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...AND 1-MSAMPLE/S DATA ACQUISITION**

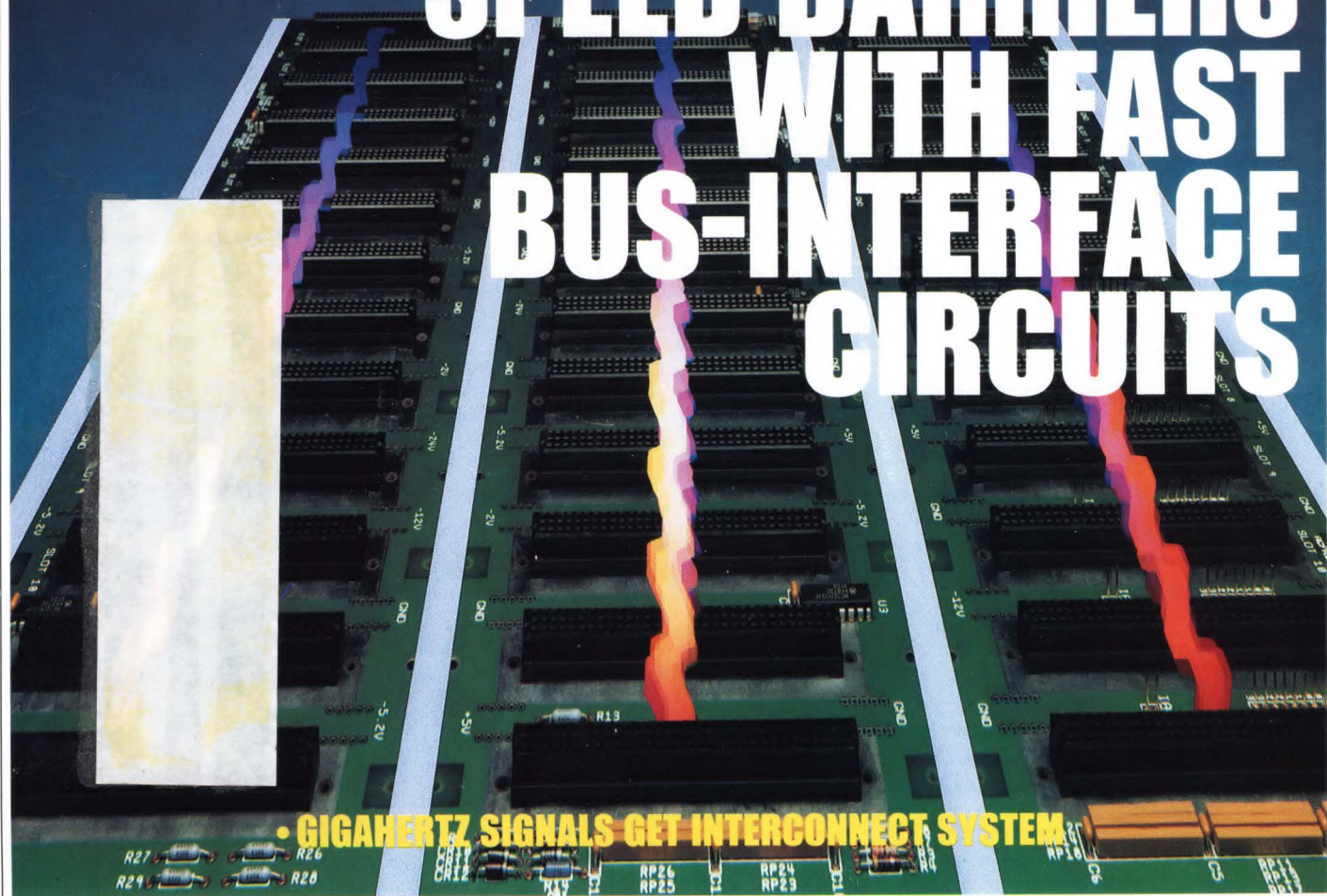
# **ELECTRONIC DESIGN**

A PENTON PUBLICATION U.S. \$5.00

DECEMBER 14, 1989

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**• GIGAHERTZ SIGNALS GET INTERCONNECT SYSTEM**





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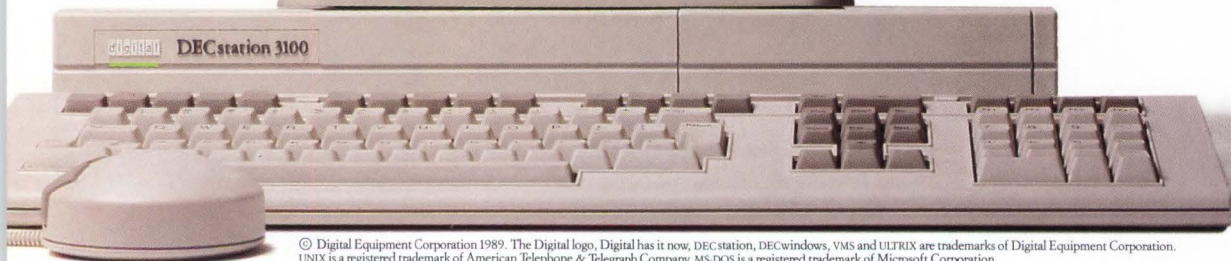
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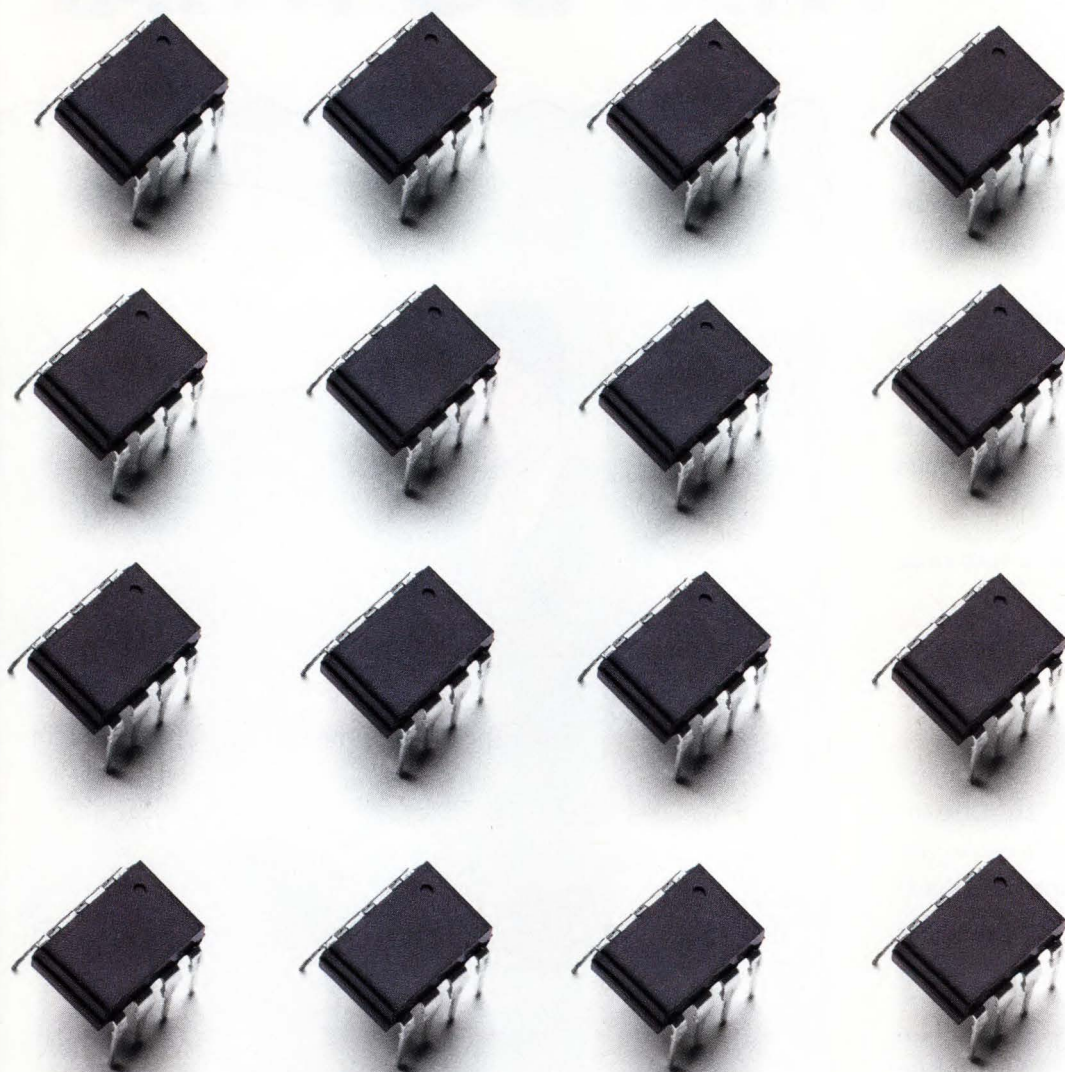
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Samsung's new Programmable Flag FIFOs extend our FIFO leadership by doing things for system performance that even the fastest conventional FIFOs can't.

Because the programmable flags let you tell the FIFO what to do. Specifically, when to empty or load. Which you can't with any other available FIFOs, because their flags aren't programmable.

#### SAMSUNG'S NEW PROGRAMMABLE FLAG FIFOs.

Part No.	Org.	Packages	Offset	Read/Write Speeds
KM75C101A	512x9	28-pin DIP	128 byte	Up to 20 ns
		32-pin PLCC		
KM75C102A	1Kx9	28-pin DIP	256 byte	Up to 20 ns
		32-pin PLCC		

What you gain, is a significant increase in system speed. Because you can tell the FIFO to empty (or load) when the data flow of the system is pausing anyway.

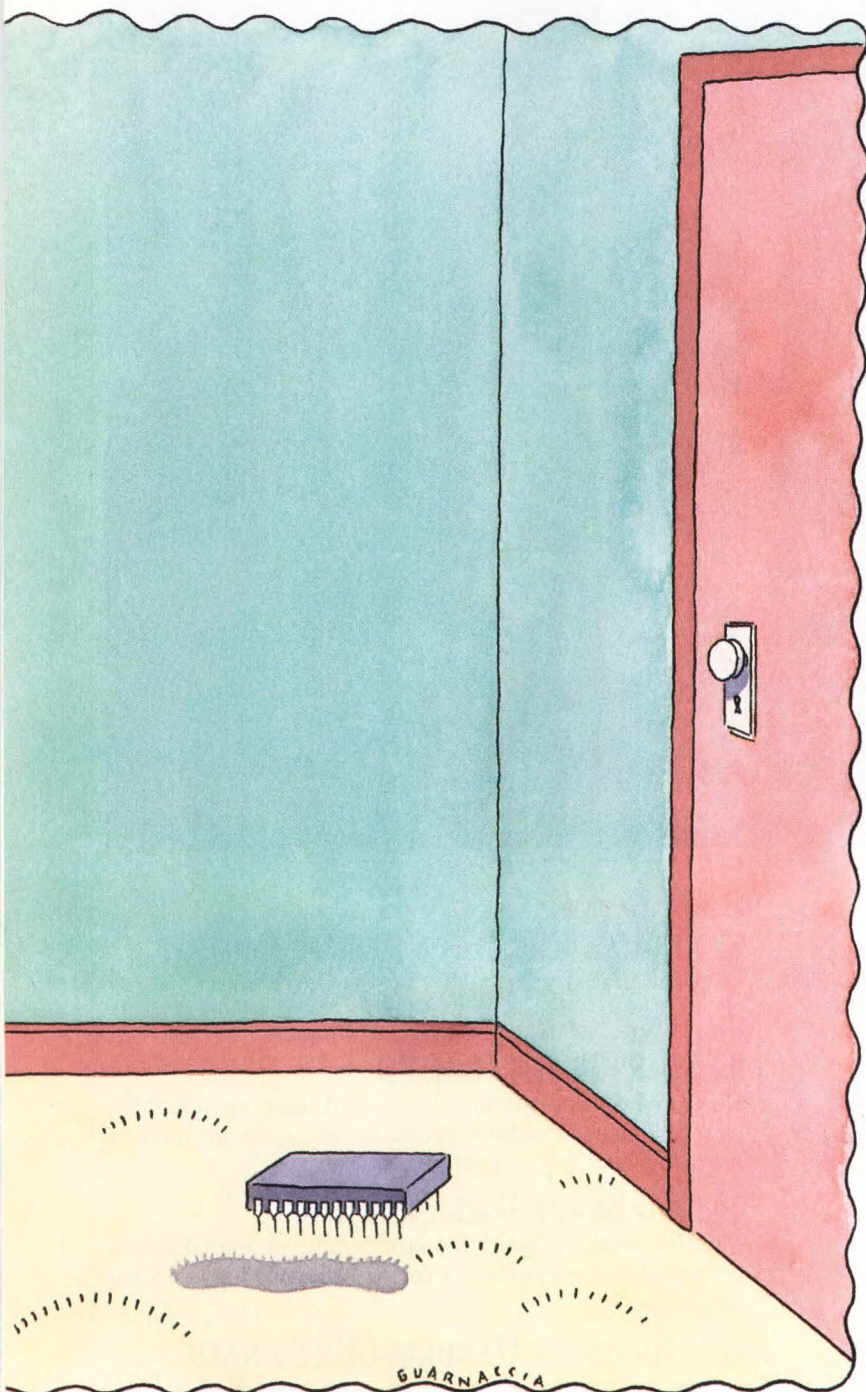
Conventional FIFOs, when the full flag is used, empty only when they're completely full. And when they *are* full, the system has to stop and wait because there's no FIFO capacity available to load into. Over a stretch of time, that stopping occurs quite often, and the result is a slower system.

Our Programmable Flag FIFOs, which can empty at the inherent data-flow pauses of the system, when it's going to have to stop anyway, solve the problem.





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There is a way to use conventional FIFOs that optimizes performance, but it does so by means of their half-full flag. The result being that one half of the FIFO is virtually never used. Samsung's Programmable Flag FIFOs give you full use of your density, and can result in your being able to gain the same usable density with fewer FIFOs.

We offer two Programmable Flag FIFOs — a 512x9 and a 1Kx9 — both with three flags: an Almost-Full Flag and an Almost-Empty Flag, with offsets that are programmable in 2-byte increments to let you define quantities; and a selectable Half-Full or Full-Empty Flag, which can let you eliminate a counter.

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Request data sheets and availability information today by calling 1-800-669-5400, or 408-954-7000. Or write to FIFO Marketing, Samsung Semiconductor, 3725 North First Street, San Jose, CA 95134.



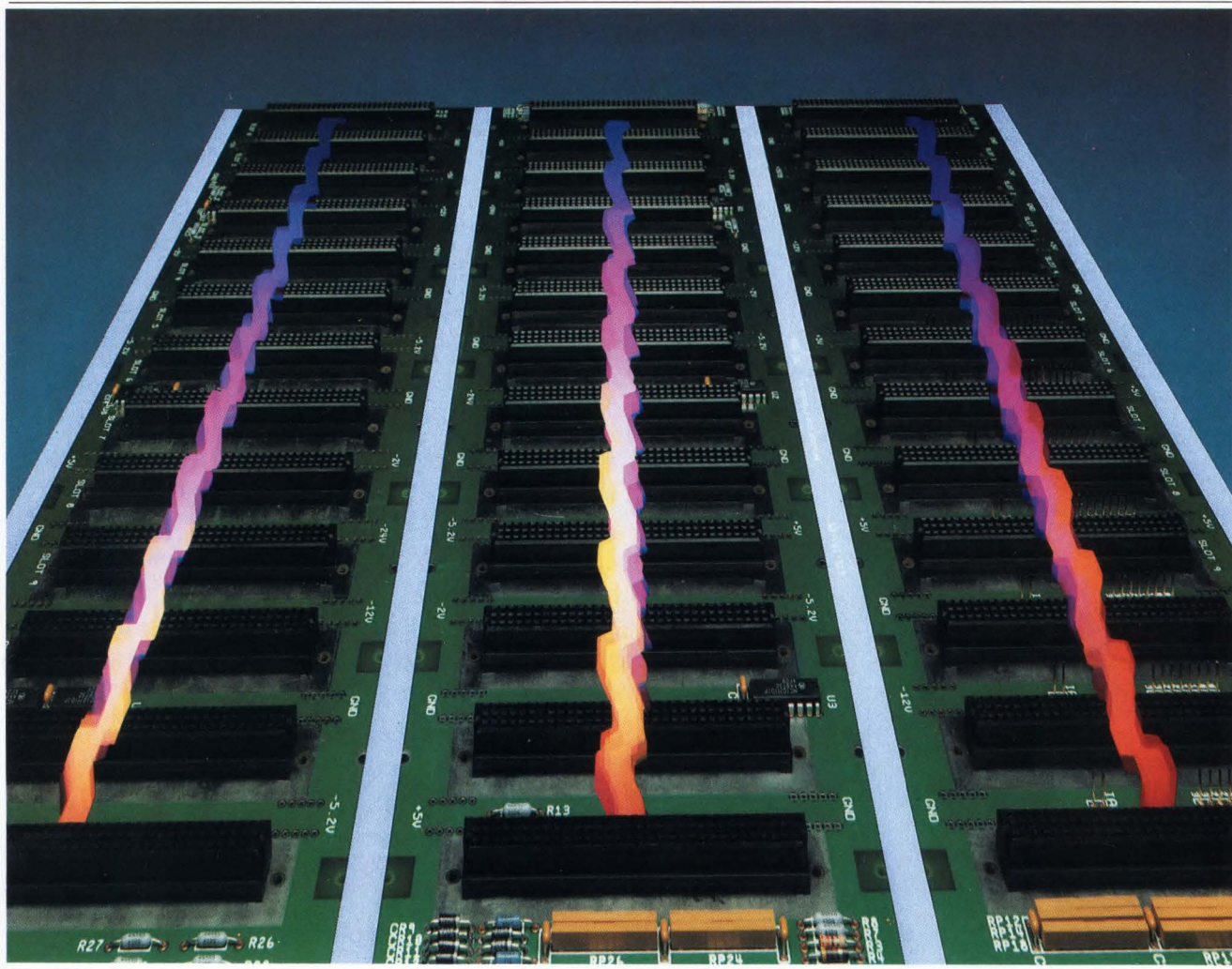
**SAMSUNG**  
Semiconductor

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# ELECTRONIC DESIGN



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CIRCLE 66

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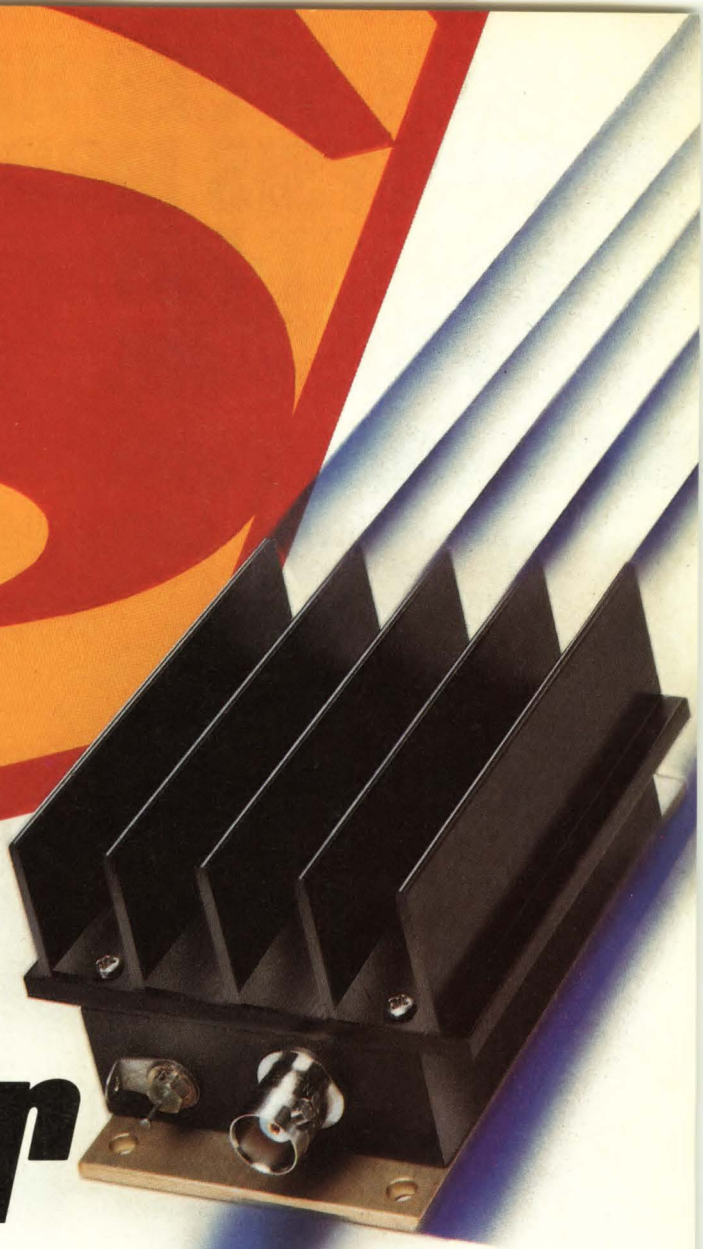
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**2.5KHz to 500MHz 250mW only \$199**

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**UNCONDITIONALLY STABLE** regardless of load

**DAMAGE-RESISTANT** built-in voltage regulator; supply voltage 24V, 0.35A

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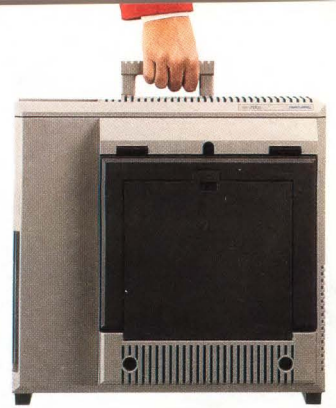


CIRCLE 84

F127 REV. ORIG.



# HIGH-SPEED HARDWARE ANALYSIS MODULES: THE NEWEST PAYOFF TO YOUR PRISM INVESTMENT.



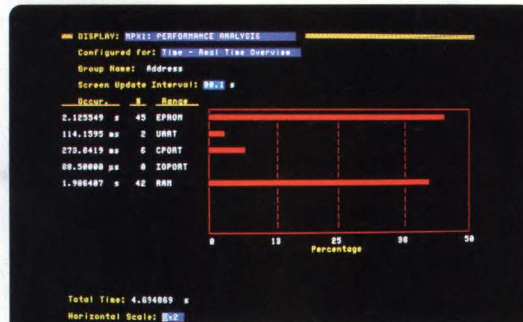
Visualize a logic analyzer that not only acquires microprocessor state and timing data, but adds emulation capabilities... real-time performance analysis... high-speed timing for hardware analysis... and more—all usable in precise, time-correlated combination. All configurable to your needs.

That's the visible edge of the Prism 3000 Series from Tektronix.

## The new dimension of integrated analysis.

<b>MPM/MPX Module</b>	Microprocessor control Real-time performance analysis 200 MHz hardware analysis 8K deep state analysis Multiple Microprocessor support
<b>HSM Module</b>	2 GHz hardware analysis 300 MHz state analysis 1.5 ns glitch capture 12K transitionally-stored memory (up to 120K effective memory)

Now, just months after introduction, Prism breaks *new* barriers with a module specifically designed for hardware analysis—for detecting glitches, metastability, and the other common problems of state machines, busses, and sequential logic.



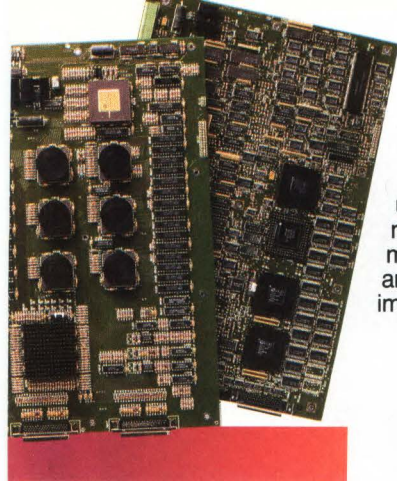
Start with up to 96 channels and the exceptional resources of Prism's 8/16/32-bit microprocessor integration modules.

You can view 200 MHz timing and 8K of state data per channel,

(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.







(Left) Prism microprocessor and hardware analysis modules are user-installable in minutes. These application modules can be configured in any combination, up to a maximum of ten cards per system.

all time-correlated and integrated on the same display. Set up state and timing sections to cross-

trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

**Push beyond microprocessor observation into microprocessor control.**

With its unprecedented Prototype Debug Tool, Prism lets you easily set breakpoints, patch registers and memory, restart the system—all without an emulator's intrusiveness.

**Use real-time performance analysis to get a true, non-statistical view of system performance.**

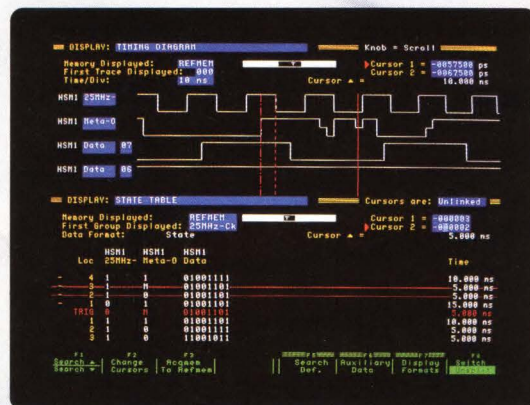
Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

**Now, with Prism's HSM high-speed hardware analysis module, you can add capabilities like 2 GHz timing and 300 MHz state analysis—and use these tools in tight time-correlation with other Prism modules.**

Detect race conditions, setup and hold time violations, and glitches as small as 1.5 ns. Switch to dual threshold or digitizing modes to get a quick look at intermittent problems like ringing or undershoot.

**Memory constraints are virtually eliminated:** the HSM's 12K of transitionally-stored memory offers the equivalent of as much as 120K of conventional memory!

(Below) The Prism HSM's dual threshold mode triggers on and displays a metastable condition. Middle thresholds are displayed as "M" in the time-correlated state table. Cursors measure the setup time violation that caused the metastable state.



**Choose from a stand-alone Prism, expandable main-frame-and-monitor, even a portable model with fold-up flat panel screen.**

Features like autoload, split-screen displays, smooth scrolling and on-line help make Prism refreshingly simple to learn and use.

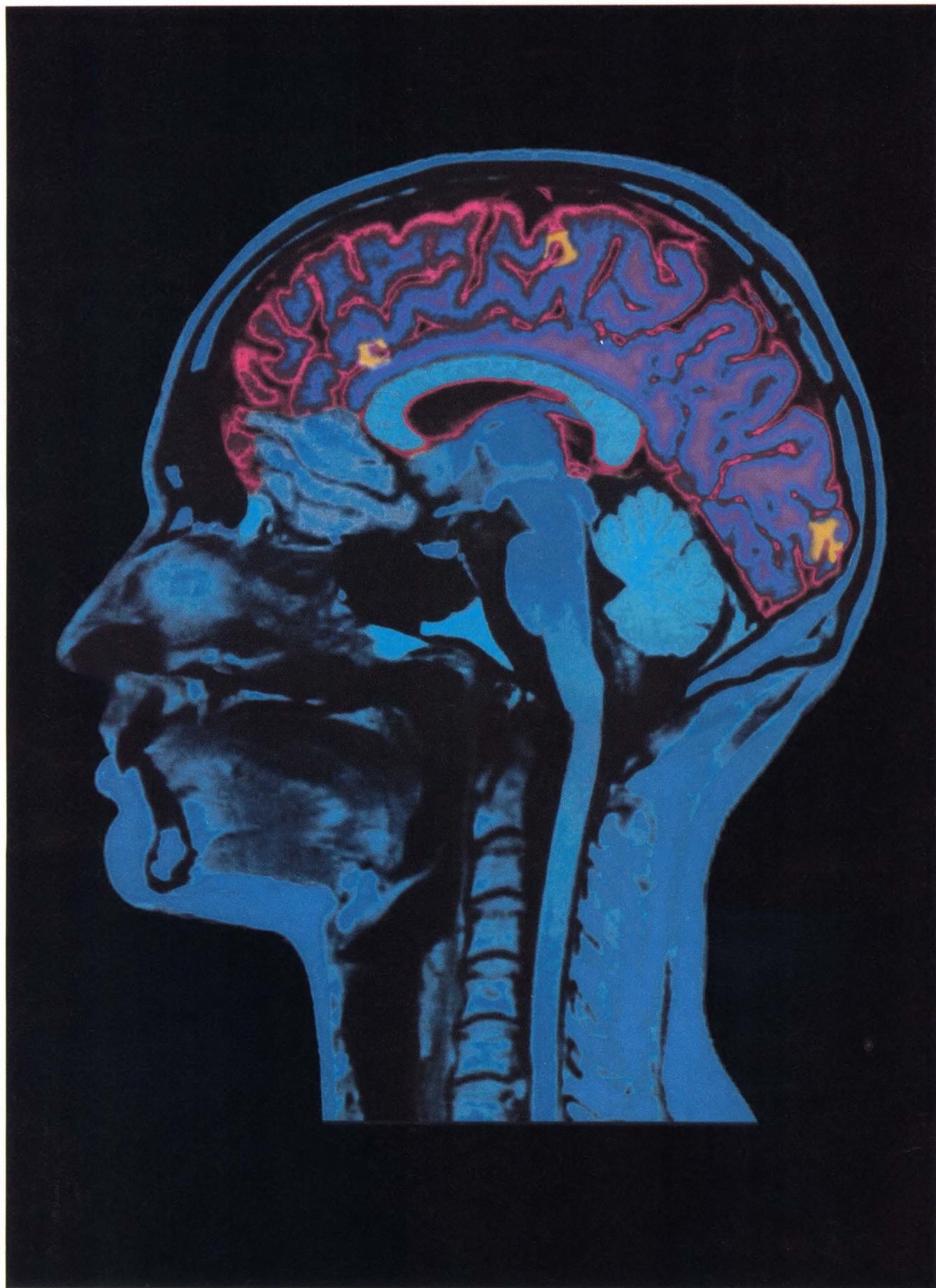
**The clincher?** You can step into this new generation of logic analyzers at prices starting at \$8600.

**Call 1-800-426-2200 for our free video demo and literature packet.** For a hands-on introduction, call your Tek sales engineer soon.



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YOUR VISIBLE EDGE  
CIRCLE 90







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The sooner a disease is diagnosed, the sooner it can be treated. Today, medical diagnostics techniques that once seemed like science fiction are pushing the electronics industry harder and faster than ever.

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CIRCLE 70

## EDITORIAL



### WHEN JAPAN SPEAKS, LET'S LISTEN

A recent issue of *The New York Times* carried an interesting pair of articles about competition between the U.S. and Japan. The first, a front-page story, reports that Perkin-Elmer's IC production equipment operation in Norwalk, Conn., the major U.S. supplier of steppers and aligners, will probably be sold to a Japanese company. The second, an editorial, acknowledges the validity of Japan's recent critique of the American system, which pointed out the problems in U.S. spending for education, the government budget deficit, the low level of investment in plant modernization, the growing number of leveraged buy-outs, management's concentration on short-term results, and laws that restrict industrial collaboration.

Perkin-Elmer certainly has the right to sell its operation. No one can force any company to remain in a business that doesn't meet its own profit goals. But this situation is particularly alarming in light of the present administration's reported cooling of interest regarding continued support of Sema-tech—a company whose major mission is to improve U.S. semiconductor production capabilities. No matter how anyone might try to explain it away, it's not good for U.S. industry to lose control of the equipment needed to produce advanced VLSI devices.

Even if we put aside the military implications, the electronics industry of the future will still be the basic element in U.S. economic success. If it's true that we are now in the information age, you don't have to be particularly insightful to see that prowess in electronics—the means by which information is communicated and processed—is the key to prosperity in the new age.

Let's listen to what Japan has to say about the way we've been doing things here for the past 40 years or more. It looks to us like they're right on the money with their criticisms.

*Stephen E. Scrupski*

Stephen E. Scrupski  
Editor-in-Chief





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1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 12, 15, 20, 30, and 40
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- **Price** (1-9 qty.)  
CAT (BNC) \$16.95 SAT (SMA) \$20.95  
NAT (N) \$23.95

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*Freq. (MHz)	Atten. Tol. (Typ.)	Atten. Change, (Typ.) over Freq. Range		VSWR (Max.)	
		DC-1000	1000-1500	DC-1000 MHz	1000-1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

\*DC-1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

#### Model Availability

SAT (SMA) CAT (BNC) NAT (N)

Model no. = a series suffix and dash number of attenuation.

Example: CAT-3 is CAT series, 3 dB attenuation.

**Precision 50 ohm terminations** from \$8.25 (1-9)  
DC to 2 GHz, 0.25W power rating, VSWR less than 1.1  
BNC (model BTRM-50), TNC (consult factory)  
SMA (model STRM-50), N (model NTRM-50)



# At about strange things happen to

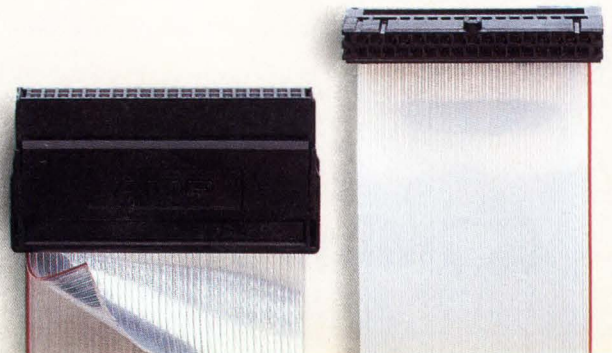
As rise times approach 3ns, all cable/  
connector assemblies become trans-  
mission line assemblies.

But not necessarily good ones.

Newer, faster logic families require  
controlled impedance cable assem-  
blies. Designed for high-speed per-  
formance. Engineered for controlled  
impedance and propagation rate. And  
manufactured for absolute conformity  
to specifications.

Creating controlled impedance  
assemblies to these standards demands  
extensive CAD/CAE use. Plus a wide  
range of specialized connector choices.  
Plus the capability to custom design  
quickly. Plus intimate knowledge of  
the various termination techniques,  
including advanced wire attachment  
techniques.

Our people are equipped to work







# $t_r = 3\text{ns}$ , ordinary cable assemblies.

with you early in the design stage to provide an optimum solution to your requirements. We help you determine the characteristics for impedance and propagation velocity that you need to match timing requirements, and the crosstalk figures you have to meet.

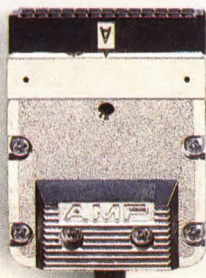
We engineer and manufacture controlled impedance assemblies in a way you'll especially appreciate.

Our manufacturing facilities are unmatched in the industry. Every assembly is individually inspected and 100% electrically tested. All work is part of the overall statistical process control system at AMP, and comes under our corporate-wide quality program.

**For technical literature and more information on high-speed controlled impedance assemblies—for logic rise times from 3ns down to the sub-nano-second range—call 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.**

CIRCLE 33

## **AMP** Interconnecting ideas





# Take a look at the fastest SRAMs in the world.

*The original  
BiCMOS  
256Kx1 at 15 ns*

*The new  
BiCMOS  
16Kx4 at 10 ns*

*The new  
BiCMOS  
64Kx4 at 12 ns*



# Wanna see them again?

---

## OUR FAMILY OF BiCMOS ECL I/O SRAMs IS GROWING FAST. AND GROWING FASTER.

---

You may have *heard* of a faster SRAM. Maybe you've even seen one — some lone sample somewhere. But there are no faster, denser SRAMs in production anywhere than these new devices from National.

We've been shipping our 256Kx1 for more than 18 months. Now production quantities are also available of our new 64Kx4 and 16Kx4. And more new SRAMs are on the way.

Our family is not only growing fast, it's growing faster. The 256Kx1's already-fast access time of 15 ns has been cut to 12 ns for the 64Kx4. And to 10 ns for the 16Kx4.

---

### THE DIFFERENCE IS BiCMOS III.

---

National's proprietary BiCMOS III one-micron process — which we've been running for more than two years — combines the speed of pure bipolar with the high density, low power, and manufacturability of CMOS.



*The original BiCMOS 256Kx1 at 15 ns*



*The new BiCMOS 64Kx4 at 12 ns*



*The new BiCMOS 16Kx4 at 10 ns*

That's why Cray Research has been one of our biggest SRAM customers. BiCMOS III gives them the best ratio of speed, power and cost per bit.

And we designed reliability into the process from the beginning. In fact, one-third of the development team had reliability as their sole responsibility.

The pay-off is a life-test failure rate of less than 50 FIT with more than 400,000 device hours. And soft-error rates as low as 20 FIT at 5.2 volts VEE. So you'll have fewer system problems and less need for error detection and correction.

---

### YOU'LL SEE THE DIFFERENCE IN SYSTEM PERFORMANCE.

---

Because of their stable memory cells, these new SRAMs tolerate skewed address signals without disturbed bits.

Customers like HiLevel Technology also report low system noise and cleaner, quieter, faster signals. This high noise immunity is due to on-chip decoupling and minimal di/dt.

Unlike other SRAMs, these devices allow almost a third of the cycle time for system skews, so you can easily design them in and achieve rated speeds.

Our ECL I/O SRAMs are input/output compatible with existing 10K and 100K ECL parts. Industry-standard pin-outs enable multiple sourcing.

---

### TAKE A LOOK AT OUR OTHER ECL PRODUCTS.

---

In addition to our BiCMOS SRAMs, we offer a variety of other ECL products in areas critical to high-speed applications. They're worth a second look.

But call today because our BiCMOS ECL I/O SRAMs are going fast. Call toll-free (800) 825-5805, ext. 115.

#### NATIONAL ECL SYSTEM SOLUTIONS

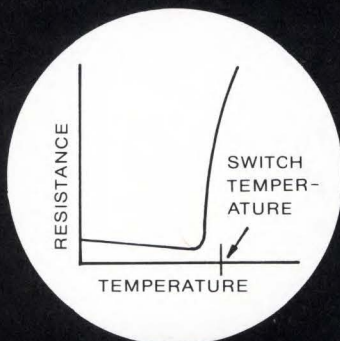
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ASPECT™ standard cells  
FGE gate arrays  
ECL PALs  
F100K digital logic

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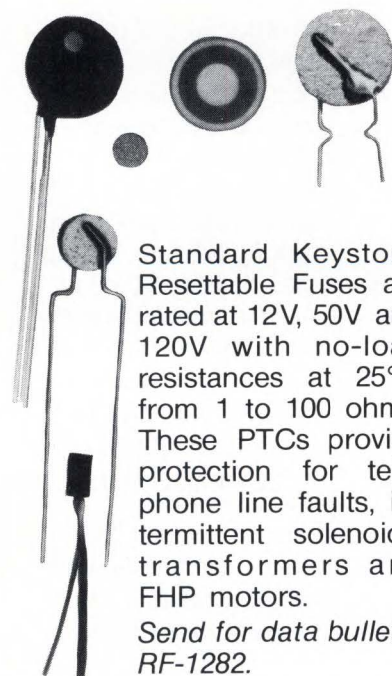


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Standard Keystone Resettable Fuses are rated at 12V, 50V and 120V with no-load resistances at 25°C from 1 to 100 ohms. These PTCs provide protection for telephone line faults, intermittent solenoids, transformers and FHP motors.

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CIRCLE 24

## TECHNOLOGY BRIEFING

### CFL WORKS FOR USEFUL EDA STANDARDS

**F**rameworks create a unified design environment by serving as a software front-end that manages different EDA vendors' application tools. Currently, many larger EDA companies offer their own frameworks. But as the design-automation industry grows, and chip and system designs become more complex, standards will be necessary to optimize the productivity of tool sets that carry a designer from concept to manufacturing. These standards must be useful and meet the needs not only of EDA vendors, but also of EDA users.



LISA GUNN  
CAE EDITOR

The CAD Framework Initiative (CFI), a non-profit member organization that was formed by the Microelectronics and Computer Technology Corp. (MCC), is currently working on establishing framework standards. The group's charter is to "develop industry acceptable guidelines for design automation frameworks that will enable the coexistence and cooperation of a variety of tools." To approach the problem from all angles, CFI includes as members chip and system manufacturers, as well as EDA tool vendors.

In September, MCC formed the CAD Framework Laboratory (CFL) to offer technical support for the framework standardization efforts of the CFI. The CFL list of targeted affiliates includes vendors of workstations, broadline CAE software, semiconductors, logic-synthesis tools, analysis tools, and layout tools, plus system houses. The proposed diversity of CFL members and broad range of services will promote the adoption of useful standards.

The CFL, working closely with the CFI, performs a variety of functions. Before a candidate CFI standard has been proposed in a key framework area, the CFL may propose selected framework interfaces for consideration as candidate standards. The laboratory will serve as an early prototyping center for all proposed candidate standards. It will provide feedback to the CFI's technical coordinating committee reporting on the effectiveness of the proposed standards based on experimental implementation and benchmarking. In addition, the CFL will supply an evaluation facility and support services so that CFL affiliates can individually test and respond to the candidate standards.

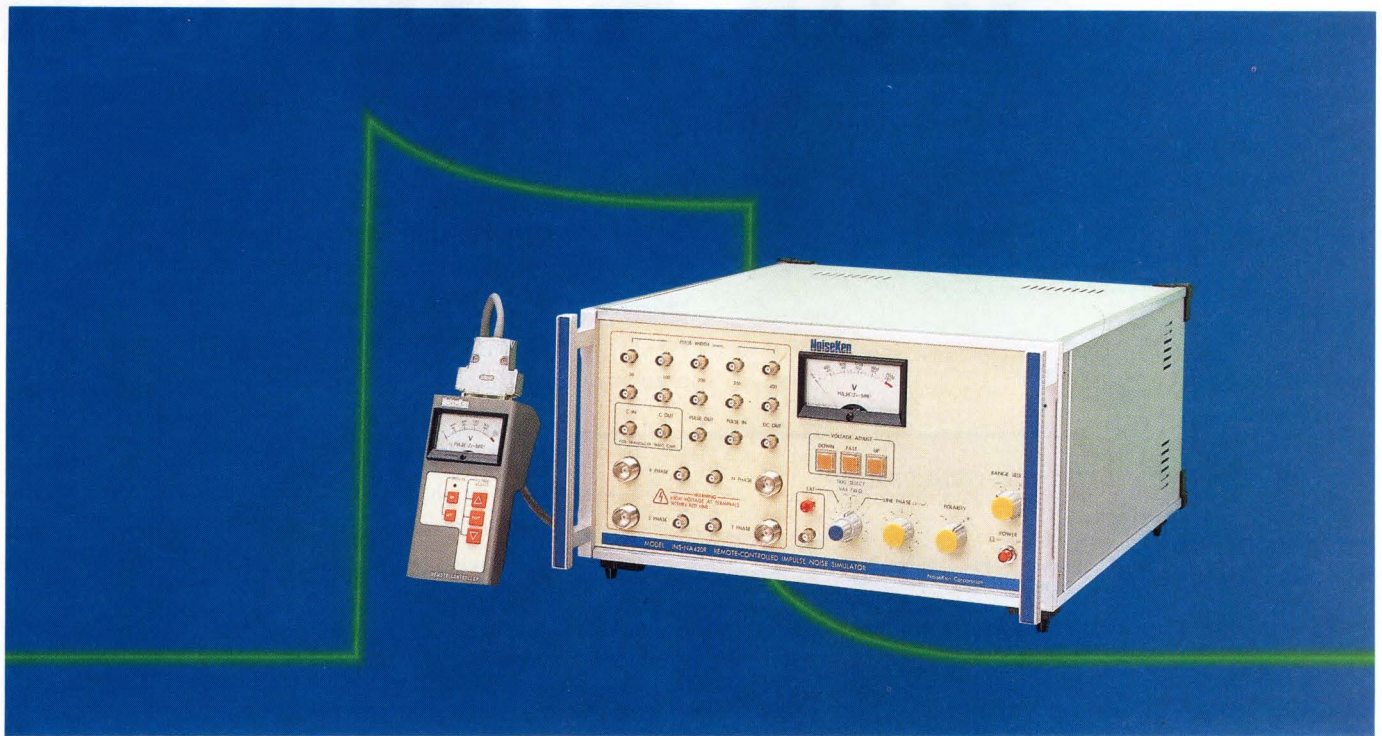
CFL also offers support for adopted standards. It develops a Verification/Validation (V/V) software system for each standard adopted by CFI. The V/V systems are used by the CFL affiliates to develop and test their own software against CFI standards.

There are two levels of membership in the CFL. Level-one affiliates receive the V/V system software in both source and object code, while level-two affiliates get only the object code. Each V/V system will support full use of the CFI standard that it relates to, but may require additional software to exercise the standard interface. CFL will supply the necessary software. MCC proprietary software will be given to CFL affiliates in object code only, and will be subject to re-use restrictions. The affiliates can also access CFL supporting technology, such as example designs, for benchmarking their use of CFI standards. Training and educational services will be offered to affiliates.

Support for CFL and CFI is growing. Last month, seven companies joined the CFL: Cadence Design Systems, Harris Corp., Hewlett-Packard, Motorola Inc., National Semiconductor, NCR, and Texas Instruments. All seven companies joined the group as level-one affiliates—the highest level of participation. More new CFL members, both level-one and -two affiliates, will be announced by year's end.



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## Introducing Oki's 4-Meg DRAMs and Modules

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OKI 4-MEG PRODUCT LINE-UP			
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MSM514100-10XX			100
MSM514102-8XX	4M x 1	Static Column	80
MSM514102-10XX			100
MSM514400-8XX	1M x 1	Fast Page	80
MSM514400-10XX			100
MSM514402-8XX	1M x 1	Static Column	80
MSM514402-10XX			100
Packaging Options Include: XX = 'JS'...350 mil SOJ 'RS'...400 mil DIP 'ZS'...400 mil ZIP			
MSC2340-XY59	4M x 9	Fast Page	80, 100
Speed Options Include: X = '8'...80 ns. '10'...100 ns.			

Oki's advanced 4-Meg DRAM technology can ease the pressure. Our space-saving 4-Megx9 single inline memory module, 4-Megx1 and 1-Megx4 DRAMs offer the problem-solving advantages you need to simplify high-density design tasks. Like quadrupling memory with our 4-Megx9. Manufactured to JEDEC standard dimensions and pin-outs like our 1-Megx9, Oki's 4-Megx9 easily replaces the 1-Meg—saving valuable redesign time, increasing reliability, and cutting costs.

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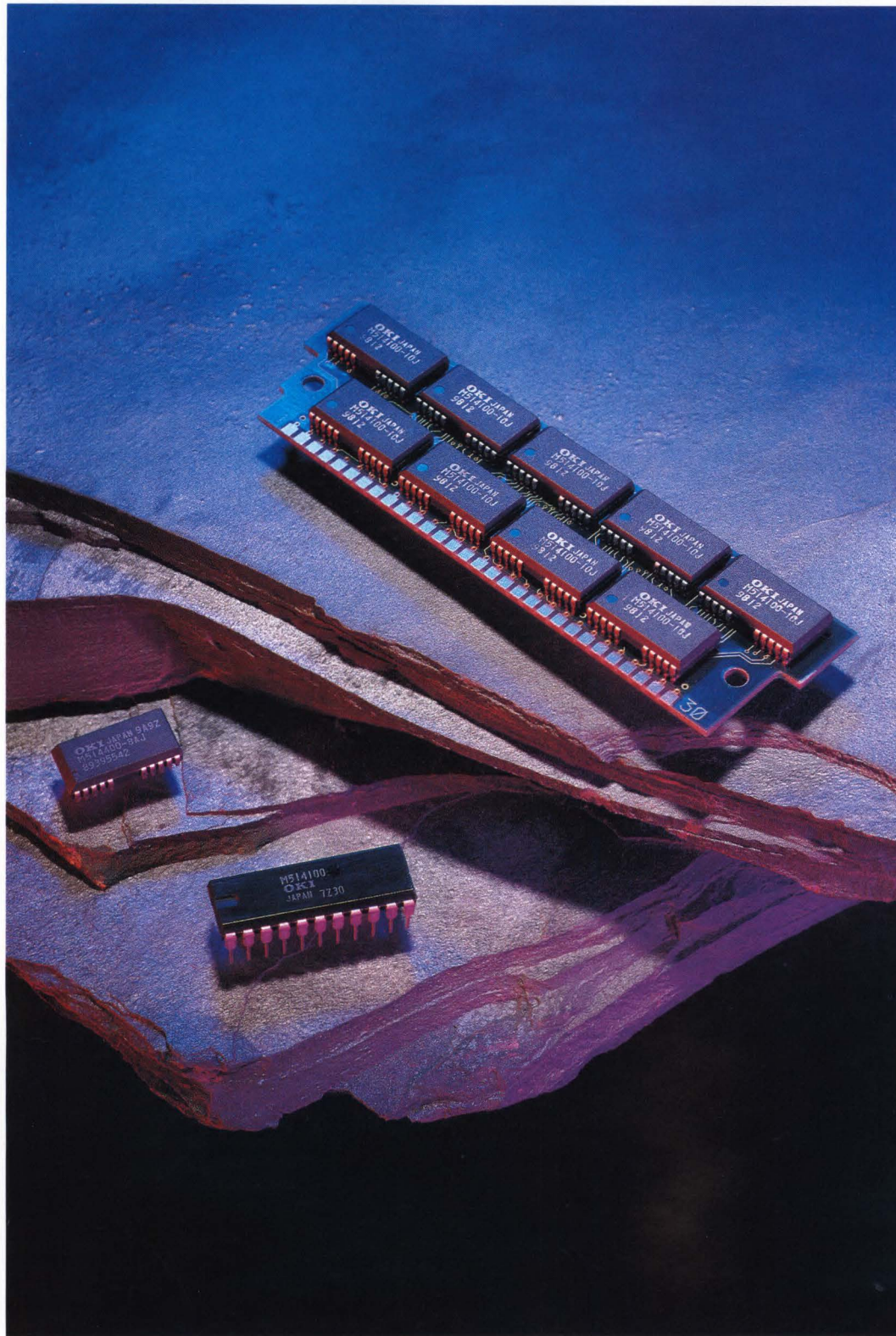
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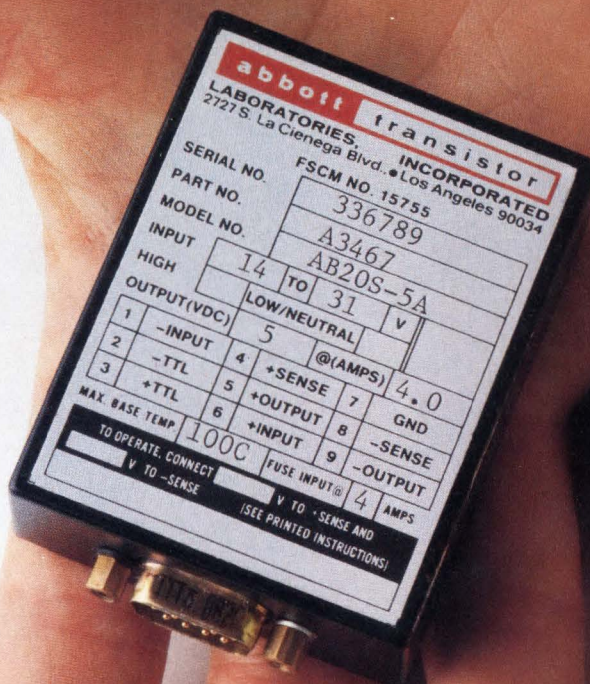




## Actual output

20 WATTS

## Actual size



## Actually meets

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## FAST CORRECTING CHIP FITS IN TIGHT SPOTS

Operating on byte-wide data, a bus-structured error-checking and correction (ECC) circuit can correct data on-the-fly at rates to 10 Mbytes/s. To fit into tight subsystems such as disk drives, the CMOS chip comes in a 28-lead plastic leaded chip carrier. Jointly defined by GT Technology Inc., Saratoga, Calif., and Everex Systems Inc., Fremont, Calif., the ECC chip corrects data records with single-burst errors in 15 to 40  $\mu$ s. What's more, it makes the corrections without microprocessor intervention. To do that, the circuit employs a modified Reed-Solomon polynomial that corrects single-burst errors up to 41 bits long. Double-burst errors up to 17 bits long are also corrected. The circuit's probability of making an improper correction is  $1.26 \times 10^{-17}$ , 12 orders of magnitude better than standard 32-bit ECC schemes. For header fields, the circuit employs a cyclic-redundancy-check polynomial to detect single-burst errors up to 16 bits long. The check also detects all 2-bit errors in header fields of 56 bytes or less. A secondary ECC in the form of a cross-check polynomial makes a secondary check on the data record to ensure data integrity. Though Everex initially developed the chip for internal use, it plans to offer it as a commercial product. DB

## STANDARD PROPOSED FOR 80860 PROCESSOR

A software standard for parallel computing on the Intel 80860 microprocessor is being promoted in a joint venture by Intel Corp., Santa Clara, Calif., and Alliant Computer Systems Corp., Littleton, Mass. The Parallel Architecture Extended (PAX) standard consists is a set of rules for hardware and software vendors to follow when developing products that incorporate the 80860 CPU. Ideally, the PAX standard will help application programs take advantage of the varying number of 80860 processors in a parallel system. It should also expand the availability of "shrink-wrapped" software for systems ranging from single-processor workstations to shared-memory, parallel-processor machines. A list of independent software vendors have endorsed the PAX standard. RN

## MODEL EXCHANGE HELPS DESIGNERS

As they grow more dependent on logic simulation, designers face the problem of finding reliable IC models. The International Technology Exchange Corp. (ITEX), Newbury Park, Calif., sees an answer in its users-helping-users approach to the problem. ITEX not only sells VHDL simulation models, but also gives users PC-based modeling tools at no charge, and encourages them to sell any models they develop. The tools from Aldec Co., also of Newbury Park, make use of an easy-to-learn VHDL shorthand. Models are sold for royalties over a network of Aldec's Susie logic-simulator users, called the ITEX Bulletin Board Network. As a result, the network acts as an international technology exchange service for sharing VHDL models. Model users can list what they need on the bulletin board. Similarly, developers can list the models that they are working on, as well as the expected completion dates. All models are qualified by ITEX before being put on line. For more information, call (800) 499-6860. LG

## CAD FRAMEWORK INITIATIVE GAINS SUPPORT

The move toward standardization in the electronic design automation (EDA) industry got a boost from Mentor Graphics Corp., Beaverton, Ore., which has agreed to share the architecture of its next-generation environment with the members of the CAD Framework Initiative (CFI). Mentor will also help develop CFI's demonstration for the 1990 Design Automation Conference (DAC) by offering the services of its OpenDoor Integration Laboratory to CFI members, free of charge. The Laboratory maintains engineering workstations and full-time OpenDoor specialists. The DAC demonstration will give the first glimpse of CFI's proposed standard data model and procedural interface, which integrates tools from multiple EDA vendors. Mentor Graphics will demonstrate the procedural interface between its tools and those of other vendors. OpenDoor will employ CFI-endorsed interface standards as soon as they are available. LG

## MODELS EMERGE FOR PGAS

The flexibility of field-programmable gate-array circuits makes it difficult to model them in large multichip simulations. However, Xilinx Inc., San Jose, Calif., shared the inner workings of its RAM-based programmable arrays with Logic Automation Inc., Beaverton, Ore., to create the first behavioral models for the Xilinx XC2000 and XC3000 FPGA families. To develop the models, Logic Automation took a new approach to the simulator: A model holds all events and node transitions within itself, rather than lining up those events in the main simulator's event queue. That approach avoids overloading the main simulation program by preventing too many events from ending up in the queue. In addition, the software permits multiple windows to be opened, so designers can "look" inside the logic. To help designers analyze a chip's operation, each window contains



user-defined groupings of logic elements. The windows can be set up for one chip or across multiple chips when system simulations are done. Data in the windows can even be changed on the fly, and breakpoints can be set, even across multiple chips, to reduce the time needed to debug a circuit. DB

## MICROCONTROLLER USERS CAN MEET THEIR MATCH

One-chip microcontrollers usually come in many configurations, so users can choose the cost and features that match their needs. With that variety, however, comes confusion for designers who may not know every available version. This is the problem that the microcontroller product group of Motorola Inc., Austin, Texas, found after examining many of the chip requests coming in from potential customers for its 8-bit 68HC05 family of microcontrollers. To solve that problem, Motorola developed a disk-based questionnaire that runs on IBM PCs and compatibles or Apple Macintosh computers. With the electronic questionnaire, designers can specify their "ideal" microcontroller. After receiving a completed questionnaire, Motorola's engineers run it through an expert-guided analysis program that tries to match up the requirements against a standard chip and against other incoming requests. If a match is found with any of the over 40 versions of the 68HC05 controller, a standard part can be used; if not, a customer-specific chip can be created with the company's design automation system by "cutting and pasting" features from other chips. If Motorola finds that the chip has good market potential, and the customer is willing to release the design for general sale, there's no development charge for the customization. DB

## SHRINK-WRAP UNIX SUPPORTS INTERFACE

In a move to support a standard Unix operating system on platforms built around its 80386 and 80486 microprocessors, Intel Corp., Hillsboro, Ore., will sell and support a "shrink-wrap" version of Unix software. The prepackaged software accommodates the Intel/AT&T-developed Applications Binary Interface (ABI). The ABI is a software standard that makes it possible for applications to run on any computer, regardless of its manufacturer. More than 20 independent software and hardware vendors, and computer manufacturers say that they are supporting ABI. To date, the shrink-wrap line includes Unix System V/386 Release 3.2, as well as NFS, TCP/IP, the X Window System, and Locus Merge programs. Unix System V/386 Release 4.0, which includes enhancements to Revision 3.2, as well as the Openlook and the OSF/Motif graphical user interfaces, will be available in the first quarter next year. RA

## HAND-HELD GAME DISPLAYS ARCADE-QUALITY GRAPHICS

A pair of custom ASICs, an LCD controller, and a 3.5-in. full-color LCD screen are some of the engineering achievements behind a new hand-held video game. Featuring high-resolution graphics and animation, the game weighs 1 lb. and is slightly larger than a videocassette. One of the two ASICs contains an 8-bit microprocessor running at 4-MHz (clock rates to 16 MHz are possible) and a 16-bit graphics engine. With a screen resolution of  $160 \times 102$  pixels and up to 16 simultaneous colors drawn from a 4096-color palette, the Lynx from Atari Corp., Sunnyvale, Calif., displays graphics comparable to that found on TV and arcade games. The advanced graphics also lets a player zoom in on an infinite number of screen pixels to make them larger or smaller, and to change image size and depth for better perception and a highly dynamic image. The unit operates on six AA batteries for up to 5 hours of play and employs credit-card-sized 1-Mbyte ROM game cards. A novel feature links up to eight of the games over a network and lets eight players participate in simultaneous interactive games. RA

## COMPANIES COOPERATE TO IMPROVE OPTOCOUPERS

Bidding for a leading position in optocoupler technology, the Hewlett-Packard Co., San Jose, Calif., and the Philips Components Division, Eindhoven, the Netherlands, have agreed to jointly develop and manufacture a new series of optocouplers. The agreement enables both companies to combine their strengths in building optocouplers. HP will contribute its expertise in high-speed and high-performance optocouplers; Philips, its know-how in high-voltage, high-insulation packaging. The new package is wide-bodied and mechanically robust, with 400-mil-center leads instead of the 300-mil leads typically used. The series will include five models: the CNW135 and 136 high-speed transistor-output optocouplers, the CNW137 high-speed optically coupled logic gates, and the CNW138 and 139 Darlington-output, high-gain optocouplers. Samples of the first products will be available this month. According to the agreement, both companies will retain exclusive rights to proprietary technology. Jointly developed technology, however, will be owned by both companies. JG



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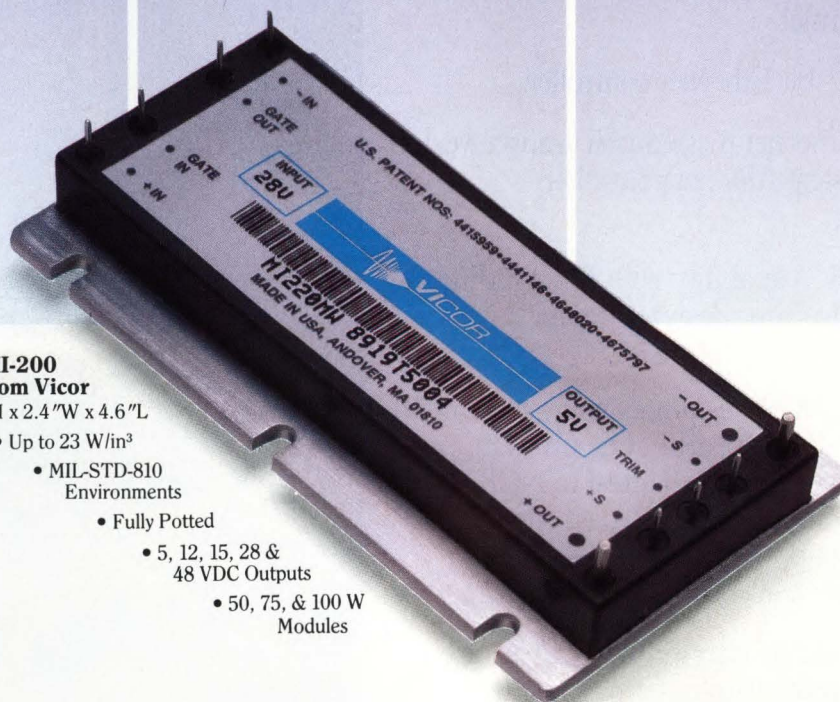
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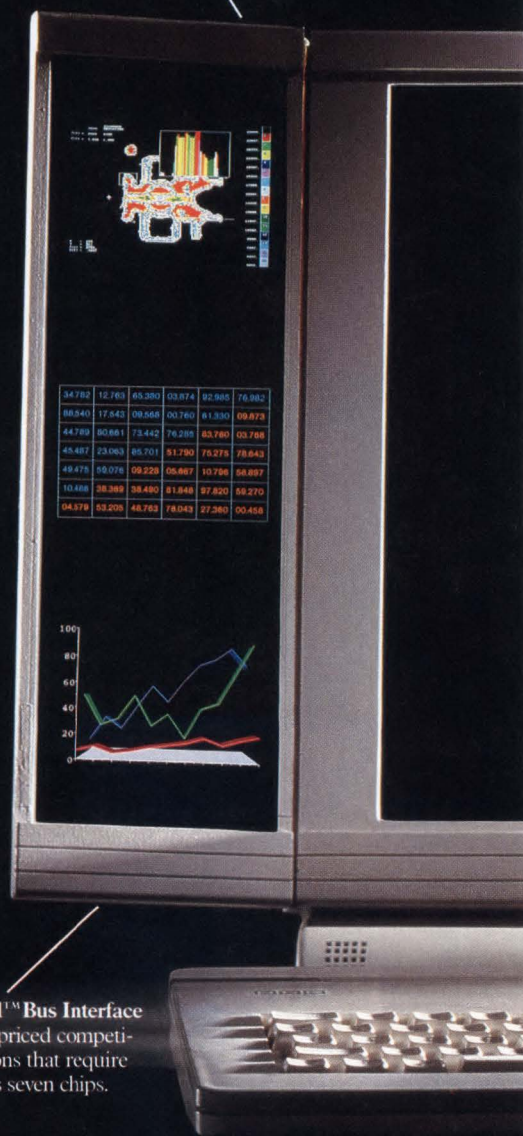
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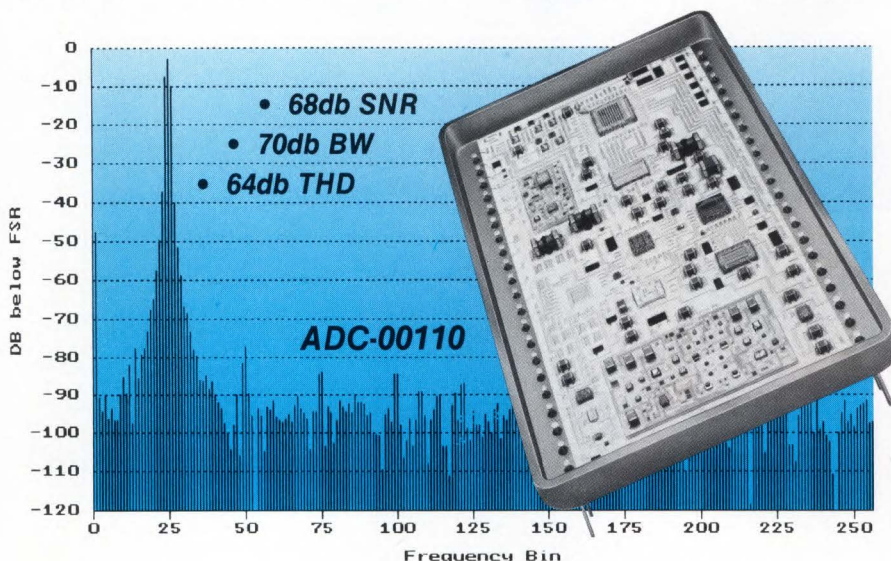
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DDC is pleased to announce that circuit and component advancements have enhanced the performance of its leadership 12-bit 10 MHz sampling A/D converter hybrid. The specification improvements include key dynamic parameters which are of particular interest to radar and infrared equipment designers. The ADC-00110 is now available with guaranteed no missing codes and with specifications for Signal-to-Noise Ratio (SNR); Total Harmonic Distortion (THD); and Bandwidth of 68.5 db, 64 db, and 70 MHz respectively.

The ADC-00110 contains a track/hold amplifier, a 12-bit A/D converter, a precision DC reference, data registers, tri-state buffers, and timing circuits in its small 46 pin plug-in package. Its output registers and tri-state buffers provide a simple interface to most commonly used CPUs. Since all timing is self-contained, only an

encode command is required to start its conversion cycle. Both TTL and ECL logic compatibility models are available. In addition, its  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range and screening to MIL-STD-883 are uniquely suited to the most demanding military and industrial DSP applications.

The ADC-00110 is implemented with a 2-step A/D conversion algorithm, which operates as follows: First, the track/hold samples and stores the analog input signal, after receiving an external start command. Then, a flash ADC generates a coarse encode of the sampled voltage and stores its 6 bits in the MSB register. At the same time, a high-speed DAC and amplifier convert the 6 bits to an analog voltage, which is subtracted from the original input. Next, a second flash ADC generates a fine encode of the subtracted voltage and stores these 8 bits in the LSB register. Finally,

the contents of the 6 bit MSB and 8 bit LSB registers are combined in a digital error correction circuit to yield the 12-bit output. All of these steps take place at a 10 MHz rate.

High speed, wide operating temperature range, and small size make the ADC-00110 ideal for numerous digitizing requirements such as in radar and sonar, electronic warfare receivers, digital signal processors, medical and nuclear instrumentation, and high speed data acquisition. **Learn more about this newly improved hybrid by calling Mike Johnson at toll-free (outside N.Y. state) 800-DDC-1772 or any of the regional offices listed below.** □

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## LATEST VERSION OF BIPOLAR PROCESS SQUEEZES 100,000 GATES PER CHIP

**D**esigners using standard-cell design techniques can now pack up to 100,000 bipolar gates on one chip. That's the promise of the latest revision of National Semiconductor Corp.'s advanced single-polysilicon, emitter-coupled technology—Aspect III. With drawn dimensions down to 0.8  $\mu\text{m}$  minimum, the process cuts the speed-power product to 50 femtojoules/gate.

Individual gates built with the Aspect III process will offer three speed-current choices: sub-50-ps delays with a switching current of 1 mA, 80 ps at 0.2 mA, and 130 ps at 0.1 mA. By shrinking the minimum feature size to 0.8  $\mu\text{m}$ , which is down about 50% from the previous version of the process (Aspect II), designers at the Santa Clara, Calif., company were able to shrink the area that's occupied by a gate proportionally—just 0.8 to 1  $\text{mil}^2$ .

As with previous versions of Aspect, the self-aligned process forms contactless silicided transistors with polysilicon emitters. Titanium-silicide is used for some local connections to reduce routing complexity on the first layer of metal.

With the local silicide connections and contactless structure, Aspect keeps the area of a typical gate to less than half the area of one built with a conventional contact structure and no silicide, estimates Hem Hengarth, the process development manager at National Semicon-

ductor.

Moreover, with lower values of the intrinsic parasitic elements, Aspect transistors can operate with a 14- to 16-GHz maximum cutoff frequency. Those transistors, in turn, can form flip-flops having typical toggle frequencies in the 5-to-6-GHz range. At the same time, the power per gate is less because losses are reduced: A typical internal gate dissipates from 0.2 to 0.4 mW.

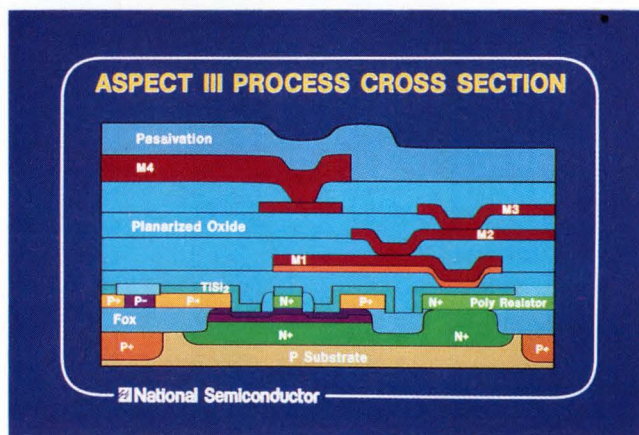
To interconnect all of the gates in a large chip, National's engineers developed a planarization process that smoothes the intermetal dielectric, which makes it possible for four layers of metal (see the figure). Consequently, signif-

icantly compact chips can be created because circuits require less space between them for wiring tracks.

National recently released a standard-cell library for Aspect III. It contains most of the 175 macrocells of the Aspect I li-

brary, as well as 25 larger megacell macros that include such blocks as ALUs, multipliers, and RAM. Single-port RAMs can access in as little as 2 to 3 ns, while multiport register files have 3- to 5-ns access times. Gate arrays with 200 to 50,000 gates are slated for release in the second half of 1990.

DAVE BURSKEY



## INTERPOLATORS PUT 10-BIT 75-MHz A-D CONVERTERS ON 8-BIT DIGITAL PROCESS

**B**y incorporating an interpolating architecture, Chuck Lane, design engineer at Analog Device's Computer Labs Div., Greensboro, N.C., built a 10-bit flash a-d converter IC with 512 comparators instead of the usual 1023. Moreover, interpolation made it possible to create the converter on a fast, dense, digital process that could not otherwise yield enough die per wafer—with 10-bit accurate comparators—to be economically viable. With its sampling (conversion) rate of over 75 megasamples/s, it's the fastest 10-bit a-d converter yet. The chip, which will sell for under \$200, will replace a \$1500 5-by-7-in. board that's half as

fast.

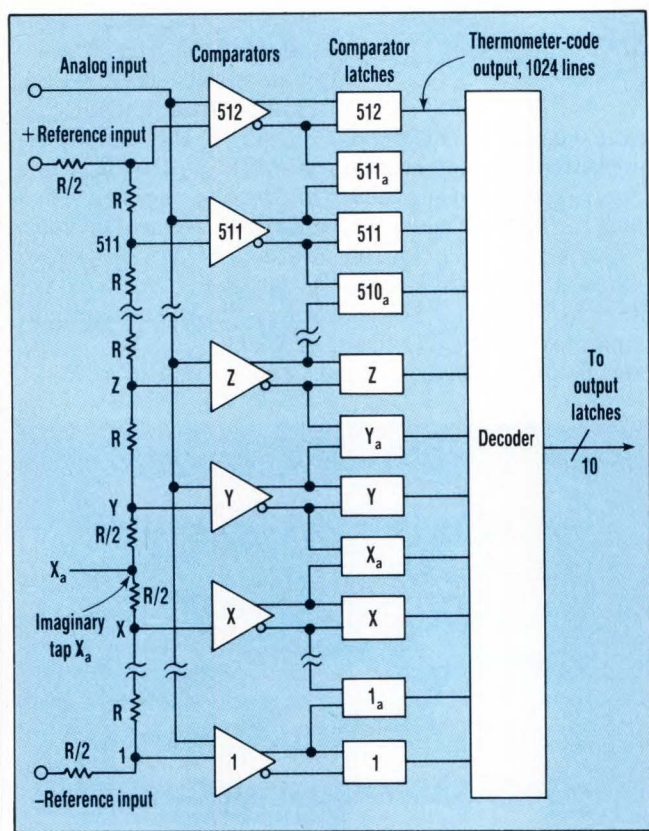
At first glance, the converter circuit looks like any other flash device: The taps of a reference resistor-divider string connect to the inputs of a comparator array (see the figure). Each comparator in turn drives a strobed latch and the analog-input bus drives the other side (the input) of the comparators. But only 512 comparators are used, and the circuit has an additional latch between all of the adjacent comparators' outputs. These latches are the interpolators.

To understand how the circuit works, assume that the analog input voltage, once strobed in, causes the outputs of latch X and all of

the latches below to be a "one", and causes the outputs of latch Y<sub>a</sub> and all of the above latches to be a "zero." Then, all of the comparators below comparator X will be in saturation, showing a "one" at their noninverting output. And those above comparator Y will be in saturation, showing a "one" on their inverting output. Comparators X and Y, however, will be operating in their linear region. They will be amplifying the difference between the analog input and their respective tap on the reference divider.

In that case, latch X<sub>a</sub> acts as a comparator, comparing the inverting output of Y with the noninverting output of X. If the analog





input is less than the voltage that would appear at the imaginary tap ( $X_a$ ) on the divider (that is, the voltage half way between tap A and tap B), latch  $X_a$  will show a "zero" at its output. However, if the analog input voltage is greater than that at tap  $X_a$ , latch  $X_a$  will show a "one."

Just as all flash converters, the 1024 thermometer-code output lines from the latches feed a decoder that converts them to a 10-bit binary word. From there, they go to output latches (a word in thermometer code consists of a string of consecutive ones adjacent to a string of all 0s, or vice versa.)

To be small enough for economic viability, a 10-bit flash converter must fabricate on a dense digital process. The converter is built on an ECL process with triple-layer metal. The effective

emitter area of the process' npn transistors is 8  $\mu\text{m}^2$ , and gate delays run

300 ps with 100  $\mu\text{A}$  of collector current. But this fast bipolar digital technology runs off 5 V rails, which means a least significant bit will be significantly less than 5 mV.

To get under 1 LSB of differential non-linearity (DNL) error, the base-emitter voltages of the transistors that form the comparators must have a  $3\sigma$  match within 1 LSB. That requirement demands a similar match among transistor areas. This degree of match is achieved routinely with precision analog processes. The same is not true for dense digital logic.

Enlarging the transistors improves area matching, but it does so at the expense of dynamic performance because transistor capacitance grows with area.

The interpolation architecture also reduces the DNL problem. In a tradi-

tional flash a-d converter design, a device mismatch of 1 LSB in a comparator results in one missing code and one code-width appearing 2 LSBs long, assuming adjacent comparators are ideal. Interpolation spreads the 1 LSB error over four codes; two of them 0.5 LSBs long, the other two 1.5 LSBs long.

What else does this interpolation offer users besides price performance when this converter—the AD9060—becomes available? For one thing, it cuts the input capacitance in half. In addition, the comparators employ a cascode design that further reduces the input capacitance and keeps it virtually constant. This makes it much easier to drive with a 35-MHz analog signal. The value typically varies just 2 pF (between 45 and 47 pF) over the input voltage range,  $\pm 1.75\text{ V}$ .

FRANK GOODENOUGH

## PACKAGE OF SPARC BOARDS AND SOFTWARE BECKONS WORKSTATION MANUFACTURERS

Usually, the time-consuming job of designing a RISC-based workstation or system, from pc-board layout to developing firmware, must be duplicated by every company that undertakes the task. Now, however, a company can cut its startup time by up to 75% by licensing a manufacturing package of Sparc-processor-based hardware and software. By developing the manufacturing package, Fujitsu Microelectronics Inc., San Jose, Calif., hopes to greatly increase the number of companies building Sparc (scalable processor architec-

ture) systems.

The hardware includes VMEbus boards consisting of CPU, memory, and peripheral boards, each in 6U double-high format. Together, they contain all of the basic workstation functions. To complement the boards, Fujitsu's advanced products division joined with three California companies—Insignia Solutions, Sunnyvale; Interactive Systems Corp., Santa Monica; and Via Technologies Inc., Fremont—to round out the boards with various software packages and, eventually, higher-integration chip sets to further reduce system costs.

Under SunOS—Sun Microsystems's Unix operating system—the board set executes 12 to 15 MIPS. To let companies get a jumpstart on building the boards and integrating the software into the system, the manufacturing package contains all of the specifications, layout data, drawings, bills of materials, and related documents that a company needs to give to its manufacturing department to build a Sparc-based system. Or companies can modify the manufacturing package to customize the hardware.

The CPU card contains an S-20 or S-25 Sparc re-



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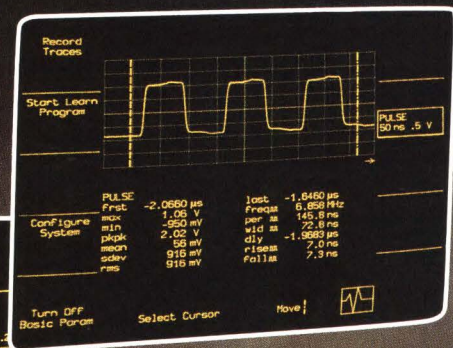
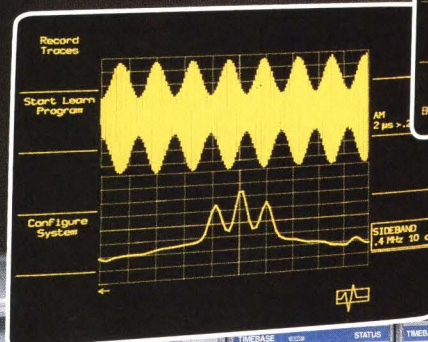
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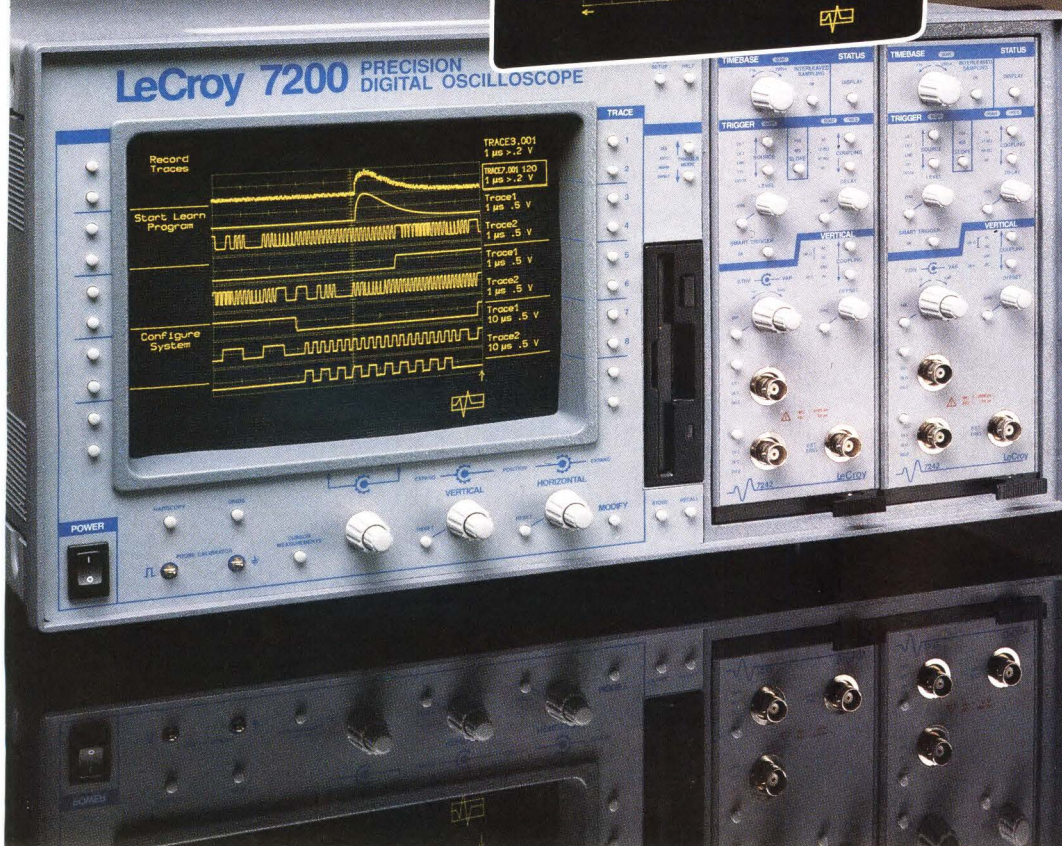
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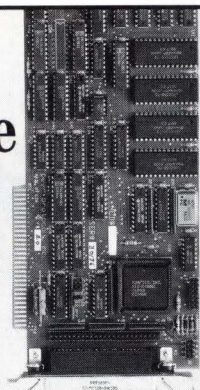
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CIRCLE 83



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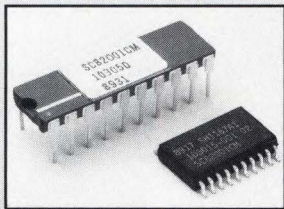


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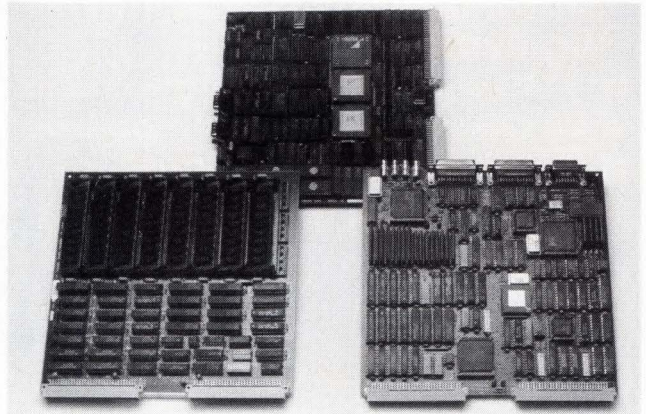
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CIRCLE 49

## TECHNOLOGY ADVANCES



duced-instruction-set-computer (RISC) processor, its memory management unit, a Weitek 3170 floating-point math unit, 64 kbytes of cache memory, 256 kbytes of EPROM, a real-time clock, two RS-232 ports, a private-memory local bus, and a VMEbus interface. The memory card holds 8 to 16 Mbytes of parity-checked dynamic RAM, control logic for the cache and dynamic memory, a private-memory local interface, and the VMEbus interface logic.

The last board contains a montage of hardware that seems only to lack the proverbial kitchen sink. The hardware includes an Ethernet interface; a second serial port; a four-channel DMA controller; a SCSI port for peripheral control; and a Sun-compatible video graphics controller, video memory, and RGB outputs for displaying a 1152-by-900-pixel image.

The initial software from Insignia and Interactive starts with Insignia Solutions' SoftPC, a 100% software emulation of an IBM PC. That package opens the Sparc system to over 50,000 MS-DOS application programs. The software comes installed with MS-DOS 3.3; MS-mouse, a

mouse-driver to emulate the Microsoft mouse; GW Basic; and Slave PC, a routine that makes it possible for direct-cable data transfers between the Sparc host and a PC.

To make the hardware compatible with Sun software, Interactive Systems created a version of SunOS to run on the VMEbus boards. The operating system includes NFS, Sun's network file system; C and Fortran compilers and their associated software development tools; and SunView, Sun's proprietary windowing system. By the second quarter of 1990, X11 and News, as well as the OpenLook and Motif graphical user interfaces, will be supported.

Also on the horizon are hardware cost reductions from Via, which is planning a chip set that will make it possible to pack all of the basic system features onto one motherboard. Via will produce chips and a comprehensive manufacturing package for the motherboard. So far, several companies have already committed to the manufacturing package approach and expect to release systems in the second quarter of 1990.

DAVE BURSKEY



# FAST BUS INTERFACE CHIPS TACKLE TOUGH SYSTEM DESIGN

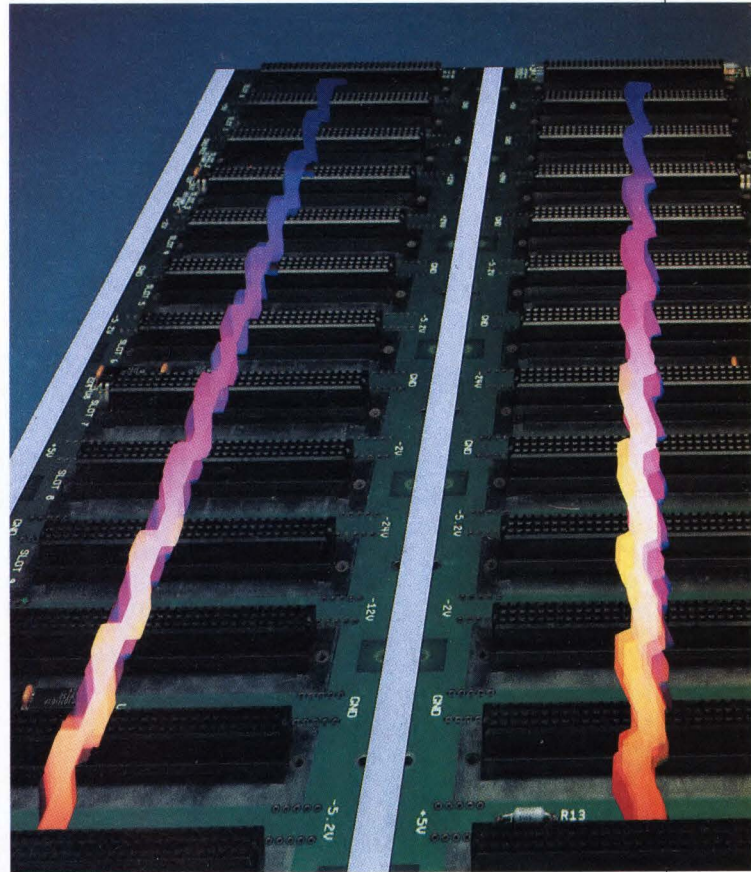
BY TRIMMING SYSTEM DELAYS,  
BUS INTERFACE CIRCUITS  
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DAVE BURSKY

**A**s digital systems up their clock speeds, data throughout the system must move at ever faster transfer rates to keep the processors and subsystems running at top speed. And not only will circuits be pushed to their limits, but multiple chip technologies—ECL, TTL, CMOS, biCMOS, and GaAs—will often be utilized in the same system to optimize the performance of each subsection.

With such a mixed bag of circuit types (whether they're custom chips or catalog circuits), a raft of bus buffers, level translators, and other bus interface chips will be needed to tie everything together over system buses. Many chip manufacturers have responded to these needs by developing multiple families of bus interface circuits that range from simple buffers to bidirectional latched transceivers and bidirectional ECL-to-TTL translators. In addition, new generations of more complex interface chips that throw in such system functions as parity generation and checking are also appearing.

Whether the buses that shuttle the data are standard structures—such as VME, Multibus, NuBus, Micro Channel, Futurebus, and others—or proprietary 64-, 128-bit, or wider buses in large computers, the interface circuits that tie the subsystems together play a key role in system performance. During the 1970s, a typical logic catalog contained roughly 80% logic circuitry



and around 20% was devoted to bus-interface circuits. Today, similar catalogs are almost evenly divided because many more types of interface circuits were added to deal with various buses.

In the highest-speed system subsections, TTL-to-ECL and ECL-to-TTL translators and ECL transceivers with 1.3-to-3.5-ns propagation delays introduce the smallest speed penalty for ty-



## COVER: BUS INTERFACE CHIPS

ing subsystems into one another. This speed-critical area has attracted seven major suppliers: Fujitsu, Motorola, National Semiconductor, NEC, Philips (Signetics), Sony, and Texas Instruments.

Bipolar TTL chips in the FAST family (originally developed by Fairchild Semiconductor Corp. and called the Fairchild Advanced Schottky TTL series) and the latest advanced CMOS interface circuits (categorized under various family names, such as 74FCTA, FCTC, PCTA, and others) keep typical propagation delays to between 3.5 and 8 ns (depending on the interface function). Some of the latest advanced CMOS circuits and some of the mixed bipolar-CMOS (biCMOS) interface chips cut the propagation delay times to less than those in the FAST family while operating at lower power levels.

The short delays of the lower-power CMOS chips make it possible for them to compete speed-wise with the FAST family, the highest-speed bipolar TTL circuit series now in production. However, though the fastest CMOS chips may match or exceed

many of the FAST specifications for an identical function, the CMOS chips are considerably more expensive. The CMOS circuits might command a premium of 300% to 400% over the price of the bipolar chips, according to Bill Hall, manager of advanced CMOS logic at National Semiconductor.

Slightly slower CMOS bus interface circuits—chips in the FACT, ACT, FCT, and other families—insert propagation delays of 6 to 10 ns. More moderate bipolar TTL chips, such as those in the AS and ALS series, typically have 5-to-8-ns delays. These CMOS and TTL circuits are still the bread and butter of today's bus interface designs, but they're slowly giving way to the faster chips as system speeds increase.

### THE SPEED LEAD

As system buses get wider and faster, ECL interfaces supply some of the cleanest signal handling because the circuits were designed for controlled-impedance pc boards and backplanes. Most ECL circuits, however, are designed for 50- $\Omega$  systems,

and a new generation of ECL interface circuits will be needed to handle the higher-performance doubly terminated systems with 25- $\Omega$  dc impedances (*Fig. 1*). Such new circuits must drive the higher, 128-mA currents that will be placed on the bus. In these systems, the driver "sees" a 50- $\Omega$  ac load because the board is designed with 50- $\Omega$  transmission-line techniques. That driver must source and sink enough current to maintain standard ECL dc levels into an effective 25- $\Omega$  dc load (the two 50- $\Omega$  termination resistors in parallel).

A pair of 9-bit-wide transceivers developed by Signetics to handle the high-current buses (the 100990 and 100790, for 10K and 100K logic families, respectively) insert as little as 1.3 ns into the signal path. Both chips include controlled-ramp outputs to minimize the bus noise that transitions on the bus might cause. Furthermore, three-state buffer outputs deliver clean, non-reflected signal transmission and eliminate bus impedance discontinuities and wire-OR problems.

The 100990 is the faster of the two

## THE BATTLE OF THE BUSES

**T**here are over half-a-dozen standardized computer buses in the TTL world, including the popular VMEbus, Multibus, PC-AT, and NuBus. Coming on strong is the Micro Channel bus and perhaps in the next few years, Futurebus. Each of these buses, which has a predefined protocol as to how boards must communicate with each other and as part of the definition, includes a sink and source current limit for each line. With these basic definitions, custom but commodity chips can be developed to minimize the logic that's needed on a pc board to handle the bus-interface function.

Over a dozen companies have already developed circuits to simplify the bus logic for PC/AT's and compatibles, as well as add-in cards for the newer Micro Channel motherboards and add-in

cards. The chip sets often include specialized bus buffer and transceiver chips to replace many of the simple circuits, such as discrete latches and buffers. Approximately one year ago, Texas Instruments similarly developed a two-chip set to simplify the interface to NuBus systems in hopes of capturing a major share of the market for Apple Macintosh add-in cards.

There's considerable activity in support circuits for both Multibus and VMEbus systems—several VMEbus vendors have already developed a protocol chip that reduces a considerable chunk of the bus communication logic to one IC. Motorola has also developed chips to handle VMEbus interfaces. Similar activities have taken place in the Multibus world with Intel Corp., Santa Clara, Calif., and VLSI Technology Inc.,

San Jose, Calif., producing a protocol chip. In addition, Intel recently released a simplified bus communication chip to cut system cost.

Focusing on customizable bus interface circuits, PLX Technology Inc., Mountain View, Calif., developed flexible high-current output programmable logic circuits that can be configured to handle various bus requirements. The logic chips can handle 24 and 48 mA drive requirements, which covers a majority of bus drive applications. The company's latest release is a bus-master chip set for IBM's Micro Channel architecture. Housed in two 28-lead plastic leaded chip carriers, the MCA 3200 chip set connects directly to the bus, supplies all of the bus-master control signals, and performs local arbitration for 32-bit Micro Channel bus masters.



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MAP80-4000	80W/110W PK	5V @ 14A	12V @ 4A/7A PK	-12V @ 1A	-5V @ 1A
MAP80-4001		5V @ 14A	12V @ 1A	-12V @ 1A	24V @ 2A
MAP80-4002		5V @ 14A	12V @ 4A/7A PK	12V @ 1A	-12V @ 1A
MAP130-4000	130W/165W PK	5V @ 20A	12V @ 5A/8A PK	-12V @ 1A	-5V @ 1A
MAP130-4001		5V @ 20A	12V @ 1A	-12V @ 1A	24V @ 3.5A
MAP130-4002		5V @ 20A	12V @ 5A/8A PK	12V @ 1A	-12V @ 1A

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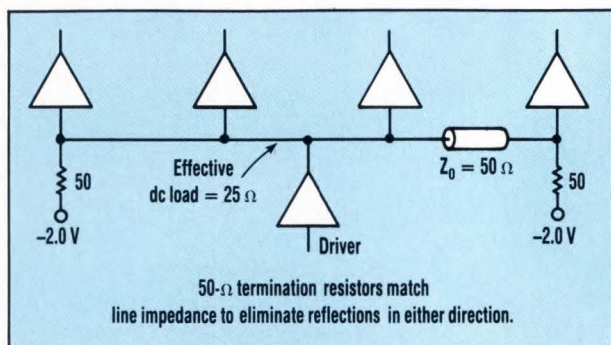
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# COVER: BUS INTERFACE CHIPS



**1. DOUBLY TERMINATED BUSES**, such as this one suggested by National Semiconductor, can eliminate signal reflections in both directions. However, the double termination reduces the dc impedance to just 25  $\Omega$  and requires that the ECL bus drivers handle up to 128 mA.

with a typical  $t_{PD}$  of 1.3 ns (2 ns worst case). It also has a complementary enable control function for systems in which the bus has two multiplexed sources of information, such as addresses and data. Contention is prevented by an enabling-scheme that gives priority to the A bus. The 100790 inserts 1.6 ns typical (2.2 ns worst case) and includes simple Output-Enable and Transmit/Receive inputs that let multiple chips be easily cascaded and controlled.

Tackling the wide unidirectional buses in ECL systems, a 9-bit-wide backplane driver, the F100126 from National Semiconductor, adds just 2.55 ns maximum to the signal flow. The chip contains nine independent, high-speed buffer gates with 50-k $\Omega$  pull-down resistors on the inputs. Also pushing interfaces to nine bits, Sony created a pair of translators: the CXB1125 and CXB1124. The CXB1125 offers an ECL-to-TTL interface and the CXB1124 does the TTL-to-ECL conversion. Worst-case  $t_{PD}$ s are 3.3 and 2 ns, respectively, while each chip consumes about 700 mW. Aimed at power-critical applications, National is developing a pair of low-power hex unidirectional translators—the F100324 and 325—which consume half the power of the older 100124 and 125, yet deliver similar propagation delays.

Both Motorola and Texas Instruments also offer unidirectional translators. There are two sets of three chips from Motorola—one set for 10K logic and the other for 100K

series ECL. The MC10H/100H601 are 9-bit TTL-to-ECL translators; the '602 is a latched version of the 601 and the '603 is a latched ECL-to-TTL 9-bit wide translator. TI's circuits include a pair of octal ECL-to-TTL chips, the SN10KHT5540 and 5541 (inverting and true outputs, respectively), which have  $t_{PD}$ s of about 4

ns. TTL-to-ECL versions of the chips with typical  $t_{PD}$ s of 1.6 ns are due soon.

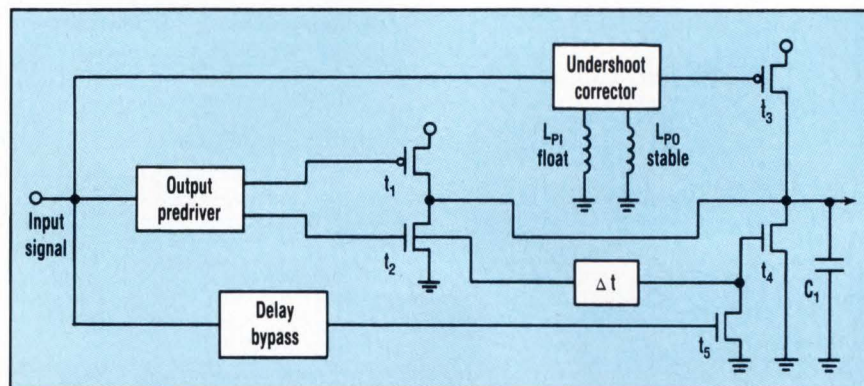
Translators are also available in hex or quad versions, depending on the price designers are willing to pay for board density. Signetics, for instance, has the 100984 quad, or the 100982 hex bidirectional transceivers. Both have latches on their outputs to better stabilize the signals and reduce skew. National's F100128, which is an octal circuit, cuts the board space even further. Signetics' circuits have a worst-case  $t_{PD}$  of 3.5 ns and 4 ns, respectively, for TTL-to-ECL and ECL-to-TTL conversions. National's circuit has  $t_{PD}$ s of 4.3 and 8 ns for exactly the same operations.

Some of the shortest propagation delays for 100K-family ECL systems are available in a pair of chips—a dif-

ferential line receiver and a buffer—developed by Sony: the CXB1103 and 1105, respectively. The quintuple receiver has a maximum  $t_{PD}$  of just 520 ps (low-to-high transition) and 540 ps (high-to-low transition), while the triple buffer adds just 840 or 800 ps of delay to a signal. Both are housed in 24-lead quad-sided packages to minimize propagation delays. Similar functions found in the F100114 and F100113 from National Semiconductor have  $t_{PD}$ s of 2.2 and 1.7 ns, respectively, for similarly packaged circuits. To get the higher speed, though, Sony's chips pay a power penalty: They consume about 800 mW vs. about 500 mW for National's chips.

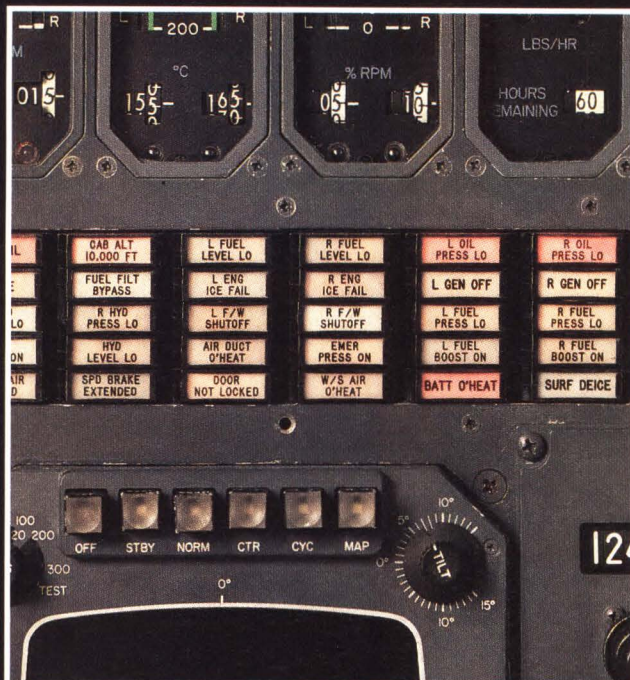
Requiring just one 5-V power supply, a series of translators recently released by Motorola—the MC10H351 and 352—convert TTL to ECL and CMOS to ECL, respectively. The circuits have typical  $t_{PD}$ s of just 1.3 ns. Also on the horizon are 9-bit-wide dual-supply ECL-to-TTL and TTL-to-ECL translators. Versions of the chips will be available with or without output latches.

With ECL signals running around on backplanes and system boards, one of the most critical problems is keeping signal skew under control. Even timing differences of 0.5 ns can be crucial for system timing. To tackle that problem, low-skew buffers and clock-distribution circuits were developed by Motorola, National, and others. The 100115 quad driver from National, for example, keeps



**2. TO MINIMIZE SWITCHING NOISE** and reduce ground bounce, designers at National Semiconductor included edge-control circuits to ensure the signal doesn't change too fast and an undershoot corrector to minimize the amount of undershoot the output generates.





Before



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# COVER: BUS INTERFACE CHIPS

signal skew to less than 75 ps, while the 100E111 from Motorola controls skew to less than a few hundred picoseconds between outputs.

## SIMILAR PROBLEMS

Basically, the same battle that rages in ECL is being waged in most TTL and CMOS systems with just two small differences: the level translation isn't needed, and a number of standardized buses for which chip makers can design economical chips that will specifically handle the interface functions, rather than just buffer the signal lines (see "The battle of the buses," p. 34).

When compatibility with standard TTL signals isn't necessary, there are alternatives to TTL or CMOS transceivers for faster systems. One solution, National's DS3890 octal

trapezoidal drivers, 3892 three-state receivers, 3893 single-ended transceiver, and 3898 repeaters offers an off-the-shelf chip set. Designed specifically for high-speed backplanes, such as Futurebus, the bipolar chips use a 1-V signal swing (centered around 1.5 V) to minimize power consumption. Alternatively, custom circuits can be developed around a proprietary signal definition.

The trapezoidal circuits also have low output capacitances (less than 5 pF) to minimize bus loading and include internal circuits to control the signal edge rise and fall times. Thus, rather than generate square logic signals, the chips generate precise trapezoidal waveforms with typical rise and fall times of 6 ns. Both the driver and repeater can drive an equivalent dc load of 18.5  $\Omega$ . The

trapezoidal receiver has a precise threshold that tracks the Bus Logic signal level to maximize noise immunity in both logic high and low states.

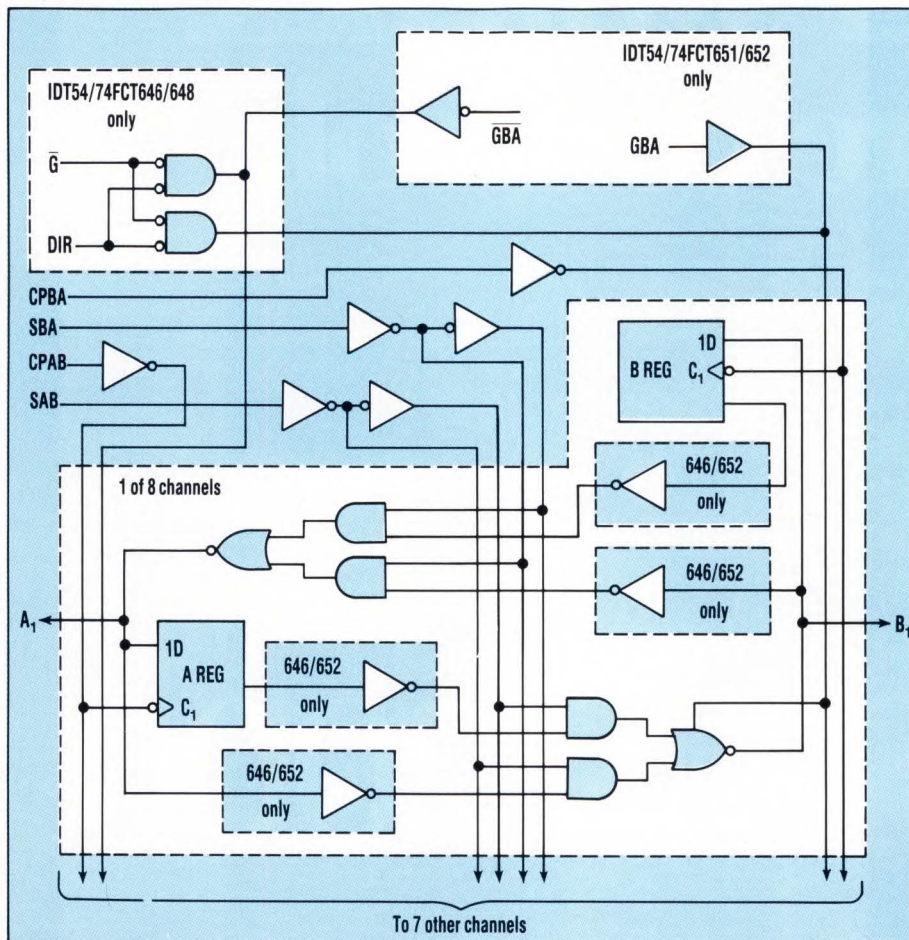
Switching noise and the coupling of that noise into adjacent signal lines are enemies to all digital-system designers. In high-speed TTL and CMOS systems, the problems are more apparent than with ECL systems because signal swings are much larger and the pc boards are rarely designed as controlled-impedance systems. As a result, such problems as ringing, ground bounce, and reflections, among others, are constant headaches designers have to deal with.

Several years ago, designers at Texas Instruments came up with one possible solution for the Fact logic family: an improved circuit pinout with center-pin power and ground connections rather than the conventional diagonal corner-pin power and ground layout. That approach, coupled with some edge-rate control, shows a marked reduction in generated noise.

But many designers and manufacturers were reluctant to adopt the new pinout—even though Signetics signed on early as an alternate source—because a larger package was required for each chip. With several more years of design experience under their belts, most logic manufacturers feel they can deliver circuits with similar reduced noise characteristics without requiring the revised pinout by doing a better job of controlling the signal edges.

One such attempt from National resulted in the release of the Fact Quiet series earlier this year. Proprietary graduated turn-on output circuits minimize the ground-bounce pulse while maintaining circuit performance (Fig. 2). On-chip undershoot correction circuits also eliminate the output signal's excursions below ground level. Additional design changes include a redesign of the chip to physically separate the output ground from the rest of the circuitry and a new leadframe to reduce common inductance and isolate circuit elements.

Consequently, National can guar-



**3. EXTRA CONTROL LOGIC** on this single bit of the 74FCT646 octal transceiver makes it possible for Integrated Device Technology to manage the signal flow of multiplexed transmissions. Data can be moved directly from the data bus or from the dual sets of internal D-type storage registers.



# COVER: BUS INTERFACE CHIPS

## BUS INTERFACE CIRCUIT PURVEYORS

<b>Advanced Micro Devices Inc.</b> Sunnyvale, Calif. (408) 732-2400 <b>CIRCLE 451</b>	<b>Integrated Device Technology Inc.</b> Santa Clara, Calif. (408) 727-6116 <b>CIRCLE 455</b>	<b>NEC Electronics Inc.</b> Mountain View, Calif. (415) 960-6000 <b>CIRCLE 459</b>	<b>Texas Instruments Inc.</b> Dallas, Texas (214) 868-7682 <b>CIRCLE 463</b>
<b>Fujitsu Microelectronics Inc.</b> San Jose, Calif. (408) 922-9000 <b>CIRCLE 452</b>	<b>Mosaic Semiconductor Inc.</b> San Diego, Calif. (619) 271-4565 <b>CIRCLE 456</b>	<b>Performance Semiconductor Corp.</b> Sunnyvale, Calif. (408) 734-8200 <b>CIRCLE 460</b>	<b>Toshiba America Inc.</b> Tustin, Calif. (714) 832-6300 <b>CIRCLE 464</b>
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<b>Harris Semiconductor Corp.</b> Melbourne, Fla. (305) 724-3800 <b>CIRCLE 454</b>	<b>National Semiconductor Corp.</b> Santa Clara, Calif. (408) 721-5000 <b>CIRCLE 458</b>	<b>Sony Corp.</b> Cypress, Calif. (714) 226-4195 <b>CIRCLE 462</b>	

Consider this a guide rather than a definitive list.

antee maximum levels of the critical noise specifications—ground-bounce voltage ( $V_{OLP}$ ) of 1.5 V, undershoot ( $V_{OLV}$ ) of -1.2 V, and minimum dynamic threshold of 2.2 V (high) and 0.8 V (low). In other CMOS families, undershoot values greater than -2 V were measured. These large values can cause incorrect operation of circuits tied into the same power bus. The result of those guaranteed limits is the first guaranteed noise margin for advanced CMOS logic circuits. Fact QS versions of the Fact family chips ensure a minimum of 400 mV of positive noise margin under input switching conditions. Initial circuits in the QS series include the 74ACTQ240, 244, 245, 374, and others. Approximately 30 octal bus interface circuits will be included in the QS family.

Circuits in the Fact family started to appear about 1984 or 1985. Since then, there have been many opportunities for enhancements thanks to improvements in CMOS technology and processing. Aside from achieving shorter  $t_{pDs}$ , the other major improvement is the more than doubling of the output current capability of the chips, from 24 mA to as much as 64 mA. As a result, the chips can directly replace the bipolar devices in the ALS, AS, and FAST families. National Semiconductor is currently working on a family of FCTA high-speed CMOS logic circuits with a high-current-handling capability.

The chips will have  $t_{pDs}$  in the 3-to-5-ns range—about 30% faster than the standard FCT family devices.

The basic "AC" TTL-compatible logic has thus spawned many offshoots—some TTL compatible and some intended for CMOS-only systems. Common to all of these offshoots are the bus interface functions that originated in the bipolar families. These functions tend to always be used in systems (the buffers, latches or registers, and transceivers) in varying configurations and bit widths.

## OPEN WIDE

The most popular bus interface circuits come in octal versions, which in a 20-pin package pack eight bus lines (eight inputs and eight outputs) plus two control signals, as well as the power and ground lines. For systems requiring parity, Advanced Micro Devices pioneered wider bipolar chips, such as 9-bit-wide versions in 22-pin packages and 10-bit versions in 24-pin packages (the Am29800 series). It has since implemented many of the same functions in its 29C800 family, which can handle loads of up to 48 mA. Aside from the simple functions, AMD has the 29C833, 853, and 855, which are bus transceivers with on-chip parity generation and checking circuits.

Pushing densities still higher, Texas Instruments released preliminary details on a 16-bit bus transceiver,

the 74AC16245. The first of the company's Widebus family, the circuit is basically the equivalent of two 74AC245s in one 48-lead very-small-outline 300-mil package with 25-mil center-to-center lead spacing. The chip, created in a 1- $\mu$ m CMOS process, achieves typical  $t_{pDs}$  of less than 5 ns and employs multiple power and ground pins to minimize switching noise. Divided into two identical halves, each with its own direction and enable control lines, the chip can be used in split-bus applications or it can isolate buses by disabling the outputs.

In addition to specifying the circuit to operate from a standard 5-V supply, TI and other companies characterized their chips to operate at 3.3 V. At the lower supply voltage level, TI's circuits slow down by about 2 ns, increasing the typical  $t_{pDs}$  to just less than 7 ns.

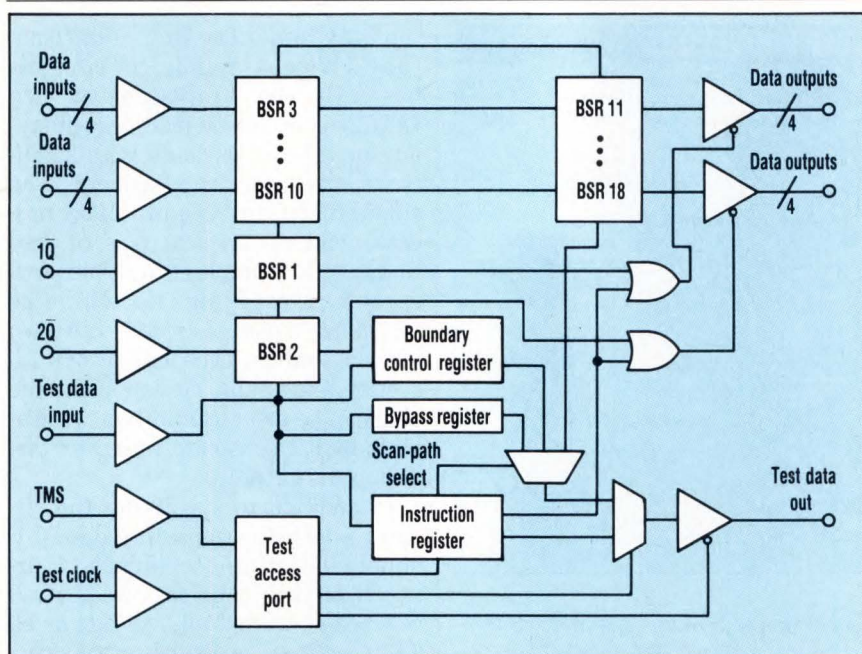
Claiming some of the shortest  $t_{pDs}$  for CMOS bus logic running at 3.3 V, the PCT33 series from Performance Semiconductor achieves a 3-ns  $t_{pD}$  for their equivalent to the 74FCTA244 octal buffer, 3.3 ns for the 245 octal transceiver, 3.7 ns for the 373 octal D-latch, and 4.2 ns for the 374 octal D flip-flop. The company's 5-V family, the PCTA series, has  $t_{pDs}$  of 4.2, 4.6, 5.3, and 6.5 ns, respectively, for the same functions. Falling right between those specifications, a family of chips from Integrated Device Technology (IDT) produces 4.1, 3.7, 4.2, and 5.2 ns  $t_{pDs}$  for the same functions.

Typical of IDT's family is the 74FCT646, an octal bus transceiver with three-state D-type flip-flops and control circuits (Fig. 3). The extra control logic manages the multiplexed transmission of data directly from the data bus or from the internal storage registers. The circuit comes in a T version that's speed compatible with FAST TTL, the AT versions that are 30% faster than FAST, and the CT series, which is 40% faster than FAST.

Several proprietary circuits are now in design at IDT. Due out in early 1990 is a clock distribution chip, the 49FCT805/806 (true/inverting outputs). Delivering up to 10 clock



# COVER: BUS INTERFACE CHIPS



**4. ON-CHIP BOUNDARY-SCAN** test circuits embedded by Texas Instruments in its 74BCT8xxx series make it possible for system designers to run tests on the chips through a four-line test port that can be cascaded with ports on other chips to make entire systems testable.

outputs with minimal skew, the circuit will use its CMOS roots to supply rail-to-rail signal swings.

Also being developed at IDT is a family of biCMOS bus-interface chips, the FBT series, which boost the output-current sinking level up to 64 mA for commercial devices and up to 48 mA for the military versions. The FBT series will initially focus on memory and line-driver circuits and include on-chip series termination resistors to minimize ground bounce. Circuit performance will be at least 25% faster than devices in IDT's FCTA series, which have delays of about 4.8, 4.6, 5.2, and 6.5 ns for the four aforementioned circuit types.

BiCMOS interface circuits are also in development at Signetics, but the company won't release performance details until the first half of next year. A surprise entry in the biCMOS interface circuit area is Harris Semiconductor, which just released a series of 13 74FCT compatible parts that have current drive of 48 or 64 mA per output, depending on the device type. Typical  $t_{PDs}$  are between 3 and 4 ns for the octal chips. Included in the initial offering are D-type latches, octal transceivers, and D-

type flip-flops. Another 10 chips are slated for release in the first quarter of next year. Ground-bounce for the Harris FCT chips is limited to a peak value of 1.2 V—even lower than the National Quiet series. Quiescent power consumption of the Harris chips will be about 200 times lower than FAST circuits, while operating currents are about one-fifteenth that of FAST (switching at 5 MHz).

Working jointly, Motorola and Toshiba are offering a family of chips that have 50- $\mu$ A standby current levels. But the circuits can't handle quite as much on their outputs as the IDT chips—they can only sink up to 48 mA per output. Propagation delays are also a little longer, running close to 6 ns for the MC74BC244 and 8.5 ns for the equivalents to the 373 and 374.

Though they don't have  $t_{PDs}$  as fast as the other chips, a family of octal devices developed by TI pack boundary-scan logic on the chip as well as the traditional octal buffer, transceiver, and latch or flip-flop. The SN74BCT8244, 8245, 8373, and 8374 include the company's Scope boundary-scan test capability that conforms to the JTAG scan-access

testability standard (Fig. 4). Four additional pins are required for the scan signals, which make it possible for the chip to run through some thorough testing of the I/O lines. When the chip is in its normal mode, the test circuits can either be activated to take snapshot samples of the data appearing on the circuit pins or to perform a self-test on the boundary-scan register.

Also breaking into biCMOS logic, Mosaic Semiconductor plans to use commercially available chips and put them in vertical-in-line through-hole packages that it developed for housing memory chips. The ceramic vertical "DIPs" meet military specifications and have two rows of pins on 100-mil centers between pins and between rows. By positioning the packages vertically rather than horizontally, packing density on the boards for the interface logic improved more than 50%, even over surface-mounted packages.

Pure bipolar TTL circuits aren't totally overwhelmed because many applications exist in which the low power of CMOS isn't a requirement and thus the premium price for CMOS needn't be paid. FAST logic circuits are available from nearly every bipolar logic supplier. And for bus interface circuits, the name of the game is integration. One direction is, of course, to put more buffers or latches on a chip. The other is to put more logic on the chip so that some of the system functions are absorbed into the interface circuit. This direction was taken with the 74F899 from National Semiconductor, a 9-bit latched transceiver that includes parity generation and checking logic on the chip. By including the circuitry on the chip, logic delays going from chip to chip were eliminated and the 74F899 can perform the parity generation and checking operation in 36 ns maximum—about half the time of a system built from lower-integration FAST chips. □

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### FACT QS 74ACTQ244 Specifications

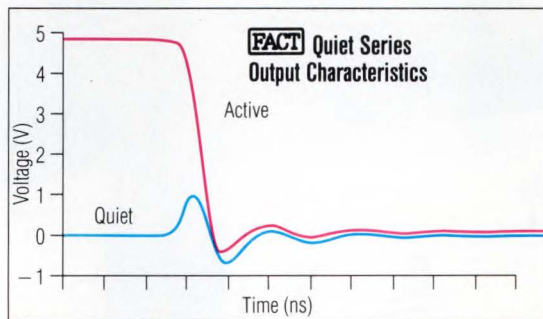
	Typical	Max
$V_{OLP}$	1.0V	1.5V
$V_{OLV}$	-0.5V	-1.2V
$V_{IH0}^*$	1.8V	2.2V
$V_{ILD}^*$	1.4V	0.8V
Tskew	0.5ns	1.0ns
ESD	6,000V	4,000V min
Latchup	1.0A	300mA

\* $V_{IH0}$ —Dynamic Input threshold high.

\* $V_{ILD}$ —Dynamic Input threshold low.

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### FACT QS vs. THE COMPETITION [Typical (+25°C, 5.0V)]

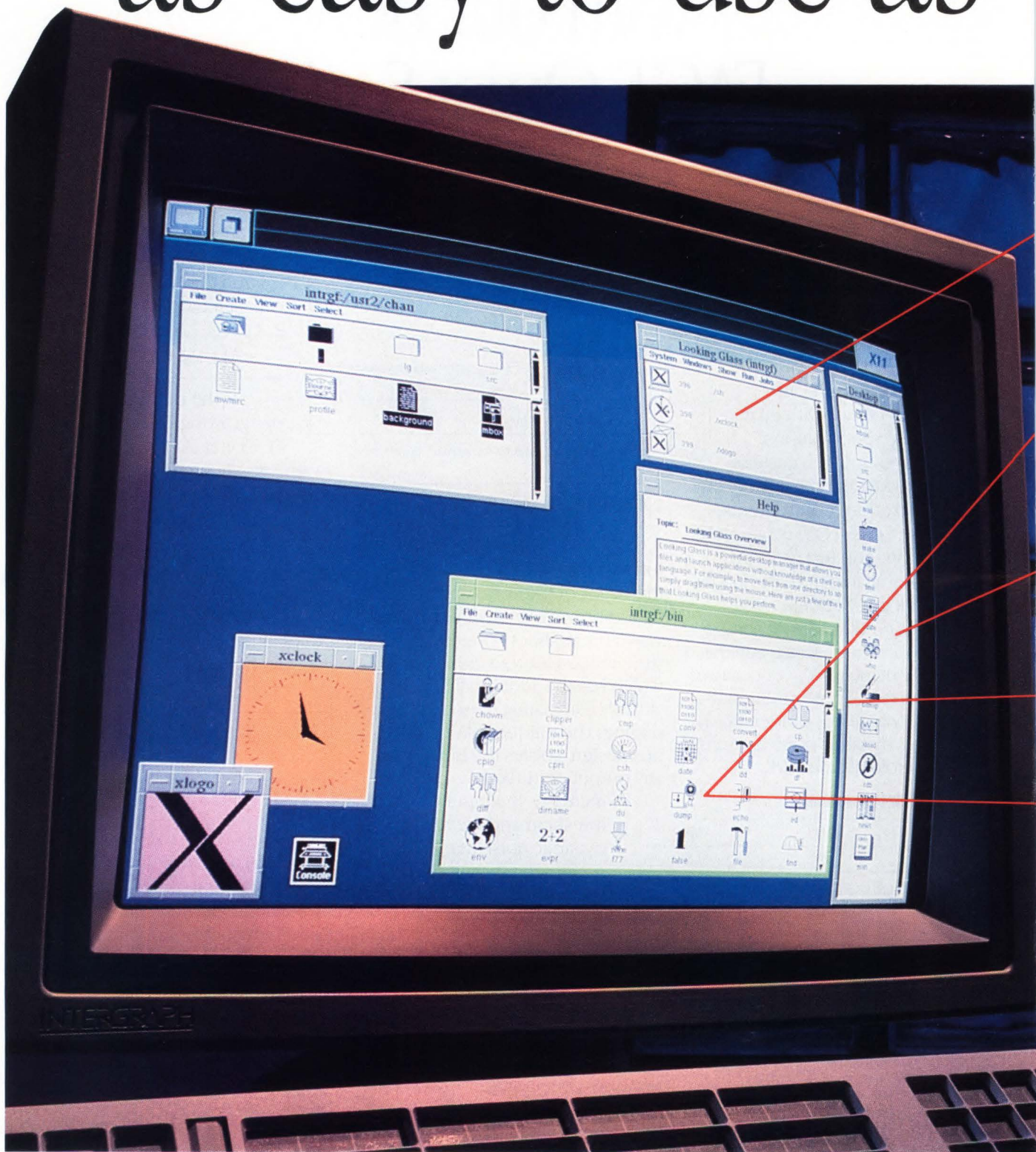
Parameter	1. National's FACT QS	2. Competitor A Center Pin ACL	3. Competitor B FCTA
$V_{OLP}$	1.0V	1.4V	3.0V
$V_{OLV}$	-0.5V	-1.5V	-1.6V
$V_{IH0}$	1.8V	2.3V	2.4V
$V_{ILD}$	1.4V	0.6V	0.4V

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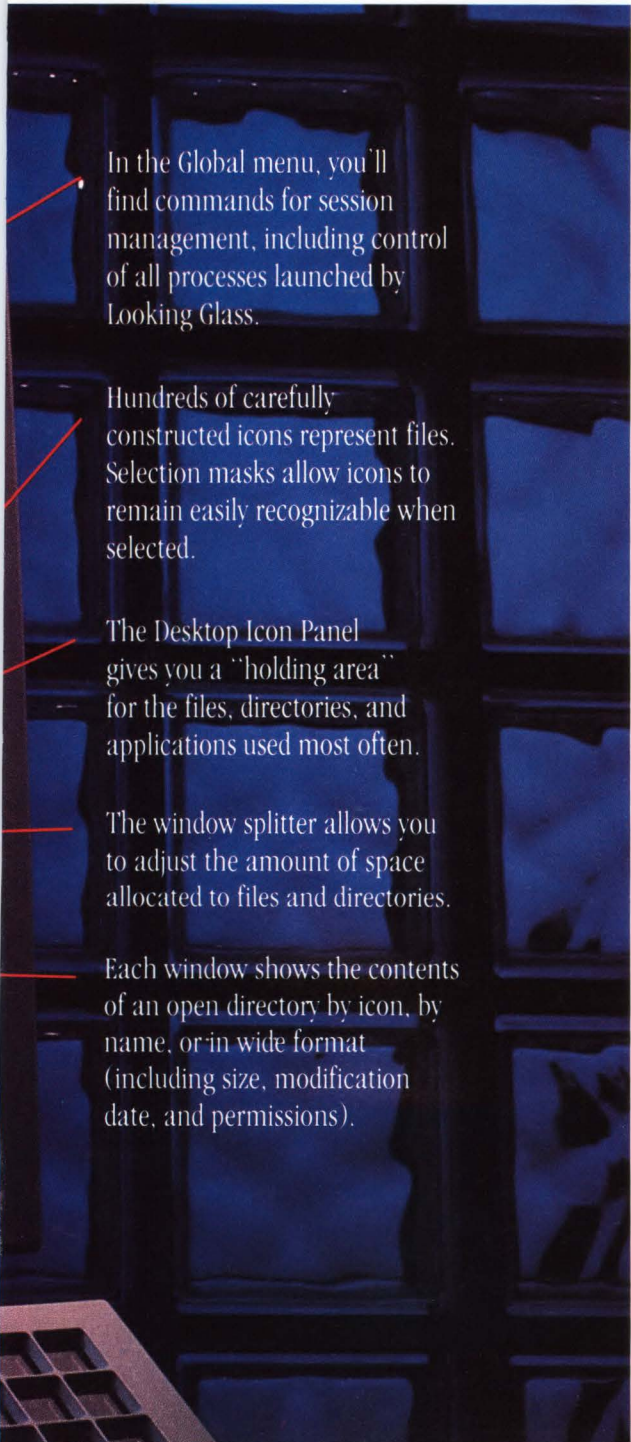


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AS THE NEED FOR  
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GROWS, FDDI STANDS  
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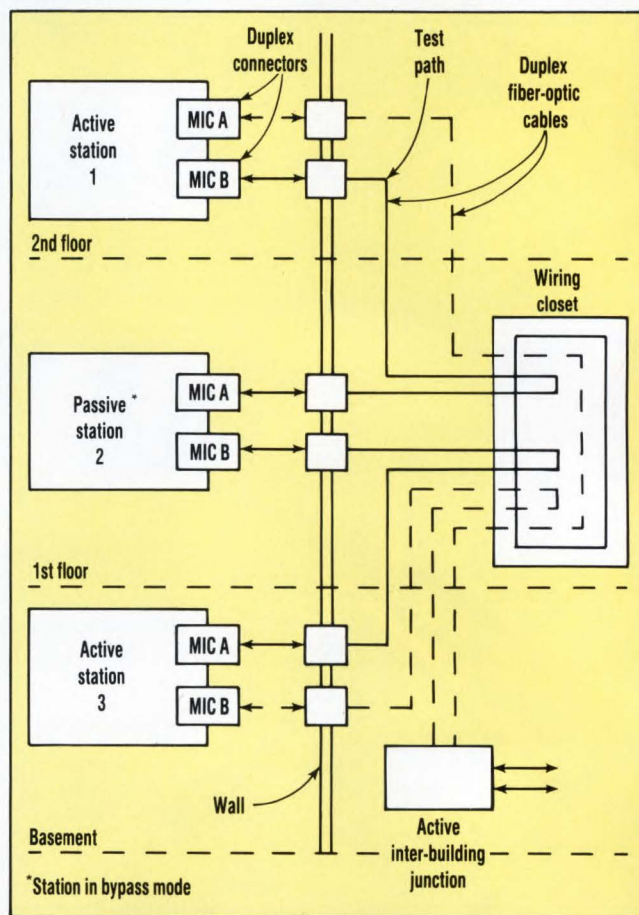
KAREN PARKER and STEVE KAUFMAN

National Semiconductor, 2900 Semiconductor Dr.,  
P.O. Box 58090, Santa Clara, CA 95052-8090;  
(408) 721-5000.

**T**he need for higher data-transfer rates in local-area networks is outstripping the capabilities of Ethernet, the leading local network in business office and data communications applications. Faster, more powerful computer workstations are forcing system designers to devise faster data highways to carry information between networked machines. The 10-Mbit/s data rate possible on Ethernet, the first of the IEEE-802-standard networks developed in the 1970s, won't be sufficient in the 1990s.

Fiber-optic technology, which can transfer data much faster than copper-cable networks, will complement Ethernet. A fiber-optic local-network standard nearing approval is the fiber distributed data interface (FDDI). Not only does an FDDI network transfer data faster than any other network, it's also more reliable because it incorporates error-handling utilities.

As defined by the American National Standards Institute's X3T9.5 system I/O interface committee, FDDI is a 100-Mbit/s fiber-optic local network using a dual counter-rotating ring architecture and a token-passing access method. In a ring configuration, two or more nodes connected by a physical medium (cable) pass infor-



**1. THE FIBER DISTRIBUTED data interface physical medium-dependent layer defines the optical cable, connectors, and transceivers needed by a network.**



## DESIGN APPLICATIONS

# FIBER-OPTIC LANs

mation sequentially. Each node examines or copies and repeats the information to the next node, with the information finally returning to the originator.

A counter-rotating ring offers better reliability and performance than conventional bus, star, or ring architectures because it continues to operate even if a link or station fails. Unlike Ethernet, FDDI can support hundreds of nodes (stations) and can operate over distances greater than 10 km.

FDDI conforms to the open-systems interconnection (OSI) model of the International Standards Organization. This well-known layered model of computer interconnection levels makes it possible to develop standards independently for each level. Moreover, designers can integrate the unique technology of fiber optics with the IEEE-802 Ethernet standards so FDDI can serve as a high-speed backbone to Ethernet.

Layer 1 (the physical layer) of the OSI model defines the mechanical and electrical aspects of activating, maintaining, and deactivating the physical connections needed to transfer information between network data links. This layer includes wire and cable systems and other mechanical and electrical components that connect devices or stations. Common examples of the physical layer include some of the best known standards in data communications: RS-232C, RS-422, RS-449, and others.

Typically, Layer 1 consists of two parts: the physical medium-dependent (PMD) layer and the physical layer, or PHY. The PMD layer defines the special optical hardware that links stations on the network. Included are media interface connectors (MICs), optical transmitters and receivers, and the fiber-cable plant, which contains all of the connection hardware and facilities between stations (Fig. 1). The PHY layer includes the encoding and decoding mechanisms that move data around the network.

FDDI's 100-Mbit/s data rate (125-Mbaud transmission rate) is based on using a 1300-nm wavelength and

an light-emitting diode (LED) light source. The data-rate and distance capabilities of a 1300-nm LED are well suited to ANSI X3T9.5 fiber-optic local-network specifications. For example, at 1300 nm, the attenuation between stations that are 2 km apart permits the use of an LED instead of a higher-power laser diode.

Moreover, LEDs work with low-cost fiber components, such as 62.5-micron core diameter, 125-micron cladding diameter multimode fiber cable, which will be commonly used for FDDI. Single-mode fibers cost more than multimode fibers and are designed for optimum propagation at 1310 and/or 1550 nm—wavelengths that require the use of an expensive laser diode.

The PMD specification also defines the optical cable's aperture and maximum attenuation. The numerical aperture (0.275) is necessary for specifying connectors, while the attenuation determines the maximum distance between stations. The maximum attenuation is 11 dB and includes the attenuation of the cable, connectors, and optical bypass switch(s). The cable can have a maximum attenuation of 2.5 dB/km, for a total of 5 dB. The cable splice adds another 5 dB of attenuation, giving a total of 10 dB over the 2-km distance. The attenuation specification of 11 dB is related to the optical transmission and reception characteristics of FDDI.

ANSI X3T9.5 requires the optical power output of the transmitter device to be between -20 and -14 dBm. Pulse characteristics of the output waveform include a duty-cycle distortion of less than 1 ns and rise and

fall times of less than 3.5 ns.

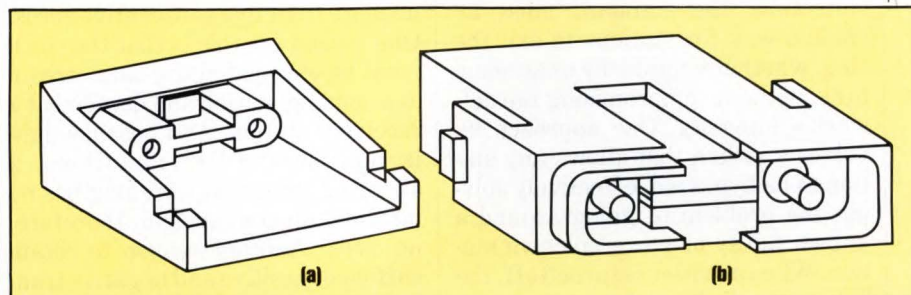
Every optical transmitter on a FDDI local network transmits to a receiver or an optical-to-electrical transducer device. The minimum input sensitivity for a receiver per the specification is -31 dBm. As a result, a transmitted signal at the minimum power output of -20 dBm can be attenuated 11 dB by the optical cable and the resulting -31-dBm signal can still be detected by the receiver. Rise- and fall-time specifications for the receiver input are 5 ns maximum.

The fiber-optic receiver, which amplifies and converts the analog transducer signal into ECL levels, is the most critical component of the PMD. It contains a PIN diode, a high-gain preamplifier, and a decision circuit, all of which are very noise sensitive. And noise is a big problem at the very low signal levels in the receiver.

At this early stage of FDDI's development, the receiver preamp, called a transimpedance amplifier, is difficult to design properly. One alternative for fiber-optic receiver manufacturers is to integrate all of the receiver functions in a monolithic circuit. This requires a high-performance bipolar process that can isolate noise within individual elements on the chip and still offer the needed input-level sensitivity.

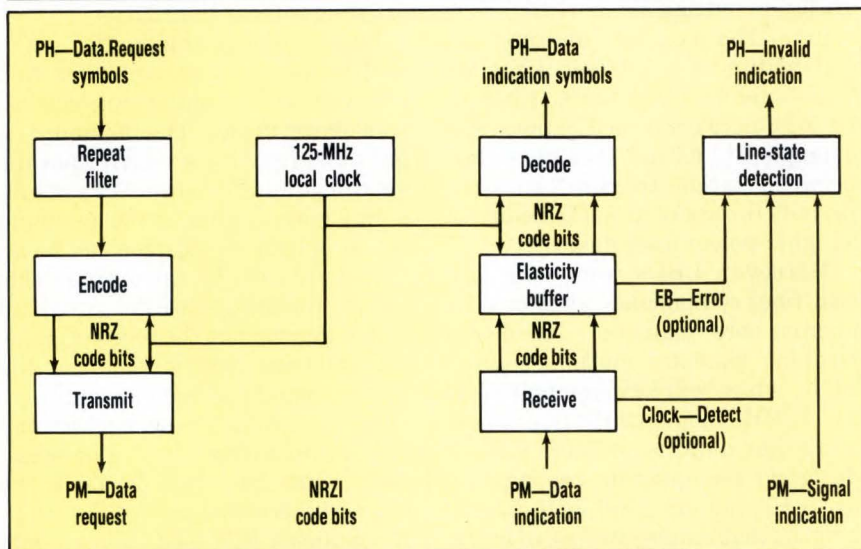
Other chip makers implement the receiver as a hybrid circuit, but this scheme doesn't minimize noise, which is vital for meeting the PMD performance specifications. Moreover, a hybrid won't create the most compact package, which is crucial to reducing the receiver's cost and the board area it occupies.

Every station in a FDDI local net-



**2. THE FDDI SPECIFICATION** defines the media interface connector receptacle with a keying scheme that prevents station miswiring (a). Although the plug portion isn't described, its form is determined mostly by the need to mate with the receptacle (b).





**3. THE ENCODING AND DECODING TECHNIQUES** used to transmit data over the network are defined by the FDDI physical layer.

work needs a MIC to connect the fiber-optic transceiver to the cable plant. The MIC's primary function is to mechanically align the optical transmission fiber to a similar fiber or to an optical port on a component, such as a receiver, transmitter, or bypass switch.

Although the PMD defines only the receptacle portion of the connector, specifications for the plug portion are defined implicitly because the two parts must mate (*Fig. 2*). The MIC's dimensions—1.290-in. wide by 1.569-in. long by 0.367-in. high—were chosen to facilitate mounting on a printed-circuit board, but bulkhead mounting is also possible. Height is the most critical dimension, because the connector must fit on a pc board connected in the standard bus configuration.

Because FDDI employs a ring architecture, the standard must include a way for stations to exit the ring, whether voluntarily or accidentally, without compromising the network's integrity. One approach involves a switch that allows any station to be bypassed, effectively solving the problem of going around a known faulty or powered-down station. When a station is turned off, the bypass switch reroutes the data through an internal relay. Because it's directly in the network's signal path, the switch's key parameters

are response time, attenuation, and reliability.

Another way to maintain integrity is to use a concentrator, a device that's connected to the ring as a node. The concentrator links stations outside the ring to the ring, giving the configuration the appearance of a star arrangement. Any station can be switched out of the ring without disturbing any other station's connectivity. In general, a concentrator is more reliable than a bypass switch.

The ANSI specification for the FDDI's PHY layer includes definitions for data encoding and decoding, control and data symbols, filtering, buffering, and other functions (*Fig. 3*).

To encode data on the media, the standard specifies a 4B/5B code, which ensures that a data stream has no more than five consecutive zeros. One reason for this is that the clock must be encoded in the data stream at a sending station and decoded at a receiving station. And because data is represented by transitions, a string of zeros that's too long has no information content and, therefore, no clock. Another reason to retain sufficient positive and negative transitions in a data stream is to maintain the network's dc balance, the lack of which affects a network's bit-error rate (BER).

The 4B/5B technique is also more efficient than the commonly used Manchester data-encoding scheme, which needs more signal bandwidth to convey the same amount of information across a network. For example, a Manchester scheme needs 200 Mbits/s to send the same amount of information as 4B/5B encoding does at a 125-Mbit/s bandwidth. Consequently, FDDI local networks can use less expensive transceiver devices.

FDDI's 4B/5B encoding is based on a non-return-to-zero-inverted (NRZI) technique. Actually, the encoder's output is NRZ data that's translated into an NRZI format. The translation creates the number of transitions needed for the 4B/5B coding. For example, five consecutive logic 1 bits would be sent out in NRZ code for an Idle signal. But because the NRZI format inverts the output level whenever it encounters a logic 1, the resulting NRZI pulse train includes sufficient transitions (*Fig. 4*).

Information in a FDDI ring is transmitted as frames and tokens. A frame contains data and a token signifies the right to transmit information. Within each frame and token are fields composed of symbols. On the media, the FDDI information is arranged in code groups, with each group representing a symbol.

There are essentially two kinds of symbols: control and data. Control symbols permit operation between the PHY and the layer above it. Layer 2, called the data-link layer in OSI terminology, is divided into two parts: the media access control (MAC) and the logical link control (LCC). The transmitter in the PHY accepts symbols from the MAC, encodes them into 5-bit groups, and transmits the serial data over the media. Control symbols interpreted in the PHY and MAC are delimiters: Quiet, Idle, and Halt line-state control symbols, J and K start delimiters; the T end delimiter; and the Set and Reset symbols used for status indicators in the trailer of the frame.

In addition to control symbols, FDDI receivers use violation indicators to recognize bit patterns con-



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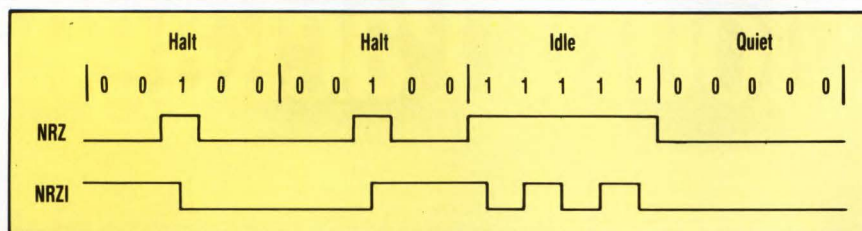


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## DESIGN APPLICATIONS

# FIBER-OPTIC LANs



**4. ALTHOUGH THE ENCODER'S OUTPUT** is non-return-to-zero data, the information is translated into a non-return-to-zero-inverted format to increase the number of transitions.

taining bad data. If a station receives violation indicators, it corrects the errors rather than propagate them along the network. The receive station does this automatically using hardware techniques, which include a repeat filter in the PHY layer.

The filter inserts idle symbols into a data stream until the erroneous bit patterns disappear and proper data is sent. Because every station performs repeat filtering, very few errors exit on the network and down-

time caused by errors is low.

Another piece of error-correcting hardware in each station is an elasticity buffer, which compensates for clock frequency variations between neighboring stations. The buffer effectively resynchronizes data frames as it receives them by either adding or subtracting a byte of data at an appropriate time. By doing so, it increases or decreases the length of the preamble that precedes each frame, keeping the data length con-

stant. If the data frames aren't re-synchronized, some bits would be lost or gained as a frame is repeated around the ring. □

*Karen Parker, FDDI program manager at National Semiconductor and member of the ANSI X3T9.5 committee, received her BS in physics from the University of Massachusetts and has studied computer architecture at Stanford University and the University of Massachusetts.*

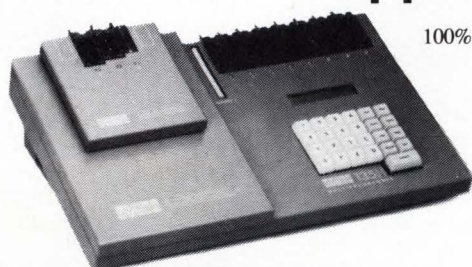
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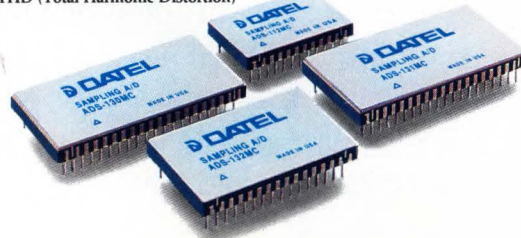
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# BE CAREFUL WHEN WRITING SCSI-2 WIDE BUS SOFTWARE

WHILE THE PROPOSED SCSI-2 WIDE BUS HAS ADVANTAGES, IT ALSO CHALLENGES SOFTWARE DESIGNERS.

The proposed SCSI-2 ANSI standard adds numerous features to the original SCSI specification. Among the more useful is a wider data bus called Wide Bus, which transfers 8-, 16-, or 32-bit data to and from SCSI peripherals. The advantages of the Wide Bus come with some problems, though, including accounting for the skew between the two cables used for data byte transfers, proper ordering of bytes in the buffer containing sector data, proper negotiation for bus width, determining when a transfer is complete, and handling parity. Designers must solve these problems in the algorithms that manage Wide Bus data transfers at the controller level.

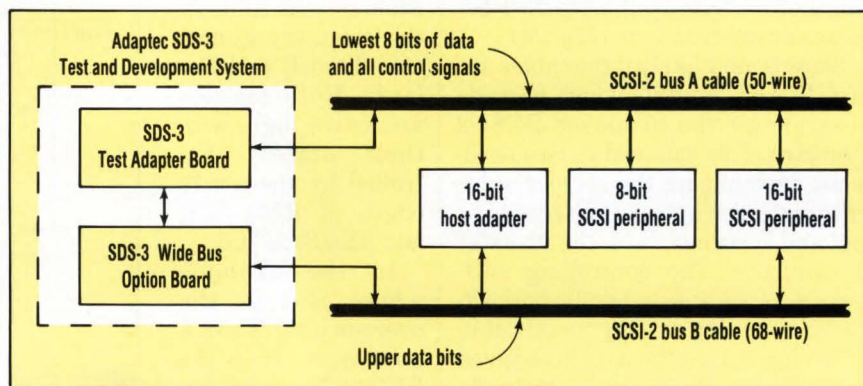
The proposed SCSI-2 Wide Bus consists of two cables (Fig. 1). Many of the software requirements of SCSI derive from the fact that data transfers on the cables need not be synchronized, creating a possible skew between them. The A cable is identical to SCSI-1's single cable, so SCSI-1 and -2 equipment can coexist in a system. The A cable's 50 lines carry a 9-bit data bus (8 data bits and

1 parity bit), nine control signals, a resistor-terminator power line, and ground lines.

Two of the nine control signals are handshake lines: Request (REQ) and Acknowledge (ACK). A target asserts REQ when it's ready to receive or transmit one data byte; an initiator asserts ACK to indicate that a 1-byte data transfer is complete. Note that the target always controls the data transfer process. It starts a transfer by asserting REQ and awaits an ACK from the initiator prior to commencing another single-byte transaction.

Containing 68 pins, the B cable carries 24 data and 3 parity lines, REQB and ACKB control signals, its own resistor-terminator power signals, and ground lines. The data lines are organized as three sets of 8, each with its own parity bit. Separate REQB and ACKB handshake lines are defined because the B cable's length may be different than the A cable. With a set of handshake lines on each cable, the skew between handshake signals and data lines on any one cable is minimized. This is necessary if SCSI-1 and -2 equipment are going to coexist.

In a SCSI-2 system, each target/



**1. THE PROPOSED SCSI-2 wide bus standard uses two cables: an A cable that carries the first 8 bits of data, and a B cable that can carry 24 bits for a total bus width of 32 bits.**

GEORGE HAHN

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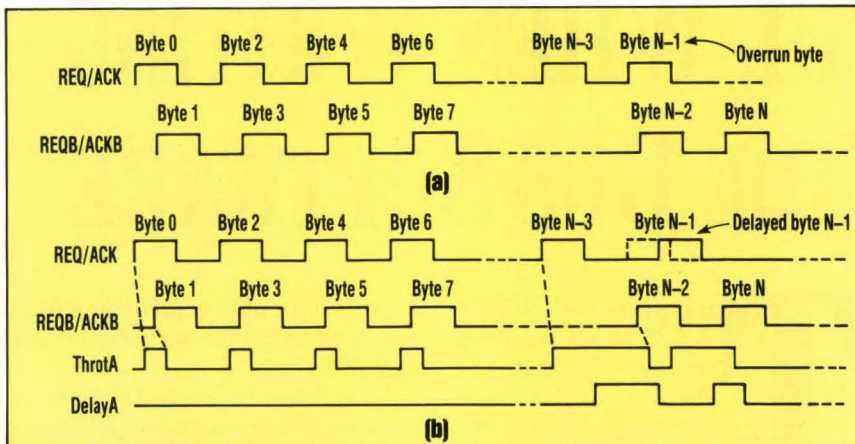
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# DESIGN APPLICATIONS

## SCSI-2 SOFTWARE



**2. BECAUSE SCSI-2's CABLES** need not be synchronized, data on one cable may lead or lag data transmitted on the other cable, a condition known as skew (a). Using a throttling technique ensures that the data bytes will be received in the proper order (b).

initiator pair must negotiate for the width of the data bus. The negotiation process that chooses a particular data bus width is a factor software designers must consider.

Only the A cable is used for an 8-bit bus width. For a 16-bit bus width, even bytes (0, 2, 4, etc.) move on the A cable as odd bytes (1, 3, 5, etc.) pass along the B cable. For 32-bit data, bytes 0, 4, and so on are transferred on the A cable, while bytes 1, 2, 3, 5, 6, 7, and so on are sent on the B cable. Because the B cable contains 24 data and 3 parity signal lines, 2- or 3-byte transfers are made on this cable in one transaction (one REQ/ACK and one ACKB).

Because the two cables need not be synchronized, data bytes transferred on one cable may lead or lag those moving on the other cable—a condition known as skew. For instance, if byte N-1 begins transferring before byte N-2, byte N-1 becomes an overrun byte (Fig. 2a).

Skew is very likely if the cables are of different lengths, which is made possible by the proposed SCSI-2 standard. This can lead to two problems: determining the correct order of transferred bytes at the receiving end and knowing when the transfer is complete. The controlling software must be able to handle both situations, making debugging difficult.

To ensure that the data is received in the proper order, the control software can prevent skew by appropriately controlling the REQ/REQB

(target) or ACK/ACKB (initiator) handshake signals. This process is called throttling. Alternatively, the software can manage the problem by skew counting, which is to maintain a running tally of the skew. Throttling, which facilitates debugging, is an important feature of test equipment. The technique can also be designed into the hardware and firmware for a controller or other SCSI device, but the reduced data throughput caused by throttling is generally unacceptable.

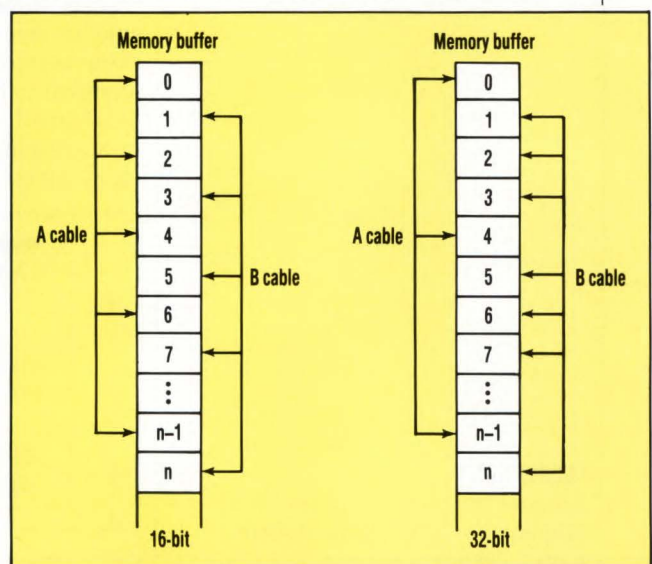
Throttling requires specialized hardware that keeps track of which cable transferred the last data byte (ELECTRONIC DESIGN, Sept. 14, p. 73). The hardware generates ThrotA and DelayA signals if cable A leads cable B by more than one data byte. If cable B leads cable A, the circuitry generates ThrotB and DelayB. Both signals are active high, with their states controlled by the active edges of REQ/ACK and REQ/ACKB.

In the example where N-1 is the overrun byte, ThrotA goes high when the REQ/ACK signal associated with byte N-3 goes high (Fig. 2b).

DelayA goes high when REQ/ACK goes high again. DelayA gates the REQ/ACK signal onto the SCSI bus, preventing REQ or ACK from going active until the next active edge of REQ/ACKB. This next active edge of REQ/ACKB causes ThrotA to go low, forcing DelayA low.

By preventing the occurrence of either REQ or ACK, the throttling circuitry prevents the occurrence of the other. Consequently, the handshaking used in both the target and initiator roles enables designers to throttle a data transfer by suppressing one of the two handshaking signals—the other end of the link suppresses the other signal. Thus, throttling synchronizes the two cables.

If the need for maximum performance eliminates throttling as an alternative, the control software must track the number of bytes transferred on each cable, as well as each byte's arrival time. The system can then derive the skew count from this information, which is the difference between the number of transfers made on the A cable (one REQ/ACK sequence per transfer) and the number made on the B cable (one REQ/ACKB sequence per transfer). As a measure of the amount by which one cable leads or lags the other, skew count can help in the proper ordering of transferred bytes and in determin-



**3. FOR 16- AND 32-BIT WIDE BUSES,** the location in which data bytes are stored in the buffer depends on which cable carried the data and how wide the bus is.



ing when a transfer is complete.

The skew count, however, isn't necessarily the same as the number of bytes sent on the A cable, less the number sent on the B cable. For a 32-bit bus, each REQ/ACK sequence accompanies a 1-byte transfer, while every REQ/ACKB sequence is associated with a 3-byte transfer. This discussion considers the case of a 16-bit Wide Bus, in which the number of bytes sent on the A cable less the number sent on the B cable is identical to the skew count.

To improve performance, SCSI systems often buffer data bytes at the receiving end of the SCSI cable. For reads, buffering typically takes place at the host end of the cable; for writes, it's generally at the drive end. The algorithm that controls the byte order must also account for buffering.

For an 8-bit bus, all of the bytes come from the A cable and are stored in the order received. For 16- and 32-bit busses, the offset at which incoming bytes are stored from the beginning of the buffer depends on the cable from which a byte came and the width of the SCSI data bus (Fig. 3). Thus, the algorithm must consider each byte's source as well as the relative skew of the cables.

A Warnier-Orr diagram highlights the prominent features of an example algorithm (Fig. 4). This is for an asynchronous 16-bit bus, whereby even bytes are transferred on the A cable and odd bytes are transferred on the B cable.

In the diagram's upper left corner is the index, or the offset within the buffer at which the next byte from each cable will be stored. The A index is initialized to zero, and the B index to 1. At the center of the leftmost brace is a loop that constantly checks for Command Complete (a second algorithm determines command completion). The loop executes as many times as necessary, therefore the C in the parentheses is a variable.

Within the command completion loop are two "if" statements: Byte Available from A and Byte Available from B. Based on conditions specified at the bottom of the diagram, the "if" statements look for REQ assert-

ed and REQB asserted, respectively. The statements are loops that execute 0 or 1 time, depending on the condition specified.

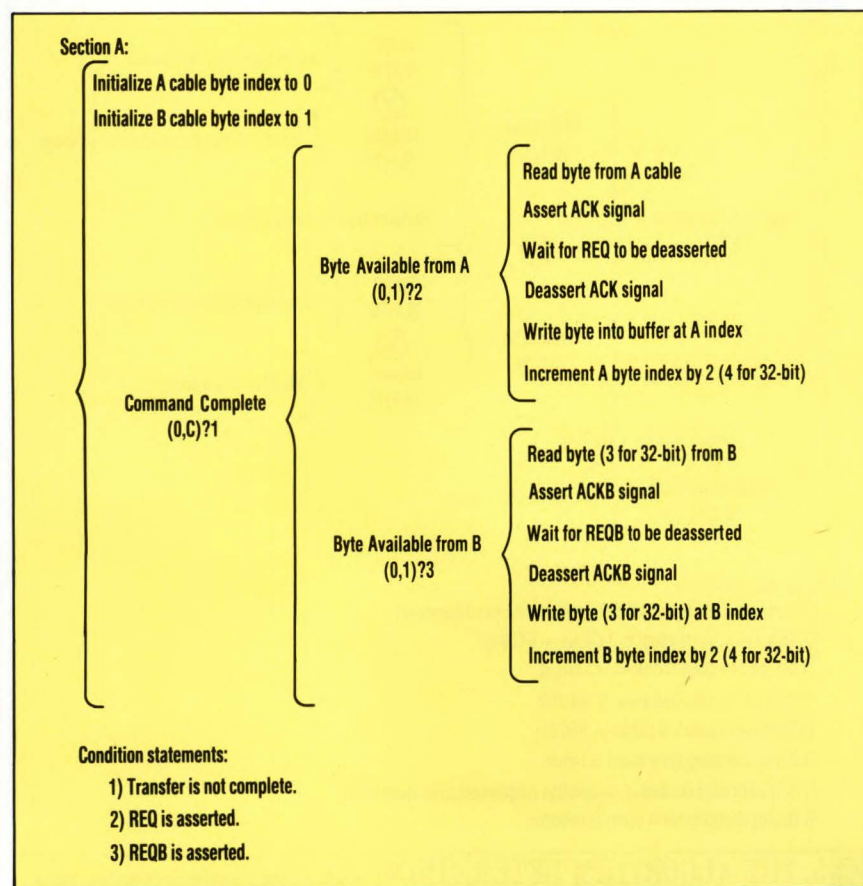
When the condition in one of the "if" statements is satisfied, the algorithm executes a series of tasks, which are in the rightmost brace of the Warnier-Orr diagram. These tasks involve the following: reading the incoming byte, performing the REQ/ACK handshake protocol, writing the byte to the buffer at the appropriate index, and incrementing the index value.

The algorithm loops continuously through the tests for Command Complete, Byte Available from A, and Byte Available from B, in that order, until the condition for Command Complete is met. Thus, if Byte Available from A is true, the algorithm executes the statements associated with this "if" statement, then goes to Byte Available from B. A true result there causes the execu-

tion of the corresponding statements and then an evaluation of Command Complete.

This sample algorithm is for an initiator. For instance, the algorithm could be used when a host is placing bytes received from a disk controller or other SCSI target device into a buffer. The algorithm for a target is similar: REQ/REQB and ACK/ACKB are transposed and the Command Complete loop is replaced by one that determines if all of the bytes were transferred.

The next problem is how to determine when a data transfer is complete. One obvious value to check is skew count. Because it's the difference between the number of transfers made on the A cable and those on the B cable, the skew count will be zero when a transfer is complete. It may also be zero, however, when a transfer is partially complete, as when an equal number of transfers have occurred on both cables. This



**4. A TYPICAL BUFFER PLACEMENT ALGORITHM** includes condition statements to determine when REQ or REQB is asserted.



may happen repeatedly if a transfer proceeds in lock step. Thus, a skew count of zero is a necessary but insufficient condition for checking command completion.

Another measure of a completed SCSI transfer is the Command Complete message that's sent from the target to the initiator. Consider that the least significant byte of all messages is always transferred on the A cable. In the case of a Command Complete message, which has a value of zero, there are no further message bytes. In messages that do have additional bytes, the first byte must be nonzero.

The SCSI specification prohibits the sending of a Command Complete message until all bytes are sent on both cables. This restriction prevents the Command Complete message on the A cable from leading the last data bytes moving across the B cable. If the two cables are of vastly

different lengths, however, the circuitry at the receiving end might accept the Command Complete message before processing the last data bytes transferred on the B cable.

Thus, the algorithm that determines when a data transfer is done must contain two conditions:

1. A Command Complete message must be received on the A cable, indicating that all of the bytes were transferred on this cable.
2. The skew count must be zero, indicating that all of the bytes were transferred on the B cable.

In the Warnier-Orr diagram of a general algorithm for assessing whether command execution is finished, the leftmost brace contains the Command Complete message (Fig. 5). For an initiator, the message is received; for a target, the message is sent. After the Command Complete message is received, the algorithm checks for a zero skew count.

If both conditions are met, a test for status phase is made.

If the skew count isn't zero after a Command Complete message is received or sent, an error condition must be flagged. In the case of a target, this takes the form of a Check Condition Status statement; for an initiator, it emerges as an Initiator-Detected Error Message.

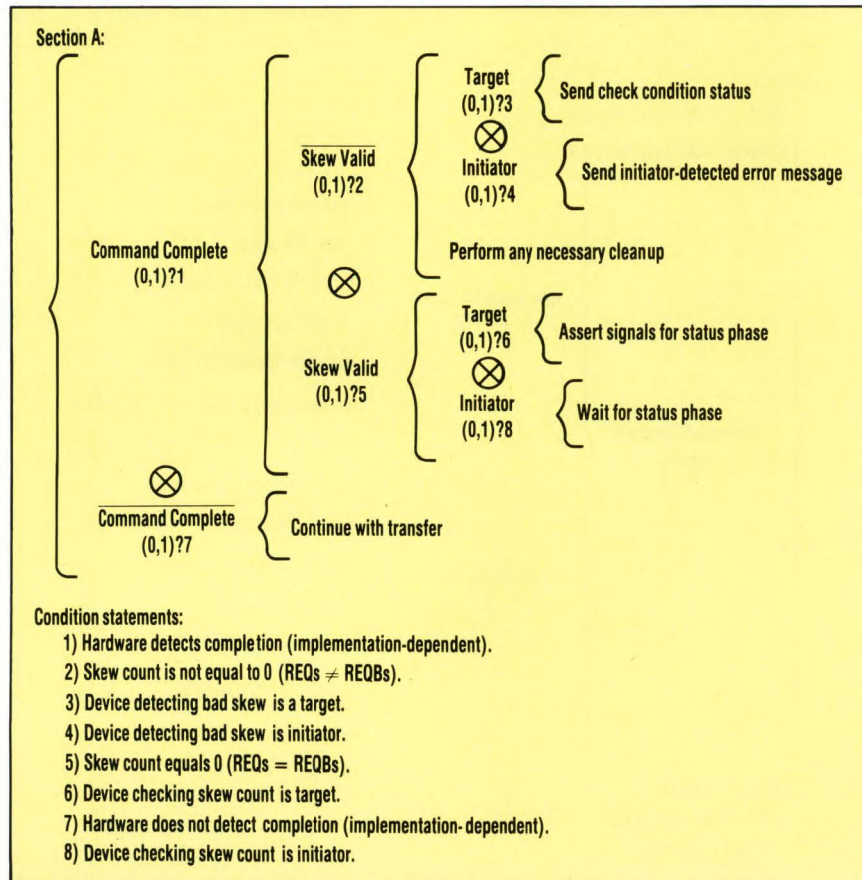
Another piece of software that's peculiar to the SCSI-2 Wide Bus is the negotiation sequence. Each target/initiator pair must negotiate the width of the data bus they will use for their transactions prior to their first data transfer. In the absence of this negotiation, an 8-bit width is used. This default feature allows the simultaneous use of devices with different bus widths.

The negotiation is simple: The initiator requests a width using a Message Out sequence, and the target responds with a Message In sequence specifying that width or a smaller one. There isn't any further negotiation.

An example of such a negotiation is a state log display generated by the Adaptec SDS-3 SCSI test and development system (Fig. 6). The first Message Out byte (C0) is an Identify message sent from the initiator to the target. This is signalled by the highest order bit, bit 7, which is set to a one. Also, bit 6 of this message byte specifies whether the initiator has granted the target the right to disconnect. In this example, the bit is a 1, indicating that the target may disconnect. This byte also contains bits that make it possible to select either a specific logical unit number or a target routine number. The proposed SCSI-2 standard gives further details.

The next Message Out byte (01) indicates the beginning of a message containing more than one byte. Afterwards comes a 02 Message Out byte, which specifies that two more message bytes will follow. The first of these, a 03, tells the target that this is a Wide Bus negotiation sequence. The second, a 02, requests a bus width of 32 bits.

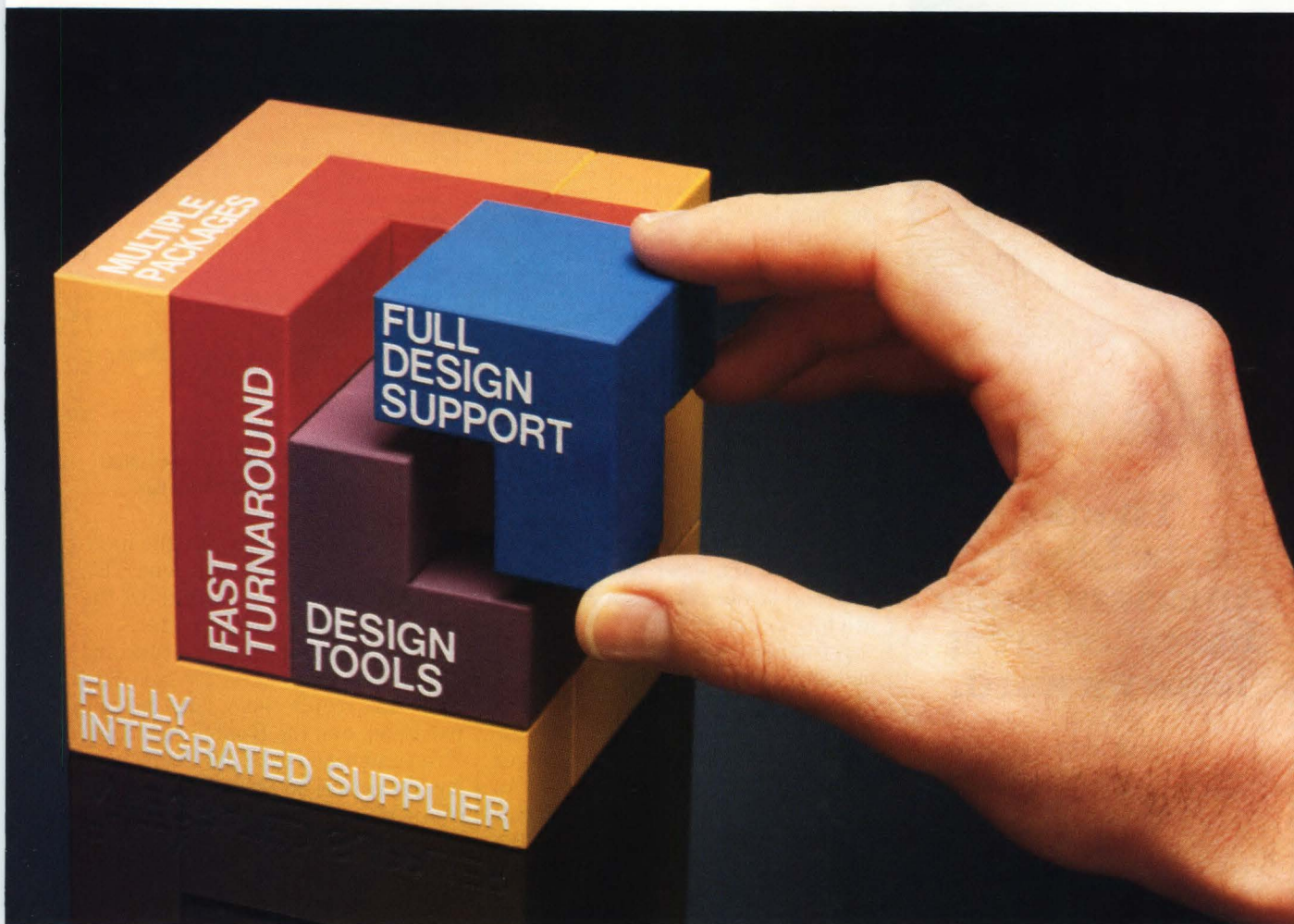
The next four Message In bytes in the state log are the target's re-



**5. THE ALGORITHM DETERMINING** when a data transfer is complete must ensure that a Command Complete message was received on the A cable and that the skew count is zero.



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## DESIGN APPLICATIONS SCSI-2 SOFTWARE

sponse. The first byte, a 01, specifies that more Message In bytes will follow. The second, a 02, reports the number of Message In bytes that will be sent. Next comes a 03, which tells the initiator that this is a Wide Bus negotiation sequence. The last Message In byte, a 01, is the target's reply.

The message specifies a width of 16 bits, which is less than the requested width of 32 bits. Because the smaller of the two widths is used, this negotiation sequence will result in a bus width of 16 bits.

A further consideration is the data padding that may be needed by a SCSI-2 Wide Bus. The SCSI standard states that the number of bytes in every data transfer must be an integer multiple of the bus width in bytes. As a result, a 16-bit bus must transmit an even number of bytes, and the bytes transferred by a 32-bit bus must be a multiple of four. If the data doesn't meet this restriction, the transmitter must pad the data.

To ensure data integrity when pad bytes are needed, the transmitter must also send an Ignore Wide Residue message. This message specifies the number of undefined pad bytes included in the final bus transaction (the last set of REQ/ACK and REQ/ACKB handshakes).

In the example code, the Command Out message with an op code of 03 is a Request Sense command that results in the transfer of 19 hex (25 decimal) bytes from the target to the initiator. The next line specifies that number: Data In 19H bytes (Fig. 6, again). Because 25 bytes are transferred on a 16-bit bus, the transaction would consist of 12, 2-byte transfers plus one 1-byte transfer. Consequently, a pad byte is needed to make the transaction 26 bytes.

Immediately below the line specifying the number of bytes transferred are two Message In bytes. The first byte, a 24, tells the initiator that it must ignore a wide residue.

### STATE LOG BUFFER DISPLAY

00020.30760	Bus Free Detected		046
00045.88097	Arbitration as 07	45.88108	045
00045.88122	Selection ids = (1001 0000b)	45.88143	044
00045.88243	Message out C0		043
00045.88254	Message out 01		042
00045.88265	Message out 02		041
00045.88271	Message out 03		040
00045.88276	Message out 02		03F
00045.88332	Message out 01		03E
00045.88366	Message out 02		03D
00045.88380	Message out 03		03C
00045.88400	Message out 01		03B
00045.88501	Command out 03 00 00 00 19 00	45.88534	03A
00045.89881	Data in 19H byte (s)		039
00045.89914	Message in 24		038
00045.89950	Message in 01		037

### 6. THIS STATE LOG DISPLAY shows a typical bus-width negotiation sequence for a SCSI-2 Wide Bus.

The second, a 01, indicates the number of bytes to be ignored—one. This corresponds to bits 8 through 15, the second byte of the last transfer.

The proposed SCSI-2 standard also defines a parity bit for each data byte. As a result, the A cable has one parity bit, and the B cable has three. Even undefined bytes have valid parity. Therefore, in the above example of a wide residue, the pad byte sent from the target to the initiator has valid parity to ensure that all bytes transferred have valid parity.

Handling of parity errors is implementation-dependent. Retries up to a specified number is one type of handling method. If this doesn't produce a successful transfer, an error message is supplied from one level of software to another. The result may be a display message flagging the parity error. The error may also be written to an error log file. □

*George Hahn, software engineer with Adaptec's Development Systems Operation, holds a BSAE from Rensselaer Polytechnic Institute, Troy, N.Y., and an MSME from the University of California at Berkeley.*

*Mark S. Gordon, founder and president of Digital Finesse, designed ICs at Zilog and helped found Verticom Inc.*

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# SIMPLIFY HIGH-RESOLUTION MONITOR DESIGN

**D**esigning the video circuitry for a high-resolution CRT monitor is more complicated than it first appears to be. The amplifier must have the ability to drive the cathode of the monitor's CRT with a video signal whose peak-to-peak amplitude is 40 V, and whose bandwidth is on the order of 100 MHz.

The circuitry should include a section for restoring the signal's dc component, and it should have provision for adjusting the picture's brightness and contrast.

In the case of color displays, the amplifier needs to handle the (usually) mismatched guns in a typical CRT. It must also compensate for the different efficiencies of the red, green, and blue phosphors.

Meeting these requirements is far from trivial, but it's much easier than it used to be, thanks to a pair of video ICs, which include most of the circuitry needed between the monitor input connection and the CRT cathode. By encompassing most of the circuitry in IC form, the LM1201 monolithic preamplifier and the LH2422 hybrid power amplifier deliver such benefits as compact design, reduced cost, improved reliability, and superior high-frequency performance.

The LM1201 preamp accepts a 1-V<sub>pk-pk</sub> video signal as its input. Along with amplification, it allows brightness and contrast control, and black-level clamping for dc restoration. The LM1201 sports a rise time of 2.5 ns at 4-V<sub>pk-pk</sub> output, which translates to an effective bandwidth of over 140 MHz (*Table 1*).

The LH2422 is a simple four-transistor hybrid integrated circuit that can directly drive a CRT cathode with 40 V<sub>pk-pk</sub> (*Table 2*). Although, by itself, the LH2422 is a transimpedance (current-to-voltage) amplifier, it can be easily converted into an ordinary voltage amplifier by adding a gain-setting resistor (*see "Inside the LH2422," p. 66*).

Building a high-resolution monitor with the LM1201 and LH2422 combination is a fairly straightforward job, despite the high bandwidth requirements of such a display. To review, a monitor with a resolution of 1024 by 1024 pixels and a refresh rate of 60 Hz requires that over a million pixels be energized 60 times/s. This allows for less than 16 ns per pixel. With retrace time and other overhead, a more realistic figure is 12 ns. Typically, a third of that figure is allowed for each

**ZAHID RAHIM**

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## DESIGN APPLICATIONS

# DESIGNING VIDEO AMPLIFIERS

of the transition (rise and fall) times, which means that the rise time should not exceed 4 ns at the cathode of the CRT monitor. This corresponds to an effective overall system bandwidth of approximately 100 MHz.

A complete system that can meet that requirement can be built with the LM1201, LH2422, and a few additional components (Fig. 1). Note that the circuitry doesn't provide for retrace blanking because that function is more conveniently performed at the control grid than at the cathode.

In the system, the video signal is ac coupled to the input of the LM1201 through a 10- $\mu$ F electrolytic blocking capacitor. If the capacitor's lead inductance turns out to be high enough to affect the system's high-

frequency performance, the problem can be alleviated by soldering a small high-frequency capacitor across  $C_1$ . On the inboard side of  $C_1$ , the purely ac video signal, is made to ride on a very stable 2.6-V bias source, supplied by the LM1201's internal reference.

## BOOSTING GAIN

Amplifiers  $A_1$  and  $A_2$  supply a gain of 8.  $A_2$ 's gain is externally controllable by varying the drive resistor  $R_{20}$ . To increase the gain,  $R_{20}$  may be reduced or even short-circuited. Alternatively, a 0.01- $\mu$ F capacitor may be placed across  $R_{20}$  to boost the high-frequency gain, if that's what is required.

The LM1201 provides contrast control through potentiometer  $R_{18}$ .

The voltage tapped off  $R_{18}$  allows voltage-controlled attenuation of amplifier  $A_2$ 's signal. With 12 V at the contrast control pin (pin 4), the output signal level is at its maximum (0-dB attenuation). Reducing the potential at pin 4 attenuates the output signal. The LM1201 offers a nearly linear 30-dB attenuation range.

Brightness is controlled by varying the potential at the brightness control pin (pin 9) using potentiometer  $R_{19}$ . The brightness control varies the dc offset of the output signal.

## INTERFACING THE CIRCUITS

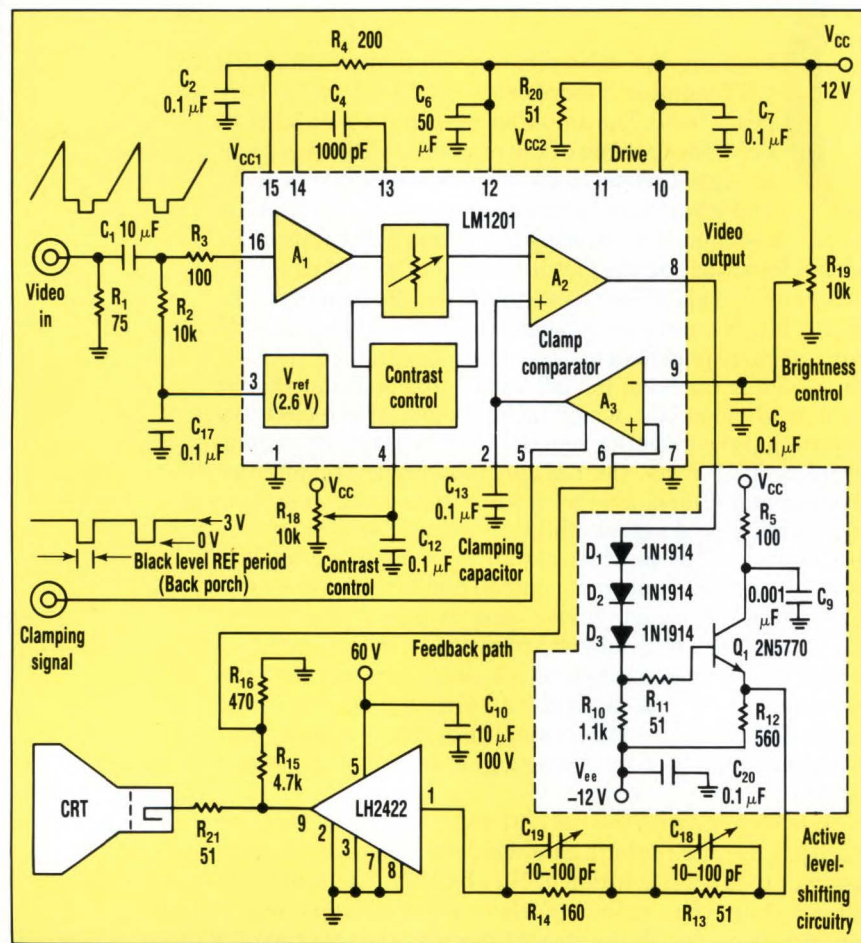
For proper operation, the LH2422 requires that its input signal be referred to 1.5 V dc. The LM1201's quiescent output voltage, however, is much higher than that. Consequently, the two ICs must be coupled by a high-speed level-shifting stage.

For maximum design flexibility, and to keep the design of the LH2422 power output amplifier simple, that level-shifting circuitry is implemented by external components. Consider two ways to configure that stage: a high-performance approach and a simpler one.

The high-performance active-level shifter comprises diodes  $D_1$ ,  $D_2$ ,  $D_3$ , high-speed buffer transistor  $Q_1$ , and negative supply  $V_{EE}$  (Fig. 1, again). The circuit feeds the input of the LH2422 through gain-setting resistors  $R_{13}$  and  $R_{14}$ . The values shown yield an ac gain of -14 (see "Inside the LH2422," eq. 2).

Capacitors  $C_{18}$  and  $C_{19}$  are peaking capacitors that allow the LH2422's pulse response to be optimized by trading off transition time and overshoot. Increasing  $C_{19}$  will decrease the transition times but increase the overshoot, which increases the circuit's settling time. It should generally be adjusted so that the overshoot doesn't exceed 5%. Placing a small resistor (between 10 and 30  $\Omega$ ) in series with  $C_{19}$  will reduce the settling time, but it does so at the expense of increased rise and fall times.

Capacitor  $C_{18}$  allows for fine-tuning of the pulse response after it has been roughly determined by  $C_{19}$  and the series resistor, if any. Once val-



**1. ALL OF THE CIRCUITRY** needed for a high-resolution monochrome CRT monitor is contained in just two ICs and a handful of other components. In this circuit, black-level clamping is done by the feedback loop, which consists of  $A_2$ , the active level-shifting circuitry, the LH2422, and  $A_3$ . This CRT video amplifier has a rise time of 3.4 ns, and a bandwidth in excess of 100 MHz.



# DESIGN APPLICATIONS

## DESIGNING VIDEO AMPLIFIERS

**TABLE 1:  
KEY SPECIFICATIONS  
OF THE LM1201**

Typical specifications at $V_{CC} = 12V$ , $T_A = 25^\circ C$	
Parameter	Specification
Maximum gain	8 V/V
Attenuation range	0 to 45 dB
Distortion at $V_{out} = 1 V_{pp}$	0.3%
Rise time at $V_{out} = 4 V_{pp}$	2.5 ns
Effective B.W. (f-3dB) at $V_{out} = 4 V_{pp}$	140 MHz

ues of the two variable capacitors are experimentally determined, they can be replaced by fixed capacitors for actual production.

Depending on the length of the wire connecting the CRT video amplifier's output to the CRT's cathode, its inductance may interact with the cathode capacitance to form an LC tank circuit. That tank circuit may introduce excessive overshoot and ringing at its resonant frequency. To eliminate that problem, a damping resistor ( $R_{21}$ ) is included in the circuit (Fig. 1, again).  $R_{21}$  must not be made too large or the time constant it sets up in combination with the CRT's cathode capacitance may adversely affect the signal's rise and fall times. A value of 50 to 100  $\Omega$  works well for most applications.

In addition to reducing ringing, the damping resistor also protects the CRT video amplifier against damage caused by arcing within the CRT. During arc-over, the damping resistor effectively limits the arc-over current.

### THE BLACK LEVEL

The LM1201 uses an externally gated clamp comparator ( $A_3$ ) to accomplish black-level clamping for dc restoration of the video signal. A clamping signal applied through pin 5 enables  $A_3$  during the back porch portion (black-level reference period) of the composite video signal. When enabled,  $A_3$  becomes the key element in a feedback loop that compares the dc feedback taken from the LH2422's output with the voltage set by the brightness control potentiometer. Depending on the LH2422's output, the clamping capacitor,  $C_{13}$ ,

is either charged or discharged until the feedback loop is stabilized. This action clamps the video signal to the black-level reference voltage set by the brightness control potentiometer.

During the video portion of the signal,  $A_3$  is disabled and  $C_{13}$  holds the black-level reference voltage until it is refreshed by the next video signal. Because the video signals corresponding with each line of the raster are clamped at a fixed reference potential, the dc component of each line is restored.

The dynamic black-level clamping not only boosts the monitor's power supply rejection ratio (PSRR), but it also keeps its black-level drift very low. That drift stays low because the black level of each video signal is brought back to the correct reference potential during the signal's back-porch interval.

### MEASURED PERFORMANCE

For the complete high-performance circuit, rise and fall times of under 3.4 ns were measured at the cathode. With a corresponding bandwidth of over 100 MHz, the circuit is well suited for 1024-by-1024 display resolution monitors.

Not every design requires the absolute maximum performance that the LM1201 and LH2422 can deliver. For situations in which a bandwidth of about 80 MHz will suffice, the simplified circuit may be preferred to that of the high-performance circuit (Fig. 2). The main difference between the two circuits is that the simpler one eliminates the active level

shift stage and the need for a negative supply,  $V_{EE}$  (Fig. 1, again).

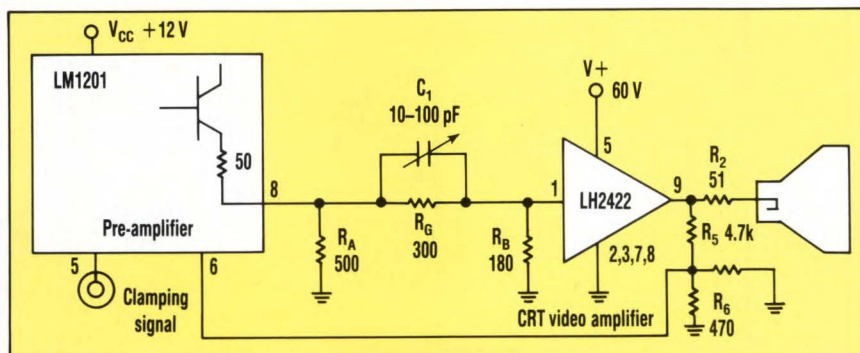
Instead, it uses pull-down resistor  $R_A$  to bias the emitter follower output of the LM1201. With  $R_G = 300 \Omega$ , the LH2422 is configured for an ac gain of -10. In the absence of  $R_B$ , the high-quiescent output voltage of the LM1201 would cause the LH2422's output to be in negative saturation. Resistor  $R_B$  counteracts this effect by pulling the LH2422's input low, which causes the amplifier's output to go high. The value of  $R_B$  depends on the value chosen for  $R_G$ . If  $R_G = 300 \Omega$ , a value of 180  $\Omega$  for  $R_B$  is optimum. If a different value of  $R_G$  is chosen (to change the gain of the LH2422), then the value of  $R_B$  will need to be modified as well.

The required value of  $R_B$  is determined by measuring the dc level of LM1201's output and using that value in equation 3 (see "Inside the LH2422"). Alternatively,  $R_B$  can be determined experimentally by using a potentiometer and adjusting it until the correct output offset is obtained. If that is done, it's important for the designer to make sure that the chosen resistor values are such as to draw less than 20 mA from the LM1201's output.

The simplified circuit was built and tested. Its rise and fall times came in at under 4.2 ns, which corresponds to an effective bandwidth of over 80 MHz.

### STEPPING UP TO COLOR

With the basics of building high-resolution monochrome monitors in place, moving up to the design of col-



**2. GREAT SIMPLIFICATION RESULTS** when the active level shifter in figure 1 is replaced by an RC interface network. The downside is a change in bandwidth from 100 MHz down to 80 MHz.



## DESIGN APPLICATIONS

# DESIGNING VIDEO AMPLIFIERS

or systems isn't too big a step. What's needed is an LM1201-LH2422 pair for each video channel. The circuitry for the green channel with lines ending in arrows indicates connections to corresponding points in the circuitry for the red (R) and blue

(B) channels (*Fig. 3*).

Note that the LM1201's contrast control pin (pin 4) is connected to the corresponding pins of the red and blue channels so potentiometer  $R_{13}$  can control the contrast for all three guns. Similarly, common brightness

control for all three guns is achieved by connecting the brightness control pins (pin 9) of all three channels together.

Because the light emitting efficiencies of the red, blue, and green phosphors are different, the guns

## INSIDE THE LH2422

**T**he LH2422 is a wide bandwidth, high-voltage amplifier that uses only four transistors (*see the figure, part a*). Key to the device's performance are its transistors' specifications: breakdown voltages of 70 V to 80 V and an  $f_T$  near 1 GHz. The LH2422 is constructed using hybrid technology.

The amplifier is essentially a transimpedance (current-to-voltage) amplifier with a 3-k $\Omega$  internal feedback resistor ( $R_F$ ). Resistors  $R_1$ ,  $R_2$ , and  $R_3$  set up a supply-dependent bias current, which produces a supply-dependent bias voltage at the base of  $Q_1$ . A simple model of the circuit can help in analyzing the circuit's operation (*see the figure, part b*).

Because the amplifier operates from one power supply, the output needs to be biased at half the supply voltage ( $V_+/2$ ) so that symmetrical output swing can be achieved. This is accomplished by the supply-dependent bias voltage  $V_B$  and the resistor  $R_B$  (con-

nected between the amplifier's inverting input and ground). With no external input signal, the amplifier's quiescent dc output is:

$$V_{out}(dc) = (1 + R_F/R_B)V_B \quad (\text{eq. 1})$$

with a 60-V power supply, the amplifier's input bias voltage is specified at 1.55 V. Thus, at  $V_+ = 60$  V and  $R_B = 165 \Omega$  nominal, the amplifier's output is biased at 30 V. Note that any current injected at the inverting input flows entirely through the feedback resistor because the current through  $R_B$  remains unchanged due to the voltage  $V_B$  impressed across it. In the transimpedance mode of operation,  $\pm 6.67$  mA at the inverting input causes the amplifier's output to swing  $\pm 20$  V from its quiescent output dc voltage.

Voltage-to-voltage gain can easily be accomplished by inserting a gain-setting resistor  $R_G$  in series with the input signal and the amplifier's inverting input (*see the figure, part b, again*).

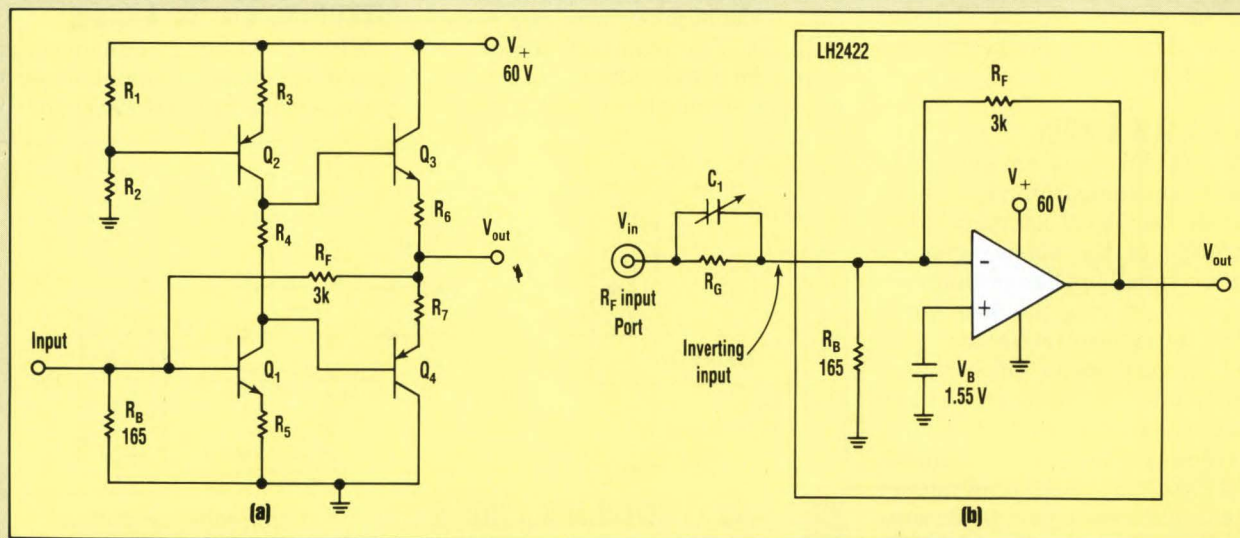
Note that for proper operation, the input signal must be referred to the same potential as LH2422's internal bias voltage,  $V_B$ . The amplifier's ac gain is given by:

$$A_V = -(R_F/R_G) \quad (\text{eq. 2})$$

An equation that combines the ac and dc components of the signal and gives  $V_{out}$  for any given input signal voltage is:

$$V_{out} = V_B(1 + R_F/R_B + R_F/R_G) - V_{in}(R_F/R_G) \quad (\text{eq. 3})$$

A variable capacitor  $C_1$  called the peaking capacitor can be used to optimize the amplifier's pulse response by peaking the amplifier's frequency response. The peaking network made up of  $R_G$  and  $C_1$  must be driven from a specified source impedance, such as 50  $\Omega$ . By varying  $C_1$ , which should be a 10 pF – 100 pF variable capacitor, excellent rise and fall times can be achieved at the expense of some overshoot in the pulse response.





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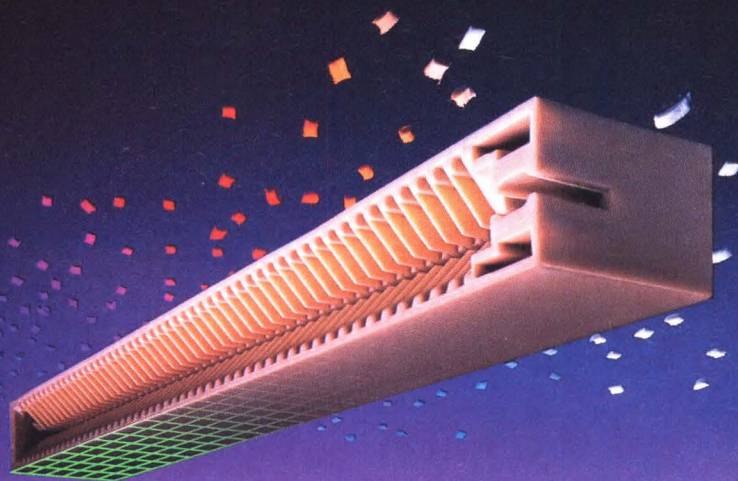
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# DESIGN APPLICATIONS

## DESIGNING VIDEO AMPLIFIERS

need to be driven at different levels to produce a neutral white color. By making the drive resistor ( $R_5$ ) variable, the gains of the green and blue channel preamplifiers can be adjusted relative to that of the red channel. Once the adjustments are made, the contrast control potentiometer can be used to vary the drive level of all three guns simultaneously.

To ensure that the three amplifiers track well over a wide range of contrast adjustment, the contrast capacitor,  $C_9$ , should be common to all three preamplifiers. That's a bit harder to do than it sounds because simply connecting  $C_9$  across pins 13 and 14 of all three LM1201s would lead to instability problems. The fix shown is to parallel the pin 14s together directly, and to insert 10- $\Omega$  decoupling resistors in the lines con-

necting the pin 13s.

Because the three guns within a color tube rarely turn out to be identical, each will cut off at a different cathode potential. Separate adjustments are therefore necessary to ensure that each gun's amplifier has its black level set to the cutoff voltage of its gun. Provided that the variation in cutoff voltage is no more than 15 V, this is easily accomplished by making the feedback resistor,  $R_{11}$ , variable. If the variation exceeds 15 V, as it often will, then the simple fix won't work, and a different approach must be used.

### OPERATING LIMITS

The 15-V limitation for the direct-coupled circuit is dictated by the 70-V absolute maximum rating for the LH2422's power supply. Given the

absolute voltage limit of 70 V, good practice demands that the circuit be operated at 65 V or less. Because the amplifier's linear range extends to within 5 V of each supply rail, the output can swing to a minimum of 5 V and a maximum of just 60 V—a total swing of 55 V.

With the video amplifier coupled directly to the cathode, and the video signal itself swinging 40 V at each cathode, only 15 V is left to accommodate variations between the guns of the color CRT.

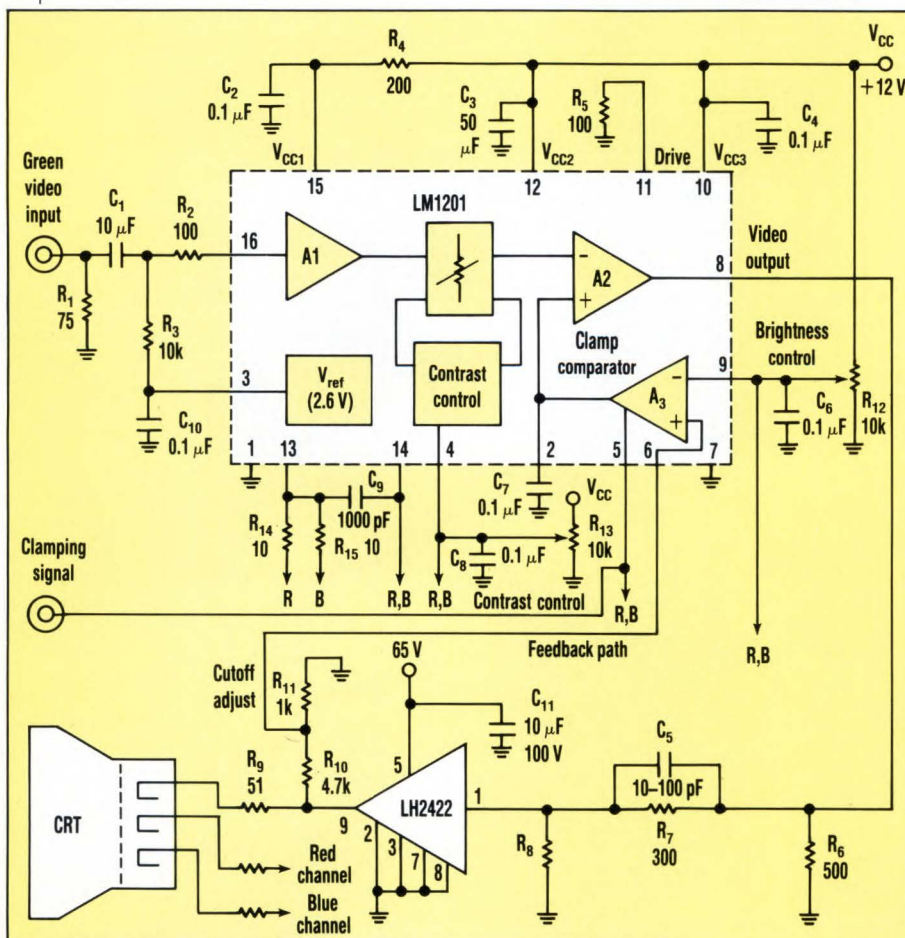
Many color tubes have spreads of more than 25 V in cutoff voltage for the three guns within the same tube. Because the absolute maximum rating of the LH2422 can't be changed, handling those tubes means that the amplifier output can no longer be coupled directly to the cathode. Instead, the output can be ac coupled to the cathode, which works fine except that it causes the dc component of the video signal to be lost. The solution to that problem is to use diode clamping to restore the dc component of the video signal (Fig. 4).

At dc, resistor  $R_1$ , diode  $D_1$ , and potentiometers  $R_2$  and  $R_3$ , clamp the red gun's cathode at a potential determined by the setting of  $R_2$  and  $R_3$ . This is how the cathode of each gun is clamped at its respective cutoff voltage.

At the frequency of interest, capacitors  $C_1$ ,  $C_2$ , and  $C_3$  behave as short circuits and couple the ac video signals to the respective cathodes. Because of the diode clamp circuit, each video signal's black level is clamped to the cutoff potential. Consequently the dc component of the video signals is restored.

Note that potentiometers  $R_3$ ,  $R_6$ , and  $R_9$  allow for the individual adjustment of the cutoff voltage for each gun. Potentiometers  $R_2$ ,  $R_5$ , and  $R_8$  are ganged together, allowing for simultaneous brightness control of all three guns with one knob. The circuit accommodates tubes with a large spread in cutoff voltages and also makes for brighter pictures by biasing the cathode of the CRT at a high voltage.

The disadvantages of the diode clamp circuit are that any fluctua-



**3. THREE IC PAIRS**, one each for the red, green, and blue channels, are needed to build a high-resolution color monitor. It's not too difficult, but care must be taken to ensure proper contrast tracking, and to compensate for the different sensitivities of the different color phosphors.



# DAS 9200 Version 2

Now \$18,000 will  
put the best on  
your bench: the  
DAS 9200.

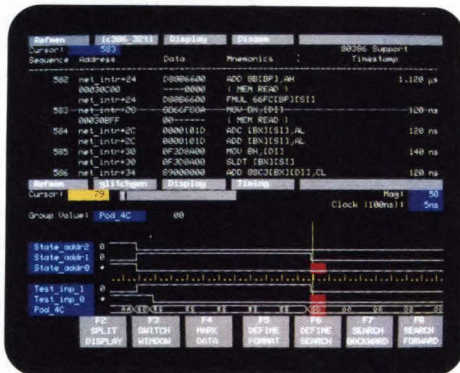
The most impressive number to come out of the Tek DAS 9200 may be its price: now you can leverage the power of the DAS for little more than the cost of systems that aren't even in the same league. Consider:

## 32-bit MICRO SUPPORT

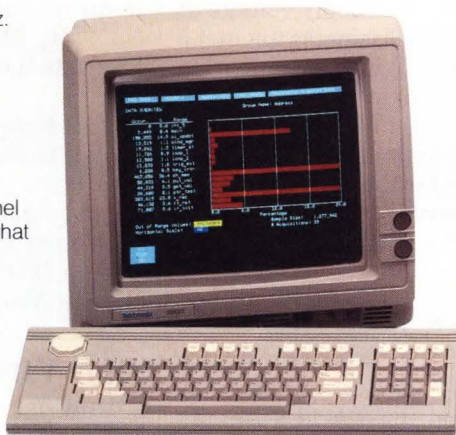
The smoothest, most elegant implementation for chips like the 80386, 68030 and 68020. The most sophisticated triggering of any logic analyzer ever built. Expand to monitor as many as six micros at once, with clock rates to 40 MHz.

## 32 K BITS OF MEMORY DEPTH

That's *minimum* per channel—which is 4 to 32 times what competitive instruments offer at best. And you can keep expanding the DAS acquisition memory up to **128K** bits per channel.



Split screen displays can show microprocessor activity time correlated with high-speed timing data (above) or disassembly of another microprocessor. The cursors can be locked to scroll in parallel, highlighting data nearest to the same point in time.

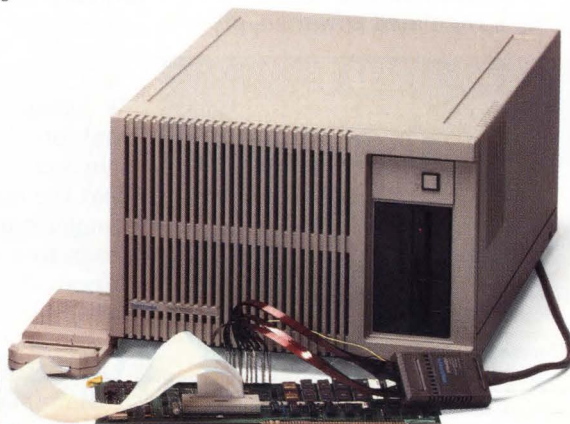


Performance analysis, disassembly, signal passing, color display, pop-up menus, impressive new Release 2 software—all this and much more can be on your bench or in your department for under \$18,000... with vast expandability built in.

**Stop hankering after the DAS 9200, and get your hands on it at last.** For information or a demonstration, contact your Tek sales engineer, or call 1-800-245-2036. In Oregon, 231-1220.

## 90 CHANNELS

Expand up to 540 acquisition channels or, using other modules, up to 160 channels at 2 GHz. Apply up to 1008 stimulus channels at 50 MHz.



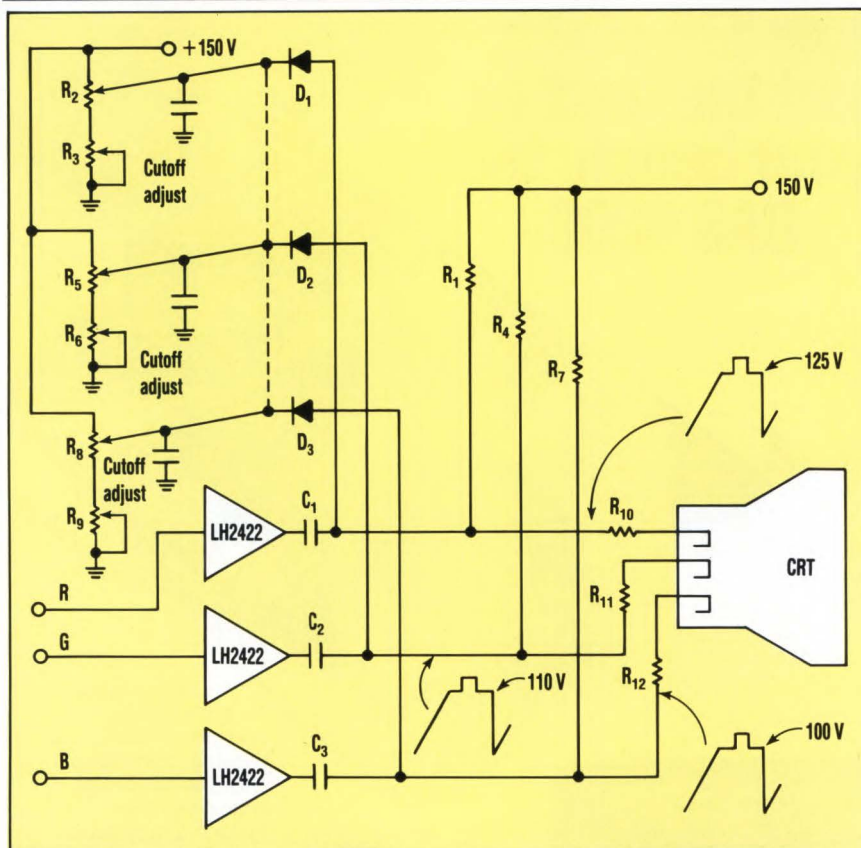
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# DESIGN APPLICATIONS

## DESIGNING VIDEO AMPLIFIERS



**4. MISMATCHED CRT GUNS** require high-voltage cutoff adjustment, which a low-voltage amplifier simply can't supply. This circuit overcomes the problem by ac coupling the amplifier output to the CRT and using a diode clamping circuit for dc restoration.

tions in the power supply line and any noise impulses that couple to the power supply will also couple to the CRT's cathodes. In addition, any drift in the power supply voltage and the diode's forward drop will cause the black level to drift. Most problems can, however, be eliminated by using a regulated power supply and

adequate filtering.

For proper operation, the LH2422 must be heat sunk under all conditions. Its power dissipation increases almost linearly with frequency, which means that it will be maximum during full scale transitions—when alternating black and white stripes are displayed on the screen. In that situation, and at a supply voltage of 60 V, the device dissipates about 4.5 W. Using that figure, assuming an ambient temperature (inside the monitor cabinet) of 50°C, and noting that the maximum permissible case temperature for the LH2422 is 80°C, leads to a maximum thermal resistance value for a heat sink of  $(80^{\circ}\text{C} - 50^{\circ}\text{C})/4.5\text{ W} = 6.7^{\circ}\text{C/W}$ .

### CHOOSING A NEAT SINK

Many such heat sinks are available commercially, such as the Thermalloy 15509 and the AAvid 61875. To get the best possible results from those heat sinks, follow the follow-

ing four guidelines:

- Use a thermal joint compound between the heat sink and the LH2422's metal tab. Thermal joint compound is a thermally conducting grease that lowers the thermal resistance between the device package and the heat sink by filling in the air gaps between them.
- Apply adequate torque to the heat sink so that good thermal contact is established.
- Mount the heat sink vertically. This will cause it to lose heat quickly through convection, and is especially useful for heat sinks with fins (such as the Thermalloy 15509 or the AAvid 61875).
- Paint the heat sink with black oil paint or apply a dark varnish. That will further reduce the heat sink's thermal resistance by improving its radiation heat transfer. □

The author thanks Ron Page, designer of the LM1201, and Tom Mills, designer of the LH2422, for their assistance. Thanks also to Mike Parsin.

### Bibliography

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Tainsky, Steve, "Video Amplifier Design: Know Your Picture Tube Requirements," Application Note No. 761, Motorola Semiconductor Products Inc., 1976.

Zahid Rahim, a senior applications engineer at National Semiconductor Corp., has a B.A. in mathematics and physics from Wartburg College, Waverly, Iowa, and an MSEE from Columbia University, New York City.

**TABLE 2:**  
**KEY SPECIFICATIONS**  
**OF THE LH2422**

Typical specifications at  $V_+ = 60\text{V}$ ,  $C_L = 8.5\text{ pF}$  and  $T_A = 25^{\circ}\text{C}$

Parameter	Specification
Output dc voltage	30 V
Rise time at $V_{out} = 40\text{ V}_{pp}$	3 ns
Effective B.W (f-3dB) at $V_{out} = 40\text{ V}_{pp}$	120 MHz
Output voltage range	5 V to 55 V
Linearity error	1 %
Overshoot	10% (externally adjustable to 0%)

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MODERATELY  
SLIGHTLY

### CIRCLE

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557  
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.0435  $\mu$ H - 1.5  $\mu$ H  
49 shielded, 49 unshielded (2 of each)  
Kit M102 \$60

## "Slot Ten" 10 mm Tuneable Inductors

0.7  $\mu$ H - 1143  $\mu$ H  
18 shielded, 18 unshielded (3 of each)  
Kit M100 \$60

## Surface Mount Inductors

4 nH - 33  $\mu$ H  
48 values (10 of each)  
Kit C100 \$125

## Axial Lead Chokes

0.1  $\mu$ H - 1000  $\mu$ H  
25 values (5 of each)  
Kit F101 \$50

## Horizontal Mount Inductors

Tuneable and fixed  
Inductance: 31.5 - 720 nH  
33 Values (6 of each)  
Kit M104 \$60

## Common Mode Data Line Filters

Attenuation bandwidth: 15 dBm, 1.5-30 MHz  
DC current capacity: 100 mA  
2, 3, 4 and 8 line styles (4 of each)  
Kit D101 \$65

## Common Mode Line Chokes

Current: .25 - 9 amps RMS  
Inductance: 508  $\mu$ H - 10.5 mH  
8 styles (2 of each)  
Kit P202 \$100

## Current Sensors

Sensing range: 0.5-35 amps  
Freq. resp.: 1 - 100 kHz, 50 - 400 Hz  
Transformer and sensor-only versions  
8 styles (15 total pieces)  
Kit P203 \$50

## Base/Gate Driver Transformers

Inductance: 1.5 mH Min.  
Frequency: 10 - 250 kHz  
2 single, 2 double section (2 of each)  
Kit P204 \$50

## Mag Amp Toroids

Current: 1, 5 amps  
Volt-time product: 42 - 372 V- $\mu$ sec  
6 styles (2 of each)  
Kit P206 \$100

## Power Filter Chokes

Current: 3, 5, 10 amps  
Inductance: 5 - 300  $\mu$ H  
18 styles (48 total pieces)  
Kit P205 \$75

## Axial Lead Power Chokes

Current: .03-4.3 amps  
Inductance: 3.9  $\mu$ H - 100 mH  
60 styles (2 of each)  
Kit P209 \$150



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SPECIFICATIONS (typical)	SCM-1L SCM-1NL (L=with leads)	SCM-2L SCM-2NL (NL=no leads)
FREQ. RANGE (MHz)		
LO, RF	1-500	10-1000
IF	DC-500	DC-500
CONVERSION LOSS (dB)		
Midband	6.3 dB	6.5 dB
Total Range	7.5 dB	8.0 dB
ISOLATION (dB)	(L-R)(L-I)	(L-R)(L-I)
Low-Band	60 45	45 35
Mid-Band	45 40	35 30
High-Band	40 35	25 20
PRICE	\$3.30 (1000 qty) \$4.25 (1-9)	\$4.15 (1000 qty) \$5.45 (1-9)

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

\*NOTE: L & NL suffix for ordering only  
Not marked on units.

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# Annual "Ideas For Design" Contest

Welcome to ELECTRONIC DESIGN's Annual "Ideas for Design" Awards Contest. On the following pages, we have included the 24 best-of-issue winners for the year beginning June, 1988, and ending May, 1989. We are asking you, the readers of ELECTRONIC DESIGN, to select the best idea of the year.

Please look over these entries carefully and cast your vote for the one idea (only one, please) that you feel is the year's best by circling the appropriate number on the Reader Service Card. The winner, who will be announced when the votes are tallied, will receive a cash award of \$1500.

A few points about this section:

When casting your ballot, please concentrate on the broad significance of the idea as well as its cleverness—its breadth of applications and its

contribution to the art of design.

Because of space constraints, we have only reprinted the circuit or block diagram for each idea, along with a brief write-up describing the intent of the circuit. Although we couldn't include all of the details of circuit operation, we did include a reference to the issue date and page number for each entry. Layout restrictions also prevented us from publishing the entries in chronological order.

You may want to go through this section and narrow your potential choices down to three or four, and then refer back to the original issue, where the entry appeared in its entirety.

The author's name and company affiliation are omitted to avoid any bias for or against the author's company or multiple winners. Some authors won the best-of-issue contest more than once and their names would have appeared in multiple locations here.

## **CIRCLE** 524 SYNTHESIZER VARIES WAVEFORM, FREQUENCY

Digital waveform synthesizers have significantly better waveform accuracy and stability than their analog counterparts. High-speed registered PROMs and a high-performance ad-

ressing generator make possible a wide range of waveform and frequency control. One address generator (IC<sub>1</sub>) supplies an 8-bit address for a 256-by-8-bit ROM space, consisting

of two 256-by-4-bit PROMs, which contain the waveform shapes. Another address generator (IC<sub>2</sub>) subdivides an Input Clock frequency to modulate the output waveform frequency. To reconstruct the analog waveform, an 8-bit output from the PROM feeds into a fast digital-to-analog converter. Switch S2 selects between the two sets of addresses load-

### DEMONSTRATION INSTRUCTION SEQUENCE

WAVEFORM 1					WAVEFORM 2			
CIRCLE NO.	Mnemonic	Operational Code	Data IC <sub>1</sub>	Data IC <sub>2</sub>	Mnemonic	Operational Code	Data IC <sub>1</sub>	Data IC <sub>2</sub>
1	CLRCR	7H	XX	XX	CLRCR	7H	XX	XX
2	LCRDI	4H	XX	XX	LCRDI	4H	XX	XX
3	LIRDI	CH	00H	00H	LIRDI	CH	80H	00H
4	LS1DI	8H	00H	NN	LS1DI	8H	00H	NN
5	LCPDI	EH	00H	00H	LCPDI	EH	80H	00H
6	CCJS1	1H	7FH	00H	CCJS1	1H	FFH	00H
7	CCJS1	1H	XX	XX	CCJS1	1H	XX	XX
etc.								

Notes: 1.XX = Don't care

2.NN = Step size from switch S1

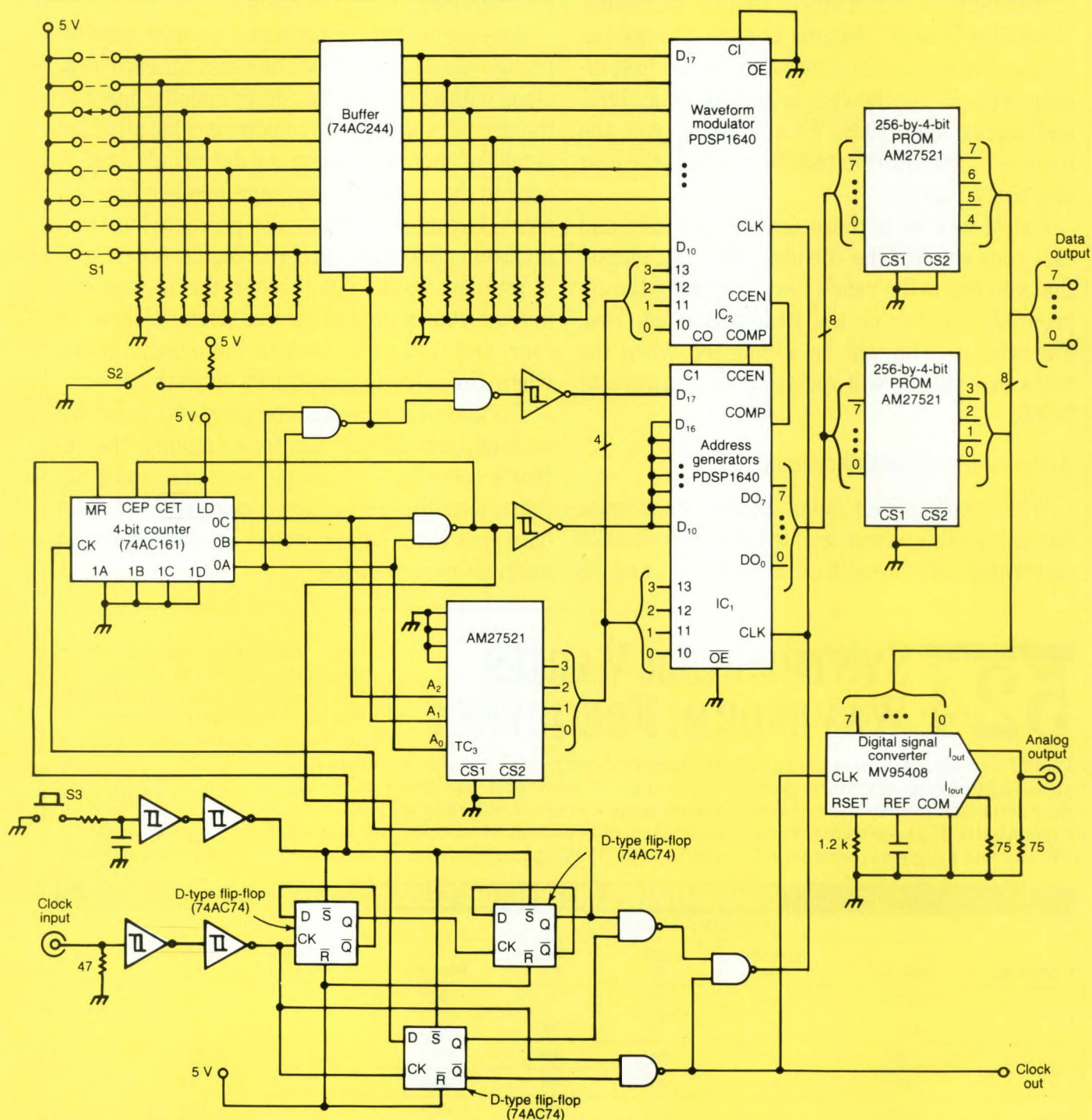


## IDEAS FOR DESIGN

ed into IC<sub>1</sub>, depending on the selected waveform. The program in the waveform modulator IC<sub>2</sub> causes IC<sub>1</sub> to continually cycle through addresses

OOH to FFH in step sizes selected by switch S1. Step sizes vary in powers of two, from 2<sup>0</sup> to 2<sup>7</sup>. The step size determines the input clock's division

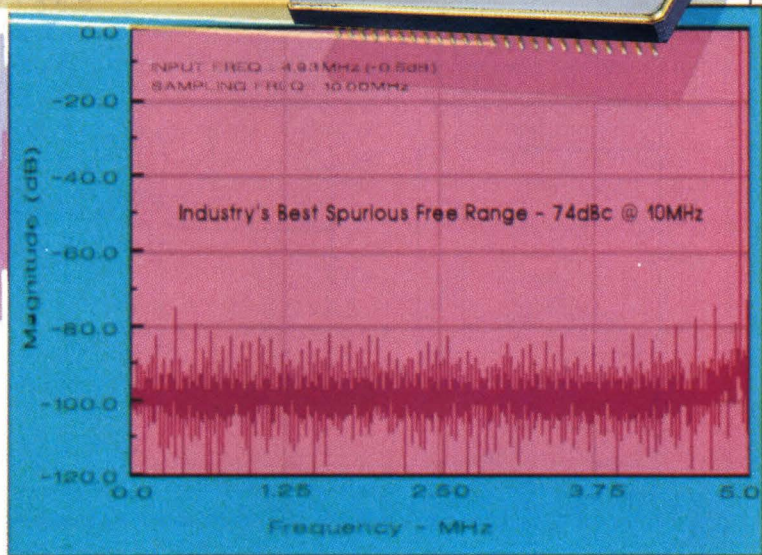
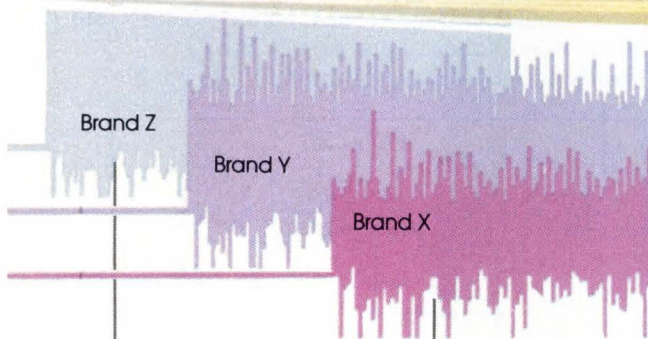
ratio, which in turn sets the generated waveform frequency; the larger the step, the higher the frequency. □  
(Winner, June 9, 1988, p. 128)



**ONE 40-MHZ CMOS PDS1640** address generator (IC<sub>1</sub>) supplies an 8-bit address for a 256 by 8-bit PROM, which consists of two AM27521, 256 by 4-bit PROMs containing two waveform shapes. Another PDS1640 (IC<sub>2</sub>) subdivides an input clock frequency to modulate output waveform frequency. An 8-bit output from the PROM feeds into a fast MV95408 d-a converter to reconstruct the analog waveform.



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## 100% TESTED SPECIFICATIONS (at 10MHz sample, 5MHz input)

	ADC603 K Grade		ADC603 J Grade	
	25°C	Over Temp	25°C	Over Temp
IMD, max (8MHz Sample)	-71dBc	-68dBc	-67dBc	-64dBc
SINAD, min	62dB	61dB	60dB	57dB
Spurious Free Dynamic Range, max	-66dBc	-65dBc	-63dBc	-60dBc
THD, max	-64dBc	-62dBc	-61dBc	-58dBc
SNR, min	66dB	64dB	63dB	60dB

Price*	\$941.00	\$590.00
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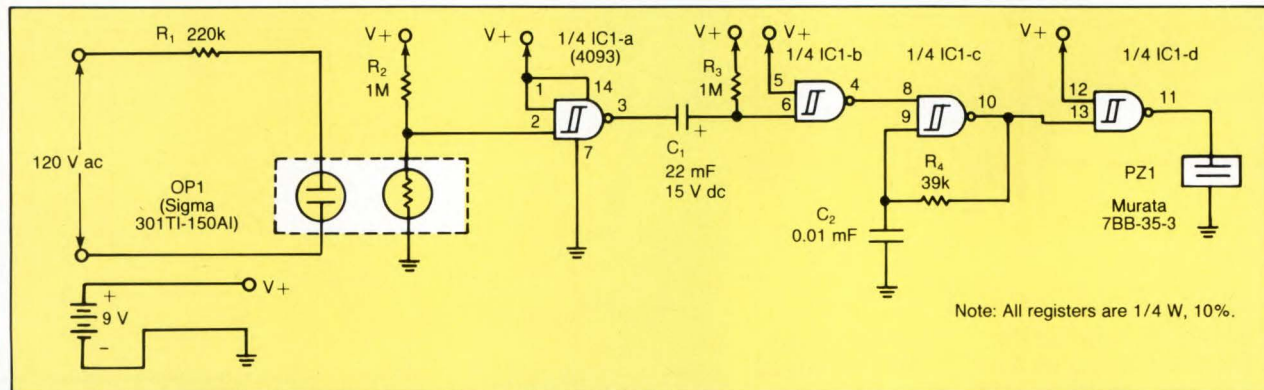


# CIRCLE 525 POWER-LOSS ALARM PROTECTS EQUIPMENT

Expensive damage to vital equipment can occur if the power fails without warning. Sounding an alarm when the power goes out is often es-

sential so that proper action can be taken. An inexpensive, compact, and reliable solution is an ac power-loss alarm. This circuit plugs directly into

a 120-V ac outlet. Upon power loss, the circuit generates an audible warning for about 30 seconds. The alarm doesn't sound again until the power comes on and goes out once more. Quiescent current from a 9-V battery is 5  $\mu$ A, making battery life about equal to shelf life.  $\square$   
(Winner, August 25, 1988, p. 116)



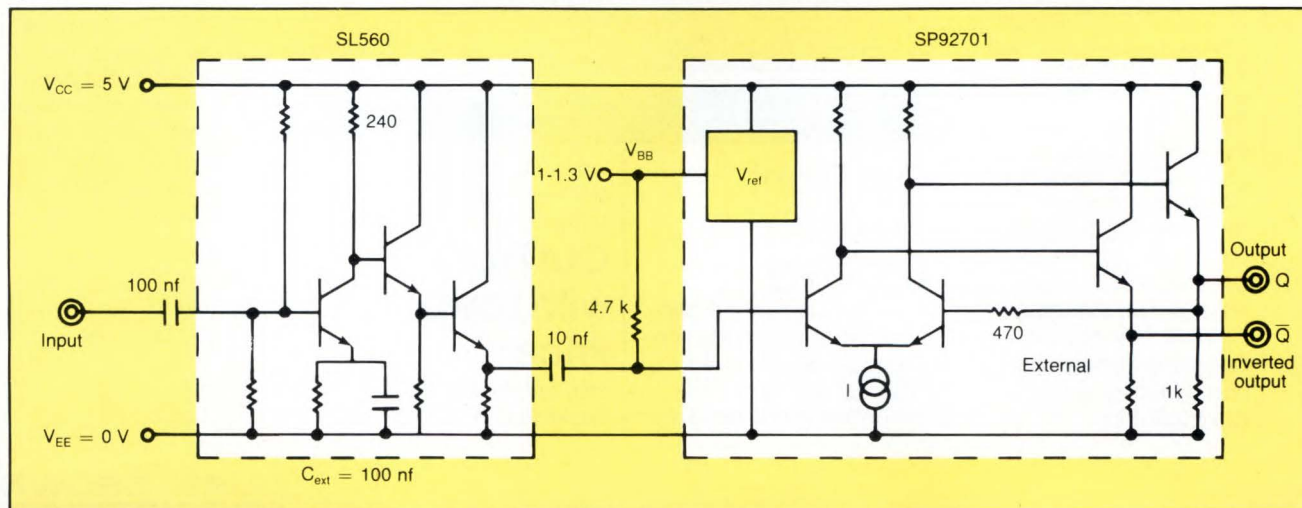
**THE CIRCUIT'S OPTOISOLATOR (OP1)** consists of a neon lamp and photocell. A power loss triggers the monostable multivibrator, which consists of capacitor  $C_1$ , resistor  $R_3$ , and IC1-a. The monostable, in turn, activates the stable multivibrator, consisting of IC1-c, resistor  $R_4$ , and capacitor  $C_2$ , for about 30 seconds. The astable multivibrator, operating at a frequency of about 2.6 kHz, feeds a piezoelectric alarm sounder, PZ1, through IC1-d, which acts as a buffer/driver.

# CIRCLE 526 DIGITAL LINE DRIVER DOES ANALOG DUTY

Most analog systems require at last one pair of differential transistors to glue together the parts of a complete system. Discrete transistors or a

transistor array are convenient, but they often need a current source to supply a reasonable common-mode range and a stable bias voltage for

single-ended operation. This circuit uses an SP92701 ECL line driver, designed for high-speed digital applications, and a low-noise high-speed SL560 preamplifier. The performance is often much better than or at least equal to that of hybrids, which can cost 50 times as much.  $\square$   
(Winner, July 28, 1988, p. 154)



**ADDING A LOW-NOISE, HIGH-SPEED SL560** preamplifier to the SP92701 ECL line driver delivers a gain of 30 dB with a 300-MHz bandwidth flat to within  $\pm 1$  dB. The circuit's complementary output can drive a 100- $\Omega$  twisted pair from a single-ended analog source. The SP92701 includes a current source in its input differential-transistor pair, a voltage reference, and a pair of emitter-follower output drivers.



# PURE SIGNAL

## LOW SSB PHASE NOISE OF $-140\text{dBc}$

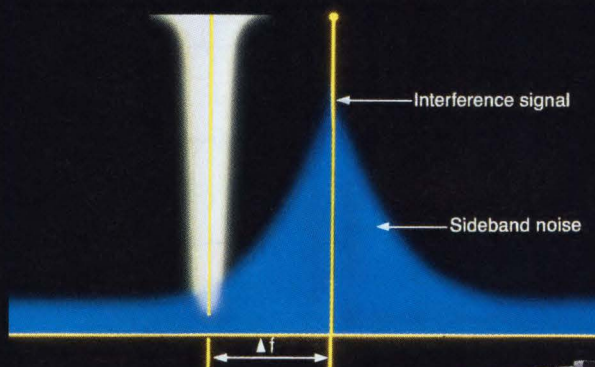
Anritsu's MG3633A Synthesized Signal Generator reduces sideband noise to  $-140\text{dBc/Hz}$  (20kHz offset from 1GHz signal), for the most precise performance and characteristics evaluation of all bands of radio communications equipment, even quasi-microwave.

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### SYNTHESIZED SIGNAL GENERATOR MG3633A



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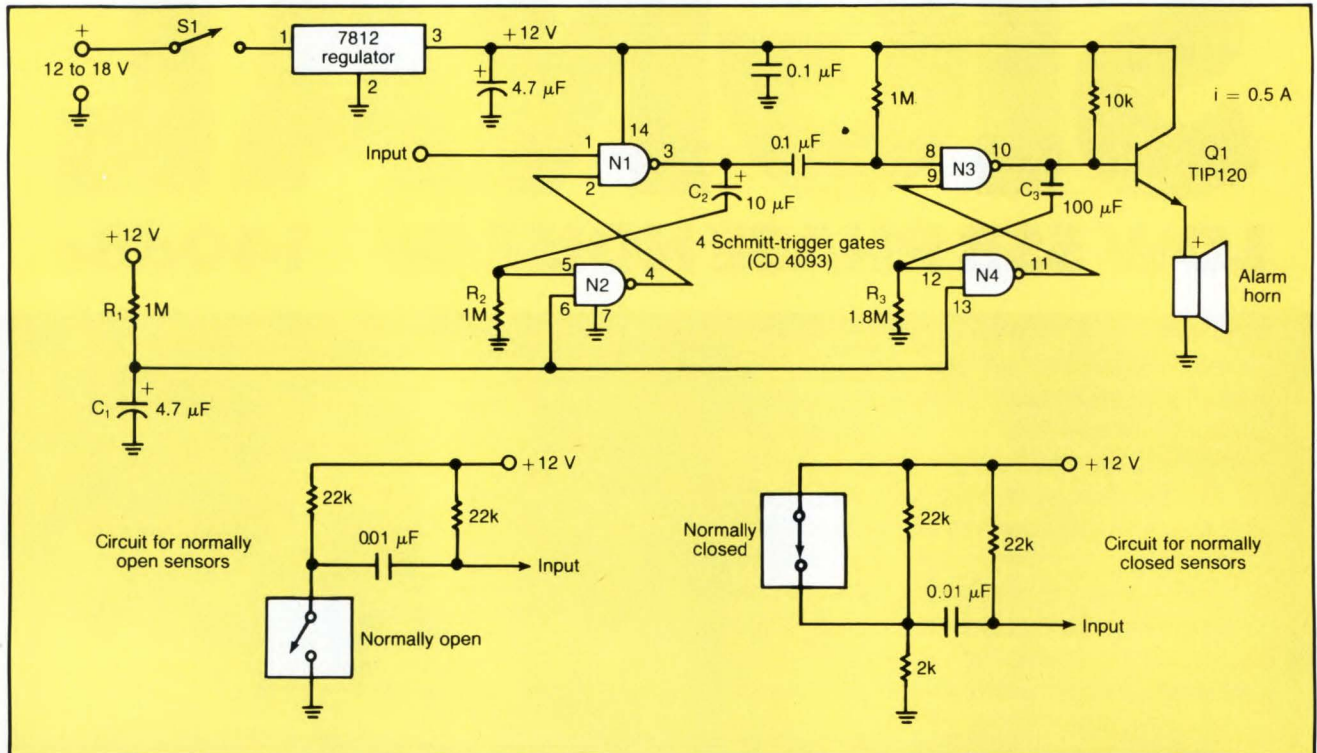
# CIRCLE 527 ALARM USES IC, TRANSISTOR, REGULATOR

The features found in most alarm systems for homes or cars can be built around one integrated circuit, a power transistor, and a 12-V voltage

regulator. A hidden switch (S1) inside the car or the house turns on the alarm. The circuit inhibits it for 34 seconds before becoming active to

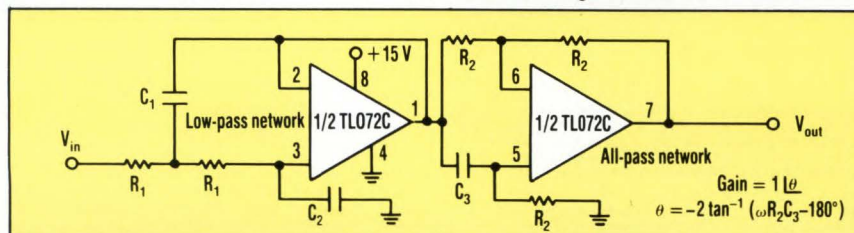
let the user exit and close the door without problems. The  $R_1C_1$  network controls this time delay. The time to disarm the alarm when a door or window opens is determined by the time constant of  $R_2C_2$ . The time that the siren sounds is set by the time constant of  $R_3C_3$ . □

(Winner, July 14, 1988, p. 123)



**WHEN THE VOLTAGE** across  $C_1$  reaches a threshold value, the inputs of the Schmitt-trigger NAND gates (N2 and N4) go to a high state, enabling the two monostable circuits that include N2 and N4. The alarm can then detect the opening of a door or a window by a negative pulse from a sensor switch. The pulse triggers the first monostable, causing its output to go high for almost 11 seconds to give time to disarm the alarm. When this pulse ends, the first monostable triggers the second, which turns on transistor Q1 to sound the alarm.

# CIRCLE 528 CROSSOVER NETWORKS ARE PHASE EQUALIZED



**1. THE BASIC BUILDING BLOCK** for implementing a crossover filter consists of a Butterworth low-passed filter of the second order and an all-pass network of the first order. The all-pass network has little effect on phase delay.

quency range (Fig. 1). As a result, a crossover network free of phase-shift errors becomes possible. This equalization occurs because the compensating phase shift caused by an all-pass network of the proper order can be nearly as large as that of a low-pass network of a given order. Two cascaded building blocks, one with a low-frequency low-pass cutoff and the other with a medium-frequency low-passed cutoff, supply the low- and medium-band outputs of a crossover filter when connected in parallel through a differential-input operational amplifier, such as an INA105 (Fig. 2). □

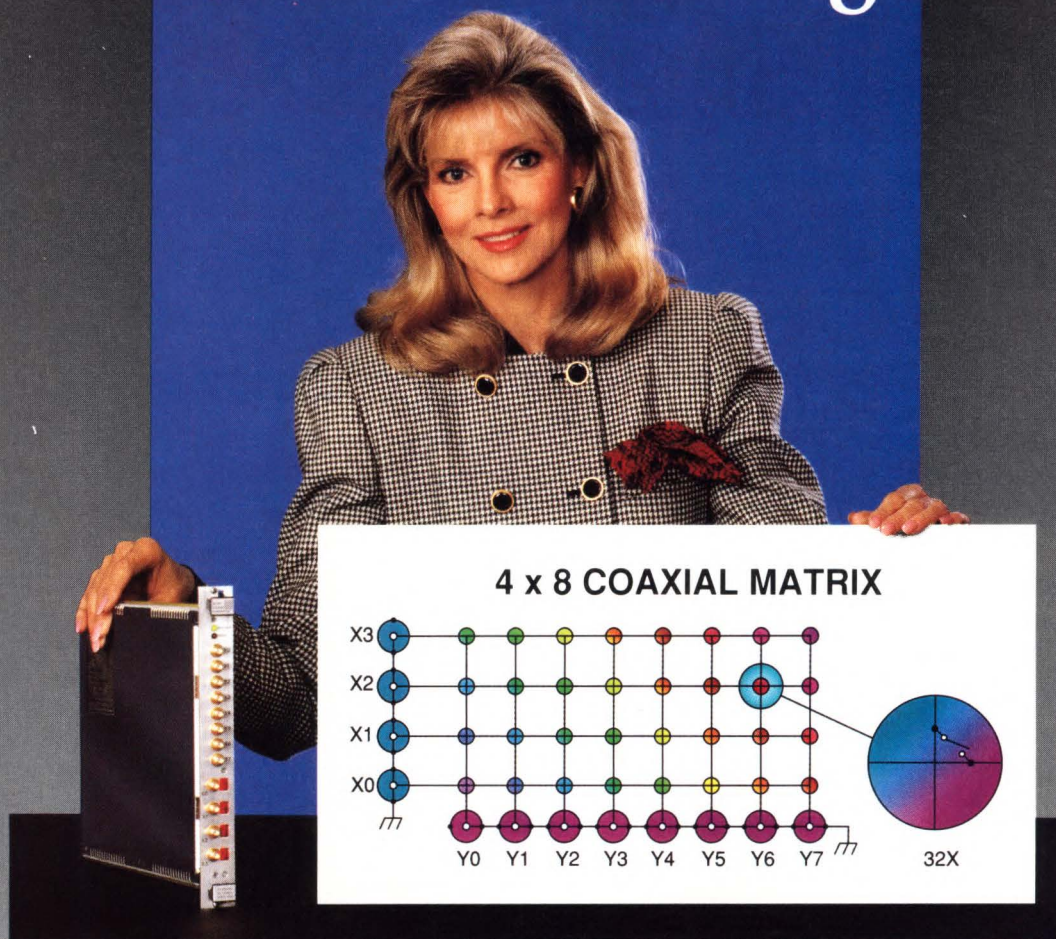
(Winner, Nov. 10, 1988, p. 141)

(cont'd. on p. 80)

When cascaded with a given low-pass network, an all-pass network of the proper order can equalize the overall phase delay over a given fre-



# "For VXIbus Users... The First 4x8 Coaxial DC to 625MHz Switching Matrix"



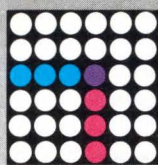
**Here's great news for VXIbus users.** It's the first VXIbus compatible 4x8 coaxial fully shielded message based switching matrix.

Model 10081 comes in a C-size package, and has a frequency range of DC through 625MHz, making it ideal for use in Automatic Test Equipment (ATE) systems where instruments such as frequency counters, signal generators, oscilloscopes, pulse generators, RF analyzers and other broad band devices are to be interconnected using the VXIbus



(Revision 1.3) specifications.

Available in 50 and 75 ohm configurations, Model 10081 has twelve front panel SMA signal connectors to provide



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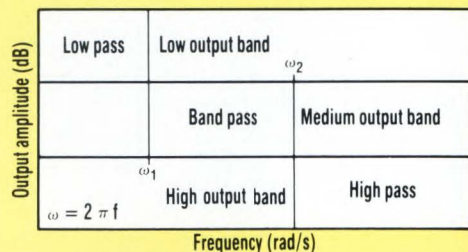
access to the bi-directional coaxial matrix at a switching speed of one milli-second.

Our matrix module also has a handy seven-segment display next to each of the four "X" axis signal connectors to provide front panel indication of any crosspoint with verification.

It's new products such as the VXIbus compatible 10081 switching module that makes Matrix Systems the leader in broad band matrices.

The price is right, too. \$2750 with quantity discounts available.





**2. A THREE-BAND CROSSOVER** filter uses two building-block circuits in cascade and an all-pass circuit, all paralleled through two operational amplifiers. The differential input operational amplifier, INA105, evens out the differences in amplitude between low, medium, and high frequency bands.

# CIRCLE 529

## CLOCK TRACKS SWITCH-CAP FILTER

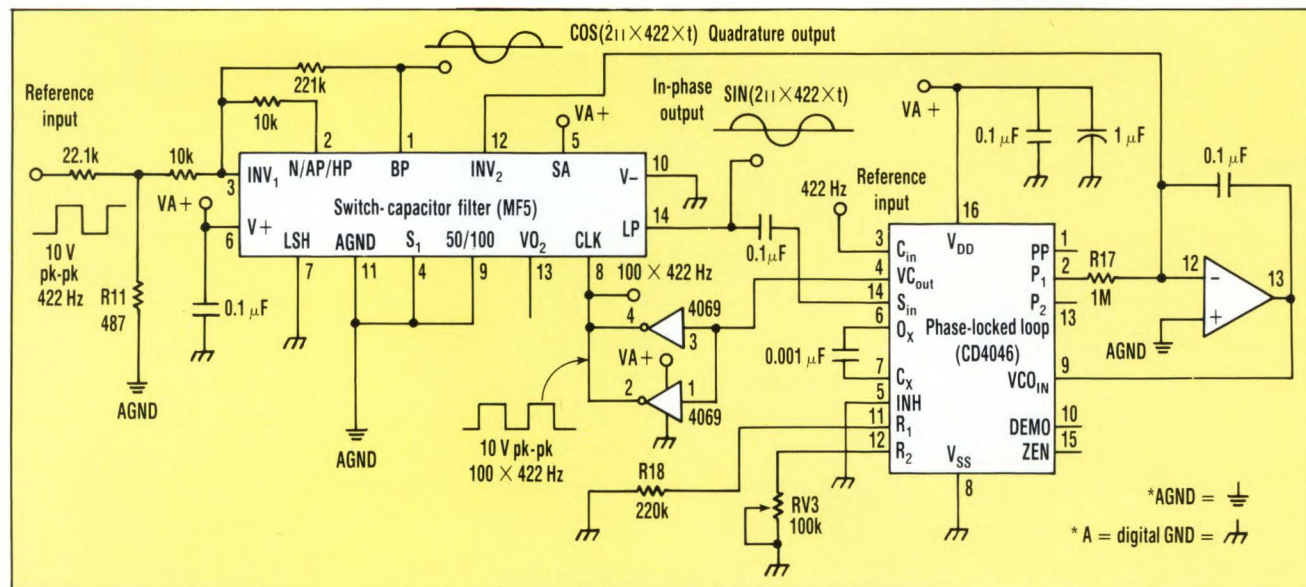
By adding a few standard-tolerance resistors to switched-capacitor filters to determine system gain, you can create single-chip filter building

blocks with better than 0.1% cutoff frequency accuracies. But switched-capacitor filters need a clocking signal that's a fixed multiple of the fil-

## COMPARATIVE ANALYSIS OF FILTER TOPOLOGIES

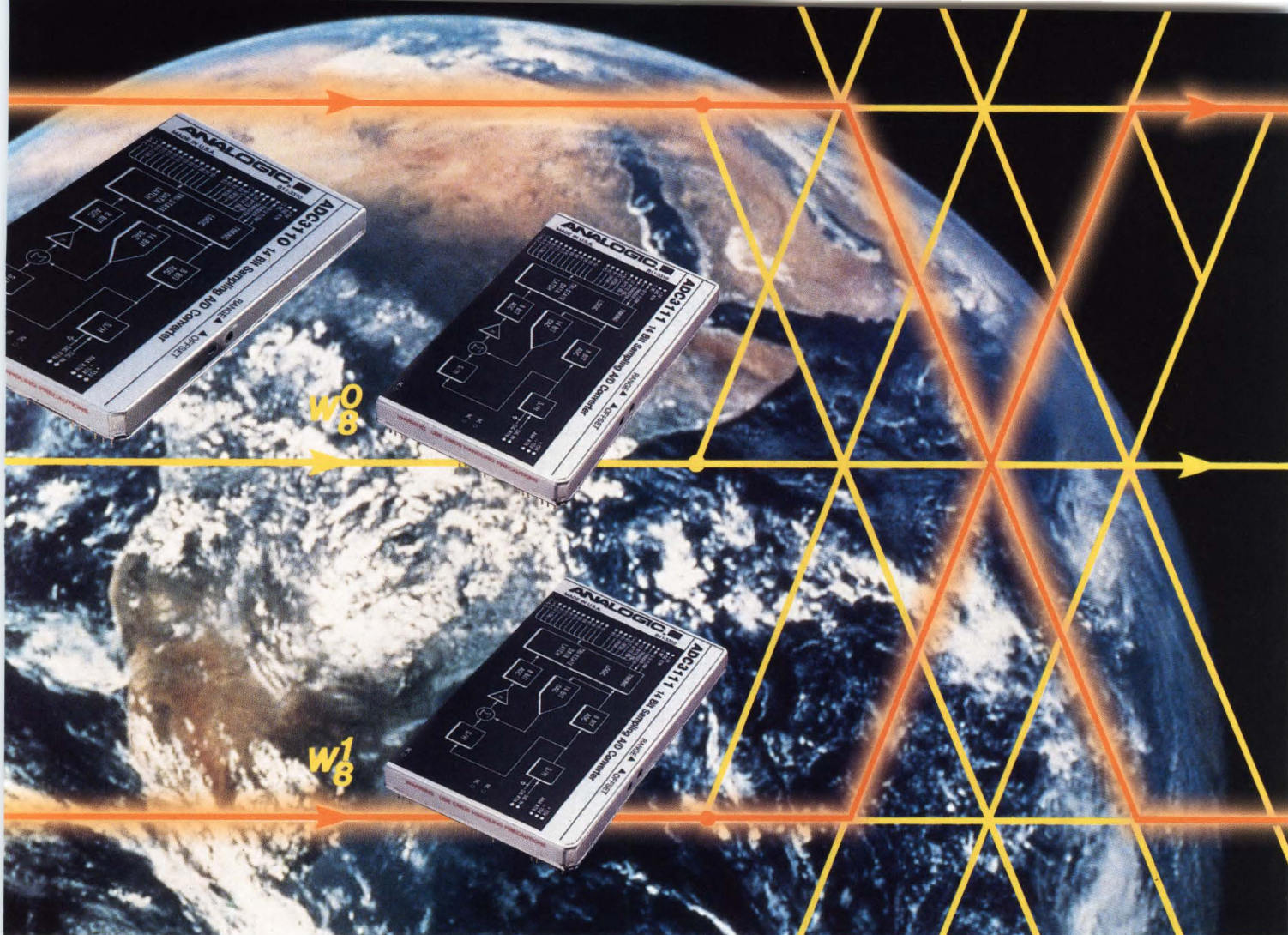
Filter type	Delay (D) in seconds
1. Butterworth low-pass of the 4th order	1.296503128
2. Butterworth low-pass of the 4th order plus equalizer of the first order	0.7279840
Butterworth low-pass of the 4th order plus equalizer of the second order	-0.7463950866
3. Two Butterworth low-pass networks of the second order in cascade	0.585784962
4. Two Butterworth low-pass networks of the second order in cascade with an equalizer of the second order	0.585784962
5. One Butterworth low-pass network of the second order without an equalizer	0.2928920
6. One Butterworth low-pass of the second order in cascade with an equalizer of the first order	0.0287793211

ter's cutoff frequency. For the MF series, the multiple is 50 or 100. Some applications (such as adaptive filtering) require the filter transfer-function cutoff frequencies to track a varying signal frequency within the system. A locked-loop system can overcome these clocking problems. □ (Winner, January 12, 1989, p. 131)

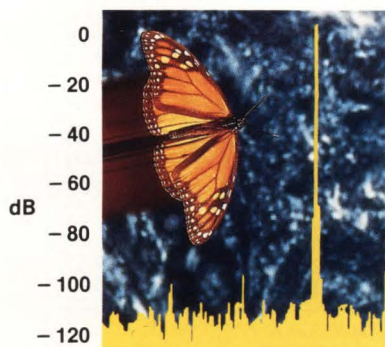


**AN INPUT SIGNAL** to the switched-capacitor filter feeds through to the locked-loop IC, which then feeds back a clocking signal to the switched-capacitor filter. In this way, the circuit automatically determines the proper filter clock-frequency multiple and the filter's frequency response tracks the input signal frequency. The active integrators in the MF5 ensure that the phase relationship between the MF5's LP (pin 14) and BP (pin 1) outputs is always 90°. These signals can serve as quadrature signals with a system, if needed.





## Our A/D's Were Designed to Give You Butterflies!



*True 14-Bit  
Performance  
at a 2 MHz  
Sampling Rate*

\* The illustrated flow graph of the Cooley-Tukey algorithm is known in the industry as a butterfly computation.


Analogic's new, ultra stable 14-bit sampling A/D converters make the most of your post-processing computations. Using advanced hybrid and surface mount technology, these sampling A/D's provide the most cost-effective solution to your high speed, high resolution applications.

The ADC3110 and ADC3111, designed for low noise and low distortion, provide 14 bits of resolution with true 14-bit performance. A 76 dB signal-to-noise ratio and our guarantee of no missing codes over an operating temperature range of 0°C to 60°C make these units unique. The ADC3110 in the time domain and the ADC3111 in the frequency domain will digitize signals up to 1 MHz at a 2 MHz rate, thus achieving unprecedented speed vs. accuracy performance.

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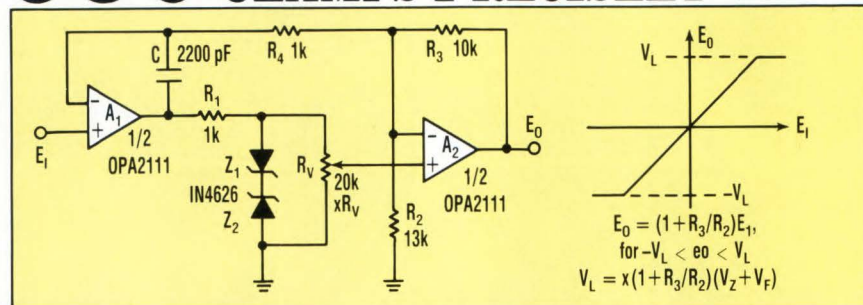
We even pledge it in writing. Unlike other manufacturers, Analogic puts all our sampling A/D's through exhaustive tests on our proprietary automatic test systems. The test data shipped with each product is our proof that it meets or exceeds our published specifications. What else would you expect from the world resource for A/D converter technology?

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The World Resource  
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# CIRCLE 530 FEEDBACK CIRCUIT CLAMPS PRECISELY



**AMPLIFIER A1 BUFFERS** and amplifier A2 scales input signals under feedback control. Zener diodes and a potentiometer or voltage divider in the feedback loop supply a continuously variable bipolar-clamping limit. For frequency stability, resistor  $R_1$  and capacitor  $C$  supply a frequency roll-off in A1. At high frequencies, the capacitor shorts the output of A1 to its inverting input. Then A1 and A2 have independent feedback loops.

A limiter circuit consisting of an input buffer (A1), an output-scaling amplifier (A2), two zener diodes ( $Z_1$  and  $Z_2$ ) and several other components can supply sharp, precise, bipolar clamp levels with continuous variable control, from 0 to  $\pm 11$  V.A feedback loop enclosing the amplifiers and zeners generates the high clamping accuracy. The 5% tolerances of the zener voltages determine the basic accuracy of the clamp levels. However, adjusting the gain with  $R_2$  and  $R_3$  can compensate for any zener-voltage error and resistor tolerances. With matched zeners, the adjustment can readily reduce the clamp-level errors to less than 1%. □

(Winner, Feb. 23, 1989, p. 89)

# CIRCLE 531 CIRCUIT ANNOUNCES AC-LINE VOLTAGE

With a few passive components and a speech-processor chip, a circuit can announce the measured voltage of ac lines, from 100 to 140 Vac, with a res-

olution of 1 V (see the figure, p.95). The speech chip interprets an 8-bit binary code from an analog-to-digital converter. The processor's pulse-

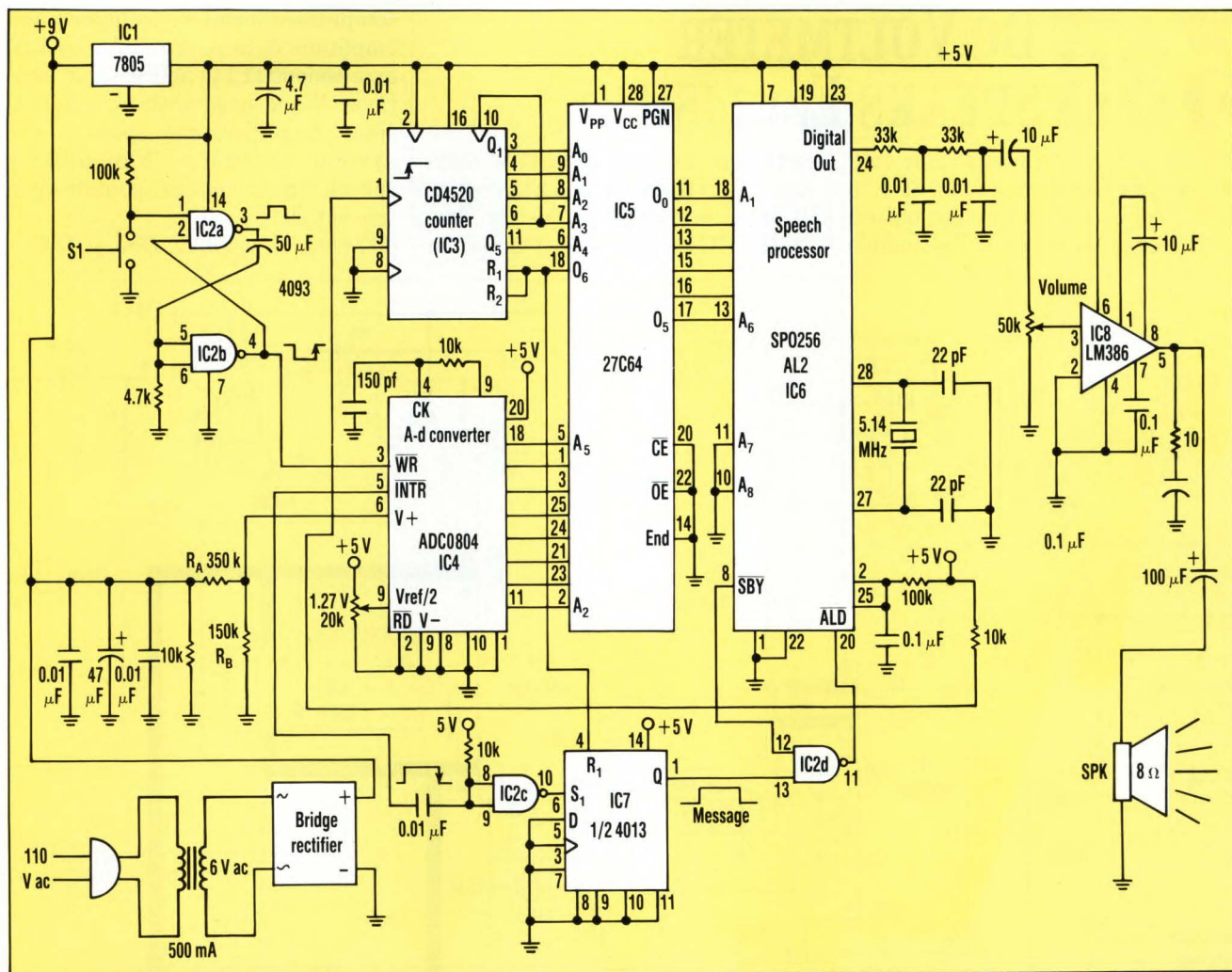
code-modulated output then passes through a filter and amplifier before driving the speaker to vocalize the corresponding number. Each time S1 is pressed, the speech-processor program enunciates the voltage readings, depending on the code at the input of a 27C64 EPROM. □

(Winner, January 26, 1989, p. 130)

## EPROM PROGRAM FOR THE AC-VOLTMETER

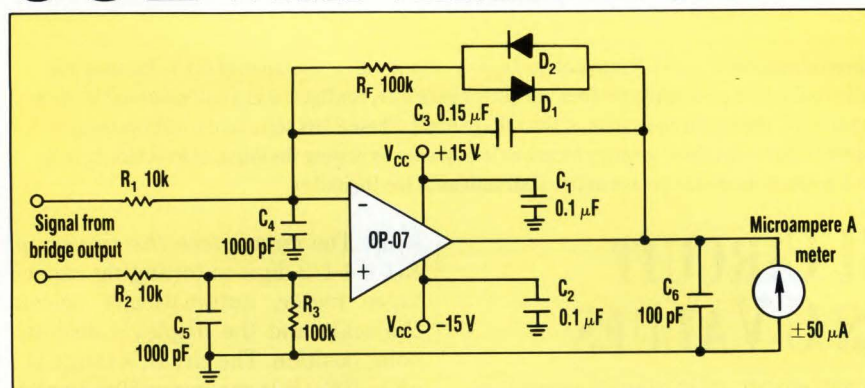
HEX ADDRESS	HEX DATA	HEX ADDRESS	HEX DATA
C20	2E,F,F,B,39,F,F,B,21,27,C,C,15,23,35,2D,D,37,4,44	FC0	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,2E,F,F,B,23,35,2D,D,37,4,44
C40	2E,F,F,B,39,F,F,B,21,27,C,C,15,2E,F,F,B,23,35,2D,D,37,4,44	FE0	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,D,1F,23,35,2D,D,37,4,44
C60	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,1F,23,35,2D,D,37,4,44	1000	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,D,1F,23,35,2D,D,37,4,44
C80	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,E,13,23,35,2D,D,37,4,44	1020	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,1D,E,13,23,35,2D,D,37,4,44
CA0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,E,13,23,35,2D,D,37,4,44	1040	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,1D,E,13,23,35,2D,D,37,4,44
CO0	2E,F,F,B,39,F,F,B,21,27,C,C,15,28,28,3A,23,35,2D,D,37,4,44	1060	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,28,28,3A,23,35,2D,D,37,4,44
CE0	2E,F,F,B,39,F,F,B,21,27,C,C,15,28,28,3A,23,35,2D,D,37,4,44	1080	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,28,28,6,23,4,44
D00	2E,F,F,B,39,F,F,B,21,27,C,C,15,28,28,6,23,23,35,2D,D,37,4,44	10A0	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,37,37,C,29,37,23,35,2D,D,37,4,44
D20	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,C,2,29,37,23,35,2D,D,37,4,44	10C0	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,37,37,C,29,37,23,35,2D,D,37,4,44
D40	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,C,2,29,37,23,35,2D,D,37,4,44	10E0	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,37,37,C,29,37,23,35,2D,D,37,4,44
D60	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,7,7,23,C,B,23,35,2D,D,37,4,44	1100	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,14,2,D,23,35,2D,D,37,4,44
D80	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,7,7,23,C,B,23,35,2D,D,37,4,44	1120	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,38,18,6,b,23,35,2d,d,37,4,44
DA0	2E,F,F,B,39,F,F,B,21,27,C,C,15,14,2,D,23,35,2D,D,37,4,44	1140	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,23,35,2d,d,37,4,44
DC0	2E,F,F,B,39,F,F,B,21,27,C,C,15,14,2,D,23,35,2D,D,37,4,44	1160	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,2E,F,F,B,23,35,2D,D,37,4,44
DE0	2E,F,F,B,39,F,F,B,21,27,C,C,15,38,18,6,B,23,35,2D,D,37,4,44	1180	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,2E,F,F,B,23,35,2D,D,37,4,44
E00	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,7,7,B,23,35,2D,D,37,4,44	11A0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,D,1F,23,35,2D,D,37,4,44
E20	2E,F,F,B,39,F,F,B,21,27,C,C,15,C,2D,7,7,23,C,B,23,35,2D,D,37,4,44	11C0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,1D,E,13,23,35,2D,D,37,4,44
E40	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,2D,23,23,35,2D,D,37,4,44	11E0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,28,28,3A,23,35,2D,D,37,4,44
E60	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,2D,23,23,35,2D,D,37,4,44	1200	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,28,28,3A,23,35,2D,D,37,4,44
E80	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,13,47,D,13,B,23,35,2D,D,37,4,44	1220	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,28,28,6,23,23,35,2D,D,37,4,44
EA0	2E,F,F,B,39,F,F,B,21,27,C,C,15,28,28,3A,D,13,B,23,35,2D,D,37,4,44	1240	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,28,28,6,23,23,35,2D,D,37,4,44
EC0	2E,F,F,B,39,F,F,B,21,27,C,C,15,28,C,28,D,13,B,23,35,2D,D,37,4,44	1260	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,37,37,C,29,37,23,35,2D,D,37,4,44
EE0	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,C,29,37,D,13,B,23,35,2D,D,37,4,44	1280	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,37,37,7,7,23,C,B,23,35,2D,D,37,4,44
FO0	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,C,29,37,D,13,B,23,35,2D,D,37,4,44	12A0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,14,2,D,23,35,2D,D,37,4,44
F20	2E,F,F,B,39,F,F,B,21,27,C,C,15,37,37,7,23,C,B,D,13,B,23,35,2D,D,37,4,44	12C0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,14,2,D,23,35,2D,D,37,4,44
F40	2E,F,F,B,39,F,F,B,21,27,C,C,15,14,2,d,13,b,23,35,2d,d,37,4,44	12E0	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,38,18,6,B,23,35,2D,D,37,4,44
F60	2E,F,F,B,39,F,F,B,21,27,C,C,15,14,2,d,13,b,23,35,2d,d,37,4,44	1300	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,23,35,2D,D,37,4,44
F80	2E,F,F,B,39,F,F,B,21,27,C,C,15,B,6,B,D,13,B,23,35,2D,D,37,4,44	1320	2E,F,F,B,39,F,F,B,21,27,C,C,15,1D,34,2,D,13,23,35,2D,D,37,4,44
FA0	2E,F,F,B,39,F,F,B,21,27,C,C,15,D,30,7,7,B,D,13,23,35,2D,D,37,4,44		





**A ONE-CHIP, N-CHANNEL MOS DEVICE**, using a stored program to synthesize speech, announces monitored ac-voltage readings between 100 and 140 Vac. The chip contains 59 allophones (sounds) plus five pauses with variable gain.

## CIRCLE 532 GET ACCURATE NULL WITH VARIABLE GAIN



**AN ELECTRONIC NULL DETECTOR** for a bridge has a variable-gain feature for which the op-amp's feedback path needs a dynamic resistance that increases as the input signal drops. Two common signal diodes ( $D_1$  and  $D_2$ ) supply that function.

Bridges are among the most accurate instruments for component-value measurements. But the precision depends on how finely the null detector can discriminate the bridge's final balancing position. The old, delicate, and inconvenient spot galvanometers provided about a  $7\text{-}\mu\text{V/division}$  deflection sensitivity. By contrast, a modern electronic null-detector op-amp circuit offers a sensitivity of about  $2\text{ }\mu\text{V/division}$  much more conveniently and at lower cost. Moreover, with variable gain, the circuit's sensitivity automatically increases as the null signal approaches zero, and the readings repeat perfectly. The circuit can use any general-purpose, low-offset, low-drift op amp, such as the OP-07. □  
(Winner, February 9, 1989, p. 90)



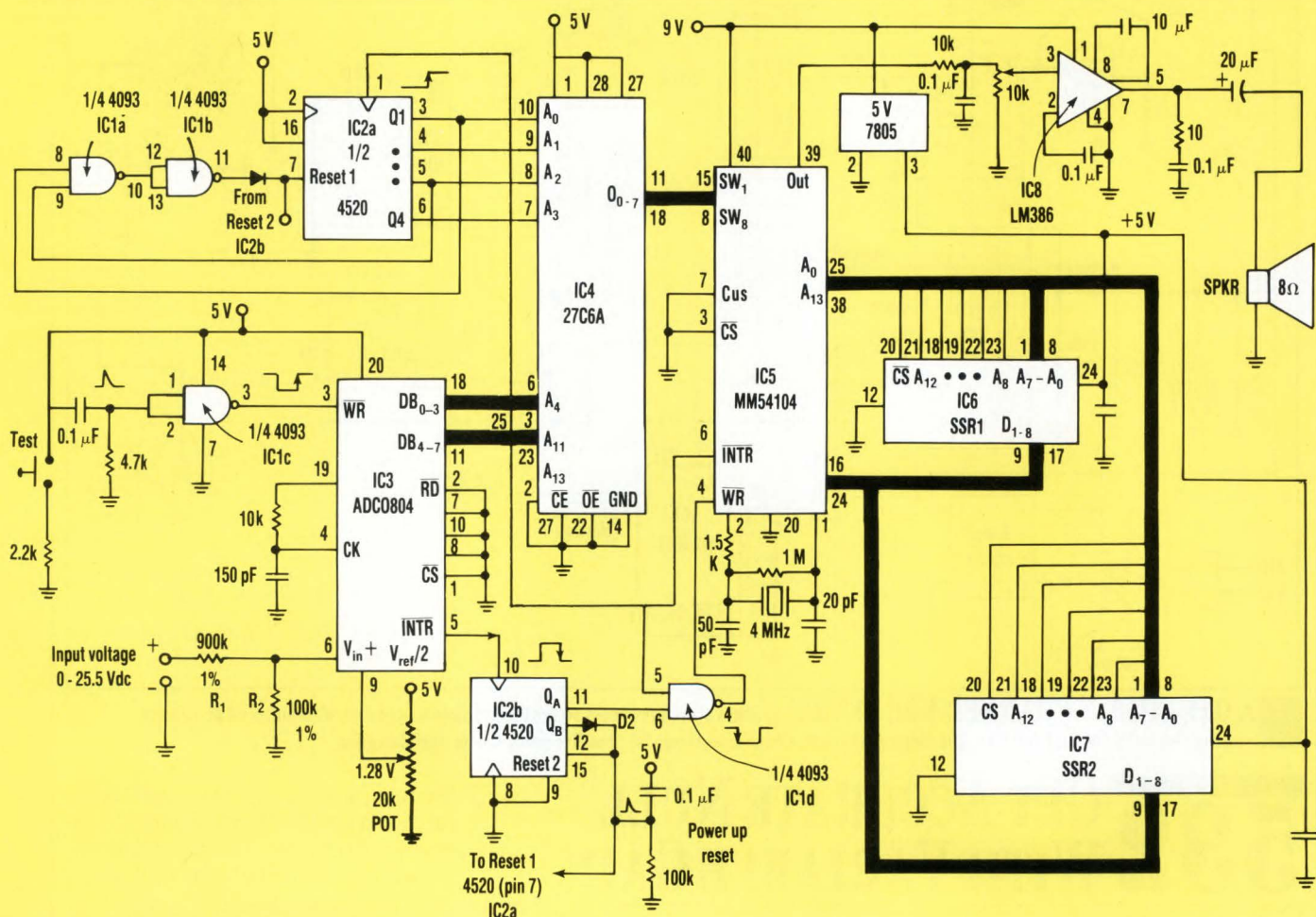
# CIRCLE 533 DC VOLTMETER SPEAKS ENGLISH

For just \$30, you can build a dc voltmeter that converts inputs of 0 to 25.5 V into a plain-English output with a resolution of 0.1 V. The audible

voltmeter uses an MM54104 Digitalker chip from Jameco Electronics (IC5) as the speech synthesizer. Two ROMs (IC6 and IC7) contain (in

compressed form) the frequency and amplitude data required for spoken expressions at 144 addressable locations. When used with an external filter, amplifier, and speaker, the system generates high-quality speech. Each report can contain up to five words. □

(Winner, October 27, 1988, p. 135)



**A LOW COST DC VOLTMETER** converts inputs of 0 to 25.5 V into a plain-English output with a resolution of 0.1 V. Pressing the Test switch to take a reading sends a 4-ms negative pulse to the a-d converter from the NAND gate IC1c, configured as a half-monostable. An a-d converter generates an 8-bit binary-coded output word, the digital equivalent of the voltage input. These 8 bits serve as the address input to the pins of an EPROM. Half of a 4520 dual counter (IC2a) scans those memory locations in sequence by driving the lower address bits A<sub>0</sub> to A<sub>3</sub> of the EPROM. As a result, the EPROM delivers a preprogrammed sequence of five instructions to the Digitalker.

# CIRCLE 534 CMOS MSI CIRCUIT MEASURES C VALUES

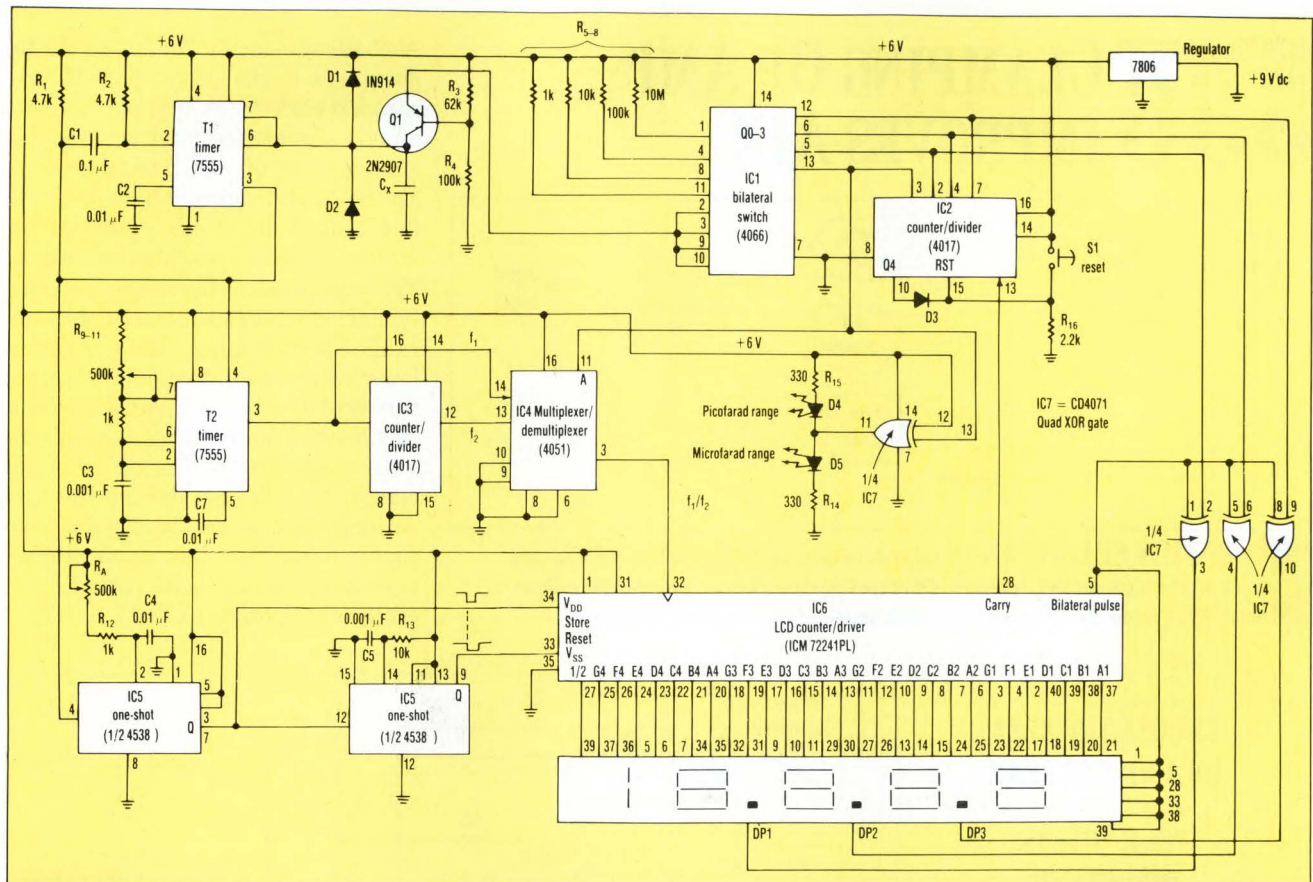
The problem with many digital capacitance-measuring circuits lies in their TTL or LS technology, which draws high current and mandates a high

part count. Also, liquid-crystal displays (LCDs) use far less current than LED displays. A CMOS MSI circuit with an LCD solves both prob-

lems. The circuit (see the figure, p. 85), a 4-1/2-digit autoranging capacitance meter, automatically selects the scale and the display's decimal-point position. The circuit's range is 1 pF to 100 μF. It consumes 50mA at 6 V and operates on a 9-V battery with a 7806 regulator IC. □

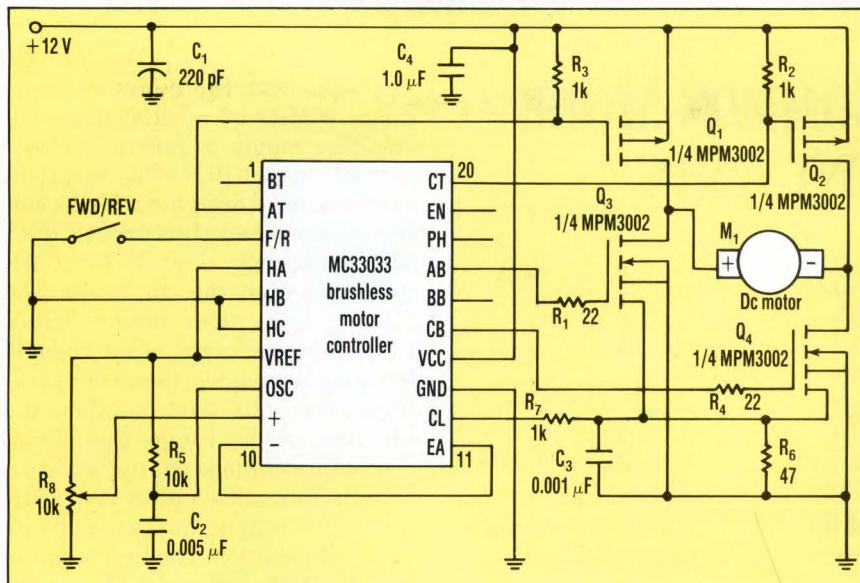
(Winner, Sept. 22, 1988, p. 148)





**A 4.5-DIGIT LCD** autoranging capacitance meter automatically selects the scale and the display's decimal-point position. The meter requires only the insertion of the unknown capacitor,  $C_x$ , to select a range from 1 pF to 1000  $\mu$ F. Timer T1, operating in a linear monostable mode, charges  $C_x$  through a constant-current source formed by transistor Q1 and resistors  $R_5$  to  $R_8$  in accordance with the scale. IC1, a CD4066 quad bilateral switch, automatically selects one of these resistors. The time between pulse outputs from T1 then depends on the value of  $C_x$ .

## CIRCLE 535 DRIVE BRUSH MOTORS WITH BRUSHLESS IC



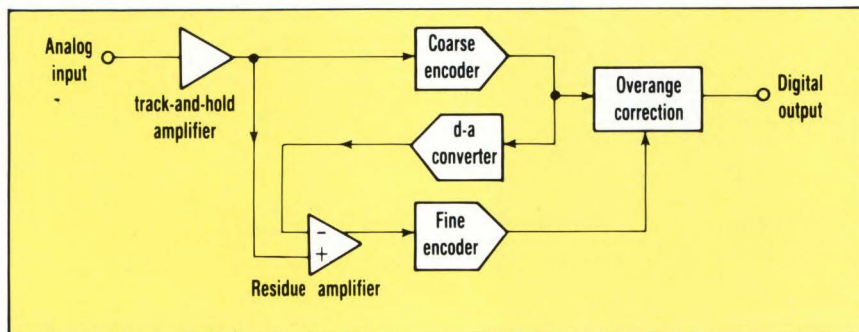
An effective way to drive brush-type dc motors is with inexpensive ICs intended to control brushless motors. An MC33033 brushless controller driving an MPM3003 H-bridge results in a minimum-parts-count drive for a 1/10th-hp motor. The key to the circuit is a Hall code (100) that produces a top-left, bottom-right drive when the controller's forward-reverse (F/R) pin is at logic-level one; a top-right, bottom-left drive when it's at logic level zero. □

(Winner, May 25, 1989, p. 67)

**NETWORK**  $R_5$  and  $C_2$  establishes a pulse-width-modulated frequency of about 25 kHz. Varying the noninverting input of the PWM loop's error amplifier from zero to  $V_{REF}$  with  $R_8$  sets the motor speed. With the FWD/REV switch open, Q1 is on, and the controller pulse-width modulates Q4 to drive the motor. Closing FWD/REV turns Q2 on, and Q3 modulates the current, reversing the motor.



# CIRCLE 536 CLAMPING OP AMP IMPROVES ADC



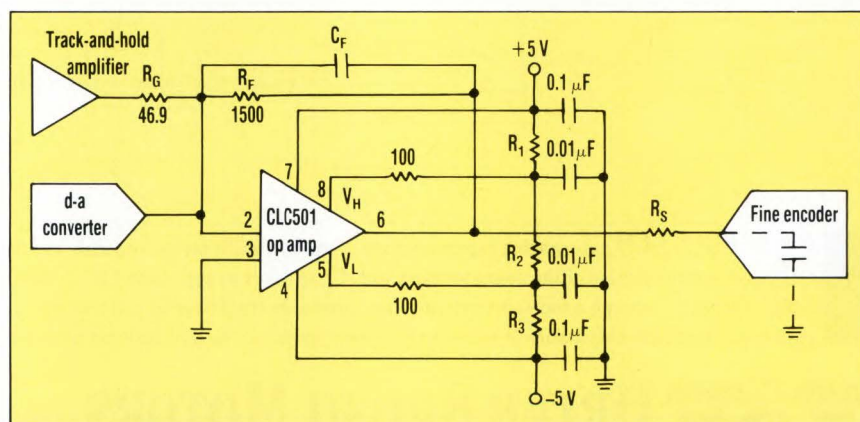
**1. IN THIS SUB-RANGING** a-d architecture, the difference between a present track-and-hold output and a previous a-d output can be enough to overload the residue amplifier. Frequently, the error term will be amplified in the conversion process.

A challenge facing analog-to-digital designers is the production of sub-ranging converters that will convert analog signals to 12-bit accuracy at sample rates of 10 MHz and beyond. To that end, track-and-hold and residue amplifiers of adequate performance remain sought-after items. The residue amplifier (*Fig. 1*), in particular, establishes much of the sub-ranger performance. The CLC501, a low-power, monolithic device, solves this problem by teaming a current-feedback op amp with an internal output-voltage clamp. The op amp and clamp (*Fig. 2*) help deliver the fast settling time at the high gains routinely needed in this application—necessary for high clock rates. □  
(Winner, October 13, 1988, p. 124)

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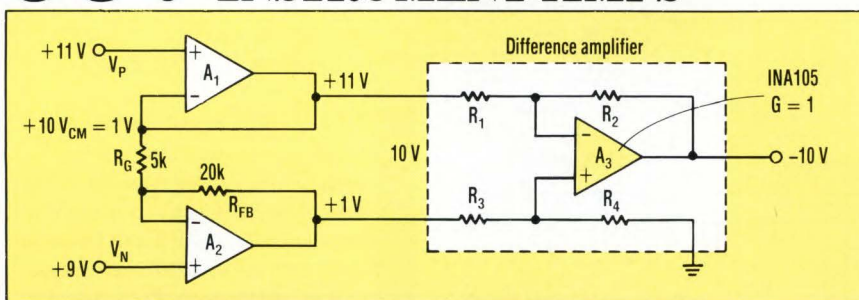
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**2. TO CONSTRUCT** a residue amplifier, use a feedback resistor  $R_F$  of about 1.5k. For a voltage gain of -32,  $R_G$  is 46.9k. A feedback capacitor,  $C_F$  (about 1 pF), must supply lead compensation to eliminate ringing. A damping resistor,  $R_S$ , improves settling time.

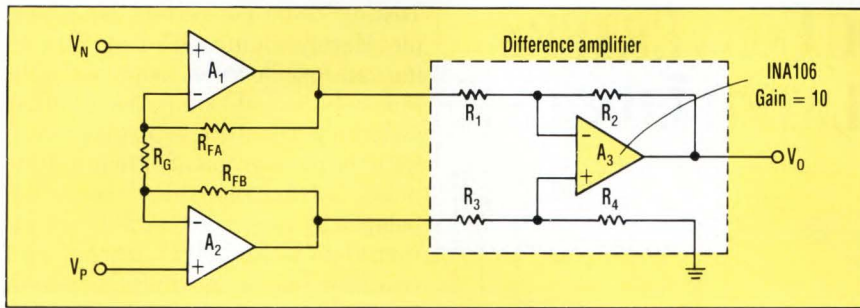
# CIRCLE 537 EXTEND COMMON-MODE INSTRUMENT AMPS



**1. THIS INSTRUMENT-AMPLIFIER CIRCUIT** supplies a  $\pm 10$ -V common-mode range with a  $\pm 10$ -V output. However, it requires a minimum gain of 10 in the differential-amplifier circuit.

The fact that the common-mode range (CMR) of most instrument-amplifier inputs is generally closer to  $\pm 6$  V than  $\pm 10$  V often surprises even seasoned designers. Moreover, the many manufacturers' data sheets showing  $\pm 10$  V for CMR specs heighten the confusion. The fact is, those units have a  $\pm 10$ -V CMR only near zero output voltage. Because most applications rely on at least a few volts of output, if not the full 10-V output range, this limitation compromises many designs. Two circuits can supply a 10-V CMR with a 10-V output, but each imposes a special condition. The first supplies  $\pm 10$ -V CMR with a  $\pm 10$ -V output,





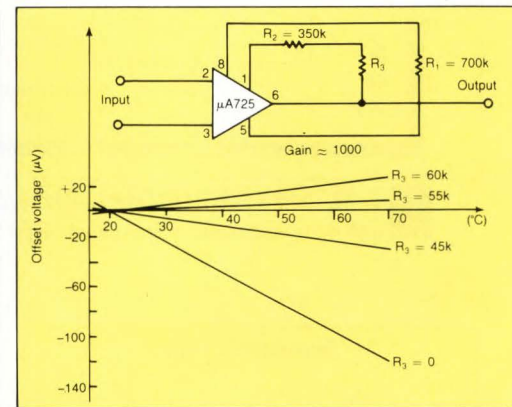
but it requires a minimum gain of 10 (Fig. 1). The second imposes no restriction on gain, but limits the CMR to 10 V output only (Fig. 2). □ (Winner, Dec. 22, 1988, p. 67)

**2. THERE'S NO** restriction on gain with this instrument-amplifier circuit. But it limits the output to -10 V and the CMR to 10 V as an output only.

## CIRCLE 538 COMPARATOR SUPPLIES FULL OP-AMP OUTPUT

Many circuits need the controlled characteristics of a closed-loop gain, highly stable amplifier. Among these circuits is the comparator in ac voltage and current regulators, as well as the comparator that closes the loop around the storage capacitor in a sample-and-hold circuit. Not only must the gain within the comparator's linear region be accurately controllable, but the input impedance must be high. Such an extend-

ed-use comparator—an attractive alternative to typical comparators—can be built with one  $\mu A725$  op amp and just three resistors. This comparator delivers a full-range op-amp output of  $\pm 10$  V. It allows the closed-loop voltage gain to be set between 500 and 100,000. This circuit also exhibits a low offset-voltage drift of  $0.1 \mu V/^{\circ}C$  and furnishes a high input impedance of  $1 M\Omega$ . □ (Winner, June 23, 1988, p. 120)



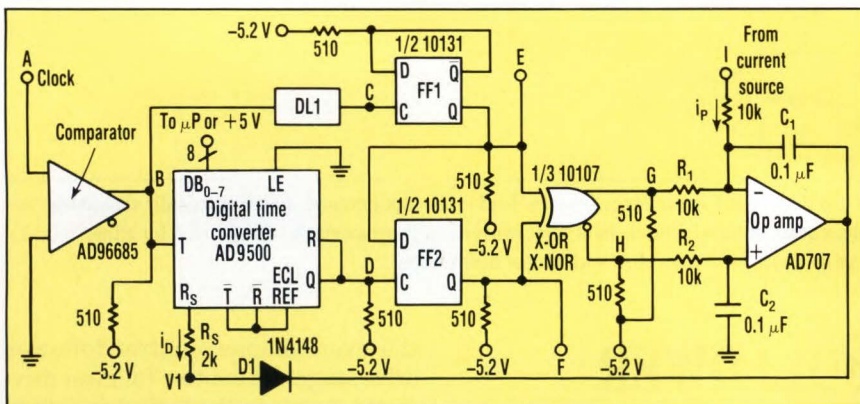
**BUILD AN** alternative to typical comparators with one  $\mu A725$  op amp and three resistors.

## CIRCLE 539 ELIMINATE OSCILLATOR FROM A LOOP

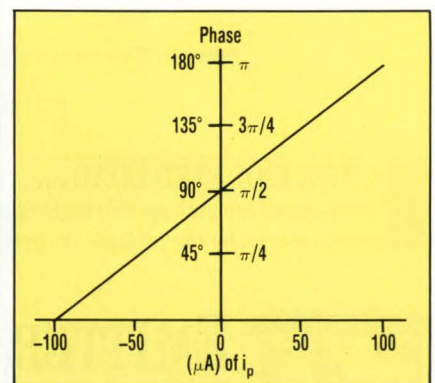
For a phase-locked loop covering inputs of 40 kHz to 40 MHz, a digital-to-time converter (DTC) can supply a current-controlled delay to replace

the oscillator. The circuit employs negative feedback to the DTC to close the circuit's loop, which is stable over all three frequency decades.

The DTC's digital inputs DBO-7 supply maximum (full-scale) delay when the inputs are all high (at +5V) and its  $R_S$  input is at ground voltage. However, a negative voltage at node V1 from the op-amp integrator's output and the resulting current  $i_D$  decrease the DTC's delay. □ (Winner, April 27, 1989, p. 107)



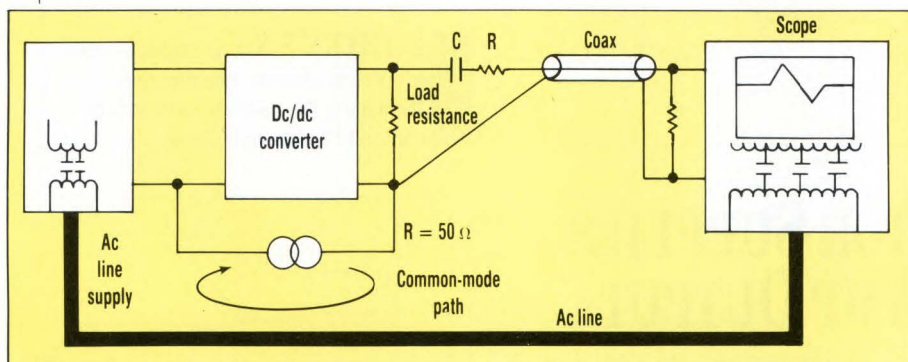
**1. A CIRCUIT EMPLOYING NEGATIVE FEEDBACK** to a digital-to-time converter can supply a current-controlled delay to replace the oscillator in a phase-locked loop. This circuit will handle input frequencies from 40 kHz to 40 MHz. The op-amp output ranges from -5 to -13 V at equilibrium. Diode D1 is used to block positive voltages to  $R_S$ .



**2. A CURRENT SOURCED** into the inverting input of the op-amp integrator's summing node can phase shift the pulses at F in relation to those at E by up to  $180^{\circ}$ .



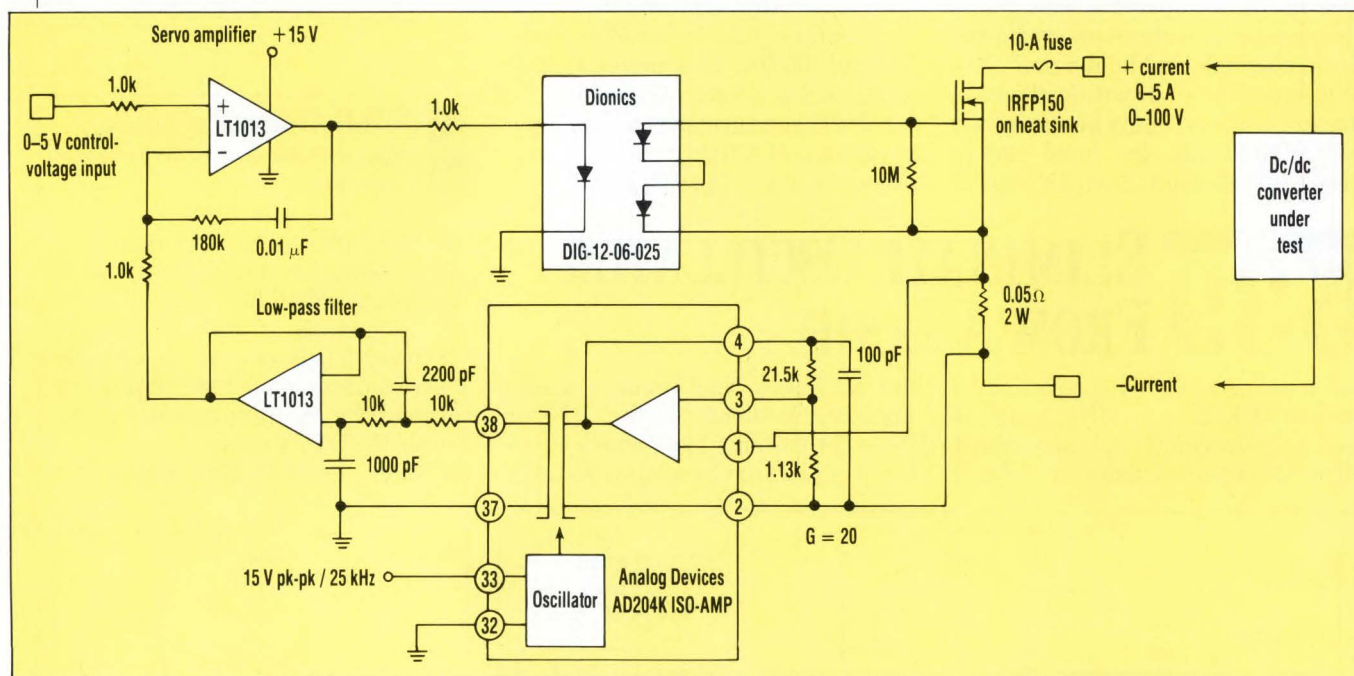
# CIRCLE 540 TEST DC/DC CONVERTERS WITH ISOLATED LOAD



**1. MASSIVE GROUND-LOOP** paths and fast switching waveforms can play havoc with the measurement of true output noise.

Testing dc-dc converters isn't simple. Merely adding a load and attaching an oscilloscope isn't enough. Massive ground-loop paths and fast switching waveforms can play havoc with the measurement of true output noise. A common-mode current, developed by the converter's 100-ns, internal-switching waveforms and transformer interwinding capacitance, usually finds a path through the measuring scope, the ac line, and back to the converter. An isolated load is thus needed for testing dc-dc converters. It has less than 100-pF capacitance from the load to the input ground. This low coupling capacitance reduces the possibility of common-mode ground loops. □

(Winner, Nov. 23, 1988, p. 123)



**2. THE ISOLATED LOAD** circuit has less than 100-pF capacitance from the load to the input ground, which practically eliminates common-mode ground loops that might cause inaccurate noise measurement of dc-dc converters. Programmable from 0 to 5 A for either positive or negative current loads, the circuit can dissipate more than 50 W with proper heat sinking.

# CIRCLE 541 EMITTER FOLLOWER DRIVES LEDs

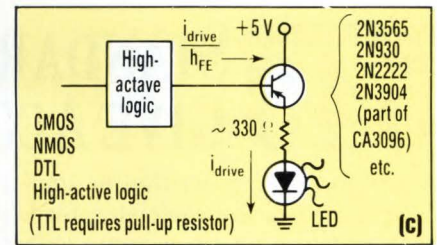
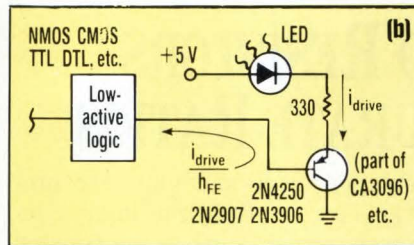
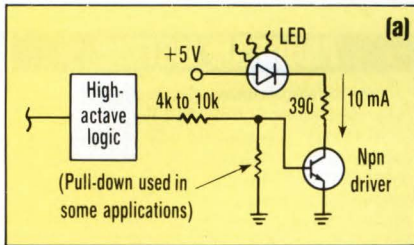
Designers typically use saturated common-emitter npn stages to drive light-emitting diodes from logic sys-

tems. Although that approach is widespread and workable, the npn common emitter isn't as efficient as

the even simpler emitter-follower drive stage. An emitter-follower driver can couple to the logic-drive stage without any resistors between logic and base of the emitter follower (see the figure, p. 101). This setup represents the minimum parts count. □

(Winner, December 8, 1988, p. 104)





**A TYPICAL COMMON-EMITTER** driver requires at minimum a base-drive current-limiting resistor plus a current-control resistor in series with the LED (a). The input to the emitter follower can be either from an active-low logic output (b), or from an active-high logic output (c).

## CIRCLE 542 SPREADSHEET SIMULATES LOGIC

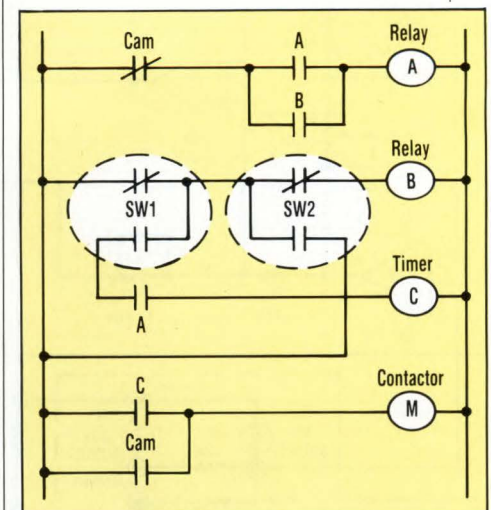
### LOGIC SPREADSHEET

	A	B	C	D	E	F	G
1	Switch-1		Relay-A	Relay-B	Timer-C		Contactor-M
2	0		1	1	0		0
3							
4	Switch-2						
5	0						
6							
7	Timer-C Contact						
8	0 <-- (Contact = 1 after Timer-C = 1) -----						
9	(Contact = 0 before Cam = 0)						
10	Cam						
11	0 <----- (Cam = after M = 1 and before Timer-C = 0) -----						
12	(Cam = 0 when cycle is complete)						
13							
14							
Cell	Cell name	Cell contents					
A1		Switch-1					
C1		Relay-A					
D1		Relay-B					
E1		Timer-C					
G1		Contactor-M					
A2	SW1	0					
C2	RLYA	@AND(CAM = 0, (@OR(RLYA = 1, RLYB = 1)))					
D2	RLYB	@AND(SW1 = 0, SW2 = 0)					
E2	TIMC	@AND(RLYA = 1, SW1 = 1, SW2 = 1)					
G2		@OR(CAM = 1, CONTC = 1)					
A4		Switch 2					
E4		:					
A5	SW2	0					
E5		:					
G5		:					
E6		:					
G6		:					
A7		Timer-C Contact					
E7		:					
G7		:					
A8	CONTC	0					
B8		<-- (Contact = 1 after Timer-C = 1) -----					
G8		:					
B9		(Contact = 0 before Cam = 0)					
G9		:					
A10		Cam					
G10		:					
A11	CAM	0					
B11		<----- (Cam = 1 after M = 1 and before Timer-C = 0) -----					
C12		(Cam = 0 when cycle is complete)					

Notes: \* Unprotected cells; all others protected.  
@ = Logic equation

Logic	1	0
Device	activated	not activated

Spreadsheet programs are common, easy to use, and can usually supply the logic functions AND, OR, and NOT. Consequently, it's easier to execute simple-logic simulation with spreadsheets than by experimenting with hardware. For example, in a relay-logic machine-control circuit for a punch-press, contactor-M energizes and the motor-M starts only when simultaneously pressing both palm switches, SW-1 and SW-2. The motor should then complete one cycle, and the cycle shouldn't start again unless both palm switches were first released. A spreadsheet supplies simulation with names and logic entered from the wiring diagram. The logic functions require only spreadsheet cells A2, C2, D2, E2, G2, A5, A8, and A11. The remaining cells are optional graphics. □  
(Winner, March 23, 1989, p. 79)



**A SPREADSHEET** supplies a quick and direct simulation with the device, names, and the logic circuit entered directly from the wiring diagram.



# CIRCLE 543 STANDARD RESISTORS GIVE ACCURATE RATIOS

A simple program written in standard Basic quickly calculates feedback resistors to get accurate gain values for inverting and noninverting op amps and resistors. It also gets accurate ratios for voltage dividers, when using standard resistor values. After the user enters the per-

centage values and gain, the program operates for a time interval inversely proportional to the resistor tolerance. The smaller the tolerance, the longer it takes. The resulting resistor values supply standard resistor values and tolerances. □  
(Winner, Sept. 8, 1988, p. 111)

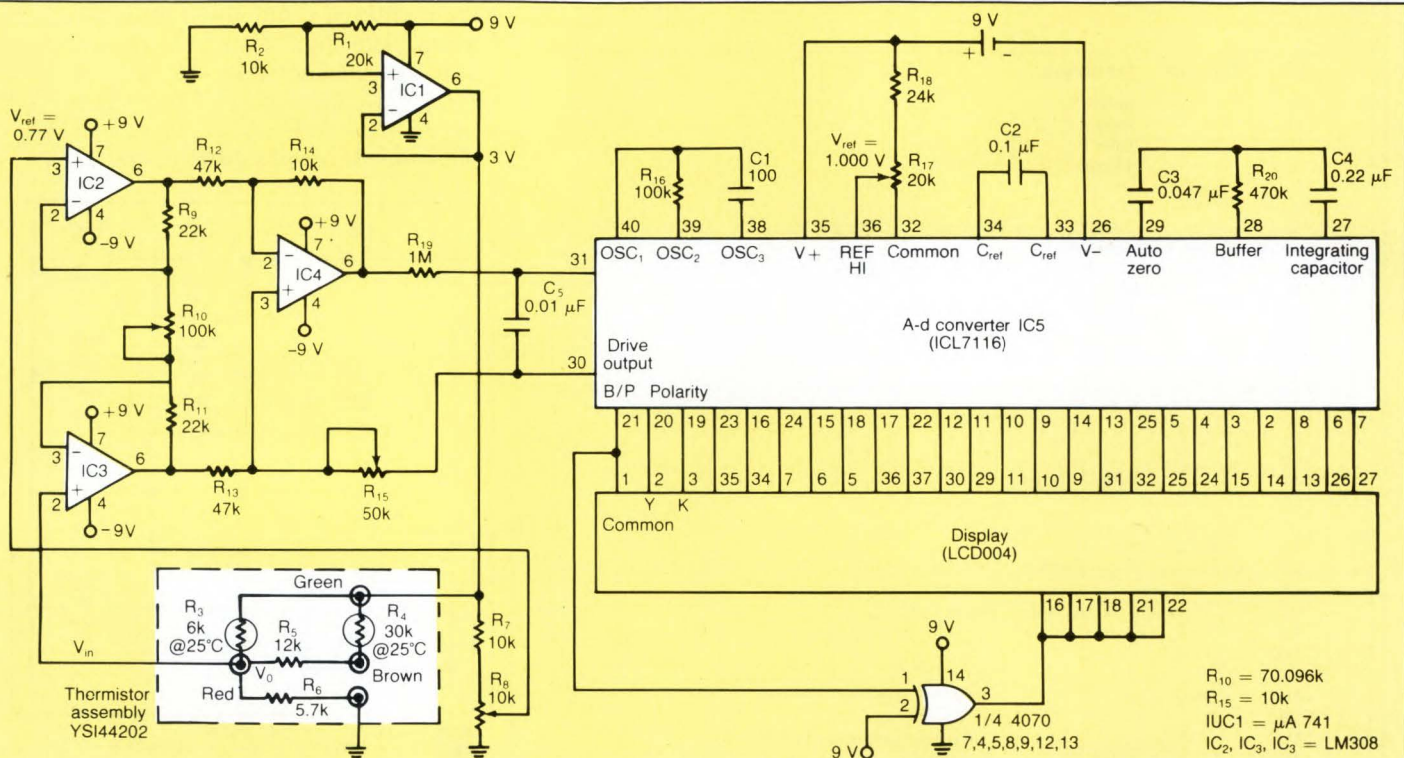
# CIRCLE 544 READ TEMPERATURE To 0.1°C RESOLUTION

Most mechanical and liquid-sensing thermometers can't supply the 0.1°C resolution called for in many biological applications. A digital thermometer, with a liquid-crystal display (LCD) operating from 5 to 45°C, readily delivers that high resolution. The circuit uses a thermoliner sensor element (YSI 44202) containing a

linearization network. Biasing the network is a low-voltage, 3-V regulated power source from a  $\mu$ A741 op amp, IC1. An instrumentation amplifier formed by LM308 op amps IC2, IC3, and IC4 is a high-gain configuration, basically an improved version of a differential amplifier. □  
(Winner, August 11, 1988, p. 128)

## PROGRAM LISTING

```
10 REM Accurate gain ratios - dividers/op-amps
20 F5=0:REM Swap R1 & R2 if F5=1
30 DEF FNA(X)=.01*INT(X*100+.5)
40 DEF FNB(X)=.1*INT(X*10+.5)
50 DEF FNC(X)=INT(X+.5)
60 REM Roundoff routines
70 INPUT "2, 1, or 0.5% ";B
80 INPUT "Gain ? ";G
90 IF G=-1 THEN R1=1:R2=1:GOTO 350
100 IF G=1 THEN R1=1:R2=0:GOTO 350
110 IF G<0 THEN A=-1/G:GOTO 150
120 IF G<1 THEN A=1/G-1:GOTO 150
130 IF G<2 THEN A=1/(G-1):GOTO 150
140 A=G-1:F5=1
150 B=96/B
160 REM B = No. of discrete resistor values, 48, 96 or 192
170 E=B
180 REM Initialize error E
190 IF A<1 THEN A=1/A:F5=1
200 L=FNC(B*LOG10(A))
210 FOR M=1 TO B
220 N=L+M-1
230 R8=10*(N/B)
240 REM R8 = trial value of R1
250 IF N<=B THEN R8=FNA(R8)
260 IF N>B AND N<=2*B THEN R8=FNB(R8)
270 IF N>2*B THEN R8=FNC(R8)
280 REM Insures just 3 significant figures
290 R9=FNA(10*((M-1)/B)):E1=ABS(R8/R9-A)
300 REM R9 = trial value of R2
310 IF E1<E THEN E=E1:R1=R8:R2=R9
320 REM Find smallest error E
330 NEXT M
340 IF F5=1 THEN S=R1:R1=R2:R2=S
350 PRINT G;R1;R2
360 END
```



**THE THERMOMETER CIRCUIT** uses a thermoliner sensor element with a high-gain differential amplifier. Two stages of feedback achieve precision high gain.



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3. CYM1832PZ-64K x 32 SRAM, 25ns. 60-pin ZIP. 1.0" Sq. req.



4. CYM1831PZ-64K x 32 SRAM w/OE, 25ns. 64-pin ZIP. 1.2" Sq. req.



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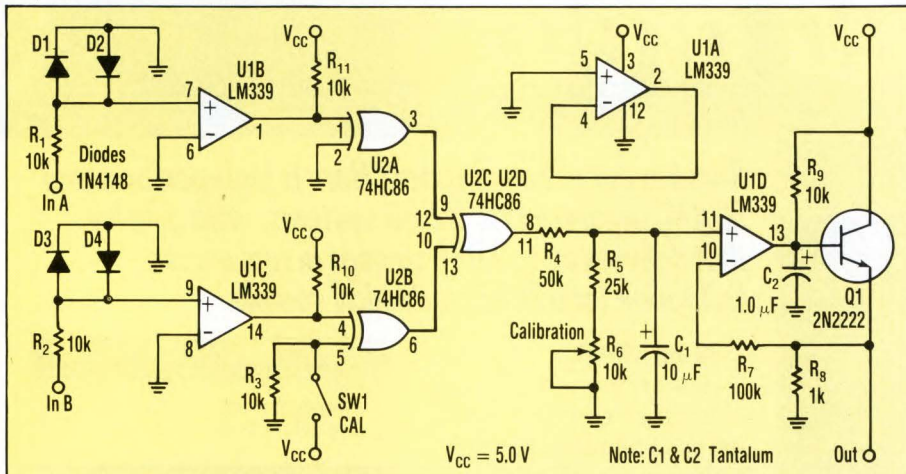


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# CIRCLE 545 PHASE METER USES JUST TWO CHIPS

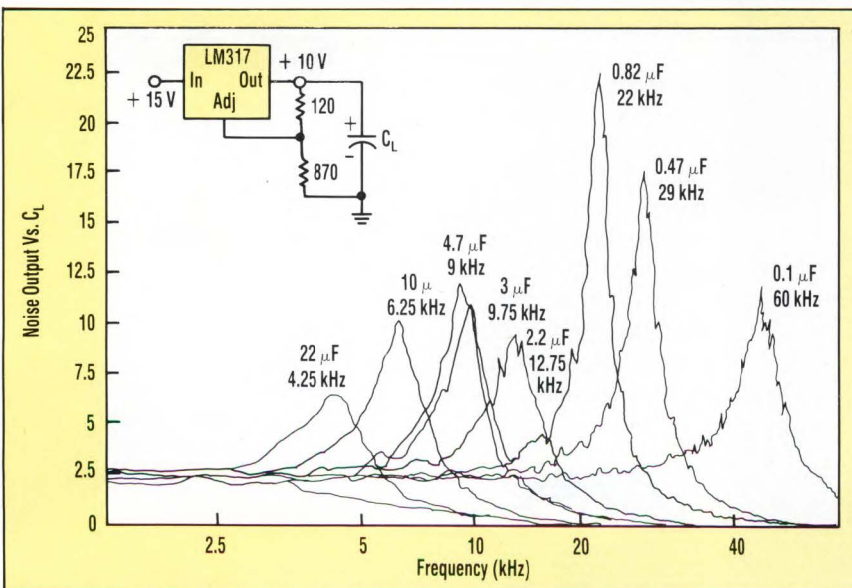


**THE PHASEMETER USES JUST TWO ICs:** a 74HC86 CMOS Exclusive-OR gate and an LM339 CMOS quad comparator. The outputs from U2C and U2D (exclusive-ORs connected in parallel) have a positive pulse width proportional to the time difference between the zero-crossing points of the two inputs—A and B. Accordingly, the average voltage across  $C_1$  is proportional to the absolute phase difference between the inputs.

A simple, but effective low-frequency phase-meter circuit, needing just two IC chips, achieves an absolute accuracy of better than 1°. The ICs are a readily available CMOS quad comparator. Sections U1B and U1C of the quad comparator, an LM339, form zero-crossing detectors for each input. Two sections of a 74HC86 Exclusive-OR—U2B—function as buffers (SW1 open) to drive two other parallel-connected Exclusive-ORs, U2C and U2D, which are in parallel to supply a reduced output impedance. At their output, resistors  $R_4$ ,  $R_5$ ,  $R_6$ , and capacitor  $C_1$  form a voltage divider and low-pass integrating filter that scales and filters the signal. With a digital voltmeter connected to the output, the scale can be calibrated to indicate the absolute phase difference between the circuit's two inputs with a scale factor of 0.01 V/degree with a 3-V rms sine wave, accuracy is better than 1°. □

(Winner, May 11, 1989, p. 115)

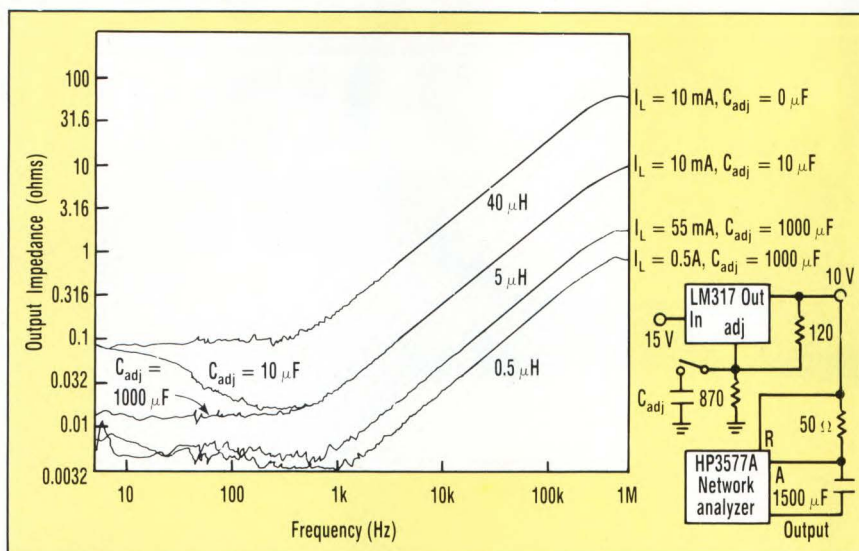
# CIRCLE 546 REDUCE NOISE IN VOLTAGE REGULATORS



**1. SHUNTING THE INDUCTIVE OUTPUT IMPEDANCE** of a three-terminal regulator to ground with a capacitor can produce a noise peak at the resonant frequency of this inductance and added capacitance. However, the output inductance also varies with load current (see Fig. 2).

Simply placing capacitors across the output and the adjust pins of three-terminal regulators is the usual approach to reducing regulator noise. However, the output impedance of the LM317 voltage regulator, for example, over a 1-kHz to 1-MHz range, is inductive. This is not because of lead inductance, but rather because its internal gain roll-off is 6 dB/octave—just as for an op amp. When users shunt this inductive output impedance to ground with a capacitor, the combination can produce a noise peak at the resonant frequency. For an LM317 with various capacitive loads, the frequency range of the noise spike doesn't extend much above 100 kHz nor below 10 kHz. This is because of ohmic losses in the inductance of the regulator and in the added output capacitance. A noise spike's magnitude depends on the Q of the resonant circuit, which the series resistance of the output capacitor mainly dominates. In most cases, several microvolts of power-supply noise peaking at 5 or 10 kHz won't cause problems. But if the circuit is sensitive to excess noise from





**2. THE OUTPUT IMPEDANCE** of three-terminal regulators versus frequency forms a family of curves, one for each current level, which changes the output inductance. The most effective noise reduction occurs with electrolytic capacitors of 50  $\mu\text{F}$  or greater connected across the output and at least 1  $\mu\text{F}$  connected from the adjust pin to ground.

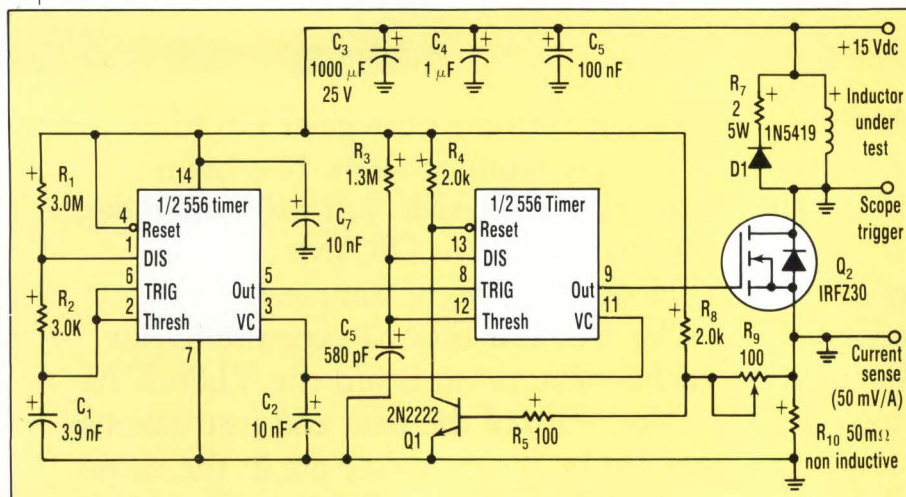
the supply at a particular frequency, users can easily engineer the regulator's circuit so that the noise peak

falls outside the critical frequency range. □  
(Winner, March 9, 1989, p. 84)

## CIRCLE 547 TEST POWER-INDUCTOR SATURATION CURRENT

A simple circuit can measure the saturation characteristics of a power inductor and compare its inductance value with that of a known unit. At saturation, the current in the inductor rises sharply from its otherwise linear slope. This sharp rise occurs

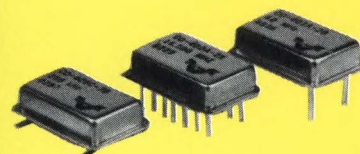
because the circuit keeps the voltage across the inductor fairly constant, while the coil's inductance drops radically at saturation. Consequently, the slope of the current waveform's linear part indicates inductance. □  
(Winner, April 13, 1989, p. 148)



**AN OSCILLOSCOPE MEASURES** a power inductor's saturation characteristics. This circuit can test inductors in the 200- $\mu\text{H}$  range at up to 15 A.



## ECL DIP to 400 MHz



	Std ECL	100K ECL
Frequency:	5-300 MHz	5-500 MHz
Accuracy:	$\pm 10$ , $\pm 15$ , $\pm 25$ or $\pm 50$ ppm	
Stability:	$\pm 25$ ppm over 0°C/70°C $\pm 5$ ppm over 0°C/50°C	

## Ga As to 600 MHz



Frequency:	300-600 MHz
Accuracy:	$\pm 10$ ppm ( $\pm 1$ ppm optional)
Stability:	$\pm 25$ ppm over 0°C/70°C $\pm 5$ ppm over 0°C/50°C



The Crystal Oscillator Company

VECTRON LABORATORIES, INC.  
166 Glover Avenue, Norwalk, CT 06850  
Phone: (203) 853-4433. FAX: (203) 849-1423

CIRCLE 55



# THE ONLY RISC PROCESSOR ON REGULAR AS IT



We have nothing against SRAMs. As a matter of fact, VLSI's SRAMs will run circles around anything most of our competition has to offer.

But if you're looking for a way to pump some speed into an embedded controller application and get the most mileage for your money, take a look at the new VL86C020.

It's the only 32-bit RISC processor with the ability to go 10 MIPS at

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Not premium SRAMs. Not high-octane video RAMs. Just plain, everyday, inexpensive 120 ns DRAMs.

How do we do it? Simple.

We used our SRAM expertise to put cache memory on board the VL86C020.

Now 93% of the data and instructions needed by the processor are in the cache.

And if you think all this performance turns the VL86C020 into a power



# OR THAT RUNS AS WELL DOES ON PREMIUM.



guzzler, you're wrong. Typically, it sips half a watt.

So you can forget about buffers and cooling systems.

The VL86C020 from VLSI will be better down the road, too.

Even when our new 30 MHz version hits the street it will still run on the same DRAMs. And it will still use the same memory interface.

For a free brochure on the VL86C020

and more information on our entire RISC family and development tools, call 1-800-872-6753, your local sales office or our authorized distributor, Schweber Electronics. Or write our Logic Products Group directly at 8375 S. River Parkway, Tempe, AZ 85284.

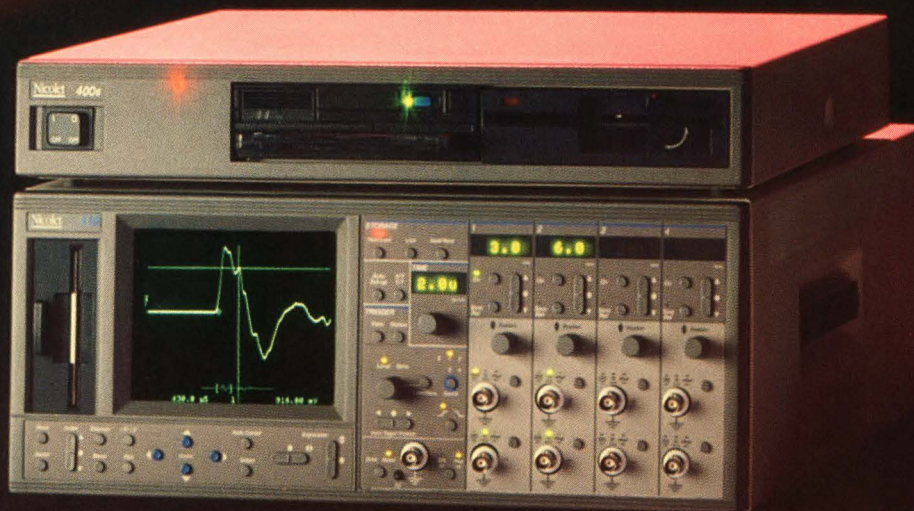
We'll show you how to get on the super-highway for embedded control. Without paying the toll.



VLSI TECHNOLOGY, INC.



# THE SHAPE OF THE FUTURE



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memory. Easy upgradability. Even  
removable hard drive.

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CIRCLE 36

**Nicolet**

INSTRUMENTS OF DISCOVERY



## OPTIMIZE ELECTRO-MECHANICAL DESIGNS

Tailored to meet specific manufacturing needs, I-DEAS for Electro-Mechanical Design, from Structural Dynamics Research Corp., Milford, Ohio, helps engineers optimize all phases of electro-mechanical products design. The application, which can directly transfer pc-board layout data to electronic design-automation software systems, such as Racal-Redac's Visula and Mentor Graphics' Board Station, includes interfaces that can generate solid models of pc-board assemblies directly from existing layouts. Once the design data is transferred, the fit between the circuit board assembly and other mechanical parts can be verified. The software also includes automatic interference checking, thermal and structural analysis, and plastic filling and cooling analysis. The software is available for a one-time license fee of \$49,500 or an annual fee of \$30,000. Modules for plastic filling and cooling analysis are an additional one-time license fee of \$30,000, or \$18,000 annually. Call Jere Brooks Hunter, (513) 576-2469. RE

CIRCLE 301

## 8-INPUT ANALOG SWITCHES ACCEPT 160 VOLTS

Two high-voltage switch ICs from Supertex, Sunnyvale, Calif., the HV21 and HV22, contain eight CMOS bilateral analog switches. Each has an on resistance of less than  $20\ \Omega$  and can switch up to 160 V. A standard three-line serial microprocessor interface drives an 8-bit input shift register, which in turn drives latches, level shifters, and the 160-V switches. Serial address words are shifted in with the clock and loaded with the latch-enable command. The HV22 has a Clear input to reset the latches. With a data-out line, it's possible to daisy-chain multiple ICs. Aimed at driving the piezoelectric transducers in medical ultrasonic scanners, the chips are also useful in printers, ATE systems, liquid-level sensors, and braille equipment. In 24-pin plastic DIPs, the HV21 and 22 cost \$24.26 and \$21.37 each, respectively, in quantities of 1000. Call Dilip Kapur, (408) 744-0100. FG

CIRCLE 302

## CLOCKS BOOST VXIBUS STABILITY

Engineers using VXIbus test systems can improve the accuracy and repeatability of their measurements with two high-stability reference oscillators from Racal-Dana. Configured as two-slot, C-size, register-based modules, the oscillators offer three outputs. Users can select 1, 5, or 10 MHz, or an optional 1 pulse/s for satellite and telemetry work. Model 1260-04E is an ovenized oscillator with an aging rate of less than  $5 \times 10^{-10}$  per day and temperature stability of less than  $7 \times 10^{-9}$  averaged over 0 to 50° C. Model 1260-04R is a rubidium oscillator featuring an aging rate of  $5 \times 10^{-11}$  per month after one month of operation. The 1260-04R's temperature stability is at least  $3 \times 10^{-10}$  averaged over 0 to 50° C. The 1260-04E costs \$2485 and the 1260-04R goes for \$10,950. Delivery is in eight weeks. Call Arlene Meadows, (714) 849-8999. JN

CIRCLE 303

## 12-BIT ISOLATION-AMP KEEPS 750 V AT BAY

Aimed at industrial process-control applications, the ISO212P from Burr-Brown, Tucson, Ariz., contains a low-cost, two-port isolation amplifier that's capable of 12-bit accuracy. A dc-dc converter in a 2.2-in.-by-0.3-in.-by-0.43-in. plastic SIP carries power from the output side of the isolation barrier to the input side. Both signal and power paths employ toroidal transformers rated to take a minimum of 750-V rms—continuously—between input and output. Every device is given a 1200-V rms partial discharge test for 1 second. The package's low height makes it possible for 0.5-in. board spacing without mechanical interference. An internal op amp can be set for gains between 1 and 100, and gain-linearity of the isolation amplifier for a  $\pm 5$ -V output is 0.025% of full-scale range. Multiple devices that are close to the same board can be synchronized. In quantities of 100, the ISO212P costs \$28 each. Call Barry Ehrman, (800) 548-6132. FG

CIRCLE 304

## 3.5-DIGIT PANEL METER RUNS FOR A YEAR NON-STOP

Equipped with a true single-ended input and primary power operation that spans from +3.5 to +7.5 V dc at only 145  $\mu$ A, the 3.5-digit DP-176S digital panel meter from Acculex, Taunton, Mass., allows up to 8000 hours (1 year) of continuous operation from any battery source in this range. The DP-176S includes a high-accuracy dual-slope integrating analog-to-digital converter, an integral dc-dc converter, 86-dB common-mode rejection, and an enhanced 12.3-mm LCD. It can be configured for analog inputs from  $\pm 200$  mV to  $\pm 200$  V dc. The meter's versatility is illustrated by its input-offset adjustment and protection to  $\pm 10$  V dc. An accuracy of  $\pm 0.1\%$  full scale, automatic polarity changeover, over and under range indication, and 100-M $\Omega$  input impedance are also featured. With a temperature coefficient of  $\pm 100$  ppm/°C, the quick-mounting DP-176S can run at maximum accuracy at various temperatures. The DP-176S's applications range from hand-held instrumentation to process-control tasks. Each DP-176S costs \$64. A \$3 bezel kit for mounting is also available. Contact Brian Smothers, (508) 880-3660. RE

CIRCLE 305



## **EXCITE AND CONDITION AC TORQUE SENSORS**

With a small module—the 3B20 from Analog Devices, Norwood, Mass.—you can excite an ac-operated torque sensor and bring its output to a high-level dc voltage or process-control current signal. Torque transducers (strain gages with transformer coupling for excitation and response) eliminate the need for slip rings or other unreliable connections in applications where physical contact between a sensor and its associated electronics is difficult or impossible. The 3.3-in.-by-0.7-in.-by-3.3-in. 3B20 excites the sensor with 2- to 20-V rms at frequencies between 1 and 10 kHz. Full-scale signals from the sensor to the 3B20 can be user or factory set between 1.5- and 150-mV rms. Signal bandwidth is 100 Hz. Outputs of  $\pm 10$  V, 4–20 mA, and 0–20 mV are all simultaneously available from the module. In quantities of 100, the 3B20 costs \$190 each. Call Steve Guinta, (617) 461-3055. FG

CIRCLE 306

## **LASER-DIODE PACKAGE OFFERS TWO CHANNELS**

A new path will be carved through the conventional one-channel laser-design field with the LT091MD, a laser-diode package that incorporates two independently drivable channels for significantly increased access speeds. The diode package, from Sharp Electronics, Mahwah, N.J., operates at a maximum optical power output of 10 mW per channel with a wavelength of 780 nm. Constructed from GaAlAs in double-heterojunction fashion, the LT091MD includes two parallel V-channeled substrate structures for durability and high reliability. It can be processed in parallel, increasing read and write speeds. Mesa-etching down to the p-GaAs substrate achieves precise spacing between the two independent channels. Each package costs \$975. Small quantities are available from stock. Call Joe Inada, (201) 529-9686. RE

CIRCLE 307

## **6.5-DIGIT DMM COMES IN VXIBUS MODULE**

A full-function digital multimeter (DMM) features 4.5- to 6.5-digit resolution and up to 1000 readings per second, all packed into a single-width C-size VXibus module. The 1362 DMM from Datron Instruments, a division of Wavetek Corp., San Diego, Calif., offers dual triggering, using either an internal system trigger or an external TTL level at the front-panel trigger connector. Voltage ranges go from 100 mV to 250 V, and resistance ranges extend from 100  $\Omega$  to 10 M $\Omega$ . The unit makes true rms measurements for ac voltages from 10 Hz to 1 MHz. A version that's compatible with the U.S. Air Force's Modular ATE (MATE) standards, model 1362MT, works with the control interface intermediate language (CIIL). The 1362 costs \$3695, and the MATE version costs \$3995. Delivery is in six to eight weeks. Call (619) 450-9971. JN

CIRCLE 308

## **GET CAE/CAD TOOLS FOR 100-V MIXED ARRAY**

Now there's a complete set of IC CAE design tools for the MPD8020 high-voltage mixed analog-digital array from Micrel, Santa Clara, Calif. Built on a bipolar-CMOS-DMOS process, the array enables designers to build complex circuits by mixing its wide range of active and passive devices. These devices include 200 gates of 5-V CMOS logic, small signal bipolar (analog) transistors, and 16 120-V, 200-mA vertical DMOSFETS. The CAE tools—called ASISD—are designed for use on PCs. They perform schematic capture with OrCAD/SDT III, analog (and digital) simulation with PSpice, and digital simulation with OrCAD/VST. Additional tools include Probe, which presents the results of the simulation and ICED for IC layout. Various model libraries range from the chips basic active and passive components to analog and digital macros for circuits ranging from op amps and comparators to shift registers, voltage doublers and a pulse-width-modulated DMOSFET H-bridge. Each macro is available as a kit part for breadboarding. Call Marvin Vander Kooi, (408) 245-2500. FG

CIRCLE 309

## **TEST SOFTWARE FOR SUPPLIES IS UPGRADED**

A PC-based software package for power-supply testing has gotten a face-lift. Powerflex 3.0, from NH Research, Irvine, Calif., automates testing of virtually any type of power supply. Traditional power-supply test software offered a fixed library of standard tests, from which users built programs. Powerflex 3.0 offers templates for test routines so the only user-written code is the test algorithm—everything else is automated. The software supports the company's Powertest 8100 automatic power-supply test systems, as well as its new Powertest 8100i, which bowed at October's Autotestcon '89. The 8100i is the first power-supply test system to incorporate the VXibus standard. Users of 8100 and 8100i systems will receive free upgrades, while others can purchase upgrades for \$995. Call Gary Pollard, (714) 474-3900. DM

CIRCLE 310

*EDITED BY CLIFFORD METH*



# MULTIPLE-PROCESSOR EISA PCs HIT 40 MIPS

DESIGNED FOR  
NETWORKING  
AND MULTIUSER  
APPLICATIONS,  
386/486-BASED  
PC SYSTEMS  
INCLUDE  
HARDWARE AND  
SOFTWARE  
SUPPORT.

JON CAMPBELL

**B**y adding a second microprocessor, a first for a PC-based system, Houston, Texas-based Compaq Computer has taken the wraps off 386/486-based multitasking PCs that use the 32-bit Extended Industry Standard Architecture (EISA) expansion bus. The PCs include the tower Systempro version and a desktop Deskpro version. In addition, a host of supporting hardware and software products from other firms have also become available.

Competing with high-end mini-computer systems, such as the Digital VAX line, and low-end mainframe systems, such as the IBM 3090 computer line, the Systempro PCs are designed for networking and multiuser applications (*Fig. 1*).

With two microprocessors—either two 386s, two 486s, or one of each—the Systempro PCs can process up to 40 million instructions per second (MIPS). They offer better expansion capability and greater storage capacity than previous Compaq PCs, with 32-bit memory expansion of up to 256 Mbytes for a maximum storage capacity of 4.28 Gbytes. There's room for 11 internal mass-storage devices and a total of 11 expansion slots.

Including a second 386/33 microprocessor will double the comput-

ing power from 8 to 16 MIPS. Two 33-MHz 486 microprocessors deliver up to 40 MIPS of computing power. As a result, this multiple processor system offers a performance growth path from 8 MIPS to up to 40 MIPS of computing power as user applications increase in complexity.

Initial models of the Systempro PCs incorporate a 386/33 processor board containing a 33-MHz Intel 386 microprocessor, a 82385 33-MHz cache memory controller, 64 kbytes of 25-ns cache memory, 4 Mbytes of 32-bit system memory (expandable to 256 Mbytes), and sockets for both a 33-MHz Weitek 3167 and a 33-MHz Intel 387 numeric coprocessor. Because the cache-memory controller uses 25-ns RAM, the system can operate at its full 33-MHz clock speed on almost all memory cycles, delivering zero wait-states more than 98% of the time.



## 1. THE FIRST MULTITASKING 32-BIT

EISA PC includes Compaq's Systempro. The 386/486-based PC is designed for networking and multiuser applications. It can handle multiple processors—two 386s, two 486s, or one of each—for up to 40 MIPS of computing power.



# MULTITASKING 386/486 EISA PCS

The Systempro will also support a 33-MHz 486 processor as it becomes available. Users can upgrade to the next generation processor by adding a 486 processor without discarding the original 386 processor.

Compaq claims that these machines are five times as powerful as any of its previous computers. According to Compaq, the Systempro was six times faster than a comparable VAX in a standard benchmark test, even though it costs \$135,000 less.

The multiple-system processors are supported by leading network and multiuser operating systems, including Novell NetWare 386, Santa Cruz Operation UNIX System V/386, and the newly announced Compaq LAN Manager 386/486, which makes it possible for users to run the thousands of standard networking and multiuser applications without modification. A shared-system memory design allocates memory between both processors, reducing the need for additional memory as users scale up processor performance.

## 8-, 16-BIT SUPPORT

The PCs support all of the 8- and 16-bit Industry Standard Architecture boards. With new 32-bit EISA expansion boards, the EISA design enables users to take advantage of multiple 32-bit boards to maximize system throughput in connected-user environments. For example, users can add up to six 32-bit network-interface controllers to obtain the highest possible network server throughput. Because of the standard compatibility inherent in the EISA expansion bus, users can choose from a large selection of high-performance expansion options and peripherals.

New 32-bit network-interface controllers capitalize on EISA bus mastering and higher burst-rate data-transfer rates to contribute to total system performance, giving users

efficient access to shared information. For example, the EISA-based Novell 3200 Ethernet Controller offers greater network throughput than the comparable Micro Channel Architecture-based Novell NE/2-32 by demanding network server environments and reducing system processor utilization. Other high-performance EISA-based interface controllers are also available from Proteon, Standard Microsystems, Codenoll Technology, and Compu-tone.

To respond faster to the data re-

croprocessor, a 33-MHz cache memory controller, 64 kbytes of cache memory with a 25-ns access time, and 4 Mbytes of 32-bit system memory. A 240-, 420-, or 840-Mbyte fixed-disk array is included with Models 386-240, 386-420, and 386-840, respectively.

## A POWERFUL DESKTOP

The desktop version, the Deskpro 486/25, is claimed by Compaq Computer to be the most powerful desktop PC available. Based on the new Intel 32-bit 486 microprocessor and EISA, it delivers 15 MIPS of computing power and up to three times the performance of 25-MHz 386-based systems (Fig. 2).

The 486 processor design integrates three 32-bit processing components into one chip: the processor itself, a 387-compatible numeric coprocessor to speed numeric calculations, and a built-in high-speed cache memory controller with 8 kbytes of high-speed static RAM for the fastest possible microprocessor-to-memory interaction.

To maximize performance, Compaq designed a new, second-level cache controller with 128 kbytes of high-speed cache memory that ensures zero wait-states 98% of the time. The Deskpro 486/25 also fea-

tures an interleaved memory architecture that uses enhanced page memory.

The Deskpro 486/25 runs thousands of MS-DOS, OS/2, and UNIX applications designed for standard PCs and it utilizes the thousands of available Industry Standard Architecture (ISA) plug-in cards, boards, and peripherals, as well as the new 32-bit EISA products.

## A NETWORK MANAGER

A local-area network manager, developed jointly by Compaq and Microsoft Corp., Redmond, Wash., is claimed by both to be the highest-performance local-network operat-



**2. THE MOST POWERFUL DESKTOP PC** is Compaq's 25-MHz 486/25. Based on the 486 microprocessor and the EISA bus, it offers up to three times the performance of 386-based 25-MHz desktop PCs.

quests of multiple users, the Systempro incorporates an innovative 32-bit fixed-disk-drive array technology. A series of synchronized fixed-disk drives are configured as a drive array that's addressed as one higher-performance unit. A 32-bit intelligent-drive array controller takes full advantage of the EISA bus-mastering capabilities and the 32-bit data path to supply effective data-transfer rates up to four times faster than non-arrayed fixed-disk-drive subsystems.

Three versions of the Compaq Systempro PCs are available. Each version includes the 386/33 system processor board with a 33-MHz Intel mi-



## MULTITASKING 386/486 EISA PCS

### PRICE AND AVAILABILITY

Systempro models 386-240, 386-420, and 386-840, are priced at \$16,000, \$20,000, and \$26,000. Shipments start this month. Deskpro 486/25 models 120, 320, and 650 cost \$14,000, \$17,500, and \$20,500. Shipments are scheduled for next month. The LAN Manager 386/486, LAN Manager 386/486 advanced system, and the multiple-system processor option, are priced at \$2500, \$7000, and \$2500. Shipments will begin early 1990.

Banyan's Vines/486 upgrade option will be available in early 1990, price will be announced later. EmLIB, EmSAVE, and EmQ software from Emerald Systems costs \$395, \$395 to \$695, and \$1195 to \$1495, respectively, and are available now. Codenoll's CodeNet 8300 card costs \$995 and is available now. The CodeNet 9500 cards range from \$2795 to \$9995 and will be available in the first quarter of 1990. The ALC controller and the Async and Ethernet Feature Models from Computone cost \$1595, \$1195, and \$695, respectively, and are available now. The Async/Sync and Fax/Scanner Models are also available, prices will be announced.

The Novell NE3200 costs \$1295 and is available now. Proteon's p1990 ProNET-4/16 card costs \$995 and will be available late in the first quarter of 1990. SCO Unix System V/386 from The Santa Cruz Operation is currently available. Its 2-user and unlimited-user versions go for \$595 and \$995. Open Desktop will be available in January, 1990, for \$995. The SCO Extension to V/386 Release 3.2 is priced at \$895 and will be obtainable in early 1990. The Arcnet-EISA 3200 from Standard Microsystems costs \$995 and will be available in January, 1990. Torus' EISA Ethernet adapter is available now.

Compaq Computer Corp., P.O. Box 692000, Houston, TX 77269-2000; (713) 370-0670.

CIRCLE 511

ing system for OS/2-based networks.

The LAN Manager 386/486 is optimized to benefit from performance features specific to the new Compaq Systempro, such as multiple processors, innovative drive-array technology, and 32-bit network-interface controllers. It includes a 32-bit version of OS/2's High Performance File System (HPFS/386), which offers enhanced performance for accessing data on hard disks. An EISA device driver improves performance for such I/O devices as disk and network interface controllers. A multiple-processor support option distributes LAN Manager processing across two processors in the Systempro, which increases network capacity while maintaining high performance levels.

The LAN Manager 386/486 utilizes the strengths of OS/2 as a standard environment, which include multitasking, protected-mode application program security, and named-pipes interprocess communications. This standard software environment facilitates the development of new client-server applications for both OS/2 and MS-DOS PCs connected to the network.

The LAN Manager 386/486 is available in two versions: a standard system for up to 10 users and an advanced system for an unlimited number of users. The multiple-processor support option is available only for the advanced system.

### MANY SUPPORTING PRODUCTS

A number of third party software and hardware products are also available to support the Systempro and/or the Deskpro 486/25 PCs. Banyan Systems Inc., Westborough, Mass., for example, is offering full support for its Vines network operating system through new Vines/386 software options, and standard features in the recently announced Vines 4.0 release. And Emerald Systems Corp., San Diego, Calif., is making available Ramp data-management software for the new Compaq products.

Codenoll Technology Corp., Yonkers, N.Y., is offering the first 10-

and 100-Mbit/s fiber-optic local-area network boards for computers using the EISA bus. And Computone, Roswell, Ga. has begun shipping Computone ALC, the industry's first EISA bus communications subsystem. ALC consists of an intelligent communications controller board and four Feature Modules, that bring asynchronous, synchronous, Ethernet, facsimile, and scanner capabilities, to EISA-based workgroup systems.

The first EISA plug-in data-acquisition board and two associated software products for developing industrial and laboratory test, measurement, and control application programs is now available from National Instruments (*see related story, p. 103*). From Novell, South Provo, Utah, comes the first 32-bit-bus master Ethernet adapter built to the EISA specification. The adapter was jointly developed with Compaq.

There are other supporting products for the Systempro PCs. Proteon, Westborough, Mass., is offering the first token-ring network interface card for the EISA PC platform. The Santa Cruz Operation Inc., Santa Cruz, Calif., announced that its SCO UNIX System V/386 and SCO Open Desktop software fully support the 25-MHz 486 processor used in the Compaq Deskpro 486/25. A new SCO UNIX multiprocessing extension to SCO UNIX System V/386 will support the Compaq Systempro.

In addition, Standard Microsystems Corp., Hauppauge, N.Y., is offering the Arcnet-EISA3200, an intelligent 32-bit interface card for the Arcnet local-area network. The interface card can be used in EISA-based Compaq computers. Furthermore, Torus Network Products, Cambridge, England, has an EISA 32-bit Ethernet network adapter. The adapter card said to be Europe's first such card. □

### HOW VALUABLE?

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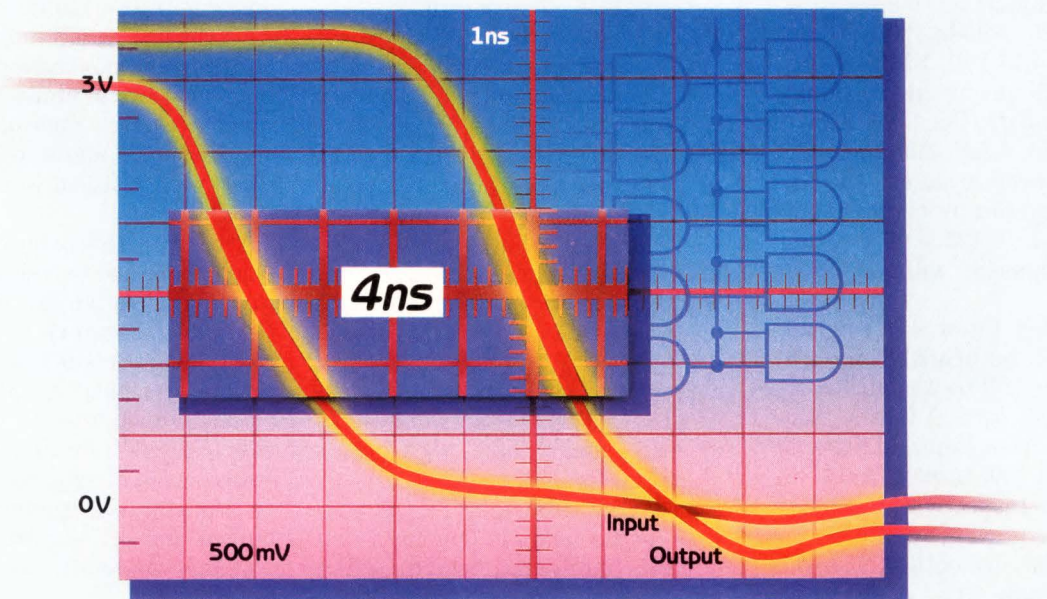
### CIRCLE

562  
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# FCT-T Logic

## Fast and Friendly



## CMOS Power at TTL Levels

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\*Please specify size for T-shirt.

CIRCLE 45



# FIRST EISA-BASED DATA-ACQUISITION BOARD. A-D BOARD USES EISA BUS To PUMP OUT 1 MSAMPLE/S

JOHN NOVELLINO

**A**lthough the IBM PC/AT bus is widely used in data-acquisition applications, it has some basic speed limits that have hindered its use by engineers who must sample data at very fast rates. Approximately 400 ksamples/s is the practical top speed for sending data to the computer's memory over a PC/AT bus, also known as the Industry Standard Architecture (ISA). With the introduction of the first Extended Industry Standard Architecture (EISA) products, that limit no longer applies.

The EISA-A2000 from National Instruments digitizes analog signals at up to 1 Msample/s with 12-bit resolution, sending the data directly to the computer's memory rather than buffering it for later transfer. The unit is the first plug-in data acquisition board for EISA computers (*Fig. 1*). Along with the board, National introduced two software control packages, including one that gives the EISA-A2000 the look and feel of a digital oscilloscope.

National's first EISA products debuted in a joint announcement with Compaq Computer Corp.,

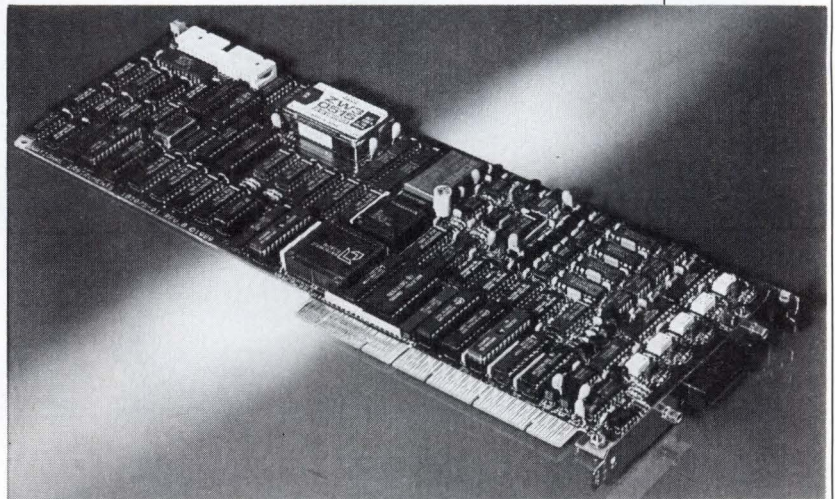
which introduced the first EISA-based computer (*see related story, p. 99*).

The EISA bus grew out of dissatisfaction with the IBM Micro Channel Architecture, which is found in the IBM PS/2 models 50 through 80. Though the 32-bit Micro Channel bus is fast, it's incompatible with the PC/AT bus and its huge installed base. Also, the Micro Channel bus doesn't allow DMA transfers that use the system controller.

Although the ISA bus does make it possible for DMA data transfers to the computer, it limits them to 1.6 Mbytes/s. Because high-end applications that

need good resolution require two bytes for every sample, the top transfer rate drops to 800 ksamples/s. However, a more practical limit that doesn't completely tie up the computer for data collection is around 400 ksamples/s.

To get higher analog-to-digital conversion rates on ISA, the data-acquisition board must have a large buffer memory. The data is held there and eventually sent to the system memory at a slower bus transfer rate. This scheme boosts hardware costs and limits the amount of data that can be collected in one continuous acquisition. In addition, the data isn't im-



**1. THE FIRST PLUG-IN DATA-ACQUISITION board** for the EISA bus is the National Instruments EISA-A2000. It has a 1-Msample/s sampling rate at 12-bit resolution.



# EISA-BASED DATA-ACQUISITION BOARD

mediately available for processing.

Teamed with the EISA bus, the EISA-A2000 eliminates these problems. The board transfers data directly to the computer using a burst-mode (type C) DMA transfer. Because a DMA controller handles the transaction, the computer's microprocessor is unoccupied. As a result, the acquired data can be processed immediately.

Each of the EISA-A2000's four single-ended input channels has its own sample-and-hold circuitry, so users can acquire multiple signals simultaneously. The board can sample two channels at 500 ksamples/s each and four channels at 250 ksamples/s. The input circuitry's small-signal bandwidth is 1.8 MHz, and the full-power bandwidth is 1.5 MHz.

With a voltage input range of  $\pm 5$  V, the unit's 12-bit resolution offers a voltage resolution of 2.44 mV. Effective resolution can be extended to 16-bit, two's-complement numbers by using the on-board 0.5-least-significant-bit Gaussian dither generator to average the acquired samples.

Users can select from analog, digital, or software triggering to start data acquisition. In the analog trigger mode, acquisition begins when the level and slope of an external signal—one of the four channels or a

## PRICE AND AVAILABILITY

The EISA-A2000 costs \$2995, and the VisionScope and DOS LabDriver software packages are \$295 each. The optional coax adapter with seven BNC connectors costs \$175. Delivery is within 30 days.

*National Instruments, 12109 Technology Blvd., Austin, TX 78727-6204; (512) 794-0100.*

**CIRCLE 512**

separate trigger input—meets programmed values. A digital-to-analog converter with a resolution of 10 mV generates the programmed voltage level. To use digital triggering, users direct the board to acquire data starting at the rising or falling edge of an external digital trigger input. With software triggering, the software specifies when the acquisition begins.

With pre- and post-triggering, the board can start collecting data before or after a trigger event. In the pretrigger mode, the software starts the acquisition and the board fills a buffer circularly until receiving a trigger. The EISA-A2000 then acquires a specified number of post-trigger samples. The board also has a delay mode in which the software

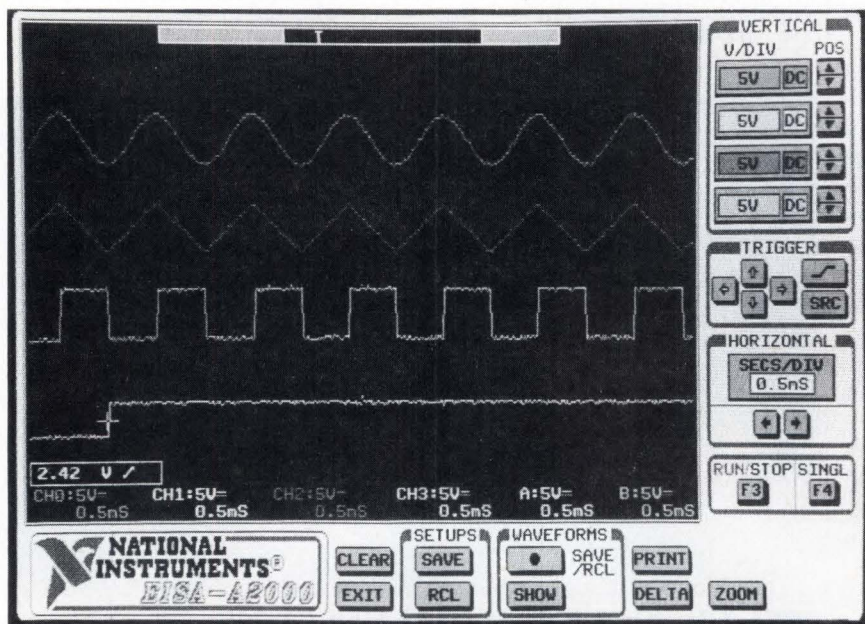
inhibits acquisition until a specified time after the trigger.

National EISA-A2000 documentation includes complete register descriptions and examples that make it possible for users to program the board directly. National also offers DOS LabDriver 3.0, a library of high-level software functions for programming the EISA-A2000 and the company's ISA plug-in data-acquisition boards. Users merely call the functions from Microsoft C or Quick-Basic to program the fast analog input, triggering, ac/dc coupling configuration, and calibration. Moreover, because software controls all of the configuration and calibration functions, the board has no jumpers, switches, or trimming potentiometers to set.

The EISA-A2000's triggering capabilities and programmable ac/dc coupling make oscilloscope emulation a natural application. Therefore, it's no coincidence that National's first DOS-based virtual instrument package is VisionScope, which supplies the board with an interface that mimics a traditional oscilloscope's front panel and controls (*Fig. 2*). The software employs technology that National acquired earlier this year from Virtual Instruments Corp., Georgetown, Conn.

The package doesn't need programming, and the intuitive interface features on-screen "point-and-click" controls. Users can store frequently needed setups for recall. The software can capture and display repetitive and one-shot waveforms, zoom in on the waveform buffer, and use delta cursors to measure voltage, time, and frequency.

The screen can display up to six traces chosen from the four hardware channels and four auxiliary displays. An on-line help function is also included. When equipped with the optional coax adapters with BNC inputs, the board can be directly connected to oscilloscope probes. □



**2. THE VISIONSCOPE SOFTWARE PACKAGE** creates a software front panel and controls that give the EISA-A2000 the look and feel of a traditional oscilloscope.

## HOW VALUABLE?

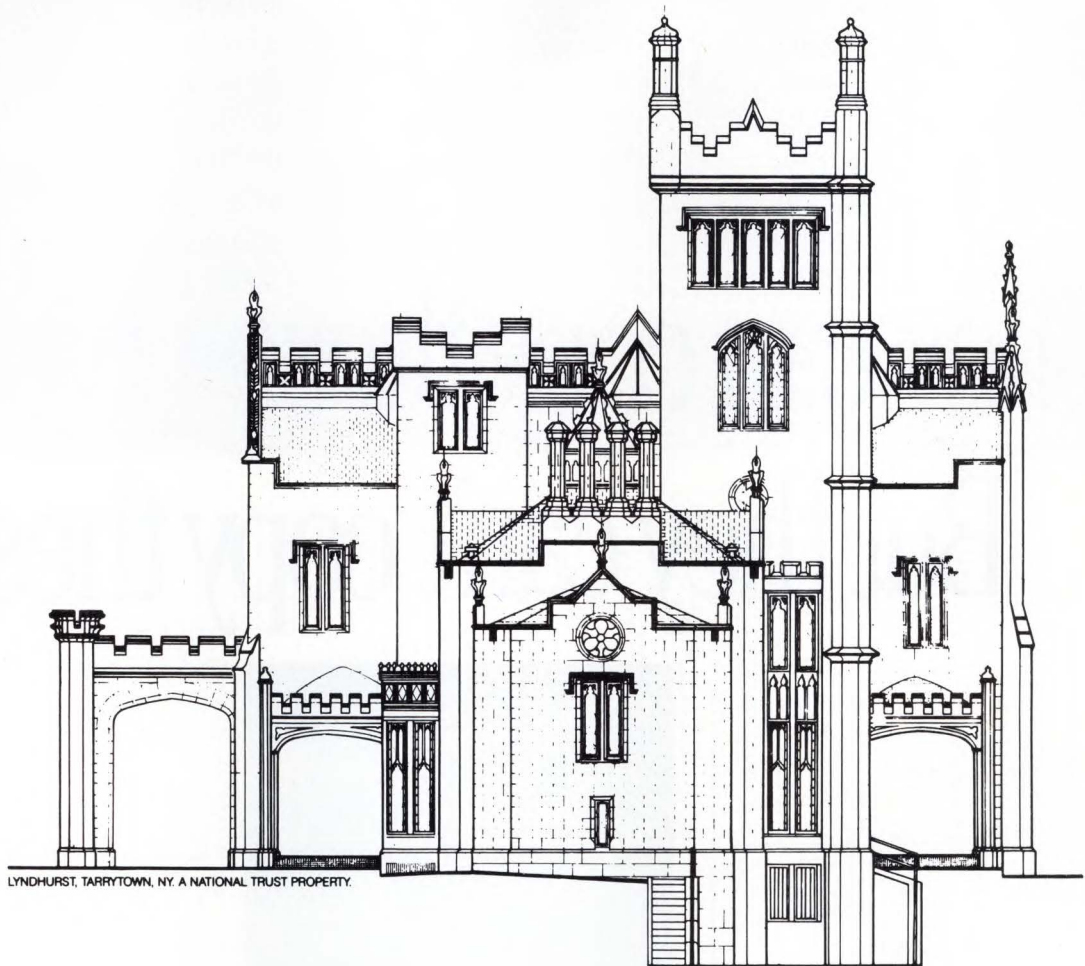
HIGHLY  
MODERATELY  
SLIGHTLY

## CIRCLE

565  
566  
567



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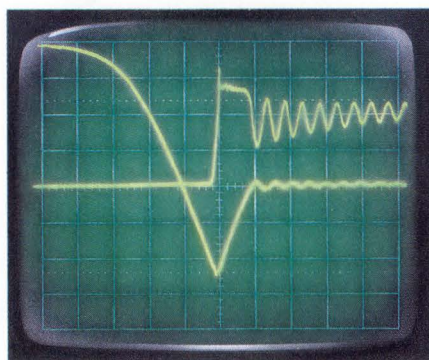
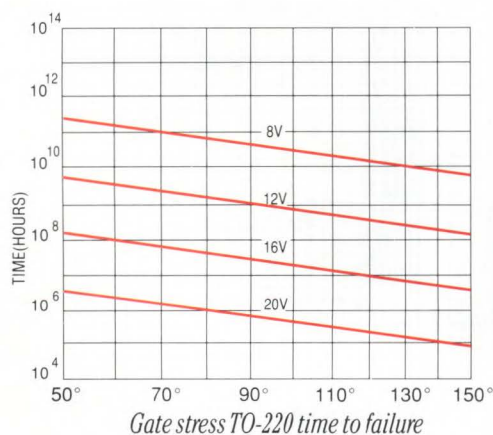
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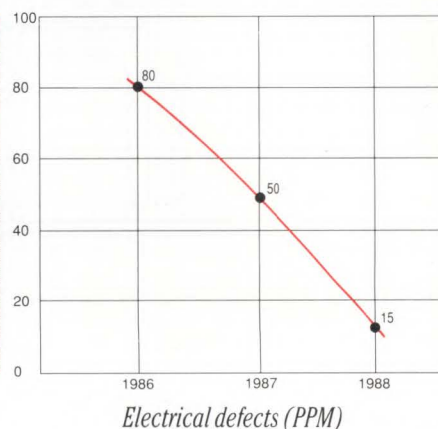
IRF724	IRFBG30	IRLS40	IRFP360	IRF9140
IRF744	<u>HEXSense®</u>	<u>FULLPAK</u>	IRFP440	IRFAC50
IRF520	IRCZ24	IRFIZ24	IRFP448	IRFAE50
IRF530	IRCZ34	IRFI530	IRFP450	IRFAF40
IRF540	IRC530	<u>SOT-89</u>	IRFP460	IRFAF50
IRF630	IRC540	IRFS1Z0	IRFP9140	IRFAG50
IRF640	IRC640	<u>D-PAK</u>	IRFP9240	<u>TO-39</u>
IRF624	IRC634	IRFR014	IRFPC40	IRFF024
IRF644	IRC730	IRFR024	IRFPC50	IRFF110
IRF720	IRC830	IRFR120	IRFPE40	IRFF120
IRF730	IRC840	IRFR220	IRFPE50	IRFF130
IRF820	<u>HEXDIP™</u>	IRFR310	IRFPF40	IRFF420
IRF830	IRFD1Z0	IRFR320	IRFPG50	IRFF9010
IRF840	IRFD014	IRFR420	<u>TO-3</u>	IRFF9110
IRF9224	IRFD024	IRFR9014	IRF140	<u>TO-240AA</u>
IRF934	IRFD110	IRFR9024	IRF150	IRFK2H250
IRF910	IRFD120	IRFR9120	IRF240	IRFK2H450
IRF930	IRFD220	<u>TO-18</u>	IRF250	IRFK4H250
IRF940	IRFD901	IRFP044	IRF244	IRFK4H450
IRF9620	IRFD9024	IRFP054	IRF254	IRFK6H150
				IRFK6H450

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# But they can't copy these.



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As IR HEXFETs® hold their lead in power MOSFETs, our competitors become bolder and bolder in attempting to duplicate our success.

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# CONNECTOR MAINTAINS SIGNAL INTEGRITY

A CONTINUOUS-GROUND-  
PLANE DESIGN,  
MATCHED IMPEDANCES,  
AND HIGH SIGNAL  
DENSITY TAKE A  
CONNECTOR INTO THE  
GIGAHERTZ RANGE.

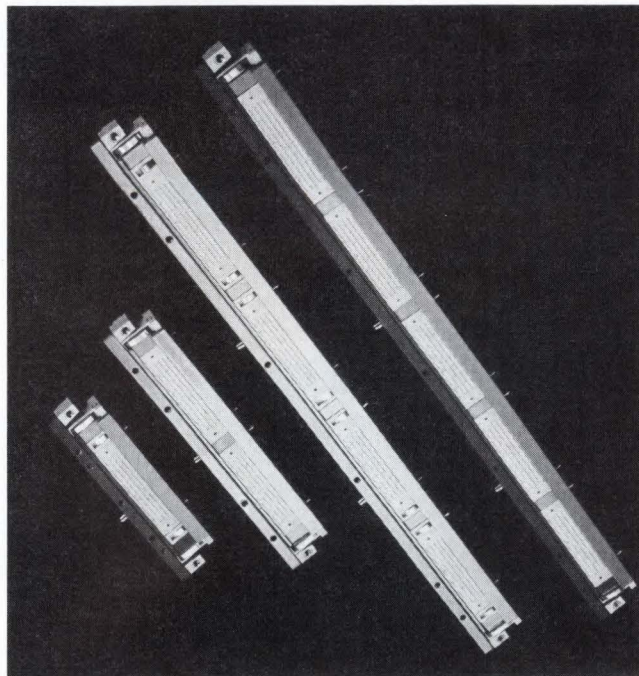
DAVID MALINIAK

**C**onventional connectors, such as post-and-box and pin-and-socket types, are based on long-standing designs. These designs don't fare well with the increasingly fast rise times of today's submicron ICs as their signals pass from board to board. These older interconnection technologies bring with them a paucity of signal density as well as impedance mismatches that can severely degrade signal integrity in high-speed circuitry.

The Interconnection Products Group at Augat Inc., Attleboro, Mass., has come up with an interconnection system that solves these problems in an elegant fashion. The Electronically Invisible Interconnect (EII) maintains the signal integrity of ICs that operate into the gigahertz range with rise times well below 1 ns (*Fig. 1*).

As ICs increase in logic density, connector manufacturers are forced to keep pace in terms of signal I/O, which means much higher contact densities. Higher-density connectors, however, require very high ground-to-signal ratios to reduce the signal reflections and crosstalk generated by the high-speed signals they pass. Because so many contacts must be dedicated to ground—with a ratio as high as 1:1—fewer and fewer contacts are available for signal lines. The result is a drop in effective signal density.

Connector manufacturers define contact density as the total number of contacts available per linear inch of connector length. Signal-contact density, however, is the number of contacts available to carry signals in a high-



**1. WITH MODULAR DESIGN**, Augat's Electronically Invisible Interconnect (EII) can be configured according to the end-user's specifications.



# HIGH-SIGNAL-INTEGRITY CONNECTOR

speed system. The latter is far more important to system designers.

In conventional connectors, high contact densities often result in high costs, more fragile connector construction, and greater degrees of difficulty in routing signals to the contacts. Augat's EII system addresses the signal-contact-density issue with a design that offers a continuous ground plane. This eliminates the need to use signal contacts as ground returns. The modular connector carries true signal-contact densities of 60 to 80 contacts/in., depending on overall length. Modules are available in 200-pin increments to customize interconnections from the signal, power, and ground blocks. A maximum of 1120 I/O lines is possible with this system.

Another significant problem that arises as signal speeds increase is mismatched impedances. Typically, signals move from a printed-circuit pathway of a particular characteristic impedance through a plated-through hole. They then travel along the relatively long path of the mated male-female contacts, which have a different impedance. The signals re-

## PRICE AND AVAILABILITY

As of October 18, prototype costs for a 1000-pin connector range from \$0.75 to \$1 per line, depending on configuration. Target pricing for 1000 pins is \$0.50 per line. Preproduction samples and a test and evaluation kit for electrical characterization will be available in the first quarter of 1990.

*Augat Inc., Interconnection Products Group, 33 Perry Ave., Attleboro, MA 02703; Mike Prisco, (508) 222-2202. CIRCLE 513*

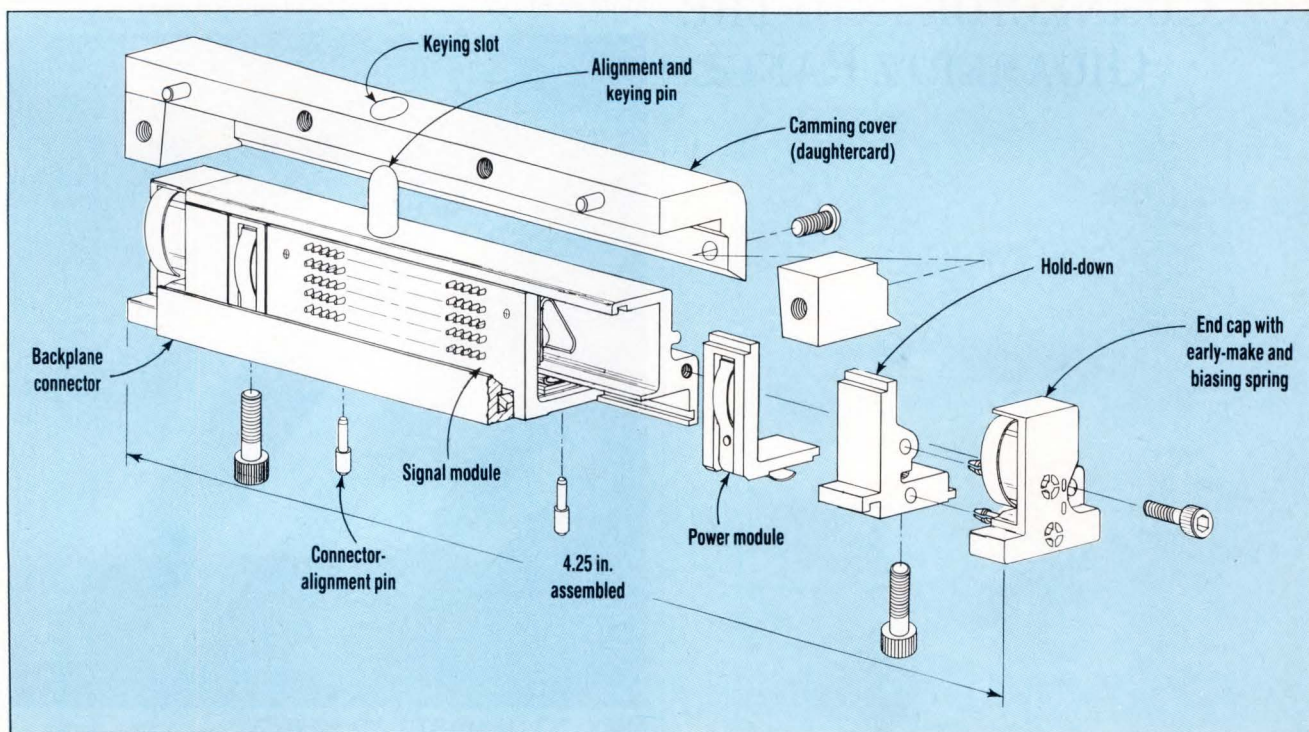
enter the printed-circuit environment by way of another plated-through hole that may have a third impedance.

The EII connector, which is supplied with a user-specified characteristic impedance, reproduces the printed-circuit environment using a flexible circuit as the main signal pathway within the connector itself. The result is an interconnection that's virtually electrically invisible to high-speed signal propagation. Signals pass through the connector with a minimal loss of fidelity.

This impedance-matching feature is one of the EII system's outstanding electrical characteristics. In its standard configuration, the connector's microstrip design supplies an impedance of 50  $\Omega$  with a tolerance of 10%. The connector can be configured to virtually any impedance level by replacing the standard configuration with a new microstrip with adjusted parameters.

The EII is a fully sequential interconnection. First, ground is established through ground clips attached to the backplane portion of the connector system. The purpose of making ground early is to remove electrostatic charges. This makes it possible for the card to reach the same potential as the rest of the system. After making ground contact, power is applied to the daughtercard through power modules rated at 10 A. By mating the signal pins last, the system logic is protected from power-up transients.

In addition, sequencing the interconnection makes it easy to pull and insert daughtercards while the system is powered up. This is a boon for field-repair work and locating board-



**2. DRY-COMPRESSION MOUNTING** of the EII connector uses a cam actuation to reduce insertion forces. Each signal block contains pins that make it possible for the module to float without accumulating tolerance during mounting.



# W I D E S T

## LAMBDA LW SERIES PC-BOARD MOUNTABLE DC-TO-DC CONVERTERS.

**LAMBDA**  
*Electronics*   
Lambda Group of Unitech plc

48 individual models and  
a wide input/output range,  
completely isolated.



# DC-TO-DC S E L E C T I O N



# LW SERIES:

## UP TO 60VDC . . . UP TO 60W, FOR LOW POWER DC-TO-DC APPLICATIONS

Lambda's LW Series DC-to-DC Converters are convection cooled. The addition of a heatsink is not necessary to achieve reliable operation at full output power. Wide range DC voltage operation is a feature of most of the LW modules allowing use in a variety of industrial applications where input voltage specifications might differ.

### FEATURES:

- Available with inputs and outputs to 60VDC, with up to 60W of output power in single and dual output packages. This wide choice allows the design engineer to choose the product that best meets his low power DC-to-DC applications.
- All models are thoroughly regulated and are designed with the necessary PI input filtering. This allows the user to maintain the required voltages at specific loads, regardless of the quality of the input source.
- All models provide an isolation rating of 500VDC. 48VDC nominal input modules feature an industry recognized isolation rating of 1500VDC, ideal for the telecommunications industry. This ensures the user of isolation from the power source to the load.
- Available for one day delivery from stock so that the manufacturing or design engineer may obtain product at a moments notice. This gives flexibility to the manufacturing process and to small breadboard designs.





## DC-To-DC Converters

## SINGLE OUTPUT.

DC INPUT 20.0-40.0 VDC	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE			MODEL
	40°C	50°C	60°C				QTY. 25	QTY. 100	QTY. 250	
	4.75-16 VOLTS ADJ.									
	5.0(25)	4.3(21.5)	3.6(18)	2.5 x 4.5 x 1.5	\$165	\$158	\$150	\$127	\$113	LWS-295-5
	15-30 VOLTS ADJ.									
	1.65(25)	1.4(21.5)	1.2(18)	2.5 x 4.5 x 1.5	165	158	150	127	113	LWS-295-24
	20-40 VOLTS ADJ.									
2.5(50)	2.1(42)	1.8(36)	2.5 x 4.5 x 1.5	219	210	200	170	150	LWS-296-28	
30-60 VOLTS ADJ.										
1.67(50)	1.4(42)	1.2(36)	2.5 x 4.5 x 1.5	219	210	200	170	150	LWS-296-48	

DC INPUT 20.0-60.0 VDC	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE QTY. 25	QTY. 100	QTY. 250	MODEL
	40°C	50°C	60°C							
	4.75-16 VOLTS ADJ.									
	3.0(15)	2.6(12)	2.3(11.5)	1.25 x 3.5 x 2.5	\$131	\$125	\$119	\$101	\$90	LWS-394-5
15-30 VOLTS ADJ.										
1.0(15)	0.9(13)	0.75(11.5)	1.25 x 3.5 x 2.5	131	125	119	101	90	LWS-394-24	

DC INPUT 30.0-60.0 VDC	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE		QTY. 25	QTY. 100	QTY. 250	MODEL
	40°C	50°C	60°C									
	4.75-16 VOLTS ADJ.											
	5.0(25)	4.3(21.5)	3.6(18)	2.5 x 4.5 x 1.5	\$165	\$158	\$150	\$127	\$113	LWS-395-5		
	15-30 VOLTS ADJ.											
	1.65(25)	1.4(21.5)	1.2(18)	2.5 x 4.5 x 1.5	165	158	150	127	113	LWS-395-24		
	20-40 VOLTS ADJ.											
	3.0(60)	2.5(50)	2.1(42)	2.5 x 4.5 x 1.5	219	210	200	170	150	LWS-397-28		
	30-60 VOLTS ADJ.											
	2.0(60)	1.67(50)	1.42(42)	2.5 x 4.5 x 1.5	219	210	200	170	150	LWS-397-48		

## DUAL OUTPUT.

DC INPUT 5V ± 10%	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE			MODEL
	40°C	50°C	60°C				QTY. 25	QTY. 100	QTY. 250	
	± 12 VOLTS ± 3% FIXED									
	.060	.060	.060	1.77 x 1.19 x .40	\$69	\$66	\$62	\$49	\$40	LWD-191-12
	.120	.120	.084	1.85 x 1.85 x .47	84	80	76	60	49	LWD-192-12
± 15 VOLTS ± 3% FIXED										
.050	.050	.050	1.77 x 1.19 x .40	69	66	62	49	40	LWD-191-15	
.100	.100	.070	1.85 x 1.85 x .47	84	80	76	60	49	LWD-192-15	

DC INPUT 12V ± 10%	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE			MODEL
	40°C	50°C	60°C				QTY. 25	QTY. 100	QTY. 250	
	± 12 VOLTS ± 3% FIXED									
	.060	.060	.060	1.77 x 1.19 x .40	\$69	\$66	\$62	\$49	\$40	LWD-291-12
	.120	.120	.084	1.85 x 1.85 x .47	84	80	76	60	49	LWD-292-12
± 15 VOLTS ± 3% FIXED										
.050	.050	.050	1.77 x 1.19 x .40	69	66	62	49	40	LWD-291-15	
.100	.100	.070	1.85 x 1.85 x .47	84	80	76	60	49	LWD-292-15	

DC INPUT 24V ± 10%	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE			MODEL
	40°C	50°C	60°C				QTY. 25	QTY. 100	QTY. 250	
	± 12 VOLTS ± 3% FIXED									
	.060	.060	.060	1.77 x 1.19 x .40	\$69	\$66	\$62	\$49	\$40	LWD-391-12
	.120	.120	.084	1.85 x 1.85 x .47	84	80	76	60	49	LWD-392-12
± 15 VOLTS ± 3% FIXED										
.050	.050	.050	1.77 x 1.19 x .40	69	66	62	49	40	LWD-391-15	
.100	.100	.070	1.85 x 1.85 x .47	84	80	76	60	49	LWD-392-15	



# LW SERIES

## DC-To-DC Converters

### SINGLE OUTPUT.

DC INPUT 4.5-6.0 VDC	MAX CURRENT IN AMPS				DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE QTY. 25	QTY. 100	QTY. 250	MODEL
	45°C	50°C	60°C	65°C							
	5V ± 5% NON-ADJ.										
	.05	0.5	—	0.200	1.85 x 1.85 x 0.47	\$54	\$52	\$49	\$39	\$31	LWS-190-5
	1.0	—	0.400	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-191-5
	12V ± 5% NON-ADJ.										
	0.21	0.21	—	0.084	1.85 x 1.85 x 0.47	54	52	49	39	31	LWS-190-12
	0.42	—	0.168	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-191-12
	15V ± 5% NON-ADJ.										
	0.17	0.17	—	0.060	1.85 x 1.85 x 0.47	54	52	49	39	31	LWS-190-15
0.34	—	0.136	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-191-15	

DC INPUT 4.5-10.0 VDC	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE	QTY. 100	QTY. 250	MODEL
	40°C	50°C	60°C				QTY. 25			
	4.75-16 VOLTS ADJ.									
	2.0(10)	1.7(8.5)	1.5(7.5)	1.25 x 3.5 x 2.5	\$98	\$94	\$89	\$76	\$67	LWS-193-5
	3.0(15)	2.6(12)	2.3(11.5)	1.25 x 3.5 x 2.5	131	125	119	101	90	LWS-194-5
	15-30 VOLTS ADJ.									
	0.65(10)	0.57(8.5)	0.50(7.5)	1.25 x 3.5 x 2.5	98	94	89	76	67	LWS-193-24
	1.00(15)	0.90(13)	0.75(11.5)	1.25 x 3.5 x 2.5	131	125	119	101	90	LWS-194-24

DC INPUT 10.0-15.0 VDC	MAX CURRENT IN AMPS				DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE QTY. 25	QTY. 100	QTY. 250	MODEL
	45°C	50°C	60°C	65°C							
	5V ± 5% NON-ADJ.										
	0.60	0.60	—	0.24	1.85 x 1.85 x 0.47	\$54	\$52	\$49	\$39	\$31	LWS-290-5
	1.20	—	0.48	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-291-5
	12V ± 5% NON-ADJ.										
	0.25	0.25	—	0.10	1.85 x 1.85 x 0.47	54	52	49	39	31	LWS-290-12
	0.50	—	0.20	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-291-12
	15V ± 5% NON-ADJ.										
	0.20	0.20	—	0.08	1.85 x 1.85 x 0.47	54	52	49	39	31	LWS-290-15
0.40	—	0.16	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-291-15	

DC INPUT 10.0-20.0 VDC	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE QTY. 25	QTY. 100	QTY. 250	MODEL							
	40°C	50°C	60°C														
	4.75-16 VOLTS ADJ.																
	5.0(25)	4.3(21.5)	3.6(18)								2.5 x 4.5 x 1.5	\$165	\$158	\$150	\$127	\$113	LWS-195-5
	15-30 VOLTS ADJ.																
1.65(25)	1.4(21.5)	1.2(18)	2.5 x 4.5 x 1.5	165	158	150	127	113	LWS-195-24								

DC INPUT 10.0-30.0 VDC	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS)			DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE QTY. 25	QTY. 100	QTY. 250	MODEL							
	40°C	50°C	60°C														
	4.75-16 VOLTS ADJ.																
	3.0(15)	2.6(13)	2.3(11.5)								1.25 x 3.5 x 2.5	\$131	\$125	\$119	\$101	\$90	LWS-294-5
	15-30 VOLTS ADJ.																
1.0(15)	0.9(13)	0.75(11.5)	1.25 x 3.5 x 2.5	131	125	119	101	90	LWS-294-24								

DC INPUT 20.0-30.0 VDC	MAX CURRENT IN AMPS				DIMENSIONS (inches)	QTY. 1	QTY. 10	PRICE QTY. 25	QTY. 100	QTY. 250	MODEL
	45°C	50°C	60°C	65°C							
	5V ± 5% NON-ADJ.										
	0.60	0.60	—	0.24	1.85 x 1.85 x 0.47	\$54	\$52	\$49	\$39	\$31	LWS-390-5
	1.20	—	0.48	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-391-5
	12V ± 5% NON-ADJ.										
	0.25	0.25	—	0.10	1.85 x 1.85 x 0.47	54	52	49	39	31	LWS-390-12
	0.50	—	0.20	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-391-12
	15V ± 5% NON-ADJ.										
	0.20	0.20	—	0.08	1.85 x 1.85 x 0.47	54	52	49	39	31	LWS-390-15
0.40	—	0.16	—	1.85 x 1.85 x 0.75	65	62	59	47	37	LWS-391-15	



# LW SERIES:

# Specifications

## DC OUTPUT

Voltage range shown in tables.

## REGULATED VOLTAGE

regulation, line . . . . . 0.1% from minimum to maximum and from maximum to minimum. 0.5% on LWS-190, 191, 290, 291, 390, 391. 0.2% on both outputs of dual output models for input variations from 21.6 to 26.4 VDC or 26.4 to 21.6 VDC on LWD-391, 392; from 10.8 to 13.2 VDC or 13.2 to 10.8 VDC on LWD-291, 292; from 4.5 to 5.5 VDC or 5.5 to 4.5 VDC on LWD-191, 192.

regulation, load . . . . . 0.4% for load variations from no load to full load and full load to no load. 1.0% on LWS-190, 191, 290, 291, 390, 391. 0.2% on dual output models.

ripple and noise . . . . . 20mV RMS, 100mV pk-pk for 5V models of LWS-193, 194, 195, 294, 295, 394, 395. 120mV pk-pk for 5V models of LWS-190, 191, 290, 291, 390, 391, and 12V models of LWD-191, 192, 291, 292, 391, 392. 150mV pk-pk for 12V models of LWD-191, 192, 291, 292, 391, 392 and 12V and 15V models of LWS-190, 191, 290, 291, 390, 391. 25mV RMS, 200mV pk-pk for all other models.

efficiency. . . . . LWS-194, LWS-294, LWS-394, and LWS-193: 50% minimum  
LWD-191, 291, 391, 192, 292, 392: 56% minimum  
LWS-195, 295, 395: 57% minimum  
LWS-190: 58% minimum  
LWS-191: 60% minimum  
LWS-391: 64% minimum  
LWS-390: 67% minimum  
LWS-291: 68% minimum  
LWS-290: 70% minimum  
LWS-296, 397: 75% minimum

temp. coeff. . . . . 0.03%/°C. 0.02% on LWS-190, 191, 290, 291, 390, 391 and on all dual output models

## AMBIENT OPERATING TEMPERATURE

Continuous duty 0 to +60°C with suitable derating above 40°C for LWS-193, 194, 195, 294, 295, 296, 394, 395, 397, and dual output models. Continuous duty -5°C to +60°C with suitable derating above 45°C for LWS-191, 291, 391.  
Continuous duty -5°C to +65°C with suitable derating above 50°C for LWS-190, 290, 390.

## OVERLOAD PROTECTION

External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

## STORAGE TEMPERATURE RANGE

-55°C to +85°C. -20°C to +85°C for LWS-190, 191, 290, 291, 390, 391. -30°C to +85°C on all dual output models.

## OVERSHOOT

No overshoot at turn-on, turn-off, or power failure.

## COOLING

All units are convection cooled. No fans or blowers needed.

## MOUNTING

PC board mountable. Refer to outline drawings in catalog.

## OUTPUT VOLTAGE ADJUST

LWS-193, 194, 195, 294, 295, 296, 394, 395, 397  
Output voltage can be set to desired value within the entire range by inserting a resistor between +V and RP terminals. Resistor can be selected as per equations supplied in instruction manual.

## INPUT/OUTPUT CONNECTIONS

DC input and outputs are via pin type connections. Refer to outline drawings in catalog.

## ISOLATION RATING

1500 VDC on LWS-394, 395, 397.  
500 VDC on all other models.

## PHYSICAL DATA

Package Model	Weight		Size Inches
	Lbs. Net	Lbs. Ship	
LWS-190, 290, 390	.10	.12	1.85 × 1.85 × 0.47
LWS-191, 291, 391	.16	.19	1.85 × 1.85 × 0.75
LWS-193	.65	.90	2.50 × 3.50 × 1.25
LWS-194, 294, 394	.65	.90	2.50 × 3.50 × 1.25
LWS-195, 295, 395	.75	1.00	2.50 × 4.50 × 1.50
LWS-296	.75	1.00	2.50 × 4.50 × 1.50
LWS-397	.75	1.00	2.50 × 4.50 × 1.50
LWD-191, 291, 391	.06	.10	1.77 × 1.19 × .40
LWD-192, 292, 392	.09	.12	1.85 × 1.85 × .47

## UL / CSA

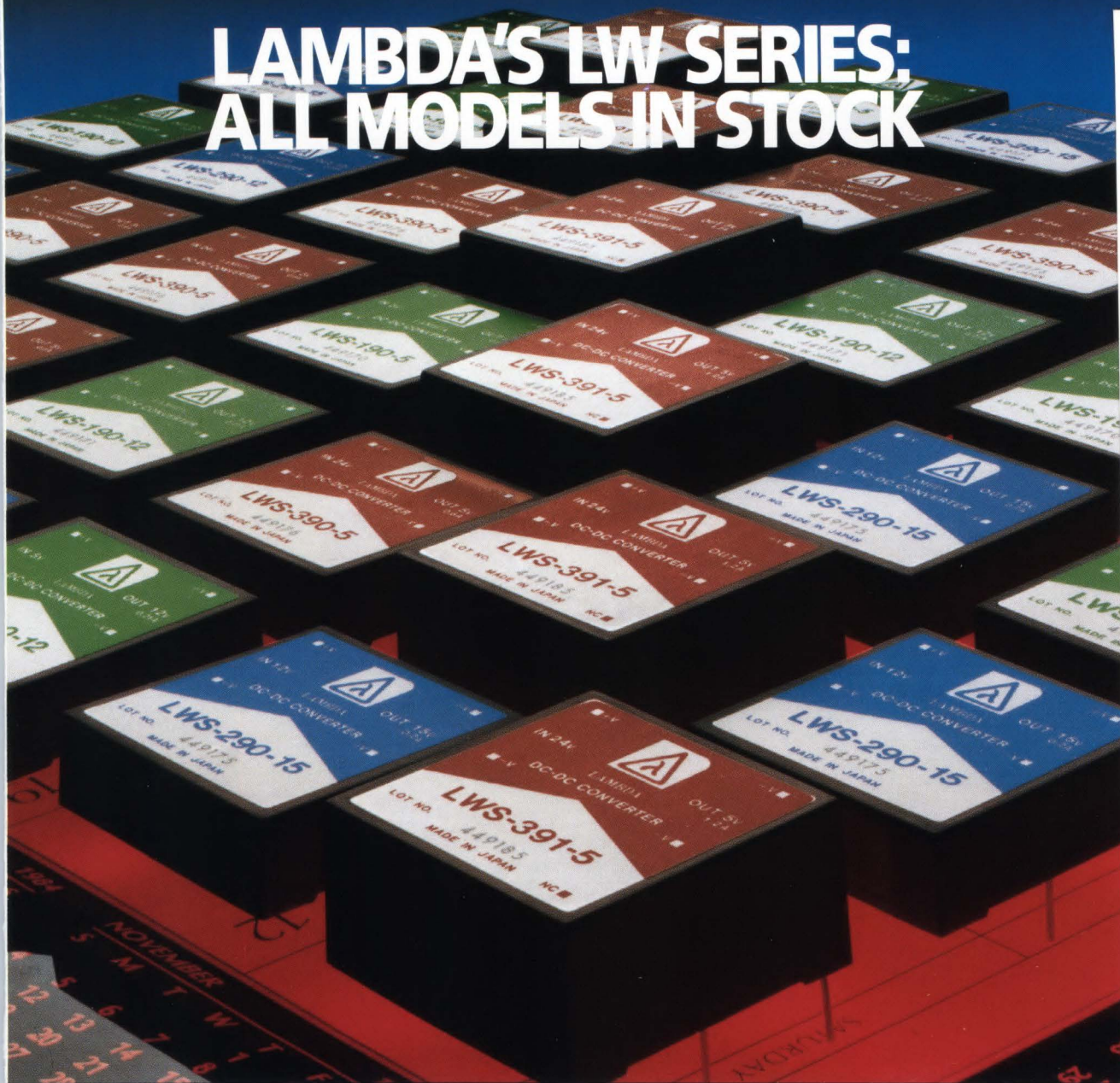
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ED/8H

CIRCLE 113

## HIGH-SIGNAL-INTEGRITY CONNECTOR

level faults.

Besides its unique set of electrical characteristics, the EII system is a surface-mountable connector that reduces the board-to-board pitch on the system backplane. The connector's pins to the backplane are on a 0.05-in. grid, which makes possible a connector pitch as small as 0.8 in. without compromising mechanical performance. The pins mating to the daughtercard are center-spaced at 0.05 in. horizontally and 0.1 in. vertically. This center-spacing provides for 0.05 in. of contact wiping at the separable interconnection areas for high reliability.

Rather than pins, the EII system uses gold-plated posts. The connector is mounted with a dry-compression scheme, in which a designed-in cam actuation reduces the insertion force. The cam actuation also supplies a tactile feedback that indicates when the connector is fully seated

(Fig. 2).

Thanks to the dry-compression mounting feature, manufacturing costs are lower. Because of the shrinkage in connector-feature sizes, alignment has become a critical issue. Elaborate alignment schemes used to decrease connector dimensions are becoming commonplace in the market. But wet-fixturing methods that attach connectors to boards usually mean more manufacturing steps.

As the EII system is attached to boards, each signal block contains pins that enable the module to float without accumulating tolerances during compression mounting. Horizontal and vertical alignment pins ensure that the contacts hit the correct pads on the film and the pc board.

Durability and reliability issues are addressed by the EII system as well. An all-gold system within the

EII connector helps ensure high reliability in the face of environmental stresses. The system's gold interfaces yield superior mechanical contact with a high normal force of more than 100 grams/post. This ensures a high-integrity interconnection for systems operating into the gigahertz range.

A tin-lead interface also can be configured on the backplane side with a minimum normal force of 200 grams/post. Extruded aluminum housings supply mechanical strength and reduce susceptibility to electromagnetic interference. Because low-creep materials are used, excellent performance over temperature is ensured. □

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### CIRCLE

568  
569  
570



# DENSEST GAAS GATE ARRAY DELIVERS 30,000 USABLE GATES

DAVE BURSKY

**P**acking over 30,000 2-input NOR gates and 256 signal pins, the VSC30K gallium-arsenide gate array lets designers build the most complex high-speed circuits to date. Vitesse's chip, which is the largest and latest member of its Fury family, competes head-on with silicon ECL gate arrays in terms of both performance and cost. The most complex ECL chips offer comparable equivalent gate counts, but consume more than twice the GaAs array's typical 8-to-12-W dissipation. What's more, Vitesse guarantees that its array can be 100% utilized, because the routing channels between rows of gates can hold a large number of signal lines.

In terms of performance, circuits built on the VSC30K match the best high-density ECL arrays. D-type flip-flops toggle at rates of more than 1 GHz, and the typical gate delay is 177 ps for a 2-input NOR gate loaded with a fanout of 3 and 1.5 mm of wiring. That gate also has a power dissipation of 1.1 mW and a typical speed-power product of 0.025 pJ. Most logic functions in the company's macrocell library offer a choice of three drive (and power-dissipation) levels to best suit the application.

As with earlier Fury-family members, the 30,000-gate chip is fabricated with a 0.8- $\mu$ m enhancement-depletion MESFET process that yields a die size about half that of silicon ECL arrays with equivalent densities. As a result of the MOS-like processing that Vitesse uses to fabricate the chips, their prices are in the ECL-array ballpark—about \$0.03 to \$0.05 per gate.

To optimize the size of the signal buffers that surround the array, the company included 92 input-only buffers and 156 input/output buffers. Each input cell can be configured as a latch or buffer and can be made compatible with incoming TTL, ECL, or native GaAs-level signals. Input signals are then converted to the in-

ternal GaAs logic levels used by the macrocell's direct-coupled FET logic circuits. Several input cells are pre-configured as high-drive receivers so that they can be used as clock buffers. These special buffers can deliver up to six times the drive of the standard input cell and make it easier to distribute high-speed clock signals throughout the chip.

The I/O cells contain an input cell as a portion of their structure and have more flexibility. Each I/O cell can be an input, output, or bidirectional signal line. The cells can include a latch, flip-flop, or 2- or 3-input ORs or NORs. They also can serve as an inverting or non-inverting buffer. Like the input lines, the I/O cells can be set to handle ECL (10K, 10KH, or 100K), TTL, or native-GaAs signal swings. When configured as outputs, each cell can drive 50- $\Omega$  loads. Also, two drivers can be paralleled to deliver 25- $\Omega$  drive capability.

To house the array, Vitesse has developed a 344-lead ceramic chip carrier that nominally measures 2.34-by-1.46 in., not including the leads, which extend about 0.25 in. beyond the package edge. The chip's actual count of 30,528 2-input NOR gates can implement up to 2544 D-type flip-flops—that's one measure of its integration capability. Versions of the chip are available for operation over

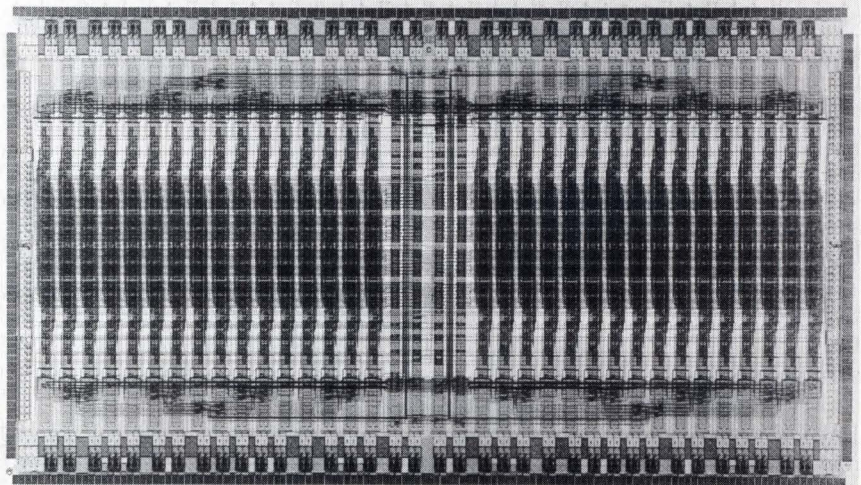
either the commercial or the industrial temperature range (zero to 70°C and -40 to +85°C, respectively).

A wide variety of applications is supported by the array, including computers, workstations, communications, and instrumentation. The Fury family is suited to systems requiring very fast and low-power digital logic at high levels of integration. Existing mainframe systems using ECL or TTL technologies can improve their speed and reduce power dissipation with the Fury arrays. Superminicomputers using ECL arrays can boost system performance while reducing overall cooling requirements. Workstations using standard microprocessors can bring supercomputing power to their system with the Fury arrays. Fiber-optic communication links are another application for the arrays.

Designs are supported by a library of over 50 macrocells; design platforms from Mentor Graphics, Daisy Systems, and Valid Logic; and design tools from Synopsys and Verilog, with more expected next year. First production shipments of the VSC30K arrays are slated for the first quarter of 1990.

Vitesse Semiconductor Corp.,  
741 Calle Plano, Camarillo, CA  
93010; Robert Nunn, (805) 388-3700.

CIRCLE 311





## NEW PRODUCTS

DIGITAL ICs

### BY MATCHING THE BEST SPEED OF TTL PLDs, CMOS IC REPLACES MOST

**P**ushing Intel's CMOS III E process to its best performance yet, the company's 85C220 programmable-logic circuit achieves propagation delays as short as 10 ns—the best to date for EPROM-based CMOS PLDs. The chip also offers more flexibility than simple 20-pin PLDs. Its eight macrocells each have programmable I/O architectures for registered or combinatorial operation. As a result, the chip can replace most popular 20-pin D- and even E-grade PLDs—while significantly trimming power use.

When idling, the chips enter a zero-power mode. They draw just 0.5 mW when operating in medium-speed (25-ns propagation delay) systems and 200 mW maximum when used at top speed. The 85C220 uses from 25% to as little as 1% of the average bipolar TTL PLD's power. The high-speed circuit is also 100% pin-compatible with Intel's 5C032 alternate source to Altera Corp.'s 5032 programmable-logic device. Intel, however, also improved on the circuits by adding an extra output-enable p-term to each macrocell in the 85C220. They also boosted the output drive capability by raising the current drive for the low-logic level on the outputs to 12 mA.

The chip has a maximum counting frequency of 80 MHz (with feedback for the count chain). Its clock-to-output delay is 5.5 ns and setup time is 7 ns. The programmable I/O cells can be set up to give the chip a total of 18 inputs (10 dedicated and eight when the I/O cells are programmed as inputs), or 10 inputs and a maximum of eight outputs.

The chip comes in either a windowed 20-pin ceramic DIP, 20-pin one-time-programmable (OTP) plastic DIPs, or plastic leaded chip carriers. Prices start at \$7.95 in quantities of 1000 for the OTP plastic-DIP version. Delivery is from stock.

Intel Corp., 1900 Prairie City Rd., Folsom, CA 95630; (916) 351-8080.

CIRCLE 312

DAVE BURSKY

### MEMORY CONTROLLERS MANAGE TRIPLE-CHANNEL SCSI DATA BUFFERS

**W**ith NCR Corp.'s 52C60 and 52C61 memory-management chips, a microprocessor-hosted SCSI subsystem can manage a large buffer built from dynamic RAMs. That buffer can be accessed by up to three peripherals that use a fixed-priority scheme to determine which of the three peripheral channels has access to the memory. As a result, the buffer's basic memory bandwidth is improved. The 52C60 can address up to 256 kwords of dynamic RAM, while the 52C61 addresses 1 Mword.

In the 52C60, the memory port can transfer data at rates of 6 Mwords/s when working with 85-ns dynamic RAMs. The 52C61, which can operate at the same speed, offers a "fly-by" mode, in which data moves from the peripheral to the buffer without passing through the controller chip. As a result, the controller works with buffers wider than eight bits. Also included on both controllers are two general-purpose 16-bit timers and RAS-only refresh signals for the RAMs.

While not limited to SCSI applications, the memory-control chips can tie into NCR's 53C90 SCSI controller. The three peripheral channels (A, B, and C) on the 52C60 and 61 supplement the host-processor and memory-interface ports. Channel A supplies a 1-bit-wide tag field that can be attached to blocks of data transferred from the buffer to the peripheral. The fields provide pointers to other data blocks or simply the number of blocks. Channel B has a 9-bit SCSI data bus and a 4-byte FIFO register that reduces buffer latency. The third channel is a control port.

The 52C60 comes in a 68-lead plastic leaded chip carrier while the 52C61 requires an 84-lead PLCC. In lots of 5000, the chips cost \$21.35 and \$23.25, respectively. Samples are available now.

NCR Corp., 1635 Aeroplaza Dr., Colorado Springs, CO 80916; Brian Brown, (719) 596-5612.

CIRCLE 313

DAVE BURSKY

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CIRCLE 61



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Intel® 386™ Microprocessor Clock Speed	Micron MT56C0816 Cache Data SRAM*	
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\*All timing rated at 100 pF loads. The MT56C0816 is available in a 52-pin plastic leaded chip carrier (PLCC).

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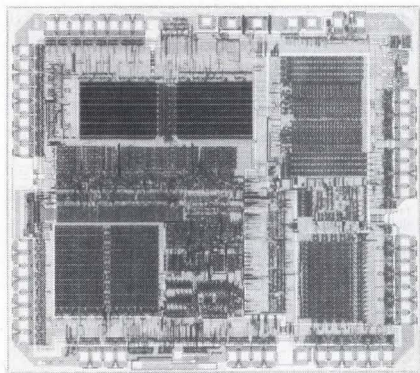
CIRCLE 51



## NEW PRODUCTS

DIGITAL ICs

### MORE I/O, DUAL-PORT RAM, AND FIFO REGISTERS BOOST MICROCONTROLLER



**B**y adding 21 more I/O lines, a dual-port 16-byte mailbox RAM, and twin 20-byte FIFO registers, Advanced Micro Devices' 80C525 microcontroller delivers a superset of the features of its 8051 and 80521 siblings. Additional features include an enhanced interrupt subsystem with eight interrupt sources, and the means for a DMA controller or host CPU to access the 80C525's data space. The single-chip CMOS controller packs 53 I/O lines as well as an 80C51 core, two 16-bit counter-timers, 256 bytes of RAM, 8 kbytes of ROM, a programmable watchdog timer, and a full-duplex serial port.

The small dual-port RAM provides an optimized asynchronous slave interface with a 90-ns access time. Write operations to the dual-port RAM generate interrupts to the microcontroller, which can then respond to the interrupt. Data-transfer rates are independent, thanks to the 20-byte FIFO registers that buffer data over two of the ports. Each register has full threshold-level detection to match the 80C525's latency to that of the external CPU or DMA controller.

The chip is housed in a 68-lead plastic leaded chip carrier. In quantities of 5000, the 12-MHz version of the processor sells for \$17.12 and the 16-MHz version costs \$19.52. A ROM-less version is also available. Samples ship next month.

*Advanced Micro Devices Inc., P.O. Box 3453, 901 Thompson Pl., Sunnyvale, CA 94088; (408) 732-2400.*

CIRCLE 314

### DUAL RS-232 TRANSCEIVER IC WITHSTANDS 1520 V RMS FROM INPUT TO OUTPUT

**A**dding high-voltage electrical isolation to an RS-232 I/O channel once required costly, space-hungry pc-board circuitry. Maxim's 40-pin MAX252 holds two transceivers rated at 1520 V rms for one second between inputs and outputs, 1260 V rms for one minute, and 130 V rms continuously. UL approval for the device is pending. The MAX252 is intended for industrial communication and control applications where the isolation eliminates ground loops and helps reduce the effects of voltage transients and numerous noise sources from the 9600-bit/s data.

The double-width plastic DIP contains two transceivers conforming to EIA specification RS-232 and CCITT recommendation V.28. Two CMOS ICs in the package, one on either side of the isolation barrier, hold transceiver and transformer-driver circuits. The barrier itself consists of four fast optocouplers (one each for the input and output of each channel) and a small toroid transformer that transfers power across the barrier from the hardware to the cable side. No other parts are needed.

The MAX252's optocouplers limit maximum (guaranteed) data rates to 9600 bits/s, but the transceiver ICs inside support rates well above the practical 20-kbit/s limits specified for RS-232. To transmit at data rates to 90 kHz, users can build their own circuit with the MAX250 and MAX251, which are the chips contained within the MAX252, and 6N136 optocouplers.

The MAX252 runs off one 5-V supply. Maximum operating current is 130 mA. In quantities of 100, the commercial-temperature-range MAX252CHL costs \$32. The extended-industrial-range MAX252EHL goes for \$38.40 in similar quantities. Small quantities are in stock.

*Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Garry Shapiro, (408) 737-7600.*

CIRCLE 315

FRANK GOODENOUGH

# Experience



# Gourmet Multi-Chips



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CIRCLE 62



## NEW PRODUCTS

DIGITAL ICs

### SPEEDY EEPROMS COME IN BOTH COMMERCIAL AND MILITARY VERSIONS

**W**ith access times as short as 90 ns, a family of 256-kbit electrically-erasable

PROMs from Microchip Technology tackles high-performance commercial and military applications. The family's fastest chip, the 28HC256, comes in both military-qualified and commercial versions and sports a 90-ns access time. The chip also includes

a page-write mode that allows it to store 64 successive bytes in only 3 ms. In comparison, most other 256-kbit EEPROMs require about 10 ms. This means the Microchip circuit can load new programs much faster than the slower chips—an important consideration if program upgrades are transferred using a telephone or other communication channels.

All of Microchip's 256-kbit chips are organized as 32 kwords by 8 bits and operate from a 5-V power supply. When in standby, the EEPROMs have a current drain of just 150  $\mu$ A. When operating at full speed, they draw an operating current of 65 mA.

Commercial versions of the chip come in 90-, 120- and 250-ns speed grades. MIL-STD-883C types include 90-, 100-, 120-, 150- and 200-ns versions. Prices for commercial units range from \$54 to \$135. The military chips range from \$177 to \$246. All prices are for lots of 1000.

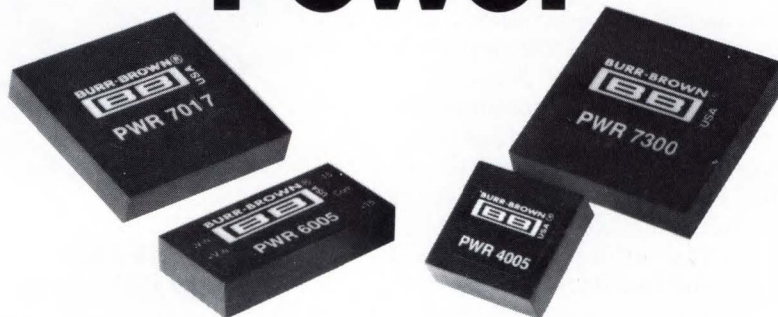
*Microchip Technology Inc., 2355 West Chandler Blvd., Chandler, AZ 85224-6199; Jim Ciraulo, (602) 963-7373.*

CIRCLE 316

DAVE BURSKY

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PWR73XX	3W, Regulated	2x2x0.4
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PWR70XX	5W, Regulated	2x2x0.4

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CIRCLE 81

### I/O CONTROLLERS SUIT PC APPLICATIONS

Manufactured in CMOS, two highly integrated interface controllers are designed for a wide variety of personal computer-based I/O applications. The SAB 82C250-N combines two serial I/O ports with a parallel bidirectional printer interface. The SAB 82C251-N has one serial I/O port and one parallel bidirectional interface. Both devices can also use the parallel port in an IBM PS/2 register-compatible mode. Serial I/O ports have baud rates of up to 512 kbaud and are compatible with 16550 AC characteristics for PS/2 applications. The parallel printer port eliminates the need for external drivers by supplying a high-current drive for data. In 1000-unit lots, respective prices for the SAB 82C250-N and 82C251-N are \$10 and \$7.

*Siemens Components Inc., Integrated Circuit Division, 2191 Laurelwood Rd., Santa Clara, CA 95054; (408) 980-4526.*

CIRCLE 346



## NEW PRODUCTS

DIGITAL ICs

### PLDs IN CMOS, TTL, AND ECL ALL VIE FOR HIGH-SPEED APPLICATIONS

**P**arallel technology developments in CMOS, TTL, and ECL by National Semiconductor have yielded the fastest programmable logic devices in all three technologies. In CMOS, the company has released 10-ns, 20- and 24-pin electrically-erasable PLDs, the GAL16V8A and 20V8A, which are faster versions of Lattice Semiconductor's original GALs. The TTL chips—a series of 20-pin, 7-ns PAL devices—will initially include the popular 16L8, 16R4, R6, and R8. The ECL ICs—the PAL10/10016C4-2 pair of 2-ns PAL devices—offer 10K and 100K interface levels, respectively.

Both of the 10-ns CMOS chips contain eight programmable macrocells. Either chip can replace most popular PAL devices in their respective 20- and 24-pin DIP formats. The chips also come in 20- and 28-lead plastic leaded chip carriers.

The TTL chips drop into sockets that held their slower predecessors. However, the company's vertical-fuse structure resulted in a worst-case programming yield of 99.8%.

Lastly, the ECL circuits, which come in 28-lead plastic leaded chip carriers, inject just a 2-ns delay into the signal path. The circuits have four complementary outputs, 16 complementary input pairs, and 32 product terms.

Samples of all circuits are available and some typical prices in quantities of 100 are \$60.50 for the ECL chips, \$7.90 for the TTL PALs, and \$6.45 for the CMOS GALs. Delivery is from stock.

*National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000.*

CIRCLE 317

DAVE BURSKY

### FAST CACHE MEMORY IS APPLICATION-SPECIFIC

An ultra-high-speed memory device matches the performance of fast PC processors running from 16 to 33 MHz. The Model CXK7701J is a two-

way set-associative cache memory. Used with the Intel 80386 CPU and the 82385 cache controller, the application-specific memory combines the functions of address latch, memory, and transceiver into one or two ICs. Maximum access times are 10, 13, 16,

and 18 ns. Based on 8.0- $\mu$ m CMOS technology, the part comes in a 52-pin PLCC. Samples cost \$49.50.

*Sony Corp. of America, Component Products Co., 10833 Valley View St., Cypress, CA 90630; (714) 229-4190.*

CIRCLE 347

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CIRCLE 87



## 1-MICRON CMOS STANDARD-CELL FAMILY BOASTS EXTENSIVE LIBRARY

A joint venture between Hitachi America Ltd. and VLSI Technology Inc., San Jose, Calif. has yielded an extensive standard-cell library for Hitachi's new 1- $\mu$ m CMOS family. The two-layer silicon gate HG51 series is Hitachi America's first standard-cell product line.

The HG51-series devices operate at speeds of up to 60 MHz from one 5-V power supply. At 20  $\mu$ W/gate/MHz, the devices exhibit extremely low power dissipation. The series has TTL, CMOS, and Schmitt-trigger-I/O compatibility. Separate I/O and core-power buses reduce chip noise. In addition, the 1- $\mu$ m CMOS process produces gate-delay times of just 0.7 ns.

The HG51 series standard-cell library was codeveloped with VLSI Technology Inc. It consists of more than 300 cells covering a wide range of functions including gates, buffers, complex gates, flip-flops, multiplexers, decoders, and various I/O functions.

Other development tools include a powerful cell compiler that creates RAM, ROM, and multipliers for any configuration, and a data-path compiler that creates functions like barrel shifters and n-bit ALUs. Logic-synthesis software designs complex functions by describing these functions as a state diagram, Boolean equation, or truth table. All of these tools and macros can be used on Apollo, Daisy, DEC, Hewlett-Packard, Mentor, Sun, and Valid workstations.

Hitachi is taking customer designs now. Customers can use Hitachi America's new design center in Brisbane for assistance with any step of the design process. Prices and nonrecurring engineering charges are dependent on the complexity of the design.

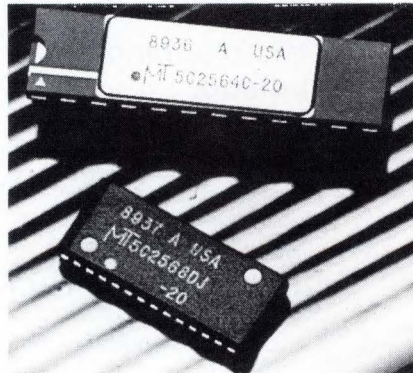
*Hitachi America Ltd., Semiconductor and IC Division, Hitachi Plaza, 2000 Sierra Point Pkwy., Brisbane, CA 94005-1819; (415) 589-8300.*

**CIRCLE 331**  
LISA GUNN

## FAST SRAM FAMILY ADDS 20-NS, 256-KBIT MEMORY CHIPS AND 25-NS CACHE

Two new offerings were added to Micron Technology's family of fast static RAMs (SRAMs): a family of 20-ns 256-kbit SRAMs in by-one, by-four, and by-eight configurations, and a 25-ns cache data SRAM. Both parts are fabricated in double-layer metal, double-layer polysilicon technology. A four-transistor memory cell stores data using a 5-V ( $\pm 10\%$ ) power supply. All of the Micron memory devices meet Jedec standards.

The cache data SRAM can operate in two configurations. It acts either as a single 8-kword-by-16-bit memory, or as two 4-kword-by-16-bit memories with common addresses and data. Access times of 25, 35, and 45 ns let the cache RAM work with 33-, 25-, and 20-MHz microprocessors, respectively. The output-enable time is



10 ns.

Built-in address latches on the cache devices reduce system chip count. The cache chip directly interfaces with Intel Corp.'s 82385 cache-memory controller and 80386 microprocessor in either the direct-mapped or two-way set-associative modes.

Samples of the MT5C2561 (by one), MT5C2564 (by four), and MT5C2568 (by eight) 20-ns 256-kbit SRAMs are available now for less than \$100 per unit. The MT56C0816 cache SRAM is available now for \$44 per unit in quantities of 100.

*Micron Technology Inc., 2805 East Columbia Rd., Boise, ID 83706; (208) 383-4000.*

**CIRCLE 319**  
LISA GUNN

## ICS INCREASE PRODUCT TESTABILITY

Three integrated circuits simplify the implementation of boundary-scan testability of printed circuit boards, boxes, and systems as specified in IEEE P1149.1. Two of these functions, the ACT8990 test bus controller and the ACT8997/8999 scan path selector, allow designers to partition a system into several short scan paths. As a result, each scan path is provided with a fault tolerance that helps minimize data-path corruption. The third device, the ACT8994 16-bit digital bus monitor, lets designers monitor signal paths off-line with the IEEE P1149.1 test bus or monitor signal paths at the system clock rate using the device's embedded memory. Each of the three components are part of Texas Instruments' System Controllability/Observability Partitioning Environment, SCOPE for short.

*Texas Instruments Inc., Semiconductor Group (SC-959), P.O. Box 809066, Dallas, TX 75380; (800) 232-3200, ext. 700.*

**CIRCLE 340**

## 16K STATIC RAMS ACCESS IN 12 NS

Three 16-kbit static RAMs, designed for such applications as cache memory, graphic buffers, and look-up tables, feature a fast address access time of 12 ns over the commercial temperature range. The devices have TTL I/O interfaces and offer industry-standard pinouts and functional-compatibility to permit upgrading. The SSM6116 is organized as 2k by 8 bits with common data I/O. The SSM6168 and 6170 are both 4k-by-4-bit parts with common data I/O. Additionally, the SSM6170 is equipped with an output-enable feature that facilitates control for a tristated bus. All are fabricated in a BiCMOS process. A wide variety of packaging options is available, including DIP, PLCC, and SO configurations. Prices start at \$20.80 (1000 units).

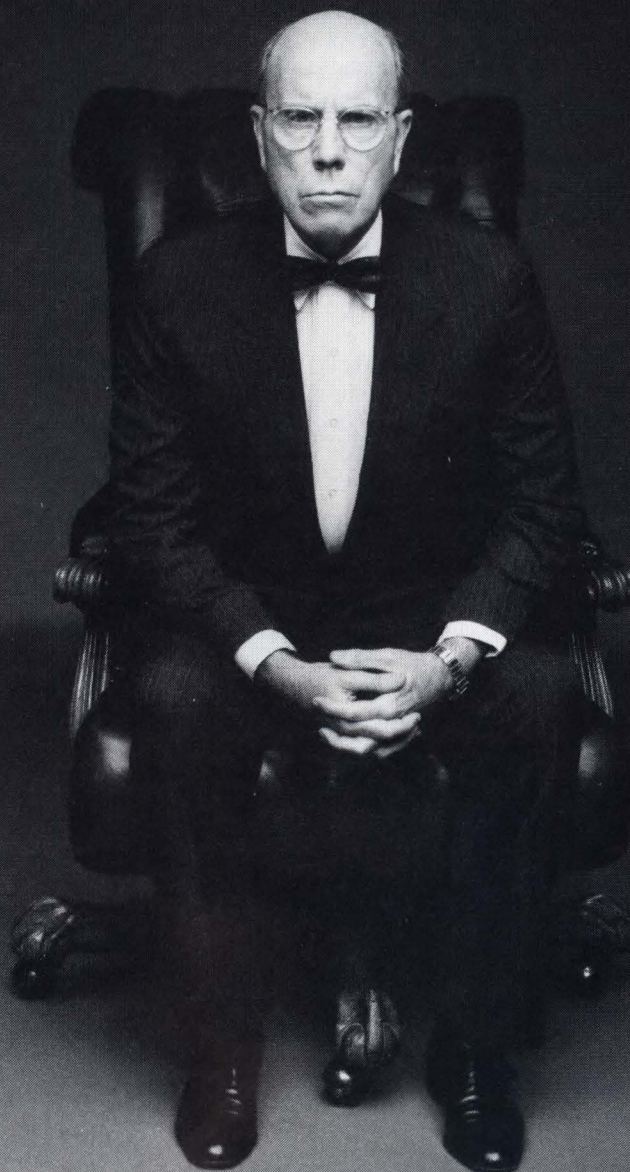
*Saratoga Semiconductor, 686 W. Maude Ave., Sunnyvale, CA 94086; (408) 522-7500.*

**CIRCLE 341**



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# NORTHWEST AIRLINES



## EISA-BASED 80486 PC DELIVERS TOP SPEED WITHOUT CACHE

**B**y combining Intel's 80486 microprocessor, an extended industry standard architecture (EISA) bus for peripheral expansion, and a proprietary memory-controller chip, Hewlett-Packard has created the highest-performance member of its Vectra PC family. The memory subsystem in the Vectra 486 PC follows a tightly coupled path to the 80486 along with intelligent paging control, burst transfers, and parity checking. The system, which runs at 25 MHz, delivers 33% higher throughput than a 33-MHz 80386-based PC and more than double the floating-point throughput of the 80386—even when working with its 80387 math coprocessor.

Using the memory subsystem, up to 64 Mbytes of main memory can be coupled directly to the CPU board, and that memory can be composed of pairs of 1-, 4-, or 8-Mbyte single-inline memory modules with 80-ns access times. All other add-in cards plug into the eight 32-bit EISA bus slots. One such optional card is a VGA display controller that was also released with the system.

The Vectra 486 also has an optimized disk subsystem with a drive that delivers data at a rate of 20 Mbits/s off the head. That high data-transfer rate and a short 15.5-ms access time make the mass-storage subsystem about 33% faster than any other Winchester PC subsystem. A 128-Mbyte tape-backup subsystem is optional.

The basic model 150 comes with 2 Mbytes of RAM; a 5.25-in., 1.2-Mbyte floppy disk drive; and one 152-Mbyte hard-disk drive. It costs \$13,999 (video controller and display are optional). Larger 330- and 670-Mbyte drives come with models 330 and 670, respectively. Prices increase to \$16,999 and \$19,999, respectively for those two upgrades. Systems will be available in the first quarter of 1990.

Hewlett Packard Co., 3000 Hanover St., Palo Alto, CA 94304; (415) 857-1501.

CIRCLE 320

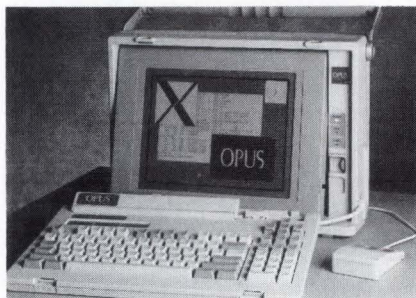
DAVE BURSKY

## GET 21 MIPS FROM A COMBINATION PC AND WORKSTATION

**W**ith its RISC and CISC processors that run DOS and Unix operations at the same time, Opus Systems' model 8110 Portable Mainframe comes the closest yet to a cross between a PC and a workstation. The 22-lb. machine accomplishes this feat by integrating a Motorola 88000 chip with an Intel 80386 microprocessor.

Opus has expanded the functionality of the two operating systems, allowing users to transfer files between Unix and DOS. Also, commands for one operating system can be executed from the other. A single keystroke jumps the user back and forth between operating systems.

The Personal Mainframe comes with Opus' version of the standard Unix Version 5, Release 3.2. The software contains all the standard utili-



ties, commands, and other programs found in the AT&T release, as well as the portable C compiler and an ANSI-standard Fortran 77. The CISC side of the Portable Mainframe runs MS-DOS version 3.3. The memory subsystem contains 4 Mbytes of parity-protected dynamic RAM (expandable to 24 Mbytes) while the I/O subsystem contains 2 Mbytes of dynamic RAM.

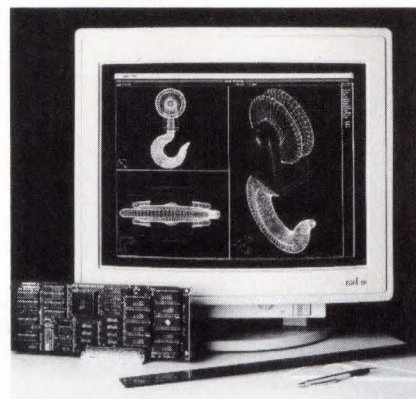
Designed for single or multiple users, the 25-MHz, 21-MIPS computer is suitable for such applications as CAD, CAE, and other compute-intensive areas. Available immediately, the Portable Mainframe sells for \$13,995.

Opus Systems Inc., 20863 Stevens Creek, Building 400, Cupertino, CA 95014; (408) 446-2110.

CIRCLE 321

RICHARD NASS

## RISC-BASED ENGINE ACCELERATES CAD GRAPHICS ON MACINTOSH PC



**T**he speed of pans, zooms, and redrawing is improved by as much as 10 to 30 times by the QuickCAD NuBus card for the Apple Macintosh II family. The card lets the systems deliver CAD graphics at speeds comparable to any competitively priced upgrade to an IBM PC or compatible. The QuickCAD card, from Radius, uses a low-cost 32-bit RISC processor that delivers about 6 MIPS of computing power. Proprietary display-list-processing software gives the system the tools it needs to accelerate the Macintosh's graphics operations.

The QuickCAD engine consists of the NuBus card and the accompanying display-list software. The card transfers data over the NuBus at up to 32 Mbytes/s using the NuBus's block-transfer capability. As a result, it moves data up to seven times faster than the Macintosh's processor can transfer. The software contains a combination initialization and /cdev file that is placed in the Macintosh system folder and is activated at startup.

Because the card adheres to Apple Computer Corp.'s 32-bit QuickDraw standard, all software programs operate normally on Macintosh II platforms. The first software driver will be for Autodesk Inc.'s AutoCAD software. The card and software costs \$1495 and are available now.

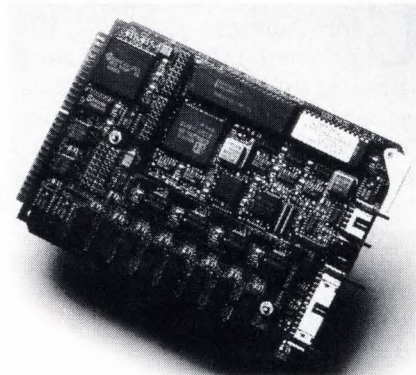
Radius Inc., 1710 Fortune Dr., San Jose, CA 95131; (408) 434-1010.

CIRCLE 322

DAVE BURSKY



## INDUSTRIAL COMPUTER FAMILY MEETS STRICT SPECIFICATIONS



A family of industrial computers from Pro-Log Corp. provides multitasking and multiprocessing (parallel-processing) capabilities for complex control systems and single-board controllers for embedded-control applications. Designated the System 2 series, the family's three computers each meet a common set of rugged specifications that include a zero-to-65°C operating-temperature range, a MTBF of more than 10 years at 55°C, and the ability to withstand up to 40 Gs of shock and 5 Gs of vibration.

The STD-bus cards plug into a passive backplane for easy service. They differ only in their core processor set.

The high-end model 60 is based on a 25-MHz 80286 microprocessor. Model 40 is built around a 16-MHz 80386SX processor. At the low end, model 25 uses a 9.55-MHz V20 microprocessor. All three systems come with MS-DOS 3.3 built in. Model 60 comes with 1 Mbyte of RAM; Model 40 has either 512 kbytes or 1, 2, or 4 Mbytes; and Model 25 is supplied with either 128 or 256 kbytes.

All three models contain a PC-compatible serial port, an interrupt controller, a counter-timer, and a time-of-day clock. Model 25 adds a second serial port and a printer port.

The systems are available now with prices beginning at \$895.

Pro-Log Corp., 2560 Garden Rd., Monterey, CA 93940; (408) 372-4593.

CIRCLE 323

RICHARD NASS

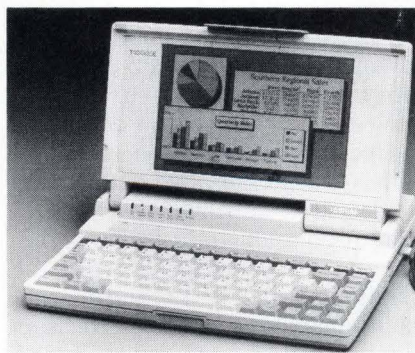
## NOTEBOOK PC MAINTAINS DESK-TOP PERFORMANCE LEVEL AT A LOW PRICE

As may have been expected, Toshiba has thrown its hat into the notebook-PC ring. Its T1000SE weighs in at 5.9 lbs., has dimensions of 12.4 by 10.2 by 1.78 in., and comes with a full-size, 82-key keyboard. But best of all, the price was held down to just \$1699.

The computer contains an industry-standard 1.44-Mbyte, 3.5-in. disk drive, which maintains compatibility with other systems. The PC also features 1 Mbyte of RAM that is expandable to 3 Mbytes. MS-DOS 3.3 is built into ROM for automatic booting when the system is turned on. The T1000SE system's processor is an 80C86 running at 9.54 MHz.

The PC's backlit-LCD display has adjustable contrast and brightness, measures 4-3/4 by 7-5/8 in., and features 640 by 400 pixels. The company says that its CGA-compatible display is actually better than CGA—the characters are more defined because there are twice as many dots.

The unit's power-management features include the ability to turn



off power to the display. In non-processor-intensive applications like word processing, the CPU's speed can be dropped from 9.54 to 4.77 MHz, which further conserves battery life. In addition, the removable battery pack can be recharged in four hours. The computer will be available in January.

Toshiba Information Systems Inc., Computer Systems Division, 9740 Irvine Blvd., Irvine, CA 92718; (800) 334-3445.

CIRCLE 324

RICHARD NASS

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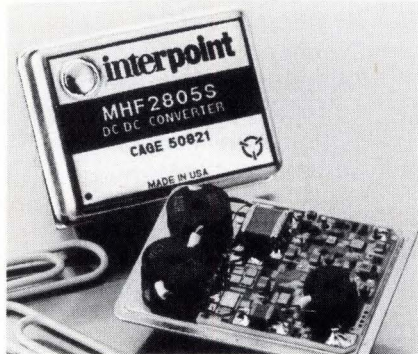


## 12-W DC-DC CONVERTER BREAKS 30-W/IN.<sup>3</sup> BARRIER WITH MIL SCREENING

**M**ajor increases in packaging density for military, aerospace, and high-reliability industrial applications are promised by the MHF series of dc-to-dc converters from Interpoint. The series offers 12 W of power in a package only 0.315 in. high. With a cubic volume of less than 0.5 in.<sup>3</sup>, power density is 30 W/in.<sup>3</sup>, which is the industry's highest. Not only that, the devices include internal filtering, eliminating the need for external capacitors.

The miniature supply is designed to meet full MIL-STD-883 environmental standards. Operating temperature for the hermetically sealed metal case is -55 to +125°C. Models are available that offer full rated power at the high-temperature limit. The converters also meet the MIL-STD-883 5000-g acceleration requirement and have a MIL-HDBK-217 MTBF rate of over 1.5 million hours at 45°C.

Key to the high power density is a proprietary design technique that permits operation at 600 kHz with up to 84% conversion efficiency. Units are available with single or dual outputs at +5,  $\pm 12$ , or  $\pm 15$  V over a



wide input range of 16 to 40 V dc. Typical load and line regulation is within 10 mV.

The MHF series dc-dc converters start at \$296 in lots of 100. Delivery is from stock to 30 days.

*Interpoint Corp., 10301 Willows Rd., P.O. Box 97005, Redmond, WA 98073-9705; (206) 882-3100.*

**CIRCLE 325**

**DAVID MALINIAK**

## TINY OP AMP PUTS OUT $\pm 160$ V AT $\pm 200$ A PEAK AND $\pm 90$ A CONTINUOUSLY

**C**rammed into less than 3/4 of a cubic foot, Copley Controls' Model 232-10 power amplifier can function as a 14-kW op amp, a programmable dc and/or ac voltage or current source; or a  $\pm 160$ -V power conditioner rated at  $\pm 200$  A peak or  $\pm 90$  A continuous. Moreover, if that's not enough power, up to 20 of these 95%-efficient amplifiers can be paralleled to yield almost 300 kW of sine-wave power to 4 kHz.

The secret behind these power amplifiers is, of course, switching. Pulse-width modulation is employed at 81 kHz to provide a 4-kHz 3-dB bandwidth. Internal filtering removes the harmonics of the switching frequency. While putting out 100 A at 200 Hz, total harmonic distortion is 0.2%. In addition, the amplifier doesn't need a regulated power supply. It will work off one unregulated 60-to-160-V dc source.

Settling time is impressive. For a positive or negative 100-A pulse, the output settles to within 100 mA (0.1%) of the final value in 1.2 ms. It's 0.3 ms quicker to 1 A.

Various applications can take advantage of the Model 232-10's capability and performance. For instance, it can be used for control of the focusing and beam steering magnets in the nuclear accelerators used for research as well as the synchrotrons used in chip-making X-ray lithography. They also can energize the gradient coils of magnetic-resonance-imaging scanners. Precision electroplating processes using "pulse-reverse" current sources can make use of the amplifiers, as can high power, sub-audio active sonar. Finally, they can replace vacuum-tube linear amplifiers.

In quantities of one to nine, the Model 232-10 goes for \$7500 each. Delivery is in 6 to 8 weeks after receipt of order.

*Copley Controls Corp., 375 Elliot St., Newton, MA 02164; Barry Friedman, (617) 965-2410.*

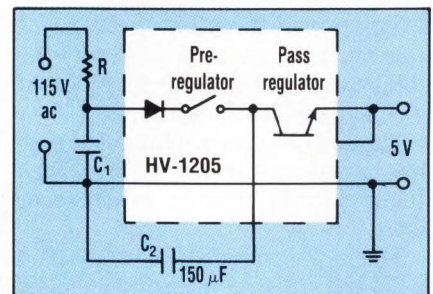
**CIRCLE 326**

**FRANK GOODENOUGH**

## 8-PIN DIP RECTIFIES 115-V AC LINE; YIELDS REGULATED 5 TO 24 V DC AT 50 MA

**C**onnect the 8-pin plastic mini-DIP containing Harris' HV-1205 to the 115-V ac line, along with a handful of resistors and capacitors, and the result is a user-programmable 5-to-24-V dc regulated power supply rated at 50 mA. Take care, however: The output is not isolated from the ac line. Set the output at +5 V and it varies a maximum of 15 mV as the line is varied from 80 to 132 V rms. Load regulation is just as good. The output holds within 40 mV as the load is varied from 5 to 50 mA. Both line and load specifications are given over temperature and both commercial (HV-1205-5) and extended-industrial (HV-1205-9) range versions are available.

The chip is built on a dielectrically isolated (DI) bipolar process rated at a breakdown of 400 V. It consists of two sections: a patented switching preregulator followed by a series-



pass regulator. The preregulator connects  $C_2$  to the ac line until it charges to 6 V above the preset output voltage. It then switches to a blocking mode, where it stays until the next line cycle starts. The capacitor supplies power to the series-pass regulator and to the load, which is connected between pins 6 and 3. Each cycle refreshes the charge on the capacitor. Resistor R limits the inrush current to  $C_2$ .

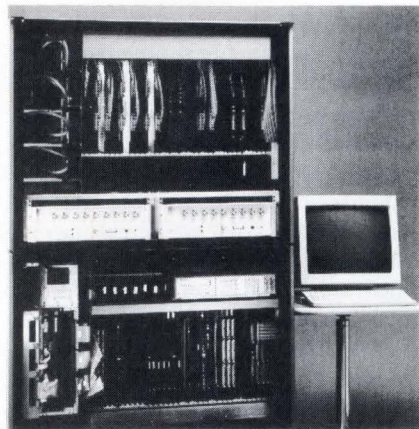
In quantities the HV-1205-5 and HV-1205-9 respectively go for \$3.06 and \$2.55 each. Small quantities are in stock.

*Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; Gloria Simpson, (407) 724-3739. CIRCLE 327*

**FRANK GOODENOUGH**



## MIXED-SIGNAL TESTER BOASTS DUAL-CLOCK TIMING SYSTEM



A parallel synchronous and asynchronous per-pin design gives the STS 5000 the flexibility to do both characterization and volume testing of mixed-signal devices. The tester's dual-clock timing system lets engineers mix synchronized and asynchronous modes, timing, and digital patterns to simulate different real-world conditions.

Digital signals can be run synchronously on all of the system's 64 channels or asynchronously on 16 channels. Devices with separate analog and digital sections can be tested at different clock speeds or synchronized to either of the two speeds. The system, which is controlled by a 32-bit Sun computer, has 1 Mvector of memory per pin and a 20-MFLOP floating-point array processor to speed throughput. The processor can perform a 1000-point fast-Fourier transform in 3.4 ms.

An optional ISDN subsystem does functional testing of S- and U-interface devices. The subsystem features differential outputs and multi-level coding, jitter generation, and an ISDN hardware transmission-line simulator.

Deliveries will begin in the second quarter of 1990, with prices ranging from \$350,000 to \$700,000, depending on configuration.

*Semiconductor Test Solutions, Axion Technology Div., 21 North Ave., Burlington, MA 01803; (617) 229-6611.*

CIRCLE 328

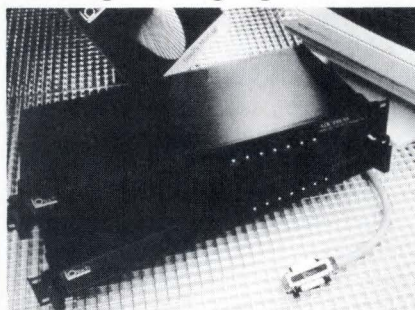
JOHN NOVELLINO

## 100-KSAMPLE DIGITIZERS FEATURE 16-BIT RESOLUTION, HIGH NOISE IMMUNITY

As outboard standalone instruments, two high-resolution digitizers from Iotech are shielded from the noisy environment that surrounds plug-in digitizers inside the controlling computer. Both IEEE-488-based units offer 100-kHz maximum sampling rates with 16-bit resolution.

The ADC488/16 features 16 single-ended or eight differential analog channels. The ADC488/8S has eight differential analog inputs and independent sample-and-hold circuits that reduce interchannel skew to  $\pm 20$  ns. Channel sequences can be programmed to any of 20 levels from 1  $\mu$ s to 50 s in a 1, 2, 5, 10 sequence. Programmable inputs of  $\pm 1$ ,  $\pm 2$ ,  $\pm 5$ , and  $\pm 10$  V are available.

A variety of trigger capabilities permits unattended signal acquisitions and lends the units to use as digital oscilloscopes or waveform digitizers. For analog-input-level triggering, both the level and slope are programmable. Users can also program the digitizers to trigger on the rising or falling edge of an exter-



nal TTL signal or choose the IEEE-488 Group Execute Trigger (GET) and Talk commands for triggering.

The instruments store acquired data in a 2-ksample buffer (expandable to 128 ksamples), and use direct memory access to output the data at up to 200 kbytes/s.

The ADC488/16 costs \$1495, and the ADC488/8S goes for \$1995. Both units are available immediately.

*Iotech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4093.*

CIRCLE 329

JOHN NOVELLINO

## 34-GHZ DIGITIZING SCOPE INCLUDES TDR AND ANALYSIS CAPABILITY

Designers working in the high microwave range will find the HP 54123T four-channel, 34-GHz digitizing oscilloscope especially useful. The scope includes a time-domain reflectometer (TDR) function and analyzes statistics.

Automatic scaling and parameter measurements, along with a 9-in. color display and menu-driven front panel, make the HP 54123T easy to use. The unit is programmable over the HP-IB (IEEE-488), and users can output the waveform, scaling information, and measurement results to plotters and printers.



The scope can trigger on signals to 2.5 GHz, but an optional external trigger, the HP 54118A, handles signals with bandwidths to 18 GHz. Because it uses true-edge triggers rather than countdown triggers, the HP 54123T can trigger on rf bursts, logic signals, and sine waves.

A 12-bit analog-to-digital converter offers up to 14 bits of effective voltage resolution. Matched IF filters ensure a low noise floor that permits a sensitivity of 1 mV/div.

The built-in TDR function measures impedance, reflection coefficient, and distance from a reference plane. Differential, as well as standard, TDR measurements are possible. Using the internal statistical analysis and histogram capability, designers can make quantitative and repeatable noise measurements and evaluate jitter and eye patterns without an external controller.

The HP 54123T costs \$34,800 with an estimated delivery time of seven weeks after receipt of order. The HP 54118A 18-GHz trigger costs \$8925.

*Hewlett-Packard Co., Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80901-2197; (800) 752-0900.*

CIRCLE 330

JOHN NOVELLINO



## VIDEO DACS SPAN 4-TO-8-BIT RESOLUTION AND PACK LCD-CONTROL CIRCUITRY

A family of monolithic triple video digital-to-analog converters with on-chip color palettes have bandwidths of 65 MHz—high enough to handle the 1024-by-768-pixel resolution of the IBM 8514/A standard. There are three basic versions of the converters: one with triple 4-bit converters, another with triple 6-bit devices, and a third with three 8-bit d-a converters. The converters are fabricated with a merged bipolar-CMOS process.

The HD153108 packs triple 4-bit converters and runs at 50 MHz. The HD153109, 129, and 119 run at 65 MHz with 6-bit resolution. Lastly, a lone triple 8-bit unit, the HD153110, also runs at 65 MHz. In addition to their triple video outputs, the HD153108 and 109 both include circuits that control a monochrome liquid-crystal display (LCD). Color-LCD panels can be controlled by the HD153119 and 110 6- and 8-bit palette d-a converters, which supply RGB digital data to the flat display. The third 6-bit unit, the HD153129, replaces the VGA interface's original Inmos color-palette chip.

Included on the 4-bit chip is a blanking input for display control and a four-color overlay color register for cursors or menus. On the two proprietary 6-bit converters, a pixel word mask is included for display control. The 8-bit converter chip includes a programmable black level of zero or 7.5 IRE and has selectable timing synchronized to the rising or falling edge of the clock.

The HD153108 and 109 come in 44-lead plastic leaded chip carriers and sell for \$26.60 and \$25.60, respectively, in quantities of 1000. Both are available from stock. Prices for the other chips have not yet been set. Samples of the 28-pin HD153129 are available, while both the 153119 and 110 will be sampled in early 1990.

*Hitachi America Ltd., 2000 Sierra Point Pkwy., Brisbane, CA 94005; John Hull, (415) 589-8300.*

CIRCLE 318

DAVE BURSKEY

## FAST, PRECISE UNITY-GAIN-STABLE OP AMPS COME TWO AT A TIME

National Semiconductor's several-year-old junction-isolated complementary bipolar process has produced a precision op amp, the dual LM6118, and it was worth waiting for. For example, its minimum open-loop gain over temperature reaches 90 dB while putting  $\pm 10$  V across 500  $\Omega$ . That rises to 100 dB when putting  $\pm 17$  V across 10 k $\Omega$ . That's while running off  $\pm 20$ -V rails. Or, it can put  $\pm 1$  V across 50  $\Omega$ .

Minimum unity-gain bandwidth is 14 MHz and a typical settling time to 0.01% for a 10-V step is 400 ns. Minimum slew rate over temperature at a gain of +1 is 50 V/ $\mu$ s. At a gain of -1, the minimum rate is 30 V/ $\mu$ s. This translates into a full-power bandwidth of 1 MHz. That's while driving 500  $\Omega$  with  $\pm 10$  V. Total harmonic distortion is 3%. Moreover, two of these come in a DIP for \$4.65 in quantities of 100. That union of speed and output current demands just 7.5 mA from the supply rails.

These op amps' blend of unity-gain stability and speed lend them to applications where the closed-loop noise-gain is unity—output amplifiers for fast 12-bit d-a converters, fast integrators, and active filters. By using both halves of the device, users can build a single-ended input to a differential output amplifier that can swing 40 V pk-pk at 1 MHz.

Maximum bias current and offset voltage over temperature are no more than 1250 nA and 4 mV respectively, regardless of grade. Similarly, common-mode rejection ratio is never less than 75 dB. As noted, price in quantities of 100 start at \$4.65 each in an 8-pin plastic DIP for a -40° to +85°C device. The part also comes in 14-pin plastic DIPs and SOICs, 8-pin ceramic DIPs, and 8-pin metal cans. Military versions are also available. Small quantities are available from stock.

*National Semiconductor Corp., P.O. Box 58090, Sunnyvale, CA 95052-8090; Bettina Briz, (408) 721-2274.*

CIRCLE 339

FRANK GOODENOUGH

## MULTIPLEXERS TAKE $\pm 60$ -V FAULT ON INPUT OR OUTPUT WITH POWER OFF OR ON

In a typical data-acquisition system using general-purpose IC analog multiplexers, faults that put much more than the supply voltage across the chip's input or output pins cause it to self-destruct. Worse, the expensive system may go with it. Now, Maxim's MAX378/389 has ended that problem. Without power applied, these CMOS chips can take up to  $\pm 75$  V on either their input or output pins. Under this condition, a maximum of 20  $\mu$ A of leakage current flows in the circuit whether 0 or 5 V is on the digital-control pins. Under similar conditions, but powered up with  $\pm 15$  V on the supply pins, no more than 40  $\mu$ A flows. A fault voltage always sees an open circuit.

These chips double the voltage rating and improve on the performance of available fault-protected multiplexers. Their inputs can be protected from high-voltage transients by simple RC circuits or varistors. There's another advantage in systems in which the input channel of more than one multiplexer samples the same analog signal. If one multiplexer is powered down or fails, signal integrity is maintained.

The MAX378 and MAX379 are 8-channel single-ended and 4-channel differential break-before-make circuits, respectively. Series-connected n-channel, p-channel, and n-channel MOSFET switches provide fault protection. Access time, break-before-make delay, enable delay, and settling time to 0.01% are respectively 1000, 25, 1500, and 3500 ns. On resistance runs a maximum of 4000  $\Omega$  over temperature. Off isolation at 25°C with a 7-V rms, 100-kHz signal and a 1-k $\Omega$  load is 50 dB minimum. Both multiplexers come in 16-pin plastic and ceramic DIPs as well as 16-pin SOICs. Commercial-, industrial-, and military-grade units are available. In quantities of 100, prices start at \$13.31.

*Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.*

CIRCLE 332

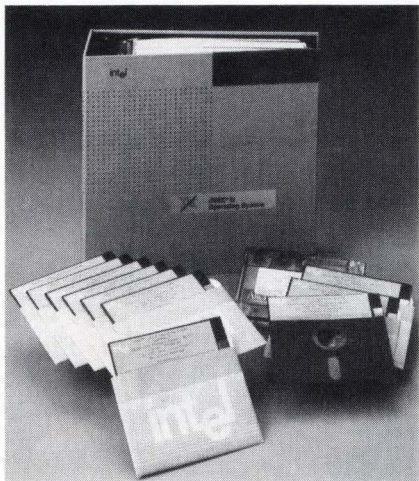
FRANK GOODENOUGH



## NEW PRODUCTS

SOFTWARE

### REAL-TIME 80386 OPERATING SYSTEM JUMPS FROM 16 TO 32 BITS



With Intel's introduction of the iRMX III operating system, they have extended their existing software to 32 bits. This protected-mode, real-time operating system was designed with the 80386 microprocessor in mind.

The 32-bit version of iRMX III is binary-compatible with existing 16-bit iRMX II applications. This means those applications can be run concurrently with 32-bit code. In addition, 16- and 32-bit tasks can communicate with one another.

The operating system gives users more powerful I/O capabilities, and lets them use memory pools up to 4 Gbytes. On top of that, it improves integer-math performance with its 32 bits and permits larger segment sizes to be processed.

Users familiar with previous versions of the software won't need any training to upgrade to the newer level. The user interface is almost identical. The operating system sells for \$5650 for the AT bus version and \$6450 for the Multibus version and is available immediately. Users of version II can upgrade to version III for \$3150. The software is shipped with the ASM 386 assembler, the PL/M 386 compiler, SMD III debug monitor, and a text editor.

Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Santa Clara, CA 95052; (800) 548-4725. **CIRCLE 333**

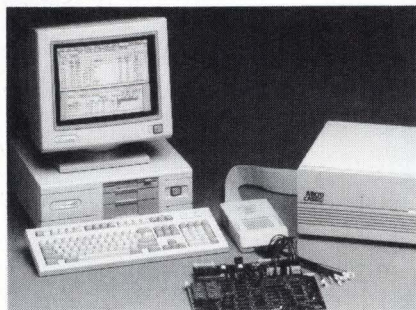
RICHARD NASS

### SOFTWARE-ANALYSIS WORKSTATION ADDS REVERSE ENGINEERING

With the addition of the P1750A probe and ISA-1750A disassembler software, Cadre Technologies' Software Analysis Workstation (SAW) can reverse-engineer, debug, and test software for 1750A-based applications. Companies developing 1750A-based software can use the SAW not only for verification of new code, but also for analysis and debugging of existing software.

Any of the popular 1750A implementations can be accommodated by the new probe. It connects to the target using coaxial flying leads. These connections can be made directly at the processor, from peripheral controllers, at defined debug ports, or at any point on the target where signals are accessible.

The probe opens the door for engineers to use Cadre's PathMap run-time reverse-engineering tool on 1750A-based software. PathMap creates a comprehensive run-time view of 1750A embedded-software execution from one in-target measurement. It does so by drawing a structure chart, which represents the code's actual behavior.



The P1750A probe and ISA-1750A disassembler software are available now. Existing users of the SAW can upgrade by buying the probe for \$3500, the software for \$765, and the SFA-1750A accessory-kit software for \$145. Complete systems start at \$17,000.

Cadre Technologies Inc., Portland Division, 19545 N.W. Von Neumann Dr., Beaverton, OR 97005; (800) 547-4455. **CIRCLE 334**

LISA GUNN

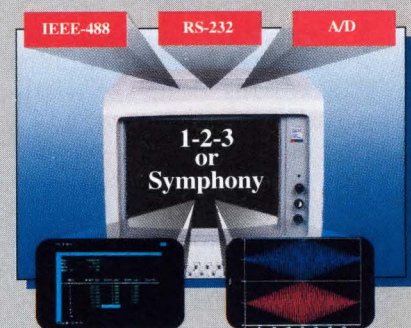
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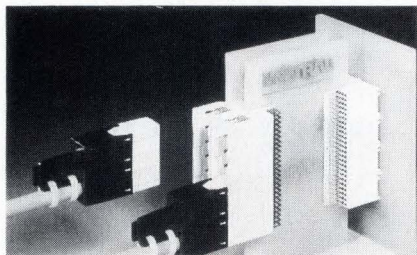
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CIRCLE 67



## 2-MM CONNECTOR SYSTEM FITS IN WITH IEEE'S FUTUREBUS PLUS STANDARD

**F**uturebus Plus, which has been designed as the next-generation standard bus that will pick up where the VME and Multibus II formats leave off, has an interconnection system ready that fits its standards. The Metral connector system, introduced jointly by AT&T



Microelectronics and DuPont Electronics, meets the IEEE's Futurebus Plus working group's standard.

The system is based on a 2-mm grid and provides up to 432 signal positions on a double-height Euro-board, which is more than twice the 192 signal positions available with today's DIN connector system. Boards can be spaced on a 15-mm pitch.

Components are included in the modular system for board-to-board and board-to-cable interconnections with input/output options. It is based on a 12-mm building block to provide connectors with 24, 48, 96, and 192 contact positions.

The system's modularity enables designers to upgrade their designs to take on new functions without major changes. It is compatible with the 96-pin DIN connector for systems that combine Futurebus Plus and Multibus boards.

In large volumes, both companies estimate that pricing will range from \$0.05 to \$0.10 per mated pair. Production quantities will be available in the first quarter of 1990.

*AT&T Microelectronics, 555 Union Blvd., Dept. 52AL330240, Allentown, PA 18103; (800) 372-2447.*

**CIRCLE 335**

*DuPont Electronics, Barley Mill Plaza, Customer Service, Wilmington, DE 19880-0022; (800) 237-2374.*

**CIRCLE 336**

DAVID MALINIAC

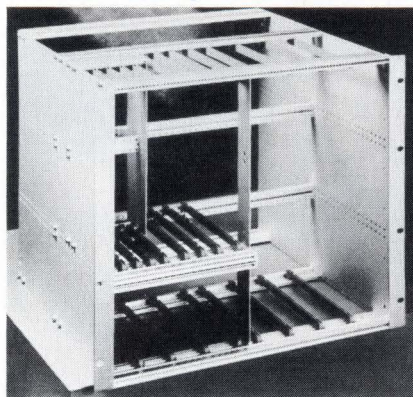
## SUBRACK MECHANICALLY SUPPORTS AND PROTECTS ELECTRONIC SYSTEMS

**C**alled the industry standard for the 1990s, BICC-Vero Electronics' KM6-II subrack succeeds the company's KM6 subrack. The new unit incorporates all the benefits of its predecessor, such as rugged construction, totally conductive components, and low piece-part counts. The unit is easily converted into a high-performance EMC subrack.

The KM6-II is fully compatible with all existing KM6 accessories, front panels, and plug-in units. Besides full compliance with IEC standard 297-3, the subrack offers increased strength for applications involving vibration.

In addition to its likeness to the earlier design, the KM6-II sports some new features. It is easier to assemble and customize, and its guides are assembled or removed simply and quickly. The guides can be fixed with a screw where required, and offer an anti-vibration boss and provision for a grounding clip. The entire unit is conductively finished.

In addition to the standard version, which accepts 220- and 160-mm



boards, the KM6-II is available in a universal version that houses Euro-cards of different sizes in a variety of configurations.

The KM6-II subrack will range from \$98 to \$325 in single quantities. Delivery is from stock to 6 weeks.

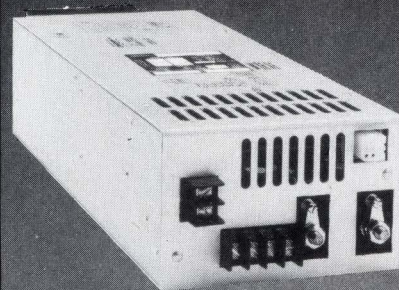
*BICC-Vero Electronics Inc., 1000 Sherman Ave., Hamden, CT 06514; (800) 242-2863.*

**CIRCLE 338**

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CIRCLE 78



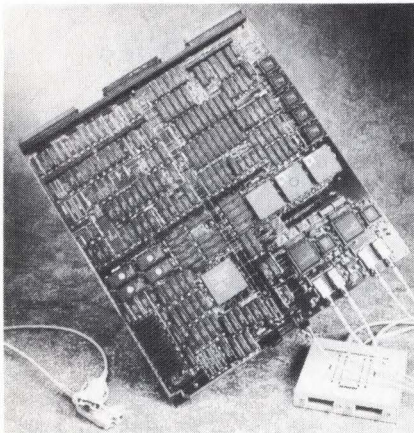
## NEW PRODUCTS

COMMUNICATIONS

### DEVELOPER'S PROGRAM AIDS OEM IMPLEMENTATION OF FDDI NETWORKS

A combination of hardware, software, training, and support is now available to OEMs and system integrators to help them evaluate and implement FDDI networks. CMC's Forerunner program is based on the company's VMEbus FDDI network interface.

Offered to developers, CMC's VMEbus FDDI processor implements the company's FXP architecture. An Advanced Micro Devices 29000 microprocessor with RISC architecture provides full throughput on the FDDI network and the VME-



bus interface.

The CMC-1056 card is being offered in two versions of the Forerunner developer's kit. The first kit is designed for OEMs and integrators who want to develop device drivers using CMC-135 Ethernet adapters and to be able to use those drivers for FDDI later. It contains two CMC-135 Ethernet boards and two CMC-1056 cards. The second package provides two CMC-1056 cards for users interested only in FDDI.

The FDDI developer's kit with FDDI and Ethernet interfaces costs \$29,995. The FDDI-only version goes for \$24,995. Both kits include two days of training at CMC and 90 days of telephone engineering support as well as software development. Both versions are available from stock.

CMC, 125 Cremona Dr., Santa Barbara, CA 93117; (805) 968-4262.

CIRCLE 337

DAVID MALINIAK

### TOKEN BRIDGES SUPPORT IBM SOURCE ROUTING

The TokenMaster 400 family of IBM token ring bridges is one of the first to offer 100% compatibility with the IBM source routing protocol. The products can be used to integrate token rings in both broadband and baseband environments. Frequency agile across six user-selectable channels, the TokenMaster 400 broadband bridge connects multiple 4-Mbit/s IBM token rings as far as 10 km away and is available in both single-cable and dual-cable versions. The TokenMaster 425 subnetwork bridge allows users to seamlessly interconnect multiple token ring networks in a baseband environment. All IEEE 802.5-compatible bridges are driven by a 12-MHz 80286 processor. External broadband channel switches and ROM-based programming permit plug-and-play performance. Units cost \$5890.

Netronix, 1372 N. McDowell Blvd., Petaluma, CA 94952; (800) 282-2535 or (707) 762-2703.

CIRCLE 344

### MODEM IC MEETS EUROPEAN NEEDS

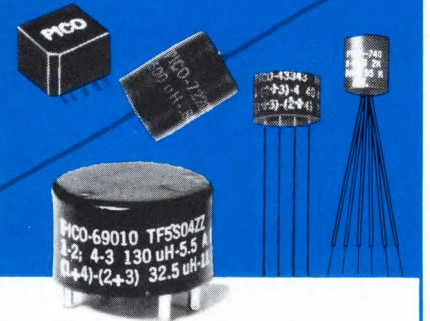
The SSI 73K321L single-chip modem, designed specifically for European Videotex applications, can outperform other solutions when operating over a range of European telephone line conditions. It is both V.23- and V.21-compliant and requires only 30 mW from a single 5-V power supply. The device operates at 1200-bit/s in the V.23 mode (for Videotex) and allows 300-bit/s fall-back in the V.21 mode (for PC and other telecommunication applications). In addition to detecting and generating the 2100-Hz answer tone needed for call initiation, the circuit provides a number of other functions, including FSK modulation and demodulation. Packaging options for the SSI 73K321L include 22- and 28-pin DIPs, as well as 20-pin PLCCs. In lots of 100, the device sells for \$11.

Silicon Systems, 14351 Myford Rd., Tustin, CA 92680; (714) 731-7110.

CIRCLE 345

## PICO POWER INDUCTORS

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CIRCLE 43

ELECTRONIC

DESIGN  
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## NEW PRODUCTS

### COMMUNICATIONS

#### IC CREATES 1553B BUFFERED INTERFACE

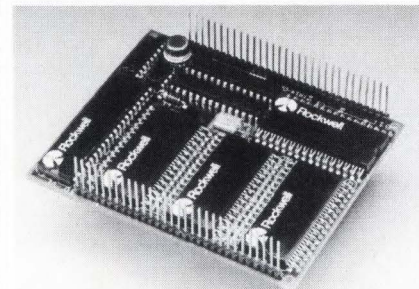
Intended for both military and commercial applications, the MCT83000 remote terminal interface unit provides a fully buffered intelligent link

between either a single- or dual-redundant MIL-STD-1553B data bus and any 8- or 16-bit CPU. Each 2.375-by-2.375-in. package contains two low-power 1553B transceivers, a 1553B monolithic remote terminal protocol device, a gate array for

memory contention resolution and control, a 2k-by-16-bit area of double-buffered dual-port RAM into which all 1553B transfers to the host CPU are memory mapped, and four MSI devices to buffer the MCT83000's initialize word and make available the 1553B command word. The part allows the host CPU to access the memory at all times and guarantees that only complete valid messages are received or transmitted. Packaging possibilities include 90-pin quad-in-line configurations and 90-pin flat-packs. Single-unit pricing starts at \$1450.

*Marconi Circuit Technology Corp., 45 Davids Dr., Hauppauge, NY 11788; (516) 231-7710. CIRCLE 348*

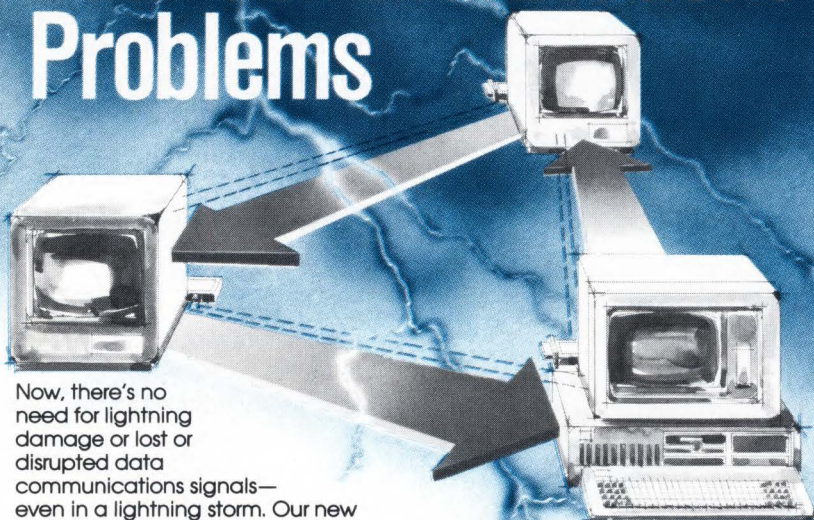
#### V.32 MODEM PROVIDES 12-KBIT/S TURBO MODE



Packaged as a dual-in-line module, the RC9696/12 V.32-compatible modem supports data transmissions at 9600 bits/s, as well as a turbo mode, in which data is transmitted at 12,000 bits/s. The unit can be used with all of the popular dial-up standards, in addition to the 12-kbit/s full-duplex mode for dial-up operation over the public switched telephone network. CMOS construction results in a low power consumption of only 2 W (typical). Standard features include trellis-coded modulation (TCM) for improved error detection and correction, adaptive equalization, a parallel microprocessor bus interface, a CCITT V.24/RS-232-C port, and a dynamic receive range of -43 to 0 dBm. The 3-1/4-by-4-in. module sells for \$250 in lots of 1000 units.

*Rockwell International Corp., Semiconductor Products Division, 4311 Jamboree Rd., P.O. Box C, MS 501-300, Newport Beach, CA 92658; (714) 833-4700. CIRCLE 349*

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# Watt's Up<sup>TM</sup> from Semiconductor Circuits, Inc.

## New 7.5 Watt DC/DC Converter Series Achieves Breakthrough Performance

The pioneering technology leader in encapsulated power converter modules, Semiconductor Circuits, Inc. introduces the HA series. The HA series offers up to 7.5 watts in single or dual outputs in a product configuration more typical of 3 to 5 watt converters.

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reflected ripple,  
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circuit

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tection,  
six-sided  
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and tight output  
regulation, the  
new HA series is perfect for board-  
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requiring low output noise.

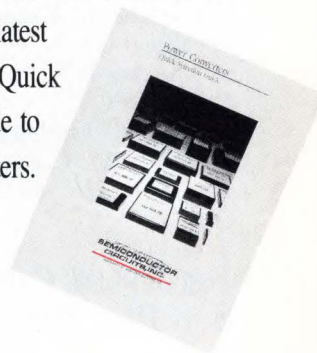


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and 15, as well as  
 $\pm 12$  and  $\pm 15$  Vdc. And all these  
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Circuits, Inc. distributor or representa-  
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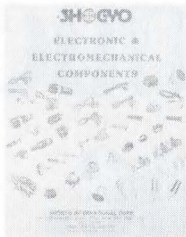
49 Range Road • Windham, New Hampshire 03087  
(603) 893-2330

CIRCLE 69



## CATALOG DESCRIBES CONNECTOR LINE

Schematics and photographs are used to illustrate this 40-page catalog of miniature, microminiature, and subminiature connectors; jacks; and plugs. Covering both standard and custom designs, the publication provides data on such connectors as modular, panel, and chassis mount; pc board mount; DIN; coaxial; miniature and feeder consent; BNC, UHF, and MIC; and communication types in a wide variety of angles, sizes, and shapes. Terminal boards, binding posts, barrier strips, clips, and fuse holders are also depicted.



*Shogyo International Corp., 287 Northern Blvd., Great Neck, NY 11021; (516) 466-0911.* **CIRCLE 350**

## ARCNET LAN PRODUCT SUMMARY

Volume I of the *Local Area Network Product Summary* is a 12-page tabloid that discusses the merits of ARCNET local area networks in industrial applications. In addition to comparisons between ARCNET and Ethernet, the document describes hardware, software, and training products for LAN designers, managers, and administrators. It is organized by bus structure and vendor, offering products from nine different sources for the IBM PC bus, 3U and 6U VMEbus, Q-bus, and Unibus structures under MS-DOS, OS/2, Unix, RTUX, VMS, and OS-9 operating systems. Extensive technical specifications are given for starter kits linking PCs, PC to VMEbus, and Q-bus to PC.

*C&C Technology Inc., Bldg. 9, Unit 60, 245 W. Roosevelt Rd., West Chicago, IL 60185; (312) 231-0015.* **CIRCLE 351**

## DECOUPLING CAPS SUIT PGA DESIGNS

Information is provided in this eight-

page pamphlet on Rogers' Micro/Q 3000 capacitors, a family of very low inductance decoupling capacitors specifically designed for through-hole mounting under pin-grid-arrays (PGAs), PGA sockets, and socketed PLCCs and LCCs. The brochure discusses their key benefits, performance characteristics, supplies all necessary specifications, and shows how to incorporate the Micro/Q 3000 into the user's design.

*Rogers Corp., 2001 W. Chandler Blvd., Box 700, Chandler, AZ 85244; (602) 963-4584.* **CIRCLE 352**

## BOOK FOCUSES ON SUN WINDOW SYSTEM

The first in a planned 10-book series, *The NeWS Book* is a definitive work on Sun Microsystems' Network/extendible Window System (NeWS). Aimed at users who have a basic understanding of programming and window systems, it serves as a guide to developing windowed applications. Other books in the Sun Technical Reference Library series will address SPARC, RPC programming, and CAD/CAM. Next to be introduced is *The SunTechnology Papers*, which will include articles from Sun's quarterly magazine, *SunTechnology*. The books will be available in computer book stores or directly from the publisher, Springer-Verlag. For more information about *The NeWS Book*, contact Gerhard Rossbach, Springer-Verlag, at (805) 963-7960.

*Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; (415) 960-1300.* **CIRCLE 353**

## DIGITAL SCOPE EVALUATION KIT

Users and prospective users of digital oscilloscopes can compare various models with the Scope Evaluation Kit. The kit contains a surface-mount circuit board that generates three test signals typical of applications in which 100-500-MHz digital scopes are used. An instruction manual and 9-V battery are included so testing can be performed within minutes. The kit also includes a booklet

that discusses important criteria to look at when considering a change from an analog to a digital oscilloscope.

*Tektronix Inc., P.O. Box 500, Beaverton, OR 97077; (800) 426-2200.* **CIRCLE 354**

## COAXIAL COMPONENTS

Detailed specifications, as well as operating and installation information, are given in the 60-page *Coaxial Components Catalog* (literature release 5959-7861) for Hewlett-Packard's line of switches, detectors, and fixed and step attenuators. Intended for system design engineers and microwave product designers, the publication includes such products as the new HP 33314 SPDT coaxial switch, which is specified for a life of 5 million cycles with better than 0.03-dB repeatability. The company's 11-, 70-, and 90-dB step attenuators with ranges to 40 GHz are also included as are several families of coaxial detectors.

*Hewlett-Packard Co., Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900 or call local sales office.* **CIRCLE 355**

## DEVELOPMENT GUIDE TARGETS STD BUS

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*Computer Dynamics Sales, 107 S. Main St., Greer, SC 29650; (803) 877-8700.* **CIRCLE 356**



## UPCOMING MEETINGS

### JANUARY

**International Winter Consumer Electronics Show (CES), January 6-9, 1990.** Mirage Hotel, Las Vegas, NV. Cynthia Saraniti, Electronic Industries Association/Consumer Electronics Group, 1722 Eye St., N. W., Ste. 200, Washington, DC 20006; (202) 457-8700.

**ATE & Instrumentation West, January 9-11, 1990.** Disneyland Hotel Convention Center, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-3976 or (800) 223-7126.

**VXIbus User Group Meeting, January 10, 1990.** Disneyland Hotel, Anaheim, CA. Sandy Garza, National Instruments, 12109 Technology Blvd., Austin, TX 78727-6204; (512) 794-0100 or (800) 433-3488.

**SMART VI (Surface Mount and Advanced Related Technologies) Conference and Exhibition, January 15-18, 1990.** Buena Vista Palace, Orlando-Lake Buena Vista, FL. EIA Components Group, 1722 Eye St., N. W., Ste. 300, Washington, DC 20006; (202) 457-4930.

**Fifth Annual Battery Conference '90, January 16-18, 1990.** California State University, Long Beach, CA. Julie Allison, Dept. of Electrical Engineering, California State University, 1250 Bellflower Blvd., Long Beach, CA 90840; (213) 985-4605.

**Network Management Conference, January 24-26, 1990.** Innisbrook Resort, Tarpon Springs, FL. Frost & Sullivan Inc., 106 Fulton St., New York, NY 10038-2786; (212) 233-1080.

**SEMICON/Southwest 90, January 31-February 1, 1990.** The Infomart, Dallas, TX. Lisa Anderson, Semiconductor Equipment and Materials, 805 East Middlefield Rd., Mountain View, CA 94043; (415) 964-5111.

### FEBRUARY

**International Tape Automated Bonding (TAB) Symposium, February 5-7, 1990.** Red Lion Inn, San Jose, CA. Courtney Miller, Texas In-

struments, 8315 LBJ Freeway, P.O. Box 225474, TX 75265; (214) 997-3952.

**Application Technology Conference, February 12-15, 1990.** San Jose Convention Center, San Jose, CA. Ed Teja, Systems/USA Technical Conference, AEA, 5201 Great America Pkwy., Santa Clara, CA 95054; (503) 231-9914.

**NetWorld 90 Boston, February 12-15, 1990.** Hynes Convention Center, Boston, MA. Ann Scully, NetWorld, 385 Sylvan Ave., Englewood Cliffs, NJ 07632; (201) 569-8542.

**Buscon '90 West, February 13-16, 1990.** Long Beach Convention Center, Long Beach, CA. Sharon Green, Conference Management Corp., 200 Connecticut Ave., Norwalk, CT 06856-4990; (203) 852-0500, ext. 247.

**Power Electronics Conference, February 13-16, 1990.** Long Beach Convention Center, Long Beach, CA. For more info call (203) 852-0500.

**International Solid State Circuits Conference (ISSCC), February 14-16, 1990.** San Francisco Hilton, San Francisco, CA. For more info call (202) 347-5900.

**National Electronic Packaging and Production Conference (NEPCON) West '90, February 26-March 1, 1990.** Anaheim Convention Center, Anaheim, CA. Janet Schafer, Cahners Exposition Group, 1350 E. Touhy Ave., Des Plaines, IL 60017-5060; (312) 299-9311.

**Compcon Spring 90, February 26-March 2, 1990.** Cathedral Hill Hotel, San Francisco, CA. Dr. Kenichi Miura, Fujitsu America, 3055 Orchard Dr., San Jose, CA 95134; (408) 432-1300 ext. 5408.

**Third International Software for Strategic Systems Conference, February 27-28, 1990.** Von Braun Civic Center, Huntsville, AL. Carolyn Freeman, Conferences & Marketing, The University of Alabama in Huntsville, Huntsville, AL 35899; (205) 895-6372 or (800) 448-4035.

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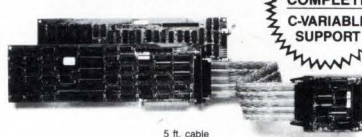
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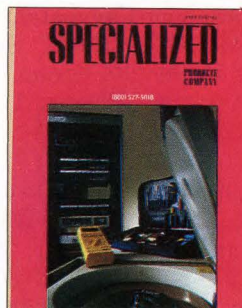
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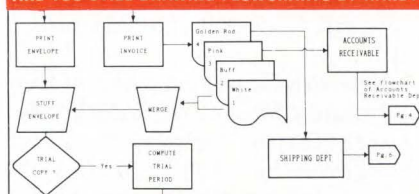
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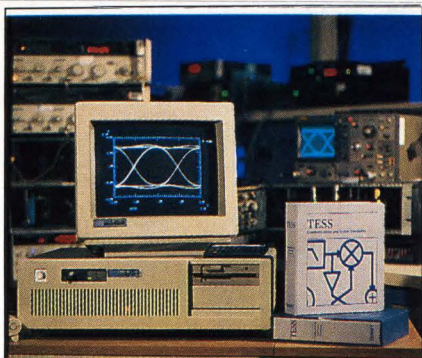
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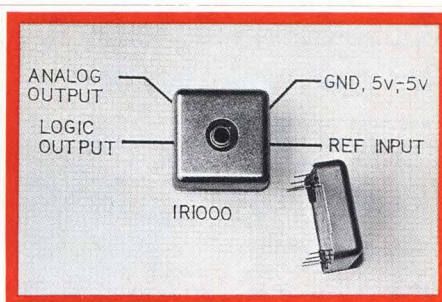
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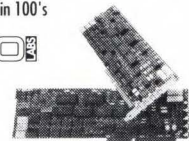
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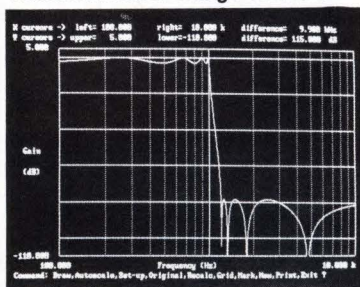
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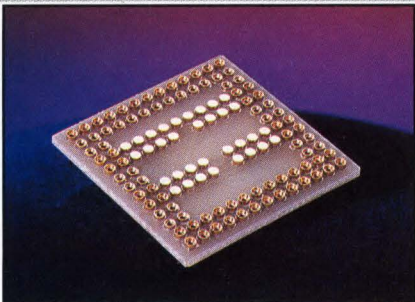
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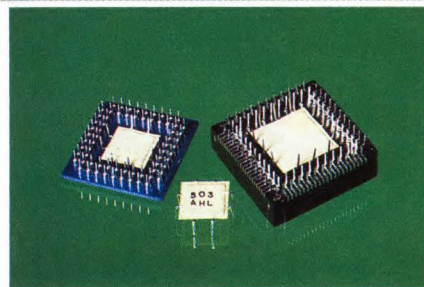
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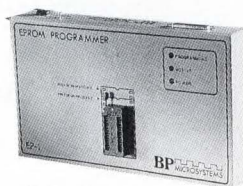
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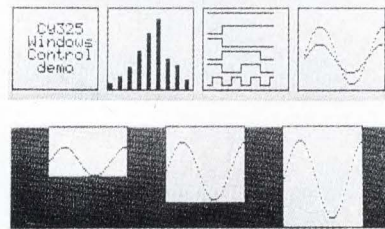
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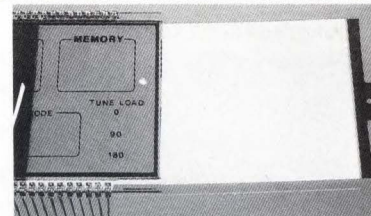


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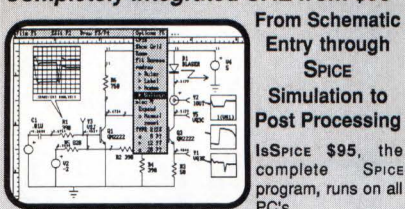
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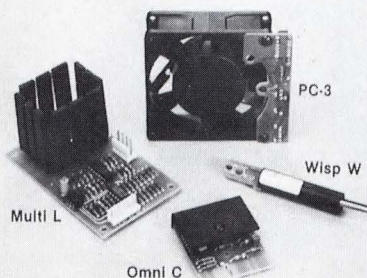
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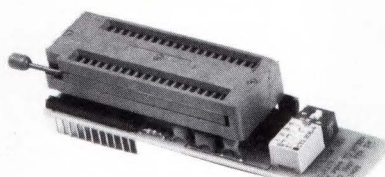


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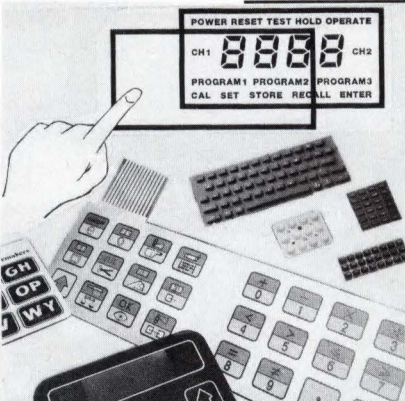
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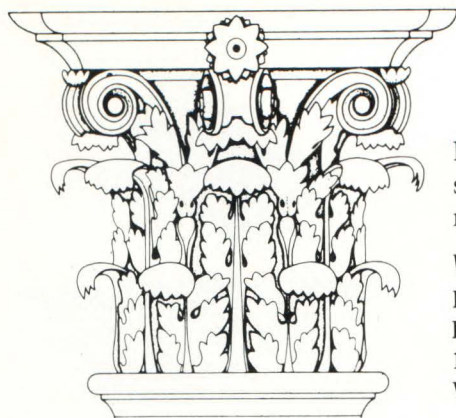
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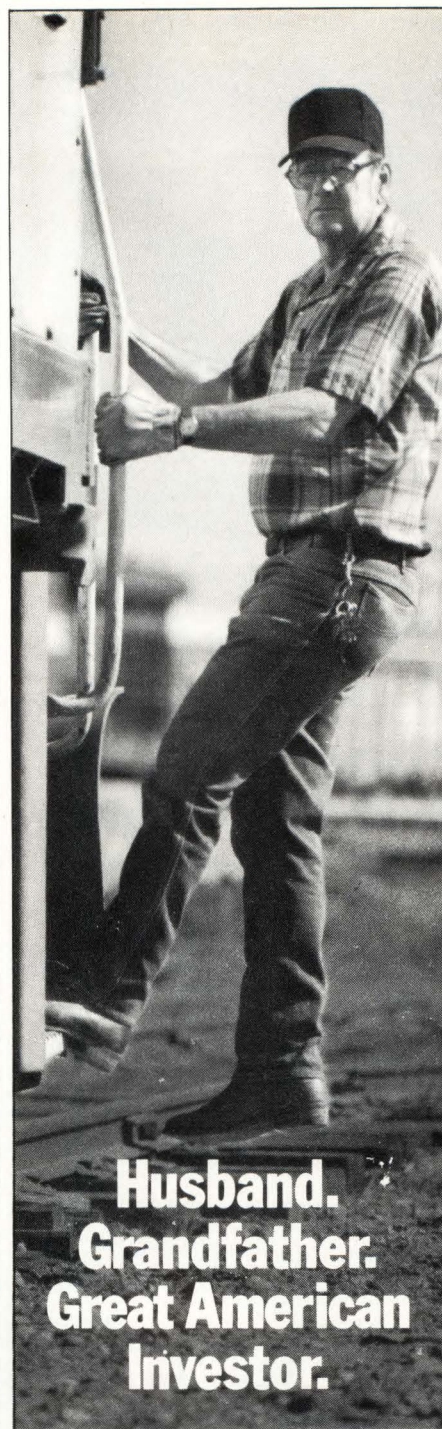
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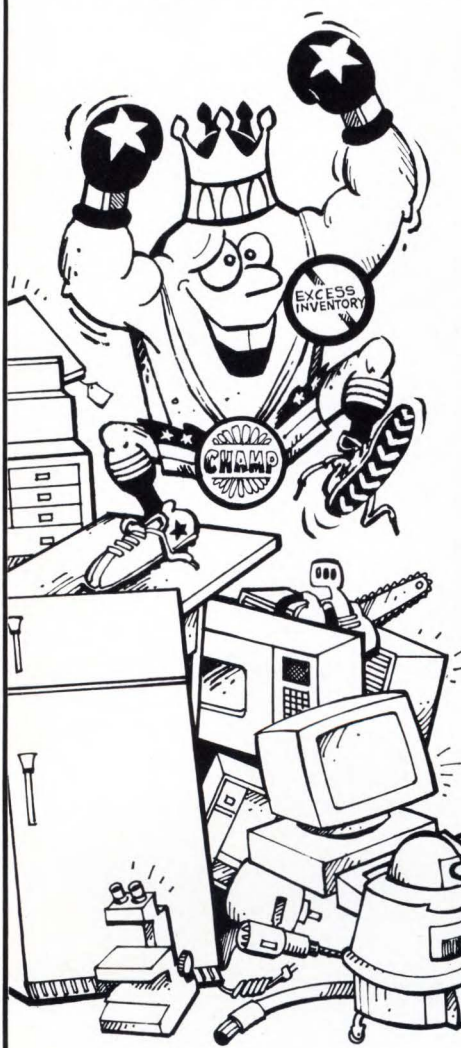
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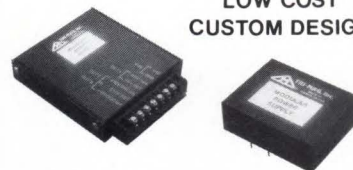
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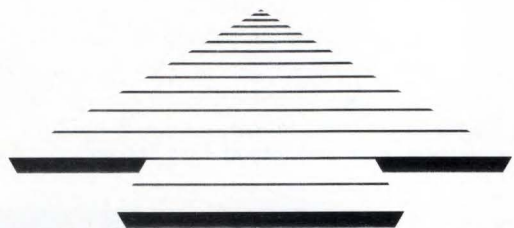
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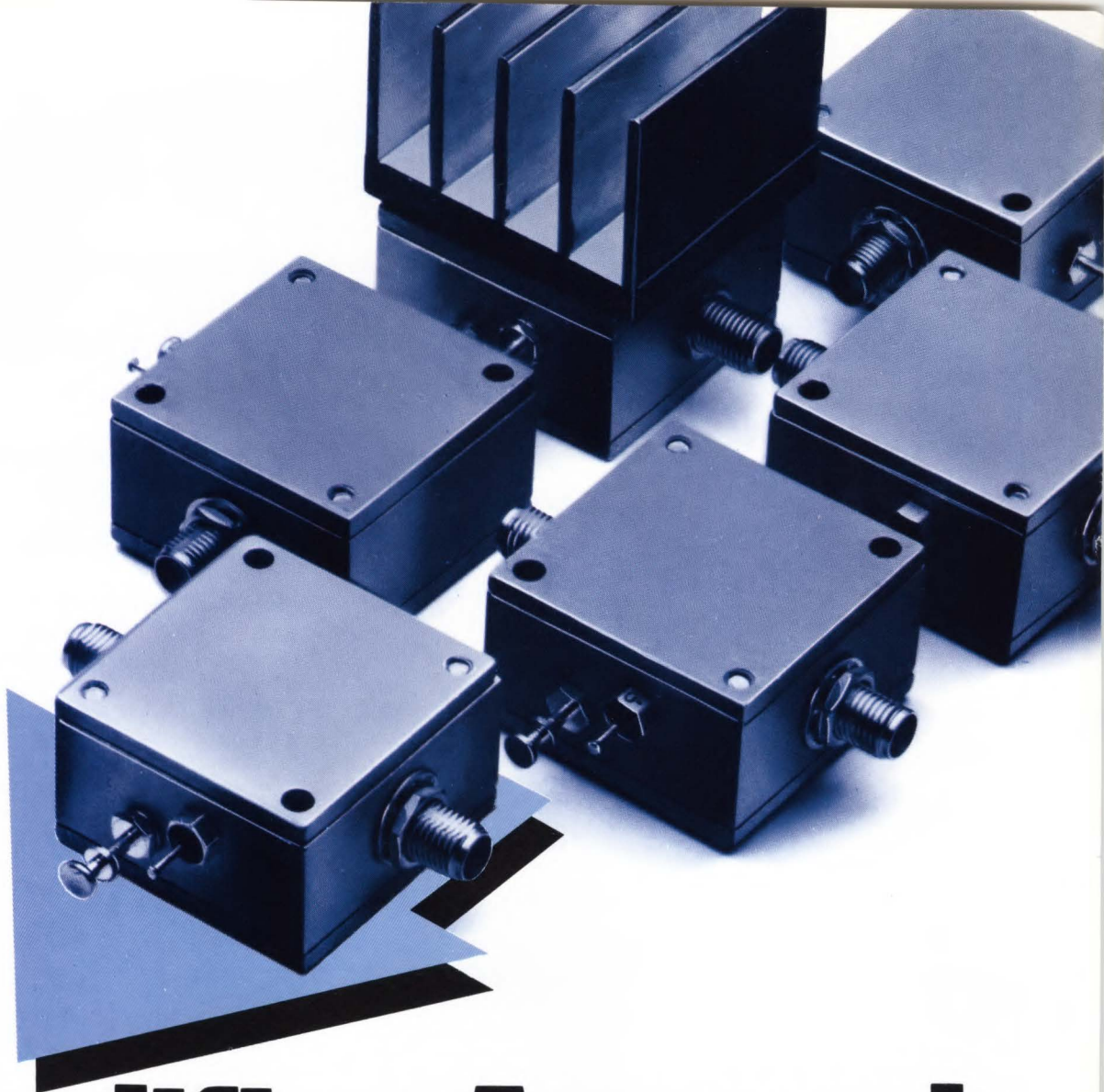
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**Fact: Scalable High Performance.** Operating from 25MHz to 40MHz, and offering 18 to 29 MIPS, this chipset demonstrates the scalability of the SPARC™ RISC architecture. That scalability has already produced high performance SPARC implementations in CMOS, ECL, and GaAs. This scalability enables high performance, binary compatible systems all the way from low-cost desktops to mainframe-class systems — consistent with the trend toward networked computing. This new chipset will enable new performance standards in desktop and workstation/server systems.

**Fact: Shrink Wrapped Applications.** SPARC is the only RISC architecture that is truly open, with available, binary-compatible clones. The shrink-wrapped UNIX® applications base — including the leading database, publishing, office and engineering packages — is larger than for ALL of the other RISC architectures combined. And with major new support announcements from Lotus, Santa Cruz Operations (SCO), and Wordperfect, expect significant new applications. Applications drive the industry's next computing standard.

**Fact: Complete Solution.** This chipset you see, designed by Ross Technology, a Cypress subsidiary, is available today. It includes the Integer Unit, Floating Point Unit, Cache Controller/Memory Management Unit, and 256K Cache RAMs.

**Fact: Proven Support.** SPARC runs UNIX. It runs the major windowing systems — NEWS™ and X-Windows™. It supports the AT&T OPEN Look user interface. SPARC-based development systems are available now, with a full complement of development tools, compilers, debuggers, documentation packages, and utilities.

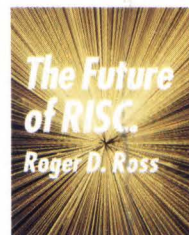
**Fact: The Leaders.** The system companies that support SPARC — AT&T, Sun, Toshiba, Solbourne, ARIX, Philips, and ICL, to name a few — are moving faster toward the industry's next computing standard than are the supporters of any other RISC architecture.

**Call today for this important article:**  
**1-800-952-6300\* Dept. C32.**



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