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THE ART OF DEBUGGING PARALLEL COMPUTERS

ELECTRONIC DESIGN

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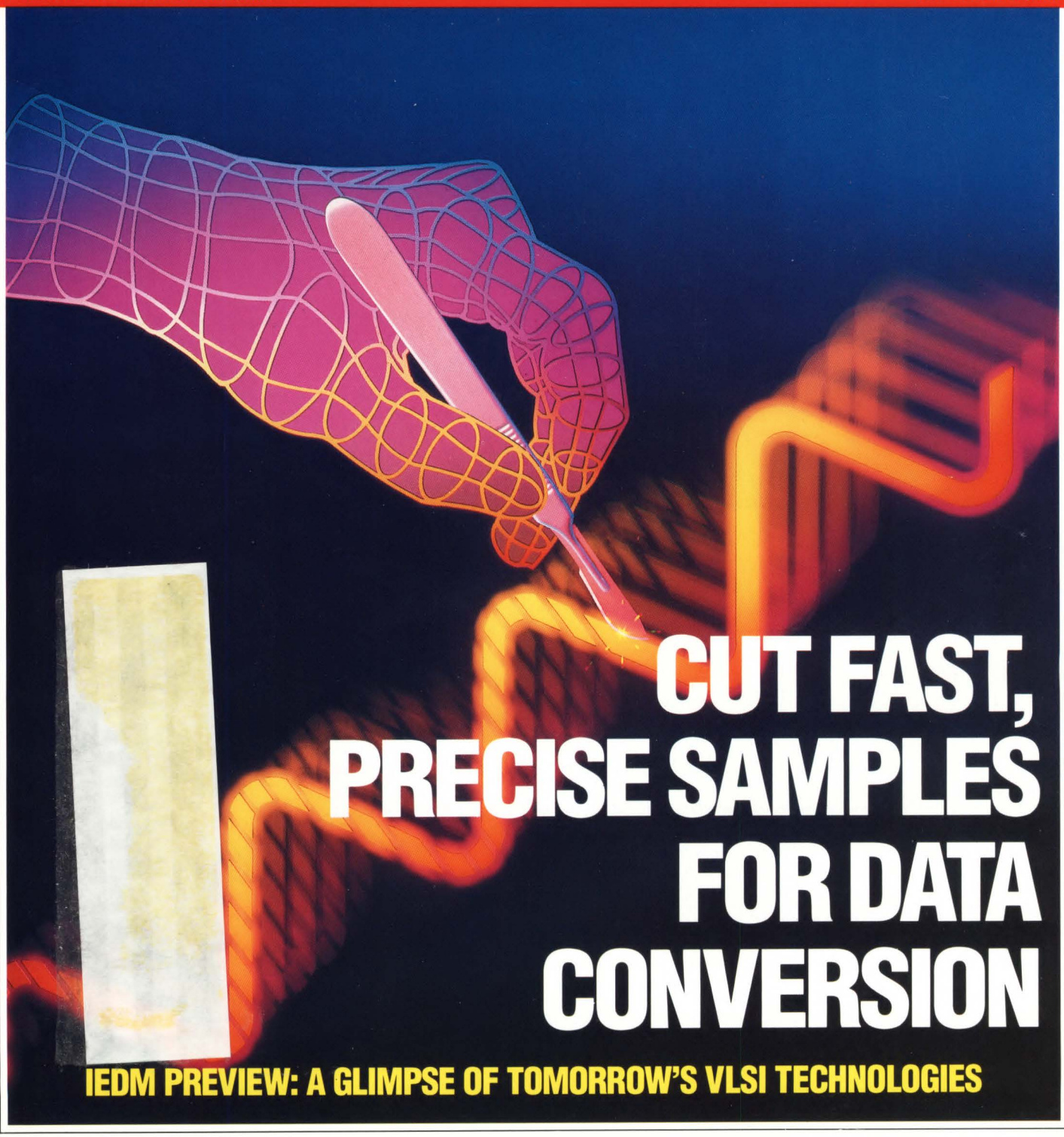
NOVEMBER 23, 1989



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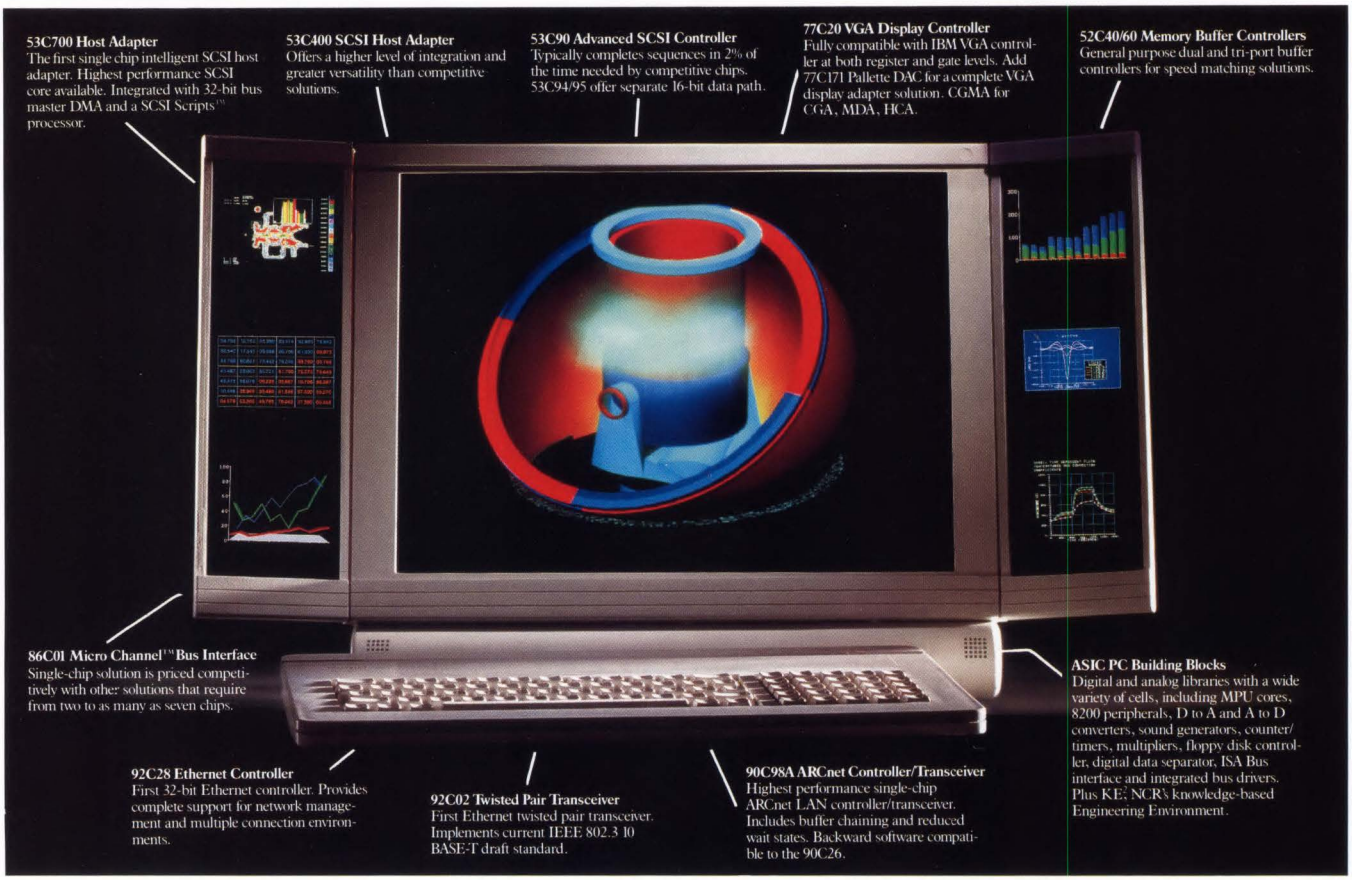

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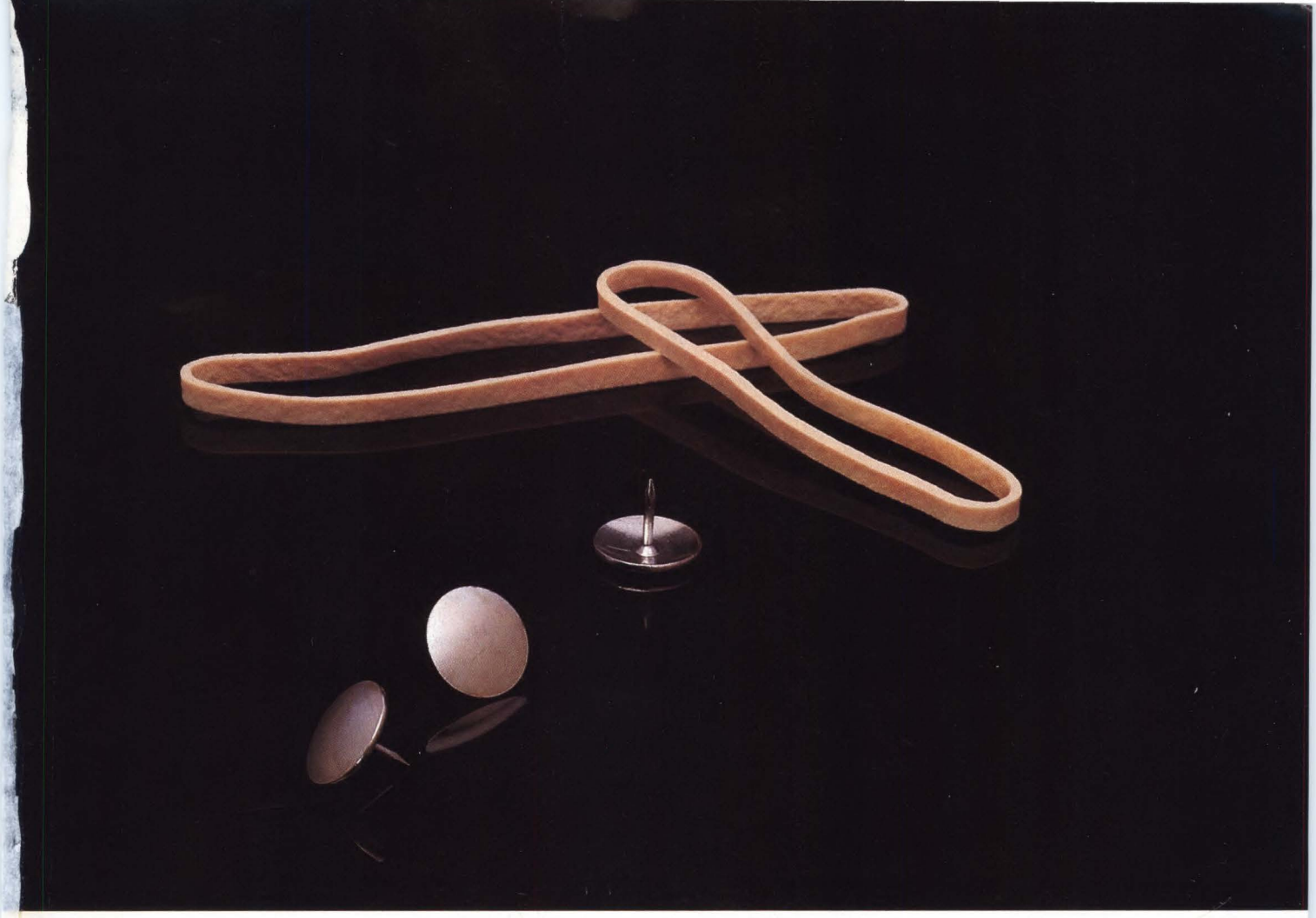
Creating value

CIRCLE 25



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	KM6465L	16K x 4	25/35/45ns	SDIP
	KM6865	8K x 8	35/45/55ns	SDIP
	KM6865L	8K x 8	35/45/55ns	SDIP
256K	KM61257	256K x 1	25/35/45ns	SDIP/SOJ
	KM61257L	256K x 1	25/35/45ns	SDIP/SOJ
	KM64257	64K x 4	25/35/45ns	SDIP/SOJ
	KM64257L	64K x 4	25/35/45ns	SDIP/SOJ
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CIRCLE 47

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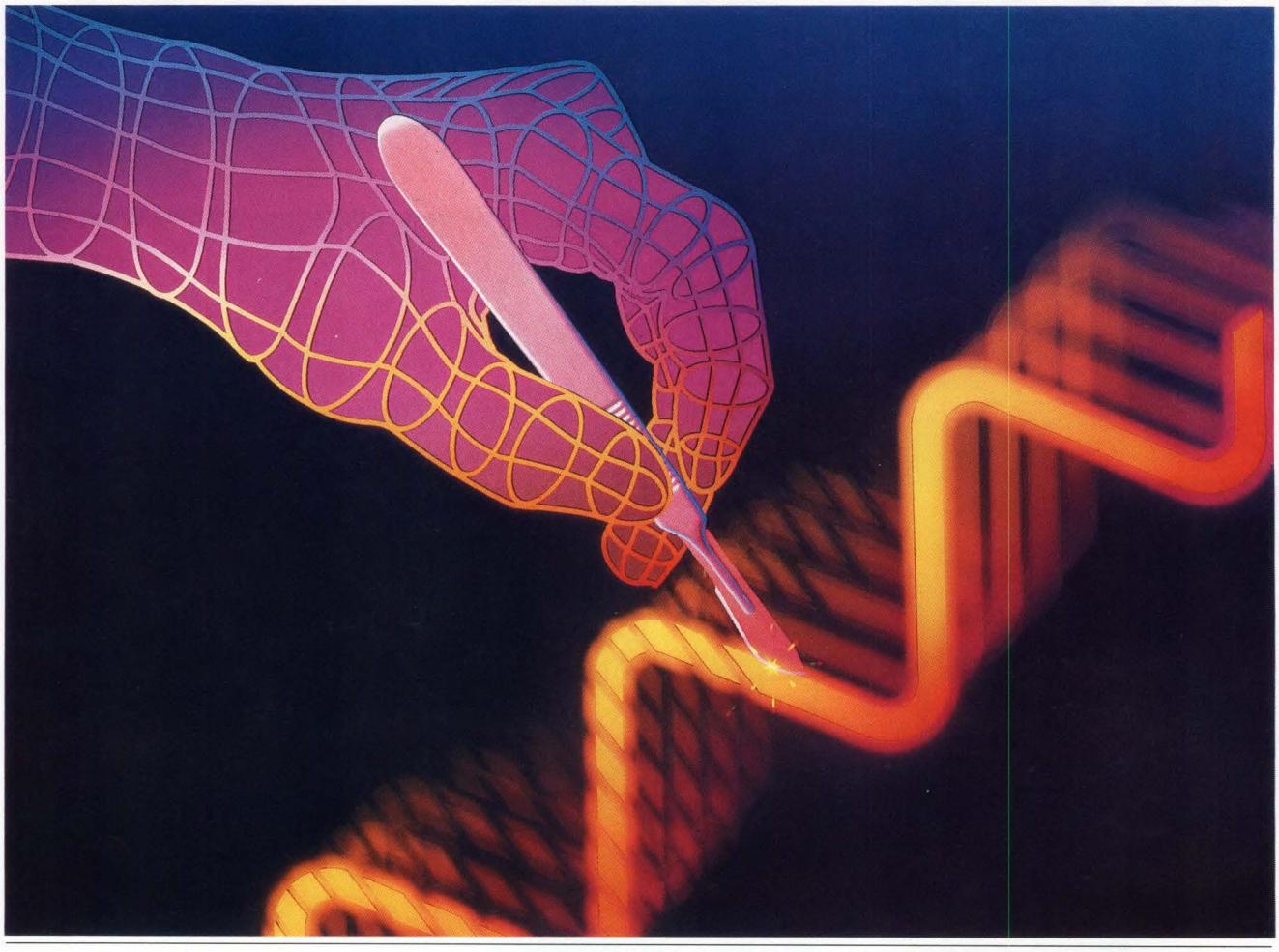
NOVEMBER 23, 1989 VOL. 37, NO. 24

ELECTRONIC DESIGN



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- An analysis of bus-interface logic devices for high-speed systems.
- Design details on Compaq's 386/486 EISA personal-computer system and supporting plug-in pc-board and software products.
- A surface-mounted connector that operates into the gigahertz range.
- Tips on writing software for the SCSI-2 Wide Bus.
- Design details on the specifications for the Fiber Distributed Data Interface (FDDI).
- Designing high-resolution monitors.

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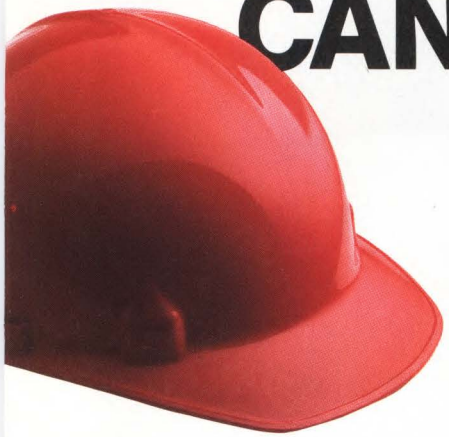

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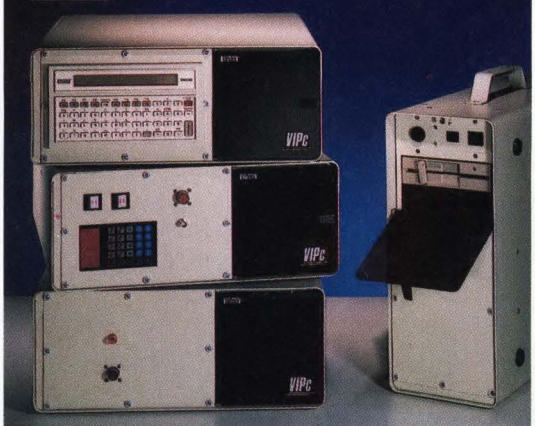

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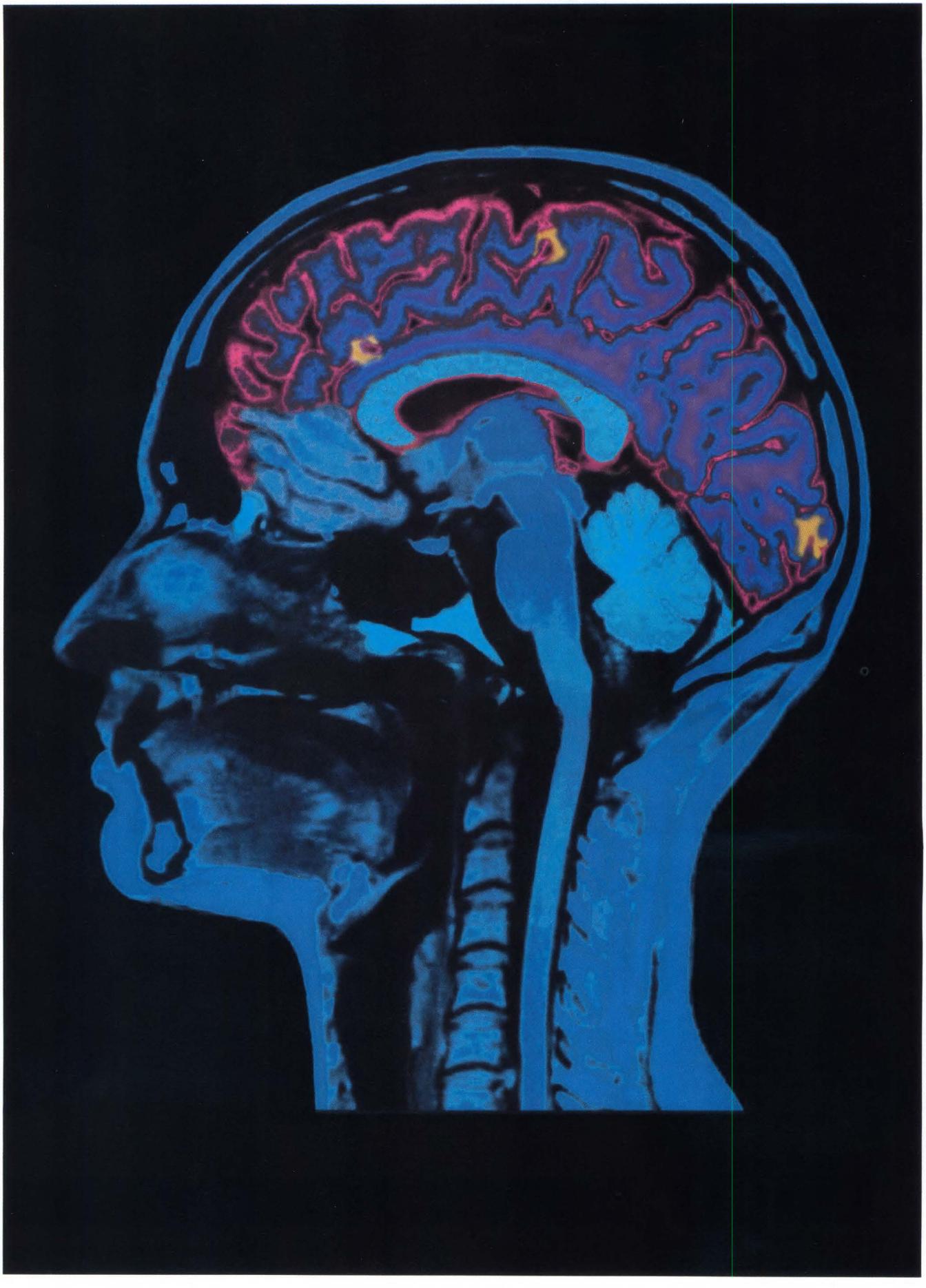

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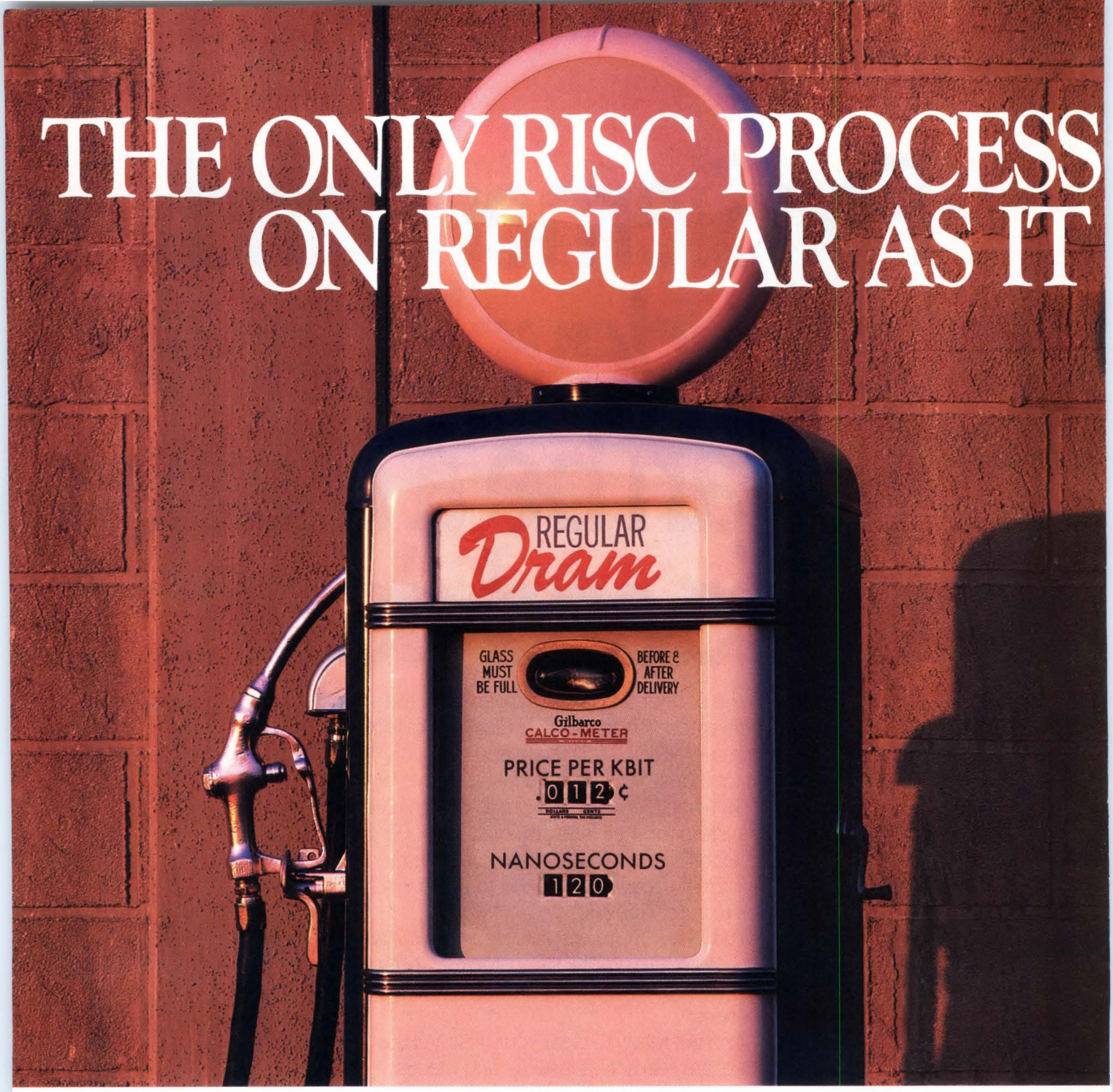

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CIRCLE 49

PUTTING SCIENCE AND TECHNOLOGY FIRST

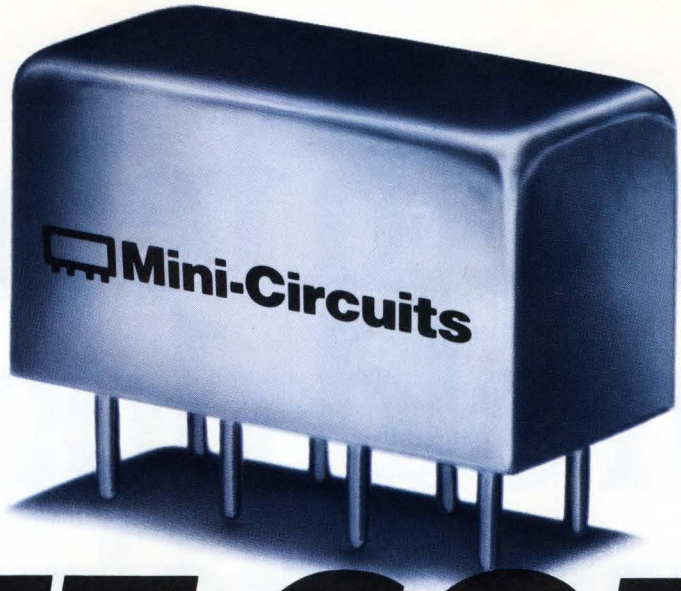
Speaking last month in New York City, Larry W. Sumney, president of Semiconductor Research Corp. and former head of the U.S. Department of Defense's VHSIC program, called for a new Cabinet-level department within the federal government: a Department of Industrial Science and Technology. Addressing the IEEE's Annual Briefing for the Media, Sumney said this department would need at least $10 billion annually. The funds would be used to double U.S. support of generic science and technology in critical technologies; to fund commercially oriented technology development in cooperation with industry; and to provide industry with zero-interest loans for the creation of new production facilities.

We hesitate to suggest more bureaucracy in Washington, D.C., but we do think that such a Cabinet post is worth serious consideration. For too long, support for science and technology has been scattered among many government departments and it's time to unite government support for this critical area. The fact that most departments have some responsibility for science and technology indicates the need for a single department to focus all government energies.

Science and technology has been a poor cousin within the Department of Commerce. Although Presidents have had science and technology advisers, these people have carried little clout within government. Compare the importance of science and technology with, say, agriculture: Despite the Department of Agriculture's importance to the country, its concerns are clearly outweighed by science and technology in today's world.

We would even suggest that support for undergraduate and graduate-level technical education be placed within this proposed department, which could presumably be staffed by people who really understand the problems of our engineering schools. And, given the sorry state of science education in our primary schools, it wouldn't be too much to ask of this proposed department to help stimulate scientific interest among our school-age children—the very spot where this nation's competitive edge will grow or die.

Stephen E. Scrupski
Editor-in-Chief



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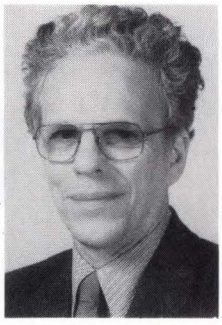
CIRCLE 37

ANALOG CAE GAINS POTENT TRAITS



FRANK GOODENOUGH
ANALOG & POWER EDITOR

Long the stepchild of the digital world, analog CAE for linear system or chip design continues to be bolstered by new tools. These tools are not only easier to use, but they also offer previously unavailable—even exotic—capabilities. Such packages are needed for straight analog designs, as well as for the growing number of systems that mix analog and digital.

In many ways, analog design is more of an art than digital design: It's more intuitive and heuristic. Many statistics highlight a significant trend: On the one hand, there's a growing shortage of *skilled* analog designers; on the other hand, there has been a rapid growth of systems—and now ASICs—containing some analog circuitry. Such companies as IMP, NCR, and Sierra have cited the fact that 20–40% of all digital designs now contain some analog circuitry; the analog portion runs from under 5% to over 80%, with most about 20%.

The only way to get enough designers for such chips is to put smart, easy-to-use tools in the hands of novice analog designers—be they experienced digital people or recent graduates. Add this to the fact that digital clock rates now exceed 50 MHz. Consequently, digital-system and chip designers are also beginning to run into analog-type design problems.

Three recent analog-design software packages attack three key aspects of the analog design problem: Cadence, Santa Clara, Calif., offers a chip-design system complete from hierarchical schematic capture and simulation to layout and back annotation; Silicon Compiler Systems, San Jose, Calif., has an analog IC-design tool that can synthesize such circuits as op amps and references; and Intergraph, San Ramon, Calif., is introducing a waveform editor that can interface a Spice simulator with real-world signals.

Cadence's Artist is the first product from the company's fledgling Analog Division, which is under the aegis of ex-linear-IC designer Jim Solomon. With Artist, designers can capture the complete chip schematic—with each subcircuit entered at any level in a hierarchy, ranging from transistor, macro and behavioral models, to simple (or complex) equations. Once captured, the circuit is simulated in Cadence Spice, or HSpice, in a true interactive mode, with features such as restart from a previous simulation and post-simulation voltage probing. Artist's post-simulation processing and graphics system displays results in linear or logarithmic formats, algebraically combines and plots waveforms, and overlays the results of multiple simulations. Node voltages and operating points can be annotated. Following successful simulation, designers move to layout via the Cadence Design Framework, and then to design-rule checks, verification, back annotation, and resimulation.

Explorer AutoFilter and Explorer AutoLinear, from Silicon Compiler Systems, represent the first commercially available suite of circuit and layout-synthesis tools for analog and mixed-analog-digital IC design. With these tools, designers define a required circuit type and performance, and then the tools come up with a recommended circuit and layout, requiring minimum silicon area. If it's an op amp, designers can choose from a number of topologies to start with, and potentially cut the "expert system's" compute time; if the designer is less experienced, the tool can do it all. The tool will be extremely useful to IC suppliers to make those minor, but labor-intensive, cell modifications needed by virtually every customer.

The Intergraph Analog Waveform Editor (AWE) puts simulator waveform creation in the hands of the system designer when used with Intergraph's Analog Engineer Series. The series is a sophisticated schematic capture, simulation, and analysis system with graphics that are second to none. With the AWE, designers employ real-world signals from a signal generator (via IEEE-488) or even from hardware as the simulator's input.

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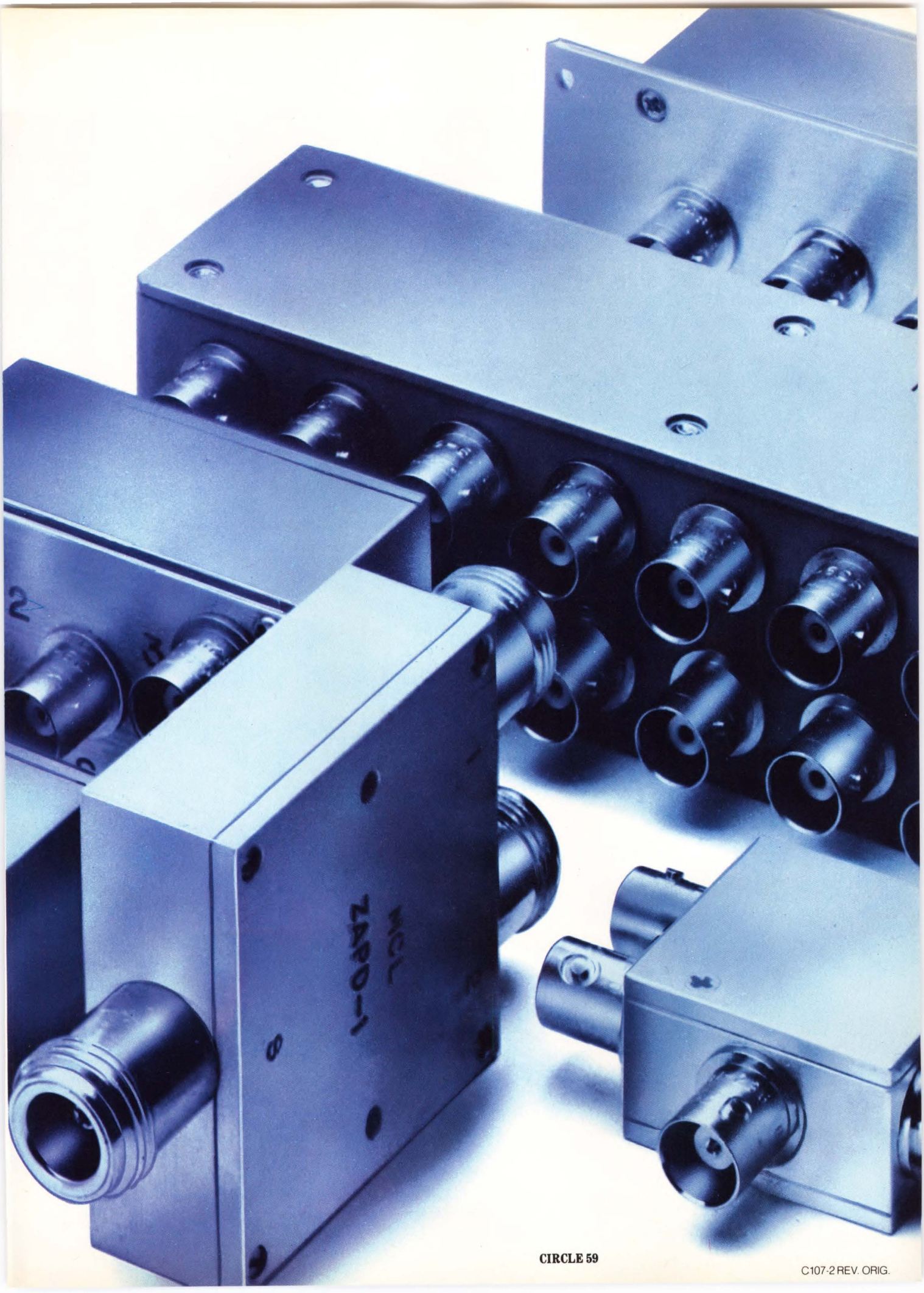

CIRCLE 59

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Thanks to its advanced bus interface and its on-chip caches, the 32GX32 is able to sustain most of its performance while using slower, inexpensive DRAMs. This fact alone has a tremendous impact on the system cost of today's printers, which typically require large amounts of memory.

The 32GX32 performs single-cycle operations on information contained in on-chip instruction and data caches. The data cache organization can accommodate both a stack *and* a scratch pad for high-speed font generation. These factors minimize the effect of low-cost, slow external memory on system performance.

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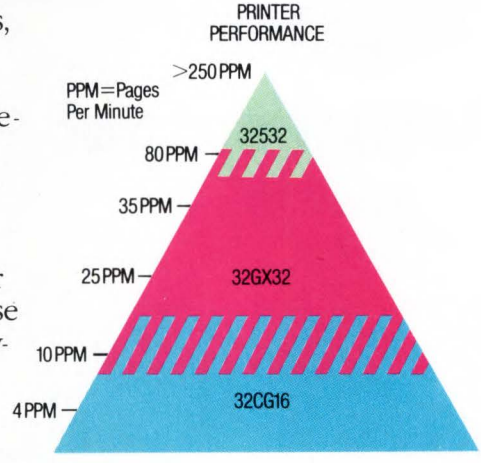

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CIRCLE 51

VXIbus Standard Gets Midcourse Corrections

The VXIbus Consortium has added several electrical and mechanical specifications to the document that defines the VXIbus open architecture for modular instruments. Revision 1.3 also removes the section on shared memory protocols from the main document. Those protocols are being revised and will be published separately. Reorganized as a nonprofit corporation, the consortium enhanced the rules for ECL-trigger drivers to prevent possible glitches. It also established different separation distances for shielded and unshielded modules. The revision defines backplane connector-shield dimensions and augments the rules for backplane jumpering of empty slots. Based on the VMEbus standard, VXIbus allows modules from different manufacturers to operate within one mainframe chassis. JN

Access Hooks Ease Emulation Hassles

Microcontroller manufacturers are accustomed to building special, costly bond-out or piggyback versions of their devices to develop emulation tools. In a technology agreement with MetaLink Corp., Chandler, Ariz., Philips Components-Signetics, Sunnyvale, Calif., will solely license a MetaLink technology that eliminates the need for these special chips. Called emulation hooks, the technology is embedded in the microcontroller itself and makes it possible to directly access a microcontroller's internal program memory. It is initially targeted for use in Philips Components-Signetics' line of 80C51 derivatives. Now Signetics can commit itself to IC development without having to divert resources to developing related bond-out versions of its microcontroller products. DM

X-Ray Lithography Finds Heightened Interest

As if to retaliate against the deal struck between Motorola and IBM to co-develop advanced X-ray lithography, AT&T Bell Laboratories, Murray Hill, N.J., has inked a collaboration agreement with Hampshire Instruments Inc., Marlborough, Mass. to develop production X-ray lithography systems that can produce transistors with feature sizes between 0.5 and 0.25 μm. The deal encompasses three aspects of development: X-ray optics, reticle technology, and X-ray resists for coating the wafer. Hampshire Instruments already sells an X-ray stepper and has initially settled on an electron-beam lithography system for generating the reticle. The X-ray system that the company now offers, the Series 5000, is already used by other companies, including Sanders Associates, Nashua, N.H., which employs the system to build gallium-arsenide monolithic microwave ICs under a U.S. government Darpa contract. DB

Plasma Display Panel Cuts Power Drain

Although displays like gas-plasma flat panels, which emit their own light, are easier on the eyes and faster to respond than liquid-crystal panels, their high power drain precludes their use in most battery-powered computers. However, by going to a novel current-source driver circuit, improving the efficiency of the discharge circuit, and creating a novel trigger electrode structure, designers at Toshiba Corp., Tokyo, were able to cut overall plasma display power to a third or fourth that of conventional plasma panels with VGA resolution. Two side benefits also resulted from the new internal structures: First, because the trigger electrode is quick, it limits the light wasted by auxiliary discharge to only about 1%, thus improving the contrast ratio of the display sixfold, to 100:1. Second, the more efficient display consumes less power, reducing the power-supply size and weight, and contributing to smaller and lighter systems. Samples of the display panels will be available through the Toshiba America Information Systems Inc., Irvine, Calif. DB

Compiler Enhancements Boost ASICs' Speed

Designers using one company's logic synthesis tools can now put faster state machines into their ASICs. In addition, they can improve the timing performance of synthesized circuits. With version 1.2 of Design Compiler from Synopsys Co., Mountain View, Calif., designers can produce ASICs that are 8% faster than those produced with the previous version. State-machine speed is a function of gate optimization and state assignment. The state-assignment algorithm in the Synopsys compiler analyzes the specified state machine and automatically chooses an optimized state assignment. With the new compiler, designers can also explore the implementation of a state machine interactively by varying the number of bits encoded from the minimum possible (for area efficiency) to one per state (for maximum speed). Designers can also evaluate the effects of different types of flip-flops on the state-machine implementation. LG

EISA Systems Get Data-Acquisition Card

The myriad of extended industry standard architecture (EISA) systems just released at this month's Comdex show face a dearth of specially designed add-in cards that can exploit the enhanced bus structure. One of the first cards to add instrumentation capabilities to EISA-based systems will come from National Instruments Corp., Austin, Texas. Under a DMA burst mode, the card can move data at 16.5 Mbytes/s, about ten times faster than PC/AT-bus based systems. The EISA-A2000 card is a complete four-channel 12-bit data-acquisition subsystem that takes up to 1 Msample/s. Because data can be transferred quickly, the subsystem was designed with a sample-and-hold front end on each channel. Consequently, all four channels can take samples simultaneously. The board also contains a proprietary local bus to route timing and trigger signals among multiple data-acquisition boards. Controlling the card are various software packages that supply set-up and calibration utilities, board programming, and oscilloscope emulation so that the captured signals can be displayed on the PC's screen. DB

Merged Process Adds EEPROM To Mixed ASIC

A process that mixes analog, digital, and electrically erasable memory on one chip will let designers re-use older circuits built in p-wells on an n-type substrate. Other mixed processes often use the reverse: n-wells on a p substrate. As a result, many older circuits must be redesigned before the EEPROM cells can be added. However, this novel mixed-technology process from Gould AMI, Pocotello, Idaho, will make it possible for designers to enhance previously designed circuits with EEPROM cells or blocks. The process also gives circuit designers the option to use intrinsic bipolar devices that have uncommitted collectors. Though the bipolar transistors have only a moderate cutoff frequency of 300 MHz, they also have high gains—typically between 300 and 500—and can tackle a wide range of applications. For EEPROM-based designs that take about the same area as chips that don't have an EEPROM on board, the company estimates that the chips with electrically erasable cells will sell for 12% to 15% more than a plain chip. DB

Speedy Logic Simulator Attracts CAD Partners

The latest in a flurry of strategic alliances among CAD software vendors revolves about a real-time, PC-based logic simulator from Aldec, Newbury Park, Calif. Called Susie (standard universal simulator for improved engineering), the CAD tool has a 40,000-gate capacity and performs simulations at 2 million gates/s on a 25-MHz 386-based computer. An optional companion package, called Tim (timing interactive module) provides 10-ps timing resolution. In a business partnership with Aldec, Cadam's P-CAD division, San Jose, Calif., will include Susie with Tim as a subset of its Digital Design Lab CAD software. A similar agreement with the Racal-Redac Group, Westford, Mass., will add Susie to Racal-Redac's Cadstar suite of circuit-board CAD tools. The addition will make it possible for designers to interactively simulate circuits produced on the Cadstar Schematics package. A third agreement with Wacom Co., Ltd., Tokyo, will include Susie with Zycad's MACH1000, IKOS's S800, and GenRad's HILO-3 simulators as optional adjuncts to Wacom's E-CAD/gate CAD package for gate-array design. ML

Improved ALU Macro Doubles Data-Path Speed

A new ALU architecture added to a data-path compiler gives CMOS ASIC designs faster data-paths. The speed increase comes from a modified conditional-sum algorithm in the ALU's carry chain that avoids large fan-outs and fan-ins typical of carry-look-ahead schemes. The modified architecture doubles the performance over similar ALUs employing other carry-propagation algorithms. The data-path compiler, from VLSI Technology Inc., San Jose, Calif., generates ALUs with n-bit widths, ranging from 4 to 72 bits. Typical speeds are 9 ns for a 32-bit width, 12 ns for a 64-bit width, and 14 ns for a 72-bit width. In conventional ALUs, delays are proportional to the bus width. With the modified architecture, however, the delays are proportional to the logarithm of the width. To incorporate the ALU into an ASIC, designers need only specify the bit-width, and the compiler automatically generates the ALU circuitry within the data-path. LG

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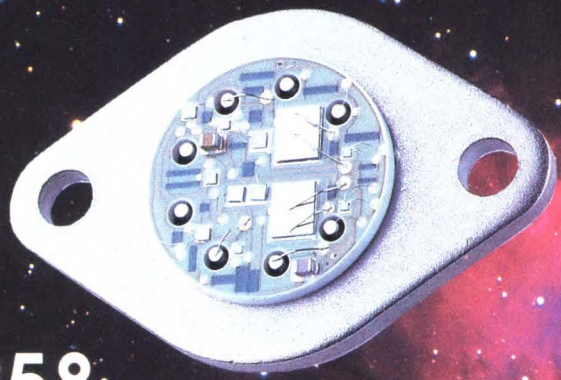

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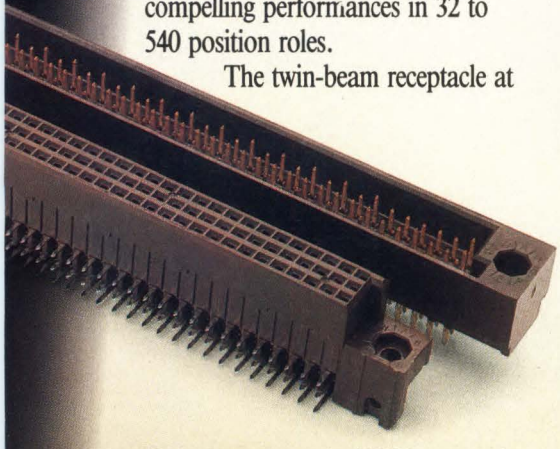

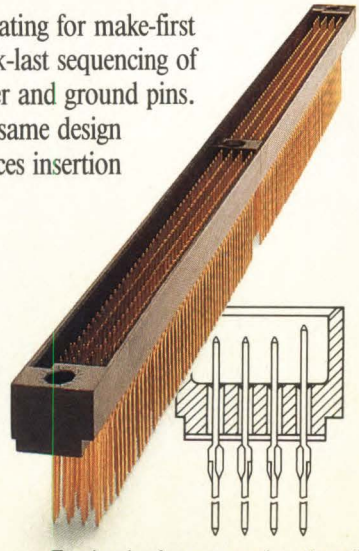

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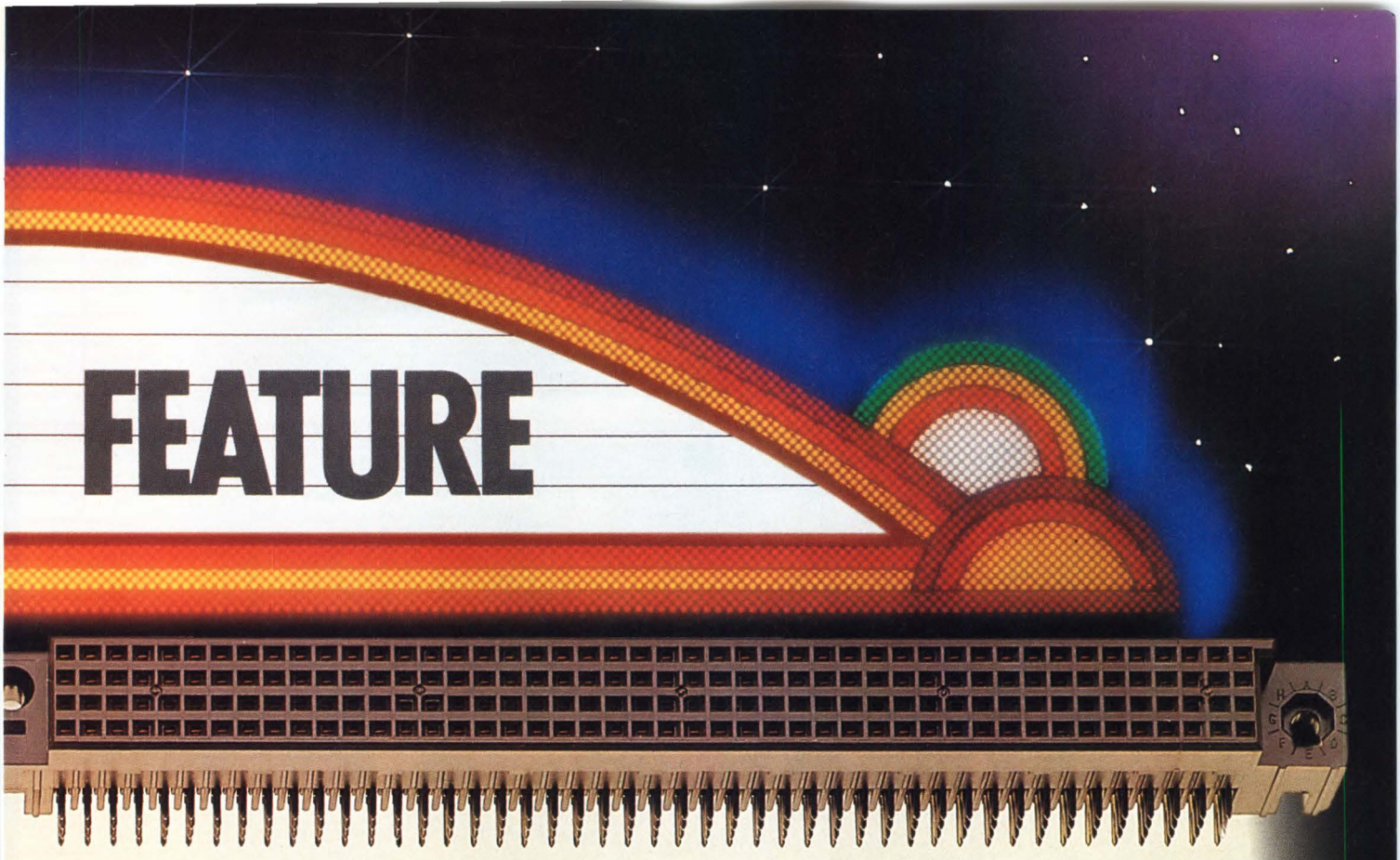

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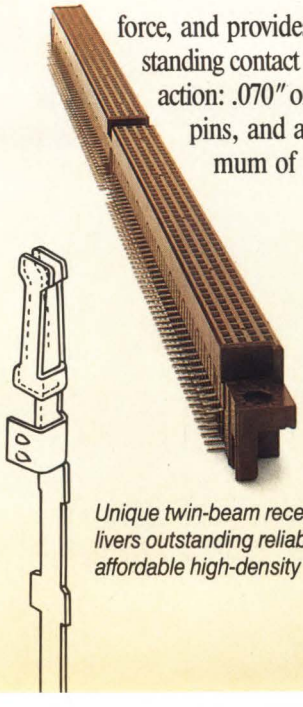

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AMP Interconnecting ideas

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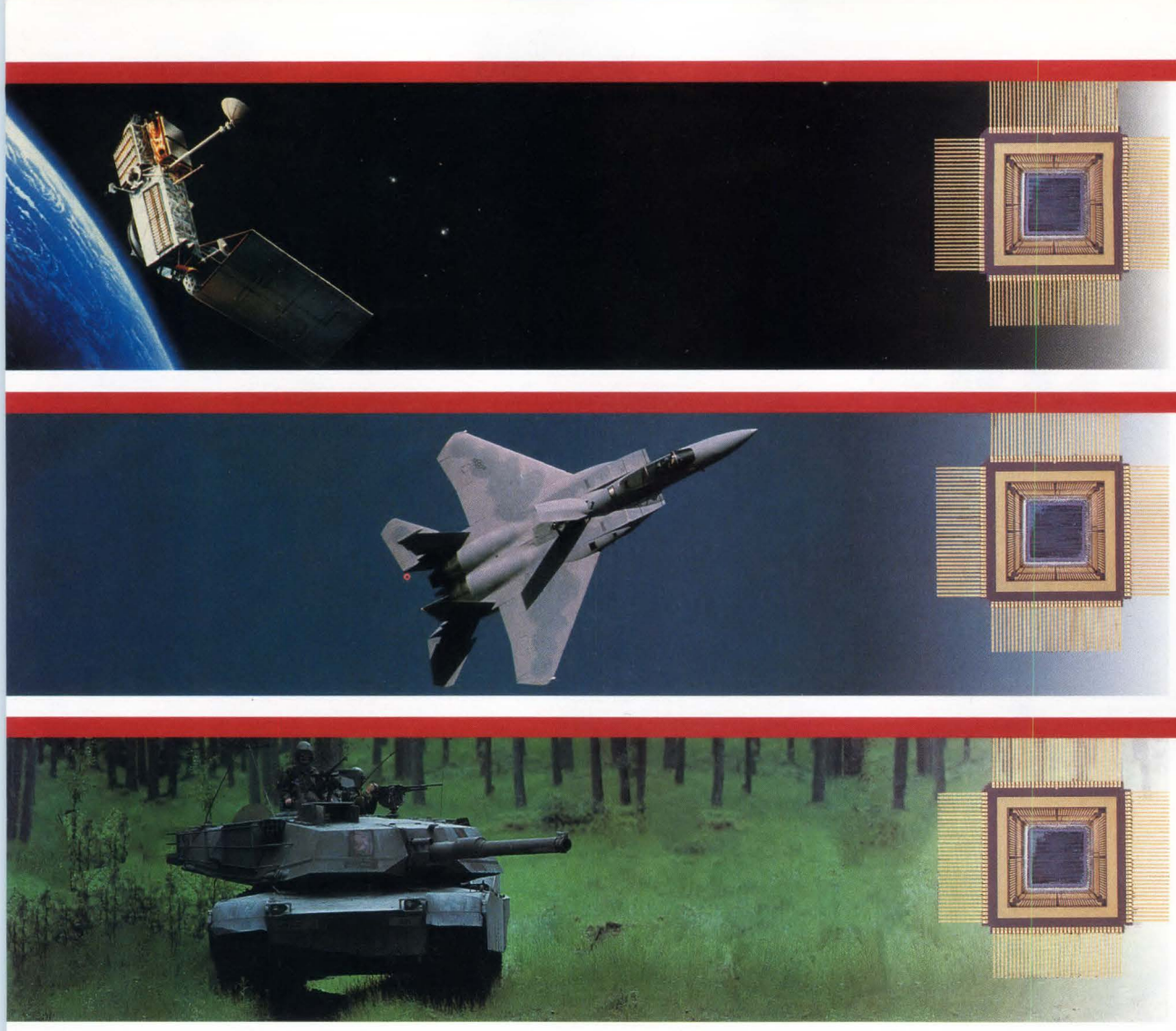

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CIRCLE 41

CMOS PROCESS BREAKS "BIRD'S BEAK" BARRIER

When transistors shrink to submicron size, it's the isolation distances between them, rather than their size, that limits circuit density. To break that limit, an advanced process developed by NCR Corp., Colorado Springs, Colo., replaces conventional local oxidation (Locos) isolation with a recessed sealed sidewall field oxidation (Ressfox).

The result is a tighter packing of CMOS circuits, because Ressfox eliminates oxide intrusion into a transistor's active regions. The intrusion is commonly referred to as the bird's beak problem because the shape resembles the side view of a bird's beak.

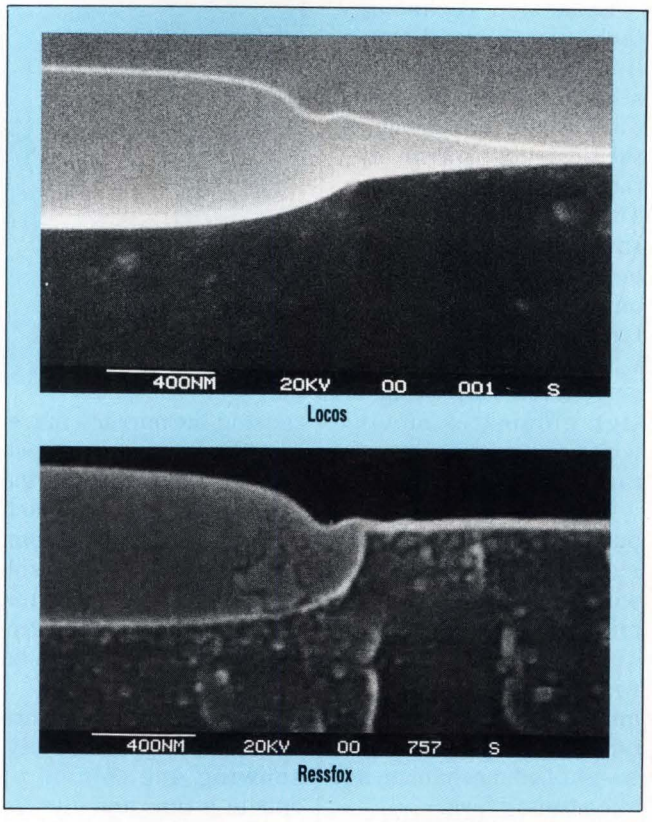
By reducing the beak length to almost zero (about 0.05 μm) from the typical length of about 0.5 μm or longer for other oxide isolation schemes, transistor spacing can shrink as much as 30% *(see the figure)*. Of course, other limiting factors, such as metallization pitch and contact opening (via) dimensions, must keep pace with the Ressfox process.

To obtain the reduced intrusion, the Ressfox process adds some steps over the standard Locos processes. This increases chip manufacturing costs by an estimated 5%, according to Gayle Miller, manager of advanced process development at NCR. However, Miller notes that the Ressfox process only adds about half as much to the chip cost than the more complex side-wall mask isolation (Swami) schemes currently used elsewhere. As a result, Sematech, the research consortium in Austin, Texas has decided to adopt NCR's Ressfox process for its submicron VLSI.

Wafer processing starts with a sequence similar to standard Locos structures: twin wells are formed in the substrate, the pad oxide is grown, and a layer of nitride is deposited. Next, with Locos wafers, windows are opened in the nitride and oxide layers and the exposed silicon regions are oxidized. But with Ressfox, the exposed silicon is first slightly etched using reactive ion etching to a depth of less then 0.25 μm and then a consumable nitride layer is formed before the silicon is thermally oxidized.

The consumable nitride layer prevents the bird's beak from intruding into the active transistor region and then is consumed during the oxide creation. Because the nitride is consumed, stress-induced defects in the bird's beak region are also minimized. Tests performed on diodes and MOS devices made with Ressfox show that the device characteristics are improved over similar devices made with standard Locos schemes.

DAVE BURSKY



TINY DISPLAY SUSPENDS IMAGE IN SPACE BY SYNCHRONIZING SCANNING MIRROR TO LEDS

A tiny 2.5-oz "virtual" display projects an image that appears to float in space, and gives roughly the resolution and appearance of a 12-in. monitor. The Private Eye comes in a light-tight package that's 1.2 in. high by 1.1 in. deep by 3.2 in. wide. It can be hand-held or serve as a visual Walkman on a lightweight headset.

The display produces text and graphics at a resolution of 720 by 280 pixels. The screen can be formatted to 25 lines of 80 characters per line, making it suitable as a display device for pocket PCs, full-screen radio pagers, and pocket fax machines, as well as military and industrial head-up displays.

A start-up company, Reflection Technology, Waltham, Mass., has been marketing the Private Eye for over a year, but only now is it revealing how the display works. The patented display is the brainchild of Reflection Technology founder and president Allen Becker. To develop Private Eye, Becker combined LED and scanning-mirror technology. It consists of an LED column display, a magnifying lens, a spring-mounted moving mirror attached to a voice coil, a counter-moving weight to cancel mirror vibrations, and some custom ICs.

Instead of adding dots (pixels) to make a matrix, Becker set the mirror on an angle to the staggered LED column *(see the figure, p. 30)*. By hinging the mirror at one end and adding an electromagnet, the mirror is made to resonate, like an audio-speaker cone, through a 15° arc.

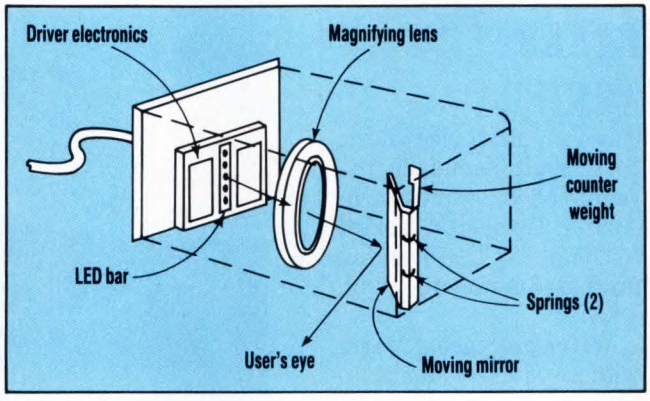
Reflection Technology took a new approach to earlier scanning-mirror schemes by synchronizing the varying frequency of the scanning mirror with the rate of the LED output. The mirror is moved by the small voice coil mounted behind it. What's more, the mirror mounts on two electrically isolated springs, which are used to carry current to the coil. That design eliminates moving wires, which are subject to fatigue and breaking.

The voice-coil motor pushes against a spring-mounted counterweight, which is set opposite to the mirror. The resonant frequency of the counterweight is the same as the mirror's, which makes the entire mirror-counterweight-coil mechanism act like a tuning fork.

Resonance is triggered by a photodetector sensor mounted to the case behind the mirror. A tab on the back of the mirror interrupts the sensor circuit as the mirror approaches maximum deflection, then allows the sensor circuit to close again as the mirror moves back from maximum deflection. The frequency is calculated from the timing of these events, and power is applied at the correct time to maintain resonance.

The mirror mechanism isn't the only innovation in Becker's design—there's also his novel approach to the LEDs. The array consists of two columns of staggered LEDs, which appear almost as a single column. The individual pixels alternate between the columns.

To construct an image, each column is illuminated at a slightly different time,



causing the mirror's movement to combine the two columns and making the pixels appear to touch each other from top to bottom. The resulting image is solid, without any of the blank interrupt lines usually apparent between scanned lines on a CRT.

The LED columns are turned on and off rapidly, showing one column of dots at a time and moving the mirror to "paint" an array of single columns across a virtual full screen. Red LEDs are used now, but other colors and color combinations are planned. The last element in the visual apparatus is a plastic lens located between the mirror and LED array. The lens magnifies the image by 50 times.

Private Eye operates asynchronously, driven by all-CMOS circuits. An 8-bit microprocessor handles the housekeeping, such as initializing the unit at startup and controlling current to the mirror. An ASIC gate array, together with the microprocessor, helps control the servo loop to determine when to apply power to the voice coil.

A 256-kbit static RAM holds the bit map of the screen image after it's been sent from the host to the microprocessor. Finally, two shift registers mounted in the same package as the LED array convert the serial bit map from the static RAM into parallel data for display.

So far, the company has at least two customers: Medbar Enterprises Inc., Queens, N.Y., is using the display for a paperless portable fax machine, and Blue Mountain Software, Atlanta, is applying it as a head-up display for pilots.

LARRY CURRAN

SILICON-ON-INSULATOR PROCESS STRIDES CLOSER TO PERFECTION

An improved CMOS process that eliminates junction isolation between transistors enhances the transistors' immunity to radiation and lifts several performance limitations. Called separation-by-implantation-of-oxygen (Simox), the process was developed by Harris Semiconductor, Melbourne, Fla., for military and space applications and has been used to make 64-kbit static RAMs.

A variation of the silicon-on-insulator (SOI) technique, the process brings numerous improvements over earlier techniques. It implants oxygen in the wafer at a very high dose rate to create a Gaussian distribution of oxygen below the surface of the silicon wafer. Subsequent annealing converts the implanted oxygen to a buried layer of silicon dioxide (SiO_2) and also repairs any dislocations in the crystalline structure caused by the bombardment of oxygen during implantation.

Building circuit devices within the layer of insulation produces several advantages over conventional fabrication methods. First, there's no need for space-consuming junction isolation between CMOS transistors because each transistor is effectively surrounded by glass. That cuts the spacing between devices by up to 50%.

Second, without the depletion regions generated by p-n junction isolation, the circuits are highly resistant to damaging particles from single-event upset (SEU) radiation. This type of radiation emits high-intensity, transient bursts of atomic particles that burrow into bulk silicon, leaving a trail of electron-hole pairs. In the presence of the voltage field of a p-n junction depletion region, the effects of the resultant spurious current can range from device latchup to destruction.

The absence of p-n junctions also increases device speed because there aren't any speed-limiting junction capacitances. Finally, without the leakage currents associated with p-n junctions, CMOS circuits built with SOI processing can operate in ambient temperatures up to about 300°C. This capability intro-

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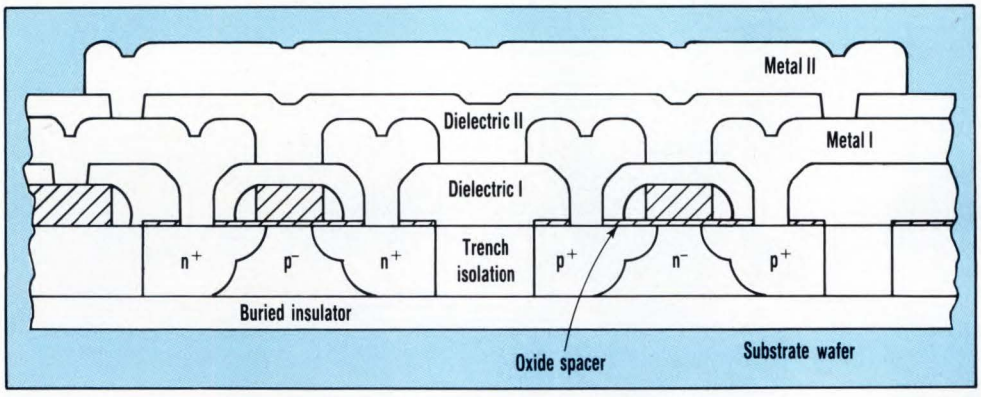


duces application possibilities for various high-temperature environments, such as in automotive and similar products.

The Harris process includes two levels of interconnections and 1.25-μm (drawn) feature size, which is scalable to submicron geometries. The company also developed a 0.25-μm GaAs process at its Military and Aerospace Division's microwave operation, Milpitas, Calif. Intended for higher frequency applications, the process offers increased gain through the K_u-band, and uses direct-write lithography on 3-in. and larger wafers.

MILT LEONARD

ROBOTICS AND ARTIFICIAL INTELLIGENCE TEAM UP TO OFFER SELF-LEARNING MOTION CONTROL

Robot control technology has leaped ahead now that experts at Ruhr University, in Bochum, West Germany, have readied a prototype mobile robot that draws on artificial intelligence. Using a self-learning expert system, the robot builds up the expertise and models of the environment needed to move unhindered in a given area to perform its tasks.

Because the university's robot uses AI techniques, its capability far exceeds that of conventional machines, like automatic welders in the car industry, that go through a fixed repetitive routine. The new robot is also superior to the kind of machine that stores a number of programs and picks one for execution.

In fact, the Ruhr University system is only the first of a new generation of robots, according to Wolfgang Weber, head of the university's Computer Sciences Department, where he and a team of engineering students developed the system. Except for some little-publicized work going on at the National Aeronautics and Space Administration (NASA), Weber knows of no similar self-learning, AI-based mobile robot that has reached the prototype stage.

Among the applications Weber sees for the system are transporting objects in factory halls, hospitals, and offices, or for moving dangerous materials in atomic power plants.

Called Auroma (for Autonomous Robot for Multiple Applications), the system weighs about 20 kg, occupies a 50-by-60-cm floor space, and is 40-cm tall. Its positioning accuracy is within 2 to 3 cm over a distance of 20 m.

At present, Auroma's maximum speed is about 50 cm/s in straight-line motion. But Weber's team is working to increase the speed so that a 600-m^2 (5000-ft^2) office or supermarket can be cleaned in 15 to 20 minutes.

Controlling Auroma are three microprocessors, all operating in parallel and one each assigned to the robot's three control levels. The lowest level, implemented with Intel's 8031, controls the drive motors' speed and acceleration, with the processor delivering suitable control signals to the drives and acquiring data on speed and distance moved.

The next higher level, based on a Z80 processor, which is responsible for the robot's position, keeps tabs on its direction and position coordinates. For this task, the Zilog device processes and evaluates the data coming from the robot's sensors.

The highest and most complex level of robot guidance realizes the concept of learning strategies. This level takes into account the control parameters of the two levels below it. For highest-level control, the Bochum engineers have programmed a Motorola M68000 processor to pick and execute a number of routing strategies.

These strategies define how the robot may move to find its way around and perform a task. Among the motion choices are an east-west or north-south direction, along a zig-zag or spiraling course, or in a back-and-forth lawn-mower fashion.

Beyond that, however, the robot uses automatic learning processes. Consequently, it builds up a model of its environment, along with all obstacles in the area. Using this self-programmed model, the robot knows which way to move to avoid obstacles. In this operation, methods of artificial intelligence are used which, in effect, turn the robot into an expert system that, on its own, acquires the expertise needed to move around in its environment.

Performing and evaluating the strategy calculations also takes 5 ms, while for route planning about 3000 Pascal operations are needed. Roughly 100 ms are needed to perform these operations.

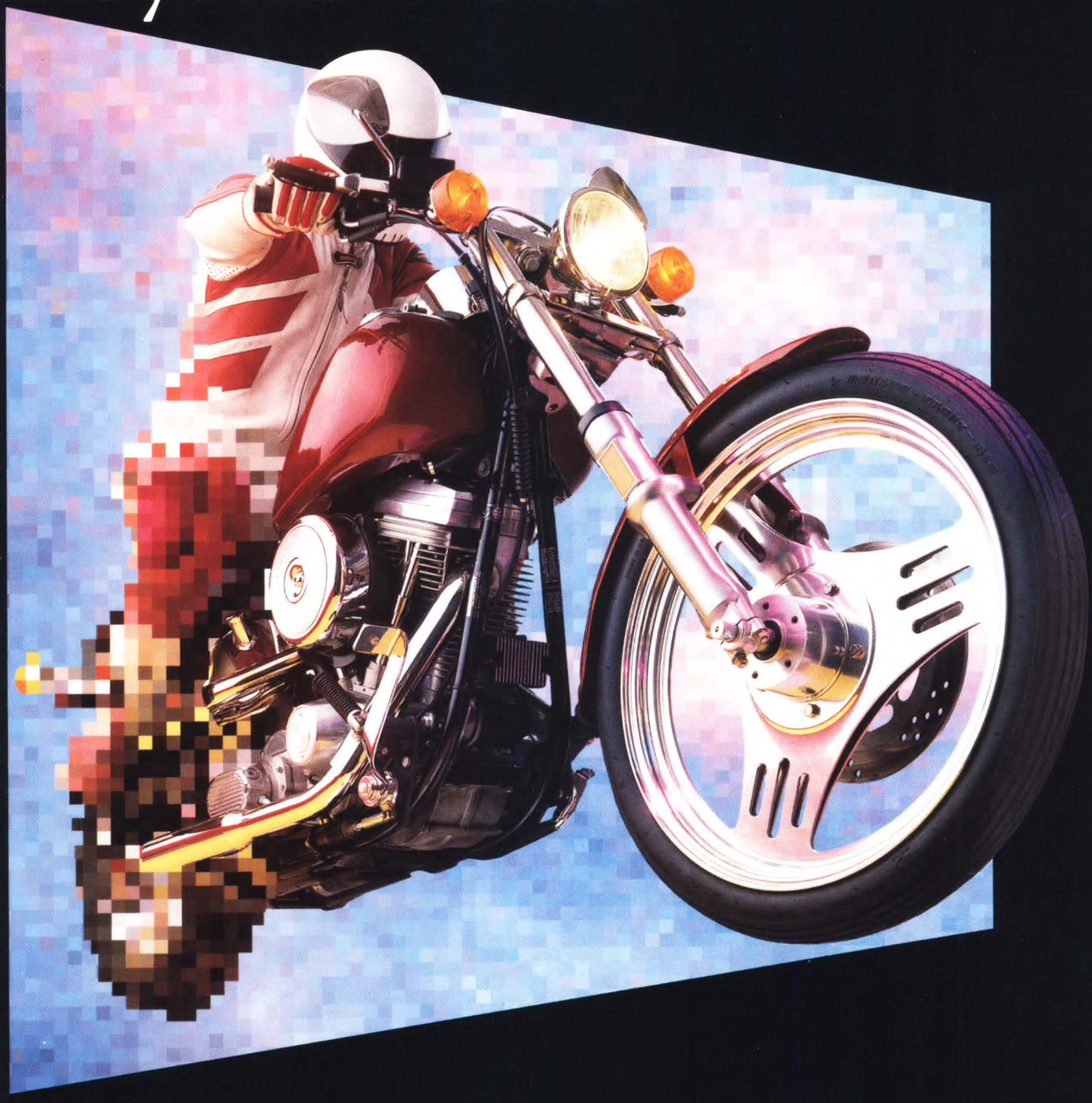
The robot's eight sensors detect obstacles ahead. These sensors are 39-kHz ultrasound types with a 2-m sensing range—their beam points straight ahead. A number of infrared sensors come into play should the ultrasound types fail to supply data on obstacles.

JOHN GOSCH

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Beyond VGA



IN THE ERA OF

MegaChip TECHNOLOGIES

TIGA-340 from Texas

The open graphics interface standard a clear path for your future.

A ground swell of support is rallying behind TIGA-340™, the Texas Instruments Graphics Architecture. It and TI's TMS340 family are poised to become the next standard beyond VGA as PC users demand higher performance and resolution.

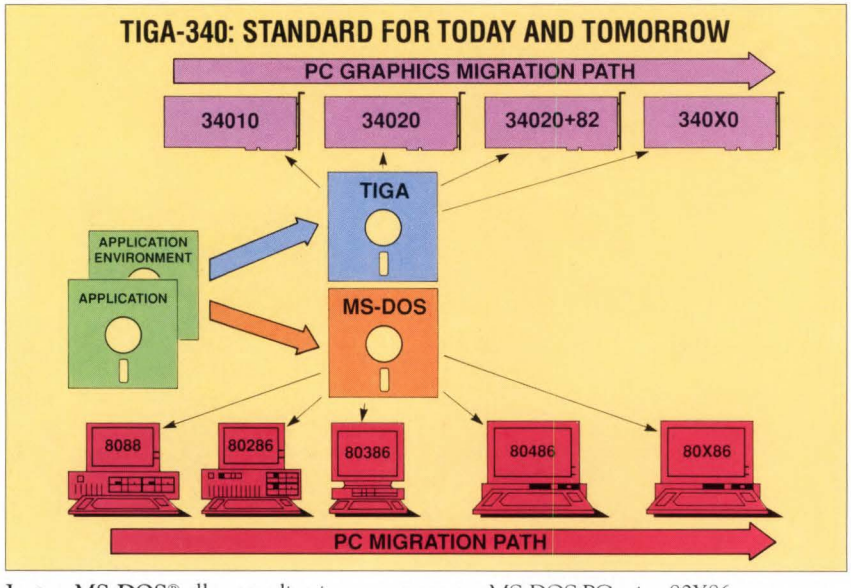
The PC graphics standard anyone can use

TIGA™ is a high-performance software interface that optimizes communications between industry-standard 340 family processors and the PC host processor.

With TIGA, hardware and software specifications for a PC graphics standard are open and available from inception — one of the reasons why more than 100 companies have already made plans to evaluate TIGA-compatible hardware and software products.

Lowest cost, highest performance

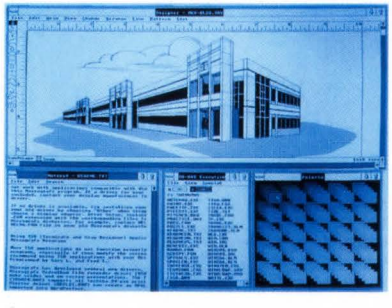
TIGA's move into the mainstream is being fueled by the price of TMS34010-based boards falling to well below $1,000. In fact, TI's 34010 processor is the most economical way to implement high-performance 1024 x 768 resolution PC graphics boards. The faster speed and greater throughput of the second-generation 34020 result in even higher performance boards.



Just as MS-DOS® allows applications to run on any MS-DOS PC using 80X86 processors, TIGA allows graphics applications to run on any TIGA display system using a 340X0 processor.

Clear migration path

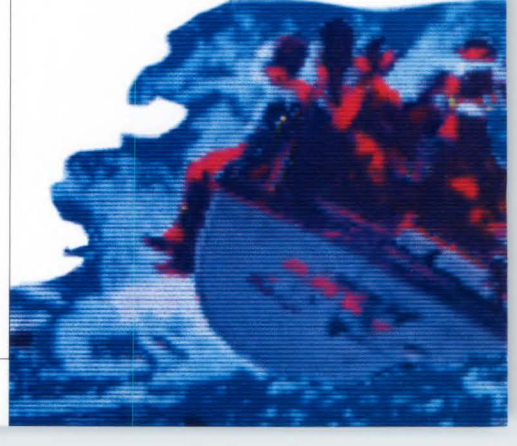
TIGA provides a common platform upon which graphics applications can take advantage of the processing power of the TMS340 family.



Software developers no longer have to rewrite code in order to migrate to higher performance hardware. Software applications that run through TIGA on the 34010 processor run on the upward-compatible 34020 as well as on future 340 family members.

Hardware developers benefit from wide software support, reduced system development time and costs, and easy differentiation of products.

At present, TIGA supports DOS-based PCs, with UNIX™ and OS/2 forthcoming.



Instruments:
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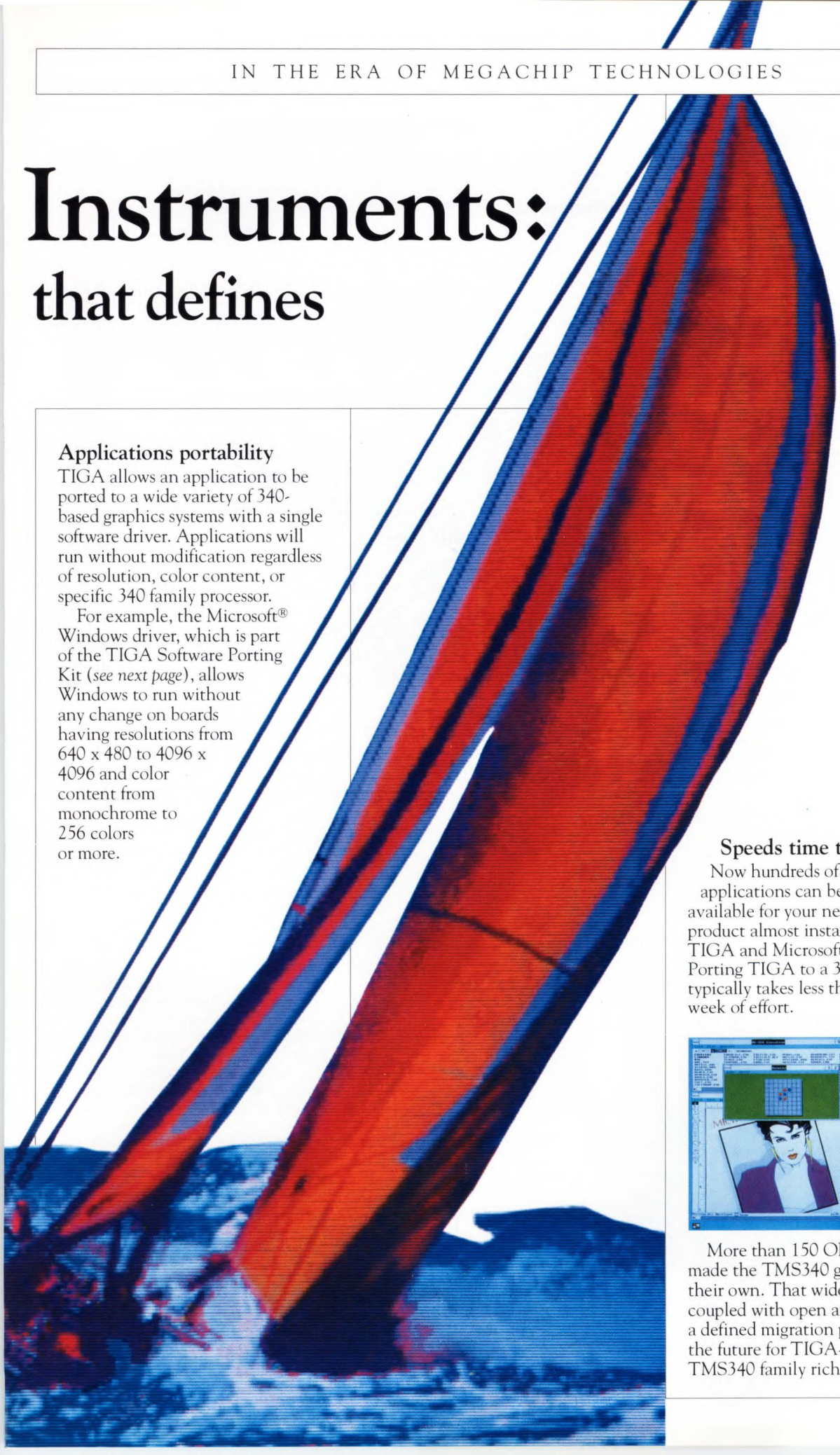


Applications portability

TIGA allows an application to be ported to a wide variety of 340-based graphics systems with a single software driver. Applications will run without modification regardless of resolution, color content, or specific 340 family processor.

For example, the Microsoft® Windows driver, which is part of the TIGA Software Porting Kit (*see next page*), allows Windows to run without any change on boards having resolutions from 640 x 480 to 4096 x 4096 and color content from monochrome to 256 colors or more.

Speeds time to market

Now hundreds of popular applications can be made available for your new graphics product almost instantly using TIGA and Microsoft Windows. Porting TIGA to a 340-based board typically takes less than one man-week of effort.

More than 150 OEMs have made the TMS340 graphics family their own. That wide acceptance, coupled with open architecture and a defined migration path, makes the future for TIGA-340 and the TMS340 family rich and promising.

TI's leadership TMS340 graphics family

No other supplier comes close to TI in the range of cost/performance options for the development of integrated graphics solutions. The widely used TMS34010 processor and other family members are now

being joined by a group of new-generation products that will bring the higher levels of workstation performance to PCs.

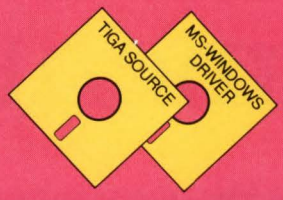
Chief among these is the TMS34020, a programmable, 32-bit processor up to 20 times faster than the 34010.

For use with the 34020, the TMS34082 will perform floating-point operations up to 100 times faster than current PC coprocessors. It is the industry's first graphics floating-point coprocessor.

The family's video RAMs, invented by TI, have been augmented by the TMS44C251 1-megabit VRAM. It was designed in conjunction with the 34020 for the high system bandwidths demanded by today's mid- and high-resolution graphics systems.

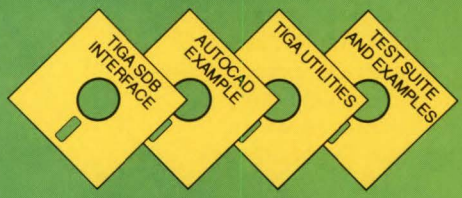
TIGA-340 DEVELOPMENT KITS

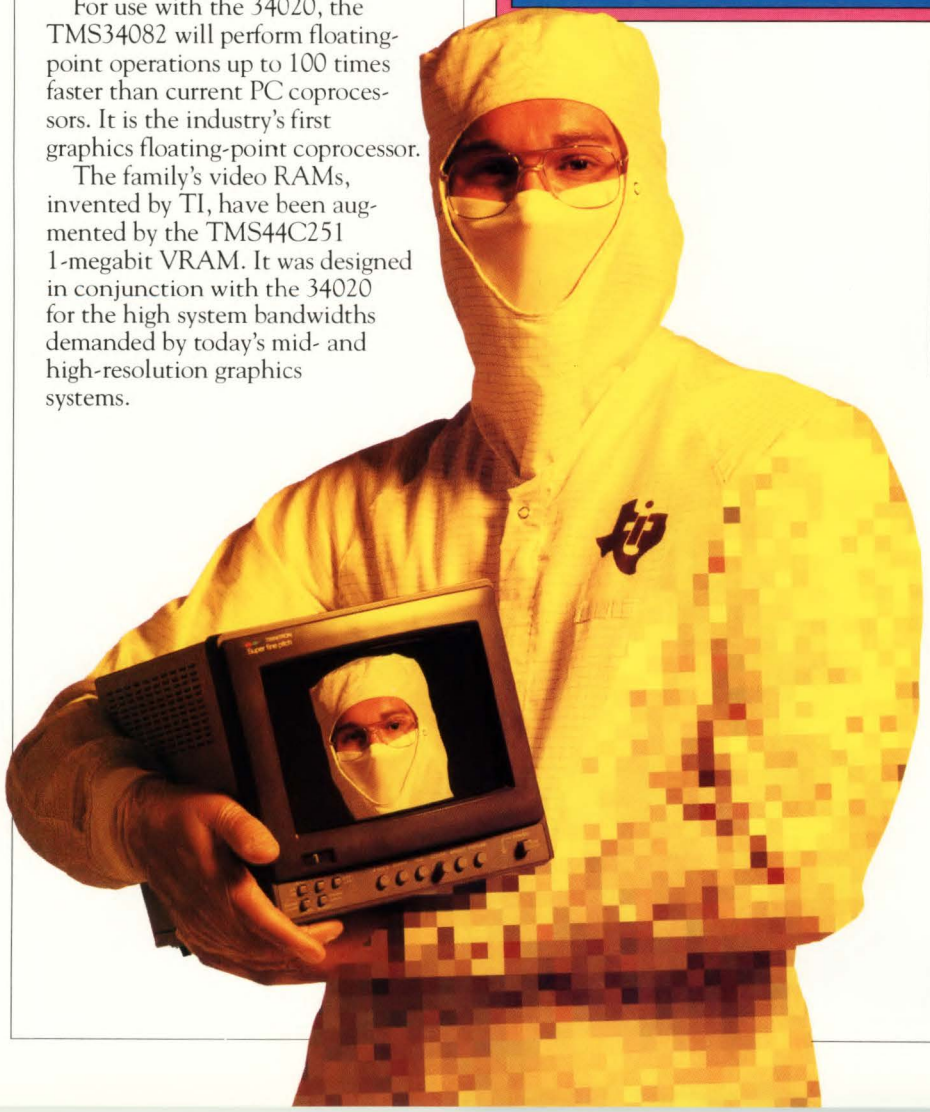
TMS340SPK-PC SOFTWARE PORTING KIT
is for use by hardware developers to port the TIGA interface to any TMS340-based system.



TMS340SDK-PC SOFTWARE DEVELOPER'S KIT
is designed for those who want to develop direct 34010 code or downloadable extensions to TIGA.

TMS340DDK-PC DRIVER DEVELOPER'S KIT
allows software developers to make existing software applications run on TIGA-compatible 340-based systems or develop new applications.





Free user's guide

For more information about the TIGA-340 standard, get your free copy of the *TIGA-340 Interface User's Guide* and the *TIGA-340 Interface Brochure*.

Call 1-800-336-5236, ext. 3526, or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

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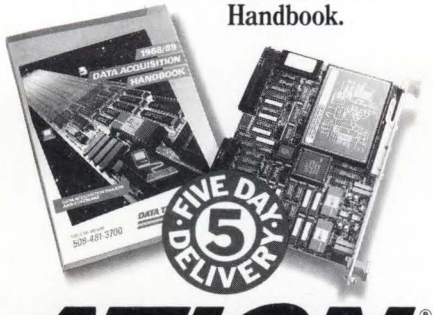
DT1492-F	16SE	12	1, 2, 4, 8	150	2	130/DAC	16	3075
DT1492-F	8DI	12	1, 2, 4, 8	150	2	130/DAC	16	3075
DT1492-G	16SE	12	1, 2, 4, 8	250	2	130/DAC	16	3515
DT1492-G	8DI	12	1, 2, 4, 8	250	2	130/DAC	16	3515
DT1492-L	4DI	12	1	750	2	130/DAC	16	4175
DT1495	16SE/8DI	12	1, 10, 100, 500	40/2.5	2	130/DAC	16	2525
DT1497	4DI	16	1	100	2	130/DAC	16	3515
DT1498	4SE(SS&H)	12	1	100	2	130/DAC	16	3075



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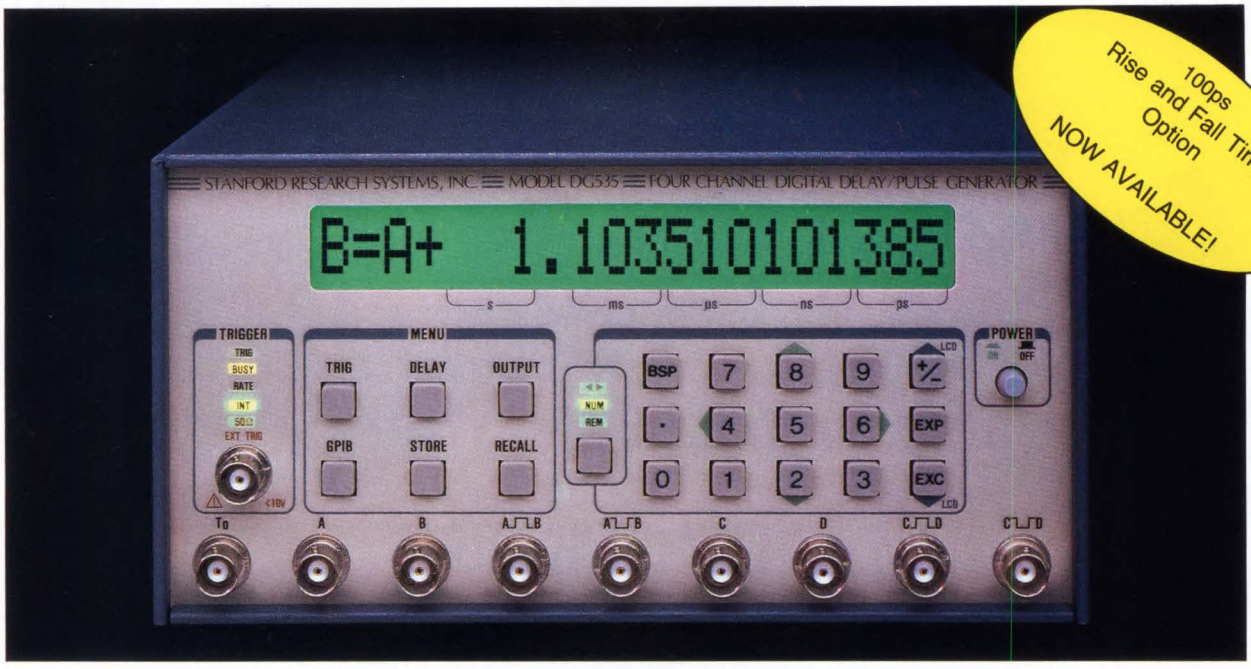
New Precision Pulse Generator



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- **Times from 0 to 1000 sec.**
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- **50 ps rms Jitter**
- **1 ppm Accuracy (Option 03)**
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CIRCLE 53

IEDM TACKLES FRESH DESIGN APPROACHES

RESEARCHERS TURN TO NEW STRUCTURES, EXOTIC COMBINATIONS OF MATERIALS, AND MORE SOPHISTICATED PROCESSING.

MILT LEONARD

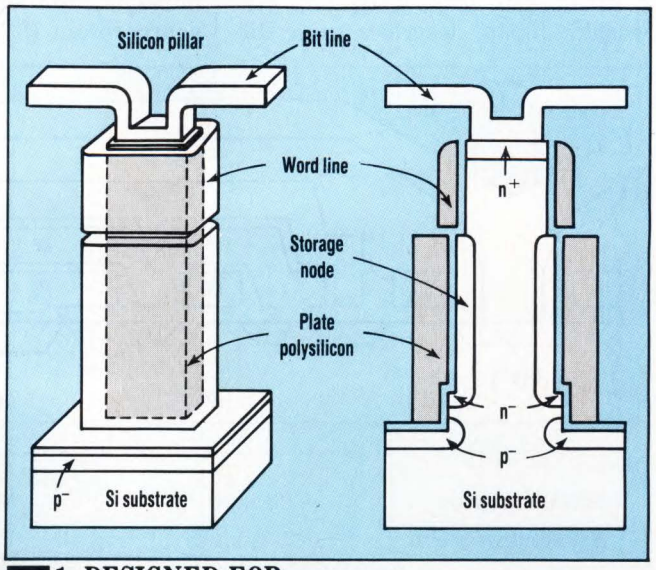
This year's International Electron Devices Meeting (IEDM), to be held Dec. 3 through 6 at the Washington Hilton and Towers, Washington D.C., will give a sneak preview of exciting new technologies that will dominate in years to come. Advances in wafer processing are making it possible for gallium-arsenide circuits to interface directly with silicon. Memory and logic device manufacturers are developing new scaling scenarios, dipping into submicron feature sizes, and experimenting with unconventional materials to improve performance. And power-device designers are overcoming traditional switching-speed limits by resorting to novel device structures.

Featuring almost 200 papers partitioned into 35 sessions, this year's IEDM program spans topics ranging from radical concepts still on the drawing board to tried-and-proven device designs on the verge of commercialization. Systems designers will be particularly interested in recent developments in memory, logic, and power-device technologies.

MULTIMEGABIT MEMORIES

Memory continues to be the staging ground for developing new device structures and fabrication processes. Motorola, Austin, Texas, will describe a sub-micron technology for fast CMOS static RAM (SRAM). This process has been used to produce an experimental 16-kword-by-4-bit SRAM whose NMOS and PMOS transistors have effective gate lengths of 0.30 and 0.35 μm, respectively. Used in a ring-oscillator circuit, the SRAM features delay times are 85 ps at 3.3-V and 65 ps at 5-V supply voltages. Predicted lifetime exceeds 10 years for 0.3-μm NMOS transistors that are operated at 3.3 V.

Two papers describe advances in SRAM performance using biCMOS technology. In one paper, researchers at National Semiconductor, Puyallup, Wash., will present a next-generation 0.8-μm biCMOS technology—biCMOS-



1. DESIGNED FOR multimegabit DRAMs, Toshiba's memory cell design surrounds a silicon pillar with a transfer gate and capacitor electrode. The result is a cell area of just 1.2 μm^2 and a 30-fF capacitance, using 0.5-μm design rules.

IV—optimized for producing 256-kbit ECL I/O SRAM. This paper includes a detailed description of the process technology, MOS and bipolar transistor characteristics, and ring-oscillator circuit performance.

Probing deeper into the sub-micron biCMOS regime, a paper from Texas Instruments, Dallas, details a 0.5-μm biCMOS process technology developed for high-performance logic and 4-Mbit SRAMs. The process flow supports a 23-μm^2 SRAM cell that uses a polysilicon PMOS load and a vertical NMOS driver. At a 4-V operating voltage, the measured CMOS inverter delay is equal to the delay in a 0.5-μm CMOS-only process and is 40% faster than a previous generation 5-V 0.8-μm CMOS technology.

Novel Architectures

Dynamic RAMs (DRAMs) will also receive their share of attention, with most papers focusing on attempts to reduce cell area to less than 1.5 μm^2 for large-scale commercialization of 64-Mbit densities. To reach this goal, several vendors are experimenting with novel architectures which are more scalable that conventional structures.

In separate papers, Toshiba, Kawasaki, Japan, describes three different approaches: Toshiba's first paper discusses a surrounding gate transistor (SGT) cell structure in which a transfer gate and capacitor electrode surround a pillar of silicon *(Fig. 1)*. The bit-line contact is formed on the top of the silicon pillar, which also has the transistor source and drain contacts. Using 0.5-μm design rules, the structure is said to be scalable to a 4-μm pillar height and occupy just 1.2 μm^2, for 64- and 256-Mbit DRAMs with storage capacitance of 30 pF. In contrast, current 16-Mbit DRAMs have a cell area of 3.3 μm^2.

Toshiba's second paper details the spread-stacked capacitor (SSC) cell, which is a variation of the conventional stacked-capacitor cell design. By interleaving the storage capacitance of adjacent cells, the SSC cell has up to four times the capacitance of conventional designs without increasing cell size. This paper proposes the SSC approach for 64- and 256-Mbit SRAMs.

The final related presentation from Toshiba discusses a selective epitaxial technology that forms an elevated source/drain MOSFET structure (with contacts overlapping the field and gate regions) and minimizes junction depth. Called a spread source/drain (SSD) MOSFET, this structure has reduced short-channel effect and requires less isolation spacing than a conventional lightly doped drain MOSFET. The paper concludes that the SSD design combined with a stacked-capacitor structure can result in cell sizes down to 1.3 μm^2.

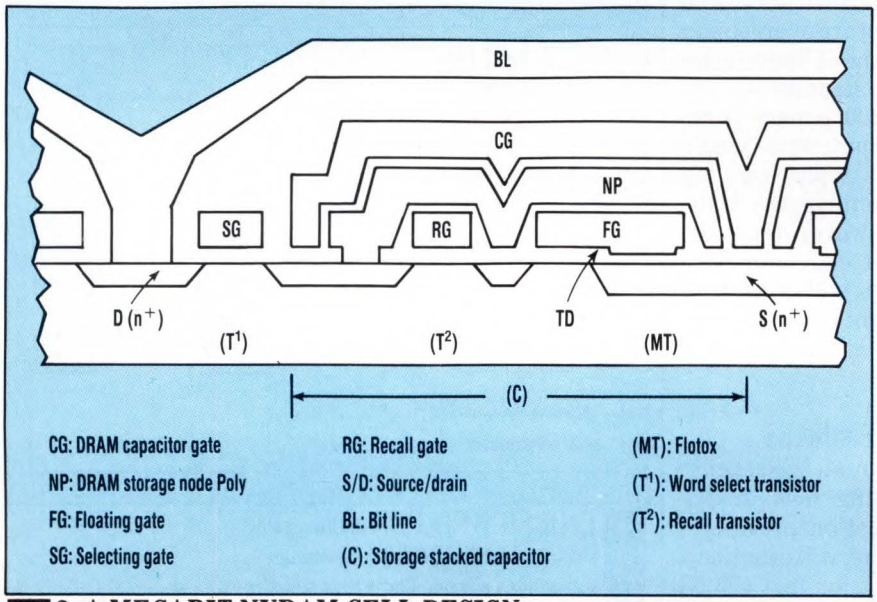
Texas Instruments researchers continue to refine the trench-capacitor DRAM cell design for 64-Mbit densities because of its advantages of large cell capacitance, planar topology, and processing simplicity. TI's paper describes a conventional trench cell made with a unique field-plated isolation, a thin nitride/oxide storage insulator, and a trench sidewall doping adjustment. These combined attributes minimize leakage currents within the device, which have been an obstacle to further down-scaling to 1.5- to 2.0-μm^2 cell sizes.

Developers of other types of memory devices exhibit the same degree of innovation in their pursuit of improved cell performance. In the 16-Mbit EPROM arena, the cell area required for a practical die size is less than 4 μm^2.

A paper from SGS-Thompson Microelectronics, Agrate Brianza, Italy, will report on the development of a process technology for its SFOX (self-aligned field oxide) cell structure, which is 30% smaller than a conventional T-shaped cell. The cell is used to produce contactless 16- and 64-Mbit EPROM arrays, which can be organized for either common-ground or virtual-ground selection. The paper will include performance results for a 4.16-μm^2 cell.

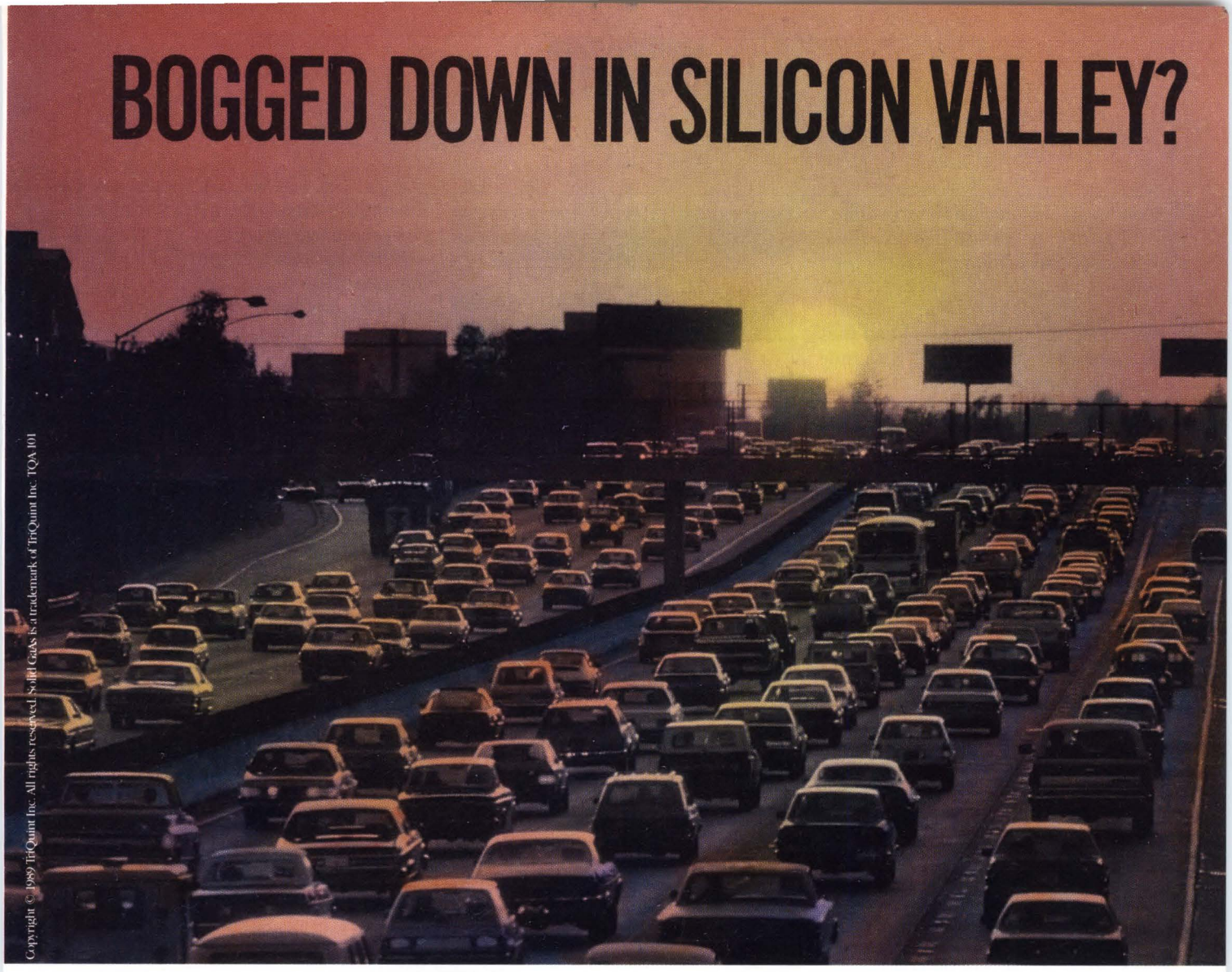
A similar cell-size reduction will be disclosed by NEC Corp., Kanagawa, Japan. This presentation will include processing details, cell structure, and the design details of the bit-line contacts that reduce the parasitic resistance of the cell transistors. The 3.6-μm^2 cell is programmed in just 10 μs.

Toshiba will describe a 3.85-μm^2 EPROM cell based on a new scaling method. The EPROM cell uses 0.6-μm design rules and is made with a self-aligned source (SAS) process, with the self-aligned source diffu-



2. A MEGABIT NVRAM CELL DESIGN with a stacked storage capacitor by Sharp is made with a triple-stacked polysilicon process. The approach produces a cell area of 35.02 μm^2 and a 50-fF storage capacitance using 0.8-μm design rules.

BOGGED DOWN IN SILICON VALLEY?



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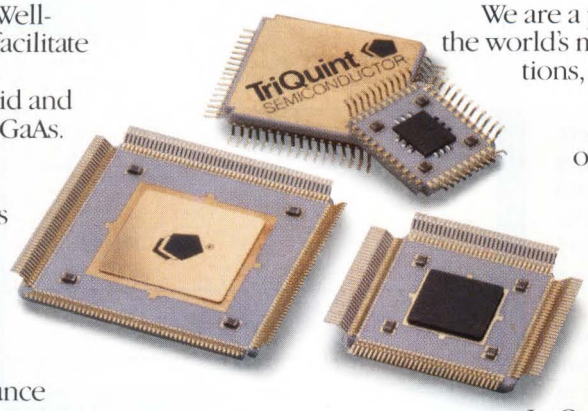

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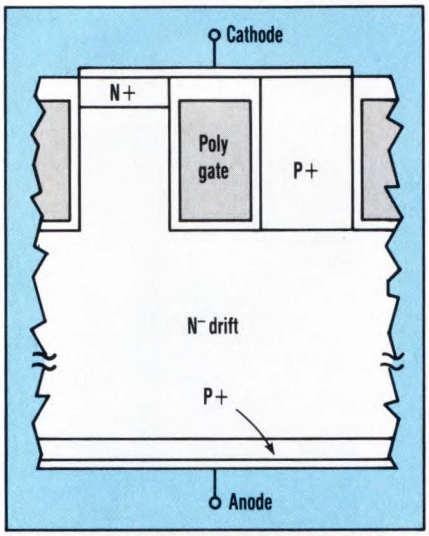
Conference attendees involved with nonvolatile memory technology will be interested in a presentation from Sharp Corp., Nara, Japan, which examines a NVRAM cell that integrates a volatile RAM with nonvolatile store and recall functions. The 35.02-μm^2 cell is created by a triple-stacked polysilicon technology with 0.8-μm design rules and has a 50-fF storage capacitance *(Fig. 2)*. This paper divulges the process technology, cell structure, and read/write and flash store/recall mechanisms. Also included in the presentation are measured data-store characteristics, data-retention times, and endurance.

Two papers from Toshiba will describe new EEPROM cell designs. The first paper details a technique for improving endurance to 10-million write/erase cycles by reducing oxide damage. This cell design has potential applications in 64-Mbit flash or 4-Mbit full-featured EEPROMs.

The second paper proposes a flash-erase EEPROM cell with 5-V-only programming that uses three layers of polysilicon to get a 13.5-μm^2 cell size with 1.0-μm design rules. A related joint paper from Philips Research Laboratories, Eindhoven, The Netherlands, and Faselec AG, Zurich, Switzerland, illustrates the use of a titanium-silicide gate to combine an EPROM or EEPROM module with single-level polysilicon CMOS logic.

Several interesting papers will report on advances in the performance of bipolar and biCMOS devices. Two companies have independently reached a record-setting 29-ps ECL circuit delay.

NEC will describe in a paper, a 40-GHz silicon bipolar transistor based on 0.8-μm design rules for VLSI devices. The paper focuses on the process technology that produces a graded doping profile in the n-type epitaxial layer, a buried-emitter electrode structure, and trench isolation. To get the same speed, Hitachi, Tokyo, developed a 0.5-μm SICOS technology with reduced base resistance and U-groove isolation, which decreases the base resistance and substrate capacitances. This paper discusses the fabrication process, which produces a 44.2-μm^2 transistor size and a 0.3-μm emitter-base separation and analyzes ac characteristics.

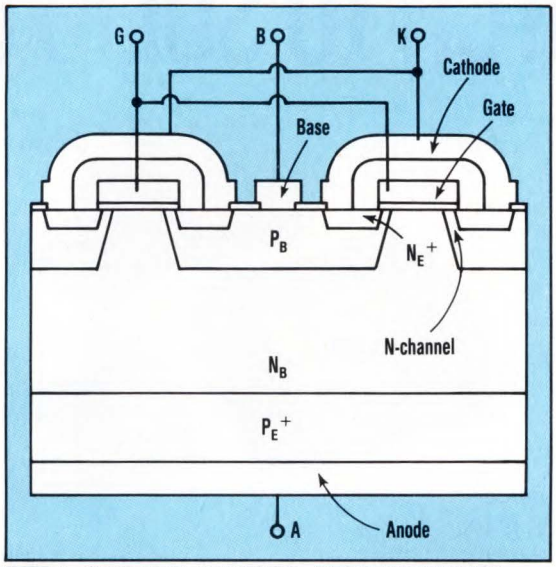


3. A FIELD-CONTROLLED thyristor from General Electric departs from past designs by using high-impedance MOS gate control to replace the parasitic thyristor. The thyristor can cause unwanted turn-on in conventional devices.

Epitaxial base bipolar technologies are attracting attention because of their adaptability to very thin base formation. But this advantage is difficult to maintain in self-aligned structures because of the subsequent heat treatment following base formation. The IBM T.J. Watson Research Center, Yorktown Heights, N.Y., reveals low-temperature epitaxial techniques that produce npn transistors with an ultrathin 60-nm base structure that's unaffected by subsequent processing.

Another processing development for producing self-aligned bipolar transistors will be reported by Philips Research Laboratories. This technique yields a sidewall-contacted structure that has significantly reduced parasitic capacitances and base resistance. The process reportedly solves the base-linkup problem for use in such high-performance analog applications as integrated front-ends.

Three papers deal with advances in biCMOS technology. In one paper, Toshiba will explain its development of a low-temperature (800° to 850° C) process for producing 0.5-μm biCMOS devices. In another paper, Fujitsu, Kawasaki, Japan, will describe a high-speed 0.6-μm process that uses the same polysilicon layer for bipolar base contacts, and PMOS gates to get 330-ps delays with a 0.5-pF load capacitance. And a joint presentation by Signetics Co., Sunnyvale, Calif., and Applied Materials, Santa Clara, Calif., will discuss the use of an ultrathin epitaxial layer over patterned arsenide subcollectors to solve auto-doping problems in a 0.8-μm biCMOS process. The key to this accomplishment is using a low-temperature chemical vapor-deposition technique.



4. PULSED-POWER APPLICATIONS can make use of Toshiba's MOS-assisted, gate-triggered thyristor. The device's architecture is designed to deliver extremely low turn-on power losses while exhibiting high breakdown-voltage capability.

III-V TECHNOLOGIES

Conference papers from companies evaluating GaAs devices reflect the continuing push toward lower power dissi-

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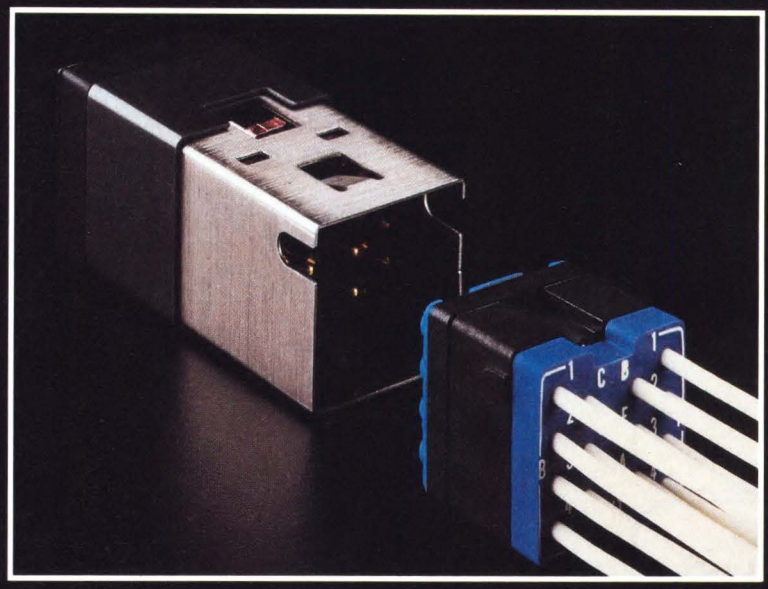

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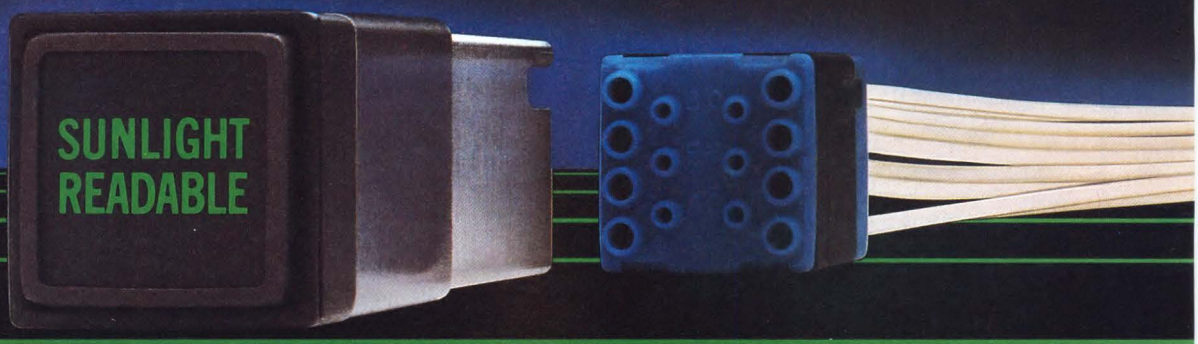

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pation and higher circuit densities. For low-power circuits, a paper shows how NTT LSI Laboratories, Kanagawa, Japan, developed a novel bridged-electrode process to create GaAs heterojunction bipolar transistors (HBTs) with 1-μm^2 emitters. This paper discloses the fabrication process and presents performance measurements.

Also driving toward higher circuit densities, Matsushita Electronics, Osaka, Japan, will discuss in a paper a bipolar-FET design that combines the low power consumption of a modulation-doped FET (MODFET) with the large current-driving capability of a GaAs/AlGaAs HBT. This paper details the fabrication process, which merges the MODFET into the HBT collector region with one epitaxial growth. A ring oscillator circuit made with the bi-FETs exhibits a 150-ps delay and dissipates 3.0 mW/gate.

One difficulty with GaAs HBT technology is interfacing these devices with other high-speed standard ICs, such as silicon ECL 100K. A paper from TI shows how the integration of isolated-emitter transistors (IETs) into a VLSI HBT process supplies I/O interfaces to other high-speed technologies. The paper includes performance results for a 19-stage ring oscillator circuit, as well as other circuits made with this process.

With an eye toward monolithic integration of optical devices, the Xerox Palo Alto Research Center, Calif., improved an earlier design of a lateral HBT with an annular ring configuration. This presentation will describe how three advances in the device architecture increased gain to 610 at optimum collector current. The discussion will also examine a prototype for an optoelectronic element that combines three transistors with a laser on a common substrate.

Power Semiconductors

Three conference papers on power semiconductors will unveil new device structures designed to improve thyristor turn-on and turn-off characteristics. General Electric Co., Schenectady, N.Y., presents a field-controlled thyristor (FCT) that uses MOS trench gates to control device turn-off.

The P^+ region, which forms a bipolar transistor segment, is formed laterally adjacent to the diode segment and is connected to the cathode instead of the gate *(Fig. 3)*. By using high-impedance MOS gate control, this type of architecture eliminates the unwanted parasitic thyristor and improves turn-off characteristics.

Swiss researchers have also examined MOS-controlled thyristors that use MOS gates with submicron channel lengths. A joint paper by ABB Corp., Baden, the Swiss Institute of Technology, Zurich, and Centre Suisse D'Electronique, Neuchatel, examines a cellular design employing up to 21,000 cells. It also presents measured and calculated values for turn-on, turn-off, and dc characteristics for various submicron MOS channel widths.

Toshiba devised a somewhat different architecture for a MOS gate-triggered thyristor for such pulsed-power applications as high-repetition excimer laser systems. A MOS gate located on the edge of the p-base layer turns on the thyristor with a high di/dt ratio *(Fig. 4)*. An additional bipolar gate on the p-base layer ensures constant p-base potential and high immunity to dv/dt. This paper includes waveforms and measured data that define device characteristics.

Another solution for switching elements in pulsed-power systems will be reported by researchers at the University of Southern California and the University of California at Los Angeles. Their paper details the process technology for a GaAs-based opto-thyristor that delivers an impressive peak current of over 70 A with a 1-Ω load resistor. Triggered by an AlGaAs laser diode, the device exhibits a di/dt of over 1.4 by 10^{19} A/s.□

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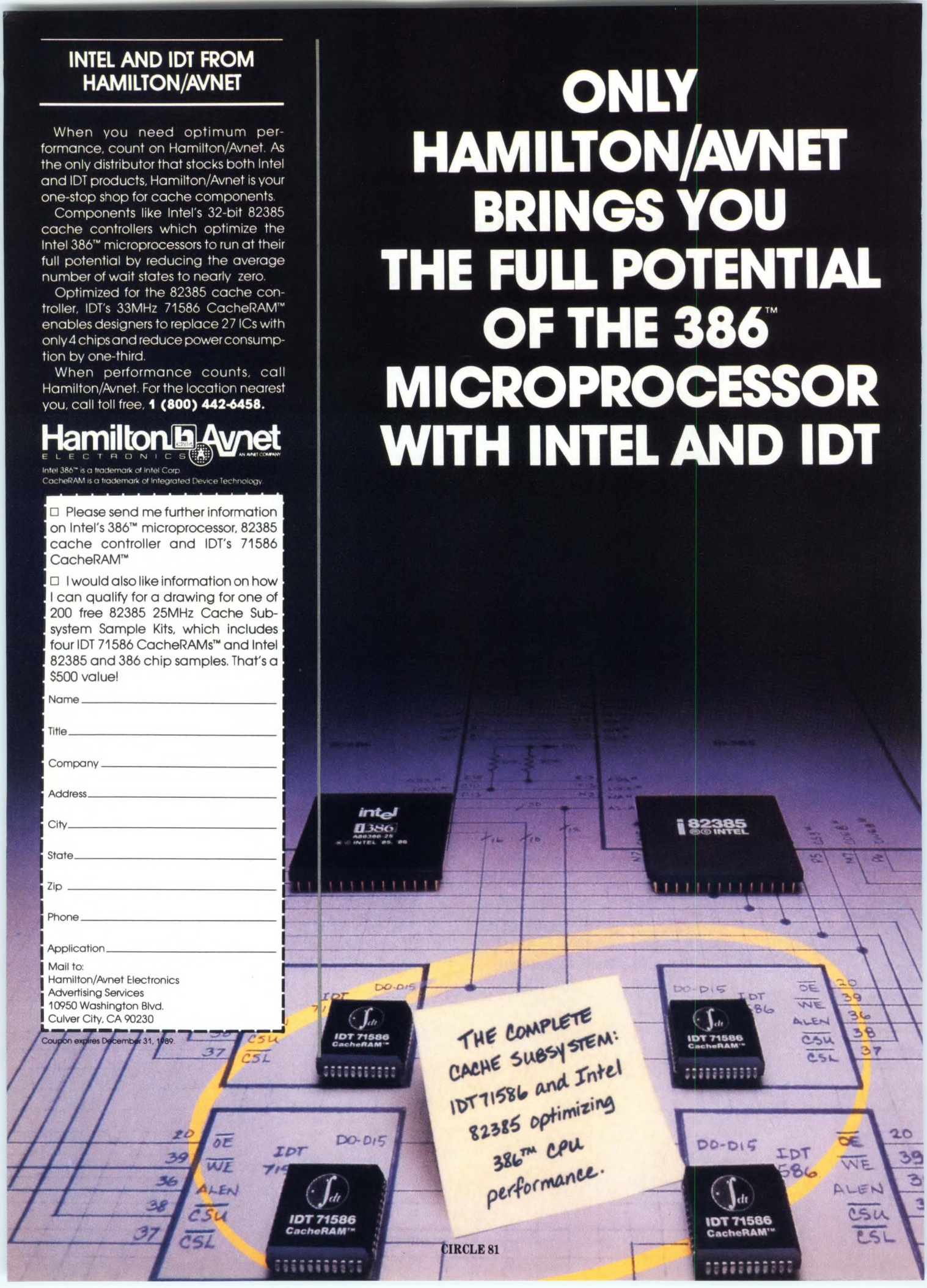

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IC ADCs SPOUT 12-BIT-ACCURATE WORDS AT 2 MSPs

FRANK GOODENOUGH

If you're a system designer who's been waiting on the long-promised 2-MHz-throughput-rate, 12-bit analog-to-digital converter on one chip, wait no longer. Two different chips are now available: the AD671 from Analog Devices, and the CAT5412 from Catalyst Semiconductor, a newcomer in the analog arena. Moreover, you don't need a sample/track-and-hold amplifier (SHA/THA) ahead of the CAT5412.

And if that weren't enough, two reasonably priced sampling amplifiers that can grab a new sample to 10- or 12-bit accuracy in under 40 ns have also arrived. Comlinear is offering you a small, low-chip-count, THA IC that acquires a fast-changing 2-V signal to within 0.01% accuracy in 36 ns maximum, and to within 0.1% accuracy in 32 ns maximum. Vanguard Semiconductor, another newcomer (grubstaked by California Micro Devices), on the other hand, has a one-chip THA that grabs a similar 2-V step to within 0.1% accuracy in 40 ns maximum—it's the fastest 10-bit-accurate chip you can buy. Vanguard expects it to reach 12-bit precision and plans to characterize it to 0.1% accuracy.

All four ICs offer impressive performance, use bipolar transistors, and dissipate under 1 W of power. For both converters, which each need an external reference, the 1 W is significantly less than the dissipation of large and costly power-hungry hybrids they replace. The 12-bit-accurate Comlinear hybrid THA sticks with an open-loop design (the storage capacitor isn't in the feedback loop), while the monolithic Vanguard sampler operates in a closed-loop manner.

Active devices in the Comlinear sampler consist of just three bipolar ICs and a pair of JFETs, while the trio of monolithic ICs are built on bipolar/MOS processes. The one-chip ICs make optimum use of the bipolar transistors for critical

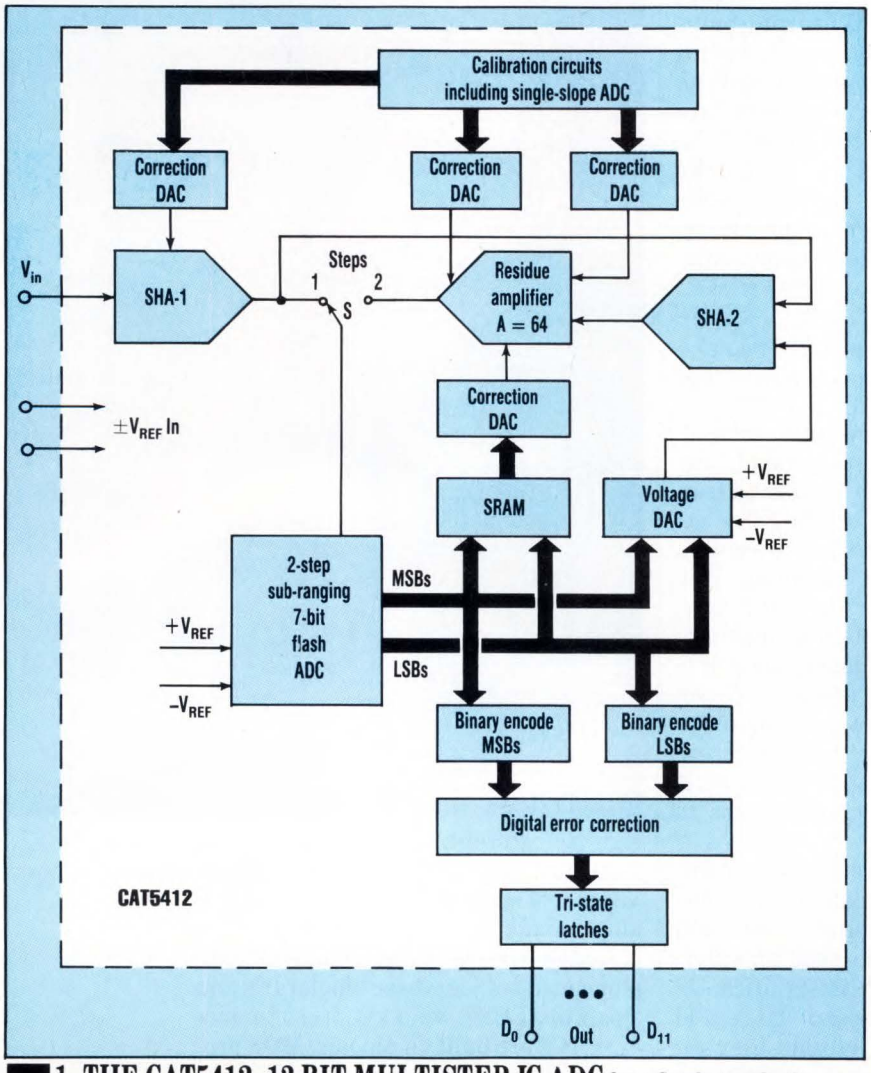
analog circuits and the MOSFETs for dense, fast logic as well as high-speed analog switches.

The four ICs are somewhat expensive, ranging from about $70 for the AD671 to just under $200 for the CAT5412. But that's nearly half the price of current devices, and their price-performance is unparalleled.

The two converters are very different except that they employ digitally corrected sub-ranging (multistep flash) architectures that offer high-speed a-d converter designers an almost unlimited opportunity for innovative analog circuit design.

In its 40-pin, double-width ceramic DIP, the CAT5412 is an improved (twice the speed) drop-in replacement for the Crystal Semiconductor CSZ5412 *(Fig. 1)*. Just as the Crystal part and the AD671, it needs an external reference. A version with an on-chip 1-ppm/°C reference will arrive sometime next year. The reference will be trimmed, after packaging, by an on-chip EEPROM.

The converter's input SHA supplies a typical input impedance of 10 MΩ in parallel with 10 pF and acquires a full-scale signal in 300 ns. Operating with a 16-MHz clock, conversion time is guaranteed to be between 625 and 688 ns. However, the pipelined analog front-end formed by the pair of SHAs gives the converter a minimum guaranteed throughput of 2 MHz—about 1-1/2 times faster than you may expect. Aperture jitter is typically 50 ps rms.



1. THE CAT5412, 12-BIT MULTISTEP IC ADC from Catalyst grabs the input with a sampling amplifier and supplies new 12-bit digital words at a 2-MHz rate.

With its usual full-power and small-signal bandwidths of 3 and 4 MHz, respectively, the converter easily handles Nyquist-frequency signals.

Full-scale analog input signal is from $-V_{REF}$ to $+V_{REF}$. The input is from 2 to 3 V for unipolar signals and ±1.5 V for bipolar signals.

Six versions of the chip are available: two grades (basic-J and premium-K) for the commercial (-C models), extended industrial (-I models), and military (-M models) temperature ranges. At 25°C and a 100-kHz input, all three models feature maximum peak harmonic and spurious noise and maximum signal-to-noise ratio plus distortion of –74 dB (J grade) and –77 dB (K grade). Typical total harmonic distortion is 0.02%.

Integral linearity error for J-grade C and I models is ±2.5 LSB maximum; ±1 LSB is typical for M models. For K-grade C models, it's a maximum of ±1.5 LSB and a norm of ±3/4 LSB (C and M models). Differential linearity for all devices with no missing codes guaranteed is ±0.9 LSB for J- and K-grade C and M models. Typical full-scale (gain) error for C, M, and I models is ±0.5, 1.5, and 3 LSB, respectively. Offset error for C and I models is ±0.5 LSB; for M models it's ±2 LSB.

All dc accuracy specifications apply from T_{MIN} to T_{MAX} after an on-chip auto calibration was performed. All devices operate from ±5-V analog supplies at 90 mA maximum, and ±5-V digital supplies at 10 mA maximum. Total dissipation is 1 W.

With its smaller 24-pin "skinny DIP" package and lower cost, the AD671 presents an interesting contrast to the CAT5412, which, unlike the AD562, doesn't need an external SHA *(Fig. 2)*. It's ideal where tens or even hundreds of channels must be rapidly scanned and digitized at a 2-MHz rate, and the data is fed to a host processor. Applications for the AD671 include both military and industrial data-acquisition systems.

By adding a high-speed SHA between the AD671 and the multiplexer, higher-frequency signals can be digitized. Furthermore, by adding a pair of Harris 500-ns-acquisition-time HA5330 SHAs ahead of it in a

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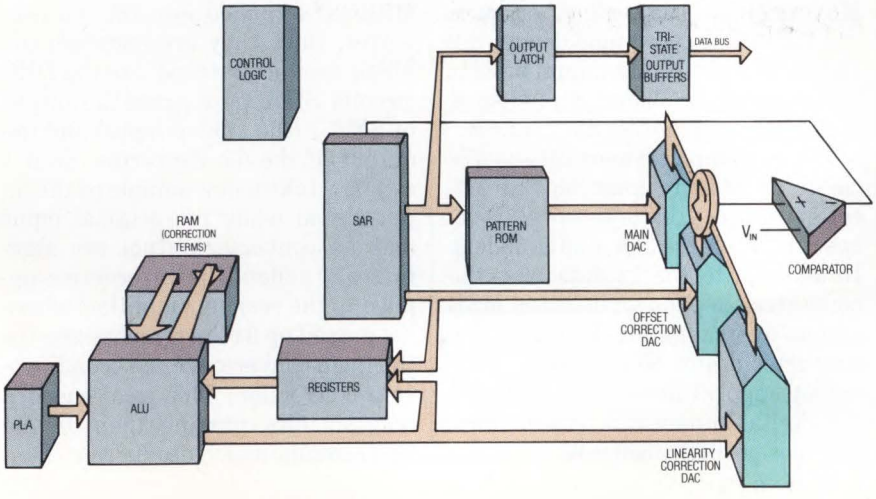
On-Board Sample/Hold	Yes	No	Yes
Self Calibrating	Yes	No	Yes
Max Power Consumption	70mW, +5/−5V	215mW, +5/−15V	250mW, +5/−5V
Price, 100pc	$15.90	$35.00	$37.40



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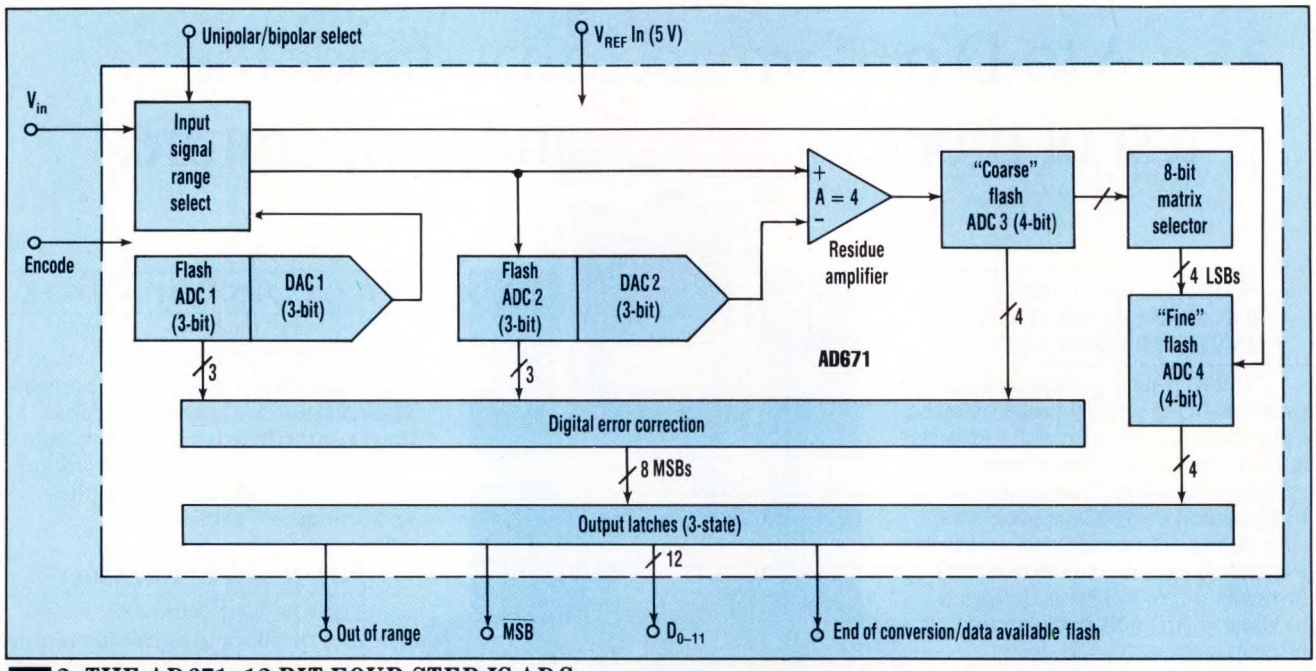

2. THE AD671, 12-BIT FOUR-STEP IC ADC from Analog Devices makes four sequential input-conversions with four flash converters, producing a new 12-bit word every 0.5 μs.

"ping-pong" circuit, it can keep up with the CAT5412.

Alternatively, the AD684 quad SHA can be used in a similar manner with signals to 100 kHz. The AD671 architecture, with its four sequentially employed flash converters and digital error correction, lends itself particularly well to this technique. That's because, unlike a successive-approximation (SAR) converter whose input signal must settle to 12-bit accuracy prior to the start of conversion, the 671's input can take 200 ns to reach 12-bit accuracy. Even with one SHA ahead of the 671, throughput rate is increased by overlapping the SHA's hold-mode settling time with the 200-ns window.

Dynamic specifications are impossible for the converter on the 671's data sheet without on-chip sampling. As a result, Analog Devices will offer a complete set of specifications built around a specific SHA.

Full-scale input voltage ranges for the AD671 are user selectable at 0 to 5, 0 to 10, and ±5 V with an external 5-V reference. The device's input resistance for the 5- and 10-V ranges are a minimum of 500 and 1000 Ω, respectively. On the other hand, the CAT5412 needs a negative reference for bipolar signals.

When a conversion starts, the 671's input sinks up to 5 mA in a few nanoseconds. The signal source must respond to this step by settling the input voltage back to a fraction of an LSB's original value—within about 100 ns. Input capacitance is a maximum of 15 pF. The J, A, and S models of the 671 are rated for the commercial and extended-industrial temperature ranges.

At 25°C, K-grade devices feature an integral linearity error of ±1 LSB maximum, and differential linearity of 12 bits minimum. Maximum gain error is within 0.25% of full scale. Maximum unipolar offset error is ±4 LSB for J and S models and ±2 LSB for I models. Maximum bipolar offset error for J and S models is ±10 LSB; for I models it's ±4 LSB.

The maximum temperature coefficients of gain/unipolar/bipolar offset error are ±10/5/15 ppm/°C, respectively, for the J, A, and S models. In addition to the 12 data bits, the converter supplies an inverted MSB and an overrange bit. Typically, the converter draws 45 mA from ±5-V analog supply rails and 15 mA from a 5-V digital supply rail. Power dissipation is normally 500 mW.

Being complex devices, high-resolution, multistep sub-ranging a-d converters make the reliable SAR appear simple. For example, Catalyst's CAT5412 has a pair of SHAs, a 7-bit two-step flash converter, a 7-bit polysilicon resistor-ladder voltage d-a converter, a residue amplifier with a gain of 64, and digital error-correction (DEC) and auto-calibration circuits. The converter can use an external clock, or a crystal connected between two pins. On-chip circuits supply the remainder of the timing.

At the convert command, SHA 1 goes into hold, and the 7-bit two-step flash produces the 7 MSBs. The MSBs are latched into the d-a converter. Once they are encoded, the MSBs are then latched into the DEC circuits. SHA 2 now grabs the output of SHA 1 (the analog input) and the output of the d-a converter. SHA 1 can now take a new sample of the input signal while the original input and d-a converter output are algebraically added. The difference is applied to the residue amplifier, where it's gained up 64 times and applied to the flash converter for a second two-step conversion. This pass encodes only six bits, passing them to the DEC circuit, which produces a 12-bit

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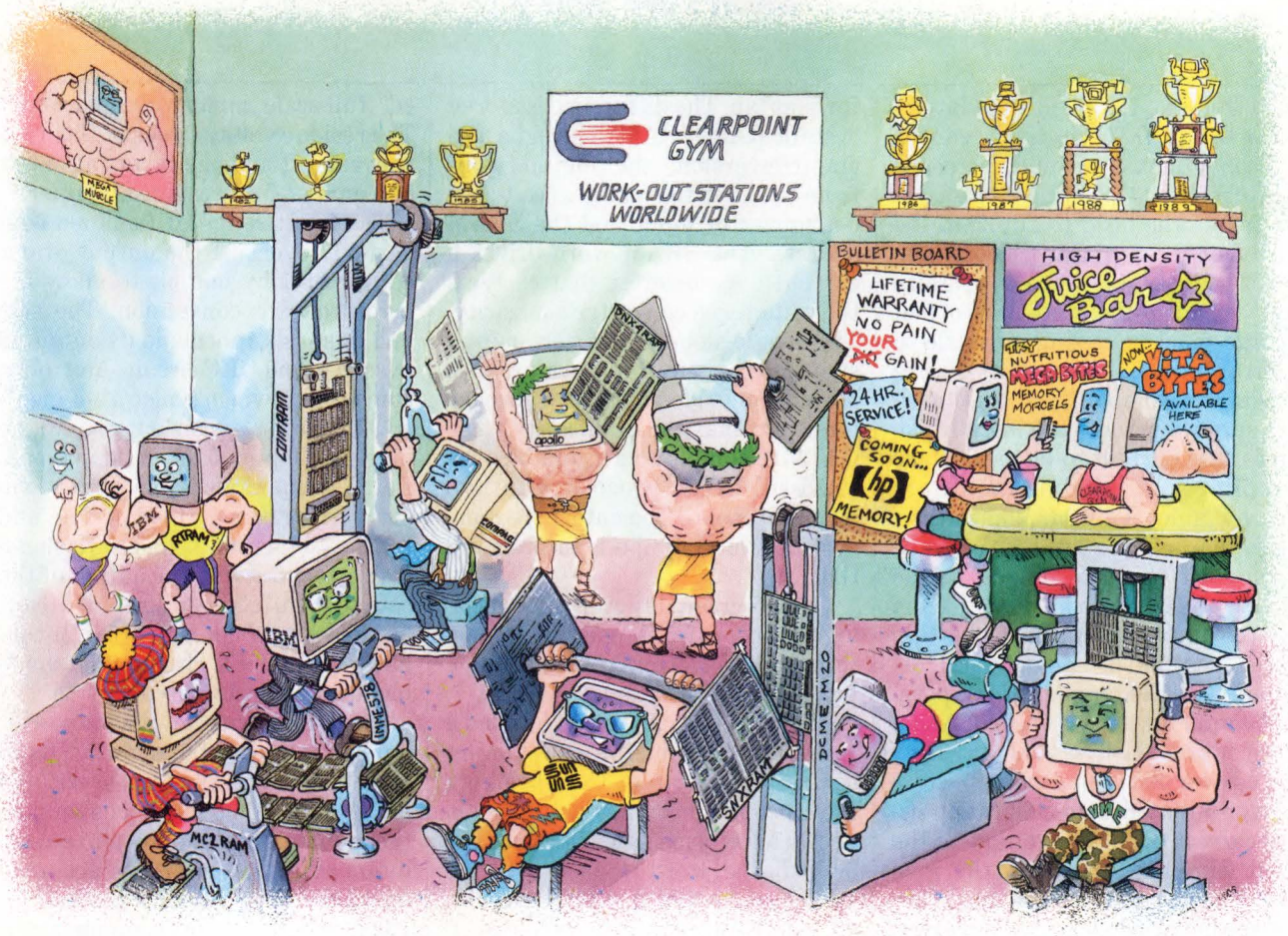

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word from the 13 (7 + 6) input bits.

The use of DEC circuitry reduces the conversion time and increases the effective throughput rate. It eliminates the need to autozero the flash converter's CMOS comparators. The time that's saved is significant because the autozero offset voltage must have time to settle to 12-bit accuracy. It also allows the use of simpler comparators that need less supply current, making it possible for the current to be used in the sampling and residue amplifiers where it's needed to maximize their speed. The use of a two-step converter for each 7-bit conversion cuts the total number of comparators from 128 to 32. If two flash converters were used, as in some hybrid designs, twice the number of comparators would have been needed. And a 12-bit pure flash would have required over 4000 comparators.

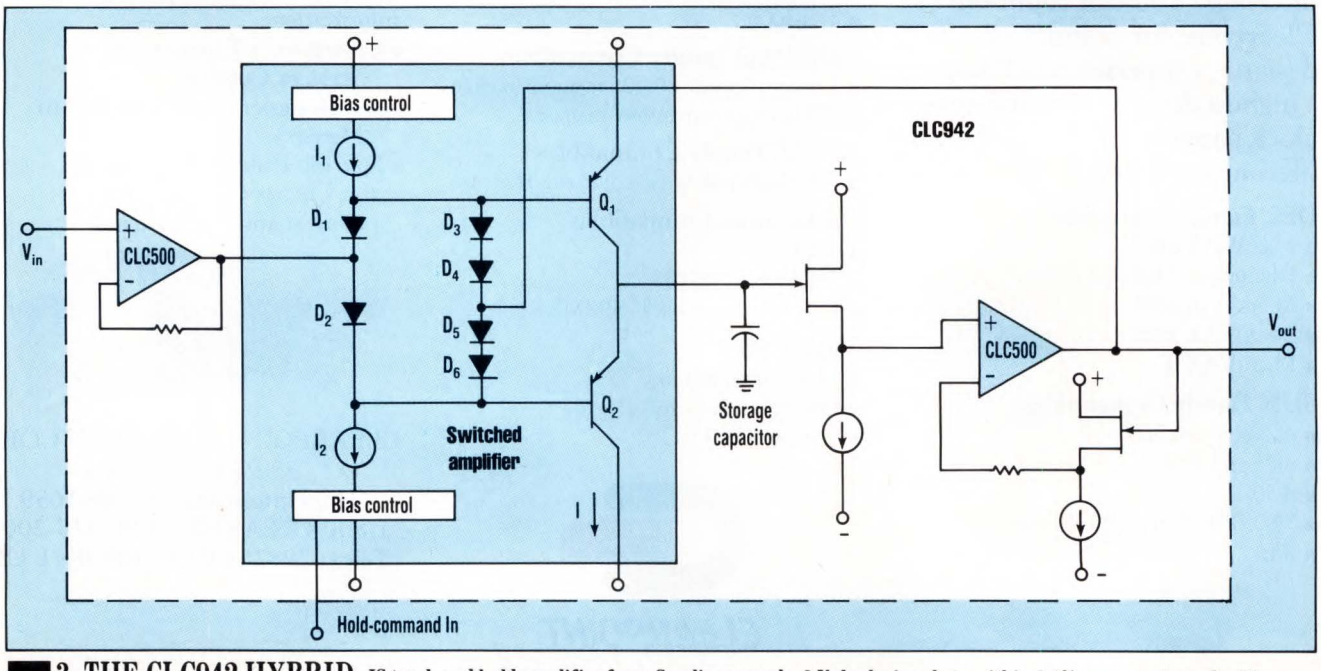
User-initiated auto-calibration cycles correct the offset voltage of the input sampling amplifier, the gain and offset of the residue amplifier, and the linearity of the d-a converter. An on-chip, single-slope, integrating a-d converter individually measures the voltage at each tap of the d-a converter. Each tap's digital word is compared with the word expected for that tap. The difference is stored in static RAM (SRAM). During a normal conversion, the digital word from the first flash step goes to the d-a converter input and the SRAM address. The SRAM word drives a current d-a converter that corrects the voltage d-a converter's linearity. The single-slope converter uses a switched-capacitor integrator with polysilicon-oxide-polysilicon capacitors, for maximum linearity. The CAT5412 is built on a 2-μm, bipolar-MOS-EEPROM process with two layers of metal. The cutoff frequency of its floating npn transistor is 3 GHz.

Doug Mercer, designer of the Analog Devices AD571, used four separate flash converters in four sequential steps in his product *(see Fig. 1, again)*. Thus, it can truly be called a four-step design. Internal timing controls its operation. Upon bringing the Encode pin high, flash a-d converter 1 performs its conversion. The 3-bit digital word is passed to the DEC circuits and to 3-bit, segmented, current-output d-a converter 1. The a-d converter's current runs through a resistor to the analog input. There, it's summed with the input, forming a residue voltage with a value less than 1/8 that of the selected, full-scale input voltage range. The residue voltage goes to flash a-d converter 2 and the inverting input of a gain-of-four residue amplifier.

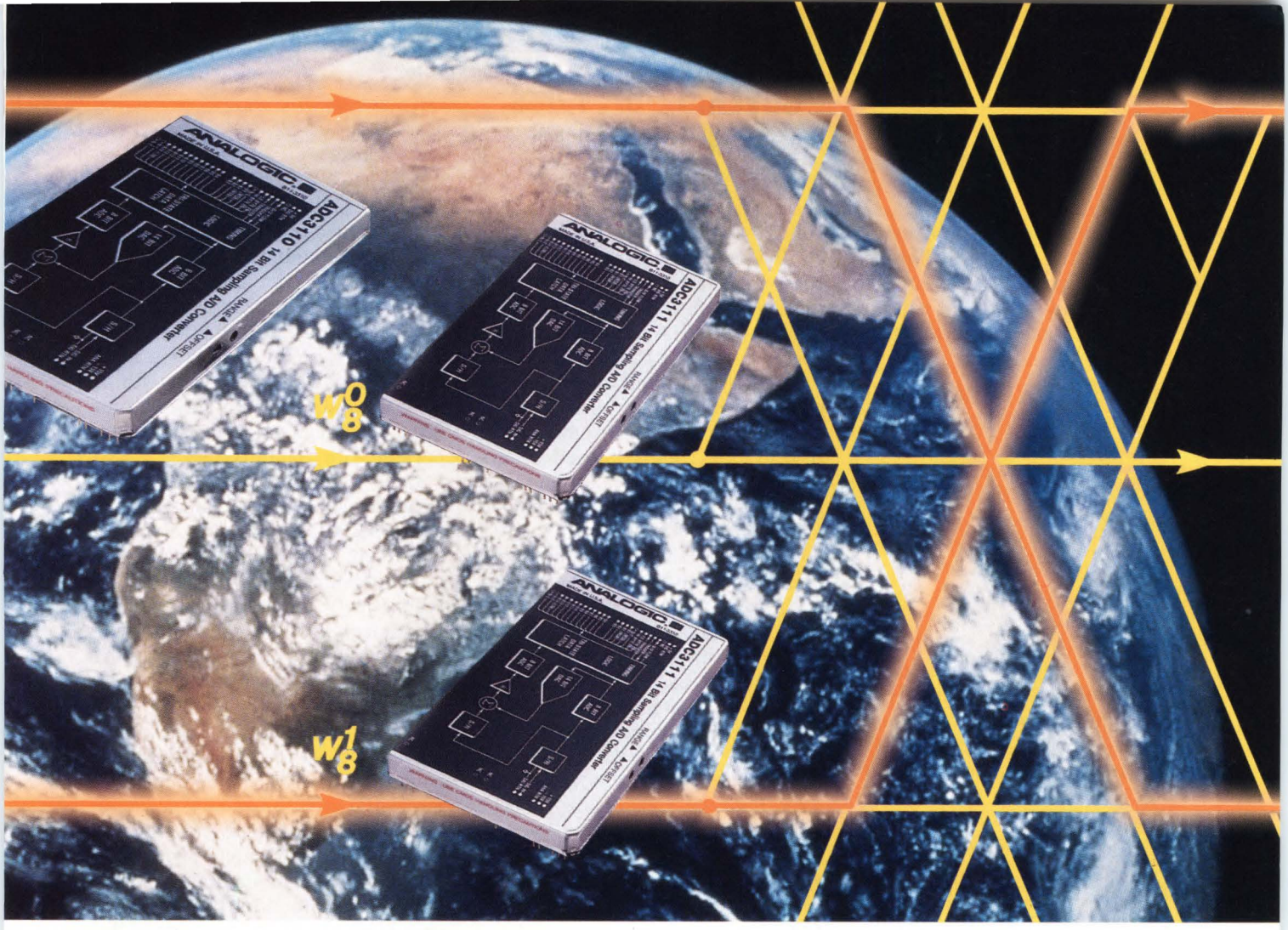
The input range of flash a-d converter 2 overlaps the output of d-a converter 1 by one bit to allow for errors during conversion. The second flash is strobed and its output is passed to the DEC circuits and to d-a converter 2, which is also a segmented 3-bit circuit. Its output goes to the inverting input of the residue amplifier. The amplifier connects to a two-step, 8-bit flash formed of fine and course 4-bit circuits, and to flash a-d converters 3 and 4. The output of the course flash (also configured to overlap one bit of d-a converter 2) connects to the DEC circuits and the 8-bit matrix-selector circuit.

The DEC circuit now has two overlap bits to create the eight MSBs to 12-bit accuracy, plus an overrange bit. At this point in the conversion, the input voltage is known to a resolution of 8 bits—to 12-bit accuracy (visualize the reference divider of a 12-bit-accurate, 8-bit flash converter: The 671 now knows the adjacent taps that the input voltage lies between on that divider).

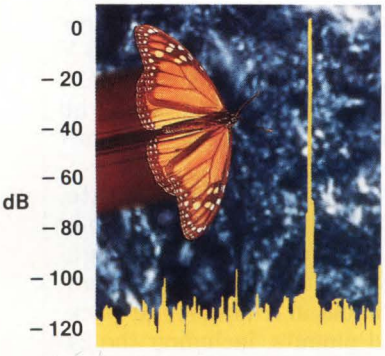
The 8-bit matrix selector chooses the appropriate set of fine taps which



3. THE CLC942 HYBRID, IC track-and-hold amplifier from Comlinear grabs 2-Vpk-pk signals to within 0.1% accuracy in under 24 ns, and to within 0.01% accuracy in under 31 ns.



Our A/D's Were Designed to Give You Butterflies*!



True 14-Bit Performance at a 2 MHz Sampling Rate

* *The illustrated flow graph of the Cooley-Tukey algorithm is known in the industry as a butterfly computation.*

Analogic's new, ultra stable 14-bit sampling A/D converters make the most of your post-processing computations. Using advanced hybrid and surface mount technology, these sampling A/D's provide the most cost-effective solution to your high speed, high resolution applications.

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span the course two taps the analog input lies between. The difference between the two voltages is equal to 1/256 of the full-scale input voltage. As with any flash converter, each voltage at the taps of a-d converter 4's divider connects to one out of the 15 comparator's inputs. The 671's original input voltage goes to their other inputs. The output of a-d converter 4 produces the four LSBs.

The AD671 is built on a 2.0-μm bipolar-CMOS process. Its floating, vertical npn transistors cutoff at 1.5 GHz. Lateral pnps, buried zeners, and laser-trimmed thin-film resistors (used in the reference dividers of the 671) are also available. The double-metal single-polysilicon process handles 10-V supplies.

Until Comlinear's CLC942 arrived, the fastest, 12-bit-accurate sampling amplifiers showed acquisition times of 50 to 200 ns, with prices in the range of $100 to $200 *(Fig. 3)*. While 10-bit-accurate samplers had acquisition times of 10 to 20 ns, their cost ran $200 to $400. (ELECTRONIC DESIGN, Sept. 22, 1988 p. 63). The $139 CLC942, with a maximum acquisition of 36 ns to within 0.01% (for a 2-V step and over the industrial temperature range), thus can't be touched for price or performance.

With the concurrent arrival of Vanguard's VN1025, the 10-bit arena may be more competitive *(Fig. 4)*. While the 942 takes a maximum of 32 ns to acquire a signal to that accuracy, the $109 VN1025 only takes 40 ns, albeit at 25°C. At that temperature, the 942 takes 24 and 31 ns, respectively, to grab signals 10- and 12-bit accurate. Typical aperture jitter for both devices is just 2 ps rms. The 942 drives a 100-Ω load while the 1025 drives a 50-Ω load, which is mandatory in some applications.

Both amplifiers have other similar specifications. The 942, with minimum full-power 3-dB bandwidth of 40 MHz and a minimum slew rate of 220 V/μs, shouldn't have any trouble sampling 10-MHz sine waves. In fact, the 942's circuitry is embedded in Comlinear's 12-bit 10-MHz hybrid a-d converter. The 1025 has a minimum full-power 3-dB bandwidth of 60 MHz and minimum slew rate of 300 μV/s, and a value at 125° C comparable with that of the 942.

Gain, gain nonlinearity, and gain temperature coefficient for the 942 are 0.993, 0.025%, and 40 ppm/°C, respectively. For the 1025, gain and gain nonlinearity are 0.99 and 0.01%, respectively; gain temperature coefficient isn't specified. Maximum full-scale signal for both amplifiers is ±2 V. For the 942, minimum feedthrough rejection (FTR) in the Hold mode with a 20-MHz 2-Vpk-pk sinewave input is –70 dB. Under similar conditions, the 1025's minimum FTR is –55 dB.

Input impedance of the 942 is 50 kΩ in parallel with 5.5 pF, while that of the 1025 is a minimum of 100 kΩ. This variable input resistance shouldn't cause you a problem, because circuit impedances at the frequencies of interest should be orders-of-magnitude lower.

The 1025 holds a significant advantage for operating at a high-temperature with relatively slow converters that need long Hold times. Its droop rate at 125°C is 12 μV/μs; that of the 942 is 100 times greater. Like all high-speed samplers, both have complex power needs. The 942 requires five supplies: ±5 V at 64 mA, ±5 V at 81 mA, and 11 to 15 V at 18 mA. The 1025 requires six, but they're all 5 V: ±5 V at 35 mA, ±5 V at 8 mA and ±5 V at 50 mA.

The monolithic, 10-bit-accurate, Vanguard VN1025 THA is a drop-in replacement for a number of high-speed hybrid sampling amplifiers. It's available in a number of packages and pinouts, including the 24-pin double-width metal and ceramic DIPs employed by the Analog Devices HTC0010, the Burr-Brown SHC601, and even the 12-bit Vanguard CLC942. It will also be available in single- and double-width, 18-pin ceramic DIPs, 24-pin SOICs, and 24-pad leadless chip carriers.

PRICE AND AVAILABILITY

In quantities of 100, unit prices of the Catalyst CAT5412 in its 40-pin double-width ceramic DIP range from $98 each for the lower commercial-grade units to $260 each for the military version.

Catalyst Semiconductor, 2231 Calle De Luna, Santa Clara, CA 95054; Krish Panu, (408) 748-7700. **CIRCLE 515**

Analog Devices' AD671, in its 24-pin side-brazed "skinny DIP," runs from $95 each for the commercial (J) models in quantities of 100. Samples are available from stock.

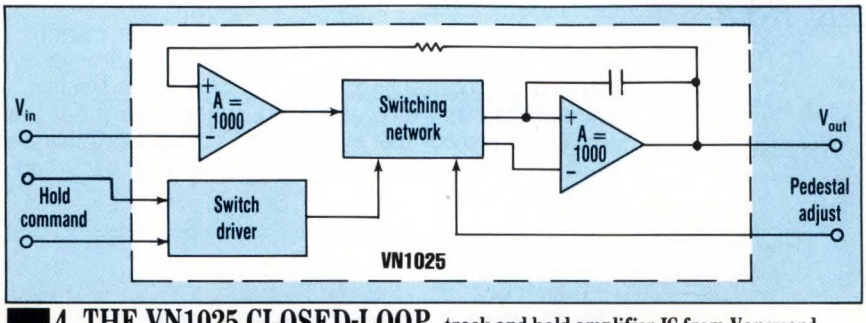
Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; Paul Errico, (508) 658-9400. **CIRCLE 516**

The commercial model of the Vanguard VN1025 runs $109 each, the military model $249 each in quantities of 100.

Vanguard Semiconductor Corp., 211 Topaz St., Milpitas, CA 95035-5430; Steve Pass, (408) 946-9111. **CIRCLE 517**

In its 24-pin ceramic double-width DIP, the Comlinear CLC942AI (industrial model) runs $139 each in quantities of 100. The military (AM) model costs $274 each in similar quantities.

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; Wayne Lownowski, (303) 226-0500. **CIRCLE 518**



4. THE VN1025 CLOSED-LOOP, track-and-hold amplifier IC from Vanguard Semiconductor acquires 2-Vpk-pk signals to within 0.1% accuracy in 40 ns maximum.

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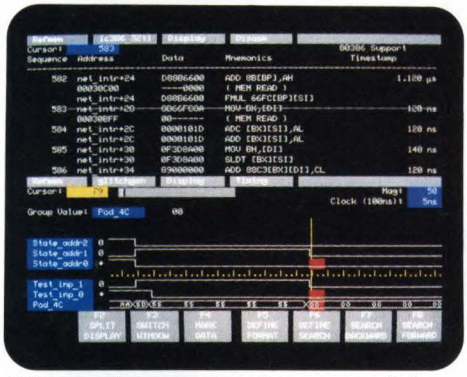

Split screen displays can show microprocessor activity time correlated with high-speed timing data (above) or disassembly of another microprocessor. The cursors can be locked to scroll in parallel, highlighting data nearest to the same point in time.

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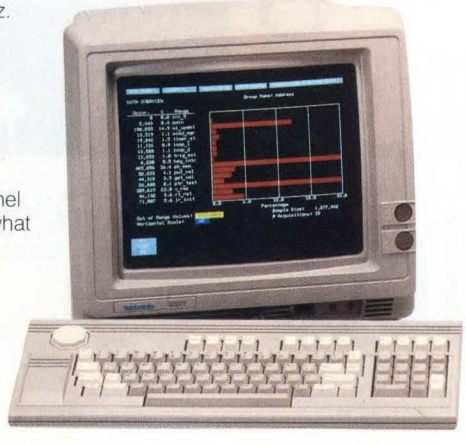

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COVER: 12-BIT ADCs, SAMPLING AMPS

Comlinear designer Kurt Rental is credited with designing the fastest 12-bit-accurate THA in the CLC942. It's also the only one with an open-loop design that's 12-bit accurate.

The Vanguard device, designed by Mehrdad Nayebi, is by far the fastest closed-loop IC design. While acquiring or tracking a signal, a transconductance buffer amplifier drives an integrating amplifier through a switching network—all inside a closed feedback loop. Both amplifiers achieve 60 dB of open-loop gain (to ensure 10-bit accuracy) with folded cascode circuits. Closing a unity-gain loop around 120 dB of gain supplied by 1-μm MOSFETs and npns with an f_T of 7 GHz—without creating an oscillator—is an indication of the design's sophistication. An n-channel MOSFET, with bipolar transistor clamps on the output, opens the loop to put the circuit into Hold.

Though Comlinear's 942 doesn't enclose the storage capacitor in the feedback loop, it still achieves 12-bit accuracy. The circuit consists of a high-speed, precision op amp (Comlinear's CLC500) connected as a closed-loop unity-gain buffer. It charges the storage capacitor through a custom, switched-amplifier IC. The charge on the capacitor is buffered by a discrete JFET follower which drives the output buffer (a second CLC500). Its feedback loop is closed through a second discrete FET. Laser-trimmed, thin-film resistors set the gain.

When the 942 is tracking its input, the two current sources (I_1 and I_2) are each passing about 3 mA through diodes D_1 and D_2. In turn, the diodes are biased on, turning on transistors Q_1 and Q_2. The transistors are the same size as the diodes and thus pass similar currents. This class-B amplifier stage supplies a low-offset drive for the storage capacitor. Its input impedance is higher than a simple diode bridge. A current gain of five is achieved, giving the circuit its 300-V/μs slew rate.

Bringing the Hold input high reverses the direction of the current sources. Current now flows through diodes D_3 through D_6. D_1, D_2, and the transistors are biased off, putting the 942 in Hold. Connecting its output voltage to the diodes keeps a constant reverse bias on the transistors and forces a repeatable voltage step on their bases. This step causes unwanted charge dump onto the storage capacitor, creating the Hold pedestal. A constant step results in the constant pedestal level required for 12-bit accuracy.□

HOW VALUABLE?	CIRCLE
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MODERATELY	570
SLIGHTLY	571

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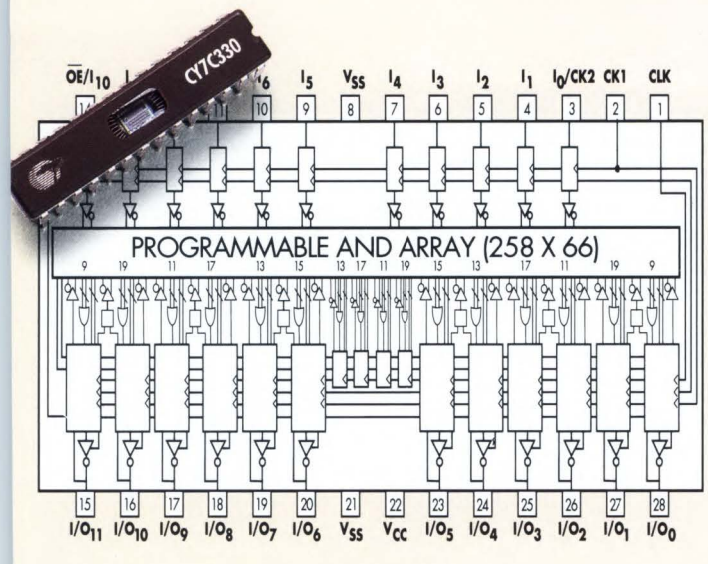
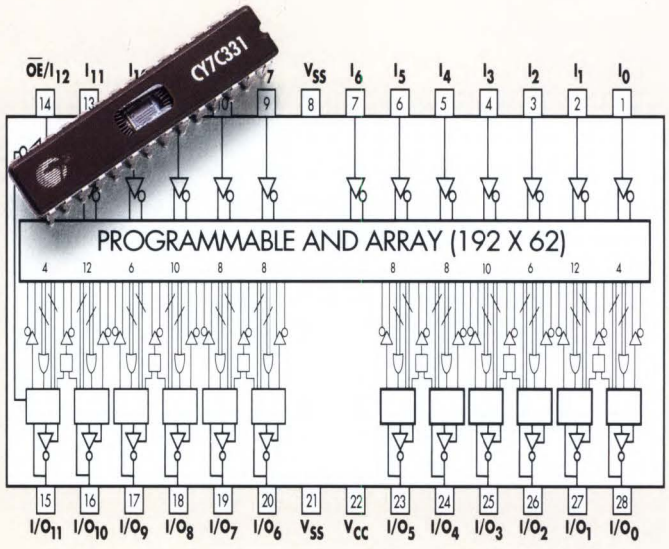


CY7C330
66 MHz Synchronous State Machine PLD



CY7C331
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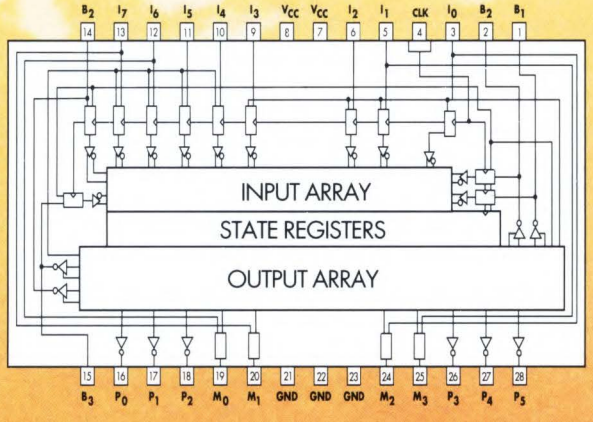
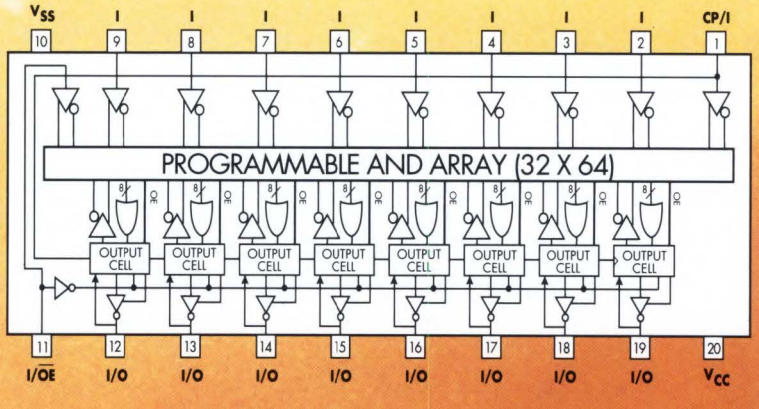
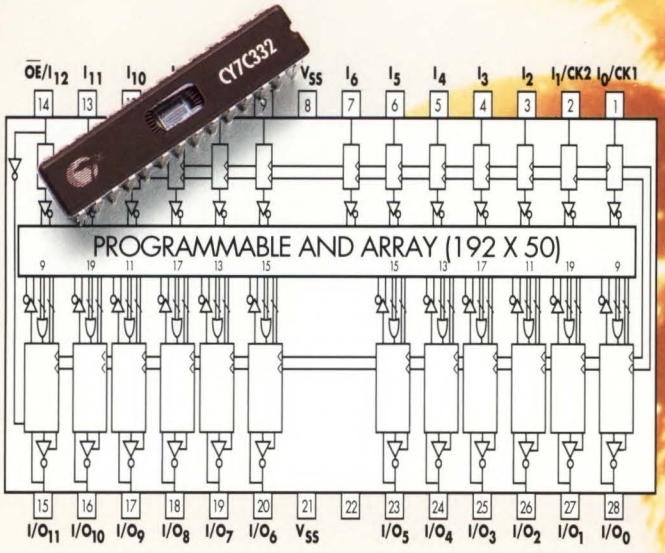




CY7C361
125 MHz Ultra High Speed
State Machine EPLD

CY10E301
2.5ns ECL PLD



CY7C332
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Reprogrammable Ultra High Performance PLD.

speeds to 125 MHz.

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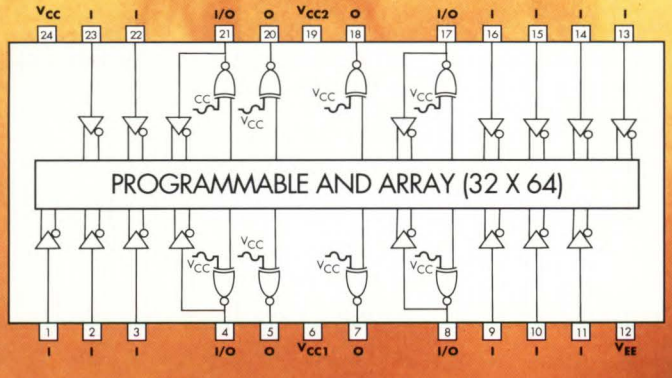
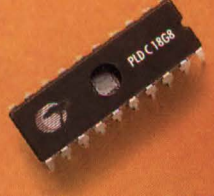
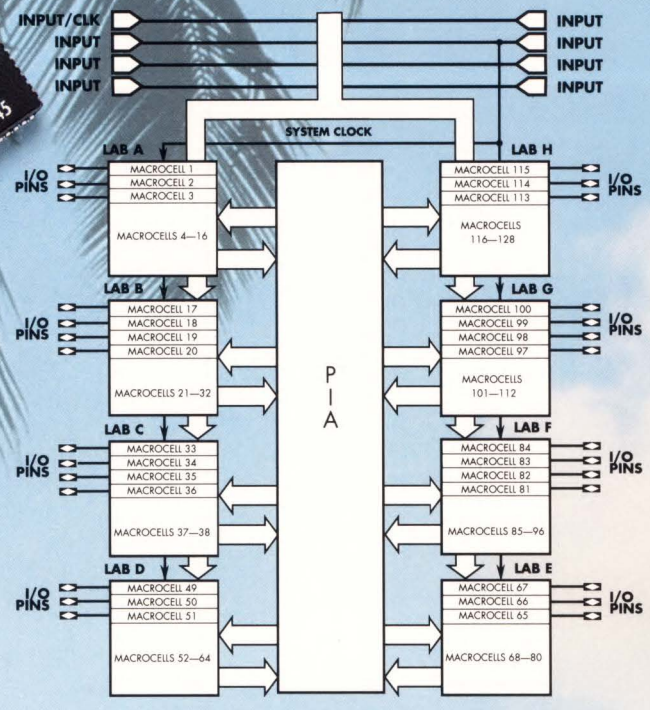




PLD C 18G8
12ns Universal 20-pin Programmable Logic Device



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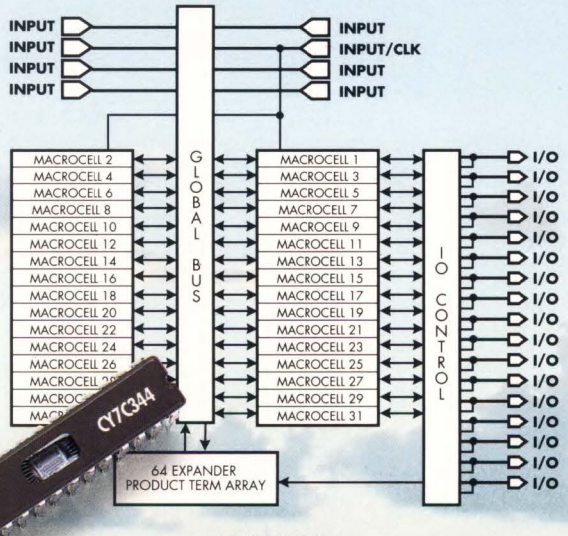
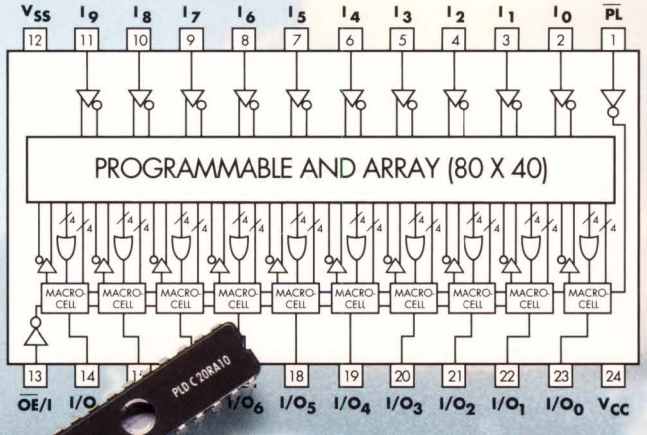
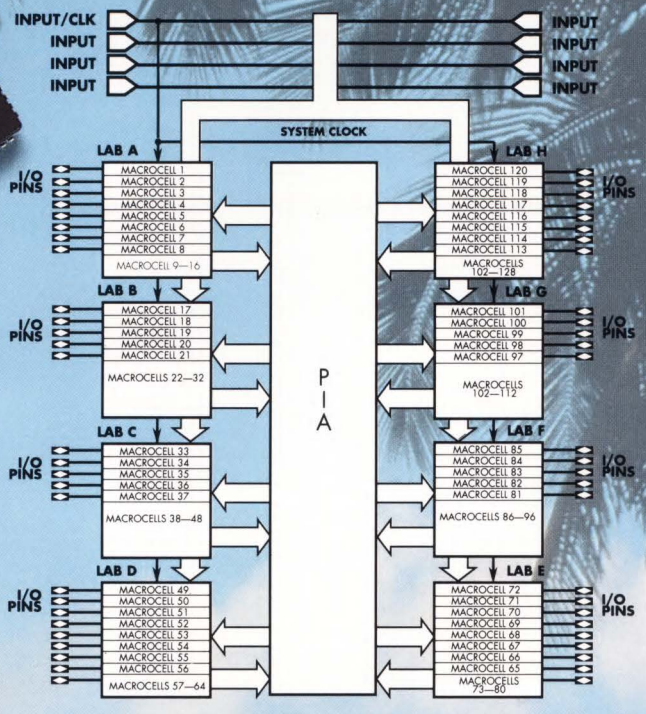


CY7C344
20ns 32 Macrocell MAX PLD

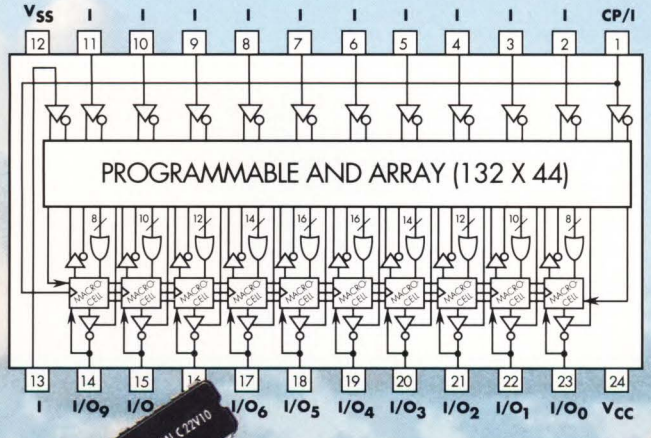


PLD C 20RA10
20ns Asynchronous PLD



CY7C342
30ns 128 Macrocell MAX PLD

speeds to 50MHz.



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MAX FlipFlops	32	64	128	128
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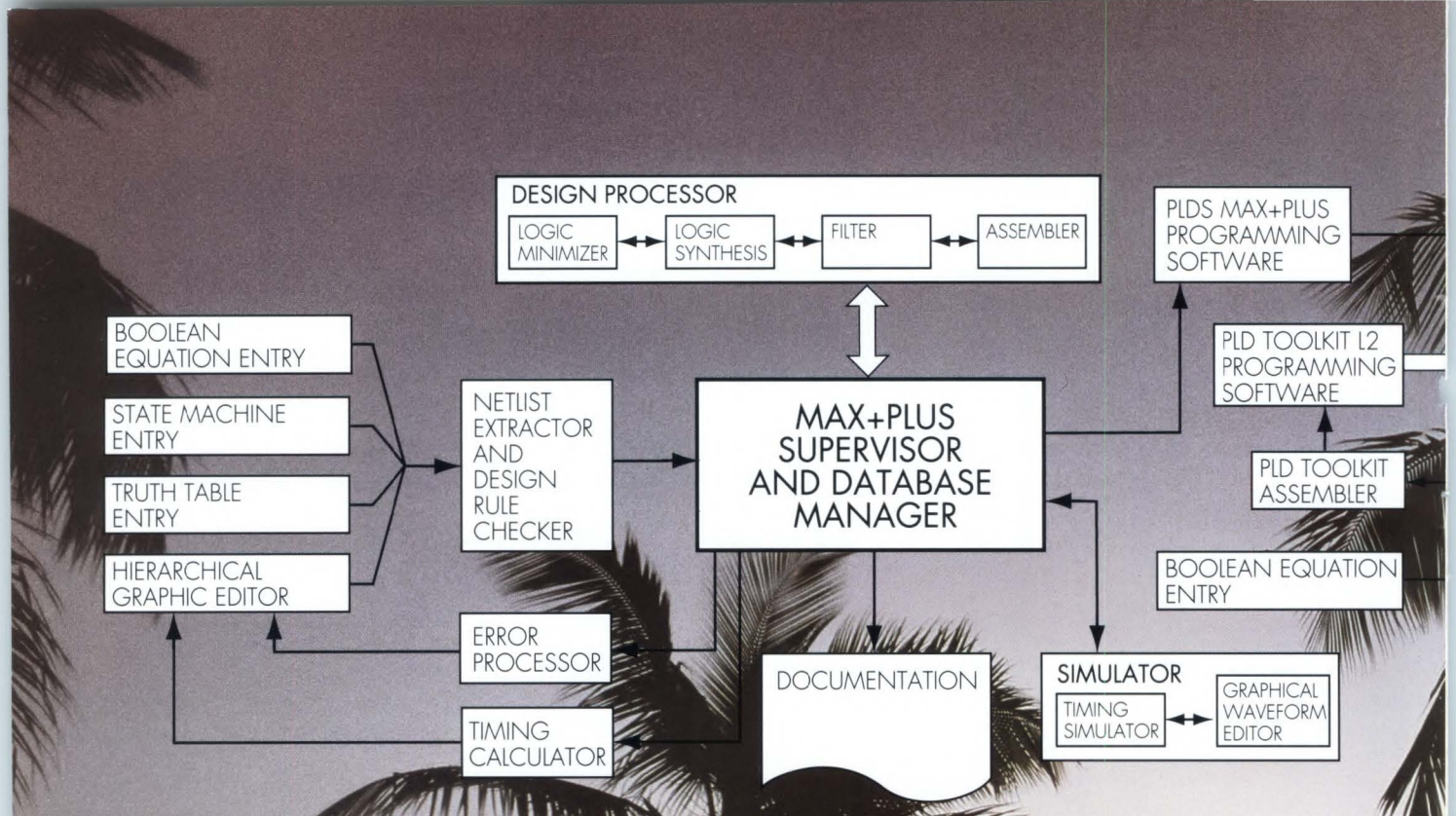

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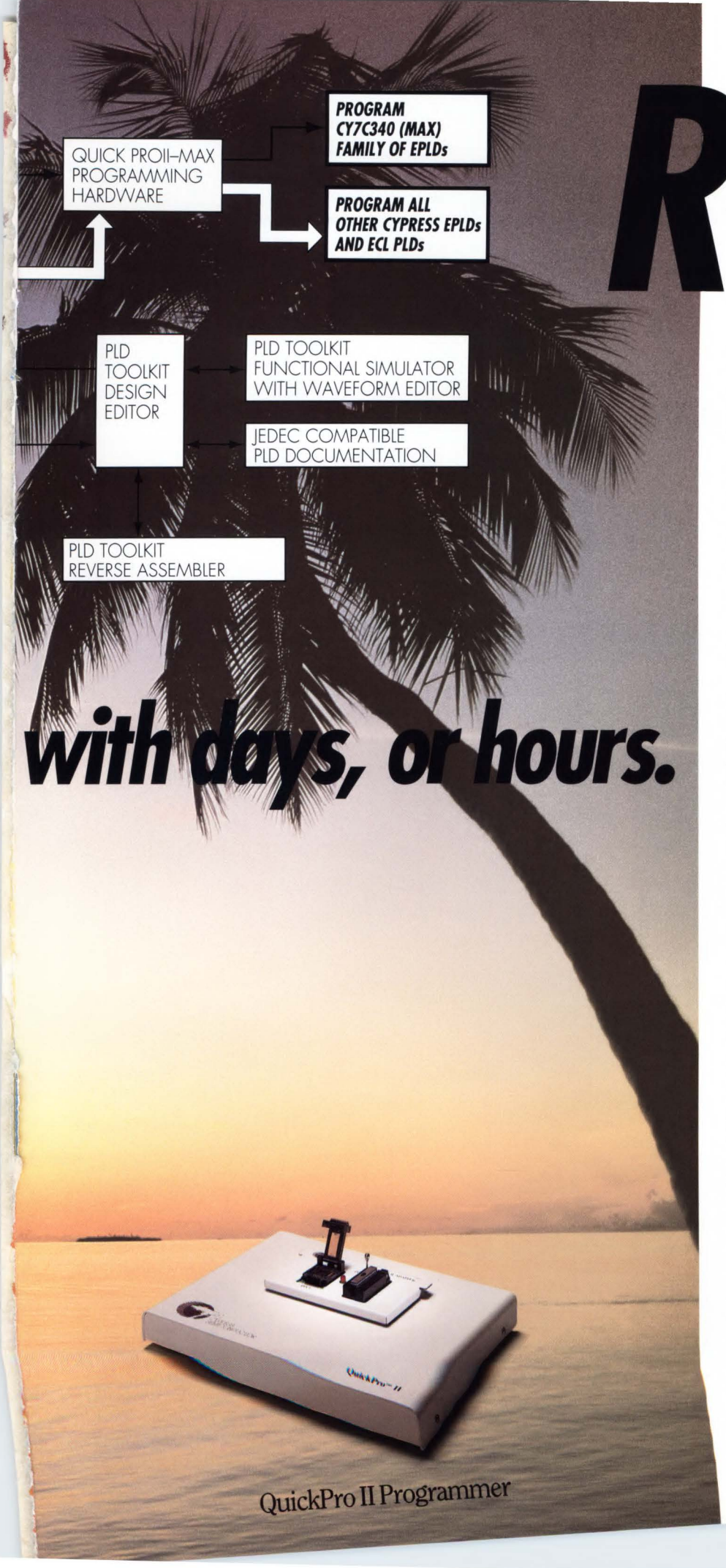

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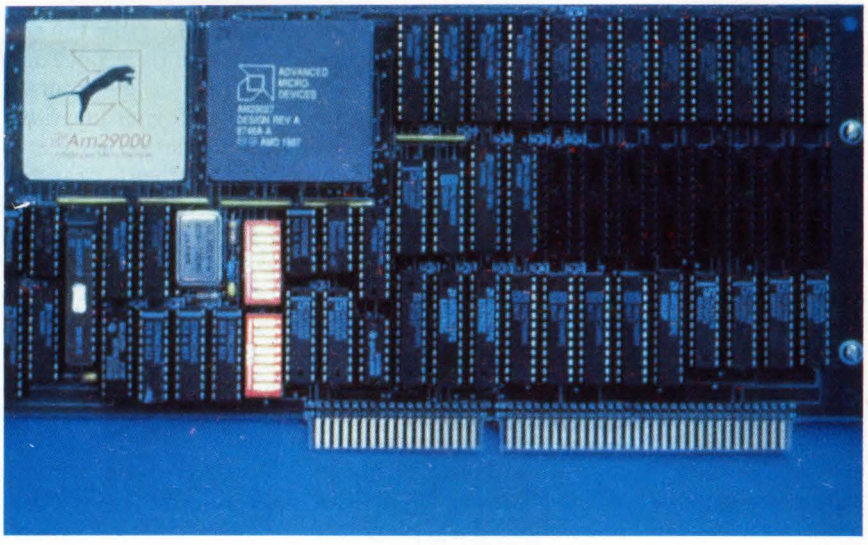


THE PROBLEMS OF RISC-BASED DESIGNS

LISA GUNN

EFFICIENT MEMORY DESIGN IS THE KEY TO EXPLOITING THE ASSETS OF RISC CHIPS.

Reduced-instruction-set-computer (RISC) processors have flourished in the performance-hungry electronics industry. Whether powering a workstation or a laser printer, these processors supply the raw MIPS needed by many of today's designs. However, while a RISC chip's speed increases processing capabilities, it also increases the number design problems. Requiring the CPU to receive a new instruction every 40 or 50 ns puts a strain on memory design. The fastest RISC chip is only as efficient as the system it's built into.

Evolving from complex-instruction-set-computer (CISC) processors, RISC processors might have been more appropriately named streamlined-instruction-set architecture: The objective in designing RISC machines was to streamline the CISC instruction set to include only the instructions needed to most efficiently do a computer's work. The differences between RISC and CISC processors don't have much impact on overall system design. The only real disparity is in the memory requirements—the speed of the RISC processor is much more demanding on the memory. But it's clear that RISC and CISC processors are beginning to merge, with each adapting qualities of the other. Design issues don't address the debate of RISC vs. CISC, but rather how to keep up with faster machines.

Traditionally, CISC processors have used microcode to implement the instruction set because the memory interface was slow. RISC technology, however, takes a different approach. Performance is looked at from a compiler perspective: How many instructions actually get used? The microprocessor instruction set was redefined to contain only those instructions that were frequently used by the compiler. The purpose was to implement the instruction set so that any instruction could be executed in one cycle.

Because RISC processors execute basic building-block instructions faster than CISC machines do, they can execute many more instructions per second. Consequently, RISC processors need to be fed those instructions at a much higher rate. The same principle applies to data. In most cases, a very large, very fast main memory isn't feasible, so performance rests on good cache design.

There are three basic differences between RISC and CISC processors that affect system design issues. First, RISC architectures use a load-store type of execution. Only load or store instructions can go out to main memory through the memory bus. CISC architectures use a register-model type of execution. For example, a CISC add instruction may add a quantity from a certain memory location into a register. Inherently there is a load operation buried in that CISC instruction, because the operands must first be loaded before performing the add. In a RISC processor, the load operation is decoupled from the data-processing operation.

The second difference is that RISC processors have a non-destructive-register model of execution, and CISC processors use an accumulator model of execution. Nondestructive means that the architecture preserves data until the user wants to get rid of it. For example, a RISC machine add instruction would be between any two source operands into any destination register. The add operation wouldn't destroy information as a byproduct of the source-operand fetches. The processor may add the contents of register B to the contents of register C, and store the results in register A.

The CISC processor, on the other hand, accumulates into register A the contents of register A added to the contents of register B. The CISC add operation basically destroys what existed in register A before that operation.

There are naturally occurring stalls in the instruction flow of a processor. For instance, it may take several clock cycles from when a load instruction is issued until the data actually arrives. Another example of a stall is when a cache has a branch-delay slot that can't be filled.

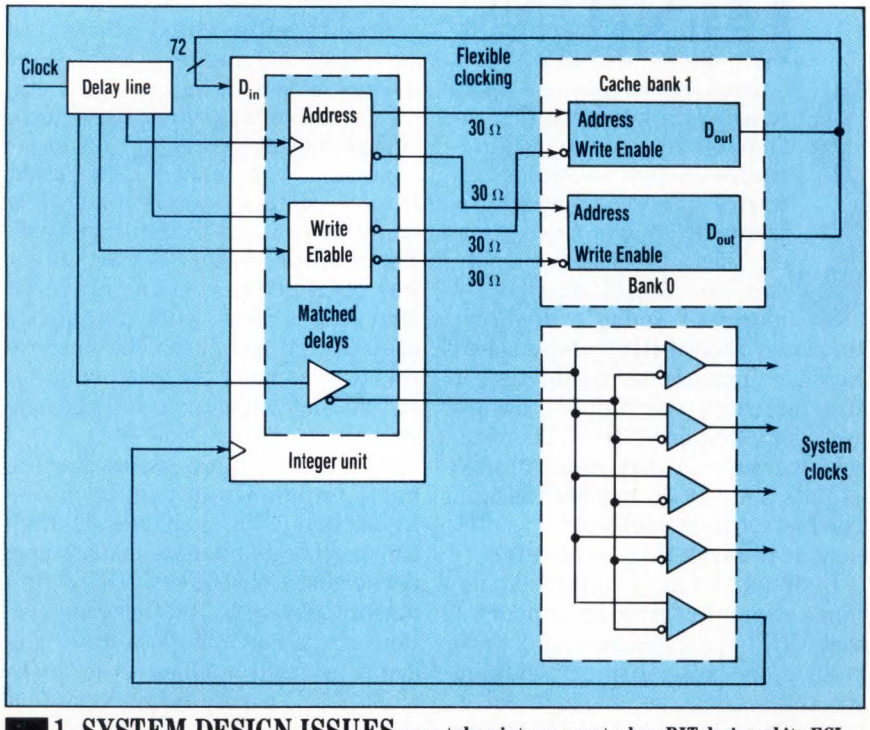
The best design would fill those naturally-occurring stall slots with useful instructions. This can occur only if the useful instructions aren't data dependent, or dependent on data that's being waited for. RISC designs can fill these empty slots because the processor is a non-destructive register model. The code can be reorganized because information is preserved. The compiler checks for data dependencies when this type of rearrangement occurs. Because CISC machines are a destructive model and destroy information, their instruction flow is location sensitive. In addition, load and store operations couldn't be rescheduled because they're essentially buried within other operations.

The last difference between the two processor types is that RISC chips have fixed-length instructions and CISC chips have variable-length instructions. In RISC, all of the encoding is in 32 bits of information. The benefit here is that decode time is shorter and decode circuitry is simpler.

When a 32-bit RISC instruction is fetched, the whole instruction is there. With variable-length CISC instructions, it can take from two to eleven fetches to obtain a whole instruction. Because RISC machines use fixed-length instructions, instruction fetching and decoding can easily be parallelized. In other words, RISC exploits fine-grain parallelism.

"The real issue isn't one of RISC vs. CISC, but of balanced system design," says Jim Peterson, design engineering manager for Bipolar Integrated Technology Inc. "The performance of the system elements must match the performance of the processor." Differences in RISC- and CISC-based system design are highly dependent on which RISC processor and which CISC processor is used. The bottom line is that once any processor goes above a certain performance mark, cache memory is a necessity for adequate data input. As Steve Goldstein, director of marketing at Ross Technology Inc., puts it, "If an engine is running faster, you have to feed it more gasoline. A RISC processor is a finely tuned engine that needs more gasoline than other processors do."

One of the highest-performance RISC chips is Bipolar Integrated Technology's (BIT) ECL Sparc chip. The ECL part runs at 80 MHz. How does a designer handle such speed? "It's easier to design an ECL system at 80 MHz than it is to design a CMOS system at 40 MHz," answers Peter-



1. SYSTEM DESIGN ISSUES were taken into account when BIT designed its ECL Sparc processor. Matched delay paths mean that a 12.5-ns cycle time can be treated as a 15-ns cycle time, and the processor achieves peak speed with slower memory.

son. For a CMOS design running at 40 MHZ, there's always a critical path in the system where I/O speed isn't up to par due to chip-crossing delays.

ECL designs take into account the transmission-line nature of all board interconnects. BIT's parts have clocked output delays of 3.5 ns across a 32-bit address bus with 30-Ω address drivers *(Fig. 1)*. In addition, ECL has smaller voltage swings.

In addition, BIT worked very closely with Sun Microsystems on the system aspects of the chip design. Sun specified the skew on the address line going to the cache to allow an early clock for the cache register. Depending on how early the clock is put on a cache's address register, a 12.5-ns system could make possible somewhere between 14.5- and 16.5-ns cycle equivalents for a cache access. This significantly reduces the speed of the required cache.

Many RISC processors now have on-chip caches. A big issue with on-chip cache is the chip architecture itself. Many CISC chips that have on-chip caches have poor interfaces to the outside world, and it may take longer than one clock cycle just to get an address off the chip. But as RISC chips add on-chip cache, they'll still maintain their very fast interface to the outside world and you'll see a tremendous performance increase. It's very important to system design that the RISC chip have a good interface to the outside cache.

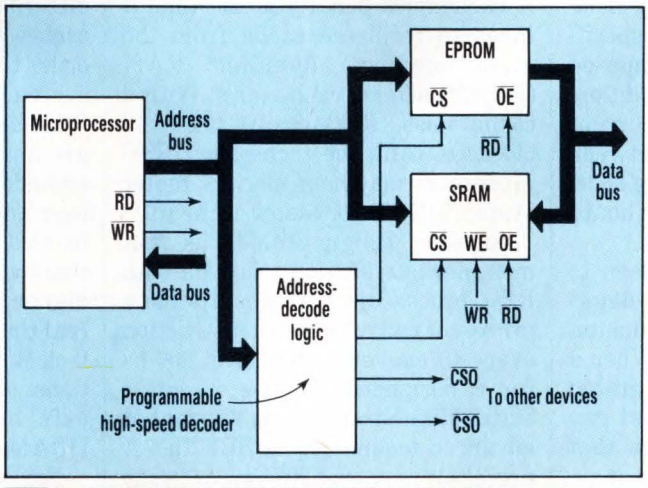
Historically, once processors began running at 16 MHz, a cache was needed because the logic elements could cycle much faster than memory could be accessed. Now that processors run at 33 MHz, some manufacturers have even put the cache on the chip. For instance, the 68040 and 80486 each have a small on-chip cache. The Sparc chip set supplies 64 kbytes of integrated cache. The MIPS Computer Systems' architecture requires a discrete cache subsystem. Therefore, differences in RISC- and CISC-based system design depend on whether or not a particular processor has an integrated cache, and just how big that cache is. For a RISC chip to sustain high performance, it needs 64 kwords of 32-bit cache to get a reasonable hit rate.

Fast RISC machines have a greater need for high bandwidth into the execution units than CISC machines do. Consequently, it follows that a RISC machine is more in need of an integrated cache than is a CISC processor. Discrete caches that run above 33 MHz are tough to build anyway. A cache like that requires 12-ns static RAM (SRAM).

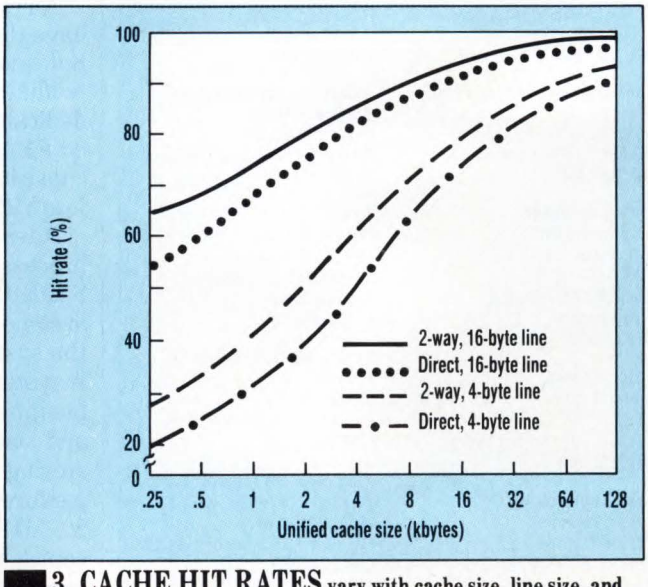
"A RISC processor must have a lean, clean, and mean cycle relationship with its memory," states Jesse Jenkins, applications manager for Signetics Co. "That is really tough when the speed of the memory is exactly the same as the speed of the processor. There is no fat in your budget."

Implementing the processor-to-memory interface as simply and straightforward as possible is the key to getting the performance out of the processor. The goal is to get SRAM with 20–35 ns access times to sustain RISC processors running at 25–33 MHz. Price goes up dramatically as the 20-ns access time is approached. On the board, parasitic capacitances and lead impedances add multiple ns delays that designs can't afford. System memory must therefore be carefully matched to the speed of the processor and to the board impedance.

In addition, most likely there will be multiple memory modules, and the processor must be able to point at one and distinguish it from all the rest in almost zero time. The memory itself requires a certain amount of time in each cycle to produce the desired data. A new Signetics product line, called programmable high-speed decoders (PHDs), recognizes these facts, and interfaces between the processor and the memory to minimize the time that's



2. A PROGRAMMABLE HIGH-SPEED decoder is ideally suited to interface with a RISC processor. The devices performs address decoding on 16–44 address bits in just 5–8 ns.



3. CACHE HIT RATES vary with cache size, line size, and set associativity.

required in selecting memory modules *(Fig. 2)*. These parts have specific time-delay requirements imposed by RISC processors. In addition, they have the necessary current drive to charge up the metal between the PHD part and the memory so as not to lose time delay into the board capacitance.

"Cache architecture has risen to be the largest performance-determining factor in a RISC implementation," says Steve Goldstein. When a processor does have an integrated cache, a system designer must pay attention to the physical bus that goes from the cache to the main memory. The cache-hit ratio, or the percentage of correct data from the primary cache, is a very important feature. So is the cache-miss penalty. Designers want a low cache-miss penalty on a RISC machine *(Fig. 3)*. A cache-miss penalty is the time it takes to refill the cache from the main memory dynamic RAM (DRAM) after a cache miss. With a cache miss, it typically takes 15 clocks to refill the cache line. RISC processors may need slightly faster system DRAM for faster cache fill.

Another design problem is that most peripherals don't fit well with RISC processors. "It's absurd that a processor can execute an instruction every 40 ns, yet it must wait 300 ns for a peripheral to give it data," states Mike Strang, vice president of advanced technology at SBE Inc. A processor may wait 20 clock cycles to access an 8-bit peripheral. It could have been executing 20 instructions.

The memory requirements of a RISC-based system differ according to the application. Embedded-control systems and workstations have very different needs. Workstations need caches and memory management in order to efficiently run an operating system and applications.

Embedded control isn't as programmable as workstations are. The embedded CPU runs one application over and over again. Therefore, embedded designs can use less memory than workstations need, but need higher performance because of the real-time nature of embedded control. With embedded-control applications, designers may make tradeoffs between using SRAM and DRAM on a basis of speed and price.

For some of the more simple embedded applications, all that may be needed is an integer-unit processor hooked up directly to main memory. Other, more complex embedded tasks may require more memory and memory management than that. In a robot, for example, several processors may work together—memory management is then needed to coordinate the processors' accesses.

Another difference between designing for embedded-control applications rather than workstations is that in embedded control you need to worry about interrupt latency. Some of the chips designed for workstations have much simpler interrupt latency and context-switching capabilities than those designed for embedded control applications.

An embedded application may not have the conventional type of cache, but may have very fast memory holding the code. If a system runs a dedicated application set in dedicated SRAM, it doesn't need cache because it can put the entire application into 512 kbytes of RAM.

Advanced Micro Devices' 29000 processor is designed for use in embedded systems. It has 192 registers, in some cases enough storage so that the system doesn't need data RAM. A system could have very high-speed peripherals and instruction RAM and use the internal registers for storing data, yielding a very high-performance board that runs close to 20 MIPS. The instruction stream comes in on a burst mode from inexpensive RAM.

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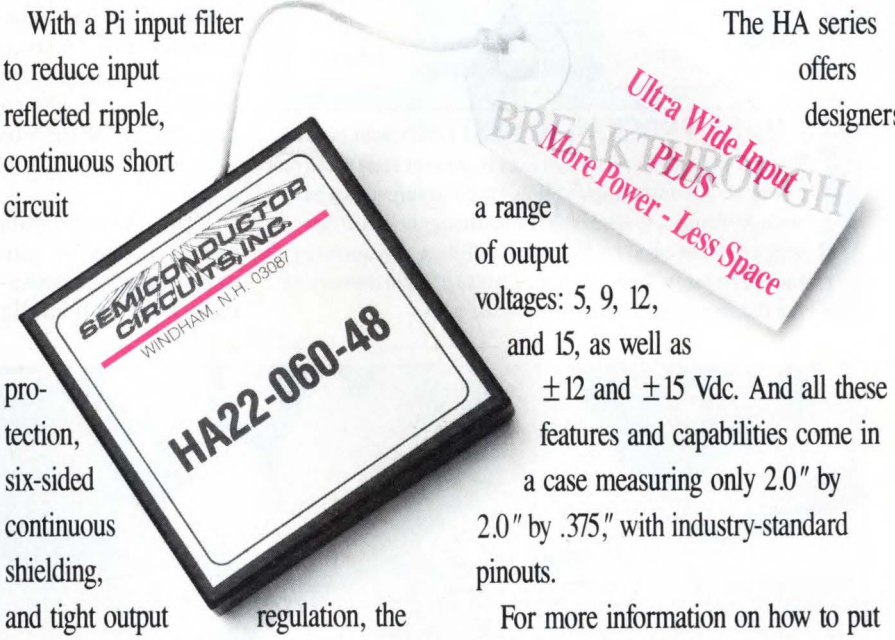

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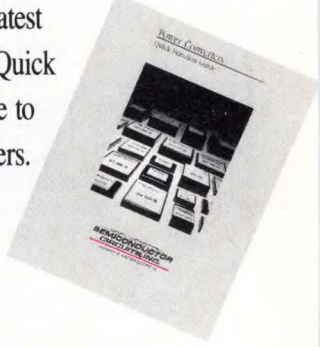

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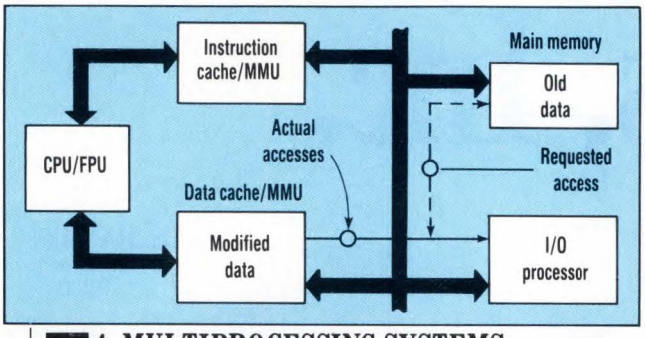
CIRCLE 23

even more demanding on memory design. Single-launch instruction machines will quickly go to multiple-launch instruction machines, called superscalar architectures. These architectures dispatch multiple instructions from a standard instruction stream in a given clock cycle, yielding a cycles-per-instruction ratio of less than one. These new processors will have multiple execution units on the chip, much like the i960CA from Intel Corp.



4. MULTIPROCESSING SYSTEMS must have an effective method of cache coherency to prevent stale data from causing errors. Intergraph's Clipper architecture uses a bus-watch mechanism to ensure data consistency between the cache and main memory. Bus watch fulfills read requests by other bus masters from the cache instead of main memory, in case the data in each location is not the same.

To launch more than one instruction per clock cycle, the system requires a sustainable high bandwidth, which means a good cache architecture. A reasonable transistor budget is needed to get the cache size to sustain that bandwidth.

"The future holds much more in the area of multiprocessing, both internally and externally," says Clara Serrano, 88000 applications manager for Motorola. Cache becomes a much more important issue when multiple processors are involved. Multiprocessing needs to maintain cache coherency *(Fig. 4)*.

Motorola's 88000 chip set took all of this into account. With multiple processors running, each monitors the activity going in and out of the caches automatically to see if there is the problem that one processor is using data that was modified by another processor. The hardware snoops to see what is happening in the other cache/MMUs to guard against any problem with old or stale data or dirty data.□

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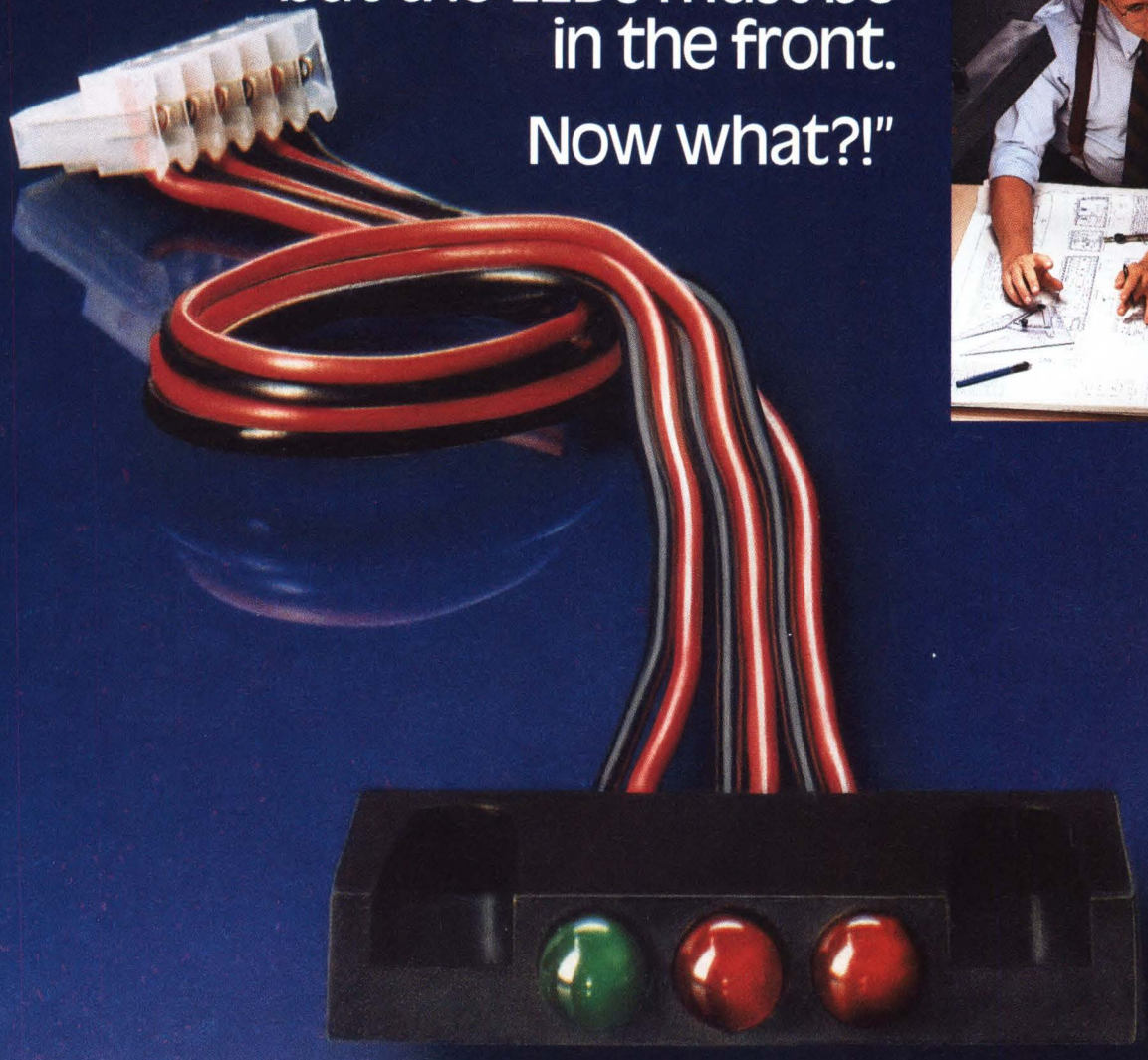

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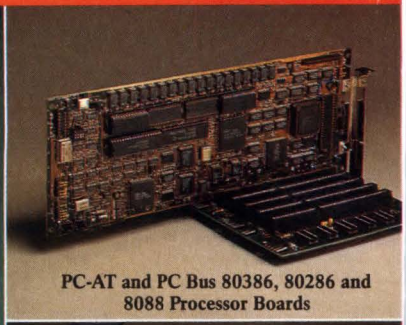

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Five years ago, engineering workstations were limping along at a throughput of 0.5 MIPS. Today, such processors as the 80486, 68040, and 88000 muster from 13 to 18 MIPS, which translates into 5 to 12 MFLOPS or 30,000 to 50,000 Dhrystones. If the trend persists, 1000 MIPS will be reached on a workstation well before the millennium turns (ELECTRONIC DESIGN, Jan. 8, 1987, p. 91, *Fig. 1*). Assuming that the software matches the hardware, the number-crunching throughput can approach 1 GFLOP.

However, single processors can't readily be pushed beyond a GFLOP, because at the speed of light, only a billion data packets can pass through a 1-ft. box each second. Though one GFLOP may seem to be all that's needed from a workstation, appetite continues to outrun available means. Only parallel processing can open the gates to even larger throughputs. Consequently, it comes as no shock that parallel processing has vigorously advanced from a hot research topic into a plethora of products (ELECTRONIC DESIGN, May 25, p. 41).

Most commercial multiprocessors still work with shared memory, where monitoring the flow of execution poses a challenge but remains manageable. However, this architecture tends to saturate once the processing elements (PEs) reach a few dozen. More complex architectures, such as hypercubes or tree structures, remain viable into the thousands of PEs and are rapidly gaining favor. The Department of Defense's Defense Advanced Research Projects Agency (Darpa), for example, is funding a program that uses Intel's hypercube (eventually with 2048 PEs) and presses the 80860 "Cray on a chip" into PE service (ELECTRONIC DESIGN, May 11, p. 23).

Cogent Research Inc., Beaverton, Ore., typifies the efforts that are made in the private sector with a desktop system that incorporates up to 400 Transputers and yields over 45 MFLOPS. In Europe, an Esprit project is underway that aims at 1 GFLOP from several hundred PEs. There's no doubt that multiprocessing holds the key to the future, but software for these megamachines remains a tough nut to crack (ELECTRONIC DESIGN, May Special issue, 1987, p.27).

Vectorized programs for array processing are the easiest to handle. Arrays and their building blocks (vectors) dominate in the "hard" sciences, where most of the demand for parallel number-crunching originates. Consequently, vector and array processors have existed for decades, as have vectorizing compilers

PARALLEL PROCESSING

that hunt for Fortran DO loops. This type of parallelism is known as synchronous multiprocessing.

Recent multiprocessors aim higher, ideally for universal employment. Massive sorting and ray-tracing graphics typify one major branch on the multiprocessor tree: all of the PEs (except for a "master") do the same job. Such systems, which handle only a single-instruction stream but multiple-data streams (hence called SIMD machines) pose few software problems and can easily be improvised, even through networked PCs. However, multiple-instruction, multiple-data (MIMD) systems are much more desirable because they can tackle any job efficiently—at least in theory.

Needless to say, MIMD systems also pose a much greater technical challenge, even in their SPMD (single-program multiple-data) incarnation, which parallelizes one large program. MIMD computers have sprouted a jumble of architectures (collectively known as ensemble machines) to best satisfy the needed communications between the executing processes. Consequently, keeping track of communications offers the best method of reconstructing program execution come debugging time.

TRICKY ENSEMBLES

The efficiency of ensemble machines depends on a match between the parallelism of the problem and that of the hardware. For example, running six comparable tasks on five PEs virtually guarantees poor speed-up. To utilize all PEs effectively, ensemble systems must therefore be dynamically reconfigurable—their architecture must change on-the-fly as the code changes. Debugging a user program on such a computer can become a nightmare, especially when automatic load balancing varies the configuration from one run to the next.

Unlike serial programs, their multiprocessing cousins may catch users off balance with every new run. Algorithm type, problem size, and computer size all tend to be interrelated in unfathomable ways—at least without the benefit of hindsight. For example, the execution order of inherently concurrent functions can affect results—an effect

PARALLEL LANGUAGES: A NEW BREED

While popular "solo" languages can be made to play in an "orchestra," specialized parallel languages are also evolving, such as Occam or DGL (Data graph language). Some (such as Occam) require that programmers define which PE tackles which assignment, while the majority (including Ada) leaves the matching of processors and processes to the computer. It goes without saying that in most cases, the automatic assignment off the latter group takes the prize because it greatly facilitates load leveling. It's unfortunate that Occam as a static language doesn't condone such freewheeling behavior.

Parallelized Fortran, another parallel language, has most of its programs run on hardware with only a few PEs, assisted by vector processors. Some parallel dialects, however, can define individual processes even for hypercubes. Still, Fortran suits the synchronous world of array processors much better than that of asynchronous message-passing architectures. Even some recent parallel languages—for example Concurrent C from Bell Laboratories—make do with synchronous message passing. Worse yet, a few Ada implementations treat concurrent tasking synchronously as the function calls. Because the calling process must wait for a result before it can continue, synchronous tasking obviously isn't the way to attain large-scale parallelism.

Languages that truly cater to massive parallelism include the data-flow concept, which took the form of "IPs" (integrated processes) in the Software Series (ELECTRONIC DESIGN, Feb. to July, 1988). The concept is implemented in the Loral Dataflow LFD 100, which sports a rather unusual architecture. Actually, the Loral doesn't use data-flow; it employs process-flow programming because its serial code segments are written in Fortran.

Loral's data-flow graphs resemble data-flow diagrams *(see the figure)*. Internally, the graph elements are described by their imports and exports, as the example for the first worker shows:

```
worker_1 = " worker''
                <C0> <P10>
import {word[6]
    d01_nprocs}
export {word[2]
        d03_sum}
```

The word[n] clause defines the length of inputs and outputs for each process and <C0> specifies where the process runs.

The depicted algorithm finds the approximation of an integral by slicing the area under the curve into thin rectangles, then adding up their heights—the classical $\Sigma f\Delta t$ method. The Manager splits the function into big chunks that are passed to the Workers. Each of them integrates its chunk and passes the result to Summing, which adds up the partial results. In the figure, control flow turns on the worker processes first, and when they're finished, the summing process gets turned on.

The IPs could be decomposed further, to the point where the processes responsible for communications and those assigned to number crunching can be distinguished. Then it must be decided what module should be realized in software and in hardware. Because the communications machinery would be needed no mat-

PARALLEL PROCESSING

known as indeterminacy. In fact, purely sequential bugs may suddenly appear during parallel execution. Or, one of the processes can inadvertently pass some variable to an obscure subroutine and be picked up by another process using the same storage.

To avoid such "aliasing," parallel languages have long employed mechanisms that range from simple semaphores to complex monitors. When shared variables are scattered through a whole program, the monitor becomes a domicile for critical sections that are removed from their native processes. Whenever a process wants to enter one of these sections, it calls the appropriate monitor procedure. Only one process can enter the monitor after one process exits, preserving data integrity.

However, program modularity plays a role that's just as important. With such languages as Modula-2 and Ada firmly established, most recent (and hopefully all future) software can now be considered intrinsically parallelizable. But most older scientific programs were written in Fortran and they won't die easily. So the burden of their integrity rests either on a parallelizing compiler, or, more often, on the users.

Parallel languages need specific directives to convey the software designers' multiprocessing wishes to a compiler. These directives often take the form of extensions to popular languages, such as Fortran, C, or Lisp, even though special parallel languages (for example, Occam) also evolved *(see "Parallel languages—a new breed," below)*.

Inmos demonstrated an Occam programming environment in 1982. This Transputer Development System has now grown into an impressive instrument. Combined with other tools from Computer Systems Architects—including a parallel C—it makes software design for the Transputer easier than most other multiprocessing systems. For example, with one keystroke users can make the details of a program segment disappear, level by level, until only the "outline" of the software package under construction remains on the screen.

Though beneficial during program development, hiding details when debugging could turn counter-

ter what the problem is, this module would best be implemented in hardware with at least one input and one output channel for each of the processes.

Of course, that's precisely the concept of the Transputer from Inmos, now part of SGS Thompson Microelectronics. On one chip, each Transputer contains a powerful microprocessor, a large cache memory, and four communications links—of which as many can be used as desired. Unfortunately, the Transputer was touted for years as a high-level-language machine with (naturally) its own language, Occam. Now that Inmos has published the Transputer's native instruction set, the company is reaping a growing crop of potential customers.

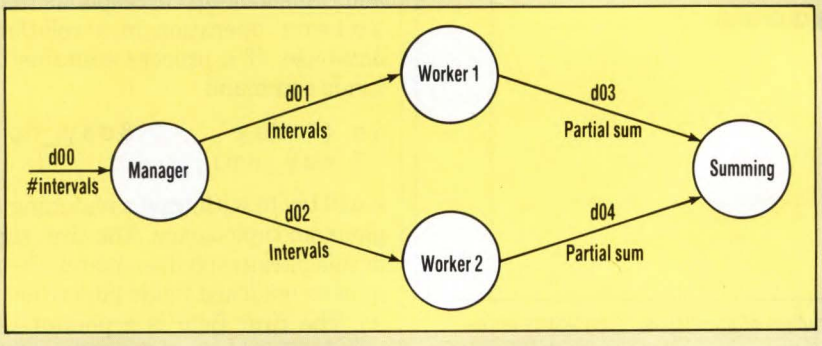
For sequential code, Occam closely resembles Pascal except that it permits multiple assignments. Because it was originally meant to serve as the Transputer's native language, Occam includes many operators needed only for "bit diddling," such as left and right shift, as well as bitwise logic. Occam does lack non-numeric operations and constructions, such as concatenation and records.

More important, however, are Occam's concurrency features—the way sequential threads can be combined into a multidimensional fabric. A parallel replicator, for example, spawns the specified number of equal processes. A sequential "alternation" (which corresponds to a logical OR) can, for instance, merge two communications channels into one:

```
ALT
left ? packet
joint ! packet
right ? packet
joint ! packet
```

Depending on whether the left or the right channel receives a data packet (`? packet`), this construct sends it on to the joint channel(`! joint`).

As the example shows, Occam demonstrates the requirements, and probably the best solution for parallel languages. Hopefully, some of Occam's features will find their way into emerging Ada 9x to supplement this language's rendezvous mechanism.



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productive. For debugging, a program must be "instrumented" so that what goes on inside can be seen. Worse yet, old instrumentation tricks that are used on a parallel system, such as inserting Print statements, won't work because the I/O disrupts the normal time relationship between processes. This disruption is known as the probe effect, which must be avoided at any cost. Indeed, sometimes the only solution is to leave the probes inserted during normal execution.

Furthermore, getting correct answers doesn't prove that the program's correct—it only establishes that erroneous segments weren't executed in a particular run. Therefore, before deciding on a parallel language, it's important to make sure what debugging support comes with it. This is because the amount of information to be conveyed to the programmer can be staggering—pages upon pages of diagnostics for every run.

To read a screen full of such text (say, 2000 characters) takes well over 60 seconds. In the same time, the eye can absorb several full-screen pictures of 100,000's of pixels each, which could convey 100 times as much information as the text (even more with color). Compare, for example, two methods for debugging hypercube programs: Inmos' textual program and the visual Tuple Scope. Cogent Research has forgone Occam and its development system in favor of Linda for system programming. Linda avoids some of the problems encountered with conventional parallel languages; it also offers a visual debugger.

Developed at Yale University and commercially available from Scientific Computing Associates, Linda is more a multiprocessing paradigm than a language. For example, Linda gets around synchronization, locking, and message passing by taking these functions away from processes or processors and turning them over to a type of bulletin board. Messages are posted in "tuple space," which is a content-addressable (or associative) memory region. Idle PEs search tuple space for appropriate messages. As a result, Linda sidesteps the tough problem of process interactions; if one "worker process" functions correctly, all of them will.

To see how Linda acts in an operating system (where, for example, Cogent's Linda resides), consider the screen handler PIX (parallel interactive executive), a PostScript-based window server compatible with Sun's NeWS. To increment a value `val` in dictionary `dict`, PIX uses the statement:

```
dict/val in 1 add out.
```

The Linda operator `in` removes the tuple containing `val` from tuple space `dict`, and while it's being updated in one process, no other process can get hold of it until the Linda process `out` puts the tuple back in circulation. Consequently, `in` corresponds to Occam's ? and `out` to !.

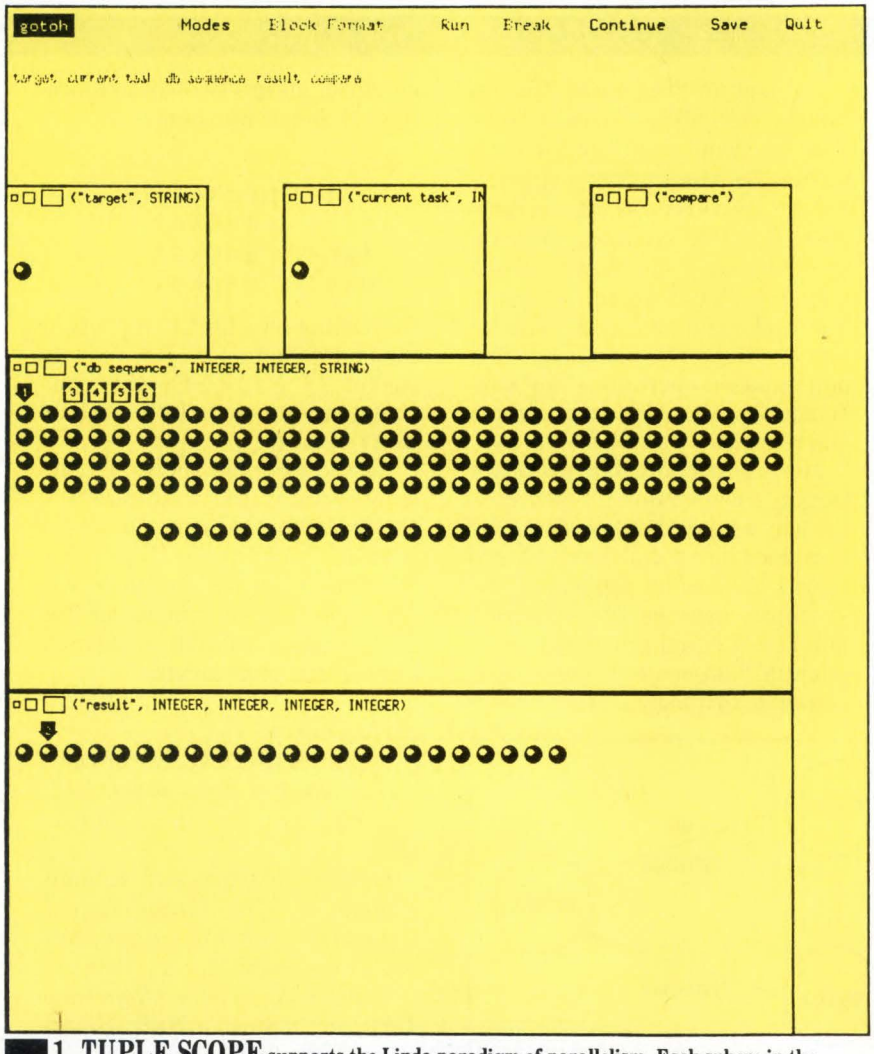
Tuples are simply collections of related symbols and data, for example

```
<" day'', 5,
 " Friday''>,
```

and tuple look-up corresponds to the `select` operation in a relational database. If a process contains the Linda command

```
in (" day'', ? &day_no,
 ? day_nm),
```

it will try to withdraw a matching tuple from tuple space. The first tuple in this paragraph does match the request's wildcard fields (identified by ?). The first field is a pointer to a storage location—a formal variable



1. TUPLE SCOPE supports the Linda paradigm of parallelism. Each sphere in the upper large window depicts one search tuple; solution tuples aggregate in the lower window.

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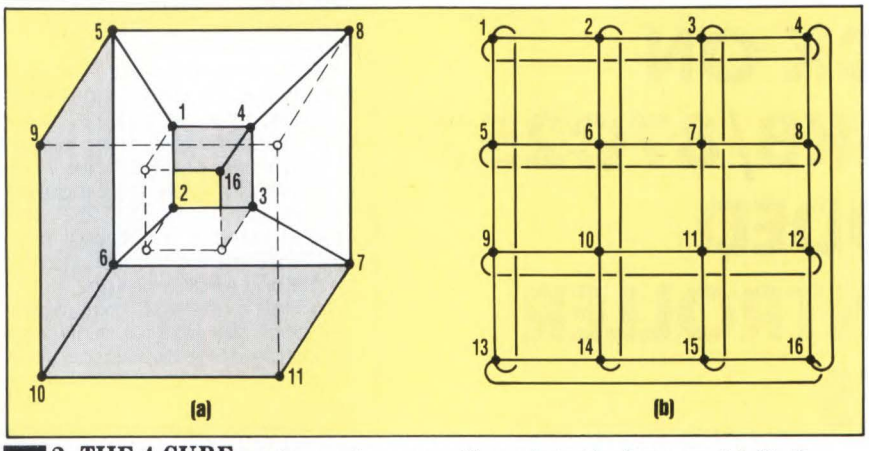

2. THE 4-CUBE topology can be expressed by a cube inside a larger one (a). Shading conveys the similarity with a torus, which can then be slit and flattened into a grid (b).

that's now bound to 5. In the second tuple, the formal variable day_nm is bound to the actual variable Friday.

In addition to the in and out procedures, Linda comprises rd and eval commands. The former works similar to in, except that it doesn't remove the matched tuple. The latter's function is more complex: eval emulates out and spawns a new process known as an active process tuple, Linda's mechanism for creating parallel processes. When all of an active tuple's variables are bound, it becomes inactive and can be incorporated in the program's solution.

These four commands (plus two variants) make up the entire Linda language. However, when C-Linda or Fortran-Linda is purchased, a number of tools are also included. The key tool is the Linda kernel, which contains code for setting up and searching tuple space. Because the pattern-matching algorithm can make or break the whole tuple method, the tools can be more important than the language itself.

TINY BUT POTENT

Linda is currently installed on about a dozen parallel computer models, but data on its performance are still sketchy. Tuple exchanges consume from a fraction of a millisecond on the Encore machine to several milliseconds on an older Intel hypercube. In the latter case, however, nearly 4 ms were exacted by the machine's message-passing overhead, which is now much lower.

Performance in actual applications would be of greater importance, but those results remain even sketchier than the data. On a matrix multiplication problem, speed-up was about 78% of ideal on an iPSC with 8 nodes, but it was only 64% with 16 nodes. Matching of amino acid sequences (which requires little communications) came in at 94% on 16 nodes but fell to 71% on 32 nodes. Performance on the Encore with 16 PEs was close to the hypercube with the same number of nodes. A search for prime numbers on the Encore computer with 10 PEs yielded 83% of ideal speed-up.

The performance of Tuple Scope, Linda's debugging aid, can be observed by running a DNA search on a common-memory machine *(Fig. 1)*. This search finds matches between short strings of the integers 1 to 4 (each standing for one of the basic amino acids) and longer strings that could, for example, represent genetically engineered "designer genes." The left small window holds the target tuple of the current search. Any tuple sphere can be opened up and viewed for content by clicking a mouse on it.

The top large window displays tuples from the sequences in the database and waits for workers to match them. Each tuple appears on the screen in the order in which it was spawned. In the lower window, result tuples wait for the "master" to collect them. Each individual tuple retains its location on the screen so that irregular patterns form as work progresses. When all of the tuples in both windows have been mopped up,

3. SEEPLEX OFFERS A WIDE RANGE OF VIEWS for events in a hypercube, of which "3-cubes in space" is most easily understood (a). The Gray-code circle displays link traffic even for large systems (b).

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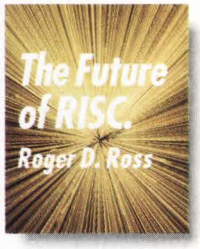

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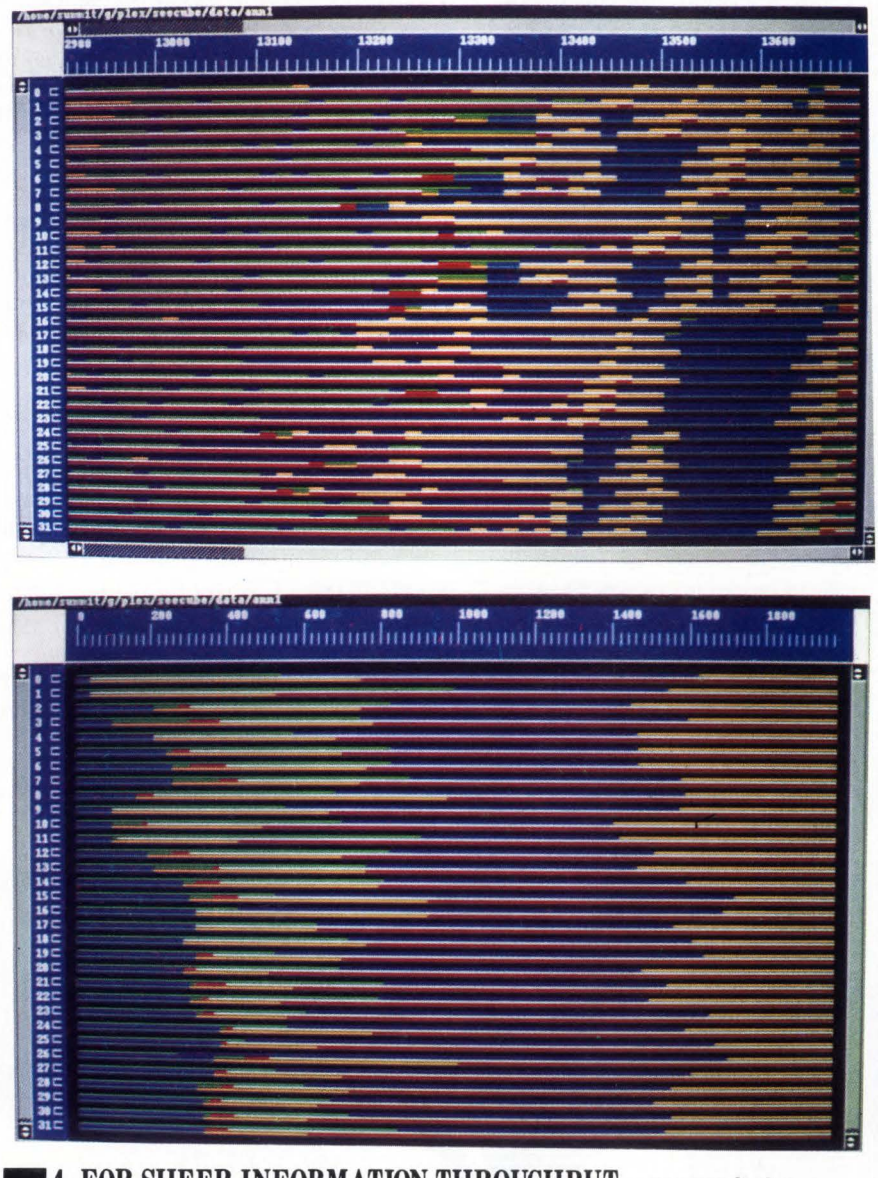
the job is done.

While Linda has proven its mettle on a number of concurrent computers, it must still conquer massively parallel systems. Although hypercube versions of Linda are underway, it remains to be seen how they'll stand up in practical use. Debugging thousands of parallel processes certainly imposes a challenge. Yet, hypercubes of order 10 and up (over 1000 PEs) are on the market, and they'll need debuggers custom-tailored to match both the topology and the programs.

Computer Scientists at Tufts University have pursued this debugging problem for years, both on Intel's and NCube's hypercubes. One solution, called Seecube, has been available since 1987 for a nominal license fee, and the more powerful Seeplex debugger is near its release. While Seecube primarily relies on stored data that are played back in post-mortem fashion, Seeplex aims at real-time performance.

Hypercubes primarily rely on message passing for communications. Both of the Tufts systems therefore attach themselves to the message streams. And, to broaden the information bandwidth, both rely on color as a third dimension, with time offering a fourth. Just by observing traffic distribution at the global level, users can judge which nodes are overworked and which idle too much. Gross errors, such as load imbalances, thus become readily apparent.



4. FOR SHEER INFORMATION THROUGHPUT, a summary display remains unsurpassed (top), especially when sorted by color (bottom).

SEEING IS BELIEVING

Seeplex can display no less than 256 parameters of 94 distinct types on each node. Furthermore, each parameter's current value, last change, average value, difference between current and average value, and difference between current value and an average of all nodes can be accessed. That amounts to well over a million parameter values on a 1024-node system—clearly much more information than users can readily absorb. Seeplex' main challenge is to offer displays that convey as much of these data as possible in the most meaningful manner.

Seeplex derives this monitoring power by tapping the custom-built Simplex operating system for the NCube, which can be substituted for the normal Vertex operating system. Although collecting the data mentioned above takes at most 10 machine cycles (a 10% overhead), it makes sense to collect only what will be used. That way, the multiprocessing boogeyman—the probe effect—can be kept at bay.

Data are collected by a library of subroutines that store diagnostic event traces in local memory for shipment to the host, which is usually a Sun workstation. A second set of routines cross-references the time-stamped traces and sorts them into a global trace that can be viewed as a movie.

Visual representations of hypercubes by themselves pose a challenge. A purely geometric representation is limited to the 4-cube arrangement *(Fig. 2a)*. Here, the shape of a hollowed-out 3-cube arrangement embodies the 4-cube topology. Above 5 cubes, the best model is the n-torus grid, which shows nodes as intersections on a square lattice.

The torus grid of the 4-cube model can be turned into a doughnut by first wrapping it around a horizontal

axis until the top meets the bottom; then the resulting tube must be bent until the left side mates with the right side. *(Fig. 2b)* At first glance, the grid and the 4-cube model don't appear topologically identical. But if the hypercube is envisioned as hollow and made of putty, it can easily be kneaded into a bagel.

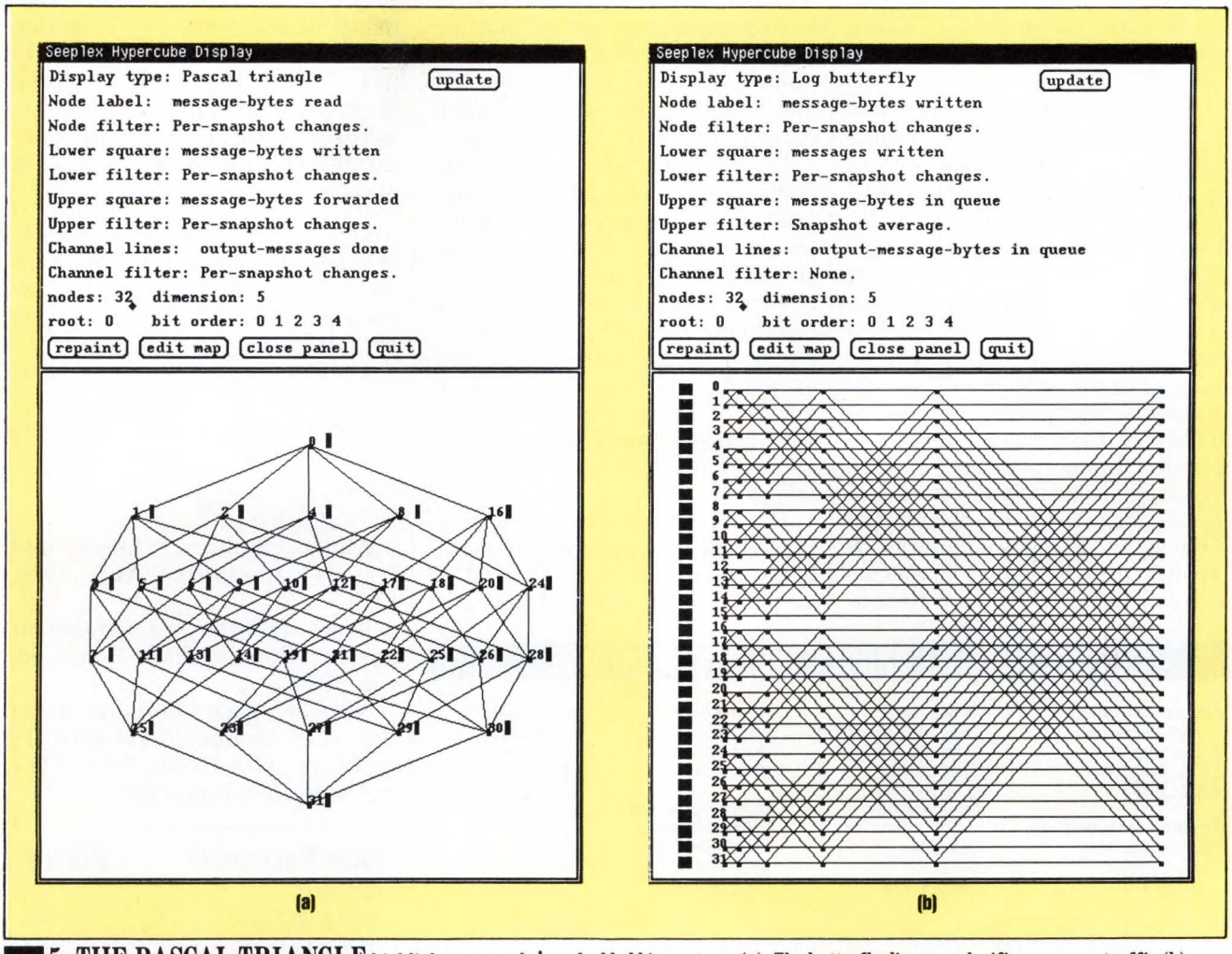
Seecube's "3-cubes in space" format may be easiest to comprehend, but it can't readily be expanded beyond the 5-cube arrangement *(Fig. 3a)*. Links between the nodes are split—each half is dedicated to one direction of transmission. Unfortunately, actual links between nodes can only be shown within the 3-cubes model; users must mentally find the target node for channels between the 3-cubes model.

An interesting alternative is the "Gray-code circle," whose links (for example, diagonals and sides) are again bisected to distinguish between incoming and outgoing traffic *(Fig. 3b)*. An interesting quality makes this display even more useful: links between sub-cubes appear as parallel lines. Although the number of nodes (located on the circumference) isn't limited in theory, the graph in the figure approaches the practical limit.

Color greatly helps users to visualize an n-cube model's complex inner life. Summary displays, which extract node status from the time display, often may reveal a problem most clearly. For example, the length of message queues (a giveaway for load imbalance) can be displayed at each node in the form of a bar chart, or the state of all processors can be viewed as a function of time *(Fig. 4, top)*. Node activities are seen in three lines as a function of time.

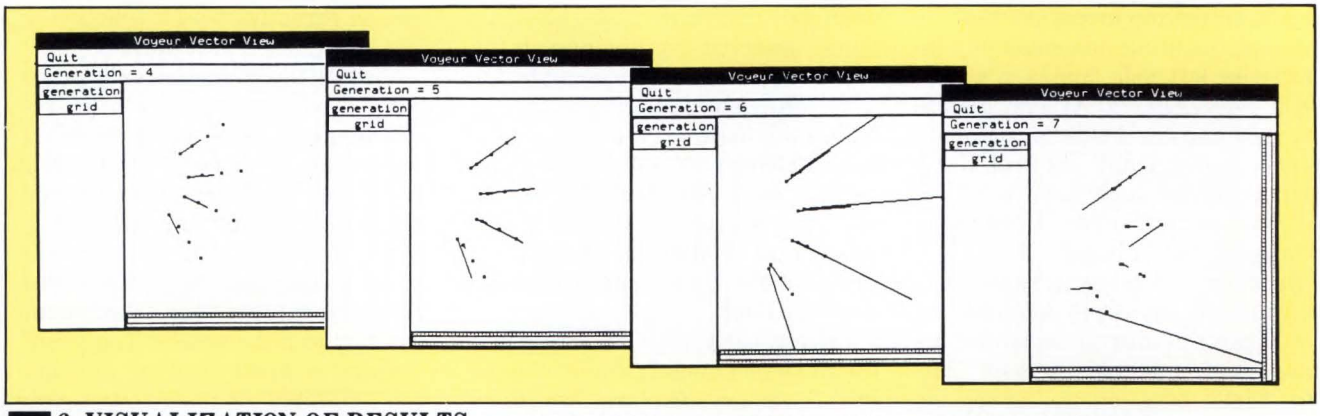
The first line gives the node's state using the following color code: red for idle, green for computing, yellow for writing, and blue for reading (which also blocks the node). The second line color-codes the message intensity from blue for zero to white for rush-hour, and the third line uses the same scale for (worst-case) number of bytes in a message. This graph contains a great deal of information—possibly too much. Once some irregularity is suspected, the graph should probably be sorted by color *(Fig. 4, bottom)*. Because the color selection is controlled on summary graphs, there's an unlimited amount of display choices.

The choice of hypercube representation further enhances comprehension. A binary Pascal triangle dis-



5. THE PASCAL TRIANGLE highlights an n-cube's embedded binary trees (a). The butterfly diagram clarifies message traffic (b).

PARALLEL PROCESSING



6. VISUALIZATION OF RESULTS will be vital for debugging parallel programs like this problem in fluid dynamics.

play, for example, serves as a natural representation for embedded binary trees *(Fig. 5a)*. From top to bottom, each layer differs from the next by one bit of the numbering scheme. In a butterfly diagram, messages always appear as diagonals in the same direction. The diagonals may be offset along the vertical dot rows, which in this graph represent nodes *(Fig. 5b)*.

Clearly, Seeplex—even more than Tuple Scope—relies on the behind-the-scenes activities to make process management visible. However, proper execution of a program on a multiprocessor doesn't ensure correct results. Most often, engineers must solve number-crunching problems. Examining these reams of numerical results is at best a tedious way to debug application code. Therefore, it's no surprise that general-purpose visualization tools have emerged to ease the burden.

In fact, visualization systems are already common in such fields as fluid dynamics. However, they can be expensive as behooves problems solved on the likes of a Cray. Recently, several universities have derived more affordable tools.

Voyeur, a tool developed at the University of Washington in Seattle for MIMD systems with non-shared memory, can serve as an example. To be effective, debugging systems must control execution (for example, by single-stepping), gather data during the run (through embedded probes), and then transform the data into a meaningful display. Voyeur concentrates on the last two steps.

To illustrate how Voyeur functions, consider a program that simulates fluid dynamics. To simplify matters, assume the system under scrutiny has cylindrical symmetry—all of the flow in a top view must proceed along radii. Any other flow direction indicates an error in the model or in the operating system. A sequence of Voyeur views illustrates what happens during several successive "generations" of execution *(Fig. 6)*.

The first view, taken after generation 3 implies that everything is in order; vectors at the innermost grid circle point radially outward. Soon, the bottom row of the grid is in trouble, and after generation 7 the calculation blows up altogether. Users can now look at some variables' values during the last generation and narrow down the error in the algorithm.

Voyeur presently deals only with vectors and icons, but puts the nitty-gritty of accessing and collecting variables, and displaying them, in place. Tools of this type will prove indispensable on multiprocessors, because only a visual display can master the data stream from thousands of solutions every second.□

This article is based on the author's book "Computer-Aided Software Design-Build Quality Software With CASE". The book, which will be published this month by John Wiley and Sons, New York, expands on the concepts discussed in the ELECTRONIC DESIGN *Software Series (Feb. 4 through July 28, 1988).*

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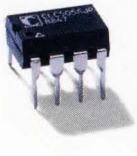
This fast op amp takes a fraction of the power of any other in its class. And gives you a 10-to-1 range of supply-current programmability. Bandwidth at 10mW is an exceptional 50MHz. And you can increase supply current for even higher speed... 150MHz and 13ns settling at only 90mW. Fast disable saves even more power on standby.

At just $6.95 in 1000-piece quantities (USA), the CLC505 can end your power-speed tradeoffs in remote-site and portable applications. As well as multichannel designs such as video distribution systems, ATE, and phased-array radar systems.

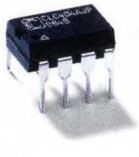


At 2600V/μs, you can stop worrying about slew-rate limits.

It took a new topology, but the monolithic CLC404 is changing the rules in large-signal applications. With a spec of 2600V/μs, slew rate just isn't a factor. Now, you get a full 165MHz bandwidth with a $5V_{pp}$ signal.

With a blazing slew rate like this, you'd think the CLC404 was a hybrid. But there's more good news. It's monolithic. With only 110mW power consumption. What's more, differential gain is only 0.07%, and differential phase is a mere 0.03°.

All this makes the CLC404 perfect for video designs. And fast slew rate in a monolithic is ideal for your large-signal applications.

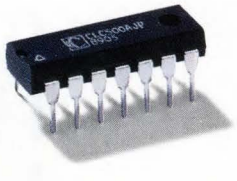


0.01% settling in 18ns... which settles all questions on 12-bit op amps.

Speed and accuracy is another tradeoff you can forget. Because the new monolithic CLC500 settles to 0.01% in just 18ns. And, unlike other 12-bit op amps, settling time is virtually independent of gain.

But that's not all. The CLC500 also delivers better than −80dB harmonic distortion at 5MHz, and input-referred noise is only $40\mu V_{rms}$, which means you don't sacrifice dynamic range. And an output clamping feature protects downstream circuits from overload and saturation.

Altogether, this spells the best op amp yet for A/D and D/A converter systems.



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SPEED MEMORY, EASE TIMING REQUIREMENTS WITH VRAM FUNCTIONS

THOUGH VRAMS COST MORE THAN DRAMS, THEY ARE ACCESSED MORE READILY AND NEED NO EXTERNAL ARBITRATION.

In addition to their standard functions, 1-Mbit video RAMs (VRAMs) have several special functions that speed memory operations and ease critical timing requirements. These functions serve to increase the efficiency of video-frame buffers and other VRAM applications.

For graphics and networking applications, the advantages of using VRAMs over dynamic RAMs (DRAMs) are significant. These systems suffer a memory tug-of-war between the processor and the video display or some other device. In a graphics application, for example, the processor needs to access the video-frame memory contained in the VRAM to draw what's being shown on the display. At the same time, the entire contents of the video memory must be sent to the display 60 to 70 times/s. In this application a processor can access a standard dynamic RAM only 40% of the time; a video RAM can be accessed 99% of the time.

VRAMs also require less external hardware to implement dual-port memory arrays. The built-in serial-shift register eliminates the need for an external shift register, and no external arbitration or multiplexing of the DRAM port is required. Finally, most 1-Mbit VRAMs offer added special functions to ease timing constraints and speed memory operation.

However, the added performance of VRAMs comes at a higher price than DRAMs, making them too costly for some low-speed applications. Another drawback is that VRAMs come in higher pin-count packages. In addition, DRAMs come in higher densities than VRAMs. Overall, the benefits far outweigh the costs for medium to high-end applications. Less demanding applications may or may not use VRAMs over DRAMs on a cost-benefit basis.

The 1-Mbit VRAM consists of a standard 256k-by-4-bit DRAM and a 512-word-by-4-bit serial-access memory (SAM) *(Fig. 1)*. Access cycles, timing, and refresh rates for the DRAM portion are similar to those for a 256k-by-4-bit DRAM. The SAM acts similar to a large shift register that's loaded from the DRAM in

JEFF MAILLOUX, JEFFREY MILLS, and MICHAEL J. SEIBERT
Micron Technology Inc., 2805 E. Columbia Rd., Boise, ID 83706; (208) 383-4000.

VRAM SPECIAL FUNCTIONS

256k-BY-4 BIT VRAMS - CROSS REFERENCE GUIDE

	Micron Technology	Texas Instruments	Toshiba	Toshiba	NEC	NEC	Fujitsu	Mitsubishi	OKI
	MT42C4256	TMS44C251	TC524258A	TC524256A	uPD42274	uPD42273	MB81C425	M5M442256	MSM514252
DRAM:									
Non-persistent masked write	Y	Y	Y	Y	Y	Y	Y	Y	Y
Persistent masked write	N	N	N	N	N	N	N	Y	Y
Block write	N	N	N	N	N	N	Y	Y	Y
Non-persistent masked block write	N	N	N	N	N	Y	Y	Y	Y
Persistent masked block write	N	N	N	N	N	N	N	Y	Y
Load mask register	N	N	N	N	N	N	N	Y	Y
Load color register	N	Y	N	N	Y	N	Y	Y	Y
SRAM/TRANSFER									
Read transfer	Y	Y	Y	Y	Y	Y	Y	Y	Y
Split read transfer	N	Y	N	N	N	N	Y	Y	Y
Write transfer	Y	Y	Y	N	N	Y	N	Y	Y
Pseudo write transfer	Y	Y	N	N	N	Y	Y	Y	Y
Alternate write transfer	N	N	N	N	N	N	N	Y	Y
Masked write transfer	N	Y	N	N	N	N	Y	N	N
Split wire transfer	N	Y	N	N	N	N	Y	N	N
Flash write	N	Y	N	N	Y	N	Y	N	N

parallel. It interfaces the video look-up table to the digital-to-analog converter or between peripherals in networking applications.

Besides having two I/O ports, the video RAM also sports very wide internal data paths between the dynamic RAM and the serial-access memory. For a 256k-by-4 bit VRAM, data I/O and internal data transfer are done using three separate bidirectional data paths: the four-bit random access I/O port, the four internal 512-bit wide paths between the DRAM and the SAM, and the four-bit serial I/O port for the SAM. Each of the I/O ports may be operated asynchronously and independently of the other, except when data is transferred internally between them. The rest of the VRAM's circuitry consists of the control, timing, and address-decoding logic.

Special Functions

The Joint Electron Device Engineering Council (Jedec) established two standards: one for the basic 1-Mbit VRAM (the minimum function truth table), and the other for implementing special functions on the 1-Mbit VRAM (the extended function truth table). To be a standard VRAM, the part must meet the minimum functions, but it doesn't have to implement any of the special functions.

The difficult question for system designers is when and where should special functions be used? First of all, designers must decide if it's worth the time and effort to implement the special functions. Will they speed up processing significantly or only add complexity to the design? Secondly, designers must determine if a particular special function will limit them to just a few or even one source of VRAMs. Or in the worse case, will the design be obsolete if a manufacturer stops offering that special function.

Currently, at least nine manufacturers produce or plan to produce 1-Mbit VRAMs: Fujitsu, Hitachi, Micron Technology, Mitsubishi, NEC, Oki, Samsung, Texas Instruments, and Toshiba *(see the table, above)*. The chips' special functions are grouped into two functional blocks—the DRAM port and the transfer circuitry.

DRAM Port Functions

Graphics systems often need to change some memory bits while leaving others unchanged. A good example is drawing a line on top of a color picture. Certain bits need to change in order to draw the line, but the bits that make up the picture shouldn't change.

The masked-write function, also called the write-per-bit or dynamic masked-write function, has been available on 256-kbit VRAMs for some time. Without this function, a processor has to first read a DRAM location, change only certain bits, and then write the data back to the DRAM. This operation can be accomplished in just one masked-write access cycle.

There are two types of masked write functions—the more common non-persistent masked write and the persistent masked write. With the non-persistent masked write, the data present on the DQ_{1-4} inputs is temporarily written into the mask-data register when the $\overline{RAS}$ signal falls. The mask data then acts as an individual Write Enable signal for each of the four DQ_{1-4} pins. The input port for a bit is disabled when the mask-data register bit is low (logic 0), and it's enabled when the register bit is high (logic 1). For a non-persistent masked-write function, the mask-data register is loaded with the data on the DQ inputs at every falling edge of $\overline{RAS}$.

The persistent masked-write function can be used when the same mask data is needed for several cycles. For example, if a line is drawn across a screen, the same mask information will be needed 1280 times for a 1280-by-1024 pixel screen. The load mask-data register operation is used before a persistent masked-write cycle to load the mask register.

Persistent masked-write cycles use the mask-register data; they don't require new mask data for each cycle. The load mask-register cycle is used with persistent masked write to give graphics controllers that can't output data at the $\overline{RAS}$ signal time to perform masked writes.

A block-write operation clears a large area of the DRAM quickly. It's useful for writing window areas to a background color. Instead of writing to just one location consisting of four bits (a normal by-4 DRAM write cycle), the block write function makes it possible for the system to simultaneously write data to four locations of four bits each (16 bits total). This will speed memory operation by a

VRAM SPECIAL FUNCTIONS

factor of four.

Before performing a block write, the system must first perform a load color-register cycle. This cycle is similar to the load mask-register cycle. The contents of the color register are kept until changed by another load color-register cycle. The contents of this register are used as the data during the block-write cycle.

During the block-write cycle, the DQ inputs to the video RAM enable or disable the four column locations. A logic one enables the write function; a logic zero disables it. Each enabled DQ location of the color register is written to each enabled column location in the corresponding DQ bit plane *(Fig. 2)*.

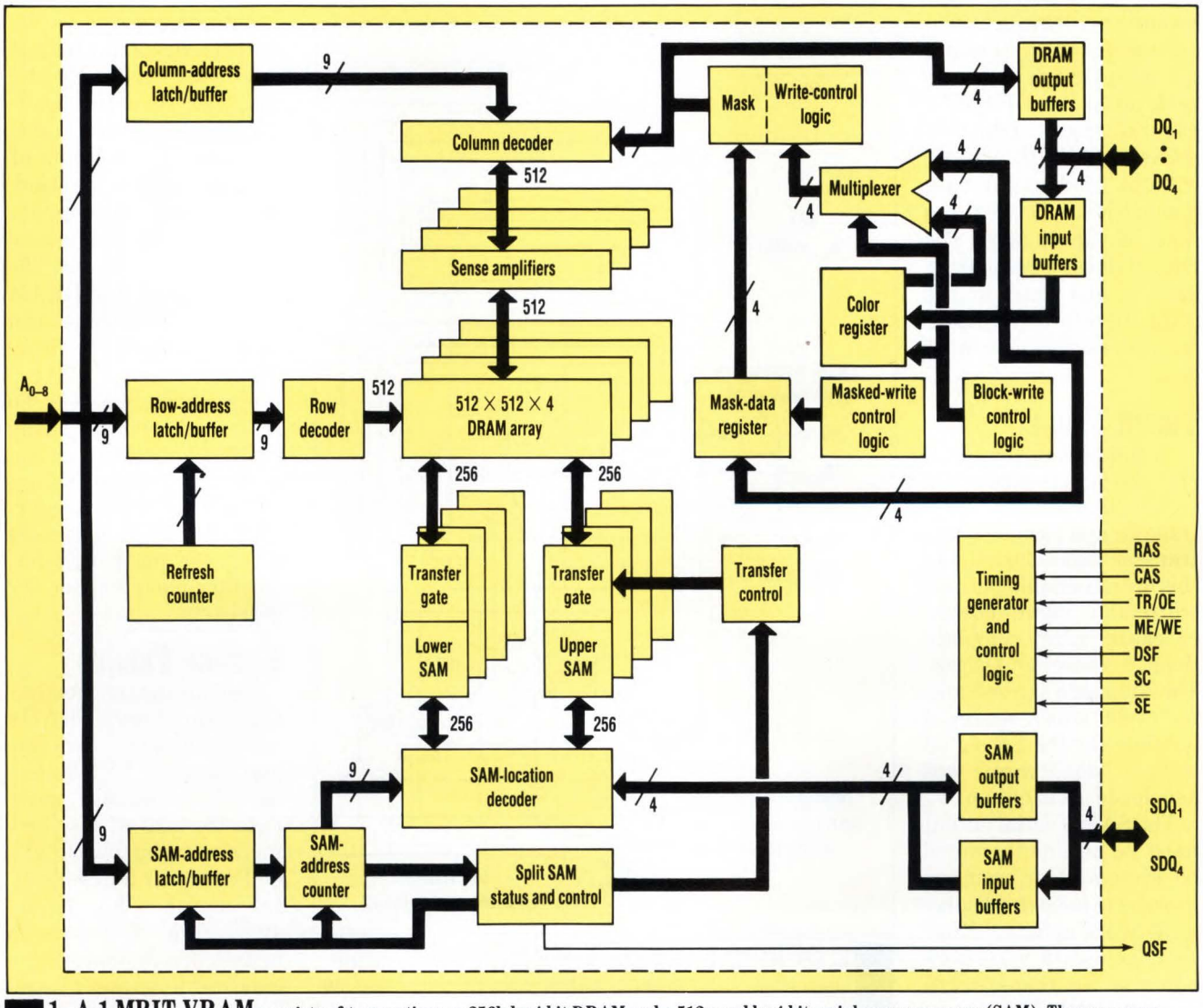
The masked-write functions can be used in conjunction with block write to perform a non-persistent or persistent masked block write. The masked-blocked-write function operates in the same way as masked write, except that the mask data are now applied to four column locations instead of one.

Masked Combinations

By using both the column mask input and the masked-write function, combinations of the four bit planes and the four column locations can be masked. The block-write feature is useful for clearing areas of the screen to a background color. This changing of background color is usually done before data or picture information is put in a windowed area on the screen.

All VRAMs have read transfer/serial output. With this function, the SAM can send data to the display or to other memory boards within a network. Almost any networking application, and some graphics and imaging applications, require serial input/write transfer.

In networking applications, the SAM port sends and receives data between memory boards, leaving the DRAM port free for the system microprocessor to access the memory. Consequently, the SAM port is used regularly for both input and output transfers. Graphics and imaging



1. A 1-MBIT VRAM consists of two sections: a 256k-by-4-bit DRAM and a 512-word-by-4-bit serial-access memory (SAM). There are very wide internal data paths between the two portions.

VRAM SPECIAL FUNCTIONS

boards that capture data from cameras or video displays also use the SAM port to input data to the VRAM memory and then to output data to the display.

With the write-transfer function, data can be input to the SAM and then transferred up to the DRAM. This write-transfer function is available on most 256-kbit VRAMs and most vendors offer it on their 1-Mbit VRAMs.

Complementing the write transfer operation is the pseudo-write transfer, also known as the serial-input-mode enable. When a write transfer is first performed, the SAM changes direction from output to input and the contents of the SAM are transferred to the DRAM. This avoids the complications associated with sending the output data's last cycle back up to the DRAM. A pseudo-write transfer turns the SAM around without sending the data present in the SAM at the time of the change. The DRAM doesn't receive the data it just sent to the SAM, therefore the SAM is ready to receive new input data.

TRUTH TABLE

In the present truth table, the serial-enable pin selects between the write-transfer and pseudo-write-transfer functions. Using this output-enable pin as a truth-table input, however, causes many complications in controller designs. The alternate write-transfer cycle, which makes it possible for the $\overline{SE}$ signal to be a "don't care," was developed as an option.

The SAM's serial output must be an uninterrupted bit stream of information in order to keep the display or network updated. However, new data must periodically be transferred from the DRAM down to the SAM before sending it out. These real-time transfers require very careful system design and timing: The transfer must occur exactly when the last bit of old data is being shifted out of the SAM.

The split-read transfer function eliminates this constraint by splitting the SAM in half and enabling the system to transfer data to one half of the SAM while the other half is shifting data out. When the half that shifted the data empties itself, the SAM automatically switches sides and starts shifting data out of the freshly loaded half. The system can reload the idle half at any time while the other half is being shifted out.

The split-write transfer function mirrors the split-read transfer, except that it operates in the opposite direction. Half of the SAM can be transferred up to the DRAM at any time while the second half is filling with data. Easier, less expensive controller and bus designs result from split transfers.

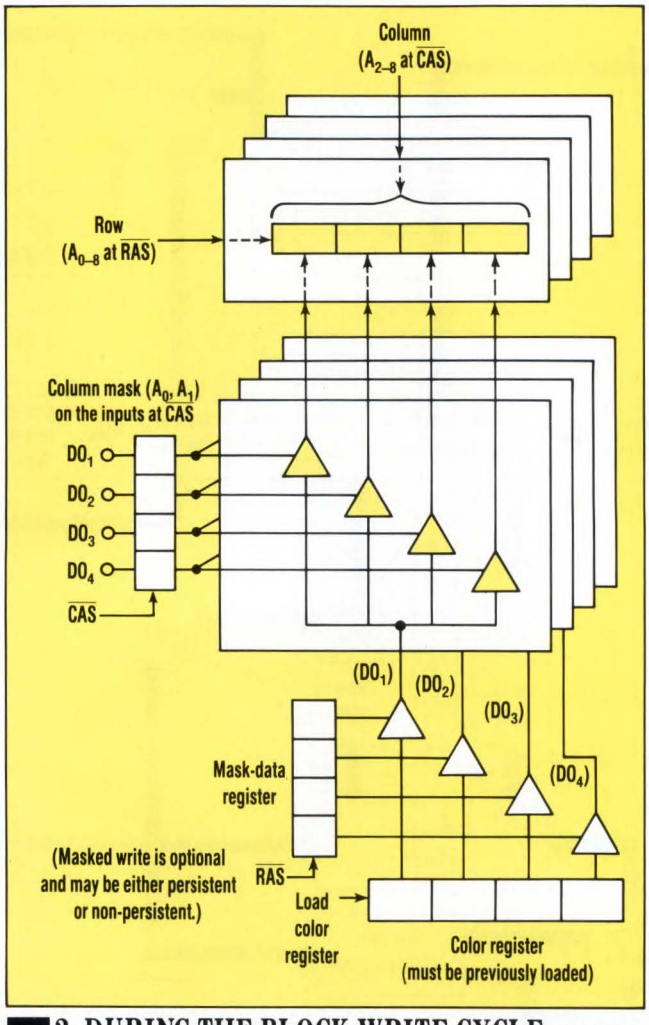
With the masked-write transfer function (both full and split), the system can choose which of the four rows of DRAM data (DQ_{1-4}) will get transferred from the SAM registers (SDQ_{1-4}) to the DRAM when a write-transfer cycle is performed. "Full SAM" write transfer cycles can be either masked or unmasked; all split-write transfers are masked. Mask data must be supplied on the DQ inputs whenever a split-write transfer cycle is done.

With flash write, the entire contents of any DRAM row can instantly be changed to a predetermined value. In one transfer cycle, the contents of the color register are loaded into each appropriate bit plane on the entire width of the row. All 256 bits of each of the DRAM row's four DQ planes can be set to all ones or all zeros.

Flash write can clear the screen on a graphics terminal. Block write can accomplish the same thing, though it takes longer. Flash write is maskable using the mask register, whether non-persistent or persistent.

FUTURE TRENDS

As with any semiconductor technology, VRAMs will continue to evolve rapidly. Because VRAM density is increasing faster than the size of displays, there's a trend toward wider data words that will better match CRT frame sizes. The pressure to maintain or to improve the bandwidth of the VRAM-based frame buffers will also force vendors to offer



2. DURING THE BLOCK-WRITE CYCLE, the DQ inputs either enable or disable the four column locations. Each DQ location of the color register that's enabled is written to each of the enabled column locations in the corresponding DQ bitplane.

VRAM SPECIAL FUNCTIONS

wider I/O paths and faster SAM clock rates on higher density VRAMs. Eight-bit I/O transfers were announced by several manufacturers on 1-Mbit VRAMs and 16-bit I/O will be available on the next generation of parts.

Some vendors are also beginning to offer VRAMs that can perform logic operations between incoming data and data resident on the VRAM. These logic operations can be utilized for such common graphics functions as adding transparent images to the screen or merging graphic images together.

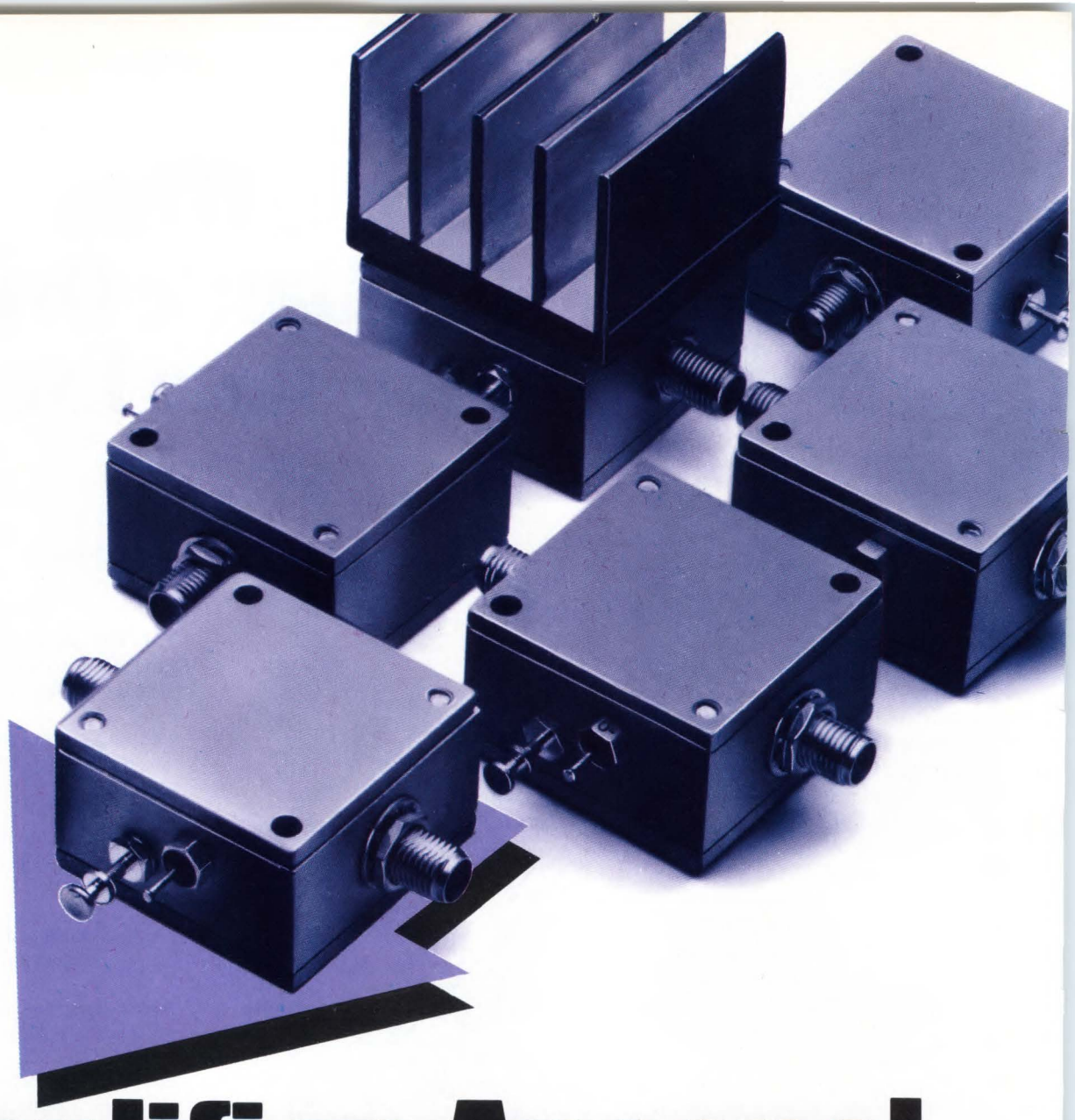
There isn't any Jedec standard on how logic operations should be implemented on VRAMs. In most systems, the graphics processor hardware performs these operations. Once standards emerge, two more factors should be considered before moving logic operations to the VRAM. First of all, the higher cost of VRAMs with logic-operation capability must be justified by lower chip count or increased performance for the graphics processor hardware. Secondly, a sufficient amount of vendors must offer these parts to ensure their availability.□

Jeff Mailloux, advanced products marketing manager at Micron Technology, has a BS in electrical engineering technology from the Milwaukee School of Engineering.

Jeffrey Mills, product marketing engineer for Micron's multiport DRAMs, has a BA in natural science from Lewis and Clark College, Portland, Ore., and a master in international management from the American Graduate School of International Management, Phoenix.

Michael J. Seibert is an applications engineer at Micron, specializing in graphics and imaging technology. He has a BA in physics from St. Mary's College, Winona, Minn.

How Valuable?	Circle
Highly	554
Moderately	555
Slightly	556



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ZFL-1000	0.1-1000	17	+9	6.0	79.95
ZFL-1000G*	10-1000	17	+3	12.0	199.00
ZFL-1000GH*	10-1200	24	+9	15.0	219.00
ZFL-1000H	10-1000	28	+20	5.0	219.00
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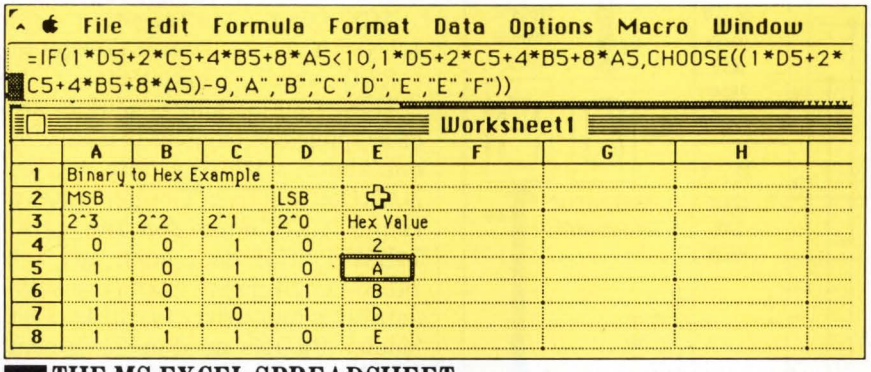
CIRCLE 524 LET A SPREADSHEET DO THE WORK

JIMMY D. SLIFE
XEL Communications Inc., 17600 E. Exposition Dr., Aurora, CO 80017; (303) 696-2223.



	A	B	C	D	E	F	G	H
1	Binary to Hex Example							
2	MSB			LSB				
3	2^3	2^2	2^1	2^0	Hex Value			
4	0	0	1	0	2			
5	1	0	1	0	A			
6	1	0	1	1	B			
7	1	1	0	1	D			
8	1	1	1	0	E			

THE MS EXCEL SPREADSHEET can use a simple algorithm to convert binary values to hex values.

Spreadsheet programs such as Lotus 1-2-3 or Microsoft Excel can be used for engineering as well as financial purposes. One engineering application for spreadsheets is for recording the inputs and outputs of digital devices in different states. The spreadsheet keeps all of the ones and zeros lined up perfectly and makes it possible to easily adjust column widths *(see the figure)*.

In such cases, it's often convenient to represent the bits in a hexadecimal (hex) form. A simple MS Excel algorithm converts a 4-bit binary field into the correct hex value:

if numerical hex value is less than 9,
then print the value
else subtract 9 from numerical hex value
and represent the result as one of the characters A through F.

Operation of the equation follows a step-by-step procedure: First, the spreadsheet calculates the numerical value of the 4-bit field. The 2^0 place is multiplied by one; the 2^1 place is multiplied by 2; and so forth. The results are then added together to determine the numerical value of the bits.

The "if" statement consists of a logical test, a "do-if-true," clause and a "do-if-false" clause. The test statement determines if the numerical value is less than 10. The do-if-true clause, simply prints the numerical value of the 4-bit field if the value is less than 10. The do-if-false clause subtracts 9 from the numerical value and represents the result as one of the characters A through F.□

IFD WINNERS

IFD Winner for August 24, 1989

Wes Freeman, Teledyne Semiconductor, 1300 Terra Bella, P.O. Box 7267, Mountain View, CA 94039. His idea: *"Prescaling Eases Thermometer Design."*

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CIRCLE 525 DISPLAY VALUABLE SCSIBUS INFORMATION

JIM MURASHIGE
Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, CA 94086; (408) 720-8630.

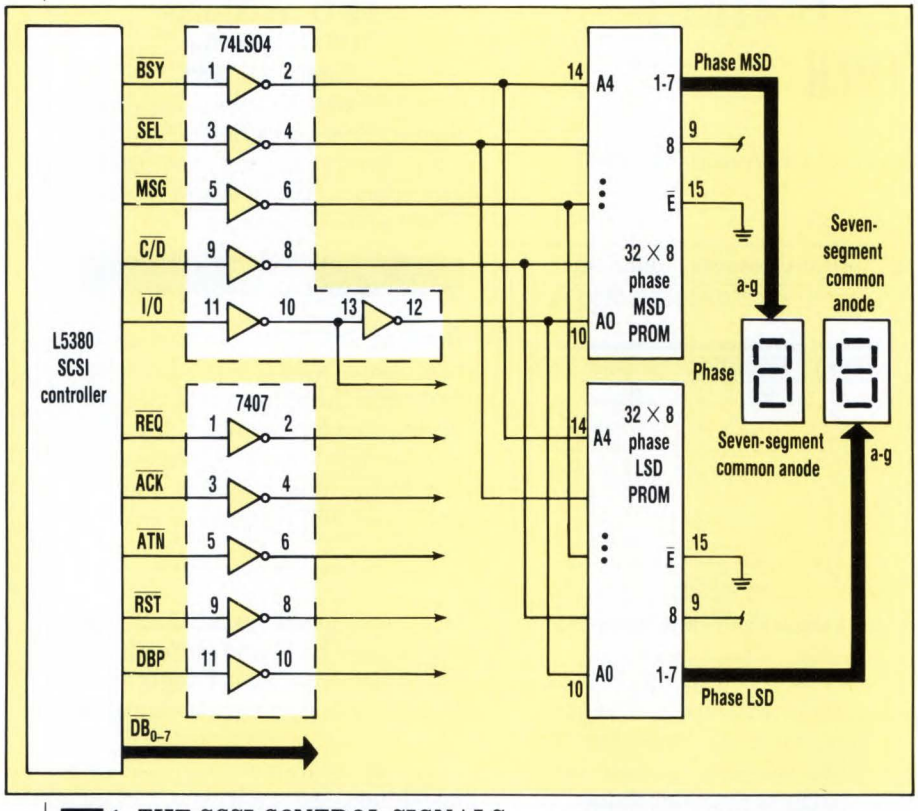
Debugging a SCSI interface design requires knowledge of all current SCSI signal conditions. It can be done by constructing an in-circuit bus analyzer that can monitor, decode, and display pertinent SCSI phase, data, and control functions. This bus analyzer works in single-ended asynchronous SCSI environments and can be used in either arbitrating or non-arbitrating systems where selection-reselection is implemented.

Built onto a small board, the bus-analyzer circuit accesses the SCSI signal bus through the user board's SCSI controller—in this case a Logic Devices L5380 *(Fig. 1)*. This is accomplished by placing the L5380 directly on the bus-analyzer board, rather than the user board, and then running all of the signals back down to the user board through either a socket extender under the L5380 or a one-to-one ribbon-cable plug.

The L5380 SCSI control signals are buffered and in turn drive other parts of the circuit. BSY, SEL, MSG, C/D, and I/O are specifically used to decode the various SCSI bus phases. All SCSI bus signals are negative true, active low. Actual decoding is performed by two 32-by-8-bit bipolar PROMs used as decoder-drivers to generate a two-character phase mnemonic.

The 8-bit SCSI data bus ($\overline{DB}_{0-7}$) and parity $\overline{DBP}$ are latched for display on any one of four significant control-signal edges *(Fig. 2)*. The latching conditions and data latch are:

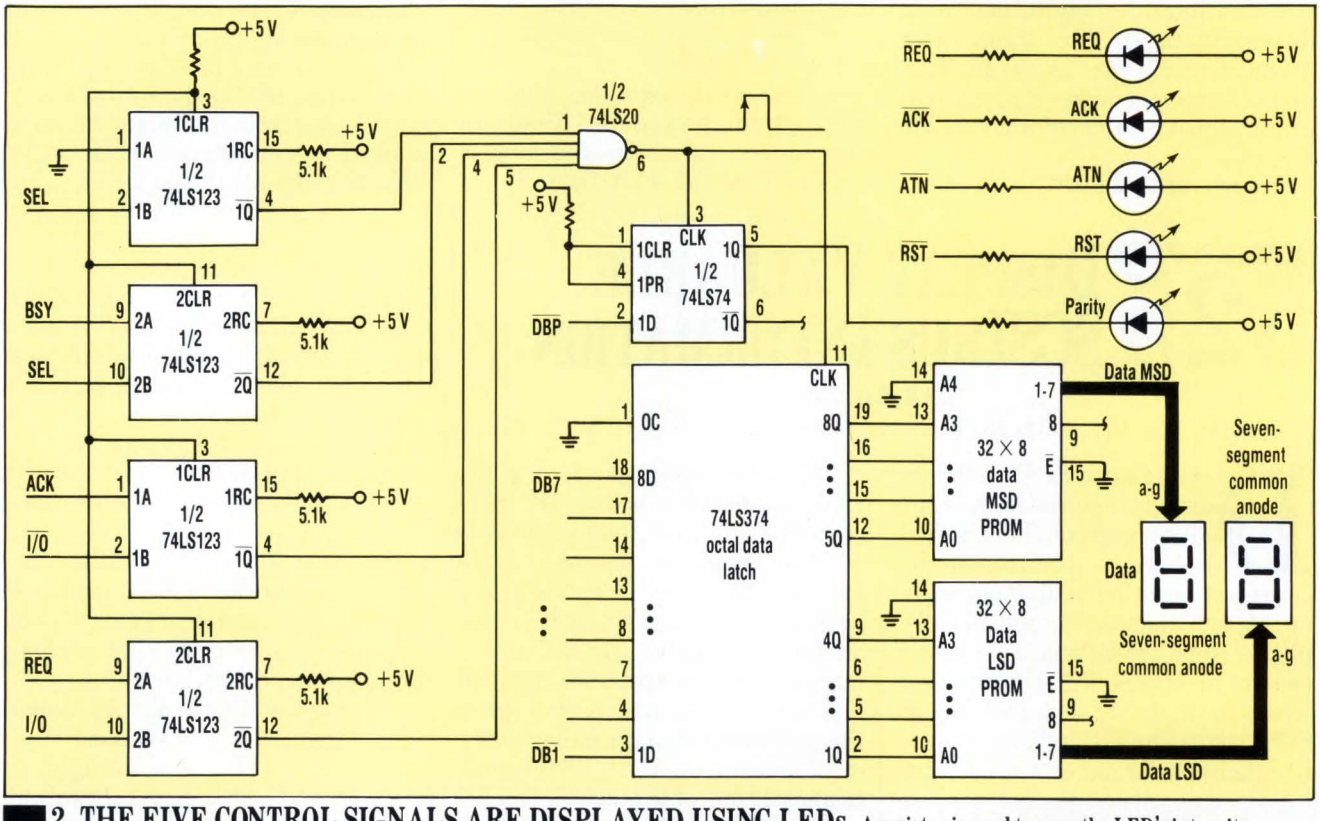
Latching Condition	Data Latched
1. SEL rising	Winning arbitration # in arbitrating systems.



1. THE SCSI CONTROL SIGNALS coming from L5380 controller are buffered and sent to other areas in the circuit.

	Selected target # in non-arbitrating systems.
2. SEL = 1 and BSY falling	Selected target # or Reselected initiator # in arbitrating systems.
3. I/O = 0 and ACK rising	Data out (Initiator to Target)
4. I/O = 1 and REQ rising	Data in (Target to Initiator)

These four latching conditions are each applied as triggers to a bank of one-shots with the low pulses NANDed together. This generates a rising CLK edge for the octal 74LS374 SCSI data latch and 1/2 74LS74 SCSI parity latch. The octal data latch then drives two 32-by-8-bit bipolar PROMs used as 7-segment hex decoder-drivers. SCSI data parity is displayed on one light-emitting diode (LED), as are the SCSI control signals REQ, ACK, ATN, and RST. All outputs driving LEDs will require a series current-limiting resistor to adjust the LEDs. For more information displaying SCSIbus signals, contact Logic Devices.□



2. THE FIVE CONTROL SIGNALS ARE DISPLAYED USING LEDs. A resistor is used to vary the LED's intensity.

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CIRCLE 526

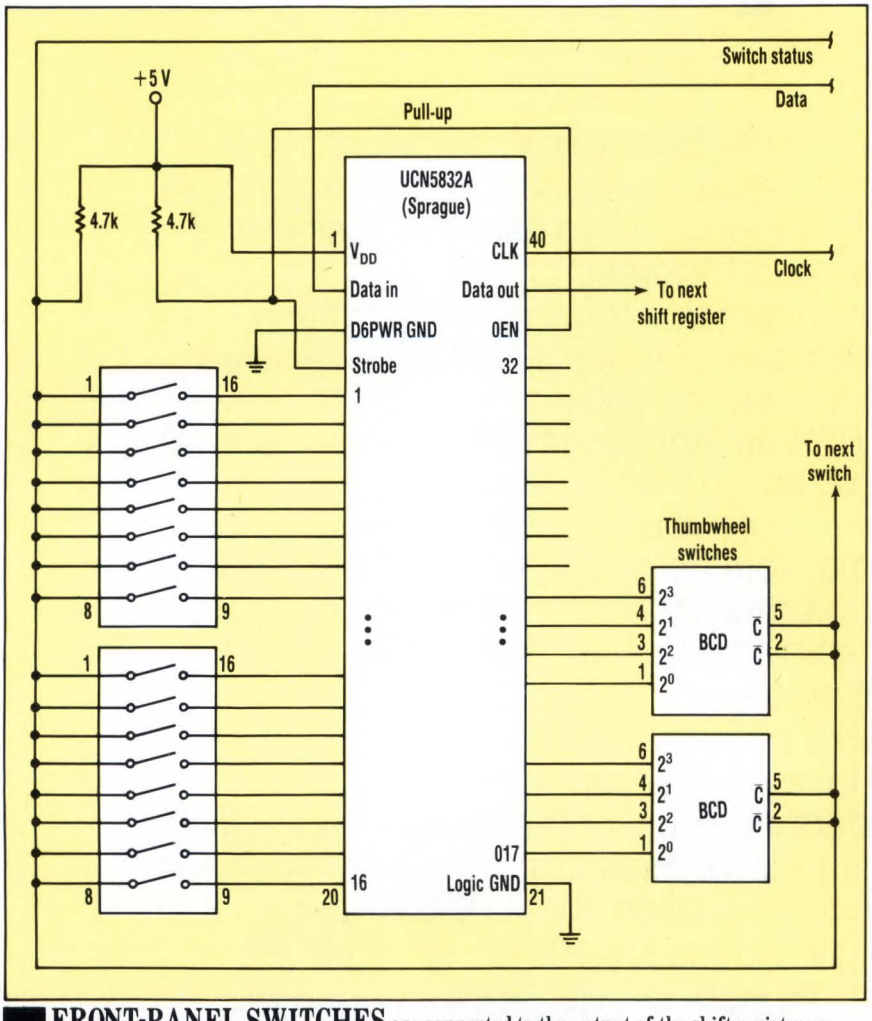
THREE WIRES, ONE CHIP READ 32 INPUTS

NOOR SINGH KHALSA
EG&G Inc., EM Div., P.O. Box 809, MS E-1, Los Alamos, NM 87544.

A shift register with open-collector outputs is just the ticket for interfacing front-panel switches to a microcontroller. One side of each switch is connected to an output bit of the shift register—the other side tied to a common input. The input is pulled high by a pull-up resistor and fed to an input pin on the controller.

When one of the shift register's outputs is active, the common line will be pulled low, but only if the switch connected to this pin is closed. The switches are sequentially read by propagating an Active Low signal through the shift register and reading the common pin after each shift. If more than one switch is closed, the other closed switches won't affect the reading because the open-collector outputs of the shift register make them effectively open.

This circuit is very versatile. Because all switches have a common side, the scheme works with encoded thumbwheel and rotary switches, as well as dip and toggle switches *(see the figure)*. Many switches can be read by cascading shift registers.□



FRONT-PANEL SWITCHES are connected to the output of the shift register on one side and to a common input on the other side.

ANALOG SIMULATOR TAKES GRAPHICAL INPUT

With the Stimulus Editor from MicroSim Corp., Irvine, Calif., users can input stimulus waveforms to the PSpice analog simulator in graphical form. Waveforms are entered by specifying parameters or by drawing them with a mouse. In either case, immediate graphical feedback makes verifying and correcting the waveforms easy. Menu prompts guide users to give the necessary parameters, such as rise time, fall time, and the period of a repeating pulse. The Stimulus Editor also offers a way to create digital stimuli for the Digital Simulator option. The input waveforms created by the editor are automatically saved in the circuit file, so users need only set up the waveforms once. The Stimulus Editor is included with PSpice, starting with version 4.02 at no extra cost. PSpice costs between $950 and $29,900, depending on the platform and options. Call Susan Kennedy, (714) 770-3022. LG

CIRCLE 301

ANALYZE ANALOG CIRCUITS ON YOUR MACINTOSH

Designers can run analog circuit analysis on a Macintosh computer with the AC Network Analysis Program (ACNAP) from BV Engineering Professional Software, Riverside, Calif. ACNAP, a general-purpose circuit simulation program, analyzes linear circuits containing up to 200 active and passive components. Functions in the software package include Bode plotting, noise-equivalent bandwidth calculations, component iteration, spectra analysis, and worst-case analysis. Users can create macros with embedded comments, delays, and pauses to automate repetitive tasks. Component models and circuits may be created, combined, edited, and saved to a component library as single devices. ACNAP needs 512 kbytes of memory. It runs on a floppy- or hard-disk-based Macintosh 512k, Mac Plus, Mac II, or Mac SE under System 3.2 or later, or Finder 5.3 or later. The software is available now for $349.95. For $95, an optional plotter-driver module plots results on most color-pen plotters. Call Steve Sauls, (714) 781-0252. LG

CIRCLE 302

FAST BiCMOS SRAMs HALVE BIPOLAR POWER

Each of a pair of 256-kbit ECL SRAMs from Fujitsu Microelectronics, San Jose, Calif., consume about half the power of bipolar devices on a per-bit basis. The MBM101C500-15 and MBM101C504-15 are organized as 256 kbits by 1 and 64 kbits by 4, respectively. Both have access times of 15 ns, and both are offered in the 10K and 100K series. The company's ECL biCMOS process uses 1.2-μm CMOS with a buried n+ layer for latch-up prevention and better soft-error immunity. In addition, p-well isolation layers decrease hot-electron effects. Both come in ceramic flat packs, DIPs, and leadless chip carriers. The MBMC500-15 series is now available in production quantities and costs $87.50 for ceramic DIPs, $91.88 for flat packs, and $95.33 for LCCs. The MBMC504-15 series will be sampled in the fourth quarter of 1989, with production in the first quarter of 1990. LCCs will cost $125. All prices are for quantities of 1000. Contact Fujitsu, (800) 642-7616. DM

CIRCLE 303

FIND CIRCUIT ERRORS AS SIGNALS PROPAGATE

An enhancement to its software tool set for ASIC designs, the NavNet graphical shell from S-MOS Systems Inc., San Jose, Calif., makes it possible for designers to trace signal timing errors as they propagate through a system. The company estimates that the ease of tracing errors with the new software could halve the time to simulate designs. The software graphically displays pulse-width violations as a waveform. Consequently, when a glitch is traced, the location of the error is simultaneously displayed on the schematic, so designers can quickly identify and trace the glitches, make changes, and then resimulate. With the hierarchical navigator, engineers can identify many common errors during the initial design stage, rather than wait until the simulation is done. The navigator also manages the connectivity throughout a multipage schematic by automatically highlighting connections between functional blocks. Thus, in addition to capturing schematics, NavNet helps users perform sequential "undo" and "redo" to recover from previous operations. Running under Microsoft MS-Windows and Sun Microsystems' Sunview, the software can run on 286, 386, RTX, and Sun 3 or 4 systems. A site license for either version runs $2000 to $3000. Call John Conover, (408) 922-0200. DB

CIRCLE 304

SMALL MODULES EXPAND CPU CARD FAMILY

With board space extremely limited on its single-board PC family, Ampro Computers Inc., Sunnyvale, Calif., developed a family of industrial add-on modules and adapter cards that make it possible to expand its family of single-board PCs. The Minimodule family of expansion cards include network and display controllers (CRT or flat-panel), serial or parallel I/O functions, and other system support functions. The Ampro's computers pack most PC features and then some—timers, DMA control, floppy-disk control, SCSI controller, DRAM, RAM-disk, and a PC expansion bus. Measuring

just 3.5 by 3.8 in., one Minimodule attaches to the single-board computer through a header-type connector with a pinout that duplicates the signals on a PC-bus edge connector. When more than one Minimodule is needed in a system, users can add the new module stacker card, which serves as a bus extender to the Little Board computers and can hold two Minimodule cards. Call Paul Rosenfeld, (408) 734-2980. DB

CIRCLE 305

STORE 600 MBYTES ON BACKUP TAPE DRIVE

A 3.5-in. form-factor cassette drive extends its capacity to 600 Mbytes without resorting to data compression or employing a longer tape. The MT2ST/N from Teac America, Montebello, Calif., features a 60-in./s tape speed and a 242-kbyte/s data-transfer rate. The number of recording tracks in the drive was increased from 17 to 21 and recording density has gone from 24,000 to 48,000 flux transversals/in. A cassette with a higher density is employed, but the drive retains the ability to read data written onto earlier, lower-density cassettes. In addition to high capacity, the drive adds some performance improvements over existing models, including a tension-control system that virtually eliminates the instantaneous-speed-variation problems associated with other backup-tape systems. Call Michael Helsel, (213) 727-0303, x. 786. RN

CIRCLE 306

VISION SYSTEM GAUGES FIDUCIAL-MARK QUALITY

Placement of surface-mounted devices leaps forward with the introduction of the visual fiducial-quality meter from International Robomation Intelligence (IRI), Carlsbad, Calif. Foil fiducial marks are used by vision systems to register component placement. If the fiducial marks placed by board suppliers are obscured by inconsistent hot-air-leveled solder, they can appear misshapen to the placement equipment. This can limit or ruin placement accuracy, which may be critical with fine-pitch devices and tape-automated bonding techniques. The meter assigns quality grades to fiducial marks ranging from 100, for a perfect mark, to zero, for one that's missing. IRI's Supravision computer, which powers the meter, is based on a 68020 host CPU operating at 16 MHz. Typical fiducials can be measured in under 1 second. The meter starts at under $40,000. Contact Donald Mead, (619) 438-4424. DM

CIRCLE 307

15-V CHOPPER OP AMP HAS ON-CHIP CAPACITORS

The LTC1150 chopper stabilized op amp from Linear Technology, Milpitas, Calif., plugs into any standard 8-pin DIP socket, runs off $\pm$15 V, and needs no external capacitors. Moreover, the capacitors are on the chip rather than in the package, which drops the cost to just $3.90 each in hundreds. The 1050 is built on a proprietary, 36-V CMOS process. Maximum offset voltage is just 5 μV. More importantly, maximum offset drift is only $\pm$0.05 μV/°C. Input voltage noise with a 100-Ω source resistance typically runs 0.6 μVpk-pk in the band from 0.1 to 1 Hz; 1.8 μV from 0.1 to 10 Hz. Minimum open-loop gain and common-mode rejection ratio run 140 and 120 dB, respectively. The op amp typically slews at 3 V/μs, and unity-gain bandwidth is 2.5 MHz. Operating from $\pm$15-V rails, it draws just 1.8 mA (maximum) of supply current and can put $\pm$13.8 V across 10 kΩ. Extended industrial and military grade devices are available in small quantities. Call Bill Reutelhuber, (408) 432-1900. FG

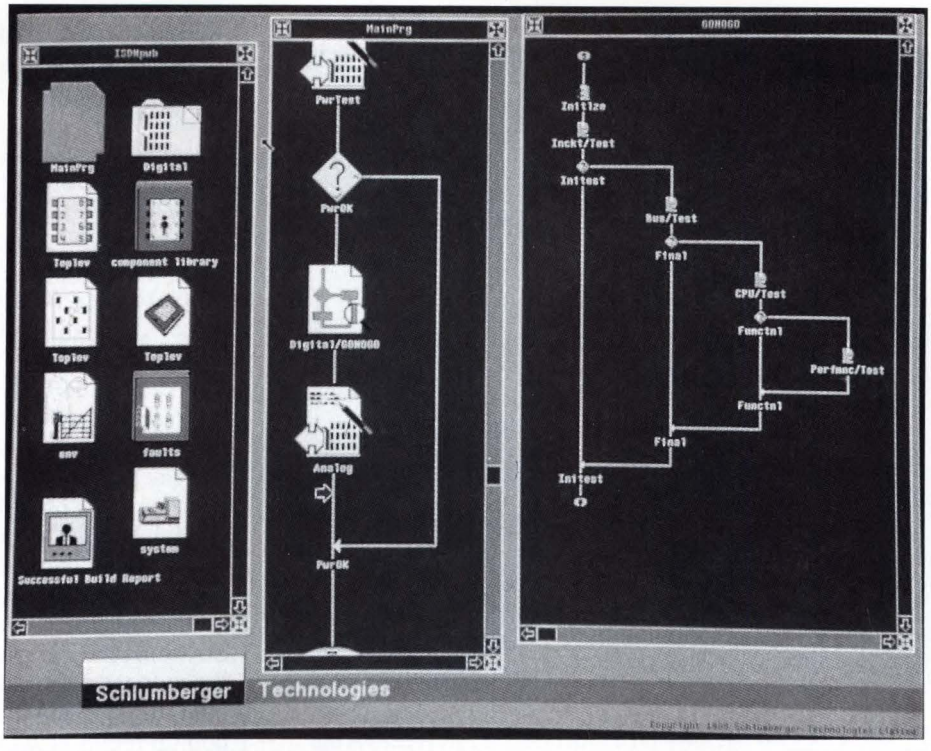
CIRCLE 309

GET 600-V, 50-A IGBTs IN INSULATED PLASTIC TO-3P

A pair of insulated-gate bipolar transistors (IGBTs) from International Rectifier, El Segundo Calif., the IRGPC40 and IRGPC50 switch 600 V at 37 A and 50 A, respectively. Peak repetitive currents are four times continuous current. Collector-emitter saturation voltage for the 50-A device is 2.4 V at 30 A and 3 V at 50 A; for the 37-A IGBT, 2.8 V at 21 A and 4 V at 37 A. Maximum turn-off delay time for both devices is 1 μs; effective turn-off time for both is typically 320 ns. IGBTs are voltage controlled, like power MOSFETs: They simplify drive circuitry and, when turned on, behave like bipolar transistors in that they control high currents at high voltage and have a low forward drop. Both IGBTs come in plastic TO-3P packages with an insulated mounting hole. Consequently, neither of them need an insulated mounting bushing—metal contact is made to the heat sink. In quantities of 1000, the IRGPC40 costs $610; the IRPGC50, $14.46. Call Bruce Watson, (213) 607-8899. FG

CIRCLE 310

EDITED BY CLIFFORD METH



1. THE ICON-BASED STRATEGIZER module displays a flowchart of the test program, showing the sequence of execution and the location of conditional jumps and repeat loops.

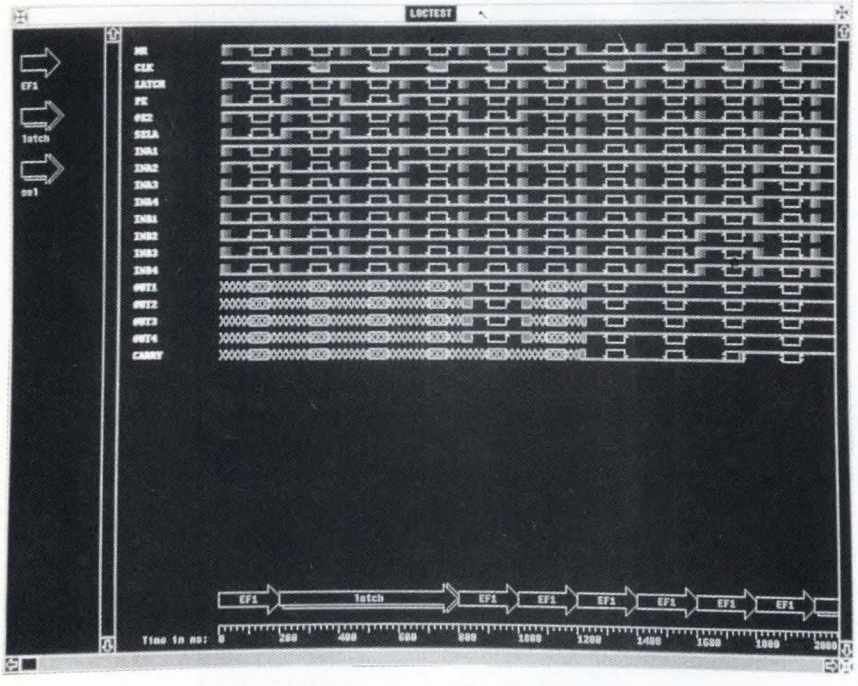
BOARD TESTER USES AI TO DIAGNOSE FAULTS

JOHN NOVELLINO

Many people in the electronics business foresee the decline of test engineering as a separate discipline. They envision improving design-to-test links that quickly and automatically translate simulation data into the thousands of test vectors that can take so much time and effort to write. When that happens, according to this scenario, technicians can perform the test function.

Not so, say the planners at Schlumberger Technologies ATE Div. In their view, test engineering is too complex and important to be displaced by automatic test-vector generation. To back this up, Schlumberger developed the S790 mixed-signal board tester, which relies heavily on a concept the company calls computer-aided test engineering (CATE). CATE uses advanced software and workstations for test-program generation, fault simulation, debugging, fault isolation, and data collection.

The new tester is based on Schlumberger's belief that automatic test equipment (ATE) in the coming decade must not merely find faulty boards—it must also supply the engineer accurate failure and repair data. Using this information, operators can improve yields by quickly and economically repairing bad boards. In addition, the data will help designers understand where process improvements are



2. USING THE DIGITAL WORKBENCH MODULE, programmers can create and edit digital activity by placing the appropriate edges with mouse strokes.

needed.

The S790 comprises high-performance tester hardware. It can include up to 960 universal test pins or 3840 Flexpins using Schlumberger's 8:7:1 pin-multiplexing scheme. The system can run at a 40-MHz data rate, with edge-placement resolution of 200 ps and edge-placement accuracy within ± 3 ns. Pin memory is 16k by 4 bits, and scan memory is 64 Mbits.

The real power of the S790 is in the software developed to run on the system. With the package, engineers can create diagnostic test programs that pinpoint a fault's location. Key elements include the Strategizer—an icon-based module for graphically building, running, and debugging test programs; and Digital Workbench, a set of tools for creating, monitoring, and modifying graphical waveform signals. Another important module is Analyst, an object-based, rule-oriented expert (artificial intelligence) system that uses about 50 heuristic algorithms to analyze test results and locate faults.

The S790, which is compatible with older S700 testers, features a modular open architecture. Included are a Sun 3 workstation running on a Unix operating system with X-Windows, a 68020-based tester controller that runs on real-time PSOS, universal digital pin electronics, a digital timing subsystem, analog matrixes, and an analog subsystem. Users can design a test strategy with any of the conventional test techniques: digital functional testing through simulation, scan chains, analog function testing, and both digital and analog in-circuit testing (including full cluster tests and diagnostics).

Unlike conventional design-to-test aids that offer a one-way path from the design task to the test environment, the S790 offers a bidirectional link. This link imports data from CAE/CAD tools and simulators and exports information to them. As a result, users can start in the test environment, write a program, and then export it to the design engine for simulation. Because the same database can be used, only one file is needed for the design and test information.

Industry standard formats and various optional software modules maximize flexibility. For schematic and board layout data, the EDIF 2.0 and Gerber formats are used. Furthermore, the CAD data interchange format (CADDIF) makes it possible for data exchanges with various simulators. For easy networking, the system is based on an Ethernet communications protocol (DECNet or TCP/IP). Consequently, existing Unix-based systems can quickly be integrated into the S790 system.

Strategizer, a standard module, helps users develop a hierarchical test plan. The software displays a flow diagram of live icons, a graphical representation of the test plan showing the sequence of execution, and the location of conditional jumps and repeat loops *(Fig. 1)*.

Each cluster test database resides in its own folder beneath the Strategizer folder. Operators edit and manipulate a cluster subtest plan using Strategizer. The graphical test plan is produced either manually with the help of the module's background pop-up menu or by Capital APG, an optional module that automatically generates in-circuit test programs.

With the exception of the Start and Stop icons (green and red traffic signals), the test icons, which contain menus, can be opened, deleted, copied, and moved with a mouse. All underlying databases move with the icon, with Strategizer taking care of file management. Using the zoom capability, the programmer can switch from the display of the entire test plan to a smaller, enlarged segment.

Schlumberger describes Digital Workbench as the "digital input/output window" to the S790 and external simulators. The optional module, which resides on CADDIF, automatically generates the simulator net list and input language, creating the bidirectional link between the tester and the simulator.

With simulation results displayed on Digital Workbench, the programmer can quickly identify problem areas, modify the input vectors, and perform a new simulation. The same vectors are then used in test execution. As vectors are added and edited, the Validator module (standard) ensures that the test program is syntactically and operationally correct.

Digital Workbench supplies a structured edge-placement format.

BOARD TESTER

The programmer creates and edits digital activity by locating the appropriate edges using mouse strokes *(Fig. 2)*. The software automatically places the edges in valid positions as determined by the timing definitions. Measure positions may also be placed and viewed graphically.

The programmer can group signal waveforms and their associated timing together to create a protocol, such as a read or a write cycle. The protocol can then be dragged to any location in the test program and stored in the icon field for use in other test programs.

Analyst is a sophisticated software package that can call on a wide variety of diagnostic tools that use artificial intelligence techniques to pinpoint the cause of the failure—to a specific component or small number of components, rather than to a node. Analyst uses fault dictionaries, fuzzy fault dictionaries, and context-dependent probing to locate the problem. The software was originally written in Prolog on a Sun Microsystems platform, then hard coded for the S790.

System diagnostic prompts guide the operator through the process. The software includes operator error-detection and error-recovery routines to ensure accuracy. A picture of the board layout on the screen helps the operator through the probing process.

All debugging information is communicated to the various editors and displays. To facilitate the repair process, the graphical tools track the failure. Consequently, as Analyst directs the operator to probe a point, the schematic, the Gerber files, and Digital Workbench track the movements of Analyst and the operator. They then display the correct interactive information.

The S790 comes with a power-tiltable test head with slots for 30 universal modules and 8 analog matrix modules. Testing capability depends on which of the three digital and two analog module types are installed.□

PRICE AND AVAILABILITY

The S790 costs from $500,000 to $1.2 million, depending on the hardware and software modules selected. Deliveries will be written 90 to 120 days after receipt of order, starting in the first quarter of 1990.

Schlumberger Technologies, ATE Div., 1601 Technology Dr., San Jose, CA 95110-1397; (408) 437-9031. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	557
MODERATELY	558
SLIGHTLY	559

IMAGING SUBSYSTEM BOASTS FIRST-CLASS GRAPHICS

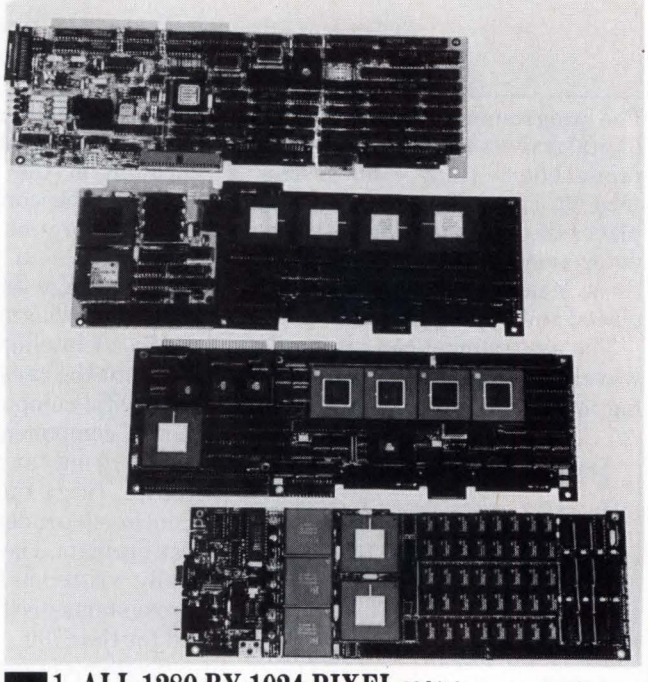
BOARD FAMILY FOR THE PC/AT COMBINES REAL-TIME IMAGE PROCESSING WITH HIGH-RESOLUTION GRAPHICS.

LAWRENCE CURRAN

High-resolution graphics and real-time image processing usually dictate the use of two different dedicated computers. But Matrox Electronic Systems Ltd. has now merged both into one system. Its Image Series board set combines real-time processing with 1280-by-1024-pixel graphics and imaging in one scalable platform. As a result, the board set transforms an IBM PC/AT into a high-speed, high-resolution imaging work station.

The Image Series puts 1280-by-1024-pixel, 32-bit image-processing resolution at the hands of AT-class PC users, where most imaging applications are done at 640 by 480 by 8 bits. Furthermore, use of the Texas Instruments TMS34020 graphics microprocessor and TMS34082 floating-point coprocessor speeds up imaging applications by 2 to 10 times, compared with Matrox' existing 640-by-480-pixel MVP-AT product.

The series packs onto three boards "all of the functions that today's boxed image-processing systems do and then some," says Lorne Trottier, president of Matrox, Dorval, Canada *(Fig. 1)*. That's largely made possible by the company's use of the 34020 as an intelligent imaging subsystem controller, in conjunction with a modular hardware architecture, high-level software tools, and high-speed graphics. According to Matrox engineers, that versatility challenges the sophistication of



1. ALL 1280-BY-1024-PIXEL 32-bit image-processing functions generally supplied by box-level systems for PC/ATs are now available in a three-board set from Matrox. The three boards include a controller (two different-resolution versions), a monochrome digitizer and acquisition, and a real-time processor.

standalone boxed imaging systems.

Real-time image processing is the ability to process 30 frames of 512-by-512-pixel data per second. The Image Series runs at a 15-MHz processing rate, which translates into 50 frames/s. "That means that the new family's hardware execution time for a 3-by-3 convolution—a typical image-processing function—is one frame time compared with 10 frame times for the MVP-AT," says Danny Mueller, a Matrox integration specialist. That works out to between 1/30 and 1/50 of a second, versus 1/3 of a second for the older board.

Mueller points out that graphics is becoming more important in image processing. This is where the 34020 fits in, whether the task is as simple as annotating images or as complex as implementing user interfaces, such as the X Window standard. "Image-processing boards usually require users to sacrifice part of the image buffer to handle graphics overlays," Mueller notes. "We overcome this by using a separate overlay buffer for graphics."

According to Mueller, graphics drawing should also be very fast to implement an interactive-windowed interface. "For example, when users re-size a window, it should happen immediately," Mueller contends. "Similarly, the display must draw in the overlay buffer while images are processed in the image buffer." Use of the graphics engine and coprocessor, along with Matrox' library of high- level graphics primitives, fulfills those needs.

The initial Image Series consists of three boards that fit into AT-host work stations and systems for medical imaging, printing and publishing, satellite imaging, training, and simulation. The controller board (IM-1280) is the intelligent subsystem and display controller. It delivers 1280-by-1024-pixel 32-bit resolution. Another baseboard version is offered for applications that require a resolution of 640 by 480 pixels.

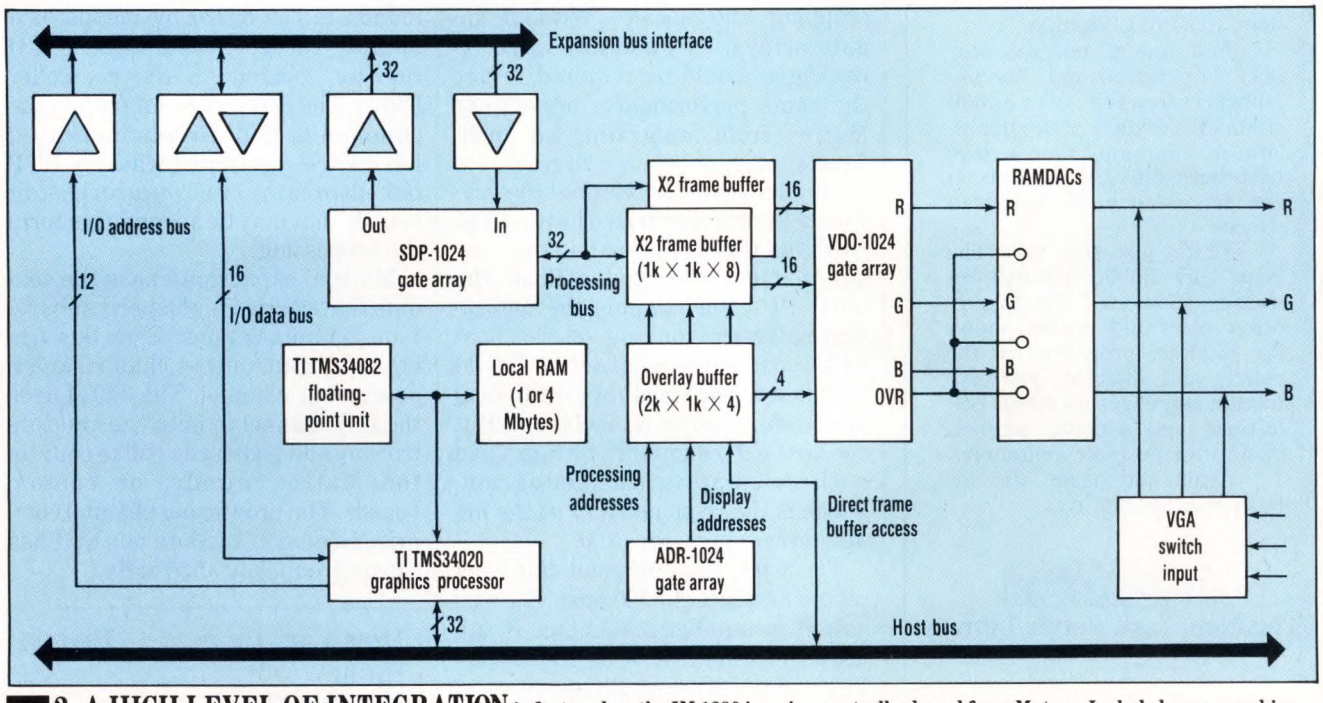
The IM-ASD monochrome acquisition and digitizer module and the IM-RTP real-time processor complete the initial series. Matrox is also developing additional boards for the family. One of the first will be the IM-CLD color acquisition and digitizer board, for release next March.

The 34020 on the controller board is the subsystem CPU, which performs command interpretation, interrupt-driven processing-hardware control, and graphics generation. This performance frees the AT-host system processor of those functions. Depending on the controller board version used, the display resolution can be tailored to deliver either a landscape format of 640 by 480 pixels or 1280 by 1024 pixels. It can also deliver a portrait format of 1024 by 1280 pixels or 480 by 640 pixels. It accommodates European display formats under software control.

The controller board also has two types of buffers, local RAM, the RAM digital-to-analog converters (RAMDACs) that directly drive the display, and three gate arrays *(Fig. 2)*. The buffers consist of a 2048-by-1024-pixel 4-bit graphical overlay, and four 1024-by-1024-pixel 8-bit main frame buffers to store digitized image-frame data.

The overlay and main frame buffers can be independently panned, scrolled, and zoomed. The main frame buffers can also be reconfigured under software control, creating, among other things, 32-bit-deep buffers for true color applications.

One CMOS gate array (SDP-1024) is a serial data processor, which controls data distribution over the subsystem's internal expansion bus,



2. A HIGH LEVEL OF INTEGRATION is featured on the IM-1280 imaging controller board from Matrox. Included are a graphics processor, a floating-point unit, RAM, RAMDACs, frame buffers, an overlay buffer, three gate arrays, and a VGA switch.

IMAGING BOARD FAMILY

PRICE AND AVAILABILITY

The IM-1280 baseboard/controller board, IM-ASD monochrome acquisition and digitizer board, and the IM-RTP real-time processor board will all be available in December. The IM-CLD color digitizer is scheduled for shipping in the first quarter of 1990. Prices for single quantities in U.S. dollars are $9995 for the IM-1280, $1995 for the IM-ASD and IM-RTP, and $4995 for the IM-CLD.

Matrox Electronic Systems Ltd., 1055 St. Regis Blvd., Dorval, Quebec, Canada H9P 2T4; (514) 685-2630. **CIRCLE 513**

"acting as the interface device between the frame buffers and the outside world," Mueller says. Another gate array (ADR-1024) is the address generator, generating four sets of processing addresses simultaneously for the main frame buffers and two sets of display addresses for the overlay buffer.

The third gate array (VDO-1024) supplies display data to the RAMDACs, acting as a multiplexer that drives the display, as well as giving the display such effects as zooming, cropping, and mosaics. Without the gate arrays, substantially more IC packages would be required to get the same performance, preventing Matrox from integrating so much functionality onto three boards.

Mueller says it's essential that the IM-1280 controller board have a local CPU "so that it can manage the imaging subsystem and offload the host CPU." For example, the application software running on the host CPU must decide what action should be taken as the result of a statistical operation, such as a histogram. But the host CPU shouldn't be burdened with calculating the histogram, which is the responsibility of the image-processing subystem.

The 34082 floating-point chip complements the CPU because it's well suited to number-crunching. It can draw in formats of 4-, 8-, 16-, and 32-bit pixels in either of the two types of buffers, assuring high-speed drawing as well as flexibility.

The IM-ASD monochrome module and the planned IM-CLD color acquisition module is to acquire images. The monochrome unit takes inputs from any analog source between 0 and 15 MHz, including RS-170 cameras. It can also handle input signals from any 0-to-30-MHz digital source, including cameras and scanning-electron microscopes.

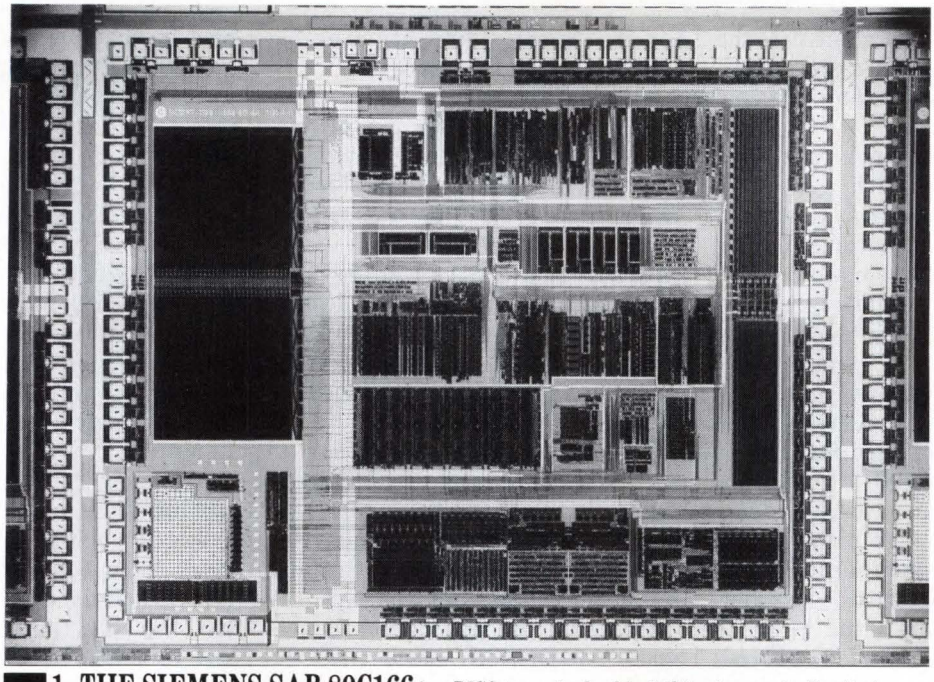
The IM-RTP board rounds out the subsystem. It's the real-time image-processing heart of the family, controlling point-to-point transforms; spatial filtering, including convolutions; binary, gray-scale, and high-level morphology; statistical functions, such as histograms; and object analysis. The board processes data directly from the digitizer boards or the frame buffers at a sustained rate of 15 MHz, or 50 frames/s for 512-by-512-pixel images.

A two-layer software approach in the Image Series simplifies the work of application programmers. Board-resident software runs on the local CPU—the 34020; a host layer runs on the host processor. Code that runs on the local CPU performs the graphics, image processing, acquisition, and display functions.

Host-resident code issues commands to the 34020 by means of a memory-mapped command FIFO register located on the controller board. The 34020 then interprets the commands and directs dedicated hardware, including the IM-RTP board or any custom-processing boards that may be added to perform the processing.

Matrox' expansion bus is the conduit that carries high-speed subsystem communications. That bus has both an input/output channel and a processing channel. The 34020 uses the I/O channel to initialize and control any add-on boards still to come in the Matrox family, or custom boards. The processing channel comprises a dual 32-bit data bus that has a peak frequency of 30 MHz.□

HOW VALUABLE?	CIRCLE
HIGHLY	563
MODERATELY	564
SLIGHTLY	565



1. THE SIEMENS SAB 80C166 is a RISC-type, single-chip 16-bit microcontroller that meets high-performance, time-critical requirements of real-time embedded control applications. Using the company's 1-μm ACMOS (advanced CMOS) technology, the device comes in a 100-pin plastic quad flatpack.

MICROCONTROLLER REACHES NEW PERFORMANCE LEVELS

JOHN GOSCH

If you're designing a high-performance data-communications system, you'll probably need a microcontroller to handle the higher level portions of the communication protocols. However, you also need a second controller that, working with the first one, controls the lower-level functions. This two-controller scheme with the necessary subsystems, such as peripherals and clocks, is a costly solution.

Another example is illustrated in automotive electronic design. For engine management, a standard microcontroller is generally used. But with this microcontroller, you can build a system that only partially controls just one cylinder. The other cylinders, which are offset by a constant timing factor, simply follow the first one. The problem is that as engine conditions change, a simple offset in timing from cylinder 1 isn't an optimum solution. What's needed is a microcontroller with higher performance so it can actively control not just one, but all cylinders in parallel. The answer is the SAB 80C166, a RISC-type single-chip 16-bit CMOS microcontroller system from Siemens AG that offers high performance and an economical solution to your design problem *(Fig. 1)*. It is the first member of a controller family using an architecture of the German company's design.

The 80C166 meets the high-performance, time-critical requirements of real-time embedded control applications. According to Siemens, the 80C166 is up to 20 times more powerful than competitive 16-bit controllers, depending on its use. And for

$25 to $40 in volume quantities, the 80C166 delivers much more performance and integration than similarly priced devices.

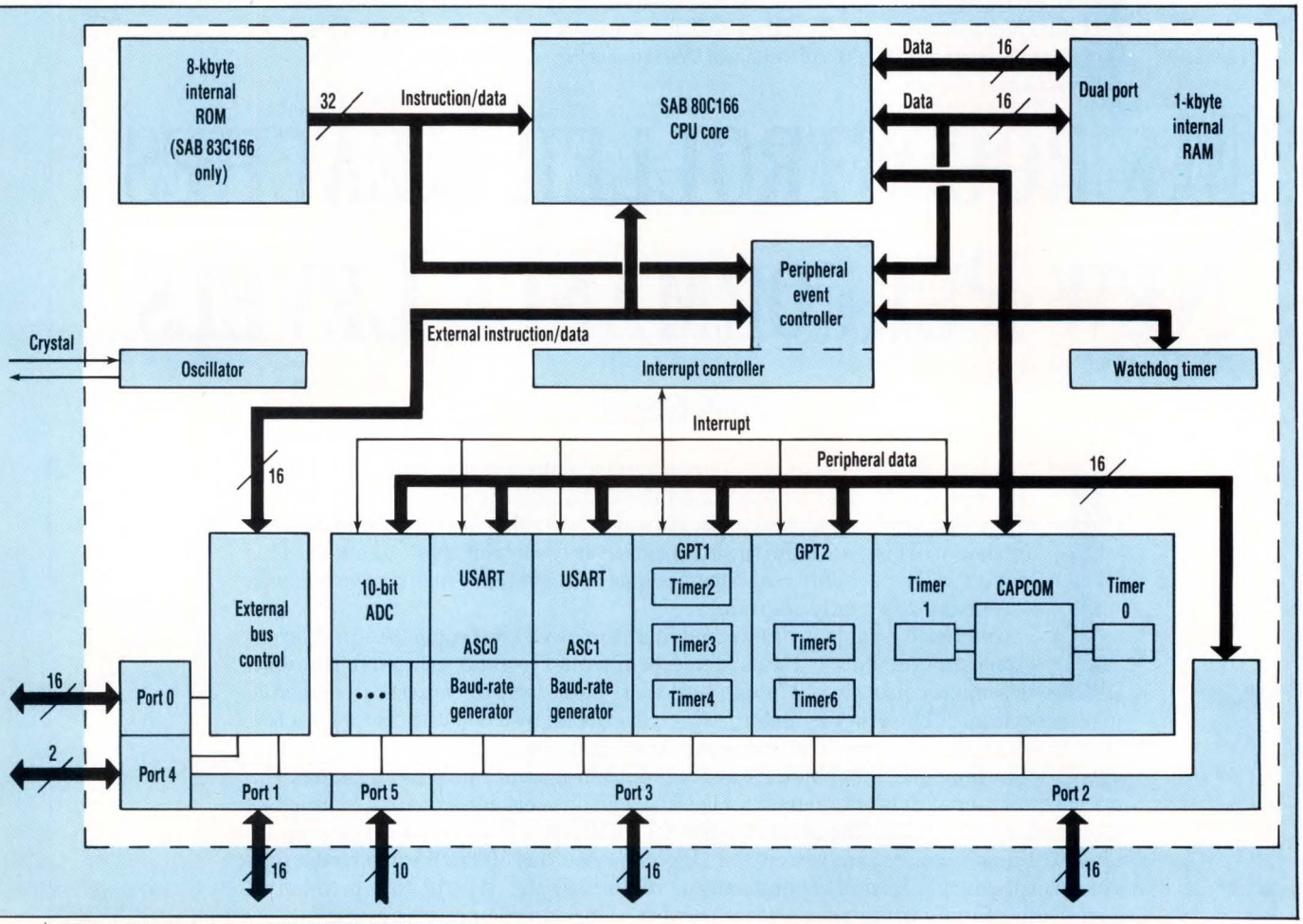
The controller boasts a 100-ns machine cycle time with a 20-MHz clock—most instructions are executed in one cycle. According to Siemens, that performance was achieved only in digital-signal and RISC processors, not in a single-chip microcontroller.

The interrupt response time is 400 ns under worst-case conditions when instructions are fetched from internal ROM, compared to 1 to 5 μs for competitive devices. Another advantage is the four-stage pipeline concept, which is common for RISC processors but not for a microcontroller. Furthermore, there's the large 16 Mbyte memory space (256 Kbytes for the family's first member because of package limitations).

The 80C166 owes its high performance to an architecture that combines the best features of a microprocessor with those of a microcontroller. Specifically, it brings together a processor's high computational speed, large address space, easy programmability, and flexible addressing modes, and a controller's task-oriented architecture, fast interrupt response, and widely configurable system of peripherals.

It's this concept, in addition to such other features as four-stage pipelining and a small internal branch cache, that has made the 80C166 more powerful than existing 16-bit controllers, Siemens says. Depending on the application, benchmark comparisons show that the new device is 10 to 20 times more powerful than Intel's 80C196 and twice as powerful as Motorola's 68020. Its closest competitor is Motorola's 32-bit 68332.

While high performance is achieved through a new architecture, economy is obtained through high systems integration. The 80C166 incorporates three independent subsystems: a programmable interrupt controller, a high-performance microprocessor, and independent intelligent peripherals *(Fig. 2)*. Consequently, the device sharply contrasts with classical embedded systems built up with discrete subsystems, such as a microprocessor, clock generator, interrupt controller, and peripherals—systems that have reached the limits of cost and size to suit today's complex control



2. THE 80C166 INCORPORATES three independent subsystems: a programmable interrupt controller, a high-performance microprocessor, and independent intelligent peripherals. Siemens also offers the SAB 83C166, which is the same controller version but with an 8-Kbyte internal ROM.

applications.

In the Siemens device, each subsystem is designed so that many real-time events can be processed while supplying a large amount of computational power. With this design, new embedded control functions can be incorporated—an impossibility with today's controllers.

The modular peripheral subsystem can either be expanded to give greater functionality or be made smaller to reduce cost. This concept, implemented at the initial design, will enable Siemens to quickly make available a controller family that meets specific embedded-control market requirements.

With the on-chip interrupt subsystem, up to 64 independent incoming peripheral interrupts can be prioritized every 100 ns. You can program each interrupt source to any of 16 priority levels, independent of the peripheral used. As a result, extra polling and control software aren't needed to determine the highest priority event. Because each interrupt mode contains the same hardware and features, Siemens can easily modify the size of the interrupt subsystem so that unessential hardware isn't required for other family members.

PRICE AND AVAILABILITY

Housed in a 100-pin plastic quad flatpack and made with Siemens' 1-μm advanced CMOS (ACMOS) process, the 80C166 will be offered as samples during the first quarter of 1990. Volume prices will be $25 to $40. The 83C166, which includes an 8-Kbyte internal ROM, will also be offered in early 1990. Both the ROM-less 80C166 and the ROM-carrying 83C166 will enter full production in early 1991.

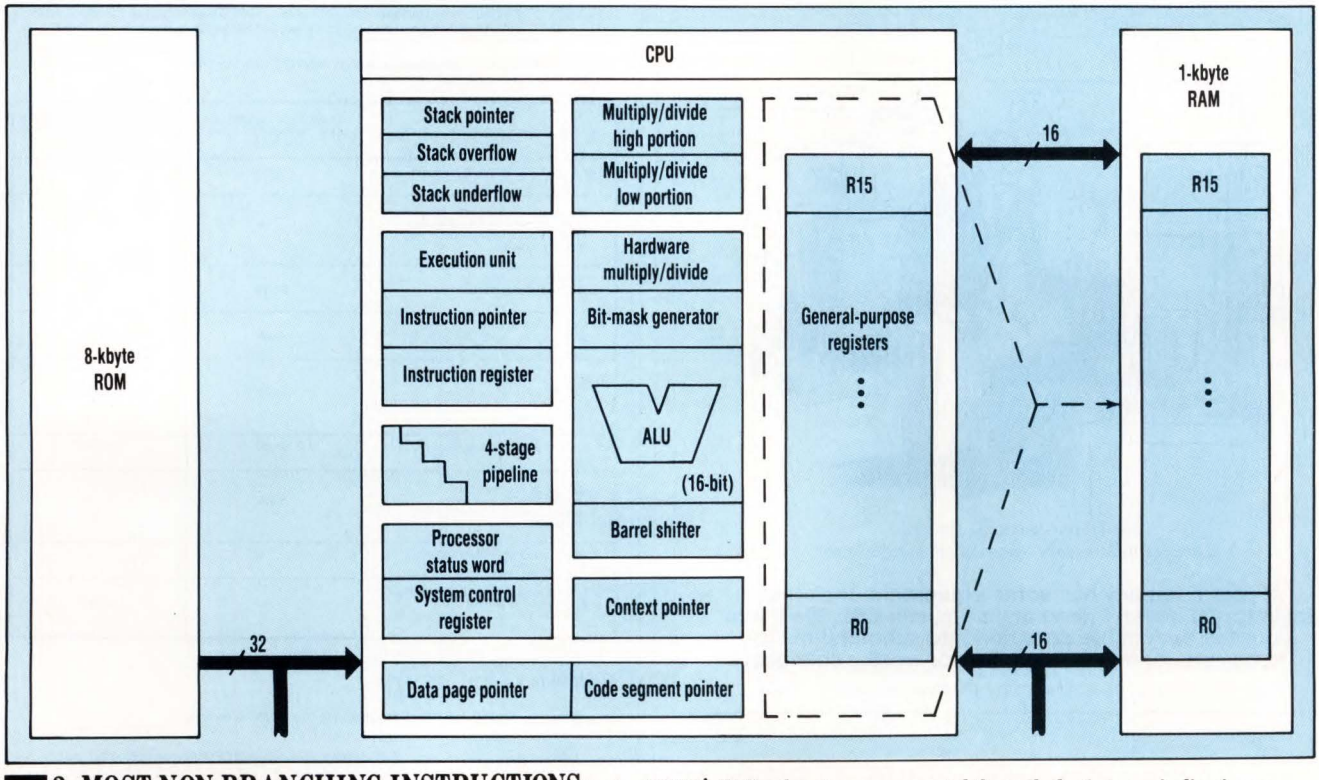
Siemens AG, Semiconductor Division, P. O. Box 801709, D-8000 Munich 80, W. Germany. Siemens Components Inc., 2191 Laurelwood Rd., Santa Clara, Calif. 95054; (408) 980-4583.

CIRCLE 512

Also contributing to the 80C166's performance is direct memory access (DMA), implemented with a peripheral event controller. This PEC, which is part of the interrupt subsystem, lets any interrupt request perform a byte or word transfer from any peripheral or memory location to either another peripheral or memory without interrupting the CPU. Thus, you can reprogram any peripheral, store new data, collect data, or perform a DMA transfer within memory without incurring the penalties of entering or exiting a software interrupt procedure.

The 80C166's microprocessor subsystem includes a high-level language-oriented instruction set, RAM and ROM, a clock, and an external bus controller *(Fig. 3)*. Most nonbranching instructions are executed through the four-stage pipeline in one 100-ns machine cycle. Non-loop branch instructions are executed in two machine cycles, and a small branch cache is also included to reduce delays to one cycle inside user loops.

With the 80C166, you can also move the general-purpose register set to any location within the internal RAM in one machine cycle. This avoids costly pushing and popping of



3. MOST NON-BRANCHING INSTRUCTIONS in the 80C166's CPU subsystem are executed through the 4-stage pipeline in one 100-ns machine cycle. A small branch cache reduces branch delays to one cycle inside user loops.

registers before and after switching from one task to another.

The CPU's bus controller supports three bus types, enabling you to link to either a low-speed external 8-bit multiplexed bus, a medium-speed 16-bit multiplexed bus, or a high-speed 16-bit demultiplexed bus. The bus configuration, some bus control signals, and a wait-state generator are user-programmable. Consequently, the number of required external interface chips is minimized.

The peripheral subsystem was designed to quickly introduce new family members, offer a standard environment for users, reduce CPU dependence, and adapt to a multitude of embedded control tasks.

The 80C166 has six independent peripherals: a 10-bit, 10-channel successive-approximation analog-to-digital converter, a 16-channel capture-compare (CAPCOM) unit for signal tracing and generation with two independent timers, a general-purpose timing (GPT) unit with five timers, a programmable watchdog timer unit for system security, and two serial-channel interface units with independent baud-rate generators that can support communications up to 2.5 Mbaud.

As new embedded systems' integration and functionality become greater, the cost of programming and debugging these systems has increased dramatically. Siemens' goal in developing the 80C166 was to give users a new design environment so that they could quickly integrate the device into new and existing designs.

This was accomplished by supplying high-level-language compatibility, accessibility to low-level functions, and an efficient and consistent user interface to powerful tools. These tools include a macro-assembler, linker, locator, library manager, software simulator, C-compiler, and hardware emulator. Consequently, design time can be reduced and the reliability of target systems can be improved.

An embedded control application targeted by the 80C166 is the automobile, a sector that has long been a driving force in microcontroller development. In this field, controllers must meet stringent demands under real-time conditions as they exist.

Other uses are in the industrial field: robot control, process automation systems with distributed intelligence, and controlling asynchronous, servo, and stepping motors. The 80C166 also suits the demands of data-communications equipment, such as hard disk drives.□

HOW VALUABLE?	CIRCLE
HIGHLY	560
MODERATELY	561
SLIGHTLY	562

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RISC-LIKE EPROM-BASED 8-BIT CPUS SPEED PROGRAM EXECUTION

TACKLE DEMANDING APPLICATIONS WITH 8-BIT RISC-LIKE MICROCONTROLLERS THAT KEEP SYSTEM COSTS MINIMAL.

DAVE BURSKY

Eight-bit microcontrollers already span a wide price and performance range: On the low end, low-I/O-count chips sell for about $1 in large quantities; on the high end, 8-bit chips with 64 I/O lines exceed $20. Chips at the low end of the price curve, though, suffer from low throughput, too, because throughput is sacrificed to minimize chip area and thus reduce cost. In addition, chip area is kept to a minimum by setting the architecture to perform tasks sequentially by shared hardware, rather than in parallel by multiple subsystems.

Striking a balance between small chip area and high throughput, a new family of microcontrollers from Microchip execute programs faster than any other 8-bit microcontrollers—achieving a peak throughput of 5 MIPS. The revamped PIC series of EPROM-based controllers deliver time-critical control solutions for under $3 per chip (in quantities of 2500). To achieve that price-performance point, Microchip's designers employed a RISC-like instruction set, a Harvard architecture, and a two-level instruction pipeline, to maximize throughput without making the chip too large.

The microcontrollers are an extension of the old PIC family originally made under the General Instrument label. Microchip reconstructed the CPU architecture so one instruction can be decoded while another is being executed. With a 20-MHz clock and an internal divide-by-four circuit to create timing edges, instructions on the 16C5x family execute in as little as 200 ns (branch operations require 400 ns because the pipeline register must be cleared, too).

Most instructions, which are 12-bits wide, execute in just four oscillator cycles, with branches requiring eight oscillator cycles. In contrast, such popular microcontrollers as the Intel 8051 and the Motorola 68HC11 typically require 8 to 32 oscillator cycles to execute their simpler, byte-wide instructions. The extra four bits of the PIC's instruction words make it possible for more complex

RISC-LIKE 8-BIT MICROCONTROLLER

operations to be executed in one instruction. Consequently, smaller program memories can be used on the microcontroller chips.

To keep the chip area small—and chip price low—the company also elected to keep the on-chip resources of its initial family members to a minimum, with the first PIC family members, the PIC16C54 and 16C55, coming in 18- and 28-pin packages, respectively. Included on the two chips are just 512 words of EPROM for instruction storage, 32 bytes of RAM, an 8-bit counter-timer with 8-bit prescaler, a watchdog timer, and 12 and 20 I/O pins, respectively *(see the figure)*. Future controller versions will have more EPROM, RAM, and more and fancier I/O resources, such as analog-to-digital converters.

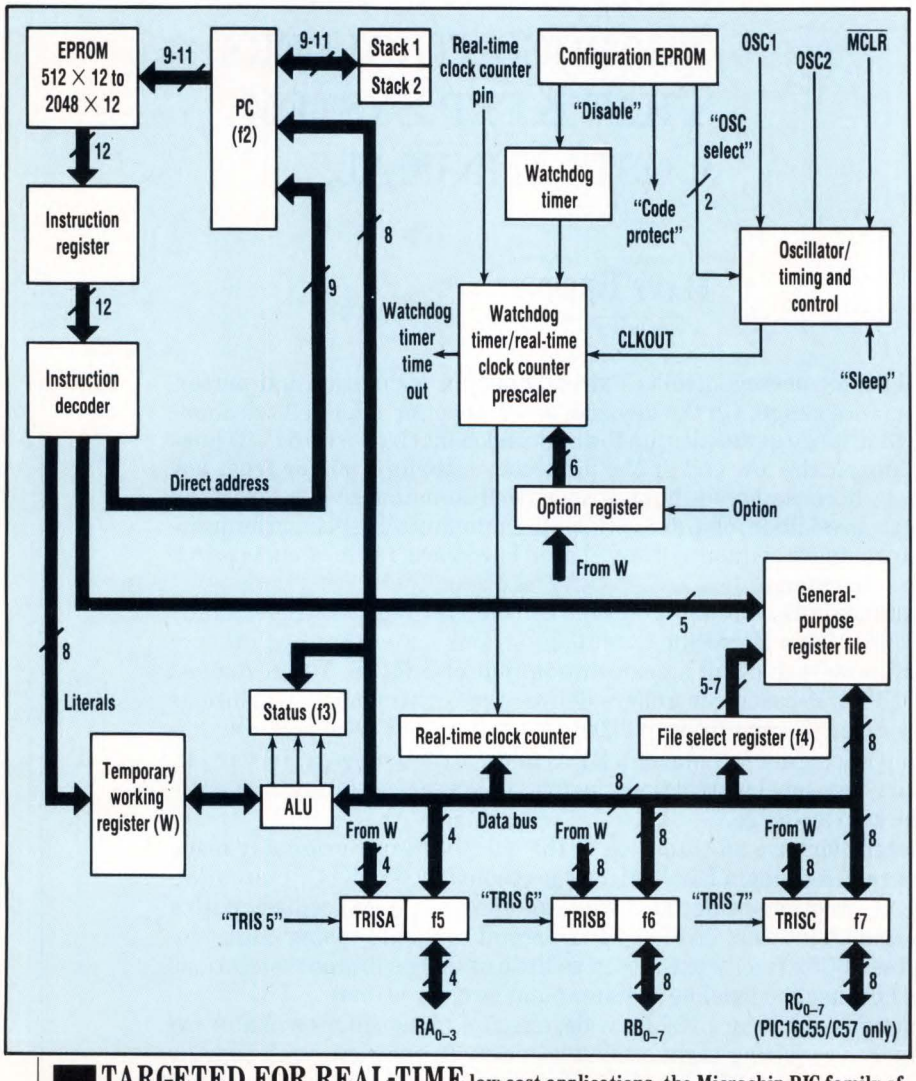
As with commands in the original PIC family, the 33 instructions are 12-bits wide and include most of the same commands, easing the migration to the new family for existing PIC users. The small instruction set also simplifies the designer's task of learning the commands before programming can start. Other popular microcontrollers typically have instruction sets of 50 to more than 100 commands, so they take longer to learn.

Thanks to the short, 200-ns instruction cycle time, the 16C54 and C55 have a peak throughput of close to 5 MIPS. With that high throughput, the chip can tackle real-time control operations. However, unlike most other microcontrollers that readily handle interrupts and can switch tasks quickly, the new PIC chips aim for single-task control operations. Furthermore, the on-chip pipeline, which gives the chip some of its speed, would have to be cleared for the program flow to divert. Some typical applications for the controllers include keyboards, pointing devices, disk controllers, keyless locks, scanners, remote controls, and cordless telephones.

The PIC controllers were also designed to operate over a wide range of temperatures, power-supply voltages, and clock frequencies. Versions of the chip are available for commercial, industrial, and soon for automotive temperature ranges. The circuits operate from a power supply that can range from 2.5 V to 6 V. Furthermore, designers have a choice of four clock-oscillator frequency ranges that make it possible for the chip power consumption to be optimized to the application.

Ernest Villicana, Microchip technical marketing manager, explains that rather than build one oscillator that can span the entire frequency range of operation, four separate oscillators are embedded in the chip, with one of the four to be selected by programming some UV EPROM control cells. By using four different oscillators, each can be optimized for different power or oscillation characteristics.

The lowest power option oscillates over a 32-to-400-kHz range, and at the lowest frequency, it keeps the typical operating current of the entire chip to just 5 mA (with a 2.5-V power supply). During standby, the chip current drops by more than 80% to less than 1 μA at 2.5 V—a value that holds true with any selected oscillator option. The second and third oscillator choices are basically the same but they give the option of using either a crystal or RC network. With either option, the oscillator generates a 400-kHz-to-4-MHz clock signal, causing the chip to draw 1.8 mA (at 4 MHz and 6 V). For peak performance, the fourth high-frequen-



TARGETED FOR REAL-TIME low-cost applications, the Microchip PIC family of controllers contains a minimal amount of on-chip resources, but they can execute the program many times faster then competing controllers.

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Clock Speed	Access Time	Max Output Enable Time
33 MHz	25ns	10ns
25 MHz	35ns	13ns

*All timing rated at 100 pF loads. The MT56C0816 is available in a 52-pin plastic leaded chip carrier (PLCC).

MICRON TECHNOLOGY, INC.

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CIRCLE 33

RISC-LIKE 8-BIT MICROCONTROLLER

PRICE AND AVAILABILITY

The PIC 16C54 and C55 microcontrollers from Microchip will come in 18- or 28-lead one-time programmable plastic or windowed reprogrammable ceramic DIPs as well as small-outline gull-wing and plastic leaded chip carriers. The DIP version of the one-time programmable 16C54 sells for $2.40 in quantities of 2500; the 16C55 costs $2.95. Production quantities are immediately available.

Microchip Technology Inc., 2355 W. Chandler Blvd., Chandler, Ariz. 85224-6199; Ernest Villicana, (602) 345-3315

CIRCLE 514

cy oscillator runs at between 4 and 20 MHz. At 8 MHz and 6 V, the chip still draws a small 5-mA operating current.

Both one-time programmable and windowed, reprogrammable versions of the PIC chips will be sold, but the oscillator choice option will only be available on the reprogrammable version. One-time programmable controllers will be sorted and configured prior to being packaged. As a result, one-time programmable versions will be offered with a preset oscillator option. In addition, the all of the PIC microcontrollers have an on-chip free-running watch-dog timer, which runs off its own RC clock and can be disabled by programming an EPROM cell. When the watch-dog timer is disabled, chip power consumption is further reduced.

Software development tools from Microchip are available for the PIC family. The PIC Pak software tool package and the Pices III real-time hardware emulator are the first two tools that will be hosted on an IBM PC or compatible. A version of the PIC Pak for the Apple Macintosh is in development and should be ready by year's end.□

HOW VALUABLE?	CIRCLE
HIGHLY	566
MODERATELY	567
SLIGHTLY	568

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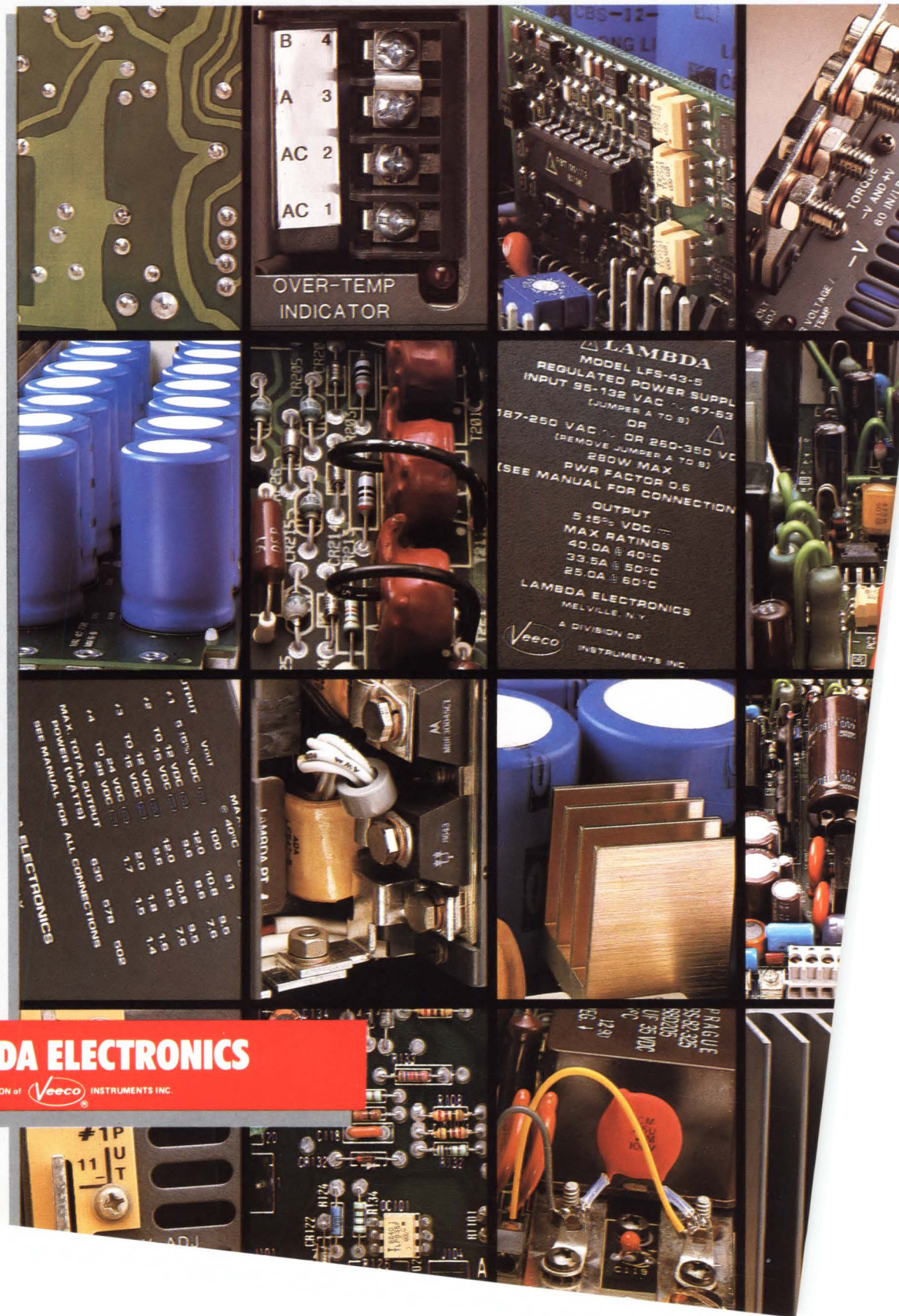

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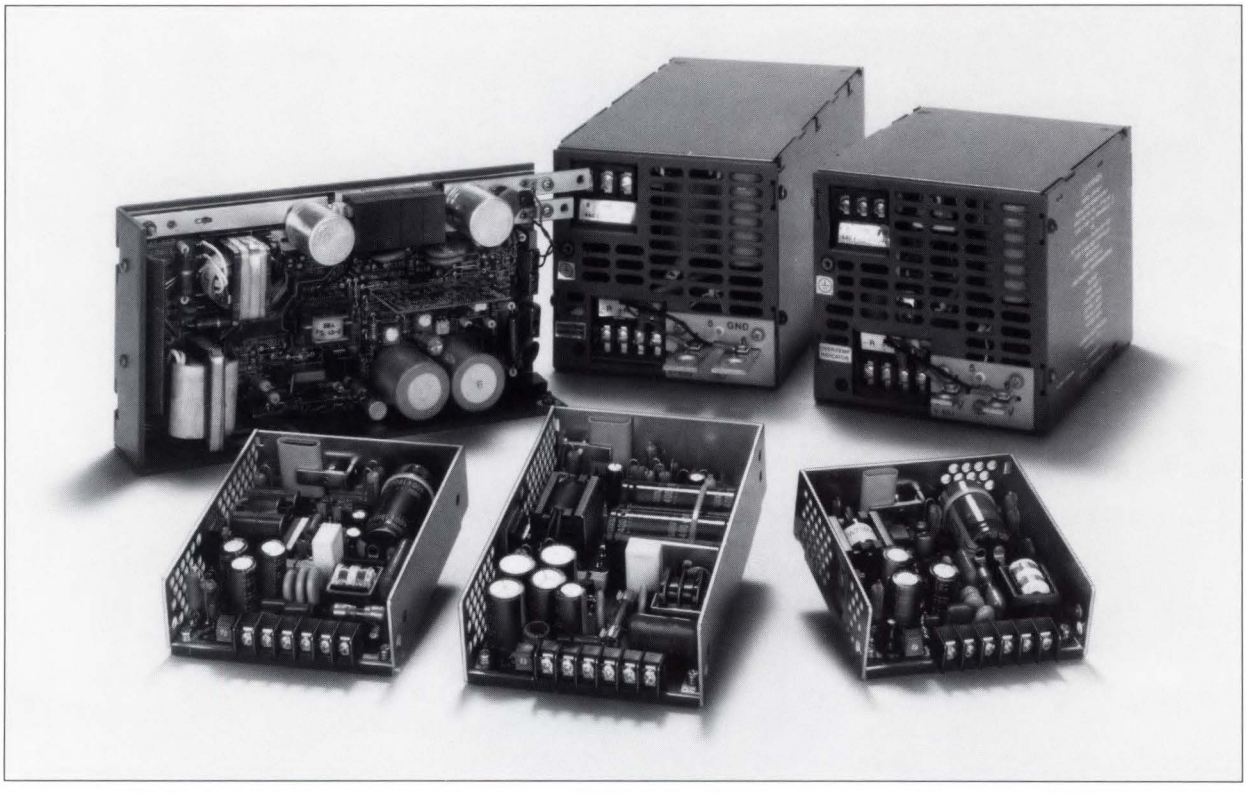
LFS Series:

THE INTERNATIONAL SOLUTION FOR INDUSTRIAL POWER SUPPLY APPLICATIONS



Industrial electronic equipment used in applications such as factory automation, process controls, etc., must be reliable. The consequences due to a failure can be costly and sometimes dangerous. Choosing the right power supplies for new equipment is a key element in the design process — especially when the operating conditions and geographical deployment are diverse and unknown. For example, line and load transients happen frequently in AC supply networks throughout the world, and it is generally accepted that the situation varies from country to country for a given type of industrial application.

Operating conditions for switching power supplies also vary for each application according to the ambient operating temperature, the possibility of AC line interruptions, and the characteristics of the DC load. The worst case combination occurs when switching power supplies are used at their maximum operating temperature and a step function of DC load (up to the maximum rated current) occurs at the moment an AC line interruption severely reduces the input voltage. Random failures can occur in power supplies which might otherwise appear suitable in terms of rating versus temperature, QA/QC standards etc.

Reliability starts with the design, and the LF Series embodies a unique control concept developed by Lambda which provides inherently reliable operation in transient line and load conditions. In addition, the LF Series allows increased power density up to 5 watts/inch^3. This design approach, coupled with the controlled manufacturing and quality standards (always expected of Lambda) makes the LF Series the natural choice in demanding industrial applications.

Now the LFS Series has been extended to include five new packages at 19W, 30W, 60W, 90W, and 125W.

FEATURES:

- Priced from 38¢/W.
- Up to 2.4kW
- Up to 5W/in^3
- International input of 85-265VAC on 19W, 30W and 60W models and 85-132VAC/170-265VAC on 90W and 125W models.
- Meets UL/CSA/TUV/IEC
- Industrial isolation ratings: 3750VRMS input to output; 1500VRMS input to ground; 500VRMS output to ground.
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LFS SERIES

Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line ..... 0.1% from 95 to 132VAC or 187 to 265VAC on LFS-43, 44, 45, 45A, 46, 47, 48. 85 to 265VAC on LFS-38, 39, 40. 85 to 132VAC or 170 to 265VAC on LFS-41, 42. 170 to 265VAC or 3 phase on LFS-49, 50.

regulation, load ..... 0.1% from 0 to full load.

ripple and noise ..... 15mV RMS, 75mV pk-pk for 2V, 5V and 6V models.
20mV RMS, 150mV pk-pk for 12V through 28V models.
35mV RMS, 200mV pk-pk for 48V models.

temperature coefficient ..... 0.03%/°C.

remote programming resistance ..... 1000Ω/V nominal.

remote programming voltage ..... volt per volt.

AC INPUT

line ..... 95 to 132VAC / 187 to 265VAC, 47-440Hz.
85 to 132VAC / 170 to 265VAC, 47-440Hz on LFS-41, 42 (user selectable). 85 to 265 VAC, 47-440Hz on LFS-38, 39, 40 (wide range input, no tap change). 170 to 265VAC, 47-440Hz single phase or three phase on LFS-49 and LFS-50.

power ..... LFS-38: 31.5 watts maximum.
LFS-39: 45 watts maximum.
LFS-40: 89.5 watts maximum.
LFS-41: 120 watts maximum.
LFS-42: 186 watts maximum.
LFS-43: 326 watts maximum.
LFS-44: 440 watts maximum.
LFS-45: 682 watts maximum.
LFS-45A: 682 watts maximum.
LFS-46: 882 watts maximum.
LFS-47: 1103 watts maximum.
LFS-48: 1470 watts maximum.
LFS-49: 2457 watts maximum.
LFS-50: 3220 watts maximum.

RMS current ..... 0.4A RMS maximum on LFS-38.
0.75A RMS maximum on LFS-39.
1.5A RMS maximum on LFS-40.
2.0A RMS maximum on LFS-41.
3.7A RMS maximum on LFS-42.
5.7A RMS maximum on LFS-43.
7.5A RMS maximum on LFS-44.
12.0A RMS maximum on LFS-45.
12.0A RMS maximum on LFS-45A.
15.0A RMS maximum on LFS-46.
18.0A RMS maximum on LFS-47.
25.0A RMS maximum on LFS-48.
22.0A RMS maximum (single phase); 16.0A RMS maximum (three phase) on LFS-49.
30.0A RMS maximum (single phase); 20.0A RMS maximum (three phase) on LFS-50.

EFFICIENCY
40% minimum on 2V model of LFS-38. 45% minimum on 2V models of LFS-39, 40, 41. 55% minimum on all other 2V models. 60% minimum on 5V and 6V models of LFS-38. 67% minimum on 5V and 6V models of LFS-39, 40. 68% minimum on 12V through 20V models of LFS-38. 70% minimum on 12V through 20V models of LFS-39. 71% minimum on 24V through 48V models of LFS-39. 72% minimum on 5V through 15V models of LFS-42. 73% minimum on 12V through 20V models of LFS-40. 74% minimum on 24V through 48V models of LFS-38, 40. 75% minimum on 5V through 15V models of LFS-41, 42, 43, 44, 45, 45A, 46, 47, 48, 49, 50. 78% minimum on 20V through 48V models of LFS-41. 80% minimum on all 20V through 48V models of LFS-42, 43, 44, 45, 45A, 46, 47, 48, 49, 50.

DC INPUT
110 to 370VDC on LFS-38, 39, 40. 230 to 370VDC on LFS-41. 260 to 370VDC on LFS-42, 43, 44, 45, 45A, 46, 47, 48 (unit must be wired for 220V configuration). 240 to 370VDC on LFS-49, 50.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
Continuous duty 0° to 60°C with suitable derating above 40°C. Guaranteed turn-on at −10°C with reduced specifications.

OVERLOAD PROTECTION
ELECTRICAL
External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

HOLD UP TIME
2V, 5V and 6V models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, Vo max and 105VAC input at 60Hz. 100 msec hold up when operating at maximum output power and 210VAC input at 50Hz on LFS-38, 39, 40 and 41. (When configured at 220V input: 20 msec holdup when operating at maximum output power and 210VAC input at 50Hz.)

IN-RUSH CURRENT LIMITING
All models are provided with in-rush current limiting to limit the current to a preset value.

OVERVOLTAGE PROTECTION
Non-crowbar, inverter shutdown type OV protection is standard on all models.

COOLING
LFS-38, 39, 40, 41, 42, 43, 44, 45 are convection cooled. LFS-45A, 46, 47, 48, 49, 50 are fan cooled.

DC OUTPUT CONTROLS
Simple screwdriver adjustment over the entire voltage range.

INPUT AND OUTPUT CONNECTIONS
All input, sensing and remote on/off connections are made via PC board mounted terminal block. DC output connections are made via heavy duty bus bars (LFS-38, 39, 40, 41 are PC board mounted terminals). Ground connections are made via chassis stud.

MOUNTING
One mounting surface and one mounting position on LFS-38, 39, 40, 41, 42, 43, 44, 45. One mounting surface, multiple mounting positions on LFS-45A, 46, 47, 48, 49, 50.

REMOTE TURN-ON / TURN-OFF
TTL compatible signal enables remote turn-on/turn-off of the power supply. A voltage of 2.8V to 5.0V applied to remote on/off terminals will initiate turn-off. Open circuit or short circuit condition, or a zero to 2.8V signal will cause turn-on.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation.

ISOLATION RATING
3750V RMS input to output (8mm spacing). 1500V RMS input to ground. 500V RMS output to ground.

CURRENT SHARING
The LFS-49 and LFS-50 have internal circuitry that allows units operated in parallel to share load current. Effects of different supply ambient temperatures are compensated for. For example, the hottest unit will automatically supply less load current. A single additional connection must be run between the supplies. This connection is available on the terminal block.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LFS-38	0.58	1.58	1.38 × 3.82 × 3.54
LFS-39	0.74	1.74	1.38 × 3.82 × 4.53
LFS-40	1.03	2.03	1.46 × 3.82 × 6.02
LFS-41	1.25	2.25	1.78 × 3.82 × 6.30
LFS-42	1.30	2.30	1.9 × 4.75 × 5.687
LFS-43	3.00	4.00	1.9 × 4.75 × 9.125
LFS-44	3.50	4.50	1.9 × 4.75 × 11.75
LFS-45	6.00	7.00	1.9 × 4.75 × 16
LFS-45A	6.00	7.00	4 × 4 × 9
LFS-46	8.75	11.75	5 × 4.875 × 7.25
LFS-47	9.19	12.19	5 × 4.875 × 8.875
LFS-48	12.31	15.31	5 × 4.875 × 11
LFS-49	16.00	19.00	7.375 × 4.875 × 11.50
LFS-50	18.00	21.00	7.375 × 4.875 × 12.875

FINISH
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ACCESSORIES
LRA-17 and LRA-18 Rack Adapter available. LRA-15 Rack Adapter also available for LFS-38, 39, 40, 41, 42, 43, 45A, 46, 47, and 48 only.

GUARANTEED FOR 3 YEARS
Three year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of three years.

UL / CSA / TUV / IEC
Most units have received formal agency approval or have passed all tests and are waiting for formal notification.

LFS SERIES Switching Power Supplies

	MAX CURRENT AT AMBIENT OF (A) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 10	QTY. 25	QTY. 100	QTY. 250	QTY. 1000	MODEL
2V ±5% ADJ.	3.8	2.6	1.9	1.38 × 3.82 × 3.54	$ 80	$ 76	$ 72	$ 63	$ 55	$ 51	**LFS-38-2**
	6.0	4.2	3.0	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-2**
	12.0	8.4	6.0	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-2**
	18.0	12.6	9.0	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-2**
	25.0	21.8	17.3	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-2**
	40.0	33.5	25.0	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-2**
	60.0	45.0	33.5	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-2**
	90.0	67.5	45.0	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-2**
	90.0	67.5	45.0	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-2**
	120.0	112.0	93.5	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-2**
	150.0	142.5	120.0	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-2**
	200.0	185.0	157.0	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-2**
	335.0	318.0	291.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-2**
	400.0	375.0	350.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-2**
5V ±5% ADJ.	3.8	2.6	1.9	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-5**
	6.0	4.2	3.0	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-5**
	12.0	8.4	6.0	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-5**
	18.0	12.6	9.0	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-5**
	25.0	21.8	17.5	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-5**
	40.0	33.5	25.0	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-5**
	60.0	45.0	33.5	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-5**
	90.0	67.5	45.0	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-5**
	90.0	67.5	45.0	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-5**
	120.0	112.0	93.5	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-5**
	150.0	142.5	120.0	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-5**
	200.0	185.0	157.0	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-5**
	300.0	285.0	261.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-5**
	400.0	375.0	350.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-5**
6V ±5% ADJ.	3.2	2.2	1.6	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-6**
	5.0	3.5	2.5	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-6**
	10.0	7.0	5.0	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-6**
	15.0	10.5	7.5	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-6**
	21.0	18.3	14.5	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-6**
	35.0	28.0	20.5	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-6**
	50.0	37.5	28.0	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-6**
	75.0	56.0	37.5	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-6**
	75.0	56.0	37.5	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-6**
	101.0	94.5	79.0	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-6**
	126.0	120.0	107.0	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-6**
	168.0	155.0	132.0	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-6**
	260.0	244.0	224.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-6**
	345.0	325.0	300.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-6**
12V ±5% ADJ.	1.6	1.1	0.8	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-12**
	2.5	1.75	1.25	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-12**
	5.0	3.5	2.5	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-12**
	7.5	5.2	3.7	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-12**
	10.5	9.5	8.0	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-12**
	19.0	15.0	11.0	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-12**
	26.0	18.5	13.5	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-12**
	40.0	30.0	20.0	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-12**
	40.0	30.0	20.0	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-12**
	51.5	48.0	40.0	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-12**
	64.5	61.5	55.0	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-12**
	86.0	79.5	67.5	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-12**
	145.0	138.0	126.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-12**
	190.0	180.0	170.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-12**
15V ±5% ADJ.	1.3	0.9	0.65	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-15**
	2.0	1.4	1.0	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-15**
	4.0	2.8	2.0	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-15**
	6.0	4.2	3.0	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-15**
	8.5	7.5	6.3	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-15**
	15.5	12.0	9.0	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-15**
	21.0	15.5	11.5	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-15**

NOTE: 15V models continued on next page.

LFS SERIES Switching Power Supplies

	MAX CURRENT AT AMBIENT OF (A) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 10	QTY. 25	QTY. 100	QTY. 250	QTY. 1000	MODEL
15V ±5% ADJ. (cont'd.)	32.5	24.5	16.0	1.9 × 4.75 × 16	$ 527	$ 504	$ 480	$ 392	$ 371	$ 342	**LFS-45-15**
	32.5	24.5	16.0	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-15**
	42.0	39.0	33.0	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-15**
	52.5	50.0	44.5	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-15**
	70.0	64.5	55.0	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-15**
	115.0	108.0	100.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-15**
	153.0	143.0	133.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-15**
20V ±5% ADJ.	0.95	0.65	0.45	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-20**
	1.5	1.05	0.75	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-20**
	3.0	2.1	1.5	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-20**
	4.5	3.1	2.2	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-20**
	6.7	6.1	5.1	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-20**
	11.8	9.2	6.8	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-20**
	16.0	11.5	8.5	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-20**
	25.0	19.0	12.5	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-20**
	25.0	19.0	12.5	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-20**
	32.0	30.0	25.0	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-20**
	40.0	38.0	34.0	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-20**
	53.0	49.0	41.5	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-20**
	85.0	80.0	72.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-20**
	111.0	104.0	97.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-20**
24V ±5% ADJ.	0.8	0.55	0.4	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-24**
	1.3	0.9	0.65	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-24**
	2.5	1.75	1.25	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-24**
	3.8	2.6	1.9	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-24**
	5.7	5.1	4.3	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-24**
	10.0	7.8	5.7	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-24**
	13.0	10.0	7.5	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-24**
	20.0	15.0	10.0	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-24**
	20.0	15.0	10.0	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-24**
	27.0	25.0	21.0	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-24**
	33.5	32.0	28.5	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-24**
	44.5	40.5	35.0	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-24**
	72.0	68.0	63.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-24**
	97.0	90.0	84.0	4.875 × 7.375 × 12.75	1427	1365	1300	1100	940	920	**LFS-50-24**
28V ±5% ADJ.	0.7	0.5	0.35	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-28**
	1.1	0.77	0.55	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-28**
	2.2	1.5	1.1	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-28**
	3.3	2.3	1.6	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-28**
	5.0	4.4	3.7	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-28**
	8.6	6.8	5.0	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-28**
	11.5	8.5	6.3	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-28**
	17.5	13.0	8.5	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-28**
	17.5	13.0	8.5	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-28**
	23.0	21.5	18.0	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-28**
	29.0	27.5	24.5	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-28**
	38.5	35.0	30.0	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-28**
	64.0	61.0	56.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-28**
	86.0	80.0	75.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-28**
48V ±5% ADJ.	0.4	0.28	0.2	1.38 × 3.82 × 3.54	80	76	72	63	55	51	**LFS-38-48**
	0.65	0.45	0.32	1.38 × 3.82 × 4.53	108	103	98	80	70	65	**LFS-39-48**
	1.25	0.87	0.62	1.46 × 3.82 × 6.02	154	147	140	115	99	92	**LFS-40-48**
	1.9	1.3	0.9	1.78 × 3.82 × 6.30	204	195	185	148	130	120	**LFS-41-48**
	2.8	2.6	2.1	1.9 × 4.75 × 5.687	259	247	235	170	155	140	**LFS-42-48**
	5.0	4.0	3.0	1.9 × 4.75 × 9.125	308	294	280	228	207	189	**LFS-43-48**
	6.5	5.0	3.8	1.9 × 4.75 × 11.75	396	378	360	297	270	252	**LFS-44-48**
	10.0	7.5	5.0	1.9 × 4.75 × 16	527	504	480	392	371	342	**LFS-45-48**
	10.0	7.5	5.0	4 × 4 × 9	527	504	480	392	371	342	**LFS-45A-48**
	13.5	12.5	10.5	5 × 4.875 × 7.25	637	609	580	450	428	403	**LFS-46-48**
	17.0	16.0	14.5	5 × 4.875 × 8.875	747	714	680	560	478	450	**LFS-47-48**
	22.5	20.5	17.5	5 × 4.875 × 11	878	840	800	680	600	560	**LFS-48-48**
	37.0	34.0	31.0	4.875 × 7.375 × 11.50	1197	1145	1090	900	780	760	**LFS-49-48**
	48.0	45.0	42.0	4.875 × 7.375 × 12.875	1427	1365	1300	1100	940	920	**LFS-50-48**

LFS SERIES Assembled Cover Option "K"

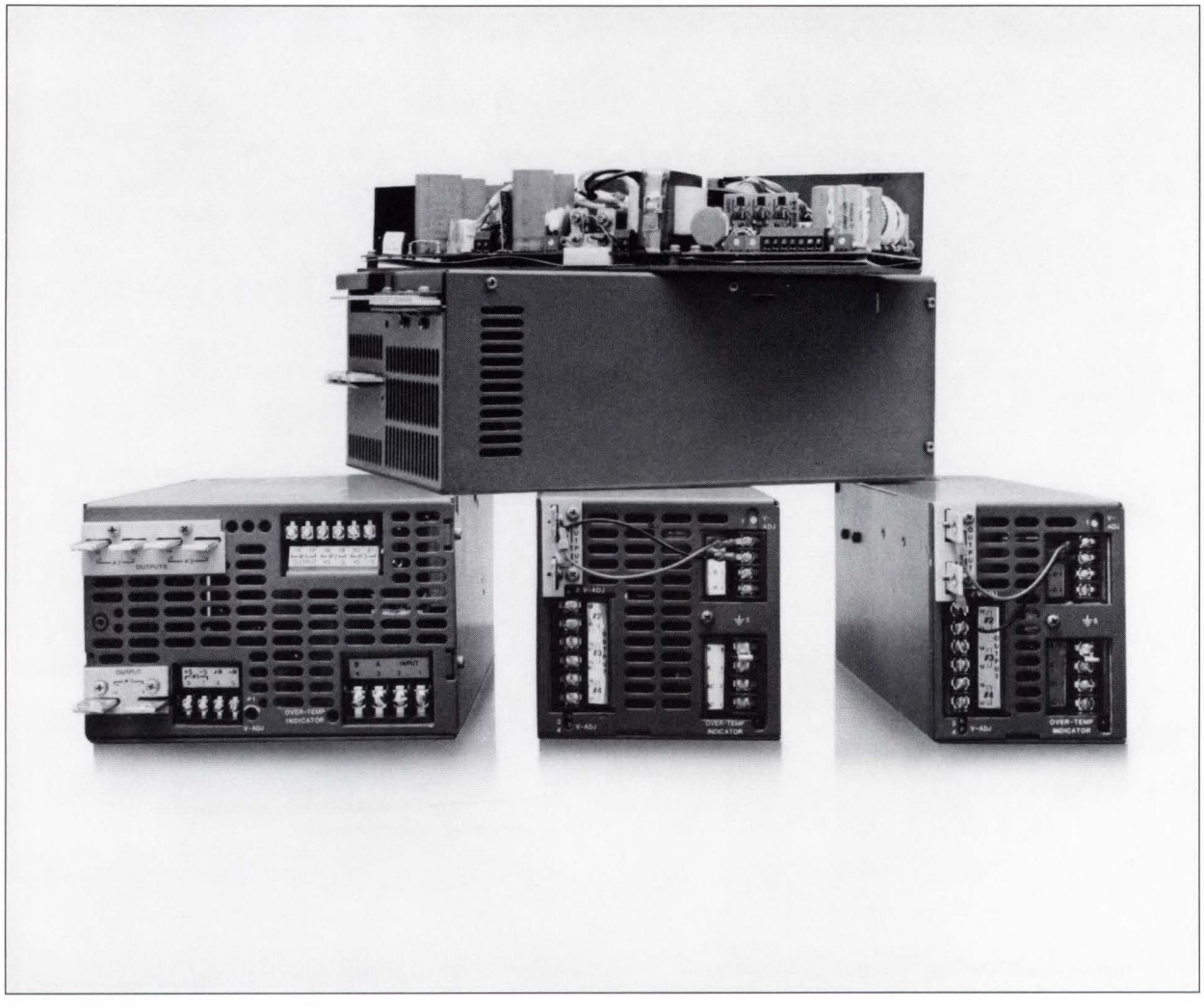
Safety requirements for industrial applications impose a need for enclosed power supplies. Covers provide extra protection that ensures the end user is safeguarded from dangerous voltages. The LFS Series is designed with a cover on all models exceeding 450W. In the power range of 107W to 240W, Lambda can provide an LFS-42, 43, 44 with a protective cover option. As these models are convection cooled, they require derating when covers are used.

	MAX CURRENT AT OPERATING TEMPERATURE OF			PRICE						
	40°C	50°C	60°C	QTY. 1	QTY. 10	QTY. 25	QTY. 100	QTY. 250	QTY. 1000	MODEL
2V ±5% ADJ.	21.3	17.4	13.0	$267	$255	$243	$176	$161	$145	**LFS-42-2K**
	34.0	28.5	21.3	317	303	289	235	213	194	**LFS-43-2K**
	48.0	38.3	20.1	405	387	369	304	277	258	**LFS-44-2K**
5V ±5% ADJ.	21.3	17.4	13.0	267	255	243	176	161	145	**LFS-42-5K**
	34.0	28.5	21.3	317	303	289	235	213	194	**LFS-43-5K**
	48.0	38.3	20.1	405	387	369	304	277	258	**LFS-44-5K**
6V ±5% ADJ.	17.9	14.6	10.9	267	255	243	176	161	145	**LFS-42-6K**
	29.8	23.8	17.4	317	303	289	235	213	194	**LFS-43-6K**
	40.0	31.9	16.8	405	387	369	304	277	258	**LFS-44-6K**
12V ±5% ADJ.	8.9	7.6	6.0	267	255	243	176	161	145	**LFS-42-12K**
	16.2	12.8	9.4	317	303	289	235	213	194	**LFS-43-12K**
	20.8	15.7	8.1	405	387	369	304	277	258	**LFS-44-12K**
15V ±5% ADJ.	7.2	6.0	4.7	267	255	243	176	161	145	**LFS-42-15K**
	13.2	10.2	7.7	317	303	289	235	213	194	**LFS-43-15K**
	16.8	13.2	6.9	405	387	369	304	277	258	**LFS-44-15K**
20V ±5% ADJ.	5.7	4.9	3.8	267	255	243	176	161	145	**LFS-42-20K**
	10.0	7.8	5.8	317	303	289	235	213	194	**LFS-43-20K**
	12.8	9.8	5.1	405	387	369	304	277	258	**LFS-44-20K**
24V ±5% ADJ.	4.8	4.1	3.2	267	255	243	176	161	145	**LFS-42-24K**
	8.5	6.6	4.8	317	303	289	235	213	194	**LFS-43-24K**
	10.4	8.5	4.5	405	387	369	304	277	258	**LFS-44-24K**
28V ±5% ADJ.	4.3	3.5	2.8	267	255	243	176	161	145	**LFS-42-28K**
	7.3	5.8	4.3	317	303	289	235	213	194	**LFS-43-28K**
	9.2	7.2	3.8	405	387	369	304	277	258	**LFS-44-28K**
48V ±5% ADJ.	2.4	2.1	1.6	267	255	243	176	161	145	**LFS-42-48K**
	4.3	3.4	2.6	317	303	289	235	213	194	**LFS-43-48K**
	5.2	4.3	2.3	405	387	369	304	277	258	**LFS-44-48K**

NOTE: For vertical mounting in free air only. Consult factory for other mounting positions and for external fan cooling for increased ratings. Safety ratings are with cover fitted. All prices are with cover fitted by Lambda.

WattBox™ LFQ SERIES:

IMMEDIATE SOLUTIONS FOR QUAD OUTPUT INDUSTRIAL APPLICATIONS. FROM 325W TO 1200W.



Reliability starts with the design. The WattBox LFQ Series embodies a unique control concept, developed by Lambda, which provides inherently reliable operation in transient line and load conditions. In addition, the WattBox allows increased power density up to 2.8W/in^3 for a quad output. This design approach, coupled with the high quality standards you've come to expect from Lambda, makes the WattBox LFQ Series the natural choice in demanding industrial applications.

Now the LFQ family has been expanded to include two new packages: The LFQ-29 @ 920W; and the LFQ-30 @ 1200W. All of the outputs from each LFQ WattBox are floating and regulated. Dynamic performance is guaranteed for each output over the full AC input range and from zero to full load (up to the maximum total power for the individual package). Cross regulation between outputs is controlled within 0.1% with respect to the other.

FEATURES:

- Priced from 63¢/W
- High power up to 1.2kW
- Power density up to 2.8W/in^3
- Meets UL/CSA/TUV/IEC
- Short circuit, overvoltage and fan failure protection
- TTL compatible signal enables remote turn-on/turn-off
- Performance guaranteed for the full range of line and load regulation
- International Input: 85–132VAC/ 170–250VAC/ 47–63Hz/ 250–370VDC
- Industrial Isolation Ratings: 3750V RMS input to output; 1500V RMS input to ground; 500V RMS output to ground.
- Continuous duty from 0 to 60°C. Guaranteed turn-on at −10°C.
- All components and ratings are rigidly specified by Lambda including Class H insulated magnetics, high grade electrolytic capacitors, high quality fans (where used), Lambda PWM controller and CC4 printed circuit boards. All mounted in heavy gauge sheet steel enclosures.
- LRA-18, 19-inch rack mounting accessories and standard assemblies available.

LFQ SERIES

Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line . . . . 0.1% for line variations from 187 to 265VAC and from 95 to 132VAC. On LFQ-29, 30, 0.1% for line variations from 85 to 132VAC and from 170 to 265VAC.

regulation, load . . . 0.1% for load variations from 0 to full load for main output; 0.2% for fourth output (5V) of LFQ-26-1, LFQ-27-1, LFQ-28-1; 1% for 12V/15V outputs*; 2% for 24V/28V outputs*; (*5V outputs require a preload of 12.5A on LFQ-26, 19.0A on LFQ-27, 25.5A on LFQ-28 for full power on other outputs, and 4.0A on output #2 of LFQ-29, 30 for max power out on outputs 3 and 4. Output #2 must be greater than or equal to output #3). 0.2% for second 5V output of LFQ-29-1, 30-1.

ripple and noise . . . 15mV RMS, 100mV pk-pk for 5V outputs. 25mV RMS, 150mV pk-pk for 12V/15V outputs.
25mV RMS, 250mV pk-pk for 24V/28V outputs.

cross regulation . . . 5V outputs: 0.1% max for load variations on auxiliary outputs from no load to full load; Auxiliary outputs: 0.1% max for load variations on 5V output from preload to full load current.

remote programming resistance . . . . . 1000 Ω/V nominal (main output and output 1, 2, 3 on LFQ-29, 29-1, 30, 30-1).

remote programming voltage . . . . . volt per volt.

temperature coefficient . . . . . 0.3%/°C.

AC INPUT (User selectable)

line . . . . . 95 to 132VAC/187-265VAC, 47-440Hz. 85 to 132VAC 170 to 265VAC on LFQ-29, 29-1, 30, 30-1.

power . . . . . LFQ-26, 26-1: 434 watts maximum.
LFQ-27, 27-1: 633 watts maximum.
LFQ-28, 28-1: 880 watts maximum.
LFQ-29, 29-1: 1310 watts maximum.
LFQ-30, 30-1: 1710 watts maximum.

RMS current . . . . . LFQ-26, 26-1: 7.0A RMS maximum.
LFQ-27, 27-1: 11.0A RMS maximum.
LFQ-28, 28-1: 15.0A RMS maximum.
LFQ-29, 29-1: 20.0A RMS maximum.
LFQ-30, 30-1: 26.0A RMS maximum.

EFFICIENCY
75% minimum on LFQ-26, 26-1, 27, 27-1. 72% minimum on LFQ-28, 28-1. 70% minimum on LFQ-29, 29-1, 30, 30-1.

DC INPUT
260 to 370VDC. (Units must be configured for 220V input.) 250-370VDC on LFQ-29, 29-1, 30, 30-1.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

STORAGE TEMPERATURE RANGE
−55°C to +85°C.

AMBIENT OPERATING TEMPERATURE
Continuous duty 0° to 60°C with suitable derating above 40°C. Guaranteed turn-on at −10°C with reduced specifications.

OVERLOAD PROTECTION
ELECTRICAL
External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

HOLD UP TIME
All outputs will remain within regulation limits for at least 16.7 msec after loss of AC power when operating at maximum output power and 105VAC input at 60Hz. (When configured at 220V input: 20 msec holdup when operating at maximum output power and 210VAC input at 50Hz.)

IN-RUSH CURRENT LIMITING
The turn-on in-rush current will not exceed 40 amps peak on LFQ-26, 26-1. (75 amps peak on LFQ-27, 27-1, 28, 28-1, 29, 29-1, 30, 30-1.)

OVERVOLTAGE PROTECTION
Main 5V outputs only. If output voltage exceeds a preset value, inverter drive is removed.

COOLING
The LFQ-26, 26-1 are convection cooled. The LFQ-27, 27-1, 28, 28-1, 29, 29-1, 30, 30-1 are fan cooled. A fan failure circuit will shut down the inverter in the event of fan failure or interference of fan rotation. AC input power must be momentarily interrupted to reduce output after fault condition is corrected.

LED INDICATOR
An LED fan failure indicator will illuminate in the event of fan failure or interference of fan rotation.

DC OUTPUT CONTROLS
Simple screwdriver adjustment over entire voltage range.

INPUT AND OUTPUT CONNECTIONS
PC Board mounted barrier strip: AC input, 5V DC sensing and remote turn-on/turn-off of LFQ-27, 27-1, 28, 28-1; AC input, remote turn-on/turn-off, DC sensing outputs 1, 2, 3 of LFQ-29, 29-1, 30, 30-1. DC output 4 of LFQ-29, 29-1, 30, 30-1; Auxiliary outputs of LFQ-27, 27-1, 28, 28-1.
PC Board mounted terminal block: AC input, 5VDC, sensing and remote turn-on/turn-off and auxiliary outputs of LFQ-26, 26-1.
Chassis stud: all ground connections.
Bus Bars mounted on PC Board: 5VDC outputs of LFQ-26, 26-1, 27, 27-1, 28, 28-1; DC outputs 1, 2, 3 of LFQ-29, 29-1, 30, 30-1.

MOUNTING
Two mounting surfaces and two mounting positions on LFQ-26, 26-1. LFQ-27, 27-1, 28, 28-1, 29, 29-1, 30, 30-1 have one mounting surface. Forced air cooling will allow multiple mounting positions.

REMOTE TURN-ON/TURN-OFF
TTL compatible signal enables remote turn-on/turn-off of the power supply. A voltage of 2.8V to 5.0V applied to remote on/off terminals will initiate turn-off. Open circuit or short circuit condition, or a zero to 0.5V signal will cause turn-on.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation. (Main 5V outputs only of LFQ-26, 26-1, 27, 27-1, 28, 28-1 and outputs 1, 2, 3 of LFQ-29, 29-1, 30, 30-1.)

ISOLATION RATING
3750V RMS input to output, (8mm spacing).

EMI
Conducted EMI conforms to FCC Docket 20780 Class A and VDE 0871 Class A above 150 kHz.

PHYSICAL DATA

Package Model	Weight Lb. Net	Weight Lb. Ship	Size (In.)
LFQ-26, 26-1	6	7	2.5 × 4.75 × 13
LFQ-27, 27-1	12	14	4.0 × 4.875 × 11
LFQ-28, 28-1	13	15	5.0 × 4.875 × 11
LFQ-29, 29-1, 30, 30-1	17	20	7.75 × 4.875 × 11.5

FINISH
Grey, Fed. Std. 595, No. 26081

GUARANTEED FOR 3 YEARS
Three year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of three years.

/CSA/TUV/IEC
All models are approved for UL/CSA/TUV, except for LFQ-29, 29-1, 30, 30-1 which are under evaluation.

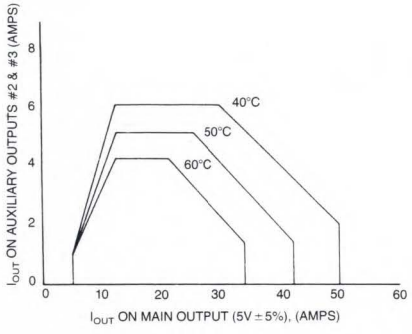
WattBox™ LFQ SERIES

Switching Power Supplies

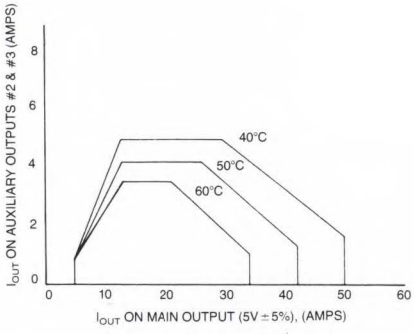
MODEL	OUTPUT NUMBER	ADJUSTABLE VOLTAGE RANGE (VDC)	VOLT NOMINAL (Vo)	MAX OUTPUT POWER (WATTS) 40°C	50°C	60°C	MAX CURRENT (AMPS AT) 40°C	50°C	60°C	DIMENSIONS (INCHES)	PRICE QTY. 1	QTY. 10	QTY. 25	QTY. 250	QTY. 1000
LFQ-26	1	5V ± 5%	5	325	276	227	50.00	42.00	34.00	2.5 × 4.75 × 13	$ 495	$ 473	$ 450	$375	$325
	2	11.4-15.75	12				6.00	5.10	4.20						
			15				4.80	4.10	3.40						
	3	11.4-15.75	12				6.00	5.10	4.20						
			15				4.80	4.10	3.40						
	4	22.8-29.4[1]	24				1.00	0.85	0.70						
			28				0.86	0.73	0.60						
LFQ-26-1	1	5V ± 5%	5	325	276	227	50.00	42.00	34.00	2.5 × 4.75 × 13	495	473	450	375	325
	2	11.4-15.75	12				6.00	5.10	4.20						
			15				4.80	4.10	3.40						
	3	11.4-15.75	12				6.00	5.10	4.20						
			15				4.80	4.10	3.40						
	4	5V ± 5%	5				5.00	4.20	3.50						
LFQ-27	1	5V ± 5%	5	475	420	362	75.00	66.00	57.00	4.0 × 4.875 × 11	626	599	570	485	435
	2	11.4-15.75	12				9.00	7.90	6.90						
			15				7.20	6.40	5.50						
	3	11.4-15.75	12				9.00	7.90	6.90						
			15				7.20	6.40	5.50						
	4	22.8-29.4[1]	24				1.50	1.30	1.10						
			28				1.30	1.15	1.00						
LFQ-27-1	1	5V ± 5%	5	475	420	362	75.00	66.00	57.00	4.0 × 4.875 × 11	626	599	570	485	435
	2	11.4-15.75	12				9.00	7.90	6.90						
			15				7.20	6.40	5.50						
	3	11.4-15.75	12				9.00	7.90	6.90						
			15				7.20	6.40	5.50						
	4	5V ± 5%	5				7.50	6.70	6.00						
LFQ-28	1	5V ± 5%	5	635	578	502	100.00	91.00	79.00	5.0 × 4.875 × 11	741	709	675	575	510
	2	11.4-15.75	12				12.00	10.80	9.50						
			15				9.60	8.60	7.60						
	3	11.4-15.75	12				12.00	10.80	9.50						
			15				9.60	8.60	7.60						
	4	22.8-29.4[1]	24				2.00	1.80	1.60						
			28				1.70	1.50	1.40						
LFQ-28-1	1	5V ± 5%	5	635	578	502	100.00	91.00	79.00	5.0 × 4.875 × 11	741	709	675	575	510
	2	11.4-15.75	12				12.00	10.80	9.50						
			15				9.60	8.60	7.60						
	3	11.4-15.75	12				12.00	10.80	9.50						
			15				9.60	8.60	7.60						
	5	5V ± 5%	5				7.50	6.70	6.00						
LFQ-29	1	5V ± 5%	5	920	830	700	150.00	130.00	105.00	7.75 × 4.875 × 11.5	922	882	840	710	635
	2	11.4-15.75	12				18.00	15.70	12.60						
			15				14.40	12.50	10.00						
	3	11.4-15.75	12				18.00	15.70	12.60						
			15				14.40	12.50	10.00						
	4	22.8-29.4	24				2.70	2.30	1.90						
			28				2.30	1.80	1.60						
LFQ-29-1	1	5V ± 5%	5	920	830	700	150.00	130.00	105.00	7.75 × 4.875 × 11.5	922	882	840	710	635
	2	11.4-15.75	12				18.00	15.70	12.60						
			15				14.40	12.50	10.00						
	3	11.4-15.75	12				18.00	15.70	12.60						
			15				14.40	12.50	10.00						
	4	5V ± 5%	5				10.00	8.70	7.00						
LFQ-30	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	7.75 × 4.875 × 11.5	1098	1050	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00						
			15				16.00	13.90	11.20						
	3	11.4-15.75	12				20.00	17.40	14.00						
			15				16.00	13.90	11.20						
	4	22.8-29.4	24				3.30	2.90	2.30						
			28				2.80	2.40	2.00						
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	7.75 × 4.875 × 11.5	1098	1050	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00						
			15				16.00	13.90	11.20						
	3	11.4-15.75	12				20.00	17.40	14.00						
			15				16.00	13.90	11.20						
	4	5V ± 5%	5				10.00	8.70	7.00						

NOTE: [1] Peak output current (40°C) for 5 sec.: LFQ-27 — 4.5A; LFQ-28 — 6.0A.
[2] All outputs are floating and regulated. They can be configured in either a positive or negative mode.

OUTPUT CURRENT ON AUXILIARY OUTPUTS 2 AND 3 VERSUS I_{OUT} ON MAIN OUTPUT
(Auxiliary output 4 and maximum output current at appropriate ambient temperature.)



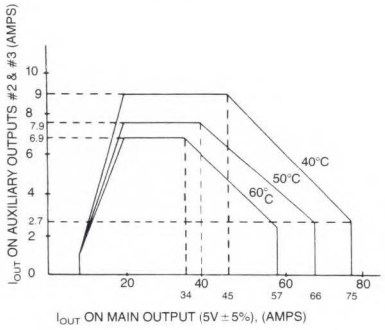
Auxiliary Outputs #2 and #3 Adjusted to 12V ±5%



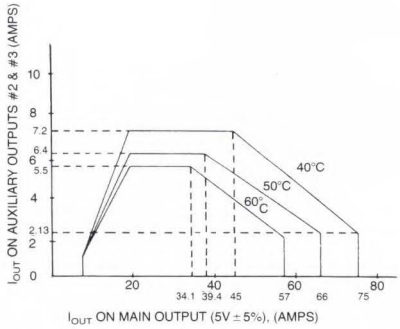
Auxiliary Outputs #2 and #3 Adjusted to 15V ±5%

Figure 1. LFQ-26 Output Current Profile

OUTPUT CURRENT ON AUXILIARY OUTPUTS 2 AND 3 VERSUS I_{OUT} ON MAIN OUTPUT
(Auxiliary output 4 at maximum output current at appropriate ambient temperature.)



Auxiliary Outputs #2 and #3 Adjusted to 12V ±5%



Auxiliary Outputs #2 and #3 Adjusted to 15V ±5%

Figure 2. LFQ-27 Output Current Profile

MINIMUM LOAD REQUIRED

The minimum load specified for the LFQ Series is not required for reasons of cross regulation. Line and load transients happen frequently in industrial applications throughout the world. This imposes the need for a wide variation in duty cycle and precise control under all circumstances, including the effects of power supply load variations. Minimum loading requirements are specified for the LFQ Series (shown for the main 5V output on single inverter designs employed in LFQ-26, 27 and 28, and output number 2 in LFQ-29 and 30 which use a double inverter approach). The minimum loading specified is required to ensure that the minimum duty cycle of the inverter does not fall below the design limit when maximum current is required from the dual auxiliary outputs. In the majority of applications, where the full rated output is not required from the auxiliaries, the minimum loading on the main output can be reduced. Figure 1 (a) and 1 (b) thru 5 (a) and (b) exemplify these options for the LFQ Series.

SOLDERLESS TECHNIQUE BONDS DEVICES TO TRACES PRINTED ON FLEXIBLE FILM

DAVID MALINIAK

A solderless technology has been developed that can cut the cost of printed circuitry by 50%. In Poly-Flex Circuits' Additive Polymer Circuit (APC) technology, conductive-ink traces are printed on low-cost polyester film. Surface-mounted components are then attached to the traces with the company's Poly-Solder, a special conductive epoxy. As a result, stiff copper-epoxy-substrate circuit boards are replaced by ultralight-weight, flexible circuit boards that offer numerous packaging and production advantages.

Single-and double-layer circuits can be produced over a 20-by-20-in. maximum area. The single-layer circuitry is produced by directly printing and curing electrically conductive polymer ink on a 0.005-in.-thick polyester film. Double-layer circuits are achieved when a polymer-based insulation layer is printed over the first conductive layer. This is followed by a second, or top, conductive layer.

Production of copper-epoxy-based pc boards involves about 10 steps, which culminate with the cleaning of flux from the soldered board with fluorocarbons. If not removed completely—as is often the case—the flux can corrode and short-circuit the board in the field. Moreover, fluorocarbons are seen as an environmental hazard.

By eliminating solder, the APC technology deftly sidesteps several production problems. For starters, there is no longer any need to clean boards with fluorocarbons, which gets rid of both the environmental hazard and the added costs. In addition, the over-260°C-heat of soldering processes can cause thermal stresses that result in minute cracks in semiconductors and other devices. These cracks are very difficult to detect and are a major cause of field failure for boards. In contrast, the APC technology's Poly-Solder conductive epoxy is cured at relatively low temperatures (140°C) that do not cause cracking. Also, other soldering problems, such as tombstoning and solder balls, are left behind.

Cost advantages are significant with APC technology compared with copper-etched boards. Because the production process requires only four steps for the film-based substrate compared with 10 for copper-etched boards, the average cost of a two-layer Poly-Flex circuit is $0.05 per square inch. That's a significant advantage over copper-etched costs, which can run from $0.09 to $0.12 per square inch.

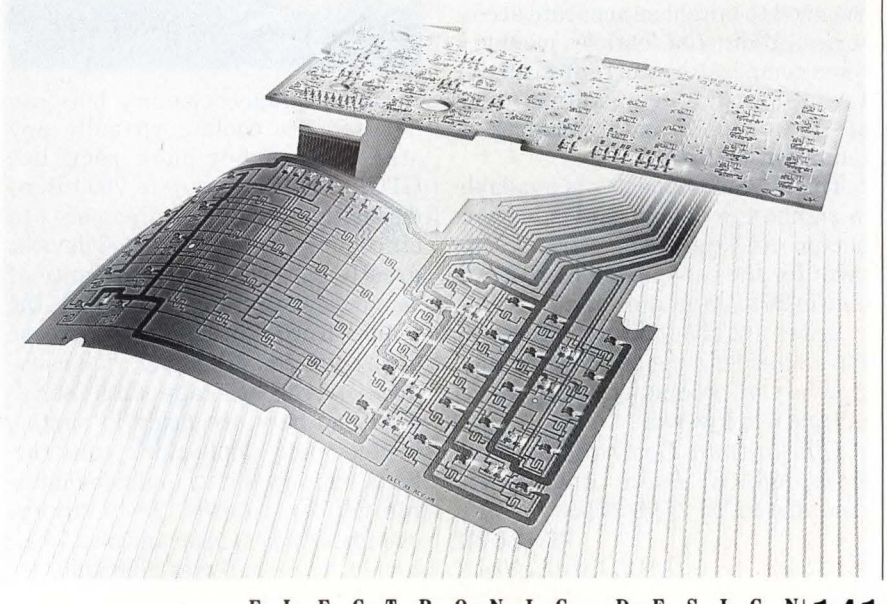
Packaging engineers will find much to like about APC technology. The film-based boards are extremely light and low in profile. They can be wrapped around the inner contours of enclosures without need for interconnections or cables. In addition, the circuits can be laminated directly to housings, which eliminates standoffs, fasteners, and screws. Integral membrane switches can be printed onto the film, realizing further savings and reliability gains.

As of now, Poly-Solder connections permit attachment of LEDs, resistors, inductors, diodes, small-outline ICs, and plastic leaded chip carriers with lead pitches as low as 50 mils. The devices are attached to the printed-circuit traces using high-speed pick-and-place equipment. Unlike solder paste, which can cause components to slide out of place on the board as it liquefies, the Poly-Solder material securely fastens the devices.

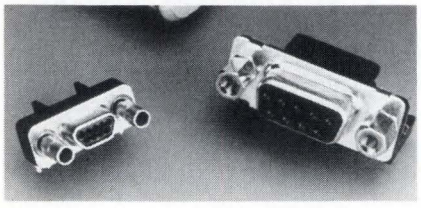
The technology is not without its limitations. Single- and double-layer circuits are now being produced, although four-layer circuits may be within grasp. At present, the company feels most comfortable restricting itself to 20-mil traces on 20-mil spacing, although 15-mil and even 10-mil dimensions are not far out of reach.

Production-tooling costs run from $300 to $1500 for steel-rule die for perimeter cutting, $500 to $2000 for artwork design and generation, and $500 to $1500 for test fixtures. Production lead times are about 8 weeks. Prototypes can be turned around in about 4 weeks for a cost of $1500 to $2500. On average, single-layer Poly-Flex circuits cost about $0.02 per square inch.

Poly-Flex Circuits Inc., 30 Kenney Dr., Cranston, R.I. 02920; (401) 463-3180. **CIRCLE 339**



D-TYPE CONNECTOR IS SMALLEST WIRE-TO-BOARD I/O INTERCONNECTION



The industry's smallest D-type I/O wire-to-board connector is ITT Cannon's Micro-D MDSM series connector. The low-cost, high-density interconnection is set on 0.050 in. between centerlines and 0.043 in. between rows. It is less than one-third the size of other I/O wire-to-board connectors now available. The connector is the first member of a new Micro D family from ITT Cannon.

The space-saving design minimizes the space needed for interconnection devices. This makes the connector suitable for applications in information systems, medical electronics, and test equipment where space constraints are critical.

Features include snap-in crimp contacts and a shielding system that incorporates an integral shield can into the backshell. The insulator is snapped into the backshell and a plastic hood completes the assembly. The simple assembly makes possible significant labor savings. In addition, overmolding is eliminated, as is the need to purchase separate accessories. Additional features include a room-temperature current rating of 1 A, an operating-temperature range of –55 to +125°C, and a shielding attenuation of 70 dB.

The MDSM connector is available in right-angle-mount and cable-connector configurations. Crimp contacts for the cable version are available in 26 to 28 gauge wire.

Prices are about $6 per mated pair for a shielded nine-position version. Delivery of production quantities is in from 6 to 8 weeks.

ITT Cannon Components Division, 1851 E. Deere Ave., Santa Ana, CA 92705; (714) 261-5300.

CIRCLE 312

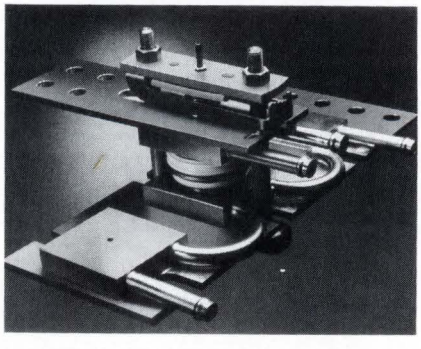
DAVID MALINIAK

THERMAL PROCESSOR AIDS GaAs PRODUCTION

Designed specifically for production gallium-arsenide applications, the Heatpulse 4100 III-V rapid thermal processor (RTP) employs a proprietary GaAs susceptor that keeps arsenic from escaping, supports the wafer to reduce cracking, allows uniform heating and controlled cool down, and provides slip-free rapid thermal processing. An all-quartz processing chamber eliminates metallic ion contamination and, because it can be cleaned using conventional methods, reduces downtime as well. The system can handle up to six different gases (O_2, NH_3, N_2, Ar/H_2, HC_1, and Ar), the flow rates of which are programmable. Software is available for linking the 4100 III-V to an IBM PC or compatible computer.

AG Associates, 1325 Borregas Ave., Sunnyvale, CA 94089; (408) 745-1790. **CIRCLE 313**

SEMICONDUCTOR BUS BARS ARE WATER-COOLED



A line of liquid-cooled bus bars can be used for cooling virtually any standard hockey-puck rectifier, GTO, or SCR with up to 2000 W of dissipation per device. Compared to air cooling, the water-cooled devices greatly improve the performance of semiconductors by decreasing the temperature rise. They also increase device life and MTBF, as well as reduce overall package size. Series 4700 bus bars are made in single-, double-, and triple-block constructions and use 3/8-in. outside-diameter copper tubing. They accept clamps with post spacings on 2.75- or 3.50-in. centers. Series 4750 units are available in single- and double-sided styles and use 1/2-in. copper tubing. They accept clamps with a post spacing of 4.00-in. on centers.

Aavid Engineering Inc., One Kool Path, P.O. Box 400, Laconia, NH 03247; (603) 528-3400. **CIRCLE 314**

CARRIER SOCKET HAS RIGID INSULATOR

The Pull-Off Carrier Socket, a carrier-socket assembly with a rigid insulator, provides many benefits over assemblies with flexible carriers. Not only does the insulator protect the assembly during transport, but it also maintains pin-to-pin location and perpendicular alignment to the mounting surface of the pc board. Exact alignment guarantees proper insertion and withdrawal of components and prevents device breakage. The rigid insulator pulls off easily after the carrier-socket assembly is soldered on the pc board, allowing the socket to be installed automatically. Because the insulator is removed and discarded, air can flow freely around the socket pins.

Andon Electronics Corp., 4 Court Dr., Lincoln, RI 02865; (401) 333-0388. **CIRCLE 315**

ETCH SYSTEMS HANDLE SUBMICRON PROCESSING

The K series of dry etch systems provides submicron processing of wafers up to 200 mm in size. Three models in the series specifically address the stringent requirements of 4-Mbit dynamic RAM fabrication. Machines are classified according to process application. The VE 4000 is used for gate and isolation materials; the VE 5000 is for contact holes, lightly doped drain sidewalls, and etchback processes; and the VE 6000 handles metal interconnections. All models deliver an anisotropic profile and high selectivities in the submicron feature size. Pricing is in the $750,000 range. Delivery takes six months.

Varian Associates Inc., Semiconductor Equipment Group, 611 Hansen Way, Palo Alto, CA 94303; (415) 424-5781. **CIRCLE 316**

INTEGRATED FEATURES TURN MICROPROCESSOR INTO NETWORK CONTROLLER

By combining many of the peripheral functions needed to control network communications, Hitachi's HD64180S 8-bit CMOS microprocessor drastically reduces system complexity. Besides its powerful multiprotocol communications controller, the processor packs a second serial port, two channels of direct-memory-access control, a memory-management unit capable of addressing 1 Mbyte of storage, and an enhanced Z80 processor core. Other resources include a dynamic-RAM refresh controller, a wait-state generator, two 8-bit counter-timers, and multiple chip-select outputs.

The processor's primary serial port can operate with bit- or byte-synchronous protocols (HDLC/SDLC) at rates of up to 7.1 Mbits/s. Not only that, the multi-featured serial port can function asynchronously at rates of up to 4 Mbits/s—all when the processor operates from a 10-MHz clock. The second serial port operates only in an asynchronous mode at rates of up to 4 Mbits/s. Digital phase-locked loops on the chip quickly and accurately lock it onto incoming data streams and deliver stable serial-output streams to other systems.

The shortest instructions on the 64180S require just 300 ns, which is one of the shortest instruction-cycle times for a commercial 8-bit microprocessor. The on-chip direct-memory-access controllers include packet-buffer management to ease the control and manipulation of data packets.

The 10-MHz HD64180S network-processing unit comes in an 84-lead plastic leaded chip carrier and sells for $25.90 in quantities of 100. Six- and 8-MHz versions are also available. Delivery of production quantities is from stock.

Hitachi America Ltd., 2000 Sierra Point Pkwy., Brisbane, CA 94005; Scott McClung, (415) 244-7159.

CIRCLE 340

DAVE BURSKY

PROPAGATION DELAYS DECREASE TO YIELD FASTEST GaAs PLD YET

By taking advantage of gallium arsenide's higher operating frequencies, Gazelle Microcircuits has produced the fastest version of the 22V10 programmable logic device to date. The GA22V10-5 chip boasts a 5.5-ns propagation delay, which permits its operation from an externally supplied 125-MHz clock source or an internal clock rate of 250 MHz.

The short delays make the GA22V10-5 one of the few chips that can keep up with systems based on advanced complex-instruction-set-computer (CISC) and reduced-instruction-set-computer (RISC) CPUs. In addition, its 3-ns setup time and 5-ns clock-to-output time mean that it can implement faster logic blocks than are possible with discrete logic circuits. To minimize ground bounce, the circuit includes the company's unique One-Up control circuits that slow the rising and falling edge rates while maintaining high internal speeds. Edge rates are controlled to within 1 to 1.5 V/ns.

Like Gazelle's earlier chips, the GA22V10-5 has TTL-compatible inputs and outputs that run from a 5-V power supply and is factory programmed with a laser to configure the logic. Turnaround times are typically three to five days after submitting the desired Jedec file. There are no nonrecurring-engineering or setup charges, and the minimum order is one piece. In quantities of 100, the circuit costs $36 and comes housed in a 22-pin, 300-mil DIP.

Gazelle Microcircuits Inc., 2300 Owen St., Santa Clara, CA 95054; Bob Gunn, (408) 982-0900.

CIRCLE 341

DAVE BURSKY

BIPOLAR PLDS CUT PROPAGATION DELAYS

With a maximum propagation delay of just 5 ns, a programmable logic chip takes the speed crown for TTL-compatible PLDs. Optimized for address decoding operations, the PHD16N8-5 can tackle some of the most critical delay paths in high-speed system design. Housed in a 20-pin DIP or PLCC, the 16N8 has 10 dedicated inputs, two dedicated outputs, and six programmable, bidirectional I/O lines. The 16N8 has a typical power consumption of less than 600 mW. Each output can drive loads of up to 24 mA. Individual three-state control of each output can also be programmed in. A security fuse prevents fuse-map readout. In quantities of 1000, the PHD16N8-5 sells for $7.50 and is available from stock.

Philips, Signetics Div., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; (408) 991-2000. **CIRCLE 350**

SCSI Controller For Embedded Drives Handles Sync, Asynch Transfers

The first SCSI disk-controller chip designed specifically to be embedded into 3.5- or 5.25-in. disk drives delivers data at rates of 5 Mbytes/s for synchronous, or 3 Mbytes/s for asynchronous, streams. Available from Cirrus Logic, the CL-SH350 is an enhanced but pin-compatible version of the company's earlier asynchronous-only SH250 SCSI controller.

Also integrated on the CMOS chip are 48-mA SCSI-bus drivers and control signals for off-chip differential drivers. The on-chip single-ended drivers further reduce system chip count, which is critical for space-limited applications such as in 3.5-in Winchester disk drives.

Separate host- and disk-interrupt structures permit firmware designs with either interrupt handlers or polled loops, making it easier to design for time-critical response requirements. Also included on the chip is a programmable sector formatter that employs a split data field processing scheme. The scheme maximizes disk space by skipping only the defects in a sector, not the entire sector. In addition, a zoned formatting approach packs more bits into the outer tracks.

Internal error-correction circuits provide either 16-bit cyclic-redundancy checking or 32/56-bit error-checking codes with hardware assistance to speed corrections. The chip's buffer manager coordinates concurrent memory transfers at up to 12 Mbytes/s and supports through-parity verification from the SCSI bus to the formatter and memory. Either static or dynamic RAMs can be used with the controller to form the buffer.

The CL-SH350 comes in a plastic, 100-lead quad-sided flat package and costs $42 in sample quantities, which are available now.

Cirrus Logic Inc., 1463 Centre Point Dr., Milpitas, CA 95035; George Alexy, (408) 945-8300.

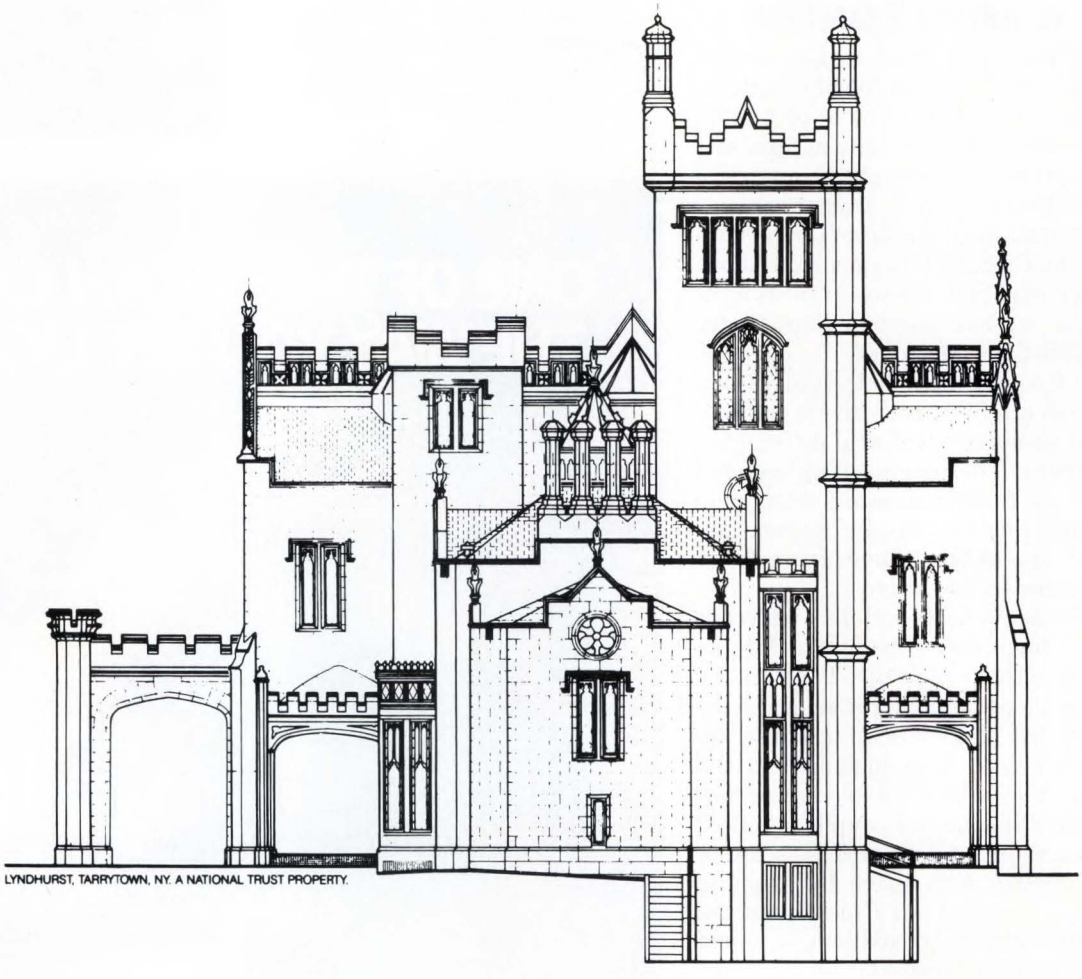
CIRCLE 342

DAVE BURSKY

Get More From ELs

A self-adjusting DC-AC inverter that matches performance to EL lamp capacitance changes, to extend lamplife and optimize brightness. (For more information, see Loctite ad, below.)

PRESERVATION PLAN ON IT



LYNDHURST, TARRYTOWN, NY. A NATIONAL TRUST PROPERTY.

Planning on restoring a house, saving a landmark, reviving your neighborhood?

No matter what your plans, gain a wealth of experience and help preserve our historic and architectural heritage. Join the National Trust for Historic Preservation and support preservation efforts in your community.

Make preservation a blueprint for the future.

Write:

National Trust for Historic Preservation
Department PA
1785 Massachusetts Ave., N.W.
Washington, D.C. 20036

ADVANCED GRAPHICS CONTROLLER, VGA CHIP DELIVER SYSTEM SOLUTIONS

Two graphics circuits, one delivering high-resolution graphics for systems with resolution up to 1280-by-1024 pixels, and the other providing enhanced VGA capabilities, have emerged from Hitachi. The premier device is the HD64400, a graphics data processor that manipulates four hardware windows and stores fill patterns and line styles on the chip.

The HD64400 chip has hardwired instructions modeled after the computer graphics interface standard, a direct interface to video RAMs, and smooth scrolling capability with independent horizontal and vertical control. Drawing speeds are 25 ns/pixel for lines and fills, 37.5 ns/pixel for text, and 75 ns/pixel for bit-block transfers.

The second new graphics chip, the CRTC+ or HD64460, implements IBM Corp.'s Video Graphics Adapter and adds some enhanced-display modes. The circuit is backwards compatible with EGA, CGA, and MDA operating modes. For EGA, however, it is not compatible at the hardware-register level. A unique Smart-Access RAM interface makes possible drawing speeds four times higher than IBM's VGA.

In quantities of 1000, the 16-MHz HD64400 graphics processor costs $250 and comes in a 135-lead ceramic pin-grid-array package. The HD64460 VGA controller sells for $39.90 in similar quantities and comes in a 136-lead quad-sided plastic flat package.

Hitachi America Ltd., 2000 Sierra Point Pkwy., Brisbane, CA 94005; John Hull, (415) 589-8300.

CIRCLE 343

DAVE BURSKY

1-MBIT STATIC RAMS ACCESS IN 35 NS

One of the first manufacturers to offer high-density static RAMs in a medium-speed range, Sony Corp. is introducing 1-Mbit devices with access times ranging from 120 ns all the way down to 35 ns. The parts are organized as 128k by 8 bits. Packaging options include 32-pin (600-mil) DIPs and plastic surface-mount packages. The 100-unit DIP price of the Model CXK581000 in 100- and 120-ns versions is $200 and $166.70, respectively. Pricing for the Model CXK581001 (70 and 85 ns) and CXK581020 (35, 45, and 55 ns) is not yet available.

Sony Corp. of America, Component Products Co., 10833 Valley View St., Cypress, CA 90630; (714) 229-4190.

CIRCLE 352

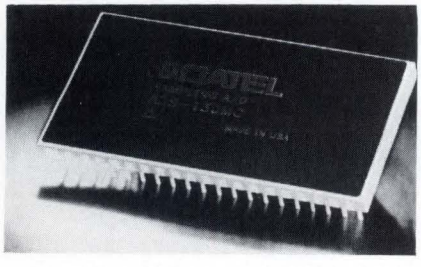
12-Bit Sampling A-D Converter Features 10-MHz Throughput

Superior dynamic performance at low cost is the hallmark of Datel's ADS-130 sampling analog-to-digital converter. The 12-bit device features a minimum throughput of 10 MHz, harmonic distortion of –69 dB, and a signal-to-noise ratio of –70 dB. Applications for the functionally complete converter include spectrum analysis, imaging, radar, high-speed data-acquisition systems, and medical instrumentation.

Power dissipation for digitizing sinusoidal signals is 4.3 W. Analog inputs are ±1.25 V with a ±1-LSB linearity at Nyquist input frequencies.

The ADS-130 contains a sample-and-hold amplifier with 225-V/μs slew rate. Three-state outputs are provided and coding can be selected by the user to be offset binary or complementary offset binary through use of a CBIN pin.

The converter's specified throughput rate is guaranteed over the temperature range when the Start Con-



vert pulse of 10 ns minimum is delivered at the specified rate. The acquisition time for pulse or dc-level signals is 50 ns maximum.

Power-supply requirements for the converter are ±15 V and ±5 V. The device comes in a 40-pin triple-width DIP and is available in commercial (zero to +70°C) and military (–55 to +125°C) temperature ranges. The commercial ADS-130MC goes for $775 in small quantities, while the military ADS-130MM costs $896 in similar quantities. Delivery is in from 2 to 6 weeks.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000. **CIRCLE 344**

DAVID MALINIAK

Analog Comparators Blaze New Trails To Speed, Low Power, And Accuracy

Always overshadowed by their op-amp kin, those 1-bit a-d converters called analog comparators keep improving, too. Not only are they getting faster, as illustrated by Analog Devices' new AD9696 (single) and AD9698 (dual) comparators, but the AD790 gives users more speed at lower power, and with more accuracy and versatility.

The 5-V-logic-compatible AD790, aimed at general-purpose applications, has a maximum propagation delay of just 50 ns with 5 mV of overdrive. Moreover, that's powered from one 5-V rail, or ±15 V. Not only that, it needs just 60 mW of power from the 5-V supply. Two performance grades provide offset voltages of 250 μV or 1 mV. A built-in 500 mV of hysteresis stops oscillations when handling slow or low-level signals.

If the 790 isn't fast enough, try the AD9696, which is also TTL-compatible. If two devices are required, perhaps for a window comparator, the dual AD9698 fills the bill. Their propagation delay, measured with a 100-mV input pulse and 10 mV of overdrive, is a mere 6 ns maximum. Until now, only ECL comparators were so fast. Propagation-delay dispersion (variation) with the input overdriven from 10 mV to 1 V is 200 ps maximum. This specification is vital for fast ATE.

In quantities of 100, the AD790 ranges from $2.50 to $7.95. In similar quantities, the AD9696 and AD9698 start at $3.50 and $6 each, respectively. The AD9696 comes in 10-pin TO-100 metal cans, 8-pin ceramic DIPs, and 8-pin plastic SOICs. The 9698 comes in 16-pin plastic and ceramic DIPs and a 16-pin SOIC.

For the AD790: Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; Dave Kress, (508) 658-9400. **CIRCLE 345**

For the AD9696/9696: Analog Devices Inc., 7910 Triad Dr., Greensboro, NC 27409; Walt Kesta, (919) 668-9511. **CIRCLE 351**

FRANK GOODENOUGH

Trim Circuits With 8-Bit IC Voltage DACs Cost Less Than 12 Cents A Bit

Are the ubiquitous trimpots a dying breed? Certainly PMI, a division of Bourns (one of the leaders in the trimpot industry), is trying to kill them with its DAC-8800 TrimDAC. Just one die in a 20-pin DIP holds eight, 8-bit voltage-output digital-to-analog converters. With them, users can let a host processor set the reference voltage for comparators, calibrate an instrument, zero the offset voltage of virtually any circuit, or set system gain with an analog multiplier. An EPROM or EEPROM stands in for the pot's mechanical memory. The chip fits into a 20-pin package because digital words are fed to it over a standard three-wire serial interface.

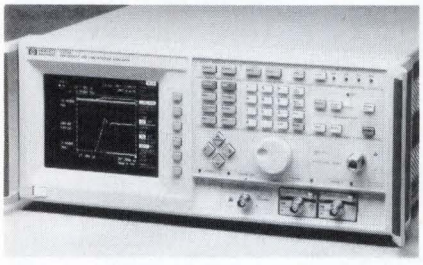
The eight converters are divided into two sets of four, each of which can be given separate output-voltage ranges, either unipolar or bipolar, by means of their reference inputs. Unlike most converters, which have one reference input, this chip provides two sets of reference inputs for each of the four d-a converters. The two inputs set the high and low values of the converters' output voltage. The high reference inputs must be kept at least 4 V below the positive rail. The low input can reach to the negative rail. As for its power, the DAC-8800 operates off any mix of single or split supplies from +17 V and zero to +5 and –12.

Basic specifications for all the d-a converters include a maximum total unadjusted error (includes integral linearity, full scale, and zero error) of ±1/2 LSB and a maximum differential-linearity error of ±1 LSB. Maximum power dissipation is just 25 mW. The DAC-8800 is available in 20-pin plastic and ceramic DIPs and plastic SOICs and in extended-industrial and military-temperature-range models. In quantities of 100, prices range from $9 to $30. Small quantities are in stock.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, CA 95010; (408) 562-7254. **CIRCLE 346**

FRANK GOODENOUGH

ANALYZER CHARACTERIZES SIGNALS TO 2 GHz IN THE MODULATION DOMAIN



Designers working on applications up to 2 GHz can characterize frequency, phase, or time information automatically with the HP 5371A frequency and time-interval analyzer. The analyzer can eliminate the need for additional instrumentation or off-line processing.

Using a technique that Hewlett-Packard Co. calls modulation-domain analysis, the instrument displays phase, continuous-frequency, or time-interval values as a function of time. In addition to numeric results, displays include time profiles, histograms, and event-timing graphs.

The new model features hardware data reduction to sort time-inteval measurements into histograms at a rate of 13.3 million measurements per second. An enlarged memory lets users make up to 8191 measurements in one pass. With the optional FastPort interface, raw event and time data go directly to an external memory.

To reduce the effects of trigger noise, the user can vary input hysteresis by adjusting the HP 5372A's sensitivity. This allows better measurements on noisy signals like those found in radar systems and low-frequency applications.

The HP 5372A costs $28,000, including one-half day of application consulting. Delivery is estimated at 4 weeks after receipt of order. The 2-GHz channel C option goes for $2000, and the FastPort interface costs $1500.

Hewlett-Packard Co., 5301 Stevens Creek Blvd., P.O. Box 58059, Santa Clara, CA 95052; (408) 246-4300. **CIRCLE 347**

JOHN NOVELLINO

TESTER TARGETS POWER ICS WITH RATINGS OF UP TO 2000 V AND 100 A

Aimed at the fast-growing field of power semiconductors with integrated analog and digital control, the Teradyne A510 Smart Power Test System offers wide voltage and current ranges and precise timing control. The modular A510-SP incorporates the advanced features of the A500 series testers, plus a high-speed digital subsystem and a Smart Power Subsystem that users can customize with seven options.

The tester can deliver up to 2000 V and 100 A in a design that emphasizes operator safety as well as instrument protection. Features included are Teradyne's graphics-based programming environment (Image), dual Sun computers, and full tester simulation on stand-alone workstations. The digital subsystem provides 5-MHz, 56-pin capability.

The power modules address specific needs. The high-power V/I unit offers floating 680-V and 10-A capability to accommodate line-voltage devices at all international standard voltages. The high-current voltage source generates 100 V and 100 A, and the high-current current source supplies a floating 100-A source and 40-A load, both for automotive power ICs. For leakage and breakdown testing, the high-voltage V/I module delivers 2000 V at 50 mA.

Multiple-output devices can be tested with the high-power matrix, which provides up to 48 10-A, 2000-V pins that can be connected in parallel. A floating high-voltage ammeter has ranges from 1 μA to 100 mA for high-voltage leakage measurements. Finally, the floating voltage source acts as a floating bias supply for high-side MOS gate drives that can accommodate up to 5-V/ns device transients.

The A510-SP costs from $400,000 to $800,000, depending on configuration. Deliveries will start in the first quarter of 1990.

Teradyne Inc., 321 Harrison Ave., Boston, MA 02118; (617) 482-2700. **CIRCLE 348**

JOHN NOVELLINO

MULTIPLE WAVEFORMS AND MODULATIONS ENHANCE FUNCTION GENERATOR

With the ability to create eight waveform types and seven modulation modes, the PM 5138 10-MHz function generator offers exceptional flexibility at a relatively low cost. An optional IEEE-488 interface adds arbitrary waveform-generation (AWG) capability.

The instrument's outputs include sine, square, triangular, and positive and negative sawtooth waveforms and positive and negative pulses. The outputs can be modulated with AM, FM, PSK, burst, gating, and linear or logarithmic sweep modes. The operator can vary duty cycles in 1% steps from 1% to 99% to 20 kHz and between 20% and 80% up to 5 MHz.

Frequency stability is 0.2 ppm/°C, and accuracy is $\pm$2 ppm. The five-digit readout delivers a maximum resolution of 0.1 mHz on the lowest frequency range. The AWG option features a 20-Mpoint/s sampling rate and 1024-point horizontal and vertical resolutions.

For easy operation, the PM 5138 has a large backlit multifunction LCD and pushbutton parameter selection. The operator sets frequency, ac voltage, dc offset, and other numerical parameters by pushing the appropriate button and turning the one knob until the correct value appears on the display.

List price of the PM 5138 function generator is $3590; delivery is in 4 to 6 weeks. With the IEEE-488 interface, the unit sells for $3990.

John Fluke Mfg. Co., P.O. Box C9090, Everett, WA 98206; (800) 443-5853, ext. 77. In Europe, contact Philips Test and Measurement, Bldg. HKF, 5600 MD, Eindhoven, The Netherlands. **CIRCLE 349**

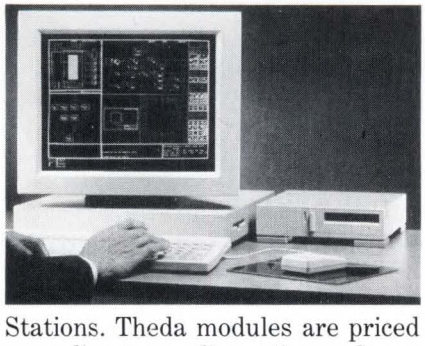
JOHN NOVELLINO

CAE Software Carries Users From Design To Manufacturing

Tightly-integrated modules make up a software family for the design, analysis, and manufacturing of electronic and electromechanical components and assemblies. The Theda family from Prime Computer Inc. performs circuit design, digital and analog simulation, logic design, pc-board design, production documentation, manufacturing, and electromechanical design and packaging.

Included in the Theda software are seven new modules and enhancements to five existing modules. The high-speed logic workbench, which aids in design of fast circuits, allows signals and parameters to be specified in the schematic creation so that the pc board will be automatically verified against design rules during layout. An electronic database extractor converts pc-board design data into ASCII form for use with manufacturing machinery. Other new modules include a mixed-mode simulator, an electronics-library manager, and an EDIF interface.

The Theda family, which is available now, runs on all Prime CADD-



Stations. Theda modules are priced according to configuration and use, and are available for license. Prices for the high-speed logic workbench, the electronic database extractor, the EDIF netlist and schematic interfaces, mixed-mode simulator, and the electronics-library manager are $12,000, $5500, $5000, $5000 and $2500, respectively.

Prime Computer Inc., Prime Park, Natick, MA 01760; (508) 655-8000. **CIRCLE 317**

LISA GUNN

Customized Megacells Create A Complete Digital System On One ASIC

Designers can create a system on a chip with a new library of configurable megacells from Gould Inc. The megacells consist of several thousand logic gates that perform board-level functions. These logic cells combine to form a complete board-level system on one ASIC.

The first available megacell is the MG82C54 programmable-interval timer, which is compatible with the industry-standard 8254 timer. Two other megacells, the MG82C59 interrupt controller and the MG80C85 8-bit microprocessor, are slated for introduction by the end of this year.

The 20-MHz MG82C54 timer has three independently programmable 16-bit timers and six programmable counter modes. Counting can be performed in both binary and binary-coded-decimal formats. Because of this flexibility, the timer can implement a host of functions for high-speed microprocessor systems, including event counters, elapsed-time indicators, and waveform generators.

Gould's megacells can be extensively customized. For instance, one customer recently extended the timer's counters from 16 to 24 bits, and placed four of these modified cells on one ASIC.

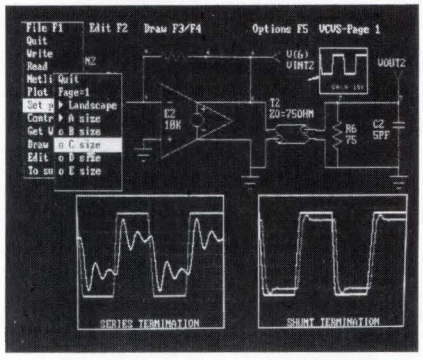
A big advantage of the Gould configurable megacells is that they are independent of process technology. The timer cell, for instance, can be built with CMOS processes ranging from 2 μm to 1.25 μm. In addition, the cells can be implemented in either standard-cell or gate-array circuits to meet users' cost and turnaround requirements.

The MG82C54 interval-timer megacell is available now. A typical standard cell device consisting of an MG82C54 megacell and about 3000 logic gates costs $4.75 per unit.

Gould Inc., Semiconductor Division, 2300 Buckskin Rd., Pocatello, ID 83201; Cathy Payne, (208) 234-6798. **CIRCLE 318**

LISA GUNN

Schematic Program Works With Spice



An interactive schematic-entry program for the Spice analog-circuit simulator allows designers to use PCs to graphically draw and edit electrical circuit designs. SpiceNet version 2.0 produces a complete Spice net list compatible with most popular Spice simulation programs running on PCs, workstations, or mainframes. It also displays post-processor waveforms and node voltages directly on the schematic design. Additionally, it provides automatic creation of subcircuit net lists, automatic pin placement on subcircuit symbols, and placement of any Spice primitive with a single keystroke. The program sells for $295.

Intusoft, P.O. Box 6607, San Pedro, CA 90734; (213) 833-0710. **CIRCLE 319**

PCB Software Has 0.01-Mil Resolution

Upgraded to support complex board layouts, such as those containing metric parts, blind and buried vias, and surface-mounted devices on both sides of the board, the Prance GT design automation system now also provides a data resolution of 0.01 mil. Moreover, two new routing techniques — SX router technology and Warp Grid — work together to provide 100% automatic completion rates of 200 to 370 EIC (equivalent 16-pin ICs) on large, dense, ECL, TTL, and CMOS designs. Prance GT Release 2.0 is available for the VAXstation 3500 and DECstation 3100.

Automated Systems Inc., 4105 Sorrento Valley Blvd., San Diego, CA 92121; (619) 546-0024. **CIRCLE 320**

MINIATURE YIG-TUNED OSCILLATORS COVER FROM 3 TO 6 AND 2 TO 8 GHZ

For approximately half the cost of conventional yttrium-iron-garnet (YIG) tuned oscillators, a pair of devices from Avantek covers the spectrum from 3 to 6 and 2 to 8 GHz. The miniature oscillators weigh just 1.8 ozs. with dimensions of 1 in. in diameter and 0.72 in. high (not including pins and connector). Model AV-7036 covers from 3 to 6 GHz, while model AV-7028 covers from 2 to 8 GHz.

Performance features include +13-dBm minimum output power, ±0.1% (2 to 8 GHz) and ±0.02% (3 to 6 GHz) tuning linearity and single-sideband phase noise of −100 dBc/Hz at 20 kHz from the carrier. The low-

inductance (15 mH) tuning coils offer tuning speeds twice as fast as conventional cylindrical YIG-tuned oscillators. As with all Avantek YIG-tuned oscillators, the low-cost units are equipped with a low-inductance, high-tuning-rate secondary coil for frequency modulation or phase locking.

The oscillators are a likely candidate for commercial applications. These may include bench or portable test instruments such as swept and synthesized signal generators and spectrum analyzers. Other applications may be found in specialized receiving systems.

The AV-7036 and AV-7028 YIG-tuned oscillators cost $385 in quantities of 1000 and $654 in single quantities, and are available from stocking distributors. Complete technical information, including a full data sheet, is available from Avantek's distributors.

Avantek Inc., 461 Cottonwood Dr., Milpitas, CA 95035; Rich Leier, (408) 943-4572. **CIRCLE 321**

DAVID MALINIAK

MINI ATTENUATORS COME IN 1-DB STEPS

To meet industry demand, subminiature attenuators with SMA connectors are now available in 1-dB steps, from 0 to 10 dB. At each dB level, users can select attenuators for frequencies of up to 18 GHz, 12.4 GHz, and 3 GHz. The Series 6600 meets the environmental requirements of MIL-A-3933 D/25 standards and can withstand continuous power of 2 W. Devices with attenuation values of 20 and 30 dB are also available.

Huber & Suhner AG, RF & Microwave Division, CH-9100 Herisau, Switzerland; 071 53 41 11. Telex: 882729. **CIRCLE 322**

MINIATURE CASE PACKS FULL-SIZE DIGITS

Featuring a full-size 14.2-mm light-emitting-diode display in a 24- by 72-mm package, the 205-P digital process meter requires just 37.5% of the panel space that is needed for a conventional 1/8-DIN-sized meter. The device can operate from either an ac or dc supply. Zero and span adjustments of 2000 counts are easily

achieved from the front of the panel through potentiometers (behind the lens). Full-scale signal ranges of 4 to 20 mA, 0 to 199.9 mV, 1 to 5 V, 0 to 10 V, and 0 to 100 V can be read with the meter's 3-1/2 digits and are also jumper selectable.

Newport Electronics Inc., 630 E. Young St., Santa Ana, CA 92705; (714) 540-4914. From $139. Available from stock. **CIRCLE 323**

NOTEBOOK PCs COME WITH HARD DRIVE AND TAKE STANDARD 3-1/2-IN. DISKS

Following in the footsteps of their competitors, Compaq Computer Corp., Houston, TX, has introduced two "notebook" PCs. These computers, the LTE/286 and the LTE, measure 8-1/2 by 11 by 2 in. and easily fit in a standard briefcase with plenty of room to spare. They

weigh only 6 lbs. each.

The difference between these computers and the others is that Compaq's use a 1.44-Mbyte, 3-1/2-in. disk drive. Also, a 20- or 40-Mbyte hard drive is available.

The two PCs look identical on the outside. The biggest difference is that the LTE/286 employs an 80C286 processor running at 12 MHz. Its companion, the LTE, uses a 9.54-MHz 80C86.

One of the major concerns of notebook-PC users is the battery life per charge. According to the company, the computers' enhanced NiCad battery pack lasts more than three hours under normal use. Not only that, it recharges in just 1-1/2 hours. Or, it can be charged during operation if an ac source is available. This takes from eightto 10 hours.

Both versions come standard with 640 kbytes of RAM. The LTE/286 is expandable up to 2 Mbytes, while the LTE can be expanded up to 1 Mbyte. Five different configurations are available in all. The LTE starts at $2399 while the LTE/286 starts at $3899. Both are available now.

Compaq Computer Corp., P.O. Box 692000, Houston, TX 77269; (713) 370-0670. **CIRCLE 324**

RICHARD NASS

PRINTER FOR MACINTOSH OFFERS LASER QUALITY

An ink-jet printer developed specifically for the Apple Macintosh computer provides laser-quality printing at a personal printer price. Called the HP DeskWriter, the printer features a resolution of 300 by 300 dots/in. on plain paper. It produces a page of text and graphics at speeds comparable to that of an Apple LaserWriter. What's more, users can increase printing speed by up to 50% by selecting the draft-quality mode, which produces 150 by 150 dots/in. The HP DeskWriter supports all Macintosh QuickDraw features, including font rotation in 90-degree increments, font substitution, precision bitmap printing, and document reduction and enlargement. It sells for $1195.

Hewlett-Packard Co. Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; call local sales office. **CIRCLE 325**

LIGHT LAPTOP HAS 20-MBYTE HARD DRIVE

Weighing only 9.5 lb, the GRiDLITE XL (extra light) is one of the lightest laptop computers to sport a fast-access 20-Mbyte hard-disk drive. It is also one of the first to incorporate the latest high-contrast, low-power display technology. The reflective liquid-crystal display produces sharp, easily readable text and graphics, both indoors and outdoors, with 12:1 contrast ratio. Moreover, the reflective-film, black-and-white supertwist display requires less power than backlit, double-supertwist LCDs. The GRiDLITE XL is based on an 80C86 processor and comes with a 3-1/2-in. 1.44-Mbyte floppy-disk drive and 128 kbytes of RAM. The optional 2-1/2-in. 20-Mbyte hard-disk drive has an access time of 28 ms. Other options include a 2400-baud MNP-compatible internal modem, 640 kbytes of RAM (expandable to 2 Mbytes), and an 8087 math coprocessor. The standard configuration is priced at $1950.

GRiD Systems Corp., 47211 Lakeview Blvd., Fremont, CA 94538; (415) 656-4700. **CIRCLE 326**

TRACKBALL OUTPERFORMS CONVENTIONAL MOUSE

Designed to work with IBM PC, Apple II, and Macintosh computers, a high-performance trackball can replace conventional mouse devices in CAD, CAM, CAE, and other object-oriented applications. Called RollerMouse, the unit offers three times the pointing accuracy and positioning speed of most pointing devices. And, it is less susceptible to problems such as dust. It is based on an opto-mechanical design with precise point-and-click action on an X and Y axis.

RollerMouse supports a resolution of 200 dots/in. and features automatic acceleration, which matches the speed of the ball to the cursor for pin-point accuracy. The trackball is 100% compatible with the Microsoft Mouse. PS/2 and Macintosh versions provide full keyboard protocol implementation. It sells for $169.95, including a one-year replacement warranty.

CH Products Inc., 1225 Stone Dr., San Marcos, CA 92069; (619) 744-8546. **CIRCLE 327**

8-IN. DRIVE BREAKS 2-GBYTE BARRIER

With the introduction of the M2392K, users can now have an 8-in. Winchester disk drive that stores up to 2.02 Gbytes, which is 800 Mbytes more than any other 8-in. OEM disk drive. What's more, it does so with an average access time of only 12 ms. The drive gives system OEMS greater storage capacity in a smaller footprint than is possible with multiple 5-1/4-in. drives, and it consumes less power per megabyte than any other 8-in. disk drive.

The M2392K has an ESMD transfer rate of 3 Mbytes/s and an MTBF in excess of 50,000 hours. Track capacity is 50,400 bytes, which can be read at a track-to-track rate of 2 ms. The drive sells for $6995 in OEM quantities.

Fujitsu America Inc., Computer Products Group, 3055 Orchard Dr., San Jose, CA 95134; (408) 432-1300. **CIRCLE 328**

8-Pole Active Circuits Bring Precision Filtering To 16-Bit Linear Systems

A family of fixed-frequency, high- and low-pass active filters from Frequency Devices offers wide dynamic range and a broad selection of transfer functions. All six of these 680-series models are user-specified for a corner frequency between 100 Hz and 51.2 kHz, ±2%. They couple a typical total-harmonic-distortion floor of –94 dB with the 100-dB dynamic range needed for 15-bit data acquisition.

The following transfer functions are offered: 8-pole low-pass Butterworth, 8-pole low-pass Bessel, 8-pole and 6-zero low-pass elliptic, 8-pole and 6-zero constant delay, 8-pole high-pass Butterworth, and 8-pole and 6-zero high-pass elliptic. All handle a full ±10-V input signal, and the output is free of switching spikes.

The four low-pass models are aimed at anti-aliasing applications. The low-pass Butterworth and Bessel units exhibit monotonic stopband rolloff that reaches 160-dB/decade well above the 3-dB corner frequency. The Butterworth filter gives maximally flat passband gain while the Bessel achieves constant delay and a transient response free of overshoot.

The gain of the elliptic low-pass unit plummets 80 dB from the 0.03-dB passband edge to within just 1.77 times the corner frequency. This response handles antialiasing jobs where sampling and signal frequencies are close and phase and pulse response are not critical. The constant-delay filter, used when linear phase response is needed and high speed is not, reaches 80-dB attenuation at 3.57 times the corner frequency, a far faster rolloff than a classic Bessel filter provides.

In quantities of 100, each of the Model 680 filters in their 2-by-3-by-0.4-in. modules costs $69. Delivery is in 4 weeks for small quantities.

Frequency Devices Inc., 25 Locust St., Haverhill MA, 01830; Frank DeGiso, (508) 474-0761.

CIRCLE 329

FRANK GOODENOUGH

Varistors Suppress Lightning Strikes

Employing metal-oxide varistors as its primary suppression components, the Surge Master B series of high-end lightning protectors provides excellent transient absorption to protect sensitive equipment inside an entire facility. Units are available for most standard electrical service, including 120-, 240-, and 480-V ac service, as well as single- or three-phase wye and delta systems. Each module is designed to handle repeated surges and spikes and has a component reaction time of less than 5 ns. The devices feature an audible alarm, on-board diagnostics, self-test capability, and remote monitoring capabilities using low-cost telephone cabling.

MCG Electronics Inc., 12 Burt Dr., Deer Park, NY 11729; (516) 586-5125. **CIRCLE 330**

Insulators Help Dissipate Heat

Two thermal-management products provide low thermal resistance and excellent electrical insulation for power components over a wide range of operating conditions. Thermstrate interface pads effectively transfer heat to increase component life and reliability. The thermally conductive die-cut pads provide a contact thermal resistance of 0.019°C/W. Isostrate thermally conductive electrical insulators offer a contact thermal resistance of 0.167°C/W and a dielectric strength of 4000 V.

Power Devices Inc., Thermal Interface Products Group, 27071 Cabot Rd., Bldg. 114, Laguna Hills, CA 92653; (714) 582-6712. **CIRCLE 331**

220-W Unit Powers Medical Equipment

Intended for use with medical electronic equipment, a quad-output 220-W switching power supply meets the stringent low ac line leakage limits of UL 544 and IEC601 for patient attachment. What's more, it does so in a lightweight, low-profile package that is only 9 by 5 by 2.5 in. The unit provides 30 A of +5 V for logic and memory and peak currents of up to 12 A for motor starting. Two auxiliary outputs of ±12 or ±15 V at 1.5 A are also provided. The open-frame construction of the MDT-224 is designed to efficiently transfer heat energy to the outside frame. Unit pricing in quantities of 100 is $265. Delivery takes six weeks.

Todd Products Corp., 50 Emjay Blvd., Brentwood, NY 11717; (516) 231-3366. **CIRCLE 332**

Power Package Boosts MOSFET Drive Speed

A family of MOSFET drivers housed in TO-220 power packages can drive capacitive loads of up to 30,000 pF at 1 MHz or 15,000 pF at 3.0 MHz — ten times that of conventional MOSFET drivers. The power packaging of the TSC4420/29 family enables the devices to outperform any other type of MOSFET driver currently available. The 6-A drivers offer such inherent advantages as latch-up-proof input, immunity to ground spikes above or below ground, latch-up protection against reverse currents into the output, and ESD protection. Pricing starts at $2.79 in lots of 100. Delivery is from stock to six weeks.

Teledyne Semiconductor Corp., 1300 Terra Bella Ave., Mountain View, CA 94039; (415) 968-9241.

CIRCLE 333

Lithium Battery Backs Up PC Memory

Designed specifically for computer memory backup systems, including those of the IBM PC, a 3.6-V lithium thionyl chloride battery boasts a capacity of 1900 mAh and an operating temperature of –55° to +85°C (–67° to +185°F). The ER6, which comprises a AA battery, is encapsulated in a plastic case. It comes with a lead and connector, which allows for foolproof replacement by the user. The device is designed exclusively for the industrial market.

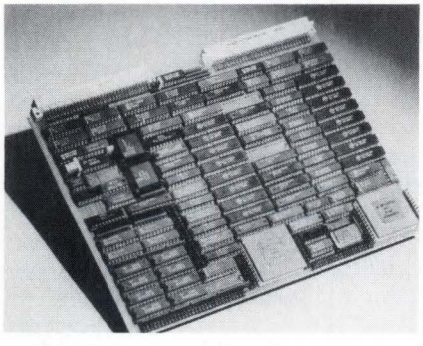
Maxell Corp. of America, 22-08 Rt. 208, Fair Lawn, NJ 07410; (201) 794-5900. **CIRCLE 334**

DSP Board Develops, Tests Applications On VMEbus Workstations

Applications for AT&T's WE DSP32C floating-point digital-signal processor can be developed and tested on VMEbus workstations using the company's WE DSP32C development board. The board provides 50 MFLOPS of arithmetic throughput with two DSP32C devices.

With the DSP32C VMEbus board, designers who implement digital-signal processors in large systems, such as Sun Microsystems workstations, can take advantage of the DSP32C processor's speed and flexibility. Designers of large systems can create and simulate graphics, image-processing, speech, and audio applications.

In addition to its high throughput, the board has a private backplane bus with 24-Mbyte/s I/O-data throughput. Expansion connectors



enable users to add custom circuitry on daughterboards. The board also enjoys Sun software-library support.

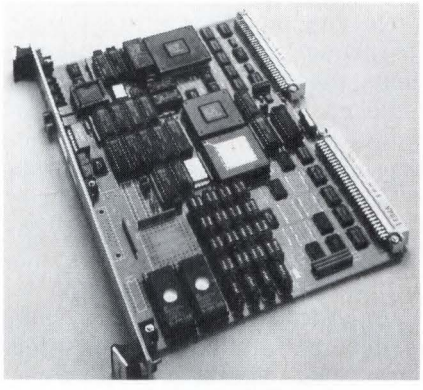
In addition to the development board, AT&T offers software-development tools that can be used on AT&T 6300 personal computers and compatibles, Apple Macintoshes, and VAX 11/780-series computers.

The VMEbus development board for the DSP32C digital-signal processor costs $7500 in single quantities. It will be available in the first quarter of 1990.

AT&T Microelectronics, Dept. 52AL330240, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447. **CIRCLE 335**

DAVID MALINIAK

VME Board Takes On Interprocessor Tasks



Suitable for applications in communications, industrial control, robotics, and process control, a 68020-based single-board computer offers a wide range of interprocessor communication and control functions, along with a fully programmable VMEbus interface. Custom gate arrays provide the programmable link with the VMEbus and allow dynamic software configuration of addresses and functions typically requiring hardware jumpers.

The board, designated the VPU-21, can address the short I/O (A16), standard (A24), and extended (A32) address spaces and transfer byte (D08), word (D16), and long-word (D32) data. It comes with 1 Mbyte of dual-port dynamic RAM and sockets for up to 256 kbytes of EPROM and up to 8 kbytes of EEPROM or nonvolatile RAM. Also included are two RS-232-C I/O channels, a 16-bit counter-timer, and a battery-backed real-time clock.

SBE Inc., 2400 Bisso Lane, Concord, CA 94520; (800) 221-6458 or (415) 680-7722. **CIRCLE 336**

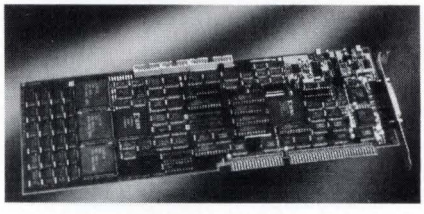
Mac Converters Boast 16-Bit Resolution

Optimized for high-resolution data sampling and conversion, the MBC-GAD and MBC-DAC are plug-in daughterboards for the MBC-625 data-acquisition system for Macintosh II and SE microcomputers. The latter provides two independent 16-bit analog output channels that can process100,000 samples/s at voltage accuracies to within 0.006%. The voltage range of each channel is fixed at ±10 V.

The MBC-GAD performs a 16-bit analog-to-digital conversion at a rate of 16,000 samples/s. Resolution is one part in 65,536 with a measurement accuracy to within 0.003%. The differential analog input may be configured for voltage ranges of ±2.5, ±5, ±10, 0 to 5, or 0 to 10 V. Both units are driven from programs written in languages such as Basic, Pascal, C, or Fortran. The MBC-GAD and MBC-DAC are priced at $550 and $475, respectively. Delivery is from stock.

MetraByte Corp., 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000. **CIRCLE 337**

Imaging Cards Supply Mid-Level Functions



A family of PC AT-based frame grabbers gives OEMs and system integrators a choice of image processors with mid-level capabilities for applications in image analysis, machine vision, and scientific research. Currently, the Visionplus-AT line consists of four boards: an overlay frame grabber (OFG), a color frame grabber (CFG), an advanced frame grabber (AFG), and an image processing accelerator (IPA). All of the frame grabbers can communicate directly with the IPA through Imaging Technology's Visionbus, a high-speed interface that provides real-time data transfers between boards without burdening the host computer. Each board is supported by ITEX, a subroutine library consisting of hundreds of functions, and an interactive command-line interpreter. Prices range from $2395 for the OFG to $4495 for the IPA. ITEX software is between $600 and $2000 for each board.

Imaging Technology Inc., 600 W. Cummings Park, Woburn, MA 01801; (617) 938-8444. **CIRCLE 338**

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UPCOMING MEETINGS

DECEMBER

International Conference on Design for Manufacturability and Concurrent Engineering '89, December 3-6, 1989. Fontainebleau Hilton, Miami Beach, FL. Kim Takita, Management Roundtable Inc., 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-8080.

1989 Winter Simulation Conference, December 4-6, 1989. The Capital Hilton Hotel, Washington, DC. Barry Nelson, Ohio State University, Dept. of ISYEE, 1971 Neil Ave., Columbus, OH 43210; (614) 292-0610.

UNICOM '89, December 5-7, 1989. Infomart, Dallas, TX. Jozy Schlosser, North American Telecommunications Association, 2000 M St., N.W., Washington, DC 20036; (202) 296-9800, ext. 229.

American Society of Mechnical Engineers' (ASME) Winter Annual Meeting, December 10-15, 1989. San Francisco Hilton, San Fransisco, CA. Jeff Lenard, ASME, 345 E. 47th St., New York, NY 10017; (212) 705-7740.

1989 AEC Expo, December 12-14, 1989. Javits Convention Center, New York, NY. Expoconsul International Inc., 3 Independence Way, Princeton, NJ 08540; (201) 987-9400.

Technology '89 (Advanced Manufacturing & Technology Expo), December 13-14, 1989. Mesa Convention Center, Mesa, AZ. C/S Communications Inc., P.O. Box 23899, Tempe, AZ 85285; (602) 967-7444.

JANUARY

International Winter Consumer Electronics Show (CES), January 6-9, 1990. Mirage Hotel, Las Vegas, NV. Cynthia Saraniti, Electronic Industries Association/Consumer Electronics Group, 1722 Eye St., N. W., Ste. 200, Washington, DC 20006; (202) 457-8700.

ATE & Instrumentation West, January 9-11, 1990. Disneyland Hotel, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-3976 or (800) 223-7126.

SMART VI (Surface Mount and Advanced Related Technologies) Conference and Exhibition, January 15-18, 1990. Buena Vista Palace, Orlando-Lake Buena Vista, FL. EIA Components Group, 1722 Eye St., N. W., Ste. 300, Washington, DC 20006; (202)457-4930.

Fifth Annual Battery Conference '90, January 16-18, 1990. California State University, Long Beach, CA. Julie Allison, Dept. of Electrical Engineering, California State University, 1250 Bellflower Blvd., Long Beach, CA 90840; (213) 985-4605.

Network Management Conference, January 24-26, 1990. Innisbrook Resort, Tarpon Springs, FL. Frost & Sullivan Inc., 106 Fulton St., New York, NY 10038-2786; (212) 233-1080.

FEBRUARY

Application Technology Conference, February 12-15, 1990. San Jose Convention Center, San Jose, CA. Ed Teja, Systems/USA Technical Conference, American Electronics Association, 5201 Great America Pkwy., Santa Clara, CA 95054; (503) 231-9914.

Buscon '90 West, February 13-16, 1990. Long Beach Convention Center, Long Beach, CA. Sharon Green, Conference Management Corp., 200 Connecticut Ave., Norwalk, CT 06856-4990; (203) 852-0500, ext. 247.

Power Electronics Conference, February 13-16, 1990. Long Beach Convention Center, Long Beach, CA. For more info call (203) 852-0500.

International Solid State Circuits Conference (ISSCC), February 14-16, 1990. San Francisco Hilton, San Francisco, CA. For more info call (202) 347-5900.

Compcon Spring 90, February 26-March 2, 1990. Cathedral Hill Hotel, San Francisco, CA. Dr. Kenichi Miura, Fujitsu America, 3055 Orchard Dr., San Jose, CA 95134; (408) 432-1300 ext. 5408.


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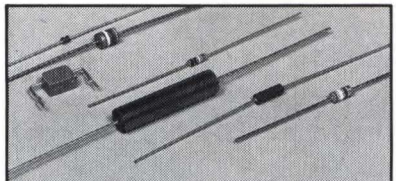

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CONVERSION DEVICES, INC., 15 Jonathan Drive, Stoughton, MA 02401. TEL: (508)559-0880 FAX: (508) 559-9288

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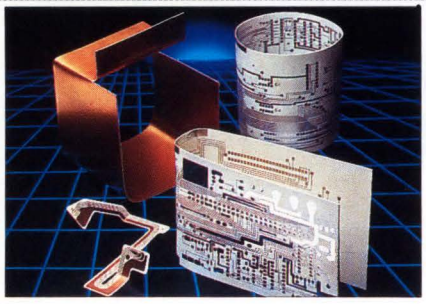

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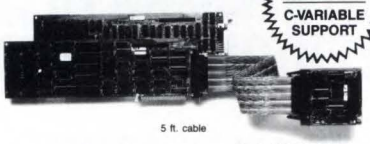

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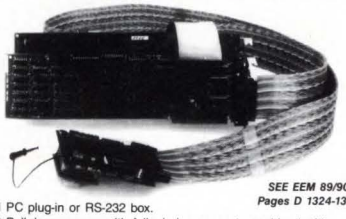

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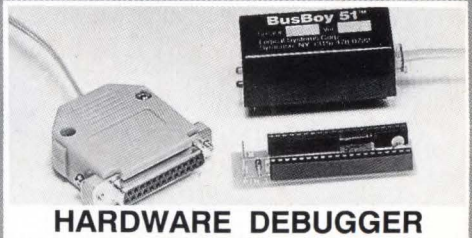

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The BusBoy51 is a new in-circuit debugging tool for 8051 based boards. Useful in both prototype and production testing, it will help isolate wiring errors and component failures. The BusBoy 51 is menu driven with a serial interface to the operators terminal. It provides pre-programmed tests for 8051 memory and I/O, detecting stuck and shorted address or data bits. The BusBoy 51 is powered by the target system and autobauds. Use the BusBoy 51 to verify prototypes, test failed boards to isolate the memory or buffer chip responsible, final check production boards for proper memory and I/O operation.

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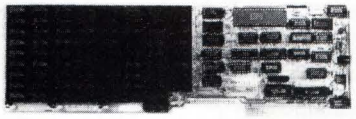

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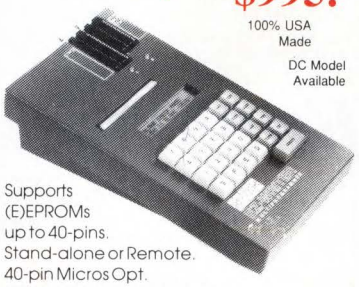

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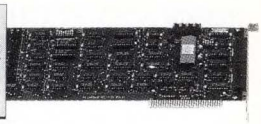

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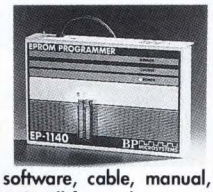

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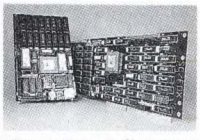

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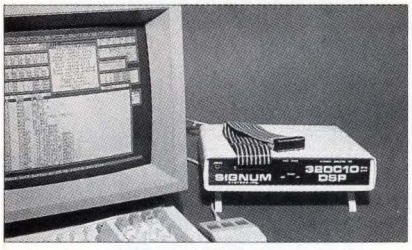

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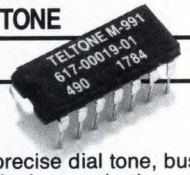

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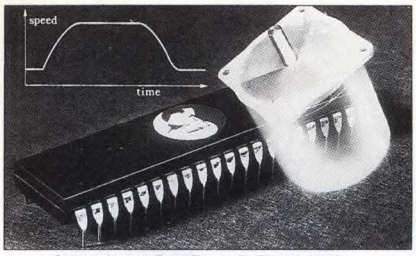

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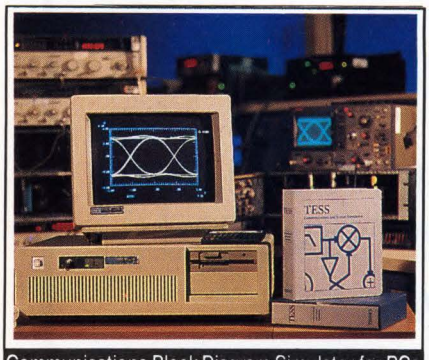

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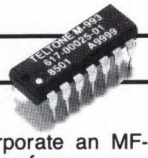

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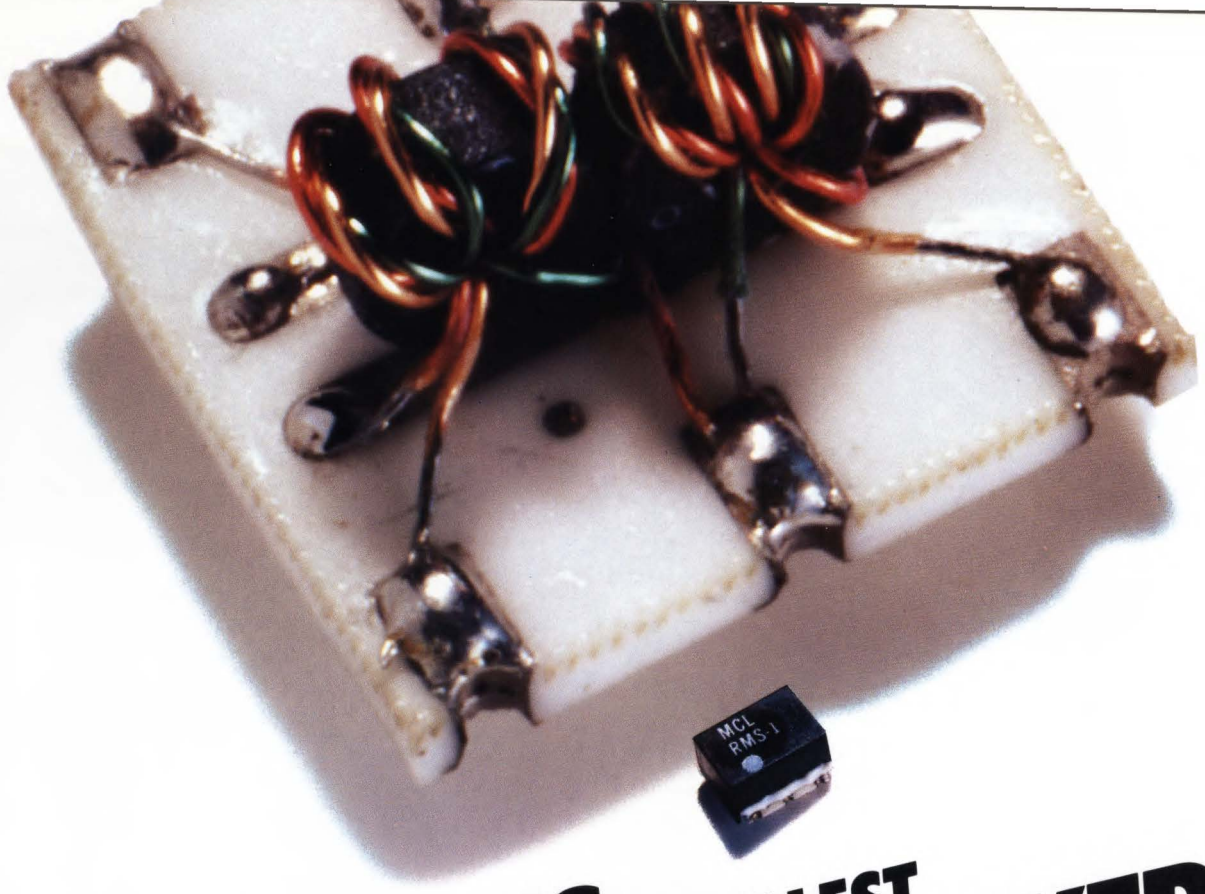

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