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ELECTRONIC DESIGN

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NOVEMBER 9, 1989



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IRC640
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IRFD9024

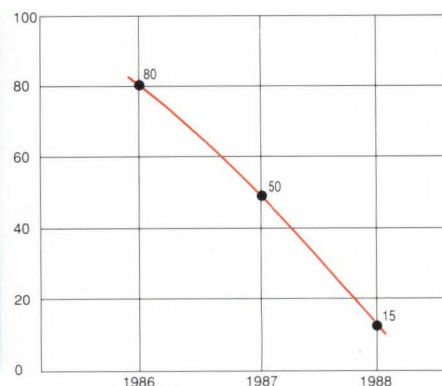
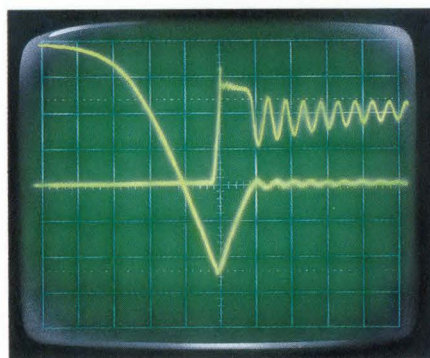
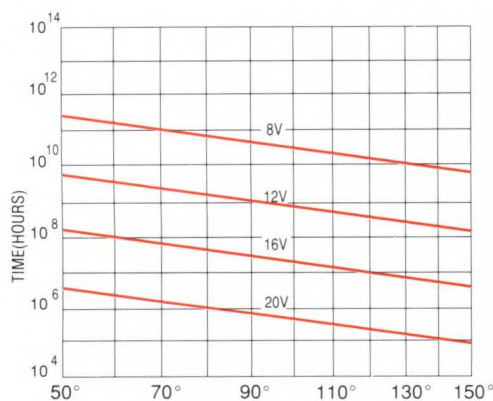
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IRF9140
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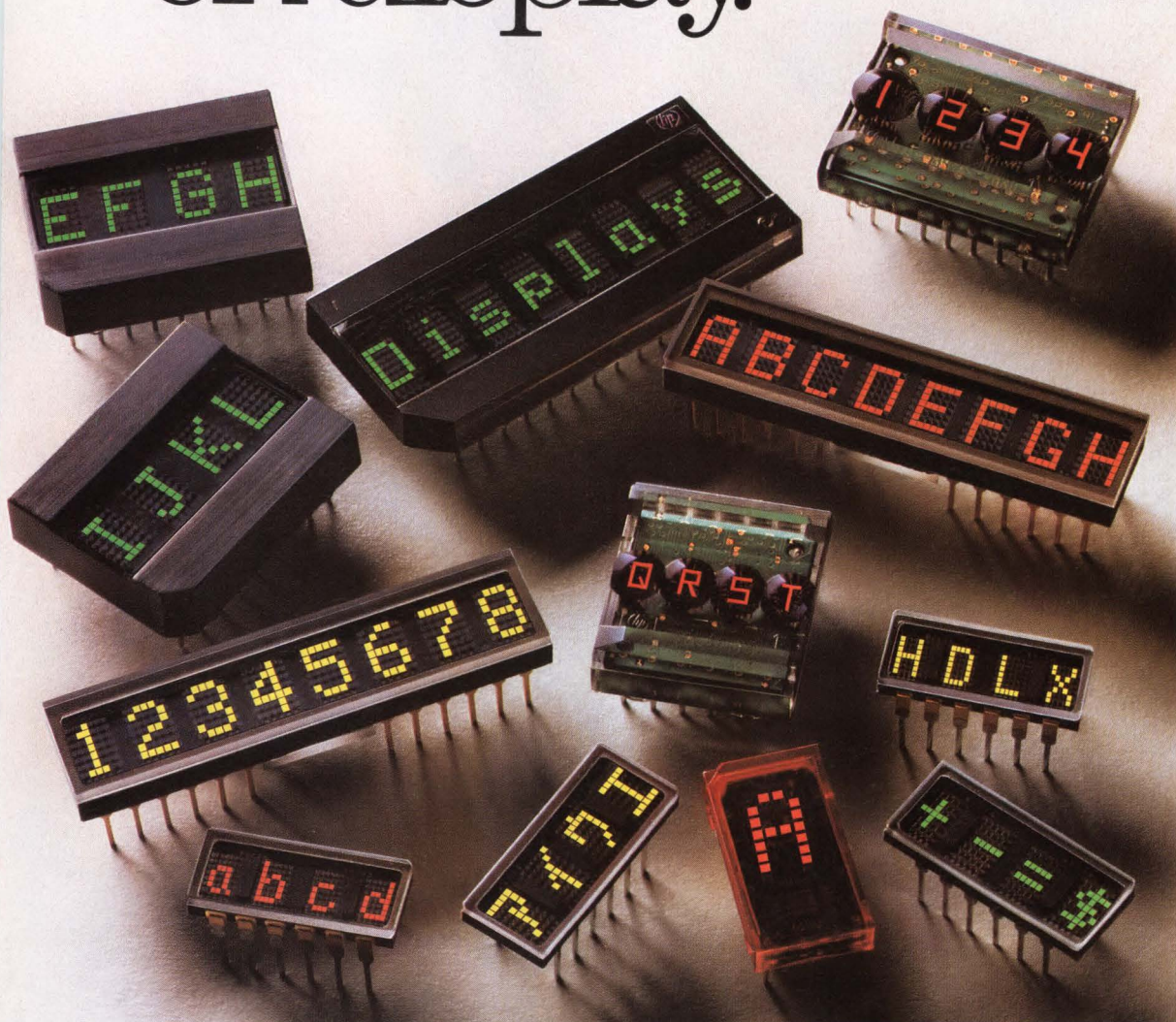
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CIRCLE 85



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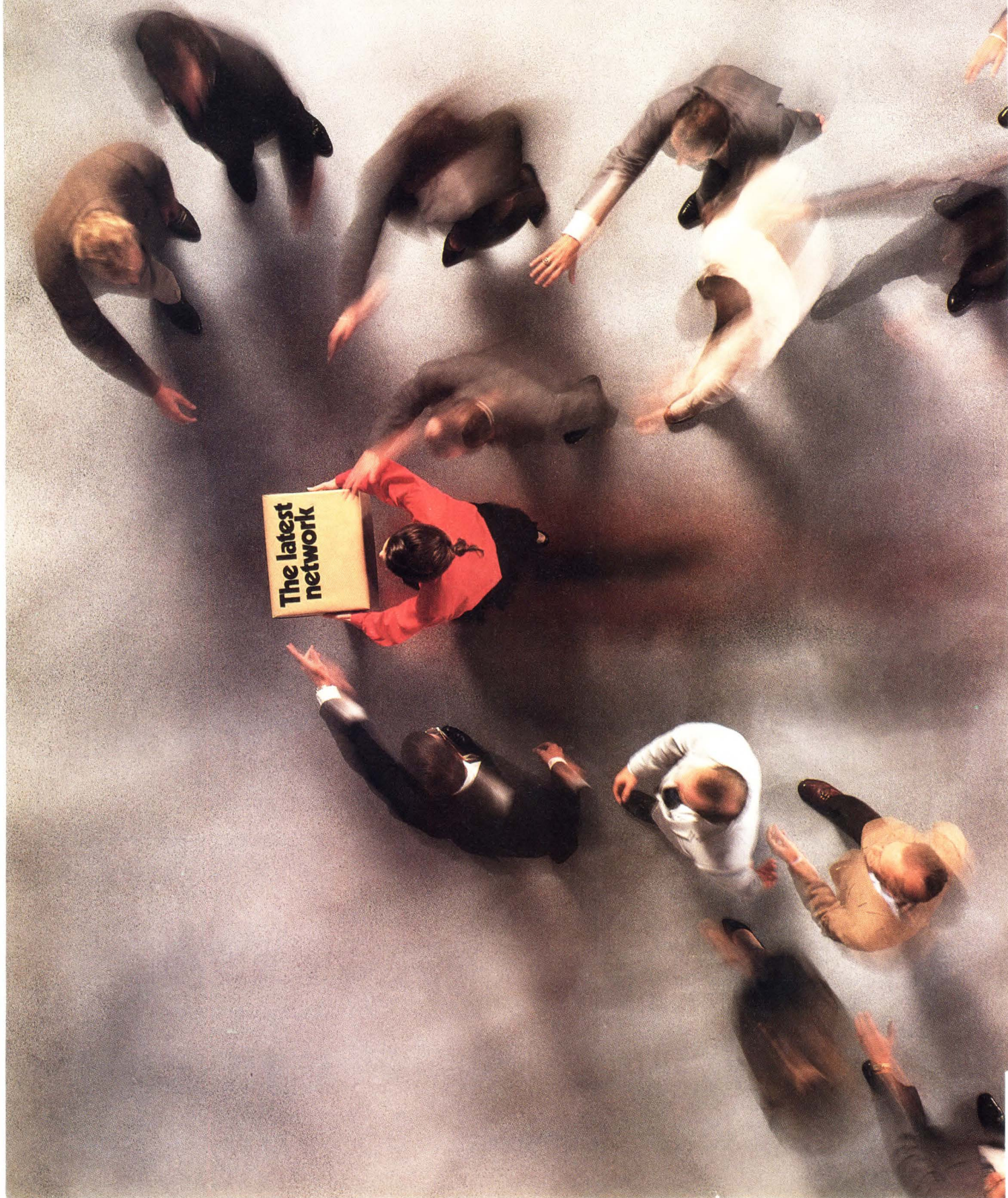
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There is a better way.



**HEWLETT
PACKARD**

You didn't get into this



business to come in second.

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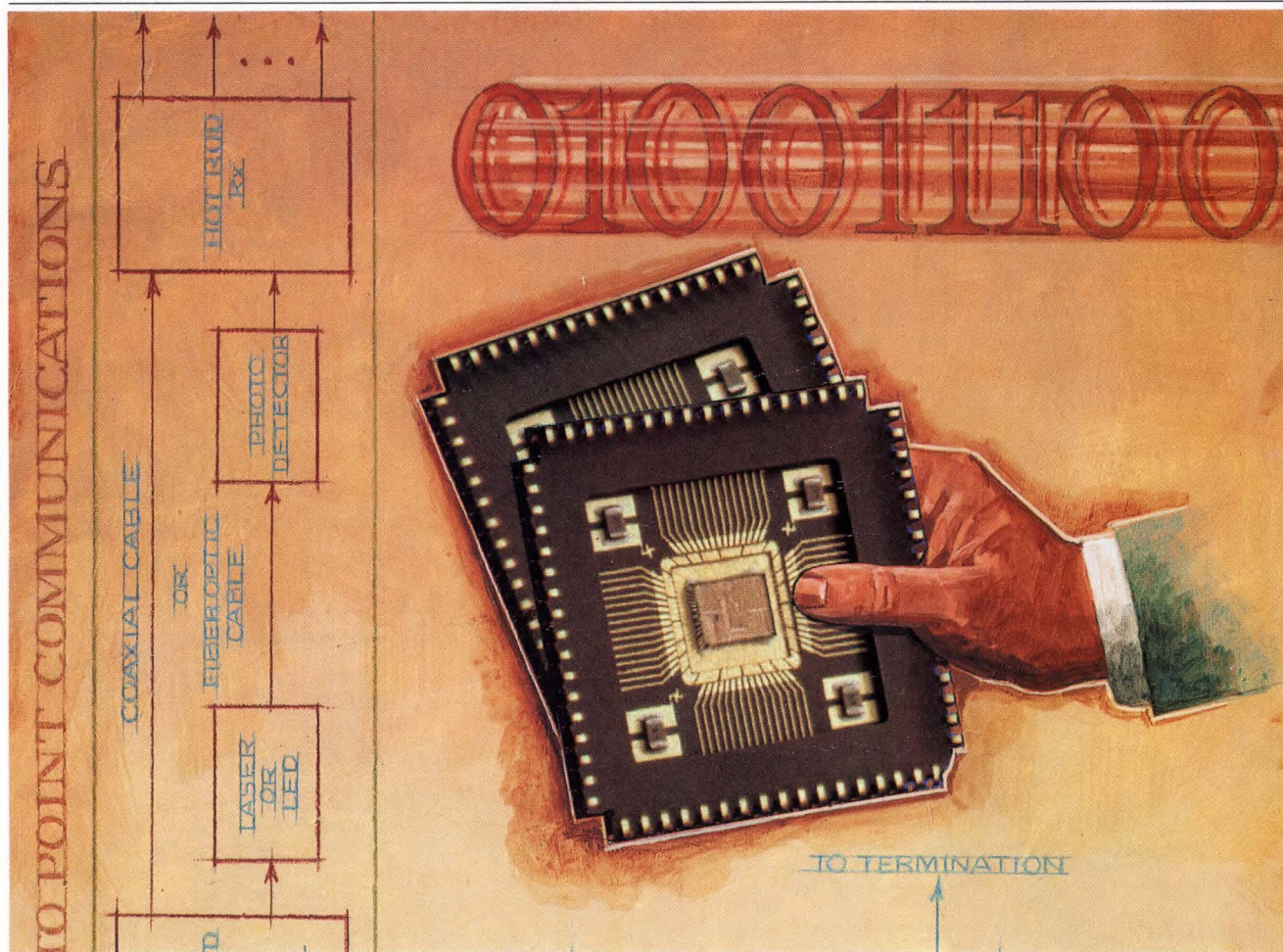
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CIRCLE 49

ELECTRONIC DESIGN



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At this year's show, the big news is ICs, not PCs.

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51 GAAS CHIP SET SHUTTLES SERIAL DATA

Accepting and delivering parallel data at 25 MHz, these GaAs chips eliminate wide, fast buses by transferring data serially at 1 Gbit/s.

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89 ADD COLOR IMAGING TO GRAPHICS

Two dedicated CMOS ASICs, running at real-time video rates, anchor a color-value-conversion circuit that enhances imaging capabilities.

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141 8-BIT CONTROLLERS BOOST THROUGHPUT

RISC-like architecture improves instruction efficiency with just two cycles.

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Computer makers can now go head-to-head

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- ASICs combine fast, low-power circuits

29 TECHNOLOGY ADVANCES

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111 IDEAS FOR DESIGN

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- A preview of VLSI innovations to be discussed at the 1989 International Electron Devices Meeting.
- Special Report on RISC-based systems.
- Designing software for parallel-processing systems.
- Design details on two impressive new microcontrollers.
- How VRAMs deliver faster memories with less critical timing.

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi-monthly with one additional issue in March, June, September and December by Penton Publishing, Inc., 1100 Superior Ave., Cleveland, OH 44114. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6000. Facsimile (201) 393-0204.

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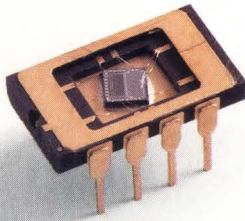
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**Your
perceptions
of
power ICs
are about to
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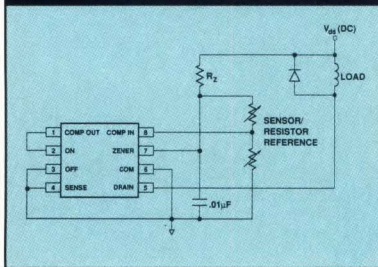


400 Volt

The times, they are a' changin'—Power Integrations

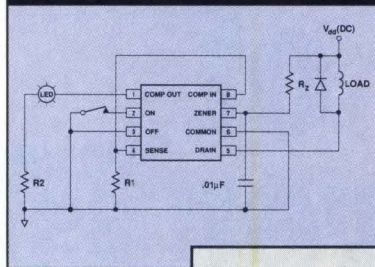
Simple to use.

Analog sensor application



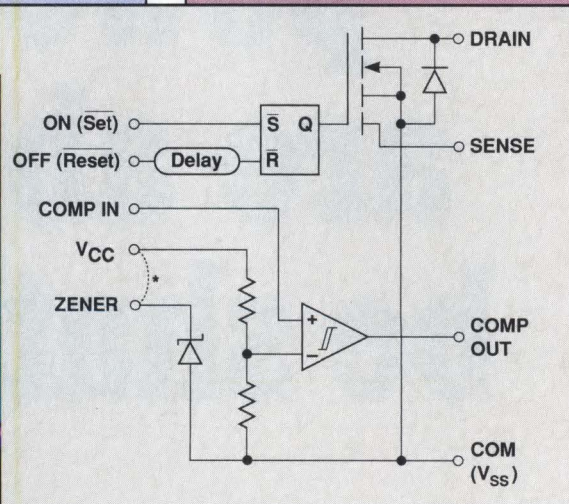
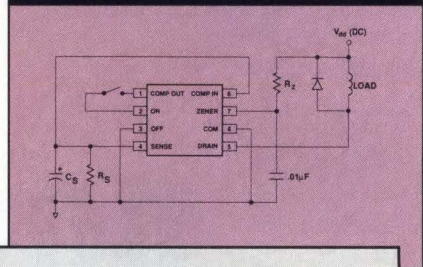
Adds more value.

LED can indicate current thru load



More versatile.

Simple pulse width modulation



The PWR-DRV1 Universal Power Driver is an easy-to-implement, cost-effective interface between control electronics and high voltage loads such as displays, relays and solenoids.

- 200V, 300V, 400V versions
- 350mA
- $R_{DS(ON)}$ 5Ω

- Operates from rectified AC or DC power source
- Controlled by analog sensors, mechanical switches and digital logic (TTL or CMOS)
- On-board low voltage power for control circuitry

- Variable output (operates low voltage loads from high voltage, reduces power consumed by a load)
- Controls an AC load from a DC power source
- Measures current without external voltage drops

Rock'n Roll!

bridges the gap between high and low voltage.

Remember the first time you heard Elvis, Dylan, the Stones or the Beatles? You were experiencing something different. And you knew your life would never be the same. Well, Power Integrations is about to do it to you again!

Not musically. But professionally. And profoundly. With a brand new **CMOS Power IC** technology that's easy to implement in both electronic and electro-mechanical designs.

Our new family of 200V, 300V and 400V enabling ICs will have you "rocking around the clock" developing new products. And rolling over the competition with your new-found ability to interface directly with solid state.

Now you can control almost anything! From automatic pumps to the fully electronic home. Upgrade or customize your current system. Or innovate—demonstrating your engineering genius and creativity.

The enabling functions of our ICs generate added system value far beyond the price of the parts they replace. And they interface with 5V logic. Easily. Reducing the risk of product failure and enhancing your reputation as an innovative, yet reliable designer.

Imagine what you can do with a...

Universal Power Driver (PWR-DRV1) that provides all necessary interface between electro-mechanical loads and electronic circuits. And produces variable output. Or a...

Dual Relay/ Solenoid Driver (PWR-DRV2) that saves board space and prevents simultaneous "on" states. Or an...

Isolated Relay/Solenoid Driver (PWR-ISO1) that alleviates potential system failure by isolating control logic up to 1500V. Or a...

Dual Level Power Driver (PWR-DRV3) that allows quick actuation and then reduced power. Or...

High-Voltage Peripheral Drivers (PWR-DRV451/2/3/4), that interconnect digital logic to the AC line. And are pin-compatible with 75451s and 3611s. Or an...

8-Channel MOSFET Array (PWR-NCH801) a single chip that provides more power in less space. Eight high

voltage channels controlled directly from digital logic signals.

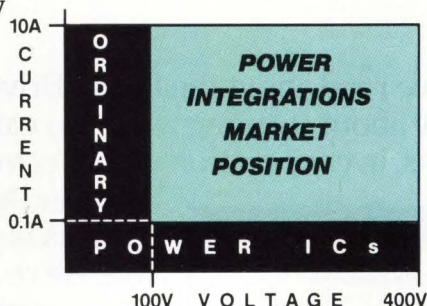
We've provided the intro with our enabling ICs. And created the bridge between low and high voltage. Now it's time to rock 'n roll!

We're Power Integrations—bringing you the power to control. Our lines are open and we're taking requests. So pick up the phone and call for samples and more information. Or lay down some hot application licks on your PC and FAX them to our application support team.

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The Power to Control

411 Clyde Avenue
Mountain View, CA 94043

And the beat goes on...

Win an Epson portable Computer! Or a Casio Digital Diary! Or a Sony Watchman TV!

Now that you've read about the Power Driver 1. (See the previous three pages.) How about showing what you can do with it? Power Integrations, in cooperation with *Electronic Design*, is sponsoring


a **Power Driver 1 Design Contest.**

This is your chance to be innovative. We're looking for the most clever application of the PWR-DRV 1 Universal Driver.

Judging. Power Integrations will pick the ten best PWR-DRV 1 design applications and submit them to the editorial staff of *Electronic Design* for final judging. The top five entries will be announced in one of the March issues of this publication.

Design Contest Prizes	
1st Prize:	Epson Equity portable computer with 20MB hard drive and 3.5" floppy.
2nd Prize:	A Casio 32K Digital Diary that stores up to 1500 names and phone numbers.
3rd thru 5th Prizes:	A Sony Watch Man TV
6th thru 10th Prizes:	Autographed copies of <i>Marketing High Technology</i> , <i>An Insider's View</i> by Bill Davidow

How to enter: Just call Power Integrations at 1-800-552-3155 for an entry form and free PWR-DRV 1 samples. Or write to us at 411 Clyde Avenue, Mountain View, CA 94043.

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INTEGRATIONS, INC.
The Power to Control

	MODEL	DESCRIPTION	ANALOG INPUT		Resolution (bits)	Channels	TI	PRICE
			Channels	Resolution (bits)				
LOW COST	DT2811-PGH	Low Cost A/D, D/A, Interrupt	16SE/8DI	12				\$795
	DT2811-PGL	Low Cost, Low-Level A/D, D/A; Interrupt	16SE/8DI	12				\$895
	DT2814	Low Cost A/D, Int.	16SE	12				\$395
	DT2815	Low Cost D/A	—	—				\$575
	DT2817	Low Cost DIO	—	—				\$239
	DT2819	Am2935A Counter/Timer, DIO	—	—				consult factory
GENERAL PURPOSE	DT2808	Low Cost, DMA	16SE	10				\$595
	DT2801	General Purpose, DMA	16SE/8DI	12				\$995
	DT2801-A	Higher Throughput, DMA	16SE/8DI	12				\$1,095
	DT2801/5716A	High Resolution, DMA	8DI	16				\$1,970
	DT2805	Low Level, DMA	8DI	12				\$1,095
	DT2805/5716A	Low Level, DMA	8DI	16				\$2,070
	DT2809	16-bit SS&H, DMA	8SE, SS&H	16				\$2,495
	DT2816	SS&H, DMA	4SE, SS&H	12				\$1,895
	DT2824-PCH	High Throughput, Low Cost A/D; DMA, Ints.	16SE/8DI	12				\$1,095
	DT2824-PCL	High Throughput, DMA	16SE/8DI	12				\$1,345
HIGH SPEED	DT2821	High Throughput, DMA	16SE/8DI	12				\$1,995
	DT2821-F-16SE, DT2821-F-8DI	Very High Throughput, DMA, Interrupts	16SE or 8DI					\$2,995
	DT2821-G-16SE, DT2821-G-8DI	Ultra High Throughput, DMA, Interrupts	16SE or 8DI					\$2,895
	DT2823	High Res., DMA, Ints.	4DI					\$1,545
	DT2825	Low Level, DMA, Ints.	16SE/8DI					\$2,595
	DT2827	High Resolution, DMA	4DI					\$2,195
	DT2828	High Throughput, SS&H, DMA, Interrupts	4SE, SS&H					\$2,995
	DT2829	16-bit SS&H, DMA, Int.	8SE, SS&H					\$1,450
	DT2841	40kHz, DT-Connect™	16SE/8DI					\$2,095
	DT2841-F-16SE, DT2841-F-8DI	150kHz, DT-Connect™	16SE or 8DI					\$2,695
	DT2841-G-16SE, DT2841-G-8DI	250kHz, DT-Connect™	16SE or 8DI					\$2,995
	DT2841-L	750kHz, DT-Connect™	4DI					\$2,495
DT-Connect™	DT2847	16-bit, DT-Connect™	4DI					\$2,095
	DT2848	SS&H, DT-Connect™	4SE					\$375 to \$2,140
	DT2806	16-bit A/D	Up to 80SE/40DI	12				
	DT2806	16-bit A/D	Up to 80SE/40DI	12				

Pages 16-17, New Products Handbook

—Fred Molinari, President

Year after year, we win acclaim for having the standard in the industry.

The DT2801 general purpose data acquisition board.

Most informed people would tell you that this is the board that actually launched the data acquisition industry, particularly for scientific, medical, and industrial applications.

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FREE

*Making the change from
Analog to Digital scopes.*

**Scope Evaluation Guide
& Circuit Board instructions**



The Digital Scope Evaluation Kit



Do 3 simple tests you'd expect any digitizing scope to pass. And see why some don't.

Beware of bargain digitizing oscilloscopes that look good on paper but fall apart on the job.

Now, put any 100-500 MHz DSO to a true test of ability with Tek's free Scope Evaluation Kit.

All you need is a scope, ten minutes of your time, and this free kit.

You'll discover how well the scope you're testing stands up to the three challenges facing a digitizing scope buyer:

- Will the scope miss important events?
- Will it trigger on your signals?

- Will it accurately capture and measure your signals?
You can't safely assume that all scopes will meet these simple challenges.

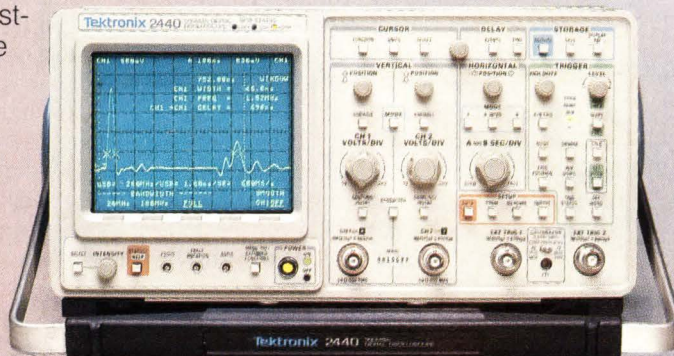
See for yourself: The kit includes a compact, surface-mount circuit board with specially-designed signals that represent typical real-world measurements.

You'll be guided by an easy-to-follow, fully illustrated instruction manual. Even the battery is included.

Before you buy a DSO, you owe it to yourself to put any scope you're considering to the test. When you put Tek digitizing scopes alongside any other DSO, we're confident you'll see the difference.

To prove the point, Tek will give you the Scope Evaluation Kit — a \$20 value. Free.

Order your scope Evaluation Kit today. Return the reply card or call Tektronix toll-free: **1-800-426-2200**

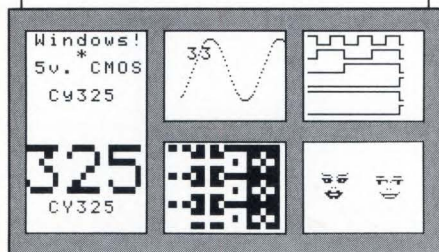


**Offer expires
March 31, 1990.**

Tektronix
YOUR VISIBLE EDGE

What's Missing on this LCD?

(answers below)



If you peeked at the answers, then you know it's Motion. In the actual LCD every one of the windows is in motion. Think for a minute how you would make six or seven unique motions simultaneously with the low level LCD controllers that you have seen. No way! Now think what your instrument or new systems could do with dynamic text and graphics. Tests show that programmers can achieve animated presentations in only hours using the CY325.

The CY325 LCD Windows Controller Chip

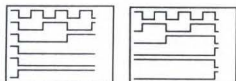


lets you: specify any of 250 built-in windows, or create your own with a single command; manage text and graphics with automatic cursor control; wrap or scroll text with window relative pixel plotting and clipping; read an A/D and write the waveform into the window; drive up to 6 I/O pins with logic waves, or use the 'soft-key' feature of the CY325 for menu management. Only \$75 each (\$20/1000)

Answer:

Motion is missing in each of the windows. Text actually scrolls up in the top left window above, and . . .

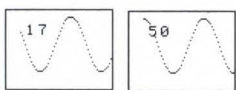
Logic waves flow right to left.



Boy and girl wink, smile, and flirt.



Counter counts and sine wave advances.



Pseudo random patterns change.



The next move is yours . . .

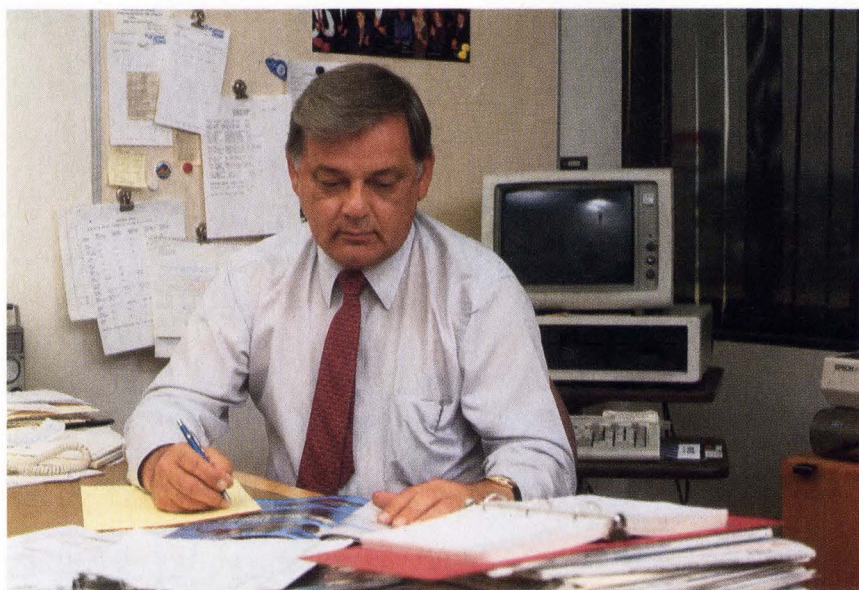
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CIRCLE 117

EDITORIAL



SURVIVAL—AND THEN GROWTH

Semiconductor manufacturers in the U.S. have good reason to put the 1980s behind them, and look forward to the 1990s—the past decade has not been particularly kind. The 1980s witnessed the Japanese takeover of the DRAM market; two mini-crashes on Wall Street; and now, with just 10 weeks left in the decade, a 6.9 Richter-scale earthquake has come along to further shake up Silicon Valley.

We realize that it's all too easy to write about a west coast earthquake from the east coast, and we are shocked and saddened by the loss of lives in the Bay area. The "health" of machines is nothing compared with human concerns. However, in some ways, the earthquake does seem consistent with this difficult decade.

Nevertheless, barring any serious aftershocks that may occur in the interval between the writing of this editorial and its appearance on readers' desks, it appears that semiconductor production facilities in the valley have come through the quake basically unscathed.

The 1990s can be an excellent decade for the U.S. semiconductor industry. The DRAM war was composed of a series of battles waged for each generation of memory density. The 1-Mbit battle is clearly over, and the 4-Mbit skirmish is probably finished, too. But, for the foreseeable future, memory-chip densities will continue to quadruple in each generation, opening new opportunities at each level. Furthermore, there are many markets to be satisfied beyond DRAMs. The 1990s will see digital, analog, and mixed-signal ASICs pervade equipment designs. The semiconductor processing technology is available, the computer-based design tools are at hand, and the applications are ready and waiting for this technique, which allows designers to essentially customize equipment for a broad spectrum of users.

Let's hope that Silicon Valley's survival of the '89 earthquake will be followed by a new era of growth.

Stephen E. Scrupski

Stephen E. Scrupski
Editor-in-Chief

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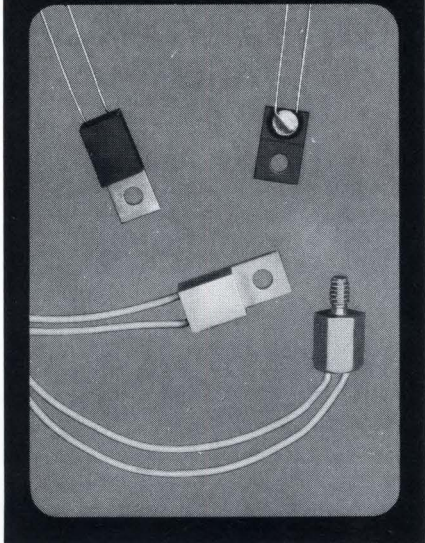
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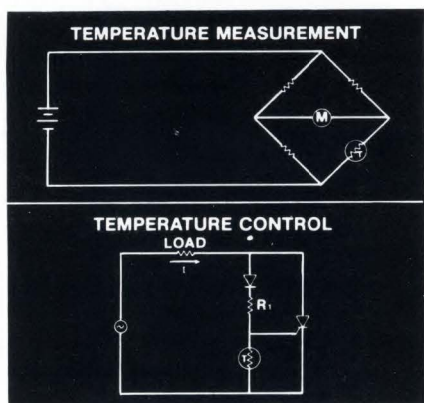


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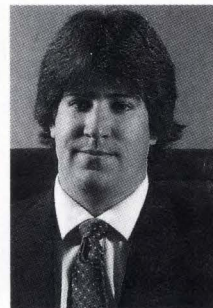
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TECHNOLOGY BRIEFING

COMPUTER MAKERS CAN GO HEAD-TO-HEAD

Computer manufacturers have always used a set of specifications to rate their products, but for no apparent reason, these specs aren't necessarily the same from manufacturer to manufacturer. Is this because manufacturers only publish specs that rate their machines highly?

Fortunately, thanks to a group that calls itself SPEC (Systems Performance Evaluation Cooperative), this situation is changing. SPEC developed a suite of benchmark programs that are effective and fair in comparing the performance of high-performance computing systems. The group also ensures that the benchmarks are readily available to users and manufacturers of these types of systems.



RICHARD NASS

COMPUTER SYSTEMS EDITOR

Recently, the group announced the availability of Release 1.0 of the SPEC Benchmark Suite, which consist of ten engineering and scientific benchmarks. Picked on the basis of their ability to demonstrate overall processor and system performance running real-world applications, the benchmarks were chosen from more than 50 originally proposed.

The initial benchmarks—additional ones are in the works—cover text processing, hardware and software simulation, scientific applications, multi-user applications, CAD, ECAD, and CASE. Benchmarks being considered for possible inclusion in a later release include multiprocessing, parallel processing, graphics, and communications (including networked systems).

The benchmarks weren't chosen on a whim—the benchmark development process is long and detailed. A proposal must go through many hands and be accepted by many industry experts before it's approved as a standard.

The SPEC guidelines are fully endorsed by the 12 current members: AT&T, Control Data Corp., Data General, Digital Equipment Corp., Hewlett-Packard Co., IBM, Intergraph Corp., MIPS Computer Systems Inc., Motorola Microcomputer Div., Multiflow Computer, Stardent, and Sun Microsystems Inc. Any company or organization can join SPEC by paying a \$10,000 initiation fee and the annual dues.

The benchmarks are: gcc, which measures the time for a Gnu Compiler to convert 19 preprocessed source files into optimized Sun-3 assembly output; Espresso, which performs heuristic Boolean-function minimization; spice 2g6, the Fortran version of Berkeley Spice, for analyzing a typical analog circuit; doduc, a nonvectorizable scaler floating-point Fortran benchmark; nasa7, a set of floating-point-intensive kernels that perform an operation and judge the solution against the expected result; Li, a Lisp interpreter that measures the time needed to solve a problem; eqntott, which produces a sorted truth table; matrix300, which uses double-precision floating-point math to measure the time between two internally-defined points; fpppp, a quantum-chemistry benchmark that measures a style of computation occurring on the GaussianXX series of programs; and tomcatv, a highly vectorizable double-precision floating-point benchmark that is a vectorized mesh-generation program.

Running the complete series of benchmarks on a high-end technical workstation or minicomputer takes about three hours. To accommodate as many machines as possible, SPEC members decided to base the benchmarks on Unix. All of the benchmarks in Release 1.0. were run successfully on VMS machines. SPEC also encourages makers of other operating systems to port the benchmarks onto their platforms.

To further facilitate fair play, all SPEC members must agree to follow common guidelines when reporting the results of the tests. These guidelines require full and complete documentation of all significant resources and configurations as well as any changes made to the benchmark tape.

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100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ.	max.	typ.	max.
	1.3	1.6	1.3	1.6
Switching Time (μsec)	typ.	max.	typ.	max.
(from 50% TTL to 90% RF)	2.0	4.0	2.0	4.0
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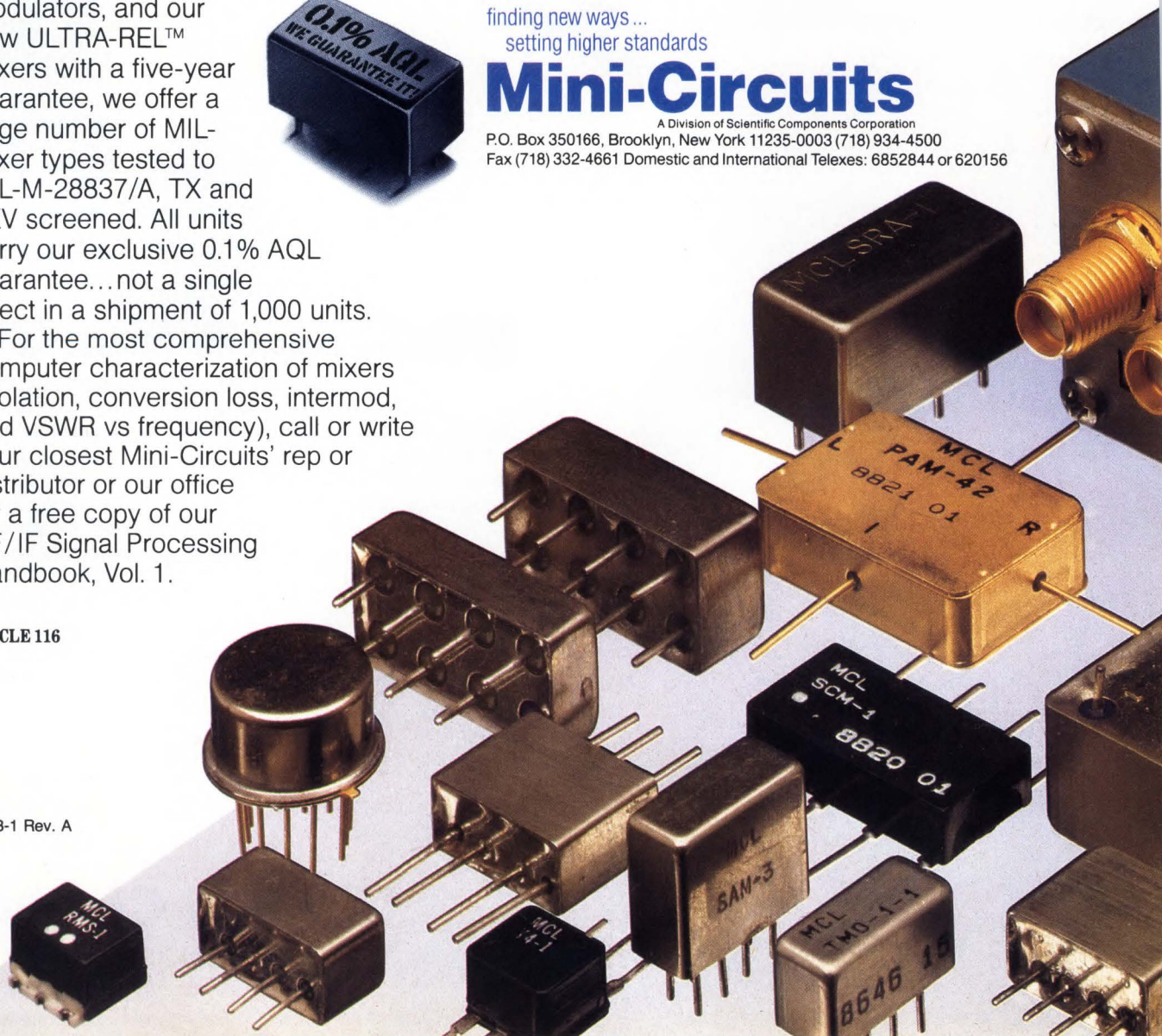
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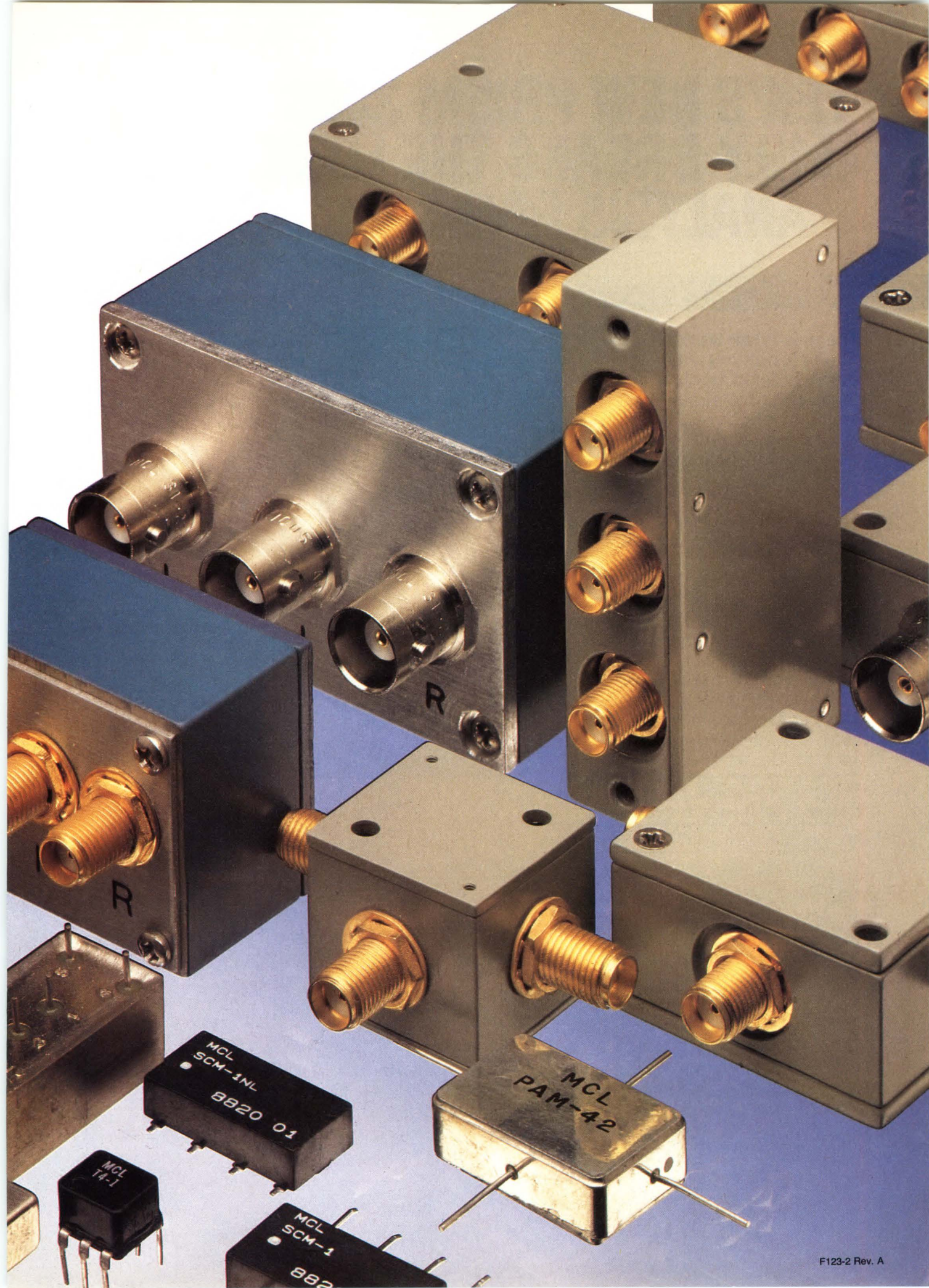
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TEK'S NEW PRISM 3000 FAMILY BREAKS THE LOGIC ANALYSIS BARRIER.



The new Prism 3000 Series is nothing less than a breakthrough in the evolution of logic analysis: once you see what it can do, you may scarcely imagine doing without it.

Now digital designers and integrators can start with all the speed, channels and memory depth they need — without tradeoffs. They can mix-and-match tools for their specific needs, including 8, 16 and 32-bit microprocessor debug modules brimming with features never before possible in a logic analyzer. They can add other modules, such as for high-speed timing and waveform analysis, later.

The new dimension of hardware/software integration.

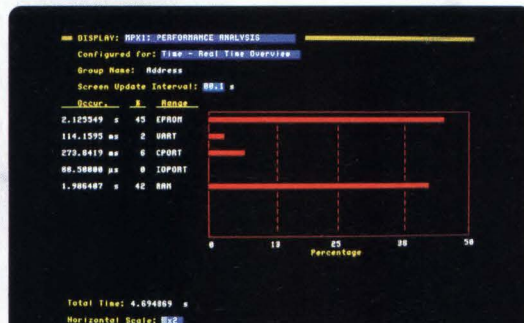
Microprocessor control

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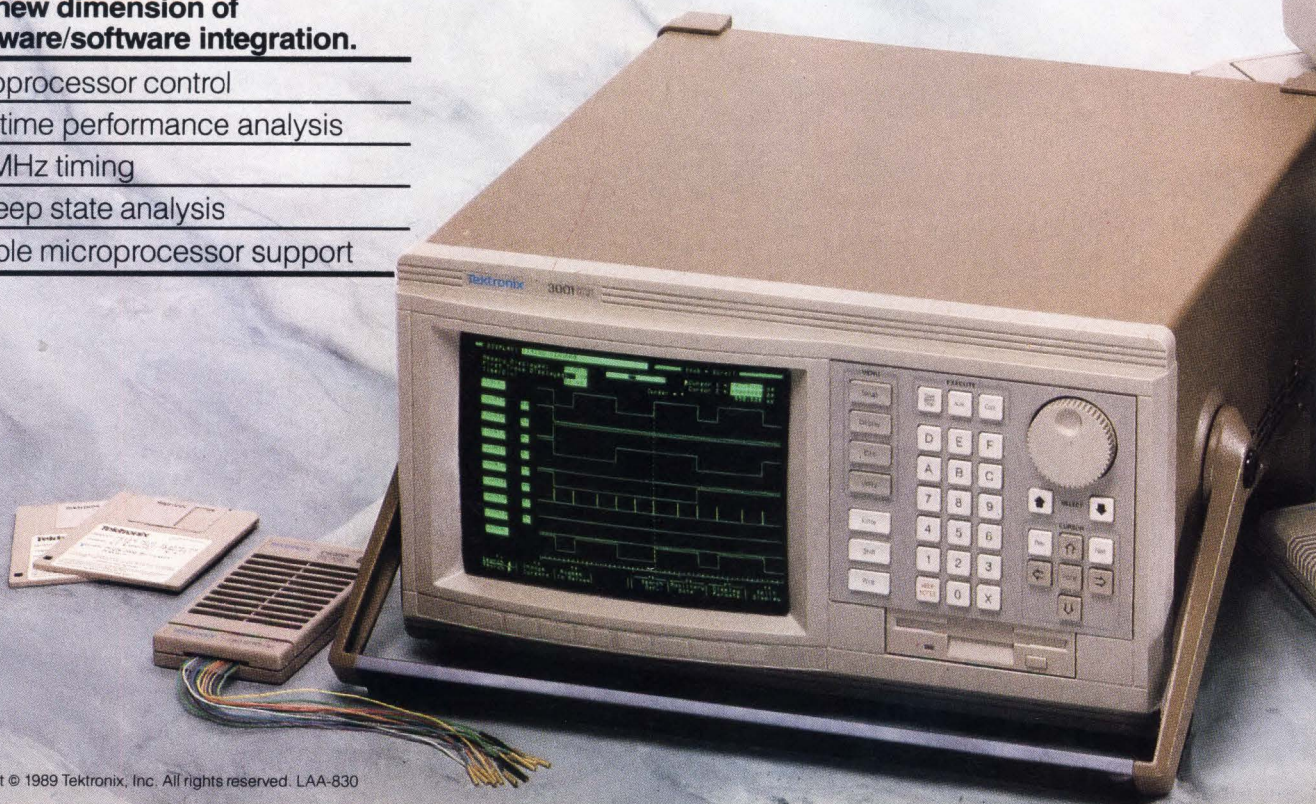


You can view 200 MHz timing and 8K of state data per channel, all time-correlated and integrated on the same display.

Observe data from multiple microprocessors or time-bases simultaneously. Set up



(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.





The Prism 3002P configuration features a slide-away keyboard and a 640x400 flat panel display that folds against the mainframe when not in use.

state and timing sections to cross-trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

Push beyond microprocessor observation into emulator-like microprocessor control.

With its unprecedented Prototype Debug Tool, Prism is the first logic analyzer to let you set breakpoints, patch registers and memory, restart

the system, and more —without an emulator's intrusiveness (or the long wait for new emulator availability).

Use real-time performance analysis to get a true, non-statistical view of system performance.

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Complete front panel controls are included on the Prism keyboard, enabling users to move easily from one Prism mainframe to another.



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IMAGE PROCESSOR PUTS 20 CPUS IN PARALLEL

A highly parallel system architecture that contains 20 Clipper microprocessors for image processing is being evaluated by the Systems and Sondertech-nik division of Philips, Bremen, W. Germany. The system can detect and symbolically describe objects in near real time. Rather than evaluate images from clusters of pixels, the symbolic approach analyzes the objects, which are represented as geometric shapes or luminance features. In contrast to a VAX 750, which requires about 15 minutes to process an image, the 20-processor Samba needs just 200 ms.

To recognize objects, the system takes data through three processing stages: object generation, object selection, and result reporting. In the first stage, gray-scale video images are digitized and split into 20 related binary images. From each image, a set of seed parameters is extracted and sent to each of the 20 Clipper CPUs (made by Intergraph Inc., Palo Alto, Calif.), which then process the data in a loosely coupled structure. Next, the processors analyze the object data to see which data sets meet a predetermined set of characteristics. In this phase the processors operate in a tightly coupled mode as a chain of 10 master-slave pairs. Information is shared by passing it up and down the chain of master-slave pairs. The last phase continually monitors objects and highlights the ones that meet the specified criteria. DB

NONSTOP PROCESSOR CLOCKS TWO INSTRUCTIONS/CYCLE

By executing two instructions per clock cycle, a multiprocessor computer system optimized for on-line transaction processing delivers almost five times the throughput of its predecessor. Just out from Tandem Computers Inc., Cupertino, Calif., the nonstop scalar computer combines 4 to 16 CPUs, each containing dual two-stage prefetch queues and dual six-stage pipelines. To maximize throughput, each processor has from two to four direct-memory-access I/O channels and controls up to 128 Mbytes of RAM. At any time, the dual pipelines keep up to 16 instructions in various stages of execution, far more than in most other systems. In addition, the system optimizes the use of its deep pipeline by employing dynamic branch prediction to deal with conditional branches.

The system draws from all technologies to optimize performance and packing density: TTL circuits serve as the communication buses; ECL circuits serve as the arithmetic and cache logic, which demands high speed; and CMOS circuits form the storage arrays, where maximum density is needed. For the most efficient cooling, a high-speed impingement system funnels cool air directly onto each high-power component. The Non-Stop Cyclone system, which supersedes the VLX series computers, is software compatible with the VLX series and can be tied to them over the Tandem's Dynalink fiber-optic serial network. DB

BOARD ADDS ZIP TO MAC II'S GRAPHICS

A Nubus board that accelerates Macintosh II graphics processing by as much as thirty-fold gets its computational muscle from a RISC chip running proprietary display-list software. Radius Inc., San Jose, Calif., held down the cost of its graphics engine by using VLSI Technology Inc.'s Acorn RISC processor, which delivers about 6 MIPS of throughput. With the board, users get nearly instantaneous redrawings, pans, and zooms. This reduces the overall waiting time and improves productivity. When a graphics command is entered, the engine quickly traverses the vector-based display list stored in system memory. Clips and transforms are performed by the Acorn processor, which relieves the Macintosh and application software of all graphics processing tasks. The Quick-CAD card was first exhibited at last month's Autofact Conference in Detroit. DB

NEW YEAR TO RING IN NEW VOLT AND OHM, TOO

Changing technology is bringing about changes in two of the most basic of electrical units: volts and ohms. As of January 1, the National Institute of Standards and Technology will establish new values for the volt and ohm based on state-of-the-art standards that use the Josephson effect and the quantum Hall effect, respectively. Also the changes will hold both units to the same worldwide standards. In the U.S., the standard volt will increase by about 9.26 ppm (parts per million), and the standard ohm by about 1.69 ppm. The institute recommends that instruments with a required accuracy of less than five times the magnitude of the change be recalibrated as soon as possible after January 1. If accuracy is more than 10 times the magnitude of the change, no adjustment is needed. Instruments falling between these limits should be evaluated case by case. John Fluke Mfg. Co., Everett, Wash., is offering an explanatory application note, designated B0193, "Changing to the 1990 Volt and Ohm." Starting December 1, Fluke will use the new values for all manufacturing and calibration operations. For information on the application note or calibration services, contact the nearest Fluke office or call (800) 443-5853, ext. 554. JN

DESIGNERS GET HELP BUILDING TELECOM VLSI

Given the many telecommunications standards and interfaces, it takes a communications-system expert to develop telecomm custom chips and ensure their compatibility with existing systems and standards. Fortunately, a licensing arrangement between Microtel Pacific Research Ltd., Vancouver, Canada, and VLSI Technology Inc., San Jose, Calif., can help. The agreement gives VLSI access to Microtel's telecommunication standard-cell building blocks (Telecom System Blocks) along with the systems expertise of Microtel and its Pacific Microelectronics Center (PMC) division. Included in the library are clock- and data-recovery circuits, framers, signalling extractors, an HDLC data-link receiver or transmitter, and an inband loopback code detector, as well as many other blocks. On top of letting VLSI Technology offer system-level solutions for telecommunication applications, the deal gives PMC a manufacturing and marketing arm for standard parts, as well as custom design services through VLSI Technology.

The system blocks will be available in two forms: as a netlist that can be built into a gate array or standard cell, and as individually packaged ICs for physical breadboards. The individual ICs, called silicon verification chips, will ensure that designs meet critical performance specifications and standards before the custom circuit is built. Designers that sign up with VLSI Technology to develop a circuit also gain access to a complete set of test vectors for each block, which should help reduce the time needed to test the final circuit. DB

68000 CPU SUPERCELL POWERS LASER CONTROLLER

One of the first fruits following Toshiba Ltd.'s (Tokyo) licensing of the Motorola Corp. 68000 microprocessor is a laser-printer controller chip that employs the CPU as a large standard-cell building block. The forthcoming controller combines the CPU with control and I/O functions, including three serial ports and a baud-rate generator that can operate at up to 1 Mbit/s, three 16-bit counter-timer channels, a byte-wide parallel I/O port, an interrupt controller, and an address decoder. With the ability to operate at 16 MHz, the core processor can perform all of the routine control operations that most laser printers require, from responding to front-panel controls to controlling the mechanics along the paper path. What's more, standard development tools for the 68000 processor will help develop software and system hardware for TMP68301-based systems. DB

SCANNED-LASER SYSTEM SPEEDS MASK MAKING

Building custom chips can cause bottlenecks—not only in the design and test cycles, but also in producing the masks for the photolithographic steps of the chip fabrication. Cutting that time in half over its predecessor system, an advanced scanned-laser lithography system from Ateq Corp., Beaverton, Ore., can create reticles for 1X, 5X and 10X optical stepper systems, with feature sizes as small as 1 μ m drawn on the reticles. The system employs an enhanced rasterizing engine that moves the laser beam much faster than the previous system and, in some cases, four times faster than competing electron-beam lithography systems. An improved steering-mirror control and response system also enhances the beam movement by more quickly handling the fine positioning. Furthermore, the system's disk-storage capacity for the reticle data was boosted to over 675 Mbytes—almost double that of its predecessor. The laser system also avoids the problems and overhead imposed by electron-beam lithography systems, which require a vacuum to operate the electron gun, and are very sensitive to electrical and magnetic fields. That sensitivity means that electron-beam systems require compensation during pattern writing or if they are physically relocated. The company expects to have the Core-2100 scanned-laser system ready in the second quarter of next year. DB

ASICs COMBINE FAST, LOW-POWER CIRCUITS

ASICs built with biCMOS technology combine the high speed and high-output drive of bipolar circuits with the low power and high density of CMOS circuits. S-MOS Systems Inc., San Jose, Calif., offers a pure CMOS gate-array core cell surrounded by a ring of bipolar buffer drivers. The bipolar drivers give a 48-mA output current with two parallel I/O cells. Yet, at 15 μ W/MHz, the internal power dissipation is similar to CMOS devices. The new biCMOS series, called the SLA800B, uses a sea-of-gates architecture. All of the internal logic cells are implemented in 1.2- μ m CMOS technology, while the peripheral macrocells are built in bipolar technology. The array has 172 I/O pads and a maximum gate count of 20,064 usable gates. BiCMOS is most effectively used in applications that require heavy loads, such as interface peripherals, telecommunications, and imaging systems. LG

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Face it, flash really was a great idea. They billed it as an easy-to-use, in-system programmable memory. And, it would be priced right.

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We call our flash a programmable read-only memory (PEROM). It's easier to use because there is no pre-write erase cycle. Erase is automatic; all you do is write. Atmel's PEROM (AT29C256) executes a complete, full-chip erase/write cycle in 10 seconds and only uses less than 40 bytes of code. Theirs takes two minutes because it uses a trial and

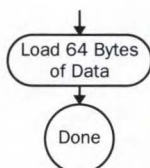
error algorithm that needs over 200 bytes of code (want to guess who has to write and debug the code?). Just look at the number of steps to run each write routine—remember theirs also requires a trial and error full erase routine.

NOW FOR THE GOOD NEWS! The Atmel PEROM fits snugly into your 5-volt system. No extras. Theirs requires a 12-volt power source. Not only is a second power source a pain, it requires up to \$8 more in circuitry per system, which in itself increases the potential for system failure.

So if you want in-system programmable memory without the hassle remember that the *real flash* is called PEROM.

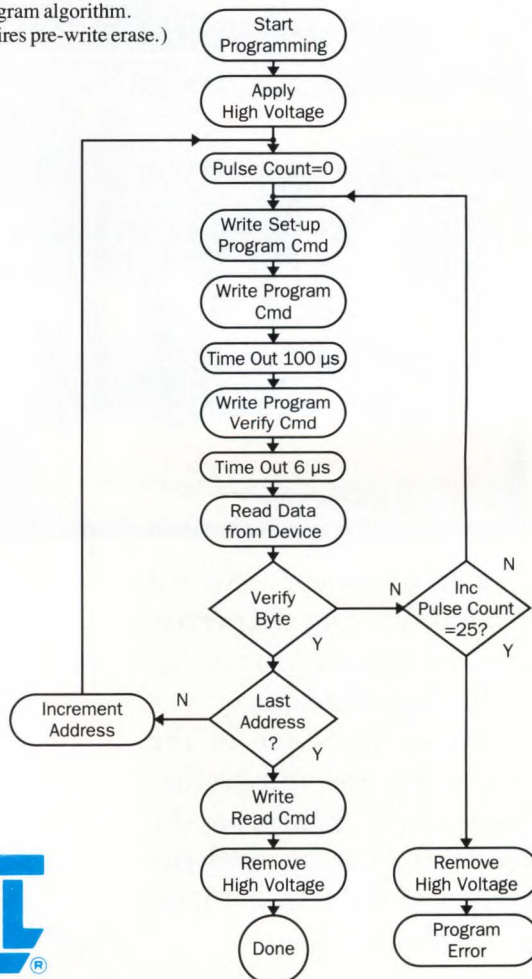
OURS

Reprogram algorithm.
(No erase required.)



THEIRS

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	KM6465	16K x 4	25/35/45ns	SDIP
	KM6465L	16K x 4	25/35/45ns	SDIP
	KM6865	8K x 8	35/45/55ns	SDIP
	KM6865L	8K x 8	35/45/55ns	SDIP
256K	KM61257	256K x 1	25/35/45ns	SDIP/SOJ
	KM61257L	256K x 1	25/35/45ns	SDIP/SOJ
	KM64257	64K x 4	25/35/45ns	SDIP/SOJ
	KM64257L	64K x 4	25/35/45ns	SDIP/SOJ
	KM68257P	32K x 8	35/45/55ns	DIP
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DDC's newest Microcomputer SEM E card, the BUS-67007, provides a general purpose, single chip, 16 bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support conforming to the MIL-STD-1750A instruction set architecture. The Performance (Pace 1750A) CMOS microprocessor and onboard 32K words of EPROM offers an embedded system controller that can be used as a generic 1750A processor with a BUS-61555, full intelligent dual redundant MIL-STD-1553B Remote Terminal (RTU), Bus Controller (BC), and Monitor (MT). Its RS-422 port facilitates software development and system integration.

The BUS-67007 is packaged on a standard SEM E card with a 150

pin connector. Its on-board 8K x 16 SRAM supports the 1750A CPU. The separate internal 8K x 16 dual access shared RAM of the BUS-61555 AIM-HY supports the 1553B messages, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The AIM-HY off-loads the microprocessor from the 1553 communication protocol tasks and offers the host additional RAM for program or data.

Equipped with 8 L.E.D.'s, the card gives visual BIT feedback as to the CPU self-test (green), unrecoverable errors (red), software errors (red), RS-422 status (green), EPROM status (green), SRAM status (green), 1553 terminal self-test status (green), and the CPU watch-dog timer status (green); which can be changed by software

for other future meanings. The BUS-67007, requires only 5 volt DC power, with a total power dissipation under 5 watts.

The Microcircuit, Digital, CMOS, 16-BIT MIL-STD-1750A MICROPROCESSOR, is on DESC drawing #5962-87665-01XC. The PACE 1750A CPU are also available in CMOS/SOS technology for radiation environment applications, in production by 1990. DDC's AIM-HY, BUS-61555 Terminal is on DESC drawing #5962-88692-01XC. The BI-POLAR & CMOS-SOS technology used is available to support tactical and strategic environments.

For additional information on the BUS-67007, contact Steve Friedman at toll-free 1-800-DDC-1772 (outside New York) or call the DDC office nearest you. □

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TINY DISPLACEMENT BOOSTS RESOLUTION OF CHARGE-COUPLED DEVICE

By using a simple and ingenious trick, a researcher at the University of Munich, West Germany, has raised charge-coupled-device (CCD) camera technology to a new plateau. The gimmick increases the resolution well beyond present limits, advancing it to a level that rivals a high-quality 35-mm-format color negative or slide.

Reimar Lenz, a professor at the Institute for Communications Technology, developed the color camera whose CCD sensor chip offers a maximum resolution of 2994-by-2320 picture elements, or pixels, in an 8.5-mm-by-6.4-mm image field. That comes to about 7 million pixels per color channel, or nearly 21 million pixels for the camera's red, green, and blue channels.

This sets the record for a 2D array sensor. According to Lenz, the maximum resolution until now stood at 2048 by 2048 pixels. That was for an 18.4-mm-by-18.4-mm monochrome sensor, which Kodak, Rochester, N.Y., showed at this spring's Hanover Fair in West Germany.

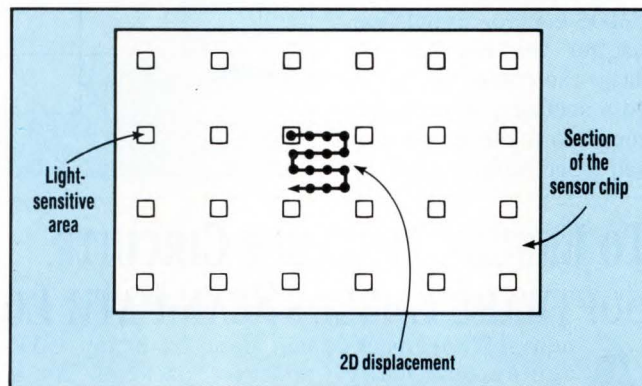
The tactic employed by Lenz to crank up the resolution is indeed simple: Instead of increasing the number of light detectors on the CCD sensor chip, the resolution is stepped up by mechanically moving the chip in the image plane horizontally and vertically in tiny increments.

This motion continually puts the detectors in new positions relative to the object. Consequently, inter-

mediate images are taken, which are then interleaved to raise the overall resolution.

Typically, a CCD sensor's resolution is increased by raising the chip's level of integration, but this has become more expensive as the limits of semiconductor technology are approached.

The CCD sensor chip in the Lenz camera has a basic resolution of 499 by 580, or nearly 300,000 pixels. In contrast to other sensor chips, the sensor is laid out so that the light-sensitive areas (the detector apertures) take relatively little space (*see the figure*).



According to the chip-displacement principle, the sensor moves two-dimensionally in incremental steps after the first image is taken.

Each step amounts to a fraction of the spacing between detectors. As a result the sensor produces a new image at each step. These intermediate images are interleaved to bring up the resolution.

The sensor movement is produced by small piezopositioning elements attached to the sensor. Voltages applied to these ele-

ments cause them to expand and contract, which in turn displaces the sensor in a procedure called piezo-controlled aperture displacement. The sensor can move over a maximum distance of 50 μm . The displacement accuracy is $\pm 0.2 \mu\text{m}$, and the displacement speed is one second for 12 different sensor positions.

In principle, the number of intermediate images—and thus the obtainable resolution—can be raised beyond 7 million pixels per color channel. However, a practical limit is reached when the pixels start overlapping each other by more

than 50% because they no longer yield any useful information.

Some information gain can be achieved by decreasing the detector aperture size, but that would have to be done at the cost of lower the sensitivity.

The images are read out individually in 40 ms, then digitized to 8-bit resolution per color channel at a 10-MHz scan rate, and finally stored in a host computer that can be connected to the camera.

Because of the large amount of data involved,

this process takes time: 8 seconds for 28 Mbytes of data at maximum resolution. Consequently, with such a long processing time, the camera is unsuitable for taking moving pictures. Instead, the camera's applications are limited to still photography, particularly for taking high-quality pictures such as those for color ads or documentation.

A convenient feature of the sensor is its programmable resolution, which can be set from 499 by 580 pixels in steps up to the maximum of 2994 by 2320 pixels. A reproduction from a color laser printer on letter-sized paper yields 10 pixels/mm, which makes the camera comparable to the resolution for high-quality photographic prints.

Because the images can be stored as digital signals, large electronic tape-based archives can be built up. As a result, access times are much shorter than for pictures stored in their physical form.

Another advantage of digital storage is that, in contrast to photos that are printed on paper, digitized pictures don't deteriorate with time. The almost limitless quality is beneficial in archiving the images of works of art.

It's also useful in medical applications for long-term storage of, for example, images of bodily details. Because of the 2D-array sensor's inherently high geometrical accuracy, applications in photogrammetry (using photographs to make accurate measurements) and quality control in machine vision are also possible.

JOHN GOSCH

FLASH EEPROM TAKES CHANGES IN PLACE BY CUTTING PROGRAMMING SIGNAL TO 5 V

The highest density in flash nonvolatile memories is achieved with cell structures that need only one transistor per cell. Programming such chips typically takes about 12 V—considerably higher than the 5-V logic signals coursing around the surrounding circuitry. But by shifting to a two-transistor per cell structure, designers at Atmel Corp., San Jose, Calif., have created a circuit structure programs at 5-V levels. Consequently, it becomes easier to reprogram the memory in situ. The company plans to incorporate the double transistor cells in a family of programmable and erasable memories starting with 256-kbit and 1-Mbit versions.

Though the double-transistor cell occupies more area, it also eliminates the need for trial-and-error high-voltage programming. One of the two transistors isolates the particular cell being programmed from all the other cells, so on-chip circuits can generate the necessary signals and voltages from an external 5-V supply (see the figure).

With the ability to withstand 1000 erase cycles, the cells can also retain data for a minimum of 10 years, as do standard EEPROMs. However, by requiring just one 5-V power supply, the chip can be reprogrammed in the system. And, unlike other flash EEPROMs, which must be rewritten entirely to change any data, the dual-transistor memory

chip can rewrite data a 64-byte page at a time.

Only 10 ms is needed to write a page of data, thanks in part to an on-chip 64-byte page register that captures the data from the host system at a rate of 150 ns/byte, and then transfers it in parallel to the non-volatile storage elements. This control sequence also simplifies the algorithm that the host system must execute to store data in the memory. Further, the chip doesn't have to be erased before new data is written. Instead, all of the house-keeping is taken care of by internal circuits.

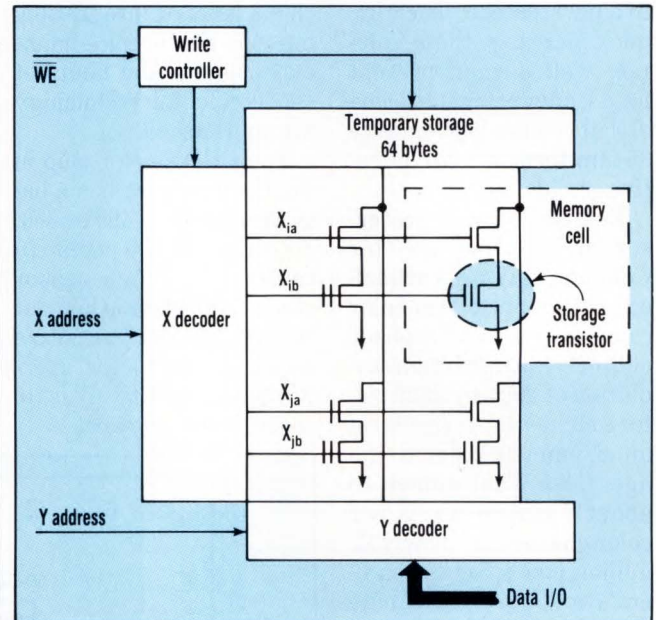
Because common TTL or CMOS control signals can trigger the rewriting of data, the company included a security scheme that requires a three-byte key sequence before data can

be written, and a six-byte software code must be loaded into the chip to "unlock" it before erasing all its data.

For added protection,

the chip has a 5-ms Write-Inhibit control, which locks out all write signals until the power-supply voltage has stabilized. It also has glitch filters on the Write Enable and Chip Enable lines that block signals shorter than 15 ns.

DAVE BURSKY



TO ENSURE TESTABLE CIRCUITS, SOFTWARE EMBEDS SCAN-PATH LOGIC

A new software package automatically generates test vectors for a circuit by first inserting scan-path logic into the design. Developed by Gould AMI, Pocatello, Idaho, the NetScan program ensures that designs can be thoroughly tested. What's more, as gate count goes up, NetScan's run time increases more or less linearly with the gate count, rather than exponentially as with other test generators. The result is less design overhead.

The tool's maker claims that it's the first fully automated ASIC test-pattern generator to work with cir-

cuit data from any CAE software package. As a batch-run program, NetScan would typically be used with the company's NetTrans universal net-list translator.

NetScan takes about 30 minutes for every 1000 logic gates to produce enough test patterns to reveal 95% of all possible faults, according to Robert Kirk, Gould's CAE research manager. Based on scan-path techniques, the software automatically inserts scan cells at every node that needs them, or converts existing registers or latches into scan cells.

To develop test patterns,

the software combines scan-path design techniques with an older algorithm called the D-algorithm, a model-based test-generation program.

The D-algorithm applies the single-stuck-line (SSL) fault model, which makes the following assumptions: there is at most one fault, and any physical fault causes a stuck-at behavior at the fault site (in other words, it's behavior doesn't change during the test).

Using the algorithm, the program generates a test vector for each potential SSL fault in a combinatorial circuit. This is done by

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repeatedly inserting faults, and then generating a vector that distinguishes between faulty and fault-free behavior in the circuit.

When testing a chip, faulty gates are found by applying the generated vectors to the chip's inputs and comparing its outputs to the expected result. Though the vectors don't guarantee a correct design, they do determine if the chip has manufacturing defects.

The D-algorithm works for sequential circuits too, but NetScan doesn't use it that way because analysis time increases in proportion to the cube of the number of logic gates. Instead, by modifying the D-algorithm and imposing a time limit (set by the user), within which it must generate tests for sequential circuits, the software's execution time can be roughly controlled. If the program exhausts its time limit, then the user can modify the circuit to help the test program generate a test.

To avoid long analysis times and complex user interaction, Gould limited the D-algorithm portion of NetScan to only generate tests for combinatorial logic. Once the program analyzes the combinatorial logic it inserts a scan path into the circuitry.

Thus, sections of the combinatorial logic can be isolated and surrounded by scan elements. Vectors are shifted into the subdivisions through a scan-path input. Similarly output vectors are shifted out from each block to a scan-path output pin.

In most cases, NetScan doesn't have to insert new memory elements into the

circuit to create a scan path. Rather, the software converts the existing latches and flip-flops into scanable elements. Then NetScan computes the ordering of the elements in the scan path to avoid creating any reconvergent fanout in the scan path, which might make the path

untestable. A modified netlist is then generated. After inserting the scan-path logic, NetScan has the D-algorithm generate the test vectors.

To minimize circuit complexity, Gould's designers incorporated another trick: Special latch and flip-flop models were created for

the D-algorithm so that they can be treated as combinatorial elements rather than sequential ones. Consequently, the D-algorithm can treat the entire circuit as combinatorial logic and generate the tests in a matter of hours, rather than days.

DAVE BURSKY

TIGHT HEAD TRACKING, DSP ANALYSIS HELPS 8-IN. DRIVE PACK 2.5 GBYTES

To improve the storage capacity of 8-in. disk drives and achieve a capacity of 2.5 Gbytes (unformatted)—the highest to date for a drive this size—engineers at Seagate Corp.'s Imprimis subsidiary, Minnetonka, Minn. have developed improved schemes for controlling and positioning the heads. For starters they designed a disk-control scheme that combines an intelligent, continuously self-calibrating servo system to maximize seek performance. Furthermore, a closed-loop micropositioning system was devised to continuously correct for long-term changes in the head position.

According to Rady Thibodeau, engineering manager for the Saber 2500 drive, such control techniques are required to pack tracks at nearly 1900/in. across 19 of the drive's 22 platter surfaces.

Though 10 disks could do the job, Thibodeau's team decided to use 11 and sacrifice the outer surfaces, in other words the top and bottom of the platter stack. Sacrificing the outer surfaces simplified the head assembly design, explains Thibodeau, because the aerodynamics of the two

outer surfaces are trickier to design for than on the inner platter regions. To help squeeze 11 platters into the 8-in. format, the design team came up with thin-film read-write heads that are small and light.

Furthermore, the reduced mass and improved aerodynamic design of the heads makes it possible for them to track the disk surface better. They can also seek data faster than heavier heads because of their low inertia. In fact, the drive boasts one of the shortest seek times for an 8-in. format unit: just 13 ms on average and no more than 26 ms. A balanced actuator abets the fast seek time. Moreover, the drive can operate in any position because the actuator doesn't require a particular mounting orientation.

In the continuously self-calibrating servo system, an embedded digital-signal processor continually monitors the servo system and corrects it if there are any changes. The intelligence of the servo system extends to a servo-encoding technique that reads the binary (absolute) address of each track as the servo head passes over it. As a result, the head gives the system absolute position feed-

back, and the drive can correct itself if the destination track were somehow missed during a seek.

The other circuit that's central to the drive's data integrity is the micropositioning control scheme. This closed-loop subsystem corrects any long-term changes in the position of the data head with respect to previously written data. To ensure proper positioning, a small heater mounted on the arm of the read-write heads is activated during startup by a position-control signal. As the metal arm warms slightly, the arm's position changes a tiny amount until the detected signal's strength is highest. The small position change keeps the heads centered on the data tracks, ensuring peak signal strength.

Lastly, a test verifies the heads' flying integrity when assembly is complete to ensure that the drive's many assembly steps don't produce surface flaws on the platters. The proprietary scheme performs electrical tests using the assembled drive's own data heads to search for and detect any disturbances in the head-disk interface.

DAVE BURSKY

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

ASICs – Choice not compromise

IN THE ERA OF

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The TI Action Logic System (TI-ALS) is a powerful development tool for implementing your FPGA designs while avoiding NRE fees. The TI-ALS accepts designs from popular CAE software packages including Viewlogic™, OrCAD™, Mentor Graphics™, and Valid™ — resident on PC386, Apollo™, and Sun-3™ platforms.

Gate arrays for greater differentiation

For applications requiring higher-density, high-performance ASICs with fast prototype delivery, TI's TGC100 Series 1-micron gate arrays are an excellent choice. Offering gate-array complexities up to 26K gates and 256 I/Os, the TGC100 Series utilizes familiar general-purpose logic libraries. You can define macros and pinouts, as well as specify packages with pin counts up to 256 pins.

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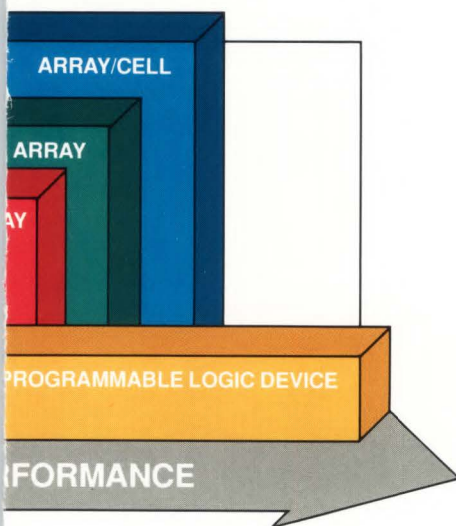
“I need a high-speed part with unique functionality. Standard architecture is a big priority, too. Plus, I'm going into production and need volume delivery now.”

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For details about the support and service TI offers, please turn the page.

At TI, we cover your ASIC needs from silicon to software to service and support.

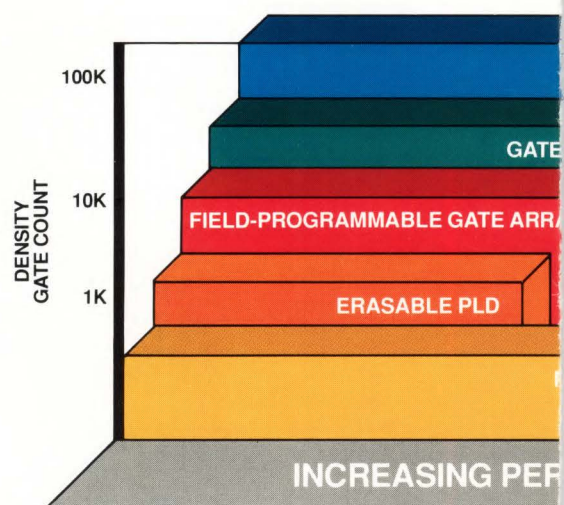
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“An ASIC solution also brings with it assurances of the supplier’s dependability, stability, and capability to produce and deliver.

“At TI, we invite you to experience the difference between compromise and choice — the difference between an ASIC device and an ASIC solution.”



Walden C. Rhines, Ph.D.
Executive Vice President, Semiconductor Group
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“On my schedule, delivery delays and unnecessary risks are out. Our design requires the density of a gate array, but we need to handle all the programming ourselves.”

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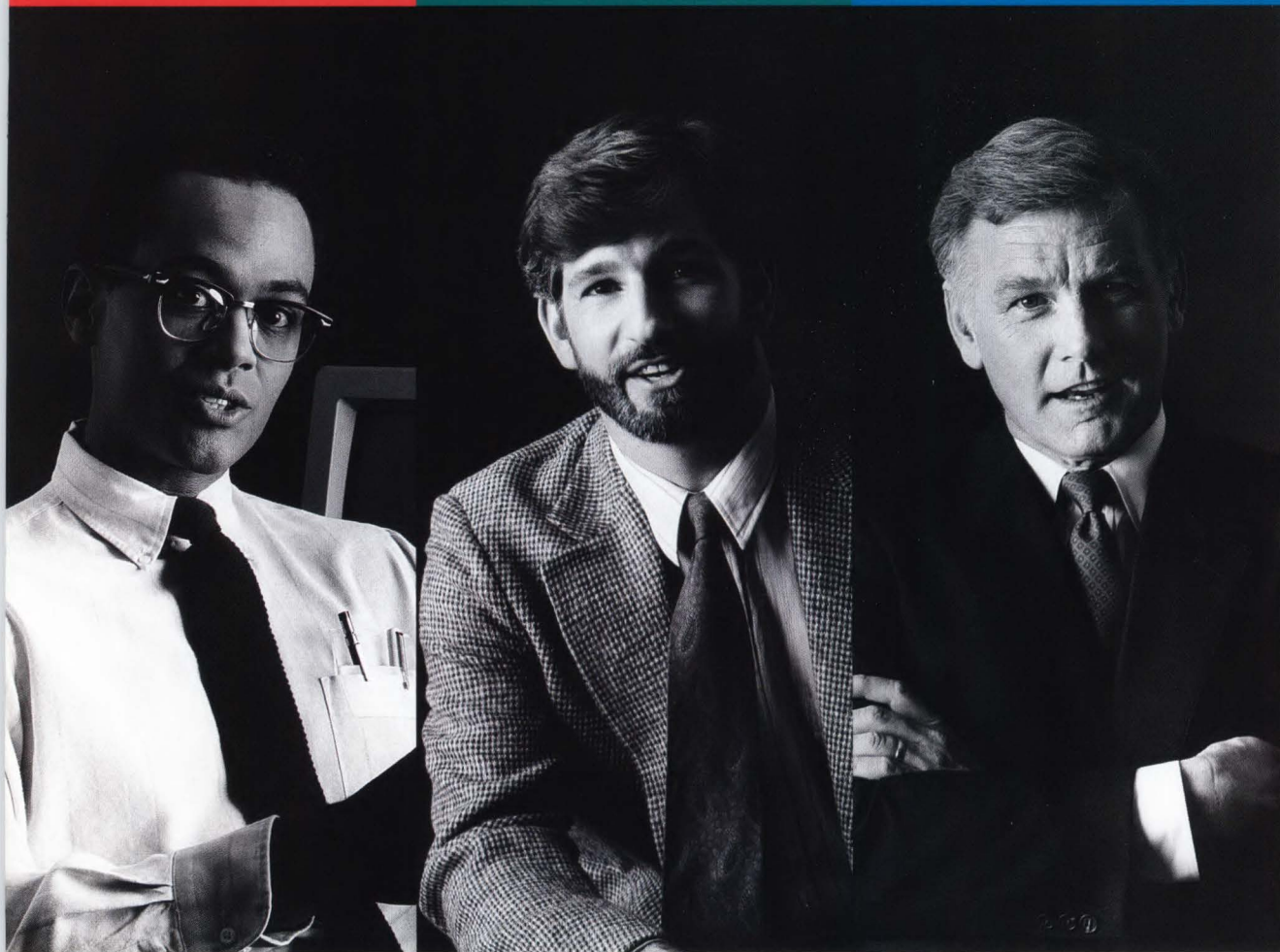
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The TI Solution:

Gate Arrays

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Our design flow is straightforward and minimizes the possibility of surprises.

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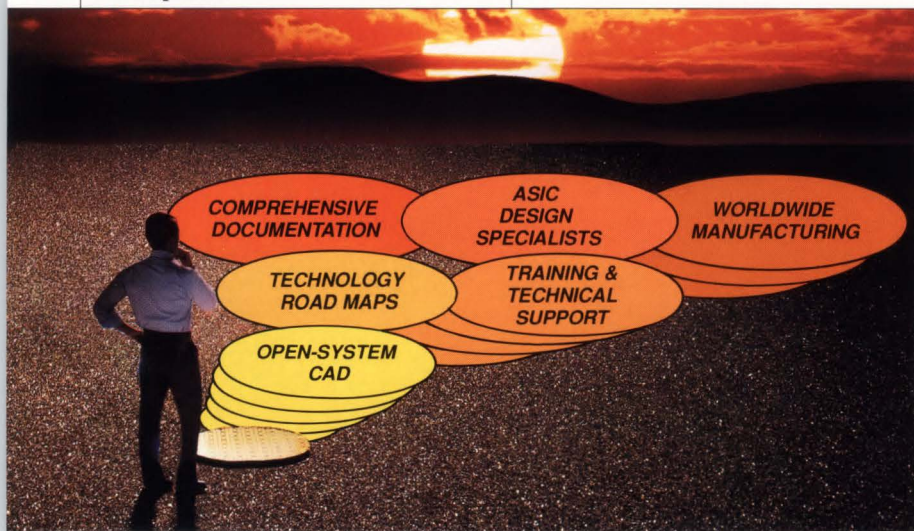
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COMDEX/FALL '89: A SHOWPLACE FOR SEMICONDUCTORS?

AT THIS YEAR'S SHOW, THE BIG NEWS IS ICs, NOT PCs.

RICHARD NASS

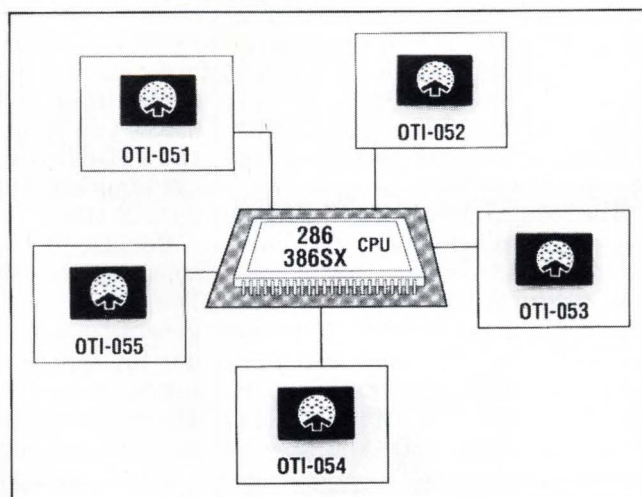
Historically, semiconductor companies haven't made much of a showing at Comdex. The show has traditionally been a place for computer and peripheral manufacturers to strut their stuff. But this year's Comdex will show a trend toward semiconductor announcements, due in part to systems-oriented semiconductor companies doing a large percentage of the overall computer design in IC integration. Hence, rather than do designs themselves from scratch, customers are getting a more complete solution. Fall Comdex, to be held in Las Vegas, November 13-17, will set the table for announcements of PC chip sets, video chips, disk and cache controllers, power-management units, and math co-processors.

It's easy to see the catalysts that are turning a show like Comdex into a showcase for semiconductors: Because the people that design with the chips will attend, it's wise for semiconductor makers to show them what's available. Furthermore, no single show hosts as many semiconductor manufacturers. But for the most part, attendees at Comdex won't be at the true semiconductor shows. More over, as one marketing manager put it, "if just one of our competitors is there, we have to be there."

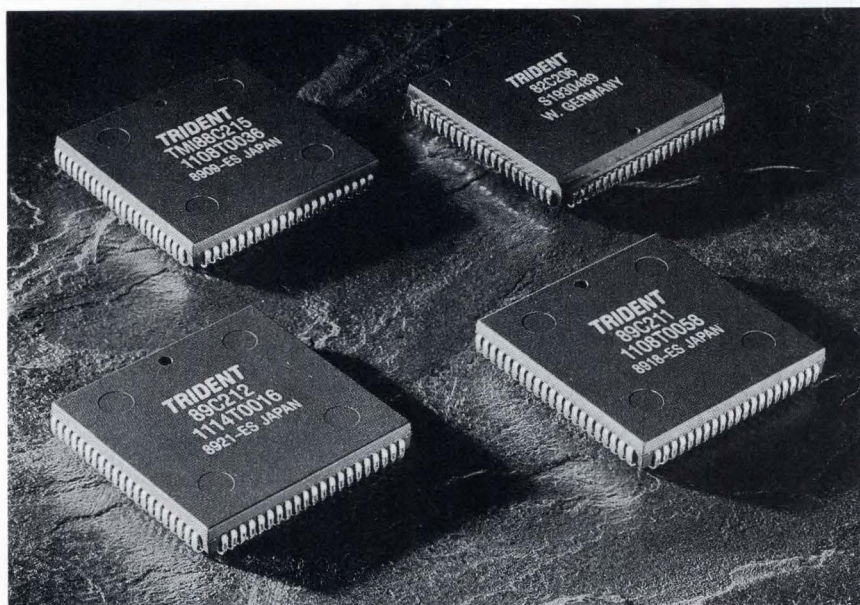
In addition to the semiconductor an-

nouncements and the many seminars, presentations, and discussions, over 1700 domestic and international exhibitors will be on hand to display their products. These products include hardware, software, CAD/CAM products, peripherals, communications devices, desktop-publishing and graphics software, computer furniture, and more. The show will be attended by value-added resellers, retailers, and both hardware and software developers.

Technical sessions will focus on computer industry trends. For instance, where will the next generation of de-



1. THE OAKHORIZON pc chip set supplies all of the necessary system-support circuitry for a 286- or 386-based laptop. The chip set's low power consumption makes it compatible for laptops.



2. TRIDENT'S BEAT CHIP SET supports a 286-based system and maintains complete compatibility with the original IBM PC AT bus specification.

signers take us? Many business-oriented sessions will deal with buyer and seller demographics, and how to get the most out of your computer system.

But there's no question that the semiconductor companies are trying their best to make an impact at Comdex. For instance, VLSI Technology Inc. has introduced 80286- and 80386-compatible chip sets. The two-chip VL82C286 is intended for 286 and 386SX systems at clock speeds of 25 MHz and below, and with peripheral bus speeds up to 12 MHz. The three-chip VL82C386 is for 386-based systems running at clock speeds 33 MHz and below, and with peripheral bus speeds up to 16 MHz.

The 286 set consists of a VL82C320 system controller data buffer, and a VL82C331 ISA (industry-standard architecture) bus controller. The VL82C386 is made up of a system controller, an ISA bus controller, and a data buffer. Both sets support 256-kbit, and 1- and 4-Mbit DRAMs. A built-in sleep mode and power-down control are both useful in laptop computers and other low-power applications, and three-state control pins are added to simplify board-level testing.

All of the devices are packaged in plastic quad flatpacks. Samples of

the VL82C386 are available now for \$185. Volume quantities (of 1000) will be available in March, 1990 for \$95. The VL82C286 will be available in sample quantities in December for \$160 and volume quantities in May, 1990 for \$80.

Oak Technologies will introduce a low-power CMOS chip set aimed at 286- and 386-based laptop computers. The OakHorizon set consists of five ICs that control system control logic, clock circuits, serial and parallel peripheral controllers, DMA and memory controllers, and address and data buffers (Fig. 1). By adding a 286 or 386SX CPU chip, memory, and just two TTL devices, a complete system can be up and running at clock rates up to 20 MHz.

Because of their low power consumption, the chip set suits diskless PCs, which need to minimize heat generation. Logic is included to monitor the activity of the system and turn it on or off at appropriate times. The set is available now for \$90 in quantities of 1000.

PC AT 386 and 386SX chip sets are also available from Headland Technology. The 386SX is a three-chip set that requires only three external TTL devices, a real-time clock, a keyboard controller, a CPU, and memory. The bottom line is that little needs

to be added to this chip set to complete the system. The set features bi-modal operation and supports clock speeds up to 16 MHz.

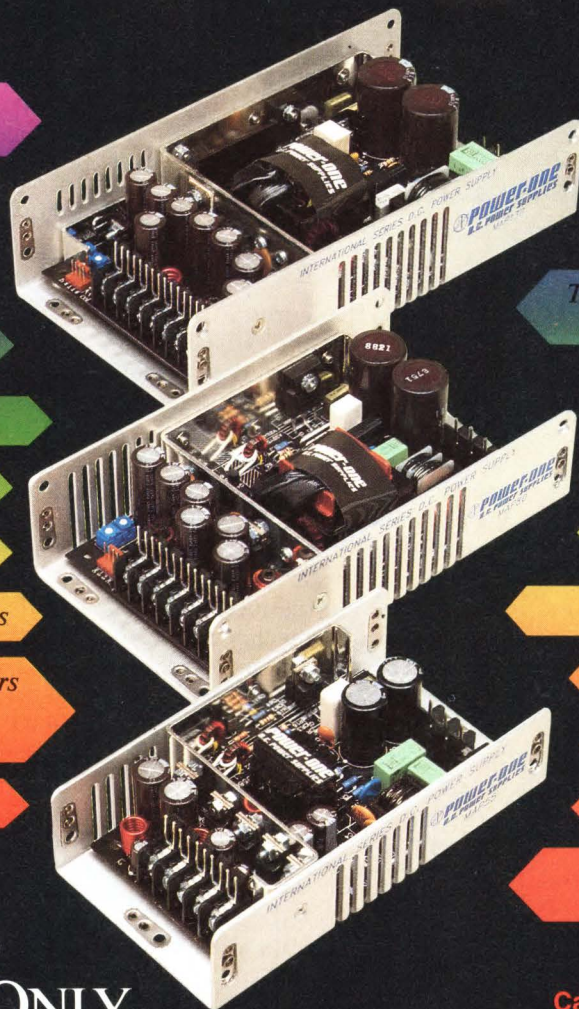
The 386 set from Headland is also comprised of three chips, but runs at speeds up to 33 MHz and supports 80287 and 80387 numeric coprocessors. The set's best feature is its flexibility: Some manufacturers force users to manipulate hardware switches to alter their system's configuration, but Headland implemented a different configuration and makes it possible for manufacturers to program an EEPROM chip, or for software to alter or optimize a system configuration of memory chips and peripheral devices. Both the 386 and 386SX sets are available now.

A four-chip set from Trident Microsystems Inc., designated the BEAT (best enhanced AT), supports a 286 system while the BEATsx is a similar set for 386 systems (Fig. 2). Both chip sets maintain complete compatibility with the original IBM PC AT bus specification. In addition, both are optimized for OS/2 operation. The two sets are pin-for-pin compatible with Chips & Technologies' NEAT and NEATsx chip sets and can be used as direct replacements for those sets on an existing motherboard.

The BEAT sets have a marked improvement in memory speed over similar chip sets. Trident's design includes an enhanced data-bus structure that supplies a direct link from dynamic RAM to the CPU. With programmable command delays and wait states, OEMs can select timing and system speeds of 12, 16, or 20 MHz. Other features include a two- or four-way page-interleaved memory control, and software-configurable memory organization.

Also from Trident is a graphics chip that combines the functions of the IBM 8514/A with the VGA standards, using the specifications from Trident's TVGA 8800 graphics controller. The TAVA 9000 is a single-chip solution that's compatible with the 8514/A specifications as well as with all previous graphics standards, including EGA, CGA, MDA, and Hercules. The TAVA 9000 will be

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MAP55-4002		5V @ 6A	12V @ 3A/4A PK	12V @ 1A	-12V @ 1A
MAP80-4000	80W/110W PK	5V @ 14A	12V @ 4A/7A PK	-12V @ 1A	-5V @ 1A
MAP80-4001		5V @ 14A	12V @ 1A	-12V @ 1A	24V @ 2A
MAP80-4002		5V @ 14A	12V @ 4A/7A PK	12V @ 1A	-12V @ 1A
MAP130-4000	130W/165W PK	5V @ 20A	12V @ 5A/8A PK	-12V @ 1A	-5V @ 1A
MAP130-4001		5V @ 20A	12V @ 1A	-12V @ 1A	24V @ 3.5A
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COMDEX PREVIEW

SOME COMDEX SEMICONDUCTOR VENDORS

Austek Microsystems Inc.
Santa Clara, Calif.
(408) 988-8556
CIRCLE 451

Cirrus Logic Inc.
Milpitas, Calif.
(408) 945-8300
CIRCLE 452

Headland Technology Inc.
Fremont, Calif.
(415) 656-7800
CIRCLE 453

Oak Technology Inc.
Sunnyvale, Calif.
(408) 737-0888
CIRCLE 454

Trident Microsystems Inc.
Sunnyvale, Calif.
(408) 738-3194
CIRCLE 455

VIA Technologies Inc.
Fremont, Calif.
(415) 651-2796
CIRCLE 456

VLSI Technology Inc.
Tempe, Ariz.
(602) 752-8574
CIRCLE 457

Weitek Corp.
Sunnyvale, Calif.
(408) 738-8400
CIRCLE 458

Zymos Corp.
Sunnyvale, Calif.
(408) 730-5400
CIRCLE 459

available in the second quarter of 1990, either as a single chip or configured on a board.

Another VGA graphics chip, the Poach 52 from Zymos Corp., offers complete compatibility with VGA, EGA, CGA, and Hercules standards. It's housed in one chip and requires little support logic. Two logic devices that are typically required were incorporated into the single package. Because of the low component count, the Poach 52 becomes a cost-effective alternative to VGA systems.

Designed for IBM PC XT, PC AT, PS/2, and compatible computers, the chip supports many super-VGA modes, including 1024 by 768 pixels with 16 colors, or 800 by 600 pixels with 256 colors—both from a palette of 256,000 colors. It contains an internal 512-kbit memory decoder, an automonitor detector, and a 50-MHz pixel clock. The chip supports either 1-Mbit (256-kbit by 4) or 256-kbit (64-kbit by 4) DRAMs. To maintain compatibility with future high-end workstations, it includes an interface to Texas Instruments' 34010 and 34020 graphics processors.

Packaged in a 100-pin Jedec quad flatpack, Poach 52 sells for \$47 in 100-piece quantities. Samples are available immediately and production quantities will be available in the first quarter of 1990.

A single-chip disk controller, from Cirrus Logic Inc., combines a flexible architecture with synchronous/asynchronous SCSI protocols. The CL-SH350 integrated SCSI disk controller lets a 3.5-in. drive incorporate the performance and functionality of a 5.25-in. drive. These capabilities are required in intelligent disk drives for smaller, next-generation Unix work-

stations and file servers.

The low-power device incorporates extensive hardware support for the SCSI bus, a high-speed microcontroller interface, a powerful buffer manager, and a high-performance sector formatter. The speed-matching capabilities of the SCSI bus interface make possible up to 15-byte synchronous-transfer offsets and 12 programmable-transfer periods. Also integrated on-chip are 48-mA SCSI bus drivers. Control signals for external differential drivers are supplied. The disk controller can interface directly with high-speed microcontrollers. Samples are available now for \$42.

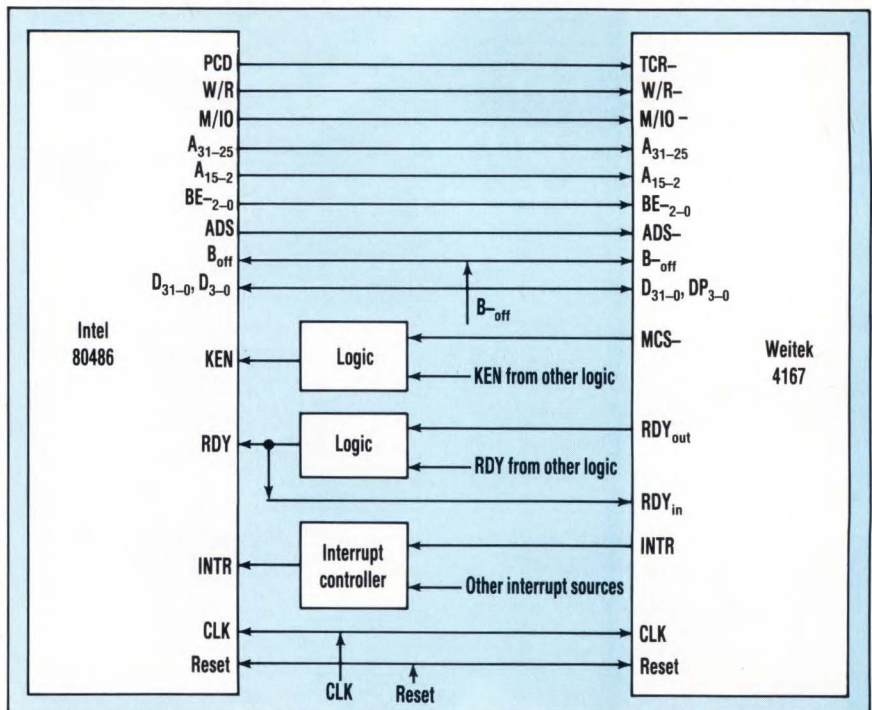
Used with any Intel microproces-

sor-based design (286, 386SX, 386DX, and 486), the SL9095 power-management unit (PMU) minimizes power consumption and maximizes battery life in laptop computers. This single CMOS chip from VIA Technologies Inc. is compatible with all CPU clock rates from 8 to 33 MHz. The PMU supports three modes of operation: sleep, auto power-off, and suspend-resume. As an option, slow-refresh DRAMs can further reduce power during power-down modes.

ASLEEP ON THE JOB

The chip enters the sleep mode if an interrupt doesn't occur within the user-selectable time frame. In this mode, the real-time clock interrupt is blocked, the CPU is halted, and the microprocessor and system-controller clock are stopped. Power is also turned off for the address, memory, and data controllers, the EEPROM, display, and SCSI hard-disk controller. Following a keyboard entry, power is turned back on and the PMU refreshes the memory.

The PMU supplies a programmable time-out counter that monitors the activity of a high-powered device. Its auto-power-off mode will



3. A FEW SIMPLE CONNECTIONS to the 142-pin grid array connect the Abacus 4167 math coprocessor to the 80486 microprocessor.



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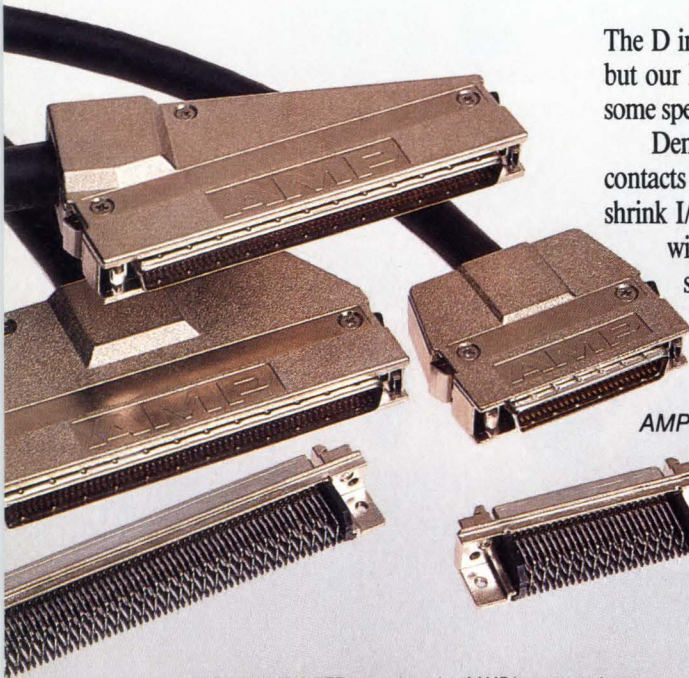
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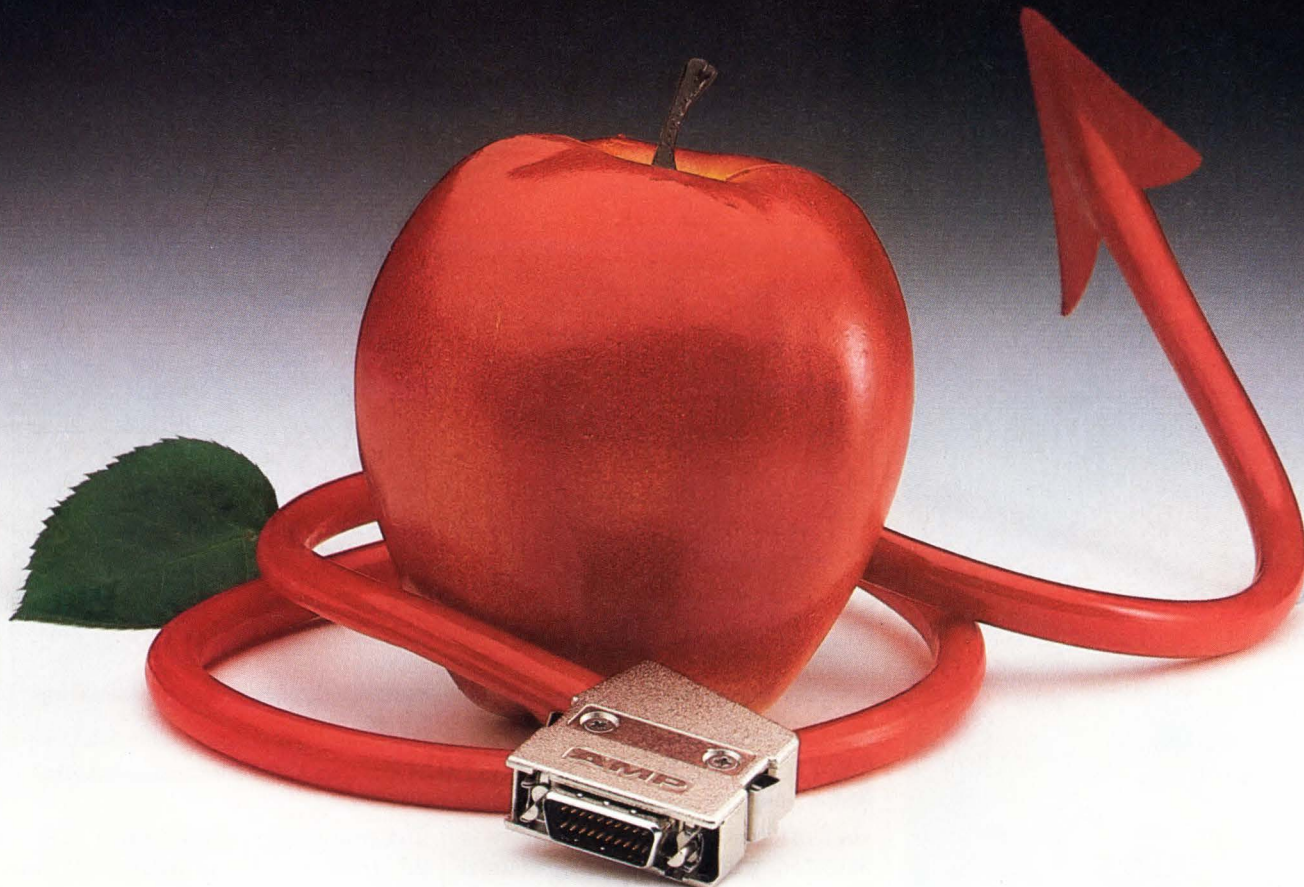
AMPLIMITE .050 Series 50 and 68 position connectors were recently selected as the Small Computer Systems Interface (SCSI). The X3T9.2 Standards Committee anticipates approval as an ANSI standard in 1989.

layout frees up more board, too, but still leaves trace routing uncomplicated.

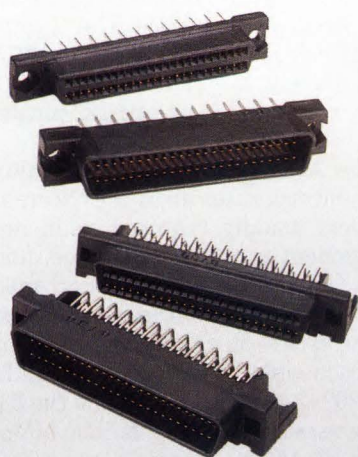
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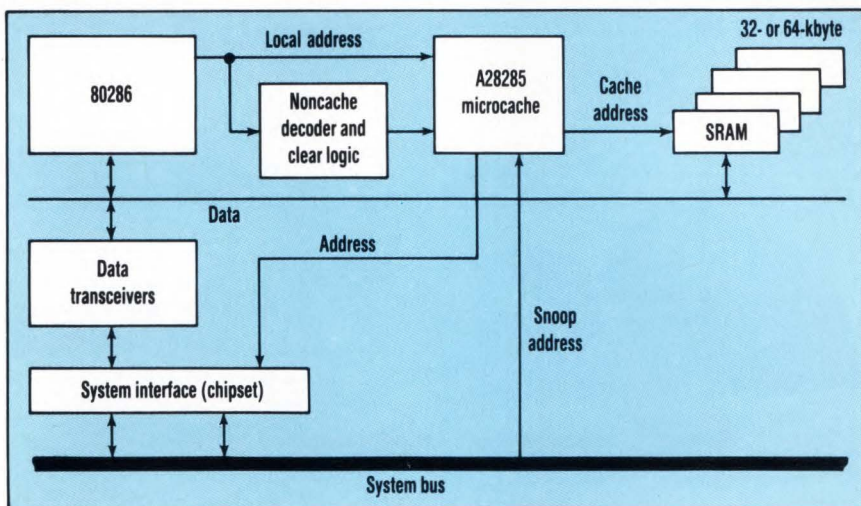
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CIRCLE 52

COMDEX PREVIEW



4. THE A28285 CACHE CONTROLLER from Austek Microsystems links the 80286 microprocessor and a 32- or 64-kbyte static RAM.

shut off the device if no activity is detected within a preprogrammed time interval. With the suspend-resume mode, users can shut the system down (suspend) and return to the same point they left (resume).

The latest version of Weitek Corp.'s Abacus 4167 math coprocessor is designed to work with Intel's 80486 microprocessor and is upwardly compatible with the Abacus 3167. It runs numerically-intensive scientific and engineering application programs two to three times faster than systems running the 486 alone. A 486-based PC running at 25 MHz will deliver 17 MWhetstones of single-precision numerics performance, compared with 7 MWhetstones delivered by the lone 486.

Delivering RISC-level performance, the chip plugs into a socket on the system board of a 486-based computer and installs with just a few simple connections (Fig. 3). A 142-pin grid array designed onto the system board supplies all of the signals needed to interface the processor. Because the chip is memory mapped, it appears to the CPU as a block of system memory. For this reason, most of the signals from the coprocessor are connected to the 486's address and data buses.

All existing applications that support the Abacus 3167 for 386-based PCs automatically support the new chip. In quantities of 1000, the Abacus 4167 will sell for \$565. It is avail-

able now in sample quantities. Limited production quantities will be available in December.

Austek Microsystems has released two high-performance cache controllers: the A28285 for 286-based systems and the A38202 for 386-based systems. Both feature 32- or 64-kbyte caches, while the A38202 extends to 128 kbytes. The A28285 supplies a direct interface to either an 80286 microprocessor or to a PC AT286 chip set, as well as to by-4, by-8, and by-16 SRAMs (Fig. 4). Running at 25 MHz, the cost-effective chip offers performance comparable to a 386 25-MHz system. The 20- and 25-MHz versions sell for \$51 and \$57, respectively, in quantities of 10,000. They're housed in plastic 132-pin Jedd packages.

The A38202, a second-generation part, incorporates all of the external support usually required, reducing component count, board space, and cost. It can operate at either 25 or 33 MHz in multiple configurations, and features an on-chip declaration of noncacheable regions. The 25-MHz A38202 is priced at \$84, while the 33-MHz version costs \$98, both in quantities of 10,000. Production quantities are available now.

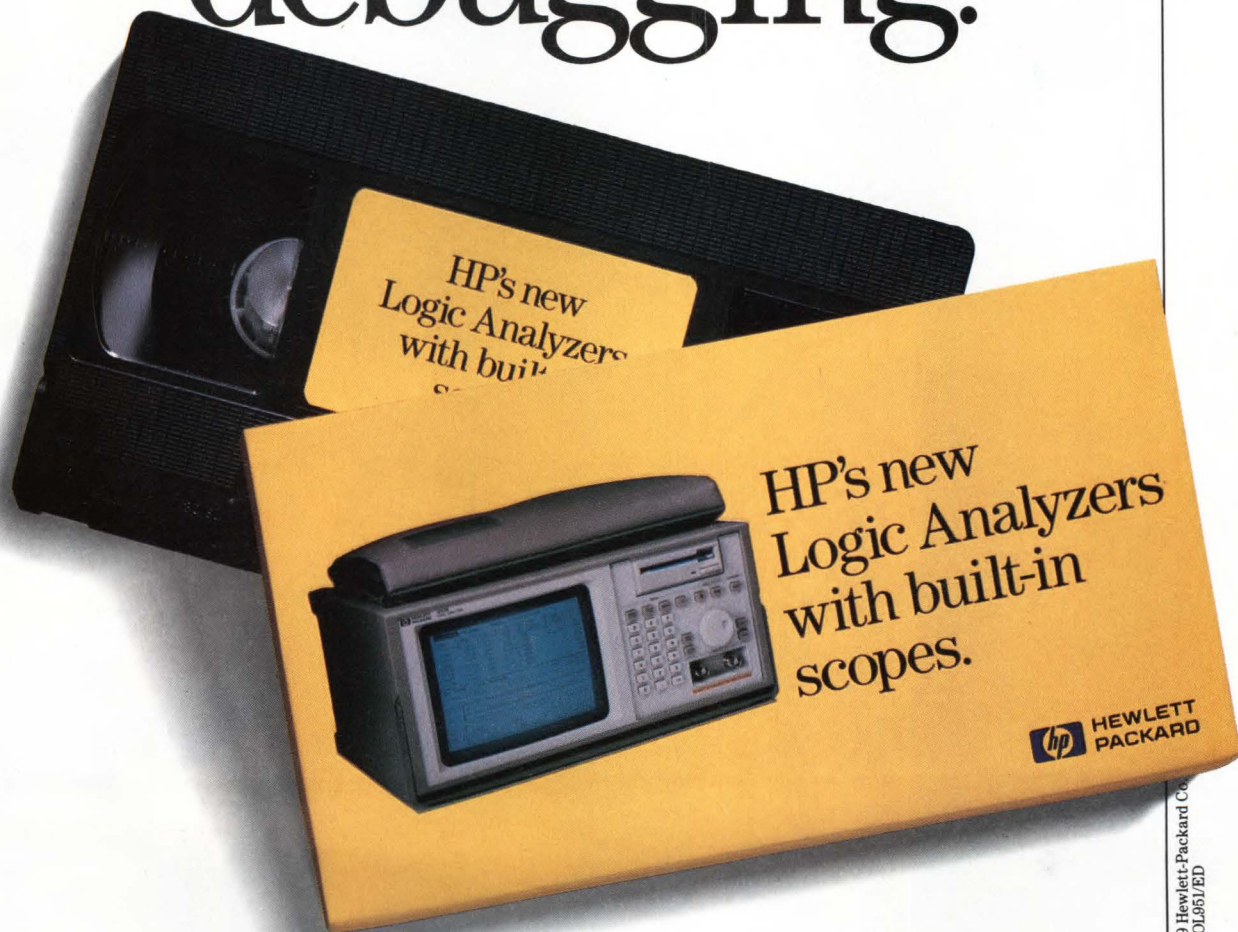
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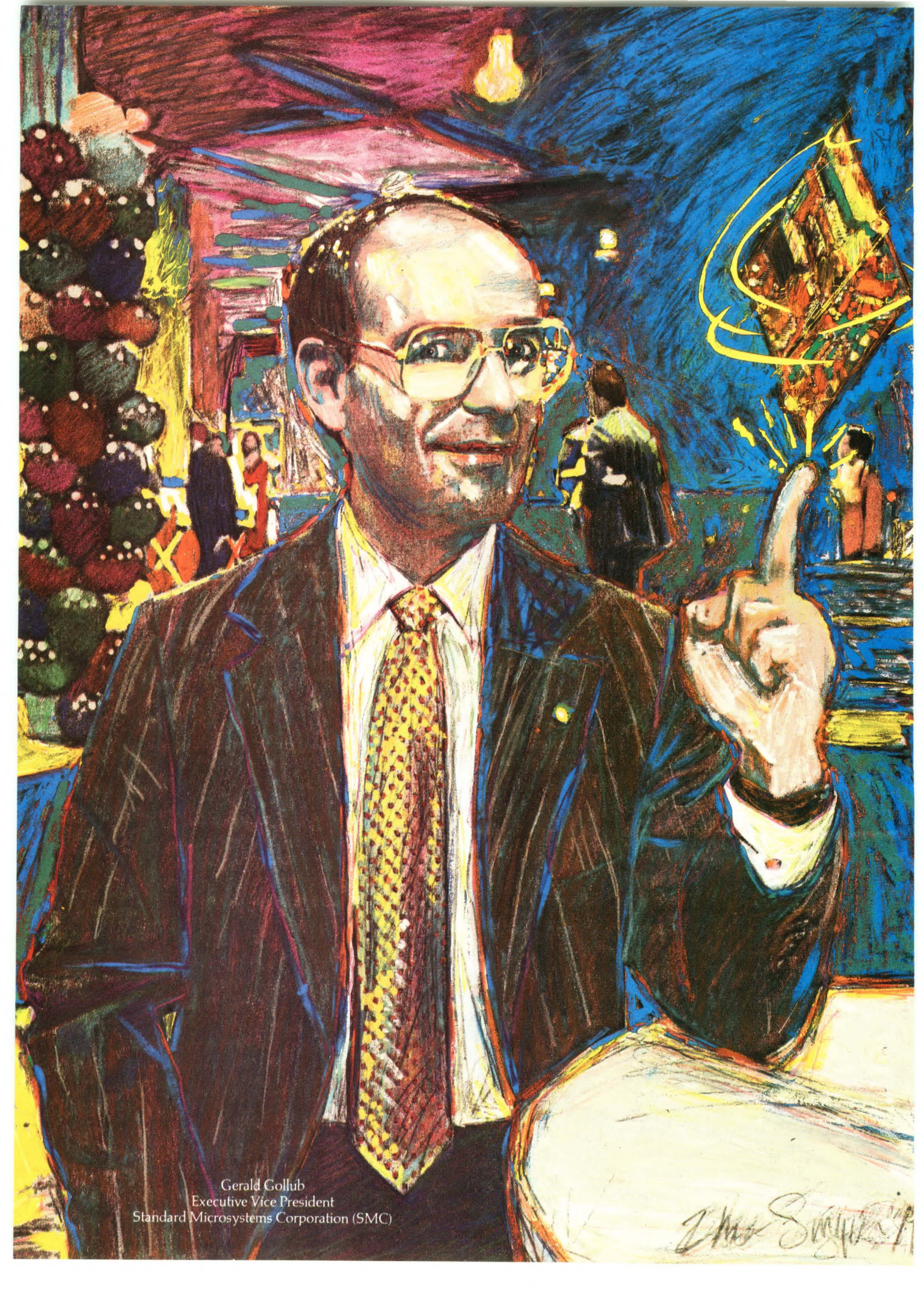
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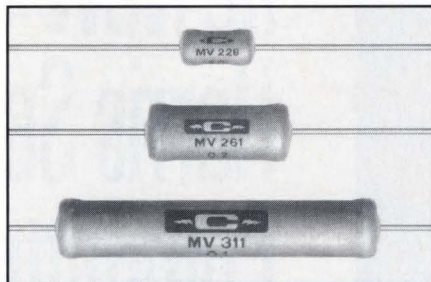


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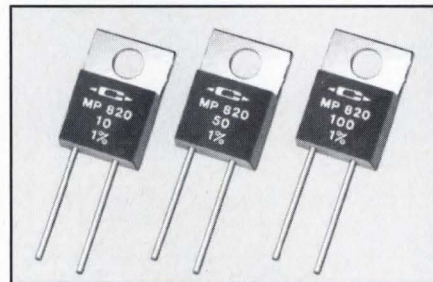


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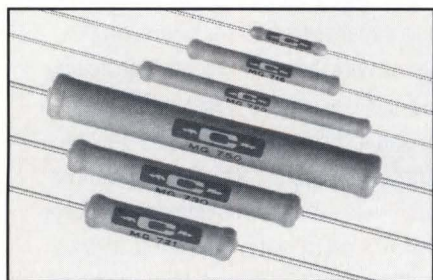
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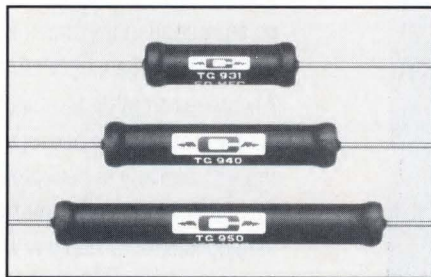


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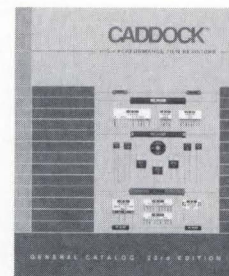
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GAAS CHIP SET SHUTTLES SERIAL DATA AT 1 GBIT/S

DAVE BURSKY

As system backplanes and local buses increase their operating frequencies to keep pace with the higher operating speeds of the microprocessors, costlier design approaches must be applied to reduce the noise, ringing, and crosstalk—all of which degrade signals as they traverse the bus. One solution is to limit the length of the bus. But that's impractical because tomorrow's systems will be more complex and distributed processing will require more data to be shared than ever before. Another solution is to use point-to-point serial buses to transfer key information if the full bus isn't needed. A new gallium-arsenide transmitter and receiver chip set known as the Hot Rod, makes this practical.

The chip set can transfer data at rates as high as 1 Gbit/s. Developed by Gazelle Microcircuits, the chips offer a solution for high-speed point-to-point communications in systems where data communications is the bottleneck in system performance. With the chips, entire parallel buses or data paths can be serialized, transmitted over a coaxial cable or fiber-optic link, and reparsed on the receiving end with minimal overhead.

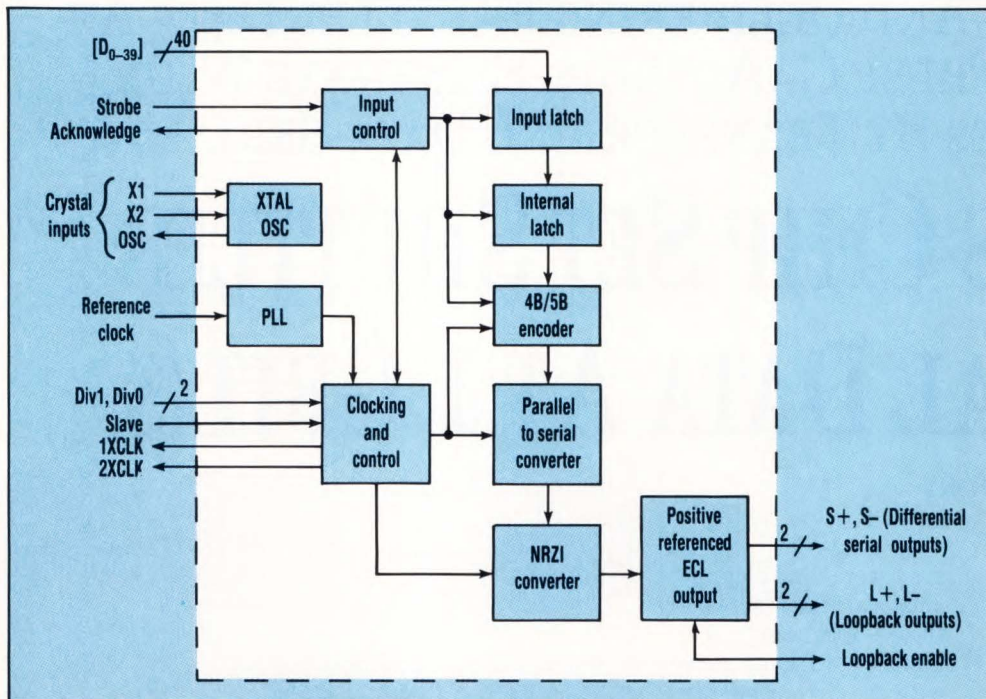
Operating with TTL interfaces to their respective host systems, the GaAs chips run from a standard 5-V power supply, each consuming a maximum of 2 W. To deliver an optimum high-speed serial data stream, the transmitter out-



put and the receiver input employ positive-referenced differential ECL signal swings. Those signal swings are compatible with both coaxial-cable and fiber-optic links.

The Hot Rod transmitter chip—the GA9011—accepts up to 40 parallel bits of TTL data at clock rates of up to 25 MHz with a simple asynchronous strobe/acknowledge handshake proto-

SPEEDY SERIAL DATA LINK



1. PACKING ALL OF THE CIRCUITRY needed to convert 40 parallel bits of data into a 1-Gbit/s NRZI data stream, the Gazelle GA9011 transmitter generates the 1.25-GHz internal timing signal from a 25-MHz crystal.

col (Fig. 1). Each 40-bit input gets encoded into a 50-baud word (frame) using the non-return-to-zero-invert-on-ones (NRZI) 4B/5B coding scheme from the fiber-distributed data interface (FDDI) standard. The 4B/5B scheme translates 4-bit nibbles into 5-baud code symbols (40 data bits become a 50-baud frame). Lastly, the encoded word is shifted out serially through a positive-ECL differential interface.

Two benefits arise from the combined 4B/5B and NRZI encoding: First, the encoding guarantees frequent transitions on the transmitter's serial output. No more than three consecutive non-transitions (0s) can occur. These frequent transitions on the incoming differential data port of the receiver aid the receiver's phase-locked loop in maintaining synchronization with the transmitter. Second, the format ensures a worst-case 60%/40% duty cycle, important for fiber-optic media, because it limits the dc offset voltage of the transmitter's serial outputs.

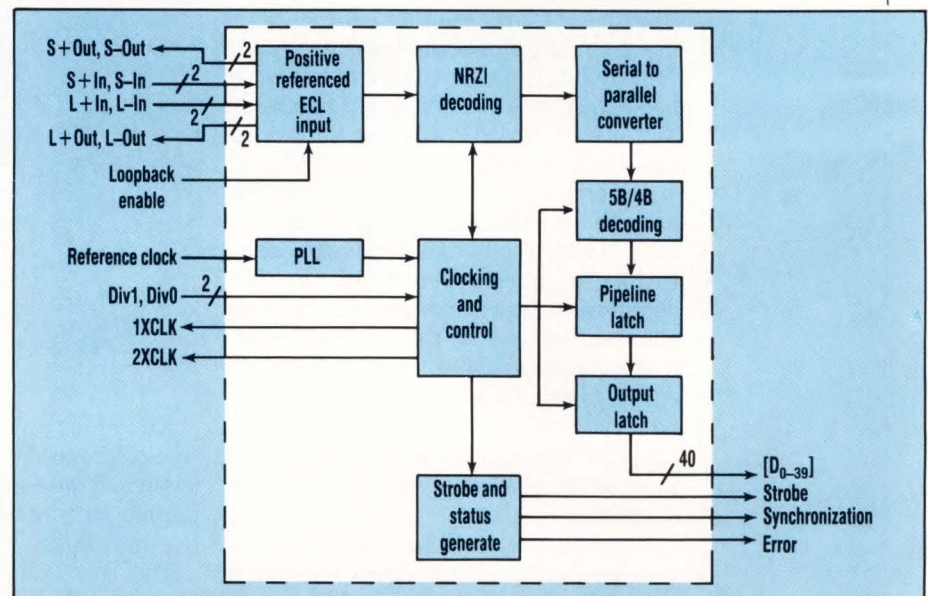
On the receiving end, the GA9011 receiver collects the serial data and recovers both the clock and data in-

formation from the differential signal (Fig. 2). The data is decoded and a 40-bit word is reconstructed for delivery to a TTL bus. New data on the bus is indicated by the rising edge of the Receiver Strobe signal.

signals stems from the increasing use of parallel and distributed processing, remote sharing of massive files, the movement toward high-resolution graphics, and high-definition television. For instance, a high-reso-

In addition, noise and jitter on the serial link can cause the data transmission to be corrupted. Such changes could alter the 5B symbol transmission. As a result, the receiver could detect that one or more invalid 4-bit nibbles were received. When an invalid 5B symbol is received, the receiver chip brings its Error line high and the invalid symbol is decoded as 1111.

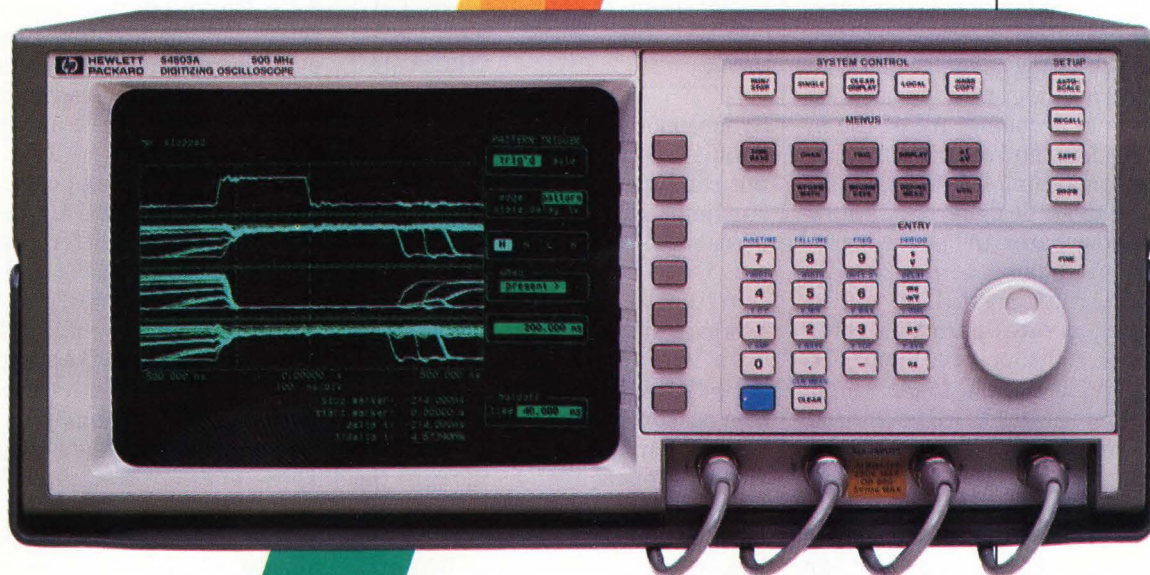
Consequently, entire 32-bit microprocessor data or address buses can be loaded into one Hot Rod transmitter, or multiple transmitter-receiver chip sets and serial links can be employed to transfer 64-bit and wider buses. The need to move these large amounts of data and related control



2. DECODING THE SERIAL DATA STREAM and recovering the clock and data, the receiver chip delivers a 40-bit output along with three system control and flag signals: Strobe, Synchronization, and Error.

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lution 1280-by-1024-pixel display with just 10 bits/pixel for color that's refreshed at 70 Hz requires a serial video-data stream of over 800 Mbits/s. And, still higher data-content displays are expected in the next few years.

Both transmitter and receiver chips are housed in 68-contact leadless chip carriers or ceramic J-leaded chip carriers to minimize board area and lead lengths. Each IC contains all of the circuitry needed to perform the data encoding, transmission, reception, and decoding. All of the internal clocking and control functions required to accomplish the task are transparent to designers. An internal clock oscillator and phase-locked loop are used along with a 20-to-25-MHz external crystal or timing source to generate the internal reference clock (50 times the input frequency). As a result, a 25-MHz input clock becomes a 1.25-GHz internal clock and the problem of routing high-speed clock signals on a circuit card is eliminated.

To the host system, each half of the chip set appears to be a 40-bit parallel register and each of the 40 bits is totally user definable. Input control circuits on the transmitter chip deal with the incoming data and its clocking through the front end of the chip. The transmitter has four selectable speed ranges, which are determined from the frequency of the reference clock input and the value set up on the Div0 and Div1 control pins. Control circuits insert a synchronization frame into the data path whenever there aren't any data words to send, and that frame is resent until new data is loaded into the transmitter chip.

There are actually five distinct ways of clocking data into the transmitter, which gives designers a range of choices to best fit the system. The options include: Asynchronous Strobe/Acknowledge handshake with edge-driven or level-driven signals, Synchronous to the 1X clock signal (a buffered version of the input reference clock),

PRICE AND AVAILABILITY

The GA9011 and GA9012 Hot Rod transmitter and receiver chips are available in 68-lead ceramic J-lead chip carriers and sell for \$157 and \$213, respectively, in 100-unit quantities. Small quantities are available from stock.

*Gazelle Microcircuits Inc.,
2300 Owen St., Santa Clara, CA
95054; Jon Zierk, (408) 982-0900.*

CIRCLE 511

Synchronous to the 2X clock signal (a double-frequency version of the input reference clock), or with a free-running strobe. The 1X and 2X clock signals can also supply timing signals for the host system logic.

With the free-running strobe, however, data words are loaded at 9/10 or less the rate at which they're serially transmitted. This is because a synchronization frame will be inserted approximately as every tenth frame. Consequently, though the free-running scheme has a low overhead, it limits the system to 90% or less of the maximum possible data rate of the chip.

Once the 40-bit data word is in the chip, all operations in the GA9011 become autonomous and the serial data stream appears on differential positive-referenced ECL output lines S+ and S-. The circuit also has two loop-back output test pins, L+ and L-, which can be used for system diagnostics. A separate control pin, Loop Enable, switches the output data flow from the S to the L pins. If the loop-back diagnostic mode isn't

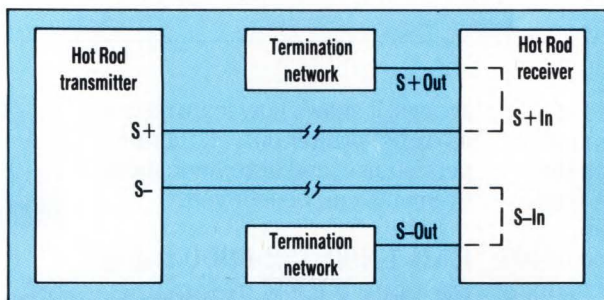
needed, the L pins could actually be used as a second serial data path and the Loop Enable pin could serve as a multiplexer control pin, thus enabling one transmitter to alternately send data to two receiver chips.

The positive-referenced ECL interface delivers ECL signals referenced to 5 V. As a result, a logic high is 4.2 V and a logic low is nominally 3.2 V. The output stage consists of an active pull-up resistor. However, a passive pull-down resistor—50 Ω tied to +3 V, or a Thevenin equivalent circuit to +5-V and ground—must be used.

Performing the opposite task of the transmitter, the GA9012 receiver accepts the serial differential signal and recovers the clock and data. It then performs the NRZI to 4-bit nibble conversion, assembles the 40-bit word, and delivers that word to the 40 output lines. The receiver circuit also has two Loop-Input lines (L+In and L-In) for system diagnostics. Those lines are also controlled by a Loop-Enable input pin.

To make the receiver easier to terminate, which in turn ensures minimal signal reflections, Andy Graham, Gazelle's vice president of engineering, and his design team came up with a scheme they call Fly-By termination (*Fig. 3*). In a system, termination would typically be done right next to the chip package, yet that approach often causes considerable restrictions for the circuit-board layout. But with Fly-By, Graham explains that the input signal, after being sampled by the chip, is routed out of the chip package over two additional pins: S+Out and S-Out. The continuations of the input signal may then be routed to a convenient location for termination. The Hot Rod receiver chip is designed for use with 50- Ω traces. Termination schemes similar to those for the transmitter chip can be employed.

On the receiver chip, the phase-locked loop multiplies the incoming reference clock signal by 50 to generate the timing references

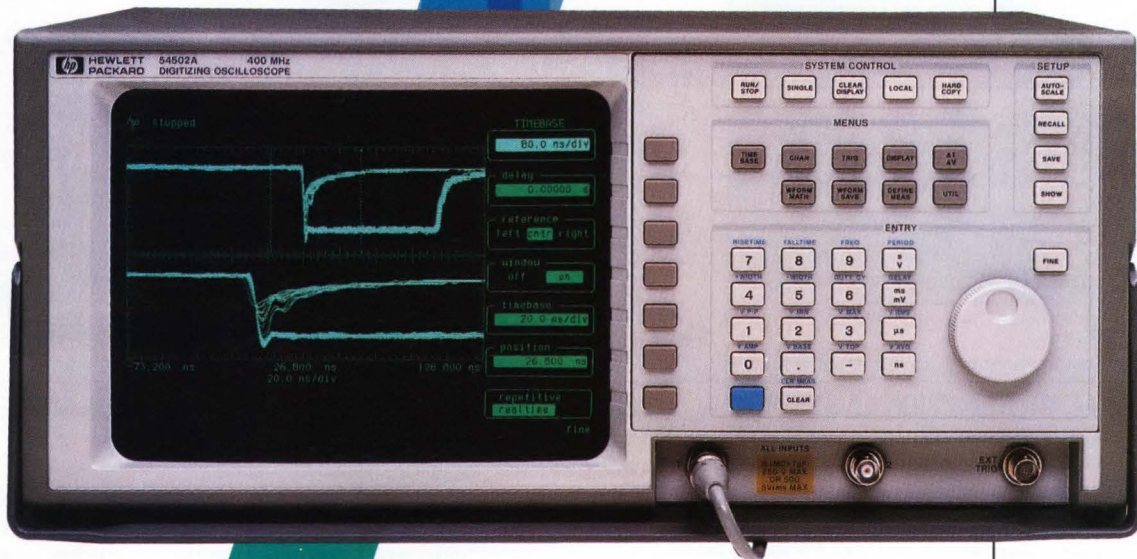


3. TO AVOID THE LAYOUT RESTRAINT

imposed by standard termination schemes, Gazelle developed an approach it calls Fly-By termination. With this technique, input signals can be routed back out of the chip and terminated in a convenient location on the circuit board.

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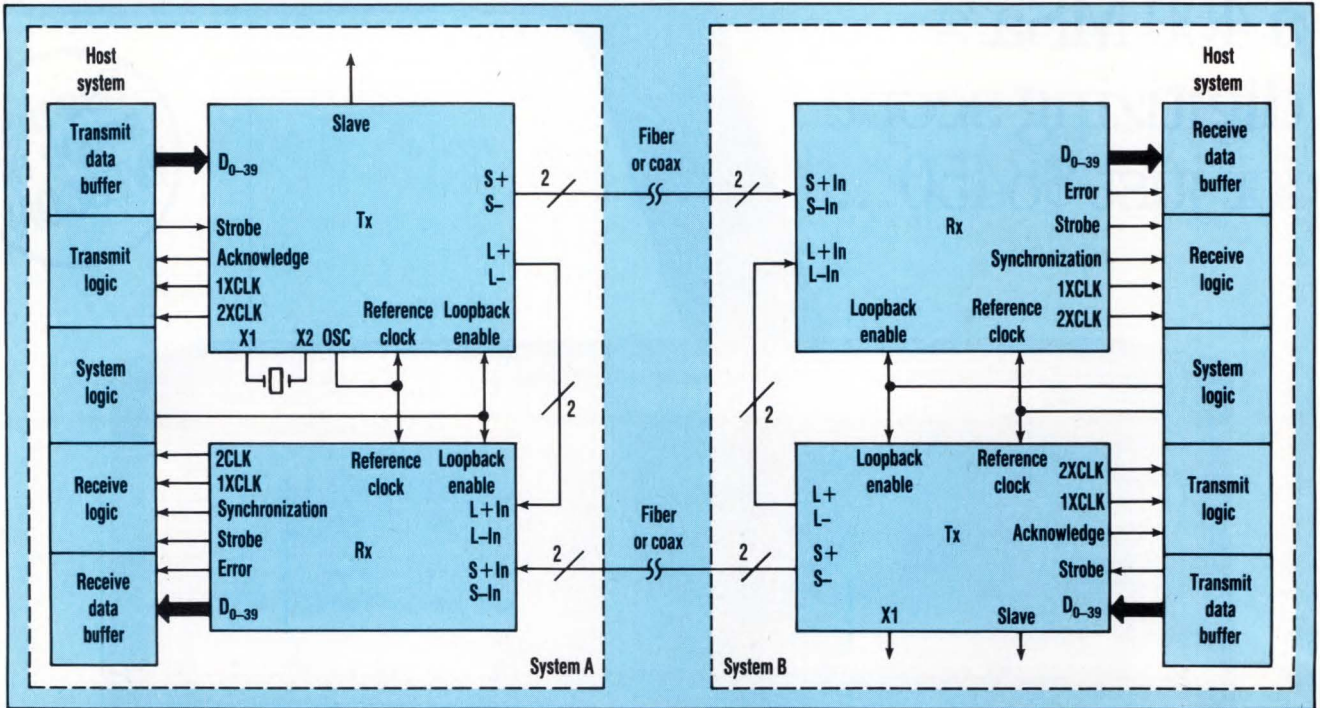
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4. A FULL BIDIRECTIONAL SYSTEM requires both a transmitter and a receiver chip on each side of the system, and twin coaxial or fiber cables to carry the data streams.

that recover the incoming data. Unlike the transmitter chip, though, the receiver doesn't have an on-chip oscillator—the host system must supply the chip with the 20- to 25-MHz reference clock signal. In bidirectional systems that use both transmitter and receiver chips, the oscillator output from the transmitter circuit can also be used by the receiver.

Before any data can be recovered, the receiver must be synchronized to the incoming data stream so that the reception rate matches the transmission rate of the sending unit. Once synchronization is achieved, data can be recovered without any host system intervention. As new data arrives on the serial inputs, the receiver chip writes the just decoded parallel words to the host system bus. The host system must capture this data before the next word is written. The Strobe output from the receiver can be used to control a latch, register, or other storage element (such as a FIFO memory) that should capture the 40 data bits in addition to the Error Flag bit.

An incoming 50-baud frame can be either a data frame or a synchroniza-

tion frame. If it's a synchronization frame, it's discarded and the Synchronization signal on the chip is asserted. The Synch signal can be sampled synchronously on the rising edge of the 1X clock signal. The last data word received (previous to one or more synchronization frames) remains on the output bus. If the incoming frame contains data, the decoding circuits reconstruct the 40-bit word and place the data on the output bus, while raising the Strobe signal line at the same time.

The transmitter and receiver chips can typically be used in four modes—bidirectional, unidirectional, parallel, and loopback. In the bidirectional mode, two sets of chips and two serial channels are needed so that each end of the line is a full transceiver (*Fig. 4*). Unidirectional systems require just one transmitter on one side and a receiver on the other. Parallel systems would be used when large buses or wide data words must be transferred. Multiple transmitter chips, all synchronized to the same clock, can send data over multiple serial channels to multiple receivers, which are also off a common clock.

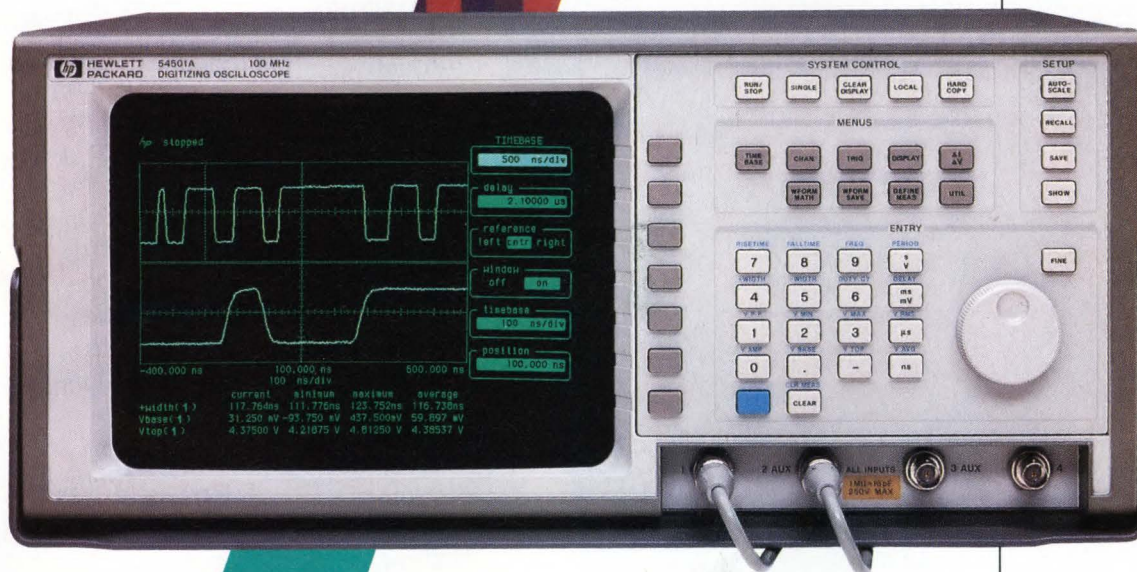
Moreover, the loopback mode, as mentioned earlier, is handy for system diagnostics: It makes sure that the chips are functioning as they should be.

To ensure synchronization in the parallel mode, one transmitter chip is selected as the master device and the rest are set up as slaves to that master. To do that, the Slave control pin on the master device is grounded and the 1X clock pin from that chip drives the Slave pins on the other transmitter chips. Because the 1X clock signal is aligned to the frame transmission, it will enable each slave transmitter to align its frame boundaries to those of the master transmitter. There aren't any Slave pins on the receiver chips, and incoming data is reconstructed as received. To deskew the multiple words to create an 80, 120, or larger bus signal set, a deskewing buffer can be created in the host system. □

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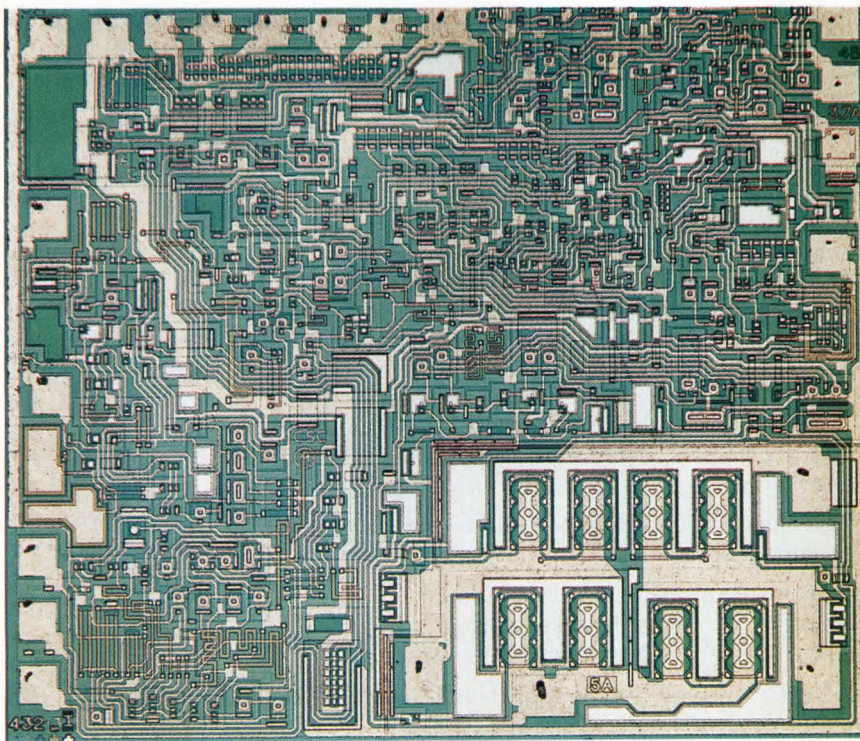
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choose from various converter topologies and employ a vast array of design techniques and features. No longer are you stuck with constant-frequency, voltage-mode, pulse width modulation (PWM) as your basic control technique. Current-mode and resonant-mode control are also available. The choice of control mode depends on trade-offs in switcher price, performance, and size. To cut switcher size, consider current-mode control and switching frequencies above 100 kHz. Above 500 kHz, use resonant-mode control.

Switchers make it possible for shoe-box-sized 500-W off-line supplies, as well as 25-W dc-dc converters that you can hide in your hand. But as system designers call for more speed and computational power (and million-pixel CRT graphics), the demand is on for another round of size slashing. And the only way to up power density is to raise switching frequency, to cut the size of the magnetics along with the capacitive, storage, and filter components. While most controllers and switching transistors easily run at frequencies between 300 kHz and 1 MHz, many supplies still operate well below 100 kHz. This is because it's difficult to design and make circuits for fast power pulses. Furthermore, higher power-supply switching frequencies mean increased switching losses and more rfi/emi.

But switching frequencies are still rising, and as they do and the costs of power FETs drop, you must choose between bipolar or DMOSFET pow-

POWER-SUPPLY IC CONTROLLERS PROLIFERATE

Designers of switch-mode power supplies (SMPSs) or switchers—off-line types or dc-to-dc converters—have at their disposal a wide selection of ICs that satisfy a broad range of power-supply applications. These ICs, which simplify previously discrete-component designs and cut switcher size and cost, include controllers with or sans an on-board power switch (regulators) and switch drivers.

Currently available as well as upcoming ICs range from very basic, general-purpose controllers to special-purpose complete regulators that only need inductors, capacitors, and diodes. They help designers

POWER-SUPPLY IC CONTROLLERS

er switches. In addition, each chip offers a mix of operational, output drive, and protection features, which often distinguish these ICs from one another. Finally, the last six months has seen the emergence of power-factor correction. Whether or not to incorporate power-factor correction into any off-line switcher that controls more than 600 W has become a critical decision. Power-factor correction will affect the design of any off-line supply controlling much more than one-tenth of that power in the near future (*see ELECTRONIC DESIGN, Oct. 12, p. 16*).

In contrast, less than 15 years ago, designing an SMPS meant "rolling your own." You used available op amp and comparator ICs, discrete transistors, or perhaps did it all with just a 555 timer. No controller ICs were available.

The first controller ICs, Silicon

General's SG1524/2524/3524 family, arrived in 1976. At that point, unless you had plenty of money and were willing to gamble on the just emerging MOSFET, your power switches were bipolar transistors. Switching frequencies ran from just above audio to 40 or 50 kHz.

Although things are different today, your task isn't any easier. The wide range of available ICs also means more interrelated and critical design decisions:

- The choice of supply topology.
- The choice of a discrete or an IC controller.
- The choice of control mode—voltage, current, or resonant.
- For resonant-mode control, at a minimum, the choice between zero-current and zero-voltage switching.
- The choice between a multiple-

sourced controller that's been around a while, or one of the unique, advanced devices arriving every day.

- The mix of operational, output drive, and protection features.
- The choice of whether or not to add power-factor correction.

Practical switching rates for current-mode controllers will climb above 1 MHz, and to above 3 MHz for resonant-mode controllers. Choices of current- and resonant-mode and power-factor controller architectures and features will also rise. We may see all of the parts needed for a 5-to-10-MHz resonant supply within 18 months. In fact, circuits working well above that frequency have already been built. Most of the newer (and some earlier) controllers are available in one or more surface-mount packages.

The first PWM controller ICs, the

TABLE 1: VOLTAGE-MODE SMPS CONTROLLER ICs

Model		Originating company		Control circuits		Output device rating		Maximum oscillator frequency	Outputs	Maximum duty cycle	Features									
											Operational					Output drive				
				Voltage range	Quiescent current	Voltage	Continuous current				Sync input	Usable I _{REF}	Feed forward	Low-current start up	On-chip zener	Uncommitted transistor	Totem pole	NOR	OR	Open collector
		(V)	(mA)	(V)	(mA)	(kHz)		(%)												
SG1524	Silicon General	8-40	7	40	100	300	2	50	★	★					★					
UC1524A	Unitrode	10-40	10	60	200	500	2	50	★	★					★					
SG1524B	Silicon General	7-40	12	60	200	400	2	50	★	★					★					
NE1524C	Signetics	7-40	10	60	200	500	2	50	★	★					★					
SG1525/27	Silicon General	8-35	20	35	400	400	2	50	★	★						★	★	/★		
TSC35C25/27	Teledyne Semi-conductor	8-18	2.2	35	100	500	2	50	★	★			★			★	★	/★		
SG1526	Silicon General	8-35	30	35	100	350	2	50	★	★					★					
UC1526A	Unitrode	7-35	20	40	100	550	2	50	★	★					★					
SG1526B	Silicon General	8-35	30	35	100	500	2	50	★	★					★					
SG1529	Silicon General	7-40	12	60	200	400	2	50	★	★	★				★					
UC1840	Unitrode	8-30	15	40	200	1,000	1	100		★	★	★	★	★				★		
TL433/494	TI	7-40	15	40	200	300	2	100	★	★					★					
TL495	TI	7-40	15	40	200	300	2	100	★	★				★	★					
TL594	TI	7-40	18	40	200	300	2	100	★	★						★				
TL595	TI	7-40	18	40	200	300	2	100	★	★				★		★			★	
TDA4714	Siemens	11-30	16	30	20	250	2	100	★		★							★		
TDA4716	Siemens	11-30	16	30	20	250	2	100	★									★		
TDA4718	Siemens	11-30	20	30	20	250	2	100	★		★							★		
TDA4700	Siemens	11-30	20	30	20	250	2	100	★		★							★		
NE5560	Signetics	10-20	15	20	40	100	1	100	★		★			★	★					
NE5561	Signetics	10-20	13	20	40	100	1	100						★				★		
NE5562	Signetics	10-16	15	16	100	600	1	100	★		★			★		★				
MC34060	Motorola	7-40	15	40	200	200	1	100	★	★					★					
MC34060A	Motorola	7-40	15	40	200	500	1	100	★	★					★					
LAS3800	Lambda	12-40	13	40	500	500	2	100	★	★					★					
LAS3840	Lambda	10-40	30	40	200	400	1	50	★	★						★				

POWER-SUPPLY IC CONTROLLERS

SG1524/2524/3524 family, arrived from designer Bob Mammano, then at Silicon General, sometime in 1976. (Since then, the vast majority of the available controller ICs have kept the model numbering standard set by Silicon General. The first digit of the model number is either 1, 2, or 3, indicating operation over military, industrial, and commercial temperature ranges, respectively. The initial letters indicate the supplier.)

The SG1524 is a basic device that supplies voltage-mode control with few features. However, it now has at least 10 different sources. Moreover, at least four improved versions have appeared from four sources, including Silicon General's own SG1524B.

All 1542 versions are pin-for-pin compatible, but the A, B, C, and D versions add both increased performance and features (Table 1). For example, the SG1524B ups output drive

transistor rating from 40 to 60 V and 100 to 200 mA, reference accuracy error from 5% to 1%, and oscillator frequency from 300 to 500 kHz. Added features include double-pulse suppression, programmable cycle-by-cycle current limiting, a PWM latch, a shutdown pin, and under-voltage lock-out (UVLO).

Most of those specifications and features have become starting points for the families of voltage-mode devices spawned by the 1524. These families, Silicon General's SG1525, SG1526 and SG1527, replace the 1524's transistor outputs with totem poles and offer features, such as soft-start and high-speed shut-down paths. The 1525 and 1527 are virtually identical except that the output totem pole goes low when off in the former; high in the latter (NOR vs. OR). The SG1529 is identical with the SG1524B but it adds feed forward to

improve line regulation.

One of the last voltage-mode controllers to appear (in 1981), Unitrode's UC1840 not only moved oscillator frequency to 1 MHz but also offered 1-A totem pole outputs. It also added feed forward plus an on-chip 40-V zener to simplify off-line operation. Its UVLO circuits keep quiescent currents below 5.5 mA while operating current is 15 mA. The fast switching and high peak-current capability of the chip lent it to driving the on-coming surge of power FETs. The 1840 is also available from SGS and Silicon General.

Though it didn't reach the popularity of the 1424, Texas Instrument's TL493/494/495 family—another very basic set of controllers—was also widely sourced. Designed by Barney Holland (now of Unitrode), it arrived less than a year after the 1424. The TL495 has an on-chip zener, one of the few simple controllers so equipped. The TI594/595 added UVLO, with the 595 also sporting a zener. The TL598 is similar but has totem-pole outputs. Motorola's MC34060 is another simple controller in volume production, and it's also available from TI.

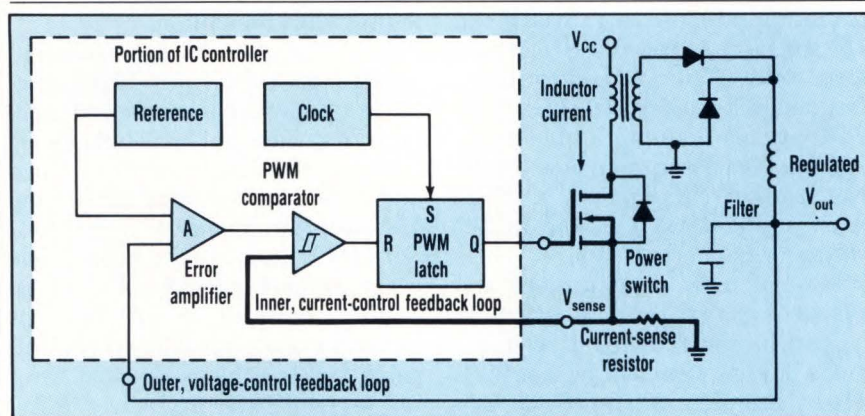
Additional controllers, both simple and sophisticated, are available from Signetics, Siemens, and Lambda. The Signetics units all have on-chip zeners. An additional voltage-mode device, TI's TL497, was also announced in 1976. Rather than employ PWM, it uses constant on-time, variable frequency modulation (fm)—a forerunner of resonant-mode supplies.

SWIM WITH THE CURRENT

The first current-mode controller burst on the scene in 1983, Unitrode's UC1846. It started an explosion of new devices and improved clones that still continue (Table 2). In current-mode control, an inner or secondary loop is used to directly control peak inductor current with the error signal, while the outer loop is used to control output voltage. Instead, voltage-mode converters control the duty cycle of the pulse-width modulator with just the output voltage (see the figure). The technique

Features											Other sources, from company table	
Protection							UVLO					
Programmable current limit	Shut-down pin	Double-pulse suppression	Pulse-by-pulse current limit	PWM latch	Soft-start	High-speed current-fault or shut-down path	Overvoltage lock-out	Senses V _{REF}	Senses supply V	Senses either		DIP pins
★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★		★		★	★ ★ ★ ★		16 16 16 16	13,14,16,19,21
★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★		★ ★ ★ ★ ★	★ ★ ★ ★ ★		16 16 18 18 18	10,11,13,14,19,20,21 10,16,20
★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★		★	★		★ ★ ★ ★	★ ★ ★ ★	16 18	18
★ ★ ★ ★ ★		★ ★ ★ ★ ★						★ ★ ★ ★ ★			16 18 16 18 18	11,14,19,21
★ ★ ★ ★ ★	★ ★ ★ ★	★ ★ ★ ★ ★		★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★		★ ★ ★ ★ ★		14 16 18 24	
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POWER-SUPPLY IC CONTROLLERS



IN CURRENT-MODE PWM CONTROL, each pulse is terminated when the inductor current reaches a certain value. That value is determined by the output of the error amplifier and the voltage across a current-sensing resistor.

offers numerous performance advantages over voltage-mode control—particularly as switching frequencies climb above 500 kHz. To quote Barney Holland, the designer of the UC1846, "The advantages read like a frustrated power-supply designer's wish list."

Most current-mode controllers are designed to charge the 1000 pF, seen at the gates of the HEX-3-size power FETs, with 12-V pulses, in under 300 ns; advanced devices do it in under 100 ns. Current-mode control gives you inherent feed forward, cycle-by-cycle current limiting, and symmetry correction (flux balancing) in push-pull designs. In addition, one of the two poles is eliminated from the control loop, theoretically resulting in inherent closed-loop stability. Overall loop compensation becomes simpler, and both the small- and large-signal response of the loop to load changes speeds up. At the same time, input-voltage feed-forward supplies instantaneous correction for any changes in the supply voltage, while using none of the error amplifier's dynamic range. Line regulation is excellent, and the error amplifier need only work on load changes. Current-mode controllers also lend themselves to power-factor correction and voltage-mode control.

The UC1846 and UC1847 (outputs off in high and low states, respectively) caught on and are also available from Silicon General and TI. They can also be expected sometime in the near future from Teledyne Semicon-

ductor. These chips, which are large, complex, and pack plenty of features, are expensive. They were followed quickly in 1984 by Larry Woford's UC1842/43/44/45. If imitation is the highest form of flattery, then the UC1842/43/44/45 family is a success. In just over five years, Unitrode's chips were cloned by at least six companies. Unitrode has announced improved A versions. The biCMOS TLC38C42-45 are available from Teledyne Semiconductor.

The UC1842/43/44/45 are low-cost 8-pin DIP and SO-14 devices. They offer the major features of the 1840 and 1841, including the on-chip zener and low start-up currents, and are specified for peak drive currents of 1 A—just the output you need to drive MOSFETs fast.

The 1842 and 1843 are for 100%-duty-cycle topologies; their siblings for 50%-duty-cycle circuits. The 1842 and 1844 are optimized for off-line operation with UVLO on/off thresholds of 16 and 10 V. Their cohorts are optimized for dc-to-dc converter applications, so the UVLO thresholds are set at 8.5 and 7.9 V. In addition, start-up currents were dropped to just 1 mA from the 1840's 5 mA. That is, when power is applied to the controller's supply pin, the output is low and only start-up current is drawn, as long as the voltage pin is below the upper UVLO threshold. Once on, the supply must drop below the lower level to go into UVLO.

Unitrode's recent A version of these controllers has start-up cur-

rent of just 0.5 mA. During UVLO, the output can sink at least 10 mA at 1.2 V when the supply voltage is over 5 V. And the oscillator discharge current is trimmed between 7.8 and 8.8 mA, further adding to precision and reliable performance.

SPEED DEMONS

Woford didn't rest on his laurels after the 1842/45. With the demand for higher switching speeds and lower-cost power FETs becoming available, Unitrode announced his UC1823/1825 in 1985 (ELECTRONIC DESIGN, May 30, 1985, p. 97). The 1842/45 can switch at over 1 MHz and also put out peak pulses of 1 A. Consequently, they can charge the 1000-pF gate of a MOSFET to 12 V in under 150 ns. The 1823 suits 100%-duty-cycle operation and has one output; its sibling is for 50%-duty-cycle work. The latter doesn't have an on-chip zener, but its UVLO circuit keeps start-up current below 2.5 mA, although run current is 33 mA. One of the secrets of the chips' speed is internal propagation delays, in critical control-loop paths, of under 60 ns.

Returning to the UC1823/1825, the fact that it took over three years to come up with a controller to drop into its socket is indicative of the significance of Woford's controller. The solution came from a new player, Micro Linear, which did it on an array in less than a year (ELECTRONIC DESIGN, Nov. 30, 1988, p. 135). The result is actually a family of controllers: The ML4823/25 are moderately improved versions of the UC1823/25, while the ML4809 and new ML4810/11 offer additional mixes of features and performance. On the other hand, you can have it built "your way" on the ML3480 array and specify an exact mix of features. Turn-around time from the design to prototypes can be as short as six weeks.

The output stage, common to all controllers built with the Microlinear array, drives a 1000-pF FET gate 13 V positive in 60 ns. That's about one-third of the time it takes the Unitrode chip. Moreover, the propagation delay in Micro Linear's current-limit shutdown path is just 70 ns. In addition, the outputs are low during

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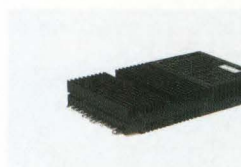
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UVLO, and the soft-start latch insures a full soft-start cycle. The dual-output ML4809, released not long after the 1823/25, adds or alters multiple features, including UVLO thresholds similar to those of the UC1842/44 (16 V to start, with 7 V of hysteresis), a voltage-controlled oscillator input for synchronization or frequency control, a PWM comparator blanker for noise immunity, programmable soft-start delay, and programmable ramp compensation.

Until now, the need for ramp compensation in current-mode regulators operating with duty cycles above 50% has meant the use of about half-a-dozen external passive devices plus a transistor. The 4809 needs just one programming resis-

tor. The comparator blanker eliminates the effect of noise spikes during the first few nanoseconds that the FET switch is on. Such spikes, potentially caused by inductance in the current-sensing resistor, inter-winding capacitance in the transformer, or reverse recovery in the rectifiers or FETs, can quickly terminate the FET on-time and cause instability.

Micro Linear's just now available ML4810/11 controllers (also built on the array) offer additional mixes of features and performance. Like the 4809, they're dual-output units. However, the 4811 abandons the 16-pin DIP for 20 pins. Both devices pick up all of the features of the ML1823/25, as well as the UVLO of the 4809. The 4811 also offers a soft-start, re-

set delay, and a sync input.

A true innovation offered by both devices is called integrating soft-start. The circuit "counts" (integrates) the number of times that the cycle-by-cycle current limiter terminates a PWM cycle. After a preset number, programmed with an RC network, the circuit activates a soft-start cycle. The scheme is needed because at high switching speeds and short propagation and turn-off delays in the controller, a true load fault may never be detected.

Rather than design a drop-in for the Unitrode 1523 controller, Silicon General chose a slightly different architecture for its SG1528/30 and moved to an 18-pin DIP. The company's single-totem-pole output has a

TABLE 2: CURRENT-MODE SMPS CONTROLLER ICs

Model		Originating company	Control circuits		Output device rating		UVLO On-Off thresholds	Start-Up current	Duty cycle	Maximum oscillator frequency	Outputs	Features								
					Current							Operational								
			Voltage range	Quiescent current								Voltage	Continuous	Peak	Feed forward	Low-current start up	On-chip zener	Usable I_{REF}	Duty cycle control	Sync input
(V)	(mA)	(V)	(mA)	(A)	(V)	(mA)	(%)	(MHz)												
UC1840	Unitrode	8-30	15	40	200	1.5	NS	5.5	100	0.5	1	★	★	★						
UC1841	Unitrode	8-30	12	40	200	1.5	NS	5	100	0.5	1	★	★	★						
UC1851	Unitrode	8-30	21	40	200	1.5	NS	6	50	0.5	1	★	★	★						
UC1842	Unitrode	11-30	17	30	200	1	16-10	1	100	0.5	1	★	★	★	★	★				
UC1843	Unitrode	8-30	17	30	200	1	8.4-7.6	1	100	0.5	1	★	★	★	★	★				
UC1844	Unitrode	11-30	17	30	200	1	16-10	1	50	0.5	1	★	★	★	★	★				
UC1845	Unitrode	8-30	17	30	200	1	8.4-7.6	1	50	0.5	1	★	★	★	★	★				
UC1842/45A	Unitrode	Equal or superior to 1842/1845. See text for improvements.						0.5	Equal or superior to 1842/1845. See text for improvements.											
TSC38C42	Teledyne Semiconductor	8-28	1.5	28	200	0.7	16-10	0.2	100	0.5	1	Low-power BiCMOS versions of 1842/1845. All features. See text for additional improvements.								
TSC38C43	Teledyne Semiconductor	8-28	1.5	28	200	0.7	8.4-7.6	0.2	100	0.5	1									
TSC38C44	Teledyne Semiconductor	8-28	1.5	28	200	0.7	16-10	0.2	100	0.5	1									
TSC38C45	Teledyne Semiconductor	8-28	1.5	28	200	0.7	8.4-7.6	0.2	100	0.5	1									
UC1846	Unitrode	8-40	21	40	100	0.4	8-7	2.5	50	0.5	2	★	★		★	★				
UC1847	Unitrode	8-40	21	40	100	0.4	8-7	2.5	50	0.5	2	★	★		★	★				
TSC38C46/47	Teledyne Semiconductor	8-16	2	NA	100	0.3	8-7	0.2	50	0.5	2	Low-power BiCMOS version of 1846/1847, has all features.								
UC1823	Unitrode	10-30	33	30	500	1.5	9-8	2.5	100	2	1	★	★		★	★				
UC1825	Unitrode	10-30	33	30	500	1.5	9-8	2.5	50	2	2	★	★		★	★				
ML4823	Micro Linear	10-30	33	30	500	1.5	9-8	2.5	100	1	1	★	★		★	★				
ML4825	Micro Linear	10-30	33	30	500	1.5	9-8	2.5	50	1	2	★	★		★	★				
ML4809	Micro Linear	10-30	38	36	500	1.5	16-9	2.5	50	1	2	★	★		★	★	★			
ML4810	Micro Linear	10-30	39	30	500	1.5	16-9	3	50	1	2	★	★		★	★	★			
ML4811	Micro Linear	10-30	39	30	500	1.5	16-9	3	50	1	2	★	★		★	★	★			
SG1528	Silicon General	13-17	30	20	200	2	NA	0.6	50	0.44	1	★	★		★	★				
SG1530	Silicon General	13-17	30	20	200	2	NA	0.6	100	0.44	1	★	★		★	★				
TDA4918	Siemens	10-30	20	30	500	NS	7-6	3.5	50	0.3	2	★	★							
TDA4919	Siemens	10-30	20	30	500	NS	7-6	3.5	100	0.3	1	★	★							
CS-322	Cherry Semiconductor	13-17	20	20	200	1	14-10	1.5	100	1	1	★	★				★			
CS-324	Cherry Semiconductor	13-17	20	20	200	1	6-9	1.5	100	1	1	★	★				★			

NS = not specified NA = not available

POWER-SUPPLY IC CONTROLLERS

continuous current of 500 mA with peaks of 2 A. The 1528 is for 50%-duty-cycle applications; its sibling for 100% tasks. On-chip over- and under-voltage comparators are programmed externally with resistive dividers. Like many of these fast controllers, it lacks an on-chip zener. However, it supplies low-current start-up circuitry with on/off thresholds of 17 and 13 V. Start-up current is a low 600 mA, while operating current is 36 mA.

Another feature of the 1528/30, its "Hiccup" comparator, triggers the soft-start circuit (as do the under- and over-voltage comparators) when the output of the current (error) amplifier exceeds a programmable limit. In addition, like many of the ad-

vanced controllers, the soft-start circuit goes through a complete cycle every time it's triggered.

40-V FAST BiCMOS

Controllers are the domain of a small cadre of chip designers who, working closely with top power-supply designers and application engineers, stretch their analog circuit expertise to its limits. Controlling 100-ns, 15-V, 3-A pulses with precision isn't a trivial task.

Most controllers are built on 36- to 40-V processes. And all of them are versions of a standard analog bipolar process (except those from Teledyne Semiconductor). As noted, Teledyne is entering the fray with BiCMOS controllers that have features and

performance equal or superior to available devices. Thanks to the process and circuit tricks, controllers from the 3- μ m (and greater) metal-gate process, dubbed "Tough CMOS," successfully handle the required voltages. It should also be noted that resonant-mode controllers for switching rates beyond 1 MHz have moved to 20-V bipolar processes that build ECL logic.

Teledyne is now bringing its BiCMOS process to two families of controllers: the current-mode 1842/45 and 1846/47, and the older voltage-mode 1525/27. Three versions of the 1842/45 will join the party: the TSC38C42/43/44/45, the TSC172/3/4/5, and the TSC18HC42/43/44/45. Quiescent current for all of these controllers is no more than 2 mA, which is at least an order-of-magnitude less than that of bipolar units. Start-up current is under 250 μ A, greatly simplifying off-line operation. And even while driving FETs fast and hard, operating current is lower than earlier units. While most of these chips will go into line-powered systems, the low current offers advantages in battery or other applications with limited sources of power.

Basic specifications and features for the TSC38C42/43/44/45 controllers are similar to those of the bipolar units. Improvements include a tightly specified clock-ramp reset current ($1 \text{ mA} \pm 10\%$) for accurate dead-time control. The 172 through 174 offer more. To start with, they're faster, with an oscillator frequency of 1 MHz. Typical propagation delays from current amplifier to output drop from 250 to 140 ns; delays between shutdown and output drop from 200 to 90 ns. Instead of an 8-pin DIP, the 172 and 174 come in 16-pin DIPs; the 173 and 175 in 14-pin DIPs. On all four, the extra pins supply a power ground, user-programmable UVLO levels, and hysteresis. They also make it possible to replace the exponential timing ramp with a linear one.

Cherry Semiconductor's CS-320/21 and CS-323/24 controllers employ what's called Hysteretic—current-mode control. The general-purpose

Features

Output drive					Protection										UVLO			DIP pins	Other sources, from company table
Open collector	Totem pole	Power ground	NOR	OR	Double-pulse suppression	High-speed current-fault path pin	Over-voltage lockout	Programmable current limit	Pulse-by-pulse current limit	PWM latch	Soft-start	Shut-down pin	Senses V_{REF}	Senses V_{IN}	Senses either				
★					★	★	★	★	★	★	★					18	13,18		
	★				★	★	★	★	★	★	★	★			★	18			
					★											18			
	★	★			★			★	★	★				★		8/14	} { 9,10 13,14 16,18 19,20		
	★	★			★			★	★	★				★		8/14			
	★	★			★			★	★	★				★		8/14			
	★	★			★			★	★	★				★		8/14			
Equal or superior to 1842/1845. See text for improvements.																			
Low-power BiCMOS versions of 1842/1845. All features. See text for additional improvements.																			
	★		★		★			★	★	★	★	★		★		16	} { 18,19		
	★			★	★			★	★	★	★	★		★		16			
Low-power BiCMOS version of 1846/1847, has all features.																			
	★	★			★	★		★	★	★	★	★		★		16	Improved UC1823/25 (as shown) has all features plus additional features and improvements (See text).		
	★	★			★	★		★	★	★	★	★		★		16			
	★	★			★	★		★	★	★	★	★		★		16			
	★	★			Improved ML1825, extra pins. See text for details. Improved ML1825, some features of ML4809 and others. (See text) Improved ML1825. All features of ML4810 and others. (See text)											24			
	★	★														16			
	★	★														20			
	★	★			★	★	★	★	★	★	★				★	18			
	★	★			★	★	★	★	★	★	★				★	18			
	★	★			★	★	★	★	★	★	★				★	20			
	★	★			★	★	★	★	★	★	★				★	20			
	★				Not PWM (See text)			★	★							8			
	★							★	★							8			

POWER-SUPPLY IC CONTROLLERS

A SAMPLING OF IC POWER-SUPPLY CONTROLLER SUPPLIERS

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Code: 1 = voltage mode; 2 = current mode; 3 = resonant mode; 4 = power-factor correction; 5 = complete regulator; 6 = charge pump; 7 = miscellaneous

CS-320/21 can also operate in a constant-frequency current mode as well as in a constant off-time mode.

In a hysteretic controller, a window comparator compares the inductor current with the output of the error amplifier and turns off the FET when a maximum, programmed value is reached. The comparator turns the FET back on when the inductor current drops by a preset amount (the hysteresis). The frequency of the resulting free-running "oscillator" is a function of the input and output voltage of the supply, and of the circuit's inductance. It can reach 1 MHz with these ICs. This technique offers the fastest response time to changes in inductor current, and thus changes in-line voltage or load current. Feed forward applies easily and ramp compensation is never needed.

In a typical SMPS, during the few hundred or less nanoseconds it takes

the FET switch to turn on or off, voltage appears across the switch while current flows through it. In a typical example, peak powers of 1000 or more W (10 A at 100 V) could result. However, even switching at 100 kHz, this power is less than 1% of the total duty cycle, and the average switching loss is less than 10 W, or less than the on-time conduction losses.

At 1 MHz, however, the switching time can approach 10% of the duty cycle and average switching losses could approach 100 W. Consequently, as you raise switching frequencies to cut component size, your heat sink will have to get bigger to get rid of the heat from higher switching losses. You can use a larger FET than you need with a lower on resistance to significantly cut conduction losses (and thus heat-sink size), but switching losses won't be cut at all. In fact they may rise. The larger FET will have a larger input capaci-

tance, and if not driven harder may take longer to turn on.

At 1 MHz, significant switching losses also arise due to parasitic circuit and component inductance and capacitance. These parasitics also create voltage and/or current stresses on the semiconductor components, as well as unwanted oscillations. And of course there's rfi/emi. The edges of the fast power pulses contain lots of energy between 10 and 100 MHz—energy that must be contained (filtered and shielded).

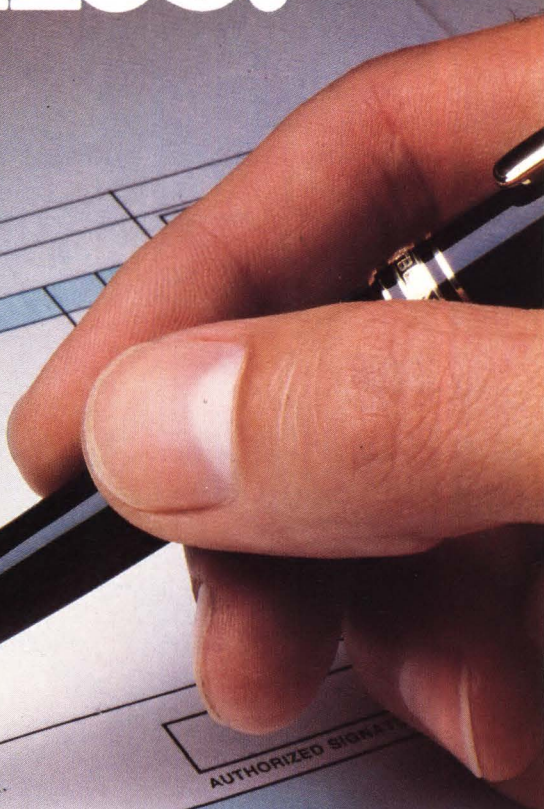
RAISE SMPS FREQUENCY

One way to raise SMPS switching frequency without suffering the consequences is to switch from PWM voltage or current-mode control to resonant-mode control. In resonant converters, the power switch applies pulses of current or voltage to an LC circuit causing it to resonate. The energy circulating in the resonant circuit is in turn passed on to the load. This control technique has exploded on the scene in the past 15 months because it gives you zero-current switching (ZCS) or zero-voltage switching (ZVS), virtually eliminating switching losses, and reducing component stress and rfi/emi.

With resonant-mode control, you turn the FET switch on and off when there's no current flowing through it (zero-current switching), or alternatively when there's no voltage across it (zero-voltage switching). Until now, IC controllers were only available for the former method. While there are over 40 ways to implement resonant-mode control, the two most common methods are quasi-resonant, variable-frequency, constant on-time control, and quasi-resonant, variable-frequency, constant off-time control. The former lends itself to off-line supplies with high-voltage inputs; the latter to lower-voltage-input dc-to-dc converters.

Both species of switchers use similar control loops. The variable-frequency oscillator turns the switch on via a one-shot at a repetition rate determined by the output of the error amplifier. Pulse width from the one-shot can be fixed. Or it can be a function of the time constant of the reso-

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LH5491	64 X 9	35MHz	X		X
LH5485	256 X 8	35MHz	X		
LH5495	256 X 9	35MHz	X		X
LH5496	512 X 9	20nS	X	X	X
LH5497	1K X 9	20nS	X	X	X
LH5498	2K X 9	20nS	X	X	X
LH5499	4K X 9	20nS		X	X
LH9131	32 X 32 integer multiplier accumulator	23MHz	169PGA		

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LH5116	2K X 8	100nS	X	X		X
LH5160	8K X 8	100nS	X	X		X
LH51256	32K X 8	100nS		X		X
MIXED MOS						
LH5261	64K X 1	25nS	X		X	
LH52251	256K X 1	25nS	X		X	
LH52252	64K X 4	25nS	X		X	
LH52254	32K X 8	25nS	X		X	
CS TYPE						
LH52256	32K X 8	70nS		X		X
LH52258	32K X 8	25nS	X	X	X	



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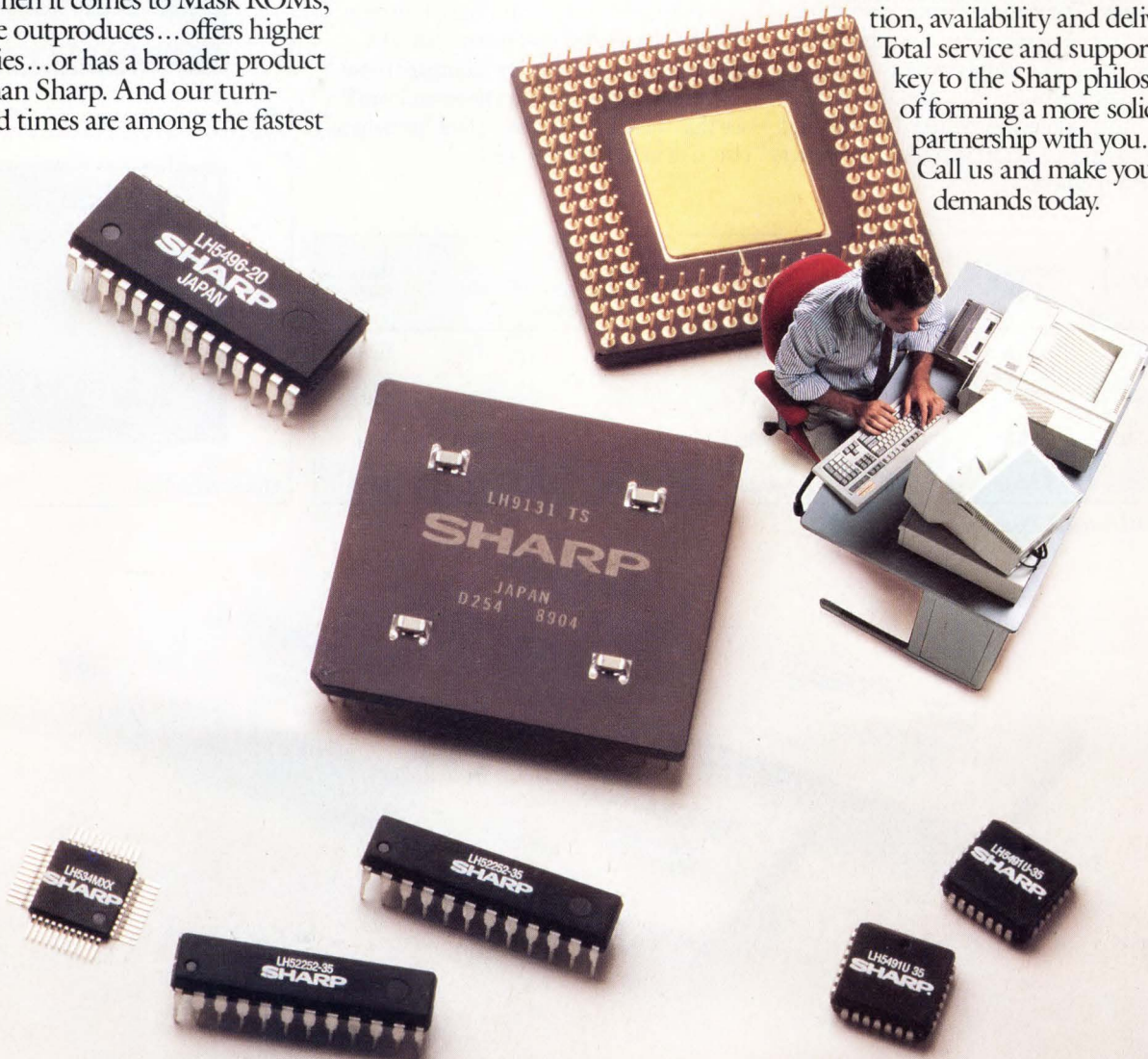
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MASK ROMS				
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LH532XXX	2 Meg	X8 or X16	150,200,250	DIP, QFP, SOP
LH534XXX	4 Meg	X8 or X16	*100,150,200	DIP, QFP, SOP
LH538XXX	8 Meg	X8 or X16	200,250	DIP, QFP
LH536XXX*	16 Meg	X8 or X16	200	QFP

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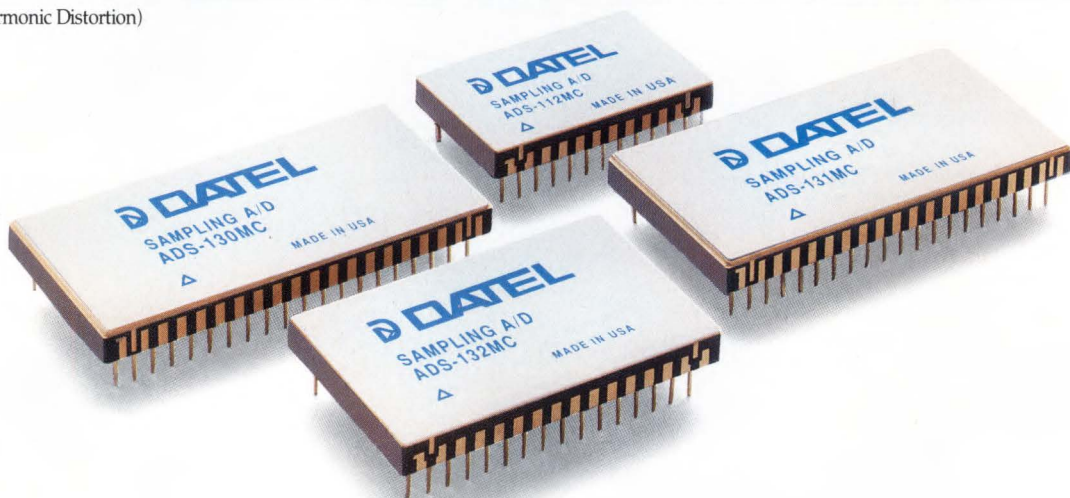
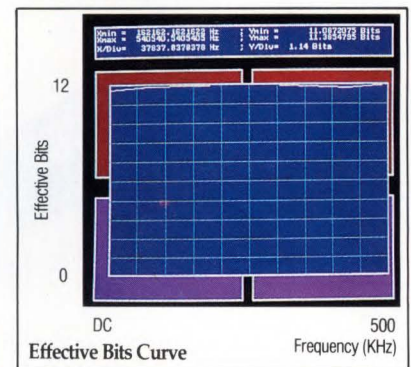
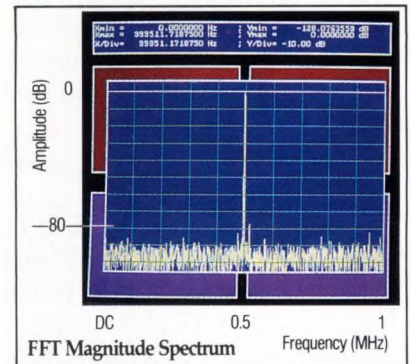
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ADS-132	2MHz	11.0	-73 dB	2.9 watts	32-pin TDIP	\$346
ADS-131	5MHz	10.6	-69 dB	4.2 watts	40-pin TDIP	\$549
ADS-130	10MHz	10.6	-69 dB	4.5 watts	40-pin TDIP	\$775

* THD (Total Harmonic Distortion)



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POWER-SUPPLY IC CONTROLLERS

shot can be fixed. Or it can be a function of the time constant of the resonant circuit, and/or the switch can be turned off when zero voltage or current is detected.

When the controller turns on the switch in a ZCS circuit, the voltage across the switch drops to zero and a half-sinusoidal pulse of current flows through it and into the load. The input voltage and resonant tank parameters determine the current pulse's peak value and width. Any time after the value of the current drops to zero, the switch can be turned off with zero loss. There is a small switching loss at turn-on, during the rapid rise of the current pulse as the switch voltage drops. Each time the switch closes, a packet of energy is transferred to the load. If the output voltage drops, the frequency goes up and vice versa.

The sinusoidal pulse contains little energy above the fundamental switching frequency, greatly reducing rfi/emi. A more subtle advantage is that some or all of the parasitics can be incorporated in the resonant circuit, aiding rather than abusing components and performance. However, the energy carried by the sinusoidal current pulse averages about half that of a square pulse of equivalent width and height. Therefore, the switch and diodes must be chosen to carry peak currents about twice that found in a conventional switcher. But their voltage ratings can be similar.

The ZVS converter can be considered the dual of the ZCS. When the switch is closed, the current through it rises instantly to a value based on the resistance in the circuit. The tank capacitor is shorted by the switch. When the switch is opened, the tank resonates, a half-sinusoidal voltage appears across the switch (and capacitor), and a packet of energy is transferred to the load. As the load demands more power, the switching frequency drops. When the voltage pulse drops to zero, the switch is closed. We have a square wave of current, but a sinusoidal voltage. However, with the ZVS circuit, the switch will see twice the voltage rather than, like the ZCS circuit,

twice the current of a conventional converter. Thus, the ZCS circuit will be used in off-line converters where the voltages will tend to be high and the currents low; the ZVS circuit in dc-to-dc converters where the opposite voltage and current require-

ments are needed in the switch. □

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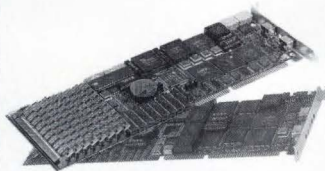
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CIRCLE 67

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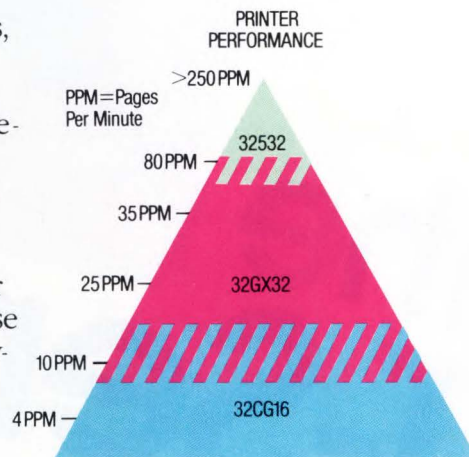
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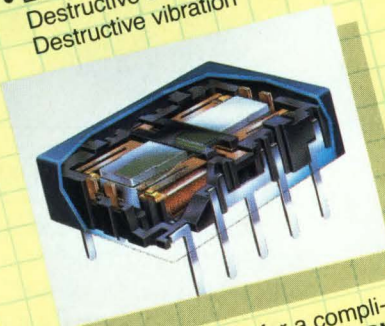
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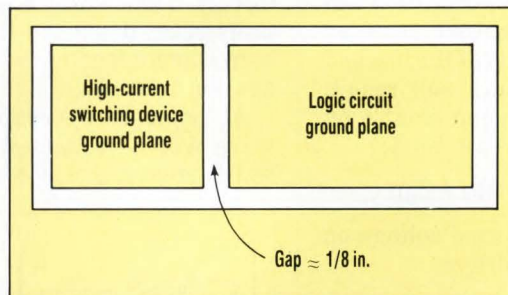
MAKE SURE THAT YOUR TURBO-CHARGED LOGIC SYSTEM WORKS BY PAYING AS MUCH ATTENTION TO PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES AS TO LOGIC DESIGN CONSIDERATIONS.

AVOID THE PITFALLS OF HIGH-SPEED LOGIC DESIGN

Modern high-speed systems demand modern high-speed logic families. Consequently, semiconductor houses have developed such product lines as ACT, FACT, and AS. But these systems also demand that the lay-out of their boards conform with the results of distributed-element theory, otherwise ringing, crosstalk, and other transmission-line phenomena render those systems inoperative. Meeting this second requirement necessitates something more than a new product introduction—it insists on a change in the way logic boards are engineered. The logic-systems designer and the board-layout designer must work hand-in-hand if a viable high-speed board or system is to be produced.

In the past, logic design and board layout were usually regarded as separate parts of the design process. First the system designer configured the logic, then the board engineer laid it out. That approach worked because slew rates were so low (0.3 to 0.5 V/ns) that crosstalk wasn't much of a problem; rise times were so long (4 to 6 ns) that ringing could settle down before a logic element could change state; and in general, the assumptions of lumped-element circuit theory usually worked out pretty well.

For systems designed with today's high-speed logic circuitry, those underlying assumptions no longer hold true. Today's slew rates are on the order of 2 to 3 V/ns, rise times are below 2 ns (frequently, below 1 ns), and transmission-line phenomena, such as ringing, can be a problem for trace



1. TO MINIMIZE NOISE, THE ground plane should be fragmented into separate areas for noisy high-current devices and for sensitive logic circuits. For best results, the number of signal lines that cross the gap between the fragments should be minimized.

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DESIGNING WITH HIGH-SPEED LOGIC

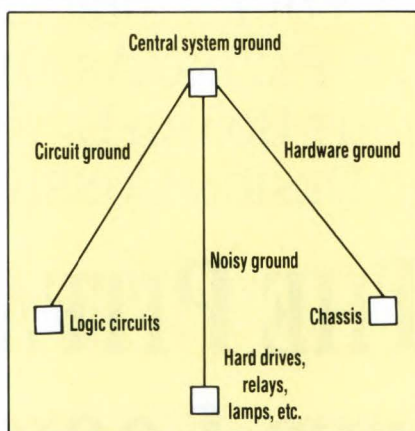
lengths as short as 7 in. As a result, logic designers must take certain steps:

- Use ground and power planes.
- Control conductor spacings to eliminate crosstalk.
- Make extensive use of decoupling capacitors.
- Pay attention to ac loading.
- Terminate lines properly to minimize reflections.

PLANE ADVICE

For high-speed logic, ground planes aren't simply suggested for reliable board performance—they are absolutely necessary. It's essential that one layer of the board be assigned for a ground plane and that it cover as large an area as possible. A solid ground plane lowers the ground-return-path impedance as well as the device-to-device ground pin impedance.

But a common ground plane for all of the circuitry in a system can cause problems by coupling noise from high-current switching devices into sensitive logic inputs. Therefore, the ground plane for such high-current



2. SEPARATE DEDICATED grounds should be supplied for the logic circuitry, noisy high-current devices, and the chassis. The three should come together at one point, the central system ground, which is usually located near the power supply.

devices as relays, lamps, motors, and hard drives should be separated from the logic ground. This can be accomplished by fragmenting the ground plane into discrete areas (Fig. 1).

But fragmentation causes problems of its own—it creates discontinuities in the characteristic imped-

ance of any transmission line that crosses the separation between fragments. Therefore, for best results, boards should be laid out so that only two fragments are needed. The gap between those fragments should be kept as narrow as possible (an eighth of an inch works well in most applications), and the number of signal lines that cross the gap should be minimized. Designers should also bear in mind that through-holes and vias subtract from the effective area of the plane, increasing its effective impedance.

As with grounding, an entire layer of the board should be designated as a power plane. Even though it is at a different potential, the power plane should be implemented in accordance with the same concepts as the ground plane. Therefore, it should be fragmented when necessary to isolate noisy components from delicate logic circuits.

A WELL-GROUNDED SYSTEM

In addition to properly designed power and ground planes, high-speed logic systems require the establishment of a good, clean (low-

SIGNAL LINES BECOME TRANSMISSION LINES

For the transmission line model illustrated in the diagram, the rise time (t_R) is less than the line propagation delay (T_D). In other words, a complete TTL level transition will occur before the pulse is received at the receiving end of the line and reflections (ringing) will result. The voltage change at point A on the line is expressed in Eq. 1:

$$\Delta V_A = \Delta V_{int} (Z_0 / (R_0 + Z_0))$$

Where: V_{int} = internal voltage on the output of the driver;

R_0 = output impedance of the driving gate;

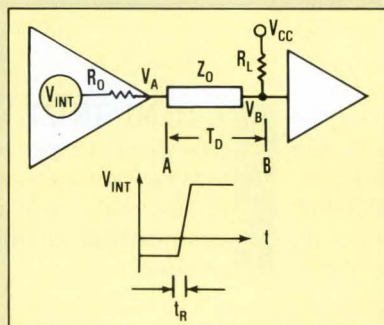
R_L = load impedance;

Z_0 = the characteristic line impedance;

and V_A = the source voltage at the sending end of the line.

Because R_0 is so small when compared to the line impedance, the change in voltage at point A (ΔV_A) will approximately equal the change in internal voltage (ΔV_{int}). This voltage transition propagates down the line and is seen at point B after the line propagation delay, T_D .

At point B, a portion of the wave will be reflected back towards point A in accordance with



the formula (Eq. 2):

Eq. 2

$$\rho_L = (R_L - Z_0) / (R_L + Z_0)$$

where ρ_L , called the voltage reflection coefficient (rho), is the ratio of the reflected voltage to the incident voltage.

After examining Eq. 2, it should be evident that $-1 \leq \rho \leq +1$. It should also be evident that there will be no reflected wave if $R_L = Z_0$ —if the line is terminated in its characteristic impedance. Note that the reflected wave can, in principle, be as large as the incident voltage and of either positive or negative polarity.

This analysis holds true for the sending end of the line, as well as the receiving end. That is,

Eq. 3

$$\rho_S = (R_0 - Z_0) / (R_0 + Z_0)$$

DESIGNING WITH HIGH-SPEED LOGIC

noise) system ground for reliable performance. A clean system ground ensures less noise within the system, and thus ensures good, strong transistor margins. At least 10% of the ground connections on the pc card should be connected to the system ground to reduce card-to-ground impedance.

Like the ground and power planes of the individual boards, the overall grounding scheme should be fragmented with separate conductors provided for the various sections of the system. For example, all relays, lamps, hard drives, and other noise-generating devices should have their own separate ground path. The system's mechanical package (chassis, panels, and cabinet doors) should have a dedicated ground. And, of course, the logic circuitry should have a ground of its own.

Those three grounds should then come together at the central system ground point, which will usually be located near the power supply (Fig. 2). This common-point grounding technique can also be very effective in reducing radiated interference (EMI and RFI).

TAMING CROSSTALK

Crosstalk—the undesirable coupling of a signal on one conductor to one on a nearby conductor—becomes an increasingly serious problem as slew rates go up. This signal coupling is made worse if the second trace has a high impedance or if the traces run parallel to one another for more than a few inches and are spaced less than 100 to 150 mils apart.

Crosstalk can be catastrophic to a logic board, sabotaging a conceptually flawless piece of logic design. For example, if a clock line and a data line run parallel to each other for more than several inches, and if the

data line cross-couples or superimposes its signal onto the clock line, the device that the clock is driving may detect an illegal level transition.

Methods to reduce crosstalk are straightforward, though not particularly elegant. The coupling can be attenuated by separating the adjacent traces as much as possible. The trouble with this approach is that available board real estate often lim-

creating a stub or a high-frequency antenna.

Another step that can be taken to reduce crosstalk is to lower the impedance of those traces into which crosstalk is especially to be avoided. The lower the impedance that a trace presents, the harder it will be to cross-couple a signal into it.

Even with the use of power and ground planes on a pc board, decoupling capacitors must be used on the V_{CC} pins of every high-speed device. Those devices demand a nearly instantaneous change in current whenever they switch states. Because the power plane can't meet that demand, a high-quality decoupling capacitor is required, otherwise the switching will cause noise on the V_{CC} plane.

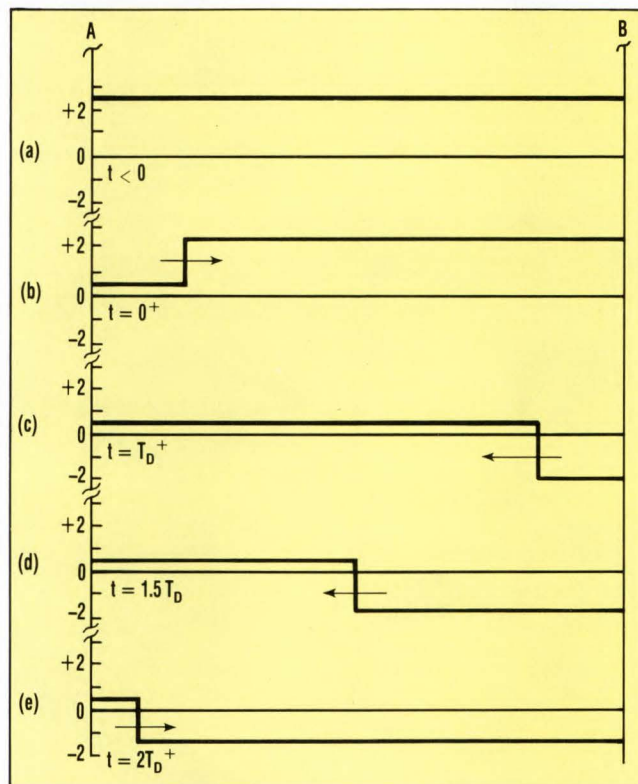
A 0.1- μ F multilayer ceramic (MLC) or other RF quality (low-inductance) capacitor should be placed on every fast-slew-rate device as close to the V_{CC} pin as possible. The commercially available DIP sockets with built-in decoupling capacitors also work well in this application.

Most designers, when they think of loading at all, think in terms of dc loading—traditionally referred to as fan-out and fan-in. But that type of loading rarely presents a problem with today's state-of-the-art logic devices. Much more signifi-

cant when designing with high-speed logic are input and output ac loading.

INPUT CAPACITANCE

Because the input capacitance of a device impacts the overall performance of the logic circuit, it should be examined before a particular device is selected for a design. To ensure specified performance, the total load capacitance that a device drives—including the distributed ca-



3. WAVE PROPAGATION along a transmission line

occurs as follows: Prior to time zero, there is a steady-state voltage of 2.5 V dc on the line (a). At $t = 0$, the voltage at point A drops to 0.5 V, sending a negative pulse of -2 V toward point B (b). At $t = T_D$, that negative pulse is reflected from point B. It adds algebraically to the 0.5 V on the line and sends a -1.5-V pulse back toward point A (c). The reflections then continue as in (d) and (e).

its the possible separation to an inadequate amount.

Ground striping, or shielding, is an effective way to reduce crosstalk and it makes better use of available board area. With ground striping, a ground trace (the stripe) is run between the two parallel traces to act as a shield. If ground striping is used, through holes to the ground plane should be placed every 1 to 1.5 inches along the ground strip to eliminate the possibility of inadvertently

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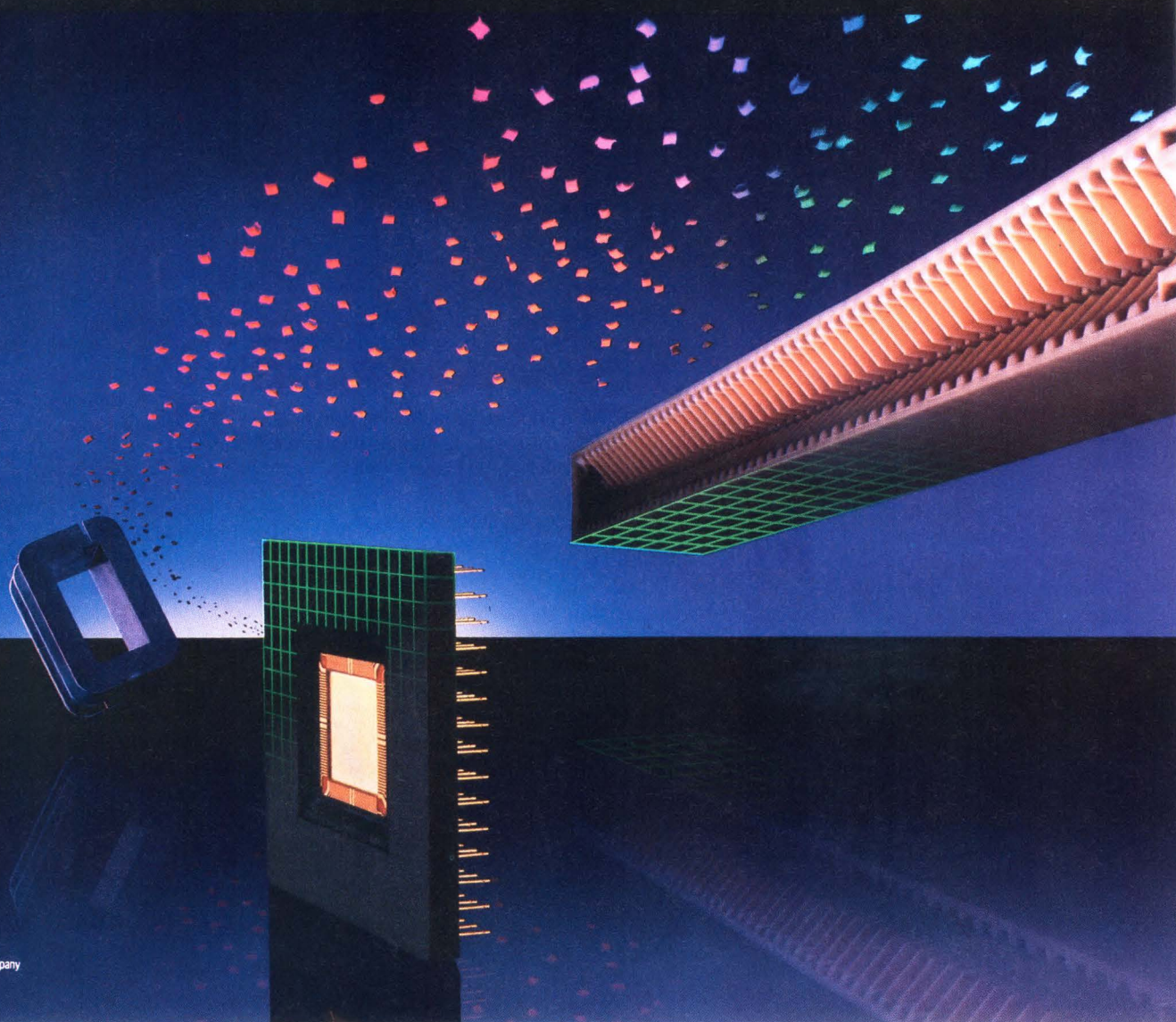
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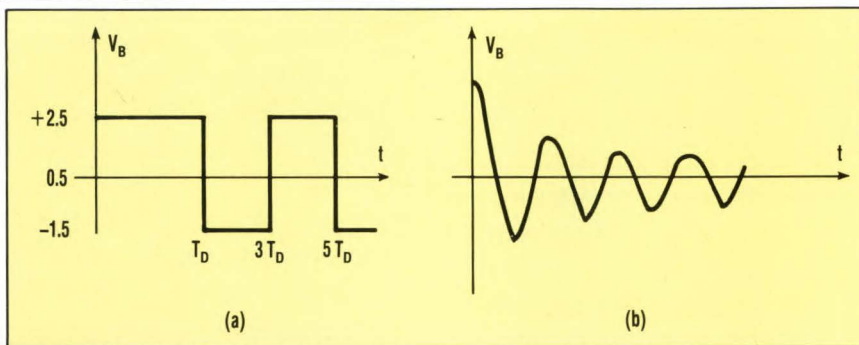
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DESIGNING WITH HIGH-SPEED LOGIC



4. IDEALLY, THE VOLTAGE at point B oscillates forever between +2.5 V and -1.5 V (a). In reality, it will be a damped ringing (b).

capacitance of the trace—shouldn't exceed the device's specified capacitive load. Most high-speed logic devices have a maximum loading of 50 pF. As a rule of thumb, the maximum load on any logic element should be no more than four to six devices for best speed/load performance. However, there are some high-slew-rate devices on the market that have higher output drive capabilities.

BEWARE OF AUTOROUTER

The most common reason for not following the board-layout principles mentioned so far is having an autorouter do the layout. Autorouters do what they were designed to do very well: They place traces so as to make the most efficient use of the pc-board real estate. But most autorouters don't have the capability to determine which devices are high-speed and which are not. This is where the logic designer must step in

and lay out sections, or islands, of high-speed logic by hand in order to avoid the pitfalls of designing with high-speed logic.

TRANSMISSION LINES

In addition to the common-sense layout considerations discussed so far, designers of high-speed systems must have at least a basic understanding of transmission lines and proper termination techniques (see *"Signal Lines Become Transmission Lines,"* p. 76). The reason: As frequencies go up, wavelengths come down to the point where they are of the same order as circuit-board dimensions. Once that happens, any connection between devices should be considered a transmission line. The lumped-element assumption is simply invalid above that point.

The most common consequence of failing to consider the distributed na-

ture of a high-speed logic board is ringing, which is caused by multiple reflections from the ends of unterminated transmission lines. An unterminated line has no load impedance ($R_L = \infty$) and is therefore an impedance-mismatched line. The behavior of this line when connected to a device with a fast slew rate can be understood from the following example: Prior to time zero, there's a steady-state voltage of 2.5 V dc at all points on the line (Fig. 3a). At $t = 0$, an initial TTL voltage transition from 2.5 V to 0.5 V occurs at point A (Fig. 3b). Time T_D later, the signal reaches point B and is reflected by the load reflection coefficient, ρ_L .

The input impedance of the device at point B is very high with respect to Z_0 ; R_L can be approximated by infinity. By plugging into Eq. 2 from the box (p. 76), the reflection coefficient approximately equals +1. In other words, the voltage reflected by the load is equal to the incident voltage (Fig. 3c). The reflected wave passes back along the signal path toward point A (Fig. 3d).

Repeating the calculations for the sending end of the line (point A), where $R_0 \approx 0$, you get a value for the source reflection coefficient, ρ_S , of -1. In other words, there are reflections from the source as well as the load, but the source reflects the inversion of the wave that is incident upon it (Fig. 3e).

Looking just at the behavior of the signal at point B, the single-step volt-

RULES TO REMEMBER

The following ten rules summarize everything the logic designer needs to know when designing with high-speed CMOS.

- 1) Keep signal interconnections as short as possible.
- 2) Use a multilayer PCB.
- 3) Provide ground and power planes. Discontinuities in the planes should be avoided because reflections can occur from abrupt changes in the characteristic impedance.

- 4) Fragment the ground and power planes to supply separate sections for high-current switching devices.

- 5) Use decoupling capacitors on every high-speed logic device (0.1 μ F MLC type) located as close to the V_{CC} pin as possible.

- 6) Provide the maximum possible spacing among all high-speed parallel signal leads.

- 7) Terminate high-speed signal lines where $t_R < 2T_D$.

- 8) Beware of ac loading conditions within the design. Exceeding the manufacturer's recommended operating conditions, especially for capacitance, can cause problems.

- 9) When using parallel termination, put bends in all high-speed signal runs that go to more than one load. Use a termination load at the absolute end of the line.

- 10) Create islands of high-speed devices on the pc board. This simplifies board layout and ropes-off the high-speed areas.

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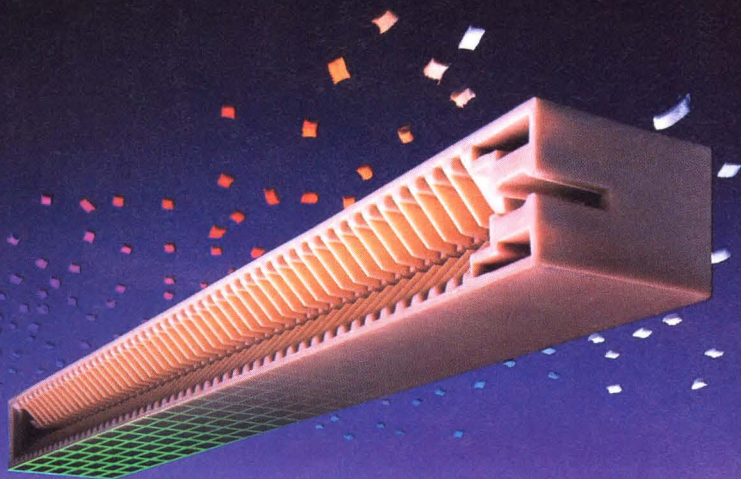
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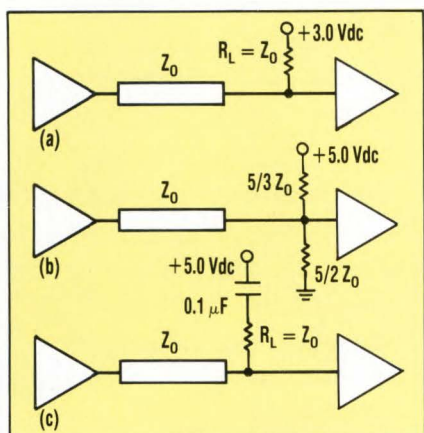
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DESIGNING WITH HIGH-SPEED LOGIC



5. THE BASIC PARALLEL

termination scheme works well but requires a separate 3-V supply (a). The Thevenin equivalent eliminates the need for a separate supply, but dissipates extra power from the regular 5-V supply (b). The use of a capacitor cuts dc dissipation altogether while supplying ac termination (c).

age transition at $t = 0$ leads to an endlessly oscillating signal with a total voltage swing of 4.0 V—twice the original level transition. The voltage doubling comes about because the voltage at point B is the sum of the incident and reflected waves at that point (Fig. 4a). Actually, because of the non-ideal nature of a real circuit board (finite input and output impedances, losses in the transmission lines, and so forth), ρ_L will be less than +1, and ρ_S will be greater than -1. As a result, the reflections will become successively smaller, causing the familiar damped ringing condition (Fig. 4b).

If the ringing amplitude is large enough, it can cause the receiving device to see an illegal level transition and possibly result in spurious logic states occupying the logic design. In some cases, the amplitude of the ringing can actually be large enough to damage the input of the receiving device.

TERMINATE YOUR TROUBLES

The way to eliminate ringing on a transmission line is to terminate the line in its characteristic impedance at either the sending or receiving end. The most common way to terminate a line is with a parallel termination at

the receiving end (Fig. 5).

In the configuration (Fig. 5a), $R_L = Z_0$ and R_L is pulled up to 3 V dc. In principle, R_L could be tied to ground, but TTL-compatible devices could not then supply the necessary drive.

Solving for ρ_L (Eq. 2), it can be seen that $\rho_L = 0$. Terminating a line in its characteristic impedance results in a reflection coefficient of zero, which means that there will be no reflections or distortions on the line. Other than the time delay, T_D , the line will act as if it were a dc circuit. It's important to note that even though devices or gates may be placed at any location on the line, the terminating resistor should be placed at the end of the line. In no case should the line be split like a Tee to feed several devices in parallel (Fig. 6a). Instead, it should be serpentine to feed them sequentially (Fig. 6b).

The 3-V power source shown (Fig. 5a) appears at first to be a major drawback, but R_L and the power supply can be expressed as a Thevenin equivalent running off the system power supply of 5 V dc (Fig. 5b). This variant works well, but the designer should bear in mind that it dissipates additional power.

REDUCING DISSIPATION

A solution that dissipates less power than either of the others uses a capacitor to cut the dc dissipation to zero (Fig. 5c). The recommended capacitor is a 0.1- μ F MLC type. Several manufacturers produce both capacitor-resistor and pull-up/pull-down termination packs. The pull-up/pull-down packs usually come in a single in-line package (SIP) with pins on 0.1-in. centers, while the capacitor-resistor combination comes in a standard 16-pin DIP. The most common SIP pull-up/pull-down resistor values are 220 Ω /330 Ω , 330 Ω /470 Ω combinations.

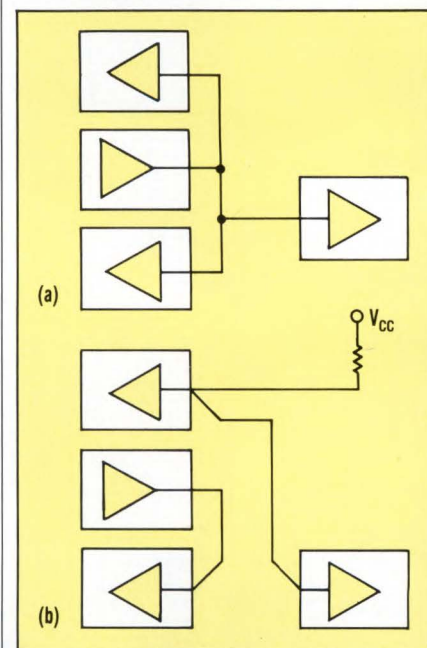
An alternative to a parallel termination at the receiving end is a series termination at the sending end (Fig. 7). The idea behind serial termination is to make $\rho_S = 0$ and $\rho_L = +1$. To do so, R_L is made equal to infinity (left unterminated) and a series resistor is added at the source to make the overall source impedance equal to the

characteristic impedance of the line—that is, $R_S + R_O = Z_{OL}$.

Making $R_S + R_O$ equal to Z_{OL} , of course, creates a voltage divider, which puts half of the signal amplitude across the line and half across the series combination of R_S and R_O . Therefore, with the series termination, the amplitude of the transmitted wave is half of what it would be without the termination.

Interestingly enough, the unterminated receiving end of the line precisely compensates for this halving of the amplitude. The reason is as follows: At the receiving end, the half-amplitude wave is received and a half-amplitude wave is reflected. But bear in mind that those are two separate waves whose amplitudes add at the point of reflection. As a result of this addition, the only thing seen at the receiving end of the line is a full-size pulse.

The main disadvantage of a series termination is that the receiving gate or gates must be at the end of the line—no distributed loading is possible. The obvious advantage of a series termination over a parallel one is that a series termination doesn't



6. SERPENTINING IS essential when terminating a line. Never split the line to feed parallel devices (a). Rather, feed them sequentially with a serpentine line (b).

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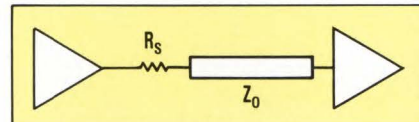


DESIGN APPLICATIONS

DESIGNING WITH HIGH-SPEED LOGIC

require any connection to a power supply.

Transmission-line effects must be taken into consideration whenever line propagation delays get up to the point where a signal transition can be completed before that signal can travel down a line, be reflected, and travel back to its starting point. In other words, lines must be terminat-



7. THE SERIES termination needs no pull-up supply. Its main disadvantage is that it can't handle distributed loads.

ed when,

$$2T_D = T_R$$

CALCULATING DELAY

Taking 2 ns as a typical rise time for a state-of-the-art high-speed logic device, how long can a board trace get before its propagation delay gets to be 1-ns long? For a pc board with a continuous ground plane and a signal trace on the adjacent layer, the propagation delay depends on only one variable, the dielectric constant of the board material. That delay time is given by:

$$t_{PD} = 1.017 (0.475 e_R + 0.67)^{1/2} \text{ ns/ft}$$

For a typical board constructed of FR4 material, e_R (the dielectric constant) is 4.7 to 4.9. If an average e_R of 4.8 is used in the equation, then t_{PD} turns out to be 1.75 ns/ft, which works out to 6.86 in./ns. As a rule of thumb, then, any line that is over 7 in. long should be considered a transmission line and approached accordingly. □

Jock Tomlinson, senior applications engineer at Lattice, holds a BSEE from Colorado State University.

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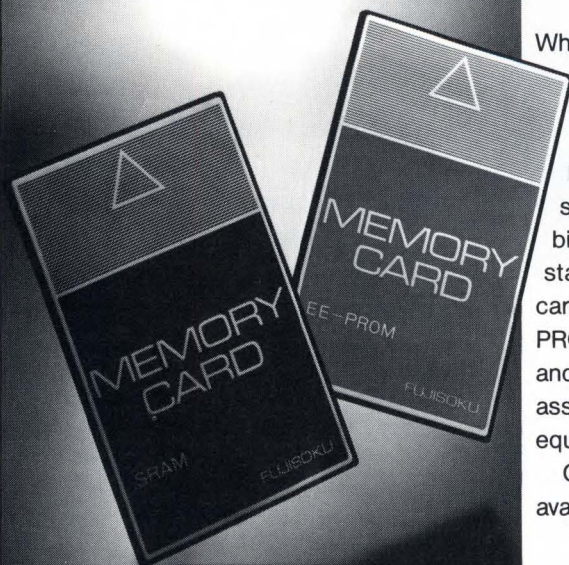
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		40°C	50°C	60°C				QTY. 25	QTY. 100	QTY. 250	QTY. 1000		
2V	±20% ADJ.	60.0	60.0	42.0	4.72 × 3.62 × 7.48	\$475	\$455	\$439	\$360	\$325	\$313	EWS-300-2	
		120.0	120.0	84.0	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-2	
5V	±10% ADJ.	3.0	3.0	1.5	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-5	
		5.0	5.0	2.5	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-5	
		10.0	10.0	5.0	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-5	
		24.0	19.9	9.6	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-5	
		36.0	29.9	14.4	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-5	
	±20% ADJ.	60.0	60.0	42.0	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-5	
		120.0	120.0	84.0	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-5	
	6V	±10% ADJ.	2.5	2.5	1.25	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-6
			4.2	4.2	2.1	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-6
			8.4	8.4	4.2	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-6
20.0			16.6	8.0	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-6	
30.0			24.9	12.0	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-6	
±20% ADJ.		50.0	50.0	35.0	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-6	
		100.0	100.0	70.0	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-6	
12V		±10% ADJ.	1.4	1.4	0.7	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-12
			2.2	2.2	1.1	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-12
			4.4	4.4	2.2	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-12
	10.0		8.3	4.0	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-12	
	15.0		12.4	6.0	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-12	
	±20% ADJ.	27.0	27.0	18.9	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-12	
		53.0	53.0	37.1	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-12	
	15V	±10% ADJ.	1.1	1.1	0.55	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-15
			1.8	1.8	0.9	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-15
			3.6	3.6	1.8	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-15
8.0			6.6	3.2	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-15	
12.0			9.9	4.8	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-15	
±20% ADJ.		22.0	22.0	15.4	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-15	
		43.0	43.0	30.1	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-15	
24V		±10% ADJ.	0.7	0.7	0.35	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-24
			1.2	1.2	0.6	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-24
			2.4	2.4	1.2	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-24
	5.0		4.1	2.0	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-24	
	7.5		6.2	3.0	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-24	
	±20% ADJ.	14.0	14.0	9.8	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-24	
		27.0	27.0	18.9	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-24	
	28V	±10% ADJ.	0.6	0.6	0.3	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-28
			1.0	1.0	0.5	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-28
			2.0	2.0	1.0	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-28
4.3			3.5	1.7	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-28	
6.5			5.4	2.6	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-28	
±20% ADJ.		12.0	12.0	8.4	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-28	
		23.0	23.0	16.1	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-28	
48V		±10% ADJ.	0.35	0.35	0.175	1.38 × 3.82 × 3.54	90	86	83	70	61	55	EWS-15-48
			0.6	0.6	0.3	1.38 × 3.82 × 4.53	120	113	109	94	79	73	EWS-25-48
			1.2	1.2	0.6	1.38 × 3.82 × 6.02	175	168	162	132	113	108	EWS-50-48
	2.5		2.0	1.0	2.13 × 3.82 × 7.87	290	280	270	215	185	175	EWS-120-48	
	3.8		3.1	1.5	2.56 × 3.82 × 7.87	350	340	328	265	228	218	EWS-180-48	
	±20% ADJ.	7.0	7.0	4.9	4.72 × 3.62 × 7.48	475	455	439	360	325	313	EWS-300-48	
		13.0	13.0	9.1	7.48 × 3.62 × 7.87	760	735	710	535	518	503	EWS-600-48	

EWS SERIES

Specifications

DC OUTPUT

Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line 0.4%
regulation, load 0.8% for load changes from zero to full load and from full load to zero. .6% for EWS-300 and EWS-600.
ripple and noise EWS-15, 25, 50: 120mV pk-pk on 5V and 6V models; 150mV pk-pk on 12V and 15V models; 200mV pk-pk on 24V and 28V models; 250mV pk-pk on 48V models.
EWS-120, 180: 150mV pk-pk on 5V and 6V models; 200mV pk-pk on 12V and 15V models; 250mV pk-pk on 24V, 28V and 48V models.
EWS-300, 600: 100mV pk-pk on 2V and 5V models; 200mV pk-pk on 6V through 28V models; 300mV pk-pk on 48V models.
temperature coefficient 0.02%/°C
remote programming resistance 1000Ω/V on EWS-120, 180, 300, 600.
remote programming voltage volt per volt on EWS-120, 180, 300, 600

AC INPUT

line 85-265VAC, 47-440Hz.
85-132VAC/170-265VAC, 47-440Hz (auto selectable) for EWS-300, 600.
RMS current EWS-15: 0.4A RMS max.
EWS-25: 0.6A RMS max.
EWS-50: 1.2A RMS max.
EWS-120: 2.5A RMS max.
EWS-180: 3.9A RMS max.
EWS-300: 3.5A RMS max on 2V models.
7.0A RMS max on all other models.
EWS-600: 7.0A RMS max on 2V models.
14.0A RMS max on all other models.

EFFICIENCY

Typical. 60% on 2V model of EWS-300. 61% on 2V model of EWS-600. 70% on 5V, 6V models of EWS-15. 74% on 5V, 6V, of EWS-25; 12V, 15V models of EWS-15 and 5V model of EWS-300. 75% on 5V, 6V models of EWS-50, 120, 180, 600; 6V model of EWS-300; 12V, 15V models of EWS-25. 76% on 12V models of EWS-50, 120, 180; 24V and 28V models of EWS-15. 77% on 15V model of EWS-50; 24V model of EWS-25. 78% on 15V models of EWS-120, 180; 24V model of EWS-50; 28V model of EWS-25; 48V model of EWS-15. 80% on 12V and 15V models of EWS-300, 600; 24V and 28V models of EWS-120, 180; 28V, 48V of EWS-50. 82% on 24V, 28V, 48V models of EWS-300; 48V models of EWS-120, 180. 83% on 24V, 28V, 48V models of EWS-600.

DC INPUT

110 to 330 VDC on EWS-15, 25, 50, 120, 180.

OVERSHOOT

No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE

Continuous duty from 0° to 60°C with suitable derating (see table). Guaranteed turn-on at -10°C with reduced specifications.

OVERLOAD PROTECTION

External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

HOLD UP TIME

16 msec minimum at 100VAC/200VAC when operating at full load (20 msec on EWS-300, 600 models).

IN-RUSH CURRENT LIMITING

The turn-on in-rush current will not exceed 14 amps peak (25 amps peak on EWS-300, 30 amps peak on EWS-600).

OVERVOLTAGE PROTECTION

Non-crowbar, inverter shutdown type overvoltage protection is standard on all models.

COOLING

The EWS-15, 25, 50, 120, 180 are convection cooled. The EWS-300, 600 are fan cooled.

DC OUTPUT CONTROLS

Simple screwdriver adjustment over the entire voltage range.

INPUT AND OUTPUT CONNECTIONS

All connections are made via terminal blocks. DC output connections are made via studs on EWS-600.

MOUNTING

One mounting surface and one mounting position on EWS-15, 25, 50, 120, 180. Two mounting surfaces and two mounting positions on EWS-300, 600.

REMOTE TURN-ON/TURN-OFF

TTL compatible signal enables remote turn-on/turn-off of the power supply. A voltage of 2.8V to 5.0V applied to remote on/off terminals will initiate turn-off. Open circuit or short circuit condition, or a zero to 2.8V signal will cause turn-on on EWS-300, 600 only.

REMOTE SENSING

Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation for EWS-120, 180, 300, 600.

ISOLATION RATING

3750V RMS input to output (8mm spacing). 2500V RMS input to ground. 500V RMS output to ground.

MONITORING SIGNAL

D.C. Power fail (open collector output) signal available on EWS-300, 600.

EMI

Conducted EMI conforms to FCC Docket 20780 Class A.

PHYSICAL DATA

Package Model	Weight		Size Inches
	Lbs. Net	Lbs. Ship	
EWS-15	0.66	1.00	1.38 × 3.82 × 3.54
EWS-25	0.87	1.25	1.38 × 3.82 × 4.53
EWS-50	1.10	1.60	1.38 × 3.82 × 6.02
EWS-120	2.50	3.00	2.13 × 3.82 × 7.87
EWS-180	2.95	3.50	2.56 × 3.82 × 7.87
EWS-300	6.20	7.20	4.72 × 3.62 × 7.48
EWS-600	10.00	11.00	7.48 × 3.62 × 7.87

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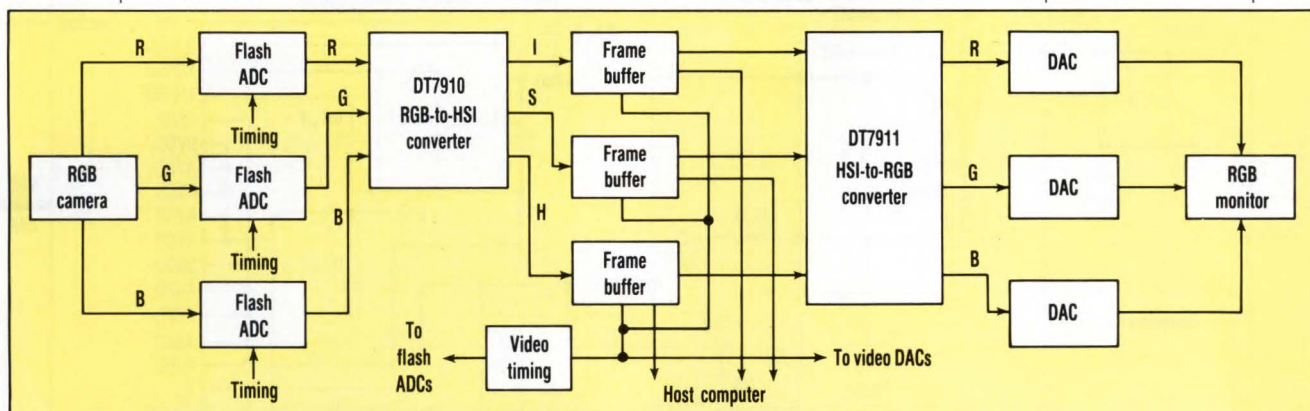
TWO DEDICATED CMOS ASICs, RUNNING AT
REAL-TIME VIDEO RATES, ANCHOR
A COLOR-VALUE-CONVERSION CIRCUIT
THAT ENHANCES IMAGING CAPABILITIES.

DESIGN COLOR IMAGING INTO ANY GRAPHICS SYSTEM

Despite the ease with which digital technology generates clear, sharp color pictures on display screens, high-quality color imaging remains an elusive goal for many computer-graphics systems. Technique, rather than cost, is a major reason. In fact, most of today's color-image processing

is mired in 50-year-old methods developed for the first color-TV cameras and monitors. Those methods depend on the well-known RGB color values. Unfortunately, the RGB color-value method fares poorly because of the extensive data processing needed to analyze color data and generate graphics images.

RGB's successor is a little-known but well-developed color-value system called hue, saturation, and intensity (HSI). HSI offers two significant advantages over RGB: perception and processing. Human perception isn't adapted to understanding color in terms of relative proportions of red, green, and blue light. Rather, people perceive color in terms of its hue or actual color (red, orange, brown, and so forth); its saturation or vividness (the more vivid, the less



1. ADVANCED COLOR-IMAGE PROCESSING requires the conversion of the RGB color space to the HSI color space by the system shown here.

BERNADETTE MORRISSEY-GOLAS

Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752-1192; (508) 481-3700, ext. 556.

DESIGN APPLICATIONS

REAL-TIME COLOR IMAGING

white in the color); and its intensity, or relative brightness or darkness (no color attributes at all).

From a data-processing standpoint, it's simpler and faster to manipulate and operate on HSI data. For example, almost all RGB operations require the values of all three colors to be processed simultaneously. With HSI, most operations involve a simple alteration of one value, because they are independent of each other.

By changing one HSI value, a color image can be altered significantly. For example, to change an object's color from orange to purple requires adjustment of only the hue value, not three values as in RGB. Likewise, the intensity or softness of a color can be increased or decreased by adjusting only the saturation value. Because only one value is changed, HSI takes far less processing time than RGB.

With HSI color-data processing, sophisticated graphics subsystems can be designed to interface with moderately priced (under \$10,000) personal computers and workstations. Under the constraints of RGB processing, it takes powerful, expensive computers to produce results of similar quality. As it migrates to lower-end computer platforms, image-

processing technology is seeping into diverse application areas (*"Image processing is finding niches," opposite*).

To implement an HSI color-processing system, there are two prerequisites: The color information must be translated from the RGB format into HSI parameters, and its processing must be performed through specialized hardware and not software. Working in RGB eats up time and computations because a computer must manipulate three separate color values. Moreover, if RGB and HSI conversions are made through software algorithms executed by a PC, the system can't possibly produce real-time images on a display.

Memory considerations dictate many of a real-time frame grabber's architectural features. At least one frame's worth of memory should be located on or very near the image-processing board. Depending on system requirements, a second frame buffer can process image data while the first buffer displays its contents on the monitor.

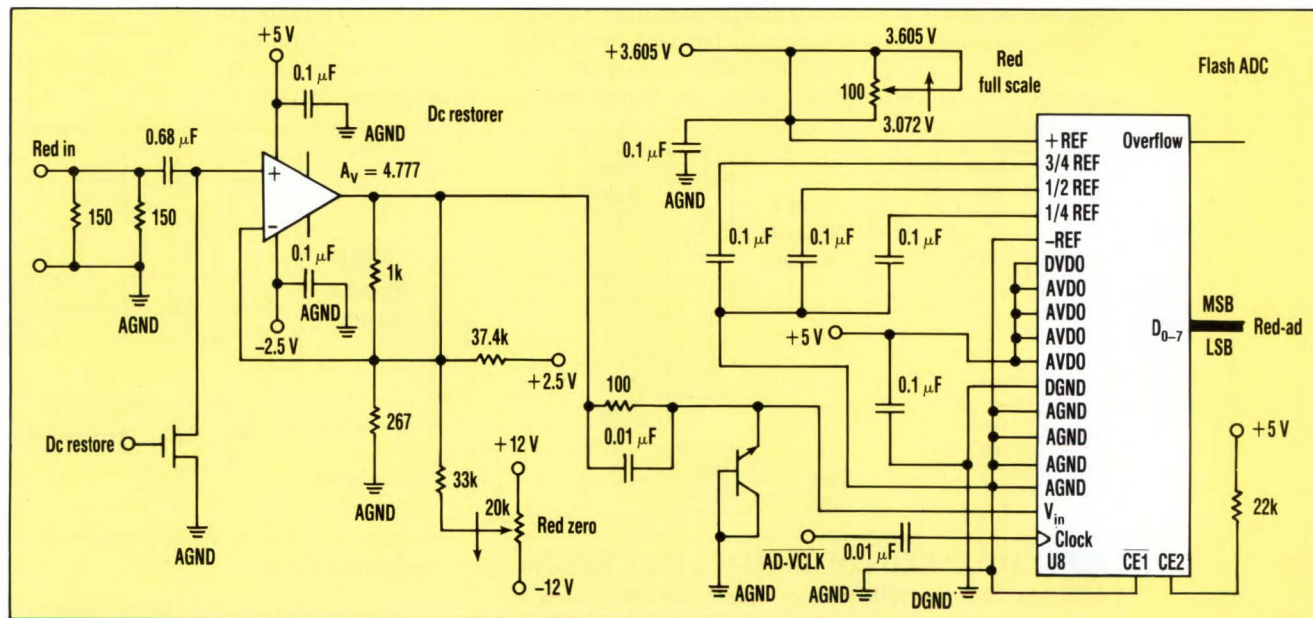
Production of real-time color images calls for a CPU with much higher performance than those found in PCs. But even if the CPU were fast enough, PC buses don't have enough

data-transfer bandwidth to accept frame-buffer data at the rate necessary for real-time operation. The PC/AT bus, for example, has a maximum transfer rate of 200 kbytes/s. Displaying images at 30 frames/s requires a 10-Mbyte/s transfer rate.

Low-cost, real-time color imaging is possible only if performed in the HSI domain using dedicated hardware. But the lack of sufficiently fast hardware to convert from RGB to HSI and back has been the bane of real-time color-image processing. A pair of specialized CMOS ASICs from Data Translation handles RGB-to-HSI and HSI-to-RGB conversion at the video rates required for real-time imaging.

The DT7910 (RGB-to-HSI) and DT7911 (HSI-to-RGB) converter chips form the core of a color-image subsystem that accepts color data from an RGB camera, VCR, or other input device and delivers color data to a standard RGB monitor (*Fig. 1*). The system is essentially the image-processing portion of a frame grabber that captures color images and converts them into a complete frame of video information in real time (1/30-second or 30 frames/s).

A frame grabber can be purchased as a complete turnkey, board-level system that contains all the image



2. THE INPUT PORTION of the system digitizes RGB analog signals in flash A/D converters after first performing the dc-restoration function through the input op amps. Each camera input (R, G, B) goes through a circuit identical to the one shown.

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grabbing, processing, and display circuitry, as well as computer communications on a pair of boards. It can also be designed for a specific application in a new system or to enhance an existing system. An example of the former is Data Translation's DT2871 (HSI)Color frame grabber, which plugs into IBM PC/AT computers and compatibles to perform color processing (ELECTRONIC DESIGN, Jan. 12, p. 147).

Designers can build the less-costly, application-specific version with the two converter chips. Moreover, this version operates with simpler software for PCs or scientific workstations. The resulting subsystem is compatible with any computer bus. Not only that, it's far more capable than boards that simply capture RGB signals for color databases. In addition to picture enhancement, the HSI format's digitization makes it possible for color data to be manipulated by arithmetic and logic operations, filtering, histogram generation, and other functions.

DESIGNING A GRABBER

Red, green, and blue analog video-input signals from an RGB camera are fed into three op amps that perform the dc-restoration function (Fig. 2). Dc restoration reestablishes the dc and low-frequency components of the display signals, which are suppressed by ac coupling of the signals into the op amps.

RGB-input signals must conform to the widely used EIA RS-170 standard for monochrome-display signals. Even though RS-170 defines standards for monochrome signals, it's equally valid for RGB color signals. RS-170 signals contain lines of monochrome video information and synchronization (vertical and horizontal) timing data. The RS-170 signals produce a TV frame consisting of two fields of horizontal image lines. The odd field comprises all odd-numbered lines and the even field all even-numbered lines. Horizontal sync pulses synchronize the start of each line while vertical sync pulses synchronize each field. Displaying alternate odd and even fields at a rate of 60 fields/s yields a complete,

interlaced image at the real-time viewing rate of 30 frames/s.

The RGB analog outputs of the dc-restoration amplifiers are sent to three identical 8-bit flash analog-to-digital converters (Fig. 2, again). These devices establish the range of values that represent the range of intensities, or gray or brightness levels, for each picture element (pixel). An 8-bit converter, for example, produces 2^8 (256) gray-level values. The brightness ranges from shades of gray to pure black and pure white.

In digitizing the RGB signal, each video frame is divided into a fixed

number of rows, each of which contains a fixed number of pixels. The a-d converter divides the input image into a grid (usually 512 by 512) and assigns each pixel a brightness level as it is digitized. A frame grabber's spatial resolution and brightness-level resolution are often described in one specification, such as 512 by 512 by 8.

A video-speed a-d converter is mandatory for a frame-grabber application. An RS-170 signal gives the converter just 59.52 μ s to sample each line. During this time, a 512-by-512-pixel grabber must be able to

IMAGE PROCESSING IS FINDING NICHES

What are some of the applications that image processing addresses? First, the quality of an image can be enhanced aesthetically and objectively. Aesthetic enhancement makes the image more pleasing, while objective enhancement yields more information through spatial or contrast adjustment. For example, spatial enhancement alters the image's detail using edge enhancement. Contrast enhancement alters the image through changes in brightness.

A more important end product of image processing is the analysis of graphic or numeric data obtained from an image. One of the more common image-analysis tools is the histogram, which graphically represents an image's dynamic range with respect to contrast and brightness. An advantage of hue analysis by histogram processing is high immunity to intensity variations caused by changes in lighting. An application of this histogram is in color-quality inspection, such as the grading of fruits and vegetables, or paint

and color-print control.

Another application made easier by HSI parameters is image filtering to improve picture quality. High-pass filtering, for example, can make it easier to see small variations in an image while low-pass filtering can diminish features to make the overall shape of objects more apparent. Laplacian edge enhancement, which amplifies high frequencies while removing low frequencies, is a particularly good method for locating boundaries between objects.

Color-image processing is just now reaching a wide variety of applications in factories, laboratories, publishing, and other areas.



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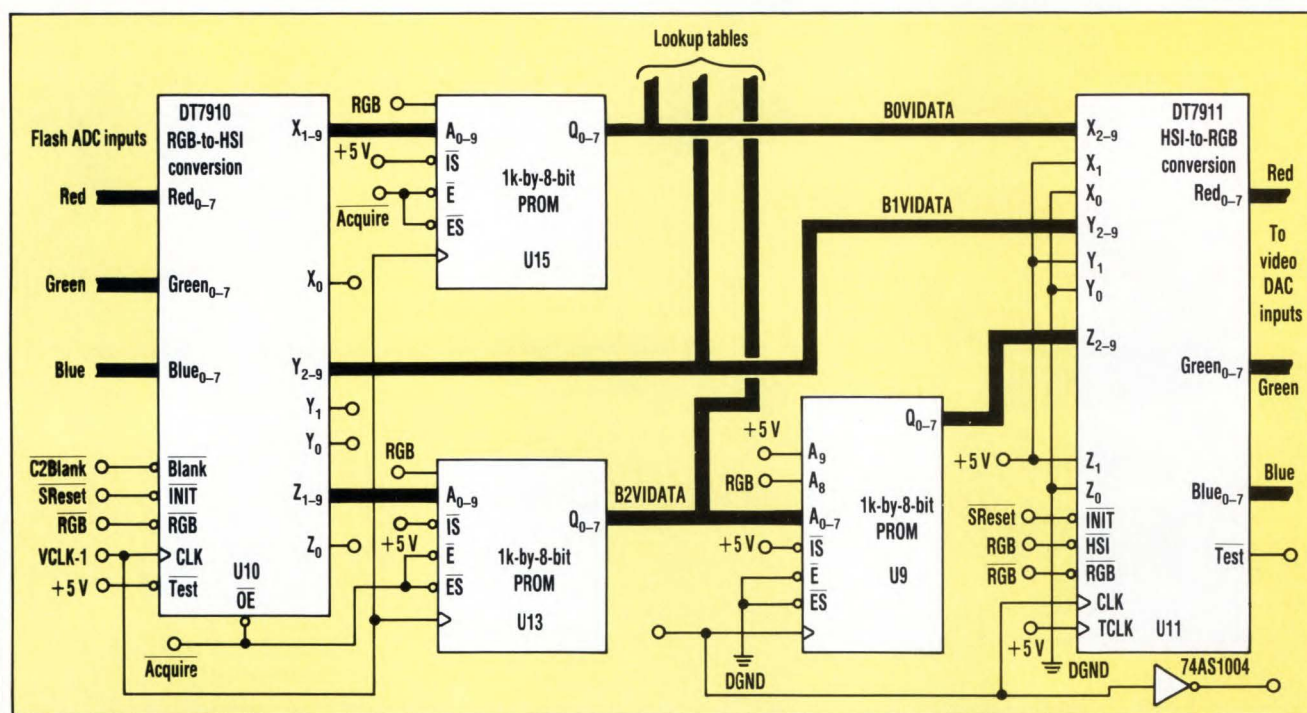
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3. TWO DEDICATED CMOS ASICs (the DT7910 and DT7911) and three PROMs programmed as look-up tables (LUTs) perform all of the real-time RGB-to-HSI and HSI-to-RGB conversion functions in the frame grabber. Pixel data from the outputs of the DT7910 and LUTs U13 and U15 are stored in a frame buffer for further processing.

convert 512 analog values to digital pixels. To do so, the a-d converter must have a throughput of at least 10 MHz. Clock signals feeding the converter (AD-VCLK) must be 10-MHz signals. The clock-generation circuit usually includes a phase-locked loop (PLL) to align the timing of the grabber board with that of the incoming video signal. A PLL can lock onto the video signal's stable horizontal and vertical sync pulses to generate timing pulses for the grabber.

Eight-bit digitized RGB outputs from the flash converters go directly to a DT7910 RGB-to-HSI converter chip (U10), as illustrated in the frame grabber's second stage (Fig. 3). Eight bits each of red, green, and blue pixel values are converted in the DT7910 into 8 bits each of hue, saturation, and intensity data values for storage or further processing.

The DT7910's sister chip, the DT7911 (U11), converts the values from HSI back to RGB. The RGB outputs from the DT7911 go to three video-speed digital-to-analog converters, where they are changed back into analog values suitable for

driving an RGB monitor.

Both the DT7910 and DT7911 are high-speed, low-power CMOS ASICs that implement trigonometric algorithms. These algorithms are executed at the 15-MHz pixel-throughput rate required to deliver real-time (30 frames/s) video operation. Thanks to a pipelined architecture, several arithmetic operations take place simultaneously, which accelerates the throughput rate. The most difficult function in the conversion process is dividing one variable by another. To achieve real-time conversion, Data Translation developed a proprietary floating-point-division algorithm for the DT7910, which executes at the 15-MHz rate.

Note that three devices—U9, U13, and U15—interface to the converters. These are 1k-by-8 look-up-table (LUT) memory devices that complete the conversion process. Two LUTs (U13, U15) are required by the DT7910 to convert intermediate intensity and hue values into their final form. The DT7911 uses a hue-value LUT (U9) at its input to convert the DT7910's hue-LUT data into an inter-

mediate form before conversion. The LUTs are available from Data Translation preprogrammed with the conversion information, or they can be supplied by the user. Each device is a Cypress Semiconductor 8-kbit PROM packaged in a 24-pin DIP. The Data Translation LUTs are the DT7970 (U15), the DT7971 (U13), and the DT7972 (U9) 8-kbit PROMs.

LUTs allow for pixel-point processing, a procedure that alters the value of individual pixels in an image. A LUT can add, subtract, multiply, or divide pixel values to produce an output for further processing. LUT outputs can represent results, mathematical functions, or arbitrary data values.

After power is applied to U10, the device must be initialized to reset all internal registers in the pipeline. Initialization is accomplished by pulling the INIT line low for at least 1.5 clock cycles and returning it to a high level. The device can operate as an RGB-to-HSI converter or it can be bypassed. In bypass mode, RGB data passes through without conversion. A high level on the RGB input selects

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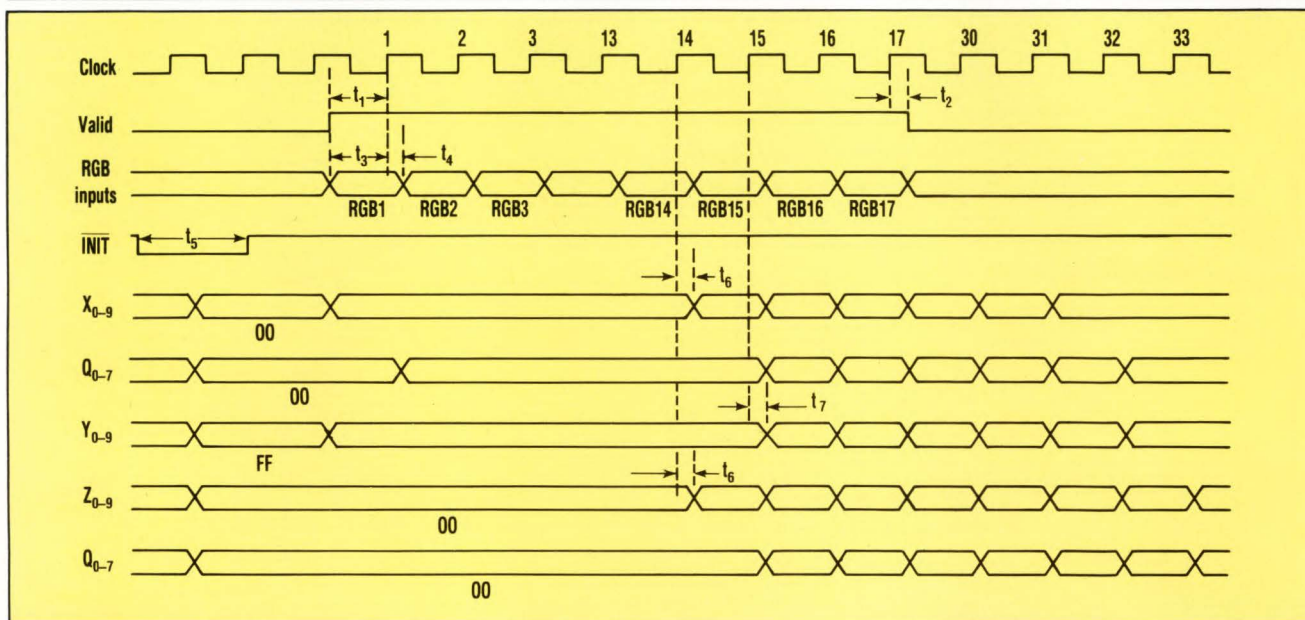
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REAL-TIME COLOR IMAGING



4. CONVERTING RGB TO HSI VALUES occurs at a 10-MHz clock rate to supply a real-time (30-frame/s) display image. After an initial delay of 15 clock cycles, the HSI data outputs are continuous in time.

the conversion mode, while a low level selects bypass.

Following initialization, all X_{0-9} (intensity) and Z_{0-9} data (hue) lines are cleared (logic 0), while the saturation-output lines, Y_{0-9} , are set to logic 1. Once a signal is applied to the clock input, the output data will begin to change state. The DT7010's throughput rate equals the clock rate; the minimum clock-pulse width (high or low) is 15 ns and the maximum frequency is 15 MHz.

It takes 14 clock cycles for output-pixel data to appear on the X_{0-9} and Z_{0-9} lines (Fig. 4). The delay from RGB inputs to output data on the Y_{0-9} lines is 15 clock cycles. Besides performing conversion operations, the LUTs introduce a delay of one clock cycle to align the H, S, and I values after a conversion. This can be seen in the Q_{0-7} outputs from U13 and U15 (Fig. 4, again). Once the initial 15-clock-cycle delay has occurred for the first group of RGB inputs, new HSI data values emerge from the RGB-to-HSI conversion process at the clock rate.

Operations in the DT7911 HSI-to-RGB converter (U11) are very similar to those in the DT7910. The initialization procedure is the same and the device can be run in either an HSI-to-RGB conversion mode or a bypass

mode. Following initialization, all Output-Data lines (Red_{0-7} , $Green_{0-7}$, and $Blue_{0-7}$) are reset. When a clock is applied, output data begins to change state.

In total, nine clock cycles are needed to convert HSI data back into RGB form suitable for output to high-speed d-a converters. Intensity (X_{0-9}), saturation (Y_{0-9}), and an intermediate value of hue data that come through a LUT (U9) into the Z_{0-9} inputs are converted by the 7911 into RGB format. After the initial nine-clock-cycle delay, new data values emerge at the clock rate.

Three 8-bit video d-a converters take the red, green, and blue digital outputs from the DT7911 and convert them into analog values suitable for driving an RGB monitor. The converters' relative output levels determine the color and intensity of each pixel. Embedded within the d-a converter's outputs are vertical and horizontal sync signals that conform to the RS-170 standard. Images appear on the display screen in real time.

The color-imaging system described takes RS-170 RGB data from a color camera and delivers RGB data enhanced by HSI processing to a color monitor. To take full advantage of the digitized HSI information, however, it must be manipulat-

ed by a high-performance processor.

For a computer to operate on HSI data, the information must be stored in a memory. HSI outputs from the DT7910 converter and its two LUTs are fed to a large memory array. This array is called a frame buffer, because it stores pixel data for a complete display frame.

A frame buffer for a 512-by-512-by-8 image-processing system requires 256 kbytes to store the information for each of the three data variables. If each 256-kbyte array is implemented with 256k-by-1 dynamic RAMs, it takes eight dynamic RAMs to store the data for one variable and 24 dynamic RAMs to store the data for all three variables. □

Bernadette Morrissey-Golas is a product-marketing manager for Data Translation's scientific-imaging and array-processing products on the PC/AT, Qbus, VME, and PS/2 platforms. She holds degrees in computer science and marketing from Bridgewater State College, Bridgewater, Mass.

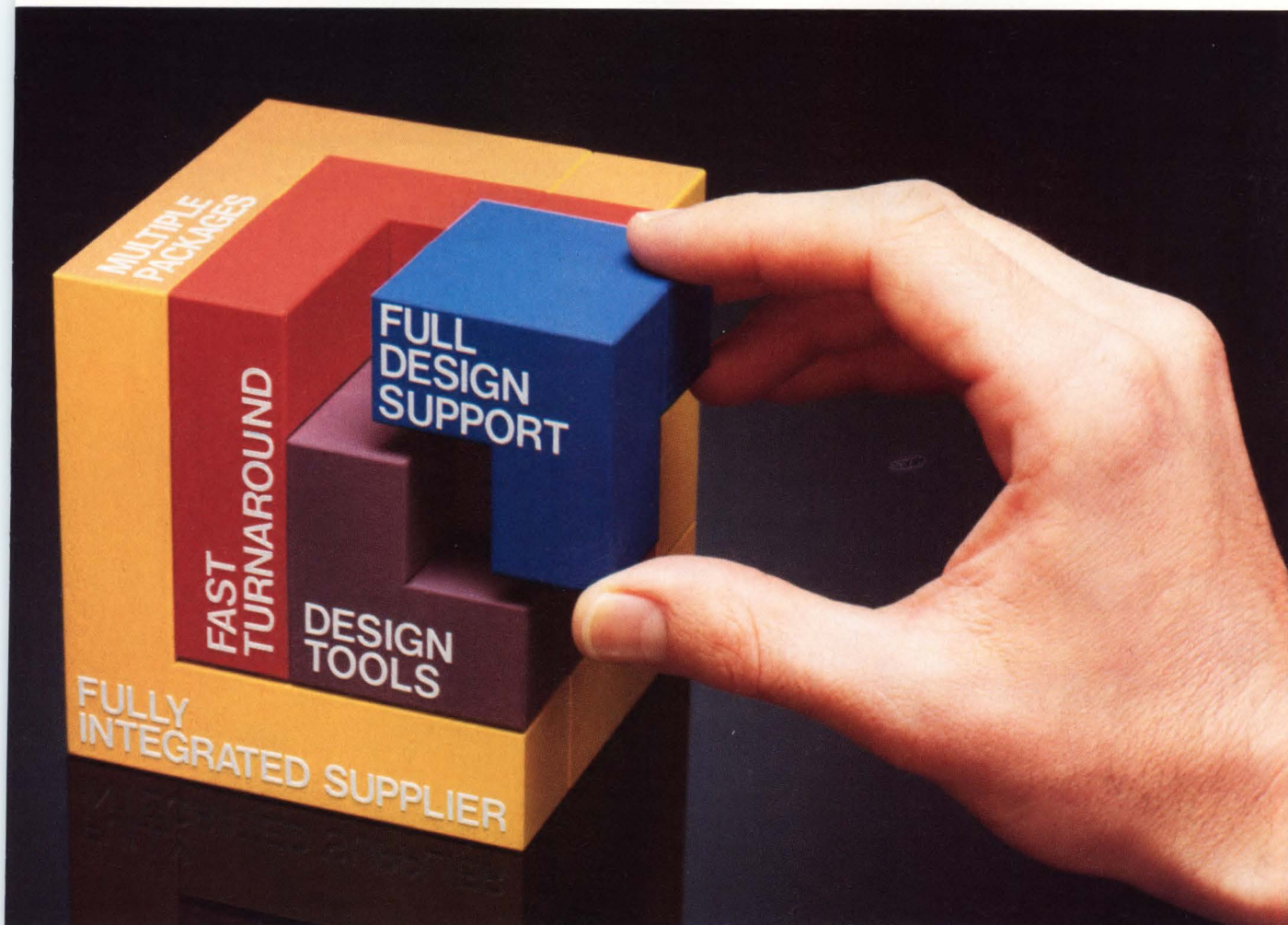
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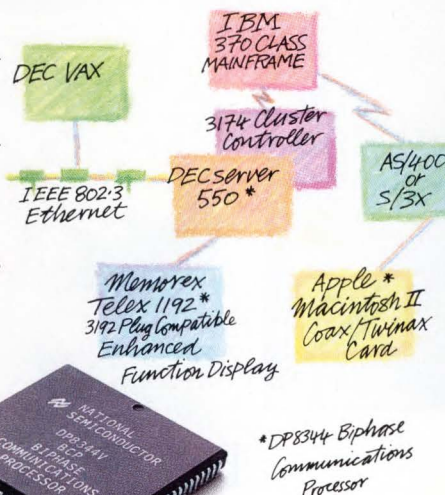
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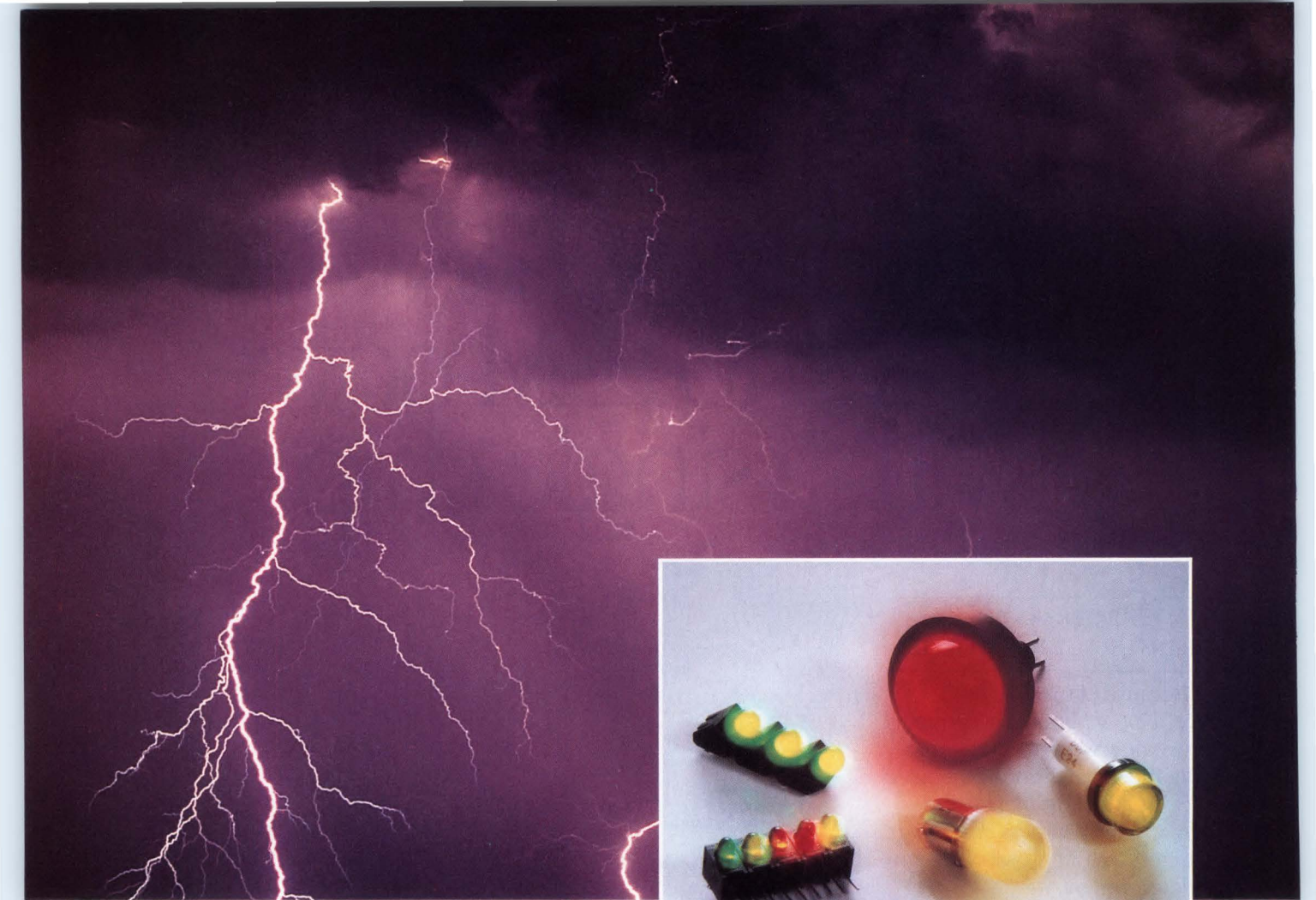
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OPTIMIZE DATA FLOW IN DSP IMAGING APPLICATIONS

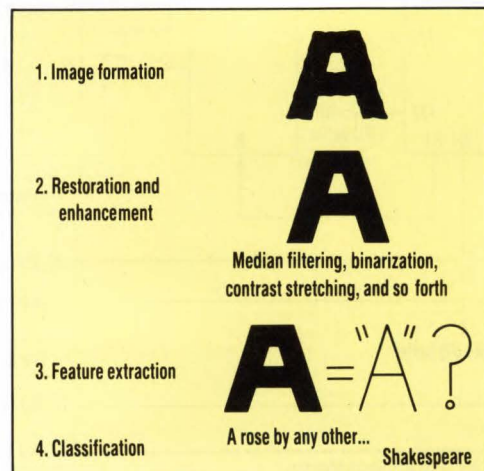
BY CONTROLLING
THROUGHPUT BETWEEN
PROCESSING STAGES,
MICROSEQUENCERS
OFFLOAD THE SIGNAL
PROCESSOR.

Digital image processing encompasses many applications, ranging from satellite image processing and medical imaging to such traditional areas as radar and sonar. These applications transform a two-dimensional representation of an image into a more desirable form with digital-signal processing. But DSP imaging speed is often limited by the data throughput of the system.

Data throughput can be improved with intelligent microsequencers, which supply a fast, compact, low-power control element in the data path to offload data-housekeeping tasks from the digital-signal processors. In addition to controlling data flow, the microsequencers relieve the DSP processors of synchronization and FIFO-buffer error-condition checking.

A typical imaging application needs four operations (*Fig. 1*). The first is image formation. An image is represented by a quantity given to each picture-element or pixel. This image can be represented by the absorption characteristic of body tissue (for x-ray imaging), a temperature profile of a region (infrared imaging), or the

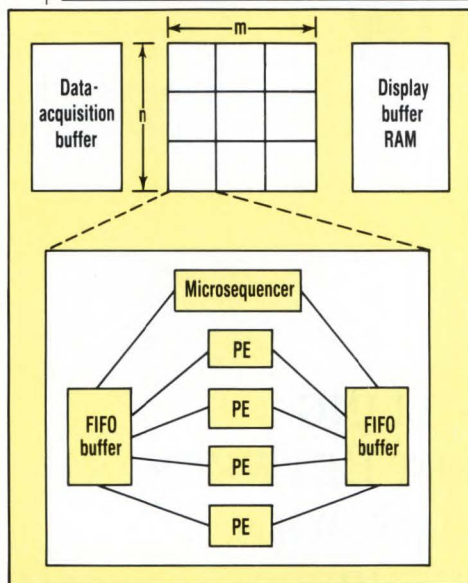
1. A TYPICAL DSP imaging system has four distinct stages: image formation, image restoration and enhancement, feature extraction, and classification. This example shows the four stages of a text reader.



DAVID CREAMER AND MICHAEL K. WEBB

Altera Corp., 3525 Monroe St., Santa Clara, CA 95051; (408) 984-2800.

MICROSEQUENCER-BASED DATA CONTROL



2. PROCESSORS ARE arranged as a matrix. A microsequencer controls the parallel and pipelined data flow of the system array, and the parallel data flow within a particular cell.

brightness of objects in a particular cross-section (a picture taken by a camera).

The image under analysis is sampled and quantized. The sampling rate, which is determined by the image's bandwidth, must be high enough to capture the useful information in an image. The sampled image is quantized into a finite number of gray levels by an analog-to-digital conversion. Each pixel is assigned a value based on the average level of gray contained within its area.

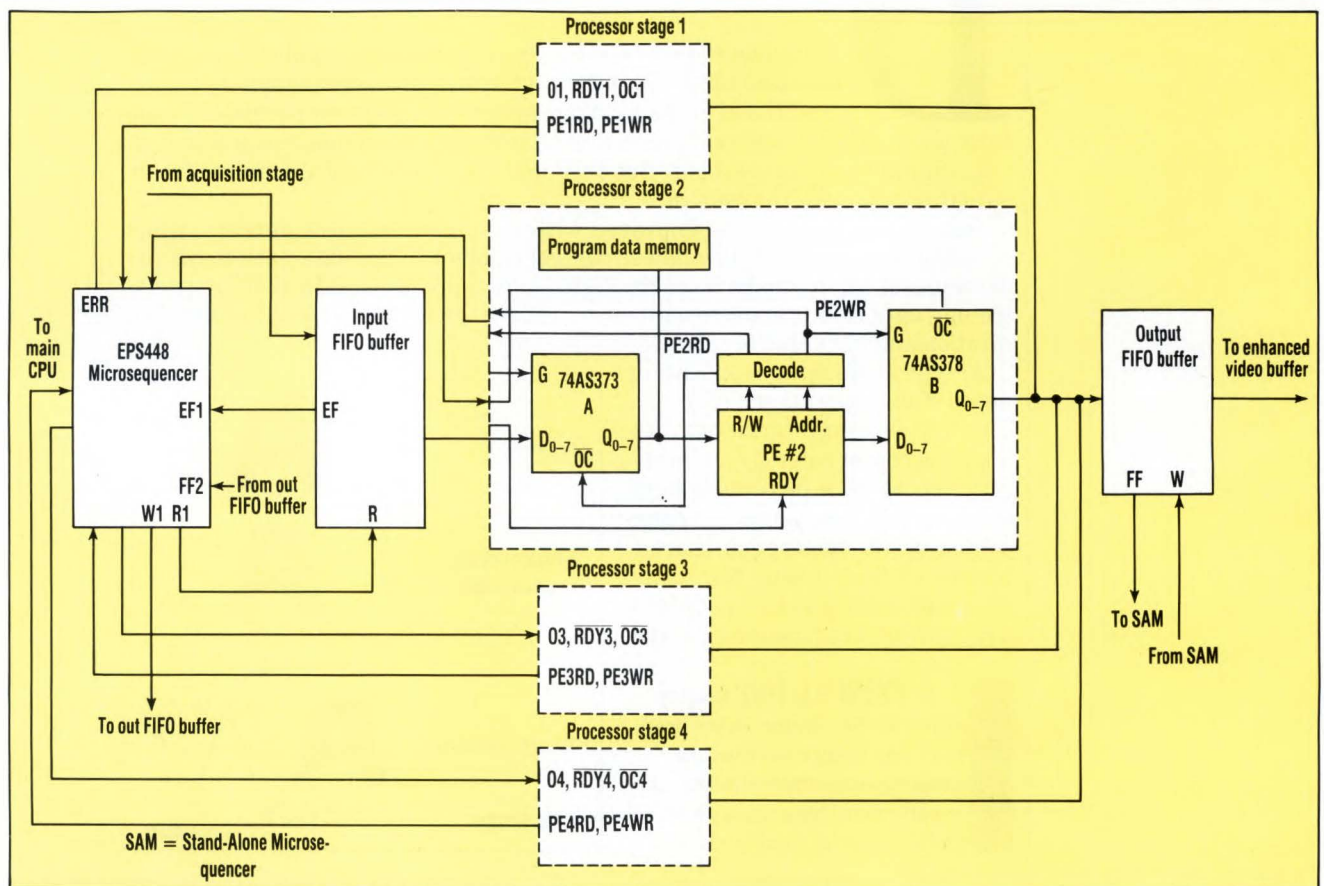
After the conversion, the image is enhanced and restored. In image enhancement, particular features of an image are emphasized. A quantitative model performs special tasks, such as contrast stretching (where gray levels in a small region are stretched to occupy a larger region) and median filtering (where each pixel is replaced by the median pixel value in its immediate area). These

techniques don't generate new information on an image but instead emphasize particular image characteristics.

Image restoration is the process of approximating an image with known problems, such as blurring and bad focusing. Unlike image enhancement, image restoration is more subjective and doesn't depend on specific quantitative analysis.

Other processing involves feature extraction and object classification. During these stages, pixels are grouped with their local neighbors to create small subwindows, varying in size from 3-by-3 to 64-by-64 pixels. Real-time calculations are required to measure such features as edge density and variance, and they're also required to create histograms.

Real time refers to the ability to digitize, process, and display signals at standard video rates without any perceivable delay due to the DSP



3. THIS MODULE CONSISTS of four processing elements. The microsequencer controls the writing and reading into the 74AS373 latches to properly distribute data to the elements, and performs error checking for the system.

MICROSEQUENCER-BASED DATA CONTROL

processing overhead. To do this, feature-based image classification requires large amounts of throughput, which are related to the subwindow size. A typical television quality image—512-by-512 pixels—and a frame rate of 30 frames/s results in a sampling rate of about 10 MHz. This means that during the feature extraction stage for a subwindow of only 3-by-3 pixels, a memory access rate of 10^8 /s is required.

THE SYSTOLIC APPROACH

An important ingredient in real-time image analysis is data throughput, and fast throughput can be acquired through many methods. One approach is using the systolic system, in which a set of regularly interconnected cells is formed, and each processing element (PE) is dedicated to perform a particular task. Data flows between cells in a pipelined manner, and communication with the outside world occurs only at the boundary elements. Each stage of the pipeline has its own data storage instead of using global memory. The goal is to make it possible for the cascaded processors to store data between processor stages so that new data can enter the pipeline as previous data is processed. The speed of the individual processors plus the number of stages in the pipeline is the critical performance factor.

In addition to pipelining the data, other techniques are also used to increase system throughput. The pipelined processors are often expanded into a processor matrix by adding parallel processors (*Fig. 2*). In this way, similar data elements, such as blocks of pixels, are processed synchronously in parallel to increase system throughput. Processor matrices, however, increase system performance but complicate the data-management task.

The need for speed has resulted in dedicated DSP processors, such as Texas Instruments' TMS320 family. System data-flow design is critical to system performance, particularly in a heavily pipelined system. Ideally, the system's data flow should continue automatically without involvement from the PEs. This minimizes

the housekeeping overhead on the processor elements, and maximizes useful imaging cycles.

Data flow between processing stages can be handled by software or hardware. Software is used if data rates are slow enough. Software polls the status of the processors to determine when they're ready to accept or generate data. But this severely hampers system performance and is fading from use in favor of interrupt driven approaches.

Hardware interrupts are another approach that's often used by general-purpose systems. However, this approach also requires significant software overhead to call and service interrupt routines, and then to restore the processor to its original task. This overhead is multiplied in a multiprocessor DSP system and becomes unacceptable.

An ideal system would use the processors exclusively to perform the necessary algorithms with no time

wasted on handshaking. But until the advent of fast microsequencers, this approach was costly because it required significant amounts of hardware to synchronize the processors. Microsequencers implement this approach with significantly less hardware.

To supply a transparent interface between processors, data buffers (RAMs, FIFO buffers, register files) absorb the data output by one processor when the following processors in the chain aren't ready to accept incoming data. For example, a parallel engine element can consist of four processors in parallel, sharing common input and output FIFO buffers (*Fig. 2, again*). This structure can be expanded in both the m and n directions to tailor it to individual applications.

A processor module contains an input FIFO buffer, four PEs, an output FIFO buffer, and an Altera EPS448 microsequencer to control

SAM: A STANDALONE MICROSEQUENCER

Altera's EPS448 Stand-Alone Microsequencer (SAM) has a generic microcoded architecture to implement a broad range of controllers. These controllers range from basic state machines to complex microcoded controllers.

The architecture includes a 448-by-36-bit EPROM that stores 448 unique states. Among the 36 bits, 16 are dedicated to define that state's outputs and the other 20 are internal control signals. Also contained within the EPS448 microsequencer are 768 product terms that determine next-state information.

An 8-bit down counter, a 15-bit deep stack, and a 36-bit pipeline register are also contained within SAM's 28-pin package. Built in a 1.0- μ m CMOS EPROM technology, SAM operates at a 30-MHz clock frequency while enjoying the benefits of low power consumption.

The standalone microsequencer's counter is a down

counter used for timing loops. The counter value can be loaded from various internal locations and can be accessed by the stack. A zero flag indicates when the down counter has reached zero, and is used with the LOOPNZ command to control program flow.

The stack is a last-in-first-out arrangement used to perform subroutines, nested loops, and other iterative structures. In addition, inputs can be pushed onto the stack to perform dispatch routines. The 36-bit pipeline register synchronizes the internal signals and allows SAM's outputs to be tri-stated.

Ten of the microsequencer's 28 pins are inputs and 16 are dedicated outputs. If more than eight inputs are required, external logic can be used to reduce the number of signals. If an application requires deeper microcode EPROM (more states) or more outputs, multiple SAM devices can be cascaded vertically and horizontally, respectively.

MICROSEQUENCER-BASED DATA CONTROL

the data flow (see "SAM: a standalone microsequencer"). Each PE in this example handles a portion of image enhancement. The PEs share input and output FIFO buffers to absorb incoming and outgoing data (Fig. 3). The buffers each have a 74AS373 latch on the input and output processing-element buses to latch incoming and outgoing data.

Altera's EPS448, Standalone Microsequencer (SAM), controls the writing and reading into and out of the latches to properly distribute the data to the PEs, and performs error checking for the system. The microsequencer handles all of the data transfers between the four processor elements—including full error checking—to offload the task from the DSP engines.

The first step in handling the data

flow is to manage the FIFO read and write cycles (Fig. 4). A TMS32020 digital-signal processor is used here, though any processor is acceptable. This processor has two output clocks: CLKOUT1 and CLKOUT2. Both output clocks have 200-ns periods, with CLKOUT2 lagging by 50 ns. Another output from the processor is $\overline{\text{STRB}}$, which is in sync with CLKOUT2. Its rising edge determines when a read or write is complete.

Other relevant processor outputs are the address and R/W signals. These signals are issued 20 ns prior to $\overline{\text{STRB}}$ going low. The R/W signals are decoded to generate PE2RD and PE2WR. These are input signals to the microsequencer that indicate when a read or write was requested.

To get the second processor to

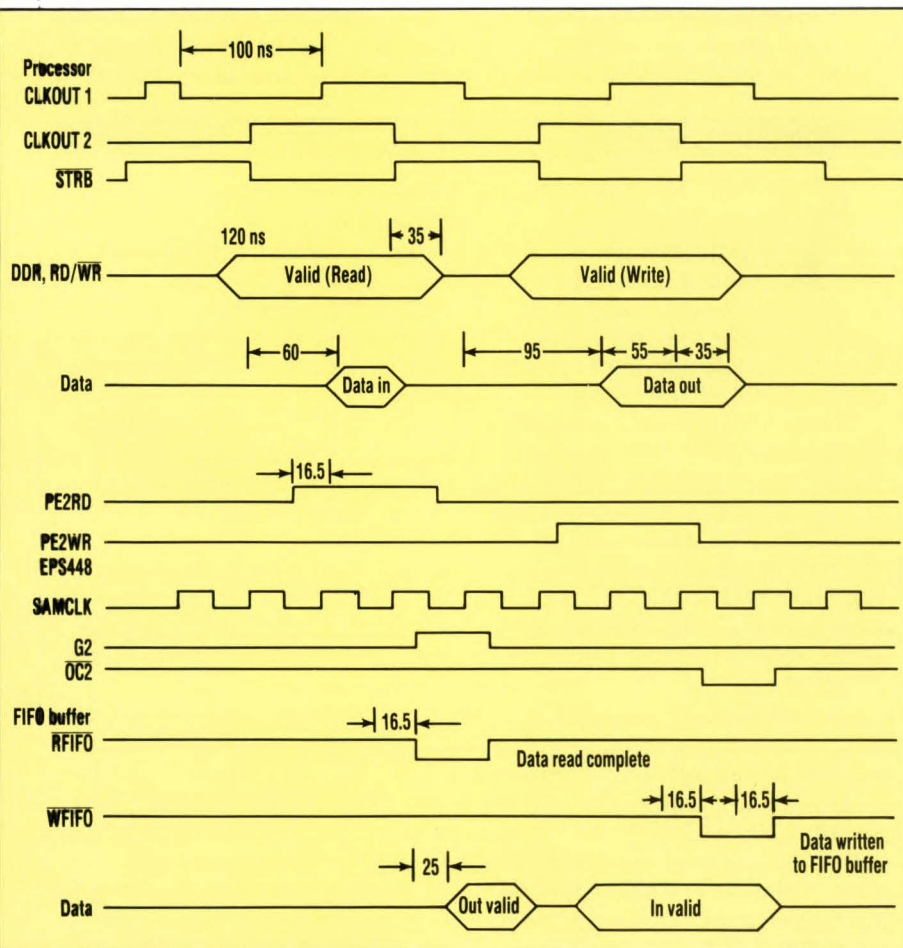
read data, a two-phase read cycle occurs. First, the processor reads the data on its input latch. Then the A-latch's output is enabled, the processor reads this data, and the outputs are disabled. During the second phase, data is read from the FIFO buffer to the A latch. The entire cycle begins on the falling edge of $\overline{\text{STRB}}$. $\overline{\text{OCA}}$, which is a decode of the processor's $\overline{\text{STRB}}$, R/W, and address signals, will activate at this time and enable the latch's outputs. The latch remains enabled until $\overline{\text{STRB}}$ goes high. On this edge, the processor reads the latch's data before $\overline{\text{OC}}$ is deasserted and the latch is disabled.

Once the processor has read the data, the microsequencer must refill the latch. The microsequencer initiates the read from the FIFO buffer into the latch when it detects PE2RD. This occurs on the rising edge of SAMCLK 50 ns after $\overline{\text{STRB}}$ goes low. The microsequencer waits one clock until it drives $\overline{\text{RFIFO}}$ low. $\overline{\text{RFIFO}}$ then requests the FIFO buffer to output a word.

The input enable to the A latch (G) is also activated by the microsequencer at this time. $\overline{\text{RFIFO}}$ and G are actually asserted on the microsequencer's pins 16.5 ns after SAMCLK (clock-to-output delay). If the FIFO buffer has an access time of 25 ns, the output data of the FIFO buffer appears at A latch's inputs 41.5 ns (16.5 ns + 25 ns) after PE2RD is detected. The $\overline{\text{RFIFO}}$ pulse remains low for 50 ns. Data is valid at the A latch for 25 ns ($\overline{\text{RFIFO}}$ low for 50 ns and a 25-ns FIFO access time), easily meeting the setup time of the latch. On the rising edge of $\overline{\text{RFIFO}}$, the data is latched in.

This process requires two SAMCLKs—one to detect PE2RD and one to assert $\overline{\text{RFIFO}}$ to the FIFO buffer—half the 200-ns processor cycle time. If the FIFO buffer is empty (EF1 high) at the time of the read request, the microsequencer will deactivate the RDY signal to the processor and inform the system processor of the error status. The microsequencer might have a special set of routines so the PE can recover from the error dynamically.

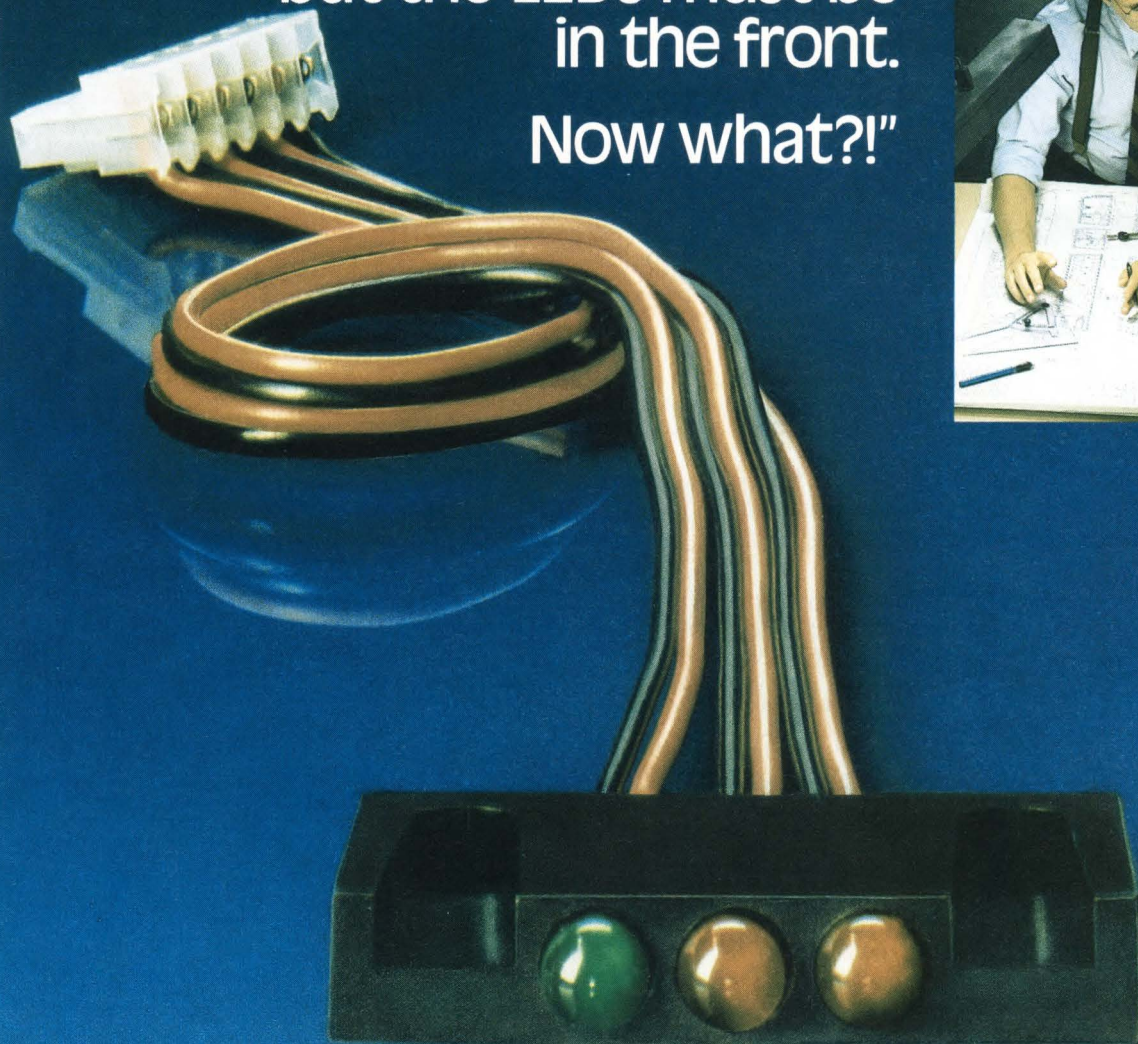
PE2WR goes active when the pro-



4. THE FIRST STEP IN HANDLING the module's data flow is managing the FIFO buffers' read and write cycles. The diagram shows how the processing element, microsequencer, and latch work together to efficiently move data.

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MICROSEQUENCER-BASED DATA CONTROL

cessor issues a write cycle. After PE2WR goes high, the B latch's inputs are enabled because G is tied to PE2WR. The latch is then ready to accept a new data word.

To write data into the output FIFO buffer, \overline{OCB} and \overline{WFIFO} appear 16.5 ns (clock-output delay) after the clock cycle following the detection of PE2WR. This gives the second stage control of the FIFO buffer's data bus and begins the FIFO read.

The \overline{OC} and \overline{WFIFO} pulse deassert (go high) 50 ns later, and the B latch's data is written into the FIFO buffer.

The write process also requires two SAMCLKs, one to detect PE2WR and one to assert to the FIFO buffer. If the buffer is full (indicated by FF2 high) at the time of the write request, the microsequencer deactivates RDY to the processor and informs the system processor of the error status.

The microsequencer-subsystem control tasks include checking the processors for read and write requests, servicing these requests, and checking for FIFO-buffer error condition. The state machine language is the code used to enter EPS448 microsequencer designs that perform these tasks (Fig. 5). This language consists of simple "if-then" constructs. Output specifications for any particular state are designated in brackets and appear in the same order in which they are placed in the outputs section. For example, the first output in brackets represents \overline{RFIFO} . Macros are used to substitute text for commonly used output strings. For instance, idle substitutes for $G=0$ (inactive), $RDY=1$ (active), and $\overline{OC}=1$ (inactive). Control flow starts at the label PE1SRVC.

PE1SRVC is the starting point for data-flow control in this example, but it's identical to the PE2SRVC subroutine that's shown in detail. PE2SRVC is reached when the first

OUTPUTS:	\overline{RFIFO} , \overline{WFIFO} , G1, RDY1, $\overline{OC1}$, G2, RDY2, $\overline{OC2}$,, ERR
MACROS:	IDLE = "011"
PE1SRVC:	%SIMILAR TO PE2SRVC%
PE2SRVC:	IF EF1 + FF2 THEN [11 001 001 . . . 1] GOTO SYSERR %PROC. NOT READY% ELSEIF PE2RD THEN [11 IDLE IDLE . . . 0] GOTO RDPE2; %READY TO READ% ELSEIF PE2WR THEN [11 IDLE IDLE . . . 0] GOTO WRPE2; %READY TO WRITE% ELSE [11 001 001 . . . 0] GOTO SYNCH; %ERR, NEED TO SYNC% [01 IDLE 111 . . . 0] GOTO PE3SRVC; %READ FROM INP FIFO% [10 IDLE 010 . . . 0] GOTO PE3SRVC; %WRITE TO OUT FIFO%
RDPE2:	
WRPE2:	
PE3SRVC:	%SIMILAR TO PE2SRVC%
PE4SRVC:	%SIMILAR TO PE2SRVC%
SYNCH:	RECOVERY, WAIT FOR ERROR CONDITIONS TO CLEAR STOP PROCESSORS, SYNCH SUBSYSTEM

5. CODE CONTROLS how the microsequencer checks the processors for read and write requests, services those requests, and checks the FIFO buffers for error conditions.

processor is serviced. One of four different states becomes active when PE2SRVC is called (after processor one has been serviced). The first state at PE2SRVC becomes active if the input FIFO buffer is empty or the output FIFO buffer is full (EF1 and FF2). When either error condition takes place, the processors' RDY signals are forced low and a transition to SYSERR occurs. This system error shouldn't happen because the FIFO-buffer depths are chosen according to worst case data build-up. But if either error condition does take place, users can customize the SYSERR subroutine to a particular system. SYSERR should inform the main CPU of the subsystem error and have the microsequencer clear the error status.

If PE2RD is true, the second state takes place. All outputs are static to prepare to perform the required read cycle, assuming no errors occurred at the label PE2SRVC. The label RDPE2 becomes active on the next SAMCLK, when \overline{RFIFO} and G2 become active. This state causes a read from the FIFO buffer to the A latch. On the next SAMCLK, a transition to PE3SRVC occurs. The third processor is then serviced and all outputs relating to the second processor stage are deactivated.

The third state at the PE2SRVC label develops when PE2WR is true, which prompts a write cycle to begin. All outputs remain static until

SAMCLK causes a transition to the only state at the WRPE2 label. With this state's outputs, which force \overline{WFIFO} and \overline{OC} low, the processor can write data to the output FIFO. On the following SAMCLK, there is a transition to PE3SRVC. At PE3SRVC, the third processor is serviced and all outputs relating to the second processor stage are deactivated.

In the fourth state, neither error condition is true and both PE2RD and PE2WR are inactive. This error condition informs users that the processors aren't synchronized. The subsystem was designed so that the second processor stage lags the first stage by 100 ns, which is the same time it takes to read or write from the first processor.

Furthermore in this simplified example, it's assumed that all of the processors in this system are executing instructions requiring the same amount of time. If the first processor has just read data, the second processor should also be ready to read data as PE2SRVC is reached. If it's not ready, a synchronization error ensues and all of the processor's RDY signals are pulled low. A transition to SYNCH takes place, which resynchronizes the subsystem processors through a user-created subroutine. □

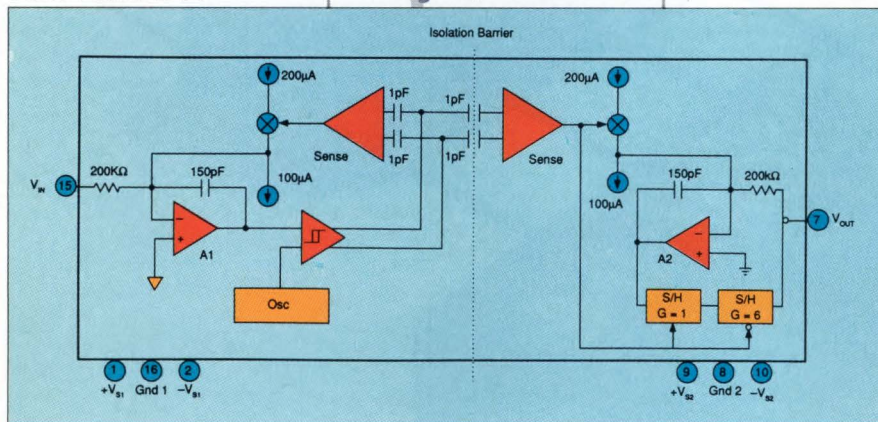
David Creamer, an applications group leader at Altera, has a BSEE/CS from the University of California at Berkeley.

Michael K. Webb, director of product planning and applications at Altera, has a BSEE from the University of Texas.

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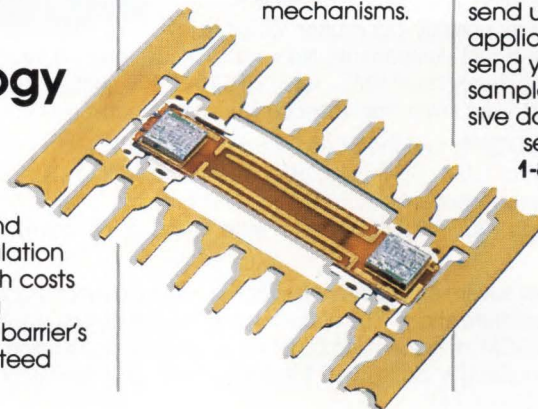


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CIRCLE 521 DIVIDE-BY-N COUNTER RUNS ABOVE 1 GHz

JOHN HATCHETT

Motorola Inc., 3102 North 56th St., Phoenix, Ariz. 85018; (602) 952-3416.

Counter speeds for CMOS and TTL programmable counters are limited to under 100 MHz. ECL-type devices can approach a few hundred MHz, but with significant current requirements. However, coupling the dual-modulus-prescaling technique with the available phase-locked loop synthesizer chips that control the prescaler circumvents these frequency and power-drain constraints.

With this approach, designers can also choose various counter-programming schemes (serial, parallel, or data bus) in addition to achieving higher frequency capabilities. Low-power drain (less than 75 mW) and low-cost devices can also be selected.

Moreover, only two ICs are necessary to achieve divide values above 131,000.

Maximum input frequency and dividing range for the counter are controlled by choosing an appropriate 8-pin dual-modulus prescaler. The counter's output appears at synthesizer pin F_V (see the figure). The total input-to-output divide value is governed by the equation:

$$N_{\text{total}} = N \times P + A.$$

N and A represent the value programmed through the serial port into the divide-by- N and divide-by- A counters. P is the lower dual-modulus value established by the synthesizer's modulus-control signal.

IFD WINNERS

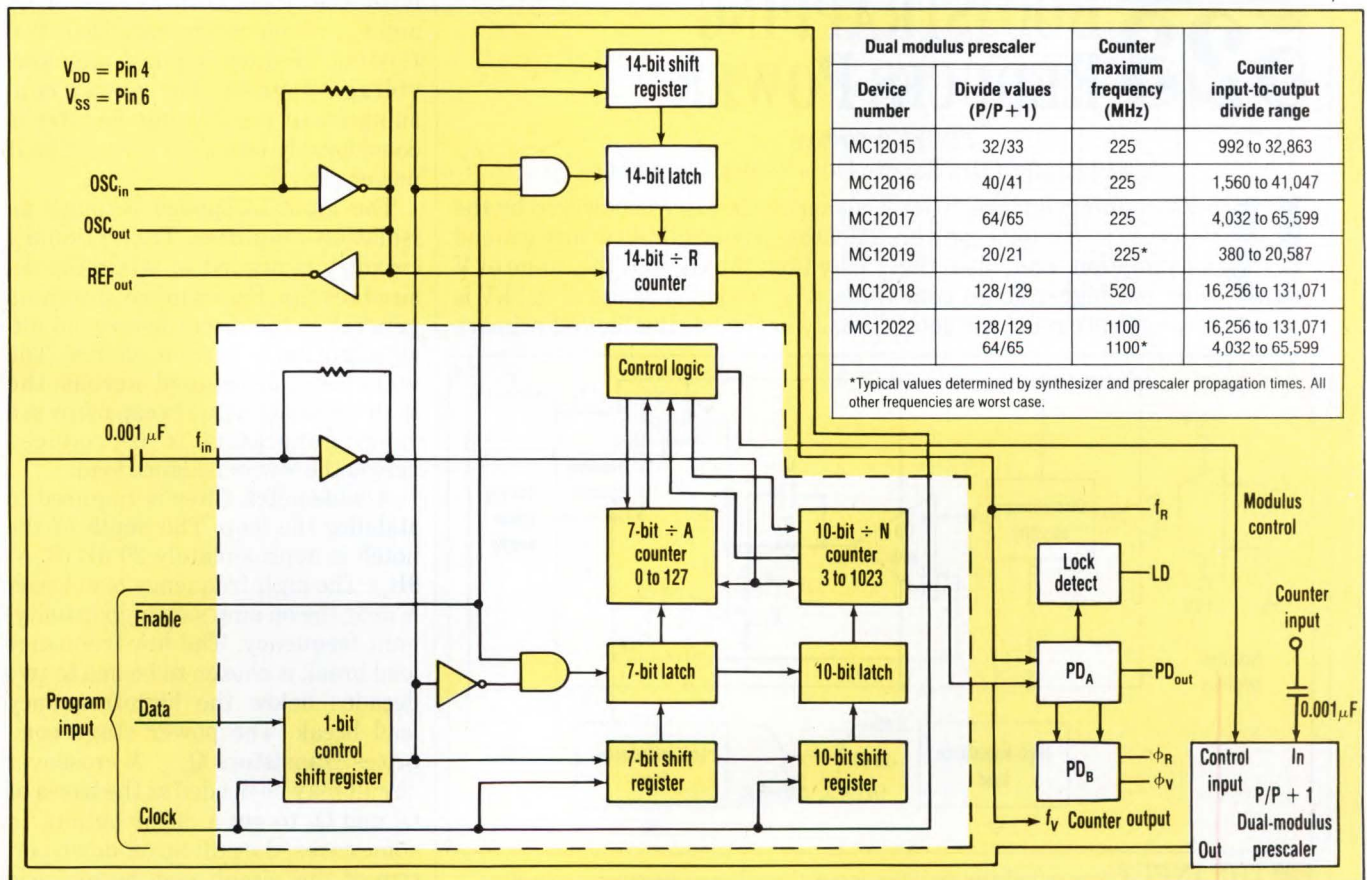
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Israel Yuval, ADA (Israel), P.O. Box 2250, Haifa, Israel. His idea: "Sync Detector's Failures Cut."

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Typically, A varies from zero to $P-1$ to achieve unit steps within the system's divide range. And N must be equal to or greater than A . $N \gg A$ then sets a lower limit on N_{total} , which is dictated by $A_{\text{MAX}} = P-1$. □



THIS TWO-CHIP COUNTER SCHEME can operate at more than 1 GHz and consume less than 15 mA from a 5-V supply.

CIRCLE 522 GET A PRECISION -10-V REFERENCE

R. MARK STITT

Burr-Brown Corp., P.O. Box 11400, Tuscon, AZ 85734; (602) 746-7445.

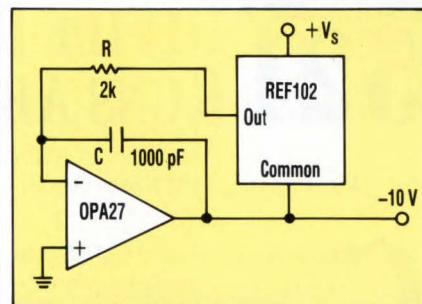
Most popular CMOS multiplying digital-to-analog converters (MDACs) require an external op amp and a reference for a -10-V voltage output. But by using the correct circuitry, any +10-V reference can be accurately converted to a -10-V reference (see the figure). Precision resistors aren't required, and the error contributed by the op amp is negligible (the $0.6\mu\text{V}/^\circ\text{C}$ V_{OS} drift of an OPA27 adds only 0.06 ppm/ $^\circ\text{C}$ voltage-reference drift).

This same circuit also incorporates reference noise filtering. When a monolithic buried zener reference is

used, such as a Burr-Brown FEF102, drift with temperature is just 2.5ppm/ $^\circ\text{C}$ maximum, and noise and stability are significantly better than for bandgap references.

The reference signal is in the op amp's feedback loop. The amp output forces the reference-common connection to -10-V so that the inverting-input voltage is the same as its noninverting input (ground). Because current doesn't flow into the op-amp input, the reference output current stays at zero.

The $2\text{-k}\Omega \times 1000\text{-pF}$ network ensures loop stability and adds noise filtering. With these values, the ref-



A -10-V PRECISION reference can be designed with a +10-V reference and an external op amp. Precision resistors aren't needed.

erence noise is filtered by one pole where $f_{-3\text{dB}} = 1/(2\pi RC)$. For a lower pole, R should stay at 2 k Ω and C should be increased. Keeping R small reduces bias-current errors and noise from the op amp that's reacting with it. For reference output adjustment, put a potentiometer between the reference output and reference-common pin (-10-V output). □

CIRCLE 523 BOOTSTRAPPING REDUCES POWER

PATRICK H. CONWAY

28361 Plainfield Dr., Rancho Palos Verdes, CA 90274.

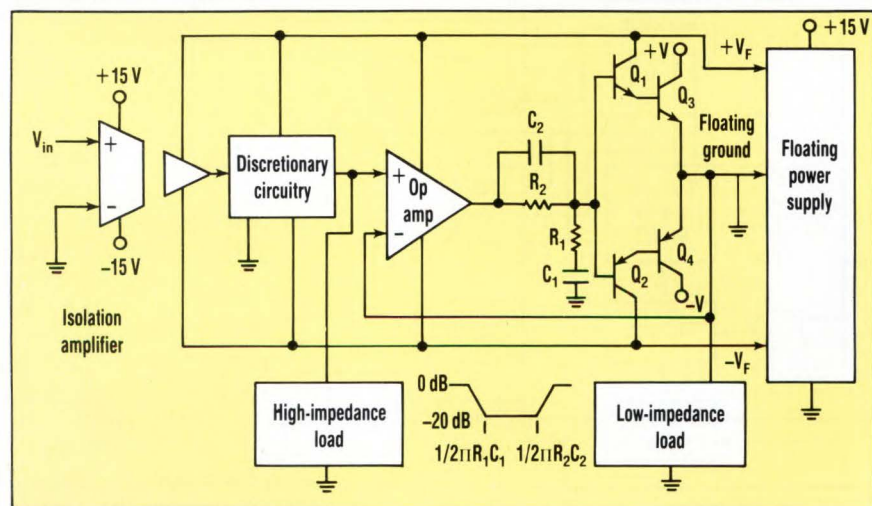
Bootstrapping an amplifier reduces a circuit's power consumption and also the need for high-voltage components. In a typical circuit, the boot-

strapped circuitry is powered by the floating power supply whose ground may float throughout the range of V (see the figure). A range of $\pm 1\text{ kV}$ is easily achieved. It's limited primari-

ly by the breakdown ratings of Q_3 and Q_4 , which can be cascoded. The floating circuitry requires only low-voltage devices. The power consumption of the floating circuitry is considerably less than it would be if powered by V.

The input is applied through an isolation amplifier. Discretionary circuitry is needed to attain the desired results. For example, in a ramp generator, the discretionary circuitry might be a current source. The waveform developed across the high-impedance load (a capacitor in a ramp generator) is reproduced across the low-impedance load.

A wide-notch filter is required to stabilize the loop. The depth of the notch is approximately 20 dB ($R_2 = 9R_1$). The high-frequency lead break is near the op amp's open-loop unity-gain frequency. The low-frequency lead break is chosen to be one to two decades below the high-frequency lead break. The power stage comprises transistors Q_{1-4} . A crossover circuit may be needed at the bases of Q_1 and Q_2 to get a linear output. In some cases, the pull-up or -down portion of this circuit may be replaced with a current source. □



THE INPUT from an isolation amplifier, is sent through some discretionary circuitry, an op amp, and an RC network before it goes through the transistors.

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WESCON CENTERS ON COMPONENT AND SYSTEM TECHNOLOGIES

M

aturing and emerging ASIC technologies are giving today's CAE and CAD tools a run for their money. Concurrently, ECL is settling in as a mainstream technology for the 1990s. These and many other

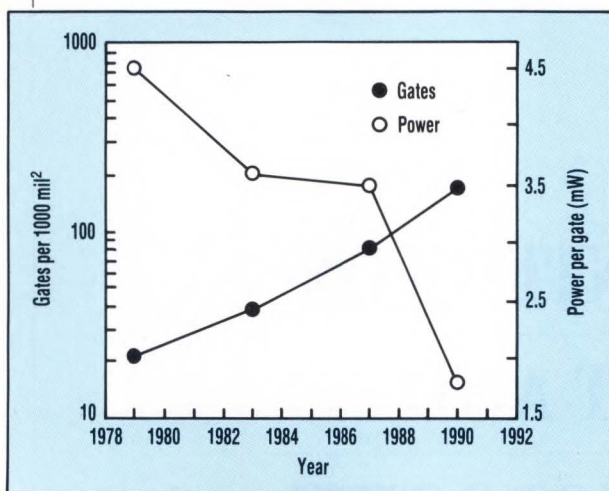
technical trends will be examined during the professional-advancement program sessions at Wescon/89. Component and system technologies and manufacturing issues are the three broad areas that the sessions will concentrate on. The sessions, which run from November 14 to 16 in San Francisco, will cover topics ranging from memory issues, video technology, and specialized processors to neural networks and software tools.

In the component-technology sessions, recent advances in ECL that have keyed faster, lower-power systems will be explored. As ECL becomes a mainstream technology, it leaves its niche applications behind for acceptance by system designers as a means to boost performance. In a paper by Joseph Vithayathil, marketing manager at Synergy Semiconductor Corp., Santa Clara, Calif., three recent trends are considered stepping stones for ECL to emerge as a bread-and-butter technology.

The first trend is increased system-clock speeds. As clock frequencies surpass 50 MHz, the limitations of the TTL-interface standard present a technical obstacle for system designers. Thanks to its superiority in such a transmission-line environment, ECL is becoming the technology of choice. A second trend pushing ECL to the forefront is the wave of ECL implementations of popular microprocessors, including RISC processors. These first implementations are expected to run in the 70-to-100-MHz range. Finally, innovative techniques are being applied to ECL circuits and bipolar technology. These techniques eliminate the traditional disadvantages of such technologies to bring them to the

DAVID MALINIAK

PREVIEW



1. POWER DISSIPATION continues to drop as gate counts rise in ECL ASICs. Smaller device geometries and three-level series gating are keys.

forefront in terms of performance, power, integration, and manufacturability.

ASIC technologies are also maturing. As new architectures and tech-

turn, means denser logic (*Fig. 1*). As for CMOS ASICs, increasing gate densities calls for more I/O. The mounting power dissipation eclipses the 2-to-3-W threshold that had dis-

nologies appear, they must support higher levels of system integration. This carries implications for designers in terms of chip specifications as well as design tools. According to Virgil P. LaBuda and Clarence S. Nataka of Motorola's ASIC Division, Chandler, Ariz., established ECL and CMOS technologies are evolving to support higher integration. Smaller device geometries in ECL ASICs are curbing their high power consumption. Three-level series gating, in

tinguished CMOS packaging needs from those of bipolar.

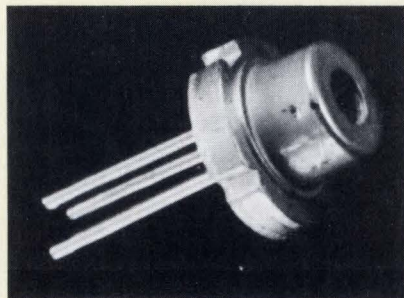
Gallium-arsenide ASICs continue to challenge ECL for performance leadership at a fraction of ECL's power consumption. Cost-effective, reliable fabrication techniques must be developed for GaAs, however, before its challenge can be taken seriously, LaBuda and Nataka contend. BiCMOS technologies overcome the performance limitations of CMOS not only through enhanced internal logic drive, but also by greatly expanding the variety of I/O characteristics.

These expanding technology choices for ASICs are testing the limits of the CAD tools used in their design. LaBuda and Nataka confirm that CAD tools must continually evolve to give users automation and flexibility within the design process. A common problem—incompatibility between tools—is being addressed by framework-based CAD



Wescon®/89 PRODUCTS

Molecular-beam-epitaxy laser diode is mass-produced. The RLD 78 Series molecular-beam-epitaxy (MBE) laser diode is the first to be mass-produced. The fabrication process results in a laser that is more planar and uniform than those produced by liquid-phase epitaxial techniques. The diodes feature a 770-to 800-nm wavelength



range and operate from 1.9 V with a threshold current of 45 mA. Signal-to-noise ratio varies from 60 to 85 dB with device type. In quantities of 1000, prices range from \$20 to \$30. Delivery is in eight to 10 weeks.

Rohm Corp.
Irvine, Calif.; (714) 855-2131.
Booth 351

Circle 482

Lithium batteries can now be surface-mounted. The TL-5186/SM lithium thionyl chloride battery is believed to be the first lithium cell able to withstand the stresses of surface mounting and wave soldering without degradation. The hermetically sealed battery can be fed into an automatic placement system for higher throughput. It can handle infrared or vapor-phase sol-

dering. Rated at 3.6 V, the battery measures 7/8-in. square and 9/32-in. thick. Maximum capacity at 100 μ A to 3 V is 0.37 Ah. In quantities up to 1000, the batteries go for about \$4. Delivery is from 6 to 8 weeks.

Tadiran Electronic Industries
Port Washington, N.Y.; (516) 621-4980.
Booth 2303

Circle 483



Unleash the infinite memory power of Hitachi's digital oscilloscopes

Slide a pocket-size IC card with a three-year memory into the front-panel slot and store up to 15 waveforms (4K each). Retrieve historical data on prototype designs, reconfigure test workstations quickly and at low cost, and create comparison waveforms to speed equipment maintenance.

Memory is unlimited. Use as many cards as you wish to store as much information as you wish, to distribute to as many associates as you desire. Using an optional card reader/writer, waveforms on the PC card can be transferred to/from an IBM PC or compatible; with an

optional high-speed interface, signals can be transferred to the PC for data analysis.

An external clock permits sampling in units other than time base (angle, rotation speed, displacement, etc.). Or sampling synchronization with the operational clock of the device being measured. Other usual functions include: four sampling modes, three interpolation modes, and GPIB, as well as plotter outputs. Also, any model can be used as a 100MHz bandwidth two-channel real-time oscilloscope.

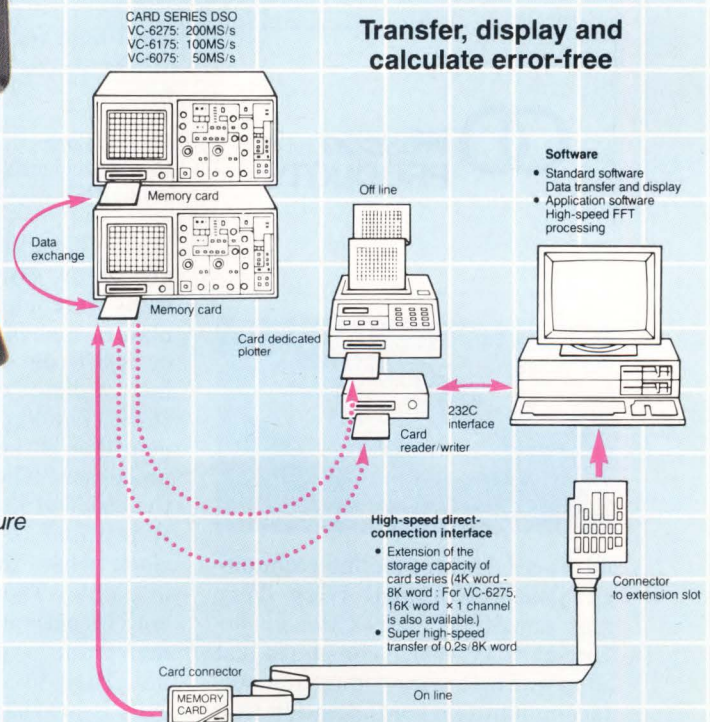
This new, cost-effective way to communicate data quickly and error-free is only possible with Hitachi's Card Series DSOs available in three sampling speeds: the VC-6275 at 200MS/s, the VC-6175 at 100MS/s, and the VC-6075 at 50MS/s. Units are available on GSA contract GS00F03461.

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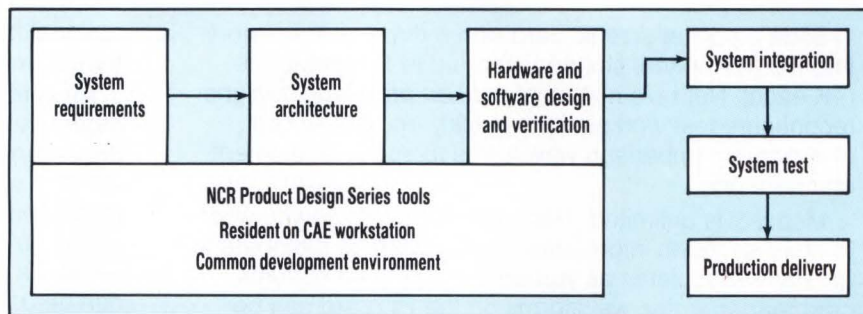
CIRCLE 31

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systems that integrate third-party and internally developed tools into one system.

Accuracy advancements in CAE and CAD tools have resulted in impressive ASIC first-pass success rates when the criterion was the ASIC's specifications. For successful products, however, the ASIC must work properly in the system. This is the central assertion made by Earl O. Reinkensmeyer, director of software products at NCR Corp., Ft. Collins, Colo., in his paper, "CAE Applied to ASIC and System Design." Reinkensmeyer describes how NCR's Product Design Series (PDS) of CAE/CAD tools help assure that the product-definition phase of the design cycle will be successful.

The tools included in the PDS encompass architectural simulation and design synthesis. These functions use behavioral-level descriptions with selected structural considerations. The resulting "what-if"



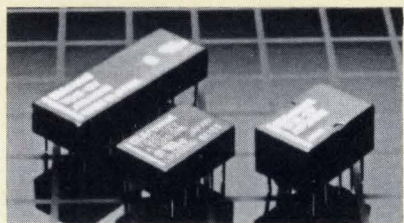
2. BY MIXING behavioral and structural analysis, NCR's Product Design Series of design tools can shorten the product-definition phase of the design cycle. ASICs can be designed to work better in the system.

analysis helps product-marketing staffs develop product requirements. This blend of behavioral and fast structural analysis yields a better product definition (*Fig. 2*).

The design cycle of digital systems can be problematic when various incompatible CAD, CAE, and CAT tools each require a special language and specific interface. Sharing of data among different organizations

or across levels of design becomes very difficult. In his paper, "VHSIC Hardware Description Language (VHDL) for CAD/CAE/CAT," H. Edward Tsou, senior staff engineer at TRW Electronic Systems Group, Redondo Beach, Calif., brings Wescon attendees up to date on the progress of VHDL-related technologies. Tsou describes how VHDL has indeed fulfilled its specified


Wescon[®]/89
PRODUCTS



Advanced surface-mount technology yields ultra-small relay. Very high sensitivity marks the TF polarized relay, which consumes just 80 mW. The device comes in a surface-mountable configuration that withstands either infrared or vapor-phase reflow soldering processes. Contacts are 2 Form C with available coil voltages of 3, 4.5, 5, 6, 9, 12, 24, and 48 V. A gold-clad, crossbar bifurcated contact en-

suces high reliability. In quantities of 500, prices range from \$3.31 to \$4.38.

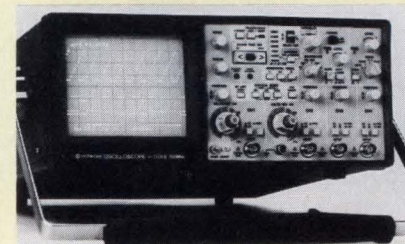
Aromat Corp.
New Providence, N.J.; (201) 464-3550.
Booth 2337 **Circle 493**

In-circuit emulator is first for 80486 processor. Microcosm customers using the company's hyperICE emulators for 80286, 80386, 80386SX, or 80376 development work now have a direct upgrade path to the 80486. The hyperICE-486 in-circuit emulator is the first for that Intel processor. The system emulates the 80486 at its full 25-MHz speed. It is rated to support a 33-MHz clock when that silicon becomes available. The emulator can run with its native interface from a PC, mainframe, workstation, or terminal. High-level-language debugging is provided by the company's hyperSOURCE software. The system starts at \$24,990. Delivery is in 45 days.

Microcosm Inc.
Beaverton, Ore.; (503) 626-6100.
Booth 1144 **Circle 485**

100-MHz, four-channel scope weighs in at just 15.4 lbs. Lightweight and compact, the V-1085 four-channel oscilloscope is packed with popular features. Among them are autoranging sweep, trigger lock for complex patterns, and cursor measurements. All four channels have independent position control, 100-MHz bandwidths, and $\pm 3\%$ accuracy. A built-in counter operates from the triggering signal of any channel or external source. There is also a triggerable delayed sweep for sophisticated analysis of transient signals. The scope is available immediately and goes for \$2295.

Hitachi Denshi America Ltd.
Woodbury, N.Y.; (800) 645-7288.
Booth 1044 **Circle 486**



Hirose

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For maximum design flexibility all HFDDI connectors are offered with a choice of four different standard keying positions.

Also new from Hirose are the HSC single or multi-mode fiber optic connectors. Conforming to NTT SC standards, these connectors incorporate Zirconia ferrules and offer insertion loss of less than 0.5dB with a minimum reflection loss of 22dB on assemblies using SM-10/125 cable.



Hirose HSC Connector

Fiber optic connectors with *built-in* security protection; everything you'd expect from the world's finest connector company. For additional information, specifications and samples, call the experts at Hirose Electric (USA) Inc.



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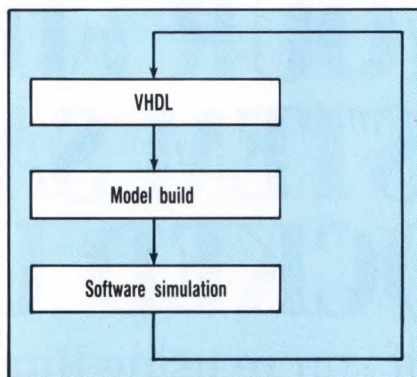
*PLUG
HOUSING*

PREVIEW

requirements.

A paper by Richard M. Braid, development engineer manager, and Mark A. Johnson, staff engineer, both at IBM Application Business Systems, Rochester, Minn., demonstrates how the VHDL design methodology can speed products to market. An IBM hardware-design team used VHDL to quickly define, implement, verify, and physically design a tape controller in less than nine months. The 20K CMOS design, which was to be a 370-tape attachment for the 9406 models of the IBM Application System/400, was segmented into four phases. In the first phase, the design was defined, the design strategy laid out, and the design team was staffed. VHDL chose the design tool at this point because it would enable the design to be used as a basis for future efforts.

The second phase involved dividing the controller chip's functions and assigning them to individual designers. These team members each



3. IN AN ITERATIVE process for verifying VHDL designs, a VHDL description is translated into a model, which in turn is simulated in software. Design problems are rectified at the VHDL level; then the process restarts until all bugs are out.

learned VHDL in three classes over a one-month period. As the hardware design progressed, the project entered its third phase, which was to verify the design. Simulation was performed with a software simula-

tion tool. An iterative process fixed problems with the design at the VHDL level. A model of the hardware was then created and test cases were run using the simulation tool. As design problems were found during simulation, the process started over with fixes applied at the VHDL level (*Fig. 3*).

In the final physical-design phase, preliminary runs allowed changes to be made with regard to testability and timing before the design was frozen. At this point, the decision was made to change the technology design point. The cell count was rapidly approaching the 10k capacity of the CMOS family that was chosen, which necessitated a switch to a technology with a higher circuit capacity. Fortunately, VHDL is technology-independent, so the change had no impact to the design schedule. According to the authors, this represents one of the strengths of VHDL.

As the design and its verification neared completion, the design was



Sub-compact sealed lead-acid batteries pack high energy. Substantial reductions in size and weight without performance loss are features of the My-Act lead-acid batteries. The thin, rectangular batteries are made up of individual 2-V cells that can form custom battery packs with a wide range of capacities,



voltages, and terminations. A typical 0.65-Ah My-Act cell (model UP2V0-6P) delivers 65 mA for 10 hours to a cutoff of 1.8 V. Standard-cell deliveries are from stock to 12 weeks. Prices vary with battery configuration.

Panasonic Industrial Co.

Secaucus, N.J.; (201) 348-5266.

Booth 456

Circle 487

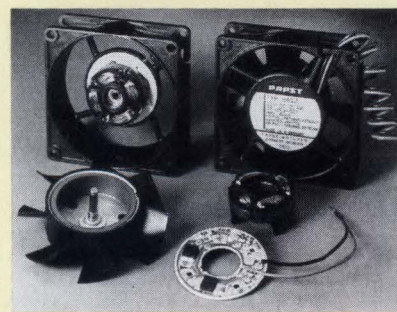
Pc-board-layout package is upgraded in new version. Increased capacity and via and track optimization are among many new features in the completely updated PCB II layout package. The product now supports more than 270 14-pin-IC equivalent designs, over 6000 pads, and over 16,000 equivalent track segments. Powerful analysis and rip-up rerouting capability optimizes and improves track placement and minimizes vias in a design. Over 50 printers are supported. The package costs \$1495.

OrCAD Systems Corp.

Hillsboro, Ore.; (503) 640-9488.

Booth 1454

Circle 488



1-in.-thick dc fan cools enclosures in minimal space. Very quiet operation and high performance for package size are features of the 1-in.-thick dc Multifans. The fan is available in three sizes with three different speeds. As part of the 600, 8400, and 3400 series, they all will be offered in 12- or 24-V dc versions. The 8400 and 3400 series will also be offered with sleeve bearings. Made of fiberglass-reinforced plastic, the fans mean significant cost savings to OEMs.

Pabst Mechatronic Corp.

Newport, R.I.; (401) 849-8810.

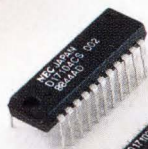
Booth 2255

Circle 489

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I/O ports	11		16	
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Standby mode	STOP/HALT			
Oscillation	Ceramic	RC	Ceramic	RC
Package	16-pin shrink DIP/16-pin SOP		22-pin shrink DIP/24-pin SOP	
Onetime PROM	4Q '89	1Q '90	4Q '89	1Q '90

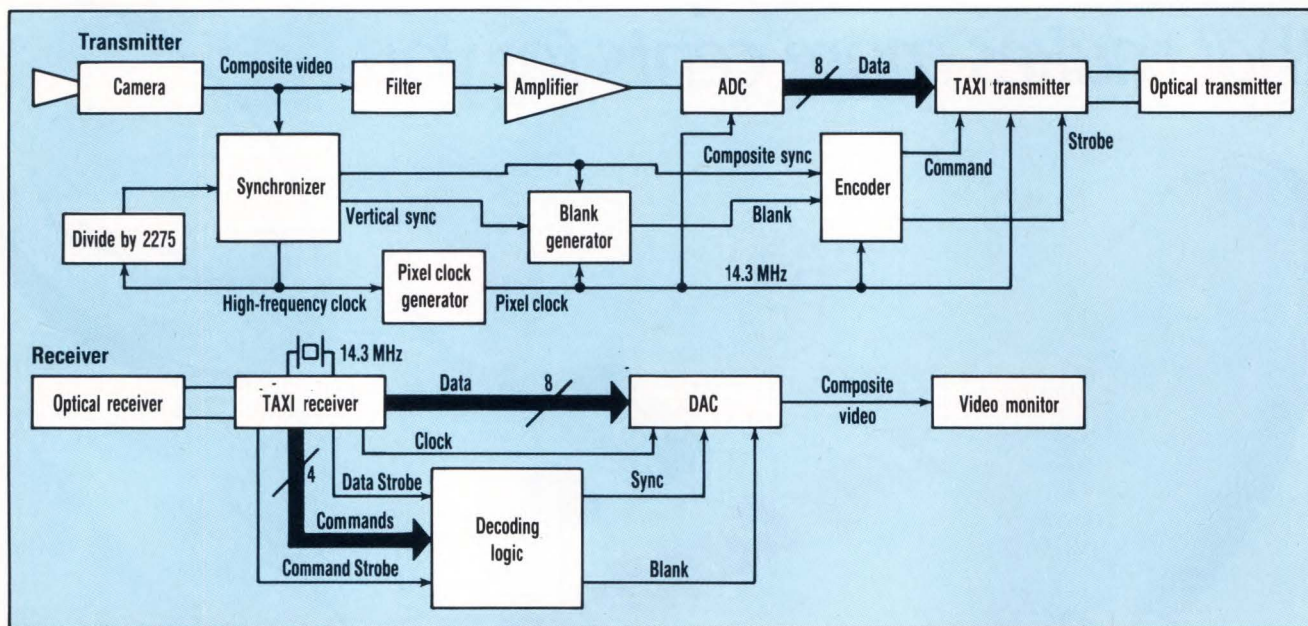
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PREVIEW



4. REAL-TIME NTSC COLOR VIDEO can be transmitted over a fiber-optic link at distances of up to 2 km with Advanced Micro Devices' TAXIchip set. By combining fiber optics with standard encoding and decoding ICs, the link eases serial transmission of high-bandwidth signals. The fiber-optic components eliminate media constraints.

frozen and the VHDL was synthesized to a technology-dependent representation. The chip was then placed and wired. But a static timing-analysis tool didn't work as well as expected, making it difficult to sort out valid timing problems from inva-

lid problems. Several valid problems were nearly overlooked. This pointed out the need for better static timing-analysis tools for use with VHDL-based designs.

On the systems-communication front, fast fiber-optic links are being

used in applications ranging from local-area networks and computer-to-peripheral links to process control, robotics, and automotive communications. A paper by Eugen Gershon, Neil Mammen, and Steven Sidman of Advanced Micro Devices, Sunny-



1000-W switcher reaches new heights in power density. Packaging and design techniques applied in the 9A, 9B, and 9C SuperSwitcher II series of single-output switchers have yielded a 5-by-5-by-10-in. size for a 5-V, 200-A supply. This permits three such units to be placed side-by-side in a 19-in. rack. Featured is a control card only 7.5 in. square, compared with 20 in. square for an earlier version. The control card uses custom hybrid circuits and surface-mounted compo-

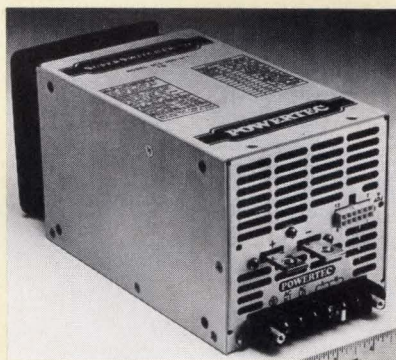
nents. Features include overvoltage protection, remote sense, automatic thermal shutdown, and more. An integral dc fan cools the supply. In single quantities, a 5-V, 200-A supply goes for \$745. Samples are available now with delivery in eight to 10 weeks.

Powertec

Chatsworth, Calif.; (818) 882-0004.

Booth 2359

Circle 490



Schematic-capture tool presents seamless user interface. Full compatibility with Accel's pc-board layout and autorouter tools is featured in its Tango-Schematic Series II schematic-capture tool. All the tool's capabilities are contained within one menu-driven program. As a result, designers can draw schematics on the screen, create new library components, perform design-rule checks, generate net lists, and produce hard-copy out-



Wescon®/89

PREVIEW

vale, Calif., describes how AMD's TAXIchip set transmitted real-time NTSC color video over 2 km of optical fiber (*Fig. 4*). The authors address the problems of transmitting both video-signal-amplitude information and video-timing information for link synchronization.

Serial transmission of higher-bandwidth signals, such as NTSC video, isn't common yet. This stems from a combination of media constraints and a lack of standard ICs to serialize, encode, recover, and deserialize the data. According to the authors, media constraints can be eliminated by choosing fiber-optic components, and the standard-IC void can be filled with AMD's chip set.

The dispersion effects of optical fiber are minimal compared to metallic media, which lends the fiber to very high data rates. Similarly, optical fiber's attenuation is much less than that of metallic media, meaning that long links can be established without repeaters. As a result, for many applications, the maximum usable distance and data rate for a fiber-optic link is established primarily by the characteristics of the drivers and receivers, not the medium itself.

Gershon, Mammen, and Sidman describe how the video signal, with its relatively large 3-to-5-MHz bandwidth, is digitized at twice the maximum frequency expected in the signal. In this case, 14.31818 MHz is the digitizing rate, which is four times the frequency of the color burst. Therefore, the TAXIchip set is run at a 143-MHz serial baud rate. For transmission along the link, the video signal is processed in three different sections: video sync, video blank, and data.

The video digital-to-analog converter's output is a composite video signal that can drive a monitor. The digitized and transmitted picture doesn't have any visible loss of quality compared to the original taken directly from the camera to the monitor. The total dynamic range of the digitized video signal is about 10% larger than the video gray scale, which enables the color burst to be included accurately. □

HOW VALUABLE?

	CIRCLE
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MODERATELY	560
SLIGHTLY	561

put. The tool, which runs on IBM PC, PC/XT, PC/AT, and PS/2 computers, includes comprehensive component libraries with over 5000 parts spanning various technologies. Each component is guaranteed for its accuracy. The schematic-capture tool goes for \$495.

Accel Technologies Inc.

San Diego, Calif.; (619) 554-1000.

Booth 1343

Circle 491

Pc-board autorouter joins design-tool family. Features found only in mainframe or supermini-class routers are packed into the Z-Route autorouter, an addition to the AutoPCB family. The tool routes directly to off-grid components and offers true 45° routing. A warp-grid feature permits traces to warp around a pin without losing real estate. Design-rule checking and a user-definable routing strategy

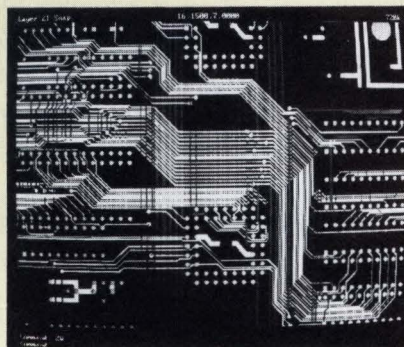
round out the package. The router is 100% compatible with AutoCAD. A display-list processor permits split-second zooms and pans. The complete AutoPCB product, which includes the router as well as schematic capture and complete parts libraries, goes for \$4295.

Cadisys Corp.

Sunnyvale, Calif.; (408) 732-1832.

Booth 1342

Circle 492



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CIRCLE 101

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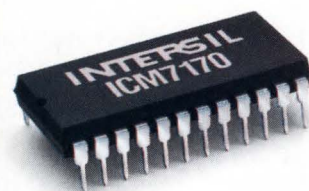
cess time and high compatibility make it a perfect peripheral for a whole range of applications, from data logging and portable and personal computers to industrial process control and point of sale systems.

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forming where performance counts most — in demanding strategic and tactical systems. Packages include 24-pin plastic and ceramic DIPs and 24-pin SOIC.

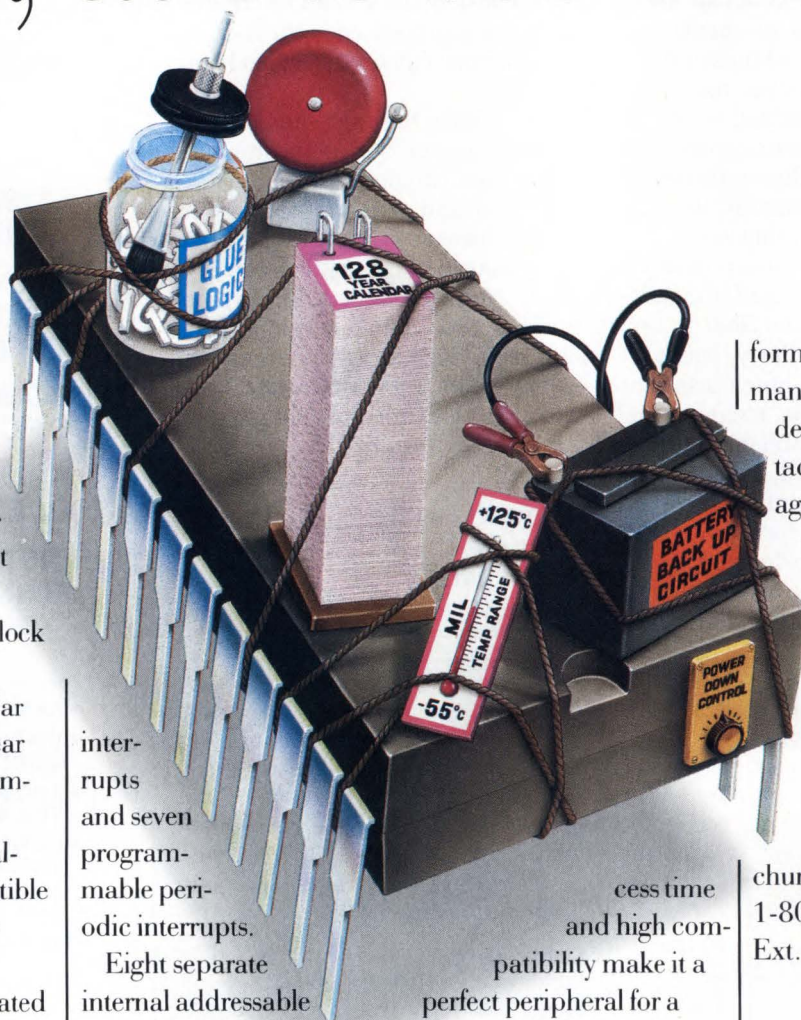
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PC SOFTWARE AUTOMATES BANDPASS-FILTER DESIGN

With a bandpass-filter design package from Phil Geffe's Filterware, Cincinnati, users need only enter filter specifications and the program will do the rest. Called Band, the software runs on IBM PCs and compatibles and gives practical designs for the frequency range of 10 Hz to 2 GHz. Inductor-capacitor (LC) filters can be designed with up to 20 coils. The program also handles Butterworth, Chebyshev, Bessel, and constant-K bandpass filters that have all coils equal to a specified inductance value. The lossy bandwidth is automatically adjusted to an accuracy of better than 0.1% using components with specified Q values, and band-edge attenuation error is typically less than 0.02 dB. Narrow-band and Norton transformations are performed automatically. The Band software costs \$99. Call Phil Geffe, (513) 948-1599. LG

CIRCLE 301

DESIGN AND ANALYZE FILTERS ON A MACINTOSH

MacFilter software from Momentum Data Systems Inc., Costa Mesa, Calif., combines a simple user interface with complex digital-filter design. The system also features extensive error checking and detailed help screens. MacFilter supports the design of three different filters: finite-impulse response, infinite-impulse response, and Parks McClellan. In addition, it performs system analysis by determining magnitude, phase, group delay, impulse response, pole and zero locations, and step response of a given transfer function. Once designers have completed their filter specification, they can invoke a separate code generator that automatically outputs assembly code for the Motorola 56001 digital-signal processor. Results are output graphically with zoom capability for both axes. MacFilter runs on the Macintosh SE and Macintosh II. A math coprocessor is strongly recommended. The system is available now for \$995. The Motorola 56001 code generator is sold separately for \$200. Call Jerry Purcell, (714) 557-6884. LG

CIRCLE 302

CONFIGURABLE ANALYZER ADDS 80386 CAPABILITY

Gould Inc.'s Design & Test Systems Div., Cupertino, Calif., has added 80386 support to the CLAS 4000 Configurable Logic Analysis System. The 80386 Microprocessor Analysis Package (MAP) offers disassembly with symbolic address replacement in Intel-standard mnemonics at clock and data capture rates to 50 MHz. The analyzer-to-chip connection is through an interface module that accepts standard CLAS 4000 high-impedance probes. The MAP slows edge rates by less than 1.5 ns. The header that connects to the target board is 2.2 by 2.8 by 0.2 in., so it fits on high-density boards with a minimum spacing of 0.4 in. on three sides. The disassembler, which operates in 16- or 32-bit modes, can start at the beginning of the captured data or at any point within the recording. The 80386 MAP costs \$3000 and is available from stock. Call (800) 538-9320. JN

CIRCLE 303

GENERATOR PUTS OUT PULSES AT 300-MHZ RATE

With a 300-MHz repetition rate, the HP 8130A programmable pulse generator can test the fastest semiconductor devices at their rated speeds. The instrument features variable transitions from 1 ns to 100 μ s and 10-ps resolution for all timing parameters. Amplitudes from 100 mV to 5 V are possible in a ± 5 -V window. Full programmability over the HP-IB (IEEE-488) bus increases the unit's flexibility, especially in production ATE. The generator can also be used to analyze timing and level parameters. The HP 8130A sells for \$12,100, with an estimated delivery date of six weeks. For \$6300, an optional second channel has a synchronous period, but all other pulse parameters are independently programmable. Contact Hewlett-Packard at (800) 752-0900. JN

CIRCLE 304

SEALED ROTARY SWITCHES SUIT SCSI CONTROL

SCSI control and other 3-bit digital settings are among applications targeted for the S-8000 series of sealed DIP rotary switches from Mecopac Co., San Diego, Calif. The binary-coded, octal eight-position devices measure 0.283 by 0.283 by 0.156 in. They are sealed with an O-ring for trouble-free soldering and washing processes. Mechanical life is a minimum of 10,000 steps. The switches' gold-plated contacts are rated for 5 V dc at 100 mA (resistive) when switching, and 50 V dc (open) at 100 mA (closed) when not switching. In quantities of 1000, the switches cost \$1.59 each and are delivered in eight weeks after receipt of order. Call Leona Anderson, (619) 453-0332. DM

CIRCLE 305

OUTPUT MODULES OFFER DRY CONTACTS

True dry-contact switching of small or large ac and dc signals is accomplished by the DRY5 series of output modules from Brentek International Inc., Reading, Pa. The modules offer designers direct plug-in packaging for standard I/O racks, such as those from Gordos and Opto 22. I/O-system power-down defaults can be easily configured by selecting Form 1A or 1B types for predetermined I/O points. Switching current is rated at 1 A, 200 V ac or dc for Form 1A types; and 0.5 A, 200 V ac or dc for

Form 1B units. Operate and release times are less than 1 ms. Modules are available for 5-, 15-, and 24-V I/O systems. In quantities of 100 or more, the modules cost \$18.90. Small quantities are available from stock. Call Brian Breneman, (215) 375-7200. DM **CIRCLE 306**

ENHANCED IBM PS/2 ZIPS ALONG AT 33 MHZ

The MicroMaster 386 Series of CPU enhancement boards has a new addition: a 33-MHz version for IBM PS/2 Models 50, 60, and 50Z. By exploiting the Micro Channel architecture, the board, from Aox Inc., Waltham, Mass., multiplies the computer's power by five. It achieves this by becoming the primary source of instructions for the computer. The board simply slips into a standard 16-bit PS/2 slot and doesn't require the user to remove the existing 80286 CPU board. The PS/2 will recognize the MicroMaster 386 as the host processor. It can access system peripherals and memory and also direct the 286 processor to low-level tasks for more efficient computing. The board costs \$2495 and is available immediately. Lower-speed configurations are available at lower cost. RN

CIRCLE 307

ELECTROSTATIC COLOR PRINTER CUTS COST

With the ability to print D-size engineering drawings (22-by-34-in.) in full color, the Color Station D, a wide-format electrostatic printer developed by Raster Graphics Inc., Sunnyvale, Calif., slashes the cost of printing. As a result, a system can compete with slower, more expensive color pen plotters. The standard version of the electrostatic printer, which delivers a resolution of 200 dpi and prints at 2 ips, costs \$18,500. An optional package doubles the number of passes that the paper makes through the printer, pushing resolution to 400 dpi. The system can deliver 256-color plots for line drawings, and rendered images can be done from a palette of 16 million colors. The system has a proprietary write-head, which improves speed and accuracy while eliminating flare and striations in areas of solid fills. The system is compatible with HP-GL data and performs vector-to-raster conversion with data files from such packages as ADI, AT&T Truevision, Autodesk, Autosolid, and Targa. Weighing about 240 lbs., the system is about one-third the size and weight of other color electrostatic printers. Call Jack Androvich, (408) 738-7800. DB

CIRCLE 308

ENSURE TESTABLE ICs WITH TEST EXPRESS

Enhancing its suite of ASIC software design tools, VLSI Technology Inc., San Jose, Calif., has added Test Express, a program that integrates and optimizes various test techniques into a circuit's design-file description. The software encompasses multiple test methodologies—functional block isolation, built-in self-test, automatic test vector generation (ATVG), and scan cell—which are part of the company's Testable Design environment. Test Express includes several sub-programs: Test Assistant, BISTRAM and LFSR for BIST applications, ProFault for probabilistic fault simulation, and many automatic test vector generators. When optimizing a design for testability, the Test Express software offers ATVG as part of the RAM, ROM, PLA and multiplier compilers, and as part of the logic synthesis process. Vectors produced by the compilers can often eliminate weeks or months of the design time typically needed to generate the test vectors. The Test Express bundle of programs sells for \$70,000 and will be available this quarter. Call Bill Murray, (408) 434-7660. DB

CIRCLE 309


LATE-BREAKING WESCON PRODUCTS

A line of surface-mounted connectors from Hirose Electric, Simi Valley, Calif., includes five memory-card connectors with 0.050-in. centers. Contacts range from 38 to 90. Booth 4216. **CIRCLE 310...** Modular packaging that protects against dust and moisture to NEMA 12 standards is available from Optima Enclosures, Tucker, Ga. The 19-in. units also protect against interference as per FCC rules. Booth 1855. **CIRCLE 311...** European-styled switches and indicators from Eaton Corp., Milwaukee, suit ac and low-voltage dc applications. The switches handle up to 20 A. Booth 1738. **CIRCLE 312...** Audio cables from American Insulated Wire, Pawtucket, R.I., meet the noise-free demands posed by today's digital audio. The cables conform to UL ratings and can be made with thermoset or thermoplastic insulation. Booth 4200. **CIRCLE 313...** The ADS-928, a 14-bit sampling a-d converter from Datel, Mansfield, Mass., digitizes sinusoidal input signals at a minimum rate of 500,000 samples/s. The device sports $\pm 1/2$ -LSB linearity. Booth 1730. DM **CIRCLE 314**

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CIRCLE 41

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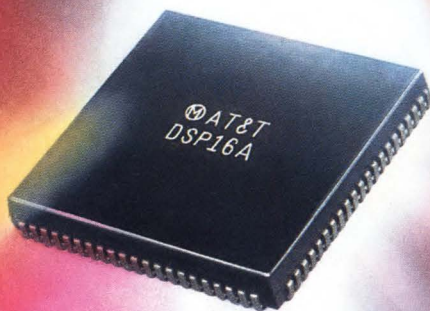
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CIRCLE 55

PROGRAMMABLE LOGIC CHIP FITS MULTIPLE MICROCONTROLLERS

IC HAS EPROM, RAM,
AND LOGIC FOR
45 CONFIGURATIONS;
INTERFACES
8- AND 16-BIT
MICROCONTROLLERS.

MILT LEONARD

The embedded-controller market embraces a myriad of 8- and 16-bit microcontroller architectures that can satisfy just about any conceivable application requirement. However, each different controller requires its own unique combination of discrete devices to link the part to other system elements. Furthermore, changing application requirements usually call for restructuring I/O ports. Consequently, the application may eventually outgrow system memory and shared resources may demand multiple chip solutions. This means that in addition to comparing controllers on the merits of price and performance, prospective users must also consider the external circuitry that the controller needs to interface to the rest of the system.

A new chip from WaferScale Integration Inc., Fremont, Calif., simplifies system integration by combining RAM, EPROM, programmable decoding, and configurable I/O ports that expand 8- or 16-bit microcontrollers when they run out of on-chip resources. WaferScale's MAP301 is the first single-chip solution to offer a microcontroller with port expansion, latched address lines, a programmable address decoder (PAD), an expansion interface to shared resources, a 256-kbit EPROM, and a 16-kbit static RAM. In addition, the chip links directly to popular 8- and 16-bit microcontrollers without using glue logic.

The MAP301 architecture is a major enhancement of WaferScale's MAP168 mappable memory chip introduced last year (*see ELECTRONIC DESIGN, July 28, 1988, p. 91*). In addition to the memory, decoding, and multiplexer functions of the 168, the 301 includes three software-configurable 8-bit I/O ports (A, B, and C), configuration registers, latched inputs, more chip-select lines, and more control on the strobe lines (*Fig. 1*). Like the 168, a programmable security bit is given to protect against reverse engineering.

Most controllers can't be reprogrammed once they're configured. Moreover, their controller's I/O ports are designed to perform one of two mutually exclu-

USER-CONFIGURABLE MICROCONTROLLER INTERFACE

sive functions: convey control signals to peripheral devices or address and data signals to shared resources. Supplying both of these functions requires a multiple chip solution.

Microcontrollers also differ in boot-up locations and address mapping in memory. The 8051 and 8096 microcontrollers, for example, locate boot-up sequences in the lower half of their memory maps, while the 80186/88 and 68HCXXX use a high memory boot-up address. Another factor is the differences in control-signal polarities.

The MAP301 is designed to adapt the characteristics of different microcontrollers to an embedded-control design. The PAD plays a major role in this function. It performs similarly to a small programmable array logic (PAL) device. The PAD has up to 13 inputs and 11 outputs in a NOR-gate array, and it can implement up to four sum-of-product expressions

based on address inputs, control signals, and chip-select inputs. The PAD selects all of the chip's internal parts, and generates external chip selects with a 35-ns delay.

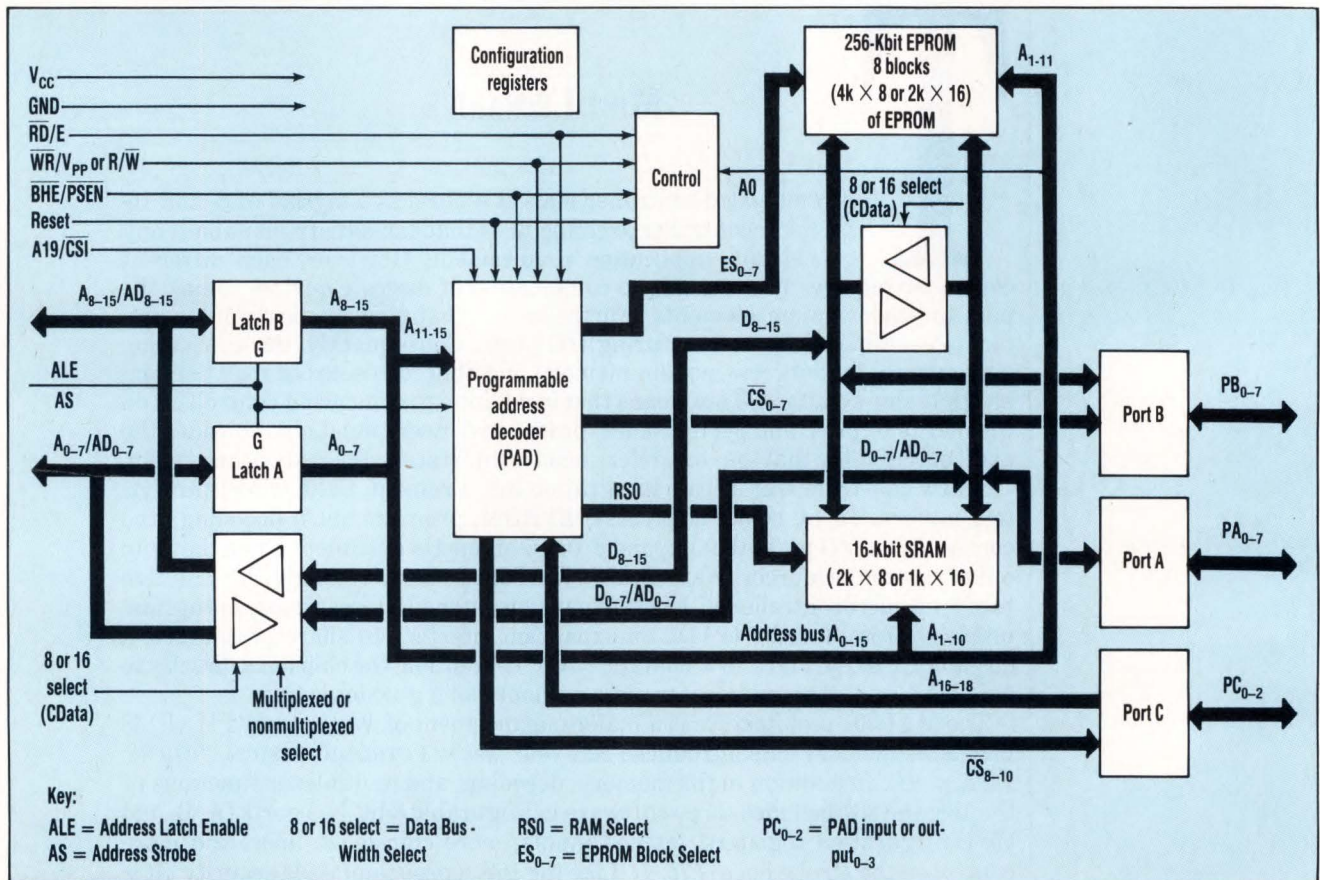
Address inputs from the host microcontroller are first fed to the 301's input latches, which stabilize the inputs when the device accesses memory in the multiplexed mode. The latches are made transparent in the nonmultiplexed mode. Five low-order address inputs and five programmable control lines are fixed functions; the Address-Latch-Enable and Reset lines have programmable polarity. The high-order address lines can be either address or general-purpose inputs for logic functions.

For more efficient use of memory space, internal and external PAD-Select signals can override EPROM memory with overlapping addresses. Therefore, if all of the EPROM isn't used for program storage, the

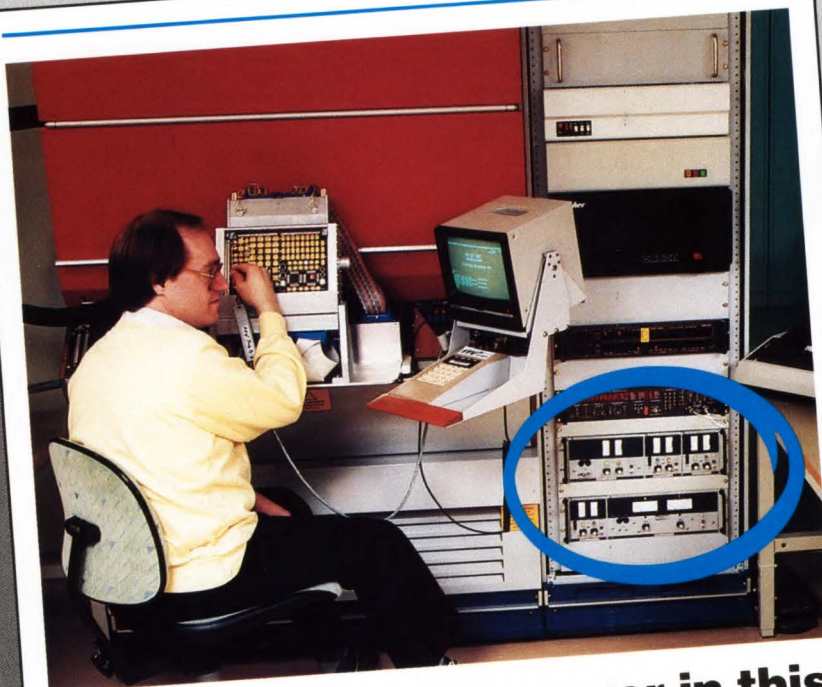
unused space can be allocated to I/O ports, static RAM, or other PAD-select signals.

The EPROM is configurable as 32 kwords by 8 bits, or 16 kwords by 16 bits, and it's partitioned into eight equal mappable blocks with a resolution of 4 kbytes or 2 kwords. Access time, including PAD decoding time, is 120 ns. The configuration registers also consist of EPROM cells. The registers store the programmed configuration bits that make it possible for users to set the device, I/O, and control functions according to the required operating mode. The 16-kbit 120-ns static RAM is configurable as 2 kwords by 8 bits, or 1 kword by 16 bits. The memory blocks can be noncontiguously mapped over the addressable range of 1 Mbyte or 0.5 Mwords. Consequently, programmers can scramble the code to prevent direct copying.

I/O ports A and B in the 8- and 16-



1. A HIGHLY RECONFIGURABLE MAP301 microcontroller peripheral from WaferScale Integration has multiplexed or nonmultiplexed data and address buses with selectable 8- or 16-bit bus widths. The programmable address decoder (PAD) helps supply up to 45 configuration options for supporting a range of 8- and 16-bit microcontrollers.



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INFLUENCE QUANTITY	OUTPUT EFFECTS VOLTAGE MODE		OUTPUT EFFECTS CURRENT MODE		OFFSETS ⁽⁴⁾	
	Typ.	Max.	Typ.	Max.	ΔE_{IO}	ΔI_{IO}
SOURCE VOLTAGE (min.-max.):	< 0.0005% E_0 max.	0.001% E_0 max.	< 0.002% I_0 max.	0.005% I_0 max.	< 1 μ V	< 1 nA
LOAD (no load-full load):	< 0.001% E_0 max.	0.002% E_0 max.	< 0.5 mA ⁽¹⁾	1 mA ⁽¹⁾	—	—
TIME (8-hour drift):	< 0.005% E_0 max.	0.01% E_0 max.	< 0.01% I_0 max.	0.02% I_0 max.	< 20 μ V	< 1 nA
TEMPERATURE, per °C:	< 0.005% E_0 max.	0.01% E_0 max.	< 0.01% I_0 max.	0.02% I_0 max.	< 20 μ V	< 2 nA
RIPPLE and NOISE ⁽²⁾ rms:	< 0.1 mV	0.3 mV	< 0.01% I_0 max.	0.03% I_0 max.	—	—
(Slow Mode) p-p: ⁽³⁾	< 1 mV	3 mV	< 0.1% I_0 max.	0.3% I_0 max.	—	—
RIPPLE and NOISE ⁽²⁾ rms:	< 1 mV	3 mV	< 0.01% I_0 max.	0.03% I_0 max.	—	—
(Fast Mode) p-p: ⁽³⁾	< 10 mV	30 mV	< 0.1% I_0 max.	0.3% I_0 max.	—	—
INPUT:	User Selectable 104, 115, 208, 250V a-c 47-65Hz single phase					

⁽¹⁾ For models with output current rating of 50A and higher, the load effect is 2 mA typical and 5 mA maximum. In slow mode, the leakage current through the output capacitor adds approximately 0-6 mA to the current mode load effect.

⁽²⁾ One terminal must be grounded for this measurement, or connected so that common mode current does not flow through the load or, in current mode, through the current-sensing resistor.

⁽³⁾ Peak-to-peak ripple is measured over a 20 Hz to 10 MHz bandwidth.

⁽⁴⁾ Uncommitted amplifier offsets.



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ACCESSORY FOR RACK MOUNTING: RA 37

50 WATTS 0-55°C No Derating QUARTER RACK SIZE A	MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
		VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT (2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
	ATE 6-5M	0-6	0-5	24 $\mu\Omega$	0.5 μH	5 μH	12 k Ω	1,000 μF	1 μF
	ATE 15-3M	0-15	0-3	100 $\mu\Omega$	0.5 μH	5 μH	30 k Ω	450 μF	0.4 μF
	ATE 25-2M	0-25	0-2	250 $\mu\Omega$	1 μH	10 μH	50 k Ω	250 μF	0.25 μF
	ATE 36-1.5M	0-36	0-1.5	480 $\mu\Omega$	1 μH	10 μH	72 k Ω	200 μF	0.2 μF
	ATE 55-1M	0-55	0-1	1.1 m Ω	2 μH	20 μH	110 k Ω	150 μF	0.15 μF
	ATE 75-0.7M	0-75	0-0.7	2.15 m Ω	2 μH	20 μH	150 k Ω	110 μF	0.1 μF
	ATE 100-0.5M	0-100	0-0.5	4 m Ω	4 μH	40 μH	200 k Ω	50 μF	0.05 μF
	ATE 150-0.3M	0-150	0-0.3	10 m Ω	4 μH	40 μH	300 k Ω	55 μF	0.02 μF

Size: 57 $\frac{32}{32}$ " H x 45 $\frac{32}{32}$ " W x 17 $\frac{16}{16}$ " D (132.6mm H x 105.6mm W x 435.0mm D)⁽¹⁾ Net Weight: 14 lbs. (6.4 kg.)

100 WATTS 0-55°C No Derating QUARTER RACK SIZE B	MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
		VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT (2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
	ATE 6-10M	0-6	0-10	12 $\mu\Omega$	0.5 μH	5 μH	12 k Ω	1,800 μF	2 μF
	ATE 15-6M	0-15	0-6	50 $\mu\Omega$	0.5 μH	5 μH	30 k Ω	1000 μF	0.8 μF
	ATE 25-4M	0-25	0-4	125 $\mu\Omega$	1 μH	10 μH	50 k Ω	500 μF	0.5 μF
	ATE 36-3M	0-36	0-3	240 $\mu\Omega$	1 μH	10 μH	72 k Ω	350 μF	0.4 μF
	ATE 55-2M	0-55	0-2	0.55 m Ω	2 μH	20 μH	110 k Ω	200 μF	0.3 μF
	ATE 75-1.5M	0-75	0-1.5	1 m Ω	2 μH	20 μH	150 k Ω	110 μF	0.2 μF
	ATE 100-1M	0-100	0-1	2 m Ω	4 μH	40 μH	200 k Ω	80 μF	0.1 μF
	ATE 150-0.7M	0-150	0-0.7	4 m Ω	4 μH	40 μH	300 k Ω	55 μF	0.04 μF

Size: 57 $\frac{32}{32}$ " H x 45 $\frac{32}{32}$ " W x 17 $\frac{16}{16}$ " D (132.6mm H x 105.6mm W x 435.0mm D)⁽¹⁾ Net Weight: 17 lbs. (7.7 kg.)

ACCESSORY FOR RACK MOUNTING: RA 37

250 WATTS 0-55°C No Derating HALF RACK SIZE C	MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
		VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT (2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
	ATE 6-25M	0-6	0-25	4.8 $\mu\Omega$	0.5 μH	5 μH	12 k Ω	11,000 μF	5 μF
	ATE 15-15M	0-15	0-15	20 $\mu\Omega$	0.5 μH	5 μH	30 k Ω	5,800 μF	2 μF
	ATE 25-10M	0-25	0-10	50 $\mu\Omega$	1 μH	10 μH	50 k Ω	2,900 μF	1.25 μF
	ATE 36-8M	0-36	0-8	90 $\mu\Omega$	1 μH	10 μH	72 k Ω	2,400 μF	1 μF
	ATE 55-5M	0-55	0-5	0.22 m Ω	2 μH	20 μH	110 k Ω	1,400 μF	0.75 μF
	ATE 75-3M	0-75	0-3	0.5 m Ω	2 μH	20 μH	150 k Ω	850 μF	0.5 μF
	ATE 100-2.5M	0-100	0-2.5	0.8 m Ω	4 μH	40 μH	200 k Ω	375 μF	0.25 μF
	ATE 150-1.5M	0-150	0-1.5	2 m Ω	4 μH	40 μH	300 k Ω	275 μF	0.1 μF

Size: 57 $\frac{32}{32}$ " H x 81 $\frac{32}{32}$ " W x 17 $\frac{16}{16}$ " D (132.6mm H x 211.9mm W x 435.4mm D)⁽¹⁾ Net Weight: 35 lbs. (15.9 kg.)

ACCESSORY FOR RACK MOUNTING: RA 37

500 WATTS 0-55°C No Derating THREE-QUARTER RACK SIZE D	MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
		VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT (2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
	ATE 6-50M	0-6	0-50	2.4 $\mu\Omega$	0.5 μH	5 μH	12 k Ω	12,000 μF	10 μF
	ATE 15-25M	0-15	0-25	12 $\mu\Omega$	0.5 μH	5 μH	30 k Ω	8,000 μF	4 μF
	ATE 25-20M	0-25	0-20	25 $\mu\Omega$	1 μH	10 μH	50 k Ω	5,800 μF	2.5 μF
	ATE 36-15M	0-36	0-15	48 $\mu\Omega$	1 μH	10 μH	72 k Ω	4,900 μF	2 μF
	ATE 55-10M	0-55	0-10	0.11 m Ω	2 μH	20 μH	110 k Ω	2,900 μF	1.5 μF
	ATE 75-8M	0-75	0-8	0.19 m Ω	2 μH	20 μH	150 k Ω	1,200 μF	1 μF
	ATE 100-5M	0-100	0-5	0.4 m Ω	4 μH	40 μH	200 k Ω	600 μF	0.5 μF
	ATE 150-3.5M	0-150	0-3.5	0.86 m Ω	4 μH	40 μH	300 k Ω	440 μF	0.2 μF

Size: 57 $\frac{32}{32}$ " H x 121 $\frac{32}{32}$ " W x 17 $\frac{16}{16}$ " D (132.6mm H x 318.3mm W x 435.4mm D)⁽¹⁾ Net Weight: 43 lbs. (19.5 kg.)

The full rack model is supplied with brackets for direct mounting in a standard 19-inch rack.

1000 WATTS 0-55°C No Derating FULL RACK SIZE E	MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
		VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT (2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
	ATE 6-100M	0-6	0-100	1.2 $\mu\Omega$	0.5 μH	5 μH	12 k Ω	22,000 μF	15 μF
	ATE 15-50M	0-15	0-50	6 $\mu\Omega$	0.5 μH	5 μH	30 k Ω	12,000 μF	6 μF
	ATE 25-40M	0-25	0-40	12.5 $\mu\Omega$	1 μH	10 μH	50 k Ω	11,000 μF	4 μF
	ATE 36-30M	0-36	0-30	24 $\mu\Omega$	1 μH	10 μH	72 k Ω	9,500 μF	3 μF
	ATE 55-20M	0-55	0-20	55 $\mu\Omega$	2 μH	20 μH	110 k Ω	5,200 μF	2.25 μF
	ATE 75-15M	0-75	0-15	0.1 m Ω	2 μH	20 μH	150 k Ω	3,400 μF	1.5 μF
	ATE 100-10M	0-100	0-10	0.2 m Ω	4 μH	40 μH	200 k Ω	1,200 μF	0.75 μF
	ATE 150-7M	0-150	0-7	0.42 m Ω	4 μH	40 μH	300 k Ω	1,050 μF	0.3 μF

Size: 63 $\frac{1}{32}$ " H x 161 $\frac{1}{2}$ " W x 20 $\frac{1}{16}$ " D (177.0mm H x 419.1mm W x 508.4mm D)⁽¹⁾ Net Weight: 87 lbs. (39.5 kg.)

⁽¹⁾Add 2 $\frac{1}{2}$ " (63.5mm) for connector protrusion. ⁽²⁾Based on 0.5 mA load effect in FAST mode.

⁽³⁾For determining dynamic impedance in voltage mode. ⁽⁴⁾For determining dynamic impedance in current mode.

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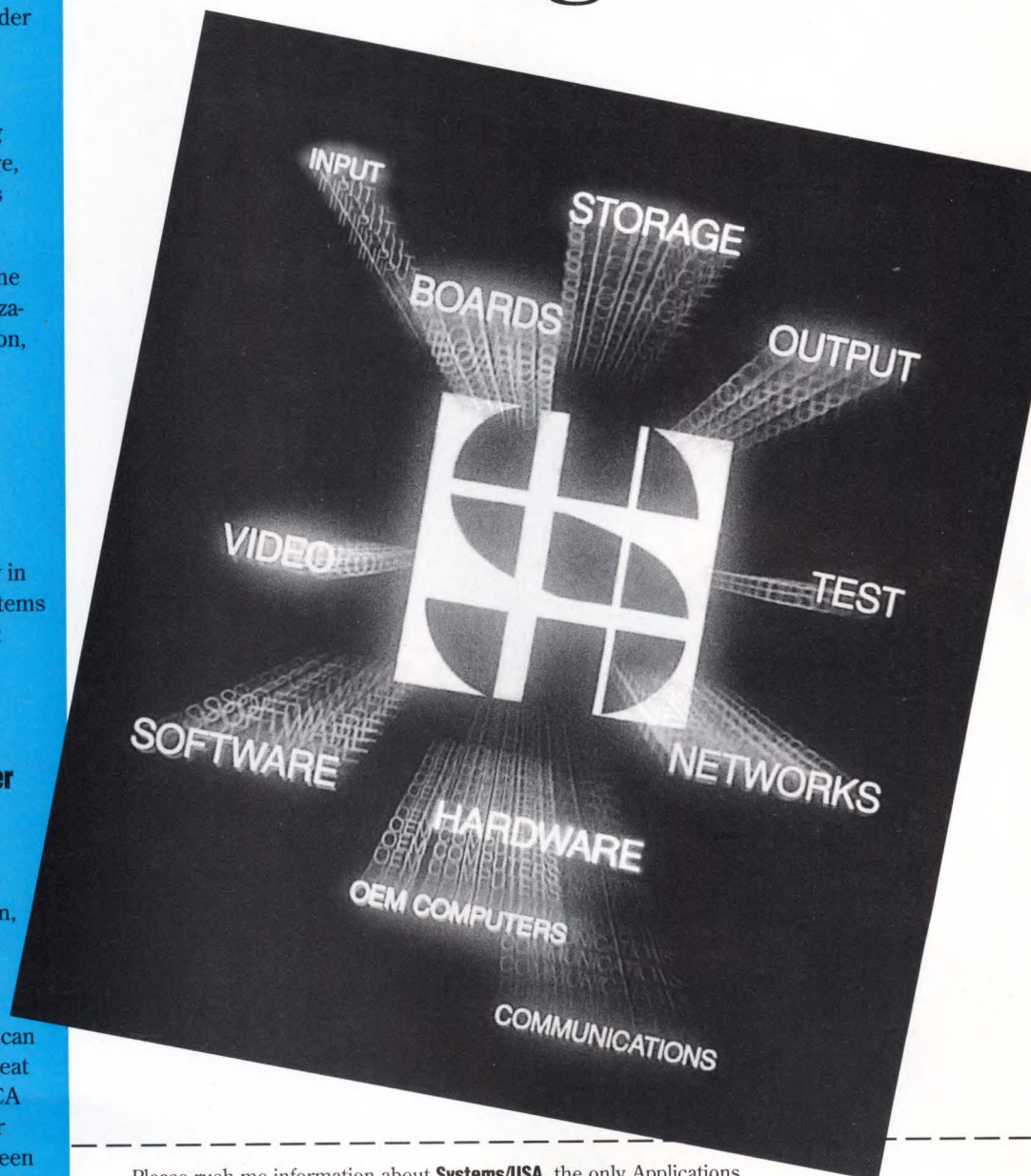
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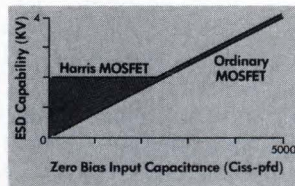


Harris announces power MOSFETs with ESD protection at a price that will shock the competition.

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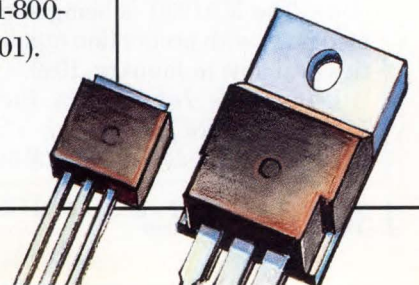
Yet, for all their advantages, the new Harris logic level 3055 series power MOSFETs cost no more than competitive devices. As low as 25 cents in quantity.

And they're available today in both D-pak and TO-220 packages. For more information and samples, just give us a call at 1-800-4-HARRIS, ext. 1001 (in Canada, 1-800-344-2444, ext. 1001). Or call your local Harris sales office or distributor.

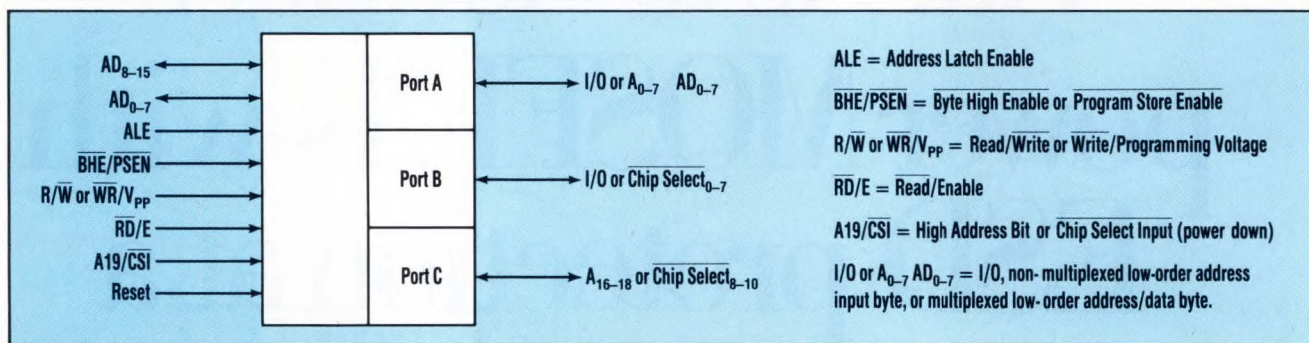
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USER-CONFIGURABLE MICROCONTROLLER INTERFACE



2. I/O PORT CONFIGURATION FOR THE MAP301 IS PROGRAMMED by signals from the PAD, which are derived partly from programmed bits in the configuration registers. The three ports configured for multiplexed address and data with a 16-bit wide data bus are shown.

bit configurations are data ports in the nonmultiplexed mode, and both ports can be configured as either data or address ports in the multiplexed mode (Fig. 2). Port C is independent of any configuration—it can supply multiple chip-select outputs or serve as address inputs.

The default configuration of port A in the nonmultiplexed address/data mode sets the port to deliver I/O lines. In this mode, each pin can be set as an input or output and can have a CMOS or open-drain output. Alternatively, each bit of port A can be configured as a low-order latched-address-bus bit to access external peripherals or memory that requires several low-order lines. Another option in this mode sets the entire port to track the low-order address/data multiplexed bus. This feature links the host microcontroller to shared resources without the use of external buffers and decoders.

In the nonmultiplexed mode, port

A becomes the chip's low-order data-bus byte. When a read operation is executed from an internal 301 location, data is directed out on port A pins. When a write cycle is executed into an internal 301 location, data is driven into port A.

The operation of port B in the multiplexed address/data and 8-bit non-multiplexed modes is the same as port A. However, as an alternative, each bit can be configured to supply a Chip-Select Output signal from the PAD. In the 16-bit nonmultiplexed mode, port B is the high-order data-bus byte of the chip. When a read operation is executed from an internal high-order data-bus byte location, the data appears on port B pins. When a write operation is executed into an internal high-order data-bus byte location, data and write operation signals are present at port B.

Each pin of port C in all modes can be configured as an input or output from the PAD. Although designated as high-order address bus pins, they can be used for any logic inputs to the PAD or for external chip-select outputs from the PAD.

With this degree of operational flexibility, the 301 can team up with all popular 8- and 16-bit microcontrollers from such companies as Advanced Micro Devices, Intel, Motorola, National Semiconductor, Texas Instruments, and Zilog. For example, the polarity of the 301's control signals can be programmed for direct connection of the read-write and output enable pins of the 68HCXX microcontroller family. The 16-bit configuration can boost the perfor-

mance of 16-bit controllers, such as the 80186, 8096, 80196, 16000, and others, without adding external devices. And the 8051 microcontroller family can extend its memory space by using the separate address and program memory space of the 301. The 301 is cascadable for increased width or depth for multiplexed byte- or word-wide embedded-control designs.

In the standby mode, commercial versions of the 301 draw 150 μA and 1.5 mA for CMOS and TTL interfaces, respectively. Active current for CMOS interfaces with or without selected memory blocks, or with the EPROM blocks selected, is 55 mA. That level increases to 80 mA for TTL interfaces. Selecting the static RAM block increases active current to 105 mA and 130 mA for CMOS and TTL, respectively.

WaferScale Integration houses the device in a 44-pin surface-mounted package to meet the form-factor requirements of such products as 5.25-, 3.5-, and 2.5-in. disk drives, cellular phones, and modems. System development tools include an IBM-PC plug-in programmer board and remote socket adaptor. They also contain a software development package that runs on an IBM PC/XT/AT or compatible computer with a MS-DOS version 3.1 or higher, 640 kbytes of RAM, and a hard disk. □

PRICE AND AVAILABILITY

The commercial version of the MAP301, packaged in a 44-pin plastic leaded chip carrier, is priced at \$15 each in quantities of 1000. Military parts are also available. Other package options are ceramic leaded chip carriers and pin grid array packages with windows. The MAP301 is being sampled now, with production quantities available in January, 1990.

WaferScale Integration Inc., 47280 Kato Rd., Fremont, CA 94538; (415) 656-5400. **CIRCLE 514**

HOW VALUABLE?

HIGHLY
MODERATELY
SLIGHTLY

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565
566
567



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ELECTRICAL/COMPUTER: BSEE/MSEE/BSCE/BSCE or equivalent. Seeking experience in any of the following areas: analog and RF circuit design; receiver or transmitter RF circuits; LCD display technology, acoustics, and 8-bit microprocessor software; infrared and fiber optics; low speed data; digital modulation; 900 Mhz RF power amplifier design with hybrid or microstrip circuitry; RF device development; parallel and/or push-pull RF amplifier design at 900 Mhz or UHF; A/D and D/A converters; RF propagation; passive/active filter theory; microwave antenna design; UL, EMI and RFI requirements; HP 3062 test system; HP 9000; digital hardware, microprocessor applications and interfaces; digital switching technology; firmware development methodology; PCM and digital telephony; digital signal processing; ASIC design; LAN systems, PSTN standards, ISDN standards, processor architectures, high speed logic; 16-bit MPU design practices, programmable logic; digital modulation, synchronization, adaptive signal processing, viterbi algorithm and MLSE, decision feedback equalizer; convolutional code and linear block code, speed coding, echo cancellation, encryption; CAE techniques for digital hardware design using Mentor Graphics, etc.; data communications protocols (CCITT #7, OSI,

X.25, X.75, PAD, LAPB, LAPD, Ethernet, ISDN, CCITT V Series modem, group 3 fax); computer network management/administration (Apollo, Sun, Mentor Graphics, AppleTalk). **Refer to Dept. #EC/YF.**

SYSTEMS: BSEE/BSCE/BSCE or equivalent. We are seeking persons with experience in any of the following technologies: radio/cellular communication systems engineering; RF propagation prediction methods; PSTN traffic planning; telephone network, interconnection and telecommunication industry standards; microwave system design and equipment engineering; telephone switching systems; software programming skills. **Refer to Dept. #SY/YF.**

MANUFACTURING: BSME/BSEE or equivalent; and experience in any of the following areas: CAD/CAM or robotics assembly; pedros and bills of material; automatic placement equipment, robots or machine controllers; surface mount technology; reflow and wave solder techniques; automatic chip component placement (Fuji machines preferred); front-end printed circuit card production. **Refer to Dept. #MA/YF.**

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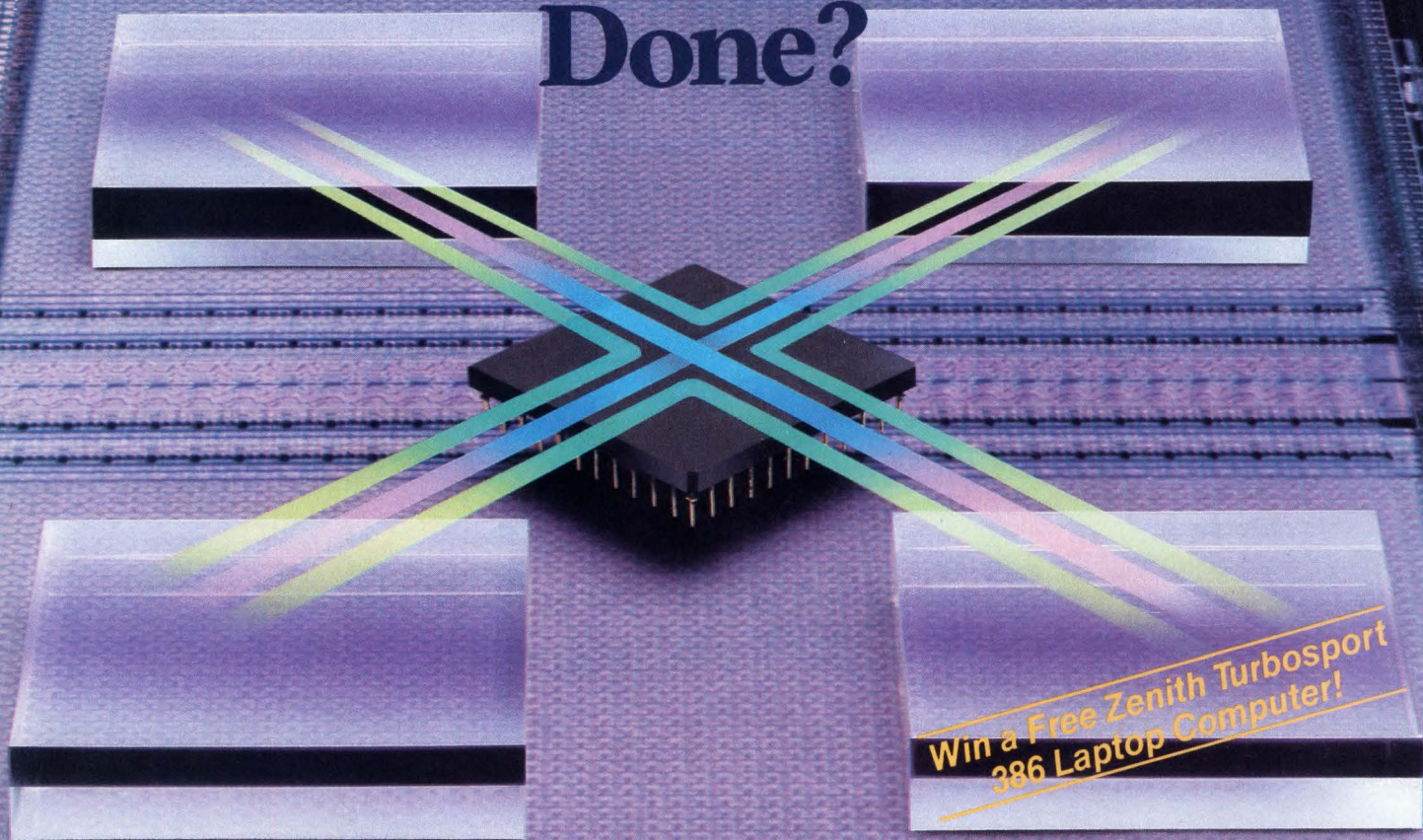


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8-BIT CPU FAMILY BOOSTS THROUGHPUT.

STREAMLINED CONTROLLERS UP INSTRUCTION RATES

DAVE BURSKY

As embedded control applications that rely on 8-bit microcontrollers get more challenging, current generation single-chip microcontrollers are starting to bog down as applications demand more processing in less time. And, due to system cost constraints, most applications can't afford to move to the more powerful and costlier 16-bit all-in-one processors. To solve that processing dilemma, a forthcoming family of 8-bit controllers from NEC manages to boost the throughput by moving to an architecture that resembles the latest reduced-instruction-set computers.

The NEC family processors have more efficient instructions that require just two clock cycles to execute, rather than the typical 8 to 16 cycles needed by such popular chips as the Intel 8051 and the Motorola 68HC11. However, rather than use its existing 8-bit microcontroller architecture, NEC decided to create a new, more streamlined family—the 78K2 series—which can execute its 65 commands at a rate of one instruction every two clock cycles. Consequently, with a 12-MHz

clock, NEC's controllers have a minimum instruction execution time of 333 ns. That time will shrink to 250 ns when the clock frequency goes up to 16 MHz in an upgraded version already slated for early 1990.

There will initially be three members in the 78K2 series that will be offered in the U.S., the μ PD78224, 78220, and 78P224. All of them have the same resources, except for the nonvolatile storage. The 78224 comes with 16 kbytes of ROM, 640 bytes of RAM and 63 I/O lines. The 78220 contains no ROM and can address external memory. And the 78P224 substitutes on-chip EPROM for the ROM instruction storage area. Beyond those chips, NEC plans to release the 78233 and 78234, which are ROM-less and ROM-based versions of the 7822x series that include dual-channel 8-bit digital-to-analog converters and the ability to build an 8-channel, 8-bit a-d converter (*see the figure*).

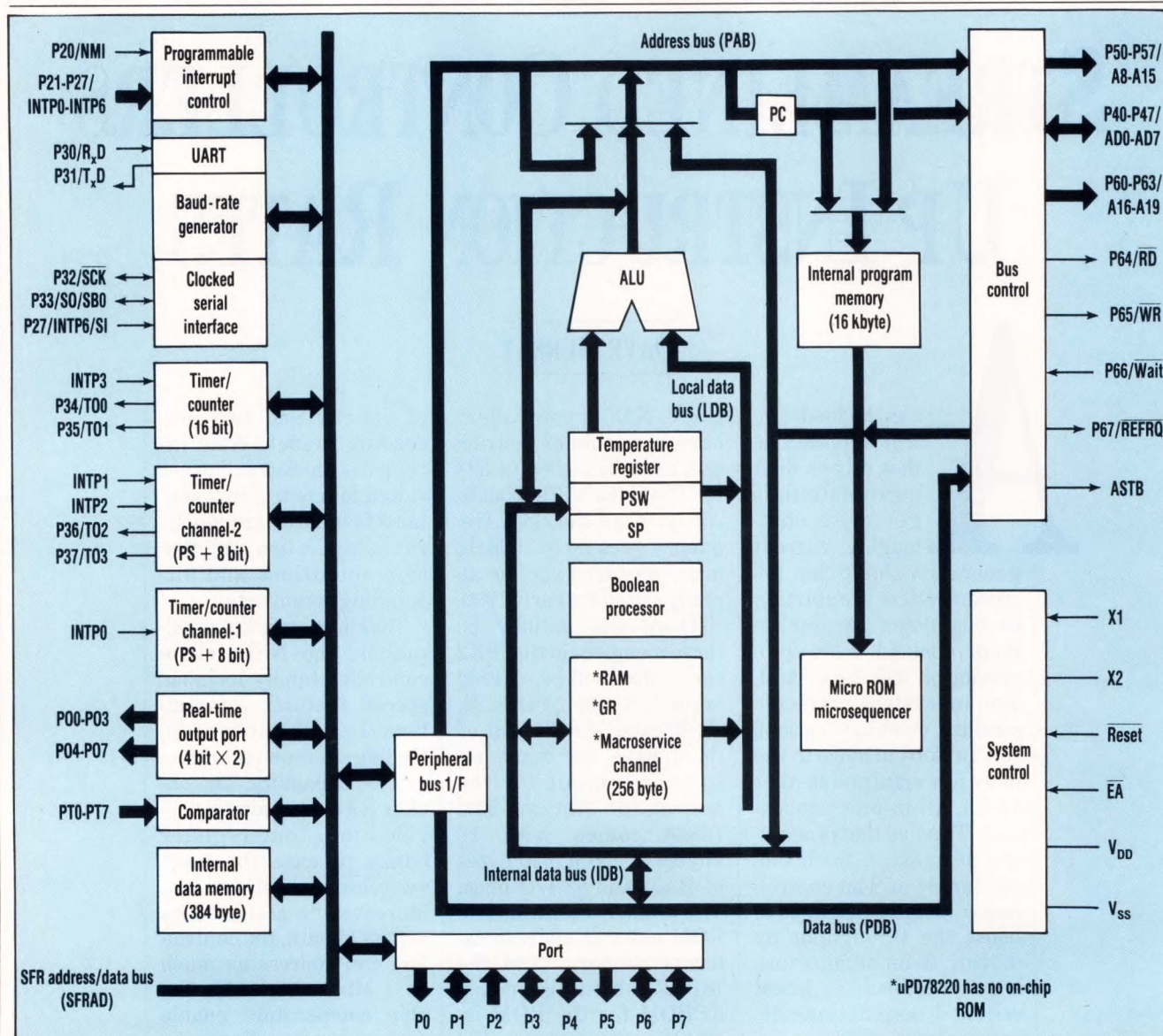
Common resources beyond the memory include a clocked serial channel, a full serial UART port, three counter-timers (one 16-bit and a pair of 8-bit units), and an on-chip interrupt controller capable of two programmable levels

of priority and two processing modes. Also included is an instruction set suited for control that contains fast hardware-assisted multiplication and division operations and bit-handling commands.

Tackling complex applications, the NEC microcontroller family includes special features for real-time I/O operations, including an unusual microservice capability. The on-chip RAM can also be divided into four register banks to ease the task-switching applications. Moreover, to access large arrays of data, the controllers can address as much as 1 Mbyte of RAM. On-chip comparators enable designers to configure up to eight-channel 8-bit a-d converters, two-channel d-a converters, and 8-channel analog comparators.

The macroservice routine aspect of the I/O channels makes it possible for bit, nibble, or byte-wide data to be transferred automatically from memory to a real-time output port. This ability frees designers to come up with such applications as eight-variable frequency-duty-cycle pulse-width modulated controllers to stepper-motor acceleration-deceleration patterns. The

ENHANCED 8-BIT CPU FAMILY



PACKING MORE FEATURES than the Microchip controllers, the NEC 78K2 series offers serial ports, a virtual I/O processor, and analog-interface circuits that implement a-d converters, pulse-width modulated controllers, and d-a converters.

PRICE AND AVAILABILITY

The PIC 16C54 and C55 will come in 18- or 28-lead one-time programmable plastic or windowed reprogrammable ceramic packages. The 16C54 sells for \$2.40 (2500); the 16C55 costs \$2.95. Production quantities are immediately available. The NEC 78K2 comes in plastic leadless packages and costs \$6.70 in lots of 10,000.

NEC Electronics Inc., 401 Ellis St., P.O. Box 7241, Mountain View, CA 94039; Ian Olsen, (415) 960-6000. **CIRCLE 512**

macro-service capability can be compared to a virtual I/O processor because the service feature operates somewhat behind the scenes to transfer either individual bytes or blocks of data, which can be transferred between any combination of memory and peripherals.

Macro-service ports can handle the rapid output of tabular information, such as information for nonlinear PWM systems. Associated with the I/O lines, the processors have 256 kbytes of special function registers. Those registers aid the implementation of logic operations associated with an I/O line. The tabular trans-

fers can calculate the ΔF (change in force) and ΔT (change in time), as required by a stepper motor. Future family members will include versions with more EPROM and I/O lines, as well as some advanced analog features. The newly released devices, though, can implement 8-bit 8-channel a-d converters, eight 4-bit analog comparators, or dual 8-bit d-a converters. □

HOW VALUABLE?

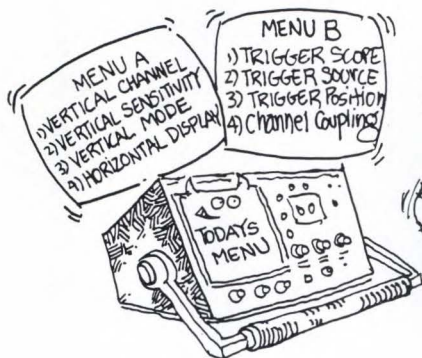
HIGHLY
MODERATELY
SLIGHTLY

CIRCLE

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"USER-FRIENDLY" IS THE WATCHWORD FOR TODAY'S OSCILLOSCOPES.

Recent advances in oscilloscope technology have proceeded at a very rapid pace. Almost across the board these advances have been beneficial. In these "high-tech" units, manufacturers have held out the promise of a scope loaded with every feature under the sun. And from auto setup to menu select capabilities, every function is shown to be ac-



cessible at the touch of a button. But a true reading of a scope's user-friendly potential cannot be obtained until the scope is applied to an actual project. Only at that point can it be determined how much time it will take to gain full use of the oscilloscope.

A new unit may allow work to proceed without a hitch. But where things haven't gone smoothly, situations similar to this have been reported. Turn on the new unit and a menu immediately appears. Should horizontal display, triggering, channel coupling, or another of the many alternatives listed be chosen? Triggering is chosen, but then a sub-menu is displayed. Now a decision has to be made among trigger source, trigger coupling, trigger slope, etc. Okay, trigger source is opted for and set. Now, if information from another menu is needed, trigger source must be exited and the needed menu brought up. With all this going on, the engineer may become distracted from the task at hand — the close observation of waveforms on the screen.

This potential for confusion points up exactly why careful examination has to be made when equipment is advertised as user-friendly. A closer look may reveal that sophisticated, menu-driven scopes are not always the easiest to operate. A new scope that builds and improves on controls that are already being used efficiently may turn out to be the most user-friendly. Toward this end, a number of features have been developed that improve the efficiency and precision of conventional oscilloscopes. Among these features are cursors with digital readouts, auto ranging, and relative hold-off, to name a few.

CURSORS WITH DIGITAL READOUTS — A QUANTUM LEAP IN EFFICIENCY

One user-friendly breakthrough, in terms of both speed and accuracy, has been the development of cursors.

Whereas older scopes required counting graticule divisions, cursors now allow measurements to be displayed digitally. Cursors supply readouts such as time, voltage, frequency, and phase, plus time and voltage difference ratios. Time difference ratio is ideal for performing phase shift measurement. With

voltage difference ratio, the measurements of waveform overshoot can be made. The cursors make measurement of waveform parameters more consistently accurate.

On-screen readouts provide a constant reminder of operating conditions and keep a record of these settings in waveform photographs. Many important settings are displayed, including TV field/line setting, which expands the oscilloscope to video-related applications.

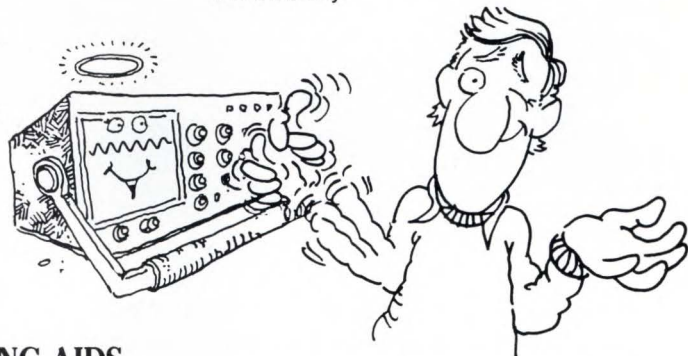
AUTO RANGING AIDS TIME BASE SELECTION

Of great help is a scope that offers both auto ranging and alternate time base. Auto ranging selects from 22 possible time base settings to display an optimum number of cycles. This is another feature that makes an oscilloscope a bit more user-friendly. Alternate

time base allows observation of both the main and the delay time base, so that the expanded portion of the waveform can be simultaneously compared with the original.

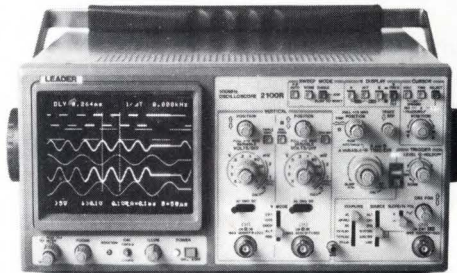
ANOTHER FEATURE TO CONSIDER CAREFULLY — DOES THE WARRANTY HAVE TEETH?

Another factor that needs to be examined just as closely as those mentioned previously is the warranty. In competing for market share, longer and more extensive warranties are offered every year. Before basing a decision only on warranty, though, consider its true value if the equipment is not reliable. Remember, no warranty can make up the cost of a scope that's out for repairs for 4 to 6 weeks, or more. That's why even more important than the actual wording of a warranty is the reliability that's built into every oscilloscope. Ideally, of course, no piece of equipment should ever break down. But if a unit needs repair, it's important to know who provides the fastest turnaround time in the industry.



Now there is an oscilloscope whose user-friendly format includes all the features discussed earlier, plus many more. This unit, introduced by Leader Instruments Corporation, is the 100 MHz CRT readout with cursors, Model 2100R. The unit is easy to use and also incorporates these additional features: TV full-line selection, alternate triggering, and relative hold-off. This and every other Leader product come with an iron-clad 2-year warranty, which is backed by a return rate of less than 1% during the warranty period and a very rapid turnaround time. In other words, the 2100R offers a complete oscilloscope package.

For more information or Leader's full-line catalog, call toll free: 1 800 645-5104. In NY call 516 231-6900. Or write Mike Hoyer at Leader Instruments Corporation, 380 Oser Avenue, Hauppauge, NY 11788.



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Clock Speed		
33 MHz	25ns	10ns
25 MHz	35ns	13ns

*All timing rated at 100 pF loads. The MT56C0816 is available in a 52-pin plastic leaded chip carrier (PLCC).

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MICRON
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CIRCLE 36

ECL ARRAY BOASTS SPEED; EMBEDDED ARRAY FLAUNTS DENSITY, FAST TURNAROUND

LISA GUNN

Gate arrays introduced by Fujitsu Microelectronics Inc. and LSI Logic Corp. present very different offerings to ASIC designers. With 80-ps peak gate speeds, Fujitsu's 30,000-gate ECL array is one of the fastest to date. The LSI Logic array, on the other hand, combines the best of the standard-cell and gate-array worlds. It incorporates embedded megacells in its structure to obtain the density and performance of cell-based designs and the fast prototype turnaround of gate arrays.

The 30,000-gate ECL array from Fujitsu is the first device in a new family of ECL arrays. The E30000VH chip boasts typical individual gate speeds of 80 ps unloaded, and 240 ps when loaded with a fanout of three and a line length of 3 mm. A fixed-clock distribution scheme guarantees less than 150 ps of clock skew to internal gates. To save power, high speed is used on the circuit only where needed. Total chip power dissipation is typically 15 to 30 W.

Gate counts range from 29,568 to 38,948 gates, depending upon the application. The E30000VH has 300 I/O pins, with over 200 of the pins acceptable for use as outputs. The I/O pins can be compatible with either 10KH (-5.2-V) or 100K (-4.5-V) systems. In addition, the chip needs a -3.3-V supply.

The LEA100K EmbeddedArray Series from LSI Logic takes an innovative "systems on a chip" approach to ASIC design. The new arrays are 0.7- μ m channel length, channel-free, HCMOS devices into which user-defined, cell-based structures—megacells or memory—can be embedded. With this technology, the designer can create a device of up to 150,000 equivalent gates using a combination of cell- and array-based methodologies (see the photo). Yet complete prototype metalization, assembly, and test is completed in as little as 14 days, the same as for a gate array.

Designers select the cell-based

blocks to be embedded on a base array. These blocks can consist of memories, megacells, or user-defined cores in a standard-cell format. The blocks can be positioned in any location on the base array. The designer then implements random logic and soft-coded megafunctions in the channel-free array, using the remaining area of the LEA100K design.

Memory blocks that can be embedded into LEA100K designs include high-speed static RAMs of up to 144 kbits, multiport RAMs with up to five ports, and a variety of specialized memories. Megafunctions include RISC microprocessors, floating-point controllers, communications controllers, adders, multipliers, and barrel shifters.

The Fujitsu E30000VH gate array comes in a 441-pin ceramic, surface-

mount PGA with 50-mil spacing and a choice of preattached heat sinks. Design input is being accepted now, with engineering samples and production quantities available in the first and second quarters of 1990, respectively. The E30000VH gate array costs \$1600 each in quantities of 10,000.

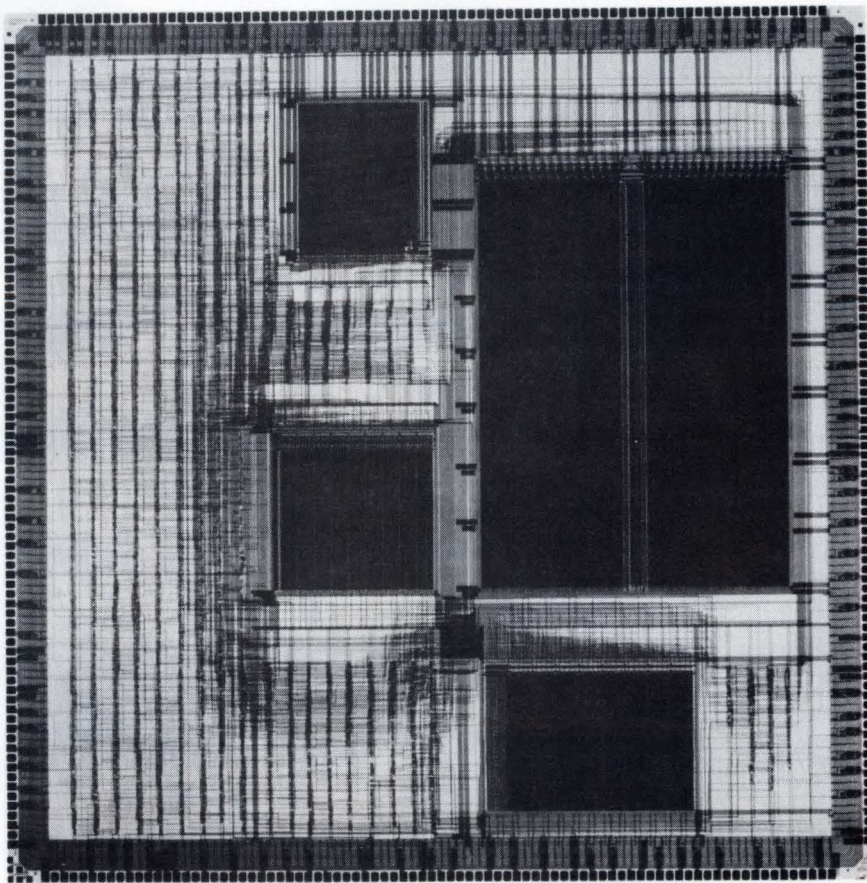
The LSI Logic LEA100K EmbeddedArray Series is available now. Packaging includes the full range of plastic and ceramic dual in-line packages, leadless and leaded chip carriers, pin-grid arrays, and quad flat-packs.

Fujitsu Microelectronics Inc., Integrated Circuits Division, 3545 N. First St., San Jose, CA 95134-1804; (800) 642-7616.

CIRCLE 392

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035; (408) 433-8000.

CIRCLE 393



NEW PRODUCTS

DIGITAL ICs

FAST PUBLIC-KEY DATA- ENCRYPTION SYSTEM SECURES NETWORKED INFORMATION

With throughput of 150 kbits/s, the CA34C168 data-encryption processor from Newbridge Microsystems secures the information circulating in computer networks without degrading system performance. The burgeoning need for network security can be seen from the increase in computer viruses and electronic theft.

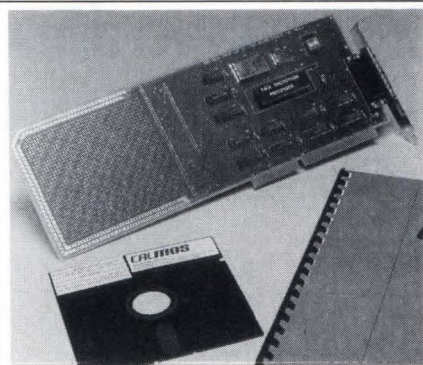
The processor's public-key architecture uses pairs of reciprocal keys, which enables users to send data to other users using a public key. Only the recipient, however, has the private key that unlocks the data.

The public-key architecture solves the problems associated with distribution of keys, digital signatures, transaction verification, and key exchanges. Solving these problems

with conventional private-key schemes is either more cumbersome or impossible.

The general-purpose architecture of the processor is oriented to the needs of communication systems. Forty high-level instructions let users implement their own cryptographic protocols for key management, authentication, and data encryption in either block or stream-cipher modes. The device contains two 256-bit write-only registers for secure key storage, a mask-programmable key for user and equipment verification, and a level of error detection for catastrophic cryptographic errors.

A range of development products are available to support the processor. These include the EDS-001 D evaluation and development system for use on the IBM PC/XT. With the system, users have a powerful, user-friendly environment in which to cre-



ate CA34C168-based cryptosystems.

The CA34C168 processor costs \$175 in quantities of 100 and is available now in small lots. The EDS-001 D development system goes for \$1950. The two-node EDS-002 system costs \$2950. Both are available in sample quantities.

Newbridge Microsystems, 20 Edgewater St., Kanata, Ontario, Canada, K2L 1V8; (613) 836-1014.

CIRCLE 337

DAVID MALINIAK

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NEW PRODUCTS

DIGITAL ICs

100-V, 8-CHANNEL LATCHED SINK-DRIVER DROPS INTO 50-V DEVICE SOCKETS

Built on a high voltage bipolar-CMOS-DMOS process, Micrel's MIC4807 latched-sink driver converts TTL-compatible microprocessor-bus signals into eight latched current-sinking outputs rated at 80 V each. Applications include computer control of lamps, solenoids, relays, print heads, and driving large power MOSFETs connected as high-side switches. It can also drive high-voltage displays.

The Micrel device is a pin-for-pin replacement for the 50-V UCN4807, but offers advantages compared with that part. While the MIC4807 operates from one 5-to-15-V logic supply and draws just 10 mA, the UCN4807 needs 50 mA and an additional 5-V base-drive source for its bipolar output transistors. With the

MIC4807, all eight outputs internally limit their current at 200 mA in the event of a short to the positive supply. In addition, if the chip's temperature rises above 145°C because of repeated or continuous faults, the on-board overtemperature sensor shuts it down. The chip's built-in 100° of hysteresis permit it to start again when it reaches 45°C.

At 25°C and with a 10-V logic supply, the DMOS output transistors have an on-resistance of 7 Ω maximum. With a similar supply voltage, saturation voltage is 0.35 V while sinking 50 mA and 0.70 V while sinking 100 mA.

In quantities of 100, the MIC4807 latched-sink driver costs \$3.95 in an 18-pin plastic DIP. Small quantities are available from stock.

Micrel Inc., 560 Oakmead Pkwy., Sunnyvale, CA 94086; Robert Johnson, (408) 245-2500.

CIRCLE 315

FRANK GOODENOUGH

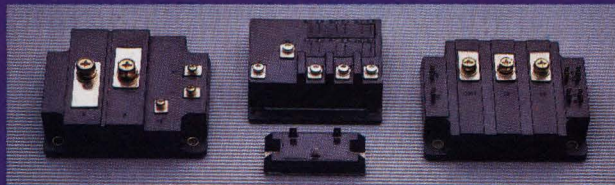
HYBRID MULTIPLEXER SERVES MIL-STD-1553

Operating over the full military temperature range of -55° to +125°C, the BUS-61555 provides a flexible solution for MIL-STD-1553 interface applications. The Advanced Integrated Mux hybrid requires only a +5-V power supply and consists of a complete bus controller, remote terminal unit, bus monitor terminal protocol, memory-management and host interface IC, and 8 by 16 bits of CMOS SRAM. Using an industry-standard dual transceiver and standard status and control signals, the BUS-61555 simplifies system integration at both the MIL-STD-1553 and host-processor interface levels. It is packaged in a 78-pin DIP and sells for \$1475. Delivery takes 30 to 90 days.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 563-5678.

CIRCLE 316

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CIRCLE 119

NEW PRODUCTS

DIGITAL ICs

80387-COMPATIBLE MATH CHIP COMPUTES UP TO TEN TIMES FASTER

A combination of more efficient algorithms and architectures lets Cyrix's CX-83D87 Fast-Math chip perform floating-point operations from five to ten times faster than Intel's 80387 numerics coprocessor. On top of that, the new chip consumes only about half the power of the 80387 when active and just 1/20th on standby. Not only is the chip faster, but it drops into the 80387 socket and uses the same software. Systems are easily upgraded.

Because it operates at system clock frequencies of 20, 25, or 33 MHz, the 83D87 can keep pace with the integer operations of the 80386. But because the 80386 coprocessor interface assumes a slower numerics chip, the Cyrix chip includes a memory-mapped operating mode. In that mode, the 83D87 can rip through floating-point operations at twice the speed of even Weitek Corp.'s numerics accelerator for the 80386. Furthermore, in the memory-mapped mode, instruction setup, including operand transfers, can usually be performed by the 80386 in parallel with the previous instruction executing in the 83D87.

To distinguish the chip's performance, the company specifies two instruction-execution times for each command. One defines the number of clock cycles for the instruction, while the other includes the time required by the 83D87 and 80386 combination and all the 80386 setup overhead. By using this information and crafting a smart interface, systems could deliver sustained execution rates equal to the basic number of clock cycles for each command.

Housed in a 68-lead pin-grid array package, the CX-83D87 costs \$471 for the 20-MHz version, \$585 for the 25-MHz unit, and \$773 for the 33-MHz chip. All prices are for quantities of 100. Samples are available from stock.

Cyrix Corp., 1761 International Pkwy., Suite 135, Richardson, TX 75081; (214) 234-8388. **CIRCLE 338**

DAVE BURSKEY

SINGLE CHIP PACKS ALL MOTHERBOARD LOGIC FOR BASIC AT-CLASS COMPUTERS

Only 14 components plus memory is now all that is needed to build a basic desktop PC/AT-class system (minus display and disk controller). The 82C235 single-chip AT-system controller from Chips and Technologies reduces the cost and size of both embedded AT-class systems and price-sensitive PC/AT clones. The controller operates with 8-, 10-, and 12.5-MHz clock rates and zero wait states for the main memory, or at 16 MHz with one wait state.

Included on the chip are equivalents to dual 8237 DMA controllers, two 8259 interrupt controllers, and an 8254 programmable interval timer. Also included are an 8255 programmable peripheral interface and a 68818 real-time clock.

In addition, an 80287 math-coprocessor interface is built in, as is support for fast CPU reset and fast gate A20, which ease switching the 80286 in and out of protected mode. Dynamic-RAM refresh control is also on the chip. Memory control for up to 16 Mbytes of RAM also comes with the chip.

The circuit also packs 32 extended-memory-standard registers for enhanced LIM 4.0 compatibility. Shadow-RAM operation, as well as 8 or 16-bit BIOS memories, are also supported. To round out a system, designers need only add the 80286, a keyboard controller, the BIOS EPROM, 10 TTL chips, and the desired amount of RAM. Further enhancements can be added—a separate EGA or VGA video controller; floppy- and hard-disk controllers; and the 82C601, which includes serial and parallel ports.

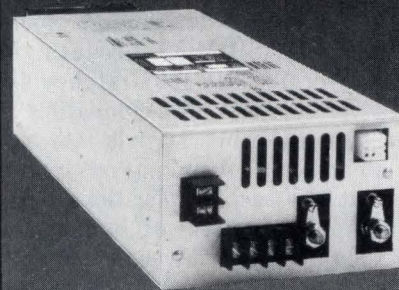
Samples of the 82C235 system controller, which comes in a 160-lead plastic quad-sided flat package, are available this month. In quantities of 1000, the chip costs \$46. Production quantities will be ready in the first quarter of 1990.

Chips and Technologies Inc., 3050 Zanker Rd., San Jose, CA 95134; Chris Maskiell, (408) 434-0600. **CIRCLE 339**

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CIRCLE 120

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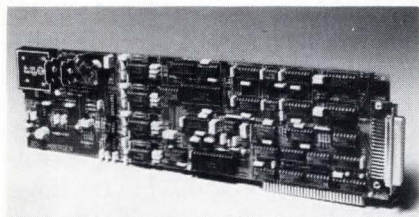
NEW PRODUCTS

ANALOG

LVDT CONDITIONING CARD, MEASUREMENT PODS SPELL HIGH-ACCURACY READINGS

A 16-channel conditioning card and an isolated measurement pod (IMP) from Schlumberger yield extremely high-accuracy linear variable differential transformer (LVDT) measurements.

The conditioning card fits into expansion slots in any IBM PC/AT or compatible and is designed to interface with the internal bus for data management. The card contains a dual 14-bit analog-to-digital convert-



er and accepts either ac or dc inputs. Provision is made for four digital inputs to monitor external switches or relays.

A sinewave oscillator, which is factory-set for either 2.5, 5, or 10 kHz, constantly energizes the 16 transducers in groups of four. The associated conditioning circuitry is in four blocks, each of which has software-controlled gain and offset.

The IMP provides continuous energizing of up to 20 LVDT-type transducers, and is designed for end users who need to take linear measurements with a high degree of accuracy. The front-end units withstand the harshest industrial environments and accommodate all standard transducers without need for external signal conditioning.

The unit is dust- and water-proof and is resistant to shock and vibration to IP55 standards. It will operate in ambient temperatures from zero to +55°C without added protection.

The 16-channel conditioning card goes for \$1500, and the IMP costs \$3200. Both are available from stock in small quantities.

Schlumberger Industries, Sanyo Transducer Division, 5586 Main St., Suite G-1, Williamsville, NY 14221; (716) 634-4452. **CIRCLE 340**

DAVID MALINIAR

80-MHZ PALETTE DACS MIX VGA COLOR WITH LAPTOP-SPECIFIC FEATURES

Like their predecessors, the Bt471, 476, and 478, Brooktree's Bt475 and Bt477 80-MHz triple 8-bit color palette digital-to-analog converters aim at desktop publishing, CAE-CAD-CAM, image processing, and other high-resolution color-graphics applications. However, the 475 and 477, with 256-by-18 and 256-by-24 palettes, respectively, pack extra features that lend them to laptop computers that can drive VGA monitors. For example, a power-down mode drops the typical 180 mA of current drawn from the 5-V supply rail to 10 mA, and to just 1 mA if the clock is inhibited. The converters are also compatible with PS/2 systems.

To further ease designers' task and save board space, a reference has been added that permits setting, with one external resistor, of full-scale output currents of up to 20 mA from each of the three (RGB) on-chip converters. For the first time, both devices also offer on-chip comparators that verify and indicate proper connection to the CRT. In addition, an anti-sparkle circuit eliminates the scattered white dots that sometimes occur when writing to a palette d-a converter during active video operation.

To reduce noticeable sparkle, internal logic maintains the previous output color on the RGB analog outputs while data is transferred between the lookup table RAMs and the RGB registers. The new features enhance the converters' flexibility and price-performance ratio while maintaining pin compatibility with earlier siblings.

In quantities of 100, 35-MHz Bt475 converters in 40-pin PLCCs cost \$8. The Bt477 goes for \$11. Small quantities are available from stock. The higher speed grades (50, 66 and 80 MHz) will be available early in 1990.

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92121; Dale Roark, (619) 452-7850.

CIRCLE 341

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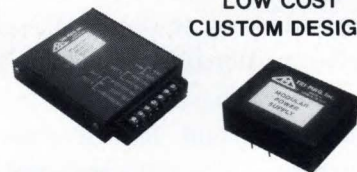
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CIRCLE 121

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FAX 209-651-0188

NEW PRODUCTS

ANALOG

VOLTAGE-TO-FREQUENCY-CONVERTER IC RUNS OFF SINGLE 4.5-TO-36-V SUPPLY

Until now, available precision voltage-to-frequency (VFC) ICs required split power supplies. However, Burr-Brown's VFC121 changes that condition. Not only does it work from a supply rail anywhere between 4.5 and 36 V, but its specifications are given operating from a +5-V supply. Thus, if it is run off a 5-V logic supply, the expected performance is available.

At a full-scale frequency of 100 kHz, nonlinearity runs a maximum of 0.03% for the premium-grade VFC121B and 0.05% for the VFC121A. If the external-component values are changed to provide a full-scale frequency of 1 MHz, nonlinearity for the VFC121B is still a maximum of just 0.1% and is 0.1% typical for the VFC121A. Gain error

at 100 kHz, full scale, is a maximum of 10%, and gain drift is no more than 40 ppm/°C. Initial offset voltage for the 121B is a maximum of 400 μ V for the 121B and 800 μ V for the 121A.

The input-signal range for the converter's 10-M Ω input impedance is from zero to 2.5 V less than the supply voltage. An on-chip 2.9-V ($\pm 0.3\%$) reference can provide up to 10 mA for external circuits. The output, like that of most voltage-to-frequency converters, consists of an open-collector npn transistor rated at 10 mA and 36 V. Saturation voltage at 10 mA is a maximum of 0.4 V.

The VFC121 comes in a 14-pin plastic DIP and is rated for industrial temperatures. In quantities of 100, the VFC121A costs \$7.35 while the VFC121B goes for \$9.95.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; Mark Gordon, (800) 548-6132.

CIRCLE 342

FRANK GOODENOUGH

DUAL SPST IC SWITCH FOR STUDIO AUDIO MAKES NO CLICKS TO MAR SOUND

Typical CMOS analog switches do their job at high speeds. All well and good, except in high-end consumer and recording- or broadcast-studio applications—where speed kills. It inserts clicks in the high-quality audio. To replace less reliable relays with smaller ICs, PMI has come up with a slow pair of dual single-pole, single-throw audio switches. Moreover, they are truly bilateral. The SSM-2402 typically turns on in 10 ms and off in 4 ms. Its sibling, the SSM2412, turns on in 3.4 ms and off in 1.5 ms.

These T-type analog switches use a JFET-bipolar process that builds thin-film resistors. A ramp generated on the chip is applied to the three FETs, which forms the T. The two FETs forming the bar of the T are driven by op amps. Break-before-make switching is guaranteed, with a typical delay time (break-before-make) of 6 ms for the 2402 and 2 ms for the 2412.

These switches can handle current, too. On-resistance is just 85 Ω maximum while passing currents between minus and plus 10 mA with ± 14 V on the I/O pins. The on-resistance of the chip's two switches match within 5% minimum. Off-isolation typically runs better than 120 dB at 20 kHz and approaches 180 dB at 20 Hz—while handling an analog voltage of 10 V rms. Total harmonic distortion over a similar frequency range for 0-to-10-V-rms signals is a maximum of 0.01%. The low distortion permits switching the signals in low-impedance loads without buffer amplifiers. The chip uses a maximum of 7.5 mA from ± 18 -V rails.

The dual switches come in 14-pin DIPs and 16-pin small-outline packages. In quantities of 100, the SSM-2402 and SSM-2412 go for \$3.53 each in either package. Small quantities are available from stock.

Precision Monolithics Inc., 1500 Space Park Dr., P.O. Box 58020, Santa Clara, CA 95052-8020; Dan Parks, (408) 562-7513.

CIRCLE 343

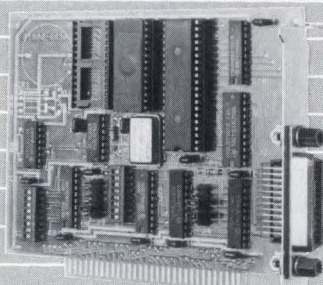
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Technical assistance 617-273-1818



Capital Equipment Corp.
Burlington, MA. 01803

CIRCLE 122

NEW PRODUCTS

ANALOG

HIGH-SPEED, WIDEBAND OP AMP SPORTS PRECISION SPECIFICATIONS

Designed to provide a mix of superior ac and dc specifications, the HA-2548 op amp from Harris combines a minimum open-loop gain of 120 dB while putting ± 10 V across 1000 Ω . Not only that, the maximum offset voltage over temperature is 1200 μ V and typical full-power bandwidth approaches 2 MHz. That's based on a typical slew rate of 120 V/ μ s, but minimum slew rate over temperature is still 70 V/ μ s, which translates to a full-power bandwidth of over 1 MHz.

Although the op amp is optimized for a minimum stable gain of 5, it still maintains a typical open-loop gain of 108 dB while putting ± 3 V across 100 Ω . An output current of 30 mA is available for charging capacitive loads. Small-signal gain-bandwidth (GBW) product, at an inverting gain of 100 and from 100 kHz to 10 MHz, is a minimum of 110 MHz over temperature. Such a detailed GBW specification is a pleasant surprise. In most cases, it is given for a single frequency and at low gain.

Not only does the chip offer a wide bandwidth, but it settles fast, too, thanks to its single gain stage. Settling time to 0.01%, for a 10-V output step at a closed-loop gain of 5, is a mere 260 ns. When handling small, fast pulses, 100-mV rise and fall times are 20 ns maximum.

Broadband input-voltage noise from 0.1 to 10 Hz is typically 0.2 μ V rms and 0.8 μ V to 1 MHz. At 100 nA maximum over temperature, bias current is not high considering the low impedances required to handle the speedy signals the HA-2548 will see.

The HA-2548 comes in commercial, extended-industrial, and military temperature grades; and in ceramic DIPs and TO-99 cans. Unit prices start at \$10.46 each in lots of 100. Small quantities are available from stock.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; Gloria Simpson, (407) 729-3739. **CIRCLE 344**
FRANK GOODENOUGH

FASTEST FET IC OP AMP SETTLES A 10-V OUTPUT STEP TO 0.1% IN 95 NS

Aimed at building fast, accurate sampling amplifiers and integrators, Analog Devices' AD843 is the widest-bandwidth and fastest FET-input op amp. In fact, with a typical settling time of 130 ns to 0.01% for a 10-V step, it beats all the \$10-to-\$75 hybrids it can replace. Settling to 0.1% takes 95 ns.

The 843 is the 10th and last of the first generation of op amps to come off the company's complementary process, which is responsible for its speed (ELECTRONIC DESIGN, March 3, 1988, p. 29). Other applications include fast peak detectors, active filters, and current-to-voltage converters. For example, the op amp can accurately handle high-speed linear (or digital) signals from fast photodiodes. Maximum "warmed-up" bias

current is 2.5 nA at 25°C, which rises over temperature to a maximum of 60 nA at 70°, 160 at 85°, and 2600 nA at 125°C. Devices rated at all three temperature are available.

Other dynamic specifications include a minimum slew rate of 160 V/ μ s. That translates to a minimum full-power (20 V p-p) bandwidth of 2.5 MHz while driving 500 Ω . Minimum open-loop gain, over temperature, is 80 dB while putting ± 10 V across 500 Ω . Unity-gain bandwidth for a 90-mV p-p output signal is typically 34 MHz.

In quantities of 100, the commercial-grade AD843JN in a plastic mini-DIP costs \$8.80. The premium AD843KN, with a maximum bias current of 9 nA at 70°C, costs \$13.75. Small quantities are in stock.

Analog Devices Inc., 181 Ballardville St., Wilmington, MA 01887; (508) 658-9400. **CIRCLE 345**

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Technical assistance 617-273-1818



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CIRCLE 123

ELECTRONIC

DESIGN
NOVEMBER 9, 1989

155

SPEEDY BIPOLAR D-A CONVERTERS TACKLE VIDEO DISPLAYS

Taking advantage of the speed gains from its advanced ECL process, Sony has introduced a

trio of high-speed 8-bit video digital-to-analog converters. The fastest of the three, the CXA1236Q, contains one converter but operates at 500 MHz, which is the highest update rate of any monolithic silicon d-a converter. The other two chips, the

CXA1156Q and CXA1146Q, pack three converters each and operate at update rates of 300 and 160 MHz, respectively.

To load data fast enough to keep the 500-MHz converter running at top speed, dual byte-wide data-bus inputs to the chip allow 2 bytes to be loaded into the CXA1236Q's internal memory registers. An internal multiplexer switches between the registers. Also on the chip are Synchronization, Blanking, Reference White, and Bright control inputs. The converter can deliver its differential RS-343A-compatible output to either 25- or 37.5- Ω loads. Inputs are both ECL 100K- or 10K-compatible and the chip runs from a -5.5-to-4.2-V supply.

Both triple converters are available in production quantities. The 500-MHz unit will reach production late in the second quarter of 1990. Prices in quantities of 100 start at \$45 for the 160-MHz unit and increase to \$55 for the 300-MHz chip. Prices for the 500-MHz single d-a converter have not been set.

Sony Corp. of America, 10833 Valley View St., Cypress, CA 90630; (714) 229-4197.

CIRCLE 317

DAVE BURSKY

Low-Cost Signal Conditioning



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90-MHZ OP AMP SLEWS 250 V/ μ S

With the EL2041 operational amplifier, designers can find a combination of wide bandwidth, high slew rate, high open-loop gain, and unity-gain stability in a single device. The monolithic 90-MHz device can be used for high-speed analog-signal processing, as well as digital-to-analog-conversion applications. It offers a slew rate of 250 V/ μ s and settles to within 0.05% in 90 ns. The EL2041 draws only 13 mA of supply current and drives ± 50 mA to the load. When used as a video amplifier, the device amplifies and transmits NTSC and PAL signals with low distortion. It is available in 14-pin ceramic DIPs, 8-pin plastic DIPs, and 12-pin TO-8 packages. Pricing starts at \$5 in lots of 100.

Elantec Inc., 1996 Tarob Ct., Milpitas, CA 95035; (408) 945-1323.

CIRCLE 318

CIRCLE 124

NEW! Backlighting Options

The Blues always help you see things more clearly.

If you've been singing for higher contrast Liquid Crystal Displays, Seiko Instruments has some happy news for you. Thanks to the unique blue characters on their LCD modules, seeing what's on the screen is easier than ever.

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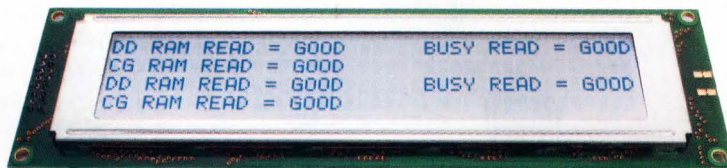
you were using Seiko's parallel interface, TN type modules. Making a visible improvement in your products easy. Quick. And free of retooling costs.

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Seiko Instruments

PHASE-DETECTOR IC ELIMINATES DEAD ZONE

Unlike similar ICs, the AD9901 phase-frequency detector exhibits no dead zone in the middle of its phase detection range, thus eliminat-

ing excessive phase noise. The device, which is capable of comparing signals up to 200 MHz, can be used in a wide range of phase-locked loop applications. It has a linear phase-detection range of 360°, 320°, and 270° at 40 kHz, 30 MHz, and 70 MHz, respec-

tively.

The AD9901's output current is from 1 to 10 mA with a programmable voltage swing of up to 1.8 V pk-pk. The AD9901 operates with TTL, CMOS, or ECL logic levels over operating temperature ranges of 0° to 70°C and -55° to +125°C. Packaging options include 14-pin ceramic DIPs and 20-terminal LCCs. Prices start at \$8 in lots of 100 units. Delivery of all grades is from stock.

Analog Devices Inc., 7910 Triad Center Dr., Greensboro, NC 27409; (919) 668-9511. **CIRCLE 346**

Programmable Anti-Alias Filters for Critical A/D Prefiltering

**848P8E Series
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lowpass filters
providing
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roll-off for
A/D prefiltering.**

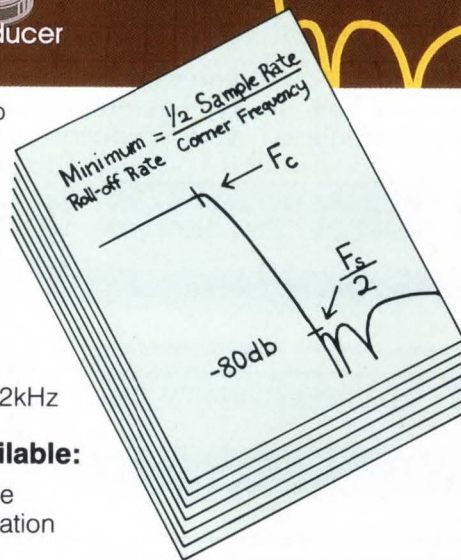
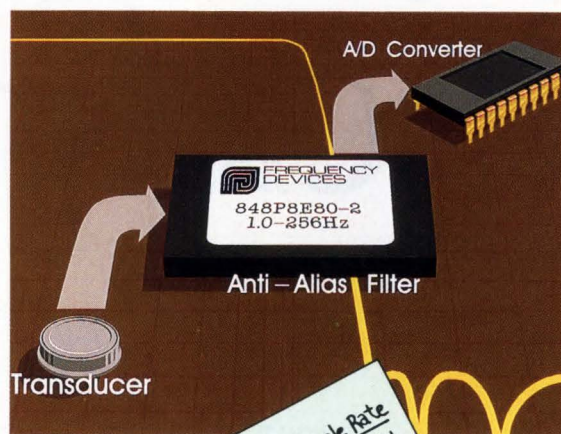
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RTD CONDITIONER IS FULLY ISOLATED



Unlike RTD (resistance-temperature detector) interfaces that require separate isolated power for each channel, the 1B41 RTD conditioner generates its own floating current excitation for the RTD sensor, providing true channel-to-channel isolation from a common supply.

The compact 1.00-by-2.1-by-0.35-in. device includes amplification with resistor-programmed gain and zero suppression, lead-resistance compensation, and filtering. It supports RTDs with resistance ranges from 20 Ω to 5 kΩ. Isolation is specified at 1500 V rms with transient protection meeting the IEEE-STD 472 (SWC) specification. Its ±10-V output is directly connected as a high-level input to multichannel temperature-measurement systems, data acquisition systems, and precision temperature instrumentation. The device requires a ±13.5- to ±18-V dual supply delivering 12 mA of current. Prices start at \$58 in quantities of 100. Delivery is from stock.

Analog Devices Inc., 1 Technology Way, P.O. Box 9106, Norwood, MA 02062; (617) 461-3055. **CIRCLE 347**

CIRCLE 125

Our AUTO-SLIDES stand out in a crowd.

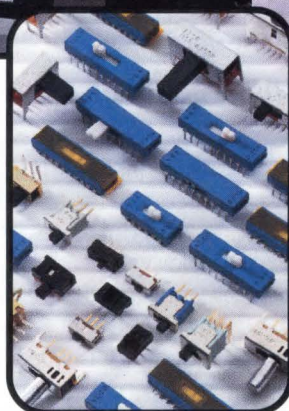
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Introducing the new SCHLEGEL®-C² shielding gasket.

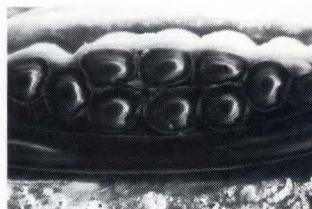
Galvanically compatible with virtually any metal or metallic coating, under almost any operating condition.

Specifying an EMI gasket is now simple. Because the patented SCHLEGEL-C² shielding gasket spans the spectrum of galvanic compatibility, from noble to active metals. No worry about corrosion, even under severe operating conditions. No loss of shielding efficiency.

The reason is an ultra-smooth, non-metallic coating over conductively clad urethane foam. The soft, spongy gasket fills big gaps, while the revolutionary coating conforms to even the smallest irregularities in metal surfaces. The result is a highly efficient shielding gasket and a superb environmental seal. For the design life of your equipment.

SCHLEGEL-C² gasketing is available in more than 20 profiles and in a variety of attachment methods. For a free sample or applications assistance, call or write now.

Ultra-smooth coating over silver-metallized nylon ripstop is bonded to resilient urethane foam. Seals mating surfaces and blocks electrolytic action.



Sandwich construction at 700x magnification shows urethane foam at bottom of photo, clad with conductive silver-metallized ripstop (circular fiber ends). The entire assembly is encapsulated in a conductive, galvanically compatible coating.



At 250x magnification and after 100,000 wear cycles, the equivalent of being shipped three times cross-country, the outer coating of the gasket shows only minimal abrasion. Shielding efficiency is unaffected.



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CIRCLE 143

NEW PRODUCTS

INSTRUMENTS

INTERFACE BOARDS CONTROL IEEE-488 INSTRUMENTS FROM APPLE COMPUTERS

Two plug-in interface boards supply fast IEEE-488 (GPIB) instrument control for the Apple Macintosh family of computers. The boards come with control software suitable for both novice and experienced instrument programmers.

The MacADIOS 488s connects to the SCSI port of the Macintosh Plus, SE, or II. The board permits data transfers of up to 150 kbytes/s on the Mac Plus, 600 kbytes/s on the Macintosh SE, and 800 kbytes/s on the Macintosh II. Because the MacADIOS 488n is Nubus-compatible, it can fill any of the Nubus slots in the Macintosh II.

The interfaces come with the MacDA488 desk accessory, which is accessible from any Macintosh applications software. The software lets users create command sequences by referring to devices mnemonically. Device-specific characteristics such as addresses, terminators, and response filtering are invoked automatically.

More experienced programmers can use the MacDriver488 software, a comprehensive set of over 30 high-level Hewlett-Packard-style bus commands for instrument control. All popular programming languages can access MacDriver488.

MacADIOS 488s costs \$795, and MacADIOS 488n goes for \$595. Both boards are available in 2 weeks after receipt of order.

GW Instruments Inc., 35 Medford St., Somerville, MA; (617) 625-4096.

CIRCLE 319

JOHN NOVELLINO

EMULATOR EASES TMS370 DESIGNS

In addition to lowering the price of existing TMS370 development support tools by 25%, Texas Instruments has introduced a low-cost in-circuit emulator for its TMS370 family of configurable 8-bit microcontrollers. The TMS370 XDS/11 supports real-time in-circuit emulation of the 15 standard configura-

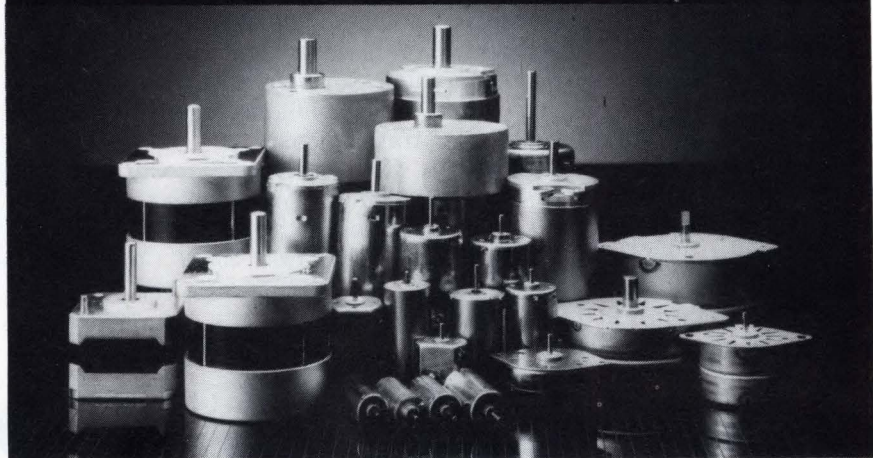
tions and 16 modules of the TMS370 family. The accompanying debugging software provides interactive control of the emulator in the XDS/11 from an IBM PC or compatible computer. Two models of the system are available: one with a 68-pin tar-

get connector and the other with a 28-pin target connector. Either version costs \$2850.

Texas Instruments Inc., Semiconductor Group, SC-935, P.O. Box 809066, Dallas, TX 75380; (800) 232-3200.

CIRCLE 320

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- Low in cost, high in performance.
- Step angle 0.9, 1.8, 7.5 and 15 degrees
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BRUSHLESS DC BOX FANS

- Low cost • High air flow
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CIRCLE 59

NEW PRODUCTS

INSTRUMENTS

BUS ANALYZER SIMPLIFIES TROUBLESHOOTING OF IEEE-488 TEST SYSTEMS

Troubleshooting IEEE-488-based test systems is easier with the Analyzer488 from Iotech. The instrument operates in three modes: as a bus monitor-analyzer, as a bus controller, and as an instrument simulator.

With its own keypad and display, the Analyzer488 can work as a stand-alone benchtop unit. An RS-232 port also lets users control the analyzer from any computer or terminal with a serial port. A companion software package for IBM PC and PS/2 computers and compatibles supplies pull-down menus and multiple windows for easy interaction.

The Analyzer488 displays bus operations in several formats, including a message format that translates bus commands into understandable

mnemonic messages. A 32-kbyte nonvolatile memory records bus transactions at 1 Mbyte/s. Complex triggering sequences and pre- and post-trigger options let users capture only the data they need. The analyzer can also measure the average transaction speed to verify device or system performance. Comprehensive search and compare features quickly maneuver through large blocks of captured data.

As a controller, the Analyzer488 accepts high-level commands to operate instruments on the bus. The unit can then exercise instruments while simultaneously recording bus transactions.

The Analyzer488 costs \$1495, including the Analyst488 software and is available from stock.

Iotech Inc., 25971 Canyon Rd., Cleveland, OH 44146; (216) 439-4091.

CIRCLE 321

JOHN NOVELLINO

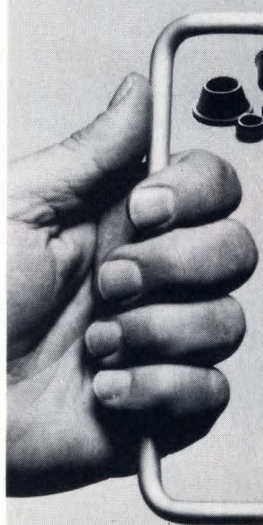
386 EMULATOR WORKS WITH ETHERNET WORKSTATIONS

Designed to be easily integrated with Ethernet-based engineering workstations, the 386 SmartProbe in-circuit emulator lets software engineers download and debug 80386 code in the target system without leaving the software development environment. The instrument offers transparent emulation to 25 MHz. Comprehensive hardware and software breakpoints permit sequential breakpoint construction that helps locate trouble spots in complex code. Integrated source-level debug facilities support C and Ada, so designers can use high-level code statements and symbols during debug. The 386 SmartProbe is priced at \$13,000 and delivery takes 30 days.

Cadre Technologies, Atron Div., 12950 Saratoga Ave., Saratoga, CA 95070; (408) 253-5933.

CIRCLE 322

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CIRCLE 127

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Improve your dynamic range and resolution to match today's high-performance filters, tuners and other components.

Anritsu's MS3606A Network Analyzer now offers you an amazing 120 dB dynamic range for a clear picture around peak and cutoff frequencies. The fully synthesized signal source provides 1 mHz resolution and dramatic increases in phase/delay-time measurement resolution to give you the best sensitivity and precision for advanced video and mobile-communications components.

With the MS3606A, you can measure at a super-high speed of just 400 μ s. The Personal Test Automation (PTA) option gives you faster signal processing and ATE capability to improve productivity. You'll even have the flexibility to transplant program assets from other equipment.

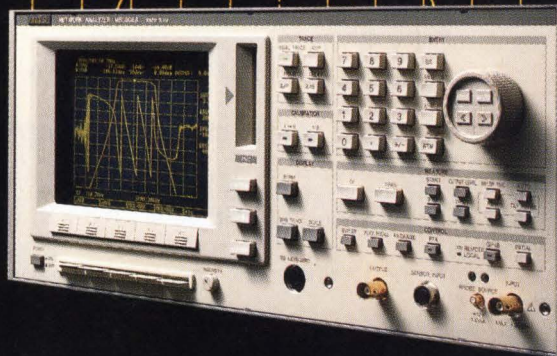
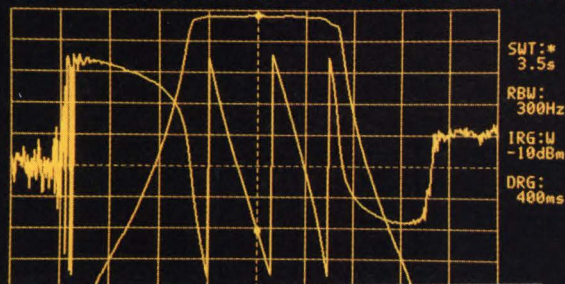
Scalar analysis for complicated tests involving different input and output frequencies is also available, along with conventional vector analysis.

The MS3606A gives you all these features over a wide frequency range of 10 kHz to 1 GHz, for a broad spectrum of applications. And of course, a full selection of peripherals, including equipment for testing analog ICs, is also available.

For R&D or mass production, you'll get the greatest capabilities from Anritsu.

NETWORK ANALYZER MS3606A

MKR(250): 10.7MHz
A: MAG -17.53dB
B: PHA -106.11deg
10dB/50deg
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512-PIN TESTER OFFERS 100-MHz DATA RATE IN SMALLER FOOTPRINT

Designed to take up to 40% less floor space than systems with similar capabilities, the T3382

VLSI logic tester from Advantest America offers a 100-MHz test rate (200 MHz in multiplex mode) on up to 512 I/O pins.

The system comes with either general-purpose pin electronics that deliver a ± 500 -ps accuracy or with

ECL pin electronics that improve accuracy to ± 400 ps. Pin-to-pin skew is less than ± 100 ps. On-the-fly switching of up to 256 timing sets is possible, with a resolution of 62.5 ps. With one timing set, edge resolution is 5 ps.

Behind each pin is a 256-kword-by-3-bit stimulate and expected-vector buffer. In addition to the 1 and 0 logic levels, therefore, users can characterize test vectors by generating stimulate and expected values like positive, negative, high-level, low-level, and don't care. For flexibility, the T3382 includes an algorithmic pattern generator that creates triple address (12X, 12Y, 8Z) vectors with dummy cycles.

The system's test processor runs Advansite, a multiwindow, menu-driven software environment. The package is optimized for test applications, which speeds up throughput. In addition, a general purpose operating system (VMS or UNIX) accommodates tools such as simulators, compilers, and debuggers.

The T3382 VLSI logic tester costs from \$1.5 to \$3 million, depending on configuration.

Advantest America Inc., 300 Knightsbridge Pkwy., Lincolnshire, IL 60069; (312) 634-2552.

CIRCLE 323

JOHN NOVELLINO

AN EFFICIENT C-COMPILER FOR YOUR 8051 PROJECT

- Optimizing compiler for tight, fast code.
- Configurable for all 8051 derivatives.
- For PC/XT/AT, PS/2 and compatibles.
- Produces objectfile containing full symbolic information for use with all popular emulators.
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- Comes complete with a macro assembler, linker, and librarian with SMALL, COMPACT and LARGE library models, with and without floating point.
- Datatypes: (signed / unsigned) char, int, long, float (32 bit IEEE) and bit.
- Can be linked with existing PL/M-51 and ASM-51 object modules.**
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* Except where inconsistent with maximum 8051 efficiency.

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CIRCLE 129

POCKET INSTRUMENTS MEASURE HIGH RESISTANCE

Ideal for testing transformers, motors, generators, and the like, a line of hand-held, microprocessor-controlled testers provides analog and digital readouts of insulation resistance. The Pocket Meggers are compact — just 7-5/8 by 3-7/8 by 1-1/2 in. — and measure insulation resistance from 0 to 1000 M Ω . Additionally, they measure resistance to 1000 k Ω and continuity to 50 Ω , with an audible indicator to 1 k Ω . Two versions are available: the Model 210200 has selectable test voltages of 500 and 1000 V dc; the Model 210201 measures to 500 V dc.

Biddle Instruments, 510 Township Line Rd., Blue Bell, PA 19422; (215) 646-9200.

CIRCLE 324

Simplicity...Versatility

Lambda's LSH and LAS Series are now available with extended input voltage ranges in plastic and metal packages.

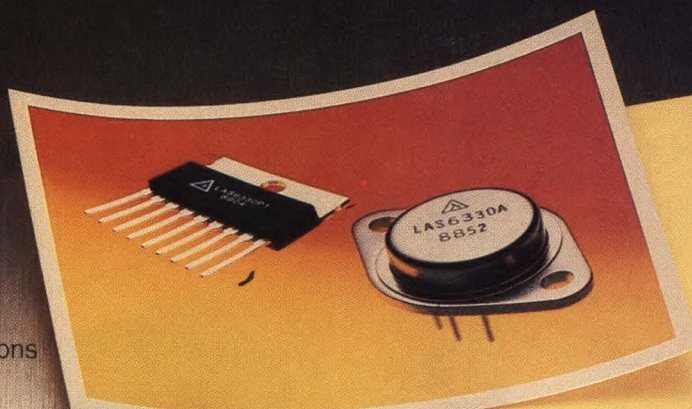
Lambda Semiconductors offers two solutions for switching converter problems...The LAS and LSH DC-to-DC Switching Regulators.

Simple—LSH Series. Lambda's LSH family of complete switching regulators makes DC-to-DC converter design simple, compact and reliable. With input values up to 40 Volts max and output current from 2 to 8 Amps, this microconverter is still the simplest switching regulator to design. Just add 3 external components and your design is complete. You've minimized assembly, troubleshooting, and design time.

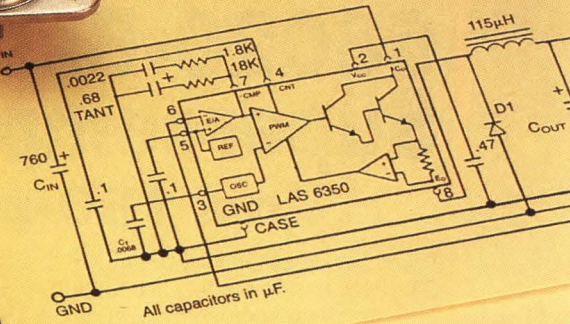
The LSH Series—the smallest regulator on the market today—now comes in your choice of TO-220 style packages or the soon-to-be-available hermetically sealed TO-3 metal packages.

Versatile—LAS Series. The versatile LAS family of switching regulators now features extended input voltage capabilities up to 40 VDC. These flexible regulators are easily adaptable to step-up, step-down, flyback, forward, Cuk, and voltage inverting designs. And they're available in your choice of either TO-3 metal or SIP plastic packages. The complete LAS family offers solutions that maximize on-card regulator design with high efficiency.

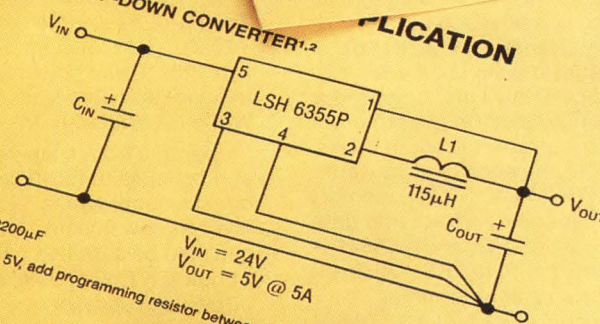
Both the LSH and LAS Series are available with extended input voltages of up to 40V, in your choice of plastic or metal packages, with 2, 3, 5, or 8 Amp output currents. To order call toll free: 1-800-255-9606. In Texas, or for application assistance call 512-289-0403.



5 AMP DC-TO-DC STEP-DOWN CONVERTER



DC-TO-DC STEP-DOWN CONVERTER^{1,2}



¹ C_{IN} = 470µF; C_{OUT} = 2200µF

V_{IN} = 24V
V_{OUT} = 5V @ 5A



121 International Boulevard, Corpus Christi, Texas 78406, FAX: (512) 289-0472

VLSI TESTERS INCLUDE ADVANCED PATTERN- GENERATION CAPABILITY

Two VLSI testers from Semiconductor Test Systems expand the company's digital-

test-system lines with high-performance CPUs and enhanced pattern-generation capabilities, including an algorithmic pattern generator. The STS 8500 can be configured for 256-pin devices, and the STS 6500 can handle up to 120 pins.

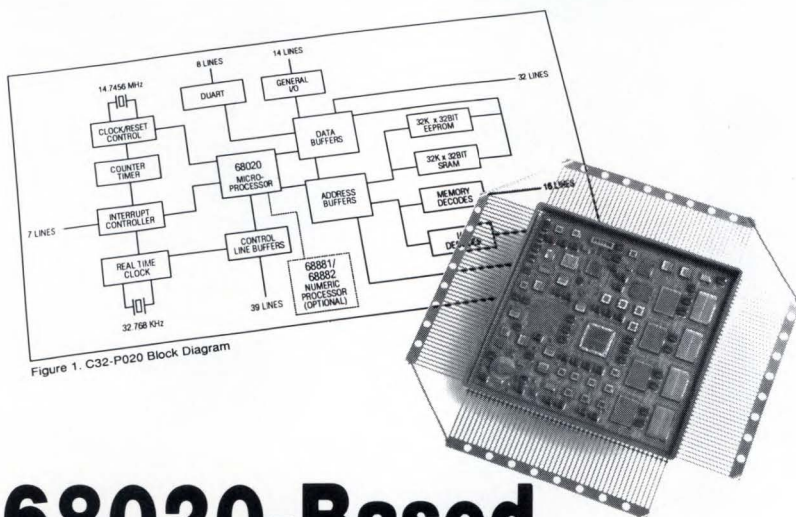


Figure 1. C32-P020 Block Diagram

68020-Based Supercomputer ...in a 180-pin Flatpack

Twice as fast as an AT, our new C32-P020 hybrid module is a fully self-contained microcomputer system crammed into a single, hermetically-sealed, 180-pin 2.4" x 2.4" x 0.190" metal flatpack. But, just because it weighs only 76 grams, it certainly can't be called a lightweight. Based on the Motorola MC68020 microprocessor, it packs in 32K x 32 bits each of zero-wait state EEPROM and SRAM, memory and I/O decodes, address and data buffers, general I/O, and a 68681-type DUART with full RS-232 levels. There is also a counter timer, interrupt controller and a 32.768kHz real-time clock with provisions for external battery back-up. It's a lot of system in a very small space.

Standard operating speed is 15MHz with zero-wait state. Options include 20MHz and zero-wait state, or 25MHz and one wait state. Temperature ranges include: 0°C to +70°C; -40°C to +85°C; and -55°C to +125°C, and screening and burn in to Military standards are options. White is certified to MIL-STD-1772.

It operates from a single 5V supply, and because of its 100% CMOS construction, typical current drain is a very low 600mA. The C32-P020 can also be supplied with an onboard MC68881/68882 floating-point co-processor.

There's more. Much more! We have larger memory options, larger systems capabilities, and very friendly applications assistance. Give us a call for complete details.

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MIL-STD-1772

White Technology, Inc.

A wholly owned subsidiary of Bowmar Instrument Corporation
4246 E. Wood St. • Phoenix, Arizona 85040 • (602) 437-1520
FAX 602-437-9120 • TWX 910-951-4203

CIRCLE 130

Both testers feature STS Scan, which supports all scan test methods with up to 64 million vectors. STS Scan is software reconfigurable with 1, 2, 4, or 8 data pins and works with any tester pin. Also, their multistate vector programming capability allows flexible pin definitions and improves compatibility with CAD vector output and test program translators.

A 1-Mvector memory (standard on the STS 8500 and optional on the STS 6500) and a 64-kbit/channel optional subroutine memory eliminate the need to reload test routines. The systems come with STS' Testertools, an interactive user interface that runs on Sun workstations.

The testers have 1-ns period resolution and 50-ps timing generator resolution. Accuracy is 500 ps for the STS 8500 and 750 ps for the STS 6500. To improve throughput, the STS 6500 includes two parametric measurement units for parallel testing.

The STS 8500 costs from \$500,000 to \$750,000, depending on configuration. The STS 6500 ranges from \$200,000 to \$350,000.

Semiconductor Test Solutions,
VLSI Test Division, 4101 Burton
Dr., Santa Clara, CA 95054; (408)
727-9488.

CIRCLE 325

JOHN NOVELLINO

FOURIER ANALYZER HAS 20-KHZ BANDWIDTH

Using a personal computer as a smart terminal, the 2622 Personal Fourier Analyzer can be used for extensive analysis of signals up to 20 kHz. It offers many of the advanced analysis features of the 2630 Personal Fourier Analyzer in a compact, affordable package. The two-channel instrument provides turnkey spectrum, frequency response (network), and waveform analysis of analog signals, with 28-ms FFTs and frequency spectra measurements with up to 6 MHz resolution anywhere within the unit's 20-kHz input bandwidth. Priced from \$7950, the instrument has a four-week delivery time.

Tektronix Inc., 1350 Dell Ave.,
Suite 104, Campbell, CA 95008;
(800) 234-1256.

CIRCLE 326

HAMILTON/AVNET HAS THE LOCK ON INTEL 80C196KB/87C257 EMBEDDED MICROCONTROLLER KITS



INTEL from HAMILTON/AVNET

Fasten your seat belts for the only highly integrated component kit tailored for motor control applications — Intel's 80C196KB embedded microcontroller and 87C257 latched EPROM kit from Hamilton/Avnet.

Featuring 256 bytes of RAM, a 10-bit A/D converter and high-speed I/O modules, Intel's 80C196KB microcontroller supports fast math instructions and short interrupt latencies. And with no additional "glue" logic required, the 32K x8 (or 256K), 87C257 latched EPROM directly interfaces with the 80C196KB microcontroller, providing a simple and reliable design.

Available in PLCC packages, the compact size of the microcontroller and latched EPROM saves board space which allows for cost-effective, motor control solutions. And Hamilton/Avnet has inventory to support your production requirements.

Hamilton/Avnet also stocks Intel hardware and software development tools, and provides technical literature, design application notes and technical specialists to assist you with your design.

Let Hamilton/Avnet hook you up with components that meet your embedded application requirements. For the location nearest you, call toll free, **1 (800) 442-6458**.

If you're interested in sampling a free 80C196KB/87C257 kit, please fill out the coupon below*. The kit includes the 80C196KB and 87C257 components, as well as technical documentation. Hurry! This offer is for a limited time only.

*Free 80C196KB/87C257 kit limited to first 500 responses; one per customer.

CIRCLE 160

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THREE GREAT SUPER POWERS!

Super Powers Attend Sorensen's Summit Meeting

Reuters

Chicago — World Super Powers gathered at a special Summit to meet with Sorensen, the new leader in single and multiple output switching power supplies. They discussed the strengths of Sorensen's new S Series which offers thousands of models with 1-5 outputs and power levels ranging from 500-2000 W.

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Sorensen Announces Super Power Demo Program

To truly understand the ramifications of this new Super Power, we invite you to try it in your own environment. We're confident you'll agree that the S Series is the best source of power for your application. Call Sorensen at 1-800-525-2024 or your local Sorensen representative and put the powerful S Series to work for you!

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NEW PRODUCTS

COMPUTER BOARDS

VME I/O CARD GRABS ANALOG SIGNALS AT 300 KHZ TO 12-BIT ACCURACY

Designed for DSP applications such as array processing and fast-Fourier transforms, Datel's versatile DVME-601E performs intelligent acquisition and coprocessing of analog voltages on a 6U VME board. Applications include high-speed process control, fast ATE, communication signal analyzers, and spectrum analysis. The board packs a multichannel fast-Fourier-transform front end for a host digital-signal processor or any high-speed analog-to-digital-converter application.

The board combines a 16-channel analog multiplexer that drives a 12-bit, 2- μ s a-d converter with a local 68010 CPU. Control and data interfaces are made by means of a 64-kbyte dual-ported RAM window that

is shared with the VMEbus. Also available are 64-kbytes of local non-VME RAM and EPROM, although there is socket space for 128 kbytes.

Other peripherals include an interrupt controller, a full-duplex RS-232 port, five TTL I/O channels, three general-purpose timer outputs, and a pair of timer-counter inputs. The TTL lines may be individually mapped to the local CPU.

Executive-monitor firmware supplied in EPROM can control of the board from either the RAM or the RS-232 port. It may be run in a no-programming mode with internal a-d-converter subroutines and a local command language, or user-written code may be downloaded from the host. Bidirectional interrupts offer fully arbitrated control, which is ideal for real-time multitasking host operating systems.

In addition to its a-d converter, the board's analog section includes the

multiplexer with 16 single-ended or eight differential inputs and a gain-programmable instrumentation amplifier. Up to 256 channels may be added on VME-compatible boards. Another option is the DVME-645 board, which can simultaneously sample 16 analog inputs. The 601E's a-d converter can be started by external events, by a timer, or by the local CPU. Using a local fast-throughput mode, single-channel signals can be fed to RAM at 300 kHz.

The DVME-601E is a 6U double-height VME board. It needs 3.1 A of +5 V and 10 mA of ± 12 V. An on-board dc-to-dc converter supplies low-noise analog power. The board goes for \$2195 each with volume discounts available. Delivery is from stock to four weeks.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; Larry Copeland, (508) 339-3000, ext. 123. **CIRCLE 348**
FRANK GOODENOUGH

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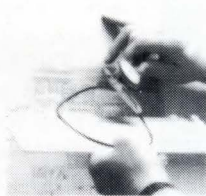
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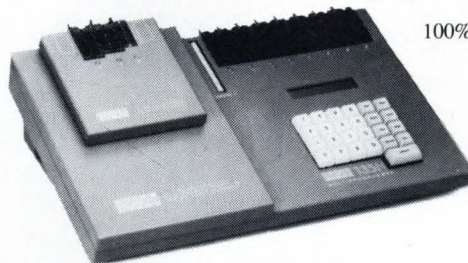
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CIRCLE 132

NEW PRODUCTS

COMPUTER BOARDS

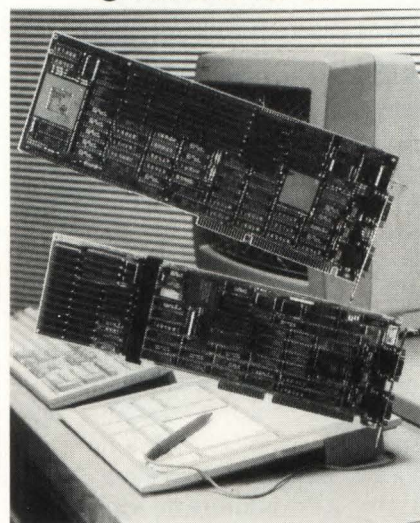
GRAPHICS-CONTROLLER CARDS SHATTER PRICE-PERFORMANCE BARRIERS

Two PC graphics cards have been added to Hewlett-Packard Co.'s high-resolution fam-

ily. These cards give a healthy boost to the price-performance ratio: The TMS34010-based HP Intelligent Graphics Controller 10 is priced at \$995 while the 34020-based card sell for \$2495.

The Model 20 is the first to incorpo-

COMDEX/Fall '89



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rate Texas Instruments' 10-MIPS, 30-MHz TMS34020 graphics processor. It delivers up to 15 times the performance of conventional VGA cards, supplying 1024-by-768- and 1280-by-1024-pixel resolutions. It can display 16 to 256 colors from a palette of 16.7 million.

Using the 50-MHz TMS34010 processor, the Model 10 can display resolutions of 640 by 480, 800 by 600, or 1024 by 768 pixels in 16 or 256 colors from a palette of 256,000. It offers up to five times the performance of conventional VGA cards.

The boards are designed for both ISA- (Industry-Standard Architecture) and EISA-based (Extended Industry-Standard Architecture) PCs and are targeted at users of CAD and graphical user interfaces. Both boards rely on optimized versions of the TIGA-340 (Texas Instruments Graphics Architecture) and DGIS (Direct Graphics Interface Standard) to supply the high-resolution graphics. They offer noninterlaced display refresh, and analog VGA pass-through to ensure compatibility with existing VGA graphics cards for single monitor configurations. In addition, the memory on either board can be upgraded. Model 10 is available immediately, and HP says Model 20 will be available by February of next year.

Hewlett-Packard Co., 3404 East Harmony Rd., Fort Collins, CO 80525; (303) 229-3800.

CIRCLE 349
RICHARD NASS

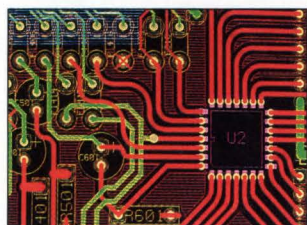
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CIRCLE 133

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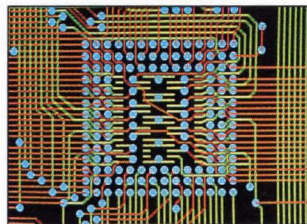
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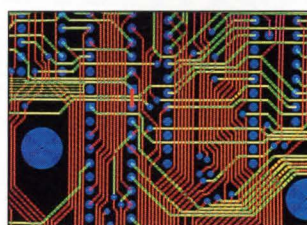


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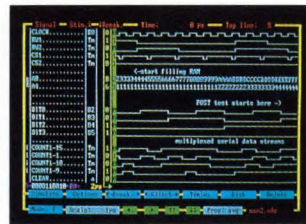
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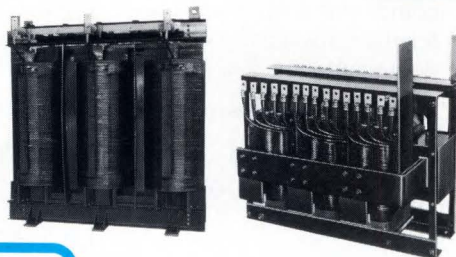
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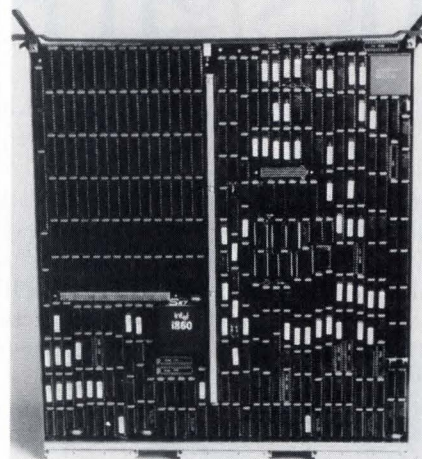
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COMPUTER BOARDS

ACCELERATOR BOARD REACHES 40 MIPS, 80 MFLOPS WITH i860, i960



The Skybolt accelerator board from Sky Computers achieves 40 MIPS and 80 MFLOPS on Sun workstations and other VME-based systems. This burst of speed is the result of combining the Intel i860 and i960 RISC-based microprocessors. By using the two processors and enhanced MetaWare software compilers, near-supercomputer performance can be achieved.

The i860 is a 64-bit processor that fully integrates integer, floating-point, and graphics computations. The i960 is a 66-MIPS general-purpose microprocessor. On the accelerator board, the i960 handles the I/O and boot operations and system diagnostics. This takes care of all house-keeping functions so that the i860 can focus all its computational power on accelerating the task at hand.

The MetaWare C and Fortran compilers are specifically designed to complement the i860 computational capabilities. In addition to the compilers, the Skybolt contains a second-generation vectorizing module that automatically produces vectorized code during compilation rather than before. This is the same approach taken by supercomputers. The accelerator board is available immediately for \$12,450.

Sky Computers Inc., 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920.

CIRCLE 350

RICHARD NASS

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32-BIT	80386, 68020 (25 MHz)

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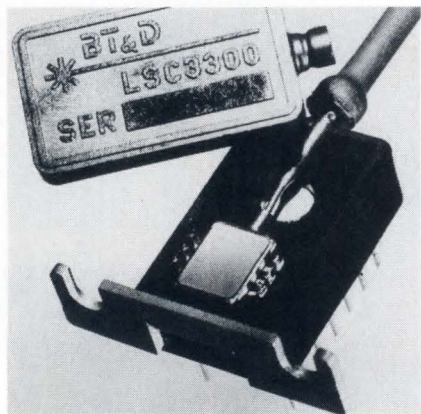
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MINIATURE HERMETIC-PACKAGED LASER COMES IN 14-PIN PLASTIC PACKAGE

The industry's smallest hermetic-packaged laser is BT&D's LSC3300, which is supplied in a 14-pin dual-in-line plastic package. The combination of the company's highly reliable laser and the plastic DIL package results in lower manufacturing costs and substantially higher manufacturing yields.

The laser, which was designed for low-power, uncooled operation, can replace more costly lasers. It can also be used for high-power uncooled applications.

All active components within the LSC3300 device are completely sealed within a hermetic submodule. The internal semiconductor lasers are based on InGaAsP buried-heterostructure technology and include a



photodiode for monitoring the laser output.

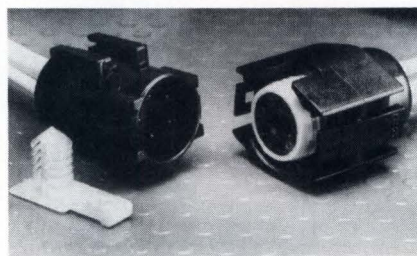
The device is available with a single-mode fiber pigtail and has a MTTF of 450,000 hours at 25°C. It operates in the 1280-to-1330-nm wavelength with typical output of 200 μ W and a modulation capability of up to 1 Gbit/s. A longhorn-type heat sink mounting flange is incorporated in the industry-standard 14-pin package.

In quantities of 100, the LSC3300 costs \$390. Delivery is from stock to 6 weeks.

BT&D Technologies, Delaware Corporate Center II, Suite 200, Two Righter Pkwy., Wilmington, DE 19803; (800) 545-4306. **CIRCLE 327**

DAVID MALINIAK

ENVIRONMENTAL CONNECTOR WITHSTANDS HARSH AUTOMOTIVE APPLICATIONS



Total environmental sealing when exposed to automotive fluids is featured in the Snap Lock connector from ITT Cannon. The connector is well suited for under-the-hood applications involving automotive sensors where safety and high reliability within the system's electrical circuitry are required. The connector, whose operating temperature range is from -40 to +135°C, is an addition to ITT Cannon's broadening line of Snap Lock connectors.

With its snap-lock mating feature, the connector provides audible and tactile feedback to confirm proper mating. A pull-to-test feature also gives confirmation of contact seating. Special mechanical features guard against mismatching. Superior sealing by an O ring at the interface and a multilabyrinth at the rear of the connector means that there is no need for protective greases or sprays. An accessory shoe on the side of the receptacle is included for snap-in automotive accessories. The connector fits through a 1.25-in. hole.

The connector comes in three-, four-, or five-contact densities which can be automatically or hand inserted. The stamped, low-cost contacts are rated for 6 A. A 10-contact version is now under development. The connectors are designed to specification CS-206 and are tested to specification C-73-88.

Pricing for the Snap Lock environmental connector is \$.24 per line. Initial deliveries are in 10 to 12 weeks after receipt of order.

ITT Cannon, Santa Ana Division, 666 E. Dyer Ave., Santa Ana, CA 92705; (714) 754-2150. **CIRCLE 328**

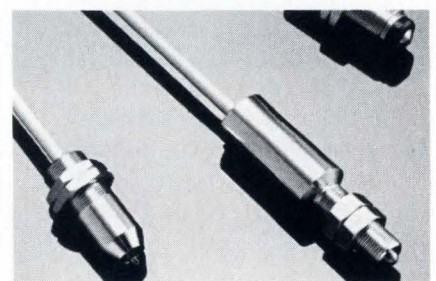
DAVID MALINIAK

ACCELEROMETER CAN BE SURFACE MOUNTED

The Model 3031 accelerometer is one of the first devices of its type to be available in a surface-mounted package. Using a sensor chip that is just 0.135 by 0.135 in, the solid-state piezoresistive device fits in a package with a 0.3-by-0.3-in outline. It is particularly suited for high-volume production where small size, light weight, low cost, and compatibility with other surface-mounted components are required. Full-scale acceleration ranges from ± 2 to ± 500 g. Operation is from a 5-V supply. Performance characteristics and packaging can be easily tailored to meet specific applications. Pricing for the Model 3031 starts at \$77 in sample quantities. Delivery is from stock to four weeks.

IC Sensors Inc., 1701 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1800. **CIRCLE 351**

MECHANICAL SWITCH IS ACCURATE TO 1 μ M



With tolerances of 1 μ m (40 millionths of an inch), My-Com mechanical switches provide extremely precise gauging control and unequivocal on-off status. They are offered in a variety of basic configurations, including a choice of sapphire, ruby, or hardened-steel activation pins. Optional design features include waterproof housings, two-step switches, and tubular or rectangular housings. Devices can be specified with either 15-V dc or 24-V ac ratings with contact or transistor output. LED indicators are available on transistor versions.

Baumer Electric Ltd., 122 Spring St., Southington, CT 06489; (203) 621-2121. **CIRCLE 352**

Guess who's first in CAD/CAM/CAE and fastest growing in workstation sales? Guess again.

The first name you probably thought of is not the first. Intergraph is #1 in CAD/CAM/CAE in North America. Also, we're the world's 4th largest and the fastest growing workstation company.

And it should be no surprise. Intergraph offers the broadest range of integrated solutions — more than 500 Intergraph and third-party applications. Intergraph introduced the first workstation based on a commercial RISC microprocessor — CLIPPER. Today, we're the world's largest supplier of UNIX RISC-based workstations and servers. Over 25,000 units shipped.

With Intergraph, you get open, industry-standard workstations, servers, peripherals — and integrated solutions. Plus the connectivity to tie everything together.

And, at Intergraph we take service and support very seriously. Our people are available over the long-term — where and when you need them. We're committed to maintaining our ranking as #1 in customer loyalty and satisfaction.

So, avoid the guessing game in choosing workstations and applications. Call Intergraph — a Fortune 500 company — first. In the U.S. 800-826-3515, Canada 416-625-2081, Europe 31-2503-66333, Asia 852-5-8661966.

CIRCLE 80

INTERGRAPH

Intergraph Customers Loyal

BY CHARLES FOUNDYLLER

A survey of Intergraph users shows the firm enjoys outstanding loyalty from its customers. Fully 94% of respondents said they would still buy from Intergraph if they had the decision to make over again. One source were very

Source: Daratech, Inc., as printed in Computer-Aided Engineering, October, 1988

What Users Say

Would buy from same vendor again.

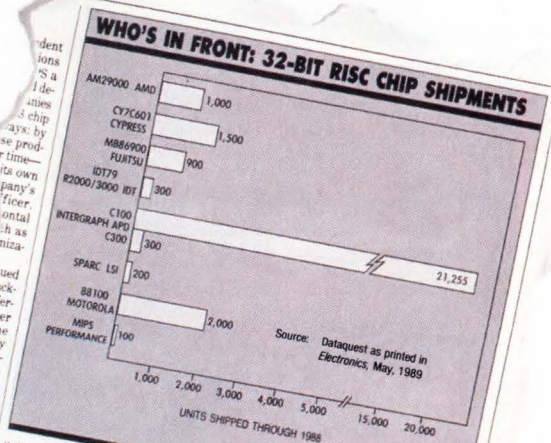
36%

1988 Worldwide Workstation Revenue and Marketshares (Estimates)

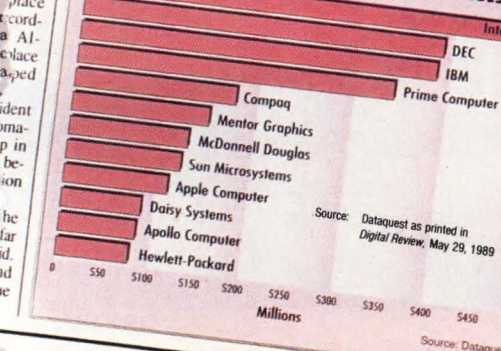
Company	1988 Revenue(M)	Market Share	Point Change	87-88 Growth
Sun Microsystems	\$1,165	28.3%	+4.2	80.6%
Digital	\$765	18.6%	+1.8	70.8%
Hewlett-Packard	\$695	16.9%	+0.7	59.8%
Apollo	\$555	13.5%	-4	18.1%
Intergraph	\$275	6.7%	NR*	83.3%
Silicon Graphics	\$180	4.4%	+0.7	81.8%
IBM	\$105	2.6%	-1.1	10.5%
Others	\$370	9 %	-3.5	10.4%
Total:	\$4,110	100%		53.0%

*Not reported last year.

Source: Dataquest as printed in Computer Graphics Review, March, 1989



LEADING CAD/CAM/CAE VENDORS' 1988 REVENUES



NEW PRODUCTS

COMPUTERS & PERIPHERALS

TWO-, THREE-BUTTON LOW-COST OPTICAL MOUSE DEVICES RAISE RESOLUTION

Two models have been added to the already extensive mouse-product line from Mouse Sys-

tems Corp. The White Mouse is a high-end optomechanical mouse with three input buttons. It offers a base resolution of 350 characters/in.

Using the bundled Ultra-Res software package, users can select a resolution value ranging from 35 to

COMDEX/Fall '89



11,200 characters/in. (cpi). The user also has control over the White Mouse's compatibility using its built-in microprocessor. It is fully Microsoft-compatible and can be used as either a Microsoft, Logitech, or Mouse Systems mouse by throwing a control switch on the bottom the device. The White Mouse sells for \$119.

Designed to reach first-time buyers, the OmniMouse II is a low-end, two-button mouse that costs just \$79.95. As with the White Mouse, it is 100% Microsoft-compatible. It has a base resolution of 250 cpi and is user-selectable from 20 to 6400 cpi.

The minimum requirements for either device are an IBM PC/XT, PC/AT, PS/2, or compatible; DOS version 2.1 or higher (3.3 or higher for the PS/2); and an RS-232-C port.

Mouse Systems Corp., 47505 Seabridge Dr., Fremont, CA 94538; (415) 656-1117.

CIRCLE 329

RICHARD NASS

COMDEX/Fall '89

PC BOASTS 71-MBYTE HARD DRIVE, 4-MBYTE RAM

The 386/16 PC is the latest addition to an existing PC line. Peripherals included with the system include a monochrome monitor and a 71-Mbyte 5-1/4-in. hard drive. The computer can handle all IBM-compatible software with its 4 Mbytes of RAM.

The computer can run at either 8 or 16 MHz. Its features include a 1.2-Mbyte 5-1/4-in. floppy disk drive, two 32-bit expansion slots, four IBM PC AT slots, two XT slots, and a 101-key AT-style keyboard. A high-resolution color monitor is optional. The system sells for \$3460 and is available immediately.

Maxar PCs, 710 Lakeway, Suite 285, Sunnyvale, CA 94086; (408) 733-0810.

CIRCLE 330

High Voltage 20¢/Volt

The PS300 programmable power supply series provides up to 5kV at 25 Watts for laboratory and ATE applications. These supplies offer a wide range of features including programmable current and voltage limits, selectable overload response, and short circuit protection.

Dual LED displays monitor both output current and voltage, while a third display allows error-free front panel entry. A full GPIB interface is available for ATE systems.

The combination of features, price, and performance make the PS300 series the perfect choice for laboratory or systems use.

\$995

PS350	0 to 5kV
PS325	0 to 2.5kV
PS310	0 to 1.25 kV

25 Watts output power
0.001% regulation
0.1% accuracy
Low output ripple
Dual polarity
Voltage and current readouts

GPIB Interface **\$495**



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CIRCLE 135

NKK'S new 400-page Big Cat. makes your job easier. A lot easier.

NKK's new Big Cat. — biggest catalog in the switch jungle — has the power to help you tame the toughest tasks. The Big Cat. quickly tracks down over 873,000 different switches and 38 distinct switch families, including the industry's largest selection of washables.

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NKK Switches, 14415
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Scottsdale, AZ 85260.

CIRCLE 6

NKK
switches

See us at WESCON Booth #146



PSpice

The Standard for Circuit Simulation



Mixed Analog/Digital Simulation

Available on Popular Computers, Including the New DECstation 3100

Whether your installation uses computers from Apollo, Apple, DEC, IBM, or Sun, PSpice can help your circuit designs. By maintaining consistent file formats across different platforms, PSpice insures that circuit designs, both old and new, can be simulated on all your computers.

In addition, we customize our graphics to get the best performance on each platform. Our drivers span the range from direct writing into refresh memory to higher level interfaces such as X-Windows. Since we use consistent file formats, that means that, for instance, a simulation done on a VAX 8800 can have its results viewed graphically on a Macintosh. Or, if you prefer, you can simulate on the Mac and do the viewing on the 8800.

Since its introduction over five years ago, MicroSim's PSpice has more copies sold than all other commercial SPICE programs combined. Here are some of the features which have made PSpice so popular:

- Standard parts libraries of over 2200 analog models: diodes, bipolar transistors, small-signal JFET's, power MOSFET's, opamps, voltage comparators, transformer cores, and opto-couplers.
- GaAs MESFET devices, BSIM MOS model.
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

These PSpice options are also available:

- **Digital Simulation**, which allows you to simulate mixed analog/digital circuits with feedback between the analog and digital sections. A library of 690 TTL devices is included.

- **Analog Behavioral Modeling**, which allows you to specify arbitrary transfer functions for devices, either by formula or look-up table. This can be done in both the time and frequency domains. In time domain the devices may be non-linear as well as linear.
- **Monte Carlo** analysis to calculate the effect of parameter tolerances on circuit performance. This includes statistical, sensitivity, and worst case analyses.
- **The Probe** "software oscilloscope" provides an interactive viewing environment for simulation results (see photo above).
- **The Parts** parameter extraction program, allowing you to extract a device's model parameters from data sheet information.

PSpice is available on these computers:

- The PC family (including the PS/2) running DOS, DOS with extended memory, or OS/2.
- The Macintosh II and SE30.
- The Sun 3, Sun 4, and SPARCstation families.
- The Apollo DN3000 and DN4000 workstations.
- The VAX/VMS family, including the MicroVAX.
- The DECstation family, running Ultrix.

Each copy of PSpice comes with our extensive product support. Our technical staff has over 100 years of experience in CAD/CAE and our software is supported by the engineers who wrote it. With PSpice, expert assistance is only a phone call away.

For our free information packet, including a PSpice demo diskette, call us **toll free** at (800) 826-8603 or, in California, (714) 770-3022. Find out for yourself why PSpice is the standard for circuit simulation.



MicroSim Corporation

20 Fairbanks • Irvine, CA 92718 USA • Telex 265154 SPICE UR

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CIRCLE 125



Miller-Stephenson introduces new CFC-Free SAFEZONE Solvent & Flux Remover

Now by special formulation and in the interest of a better environment, Miller-Stephenson presents **SAFEZONE** CFC-Free Solvent & Flux Remover offering a "new solution" no rinse, quick cleaning action; so expedient for field service, so perfect for prototype and production work. For sample fill out coupon below or call (203) 743-4447. For technical service call **1-800-992-2424** (8-4 Eastern Time). In Canada call 1-800-323-4621 (8-4 Eastern Time).

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CONNECTICUT
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Danbury, Conn. 06810
203 743-4447

CANADA
514 Carlingview Dr.
Rexdale, Ontario M9W 5R3
416 675-3204

CIRCLE 136

NEW PRODUCTS

COMPUTERS & PERIPHERALS

PS/2-COMPATIBLE TRACKBALL PLUGS DIRECTLY INTO MOUSE PORT

The PC-TRAC trackball, packaged in a rugged plastic housing, can be used with IBM PS/2 computers. The pointing device, from MicroSpeed is hardware-compatible with IBM's PS/2 mouse and plugs directly into the PS/2 mouse port. Consequently, it doesn't unnecessarily tie up a serial port or bus slot.

As with similar trackballs, the stationary PC-TRAC takes up much less space than a mouse and does the same job with some added stability. Its ball, which is about the same size as a cue ball, doesn't need to be cleaned nearly as often as a mouse. The low-power, CMOS-design trackball has a footprint less than 4-1/4 in. wide. For input, it contains two buttons and a cursor drag-lock button for pointer control.

The trackball includes an advanced multi-axis-pointer device

driver that is software-compatible with standard mouse drivers and supports user-selectable ballistic gain. This adjustable gain, which continuously monitors the rate at which the pointing device is moving, yields effective pointing resolutions from 50 pulses/in. to more than 2000 pulses/in. Operation can be on either two or three axes.

PC-TRAC sells for \$119 and includes a one-year limited warranty. It is available immediately.

MicroSpeed Inc., 44000 Old Warm Springs Blvd., Fremont, CA 94538; (800) 232-7888.

CIRCLE 331

RICHARD NASS



COMDEX/Fall '89

LOW-COST ELECTROSTATIC PLOTTER IS ALTERNATIVE TO PEN PLOTTER

A high-performance monochrome electrostatic plotter can be a low-cost replacement for pen plotters in mechanical and architectural applications. With a price tag under \$14,000, the CADmate offers higher perfor-

mance at a lower price. CADmate provides near-laser quality, 300-point-per-in. (ppi) drawings in a 36-in. wide format. And its high resolution and definition don't demand the high data-transfer rates required by plotters with 400-ppi resolution.

Paper is plotted at a rate of 0.65 ips, producing E-size (34 by 44 in.) drawings in under 30 s, up to six times faster than pen plotters. Long plots or drawings are limited only by the length of CADmate's media roll. Drawings can also be batched and produced at a later time, a feature useful in high-volume applications. Special features include variable line widths and mirror imaging. Available immediately, the system is priced at \$13,900. Quantity discounts are available. That price includes the plotter, an interface board, a driver, and the software to run the plotter.

Versatec, a Xerox Co., 2710 Walsh Ave., Santa Clara, CA 95051; (800) 538-6477 or (800) 341-6060.

CIRCLE 353

RICHARD NASS

Extraordinary PC systems demand extraordinary chips.

53C700 Host Adapter
The first single chip intelligent SCSI host adapter. Highest performance SCSI core available. Integrated with 32-bit bus master DMA and a SCSI Scripts™ processor.

53C400 SCSI Host Adapter
Offers a higher level of integration and greater versatility than competitive solutions.

53C90 Advanced SCSI Controller
Typically completes sequences in 2% of the time needed by competitive chips. 53C94/95 offer separate 16-bit data path.

77C20 VGA Display Controller
Fully compatible with IBM VGA controller at both register and gate levels. Add 77C171 Palette DAC for a complete VGA display adapter solution. CGMA for CGA, MDA, HGA.

52C40/60 Memory Buffer Controllers
General purpose dual and tri-port buffer controllers for speed matching solutions.

86C01 Micro Channel™ Bus Interface
Single-chip solution is priced competitively with other solutions that require from two to as many as seven chips.

92C28 Ethernet Controller
First 32-bit Ethernet controller. Provides complete support for network management and multiple connection environments.

92C02 Twisted Pair Transceiver
First Ethernet twisted pair transceiver. Implements current IEEE 802.3 10 BASE-T draft standard.

90C98A ARCnet Controller/Transceiver
Highest performance single-chip ARCnet LAN controller/transceiver. Includes buffer chaining and reduced wait states. Backward software compatible to the 90C26.

ASIC PC Building Blocks
Digital and analog libraries with a wide variety of cells, including MPU cores, 8200 peripherals, D to A and A to D converters, sound generators, counter/timers, multipliers, floppy disk controller, digital data separator, ISA Bus interface and integrated bus drivers. Plus KE; NCR's knowledge-based Engineering Environment.



Your latest brain child can't be just another PC or peripheral.

You've got to have the edge in performance.

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At NCR, we understand your problems. And we've got solutions: SCSI chips with the lowest overhead in the business. The first third generation intelligent SCSI host adapter. A single-chip VGA that's fully compatible with IBM and offers greater performance.

Single-chip CMOS solutions for interfacing peripheral chips to NU Bus, EISA, AT and Micro Channel.

The first 32-bit Ethernet controller.

The first Ethernet twisted pair transceiver. Plus the fastest ARCnet controller/transceiver.

And an ASIC capability with PC building blocks to give your design a competitive edge.

No wonder NCR customers enjoy some of the shortest development cycle times in the industry. And they'll attest to NCR's enviable reputation for first-pass success, responsive support, competitive pricing and on-time delivery.

If you're building extraordinary PCs, or plugging products into them, shouldn't you be talking to an extraordinary semiconductor manufacturer? For data sheets and complete information, call the NCR Hotline: 1-800-334-5454.

Creating value

NEW PRODUCTS

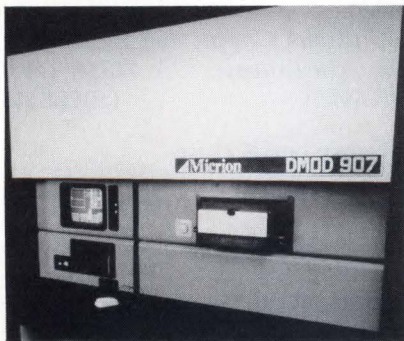
PACKAGING & PRODUCTION

IC MODIFIER CAN MAKE CHANGES TO COMPLEX PARTS IN HOURS, NOT WEEKS

Instead of taking days or even weeks to modify complex IC or wafer prototypes, the DMOD 900 Series from Micrion Corp. can make those same changes in a matter of hours. Moreover, the changes are made without having to wait for new silicon.

The automated system not only disconnects existing wire and generates new contact areas, but also selectively deposits new metal between existing conductors. This task is performed by a finely focused beam of gallium ions as small as 0.2 μm in diameter and a local decomposition of tungsten carbonyl gas. Sub-micron holes or chip cross sections can be milled with an accuracy of $\pm 0.75 \mu\text{m}$. This affords access to buried layers and test points that had been inaccessible. Until now, this technology had been available to mask makers but not circuit designers, test engineers, or wafer-fabrication lines.

Because of its inherent process control and accuracy, the DMOD



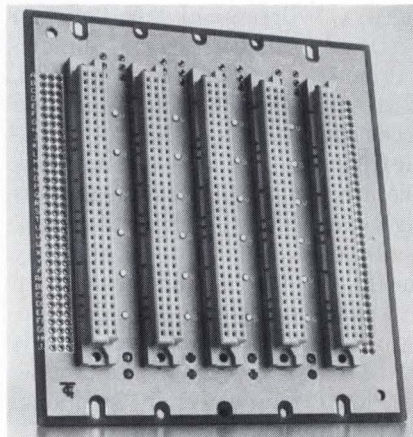
systems can be used on the most advanced ICs including 4-Mbit dynamic RAMs, 32-bit microprocessors, and ASICs.

The DMOD 900 Series consists of three models: the 905, 907, and 909. Prices start at \$700,000, depending on model type, configuration, and degree of automation. Options include an RS-232 interface, a CAD interface, and an Ethernet link.

Micrion Corp., One Corporation Way, Centennial Pk., Peabody, MA 01960; (508) 531-6464. CIRCLE 354

RICHARD NASS

A TRIO OF UNBUSSED BACKPLANES MAKES CUSTOM INTERCONNECTIONS FOR PCs



A completely unbusSED platform for custom interconnections in systems with 0.8-in. board spacing is provided by three backplanes from BICC-VERO. Designed to be used on their own or with standard Eurocard systems such as VME and Multibus II, the J3V backplanes come in modular, five-slot sizes for versatility.

Each model comes fully loaded with DIN connectors that feature a compliant, press-fit design. Three-level, gold-flashed wire-wrap tails on the models J3V1 and J3V2 offer a means of linking signal lines to customer specifications with regard to I/O or power commitments.

The J3V1 and J3V2 models feature two-layer construction with a 2-oz. power and ground plane. Model J3V1 is an on-board backplane with 96 plated-through holes at each end for use in building custom signal terminations. Model J3V2 is similar, but does not include the on-board termination holes. Model J3V3 is simply a connector holder, with no copper power or ground planes. It is supplied with tin-plate, three-level DIN connectors.

The J3V1, J3V2, and J3V3 backplanes cost \$123.79, \$111.45, and \$75.65, respectively, in single quantities. Delivery is from stock to 2 weeks from receipt of order.

BICC-VERO Electronics Inc., 1000 Sherman Ave., Hamden, CT 06514; (800) 242-2863. CIRCLE 355

DAVID MALINIAK

Over 600 standard
PICO Ultra-Miniature
DC-DC Converters
DELIVERY—STOCK TO ONE WEEK



from .3" ht.
1 to 20 Watts

- Input Voltages of 5, 12, 24, 28 and 48V DC Std.
- 129 New Wide Input Range Units (5 to 60V DC)
- Single and Dual Output
- 1 to 30 Watts Output Power
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- New High Voltage Models 100–250 Volt Output
- Over 100 Models with 28 Volt Inputs and Outputs
- 180 Regulated Models
- Ultra-Miniaturized Encapsulated Package (.3" height)
- Ambient Temp. Range -25°C to $+70^{\circ}\text{C}$ with No Heat Sink or Electrical Derating
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New M Series—Single and Dual Outputs. Up to 1.25 Watts. All JAN/TX Military Components.

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CIRCLE 137

FAULT-SIMULATION TOOLS EVALUATE 100,000-GATE DIGITAL ASICs

To date, fault simulation has been available only to those who had the money for expensive hardware simulators, or enough time to run software-only tools. The FasFault family of fault-simulation tools from Intrinsix Corp. combines a hardware-based core with an efficient suite of software to perform analysis at a rate of two million evaluations/s. The first two FasFault versions can simulate 10,000 and 25,000 digital gates, and a 100,000-gate version will be available by the end of the year.

The accelerator-based FasFault products achieve fast, deterministic, serial fault simulation by setting up a virtual tester in custom hardware. Users can perform a unit-delay logic simulation at the same speed. For instance, Intrinsix benchmarked a 10,000-gate logic simulation with 9500 vectors at 7 s.

FasFault consists of C-based software programs and one PC/AT add-in board for 80286- and 80386-based computers. The system can also be configured as a resource for all other Unix and non-PC/AT machines connected on a network.

A layer of Intrinsix primitives below each simulator primitive ensures compatibility with existing software simulators. As a result of this technique, instant support is provided for all libraries for those software simulators. Users begin fault simulation by compiling the design database through an additional hierarchical layer to the Intrinsix primitives.

Base prices for the FasFault-8 (8k primitives and 10,000 gates) and FasFault-16 (16k primitives and 25,000 gates) are \$4500 and \$7500, respectively. The interface for the Viewlogic Workview system costs \$1500. Netware software for accessing the FasFault system from a non-AT CAE workstation is \$3000. All products are available now.

Intrinsix Corp., 33 Lyman St., Westboro, MA 01581; (508) 836-4100.

CIRCLE 332

LISA GUNN

ENVIRONMENT LINKS DESIGN AND TEST

The TESYS integration system provides a bidirectional link between CAD and CAE systems, logic simulators, and automatic test equipment. With the system, users convert and cross netlists among the most popular CAD and CAE systems, interconnecting tools for logical design, design validation, and physical design. Simulation can be executed either by the TESYS logic simulator or by an external simulator. In addition to design verification, the system extends post-processing capabilities for device-level diagnostics in functional performance-level testing.

Firstec SA, 35, route du Velodrome, CH-1228 Plan-les-Ouates/Geneve, Switzerland; (41) 022/794 39 35.

CIRCLE 356

SOFTWARE GENERATES TEST VECTORS



An automatic test-vector generation (ATVG) program for programmable logic devices provides fault coverage, design for testability, and ATVG capabilities for non-preloaded and preloaded registered and combinatorial devices. Called PLDtest Plus, the software produces the highest fault coverage with a minimum number of test vectors to greatly reduce testing time. The vectors can be used with in-circuit testers and component testers or programmers. Additionally, PLDtest Plus allows users to determine if the circuit can be initialized.

The program runs under DOS 3.1 or higher on the IBM PS/2, PC, XT, AT, and compatibles, as well as OS 3.4 or higher on the Sun-3 worksta-

tion platform. DOS versions cost \$5995, while the Sun program is priced at \$9600. Delivery takes four to six weeks.

Data I/O Corp., 10525 Willows Rd. N.E., Redmond, WA 98073; (206) 881-6444.

CIRCLE 357

PCB PROGRAM INCLUDES SURFACE MOUNTING

Full support of surface-mounted technology has been added to the AutoPCB printed circuit-board design system. New functions of Release 5.3 include component placement on both sides of the board, the ability to interactively switch any surface-mounted component to the opposite side of the board, an SMT autorouter that routes to surface-only pads for components on both sides of the board, support for blind and buried vias, and a parts library of surface-mounted devices. Parts or any other board features can be defined in metric dimensions and used with parts and board features having English dimensions. In order to ensure design correctness after interactive editing, a fast mechanical and electrical design rule checker has been added.

Cadisys Corp., 624 E. Evelyn Ave., Sunnyvale, CA 94086; (408) 732-1832.

CIRCLE 358

INTERFACE LINKS PCB DESIGN SYSTEMS

P-CAD has linked its Master Designer II and Associate Designer PCB Design packages with Cadam's Professional Cadam Prance and Interactive Prance Cadam PCB design systems. In applications involving unusually complex designs or designs with extensive high-speed ECL technology, P-CAD users now have the option to invoke the power of the high-end Prance software. The interface between P-CAD and Cadam Prance is priced and configured according to each specific user's applications.

Personal CAD Systems Inc., 1290 Parkmoor Ave., San Jose, CA 95126; (800) 523-5207 or (408) 971-1300.

CIRCLE 359

Free At Last.



Introducing DrawingMaster™ From CalComp

At last a plotter that sets you free to do what you do best: plan, design and manage.

The superior reliability of DrawingMaster's advanced direct imaging technology gives you the power to output clean, sharp A to D size plots within minutes. And with a lot less effort.

How? DrawingMaster uses direct thermal imaging. So there are no chemicals, toners, ribbons or pens to slow you down. Which makes it convenient and easy to use.

What's more, DrawingMaster's automatic paper cutter and optional media take-up reel free you up to do more important things. Which translates into productivity *beyond* your imagination.

As for output versatility, DrawingMaster's three printing modes give you the choice of quality or speed with Qualplot, Quickplot and Normal settings, including two-color capability on the same plot.

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at one time. Plus, it has a small footprint for the most efficient work spaces. So whether you plot at your own desk or in a group setting, DrawingMaster gives you the freedom to work where you want.

But best of all, DrawingMaster is packed with all of these features at a price that's way below monochrome electrostatics. Plus, it comes with CalComp's 90-day warranty, 30 years of experience, and 800 hotline for technical service and support.

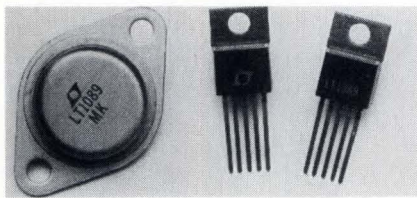
For performance and reliability, DrawingMaster lets you get down to the business at hand. And honestly, wouldn't you rather spend your time doing what you do best?

Set your imagination free by calling 800-CALCOMP, toll free, and ask for your free information packet. Or write to us at CalComp, P.O. Box 3250, Anaheim, CA 92803. In Canada, call (416) 635-9010.

**We draw on
your imagination.™**



BIPOLAR HIGH-SIDE SWITCHES CHALLENGE DMOS PERFORMANCE



Built on a bipolar process that handles 60 V, a pair of high-side switches from Linear Technology Corp. equal the performance of switches built on multi-mask BCD (bipolar/CMOS/DMOS) processes. High-side switches are inserted between the positive power source and the load. Rated respectively at 1.5 and 7.5 A at 20 V, the LT1188 and LT1089 come in 4-pin (case ground) TO-3 packages and 5-pin (tab and center-pin ground) TO-220 packages. They switch up to 20 V with an internal drop of less than 1.5 V at the rated current.

Both devices are designed to enable 5-V logic signals to drive ground- or negative-voltage-referenced resistive and inductive loads including lamps, solenoids, and motors. Because the LT1188 is aimed at automotive applications, it provides a status-output logic flag. It can handle a 60-V, 200-ms transient on its supply rail (load dump) and is rated for operation at junction temperatures from -55 to $+175^{\circ}\text{C}$. The LT1089, sans status flag and load-dump specification, operates at junction temperatures between -55 and $+150^{\circ}\text{C}$.

Self protection in both devices includes current limiting as a function of switched voltage and over-temperature shutdown. For example, if the LT1089 is switching 5 V, current is limited to 12 A.

In quantities of 100, the commercial-temperature-range LT1089 costs \$5.30 in the TO-220 package. Plastic-packaged devices go for \$4.20.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas CA 95035-7487; Bob Scott, (408) 432-1900.

CIRCLE 333

FRANK GOODENOUGH

HYBRID BUFFERS DRIVE HIGH CURRENT TO 400 MHz

Five high-speed voltage follower buffers provide high current drive at frequencies ranging from dc to over 400 MHz. The hybrid devices are designed to meet the needs of a wide variety of applications, including high-speed line drivers, video impedance transformation, yoke drivers for high-resolution CRTs, and high-impedance input buffers. The LH4008 and LH4009 deliver a drive current of ± 200 mA into a $50\text{-}\Omega$ load at a slew rate of $10,000\text{ V}/\mu\text{s}$. Power bandwidth for the latter device is dc to 150 MHz, while the former's is dc to 130 MHz. The LH4010, with a bandwidth of dc to 20 MHz, has a slew rate of $2500\text{ V}/\mu\text{s}$ and a drive current of ± 100 mA. Coming in at dc to 160 MHz, the LH4011 provides ± 200 mA of drive current at slew rates of $5000\text{ V}/\mu\text{s}$. Finally, the LH4012 wideband buffer operates from dc to 490 MHz, provides ± 200 mA of drive current, and has a slew rate of $11,500\text{ V}/\mu\text{s}$. Prices range from \$21.60 to \$35.38 in 100-unit lots.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052; (408) 721-6486.

CIRCLE 360

DC CONVERTERS HAVE WIDE INPUT RANGE

In addition to offering a variety of output combinations, a family of dc-dc converters has a wide input voltage range to accommodate applications where the input voltage may vary substantially. Twenty-six different models are available ranging from 15 to 30 W. All units operate at a switching frequency of 100 kHz and attain efficiencies as high as 84%. The operating temperature range can be varied between -25° and $+71^{\circ}\text{C}$ without derating. Input/output isolation is 500 V dc. Several packaging options are available for pc board mounting. The converters are shipped from stock with prices starting at \$107.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000.

CIRCLE 361

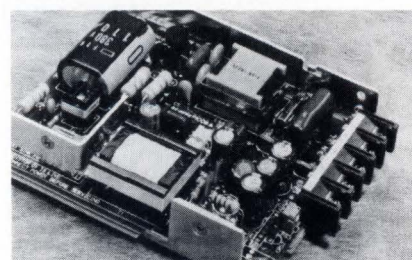
POWER MOSFETS COME IN SOT-89

Two new devices have been added to Supertex's current line of power MOSFETs, the TN0104N8 and TP0104N8, both housed in SOT-89 (TO-243AA) surface-mount packages. The latter is a p-channel complementary device, while the former is an n-channel, low-threshold version. Each has a drain-to-source breakdown voltage equal to 40 V minimum. On-resistance is rated at $2.0\text{ }\Omega$ maximum for the n-channel device and $4.0\text{ }\Omega$ maximum for the p-channel part at a V_{GS} of 10 V, as well as 5 V, for ensured performance with logic-level drive voltages. Both MOSFETs have a gate threshold voltage of 1.6 and 2.4 V maximum, respectively. The TN0104N8 and TP0104N8 are priced from \$0.49 to \$0.56 each, respectively, in lots of 1000.

Supertex Inc., 1225 Bordeaux Dr., Sunnyvale, CA 94089; (408) 744-0100.

CIRCLE 362

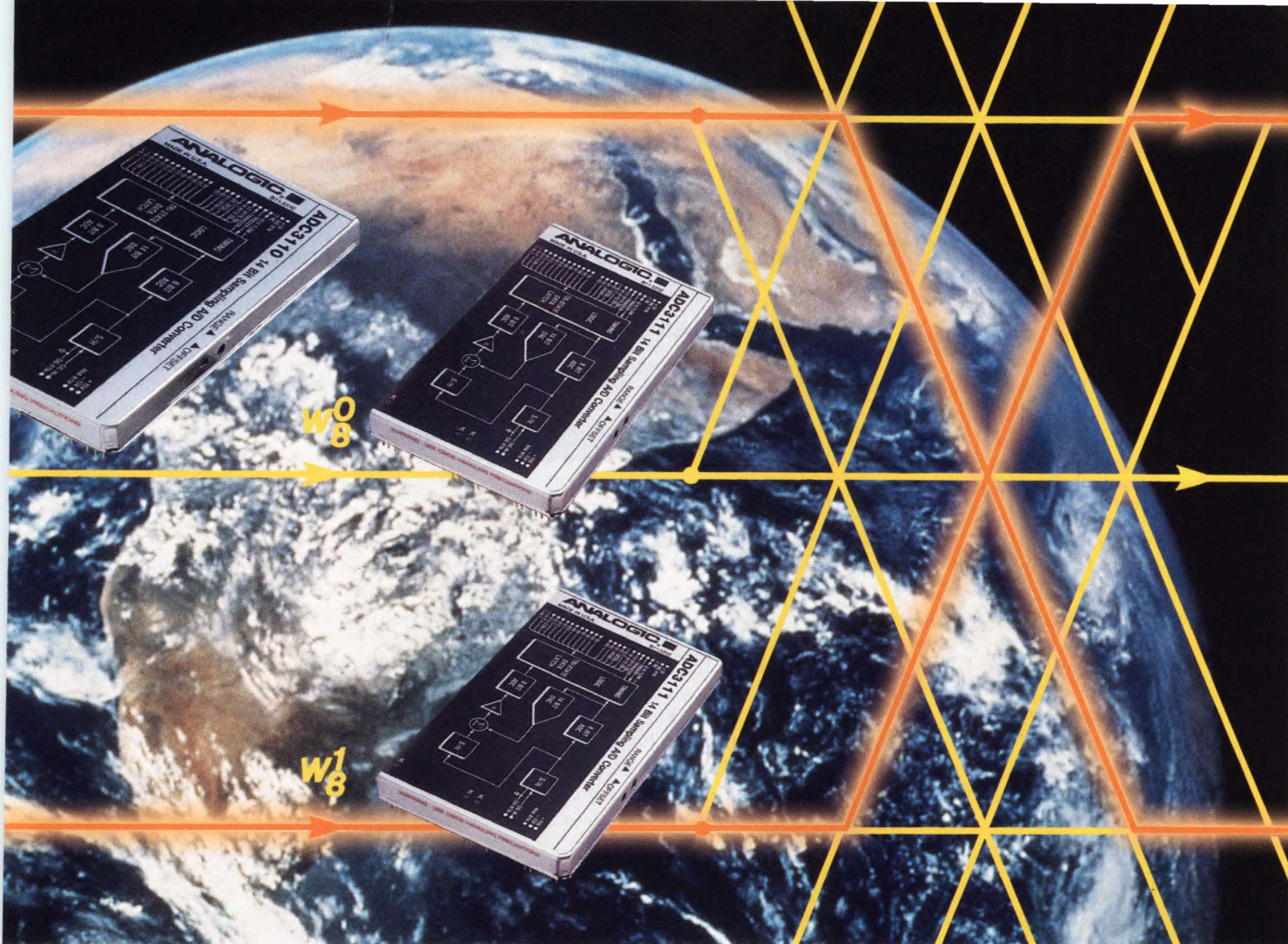
DC SUPPLIES KEEP A VERY LOW PROFILE



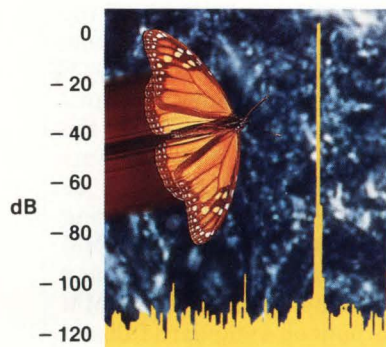
Available in three sizes — 15, 25, and 50 W — all models in the FAW series of dc power supplies are less than 1 in. high, allowing them to fit into spaces normally too small for conventional power supplies. Their wide input range accepts ac voltages from 85 to 264 V without selection. The filtered input of the supplies reduces conducted emi below FCC Class B and VDE 0806 levels. Units are housed in an open-frame L-chassis. Prices in unit quantities are as follows: \$55 for the 15-W supply; \$85 for the 25-W model; and \$110 for the 50-W version.

Kepco Inc., 131-38 Sanford Ave., Flushing, NY 11352; (718) 461-7000.

CIRCLE 363



Our A/D's Were Designed to Give You Butterflies*!



*True 14-Bit
Performance
at a 2 MHz
Sampling Rate*

* The illustrated flow graph of the Cooley-Tukey algorithm is known in the industry as a butterfly computation.

Analogic's new, ultra stable 14-bit sampling A/D converters make the most of your post-processing computations. Using advanced hybrid and surface mount technology, these sampling A/D's provide the most cost-effective solution to your high speed, high resolution applications.

The ADC3110 and ADC3111, designed for low noise and low distortion, provide 14 bits of resolution with true 14-bit performance. A 76 dB signal-to-noise ratio and our guarantee of no missing codes over an operating temperature range of 0°C to 60°C make these units unique. The ADC3110 in the time domain and the ADC3111 in the frequency domain will digitize signals up to 1 MHz at a 2 MHz rate, thus achieving unprecedented speed vs. accuracy performance.

Our new sampling A/D's will perform superbly in your most demanding OEM applications. Digital oscilloscopes, waveform analysis, high speed data acquisition, sonar and digital signal processors. Whatever your DSP needs, Analogic has a sampling A/D to help you catch the butterflies...fast.

We even pledge it in writing. Unlike other manufacturers, Analogic puts all our sampling A/D's through exhaustive tests on our proprietary automatic test systems. The test data shipped with each product is our proof that it meets or exceeds our published specifications. What else would you expect from the world resource for A/D converter technology?

For Application Assistance: Richard Lentini
Analogic Corporation, 360 Audubon Road,
Wakefield, MA 01880 (508) 977-3000 X2170
Telex: 466069, Fax: (617) 245-1274

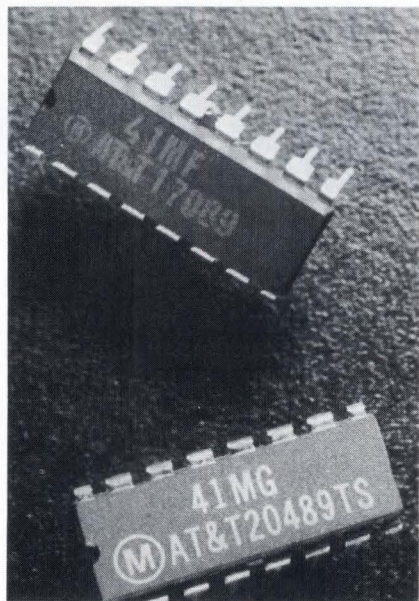
ANALOGIC ■

*The World Resource
for Precision Signal Technology*

LINE DRIVER-RECEIVER ICS SEND, RECEIVE DATA AT 400 MBITS/S

A series of line driver-receiver data-transmission ICs from AT&T Microelectronics offers data rates up to 400 Mbits/s. The M Series includes the 41MF, 41MR, and 41MT quad differential line receivers and the 41MP and 41MG quad differential line drivers.

The communications devices are pin-compatible with the industry-standard 26LS31 and 26LS32 TTL devices. But they generate a much lower level of emi because of their shifted ECL output levels, which reduce the common-mode output current. These same outputs have a low typical output skew of 0.2 ns, which helps maintain data fidelity.



The M Series parts are produced using AT&T's scaled fast oxide-isolated logic (SFOXIL) process technology. The series represents a redesign of an existing slower line of data-transmission devices.

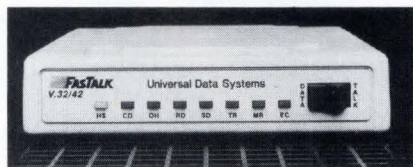
Prices for the chips in quantities up to 1000 are \$3.45 each in a DIP package and \$3.95 in a small-outline IC (SOIC) or small-outline J-leaded (SOJ) package. Quantity discounts are available on both versions.

AT&T, Dept. 52AL330240, 555 Union Blvd., Allentown, PA 18103; (800) 553-2448.

CIRCLE 334

RICHARD NASS

COMDEX/Fall '89 9600-BPS MODEM IS V.42 COMPATIBLE



A low-cost, 9600-bps V.32 modem complies with the CCITT's new V.42 error-correction standard. The FastTalk V.32/42 incorporates the standard, which uses both MNP-4 and LAP-M error-correcting protocols. The modem is compatible with the PC/AT command-set and supports MNP 5 data compression, which can increase its effective throughput up to 19,200 bps. The modem packs all this functionality in a small 9-by-6-by-2-in. case. This is comparable in size to other PC modems and is one of the smaller V.32 modems on the market. Other features include automatic adaptive equalization, tone-pulse dialing, audible call-progress detection, and integral diagnostics. Reliable full-duplex 9600-bps operation is achieved through the use of an echo-cancellation technique and a compact trellis-coded error-correcting capability. The modem is available now and sells for \$1045 each.

Universal Data Systems, 5000 Bradford Dr., Huntsville, AL 35805; (205) 721-8926.

CIRCLE 364

WIRELESS NETWORK USES INFRARED LIGHT

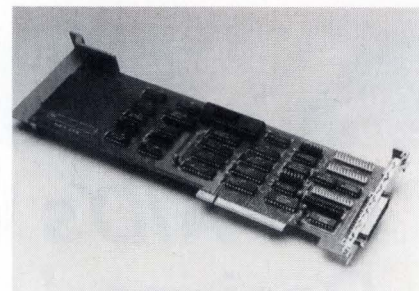
Designed to serve work groups in open or partitioned environments, the Photolink networking system uses infrared light, instead of cabling, to transmit data between computers within a local area network or between terminals and a host computer. The unit, which sits atop a partition or piece of furniture, is connected to the computer and shines an infrared light at the ceiling. Additional Photolink units are pointed at the same common spot, while an indicator light shows the user when the alignment is correct. The system automatically performs a sign-on procedure to ensure that neighbor-

ing units are aware of its presence, and the network is ready to run. Photolink is currently available for AppleTalk and LocalTalk networks for Macintosh-to-Macintosh connectivity and RS-232-C interfaces for terminal-to-host communications. Each unit accommodates up to four computers or terminals and can be mixed with cabling for connection to existing systems, wide area networks, and through-the-wall connections anywhere along the network. Photolink is priced at \$995 per unit; \$250 per node. A concentrator, required for RS-232-C hookups, costs an additional \$995.

Photonics Corp., 200 E. Hacienda Ave., Campbell, CA 95008; (408) 370-3033.

CIRCLE 365

PS/2 CARD SUPPORTS SYNC, ASYNC TASKS



Able to solve many OEM communication applications for the IBM PS/2, a dual-channel communication card supports synchronous and asynchronous transmissions at rates of up to 19,200 bits/s. Each of the GMM Sync/2's channels can be independently configured for either DTE or DCE operation. A built-in null modem option is also available. In the synchronous mode, the card supports such high-level protocols as SDLC, HDLC, and Bisync. During asynchronous operation, the GMM Sync/2 can communicate with any asynchronous device. The GMM Sync/2 is built on a standard full-slot Micro Channel Architecture card and requires 900 mA at 5 V, 40 mA at 12 V, and 40 mA at -12 V. It sells for \$100 in lots of 500.

GMM Research Corp., 2938 S. Daimler St., Suite 121, Santa Ana, CA 92705; (714) 752-9447.

CIRCLE 366



Smallest footprint. Lowest power.

A Spanking-new Family of 5-Volt Devices for Power-stingy Disk Drives.

If you're designing disk drives for use in applications where low power and small footprint are important, you need Silicon Systems' new family of low-power read-channel devices.

The family consists of three 5-volt-only high performance read-channel devices—the SSI 32R1200, SSI 34R4610, and SSI 32P548. The 32R1200 (Ferrite/MIG) and the 32R4610 (Thin Film) are R/W amplifiers—each providing a low-noise read amplifier, write drivers, and data protection circuitry. The 32P548 (Pulse Detector/Data Synchronizer) is a highly integrated combination circuit containing complete pulse detection, data synchronization, and embedded servo

capture electronics.

An entire data channel using this 5-volt family is capable of operating on a stingy 750mW while still providing high performance. Alternate design solutions often consume as much as two to three times more power. In addition to low operating power, two independent power-down states are provided. The first is a sleep state included in each device for power savings during idle conditions. The second state, contained in the 32P548, powers down circuitry not required during servo acquisition.

The 32P548 comes in a 52-pin fine-

pitch quad flat pack (body 390 x 390 mils) and the 32R1200, 32R4610 Read/Write devices are available in standard 16-pin and 20-pin SO packages.

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DEBUGGER EVALUATES SOURCE-LEVEL ADA CODE IN REAL TIME

Name	Value	Unit	PA (actual)
Total Samples:	111011		
start_body	48000	43.0%	*****
in_ill_done	35600	32.0%	*****
determine_min	17200	15.0%	*****
determine_max	7200	6.0%	*****
Other	3010	2.0%	***
overflow_except	0	0.0%	
Divide_by_0	0	0.0%	

Supporting the Tektronix MV6820 emulator, the TekDB/Ada source-level debugger creates a real-time execution environment for testing and debugging Ada software. The tool works with a number of different compiler systems.

The debugger incorporates a powerful performance analyzer that can pinpoint "hot spots" in the Ada run-time code. The analyzer summarizes each run with a histogram showing the relative amount of execution time for each module or memory range. Since the program executes in real time, the user can quickly evaluate modifications. Also, the performance analyzer helps monitor the effects of compiler optimizations.

Because the debugger transfers the run-time software using a common object format supported by most Ada-compiler vendors, designers can use different compilers while maintaining the same interface and functionality. The tool works with Ada 68020 cross-compilers from Alslys, SC/SCICON, and Telesoft.

The interface employs an interactive windowed screen to display the debug information and provide control. Ada source-level statements are always displayed simultaneously with other debug data. Highlighting points out where the current program is executing and the location of active breakpoints.

Prices for the VAX versions of TekDB/Ada range from \$3850 to \$7900. The Sun 3 version costs \$3850. Delivery is in 2 weeks.

Tektronix Inc., Microprocessor Development Products, P.O. Box 12132, Portland, OR 97212; (800) 245-2036.

CIRCLE 335

JOHN NOVELLINO

DRIVER FOR MS-DOS WORKS OVER SCSI BUS

A software driver is designed for managing disk and tape drives based on the Small Computer System Interface (SCSI) in MS-DOS environments. Designated the ASW-1110, it includes the MS-DOS version of Sytron Corp.'s SY-TOS, the industry-standard 5-in. cartridge tape management package. It supports more than 20 manufacturers' drives and is the only product to support 150-Mbyte drives from Cipher, Archive, and Wangtek. Combined with Adaptec's AT and Micro Channel host adapters, the driver provides a one-slot solution to peripheral control. With it, two or more disk drives can be connected to the SCSI bus, as can tape drives, optical drives, and printers. ASW-1110 helps microcomputer users and integrators lower the cost of system development and upgrading since there is no need for new I/O boards to handle additional peripherals. ASW-1110 sells for \$149.

Adaptec Inc., 691 S. Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600.

CIRCLE 367

SOFTWARE MANAGES 68HC11 EEPROMS

Intended for use on IBM PC, XT, AT, and compatible computers, an EEPROM management program allows users to program, read, and configure EEPROMs in a variety of target systems based on the Motorola 68HC11 single-chip microcontroller. The EEPROM Manager can be used in software development, production calibration, field programming, and other applications where data in the target-system EEPROM must be read or changed. The only requirements for the target system are that it have an RS-232-level converter connected to the microcontroller's serial communications interface and that it be configured to the microcontroller bootstrap operating mode. The host PC requires a standard serial adapter and a three-wire connection. The program allows baud rate and programming algorithm adjustments to accommodate target sys-

tem clock rates from 2 to 8 MHz. A single-user license costs \$75.

Polyarts Co. P.O. Box 11517, Seattle, WA 98110; (206) 522-4871.

CIRCLE 368

SOURCE-LEVEL DEBUGGER IS MONITOR-BASED

Designed for real-time embedded C and assembly programs, the RMXDB 5.0 ROM monitor-based source-level cross debugger combines the powerful source-level debugging features of XDB 5.0 with a low-level target monitor program. Designers who previously used XDB with in-circuit emulators now have a choice of debugging their prototype systems with a monitor-based debugger. The ROM monitor version has the same multi-window user interface and command language as the emulator-based XDB. It also provides the ability to display source code, registers, and stack information; set software breakpoints; single-step at the C or assembly level; monitor and modify data; define macros and aliases; record and playback debugging sessions; simulate target I/O; and access pop-up windows for status information and online help. Motorola 68000 and Intel 8086 versions of RMXDB 5.0 will be available in the fall. Prices start at \$3000 on the IBM PC.

Intermetrics Inc., 733 Concord Ave., Cambridge, MA 02138; (617) 661-1840.

CIRCLE 369

COMPRESSION SOFTWARE YIELDS 20:1 RATIO

To meet the demand for compression and decompression of high-resolution color images without noticeable degradation, NDC has introduced a highly effective software system to do the job. The program allows images to be captured at full resolution — 2000 by 3000 pixels by 24 bits of color — and compressed for storage at 1.2 to 1.5 bits of color. The result is a compression ratio of up to 20:1, far greater than what is now available.

National Digital Corp., 2781A Hartland Rd., Falls Church, VA 22043; (703) 573-5100.

CIRCLE 370

AT&T from HAMILTON/AVNET

Put your finger on the pulse of efficient computing with the world's smallest, crystal oscillator from Hamilton/Avnet — AT&T's s-type oscillator.

Hermetically packaged in low profile, ceramic, 6-pin DIPs, AT&T oscillators have three-state output, and feature surface mount or through-hole capabilities which provide customers with a variety of design options.

The s-type oscillator's small size (300 x 335 mils) also saves board space, while its wide temperature range and TTL/CMOS compatibility provide design flexibility and long-term reliability.

And with Hamilton/Avnet's services, you're assured stock that can be shipped overnight or just-in-time.

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CIRCLE 160

YOUR SYSTEM WON'T SKIP A BEAT WITH AT&T S-TYPE OSCILLATORS FROM HAMILTON/AVNET



Why our chip inductors are more attractive for your high frequency applications

Theirs.



Ours.



The point of this little demonstration is that Coilcraft surface mount inductors are made of ceramic. A decidedly non-magnetic material.

Most other chip inductors are made of ferrite. Which is great for demonstrating the principles of magnetism, but not so hot for high frequency magnetics.

Take self resonance, for example. SRFs on our coils are up to 3 times higher than equivalent ferrite chips. And located a safe distance away from your operating frequency.

The actual inductance you'll get with Coilcraft chips at higher

frequencies is very predictable and consistent. Not so with ferrites. Beyond the test frequency, their inductance curves rise steeply and vary significantly from part to part.

Coilcraft ceramic chips also have a low temperature coefficient of inductance: +25 to +125 ppm/°C, depending on inductance. TCLs on ferrite chips are often two to four times higher!

And if you need close tolerance parts, we offer even more advantages. Thanks to our computer-controlled manufacturing and ceramic's neutral properties, it's easier for us to make 5% or 2%

parts. We can even production-test at your operating frequency! Other chip makers have to cope with ferrite's permeability variations, so their yields are lower. Which means delivery can be unpredictable.

So next time you're selecting surface mount inductors, forget the ferrite and stick with Coilcraft ceramic chips.

For complete specifications and information on our handy Designer's Kits of sample parts, circle the reader service number. Or call 800/322-COIL (in Illinois 312/639-6400).

Coilcraft

See our catalog in Vol. A, Section 1800
EEEM / electronic engineers master

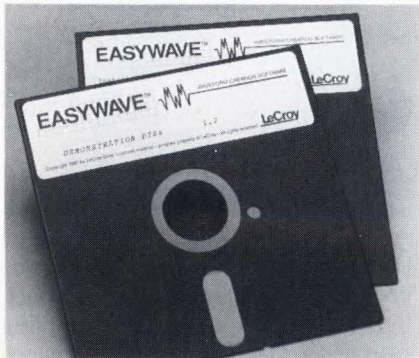
1102 Silver Lake Road, Cary IL 60013 800/322-COIL Fax 312/639-1469

SCHEMATIC SOFTWARE GAINS NEW LIBRARIES

OrCAD/SDT III, a PC-based schematic capture program from **OrCAD Systems Corp.** (Hillsboro, Ore.), has been updated with new libraries of programmable logic devices, raising the number of unique parts in the OrCAD libraries to well over 6200. These include devices from Altera and Intel, as well as generic parts. Other refinements to the software include a display-driver generating utility, which creates custom drivers for all VGA- and EGA-compatible monitors having up to 800-by-600-pixel resolution. Additionally, three new video drivers have been added for monitors with resolutions of 1024 by 768 pixels. ROM primitives are now available for use with OrCAD's logic simulator, and enhancements have also been made to the library editor. OrCAD/SDT III version 3.21 sells for \$495 with free updates to all registered users under warranty.

CIRCLE 371

WAVEFORM SOFTWARE: TRY BEFORE BUYING

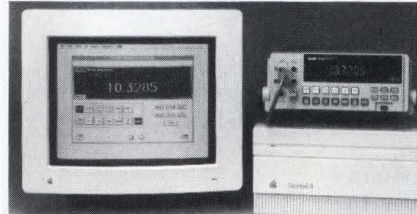


Easywave, a software package that supports the 9100 Series Arbitrary Function Generators (AFG) from **LeCroy Corp.** (Chestnut Ridge, N.Y.), is now being offered for a free trial. The software lets users create custom or standard waveforms or digital patterns, control any of the 9100 series generators, and capture, modify, and transfer any 9400 series oscilloscope display to the AFG. The waveforms and patterns can be created by equations, point-by-point entries, waveforms captured by the 9400 series scopes, or by selecting a

standard element (sine and square waves, ramp, exponential, etc.) from its library. The software costs \$1450.

CIRCLE 372

INSTRUMENT-CONTROL SOFTWARE RUNS ON MAC



A new version of an IEEE-488 handler is run on Apple Macintosh computers. This version, from **National Instruments Corp.** (Austin, Texas), includes a tool called Hyper488 that uses HyperCard stacks and a HyperTalk language interface to simplify the development of IEEE-488 control applications. The software will be furnished on a separate diskette as part of the standard NI-488 Macintosh handler software package. It is sent free with the purchase of one of the company's GPIB interface boards for the MAC SE or MAC II computers. Current NI-488 Mac software users can get free upgrades by calling National Instruments.

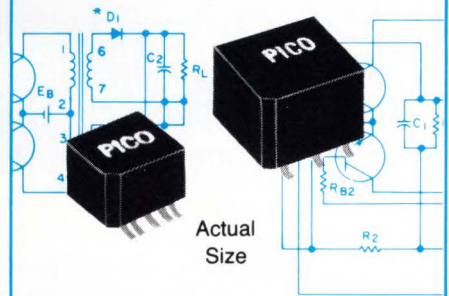
CIRCLE 373

SYSTEM LINKS BOARD-TEST EQUIPMENT

Added capabilities and greater configurability now grace the Board-Watch test process management system from **Teradyne Inc.** (Boston, Mass.). Version 2.0 now supports a new option, the Board Routing and Work-in-Progress Tracking Module, which gives users a flexible means of controlling the flow of various circuit board types through production test. BoardWatch is also now available under a single-tester license, giving first-time ATE users a pre-configured, entry-level system that can be upgraded as their production needs grow. Price of an entry-level package ranges from \$35,000 to \$42,000, depending on the tester model. The Board Routing/WIP Tracking Module starts at \$20,000.

CIRCLE 374

ULTRA-MINIATURE SURFACE MOUNT



Actual Size

DC-DC Converter Transformers and Power Inductors

These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The Inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

- Operation over ambient temperature range from -55°C to $+105^{\circ}\text{C}$
- All units are magnetically shielded
- All units exceed the requirements of MIL-T-27 ($+130^{\circ}\text{C}$)
- Transformers have input voltages of 5V, 12V, 24V and 48V. Output voltages to 300V.
- Transformers can be used for self-saturating or linear switching applications
- Schematics and parts list provided with transformers
- Inductors to 20mH with DC currents to 5.4 amps
- Inductors have split windings

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CIRCLE 137

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high-inrush applications.

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poles. Use as ON/OFF switch or with optional
lamp as power indicator.

KD1 — Pushbutton protector fits in
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CIRCLE 139

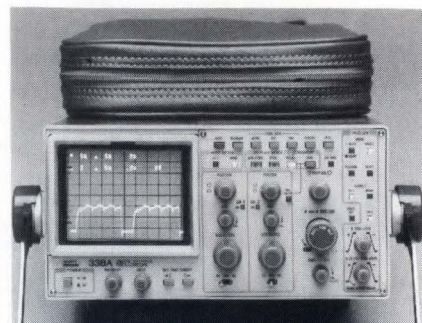
PRODUCT NEWS

ENHANCED SYSTEM SPEEDS FAULT SIMULATION

With the added support of distributed fault analysis in networked computer environments, **Teradyne Inc.**'s (Boston, Mass.) **Lasar Version 6.4** simulator cuts fault simulation run times of complex VLSI devices and circuit boards. The new release also supports the use of Teradyne's **DAT-Source VLSI modeling system** as a network resource. In addition, the company is offering a postprocessing software package that translates functional test and diagnostic programs developed on the Lasar system for use on Genrad's 2225/35 benchtop board tester. Further, the postprocessor converts Lasar's fault dictionary into a format usable by the 2225/35 tester, which until now, had no fault dictionary capability.

CIRCLE 375

SCOPE'S SAMPLING RATE JUMPS TO 20 MSAMPLES/S



An enhanced version of the 336 digital storage oscilloscope offers improved performance in a compact, lightweight package. The sampling rate of the 336A has been increased to 20 Msamples/s, the vertical resolution to 8 bits, and the expanded memory to 16 kbytes. Other new features include auto setup, GPIB compatibility, on-screen readout, and the ability to save up to 16 waveforms. With its high sampling rate and a single-shot bandwidth of 2.8 MHz, the 336A from **Tektronix Inc.** (Beaverton, Ore.) is suitable for servicing digital equipment and a variety of power-distribution and electromechanical applications. It sells for \$5745, the same as the original 336.

CIRCLE 376

THE MOMENT OF TRUTH *

Today's tough product liability laws, along with tightened manufacturing standards, demand more accurate product performance information.

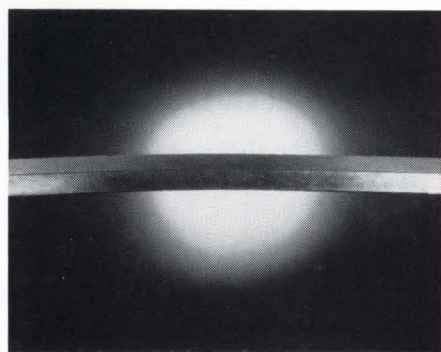
Plastics Engineering Company, Sheboygan, Wisconsin, manufacturers of Plenco thermoset molding compounds, is concerned that temperature/stress ratings for engineering thermoplastics may not reflect actual performance under load at high temperatures. Current test methods either measure strength after a heated part has cooled or measure the temperature at which a test sample deflects 0.010 in.

Plastics Engineering Company conducted a test of twelve materials' ability to perform under continued

load at high temperature to determine a heat stress rating. The results of the heat and stress tests of nine engineering thermoplastics showed catastrophic failure at maximum temperature ratings significantly below their published deflection temperature under load. The engineering-grade phenolic was a different story.

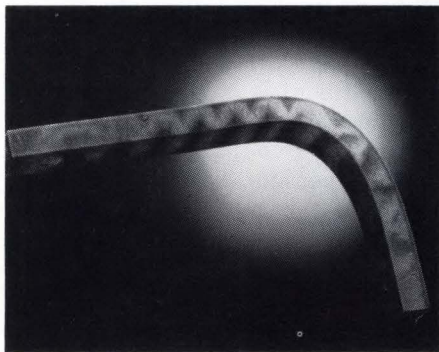
Plenco 06582 withstood the stress and more heat, far longer. And it costs a fraction of the engineering thermoplastics.

The results of these tests should be reviewed by engineers, designers, and manufacturers—anyone who specifies plastic parts. For a detailed report write or give us a call at (414) 458-2121. You'll be glad you did instead of wish you had.



* FOR PLENCO 06582— 500 HOURS AT 285°C.

Plenco 06582 was subjected to the highest heat possible in a standard laboratory test oven—285°C—for 500 hours. The test sample deflected only 4° under continued stress.

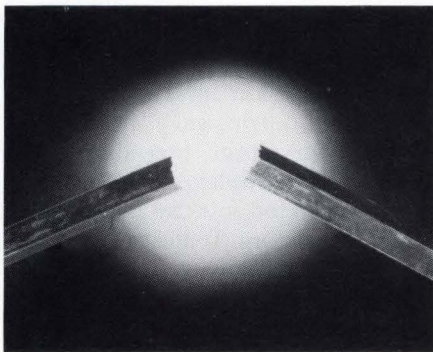


* FOR POLYSULFONE— 41 HOURS AT 170°C.

Polysulfone, under this test method, demonstrated a maximum temperature rating of 160°C compared to its published deflection temperature under load (ASTM D648) rating of 175°C. Polysulfone deflected 90° after 41 hours of exposure to 170°C.

* FOR POLYETHERSULFONE— 100 HOURS AT 190°C.

Polyethersulfone (30% glass), under this test method, demonstrated a maximum temperature rating of 180°C compared to its published deflection temperature under load (ASTM D648) rating of 205°C. Polyethersulfone deflected 90° after 100 hours of exposure to 190°C.



* FOR POLYPHENYLENE SULFIDE— 3 HOURS AT 255°C.

Polyphenylene sulfide (40% glass), under this test method, demonstrated a maximum temperature rating of 245°C compared to its published deflection temperature under load (ASTM D648) rating of 260°C. Polyphenylene sulfide fractured after 3 hours of exposure to 255°C.

* POLYBUTYLENE TEREPHTHALATE— 8 HOURS AT 150°C.

Polybutylene terephthalate (30% glass), under this test method, demonstrated a maximum temperature rating of 140°C compared to its published deflection temperature under load (ASTM D648) rating of 200°C. Polybutylene terephthalate fractured after 8 hours of exposure to 150°C.



* POLYETHELENE TEREPHTHALATE— 8 HOURS AT 170°C.

Polyethylene terephthalate (30% glass), under this test method, demonstrated a maximum temperature rating of 160°C compared to its published deflection temperature under load (ASTM D648) rating of 210°C. Polyethylene terephthalate fractured after 8 hours of exposure to 170°C.

* FOR POLYETHERIMIDE— 55 HOURS AT 195°C.

Polyetherimide (10% glass), under this test method, demonstrated a maximum temperature rating of 185°C compared to its published deflection temperature under load (ASTM D648) rating of 210°C. Polyetherimide deflected 90° after 55 hours of exposure to 195°C.

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HOW TO DIGITIZE TRANSDUCER OUTPUTS

Advice on the direct digitization of transducer outputs is given in a 16-page application note (AN7). The document details circuit techniques which directly digitize the low-level output of a variety of transducers and includes schematics of circuits used for temperature-to-frequency conversion, thermocouple-to-frequency conversion, an acoustical thermometer, a strain gauge digitizer, a photodiode digitizer, and humidity-to-frequency conversion.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900. CIRCLE 377

SPICE MACROMODELS SIMULATE OP AMPS

Available free of charge in separate application note forms, three Spice models are intended to help designers accurately simulate the OP-64 (AN-110), OP-42 (AN-117), and OP-400 (AN-120) op amps. Each note contains a macromodel schematic and a model net list. These models represent the latest in modeling techniques, which produce an unprecedented level of accuracy in ac response and device behavior to help designers accurately simulate their circuits. They pay strict attention to the frequency poles and zeros that determine the frequency response of op amps. Additionally, the macromodels have overcome the requirement for internal grounds, which do not exist with real op amps. Unlike older Spice models, all currents are accounted for in the output stage.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, CA 95052; (408) 562-7470. CIRCLE 378

BROCHURES ON SCR POWER CONTROLS

Three product brochures offer descriptions, features, mounting di-



mensions, weights, power requirements, and ordering information about the 1P Series silicon-controlled rectifier (SCR) power controls. The units are used to control voltage, current, or power to resistive and transformer-coupled loads. Current ratings are from 60 to 1200 A, and all standard line voltages are accepted at 50 or 60 Hz. A special softstart feature prevents transformer saturation, blown fuses, and circuit-breaker tripping.

Halmar Electronics Inc., 900 North Hague Ave., Columbus, OH 43204; (614) 275-0530. CIRCLE 379

PROTECTING MULTIPLEXERS AGAINST OVERVOLTAGE

A two-page brochure contains a brief analysis on overvoltage protection for the ADG5XXA series of multiplexers from Analog Devices. Although not intrinsically protected against overvoltage exceeding the rails, these multiplexers can easily be well protected with the addition of external resistors. Topics covered in the note discuss why overvoltage protection is necessary and the advantages of external protection.

Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 02021; (617) 461-3043. CIRCLE 380

FLASH TESTING CERAMIC CAPS

A six-page technical article outlines a constant-current flash testing concept for qualifying multilayer ceramic capacitors in zero defect testing programs. The illustrated bulletin provides an overview of flash testing (also known as dielectric withstanding voltage testing) used to detect internal dielectric weaknesses in multilayer ceramic capacitors. It provides a step-by-step analysis of both the conventional resistor-limited flash testing approach and the new constant-current method incorporating ESI's Model 5300 flash tester.

Electro Scientific Industries Inc., 13900 N.W. Science Park Dr., Portland, OR 97229; (503) 641-4141. CIRCLE 381

POWER REGULATION FOR BATTERY OPERATION

An informative application note entitled, *AN8: Conditioning Techniques for Batteries*, describes a variety of voltage regulation circuits for battery-powered applications. Various approaches for power conditioning are described for both switching and linear regulators, with attention paid to efficiency and low-power operation. Fourteen circuits are depicted, including schematics and performance data.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900. CIRCLE 382

MICROSTEPPING TWO-PHASE STEPPER-MOTOR CIRCUITS

In eight pages, a short tutorial is presented on microstepping two-phase stepper motors. It also contains a discussion on the advantages of using 8-bit digital-to-analog converters instead of those with 6 bits and the benefits of closed-loop versus open-loop controls. Other sections include torque-load effects, and microstepping basics. Two practical circuits are given as examples.

Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 02021; (617) 329-4700. CIRCLE 383

TRANSPUTERS FOR PARALLEL PROCESSING

A 50-page reference manual provides a comprehensive introduction to parallel processing and transputer technology. The report identifies the different types of parallel architectures and describes applications that exhibit parallelism. It also discusses transputer operating environments and languages designed to provide the microcomputer with parallel processing capabilities.

MicroWay, P.O. Box 79, Kingston, MA 02364; (508) 746-7341. CIRCLE 384

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CIRCLE 115

GUIDE DISCUSSES ELECTRICAL INSULATION

Preventive maintenance for electrical insulation of wires, cables, motors, generators, transformers, switches, and other electrical equipment is made easier with a pocket-size handbook from Biddle Instruments. The booklet defines "good" insulation, then explains what makes insulation go bad, how insulation resistance is measured, and how to interpret resistance readings. It also discusses three common test methods: short-time or spot reading, time resistance, and step or multi-voltage tests. Photos, charts, and drawings serve as visual aids. The manual costs \$5.

Biddle Instruments, 510 Township Line Rd., Blue Bell, PA 19422; (215) 646-9200. **CIRCLE 385**

DC-DC CONVERSION MADE EASY

Containing 44 pages, *AN29: Some Thoughts on Dc-Dc Converters* contains a host of information and schematics on dc-to-dc conversion. Tested circuit designs are included, complete with schematics and component values, for low-noise converters, micropower quiescent current converters, high-efficiency converters, wide-range-input converters, high-voltage converters, and switched-capacitor-based converters. Appendices offer advice on conversion from 5 to ± 15 V, inductor selection for flyback converters, optimizing for efficiency, and the most useful instruments for converter design. Descriptions of a number of monolithic converter ICs are also included.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900. **CIRCLE 386**

SCHEMATICS DEPICT POWER GAIN STAGES

An application note provides numerous voltage-gain and current-boost circuit descriptions and schematics useful for those involved in the design of power gain stages for elec-

tronic equipment. *AN18: Power Gain Stages for Monolithic Amplifiers* also includes a primer on oscillation problems and frequency compensation.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900. **CIRCLE 387**

MOUNTING TECHNIQUES FOR POWER DEVICES

Mounting Considerations For Power Semiconductors

(AN1040/D) discusses such design aspects as mounting surface preparation, state-of-the-art insulators and thermally conductive material performance data, fastener and hardware characteristics, fastening techniques, free air and socket mounting techniques, and thermal system evaluation in mounting power devices. Also described are mounting techniques for some of the new packages available from Motorola, such as the surface-mounted DPAK, isolated FullPak, ICePAK, and EMS power modules.

Motorola Inc., Literature Distribution Ctr., P.O. Box 20924, Phoenix, AZ 85063; (602) 994-6900. **CIRCLE 388**

LINEAR ICS PROVIDE POWER MANAGEMENT

Covering more than 100 devices, Silicon General's 1989 product guide provides detailed specifications and design information on a complete line of linear power-management ICs. The 720-page publication is divided into 13 chapters covering power supply circuits, motion control circuits, power driver and interface circuits, operational amplifiers and comparators, core memory, automotive, and other circuits. Also included is a chapter covering topics from designing with integrated regulated pulse-width modulators to a tutorial on power switch drivers for switched-mode power supplies.

Silicon General, 11861 Western Ave., Garden Grove, CA 92641; (714) 898-8121. **CIRCLE 389**

DATABASE PROVIDES DEVICE INFORMATION

The recently enhanced and enlarged *Integrated Circuit and Discrete Semiconductor D.A.T.A. Digest* database series provides design engineers with all the information they need to make initial device selection. Supplied in magnetic tape or CD ROM formats, the database provides useful descriptive device pinout information, product identification by function and technical characteristics, electrical parameters, generic part and specific manufacturer part numbers, packaging information, identification of numerous discontinued devices, and alternative sources and replacements for all listed devices. Specialty reference *Digests* are also available, including one with application notes and another an international semiconductor directory.

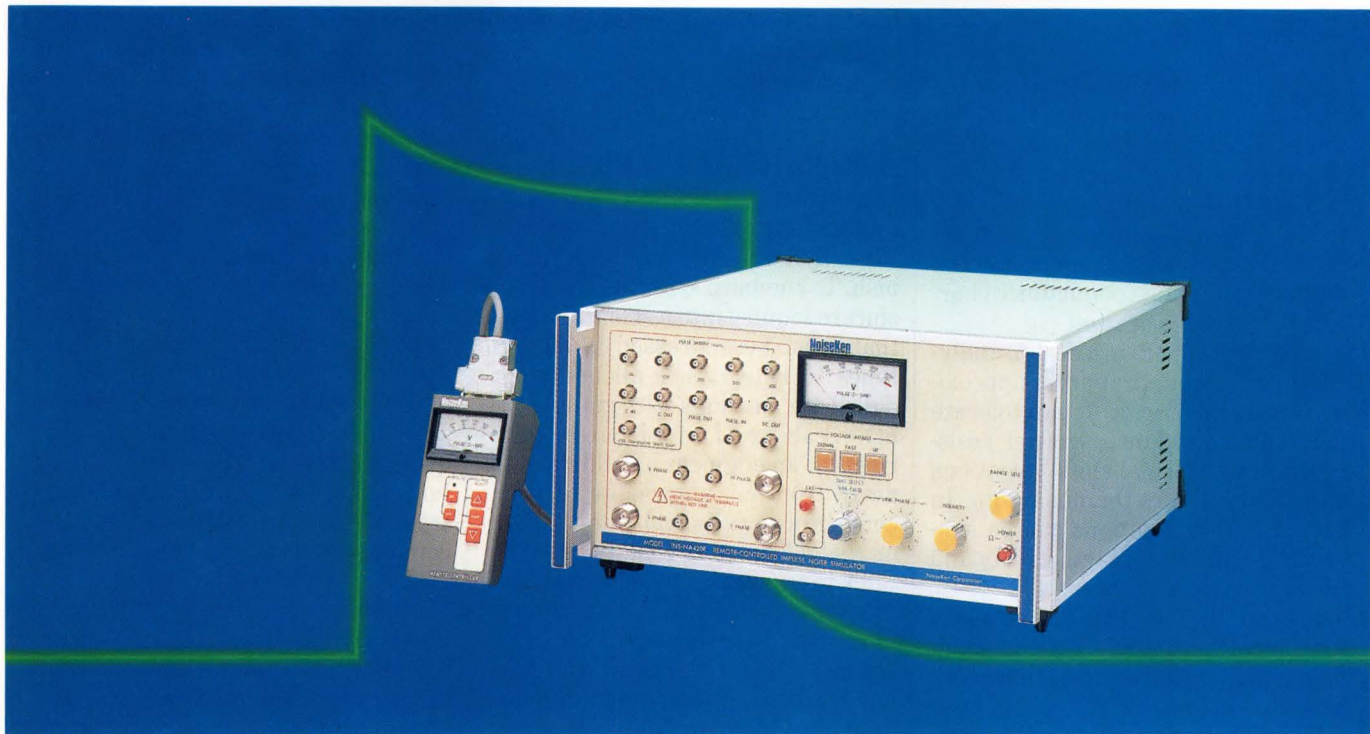
D.A.T.A. Business Publishing, 9925 Carroll Canyon Rd., P.O. Box 26875, San Diego, CA 92126; (800) 447-4666. **CIRCLE 390**

PRINCIPLES OF POWER CONVERSION

The extensive *Power Supply Engineering Handbook* contains 174 pages of detailed information on dc-dc converters, linear power supplies, and switching power supplies. Also provided is a 24-page section entitled, *Principles of Power Conversion*, which gives a basic technical background on how power supplies and dc-dc converters work, how to test them, how to apply them, and how to manage thermal problems. A technical glossary defines over 100 power supply terms. A quick selection guide lists basic specifications for cased, encapsulated, Mil-Spec, and open-frame units in order that users may locate a specific model series based on product type, output power, and output voltages.

Computer Products Inc., 3785 Spinnaker Ct., Fremont, CA 94538; (415) 657-9837. **CIRCLE 391**

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CIRCLE 170



ADDED SPICE**Dear Editor,**

I would like to respond to a letter that you published (*June 22*) by Keats Pullen, Jr. regarding the Spice article Gene Cavanaugh and I wrote (*April 13*). Gene and I take exception to Mr. Pullen's contention that transistor beta is imaginary data and that only the transconductance characteristic should be used.

First, use of beta in a design analysis yields a good, first-order approximation of the circuit. It can tolerate low input impedance, emitter resistance, and thermal-shift variations with fewer errors than using g_m . In fact, initial calculations can be simplified to ignore voltage effects and be reasonably accurate.

Second, the Gummel-Poon transistor model accurately reflects both beta and g_m effects during Spice simulation.

Third, both domestic and international semiconductor vendors publish guaranteed dc gain specs, which can be used for customer acceptance. Although g_m values can be determined from the data provided, the values are not guaranteed by the vendor.

In summary, the use of beta as a primary design characteristic is well supported in terms of design practicality, Spice simulation capabilities, and vendor guarantees.

Olive J. Smith

IVAC Corp.

San Diego, Calif.

WHO ARE YOU?**Dear Editor,**

I finally got around to reading my Aug. 10 ELECTRONIC DESIGN. Your Technology Briefing (p. 16) showed great insight and brave candor. We have been presuming that the brain is a computer simply because one of its capabilities is computing. Being human must be something more: We are self-aware, unpredictable, have personal identity, etc. No machine, even if duplicating my thoughts, could ever say, "I am you today." Who would I be then?

Boy are you going to make the pompous, presumptuous, and proud mad! But I know now I am reading an

honest journalistic endeavor. Keep up the good work.

Bryan Glett

Bellefontaine, Ohio

A ROSE BY ANY OTHER...**Dear Editor,**

Your editorial, "The Shockley-Rose Syndrome" (*Sept. 14*) is rubbish. To compare William Shockley's sincere inquiry into a scientific issue that must be addressed in modern times to Pete Rose's allegedly sordid, illegal dealings with gambling is utterly absurd. I infer from the editorial that an engineer should not step away from his knowledge of semiconductor physics and enter "another realm." In your case this is true: Stick to engineering—don't try to define ethics or morality. Your editorial reflects your incompetence in the realm. William Shockley's studies were misunderstood, and in your case they were probably not understood at all.

I am an electrical engineer but I took many courses in biology, biochemistry, and genetics and nothing William Shockley said was untrue, misleading, or unethical, unless you believe that important scientific truths should be withheld. I find your editorial to be uninformed, illogical, and an insult to the memory of William Shockley.

Robert B. Rose

Falls Church, Va.

ANOTHER THORN**Dear Editor,**

I read your editorial (*Sept. 14*) with some interest as you compared the self assuredness of Pete Rose and William Shockley. I do think that you are off base in comparing the damage the two individuals have wrought on the world. Gambling on baseball only negatively impacts the gamblers in the world and possibly the athletes involved. Considering that baseball is a "pastime" and not a major contributor to the GNP points to the insignificance of Pete Rose.

Mr. Shockley, on the other hand, by being the father of the semiconductor industry, has in effect created an environment in his likeness. At first glance you will deny this, but

look at the industry. First, I have yet to see an African-American Vice President or Director in the semiconductor industry and I have worked at two of the largest companies in the world (Motorola and Intel). Are you aware of any?

It is a well known business practice that it is important to socialize with superiors, peers, and subordinates. I am sure that in the development stages of the industry, there was a certain homogeneity of the participants in order to facilitate research and development. Consequently, there is, I believe, a consistency to the first-generation industry greats, which in turn, sets the company cultures for those to follow.

I think you have grossly trivialized the impact of Shockley on the minority community. Unfortunately your opinion and thought process is consistent with the mind-set of the industry he fathered.

Name withheld by request

Although it is not our policy to publish anonymous letters, we found the following letter regarding "The Rose-Shockley Syndrome" editorial interesting.

Over-40 engineers are being frustrated and demoralized by management. All of the state-of-the-art assignments are given to young engineers. You got the point? Young engineers are less expensive!

REAL WORLD**Dear Editor,**

Your editorial, "The Real World," (*Sept. 28*) was both refreshing and "Right on the mark." Being responsible for mixed analog-digital IC design, I also found the DSP article informative. However, the section on analog integration left me baffled.

In my opinion, the biggest problem facing "mixed" designers is preventing digital coupling from degrading the analog signals. I have yet to encounter a design where the analog section harms digital performance given that the analog signal is what is "real."

Kevin J. McCall

Sudbury, Mass.

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head to head with Thomas Gerhard Clarke.
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He's brilliant. He's quick. And he isn't nice. If you're going into a meeting with someone like this, you had better arrive there well-rested, well-nourished, and well-prepared. That's what our First and Executive Class service is designed to help you do. The way we see it, our on-ground and in-flight staff has only one job: to help you do your job. For international First or Executive Class reservations, contact your travel agent or Northwest at 1-800-447-4747.

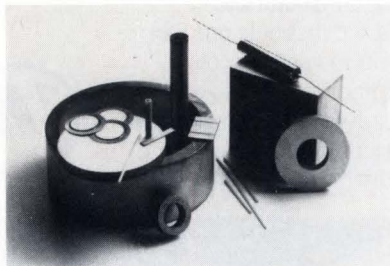


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CIRCLE 112

UPCOMING MEETINGS

NOVEMBER

COMDEX/Fall '89, November 13-17. Las Vegas, NV. Cheryl Delgreco, The Interface Group Inc., 300 First Ave., Needham, MA 02194; (617) 449-6600.

NEPCON Souteast '89 (National Electronic Packaging and Production Conference), November 14-16. Orange County Convention Center, Orlando, FL. Market Communication Associates, 230 E. Ohio St., Chicago, IL 60611; (312) 944-7610.

Wescon '89, November 14-16. Moscone Convention Center, San Francisco, CA. Alexes Razeovich, IEEE, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

Electronic Services Expo, November 28-29. Santa Clara Convention Center, Santa Clara, CA. SHO Inc., 167 S. San Antonio Rd., Ste. 4, Los Altos, CA 94022; (415) 949-2050.

Lasers in Electronics Manufacturing, November 29-30. Hyatt Palo Alto, Palo Alto, CA. Diane Korona, Society of Manufacturing Engineers, One SME Dr., P.O. Box 930, Dearborn, MI 48121; (313) 271-1500.

DECEMBER

International Conference on Design for Manufacturability and Concurrent Engineering '89, December 3-6. Fontainebleau Hilton, Miami Beach, FL. Kim Takita, Management Roundtable Inc., 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-8080.

1989 Winter Simulation Conference, December 4-6. The Capital Hilton Hotel, Washington, DC. Barry Nelson, Ohio State University, Dept. of ISYEE, 1971 Neil Ave., Columbus, OH 43210; (614) 292-0610.

UNICOM '89, December 5-7. Infomart, Dallas, TX. Jozy Schlosser, North American Telecommunications Association, 2000 M St., N.W., Washington, DC 20036; (202) 296-9800, ext. 229.

American Society of Mechanical

Engineers' (ASME) Winter Annual Meeting, December 10-15. San Francisco Hilton, San Fransisco, CA. Jeff Lenard, ASME, 345 E. 47th St., New York, NY 10017; (212) 705-7740.

1989 AEC Expo, December 12-14. Javits Convention Center, New York, NY. Expoconsul International Inc., 3 Independence Way, Princeton, NJ 08540; (201) 987-9400.

Technology '89 (Advanced Manufacturing & Technology Exposition), December 13-14. Mesa Convention Center, Mesa, AZ. C/S Communications Inc., P.O. Box 23899, Tempe, AZ 85285; (602) 967-7444.

JANUARY

International Winter Consumer Electronics Show (CES), January 6-9, 1990. Mirage Hotel, Las Vegas, NV. Cynthia Saraniti, Electronic Industries Association/Consumer Electronics Group, 1722 Eye St., N. W., Ste. 200, Washington, DC 20006; (202) 457-8700.

ATE & Instrumentation West, January 9-11, 1990. Disneyland Hotel, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-3976 or (800) 223-7126.

SMART VI (Surface Mount and Advanced Related Technologies) Conference and Exhibition, January 15-18, 1990. Buena Vista Palace, Orlando-Lake Buena Vista, FL. EIA Components Group, 1722 Eye St., N. W., Ste. 300, Washington, DC 20006; (202) 457-4930.

Fifth Annual Battery Conference '90, January 16-18, 1990. California State University, Long Beach, CA. Julie Allison, Dept. of Electrical Engineering, California State University, Long Beach, 1250 Bellflower Blvd., Long Beach, CA 90840; (213) 985-4605.

Network Management Conference, January 24-26, 1990. Innisbrook Resort, Tarpon Springs, FL. Frost & Sullivan Inc., 106 Fulton St., New York, NY 10038-2786; (212) 233-1080.

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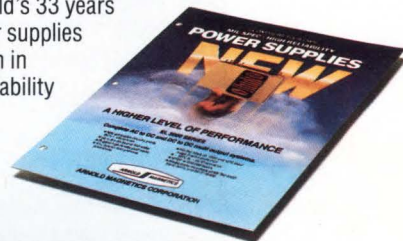
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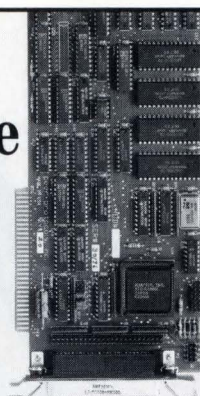
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CIRCLE 47



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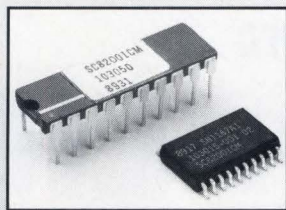


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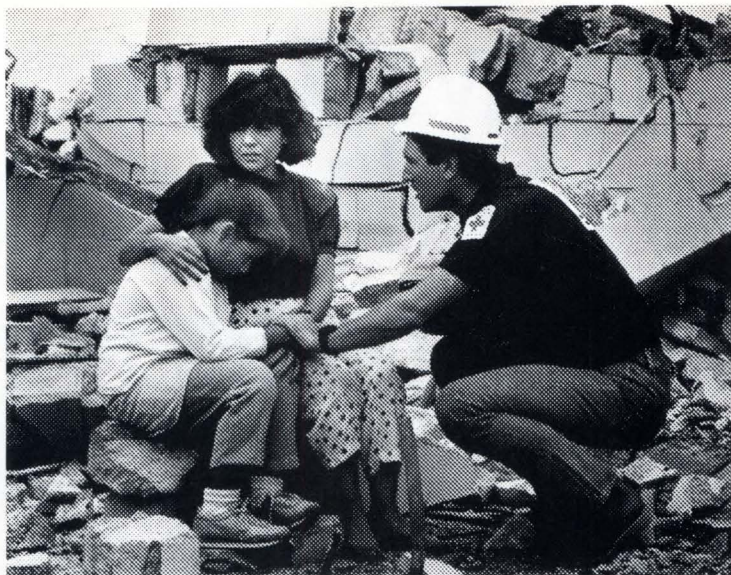
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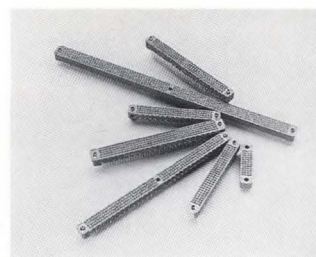
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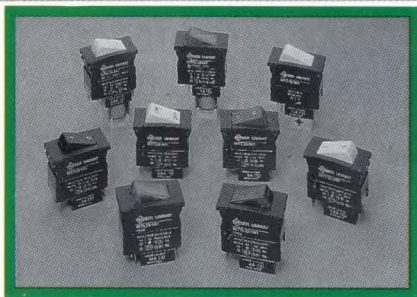
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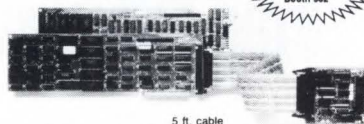
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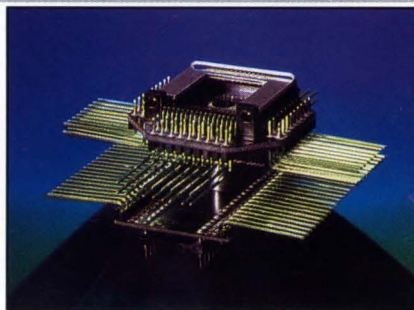
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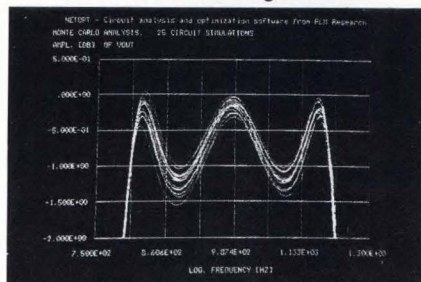
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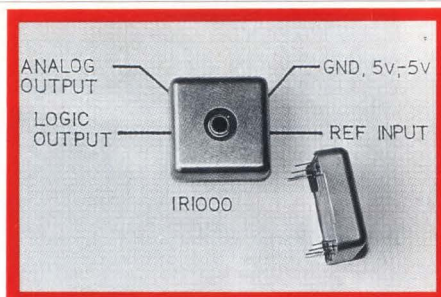
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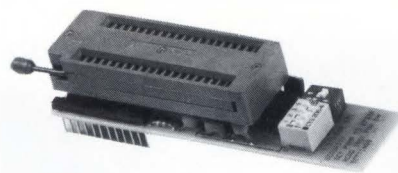
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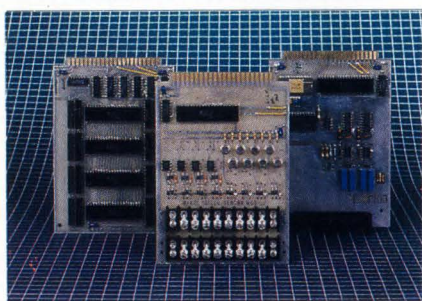
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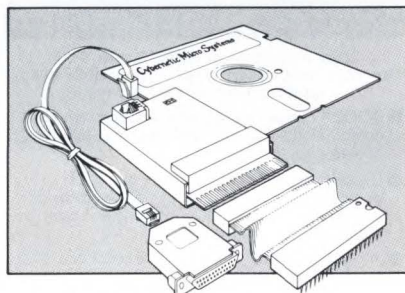
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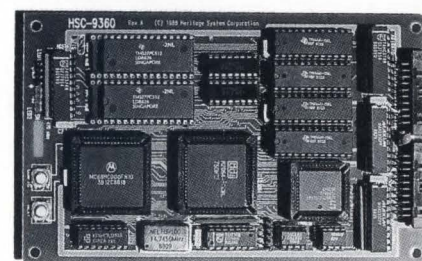
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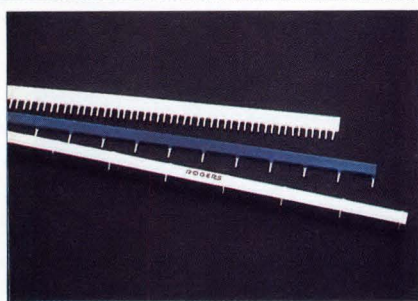
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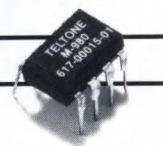
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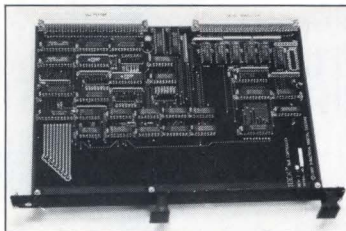
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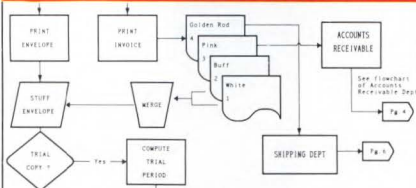
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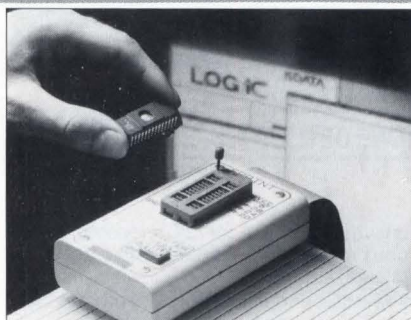
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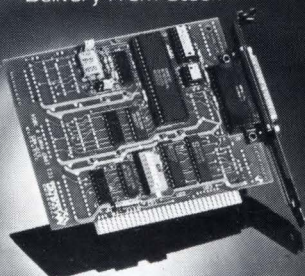
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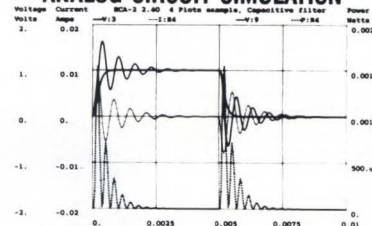
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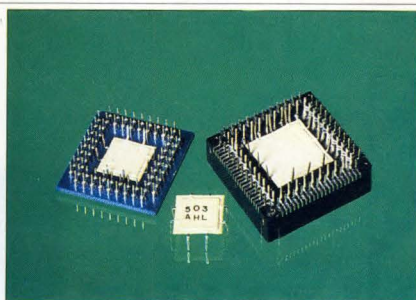
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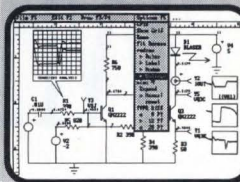
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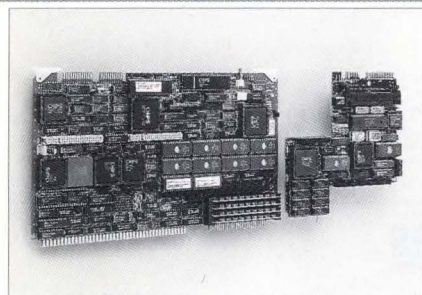
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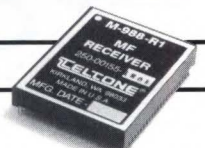
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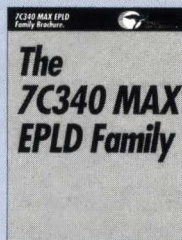
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