ELECTRONIC DESIGN

WAFER-SCALE MEMORIES FORGE 160-MBYTE SOLID-STATE DISK

SPECIAL REPORT: THE EMERGING OPTICAL-DISK DRIVE

A plot to get you to buy our Data Logger.

As if you didn't have enough reasons already.

Our Series 50 Data Logger is a fraction the size of most other data loggers. Considerably less expensive. Completely portable.

And now, as you can see, Series 50 not only gathers data, it explains it.

You can plot from one to sixteen variables at a time. Divide the width of the page into one, two or four segments, with multiple variables in each.

If conditions change, Series 50 can be programmed to change the plot with them. For instance, it can switch to higher resolution and time-stamp data with messages during alarm conditions. And it does all this on its own, no computer needed. (On the other

hand, it can also be controlled by a computer via IEEE-488 or RS-232.)

Series 50 will plot bar graphs next to numerical data. Create

min/max plots. Or generate x-y graphs from stored data.

Speaking of stored data, Series 50 can keep up to 100,000 readings in memory. Which is a good thing, because with four independent A/D converters and up to 260 channel scanning capacity, you could be gathering plenty of data.
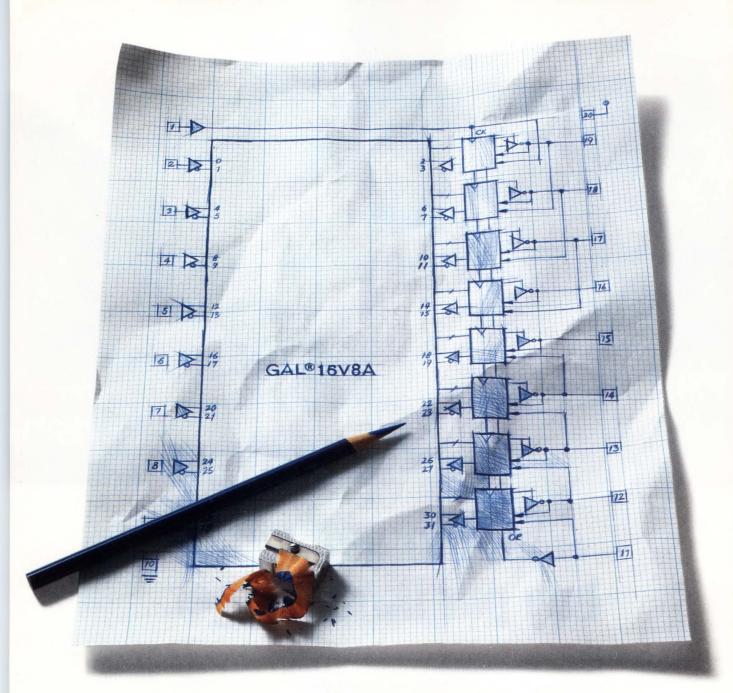
Data such as temperatures (6 thermocouple types and RTD's), AC/DC volts and current, resistance, frequency, time period, pulse width and more.

If our plot is working, you'd probably like to know more about the Series 50 Data Logger. Just phone (619) 279-2200. We'll be expecting your call.
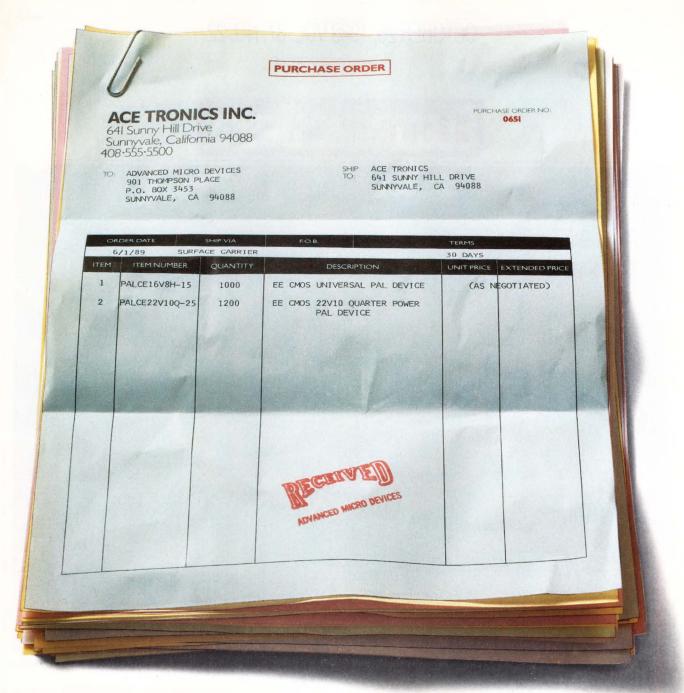
FOR LITERATURE CIRCLE 57

FOR DEMO CIRCLE 58

WAVETEK®

Universal CMOS PAL devices have always looked good on paper.

ELECTRONIC DESIGN

COMING NEXT ISSUE
• Special report on switching regulators
• First details on a high-speed GaAs chip set for high-speed serial communications
• Design optimized data flow for DSP imaging
• Avoid the pitfalls of high-speed logic design
• First details on an all-purpose logic/memory chip for microcontroller applications
• First details on a RISC-like 8-bit microcontroller that boosts system throughputs
• Comdex preview: What the semiconductor manufacturers will show
• Wescon preview: The technical program and important new products

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

Cover photo courtesy of Anamartic Inc.

Higher performance EMI filtering for high speed data lines

Coilcraft

All these ferrite beads can't equal the EMI suppression of a single Coilcraft Data Line Filter.

Our new DLFs are the most effective, low-cost way to eliminate common mode EMI from digital signals, logic level power lines, and inter-equipment cables.

Available in 8, 4, 3 and 2-line versions, Coilcraft DLFs provide >15 dB attenuation from 30 to 300 MHz. Up to 40 dB simply by adding capacitors!

Because they use a single magnetic structure to filter multiple lines, you get differential *and* common mode noise suppression, something other filters can't do.

Coilcraft Data Line Filters are easier to install and usually take less board space than beads or baluns. And they're far less expensive than filtered connectors–around 2¢ per dB per line.

For details on our complete line of Data Line Filters, circle the reader service number. Or call **800/322-2645** (in IL 312/639-6400).

Designer's Kit D101 contains 2,3,4 and 8-line filters. $65.

CIRCLE 63

1 1/8" Bead

5 1/8" Beads

Coilcraft DLF

-5dB
-10dB
-15dB
-20dB
-25dB

1MHz   10MHz   100MHz
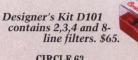
Attenuation
(50 Ohm System)

Coilcraft

1102 Silver Lake Road, Cary IL 60013

Your perceptions of power ICs are about to be shattered...

400 Volt

The times, they are a' changin'—Power Integrations

Simple to use.

Analog sensor application

Adds more value.

LED can indicate current thru load

More versatile.

Simple pulse width modulation

The PWR-DRV1 Universal Power Driver is an easy-to-implement, cost-effective interface between control electronics and high voltage loads such as displays, relays and solenoids.
- 200V, 300V, 400V versions
- 350mA
- $R_{DS(ON)}$ 5Ω

- Operates from rectified AC or DC power source
- Controlled by analog sensors, mechanical switches and digital logic (TTL or CMOS)
- On-board low voltage power for control circuitry
- Variable output (operates low voltage loads from high voltage, reduces power consumed by a load)
- Controls an AC load from a DC power source
- Measures current without external voltage drops

And the beat goes on...

Win an Epson portable Computer! Or a Casio Digital Diary! Or a Sony Watchman TV!

Now that you've read about the Power Driver 1. (See the previous three pages.) How about showing what you can do with it? Power Integrations, in cooperation with *Electronic Design*, is sponsoring a **Power Driver 1 Design Contest.**

Design Contest Prizes	
1st Prize:	Epson Equity portable computer with 20MB hard drive and 3.5" floppy.
2nd Prize:	A Casio 32K Digital Diary that stores up to 1500 names and phone numbers.
3rd thru 5th Prizes:	A Sony Watch Man TV
6th thru 10th Prizes:	Autographed copies of *Marketing High Technology, An Insider's View* by Bill Davidow

This is your chance to be innovative. We're looking for the most clever application of the PWR-DRV 1 Universal Driver.

Judging. Power Integrations will pick the ten best PWR-DRV 1 design applications and submit them to the editorial staff of *Electronic Design* for final judging. The top five entries will be announced in one of the March issues of this publication.

How to enter: Just call Power Integrations at 1-800-552-3155 for an entry form and free PWR-DRV 1 samples. Or write to us at 411 Clyde Avenue, Mountain View, CA 94043.

POWER INTEGRATIONS, INC.
The Power to Control

CAE Technology Report

Vol. 1, No. 7   October 1989

Users embrace the CAE tools in a big way

According to Frost and Sullivan (New York, NY), the CAE market is showing a strong performance in 1989 and will grow from $860 million in 1988 to $1060 million in 1989 and $2,450 million in 1993. The key factors contributing to this robust growth are significant improvement in price/performance, higher quality of software, better user interfaces and better integration of front-to-back design tools.

A new simulation standard has emerged on PCs

After several years of duplicated efforts, CAE vendors are finally going for the best overall solution and are porting to each other tools in a big way. This leads to CAE standards which further reinforces the growth of CAE tools. A prime example of such standardization is SUSIE* realtime logic simulator which is now either resold or recommended by almost every PC-based CAE vendor in the U.S., Japan and Europe, including P-CAD, Omation, Racal-Redac, Accel, Protel, Phase Three Logic, WACOM, Ultimate, etc., **Circle 101**

CAE tools - from hatred to love and affection

"Only two years back most simulator users were people who for one reason or another were forced into simulation and hated it," says Stanley Hyduke from ALDEC Company which makes the real-time SUSIE logic simulator. However, since the real-time simulators appeared and made all operations instant, designers are coming back to simulators and they are buying the most expensive versions according to Hyduke. The simulators have made a major comeback— from hatred to love and affection. **Circle 103**
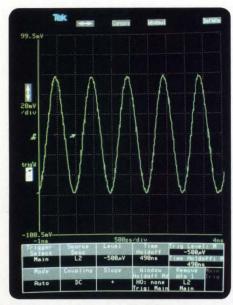
XILINX CAE tools are biggest seller

As the CAE tools are becoming more interactive and easier to use, they sell better. For example, SUSIE/PGA from ALDEC (805-499-6868) allows development of programmable gate arrays from XILINX and AMD in real time. The designer can instantly change and simulate new CLB block configurations, equations, etc. In addition, the user can imitate cell layouts. At $1,995, SUSIE/PGA which is fully compatible with XILINX tools, is the biggest seller for ALDEC. **Circle 104**
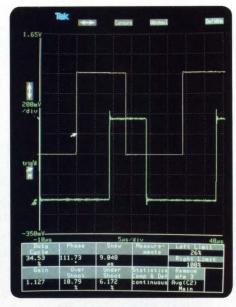
New generation of schematic capture tools may soon emerge

Schematic capture vendors have gathered with users on October 24, 1989 at a forum in San Jose, California to discuss new directions in schematic capture. With the introduction of real time simulation, there is nothing in the way to show simulation data while design is being drawn. The forum has confirmed that a new revolution in the schematic capture is in the offing. **Circle 105**

SUSIE IS A PRODUCT OF ALDEC COMPANY (805)499-6867, FAX (805) 498-7945

DEDUCTIONS

Examine fast signals in greater timing detail than ever before: the 11403 can window to 10 ps/div sweep rate in the zoom and pan mode.

Label waveforms with limitless versatility, to identify what each signal represents. Labels, plus automatic time and date stamps, are reproduced on all hard copy output.

Continuous statistics are automatically provided with each measurement, giving design and manufacturing a clearer picture of actual circuit performance as adjustments are made or as temperatures vary.

with automatic min, max, mean and standard deviation statistics for any measurement.

■ **Perform averaging, enveloping, and advanced mathematical transformations live, on-line, at a touch.**

Make the measurements you need on the waveforms you want—power or energy, for example—with no outside controller required to manipulate data.

■ **Ensure the kind of throughput and flexibility ATE needs,** with acquisition speeds of more than 2000 waveforms per second, on-board processing, plus plug-in modularity that lets you react quickly to changing needs.

All the high-performance features you expect, along with the sharpest color display in scopes, makes 11403 deductions not only brilliant, but easy to come by. To see more, including a free video introduction, contact your local Tek sales engineer, or call **1-800-426-2200.**

Tektronix
COMMITTED TO EXCELLENCE

CIRCLE 74

THINKING ABOUT U.S. MEMORIES

Unless you've spent the past several months on sabbatical in the Amazon rain forest, you must have heard about U.S. Memories, the proposed DRAM manufacturing consortium comprising Advanced Micro Devices, Digital Equipment, Hewlett-Packard, IBM, Intel, LSI Logic, and National Semiconductor. USM, which plans to bootstrap itself by using IBM's designs for 4- and 16-Mbit DRAMs, will raise $500 million as equity investment from its seven founders and other investors, and another $500 million in the form of loans. Though USM president Sanford L. Kane says he isn't asking the government to guarantee the $500 million in loans, there's no doubt that such guarantees would help the company immensely. However USM *is* looking for an exemption from antitrust laws.

T.J. Rodgers, president of Cypress Semiconductor, a manufacturer of CMOS static RAMs and other digital VLSI devices, is a major opponent of easing antitrust rules for USM. And the present method of private, venture-capital financing works just fine, he says. Moreover, he states that if IBM would license its DRAM technologies to Cypress in exchange for royalties, his company could be up and running and in production in short order.

Many important issues are involved here and we will try to address them in the future. For now, let's look at the intriguing possibility of a $500 million loan guarantee: The first thing that impresses us is that—post-1970 inflation notwithstanding—$500 million is still a lot of money. If the federal government guaranteed that much in loans, why not do it for *any* semiconductor company that demonstrates its production capabilities?

Few problems can be solved by just throwing money at them, but loan guarantees or reduced capital gains taxes will go a long way to help boost U.S. semiconductor manufacturing prowess. Chrysler Corp. received help because it was in the national interest to preserve this major U.S. vehicle manufacturer. A healthy U.S. semiconductor industry will have a far greater impact on national well-being in the 1990s and beyond.

Stephen E. Scrupski
Editor-in-Chief

Simple, practical, workable fiber optics.

Design is fun again.

Now AMP makes it easy to get your fiber optic designs up and running.

AMP engineering tackles the critical aspects of fiber optics at the component design and manufacturing stages. All our components—from board level to network level—take the hard work and guesswork out of working with fiber optics.

Our OPTIMATE Connectors and Data Links come down to a by-the-numbers data communications set. Our FSMA-style connector is the first of its type to qualify to MIL-C-83522. In fact, we offer the broadest line

OPTIMATE Data Links offer logic level compatibility, carrier sense, data quieting. In 850 and 1300 nanometer multimode, from 25 Mb/s to 220 Mb/s.

of fiber-optic connectors, cable, and components available anywhere. And because we're a connector company, we back that line up.

We're the only fiber optics supplier, for example, to provide you with dedicated field support. We play an active role in standards-setting groups like ANSI, IEEE, and

IEC, so we take compatibility and growth into consideration from the beginning. And we have the only commercial labs approved by DESC and IEC for qualification testing.

Whatever your interest in fiber technology, we have the expertise

and the commitment to help. In fact, we might even put a little fun back into the job.

For more information on AMP OPTIMATE products, call 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP **Interconnecting ideas**

THE CHALLENGE OF CONSUMER ELECTRONICS

It wasn't long ago that consumer electronics was viewed by many engineers as an unglamorous, "low-tech" niche. Designing a high-fidelity stereo amplifier was interesting, but not as challenging as, say, designing a hundreds-of-watts power supply that had to fit in a fist-size area in a space vehicle. Designing a TV was nowhere near as exciting as creating a tiny computer that could precisely guide an ICBM to its target thousands of miles away. The average consumer was somehow never equated in importance with the government as a customer.

ROGER ALLAN
EXECUTIVE EDITOR

While such leading-edge high-technology challenges still exist, mostly for government and military programs, the consumer-electronics sector is suddenly proving just as challenging—if not more so. It's one thing to design a product for military applications where dollars aren't a primary factor, but quite another thing to design that same product at the lowest possible costs.

To some extent, the military and space-age heyday of the 1960s and early 1970s fostered an atmosphere in which mediocre engineers survived. "Cost-plus" military contracts encouraged the hiring of more engineers at inflated salaries than really needed. If the final product didn't work properly and meet the specification, an elegant (though expensive) solution could be tried—and Uncle Sam would foot the bill.

But the tide is changing. More consumers are becoming the final customers, and they're proving to be a frugal bunch.
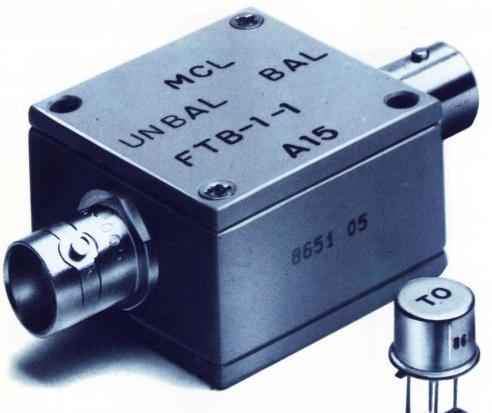
That circuit that you're designing may well wind up under the hood of a car for engine pollution control. It must operate as well in the frozen tundras of Alaska as it does in the boiling heat of the tropics. Moreover, it has to be "dirt cheap" and ultra-reliable.

To an automobile manufacturer using millions of such circuits, a cost difference of just a fraction of cent can be significant and can make the difference between a sale and no sale. It took semiconductor manufacturers of microprocessors several years to learn that hard lesson. Solid-state sensor manufacturers are fond of reciting how inexpensively they can mass-produce their chips on silicon wafers, but when the final product is packaged for harsh automotive or factory applications and signal conditioning is added, the price suddenly skyrockets. This cost is far too high for many automotive applications, which rely on tried and true mechanical or electromechanical solutions.

If you think that designing a computer keyboard to withstand harsh military environments is challenging, try creating the same product for a McDonalds or Burger King fast-food chain at a fraction of the military cost. And remember, that same keyboard must withstand the steady abuse of spilled coffee and soda, food greases, and the constant all-day pounding of human fingers and keep on working. These are the challenges that truly separate the men from the boys.

Consumer-electronics challenges are just beginning and there are many more to come. A few of the things to come to mind are high-definition TV, fiber-optic communications to homes and offices, the integrated services digital network (ISDN), smart homes, more sophisticated automotive electronics, "smart" power devices in consumer appliances, and direct-broadcast satellite TV. These applications will demand fresh thinking for advanced components and circuit designs, and will test the limits of engineering imagination. It will no longer suffice to ask "can we make it?" After all, technology has shown that we can make just about anything if enough time and money is put into it. The question of the future will be, "Can we make it quickly enough and at the right price?"

RF transformers

3 KHz-800 MHz
over 50 off-the-shelf models
from $2⁹⁵

Choose impedance ratios from 1:1 up to 36:1,
connector or pin versions (plastic or metal case built
to meet MIL-T-21038 and MIL-T-55631 requirements*).
Fast risetime and low droop for pulse applications;
up to 1000 M ohms (insulation resistance) and up to 1000V
(dielectric withstanding voltage). Available for
immediate delivery with one-year guarantee.

Call or write for 64-page catalog

*units are not QPL listed

TEK'S NEW PRISM 3000 FAMILY BREAKS THE LOGIC ANALYSIS BARRIER.

The new Prism 3000 Series is nothing less than a breakthrough in the evolution of logic analysis: once you see what it can do, you may scarcely imagine doing without it.

Now digital designers and integrators can start with all the speed, channels and memory depth they need—without tradeoffs. They can mix-and-match tools for their specific needs, including 8, 16 and 32-bit microprocessor debug modules brimming with features never before possible in a logic analyzer. They can add other modules, such as for high-speed timing and waveform analysis, later.

The new dimension of hardware/software integration.

Microprocessor control
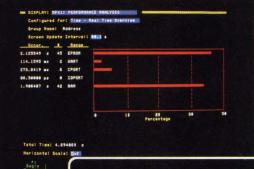
Real-time performance analysis

200 MHz timing

8K deep state analysis

Multiple microprocessor support

You can view 200 MHz timing and 8K of state data per channel, all time-correlated and integrated on the same display.

Observe data from multiple microprocessors or time-bases simultaneously. Set up

(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.

The Prism 3002P configuration features a slide-away keyboard and a 640x400 flat panel display that folds against the mainframe when not in use.

state and timing sections to cross-trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

Push beyond microprocessor observation into emulator-like microprocessor *control*.

With its unprecedented Prototype Debug Tool, Prism is the first logic analyzer to let you set breakpoints, patch registers and memory, restart

the system, and more —without an emulator's intrusiveness (or the long wait for new emulator availability).

Use real-time performance analysis to get a true, non-statistical view of system performance.

Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

Choose from a stand-alone version, expandable mainframe-and-monitor, even a portable model with fold-up flat panel screen.

Features like autoload, split-screen displays, smooth scrolling, automatic timestamping and on-line help notes make Prism refreshingly simple to learn and use.

Complete front panel controls are included on the Prism keyboard, enabling users to move easily from one Prism mainframe to another.

The clincher? You can step into this new generation of logic analyzers at prices starting at $8600.

Call 1-800-426-2200 for our free video demo and literature packet. Prism breaks so much new ground and offers so much to build on, you owe yourself a look. For a hands-on introduction, call your Tek sales engineer soon.

Tektronix
COMMITTED TO EXCELLENCE

SUPER FAST SRAMS, PRODUCTION PROVEN.

Available Now! 256K 25ns 64K 15ns/16K 15ns

When you work at the leading edge of technology, you need components that are production proven — not still in development.

At Micron Technology, we've applied the same state-of-the-art design and process technology used for our high quality DRAMs in development of our Fast Static RAMs. The result — an incredible 25ns 256K and 15ns 64K and 16K, plus a full line of other super fast parts. And we're not just sampling product, we've been shipping production volumes for over a year.

A wide variety of packages, densities and organizations are offered to meet all your application needs. And like all Micron memory products, our Fast SRAMs are backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.

So get the Super Fast SRAMs you need now by calling us at 1-208-386-3900.

Micron. Working to improve your memory.

Part #	Organization	Speed*	Packages
MT5C2561	256K X 1	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2564	64K X 4	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2565	64K X 4 $\overline{OE}$	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C6404	16K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 S.I/O	**15ns**	PDIP, CDIP, SOJ
MT5C6408	8K X 8	**15ns**	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C1604	4K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 S.I/O	**15ns**	PDIP, CDIP, SOJ
MT5C1608	2K X 8	**15ns**	PDIP, CDIP, SOJ

*Slower speeds also available.

MICRON

TECHNOLOGY, INC.

2805 E. Columbia Road, Boise, Idaho 83706 208-386-3900

CIRCLE 84

TECHNOLOGY NEWSLETTER

TO-92 CASE PACKS THREE-TERMINAL RAM A novel signal-control scheme squeezes a 256-bit low-power RAM into a low-cost plastic TO-92 package that has just three leads: power, ground, and signal. Developed by Dallas Semiconductor, Dallas, Texas, the highly multi-plexed signalling scheme combines the data, address, and control signals onto one pin. Consequently, a host processor needs only one I/O line to access the RAM's 256 locations. To multiplex all of those signals, designers developed an internal time-measurement system that encodes or decodes the digital signals by comparing pulse lengths. Designed with a low-power CMOS process, the RAM runs from a 1.5-V supply and consumes just 50 nA in its standby mode; 48 nanocoulombs when accessed. Consequently, a pea-size battery will power the RAM for over 10 years and permit over 1 million accesses. If a nonvolatile ID code is required, the RAM's first 32 bits can be factory programmed by laser to store a unique signature. Further-more, for more than 256 bits, an internal address-decoding capability makes it possible for up to four such RAMs to share the same signal line. And at just $0.25 each in large volume, the DS2222 EconoRAM becomes an attractive storage option. DB

HARDWIRING QUADRUPLES CPU THROUGHPUT By changing the CPU core of a 16-bit processor from a microcoded architec-ture to hardwiring, NEC Electronics Inc., Mountain View, Calif., boosted throughput 400% to produce a successor to its V40 and V50 processors. Avail-able soon, the CMOS processor will execute about 3 MIPS when running at 16 MHz. Replacing the microcoded structure with hardwired logic cuts the time to execute each instruction by eliminating instruction decoding. The new processor is totally software compatible with its predecessors. Furthermore, some of the peripheral I/O functions were expanded. For in-stance, the processor includes a four-channel DMA controller with a 24-bit address space, an interrupt controller, three timer-counters, a DRAM refresh circuit, a clock generator, a pro-grammable wait-state generator, and a serial I/O port. What's more, to minimize power consumption, three low-power modes were included: variable clock, which keeps the power to about 400 mW; standby, which cuts the power to about 200 mW; and stop, which cuts the power to 1 mW. DB

INTEGRATED CPU TACKLES TELECOM, DATACOM On-chip digital phase-locked loops for fast data synchronization are a key feature of a forthcoming, highly integrated 8-bit CMOS processor that can tackle high-speed telecommunications and data communications. With the ability to lock onto signals quickly, the processor communicates at synchronous rates to 7.1 Mbits/s when running from a 10-MHz clock. The HD68180S integrated processor, from Hita-chi America Ltd., Brisbane, Calif., starts with an improved version of the enhanced Z80 CPU core, which Hitachi put in the 64180 CPU and released over a year ago. The core is surrounded by a two-channel multiprotocol serial-communications subsystem that performs asynchro-nous and bit- or byte-synchronous data transfers. Both channels are full duplex. Moreover, one can handle any protocol, while the other is limited to asynchronous communications. The asynchronous-only port has a peak data rate of 4 Mbits/s. Additional support circuits include two channels of DMA control with a two-channel chained-block-transfer capability, dual 8-bit timers, multiple-input interrupt controller, and an MMU that can address 1 Mbyte of mem-ory. DB

GET CACHE PERFORMANCE WITHOUT THE EXPENSE Can a workstation perform as if it had a large, fast cache memory when in fact it doesn't? One machine from Hewlett-Packard Co., Cupertino, Calif., does by combining two-way interleaving, 64-bit-wide data transfers, intelli-gent paging algorithms, and an 80486 microprocessor exploiting its burst-mode transfer mode. The computer's custom DRAM control chip and private bus, which ties the memory card to host processor, tightly couples standard single-in-line memory modules (SIMMs) to the 80486. Though the memory card uses standard 36-bit wide 1-, 4-, or 8-Mbyte SIMMs, the private bus between the memory modules and the controller chip doubles the width to 72 bits. Conse-quently, the 160-lead controller chip can handle more data simultaneously, even though it has a 36-bit interface to the host processor. The tight coupling makes it possible for systems built with 80-ns DRAMs to execute programs as if the processor was running with an off-chip 64-kbyte cache of fast SRAMs. The Vectra 486 is also the first of HP's computers or workstations to incorporate the extended industry standard architecture (EISA) expansion bus. But it won't be HP's only such system: The company plans to offer its Apollo family of workstations as well as its RISC-based platforms with an EISA-bus option. DB

TECHNOLOGY NEWSLETTER

CAD FRAMEWORK LAB WORKS TOWARD STANDARDS

Many companies shun the latest CAD tools if they don't interface easily with their existing CAD machines. To smooth the interface, Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, has created a CAD Framework Laboratory (CFL) to support the standards proposed and adopted by the CAD Framework Initiative Inc., or CFI. CFI is an industry effort to promote standardized interfaces between CAD tools and support software. The CFL will be open for use by MCC shareholders and nonshareholders on two levels. Level-one affiliates will help to test and evaluate candidate framework standards proposed by the CFI. In addition, they will receive multiple copies of the software verification and validation (V/V) systems developed by the lab. Level-two affiliates can attend many of the meetings held by the lab, and will receive a single-machine copy of the V/V systems. For information, call Sandy Dochen at (512) 338-3545. LG

BIT-MAPPED COLOR GETS PERFORMANCE BOOST

A major problem with displaying color graphics is the enormous amount of data that a system must write: Eight bits must be sent to each screen pixel in a 256-color system. To address this problem, Tektronix has developed a proprietary CMOS gate array that optimizes bit-mapped color performance. Applied in the company's XD88/10 graphics workstation, the chip serves as an interface between the workstation's 32-bit system bus and the 256-bit pixel data bus that leads to the system's frame buffer. This buffer holds the pixel-by-pixel display information. Called Color≒Cache, the chip stores the colors being displayed—up to 32—so the processor can display them by sending just 1 bit of data, rather than the 8 bits originally needed. Consequently, the system transfers the colors eight times faster than it would without chip. RN

HP, AMD AGREE ON ICS FOR LAN STANDARDS

Chips for the emerging IEEE 802.3 10BASE-T standard for local-area networks will grow from a joint-development agreement between Advanced Micro Devices, Sunnyvale, Calif., and Hewlett-Packard Co., Palo Alto, Calif. The proposed Ethernet LAN uses existing twisted-pair telephone wiring to carry information at 10 Mbits/s among a mix of PCs and minicomputers. The agreement's first fruit will be an integrated multiport repeater, which combines the functions of 15 analog and digital ICs. The Am79C80 chip will put HP's Vectra PCs onto twisted-pair networks. DM

GENRAD GETS A TESTER THAT "REASONS"

A joint marketing agreement between GenRad Inc., Concord, Mass., and Cimflex Teknowledge Corp., Pittsburgh, Pa., gives GenRad the right to sell Cimflex's Electra, a system for diagnosing faults on analog and mixed-signal pc boards and hybrid circuits. Electra uses model-based reasoning, a form of artificial intelligence, to quickly and accurately diagnose the complex circuits. Essentially, Electra models the way that an experienced electrical engineer would troubleshoot the circuits, making the process much faster than conventional manual methods, according to Cimflex. The two companies are also working to incorporate the Electra software into GenRad's Genesis software for use with GenRad's GR2750 tester family. LC
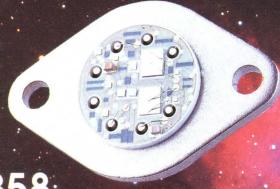
DEC JOINS MOTOROLA TO DESIGN FDDI CHIPS...

Momentum is building for chips that serve the Fiber Distributed Data Interface (FDDI) local-area network standard. A partnership between Digital Equipment Corp., Maynard, Mass., and Motorola's Microproccesor Products Group, Austin, Texas, has the two companies designing a chip set that implements the standard. FDDI pushes data-transfer rates to 100 Mbits/s for high-performance distributed computing, greatly improving on Ethernet's maximum of 10 Mbits/s. The technology exchange covers the design of an ANSI-compliant four-chip set, which will be manufactured and sold by Motorola in 1990. The affiliation puts Motorola in the FDDI component market for the first time. DEC is furnishing the technology for two chips. These have already been designed and implement the protocol portion of the standard. Motorola will supply clock recovery and system-interface circuits needed to complete the four-chip set. LC

...AND LETS AMD IN ON THE ACTION

Meanwhile, DEC and Advanced Micro Devices Inc., Sunnyvale, Calif., have reached an agreement that allows AMD to manufacture and market the same two DEC-designed FDDI devices that embody the core of the standard. AMD, which already markets its own FDDI chips, will use DEC's technology as part of a very-low-cost Supernet-3 family aimed at high-volume desktop computer applications. LC

ENHANCED MICRO CHANNEL MOVES 160 MBYTES/S

A potential eight-fold increase in the data transfer rate of IBM Corp.'s Micro Channel bus promises to accelerate desktop-system performance to workstation levels. The scheme, one of several unveiled last month by the Armonk, N.Y., company, boosts the bus transfer rate to 160 Mbytes/s by making the address bus bidirectional and concatenating it with the data bus for 64-bit data transfers.

To accomplish the fast transfers, IBM created two new operating modes (one for 32 bits and the other for 64 bits) called streaming data procedures (SDP). In the SDP modes, which double the bus' transfer rate, the address and initial data transfer take place at the bus' normal 200-ns rate. However, by assuming that subsequent data in the data block will be stored in sequential addresses, the sending device need not supply additional addresses. Therefore, after the first transfer, subsequent data words are sent over the address bus at a rate of one every 100 ns.

As a result, the 32-bit SDP mode transfers data over the 32-bit Micro Channel data bus at 40 Mbytes/s, twice the normal clock rate. In the 64-bit SDP mode, a bidirectional address bus is again linked to the data bus and, here too, only the first address need be sent. As a result, data is loaded eight bytes at a time on the double-width bus to yield an 80-Mbyte/s basic transfer rate.

Future extensions to the bus will achieve transfers of 50 ns/word or faster. When those bus improvements take place, the SDP modes will deliver 80 Mbytes/s and 160 Mbytes/s for the 32- and 64-bit modes, respectively.

Additional definitions and enhancements to the Micro Channel, such as a subsystem control-block architecture, data- and address-parity checking, and synchronous-channel checking, were also unveiled last month by IBM. Of importance to programmers, the subsystem control-block architecture defines a consistent software protocol through which bus masters may communicate and exchange data with, and independently from, the system's main processor.

With the subsystem control block, designers can have the Micro Channel bus serve as a local-area network within a system. The control block also gives a consistent method for bus masters to operate on a peer-to-peer basis.

The data- and address-parity features define additional fault detection capabilities to improve system reliability and data integrity. With synchronous channel checking, an administrator can isolate a fault to a particular card or device on a multiuser system and disable that device without interrupting the entire system.

To ease the development of bus master cards and subsystems, IBM struck a deal where Chips and Technologies Inc., San Jose, Calif., will develop a family of bus-master circuits that offers differing levels of capability. Full bus master chip specifications will be released by Chips and Technologies at the upcoming Comdex show from Nov. 13 to 17 in Las Vegas, Nev.

In addition, IBM will sponsor a series of technical seminars on the enhanced Micro Channel architecture, slated to start in the first quarter of 1990. Also, an updated version of IBM's Personal System/2 Hardware Interface Technical Reference manual will be available by year's end, and documentation on the subsystem control block architecture will be ready early next year. Contact the IBM publications hotline (800) 327-5711 or the IBM Technical Directory (800) 426-7282.

DAVE BURSKY

Micro Channel Data-Transfer Modes

32-bit basic data-transfer cycle - 20 Mbytes/s (existing)

	200 ns	200 ns	200 ns
Address bus	Address	Address	Address
Data bus	Data	Data	Data

32-bit streaming data-transfer cycle - 40 Mbytes/s (new)

	200 ns	100 ns	100 ns	100 ns	100 ns
Address bus	Address				
Data bus		Data	Data	Data	→

64-bit streaming data-transfer cycle - 80 Mbytes/s (new)

	200 ns	100 ns	100 ns	
Address bus	Address	Data	Data	Data	→
Data bus		Data	Data	Data	→

64-bit streaming data-transfer cycle - 160 Mbytes/s (new)

	100 ns	50 ns	50 ns	
Address bus	Address	Data	Data	Data	→
Data bus		Data	Data	Data	→

PACKAGING BREAKTHROUGH COULD DOUBLE COMPUTER PERFORMANCE, SHRINK CPU
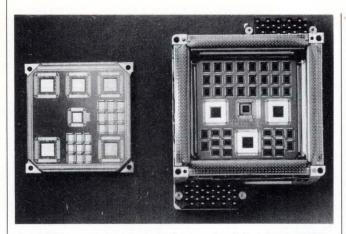
A new packaging technology developed over five years at Digital Equipment Corp., Maynard, Mass., will result in central processors with twice the performance of today's computers. The resulting circuit-package densities can be as much as 30 times greater than they are using conventional printed-circuit boards (see ELECTRONIC DESIGN, Oct. 12, p. 24).

DEC calls the concept Multi-Chip Packaging. Its fundamental difference from pc boards is reflected in a copper and polyimide vehicle, a metal-wafer based substrate with a layer of copper interconnections and polyimide insula-

tion. This arrangement is called the High-Density Signal Carrier (HDSC), and VLSI devices are mounted directly to it *(see the above figure, left)*. One 4-in.-by-4-in. HDSC holds as much logic as four 15-in.-by-12-in. circuit boards.

The resulting proximity of the chips shortens the distances that signals must travel. Consequently, the module overcomes one of the bottlenecks to greater mainframe or supercomputer performance: the propagation delays between packages that must be sufficiently spaced on a circuit board to prevent excessive heat from building up.

Each HDSC can hold as many as 72 VLSI devices, ranging from high-speed ECL gate arrays to fast static RAMs to DRAMs and other circuitry that typically form a CPU and memory. Two other elements round out the multichip packaging concept: a Multi-Chip Unit (MCU), each of which carries one HDSC and supplies physical and electrical connections to the HDSC *(see figure on right);* and a Planar Module—a mounting platform that interconnects multiple MCUs.

DEC's engineers estimate that the technique can double the performance of mainframe machines and supercomputers. To put their idea to work, they're applying it first in an as-yet-unannounced mainframe member of the VAX family.

The HDSC has nine layers for power and signal distribution, built up with alternating layers of a polyimide synthetic insulator and copper conductor. Copper is deposited onto the polyimide using sputtering and plating techniques and semiconductor-like photolithography. Connections between lines in layers above or below a given layer (vias) are made by masking the polyimide and etching a hole using a plasma etcher. The holes are filled when the next copper layer is deposited.

Signal and power interconnections are made as two separate cores. Then they're bonded together and connected, as needed, by drilling and plating through-holes between cores. Lasers cut sites for the semiconductor devices out of the HDSC, then epoxy bonding mounts the chips, and tape-automated bonding gang-solders signal and power pads to the HDSC.

The design yields a maximum power requirement of 300 W, an amount that is easily dissipated with air cooling. DEC points out that a competitive technique generates 900 W, which dictates a need for water cooling within a computer system.

After assembly, the HDSC is mounted into an MCU where signals are transferred from the HDSC to the underlying Planar Module by means of four flexible signal connectors (called a Signal Flex), each of which has more than 200 signal paths, for a total of 800 plus per MCU.
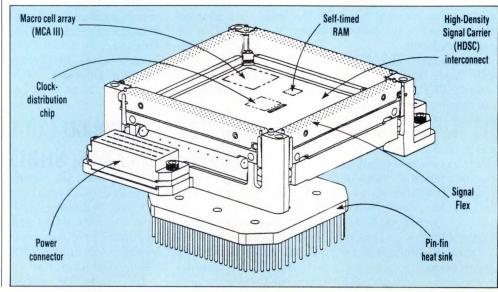
The MCU is inverted before gold bumps on the Signal Flex are mated to corresponding gold pads on the Planar Module. Separate cables attached through connectors at two sides of the HDSC power the MCU.

A copper heat spreader that's part of the MCU supplies a thermal path to a pin-fin heat sink to keep device junction temperatures at 85°C with air cooling. The MCU is the basic field replaceable unit in the design.

The Planar Module, as the platform for several MCUs, is DEC's counterpart to the pc board. The largest Planar Module to date is 25 in. by 25 in. and has 24 layers, as many as 18,200 component vias, and 17,650 buried vias.

The typical propagation delays for the MCU and Planar Module are 160 ps/in. and 170 ps/in., respectively. DEC's designers say that this compares with about 200 ps/in. for pc-board technology. Typical line widths on the HDSC are 15 μm, with spacing between lines typically 60 μm.

LARRY CURRAN

96-pin expansion card connector

(D_{0-15})

(A_{1-23})

(All of the 68000 lines plus clocks)

Interrupt switch

External video

Video board

To flat-panel display

Video RAM 32 Kbytes

RAM expansion connector

CPU MC68HC000 Interrupt inputs

Address bus

Data bus

RAM data bus buffers

RAM data

RAM 1 Mbyte

ROM expansion connector

D_{0-15}

ROM 256 Kbytes

Battery charger and power supply

Battery

Versatile interface adapter

Power manager (programmed microcontroller)

Apple desktop bus port

Keyboard processor

Keyboard and trackball connectors

SCSI

Internal hard disk

External SCSI port

SWIM disk control

Internal floppy disk

Internal floppy disk

External floppy disk

• • •

Serial communication control

Channel A

Channel B

Drivers and receivers

Port A (modem)

Port B (printer)

Serial ports

Modem connector

Apple sound chip

Sound

Sound

External audio port

Internal speaker

✳ = Custom Chips

CORRECTION: In our September 28 issue, on p. 28, we ran a story about the portable version of the Macintosh personal computer. The article made reference to a figure that was inadvertently omitted. We regret the error. Here, along with our apologies, is the missing Macintosh block diagram.

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Beyond VGA

IN THE ERA OF

MegaChip▫
TECHNOLOGIES

TIGA-340 from Texas
The open graphics interface standard a clear path for your future.

A ground swell of support is rallying behind TIGA-340™, the Texas Instruments Graphics Architecture. It and TI's TMS340 family are poised to become the next standard beyond VGA as PC users demand higher performance and resolution.
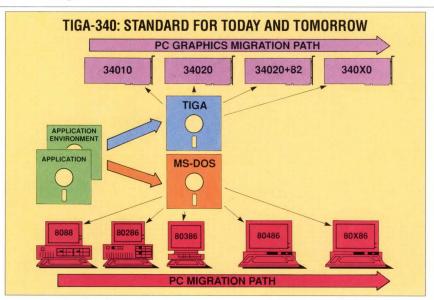
The PC graphics standard anyone can use

TIGA™ is a high-performance software interface that optimizes communications between industry-standard 340 family processors and the PC host processor.

With TIGA, hardware and software specifications for a PC graphics standard are open and available from inception — one of the reasons why more than 100 companies have already made plans to evaluate TIGA-compatible hardware and software products.

Lowest cost, highest performance

TIGA's move into the mainstream is being fueled by the price of TMS34010-based boards falling to well below $1,000. In fact, TI's 34010 processor is the most economical way to implement high-performance 1024 x 768 resolution PC graphics boards. The faster

TIGA-340: STANDARD FOR TODAY AND TOMORROW
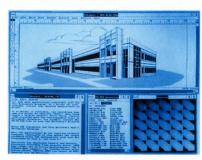
Just as **MS-DOS**® allows applications to run on any MS-DOS PC using 80X86 processors, TIGA allows graphics applications to run on any TIGA display system using a 340X0 processor.

speed and greater throughput of the second-generation 34020 result in even higher performance boards.

Clear migration path
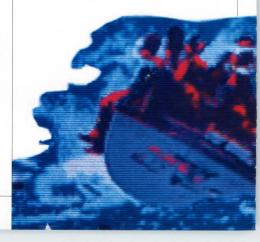
TIGA provides a common platform upon which graphics applications can take advantage of the processing power of the TMS340 family.

Software developers no longer have to rewrite code in order to migrate to higher performance hardware. Software applications

that run through TIGA on the 34010 processor run on the upward-compatible 34020 as well as on future 340 family members.

Hardware developers benefit from wide software support, reduced system development time and costs, and easy differentiation of products.

At present, TIGA supports DOS-based PCs, with UNIX™ and OS/2 forthcoming.

Instruments:
that defines

Applications portability

TIGA allows an application to be ported to a wide variety of 340-based graphics systems with a single software driver. Applications will run without modification regardless of resolution, color content, or specific 340 family processor.

For example, the Microsoft® Windows driver, which is part of the TIGA Software Porting Kit (*see next page*), allows Windows to run without any change on boards having resolutions from 640 x 480 to 4096 x 4096 and color content from monochrome to 256 colors or more.

Speeds time to market

Now hundreds of popular applications can be made available for your new graphics product almost instantly using TIGA and Microsoft Windows. Porting TIGA to a 340-based board typically takes less than one man-week of effort.

More than 150 OEMs have made the TMS340 graphics family their own. That wide acceptance, coupled with open architecture and a defined migration path, makes the future for TIGA-340 and the TMS340 family rich and promising.

TI's leadership TMS340 graphics family

No other supplier comes close to TI in the range of cost/performance options for the development of integrated graphics solutions. The widely used TMS34010 processor and other family members are now

being joined by a group of new-generation products that will bring the higher levels of workstation performance to PCs.

Chief among these is the TMS34020, a programmable, 32-bit processor up to 20 times faster than the 34010.

For use with the 34020, the TMS34082 will perform floating-point operations up to 100 times faster than current PC coprocessors. It is the industry's first graphics floating-point coprocessor.

The family's video RAMs, invented by TI, have been augmented by the TMS44C251 1-megabit VRAM. It was designed in conjunction with the 34020 for the high system bandwidths demanded by today's mid- and high-resolution graphics systems.

TIGA-340 DEVELOPMENT KITS

TMS340SPK-PC SOFTWARE PORTING KIT is for use by hardware developers to port the TIGA interface to any TMS340-based system.

TIGA SOURCE · MS-WINDOWS DRIVER
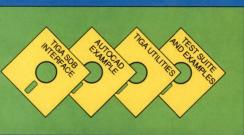
TMS340SDK-PC SOFTWARE DEVELOPER'S KIT is designed for those who want to develop direct 34010 code or downloadable extensions to TIGA.

C COMPILER · ASSEMBLER · MATH/GRAPHICS LIB. · BITMAP FONT LIB. · PC UTILITIES

TMS340DDK-PC DRIVER DEVELOPER'S KIT allows software developers to make existing software applications run on TIGA-compatible 340-based systems or develop new applications.

TIGA SDB INTERFACE · AUTOCAD EXAMPLE · TIGA UTILITIES · TEST SUITE AND EXAMPLES

Free user's guide

For more information about the TIGA-340 standard, get your free copy of the *TIGA-340 Interface User's Guide* and the *TIGA-340 Interface Brochure*.
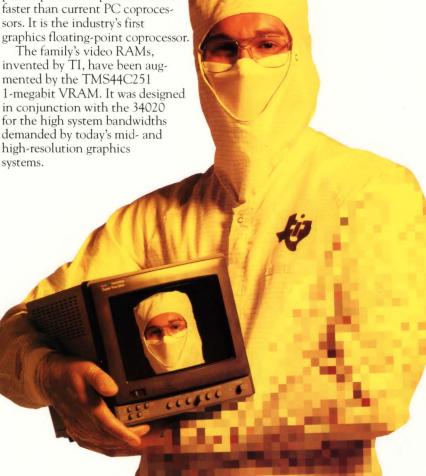
Call 1-800-336-5236, ext. 3526, or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.
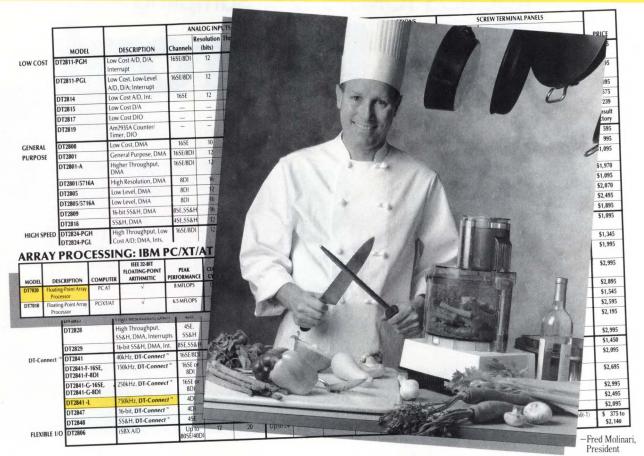
TI's MegaChip™ Technologies are the means by which we can help you and your company get to market faster with better, more competitive products. Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers.

™ TIGA-340, TIGA, and MegaChip are trademarks of Texas Instruments Incorporated. UNIX is a trademark of AT&T Bell Laboratories, Inc.
® Microsoft and MS-DOS are registered trademarks of Microsoft Corporation.
© 1989 TI   08-9254

TEXAS INSTRUMENTS

If you hunger for faster data acquisition and processing, here's the recipe...in real time.

The DT2841 and DT7020. 750kHz throughput. 32-bit floating point processing. Data acquisition has never been faster.

If PC AT® throughput bottlenecks are frustrating you, Data Translation has the answer. Our external interface, DT-Connect,™ surmounts the historically slow AT bus to deliver much faster data acquisition and array processing.

This is the answer for high-speed DSP operations such as filters and FFTs. It features A/D, D/A, DIO, and a Timer/Counter ... plus, MACH™ Subroutine Libraries that support most programming languages.

At last. High-speed data acquisition and high-speed computation power.

Together. In one tasty package.

FREE 1989 Data Acquisition Handbook.

OVER NIGHT DELIVERY

Call (508) 481-3700
In Canada, call (800) 268-0427

DATA TRANSLATION®

CIRCLE 62

ADC603 10MSPS 12-Bit Sampling ADC
Out In Front

ADC603KH

Brand Z

Brand Y

Brand X

Industry's Best Spurious Free Range - 74dBc @ 10MHz

INPUT FREQ   4.93MHz(-0.5dB)
SAMPLING FREQ 10.00MHz

Magnitude (dB)

0.0
-20.0
-40.0
-60.0
-80.0
-100.0
-120.0

0.0   1.25   2.50   3.75   5.0

Frequency - MHz

Burr-Brown invented the first IC 10MSPS, 12-bit A/D converter. And today, the ADC603 is still out in front with the best guaranteed dynamic performance, the best price, and the best delivery in the industry.

Out Front in Dynamic Performance

ADC603 achieves the best spurious-free dynamic range by minimizing noise and distortion. Laser-trimming and an efficient design ensure its ability to meet stringent distortion, accuracy, and linearity specs.

It's a complete, sub-ranging ADC subsystem with sample/hold amplifier, ADC, precision voltage reference, digital error corrector and timing controller, all in a compact 46-pin DIP. Two temperature ranges, plus a military version, are available.

And Burr-Brown offers more guaranteed performance specs for both high and standard grades than anybody else.

100% TESTED SPECIFICATIONS
(at 10MHz sample, 5MHz input)

	ADC603 K Grade 25°C	ADC603 K Grade Over Temp	ADC603 J Grade 25°C	ADC603 J Grade Over Temp
IMD, max (8MHz Sample)	-71dBc	-68dBc	-67dBc	-64dBc
SINAD, min	62dB	61dB	60dB	57dB
Spurious Free Dynamic Range, max	-66dBc	-65dBc	-63dBc	-60dBc
THD, max	-64dBc	-62dBc	-61dBc	-58dBc
SNR, min	66dB	64dB	63dB	60dB
Price*	$941.00		$590.00	

Out Front in Fast Delivery

ADC603's delivery is also out in front. All grades are available off-the-shelf. Whether you need one or hundreds, Burr-Brown will meet your most demanding delivery schedules.

Out Front with Lowest Price

Efficient production allows Burr-Brown to pass their manufacturing economies along to you through new lower prices. Burr-Brown also adds value with superior technical support and assistance in applying, testing and integrating advanced ADC603 solutions.

ADC603 can help keep your designs "out in front" of the competition, too. Contact your local sales office for comprehensive data sheets, samples and evaluation tools, or for immediate assistance call **1-800-548-6132.**

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734
*USA OEM prices in 100s.

BURR-BROWN®
BB

IC Fabrication Techniques Sculpt Silicon Sensors

Advanced Sensor Designs Integrate Movable Silicon Structures With Circuit Elements.

Milt Leonard
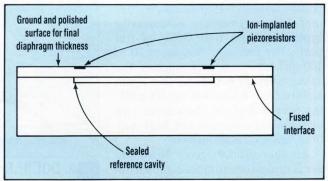
Over the past few decades, the high-volume price of microprocessors has dropped below the cost of sensors that can interface the processor to the analog world of pressure, temperature, acceleration, flow, velocity, and other physical variables. As a result, real-time control applications for microprocessors—particularly in high-volume consumer applications—was stymied by the lack of inexpensive, digitally compatible sensors. However, several devices described at the Sensors Expo International, held recently in Cleveland, Ohio, and Anaheim, Calif., indicate a growing trend toward fabricating micromachined sensors on silicon wafers to get the economies of high-volume production. IC production techniques are producing silicon sensor chips that integrate moving structures with resistive Wheatstone bridges, laser-trimmable resistor networks for calibration, and even signal-processing circuits.

Selling prices depend on sensor complexity. The cost of a micromachined silicon chip ranges from $1 to $2 as a high-volume commodity product up to $100 for a high-performance die in low volume. A packaged die with or without basic compensation and normalization can cost $2 to $4 in volume, and up to $100 for more complex chips in low volume. The addition of compensation, calibration, and signal conditioning raises the volume selling-price range from $10 to several hundred dollars, and a packaged sensor containing digital signal processing can run $30 to $1500. Such sensors typically include temperature compensation, calibration, self diagnostics, and remote communication and control capabilities.

Micromachined silicon has several advantages for use in sensors. Especially important for sensor applications, silicon has no mechanical hysteresis and is highly sensitive to mechanical stress. Its modulus of elasticity is the same as steel, and tensile yield strength is higher than steel. Silicon is also as hard as quartz and is lower in density than aluminum. Perhaps most important of all, though, silicon sensors with tightly controlled submicron geometries can be built and packaged with the same mature processes, equipment,

1. HIGH-TEMPERATURE fusion bonding creates a two-layer absolute pressure sensor from NovaSensor made of silicon. The base with a pre-etched reference cavity is joined through a crystal boundary to a pressure-sensing silicon diaphragm containing ion-implanted piezoresistors.

and ultrapure materials used for high-volume production of integrated circuits.
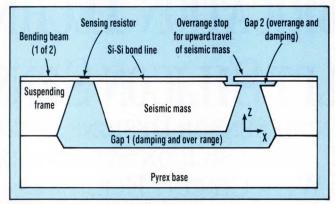
The simplest micromachined silicon structures are found in pressure sensors, which often require just a few IC processing steps. For example, in a vacuum-referenced absolute pressure sensor by NovaSensor, Fremont, Calif., a 10-μm deep cavity is formed in the silicon substrate by an isotropic etching or by plasma or wet isotropic etching *(Fig. 1)*. Then the top wafer is fusion bonded to the substrate at a temperature exceeding 900° C. Air is evacuated from the circular chamber during this step to form an absolute pressure sensor.

The next step is polishing, grinding, or etching the top wafer to a 170-μm thickness to form the pressure-sensing diaphragm. Finally, conventional IC processing is used to pattern the piezoresistive sensing elements, contact holes, and evaporated-metal interconnect lines. To form a gage or differential pressure sensor, a hole can be etched through the backside to provide pressure access to the cavity.
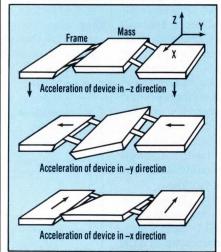
NovaSensor uses this basic process to make a variety of sensors, including a high-pressure (5000 psi full-scale) sensor chip measuring 2.5-mm square. Pressure nonlinearity typically is less than 0.05% of full scale. For pressure ranges of 50 to 100 psi, the company applies the same fabrication process to a 1-mm square chip. With a 4-in. wafer yielding over 6000 chips, the sensor is an economical solution for high-volume, low-cost applications.

Another product from NovaSensor is typical of the more complex micromachined silicon structures required for making accelerometers. These devices are used as crash sensors for air-bag deployment, motion sensors for active suspension systems, and in aerospace and military applications. The sensor is a cantilever design with one end of a beam

2. A SINGLE CANTILEVER for a NovaSensor accelerometer uses two layers of fusion-bonded silicon and a glass base. Plasma etching and programmed etch stopping creates a cross section with air gaps for damping. Interdigitated tabs on three sides of the mass offer overrange protection.

fixed and the other attached to a free-swinging seismic mass *(Fig. 2)*. A series of interdigitated flexible tabs extending over underlying shelves around three sides of the seismic mass supply mechanical stops to prevent beam breakage during overranging in all three axes of motion. Gaps formed between the two silicon layers and the glass base provide air damping to prevent overrange damage from resonant oscilla-

3. DOUBLE-CANTILEVERED accelerometers have less sensitivity than single-cantilever types but are more rugged and less prone to error caused by lateral-motion components. The 3201 from IC Sensors is a three-layer silicon IC with a seismic mass supported by four flexible silicon hinges. Each flexure has a piezoresistor implanted on each surface.

tions. With the top side of the chip completely exposed, metal lines, laser-trimmable resistor networks, and bonding pads can be added to the chip surface for specific applications.

The finished chip measures about 3.3-mm square and is 1.5-mm thick. Critical damping and overdamping have been demonstrated with roll-off frequencies of 500 Hz and higher, and the device survives shocks exceeding 1000 G in all axes. Cross-axis sensitivity typically is under 2% in any axis. These sensor chips are packaged in TO-5 and -8 cans and on hybrid circuit boards.

For a given chip size, single-cantilever accelerometers have more sensitivity than double-cantilever designs. However, accelerometers with a double-cantilevered seismic mass are mechanically stronger. The model 3021 accelerometer by IC Sensors, Milpitas, Calif., is an example of the double-cantilevered approach. The device consists of three layers of silicon, with center layer containing the proof mass suspended from a silicon frame by four silicon flexures *(Fig. 3)*. Each flexure contains a diffused piezoresistive element on each of its two surfaces. Shallow depressions etched into the two outside layers allow the seismic mass to move, protect against over-acceleration, and provide viscous air damping.

As acceleration deflects the mass vertically, each flexure bends, applying tension on one of its resistors and compression on the other. Connecting the eight sensing resistors in a Wheatstone bridge supplies a signal proportional to the acceleration of the seismic mass. The center of mass of the seismic element is below the support plane. So when accelerations in the x- or y-plane cause the mass to tilt or rock, appropriate cross-coupling of the sensing resistors cancel out undesirable off-axis responses to less than 1% of the z-axis response.

Adding an electrode to the inside surface of the top layer of the sensor gives a field self-test capability for verifying that the moving structures are intact and functional. The test is performed by applying a voltage to this electrode, which causes electrostatic attraction to exert a force on the seismic mass, and monitoring the device output for the correct response. This procedure can also be used for continuous device calibration. With a constant-deflection-voltage amplitude and mass-to-electrode spacing, the force on the mass is equivalent to a specific acceleration, regardless of changes in temperature or characteristics of the piezoresistors. Therefore a normalized acceleration can be obtained by alternately sampling the outputs from actual acceleration and acceleration plus the electrostatic equivalent during device operation. The normalized result is practically independent of temperature.

To combine shock survivability with optimum signal-to-noise-ratio, a transducer design by Endevco, San Juan Capistrano, Calif., combines a monolithic silicon sensor and signal-conditioning circuits in a hybrid microelectronics package. Developed under contract for Sandia National Laboratory, Albuquerque, the 1-mm square, one-piece silicon sensor includes the entire spring, mass, and four-arm piezoresistive strain-gage assembly configured in a bridge circuit.

The structure is made of single-crystal silicon using anisotropic etching and microelectronic fabrication techniques. After a pattern of dopant defines the strain gages on the chip, two pairs of etched channels create a seismic mass on each side of the chip. The central fixed part of the chip is then mounted on a pedestal, which allows the seismic masses to move freely in the vertical direction. This assembly is epoxied to an alumina substrate, which also carries a two-pole low-pass filter, a gain stage, and a line driver. The filter prevents saturation in the following stages in case of sensor resonance. A 30X gain stage following the filter increases the transducer's signal-to-noise ratio.
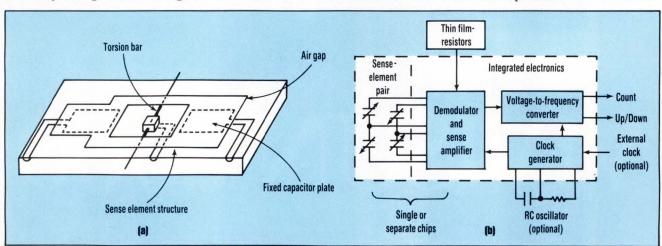
Housed in a 1/2-in. hexagonal stainless-steel case 0.3-in. high, uncalibrated low-output (0.1 mV/G) prototypes have survived 100,000-G shock levels. Uncalibrated high-output (1.0 mV/G) versions were tested for 15,000-G shocks. The transducer runs on +5 Vdc, has a dc to 30 kHz frequency response, and exhibits an off-axis sensitivity of under 5%.

A logical extension of present silicon sensor technology would be integrating signal-conditioning circuitry and sensor structures on the same chip. This is the approach of Silicon Designs Inc., Issaquah, Wash. The company developed a capacitive accelerometer that combines the sensor, demodulator, sense amplifier, and voltage-to-frequency converter on a silicon die. Thin-film resistors, built on a separate substrate, are used for sensor calibration and to compensate for bias and scale factor errors of the sensing elements.

Unlike piezoelectric designs, capacitive accelerometers are relatively insensitive to temperature and can be used over a wide temperature range without the need for expensive compensation and calibration mechanisms. However, they haven't been used in low-cost applications because of the requirement for complex and costly measurement circuitry. The Silicon Designs' device has sense element structures suitable for batch processing on the IC's surface.

SUSPENDED METAL PLATES

The sensing element consists of a metal plate supported above the substrate surface by two torsion bars mounted on a pedestal (*Fig. 4a*). Forming a common connection to two variable capacitors, the plate is free to rotate around the torsion bar axis. The two fixed capacitor plates are built on the surface of the substrate to form sense-element capacitances of several tenths of a picofarad. Because the axis of the plate is offset from that of the torsion bar, an acceleration causes the plate to rotate about the torsion bar axis to increase capacitance on one side and

Torsion bar · Air gap · Sense element structure · Fixed capacitor plate

(a)

Thin film-resistors · Sense-element pair · Integrated electronics · Demodulator and sense amplifier · Voltage-to-frequency converter · Clock generator · Count · Up/Down · External clock (optional) · RC oscillator (optional)

Single or separate chips

(b)

4. THE BASIC CAPACITIVE SENSE ELEMENT of an accelerometer from Silicon Designs, a rotatable metal bar located between two metal plates, is made with electroplating and chemical etching processes (a). CMOS circuitry located on the same chip convert capacitance changes into a pulse stream whose frequency is proportional to acceleration (b).

Time To Market

Time to market... the span between inspiration and product introduction. You want the shortest path to a successful product launch — but all too often the system power supply becomes a stumbling block . . . development delays, safety agency approvals, EMI/RFI testing, size problems, cooling issues, cost overruns, last minute changes in power requirements, manufacturing disasters...no matter how innovative your product, you know that your customer's satisfaction — and your market opportunity — may ultimately hinge on how well your "custom" power system holds up.

FlatPAC takes the uncertainty out of power development by offering unprecedented flexibility along with instant availability...in a fraction of the space required by conventional switchers. You define your requirements...output power from 50 to 600 Watts; one to three outputs; output voltages from 2 to 95 Volts...we combine our high power-density converters with modular package and front-end assemblies to configure a FlatPAC specific to your needs. You benefit from the proven field performance and inherently high reliability of our component-level power converters, without sacrificing features: UL/CSA/TUV recognition, 110/220 VAC input, surge limiting, Class A EMI/RFI, OVP, overcurrent protection, all outputs totally isolated and trimmable, sequenced AC and DC status signals...and more.

Vicor believes that power should be the least of your problems. Let us show you how FlatPAC can help you win the race to market.
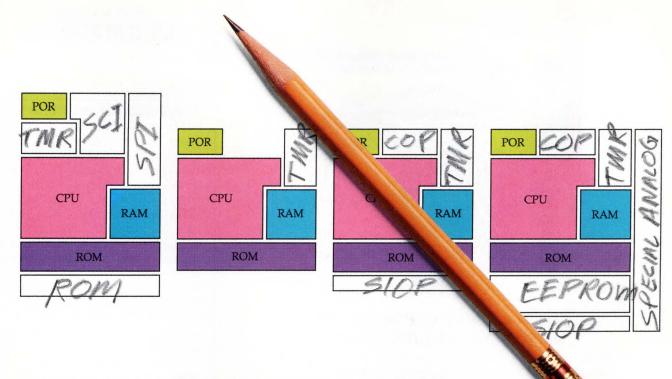
1-800-735-6200

Component Solutions For Your Power System
23 Frontage Road, Andover, MA 01810

VICOR

CIRCLE 85

FILL IN THE BLANKS.

SILICON SENSORS

decrease capacitance on the other.

The 40×25-mil sense elements are made by electroplating the metal plates onto a conductive substrate through a patterned photoresist layer. After the photoresist is stripped, the remaining metal pattern is determined by open areas of the photoresist. The suspended sense elements are built partially on top of a sacrificial spacer material, which is deposited prior to electroplating. Chemically removing this material leaves the sense element supported only where it is formed directly on the substrate surface. Built-in air damping gives an overdamped response for accelerations up to about 20,000 G full scale.

The single-chip accelerometer contains two sense elements connected in a fully active bridge circuit. On-chip electronic circuits, built in 3-mm CMOS, convert capacitance changes into a digital pulse stream whose frequency is proportional to acceleration *(Fig. 4b)*. Output frequency varies from 0 to 250 kHz. The digital pulse stream output can be connected to a microprocessor with an internal digital counter, such as the Intel 8051. Another output, derived from the count output, can drive an up-down counter or be filtered for low-to-medium frequency applications.

Package options include standard DIPs, ceramic leaded and leadless chip carriers, and metal packages with glass-to-metal seals. The circuits operate over the full military range of –55 to +125° C and run on 5 V and 1 mA. Measurement circuits can be customized for specific applications. The company says that a complete subsystem with the accelerometer and 10,000 transistors on the same chip for high-volume applications would cost under $5 each, not including nonrecurring development charges. Silicon Designs can also integrate the same circuits with other capacitive sensors to measure pressure, humidity and strain.□

How Valuable?	Circle
Highly	532
Moderately	533
Slightly	534

One chip footprint.
Six datacom solutions.

Pin-out and software compatibility between key SGS-THOMSON devices now enables you to develop datacom products in less time and at dramatically lower costs. In fact, your investment is essentially reduced to one hardware and software design effort that economically expands to six different datacom applications.
WAN: X.25, High-Speed HDLC, ISDN LAPD and CCS#7.

In addition to X.25 LAPB, SGS-THOMSON's high-speed MK5025 Link Level Controller delivers economical full duplex, fully transparent HDLC/SDLC for specialized protocols. On-chip firmware even permits performance of the Link Access Procedure for the ISDN D channel (LAPD) at speeds beyond anything available from a software-only approach.

The MK5027, a firmware derivative of the MK5025, offers complete Level 2 implementation of CCS#7 (Common Channel Signalling System #7), saving you months of software development.

Plus, the MK5027 is pin-out and software compatible with SGS-THOMSON Ethernet and X.25 controllers.
LAN: Ethernet, Cheapernet and StarLAN.

The MK5032 VLANCE controller extends the capabilities of an IEEE 802.3 network such as Ethernet, Cheapernet or StarLAN. In addition, SGS-THOMSON's MK5032 and MK68592 Manchester encoder/decoder are the only Ethernet devices second sourced by a major manufacturer.

Combine the MK5032 with our CMOS MK5030 hub and a compatible Manchester encoder/decoder like the MK50351, and you have a complete, low-cost StarLAN solution that includes automatic compensation for twisted pair wire reversal.
Multiple protocol serial controllers.

One product line covers the spectrum of SCC requirements. For example, the 7 Mbps MK5025 with on-chip DMA offers complete HDLC, X.25 LAPB, ISDN LAPD, X.32 and X.75

Link Level Protocol compatibility.

The full duplex, dual channel MK68564 satisfies numerous 68000 Series datacom applications.
Designed with your future in mind.

With one common footprint among key devices, no other manufacturer enables you to cover so many LAN, WAN and SCC markets as fast or as economically as SGS-THOMSON. We have the product compatibility to put you ahead of the competition right now — and keep you ahead.

For a complete guide to today's and tomorrow's most advanced data communication solutions, contact SGS-THOMSON Microelectronics, 1000 E. Bell Road, Phoenix, AZ 85022. Phone 602/867-6259.

SGS-THOMSON
MICROELECTRONICS

ELUSIVE SOLID-STATE MEMORY CONCEPT
COMES TO FRUITION IN 160-MBYTE
STORAGE MODULE USING 6-IN. WAFERS.

WAFER-SCALE INTEGRATION ARRIVES IN "DISK" FORM

LAWRENCE CURRAN
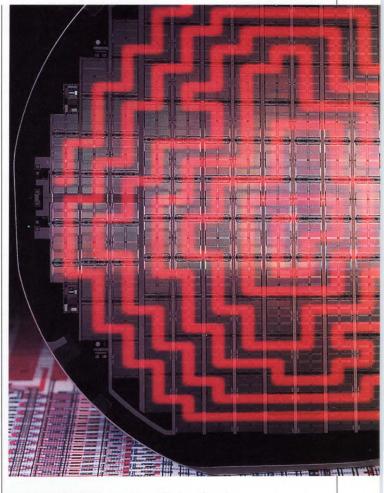
A dream that has tantalized system designers for more than 20 years—the use of full uncut wafers instead of diced and packaged semiconductor devices as logic or memory—has reached commercial reality. Hailing from Anamartic Ltd., a British firm, Wafer Stack is a solid-state storage subsystem that takes the place of conventional rotating disk drives in a computer system.

Wafer Stack enables computer system designers to realize extremely fast access times compared to conventional disk drives—an average of 200 μs with Anamartic's proprietary native-mode interface, or less than 1 ms using a SCSI interface. That's an improvement of about 200 times compared to rotating disk drives with their typical 20-ms SCSI access times.

Such a boost makes the Wafer Stack attractive for use in various computers, especially high-speed on-line transaction-processing (OLTP) systems used in banking, insurance, manufacturing, and communications applications. Those systems make frequent accesses to short blocks in a database. In fact, one of the companies that invested in Anamartic is Tandem Computers Inc., the $1.3-billion Cupertino, Calif. manufacturer of OLTP computers. Tandem is evaluating the Wafer Stack, with an eye toward having it in the product line within 18 months, according to Larry Laurich, Tandem's vice president for engineering. He reports that Tandem is

very excited about the Wafer Stack based on early results to date. "Our team is writing to and reading from devices in the lab, and is knocking off benchmarks on schedule," Laurich says.

The Wafer Stack fills the gap between ever-faster semiconductor main memory and slower disk drives, a bottleneck that has existed for the last two

decades. It cracks that bottleneck because of its inherent zero-latency performance, resulting in extremely fast access times and sustained transfer rates ranging from 1.6 Mbytes/s for a native-mode interface to 3 Mbytes/s for a SCSI interface. Conventional disk drives offer similar sustained transfer rates, but it's in the access times that the Wafer Stack shines.

The Wafer Stack uses two 6-in.-diameter wafers to form one module containing 40 Mbytes of storage in 1-Mbit CMOS dynamic RAMs (DRAMs) *(Fig. 1)*. As many as four such modules can be stacked atop one another to supply a maximum of 160 Mbytes of storage. A wafer controller board is also required to manage data storage and transfer, error correction, and "scrubbing" on the wafers.
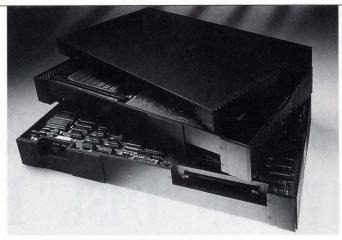
John Scandalios, vice president for marketing at Anamartic, explains that scrubbing assures that any memory cells developing random errors are purged and replaced, even if they occur long after the system was working at a customer site. One controller can handle from one to four modules, with the entire stack based on the form factor of an 8-in. disk drive—8.5-in. wide by 5-in. high by 15-in. deep.

The standard Anamartic native-mode interface can be augmented by a SCSI or another interface added by a buyer—an OEM or end user. When connected to a host computer through a SCSI interface, the Wafer Stack emulates a disk drive.

Although the Wafer Stack fits into the same footprint as a conventional 8-in. Winchester disk drive, the similarity ends there. Anamartic's considerable contribution comes inside the box housing the Wafer Stack. Where other solid-state disks use individual memory

1. TWO WAFERS FACE EACH OTHER in a clamshell-like arrangement to form a 40-Mbyte storage module in Anamartic's Wafer Stack.

chips wired to a pc board, Anamartic's wafers are mounted to a carrier intact. Using the full wafer eliminates several processing steps, including as much as 90% of the costly wiring and soldering, which can reduce wafer yield.

There are 202 dice per wafer, which is more than necessary to obtain 20 Mbytes of data per wafer. The additional devices are included to allow for the loss of device portions that test out as flawed, and to supply spares to replace those failed elements. In addition to containing a 1-Mbit DRAM, each die also carries additional programmable configuration logic, which Anamartic calls Conlog, to connect each Conlog ele-

ment to its four neighboring dice to the north, east, south, and west over signal lines that form logic networks on the wafer *(Fig. 2)*.

Using proprietary software, an external controller tests each die, then programs the Conlog elements to interconnect the good dice into one continuous bidirectional data path. The path takes the form of a spiral, running counterclockwise from the wafer's edge to the center *(Fig. 3)*. Portions of bad dice, but not the entire DRAM, are routed out of the spiral by the software. Anamartic partitions each DRAM into 32 tiles of 32,000 bits each, so that only a failed tile is discarded. In conventional practice, if just one bit of a 1-Mbit DRAM is flawed, the entire device has to be scrapped.

PROM HOLDS MAP

Each wafer-carrier board holds a CMOS flash PROM. The PROM holds the map of the Conlog spiral, including the locations of failed tiles and spare memory cells. It's called into play by the controller to access only good cells after the Conlog is established. It also activates spare cells if random errors are identified during scrubbing, long after the Wafer Stack has been in system use.

David Hall, chief executive officer of Anamartic in England, says that because of this ability to retain most of the memory tiles in a DRAM with some bad bits, "We can use about 80% of the dice on a wafer. This means that the Wafer Stack can be priced in volume at 60 to 75% of the price of equal-capacity solid-state disk drives based on traditional individual chips." He adds that conventional semiconductor manufacturing techniques may result in as many as 75% of the chips being rejected.

Transmit and receive

□ Operative Conlog   ⊠ Defective Conlog   — Interconnection (spiral)

2. EACH DRAM DIE also contains associated configuration logic, which is programmed to disable defective memory elements.

No two alike.

The 1-Mbit DRAMs are produced with a 1.3-μm n-well CMOS process. The chips have dimensions of 13.65 × 4.4 mm, which is about 20% larger than a standard device, in order to accommodate the spare cells. The DRAMs are organized as 256-kword by 4-bit fast-page units, requiring a 52-μs refresh time.

The Wafer Stack is the result of a team effort. The proprietary interconnect software and associated Conlog logic were designed in Cambridge, England, at Anamartic's research and development labs. Wafer development is a joint effort involving Fujitsu, which is producing the wafers in Japan and distributing the product there. Besides U.S. and European sales and marketing, Anamartic's U.S. operation in San Jose, Calif. is also responsible for the engineering of customer interfaces to the Wafer Stack.

LIKE A CIRCUIT BOARD
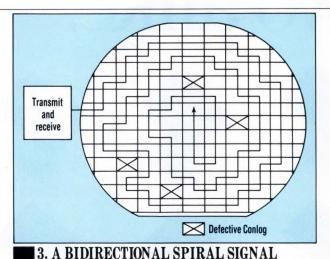
Anamartic's Scandalios says that the wafer carrier is similar to a conventional circuit board "that's a bit larger than the 6-in. wafer." A silicon nitride layer protects the top layer of the wafers, over which a silicon gel is applied, to protect the wire bonds from moisture. Two wafers are placed face-to-face in a hermetically sealed clamshell-like arrangement to form a 40-Mbyte module.

Tandem's Laurich characterizes his company's work with its early

3. A BIDIRECTIONAL SPIRAL SIGNAL network runs from the wafer periphery to the center.

Wafer Stacks as prototype and alpha testing. "We don't have a full configuration yet, but we expect deliveries of those in the next 30 days or so." The early experience prompts him to say that he's very excited about the technology and happy to work with Anamartic. "It's been a real team effort. We started with an essentially undefined project, but we've been knocking off the benchmarks quite well since getting it defined," Laurich says. "If things continue to go the way they have, 12 to 18 months seems to be a logical timeframe to have the Wafer Stack in a Tandem system."

Laurich isn't ready to elaborate on the benchmarks, but points out that Tandem plans for the Wafer Stack to eventually replace the company's V80 and XL80 Storage Facilities, which serve Tandem's own OLTP systems and are sold for use with other computers. The V80 holds 265 Mbytes of formatted data for each 8-in. disk drive. Eight of these disk drives can be put into a system to supply 2.1 Gbytes of formatted data. The XL80 uses 9-in. disk drives to supply a maximum of 7.16 Gbytes of formatted data. This large amount of storage is obtained by ganging eight disk drives.

A major attraction for Laurich is the "no-latency/fast-access" feature of the Wafer Stack applied to OLTP systems, which typically make frequent accesses to short blocks of data in a database. The da-

tabase can be partitioned to take advantage of those frequent accesses to greatly boost system throughput. Finally, Laurich is convinced that although the Wafer Stack storage subsystem carries a high initial cost compared to magnetic mass storage, it still holds the promise of being at least 50% cheaper than it would be to use standard 1-Mbit DRAMs in a conventional solid-state disk.

So-called "solid-state disks" using dice that were separated from the wafer and mounted to substrates or circuit boards are currently being used by a few computer companies. But 20 years of effort to come up with a viable commercial approach to true wafer-scale integration hasn't succeeded until now.

A 20-YEAR EFFORT

The most notable recent attempt, a project at Trilogy Ltd. that also involved development partners, failed to yield a viable product despite an investment estimated at about $100 million. Research and development into the concept goes back more than 20 years.

Texas Instruments Inc. had a project in the late sixties (funded by the then Avionics Laboratory at Wright-Patterson Air Force Base) that applied "discretionary wiring" in an airborne computer. The idea was to leave the top metallization layer of a wafer uncommitted until the wafer probing stage at which good devices are identified. Then a mask was to be created that interconnected only those good dice with final metal. However, the effort didn't evolve into commercial production. That dream was left for Anamartic to realize with the Wafer Stack storage subsystem.□
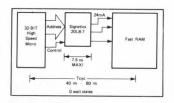
"Vroom!"

Turbocharge your memory for zero wait state design with Signetics fast 7.5ns PAL®-type devices.

Vroom! Now you can get the zero wait state performance that will allow memory to keep pace with the new ultra-fast microprocessors. And you won't have to pay top price for your memory to do it!

7.5ns PAL-type device improves system performance.

Vroom! Boost system speed, lower memory cost. Signetics offers the fastest (7.5ns) PAL-type devices for high-speed decoding. Now you can design with slower, less expensive, more available memory devices and still enhance system speed. And all Signetics PLDs are easily supported by ABEL, CUPL or our powerful AMAZE design software.

7.5ns 20-pin		7.5ns 24-pin	
PLUS16L8-7	PLUS16R6-7	PLUS20L8-7	PLUS20R6-7
PLUS16R4-7	PLUS16R8-7	PLUS20R4-7	PLUS20R8-7

Vroom! We've got the guts! That's right, we have those essential PLDs you need to improve total system performance. Programmable Macro Logic, Logic Arrays, Logic Sequencers and our PAL-type products that cut system cost while boosting system speed.

Turbocharge your memory now! Call Signetics at (800) 227-1817, ext. 985C, for a free High-Speed Decoder Handbook. For surface mount and military product availability, contact your local Signetics sales office.

PAL is a trademark of AMD/MMI. © 1988 NAPC

Signetics

Philips Components

PHILIPS

DAVE BURSKY

OPTICAL STORAGE COMPLEMENTS MAGNETIC DRIVES, FILLS MANY NICHES.

OPTICAL DISK DRIVES TACKLE ALL NEEDS

When first developed at the beginning of this decade, optical-disk storage systems were touted by many technologists as the ultimate solution for high-density storage, eventually replacing magnetic disk drives. However, that hasn't happened: Advances in capacity for magnetic storage devices have kept the magnetic disks in the running, but optical storage systems are finally starting to move into mainstream applications.

More intelligent control schemes, embedded cache memories, and higher spindle speeds have meant faster optical-disk access and data-transfer times. The rather slow 300-to-500-ms access times of early optical drives have improved to as fast as 35 ms. As a result of these features,

newer optical drives can burst data across a small-computer system-interface (SCSI) cable at rates of 4 Mbytes/s and faster, compared to data transfer times of only a few hundred thousand kbytes/s for older optical drives.

Though the 35-ms access time is still slower than the newest magnetic disk drives, it's closing in on some of the older magnetic drives. Furthermore, faster and higher capacity optical drives will appear in the next decade as a culmination of additional advances in optics and in media and control circuitry. Moreover, with improvements in system reliability, the optical drives can now tackle applications in commercial, industrial, and military systems.

Unlike Winchester disk drives, in which all drives can write and read data, there are three types of optical drives—Write-once Read Multiple (Worm), Compact Disk Read-Only Memory (CD ROM), and Erasable Optical (EO). Each has different characteristics and features *(see "Differentiating optical drives," p. 58)*. And each has found a niche that complements, rather than competes with, magnetic-disk storage systems.

Low-cost CD ROMs are excellent for documentation distribution, simple data bases, technical manuals, encyclopedias, and other slow-changing material with high information-content levels for which access time, data transfer rates, or last-minute updates aren't of paramount concern. Worm-type drives

are starting to cut into a small portion of the CD ROM market, but their main function is in the storage of large quantities of new incoming data. Some typical storage applications include engineering design files, financial recordkeeping, image management, computer backup, data logging, and others.

In addition, the drive manufacturers are continuing research that will yield rewritable CD ROM subsystems in 1990, and drives that use even smaller disks (3.5-in.) than the now standard 5.25-in. systems. Tandy Corp., for example, announced in 1988 that it was developing a rewritable CD. Even larger-di-

ameter platters—8-, 12-, and 14-in.—in Worm systems are growing in popularity for document storage systems. Their popularity is due, in part, to their very high data capacity of 750 Mbytes to 3.4 Gbytes per platter side. And with the use of the mechanical jukeboxes that automatically change the optical disks, hundreds of gigabytes of data can be within reach in just a few seconds.

ERASABLE DRIVES

The newest of the drive types, the EO drives, closely resemble Winchester disk drives. EO drive applications can mimic the magnetic storage applications that require remov-

able storage, such as secure systems where data must be locked up when not in use, portable computing environments, and data back-up. EO drives are also starting to compete with tape subsystems for data back-up applications because the optical systems can transfer data much faster than most tape systems.

New tape entrants, such as helical-scan 8-mm tape storage and 4-mm digital-audio-tape subsystems, offer gigabyte storage capacity on a palm-sized tape cartridge. Due to the low cost of the storage media, these systems will compete with other tape subsystems, as well as with the EO drives, for the back-up market.

DIFFERENTIATING OPTICAL DRIVES

To select the best drive type for a particular set of applications, optical disk drives present a critical set of trade-off choices to the system integrator. Write-once optical drives, as their name implies, lets users write new data onto a disk until the disk is full. To write, a laser can create either a pit or bubble on the disk, or cause a phase change in the disk's material to represent each bit *(Fig. A)*.

Unlike Winchester-type disk drives, Worm drives don't erase existing data on the optical disk. Instead, when a file is updated and stored under the same name, the system software stores the new file and just deletes the name of the old file from the disk directory, by modifying some control bits. Similarly, to erase a file, the directory is modified to hide the file reference.

Some of the major applications for these optical drives span large databases, archival record storage, image files, and computer backup. With file management software, users can treat the drive as if it was a slow Winchester, with one added benefit: Because data is never overwritten, work in progress can be traced through all revisions that were at various points in time stored on
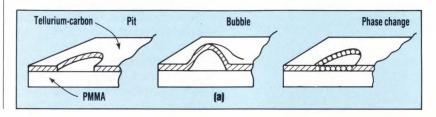
the disk. Users can supply an "audit trail" with this feature to trace the entire history of events relating to a task.

CD ROM optical drives are currently read-only devices that require pre-recorded CDs. These drives are relatively low in cost because they share many of the same features as the audio CD players. Ideal for storing manuals, books, fixed data bases, and programs for distribution, the low cost of CD drives will place the technology in many consumer applications. However, data can't be altered because the disks are pre-recorded. Consequently, CD ROMs would seem best suited to store reference material. And since the mechanisms are an offshoot of the audio CDs, data rates and access times are relatively slow—typically less than 200 kbytes/s and about 400 ms, respectively. The low data rate also limits the type of applications the drive can tackle.

Erasable optical drives can be

built with several technologies, the most popular being magneto-optic (MO). The other two approaches use a dye polymer or a phase-change material. In the MO scheme, the laser beam heats a spot on the disk. A magnetic field generated on the optical head causes the material to change its polarization. Of the three choices, MO technology has the longest durability—about 10 million write cycles. The other two technologies are at least a factor of ten worse.

For most applications, the lifetime of the MO media is considered equivalent to that of a standard disk drive. However, the complex read-write head and the higher cost of the MO recording media are trade-offs to consider when selecting the right drive for the system *(Fig. B)*. In contrast, the read-write head assemblies in phase-change and dye-polymer drives are simpler because they don't need the magnetic coil required by the MO disks to change

OPTICAL DISK STORAGE

The oldest of the drive-type choices, the large Worm drives come with 12- or 14-in. disk diameters—newer versions have 5.25-in. diameters. The 12-in. versions store from 1 to more than 3 Gbytes on each side of a platter, while the larger 14-in. system—a one-of-a-kind offering from Eastman Kodak—stores up to 3.4 Gbytes on one side. However, advanced 12-in. Worm drives slated for production in 1990, such as an enhanced version of Sony's WDM-3DLO, will deliver storage capacities of more than 6 Gbytes/platter, which is twice the 3.2-Gbyte capacity of Sony's current system.

Similar to its predecessor, the drive will use a formatting scheme called constant linear velocity (CLV), which employs a spiral data track rather than the pie-wedge-shaped track-and-sector structure used by most other companies *(Fig. 1)*. The CLV format and a variable-speed motor keep the data speed constant as it moves past the read-write head, no matter where the head is positioned on the disk. In contrast, the standard pie-wedge track-and-sector approach—referred to as Constant Angular Velocity (CAV)—used on most magnetic drives and numerous optical products, runs the spindle motor at a constant speed. Consequently, data on the outer tracks passes under the head faster than data on the inner tracks.
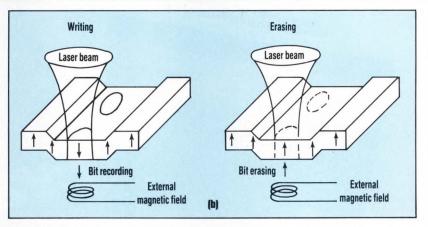
To obtain the higher capacity, Sony put more sectors on the spiral track by using a shorter-wavelength laser diode to make the spot size smaller. The company opted not to make the track longer because the algorithm that calculates the data's position in the spiral is relatively complex. A longer track would increase the computations and thus slow down the access. Most of the other large Worm drives from ATG, Hitachi, Laser Magnetic Storage, Optimem, Pioneer (the only company that offers an 8-in. Worm drive), and Toshiba use a form of the simpler the material's magnetic phase.

Furthermore, the cost of phase-change or dye-polymer platters is much lower than an MO disk. Although most applications will never require data to be rewritten even 10,000 times, it's possible that the disk's directory could reach the material's upper limit because it sees the most updates of any disk portion. Consequently, the phase-change and dye-polymer platters aren't the best choice in applications that do alot of revisions to the disk directory.

To perform a write operation, a MO drive must erase the bit that's in the desired position on the first disk rotation. On the second disk rotation, the drive writes the new bit, and on the third rotation it verifies that the data was written properly. As a result, storing data on a disk using MO technology is relatively slow because three disk rotations are required.

Each of the three passes may typically require about 25 ms when the disk spins at 2400 rpm. In contrast, a standard magnetic disk can be overwritten in just one pass. The other two erasable optical storage technologies have drives that can write the data on the first rotation and read it back to verify if it was written correctly on the second rotation. Most

(b)

MO drive manufacturers make it possible for the software to turn off the verify step if confidence in the system is high. This saves the time for one disk rotation from each storage cycle.

To find ways to eliminate the magnet, thus simplifying the read-write head and lowering the cost of MO drives, research is continuing on schemes to achieve direct overwrite that use a multi-layer disk and a permanent magnet rather than an electromagnet or no magnet at all. That would eliminate the latency time of the erase cycle.

For in-depth discussions of optical disk control software and system integration aspects, there are some reference books that might give some insight. They include:

Software for Optical Storage by Brian Berg and Judith Paris Roth; *Systems Integration for Write-Once Optical Disks* by Sanjay Ranade; *Optical Storage Technology: A Bibliography* by William Saffady; and *Optical Storage Technology 1988: A State of the Art Review*, also by Saffady. All are published by Meckler Corp., Westport, Conn. Also recommended are a trio of books on *Magnetic Recording (Volumes I, II, and III)* by C. Dennis Mie and Eric Daniel, and *The CD ROM Handbook* by Chris Sherman that are published by McGraw-Hill Book Co., New York, NY; and lastly, *CD ROM, The New Papyrus* by Steve Lambert and Susan Ropiequet from Microsoft Press, Redmond, Wash.

FREE

Making the change from Analog to Digital scopes.

Scope Evaluation Guide & Circuit Board instructions

The Digital Scope Evaluation Kit

OPTICAL DISK STORAGE

CAV approach. Toshiba, though, divides the sectors into zones, for an approach known as zoned CAV or ZCAV. Rather than keep the number of bits the same on the longer outer tracks, the bits per track are gradually increased. This results in increased disk capacity.

Offering the highest sustained data transfer rate at the 12-in. level of 600 kbytes/s, the LD1200 family from Laser Magnetic Storage Worm drive gains that speed through its proprietary direct-read-during-write scheme, eliminating one disk rotation from the latency time during a write. The high end of Optimem's family, the 4000 series drives, currently store up to 3.92 Gbytes on one disk and have an average seek time of about 150 ms. Sporting a built-in SCSI controller, the drive can transfer data over the SCSI channel at 766 kbytes/s. Also available are the 2400 and the 1000 series Worm drives that hold 2.4 Gbytes/platter.

Toshiba's WM-S500 12-in. Worm drive ups the storage to 5 Gbytes/disk thanks to the ZCAV formatting and has just a slightly slower average seek time—160 ms. Also packing at least 5 Gbytes/platter, Hitachi's forthcoming Worm drive will also up the data rate by increasing the disk rotational speed well above the 600 rpm used in the current generation OD301A, which can store up to 2.6 Gbytes on a 12-in. disk.

Maximum seek times for the large drives range from about 190 ms to 400 ms, depending on the drive, while most have an average seek time from 150 to 250 ms. When attached to SCSI controllers, the drives can transfer bursts of data from 1.1 to 1.5 Mbytes/s, or sustained data transfers of 262 to 625 kbytes/s.
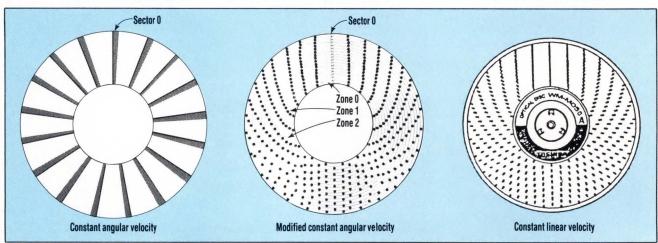
Smaller, 5.25-in. Worm drives are also divided among both the CLV and CAV types and they typically use disks that store from 100 to over 300 Mbytes/side. Furthermore, many drive manufacturers offer a proprietary-enhanced storage mode employing a zoned-sector scheme that increases the capacity to about 450 to 500 Mbytes/side. From Bernoulli Optical Systems comes the promise of a "floppy"-like optical paper technology that if brought to fruition will offer 1.2 Gbytes of storage on a 5.25-in. drive that can access in less than 40 ms and record data at up to 1.5 Mbytes/s. Currently in development, the Bernoulli optical drive will be sampled some time in 1990.

For 5.25-in. drives, there's a dual interchange standard emerging from the American National Standards Institute, which may finally provide some solution to the interchangeability problem. At least three different formats are currently in use, making it difficult to ex-change optical disks between different drive types. Larger Worm drives don't have any standards. Each manufacturer—ATG, Hitachi, Kodak, Laser Magnetic Storage, Optimem, Pioneer, Sony, and Toshiba—employs its own proprietary formatting, preventing disks from being interchanged among different manufacturers' systems.

Originally considered a negative aspect, the non-erasability of data in the Worm drives has turned into a positive feature in industries such as finance, legal, accounting, medical, and many others that must keep historical records. Managing the files on the disk is probably the hardest aspect of the subsystem design, because each time a new file version is stored under the same name, the name of the previous version must be removed from the disk directory.

Currently, there are over a dozen manufacturers of 5.25-in. Worm systems—less than half are U.S.-based. Some of the U.S. players include Cherokee, Information Storage, LaserDrive, Laser Magnetic Storage, Maximum Storage, Mountain Optech, and Shugart. Overseas, it's dominated by the Japanese, with such companies as Fujitsu, Hitachi, Matsushita, Mitsubishi, Pentax, Pioneer, Ricoh, Toshiba, and others. One European vendor—Philips—owns a part of Laser Magnetic Stor-

Constant angular velocity   Modified constant angular velocity   Constant linear velocity

1. THE TWO MAIN FORMATS for optical disks—constant angular velocity and constant linear velocity—store the data very differently on the disks. In CAV systems, a constant-speed motor spins the disk while data are stored in circular tracks. The tracks are divided into sectors similar to those on a magnetic disk (left). A modified version of CAV divides the tracks into zones and increases the bit density in the track as the radius of the track increases (middle). Achieving about the same density as the modified CAV, CLV uses spiral-shaped tracks and a variable-speed motor to keep the data-rate constant under the read-write head (right).

When it comes to SUPER POWER...

Look who's playing second fiddle to Sorensen!

Yes...all the super powers are competing in world markets, but only Sorensen's new Super Series (S-Series) multiple output switching power supplies can outperform them all! The new S-Series offers thousands of models with 1-5 outputs and power levels ranging from 500-2000 watts. All deliver outstanding reliability and fast load response for greater efficiency and performance.

Don't be fooled by look-a-likes. All high-power sources are not created equal. Sorensen's S-Series leads the way with:

- Power MOSFET design to assure high switching frequency for cleaner output

- Current Mode Control to provide instantaneous current limit protection

- Absolute current sharing to distribute the power load equally and assure product longevity and performance

- Advanced forward convertor topology which permits use of lower voltage MOSFETS with higher efficiency

Sorensen Announces Super Power Demo Program
See what super-power feels like! Try the specific S-Series model right for your application in your own environment! We're confident you'll agree that the S-Series is the best power source for your application. Call Sorensen at 1-800-525-2024 or your local Sorensen representative and put the powerful S-Series to work for you!

Call for your top secret Dossier!
Sorensen has prepared a complete specifications dossier for your eyes only. To receive this classified information, call 1-800-525-2024!

When it comes to your super power requirements, don't fiddle around with second best...call Sorensen.

Sorensen
A **Raytheon** Company

5555 N. Elston Avenue
Chicago, Illinois 60630
(312) 775-0843
FAX: (312) 775-7432
Toll-Free: 1-800-525-2024

The Balance of Power is Shifting to Sorensen!

CIRCLE 44

age. Also, many large computer manufacturers and small peripheral vendors, such as H-P, IBM, and Micro Design International, are delivering optical drives that they OEM from one of the aforementioned manufacturers.

Both Cherokee and Mountain Optech have focused their initial efforts on developing rugged military Worm drives. Mountain's SEL-2 Worm drive holds 200 Mbytes/side. Mountain is also developing the SE-400M, a version with a 400 Mbytes/cartridge capacity set for release in early 1990. By late 1990, it expects to obtain 650 Mbytes/cartridge and an access time of less than 65 ms in the SE-650M drive. Commercial versions of the same drive are also available, as are Tempest and space-ready versions of the SEL-2.
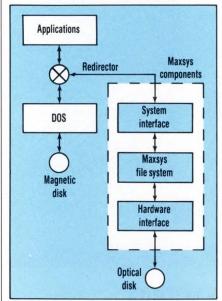
In addition, the control circuits in Mountain's drive use an adaptive digital-signal processor to achieve better repeatability and to avoid the component aging problems often encountered with analog schemes for the spin, focus, and tracking servo control. The drive also can perform a direct read during a write operation, which lets the drive sense if a particular bit was written before the laser leaves a spot. The ability to detect an error immediately gives the drive a speed edge over many of the other Worm systems, which require a second pass to verify data.

Cherokee's military Worm drive packs a capacity of 326 Mbytes and an embedded SCSI controller. Employing a positive-head-movement scheme, the drive can access data in just 112 ms. By next year, the company expects to cut that time to less than 100 ms. The drive can also read data from the company's previous 260-Mbyte/side disks. Firmware in the drive switches the optical drive to the proper operating mode.

Today's peak capacity for 5.25-in. Worm platters (about 600 Mbytes) has already started to give way to 12 Gbyte platters, thanks to a squeezing of more tracks per inch and more efficient storage formats. To make the systems easier to use, many software support packages let the Worm drives emulate Winchester-type magnetic drives. Furthermore, to leverage the removable aspects of the media, multiplatter jukeboxes that make it possible for tens of gigabytes of data to be available in less than a minute's notice are now available from some drive suppliers and a few non-drive manufacturers.

Packing the highest capacity per platter, Information Storage's ISi 525GB holds a maximum of 1280 Mbytes, thanks to a proprietary format used to store the data. Due to the

2. TYING INTO THE HOST
system software just under the application layer, the Maxsys operating system from Maximum Storage takes over and masks the Worm drive from users. This makes the Worm drive appear to be a Winchester drive with no partition limitations.

high data capacity, data transfers can be done at 6.5 Mbytes/s—the highest rate of any optical drive. The company also has the ISi 525WC, an older, 244-Mbyte drive.

Following closely in density, the Model 810 from LaserDrive squeezes 405 Mbytes on each side of a disk with a zoned form of CLV formatting. The system uses a proprietary edge-detection data-encoding scheme that makes it possible for two bits of data to be stored in each pit created by the laser. Information is encoded by the time differences between the edges of the holes and the gaps of different length. Average access time for the drive is 175 ms, while the data transfer rate over the SCSI channel is 1.5 Mbytes/s.

Boasting an effective access time of just 28 ms, an intelligent Worm subsystem from Maximum Storage—the APX-4000—gets its speed from a proprietary data format and DOS-transparent control software. A similar version for Sun's Unix environment is currently in development. The subsystem can store up to 800 Mbytes on a two-sided optical-disk cartridge and transfer data off the disk at a speed of 5 Mbits/s. About four seconds are needed to access and read a 1-Mbyte file, which is comparable, if not faster, than most Winchester disk drives. The system is fully compatible with cartridges written by the company's previous system, the APX-3000, which stores 244 Mbytes on a cartridge.

The Maxsys file system software is available as part of the subsystem kit. This software sets up a hierarchical file structure that permits up to 20 subdirectory levels with 15 simultaneous open files, unlimited files per directory or subdirectory, unlimited file sizes, and unlimited partition sizes. By tying into the operating system just below the application layer, the software redirects system operations without disturbing the PC's native operating system (Fig. 2). Moreover, the software can also manipulate files on the disk, whether they're active or hidden (deleted).

A 654-Mbyte/platter Worm system from Pioneer can be expanded to 1.3 Gbytes by adding a second drive to the first drive's controller. The system uses organic dye-based disks that are estimated to have an archival lifetime of greater than 15 years. The DD-U5001 drive has an average seek time of just 60 ms. The mechanical design employs a magnetic clamping scheme that makes it possible for the drive to squeeze into a half-height slot (41-mm high). Packing 300 Mbytes/side, the MW-501 drive from Mitsubishi delivers an average access time of 80 ms. It can be used in a jukebox system that puts up to 90 Gbytes of data within reach in about 10 seconds.

Approximately only 40,000 5.25-in. Worm drives were installed this year, according to Dataquest Inc., San Jose, Calif. That number, however, is expected to quadruple by 1991 and more than triple again by 1993. During the next few years, improvements will be made in access time and transfer rates. Today's drives range in access (seek) times from an average time of 60 to about 200 ms; worst-case times range from about 200 to almost 500 ms. Data transfer rates depend on the controller and the amount of cache used for the drive—from a low of about 210 kbytes/s to over 2.5 Mbytes/s.

A principal advantage of optical storage systems is transportability. Magnetic drives are difficult to move on the other hand, with the exception of a few low-capacity removable magnetic disk drives (less than 80 Mbytes of storage). Transporting data from magnetic drives to another system involves moving the entire drive or copying its contents onto a

OPTICAL DRIVE MANUFACTURERS

Amdek Corp.
San Jose, Calif.
(408) 922-5700
Drive type = 3
CIRCLE 451

Art Tech Gigadisc (ATG)
1270 Avenue du
   General Eisenhower
BP 1270
31047 Toulouse
Cedex, France
Drive type = 1
CIRCLE 452

Canon America Inc.
Lake Success, N.Y.
(516) 488-6700
Drive type = 2, 3, and 4
CIRCLE 453

**Cherokee Data
   Systems Inc.**
Boulder, Colo.
(303) 449-8850
Drive type = 2 and 4
CIRCLE 454

Chinon America Inc.
Information Equipment Div.
Torrance, Calif.
(213) 533-0274
Drive type = 3
CIRCLE 455

Datec Inc.
Chicago, Ill.
(312) 648-0684
Drive type = 4
CIRCLE 456

**Dolphin Systems
   Technology**
Santa Ana, Calif.
(714) 558-3220
Drive type = 4
CIRCLE 457

Epson America Inc.
OEM Products Div.,
   Peripherals Group
Los Angeles, Calif.
(714) 768-7474
Drive type = 5
CIRCLE 458

Hewlett-Packard
Palo Alto, Calif.
(619) 592-8546
Drive type = 2, 3
CIRCLE 459

Hitachi America Ltd.
Computer Division
San Bruno, Calif.
(415) 872-1902
Drive type = 1, 4
CIRCLE 460

IBM Corp.
Low-end optical products
Tucson, Ariz.
(602) 799-1000
Drive type = 2
CIRCLE 461

Information Storage Inc.
Colorado Springs, Colo.
(719) 579-0460
Drive type = 2
CIRCLE 462

Iomega Corp.
Roy, Utah
(801) 778-1000
Drive type = 2
CIRCLE 463

JVC Disc America, Inc.
Tuscaloosa, Ala.
(205) 556-7111
Drive type=3
CIRCLE 464

Kodak Mass Memory Div.
Rochester, N.Y.
(716) 724-5130
Drive type = 1, 5
CIRCLE 465

**Laser Magnetic
   Storage Inc.**
Colorado Springs, Colo.
(719) 593-7900
Drive type = 1, 2, 3
CIRCLE 466

LaserDrive
Santa Clara, Calif.
(408) 970-3600
Drive type = 2, 5
CIRCLE 467

Maximum Storage Inc.
Colorado Springs, Colo.
(719) 531-6888
Drive type = 2
CIRCLE 468

Maxtor Corp.
San Jose, Calif.
(408) 432-1700
Drive type = 2, 4
CIRCLE 469

**Micro Design
   International Inc.**
Winter Park, Fla.
(305) 677-8333
Drive type = 2
CIRCLE 470

**Mitsubishi Electronics
   America Inc.**
Computer Peripherals Div.
Torrance, Calif.
(213) 515-3993
Drive type = 2, 3, 4
CIRCLE 471

Mountain Optech
Boulder, Colo.
(303) 444-2851
Drive type = 2
CIRCLE 472

Nakamichi
Torrance, Calif.
(213) 538-8150
Drive type = 5
CIRCLE 473

**Nissei Sangyo
   America Ltd.**
Torrance, Calif.
(213) 328-9700
Drive Type = 3
CIRCLE 474

NKK Corp.
Electronics Div.
Hieikudankita Bldg.
4-1-3 Kudankita
Chiyoda-ku, Tokyo 102 Japan
(81) (3) 288-3839
Drive type = 2, 4
CIRCLE 475

**NEC Information
   Systems Inc.**
Boxborough, Mass.
(508) 264-8000
Drive type = 2
CIRCLE 476

Olympus Corp.
Torrence, Calif.
(213) 373-0696
Drive type = 4
CIRCLE 477

Optimem
Div. of Cipher Data
Mountain View, Calif.
(415) 961-1800
Drive type = 1, 2
CIRCLE 478

Optotech Inc.
Colorado Springs, Colo.
(719) 570-7500
Drive type = 2
CIRCLE 479

Panasonic Industrial Co.
Computer Products Div.
Secaucus, N.J.
(201) 392-4603
Drive type = 1, 2, 4
CIRCLE 480

Pentax Teknologies
Broomfield, Colo.
(303) 460-1600
Drive type = 2
CIRCLE 481

**Pioneer Communications
   of America**
Optical Memory
   Products Div.
Carson, Calif.
(213) 513-1016
Drive type = 1, 2
CIRCLE 482

Ricoh Corp.
San Jose, Calif.
(408) 432-8800
Drive type = 2, 4
CIRCLE 483

**Sharp Electronics
   Corp.**
Mahway, N. J.
(201) 529-8200
Drive type = 3, 4
CIRCLE 484

Shugart Corp.
Irvine, Calif.
(714) 770-1100
Drive type = 2
CIRCLE 485

**Sony Corp.
   of America**
Optical Storage Div.
Park Ridge, N.J.
(201) 930-6025
Drive type = 1, 3, 4
CIRCLE 486

Storage Dimensions
San Jose, Calif.
(408) 879-0300
Drive type = 2
CIRCLE 487

**Storage Plus Inc.
   (Sumo Systems)**
San Jose, Calif.
(408) 453-5744
Drive type = 4
CIRCLE 488

**Summus Computer
   Systems**
Houston, Texas
(713) 492-6611
Drive type = 2
CIRCLE 489

Tandy Corp.
Fort Worth, Texas
(817) 390-3693
Drive type = 3, 4
CIRCLE 490

Toshiba America Inc.
Disk Products Div.
Irvine, Calif.
(714) 583-3108
Drive type = 1, 2, 3
CIRCLE 491

Verbatim Corp.
An Eastman Kodak Co.
Sunnyvale, Calif.
(408) 773-5777
Drive type = 5
CIRCLE 492

Yahama Inc.
Buena Park, Calif.
(714) 522-9223
Drive type = 3, 4
CIRCLE 493

Consider this a guide rather than a definitive list.

Drive type coding:
1 = 8-, 12- or 14-in. Worm Drive
2 = 5.25-in. Worm Drive
3 = 5.25-in. CD ROM Drive
4 = 5.25-in. Erasable Optical Drive
5 = 3.5-in. Optical Drive (any type)

"Static can kill our circuitry. And the front panel LEDs can provide the path. Now what?!"

All indications are Dialight.

It was a problem grounded in the laws of electrical energy. And it could have caused real havoc. But the customer took the smart step of calling Dialight.

As the leader with over half a century of experience in every type of indicator light, for Dialight solving problems is standard operating procedure. Applying our engineering expertise in optoelectronics and utilizing state-of-the-art CAD equipment, our model shop quickly developed and prototyped a housing and grounding plate for the LEDs. Upon customer approval, our 100% internal tool fabrication and molding facilities provided quick turn-around on production quantities.

Saving costs while solving problems is something we've long done with our panel mount and circuit board LEDs. Over the years customers have asked us to pair, gang, piggyback, right angle mount, recess, bicolor, tricolor, slant, standoff, snap-mount, bin, do whatever you can imagine to them and we haven't been stumped yet!

So, when an indication design issue has you ground to a halt, remember that no one has more solutions than Dialight.

DIALIGHT CORPORATION
A Cambridge Electronic Industries Co.

1913 Atlantic Avenue, Manasquan, NJ 08736   201-223-9400

CIRCLE 36

Look who's talking to IBM now— with a single chip.

THE DP8344 BCP OPENS UP THE IBM WORLD.

Because of this one little device, a lot of players have found effective new ways of getting into the Big Blue game. Among them are Apple, Digital Equipment Corporation, and many others emerging as winners in IBM protocol design and development.

The DP8344 Biphase Communications Processor (BCP) is the key component in Apple's new adapter card for the Macintosh II—a landmark beginning in Apple's strategy of integration into the IBM mainframe environment.

The BCP is also a key component in Digital's new 3270 Terminal Option Card for the DECserver 550, which gives IBM 3270 displays full-screen VT220 access to VAX applications. Users can simply "hot-key" from their IBM system to Digital's program development environment, industry-leading ALL-IN-1, and world-class UNIX.

Besides putting new players in the game, the BCP gives existing plug-compatible players—like Memorex Telex—big competitive advantages.

A LOT OF POWER IN A VERY SMALL SPACE.

An intelligent transceiver and high-performance CPU are integrated on the same low-power CMOS chip. So a full system supporting all three IBM protocols—3270, 3299 and 5250—can be implemented in an area the size of a credit card.

Yet the DP8344 BCP's RISC architecture is so powerful that it's the only processor needed in the new Memorex Telex 1192 Enhanced Function Display Terminal Series. Memorex Telex was able to cut both power consumption and board space—while adding a lot of new features, like an on-screen calculator and adjustable cursor-movement rates.

The BCP also enables Digital to maintain both its own and IBM sessions for four terminals with a single chip. And Apple can implement IBM coax and twinax protocols with the same hardware platform and two-line interfaces.

WE'LL GIVE YOU ALL THE SUPPORT YOU NEED.

Our system solution includes a Multi-Protocol Adapter Demonstration System for 3270/3299/5250 connectivity. It supports all popular terminal-emulation and file-transfer software.

We also offer the BCP PocketLink, a credit-card-size terminal emulator; a demonstration/development system with monitor debugger; and the DP8344 assembler/linker/librarian system.

LET'S TALK.

If you want your system to talk to IBM, you should first talk to National. Give us a call today at (800) 825-5805, ext. 103.

National Semiconductor

NEED BROAD-BAND COAXIAL RELAYS?
FROM 2 TO 24 THROW, MATRIX HAS THE ANSWER

Our versatile 7000 series of coaxial relays have band-widths from DC up to 800 MHz. They're available from 2 to 24 throw. And by using our 9000 series cross-straps, switching matrices of any size can be configured.

Why have Matrix broad-band relays become the industry standard? Because we construct them of precision machined anodized aluminum alloy, all signal shield paths are silver plated, and basic switch elements are hermetically sealed in nitrogen filled gas envelopes with rhodium plated contacts to insure non-stick operation.

The end result is extremely low crosstalk, EMI and VSWR. Another plus, all switchpoints are individually field replaceable.

The units are plug compatible with Matrix 6100A and 1600 Series Logic Modules for compatibility with RS-232, RS-422 and IEEE-488 Interface busses as well as 16 bit parallel.

Non-blocking Matrix configuration may be easily assembled using our self-terminating relays and 5100A series power dividers. Built-in Video/RF amplifiers allow zero insertion loss designs.

So if you're looking for broadband relays, it pays to deal with Matrix. After all, we've been designing state-of-the-art reed relay and semiconductor switching systems for over 18 years.

Our customers include government agencies, defense contractors, the TV industry, ATE and telecommunications companies—and more.

Phone: 818-992-6776
TWX: 910-494-4975
FAX: 818-992-8521

MATRIX
SYSTEMS CORPORATION

5177 NORTH DOUGLAS FIR ROAD
CALABASAS, CALIFORNIA 91302
CIRCLE 49

See Matrix at Wescon '89 Booth 1151

tape. This tape, in turn, must be loaded into the other system.

In contrast, all optical drives have removable disks, so users need only to carry the disk from system to system. However, unlike tape drives that have some standardization for data formats on the tape, most company's Worm drives can't read data written by another company's Worm drive. Each drive manufacturer elected to use a different error-checking-and-correction scheme, as well as a different format for storing data on the disk tracks. Surprisingly, the blank media was standardized so that most Worm drives can use blank media from almost any firm.

The CD ROM drives, an offshoot of the CD audio technology, do have a standard format, and they have found a home in documentation distribution, now that the mastering cost for the disk was cut to less than a few thousand dollars. With the hundreds of megabytes of storage available on the 5.25-in. disk, companies can put dozens of catalogs, books, service manuals, etc. on one disk, and send out updates at a cost much lower than the printing and distribution cost of paper documents. Not only has the expense of the mastering come down, but so has the cost of the drive and control electronics.

Because the CD ROM technology shares many of the same mechanical components as the audio CD players, the cost of the mechanical portion of the CD ROM drive was reduced by the high-volume manufacturing of the audio drives. Much of the control circuitry is also similar—just a few circuit changes are required along with the elimination of the digital-to-analog converters. Nearly a dozen suppliers of CD ROM drives have emerged as a result of these similarities. This competition further reduces the price of the drives.

OEM prices for embedded half-height drives are now less than $500. Because the drives use field-removable cartridges, they give users various software to select from. According to Dataquest, about 160,000 CD ROM drives are currently installed worldwide. By 1991, that number will more than triple, and by 1993, it will triple again. A majority of those drives will come with either an AT-bus interface for use in PC-hosted systems or a SCSI interface for more general applications. In addition to PC-AT and SCSI interfaces, Hewlett-Packard has elected to offer its CD-ROM drives with its HP-IB interface to ease its connection to minicomputer systems.

Both Sony and Philips have announced a CD-Worm standard, and two other companies—Fuji Photo and Yamaha—have unveiled CD Worm systems. Furthermore, Tandy Corp. has an ongoing project for an erasable CD ROM that it expects to have ready for release in the second half of 1990. A dual-purpose drive with both CD ROM and Worm capabilities could also impact the tape drive market for system backups and software transport. That's because the need for a separate tape drive could be eliminated with a slight increase in media cost.

Many CD ROM drives include d-a converters so that both text and sound can be retrieved from the disk. Furthermore, through the use of special video compression

Square wave pulses with 1ns rise times for more realistic simulation

Simulating real power line noise is the job of our INS Series.

There's never been a more versatile noise simulator. Its wide range of simulation features can introduce many testing capabilities into your R&D and QA/QC programs.

Our INS-NA410R and INS-NA420R can superimpose square-wave impulses with super-quick rise times (under 1ns) onto AC or DC lines. The amplitude, width and repetition rate of these pulses are easily variable.

And with an optional coupling adaptor, application to uncut signal lines is not only possible but very easy. Testing against radiated noise and direct application of pulses to the metal cabinet of equipment can also be performed. All these features allow you to simulate potential noise problems and build safeguards into your products before shipment to your customers, which will give your company the competitive edge.

Helping you find sources of EMI is the job of our FVC Series

Sniff out sources of EMI before sending your product off for expensive testing. Simply by contacting the probe to the circuit to be measured, you can ascertain the electric and magnetic field strengths of each frequency band specified in the EMI standards of FCC, VDE, VCCI and CISPR. Models FVC-NA1000 locates sources of radiated emissions, and the FVC-NA30 locates sources of conducted emissions.

Contact us now for more details.

NoiseKen Corporation

Portland-Troutdale Airport 999 N.W. Frontage Road Troutdale, Oregon 97060
Tel : (503)665-0517 Fax : (503)665-2470

Visit us at Wescon/89
Nov. 14-16, Booth No. 800

CIRCLE 32

and decompression circuits, real-time video imagery can be stored on CD ROMs. With the digital video interactive (DVI) standard (now in its early stages), digitized video, audio, and digital data can be stored on a single disk. The compression scheme used by the DVI standard allows 72 minutes of video to be stored on a single disk.

THE BEST OF BOTH

Erasable optical storage drives resemble the Winchester disk drives because data can be written, erased, and rewritten. However, a common standard hasn't evolved yet because the type of media to be used is still uncommitted. For the erasable CD ROM disks, the most likely candidate is the organic-dye platter, projects Dave Herzberg, Editor of the Optical Memory News newsletter published by Rothschild Consultants, San Francisco, Calif. That platter type, he explains, will be lower in cost than other compounds and it can be used in a low-cost drive subsystem.

However, commercial ED drives are already being shipped—at least seven companies are already sampling magneto-optical drives—Canon, Matsushita (Panasonic), Maxtor, Olympus, Ricoh, Sharp, and Sony. Furthermore, at least four other manufacturers are starting to beta-test 3.5-in. erasable optical drives as well: Hitachi, Kodak, (Verbatim subsidiary), Matsushita (Panasonic), Nakamichi, and Seiko Epson. Prices for the 5.25-in. drives range from about $3500 up to $5000, but by late 1990 the OEM price for an erasable optical drive is expected to be in the $1800 to $2100 range. Only about 18,000 drives will be sold this year, but by 1991 that number should increase by 15-fold to about 240,000 units. And by 1993 over 1.5 million units should be sold.

One visionary company, NeXT Inc., Palo Alto, Calif., was the first to –incorporate a 5.25-in. erasable optical drive as standard equipment in its computer system. Although it may add a bit to the base system price, it gives users a huge amount of on-line storage and a means to transfer large amounts of data or carry an entire computing environment with all necessary data bases from machine to machine.

Though erasable drives will cost considerably more than a Winchester disk drive and not offer as fast an access time or write time, their main feature of removable media will make them attractive as an alternative memory subsystem in the overall system hierarchy. With current spindle speeds of 2400 rpm, the erasable drives can achieve sub-100-ms access times, which is within an acceptable range for read cycles.

In addition to the lack of standardization on the media type, the industry must also settle on the drive mechanics and control software. Various IEEE committees are trying to get some measure of standardization, especially regarding the drive mechanics. One of the biggest questions yet to be settled is: Should the drive use a continuous-composite servo approach to position the read-write head, or should it be a sampled-servo scheme?

Both approaches have their pros and cons, but according to Herzberg, the industry seems to be settling on the

What's more paralyzing is the way he gets treated.

The hardest part about having a disability is being constantly reminded
that you have one. Sometimes that happens when people stare at you.
Or point at you. Or don't even think of including you in every day activities.
Maybe it's time to start treating people with disabilities like people.

Easter Seals ®

continuous-composite servo scheme. Only Laser Magnetic Storage and Pioneer Electronics have adopted the sampled-servo scheme; most other erasable drive manufacturers have gone with the continuous-composite approach. Unfortunately, due to the way each system keeps track of the sectors and data, they're incompatible.

Although companies are talking about alternative media, MO-based disks are the only type in mass production and in use by drive manufacturers. With dual capacities of 650 Mbytes or 1 Gbyte, the Tahiti I drive developed by Maxtor (now shifted to its subsidiary, Maxoptix) offers one of the fastest average access times—just 35 ms. Its MO disk spins at 2200 rpm and can deliver data at up to 10 Mbits/s over an embedded SCSI channel.

Spinning its disk at 3000 rpm—the highest speed of any optical drive—the Cannon MO drive can deliver data at a speed of 9.1 Mbits/s with an average access time of 80 ms. The full-height drive accepts ISO-compatible cartridges that can store up to 512 Mbytes (two-sided). A companion bridge controller converts the drive's ESDI-like interface to a 1.5-Mbyte/s SCSI channel.
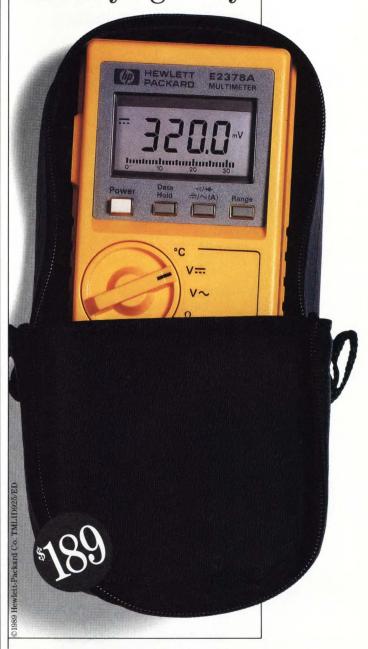
Occupying a full-height 5.25-in. drive slot, the Ricoh RO-5030E MO drive packs up to 652.8 Mbytes on a removable cartridge (two sided). It accesses data with an average time of 66.7 ms (one-third of full stroke plus latency) and spins the disk at 1800 rpm. With the embedded SCSI controller and 256-kbyte buffer memory, the drive can transfer data over the SCSI channel at 1.4 Mbytes/s. The drive is also available in an external standalone format (the RS-F), which connects to the PC-AT bus through a host adapter.

A similar drive offered by Sharp packs 422 Mbytes on a two-sided disk and has an average access time of about 150 ms because its disk rotates at only 900 rpm—half the speed of Ricoh's drive. However, comparable to the Ricoh drive, Sharp's unit includes an embedded SCSI controller that delivers data transfers of up to 2.4 Mbytes/s. Sony has a 5.25-in. drive—the SMO-D501—with a capacity of 650 Mbytes on a two-sided disk and one of the fastest transfer rates available—7.4 Mbytes/s. A short-stroke seek time of just 20 ms allows the drive to rapidly access data and deliver bursts of up to 3 Mbytes in less than 40 ms. Hitachi's OD112-1, a 644-Mbyte drive, claims an average access time of 75 ms and a maximum sustained data transfer rate of 925 kbytes/s.

One of the smallest EO drives is the TMO System 35/60, a 3.5-in. MO drive with a capacity of just over 60 Mbytes/side of a platter. Developed by Eastman Kodak's Verbatim subsidiary, the drive has a seek time of 30 ms and delivers performance similar to many small Winchester drives with the added feature of data removability/transportability. The drive will actually be offered by LaserDrive, another Kodak partner company.□

How Valuable?	Circle
Highly	547
Moderately	548
Slightly	549

The Hard &
of Performance

FACT: OEMs and system integrators cannot exist on hardware alone.

It takes more than superior board-level hardware to successfully integrate a high-performance image processing or vision system. It takes extensive, well-documented software tools, responsive hot-line customer support, and a generous selection of third-party hardware peripherals and software packages readily available to customers around the world.

FACT: Hardware performance must match customer needs.

From cost-effective plug-in boards, to sophisticated multi-board subsystems, our image processors are designed to meet *your* needs, with computers you want to use.

Compatible with PC AT, PS/2, Sun Microsystems, and many other AT and VMEbus-based computers

Variable-scan and digital input to interface with nonstandard cameras

Real-time pipeline processing for speed-critical applications

32-bit floating point processing when accuracy cannot be compromised

FACT: Good software tools speed development time.

Without good software tools, you're re-inventing the wheel! Our ITEX™ sub-routine library has *hundreds* of commonly used, high-level routines. A built-in interactive line interpreter lets you quickly test and modify sequences of ITEX functions without recompiling. And, source code is available.

Soft Facts
Image Processing

FACT: Compatible products should be abundant, and easy to locate.

Finding reliable application-specific software, cameras, monitors, and other compatible add-ons should be simple. So, we created the **Vantage Compatible Products Program** to put you in touch with third-party vendors offering products certified compatible with Imaging Technology's image processors. Our free *Vantage Listing & Reference Manual* is required reading for image processing integrators.

FACT: Imaging Technology is your best choice in image processing!

The fact is, we're working hard (and soft) to be the leading supplier of image processing boards, subsystems, software, and service. For more information, contact our technical sales support team today.

Eastern United States
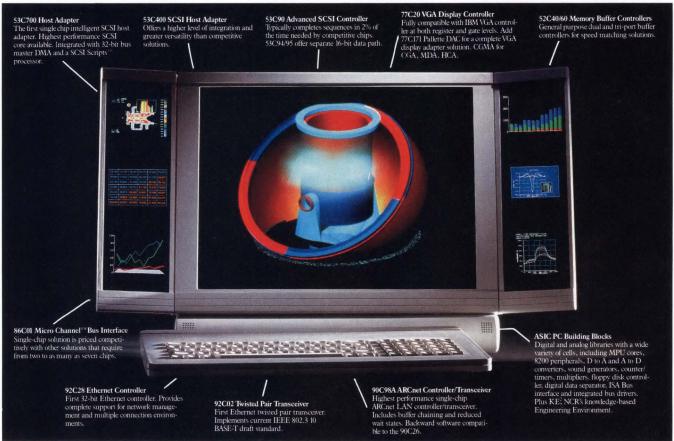
800-532-3500
(617-938-8444 in Massachusetts)

Central, Mountain, and Pacific United States

800-356-4216
(714-960-7676 in California)

Imaging Technology Incorporated
600 West Cummings Park
Woburn, Massachusetts 01801-6343
FAX 617-938-1757
TELEX 948263

IMAGING
Technology Inc.

Build A Multibus II Single-Board Computer

Making Use Of The i860's High Integration Level, Designers Can Put Together An SBC With 8 Mbytes Of DRAM.

NEAL MARGULIS
Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95052; (408) 765-8080.

By designing a complete CPU on one standard Multibus II board, system integrators can take advantage of rapidly advancing CPU technology while preserving their investments in existing hardware. Ideally, the single-board computer should have its own memory, local I/O circuitry, and a Multibus II interface.

By basing the CPU on an i860 64-bit microprocessor, the designer can bring the power of a supercomputer to the single-board computer. The board can be the main CPU running an operating system such as Unix, or it can become an application accelerator in an existing system. As an alternative, multiple CPU boards can be linked in a multiprocessor system with performance unavailable in an minicomputer.

Multibus II is a processor-independent bus architecture with full distributed-multiprocessor support. The standard, IEEE-959, defines a 32-bit parallel system bus (PSB) with a maximum throughput of 40 Mbytes/s. The PSB, which is optimized for standardized interprocessor communications, also handles accesses to I/O devices not dedicated to one CPU board.

The CPU board contains a number of functions that are made possible by the high integration level of the i860 and another key component, the 82380 integrated system peripheral. These features include a Multibus II interface using DMA and a message-passing coprocessor (MPC), a dynamic RAM (DRAM) main memory of 8 Mbytes based on 256-kbit-by-4-bit RAMs, a local I/O system, and an SBX connector *(Fig. 1)*.

Built into the i860 microprocessor are an integer execution unit, a floating-point unit, a graphics unit, a 4-kbyte instruction and 8-kbyte data cache, and memory-management and bus-control units. The integer execution unit runs 85 kDhystones, and the floating-point unit delivers 24 MWhetstones (DP) and 80 MFLOPS (SP). Z-buffer check and shading is supplied by the graphics unit. The cache memory makes possible a 960-Mbyte/s data rate. The units can operate in parallel, with high-bandwidth data rates and a 40-MHz operating frequency.

The 82389 MPC simplifies the task of interfacing the processor's local bus to the parallel system bus. Designed for the message-passing protocols of the Multibus II architecture, the coprocessor participates in the entire PSB protocol and performs bus arbitration, transfer control, error detection and reporting, and parity generation and checking. These functions occur independently of the host CPU.

Busses Isolated

The parallel system bus is isolated from the CPU local bus so that the i860 can access memory on its 64-bit data bus. In addition, decoupling the local bus activities from interprocessor communications over the PSB offers two advantages. First, resources that would be held in wait-states while dedicated bus-access arbitration is underway are instead free. This parallelism increases system performance. Furthermore, the bandwidth of one bus doesn't limit the transfer rate of the other: Each bus can perform full-speed, synchronous transfers.

The MPC's signals can be divided into three functional groups: PSB interface, local bus interface, and DMA interface *(Fig. 2)*. The primary

functions of the PSB interface signals are arbitration and system control. Six arbitration signals ($\overline{ARB}_{0-5}$) read card-slot ID and arbitration ID from the central services module (CSM) during reset. During arbitration, these signals output the arbitration ID for priority resolution.

Bus Request ($\overline{BREQ}$) shouldn't be confused with the i860 microprocessor's $\overline{BREQ}$ signal. Each bus agent asserts $\overline{BREQ}$ to gain control of the bus and samples $\overline{BREQ}$ to determine if other agents are also contending for bus control. A bus agent sends Bus Error ($\overline{BUSERR}$) to all other bus agents when it detects a transfer-cycle parity error. The CSM sends the bus Timeout signal ($\overline{TIMOUT}$) to all bus agents when a bus cycle fails to end within a prescribed time.

Ten System-Control signals ($\overline{SC}_{0-9}$) coordinate transfer cycles, as defined by the Multibus II Architectural Specification. With Directional Enables ($SCDIR_0$ and $SCDIR_1$), transceivers can buffer the bidirectional system-control signals. The MPC checks byte-parity lines (PAR_{0-3}) for incoming operations and sets the parity lines for outgoing operations.

Other parallel system bus signals are Reset ($\overline{RST}$), Reset-Not-Complete ($\overline{RSTNC}$), and ID Latch ($\overline{LACHn}$, where n = slot number). These signals are only used during system initialization.

The MPC also handles interrupts for bus agents on the parallel system bus by implementing them as virtual interrupts in the message space. To send an interrupt message, the processor writes the source destination and message type to the MPC, which coordinates the interrupt message transfer.
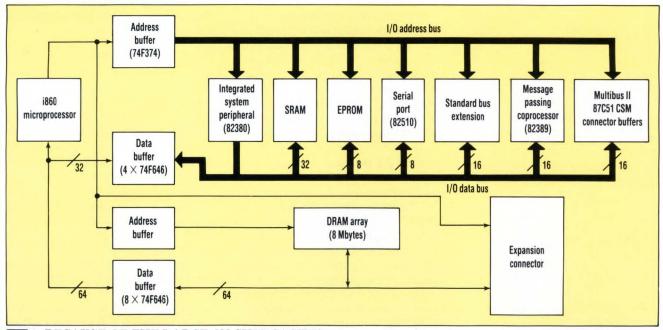
The MPC's local bus interface is like that of any other simple I/O device, consisting of select lines, address signals, and read and write control lines. The coprocessor's registers are accessed by asserting $\overline{REGSEL}$ and the appropriate register address while performing a read or write cycle. Among other functions, the registers program data message transfers, receive and send control transfers, and handle errors.

For DMA interfacing, the MPC has two channels that use the standard DMA Request (DREQ) and DMA Acknowledge (DACK) hardware transfer protocol. The two channels are dedicated to the MPC: one as the input and one as the output. Each has its own control lines and operates independently.

The CPU board includes a static RAM (SRAM) message area that isolates backplane data rates from the processor's local bus. For an outgoing solicited message (data transfer), the microprocessor sends messages to the SRAM at a high rate. The DMA channel then transfers messages from the SRAM to the MPC's outgoing message FIFO buffer. For an incoming solicited message, the DMA channel transfers the message into the SRAM buffer, signaling the microprocessor when the transfer is done. The processor can then quickly transfer the message from the SRAM into main memory.

A DRAM MAIN MEMORY

The i860's large on-chip caches and pipelined architecture make its performance less dependent on a fast—and expensive—SRAM main memory. Instead, the microprocessor's bus is optimized for interfacing directly with DRAMs. The 64-bit wide data bus accepts data on every other clock for read cycles, allowing a longer cycle time between accesses. To further increase the access time without decreasing the bandwidth, the bus accommodates two levels of pipelining, so that up to three cycles

1. BECAUSE OF THE LARGE ON-CHIP CACHES and pipelined architecture of the i860 microprocessor, the CPU can use dynamic RAMs rather than the more expensive static RAMs.

can be outstanding.

To fill a cache line, the processor performs four read cycles *(Fig. 3)*. When the Next Address signal ($\overline{\text{NA}}$) is returned to the microprocessor, the system can accept the next bus cycle. Two $\overline{\text{NA}}$s are returned before any of the cycles are completed. To complete a read cycle, the memory system puts the data on the bus and returns $\overline{\text{Ready}}$ to the microprocessor. When it's fully pipelined, the memory system supplies data and $\overline{\text{Ready}}$ on every other clock. Ordinary static-column DRAMs can deliver this data rate. The processor also supplies a control signal, Next Near ($\overline{\text{NENE}}$), to optimize DRAM control.
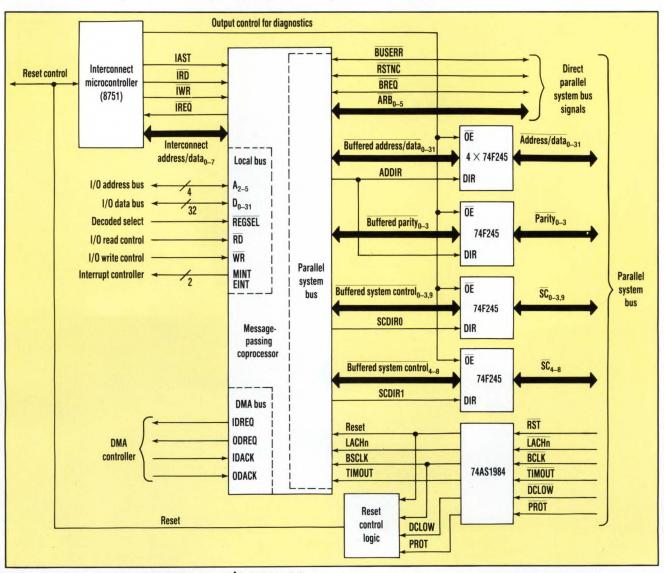
The CPU board's memory system consists of two address latches, eight latching data buffers, and a 64-bit-wide static-column DRAM *(Fig. 4)*. The memories used are 256-kbit-by-4-bit devices, which allow for an incremental system memory size of 2 Mbytes. The use of 4-bit-wide memories reduces power and signal-drive needs.

To accommodate pipelining, both address and data are latched. The address latches hold the address of the previous cycle while the data from the cycle prior to that is held in the data buffers.

Using TTL components on the ad-dress and data paths isolates the memory from the processor's pin timing. The memory system uses two address latches in order to multiplex the row and column addresses from the processor to the DRAM's address lines. When accesses occur within the DRAM page, only the column address needs to be supplied to the memory-address lines.
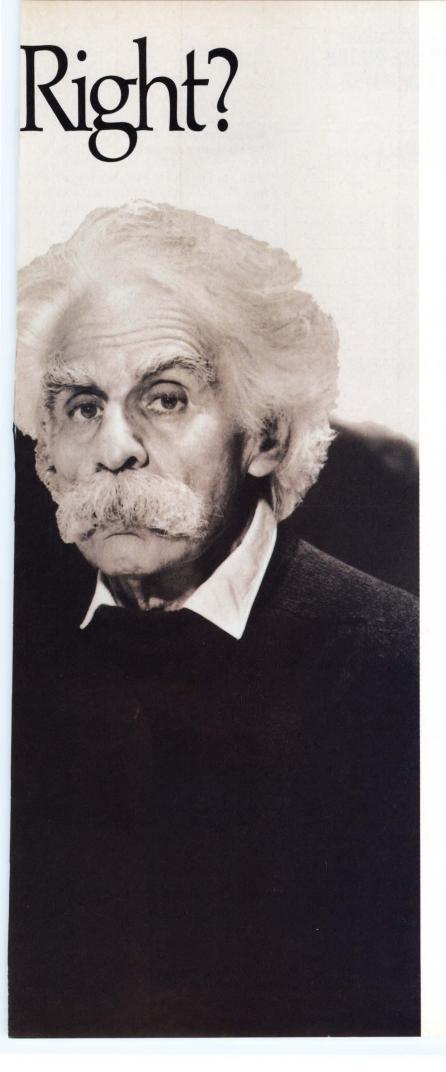
Most systems that use a fast-access DRAM mode need an additional hardware comparator, but the i860 has a comparator built into the bus unit. On each bus cycle the comparator supplies $\overline{\text{NENE}}$, which the controller uses to determine if a fast static-column mode access can occur

■ **2. THE MESSAGE PASSING UNIT'S SIGNALS** can be divided into three major groups that interface with the local bus, the parallel system bus, and the DMA bus.

A Set Is A Set,

Right?

It doesn't take a poke in the eye to figure out that great components don't necessarily lead to a great set.

What does, is what separates Western Digital XT, AT and Micro Channel-compatible chipsets from the rest. And what gives us the performance, compatibility and value we're more or less legendary for.

Consider, if you have a spare moment or two, these facts:

We design our chips with all the right hooks, so you get the kind of design flexibility you've always dreamed of.

We spent years developing our sets and software drivers, so you don't have to spend time doing it yourself.

We give you the ability to buy virtually all your chips from one vendor, so you eliminate incompatibility between chips. Not to mention incompatibility between chip vendors.

We offer unmatched EMI system expertise, so your designs can be close to noise-free. And so can your quality control people.

We manufacture chips by the millions and sell them to just about every big name PC manufacturer in the world, so compatibility is one less thing you have to worry about.

The point is, what you need is what we have.

Storage, Imaging, Communications, and Core logic.

Systems expertise, high volume/cost-effective LSI production, turnkey manufacturing packages, and design support.

It's all designed to work together. It's all from one source. From the IC company that understands systems.
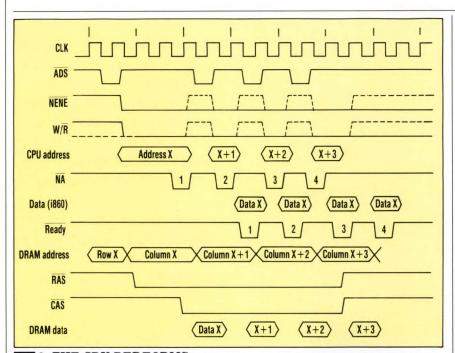
That's right, Einstein. From Western Digital.

For more information or a free poster version of this ad, call 1-800-847-6181. In Canada, call 1-800-448-8470.

Matched sets to match your needs.

WESTERN DIGITAL
Semiconductors-Storage-Imaging-Communications

3. THE CPU PERFORMS four read cycles to fill a cache. When fully pipelined, the memory system supplies data and Ready on every other cycle.

or if a full DRAM cycle must occur.

Bidirectional data buffers latch the data for both reads and writes. For reads, the data is latched and $\overline{Ready}$ is returned on the following clock. With two levels of pipelining, total access time is six clocks and data is available every two clocks.

Write cycles don't need pipelining for zero-wait-state operation. When a write occurs, the address and data are latched in the buffers, making it possible for $\overline{Ready}$ to be returned to the processor. The actual write cycle occurs after $\overline{Ready}$ is returned to the processor. This delayed write operation allows the processor to continue executing even though the write is incomplete.

With 85-ns static-column mode DRAMs for the main memory, the 33-MHz i860 can run at zero wait states for access within the DRAM page. And with the two-level pipelining and two-clock-cycle transfer rate, the CPU board doesn't need an expensive external cache memory.

The board's memory-mapped I/O system consists of an 82510 serial port, the 82380 integrated systems peripheral, one 8-bit boot EPROM, and an SBX connector. The serial port, which can be used in a polled or

an interrupt mode, is also suitable for use as a console monitor. A reduced version of the serial controller's oscillator module clocks the system's timers. A control port enables and disables the timers, whose outputs are connected as interrupts.

PROGRAMMABLE TIMERS

The 82380 serves both as a slave I/O device and as a bus master DMA controller. The peripheral contains four 16-bit programmable timers (8254s), two interrupt controllers (an 8259 master and slave), and eight DMA channels. Five internal interrupts can be used with the DMA channels and the timers. In addition, the device has connections for 15 external interrupts.

Because it uses a double-frequency clock, the 20-MHz 82380 can operate synchronously with a 40-MHz CPU. At reset, a phase clock is generated and used by the control logic for 82380 accesses. Port addressing is handled by connecting pin A_3 of the CPU to pin A_2 of the 82380.

The I/O system uses four of the eight DMA channels: two for the MPC interface and two for the SBX connector. These channels, which can transfer into or out of the SRAM

message area, are programmed with the 82380 in slave mode. Once programmed, the DMA channels become bus masters to complete transfers. To gain control of the bus, the 82380 asserts Hold. When Holda is returned to the 82380, the peripheral initiates the DMA transfer, which continues until completion or until Holda is deasserted.
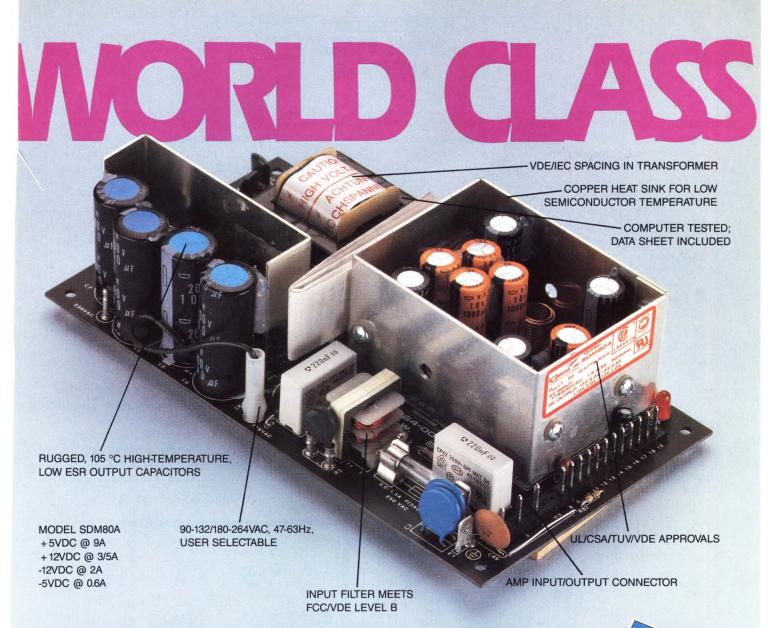
To support the SBX connector, the designer uses several jumpers on the 82380 to configure the DMA control interface as defined in the SBX specification. To access 8- and 16-bit SBX devices, the processor must address them on 8-byte boundaries. The DMA controller performs byte assembly and unassembly from 8 or 16 bits to 32 bits.

As noted, the board uses the SRAM message area to handle DMA transfers with the SBX. DMA transfers may occur in parallel with CPU main memory accesses. Both the DMA controller and the CPU can act as bus masters to access the SRAM and the I/O bus.

The SRAM bank, which is 32 bits wide, connects directly to the I/O data bus, but four data buffers are needed on the processor side. The system only uses the lower 32-bit processor data lines. Though the processor can access the SRAM with zero wait states, it may only access even-word addresses. The processor's automatic-increment addressing mode is used, and the full cycle rate is maintained. The system could handle a 64-bit SRAM bank but the memory would need buffers on the processor side, and the I/O side of the bus would require four additional SRAMs and data buffers.

A programmable logic device (PLD) arbitrates between the two bus masters, granting control of the DMA message system to the 82380 by asserting Hold. If the microprocessor begins a bus cycle that requires the DMA message system, the PLD forces the 82380 from the bus.

Arbitration occurs as follows: When the 82380 asserts Hold, the arbitration PLD returns Holda. The 82380 then takes control of the bus and performs DMA cycles until the

WORLD CLASS

VDE/IEC SPACING IN TRANSFORMER

COPPER HEAT SINK FOR LOW SEMICONDUCTOR TEMPERATURE

COMPUTER TESTED; DATA SHEET INCLUDED

RUGGED, 105 °C HIGH-TEMPERATURE, LOW ESR OUTPUT CAPACITORS

MODEL SDM80A
+5VDC @ 9A
+12VDC @ 3/5A
-12VDC @ 2A
-5VDC @ 0.6A

90-132/180-264VAC, 47-63Hz, USER SELECTABLE

UL/CSA/TUV/VDE APPROVALS

AMP INPUT/OUTPUT CONNECTOR

INPUT FILTER MEETS FCC/VDE LEVEL B

Condor's SDS and SDM Series power supplies meet FCC/VDE Level B and have agency safety approvals!

Want a tough, versatile, well-designed power supply for your next application? Try a single (SDS) or multiple (SDM) output model from Condor!

Every Condor SDS or SDM power supply meets the toughest domestic and international safety requirements, and is UL, CSA and TUV/VDE certified. All units also meet FCC 20870 Level B and VDE 0871 Class B above 150KHz.

SDS/SDM Series features:
- 5 power levels — 45 to 200 watts
- 20 single and 29 multiple-output models

(up to 5 outputs)
- Clean, low-cost, open-frame design
- Fully protected — adjustable current limit, built-in OVP and reverse voltage protection
- Full load burn-in and 2-year warranty
- LED "on" indicator
- Powerfail signal and logic inhibit on 140 and 200W levels
- High peak current disk drive outputs plus closely regulated 3-terminal-type outputs
- Extremely versatile output configurations for tough applications
- Very high value for your purchasing dollar
- Isolated outputs can be used for positive or negative sources or in series with other outputs
- Pass vibration and shock per MIL-STD 810D

Call us today and find out how a Condor SDS or SDM world-class power supply can meet your most demanding design requirements!

Send for our free catalog!

250 power supplies! Switchers and linears! Open frame and enclosed! Custom capability!

CONDOR INC.
DC POWER SUPPLIES

2311 Statham Parkway, Oxnard, CA 93030
(805) 486-4565 • TWX: 910-333-0681
FAX: (805) 487-8911
CALL TOLL-FREE: 1-800-235-5929 (outside CA)

CIRCLE 40

transfer is completed or Holda is deasserted.

If the microprocessor requests the bus, the PLD deasserts Holda and waits for the system peripheral to relinquish bus control by deasserting Hold. This process duration includes the 82380 cycle time and the data bus recovery time of the device being accessed.

Though Hold becomes active again in the next clock, Holda isn't returned to the 82380 until the processor is finished with the bus. When the processor finishes its I/O cycle, it returns Holda to the 82380. For this arbitration scheme to work, the 82380 is programmed in demand mode.

Using an SRAM message area as an I/O buffer gives the CPU design several advantages. For one thing, physical memory is paged in an i860 microprocessor system, and block

transfers are often limited to the page size. But disk access times can be better used if the seek time is amortized over a larger transfer size. The SRAM does this by supplying a continuous memory area where block transfers larger than 4 kbytes can be programmed.
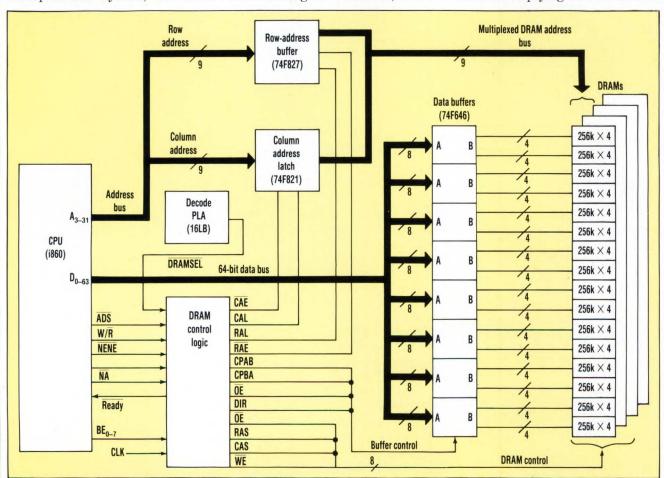
SRAM ENHANCES DMA

Also, the SRAM area enhances DMA performance, which depends on the DMA controller's transfer rate and the effect that the DMA controller has on the processor's memory bandwidth. The relative influence of these factors varies with processor workload. If the processor waits for DMA data, then transfer rate is more important. A multitasking system, however, puts a task waiting for the DMA to sleep and continues to execute other tasks. In a multitasking environment, there-

fore, the DMA's effect on CPU bandwidth is more critical.
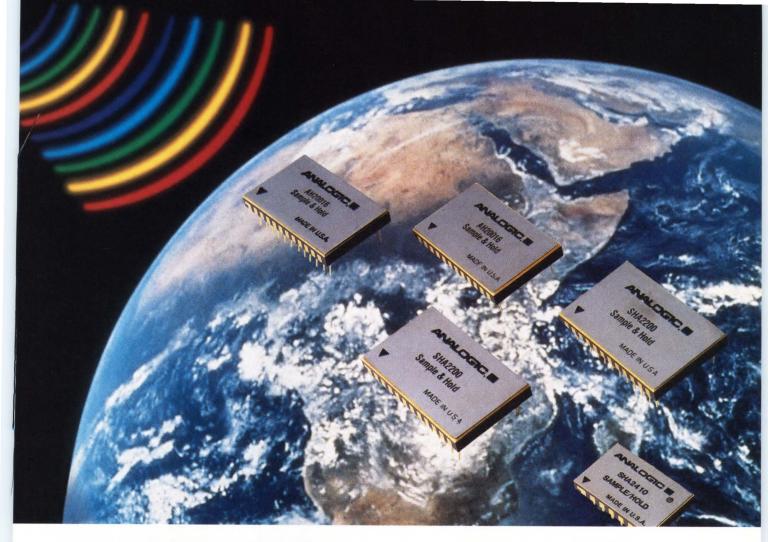
I/O system devices are slow relative to the processor's local bus. Consequently, the board design separates the DMA controller from the processor bus by address and data buffers, allowing DMA memory accesses to occur independently of processor memory accesses. As a result, the processor retains full memory bandwidth during DMA transfers to the SRAM area and may continue to execute tasks. Transfers into the SRAM area, however, require the processor to perform a main-memory data transfer once the DMA transfer completes.
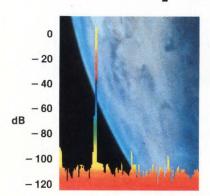
Third, transfers between the SRAM and DRAM areas execute very quickly. In the process, they automatically update the caches. If desired, a special load instruction will avoid emptying the current data

4. THE DRAM MAIN MEMORY needs little glue logic. Power and signal-drive requirements are lowered by the use of 4-bit wide memories.

Analogic Introduces The World's Quietest S/H Amplifiers

High Speed and Precision in Industry Standard Hybrid Pinouts

Analogic, the world resource for precision signal technology, brings you the quietest, fastest precision sample-and-hold amplifiers available. With noise levels as low as 20 μV rms, Analogic's new family of S/H amplifiers surpasses all others for high speed, high resolution signal processing applications.

Just look at these features. For high performance, the AH20016 offers 500 ns acquisition time, low aperture jitter of 10 ps rms, and $\pm 0.0015\%$ linearity. The SHA2200 is ideal for use with fast, high resolution A/D converters, digitizing signals up to 2 MHz with a low noise of only 30 μV rms. Low cost applications are easily supported by the SHA2410 with excellent linearity of $\pm 0.0015\%$, acquisition time of only 2.5 μs and the lowest noise — 20 μV rms. We offer standard pinouts to ease system integration, off-the-shelf delivery, and the high reliability you only get from hybrids!

The speed and accuracy of Analogic's S/H amplifiers will meet the most demanding OEM applications—wideband data acquisition systems, professional audio encoding, digital telecommunications, automatic test equipment, industrial process control, or nuclear research.

And we put our promises in writing. Every Analogic S/H amplifier is tested on proprietary automatic test systems. The test data shipped with each product guarantees that it meets or exceeds the published specifications. Surprised? Anything less is just a lot of noise.

cache contents. The copy can occur at over 40 Mbytes/s at 33 MHz.

Finally, any DMA method must also consider the CPU's write-back caching protocols. To prevent DMA accesses to stale data, a cache flush is needed before a DMA transfer into or out of main memory, or the transfer areas need to be marked as non-cacheable. But because the SRAM address area is never cached, the board requires no additional cache flushing.

Transfers between the I/O and SRAM systems may use a fly-by mode. SRAM reads and MPC writes will then occur together, producing the highest possible DMA transfer rate. Fly-by mode, however, can only be used with 32-bit DMA devices, such as the MPC.

The Multibus II specification defines an initialization sequence for the system. The 8751 microcontroller handles the sequence using the inter-connect space *(Fig. 2, again)*. The microcontroller brings the processor out of reset to start board-level operations.

RESET OUT OF EPROM

Because the i860 CPU has a code size 8 (CS8) reset mode, it can execute out of one 8-bit wide EPROM. As a result, the processor can reset out of the EPROM, initialize the local system, copy a program from EPROM to RAM, and begin execution. But the Reset address is the same as the interrupt address, so once system execution begins, the EPROM must be mapped out of the interrupt address space and replaced by the 64-bit-wide DRAM containing the interrupt service routine.

To enter CS8 mode, the system's reset PLD forces the INT/CS8 pin high. Once the reset routine is complete and the system is ready to operate out of DRAM, the processor dis-ables CS8 mode by clearing a bit in the processor status register. The processor sends a write to the command-port PLD setting a control signal the decode PLD uses to remap the EPROM. The processor can then enable interrupts, because they will trap to the service routine in the DRAM. Once the board exits CS8 mode, it can only be re-entered by resetting the processor.□

Neal Margulis, Intel's chief applications engineer for high-performance processors, is currently writing a book on programming the i860. Margulis has a BSEE from the University of Vermont in Burlington.

How Valuable?	Circle
HIGHLY	559
MODERATELY	560
SLIGHTLY	561

But it's still an old dog.

Introducing System 90™: The first 386 chip set that's more than a tricked-up 286 chip set.

386SX chip sets have been barking up the wrong tree.

To save money, every last one used the tried-and-true, but aging IBM PC architecture. A serious data bottleneck for the 386SX.

We designed System 90 differently, from scratch. The unique architecture interfaces directly with the 80386 microprocessor family. There's no compromise of system speed or IBM PC/AT compatibility.

The complement of standard peripherals runs up to ten times faster on the local bus. The ZyMOS look-ahead memory coprocessor gives you cache-like memory performance (0.1 wait state) with low-cost DRAMs (100ns). In short, you get

applications performance other chip sets claim but seldom deliver.

System 90 cuts production costs to the bone, as well. Just a 3-chip System 90/SX set, 386SX microprocessor, keyboard controller, BIOS ROM and DRAMs do it. No extra VLSI or TTL glue required.

Now, you can offer true 386 performance at entry-level 386SX prices. And you're ready to profit from our soon-to-be-released products for the full 32-bit 80386 family members.

Unleash your 386SX products today with System 90/SX chip sets. Call 800-227-2299 toll-free. Or write: ZyMOS Corp., System 90 Marketing, 477 N. Mathilda Ave., Sunnyvale, CA 94086.

And let sleeping dogs lay.

ZyMOS
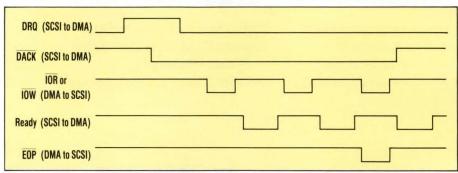
OPTIMIZE TRANSFER SPEED IN ASYNCHRONOUS SCSI

THESE SYSTEMS CAN MATCH SYNCHRONOUS SPEEDS WITH NEW CMOS DEVICES AND AN ENHANCED DMA CONTROLLER.

A synchronous SCSI systems are regarded as poor relations of synchronous SCSI applications and the newer SCSI-2 standard. In particular, the perception is that asynchronous systems can't approach the data transfer rates of their synchronous siblings. Nevertheless, many applications could benefit from increased speed, but they don't need SCSI-2's enhancements and are also cost-sensitive. Furthermore, 95% of the existing SCSI installations are 8-bit asynchronous systems.

Designers can accommodate these applications by building an asynchronous SCSI system based on new CMOS devices that are pin-compatible with components used in older systems. With these devices and some corresponding changes in circuit designs, the transfer rate for asynchronous SCSI can climb from 1.5 Mbytes/s to the synchronous standard of 4 Mbytes/s.

A typical low-cost SCSI application includes a CPU, a DMA controller, a SCSI

■ **1. THE TIMING OF A TYPICAL** 3-byte transfer demonstrates the interaction between a SCSI controller and a DMA controller.

ANDREW M. DAVIDSON
National Semiconductor (UK) Ltd., Larkfield Industrial Estate, Greenock, Scotland, PA16 OEQ, UK; 010 44 475 33733, ext. 5227

ECL Comparators Respond in 1.4ns

Maxim's new line of high-performance ECL and TTL comparators are capable of detecting low-level signals (5-10mV) in 1.4ns. The MAX9685/9690 (Single) and the MAX9687 (Dual) comparators have complementary ECL outputs. The MAX9686 (Single) and MAX9698 (Dual) have TTL compatible outputs.

These high performance comparators offer excellent DC input characteristics and true differential outputs. Maxim's comparators are ideal for high speed applications such as digital signal processing (DSP), video, and medical-imaging. Table 1 lists key parameters and prices for the complete family.

Latch Function Offers mV Resolution

Virtually all level detection techniques utilize a comparator. In the past, available comparators required an extremely high gain (1000) to achieve millivolt resolution (at the expense of speed). Comparators with a Latch Enable option provide millivolt resolution without resorting to extremely high comparator gains, resulting in reduced propagation delays. When the comparator receives a low-level (mV) signal, the input latch pulse acts as a positive feedback and delivers the extra gain required to latch the the output to the level it was "leaning" towards.

Therefore, latch comparators such as the MAX9685/9686/9687 and MAX9698 can accurately discriminate low-level signals at very high speeds.

10ns "ONE-SHOT"

Commercially available high speed "one-shots" encounter problems when generating narrow pulses. They suffer from a delay between the input pulse and the output pulse of as much as 20ns. The output pulse is dependent upon internal delays that vary with temperature. Furthermore, the input pulse must be the same logic

(Please see 1.4ns on back page)
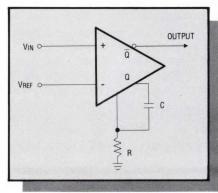
Figure 1. Low-level input custom one-shot (MAX9685 or MAX9686)

Table 1. Complete family of Maxim High Performance Comparators.

DEVICE	DESCRIPTION	PROPAGATION DELAY (TYP)	PRICE (100-UP)
MAX9685*	Latched, ECL	1.4ns	$4.60
MAX9686*	Latched, TTL	6.0ns	$3.00
MAX9687*	Dual Latched, ECL	1.4ns	$6.40
MAX9690	ECL	1.4ns	$4.00
MAX9698	Dual Latched, TTL	6.0ns	$4.20

*Industry standard pin out with improved performance

±75V Fault Protected Multiplexers

Most multiplexer applications involve routing an analog signal while blocking several unselected inputs. Fault protection, especially at the input terminals, is commonly required because of unusually high or unpredictable fault voltages occurring at the inputs or outputs. Maxim's new MAX378/379 fault protected multiplexers offer ±75V of guaranteed fault protection.

Standard CMOS multiplexers like the DG508A/509A require resistors in series with the inputs to limit current when an overvoltage condition occurs at a multiplexer input (Figure 1). Fault conditions, such as power supplies turning off when analog signals are present on the inputs or output, require blocking diodes for current limiting.
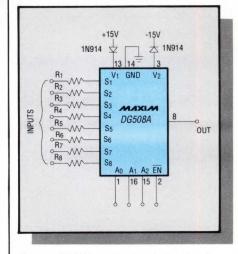

Figure 1. DG508A protected against analog signals which exceed ±15V supplies and analog voltages being present when the power supplies are off.

Maxim's unique voltage limiting structure, first introduced in the MAX358/359 devices and embodied in the MAX378/379, limits the output voltage level to approximately ±1.5V below the power supply rails when an overvoltage occurs. The MAX378/379 and all of Maxim's "Fault Protected"
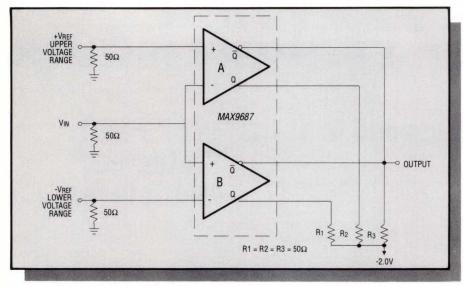
(Please see ±75V on back page)

Figure 2. MAX9687, (Dual) as a high speed window detector

Figure 2. MAX378 shown not requiring protection required by DG508A

1.4ns (cont'd)

level as the desired output pulse--TTL, ECL, CMOS, etc. Consequently, the circuits are incapable of responding to low-level, narrow pulse signals.

The MAX9685/9686 ECL and TTL single comparators are an excellent solution to this timing dilemma in a custom one-shot. As shown in Figure 1, their latch pulse-width can be adjusted by the RC feedback network. The ECL or TTL output logic signal is AC coupled into the Latch Enable input to produce an extension to the response of the short, overdrive signal present at the comparator input.

High Speed Window Detector

The MAX9687 Dual ECL comparator may be utilized to detect high speed signals within a predetermined voltage range. This is vital in applications such as high speed zero crossing detectors or fast tracking A/Ds. The circuit in Figure 2 is designed to swing high whenever the input signal is OUT-SIDE the voltage range and swing LOW whenever the input signal is within the voltage range. If, for example, reference voltages are ±10mV with respect to ground, the comparator will detect a voltage outside the 20mV (±10mV about ground) window *within 2.5 ns.*

±75V (cont'd)

devices offer both overvoltage protection and fault protection without the need for external resistors and diodes (Figure 2). Protection levels are ±60V above the 15V supplies, and ±75V with supplies off. *This provides system designs a significant amount of protection against voltage transients, transducer failures, power loss, and high common mode voltages on signal lines.*

Maxim protected multiplexers maintain a high input impedance under overvoltage conditions, whether they are powered or not. And input current under fault conditions is limited to just a few nanoamps.

The MAX358/359 offers ±35V of protection with a typical on resistance of 1.2kΩ. The MAX368/369 are similar to the MAX358/359 but have latched input lines. The MAX378/379, with protection to ±75V, have a typical ON resistance of 3.0kΩ.
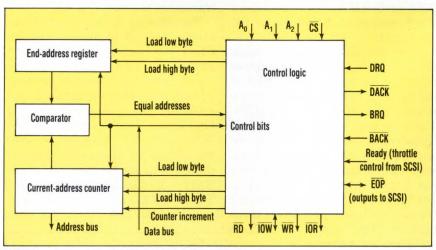
	$R_{DS}ON$	FAULT PROTECTION	PRICE (100-up)
1 of 8 CHANNEL			
MAX358	1.2kΩ	±35V	$7.35
MAX368 (Latched)	1.5kΩ	±35V	7.95
MAX378	3.0kΩ	±75V	13.31
2 of 8 CHANNEL			
MAX359	1.2kΩ	±35V	$7.35
MAX369 (Latched)	1.5kΩ	±35V	7.95
MAX379	3.0kΩ	±75V	13.31

OPTIMIZE
ASYNCHRONOUS SCSI

2. A SIMPLE DMA CONTROLLER contains a current-address register, an end-address register, a comparator, and some control logic.

controller, and some memory. By adding application-specific devices, this core can be either a peripheral controller or host adaptor. Typically, the DMA controller would be an Intel 8257, which delivers a data transfer rate of 1.67 Mbytes/s on a 5 MHz clock, with no wait states. The SCSI controller would be an NCR or AMD 5380-type device with a maximum transfer rate of 1.5 Mbytes/s.

Newer devices, such as National Semiconductor's 5380-compatible DP8490 and Logic Devices' 5380, greatly improve a SCSI controller's transfer rate, but an enhanced DMA controller is needed to handle these speeds. Because no commercially available DMA controller has the required performance, an application-specific controller must be designed.

Designers can implement the DMA controller using 74xxx-type logic devices, programmable logic arrays, or generic logic arrays. For prototyping, benchmarking, and small production runs, a Xilinx XC2018 Logic Cell Array (LCA) is ideal. It offers a quick, easily adaptable way of turning a paper design into silicon and gives designers an opportunity to fine tune the circuit.

The LCA contains 100 configurable logic blocks (CLBs) and 74 configurable I/O blocks (IOBs). Each CLB contains a flip-flop or latch (configurable as either) and a programmable array that can generate any function of four inputs, or two functions of three inputs.

An example of a typical 3-byte block transfer illustrates the interaction between a DMA controller and a SCSI controller *(Fig. 1)*. A DMA Request (DRQ), acknowledged by a DMA Acknowledge ($\overline{DACK}$) initiates the transfer. A Ready signal from the SCSI device acts as a throttle control, going high when the device is ready to transfer data. In a synchronous DMA controller, Ready is used to insert wait states while the SCSI device completes a transfer on the SCSI bus. During the last byte, the End of Process ($\overline{EOP}$) signal is driven low to instruct the SCSI device that the transfer is complete.

When it receives a DRQ, the DMA controller must seize the address and data busses from the CPU, then transfer data when Ready goes high. In a synchronous system, Ready isn't detected until the next active clock edge, causing a delay. In addition, for devices such as the 8257, Ready must be synchronized with the inactive edge of the clock to prevent possible metastability problems. This further increases the latency, as well as the chip count. The optimum design, therefore, is actually asynchronous because it transfers data immediately after a rising edge on Ready.

A simple DMA controller consists of a current-address counter, an end-address register, a comparator, and control logic *(Fig. 2)*. The counter is loaded with the address of the first byte of the block to be transferred, and the register receives the last byte's address. The controller transfers data between the I/O circuitry and the memory address pointed to by the counter.

The counter increments after each transfer until the comparator sees the same addresses in the counter and the end-address register. For bidirectional SCSI transfers, the controller must handle both memory read-I/O write and memory write-I/O read transfers.

For a 16-bit address bus, a 16-bit counter would be ideal, but to save space in the gate array, a smaller counter can be used. The design uses latches in the LCA's input blocks for the page address bits. As a result, decreasing the size to a 12-bit up-counter with a 4-bit page register saved a considerable number of gates inside the device.

This arrangement allows for transfers of 4-kbyte blocks to each of 16 pages. For maximum efficiency, the transfer is made to page-aligned memory. If gates are available and blocks larger than 4 kbytes must be sent, the counter can easily be redesigned to 16 bits.

The end-address register is a 12-bit unit that employs the LCA's input-stage latches. This configuration minimizes internal routing and the use of CLBs.

The counter is clocked synchronously, because a ripple counter would have far too great a settling time on the processor bus. Each bit of the counter receives a clock only when all of the bits below it are high, so the unit's speed is limited by the settling time of each stage. For the Xilinx device, the speed depends largely on routing, with the final version of the counter working comfortably in simulation at 5 MHz.

The outputs of the counter and page register are enabled onto the bus when $\overline{DACK}$ goes active. Therefore, the DMA controller must ensure that it has control of the busses before enabling $\overline{DACK}$.

The DMA controller also contains a 2-bit control register. The control register's least significant bit is the

OPTIMIZE
ASYNCHRONOUS SCSI

Master Enable (MASEN) bit, which must be set high before a DMA transfer can commence. When a transfer is completed, the DMA controller resets MASEN. Thus, the controller must be initialized before each transfer to prevent an unwanted transfer before the address counter and end register have been set up.

The second bit in the control register is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit. If R/$\overline{\text{W}}$ is high, then the transfer is a memory read; if low, it's a memory write.

The bus-exchange logic uses a Bus Request ($\overline{\text{BRQ}}$)-Bus Acknowledge ($\overline{\text{BACK}}$) cycle to get control of the processor bus (Fig. 3a). If the MASEN bit is low, $\overline{\text{BRQ}}$ stays high and no transfer can occur. With MASEN enabled, an active DRQ will issue a $\overline{\text{BRQ}}$ (Fig. 3b).

When the processor sees $\overline{\text{BRQ}}$, it will probably finish its current machine cycle, deassert $\overline{\text{BACK}}$, and three-state the busses and control signals. The exact actions and timings are processor dependent, so the logic retains some flexibility.

Delay Out is normally high. If it goes low, Delay In will go low after a delay time, causing the flip-flop driving Delay Out to be set. The falling edge of $\overline{\text{BACK}}$ causes Delay Out to be pulsed low for a time specified by the delay line. $\overline{\text{DACK}}$ sits high, having been set when $\overline{\text{BRQ}}$ was high, but the rising edge of Delay Out drives it active. When $\overline{\text{DACK}}$ is asserted, the DMA controller takes control of the system busses and control lines.

MASEN is reset on the rising edge of $\overline{\text{EOP}}$, driving $\overline{\text{BRQ}}$ inactive and setting $\overline{\text{DACK}}$ inactive. The processor then asserts $\overline{\text{BACK}}$ and resumes control of the busses. The DMA controller uses $\overline{\text{DACK}}$ to assert control of the bus, because it goes active a delay time after $\overline{\text{BACK}}$ relinquishes the processor's control of the busses. By changing that delay time, users can accommodate processors with different bus-exchange timings.

Connecting the input and three-state control of $\overline{\text{DACK}}$'s output buffer makes it an open collector driver (Fig. 3, again). With this arrangement, users can implement a pseudo-

DMA system if needed to transfer a small amount of data, such as the sense data.
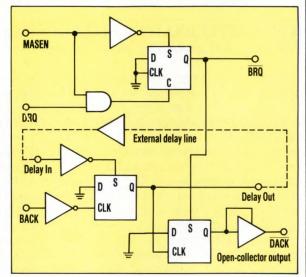
When the DMA controller takes control of the data and address busses, it must also take control of the memory and I/O read and write strobes ($\overline{\text{RD}}$, $\overline{\text{IOR}}$, $\overline{\text{WR}}$, and $\overline{\text{IOW}}$). These signals, which control data transfers between the SCSI device and memory, are driven by three-state output buffers, with the Output Enable driven by $\overline{\text{DACK}}$ (Fig. 4a). Thus, when the controller seizes the address bus, it also drives these signals. The pulse width needed depends on the SCSI and memory devices used, so the control logic includes an external delay line that determines the width of the data strobes.
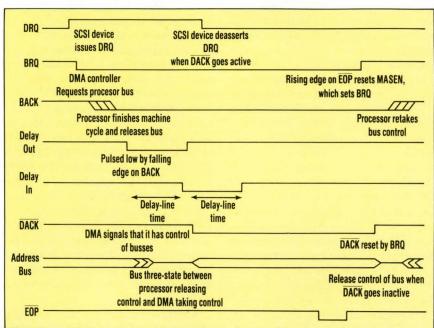
The design uses overlapped memory and I/O strobes, eliminating the need to store data and maximizing the data transfer rate. DRQ triggers the transfer of the first byte of data, and Ready triggers the

transfer of the rest (Fig. 4b).
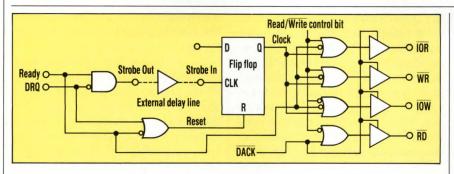
The flip-flop is the heart of the strobe control logic. Its output, Clock, is allowed onto the data strobes only when Ready is high. Before a transfer is ready to begin (that is, with DRQ high for the first byte or Ready low thereafter), Reset is held active. That forces Clock low. When the DMA controller receives the signal to begin the transfer (DRQ going low for the first byte or Ready going high thereafter), Strobe Out has a rising edge, and after the delay-line time Clock goes
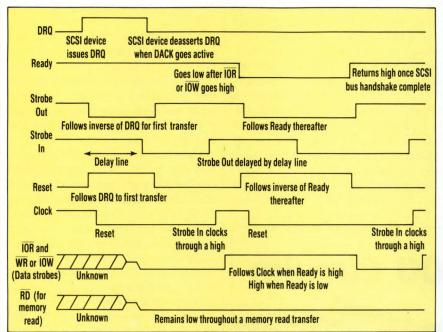
3. TO GAIN CONTROL OF THE BUS, the bus-exchange logic uses a Bus Request-Bus Acknowledge cycle (a). The timing diagram shows the signal interaction (b).

OPTIMIZE ASYNCHRONOUS SCSI

4. THE MEMORY AND I/O READ and Write strobes are driven by three-state output buffers, with the Output Enable driven by $\overline{DACK}$ (a). The overlapped memory and I/O strobes maximize transfer rates by eliminating the need to store data (b).

high. After the first data strobe, Ready is the only external signal that influences the transfer, because DRQ remains low until the next block is to be transferred.

After passing through the delay line, Ready is also used to drive Clock low—this ends the transfer. The amount of time that Ready is delayed by the delay line determines when the back edge of the data strobe occurs and, therefore, the width of the data strobe.

The design maximizes the controller's efficiency by minimizing the time between Ready returning active and the next data strobe beginning. In this case, that time is only the delay through two I/O blocks and one gate. The large delay in toggling the flip-flop can be included in the

the calculation of the size of delay line needed.

$R/\overline{W}$ determines the direction of transfer. If $R/\overline{W}$ is high, a memory read is required, so $\overline{IOR}$ and $\overline{WR}$ are held inactive. If $R/\overline{W}$ is low, a memory write is needed, so $\overline{IOW}$ and $\overline{RD}$ are inactive.

The $\overline{RD}$ logic is simpler than that for the other signals. $\overline{RD}$ can stay low throughout any memory read transfer, constantly enabling the contents of memory pointed to by the address counter onto the data bus. If $\overline{DACK}$ is active and $R/\overline{W}$ is high, $\overline{RD}$ is active.

Though $\overline{IOR}$ and $\overline{WR}$ are shown to be the same signal, in practice it's more efficient to have the two signals logically the same, but $\overline{WR}$ delayed slightly. If the pulses are iden-

tical, each must be wide enough to include the SCSI controller's data access time and the memory's write time. If the SCSI controller has a good enough data hold time, delaying $\overline{WR}$ until the data on the bus is nearly valid means that $\overline{IOR}$ can be deasserted before the write cycle has been completed. This narrowing of $\overline{IOR}$ makes it possible for the SCSI controller to deassert Ready and begin the next transfer sooner.

Clock can be buffered and used to drive the counter's clock signal. The design must ensure, however, that the address counter doesn't start changing until a sufficient address hold time after the back edge of the data strobes. Also, the counter must settle for a sufficient set-up time before the data strobes commence. These timing relationships depend on delays within the gate array and on memory access times.

The comparator checks the output of the address counter against the contents of the end-address register by exclusive NOR-ing the corresponding bits. The result is used to generate $\overline{EOP}$. Internally, $\overline{EOP}$ resets MASEN, thus removing $\overline{BRQ}$, deasserting $\overline{DACK}$, and releasing the busses. Externally, an $\overline{EOP}$ pulse, overlapping an $\overline{IOR}$ or $\overline{IOW}$, signals the SCSI controller that the transfer is complete. The SCSI controller then generates an interrupt to inform the processor that a transfer has occurred.

The $\overline{EOP}$ timing is critical. The overlap required with the data strobe depends on the SCSI controller used, but it should be optimized for compatibility. Because this design uses Clock to generate $\overline{EOP}$, it should be very similar to the data strobe. Clock is only allowed onto the EOP pin if the comparator's output was high the last time Strobe Out went high. To eliminate glitches produced while the address counter is settling, the comparator output passes through a flip-flop.

Because the comparator must settle before the next data strobe begins, Strobe Out is used to clock through the comparator output. As a result, the circuit waits until the data strobe is just about to start before

determining if it is the last byte. This scheme maximizes the time that the comparator has to settle.

The CLB structure influences the comparator's design. Because one block can generate any function of four inputs, it can implement two exclusive NORs and an AND of the result. Four of the bits, however, require an extra stage of logic. Because the counter is only pseudo-synchronous, the first four bits settle fastest, so they received the added gate delay.

In another technology, the comparator would have three four-input AND gates, each input fed by four exclusive NORs. But on the LCA that arrangement would use up too much logic. It also would be slower, because the connection between the exclusive NORs and the AND gates would be through routing, rather than as part of the same CLB.

Upon power-up, the LCA drives the Done/Program (D/P) line low to show that it's not programmed. This signal can hold the processor in a reset state. D/P remains low while the device reads in its configuration data from memory. Each read cycle takes 4 μs, so memory timing isn't a problem. When the configuration is complete, D/P is driven high, allowing the processor to begin its operations.

The design takes advantages of the fact that the XC2018 LCA is pin intensive. The end-address register and page register are wired to the data bus externally, rather than routed internally. This saves on routing and fully uses the IOB structure.

To evaluate the DMA controller's transfer speed, it was operated with a DP8490 Enhanced Asynchronous SCSI Interface (EASI), which is compatible with a 5380-type device. Also, the enhanced mode has a new interrupt architecture and features, such as interrupt-driven arbitration, which improve system performance. The interface has typical data-transfer rates of over 3 Mbytes/s.

Tests showed the width of data strobes generated by connecting Strobe Out directly to Strobe In was about 40 ns, a length sufficient for the EASI. Consequently, using a memory with a 45-ns cycle time means no delay line is needed. Systems with faster gate arrays or slower SCSI controllers would need the delay line.

Two boards were built using the DMA controller described—one configured as an initiator, the other as a target. The initiator constantly cycled through a routine of sending write and read commands to the target. This test setup exercised the transfer of data in both directions.

Using a standard ribbon cable conforming to the SCSI specification, the boards were connected and the REQ/ACK data handshake on the SCSI bus was monitored to determine the transfer rates. The test used three cable lengths: 10 cm, to represent a system with a hard disk connected to the host adaptor internally; 3 m, for a system with several extra peripherals on it; and 6 m, the maximum length defined in the specification.

Over 10 cm, the Initiator Send-Target Receive speed was 3.5 Mbytes/s. For Initiator Receive-Target Send, it was 4.9 Mbytes/s. Over 3 m, the rates measured were 3.1 and 3.9 Mbytes/s, respectively. For 6 m, the corresponding figures were 2.5 and 3.0 Mbytes/s. Note that a SCSI system's transfer rate depends on the direction of the transfer and the propagation delay introduced by the cable.□
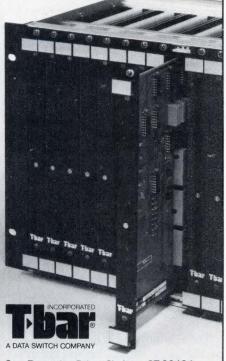
Andrew M. Davidson, a logic design engineer with National Semiconductor's Scottish Design Centre, is responsible for strategic application development for ICs designed by the Centre.

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

DISCRETE COMPONENTS ARE OUT AS THREE CHIPS
INTEGRATE BRAWN AND BRAINS FOR CLOSED-LOOP
SERVOSYSTEM DESIGNS.

CONTROL BRUSHLESS DC MOTORS WITH THREE ICS

Instant response to drive signals, high torque-to-weight ratio, and electrically and acoustically quiet operation are among the unique attributes of brushless dc motors for use in closed-loop servosystems. But until recently, there were no integrated circuits designed to control this type of servomotor. Now, three devices—a power module and two linear ICs—join forces to overcome the limitations of other approaches to controller design.

In the past, such control functions as decoding rotor-position signals from Hall-effect sensors, directional control, overcurrent and undervoltage protection, and overtemperature shutdown were implemented with discrete components. The penalty paid with this approach is excessive circuit-board area, especially if the control unit must be placed within the motor housing.

Another problem was inadequate performance of available power transistors. Bipolar power devices were ruled out because they can't be driven directly by a control IC, and Darlingtons have on-state voltage drops that are sometimes too high for delivering the required voltage amplitudes. Though power MOSFETs are easy to drive, efficient, and inexpensive, they sometimes can't withstand the electrical stresses encountered in pulse-width-modulated (PWM) motor controllers.

Motor drive power comes from the MPM3003 3-phase bridge containing three $0.28\text{-}\Omega$ p-channel power MOSFETs and three $0.150\text{-}\Omega$ n-channel MOSFETs. Housed in a 12-pin power package, the six MOSFETs have a drain-to-source voltage rating of 60 V. The 3003 requires about half of the mounting space needed by six discrete devices housed in TO-220 packages.

Three attributes make these devices more rugged than their predecessors: First, they can withstand greater electrical stress during commutation of their internal source-to-drain diodes. Second, they are less susceptible to failure caused by brief drain-to-source overvoltage transients. Finally, the MOSFETs in the 3003 have 40-V minimum gate-to-source rupture voltage ratings, instead of the standard 20 V. The higher rating improves tolerance to electrostatic discharge and gate-to-source voltage spikes and also extends gate-oxide lifetime at all operating voltages.

KIM GAUEN AND JADE ALBERKRACK
Motorola Inc., 5005 McDowell Rd., Phoenix, AZ 85008; (602) 244-4410.

THREE-CHIP SERVOCONTROLLER
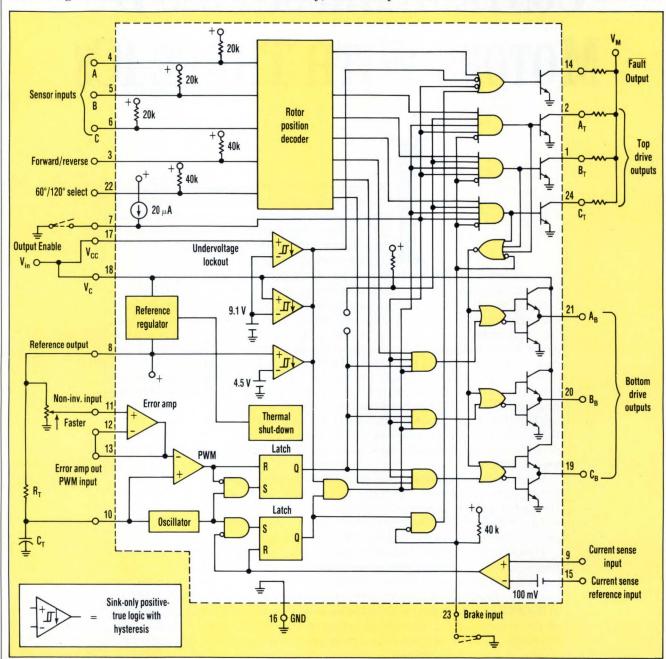
Though the 3003 drives a 1/30-hp motor in this application, it can drive motor sizes up to 1/10 hp. Larger motor sizes require the use of discrete power MOSFETs.

Controlling the MOSFETs that power the brushless dc motor is the MC33035, a 24-pin linear IC that operates as the control center *(Fig. 1)*. The main function of the 33035 is to convert signals from the Hall-effect sensors into signals for electronically commutating the motor. The commutation logic is internally fed to six output drivers, consisting of three open-collector npn transistors that drive the upper legs of the power bridge and three totem-pole drivers that control the lower legs of the bridge. The open-collector outputs can sink 50 mA. With additional external circuitry, these outputs can control either n-channel MOSFETs for higher-power applications or p-channel MOSFETs for a simple interface. With a 100-mA source and sink capability, the three lower totem-pole outputs can directly drive power MOSFETs.

The 33035 IC can also manage several types of faults. A commonly used method for detecting overcurrent conditions is to connect the

1. THE MC33035 CONTROLLER integrates all of the functions necessary for brushless dc motor control, including decoding data from Hall-effect sensors, directional control, and a range of protective mechanisms. It can drive the three lower power-bridge MOSFETs of the MPM3003 directly, and its drivers for the upper three MOSFETs have substantial sink capability.
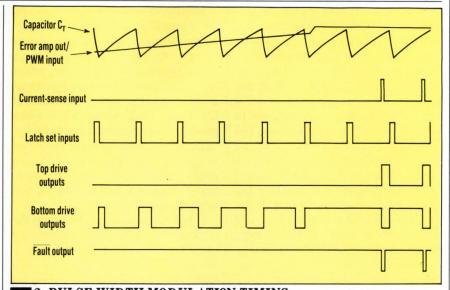
source terminals of the lower three transistors to the negative supply rail through a common current-sense resistor. The sense voltage, which is proportional to load current, is fed into a comparator on the 33035. The comparator then feeds an RS flip-flop, which ensures that the output drivers turn off the power transistors for the remainder of the oscillator cycle upon detection of an overcurrent condition. Without this safeguard the overcurrent protection loop would rapidly cycle on and off about the comparator's threshold, causing excessive power-transistor heating.

The 33035 IC's undervoltage lockout mechanisms terminate the drive to the output transistors under one of three conditions: insufficient IC operating voltage, insufficient gate-drive voltage for the power MOSFETs, or loss of the 6.25-V reference potential. An invalid set of Hall-effect signals or excessive chip temperature will also cause shutdown.

When a fault condition occurs, an npn transistor capable of sinking 16 mA pulls the Fault Output (pin 14) low. This pin can be used to inform a microprocessor of a problem, to energize an LED, to implement a soft-start feature for limiting motor-starting current, or to latch the system off at the first sign of a problem or after a fixed time delay. Resistor R_{11} is sized to maintain about 1 mA in the LED; for a 12-V system, its value should be 1 kΩ.

To inhibit further pulsing of the output transistors under a fault condition, the Fault Output can be connected to the Enable terminal (pin 7). Capacitor C6 creates a fixed latch delay with a time constant determined by the values of C6 and R10.

The 33035 contains most of the circuitry necessary for closed-loop speed control. The only missing function is a tachometer for generating a signal proportional to motor speed. Once supplied with a motor-speed signal, the chip's error amplifier and internal oscillator form the last major links of the control loop. The oscillator frequency is set by an external RC circuit. Each cycle capacitor, C_T, is charged from the reference output

2. PULSE-WIDTH MODULATION TIMING of the top and bottom driver circuits is controlled by the outputs from the 33035's oscillator and error amplifier.

through resistor R_T and then rapidly discharged through an internal resistor. The resultant sawtooth waveform combines with the error-amplifier output to control the upper- and lower-drive outputs *(Fig. 2)*.

The 33035 operates with a variety of Hall-effect sensor spacings about the rotor axis and with most commonly used brushless motor windings. A 33035-based controller is easily altered to drive either delta- or wye-connected three-phase windings with 60° or 120° Hall-effect sensor spacing.

A companion circuit, the MC33039, is a space-saving, inexpensive alternative to a tachometer. This circuit generates a pulse with a fixed duration at each positive or negative transition of the Hall-effect sensors. Filtering the pulse stream gives a voltage amplitude that's proportional to motor speed.

ASSEMBLING THE PIECES

Controller design begins with establishing system timing, which originates in the 33039 circuit. Selection of the timing components for the 33039 is based on the required maximum motor speed *(Fig. 3)*. Because the permanent magnet on the rotor used in this application (Pittman EL-COM 5112) has two pairs of poles, each mechanical degree of rotor displacement is equivalent to two elec-

trical degrees. For one complete rotor revolution each Hall-effect sensor generates two pulses, and three sensors generate six pulses. The 33039 generates 12 pulses per revolution, one for each rising and falling edge of the sensor pulses.

For a given maximum motor speed, the 33039's output pulse width has a maximum limit. For a maximum required speed of 5000 rpm (about 83 rev/s), the 33039 generates 83×12, or about 1000 pulses/s with a maximum pulse width of less than 1 ms. The values for R1 and C1 in this example are selected from the 33039's data sheet to give a maximum pulse width of 950 μs. Similarly, the values for R2 and C2 are determined from the 33035's data sheet to give a nominal PWM frequency of 24 kHz. This frequency is above the audible range, so noise generated by mechanical resonance in the motor windings is not heard.

Both inputs and the output of the 33035's error amplifier are available for implementing various control schemes. For open-loop control, a reference signal proportional to the desired speed can be fed to the error amplifier's noninverting input (pin 11). Its output is compared to the oscillator output with the amplifier configured as a unity-gain voltage follower by connecting its inverting input (pin 12) to its output (pin 13).

THREE-CHIP SERVOCONTROLLER

This obtains a PWM signal proportional to the desired motor speed, unless the control loop is overridden by an overcurrent or fault condition.
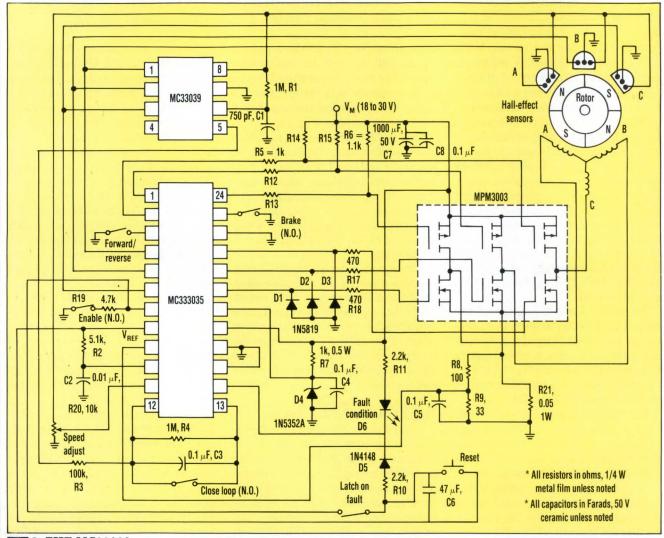
One approach to closed-loop control is to filter the 33039's output (pin 5) with a low-pass filter (R4 and C3) to generate a voltage proportional to motor speed. This signal is then fed to the inverting input (pin 12) of the 33035's error amplifier. A signal proportional to desired motor speed drives the amplifier's noninverting input (pin 11), and the ratio of the input and feedback resistances (R3 and R4) control gain. In this design, feedback capacitor C3 allows for the low-pass filtering and error-generation functions to be combined.

Ideally, the integrator circuit and error amplifier should produce a ripple-free output, even at low motor speeds. However, providing maximum filtering at very low motor speed reduces system response time. In this instance, the time constant for R4 and C3 is 100 ms, which gives good dynamic response and stability. Ultimately, these values are selected to get the best compromise between ripple content and system response time for a given inertia and friction of the load and rotor.

When motor speed falls below the setpoint value, the 33035 extends the output pulse width to the drive transistors. When motor speed exceeds the setpoint, the duty cycle decreases. But if the input signal demands an abrupt and significant speed decrease, the duty cycle goes to zero so that the motor can coast at the lower speed. Because the 33035 doesn't have provisions for rapid deceleration with dynamic braking, the chip is best suited for applications that have a large frictional load or those that don't require a controlled, abrupt deceleration. But an emergency braking scheme can be used.
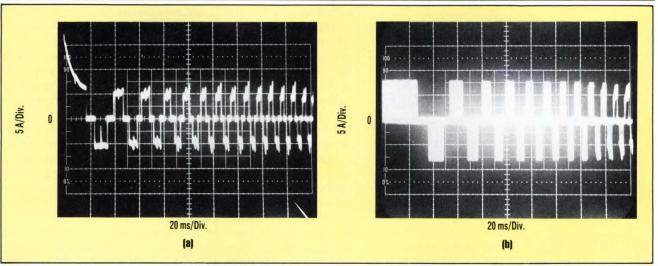
Power-supply voltage amplitude influences how power is delivered to the 33035 IC and how gate-drive supply voltage is generated for the n-channel power MOSFETs. With a 40-V rating, the 33035 can be powered directly from either a 12-V (9-V to 15-

3. THE MC33039 replaces a tachometer by generating a fixed-duration pulse for each signal transition from the Hall-effect sensors mounted in the motor. Proportional to motor speed, the amplitude of the filtered pulse train is compared with the speed setpoint voltage connected to pin 11 of the MC33035 controller. Drive logic within the 33035 adjusts motor speed to remove the error signal.

4. TO AVOID DAMAGING CURRENT LEVELS during motor start-up, the 33035 terminates power MOSFET gate drives at the onset of overcurrent conditions (a.). Without overcurrent protection, start-up current amplitude doubles (b).

V) or 24-V (18-V to 30-V) system supply voltage free of large voltage transients. To minimize local spiking across the dc bus, a large electrolytic capacitor (C7) and a small filter capacitor (C8) should be located close to the IC.

For minimum power dissipation in the 33035, the three lower output transistors can be driven by an independent power supply. This is done by tying pin 18 (V_C) to that supply instead of connecting it to pin 17 *(Fig. 1, again)*. The only drive current required for the MOSFETs is that needed to charge and discharge each device's gate-to-source and drain-to-gate capacitances. The lower n-channel devices require roughly 15 nC of gate charge to reach a gate-to-source voltage of 15 V. At a nominal PWM frequency of 24-kHz, the required average drive current for all three n-channel devices is only 0.36 mA. Because the charging current for the three p-channel MOSFETs is delivered directly from the dc bus, this charge isn't included when sizing the impedance of the gate-drive bus voltage.

Though the average current drawn by the MOSFETs is relatively small, charging their input capacitances takes high peak currents. Therefore filter capacitor C4 essentially supplies the entire turn-on current and is refreshed through resistor R7 *(Fig. 3, again)*. When the sup-

ply voltage dips to the low end of its range (18 V for a 24-V system), R7 has only 3 V across it. However, it will still supply ample current to keep the capacitor charged while supplying at least 1 mA to the zener diode to ensure good regulation. At high supply voltages, the resistor drops 15 V, passes 15 mA, and dissipates about 0.25 W. A 0.5-W power rating is adequate for both the resistor and the zener diode. For a 12-V supply, the resistor can have a 0.25-W rating.

Capacitor C4 should be large enough to deliver the entire gate charge for a single cycle without a significant voltage dip. Because a MOSFET essentially draws no drive current during the on state, the output duty cycle doesn't significantly effect average current. Capacitor C4 can be eliminated if resistor R7 is small enough to satisfy gate-drive requirements at any instant. The penalty, however, is higher losses in the zener diode and series resistor, requiring devices with greater power ratings.
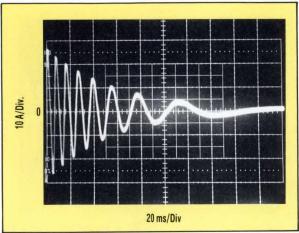
The gate drive deserves two other considerations. First, the IC sees the MOSFET as a capacitor in series with a parasitic inductance, most of which is in the current-sensing resistor. Rapid switching produces transients and ringing in the gate-drive loop. Voltage spikes on the gate drives greater than 0.7 V below

ground can forward-bias the substrate of the 33035. Three Schottky diodes (D1, D2, and D3), one from each lower-drive output to ground, are needed if substrate current exceeds 50 mA.

Problems may also arise if the gate-drive impedance of the three lower drives is too low. With little or no resistance between the 33035 and the MOSFET, the gate-drive loop may cause ringing during gate voltage transitions. Such ringing is amplified by the MOSFET and may cause excessive noise at the drain. The problem is solved by reducing the circuit's Q (ratio of reactance to resistance at a given frequency) by inserting a series resistor, whose minimum value depends on circuit parasitics. The resistance required to keep switching losses reasonably low is usually much larger than the resistance required to eliminate oscillations. In this circuit, gate-drive resistors with values less than 62 Ω cause problems.

A second reason for avoiding very fast turn-on of the n-channel MOSFETs is the possibility of generating EMI. When a lower MOSFET turns on, the drain-source diode of the p-channel device in the upper leg of the same half-bridge has been conducting current. Reverse recovery charge is swept out of the diode by the lower switch. If turn-on speed is high, EMI is generated by large re-

THREE-CHIP
SERVOCONTROLLER

10 A/Div.

20 ms/Div

5. THE BRAKE PIN of the 33035 should be used with caution because overcurrent protection isn't available in this mode of operation. Power MOSFETs must be sized to handle high surge currents, which ring between the motor windings until the kinetic energy in the spinning rotor is extinguished by power-dissipating circuit elements and frictional loading.

verse currents and rapid drain-to-source voltage swings.

A 24-V system supplies ample voltage for driving the MOSFET gates. Resistors R5 and R6 are sized to ensure that the p-channel devices receive –10 V of gate drive even when the supply voltage drops to 18 V. Resistors R5, R12, and R13 govern the charge rate of the p-channel input capacitances and thus control turn-on speed. Similarly, R6, R14, and R15 determine turn-off speed. Using lower resistance values in the voltage divider maintains the –10-V gate drive while decreasing gate-drive impedance, but at the expense of increased current and power dissipation in the resistors.

A common pitfall in the design of a p-channel drive is to assume that because the devices are switching at the motor's commutation frequency (which is much lower than the PWM frequency), they don't need the low-impedance gate drive required by the n-channel devices. However, when the drain-to-source voltage changes (due to the 20-kHz-plus switching frequency of an n-channel MOSFET in the lower legs of the bridge), the upper gate drive must charge and discharge the p-channel's gate-to-drain capacitance. With insufficient gate drive, the p-channel device will turn on briefly, causing

shoot-through currents that increase switching losses dramatically. High-voltage brushless-motor systems are especially prone to gate-drive problems because the excursions in V_{DS} are so large.

Shoot-through currents are avoided by increasing n-channel turn-on time to limit dv/dt and by minimizing the p-channel gate-drive impedance, especially in the off-state. In this application, adding a 0.01-μF p-channel gate-to-source capacitance provides the gate drive a reservoir of charge that keeps the gate off when the gate-to-drain capacitance demands displacement current.

When a 12-V supply is used, the full supply voltage is impressed across the gate and source terminals when a MOSFET is turned on. This is done by shorting or eliminating pull-down resistors R5, R12, and R13. With the absence of gate-current-limiting series resistance, turn-on speed is much faster than turn-off speed.

SENSING OVERCURRENT

The 33035 uses a comparator circuit to detect excessive load current. A signal from current-sensing resistor R21, which is common to all the n-channel sources, is fed to the comparator's current-sense input (pin 9). The sense voltage is attenuated by a divider (R8 and R9) which sets the current trip point at 8 A. The comparator's trip threshold is internally set to 100 mV. For a higher trip voltage, an additional offset voltage can be connected to the comparator's current-sense reference input (pin 15). Capacitor C5 connected across the comparator's input prevents spurious signals, such as reverse-recovery spikes from free-wheeling diodes, from tripping the overcurrent comparator. The time constant of

this resistance-capacitance network is equal to the parallel combination of R8 and R9 (24 Ω) times 0.1 μF, or 2.4 μs. Because power MOSFETs can withstand high surge currents, especially with durations under 10 ms, this time constant gives adequate protection.

The benefit of overcurrent protection is apparent in a comparison of motor start-up current waveforms *(Fig. 4)*. With no current feedback, the start-up current peaks at 16 A; with feedback, the current is limited to 8 A.

Another potentially stressful condition occurs when the motor abruptly changes its direction of rotation. Without overcurrent sensing, motor current is limited only by the motor's winding resistance and the power MOSFETs' on voltage. The braking mode also generates high current. Applying the brake signal turns on all three bottom MOSFETs to short-circuit the motor windings. Because braking current circulating between the windings through the three n-channel devices doesn't flow through the sense resistor, the 33035 can't detect high currents in the brake mode. Therefore, the MOSFETs must be sized to handle very large currents if the brake is used.

Current peaks can reach 35 A during braking and last long enough to stress the power transistors *(Fig. 5)*. Peak current during braking is a function of the resistance of the power transistors and motor windings, and the motor's back EMF. The time required for the current to decay depends on motor speed, motor winding resistance, frictional loading, and motor inertia.□

Kim Gauen, a senior applications engineer at Motorola, holds a BSEE from the University of Missouri at Rolla.

Jade Alberkrack, a senior staff engineer at Motorola, holds six patents.

How VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

524 CHARGE BATTERIES AT ANY TEMPERATURE

DAVID SHERMAN
David Sherman Engineering Co., 727 33rd Street, Everett, WA 98201;
(206) 258-4083.

THE LP2951 OFFERS MOST OF THE FUNCTIONS needed to supply a temperature-compensated constant voltage. In turn, this constant voltage charges the batteries.

A simple modification to a standard monolithic voltage regulator can deliver the temperature-compensated constant voltage required to charge lead-acid batteries. The charging voltage varies linearly from 15.5 V at –20° C to 14.1 V at +50° C. The values are for a 6-cell (12.6-V) battery. By changing resistor values, the circuit can work for other battery voltages.

National Semiconductor's LP2951 offers various functions that include voltage reference, error amplifier, series-pass element, current limit, and overtemperature shutdown *(see the figure)*. This device was chosen to regulate the voltage because of its low quiescent current, low dropout voltage, and high-impedance feedback input. The feedback loop acts with the internal bandgap reference to maintain a voltage of about 1.23 V at pin 7. Because the current into this pin is small, a constant 12 μA flows into R_1, independent of temperature. The collector current of Q1 is also 12 μA, neglecting the small current (less than 1 μA) of R_2.

The temperature coefficient (TC) of V_{BE} in a silicon transistor operating at constant collector current is –2 mV/°C. To achieve the desired charging voltage compensation, an output-voltage TC of $(14.1 - 15.5)/(50 - (-20)) = -20$ mV/°C is required. An MPSA-18 transistor is used in a V_{BE} multiplier circuit with a multiplication factor of ten to get the required TC. The MPSA-18 maintains a beta of several hundred with collector currents in the μA range. R_4 creates a constant voltage drop, which is added to the 1.23-V reference and V_{BE}, to set the charger's final output voltage.

This configuration makes it easy to customize the output voltage and temperature coefficient independently. Once the desired TC is known, R_2 and R_3 can be calculated. Then R_4 can be determined to obtain the final output voltage. If precise control of the output voltage is required, R_4 can be varied without affecting the output's TC. If more precision is required, R_2 should be partially adjustable to set the TC. In addition, all of the resistors should be low TC metal-film types.

When no input is present, D1 isolates the regulator from the battery to prevent excessive current drain. In this mode, the current drain on the battery is determined primarily by $R_3 + R_4$. The circuit is also suitable for charging a sealed lead-acid battery from an outdoor solar panel where varying temperatures and irregular charging conditions are expected.□

IFD WINNERS

July 13, 1989
Harold J. Weber, P.O. Box 6161, Holliston, MA 01746. His idea: *"Parasitic Supply Offers DC Power."*

July 27, 1989
Len Sherman, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086. His idea: *"Efficient 5-V Supply From Batteries."*

VOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

---

525 BUILD A REGULATOR WITH FEW PARTS

JERRY STEELE
Thaler Corporation, 10940 North Stallard Place, Tucson, AZ 85704;
(602) 742-5572.

Voltage references can create accurate and temperature-stable regulated power supplies with little external componentry. This achievement overcomes the stability and accuracy limitations often seen in conventional voltage-regulator ICs. Initial accuracies of ±0.01% and temperature coefficients less than 1.5 ppm/°C

THE VRE135 VOLTAGE reference supplies access to the feedback network and eliminates all of the unnecessary external components at the same time.

over the full military temperature range are attainable using this approach, which means that the regulator can operate at an accuracy within 0.0833% of 15 V under any conditions.

Minimizing the amount of stability circuitry involves selecting the proper reference. The Thaler VRE135 is a ±15-V reference for high-current designs. This reference doesn't require additional circuitry for applications up to 60 mA, and it easily lends itself to higher-current applications without adding a lot of extra componentry.

The feedback network and the phase margin make the VRE135 suitable for regulator applications. With access to the feedback network, users can keep the buffer within the reference voltage range to maintain high accuracy. And the VRE135's phase margin is high enough to ensure stability without the extra components.

A sample circuit includes a 2N3054 pass transistor and it's complement for the negative half, 2N4912 *(see the figure)*. The resulting current capability is 60 mA times the transistor's H_{FE}, which, in some cases, can be as low as 20.

In the event of short circuits, protection should be added to the pass transistor. If a current-limited source with reasonably safe supply limits is used, no further protection is necessary. Resistance in the collector circuit can also be considered for current-limiting purposes unless it cuts off the pass element's voltage supply under normal operating conditions.

The reduced base current of Darlington pass transistors improves reference performance and raises output-current capability by several orders of magnitude. Currents as high as 30 A can be supplied by using just a single reference circuit and one Darlington transistor. And this type of circuit doesn't require any additional components to ensure stability up to 2 A. But if it is being used for higher-current applications, a foldover current-limiting circuit might come in handy.

The VRE135 can accept higher output voltages by making some simple modifications. A divider circuit on the output of the pass device or buffer can obtain any value of voltage higher than the reference. This voltage originates in the regulator.

The biggest obstacle to overcome is constructing a divider that's stable enough to meet the 1.5 ppm/°C temperature-coefficient requirement. A power op amp can also supply both current pull-up and pull-down capability, which improves regulator transient response. □

526 RS-232C TRANSMITTER POWERS LEDS
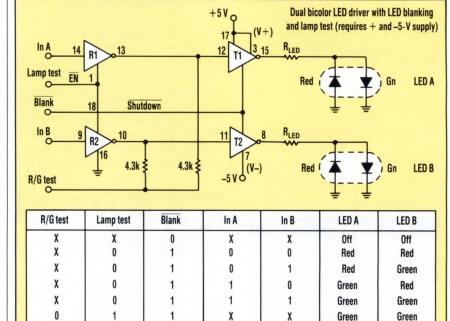
DON SHERMAN

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

Recently, there's been some light shed on the MAX232 RS232 transceiver chip that can double as a bicolor light-emitting (LED) driver. The advantages of the MAX232 aren't obvious when used in this capacity, though. It can configure a circuit that uses
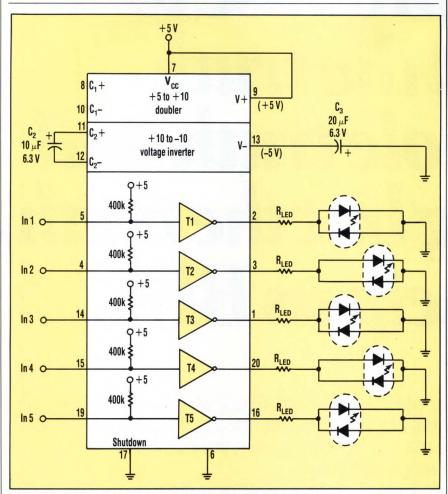
R/G test	Lamp test	Blank	In A	In B	LED A	LED B
X	X	0	X	X	Off	Off
X	0	1	0	0	Red	Red
X	0	1	0	1	Red	Green
X	0	1	1	0	Green	Red
X	0	1	1	1	Green	Green
0	1	1	X	X	Green	Green
1	1	1	X	X	Red	Red

1. IN THIS LED-DRIVER CIRCUIT, the chip's V+ terminal connects directly to the +5-V supply, and the V− terminal connects to an external −5-V supply. In this configuration, the chip's internal voltage inverter and doubler circuits aren't being used.

2. USING THIS METHOD of supplying an LED-driving output voltage, the V+ connects to the +5-V supply with no capacitors connected to the +5 to +10 voltage-doubler circuit.

only one transmitter per bicolor LED. Furthermore, the circuit has the ability to blank the display (by turning off the LEDs) and supply a test-mode operation that forces a red or green color to appear on all the LEDs.

The new driver IC includes a dual-transmitter and dual-receiver circuit, plus transmitter three-state and separate receiver three-state controls.

Several methods of supplying the driving voltage to the transmitter outputs are available. Using one of the methods, V+ is connected directly to the +5-V supply, and the V− terminal is connected to an external −5-V supply. Here, the chip's internal voltage inverter and doubler circuits aren't used.

An LED current-limiting resistor,

R_{LED} in this case, makes sure that the proper current is fed to the LEDs; the internal resistance of the circuit's output driver (Tx) is usually sufficient with the 5-V supply *(Fig. 1)*.

The output voltage can also be supplied to the transmitter outputs when the V+ terminal connects to the +5-V supply, with no capacitors connected to the 5 to 10 voltage-doubler circuit *(Fig. 2)*. In this case however, the +10 to −10 V inverter does connect to capacitors C_2 and C_3. These capacitors invert the voltage signal on pin 9 (V+). Because V+ is merely 5 V, the V− voltage will be just −5 V from the inverter circuit. Of course, the power-supply arrangements employed in the two circuits can be interchanged without any ill effects.□

PRODUCTS NEWSLETTER

WORM Optical Drive Packs 940 Mbytes

Phase-change recording packs a total of 940 Mbytes per cartridge in the LF-5012 write-once, read-many optical disk drive from Panasonic's Memory Systems Division, Milpitas, Calif. The WORM drive uses removable, double-sided media with a formatted capacity of 470 Mbytes per side. Compatible with the IBM PC/AT and Apple Macintosh, the drive features a SCSI interface and a 90-ms random access time. Data is transferred at 2.5 Mbytes/s at a corrected bit-error rate of less than 10^{-12}. Prices are negotiable. Contact Tony Tokunaga, (408) 262-2200. DM   **CIRCLE 301**

IC Op Amp Puts ±10 V At 20 MHz Across 200 Ω

Designed to handle ultra-wideband video signals, such as those expected for high-definition TV, the EL2030 IC op amp from Elantec, Milpitas, Calif., typically slews at 2000 V/μs, and 1200 V/μs is guaranteed. That translates to a minimum full-power bandwidth of 20 MHz for 20 Vpk-pk sine waves across 200 Ω. Small signal (3-dB) bandwidth at a closed loop gain of 1 is 120 MHz; at a gain of 2, it's still 110 MHz. Settling time to 0.25% for a 10-V step is 40 ns. Open loop gain runs a minimum of 60 dB, and differential gain and phase (TV specifications) are respectively 0.01% peak gain and 0.01°. The chip's performance is a function of its current-mode feedback architecture and its dielectrically isolated (DI) process. Output current is 65 mA maximum. With that much speed and power, quiescent current is just 17 mA. In a plastic miniDIP, unit prices in quantities of 100 start at $3.35. Devices are in stock. Contact Barry Siegel, (408) 945-1323. FG   **CIRCLE 302**

Get Analog Data From Bulletin Board

You can now dial up Burr-Brown in Tucson, Ariz., on your modem to get the latest information on the company's products, application tips and notes, and software utilities and updates. The data pertains to all company system products, such as intelligent analog I/O boards and VME-bus based DSP workstations, along with such Burr-Brown components as IC op amps and audio data converters. Any popular communications software, such as PROCOMM, BITCOM, XTALK, or Red Ryder, can be used. Callers will get a simple menu-driven interface designed for browsing. The access number is (602) 741-3978. Communications settings are 300/1200/2400 8-N-1. The XMODEM protocol is used. For more information, call Ed George, (602) 741-4378. FG   **CIRCLE 303**

±35-V, 10-A Op Amp Comes In Power SIP

Also from Burr-Brown, the OPA541 power op amp comes in an 11-pin plastic, single-in-line (SIP) power packages. Until now, this single chip—which can put a 45-kHz, 70-Vpk-pk sine wave across 8 Ω—was only available in an 8-pin metal TO-3 type package. Other specifications include a small-signal unity-gain bandwidth of 1.6 MHz, a slew rate of 6 V/μs, and an open-loop gain of 90 dB. The op amp will drive a 3.3-nF load connected for a closed-loop gain of unity. Offset voltage is just 1 mV, and offset drift is 30 μV/°C. The bias current of this JFET input device is just 50 pA. In quantities of 100, unit prices start at $9.95. Call Jason Arbanus, (800) 548-6132. FG   **CIRCLE 304**

Second Source For Low-Bias Current Op Amps

If you use the OPA111 or OPA121, two of the few precision, low-bias current op amps, you now have a second source—Sipex' SP111 and SP121. Like the Burr-Brown parts, these are built on a dielectrically isolated process. Furthermore, both employ very low noise JFET input stages and their specifications are similar. The SP111-A includes a maximum bias current of 2 pA, a maximum offset-voltage shift of 5 μV/°C, and maximum voltage noise (from 10 Hz to 10 kHz) of 1.2 μVrms. For the premium SP111-B, these specifications are respectively 1 pA, 1 μV/°C, and 1 μVrms. SP121-A and -B bias currents run 5 and 10 pA (maximum), respectively. Unit prices in quantities of 100 for the SP121s start at $2.87 for commercial grade devices. Sipex is located in both San Jose, Calif., and Billerica, Mass. Contact Gary Hahnert, (408) 473-8817. FG   **CIRCLE 305**

Brushless DC-Motor Driver Puts Out 3A

Designed to drive three-phase brushless dc motors in streaming tape and Winchester memories, each of the three channels of the UDN2932 from Sprague, Worcester, Mass., handles ±3.5 A peak and 2 A continuously from its 15-V (sustaining) totem-pole outputs. Saturation voltage, sinking 2 A, is 700 mV maximum; sourcing the same current, the voltage rises to only 1.3 V. The chip in its single-in-line power tab package translates logic-level pulse-width-modulation signals to the motor drive. The emitter of each sink driver is available for current sensing in a PWM loop. Protection circuitry includes thermal shutdown (with hysteresis) at 165°C, circuits that keep sink and source drivers from being on simultaneously, and high-current output clamps and flyback diodes. In quantities of 1000, unit prices start at $2.89. Call Mark Heisig, (508) 853-5000. FG   **CIRCLE 306**

PRODUCTS NEWSLETTER

GET OP AMPS WITH 1-pA BIAS FOR UNDER $4 For just $3.75 each (in quantities of 100), the AD546JN IC op amp from Analog Devices, Wilmington, Mass., offers a bias current of less than 1 pA. In addition, its sibling, the 546KN specs its bias current at half that (0.05 pA) and costs a mere $4.50 each. Such devices, which now come in plastic for the first time, can lower the cost of typical electrometer applications (from pH meters to blood analyzers). Designers can afford to use one op amp per channel in systems that multiplex the input to one op amp. Offset voltage is a maximum of 2 mV and noise from 0.1 to 10 Hz is typically 4 μVpk-pk. Quiescent current is just 0.7 mA. Call application engineering, (508) 658-9400. FG **CIRCLE 307**

RELAY SWITCHES SIGNALS FROM LOW LEVELS TO 300 V Analog signals from thermocouple levels to 300-V peak can be switched with an output capacitance of 3 pF, an off-state resistance of 10^{11} Ω, and 25-μs response time by a photovoltaic ac relay from International Rectifier, El Segundo, Calif. The PVA3055 relay, which comes in an 8-pin DIP, is a single-pole, normally open device. It can switch analog signals in the rf range at up to 25 kHz. In operation, the relay uses the company's BOSFET, a bidirectional ac- or dc-output power-MOSFET IC, which is controlled by a photovoltaic generator energized by radiation from an isolated LED. Only 3 mW of pickup power is required with an input-current range of 2 to 25 mA dc. In quantities of 1000, the PVA3055 relay goes for $3.65. Call Stan Schneider, (213) 607-8899. DM **CIRCLE 308**

MINI PHOTOCOUPLERS MOUNT LOW ON BOARDS Significant space savings, compared with standard DIPs, are offered by a line of photocouplers in mini flat packages from Toshiba America Electronic Components, Irvine, Calif. Surface-mounted in their small-outline packages, the devices are functionally equivalent to devices that come in a standard DIP but are 60% smaller. As a result, the devices suit high-density applications. Manufacturing costs are cut, too, because through-hole mounting requirements are eliminated. Samples are available now, with delivery in 12 to 16 weeks. Production is scheduled for October. DM **CIRCLE 309**

ARCNET CHIP FAMILY ADDS PC/AT INTERFACE The industry's first Arcnet chip to interface with PC/AT systems is one of two chips recently added to the Arcnet family from NCR's Microelectronics Products Division, Ft. Collins, Colo. The 90C198 Arcnet controller and transceiver chip is targeted at 16-bit cards; the 90C126 features a PC/XT interface and is aimed at 8-bit cards. Both use the 90C98A core and improve performance with new arbitration logic that reduces wait states. Buffer chaining leads to improved system throughput in file-server applications. The chips include all RAM, ROM, and I/O decoding, as well as support for multiple reset options. Both come in 68-pin packages. In quantities of 5000, the 90C198 goes for $20 and the 90C126 costs $16. Samples are available now. Call (800) 334-5454. DM **CIRCLE 310**

EMULATOR SIMPLIFIES Z180 SOURCE-LEVEL DEBUGGING An in-circuit emulator for the Zilog Z180 microprocessor makes source-level debugging possible in both C and assembly language. The Z180 IceAlyzer from Softaid, Columbia, Md., works with the company's companion debugger to support a number of popular C compilers, including those from Manx and Archimedes. Any assembler can be used. The Z180 IceAlyzer includes 64k hardware breakpoints that work at up to 10 MHz with no wait states. The unit handles fetch, read, and write breakpoints. A real-time trace buffer captures each machine cycle as it executes, and the trace can be qualified by address to capture only desired routines. Available from stock, the Z180 IceAlyzer costs $3090; the source-level debugger costs $750. Call (800) 433-8812. JN **CIRCLE 311**

SIMULATOR TEAMS UP WITH SYNTHESIS TOOLS The ToolKit ASIC-design tool from Ikos Systems Inc., Sunnyvale, Calif., couples Ikos' fast hardware simulator with the synthesis capabilities of the Design Compiler and HDL Compiler from Synopsys, Mountain View, Calif. Synopsys users can synthesize an HDL description into Ikos-compatible gate-level net lists. The resulting circuit is quickly simulated on a hardware-based Ikos simulator. The ToolKit contains two libraries—one for the Synopsys Design Compiler, and one for the Ikos simulators. Each library contains the functional data for more than 80 basic cell types, including registers, latches, flip-flops, and simple Boolean gates. With this approach, the simulators can be used early in the design cycle for system-behavior verification, and at later stages for full-timing logic and fault simulation. Ikos will market the ToolKit and Synopsys will supply the technical assistance needed for Ikos to verify and maintain the libraries. The ToolKit, with documentation, costs $15,000. Call Lois DeBois Carroll, (408) 245-1900. LG **CIRCLE 312**

EDITED BY CLIFFORD METH

■ **1. PUTTING OUT ±500 V** and ±75 mA, the Apex PA89 op amp has an open-loop gain of 108 dB. All of the active and passive devices forming this hybrid are mounted on an isolating beryllia substrate.

HIGH-VOLTAGE OP AMP PUTS OUT ±75 MA AT ±500 V

FRANK GOODENOUGH

You don't have to build your own super-high-voltage op amps anymore. The PA89 from Apex, a multichip hybrid operating with split 550-V supplies, can put a ±500-V square-wave across 6800 Ω *(Fig. 1)*. The load impedance may appear somewhat high until you realize that ±75 mA is also put through the resistor for a continuous power of 38 W.

The PA89 is a true op amp: It has a minimum open-loop gain of 108 dB and can handle any common-mode voltage up to 30 V within either supply rail. Moreover, the voltage between the supply pins can vary between 100 and 1200 V, which means that this amp can operate with 1100 V on the positive supply pin and –50 V on the negative pin (or in an active, shutdown mode with just ±50-V rails).

The PA89 was developed to drive ceramic, piezoelectric transducers known as micropositioners—not as you might expect for sonar applications. These transducers, which are assemblies of one or more individual pieces of piezoelectric ceramic, can produce precise increments of motion (for a light load) from microinches to tens of mils with response times on the order of microseconds *(see "An update on piezoelectric ceramic transducers," opposite)*.

The op amp's safe operating area (SOA) has no secondary breakdown limitations. With an appropriate current-limiting resistor, it can drive all types of loads.

The PA89 isn't unity-gain stable; it requires external compensation to operate at closed-loop gains below 20 dB. But this isn't a problem, because virtually any driver application will take a signal of up to ±10 V and gain it up about 50 times. Gain-bandwidth product at 1 MHz is 2 MHz. When the op amp is externally compensated for stability at unity gain, small-signal bandwidth is 200 kHz. Gain and bandwidth are specified while driving 10 kΩ.

The op amp isn't suited for most deflection-amplifier applications because it features a slew rate at a gain of 100 of a minimum of 30 V/μs, which translates into a full-power bandwidth of only 3 kHz (at 30 V/μs, it takes 30 μs to slew from –450 to +450 V). However, settling time for a 10-V step to 0.1% is typically just 2 μs, indicating that the response to small changes is quick and precise. That's essential-

ly what's needed to drive a micropositioner.

The PA89's maximum offset voltage is 2 mV; the PA89A's is 0.5 mV. The latter offset voltage is the equivalent of a 1 μV offset from a conventional ($\pm$10-V-output) op amp. Offset drift of the two devices are either 30 and 10 μV/°C, respectively, or no greater than 5 mV for either unit over their –55°C to +125°C case oper-

ating-temperature range. A FET-input stage supplies the pair with typical bias currents of 5 pA (50 and 30 pA maximum, respectively). With the low bias current, you can operate at an inverting gain of 1000 using reasonably-sized input resistors without worrying about significant bias-current errors. Moreover, while the amplifier easily delivers 75 mA to the load, quiescent current is a maxi-

mum of just 4 mA, resulting from a complementary class AB output stage built of n-channel and p-channel power MOSFETs. The high-voltage FETs also make it possible for the amplifiers to operate near a foolproof SOA.

Many FETs are multiple devices connected in series to aid in handling high voltages. The input stage, responsible for the high open-loop gain and the resulting accuracy is a typical cascode circuit. In addition, proprietary bias circuitry throughout the device further assists in the handling of high voltages.

1000-V TOY

If you've designed linear circuits, you know the basic circuit tricks using one or more op amps. With the PA89, you can do those tricks with signal and/or common-mode voltages that run at about 1000 or more volts. For example, if the PA89 is connected up as an inverter or current-to-voltage converter and its input is driven with a digital-to-analog converter, a digitally programmable, high-voltage power source emerges. If a 12- or 16-bit d-a converter is employed, it becomes an accurate, dc-to-3000-Hz source. It can be connected as a current source with a compliance approaching 1200 V. All of these circuits lend themselves to applications in special-purpose test equipment.
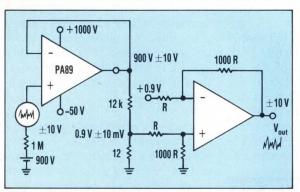
Monitoring $\pm$10 V of band-limited dc-to-100-kHz noise riding on a 900-V dc, high-impedance voltage source requires just three connections. First, connect the PA89 as a buffer with the plus input to the voltage source; then connect a 12-kΩ, 1000:1 voltage divider between output and

AN UPDATE ON PIEZOELECTRIC CERAMIC TRANSDUCERS

Piezoelectric materials have converted electrical energy to mechanical energy and vice versa for as long as the electronics industry has existed. Natural materials, such as quartz, were originally employed. Over the past 30 years, however, a family of lead-zirconate-titanate (PZT) ceramics has replaced natural materials for most applications.

The advantage of ceramics is that it can be manufactured in virtually any form factor desired by transducer designers. Acoustic applications of the material are the most familiar, ranging from phonograph pickups to megawatt sonar arrays to the "loudspeaker" in a PC and musical greeting cards (they're called unimorphs.).

These piezoelectric materials also can produce small, precise quantities of motion—particularly in a form called "bimorphs," as coined by their developer, Morgan Matroc of the Vernitron Division Corp. Past users of these materials may be more familiar with ear-

lier company names, such as Vernitron, Gould, or Clevite.

The bimorph consists of two layers of different PZT formulations that are bonded together (see the figure, part a). The two materials have different displacements for the same applied voltage. Consequently, in a manner similar to a bimetallic strip thermostat, the application of a driving voltage produces a bending motion, amplifying the lateral motion of each material. In one bimorph application, the transducers perform precise micropositioning of mirrors in optical systems for lasers.

When very large motions (1000 μin.) are required, individual transducers can be stacked (see the figure, part b). The total displacement of the stack (vertical in this case) is the sum of the displacements of the individual devices that form it.

Source: Morgan Matroc, Vernitron Division, 232 Forbes Rd., Bedford, OH 44146; Don Basco, (216) 232-8600.

(a) Bimorph transducer — PZT ceramic, Direction of motion

(b) Stack of PZT ring transducers — Motion

2. THE PA89 HIGH-VOLTAGE OP AMP can monitor small changes in voltage (in this case ±10 V) riding on top of a large voltage (900 V in this example).

common; and finally connect a fast, small-signal op amp at the tap on the divider *(Fig. 2)*.

With the PA89's power rails set at +1000 and –50 V, it's now handling over 900 V of common-mode potential. The small-signal op amp is connected as a differential amplifier

with a closed-loop gain of 1000. The divider tap goes to the plus input and +900 mV goes to the minus input, which offsets the 900 mV dc (1/1000 of 900 V) appearing at the tap. The amplifier takes the signal at the tap back to its original amplitude at the PA89's output. An instrumentation amplifier that can handle 100 kHz could be used in lieu of the op amp.

Two PA89s used as drivers could supply ±1000 V (2 kV) across a load in a bridge configuration with the load floating between their outputs. This is an ideal way to obtain maximum drive for a piezoelectric transducer. Two or more of the op amps connected as current sources with

their outputs tied together can supply 75-mA increments of current with a compliance of 1000 V. In any application, if the PA89's offset voltage is too high, it can be connected as a traditional composite amplifier circuit using a precision small-signal op amp to reduce errors.

The PA89 high-volatage op amp is contained in a 12-pin, hermetically sealed steel DIP. All active and passive components are mounted on an insulating beryllia substrate. Consequently, the case is isolated from all voltages and can be mounted directly to a heat sink—and you don't have to worry about someone getting zapped with 1000 V. The package footprint is 2.35 by 1.65 in.□

HOW VALUABLE?	CIRCLE
HIGHLY	568
MODERATELY	569
SLIGHTLY	570

SPARC WORKSTATIONS HIT 22 MIPS, 3 MFLOPS/CPU

A 33-MHZ CYPRESS CPU IS TEAMED UP WITH A WEITEK FLOATING-POINT COPROCESSOR FOR UP TO 65 MIPS OF PERFORMANCE.

LAWRENCE CURRAN

Several "firsts" are embodied in a new family of scalable-processor-architecture (SPARC)-based workstations and servers from Solbourne Computer Inc., Longmont, Colo. The Series5 is the first product family to use the 33-MHz SPARC central-processing unit from Cypress Semiconductor Corp.; the first SPARC system to have a Weitek Corp. 3171 floating-point coprocessor; the first to incorporate a completely physical cache memory; and the first workstations to use gallium arsenide (GaAs) semiconductors *(Fig. 1)*.
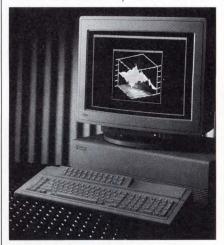
These firsts add up to impressive performance for the RISC systems, which run Solbourne's variation of the Unix-based SunOS operating system: 22 MIPS per CPU in integer operations and 3.0 MFLOPS per CPU executing a double-precision floating-point Linpack benchmark. Furthermore, when a four-CPU configuration is applied to a task, the integer performance zooms to 65 MIPS and the Linpack execution to 8.9 MFLOPS.

Solbourne was the first company to clone the original SPARC workstations from Sun Microsystems Inc., Mountain View, Calif. Less than a year later, Solbourne is at it again, more than doubling the performance of its own Series4 platforms. The CPU board is the only difference between the two generations.

In addition, the new family can outperform competing RISC-based entries from Sun and Digital Equipment Corp. For example, a Solbourne Series5/Model 501 with one CPU, a 19-in. monochrome monitor, 32 Mbytes of memory, and 661 Mbytes of hard-disk storage offers 22 MIPS of peak integer performance and 3 MFLOPS peak in a double-precision Linpack execution. It sells for $48,700 and competes with the Sun SPARCstation 4/330, which is priced a little lower ($45,300) but can't deliver the same performance.
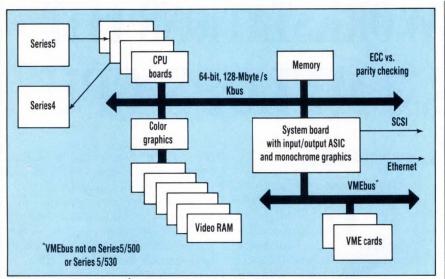
The Sun unit uses a 25-MHz Cypress SPARC chip, which enables it to reach 16 MIPS of peak integer performance and 2.6 MFLOPS for the same Linpack task. The Sun workstation also has less main memory and mass storage—24 Mbytes and 654 Mbytes, respectively.

The price and performance comparison is even more favorable for Solbourne vs. Digital's DECsystem 5810 RISC machine, which has a 25-

1. USING A 33-MHZ Cypress SPARC CPU and the Weitek 3171 floating-point coprocessor, the Series5 workstations from Solbourne Computer have 65 MIPs of multiprocessing. Each CPU does 22 MIPs of integer operations and 3 MFLOPs of double-precision floating-point Linpack math.

data addresses are arbitrarily assigned in the virtual cache index and don't always map to the same data located in another CPU's cache index," says Mati. And while a virtual-cache scheme can improve system performance, it can also complicate coordination between multiple caches (the ability to maintain cache coherence or consistency) in a multiprocessor system. This is because the design requires reverse pointers, which Mati says are cumbersome.

Solbourne designers have also reduced data contention by using a physical cache. Contention occurs in a virtual cache because certain locations tend to be used more by the system in creating and running the cache address index, according to Mati.
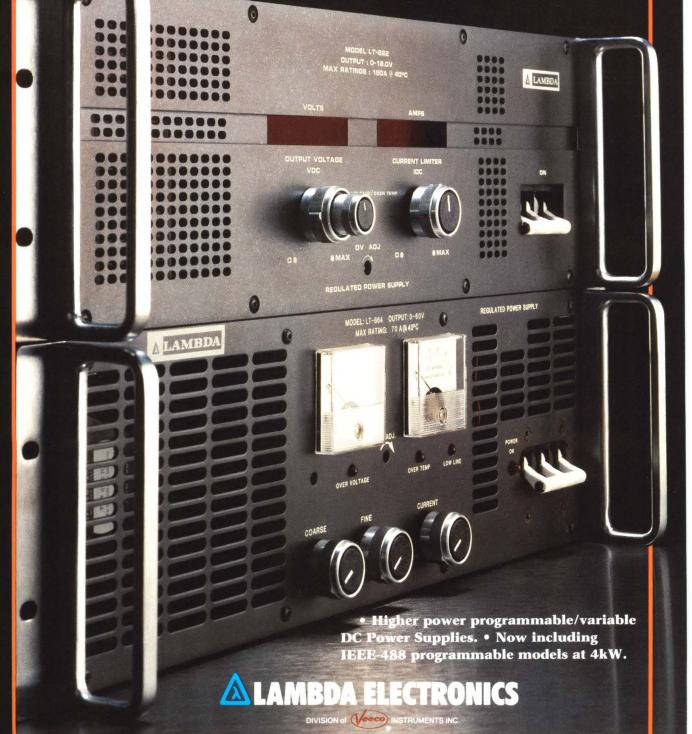
The cache is also where GaAs enters the picture in Solbourne's design, in the form of input/output, random-access memories. Solbourne uses four 256-bit-by-4-word RAMs from Vitesse Semiconductor Corp., which operate at a 5-ns access time. The RAMs perform the logical and physical translations at high speed to preserve the CPU's inherent performance.

Solbourne took another step to maintain overall system performance by using a high-speed system bus to move data around *(Fig. 2)*. The proprietary design, called the Kbus, offers a 64-bit data path operating at a sustained bandwidth of 128 Mbytes/s. Besides enabling high-speed data transfers between processors in a multiprocessor system, the Kbus also supplies a growth path to higher-performance processors when they come along. The Series5 also includes a separate VMEbus in its deskside and larger server models, which gives support for seven standard VMEbus add-in boards.

In announcing the Series5, Solbourne also introduced 32-Mbyte main memory boards for those models and for the earlier Series4.□

2. SOLBOURNE'S PROPIETARY KBUS offers a 64-bit data path and a sustained bandwidth of 128 Mbytes/s. It serves high-speed data transfers between processors in a multiprocessor system and future higher-performance processors.

MHz CPU from MIPS Computer Inc., Sunnyvale, Calif. An entry-level single-processor 5810 with 32 Mbytes of main memory and 560 Mbytes of disk storage offers a peak integer performance of 18.7 MIPS. The 5810, which costs $121,500, comes without a floating-point coprocessor.

The 22-MIPS CPU is the Cypress CY7C601 chip—a 0.8-μm CMOS device that features a windowed register file with 136 general-purpose 32-bit registers. Cypress says that this large register file cuts the load-and-store operations in half compared to

earlier chips. This makes the CPU faster by freeing the bus bandwidth to feed it instructions.

As for the Weitek Abacus 3171 coprocessor, it's described by its developers as the first single-chip floating-point unit for the SPARC architecture. Designed specifically to support the Cypress CPU chip, the unit speeds execution of floating-point operations by integrating onto one chip the floating-point data path and floating-point controller. The chip is housed in a 143-pin package. Those two functions require two chips, which are housed in 209- and 299-pin packages, respectively, in the only alternative SPARC coprocessor to date from Texas Instruments.

Use of a fully physical 128-kbyte cache memory in the Series5 instead of the 64-kbyte virtual cache design of the Series4 made it possible for Solbourne to eliminate the hardware and software overhead required to maintain cache consistency in a multiprocessor system. Nick Mati, Solbourne's engineering manager and company cofounder, reports that the physical cache eliminates most of the inefficiencies of the earlier design.

Mati also points out that with a completely physical cache, each CPU in a multiprocessor system can deal with identical data addresses. In contrast, "In a virtual-cache system,

PRICE AND AVAILABILITY

Series5 workstations are available in desktop and deskside models. Series5/500 desktop versions are 5-slot Kbus units with one or two CPUs; Series5/600 deskside versions have as many as four processors and both a 7-slot Kbus and 7-slot VMEbus provision. Prices for fully configured units are $38,200 to $122,400. Prices include a 19-in. monochrome display, keyboard, and mouse. Servers are $33,400 to $172,600, depending on configuration.

Solbourne Computer Inc., 2190 Miller Dr., Longmont, CO 80501; (303) 772-3400. **CIRCLE 513**

How Valuable?	Circle
HIGHLY	538
MODERATELY	539
SLIGHTLY	540

LAMBDA
LT-860/870 SERIES:

PROVIDES UP TO 500 AMPS IN A SMALLER, LIGHTER, LESS EXPENSIVE PACKAGE.

- Up to 60V, up to 500A, from $3296.
- Built-in adjustable overvoltage protection.
- Constant voltage/constant current operation.
- 187-265VAC, 3-Phase Input; Power factor > 0.90.
- Weighs 80% less and occupies only 35% of the volume of equivalent models.
- Front panel supervisory control group provides instant analysis of system operation.
- Compatible with Lambda's IEEE-488 Computer Programmable Power System.
- Ideal for laboratory, burn-in, test and systems applications.
- 5 Year Guarantee.
- Available for one day delivery from stock.

LAMBDA'S LT-870 STAND ALONE GPIB POWER SUPPLY

LT-860 Power Supply
Series $3296

LT-870 GPIB Power Supply
Series $4635

Lambda's new LT-870 Series is a stand alone IEEE-488 GPIB power supply. It is designed with three internal PC cards allowing for voltage and current limit programming over the bus.

The Interface Card handles the communication over the bus. The Programming Card provides the appropriate D/A conversion necessary for voltage and current limit programming over the entire voltage range. The third card, the Interconnect Card, is designed with these rear panel features:

- 5-bit DIP switch for primary address selection.
- Pushbutton reset switch — to reset the voltage and current limit to zero.
- Auto/manual select switch sets the power supply for either local or computer control.
- 9-pin connector facilitating hookup to Lambda's optional Confidence Check Card.

The stand alone LT-870 IEEE-488 Power Supply is backed by Lambda's 5 year guarantee and is available for one day delivery from stock.

	MAX CURRENT AT AMBIENT OF (AMPS)					PRICE			
	40°C	50°C	60°C	71°C	DIMENSIONS (INCHES)	QTY 1	QTY 10	QTY 25	MODEL
0-7.5 Volts	150.0	135.0	115.0	89.0	$5^3/_{16} \times 19^3/_{16} \times 8^3/_8$	1960	1875	1785	**LT-801**
	300.0	266.0	218.0	160.0	$5^3/_{16} \times 19 \times 16^1/_2$	3109	2975	2833	**LT-821**
	500.0	450.0	400.0	325.0	$5^3/_{16} \times 19 \times 17^1/_2$	3617	3461	3296	**LT-861**
	500.0	450.0	400.0	325.0	$5^3/_{16} \times 19 \times 17^1/_2$	5086	4867	4635	**LT-871(IEEE)**
0-18 Volts	70.0	61.0	52.0	40.0	$5^3/_{16} \times 19^3/_{16} \times 8^3/_8$	1960	1875	1785	**LT-802**
	150.0	133.0	109.0	80.0	$5^3/_{16} \times 19 \times 16^1/_2$	3109	2975	2833	**LT-822**
	225.0	205.0	180.0	145.0	$5^3/_{16} \times 19 \times 17^1/_2$	3617	3461	3296	**LT-862**
	225.0	205.0	180.0	145.0	$5^3/_{16} \times 19 \times 17^1/_2$	5086	4867	4635	**LT-872(IEEE)**
0-36 Volts	34.5	30.5	26.0	20.0	$5^3/_{16} \times 19^3/_{16} \times 8^3/_8$	1960	1875	1785	**LT-803**
	80.0	71.0	58.0	42.0	$5^3/_{16} \times 19 \times 16^1/_2$	3109	2975	2833	**LT-823**
	115.0	104.0	92.0	75.0	$5^3/_{16} \times 19 \times 17^1/_2$	3617	3461	3296	**LT-863**
	115.0	104.0	92.0	75.0	$5^3/_{16} \times 19 \times 17^1/_2$	5086	4867	4635	**LT-873(IEEE)**
0-60 Volts	21.5	19.0	16.0	12.5	$5^3/_{16} \times 19^3/_{16} \times 8^3/_8$	1960	1875	1785	**LT-804**
	50.0	43.0	35.0	25.0	$5^3/_{16} \times 19 \times 16^1/_2$	3109	2975	2833	**LT-824**
	70.0	63.0	56.0	45.0	$5^3/_{16} \times 19 \times 17^1/_2$	3617	3461	3296	**LT-864**
	70.0	63.0	56.0	45.0	$5^3/_{16} \times 19 \times 17^1/_2$	5086	4867	4635	**LT-874(IEEE)**

NOTE: Maximum output current applies over entire voltage range.

LT SERIES

Specifications

DC OUTPUT
Voltage range shown in table.

REGULATED VOLTAGE
CONSTANT
regulation, line . . . . 0.02% + 2mV for line variations from 187 to 242VAC (205 to 265VAC on "V1" option) for LT-800 series.
187 to 229VAC (207 to 253VAC on "V1" option) for LT-820 series.
0.05% for line variations from 187 to 265VAC for LT-860 and LT-870 series.

regulation, load . . . . 0.02% + 2mV on LT-801, 802, 821, 822; 0.02% + 4mV on LT-803, 804, 823, 824; 0.05% on LT-860 and LT-870 series for load variations from 0 to full load.

remote programming resistance
. . . . 200Ω/volt nominal.
remote programming voltage   volt per volt.
ripple and noise . . . . 10mV RMS, 50mV pk-pk for LT-801, 821.
15mV RMS, 100mV pk-pk for LT-802, 803, 804, 822, 823, 824.
20mV RMS, for LT-860 and LT-870 series.
temperature coefficient . . . . . . (0.02% + 50μV)/°C.

CONSTANT CURRENT
(Current regulated line and load) Automatic Crossover.
voltage range . . . . as shown in Table.
current range . . . . 5% to full load current.
regulation, line . . . . 0.3% of Io(max) for line variations from 187 to 242VAC (205 to 265VAC on "V1" option) for LT-800 series.
0.3% of Io(max) for line variations from 187 to 229VAC (207 to 253VAC on "V1" option) for LT-820 series.
0.3% of Io(max) for line variations from 187 to 265VAC on LT-860 and LT-870 series.

regulation, load . . . . 0.3% of Io (max) for load variations from 5% to rated DC voltage.

AC INPUT
line . . . . LT-800 series: 187 to 242VAC (205 to 265VAC on "V1" option), 47-63Hz. (Derate all ratings by 10% at 47-53Hz) LT-820 series: 187 to 229VAC, 3 phase ± 10% max phase imbalance, 4 wire, 47-63Hz (207 to 253VAC on "V1" option). (Derate 40°C ratings by 10% at 47-53Hz.) LT-860 and LT-870 series: 187 to 265VAC, 3 phase ± 10% max phase imbalance, 4 wire, 47-63Hz.

power . . . . LT-800 Series: 1985 watts maximum.
LT-820 Series: 4000 watts maximum.
LT-860, LT-870 Series: 5000 watts maximum.

EFFICIENCY
Minimum 65% at maximum output voltage for LT-800 series, 70% for LT-820 series, 78% for LT-860 and LT-870 series.

INPUT CURRENT
18A RMS max on LT-800 series, 17A RMS max per phase on LT-820 series, LT-860 and LT-870 series.

OPERATING TEMPERATURE RANGE
Continuous duty from 0°C to 71°C with appropriate deratings from 40°C to 71°C.

STORAGE TEMPERATURE RANGE
−55°C to +85°C.

OVERLOAD PROTECTION
THERMAL
Thermostat protects unit from excessive ambient temperature as well as inadequate air velocity. AC power must be momentarily removed from unit after thermal shutdown in order to restore operation.

ELECTRICAL
External overload protection — adjustable, automatic electronic current-limiting circuit limits output current to preset value. Current-limiting setability to 105% of rated current via front panel adjust.

OVERVOLTAGE PROTECTION
Built-in, adjustable overvoltage protection is standard on all sets. When preset voltage is exceeded, the overvoltage protector crowbars the output and removes the inverter drive. AC power must be momentarily removed from unit after overvoltage shutdown in order to restore operation.

OVERVOLTAGE PROTECTION ADJUSTABLE RANGES

Model	Vov(Min)	Vov(Max)
LT-801/821/861/871	3.5V	10V
LT-802/822/862/872	6V	24V
LT-803/823/863/873	9V	47V
LT-804/824/864/874	12V	70V

IN-RUSH LIMITING CIRCUIT
Limits in-rush current at turn-on to 200% of full load peak current.

COOLING
Fan cooled. Forced air cooling utilizing all metal, shaded pole, ball bearing, long life fan. (No lubrication needed). Leave adequate clearance at all air intakes and exhausts. Exhaust is at rear of unit.

CONTROLS
DC OUTPUT CONTROLS
Coarse and fine voltage adjust and single current adjust on front panel.

OVERVOLTAGE PROTECTION
Overvoltage trip point set by screwdriver adjust on front panel.

POWER
On-off switch on front panel of LT-800 series. On-off circuit breaker on front panel of LT-820, LT-860 and LT-870 series.

INPUT AND OUTPUT CONNECTIONS
Heavy duty barrier strips for AC input, ground and sensing. DC output via bus bar at rear of chassis.

METERS
Digital panel meter standard on LT-800, 820 series. Monitors output voltage/current by means of a volt/amp selector switch on LT-800 series. Separate digital panel meters on LT-820 series allow simultaneous monitoring of output voltage and current. Separate analog meters on LT-860 and LT-870 series provide for simultaneous monitoring of output voltage and current. Additional LED on front panel of LT-870 indicates auto/manual operation.

LED STATUS INDICATORS
An overvoltage/overtemperature indicator lamp will light to notify the user of the occurrence of either an overvoltage or overtemperature shutdown condition. AC power must be removed from the unit to reset the power supply and the light. A line fault indicator with automatic reset indicates power loss or loss of a phase on LT-860 and LT-870 series.

REMOTE SENSING
Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.

REMOTE ON/OFF
Isolated terminals on LT-860 and LT-870 series allows for these remote functions: Turn-on — Logic zero, short circuit or open circuit; Turn-off — provide 5mA into ± R terminals.

EMI
Conducted EMI conforms to FCC 20780 class A on LT-800 and LT-820 series.

PHYSICAL DATA

Package Model	Weight		Size Inches
	Lbs. Net	Lbs. Ship	
LT-800 series	30	37	5³/₁₆ × 8³/₈ × 19³/₁₆
LT-820 series	70	82	5³/₁₆ × 19 × 16¹/₂
LT-860, LT-870 series	60	72	5³/₁₆ × 19 × 17¹/₂

OPTIONS
AC INPUT

Series Model	Add Suffix	For Operation at:	Price
LT-800	−V1	205 to 265VAC 47-63Hz	12%
LT-820	−V1	207 to 253VAC 47-63Hz	12%

ACCESSORIES
Pot Covers available on LT-800, LT-860 and LT-870 series. LRA-17 Rack Adapter available for LT-800 series. Chassis slides available for LT-820, LT-860 and LT-870 series.

GUARANTEED FOR 5 YEARS
5 year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

GET GATE-ARRAY PLIABILITY WITH PROGRAMMABLE CHIP

REPROGRAMMABLE PLD'S NOVEL ARCHITECTURE AND FLEXIBLE LOGIC BLOCK CHALLENGE GATE ARRAYS.

DAVE BURSKY

Over the last few years, programmable logic devices progressed from simple chips with limited flexibility to complex devices that are achieving gate-array-like malleability. To date, RAM-based and one-time programmable fuse and anti-fuse programming cells have been used inside the gate-array-like chips. However, the RAM-based chips require a second memory to hold the configuration data. Moreover, one-time programmable fuse or anti-fuse devices must be relegated to the scrap heap if their configuration isn't right. But with Plus Logic's FPGA2020 field-programmable gate array, the first of a family of chips, designers have one UV EPROM-based gate-array replacement that can be erased and reprogrammed numerous times.

In addition to supplying designers with a new set of capabilities, the FPGA will eventually have a family that spans complexities from 1000 to about 10,000 gates. Furthermore, the unique logic architecture will simplify designers' tasks by making it possible for them to concentrate on the logic implementation and not spending time trying to reduce interconnection delays. The combination of the FPGA's logic and the system software developed by Plus Logic eliminate restrictions on routing and prevent any extra delays from being inserted in a design due to wiring or fan-out. Consequently, designers can precalculate all delays from a logic diagram and speed chip customization, because time doesn't need to be spent optimizing the placement and routing of the logic elements.

Approximately equal in logic capability to 2000 used gates in a mask-programmed gate array, the FPGA2020 can replace about 8 to 10 medium-density programmable logic devices (PLDs), or between 30 and 50 small- and medium-scale logic chips. When fully programmed, the new circuit can run in systems with 40-MHz clock rates and no-wait-state memory subsystems. The basic chip architecture consists of a central, programmable, universal interconnection matrix surrounded by eight configurable function blocks and programmable

PROGRAMMABLE LOGIC CHIP

I/O lines *(see the figure)*. The chip will be created with a 1.5-μm CMOS process that uses two layers of metal and two layers of polysilicon.

Packing 72 programmable I/O lines and 12 power and ground pins, the chip will be housed in either a re-programmable ceramic quad-sided leadless package, or in a plastic, one-time programmable leaded chip carrier. Of the 72 I/O lines, 12 are input only, another 24 are output only, and 36 are bidirectional (they can be configured as input or I/O). Because the chip has no architectural equivalent already on the market, Plus Logic has also developed PlusTran, a complete suite of PC-hosted programming and test-generation tools. The chip's architecture was designed to make it possible for 100% test coverage without the circuit being programmed. The chip can thus be tested with 100% fault coverage, either at the factory or during inspection.

The basic structure of the FPGA2020 contains eight programmable logic function blocks, each approximately equivalent to 125 to 400 gates. All eight of the blocks are tied into the universal interconnection matrix and any function block's output can be tied to any function block's input line. According to Cecil Kaplinsky, vice president of research and development, the ability to set up any interconnection path simplifies the task of placing and routing the desired logic. Furthermore, the circuit speed is independent of the fan-out through the interconnection matrix and the placement of logic in the blocks.

Each function block has nine outputs and 21 inputs, as well as clock and carry lines. To simplify the structure, an AND plane connected to an OR plane provides a range of product terms for each output. Streamlining the planes by removing some terms improves the chip's speed—a depopulated OR array reduces the loading, resulting in faster array operation. Rather than deliver a fixed number of product terms for each output, the OR plane combines both PAL-type and PLA-type architectures. For example, some product terms are dedicated to their outputs, while others can be freely shared.
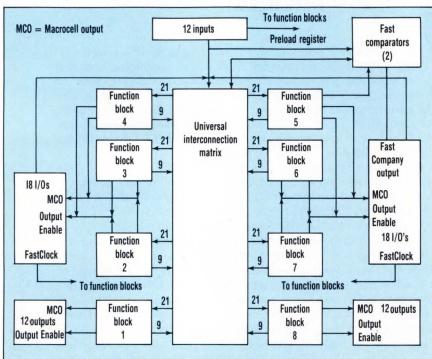
The design tools developed by Plus Logic make the chip seem very simple. However, the tools mask the complexity of the on-chip logic structures. Each configurable I/O block contains several multiplexers, a programmable register in the output path, and Exclusive-OR inputs that can be expanded through a function extender. Both shared and private product terms feed into the configurable logic section.

In addition to the standard AND-OR, combinatorial, and registered logic functions, each function block's output contains a configurable logic unit. With these logic units, any function block's output can be a logical operation of up to two levels or an arithmetic Add or Subtract operation of any two functions within the block. Any logic operation defined and implemented in the function block can occur in less then 25 ns, including the set-up time for the next logic operation, which can be internal or external to the FPGA2020.

The central interconnection matrix not only makes it possible for 100% routing of all signals, explains Kaplinsky, but it can also perform logical gating operations. Consequently, many of the gate-level library elements selected by designers can be absorbed by the architecture of the programmable array without using the function block resources and without incurring any additional signal delay. The company's Plusware development system software performs the necessary mapping operations to take advantage of the architecture.

Although the inner logic elements aren't blazingly fast, the FPGA2020 packs four Fast Compare circuits that can be put to work in two different modes. Each compare circuit supplies an "equal" flag when a match takes place for up to a 12-bit preprogrammed word matched against 12 of the chip's input lines. A match can be recognized and signalled in just 15 ns, or typically about 12 ns for signals out to the chip's I/O lines. With these short match times, the chip can perform critical operations at a clock

WITH PLIABILITY comparable to that of a gate array but with a shorter turnaround, Plus Logic's new FPGA2020 provides more complexity than a 2000-gate mask-programmed gate array. A universal interconnection matrix allows for any output to be connected to any input without blocking any connections. For complex logic functions, the PlusTran software places the logic in the eight function logic blocks.

PROGRAMMABLE LOGIC CHIP

rate of 66.7 MHz—ideal for such applications as memory-address decoding. When the fast comparisons aren't needed, the same input and output pins can be used for other logic or decoding operations.

Chip timing can be controlled through two clocking schemes that users can set up. Clock signals that are optimized for short clock-to-output delays are available on two of the chip's I/O pins, if desired. Those clocks will have a skew of less then 0.5 ns, measured at the I/O pin. If the fast clocks aren't needed on the output pins, the pins can be used for general-purpose I/O. Each of the Fast-Clock pins can drive all of the internal resources. Clock signals can also come from any input or I/O pin, or they can be derived from product terms. Unlike most other PLDs, each flip-flop on the PGA2020 can be clocked by a different frequency signal. Or conversely, they can all be triggered from a common clock in a synchronous system without any additional clock skew.

To configure the chip, a bit pattern must be programmed into the on-chip UV EPROM. For programming purposes, the chip looks identical to a memory chip. In fact, with a special adapter socket that fits a 28-pin EPROM site on a memory programmer, the FPGA2020 can be configured for an application. Once programmed, the chip will automatically shift its configuration data from the internal EPROM to RAM-like control cells. Data can also be shifted in from an external source to reconfigure the chip without reprogramming the EPROM. As a result, every function on the chip can be tested, even if the EPROM is programmed to create a specific logic subsystem.

The company's PlusTran design system combines familiar, existing tools with proprietary architecture-specific tools. Initially, two companies' commercial packages—ViewLogic's ViewDraw and ViewSim schematic-capture and simulation packages and Orcad's SDT schematic capture package—that run on a PC-AT or compatible system handle the front-end of the design process. The schematic packages tie into a logic library created by Plus Logic with small- and medium-scale logic functions and PAL device equivalents. Internally developed tools, such as the Plus Director, Emulator, Integrator and Optimizer packages, hide much of the chip's complexity from the non-silicon expert.

The Director package is a menu-driven shell that lets users access all of the more complex packages. It also supplies all of the file management. With the Emulator utility, users can verify the functionality of their design as it was captured with the schematic tools. At the heart of the proprietary toolset is the Integrator, a package that reads the net list produced by the schematic-capture front end, translates it, and creates a model of the elements in the net list that can be mapped into the target device. The Optimizer utility takes unused elements, gate-level functions and combinable elements and produces optimized logic models. Additional sub-packages—Plus Configure, Plus ASM, and Plus Report—support the chip's programming, documentation, and other functions.

The company plans to introduce a series of field-programmable subsystem logic chips. The first of those parts will be the FPSL5110, an intelligent data buffer that contains both programmable logic and a 32-word-by-32-bit register bank.□
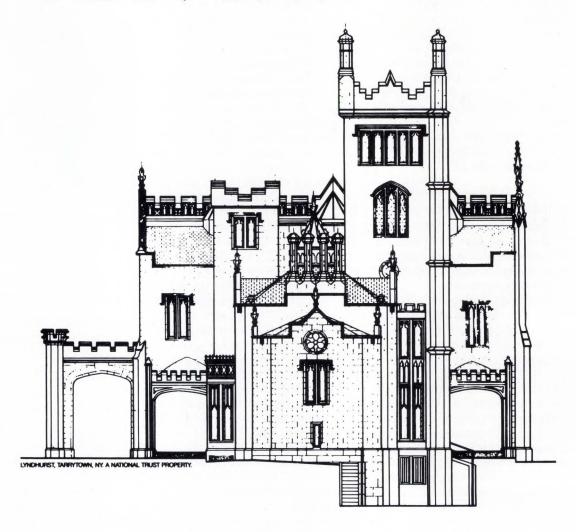
HOW VALUABLE?	CIRCLE
HIGHLY	565
MODERATELY	566
SLIGHTLY	567

PRESERVATION
PLAN ON IT

LYNDHURST, TARRYTOWN, N.Y. A NATIONAL TRUST PROPERTY.

Planning on restoring a house, saving a landmark, reviving your neighborhood?

No matter what your plans, gain a wealth of experience and help preserve our historic and architectural heritage. Join the National Trust for Historic Preservation and support preservation efforts in your community.

Make preservation a blueprint for the future.

Write:

National Trust for Historic Preservation
Department PA
1785 Massachusetts Ave., N.W.
Washington, D.C. 20036

FOCUS

SIGNAL GENERATORS

DIGITAL SYNTHESIS TECHNIQUES ADD CAPABILITY AND ENHANCE PERFORMANCE IN RF SIGNAL SOURCES.

JOHN NOVELLINO

Digital techniques, which have greatly influenced test and measurement in recent years, have even had profound effects on the staid field of rf signal generators. Most of the new signal generators create their signals digitally. Using digital synthesis, manufacturers can now offer very stable and clean signals at attractive prices. Digital processing also adds flexibility to internal modulation capability.

Along with this additional capability comes an increased diversity in performance and price among the many instruments available. Rf signal generators with internal modulation come with price tags as low as several hundred dollars and as high as over $50,000 *(see the table)*. More than ever, users must carefully examine their application needs before evaluating signal generators.

"The price-performance ratio of signal generators is really changing with advances in technology, especially direct digital synthesis," says Sara Mussmann, test-and-measurement product line manager for Wavetek RF Products. "Today, you can get much more stable performance for a lower cost than you could 10 years ago."

According to Mussman, the distinc-tion between high-end signal generators and good general-purpose instruments has grown wider. As a result, users should evaluate their applications carefully because most tend to overspecify when looking for a new unit.

The newest member of Wavetek's family of rf signal generators is the 2407, a synthesized AM/FM generator introduced earlier this year. The instrument features a two-line, dot-matrix alphanumeric display that tells users how to operate the generator's built-in diagnostic and calibration routines *(Fig. 1)*. With an extensive set of internal diagnostics, users can isolate potential trouble spots down to the board level without opening the case.

The autocalibration procedure can be initiated over a standard IEEE-488 interface. Moreover, the internal error-correction data is output over the bus so users can track the instrument's aging to schedule maintenance. The 2407 can also be programmed over the GPIB using English-language commands that include a minimum number of unique terms.

Covering frequencies from 10 kHz to 550 MHz, the 2407 has an rf output range of +13 to –127 dBm with a resolution of 0.1 dB and an accuracy within ±1.5 dB. Users can increase the accura-

1. A TWO-LINE DOT-MATRIX alphanumeric display on the Wavetek 2407 includes instructions for operating the unit's extensive set of built-in diagnostic and calibration routines.

cy by adding more calibration points as part of one of the diagnostic features. The output is flat within 1 dB over the instrument's bandwidth.

Some generators include multiple types of modulation that can be combined for greater flexibility. Digital synthesis in the modulation section adds to that flexibility. With some instruments, "you can do the same things that you can with a programmable function generator," says Earl Olsen, marketing support manager at John Fluke Mfg. Co. "Modulation signals are available from several hundred kilohertz down to several hertz and are programmable in frequency and level," he says. "In some cases, you can bring that signal out on a separate connector."

SIGNAL PURITY

After considering the frequency range and type of modulation needed, the most important specification involves signal purity. Depending on the application, that specification may be phase noise with reference to the carrier, residual FM, or single-sideband (SSB) noise. Other important factors are level accuracy and the levels available. "The ability to program the instrument down into the noise floor is important," says Olsen. "This is useful when checking a receiver's sensitivity to see if you can bring the signal up from the noise."

The most versatile modulation capabilities in the Fluke line belong to the 6062A, which offers AM, FM, and phase modulation alone or in combination, as well as fast-rise-time pulse modulation. Together with a 2.1-GHz maximum frequency, those modulation abilities make the synthesized unit suitable for various applications involving military and space equipment and land-mobile communications.

Gallium-arsenide switching technology gives the 6062A's pulse modulator rise and fall times of 15 ns and an on-off ratio of 80 dB, which makes it particularly useful for radar simulations. Pulse durations of less than 50 ns are possible, with pulse repetition rates up to 16 MHz and duty cy-

cles to 100%. Residual FM is guaranteed to be less than 6 Hz in a 0.3-to-3-kHz bandwidth from 245 to 512 MHz, and 24 Hz from 1050 to 2100 MHz. Non-harmonic spurious products are below –60 dB to 1050 MHz and –54 dB to 2100 MHz, with a typical phase noise of –123 dBc/Hz at 20 kHz from a 500-MHz carrier. An IEEE-488 interface is standard.

One way that Hewlett-Packard Co. fulfills users' needs for varying capability is by offering several models with a modular internal architecture that accommodates a number of options. With these models, such as the HP 8644, 8645, and 8665, users can then customize an instrument.

"A modular platform helps us fine tune the product to the type of application the customer has," says Rodger Tracy, marketing manager for HP's Spokane Div. "This lowers the instrument's cost because users aren't buying modules or features that they don't need."

The HP 8644A is a good example. For $17,000, users get a 1030-MHz synthesized generator that offers AM, FM, and pulse modulation with internal modulation frequencies of 300, 400, 1000, and 3000 Hz. At 20 kHz from a 1000-MHz carrier, phase noise is –128 dBc/Hz; residual FM in a 0.3-to-3-kHz bandwidth is less than 2 Hz; and FM distortion is 3%. For an extra $6000, option 2 extends frequency coverage to 2060 MHz. If state-of-the-art spectral purity is needed, option 4 ($4000) drops phase noise to –137 dBc/Hz, residual FM to

2. SEVERAL FORMS of digital modulation, including 256 levels of quadrature amplitude modulation (QAM) and 81 levels of pseudo-random-sequence (PRS) modulation, are available from the HP 8782A vector signal generator.

less than 1 Hz (at 1000 MHz), and FM distortion to 1%.

Another option greatly expands the HP 8644A's modulation capability. Using digital synthesis, the internal source creates sine, triangle, sawtooth, and square waves, as well as white Gaussian noise, at frequencies that can be adjusted from 0.1 Hz to 400 kHz. Users can also vary amplitudes and relative phase. The circuit will generate four waveforms at once, combining them by summation and modulation if desired.

For high-cycle-count applications in a production environment, the HP 8644A can be equipped with an electronic attenuator that uses solid-state switches instead of mechanical relays to set levels. The electronic attenuator reduces the specified output by 3 dB. It can't be used with the frequency doubler, but it has a 3-million-hour mean-time-between-failure (MTBF) rating and a five-year guarantee.

DIGITAL MODULATION, TOO

To accommodate the increasingly common forms of digital modulation found in microwave communication and radar or electronic-warfare systems, HP introduced what it termed a vector modulation signal generator in 1987. Last August, a second-generation version, the HP 8782A, added several more modulation formats at half the price (*Fig. 2*). The new unit covers a smaller frequency range—1 to 250 MHz versus 10 kHz to 3 GHz. Because most tests on the applicable systems are made at the intermediate frequency rather than at transmission frequencies, the trade-off is reasonable.

The HP 8782A's modulation formats include binary phase-shift keying (BPSK) through 256 levels of quadrature-amplitude modulation (QAM) and 9 to 81 levels of pseudo-random-sequence (PRS) modulation, as well as amplitude and scalar modulations with rates from dc to 50 kHz. An internal pseudo-random bit-sequence generator with a $2^{23} - 1$ sequence length makes it possible for users to create all of the standard digital formats without an external source. In addition, the instrument

handles parallel-modulation inputs with data rates to 100 MHz and serial rates to 200 MHz. Data input lines accommodate ECL and TTL signals.

Housed in a relatively small portable package, the Marconi 2022A and 2022C cover from 10 kHz to 1000 MHz with AM, FM, and phase modulation supplied by a 1000-Hz internal source. The A version's output runs from –127 to +6 dBm; the C version goes to +13 dBm. Users can introduce their own modulation signal up to a 50-kHz bandwidth. The instrument is only 10.25-in. wide by 6-in. high by 14.5-in. deep, and it weighs 16.5 lbs. (*Fig. 3*).
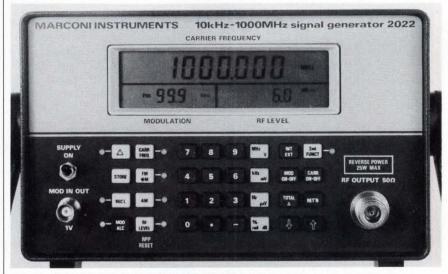
The 2022 signal generators can store 20 complete front-panel settings and 80 additional frequency settings in a nonvolatile memory. Users can recall any of the settings or step through a series of preset measurements by pushing the up and down keys. In optional GPIB operation, the memory can store up to 32 user-defined ASCII characters.

For levels above –10 dBm, the unit's output is flat to within ±0.5 dB over its entire bandwidth. Residual FM is less than 7 Hz at 499 MHz, dropping by 6 dB/octave to less than 3.5 Hz below 62.5 MHz. Harmonically related spurious signals are less than –35 dBc for carriers up to 62.5 MHz, and better than –25 dBc above that level.

Among the newer rf signal generators from Anritsu Corp. are the MG3601A (100 kHz to 1040 MHz) and MG3602A (2080 MHz top frequency). Both units include an optional video-modulation capability in addition to AM, FM, and phase modulation. The input needed for video modulation is a video composite signal of 1 Vpk-pk, with a pedestal level of 0 V and a positive-voltage white level. The modulated wave includes a pedestal level of approximately 75% of the carrier peak and a white level of about 12.5% of the carrier peak.

The generators have a wide output level ranging from –133 to +13 dBm up to 1040 MHz—above that frequency, the MG3602A's maximum output is +7 dBm. For convenience, the liquid-crystal display (LCD) level can be set to read in dBm, dBμ, mV, μV, dBμ emf, and μV emf. Signal purity is good, with an SSB phase noise of at least –123 dBc/Hz at 20 kHz from a 500-MHz carrier, and residual FM of 4 Hz at 500 MHz.

For applications that demand very high signal purity or a wide dynamic range, the Racal-Dana 9087 meets the challenge. Because the unit covers its range of 10 kHz to 1300 MHz without a doubler, there aren't any subharmonics and the output of –140 to +19 dBm is available over the entire bandwidth. Spurious signals at more than 3 kHz from the carrier run
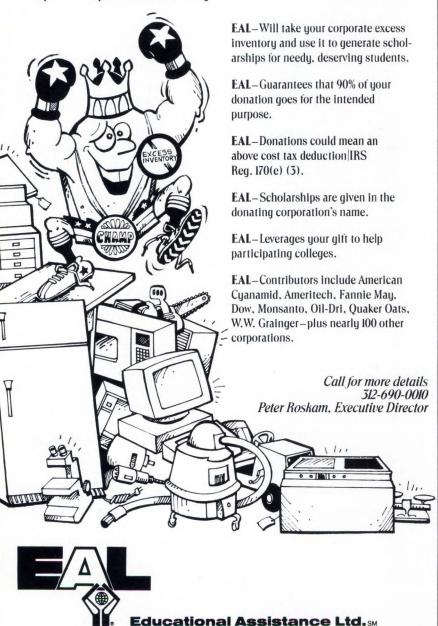
3. THE PORTABLE MODEL 2022 from Marconi Instruments comes in two versions. The A model's maximum output is +6 dBm and the C version features a +13-dBm maximum signal level.

SIGNAL GENERATORS

RF SIGNAL GENERATORS WITH INTERNAL MODULATION

Manufacturer	Model/price	Frequency range	Internal modulation	Residual FM*	SSB phase noise (offset)*	Output
Anritsu America Inc. Oakland, NJ (201) 377-1111 **CIRCLE 451**	MG439B $7,875	50 kHz - 50 MHz	AM	N.A.	[1]–130 dBc/Hz (1 kHz)	–137 - +19 dBm
	MG547A/B $8,065/$9,075	840 - 940 MHz 800 - 970 MHz	FM	–40 dB	–114 dBc/Hz (20 kHz)	–20 - +100 dBμ
	MG3601A/MG3602A $9,665/$15,799	100 kHz - 1040/ 2080 MHz	AM, FM, φM, video	2 - 7 Hz	–129 - –117/–110 dBc/Hz (20 kHz)	–133 - +13/+7 dBm
	MG645B/B1 $17,305/$18,145	50 kHz - 1040 MHz	AM, FM	–64 dB	–133/–135 dBc/Hz (25 kHz)	–143 - +17 dBm
	MG655A $34,275	100 kHz - 1300 Mhz	AM, FM	1.1 Hz	–133 dBc (10 kHz)	–143 - +17 dBm
	MG649A $42,320	100 kHz - 2000 Mhz	AM, FM, PM	–94 dB	–133 dBc (100 kHz)	–143 - +15 dBm
B&K Precision Chicago, IL (312) 889-1448 **CIRCLE 452**	2005 $195	100 kHz - 150 MHz	AM	N.A.	N.A.	100 mV rms
	3026 $595	0.5 Hz - 5 MHz	AM	N.A.	N.A.	10 V pk - pk
John Fluke Mfg. Co./Philips Everett, WA (800) 443-5853 **CIRCLE 453**	6060B $5,225	10 kHz - 1050 MHz	AM, FM	10 Hz	–116 dBc/Hz (20 KHz)	–127 - +13 dBm
	6060B/AK $5,750	10 kHz - 1050 MHz	AM, FM	12 Hz	–116 dBc/Hz (20 kHz)	–127 - +13 dBm
	6061A $5,895	10 kHz - 1050 MHz	AM, FM	6 Hz	–123 dBc/Hz (20 kHz)	–127 - +13 dBm
	6060A/AN $7,500	10 kHz - 520 MHz	AM, FM	15 Hz	–113 dBc/Hz (20 kHz)	–127 - +13 dBm
	6062A $11,295	100 kHz - 2100 MHz	AM, FM, φM, PM	6 Hz	–123 dBc/Hz (20 kHz)	–127 - +13 dBm
	6070A $18,950	200 kHz - 520 MHz	AM, FM, φM, PM opt.	1.7 Hz	–132 dBc/Hz (20 kHz)	–127 - +19 dBm
	6071A $19,900	200 kHz - 1040 MHz	AM, FM, φM	1.7 Hz	–132 dBc/Hz (20 kHz)	–127 - +19 dBm
Hewlett-Packard Co. Palo Alto, CA (800) 752-0990 **CIRCLE 454**	8656B $6,250	100 kHz - 990 MHz	AM, FM	2 - 7 Hz	–126 - –114 dBc/Hz (20 kHz)	–127 - +13 dBm
	8657A/B $7,900/$12,500	100 kHz - 1040/2060 MHz	AM, FM	1 - 4/6 Hz	–136 - –124/–118 dBc/Hz (20 kHz)	–143.5 - +13 dBm
	8640B $12,000	500 kHz - 512 MHz	AM, FM, PM	5 Hz	–130 dBc/Hz (20 kHz)	–145 - +18.5 dBm
	8683B/D $16,400/$20,500	2.3 - 6.5/13 GHz	AM, FM, PM	[2]5 kHz	–72/–66 dBc (10 kHz)	–130 - +10 dBm
	8684B/D $16,400/$20,500	5.4 - 12.5/18 GHz	AM, FM, PM	[2]10 kHz	–65/–59 dBc (10 kHz)	–130 - +10/–3 dBm
	8644A $17,000	252 kHz - 1030 MHz	AM, FM, PM	1 - 4 Hz	–145 - –121 (20 kHz)	–137 - +16 dBm
	8660D $23,350 - $29,250[3]	10 kHz - 2.6 GHz	AM, FM, φM, PM	[3]	[3]	[3]–146 - +13 dBm
	8642A/B $24,050/$33,050	100 kHz - 1057.5/2115 MHz	AM, FM, φM, PM	1.2 - 2/5 Hz	–144 - –134/–125 (20 kHz)	–140 - +20 dBm
	8782A $30,000	1 - 250 MHz	AM, digital	4 Hz	–110 dBc/Hz (10 kHz)	–100 - +7 dBm
	8645A $32,000	252 kHz - 2060 MHz	AM, FM	1 - 4 Hz	–144 - –120 (20 kHz)	–137 - +16 dBm
	8665A $35,000	100 kHz - 4.2 GHz	AM, FM, PM opt.	15 Hz	–117 - –105 (20 kHz)	–139.9 - +13 dBm
	8662A $35,100	10 kHz - 1280 MHz	AM, FM	0.5 Hz typ.	–131 (10 kHz)	–139.9 - +13 dBm
	8673E $36,500	2 - 18 GHz	AM, FM, PM	12 Hz	–60 (1 kHz)	–120 - +8 dBm

SIGNAL GENERATORS

RF SIGNAL GENERATORS WITH INTERNAL MODULATION (cont'd)

Manufacturer	Model/price	Frequency range	Internal modulation	Residual FM*	SSB phase noise (offset)*	Output
	8672E $39,000	2 - 18 GHz	AM, FM	12 Hz	−86 - −74 (10 kHz)	−120 - +8 dBm
	8673B/C/D $42,000 - $53,000	50 MHz - 26.5 GHz	AM, FM, PM	12 Hz	−86 - −74 (10 kHz)	−100 - +11 dBm
	8663A $48,700	100 MHz - 2.56 GHz	AM, FM, ϕM, PM	0.5 Hz typ.	−131 (10 kHz)	−139.9 - +16 dBm
	8780A $60,000	10 kHz - 3 GHz	AM, FM, PM, digital	4 Hz	−110 (100 kHz)	−100 - +4 dBm
Krohn-Hite Corp. Avon, MA (800) 582-1660 **CIRCLE 455**	2400 $1,900	0.003 Hz - 30 MHz	AM, FM	N.S.	N.S.	2 mV - 15 V pk - pk
Leader Instruments Corp. Hauppauge, NY (800) 645-5104 **CIRCLE 456**	LSG-231 $545	100 MHz ± 1 MHz	FM stereo	N.S.	N.S.	0.1, 1, 10 mV
	3215 $2,450	100 kHz - 140 MHz	AM, FM	73 dB s/n	N.S.	−20 - 126 dBμ
	3216 $2,995	100 kHz - 140 MHz	AM, FM stereo	73 dB s/n	N.S.	−20 - 126 dBμ
	LSG-245 $3,495	200 - 1799.9 kHz	AM stereo (C-QUAM)	N.A.	N.A.	−10 - 120 dBμ
	LSG-221B $4,200	25 MHz - 950 MHz	AM, video	N.A.	N.A.	−15 dBm
	3220 $5,995	100 kHz - 1300 MHz	AM, FM, dc-FM	3.5 Hz	−120 (10 kHz)	−133 - +13 dBm
Marconi Instruments Allendale, NJ (201) 934-9050 **CIRCLE 457**	2022A/2022C $4,395/$4,989	10 kHz - 1000 MHz	AM, FM, ϕM	3.5 - 7 Hz	−135 - −110 dBc/Hz (20 kHz)	−127 - +6/+13 dBm
	2018A/2019A $5,995/$6,595	80 kHz - 520/1040 MHz	AM, FM, ϕM	6 Hz	−130 (20 kHz)	−127 - +13 dBm
	2017 $24,950	10 kHz - 1024 MHz	AM, FM, PM	3 Hz	−136 (20 kHz)	0.2 μV - 4 V
Panasonic Factory **Automation Co.** Secaucus, NJ (201) 392-4050 **CIRCLE 458**	VP-8177A $2,200	100 kHz - 110 MHz	AM, FM	[2]80 dB	N.S.	−19 - +99 dBμ
	VP-8174A/8175A $2,990/$2,590	100 kHz - 110 MHz	AM, FM	[2]76 dB	N.S.	−19 - +99 dBμ
	VP-8191A $4,000	100 kHz - 135 MHz	AM, FM	[2]80 dB	N.S.	−10 - +132 dBμ
	VP-8254A $4,380	200 - 1999.99 kHz	AM stereo (C-QUAM)	N.A.	N.S.	−133 - +19 dBm
	VP-8179B10 $6,000	10 Hz - 240 MHz	AM, FM	[4]80 dB	N.S.	−133 - +19 dBm
Racal-Dana Instruments Co. Irvine, CA (714) 859-8999 **CIRCLE 459**	9087 $34,000	10 kHz - 1300 MHz	AM, FM, ϕM, PM	0.25 - 1 Hz (300 kHz BW)	−142 - −130 (3 kHz - 1 MHz)	−140 - +19 dBm
Simpson Electric Co. Elgin, IL (312) 697-2260 **CIRCLE 460**	423 $1,495	0.005 Hz - 13 MHz	AM, FM	N.S.	N.S.	10 V pk - pk max.
Wavetek RF Products Inc. Indianapolis, IN (800) 851-1202 **CIRCLE 461**	2407 $4,595	10 kHz - 550 MHz	AM, FM	[2]< 30 Hz	−100 dBc/Hz (10 kHz)	−127 - +13 dBm
	2505/2500A $4,595/$4,750	200 kHz - 550/1100 MHz	AM, FM	< 20 Hz	−107 dBc/Hz (20 kHz)	−137 - +13 dBm
	2510 $5,495	200 kHz - 1100 MHz	AM, FM	< 7 Hz	−123 dBc/Hz (20 kHz)	−137 - +13 dBm
	2500C $5,995	200 kHz - 1100 MHz	AM, FM, FSK	< 20 Hz	−115 dBc/Hz (20 kHz)	−137 - +13 dBm
	2520 $7,995	200 kHz - 2200 MHz	AM, FM	< 40 Hz	−123 dBc/Hz (20 kHz)	−137 - +13 dBm

* At a frequency or frequency range specified by manufacturer.
[1] Sideband am noise.
[2] 50 Hz - 15 kHz post-detection bandwidth.
[3] Depends on modules selected.

[4] 200 Hz - 20 kHz post-detector bandwidth.
N.A.: not applicable.
N.S.: not specified.

Consider this a guide rather than a definitive list.

SIGNAL GENERATORS

from –85 dBc at 650 to 1300 MHz, to –97 dBc at 100 to 350 MHz. Residual FM in a 3-kHz bandwidth is only 1 Hz above 650 MHz, and it drops to 0.25 Hz from 100 to 350 MHz.

The SSB phase noise in AM and CW modes at a 3-kHz to 1-MHz offset from the carrier ranges from –130 dBc/Hz above 650 MHz to –142 dBc/Hz at 100 to 350 MHz. Racal-Dana achieves this low phase noise by placing a high-level, low-noise 100-MHz quartz oscillator between the generator reference standard and the synthesizer drive circuits. The generator's output is phase-locked to this oscillator, reducing the noise multiplication factor by more than 20 dB.

The 9087, which includes a standard GPIB interface, offers AM, FM, phase, and pulse modulation with an internal source of 400 or 1000 Hz. The pulse rise and fall time is 40 ns, with a 200-ns minimum pulse width. Users can sweep the entire bandwidth with 1-Hz resolution, either manually or by preprogramming the step size and width. In automatic sweep, four speeds from 1 s/step to 2 ms/step are available.

The recent advent of AM broadcast-band stereo led two manufacturers to introduce signal generators aimed at that technology. The Panasonic VP-8254A (200 to 1999.99 kHz) and Leader Instrument's LSG-245 (200 to 1799.9 kHz) output an AM stereo signal using the Motorola C-QUAM format. Both instruments have 400- and 1000-Hz internal modulation signals and accept 50-Hz to 15-kHz external signals.

Along with a standard GPIB interface, the VP-8254A includes a battery-backup memory that stores 100 front-panel settings for instant recall. Users can recall any two setups in sequence. The LSG-245 also includes storage for 100 front-panel setups as well as four additional power levels—the bus interface is optional.□

How Valuable?	Circle
Highly	562
Moderately	563
Slightly	564

DEVELOP HARDWARE AND SOFTWARE SIMULTANEOUSLY IN ONE ENVIRONMENT RICHARD NASS

A large void in the CASE area—linking of hardware and software development tools from a global perspective—has been filled by the Code-Link Station from Mentor Graphics. This toolset addresses software development from the initial design through maintenance and ties a graphical interface to the debug environment. Besides tying the hardware and software tools together, it provides a common interface for a complete set of CASE tools. Thanks to these new features and the ability to perform both software and hardware design at the same time, a more reliable part can be gotten to market more quickly.

In a traditional design environment, hardware and software are designed separately, by different design teams on different tools. Until now, there was no real integration between the two technologies. The CodeLink Station lets the software developers evaluate their code on the target hardware earlier in the design cycle. This helps alleviate the bottleneck occurring at the system debug and integration level. The user need only familiarize himself with one interface rather than three to simulate, debug, and emulate.

The toolset performs behavioral and timing analysis using Mentor's QuickSim logic simulator. This is done through a link to the instruction-set simulator (ISS). Now, both software and hardware engineers can decide how to resolve design tradeoffs much earlier in the development cycle. As software executes on the ISS, events on the processor's I/O lines are translated into the appropriate signals and states for input into the hardware design.

Obviously, the amount of software in designs is growing. According to G.E. Aerospace, software makes up nearly 90% of a system's functions. To handle this barrage of software, the CodeLink Station lets programmers debug their code at a higher level of abstraction than the code level while maintaining line-level capabilities for analysis. The same debugger can also be used to evaluate code with the same interface and capabilities in three different modes: native, virtual, and physical.

Structure Map, one of the tools in the CodeLink Station, automatically generates a structure chart from any IEEE-695A-compliant C source code. This keeps a common interface within the different modes. With this structure chart, designers gains an intuitive, graphical high-level understanding of how the program works at a very early point in the process. Now, he can also gauge the complexity of his task.

In the native mode, code is executed on the development station's host processor. Here, the debugger gives the designer the full complement of debugging features that will be used later in the debugging process.
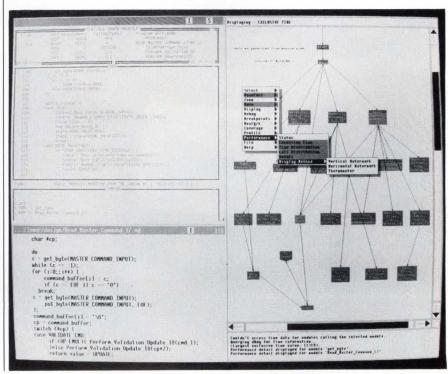
Virtual-mode code execution is in a simulated hardware environment. Integration of hardware and software functionality can start as soon as the processor is selected. The debugger environment includes instruction-set simulators and a large selection of models, such as the Motorola 680X0 and the Intel 8086. Extensive testing of the source code can occur, because the ISS can interpret thousands of instructions per second.

In the physical mode, code is executed on the prototype target with the debugger connecting to the prototype target system through an emulator. By doing this, proper integration of the object code and hardware are ensured. The CodeLink Station supports many popular emulators, including those from Hewlett-Packard. It also works with compilers from Alsys, HP, Tektronix, Telesoft, and Toshiba.

Prices for the CodeLink Station start at $27,900, and it is available immediately.

Mentor Graphics Corp., 8500 S.W. Creekside Pl., Beaverton, OR 97005; (503) 626-7000. **CIRCLE 314**

Now the family's growing. Introducing the 32GX32.

NATIONAL'S EMBEDDED SYSTEM PROCESSORS™ ARE OPTIMIZED FOR LASER BEAM PRINTERS.

That's the reason Canon chose National's 32CG16 to power its LBP-8 Mark III Series, the latest advance in desktop laser printing. And it's also the reason you should consider the newest member of our Embedded System Processor family, the 32GX32. Born of the same architectural lineage, it offers a new price/performance solution to suit your needs.

COST-EFFECTIVE SYSTEM PERFORMANCE.

Based on a powerful four-stage pipeline architecture, the 32GX32 provides peak performance of 15 MIPS for printers. This allows designers to handle the most demanding PostScript® environment with performance to spare. What's more, National's optimized solution can help achieve the lowest system cost, a key to success in the highly competitive printer market.

Thanks to its advanced bus interface and its on-chip caches, the 32GX32 is able to sustain most of its performance while using slower, inexpensive DRAMs. This fact alone has a tremendous impact on

© 1989 National Semiconductor Corporation

Embedded System Processor is a trademark of National Semiconductor Corporation. PostScript is a registered trademark of Adobe Systems, Inc.

the system cost of today's printers, which typically require large amounts of memory.
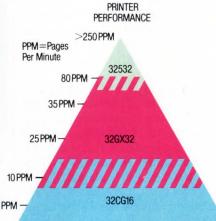
The 32GX32 performs single-cycle operations on information contained in on-chip instruction and data caches. The data cache organization can accommodate both a stack *and* a scratch pad for high-speed font generation. These factors minimize the effect of low-cost, slow external memory on system performance.

COMPACT SYSTEM DESIGN.

With the 32GX32, designers can generate extremely compact code, which leads to fewer EPROMs. This is due to National's state-of-the-art optimizing compilers, and to the 32GX32's tuned instruction set that resembles high-level page description languages.

And, even though the 32GX32 is a full 32-bit processor, its dynamic bus sizing feature allows you to use lower-cost 8- and 16-bit peripherals without need for additional logic.

PRINTER PERFORMANCE

PPM=Pages Per Minute

>250 PPM
32532
80 PPM
35 PPM
25 PPM — 32GX32
10 PPM
4 PPM — 32CG16

National offers a spectrum of system-optimized solutions for printer control.

Of all the available processors "targeted" at laser printers, only National's Embedded System Processors are truly optimized for printer designs. Competitors may claim performance that rivals the 32GX32, but nothing else can match the system cost savings that National provides.

WE'D LIKE YOU TO MEET OUR FAMILY.

Leading manufacturers worldwide are discovering that National's family of Embedded System Processors comprises the only optimized solution for laser printers. Call us today at (800) 825-5805, ext. 105, and we'll arrange an introduction at your earliest convenience.

National Semiconductor

CIRCLE 42

ANALOG, MIXED-SIGNAL IC DESIGN TOOLS IMPROVE FILTERS, PROCESS LAYOUT

Two analog and mixed-signal IC-design tools, Explorer AutoFilter and AutoLinear, from Silicon Compiler Systems, create accurate schematic, simulation, and layout views of a desired analog function. They do this by specifying desired performance levels across all key parameters and by accessing the software's embedded knowledge and numeric-optimization algorithms.

AutoFilter is tailored to designers of analog filters. It provides a single unified design environment that encompasses all of the key steps in a switched-capacitor filter design, from the initial response specification to process-specific layout. Using a combination of graphic-filter performance capture, flexible and comprehensive synthesis algorithms, and automated layout techniques, a filter can be synthesized in less than one hour using a workstation.

AutoLinear, an automatic synthesis and module-generation tool, takes an input from a high-level specification and creates a process-specific layout for analog building blocks. This is typically required for analog or mixed-signal chip design. Its circuit-synthesis capabilities account for the process, temperature, and voltage variation effects of a design. In addition, the logic-synthesis functions address such issues as transistor matching and noise coupling. Throughout the layout process, the designer can see the intermediate results and can manually override the system. The analog building blocks used in AutoLinear include op amps, comparators, voltage and current references, resistors, capacitors, and transistors.
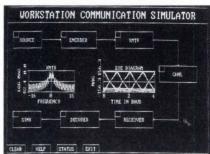
The tools fit into SCS's existing line of IC design tools. Both will be available in December. Prices start at $40,000 for Sun-3 or Apollo DN4500 versions.

Silicon Compiler Systems, 2045 Hamilton Ave., San Jose, CA 95125; (408) 371-2900.   **CIRCLE 315**
RICHARD NASS

PC TOOL SIMULATES COMMUNICATION LINKS

A PC-based communication simulation environment provides the necessary tools to enable the interactive design and evaluation of complex digital communication systems. With the Workstation Communica-

tion Simulator (WCS), users can model and analyze general point-to-point communication links for military, commercial, and space applications. It provides high-level graphical access to a wide variety of functional modules to implement the various functions in an end-to-end digital communication link. These modules include modulators and demodulators, encoders and decoders, filters, and a choice of realistic channel models. WCS runs on IBM PC, XT, AT, and compatible computers equipped with an enhanced graphic adapter (EGA) and math coprocessor. It sells for $4500.

Icucom Corp., P.O. Box 187, Wynantskill, NY 12198; (518) 274-7711.   **CIRCLE 333**

SOFTWARE INTEGRATES PLD SCHEMATICS

The PLDlinx Schematic Translator allows designers to describe their PLD designs with schematics and download the design to a PLD design package for optimization and fusemap generation. The software works between Data I/O's Future Net DASH schematic designer or DASH-PLD schematic capture packages and ABEL PLD Design software or Gates Logic Synthesizer software packages. Schematics can be entered hierarchically using any collection of symbols, including generic gates and flip-flops or any off-

the-shelf part that maps into a Boolean equivalent. It offers universal support for all of the PLD device manufacturers, covering more than 200 distinct architectures. PLDlinx is available for 286- and 386-based MS-DOS machines, as well as the Sun-3. Respective prices are $495 and $995. Delivery takes four to six weeks.

Data I/O Corp., 10525 Willows Rd. N.E., Redmond, WA 98073; (206) 881-6444.   **CIRCLE 334**

SPICE SIMULATOR HANDLES OVER 3000 COMPONENTS

Circuit designers using any 80286-based PC can take advantage of their extended memory to run in-circuit simulations involving more than 3000 components. IsSpice/286, a Berkley Spice-compatible simulator, runs in protected mode under DOS 3.1 and above. It requires an 80287 coprocessor and at least 1 Mbyte of conventional memory. One Mbyte of extended memory is also required for 3000-plus component simulations. The software sells for $200.

Intusoft, P.O. Box 6607, San Pedro, CA 90734; (213) 833-0710.   **CIRCLE 335**

CAD DATA DRIVES TOOLING, PRODUCTION

Tricam, a new service offered by pcb manufacturer Triangle Circuits, uses vendors' original computer-aided-design data to control and automate photoplotting, tooling, manufacturing, and testing of printed circuit boards. It is compatible with all CAD systems and accepts CAD files directly from modem, magnetic tape, or disk. The digital connection not only cuts turnaround time, but also ensures precision and accuracy. The CAD data is sent directly to a high-speed photoplotter to produce original photoplots and first-generation panelized films. Through Tricam, CAD data is used to generate N/C files for production tooling.
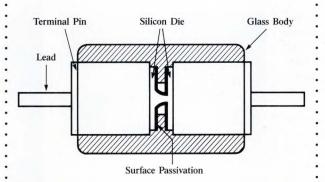
Triangle Circuits of Pittsburgh Inc., 931 Third St., Oakmont, PA 15139; (800) TRI-CAMM or (412) 828-5322.   **CIRCLE 336**

The Shape Of Things To Come At The Price Of Times Still Here

- ✓ **No cold start problems**
- ✓ **No intermittence problems**
- ✓ **No particle problems**

The totally new Unibond 1N4148-1 and 1N4150-1 diodes are not afraid of mechanical damage when temperature cycles up and down. They work well in potted environments and multilayer circuit boards. They're impervious to intermittent open problems, particle contamination, and shorting.

They're mechanically and electrically superior to any small signal diode you've ever seen because they're built with Unitrode's proprietary new die construction. There's no

Terminal Pin — Silicon Die — Glass Body — Lead — Surface Passivation

THE UNIBOND™

1N4148-1 JTX, JTXV
AND
1N4150-1 JTX, JTXV

In accordance with MIL-S-19500/116 and MIL-S-19500/231

more silver button and none of the problems commonly associated with conventional DO-35s. The only thing that's the same is the price.

Tomorrow's technology at today's prices:

As members of Unitrode's Unibond family of diodes, the 1N4148-1 and 1N4150-1 are built for rugged dependability, with features that include equal anode and cathode bond areas, a superior metallurgical bond that won't let go, and a non-cavity construction per MIL-S-19500.

See the future for yourself:

You can judge the shape of things to come for yourself. Just attach the coupon to your letterhead, send it to us, and we'll send you a free sample.

Attached is my letterhead. Please send me a Unibond diode sample.
I would like a (check one) ☐ 1N4148-1 JTX   ☐ 1N4150-1 JTX

Name _____ Title _____

Company _____ Mail Stop _____

Street _____

City _____ State _____ Zip _____

SEMICONDUCTOR PRODUCTS
UNITRODE
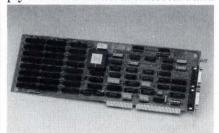
PC/AT Board Flaunts 50-MHz DSP Chip, Four Memory Configurations

PC/AT users can now have the power of the AT&T 50-MHz, floating-point digital-signal processor at their disposal with a set of add-in boards from Burr-Brown Corp. The ZPB34 family of DSP boards also includes four standard configurations of local RAM. Applications targeted for the ZPB34 DSP board include hardware development, floating-point accelerators, real-time tasks, and DSP algorithm development.

The AT&T WE DSP32C processor runs at 25 MFLOPS and executes a 1024-point complex fast-Fourier transform in 3.2 ms. This speed results from the chip's hardware multiply-and-accumulate architecture and

pipelined data processing. In addition, the processor's DMA controller may be set up to read and write data from the serial-I/O ports without interrupting the processor.
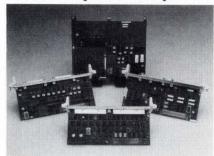
A high-speed serial bus transfers data between the processor and I/O cards. Data can also be transferred on and off the DSP board through the PC/AT parallel bus. Two sets of buffered, serial-I/O connectors work with internal or external devices. These devices may include other boards, or digital-to-analog and analog-to-digital converters to translate data to and from the real world.

The ZPB34 DSP board for the IBM PC/AT comes fitted with 64-, 192-, 320-, and 576-kbytes of on-board RAM. In single quantities, the boards cost $1995, $2995, $3495, and $4995 for the respective memory configurations.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (800) 548-6132. **CIRCLE 316**

LISA GUNN

Stackable Multibus II Architecture Decouples CPU From I/O Modules

A set of Multibus II boards from Intel Corp. is built with the new Modular Interface Extension (MIX) architecture that uses a 32-bit asynchronous-I/O bus for on-board I/O expansion. The products

include a baseboard, terminal controller, and wide- and local-area-network controllers.

A typical MIX I/O subsystem consists of an intelligent MIX baseboard and one to three stackable MIX modules that are linked by a special connector. The MIX bus uses a round-robin arbitration scheme between the baseboard and its modules.

The MIX 386/020 baseboard is a full Multibus II board containing a 20-MHz 80386 CPU, a message-passing coprocessor, and an 82258 advanced DMA controller.

Three MIX modules are available. The MIX 450 module is a 12-channel, asynchronous terminal controller. A high-performance communications module, the MIX 420, sports two independent wide-area-network interfaces that offer peak transfer rates of 64-kbits/s. An 82586 local-area-network coprocessor and an 82501 Ethernet serial interface power the MIX 560 Ethernet module.

The MIX 386/020 baseboard with 1 Mbyte of memory costs $2195. Additional memory, up to a total of 17 Mbytes, goes for $700 per Mbyte. The MIX 420, MIX 450, and MIX 560 cost $1200, $1100, and $1000, respectively. All products will be available in December.

Intel Corp., 5200 NE Elam Young Pkwy., Hillsboro, OR 97124-6497; (800) 548-4725. **CIRCLE 317**

LISA GUNN

VMEBUS CPU BOARD IS THE FIRST TO EXPLOIT INTEL'S 960CA RISC CHIP

Targeted at real-time control applications such as communications and image processing, a VMEbus board from Heurikon Corp. is the first to use Intel's new 960CA RISC chip. In addition to the processor, the HK80/V960E board features on-board SCSI and Ethernet interfaces, and zero-wait-state memory access.

When operating at the peak frequency of 40 MHz, the 960CA processor delivers 66 native MIPS and 30 VAX MIPS. The chip includes 1 kbyte of instruction cache, 1 kbyte of static RAM, and a four-channel 32-bit DMA controller.

Memory support for the HK80/V960E board includes either 2- or 8-Mbytes of 70-ns, dual-access, static-column RAM. By using a two-way interleaved architecture, accesses for single-write or burst transfers take place with no wait states. One Mbyte of EPROM and 128 bytes of nonvolatile RAM are also available.

To maximize the board's integration capabilities, Heurikon built in the VMEbus Interface Consortium's VIC068 single-chip VMEbus interface. The chip implements the full VME interface, including 32-bit data and address paths, seven bus interrupts, and master and slave operation. The interface peaks at transfer speeds of 40 Mbytes/s.

An assortment of networking and I/O capabilities makes for easy system integration. Ethernet is supported by Intel's 10-Mbytes/s, 32-bit local-area-network processor. The board also includes Western Digital's SCSI processor.

The board works with a variety of Unix development hosts. The Unix hosts and the HK80/V960E board are linked with the VxWorks cross-development environment.

A 33-MHz version of the HK80/V960E CPU board, with 2 Mbytes of memory, costs $2795 in quantities of 100. The board will be available in the first quarter of 1990.

Heurikon Corp., 3201 Latham Dr., Madison, WI 53713; (800) 356-9602. **CIRCLE 318**
LISA GUNN

OPTIMIZED THROUGHPUT EXTENDS TESTER LINE TO ASIC PRODUCTION

In an effort to cover all the bases in the ASIC test field, Hilevel Technologies has introduced the Topaz-V_P, a low-volume production tester. Unlike earlier Topaz models, which emphasized design debugging and failure analysis, the Topaz-V_P is optimized for process verification, pass-fail testing, and throughput.

The new tester comes in two versions, the Topaz-V_{P320} and the Topaz-V_{P544}, which can be configured for 320 and 544 pins, respectively. Both models feature the same specifications as the Topaz-V_A testers, which are aimed at ASIC verification, characterization, and failure analysis. Features include a 110-MHz test rate, 100-ps timing resolution, ±500-ps pin-to-pin skew, up to four device-under-test power supplies, and support for various scan-testing techniques.

To boost throughput, the new units have one dc precision measurement unit for every 16 I/O pins. For a typical 192-pin ASIC, it would take less than 1 minute to perform a

100,000-vector functional test, 25 ac parametric tests, and 25 dc parametric tests. Also, users can program slew rates on a per-pin basis from more than 1.5 V/ns to 0.2 V/ns. As a result, the tester can maintain fast edges at CMOS signal levels without sacrificing overshoot characteristics on smaller ECL signals.

The Topaz-V_P starts at $150,000 for a 32-pin unit and goes to $935,000 for a 544-pin model. The system is available immediately.

Hilevel Technology Inc., 31 Technology Dr., Irvine, CA 92718; Milton Ellis, (714) 727-2100.319

JOHN NOVELLINO

AUTOMATED SYSTEM DOES MIL-STANDARD ESD TESTS ON SEMICONDUCTORS

Engineers no longer need custom-built or manual systems to test their semiconductors for susceptability to electrostatic discharge. The Model 335 ESD test system from TriSys Inc. performs such tests up to 10 times faster than manual systems.

The Model 335 generates pulses to 8000 V in assigned steps, using the human-body model waveform specified by MIL-STD-883C. The system applies the pulses to any pin combination on devices with up to 320 pins. The results of the pin-to-pin testing are printed out as point-test analysis and curve-trace analysis reports. With these reports, users can classify and certify devices or profile breakdown characteristics.

Besides the pulse generator, the Model 335 includes a failure-analysis module for precision parametric measurement and characterization; software for test development, execution, and data logging; and an IBM-compatible controller. To detect performance changes, the failure-analysis module makes measurements before and after the device is stressed.

The software, which is based on Microsoft Windows, lets users run built-in routines that conform to the military standard. Operators can also create custom tests with a menu-driven process using a mouse to select device-under-test, pin count and combination, voltage steps, timing intervals, and measurements.

The Model 335 ESD test system starts at $43,500. Delivery is within 4 to 6 weeks after receipt of order.

TriSys Inc., 15242 Greenbriar Pkwy., Beaverton, OR 97006; (503) 645-5504. **CIRCLE 320**

JOHN NOVELLINO

ROM EMULATION SUBSYSTEM TESTS MICROPROCESSORS ON FUNCTIONAL TESTER

ROM emulation techniques can now be used to test microprocessors on Summation's SigmaSeries Functional Test System. The EMX10 ROM emulation subsystem handles a variety of devices, including Intel's 80486 and Motorola's 68030.

The subsystem is based on the company's patented emulation technique, but features a new architecture that includes a dedicated 68000 processor for higher performance. Because the module executes high-level-language, CPU-independent programs at high speeds, assembly-

language routines rarely need to be run on the target processor. Control and programming is handled within Summation's TestCASE Functional Test and Development Environment.

The EMX10 contains a reprogrammable Logic Cell Array (LCA) that performs two functions. In normal operation, the LCA handles the Cross Trigger bus signals that provide triggering and synchronization between the EMX10 and other SigmaSeries modules. In the kernel diagnostic mode, the array is reconfigured to collect diagnostic data from the failed CPU kernels. This arrangement eliminates the need for dedicated hardware.
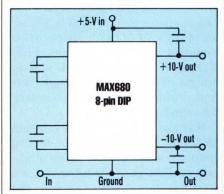
Fully configured to test an average high-end 32-bit microprocessor, the EMX10 subsystem costs about $7500. Delivery is scheduled for early in the first quarter of 1990.

Summation Inc., 11335 N.E. 122nd Wy., Kirkland, WA 98034; (206) 823-8688. **CIRCLE 321**

JOHN NOVELLINO

PUMPING CHARGE, NOT IRON, CMOS ICS TAKE 5 V IN, PROVIDE ±10-V OUT

By connecting from +2 to +6 V between the input pins and grounds of Maxim's MAX680 or MAX681 ICs, they deliver between ±4 and ±12, respectively, from their output pins. One output provides the positive voltage, the other the negative voltage. These dual, voltage-doubler charge pumps can put out up to 10 mA from each output at a typical source impedance of 150 Ω.
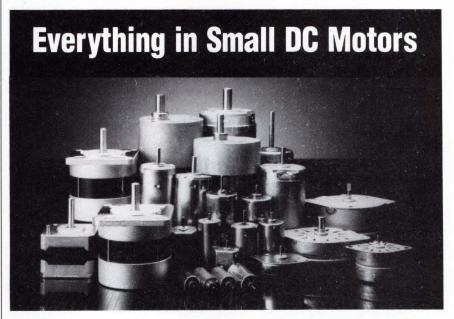
Like the standard 7660 +5-to—5-V converter which they resemble, these are not regulators. Use them with a load of a few hundred microamperes from a 10-V source, and they provide ±10 V at their terminals. Pull 10 mA from each output and the the voltages drop to under 7 V from the MAX680's positive output and at least 0.5 V less than that from the positive output of the MAX681. The negative charge pump takes its input from the output of the positive pump. As a result, the MAX680's negative output drops to under 6 V, while that of the MAX681 falls to below 5 V. The drop in output voltage, basically a function of the internal resistances of the CMOS switches on the chip and the output capacitors, is a direct linear function of the load current.

The 8-pin MAX680's outputs drop less for a given load current because it needs four large external capacitors, each 1 to 20 μF or more. The MAX681, for its part, has smaller capacitors inside its larger 14-pin DIP. Therefore, depending on the application, a tradeoff is available between the two devices: a small package with external capacitors and control over voltage versus load, or a slightly larger package and no external capacitors to take up additional board space. In quantities of 100, the MAX680 starts at $2.16 and the MAX681 at $3.64. Delivery is from stock.

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; Jim Dekis, (408) 737-7600.
CIRCLE 322
FRANK GOODENOUGH

POWER FET DRIVER TAKES LOGIC IN, OPTIMIZES GATE DRIVE AND PROTECTS FET
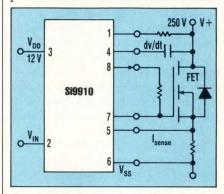
Dubbed an Adaptive Power MOSFET Driver, Siliconix's Si9910 ushers in a second generation of these driver ICs. They are designed to convert 5-V logic into the fast, high-current pulses needed to drive the capacitive load represented by large power MOSFETs. They should, however, serve any application calling for charging 2000 pF to 12 V—in under 100 ns.

The device can source and sink peak currents of 1 A. To this drive capability, Siliconix has added fault protection for the FET and its load. The fault protection senses an undervoltage or output short-circuit condition and turns off the FET. Maximum di/dt is limited, and in bridge circuits, shoot-through current during diode reverse-recovery time can be limited.

Many applications will be found in half- and full-bridge motor-control circuits where the device's low quiescent current (just 500 μA maximum with the output low) fits it to the high-side drive job while running off a floating bootstrap or charge-pump power source. A second Si9910 han-

dles the simpler low-side drive. When the output is high, quiescent current is a mere 1 μA. A non-inverting Schmidt trigger input, with 1 V of hysteresis, sets the state of the output drive for the MOSFET's gate. The voltage on pin 8 turns the FET on, while pin 7 turns it off.

If the supply voltage on pin 3 is below 9 V, the output will not go high. Pin 1 senses the voltage across the FET when it is on. If the voltage is too high, the Si9910's output is latched low.

The driver comes in plastic 8-pin DIP (Si9910DJ) and SOIC (Si9910DY) packages and is rated from –40 to +85°C. In quantities of 100, the Si9910DJ goes for $1.71. Small quantities are available from stock.

Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054; Bill Numann, (800) 554-5565, ext. 1400. **CIRCLE 323**
FRANK GOODENOUGH

ANTI-ALIASING 9-POLE LOW-PASS FILTERS ARRIVE IN STANDARD MODULES

Aimed at anti-aliasing applications in front of high-resolution analog-to-digital converters, the 5BAF family of 9-pole low-pass filters from Frequency Devices come in a standard modular package. These active RC filters plug into backplanes offered by Analog Devices, Data Translation, and Metra-Byte, from which they take 5 V. An internal dc-to-dc converter powers the module's circuits.

With an ultimate rolloff rate of 54 dB/octave, the filters are offered with either Butterworth or Bessel responses. The former exhibit the maximally flat passband and the monotonic rolloff of the classical Butterworth function. The Bessel types offer their expected overshoot-free transient response, linear phase characteristics and monotonic rolloff. Both functions are available with factory-set standard 3-dB frequencies of 1, 2, 5, 10, 20, and 50 kHz. Custom corner frequencies are optionally available.

Designed to condition real-world signals, the filters sport a differential input circuit with a common-mode rejection ratio of at least 74 dB at 1 kHz and a typical input impedance of 20 kΩ. Fixed differential gain is unity $\pm0.03\%$ at dc. The filters meet specifications with a ±10-V input in the presence of ±20 V of common-mode voltage. Either of the device's inputs take ±40 V, with power on or off.

Typical output offset is ±3 mV, while offset drift is 100 μV/°C. Output noise over a dc-to-50-kHz bandwidth is typically just 75 μVrms. With a ±10-V square-wave input, the output drives 1500 Ω in series with 0.002 μF. In quantities of 100, the standard devices go for $95 each. Delivery ranges from 3 weeks for standard to 5 weeks for custom models.

Frequency Devices Inc., 25 Locust St., Haverhill, MA 01830; Frank DeGiso, (508) 374-0761.

CIRCLE 324
FRANK GOODENOUGH

COMPLETE FLASH ADC SAMPLES AT 50 MHZ, RUNS ON JUST 560 MW OF POWER

Most flash analog-to-digital converters need both an external reference and a fast buffer amplifier between the input signal and the input pin. Moreover, even if they sample faster than 20 MHz without those external ICs, they need a watt or more of power. But Sipex has added both those chips to a low-power bipolar flash converter from Philips-Signetics and came up with a hybrid that spits out 8-bit digital words at 50 MHz. Dubbed the SP1078, the converter draws a maximum of just 561 mW from its two positive and one negative 5-V rails. The flash converter uses what is called a folded architecture. Instead of 255 comparators, it cuts power drain by including just 64.

At dc, differential and integral nonlinearity (DNL and INL) errors run a maximum of 0.4 and 0.6 LSB, respectively, over temperature. Dynamic specifications are in a similar class. With a 5-MHz input signal, DNL is typically 0.6 LSB and is no more than 0.9 LSB with 8.89 MHz in. With 8.89 MHz in, signal to noise plus distortion (SNAD) is a minimum of 39 dBc. That translates to 6.2 effective bits. Drop the input frequency by a factor of 4 and SNAD rises to 44 dBc and effective bits to 7. There are no missed codes.
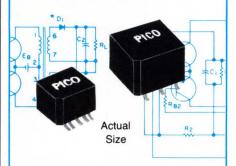
Aperture uncertainty, or jitter, is typically 50 ps, which is reflected in the converter's full-power bandwidth of 10 MHz. Small-signal bandwidth is roughly 20 MHz. Because the amplifier's full-power bandwidth is 50 MHz, it should not degrade any signal the converter can handle. For example, the converter can directly down-convert a 10.7-MHz signal from an if amplifier.

In quantities of 100, the commercial-temperature-grade SP1078C goes for $183. The B-grade military-temperature range costs $306. Small quantities are available from stock.

Sipex Corp., 6 Fortune Dr., Billerica, MA 01821; Jay Cormier, (508) 663-7811.

CIRCLE 325
FRANK GOODENOUGH

BUS-CONTROLLER CHIP PROVIDES MASTER-MODE INTERFACE TO PC BUSES

In simplifying the design of add-in cards for either IBM PCs and compatibles or Nubus-based systems, NCR Corp.'s 86C05 bus-controller chip packs all the control logic as well as 11 drivers that can handle up to 24 mA each. The CMOS chip was created as a universal solution for intelligent add-in cards. Data is transferred at sustained rates of up to 20 Mbytes/s thanks to a 32-word-by-32-bit FIFO buffer on the chip. Block data transfers can be programmed over a 1 to 64 range.

On the host side, the 86C05 IC's programmable interface can tie into buses such as Micro Channel, PC-AT, EISA, and NuBus. It provides a 24-bit address bus for the first three, and a 32-bit address for NuBus systems. Host-bus interrupts and arbitration priority are also programmable. On the bus-master-board side is a microprocessor interface to tie into the board's local intelligence. That local intelligence can maximize the efficiency of data flow.

Also on the chip is a 32-bit data path that can be programmed for 8-, 16-, or 32-bit transfers, and a DMA controller that performs 8- or 16-bit transfers with optional even or odd parity over each byte. Data can be transferred in any direction between the host, the DMA channel, and the microprocessor interfaces. The 86C05 operates at clock rates of up to 40 MHz.

The bus-control circuit also includes a BIOS memory interface so that a local EPROM on the add-in card can configure the chip upon system power-up. The multiple interface buses on the chip push the pin count up to 160. Thanks to the low-power CMOS circuitry, though, the chip consumes about 250 mW, low enough to be housed in a plastic quad-sided flat package. In quantities of 1000, the chip sells for $36.25. Samples are available from stock.

NCR Corp., 1635 Aeroplaza Dr., Colorado Springs, CO 80916; Jack Brown, (719) 596-5795. **CIRCLE 326**
DAVE BURSKY

DIGITAL MICROPHONE CAPTURES STEREO SOUND, DELIVERS SERIAL DIGITAL

With a software-selectable digital sampling rate of 88.2 kHz down to 5.5 kHz, the DM-N digital microphone captures dual channels of audio, digitally encodes the signals into 16-bit words, and then ships those words in serial fashion to a host computer. Ariel's first version of the microphone ties directly into the NeXT computer's

digital-signal-processor port. This transforms the system into a digital-recording system for music, data acquisition, and voice recognition.

Based on a pair of oversampling analog-to-digital converters, the microphone includes twin analog pickups, software-controlled preamplifiers, and serialization circuitry. In addition, the microphone's two line inputs accept prerecorded analog signals for direct feeds into the digitization section.

The microphone boasts a dynamic range of up to 92 dB and total harmonic distortion of less than 0.005%—a result of the 16-bit oversampling a-d converters. Because the microphone can be controlled from the host computer, five different sampling rates are possible, including the 44.1-kHz audio standard.

Included with the microphone are a removable windscreen, cables, and a user manual. In single quantities, the digital microphone sells for $595 and is available from stock.

Ariel Corp., 433 River Rd., Highland Park, NJ 08904; Les Listwa, (201) 249-2900. **CIRCLE 327**
DAVE BURSKY

ECL RAM OFFERS SPEED, POWER CHOICES

A 4-kbit ECL static RAM comes in two speed-power ranges, suitable for use in high-performance computers and superminis, instrumentation, and cache memories. The GXB 100474A operates in two modes: the standard SRAM mode and a self-timed STRAM mode. Typical access time for the A1 version of the device is 3.5 ns with a maximum of 5.0 ns at a power dissipation of about 1.4 W. Typical access time for the A2 version is 4.5 ns with a maximum of 6.0 ns at a power dissipation of 1.0 W. Because additional I/O latches are provided on-chip, system cycle times can be reduced from approximately 10 ns to 5 ns in the STRAM mode of the high-speed A1 version, allowing system clocks of up to 200 MHz. Prices range from $30 to $40, depending on mode, speed, package, and quantity. Small quantities are shipped from stock. Lead time for large quantities is 6 to 10 weeks.

Siemens Components Inc., 2191 Laurelwood Rd., Santa Clara, CA 95054; (408) 980-4566. **CIRCLE 337**

1-MBIT ROMS DOUBLE CONTROL-PIN OPTIONS

In addition to fast response times, the 631000 series of 1-Mbit ROMs offers double the control-pin options of most comparable ROM products. The 28-pin 631000 and 32-pin 631001 are available with 150- and 200-ns access times and up to four user-definable control pins. System designers can link as many as 16 of the CMOS ROMs on a single data bus. Such configurations are particularly useful for computer peripheral applications, such as laser printers, which demand large amounts of memory. Packaging options include 28- and 32-pin DIPs, as well as 32-pin plastic leaded chip carriers. Devices may be specified for operation over commercial, industrial, and military temperature ranges. Pricing starts at $5.50 in lots of 10,000.

Gould AMI, 2300 Buckskin Rd., Pocatello, ID 83201; (208) 234-6851. **CIRCLE 338**

ELECTROSTATIC PLOTTER DELIVERS 400-DPI COLOR COPY WITH SINGLE PASS

The first color electrostatic plotter to require only one pass of the paper through its mechanism has arrived. The ColorWriter 400 delivers 400-dot-per-inch printing resolution while printing 36-in. wide full-color images at a maximum rate of about half-an-inch per second. Within the intelligent system is an embedded Sun 3 CPU that manages the plot requests in a networked environment. Multiple jobs can be concurrently processed.

Data can be sent to the plotter by means of Ethernet using the TCP/IP Level 2 protocol, or over any of several standard parallel interfaces. After spooling the data in an industry-standard format on its embedded hard-disk drive (155, 315, or 620 Mbytes), the plotter's Sun CPU processes the files to create a special internal format. The newly formatted data is then sent to an output disk, which feeds the data to the graphics engine. That engine controls the distribution and mix of specially prepared liquid colors. The graphics engine rasterizes the data on the fly.

Avoiding the need to make as many as five paper passes through the printer lets the ColorWriter 400 handle images of almost any length since no plot registration is required, and no mechanical take-up and feedback system is needed. As a result, the mechanical portion of the 46-by-63-by-44-in. system is much simpler than that of multipass plotters. The system accepts GDS II Stream, HPGL, Versatec Random Format, and Calcomp data-format images, and can plot the images at paper speeds of 0.5, 0.25, or 0.125 ips.

Depending on interface type, disk drive capacity, and other options, the 1400-lb. plotter sells for between $115,000 and $130,000. Systems are available two months after receipt of order.

Synergy Computer Graphics Corp., 260 Santa Ana Ct., Sunnyvale, CA 94086; Brian Powers, (408) 749-8600. **CIRCLE 328**
DAVE BURSKY

CONTINUOUS BACKUP SYSTEM FOR NETWORKS CUTS HASSLES, AVOIDS LOST DATA

By continuously inscribing data on an optical disk as a function of time, the RetroChron backup system for local-area networks eliminates time-consuming system backup and possible data losses. The real-time process ensures the rapid restoration of lost data, provides crash protection, and performs complete system recovery in the event of partial or complete disk failure.

When data losses occur, the system operator can select the precise prior date and time to return to. The RetroChron system will create a virtual device containing the data exactly as it existed at that time. From this virtual device, users can then restore files or entire directories using the familiar DOS copy command. During the restoration process, normal network operations are uninterrupted.

In the event of a hard-disk crash, the backup system allows the network to continue operating from the optical disk. When the damaged hard disk is replaced, the RetroChron system provides a seamless restoration of the disk and its data without a lengthy formatting and system-rebuilding process.

The system was created for networks built around IBM PC/AT-compatible file servers with storage devices having capacities of greater than 150 Mbytes. The network should use Novell or 3Com networking software. Packaged as a standard AT card, the RetroChron system uses a 10-MHz 80186 CPU and has 1 Mbyte of local memory. The host interface is accomplished by means of a 16-bit FIFO and direct memory access with a FIFO-transfer rate of 2.5 Mbytes/s.

The RetroChron system is distributed through value-added resellers. Pricing for a minimum order of 10 units is $4995 each. Small quantities are available from stock.

Vortex Systems Inc., 800 Vinial St., Suite 406, Pittsburgh, PA 15212; (412) 322-7820. **CIRCLE 329**
DAVID MALINIAK

HIGH-FREQUENCY BURN-IN SYSTEM BRINGS HEAT DIRECTLY TO PACKAGES

Large convection ovens and liquid burn-in systems are eliminated by the Bak-Pak high-frequency burn-in system from EJ Systems Inc. The system brings a new twist to the burn-in process by bringing conductive heat directly to the device-under-test's case. The process also eliminates the need for producing burn-in boards made of costly high-temperature materials.

A closed-loop conductive heating method offers extremely accurate control ($\pm 2°C$) of the device's case temperature. In comparison, convection burn-in ovens control only the air temperature to $\pm 3°C$, but because the device itself dissipates heat, it is difficult to determine the

case's temperature.

Also, the Bak-Pak driver electronics can be placed directly on the burn-in board, which yields excellent signal quality up to 40 MHz. In standard ovens, the driver electronics must be mounted externally and are usually about 30 in. from the device positions. This decreases signal quality by permitting frequencies up to only 10 MHz.

The Bak-Pak burn-in system costs from $10,000 to $50,000 depending on configuration and is available in about 8 weeks from receipt of order.

EJ Systems Inc., 360 Merrimack St., Lawrence, MA 01843; (508) 689-0136. **CIRCLE 330**

DAVID MALINIAK

BLANKET-TUNGSTEN CVD SYSTEM CUTS COSTS WHILE IMPROVING WAFERS

With the introduction of its Precision 5000 WCVD system for blanket tungsten deposition, Applied Materials has ironed out some of the historical problems in film quality and operating efficiency associated with blanket tungsten in semiconductor manufacturing. The system boasts outstanding step coverage and film smoothness. Its high aspect-ratio filling of submicron devices improves their reliability and also reduces the potential for lithographic difficulties.

The new blanket-tungsten system is based on the proven technology of the earlier Precision 5000 CVD system. The flexibility and wide range of processes available for that earlier system makes the Precision 5000 WCVD system capable of many CVD tasks, including plasma nitride passivation and doped and undoped oxides.

The system's in situ self-cleaning chamber design virtually eliminates lengthy downtimes for cleaning and requalification, which is common in batch-type tungsten systems. The self-cleaning technology results in a minimum of particulates. In addition, slow-pump and vent-through diffusers create a minimum of turbulence, which reduce the number of airborne particulates. Also, because of a unique wafer-handling system, deposits on the backside of the wafer are eliminated.

A modular design allows up to four process chambers per system. The independent chambers are designed with a self-aligning, bolt-on capability for easy expansion of throughput or process. The system handles wafers in sizes from 100 to 200 mm.

The Precision 5000 WCVD system costs about $1,000,000 for a two-chamber system with mainframe. Delivery is in four to five months from receipt of order.

Applied Materials Inc., P.O. Box 58039, Santa Clara, CA 95052; (408) 727-5555. **CIRCLE 331**

RECEPTACLES HOUSE DISK-DRIVE MECHANISMS

Drive mechanism receptacles, designed for mass-storage units in 3U, 4U, and 6U subracks and enclosures, accommodate floppy- and hard-disk drives in 3-1/2- and 5-1/4-in. formats. They also accommodate both full- and half-height drive configurations. The mounting holes on the holders are positioned to fit most models. Special arrangements are made to insert an SCSI controller card, which can be inserted on card guides in the enclosure or card cage.

Elma Electronic Inc., 41440 Christy St., Fremont, CA 94538; (415) 656-3400. **CIRCLE 339**
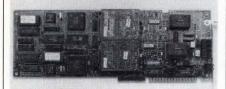
LITHOGRAPHER DOUBLES COMPLEX IC THROUGHPUT

A new generation of high-performance scanned-laser lithography systems for mask making offers a 20% overall improvement in pattern-quality specifications. It also doubles the throughput for high-density advanced semiconductor circuits. The CORE-2100 combines enhancements to both its hardware and software to meet the increasing requirements of advanced ICs using one-, five-, and ten-times reticles and one-times masks, such as 250-kgate arrays and 1- and 4-Mbit DRAMs. These include an enhanced rasterizer engine, increased disk capacity, and support of MEBES compacted data format. Existing formats are Standard EBES, MEBES I/II, MEBES Reticle Mode, MEBES Extended Address, and Varian ALF.

The plotter's substrate handler has been adapted to accept 7-in. square plates up to 1/4-in. thick. And an improved steering mirror control and response provides a 25% placement-performance improvement. Production deliveries of the scanned-laser lithography system will be in the second quarter of 1990. First-generation upgrade kits will also be available then. The CORE-2100 will sell for $2.25 million.

Ateq Corp., 9100 Gemini Dr., Beaverton, OR 97005; (503) 626-3051. **CIRCLE 340**

FACSIMILE CARD ROUTS MAIL TO RECIPIENTS IN LAN-SERVER ENVIRONMENTS

Two complete facsimile transceivers are packaged on one TR112 twin-channel facsimile card from Brooktrout Technology. The IBM PC/AT-compatible card permits incoming facsimile messages to be automatically routed to recipients in local-area-network fax-mail server environments.

The card is aimed at developers of large, multichannel fax-mail systems and applications. These include fax-mail servers for networks, electronic-mail-to-facsimile services, facsimile store-and-forward services operated by telephone companies, and integrated facsimile and voice response systems.

By packing two complete transceivers, the card doubles the number of channels that can be accommodated in a PC/AT or compatible system. As a result, half as many system units are needed to support a given number of channels, which substantially reduces the cost of developing multichannel applications. A single system can hold as many as six TR112 cards, or 12 channels.

The card's autorouting scheme takes advantage of the direct inward dialing (DID) services provided by telephone companies. These services permit outside callers to dial internal extensions directly. Optional DID circuitry on the TR112 card allows each user of a multichannel facsimile system to be assigned a personal telephone number that can be directly dialed by outside callers.

In single quantities, the basic TR112 card costs $1995. The autorouting version goes for $2495. Small quantities are delivered from stock.

Brooktrout Technology Inc., 110 Cedar St., Wellesley Hills, MA 02181; (617) 235-3026. **CIRCLE 332**
DAVID MALINIAK

DATA-COMM SYSTEM IS EASILY CUSTOMIZED

Single-board hardware platforms allow OEMs to accelerate product development by providing them with an easily customized, off-the-shelf communication system. In addition to the hardware, the CPS 1000 family consists of communication software modules (including both object and source code options) and target development systems. CPS 1000 components can be customized into such products as LAN gateways, front-end processors, bridges, PADs, or hub switches for a broad range of networking applications. The systems can simultaneously support multiple protocols, including X.25, TCP/IP, Ethernet, and token ring. Serial ports can be independently configured with RS-232-C, RS-449, RS-530, and V.35 interfaces. Pricing for the base hardware ranges from $1500 to $9300.

SBE Inc., 2400 Bisso Lane, Concord, CA 94520; (800) 221-6458 or, in Calif., (800) 328-9900. **CIRCLE 342**

HYBRID SOLVES T1 LINE EQUALIZATION

Integrating 17 components into a single hybrid device, the XR-TM044H provides ISDN primary rate line equalization of up to 36 dB of cable loss. The single-in-line hybrid also features an automatic line-build-out (ALBO) feedback and filter network, along with a preamplifier gain and compensation circuit. Together with Exar's XR-C277 repeater IC, the part forms a complete T1 front-end repeater or receiver circuit for 1.544- and 2.048-MHz applications. Its hybrid design offers significant space savings, as well as increased noise immunity compared with discrete solutions. The XR-TM044H is the first product to result from an exclusive licensing agreement between Exar Corp. and Thunder Road Communications Inc. It sells for $12.56 in quantities of 100 and is delivered from stock.

Exar Corp., 2222 Qume Dr., P.O. Box 49007, San Jose, CA 95161; (408) 434-6400. **CIRCLE 341**

NETWORK SOFTWARE FORMS SUPERCOMPUTER

A software package, called the PAX-1 Network Supercomputer, can turn a heterogeneous network of PCs, Macintoshes, RISC-based Unix workstations, VAX computers, and mainframes into a true parallel-processing network supercomputer. Initially based on TCP/IP networks, PAX-1 enables a 25-node network, 55% of which consists of PCs and Macintoshes, to generate processing power equivalent to a 3090/180 mainframe. A PAX-1 configuration of 25 RISC workstations packs the equivalent punch of a Cray X-MP/14se supercomputer. In addition to the server software, PAX-1 includes an Automated Systems Administrator (ASA) engine, which can start, stop, and manage systems, peripherals, and applications across the network. Pricing for unbundled server software starts at $9950 for a 25-node network. Unbundled client software, which starts at $450 for the MS-DOS, version is also lower without the ASA logic.

VXM Technologies Inc., Box 9121, Kenmore Station, Boston, MA 02215; (617) 730-8490. **CIRCLE 343**

MMIC ATTENUATOR SPANS DC TO 18 GHZ

Using three GaAs FETs in a π configuration, the HMR-11000 MMIC attenuator controls gain and interstage ripple with low insertion loss from dc to 18 GHz. The part, which can be used for gain control, switching, and amplitude-pulse modulation in both MMIC and MIC assemblies, can solve a wide range of signal control problems. Maximum current draw is specified at just 60 μA. Typical minimum insertion loss is 2.0 dB at 12 GHz. Typical maximum linear attenuation is 35 dB at 2 GHz and 15 dB at 18 GHz. The attenuator, which is 390 by 450 microns (15 by 18 mils), sells for $12.30 each in lots of 1000 and is shipped from stock.

Harris Microwave Semiconductor, 1530 McCarthy Blvd., Milpitas, CA 95035; (408) 433-2222. **CIRCLE 344**

INDEX OF ADVERTISERS

The advertisers index is prepared as an extra service. Electronic Design does not assume any liability for omissions or errors.

DISK SPECIFIES ADCS, DACS, MORE

Available at no charge, a disk-based component selection guide gives designers access to a functional data base containing over 1600 unique parts, including analog and digital signal processing devices and data converters. Using any IBM PC or compatible computer, a designer need only enter the minimum and maximum desired specifications. The selection guide searches its data base and displays up to 17 components meeting the desired criteria, along with their actual specifications. If the guide fails to find a device the meets the requirements, it expands the search parameters until it finds one or more devices that come close.

Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 02021; (508) 658-9400. **CIRCLE 345**

ASYST '88 CONFERENCE PROCEEDINGS

The *ASYST '88 International Conference Proceedings*, a 249-page publication, contains 48 application articles on PC-based scientific and engineering applications. The papers, which were presented at the ASYST '88 International Conference sponsored by Asyst Software Technologies Inc. and the Institute of Applied Forth Research Inc., cover such topics as data analysis, biomedical, instrumentation control, materials research, physics, and testing. Applications range from theoretical modeling to automated testing and computer-aided instruction. The document is available at a cost of $25.

Asyst Software Technologies Inc., 100 Corporate Woods, Rochester, NY 14623; (800) 348-0033 or (716) 272-0070. **CIRCLE 346**

JOURNAL ADDRESSES SIGNAL PROCESSING

Analog Dialogue is a technical journal on circuits, systems, and software for real-world signal processing. This issue, Number 23-2, highlights the ADSP-2101 monolithic CMOS microcomputer. Other application-oriented articles describe an isolated strain-gage module, the 5B38; two 6-bit monolithic flash converters, the 500-MHz AD9006 and AD9016; and the fastest-slewing monolithic op amp with wide bandwidth, the AD844. The column which addresses users' questions and problems features a discussion on voltage-to-frequency converters.

Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 02021; (617) 461-3043. **CIRCLE 347**

POWER CONVERSION DESIGN GUIDE

The 1990 edition of Calex's design guide and catalog contains detailed electrical specifications, performance curves, simplified schematics, mechanical specifications and dimensions, a quick locator section, and complete environmental data on more than 116 dc-dc converters. The 68-page publication also details over 50 low-power encapsulated modular power supplies. Single-piece pricing and ordering information is provided.

Calex Manufacturing Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523; (415) 932-3911. **CIRCLE 348**

TUTORIAL DESCRIBES SOURCE-MEASURE UNITS

A 24-page tutorial handbook covers the basic technology of a source-measure unit (SMU), a single instrument that is able to simultaneously source voltage and measure current or source current and measure voltage. Included are chapters that describe an SMU, how it works, designing test systems, sample test setups, and a glossary of terms. An applications handbook is also provided which details 24 typical source-measure test configurations. Each application contains detailed schematic diagrams.

Keithley Instruments, 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115. **CIRCLE 349**

TMOS POWER MOSFET DEVICES

This recently revised data book covering Motorola's line of TMOS power MOSFETs now includes the company's new high-energy logic-level power MOSFETs, surface-mounted DPAKs, GEMFETs, and SENSE-FETs. The comprehensive publication (DL135/D) provides reliability data, application and basic design information, a selector guide and cross reference, and data sheets for more than 380 standard devices. Application chapters discuss avalanche limitations, commutating safe operating area (CSOA), and dv/dt. It costs $3.45.

Motorola Literature Distribution Center, P.O. Box 20924, Phoenix, AZ 85063; (602) 994-6561. **CIRCLE 350**

ACQUISITION PRODUCTS RUN ON PCS

A six-page pamphlet presents an extensive line of data acquisition hardware, software, and accessories for IBM PC, XT, AT, and PS/2 computers, as well as Macintosh personal computers. Detailed technical specifications are given for a series of plug-in data acquisition boards that provide analog, digital, and timing input/output functions. Also covered are a variety of software packages that simplify the development of data acquisition, analysis, and presentation applications.

National Instruments Corp., 12109 Technology Blvd., Austin, TX 78727; (512) 794-0100. **CIRCLE 351**

To advertise call: Jeanie Griffin at (201) 393-6382

SPACE AVAILABLE

Call Linear Technology
800-637-5545

LT 1180/81
+ 4 x 0.1µF Caps

Rugged. Low Power. RS232 Space Saver.

Part Type	Drivers	Receivers	Power Supply Required	Shutdown	Drivers Fault Tolerant to ±25V	Charge Pump Cap Size Req'd.
LT1030	4	0	±12V	YES*	YES	N/A
LT1032	4	0	±12V	YES*	YES	N/A
LT1039	3	3	+5V, ±12V	YES*	YES	N/A
LT1039-16	3	3	+5V, ±12V	NO	YES	N/A
LT1080	2	2	+5V	YES*	YES	1µF
LT1081	2	2	+5V	NO	YES	1µF
LT1130	5	5	+5V	NO	YES	1µF
LT1131	5	4	+5V	YES*	YES	1µF
LT1132	5	3	+5V	NO	YES	1µF
LT1133	3	5	+5V	NO	YES	1µF
LT1134	4	4	+5V	NO	YES	1µF
LT1135	5	3	+5V, ±12V	NO	YES	N/A
LT1136	4	5	+5V	YES*	YES	1µF
LT1137	3	5	+5V	YES*	YES	1µF
LT1138	5	3	+5V	YES*	YES	1µF
LT1139	4	4	+5V, +12V	YES*	YES	1µF
LT1140	5	3	+5V, ±12V	YES*	YES	N/A
LT1141	3	5	+5V, ±12V	YES*	YES	N/A
LT1180	**2**	**2**	**+5V**	**YES***	**YES**	**0.1µF**
LT1181	**2**	**2**	**+5V**	**NO**	**YES**	**0.1µF**

*RS232 3 state outputs.

Linear's 1180/81 product using 0.1µF Caps and RS232 family:

- Save board space
- Save Cap costs
- Guarantee no latchup
- Sustain ±25V faults without disrupting supplies
- Consume power comparable to CMOS
- 1µA supply current in shutdown
- Up to 100k baud
- Start at $2.95 in 100 piece quantities

For a copy of our RS232 handbook, contact Linear Technology, 1630 McCarthy Blvd., Milpitas, CA 95035. Or Call **800-637-5545.**

LINEAR TECHNOLOGY

TOUGH PRODUCTS
FOR TOUGH APPLICATIONS.

CIRCLE 43