SIMULATOR UNTIES NETWORK DESIGN KNOT

GAAS SYMPOSIUM EYES ADVANCES

ELECTRONIC DESIGN

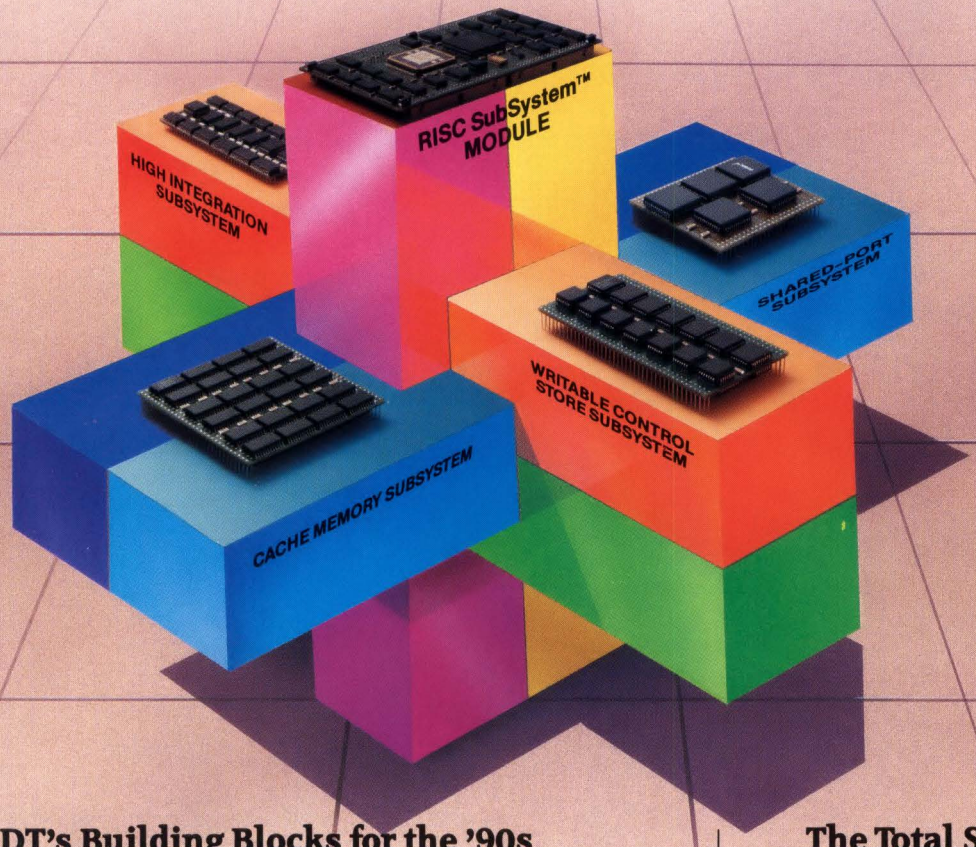
A PENTON PUBLICATION U.S. $5.00

OCTOBER 12, 1989

ISDN REACHES OUT WITH ONE-CHIP U-INTERFACE

SPECIAL REPORT: CASE STUDIES OF ASIC SOLUTIONS

The Ultimate Building Blocks



IDT's Building Blocks for the '90s

IDT is devoted to solving tomorrow's puzzles today. We recognize that our industry is changing rapidly and that future designs will require complex integrated functions using less board space. That's why IDT developed the Building Blocks for the '90s—subsystems to maximize functionality and performance while minimizing board space.

We've Figured it Out

We figure that you'll want subsystems for more than one application. IDT currently offers subsytems for cache and shared-port memories, writable control store, RISC CPU, and high-integration func-tions. But no one solution will completely solve every problem, so we will help you solve specific design dilemmas with custom subsystem designs. We can figure prominently in your design solutions—and we have the track record to prove it!

Putting It All Together

IDT's strategic mix of component products allows us to easily put all the pieces together. We draw from our extensive line of individual products and create custom components for our subsystems. We make sure that what you want in a subsystem is what you get.

Solving the Puzzle

And there's more! We do all the design, manufacture, testing, and burn-in on our subsystems. We guarantee our subsystems—all you have to do is plug them in. And we offer immediate availability for standard subsystems and deliver custom solutions in as fast as 6 weeks! At IDT, we believe in offering a total solution, not just pieces of the puzzle.

The Total Solution

Call our Marketing Hotline at **(408) 492-8551, Dept. UBB90** today for technical information. Or call (408) 492-8225 for a copy of our Subsystems Short-Form Catalog, Custom Subsystems Information Packet, and 1989 Data Book Supplement with details about all our subsystems, including RISC.

IDT, Corporate Marketing,
2975 Stender Way, Santa Clara, CA
95052-8015, FAX 408-492-8674.

When cost-effective performance counts

Integrated
Device Technology

CIRCLE 96

No two alike.

While HP's high-performance plastic optocouplers may all look alike, the similarity is only skin deep.

Because with five complete lines of plastic devices, there's clearly more to our optocouplers than meets the eye.

Like a wide variety of single- and dual-channel devices that provide you with an equally wide range of performance options.

Such as an innovative dual-channel design that combines a photon-emitting diode with a high-speed photon detector to produce data rates up to 40 MBd.

You also get high-output gain from low-input current or high-speed logic gates. Wide Vcc from 4.5 to 20 volts. And a unique AC/DC interface.

Plus they're compatible with TTL, STTL, LSTTL and, in many cases, CMOS logic families.

All of which makes HP's optocouplers the ideal solution for problems caused by ground loops and induced common mode noise.

Best of all, they're from HP. So you're assured of our commitment to excellence in service, support and reliability.

Which, come to think of it, is the one thing that makes all our optocouplers exactly alike.

To find out more about HP's optocouplers, call **1-800-752-0900, ext. 644G.** And see why looks aren't everything.

There is a better way.

HEWLETT PACKARD

CG08907

CIRCLE 97

Extraor demand

NCR

Your latest brain child can't be just another PC or peripheral.

You've got to have the edge in performance.

But you can't let costs run wild.

You've got to get to market ASAP.

But you can't compromise quality.

At NCR, we understand your problems. And we've got solutions: SCSI chips with the lowest overhead in the business. The first third generation intelligent SCSI host adapter. A single-chip VGA that's fully compatible with IBM and offers greater performance.

Single-chip CMOS solutions for interfacing peripheral chips to NU Bus, EISA, AT and Micro Channel.

The first 32-bit Ethernet controller.

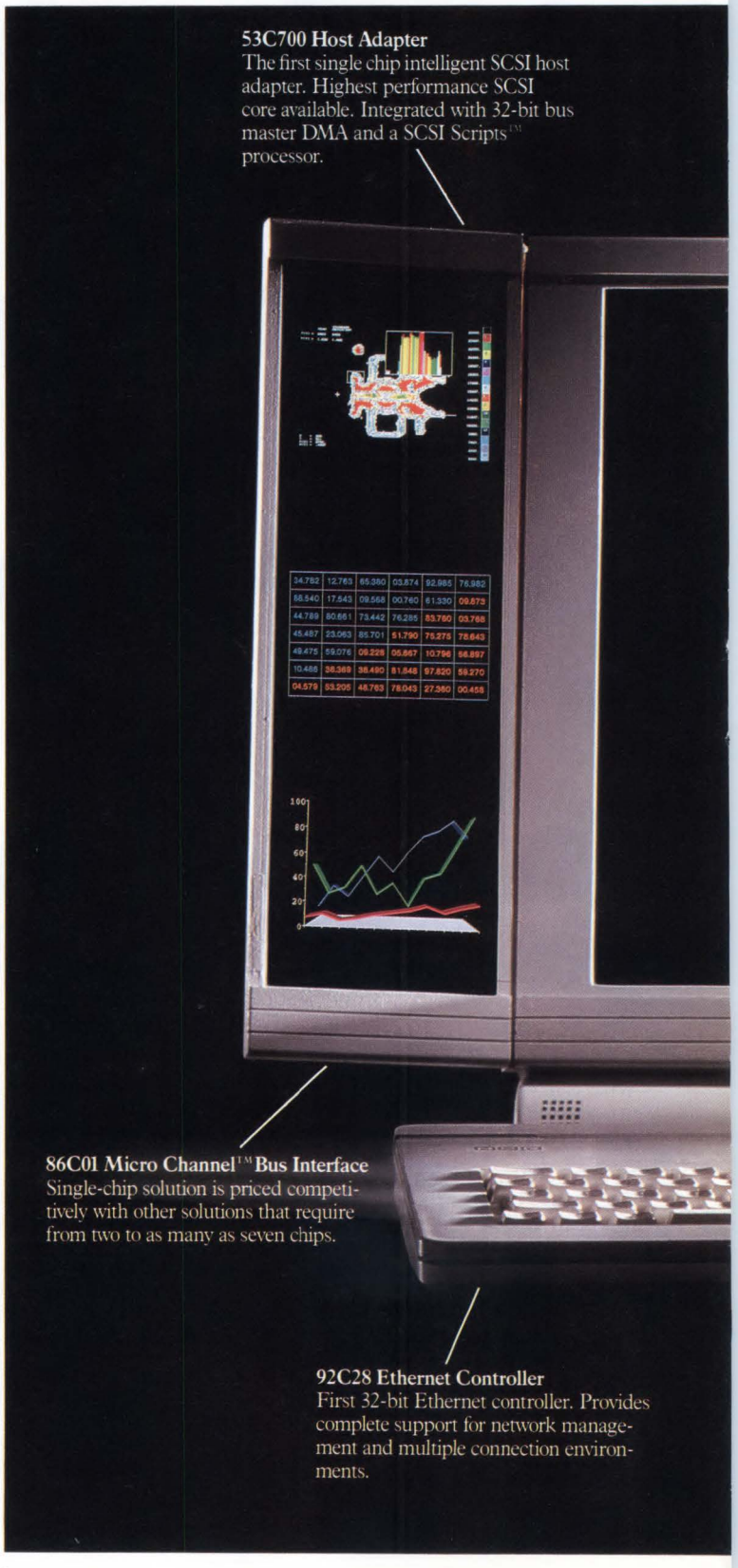
The first Ethernet twisted pair transceiver. Plus the fastest ARCnet controller/ transceiver.

And an ASIC capability with PC building blocks to give your design a competitive edge.

No wonder NCR customers enjoy some of the shortest development cycle times in the industry. And they'll attest to NCR's enviable reputation for first-pass success, responsive support, competitive pricing and on-time delivery.

If you're building extraordinary PCs, or plugging products into them, shouldn't you be talking to an extraordinary semiconductor manufacturer? For data sheets and complete information, call the NCR Hotline: 1-800-334-5454.

Creating value

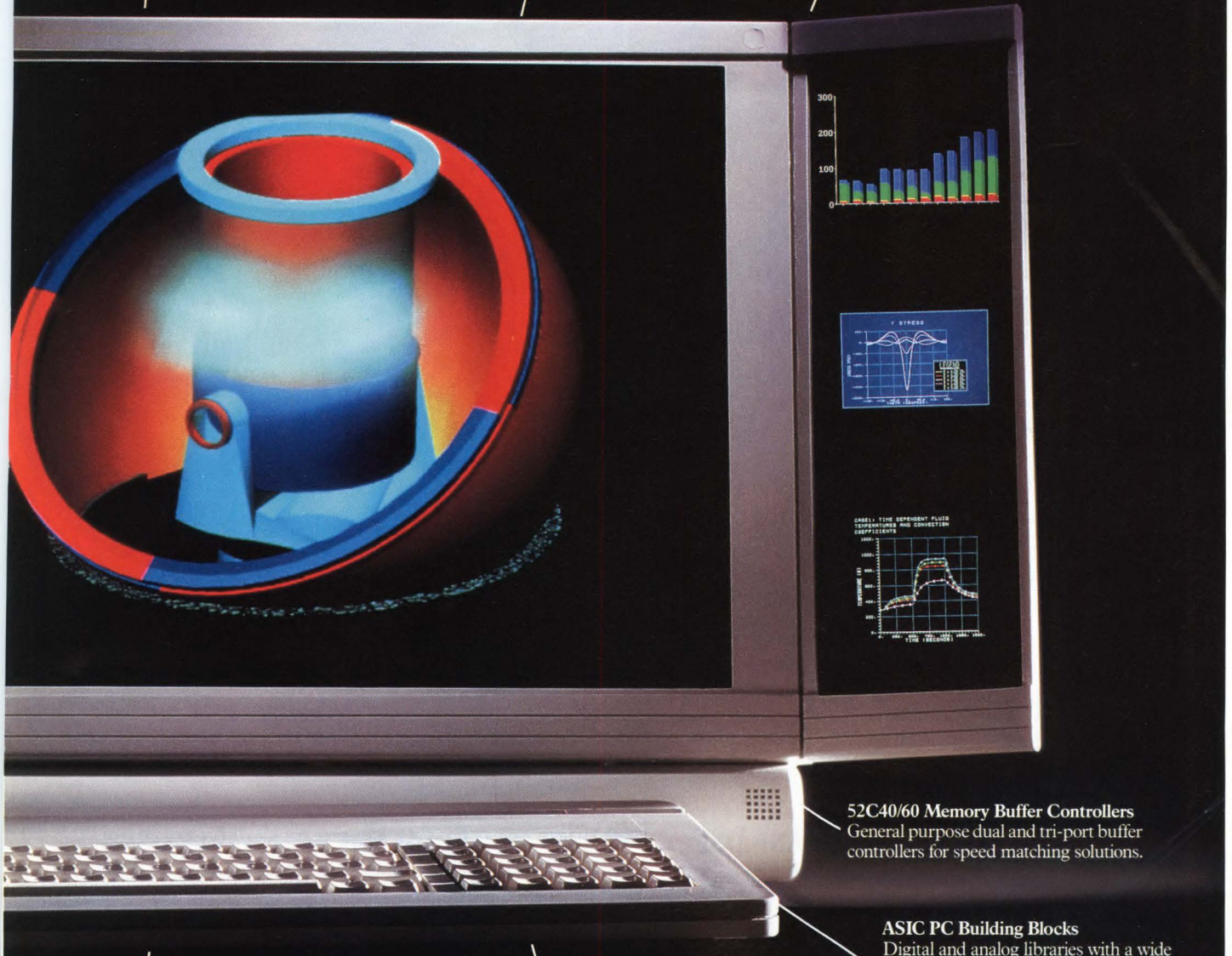


dinary PC systems extraordinary chips.

53C400 SCSI Host Adapter
Offers a higher level of integration and greater versatility than competitive solutions.

53C90 Advanced SCSI Controller
Typically completes sequences in 2% of the time needed by competitive chips. 53C94/95 offer separate 16-bit data path.

77C20 VGA Display Controller
Fully compatible with IBM VGA controller at both register and gate levels. Add 77C171 Pallette DAC for a complete VGA display adapter solution. CGMA for CGA, MDA, HCA.



52C40/60 Memory Buffer Controllers
General purpose dual and tri-port buffer controllers for speed matching solutions.

ASIC PC Building Blocks
Digital and analog libraries with a wide variety of cells, including MPU cores, 8200 peripherals, D to A and A to D converters, sound generators, counter/timers, multipliers, floppy disk controller, digital data separator, ISA Bus interface and integrated bus drivers. Plus KE^2, NCR's knowledge-based Engineering Environment.

92C02 Twisted Pair Transceiver
First Ethernet twisted pair transceiver. Implements current IEEE 802.3 10 BASE-T draft standard.

90C98A ARCnet Controller/Transceiver
Highest performance single-chip ARCnet LAN controller/transceiver. Includes buffer chaining and reduced wait states. Backward software compatible to the 90C26.

CIRCLE 92

OCTOBER 12, 1989 VOL. 37, NO. 21

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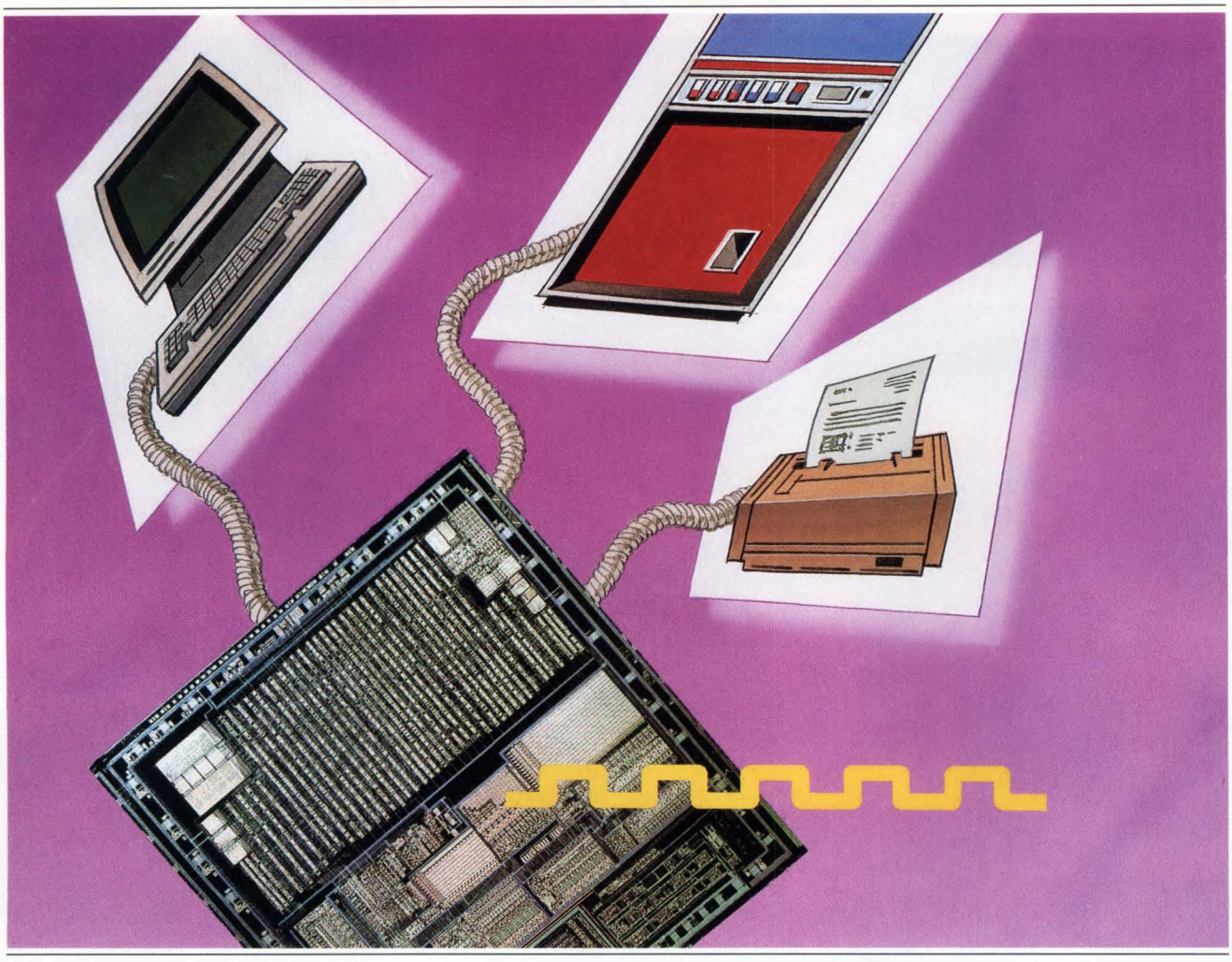

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

Cover illustration by Bob Moyer
Board photo courtesy of Siemens Corp.

COMING NEXT ISSUE
- Special Report: Optical disk drives
- Wafer-scale integration arrives in disk form
- Product Report: Rf signal generators
- Building a Multibus II single-board computer

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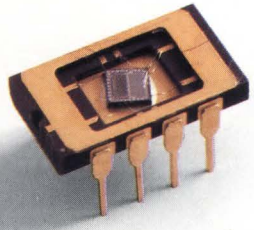
Your perceptions of power ICs are about to be shattered...

CIRCLE 91

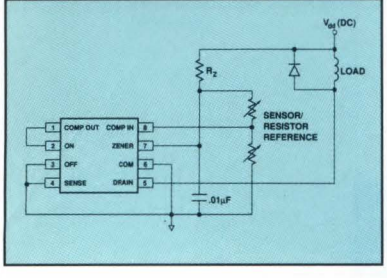


400 Volt

The times, they are a' changin'—Power Integrations

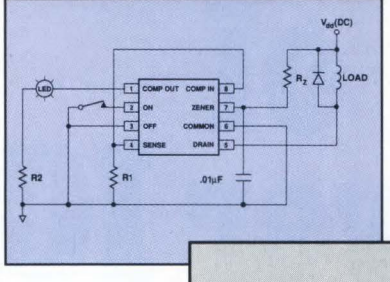
Simple to use.

Analog sensor application



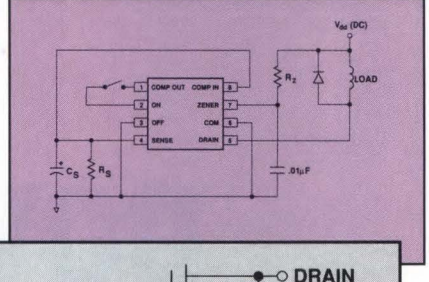
Adds more value.

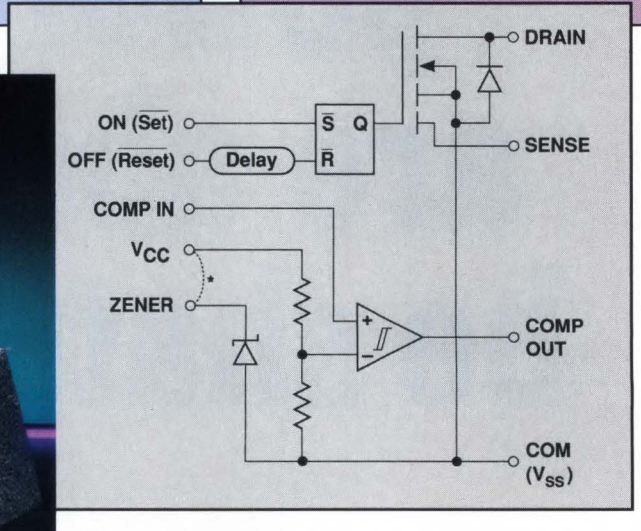
LED can indicate current thru load



More versatile.

Simple pulse width modulation





The PWR-DRV1 Universal Power Driver is an easy-to-implement, cost-effective interface between control electronics and high voltage loads such as displays, relays and solenoids.

- 200V, 300V, 400V versions
- 350mA
- $R_{DS(ON)}$ 5Ω

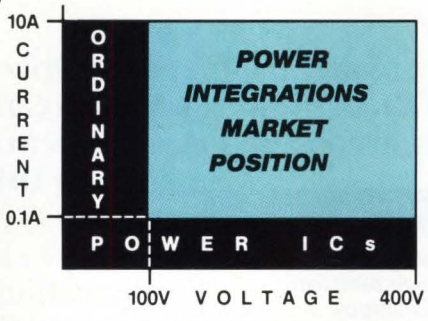
- Operates from rectified AC or DC power source
- Controlled by analog sensors, mechanical switches and digital logic (TTL or CMOS)
- On-board low voltage power for control circuitry
- Variable output (operates low voltage loads from high voltage, reduces power consumed by a load)
- Controls an AC load from a DC power source
- Measures current without external voltage drops

Rock'n Roll!

bridges the gap between high and low voltage.

Remember the first time you heard Elvis, Dylan, the Stones or the Beatles? You were experiencing something different. And you knew your life would never be the same. Well, Power Integrations is about to do it to you again!

Not musically. But professionally. And profoundly. With a brand new **CMOS Power IC** technology that's easy to implement in both electronic and electro-mechanical designs.



Our new family of 200V, 300V and 400V enabling ICs will have you "rocking around the clock" developing new products. And rolling over the competition with your new-found ability to interface directly with solid state.

Now you can control almost anything! From automatic pumps to the fully electronic home. Upgrade or customize your current system. Or innovate— demonstrating your engineering genius and creativity.

The enabling functions of our ICs generate added system value far beyond the price of the parts they replace. And they interface with 5V logic. Easily. Reducing the risk of product failure and enhancing your reputation as an innovative, yet reliable designer.

Imagine what you can do with a...

Universal Power Driver (PWR-DRV1) that provides all necessary interface between electro-mechanical loads and electronic circuits. And produces variable output. Or a...

Dual Relay/ Solenoid Driver (PWR-DRV2) that saves board space and prevents simultaneous "on" states. Or an...

Isolated Relay/Solenoid Driver (PWR-ISO1) that alleviates potential system failure by isolating control logic up to 1500V. Or a...

Dual Level Power Driver (PWR-DRV3) that allows quick actuation and then reduced power. Or...

High-Voltage Peripheral Drivers (PWR-DRV451/2/3/4), that interconnect digital logic to the AC line. And are pin-compatible with 75451s and 3611s. Or an...

8-Channel MOSFET Array (PWR-NCH801) a single chip that provides more power in less space. Eight high voltage channels controlled directly from digital logic signals.

We've provided the intro with our enabling ICs. And created the bridge between low and high voltage. Now it's time to rock 'n roll!

We're Power Integrations— bringing you the power to control. Our lines are open and we're taking requests. So pick up the phone and call for samples and more information. Or lay down some hot application licks on your PC and FAX them to our application support team.

Phone: 1-800-552-3155
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POWER INTEGRATIONS, INC.

The Power to Control

411 Clyde Avenue
Mountain View, CA 94043

CIRCLE 89

And the beat goes on...

Win an Epson portable Computer! Or a Casio Digital Diary! Or a Sony Watchman TV!

Now that you've read about the Power Driver 1. (See the previous three pages.) How about showing what you can do with it? Power Integrations, in cooperation with *Electronic Design*, is sponsoring a **Power Driver 1 Design Contest.**

Design Contest Prizes	
1st Prize:	Epson Equity portable computer with 20MB hard drive and 3.5" floppy.
2nd Prize:	A Casio 32K Digital Diary that stores up to 1500 names and phone numbers.
3rd thru 5th Prizes:	A Sony Watch Man TV
6th thru 10th Prizes:	Autographed copies of *Marketing High Technology, An Insider's View* by Bill Davidow

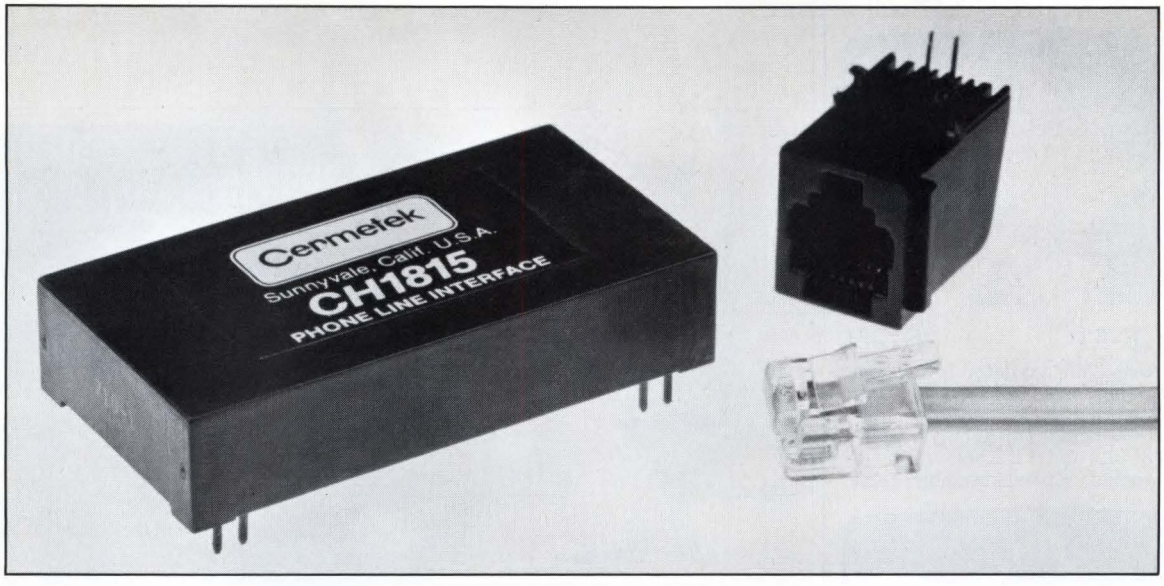
This is your chance to be innovative. We're looking for the most clever application of the PWR-DRV 1 Universal Driver.

Judging. Power Integrations will pick the ten best PWR-DRV 1 design applications and submit them to the editorial staff of *Electronic Design* for final judging. The top five entries will be announced in one of the March issues of this publication.

How to enter: Just call Power Integrations at 1-800-552-3155 for an entry form and free PWR-DRV 1 samples. Or write to us at 411 Clyde Avenue, Mountain View, CA 94043.

POWER INTEGRATIONS, INC.

The Power to Control



SELECTING A MODEM CHIP SET IS ONLY PART OF THE SOLUTION.

When considering a modem design, selecting the proper modem chip set is only part of the solution. You must consider the type of telephone interface used, what method of error control and agency approval needed, either domestic or international. Determining these factors is time consuming, costly and complex. The solution? Cermetek!

Our family of modem components allows the design engineer to surround a modem chip set, making it a complete modem, quickly and economically.

So when you need part of a solution, or the whole modem solution, Cermetek has the expertise and the right answers for you. Find out how Cermetek can enhance your existing or future modem design. Call Cermetek today for more information or write us at:

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MODEM COMPONENTS

189X Data Module Features

X.25 LapB, MNP Class 4 and 5, error correcting and data compression, autobaud speed conversion, flow control, RS-232 interface, AT compatible command format driven—1890,1891,1892.

MNP is a registered trademark of Microcom, Inc.

18XX DAA's Features

Telephone interface, Data Access Arrangement (DAA)—pre-approved domestic / international, voice data switch, 2- to 4-wire converter, surge protection, isolation, dialing feature, low cost and small size. 1810,1811,1812A, 1813, 1814, 1818, 1828.

RESTORE THE IRA DEDUCTIONS

There's a lot of talk lately about getting the federal government involved in helping the U.S. electronics industry. Many industry leaders have journeyed to Washington, D.C., to talk with members of the legislative and executive branches of government, attempting to sensitize them to our industry's problems. They have presented cases that highlight the benefits of Sematech and U.S. Memories, the need for a coordinated HDTV effort, as well as the continuing difficulties of opening up the Japanese market. In general, we applaud such efforts because the electronics industry will play a major part in assuring our nation's well-being in the years leading up to the turn of the century.

However, while industry representatives are in Washington, why not put in a good word for the people who make the industry go—the rank-and-file engineers? They should point out the importance of restoring tax deductions for individual retirement accounts. The time is right to do this because Congress is considering changing the tax laws, and many of these changes are aimed at helping industry compete with foreign companies.

Because of the industry's nature, few engineers stay with a company long enough to build up pension benefits. If a career lasts 40 years, think of the changes that have occurred and will occur in the industry over that time span.

Rapid changes in technology create a constantly changing job picture as some companies ride the crest of a new technology while others try to maintain their market lead based on older technologies. No one is safe from these changes. Consider the engineers who accepted what they thought was solid job assurance offered by such long-time electronics industry stalwarts as General Electric and RCA—both companies have been in and out of the computer and commercial semiconductor businesses.

The IRA deduction is a bread-and-butter issue for engineers. While we're asking the government to help our industry in its competitive wars, let's also do what is right and fair for the people bearing the brunt of the effects of those wars—the design engineers.

Stephen E. Scrupski
Editor-in-Chief

99¢ from

dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	•MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

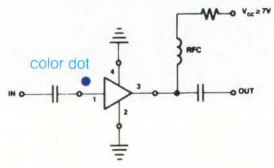
NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

Unbelievable, until now…tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers only $59.95



Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 220, 470, 680, 1000 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047. .068, .1μf

† Minimum Order 50 per Value

☐ Designers kit, KCAP-1, 50 pieces of each capacitor value, only $99.95

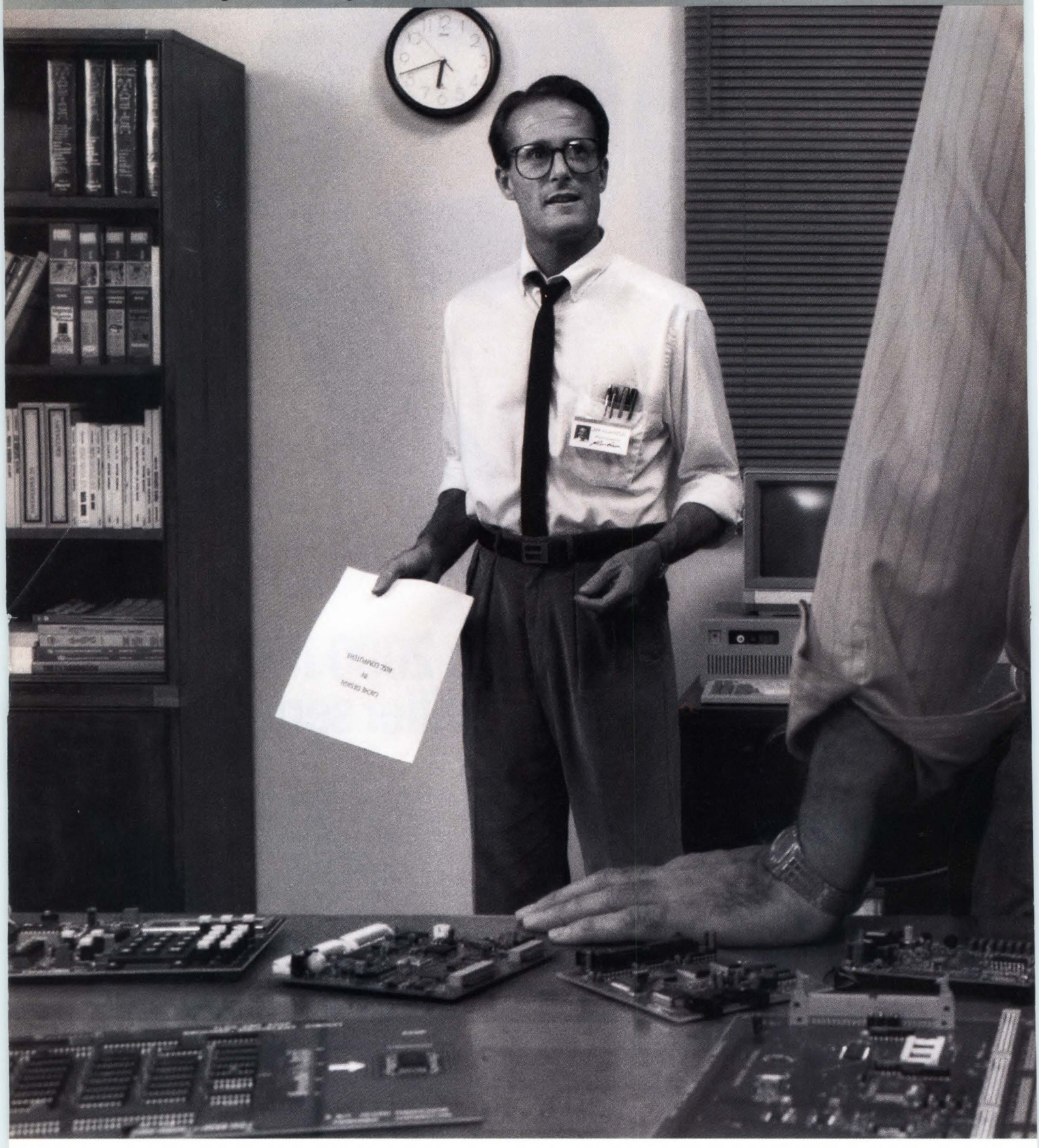
finding new ways...
setting higher standards

Mini-Circuits
A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

CIRCLE 99

C113-Rev. D

"What if I told you there's a 15ns 64K SRAM available



now?"

"I'd say you've been reading too many supermarket tabloids."

"Seriously! You get high speed and quantity delivery, plus the ability to drastically cut your qual costs!"

"OK, I'll bite. Who's got 'em?"

"Toshiba."

"Why didn't you just say that in the first place?"

While others continue to talk speed, Toshiba now delivers 15ns Static RAMs.

The exceptional access speed of the new 15ns 64K SRAM family is the result of a little technological wizardry and lots of 1.0μ CMOS know-how. The bottom line is a 15ns 64K SRAM that dissipates less power and requires a smaller-sized die than more costly BiCMOS devices.

And, if you've been looking for ways to cut qualification costs on your 64K SRAMs, look no further than Toshiba's 64K SRAM family. By using an aluminum master slice common to all configurations within the 64K family, the cost of qualifying individual parts is reduced by as much as 75%!

Toshiba builds a full line of SRAMs that offer high speed and fully static operation. A line whose depth and breadth provides higher system performance and lower system costs when designing high-speed cache memories, high-speed main memories, high-speed buffers and writeable control stores for minis, superminis, workstations, RISC-based systems, real-time processors, high-speed storage and high-end graphics applications.

When it comes to SRAMs, Toshiba's got all the speeds, configurations and densities you need. Including 256K, coming soon.

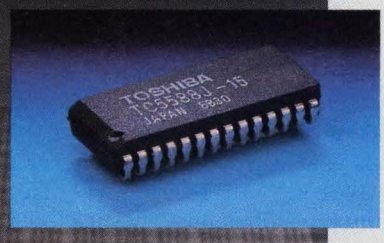
Toshiba High-Speed SRAMs

Configuration	Density	Speed (ns)				Availability
64K x 1	64K	35	45	55		Now
16K x 4	64K	15	20	25	35	Now
16K x 4 (OE)	64K	15	20	25	35	Now
8K x 8	64K	15	20	25		Now
8K x 9	72K	15	20	25		Now
64K x 4	256K	20	25	35		Early '89
64K x 4 (OE)	256K	20	25	35		Early '89
32K x 8	256K	20	25	35		Early '89
32K x 9	288K	20	25	35		Early '89
16K x 12	192K module	25	35			Now
16K x 16	256K module	25	35			Now

And plenty of packaging options, too. From JEDEC standard Skinny DIPs and SOJs to ZIP Modules.

Not to mention the kind of service and deliverability others can only talk about.

Call today for complete data sheets and applications notes at 1-800-888-0848 ext. 517.



In Touch with Tomorrow

TOSHIBA

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CIRCLE 93

MST-88-012

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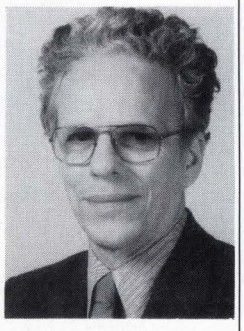
POWER GRID FACES NEGATIVE-Ω LOAD



FRANK GOODENOUGH
ANALOG & POWER EDITOR

Over the next 10 to 15 years, more than half of the load placed on the electric power grid will be switch-mode power supplies (SMPS). In addition to their ubiquitous use in our industry, they will appear in applications that range from fluorescent lights to washing-machine motors. To the power line, switchers look like a negative resistance. As the line voltage drops, they draw more current from the line. "Brown-out" techniques to cut the load won't work.

Exacerbating this problem, the power factor of a typical off-line power supply (rectifiers driving a capacitor input filter) is 0.6 to 0.7. This means that if you need 1 kW, the line must supply up to 1.6 kW. Unlike in the past, when large ac motors drew sinusoidal currents out of phase with the voltage, the electronic load draws in-phase pulses of current during the short time (about 1/8 of a cycle) that the rectifiers are forward-biased and charging the filter capacitor (see ELECTRONIC DESIGN, Nov. 28, 1988, p. 135.).

In the U.S., Underwriters Laboratories allows for 12 A from a typical line hosting a 15-A, 120-V ac circuit breaker. At a low line voltage of 90 V, the circuit will supply a resistive load with 1.08 kW of power. However, if the power factor is 0.65, the maximum available power drops to 700 W, which is less than what is needed by a growing number of workstations.

On one hand, look at a typical small office that has just added several "super clone" PCs with 80386 processors, VGA graphics, 120-Mbyte hard disks, and connected printers. Each desk will need 300 to 400 W. These can't all be put on the same line.

A large office building, on the other hand, may have several thousand PC loads, plus copiers, fax machines, and even telephones. Already, line-power considerations are affecting designers of buildings, as well as building codes. At a minimum, #12 AWG wire must replace #14. But already in these buildings, high-current pulses have appeared in the neutral wire of the buildings' three-phase systems—where no currents should appear at all—heating the wire and creating potential danger.

The problem is becoming critical. A Power Quality Conference, which is being held next week in Long Beach, Calif., (Oct. 16–20) aboard the Queen Mary, will bring power-utility people together with power-supply designers and users. Tight power-factor correction was already legislated in Europe—and it will get tighter (IEC Standard 555.2).

Don't despair. The problem becomes the solution: A handful of controller ICs are arriving to build switch-mode, power-factor correcting preregulators. They connect between the rectifier's output and a final switching regulator. While different in detail, each controller senses the line voltage and forces the current to a sinusoidal shape.

The first such chip, Siemens TDA 4814, has been in volume production since 1986. Though aimed at electronic ballasts for fluorescent lamps, it adapts to SMPS (see ELECTRONIC DESIGN, Oct. 27, 1988, p. 115). In addition, an IC just for SMPS is on the way. The first device aimed at supplies, the ML4812, came from Micro Linear earlier this year. Up coming are Cherry's CS3810, Silicon General's SG3561, and Unitrode's UC1854—each will offer supply designers a different mix of architecture, performance, features, and cost.

While adding to the cost of a supply, power-factor correction also eliminates the need for a 115/220-V ac switch. Furthermore, the design is simplified and stress is reduced on the output SMPS parts. In addition, the preregulator's output becomes a natural source for a high-voltage distributed power bus, where step-down dc-to-dc converters may be needed.

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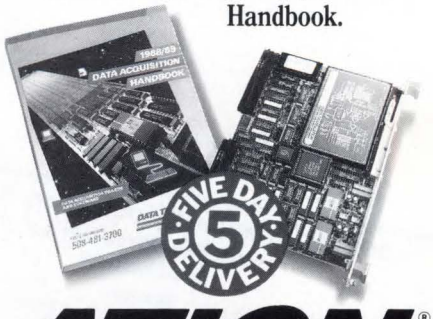
DT1492	16SE/8DI	12	1, 2, 4, 8	40	2	130/DAC	16	$2525
DT1492-F	16SE	12	1, 2, 4, 8	150	2	130/DAC	16	3075
DT1492-F	8DI	12	1, 2, 4, 8	150	2	130/DAC	16	3075
DT1492-G	16SE	12	1, 2, 4, 8	250	2	130/DAC	16	3515
DT1492-G	8DI	12	1, 2, 4, 8	250	2	130/DAC	16	3515
DT1492-L	4DI	12	1	750	2	130/DAC	16	4175
DT1495	16SE/8DI	12	1, 10, 100, 500	40/2.5	2	130/DAC	16	2525
DT1497	4DI	16	1	100	2	130/DAC	16	3515
DT1498	4SE(SS&H)	12	1	100	2	130/DAC	16	3075



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CIRCLE 95

Guess who's first in CAD/CAM/CAE and fastest growing in workstation sales?

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The first name you probably thought of is not the first. Intergraph is #1 in CAD/CAM/CAE in North America. Also, we're the world's 4th largest and the fastest growing workstation company.

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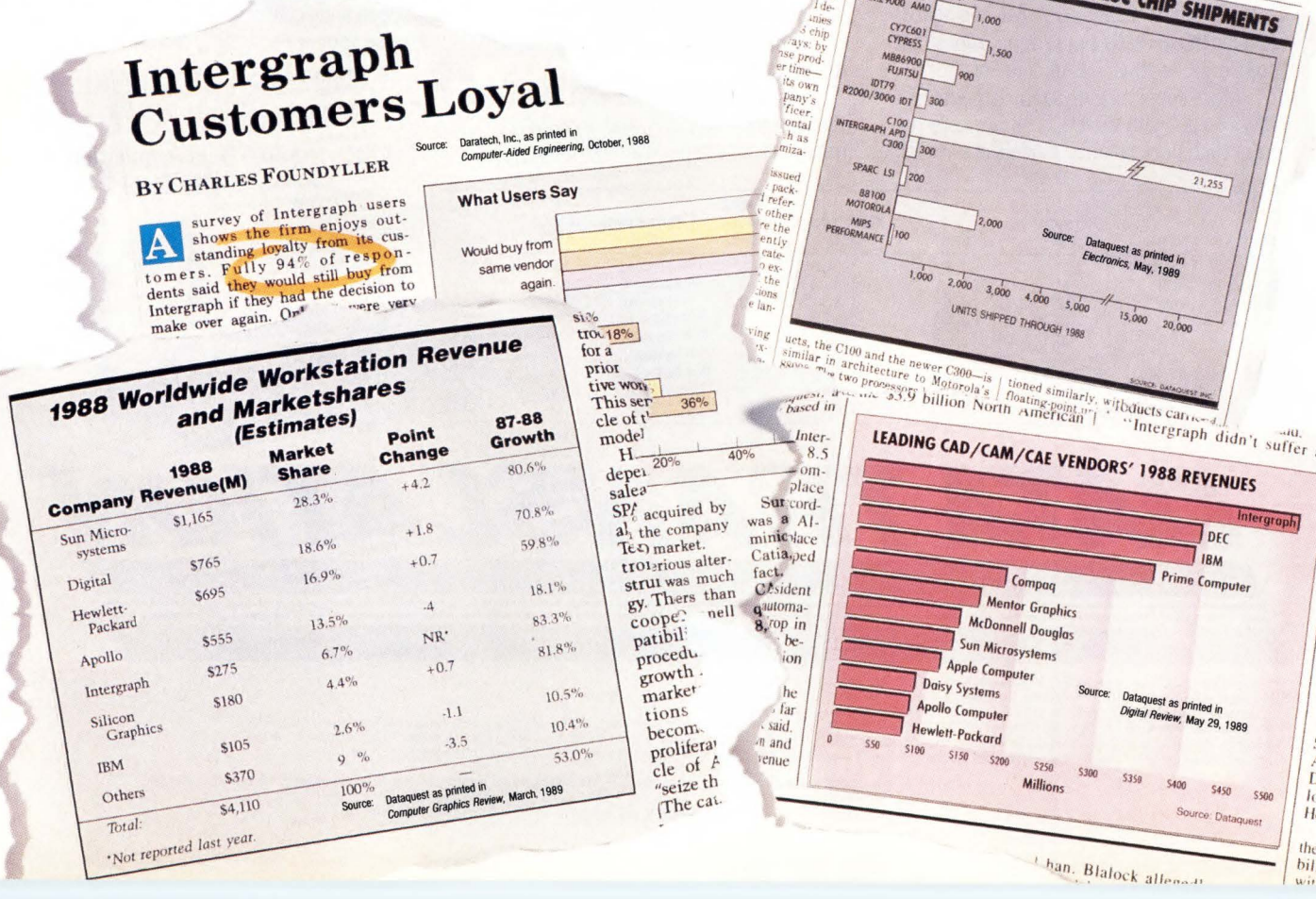

Intergraph Customers Loyal

BY CHARLES FOUNDYLLER

A survey of Intergraph users shows the firm enjoys outstanding loyalty from its customers. Fully 94% of respondents said they would still buy from Intergraph if they had the decision to make over again. On[illegible]ere very

Source: Daratech, Inc., as printed in Computer-Aided Engineering, October, 1988

What Users Say

Would buy from same vendor again

18%

for a prior

This ser[illegible] 36%

cle of t[illegible] model

H[illegible] 20% 40%

depe[illegible] sale

SP[illegible] acquired by al[illegible] the company Tek[illegible] market. tro[illegible]erious alter- stru[illegible] was much gy. Thers than coope[illegible] nell patibil[illegible] procedu[illegible] growth . market tions becom[illegible] prolifera[illegible] cle of A "seize th (The cat[illegible]

1988 Worldwide Workstation Revenue and Marketshares (Estimates)

Company	1988 Revenue(M)	Market Share	Point Change	87-88 Growth
Sun Microsystems	$1,165	28.3%	+4.2	80.6%
Digital	$765	18.6%	+1.8	70.8%
Hewlett-Packard	$695	16.9%	+0.7	59.8%
Apollo	$555	13.5%	-4	18.1%
Intergraph	$275	6.7%	NR*	83.3%
Silicon Graphics	$180	4.4%	+0.7	81.8%
IBM	$105	2.6%	-1.1	10.5%
Others	$370	9 %	-3.5	10.4%
Total:	$4,110	100%	—	53.0%

*Not reported last year.

Source: Dataquest as printed in Computer Graphics Review, March, 1989

WHO'S IN FRONT: 32-BIT RISC CHIP SHIPMENTS

Source: Dataquest as printed in Electronics, May, 1989

LEADING CAD/CAM/CAE VENDORS' 1988 REVENUES

Source: Dataquest as printed in Digital Review, May 29, 1989

Source: Dataquest

COLOR SCANNER BEATS DRUM-AND-LASER WAY

By mounting a scanning-photodiode imaging array on a piezoelectric crystal, Array Technologies Inc., Oakland, Calif., has developed an innovative way to move that array in rapid and precise submicron increments. By microstepping the array with the piezo crystal, the company was able to build a full-color image scanner, the AS-1, that will sell for about $20,000—a fraction of the cost of professional-quality drum and laser scanners. The precise placement of the imaging array assures exact spatial registration and, therefore, repeatable scans. Adding a special photodiode sensor alongside the photodiode array also gives the scanner a dynamic range of up to 12 bits per color channel. The sensor is held still at a precise location and repeated microstep scans are accumulated and averaged to obtain the full dynamic range. In contrast, other scanners must typically make three passes over the source material to capture the red, green, and blue data. As a result, they introduce small mechanical inaccuracies that smear the image and color data. Images up to 4096 pixels by 4096 lines can be generated under the control of a TMS34010 graphics processor from Texas Instruments. In addition, up to three AT&T WE-32 DSP chips offer such functions as edge enhancement and various color controls. The system was introduced last month at the Seybold Desktop Publishing Conference in San Francisco. DB

CUSTOM SPARC CPU TO CUT WORKSTATION COST, SIZE

A customized Sparc RISC processor, designed jointly by Solbourne Computer, Longmont, Colo., and Matsushita Electric Industrial Co. Ltd., Osaka, Japan, promises to yield a one-million-transistor chip that reduces workstation complexity. The 15-by-15-mm chip has 32-bit integer and 64-bit floating-point subprocessors, a memory-management unit, and separate instruction and data caches. Fabrication plans call for a submicron CMOS process that would push the chip to 40 MHz and let it execute 20 to 25 MIPS and up to 20 MFLOPS. Each cache has its own translation look-aside buffer to minimize cache access time. To operate multiple CPUs in a system, the 280-pin processor includes circuits for multiprocessor systems. In describing the chip at last month's Microprocessor Forum in San Jose, Calif., Solbourne said that it plans to put it in a family of relatively low-cost workstations set to appear by mid 1990. Matsushita is also looking at products for the chip, but neither company intends to sell it separately. DB

FAST PLOTTER CUTS COST OF HIGH RESOLUTION

With 300-point-per-inch resolution, the CADmate wide-format electrostatic printer delivers near-laser-quality monochrome plots at a cost that competes with the slower pen plotters. To get the plotter's cost under $14,000, Versatec, Santa Clara, Calif., traded off the machine's intelligence by shifting some computational burden to the host system—a personal computer or workstation CPU. As a result, the plotter doesn't a have rasterizing engine. Instead, it comes with rasterizing software and a simple high-speed parallel interface card that plugs into a desktop system, such as an 80386-based PC. The system prints the image up to six times faster than a pen plotter, moving the paper at 0.65 in./s. That rate produces an E-size (34-by-44-in.) drawing in less than 30 seconds. The rasterizing software accepts Hewlett-Packard GL and Autocad ADI files. DB

OBJECT MANAGEMENT GROUP GAINS ELEVEN MEMBERS

Eleven new members, including board members AT&T and Netwise, have joined the ranks of the Object Management Group (OMG), an international organization devoted to making different vendors' computer systems and software work and communicate together with increased efficiency. The newcomers, which also include the AION Corp., Borland International, Coordination Technology, Eastman Kodak, Objectivity, Ontologic, Softron, Unify Corp., and the University of California, bring the organization's total membership to 29. On another front, the group formed the OMG Technology Committee, which aims to influence the future direction and standardization of core object-oriented products and technologies. BM

SILICON SYSTEMS, PHILIPS SHAKE ON DISK-DRIVE ICS

A long-term agreement between Silicon Systems, Tustin, Calif., and Philips Components-Signetics, Sunnyvale, Calif. will culminate in technology and product exchanges centering around HS-3, which is Philips' 8-GHz oxide-isolated bipolar process. The process will make various products, including standard and custom microperipheral ICs for disk drives. The two companies will offer alternate sources for identical products. Under the agreement, Silicon Systems will transfer databases and test data on several existing and newly defined products to Philips Components-Signetics. Philips, in turn, will transfer the HS-3 process to Silicon Systems for its internal manufacturing. DM

First Wraps Come Off IBM's Latest RISC Chip

With IBM Corp., Austin, Texas, set to release its second-generation reduced-instruction-set computer (RISC) workstation, some details of the RISC CPU chip that drives the system were unveiled last month at the Microprocessor Forum in San Jose, Calif. First, the chip will be created with IBM's 1-μm CMOS process, which the company also uses to build its 1- and 4-Mbit dynamic RAMs. IBM designers achieved considerable instruction overlap for integer, branch, and floating-point operations so that the chip has an effective efficiency of less than one cycle per instruction. In addition, the processor will contain separate instruction and data caches, hardware features to assist database operations, and a high-speed floating-point unit. On-chip, 32-bit integer and 64-bit floating-point units execute each of their instructions in one clock cycle. Wide internal and external buses make it possible for one-cycle operand transfers. Also, with a 64- or 128-bit memory interface, two or four words can be loaded in one cycle. To ensure data integrity, the processor checks parity on external buses and internal blocks. DB

Workstation Accelerator Offers Twin RISC Chips

A forthcoming accelerator board for Sun workstations and other VME-based platforms is the first to combine Intel's i860 and i960 RISC microprocessors on one board. Within the board, the i860 is dedicated to integer, floating-point, and graphics computations, while the i960 handles the I/O and boot functions and system diagnostics. This combination propels the workstation to near-supercomputer performance: 40 MIPS and 80 MFLOPS. The board, from Sky Computers, Chelmsford, Mass., is scheduled for release early next month. By merging the microprocessors with a DMA engine and optimized C and Fortran compilers, the board will let workstations run applications, like simulation, modeling, finite-element analysis, and fluid dynamics, that previously required a supercomputer. RN

Multichip Modules Really Pack In The Gates

A multichip modular packaging scheme developed by Digital Equipment Corp.'s research center, Cupertino, Calif., holds from 100,000 to over 1 million gates. The modules increase system density by almost 30-fold. In addition, they double system-computation speed by cutting propagation delays over the packaged-chip-on-board scheme the company uses in its VAX 8800 system. Interconnections in the modules are formed on a 6-in.-diameter metal wafer by depositing alternating layers of a polyimide dielectric and copper, and patterning the layers using well-established photolithography to obtain 15-μm-wide lines. Furthermore, DEC developed a proprietary tape-automated-bonding scheme with internal ground planes for complex ECL or CMOS ICs. With this scheme, up to 360-lead circuits can be mounted directly to the sites on the module. And each module has up to 800 I/O lines for system interconnections. The first use of the modular packaging scheme will be for high-power ECL circuits, which are intended to serve as the heart of a mainframe computer the company plans to unveil later this year. When hosting ECL chips, each module can handle up to 300 W in an air-cooled environment. To allow the module to dissipate that much power, DEC developed a heatsink that looks like an inverted pin cushion with hundreds of pins. The heatsink attaches to the bottom of the metal wafer. DB

Magnetic Imaging Shows Body's Blood Flow

A magnetic-resonance imaging technique developed by General Electric Co., Schenectady, N.Y., gives doctors a noninvasive way to measure blood flow. The technique—phase-contrast magnetic resonance (MR) angiography—produces images of blood that delineate the veins and arteries. The faster the blood flows, the brighter the vessels appear on the MR scanner's display screen. At the heart of GE's system is a superconducting magnet that can produce a 1.5-Tesla field (30,000 times the strength of the earth's magnetic field) within a 1-m-wide bore. The patient is positioned within the magnet's bore and probed with high-frequency radio signals that excite the nuclei of hydrogen atoms, causing them to resonate. The resonance signals are picked up by an antenna and transmitted to a computer that reconstructs the data into a 3D image. The key to GE's phase-contrast angiography is a flow-encoding procedure that helps distinguish between the resonance signals given off by the moving hydrogen atoms in the bloodstream and the atoms in the body's stationary organs and structures. The procedure suppresses the relatively large signals emitted by the motionless hydrogen atoms and highlights those from the hydrogen atoms moving in the blood. LG

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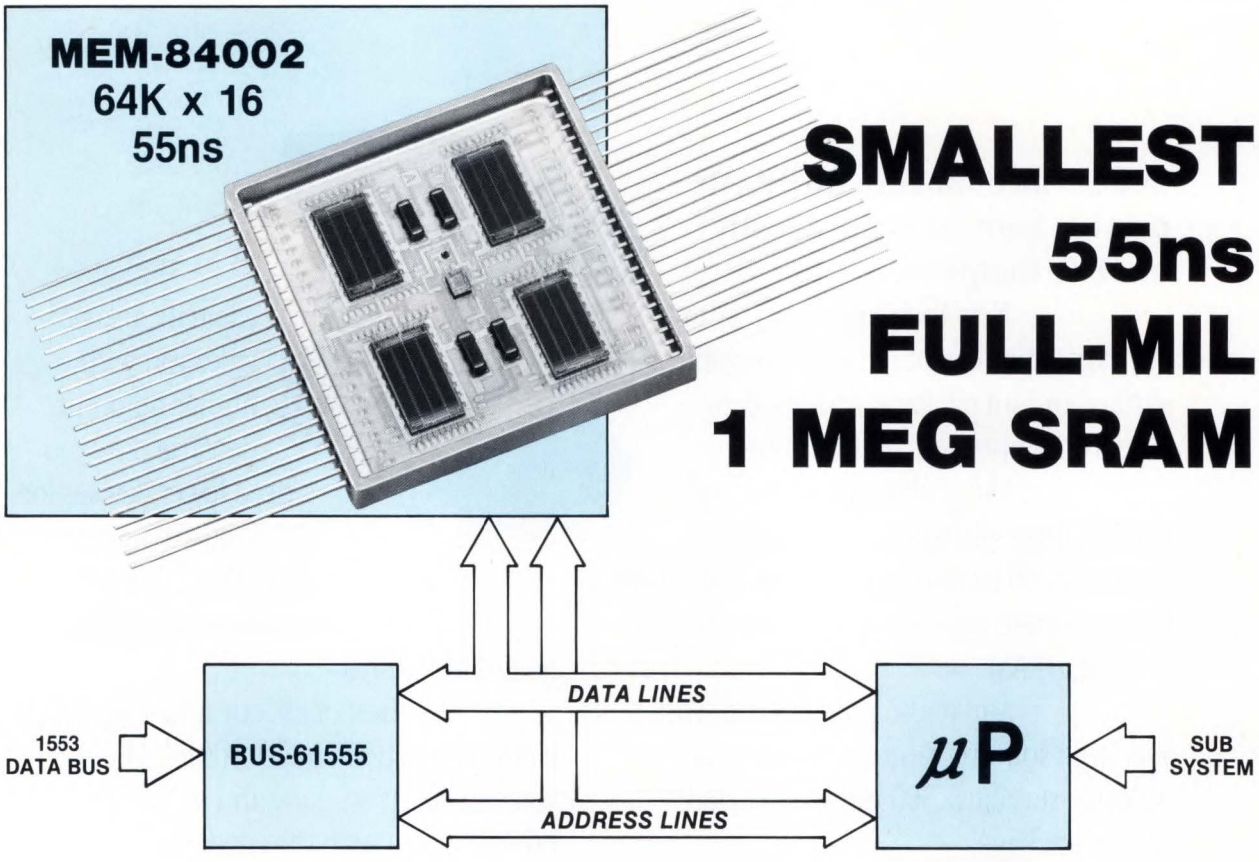
NEWS

DDC ILC DATA DEVICE CORPORATION

OCTOBER 1989

ABOUT SYNCHRO-CONVERSION • A/D & D/A CONVERSION • 1553 BUS DEVICES • POWER & CUSTOM HYBRIDS



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DIAMOND-FILM COATINGS INCH CLOSER TO BECOMING A COMMERCIAL REALITY

Diamond film, which serves as an excellent electrical insulator and thermal conductor, shows promise as a commercial entity. Process developments in diamond-film coating at the University of California at Los Angeles (UCLA) pack potential for both passive and active applications in semiconductor devices.

Other probable applications for the film are in the mechanical and optical arenas. The new process, which is called plasma-assisted physical-vapor deposition (PAPVD), offers several key advantages when compared with the chemical-vapor deposition (CVD) processes now used for diamond-film synthesis.

Developed by Prof. Rointan Bunshah, Dr. Chandra Deshpandey, and colleagues at UCLA's School of Engineering and Applied Science, the process evaporates graphite by an electron beam to form carbon vapors. These vapors are then introduced into a gas plasma containing hydrogen. The material to be coated is held in the gas plasma and the resulting reaction deposits a diamond film on the material's surface *(see the figure)*.

According to Deshpandey, earlier attempts with CVD technology to develop diamond-film coating processes for microelectronic applications were stymied by inherent problems. CVD processes require a temperature between 850 and 1000°C. Such high temperatures are incompatible with many semiconductor-device processing technologies. In contrast, the PAPVD process requires much lower temperatures—less than 350° C.

In addition, researchers using CVD have had only limited success in scaling their processes to coat wafer-sized areas. The PAPVD process has much greater potential in this respect, Deshpandey claims. Finally, diamond coatings produced with CVD processes have highly granular, faceted surfaces that render them unsuitable as substrates for semiconductor material. The coatings produced by the PAPVD process are of a uniform thickness that lends the film to microelectronic applications.

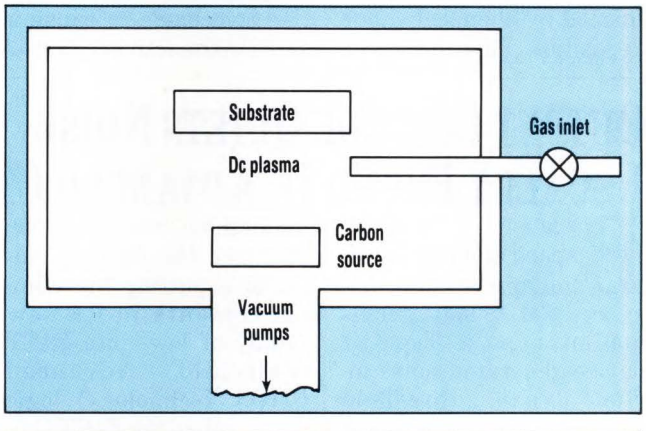
Deshpandey says that commercial applications for passive devices can be pursued immediately. The high thermal conductivity of diamond film makes it useful as a heat sink for high-power and GaAs-microwave devices. At present, the UCLA research team is working on demonstrating the processes' ability to coat large, wafer-sized areas. Once that's done, they'll begin efforts to dope the diamond film with an eye toward active-device applications. The process technology for such devices would be similar to those used for today's silicon and GaAs devices, but such applications may be years away, says Deshpandey.

Other film applications may be found in impact-protective coatings for hard disks. Diamond's inherent hardness means that a coating just 100 to 200 Å thick could protect magnetic media from the hazards of high-speed, flying read-write heads.

That same hardness, coupled with the film's smoothness and transparency, suggest a myriad of optical applications. These range from protection for infrared and UV components to scratch-resistant coatings for eyeglass lenses. Thanks to their high band gap and high resistivity, the films could also serve as radiation-protective coatings in aerospace and nuclear applications.

Finally, according to Deshpandey, Japanese researchers have had some success utilizing diamond films as coatings for high-fidelity loudspeaker diaphragms. The UCLA process, with its ability to coat large areas, certainly suits it for such applications.

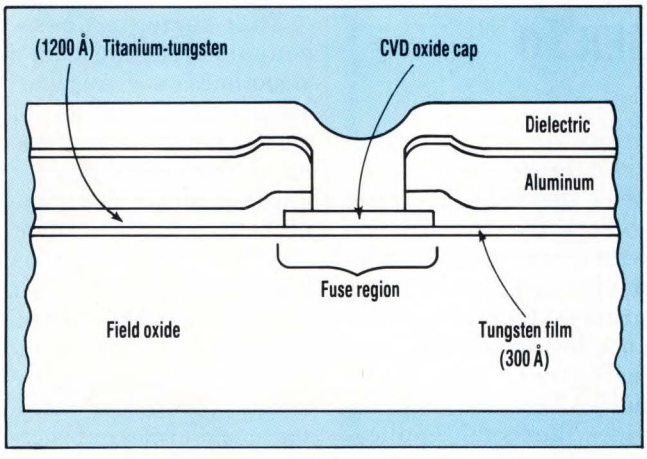
DAVID MALINIAK



PURE TUNGSTEN FUSES SHRINK DELAYS IN PROGRAMMABLE ECL DEVICES

Resistance is a curse that limits speed in any high-speed circuit, therefore affecting overall chip performance. Thus, when designers at National Semiconductor Corp., Santa Clara, Calif., had to create a new generation of extremely fast programmable ECL chips, they spent much of their time developing a low-resistance lateral fuse made of pure tungsten. With the resulting fuse structure, signals can propagate faster than ever through the unblown links.

Titanium-tungsten (TiW) has been the favored material combination for most bipolar fuses, but its resistance is about twice that of pure tungsten. National made small, low-resistance fuses by separating the TiW barrier metal film from the tungsten fuse material. In that way, the thickness and size of both the barrier material and the fuse can be separately optimized. In addition, an isotropic plasma etching can be used on the



tungsten to form very small and precisely-shaped fuses.

The basic fuse structure starts with a thin film of pure tungsten (about 300 Å) that sits on top of the field oxide *(see the figure)*. The tungsten is then patterned into the fuse links. Next, the link regions are covered with an oxide layer formed by chemical vapor deposition. Then, a thicker (1200 Å) TiW barrier film that's self-aligned to the first layer is deposited. Afterwards, a standard aluminum interconnection layer is deposited on top of the barrier film.

The TiW barrier film prevents any aluminum spikes from punching through the thin tungsten layer and pushing their way through the field oxide to cause a short to the active region of the wafer. Finally, windows (openings) are etched in the combined Al-TiW layer above each link region and the wafer's surface is covered with a dielectric layer.

With dry etching and high-resolution, direct-step-on-wafer lithography, National Semiconductor could work with very tight design rules, keeping the IC chip area small. Moreover, fine design rules minimize the performance loss that parasitic elements cause. As a result, forthcoming programmable ECL circuits will have about half the propagation delays of previous ECL PLDs. The first commercial use of the tungsten fuse will be in a family of ECL PLDs with 2-ns propagation delays that National plans to release later this year.

DAVE BURSKY

OUTPUT CONTROL QUIETS NOISE USUALLY FOUND IN ADVANCED CMOS LOGIC

Because of its high speed and rail-to-rail voltage swings, advanced CMOS logic generates lots of noise. Types of device-generated noise include dynamic-threshold shifting, which can cause false triggering; undershoot, which can induce ringing and random failures; and ground bounce, which can also produce false triggering.

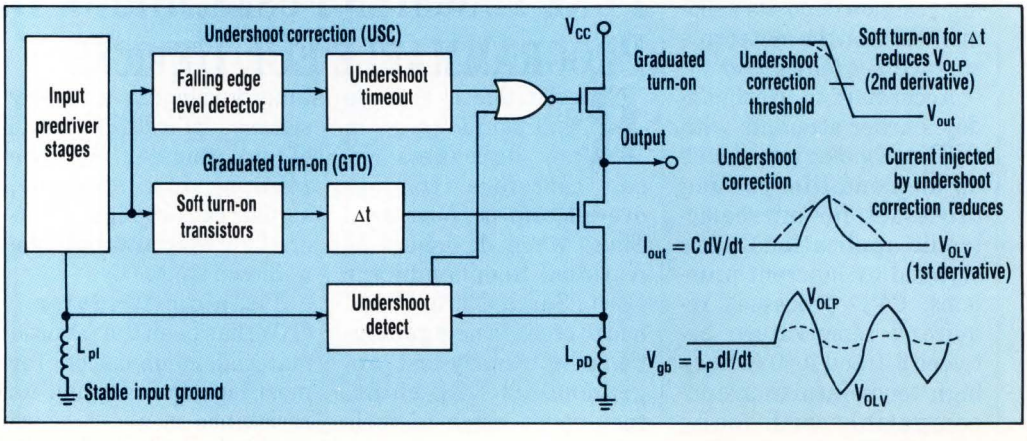
Innovative design techniques used by National Semiconductor, Portland, Maine, control a device's output to cut device-generated noise. These techniques include a split ground bus and leadframe, graduated output n-channel turn-on, and an output-undershoot correction circuit *(see the figure)*. National is putting these improvements in its new family of low-noise FACT (Fairchild Advanced CMOS Technology) logic parts, called the FACT Quiet Series (QS) family.

The split ground bus and leadframe address dynamic-threshold shift. Threshold shift is caused by the ground noise resulting from outputs switching simultaneously. Because separate input and output ground buses eliminate dynamic-threshold shift, the FACT QS parts have two ground buses—one for the input transistors and one for the rest of the internal gates, including output transistors. To further isolate output noise from the inputs, National Semiconductor designed a split leadframe for the ground pin.

Ground bounce is the voltage induced on the device ground by a current being quickly discharged into the output n-channel transistor. It occurs only during the transition of the active outputs of the device. Subsequently, ground bounce only poses problems for asynchronous lines.

The graduated-output, n-channel turn-on circuit virtually eliminates ground bounce, which is a function of the output waveshape. In the past, ground bounce was only slightly reduced by decreasing package and chip inductance. By rounding the high-to-low edge on the transition point, the graduated turn-on (GTO) circuit more effectively reduces ground bounce.

In the GTO circuitry, soft turn-on transistors change state at a relatively slow rate, thereby rounding the edges of the output-



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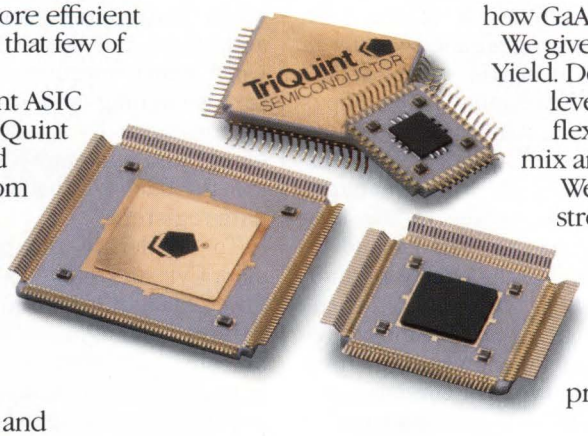

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voltage waveform. And because ground bounce is more substantial on the high-to-low transition, the low-to-high transition remains unchanged. The graduated turn-on technique cuts ground bounce to about 1 V from 2 to 3 V in a conventional part,.

Undershoot corrector (USC) circuitry eliminates output undershoot on the switching and quiescent outputs. Undershoot is a product of the change in current as a function of time (di/dt). As output edge rates speed up and voltage swings increase, undershoot increases. Undershoot also increases with the number of outputs being switched at once.

The undershoot correction circuit is a two-stage design. The first stage senses a high-to-low edge. At a predetermined point on that edge, the undershoot corrector turns on, controlling the turn-on of the transistor that supplies current to the output. In the first stage of the circuit, a resistor-capacitor (RC) timer controls the duration and the decay of the correction.

The second stage of the design backs up the first stage. If the RC timer should time out before undershoot is fully resolved, a differential amplifier senses that the output voltage is still below a reference ground. Consequently, it assumes control of the corrector current source.

LISA GUNN

MATH CHIP, COMPATIBLE WITH 80387, CHURNS OUT NUMBERS UP TO TEN TIMES FASTER

A forthcoming math chip that's totally software- and pin-compatible with Intel's 80387 numeric coprocessor can deliver more accurate results five to ten times faster the Intel chip. Essentially, it can do simple floating-point additions as fast as Intel's 80386 can do integer addition. Furthermore, the CMOS chip takes only one-twentieth the power during standby (just 35 mW) and about one-third the 80387 coprocessor's power when active (only 200 mW).

To achieve all this, Cyrix Corp., a startup firm in Richardson, Texas, came up with new algorithms for division, square root, and transcendental functions that cut the required computation time and silicon area. With a 1-μm process, the chip can operate at system clock rates of 20, 25, and 33 MHz.

Like Intel's 80387 math chip, the Cyrix CX-83D87 FasMath IC follows the IEEE-754-1985 floating-point standard with the 80-bit extended precision option. It also does eight transcendental function evaluation commands: F2XM1, which evaluates 2^x-1; FCOS, which finds cos(x); FSIN, which finds the sin(x); FSINCOS, which evaluates sin(x) and cos(x) and returns both values; FPTAN, which gives tan (x); FPATAN, for arctan(x); and FYL2X and FYL2XP1, which evaluate $y \times \log_2(x)$ and $y \times \log_2(x+1)$. To help the math chip calculate transcendental functions, it stores such preprogrammed constants as pi, $\log_2(e)$, and $\log_2(10)$.

Functionally, the chip is divided into three main regions. The first is the interface unit, which manages the interface to the host processor. The second region is the execution unit, which performs all of the floating-point primitive operations including operand-type conversions, normalizations, additions, multiplications, divisions, and result rounding. The third region, the control unit, supervises the execution of primitives and sequences of primitives needed to do complex operations.

It also manages traffic to and from the interface unit. Moreover, the chip has a hardware array multiplier, an independent mantissa arithmetic unit, and logic for fast division and square-root functions.

Just as the 80387, the Cyrix chip has an eight-register data stack, a control register, and a status register. The chip, however, extends beyond the 80387 math coprocessor by adding a data-register tag word, which improves context switching and stack performance by tracking empty and non-empty status for each of the eight data registers.

To accelerate the division, Cyrix developed a radix-128,000 division algorithm that minimizes chip area by permitting an unusual 19-by-69-bit multiplier structure to be used for all computations. The multiplier executes exact $A - (B \times C)$ functions in one cycle and supports either approximate or exact computation methods.

In the division scheme, the reciprocal of the divisor is used to estimate 17-bit quotient digits and an exact remainder of the quotient digit is calculated during each iteration. Consequently, precise 80-bit division is done in just four iterations. That iteration sequence also led to the use of polynomial evaluation methods to perform the computations for the transcendental functions.

Intel's chip computes with a Cordic method, which requires three to four times as many calculations as the Cyrix approach. Cyrix chose Horner's rule, which first makes it possible for the polynomial expression to be rewritten so that it can be evaluated with iterative calculations. Then the company applies a mini-max error minimization to achieve a relative error of less than 2^{-65}. As a result of the new algorithm, the new chip can perform the calculations in one-fifth to one-tenth the number of clock cycles required by the 80387.

In addition to the 80387 standard coprocessor interface, the 68-pin chip can also function in a memory-mapped mode to deliver twice the throughput of the Weitek Corp., Sunnyvale, Calif., floating-point accelerator.

With the memory-mapped mode, the chip can also work with other microprocessors. Moreover, with the broad range of application routines written for the Intel math coprocessor, it should be relatively easy to splice the routines needed to control the FasMath chip into an application program.

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CIRCLE 115

C118 REV. E

GaAs Technology Advances On Multiple Fronts

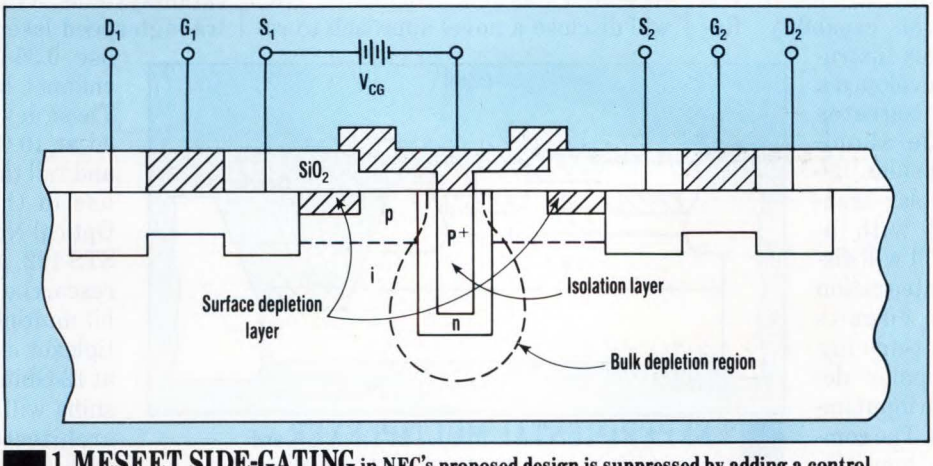
Novel Device Structures And Process And Material Enhancements Spearhead Improvements.

MILT LEONARD

Thanks to improved materials, fabrication techniques, and yield, gallium-arsenide (GaAs) technology is gaining increased prominence in high-end commercial, industrial, and military applications. This trend will be evident in the conference papers presented at this year's IEEE Gallium Arsenide IC Symposium, held at the Sheraton Harbor Island Hotel in San Diego, Oct. 22–25. Many papers will describe new GaAs chips on the verge of entering the communications, military, computer, and industrial marketplaces. Presentations on the new device structures and process technologies that will spawn next-generation market entries should be particularly interesting.

Many GaAs vendors are working to improve GaAs FET manufacturability and performance. To increase the yield of enhancement- and depletion-mode logic circuits of up to 5000 gates, ITT Gallium Arsenide Technology Center, Roanoke, Va., will propose a buried-layer, multifunction self-aligned gate process. The process uses a titanium-tungsten-nitride self-aligned 0.7-μm gate and requires only nine masking layers to make FETs, Schottky diodes, and ion-implanted and thin-film resistors. The paper will detail the fabrication process, test circuits, and parametric measurement results.

One obstacle to making high-speed, short-channel GaAs memory devices has been the difficulty of creating a self-aligned MESFET with an ion-implanted, shallow, low-resistance n-type



1. MESFET SIDE-GATING in NEC's proposed design is suppressed by adding a control gate between adjacent MESFETs and above an ion-implanted p^+ isolation layer. The n-type layer has a negative bias to prevent expansion of the surface depletion region.

channel to suppress the short-channel effect. A paper by Hitachi Ltd., Tokyo, will describe a selective-growth process that creates a low-resistance n^+ layer that suppresses the short-channel effect in a MESFET with a 0.5-μm gate. The company will demonstrate the application of the process to a 4-kbit static RAM with a 0.8-ns access time.

Another problem with GaAs MESFETs has been gate-leakage current (side-gating) during low-temperature operation. NEC Corp., Kawasaki, Japan, will describe a novel MESFET structure that suppresses this side-gating. The improved design positions a control gate on the thin silicon dioxide between two MESFETs *(Fig. 1)*. This gate is biased at the minimum negative potential of the circuit to suppress surface leakage current between the source and drain of adjacent transistors. A p^+ region located beneath the gate is surrounded by an n-type layer to suppress the bulk side-gate current. The presentation includes characteristic curves for the MESFET, static RAM waveforms, and the propagation delay of a 49-stage, DCFL (direct-coupled FET logic) ring oscillator built with the process.

Though individual GaAs devices may be faster and operate over a wider temperature range than silicon equivalents, most new silicon technologies integrate several device types for improved overall performance. For GaAs technology to compete effectively, it must have a similar integration capability. Researchers at Texas Instruments, Dallas, developed a process that integrates gallium-arsenide/aluminum-gallium-arsenide heterojunction bipolar transistors (HBTs) with p-channel JFETs. TI will discuss how this integration makes possible circuits with the current-driving capability of bipolar devices and the high input impedance of FETs. The company will cover how the complementary nature of the devices allows for the use of P-JFETs as active loads for high gain and low-voltage operation.

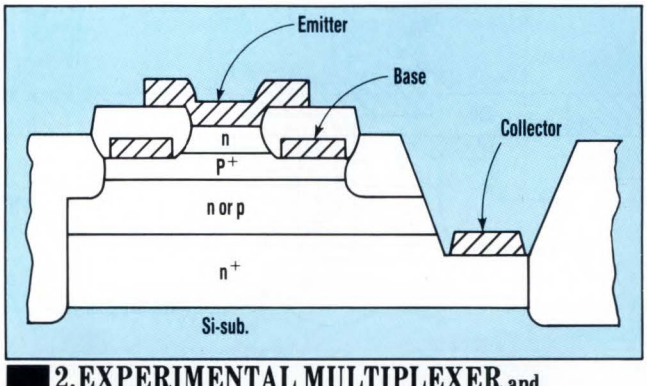
Some researchers are tweaking the AlGaAs/GaAs HBT process to create an alternative to silicon bipolar or GaAs FET technologies for application in high-speed digital communications and instrumentation. This is the case at the Toshiba R&D Center, Kawasaki, Japan. The company will report on multiplexer and demultiplexer chips that use this process to reach operating speeds that exceed 15 Gbits/s—the highest yet reported for multiplexor/demultiplexor ICs. The HBTs are built on molecular-beam epitaxy wafers with self-alignment processing *(Fig. 2)*. Toshiba will cover process and circuit details, and project how the technology can implement future ultra-high-speed systems.

A number of conference papers will report on GaAs technology developments for application in communications equipment. Regarding microwave and millimeter wave ICs (MMICs), a paper by Motorola, Tempe, Ariz., will detail the design philosophy, testing, and temperature response for a low-current, enhancement-mode MMIC amplifier intended for portable communication applications. Raytheon's Electromagnetic Systems Div., Goleta, Calif., will report on a novel MMIC-switch isolation technique that gives a 40-dB isolation over a 2- to 19-GHz frequency band. In addition, Plessey Three Five Group Ltd. and Plessey Research Caswell, Northants, UK, will disclose a novel approach to reducing the area consumed by spiral inductors on GaAs MMICs. Plessey will demonstrate the process that overlays one spiral on top of another, separated by a dielectric layer and joined in the center by a via hole. The result is inductance values as high as 20 nH but occupying an area of under 0.1 mm^2.

Other MMIC-related papers report on more esoteric aspects of the technology. For example, researchers at IBM's Systems Integration Div., Oswego, N.Y., are delving into the causes of rf gain changes in GaAs MESFETs that result from the presence of hydrogen gas. The IBM paper will explain the chemical action that leads to lower device transconductance and lower rf gain.

The promise of low-cost substrates and multiple circuit functions through integrating GaAs and silicon devices on the same chip has been blocked by major obstacles: very large dislocation densities, high unintentional doping concentration, and wafer bowing due to expansion coefficient mismatch. Hughes Aircraft Co., Torrance, Calif., will discuss their solutions to these problems. The company has built X-band power FETs by direct implantation into MBE-grown GaAs, using low-temperature buffer layers. A paper will detail the process and present test-measurement results for dc and rf characteristics.

Three companies will report on developments for lightwave communication systems: NEC will describe ultra-high-speed laser driver ICs that use 0.35-μm gate, doped channel hetero-MISFETs. These devices have operated at 10-Gbits/s with rise and fall times of 10 ps. For use in the Synchronous Optical Network (SONET) STS-192 system, Toshiba researchers developed 2-bit multiplexer and demultiplexer chips that operate at 12-Gbits/s data rate. Toshiba will discuss the chip architecture's process technology and performance parameters. Finally, a paper from AT&T Bell



2. EXPERIMENTAL MULTIPLEXER and demultiplexer chips from Toshiba are made with AlGaAs/GaAs HBTs. The HBTs have a graded-bandgap base and p-type collector structures to reduce the base and collector transit times.

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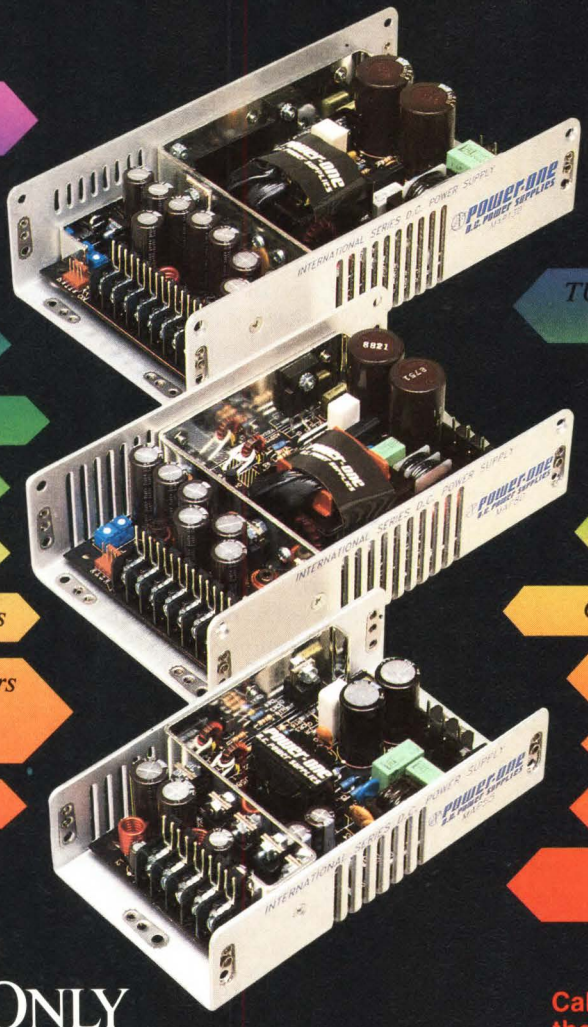

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MAP55-4001		5V @ 6A	12V @ 1A	– 12V @ 1A	24V @ 1.5A
MAP55-4002		5V @ 6A	12V @ 3A/4A PK	12V @ 1A	– 12V @ 1A
MAP80-4000	80W/110W PK	5V @ 14A	12V @ 4A/7A PK	– 12V @ 1A	– 5V @ 1A
MAP80-4001		5V @ 14A	12V @ 1A	– 12V @ 1A	24V @ 2A
MAP80-4002		5V @ 14A	12V @ 4A/7A PK	12V @ 1A	– 12V @ 1A
MAP130-4000	130W/165W PK	5V @ 20A	12V @ 5A/8A PK	– 12V @ 1A	– 5V @ 1A
MAP130-4001		5V @ 20A	12V @ 1A	– 12V @ 1A	24V @ 3.5A
MAP130-4002		5V @ 20A	12V @ 5A/8A PK	12V @ 1A	– 12V @ 1A

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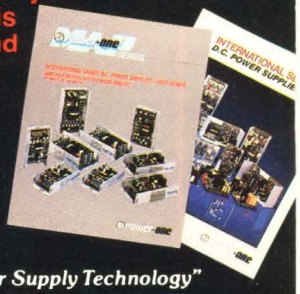

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CIRCLE 82

GALLIUM ARSENIDE

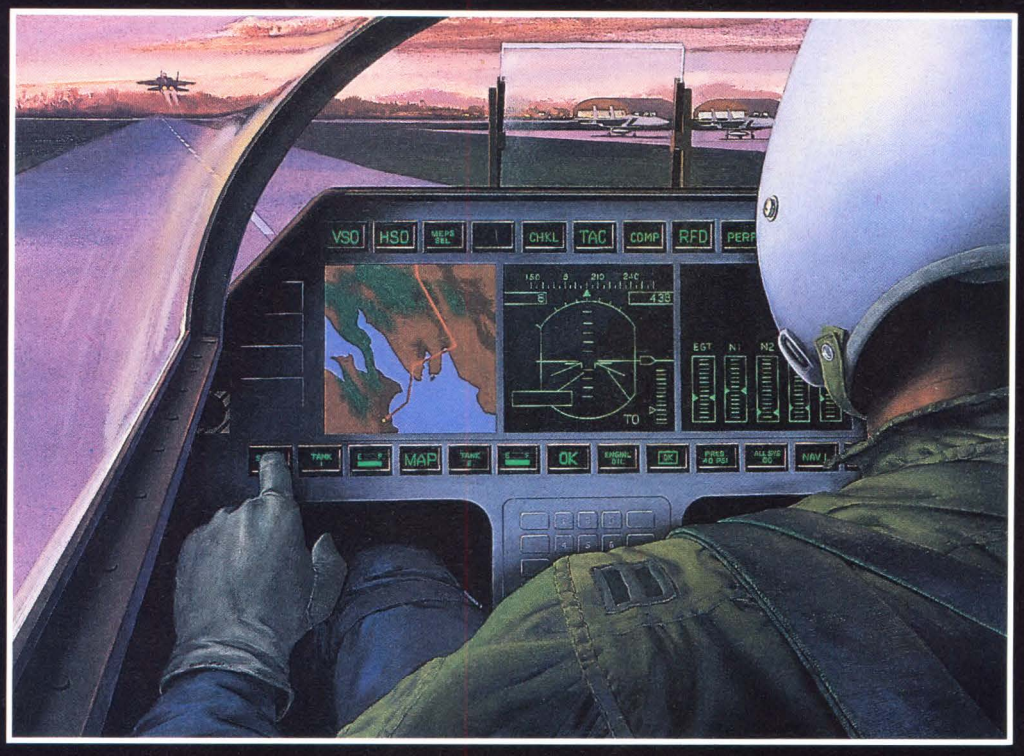
Laboratories, Murray Hill, N.J., will detail the company's GaAs-on-indium-phosphide MESFET structures and GaAs/AlGaAs devices on Si substrates for use in military and lightwave communication systems.

Though intrinsically more resistant to some forms of radiation than silicon, GaAs is still vulnerable to single-event upset (SEU). Soft-error rates for GaAs FET static RAMs are about 10^{-5} to 10^{-6} errors/bit-day, compared with the 10^{-10} errors/bit-day for CMOS/SOS static RAMs. With high device yields allowing for designs with higher device counts per memory cell, it becomes possible to include active circuit-hardening in the memory chip. North Carolina State Univ., Raleigh, N.C., under the DNA/DARPA SEU Radiation Effects Program, will examine the effectiveness of this approach. The university will present experimental results and as well as data that shows that GaAs FET static RAMs designed with SEU-hardening as a priority can be used in high-performance space microelectronics.

Until now, little investigation has been reported on regarding alpha particle immunity for GaAs static RAMs. But Mitsubishi Electric Corp., Hyogo, Japan, will disclose a 16-kbit GaAs static RAM with improved immunity from alpha-particle induced soft errors. It will discuss the fabrication process, performance, and the novel circuit designed used for the 7-ns, 2.1-W chip.

TRW Inc., Redondo Beach, Calif., has conducted radiation hardness testing for GaAs/AlGaAs HBT technology. It will detail the device structure, test conditions and instrumentation, and test results for neutron, total ionizing radiation dose, and dose rate environments. TRW will conclude that the promising test results make this technology a candidate in the front-end analog, digital, and data-conversion systems in severe radiation environments.□

How Valuable?	Circle
Highly	562
Moderately	563
Slightly	564



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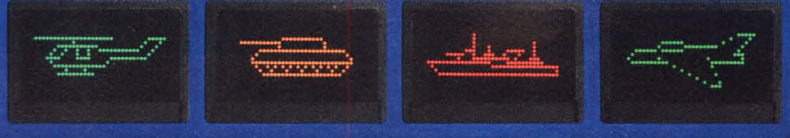

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CIRCLE 83

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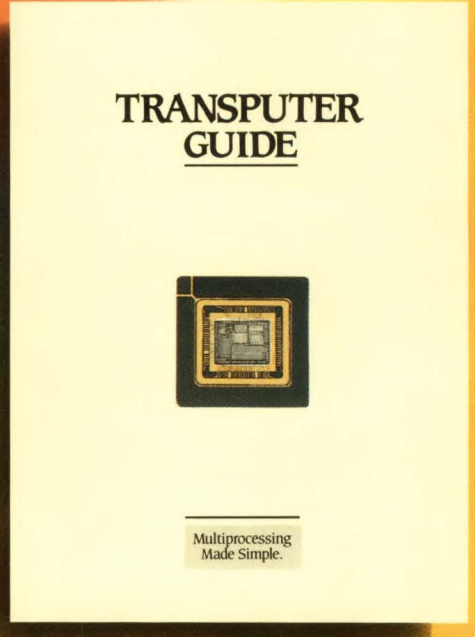

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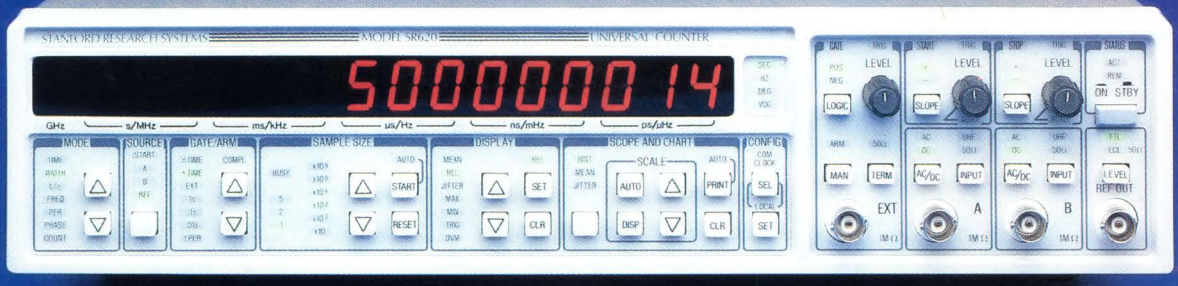

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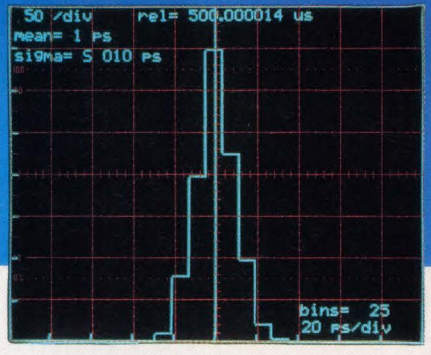

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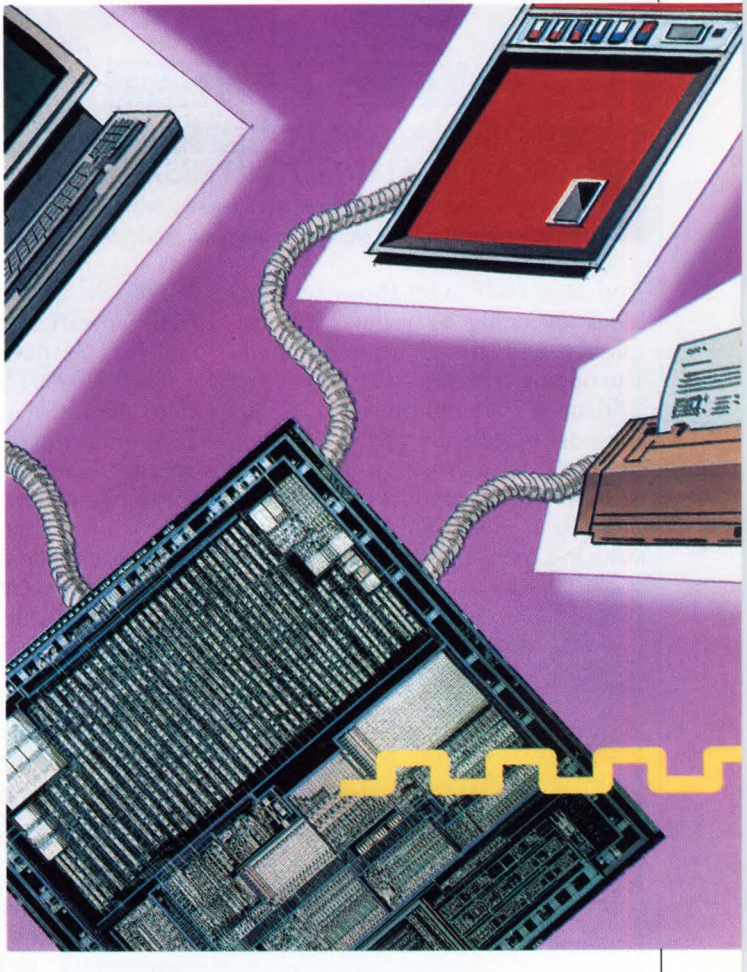
CIRCLE 85

ECHO-CANCELLING TRANSCEIVER FEATURES FLEXIBLE NETWORK INTERFACE FOR ADJUSTING TO EVOLVING ISDN STANDARDS.

U-INTERFACE TRANSCEIVER INTEGRATES ANALOG AND DSP

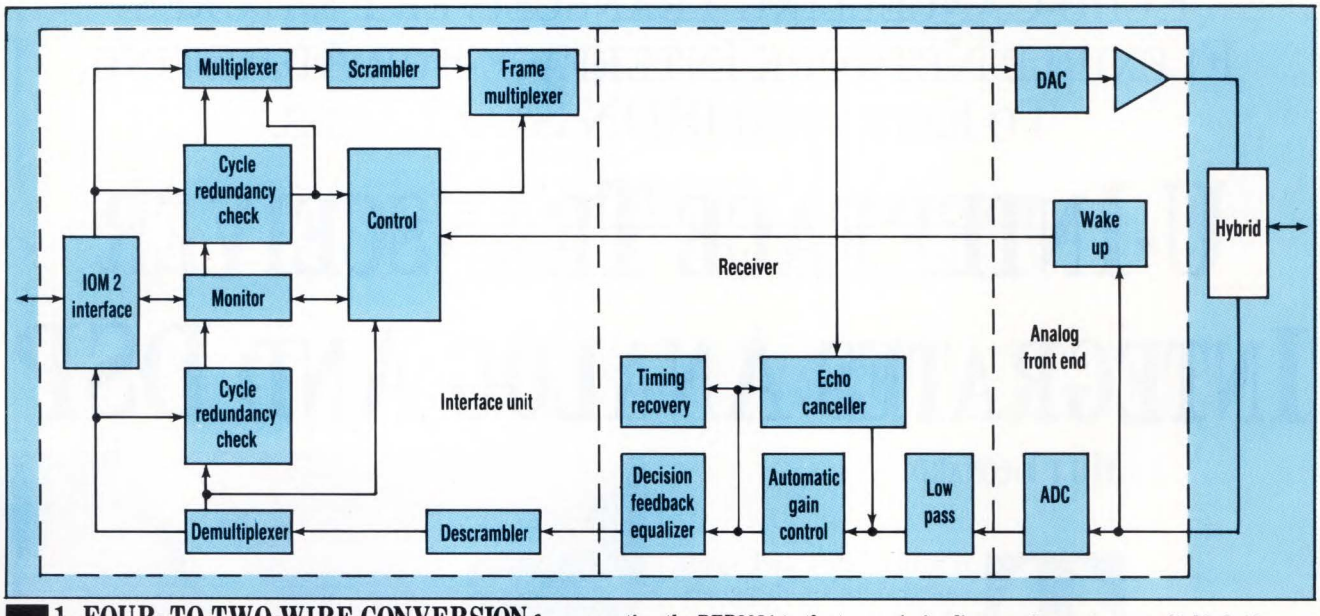
MILT LEONARD



To satisfy cost and space constraints of designers of Integrated Services Digital Network (ISDN) systems, semiconductor manufacturers have been busy cramming more functions onto one chip over the last few years. Nowhere has this been more noticeable than with the ISDN U-interface chip, which because of its analog functions and digital complexity has resisted integration onto one chip. After introducing multifunctional, single-chip transceivers that integrate communications controllers with various ISDN S- and T-interface circuits four years ago, Siemens Integrated Circuit Div. has now succeeded with the industry's first all-CMOS, single-chip U-interface transceiver. The PEB2091 includes full-duplex transmission and digital adaptive echo-cancellation circuitry.

Aimed at implementing the U-interface function in ISDN terminals, private automatic branch exchanges, and central-office exchanges, the 2091's architecture stems from a two-chip set designed for the German post office, according to the Deutsche Bundespost's FTZ Guideline ITR220 specification. To expedite market entry in Europe, where most of the world's ISDN installations are, Siemens separated the original product's digital and analog functions into two chips.

For the U.S. version, the 2091, Siemens applied experience gained from developing the European chip set to integrate both analog and digital functions on an 8 × 8-mm die using a 2-μm CMOS, double-metal, double-polysilicon process. Containing 70,000 transistors, the 5-V chip dissipates just 300 mW of power in the active mode and 30 mW in the standby mode. By comparison, multiple-chip solutions require more board space and dissipate over 1 W of power. Where the European ver-



1. FOUR- TO TWO-WIRE CONVERSION for connecting the PEB2091 to the transmission line requires a user-supplied hybrid circuit consisting of a transformer and a resistor network. For interconnecting different function modules in a network terminal, the IOM-2 interface consists of four physical connections: two lines for data and one line each for frame and data clocks.

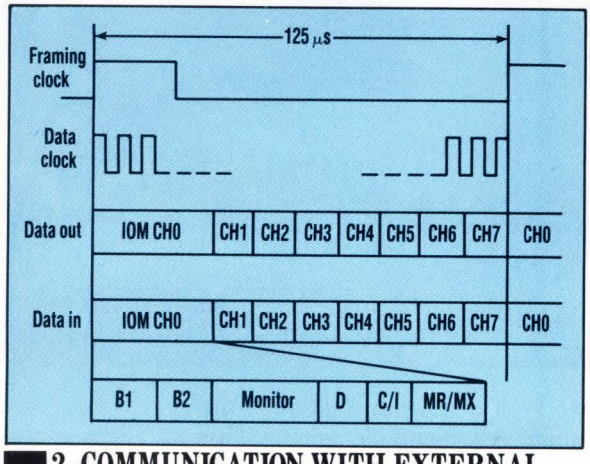
sion uses 4B3T (4-bit three- ternary) block encoding to reduce the frequency and signal attenuation on European transmission lines, the 2091 uses 2-bit 1-quaternary (2B1Q) for more effective noise suppression on U.S. transmission lines *(see "Combating transmission line impedance," p. 47)*. This technique results in a transmission range of up to 18,000 ft. according to the ANSI 604.2 specification, at an 80-kbaud (160-kbits/s) data rate.

The PEB2091 has three main function blocks: a digital system-interface unit, a digital receiver, and an analog line-interface unit *(Fig. 1)*. The system interface unit (SIU) performs activation and deactivation procedures per ANSI standards. In addition, the SIU implements all defined U-interface maintenance functions. Data is transferred through frame conversion, speed adaption, and descrambling functions. The scrambler and descrambler circuits are also part of the chip's digital signal-processing engine that performs the functions of adaptive equalization and echo cancellation.

Adaptive equalization deals with the problem of unknown transmission-line characteristics, which can be the source of transmission errors and noisy transmission. During the power-up routine, a training sequence calculates transmission-line impedance characteristics. The chip then uses the results to calculate the line's inverse transfer characteristics. The DSP engine applies this calculation to the incoming signal to restore the original pulse shapes, for more readily discernible pulse amplitudes and logic levels.

The SIU communicates with other network elements through the IOM-2 (ISDN-oriented modular) interface, an architecture jointly developed by four of Europe's largest suppliers of telecommunications equipment (France's CIE Alcatel, Italy's Italtel, Plessey of the United Kingdom, and Siemens of W. Germany). Also gaining acceptance in the U.S., the IOM-2 interface uses a four-wire bus to communicate with other ISDN chips without the use of glue logic. One wire carries an 8-kHz framing clock signal; a second wire carries the programmable data clock, which can range from 512 to 4096 kHz. The remaining two wires transmit data, one wire being used for each direction between the subscriber and network.

A 4096-kHz data clock corresponds to a 2048-kbit/s transmission



2. COMMUNICATION WITH EXTERNAL devices through the IOM-2 interface is over eight channels, multiplexed within the 125-μs superframe (shown here for an 8-kHz clock). Each channel has subchannels for voice and data (B1 and B2), signaling and packet-switched data (D), bits for control operations (C/I), a monitor (MON) channel for transferring maintenance data and messages, and handshaking bits (MR/MX).

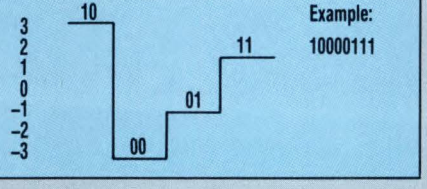
COMBATTING TRANSMISSION-LINE IMPEDANCE

Resistance, capacitance, and inductance in copper telephone lines combine to form a low-pass filter that distorts the shape of transmitted pulses. If the transmitted signal is a stream of ones and zeros, each high-level signal will inject energy into the energy-storing elements of the line impedance, and each low-level signal will discharge the line. If the number of ones and zeros is the same, the net energy in the line is zero. But in the more likely scenario, where they're not, the line will store energy during these unbalanced periods. The resultant dc offsets are superimposed on the transmitted signal, making it difficult to decode and degrading overall system performance.

As a result, transmission codes were developed that use multiple signal levels—positive highs, zero, and negative lows. The highs and lows are alternated to represent the same logic level, resulting in a balanced signal. Of the coding techniques in use, block codes have the highest performance in noise-free transmission and range, though they're difficult and expensive to put in silicon.

Siemens selected the quaternary block code for the PEB2091 because its performance best matches the transmission characteristics of U.S. telephone lines. To keep the line balanced, this technique encodes two bits as a quaternary symbol (+2.5, +0.83, –0.83, or –2.5 V) *(see the figure)*. Because each quaternary symbol represents two bits, a further benefit is twice the data rate for a given frequency. This increases the range, because line attenuation of the transmitted signal is proportional to frequency.

First bit	Second bit	Quaternary symbol	Amplitude (volts)
1	0	+3	+2.5
1	1	+1	+0.83
0	1	−1	−0.83
0	0	−3	−2.5



rate and eight multiplexed IOM channels per 125-μs frame. Consequently, up to eight transceivers can be connected to one IOM interface *(Fig. 2)*.

For the ISDN 2B+D 144-kbit/s basic access data rate, each multiplexed frame contains two circuit-switched 64-kbit/s channels for transmitting voice, data, text, and images (B1 and B2); a monitor (MON) channel that transfers maintenance messages and data; a message-oriented 16-kbit/s D channel for signaling, packet, and telemetry information; four command and indication (C/I) bits for controlling chip activation and deactivation; and monitor handshake (MR,MX) bits for data-flow control in the monitor channel.

The IOM-2 interface provides the platform for a flexible and powerful bus structure. For example, portions of a system design can be modified with minimal software changes, as U-interface standards change for coding, data transport, and other functions. The embedded control function in the IOM-2 bus makes possible back-to-back connection of the transceivers to create repeaters, which are needed to boost signal strength in lines exceeding about 18,000 ft long. Typically, designers prefer to power repeaters from the line, not from separate power supplies.

Implementing a repeater with low-power back-to-back transceivers reduces cost and power-supply requirements. As another example, an S-interface transceiver can be extended to implement the U interface by using products with the IOM architecture.

Principal DSP functions are performed by the receiver (REC), which has a multiprocessor architecture, with the various DSP algorithms separated into data-path modules with bus connection and global control. The REC performs echo cancellation, pre- and post-equalization, phase adaption, and frame detection. Unwanted echoes on a transmission line result from signal reflections to impedance mismatches at line splices, taps, and imperfectly designed line interfaces.

A 36-Tap FIR Filter

For echo cancellation, the REC uses 36-tap, 20-bit adaptive finite impulse-response filters to remove line echos and crosstalk from the received signal. An automatic-gain-control function contributes to optimizing the receiver's dynamic range.

The line interface unit (LIU) contains a crystal oscillator and all of the analog functions, including an analog-to-digital converter in the receive path, a pulse-shaping digital-to-analog converter, and a line driver in the transmit path. The LIU also includes an analog test loop, a ranging function, and a signal-level detector.

The LIU connects to the telephone transmission line through a user-supplied hybrid circuit that consists of a transformer and a resistor network. The transformer interfaces the four-wire signal from the 2091 to the two-wire telephone transmission line of the network. It also attenuates some noise. Signals from the telephone transmission line pass through the hybrid circuit to a wake-up circuit, which initiates power-up procedures, and to the a-d converter. The a-d converter is a second-order sigma-delta modulator with a 15.36-MHz clock, for a clock-frequency/base-bandwidth ratio of 192:1.

Maximum pk-pk input-signal voltage is 4 V, which conforms to present ASCII specifications for signal voltages on telephone transmission lines. For short transmission lines, automatic ranging attenuates the input signal by about 6 dB.

Internally tying the a-d converter to the transmitter's output through software control activates an analog test loop, which can be used to isolate problem areas on the telephone transmission line. Input-signal damping increases to about 12 dB when the range and loop functions operate concurrently.

Converting TTL pulse trains from network devices into quaternary code symbols with four different pulse amplitudes is the job of the d-a converter, which uses a differential switched-capacitor technique. The d-a converter's staircase-like output signal drives the output buffer's line drivers that are operating in a bridge configuration with a gain of 2. This signal is fed to the 2091's output through a switched-capacitor, low-pass filter and a first-order, resistance-capacitance filter with a nominal corner frequency of 1 MHz.

High-Resolution Word

A digital filter circuit converts the output signal to a standard digital word with a resolution and linearity of 65 dB. This is equivalent to about 11 bits. All clocks in the analog portion of the PEB2091chip are derived locally from the 15.36-MHz master clock.

Product development support for the 2091 is supplied by the Siemens ISDN PC development system, which makes it possible for hardware designers to simulate placement of a voice or data call through an AT&T #5 ESS (electronic switching system) central-office exchange. Among the applications that can be simulated are voice and data terminals, line cards, and primary-rate cards configured with various ISDN line interfaces.

The support system consists of a coprocessing board, a family of plug-in modules that make possible different equipment configurations, and AT&T-compatible call-control software. Other software packages are available from Siemens for system integration and testing functions.□

Price And Availability

Slated for sampling in November, the PEB2091 will be available in volume in the second quarter of 1990 for about $60 each. Depending upon configuration, the ISDN PC development system goes for $3000 to $5000.

Siemens Components, 2191 Laurelwood Rd., Santa Clara, CA95051; (408) 980-4535.

CIRCLE 513

How Valuable?	Circle
Highly	556
Moderately	557
Slightly	558

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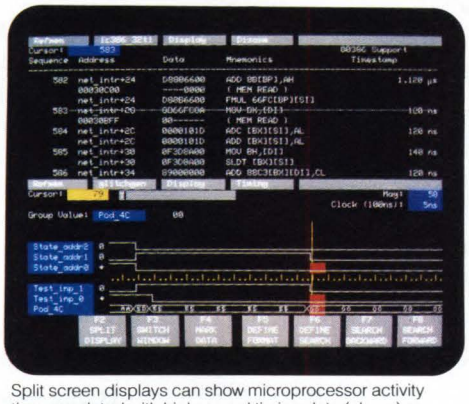

Split screen displays can show microprocessor activity time correlated with high-speed timing data (above) or disassembly of another microprocessor. The cursors can be locked to scroll in parallel, highlighting data nearest to the same point in time.

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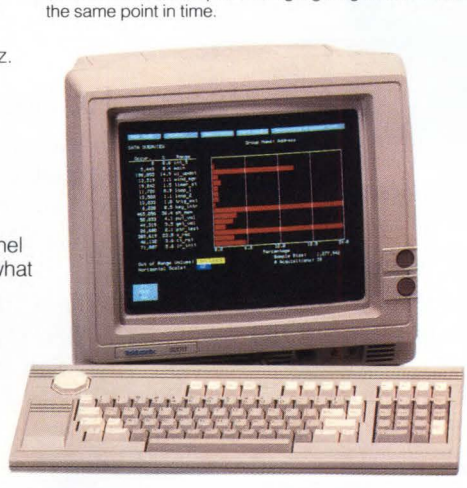

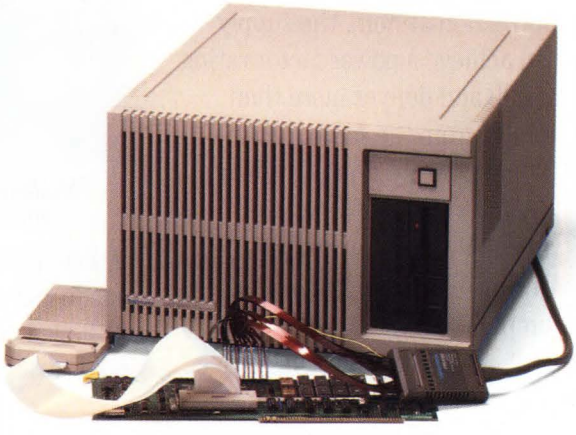

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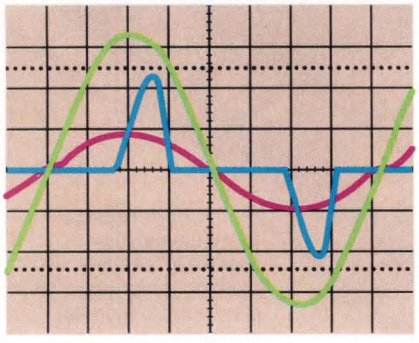
Now power factor correction is possible with just one chip.

New IC Produces 0.99 Power factor in Off-line Power Supplies.

Introducing the new Micro Linear ML4812 Power Factor Correction System, the first control IC dedicated to Power Factor Correction for Switch Mode Power Supplies.



AC Line Voltage
Line Current With Power
Uncorrected Line Current

Clean Power.

Conventional power supplies exhibit poor power factor (0.7) with a 700W limit to the amount of power that can be delivered from a conventional 15A AC line. With the new ML4812 Power Factor Correction system, the supply can achieve a power factor rating of 0.99 and deliver more than 1000W from the same 15A line.

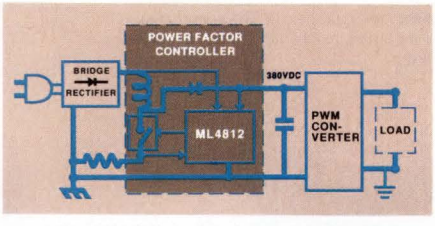
Since the system works from 90V AC to 265V AC, supplies using the ML4812 can be designed for Worldwide use without using jumpers or switches.

The ML4812 also helps reduce the "pollution" created by the undesired harmonics generated by short pulses of line current into the storage capacitor. That ability is especially beneficial now that regulations are pending in Europe to limit the harmonics that can be put on the line.

Easy to Use.

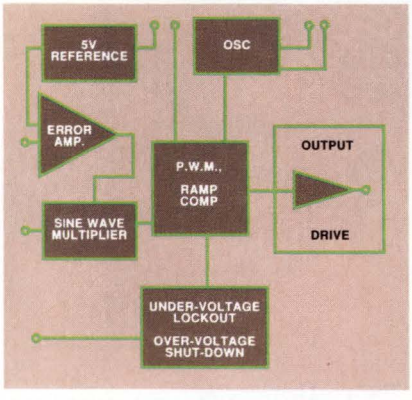
The new ML4812 is the core of a unique current-mode boost regulator with a controller that forces current in the regulator to be sinusoidal. With the ML4812, you can achieve a power factor of 0.99 and a load regulation of 1% from no-load to full-load.

To facilitate the wide-duty cycle range necessary to cause sinusoidal current, the ML4812 has internal programmable ramp compensation. An Over-Voltage Monitor Circuit protects downstream circuitry by shutting down the outputs when the load is suddenly interrupted.



The ML4812 is the Core of a Power Factor Correction System

A low-quiescent current start-up mode is controlled by the Under-Voltage Lockout Circuit with 7V hysteresis.



ML4812 Includes All Control Functions For Power Factor Correction.

Better Noise Immunity.

At the heart of the ML4812 is a current input multiplier which dramatically reduces the IC's susceptibility to switching-induced ground noise. To further enhance noise rejection, the control circuit has a 5V dynamic range, while most conventional current-mode PWM ICs only have a 1V range.

Easily Customized.

The new Micro Linear ML4812 is implemented on the FB3490 analog array, and can be easily modified for power supplies with special needs.

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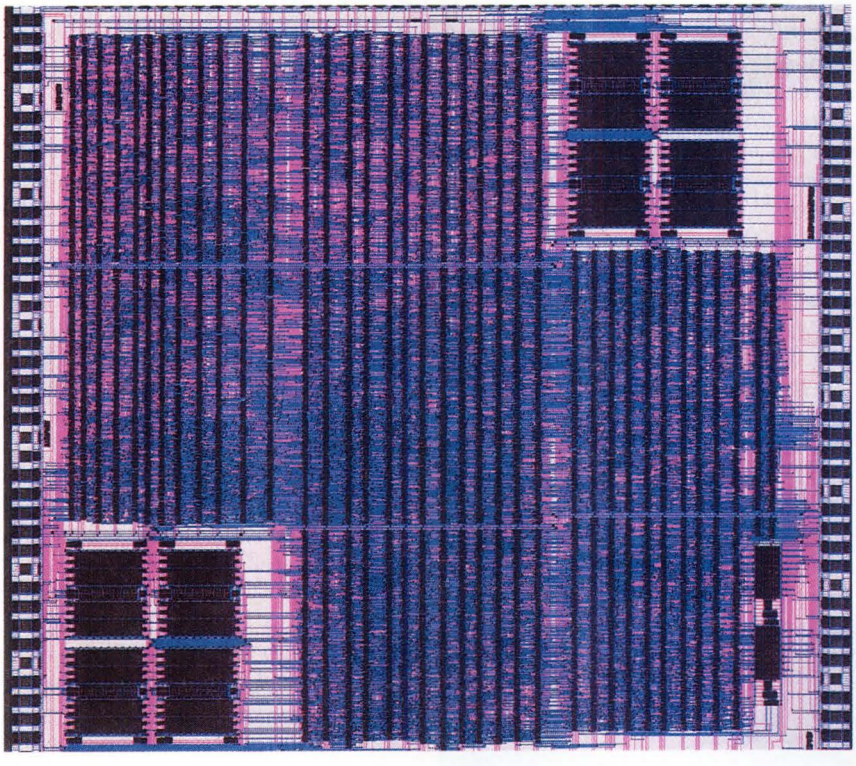


RICHARD NASS

COMPANIES ARE DISCOVERING THAT BUILDING ASICS IS AN ART THAT THEY SHOULD MASTER.

ASICs: THE LATEST ALTERNATIVE

Now that application-specific ICs (ASICs) have proven their mettle, designers are discovering that the important decision isn't so much whether or not to go the ASIC route, but rather which ASIC technology to choose. Seven specific cases illustrate how designers have followed different ASIC paths. In each case, various difficulties were encountered, including timing problems, tool inefficiencies, and placement-and-routing obstacles.

For instance, Motorola's ALPC 1, a high-density CMOS array used in laser-printer controller-board applications, was made with a triple-layer metal CMOS process. The chip, a 16,000-gate 1-μm channelless array, replaces an array made with a 2-μm technology. The chip was routed on all three layers to increase the use of its channelless sea-of-gates architecture from about 40 to 80%.

As part of a controller board, the ALPC 1 chip links the laser printer's microprocessor with its dynamic RAM. Working with Personal Computer Products Inc., San Diego, Motorola attempted to lower the cost and improve the speed of the printer (from 6 to 15 pages/min). Engineers from both companies mulled over the specifications that would have to be met to make such a device workable based on the laser printer's system requirements.

The chip, which was actually designed by two Motorola engineers in Chandler, Ariz., was to be used in a second-generation laser printer with expanded capabilities. But the microprocessor, a 68000, and the print engine weren't changed. The goal was to make it possible for the 68000 to emulate a 68020 without actually changing processors. The new interface also allowed for an easy upgrade to a 68020.

A raster-operations section was added to the chip. This section implements in hardware some of the more complex algorithms that the microprocessor must go through to send the data from the engine's memory to the page. Here, performance improvements were obtained without switching to a more exotic, high-performance microprocessor.

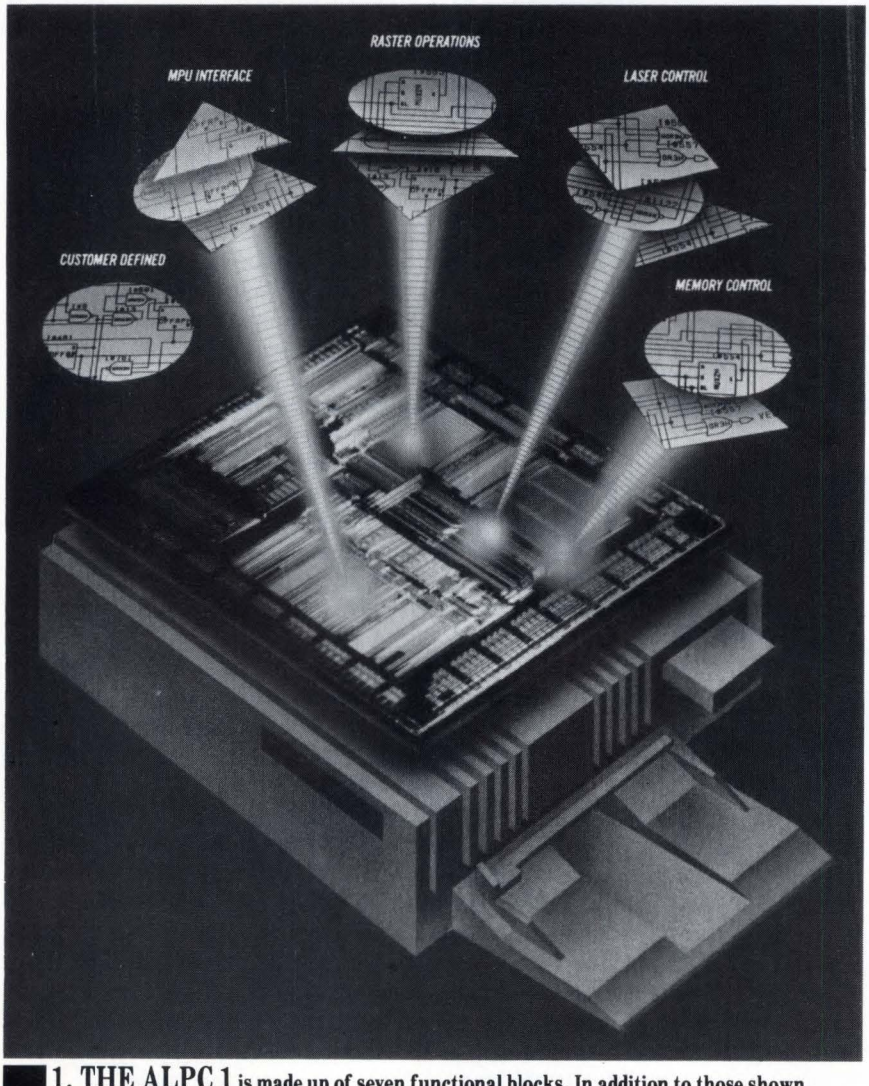
Because of the high density of the

array family, more logic can be squeezed onto the chip and routine software algorithms can be run in hardware. The ASIC also eases the microprocessor's workload by offloading some of the instructions to be executed. Some hooks and handles were also added to support other types of print engines.

While designing the ALPC 1, Motorola made certain that the chip remained standardized so the parts could be used later in similar designs. The ALPC 1 was created on a Mentor Graphics system. Then Motorola used its own Open Architecture CAD System for test-vector and timing verification.

The chip consists of seven functional blocks: an MPU interface, a dynamic RAM controller-interface, a print-engine controller, a serial communications interface, a 16-bit timer, raster operations, and a clock generator *(Fig. 1)*. Of the seven blocks, the raster-operations segment, which creates a bit-mapped picture for the print engine, stands out.

The raster-operations section must know when the printed data has reached the end of a horizontal line. Then it must alert the processor when this condition arises. But because of the system's configuration, this section must transfer the rectangular information one horizontal line at a time. And, depending on how the data is aligned and what type of shifting is being done to the data, two source fetches might be required before sending the print engine to the next line. This "invisible" procedure constitutes one of the largest design obstacles to overcome. It required a lot of sketching, rough drafting, and trial runs on paper to determine the correct algorithm. This created considerable concern because this first-generation chip had no previous design to copy.



1. THE ALPC 1 is made up of seven functional blocks. In addition to those shown, there's a clock generator, a timer, and a serial-communications interface.

Motorola's engineers typically begin a design by thumbing through the company's library of components, which contains all of the flip-flops, gates, multiplexers, adders, and so forth. Once the function and logical implementation of the chip is defined, the schematics are entered and connected via a workstation. The next step is to generate a net list and simulate the circuit. Stimulus patterns show what each particular block will see. The patterns are created by generating several simulation subroutines that mimic the processor interface to the ASIC chip.

Each block would then pass through that interface. The net list can also be converted to an EDIF net list (Motorola's standard internal net list). Decal, a delay-calculation tool, takes each node in the circuit and calculates the delay associated with each. The delays are based on the actual topology or fanout of each circuit component.

Once these delays are known, they can be inserted back into the Mentor database for the simulator. With Decal, users can also specify the temperature and voltage range that the chip is expected to endure. Consequently, environmental parameters can be taken into consideration before the delays are calculated.

The last step is to verify the simulation using the Verilog simulator on a VAX computer. This final check makes a complete simulation and compares the results against those obtained in the run using Mentor's QuickSim.

CONTROLLING DMA

A chip designed by NCR's PC Division in Columbia, S.C., was to be used as part of a 68030-based file-processor system in future systems—but it works just as well with present sys-

tems. The chip's function is to increase disk-access performance in a system. David Simpson, the chip's designer, says that if this chip, which is roughly 430 mils on a side, were built instead as a pc board, it would have taken up about three times the size of the 11-by-14-1/2-in. board that the ASIC chip was placed on with other circuitry.

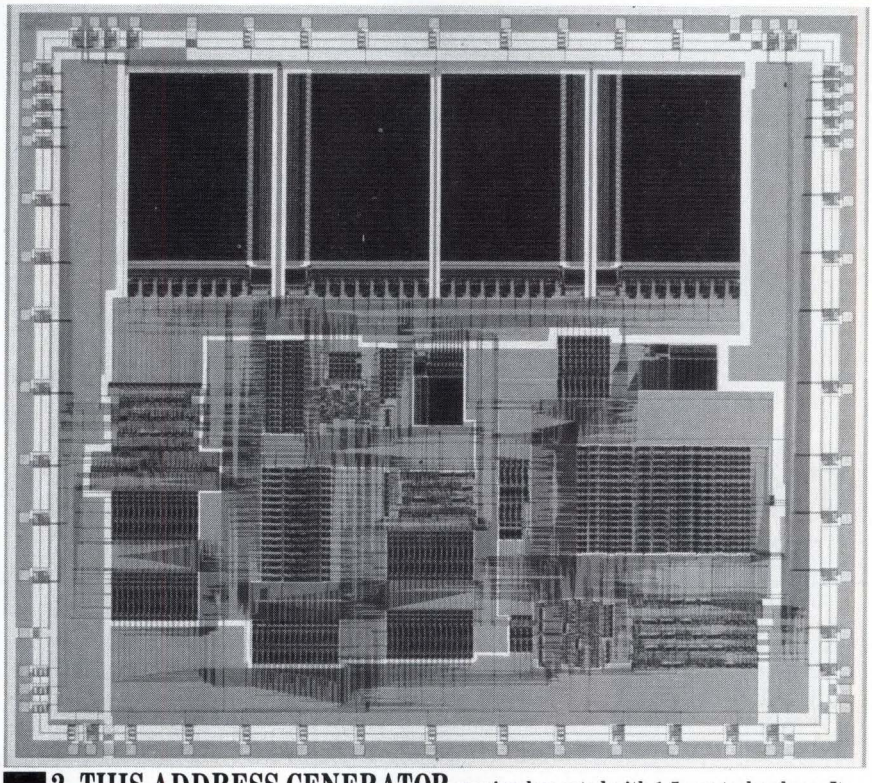
The chip is essentially a DMA controller that interfaces to SCSIbus and Multibus controllers. The advantage over previous designs is that it can execute some of the operations that were previously done by the microprocessor. And it adds more smarts to the interface between the DMA controller and the bus. The processor simply has to send the data for a transfer and the interface will carry it out.

The NCR chip actually has two different channels or interfaces. The advantage here is that one chip can do the work of two, thus saving board space while reducing cost at the same time. It can perform a disk access to or from a local-area network or it can go out onto a system bus to obtain data.

NCR's chip was designed in a Mentor Graphics environment. Mentor's schematic editor is the starting point. Then the designer used NCR's net list to extract information from the schematic and prepare it for simulation.

The next step was to run the design with functional-level verification. Here, he creates a set of models that utilize unit delay to verify that all functions are operating the way they're intended.

This particular design was one of the few that worked on the first try without any tweaking. The total design encompassed 15,000 equivalent gates. The chip was designed with a 1.5-μm technology. It contained eight dual-port compiled RAMs totaling 2 kbits of memory. The random logic includes a custom FIFO buffer. The chip's two different channels can interface to separate SCSI buses. Because of this technology, it can grab data at 5 Mbytes/s; with a Multibus, it can run at 20 Mbytes/s.



2. THIS ADDRESS GENERATOR was implemented with 1.5-μm technology. It contains about 140,000 transistors in an area of about 215,000 mils^2.

After modifying cell width and depth, a verification check can be run. At the same time, the identical tool was run at NCR's plant in Fort Collins, Colo., to generate a physical layout and automatically place and route the design. The post-layout resistance and capacitance values were then sent back to South Carolina so the original designer could input them into his workstation. Masks were then run with the actual values.

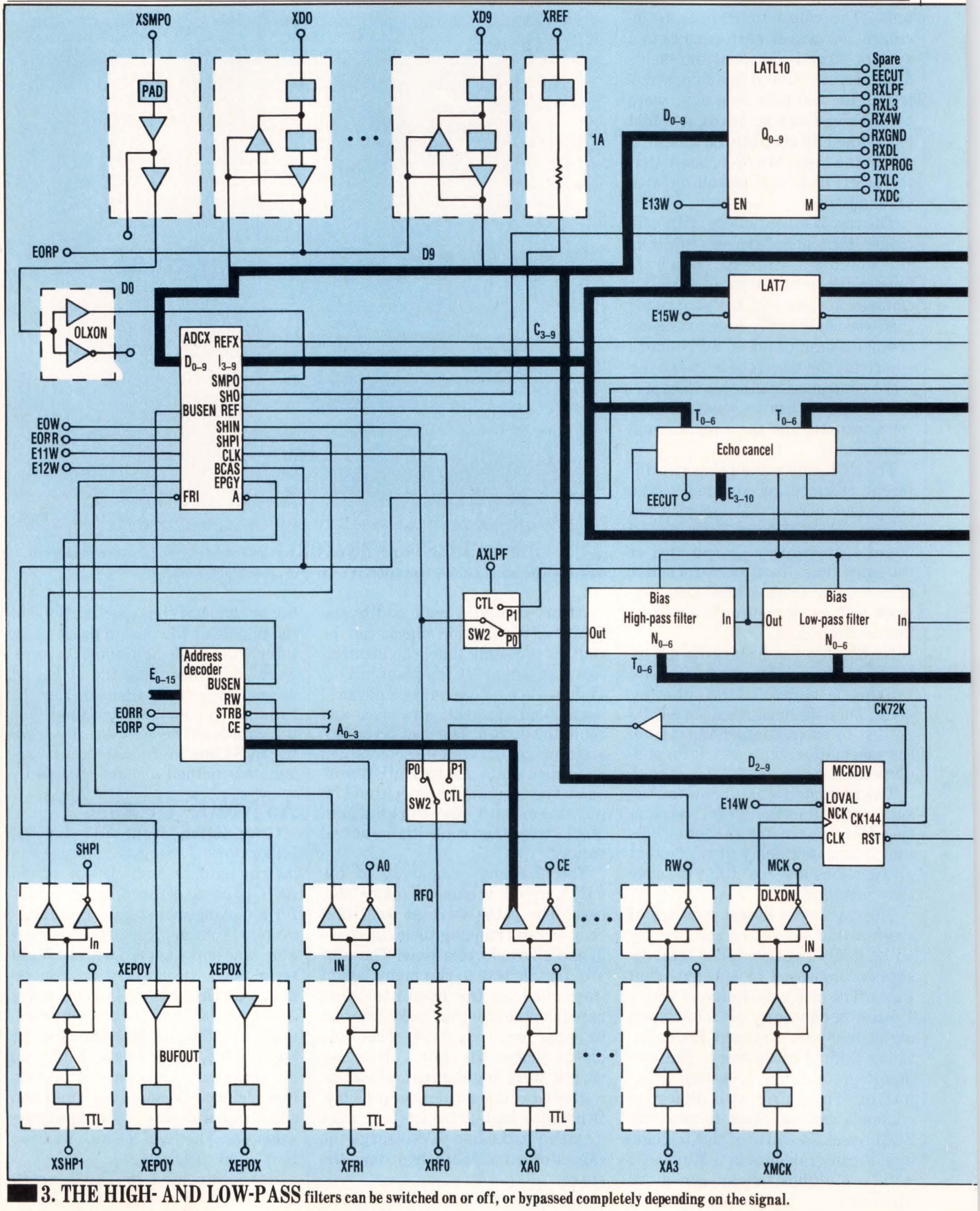
The size and complexity of the FIFO circuit became a major concern. The paths were so long that they weren't running their full route in the allotted cycle time. The way around this was to run many layout iterations on the computer, and handpick the one that looked closest to what was expected. Then the places where the worst delay occurred were highlighted. Hand reroutes were done wherever possible. Otherwise high-drive buffers were installed in the line to discharge the capacitors that were impeding the speed.

Another problem was that the customer changed chip specifications in the middle of the design process. In this particular design, some features were added including the ability to access other types of memories. In the final version, it was found that the data could be sent directly from the SCSI bus to the FIFO. As a result, this method was implemented.

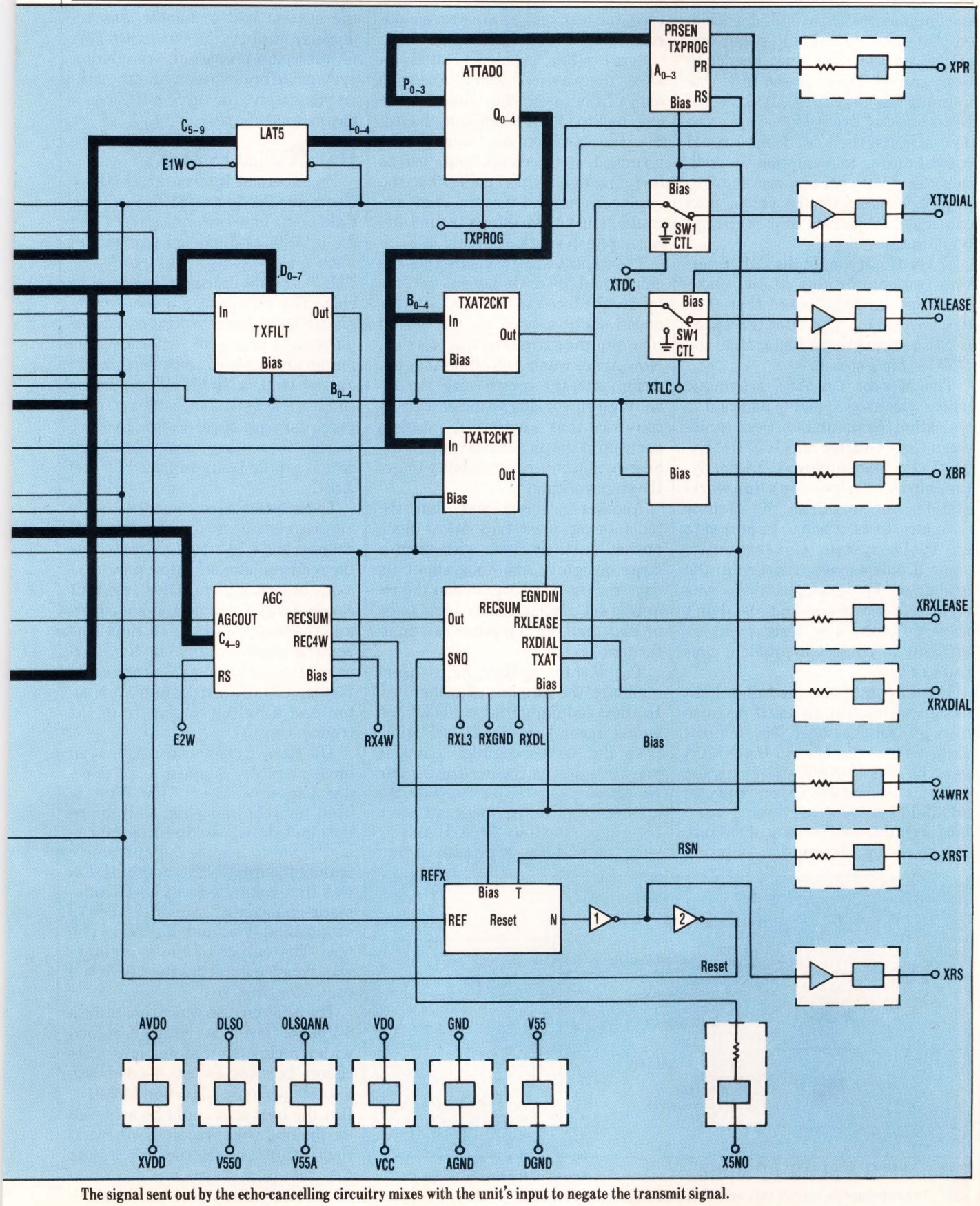
AN NMOS UPGRADE

Greg Rocco, from MIT Lincoln Laboratory, Lexington, Mass., was instrumental in the design of an ASIC to be used in a signal processor for a moving-target-detection radar system. This chip, an address generator, was implemented with a 1.5-μm technology. Because of its double-metal CMOS process, the chip holds about 140,000 transistors, of which approximately 110,000 are used for static RAM. Other areas of the chip requiring large amounts of real estate included the shift registers and some general- and special-purpose registers. The final die size was 453 by 475 mils *(Fig. 2)*.

As documented in *The Lincoln Laboratory Journal, Vol. 2, No. 1,*



3. THE HIGH- AND LOW-PASS filters can be switched on or off, or bypassed completely depending on the signal.



The signal sent out by the echo-cancelling circuitry mixes with the unit's input to negate the transmit signal.

the engineers at Lincoln Labs decided that the original chip being employed, an NMOS product, needed to be upgraded. The best way to do this upgrade was to go to a CMOS design. In addition to bringing the speed to new heights, the new design would cut the power consumption. In addition, the NMOS version was running at a speed near its top value, thus causing it to operate at a very high temperature.

Early prototypes of the CMOS version ran comfortably at the maximum speed of the board that they were placed on. This 10-MIPS speed is two to three times faster than the NMOS chip's speed.

The Mentor Graphics schematic editor was used again, in addition to QuickSim for simulation. Seattle Silicon's Chip Grafter and ICX (IC Expert) were also employed. Originally, the chip was designed on a Sun workstation, but to utilize the Mentor Graphics' tools, it had to be ported to an Apollo system. Consequently, some problems were masked in the exchange. For example, there was an interface problem that just didn't show up in the new design, and it's difficult to correct a problem that can't be seen.

Previous attempts at full-custom design weren't up to snuff because of a gap in the tools. The biggest flaw, as was the case in the NMOS version, was that the whole system couldn't be simulated at one time. In addition, test vectors weren't taken into account. Now, on top of submitting the design description for prototype, the test vectors are also included.

Some other problems came up along the way. For one, all the cells didn't fit onto the chip. Because the chip had to sit on an existing board, the size specifications were predetermined, so the components had to be rearranged. Upon doing this, the engineers learned that the database couldn't just move things around and recompile the data.

The easiest way to ensure that the chip would fit was to lay out the chip by hand. Rocco estimates that this added about a week to the design time, but the extra time was worth it. Now, there was no question that the design was the correct size. An advantage of working with Seattle Silicon was that anytime a problem came up in the physical layout, it was Seattle Silicon's responsibility to get the chip working.

Another problem was that the tools being used had never been pushed to their limit with such a large design. It also took about six days for the computer to run the required set of simulations—and most of that time the computer ran unattended.

The Mentor system helps users minimize the number of primitives. In a detailed simulation, a 16-bit latch would encompass about 200 primitives. But the tool contains an n-wide primitive that can be used as a latch. Now, by making the latch n-wide, the number of primitives was cut down from approximately 200 to 1. As a result, the number of primitives that the system had to handle was reduced from about 80,000 to 8000. This meant that a prepare-for-simulation cycle could be done in two hours rather than twelve, or three iterations a day instead of one.

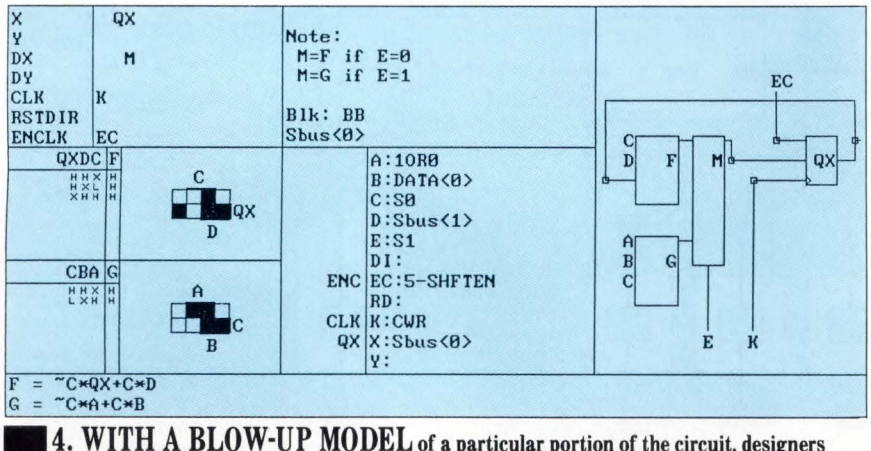
One Replaces Many

Engineers at International Microelectronic Products (IMP), San Jose, Calif., developed an analog front-end for a 9600-baud modem that works with a Texas Instruments' TMS32025 digital-signal-processing chip. The chip was intended to replace a large discrete design that employed a 14-bit a-d converter. By placing an analog echo canceler directly on the chip, a 10-bit a-d converter could be substituted, making for a much more practical design. In other words, the entire analog front-end circuitry was being replaced by one ASIC.

The solution here started with a 9-bit d-a converter for the transmit channel and a 10-bit a-d converter for the receive channel. The required analog processing for the transmit channel was a sample-and-hold operation coming out of the d-a chip. This went through a continuous-time low-pass filter with a (sin X)/X correction factor, a 24-dB (1-dB/step) attenuator, and a buffer coming from the transmit signal.

The receive channel consists of an input amplifier coupled to a 7th-order Laguerre filter. This filter is used for echo canceling as it mixes the input signal with the echo-canceling signal to negate the unit's own transmit signal. The combination was first connected to a 48-dB automatic-gain-control amplifier, then to switchable low- and high-pass filters. The output of the two filters was coupled back to the 10-bit a-d converter *(Fig. 3)*.

The original plan was to maintain a 6-Vpk-pk level. A filter designed with a technique that employs transistors as resistors was needed with a total harmonic distortion of 0.01%. But the best that could be achieved by the engineer was somewhere in the 5 to 10% range. The only way to get the total harmonic distortion down to an acceptable level was to



4. WITH A BLOW-UP MODEL of a particular portion of the circuit, designers can hand-route the signals that weren't routed properly the first time.

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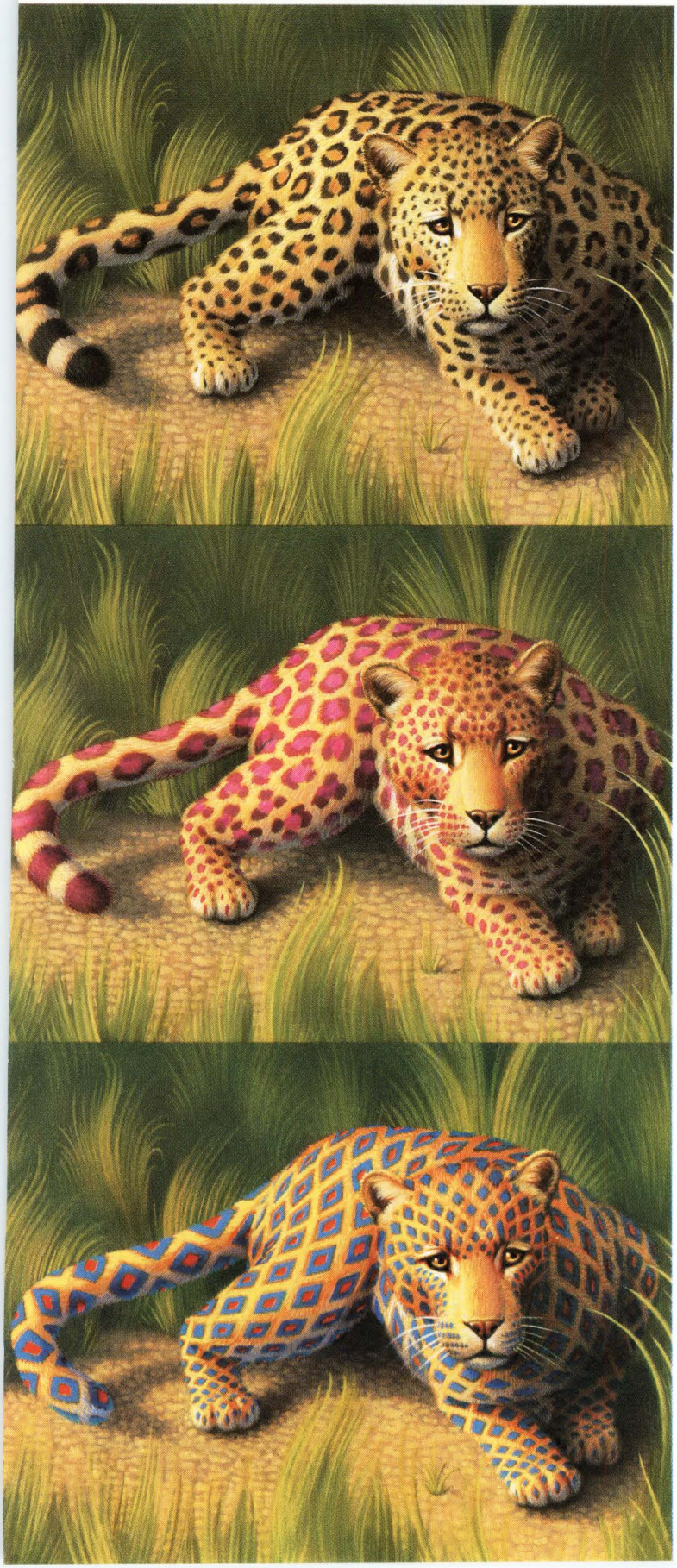

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CIRCLE 18

attenuate the input signal. But because this would throw the signal-to-noise ratio out of whack, an alternate technique had to be pioneered to generate a filter.

By adding a silicon-chromium stage to the existing double-poly, double-metal 3-μm CMOS process, a stable resistance was achieved. Now a method had to be developed to tune the RC products correctly.

Because of the computing power of the DSP chip being employed elsewhere in the circuit, a software routine was written so that every time the DSP chip was powered up, it would send a known-frequency signal through and measure the signal coming out of the two capacitors in the Laguerre filter. Now, by some simple arithmetic, the center frequency could be calculated. Then, if the RC product could be digitally tuned, an accuracy within at least 2% could be attained.

The first approach to tune the RC product was to place the resistors into a T network and use transistors to switch sections of the circuit in and out of the network. This was possible, but the signal across the switches caused harmonic distortion in the filter, raising the total harmonic distortion above the original 0.01% goal.

The next attempt was to tune the capacitors. To do this, all of the filters had to be redesigned so that they would all have the same capacitance value. Then, the resistor values were varied to get the right RC product. This technique was successful in lowering the total harmonic distortion.

The chip, which is housed in a 40-pin plastic DIP, measures 85,000 mils^2. It was designed with a Viewlogic schematic-capture package, Metasoft's HSpice simulation tools, and a mixed digital-analog simulator called ANDI from Silvar Lisko, all running on either IBM PC/AT or Sun-3 systems.

Low-Volume Chip

A programmable gate array from Xilinx was to be used in a Memorex/Telex IBM-compatible 3270 video terminal. It was needed to upgrade an existing 6845 video-controller chip. The reason for the redesign was to add some new features to the terminal—features that make the terminal more user-friendly and give users more capabilities.

The reason a programmable gate array was chosen was because of the quick turn-around time that Xilinx could provide and also the low cost that resulted from not having any nonrecurring-engineering charges. Furthermore, because only 1200 parts were needed, this type of part could be produced in a low volume.

The design began using a schematic-capture program from Data I/O's FutureNet Div., and a library of components supplied by Xilinx. This process took one engineer about four weeks time. The FutureNet program then converted the net list to an EDIF format. Then the new net list was loaded into a Xilinx automatic place-and-route tool on an 80386-based PC. This routing, which typically takes about 45 mins., was left to run on its own for an entire evening. The following morning, the optimum route was hand chosen from all the possibilities the computer spit out (each of the possibilities includes a listing of the number of signals that did and didn't route properly).

Xilinx's editor gives the designer a blow-up model of his chip *(Fig. 4)*. With this tool, the designer can go in and locate each signal that didn't route properly and hand route it. This could be a very time-consuming affair if there are many signals to be routed, as was the case with this design. But any other changes or adjustments that had to be made were easily done in minutes using the PC-based editor.

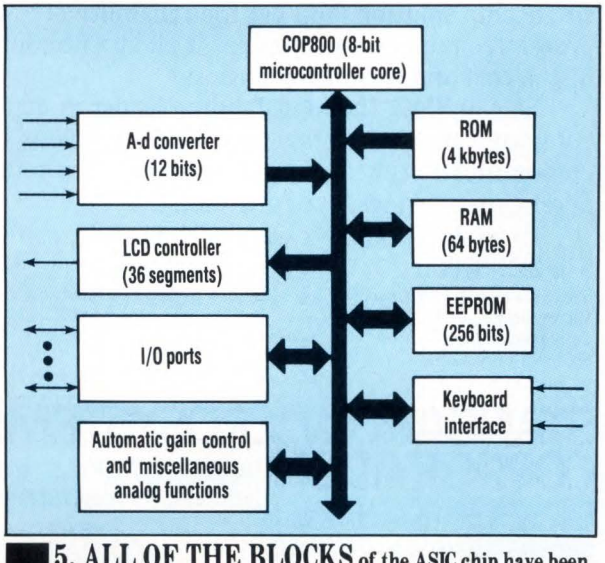
When the design was complete, there was still ample space left on the chip. Consequently, several features that weren't promised in the original proposal were added—had it not been a gate array, this wouldn't have even been attempted. The final 3000-equivalent-gate version turned out to be an 84-pin PLCC, containing 100 logic cells, with each cell adding some combinatorial logic and two flip-flops.

When placed on the board after construction, it was determined that some of the chips being shipped weren't running at the prescribed 50 MHz. To compensate, the engineer went back into the editor and rerouted some of the signals that turned out to be critical paths.

High-Powered Computing

Evans & Sutherland needed a six-chip chipset to handle most of the processing in their ES-1 supercomputer. The design team first had to decide on the architecture of the six chips and which chip would handle each part of the processing. Then they had to deal with another stumbling block: Because all of the parts were going into the same system, they all had to be completed at the same time.

The team decided on a cycle time (the slowest specification) for the computer at the onset and stuck to that specification throughout the design. To achieve this, they had to recompile and layout the design more



5. ALL OF THE BLOCKS of the ASIC chip have been upgraded: The 4-bit microcontroller became an 8-bit part while the analog-to-digital converter gained 3 bits.

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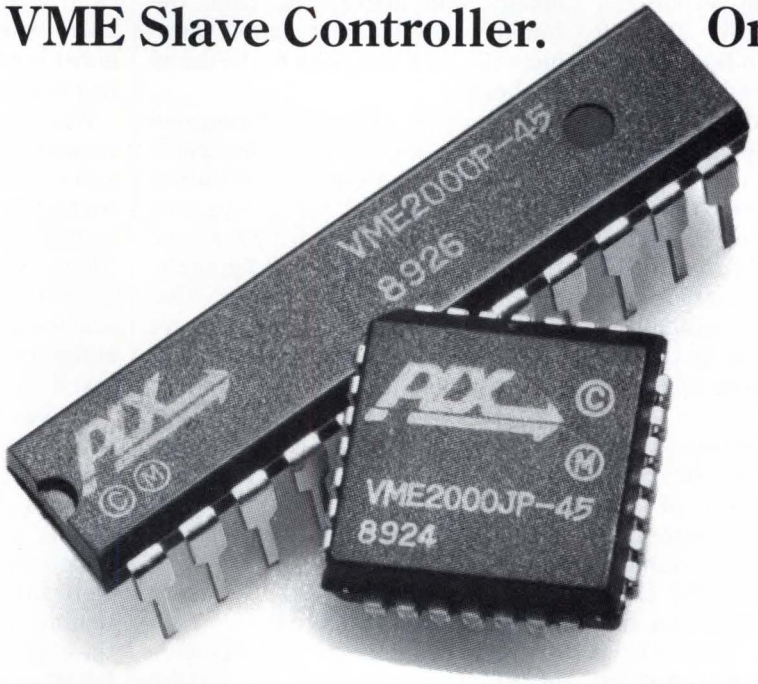

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CIRCLE 17

than 100 times.

The instruction buffer (IB), one of the six chips constructed with a CMOS technology, is measured at 525 mils on a side. It has 340 pins and contains approximately 100,000 gates. Its function is to fetch the instructions to be executed and schedule them for the processor. It's the only "intelligent" chip among the six.

The final product, which was done with 1-μm technology, was designed in a Silicon Compiler Systems (SCS) environment. One tool that was used throughout the entire process is SCS's Genesil, which can do the layout, floor planning, timing, and simulation.

This particular design was so complex that about half the time was spent on simulation. The process went as follows: First, some preliminary design was done according to the specifications. Then, the floorplanning was done. Finally, the timing was considered. These three steps became a loop that continued until completion. After the third step, the engineer went back to the beginning, did some adjusting, and continued. After each step, Genesil compiled and back-annotated the data to give the designer a complete timing report showing the critical paths, the exact speed of the chip, and the delays.

After the initial specifications were instituted, the design team went to work. But it didn't take them long to realize that their initial calculations were too aggressive as far as what could fit on one chip. As a result, after the first two months, the architecture was altered to make the existing components fit into a smaller area.

The design team considered themselves lucky having only lost two months. Time was saved by the Genesil tool, which has the ability the compile blocks of information very quickly and let the user know how much silicon is being absorbed by each block.

But the major stumbling block came when the team tried to switch from 2- to 1.25-μm technology. This was attempted for the obvious reasons of higher speed and smaller chip size. After spending the time to go to the smaller size, the designers were informed that the 1.25-μm technology was unavailable from the foundry they had anticipated working with. So it was back to the drawing board.

At this point, Evans & Sutherland decided to go with Hewlett-Packard's 1-μm technology, so more alterations were needed. "If we had done a hand layout, we couldn't have done that," notes Ed Paluch, design manager for Evans & Sutherland. "Because we were using Genesil, we switched from one foundry to another with a completely different set of design rules in a different process in a matter of weeks." Upon completion, the design team felt that they were successful in achieving their goal of making the chip "as dense as possible."

From Eight To One

A chip designed by the engineers at MIT Development Corp. (MDC), Norwalk, Conn., in conjunction with Sierra Semiconductor, San Jose, Calif., was to be used in a medical instrument that measures blood-sugar levels. The tool was made up of a circuit board containing eight ICs. The goal in this venture was to shrink all eight chips down to just one.

To achieve this, the designers took advantage of Sierra's triple technology, combining analog, digital, and EE (electrically-erasable) circuitry on the same chip. Also, a 4-bit microcontroller was replaced by an 8-bit part and a 9-bit a-d converter was upgraded to one with 12 bits. Other components of the chip included a 256-bit EEPROM, a keyboard interface, a 4-kbyte ROM, a 64-byte RAM, and a 36-segment temperature-compensated LCD driver *(Fig. 5)*.

Both teams agreed that using 2-μm double-metal CMOS technology was the way to go. First, the engineers mapped out the circuitry in the original equipment onto functions in Sierra's cell library. Extra care was taken to determine whether these "standard cells" actually fit the mold of Sierra's standard cells—those that didn't, specifically the analog parts, had to be modified. For the most part, Sierra's engineers took care of those modifications.

The new microcontroller's physical size became a problem. The engineers were resigned to putting the entire system on one chip, so they had to tackle this problem.

Sierra supplied MDC with a list of standard-cell equivalent functions and a packaged version of the microcontroller so that MDC could breadboard their own version of the chip. They also supplied a personality board used for emulating the peripheral devices. With this model, MDC's software engineers could write and test their code.

It was later discovered that the tool that creates the ROM contained a bug, so on the first pass of the chip, a useless ROM was inadvertently inserted. At that point, the engineers asked themselves whether there were any other cells in the chip functioning incorrectly. But because of the chip's design, it could be run in a ROMless mode to test the remainder of the hardware.

Later in the design, the engineers found that one of the cells—a 16-bit timer used by the microprocessor—had a slight voltage-sensitivity problem (it would lock up at levels over 5 V). By beefing up the drivers, this problem was avoided.

Sierra used their MIXsim mixed-mode simulator to perform system-level simulations. This simulator uses analog behavioral models to describe a function in terms of what it does. This is based on the relationship between the signals and their histories.

After both parties were content with the simulation, the routing was done. The microcontroller took up about 30% of the allotted space. All other components were fit in around that part. After routing, the chip was resimulated and the results were compared to those taken before the layout. The results proved favorable.□

How Valuable?	Circle
Highly	547
Moderately	548
Slightly	549

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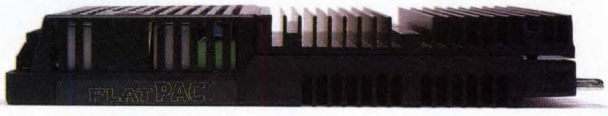

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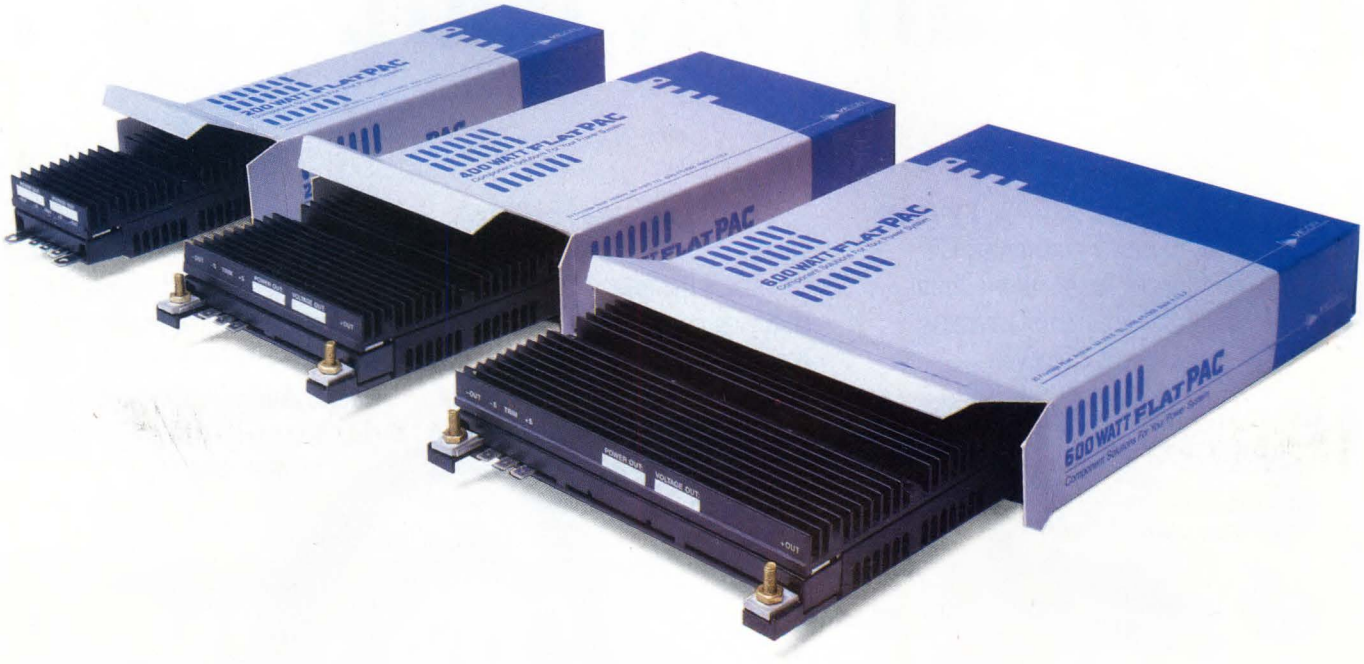

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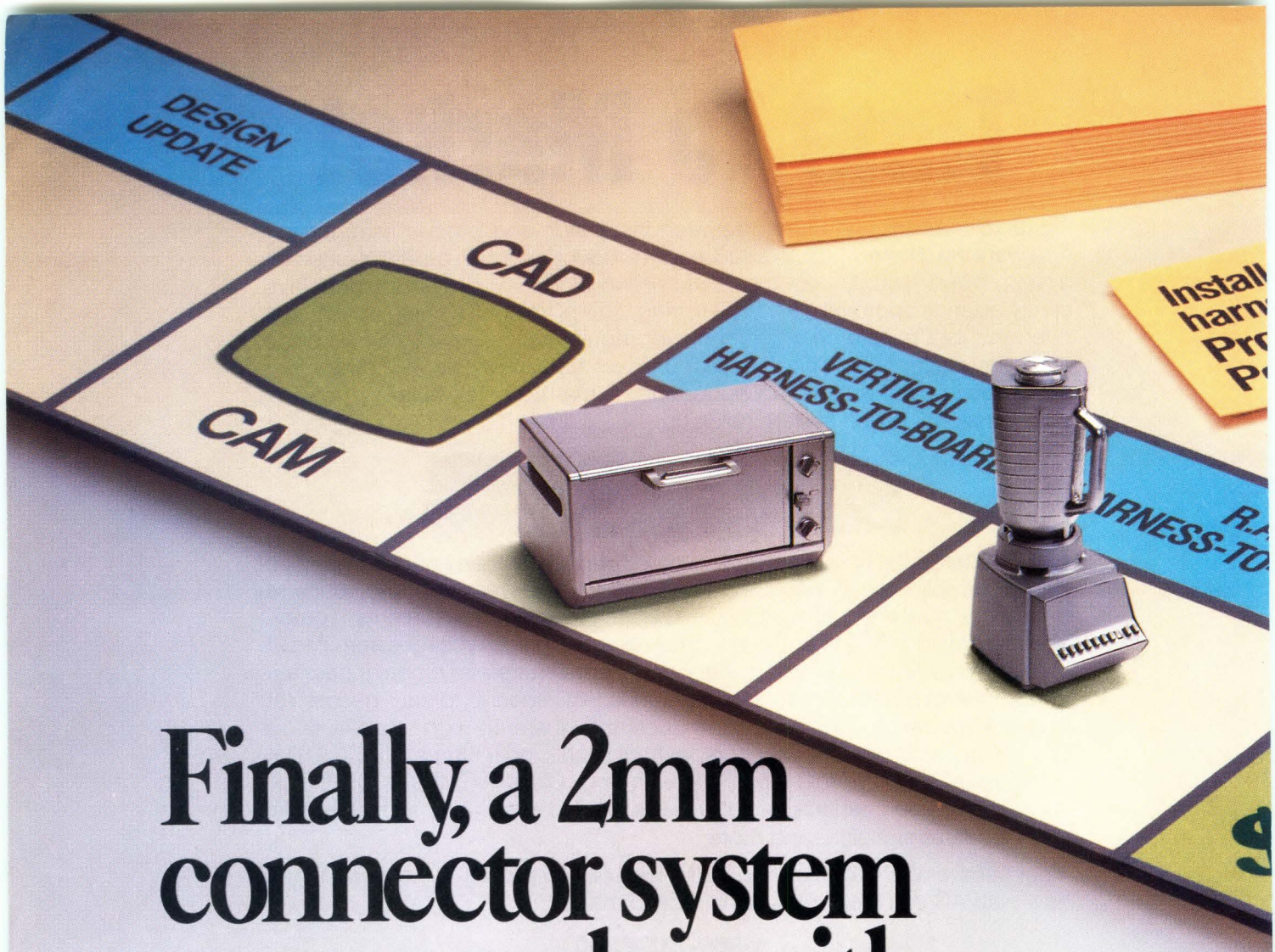

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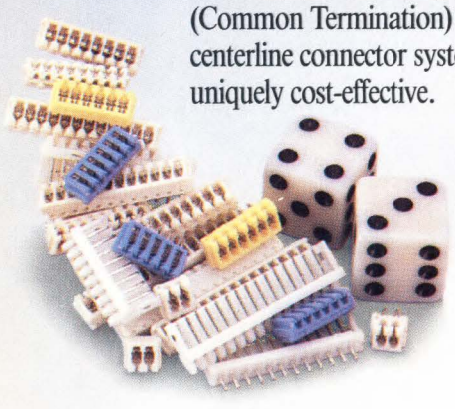

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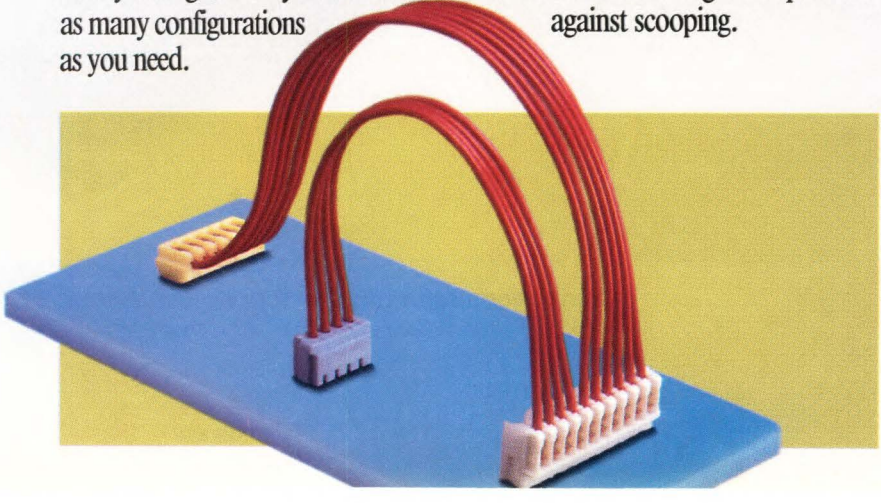

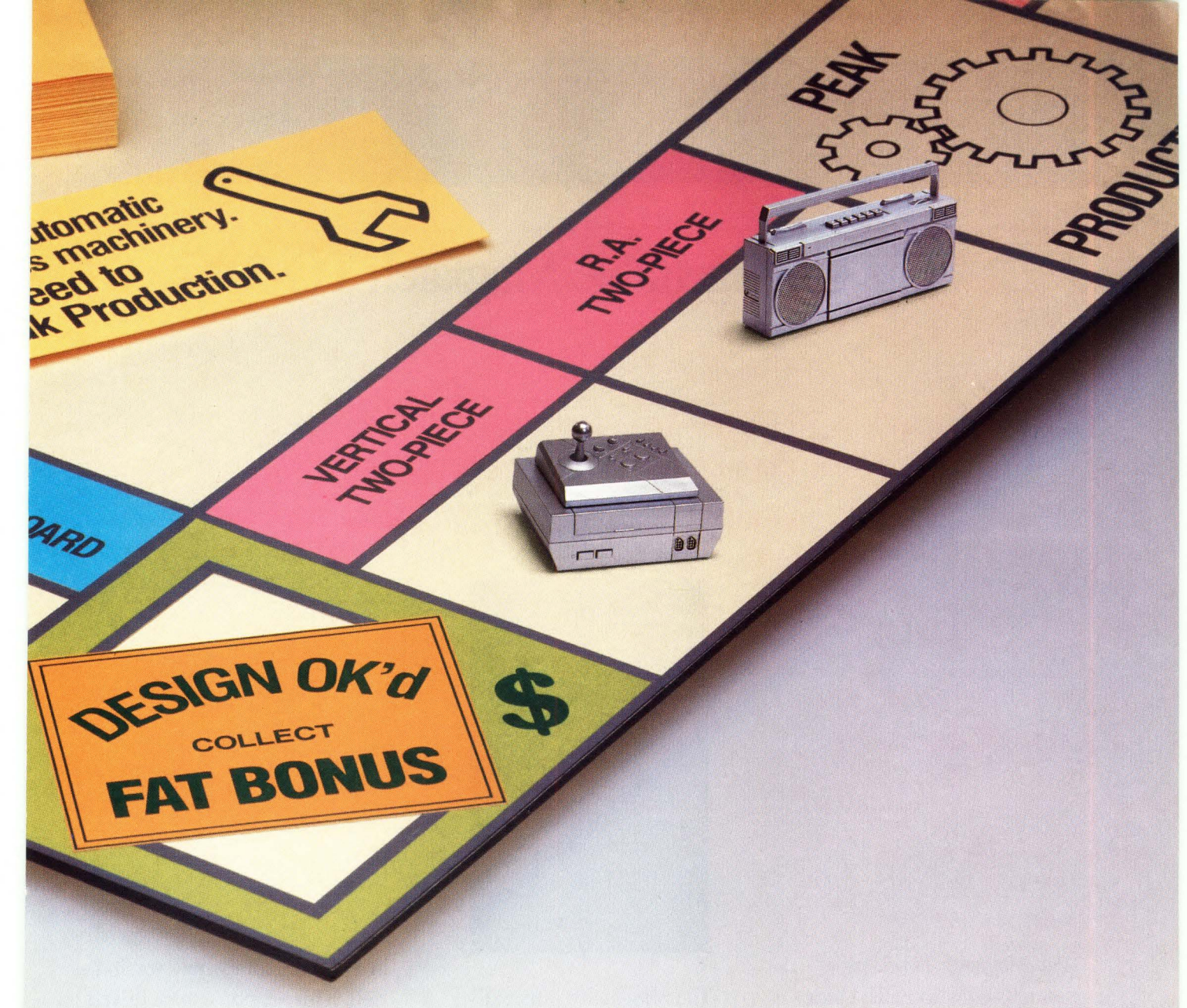

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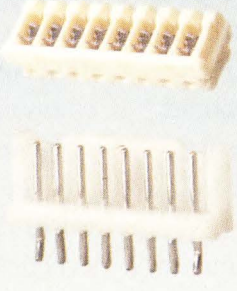

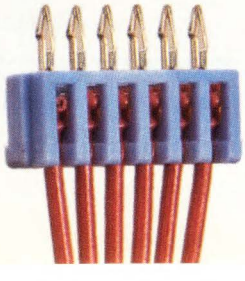

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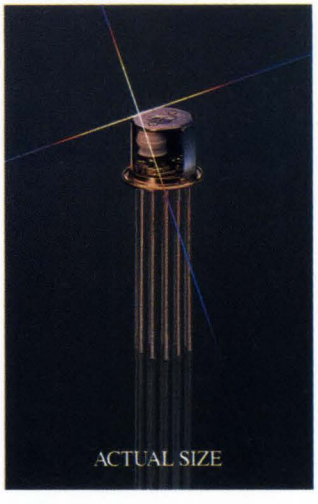

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CIRCLE 20

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SPEED SYSTEM MEMORY BY INTERLEAVING DRAM ACCESSES

DRAM PERFORMS AT SRAM SPEEDS TO KEEP UP WITH A 33-MHz 68030 RUNNING IN BURST MODE.

Matching today's microprocessors with a suitable memory system becomes a difficult and critical task because of the processors' speed. Static RAMs (SRAMs) offer the speed that's required to match the processor, but designers have to deal with cost and size problems. Most designers prefer dynamic RAMs (DRAMs) because they cost less and give higher bit density. However, DRAM can't always support a processor's fast performance, such as in a MC68030 microprocessor running at 33 MHz on burst mode. Consequently, some designers use a cache system, in which a small part of the memory is static and the rest is dynamic RAM, but this, too, adds complexity and cost to the system.

Using a column-address strobe interleaving technique with a fast-page DRAM can support a 33-MHz microprocessor in burst mode with no wait states. A system can use a 33-MHz Motorola 68030 microprocessor and 80-ns fast-page DRAM without the performance degradation that comes from slow memory *(Fig. 1)*. This design makes it possible to get data from the system memory every 30 ns, and omits the need for expensive fast static RAM or complex cache-memory technology.

The trick behind speeding DRAM accesses is to use column-address strobe interleaving while the accesses are in page mode. The DRAM is divided into two equal blocks, one for even addresses and one for odd. The $\overline{\text{CASE}}$ signal chooses column addresses for the even block and $\overline{\text{CASO}}$ chooses for the odd block. One group of column addresses strobe is active in order to access an address, while the other group of column addresses strobe goes to precharge to prepare for the next access. This technique eliminates the wait for $\overline{\text{CAS}}$ to precharge, thus satisfying the 68030's data-access time.

A processor in burst mode accesses data from sequential locations. Consequently, the next-to-be accessed address can be loaded early enough to satisfy

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FAST DRAM MEMORY SYSTEM

the column-address access time for DRAM. On a burst, the processor attempts to burst four long words, regardless of the starting location. In this example, $\overline{\text{CBACK}}$ (the burst acknowledge signal to the processor) ends the burst access at the end of the cache line, eliminating any unnecessary wraparound accesses.

The DRAM's fast-page mode can access data from the same page as fast as an SRAM can. This system uses 8 MBytes of 80-ns, fast-page dynamic RAM that's classified as 256k-by-4 bits.

A multiplexed address arrangement conserves RAM-package space. To access data, the DRAM requires 18 addresses (256 kbits). The memory system has nine multiplexed addresses and two strobe lines. A row and column of the memory array is accessed by internally latching a row address with $\overline{\text{RAS}}$ and a column address with $\overline{\text{CAS}}$.

VALID MODES

This memory system supports both interleaving and page-mode accesses. The burst runs in the fast-page mode. The system checks for a valid-page mode by examining a row-address comparator output. The comparator correlates the current row address to the last latched row address, and asserts the $\overline{\text{HSA}}$ signal if the two addresses match. If the addresses don't match, a new row address must be latched into the dynamic RAM.

A memory-system counter causes the processor to wait until the row address is strobed. The Idle signal is asserted from the memory counter to indicate that the system has finished updating the new row address to the DRAM.

A valid-page mode occurs when the Idle signal is asserted and the current $\overline{\text{RAS}}$ is kept latched active. The burst PAL device indicates a valid page if the following logic equation is true:

Valid page mode =
HSA*DRAM*Idle

The even and odd memory blocks each contain 4 Mbytes of DRAM. The processor accesses 32 bits of data from either the even or the odd block. $\overline{\text{CASO}}$ and $\overline{\text{CASE}}$ each use four $\overline{\text{CAS}}$ signals to access the 4-byte word in either the odd or even block, respectively.

During a burst, the processor transfers 32 bits of data. All four column address strobes are active. A_0 and A_1 select the byte to be accessed, and A_2 selects $\overline{\text{CASE}}$ or $\overline{\text{CASO}}$ on nonburst data transfer. If $A_2 = 0$, the even $\overline{\text{CAS}}$ ($\overline{\text{CASE}}$) is active and the even block of memory gives the data.

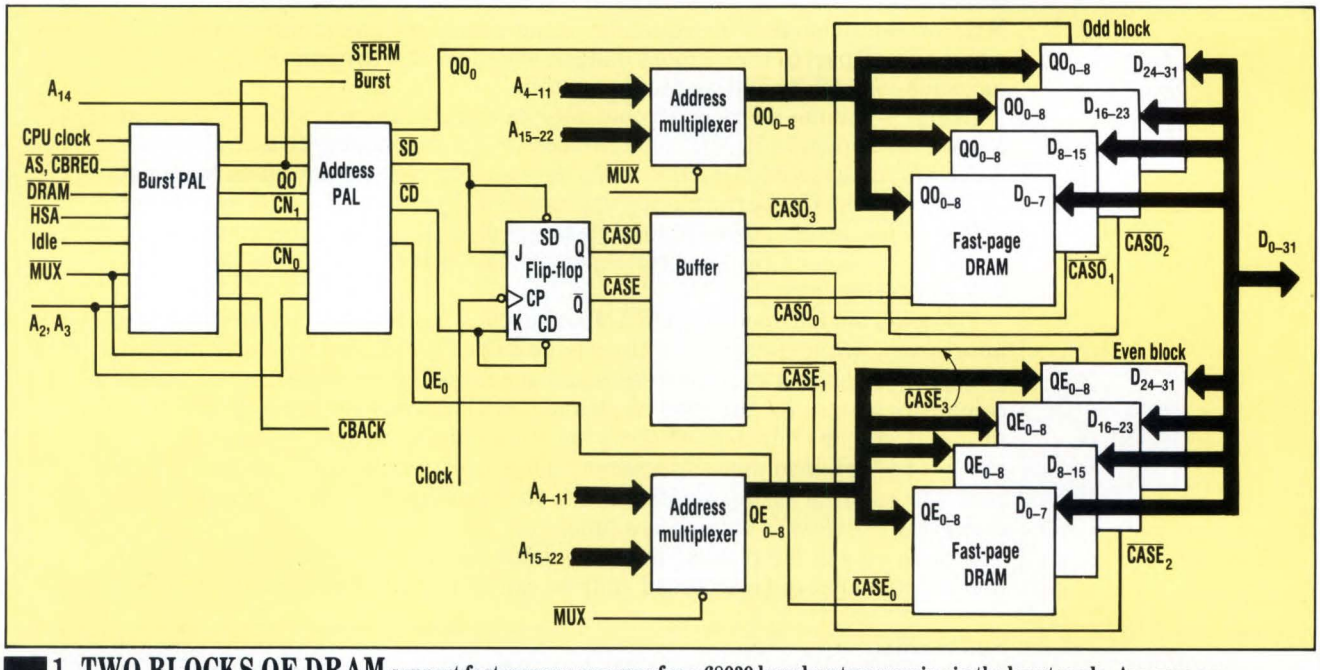
Each memory block is organized in four banks that are decoded around A_{12}; A_{13} is for $\overline{\text{RAS}}$ interleaving. The address multiplexer and address PAL units drive the DRAM row and column addresses. When the $\overline{\text{MUX}}$ signal is low, the address multiplexer outputs rows A_{15-22} and the address PAL outputs A_{14}. If the $\overline{\text{MUX}}$ signal is high, the address multiplexer outputs columns A_{4-11} and the address PAL outputs A_3.

INTERLEAVING

The J-K flip-flop toggles $\overline{\text{CASE}}$ and $\overline{\text{CASO}}$ for $\overline{\text{CAS}}$ interleaving during a burst. The address PAL device generates $\overline{\text{SD}}$ and $\overline{\text{CD}}$ from A_3 and A_2. The $\overline{\text{SD}}$ and $\overline{\text{CD}}$ signals determine group of column address strobes that should be active on the first burst access.

The burst PAL device generates the $\overline{\text{STERM}}$ and $\overline{\text{CBACK}}$ signals for the processor when it's in the burst mode. $\overline{\text{STERM}}$ is a 68030 input that's a synchronous bus-termination signal for 32-bit port size.

The design is better understood if the various signals are distin-



1. TWO BLOCKS OF DRAM support fast memory accesses for a 68030-based system running in the burst mode. Accesses are interleaved between the odd- and even-address blocks.

FAST DRAM MEMORY SYSTEM

guished. $\overline{AS}$, a 68030 output signal, indicates that the processor has a valid address. $\overline{CBREQ}$ is also a 68030 output signal, which alerts a burst request to fill the caches.

In the DRAM controller, the $\overline{DRAM}$ signal is a DRAM space decode, or a decoded valid CPU address to select the DRAM. The $\overline{HSA}$ signal is a high-speed access from the row-address comparator to detect a miss. The $\overline{MUX}$ signal is the row and column addresses multiplexing signal to output DRAM addresses. The Idle signal indicates that the accessed bank has satisfied $\overline{RAS}$ precharge on a miss. Finally, CN_{0-1} are state machine signals that generate the CNT_{1-3} and $Idle_1$ states on burst.

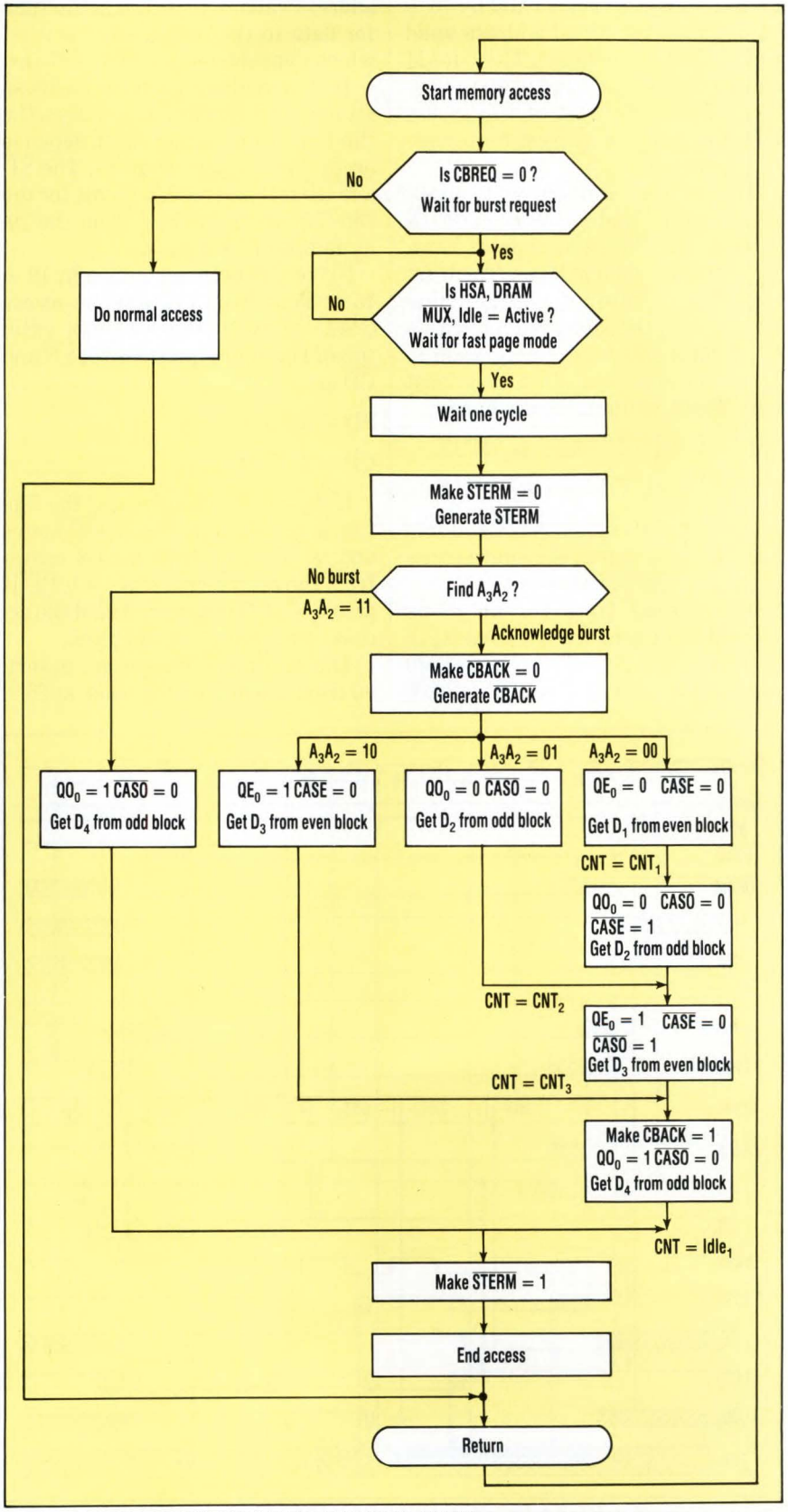
SYNCHRONOUS TIMING

The 68030 supports synchronous bus cycles terminated with a synchronous termination signal ($\overline{STERM}$). These cycles and the processor perform a minimum access time transfer in two clock periods only for 32-bit ports. Wait cycles can be inserted by delaying the assertion of $\overline{STERM}$.

The microprocessor requires that the first cycle of any burst transfer be a synchronous cycle. This cycle's exact timing is controlled by asserting $\overline{STERM}$. The system asserts $\overline{STERM}$ after the memory is in a valid fast-page mode. The system's first access on burst uses the synchronous access with one wait state and has an access time of three clock periods.

The $\overline{STERM}$ must be stable for the appropriate setup and hold times relative to every rising edge of MC68030 clock during which $\overline{AS}$ is asserted. $\overline{STERM}$ is sampled at the rising edge of S2. If one wait state (SW) is added, S2 will occur at 60 ns from the start of access (S0 rising edge). By the falling edge of this clock that occurs at 75 ns, the data must be ready and it should satisfy the setup and the hold time.

A synchronous access basically has two functions: getting the DRAM address and generating the column address strobes. To get the address, the $\overline{MUX}$ signal is generated from the 68030 address with a 10-



2. THIS FLOW CHART ILLUSTRATES how the DRAM memory system first selects between a burst or non-burst access, and then how it actually carries out the access.

FAST DRAM MEMORY SYSTEM

ns PAL delay, which is valid by 15 + 10 = 25 ns (the 68030 address valid time + PAL time delay). The DRAM column address is valid at 25 + 10 = 35 ns from the start of the access ($\overline{MUX}$ asserted + address multiplexer time delay).

The address buffers will output eight column addresses when $\overline{MUX}$ is asserted. The eight address lines, A_{4-11}, will be valid in 35 ns. The least significant column address line comes from the address PAL with a 10-ns PAL delay, becoming valid in 35 ns. The logic equation for the least significant column address line is:

$$QO_0 = A_3{}^*\overline{MUX}{}^*Idle + A_{14}{}^*MUX$$

$$QE_0 = A_3{}^*\overline{MUX}{}^*Idle + A_{14}{}^*MUX$$

On fast-page mode, $\overline{MUX}$ and Idle are true. Therefore, the above equations give $QE_0 = QO_0 = A_3$.

The access time for an 80-ns DRAM column address is 40 ns (t_{AA}). The data will be valid on the 68030 data bus in 35 + 40 = 75 ns (DRAM address valid + t_{AA}). The setup time for data to the falling edge is 0 ns, which guarantees valid data in 75 ns.

In generating column address strobes on a synchronous access, the flip-flop being set or reset depends on the first access address. The $\overline{SD}$ and $\overline{CD}$ (set and reset) signals for the flip-flop are generated from the 10-ns address PAL device.

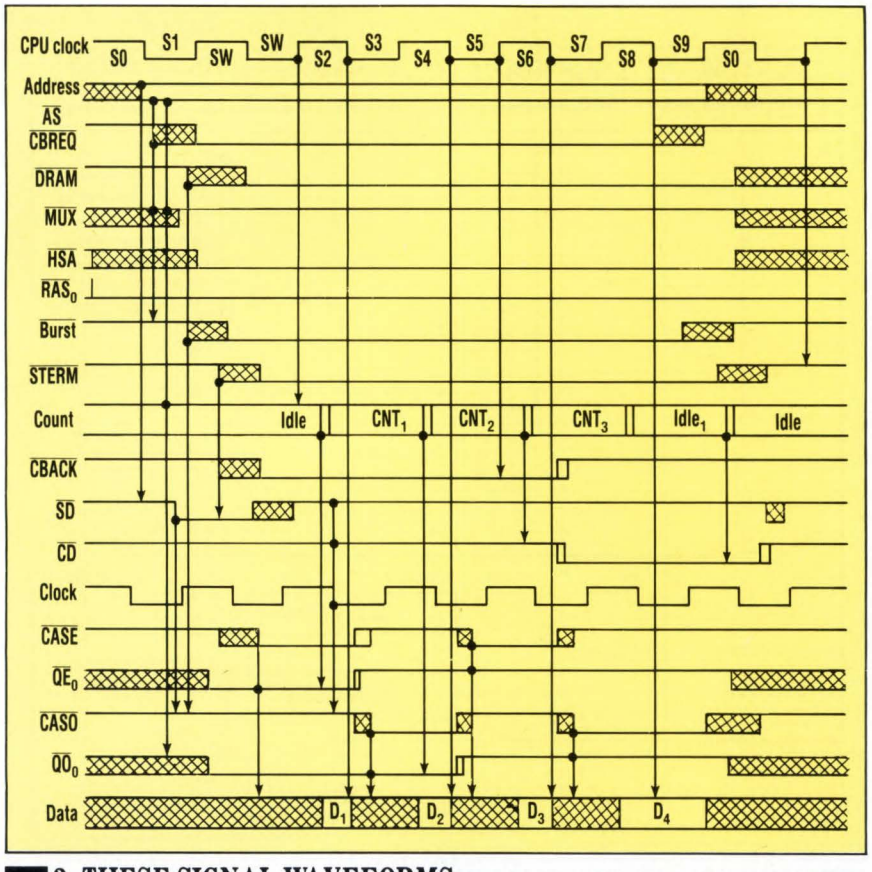
$\overline{SD}$ or $\overline{CD}$ becomes active at 10 + 15 = 25 ns from the start of access (PAL delay + the address valid time). The logic equations for $\overline{SD}$ and $\overline{CD}$ are:

$$SD = \overline{A}_2{}^*Idle$$

$$CD = A_2{}^*Idle$$

If $A_2 = 0$, $\overline{SD}$ is active and the flip-flop is set. This makes $\overline{CASE}$ active and in turn the first access comes from the even block. If $A_2 = 1$, $\overline{CD}$ is active, $\overline{CASO}$ is asserted, and the access comes from the odd block.

The column addresses are asserted from the buffer and come at 25 + 14 = 39 ns (time of $\overline{CD}$ or $\overline{SD}$ to be acive + the delay of the buffer and the flip-flop). The access time starts when $\overline{CAS}$ goes active for the DRAM (t_{CAC} = 20 ns). The data will be valid in 75 ns because 59 ns (t_{CAC} + column address strobe asserted = 59 ns) is smaller than 75 ns (t_{AA} + DRAM address valid = 75 ns).



3. THESE SIGNAL WAVEFORMS show how memory accesses occur when the system is bursting $A_3A_2 = 00$.

BURST OPERATION

The 68030 supports burst filling of its on-board instruction and data caches. In most applications, the on-board data and instruction caches are organized with a line size of four long words. Each of the four data entries on that line have the same tag address.

Most code has a large degree of locality, which makes filling the cache useful when one entry misses. To optimize cache filling, the system doesn't allow wraparound, and caches that are located before the miss don't get filled. The processor supplies a group of handshake control signals to support the filling of the cache lines.

When a miss occurs in one of the caches, the 68030 initiates an external bus cycle to fetch the required data. The processor requests a cache burst-fill by asserting the $\overline{CBREQ}$ signal to show that the 68030 wants to fill other entries in the same cache line with successive accesses.

With the 68030, a burst can fill up to four long words. The successive data's address rolls over in address bits A_3 and A_2. The $\overline{CBREQ}$ signal may be asserted during a later bus cycle of the misaligned access' operand fetch when the remaining operand portion falls within one cache line.

The 68030 won't assert the $\overline{CBREQ}$ output during a portion of a misaligned access if the remainder of the access doesn't fall in the same cache line. This warrants the use of the fast-page mode for bursting to check for a valid page at the start of the access. The burst accesses occur in the same page because the addresses are the same except for A_3A_2, which aren't row addresses.

When the $\overline{CBACK}$ signal is asserted at the end of cycle terminated

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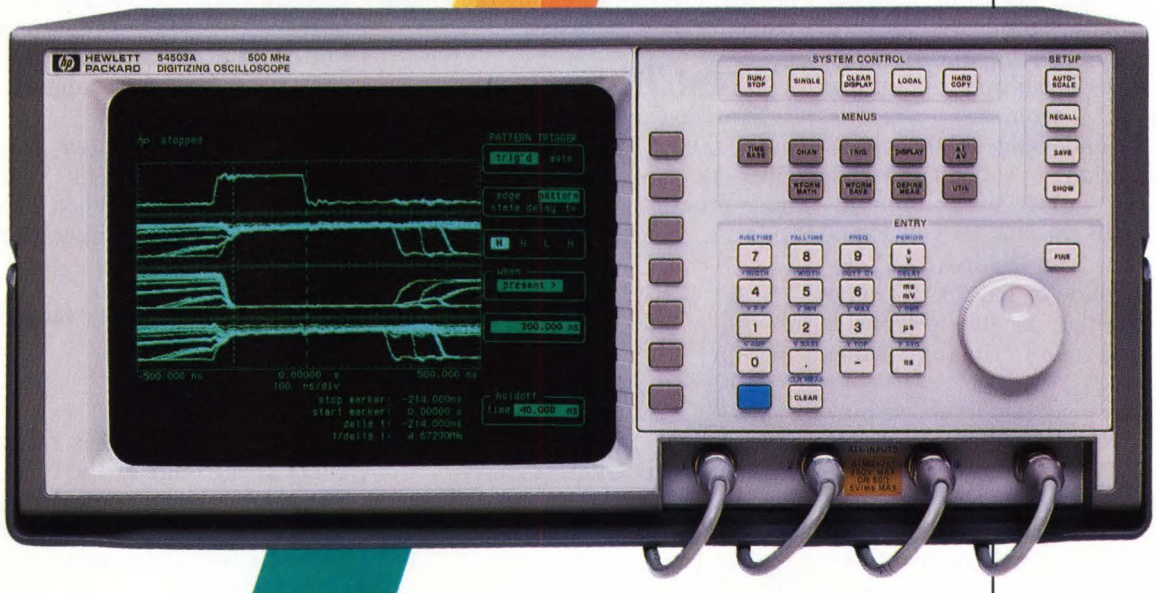

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with $\overline{STERM}$, the 68030 holds the original $\overline{AS}$, $\overline{DS}$, R/W, address, function codes, and size asserted. The processor continues to accept data on every clock where $\overline{STERM}$ is asserted until the burst is completed or terminated.

The burst system doesn't need to latch the burst's starting address because the address exists during the burst operation. Only the address buffers need to output the starting addresses by asserting the $\overline{MUX}$ signal. The address multiplexer outputs QE_{1-8} or QO_{1-8} from A_{4-11}, which is both fixed and valid on the entire burst operation.

The least significant column address bit, QE_0 or QO_0, is generated from the burst and address PAL devices. The value of QE_0 or QO_0 on a burst operation is taken from a counter that follows the same value of A_3.

The following example shows how A_2 and A_3 change on burst mode. If the initial data address is xxxx00xx when the $\overline{CBREQ}$ signal is asserted, the next address expected is xxxx01xx, then xxxx10xx, and finally xxxx11xx. The first access, which is from the even block, has $A_2 = 0$, $A_3 = 0$, and $QE_0 = 0$. The next access, which is from the odd block has $A_2 = 1$, $A_3 = 0$, and $QO_0 = 0$. The third access is from the even block and $QE_0 = 1$, and the last access is from the odd block and $QO_0 = 1$.

The value of the least significant column address bit is obtained from the address PAL device as:

$$QO_0 = QO * CNT_1$$

QO is an output from the state counter of the burst PAL chip. The value of QO depends on A_3A_2 of the first access.

The value of QE_0 in burst is always equal to one. The first access, which must have $QE_0 = 0$, is done as a synchronous access from the address PAL device. The next access is from the odd block—QE_0 is unaffected by it. At the third access, QE_0 needs to be equal to one. The design is simplified by establishing $QE_0 = 1$ in all burst accesses.

The value of QO_0 needs to be zero on the second access at CNT_1 if the starting burst address $A_3A_2 = 00$. If the burst starts from an address larger than 00, the state counter starts from CNT_2 or CNT_3 and the value of QO_0 is one on all burst accesses.

The first access of the burst is a synchronous access and the assertion of $\overline{SD}$ or $\overline{CD}$ determine which $\overline{CAS}$ is asserted first. After the first access, the flip-flop enters the toggle mode for burst accesses.

CRITICAL TIMING

The flip-flop uses the clock signal's falling edge to toggle. The clock signal leads the CPU clock (the main processor clock) by a fast gate delay (3-6 ns). The flip-flop's outputs (Q and $\overline{Q}$), which are $\overline{CASO}$ and $\overline{CASE}$, come after a delay of 3-6 ns from the falling edge of clock.

ASYNCHRONOUS ACCESS HAS TWO FUNCTIONS: GETTING THE DRAM ADDRESS AND GENERATING THE CAS.

The buffer will add a delay (which equals 3-7 ns) to the $\overline{CASE}$ and $\overline{CASO}$ signals. The maximum time that the $\overline{CAS}$ takes from the falling edge of clock can be calculated by adding 6 + 6 + 7 = 19 ns (fast gate delay + flip-flop output delay + buffer delay). This maximum time from the CPU clock falling edge is 13 – 3 = 10 ns.

The dynamic RAM access time is t_{CAC} = 20 ns maximum. The data is guaranteed to be valid at 10 + 20 = 30 ns (PAL delay + t_{CAC}) from the falling edge of the CPU clock. This will be enough for a zero-ns setup time that's needed for the next CPU clock falling edge.

The column address strobes will be down for one clock cycle (which equals 30 ns), thus satisfying the $\overline{CAS}$ pulse width (t_{CAS}) of 20 ns. The $\overline{CAS}$ will be high for one clock period of 30 ns, which will satisfy the $\overline{CAS}$ precharge time t_{CP} of 10 ns.

The 68030 supports bursts only from 32-bit ports that terminate bus cycles with the $\overline{STERM}$ signal. When the 68030 asserts the burst request $\overline{CBREQ}$ output, it samples the cache burst acknowledge synchronous input $\overline{CBACK}$ at the end of the burst cycle to see if the port supports burst mode operation.

$\overline{STERM}$ is generated from the Burst signal, which is generated from $\overline{CBREQ}$ and latched valid during the whole burst operation. The equation is:

$$Burst = CBREQ^*(Valid\ fast\ page) + Burst^*AS$$

$$STERM = Burst$$

The $\overline{STERM}$ signal is sampled at every rising edge of the CPU clock. The setup and hold time for $\overline{STERM}$ can be calculated from the assertion time of $\overline{CBREQ}$ by adding two PAL delays of 20 ns.

$\overline{CBREQ}$ comes from the falling CPU clock at 15-30 ns, then the $\overline{STERM}$ asserts at (15-30) + 20 = 35-50 ns ($\overline{CBREQ}$ asserted + 2 PAL delays). The next rising of the CPU clock edge is at 60 ns, which gives 10-25 ns of setup time and also guarantees to miss the rising edge of the CPU clock at 30 ns.

The end of $\overline{STERM}$ comes from two PAL delays after $\overline{AS}$ goes false. The time will be from a rising edge of the CPU clock (15-30) + 20 = 35-50 ns ($\overline{AS}$ deasserted + two PAL delays). This end of $\overline{STERM}$ comes at 60 ns and it also misses the rising edge of the CPU clock at 30 ns.

$\overline{CBACK}$ is used in the system to terminate the burst operation at the end of the cache line at $A_3A_2 = 11$. The processor accepts data from the accesses of cycles in which $\overline{CBACK}$ is false when $\overline{STERM}$ is asserted.

The $\overline{CBACK}$ signal must be negated one cycle before the processor is needed in order to abort burst. $\overline{CBACK}$ is negated one cycle before the end of the burst on CNT_3:

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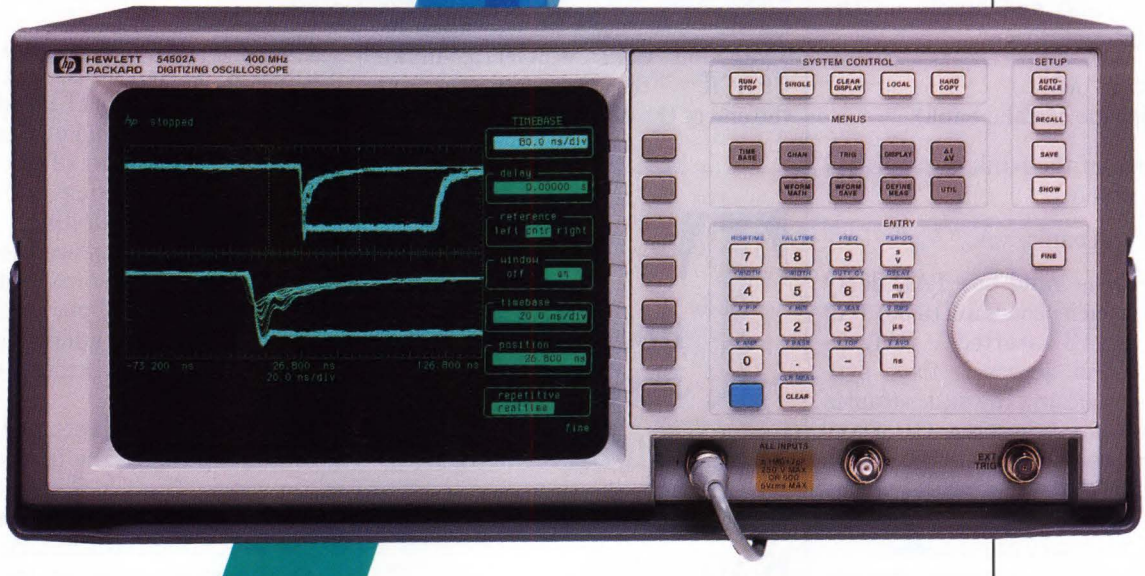

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FAST DRAM MEMORY SYSTEM

$\overline{CBACK}$ =
Burst*(Idle + CNT_1 + CNT_2)

The assertion of $\overline{CBACK}$ consists of two PAL delays from $\overline{CBREQ}$, and it satisfies the setup and hold times. It's calculated similarly to $\overline{STERM}$, which supplies the identical values.

The output enable signals to the DRAM are generated from the R/W, $\overline{AS}$, and address decoding. All of them are valid and stable on the whole burst operation:

$\overline{OE}n$ = R/W*$\overline{AS}$*
(decode of valid bank)

The decode of the bank is generated from A_{12} and A_{13}:

Decode valid $bank_0$ = $\overline{A}_{12}$*$\overline{A}_{13}$

The $\overline{OE}n$ is valid one PAL delay from $\overline{AS}$, which occurs at (15-30) + 10 = 25-40 ns ($\overline{AS}$ asserted + PAL delay). The first access is from synchronous mode and the data samples at 75 ns, satisfying the $\overline{OE}$ 80-ns DRAM access time t_{OEA} of 20 ns. On burst mode, the $\overline{OE}n$ always stay active and the $\overline{OE}$ signal satisfies the t_{OEA} time for every burst access.

For burst-mode operation, the system tests $\overline{CBREQ}$ in the start of memory access to select between burst or non-burst access *(Fig. 2)*. When $\overline{CBREQ}$ arrives, the system waits for a valid fast-page mode in the DRAM. Signals $\overline{HSA}$, $\overline{DRAM}$, $\overline{MUX}$, and Idle must be active for a valid fast-page mode.

$\overline{Burst}$ is generated when the $\overline{CBREQ}$ and the fast-page mode are active. The system waits one cycle and generates $\overline{STERM}$ to get the data by synchronous access, which takes three cycles.

If A_3 and A_2 are both high when examined, it signifies the last word in the cache line and the system doesn't support the burst mode. The $\overline{CBACK}$ signal is generated to acknowledge the burst mode if A_3A_2 isn't equal to 11.

The first access before burst (synchronous) takes three cycles. On the following accesses, the processor starts the burst and gets data during every cycle. The system handles this as follows:

- For A_3A_2 = 00, set QE_0 = 0 and $\overline{CASE}$ = 0 to get D_1 from location 00. Then, on CNT = CNT_1, set QO_0 = 0, $\overline{CASO}$ = 0, and $\overline{CASE}$ = 1 to get D_2 from location 01.

- For A_3A_2 = 01, set QO_0 = 0 and $\overline{CASO}$ = 0 to get D_2 from location 01. Then, on CNT = CNT_2, set QE_0 = 1, $\overline{CASE}$ = 0, and $\overline{CASO}$ = 1 to get D3 from location 10.

- For A_3A_2 = 10, set QE_0 = 1 and $\overline{CASE}$ = 0 to get D_3 from location 10. Then, on CNT = CNT_3, make $\overline{CBACK}$ = 1 to end the burst mode at the end of the cache line. Set QO_0 = 1, $\overline{CASO}$ = 0, and $\overline{CASE}$ = 1 to get D_4 from location 11.

- For A_3A_2 = 11, set QO_0 = 1 and $\overline{CASO}$ = 0 to get D_4 from location 11. Then, make $\overline{STERM}$ = 1 to finish the synchronous or burst access. At the end of $\overline{AS}$, finish the access.

THE FIRST ACCESS BEFORE BURST TAKES THREE CYCLES. AFTER THAT, DATA IS ACCESSED EVERY CYCLE.

WAVEFORMS, TIMING

The $\overline{Burst}$ signal goes active when $\overline{CBREQ}$, $\overline{HSA}$, $\overline{MUX}$, $\overline{AS}$ and Idle are active *(Fig. 3)*. The $\overline{STERM}$ signal is generated from $\overline{Burst}$. The processor samples $\overline{STERM}$ at the rising edge of the CPU clock of S2. The first access is synchronous with one wait state (SW1, SW2).

The burst-state counter starts from the rising edge of the CPU clock when $\overline{STERM}$ is active. When $\overline{MUX}$ is high, the address PAL chip makes QE_0 and QO_0 equal to A_3 and then loads the first address to the DRAM. QE_0 and QO_0 stay equal to A_3 until the burst counter goes to CNT_1.

$\overline{SD}$ goes active if A_2 = 0, which then activates $\overline{CASE}$ (its first access will be from the even block). $\overline{CD}$ goes active if A_2 = 1, activating $\overline{CASO}$ (its first access will be from the odd block).

Data D_1 is valid for t_{CAC} after the $\overline{CAS}$ goes active. The valid data is sampled by the falling edge of S2's CPU clock.

The $\overline{CBACK}$ is generated from $\overline{Burst}$ if A_2A_3 isn't equal to 11. The system doesn't support a burst if the cache misses at the end of the cache line. The rising edge of the CPU clock samples and requests that the processor continue bursting.

The next few cycles are the burst mode, and the processor accepts data at a rate of one word per cycle. The next least significant address is loaded from address PAL through QE_0 or QO_0 to the DRAM.

The following $\overline{CAS}$ becomes active from the flip-flop at the falling edge of the clock. The flip-flop gets in a toggle mode, and the $\overline{CAS}$ that was active will go high to precharge.

At the rising edge of the CPU clock (S4), the processor samples both the $\overline{STERM}$ and $\overline{CBACK}$ signals. On the falling edge of S4, the processor obtains the data, which creates another burst cycle.

The above task continues until the burst ends. At this point, $\overline{CBACK}$ is negated at count CNT_3 one cycle before the burst finishes. Then $\overline{CD}$ is asserted at count CNT_3 to reset the flip-flop and get the last access. That access always comes from location 11 at the end of the cache line. $\overline{STERM}$ is negated when the burst mode finishes.□

Nagi Mekhiel, a senior hardware engineer at Definicon Systems Inc., has a BSEE from the University of Assuit, Egypt, and an MSEE from the University of Toronto.

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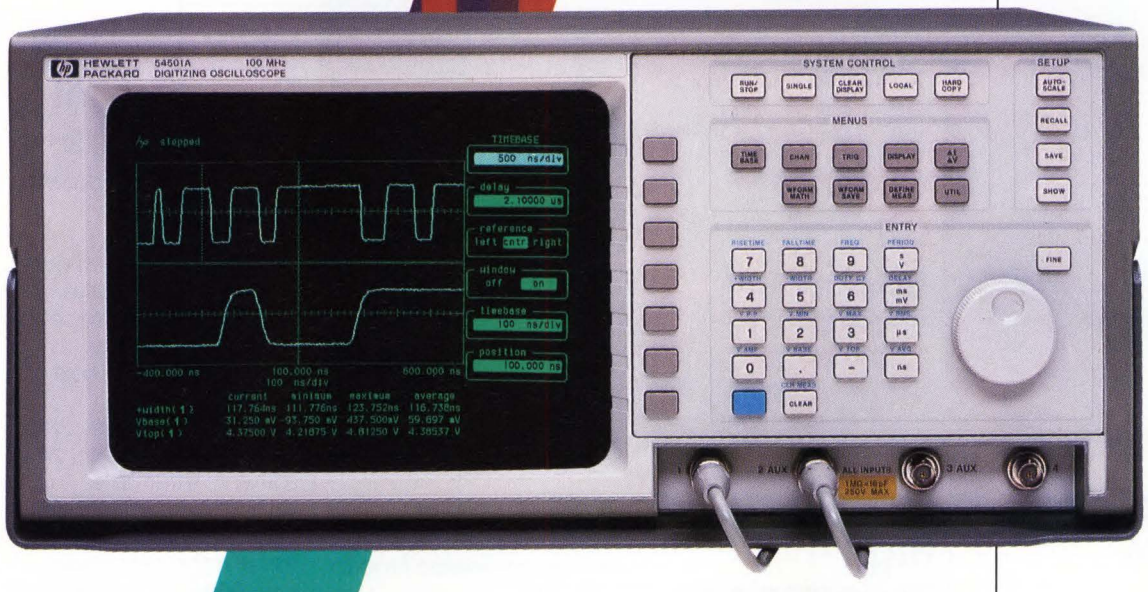

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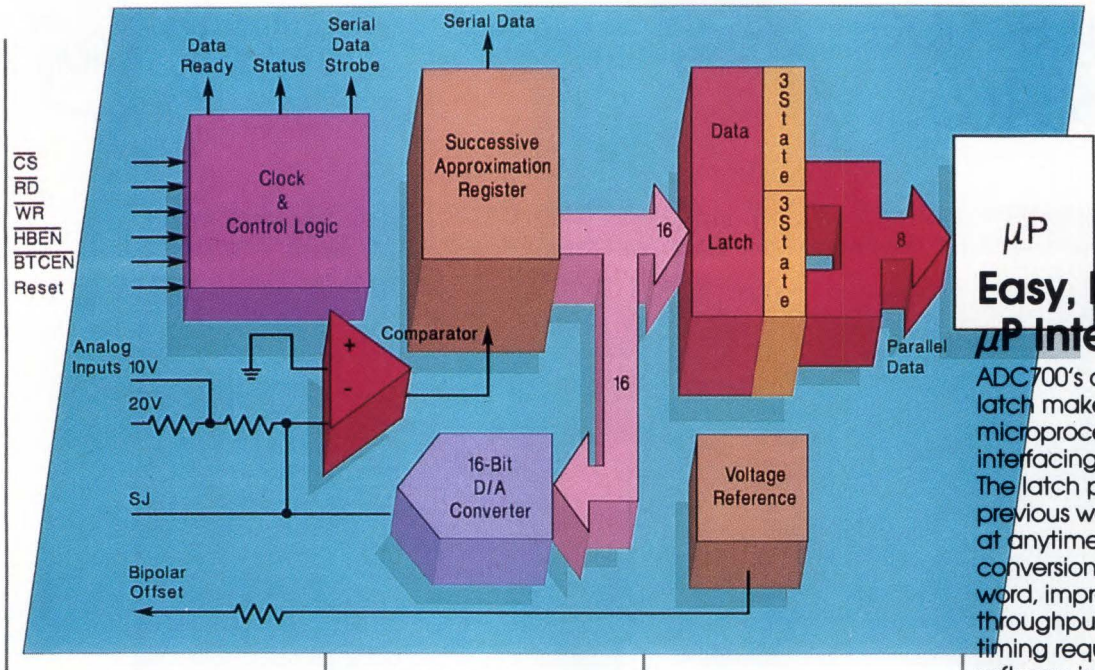

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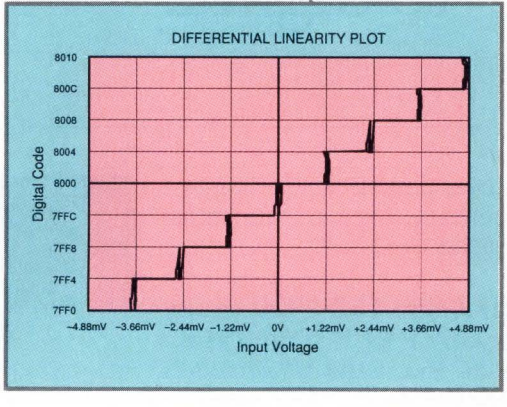

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DRIVE SAR ADCS WITH LOW-Z BUFFER

If you use successive approximation (SAR) analog-to-digital converters, you know that each time a bit-weight comparison is made, the machine's d-a converter pumps a pulse of current back into the signal source, and usually into the reference, too. If the signal source is a high impedance (more than an ohm or so), the current pulse can develop enough voltage across it to cause an error in the conversion. Your solution has been to use feedback to reduce output impedance. However, with the rise in converter speed and resolution, off-the-shelf op amps no longer have the gain-bandwidth to do the job.

In the early 8-bit, 100-μs days, the ubiquitous 741 did a fine job. But as resolution and accuracy increased to 10- and 12-bits, and conversion times dropped to 35 or so μs, you soon found you had to move to faster, more accurate op amps, such as the OP-07 and OP-27 (which are now standards). Analog Devices in particular pointed out—on every ADC data sheet—the need to use fast op amps to drive SAR converters.

Now, at the end of the decade, IC converters have reached true 16-bit accuracy and resolution while converting in under 20 μs. Sampling pulses last under a microsecond and contain significant energy above 2 MHz. In addition, the growing array of switched capacitor (charge-redistribution) converters demand a pulse of current from the signal source when they trim their sample. The now ubiquitous OP-07 and even the OP-27 just can not cut it anymore. At 10 MHz, the output impedance of both is near 60 Ω *(Fig. 1)*.

The following design procedure shows you how to create simple buffers that can supply fast-settling current pulses with little error. They have the input characteristics of precision op amps but hold their output impedance below 2.3 Ω from dc to beyond 30 MHz. In contrast, even the best wideband precision op amps show much higher output impedances above 1 MHz. Other applications for these low-output impedance buffers include flash converters, multiplexing circuits, and precision line drivers.

As an example, Crystal Semiconductor's CS-5016 16-bit switched capacitor a-d converter draws up to 10 μApk-pk at 4 MHz from both reference and signal inputs. When operating with a 4.096-V reference, the least significant bit (LSB)

JAMES A. KUZDRALL
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FAST, LOW-OUTPUT IMPEDANCE BUFFER

is just 62.5 μV. To suppress input fluctuation below 0.25 LSB (15 μV), the source impedance at 4 MHz must be less than 1.5 Ω.

For fixed references, you just strap a capacitor across the buffer's output. But for changing signals, like the a-d converter's input, that may not be practical. Available current or power may limit the ability to charge the capacitor fast. If so, it becomes impossible to sample new signals—accurately—at the a-d converter's maximum conversion rate.

The following procedure leads directly from your system specifications to component values for a production-worthy buffer. No cut-and-try iterations are needed. The output impedance of this buffer is significantly lower than that of the OP-07 and OP-27.

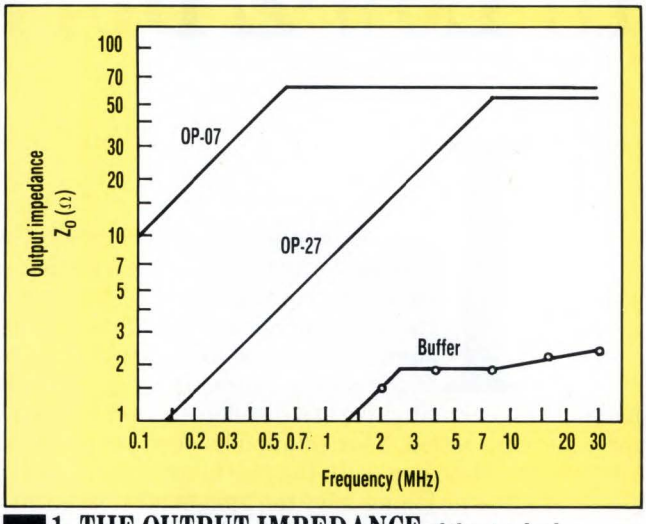
The op amp's troublesome output resistance comes from the current-limit sensing resistors in series with its output. They usually range between 6 and 60 Ω. An op amp with an open-loop dc gain of 120 dB (when operating at unity gain) cuts the 60-Ω output resistance to 60 μΩ at low frequency. However, above the op amp's unity gain frequency, usually about 1 MHz—where loop gain is gone—output resistance rises to 60 Ω.

The approach taken in the buffer design sacrifices current limit protection for an output circuit with inherently low resistance. Enclosing this circuit in a precision op amp's feedback loop supplies the needed dc performance. The combination has the new circuit's low output resistance above the op amp's unity gain frequency—and an even lower resistance below. The basic circuit is a simple cascaded, common-collector (emitter-follower) transistor stage *(Fig. 2)*.

The circuit looks simple. Indeed, if components behaved like their idealized symbols, circuit-design engineers could go home at noon every day. With real transistors, however, parasitic resistances make it difficult to achieve output resistances below 2 Ω without feedback. The design procedure identifies these resistance limits and shows how to work around them.

Fixed Voltage Buffer

To start, consider the fixed voltage buffer required between the reference and the a-d converter: Its circuit equations can later be generalized to accommodate changing voltages over a range of values. In this basic circuit, the input comes from V_{REF}. R_{REF} is the effective series resistance of the source and its resistive dividers or trim circuits.



1. THE OUTPUT IMPEDANCE of the standard precision op amps, the OP-07 and -27, while less than 1 Ω at dc, climbs rapidly reaching the neighborhood of 60 Ω above 1 MHz for the OP-07; above 10 MHz for the -27. A simple, discrete transistor buffer keeps output impedance below 3 Ω to 30 MHz.

The op amp supplies the circuit's precision performance. R_F, the feedback resistor, must match the source resistance, R_{REF}, to approximately cancel input (bias) current errors. The op amp's open-loop output resistance is shown as R_{OA}.

R_1 draws about 1 mA from the op amp to ensure that the op amp's output transistors are conducting moderately. With no current drawn, the output transistors idle at a low emitter current, reducing standby power. The small-signal output resistance of low-power op amps, such as the OP-07, can increase from 60 Ω at 1 mA of load current to as much as 600 Ω with zero load current, depending on the production tolerance of the output stage's idle current. R_1 ensures that all production units exhibit a uniform, low, open-loop output resistance in your buffer.

The buffer's output stage uses a bipolar transistor, Q_2. This is driven by an intermediate stage, Q_1, which saves power in most applications. In particular, designs requiring R_{OA} reductions by a factor of 10 or more benefit from Q_1. R_2 and R_3 set the emitter currents of their respective transistors. The unity-gain, low phase-shift, common-collector stages don't affect the op amp's loop stability. The added stages may oscillate by themselves, however, without low-impedance collector bypassing that is effective up to the transistor's unity-gain frequency, f_T (C_1 and C_2).

Begin the design with a circuit model which includes the output stage's dominant parasitic resistances. Then incorporate these parasitics in design equations that relate performance requirements directly to component values. The output resistance, R_{OQ}, of a common-collector stage is:

$$R_{OQ} = (R_{EE} + R_E) + (R_{BB} + R_B)/\text{beta} \quad \text{(Eq. 1)}$$

In the equation, R_B is the total external resistance in series with the transistor's base—usually the output resistance of the preceding transistor or op-amp stage. The transistor's current gain (beta) suppresses the effect of base resistance on the output resistance.

R_{EE} and R_{BB} are connection resistances inside the transistor package and on the die. R_E is another internal resistance—the incremental diffusion resistance. It is an inherent property of semiconductor junctions and depends on both the absolute junction temperature and the emitter current:

FAST, LOW-OUTPUT IMPEDANCE BUFFER

$$R_E = 86.25 \times 10^{-6} \times T/I_E$$

Referencing R_E to a 300K junction temperature:

$$R_E = 86.25 \times 10^{-6} \times 300/I_E = 25.9\,mV/I_E = V_R/I_E \quad \text{(Eq. 2)}$$

Of the five terms that describe R_{OQ}, three depend on the choice of transistor: R_{BB}, R_{EE}, and beta. The transistor choice will prove critical to the success of this circuit. For now, assume that transistors can be found with R_{BB} and R_{EE} low enough to contribute less than 10% to R_{OQ}. These terms can be ignored for now and brought back as a first-order correction later.

$$R_{OQ} = R_E + R_B/\text{beta} \quad \text{(Eq. 3)}$$

For betas greater than 1, the contribution of R_B can be made arbitrarily small by cascading common-collector stages. R_E can be made arbitrarily small by increasing the emitter current. Assuming that suitable transistors can be found, designers can control the buffer's output resistance without feedback.

For cascaded common-collector stages, the output resistance of the first stage becomes the input resistance for the second. The first stage emitter resistance, R_{E1}, is suppressed by Q_2's beta. The op amp's output resistance, R_{OA}, is suppressed by the product of the transistors' betas:

$$R_{OQ2} = R_{E2} + R_{B2}/\text{beta}_2 = R_{E2} + (R_{E1} + R_{B1}/\text{beta}_1)/\text{beta}_2 = R_{E2} + R_{E1}/\text{beta}_2 + R_{OA}/(\text{beta}_2 \times \text{beta}_1) \quad \text{(Eq. 4)}$$

The resistors R_2 and R_3 control the emitter currents and thereby R_{E1} and R_{E2}. Designers must decide on the best current level for each.

Though many current combinations can produce the target output resistance, there's an optimum ratio of I_{E2}/I_{E1}, n, which attains the goal with a minimum total circuit current. The most power-efficient buffer results when the second-stage emitter current is set higher than that of the first stage by the square root of the second stage's current gain. Implicit in this ratio are the assumptions that the transistor's R_{EE}, R_{BB} contribute no more than 10% to the output resistance and beta_1 is about equal to beta_2. Before the ratio can be used, however, at least one of the two currents must be determined.

EMITTER CURRENT EQUATIONS

Simple algebra relates the resistances specified by the application, R_{OA} and R_O, to the maximum allowable emitter resistances. Emitter currents replace emitter resistances and the optimum ratio eliminates one emitter current:

$$I_{E1} = I_{E2}/n = (V_{R2}/R_O) \times (1 + n/\text{beta}_2)/n = (V_{R2}/R_O) \times (1 + (\text{beta}_2)^{1/2})/\text{beta}_2 \quad \text{(Eq. 5)}$$

The output resistance of the first stage can be calculated from I_{E1}:

$$R_{OQ1} = V_{R1}/I_{E1} + R_{OA}/\text{beta}_1 \quad \text{(Eq. 6)}$$

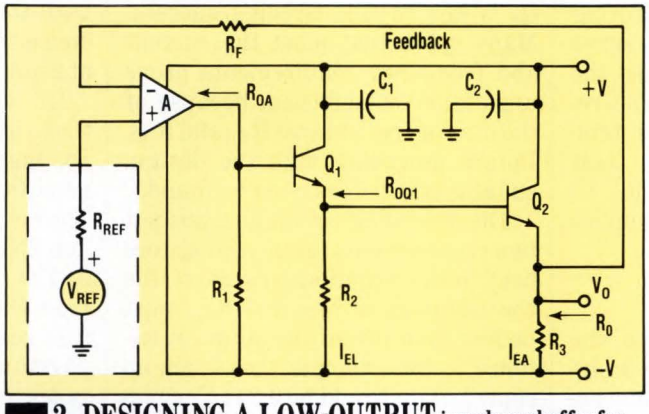
I_{E2} comes from the required output resistance, R_O, and R_{OQ1}:

$$R_O = R_{E2} + R_{OQ1}/\text{beta}_2$$

$$I_{E2} = V_{R2}/(R_O - R_{OQ1}/\text{beta}_2) \quad \text{(Eq. 7)}$$

The above equations form a convenient design sequence. The dc specifications dictate an op amp choice. The output resistance of the op amp narrows the transistor choice to those with high enough gain and low enough parasitic resistance. The transistor choice supplies parameters needed to calculate Ie1 and Ie2. These values, in turn, set the resistor values. There's a direct path between specifications and component values.

The reference buffer uses resistors to set the emitter currents of its two transistors *(Fig. 2, again)*. These currents, in turn, set the output resistance. If the buffer's input signal varies widely, as the input to most a-d converters will, the resistor's values must be set low to assure enough emitter current flows at the lowest output voltage. At the highest output voltage, the current is greater than necessary—perhaps several times greater—depending on the available supply voltage.



2. DESIGNING A LOW-OUTPUT impedance buffer for fixed voltages, such as a precision reference, seems simple. But the transistors and the op amp have some parasitic impedances that make the job tricky. For instance, R_1 draws current from the op amp to lower its zero-signal, no-load output resistance.

Replacing the resistors with simple current sources eliminates this inefficiency *(Fig. 3)*. In the circuit, transistors Q_1 and Q_2 form cascaded common-collector stages as in the fixed reference design.

As in the first circuit, the op amp supplies the precision dc performance. V_S represents the signal source with its source resistance R_S. R_3 is set equal to R_S to approximately balance bias current errors. R_4 biases the op amp's output stages at a modest current to assure a low open-loop output resistance.

The new circuit includes a noise filter, C_4 and R_5. It cuts high-frequency noise from the op amp's input without seriously affecting slew rate. R_5 becomes Q_1's source resistance at high frequencies where the op amp's output resistance is unpredictable. C_3 and C_5 filter supply noise at frequencies too high for the op amp to reject.

R_1, Q_3, and Z_2 form a current

FAST, LOW-OUTPUT IMPEDANCE BUFFER

TABLE 1: SIGNAL BUFFER SPECIFICATIONS

Environment:	Min.	Nom.	Max.	Units
Ambient temperature (at circuit card)	15°	35°	45°	C
Positive supply	14.7	15.0	15.3	V
Negative supply	−14.7	−15.0	−15.3	V
Supply noise (dc to 10 kHz)		90		μVrms
Load current fluctuation		1	10	μApk-pk
Load current frequency	0		4	MHz
Signal-voltage range	−4.1		+4.1	V
Signal source resistance		200		Ω
Performance:				
Output-voltage range	−4.1		+4.1	V
Output noise, 99.5% (1 Hz to 1 MHz)			64	μVpk-pk
Load current fluctuation error			20	μVpk-pk
Output resistance (or impedance) dc to 4 MHz			2.0	Ω
Slew and settle time (to 0.0007%, 8 V step			12	μs

source for Q_1's emitter. These parts replace R_2, of the fixed reference design. Similarly, R_2, Q_4, and Z_1 form a current source for Q_2, substituting for the original R_3. Z_1 and Z_2 serve double duty by also reducing the voltage applied to Q_1 and Q_2. This reduces the transistors' junction temperatures and consequently their emitter diffusion resistance, R_E. C_1 and C_2 bypass the collector supplies to prevent oscillation.

Design Example

This example demonstrates the design procedure by creating a signal buffer for the Crystal Semiconductor CS-5016 16-bit a-d converter. The buffer handles voltages from −4.096 to +4.096 V for the a-d converter's bipolar input range, (+4.096V reference). Assume that the buffer's input comes from a multiplexer synchronized to the a-d converter's maximum conversion rate.

The a-d converter draws up to 10 μApk-pk at 4 MHz from its signal input as it trims up the charge levels on its internal capacitors. For the bipolar range, an LSB equals 128 μV. Assume the error budget leaves 20 μVpk-pk for current-induced fluctuations after reference drift, offset drift, noise, and a-d converter errors are taken out: The buffer's output resistance must be 2 Ω or less.

The CS5016 completes a conversion cycle in about 20 μs at full speed. The input signal must be steady for 4 μs while the signal is sampled, leaving 16 μs for multiplexer switching, slewing, and settling. Arbitrarily allot a budget of 4 μs for the multiplexer to switch and 12 μs for the buffer to slew and settle *(Table 1)*.

Choosing a suitable transistor for Q_2 is key to this circuit's success. Many types that meet the current and frequency requirements prove unsuitable or inefficient because of the internal resistances R_{EE} and R_{BB}. Before preceding with the design, suitable transistors must be found.

The preceding circuit analysis put two requirements on the transistors used in the output stages. First, the contributions of R_{EE} and R_{BB} must be less than 10% of the output resistance. In this example, the maximum contribution would be 0.2 Ω. Secondly, the output resistance contributed by the op amp's R_{OA} must be less than 10%. If the betas of both stages are about equal, the minimum current gain must be:

$$\begin{aligned}\text{beta} &>= (R_{OA}/(10\% \times R_O))^{1/2}\\ &>= (55/(0.1 \times 2))^{1/2}\\ &>= 17\end{aligned}$$

But the current gain is a function of frequency. The minimum gain (beta) must be met at the highest load-current frequency (4 MHz in this example). The current gain's magnitude at any frequency, f, can be approximated from f_T and the dc current gain, beta:

$$\text{beta}(f) = \text{beta} \times f_T/(f_T + \text{beta} \times f) \quad \text{(Eq. 8)}$$

The minimum f_T which assures beta (f) is:

$$f_T = \text{beta}(f) \times \text{beta} \times f/(\text{beta} - \text{beta}(f))$$

For a dc beta on the order of 100:

$$\begin{aligned}f_T &>= 17 \times 100 \times 4\ \text{MHz}/(100 - 17)\\ &>= 82\ \text{MHz}\end{aligned}$$

Only transistors with f_T's greater than 80 MHz need to be considered for this application. This eliminates most power transistors.

From the transistors that meet the frequency criteria, designers must pick ones that also meet the R_{BB} and R_{EE} requirements. These resistances are rarely found on specification sheets. Moreover, there doesn't seem to be a reliable way to estimate them from published saturation voltages. However, an h-parameter jig that can measure h_{IB} over a range of emitter currents will give the answer. Increase the emitter current until the input resistance ($1/h_{IB}$) increases by 10% over that measured at 2 mA.

Of 20 or so transistors tested, those designed for high-voltage (80-V), high-current (1-A) switches or amplifiers best met these criteria. The best found are the 2N3725 NPN and 2N4033 PNP transistors *(Table 2)*.These transistors deviate 10% from the ideal when the emitter current reaches about 27 mA. By comparison, the 2N2222A/2N2907A types operate to 12 mA, and the 2N2369A operates to 7 mA before R_{BB} and R_{EE} contribute 10% error. Neither current rating nor saturation voltage proved to be a reliable guide in this choice. For example, the 2N3020 rated for 1-A collector current, and a 0.2-V saturation at 150 mA proved worse than the 2N2369A rated at 200-mA collector current and 0.5-V saturation at 100 mA.

Design Procedure

Before selecting components and values, it's necessary to estimate the current required in the output transistor, Q_2. This must be based on specifications alone because no parts have been chosen yet. To begin, the emitter current must reduce R_{E2} to R_O, 2 Ω in this example. To be consistent with earlier assumptions, up to 20% more current may be needed for the effects of the op amp's output resistance and Q_2's R_{BB}/R_{EE} resistances. Finally, the transistor junction won't be at 300 K. As a first ap-

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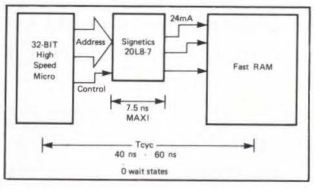

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proximation, assume Q_2's power dissipation is negligible.

$$I_{E2} = 1.2 \times V_R/R_O \times T_A\,(max)/T_{REF}$$
$$= 1.2 \times 0.026/2 \times (273+45)/300$$
$$= 17\,mA$$

Part selection begins with the op amp because its dc and noise performance are the most stringent requirements of the design. Assume that a PMI OP-27A is a suitable choice: This op amp has a nominal 55-Ω open-loop output resistance (R_{OA}) at 1 mA of output current.

A 200-Ω 5% carbon film resistor serves at R_3, matching the input signal's specified resistance. A 15-kΩ 5% carbon film resistor at R_4 maintains a minimum output current of about 1 mA.

The 2N3725 serves for Q_2. Its low R_{BB} and R_{EE} contribution leads to less emitter current and higher power efficiency. The choice being made, three key factors can be computed: the high frequency beta of Q_2, $beta_2$; the minimum high frequency beta required for Q_1; and the emitter current of Q_1:

$$beta_2 >= beta \times f_T / (f_T + beta \times f)$$
$$>= 45 \times 280 \times 10^6/ (280 \times 10^6 + 45 \times 4 \times 10^6)$$
$$>= 27$$
$$beta_1 >= (10 \times R_{OA}/R_O)/beta_2$$
$$>= (10 \times 55/2)/27$$
$$>= 10$$

From Eq. 5:

$$I_{E1} = (V_{R2}/R_O) \times (1+(beta_2)^{1/2})/beta_2$$
$$= (0.026/2) \times (1 + (27)^{1/2})/27$$
$$= 3\,mA$$

Z_1 reduces voltage on Q_1 to minimize junction heating. A rule-of-thumb advises a minimum of 2 V from collector to emitter (V_{CE}) to maintain most of a transistor's gain-bandwidth product. Z_1's voltage should be as high as possible without depriving Q_1 of its minimum voltage. Q_4 has the same V_{CE} as Q_1. The worst case occurs at the lowest output voltage, –4.1 V. Designating the negative supply as V_{SN}:

$$V_Z <= V_{SN} - V_O\,(min) + V_{BE2} - V_{CE2}\,(min)$$
$$<= -15 - (-4.1) + 0.62 - (-2)$$
$$<= -8.28 \rightarrow -8.2\,V$$

$$P_{Z1} = V_{Z1} \times I_{E1}$$
$$= 8.2V \times 0.003$$
$$= 25\,mW$$

A 1N959B, 500-mW, 5% zener diode serves for Z_1. Though the zener is tested at 15 mA, the dynamic impedance remains low over a wide current range. In this case, the maximum dynamic resistance is 6.5 Ω at 15 mA. The voltage change from the test point, 15 mA, to the operating point of this example, 3 mA, is on the order of 78 mV. Assume the nominal zener voltage is 8.1 V at 3 mA.

The low emitter current of Q_1 expands the number of transistors with negligible R_{BB} and R_{EE} contributions. Though the 2N4033 could serve, lower cost and a smaller case give the popular 2N2907A the nod. When operated at 3 mA and 2 V, V_{CE}, the 2N2907A's minimum dc beta is about 100, and its minimum f_T is about 130 MHz. The current gain at 4 MHz is:

$$beta_1\,(f) = beta \times f_T/(f_T + beta \times f)$$
$$= 100 \times 133 \times 10^6/(133 \times 10^6 + 100 \times 4 \times 10^6)$$
$$= 25$$

The power dissipation at maximum output voltage:

$$P_{Q1} = (V_O\,(max) + V_{BE2} - (V_{SN} - V_{Z1})) \times I_{E1}$$
$$= (4.1 + 0.62 - (-15 + 8.1)) \times 0.003$$
$$= 35\,mW$$

The maximum junction temperature, for a 440° C/W TO-18 case:

$$T_J <= T_A\,(max) + R_{JA} \times P_{Q1}$$
$$<= (273 + 45) + 440 \times 0.035$$
$$<= 333\,K$$

The first stage output resistance, R_{OQ1}, at 4 MHz (Eq. 6):

$$R_{OQ1} = (V_{R1}/I_{E1}) \times (T_J/T_{REF}) + R_{OA}/beta_1$$
$$= (0.026/0.003) \times (333/300) + 55/25$$
$$= 12\,\Omega$$

Z_2 minimizes Q_2's junction temperature by reducing its collector voltage. Again, a minimum collector voltage of 2 V preserves most of the transistor's gain-bandwidth product. Q_3 has the same minimum V_{CE} as Q_2. The worst case occurs at the highest output voltage, +4.1 V. Designating the positive supply as V_{SP}:

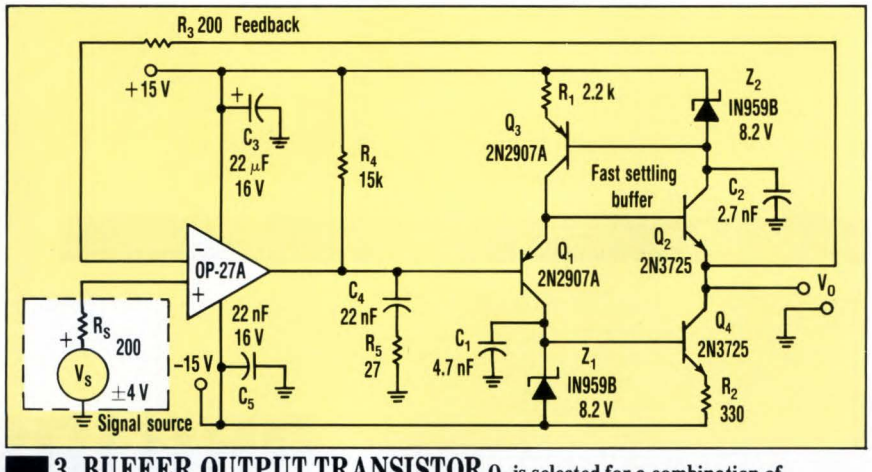
$$V_{Z2} <= V_{SP} - V_O\,(max) - V_{CE2}\,(min)$$
$$<= 15 - 4.1 - 2$$
$$<= 8.9\,V \rightarrow 8.2\,V$$

$$P_{Z2} = V_{Z2} \times I_{E2}$$
$$= 8.2 \times 0.017$$
$$= 140\,mW$$

A 1N959B 500 mW 5% zener diode serves for Z_2.

The required output stage bias current can now be calculated more precisely in preparation for selecting its current source components. First, estimate Q_2's maximum junction temperature using the estimate for I_{E2}, 17 mA:

$$P_{Q2} = I_{E2} \times (V_{SP} - V_{Z2} - V_O\,(min))$$
$$= 0.017 \times (15 - 8.2 - (-4.1))$$
$$= 185\,mW$$



3. BUFFER OUTPUT TRANSISTOR Q_2 is selected for a combination of minimum internal base and emitter resistances and maximum bandwidth—at minimum emitter current. Data sheets give little help in this selection.

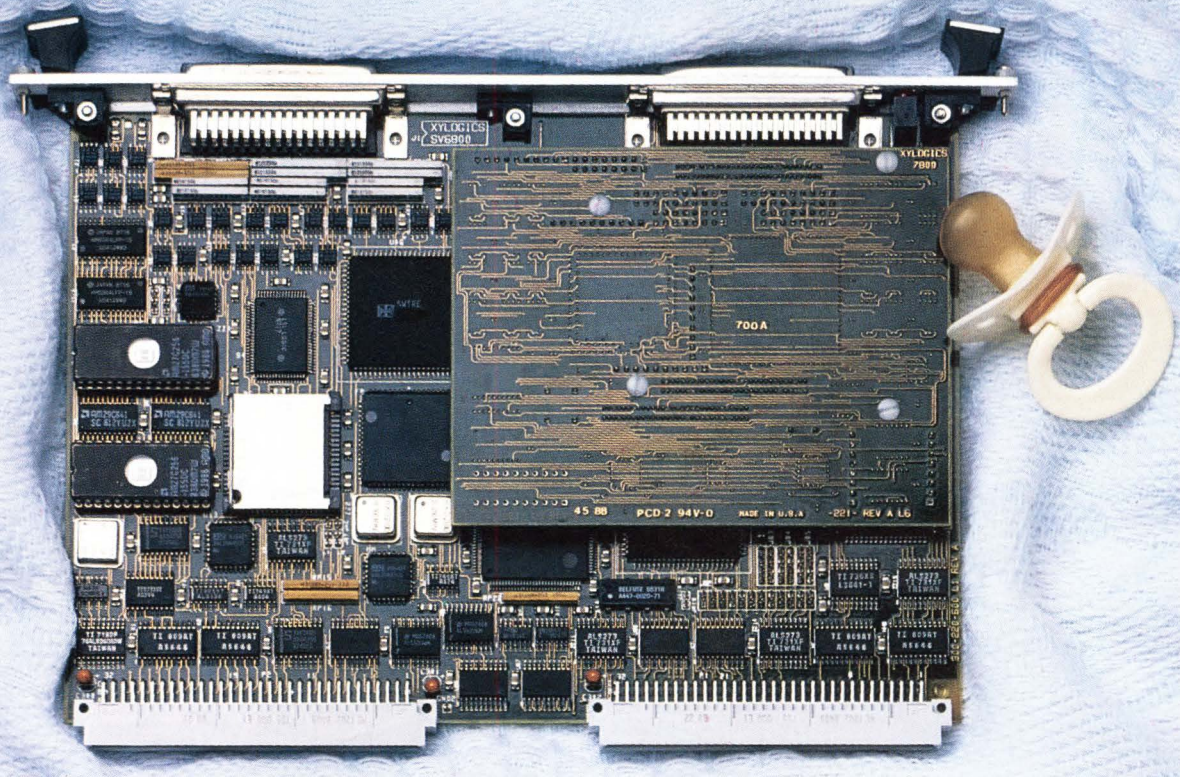


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TABLE 2: LOW REE/RBB TRANSISTORS

	2N3725			2N4033		
Parameter:	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
Unity gain frequency (f_T) (1)	280	380		130	170	MHz
Current gain (beta) (1)	45	90		100	250	
Current for 10% error in R_E (2)	25	28	31	23	26	28 mA
V_R at 300 K and I_E 2 mA		26			26	mV
Thermal resistance, junction-to-ambient		120	185		120	185 C/W
Case type		TO-39			TO-39	
Polarity		npn			pnp	

Notes: (1) Extimated for I_C = 20 mA and V_C = 5 V.
(2) 10 transistors tested

$$T_{J2} <= T_A + R_{JA2} \times P_{Q2}$$
$$<= (273 + 45) + 120 \times 0.185$$
$$<= 340\ K$$

From Eq. 7:

$$I_{E2} = V_{R2} \times (T_{J2}/T_{REF}) / (R_O - R_{OQ1}/ beta_2)$$
$$= 0.026 \times (340/300)/(2 - 12/27)$$
$$= 19\ mA$$

Recalculating the last three results with 19 mA yields:

$P_{Q2} = 207$ mW
$T_{J2} = 343$ K
$I_{E2} = 19$ mA

The circuit's symmetry makes the maximum power dissipation of the current source transistor equal that of the device it's providing current for. That is, $P_{Q4(max)} = P_{Q2(max)}$. The moderate power level of Q_4 suggests a TO-5 or TO-39 case will keep the transistor's surface temperature low. The 2N3725 turns out to be a good choice because it already appears in the circuit and happens to have excellent power transfer for its size. Power isn't a problem for Q_3, and the choice of a 2N2907A minimizes the diversity of parts.

The voltage across R_2 determines the current in Q_4 and Q_2. The relatively large value of V_{Z1} dwarfs the drifts of $Q_{4's}$ base-emitter voltage. Likewise, the zener voltage change isn't significant with the tolerances implicit in the I_{E2} calculation. Check these errors more closely for zener voltages of 5.6 V or less. A simple calculation including only the resistor and zener tolerance (tol) suffices:

$$R_2 <= (1\text{-}R_{Tol}) \times ((1\text{-}Z_{Tol}) \times V_{Z1} - V_{BE4})/I_{E2}$$
$$<= (1\text{-}0.05) \times ((1\text{-}0.05) \times 8.1 - 0.62)/0.019$$
$$<= 353 \rightarrow 330\ \Omega$$

$$P_{R2} = I_{E2} \times I_{E2} \times R_2$$
$$= 0.019 \times 0.019 \times 330$$
$$= 119\ mW$$

$$R_1 <= (1\text{-}R_{Tol}) \times ((1\text{-}Z_{Tol}) \times V_{Z2} - V_{BE3})/I_{E1}$$
$$<= (1\text{-}0.05) \times ((1\text{-}0.05) \times 8.2 - 0.61)/0.003$$
$$<= 2273 \rightarrow 2.2\ k\Omega$$

In both cases, 5% 0.25-W carbon film resistors are suitable.

The bypass capacitors are most effective if they reach series resonance just below the transistor's typical f_T, 400 MHz for the 2N3725 and 200 MHz for the 2N2907A. Using the rule of thumb that short-lead 0.1 μF ceramic capacitors resonate at 10 MHz, the proper capacitance is 4.7 nF for 200 MHz and 2.7 nF for 400 MHz resonance. The circuit layout must keep the lead inductance between the bypass point and the ground bus or ground plane on the order of 2.5 nH to 5 nH for the capacitors to work properly. Use ceramic capacitors intended for high-frequency bypass service.

C_4 forms a lag network (pole) with the op amp's output resistance and a lead network (zero) with R_5. The zero's frequency, $1/(2 \times \pi \times R_5 \times C_4)$, must be at least one decade below the normal unity gain frequency, F_{UG}, to prevent gain peaking. R_5 must be at least 22 Ω to prevent oscillations in Q_1 and Q_2. For a margin, use a 27 Ω, 5% carbon film resistor for R_5.

$$C_4 >= 1/(2 \times \pi \times R_5 \times F_{UG})$$
$$>= 1/(2 \times 3.14 \times 27 \times 5 \times 10^6)$$
$$>= 1.2\ nF$$

Though a large C_4 best suits the stability and noise goals, it must charge fast enough at the op amp's short circuit current to meet the slew rate target. Allot half of the specified 12 μs for slewing. Assume that the OP-27 can source and sink 30 mA minimum over the operation conditions.

$$C_4 <= I_{SC}/(dV/dt)$$
$$<= 0.030/(8/6 \times 10^{-6})$$
$$<= 23 \times 10^{-9} \rightarrow 22\ nF$$

The design focused on output resistance for clarity, but the output impedance will show measurable reactance above 2 MHz. A 20-mm long piece of bare wire measures 0.5-Ω inductive reactance at 4 MHz.

At 4 MHz, the hand-wired test circuit measures 1.4-Ω resistance in series with 1.25-Ω inductive reactance, for a total impedance of 1.9 Ωs. The reactance comes from layout, bypass effectiveness, and semiconductor effects. The impedance rises slowly to 2.3 Ω at 30 MHz *(Fig. 1, again.)*.

The output noise measures 8.7 μVrms or 52 μVpk-pk in a 1-MHz bandwidth (taking peak-to-peak noise as 6 times the rms calibrated average). Supply and thermal noise are minor contributors. The circuit draws about 31 mA from the 15-V supplies (930 mW). The slew and settle times are well within the 12-μs limit.

The buffer virtually eliminates load-current-induced errors for the CS-5016 16-bit a-d converter while retaining optimum offset drifts, noise levels, and slew rates. It achieves low output impedance through straightforward bias currents rather than finessed feedback. The penalty is higher power consumption; the benefit is constant, low-impedance levels into the VHF region.□

James A. Kuzdrall designs instrumentation and automated process controls at Intrel Service Co. He graduated from MIT and Northeastern University.

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Many electronic instruments and computer terminals use audible signals to supply information to users. The audio cue might accompany an error message or a request for data, or it may occur with each keystroke.

Some instruments are intended for a wide range of environments and will encounter many different ambient sound levels. Ideally, an audio signal produced by the instrument should be loud enough to be heard in the presence of ambient noise, but not so loud as to be annoying in a quiet room. Two common approaches deal with a range of ambient noise levels: Include an external loudness control on the instrument, which has the disadvantage of requiring user adjustment, or fix the amplitude of the audio cue to a level high enough to overcome any anticipated ambient sound-pressure level.

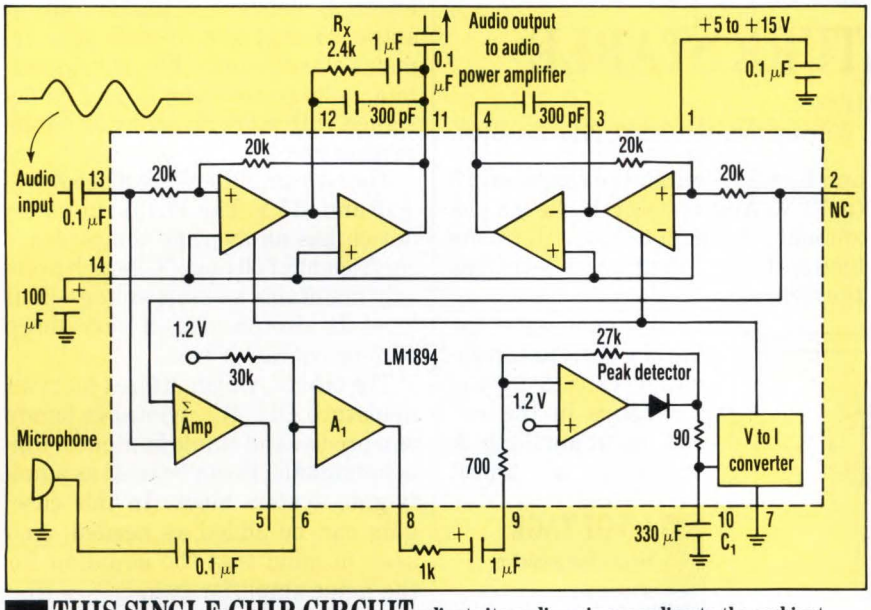
A third approach is to make the volume adjustment automatically. Ambient noise is picked up by a microphone whose output is amplified, rectified, and filtered to produce a control voltage for an amplifier (VCA). The input to VCA is the audio signal, and VCA causes the audio output to be proportional to the ambient noise. In environments with lots of ambient noise, the sound from the instrument will be loud; in quieter settings, the output will be quiet.

The entire circuit may be built with one IC, the LM1894, which is intended to implement a single-ended audio noise-reduction system. It contains a gain stage, a half-wave active rectifier, and two voltage-controlled transconductance amplifiers (one per stereo channel) *(see the figure)*. When the LM1894 is used as a noise-reduction circuit, these transconductance amplifiers are configured as low-pass filters with variable corner frequencies. In the auto-gain circuit, only one of the amplifiers is used, and it serves as a voltage-controller with a unity maximum gain and a minimum determined by R_X.

The microphone is connected to the input of amplifier, A_1, whose gain is internally fixed at 26. Its output goes to the active rectifier, which in combination with capacitor C_1 forms a slow peak detector. The coupling capacitor between the microphone amplifier and the peak detector results in a low-frequency roll-off in the detector path around 100 Hz. It may be advantageous in some systems to make this capacitor smaller so that low frequency signals are attenuated even more, because the ear is less sensitive to noise below 300 Hz than it is to noise in the 1- to 6-kHz range. If the microphone being used is too sensitive, the circuit will operate near its maximum gain even in quiet environments. But a resistive divider can attenuate the microphone's output.

What happens if the microphone picks up the acoustic output from the loudspeaker? If microphone-loudspeaker coupling is sufficient, the gain-control loop becomes a positive feedback system, and the gain will rise to its maximum value. In practice, the amount of acoustic coupling depends on the loudness of the audio signal, the locations of the microphone and loudspeaker, and on the degree of isolation from vibrations transmitted through the chassis. For example, when the microphone and loudspeaker are located on opposite sides of a computer terminal, and the microphone mounting adds vibration isolation, there shouldn't be any gain change for typical audio levels.

Alternately, if the loudspeaker and microphone are located next to each other on an instrument panel, the odds are good that there will be excessive coupling between them.□



THIS SINGLE-CHIP CIRCUIT adjusts its audio gain according to the ambient noise picked up by the microphone. When operating in a quiet environment, the audio output is quiet, while a noisy environment results in a louder audio output.

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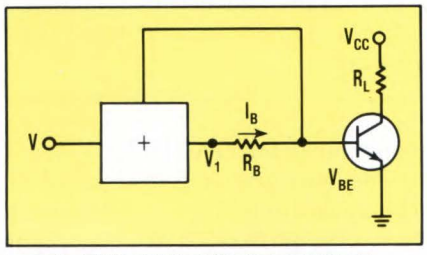
CIRCLE 522

CIRCUIT OVERCOMES V_{BE} DROP AT DC

JOSE H. RODRIGUES AND M.A.R.P. DE BARROS
Universidade Do Porto, Faculdade De Ciencias, 4000 Porto, Portugal.



1. IN THIS IMPRACTICAL circuit, the base-emitter voltage V_{BE} adds directly to the input voltage V.

When used at dc, a differential amplifier can add a voltage to overcome a transistor's base-emitter voltage drop in a transistor curve tracer design. The usual solution for a circuit to overcome this drop (0.6 V for a silicon transistor) is to add a dc bias to the signal. The signal, though, couples to the circuit through a capacitor. Accordingly, this approach becomes impractical for very low frequencies—and impossible at dc.

Consider the circuit where the base-emitter voltage V_{BE} is added to a very low-frequency or dc input signal. The following relationships can be written by simple inspection of the circuit *(Fig. 1)*.

$$V_1 = V + V_{BE} \quad (1)$$

Assuming that you can neglect the current absorbed by the feedback path, then:

$$V_1 = R_B I_B + V_{BE} \quad (2)$$

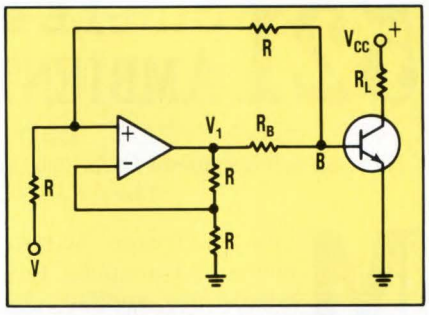
Equating expressions 1 and 2:

$$V + V_{BE} = R_B I_B + V_{BE}$$

gives

$$I_B = V/R_B \quad (3)$$

Therefore, the determination of I_B—the problem faced in the transistor curve tracer—is extremely simple, although R_B is a floating resistor.



2. A PRACTICAL CIRCUIT uses a noninverting unity-gain op-amp circuit as an adder, where the voltage V_1 equals the input voltage V plus the base-emitter voltage V_{BE}.

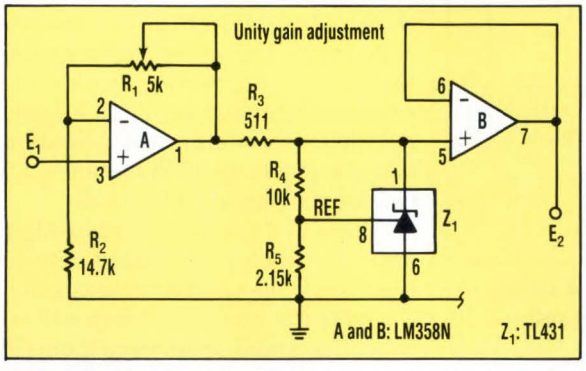
In a practical circuit that uses a noninverting unity-gain adder, the voltage V_1 equals the input voltage V plus the base-emitter voltage *(Fig. 2)*. Although the circuit has positive feedback, it remains linear for positive values of V, because the voltage at B is clamped to 0.6 V, for instance, by the transistor's forward-biased emitter diode. For negative values of V, this limitation doesn't exist, so the op amp goes into saturation. Finally, to avoid the flow of the current into the signal source, the circuit uses a large resistance (about 0.5 MΩ).□

CIRCLE 523

VOLTAGE LIMITER IS TEMPERATURE STABLE

PAUL GALLUZZI
Dynamics Research Corp., 60 Concord St., Wilmington, MA 01887; (617) 658-6100.

A TL431 precision zener-shunt regulator can be used as a voltage limiter for positive analog signals. The limiting level that is set by resistors R_4 and R_5 stays within the range of 2.5 to 13 V. And resistor R_3 keeps the amount of current that enters the limiter device (Z_1) at a safe level *(see the figure)*.



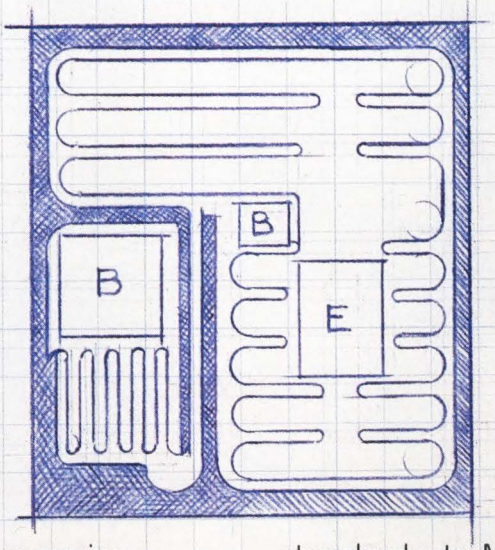
To compensate for the slight signal attenuation caused by the resistance in the circuit, input amplifier A supplies a small amount of positive gain. Voltage follower B delivers a buffer output stage so that the overall gain remains close to unity. For use in a system, voltage follower B may be designed with more inverting or noninverting gain.

A VOLTAGE limiter for positive analog signals takes advantage of a TL431 precision zener-shunt regulator.

The two amplifiers are biased with +15 and –15 V. The TL431 regulator device has an average temperature coefficient of 50 ppm/°C, which properly maintains a stable voltage-limit level. It also provides a very sharp turn-on characteristic.

The circuit, which utilizes just two miniature DIP ICs, comes in handy as a precise and stable limiter for unipolar signals. It can be used as a unity-gain system block. In this case, gain can be added as needed. And keep in mind that the equation for the input amplifier gain is $1 + (R_1/R_2)$ and the equation for the device voltage (Z_1) is $(1 + (R_4/R_5)) \times 2.495$ V (typical).□

"I NEED A DIE VENDOR THAT I CAN COUNT ON TO SUPPORT MY PRODUCTION WHEN I NEED HIM."



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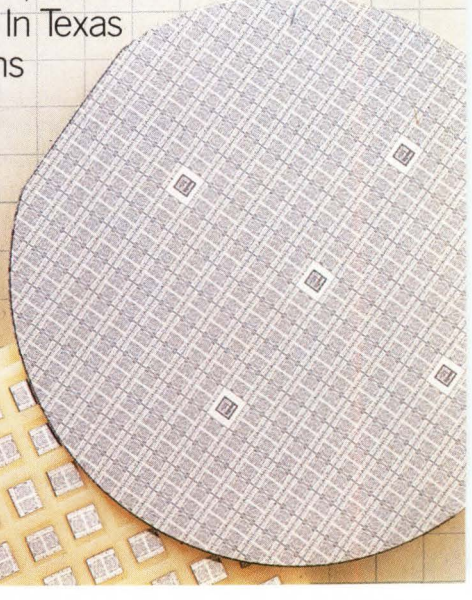

LAMBDA Semiconductors
Lambda Group of Unitech plc
121 International Boulevard, Corpus Christi, Texas 78406, FAX: (512) 289-0472

CIRCLE 54

New VR rechargeables improve performance and lower your costs.

Varta's new VR rechargeables permit improved charging rates: both trickle and overcharge. This provides new benefits: the opportunity to reduce costs by simplifying circuitry, and enhanced overcharge protection.

Cost reduction of circuitry: Until now, typical NiCd button-cell charging circuits have had two steps... charge at 0.1 CA (14-16 hours) and trickle charge at 0.01 CA (100 hours) while delivering a 5-to-6 year life. The new VR's can be used in this two-step circuitry. However, you can simplify your charging circuitry to one step, and reduce costs accordingly, by designing to both charge and trickle charge at .05 CA (only 25 hours from full discharge to full charge). The VR's will still provide 5-to-6 year life.

Improved overcharge protection. To handle user abuse or unusual conditions, the new VR's can be charged periodically at up to 0.2 CA (7-hour rate), while providing a useful life of up to six years. They can even be overcharged at 0.2 CA (room temp.) for one whole year.

VR cells are dimensionally the same size as the DK cells they replace. Initial capacities (mAh) being phased in are 60, 100, 170 and 280 (replacing the 250). Available in a wide variety of Varta battery packs and connections. For this literature on the VR series or for information on all Varta batteries, please call 1-800-431-2504, Ext. 260. Or write to Varta below.

VARTA

VARTA Batteries, Inc., 300 Executive Blvd., Elmsford, NY 10523

CIRCLE 55

COST-CUTTING CPUs TARGET CONSUMER GOODS

Based on a condensed version of the Z8 CPU core, a new family of low-cost 8-bit microcontrollers—the Z86Cxx consumer control-processor series—was released by Zilog. Aimed at cost-sensitive applications, such as consumer and automotive products, the chips will sell for $1.50 to $2.50 in 10,000-unit quantities. Chip features include operation over a wide voltage range at low current levels, on-chip analog comparators, power-on-reset timer, watchdog timer, micropower stop mode (5 μA), low emi, and a choice of an R-C, ceramic, or crystal time base. The initial family has four chips: the Z86C09, which comes in an 18-pin DIP with 2 kbytes of ROM, a 144-byte register file, and 14 I/O lines; the Z86C19, which contains double the ROM of the 86C09 but is otherwise the same; the 86C30, which comes in a 30-pin DIP and packs 4 kbytes of ROM, 256 bytes of RAM, and 24 I/O lines; and the 86C40, which comes in a 40-pin DIP and adds eight I/O lines and some memory control lines to the 86C30 features. The chips operate over a 2.5- to 5.5-V power-supply range and at clock frequencies of up to 12 MHz. Call Sam Stewart, (408) 370-8000. DB **CIRCLE 301**

SUPER CAPACITORS REPLACE BATTERIES

Designed to replace pc-mounted back-up batteries for memories and microprocessors, super capacitors from NEC Electronics, Mountain View, Calif., range in value from 0.047 to 1.5 F. All capacitors can supply 1 A or more, yet they charge quickly and discharge at rates determined by the devices they power. The capacitors operate from −40 to +70° C. Ideal for replacing lithium or NiCad batteries for short, heavy-current drains (to 1 A), the capacitors also supply long-tern backup for low drains (say 100 μA). The super capacitors also power relays, switches, and even motors. And unlike batteries, they don't need to be replaced. Prices in lots of 500 are from $2.80 each (0.047 F) to $11.77 each (1.5 F). Contact Judy Hausman, (415) 965-6121. FG **CIRCLE 302**

LOW-COST 14-BIT ADC AIMS AT PC I/O BOARDS

An integrating converter from Teledyne Semiconductor, Mountain View, Calif., offers 100-μV input sensitivity and 0.005% resolution. The TSC835 chip can supply the basic conversion needed by analog data-acquisition boards for virtually any type of PC. These boards often cost more than the computer itself. The chip's low cost also makes the converter-per-data-point system potentially affordable. While running at 5 conversions/s, the integrating converter easily ties to a UART for serial data transmission in distributed measurement applications, such as process-control systems. The chip needs just 30 mW from split 10-V rails. Packaging includes plastic and ceramic 28-pin DIPs, 44-pin PLCCs, and 44- and 60-pin plastic flat packages. Prices are just $4.48 each in quantities of 1000. Call Wes Freeman, (415) 968-9241. FG **CIRCLE 303**

70-A MOSFETs ARRIVE IN TO-247 PACKAGE

For the first time you can get a 70-A, 60-V power MOSFET in a TO-247 (plastic TO-3) package. The SMW70N06 from Siliconix, Santa Clara, Calif., which is one of six proprietary power MOSFETs, has an on-resistance of only 0.018 Ω. The SMW60N10, a second n-channel device, ups its voltage rating to 100 V, while current rating only drops to 60 A—and on-resistance rises to just 0.025 Ω. If that much performance isn't quite needed, the 60-V, 60-A SMW60N06 or 100-V, 45-A SMW45N10 might do the job: Their on-resistances run 0.023 and 0.04 Ω, respectively. A pair of p-channel devices fill out the entry: The 100-V, 20-A SMW20P10 has an on-resistance of 0.2 Ω; the 200-V, 12-A SMW12P20 features an on-resistance of 0.5 Ω. All devices are avalanche rated. In quantities of 100, prices are $7.94 to $11.44. Call (800) 554-5565, ext. 1800. FG **CIRCLE 304**

RENDERMAN EASES 3D SOFTWARE DEVELOPMENT

Creating a bridge between modeling and rendering, Developer's RenderMan from Pixar, San Rafael, Calif., is a software-development tool based on the RenderMan interface specification for 3D scene description. A model describes the shape, motion, and surface characteristics of an object to the renderer, and the renderer computes the display of the object or scene, adding light sources and other effects. Developer's RenderMan accepts various geometries or models and offers a range of rendering options, including texture mapping, anti-aliasing, motion blur, and transparency. A shading language produces such effects as environment (rain, snow, wind) and textures without adding to the database size. The Developer's RenderMan toolkit comes in Unix and MS-DOS versions, and is available now for $4650. Contact Paul Yarmolich, (415) 258-8100. LG **CIRCLE 305**

SURFACE-MOUNTED FILTERS HOLD DOWN EMISSIONS

The 601 series of surface-mounted R-C networks from Bourns Inc., Riverside, Calif., helps you control electromagnetic and rf interference from computers and peripherals. Functioning as low-pass filters, the devices feature a

T-configuration of resistors in series and capacitors bussed to a common ground. They can suppress high-frequency emi and rfi for up to eight separate lines. Packaging is a medium-body, 0.295-in.-wide small-outline style, with a choice of gull-wing or J leads. The resistance value is 50 Ω and capacitances of 50, 100, 200, and 400 pF are available. In quantities of 100, prices start at $0.95. Call (714) 781-5500. DM **CIRCLE 306**

SURFACE MOUNTING SHRINKS DC-TO-DC CONVERTERS

Low-cost, space-saving dc-to-dc converters are easier than ever to design and build, thanks to the PWS750 component system from Burr-Brown, Tucson, Ariz. A basic system consists of oscillator-driver, isolation transformer, and diode-bridge building blocks in tiny surface-mounted packages. The components can be assembled into single- or multiple-channel configurations with 15-V dc outputs and 750-V rms isolation from input to output and channel to channel. Two transformer options make operation possible from 5- or 15-V dc supplies, with output currents of 15 mA continuous and 30 mA peak. The transformers are 100% tested at 1200 V rms. In lots of 100, the oscillator-drivers cost $3.50, the isolation transformers go for $3.80, and the diode bridges cost $1.35. Delivery from stock is four weeks. Call Mark Gordon, (800) 548-6132. DM **CIRCLE 307**

DUAL VIDEO AMP SPORTS 70-MHZ, 3-DB BANDWIDTH

Designed for distributing broadcast and wider-bandwidth video signals or for driving flash converters, each channel of a dual CMOS amplifier from Maxim, Sunnyvale, Calif., supplies a 3-dB bandwidth of 50 MHz minimum (70 MHz typical) for a ±1-Vpk-pk waveform. This is achieved with a closed-loop unity gain into a 75-Ω terminated coaxial cable. Set up for a gain of 2, to retain a signal gain of 1 while driving a doubly terminated line, 3-dB bandwidth is a minimum of 35 MHz. Running from ±5-V rails, minimum output swing is ±2.1 V driving 150 Ω, and quiescent current is a maximum of 42 mA. In quantities of 100, commercial-grade versions of the MAX457 in an 8-pin DIP go for $5.00 each. Call Brian Gillings, (408) 737-7600. FG **CIRCLE 308**

DESIGN KIT LETS YOU TRY MOSFET DRIVERS

Teledyne Semiconductor, Mountain View, Calif., has a design kit for its family of CMOS ICs, which are designed to drive power MOSFETs and CCDs. These devices convert 5-V logic signals into 10- to 15-V, 1- to 6-A fast drive signals, which are required to turn on power FETs or to sample CCDs. The kit includes a pc board with sockets and connectors, a complete sampling of single and dual drivers, data sheets, capacitors for load simulation, and an instruction manual. In single units, the kit costs $39 ($65 value). Call Rich Clarke, (415) 968-9241. FG **CIRCLE 309**

ARINC 429 TX/RCVR IC ADDS BUS DRIVER

The commercial avionics industry's first one-chip ARINC 429 parallel-to-serial bus interface adds transmitter drivers and thus eliminates the existing two-chip approach. The HI-8182 chip from Holt Integrated Circuits, Irvine, Calif., directly interfaces an aircraft's avionics systems' 16-bit parallel data buses to the ARINC 429 serial bus. Receiver sampling rate is 10 times that of incoming data. The transmitter contains an 8-by-31-bit FIFO buffer, which holds up to eight ARINC words loaded from the 16-bit bus. Typical output source and sink is 125 mA from 5 and –12 V rails. The chips come in 40-pin ceramic DIPs and 44-pin J-lead chip carriers. In quantities of 100, the HI-8182 goes for $170 each. Call Bill Holt, (714) 859-8800. FG **CIRCLE 310**

DATA LOGGER SPORTS MICROFLOPPY DRIVE

With its built-in MS-DOS-compatible microfloppy drive, the 2286A data logger from John Fluke Mfg. Co., Everett, Wash., can collect up to 1.4 Mbytes of measurement data. This data can be stored in an ASCII or .DIF file format, so users can easily transfer the information to a PC for analysis on any of a number of programs, including Lotus 1-2-3, Excel, and dBase IV. Programming is performed through a front-panel keypad, and users respond to English-style prompts. The 2286A makes a wide assortment of analog and digital measurements, including dc voltage and current; ac voltage; BCD, binary, and contact closure; resistance; and frequency. Housing any of several input and output options, an extender option can be placed near the measurement point, transmitting measurements to the mainframe on a cable up to 1-km long. The 2286A will begin shipping in January with a six-week delivery schedule. Its price is $7990. Call (800) 443-5853; in Europe, contact Philips INE Export, 31-40-711-547. JN **CIRCLE 311**

EDITED BY CLIFFORD METH

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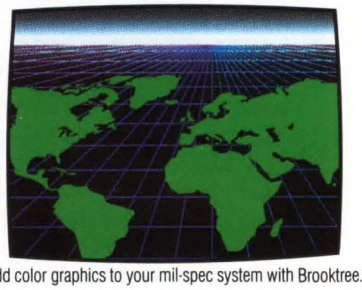

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MIL-SPEC DEVICES

DEVICE	SPEED	DESCRIPTION	PACKAGE
•Bt101SC883	30MHz	Triple VIDEODAC	40 pin Sidebraze DIP
•Bt102TC883	50MHz	Single VIDEODAC	24 pin Sidebraze DIP
•Bt438SC883	125MHz	Clock Generator	20 pin Sidebraze DIP
•Bt453SC883	40MHz	Triple RAMDAC	40 pin Sidebraze DIP
•Bt458SG883	110MHz	Triple RAMDAC	84 pin PGA

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Arium does it again!

CIRCLE 59

SETTABLE FLAGS ADD FLEXIBILITY TO FIFO ICS

SPORTING TWO PROGRAMMABLE FLAGS AND PACKING UP TO 1024 WORDS, A PAIR OF FIFO MEMORY CHIPS MAKE SYSTEMS MORE FLEXIBLE.

DAVE BURSKY

Adding new chip features is always easy when a new pinout gives access to additional control and signal lines. But for chips that drop into existing sockets, innovative control techniques must be employed for users to take advantage of new features. This is the case with a family of FIFO registers from Samsung, which offer users two independently programmable flags. The chips, however, drop into the 28-pin sockets established by previous 512-by-9-bit and 1024-by-9-bit FIFO memories.

In their unconfigured state, the KM75C101A and 75C102A CMOS FIFO registers perform just as the 75C01A and 75C02A standard 512-by-9 and 1024-by-9 chips with half-full, full, and empty (HF, F, E) flags. To access all of the superset functions, various control and signal pins on the chip serve dual or triple functions that can be invoked by applying the signals in special sequences.

Both chips have two independent and fully configurable flags—one to indicate almost full (AF) and the other to indicate almost empty (AE) *(see the figure)*. The flags are reconfigurable on-the-fly, making it possible for the system to change the flag settings depending on the application. With this feature, smart systems could adjust the flag trip points to optimize data throughput.

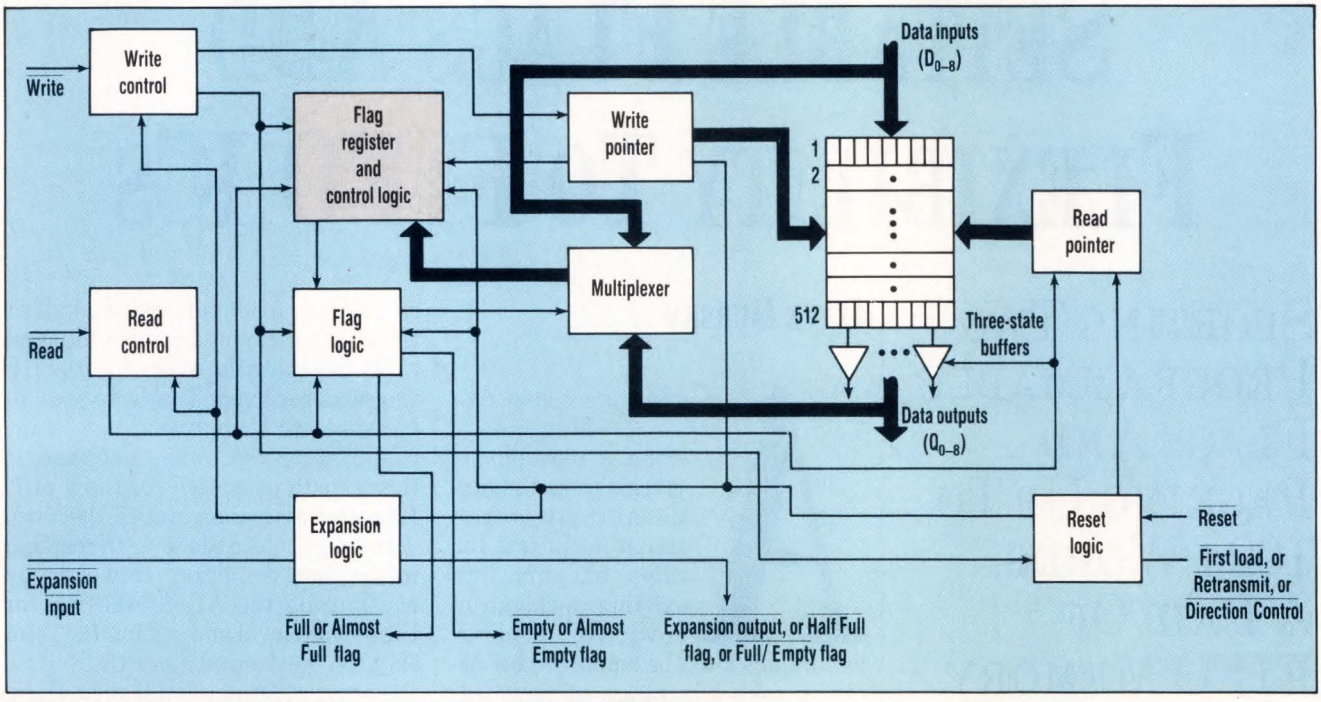
Furthermore, by adjusting the flag setpoints, the host system could be warned about pending empty or full conditions in time to invoke full service routines. Previous FIFO memories that only offered HF, F, and E flags often left unused half of the chip's memory because the host system would take over after the HF flag was received. That was done to increase the time available to slow-responding systems, because if those systems waited for the F or E flags to supply their status, the hardware might take too long to respond to the data condition. However, by configuring the AF or AE flag for the desired level and setting the third flag for the desired mode (E, F, HF), the host processor would get a warning and, in turn, the final flag. That eliminates the processor's need to keep track of how many words it requires to complete the operation.

As with other FIFO registers, address information doesn't have to be supplied to the chips—an internal ring counter generates the required addresses. Data movement into and out of the chip is controlled by the Write and Read input pins. A Retransmit pin causes the counter to recycle through the previously read locations—handy for graphics and data-communications subsystems that often need refreshing or resending of data due to noise or errors. Prior to operation, the chips should get a Reset signal to clear internal registers and reset the pointers.

The 75C101A and 102A are faster than most other FIFO memories, sporting read-write times of just 20 ns and cycle times of 30 ns. To get that speed, the chips consume a reasonable amount of power, which is about 700 mW in the active mode and 75 mW in standby.

Two internal 9-bit registers on the chips hold the flag configuration data for the AE and AF flags and for the HF or F/E flag, which is also configured on the chip. For the AE flag register, bits 0 to 5 hold an offset value and bits 6 and 7 are reserved for

FLEXIBLE FIFO REGISTERS



WITH TWO PROGRAMMABLE FLAG REGISTERS, the Samsung FIFO memories can simplify system design so users can program the flag trip points.

future use. Bit 8 is set up as a reset-locking control bit in the AE flag register and as the third flag control bit in the AF flag register.

The offset value can range from 1 to 63 words. For each offset increment, a 2-byte offset is added, yielding a 126-byte total offset range. The 2-byte increment offers a more efficient use of the host-system processor time than larger increment options (1/8, 1/4, and so forth). Furthermore, the size of the offset supplies flag output for every 126-byte (for the 512-by-9 chip) or 254-byte (for the 1024-by-9 chip) increment.

PRICE AND AVAILABILITY

The KM75C101A and 75C102A FIFO registers come in either 300- or 600-mil-wide, 28-pin DIPs or 32-lead, plastic-leaded chip carriers. In 1000-unit quantities, the 20-ns 75C101A sells for $52; the larger 75C102A goes for $63. Slower speed grades are also available. Samples are available from stock.

Samsung Semiconductor Corp., 3725 N. First St., San Jose, CA 95134-1708; Mike Shamshirian, (408) 954-7244. **CIRCLE 511**

When bit 8 of the AE flag register is low, external reset signals can reset the chip's contents. When high, the bit forces the chip to ignore subsequent reset cycles, enabling the flag registers to be reconfigured without causing the entire chip to be reset. The bit can be set low again by writing a zero into that location and then supplying a Reset signal, or the power to the chip can be temporarily removed.

The register locking capability and the on-the-fly resetability are a nice match in such data-communication applications as Ethernet. In a typical communication cycle, the first 20 bytes in an Ethernet data-transmission packet include destination address, source address, and data size. By reading the data-size value, the host processor can reprogram the AF flag. This minimizes the number of interrupts it receives because the FIFO register only needs to interrupt the processor when the entire packet is received.

The structure of the AF register is similar except that the eighth bit serves as a selection indicator for either the HF flag or the F/E flag. When set low, bit 8 sets the chip to supply a HF flag on pin 20; when set high, the bit turns that pin into a F/E flag output.

To simplify register loading over the data path, a direction (DIR) input pin makes it possible for the system to send register configuration data into the chip over either the input or output data pins. Because the main processor in many applications reads the FIFO memory, therefore having no direct connection to the FIFO register's input pins, the availability of the DIR pin eliminates the need for additional data-bus routing and external buffers. When in the register-load mode, the DIR input state determines the data-loading direction. If the DIR input state is low, configuration data are loaded through the input pins; if it's high, the data comes over the output pins. During normal operation, the DIR pin serves as either the First-Load control for multichip arrays or as the Retransmit control line.□

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

PSpice

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Available on Popular Computers, Including the New DECstation 3100

Whether your installation uses computers from Apollo, Apple, DEC, IBM, or Sun, PSpice can help your circuit designs. By maintaining consistent file formats across different platforms, PSpice insures that circuit designs, both old and new, can be simulated on all your computers.

In addition, we customize our graphics to get the best performance on each platform. Our drivers span the range from direct writing into refresh memory to higher level interfaces such as X-Windows. Since we use consistent file formats, that means that, for instance, a simulation done on a VAX 8800 can have its results viewed graphically on a Macintosh. Or, if you prefer, you can simulate on the Mac and do the viewing on the 8800.

Since its introduction over five years ago, MicroSim's PSpice has more copies sold than all other commercial SPICE programs combined. Here are some of the features which have made PSpice so popular:

- Standard parts libraries of over 2200 analog models: diodes, bipolar transistors, small-signal JFET's, power MOSFET's, opamps, voltage comparators, transformer cores, and opto-couplers.
- GaAs MESFET devices, BSIM MOS model.
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

These PSpice options are also available:

- **Digital Simulation**, which allows you to simulate mixed analog/digital circuits with feedback between the analog and digital sections. A library of 690 TTL devices is included.
- **Analog Behavioral Modeling**, which allows you to specify arbitrary transfer functions for devices, either by formula or look-up table. This can be done in both the time and frequency domains. In time domain the devices may be non-linear as well as linear.
- **Monte Carlo** analysis to calculate the effect of parameter tolerances on circuit performance. This includes statistical, sensitivity, and worst case analyses.
- **The Probe** "software oscilloscope" provides an interactive viewing environment for simulation results (see photo above).
- **The Parts** parameter extraction program, allowing you to extract a device's model parameters from data sheet information.

PSpice is available on these computers:

- The PC family (including the PS/2) running DOS, DOS with extended memory, or OS/2.
- The Macintosh II and SE30.
- The Sun 3, Sun 4, and SPARCstation families.
- The Apollo DN3000 and DN4000 workstations.
- The VAX/VMS family, including the MicroVAX.
- The DECstation family, running Ultrix.

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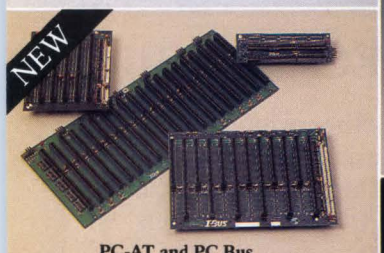
CIRCLE 60

Slim Line 4-Slot PC-AT Bus Chassis

6-Slot PC-AT Bus Expansion Chassis



NEW

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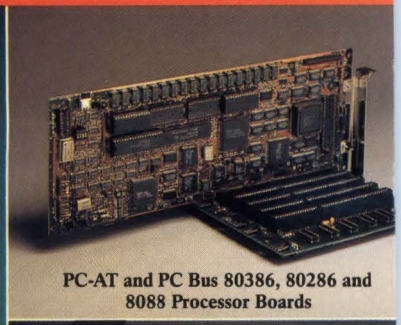
Passive Backplanes

12-Slot
PC-AT Bus Card Cage

12-Slot PC-AT Bus Chassis in Rack, Tabletop and Upright Versions



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8088 Processor Boards

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NEW

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CIRCLE 61

SIMULATOR EASES COMMUNICATION NETWORK DESIGN

WITH INTEGRATED GRAPHICS, A SIMULATOR HELPS DESIGNERS CREATE NETWORK MODELS TO ANALYZE THROUGHPUT.

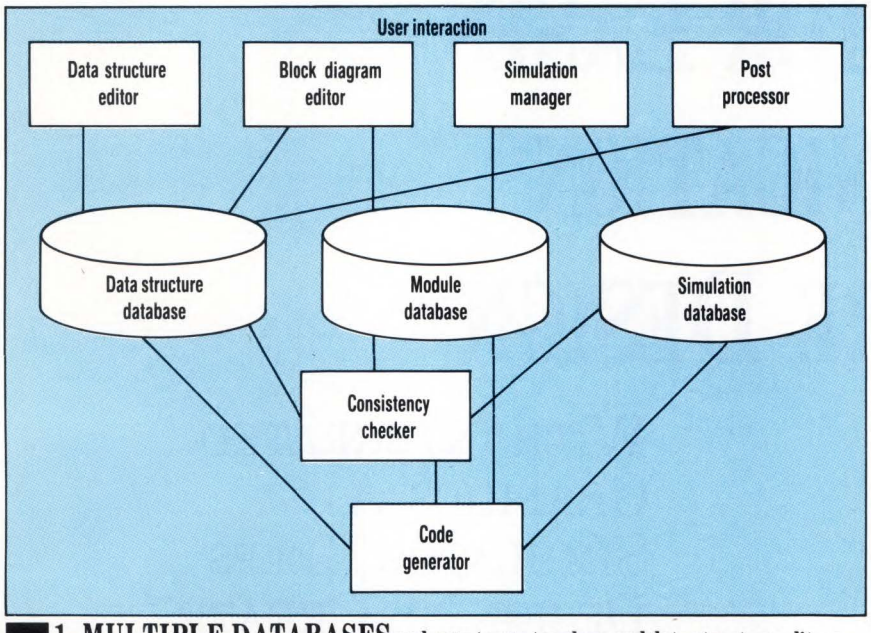
DAVE BURSKY

Network planning often means pulling out the paper and pencil to do throughput analysis or writing custom programs to simulate the network and its projected loading. Now both of these headaches can be remedied with an integrated graphical environment from Comdisco Systems that's optimized for the simulation and analysis of communication networks. The Block Oriented Network Simulator (Bones) makes an analysis job as easy as clicking a mouse, opening a window, pulling down a menu, selecting icons, and defining the parameters.

With the Bones software, designers can sketch a graphical definition of a network topology and protocol functions on the workstation screen using blocks from the built-in library or custom blocks that designers can define themselves. Once a proposed network is captured, the software incrementally compiles the system diagram into simulation code that will then be run to simulate network performance. With the integrated display and analysis tools, designers can optimize the network operation, change protocols, workloads, node types, and so forth—all without leaving the Bones environment. With on-line help, error checking and management of the databases that contain the simulation models and results, the package enables engineers to concentrate on the problem at hand, rather than on the mechanics of pulling the simulation together.

Bones will initially be available on the Sun 3 and 4 series of platforms from Sun Microsystems Inc. To execute efficiently, a minimum of about 8 Mbytes of system memory is needed (12 to 16 Mbytes preferred), along with about 208 Mbytes of disk space. For hard copy, a Postscript-compatible page printer can be driven by the program. The software also works with distributed data bases and can share models and results over a network.

Within the Bones framework, network models are structured as groups of nodes interconnected through communication links. Each node can be com-



1. MULTIPLE DATABASES and easy-to-use topology and data-structure editors make the Comdisco Bones package a simple network-simulation and analysis tool that helps designers to optimize their communication networks.

posed of one or more processors that execute various aspects of the network protocol that can even be portrayed graphically in a hierarchical block diagram. Each block represents a protocol function that accepts, processes, and outputs data structures (messages, packets, etc.).

Over 100 primitive building blocks are included in the model library that comes with Bones. Designers can easily build and save larger blocks that are hierarchical. The blocks are composed of many small blocks. Custom blocks can also be created with C-language routines and saved as new blocks in the library.

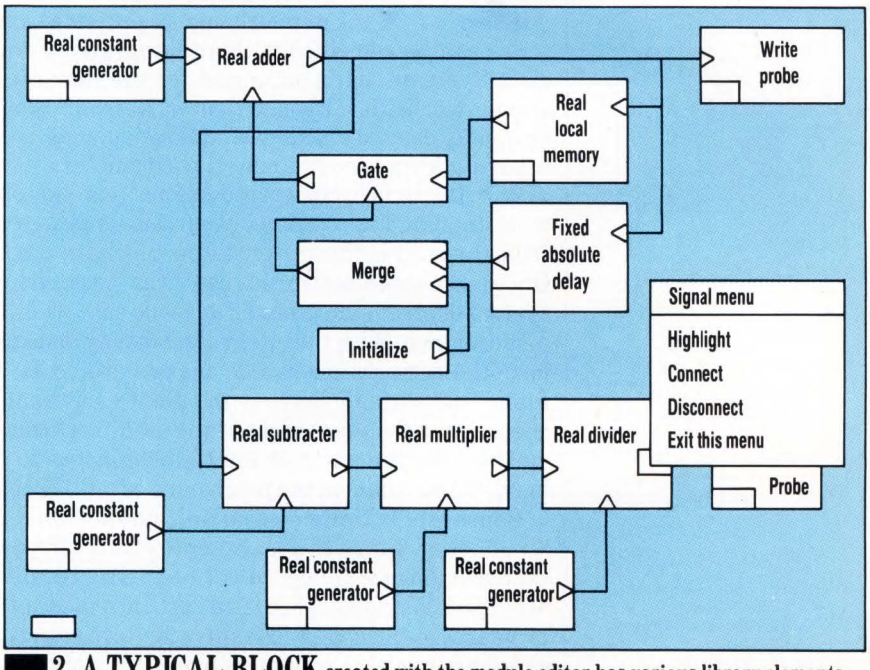
There are four major primitive modules supplied with Bones: arithmetic modules, such as adders and random number generators; timing control modules, such as initialize, absolute delay, and start timer; execution control modules, such as switches and gates; and data structure access modules, such as "create data structure" and "insert field."

From an analysis and design viewpoint, a network model consists of topology, protocol functions, and data structures. Topology specifies the location of switches and processors, their interconnections through the communication links, and the capacities of the communication links.

The rules governing the flow of data are specified in a set of protocols and data structures. To minimize design complexity, networks are organized as a series of layers or levels comparable to the ISO/OSI reference model. Each layer is built upon its predecessor (the hierarchy); the protocols are specified for layer-to-layer communication rather than for the network as a whole (example protocols include the IEEE 802.x and the X.25). Data structures specify the format of the data packets or messages that flow over a network. Each data structure typically has several fields containing headers, trailers, control, and desired data.

To measure network performance, many factors must be evaluated—throughput, connectivity, delay, line utilization, buffer occupancy, reliability, and so forth. To handle all those needs, Bones is divided into multiple databases that hold the network definition, various graphical editors that let the designer capture and customize the network description, and various other blocks that handle data consistency checks, code generation, simulation management, and post processing *(Fig. 1)*. With this environment, designers can describe data structures, protocols, layers of the ISO model, network topology, and transmission effects in a hierarchical block diagram.

The block-diagram editor helps users create, edit, document, and store the topology diagrams. With the



2. A TYPICAL BLOCK created with the module editor has various library elements, such as arithmetic elements, gates, time delays, and constant generators, interconnected to form the desired function.

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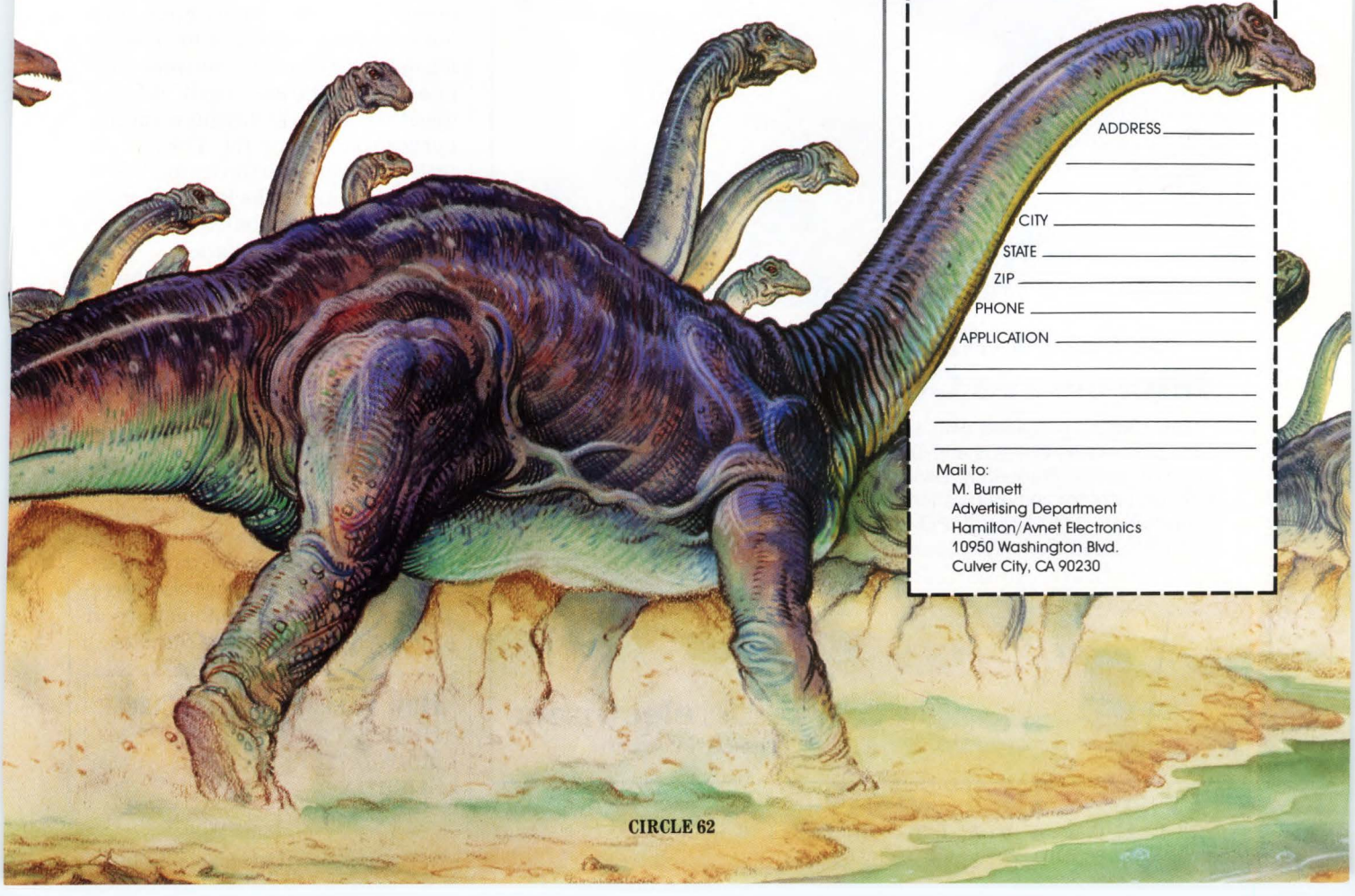

CIRCLE 62

PRICE AND AVAILABILITY

The Block-Oriented Network Simulator software sells for $20,000.

Comdisco Systems Inc., 919 E. Hillsdale Blvd., Foster City, CA 94404; Robert Grossman, (415) 358-3626. **CIRCLE 512**

data-structure editor, designers can create, edit, document, and store data structures. The code generator transparently converts the topology description into C code. A data-base manager and consistency checker organize, store, and retrieve the diagrams, data structures, simulation code and results, documentation, etc. The post processor analyzes and displays simulation results.

After capturing the model, Bones translates it into a C program and executes an event-driven simulation of the model. The various tools included in Bones enable designers to perform statistical analysis of the simulated data, extract performance measures, and display the results on the screen. With the graphical editors, changes can be made to the network topology or protocols quickly. Simulations can be rerun to try out many what-if scenarios, which makes various tradeoffs possible to optimize system performance.

Bones not only analyzes network performance prior to design, but also serves through the life of the network. Designers can analyze problems with link quality, link and node failures, and changes in protocols and data structures. Bones can also simulate error-recovery procedures.

Modeling elements at their lowest level in Bones are primitives. They perform various simple functions that include extracting and modifying a field in a data structure. Primitives are grouped and connected to form higher-level blocks, such as protocol functions (these protocol blocks can easily represent ISO model layers, for example). These higher-level blocks can again be grouped and interconnected to form processors. Another repeat of this procedure groups the processor blocks and interconnects them to simulate networks. The number of hierarchical levels is virtually unlimited, so designers can organize a model for clarity without arbitrary limits.

A typical simple block diagram drawn on the screen might consist of several constant generators, a gate block, arithmetic elements, and other functions *(Fig. 2)*. Behind each element are additional data that define the operation of each function.

Nodes are defined as collections of one or more processors that are physically co-located. A processor is a collection of tasks that share memory. Each processor is simulated with its own event calendar. According to Dr. Sam Shanmugan, senior vice president of technology at Comdisco Systems, the use of this approach does two things. First, it allows accurate modeling of processing delays and enables network engineers to address such what-if questions as "will buying a special-purpose processor for TCP/IP improve network performance?" Second, it facilitates the use of parallel processing or distributed processors to accelerate the simulation.

Prior to executing the simulation, Bones performs various error and consistency checks. Traffic rates, buffer sizes, transmission rates, and other parameters can be assigned to each node. Moreover, "probes" can be attached to any point on the model where designers would prefer to observe and collect data. Two libraries are part of the basic software package—one for protocol elements and functions, the other for data structures. Additional libraries can be created by users from combinations of primitives or from C-code routines.□

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

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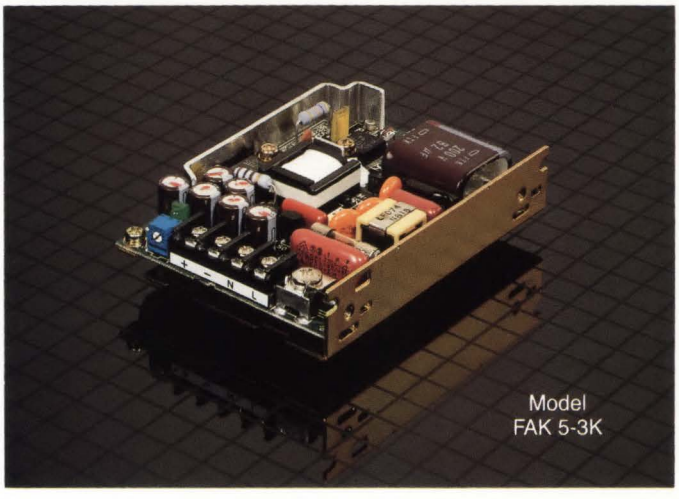
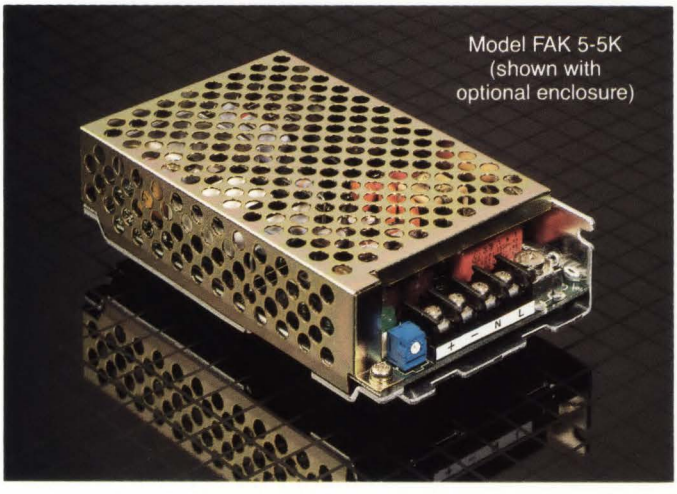
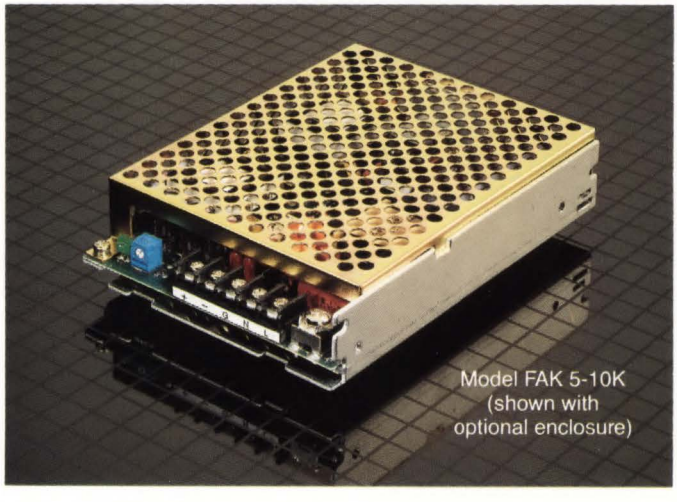
15 WATT



25 WATT



50 WATT



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FAW MODEL TABLE

SPECIFICATION	OUTPUT VOLTAGE		OVP SETTING	OUTPUT CURRENT	CURRENT LIMIT (3)	RIPPLE				NOISE (SPIKE) (4)
Unit	Volts		Volts	Amps	Amps	mV p-p		mV p-p		mV p-p
Condition	Factory Set (1)	Adjustment range	Fixed within range	0 - 50°C (2)	Fixed within range Nom Input 25°C	Source frequency		Switching frequency		d-c to 50 MHz
			Reset: a-c off: 60 sec			typ	max	typ	max	max
15 WATT MODELS	Size: Open 0.98 x 3.94 x 3.94 in. Enclosed (CA 24) 1.18 x 3.94 x 3 .94 in. Net wt. 9.52 oz, 270 gm 25 x 100 x 100 mm 30 x 100 x 100 mm									
FAW 5-3K	5	4.5 - 5.5	6.0 - 6.9	0 - 3.0	3.3 - 5.5	10	30	15	30	120
FAW 12-1.3K	12	10.8 - 13.2	13.7 - 15.7	0 - 1.3	1.4 - 2.5	20	50	10	30	190
FAW 15-1K	15	13.5 - 16.5	17.0 - 19.0	0 - 1.0	1.1- 2.0	20	50	10	30	220
FAW 24-0.7K	24	21.6 - 26.4	27.0 - 30.5	0 - 0.7	0.8 - 1.4	20	50	20	50	310
25 WATT MODELS	Size: Open - 0.98 x 3.74 x 4.92 in. Enclosed (CA 25) - 1.18 x 3.74 x 4.92 in. Net wt. 10.6 oz, 300 gm. 25 x 95 x 125 mm 30 x 95 x 125 mm									
FAW 5-5K	5	4.5 - 5.5	6.0 - 6.9	0 - 5.0	5.5 - 7.5	9	18	31	62	120
FAW 12-2.1K	12	10.8 - 13.2	13.7 - 15.7	0 - 2.1	2.3 - 3.3	17	35	32	65	190
FAW 15-1.7K	15	13.5 - 16.5	17.0 - 19.0	0 - 1.7	1.9 - 2.8	17	35	42	85	220
FAW 24-1.1K	24	21.6 - 26.4	27.0 - 30.5	0 - 1.1	1.2 - 1.8	17	35	57	115	310
50 WATT MODELS	Size: Open - 0.98 x 3.74 x 6.50 in. Enclosed (CA 26) - 1.22 x 3.74 x 6.50 in. Net wt. 15.9 oz, 400 gm 25 x 95 x 165mm 31 x 95 x 165 mm									
FAW 5-10K	5	4.5 - 5.5	6.0 - 6.9	0 - 10.0	10.5 - 12.0	10	20	30	60	120
FAW 12-4.2K	12	10.8 - 13.2	13.7 - 15.7	0 - 4.2	4.4 - 5.1	15	30	35	70	190
FAW 15-3.4K	15	13.5 - 16.5	17.0 - 19.0	0 - 3.4	3.6 - 4.1	15	30	45	90	220
FAW 24-2.1K	24	21.6 - 26.4	27.0 - 30.5	0 - 2.1	2.2 - 2.6	25	50	50	100	310

UL RECOGNIZED CSA CERTIFIED TÜV APPROVED

FAK MODEL TABLE

15 WATT MODELS	Size: Open - 0.78 x 2.76 x 3.74 in. Enclosed (CA 21) - 0.9 x 2.76 x 3.74 in. Net wt. 5.60 oz,160 gm 20 x 70 x 95 mm 23 x 70 x 95 mm									
FAK 5-3K	5	4.5 - 5.5	N/A	0 - 3.0	3.3 - 5.0	10	30	30	60	120
FAK 12-1.3K	12	10.8 - 13.2	N/A	0 - 1.3	1.4 - 2.3	10	30	30	70	190
FAK 15-1K	15	13.5 - 16.5	N/A	0 - 1.0	1.1- 2.0	10	30	30	70	220
FAK 24-0.7K	24	21.6 - 26.4	N/A	0 - 0.7	0.8 - 1.4	10	30	30	80	310
25 WATT MODELS	Size: Open - 0.98 x 2.76 x 4.53 in. Enclosed (CA 22) - 1.12 x 2 .76 x 4 .53 in. Net wt. 5.98 oz, 170 gm 25 x 70 x 115 mm 28.5 x 70 x 115 mm									
FAK 5-5K	5	4.5 - 5.5	6.0 - 6.9	0 - 5.0	5.5 - 7.5	10	30	30	70	120
FAK 12-2.1K	12	10.8 - 13.2	13.7 - 15.7	0 - 2.1	2.3 - 3.3	10	30	30	70	190
FAK 15-1.7K	15	13.5 - 16.5	17.0 - 19.0	0 - 1.7	1.9 - 2.8	10	30	30	70	220
FAK 24-1.1K	24	21.6 - 26.4	27.0 - 30.5	0 - 1.1	1.2 - 1.8	10	30	30	80	310
50 WATT MODELS	Size: Open - 0.98 x 3.75 x 5.12 in. Enclosed (CA 23) - 1.12 x 3.74 x 5.12 in. - Net wt. 8.80 oz, 250 gm 25 x 95 x 130mm 28.5 x 95 x 130 mm									
FAK 5-10K	5	4.5 - 5.5	6.0 - 6.9	0 - 10.0	10.5 - 12.0	10	30	25	50	120
FAK 12-4.2K	12	10.8 - 13.2	13.7 - 15.7	0 - 4.2	4.4 - 5.1	20	40	25	50	190
FAK 15-3.4K	15	13.5 - 16.5	17.0 - 19.0	0 - 3.4	3.6 - 4.1	20	40	25	50	220
FAK 24-2.1K	24	21.6 - 26.4	27.0 - 30.5	0 - 2.1	2.2 - 2.6	30	60	25	60	310

(1) Nominal input, maximum load, 25°C.
(2) Power supply operates with no load, however stablization is specified 10% - 100% load. See figure 1 for rating up to 71°C.
(3) FAK 15W and 25W models: foldback, fixed. FAK 50W models: rectangular, fixed. FAW use a Winker type overload protection which turns the power supply on and off at a 5-10Hz rate until overload is removed.
(4) 0 to 50°C, 10% to 100% load.

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INPUT CHARACTERISTICS

SPECIFICATION		RATING FAW 15W	FAW 25W	FAW 50W	FAK 15W	FAK 25W	FAK 50W	CONDITION
a-c voltage	nom	120/240V a-c			120V a-c			Single phase
	range	85-264V a-c			85-132V a-c			
d-c voltage	range	105-370V d-c			110-170V d-c			Polarity insensitive
Brown-out voltage	min	80V a-c / 97V d-c			80V a-c / 105V d-c			Ripple, stab spec increase
a-c current	typ	0.3A	0.55A	1.0A	0.28A	0.50A	0.9A	120V a-c rms
	max	0.4A	0.70A	1.2A	0.35A	0.65A	1.1A	
	typ	0.2A	0.35A	0.5A	—	—	—	240V a-c rms
	max	0.3A	0.45A	0.7A	—	—	—	
Fuse value		2.0A	2.5A	3.0A	2.0A	2.5A	3.15A	250V type 5x20mm
Initial turn on surge, first half cycle		22A	43A	45A	22A	43A	43A	120V a-c rms
		34A	85A	90A	—	—	—	240V a-c rms
Frequency	nom	50-60 Hz			50-60 Hz			Single phase
	range	47-440 Hz(1)			47-440 Hz(1)			
EMI		FCC 20780 and VDE 0871			FCC 20780			Conducted Class B
Soft-start circuit		Thermistor limiter			Thermistor limiter			
Efficiency	typ	70%	70%	76%	70%	70%	75%	Max load, nominal input
Leakage current	max	0.5 mA UL method			0.5 mA UL method			120V a-c, 50-60 Hz
	max	0.75 mA VDE method			—			240V a-c, 50-60 Hz
Startup time	max	500 msec			100 msec			From turn on until d-c output reaches nominal
Holdup time	typ	20 msec			30 msec			120V a-c
	min	15 msec			20 msec			100V a-c
Power OK		Green LED plus logic			Green LED			(See figure 2)
Circuit type		Flyback	Flyback	Forward converter	Flyback	Flyback	Forward converter	
Switching frequency	typ	120KHz			70KHz	50KHz	260KHz	Nominal load

(1) At 440Hz the leakage current exceeds the UL safety specification

OUTPUT CHARACTERISTICS

SPECIFICATION		RATING FAW	FAK	CONDITION
Source effect	typ	1.0%	—	FAW: 85 - 132 or 170-264Va-c FAK: 85 - 132V a-c
	max	2.0%	2.0%	
Load effect	typ	1.0%	1.2%	10% to 100% load
	max	2.0%	3.0%	
Temperature effect	typ	1.0%	0.6%	Nominal input rated load,
	max	2.0%	2.0%	
Combined effect	typ	2.0%(1)	1.0%	Source, load and temperature
	max	4.0%	3.0%	
TIme effect (drift)	typ	0.1%	0.1%	0.5 - 8.5 hr, max load 25°C
	max	0.5%	0.5%	
Recovery characteristic	excursion	<4%	<4%	Step load 50-100%, rise time >50µs
	recovery	1ms(2)	1 msec	To within 1%

(1) FAW 15W and 25W : 2.6%
(2) FAW 15W and 25W : 2ms

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Series FAW International
Series FAK North American

	FAW International	FAK North American
Safety Approval	UL 478 CSA EB1402B IEC 380 VDE 0806	UL 478 CSA EB1402B
EMI	FCC 20780 VDE 0871 Class B	FCC 20780 Class B
Input	85 - 264V a-c wide range	85 - 132V a-c

FAW FEATURES

- **Power-OK LED**: green.
- **Power-OK logic**: open collector.
- **a-c input: 85-264V a-c;**
  d-c input: 105-370V d-c.
- **Operating frequency**: 120-130KHz.
- **Soft-start circuit:** limits a-c turn on surge.
- **Adjustable voltage**: internal trimmer.
- **Holding time:** output is sustained by internally stored energy for 20ms typical 15ms minimum.
- **Built in EMI filter**: attenuates the conducted noise below the requirements of both FCC 20780 and VDE 0871 for Class B computing devices. Optional perforated metal covers attenuate radiated noise and provide protection.
- **Safety:** FAW are recognized by UL, certified by CSA and approved by TUV Rheinland.
- **Connections:** input and output screw terminal barrier strip.
- **Remote error sensing**: the 50W FAW provides separate remote error sense terminals: 0.25V drop/wire.
- **Optional Steel Enclosures:** CA 24, CA 25, CA 26

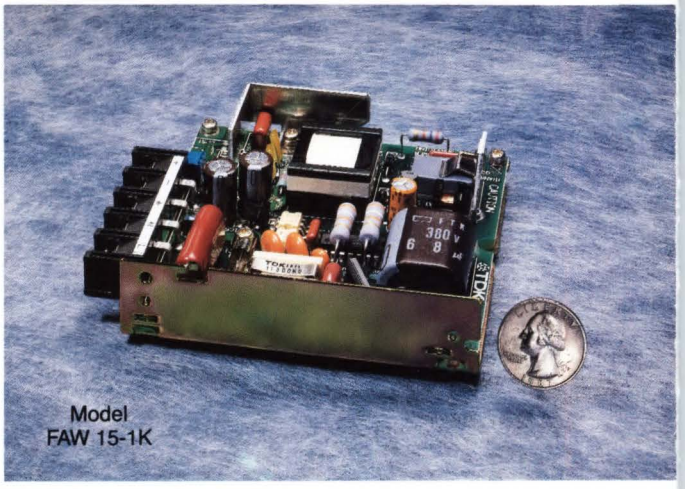
FAK FEATURES

- **Power OK LED:** green
- **a-c input 85-132V a-c**
  d-c input 110-170V d-c.
- **High frequency operation** (up to 260 KHz) for high efficiency.
- **Soft Start Circuit**: Limits a-c turn-on surge.
- **Adjustable voltage**: internal trimmer.
- **Holding time:** Output is sustained by internally stored energy for 30 milliseconds typical, 20 milliseconds minimum.
- **Built-In EMI filter** attenuates conducted noise below the requirements of FCC 20780 for Class B computing devices. Optional perforated metal covers attenuate radiated noise and provide protection.
- **Safety:** All models recognized by UL, certified by CSA.
- **Connections:** Input and output screw terminal barrier strip.
- **Optional Steel Enclosures:** CA 21, CA 22, CA 23

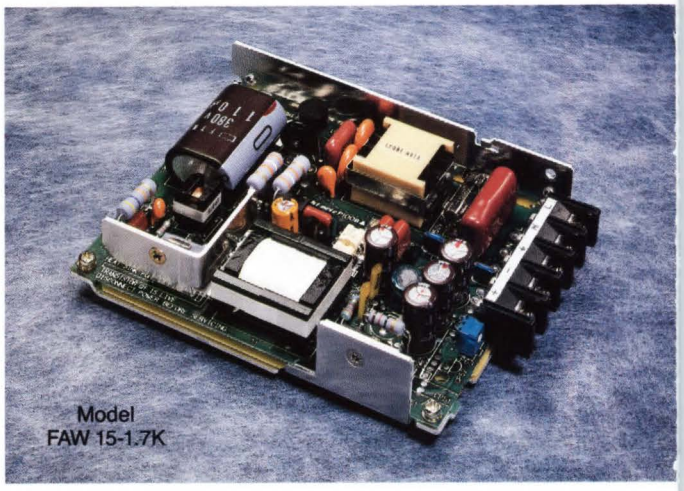
KEPCO'S VERY COMPACT SINGLE

INTERNATIONAL SERIES FAW

Wide-range input, 85-264V a-c • 15, 25 and 50 Watts
UL/CSA/TÜV approvals



Model
FAW 15-1K



Model
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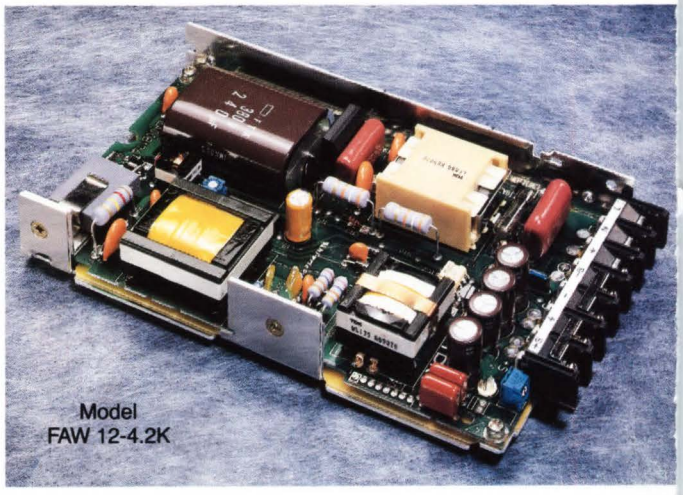


Model
FAW 12-4.2K

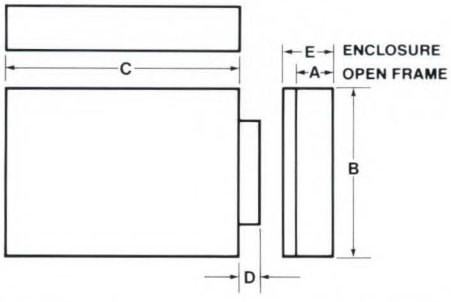
Kepco's very compact single output a-c to d-c switching power supplies

FAW/FAK GENERAL SPECIFICATIONS

SPECIFICATIONS		RATING/DESCRIPTION	CONDITION
Temperature		0 - 71°C (see fig. 1)	Operating
		-40°C to +85°C	Storage
Humidity		95% RH	Non condensing: operating & storage
Shock		20g, 3 axes (11 msec +/- 5 msec pulse duration)	Non operating, 3 shocks each axis
Vibration		5 - 10Hz: 10mm amplitude 3 axes	Non operating 1 hour each axis
		10 - 55Hz: 2g, 3 axes	
Isolation	Output to case	500Vd-c, 100MΩ	25°C, 65%RH
Enclosure		Optional metal	
Type of Construction		PC card, L-chassis	
Cooling		Convection	
FAW			
Withstand Voltage	Input to output	3.75KV a-c for 1 minute	25°C, 65%RH
	Input to Case	2KV a-c for 1 minute	
Safety		UL 478	Recognized
		CSA EB 1402B	Certified
		VDE 0806, IEC 380	Approved
FAK			
Withstand Voltage	Input to output	2KV a-c for 1 minute	25°C, 65%RH
	Input to Case	2KV a-c for 1 minute	
Safety		UL 478	Recognized
		CSA, EB 1402B	Certified

OUTLINE DIMENSIONAL DRAWINGS

Dimensions in light face type are in inches,
dimensions in bold face type are in millimeters.



FAW

MODEL	A(2)	B	C	Barrier Strip Protrusion D	E(1)
15 WATTS	0.98 **25**	3.74 **95**	3.94 **100**	0.59 **15**	1.18 **30**
25 WATTS	0.98 **25**	3.74 **95**	4.92 **125**	0.59 **15**	1.18 **30**
50 WATTS	0.98 **25**	3.74 **95**	6.50 **165**	0.59 **15**	1.22 **31**

FAK (Barrier Strip does not protrude)

MODEL	A(2)	B	C	E(1)
15 WATTS	0.78 **20**	2.76 **70**	3.74 **95**	0.9 **23**
25 WATTS	0.98 **25**	2.76 **70**	4.53 **115**	1.12 **28.5**
50 WATTS	0.98 **25**	3.74 **95**	5.12 **130**	1.12 **28.5**

(1) With cover (optional) (2) Open frame

Tolerances: 0.04" (1.0 mm) unless otherwise noted
Mounting: 4-40 tapped holes — (2) side;
maximum screw penetration 0.2 (5 mm)

FIG. 1 OUTPUT POWER VS AMBIENT TEMPERATURE

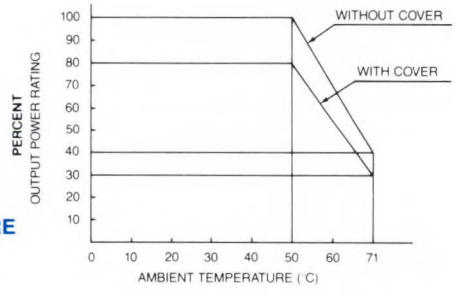
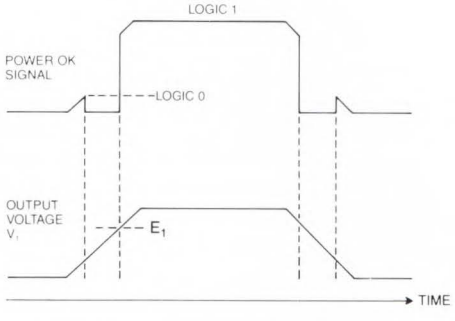


FIG. 2 POWER OK SIGNAL RELATED TO OUTPUT (FAW models only)



		5V model	12V model	15V model	24V model
E_1 (min)		4.5V	9.5V	12V	19V
Logic 1	(min)	2.5V	5V	6V	9V
	(max)	< OUTPUT VOLTAGE			

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POWER IC DRIVES MOTORS AND SOLENOIDS

WITHOUT GOING TO GREAT EXPENSE, YOU CAN PROGRAM CIRCUITS AND CURRENTS FOR DMOSFETS ON THIS THREE-CHANNEL IC.

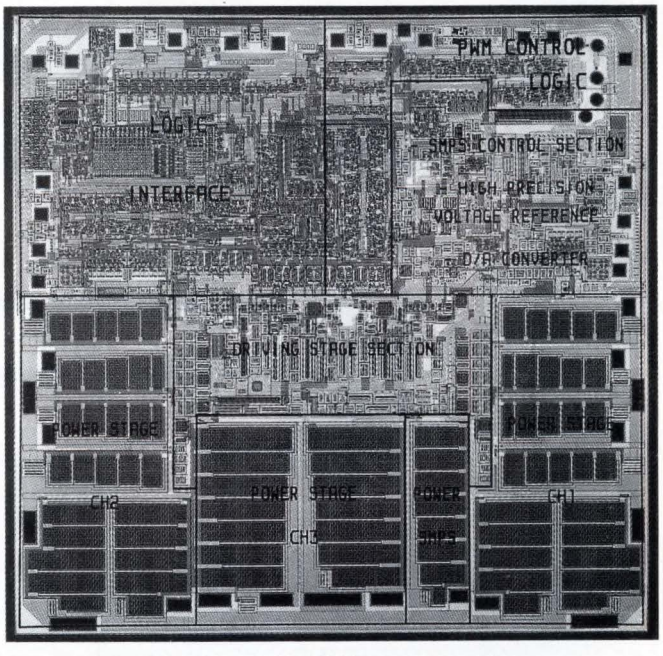
FRANK GOODENOUGH

System designers must occasionally control loads of more than several hundred milliamperes at more than 40 V. And such loads as motors, solenoids, relays, and contactors are often inductive. Though many power ICs might be available to drive the loads, there are instances where none meet your needs. Consequently, the final design may employ monolithic controller and driver ICs, but numerous discrete transistors, diodes, and ICs will remain on the pc board.

This predicament can be alleviated by employing the L6820, a three-channel multipower driver system from SGS-Thomson. Unlike most power ICs that are absolutely fixed in their application (true ASICs), the L6820's three output circuits can be configured with software to drive stepping motors, dc motors, or solenoids.

This power IC, which has about 260 mils on each side, mixes over 4000 small-signal transistors with 15 n-channel power MOSFETs. It's the most complex device of the so-called "smart power" genre *(Fig. 1)*. Small-signal digital circuitry includes about 1000 CMOS gates. Precision analog circuits contain a 5-V reference for five on-chip digital-to-analog converters. Each converter's output becomes the reference for a control loop. A total of 15 DMOS power FETs control over 15 W continuously with peaks of 250 W. The mix of that much power handling with that much small-signal circuitry resulted from SGS-Thomson's Multipower BCD fabrication process.

The L6280 offers three separate, current-controllable



1. CRAMMING 4000 SMALL-SIGNAL transistors and 15 power DMOSFETs on a die that's about 68,000 mils^2 in area, the L6280 from SGS-Thomson easily controls a peak power of over 250 W without a heat sink.

power outputs: Two supply up to 1 A of pulse-width-modulated (PWM) drive current for a stepping or dc motor, or one or two solenoids; the third offers 3 A of PWM current to drive a solenoid or a unidirectional dc motor *(Fig. 2)*. The input power rail can range from 12 to 48 V.

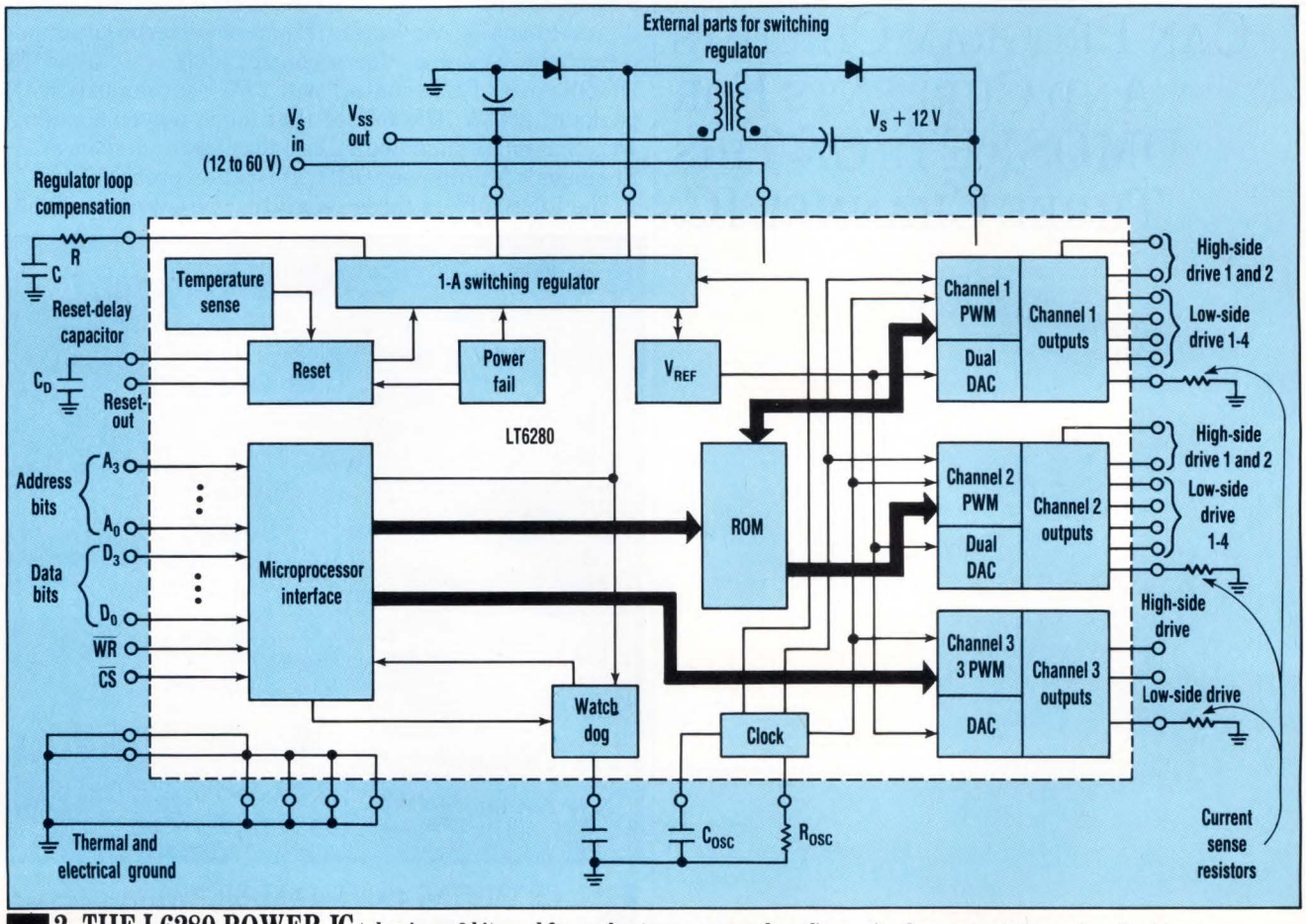
In addition, an on-chip switching regulator takes the input power rail (V_{SS}) and converts it to 1 A of regulated 5-V power (V_S) for the L6280's logic and external devices, such as its host microprocessor. This is accomplished with the help of an external inductor, rectifier, and filter. Because the chip's CMOS gates (approximately 1000) require minimum power, access is available to virtually all of the current for your host and system. A second winding on the inductor and a rectifier develop the +12-V V_S, a bootstrap voltage that powers the drive for the gates of the high-side MOSFET switches in each channel.

The complete chip is under the control and monitoring of a host microprocessor through a standard interface that consists of an 8-bit-wide bus plus and lines. The microprocessor interface decodes the first four bits (A_{0-3}). Depending on the content of the remaining four bits (D_{0-3}), this interface configures the output power-transistor circuits (channels 1 and 2), activates the PWM loops of all three channels, and sets the desired output current for each channel via the five d-a converters.

Pick A Load, Any Load

Arrangement of each output circuit for channels 1 and 2 consists of six totally isolated, vertical DMOS transistors rated at a maximum of 60 V *(Fig. 3)*. The two high-side switches (drivers) have on resistances of just 1 Ω; the four low-side switches have twice that. On resistance of the single high- and low-side switches in the 3-A channel 3 is 0.5 Ω. Four possible hardware configurations are shown: four separately controlled drives for the four coils of a unipolar stepping motor, a full-bridge drive for a dc motor, a drive for one solenoid, and a dual half-bridge drive for a dc motor *(Fig. 3a)*.

In each circuit, a current-controlling PWM loop is closed around the power FETs and the windings. With a patented time-sharing technique, one comparator and an off-chip current-sensing resistor can control the current in two separate windings of one channel, such as two solenoids *(Fig. 3b)*. A 50-kHz clock sets the PWM latch and generates two 180° out-of-phase square waves—phases 1 and 2—which close the current loop around the left and right pairs of



2. THE L6280 POWER IC takes in an 8-bit word from a host processor and configures its three outputs for various load types. Channels 1 and 2 control up to 1 A each; channel 3 controls up to 3 A. The on-chip switching regulator powers chip logic and analog circuits while externally supplying 1 A at 5 V.

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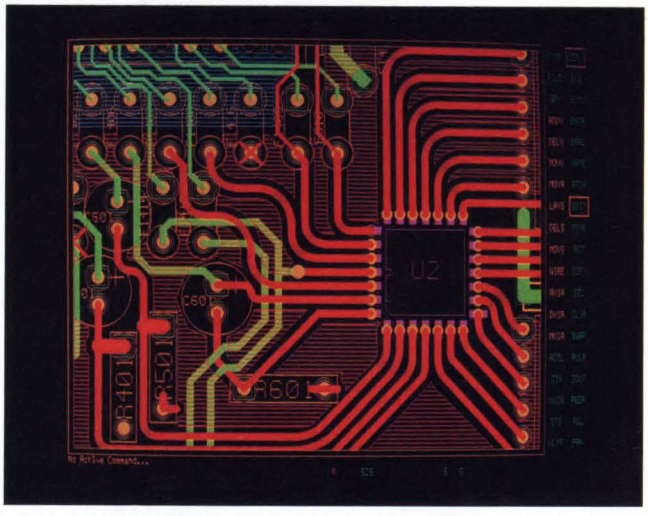

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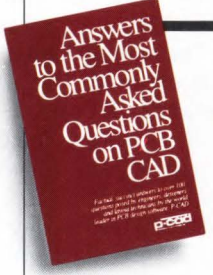

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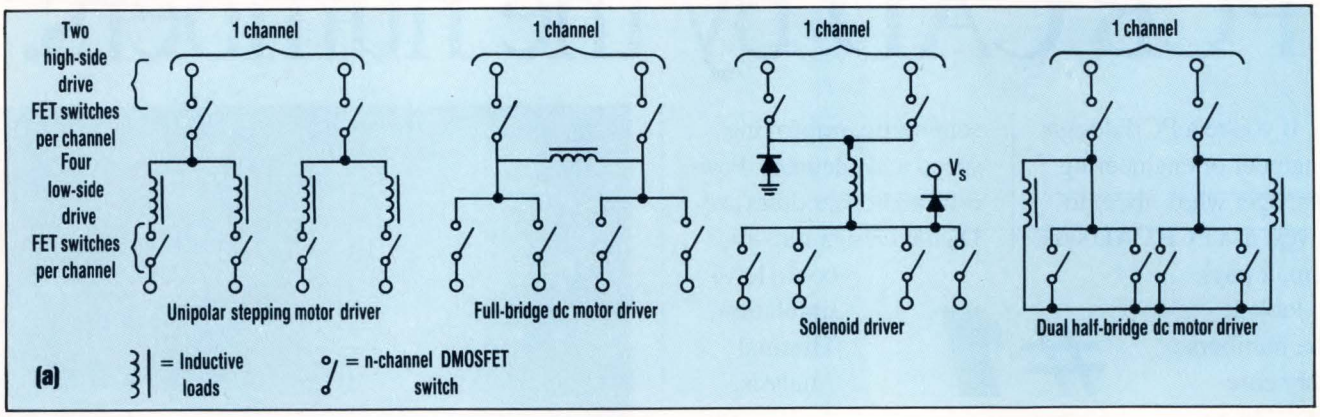
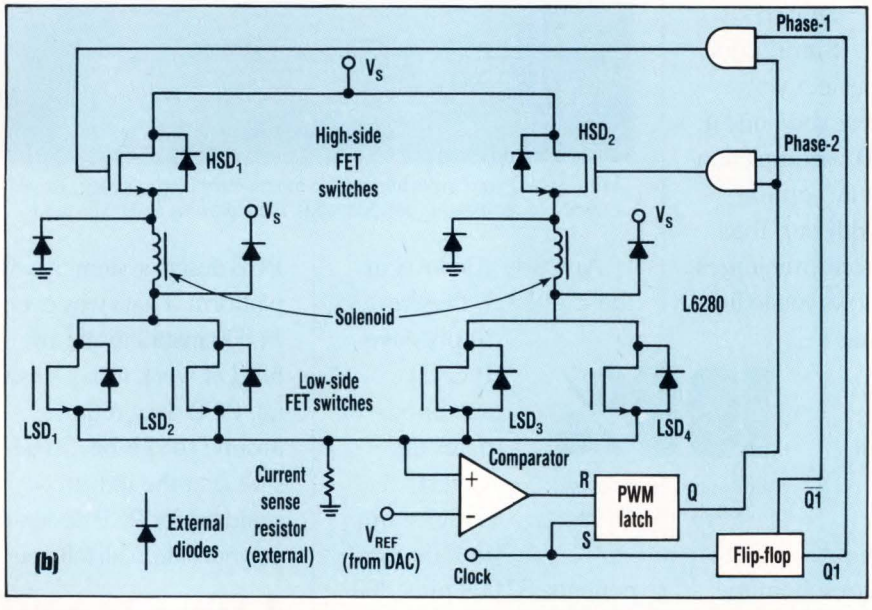
CIRCLE 63

PROGRAMMABLE "SMART" LOAD DRIVER





3. THE 4-BIT DATA WORD from the L6820's host sets up the PWM control and drive circuits of channels 1 and 2 for four different types of loads (a). When two different loads are controlled by one channel, such as these two separate solenoids, a time-sharing technique makes it possible for one PWM loop to independently control the current in both circuits (b).

winding, respectively. When phase 1 is high, phase 2 is low. Also, high-side drive transistor HSD_1 is on and HSD_2 is off, and current in the left-hand solenoid is being controlled.

Current flows through HSD_1, LSD_1, LSD_2, and the sense resistor until the voltage across the sense resistor reaches V_{REF} (which is set by the 3-bit d-a converter between 0.125 and 1 V). The comparator then fires and resets the PWM latch, turning off HSD_1. Recirculation current flows through LSD_1 and LSD_2, but not through the sense resistor, which is now free to monitor the current in the other solenoid. Current control is transferred to the right-hand solenoid by the next clock pulse when phase 1 goes low and phase 2 goes high, turning on HSD_2. The effective control frequency for each pair of windings is 25 kHz. When only one load is present, as with a dc motor, the time sharing is turned off and the PWM frequency is dropped to 25 kHz. The catch (free-wheeling) diodes at either end of the coils are external.

The on-chip switching regulator is conventional. Its 1-A and 1-Ω-on-resistance FET switch is connected in a buck topology. The drain runs to the supply V_S; the source runs to the inductor. It delivers 5 W (1 A at 5 V) with 90% efficiency while switching at 100 kHz. Its regulation loop uses a classical PWM circuit that includes a sawtooth generator, error amplifier, comparator, and PWM latch.

Protection circuits include overcurrent sensing that turns off the power transistors when a current of 1 A is exceeded and a voltage-sensing circuit that generates a power-on Reset signal for the host. The circuit senses both the input supply rail and the output regulated voltage, and sets the Reset-Out pin to its nominal 5-V supply voltage only when both sensed voltages are correct *(Fig. 2 again, upper left).*

CHECKS AND BALANCES

When you power-up the chip, its switching supply stays off until the input rail V_S reaches 12 V. After the switching supply comes on, the Reset-Out pin is low and remains low until V_{SS} reaches 4.75 V. During this period, the logic and output devices are disabled and signals from the host are ignored. In addition, the processor sees a Low on Reset-Out.

When the 5-V supply stabilizes and after a time delay is set by the external capacitor C_D, Reset-Out goes high and tells the host that L6280 is ready for the host to send a "keyword" and the initialization sequence. All commands received prior to the keyword are ignored by the L6820.

After the keyword (00111010) is received, the L6820 activates the "watch-dog" circuitry and begins to control the processor's functionality. The processor must now periodi-

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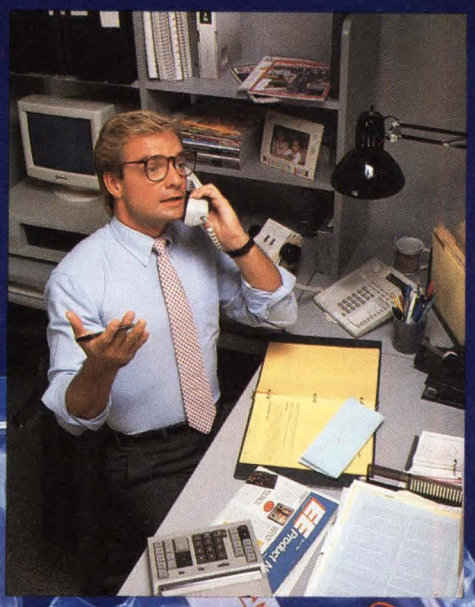
Now what?!"



All indications are Dialight.

The customer was an electronics firm known for his highly specialized, custom equipment. He had the proprietary technology; his problem was getting a wide range of custom indicators to match. And his newest product was due for immediate release. That's when he called Dialight.

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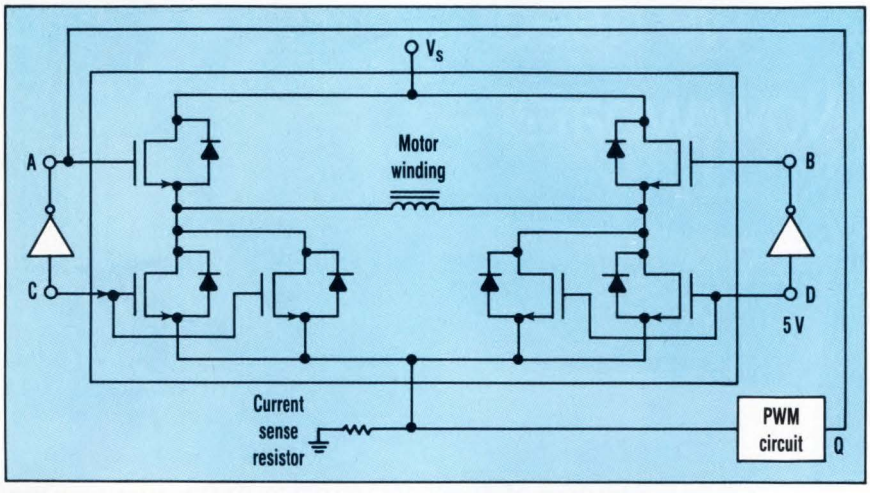
CIRCLE 64

PROGRAMMABLE "SMART" LOAD DRIVER



4. AFTER CONFIGURING CHANNELS 1 OR 2 of the L6280 for a specific load, such as a full-bridge to drive a dc motor, a series of 4-bit data words (code) from the host supply various control modes. Code X000 delivers a Tristate signal on left and right sides; code X001 supplies a Chopper signal on the left side and a Brake signal on the right side; code X011 gives a Brake signal on left and right sides; and code X101 provides a Diagonal Chopper signal on both left and right sides.

cally send the watch-dog word (00110101), or its absence is interpreted as a microprocessor failure. If the watch-dog word is absent, the L6820 disables its power output stages to prevent any damage to itself or to its loads. No reset signal for the host is generated. The chip can be started up by repeating the start-up sequence from power-up.

Next, the host configures channels 1 and 2 to fit their respective loads (stepping motor, dc motor or solenoid) through the data bus. The third and fourth address bits choose the channel, and the first three data bits choose the configuration. The first two address bits define an "output initialization status." An input configuration is ignored if the first two –bits are different from the initialization bits.

Both channels must be sequentially initialized and configured. If two initializations arrive for the same channel, the chip disables the output stages and Reset-Out goes low for the time delay set by capacitor C_D, which advises the host of the error. To commence, the start-up procedure must be repeated from the keyword step. After initialization, the chip begins to accept commands. If one is sent before its channel has been configured, the command is ignored.

The commands include loading a channel's current level into a d-a converter, incrementing or decrementing a d-a converter's output, and selection of a driving strategy for a channel (for example, half or full step and fast or slow decay).

A channel can also be set up to drive a dc motor with a full-bridge topology. *(Fig. 4).* The connection between the output of high- and low-side drivers and the load are external; the remainder is internal. Sending the data word X000 gives you a three-state output at port A, which is now shorted with C, and port B, which is now shorted with D. External connections made through a software program can result in various circuit arrangements. Because 0 V is applied to the gates of all the channel's FET switches, the switches are in the off state (open) and no current flows.

Sending the word X001 gets a Chopper signal on the left side and a Brake signal on the right *(Fig. 4, again).* The left side of the bridge is controlled by the PWM loop *(Fig. 3b, again),* while HSD_2 is held off and LSD_3 and LSD_4 are held on. During the on time controlled by the PWM loop, current flows through HSD_1, the motor winding, and LSD_3 and LSD_4. During the off time, the current recirculates through all four of the lower FETs. Used in the motor-control industry, the terms "chopper" or "chopping" refer to controlling the average power to a load by alternately switching the load's voltage source off and on.

If the word X010 is sent, a Chopper signal appears on the right side and a Brake signal on the left. The PWM loop controls the right side of the bridge and 5 V is applied to point C *(Fig. 4, again).* The direction of current flow through the coil (and thus motor rotation) is reversed. If X011 is sent, you get a Brake signal on the left and right sides. All the high-side drivers are now off and all the low-side drivers are on. The motor winding is short-circuited through the low-side drivers and the motor's back EMF brakes the rotating load.

If the data word X101 is sent, a Diagonal Chopper signal appears on both sides. During the on time with Q high, the current flows through HSD_1, the motor winding, and LSD_3 and LSD_4. During the off time when Q is low, the current recirculates through LSD_1 and LSD_2, the motor winding, and HSD_2.□

PRICE AND AVAILABILITY

The L6280 comes in a 44-lead, plastic-leaded chip carrier (PLCC). Internally, it's mounted on a 38 + 6 copper leadframe. The chip's common ground line is connected to six pins. When soldered to a typical pc-board's foil, these pins supply the only heat sinking needed by the device. With this mounting, it can dissipate 1.5 W at 70°C. Operating temperature ranges from 0° to 150° C. In quantities of 100, the L6280 costs $8.75 each. Delivery is from stock.

SGS-Thomson Microelectronics, 1000 E. Bell Rd., Phoenix, AZ 85022-2699; Tom Hopkins, (602) 867-6100. **CIRCLE 514**

HOW VALUABLE?	CIRCLE
HIGHLY	559
MODERATELY	560
SLIGHTLY	561

FAST MONOLITHIC 8-BIT ADC ENCODES 100-MHZ SINE WAVES TO 6.4-BIT ACCURACY

FRANK GOODENOUGH

Not only is it the fastest monolithic 8-bit analog-to-digital converter around, but at under $200 each in hundreds, Analog Devices' AD9028/AD9038 flash converters are less than one-tenth the cost of some faster two-chip hybrid a-d converters. Typically, they sample input signals at 325 MHz. A minimum 300-MHz rate is guaranteed and minimum and maximum dynamic (ac) specifications are given for a 250-MHz sampling rate.

These converters are aimed at two major, but very different, applications—military radar and laboratory instruments. The former include EW/ECM (electronic warfare and countermeasures, or jamming) systems; the latter, digital oscilloscopes and waveform and spectrum analyzers. But they also find uses in special-purpose instrumentation created for nuclear-accelerator experiments and classified nuclear research.

The converters use a typical flash architecture with 256 comparators (the 256th provides an "overflow" output) and a reference resistor divider. The input drives all the comparators, while each tap on the divider drives one comparator. Both the top and bottom of the 24-to-60-Ω divider have source and sense pins to ensure accuracy.

The AD9028 and AD9038 differ in just one way. The former has eight parallel ECL data outputs (plus the overflow bit); the latter contains an internal digital multiplexer and two sets of outputs. The data words alternate between the two sets of outputs, at half the sampling rate, and for twice as long as on the 9028. This eases the job of handling such high-speed data.

Depending on the ac performance required, the input signal can be handled in any one of three modes. In one, the analog input is driven and the analog-return pin (the collectors of the comparators' input transistors) is connected to ground. A second mode drives the analog input and connects the analog return to +1.5 V. In the third, both the analog input and the analog return are driven while offsetting the analog return by +1 V *(see the figure)*.

In the first mode, the input capacitance varies from about 18 pF to 15 pF as the signal goes from zero to full scale (2 V). In the second, the input capacitance remains virtually unchanged, varying between 14 and 14.5 pF. In the third mode, input capacitance remains a constant value of about 11 pF. The performance gain is dramatic. Signal bandwidth for a given accuracy (effective bits) virtually doubles.

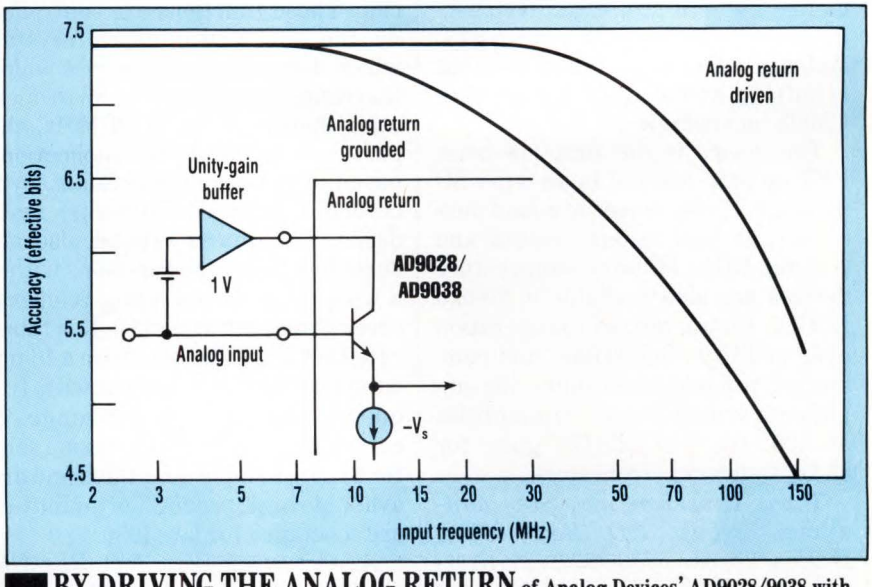
Several of the converters' minimum/maximum dynamic specifications are guaranteed (when sampling a 2-V pk-pk sine wave at 250 MHz with the analog return at +1 V). Effective bits for 9.3-, 49-, and 92-MHz signals are 7.2, 6.5, and 5.4 bits, respectively. In-band harmonics at the same frequencies are 54, 41, and 36 dBc (dB below the carrier, or below full scale). Signal-to-noise (rms) ratio with an analog input of 1 dB below full scale is 45.5, 43, and 33 dB, respectively, for the same frequencies. Two-tone intermodulation distortion rejection for 60- and 70-MHz input signals, each 7 dB below full scale, is 42 dB. In addition, no missing codes is guaranteed.

The chips can handle Nyquist-frequency signals (1/2 the sampling rate) even when sampling at over 300 MHz. This is because their full-power bandwidth is typically 250 MHz and their aperture uncertainty (jitter) is typically just 3 ps rms.

The chips require 550 mA from the –5.2 V, of which 14.5 mA flows from the analog return. The remainder flows out of the ground pins. The 178-by-148-mil die is packaged in 68-pin leaded and leadless ceramic chip carriers. In quantities of 100, prices range from $185 each for commercial-temperature-range units to $500 each for military-temperature-range units screened for MIL-STD-883. Small quantities are available from stock.

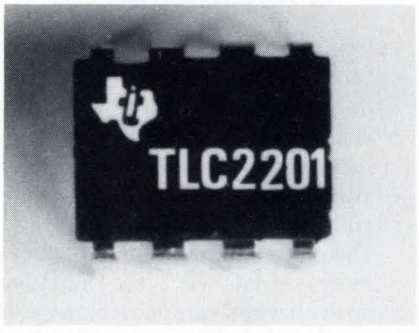
Analog Devices Inc., 7910 Triad Center Dr., Greensboro, NC 27409; David Duff, (919) 668-9511.

CIRCLE 313



BY DRIVING THE ANALOG RETURN of Analog Devices' AD9028/9038 with the input signal offset by +1 V, accuracy rises for input signals above 7 MHz.

OPERATIONAL AMPLIFIER PROVIDES LOW-FREQUENCY SIGNAL DISCRIMINATION



A low-noise CMOS-input precision op amp is now available specifically for use in signal-conditioning applications involving low-level signals from high-impedance sources. Potential uses for the TLC2201 op amp include computerized axial-tomography (CAT) scanners and underwater acoustic detectors, which currently use discrete components.

The device combines the lowest-noise JFET amplifiers with the dc precision that had been found only in bipolar amplifiers. According to the company, the TLC2201 is the lowest-noise FET op amp, either CMOS or JFET, in its power class with 18 nV/$\sqrt{\text{Hz}}$ at 10 Hz.

According to TI, its silicon-gate advanced LinCMOS process technology is key to the op amp's performance. The TLC2201 has a 100-μV input-offset voltage with a 0.5-μV/°C stability, which is far superior to that resulting from other metal-gate CMOS technologies.

The device is the first low-noise FET op amp offered in an 8-pin SO package. It also comes in 8-lead metal cans as well as 8-pin plastic and ceramic DIPs. Military-temperature devices are also available in 20-pad LCCCs. Characterized for operation over military-, industrial-, and commercial-temperature ranges, the amplifier is available now. In quantities of 100, the TLC2201CP goes for $3.26. Delivery is from stock.

Texas Instruments, Semiconductor Group, P.O. Box 809066, Dallas, Texas 75380-9066; (800) 232-3200, ext. 700. **CIRCLE 314**

JON CAMPBELL

HIGH-FREQUENCY SWITCH OPERATES AT 100 NS

Besides a wide bandwidth of 200 MHz, a dual SPST analog switch boasts a switching speed of 100 ns, suitable for demanding video and imaging applications. The monolithic device, designated HI-222, also features an on-resistance of 35 Ω. A dielectric isolation process allows complementary circuit design with low parasitics, ensuring broadcast quality differential gain and phase error performance. The latter is specified at 0.003°, while the former is rated at 0.03%. A 30-V signal range and fast TTL-compatible operation over a wide range of supplies and temperatures suit the HI-222 for military rf and medical signal-processing systems. Packages include plastic and ceramic DIPs, PLCCs, and LCCs. Prices start at $4.67 in lots of 100.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; (407) 724-3800. **CIRCLE 336**

TIMING-RECOVERY IC ENHANCES TRANSMISSION

A single-chip, crystal-based timing recovery unit is designed for precise digital-signal transmission. Designated the TRU-050, the device combines a phase detector, op amp, and voltage-controlled oscillator on one chip. These functions are controlled by the TRU-050's quartz crystal, which determines the rate at which the device transmits data. With operating speeds of up to 52 MHz, the part can be used for applications based on the developing Sonet (Synchronous Optical Networks) standards. The quartz crystal also ensures low jitter, and functions within a wide range of operating temperatures (from −40° to +85°C). It is fabricated in CMOS and housed in a 16-pin ceramic DIP. Price varies with frequency and temperature range. A commercial 32.768-MHz version sells for $125 in sample quantities and are available now; production quantities are scheduled for late 1989.

AT&T, 1 Oak Way, P.O. Box 610, Berkeley Heights, NJ 07922; (800) 372-2447. **CIRCLE 337**

COPROCESSOR BOARD MAKES OBJECT-ORIENTED SOFTWARE AVAILABLE TO SUN USERS

Sun workstation users now have access to a comprehensive object-oriented development environment, thanks to a coprocessor board from Symbolics. The UX400S board permits the company's Genera environment to run on most Sun-3 and Sparc-based workstations. The board offers high-end development capability and tight integration with the Unix environment.

The board integrates the Genera environment with the Unix-based SunOS. Genera applications appear within the host Sun window system just as native Unix applications do. A variety of standard network services, such as the X Window system; NFS; the Network Filesystem protocol; and RPC, a remote procedure-call protocol, are provided to ease communication between the two systems. With this high integration level, developers can use the extensive library of software applications and fast I/O available with Unix as well as the powerful software-development environment offered by Genera.

Thanks to its open architecture and highly integrated development tools, Genera helps software designers get from prototype to product quickly and efficiently. Its development methodology dramatically shortens development cycles for complex products.

In its standard configuration, the UX400S board includes the company's Ivory processor board complete with VMEbus interface, 10 or 20 Mbytes of main memory, and Genera delivery software. The full Genera development system and a floating-point accelerator are optional. The system boards conform to the 9U-by-400-mm Eurocard form factor and VMEbus specs.

An entry-level UX400S system goes for $13,900 and is available from stock.

Symbolics Inc., 8 New England Executive Park, Burlington, MA 01803; (617) 221-1000. **CIRCLE 315**

DAVID MALINIAK

SUBSYSTEM MODULE PACKS RISC CPU, FPU, AND 64-KBYTE CACHE MEMORIES

To take the pain out of evaluating the R3000 RISC microprocessor, Integrated Device Technology has come up with the 7RS101, a subsystem module that includes the R3000 RISC CPU chip, the floating-point accelerator (optional), dual 64-kbyte caches, and other features. Until now, designers had to build their own evaluation boards, hoping that they got the layout right and didn't compromise chip performance.

Moreover, the 3.7-by-6.5-in. module comes in 12-, 16-, 20-, and 25-MHz versions and with or without the floating-point accelerator. The first versions of the module have separate 64-kbyte instruction and data caches, a four-word read buffer, and a one-word write buffer. Future versions will offer both simpler and more complex memory arrangements. Designed to plug onto a two-board development system, the module can cut many weeks off the initial evaluation phase.

The IDT7RS301 development system has two boards that split the module's support functions. One, which is called a personality card, holds the module, the system clock, and the bus buffers. The other card packs 1 Mbyte of static memory (expandable to 2 Mbytes), a debug monitor in 32 kwords of EPROM, two serial ports, three counter-timers, and two uncommitted byte-wide ports. To further ease system analysis, the personality board includes multiple connectors that tie Hewlett-Packard logic analyzers directly to the various signal lines.

In quantities of 100, the modules start at $1856 for the 12-MHz card and go to $3396 for the 25-MHz board. The 7RS301 development board sells for $3000 in singles. Both are available from stock.

Integrated Device Technology Inc., 3236 Scott Blvd., P.O. Box 58015, Santa Clara, CA 95052-8015; Nageen Sharma, (408) 727-6116.

CIRCLE 316

DAVE BURSKY

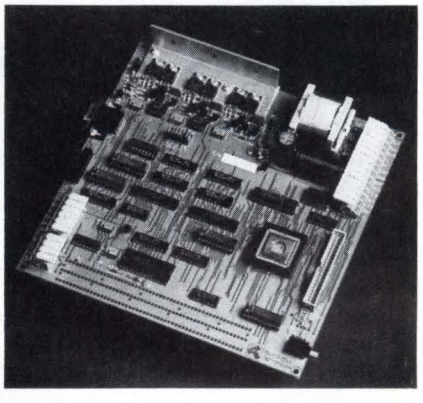
DSP BOARD, DEVELOPMENT TOOLS SIMPLIFY REAL-TIME CONTROL SYSTEMS

The Power-14 DSP board and development software from Teknic Inc. are a good solution for engineers looking at digital-signal processing for upgrading the performance of control applications. DSP devices compute control algorithms, such as Kalman filters, much faster than do analog controllers.

Built around Texas Instruments' TMS320C14 16-bit DSP microcontroller, the Power-14 board is completely configurable, and can function as a simple emulator or as a high-performance digital servo-controller. The board contains the DSP controller, an embedded monitor and debugger program, breakpoint hardware, emulation hardware, RS-232 communication hardware, and three channels of switching servo-amplifiers.

The TI DSP chip delivers 10 to 20 times the speed of conventional microcontrollers. Although it is a fixed-point processor, it can perform floating-point calculations in software.

In addition to the software-debugging program included with the board, users get motion-control soft-



ware support from Teknic's software-development tools.

The Power-14 evaluation and prototyping system and the PowerSource software package cost $987 and $995, respectively. Both are available now.

Teknic Inc., 214 Andrews St., Rochester, NY 14604; (716) 546-3212. **CIRCLE 317**

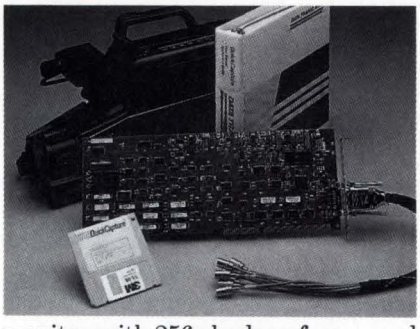
LISA GUNN

FRAME-GRABBER FAMILY EXPANDS WITH A SOFTWARE-COMPATIBLE PC/AT MODEL

The QuickCapture family of frame grabbers capture, store, and display live images from video cameras, VCRs, and still-video devices in real time. The newest family member is a PC/AT-compatible board, the DT2855, that is software compatible with the PS/2 version introduced in December, 1987. Applications developed for one board run on the other without alteration. The QuickCapture series is targeted at scientific image processing and desktop publishing.

The DT2855 frame-grabber board plugs into PC/AT-compatible machines and connects to all video equipment with RS-170, PAL, CCIR, and NTSC video formats using a simple BNC cable connection. It captures images in real time (1/30 of a second), and features a phase-locked-loop circuit for jitter-free image capture from VCRs. The images are stored in a 512-kbyte on-board memory.

Once captured, images can be displayed on any RS-170 RGB analog



monitor with 256 shades of gray and 640-by-480-pixel resolution. When an output look-up table is used, output is displayed with 256 colors. A look-up-table processor on the board enhances images in real time as they are acquired. Operations performed by the processor include arithmetic functions and contrast adjustment.

For users who wish to develop custom applications, the QuickCapture developer's kit provides pixel-manipulation capabilities as well as access to all of the board's features through the software driver. The developer's kit, which runs under PC-DOS, has more than 50 functions that simplify programming of the frame grabber's 14 control registers.

The DT2855 PC/AT QuickCapture frame-grabber board costs $1995. The optional QuickCapture developer's kit is $495 for the base package. OEM discounts are available. Both products are shipping now with five-day delivery.

Data Translation, 100 Locke Dr., Marlboro, MA 01752-1192; (508) 481-3700. **CIRCLE 318**

LISA GUNN

DC/DC Converters Well Done

All DC/DC converters are not created equal. And that can cause problems for the buyer and the design engineer. Our *well done* converters can solve your performance/pricing/delivery frustrations in a hurry.

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We'll make your life easier by getting you the right product, at the right price, with the right performance, and delivery. Time, after time, after time. **That's well done.**

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- Customer Assistance — Toll-free 800 number for immediate answers on pricing, delivery, and OEM contracts.

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We'll help you meet design deadlines and eliminate those product/performance uncertainties. We'll meet and probably exceed your specs, and give you on-time delivery of 100% tested devices that should last for a century or more. Many of our **standard** features turn out to be the expensive **options** from other manufacturers. **That's well done.**

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- Isolation tested up to 8000Vpk.
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We'll also do advanced reliability screening: burn-in, stabilization baking, temperature cycling, and more. Our quality assurance and reliability programs are second to none, and we care. That's important.

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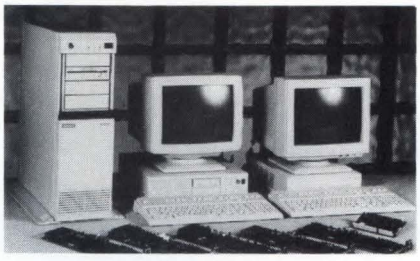
CIRCLE 69

CPU Board Family Lets Users Optimize Systems

A family of PC AT-format add-in cards provides a choice of four CPU cards, add-on option modules and several system chassis. The slot-CPU cards minimize the cost of moving between CPUs by not embedding the video or hard-disk control on the CPU card. The cost is further minimized by offering common interfaces to off-board functions. Desired support functions can be added via



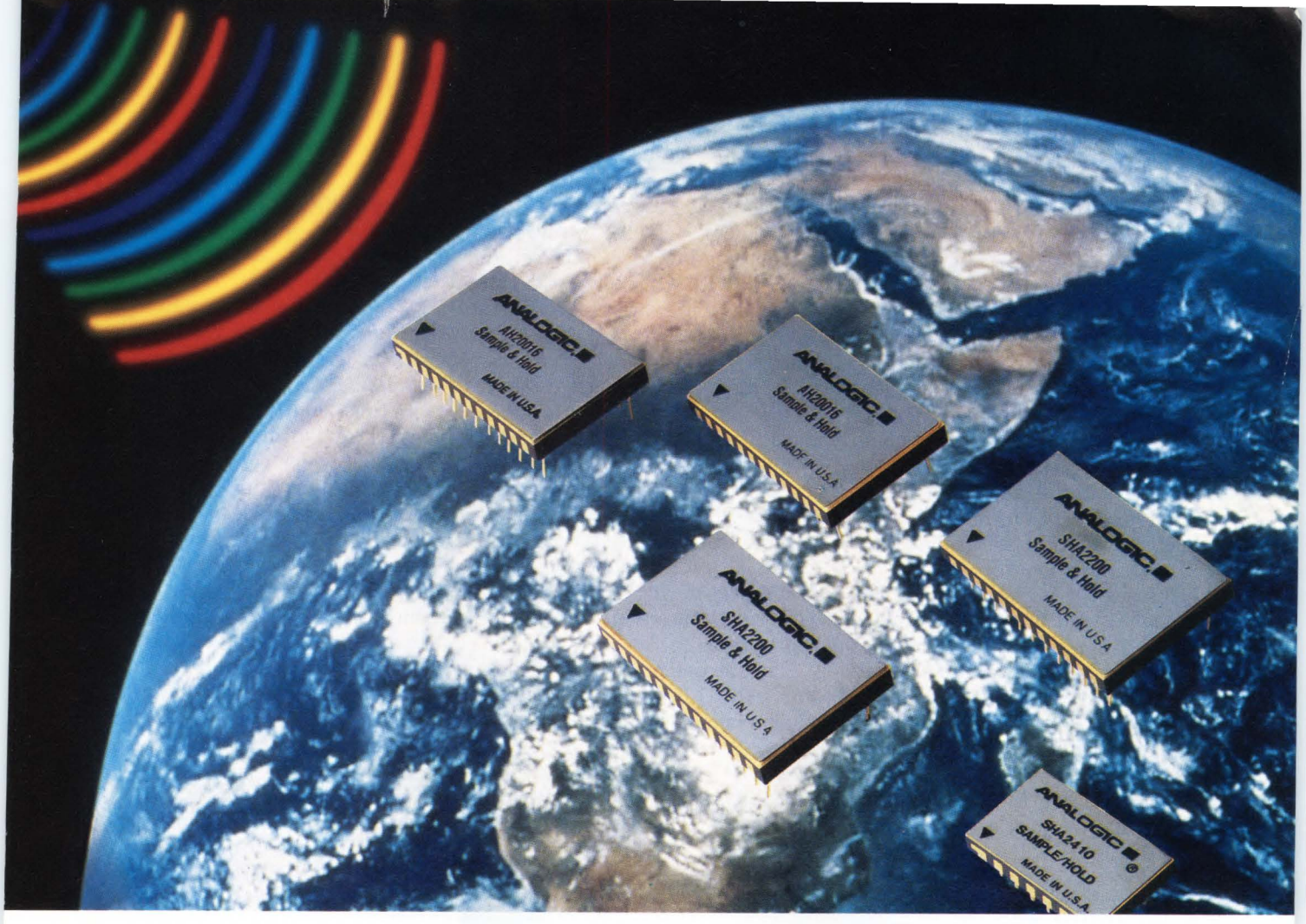
optional daughter modules. The four CPUs start with a 12-MHz 80286-based card that comes with 512 kbytes of RAM (expandable to 4 Mbytes), an 80287 coprocessor socket, floppy disk-drive controller, and three ports (two serial and one parallel). A 16-MHz 80386SX board comes with the same hardware, but packs 1 Mbyte of RAM (expandable to 8 Mbytes) and a socket for the 80387. Adding a 20-MHz 80386DX, the third board comes with 3 Mbytes of RAM, but otherwise has the same features as the SX board.

Siemens Information Systems Inc., 5500 Broken Sound Blvd., Boca Raton, FL 33487; (407) 994-8800. **CIRCLE 338**

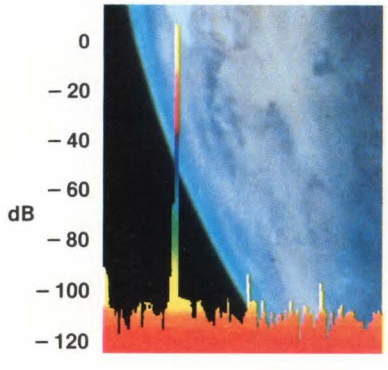
Multiprocessor Board Executes 13 MIPS

Designed for use with PC/M's HyperFlo data-flow computing system, a multiprocessor board provides 13 MIPS and 8 MFLOPS of general-purpose computing power on a single VMEbus card. The MPU-2 is equipped with four 68020 microprocessors, four 68882 floating-point coprocessors, and 1.5 Mbytes of memory. The board sports a three-level multiprocessing structure with a self-contained data-flow operating system. The FLOS operating system accepts general-purpose processors, in addition to DSP and RISC devices in the same system, so the optimum processor type can be employed at the various nodes in a multiprocessor data-flow system. A HyperFlo system can incorporate as many as 100 processors in a single VMEbus card cage. Price of the MPU-2 is $6870 with delivery taking up to 30 days.

PC/M Corp., 6805 Sierra Ct., Dublin, CA 94568; (415) 829-8700. **CIRCLE 339**



Analogic Introduces The World's Quietest S/H Amplifiers



High Speed and Precision in Industry Standard Hybrid Pinouts

Analogic, the world resource for precision signal technology, brings you the quietest, fastest precision sample-and-hold amplifiers available. With noise levels as low as 20 μV rms, Analogic's new family of S/H amplifiers surpasses all others for high speed, high resolution signal processing applications.

Just look at these features. For high performance, the AH20016 offers 500 ns acquisition time, low aperture jitter of 10 ps rms, and $\pm 0.0015\%$ linearity. The SHA2200 is ideal for use with fast, high resolution A/D converters, digitizing signals up to 2 MHz with a low noise of only 30 μV rms. Low cost applications are easily supported by the SHA2410 with excellent linearity of $\pm 0.0015\%$, acquisition time of only 2.5 μs and the lowest noise — 20 μV rms. We offer standard pinouts to ease system integration, off-the-shelf delivery, and the high reliability you only get from hybrids!

The speed and accuracy of Analogic's S/H amplifiers will meet the most demanding OEM applications—wideband data acquisition systems, professional audio encoding, digital telecommunications, automatic test equipment, industrial process control, or nuclear research.

And we put our promises in writing. Every Analogic S/H amplifier is tested on proprietary automatic test systems. The test data shipped with each product guarantees that it meets or exceeds the published specifications. Surprised? Anything less is just a lot of noise.

For Applications Assistance: Richard Lentini
Analogic Corporation, 360 Audubon Road,
Wakefield, MA 01880 (508) 977-3000 x2170
Telex: 466069, Fax: (617) 245-1274

ANALOGIC®

The World Resource for Precision Signal Technology

CIRCLE 70

MONOCHROME DISPLAY BOASTS 4096-BY-3300-PIXEL, 300-DPI RESOLUTION

MegaScan Technology is claiming the world's highest resolution for a monochrome display system with its Document Display System. The display packs 4096 by 3300 pixels onto a 19-in. screen. This adds up to nine times the image density of other high-resolution monitors, and over three times the density of any other commercially available high-end display.

The display is described by the company as the only one to provide 300-dpi resolution, which matches that of today's standard laser printers and scanners. Documents generated or displayed on the DDS screen match printed hard copy dot for dot at an exact 1:1 scale.

Included within the integrated display subsystem are a 19-in., noninterlaced grayscale monitor, interface, video controller with frame buffer, windowing software, and drivers. With 72-Hz refresh rates and a video-data rate of 1.5 GHz, the DDS system delivers a flicker-free display.

The frame buffer holds 2 Mbytes of data, which can make up large document images up to 12 million pixels with space left over for menus, display primitives, and data structures. Using the latest video-RAM technology, the frame buffer is dual ported to provide a 1.5-Gpixel/s bandwidth. As a result, it can refresh the image while simultaneously allowing a fast update rate.

The Document Display System starts at $11,000 in OEM quantities and is available immediately.

MegaScan Technology Inc., 42 South St., Hopkinton, MA 01748-2201; (508) 435-2600. **CIRCLE 319**

DAVID MALINIAK

MULTIPROCESSOR RISC SYSTEM EXECUTES UP TO 160 MIPS, 28 MFLOPS

By moving to Mips Computer Systems' higher-performance R3000 RISC processor, Silicon Graphics has added two server members to its multiprocessor Power series. The top-of-the-line system is the 4D/280S, which can deliver a maximum sustained throughput of 160 MIPS and 28 MFLOPS (double precision) when it packs eight R3000 processors and floating-point units running at 25 MHz. The other new system is the 4D/210S, a single-processor system that delivers 20 MIPS and 3.3 MFLOPS.

Each processor module carries an R3000 RISC CPU, a companion R3010 floating-point processor, a read-write buffer, and 384 kbytes of cache set up in a two-level scheme. Systems come with a minimum of 8 Mbytes of main memory and can be expanded to 128 Mbytes in 8-Mbyte increments.

The multiprocessor systems run IRIX, the company's symmetric multiprocessing implementation of AT&T's Unix operating system. For communicating with mass-storage subystems and other peripherals and systems, the Power series computers include SCSI, VME, and Ethernet interfaces. Up to 4.8 Gbytes of mass storage as well as tape backup can be housed in the Power-series cabinet. Up to 20.8 Gbytes of mass storage can be attached to the system using an optional storage-expansion chassis.

Base price for the 4D/280S with its eight processors is $172,500, while the single-processor 4D/210S sells for $54,900. A graphics-card option for the 4D/210S turns the system into a powerful graphics workstation, the 4D/210GTX, which can display 100,000 independent polygons/s. This is one of the highest display speeds available to date on any system.

Silicon Graphics Inc., 2011 N. Shoreline Blvd., P.O. Box 7311, Mountain View, CA 94039-7311; (415) 960-1980. **CIRCLE 320**

DAVE BURSKY

MULTIPROCESSOR GRAPHICS CONTROLLER LINKS RASTER PRINTERS TO HOST

Multiple processors running in parallel form the heart of a standalone graphics controller from JRL Systems that delivers very-high-speed imaging of graphic element, pure raster, compressed raster, and text data. The 340-RGP controller connects raster printers and plotters to a variety of host systems.

Rasterization and decompression is offloaded from the host to the 340-RGP controller, which directly controls devices such as electrostatic plotters and laser printers.

The 340-RGP controller analyzes the graphic-element list, text, or compressed raster data before passing it to a main processor. It may also

pass the data to one of its specialized preprocessors for computationally-intensive tasks such as CCITT groups three or four.

Input data is processed into a pure raster file and written to a 2- to 64-Mbyte image buffer. The unique image-memory buffering and porting design means that the controller can handle an infinite amount of graphic elements on each picture.

The output module handles the electrical interface to the specific hardcopy devices at speeds of up to 4 Mbytes/s. The controller supports host-output formats such as HP-GL, HP-PCL, Versatec Data Standards Random, CalComp 906/907, KMW-PLT, Trace, CCITT groups three and four, Postscript, and standard print with high-quality character fonts.

The 340-RGP graphics controller is available now. One unit, with no options, costs $5950.

JRL Systems Inc., 6101 West Courtyard Dr., Building 1, Austin, TX 78730; (512) 345-7122. **CIRCLE 321**

LISA GUNN

SCSI-BUS MULTIPLEXER ALLOWS 24 PERIPHERALS TO SHARE THE BUS

Now, a SCSI host or initiator can control more than seven peripherals or target devices. The SM-14 SCSI bus multiplexer is the first scheme in which up to 24 additional SCSI-compatible devices can reside on the bus. The multiplexer uses Ancot's proprietary solid-state switch, which handles all SCSI signals directly with no intervening hardware to degrade signal quality. Additionally, when the multiplexer is used in a SCSI test subsystem, it can decrease the per-test-slot cost, because more units can be tested at one time.

The multiplexer ties into a SCSI initiator over a master SCSI bus, and converts the single bus into four branch SCSI buses. One SCSI identification number is used by the initiator and one by the multiplexer's control unit. That leaves six ID numbers for each of the four branches. Only one branch bus and one device may be switched at a time. The dc impedance between the master and the "on" branch bus is typically 1.8 Ω (5 Ω, maximum), and the capacitance from the master to branch bus is 40 pF. Response time across the switch is just 2 ns.

Indicators on the SM-14's front panel show which SCSI-bus branch is enabled and which branch is busy. A front-panel pushbutton manually selects a branch bus.

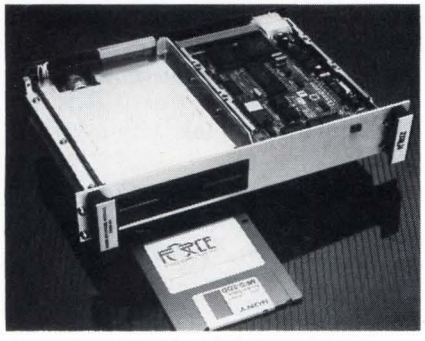
The ac-powered unit comes in a 4-by-10-by-12-in. enclosure, sells for $2840, and is available within 30 days of order.

Ancot Corp. Mid-Peninsula Business Park, 1755 E. Bayshore Rd., Suite 18A, Redwood City, CA 94063; (415) 363-0667. **CIRCLE 322**

DAVE BURSKY

DISK SUBSYSTEM FITS VMEBUS BACKPLANE

A combination hard- and floppy-disk subsystem plugs directly into standard VMEbus backplanes to provide up to 84 Mbytes of formatted Winchester storage and 720 kbytes of formatted floppy capacity. Called the Mass Storage Module (MSM), the unit requires only two 6U slots and is available in two Winchester capacities (42 and 84 Mbytes). The Winchester has an SCSI port, while the floppy employs an SA460 interface. Average access time of the 3-1/2-in. hard-disk drive is 19 ms, with a transfer rate of 2.0 Mbytes/s for asynchronous operations and 4.0 Mbytes/s for synchronous transfers. The 3-1/2-in. floppy drive transfers data at a rate of 250 kbytes/s. The 42-Mbyte version costs $1990 while the 84-Mbyte model sells for $2490. Both versions of the subsystem are available immediately.



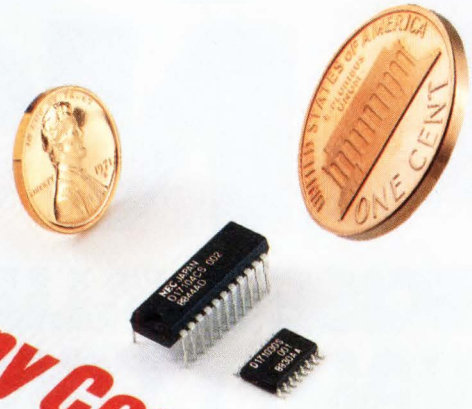
Force Computers Inc., 3165 Winchester Blvd., Campbell, CA 95008; (408) 370-6300. **CIRCLE 340**

OPTICAL DRIVE PERMITS MEDIA INTERCHANGE

A write-once, read-many (WORM) optical disk drive supports the ISO standard cartridge, media, and format to permit media interchangeability. The WM-D070 5-1/4-in. drive operates in either of two modes to accommodate the broadest possible range of applications. For situations requiring broad media interchangeability, the drive operates in a constant-angular-velocity (CAV) mode with ISO format. In this mode, the drive has a 5.5-Mbit/s data transfer rate and a standard storage capacity of 600 Mbytes. For applications where media interchange with non-Toshiba drives is not required, the WM-D070 can operate in a modified constant-angular-velocity (MCAV) mode. Under MCAV, the drive holds 900 Mbytes and achieves a variable transfer rate from 2.6 to 5.2 Mbits/s. The WM-D070 offers a fast 90-ms average seek time and an embedded SCSI port. It sells for $2295 in OEM quantities.

Toshiba America Information Systems Inc., Disk Products Division, 9740 Irvine Blvd., Irvine, CA 92718; (714) 583-3108. **CIRCLE 341**

The 4-bit microcomputer that makes more cents for you.



Tiny Controller

Tiny Controller is a price/ performance breakthrough.

Our new 4-bit CMOS microcomputers are so inexpensive you can install them where microcomputers have never been used before. Put them in fans, food processors, bathroom scales, etc. For a truly nominal cost, you'll boost sales by enhancing consumer appeal. If you're making games or toys, replace your more expensive 4-bit device with our chip and achieve significant savings on every unit.

NEC's Tiny Controllers provide high speed (2μsec cycle time) and ample memory (512 x 16-bit ROM; 16 x 4-bit RAM). With 11 or 16 I/O ports, they permit direct LED drive. They operate on a wide range of voltages: 2.7 to 6.0V. We offer a full set of development tools.

And we're making OTP versions available soon for fast, small-lot production.

Why should you specify our Tiny Controllers? Because their low price will cut your manufacturing expenses and their high performance will expand your market opportunities. If unbeatable price/ performance makes sense to you, call NEC today and ask about our new 4-bit singlechip CMOS microcomputers.

	μPD17103	17107*	17104	17108*
ROM	512 x 16-bit			
RAM	16 x 4-bit			
I/O ports	11		16	
Instruction cycle time	2μs min.			
Oscillation voltage	2.7 – 6.0V			
Standby mode	STOP/HALT			
Oscillation	Ceramic	RC	Ceramic	RC
Package	16-pin shrink DIP/16-pin SOP		22-pin shrink DIP/24-pin SOP	
Onetime PROM	4Q '89	1Q '90	4Q '89	1Q '90

*Under development

For fast answers, call us at:

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NEC

CIRCLE 71

120dB RANGE

FOR PRECISE EVALUATION OF HIGH-QUALITY COMPONENTS

Improve your dynamic range and resolution to match today's high-performance filters, tuners and other components.

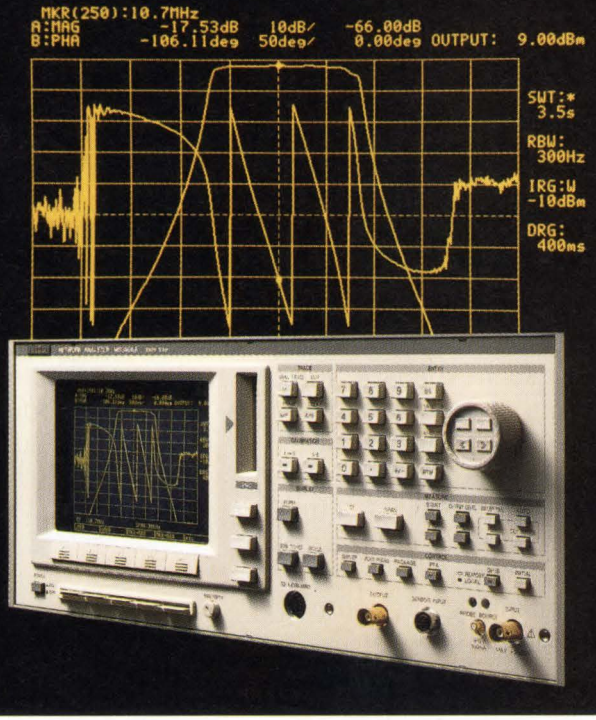
Anritsu's MS3606A Network Analyzer now offers you an amazing 120 dB dynamic range for a clear picture around peak and cutoff frequencies. The fully synthesized signal source provides 1 mHz resolution and dramatic increases in phase/delay-time measurement resolution to give you the best sensitivity and precision for advanced video and mobile-communications components.

With the MS3606A, you can measure at a super-high speed of just 400 μs. The Personal Test Automation (PTA) option gives you faster signal processing and ATE capability to improve productivity. You'll even have the flexibility to transplant program assets from other equipment.

Scalar analysis for complicated tests involving different input and output frequencies is also available, along with conventional vector analysis.

The MS3606A gives you all these features over a wide frequency range of 10 kHz to 1 GHz, for a broad spectrum of applications. And of course, a full selection of peripherals, including equipment for testing analog ICs, is also available.

For R&D or mass production, you'll get the greatest capabilities from Anritsu.



NETWORK ANALYZER MS3606A

Anritsu

ANRITSU CORPORATION 10-27, Minamiazabu 5-chome, Minato-ku, Tokyo 106, Japan Tel. 03-446-1111
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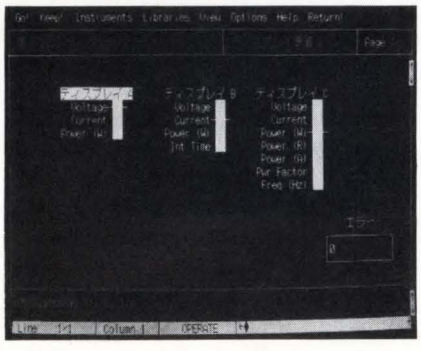
INSTRUMENTS

PACKAGE WRITES INSTRUMENT CONTROL SOFTWARE FOR NEC-9800

National Instruments Corp. has introduced LabWindows 9800, a set of instrumentation programming tools for the NEC PC-9800 personal computer, Japan's most popular DOS-based computer. The package is aimed both at end users who develop test and measurement programs for the PC-9800 and at manufacturers making IEEE-488 instruments for sale in Japan.

LabWindows 9800 uses the Kanji and Kana character sets and works with the Nihongo (Japanese-language) versions of the Microsoft QuickBasic and C high-level programming languages. An interactive development program and a set of functional libraries permit IEEE-488 (GPIB) instrument control, data formatting, analysis, presentation, and file operations.



A function panel serves as an intuitive, full-screen interface for use with the libraries. Users enter the functional parameters that appear as pictorial controls on the panel. These functions can be executed immediately, and the program will automatically generate the source code at the same time.

The package's instrument library contains more than 60 instrument drivers for controlling a wide range of GPIB instruments.

Available immediately, LabWindows 9800 costs about $1200, and the advanced analysis library is available separately for about $1700.

National Instruments Corp., 12109 Technology Blvd., Austin, TX 78727-6204; (512) 794-0100.

CIRCLE 323

JOHN NOVELLINO

20-MHz SCOPE RUNS ON AC, DC, OR BATTERY

Compact enough to fit inside a standard attache case, the Model 1422 dual-trace oscilloscope can be powered from ac, an optional internal battery, or an external 10- to 16-V dc source. The miniature scope features 20-MHz response, 10-mV/division vertical sensitivity, and front-panel X and Y operation. Eighteen sweep ranges span from 1 μs/division to 0.5 s/division in a 1-2-5 sequence, and are variable between ranges. Sweep magnification can be extended to 10 times, pushing the maximum sweep rate to 100 ns/division.

Unlike other portable oscilloscopes, the 1422's battery pack fits entirely within the scope without adding to the depth and height of the case. The instrument is priced at $1099 and comes with two ten-to-one probes.

B&K-Precision, Maxtec International Corp., 6470 W. Cortland St., Chicago, IL 60635; (312) 889-9087.

CIRCLE 342

LOGIC ANALYZERS ADD 400-MSAMPLE/S DIGITAL-SCOPE CAPABILITY

Although a state or timing analyzer can reveal the existence of the typical digital-debug problem, the source of the problem is often related to a parametric fault that must be found with an oscilloscope. For that reason, Hewlett-Packard Co. has added dual-channel digital-oscilloscope capabilities to its HP 1650-series logic analyzers.

The two new additions to the series, the HP 1652B and HP 1653B, offer a 400-Msample/s digitizing oscillosope as well as 80 and 32 logic-analysis channels, respectively. Both analyzers feature 100-MHz timing on all channels. The HP 1652B has 35-MHz state analysis, and the HP 1653B has a 25-MHz state speed. Both oscilloscopes are bandlimited to 100 MHz, one-fourth the sample speed, to prevent aliasing.

The scopes have an advanced logic-triggering set that lets users specify a wide variety of edge and pattern conditions. The analyzers feature complex-state triggering that filters out unnecessary data and lists only desired states. Combining a logic analyzer and scope in one unit allows the timing analyzer, state analyzer, and oscilloscope to show simultaneous, time-correlated displays for all three functions. For example, a glitch from the timing analyzer or address from the state analyzer can trigger the scope.

The HP 1652B costs $11,300, and the HP1653B goes for $7400. Delivery for both is an estimated 8 weeks after receipt of order.

Hewlett-Packard Co., Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80901; (800) 752-0900. **CIRCLE 324**

JOHN NOVELLINO

FREQUENCY SOURCE CLAIMS HIGH ACCURACY

The Wavebox 100 synthesized frequency source boasts 10 ppm or 0.001% accuracy and stability over its 1-Hz to 100-kHz frequency range, three orders of magnitude better than most comparable signal sources. The output frequency is dialed up directly on thumbwheel switches. Resolution is 1 Hz over the entire range. The sine-wave output is variable up to 20 V pk-pk with a ±10-V offset. Total harmonic and nonharmonic distortion is better than 40 dB. An auxiliary TTL/CMOS level square-wave output is also provided. The system is priced at $325.

Teledata Systems, 68 Reservoir Rd., New Milford, CT 06776; (203) 355-8285. **CIRCLE 358**

APPLICATION SPECIFIC PLASTICS FROM PHILLIPS 66

CONNECTING VALUE WITH PERFORMANCE

Performance and value. You can get both with Aspect™ TPPE from Phillips 66. This engineering thermoplastic polyester gives you:

- Improved flow and processability to help you mold complex, intricate parts—easily and precisely, at low injection pressures.
- Long-term thermal performance —retaining over 50% tensile strength after 17 weeks at 220° C.
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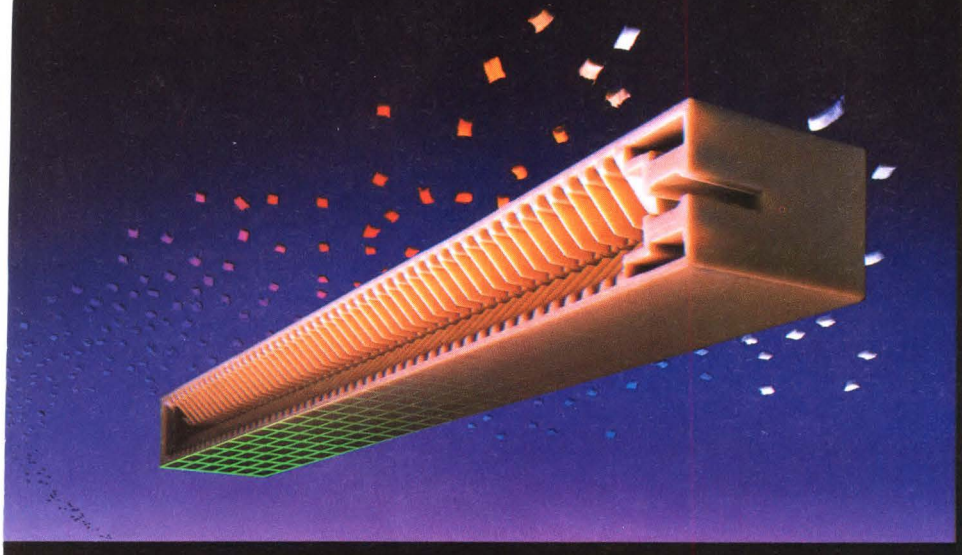
Aspect™ TPPE is ideal for applications such as high density interconnectors; thin, intricate and hard-to-mold bobbins; terminal blocks; and fuse holders.

With Application Specific Plastics such as Aspect™ TPPE from Phillips 66 you can take advantage of the expertise of the Phillips 66 Plastics Technical Center . . . its research and development and advanced molding facilities, the computer-aided design capabilities, the experienced staff, and more.

Phillips 66 offers other Application Specific Plastics for your electrical/electronic needs: Ryton® PPS, Ryton® S PPSS, and Crystalor™ PMP. For more information call toll free ***1-800-53-RESIN***. Or Telex #492455.

CIRCLE 73



ASPECT™ TPPE

PLASTICS WITH POWER TO WIN™

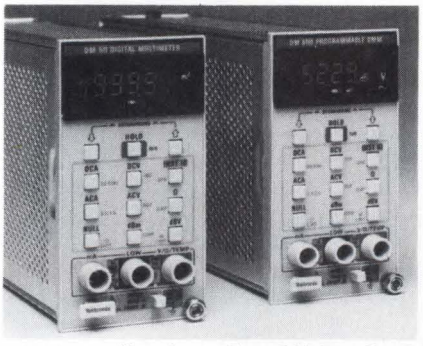
PHILLIPS 66

TWO MODULAR DMMS BOAST FLEXIBLE MEASUREMENT FEATURES

Tektronix has expanded its line of modular digital multimeters by adding the programmable DM 5110 and manual DM 511 instruments. Built in a single-width case, the DM 5110 lets users take advantage of the five remaining slots in the TM 5000 mainframe to create a customized automated test system.

The DM 5110 includes an IEEE-488 interface that makes it fully programmable over the GPIB. The manually operated DM 511 offers a choice of front or rear interface capability.

Besides a wide range of ac and dc voltage and current measurements, the two instruments let users make their measurements directly in dBv and dBm units. This feature adds measurement flexibility and is useful in certain calibration and maintenance applications. In addition, both modules feature a 4-1/2-digit autoranging mode as well as a 3-1/2-digit mode that increases throughput.



To improve the normal-mode rejection ratio, users may choose either a 50- or 60-Hz mode. Front-panel operation is through 12 soft keys that select the function and range. Other standard features include a true RMS function, null and hold modes, and high- and low-pass limit testing and compare mode with beeper.

The DM 5110 costs $895, and the DM 511 is priced at $745. Both may be ordered immediately for delivery in 6 weeks.

Tektronix Inc., P.O. Box 1700, Beaverton, OR 97075; (800) 835-9433. **CIRCLE 325**

JOHN NOVELLINO

Gate to gate service.

Standing under the torii gates of Kyoto, you're a long way from where you began this journey. But United made it easy.

With nonstops to Japan from five U.S. gateways, United gives you the convenience you need, and a level of service that makes passing through a pleasure.

Come fly the friendly skies.

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32-Bit Emulator Handles 33-MHz CPUs Now, 60-MHz Devices Later

The EL 3200 in-circuit emulator from Applied Microsystems not only keeps up with today's 33-MHz, 32-bit microprocessors, but also will work with the 60-MHz devices now being designed. The first probe modules for the EL 3200 support the Motorola 68020 and 68030, including the latter's cache burst and synchronous cycles.

Featuring a new modular architecture, the emulator runs on IBM PCs or Sun workstations, including Sun systems used in standard Ethernet networks with TCP/IP protocols. The EL 3200 sits as a node on the network trunk so no intermediary computer is needed to connect the emulator to the network.

The EL 3200 allows as many access breakpoints as the overlay memory can support. The unit also has six hardware and more than 1000 software execution breakpoints. Since cached instructions may never be executed, the emulator will break when the instruction is pulled from the cache.

Trace memory is an extra large 16 kwords deep by 139 bits wide. A dynamic trace feature lets the operator view captured traces in real time without slowing down the target system. A 512-kbyte overlay is standard, and up to 2 Mbytes is optional.

With 512 kbytes of RAM overlay, the 68020 version of the EL 3200 costs $22,000 and is available immediately. The 68030 system, which will be available next July 30, starts at $26,000 with 512 kbytes of overlay.

Applied Microsystems Corp., 5020 148th Ave. NE, Redmond, WA 98073-9702; (206) 883-3049.

CIRCLE 326

JOHN NOVELLINO

Portable DSO Costs Less Than $2500

A low-cost portable oscilloscope — priced at just $2395 — features digital and analog capabilities, along with a 50-MHz bandwidth and a 20-Msample/s sampling rate per channel. The 2211 also offers 8-bit vertical resolution and a 4k record length per channel. It builds on the feature set of the 2200 series scopes and adds on-screen cursors, a CRT readout, and a hard-copy serial interface. Enhancing accuracy and repeatability, the on-screen cursors provide delta voltage, delta time, and 1/delta time. With the unit's pre- and post-triggering capability, users can view events occurring before and after a trigger event. The 2211 also has dual digitizers for simultaneous acquisition.

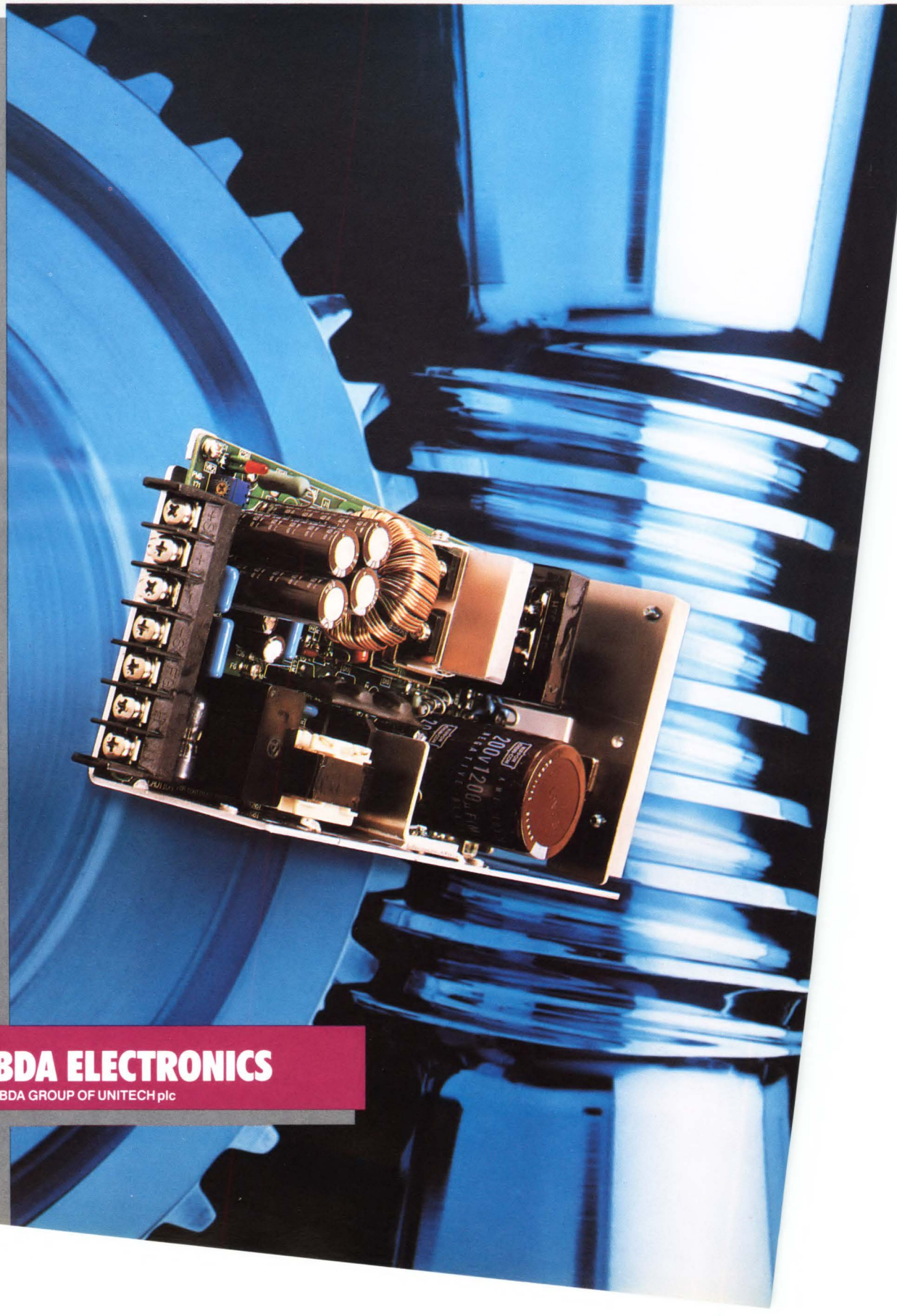
Tektronix Inc., P.O. Box 1700, Beaverton, OR 97075; (800) 426-2200.

CIRCLE 343

FOR LAMBDA, CIRCLE 43 ⟶

LAMBDA'S LS SERIES

Configured To Fit Your Industrial Application.



51 smallest single and triple models.

LAMBDA ELECTRONICS
LAMBDA GROUP OF UNITECH plc

LS SERIES:

TEN PACKAGE SIZES OFFER COMPACT, LOW COST SOLUTIONS FOR ALL YOUR LOW POWER APPLICATIONS

Single Output.

	MAX CURRENT AT AMBIENT OF (A) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 10	QTY. 25	QTY. 100	QTY. 250	QTY. 1000	MODEL
5V ±5% ADJ.	2.0	2.0	1.00	1.22 × 2.91 × 2.83	$ 49	$ 46	$ 43	$ 35	$ 26	$ 23	**LSS-34-5**
	3.0	3.0	1.50	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-5**
	5.0	5.0	2.50	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-5**
	10.0	10.0	5.00	1.54 × 3.74 × 4.72	117	112	106	88	64	58	**LSS-37-5**
	20.0	20.0	10.00	2.17 × 3.74 × 6.30	166	158	150	135	104	95	**LSS-38-5**
	30.0	30.0	15.00	2.56 × 3.74 × 7.09	237	226	215	165	141	129	**LSS-39-5**
6V ±5% ADJ.	1.7	1.7	0.85	1.22 × 2.91 × 2.83	49	46	43	35	26	23	**LSS-34-6**
	2.5	2.5	1.25	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-6**
	4.2	4.2	2.10	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-6**
	8.4	8.4	4.20	1.54 × 3.74 × 4.72	117	112	106	88	64	58	**LSS-37-6**
	17.0	17.0	8.50	2.17 × 3.74 × 6.30	166	158	150	135	104	95	**LSS-38-6**
	25.5	25.5	12.50	2.56 × 3.74 × 7.09	237	226	215	165	141	129	**LSS-39-6**
12V ±5% ADJ.	0.9	0.9	0.45	1.22 × 2.91 × 2.83	49	46	43	35	26	23	**LSS-34-12**
	1.3	1.3	0.65	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-12**
	2.1	2.1	1.05	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-12**
	4.2	4.2	2.10	1.54 × 3.74 × 4.72	117	112	106	88	64	58	**LSS-37-12**
	8.5	8.5	4.25	2.17 × 3.74 × 6.30	166	158	150	135	104	95	**LSS-38-12**
	12.5	12.5	6.25	2.56 × 3.74 × 7.09	237	226	215	165	141	129	**LSS-39-12**
15V ±5% ADJ.	0.7	0.7	0.35	1.22 × 2.91 × 2.83	49	46	43	35	26	23	**LSS-34-15**
	1.0	1.0	0.50	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-15**
	1.7	1.7	0.85	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-15**
	3.4	3.4	1.70	1.54 × 3.74 × 4.72	117	112	106	88	64	58	**LSS-37-15**
	7.0	7.0	3.50	2.17 × 3.74 × 6.30	166	158	150	135	104	95	**LSS-38-15**
	10.0	10.0	5.00	2.56 × 3.74 × 7.09	237	226	215	165	141	129	**LSS-39-15**
24V ±5% ADJ.	0.5	0.5	0.25	1.22 × 2.91 × 2.83	49	46	43	35	26	23	**LSS-34-24**
	0.7	0.7	0.35	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-24**
	1.1	1.1	0.55	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-24**
	2.1	2.1	1.05	1.54 × 3.74 × 4.72	117	112	106	88	64	58	**LSS-37-24**
	4.5	4.5	2.25	2.17 × 3.74 × 6.30	166	158	150	135	104	95	**LSS-38-24**
	6.5	6.5	3.25	2.56 × 3.74 × 7.09	237	226	215	165	141	129	**LSS-39-24**
28V ±5% ADJ.	0.4	0.4	0.20	1.22 × 2.91 × 2.83	49	46	43	35	26	23	**LSS-34-28**
	0.6	0.6	0.30	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-28**
	0.9	0.9	0.45	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-28**
	1.8	1.8	0.90	1.54 × 3.74 × 4.72	117	112	106	88	64	58	**LSS-37-28**
	3.8	3.8	1.90	2.17 × 3.74 × 6.30	166	158	150	135	104	95	**LSS-38-28**
	5.5	5.5	2.75	2.56 × 3.74 × 7.09	237	226	215	165	141	129	**LSS-39-28**
48V ±5% ADJ.	0.2	0.2	0.10	1.22 × 2.91 × 2.83	49	46	43	35	26	23	**LSS-34-48**
	0.3	0.3	0.15	1.42 × 2.91 × 3.35	57	54	51	44	31	28	**LSS-35-48**
	0.5	0.5	0.25	1.54 × 2.91 × 4.13	87	83	79	60	48	38	**LSS-36-48**

Triple Output.

	VOLT Vo	MAX OUTPUT CURRENT (AMPS) 40°C	50°C	60°C	MAX OUTPUT POWER (WATTS) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 10	QTY. 25	QTY. 100	QTY. 250	QTY. 1000	MODEL
$5V^{+0.3}_{-0}$ V ADJ., ±12V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	$130	$124	$118	$ 84	$ 71	$ 66	**LST-37-133**
	+12	1.50	1.50	0.97											
	−12	0.50	0.50	0.32											
	5	8.00	8.00	5.20	76	76	49.4	1.61 × 3.74 × 6.89	161	154	146	108	95	86	**LST-38-133**
	+12	3.20	3.20	2.00											
	−12	0.50	0.50	0.32											
	5	13.00	13.00	8.45	101	101	65.6	1.93 × 3.74 × 7.48	186	178	169	129	117	106	**LST-39-133**
	+12	4.00	4.00	2.60											
	−12	1.00	1.00	0.65											
	+5*	20.00	20.00	13.60	160	160	125.6	1.93 × 3.74 × 10.24	243	232	220	179	159	145	**LST-40-133**
	+12	5.00	5.00	3.40											
	−12	2.00	2.00	1.40											
$5V^{+0.3}_{-0}$ V ADJ., ±15V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	130	124	118	84	71	66	**LST-37-144**
	+15	1.20	1.20	0.78											
	−15	0.50	0.50	0.32											
	5	8.00	8.00	5.20	75	75	49.0	1.61 × 3.74 × 6.89	161	154	146	108	95	86	**LST-38-144**
	+15	2.50	2.50	1.60											
	−15	0.50	0.50	0.32											
	5	13.00	13.00	8.45	103	103	67.0	1.93 × 3.74 × 7.48	186	178	169	129	117	106	**LST-39-144**
	+15	3.20	3.20	2.00											
	−15	1.00	1.00	0.65											
	+5*	20.00	20.00	13.60	160	160	129.5	1.93 × 3.74 × 10.24	243	232	220	179	159	145	**LST-40-144**
	+15	4.00	4.00	2.70											
	−15	2.00	2.00	1.40											
$5V^{+0.3}_{-0}$V ADJ., +12V − 5V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	130	124	118	84	71	66	**LST-37-131**
	+12	1.50	1.50	0.97											
	5	0.50	0.50	0.32											
	5	8.00	8.00	5.20	72.50	72.50	46.5	1.61 × 3.74 × 6.89	161	154	146	108	95	86	**LST-38-131**
	+12	3.20	3.20	2.00											
	5	0.50	0.50	0.32											
	5	13.00	13.00	8.45	94	94	61.0	1.93 × 3.74 × 6.89	186	178	169	129	117	106	**LST-39-131**
	+12	4.00	4.00	2.60											
	5	1.00	1.00	0.65											
	+5*	20.00	20.00	13.60	160	160	120.8	1.93 × 3.74 × 10.24	243	232	220	179	159	145	**LST-40-131**
	+12	5.00	5.00	3.40											
	−5	2.00	1.40	1.40											

*Output 1 requires a minimum load of 3.0 amps.

LS SERIES

Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line ..... 0.4% for input variations from 85 to 132VAC or 132 to 85VAC.

regulation, load ..... 0.8% for load changes from zero to full load and from full load to zero on LSS models. 0.8% for load changes from .75A to full load on main output of LST-37; from 1.5A to full load on main output of LST-38, LST-39; from 3.0A to full load on LST-40. 150mV max from zero to full load and full load to zero on auxiliary outputs of LST-37, 38, 39, 40 with main output preloaded.

ripple and noise. ..... 15mV RMS for all models; 120mV pk-pk for 5V and 6V models; 150mV pk-pk for 12V and 15V models; 200mV pk-pk for 24V and 28V models.

temperature coefficient ..... 0.02%/°C.

AC INPUT

line ..... 85 to 132VAC, 47-440Hz.

DC INPUT
110 to 175VDC.

EFFICIENCY
72% typical for 5V LSS models. 70% typical for LST models, and 12V and 15V LSS models. 82% typical on 24V through 48V LSS models.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
0-60°C with suitable derating above 50°C. (65°C operation is possible on LST-40. Consult factory.)

STORAGE TEMPERATURE RANGE
−30°C to +85°C.

OVERLOAD PROTECTION
External overload protection, automatic electronic current limiting circuit, limits output current to a safe, preset value, thereby protecting the load as well as the power supply.

OVERVOLTAGE PROTECTION
Overvoltage protection is standard on all LSS models and on main output of LST Models. If output voltage increases above a preset level, inverter drive is removed.

HOLD UP TIME
5V and 6V LSS models, and all LST models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, nominal output voltage and 100VAC input voltage.

IN-RUSH CURRENT LIMITING
The turn-on in-rush current will not exceed 15A typical on LSS-38, LSS-39; 20A typical on LST-40; 24A typical for LSS-34; 30A typical for LSS-35, LSS-36, LSS-37; 15A typical for LST-38, LST-39; 35A typical on LST-37.

COOLING
Convection cooled, no fans or blowers needed.

DC OUTPUT CONTROLS
Simple screwdriver adjustment.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation for LSS-38 and LSS-39.

INPUT AND OUTPUT CONNECTIONS
All input and output connections are made via barrier strip terminals.

OUTPUT STATUS INDICATOR
LED indicates presence of output voltage on LSS models and 5V output of LST models.

MOUNTING
Two mounting surfaces, two mounting positions. One mounting surface and one mounting position for LSS-39. Some derating may be required in horizontal mounting position.

ISOLATION RATING
2000V RMS input to output.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LSS-34	0.46	0.55	1.22 × 2.91 × 2.83
LSS-35	0.64	0.75	1.42 × 2.91 × 3.35
LSS-36	0.66	0.75	1.54 × 2.91 × 4.13
LSS-37	0.88	1.00	1.54 × 3.74 × 4.72
LST-37	0.93	1.10	1.42 × 3.74 × 6.10
LST-38	1.21	1.41	1.61 × 3.74 × 6.89
LST-39	1.54	1.79	1.93 × 3.74 × 7.48
LSS-38	1.54	1.85	2.17 × 3.74 × 6.30
LSS-39	2.31	2.50	2.56 × 3.74 × 7.09
LST-40	2.70	2.80	1.93 × 3.74 × 10.24

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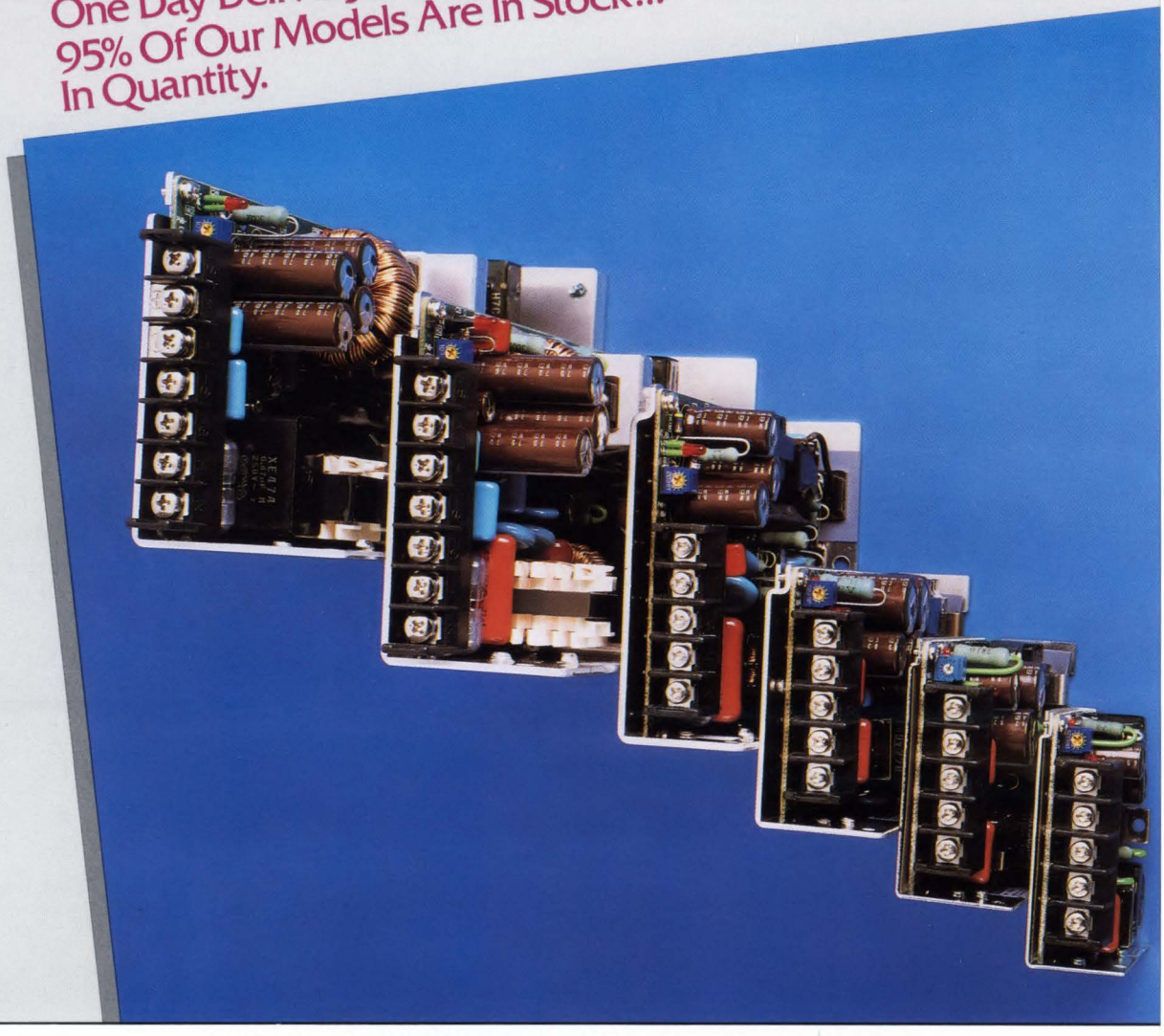

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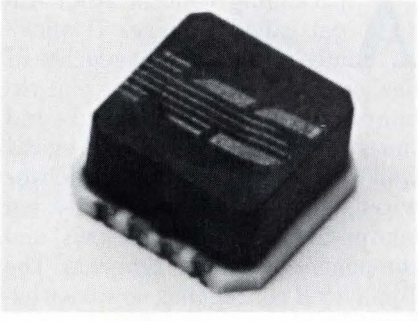
SURFACE-MOUNTED PRESSURE SENSOR BREAKS $2 PRICE BARRIER FOR OEMS



The first commercially available pressure sensor to occupy a surface-mounted package is the model 1431 from IC Sensors Inc. The solid-state, piezoresistive device is meant for high-volume production. Its small size, light weight, low cost, and compatibility with other surface-mounted components make it an attractive option for designers.

Thanks to the surface-mounted packaging, the device goes for under $2 in large quantities, which represents a significant pricing breakthrough. The sensor is based on a family of silicon chips consisting of a chemically micromachined, monolithic silicon diaphragm with a piezoresistive four-arm active Wheatstone bridge.

The device measures just 0.3 by 0.3 in. and weighs 0.3 grams. It is available in absolute pressure ranges of zero-to-15-psi to zero-to-300-psi. Operation is from either a constant-current or constant-voltage supply and accuracy is better than ±0.25%. Typical full-scale output span is 60 mV. Alternate packages are available for applications requiring gage or differential pressure measurement or other pressure ranges.

The model 1431 pressure sensor starts at $16 in sample quantities and falls to below $2 in large OEM lots. Units are shipped in a plastic, antistatic tube compatible with high-volume assembly equipment. Delivery is from stock to 4 weeks after receipt of order.

IC Sensors Inc., 1701 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1800. **CIRCLE 327**

DAVID MALINIAK

INTELLIGENT MODULE CONTROLS COMPLEX STEPPER-MOTOR MOVEMENTS

Control of complex stepper-motor movements can now be accomplished through high-level commands issued by a host computer or retrieved from a built-in, nonvolatile program memory. The GS-C200 is a 38-pin, fully encapsulated stepper-motor controller module from SGS-Thomson Microelectronics. The module has all the necessary interfaces to the host computer, standard sequencers and drivers, and auxiliary functions such as position sensors and limit switches.

Communication with the host computer is performed by means of an RS-232 serial port. The baud rate is programmable between 110 and 9600 bits/s. Commands received from the host may be executed immediately or stored in the internal program memory for subsequent interpretation and execution. The contents of the internal RAM can be transferred to a shadow EEPROM and recalled automatically when power is applied to the module. As a result, the GS-C200 can operate in a standalone mode.

The command interpreter permits motion parameters such as position, direction, speed, and acceleration and deceleration to be directly specified.

The module measures 3.3 by 2.6 by 0.8 in. and comes in a rugged metal package. It costs $115 in quantities of 100. A companion sequencer-driver module, the GS-D200, can be directly connected to the GS-C200 to build a complete stepper-motor controller and driver system. Small quantities are from stock.

SGS-Thomson Microelectronics, 1000 E. Bell Rd., Phoenix, AZ 85022; (602) 867-6100. **CIRCLE 328**

DAVID MALINIAK

HIGH-DENSITY WIRE-WRAP ALTERNATIVE COMES TO PC/AT, VAXBI BUSES

A packaging concept from Augat called Unilayer II alleviates many of the headaches of designing and debugging circuit-board designs. With turnaround times as short as five days, Augat's Quikturn wiring service can deliver wired, socketed, and 100% tested boards from a customer's netlist and component-placement diagram. The Unilayer II concept has now been extended to the PC/AT and VAXBI bus standards.

The concept starts with a board module that features a high-density, plated-thru-hole pattern on a 0.100-by-0.150-in. grid. Voltage and ground planes are individually plated and etched on each side of the double-sided board module. Etched traces connect all I/O configurations to the outer edge of the standard hole pattern.

Then, high-density wiring layers are fabricated using a special process that produces simulated "point-to-point" wiring configurations. This minimizes circuit length, reduces coupling noise, and boosts data-transfer speeds. Each wiring layer is constructed with insulated #38-gage copper wire, so that signal runs can cross over for maximum density. A wiring layer is bonded to each board surface using a thermosetting adhesive to produce the appropriate interconnection pattern.

An automated soldering process joins each wire connecting point to a solder-coated area that's electrically common to the plated-thru hole. Typically, Unilayer II boards are as dense as conventional multilayer boards with six or more layers.

The unwired Unilayer II AT board goes for $79.50 in lots of 100. It holds ninety four 16-pin DIP equivalents. For complete, wired AT boards, prices are about $5000 with five-day turnaround.

Augat Inc., Interconnection Products Group, 33 Perry Ave., P.O. Box 779, Attleboro, MA 02703; (508) 222-2202. **CIRCLE 329**

DAVID MALINIAK

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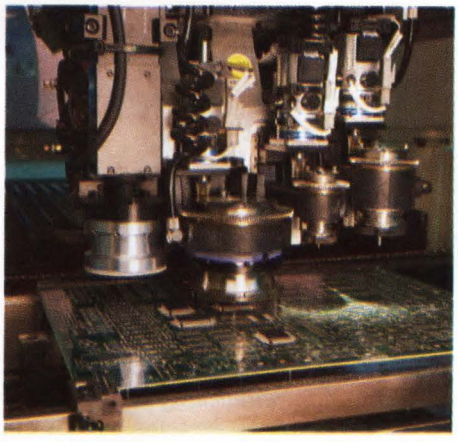

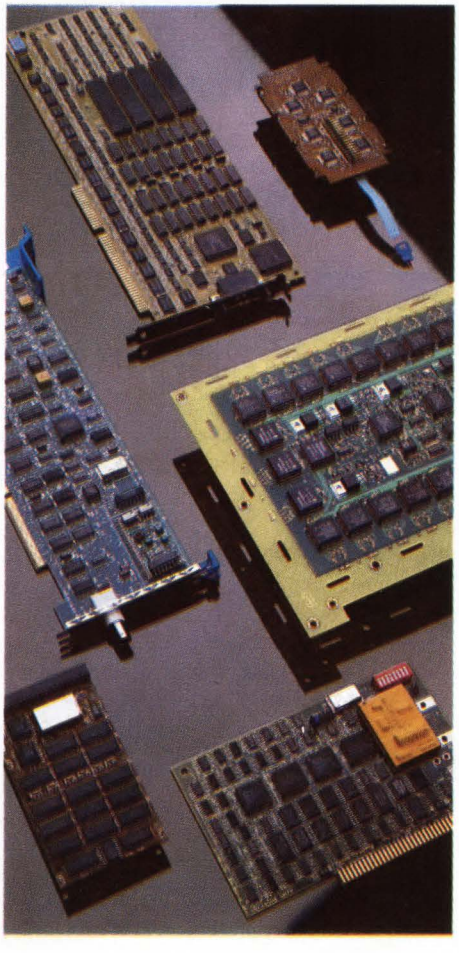

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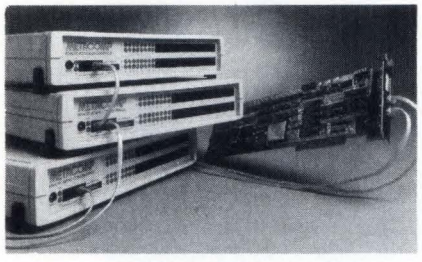
CIRCLE 74

128-Port Serial-I/O Subsystem Links Async Devices To IBM PS/2



From eight to 128 asynchronous devices can be connected to PS/2 Micro Channel systems using an intelligent communication subsystem from Metacomp. The PSconnect subsystem offers a cost-effective means of connecting multiple asynchronous devices such as terminals, printers, and modems to Micro Channel systems while taking up only one slot in the host computer.

Included within the subsystem is an intelligent host adapter that interfaces with the Micro Channel; one or more eight- or 16-channel remote asynchronous concentrators (RACs); and a single RJ-45 twisted-pair cable. The host adapter uses an 80C186 16-bit microprocessor running at 16 MHz. In addition, 512 kbytes of fast dynamic RAM are included for storing data, programs, and transferring information to the host CPU.

The host adapter supports Unix Line Discipline 0 character processing. This reduces the CPU's terminal-I/O overhead and conserves its processing resources for other functions. Moreover, the adapter can operate as a bus master or a slave resource. The master mode supports physical addressing and implements DMA arbitration of the Micro Channel. Connections between one or more host adapters and RACs is provided by a single twisted-pair wire with RJ-45 connectors.

The host adapter with software costs $1835, and the eight- and 16-port RACs go for $625 and $787, respectively. Delivery is from stock.

Metacomp Inc., 15175 Innovation Dr., Building A, San Diego, CA 92128; (619) 673-0800. **CIRCLE 330**

DAVID MALINIAK

Short-Haul Four-Port Multiplexer Moves Data At 38.4 kBits/Second

The industry's first short-haul multiplexer to provide serial asynchronous RS-232 or RS-423 communications between computers and remote terminal clusters at twice the old limit of 19.2 kbits/s is now available. Telebyte Technology's model 575 Super Mux sustains the four-port, 38.4-kbit/s transmission to 1500 ft., or about six city blocks.

By supporting four remote-terminal devices through a single four-wire composite link, the model 575 multiplexer reduces data-communication bottlenecks. It can transmit four ports worth of data over one existing set of wires to enable three additional terminal devices to be added to a site that had previously supported only one.

The 38.4-kbit data-transfer rate can give remote terminals near-instant access to the number-crunching capability of VAX-level host computers. VAX-hosted terminals can achieve performance that approaches that of a workstation. This high-speed capability translates into cost and performance advantages compared with ordinary PCs in local-area networks.

Asynchronous, full-duplex data is transmitted over dedicated in-plant wiring, rather than dial-up phone lines, to remote terminal clusters. In addition, the multiplexers can be reconfigured by jumpers to provide four-port connectivity to 5000 ft. at the reduced data rate of 19.2 kbits/s.

Separate Transmit and Receive data indicators are provided for each of the four ports, plus LED indicators for Remote Test and Error. A pair of front-panel switches controls local-loopback and remote-test operations for 100% verification of each multiplexer in a full-duplex link.

The model 575 multiplexer goes for $385 in quantities up to nine. Delivery is stock to 3 weeks.

Telebyte Technology Inc., 270 E. Pulaski Rd., Greenlawn, NY 11740; (800) 835-3298. **CIRCLE 331**

DAVID MALINIAK

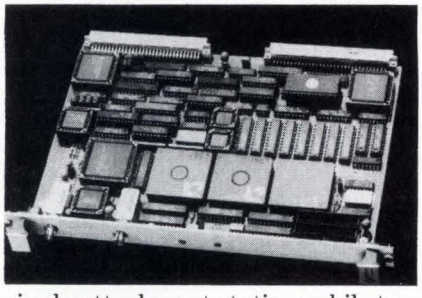
Fast Controller Links VME Workstations To FDDI Network

A high-speed controller for a VMEbus-based computer system allows up to 500 workstations to be connected to a 100-Mbit/s Fiber Distributed Data Interface (FDDI) local-area network. The data path may be up to 100 km. The Interphase V/FDDI 3211 Falcon is designed for applications such as real-time graphics, back-end networks, and backbone networks.

According to the company, the need for a second-generation network such as FDDI is now emerging. Input and output capabilities in general, and networking in particular, have not kept pace with increasing computer power. Since Ethernet's introduction ten years ago, throughput from one node to another has remained relatively unchanged.

Designed to meet the ANSI FDDI specifications and the U. S. Navy's SAFENET II specification, the 3211 Falcon is packaged on a standard double-height, 6U VME pc board. A custom-designed DMA-controller chip moves data to and from a 256-Kbyte buffer memory. Because the Falcon can transfer data over the VMEbus at 100Mb/s, it does not monopolize the VMEbus. As a result, other modules in the computer system have adequate access to the bus.

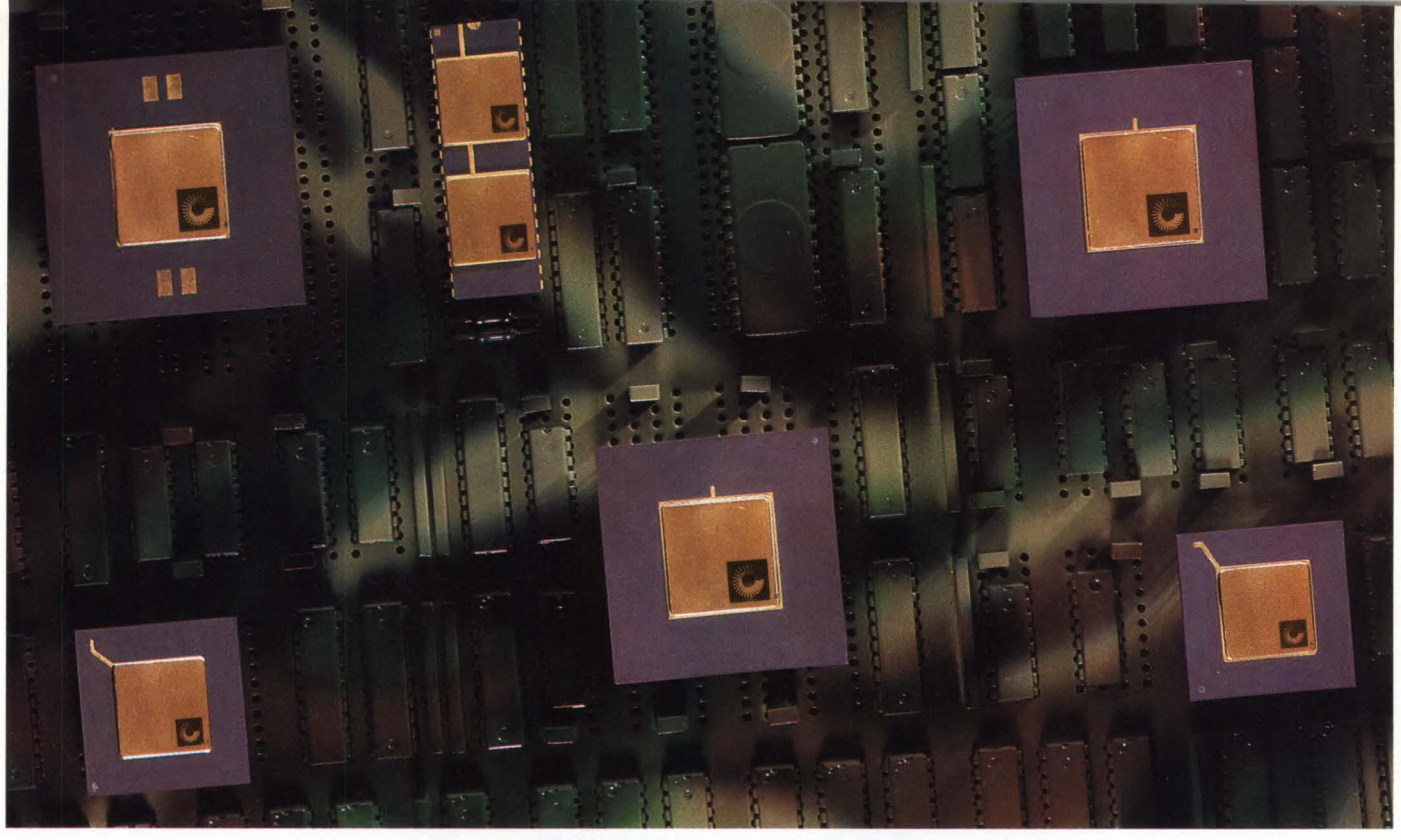
One Falcon functions as an FDDI



single-attachment station, while two can be configured in a system for a dual-attachment station. Available in the fourth quarter of 1989, the V/FDDI 3211 Falcon Controller costs $8000 apiece.

Interphase Corp., 13800 Senlac, Suite 300, Dallas, Texas 75234; (214) 350-9000. **CIRCLE 332**

JON CAMPBELL



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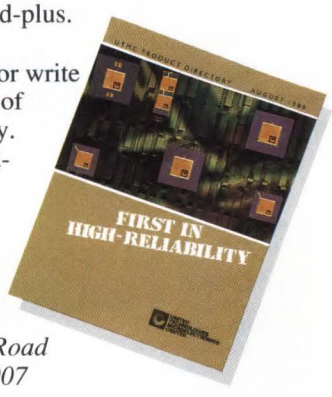

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CIRCLE 107

REVAMPED Z8000 CPUS USE CMOS, AIM AT EMBEDDED-SYSTEM TASKS

With a family of microcontrollers based on CMOS versions of its 16-bit NMOS Z8000 CPU, Zilog is taking aim at the embedded-control market. In the Z16 family, the CMOS Z8000 core will be surrounded by a superintegration bus that accepts an expandable register file, as well as high-speed peripheral functions. When the register banks are integrated on the chip, context switches can take place in less than 1 μs. Such chips are planned for release in 1990.

The processor can operate at clock rates of 10, 12.5, and 16 MHz, and its hardwired, rather than microcoded, instruction set lends the processor to tackling real-time applications.

Initially, there will be three CPU-only members of the family: the Z16C01, 16C02, and 16C03. All three are basically the same chip, but with different addressing ranges to suit different applications and board-space requirements. The 16C01 directly addresses 8 Mbytes and comes in a 48-pin DIP, while the 16C02 addresses 64 kbytes and comes in either a 40-pin DIP or 44-lead plastic leaded chip carrier. The 16C03 addresses up to 2 Mbytes and comes in a 44-lead PLCC.

To reduce some of the system glue that often surrounds the Z8000, Zilog has also come up with the Z16C20, a general logic-support chip housed in an 84-lead PLCC.

Prices for the Z16C01, 02, and 03 are the same—$9.60 in quantities of 1000. The Z16C20 sells for $7.95 in similar quantities. Samples are available from stock.

Zilog Inc., 210 Hacienda Ave., Campbell, CA 95008; (408) 370-8000.

CIRCLE 333

DAVE BURSKY

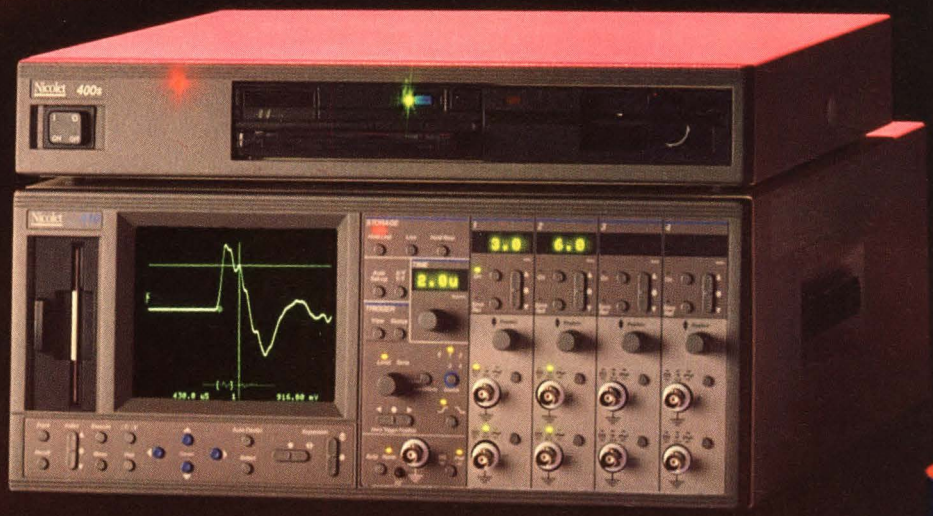
1K SERIAL EEPROM OFFERS 3-V OPERATION

In addition to standard 5-V operation, the XL93CS46 1-kbit serial EEPROM supports a low-power 3-V operating mode. In this mode, the device consumes only 2 mA operating with CMOS inputs and 2 μA on standby. It provides 16-bit data registers, accessible through a serial data input pin and a serial data output pin. It comes in an 8-pin plastic DIP, as well as a small-outline configuration. Shipped from stock, the XL93CS46 is priced at under $2 in lots of 1000 units.

Exel Microelectronics Inc., 2150 Commerce Dr., P.O. Box 49007, San Jose, CA 95161; (408) 432-0500.

CIRCLE 357

THE SHAPE OF THE FUTURE



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INSTRUMENTS OF DISCOVERY

CIRCLE 75

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CIRCLE 76

32-Bit LAN Coprocessors Relieve Host CPUs Of Media-Access Control

A family of three 32-bit local-area-network coprocessors interface with Intel microprocessors and perform all CSMA/CD (carrier-sense multiple-access with collision detection) functions. The devices serve workstations, file servers, and minicomputers interconnected in standard networks. Connected directly to the system bus and using the same bus-interface signals as the host processor, each coprocessor off-loads medium-access-control (MAC) functions from the host CPU and transfers data at the full system and network data rate. In doing so, it uses as little as 2% of the system-bus capacity.

Besides the IEEE 802.3 type 10Base5 (Ethernet) standard, the 82596 family supports 10Base2 (Cheapernet), 1Base5 (StarLAN), the proposed 10Base-T and 10Base-F LAN standards, and proprietary CSMA/CS networks. Data rates are as high as 20 Mbits/s for interconnection applications such as network bridges, gateways, repeaters, routers, and protocol engines. Each chip includes burst bus-data transfer, isolation of the network-interface system by means of a 192-byte internal FIFO, a bus master with bus throttling and direct memory access, and network and self-diagnostics.

The principal difference between the three chips is the timing and signal formats of their 32-bit interface circuitry. With a 105.6-Mbyte/s bus bandwidth, the 82596CA is optimized for use with Intel's 25-MHz i486 32-bit microprocessor and 80960 embedded controller. The 66-Mbyte/s 82596DX interface replicates that of the 25- and 33-MHz i386DX 32-bit microprocessor. The 5-V, CHMOS chips come in 132-pin plastic quad flat packs and pin-grid arrays. The 82596CA, DX, and SX are priced at $88, $65, and $53, respectively, in quantities of 1000.

Intel Corp., P.O. Box 58065, 3065 Bowers Ave., Santa Clara, CA 95051; (800) 548-4725. **CIRCLE 334**

MILT LEONARD

RAM Controller Supports All Densities

A CMOS dynamic RAM controller offers features that make it ideal for mid- to high-end memory subsystems using 16-, 20-, and 25-MHz, 16- or 32-bit conventional microprocessors and RISC processors. The Am29C668 Configurable Dynamic Memory Controller (CDMC) supports all dynamic RAM densities currently available and allows future growth to the 4-Mbit level. In addition, it can directly control and drive up to 16 Mbytes of memory. The device's programmable burst-block mode enables the controller to supply bursts of data from memory at over 39 MHz when the microprocessor indicates the starting address. Its cache mode allows the microprocessor to access a page of dynamic RAM as if it were a cache memory with on-chip row and bank comparators. Housed in a 68-pin PLCC, the Am29C668 costs $24.95 in lots of 100. PGA packages are also available. Delivery takes two weeks.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, CA 94088; (408) 732-2400. **CIRCLE 344**

Clock Driver Shaves Timing-Signal Skew

A clock-driver IC yields an extremely low skew among its four differential-output drivers, which are driven from a single differential-input clock signal. The maximum skew of the four output clock signals is guaranteed to be no more than 75 ps from each other. What's more, the propagation delay from input to output through any of the four drivers varies only ±100 ps over the full operating temperature range of 0° to 85°C. The device, designated the 100115SC, eases the task of distributing multiple timing signals in high-performance ECL systems. It comes in a 16-lead dual-in-line plastic SOIC configuration. Pricing is $13.70 each in lots of 100.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-2862. **CIRCLE 345**

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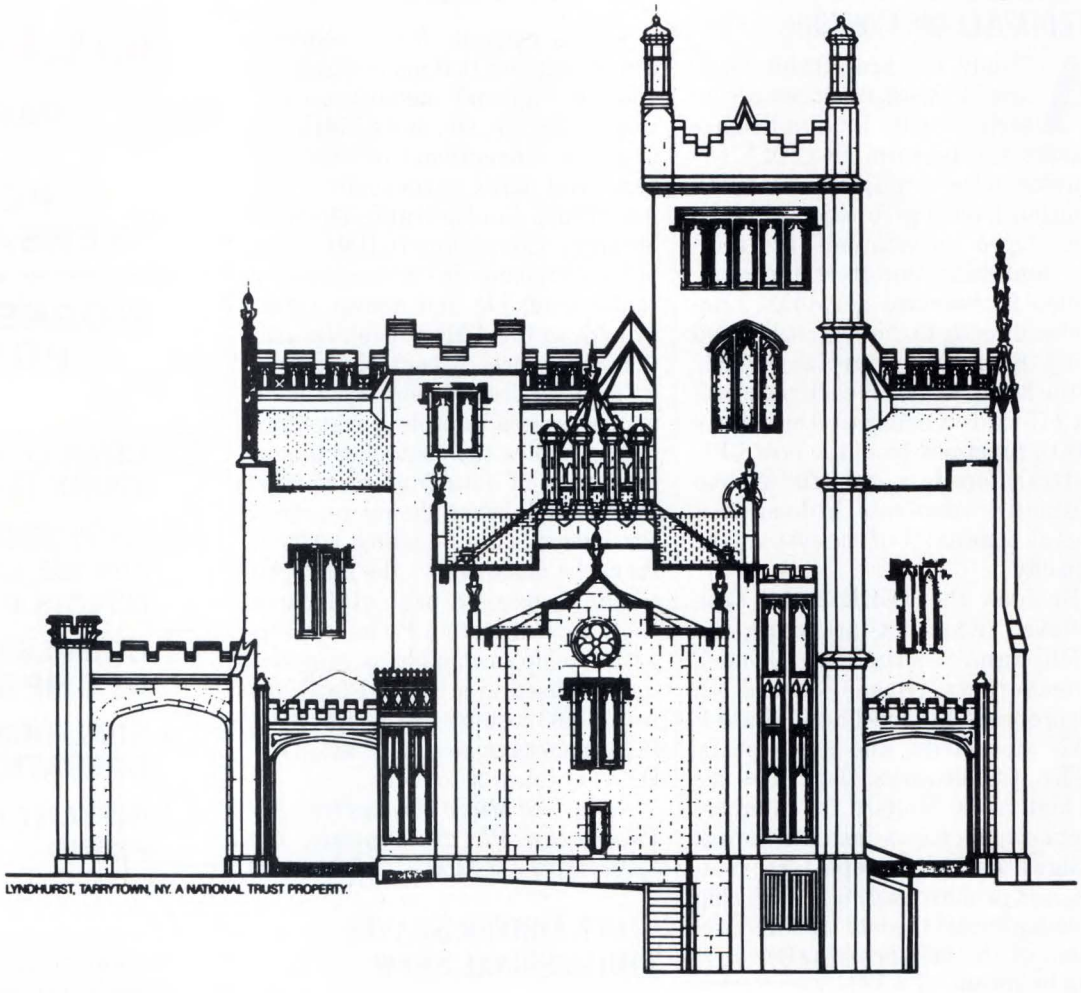

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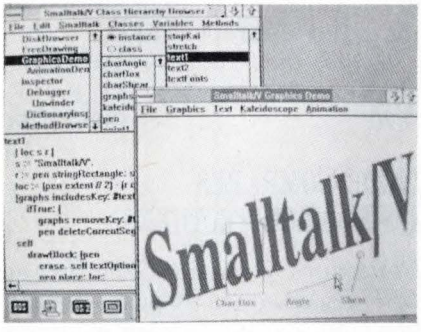


To fuel the gathering momentum of object-oriented programming (OOP), Digitalk Inc. has released Smalltalk/V PM, an OOP development environment that is fully integrated with Microsoft's OS/2 Presentation Manager. The software will be useful to developers who are prototyping applications that depend heavily on their user interface, such as data-base front ends and CASE tools.

Because of its integration with Presentation Manager (PM), Smalltalk/V PM offers easy and complete access to all PM objects, including windows, menus, dialog boxes, and scroll bars. In addition, the software simplifies some of PM's more complex features. For example, its dynamic data-exchange capabilities allow data to be linked to other applications with minimal programming.

The software can be ported to a Macintosh computer and can be integrated with other languages. A powerful pushbutton source-level debugger gives users the ability to set breakpoints or single-step through code to inspect and change objects.

Smalltalk/V PM requires an IBM PC AT, PS/2, or 80286/386-compatible computer and OS/2 Presentation Manager 1.1 or later. A Look and Feel kit is included so users can connect and optimize a mouse. An extensive user manual and a tutorial for learning OOP is also included. The software sells for $499.95 and is available immediately.

Digitalk Inc., 9841 Airport Blvd., Los Angeles, CA 90045; (213) 645-1082. **CIRCLE 335**

RICHARD NASS

Software Optimizes Telecomm Tester

New software packages for the MGTS SS7 communication test system provide user options for message administration and enhance pre-cutover testing. The Message Administration Procedures (MAP) program lets users set up, modify, save, and download SS7 messages. It also provides a complete description of each message type, message parameter, field name, and field values. The User-Defined Sequence (UDS) module defines any sequence of steps to be followed in sending, receiving, and responding to messages by the MGTS service switching points (SSP) ISDN-UP and SSP Telephone User Part (TUP) applications. Another module, the User Application Interface (UAI), receives messages from an external application and routes and transmits them to one of 15 SS7 links. Finally, the ISDN-UP Loopback software enables a single switch-under-test to complete interoffice calls to itself using SS7 signaling. Pricing starts at $2000. Delivery takes 90 days.

Tekelec, 26580 W. Agoura Rd., Calabasas, CA 91302; (800) 835-3532 or (818) 880-7900. **CIRCLE 346**

Software Works With HP Logic Analyzer

The latest module in TSSI's Test Development Series (TDS) system expands applications for the Hewlett-Packard 16500A logic analyzer. The WaveGrabber module creates a bidirectional link between the TDS waveform data base and the 16500A. With it, simulation data can be used to generate programs for the analyzer, verify the accuracy of models, debug prototypes, and assist in system integration debugging. It can also be used to acquire data from correctly operating circuits to develop test programs for ASICs, clusters, and boards. WaveGrabber costs $29,000. Current TDS users can upgrade to include the WaveGrabber capability.

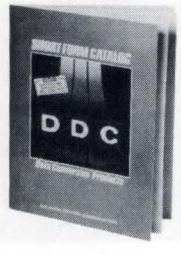
TSSI, 8205 S.W. Creekside Pl., Beaverton, OR 97005; (503) 643-9281. **CIRCLE 347**

BROCHURE DEPICTS SOLDERLESS TERMINALS

A 72-page catalog furnishes information on a full line of solderless terminals and splices, quick disconnects, terminal block hardware, cable ties, and application tooling. Technical data is provided, along with ordering information.

Molex-ETC, 4820 Park Blvd., Pinellas Park, FL 34665; (800) 237-8905 or (813) 541-4651. **CIRCLE 348**

DATA-CONVERSION AND MIL-STD-1553 DEVICES



Used as a quick design reference, this condensed catalog describes over 100 new and standard hybrid and discrete data-conversion and mil-std-1553 products. It lists the specifications and technical data for analog-to-digital converters, digital-to-analog converters, synchro-to-digital converters, digital-to-synchro converters, and mil-std-1553 data bus devices. The bulletin also covers sample-and-hold and track-and-hold amplifiers, as well as synchro and resolver instruments and 1553 testers. Unique to this edition are newly expanded sections on power and memory hybrids and systems.

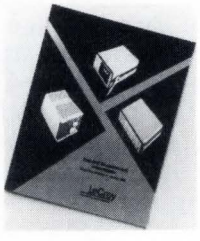
ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 567-5600. **CIRCLE 349**

SYNCHRO-DIGITAL CONVERTER TESTING

A four-page application note, entitled *Testing of S/D Converters*, expands upon the testing procedures of today's synchro-to-digital converters. Converter testing is no longer a straightforward procedure; the device must be tested according to the system in which it operates. The bulletin goes on to outline and define synchro-to-digital converter testing as it pertains to digital angle transfer rate, velocity rate and requirements, and special function and associated timing. Diagrams are used to illustrate circuits that allow for testing of digital outputs and inputs, as well as special functions of the converter.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 567-5600. **CIRCLE 350**

INSTRUMENTS AID TEST AND MEASUREMENT



This condensed catalog of LeCroy's test and measurement products gives an up-to-date inventory of premium instruments that integrate quality, precision, innovation, and speed of data conversion. Included in the brochure are descriptions of signal sources, digital oscilloscopes, and high-speed waveform digitizers.

LeCroy Corp., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977; (914) 425-2000. **CIRCLE 352**

SYNCHRO CONVERTER GIVES 0.0004° ACCURACY

A two-speed synchro(resolver)-to-digital converter that delivers 0.0004° accuracy and 22-bit resolution is the subject of a comprehensive 20-page data sheet. In addition to the usual feature, description, specification, and ordering information, this publication includes a wealth of application information, as well as theory of operation.

Natel Engineering Co. Inc., 4550 Runway St., Simi Valley, CA 93063; (805) 581-3950. **CIRCLE 353**

SELECTING THE RIGHT FIBER-OPTIC LINK

With the help of a new selection guide, choosing the right fiber-optic link to solve high-voltage isolation, ground-loop, or noise pick-up problems is as easy as five simple steps. The brochure describes how to select a fiber-optic link based on the most important considerations for applications in measurement, control, and communications. Background is provided on the advantages of a fiber-optic solution and how fiber-optic links are used. Tables assist the user in selecting the appropriate model for the intended application.

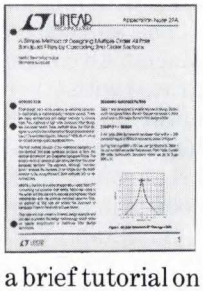
Dymec Inc., 8 Lowell Ave., Winchester, MA 01890; (617) 729-7870. **CIRCLE 354**

NOTE COMPARES DSP ARCHITECTURES

Considerations for Selecting a DSP Processor, a 16-page application note, explains five key elements for choosing between the many high-performance digital-signal-processor and microcontroller architectures currently available. The five parameters discussed include fast and flexible arithmetic, extended dynamic range on multiply-accumulates, single-cycle fetch of two operands (both on- and off-chip), hardware circular buffers, and zero-overhead looping. Based on those elements, the note compares two fixed-point processors: the ADSP-2100A from Analog Devices and Texas Instruments' TMS320C25.

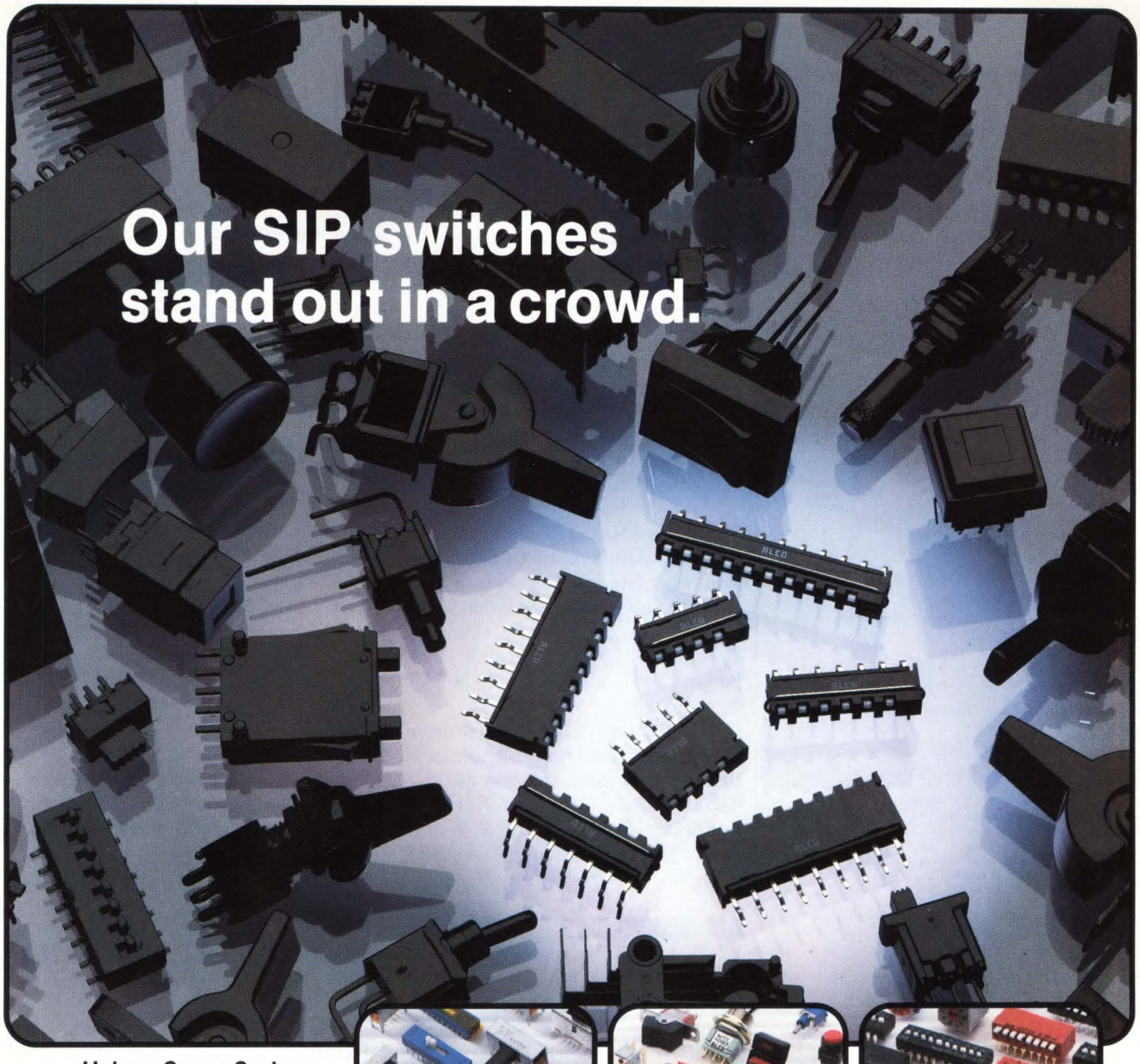
Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 02021; (617) 329-4700. **CIRCLE 355**

GUIDE TO DESIGNING BANDPASS FILTERS



A simple method of designing multiple-order all-pole bandpass filters by cascading second-order sections is the topic of discussion in application note AN27A. It includes a brief tutorial on bandpass filter theory, along with hardware implementation of designs, and tables useful in the design of Butterworth and Chebyshev bandpass filters. The brochure also describes the factors involved in deciding between Butterworth and Chebyshev filter approaches.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (800) 637-5545. **CIRCLE 356**



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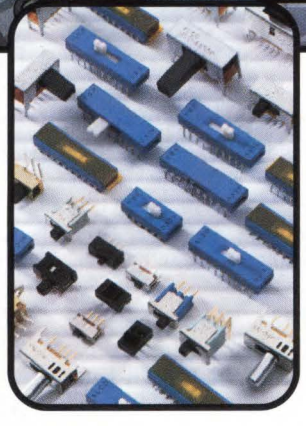

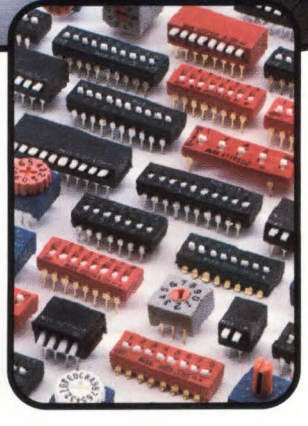

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UPCOMING MEETINGS

OCTOBER

CASExpo-Fall '89, October 23-27. San Francisco Civic Auditorium, San Francisco, CA. CASExpo, 5203 Leesburg Pike, Ste. 1210, Falls Church, VA 22041; (703) 284-7330.

International Society for Hybrid Microelectronics (ISHM '89), October 24-26. Baltimore Convention Center, Baltimore, MD. ISHM, P.O. Box 2698, Reston, VA 22090; (703) 471-0066 or (800) 232-4746.

Simulation Based Tools for the Design and Analysis of Communication and Signal Processing Systems, October 25-27. Techmart, Santa Clara, CA. Anne Purvis, Comdisco Systems Inc., 919 E. Hillsdale Blvd., Foster City, CA 94404; (415) 574-5800.

IEEE 32nd Videoconference: RISC, Recent Developments in Processor Design, October 26. 12:00 – 3:00 PM, USA Eastern Time. The Learning Channel, 1525 Wilson Blvd., Ste. 550, Rosslyn, VA 22209; (703) 276-0881 or (800) 346-0032.

NOVEMBER

UNIX EXPO, November 1-3. Jacob Javits Convention Center, New York, NY. National Exposition Company Inc., 15 W. 39th St., New York, NY 10018; (212) 391-9111.

International Conference on Computer-Aided Design (ICCAD-89), November 6-9. Convention Center, Santa Clara, CA. MP Associates Inc., 7490 Clubhouse Rd., Ste. 102, Boulder, CO 80301; (303) 530-4562.

DEXPO West '89, November 7-9. Disneyland Hotel, Anaheim, CA. Expoconsul International Inc., 3 Independence Way, Prineton, NJ 08540; (609) 987-9400.

16th Annual Computer Security Conference, November 13-15. Atlanta Hilton and Towers, Atlanta, GA. Computer Security Institute, 360 Church St., Northborough, MA 01532; (508) 393-2600.

1989 International Test Conference, November 13-16. Sheraton Washington, Washington, DC. Doris Thomas, ITC, P.O. Box 264, Mt. Freedom, NJ 07970; (201) 895-5260.

Supercomputing '89, November 13-17. Reno/Sparks Convention Center, Reno, NV. Beverly Clayton, Pittsburgh Supercomputing Center, 4400 Fifth Ave., Pittsburgh, PA 15213; (412) 268-4960.

Wescon '89, November 14-16. Moscone Convention Center, San Francisco, CA. Alexes Razevich, IEEE, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

Electronic Services Expo (ESE), November 28-29. Santa Clara Convention Center, Santa Clara, CA. SHO Inc., 167 S. San Antonio Rd., Ste. 4, Los Altos, CA 94022; (415) 949-2050.

Lasers in Electronics Manufacturing, November 29-30. Hyatt Palo Alto, Palo Alto, CA. Diane Korona, Society of Manufacturing Engineers, One SME Dr., P.O. Box 930, Dearborn, MI 48121; (313) 271-1500.

DECEMBER

1989 Winter Simulation Conference (WSC '89), December 4-6. The Capital Hilton Hotel, Washington, DC. Barry Nelson, Ohio State University, Dept. of ISYEE, 1971 Neil Ave., Columbus, OH 43210; (614) 292-0610.

UNICOM '89, December 5-7. Infomart, Dallas, TX. Jozy Schlosser, North American Telecommunications Association, 2000 M St., N.W., Washington, DC 20036; (202) 296-9800, ext. 229.

American Society of Mechnical Engineers' (ASME) Winter Annual Meeting, December 10-15. San Francisco Hilton, San Fransisco, CA. Jeff Lenard, ASME, 345 E. 47th St., New York, NY 10017; (212) 705-7740.

1989 AEC Expo, December 12-14. Javits Convention Center, New York, NY. Expoconsul International Inc., 3 Independence Way, Princeton, NJ 08540; (201) 987-9400.

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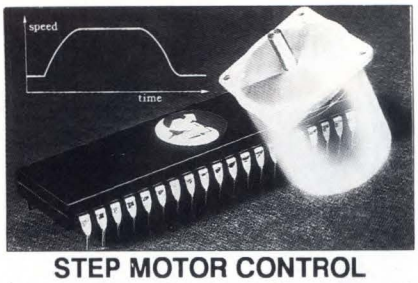

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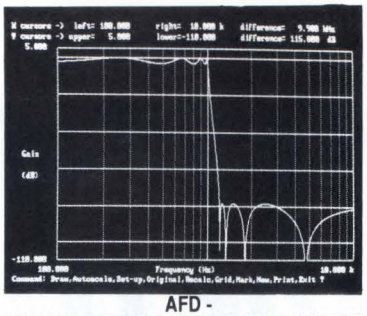

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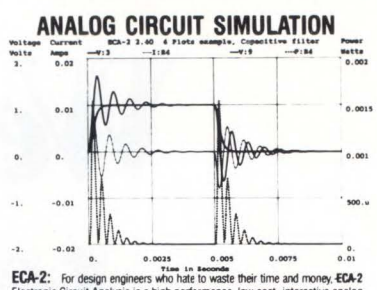

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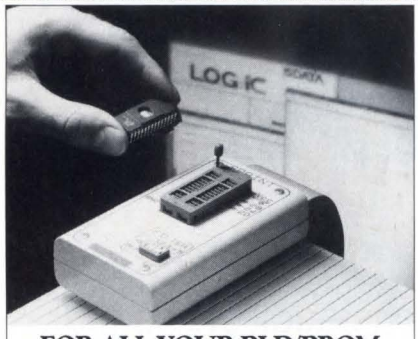

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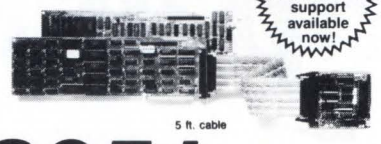

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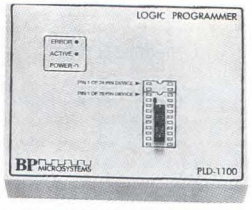

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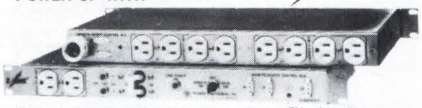

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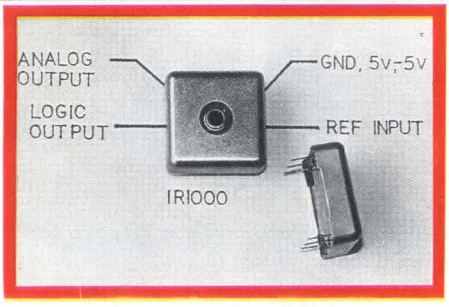

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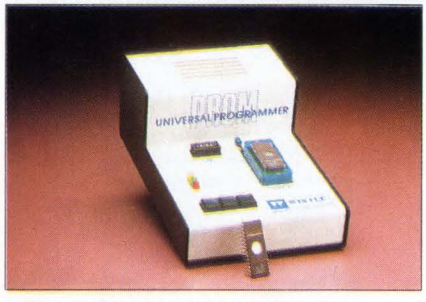

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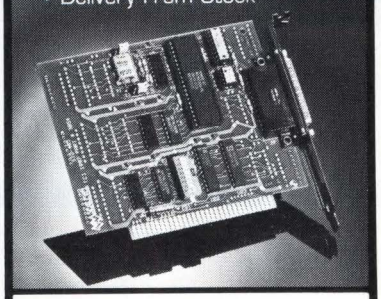

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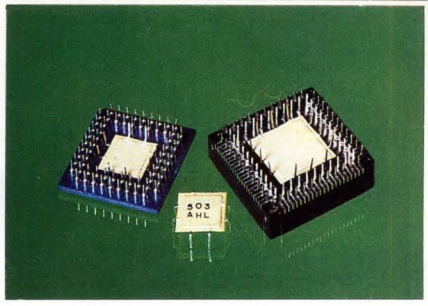

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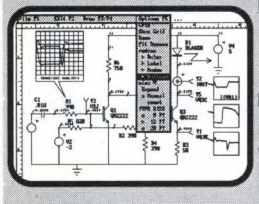

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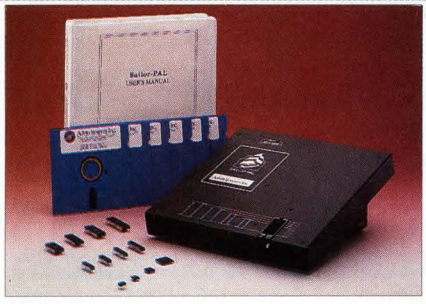

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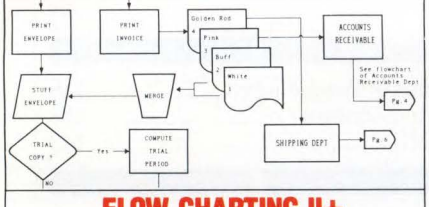

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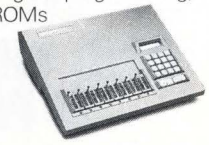

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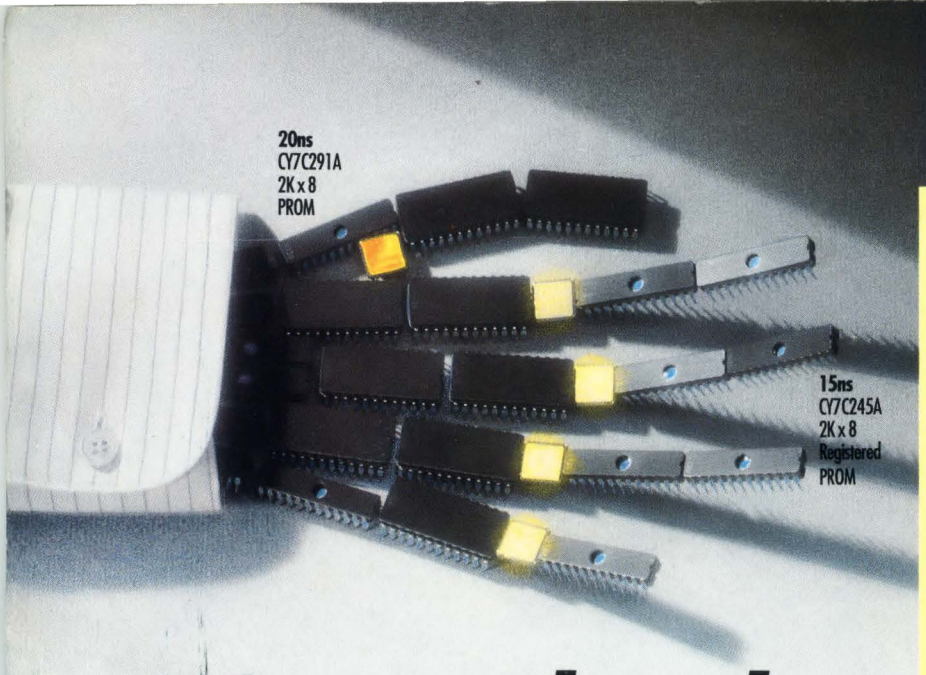

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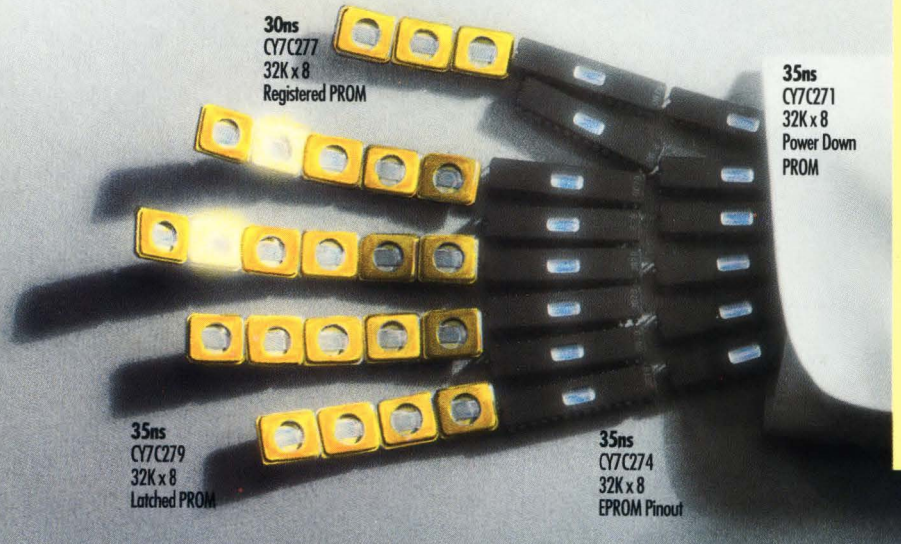

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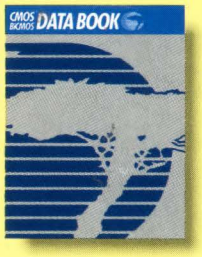

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