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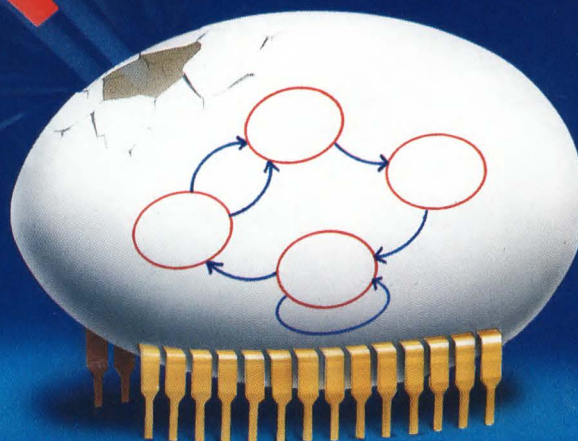
ELECTRONIC DESIGN

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SEPTEMBER 28, 1989

"SPLIT-PLANE" PLD HATCHES HIGH-SPEED STATE MACHINES

DESIGN



SPECIAL REPORT: DSP LURES AWAY ANALOG JOBS

MODEL	DESCRIPTION	RESOLUTION			Outputs	MEMORY		MEMORY		PROCESSING				
		Spatial	Gray Levels	Number		Number of	Buffer	Total	LUTs	Onboard Processor	Zoom, Pan, & Scroll	NxM Conv., Histogram	Real-Time Frame Aver. Math & Logic	Hardw Window
DT2862-60Hz ^a	Arithmetic Frame Grabber	512 x 512	256	8 ¹									8-bit or 16-bit ²	✓
DT2862-50Hz ^a	Frame Grabber & Frame Processor	512 x 512	256	8 ¹								✓	8-bit or 16-bit ²	✓
DT2862-60Hz ^a w/ DT2858 ^a	Frame Grabber & Frame Processor	512 x 512	256	8 ¹								—	8-bit	
DT2862-50Hz ^a w/ DT2858 ^a	Frame Grabber & Frame Processor	512 x 512	256	8 ¹								✓	8-bit or 16-bit ²	
DT2861-60Hz ^a	Arithmetic Frame Grabber	512x512	256	8 ¹								✓	8-bit or 16-bit ²	
DT2861-50Hz ^a	Frame Grabber & Frame Processor	512x512	256	8 ¹								✓	8-bit or 16-bit ²	
DT2861-60Hz ^a w/ DT2858 ^a	Frame Grabber & Frame Processor	512x512	256	8 ¹								—	4-bit	
DT2861-50Hz ^a w/ DT2858 ^a	Frame Grabber & Frame Processor	512x512	256	8 ¹								—	4-bit	
DT2851-60Hz ^a	High Resolution Frame Grabber	512 x 512	256									✓	4-bit or 16-bit ²	
DT2851-50Hz ^a	High Resolution Frame Grabber	512 x 512	256									✓	4-bit or 16-bit ²	
DT2871-60Hz	(HSI)Color TM Frame Grabber	512 x 512	16.8 million									—	4-bit	
DT2871-50Hz	Color Frame Grabber and Frame Processor	512 x 512	16.8 million									—	4-bit	
DT2871-60Hz w/ DT2858	Color Frame Grabber and Frame Processor	512 x 512	16.8 million									—	4-bit	
DT2871-50Hz w/ DT2858	Color Frame Grabber and Frame Processor	512 x 512	16.8 million									—	4-bit	
DT2853-SQ-60Hz ^a	Low Cost, Square Pixel Frame Grabber	512 x 512	Square Pixel Option									—	—	—
DT2853-SQ-50Hz ^a	Low Cost, Square Pixel Frame Grabber	512 x 512	Square Pixel Option									—	—	—
DT2803-60Hz	Low Cost Frame Grabber	256 x 256	64	8 ¹								—	—	—
DT2803-50Hz	Low Cost Frame Grabber	256 x 256	64	8 ¹								—	—	—

—Fred Molinari, President

Pages 6-7, 1989 New Products Handbook

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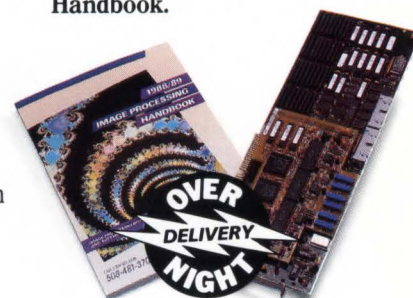
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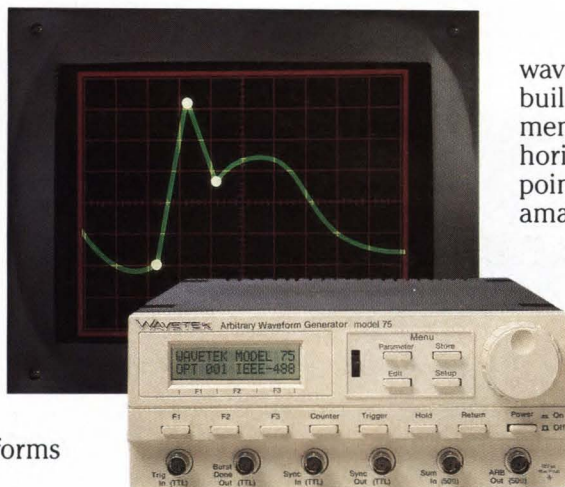


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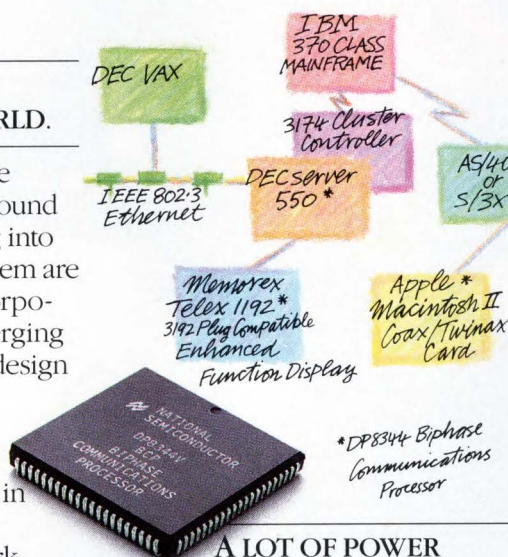
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The DP8344 Biphasic Communications Processor (BCP) is the key component in Apple's new adapter card for the Macintosh II—a landmark beginning in Apple's strategy of integration into the IBM mainframe environment.

The BCP is also a key component in Digital's new 3270 Terminal Option Card for the DECserver 550, which gives IBM 3270 displays full-screen VT220 access to VAX applications. Users can simply "hot-key" from their IBM system to Digital's program development environment, industry-leading ALL-IN-1, and world-class UNIX.

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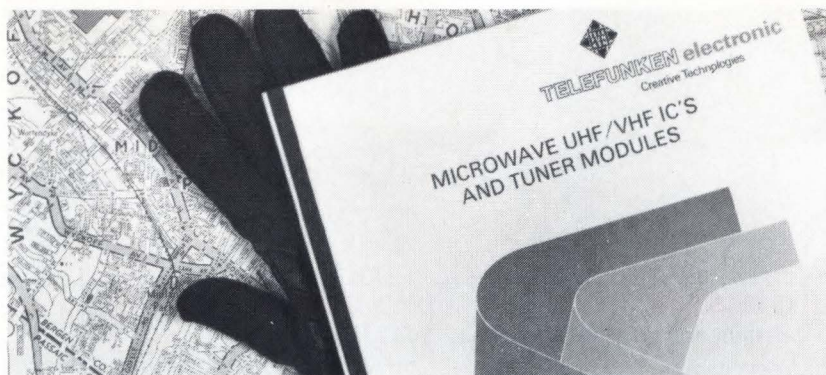
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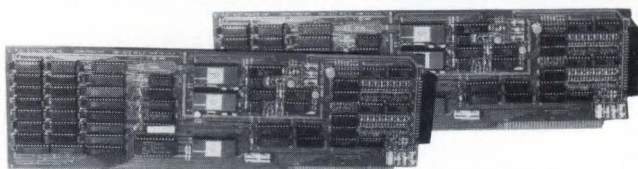


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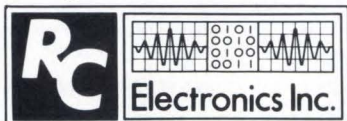
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Advertising Production:

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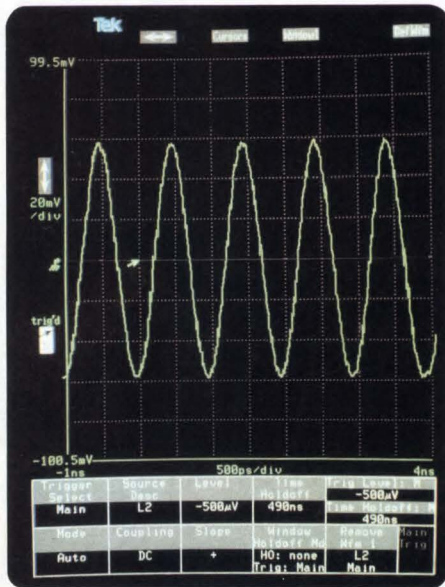
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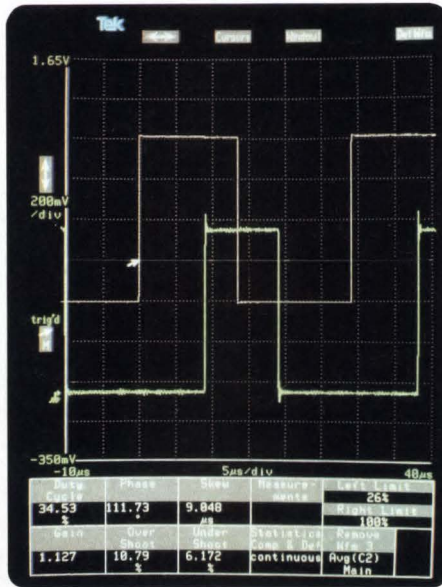
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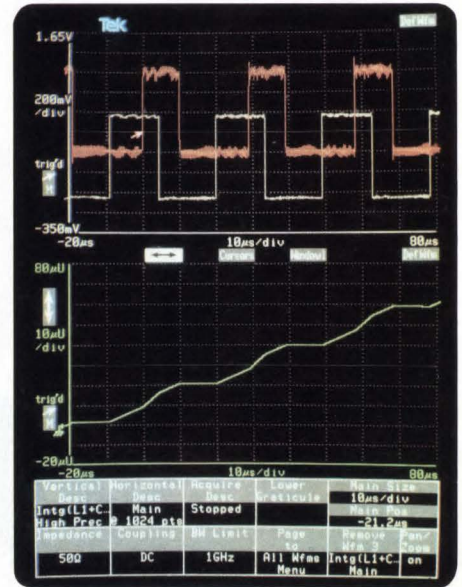
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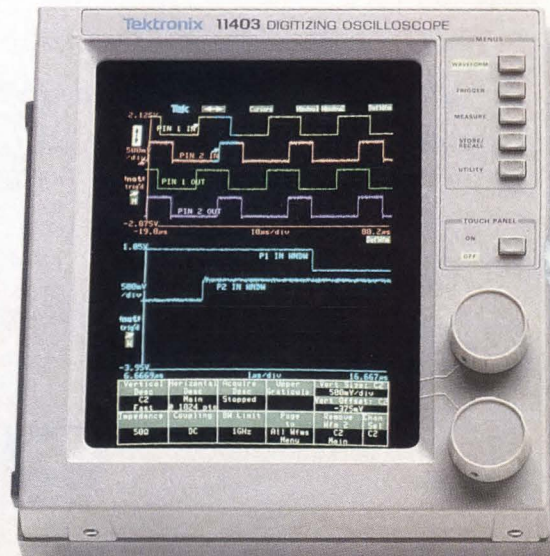
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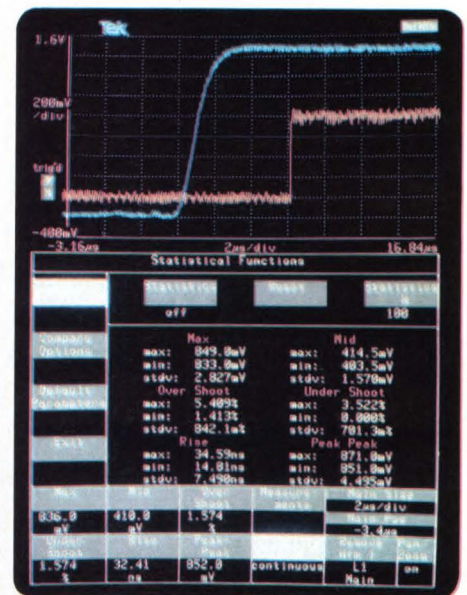
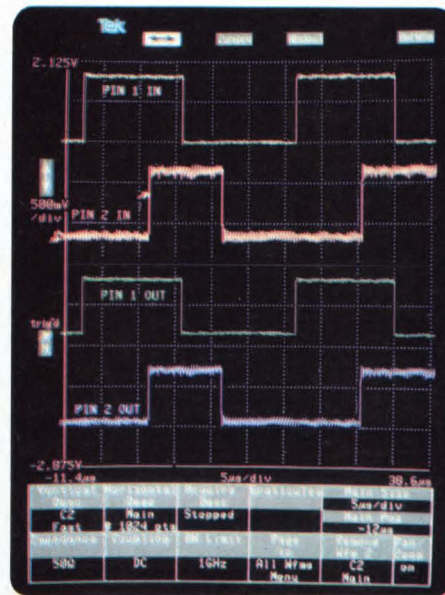
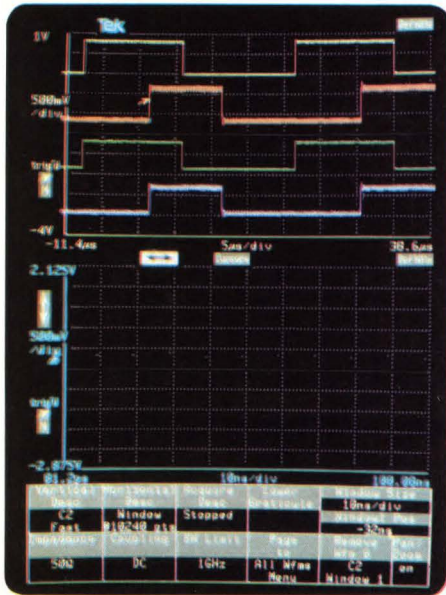
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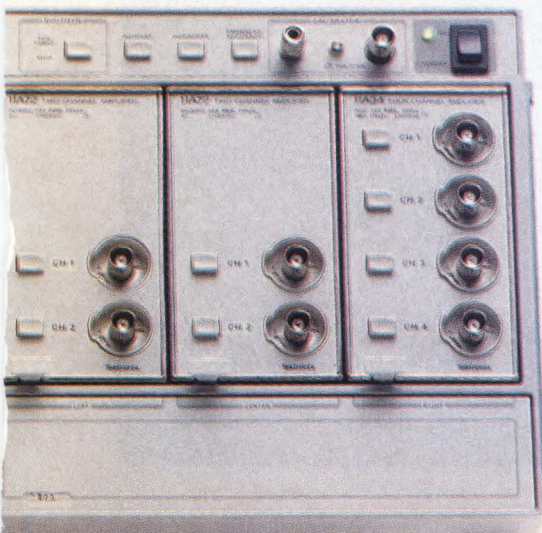
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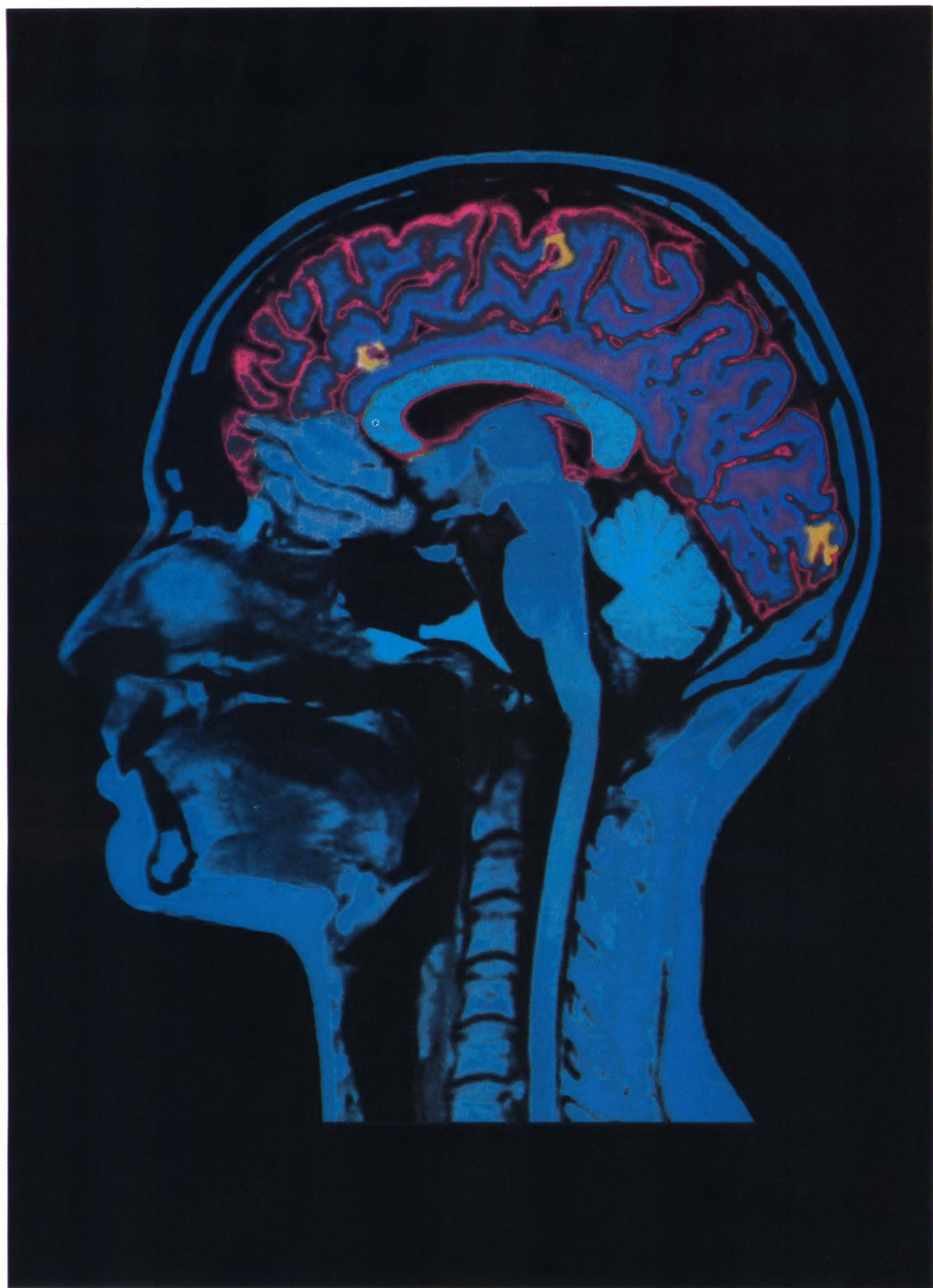
Make the measurements you need on the waveforms you want—power or energy, for example—with no outside controller required to manipulate data.

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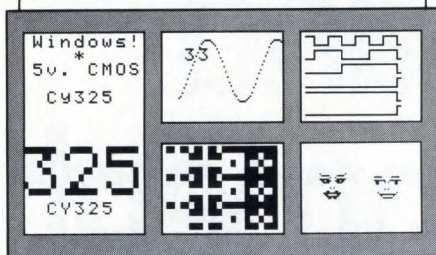
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What's Missing on this LCD?

(answers below)



If you peeked at the answers, then you know it's Motion. In the actual LCD every one of the windows is in motion. Think for a minute how you would make six or seven unique motions simultaneously with the low level LCD controllers that you have seen. No way! Now think what your instrument or new systems could do with dynamic text and graphics. Tests show that programmers can achieve animated presentations in only hours using the CY325.

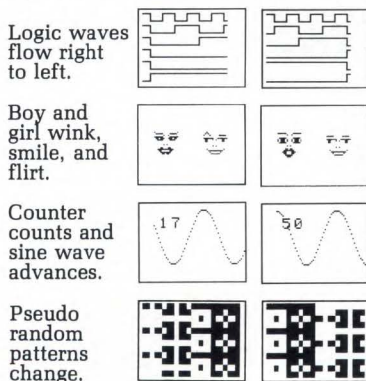
The CY325 LCD Windows Controller Chip



lets you: specify any of 250 built-in windows, or create your own with a single command; manage text and graphics with automatic cursor control; wrap or scroll text with window relative pixel plotting and clipping; read an A/D and write the waveform into the window; drive up to 6 I/O pins with logic waves, or use the 'soft-key' feature of the CY325 for menu management. Only \$75 each (\$20/1000)

Answer:

Motion is missing in each of the windows. Text actually scrolls up in the top left window above, and . . .



The next move is yours . . .

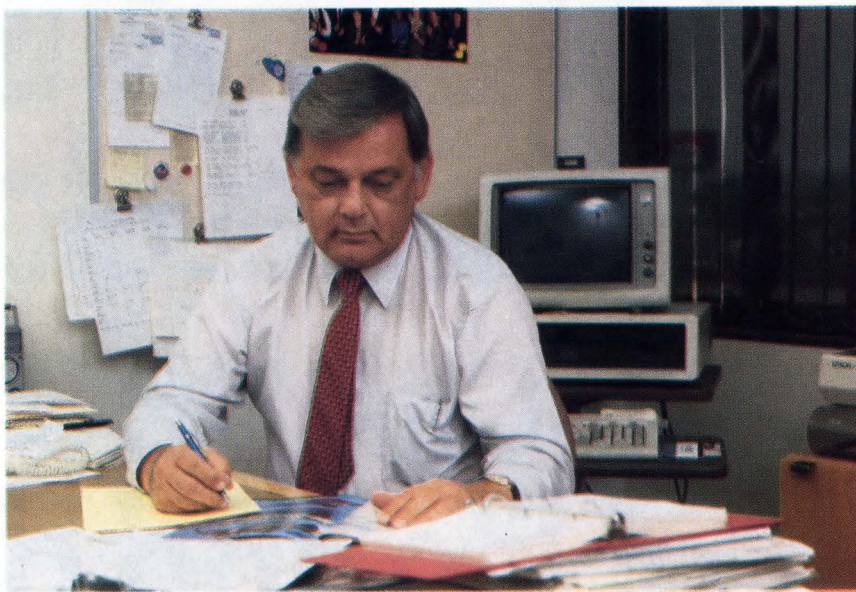
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CIRCLE 40

EDITORIAL



THE REAL WORLD

Yes, the real world is analog. Analog technology is alive and well, and specialists in linear circuits will always be needed. Indeed, this need grows critical as our industry's cadre of experienced analog designers move into management or approach retirement—and as more graduates choose the well-ordered world of ones and zeros rather than deal with the often arcane, intimidating complexities of analog circuitry.

However, digital technology is continuing its incursions into most systems' processing sections, as our report on DSP explains ("DSP Uproots Traditional Analog Jobs," p. 49). In systems with analog inputs, there's a lot to be gained in precision and flexibility by converting analog signals into digital form—as soon as these signals can be safely converted—and analyzing the signal for its information content while it's in a digital format.

The move to digitization is all around us and it's been growing for years. There are digital watches, digital scales, digital telephony, digital audio—the list is more than you can count on both hands and feet (and you can't get more digital than that). For instance, in the last issue of *ELECTRONIC DESIGN*, our cover featured a dual 18-bit analog-to-digital converter aimed at digital-audio-tape applications, as well as a host of other uses that involve signals in the audio-frequency range. And it still hasn't been settled whether high-definition television will evolve in the U.S. as primarily a conventional TV technology (with significant analog content) or as an extension of computer technology because of the functionality offered by digital circuitry.

We also are seeing more systems that combine analog and digital functions. In fact, as VLSI and CAE technologies advance, the major force driving many applications is the world of mixed analog-digital ASICs and its associated mixed-mode CAE simulators. This will be the cutting edge of many of tomorrow's systems; the area where the most critical design decisions will have to be made. And that's why digital technology won't offer a safe haven, far away from those arcane complexities of analog. There's no escape from the real world.

Stephen E. Scrupski

Stephen E. Scrupski
Editor-in-Chief



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	end, min.		200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
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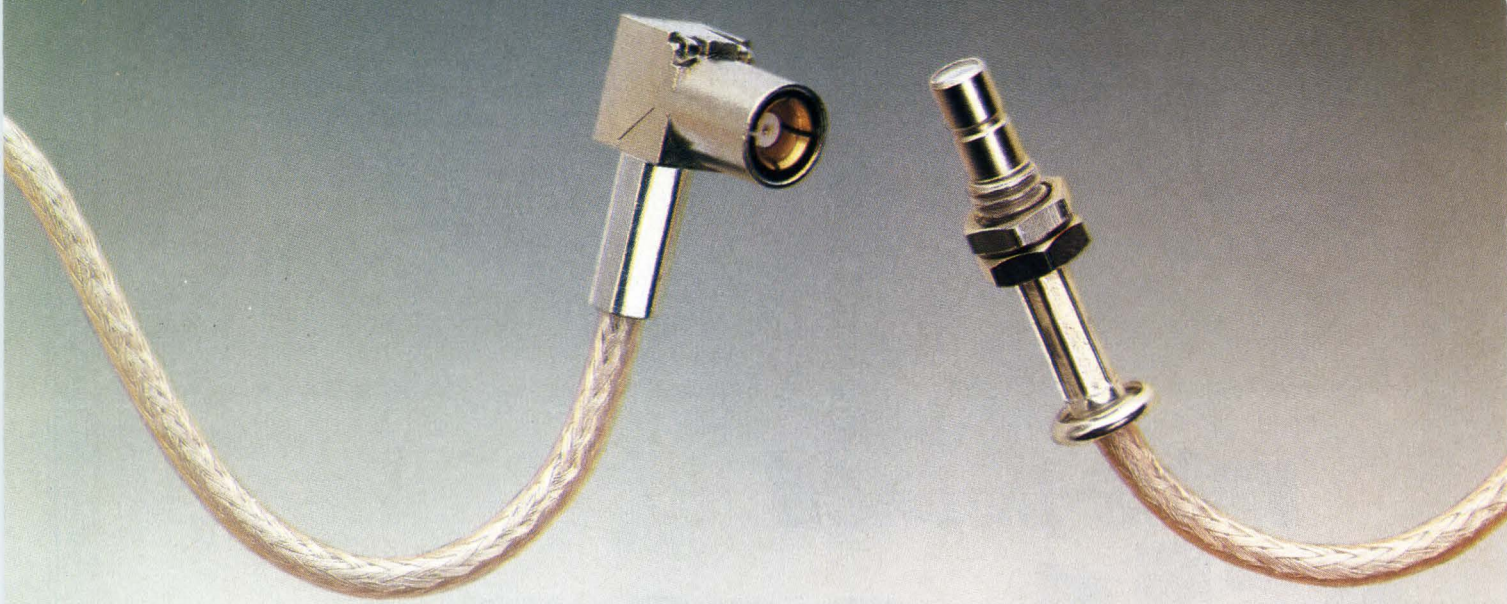
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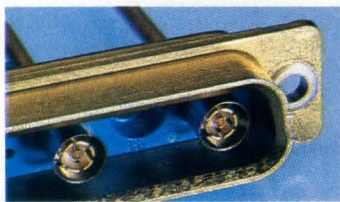
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CIRCLE 41



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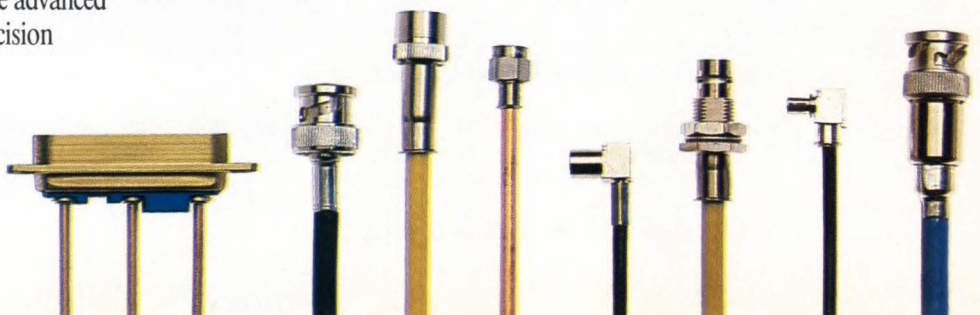
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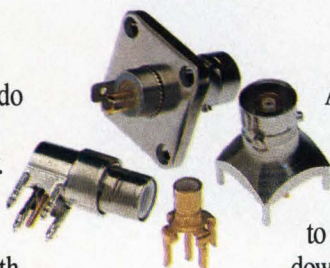
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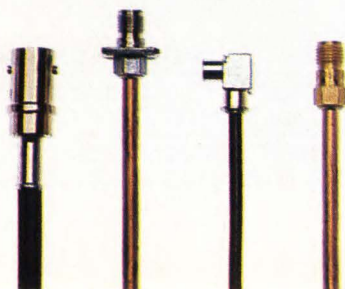
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CIRCLE 55

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NON-VOLATILE PRODUCT OFFERING												
Density	Organization	Type	Process	Access Times (ns)				Package				
								C-DIP	P-DIP	SOJ	SOJ	
256K	32 x 8	EPROM	NMOS	150	200			X				
		OTP	NMOS	170	200				X			
	32K x 8	EPROM	CMOS	70	85	120	150	200	X	X	X	
		OTP	CMOS	100	150	200			X	X		
		MROM	CMOS	200					X	X		
512K	64K x 8	FEEPROM	CMOS	170	200	250			X	X	*	
		EPROM	NMOS	170	200	250		X				
	64K x 8	OTP	NMOS	200	250				X	X		
		EPROM	CMOS	150	200			X				
		OTP	CMOS	170	200				X	X		
1 MEG	132K x 8	MROM	CMOS	150	200				X	X		
		EPROM	CMOS	150	200			X				
		OTP	CMOS	200	250				X	X		
	1 MEG	64K x 16	MROM	CMOS	120	150	200			X	X	*
			EPROM	CMOS	85	100	150	200	X			*
OTP	CMOS		200	250				X	X	*		
4 MEG	512K x 8	MROM	CMOS	120	150				X	X	*	
		EPROM	CMOS	150	200			X			*	
		MROM	CMOS	250					X	X	*	
*Indicates this package is under development.												

*Indicates this package is under development.

It's available in a 28-pin plastic DIP and a plastic flat pack; both are pin-for-pin compatible with standard 256Kb EPROMs, OTPs and ROMs. Which means it can be placed in existing sockets with no design changes required. By eliminating the separate programming step, the coplanarity of the surface-mount Flash EEPROM is preserved.

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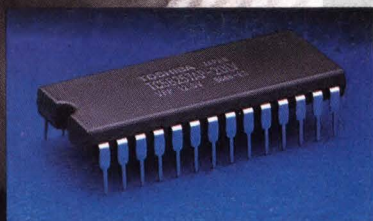
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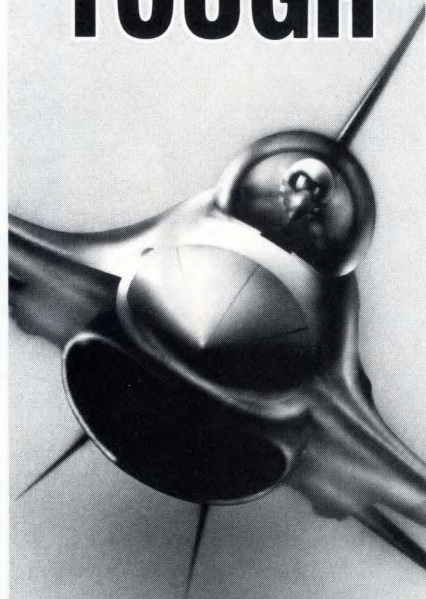


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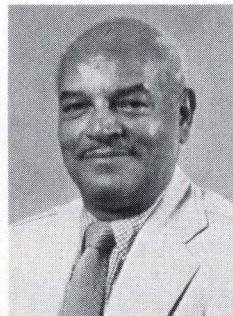
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CIRCLE 42

TECHNOLOGY BRIEFING

IC PACKAGING: THE NEXT CHALLENGE

Once relegated to second- or even third-class status, behind more glamorous aspects of electronic system design, semiconductor packaging technology is finally on a par with processing technology and circuit and system design. It's now a critical issue that should be addressed early in the design cycle. Each new generation of products is driven by five recurring design objectives that have direct bearing on packaging design: lower component and system costs, increased performance, increased interconnect density, design flexibility for custom requirements, and the use of custom multifunctional modules and single-function chips.



MILT LEONARD, EDITOR
COMMUNICATIONS AND
INDUSTRIAL

According to spokesmen at Texas Instruments, Dallas, new-generation system designs generally require a performance increase of at least two times to be competitive, which roughly translates to a four-times improvement in circuit density. The most advanced semiconductor technologies are already producing chips with logic-gate counts that exceed 100,000, requiring 500 to 600 interconnections to a board or package. The interconnection pitch for these leads are approaching limits. The constraints are imposed by practical chip size, and by the state-of-the-art in steppers that dictate the bond-pad pitch dimensions. Moreover, there still remains the challenge of board attachment.

To overcome the routing and manufacturing limitations in conventional circuit-board technology, the industry is pursuing two alternatives. One concept is to increase board-line density without significantly increasing board cost, which may call for new materials and improved board technology.

The other option is to combine existing board technology with multichip modules. This approach applies the fine-line techniques of conventional semiconductor fabrication equipment to make silicon substrates for multichip modules. The solution not only opens the way to more complex system integration, but also extends capital resources for improved return on investment.

Mounting multichip modules on a silicon substrate also reduces cooling requirements by minimizing the length of signal lines. Mosaic Systems Inc., Fremont, Calif., an early developer of this technology, already offers a silicon daughter board with a programmable interconnect for tying together eutectically bonded chips. TI also demonstrated a memory module bonded to a silicon daughter board. This technique has a density improvement of 1.28 Mbits/in.³ for a conventional DIP package, to 364.0 Mbits/in.³ for the new module, which uses 1-Mbit dynamic RAM chips.

TI has extended this packaging technique to a system-level module to reduce the number of bonding operations from 500 required for the individual chips to just 45. The 45-chip module contains three TMS320C30 signal processors, two ASICs, 32 4-Mbit static RAM chips, and eight 2-kbit EEPROMs. The module is housed in a 308-lead quad flatpack with a standard lead form factor. Taking this concept even further, silicon chips mounted to silicon substrates or daughter boards could eventually lead to silicon motherboards.

The use of silicon-based substrates for system-level modules is an elegant packaging solution for reaching the objectives of next-generation system designs. Further development may make it possible for chips with interconnects on their sides to be stacked and mounted orthogonally with respect to the substrate. This configuration results in a 300:1 improvement in memory density over DIP assemblies. The directions being taken by ongoing development of 3D packaging technology suggest a possibility for the ultimate solution. Can truly 3D, monolithic circuits implemented in blocks of silicon be far behind?

DAS 9200 Version 2

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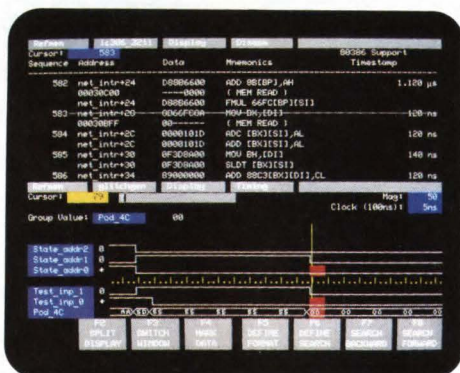
The most impressive number to come out of the Tek DAS 9200 may be its price: now you can leverage the power of the DAS for little more than the cost of systems that aren't even in the same league. Consider:

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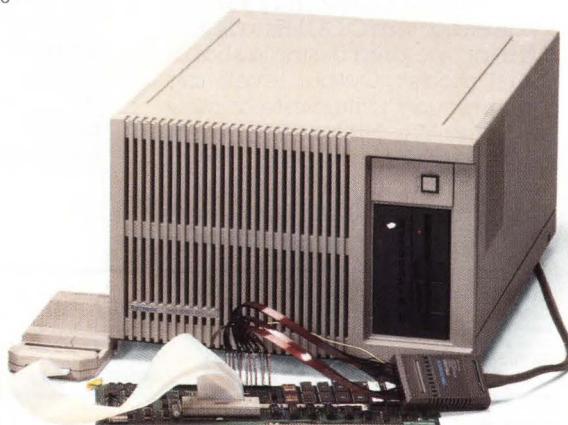
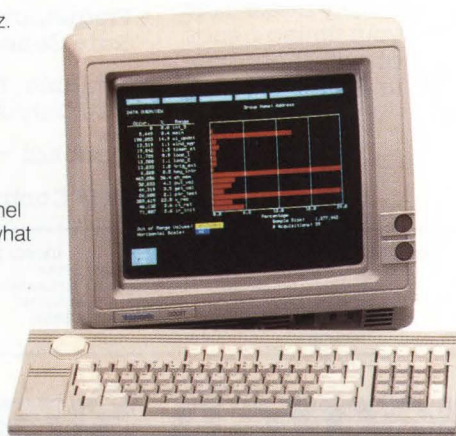
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TAPE AUTOMATED BONDING ADDS PACKAGE PROWESS

After joint research on tape automated bonding (TAB) by Digital Equipment Corp., Maynard, Mass., and the Microelectronics and Computer Technology Corporation (MCC), Austin, Texas, the technique is now being used by DEC to link the VLSI processor chips within 224-pin multilayer ceramic packages. Developed in concert with MCC's Packaging/Interconnect Program, TAB helps electronic packaging keep pace with chip integration and speed. It replaces wire bonding of chips in packages and allows for direct connection to substrates. Furthermore, it eliminates several steps in the manufacturing process. The 224-pin packages are being used by DEC in its VAX 6000 Model 400 systems. DM

SUN'S SBUS OPENS UP WITH SPEC'S RELEASE

For some time, Sun Microsystems Inc., Mountain View, Calif., was relatively mum about its SparcStation SBus, despite a promise to make the bus an open standard so third-party developers could build add-in cards (ELECTRONIC DESIGN, June 8, p. 27). Earlier this month at the Boston Buscon Exhibition, however, the company released the full SBus specification, free of any licensing restrictions. The company also plans to create an SBus developer's kit that will cut the time it takes a company to develop the postcard-sized SBus add-ins. And, in conjunction with LSI Logic Corp., Milpitas, Calif., Sun will make available the SBus direct-memory-access controller, which can run at 100 Mbytes/s on each of its two 32-bit channels. LSI Logic will sell the 120-lead chip (the L64853) on the open market for \$76 in quantities of 100 units. The system interface side of the chip includes a byte-packing feature to allow the 32-bit host bus to tie into a 16-bit Ethernet controller and an 8-bit SCSI adapter. DB

CHIPS ARE COMING FOR FASTER ARCNET LAN

Until now, Arcnet's developers, Datapoint Corp., Dallas, had no commercial suppliers for LAN chips and boards to support Arcnetplus, a 20-Mbit/s version of its network protocol. Now, the two companies that built the first generation LAN chips, Standard Microsystems Corp., Hauppauge, N.Y., and NCR Corp., Colorado Springs, Col., have joined with Datapoint to develop and sell chips, add-in cards, and end-user systems for the 20-Mbit/s Arcnetplus. Those products will also work with the more than two million existing nodes for the lower-speed Arcnet. NCR will employ its circuit design tools and libraries for developing the chips, and Standard Microsystems will serve as an alternate source for the design. Prototyping kits from Datapoint, consisting of two full-size PC/AT Arcnetplus add-in cards with documentation, will be ready in the fourth quarter. With the kits, developers can get started creating the software drivers needed to use the LAN, even before the chips are available. DB

POCKET-SIZED PC PROVES ITSELF A POWER MISER

A portable personal computer, the Poqet PC, from Poqet Computer Corp., Sunnyvale, Calif., squeezes 100 hours from a pair of AA-size alkaline batteries (see p.27 for related stories). To achieve this, just about everything in the computer was custom designed to cut the system's active power consumption to just 50 mW. System software even checks the CPU and, during inactive periods, stops the clock to the rest of the system logic to save power—even between keystrokes. What's more, to keep the PC's dimensions to 8.75 by 4.3 by 0.925 in., component count was slashed by using a pair of VLSI custom chips to hold most of the system's logic. Additionally, a custom-developed double supertwist liquid-crystal display gives a high-contrast image of 80 characters by 25 lines. To avoid all electromechanical and moving parts (except keys) and thus reduce the system's weight, designers substituted low-power static RAM or ROM cards for an internal floppy-disk drive. The unit comes with 512 kbytes of low-power static RAM. A low-voltage, high-value capacitor keeps the RAM data alive long enough to change batteries. To achieve IBM PC compatibility, the pocket-sized computer employs an 80C88 CPU and DOS 3.3. Communication with the outside world goes over two serial ports, a parallel port, and an expansion slot for an XT-compatible card, such as a disk controller. DB

INTELLIGENCE IMPROVES DRIVES' RELIABILITY

Embedded, intelligent SCSI controllers impart top performance and reliability to the ProDrive family of 120-, 170-, and 210-Mbyte (formatted) 3.5-in. disk drives. Custom circuits and firmware in the drives from Quantum Corp., San Jose, Calif., exercise precise control and include a fail-safe scheme to manage defects, and detect and correct errors. To achieve an average seek time of less than 15 ms, SCSI control circuits produce read or write operations with zero rotational latency, command queuing, and

other SCSI-2 features. In addition, up to 64 kbytes of internal cache RAM can be added to the drives to improve the burst data rate between the drive and the host system. Synchronous burst transfers of up to 4 Mbytes/s are possible. To ensure reliability, each drive can report on errors related to media, as well as to servo and motor controls. A cumulative error count for each error type is then stored in the drive for analysis by the maker if the drive should be returned. Two levels of diagnostic self-testing are also included in the drive: One tests the digital circuitry and can be used for system power-up testing; the other is more exhaustive and checks the servo and read/write circuits for, say, incoming inspection. DB

OPTICAL GAAS CHIPS BREAK DENSITY BARRIERS

Scientists at IBM's Research Div., Yorktown Heights, N.Y., believe that they have constructed the densest optoelectronic chips yet, which transmit and receive data over fiber-optic lines at 1 billion bits/s. The low-power chips combine digital, analog, and optoelectrical functions. The chips were built from a gallium arsenide MESFET (metal semiconductor FET) process that is suitable for optoelectronic parts because it can put large numbers of transistors and light-emitting and detecting devices on one substrate. One chip, a 1/4-in. detecting device, contains 8000 transistors, 50 times more than were ever assembled on a die that size. IBM believes that this chip set will open doors to fast, reliable, and inexpensive data-communication devices. RN

WORKSTATION CARRIES LOWEST PRICE TO DATE

A workstation from Hewlett-Packard's Apollo Division, Chelmsford, Mass., combines a 20-MHz Motorola 68030 microprocessor with proprietary ASICs to deliver 4 MIPS for integers, and 0.203 MFLOPS when executing a double-precision Linpack floating-point benchmark. With a 15-in. monochrome screen and 4 Mbytes of memory—but no disk storage—the \$3,990 Apollo Series 2500 is said to be the first workstation priced under \$4,000. The unit will replace the 68020-based 1.5-MIPS Apollo Series 3000. Its performance is better and its price lower than a similarly equipped Sun Microsystems 3/80, which runs 3 MIPS and costs \$5,995, though the Sun product has a 17-in. monochrome screen. A number of ASICs, including one that functions as the SCSI controller, keep down the cost and parts count, letting Apollo put all of the electronics on one motherboard. LC

WILL MICRO CHANNEL POWER IBM MAINFRAMES?

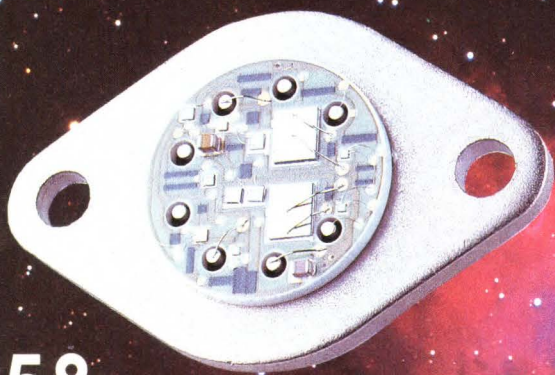
IBM Corp. plans to employ a multimicroprocessor architecture in its mainframe and midrange systems for the 1990s, according to an analysis done by the International Technology Group, Los Altos, Calif., (see ELECTRONIC DESIGN, May 11, p.23). The IBM architecture rests on proprietary RISC and CISC processors, as well as versions of Intel Corp.'s 80X86 and i860 devices. In addition, an enhanced version of the Micro Channel bus operating in a cooperative processing mode will tie the system together. Though first implemented in the PS/2 machine, the Micro Channel architecture was designed for use across IBM's entire computer line. By 1996, the complete IBM product line will move over to a common, modular microprocessor-based architecture. Consequently, mainframes, midrange systems, and workstations will easily operate together. Part of IBM's strategy is to head off the threat posed to its mainframe business by microprocessor-based systems. The analysis, "IBM Strategies for the 1990s," covers IBM's system architectures and product plans, and is available for \$1500. Call (415) 964-2565. LG

ANALOG COMPILERS BUILD FILTER, LINEAR ICS

A pair of mixed-signal compilers in development by Silicon Compiler Systems Inc., San Jose, Calif., promise to aid designers who create analog chips, especially ones with switched-capacitor filters (SCFs) and general-purpose linear functions. The company claims that these tools—Explorer Autofilter and Autolinear—are the first mixed-signal compilers to deliver optimized circuit designs down to the physical layout. Both tools are the result of partnerships that the company formed with other organizations: CSEM in Switzerland, the developers of the compilation program at the core of Autolinear, and International Microelectronic Products Inc., San Jose, Calif., which worked on the automatic generation of SCFs. Autolinear encapsulates the CSEM tools and places them in a mixed-signal environment. Users can synthesize basic linear circuits and optimize them for drive, gain, phase, noise, and so forth. Autofilter combines Autolinear with specialized algorithms that custom-size the capacitors and adjust the linear circuit parameters. A slightly simplified and lower-cost version of Autofilter uses a preset library of amplifiers and other elements. This saves on system resources and shortens the design time: Just 30 minutes are needed to compile a filter after the input specification is loaded into the software. DB,RN

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Creating value

CAE Technology Report

Vol. 1, No. 6

September 1989

CAE Enhances Designer's Job Security

During good times, CAE tools allow manufacturers to get to market ahead of the competition. Plus, a product designed with CAE tools is more reliable and better documented than one done without it. Even in the worst times, CAE tools allow greater productivity with fewer people. Furthermore, once a company establishes an effective CAE staff, it is unlikely that the team will be broken up even in the worst of times. Unquestionably, CAE expertise enhances job security. **CIRCLE 104.**

New Generation Simulators Pace CAE Industry Growth

Improved simulators are a major factor in the robust growth of the CAE industry. Not so long ago, simulation meant an off-line final design check for timing violations, bus conflicts, etc. However, it is now clear that simulating complete designs off-line is inefficient, labor intensive and slow. Today, on-line simulators eliminate this tedious, time-consuming process. These real time simulators are free of compilations and allow on-the-fly design and test vector modifications. The user can now simulate and correct a design as it evolves, cutting design time to less than 20% of what it took with the older generation simulators. Among the vendors that offer these real time simulators are: P-CAD, Racal-Redac and Omaton. **CIRCLE 105.**

Omaton Adopts PC Simulation Standard

Omaton Corp. (Richardson, TX) is the latest CAE vendor to adopt the Standard Universal Simulator for Improved Engineering (*SUSIE™). Specializing in schematic capture (Schema II™) and p.c. board layout software, Omaton is one of the oldest PC-based CAE vendors with over 12,000 users. With the new simulator, Omaton will provide a total front-to-back solution and further reinforce its leading position in the PC-based CAE marketplace. Want more information? Call Omaton at (214)231-5167 or **CIRCLE 101.**

Standards Will Aid CAE Growth

With P-CAD, Omaton and other industry leaders supporting a logic simulation standard, PC-based CAE tools will have an advantage over the more expensive workstation-based simulators. What's more, the new PC simulation standard (SUSIE) is fast, has many IC libraries and operates in real time. SUSIE provides instantaneous design and test vector changes, so these PC CAE vendors offer a very friendly design environment. In contrast, workstations still require batch compilation for any design or test vector change. **CIRCLE 103.** ALDEC: (805) 499-6867.

Putting CAE Tools On Every Engineering Desk

"Quality libraries and a friendly user interface are critical issues for the CAE industry," notes Stanley Hyduke of the ALDEC company. He adds that quality is by far the most important issue and could hamper CAE industry growth. Hyduke points out that some companies have cut quality corners in the heat of competition. However as the industry matures, the most successful CAE companies have set product quality as their number one objective. For example, ALDEC is quadrupling its QA staff. In addition, ALDEC is establishing a new company dedicated to verifying the quality of user-supplied models. Thus, designers from all over the world can submit models that would be resold to other users after QA verification. All contributors of IC models would then receive royalties. **CIRCLE 102.**

New environmental EMC shielding gaskets*: low compression force, high attenuation, and flexibility of design.

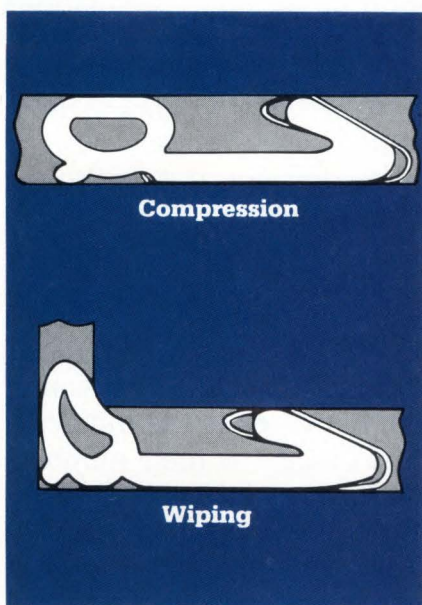
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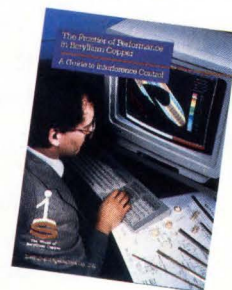
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SILICON PROCESS GIVES GAAS A RUN IN MICROWAVE SYSTEMS

An advanced silicon-based process suited for monolithic microwave ICs promises to yield microwave circuits that would otherwise be built with gallium arsenide (GaAs). The circuits include frequency dividers, broadband amplifiers, low-noise amplifiers, and gain blocks that operate at frequencies above 5 GHz. Developed by NEC Corp., Kawasaki, Japan, the DNP-III process is the company's third generation of a direct-nitride, passivated-base surface structure, which was originally unveiled several years ago.

With the process, npn transistors are created without complex self-aligned structures. Yet these transistors achieve unity-gain bandwidths (f_T) of 20 GHz, which is nearly double that of commercially available silicon transistors. Furthermore, small signal insertion gain—the squared absolute value of the S_{21} parameter—is 17.1 dB at a V_{CE} of 5 V and a frequency of 2 GHz.

The wide bandwidths translate into high operat-

ing frequencies for the circuits. For example, a simple divide-by-two prescaler circuit built with the process operates at 7.3 GHz. That's well into the frequency range currently dominated by GaAs circuits. Moreover, the circuit draws just 16.6 mA at 5 V. Products developed with this process will be marketed in the U.S. by California Eastern Laboratories Inc., Santa Clara, Calif.

To achieve high-frequency performance, the transistors have emitter stripes that are just 0.6 μm wide. Formed with high-resolution photolithography, the narrow stripes minimize transistor-base resistance and parasitic-base capacitance. An ion-implanted arsenic buried layer and a thin, low-resistance epitaxial silicon layer on the wafer also help minimize the collector resistance.

In addition, because a low-energy boron-ion implant serves as the base, the base junction depth is only 0.2 μm . At 0.1 μm , emitters are even shallower, formed by diffu-

sions from arsenic-doped polysilicon emitter contacts. The shallow junctions also trim the base transition-time delay to about half that of conventional processing.

By adding a selectively ion-implanted collector structure to the transistors, the f_T can increase by almost 50% to 30 GHz, but these implants complicate the process. The structures also lower the reverse voltage that the transistors can withstand across their collector-base and collector-emitter regions, dropping them to 7 V for BV_{CBO} and 3.3 V for

BV_{CEO} .

Consequently, circuits that are built with the collector implants must operate with power supply voltages of less than 3 V. Without the collector implants, the transistors have reverse-voltage ratings of 17 V and 6 V, respectively. These higher values enable the circuits to operate from 5-V supplies. The implanted structure's lower voltage values stem from a narrowing of the intrinsic base width and a thinning of the base-collector depletion region, which are a result of the implants.

DAVE BURSKEY

"PALMTOP" COMPUTER BLENDS MICROMINIATURE TECHNOLOGY

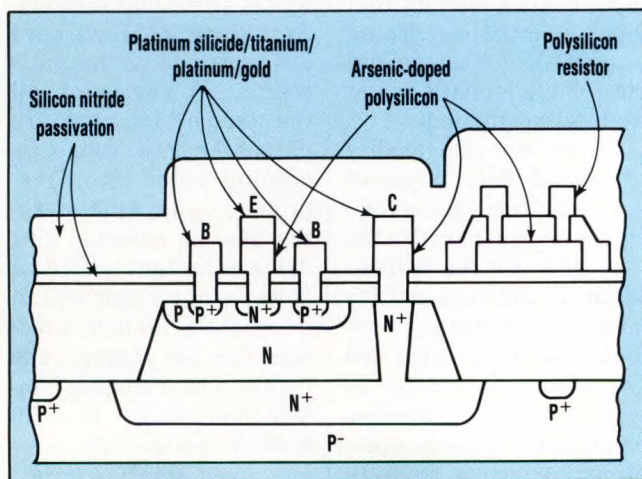
Occasionally a product design excels at blending the best of several advanced technologies to reach specific marketing objectives. Nowhere is this better demonstrated than in the industry's first MS-DOS-compatible palmtop personal computer. At just 7.8 \times 4.1 \times 1.2 in., the Portfolio from Atari Computer, Sunnyvale, Calif., is slightly smaller than a VCR tape. It comes with an operating system that's compatible with MS-DOS version 2.11, a spreadsheet program that accepts Lotus 1-2-3 files, word-processing software, a calculator, a diary, and a phone directory.

Atari designers exploited several advanced hardware and software techniques in their quest to build the smallest possible battery-powered, full-featured PC—and one that would sell for under \$400. First, the Portfolio's two-sided circuit board is popu-

lated with CMOS components in surface-mounted packages, including the Intel 80C88 microprocessor, RAM, and an ASIC chip that supplies system glue logic.

Another space-saving step replaces a floppy drive and disks with a memory-card drive and solid-state memory cards. Finally, a 40-column by 8-line LCD display helps minimize size and power consumption. The computer runs on three AA alkaline batteries or from an optional ac adapter.

System software conserves power by switching the unit into a standby mode between keystrokes. In this mode the display remains visible for 2 to 4 minutes—after that it's automatically turned off. However, data is retained and a keystroke turns the unit on again to resume work in progress. A built-in circuit senses low-battery conditions and alerts the user



with a screen message before shutting the system off. These features combine for six to eight weeks of operation under normal battery usage.

The Portfolio has a hinged clam-shell construction with the 7.8-by-4.1-in. keyboard on the bottom half and the display on the top half. The keyboard is a 63-key IBM PC-software-compatible design with full travel and an audible key-click feature that can be disabled. A special key combination activates a numeric keypad. For storing data files or application programs, the unit



comes with plastic-encased memory cards, each about the size of a credit card. Memory card options are 32 kbytes, 64 kbytes, and 128 kbytes RAM; 64 kbytes and 128 kbytes PROM; and 128 kbytes masked ROM. RAM capacity can be stretched with optional memory-expander attach-

ments. For frequent file transfers, an external memory-card drive speeds downloading and read-write operations.

A 60-pin bus connector can be used with Atari's optional serial or parallel interfaces for connecting the Portfolio to any peripheral that uses the standard Centronics parallel or RS-232-C serial interfaces. For example, the parallel interface can connect the system to a parallel printer, or it can be used to transfer files between the Portfolio and an IBM PC or compatible desktop computer.

MILT LEONARD

MHz down to 1 MHz, or turn the system off entirely. Any keystroke reactivates the system to full speed.

Additional power-saving considerations went into the main memory design. Rather than use high-density dynamic RAMs (DRAMs) that require periodic refreshing, and thus continually draw current to maintain data, designers chose 32k-by-8-bit static RAMs (SRAMs). Because only two SRAMs are needed to form a 16-bit word, only two of the memory chips in the entire 1-Mbyte bank are active at any point in time.

The system will initially come with 1 Mbyte of SRAM. An optional 1-Mbyte bank can be added. As memory chips get denser, the system can pack as much as 9 Mbytes. Although 1 Mbyte of SRAM costs more than 1 Mbyte of DRAM, data can be indefinitely retained in the SRAM with nearly unnoticeable power drain from the main battery when the system isn't in use.

As with all other new Macintosh systems, the portable Mac will include one 3.5-in. floppy "superdrive" that reads and writes all popular formats. An optional 40-Mbyte hard disk adds 2 lbs. to the unit's weight. Furthermore, all the standard I/O ports are part of the base system, including video interface, printer, audio, Apple desktop bus, an external disk drive interface, SCSI, a power adapter jack, and an internal slot to hold a modem (*see the figure*). The built-in power adapter handles line voltages from 70 to 270 V at 40 to 70 Hz.

DAVE BURSKEY

MACINTOSH GOES PORTABLE, DELIVERS DESKTOP-DISPLAY QUALITY

Blending a highly readable display and long battery life in a portable computer presents trade-offs and challenges that will test any engineer's skill. For engineers at Apple Computer Inc., Cupertino, Calif., the newly released portable Macintosh was no exception. It took an active-matrix liquid-crystal display (LCD), intelligent power management, and custom-designed chips to meet the challenge.

The 13.75-lb. battery-powered system is the first portable computer to pack an active-matrix LCD, which combines a wide viewing angle with a crispness and response time that other portable systems lack. The monochrome 640-by-400-pixel display doesn't have a backlight, but in most situations it won't need one thanks to the active matrix technology. Furthermore, having a transistor drive

each pixel—the essence of an active matrix LCD—makes the display's response time short enough to show real-time animation.

In addition, the responsive display makes it possible for Apple to embed an optical trackball mouse in the keyboard to move the cursor quickly. As an option, the trackball can be set on the left- or right-hand side of the 63-key keyboard, or it can be replaced altogether with an 18-key numeric keypad for serious spreadsheet users.

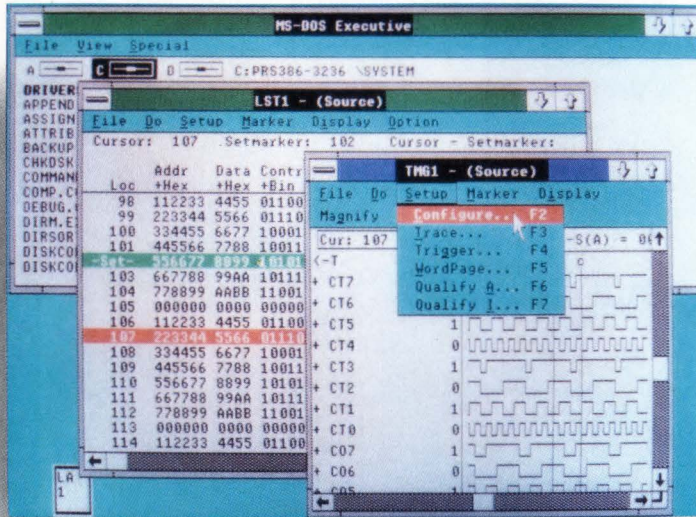
Beyond the display, Apple designers went with an all-CMOS system design, intelligent and programmable power management, low-power static RAM for main memory, and a rugged lead-acid main power source. There's also a 9-V emergency back-up battery. The net result of this strategy: the machine will operate for about 10 hours (av-

erage) on the main battery before needing a recharge.

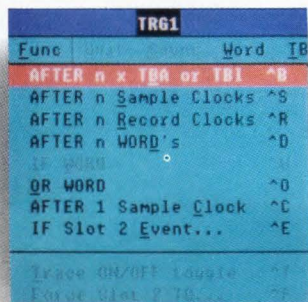
Apple designers approached the intelligent power management from two directions: First, a single-chip microcontroller was programmed to monitor all aspects of system operation and selectively turn off, or put into a sleep mode, all nonactive subsections of the system. Second, many custom chips developed by Apple include their own power management control circuits that monitor signal lines. Those internal power control circuits can trim back power drain within the chip.

Users can also modify the initial default power saving features to customize the power control to the way they use the system. With a software utility package, users can set various time delays that tell the system how long to wait before entering a slow mode, which cuts the operating frequency from 16

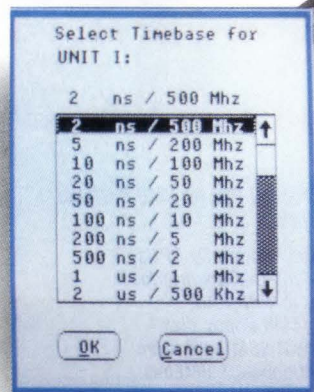
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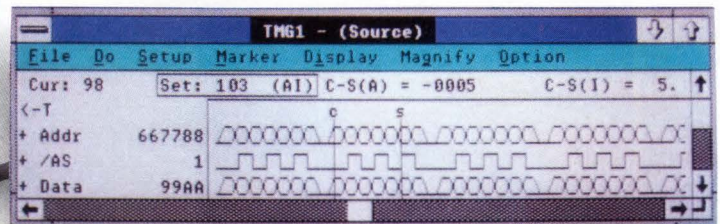
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BUT AS BOARD SPEEDS RISE, THE DESIGNS BECOME MUCH MORE COMPLEX AND ADD NEW COMPLICATIONS.

RICHARD NASS

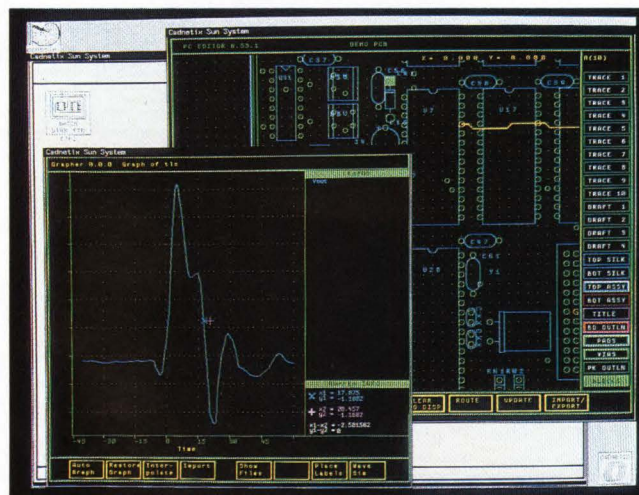
According to a Dataquest survey, 50% of all digital pc boards will run at higher than 50 MHz by 1991. With this acceleration in speed, high-speed board designers will have to pay more attention to layout and circuit problems, such as ringing, undershoot, overshoot, crosstalk, and multiple threshold crossings. Better parts placement, wiring layout, thermal design and circuit design tools, as well as techniques to handle emi/rfi and skin effect in the pc traces, are needed to help solve these critical high-frequency problems. Consequently, trouble-shooting tools are beginning to appear, each one basically tackling a specific aspect of the overall problem.

However, along with the large variety of tools comes the problem of integrating them into one system. Many large companies are developing CAE/CAD tools in-house to solve particular design problems, while simultaneously keeping their technology proprietary. Such companies also frequently look for outside help in finding specific tools that can't be developed internally. In these cases, though, the companies must be prepared to tackle the integration process. But many large CAE/CAD vendors are opening up their architectures to integrate the tools of small niche players. This is good for both users and the small CAE/CAD niche houses.

Few of today's pc-board layout tools

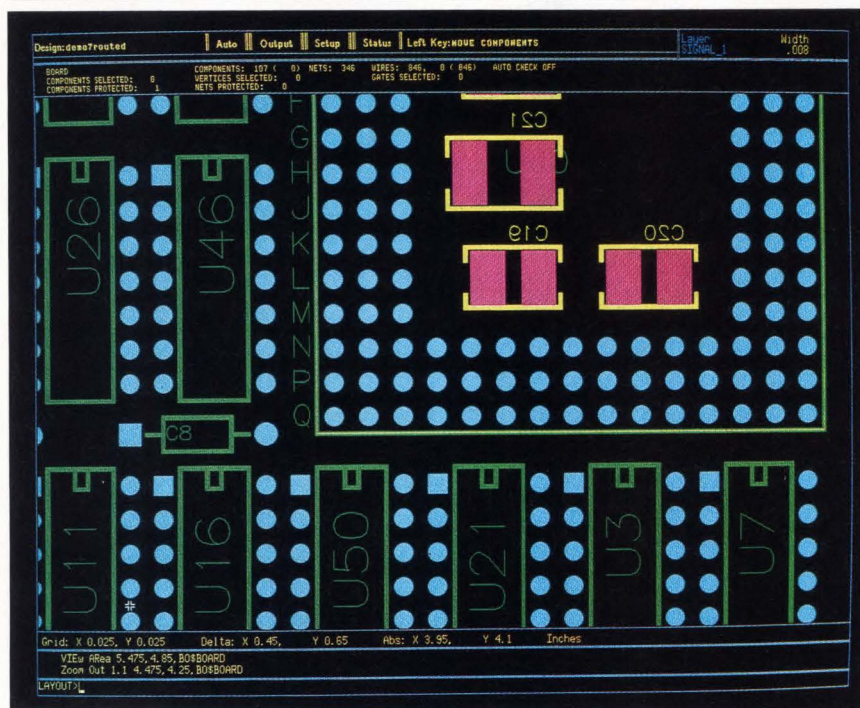
take timing into account—many only help analyze the board's high-speed performance after layout, instead of aiding in board design during layout. Until boards reached the 20-MHz plateau, such pre-layout tools were hardly needed: Experienced designers could compensate for many of the speed-layout problems by tweaking the circuit. At that level, engineers might spend only about 5% of their time ironing out the kinks.

But at higher speeds, the boards have become so sensitive to timing that simple tweaking often ends up doing more harm than good. As a result, it's not unusual for today's designers to spend



1. THE USER CAN SEE an actual board while laying out a design. Furthermore, the Transmission Line Simulator follows the path taken by the design rather than going in its own direction.

HIGH-SPEED BOARD DESIGN



50% to 60% of their time troubleshooting. Timing analysis should be done before a layout design is complete. Even if the logic correctly performs each function, the delay may be too long to meet the specified performance requirements.

ESTIMATING DELAY

Some new tools help designers analyze board designs by estimating the delay and distortion characteristics of high-speed signals. For instance, Valid Logic's Allegro Printed Circuit Board Engineering System can analyze wire delays along with such parasitic capacitances, resistances, and inductances. With this capability, designers can then make simultaneous analyses of reflections, crosstalk, thermal noise, and ohmic loss.

Another problem with today's tools is that they try to solve problems with the tools' own methodology, rather than continuing on the path that the designer took. The en-

gineers at Daisy/Cadnetix, Boulder, Colo., overcame this obstacle with the Transmission Line Simulator, which follows the designer's approach and doesn't re-layout the board. Rather than provide a table of elements, it enables users to see the board as it will appear (Fig. 1). Daisy agrees that there's an integration problem. The company is also interested in further exploring this fron-

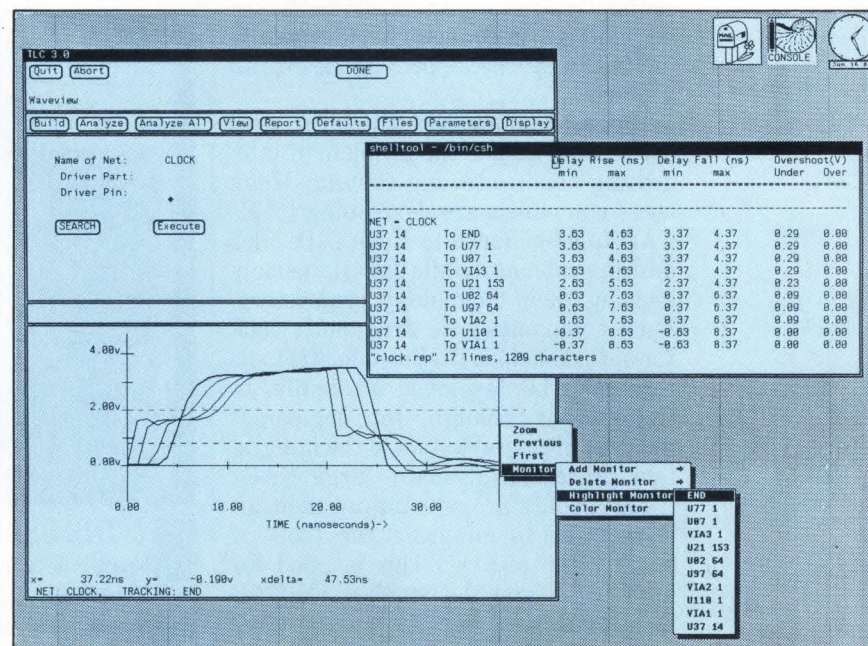
2. BY SEEING the board as it's being laid out, designers can simplify the routing during the placement process.

With the BoardStation, users can move, align, rotate, pivot, and swap individual or groups of components.

tier. In addition, most of the engineers close to pc-board design agree that workstations are—and will continue to be—the place where complex designs will happen.

Timing problems also encompass parts placement. Time-critical parts can't be placed far apart because it will result in long signal paths. Another tool, from Mentor Graphics, Beaverton, Ore., keeps routing "in mind" while doing the placement. The BoardStation allows for angled device positioning, which helps accelerate the placement process (Fig. 2). With a split-screen technique, the software makes it possible for users to move, align, rotate, pivot, and swap individual or groups of components.

Engineers know that the length of the paths is one of the critical aspects of their boards. Those familiar with pc boards, but not with the high-speed aspect, tend to overcompensate. For example, it's not uncommon to see a preliminary design with stubs (length of traces that come off the joint of a t-connection, which



3. THE TRANSMISSION line calculator evaluates the timing of a pc board to determine whether the undershoot or overshoot caused by a reflection exceeds the board's predefined specifications.

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Getting on and off the bus faster

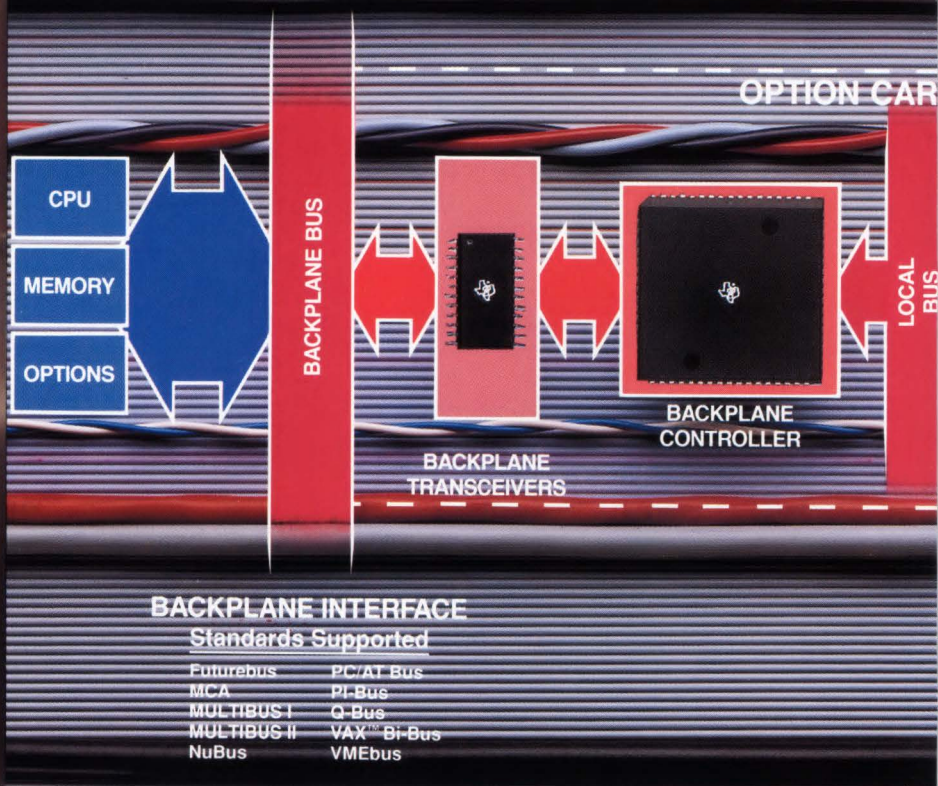
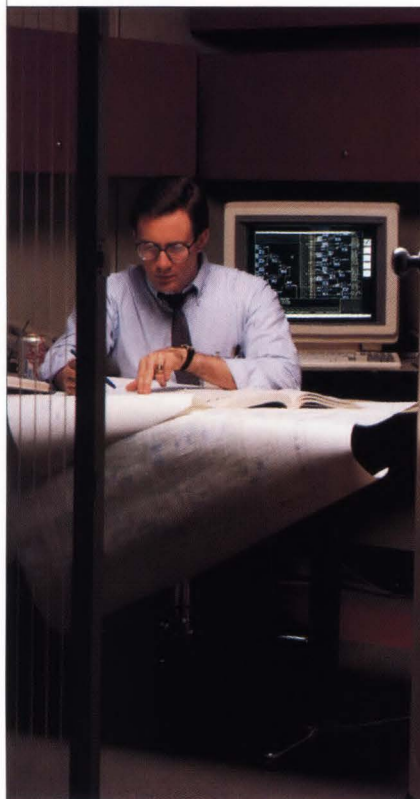
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You not only increase system throughput but cut power and conserve real estate at the same time.



What use is a high-performance CPU if its processing power can't be delivered to the backplane and outward to the peripherals?

Typically, some system throughput is lost at the local bus interface, some at the backplane interface, and some at the peripheral bus interface.

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These devices support the major industry standards listed above so that you can achieve system compatibility regardless of the bus you are implementing.

High-speed, low-power implementation of backplane and peripheral interfaces for most popular standards is made possible by TI's comprehensive family of both digital and analog physical-layer

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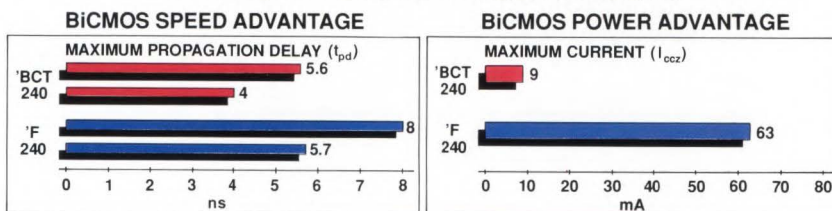
To maximize system throughput, data must be able to get on and off the bus quickly. Therefore, the backplane bus transceivers must be capable of high speed and high drive.

Our high-speed/low-power BiCMOS logic (SN54/74BCTXXX)

is specifically designed for bus interface applications.

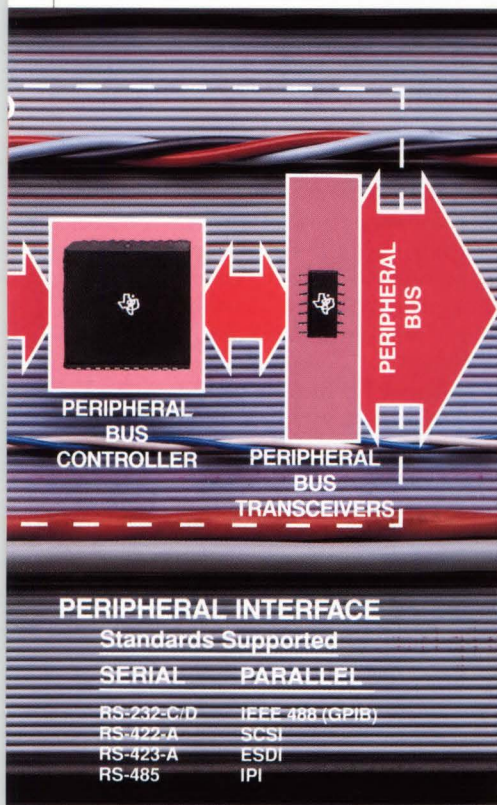
As the name implies, TI BiCMOS merges low-power CMOS with high-speed bipolar, delivering switching speeds comparable to advanced bipolar devices. You also get the 48/64-mA

BiCMOS VERSUS ADVANCED BIPOLAR



The BiCMOS lead over bipolar is proven by this comparison between TI's '74BCT240 and a comparable advanced bipolar standard device. Typical propagation delay of TI's BiCMOS part is faster (left) while power dissipation is less (right).

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ICs. To complete the implementation, TI offers a series of innovative standard and ASIC control devices. Use of TI's leadership bus interface devices can help shorten system design cycles.

drive current you need, and total system power savings can be as high as 25% (see charts).

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Our family of octal ECL translators (SN10KHT/100KTXXXX) delivers a low-power, high-speed translator solution with 48 mA of

drive capability on the TTL side.

Our high-speed Futurebus transceiver family (SN55/75ALS-05X) includes quad and octal devices compatible with Futurebus implementations of the IEEE 896.1 standard. With a drive capability of 100 mA, a 5-ns (typ) propagation delay, and a supply current of 65 mA (max), our SN75ALS053 has the best speed/power ratio of any Futurebus transceiver on the market today. ■

High-performance peripheral interfaces

Peripheral bus interface design decisions revolve around trade-offs between line length, data rate, and noise immunity.

Where data rates are low and

line lengths are short, as with the popular RS-232-C/D standard, the major concern is power savings. However, relatively high voltages (30 V) prevent the use of standard

CMOS devices. Your answer lies with TI's Linear BiCMOS family.

Included are low-power versions of industry-standard quad drivers and receivers (SN75C188/89).

Driver/receiver combinations, ranging from single to quad combinations (SN75C1154), substantially cut package count.

This BiCMOS technology will also allow us to provide charge pump circuitry for single 5-V operation.

Where data rates are high and line lengths are long, as the newer peripherals demand, noise can become a major problem. It is overcome by the use of differential drive. Typically, the major application requirement is higher speeds at, ideally, lower power.

For example, disk drives using ESDI, IPI, or SCSI interfaces will benefit from TI's SN75ALS17X devices conforming to RS-422-A and/or RS-485 standards. These chips are fabricated using our unique IMPACT™ processing that delivers up to 50% greater speed compared to competing products with as much as a 30% power reduction.

IMPACT processing is also behind the unmatched speed of our SN75AS030 RS-422 dual driver/receiver. Typical propagation delays are only 6 ns. ■

No matter which of TI's innovative devices you choose to improve speed, cut power, and reduce real estate at the media interface, the complete bus interface requires another element — controllers. For details on how TI is addressing your needs in this area, turn the page.



High-performance controllers make system design easier.

While the majority of physical-layer devices—those used to implement backplane and peripheral interfaces—transmit data, your system design also requires a device to regulate the flow of that data through the bus interface. To do the job, TI offers a series of controllers that simplify and shorten your task while cutting chip count and improving overall system throughput.

Simplified NuBus design

TI has taken much of the work out of NuBus™ design by introducing the industry's first standard NuBus interface devices. They are the SN74ACT2440 NuBus Controller and the SN74BCT2420 NuBus Registered Transceiver.

A typical implementation, using two 16-bit transceivers and one 32-bit controller (*see below*), replaces as many as 45 discrete devices. Compared to a discrete approach, this solution uses 60% less board space and 90% less power.

Because the necessary logic is embedded within the controller, design cycle time is reduced significantly.

A low-power UART

There is now more need than ever for low-power RS-232 interfaces. Our TL16C450 Universal Asynchronous Receiver/Transceiver (UART), made with CMOS process technology, is an excellent choice for desktop applications and is especially suited for use in laptop/battery-powered units.

A flexible SCSI controller

Available soon, our SCSI controller (designed to conform to ANSI X3.131-1986 specifications) will deliver data rates of 3 Mbytes/s (asynchronous) and 5 Mbytes/s (synchronous).

Unique byte-stacking control logic will allow interface to 16-, 24-, and 32-bit buses. The TI controller will also provide powerful multi-phase SCSI commands, including automatic handling of save-data pointer to minimize interrupts to the host processor. Dual 32-byte FIFOs will provide smooth, efficient buffering between processor and DMA ports.

Customized controllers, too

The NuBus and UART controllers

are available as part of our ASIC standard-cell library.

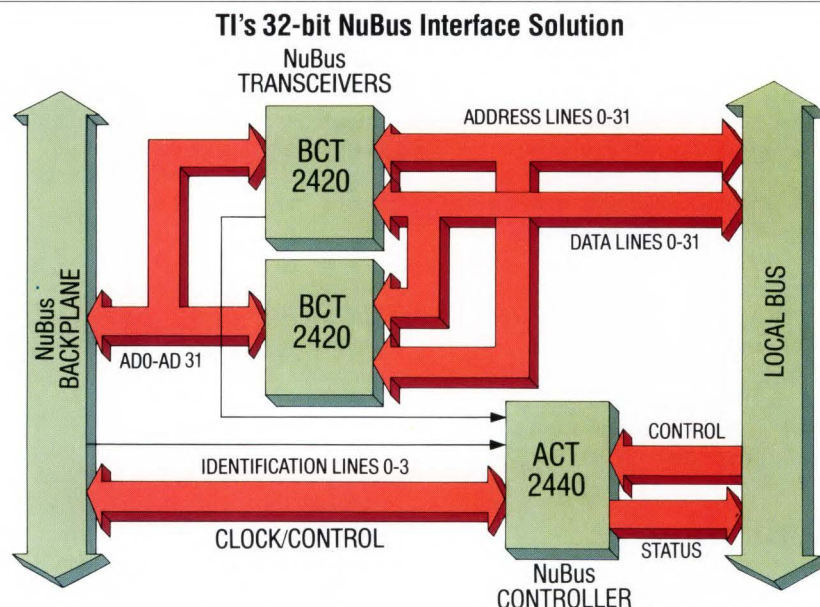
In addition, TI offers TGC100 Gate Arrays and TSC500 Standard Cells as part of our ASIC family which allows you to build the precise chip functions you need. ■

System complexity and the future

As systems become more and more complex, the need will emerge for combining the functionality of controllers and physical-layer devices on a single chip. To that end, TI is applying its acknowledged expertise in physical-layer devices to the design and development of such advanced control-level ICs.

System complexity also brings with it the need for simulation models to make design easier and faster. As a result, we already have simulation models available for more than 1,300 TI devices, including BiCMOS bus interface and ACL logic devices.

Another issue is the increasing difficulty and expense of testing boards in complex systems. Consequently, TI supports the JTAG/IEEE P1149.1 standard with the development of standard products and ASICs having on-chip test cells, as well as with development support software and device models on several leading workstations. ■



Major space savings are realized by using one TI SN74ACT2440 controller and two SN74BCT2420 transceivers to complete a full 32-bit NuBus master/slave interface. As many as 45 discrete logic devices are replaced, realizing significant reductions in board space, power consumption, and design cycle time.

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**TEXAS
INSTRUMENTS**

HIGH-SPEED BOARD DESIGN

might cause reflections) of zero length. This is great, theoretically, but tell that to the engineer doing the routing to implement the zero-length stubs and watch his reaction: He probably won't jump for joy because it's nearly impossible to create a truly zero-length stub—there's always some reflection.

DISPOSE OF CROSSTALK

The most obvious way to eliminate crosstalk is by simply separating the lines, by separating pc-board layers between ground planes, or by putting in an interdigitized ground wire between the offending grounds. In fact, it's ironic that, in the past, crosstalk problems were inadvertently avoided because designers don't make maximum use of space. Inexperienced designers often added extra (and unnecessary) layers to their boards. But this won't work with high-speed circuits.

Some of the new software tools, such as the Crosstalk Tool Kit (XTK) from Quad Design, Camarillo, Calif., can simulate the effects of crosstalk in a digital system. It does this by

supplying a detailed account of the physical, geometrical, and electrical characteristics of all drivers, loads, conductors, and dielectrics in a network.

Another tool that helps designers to judge the effects of changes in the dielectric, line spacings and lengths, and load conditions is the Greenfield, from Quantic Laboratories Inc., Winnipeg, Canada. With Greenfield, users can see an accurate description of their designs by creating matrices relating to the per-unit line length, time delays, inductance, and capacitance. This tool is also one of the few that analyzes before prototype construction. Previously, designers had to guess at these parameters and hope their guess was accurate when testing the completed board.

TOO MANY LAYERS

Often, a design won't fit into the allotted number of layers. When this is the case, what are the choices? With surface-mounting technology, there are many unavailable parts; design-rule changes for center-to-center spacing is more expensive,

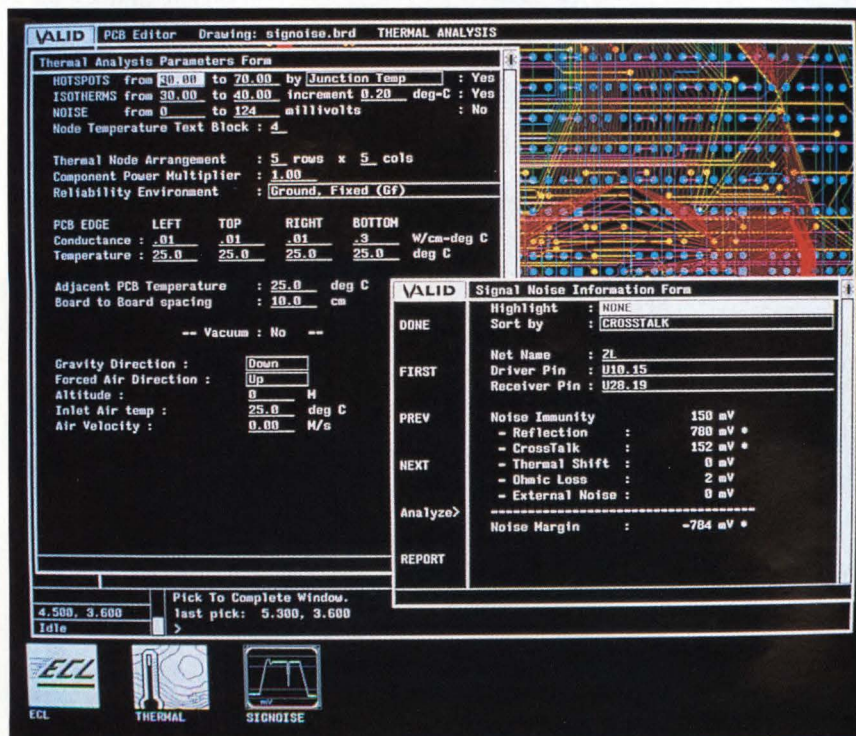
lowers the yield, and changes the impedance of the board; more layers are also more expensive, and device pins might not make it all the way through the board.

There's also radial routing, where the traces are laid out with rounded corners rather than sharp, 90° corners. Nevertheless, although radial routing saves space and can offset some of problems associated with high speed, there's a trade-off. Routing at different angles at different levels makes it difficult to route the board because lands for the device pins may not line up on all layers. This causes many channels to be lost. While some users swear that using different angles has no effect on the board's performance, others say that using 90° angles adds to the reflection. On paper, it seems logical, but this is something that can only be solved by experience.

Reflections from a stub can't be any longer than a device's reset time or the reflections will be seen as false inputs. To some components, this won't make any difference. But in a device such as a counter, where a reflection would be seen as another count, this is critical. By shortening the stub lengths below a certain distance, this false triggering can be avoided.

One way around this problem is to route the board with adequate lengths, then go back and shorten as many as possible without disturbing the board's operation. Some tools can accurately predict whether the undershoot or overshoot caused by the reflection exceeds the board's specifications. For example, the Transmission Line Calculator (TLC) from Quad Design can evaluate network topologies before or after the board is generated. If done prior to generation, the tool makes it possible for designers to tinker with various topologies and loading and termination strategies (Fig. 3).

Reflections can also cause the signal to take an excessively long time to settle. This, in turn, adds to the propagation delay and can also be predicted by the TLC as it goes through the board on a net-by-net basis.



4. ALLEGRO'S SIGNAL-NOISE ANALYSIS TOOL identifies distortion errors caused by dissimilar operating temperatures. It then uses the user-defined data to complete its analysis.

HIGH-SPEED BOARD DESIGN

Sometimes, high-speed boards employ complementary signals, where two signals must arrive at their destination at exactly the same time and not out of sequence. The lengths of these differential pairs must be the same. Again, it's asking a lot of the router to make the signal paths exactly the same length. And this would probably go unnoticed until the route-analysis stage, at which point the designer would have to go back into the layout, analyze one of the lengths, and adjust the other accordingly.

OUTSIDE INTERFERENCE

High-speed, sensitive signals are affected by the environment's elements. These signals can be isolated from interference by being laid between planes. Alternatively, these highly-sensitive signals can be routed with more clearance than the less sensitive lines, so they don't pick up

interference from parallel running signals. Both rfi and emi are generally measured after prototyping. This is because there no available tools can predict this interference.

Thermal considerations are prevalent on all pc boards, but they become even more of an issue with high-speed boards, which tend to be multilayered and densely packed with components. Consequently, a quality thermal-analysis package is essential to high-speed design. Another way to tackle the thermal-analysis problem is to do a flow analysis at the same time that the placement is done.

As the trend toward using automated tools has continued, Valid's Allegro has upgraded to include thermal-analysis capabilities. The tool applies user-specified design rules to the board in its analysis rather than following a standard path (Fig. 4).

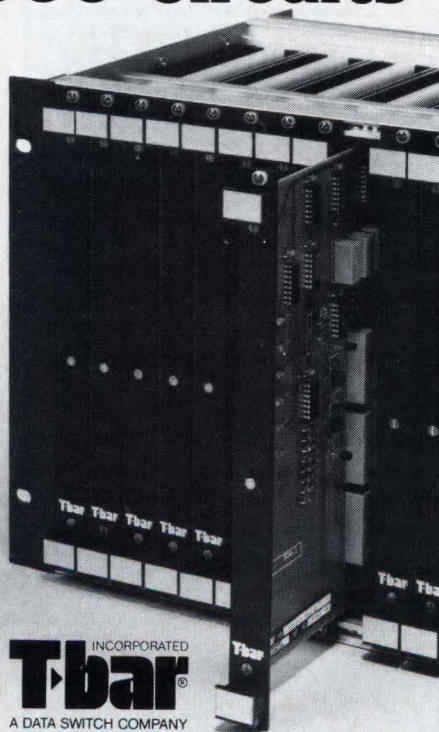
At very-high frequencies, skin effect in a wire can cause degradation. This area hasn't received much attention, so designers must once again rely on their own experiences. As frequencies get higher, the current that flows through the wires tends to run nearer to the wire's edge and further away from the center, making it look like a higher resistance. This effect (skin effect) causes a rise-time distortion that must be accounted for.

A simple solution is to use a wider or thicker wire with a larger surface area. The trade-offs here are that wider wire takes up more space and nobody wants to make a board any bigger than they have to. □

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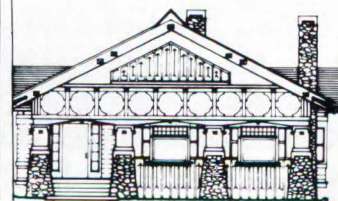
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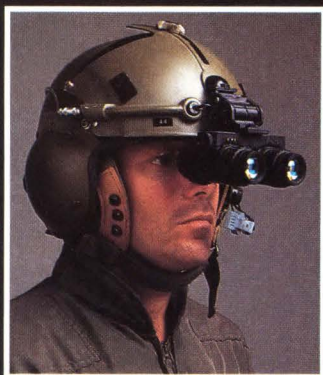
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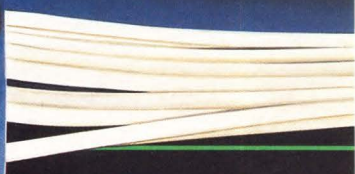
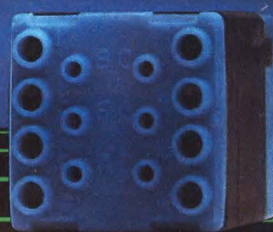
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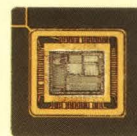
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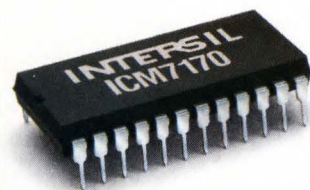
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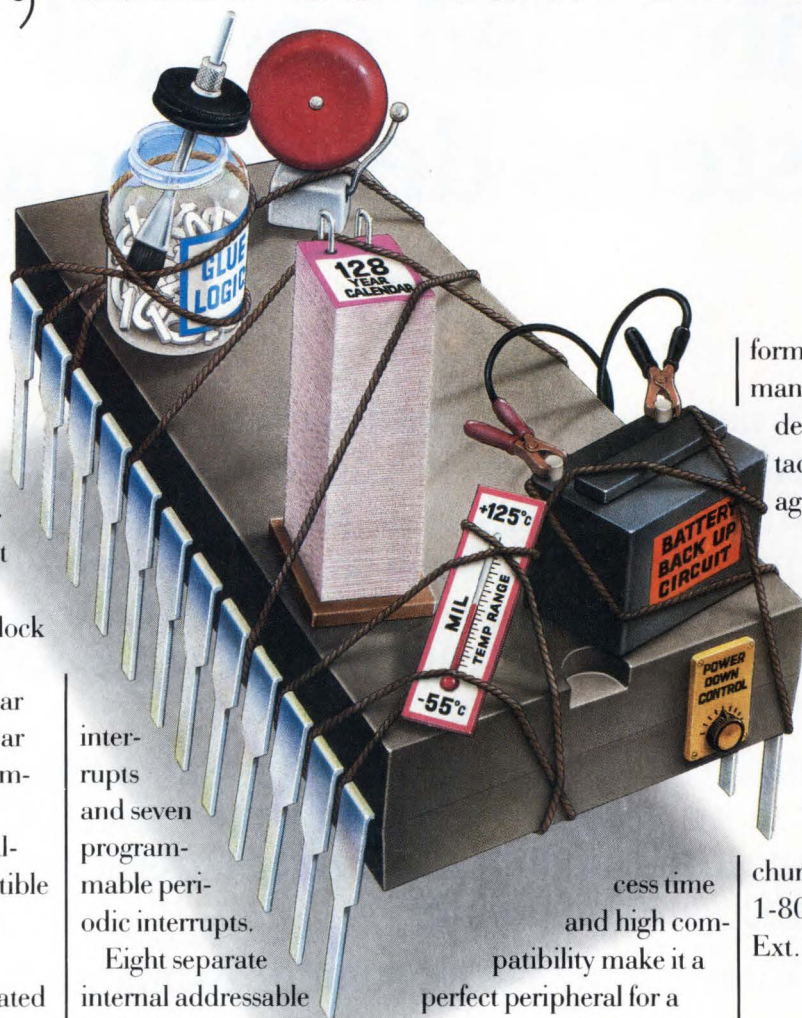
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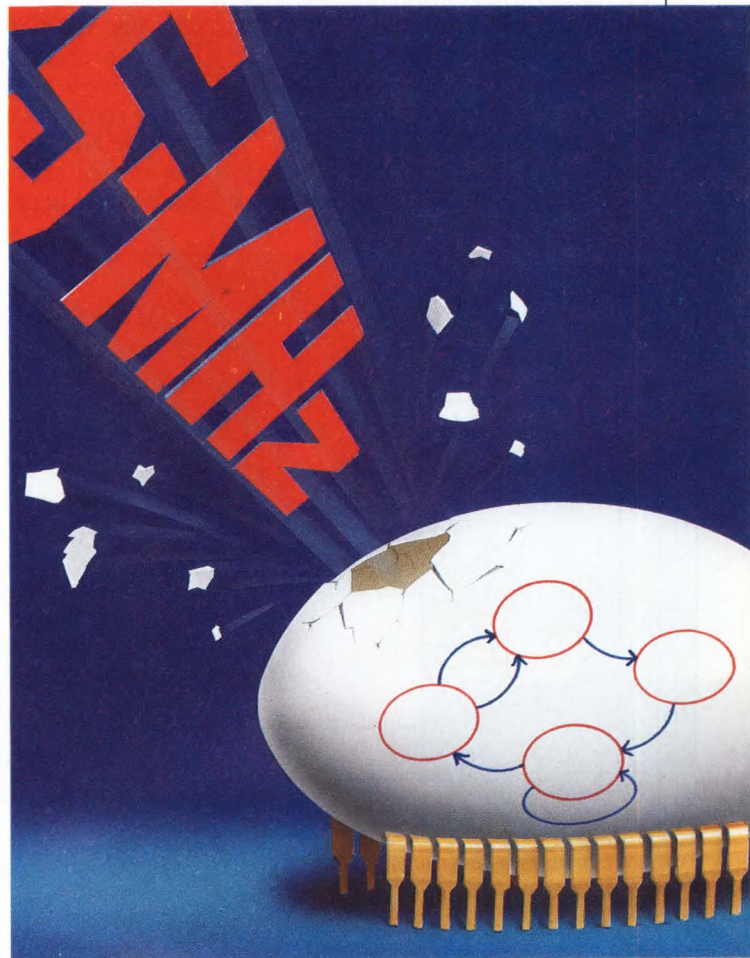
WITH NOVEL SPLIT-PLANE ARCHITECTURE, A CMOS PLD BUILDS THE FASTEST STATE MACHINES EVER WITHOUT COMPROMISING FLEXIBILITY.

PROGRAMMABLE SEQUENCER HITS 125-MHz CLOCK SPEED

DAVE BURSKY

Although VLSI chips currently enable systems to operate at clock rates well over 50 MHz, TTL-compatible glue logic has now become a performance limiting factor. As today's system clock speeds hit 40 and 50 MHz, standard TTL-compatible programmable logic devices (PLDs)—now an essential part of any system—are hard-pressed to keep pace with VLSI chips. They often must operate at twice the clock frequency of the VLSI circuits. Today's fastest bipolar or CMOS PLDs run at peak system clock frequencies of about 33 to 40 MHz; a few low-complexity ECL and GaAs programmable parts can run even faster. However, next-generation systems, with their higher clock frequencies, will demand still faster TTL-compatible programmable chips to handle the sequencing, control, and signal routing at speeds of 66 MHz and higher.

To solve this speed problem without moving to a more exotic or costly technology, such as GaAs or bipolar ECL, engineers at Cypress Semiconductor developed a novel split-plane architecture PLD. Unlike most other programmable chips that have the state registers fed by the output plane, the CY7C361 has its 32 state-register macrocells situated between the input logic plane and the output OR plane to balance the propagation delays (*Fig. 1*). With the split-plane structure, the 28-pin circuit can operate with external



clock frequencies of over 66 MHz and internal frequencies of close to 125 MHz.

The higher speed made possible by the 7C361 will open up such applications such as cache and I/O subsystem control, asynchronous system control including dataflow organizations, high-speed real-time embedded control, and many other state-machine-based sub-

COVER: HIGH-SPEED PROGRAMMABLE SEQUENCER

systems. Furthermore, its CMOS UV EPROM technology keeps the power consumption to just 700 mW, even at the 125-MHz maximum internal clock frequency.

In the traditional state machine built with a programmable logic array that incorporates registers on the output lines, the values held in the registers represent conditions or states. Those values must be fed back to the state machine's input in time to be available for the next clock cycle. In addition, the values in the state registers must propagate to the output pins so that external circuits can be controlled before the next clock cycle begins. These timing requirements are what limit the operating frequency of the typical PLD state machine.

For the state machine to operate properly, the clock period (t_p) must

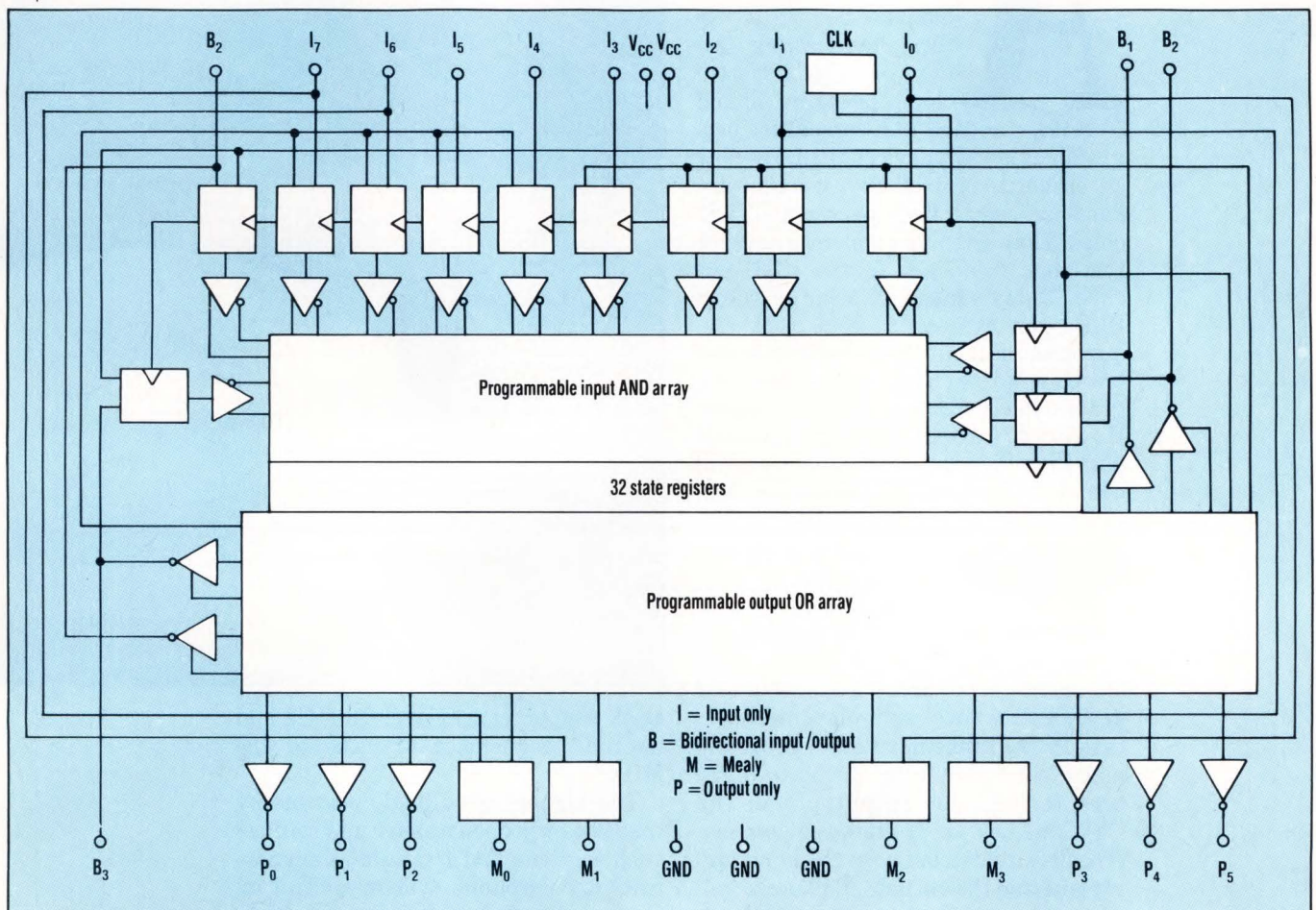
be as long as the longer of two cycles: the clock-to-output delay, (t_{CKO}) or the sum of the feedback and setup times ($t_{CF} + t_s$). In most single-plane programmable PLDs (PAL-type devices) with registers at the outputs of the fixed-OR array, t_{CKO} is small but the sum of t_{CF} and t_s is large. The more flexible two-plane-programmable PLDs (PLA-type chips) increase the length of the feedback path and unbalance the delay further. As a result, the maximum clock frequency goes down and the state machine operates slower.

By placing the registers in the middle, the CY7C361's programmable input logic plane (the input-condition array) feeds the array of registers. These registers can then feed a programmable OR plane (the output translation array), or they can feed back to the logic plane array inputs.

That middle location minimizes the length of the feedback path and moves the registers closer to the inputs. The net result is that the feedback delay time from the register output, plus data setup time, is reduced relative to the clock-to-output delay time (t_{CKO}).

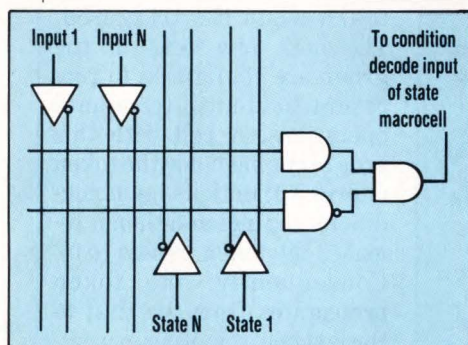
Consequently, the t_{CKO} value in the 7C361 is actually replaced by the delay measured from a clock to a de-skewing output buffer (t_{CD}). But the output signals from the output translation array would appear considerably skewed if they directly fed an external circuit. To avoid any skew problems, the array outputs are captured in a de-skewing buffer that synchronizes the output signals.

A Latch-Enable signal, generated by the clock input and traversing an independent path parallel to the out-



1. A NOVEL SPLIT-PLANE ARCHITECTURE places the state-machine macrocells between the input array and the output array. It balances the on-chip delays and makes internal operation possible at clock frequencies of 125 MHz.

COVER: HIGH-SPEED PROGRAMMABLE SEQUENCER



2. INSTEAD OF the usual AND logic plane, Cypress employs configurable condition-decoding logic, which combines AND and OR operators.

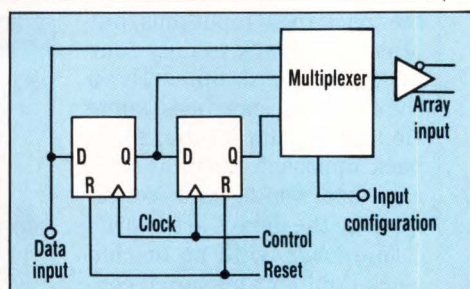
put array, has a delay equal to the worst possible delay that can occur in the output array. This signal latches the 7C361's outputs every 8 ns or less after the state clock, with a skew of no more than 1 ns when two outputs are switched, or 3 ns total when all outputs are switched. To obtain maximum performance, the internal delays must be balanced so that $t_{CD} = t_{CF} + t_S$ and neither t_{CF} nor t_S becomes one performance-limiting factor. The placement of the registers

between the arrays balances the two paths at 8 ns. The circuit can then operate at 125 MHz, the reciprocal of the time delay.

Along with the novel placement of the state registers, the array architecture uses an unusual logic structure that employs a scheme called condition decoding, which combines AND and OR logic (Fig. 2). The signal doesn't encounter the delays it might otherwise incur if propagated through a PAL-type array where up to 19 product terms must be dealt with.

The architecture is the first silicon implementation of a programmable Petri net. The Petri net is an analysis tool typically used to evaluate concurrent state machines. And by implementing it in programmable logic, building concurrent state machines can be simplified.

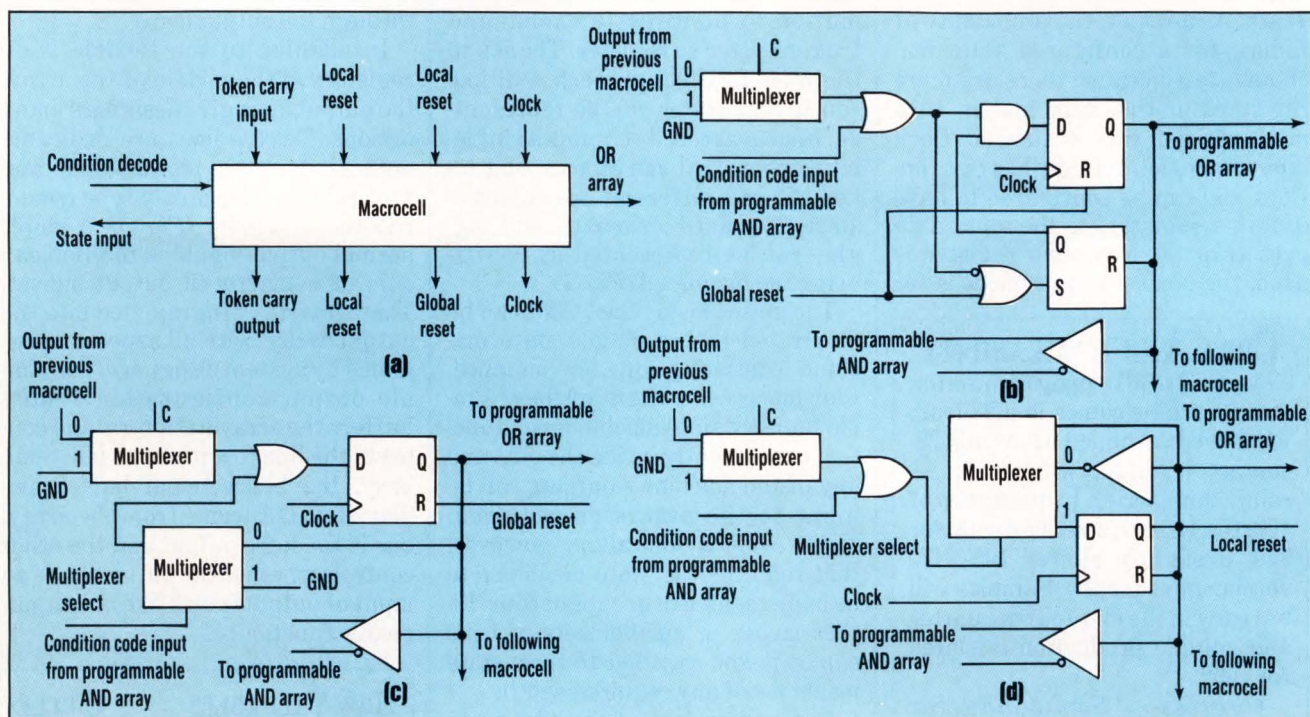
In the chip, if states are represented as S_0, S_1, \dots, S_N , and inputs as a, b, c, \dots, z , then the decoder indicates a general form of logic: $(S_0 + S_1 + S_3 + \dots S_N) \cdot (a \cdot b \cdot c \cdot \dots z)$, including cases in which any states or inputs are replaced by their nega-



3. WITH INPUT macrocells, designers can trade off metastable immunity at the expense of lower throughput by putting either 0, 1, or 2 registers into the input data path. The double-register option is targeted for applications that need synchronization.

tions. For example, the criterion for entering the state S_J from state S_0 or S_1 might be programmed as $(S_0 + S_1) \cdot (a \cdot b)$, while the criterion for leaving state S_J might be $(a + b + c) \cdot S_J$.

Additional streamlining of the logic array was achieved by limiting the register feedback network. Not all of the registers feed back to every input of the condition-decoding array. Some of the registers supply



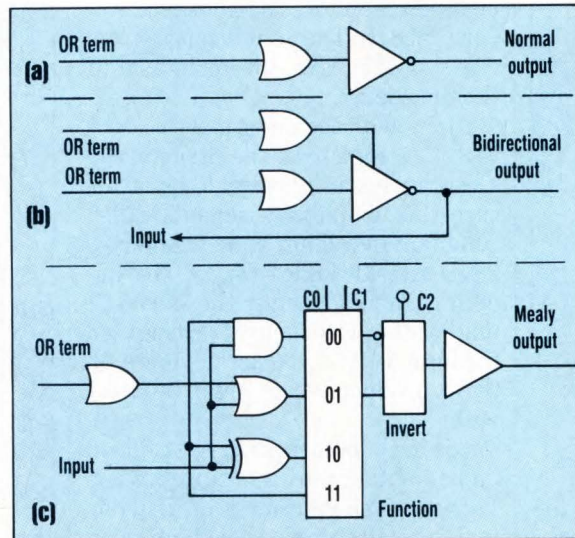
4. STATE-MACHINE REGISTERS can be configured into three types to ease system design (a). The start option creates a token based on a condition decode (b), and the hold-until-terminate option captures a token and maintains it until a particular condition is decoded (c). Lastly, the toggle option is used to implement counters (d).

COVER: HIGH-SPEED PROGRAMMABLE SEQUENCER

feedback to all input pins, but others feedback to only four or eight local pins. Even though this sacrifices some flexibility, the limited-feedback approach keeps the array size small, and consequently the delays are short.

Moreover, with an on-chip clock doubler and signal-conditioning circuit, the PLD can operate internally at 125 MHz, even though the external system clock frequency is 62.5 MHz. That same circuit also prevents asymmetric clock waveforms from causing internal timing problems. The circuit will "square-up" input clock signals that have uneven duty cycles.

The array also has 8 to 12 registered macrocell inputs. Each input macrocell is metastable hardened to minimize state-machine failures caused by metastable phenomena. With all inputs switching at the maximum frequency, one metastable event that can violate the setup-time window of the second input register could occur once every 10 years. As a result, the probability of failure for a configured state machine is low because there are more registers in the chip, and in turn more decision time is allowed. Each input macrocell actually has two flip-flops and can be configured to have 0, 1, or 2 registers in the input data path (Fig. 3). When no register is used, the largest requirement is for



5. PROGRAMMABLE OUTPUT CELLS make it possible for users to have output only, bidirectional, or Mealy-type combinatorial outputs from the chip.

the input's setup-time; one register cuts the time in half. The double register configuration is used for asynchronous input signals.

A shift-register interconnection scheme with token-passing logic simplifies state-register macrocell usage and makes it possible for information to be directly exchanged from register to register. Thanks to this more flexible approach, multiple concurrent states can be represented. Each macrocell contains a single-bit register that can store a 1-bit token. Three different operations—start, hold-until-terminate, and toggle—can be represented by configuring the macrocell (Fig. 4).

The states inside the 7C361 can be illustrated with a simple state machine consisting of, for instance, four macrocells. Eight of these simple four-cell state machines can function concurrently inside the chip and any of the machine's outputs can be input to the others as required. There isn't a limitation, however, that requires the state machines to be implemented in groups of four. Either larger or smaller sets of cells can be linked together to form state machines of any required width.

In the operation of the 4-bit state machine, the first macrocell is programmed to represent the Start operation—a function that initiates a

token when it's triggered. The next few cells in the group are configured to represent hold-until-terminate operations. A cell with this programming holds the token (stores a 1) until its input conditions are met and then it releases the token (resets to 0). Consequently, the token propagates from the first to the last cell, resulting in a pattern sequence of 0001, 0010, 0100, 1000. Alternately, the cells can be configured for toggle operation to implement simple counter chains. When enabled by the condition-decoding logic, the cell toggles between its 1 and 0 states at the chip's clock frequency (it alternately stores and releases the token).

Although states of individual cells are simple because they represent the presence or absence of a 1-bit token, the input conditions can span a wide range because they're determined by the condition-decoder array programming. The outputs of selected sets of cells can also be ORed through the output array.

In addition to the flexible state registers in the middle of the array, the output lines give designers many options. Twelve lines are dedicated outputs, four are bidirectional, and four others offer Mealy-type combinatorial capability (Fig. 5). A chip's normal output signal is the Boolean sum of a macrocell output subset. That subset is programmed into the output array, with all aspects determined by system designers. The simple output configuration simply buffers the array's OR term and connects the line to a package pin. Similarly, the bidirectional buffer employs two OR terms from the array: one is the logic output and the other controls whether the pin serves as an input or output (much like an output-enable function). □

PRICE AND AVAILABILITY

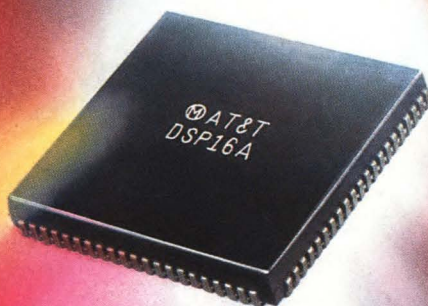
The CY7C361 programmable state machine comes in a 28-lead, windowed ceramic DIP or in a 28-contact leadless, windowed, ceramic chip carrier. In quantities of 100, the 125-MHz version sells for \$40; a slightly slower 100-MHz version goes for \$34. Samples will be ready in the mid-fourth quarter and volume production is slated for 1990.

Cypress Semiconductor Corp., 3901 N. First St., San Jose, CA 95134; Al Graf, (408) 943-2600.

CIRCLE 514

HOW VALUABLE?	CIRCLE
HIGHLY	559
MODERATELY	560
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problems of asymmetrical inputs and noisy, long settling tails associated with many current-feedback op amps. It has all the speed needed for RF/video buffering, PLL amplification, peak detecting, and signal

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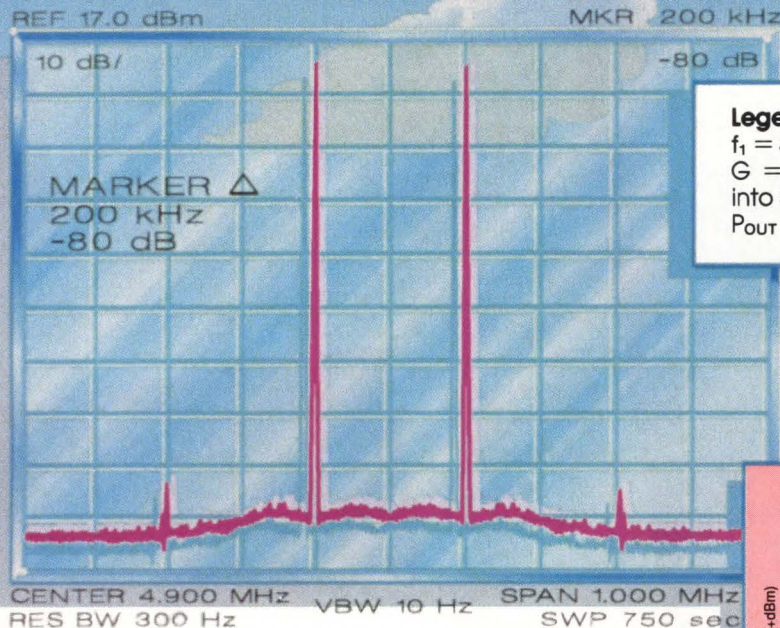
An internally compensated model, OPA620, is also available for unity-gain applications. Besides low distortion and high output drive, it settles to 0.01% in 25ns. Gain-bandwidth is 200MHz.

Design Tools

Burr-Brown makes it easy to put these parts to work in your system. The product data sheets include valuable charts and RF applications information. Demonstration PC boards

are also available to speed layout and evaluation. You can also use our SPICE models; ask for AN-167. Contact your sales rep or call

1-800-548-6132 for immediate assistance.



Legend:

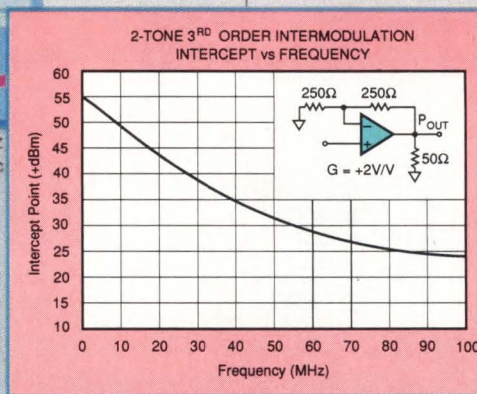
$f_1 = 4.8\text{MHz}$, $f_2 = 5.0\text{MHz}$
 $G = 2\text{V/V}$, $V_{\text{OUT}} = 5\text{V}_{\text{p-p}}$ into 50 Ω .
 $P_{\text{OUT}} = 12\text{dBm/ tone}$

For example, in gains of 2V/V and above, the uncompensated OPA621 can drive 5Vp-p into 50 Ω at 5MHz with a very low 3rd-order intermodulation ratio of -80dBc. This excellent low-distortion performance simplifies filtering tasks and improves signal purity. OPA621's classic op amp design also avoids the

distribution applications. Plus, its high current output lets you drive multiple cables and other heavy loads easily and economically.

Key OPA621 Features

- Bandwidth, 500MHz ($G = 2\text{V/V}$)
- 2-tone IMD at 5MHz, -80dBc



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CIRCLE 83

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BB

Opto-Isolated RS-232 Transceivers Improve Quality of Data Transmission

Isolated RS-232 data lines can prevent damage and possible injury that might occur when a data line makes accidental contact with a power line. Isolating the lines also reduces noise and improves data transmission, by interrupting potential ground loops.

Three new Maxim products offer this protection: the MAX250, 251, and 252 combine data-line isolation with a dual RS-232 transceiver. These devices add to the MAX230-240 series of RS-232 transceivers, boosting the number of devices in that family to 22 (see chart). The new transceivers, in which the isolation barrier is included (MAX252, Figure 1) or assembled externally by the customer (MAX250 and MAX251, Figure 2), allow designers to incorporate in their systems the evolving applications for RS-232 lines.

RS-232 lines can connect two pieces of equipment that are side by side, in different rooms, or in different buildings. The ground potential in separate buildings can differ by many

volts – and in some cases, connecting these "grounds" with an RS-232 cable can cause a spark at the connector housing. The spark itself may be of no consequence, but it may indicate that the cable, when connected, will conduct fluctuating levels of noise current.

Consider, for example, a manufacturing operation in which the RS-232 lines between a data logger and host computer pass near a large motor. At startup, the motor can induce a momentary 50V difference between ground potentials at the data logger and computer – and if the grounds are not isolated, data may be lost during the surge interval. In addition, isolation blocks the voltage spikes that might otherwise damage the computer.

Apart from isolation, the new transceivers have much in common with other products in the MAX230-240 series. These devices meet a variety of system requirements by offering many combinations of features. For a specific application, some subset of the family

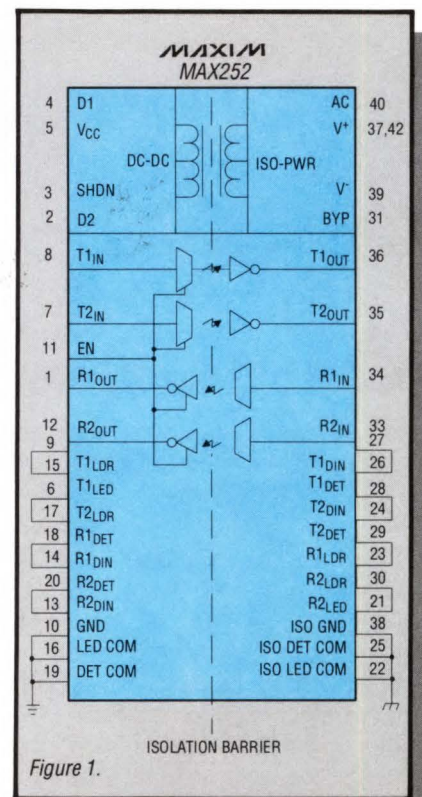


Figure 1.

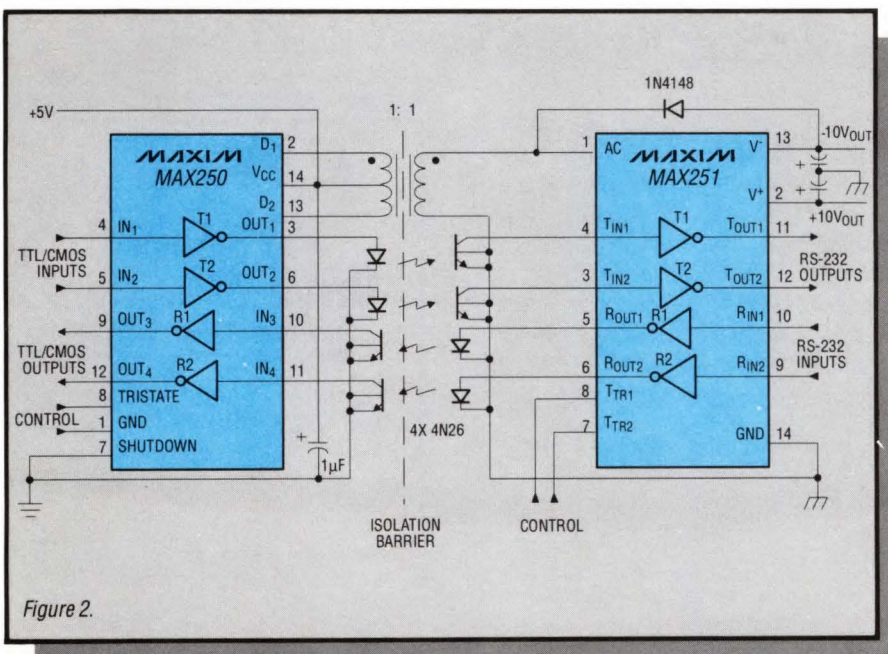


Figure 2.

usually provides the exact number of receivers and transmitters required. Most of the products operate on a single +5V supply, others accommodate a higher supply voltage. Until recently, the features that further differentiated this family were low-power shutdown, 3-state inputs, and the provision of internal charge-pump capacitors. Now, designers have the additional option of optically isolated RS-232 data lines.

Breaking the Isolation Barrier

Small size, reasonable cost, and fast response have mandated the use of opto-isolation (rather than magnetic isolation) in data channels. However, a transformer is necessary for transmitting power across the barrier, to the IC on the cable side. Accordingly, the MAX252 contains two ICs (the MAX250 and MAX251), four opto-couplers, a

Part Number	No. of RS-232 Drivers	No. of RS-232 Receivers	Ext. Caps.	Shut-down	Receivers Output 3-State	RS-232 Driver 3-State	Pins	Price (100up)
MAX230	5	0	4	Y	-	-	20	\$4.00
MAX231 [†]	2	2	2	-	-	-	14	2.40
MAX232	2	2	4	-	-	-	16	3.60
MAX232A	2	2	4	-	-	-	16	3.60
MAX233	2	2	0	-	-	-	20	4.45
MAX234	4	0	4	-	-	-	16	3.60
MAX235	5	5	0	Y	Y	-	24	9.00
MAX236	4	3	4	Y	Y	-	24	4.40
MAX237	5	3	4	-	-	-	24	4.40
MAX238	4	4	4	-	-	-	24	4.40
MAX239 [†]	3	5	2	-	Y	-	24	4.00
MAX240	5	5	4	Y	Y	-	44	6.00
MAX241	4	5	4	Y	Y	-	28	6.05
MAX242*	2	2	4	Y	Y	Y	18	3.75
MAX243*	2	2	4	-	-	-	16	3.60
MAX244*	8	10	4	-	-	-	44	9.00
MAX245*	8	10	0	Y	Y	Y	40	15.00
MAX246*	8	10	0	Y	Y	Y	40	15.00
MAX247*	8	9	0	Y	Y	Y	40	15.00
MAX248*	8	8	4	-	Y	-	44	9.00
MAX249*	6	10	4	-	Y	-	44	9.00
MAX250	2	2	-	Y	Y	Y	14	4.00
MAX251	2	2	-	Y	Y	Y	14	4.00
MAX252	2	2	0	Y	Y	Y	40	25.00
MAX1080*	2	2	4	Y	-	Y	18	3.75

[†]+5V and +12V powered. All others are powered by +5V only.

* Scheduled to be introduced Fall 1989

small toroid transformer, two diodes, and four capacitors, all in a low-cost, 40-pin plastic DIP. This transceiver offers transmission rates as high as 9.6 kbaud.

One can envision the MAX252's isolation barrier as a line running lengthwise along the middle of the DIP. Pins on one side give access to the nonisolated or "logic" side of the barrier, and pins on the other side of the DIP give access to the barrier's isolated or "cable" side. To guarantee the barrier's integrity, Maxim has applied to the Underwriters Laboratories for a product listing that should become effective in the fourth quarter of 1989. The UL listing will reflect the high-voltage testing of all parts.

The present design's 500 VAC rating, for instance, requires that each part withstand 600 VAC for two seconds. (The test involves shorting together the pins on each side and applying voltage between the shorted groups: either 500 VAC for one minute, or 600 VAC for two seconds.) Later versions of the MAX252 will carry a rating of 1kV or higher. The potential applications for this device include any RS-232 link of 9.6 kbaud or less. Industrial systems such as the elevator, for example, are notable for electrical surges.

90-kbaud Data Rates

An engineer can optimize the transceiver's transmission speed by selecting the barrier's isolation compo-

nents, which set the baud-rate limit. The plastic-encapsulated MAX252 doesn't allow that choice, but its two internal ICs are available as the MAX250 and MAX251, separately packaged in 14-pin DIPs. If an application requires higher isolation voltage or a transmission rate higher than 9.6 kbaud, one should consider building an isolated-data transceiver based on the MAX250 and MAX251. The external isolation barrier will require four opto-couplers and a small transformer.

A barrier based on model 4N26 opto-couplers (available from Motorola, TRW, and others) can achieve double the MAX252's baud rate, i.e. 19.6 kbaud. Or, the transceiver's two ICs can support rates as high as 90-kbaud when combined with model 6N136 opto-couplers (available from HP, TRW, and Quality Technologies). Although 20-kbaud is the maximum practical transmission rate specified for RS-232 lines, low line capacitance enables higher rates in some systems. For these, the MAX250/251 can provide isolated data transmission.

In selecting a transformer, the MAX250/251 data sheet offers some guidance in specifying the electrical characteristics and choosing a vendor. The data sheet also shows a recommended topology (not the actual pc traces) for layout of the transceiver on a single- or double-sided pc board.

A complete transceiver, like the self-contained MAX252, provides two RS-232 inputs and two RS-232 outputs. These serial ports conform to all requirements of the EIA RS-232D specification and to the CCITT recommendation V.28. Both transceivers have a low-power shutdown mode, in which the power consumption drops to 5 microwatts and the transmitter outputs go to the high-impedance state. Both transceivers derive their $\pm 10V$ supply voltages from an externally applied +5V on the barrier's "logic" side. Using a patented charge-pump converter technique, the transceivers convert +5V to +10V, and then convert +10V to -10V.

★ FREE ★ +5V RS-232 Driver/Receiver Data Booklet

Comprehensive descriptions and applications information on Maxim's RS-232 products.

(CIRCLE 11)

For **FREE SAMPLES** or applications assistance, call (408) 737-7600 or write Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086.

LISA GUNN

DSP IS TAKING OVER MANY ANALOG AREAS AND OPENING UP NEW DOORS.

or function-specific parts; and general-purpose or single-chip processors. Many single-chip devices tailored to a specific application are also coming on the scene. In addition, within each type there are floating-point and fixed-point parts, and devices of many different bit sizes.

The main difference between the two types of DSP chips is that single-chip devices implement a DSP algorithm in software and the building-block chips implement the algorithm in hardware. The building-block approach is used at the higher end of the price and performance spectrum; and the general-purpose devices are at the lower end.

There are several styles of solutions to serve DSP applications. For the high-end of the performance spectrum, designers pick a collection of fairly special-purpose building blocks and build a solution that solves that one problem well. The hardware design ends up looking like the flow chart that it implements. For the lower end, designers would use one of the general-purpose, single-chip DSPs.

The performance boundary between the building-block and single-chip solutions is sometimes hard to determine. According to Joel Dedrick, director of product marketing for Logic Devices Inc., a good rule of thumb is if the sample rates are above 1 MHz, a single-chip DSP device won't work.

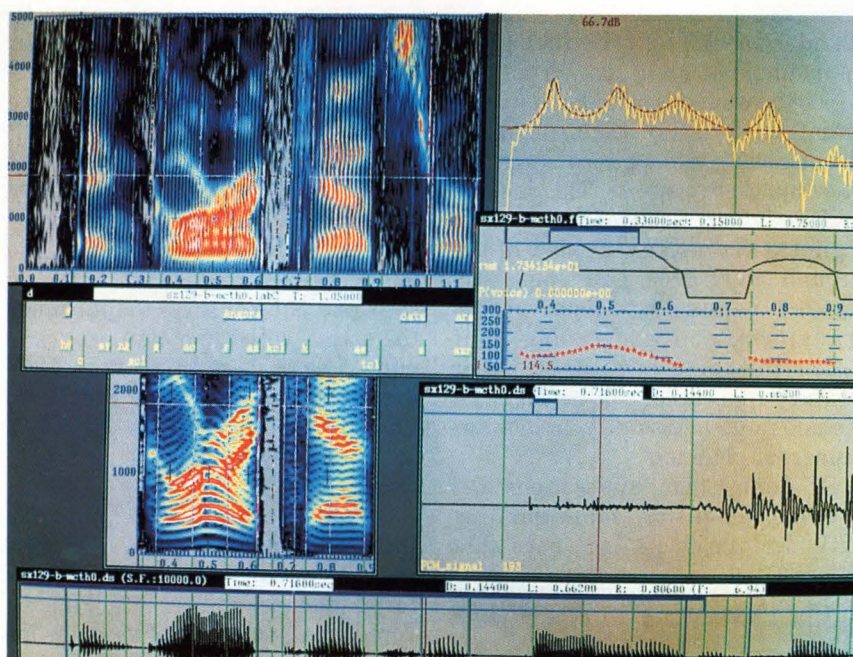
When looking at DSP performance, a good quantity to consider is the millions-of-operations-per-second

DSP UPROOTS TRADITIONAL ANALOG JOBS

Processing digital signals is faster, easier, and more precise than processing analog signals. Consequently, a proliferation of digital-signal processing (DSP) chips are invading the turf originally ruled by analog-signal processors. And this invasion is resulting in completely new applications.

Many designers know little about the relatively new practice of DSP. The truth is that any DSP task can be handled by an ordinary microprocessor. What sets a digital-signal processor apart is its ability to handle those tasks extremely quickly (see "What makes a digital-signal processor?," p. 50).

There are basically two types of DSP chips available: building-block



DIGITAL-SIGNAL PROCESSING

ond rate. The MOPS rate is the product of the sample rate and the number of operations needed per sample. Single-chip devices can do up to about 10 MOPS—a building-block approach is usually needed above that.

Real-time video is an example of an application on the performance-dividing line's upper side. Considering the number of scan lines multiplied by the number of pixels per line multiplied by a scan rate of 1/30th or 1/60th of a second, pixel rates could go as high as tens of MHz. This is beyond the capabilities of single-chip devices.

Other high-end applications can be

found in the military. Dedrick gives an example of an attack aircraft in which the weapons officer must have an infrared view of the ground. As the plane is tumbling and diving, the view must stay stable. This is done with an infrared sensor mounted on a gimbal that makes the view of the ground stay stable. DSP chips handle the various real-time, image-transformation processing that makes the perspective right. Other military applications for the high end include radar and sonar that monitor numerous channels.

Dr. John Eldon, applications and product-definition manager for TRW LSI Products Inc., says that

systems built with building-block, or algorithm-specific parts, don't require as much software as do those built with a general-purpose DSP chip. For instance, DSP chips in the Texas Instruments TMS320 family need lots of programming to perform a fast Fourier transform. The building-block parts from TRW do the same thing at three to four times the speed, with almost no programming. The trade-off is that the TRW parts offer only specific functions. Three main applications for TRW parts are video, imaging, and military.

Signal Processing Technologies Inc. (SPT) manufactures a DSP chip-set specifically designed for performing fast Fourier transforms. Tom Kopet, manager of systems architecture, and Phillip Roberts, senior systems engineer, believe that the SPT set doesn't compete with the general-purpose digital-signal processors, which are aimed at a broad base of lower-cost and higher volume applications. The SPT parts are made for high-performance applications that specifically require fast Fourier transforms. SPT went after the fast Fourier transform because it's an algorithm with a wide range of applications. The chip set is meant for use in military, high-speed image processing, and filtering in the frequency domain.

There are many building-block DSP devices available that cater to one specific application area. Inmos Corp. manufactures chips specifically for radar, machine vision, and image compression (*Fig. 1*). Andrew Rabagliati, U.S. central applications manager, states that Inmos' image-compression chip is only good for a system that works with and stores images.

Building-block chips come in both fixed-point and floating-point versions. Some functions, such as the fast Fourier transform, are too complex to build in floating point. Designers obtain a floating-point, fast-Fourier-transform function by building it from floating-point multipliers and adders.

Floating-point math works well in the single-chip devices, where every-

WHAT MAKES A DIGITAL-SIGNAL PROCESSOR?

Any microprocessor can handle a DSP algorithm given enough time. But DSP applications are generally real-time in nature, and they require more performance than a microprocessor can give. Consequently, digital-signal processors were developed to offer the required high-speed number crunching.

What exactly is a digital-signal processor, and how does it differ from a microprocessor? According to Henry Davis, director of DSP products, and Bob Fine, applications manager at Analog Devices Inc., there are five fundamental digital-signal-processing application requirements.

A digital-signal processor is distinguished from other types of microprocessors by how well it performs each of these five requirements: The first requirement is fast and flexible arithmetic. Single-cycle multiplication, multiplication with accumulation, shifting, and standard arithmetic and logic operations are a must. In addition, the chip's arithmetic units must handle any computation sequence. In this way, the DSP algorithm can be executed without being reformulated.

A second requirement is extended dynamic range on the mul-

tiply-with-accumulation operation. DSP algorithms generally have lots of extended sums-of-products operations. The extended dynamic range protects against overflow and loss of data or range.

In extended sum-of-products calculations, two operands are always needed to feed the calculation. Consequently, single-cycle fetch of two operands, from either on or off the chip, is the third requirement. A digital-signal processor must sustain two-operand data throughput.

Many DSP algorithms, including filters, use circular buffers. The fourth requirement, then, is on-and-off-chip hardware circular buffering. Hardware that handles address-pointer wrap-around reduces overhead and simplifies algorithm implementation.

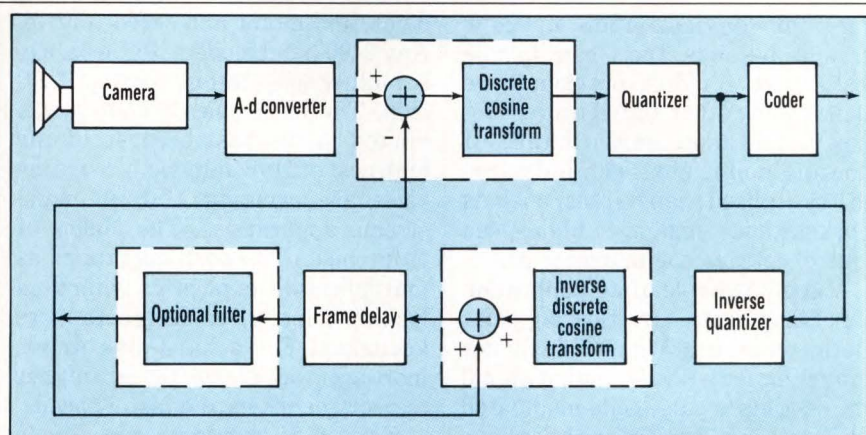
The last requirement is zero-overhead looping and branching. DSP algorithms are repetitive in nature and can easily be expressed in loops. Program sequencing that supports looped code with zero overhead simplifies programming and delivers top performance. Furthermore, overhead penalties for conditional program overflow are unacceptable in real-time oriented DSP algorithms.

thing is implemented in software, because there's no worry of the dynamic range running out. Software development is much easier for floating-point chips because designers can just concern themselves with the algorithm and not the nature of the data.

On the other hand, floating-point is generally more complex and slower, which is something designers must consider when performance is crucial. In building-block systems, floating-point capability can be added just to certain portions of the design with a barrel shifter. That implementation isn't even conventional floating point—just an intelligent scaling.

United Technologies Microelectronics Center Inc. (UTMC) makes an extremely fast, IEEE floating-point DSP chip that's designed as a system building block. Tim Hornback, applications engineer for UTMC's military standard products, says that the chip's main use will be in military applications. Its principal function in these applications will be radar, which requires very fast Fourier transform operation.

According to Hornback, the UTMC chip was built for floating-



1. A MOVING-PICTURE COMPRESSION SYSTEM needs the discrete-cosine transform and inverse discrete-cosine transform operations to perform image compression and decompression, respectively. Inmos Corp.'s IMS A121 chip is optimized for that function. The dashed-line boxes indicate the functions performed by the chip.

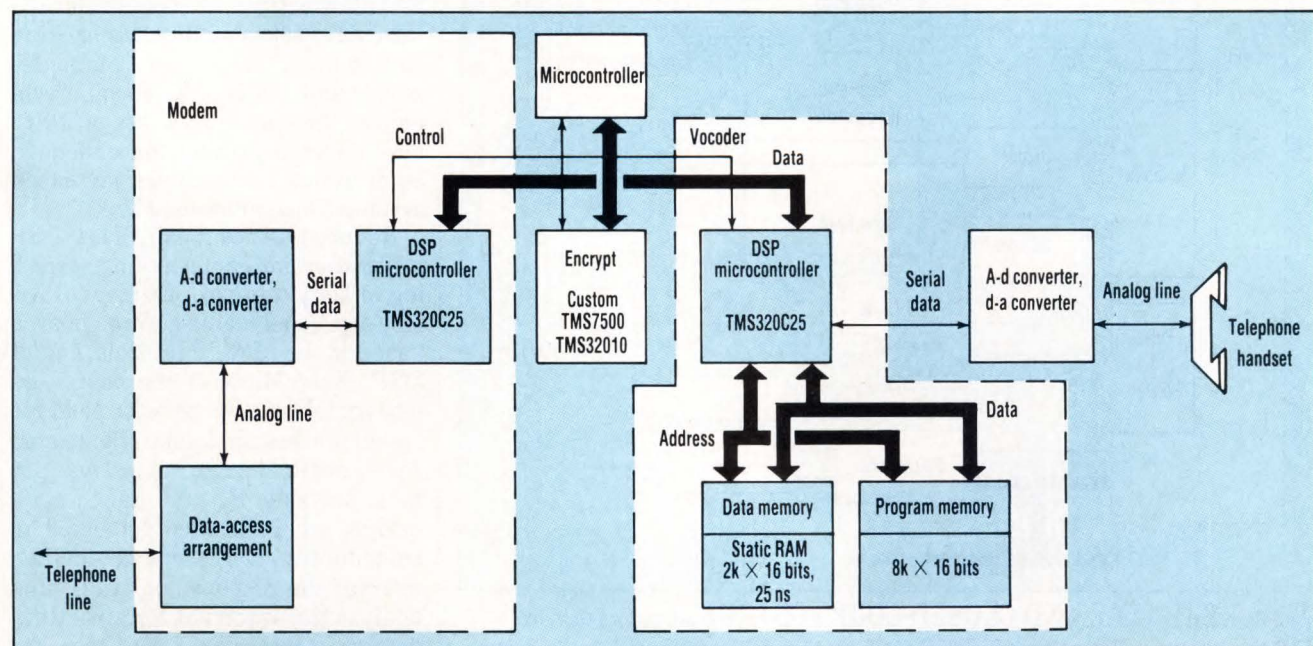
point math because of the wide dynamic range floating-point math offers. Larger fast Fourier transforms and filters are performed with floating-point math. "For 1-kpoint or smaller fast Fourier transforms, fixed-point math is okay," says Hornback. "For 1-kpoint or larger, designers need IEEE 32-bit floating point math."

What types of applications are the single-chip DSP devices used in? "In theory, the concept of DSP should

pervade all applications," says Gene Frantz, DSP applications manager at Texas Instruments. "The approach to any particular application is to process the signal in either the analog domain or digital domain."

APPLICATIONS, APPLICATIONS

DSP is becoming a cost-effective solution to more proven applications as the price of the single-chip devices goes down. At the other end of the spectrum, higher-priced, fast float-



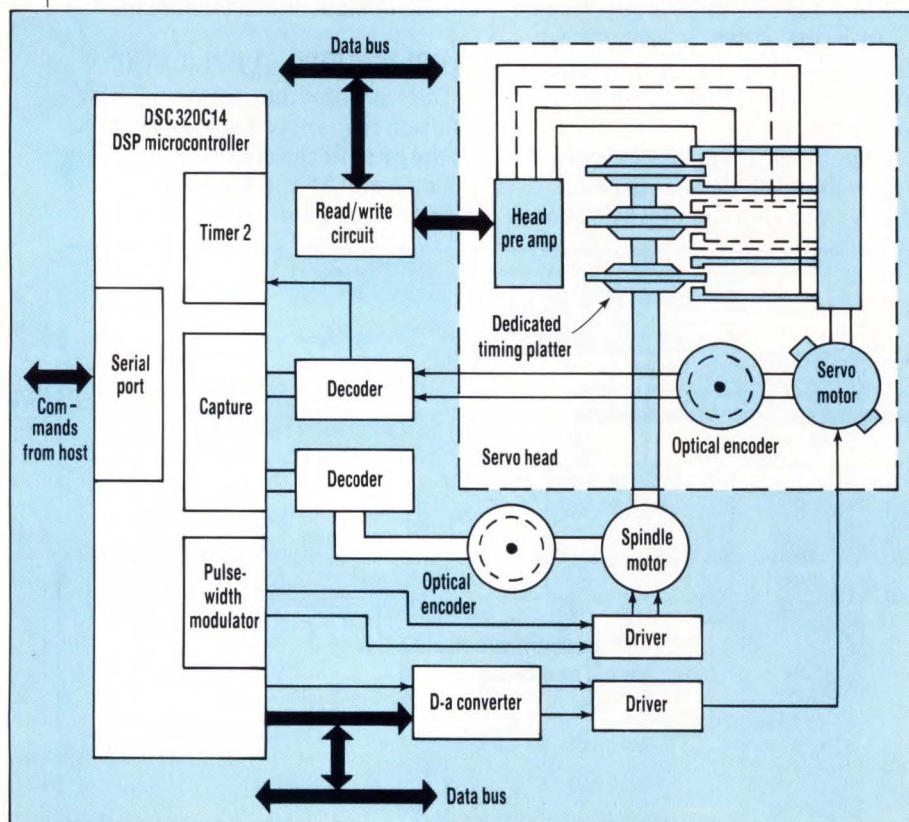
2. IN THIS SECURE TELEPHONY SYSTEM, speech signals are digitized and compressed to a low-bit rate before being encrypted and transmitted over the standard switched network. The vocoder converts the voice signal from the telephone handset into digital form, and its DSP chip reduces the 64-kbit/s data rate into a 2.4-kbit/s data rate.

Application areas for lower-cost general-purpose chips include mo-

Fujitsu Microelectronics Inc.'s strategy, according to Paul McGuire, DSP product marketing manager, and Bobby Saffari, DSP applications engineer, is to develop core digital-signal processors with a bevy of peripheral functions to give designers maximum flexibility. The new generation of processors is becoming highly integrated, and it's attacking areas typically covered by

"There are both general-purpose and application-specific devices," says McGuire. "General-purpose chips will survive many designers. But for certain designers, the general-purpose part falls short in some aspect of performance. They require a custom part." These applications vary from cost-sensitive applications that don't need some of the more powerful digital-signal processor features to the applications that need to increase some performance feature of the chip.

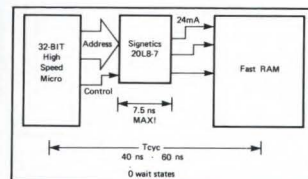
Reduced cost can really boost DSP infiltration into applications according to Tony Agnello, president of Ariel Corp. Ariel manufactures boards based on the AT&T, Motorola, and TI DSP chips. Many of the boards go into portable computers for portable signal processing. In one application, for example, the Ariel board was put in a portable PC and taken to a bridge, where it was connected to transducers. Engineers could then monitor the response of bridge and analyze the spectrum for structural defects—testing is a big area for DSP boards. In another example, a potato-chip manufacturer tests its product for freshness by crunching

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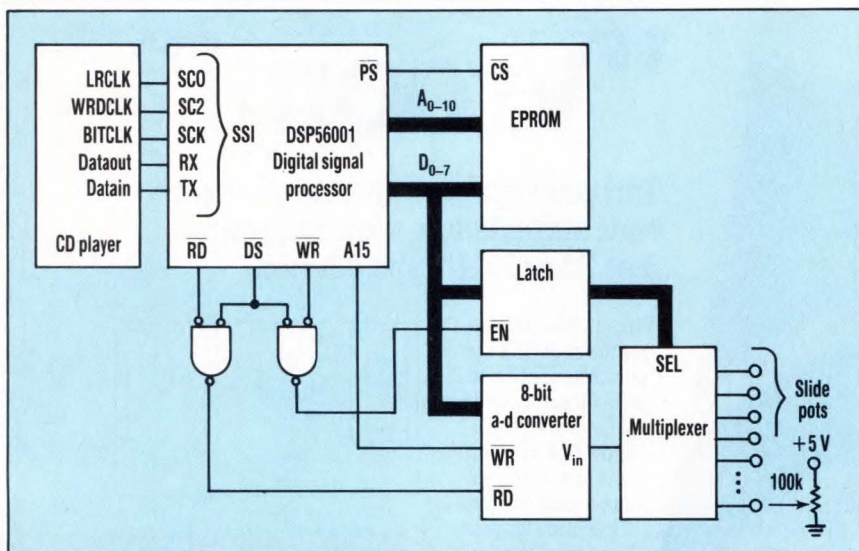
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DIGITAL-SIGNAL PROCESSING



4. MOTOROLA'S 24-BIT DSP CHIP is finding its way into many audio applications. This digital-stereo 10-band graphic equalizer uses the DSP chip to perform the infinite-impulse response algorithm needed for a bandpass filter.

chips and then analyzing its noise spectrum.

"DSP is useful in any real-time type application," says Garth Hillman, Motorola's strategic DSP applications manager. Hillman notes that DSP first found applications in the communications and telecommunications areas before spreading to communications-based systems, such as modems, audio, video, and image processing.

The newest application areas are on motherboards of workstations and PCs for signal processing of sound and audio, voice communications, and graphics. DSP chips can also work in conventional and fax modems. Currently, all computer manufacturers are searching for ways to incorporate DSP chips into their computers.

FIXED VS. FLOATING

Both fixed-point and floating-point math are available on single-chip digital-signal processors. Both types go into many of the same applications, with the fixed-point chips serving one area and the floating-point chips another.

In general, given the same speed performance, a fixed-point device will always be less expensive. Designers begin to make the decision point from a trade-off of accuracy

versus cost. "This trade-off is also a matter of religion," says Frantz of Texas Instruments. "There are fanatics who will only use floating point because they say fixed point will give a wrong answer. Conversely, there are those who say the only people who use floating point are lazy people who don't know how to scale and do a good design."

All of TI's fixed-point devices are 16 bits and the floating-point chips are 32 bits, so designers are actually making two trade-offs when going from one to the other: accuracy and dynamic range. Floating point has a much higher dynamic range.

Fixed-point chips are less expensive and consume less power, consequently they're often used for consumer applications. Jim Flynn, technical product support engineer for AT&T Microelectronics, says that digital cellular radio is a very hot area for fixed-point devices and it's quickly catching on in Europe. The U.S., however, still uses analog cellular radio.

Some argue that floating-point chips are slower than their fixed-point counterparts. In general, going from a 16-bit to a 32-bit chip slows down performance because there's a bigger data word, and it takes longer to multiply. Either performance or cost will have to be given up for float-

ing point.

Floating-point chips are larger and more expensive. Garth Hillman of Motorola Inc. explains that "floating point will take a while to catch on because the chips are so large. They need to get shrunk by better processes that will bring them down into the submicron level."

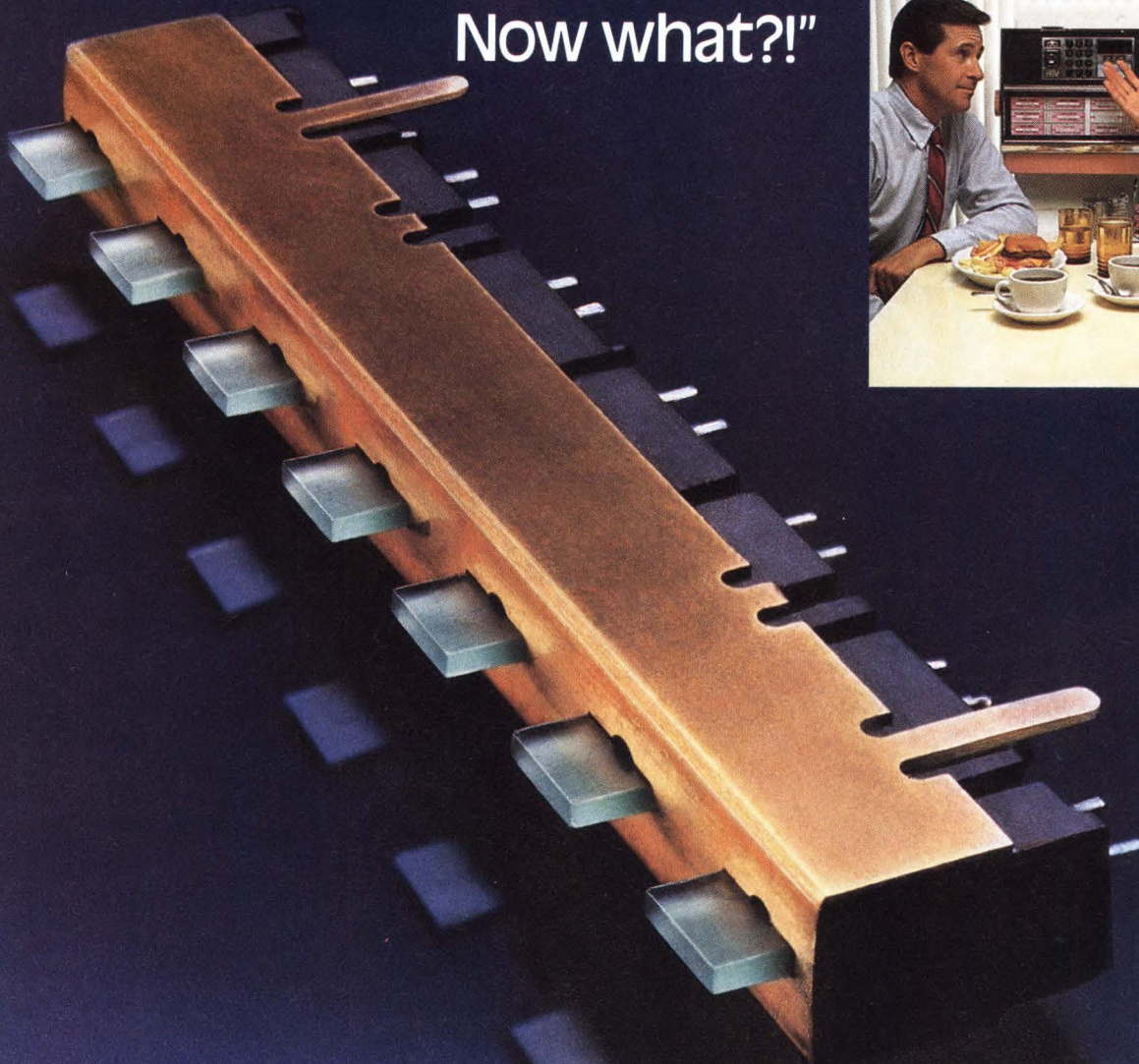
Steve Paavola, director of product management for Sky Computers Inc., notes that "fixed-point chips have an advantage in price; floating-point chips have the advantage of not worrying about scaling. With fixed point, designers implement the signal-processing algorithms and if they're not careful, they can end up losing bits of precision in places where it's unaffordable." With floating-point chips, there's no need to worry about losing bits and there isn't so much money spent on software development. The down side is that floating-point chips are more expensive. They also require more expensive memories because they're twice as wide. Low-volume applications use floating point because companies can't spend lots of money on software development.

MATRIX MATH

Many application involving matrix arithmetic need the dynamic range of floating-point chips, says Dr. Eldon of TRW. Many of the linear algebra functions that are performed on a matrix depend on the chip being able to determine if a number is exactly zero or just near zero. Floating point has a large dynamic range and can represent small numbers very accurately. With fixed point, as soon as a variable becomes lower than one, the number looks like zero. Accuracy is lost as the number gets smaller, and the entire matrix algorithm is thrown off. Many DSP applications rely on matrix operations.

One application that benefits from floating-point math is speech recognition. It needs the extra floating-point accuracy to distinguish among human voices. Human voices are a tough signal to analyze, especially when dialects and other variables are taken into account. The application also needs the sophisticated al-

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Consider this a guide rather than a definitive list.

gorithms and processing power that come with floating point.

Single-chip DSP devices have a broad range of data-word lengths: 8-, 16-, and 24-bit chips are available, as well as 32-bit floating-point chips. Where is the line drawn concerning word length and applications? Many times, application areas vary in complexity. Consequently, devices ranging from 8 to 32 bits may be used.

Motorola manufactures a 24-bit chip that has 144 dB of dynamic range, and according to the company, that's enough for just about any natural phenomenon on earth (*Fig. 4*). Any application requiring more dynamic range (which would require floating point) usually deals with synthetic objects. Graphics, image processing, and simulations are all computer generated, rather than sampled from nature.

Though digital-signal processing is fairly new, it holds much promise

for the future. Gene Frantz states that "there's lots of opportunity in DSP. Many areas are still untouched. As performance goes up and cost comes down, creative engineers will have more and more opportunities to apply this science to their problems to make a breakthrough."

The future for DSP will include a push for higher speed. Future speed increases will come from many sources, such as better architectures, customization, and better process technologies.

Higher integration of future DSP chips will bring many peripherals on board. DSP chips will become more tailored toward certain applications, resulting in single-chip solutions with better performance. Increased integration will bring more interfaces on the chip, making it easier to design into systems.

The higher integration makes the

digital-signal processor more and more like microprocessors. The devices have assemblers, linkers, simulators, and high-level languages. The two market areas will overlap in the future.

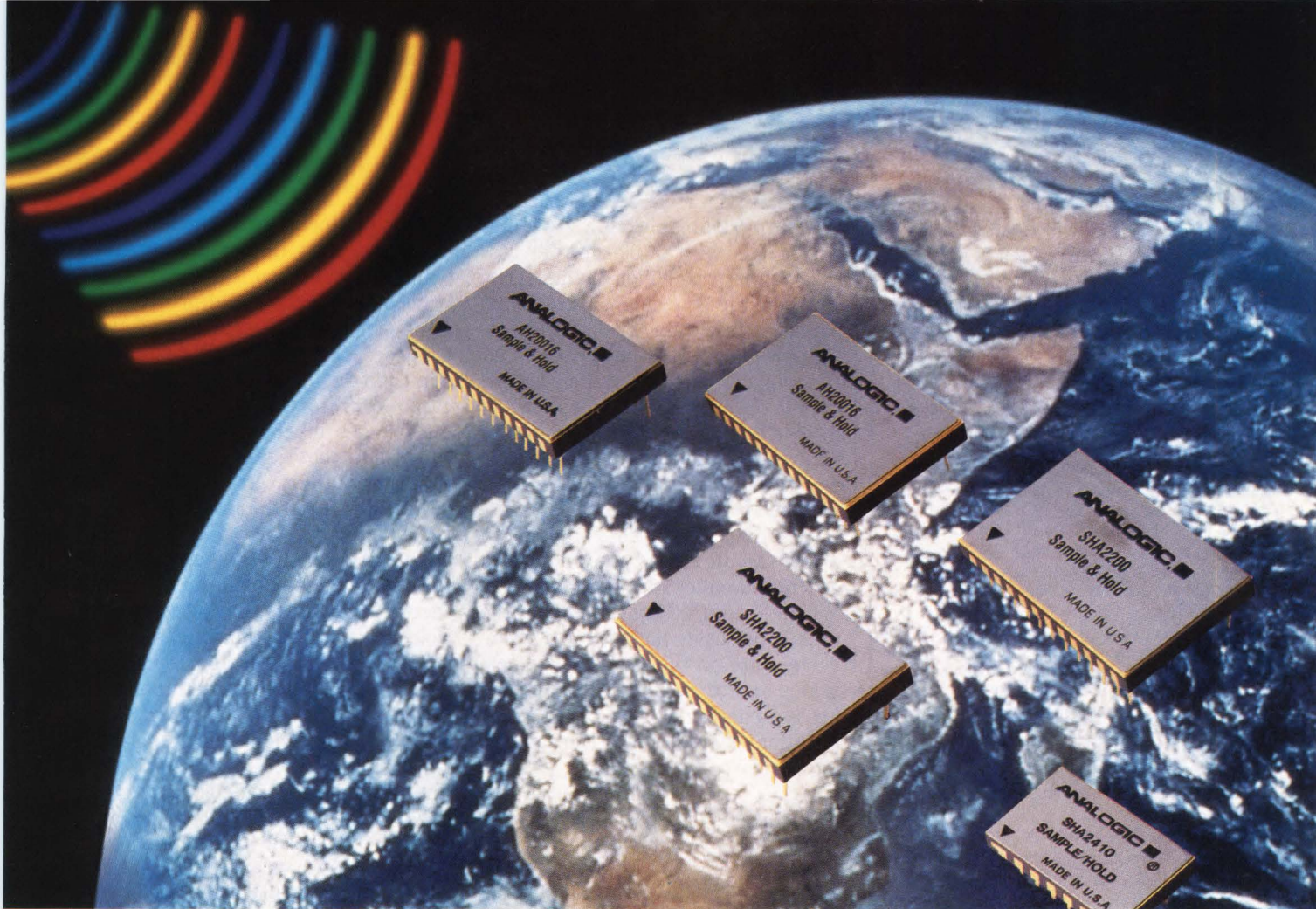
Steve Paavola of Sky Computers remarks that the functionality of 32-bit floating-point DSP chips and the new RISC chips is coming closer together. For a given performance, the DSP chips are still somewhat less expensive than the RISC chips. But the difference is decreasing, especially when all of the memory and peripherals needed by the DSP chips is factored in. DSP chips are already taking on more CPU functionality. They were always very RISC-like because of their speed and limited instruction sets, and manufacturers have been enhancing the instruction set to make it more complete.

In the future, the development tools will be just as important as the devices themselves. Designers could generate gate-level designs from algorithms. Future devices will begin to have multiprocessing—multiple multipliers-accumulators on one device. In addition, as VLSI technology improves, devices will have designated areas that will implement specific algorithms in hardware.

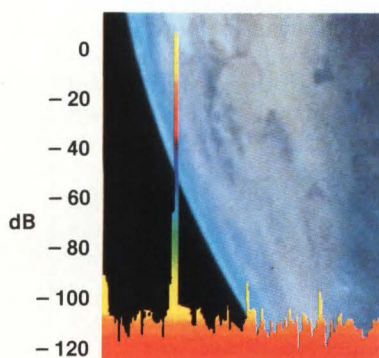
Future DSP devices will feature multiprocessing, with several math units working in parallel. Signal processors are really pushing memory technology to its limits right now, and one way to increase speed without pushing memory technology would be multiple processing. Process technology will fuel these changes.

Change may come in the form of a smaller data word. For instance, the drive for HDTV is going to create a demand for higher-performance DSP devices. Yet the higher performance will come with an 8-bit word and not a 32-bit word, because HDTV will need only 8 bits to operate.

HDTV will be a large application for DSP devices. The video for HDTV will be done with function-specific, video-digital-signal processors and not general-purpose chips. HDTV has very specific tasks that aren't programmable and don't need



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to be programmable. But the sound will be done with single-chip devices.

Though the inclusion of analog circuitry on the DSP chip will create capabilities, it will also bring problems. One problem is the device's limited functionality once the analog circuitry is on the chip. Each application has its own analog requirements. For instance, the television market needs 8-bit analog-to-digital conversion with 20-MHz sample rates. Telecommunications may need 8 bits and an 8-kHz sample rate. Audio requires a 48-kHz sample rate and 16 bits. Which should designers put on the processor? Once the d-a and a-d converters are on the chip, the application is specified. Current DSP chips are used across a broad range of applications by offering different analog parts.

ANALOG INTEGRATION

Another problem is the integration of the two circuit types on the same chip. The analog-conversion area gives off a lot of noise, which is extremely harmful to digital circuit performance—especially in the more accurate devices. Incompatibilities in process technologies will also arise. An analog process in the wafer fabrication is slightly different than the digital process.

In the 1990s, digital-signal processors will be widely offered as a core technology. Customers will build their own DSP chips based on a common core and standard and custom peripheral chips. The peripherals offered will be similar to those offered on microcontrollers, only more sophisticated. The signal processor has a real-time nature, so it needs higher throughput than a microcontroller.

The biggest difference in DSP and microcontroller peripherals is in the a-d converters. When microcontrollers have on-chip converters, they're generally 6 or 8 bits and they lack sophistication. DSP chips are more demanding: An audio signal processor, for example, samples at up to 50 kHz with 15 or 16 bits of accuracy. The converters are a challenge, but they will evolve.

Concerning applications, Brian Barrera, western region field appli-

cations engineer for Comdisco Systems Inc., says DSP will take over many traditional analog areas. This is because digital-signal processing is much more stable than analog-signal processing. With DSP, designers don't have to play around trimming capacitors to adjust the performance. It's much easier to design something that's going to work the first time without having to tweak it.

In the future, the integrated services digital network (ISDN) will devour the chips. ISDN is a standard for a common telephone digital interface to computers and peripherals. Voice mail is already an extensive application for DSP—it's currently being done, but it's not part of the computer yet. With ISDN, the computer will have a telephone line going into the back of it to receive or send faxes and voice mail. It will also contain a speaker and a microphone. Computers of the 1990s will have a computer-voice interface—users will speak to the computer, which will recognize voices and commands. In addition, phone-answering machines will scan messages for designated words.

Software will be more important in the future. Joel Dedrick of Logic Devices says that DSP is the last area that's mostly software-independent. "The idea 10 years ago was that DSP was a data-independent operation," he says. "Data was just filtered and that was it. Now, that's changing." He explains that systems need to find out if there's any useful information in that data, and then must do something that depends on that information.

For example, in the military, radar once had a blip on the screen to indicate the presence of an object. Now, radar must decide what the blip is and what it's doing. These decisions are implemented in software. The challenge for future DSP designers is to combine lots of software with these systems and not degrade performance. □

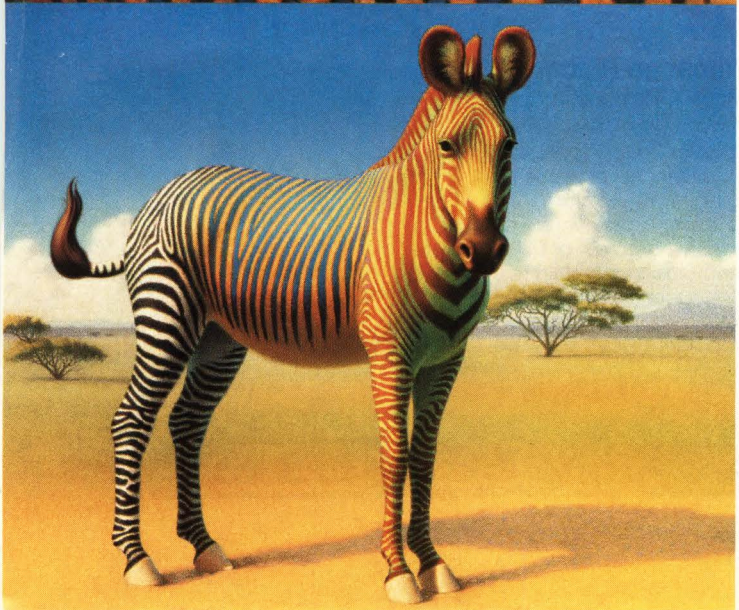
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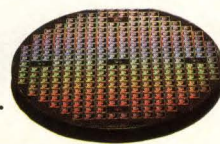
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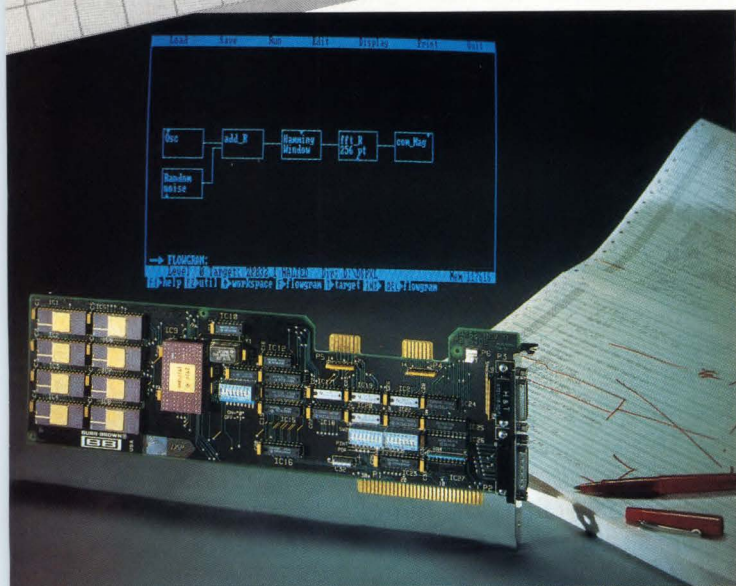
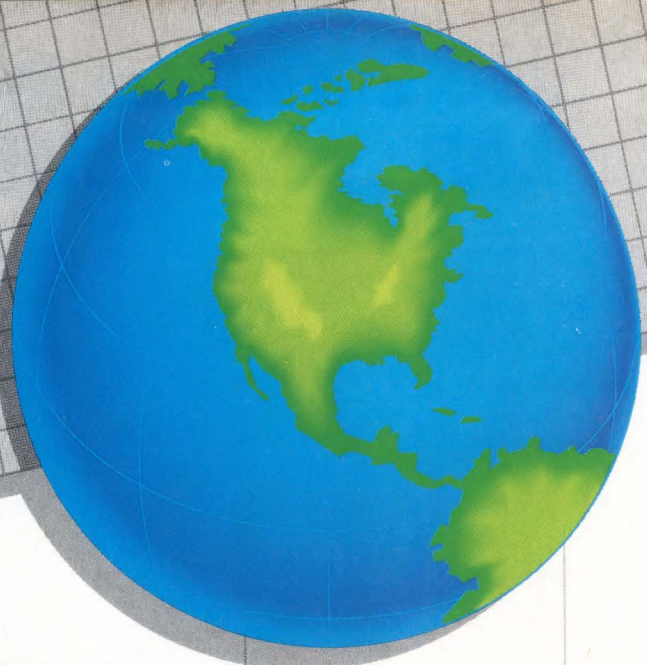
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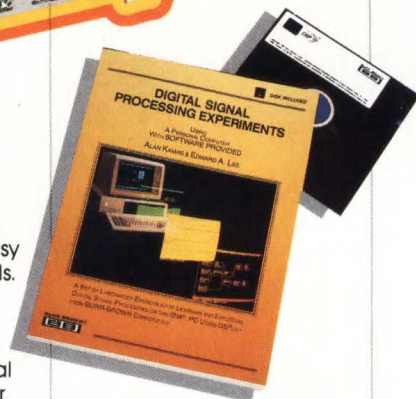
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The high computational power and speed of today's 32-bit microprocessors, such as the 68020, create interfacing complexities. Accordingly, most of their applications require heavy external support circuitry and very careful analysis of the signal timing, particularly of the interface between the microprocessor and its main dynamic RAM (DRAM) storage array. The burden of support-circuitry consisting of conventional MSI/LSI logic would tie up a large amount of board space. Moreover, poor interface timing can drastically reduce the microprocessor's performance.

The programmable features and flexible configuration modes of a special single-chip VLSI high-performance DRAM controller (DRC), however, can simplify interfacing, reduce design time, and offer proper timing and control. An example of this approach is a 68020-based application (*Fig. 1*).

In this application, the DRC provides a general-purpose 20-MHz CPU board which is capable of real-time I/O control and able to display status on an on-board liquid-crystal display (LCD). In addition to the DRC and the 68020, the design includes Samsung's CMOS PLDs (CPL), AHCT logic devices, EEPROMs, static RAMs (SRAMs), DRAMs, and linear ICs. Instructions reside in 32 kbytes of EEPROM and data occupies 32 kbytes of SRAM plus an 8-Mbyte DRAM array. The CPL devices supply address decoding, LCD control signals, and general interfacing functions. The DRC used in this design is the KS84C21. Since the application is straight forward, only the basic feature set is used in a noninterleaved memory-access mode.

VERSATILE INTERFACING

The KS84C21 offers single-chip DRAM interfacing between virtually any microprocessor or system bus and 256-kbyte and 1-Mbyte DRAMs. The companion KS84C22 can support 256-kbyte, 1-Mbyte, and 4-Mbyte DRAMs. Both DACs have a 380-pF drive capability, which is sufficient to drive memory arrays of up to 70 DRAMs.

Major features that suit these DRCs for systems employing the 68020 include: a choice of interleaved or non-interleaved and burst or nonburst memory accessing, synchronous or asynchronous operation, error scrubbing during refresh for systems with error correction and detection, and support for all of the advanced addressing modes—page, nibble, and static column.

The devices are available as user- and mask-programmable types. The user-programmable version is useful for prototyping and low-to-medium volume applications, but it may require some external logic for programming, depending on the design. Consequently, designers must make some provision to control the programming pins during initialization. For instance, designs that incorporate the user-programmable version require reprogramming after power-on reset. For this purpose, the DRC receives programming inputs on the R_{0-9} , C_{0-9} , B_0 and B_1 inputs. The programming bits are loaded into the Mode

DESIGN APPLICATIONS

68020 DRAM INTERFACING

Register when Mode Load (\overline{ML}) goes low or as the result of a "dummy" access (Fig. 2).

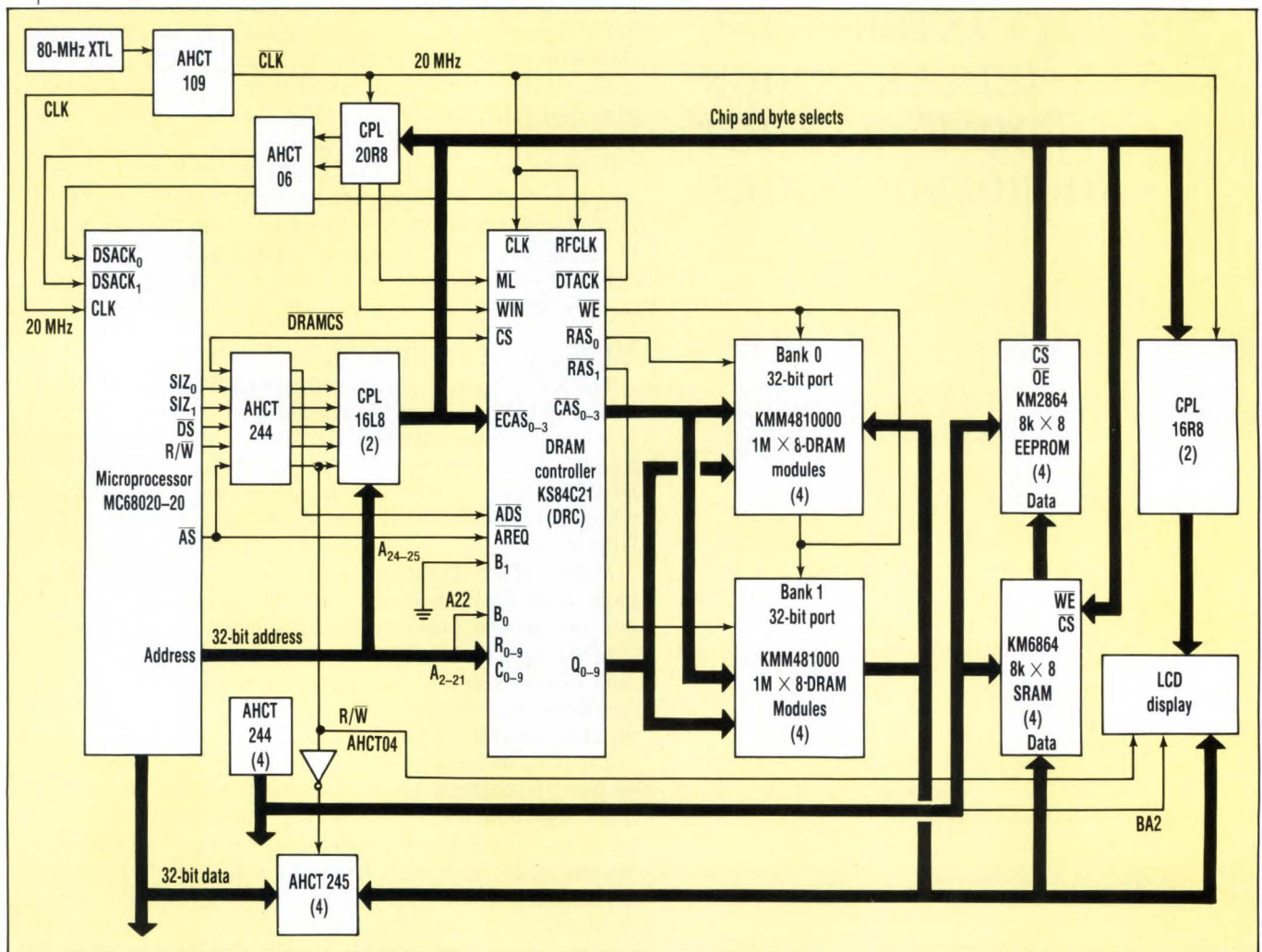
However, although external decode logic in the circuit of this 68020 application generates the \overline{ML} input, the KS84C21 actually used in the application is mask-programmed, so neither the B_1 nor \overline{ECAS}_0 input pins need provisions for programming. The mask-programmed version is for finalized designs with medium-to-large production needs. Before production of the mask-programmed parts begins, the customer receives 10 laser-programmed parts to verify in-circuit performance. Of course, the mask-programmed version offers superior reliability and a lower system parts count.

The 68020 supplies several control signals and interfaces to the display system through separate 32-bit address and data buses. Four AHCT245 transceivers buffer the data bus, four AHCT244s buffer the address bus, and one AHCT244 buffers the control signals. Two 25-ns CPL16L8 CMOS PLDs generate Address-Decoding and Chip-Select signals from the 68020's control signals.

Timing considerations dictate that the KS84C21 DRC utilize a 20-MHz clock signal (\overline{CLK}), which is inverted from that going to the 68020. This achieves an effective half-cycle delay from the 68020's internal timing. The KS84C21's RFCLK input also comes from the \overline{CLK} signal, though it could use any clock signal avail-

able to the system that's a multiple of 2 MHz.

The system's memory array consists of two banks of 1-Mbyte words with a provision for byte accesses through the DRC's \overline{CAS}_{0-3} outputs— \overline{ECAS} input pins (not used in this application) could supply burst-access control, delivering the necessary CAS timing. To minimize delays and improve timing, the address inputs from the 68020 to the KS84C21 have no buffers. Address pins A_{21} through A_2 are connected to the DRC's row and column address input pins (C_{0-9} and R_{0-9}), while address line A_{22} supplies the B_0 bank-select signal for two 32-bit, 4-Mbyte DRAM banks. Because the system uses just two banks, Bank-Select signal B_1 is con-



1. IN THIS APPLICATION the KS84C21 DRAM controller provide a general purpose, 20 MHz 68020 based, CPU board which is capable of real-time I/O control and able to display status on an on-board liquid-crystal display. In addition to the DRAM controller and the 68020, the design includes CMOS PLDs (CPL), AHCT logic devices, EEPROMs, SRAMs, DRAMs, and linear ICs.

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nected to ground.

Bit B_0 controls the on-chip address latches. Because the 68020 holds the addresses stable for the entire access, either mode—latched or transparent—can be used. In this application, addresses latch on the falling edge of ADS.

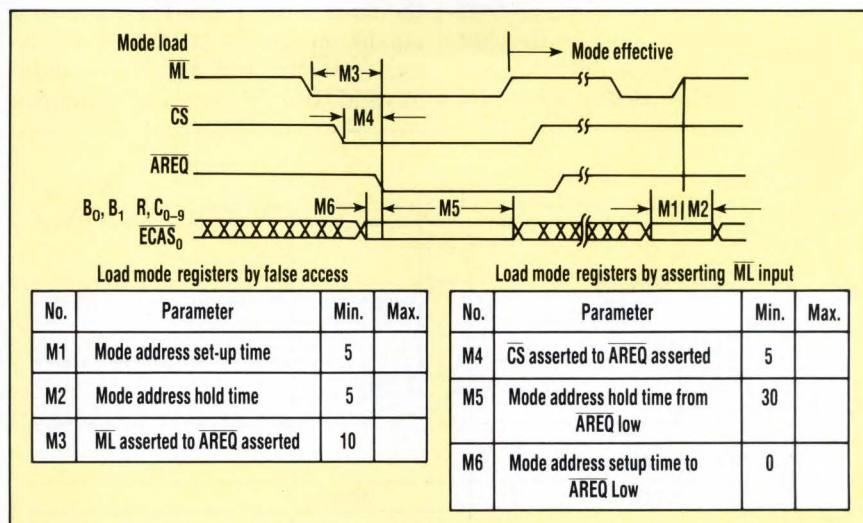
Bit B_1 controls the choice of either the synchronous or asynchronous access mode. The choice is system dependent and is based on timing considerations: In the synchronous mode, the access begins on the rising edge of the first clock after ALE goes high. In asynchronous mode, access begins at the falling edge of ADS. The mode is usually chosen so the access can start as early as possible in the CPU's access cycle to minimize the number of wait states. In this case, asynchronous access gives the best timing.

Address bits A_{23} and A_{26} remain available for future memory expansion: A_{23} as a Bank-Select and A_{26} as a Chip-Select signal.

The Chip-Select (\overline{CS}) pin of the DRC connects to the decoded \overline{DRAMCS} line, which is derived from address pins A_{24-25} , and the 68020's Address Strobe (\overline{AS}). The \overline{CS} input must be low for an access to occur, and it must meet a setup time, either t_{01} or t_{12} , and a hold time t_{010} for proper operation. The \overline{AS} signal meets all of these requirements (Fig. 3).

The 68020's \overline{AS} also supplies the proper timing for the asynchronous ADS input with a buffered \overline{DRAMCS} signal. This buffering is necessary to meet the t_{12} requirement for the \overline{CS} to ADS setup time. The falling edge of ADS latches the row, column, and bank addresses, and starts the access. While \overline{ADS} is high, the on-chip latches are transparent.

The DRC input signal \overline{AREQ} also uses the \overline{AS} strobe for its timing. The \overline{ADS} signal initiates an access; \overline{AREQ} sustains and ends the access. Because \overline{AS} signals the end of an access in a 68020, it's an ideal source for the \overline{AREQ} input. The end of an access brings RAS and CAS high in the interleaved mode. In the noninterleaved mode, the end of an access brings only RAS high. If it's pro-



2. DESIGNS THAT INCORPORATE THE USER-programmable version of the DRAM controller require reprogramming after power-on reset. For this purpose, the DRC receives programming inputs on the R_{0-9} , C_{0-9} , B_0 , B_1 and \overline{ECAS}_0 inputs. The programming bits load into the Mode Register when the ML signal goes low or as the result of a "dummy" access.

grammed, \overline{AREQ} can also bring \overline{CAS} high.

The main objective for a write is to ensure that the 68020's data is available to the DRAM at the proper time. For the write access in the figure, the delay caused by the \overline{RAS} precharge time ensures that the data will be valid for the DRAM well before it's needed. Because all of the writes are early writes, the data must be valid on the falling edge of \overline{CAS} .

REFRESH CYCLE

In the refresh cycle, the only important parameter is the number of clock cycles programmed for \overline{RAS} low during refresh. But in the KS84C21, that's tied to the programmed \overline{RAS} precharge time. Picking the proper \overline{RAS} precharge time will virtually ensure the proper \overline{RAS} low during the refresh period. The only choice for \overline{RAS} low is between 2T and 3T for \overline{RAS} low if the \overline{RAS} precharge time chosen is 2T.

The 68020's R/W signal supplies the DRC's Write-Enable (\overline{WIN}) input, which controls the DRC's Write-Enable (\overline{WE}) output. \overline{WIN} also enables a delayed CAS feature in support of an "early write" function.

The DRC's four \overline{ECAS} inputs enable the four output CAS output signals, which primarily control byte ac-

cess. They also control the access during burst-mode operation. Furthermore, the \overline{ECAS} signals in special situations can delay \overline{CAS} from going low as long as needed. The only inputs to the 68020 from the KS84C21 are data-transfer and size-acknowledge pins \overline{DSACK}_{0-1} . These inputs signal the size of the DRC's data port and are also the means for inserting wait states into the 68020's access-cycle timing.

If the KS84C21's input to the \overline{DSACK} pins was the only such input in the system, and if the DRC used a 32-bit port, the hookup would be simply to run the DRC's \overline{DTACK} output to both \overline{DSACK} inputs. For an 8-bit port, \overline{DTACK} would connect only to \overline{DSACK}_0 ; for a 16-bit port, \overline{DSACK}_1 would be the lone connection. However, this never occurs in a practical system. The \overline{DTACK} signal must logically combine with the signals from the rest of the system. In this application, CPL device, simply AND signals from the EEPROM, SRAM, and LCD display with \overline{DTACK} , create the final \overline{DSACK} signals.

For read and write accesses, the major timing consideration is how long \overline{DTACK} must be delayed from going low (asserted). For the read, input data is latched in the 68020's

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S4-S5 falling edge of CLK, so that edge must be delayed with wait states. Or if necessary, until the data is available at the 68020 and has met

the data setup time. There's also a maximum constraint that must be met on the \overline{DSACK} asserted to data-in valid time. These constraints can

be met by proper adjustment of \overline{DTACK} assertion with wait states. In this case, delaying assertion for an interval of $2T$ is sufficient.

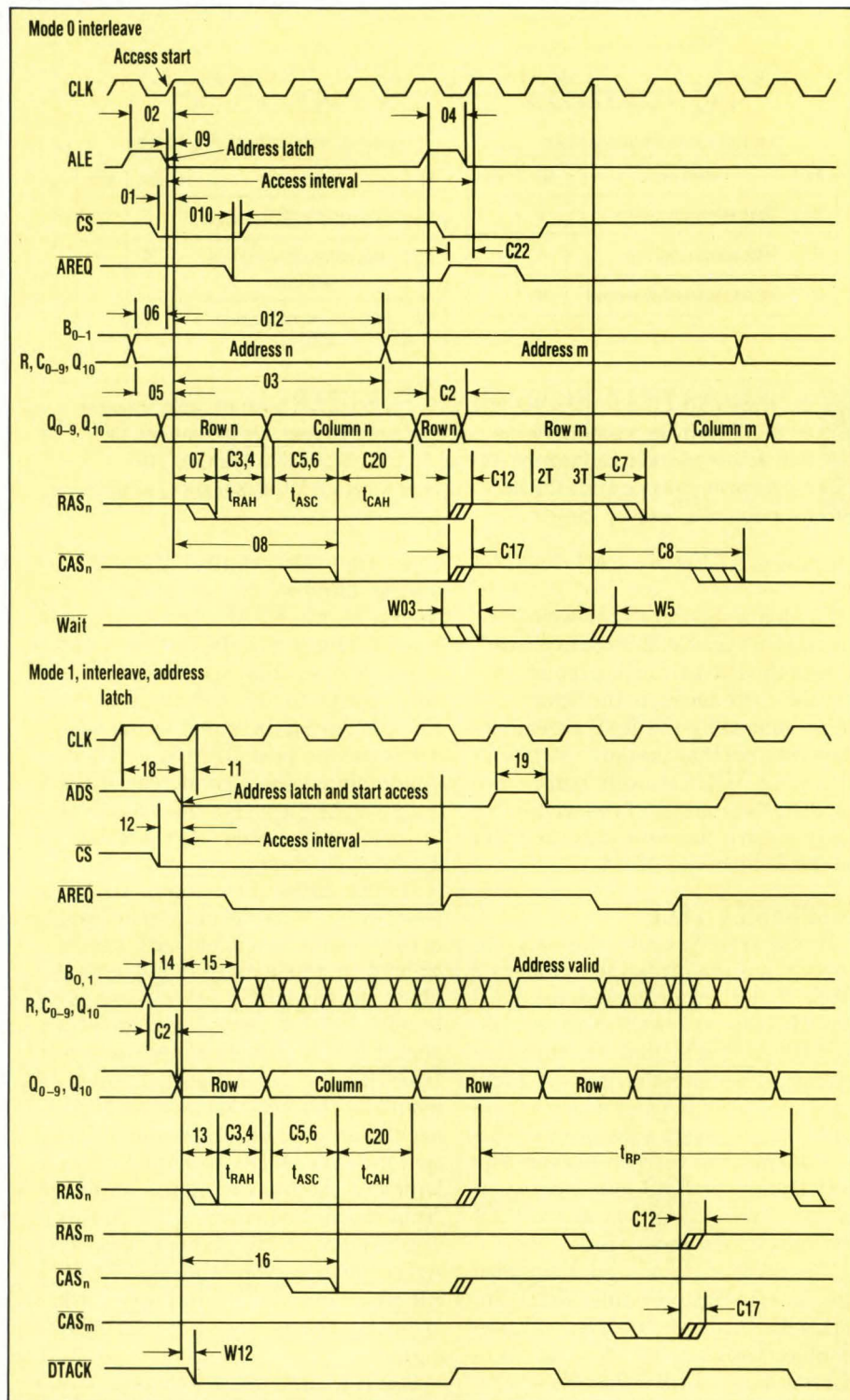
The DRC-to-RAM array interface is simple and straightforward. The multiplexed address outputs Q_{0-9} connect to two banks of four $1M \times 8$ -bit DRAM modules—each through internal series resistors that control ground bounce and over- and under-shoot problems. Because the system contains just two of these memory banks, RAS_0 and RAS_1 are the only RAS lines used—one for each bank. Each CAS output controls one byte in each bank, and the \overline{WE} signal connects to all DRAMs.

The refresh-in-progress output (\overline{RFIP}) goes low one clock period before RAS goes low; it goes high with the rising edge of the CLK that ends the refresh operation. In this system, \overline{RFIP} and input pins \overline{RFSH} , $\overline{DISRFSH}$, and $\overline{COLINC/EXTDRF}$ (which tied to V_C) are unused. \overline{RFSH} and $\overline{DISRFSH}$ serve external refresh requests, and $\overline{COLINC/EXTDRF}$ increments the latched column address during such page operations as writing a frame buffer, or extending the refresh period for a read-modify-write cycle during error scrubbing.

Because this application is noninterleaved, the system uses the multiplexed \overline{WE} of the DRC instead of its \overline{RFRQ} output. The maximum loading on the \overline{WE} output is 500 pF, sufficient to drive 2 banks of memory. An application with more than two or four banks of memory would need \overline{RFRQ} .

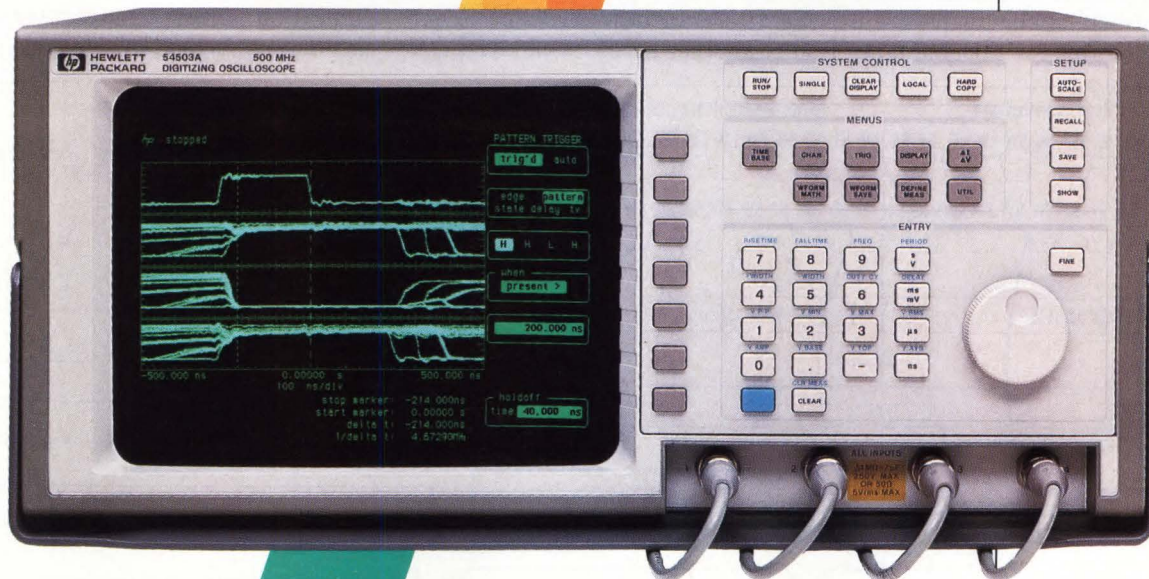
In the noninterleaved mode, the $\overline{ECAS_0}$ bit sets the way the circuit negates CAS outputs. With a zero loaded into the mode register, CAS can be negated in the same manner as the interleaved mode—with the rising edge of \overline{AREQ} . A one input, though, delays CAS negation until the first rising edge of CLK after RAS is negated. The $\overline{ECAS_0}$ bit also makes it possible to select the \overline{RFRQ} output in the noninterleaved mode.

With the noninterleaved mode, RAS can also start the precharging time early without adding wait states while still maintaining proper



3. FOR AN ACCESS TO OCCUR, the Chip-Select (\overline{CS}) pin input must be low. The falling edge of the \overline{ADS} signal latches the row, column, and bank addresses, and starts the access.

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CAS hold time. This ability is often very helpful in systems where consecutive accesses to the same bank occur frequently. It also makes sure that the DRAM output drivers (which CAS controls) aren't disabled before the CPU has time to latch the incoming data.

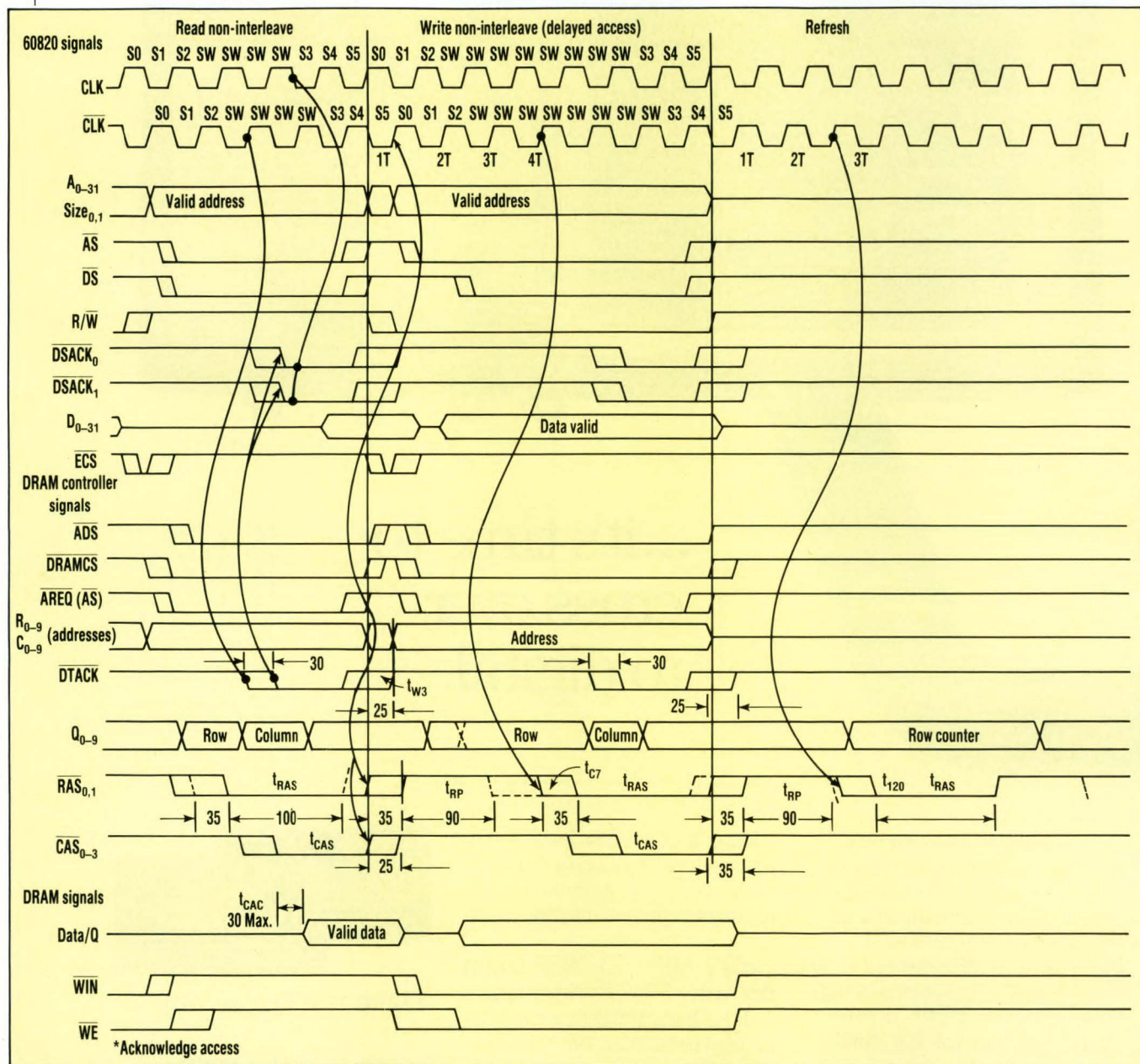
In the interleave mode, however, designers automatically select $\overline{\text{RFRQ}}$. For instance, it could serve to disable address pipelining before a refresh cycle. But for this example,

delaying the trailing edge of $\overline{\text{CAS}}$ is unnecessary because the circuit uses the $\overline{\text{WE}}$ output.

Pin R_8 puts the DRC in a noninterleaved or interleaved access mode. In the noninterleaved mode, the column addresses are held on the Q_{0-9} outputs until $\overline{\text{RAS}}$ goes high. For interleaving, the column address is held a minimum of 35 ns, then the next row address is multiplexed to the Q_{0-9} outputs. ALE/ADS can start another access while $\overline{\text{AREQ}}$ is

still low. As with noninterleaved access, $\overline{\text{AREQ}}$ going high ends the current access.

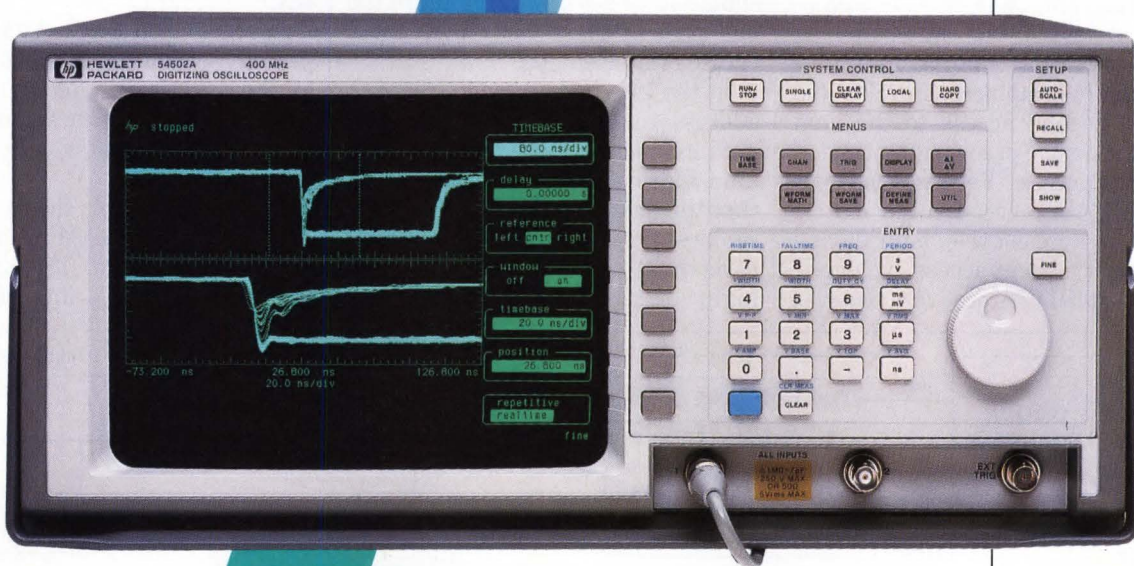
Though the application example supports burst accessing, which is useful in some situations, hooking the KS84C21 up for burst-accessing eliminates any memory interleaving—a method that offers a substantial decrease in memory-access cycle time. Four KS84C21 RAS/CAS configuration modes sustain interleaving and support various memory lay-



4. DESIGNERS MUST PAY SPECIAL ATTENTION

to the fact that the CLK signal times the 68020, while the $\overline{\text{CLK}}$ signal times the KS84C21.

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outs and $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ mixtures. In the design example, interleaving would occur by: exchanging address pins A2 and A22, selecting the interleaving mode with bit R₈, choosing an $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ configuration that supports interleaving, and changing the $\overline{\text{RAS}}$ lines to conform to that configuration. In addition, the $\overline{\text{RAS}}$ precharge timing would have to be reanalyzed.

OVERLAYING ACCESS CYCLES

The interleaving mode speeds memory-access time because the DRC can overlap access cycles and begin a second access to the next bank during the precharging time of the first access. Because the precharging time constitutes nearly half of an access cycle, interleaving can effectively cut access cycle time by almost 50%. Moreover, because

about 85% of memory accesses are sequential, this savings occurs 85% of the time.

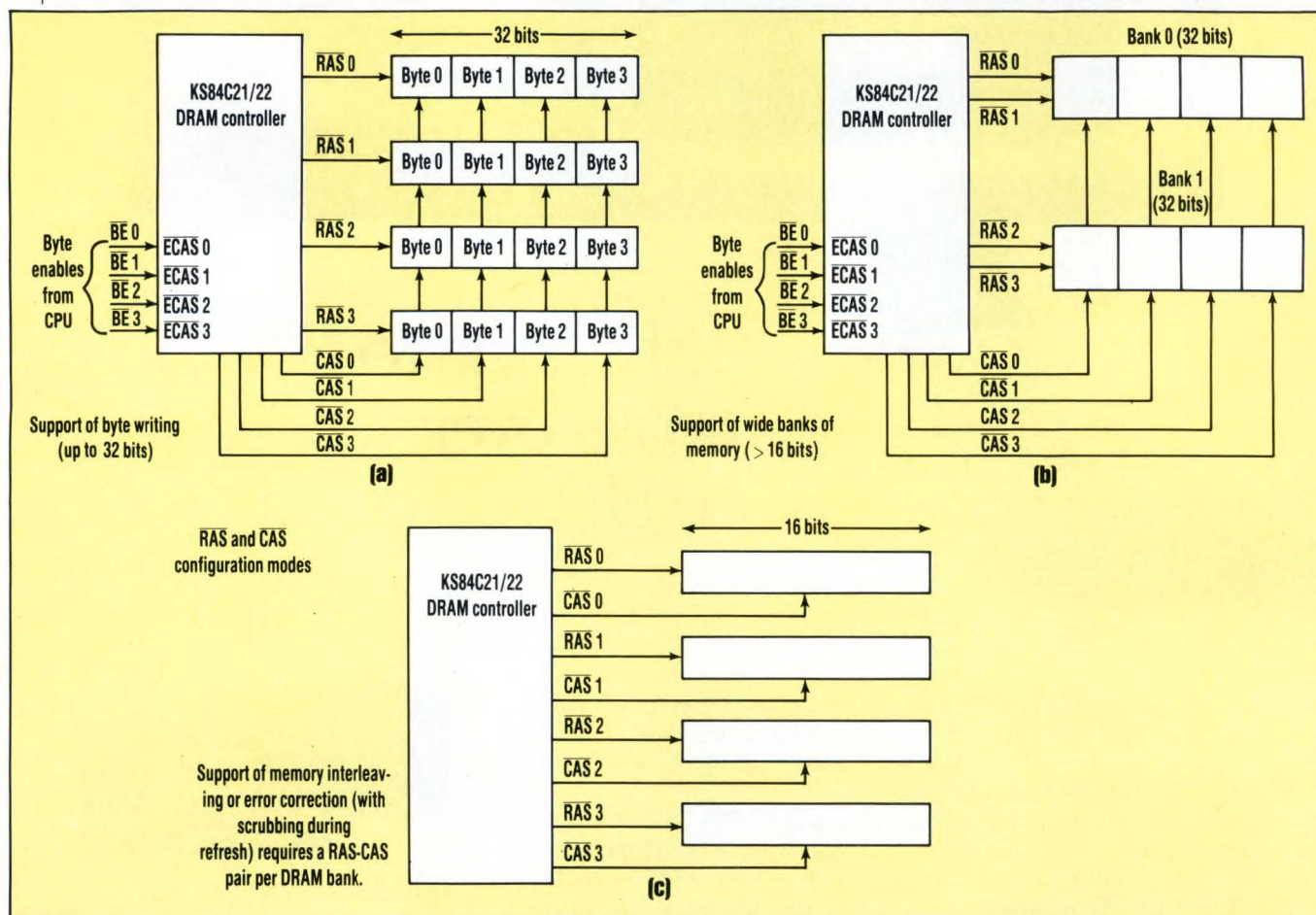
Although interleaving significantly improves system performance when the DRAMs match the speed of the CPU, interleaving is particularly advantageous with slower, less-expensive DRAMs used with high-speed CPUs. Nevertheless, the DRAMs for the 68020, which don't have pipelined address signals, should have a t_{RAS} time equal to the bus cycle of the 68020 for the most efficient interleaving.

In the interleaved mode, the row addresses are multiplexed to the outputs immediately following the column-address holding time t_{C20} so that the next access can begin. This replaces holding the column addresses on the Q₀₋₉ outputs until $\overline{\text{CAS}}$ goes high.

The refresh-arbitration logic inserts a refresh cycle between two interleaved accesses where needed. If an access is in progress, the logic holds the refresh until the access cycle is over. If consecutive accesses to the same bank occur, the KS84C21 inserts wait states to ensure that the DRAM precharges for a programmed number of clock cycles.

Inputs R₀ and R₁ control the $\overline{\text{RAS}}$ low time, and the circuit guarantees $\overline{\text{RAS}}$ precharge time by inserting wait states. But the low time is only guaranteed during refresh. During an access, the rising edge of $\overline{\text{AREQ}}$ controls $\overline{\text{RAS}}$ and the input clock's rising edge counts the occurrence of both times.

In this application, the chosen time of 3T meets the DRAM's required 90-ns precharge time. The timing requirement of the t_{C22} interval for rec-



5. COMBINED WITH BANK INPUTS B₀ and B₁, pins C₄-C₆ select the number of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs during an access. Each configuration groups the outputs so that each RAS and CAS will drive one-fourth of the memory, regardless of whether the array is arranged as 1 bank (a), 2 banks (b), or 4 banks (c).

ognition is $1T$ of the \overline{RAS} precharge time. The \overline{AREQ} high level to the CLK's rising edge can be as little as 15 ns, which is a good deal less than one clock cycle. This fact must be considered when choosing the number of clock cycles for \overline{RAS} precharging. Because each bank has its own precharge counter, the circuit will meet required precharge times (even during interleaving).

COMPLEX APPLICATIONS

Once familiarized with the features and programming of the KS84C21 in a simple application (and by extension the KS84C22), extrapolation into more complex applications is straightforward. Designers must realize that the CLK signal times the 68020, while the \overline{CLK} signal times the KS84C21 (Fig. 4). For the read and write accesses, the major timing consideration is how long to delay \overline{DTACK} from asserting (going low). For the read access, the consideration is that input data latches at the 68020's CLK S4-S5 falling edge; thus, wait states must delay that edge, if necessary. That delay must last until the data from the DRAM becomes available at the 68020 and meets the needed data setup time. Also, the timing must meet the constraint on the \overline{DSACK} 's allowed maximum asserted-to-data-valid time. Proper adjustment of the \overline{DTACK} 's assertion by means of wait states can meet both of these constraints.

Bit R_7 selects either a wait or an acknowledge output to send to the 68020. When the \overline{WAIT} signal goes low, it causes the processor to insert wait states until it goes high. The \overline{DTACK} acknowledge works the opposite way: As long as \overline{DTACK} stays high, the CPU inserts wait states. When \overline{DTACK} drops low, that serves as an acknowledgement of data transfer and the CPU can finish its access. In general, either signal can be used with any processor by adding external logic. In practice, either signal usually matches the CPU's desired input, and that one is chosen. For the 68020, the \overline{DTACK} signal connected directly to the \overline{DSACK} inputs, so that was the out-

put chosen.

System designers use bits R_2 and R_3 to ensure that \overline{RAS}_N is low for a time that's sufficient enough to meet the DRAM specifications. For non-burst-mode accesses, they select when \overline{WAIT} goes high (deasserted) or when \overline{DTACK} goes low (asserted) in relation to when \overline{RAS} is asserted. For the 68020, the S3 clock cycle can't begin until \overline{DTACK} goes low. The required delay time can be calculated based on the access time of the DRAMs. The system delays the data incurs on its way to or from the CPU. The application example uses a wait of $2T$. All of the logic in the KS84C21

AFTER MASTER- ING THE KS84C21'S BASIC FEAT- URES, DESIGNERS CAN TACKLE MORE COM- PLEX APPLICATIONS.

uses the input clock's rising edge as a reference, therefore a programmed wait of $1/2T$ \overline{DTACK} goes low on the first falling clock edge after \overline{RAS} goes low.

During burst-mode accesses, control moves from $\overline{ALE}/\overline{ADS}$ and \overline{AREQ} to the \overline{ECAS} inputs. The first access, which must be nonburst, would normally be terminated by \overline{AREQ} . Instead, it's terminated by the rising edge of \overline{ECAS}_N . \overline{ECAS} 's rising edge also takes \overline{WAIT} low or \overline{DTACK} high to begin the wait-state period, if any wait state is programmed.

The amount of \overline{CAS}_N precharge required time determines the time \overline{ECAS}_N remains high. The next access—the first burst access—begins on the falling edge of \overline{ECAS}_N . The mode bits R_4 and R_5 set the amount of time the wait state period contin-

ues beyond the fall of \overline{ECAS}_N .

For example, if R_4 and R_5 are programmed to ones (the 0T state) the $\overline{WAIT}(\overline{DTACK})$ output follows the up and down movement of \overline{ECAS}_N . The output adds no wait states of its own and makes it possible for the \overline{ECAS}_N edges to completely define the wait state period. If R_4 and R_5 are set to zero, as in the example application, $\overline{WAIT}(\overline{DTACK})$ remains deasserted from the previous access and doesn't assert on the rising edge of \overline{ECAS}_N . Though \overline{ECAS}_N controls the accesses in burst mode, \overline{AREQ} terminates the burst access mode by bringing \overline{RAS} high.

For this system, the DRC's \overline{WAITIN} pin goes to ground and mode bit R_6 , set to zero, adds one wait state to every access. With the \overline{WAITIN} input to the DRC, the number of programmed wait states for any access that requires more time than a typical access. If \overline{WAITIN} meets its setup time before assertion, the number of wait states (one or two) programmed by R_6 add to the upcoming access.

On the DRAM side, for either a read or write, the system must meet the row-address hold, column-address setup, and the \overline{RAS} and \overline{CAS} precharge times. Proper selection of the DRC's programming bits eliminates the first three time requirements. The \overline{ECAS} inputs, however, control the \overline{CAS} precharge time during burst access. Therefore, those inputs need external manipulation to meet that precharge time. Because this application doesn't support burst accesses, that control is unnecessary.

In the refresh cycle, the only important parameter is the number of clock cycles programmed for \overline{RAS} low during refresh. But in the KS84C21, that parameter depends on the programmed \overline{RAS} precharge time. Therefore, picking the proper \overline{RAS} precharge time virtually guarantees the proper \overline{RAS} low during a refresh period.

Mode bit R_9 determines whether the refresh operation is staggered or standard. For standard refresh, all \overline{RAS} outputs are asserted at the same time. The outputs stay low for



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the time programmed in bits R_0 and R_1 , and then deassert at the same time. In staggered refresh, the \overline{RAS} outputs go low in sequence. Each falling \overline{RAS} edge is separated from the previous one by one clock period.

Staggered refresh is used if peak switching current must be kept low. However, it does extend the refresh time. The DRC will use whatever refresh option is selected by R_9 for both internal and external refreshes. With automatic internal refresh, a refresh is performed once during each refresh clock period. Because peak switching currents weren't a problem with this design, standard refresh was chosen.

THE CLOCK DIVIDER

The mode bits C_0 , C_1 , and C_2 select the divider used on the RFCLK input signal to generate the internal refresh clock of approximately 2 MHz. The RFCLK input should be from 6 to 20 MHz and preferably a multiple of 2. Because the RFCLK input is 20 MHz; C_0 , C_1 , and C_2 are set to zero to select a divide by 10.

With the refresh clock at approximately 2 MHz, bit C_3 sets the divisor for the refresh cycle time—approximately every 15 or 13 μ s. This application uses a standard 15- μ s refresh period.

The mode bits C_4 , C_5 , C_6 , combined with the bank inputs B_0 and B_1 , select the number of \overline{RAS} and \overline{CAS} outputs during an access. Each configuration groups the outputs so that each \overline{RAS} and \overline{CAS} will drive one-fourth of the memory, regardless of whether the array is arranged as 1, 2, or 4 banks (Fig. 5). These bits also determine the support of error scrubbing, interleaving, or byte writing with a particular configuration. As an example, mode 0 brings all four \overline{RAS} outputs low during an access, and enables error scrubbing. The mode also selects all four \overline{CAS} outputs. Individual ECAS inputs enable the corresponding \overline{CAS} outputs.

In systems that employ error correcting, transparent error scrubbing is one method of increasing data integrity without significant performance penalty. Scrubbing removes soft errors that accumulate between

a double-bit error occurs, that would require halting the system. With scrubbing, the refresh cycle becomes a full access during which data and ECC bits are continuously checked and updated. The 12-bit internal-scrubbing counter supplies the column-address bits; the 10-bit refresh-counter supplies the row-address bits. Upon detecting an error, the error-correction circuitry writes the proper data back to the DRAM through the use of a read-modify-write operation.

To enable this type of cycle, the system must assert EXTDRF while \overline{RAS} is low. \overline{RAS} and \overline{CAS} then re-

T RANSPARENT ERROR SCRUB- BING INCREASES DATA INTEGRITY WITHOUT CAUSING A SIGNIFI- CANT PERFORMANCE PENALTY.

main low until the rising edge of the next CLK, once EXTDRF goes low again. Error scrubbing must operate on whole words—not bytes—because ECC circuitry always reads or writes whole words. Though the KS84C21 controls the error-scrubbing operation, it doesn't supply the error-detection-and-correction circuitry.

Modes 2, 4, 5, and 7 support interleaving; modes 0, 2, and 4 maintain error scrubbing; and modes 0, 1, 3, and 6 support byte-writing and burst access. The configuration in the application example is mode 3, but with B_1 tied to ground so that only two banks are used. Mode 1 can also be used, but mode 3 better demonstrates the drive capability of the KS84C21's address and \overline{RAS} out-

puts.

Mode bit C_7 selects a minimum guaranteed setup time (t_{ASC}) Column Address of either 0 or 10 ns. The KMM581000-12 DRAMs in this application don't require any column-address setup time. But designers should consider the effects of other delays, including wiring delays, when choosing a zero setup time. Similarly, mode bit C_8 selects a minimum guaranteed Row Address hold time (t_{RAH}) of either 15 or 25 ns. Of course, the mode is set to deliver the KMM581000-12's specification for the row-address hold time of 15 ns. Once again, designers must consider other delays inherent in the design when choosing this value.

Ideally, the earlier DRAM accesses begin, the higher the system performance will be. In an "early write," \overline{WE} goes low early in the access before \overline{CAS} goes low. This is the situation if the KS84C21's \overline{WIN} input is tied to the 68020's R/\overline{W} signal. \overline{CAS} can then latch the data into the DRAM earlier than if \overline{WE} followed \overline{CAS} to do the same. But there can be a problem if \overline{CAS} goes active before the input data is valid at the DRAM. This is due to delays in the transceivers and wiring.

That can be avoided by gating the 68020's Data Strobe (\overline{DS}) with the ECAS inputs to hold \overline{CAS} at least 10 ns after the data is valid at the 68020. If bit C_9 on the KS84C21's mode register is set, \overline{CAS} is delayed t_{C24} beyond the first rising edge of CLK after \overline{CAS} would normally go low. If this still isn't enough time, any \overline{CAS} output can be further delayed from going low by holding the appropriate ECAS input high. The "no delay" option was programmed for this design. □

Otto Sponring, senior system applications engineer at Samsung, holds an engineering degree (equivalent of a BSEE) from FH Munich, West Germany.

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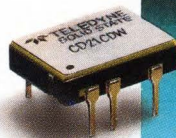
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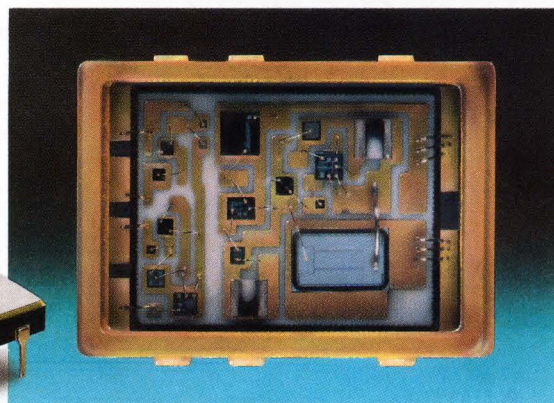
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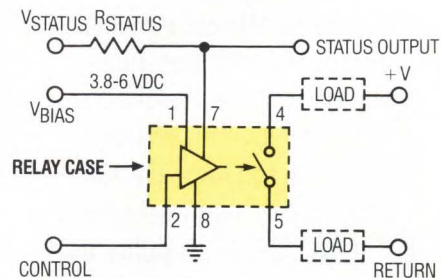
PART # CD21CDW

Review the electrical characteristics and call us for immediate application assistance.*

ELECTRICAL CHARACTERISTICS (-55°C to +105°C unless otherwise noted)				
	Min	Max	Units	
Bias Voltage (V_{BIAS})	3.8	6.0	V_{DC}	See Note 1
Bias Current (I_{BIAS})		15.0	mA	$V_{BIAS} = 5V_{DC}$
Control Voltage (V_{IN})	0	18.0	V_{DC}	
Control Current (I_{IN})		250	μA	$V_{IN} = 5V_{DC}$
Turn-Off Voltage $V_{IN(OFF)}$	3.2		V_{DC}	
Turn-On Voltage $V_{IN(ON)}$		0.3	V_{DC}	
Continuous Load Current $I_{LOAD @ 60VDC}$		1.2 0.7	A	-55°C to +25°C +85°C
Output Trip Current (I_{TRIP})		2.4 (Typ.)	A	+25°C, 100ms
On-Resistance (R_{ON})		0.65	Ohms	
Turn-On Time (T_{ON})		1.5	ms	
Turn-Off Time (T_{OFF})		0.25	ms	
Status Voltage (V_{STATUS})	1	18	V_{DC}	
Status Current (I_{STATUS})		2	mA	$V_{SAT} \leq 0.3V_{DC}$ See Note 2

Notes: 1. Series resistor is required for bias voltages above 6V_{DC}. $R_S = (V_{BIAS} - 6V_{DC})/15 \text{ mA}$
 2. A pull up resistor is required for the status output. $R_{STATUS} = (V_{STATUS} - 0.3)/I_{STATUS}$
 3. Output will drive loads connected to either terminal (sink or source).
 4. Status circuit is a built-in test feature checking the input circuitry of the relay. Status output is low (on) when the input is on.

All power FET relays may drive loads connected to either positive or negative referenced power supply lines (source or sink modes).



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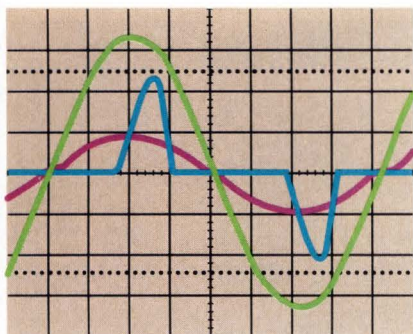
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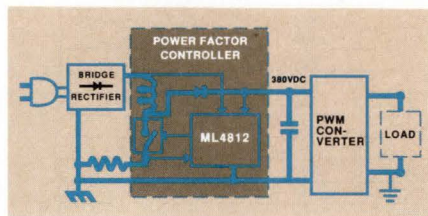
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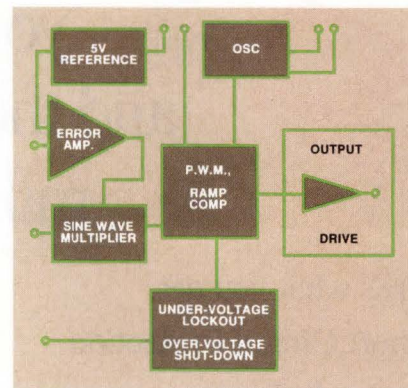
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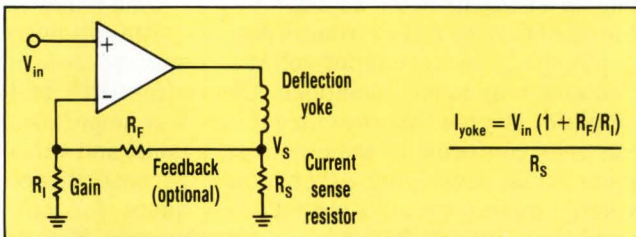
Even if you build magnetic deflection amplifiers everyday, they aren't the easiest circuits to design. Moreover, if you're a novice, they can represent a horrendous task. Not only must they accurately reproduce fast, complex waveforms, but they must handle high voltages and currents reliably and without excess dissipation. And they must drive inductive loads within a feedback loop, which can be tricky. Here's a way to simplify your job with a family of power op amps.

The term, "deflection amplifier," generally describes circuits used to deflect an electron or ion beam either directly (electrostatic) or via an inductor (magnetic). While most commonly associated with CRTs, deflection amplifiers are used in various applications, including scanning electron microscopes, small cyclotrons, and beam-deposition systems.

The two methods used for deflection—magnetic and electrostatic—require completely different amplifier designs. In general, magnetic deflection requires high power (current) at relatively low voltages, while electrostatic deflection requires high voltages but negligible current. Moreover, you can optimize the quality of the deflection, especially its linearity, by choosing the proper amplifier configuration. In particular, magnetic-deflection amplifier design requires careful consideration of power dissipation, bandwidth, and dynamic stability (they must not ring or oscillate). These requirements are typically in conflict with each other.

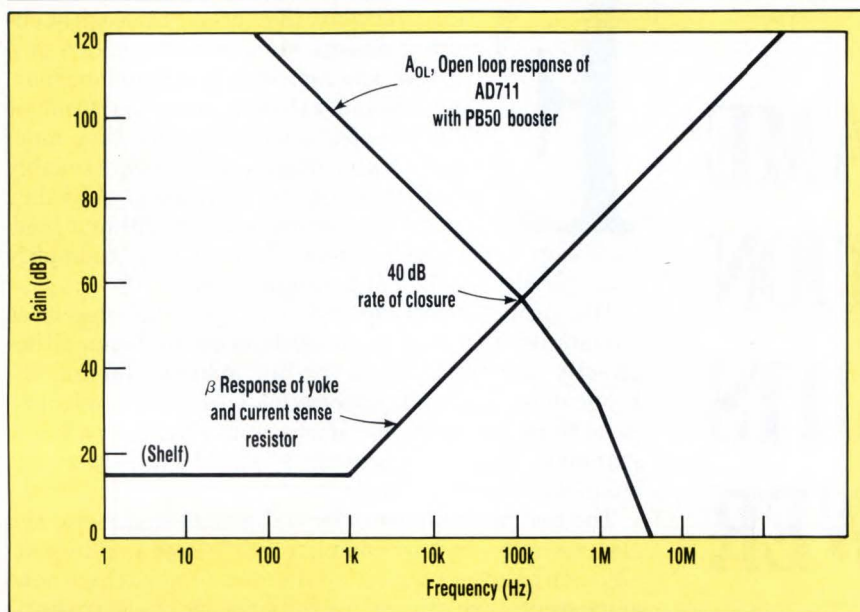
A circuit component recently introduced by Apex, the PB50 power booster-with-gain amplifier, is well suited for use in magnetic-deflection amplifiers (see "A look inside the PB50"). This hybrid's output voltage swings up to ± 90 V and ± 2 A, while slewing at 50 V/ μ s. The booster is designed to be driven by a small-signal op amp with a feedback loop closed around both devices. This configuration is called a composite amplifier. Designers may shy away from such a combination because of concerns over stabilizing the composite amplifier—particularly when the power booster has gain, as with the PB50. Furthermore, the typically employed, current feedback magnetic deflection circuit is inherently unstable.

Using the PB50 booster in a magnetic-deflection amplifier application shows you how to solve these stability problems and illustrates the ease with which the booster can be designed into even difficult applications. A circuit for a companion part to the PB50, the PB58, operates



1. THE VOLTAGE ACROSS the current-sense resistor is a function of V_{in} and the current through the op amp. Thus, the deflection yoke's current is a function of V_{in} .

MAGNETIC AND ELECTROSTATIC DEFLECTION AMPS



2. AN INDUCTANCE within the closed feedback loop of an op amp produces an inherently unstable, 40 dB/decade rate-of-closure.

from ± 150 V.

Beam position in magnetic deflection applications is a function of deflection yoke current. Consequently, among modern op-amp topologies, the basic current-control configuration, in its simplest noninverting form, becomes the circuit of choice (Fig. 1). A voltage V_{in} applied to the noninverting (+) input forces the amplifier output to reach the value necessary to make the voltage on the inverting input equal to V_{in} . The output voltage feedback V_s (in this circuit) is developed across a low-value resistor R_s in series with the deflection yoke. Because V_s is a function of the yoke current, the circuit supplies a yoke current directly proportional to the input voltage.

In addition, this current feedback linearizes the input voltage-to-output current relationship. For example, in sawtooth-scan applications, the circuit can be driven from an easily obtained sawtooth input voltage. Yet under dynamic conditions, the amplifier insures that the current in the yoke conforms to the sawtooth input while developing exponential voltage waveforms at its output (the amplifier's output). In fact, such current feedback circuits eliminate the need for a vertical-linearity control in TV and other CRT applications.

While the basic circuit and concept are really quite simple, there's problems in real-world applications. An analysis of the feedback loop frequency response, plotted against the amplifier open-loop gain, reveals inherent instability because of a 40 dB/decade rate-of-closure of the response. Your job is to come up with a stable design—without limiting the circuit's speed.

First, you must choose the right amplifier to supply the high level of performance required for deflection amplifiers—especially at the high sweep rates required for horizontal deflection in the latest raster-scan graphics systems. A typical application might need an amplifier with the following specifications:

Output voltage swing: ± 30 V
Current: ± 2 A
Slew rate: 50 V/ μ s
Gain-bandwidth: 10 MHz

The op amp parameters associated with dc accuracy—such as offset, offset drift, and bias current—are of less importance (in these applications) and values offered by general purpose devices are usually adequate for any op-amp based approach. However, the high output voltage and current requirements may steer you toward a power op-amp solution, which is often used for

magnetic deflection applications. Such power op amps as the Apex PA09 and PA19 work well for magnetic deflection because they put out up to 4 A at up to 3 MHz.

However, the cost requirements of a system often preclude the use of the power op amp. And the need to "flex" the power supply rails to minimize power dissipation (that is, to dynamically change the supply voltages in sync with the drive signal) could complicate the use of a power op amp. Previously, the only alternative was a discrete design made with discrete power transistors.

At first glance a discrete design may look good—not simple, but possible. It consists of a small signal op amp, such as an AD711, driving a power output stage. The driver op amp can operate with constant supply rails, allowing it to maintain full control of the output, while the supply rails of the output stage are "flexed" to minimize dissipation.

At a minimum, the approach requires a lengthy design effort to address all the reliability and performance requirements. For example, Class A/B biasing is required because low crossover distortion is critical. If the amplifier is needed to operate over a wide ambient temperature range, then just optimizing the output-stage biasing circuitry is complex. In addition, the amplifier's internal stability must be addressed—along with the added stability of the yoke-filled feedback network. A tough egg to crack. Moreover, what has become a high-component-count circuit results in tradeoffs of reliability and economy.

The typical discrete approach might consist of cascaded, complementary, common-emitter stages taking the output from the second set of collectors. It provides both high efficiency and bandwidth. But stabilization of the common-emitter output stage, with local gain connected in a feedback loop around an op amp, can be difficult. The PB50 booster essentially packs all the circuitry of such a discrete amplifier into an 8-pin TO-3. Moreover, it cuts valuable board area and also simplifies the job of stabilizing the com-

MAGNETIC AND ELECTROSTATIC DEFLECTION AMPS

plete composite amplifier loop—yoke and all.

The goal of this magnetic deflection amplifier design, including its compensation, is to obtain the fastest response possible while remaining free of excessive ringing or overshoot. As noted, the current feedback deflection circuit is inherently unstable (*Fig. 2*). The open loop response A_{OL} is the response of the composite amplifier—the AD711 driver plus the PB58 booster with its 22-pF compensation capacitor between pins 1 and 8 (*Fig. 3a*).

Superimposed on the amplifier response is the response of the yoke and sense-resistor feedback network. The network has a pole occurring at the frequency set by the 200- μ H yoke inductance and the 0.5- Ω sense resistor. The horizontal section of the curve, or shelf, at frequencies below 1 kHz represents the effect of the closed loop gain-setting feedback and input resistors, R_F and R_I . The effect, if any, of yoke dc resistance will appear in this region, too. The intersection of the feedback-loop response and the open-loop response exhibits a 40 dB/decade rate of closure. However, optimum stability demands a rate-of-closure less than 20 dB/decade.

Note also that at 100 kHz, the amplifier response curve encounters another pole that increases the amplifier slope to greater than 20 dB/decade, though it doesn't reach 40 dB/decade until about 1 MHz. The region above 100 kHz and at closed

loop gains below 55 dB will be marginal for stability, while the region above 1 MHz is definitely unstable for gains less than 30 dB. It will be necessary to overcome the effects of the rate of closure caused by yoke feedback, without causing the amplifier to operate in any unstable areas.

You could simply connect a damping resistor in parallel with the yoke, which would provide stability, but your intent is to create an amplifier that's a true current source. By definition, the true current source can't have pure resistance in parallel with its load, unless that resistance is an intended part of the load. This parallel resistor technique offers less than optimum performance for the magnetic deflection amplifier—especially for rapid transitions.

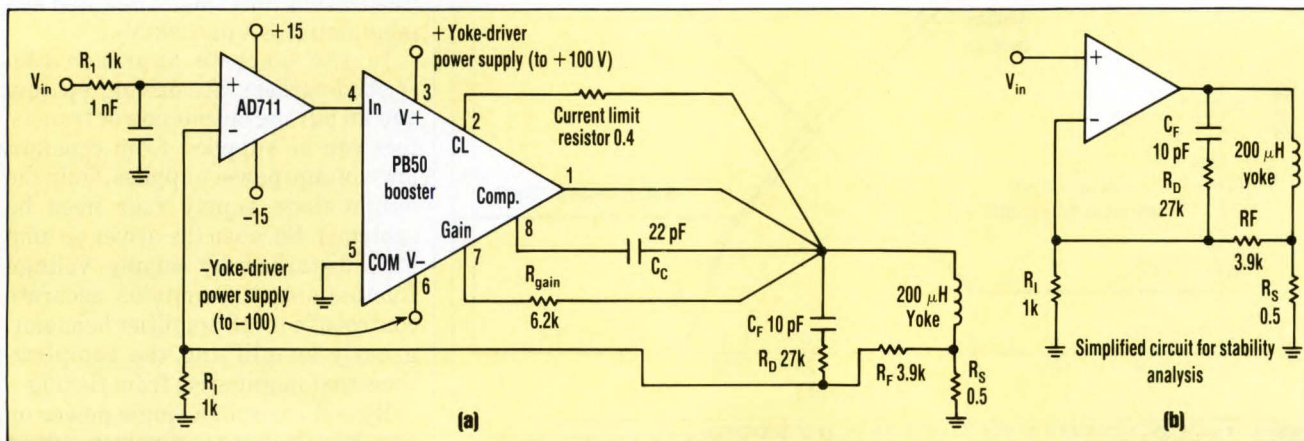
To supply maximum stability and speed, select a circuit that combines a dominant high-frequency feedback path with ideal phase and gain relationships (*Fig. 3b*). The circuit illustrates the use of the auxiliary feedback components R_F , C_F , and R_D , and gain setting resistor R_I . Here, R_I was selected to supply an overall gain of five to enhance stability.

The easiest way to select component values for the auxiliary stabilizing feedback is by plotting gain and feedback relationships graphically (*Fig. 4*). This method takes advantage of information on any amplifier data sheet. You can then see the amplifier response, superimposed on booster response, plus yoke-resistor feedback response.

To arrive at values for the stabilizing feedback, select a ratio for $R_D/(R_F \text{ in parallel with } R_I)$ greater than the open-loop gain at the point where the composite amplifier response begins to exceed 20 dB/decade. This gain level insures that the feedback isn't excessive when the phase response from the amplifiers themselves has gone past the point that's acceptable for stability. At the same time, the ratio must be at least 20 dB lower in amplitude response than the yoke feedback at the intersection of yoke feedback and A_{OL} so that the auxiliary feedback dominates at this critical point.

In the amplifier used here another approach was chosen to best realize high-speed performance. R_D was selected for a high-frequency shelf above the point where the amplifier A_{OL} response reaches 40 dB/decade at 1 MHz. Typically, this might seem potentially unstable because the high-frequency closed-loop gain intersects the A_{OL} curve where A_{OL} is still decreasing at something over 20 dB/decade. But proper capacitor selection overcomes the phase shifts present at this point.

The capacitor would usually be selected to supply an upward break in the auxiliary feedback response at a frequency an order of magnitude less than the intersection of the yoke response and A_{OL} curve. To increase response speed, the capacitor can be decreased with the limit occurring where the upward break intersects the A_{OL} curve. In this example,



3. THE PB50 BOOSTER amplifier driven by an op amp (the AD711) forms a high-speed current source for driving a CRT magnetic-deflection yoke (a). The circuit is stabilized by the RC network across the yoke. Stability analysis is easier with the simplified circuit (b).

MAGNETIC AND ELECTROSTATIC DEFLECTION AMPS

A LOOK INSIDE THE PB50

The DMOSFET output devices are the key in the architecture of the PB50 and 58, which gives the performance needed of these deflection-amplifier applications. These power transistors make possible the full-power bandwidth of the PB series over 160 kHz. The architecture resembles an op amp with a single-ended input stage. A bipolar transistor is used on the

input because FETs offer no real benefit as the device will be driven by an op amp. This transistor drives a MOSFET, which supplies the gain and high-voltage for the output stage.

The output stage consists of a V_{gs} multiplier and complementary pair of MOSFET followers with bipolar transistor between each gate and source implementing the hybrid's current-limit function. A

few other bipolar transistors serve as the current sources dedicated to biasing the amplifier.

The PB series has a built-in overall feedback loop when pin 7 is connected to the output. While this loop sets a gain of three, it can be raised with an external resistor in series with the loop. The PB series is compensated with capacitor C_C in parallel with the feedback resistance.

though, the capacitor was selected to supply an upward break in response that nearly intersects the A_{OL} curve. This causes a phase lead to occur in the feedback loop, which moderates the effect of the greater than 20 dB/decade amplifier roll-off experienced at this point. The actual circuit proved to be unconditionally stable and free from ringing.

Power dissipation in deflection amplifiers can be directly affected by the amplifier's speed requirements. The drive voltage required at the yoke is a function of how rapidly current must be changed in the yoke. Higher voltages mean higher speeds. But most deflection circuits are required to operate over a range

of speeds. Vector scan systems may operate at any rate and sawtooth raster scan systems, by their very nature, operate with at least two speeds: one for scan, one for retrace.

One approach you can take is to set power-supply voltages high enough to accommodate the highest speed required. However, this is inefficient and can produce unnecessary amplifier heating as a result of internal power dissipation.

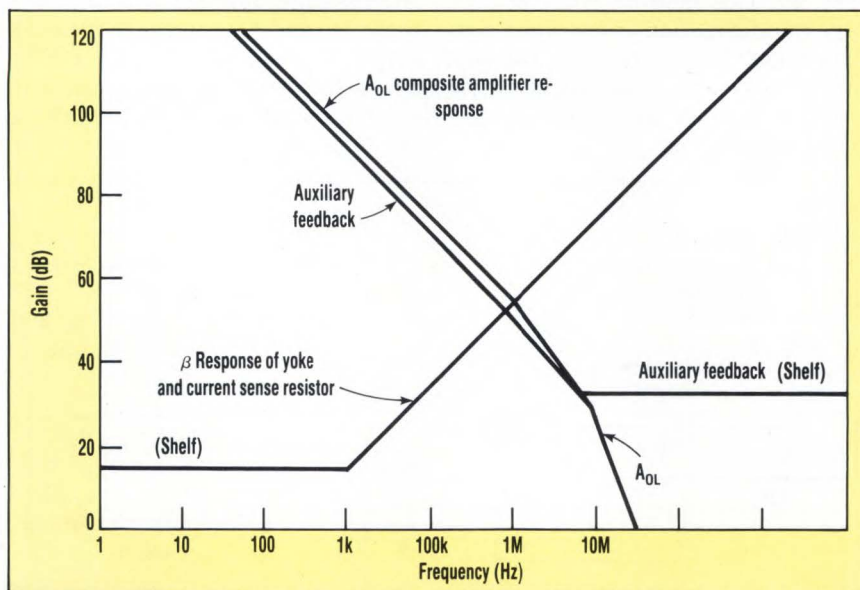
In a sawtooth raster scan application, designed to operate at a set sweep speed and amplitude, it's possible just to use nonsymmetrical supply voltages to solve the efficiency problem. In vector scan systems, or systems where widely varying

speeds are required, the power-supply voltages can be varied to suit the immediate requirements.

Generally, two discrete sets of power-supply voltages are used for the power amplifier, and its supply pins are switched between them in synch with the drive signal (*Fig. 5*). The lower voltages are obtained via the diodes ("ultra-fast" recovery devices rated for at least 1 A and 200 V) between the driver's ± 15 V supply, which can power the other analog circuits, and the booster's supply pins. Switching on Q_1 turns on the pnp Darlington and applies a positive high voltage to the PB50 booster (a maximum of 100 V), and its output can swing positive. Similarly, turning on Q_2 applies a negative high voltage to the booster (via the npn Darlington) making it possible for its output to swing negative. In either case, the diodes disconnect the low-voltage supplies from the booster (the Darlington's should be rated at a minimum of 5 A and 200 V).

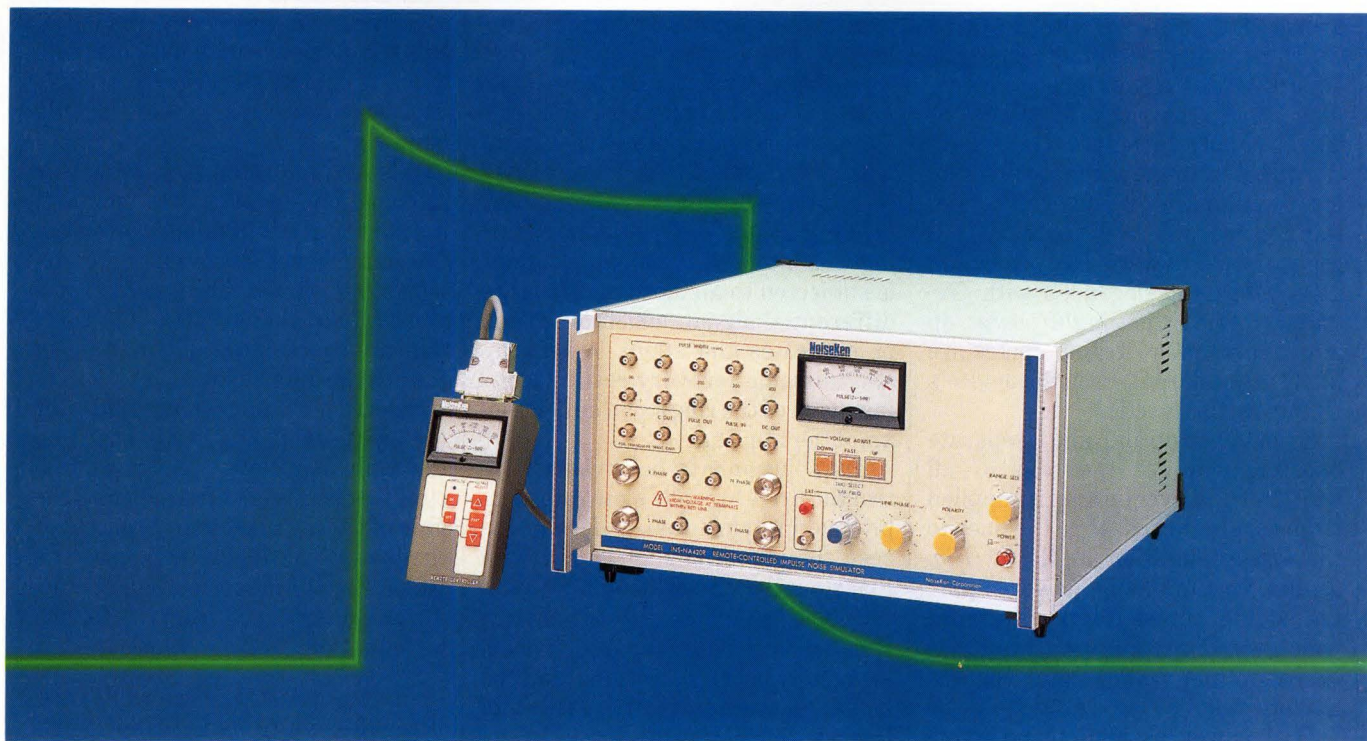
In the discrete approach (described earlier), the driving op amp and all but the output power transistors can be supplied from constant low-voltage power supplies. Only the output-stage supply rails need be switched. Because the driver op amp isn't disturbed by supply voltage fluctuations, it maintains accurate control of overall amplifier behavior, greatly simplifying the complications that might arise from flexing.

By comparison, a single-power op amp has an input and power output stage with their supply lines tied together internally. Because they



4. INSURING THAT THE AUXILIARY FEEDBACK (the RC network across the yoke) response dominates the circuit, at the point where the composite amplifier response begins to exceed 20 dB/decade, creates a stable design for driving deflection yokes.

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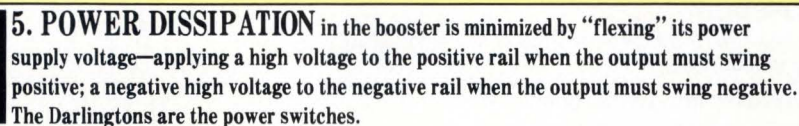
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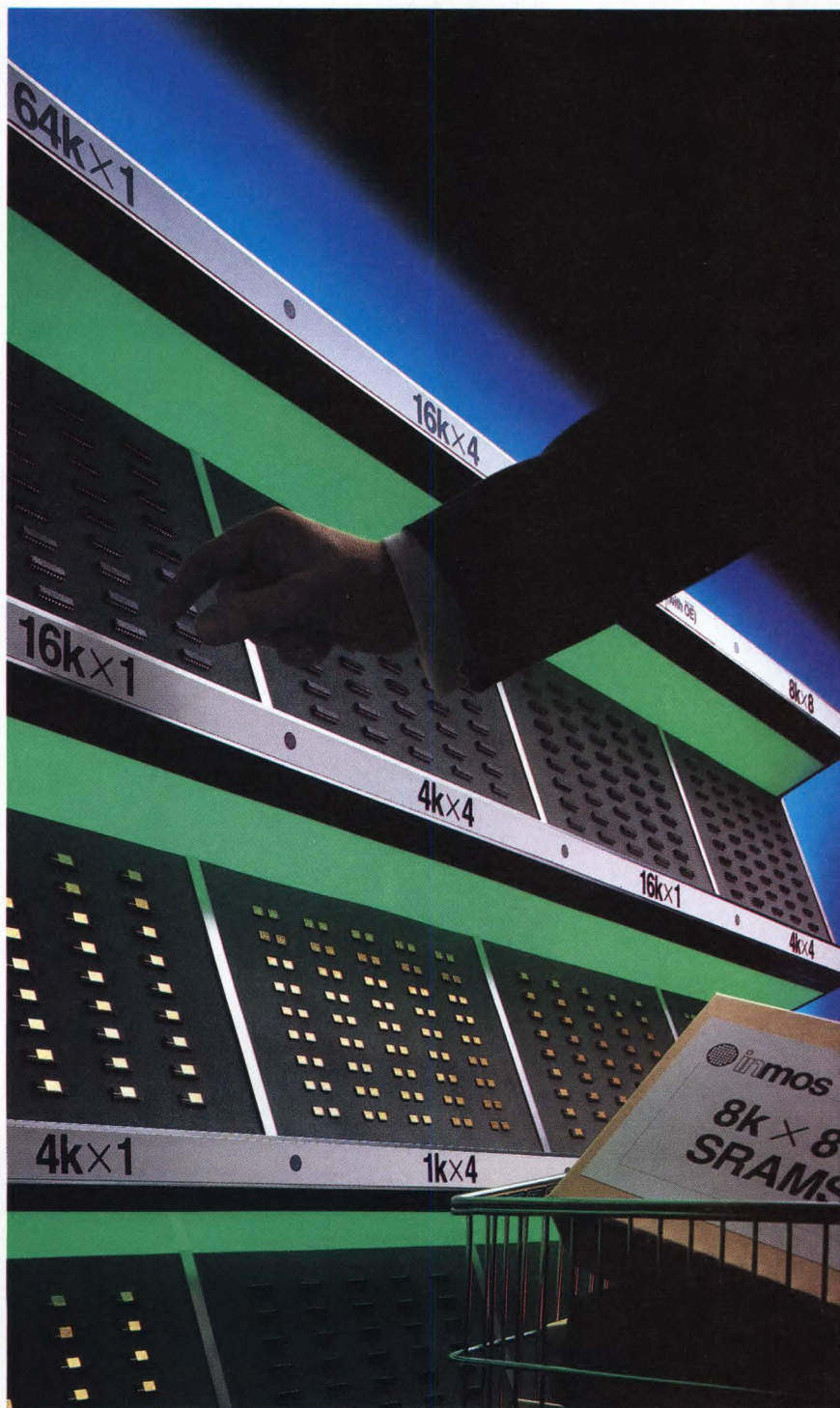
Choosing the proper stabilizing feedback is certainly the most important item in controlling settling behavior. But the effect of "slew-rate

A simple, universal method, consists of just a one-pole low-pass R-C filter at the amplifier input. Initially, this might seem undesirable because

In contrast to the magnetic-deflection amplifier's need for high currents, electrostatic-deflection amplifiers require the use of high voltages and low currents. With its ± 150 -V swing capability, or up to 300 V rail-to-rail, a PB58 power op amp is the preferred choice for electrostatic deflection. The PB58 is the most economical wideband solution available at up to 300 V. With its current capability of 1.5 A, the PB58 is also useful



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				MK 6116L	150,200
1Kx4	IMS 1223	20,25,35,45	64Kx1	IMS 1600	20,30,35,45,55
	IMS 1223M	25,35,45		IMS 1601L	45,55
16Kx1	IMS 1403	25,35,45,55		IMS 1600M	45,55,70
	IMS 1403M	35,45,55		IMS 1601LM	45,55,70
	IMS 1403LM	35,45,55	16Kx4	IMS 1620	25,30,35,45,55
	IMS 1400M	45,55,70		IMS 1620M	45,55,70
	MK 41H67	20,25,35		IMS 1620LM	45,55,70
4Kx4	IMS 1423	25,35,45,55		IMS 1624	25,30,35,45,55
	IMS 1423M	35,45,55		IMS 1624M	45,55,70
	IMS 1420M	55,70		IMS 1624LM	45,55,70
	MK 41H68	20,25,35	8Kx8	IMS 1630M	55,70
	MK 41H69	20,25,35		IMS 1630L	45,55,70,100,120
	MK 41H79	25,35		MK 48H64	70,120
2Kx8	MK 6116	150,200		MK 48H64L	70,120

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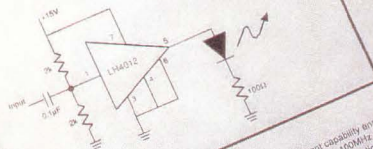
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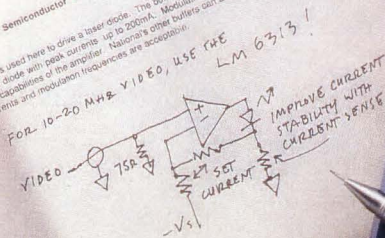
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- Operational Amplifiers
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- Voltage Comparators
- Instrumentation Amplifiers
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Laser Diode Transmitter



LM385 is used here to drive a laser diode. The buffer's high output current capability enables it to drive the diode with peak currents up to 200mA. Modulation frequencies over 100kHz are well within the capabilities of the amplifier. National's other buffers can also perform this function if lower drive currents and modulation frequencies are acceptable.



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Session III:

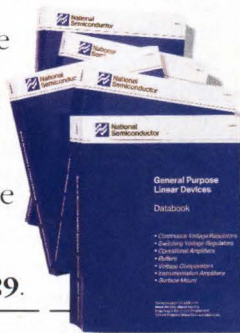
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NSCSMFP02

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Semiconductor**

KEPCO, INC. announces a new class of Programmable Power Supplies that communicate and are controlled entirely by Digital Signals...Series TMA/MAT DIGITAL POWER SUPPLIES TO THE MATE PROTOCOL



Kepco's fifth generation power control system, TMA/MAT meets MATE requirements for modular test equipment integration.

- Built-in isolation relays switching power and sense lines. Relays are switched with proper sequencing.
- Voltage polarity reversal relay.
- Linear design for fast response, full 12 bit resolution and low noise.
- Each output is fully isolated from the others and from ground.
- Modules may be programmed as either voltage or current sources through their entire range. No derating, no foldback limiting.
- LCD metering of voltage and current. Values read back to the IEEE 488 bus.
- Individual on/off circuit breakers. Modules may be removed without shutting down system.

- Each module includes an auto-tracking over-voltage sensor with crowbar, $E_o + 10\%$.
- Each module includes an auto-tracking over-current sensor, $I_o + 10\%$.
- Power loss protection, flag-signal to IEEE 488 bus from each module.
- Selectable 115V a-c and 230V a-c input mains.
- Modularity lets systems designers choose just the outputs needed. Modules for 360W, 720W and 1080W. TMA controller can address up to 27 modules.
- Each $1/3$, $2/3$ module installs and is removed from the front without disassembly.
- Front panel LEDs: voltage and current mode, output enabled, polarity.



Digital Power Supplies to the MATE Protocol..Kepco Series MAT



Three 360 Watt MAT modules shown in RA 50 Housing

Power modules, called MAT are available in 3 basic power sizes:

360 WATT 1/3 RACK WIDTH
720 WATT 2/3 RACK WIDTH
1080 WATT FULL RACK SIZE

360 WATT MODULES – 1/3 RACK

Single output. Nominally 360 Watts.
Mount in RA 50 and RA 51.

Model	Volts	Amps	Power
MAT 6-32	0-6	0-32	192
MAT 15-20	0-15	0-20	300
MAT 25-14	0-25	0-14	350
MAT 36-10	0-36	0-10	360
MAT 55-7	0-55	0-7	385
MAT 75-5	0-75	0-5	375
MAT 100-3.6	0-100	0-3.6	360
MAT 150-2.4	0-150	0-2.4	360

720 WATT MODULES – 2/3 RACK

Single output. Nominally 720 Watts. Mount in RA 51

Model	Volts	Amps	Power
MAT 6-64	0-6	0-64	384
MAT 15-40	0-15	0-40	600
MAT 25-28	0-25	0-28	700
MAT 36-20	0-36	0-20	720
MAT 55-14	0-55	0-14	770
MAT 75-10	0-75	0-10	750
MAT 100-7.2	0-100	0-7.2	720
MAT 150-4.8	0-150	0-4.8	720

1080 WATT MODULES – FULL RACK

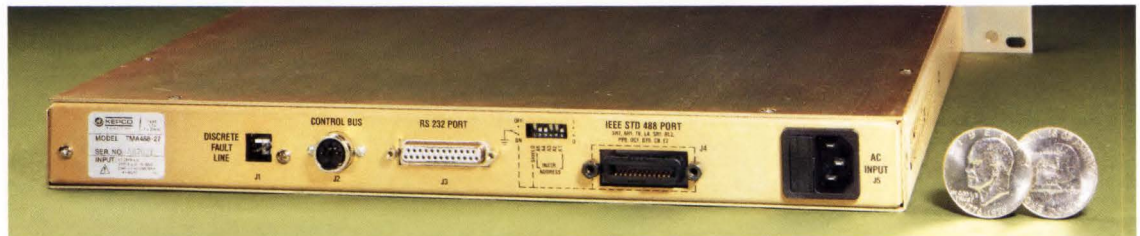
Single output. Nominally 1080 Watts.
Mount directly into 19" rack. Panel: 5 1/4" Depth: 25"

Model	Volts	Amps	Power
MAT 6-100	0-6	0-100	600
MAT 15-60	0-15	0-60	900
MAT 25-42	0-25	0-42	1050
MAT 36-30	0-36	0-30	1080
MAT 55-20	0-55	0-20	1100
MAT 75-15	0-75	0-15	1125
MAT 100-10	0-100	0-10	1000
MAT 150-7	0-150	0-7	1050

The Controller: Kepco Model TMA 488-27



Front view of Kepco Model TMA 488-27



Rear view shows discrete fault line, GPIB and RS232 inputs and the 2-wire control bus output

DESCRIPTION & SPECIFICATIONS

The Kepco model TMA 488-27 is a power supply controller to program, control and monitor the output of up to 27 Kepco power modules in the "MAT" series at distances up to 1000 feet.

The controller receives commands and transmits data to a host computer over the bi-directional digital control bus IEEE-488 (also known as GPIB) or over a serial communications link using RS232.

The IEEE-488 interface functions implemented by this controller are:

SH1, AH1, T6, L4, SR1, RL2, PP0, DC1, DT0, C0.

The programming language used by the Kepco Model TMA 488-27 is CIIL (Control Interface Intermediate Language) now the test instrumentation module programming language standard for all new U.S. Air Force "MATE" test equipment programs.

CIIL is a compiled form of Atlas. It provides a uniform programming format for all basic test instrumentation. The CIIL, also known as U.S. Air Force 2806763 Rev. C standard, facilitates systems integration, upgrades and modifications, needed to keep systems up with the latest technology.

The following CIIL commands are accepted and interpreted by the Kepco TMA 488-27 controller:

A) OP CODES

FNC - FUNCTION	OPN - OPEN
SET - SET OUTPUT	RST - RESET
SRX - SET MAXIMUM	IST - INTERNAL SELF TEST
SRM - SET MINIMUM	CNF - CONFIDENCE TEST
INX - INITIALIZE	STA - STATUS
FTH - FETCH	GAL - GO ALTERNATE
CLS - CLOSE	LANGUAGE

B) NOUNS

DCS - DIRECT CURRENT SOURCE

C) NOUN MODIFIERS

VOLT - VOLTAGE	CURR - CURRENT
VLTL - VOLTAGE LIMIT	CURL - CURRENT LIMIT

The following functions of any one of the 27 (twenty seven) type MAT power modules can be programmed from the TMA 488-27 controller over a fast digital communication 2 wire control bus:

- Output voltage with current limit
- Output current with voltage limit
- Output enable/disable via open/close command to power relays built into each MAT power module
- Output polarity reversal with power relays built into each MAT power module

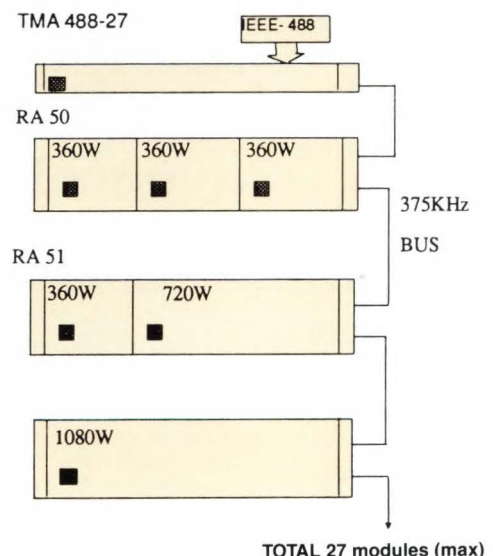
Overvoltage and overcurrent protection tracks the programmed voltage and current. The following data is read back from each power module and transmitted over the IEEE-488:

- Actual measured output voltage
- Actual measured output current
- Present status
- Error messages

The controller continuously monitors the status of each power module for the correctness of the programmed voltage or current, overvoltage, overcurrent, crowbar, overtemperature, power loss, output enable and polarity reversal status and other fault conditions. Any changes from normal set conditions will generate error flags reported over the communications bus.

For catastrophic failures, a separate 2 wire status monitor line (also known as discrete fault indicator) is activated for fast direct communication with the host computer.

An internal switching power supply featuring wide range a-c input powers the TMA 488-27.



Series MAT Specifications

PARAMETER	CONDITION	MAT POWER MODULE		
Description		360W	720W	1080W
Input Voltage Range	User Selectable	105-125V a-c 210-230V a-c		
Input Current max	115V a-c	7.0A	14.0A	21.0A
	230V a-c	3.5A	7.0A	10.5A
Input Frequency	Range	47-63 Hz		
Source Effect	Voltage	0.001% E_{omax}		
	Current	0.005% I_{omax}		
Load Effect	Voltage	0.002% E_{omax}		
	Current	3 mA		
Time 8 Hour Drift	Voltage	0.01% E_{omax}		
	Current	0.02% I_{omax}		
Temperature Coefficient/°C	Voltage	0.01% E_{omax}		
	Current	0.02% I_{omax}		
Ripple & Noise rms/p-p	Voltage	0.3mV/3mV		
	Current	0.03%/0.3% I_{omax}		
Transient Recovery	Voltage	100 μ sec.		
Programming Resolution	Voltage	0.024% E_{omax} (12 Bits)		
	Current	0.024% I_{omax} (12 Bits)		
Data Read-Back Accuracy	Voltage	0.1% E_{omax}		
	Current	0.1% I_{omax}		
Operating Temperature	Range	0° to 50°C		
Remote Sensing	Range	0.5V per lead		
DC Output Isolation	Voltage	500V d-c		
Output Display	3½ Digit LCD	Switch Selectable Voltage/Current		
Indicators	4 LED	Voltage Mode, Current Mode, Output enabled, Polarity reversed		
Output Enable/Disable		Built-in power & sense relays		
Polarity Reversal		Built-in polarity reversal power & sense relays		
Protection	Overvoltage	Tracks program voltage, crowbars output & turns-off input		
	Overcurrent	Tracks program current, crowbars output & turns-off input		
	Overtemperature	Monitors heatsink temperature, crowbars output & turns-off input		
	Polarity Reversal	Built in diode protects unipolar supply output		
	Power Loss	Detects loss of a-c input power, disables output		
Mounting	Front	1/3 rack modules plug into RA 50		
		1/3 plus 2/3 rack modules plug into RA 51		
		Full rack mounts directly in 15" rack		
Filler Panels	For either RA 50 or RA 51	RFP 50-1 1/3 panel; RFP 50-2 2/3 panel		

BACKGROUND

In 1965 Kepco introduced digitally-programmable power supplies controlled by precision ladder networks of wire-wound resistors with reed relays. Though slow, the resolution was phenomenal, even by today's standards. a 5-digit controller was top-of-the-line. (1 part in 100,000!)

In 1968 came Kepco's 2nd generation program-by-voltage instruments. They used the newly popular digital to analog converters.

The third generation arrived with the IEEE-488 bus in 1975. Kepco made (and still makes) a great variety of programmers that support the bus. Stand alone one and two-channel instruments and multiple model programmers. They address 4 or 8 separate power supplies, including conventional and high-speed varieties. Many models (Series BOP) feature an optional built-in IEEE card.

In 1984 Kepco announced support for the MATE program. We launched the TLD series that addressed up to 16 independent power supplies. Passing the various approval stages at MATE Headquarters: *Submitted... Candidate... Verified... and Inventory*, Kepco was officially awarded verified status on Oct 1 1987.

These CIIL language programmers mate with Kepco's ATE series and BOP series general-purpose power supplies. Although fully compatible with the TLD, these power supplies retain analog-control capabilities and bench-top instrument characteristics.

These new models, called MAT depart from our general purpose power supply format - with separate programmer - to integrate the digital controller within each module. A separate, low profile, interface decodes CIIL instruction received over the IEEE-488 bus and distributes them over a single 2-wire twisted pair to as many as 27 power modules ranging up to 1080 Watts.



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DIGITAL POWER SUPPLIES TO THE MATE PROTOCOL... Series TMA/MAT

FEATURES

- Simpler control processes lessen complexity and cost by eliminating features mainly used in lab or analog applications.
- Digital decoder with microprocessor is built into each power module. Permits control from a central processor over a two-wire communications bus.
- The $\frac{1}{3}$ and $\frac{2}{3}$ rack power module's mechanical structure allows installation and replacement from the front for easy maintenance.
- Increased power density without resort to switching techniques.
- Incorporates power isolation relays per the MATE protocol plus relays for voltage polarity reversal.
- Simplified interconnect cabling, no more than a twisted pair.
- Reduced size and cost.
- Fully supports the Control Intermediate Interface Language (CIIL) and the MATE Test Module Adapter (TMA) requirements.



Digital Power Supplies to the MATE Protocol...

A-C INPUT CONNECTOR

MODEL	CHASSIS MOUNT	MATING PLUG
All Models	MS3102A16-10P	MS3108A16-10S

D-C OUTPUT CONNECTORS

1/3 Rack	MAT 6-32	MS3102A20-15S	MS3106A20-15P
	All other models	MS3102A20-16S	MS3106A20-16P
2/3 Rack	MAT 6-64, MAT 15-40	MS3102A24-12S	MS3106A24-12P
	All other models	MS3102A24-20S	MS3106A24-20P
Full rack	All models	MS3102A28-20S	MS3106A28-20P

MIL STD connectors, MS type.. Amphenol or equivalent.

DIGITAL BUS CONNECTOR

All models	DIN 41524 (socket)	DIN 41524 (plug) Kepco P/N 142-0308
------------	--------------------	--

Use shielded twisted pair cable to interconnect the TMA 488-27 to MAT power modules. Use Belden type 9841 or equivalent. One 2-meter long cable with two mating connectors is supplied with each rack adapter (or full rack MAT) for field assembly.

2 NEW HOUSINGS RA 50 & RA 51

To accommodate the 1/3 and 2/3 rack size MAT modules, Kepco offers two new housings called RA 50 and RA 51. RA 50 is 5 1/4" x 19" x 25" and accepts up to three 1/3 rack power modules. RA 51 is like sized, but configured for one 1/3 rack module and one 2/3 rack module.

Filler Panels: RFP 50-1 (1/3 slot filler)
RFP 50-2 (2/3 slot filler)

The full rack (1080W) MAT power supplies mount directly into a standard 19" rack.

Features: RA 50 and RA 51

- Each power module installs from the front and has a latching means.
A MIL-type connector supplies a-c power to the modules.
- Two DIN-type connectors link to the communications bus (arrangement permits daisy chaining).
- An internal bus supports up to three plugged-in modules.

Rear view of RA 50 Housing with three 360W MAT modules. The d-c output connectors are on the rear of each module. The connector in the lower corner is the a-c main input and the two digital bus connectors are visible





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changed. “My wife and I aren’t worried about ourselves anymore. Now we’re thinking of our grandkids. We give them Bonds as gifts.” Savings Bonds come in a variety of denominations, are free from state and local income tax, and you can buy them at work or where you bank. For more information, call us, or write U.S. Savings Bonds, Dept. 892-M, Washington, D.C. 20226.

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Tough enough to meet full MIL-specs, capable of operating over a wide -55° to $+100^{\circ}\text{C}$ temperature range, in a rugged package... that's Mini-Circuits' new MAN-amplifier series.

The MAN-amplifier's tiny package (only 0.4 by 0.8 by 0.25 in.) requires about the same pc board area as a TO-8 and can take tougher punishment with leads that won't break off. Models are unconditionally stable and available covering frequency ranges 0.5 to 1000 MHz, NF as low as 2.8 dB, and power output as high as +15 dBm.

Prices start at only \$13.95, including screening, thermal shock -55°C to $+100^{\circ}\text{C}$, fine and gross leak, and burn-in for 96 hours at 100°C under normal operating voltage and current.

Internally the MAN amplifiers consist of two stages, including coupling capacitors.

A designer's delight, with all components self-contained. Just connect to a dc supply voltage and you are ready to go.

The new MAN-amplifiers series...
another Mini-Circuits' price/performance breakthrough.

MODEL	FREQ. RANGE (MHz)	GAIN dB		MAX. OUT/PWR†	NF	DC PWR	PRICE
	f_L to f_U	min	flatness††	dBm	dB (typ)	12V, mA	\$ ea. (10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇ MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
* MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_U/2$, $\pm 0.5\text{dB}$ †dB Gain Compression ◇ Case Height 0.3 in.

Max input power (no damage) +15 dBm; VSWR in/out 1.8:1 max.

*Active Directivity (difference between reverse and forward gain) 30 dB typ.

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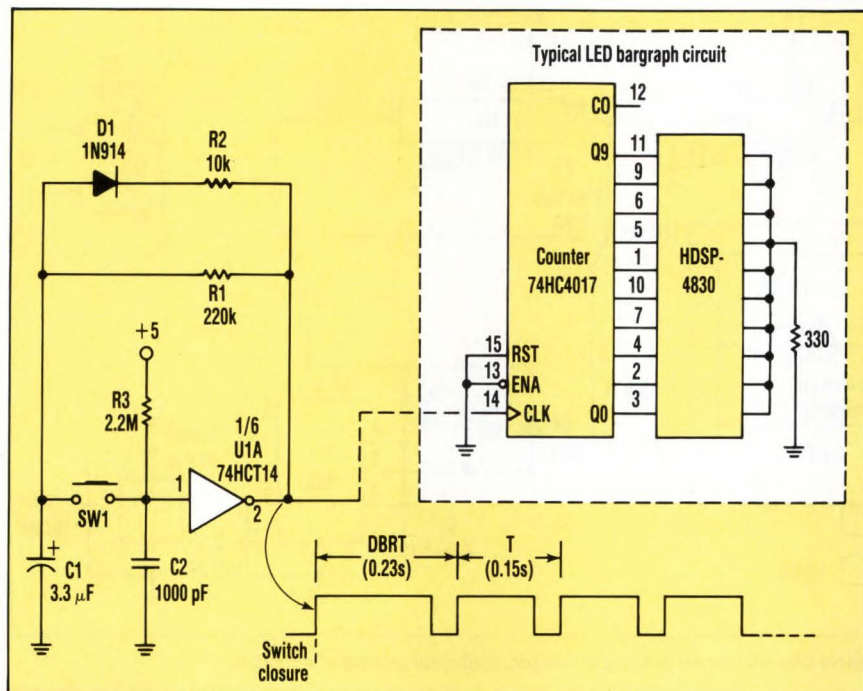
CIRCLE 123

C118 REV. E

CIRCLE 524 SWITCH DEBOUNCER ADDS AUTO-REPEAT

RALPH URSOLEO

Inovec Inc., 115 Wallis St., Eugene, OR 97402; (503) 485-7127.



THE CIRCUIT COMBINES a bar graph and an auto-repeat function. When the switch is open, the voltage in C1 is discharged back into the circuit.

A switch debouncer combined with an auto-repeat function, which is used to advance bargraph-type displays, generates one output pulse for each momentary switch closure. But if the switch is closed for longer than the delay-before-repeat time (DBRT), the circuit generates a continuous stream of pulses.

With the switch open, the gate input is pulled high. This forces the output low and discharges C1 through the feedback network (see the figure). When the switch is closed, the circuit immediately generates an output pulse and becomes the classic hysteresis-gate oscillator. It also creates a nonsymmetrical output due to R2 and D1.

The DBRT is due to the start-up time of the oscillator. The start-up time is greater than one period of the oscillator's output. For the first cycle, C1 has to charge from zero to the

upper gate switching threshold, rather than from the lower threshold as for subsequent cycles. The auto-repeat period (T) is approximately: $T = (R1 + R2) \times (C1 + C2) \times (\text{gate hysteresis/supply voltage}) = 0.15 \text{ s}$

CIRCLE 525 PHOTO-EVENT TIMER MEASURES TO 0.1 S

DENNIS EICHENBERG

6294 Mariana Dr., Parma Heights, OH 44130; (216) 888-0058.

Do you have to measure events such as flame-ignition, duration, and extinguishing times? For an accuracy to a tenth of a second, this photocell-event timer can do the job (see the figure).

In the circuit, transformer T1 couples the circuit to the power mains, and the 60-Hz line frequency sup-

plies the clocking signal. Resistor R1 and diode D3 clamp the clocking signal from T1 to 12 Vdc. The 4093 Schmitt trigger IC2 conditions the clocking signal, and voltage regulator IC1 delivers 12 Vdc.

Photocell PC1 controls the time gating through op amp IC5, which operates as a comparator, and whose threshold level can be adjusted with

IFD WINNERS

June 8, 1989

Gary Rauh, Seeq Technology Inc., 1849 Fortune Dr., San Jose, CA 95131. His idea: "Control the Vpp to Flash EEPROMs."

June 22, 1989

Bill Macbride, Glenmore Instrument Co., 12 Little Conestoga Rd., Glenmore, PA 19343. His idea: "Divide/Multiply with Only One Trim."

June EDI, 1989

Michael A. Wyatt, Space and Strategic Avionics Div., Honeywell Inc., 13350 U.S. Hwy. 19 South, Clearwater, FL 34624-7290. His idea: "Phase Meter Uses Just Two Chips."

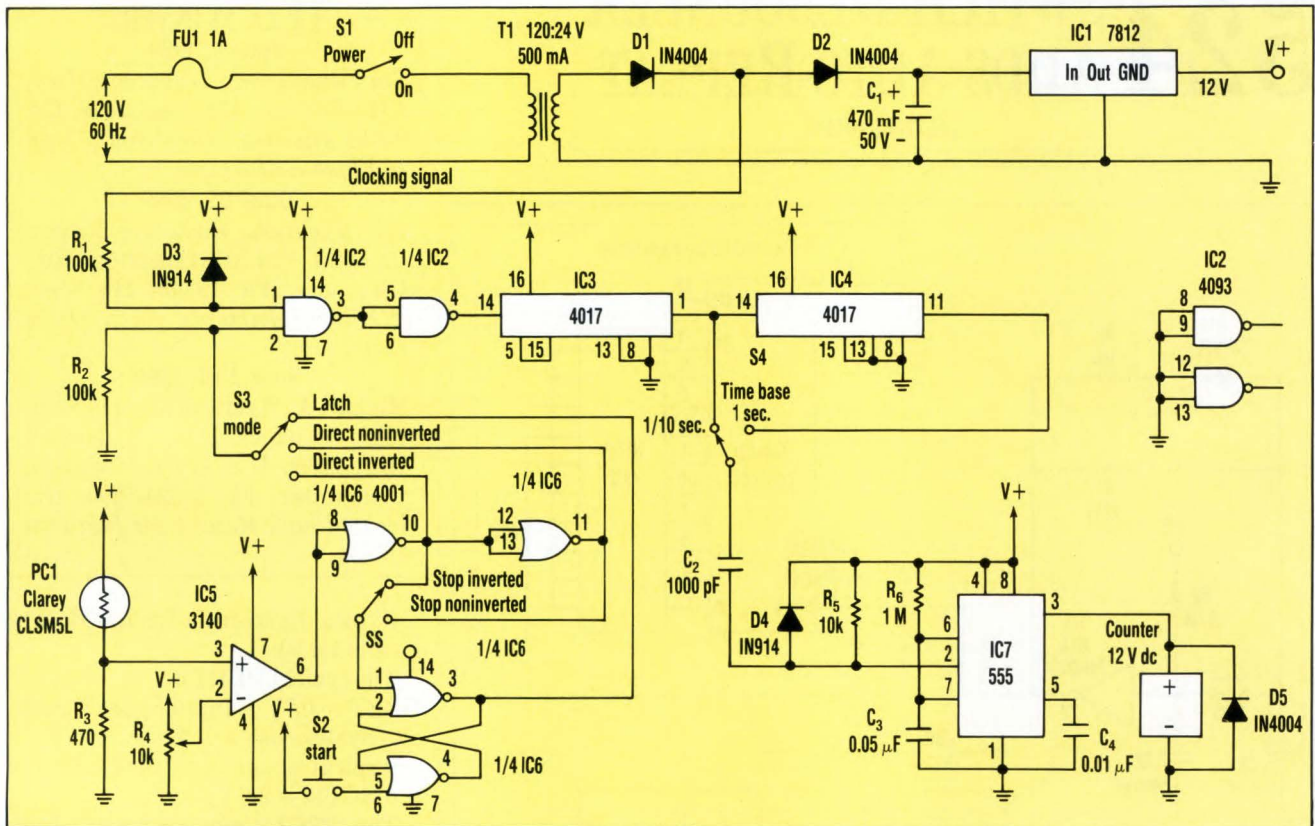
(typical hysteresis for the HCT14 gate is 1.0 V).

The typical DBRT is:

$\text{DBRT} = 0.7T \times (\text{upper gate threshold/hysteresis}) = 0.23 \text{ s}$

(typical upper gate threshold for the HCT14 is 2.3 V).

The R3C2 time constant, along with gate hysteresis, prevents the output from chattering when the switch contacts bounce. R2 and D1 (where $R2 \ll R1$) cause C1 to discharge quickly when the switch is released. This makes it possible for multiple switch closures in quick succession (faster than the auto-repeat rate) without altering the DBRT. The only restriction is that $R1 \ll R3$ to insure oscillation. □



THIS PHOTO-EVENT TIMER measures time with an accuracy of 0.1 switch, a minimal amount of circuitry.

R_4 . The quad NOR gate IC6, configured as a latch, initiates timing when switch S2 is pressed. A signal from the photocell stops the timing, which can be with either a dark-to-light or

light-to-dark transition depending upon the setting of S5. S3 offers access to a direct operating mode rather than through the latch.

Dividers IC3 and IC4 supply 0.1- or

1-s timing pulses that can be selected by S4. Timer IC7 signal conditions the pulses for a time-display counter. The counter should be a 12-Vdc unit drawing less than 200 mA. □

CIRCLE 526 MONITOR SUPPLIES Down To 0.6 V

MIKE JACHOWSKI

Precision Monolithics Inc., 1500 Space Park Dr., P.O. Box 58020,
Santa Clara, CA 95052; (408) 727-9222.

A simple circuit consisting of only a reference diode and a matched pnp transistor pair (the MAT-03) can be used to monitor low-voltage power rails, such as a +5-V logic supply. This is beneficial for microprocessor-based systems that use either battery-backed-up CMOS or EEPROM memory. The monitor prevents inadvertent writing to the memory as the rest of the digital circuitry turns off when a +5-V supply falls.

The problem with conventional comparators is that there's no guarantee what the device's output state will be once the +5-V supply falls below the comparator's own power requirements. Micropower op amps are occasionally used as comparators in these applications, but their response times usually aren't quick enough to protect the memory.

A circuit can be designed to supply a 700-ns response time and maintain an accurate output with a supply

voltage down to 0.6 V (see the figure). The circuit also enables the added flexibility to adjust the monitor trip point down to 1.25 V.

When V_{CC} falls between 0.6 V and V_{trip} , Q1's base-emitter junction becomes forward-biased so the collector can conduct current into R2, pulling the output high. As V_{CC} rises above 1.23 V, the reference diode (D1) stabilizes the voltage on the base of Q1, which sets the trip-point of the differential-pair comparator. The trip-point is reached when $(V_{CC} \times R4)/(R4+R5) = 1.23$ V. At this point, Q2 will turn on and Q1 will turn off. The output voltage then goes low, pulled down by R2. Resistor R6 supplies about 60 mV of hysteresis to guarantee clean transitions.

The comparator's output goes high as the power supply voltage

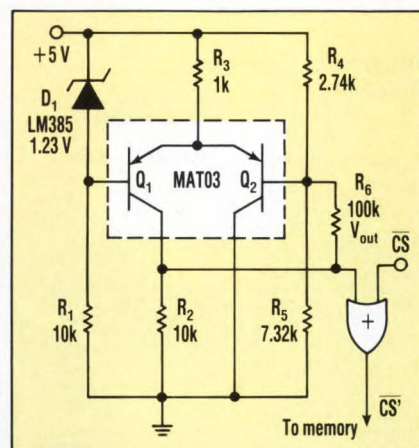
IDEAS FOR DESIGN

falls below the threshold voltage, which is arbitrarily set at 4.5. This forces the CMOS logic gate output high, disabling any write commands sent to memory while the voltage supply is low.

In this example, the comparator and logic gate were powered by the monitored +5-V supply, which shows that CS (Chip Select) remains disabled when supply voltages go as low as 0.6 V. In an application where memory has an independent battery back-up, however, both the logic gate and the comparator should be supplied by the memory's back-up voltage with only R4 connected to the supply rail. In this case, it may be preferable to lower the comparator's power consumption by increasing R1, R2, and R3 proportionally. Multiplying each of the three resistors by 10 will drop the supply current below 80 μ A.

The tradeoff for lowering the sup-

ply current is an increase in the comparator's response time. With the chosen circuit values, the comparator has a total CS-Disable response time of 700 ns for a step-supply volt-



A SIMPLE CIRCUIT can accurately detect a low supply voltage and disable inadvertent write operations to memory.

age change from 5 V to 3 V. About 600 of the 700 ns is due to RC time constants. Therefore, by multiplying the resistors by 10, the response time will slow to about 6 μ s.

Although this circuit supplies a high output when the trip point is reached, it's also possible to invert the circuit to deliver a low output upon crossing the threshold. Its operation is identical to the previous one, except that a matched npn transistor pair (the MAT-01) must now be used as the comparator. R1, R2, and R5 would then be connected to the +5-V monitored supply, while R3, R4, and D1 would be connected to ground. This produces an output which is low when V_{CC} falls between 0.6 V and V_{trip} , and an active high output when V_{CC} is greater than V_{trip} . This circuit creates a Reset signal for microprocessor systems if a power fault takes the +5-V supply below its specifications. \square



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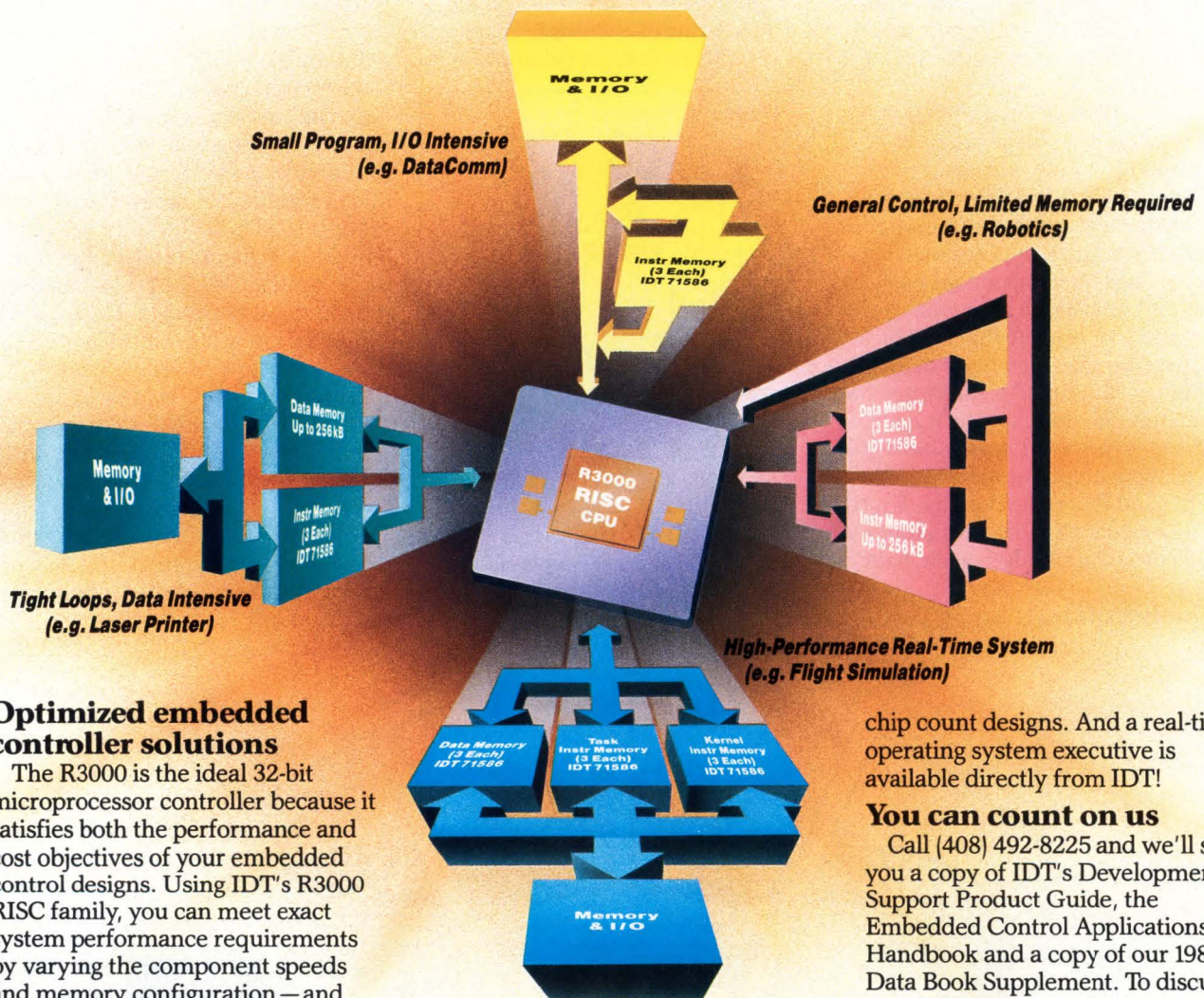
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The first commercially available VLSI component that's certified by Northern Telecom to support the T-Link rate-adaption protocol is the 89151 ISDN communication controller from Intel, Folsom, Calif. The device adapts non-ISDN applications—such as synchronous intelligent terminals as well as asynchronous machines like PCs and modems—to the ISDN. It eliminates the need for costly rate-adaption design schemes, which require numerous components. The controller also links with a wide variety of microprocessors for flexibility in selecting system architectures. In quantities of 500, the 89151 controller costs \$24. Call Kristen Bailey, (916) 351-2747. DM

CIRCLE 301

ENHANCED Z80 CPU PACKS 2-KBYTE RAM

By adding 2 kbytes of static RAM, a clock generator, and a timing controller to its Z80 CPU, Zilog Inc., Campbell, Calif., came up with a new chip: the Z84C50. With the on-chip static RAM, commonly used instructions and data can be held in the memory and executed quickly with no lost time for off-chip memory accesses. The CMOS chip executes the Z80 instruction set and can operate at clock frequencies of up to 10 MHz. In addition, the on-chip oscillator makes it possible for new power-down modes to lower power consumption to just a few milliwatts during standby. It also reduces the board space required by the processor. The chip comes in a 40-pin DIP, a 44-lead PLCC, and a 44-lead plastic quad-sided flat package. In quantities of 100, the 84C50 sells for \$6 to \$7. Delivery is from stock. Contact Jim Magill, (408) 370-8000. DB

CIRCLE 302

ENERGY-RATED MOSFETS REACH 1000 V AND 10 A

A trio of power MOSFETs from Motorola, Phoenix, brings avalanche energy and 40-V gate ratings to Motorola's high-voltage, high-current devices. These ratings allow for designs that are inherently more reliable because avalanche energy is specified, while the 40-V gate rating offers an extra margin of safety against high-voltage transients in the gate circuit. The first in the new line of energy rated FETs (E-FETs), the MTM10N100E, 24N50E, and 26N40E, are rated respectively at 1000, 500, and 400 V, with continuous currents of 10, 24, and 26 A. Their respective on-resistances are 1.2, 0.25, and 0.18 Ω . In addition, the speed of the FETs' internal body-drain diode approaches that of discrete, fast-recovery devices. All three are in TO-3 metal cans. In quantities of 100, the 10N100E goes for \$27.90 each; the 24N50E and 26N40E are \$25.38 each. Delivery is from stock. Call Jack Takesuye, (602) 244-4911. FG

CIRCLE 303

12-BIT CMOS M-DAC COMES IN 8-PIN DIP

From Maxim Integrated Products, Sunnyvale, Calif., you can now get a 12-bit monotonic—and accurate—MDAC (multiplying d-a converter) with current output in a tiny 8-pin plastic miniDIP or a 16-pin, wide-SOIC. Moreover, the MAX543 IC meets monotonicity and accuracy specifications over all temperature ranges. It's updated over a three-wire serial interface (one wire each for data, clock, and load) by a host processor. The interface has several advantages over the typical parallel approach: Fewer interface lines keeps bus noise out of the d-a converter's output and the serial bus can be inactive when it's not updating the converter. Furthermore, the serial interface simplifies applications in need of voltage isolation through opto isolators. The converter comes in two performance grades as well as commercial, industrial (extended), and military temperature ranges. In quantities of 100, prices start at \$8.50 each. Call Roy Selinger, (408) 737-7600. FG

CIRCLE 304

MODEM-IC SET SUPPORTS V.42 ERROR CONTROL

Major support of the CCITT V.42 point-to-point error-control standard has arrived in the form of the first complete V.42 IC set for 2400-bps modems. The three-chip set from Silicon Systems, Tustin, Calif., is the first offspring of the technology partnership between Silicon Systems and Hayes Microcomputer Products, Atlanta. The set is also the first from any manufacturer to incorporate CCITT V.42 and Hayes' standard AT command set, in addition to Hayes' AutoSync, adaptive data compression, and automatic feature negotiation. The V.42 standard offers backward compatibility with the installed base of Microcom Network Protocol (MNP) modems through the alternate protocol. Samples of the set will be available by November, with full production scheduled by 1990. In quantities of 100, the set will cost \$52. Call Fred Kamp at Silicon Systems, (714) 731-7110, ext. 3202; or Jane Dryden at Hayes Microcomputer Products, (404) 449-8791. DM

CIRCLE 305

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DAVE BURSKY

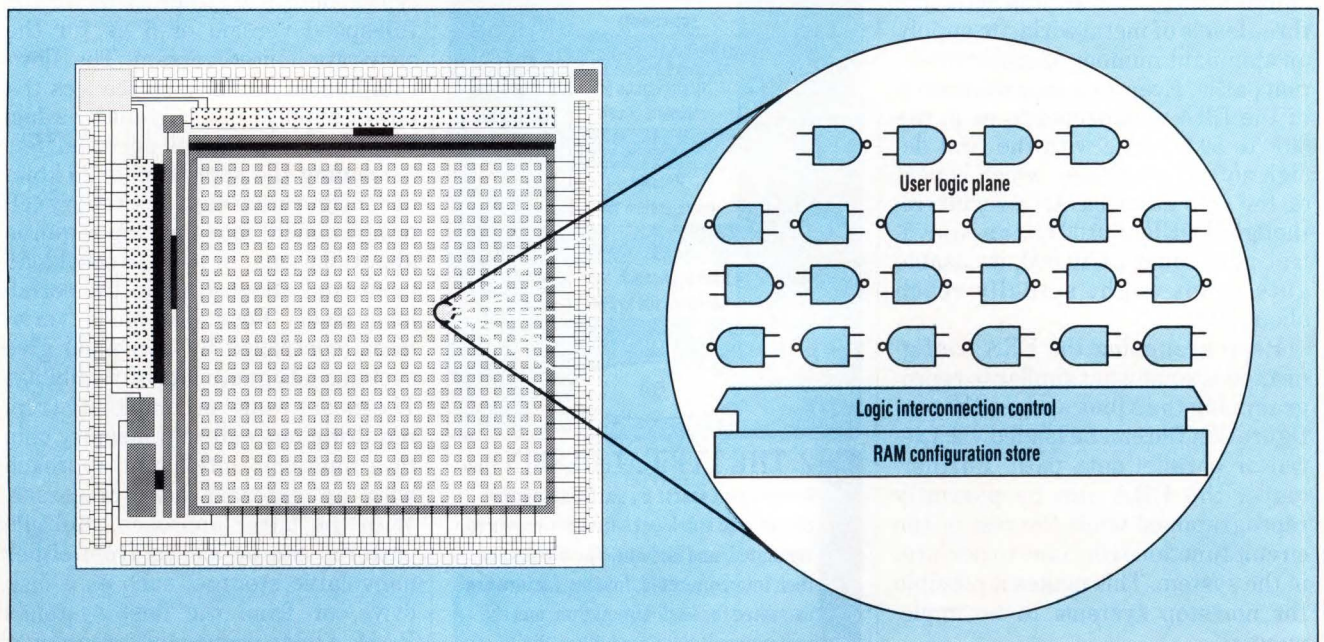
Since its introduction three years ago, RAM-based programmable logic has given designers the ability to reconfigure the logic in their system at any point during the system's operation. And, with the release of the Plessey ERA60K family of electrically reconfigurable arrays, the Xilinx Inc. LCA family will face its first major challenge from another family of RAM-based programmable logic chips. Such circuits are the only in-system reconfigurable alternative to mask-programmed gate arrays, or EPROM or fuse-based logic chips.

The first member of Plessey's CMOS array family, the ERA60100,

features densities of about 10,000 equivalent gates. Future family members will extend the gate count in both directions, from a low of 2000 to a high of 40,000 equivalent gates.

The ERA chips will use simple two-input NAND gates as the basic logic element, unlike the Xilinx chips, which are based on an array of complex macrocells called configurable logic blocks. The small size of the logic element in the ERA chip makes it possible for available logic to be used more efficiently, according to Ian Phillips, engineering manager at the company's Roborough, UK facility. He explains that in most programmable logic chips, many gates go unused when only part of the macrocell is configured. The remaining gates can't usually be reassigned to another logic function.

But in the ERA, each gate can be



1. WITH 2-INPUT NAND GATES as the basic logic element, Plessey's electrically reconfigurable array family gives designers gate-array flexibility with the alterability of static-RAM control cells.

PROGRAMMABLE GATE ARRAY

independently interconnected by storing values in the RAM cells, which switch the gate's input connections to a series of predefined interconnection paths. Moreover, because each gate is independent of the next, recursive (multilevel) logic can easily be configured. These gates are flexible and they can implement high-performance circuits—the basic gates have typical loaded delays of 2.5 ns, and a D-type flip-flop can typically operate at 200 MHz.

To facilitate circuit design, two cell libraries—one containing basic building blocks, and the other with higher-complexity macrocells—supply familiar TTL and CMOS circuit equivalents. All of the library's cells are defined through the physical layout level, and, consequently, they offer consistent performance from one design to the next. Designers can also create their own hard macrocells and add them to the library. The cells in the ERA library are actually a subset of the cells in the Plessey CLA60K family of 1.4- μ m sea-of-gates arrays. Consequently, once a design is locked in, the circuit can easily migrate to a mask-programmed gate array if volume manufacturing is needed.

To achieve a high degree of interconnectivity, the arrays will use three levels of metal wiring to supply an abundant number of interconnection paths. Even so, array utilization of the ERA is expected to be in the 30% to 50% range with the first design software release, which is part of the chip support. As a result, although the ERA60100 has an equivalent gate count of 10,000, its usable gate count might actually reach about 5000.

Reprogramming the ERA configuration is somewhat similar to reprogramming the Xilinx array—the configuration file can be loaded via a serial or parallel data path. Furthermore, the ERA can be partially reprogrammed while the rest of the circuit functions continue to perform in the system. This makes it possible for non-stop systems to be implemented.

In contrast, when reprogramming the Xilinx arrays, all configuration

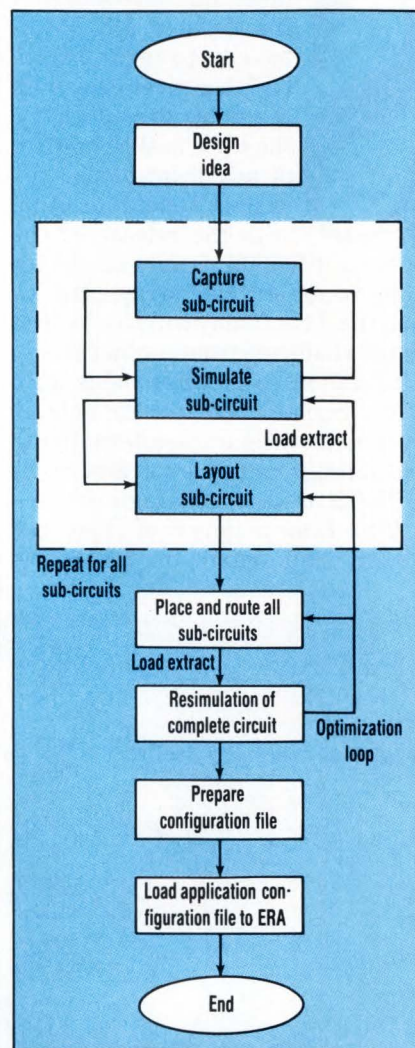
bits must be loaded into the chip, which in turn forces the subsystem where the chip resides to momentarily stop. The dynamic reconfigurability aspect of the ERA is initially set up by the automatic router, which comes with design toolkit. During the circuit design, portions of the array can be set aside for logic that will be occasionally altered.

One futuristic application might have the ERA chip reconfigure itself under intelligent control. The recon-

figuration could bypass flaws detected in either the ERA or in a section of the subsystem. Some type of system self-test program would initially be run to determine if a problem existed and in turn would send any such data to the intelligent controller. The controller would then determine the new pattern that must be loaded into the ERA. Additional applications span fields from simple glue-logic replacement to more complex needs, such as digital signal processing, neural networks, secure logic, and system simulation.

The ERA60100 consists of a central logic core containing about 10,000 gates that are set up as an array of 2500 cells, and a periphery of 84 I/O cells, each of which can be programmed into several configurations (*Fig. 1*). Each logic cell is configured with 10 bits of RAM and each I/O cell requires 4 bits to set its configuration. The circuit, operating from a 5-V supply, will come in a 120-lead, pin-grid-array package to accommodate the I/O lines, the dedicated control pins, and the multiple power supply and ground lines. Individual gates draw about 10 nA in the standby state and about 10 μ A/MHz when active. Output buffers can handle loads of up to 12 mA and have typical delays of either 2.5 ns for the full-speed version or 5 ns for the slow-rate-limited version. The slow-rate-limited buffer also reduces the power supply peak current by a factor of four over the full-speed buffer.

Loading the approximate 25 kbits of configuration data (with every cell programmed) into the chip requires about 0.5 ms in the parallel-load mode and about 4 ms in the serial-load mode. Four load-mode variations (controlled by two pins) give systems designers lots of flexibility. The modes range in complexity from requiring one external memory chip to a multichip intelligent approach with an external host processor. With the latter approach, multiple patterns can be loaded from either nonvolatile storage, such as a disk drive, or from the host system's RAM. And to ensure the integrity of the RAM configuration bits, the ERA packs cyclic redundancy check-



2. THE TYPICAL DESIGN flow for a circuit starts by partitioning the circuit into sub-blocks that are captured, simulated, and laid out. The blocks are then interconnected, loading factors are extracted for back-annotation, and the entire circuit simulated. Then the configuration file is extracted from the final net list.

PROGRAMMABLE GATE ARRAY

PRICE AND AVAILABILITY

The ERA60100 will come in a 120-lead pin-grid array package and will sell for \$225 in quantities of 100. Samples will be available next January. Versions will be available with commercial, industrial, and military-operating temperature ranges. A lower-cost version with fewer I/O lines but the same number of gates will be available in an 84-lead plastic leaded chip carrier later in the first quarter of 1990.

Plessey Semiconductors, Sequoia Research Park, 1500 Green Hills Rd., Scotts Valley, CA 95066; Steve Brightfield, (408) 438-2900. **CIRCLE 511**

ing circuitry, which tests the bits as part of a diagnostic self-test mode invoked by users.

Like the Xilinx arrays, the ERA uses a simple serial-data load mode to minimize pin usage, and a parallel data-load capability. The ERA can also be partially configured upon startup to implement an RS-232-compatible serial port. It then could load the remaining portion of the chip pattern through the serial port.

On-chip circuits enable the configuration data to be loaded automatically from an external ROM, EEPROM, or EPROM, or from a system disk under the control of a host processor. In either case, eight of the I/O pins (DX_{0-7}) are used during configuration to load the pattern into the chip. And, when a non-volatile memory is used to hold the data, another 16 lines (AX_{0-15}) supply the addresses to read the data from external memory. After chip configuration, pins DX_{0-7} and AX_{0-15} can be used as inputs or outputs as defined by the configuration pattern. Similarly, the pins used to form the simple serial data port can be put into service as user I/O lines after the configuration file is loaded.

The chip's logic cells contain some local interconnection capability to simplify routing, and many larger functions can thus be assembled without any routing overhead. Those larger functions, however,

will have to be connected to other blocks that may be located at a distance. Consequently, some logic cells will be lost during the longer routes. An important feature was added to counter that problem—a reconfigurable 10-line data bus that surrounds the core cell array just inside the I/O pad ring. With the bus, long-distance connections can skirt around the cells rather than use them. An equally attractive use for the bus would make it possible for users to route external signals to fixed I/O pad locations—this would make the signal readily available to any portion of the array core.

Developing circuits with ERA chips is similar to the process that develops a circuit for a gate array. The tools available for engineers to start a design include the ViewLogic schematic-capture and simulation software combined with a library of basic cells and macrocells, which are supplied by Plessey. Added to that combination is an autorouter that interconnects the cells, and a back-end simulator that verifies the entire circuit. The tools are available for either 80386-based IBM PCs or compatibles, with versions for the DEC Vax family and Sun-compatible computers coming soon.

In a typical development cycle, designers would first set up a hierarchy and then partition the design into a number of subcircuits that can be captured, simulated, laid out, and routed (*Fig. 2*). When all the modules are completed and interconnected, the circuit "track loads" are extracted and the final circuit simulation is performed. After final simulation, the net list is extracted and a configuration file is created. This file can be stored on disk or in a nonvolatile memory, or it can be loaded directly into the ERA chip. Designers can even download a configuration file for a block into the ERA chip, and then use the chip to emulate itself during development. □

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SPEECH SYNTHESIS CHIPS YIELD TAPE- QUALITY SOUND

SYNTHESIZERS SPAN
LOW-END TO
HIGH-END SPEECH
APPLICATIONS.

DAVE BURSKY

Speech synthesis chips have been around for over a decade, yet most of these chips are developed for toys, games, and low-end commercial applications where low cost is the overriding concern. A market is emerging, however, for high-quality speech synthesis. On the consumer side, this new market runs the gamut from digital message storage for phone answering machines to talking greeting cards. On the industrial side, applications cover the spectrum from telecommunications to banking systems.

To meet the expected market, Oki Semiconductor developed its MSM637X family of high-quality speech synthesis and voice recording/playback circuits. The chips deliver the most natural-sounding speech. Their features give system designers more options than ever.

To produce the natural-sounding speech, the Oki synthesizers employ higher-precision (12-bit) digital-to-analog converters, higher than any of the other company's chips. Most other chips only use 8-bit d-a converters. The higher-precision d-a converters, coupled with 4-bit straight adaptive-differential pulse-code modulation (ADPCM) makes it difficult to distinguish between a live voice and the synthesized outputs of the Oki chips.

There are actually several circuit subfamilies within the overall family. In one group there are four chips—the MSM6373, 6374, 6375, and 6376—which are ROM-based synthesizers that respectively store 256 kbits, 512 kbits, 1 Mbit, and no on-chip memory because the circuit addresses off-chip storage.

Another family that initially had just one member—the MSM6378RS—will have on-chip, one-time programmable storage based on UV EPROM technology. It will offer a different set of features than the previous quartet. The 6378 packs 256 kbits of one-time programmable EPROM (the one-time limit comes from the low-cost plastic windowless package that houses the chip). Larger EPROMs will be incorporated on the chip for future family members. Offering the dual capability of capturing live speech and then playing it back, a voice-recorder chip (the MSM6388) will also be added to the family.

The large on-chip ROMs for the first three members of the first family make possible playback times of 10, 20, and 40 seconds for the 6373, 74, and 75, respectively (when the speech is sampled at 6.4 kHz); the fourth chip has an unlimited playback range because it can pull what it needs from an up-to-2-Mbyte external memory. Because no address lines are needed for the ROM versions, the chips can be housed in low-cost, 18-lead plastic DIPs. The chips consume little current—typically about 4 mA when operating and approximately 1 μ A in standby.

To some extent, each of the playback times categorize the application classes each chip might handle best. For instance, the shortest time (smallest ROM) suits alarm systems, arcade games, toys, cars, vending machines, and other short-duration needs. The mid-size ROM ver-

HIGH-QUALITY SPEECH SYNTHESIZERS

sion could find homes in talking clocks, time stamps for answering machines, appliance-programming confirmation, and so forth. The largest-ROM version might serve the high-end of the previous cases or go into annunciators in elevators or appliance instruction presentations.

The MSM6373 through 6376 can address up to 110 phrases and can run at sampling frequencies from 4 to 32 kHz, depending on the desired speech quality. A separate 4096-bit address ROM, included on all the chips, holds the address-mapping sequence in which the 110 phrases (or sounds) are reproduced (*see the figure*). Two playback channels make it possible for two phrases to be played simultaneously (such as speech and background music). In addition, by using the on-chip four-step delay setting, an echo or reverberation effect can be set up. Each channel's volume can be set at one of three levels, starting with the normal volume and then incrementally decreasing from that point.

Moreover, the synthesizers have two "beep" tones—1 kHz and 2 kHz—built in so that if time or end-of-message markers are needed, the available ROM space won't have to be used. Several variations of the beep tones will generate a sum total

PRICE AND AVAILABILITY

Prices for the ROM-based MSM6373, 6374, and 6375 speech-synthesis chips are \$5.23, \$7.93, and \$11.16, respectively, in 10,000-unit quantities. The ROM-less MSM6376 comes in a 64-lead, quad-sided flat package and sells for \$18 in single-unit quantities. In 1000-unit lots, the one-time programmable MSM6378 sells for \$10.52. The MSM6388 recorder chip and the MSM6322 pitch-control circuit sell for \$7.62 and \$6.59, respectively, in similar quantities. Prices for the serial storage registers aren't set.

Oki Semiconductor, 785 N. Mary Ave., Sunnyvale, CA 94086-2909; Charu Mungale, (408) 720-1900. **CIRCLE 513**

of eight options.

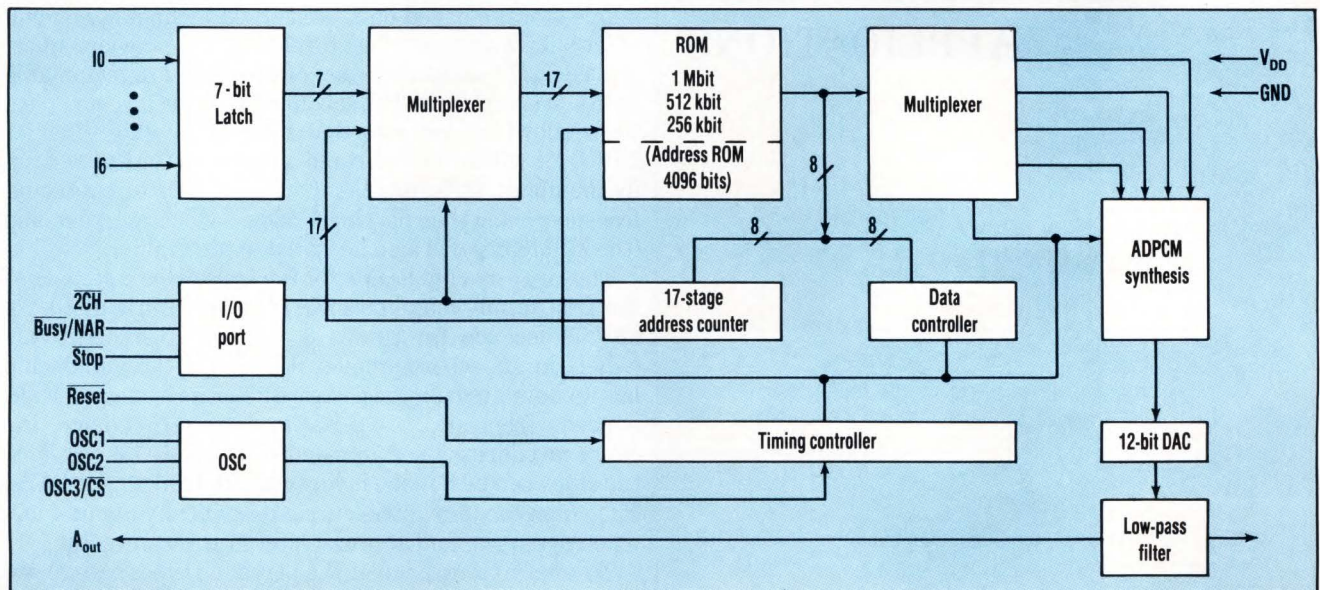
Not only do the chips deliver higher quality speech, but they also simplify system design by incorporating the output low-pass filter to smooth the signal from the d-a converter. The filter has an attenuation of 24 dB/octave. It tracks the signal in conjunction with the chip's clock frequency to ensure audio quality if the clock should drift or be intentionally changed. With a mask option, the

low-pass filter can also be bypassed if an external filter is used.

Offering a different type of flexibility and filed programmability, the 6378 has the same basic synthesizer, d-a converter, and low-pass filter. But it's designed to play one phrase, either in a one-shot or endless-loop playback mode. The 256 kbits of one-time-programmable memory on the chip make it possible for a maximum playback time of 15.6 seconds when the sampling frequency is 4 kHz (8 seconds at 8 kHz). Housed in a low-cost, 16-lead plastic DIP, the circuit has some interesting potential applications, such as in-store customized greeting cards, talking sales tags, and so forth.

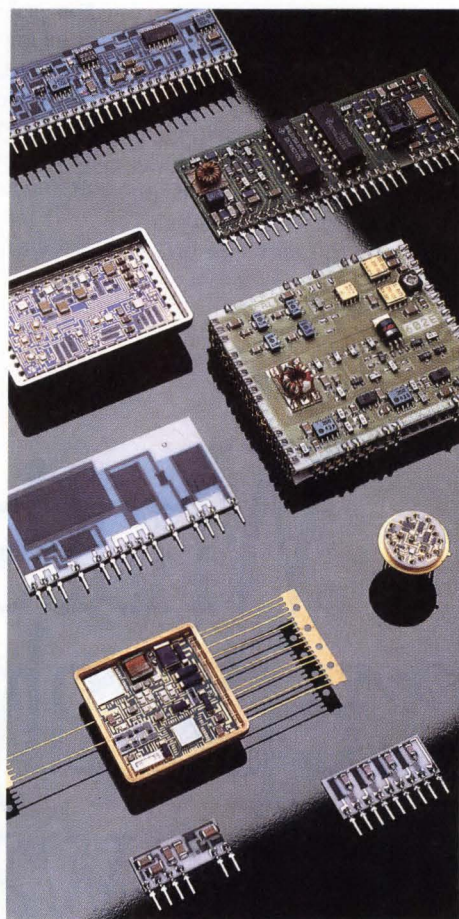
The most complex chip in the synthesizer family is the MSM6388GS-V1K ADPCM voice processor, which comes in a 44-lead, quad-sided flat package. This chip contains an input a-d converter with 12-bit resolution, an output 12-bit d-a converter, the ADPCM analysis and synthesis circuits, a microphone preamplifier, and a fourth-order, low-pass filter for both input and output lines.

Intended to operate either in standalone or CPU-hosted modes, the chip can capture up to eight channels of audio data and can store the digitized sound in special off-chip dy-



THE LATEST ROM-BASED speech-synthesis chips from Oki Semiconductor offer the most realistic-sounding audio reproduction, thanks to a 12-bit d-a converter and a built-in, low-pass filter on the output. Up to 110 phrases can be sequenced by an on-chip, 4096-bit address ROM that supplements the audio data ROM.

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HIGH-QUALITY SPEECH SYNTHESIZERS

namic serial registers. The serial storage is partitioned into as many as eight blocks, depending on the state of the chip's two Register Select lines and the number of 1-Mbit serial registers connected to the chip (up to four registers per bank). Audio sampling can be done at any frequency from 3.5 to 9.1 kHz. With 4 Mbits of off-chip memory, up to 262 seconds of speech can be stored at 4 kHz. When used in its CPU mode, the 6388 can serve as a development tool for the other speech-synthesis circuits offered by Oki (except for the new ROM-based 6373 series, which uses packetized PCM).

The MSM514201JS, a dedicated 1-Mbit serial register, supplies the off-chip storage. It has a serial access time of 3 μ s and a serial read-write access time of 4 μ s. It also includes internal self-refresh circuitry to ensure data integrity. Organized as 1-Mword-by-1-bit, the chip can access

all of its locations easily because one line enables the chip to either increment or decrement the address counter. A low-power memory, the chip has a 4-V data-retention mode that drops supply current to 0.1 mA when in standby; when it's active, current increases to about 5 mA.

One last chip that's part of the family, but not a speech synthesis circuit, is the MSM6322GS-K voice-pitch controller. This chip performs real-time voice-pitch alteration, with an upper and lower octave span of eight steps each. On-chip are an 8-bit a-d converter, a 9-bit d-a converter, the microphone preamplifier, and the output low-pass filters needed to handle the signal manipulation. This circuit can be used with the voice-synthesizer chips or in other applications, such as high-speed audio-tape sound adjustment, toys, and games.

To ease the development of digitized speech to be stored in various

ROM or EPROM regions, Oki created several tools. One is a small desktop speech programmer called the Anawriter 6378 Mark II. The system comes with a microphone, a second input for prerecorded material, a bargraph light-emitting diode display to monitor the input signal, a multifunction display for various operator feedback messages, and an EPROM programmer. Evaluation and demonstration boards are also available for the 6373 series, as well as for the 6388. The ROM-less 6376 can be used in an evaluation system for ROM-based chips to facilitate code-tuning by either Oki or the user with an analysis package that was developed by Oki. □

HOW VALUABLE?

HIGHLY

MODERATELY

SLIGHTLY

CIRCLE

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557

558

What's more paralyzing is the way he gets treated.



The hardest part about having a disability is being constantly reminded that you have one. Sometimes that happens when people stare at you. Or point at you. Or don't even think of including you in every day activities. Maybe it's time to start treating people with disabilities like people.



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The new LMS Series of remotely programmable power supplies provide modular solutions for wide range voltage applications from 0-120VDC. Equipment for test applications require wide range outputs to increase versatility and allow for changing test requirements. Deliverable test equipment, designed for use with a specific system can now have increased flexibility to reduce the cost of subsequent systems. In-house test equipment using the LMS Series can now be designed for a wide range of applications, to allow versatility and increased utilization of capital equipment expenditures.

The Lambda LMS Series is ideal for all types of test equipment. With 25 wide range output models to choose from, output voltages up to 120VDC, up to 800W, can be selected. As most of these units are half the size of industry equivalents, the test rack can be significantly

reduced while maintaining and increasing operational features within the system. Built-in user adjustable overvoltage protection, constant voltage/constant current operation, and a universally accepted user selectable 110/220 input make these units ideal for test applications worldwide. Standard output control mechanisms can be achieved by: manual control via multiturn potentiometer; remotely programmed by an analog signal in either the voltage or current mode; or, for more sophisticated ATE applications, IEEE-488 control.

The LMS Series is compatible with Lambda's IEEE-488 ATE Series Power Systems. To reduce cost, these modular power supplies exclude output metering. If voltage and current meters are required, Lambda's new LLS Series will meet the exact need.

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- Power density of 2W/in³ for zero-up wide range models.
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- Overvoltage/overtemperature indicators.
- Compatible with Lambda's ATE Series Programmable Power Systems.
- Universal operation at 110/220 VAC.
- Worldwide safety agency approvals.
- 3750VAC input to output isolation.
- Remote on/off (TTL), remote sense and remote program capabilities (current and voltage).
- Input surge protection per IEEE-587 for branch circuits and outlets (Class C).
- Standardly operates in parallel and series with like units.

	MAX CURRENT AT OPERATING TEMPERATURE OF				DIMENSIONS (inches)	QTY. 1	PRICE QTY. 10	QTY. 25	MODEL
	40°C	50°C	60°C	71°C					
0-8 VOLTS	3.50	2.90	1.75	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 8	\$ 263	\$ 250	\$ 245	LMS-3008
	5.00	4.30	3.20	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 9	390	370	360	LMS-4008
	10.00	7.90	6.30	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 10	462	440	425	LMS-5008
	20.00	20.00	16.50	13.5	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 11	620	590	570	LMS-6008
	100.00	90.00	78.00	57.0	4 ⁹ / ₃₂ × 8 × 11 ⁷ / ₈	1176	1120	1080	LMS-9008
0-18 VOLTS	1.60	1.30	0.80	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 8	263	250	245	LMS-3018
	2.40	2.10	1.50	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 9	390	370	360	LMS-4018
	4.50	3.50	2.80	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 10	462	440	425	LMS-5018
	9.00	9.00	8.20	6.6	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 11	620	590	570	LMS-6018
	45.00	40.00	33.00	25.0	4 ⁹ / ₃₂ × 8 × 11 ⁷ / ₈	1176	1120	1080	LMS-9018
0-40 VOLTS	0.70	0.60	0.35	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 8	263	250	245	LMS-3040
	1.00	1.00	0.85	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 9	390	370	360	LMS-4040
	2.00	1.60	1.30	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 10	462	440	425	LMS-5040
	4.00	4.00	3.80	3.1	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 11	620	590	570	LMS-6040
	20.00	18.00	15.00	11.0	4 ⁹ / ₃₂ × 8 × 11 ⁷ / ₈	1176	1120	1080	LMS-9040
0-60 VOLTS	0.50	0.42	0.25	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 8	263	250	245	LMS-3060
	0.70	0.70	0.60	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 9	390	370	360	LMS-4060
	1.40	1.10	0.90	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 10	462	440	425	LMS-5060
	2.80	2.80	2.60	2.1	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 11	620	590	570	LMS-6060
	14.00	12.00	10.00	8.0	4 ⁹ / ₃₂ × 8 × 11 ⁷ / ₈	1176	1120	1080	LMS-9060
0-120 VOLTS	0.25	0.21	0.13	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 8	263	250	245	LMS-3120
	0.36	0.36	0.30	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 9	390	370	360	LMS-4120
	0.70	0.55	0.45	—	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 10	462	440	425	LMS-5120
	1.40	1.40	1.30	1.0	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 11	620	590	570	LMS-6120
	7.00	6.00	5.00	4.0	4 ⁹ / ₃₂ × 8 × 11 ⁷ / ₈	1176	1120	1080	LMS-9120

LMS SERIES

Specifications

DC OUTPUT

Voltage range shown in table.

REGULATED VOLTAGE CONSTANT

regulation, line	0.05% for line variations from 85 to 132VAC or 170 to 265VAC. 0.01% + 1mV for LMS-3000.
regulation, load	0.05% for load variations from 0 to full load. 0.01% + 1mV on LMS-3000 Series.
remote programming resistance	customer adjustable from 200Ω/V to 1000Ω/V. (200Ω/V on LMS-3008 through LMS-3060. 400Ω/V on LMS-3120.)
remote programming voltage	volt per volt or 0-5 volt signal for zero to full voltage out, customer selectable.
ripple and noise	1mV RMS, 5mV pk-pk on all LMS-3000 models. 5mV RMS, 35mV pk-pk on 8V and 18V models. 10mV RMS, 75mV pk-pk on 40V and 60V models. 20mV RMS, 150mV pk-pk on 120V models.
temperature coefficient	0.03%/°C. (0.01%/°C on LMS-3000 Series.)

CONSTANT CURRENT

(Current regulated line and load) Automatic Crossover.	
current range	5% to full load current. (1% for LMS-3000)
regulation, line	0.3% of I _o (max) for line variations from 85 to 132VAC or 170 to 265VAC. 2.5mA or 0.1% (whichever is greater) on LMS-3000 models. 2.5mA or 0.3% (whichever is greater) on LMS-4000 models.
regulation, load	0.3% of I _o (max) for load variations from short circuit to rated DC voltage. 2.5mA or 0.1% (whichever is greater) on LMS-3000 models. 2.5mA or 0.3% (whichever is greater) on LMS-4000 models.
current ripple	1% I _o (max) RMS.
remote programming current	0-5 Volt signal for zero to I _o (max).

AC INPUT

line	85 to 132VAC or 170 to 265VAC, user selectable.
power	LMS-3000 Series: 62 watts max. LMS-4000 Series: 79 watts max. LMS-5000 Series: 135 watts max. LMS-6000 Series: 245 watts max. LMS-9000 Series: 1100 watts max.
RMS current	LMS-3000 Series: 1.2A RMS max. LMS-4000 Series: 1.35A RMS max. LMS-5000 Series: 2.7A RMS max. LMS-6000 Series: 4.2A RMS max. LMS-9000 Series: 17.5A RMS max.

EFFICIENCY

Model	Minimum Efficiency at Max P _{out}
LMS-3000	45%
LMS-4008, 4018	55%
LMS-4040, 4060, 4120, 5008, 5018	60%
LMS-5040, 5060, 5120, 6008, 6018	65%
LMS-6040, 6060, 6120	70%
LMS-9008	72.5%
LMS-9018, 9040	75%
LMS-9060, 9120	77.5%

OPERATING TEMPERATURE RANGE

Continuous duty from 0°C to +71°C with appropriate deratings from 40°C to 71°C (0°C to 0 + 60°C for LMS-3000, 4000 and 5000).

STORAGE TEMPERATURE RANGE

-55°C to +85°C.

OVERLOAD PROTECTION

THERMAL

Internal temperature sensing circuit protects unit from excessive ambient temperature on the LMS-3000, 4000 and 5000 Series. The LMS-6000 and LMS-9000 Series are protected from inadequate air velocity by an internal airflow sensing circuit. When shutdown occurs, a rear panel LED indicator will turn on. AC power must be momentarily removed from the unit after thermal shutdown in order to restore operation.

ELECTRICAL

External overload protection — adjustable, automatic electronic current-limiting circuit limits output current to preset value. Current-limiting setability to 100% of rated current via front panel adjust. In addition an internal peak inverter current limit circuit protects the power supply during load transients.

OVERVOLTAGE PROTECTION

Built-in, adjustable overvoltage protection is standard on all sets. When pre-set voltage is exceeded, the overvoltage protector removes the inverter drive. AC power must be momentarily removed from unit after overvoltage shutdown in order to restore operation. Trip point is set by screwdriver adjust.

Overvoltage Protection Adjustable Ranges

Model	Vov(Min)	Vov(Max)
LMS-3008, 4008, 5008, 6008, 9008	4V	11V
LMS-3018, 4018, 5018, 6018, 9018	4V	24V
LMS-3040, 4040, 5040, 6040, 9040	8V	50V
LMS-3060, 4060, 5060, 6060, 9060	8V	70V
LMS-3120, 4120, 5120, 6120, 9120	20V	130V

IN-RUSH CURRENT LIMITING

Limits in-rush current at turn-on to 20A on LMS-6000 and LMS-9000 Series, 90A on LMS-3000 Series, 20A on LMS-4000 and 5000 when connected for 110VAC input and 40A when connected for 220VAC input.

COOLING

The LMS-3000, 4000 and 5000 are convection cooled. The LMS-6000 and LMS-9000 are fan cooled. Leave adequate clearance for air intakes and exhausts.

CONTROLS

DC OUTPUT CONTROLS

Simple screwdriver adjustment over the entire voltage range.

EMI

All units will meet FCC 20780 Class A and VDE 0871 Class A.

INPUT AND OUTPUT CONNECTIONS

Input connections via an IEC power line connector. DC output connectors via heavy duty, PC board mounted barrier strips (threaded bus bars on LMS-9008 and LMS-9018 units). (AC mating connector available, consult factory.)

LED STATUS INDICATOR

Overvoltage or overtemperature indicator on rear panel.

REMOTE SENSING

Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.

REMOTE ON/OFF

A TTL low or short enables the unit. A TTL high or open circuit turns the unit off.

PHYSICAL DATA

Package Model	Weight		Size Inches
	Lbs. Net	Lbs. Ship	
LMS-3000	6	7	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 8
LMS-4000	4.5	5.5	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 9
LMS-5000	7	8	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 10
LMS-6000	7.25	8	4 ⁹ / ₃₂ × 3 ¹³ / ₁₆ × 11
LMS-9000	14.5	19	4 ⁹ / ₃₂ × 8 × 11 ⁷ / ₈

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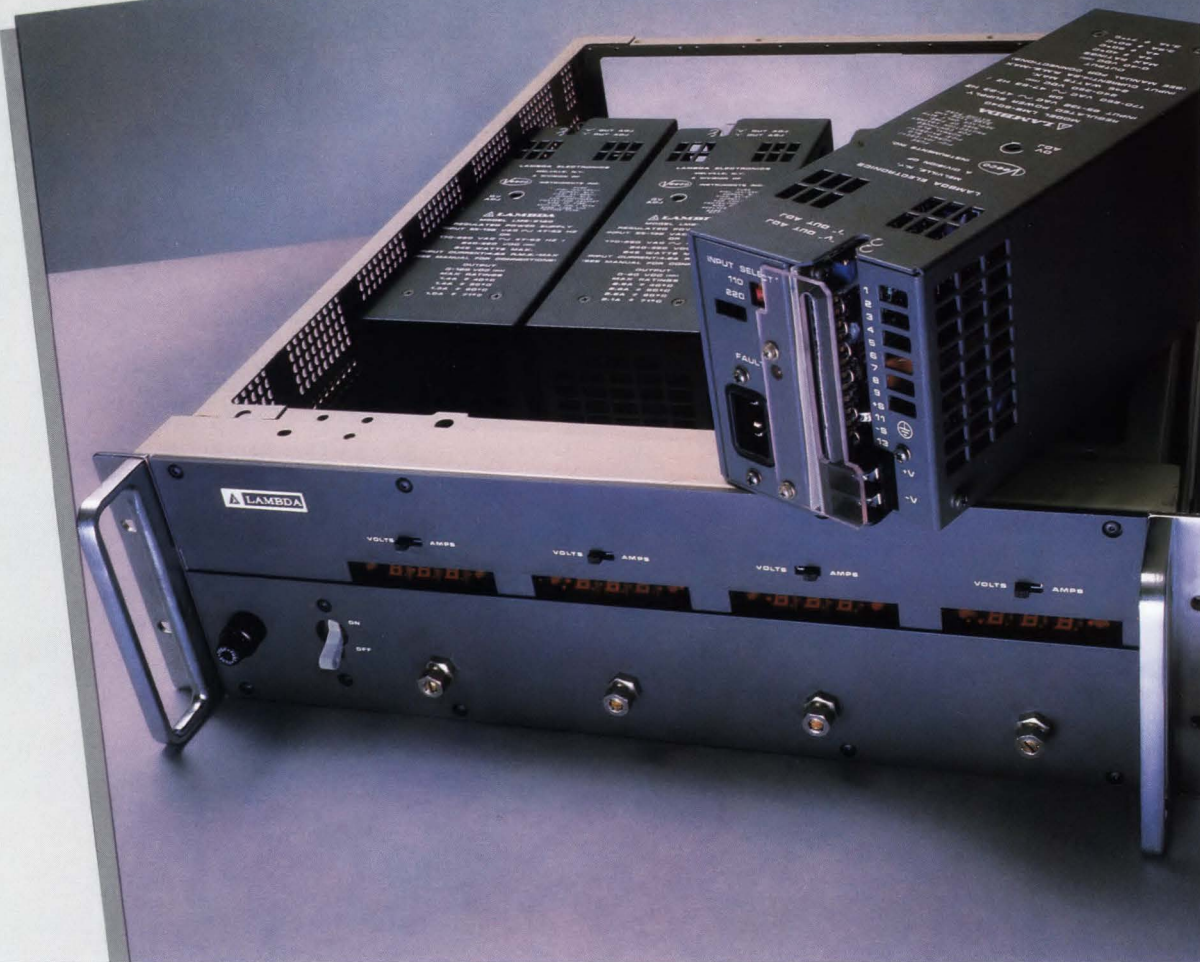
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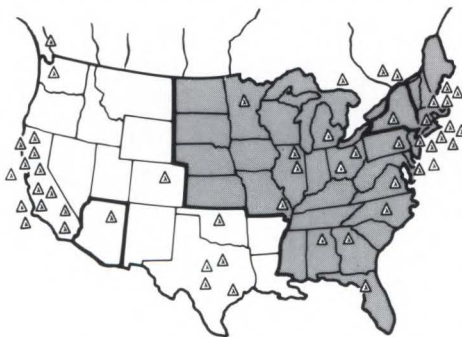
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CACHE CONTROL CHIP SIMPLIFIES SYSTEM DESIGN.

CACHE CONTROLLER SPEEDS ACCESSSES, ENHANCES SYSTEMS

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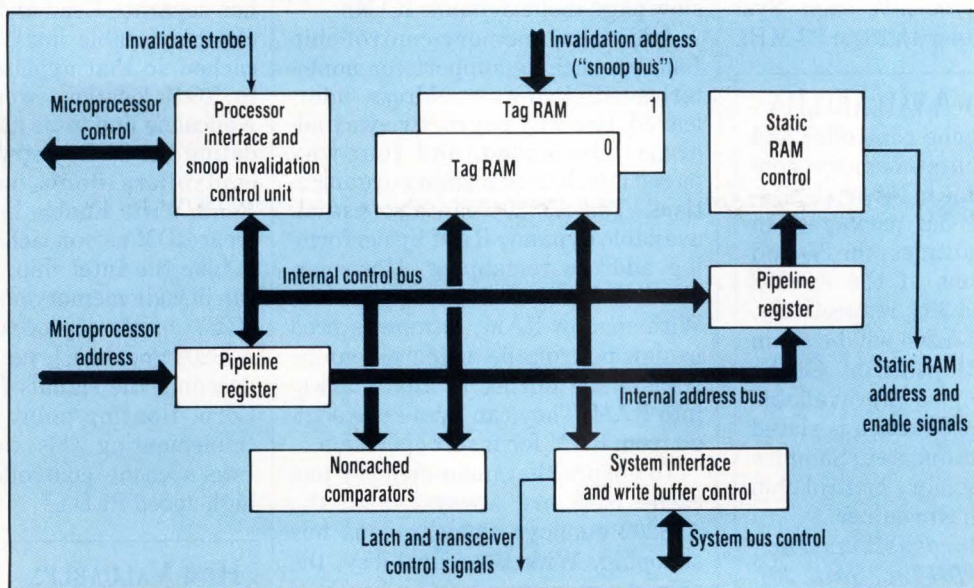
The old adage "there's more than one way to skin a cat" seems to apply to cache subsystem design: The number of options to improve system performance and capabilities are endless. Although Intel Corp. tried to standardize the cache-control aspects of 80386 systems by developing the 82385, other companies have found ways to improve functionality and system performance. The A38202 cache-controller chip and its companion A38204 burst-mode dy-

namic memory controller, both developed by Austek, are the latest and most feature-laden, cache-support chips to date.

The chips add many features and capabilities to the cache subsystem. Previously, to embed as many features, designers had to add a number of high-speed programmable logic chips, or the features just couldn't be implemented efficiently. The controller chip boosts the amount of addressable cache to 128 kbytes—four times that of Intel Corp.'s controller, and it can be programmed

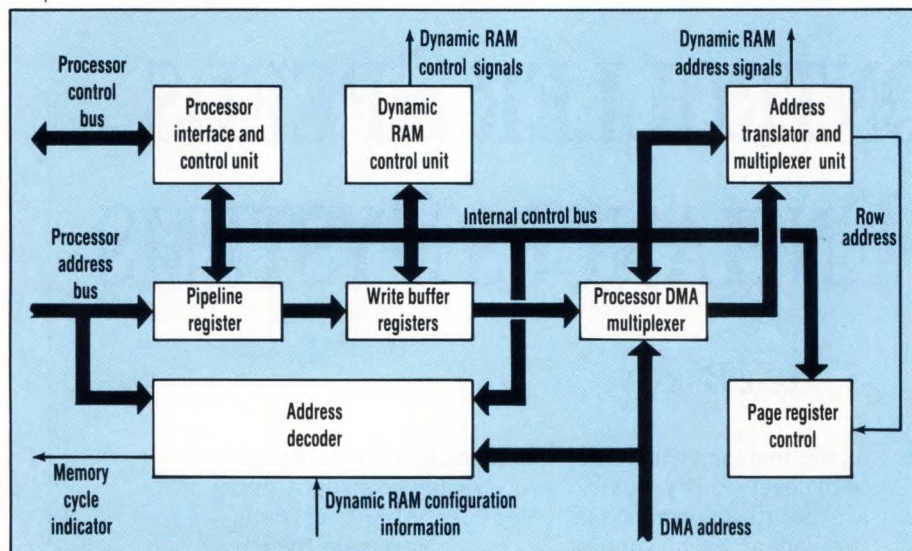
to turn up to three sections of the address space into noncacheable regions (*Fig. 1*). Moreover, the circuit has control lines that burst data into the cache under the direction of the companion A38204.

Applying the burst mode reduces the time penalty associated with a cache miss by shortening the time required to refill a line in the cache. For example, with one-wait-state memory and 16-byte subblocks, a cache miss adds an 11 wait-state penalty to the memory access without the burst mode be-



1. THE A38202 CACHE CONTROLLER can set aside up to three regions of memory as noncacheable and can perform asynchronous bus snooping. The controller can also address up to 128 kbytes of fast static RAM—four times the range of the original Intel control chip.

ADVANCED CACHE CONTROLLER



2. SUPPORT FOR THE A38202 cache controller's memory-burst mode makes it possible for the A38204 memory controller to reduce the penalty for refilling the cache line after a cache miss occurs. The A38204 also supports various interleaving options, programmable wait states, address remapping, and other features.

tween main memory and the cache to load in a new line. With the burst mode, the penalty drops to just five wait states.

The burst-mode interface on the cache-control chip ties directly into the companion A38204 burst-mode dynamic memory control chip. Both chips are implemented in CMOS and won't increase a system's power budget by much: They consume between 500 and 700 mW each. Systems that operate with 25- or 33-MHz

clock rates can currently be built with the controllers; versions that will build 42-MHz systems are planned for next year.

The A38204 delivers zero-wait-state buffered writes and burst-mode transfers from the relatively slow dynamic memory to the high-speed cache (Fig. 2). The chip, which controls from 1 to 64 Mbytes of system memory, supports both fast and slow page-mode dynamic RAMs.

Additional memory-control-chip features include support for noninterleaved, two-way address interleaved, two-way paged/two-way address interleaved, and four-way paged interleaved memory organizations. The A38204 can also use all available dynamic RAM by performing address remapping. Moreover, shadow-RAM can be supported. With shadow-RAM, routines stored in slow nonvolatile memories can be transferred during system startup into RAM. They can then be executed from RAM for faster operation.

To ensure that main memory and cache data are always valid, the A38202 employs asynchronous bus snooping. With this capability, the chip can monitor a system bus that runs at a different (often slower) speed than the processor. This is a desirable feature in 25-MHz sys-

tems, according to Nick Foskett, senior architect at Austek. Additionally, at 33 MHz snooping becomes essential, because it's impractical to use system buses that run at processor speeds. The controller also incorporates a diagnostic mode and a fault-reporting scheme, which help ease system troubleshooting.

With the A38202 controller, programmers can set up three memory regions as noncacheable areas. Two of the noncacheable regions can be assigned on 64-kbyte boundaries. The third noncacheable region can be assigned on a 4-kbyte boundary. Each region is assigned anywhere in the 80386's 4-Gbyte address space. The noncacheable regions can range in size from 64 kbytes to the full 4 Gbytes for the first two, and from 4 kbytes to 4 Gbytes for the third region. Noncacheable regions can either be separate, contiguous, or overlapping.

By having noncacheable memory regions, designers can accelerate some operations that otherwise couldn't be cached due to potential changes to the information during a cache-write operation. Even more noncacheable regions can be created, but additional off-chip logic would be required.

Furthermore, because the A38202 has separate Read and Write noncacheable Enable lines, ROM can be cached so that applications writing to ROM locations would cause the Noncache line to be asserted, invalidating the cache entry. Other cache controllers don't have separate Read/Write Enable lines, and must treat ROM as noncacheable.

Like the Intel chip, the controller can decode memory accesses for the 80387 math coprocessor. But the A38202 goes one level better by also decoding the signals for the Weitek Corp. floating-point accelerators. Implementing this capability with Intel's cache controller requires a high-speed PLD. □

PRICE AND AVAILABILITY

The A38202 cache controller and the A38204 burst-memory controller both come in 160-lead, plastic quad-sided flat packages. In 10,000-unit quantities, the 25- and 33-MHz versions of the A38202 sell for \$84 and \$98, respectively. Prices of the A38204 will be set in the mid-fourth quarter. Cache controller samples are available immediately; production is slated for mid-fourth quarter. Samples of the burst-memory control chip are expected in November.

Austek Microsystems Inc., 2903 Bunker Hill Ln., Suite 201, Santa Clara, CA 95054; Lisa Quinones, (408) 988-8556.

CIRCLE 512

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Simplicity...Versatility

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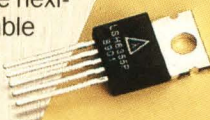
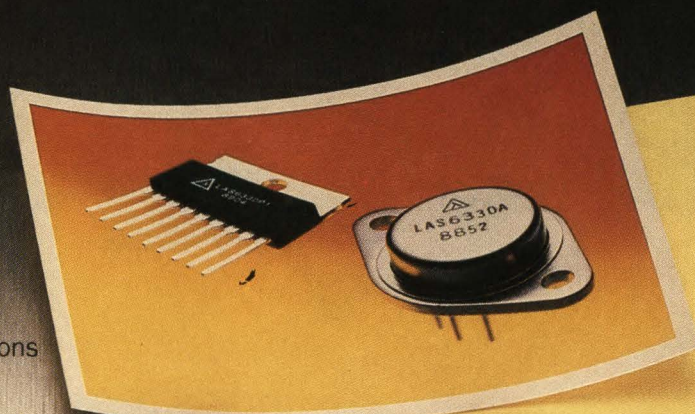
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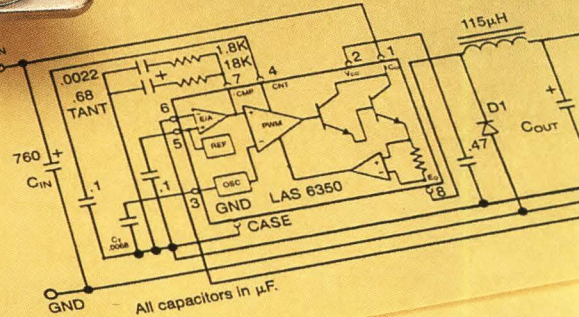
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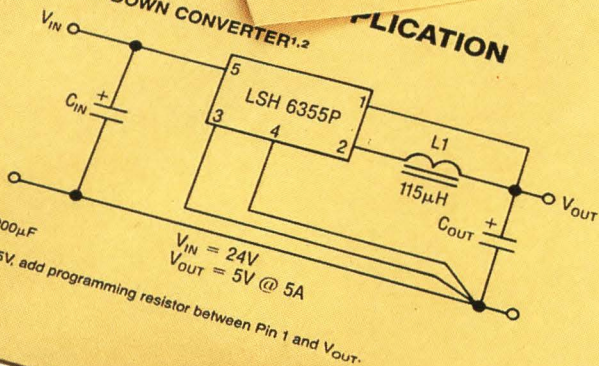
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DC-TO-DC STEP-DOWN CONVERTER^{1,2}



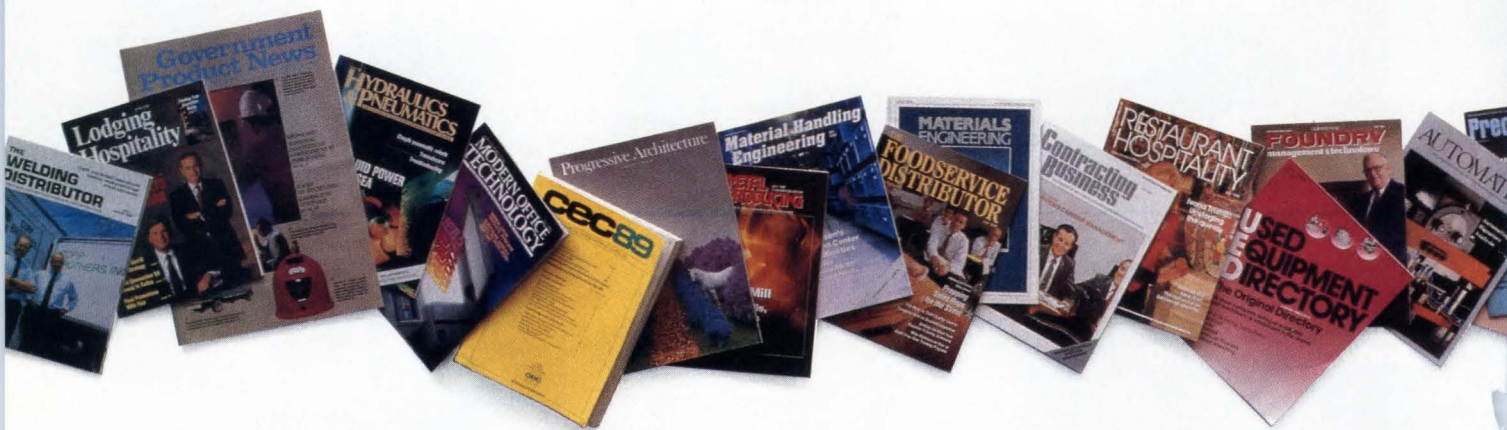
¹ C_{IN} = 470 μF; C_{OUT} = 2200 μF

² For output voltages above 5V, add programming resistor between Pin 1 and V_{OUT}.



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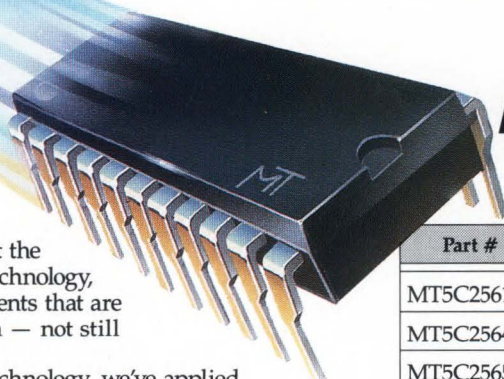
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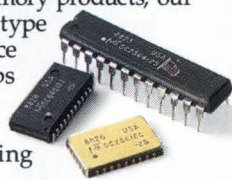
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Micron. Working to improve your memory.



Part #	Organization	Speed*	Packages
MT5C2561	256K X 1	25ns	PDIP, CDIP, SOJ, LCC
MT5C2564	64K X 4	25ns	PDIP, CDIP, SOJ, LCC
MT5C2565	64K X 4 $\overline{\text{OE}}$	25ns	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	25ns	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	15ns	PDIP, CDIP, SOJ
MT5C6404	16K X 4	15ns	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{\text{OE}}$	15ns	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 s. I/O	15ns	PDIP, CDIP, SOJ
MT5C6408	8K X 8	15ns	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	15ns	PDIP, CDIP, SOJ
MT5C1604	4K X 4	15ns	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{\text{OE}}$	15ns	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 s. I/O	15ns	PDIP, CDIP, SOJ
MT5C1608	2K X 8	15ns	PDIP, CDIP, SOJ

*Slower speeds also available.

MICRON

TECHNOLOGY, INC.

2805 E. Columbia Road, Boise, Idaho 83706 208-386-3900

68000-CODE COMPATIBILITY SMOOTHS USE OF 16-BIT MICROCONTROLLERS

LISA GUNN

With its wide variety of on-chip peripherals and 68000-code compatibility, a family of 16-bit microcontrollers from Philips Components-Signetics Co. combines flexibility with industry-standard software. The 90C100 family of CMOS controllers consumes less than 0.5 W, making it suitable for battery-powered applications. In addition, the chips are expected to cost less than \$8 apiece. Applications include screen displays, communications, automotive, and industrial systems.

The first three family members to reach the market will be the 90C100, 93C100, and 93C110 models. All are built around the CPU of the 16/32-bit SCC68070 device. In addition, each has two serial-communication controllers, three timer circuits, a seven-level interrupt controller, and various system-control circuits.

Memory for the 93C100 and 93C110 microcontrollers includes 512 bytes of RAM and 34 kbytes of ROM. The 90C100 version omits the ROM. A 256-byte EEPROM comes with the 93C110 controller.

Compatibility with industry-standard code is an important consideration for microcontroller-based systems, because fast software development means a shorter time to market. The 90C100 family extends the application spectrum of the 68000 instruction set to lower-end, mass-market applications. Development tools for the high-end 68030 and 68040 processors work equally well for the low-cost controllers.

The 90C100 family instruction set supports high-level languages such as C, and works with multitasking kernels like PSOS and VRTX. The controllers run under the GEMDOS, OS-9, and Unix operating systems, and can address programs of up to 4 Gbytes.

Although the devices usually run on a 15-MHz clock, the maximum crystal-oscillator is 30 MHz. When switched to a low-power standby

mode, the chip is clocked by a secondary, low-frequency oscillator that slashes power consumption from 400 mW to just 50 mW. During standby, the low-frequency oscillator still lets the CPU detect such external events as I²C-bus or timer signals.

All family members have 40 bidirectional I/O ports, as well as 68000, 80C51, and I²C-bus interfaces. The ports can be controlled independently as inputs or outputs, and can generate interrupts to the CPU.

Memory extension is easy thanks to the 68000 interface. Because it has two chip-select lines and automatic data-acknowledge generation, no external logic is needed for up to 2 Mbytes of off-chip memory. The I²C-bus port supports 100-kbits/s master-slave interfacing with any of the I²C-compatible modular ICs. Off-chip peripherals are added through the 80C51 interface using an 8-bit, address-data multiplexed bus.

The 34-kbytes of factory-maskable ROM that is on board the 93C100 and 93C110 is organized into 16-bit

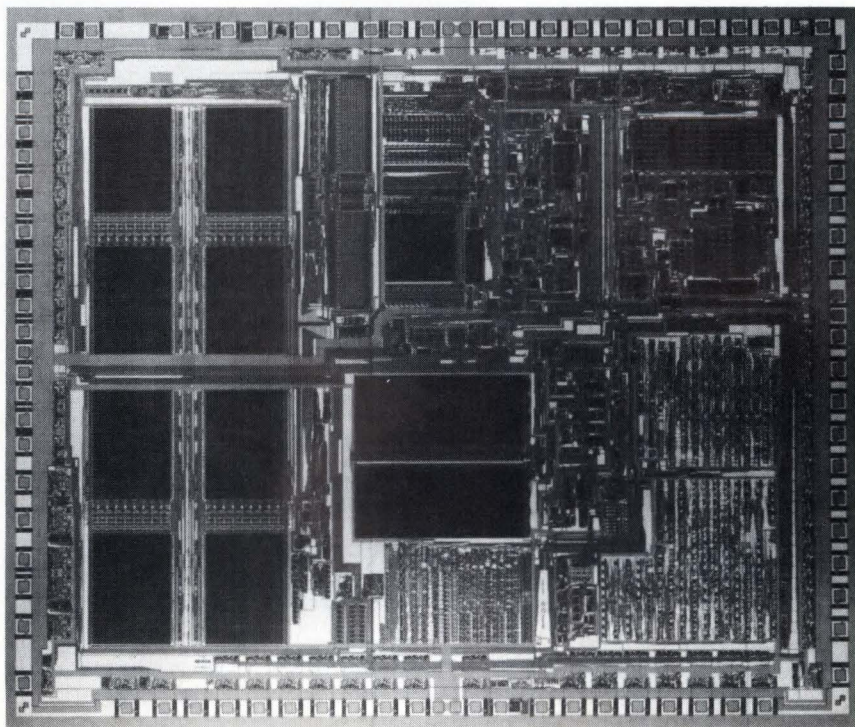
words in order to connect to the 16-bit internal bus. Also organized in 16-bit words is the 512 bytes of on-chip RAM, which can contain instructions, data, and stack.

The 90C100 family of microcontrollers is manufactured in a 1.5- μ m CMOS technology, and will also be produced in 1.2- and 1.0- μ m technologies. All three chips are available in both plastic-leaded chip carriers and quad flat packs, and in the standard-temperature (0-70°C) and extended-temperature (-40-85°C) ranges.

Samples of the 90C100, 93C100, and 93C110 are available now. Full production of the 90C100 and 93C100 versions is expected by year's end, with full production of the 93C110 by the second quarter of 1990. Initial samples of the 90C100 go for \$35 apiece, with prices expected to eventually fall to \$8 apiece. Actual pricing depends on order quantity.

Philips Components-Signetics Co., 811 E. Arques Ave., Sunnyvale, CA 94088-3409; (408) 991-2000.

CIRCLE 306



NEW PRODUCTS

DIGITAL ICs

SPEEDY BICMOS STATIC RAMS DROP ACCESS TIMES TO AS BRIEF AS 10 NS

A family of ECL-compatible biCMOS static RAMs from National Semiconductor offers

the industry's shortest access times for 64- and 256-kbit memories. The 64-kbit RAMs—the NM10494 and 100494—are organized as 16k-by-4 devices and have access times of 10, 12, or 15 ns. The NM10494 has an ECL 10K-compatible interface and

the 100494 packs ECL 100K-compatible signal lines. Offering four times the storage capacity at nearly the same speeds, the NM100504 and NM5104 are organized as 64k-by-4 arrays.

However, unlike the 64-kbit duo, which come in 10K and 100K versions, the two 256-kbit memories both have 100K-ECL-interface levels. The 100504 operates with a -4.2-to-4.8-V power supply and accesses in 15 or 18 ns, while the 5104 uses an ECL 10K power-supply level of -5.2 V but offers temperature-compensated ECL-100K input- and output-voltage levels and access-time options of 12 or 15 ns. All four chips should find a wide array of applications waiting for them—systems ranging in complexity from superminicomputers and minisupercomputers down to the caches on high-end workstations are hungry for fast memories. Instruments such as logic analyzers and in-circuit emulators also require these fast memories to run at top speed.

All four chips have balanced read and write cycles. Thanks to the mixed bipolar-CMOS process, the two 64-kbit static RAMs dissipate less than 1.3 W when accessed at a 50-MHz pace; similarly, the 256-kbit devices dissipate about 1.5 W at the same speed. Packages for any of the chips can be either 28-pin low-inductance ceramic DIPs or 28-lead fine-pitch (30-mil pitch) ceramic flatpacks. The 64-kbit DIP and flatpack use a center-pin power and ground arrangement, while the 256-kbit RAMs use a corner-pin power and ground for the DIP and a center-lead layout for the flatpack.

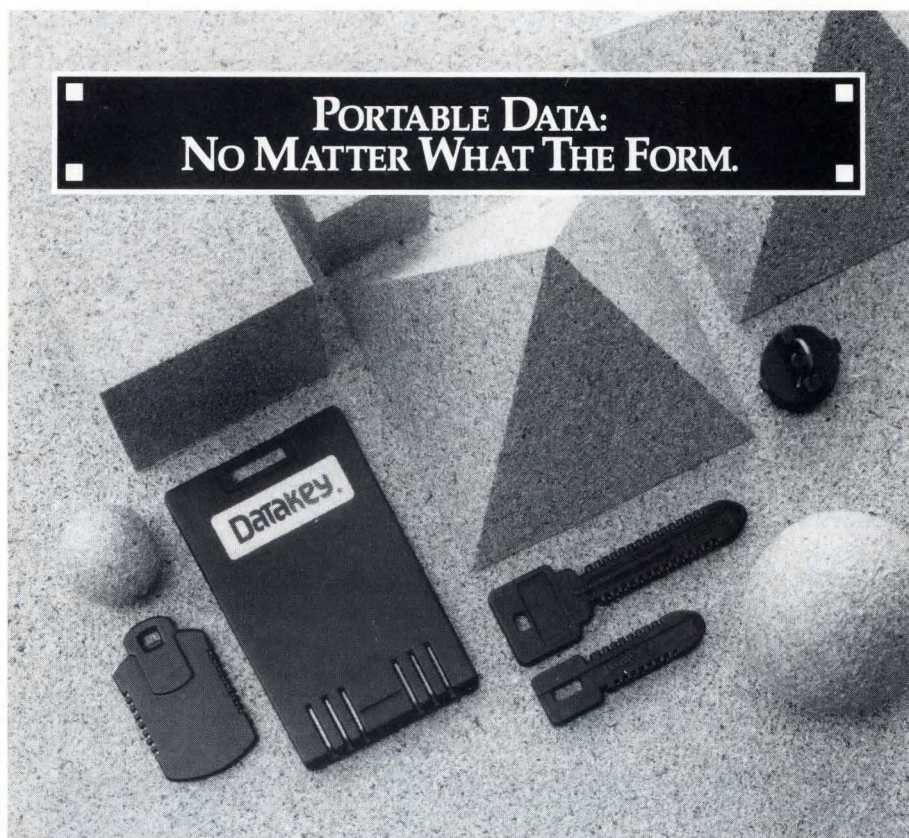
Prices for the 64-kbit RAMs start at \$95 for the 12-ns units and increase to \$115 for the 10-ns versions. For the 256-kbit chips, prices are \$125 for the 15-ns version and \$175 for 12-ns devices. All prices are for quantities of 1000, and the chips come in 28-pin DIPs. Samples are immediately available.

National Semiconductor Corp.,
2900 Semiconductor Drive, P.O.
58090, Santa Clara, CA 95052-8090;
(408) 721-5000

CIRCLE 307

DAVE BURSKY

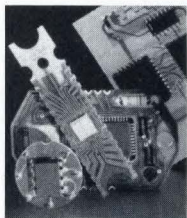
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CIRCLE 106

NEW PRODUCTS

DIGITAL ICs

CACHE CONTROLLER ADDS MORE CONTROL FEATURES AND UPS RAM HIT RATIO

Providing a superset of the features of Intel's popular 82385 cache controller, the MDS-C395e from Matra Design handles cache sizes of 32, 64, 128, or 256 kbytes. As a result, it boosts the cache-memory space by a factor of eight compared with the Intel cache-controller chip.

Besides that, the CMOS chip adds four-way set associativity to the memory-architecture options, supplementing the Intel-compatible direct mapping and two-way set-associative configurations for 80386 systems.

Yet another new feature offered by the C395e is an available copyback mode, which frees up system-bus bandwidth by maintaining main-memory coherency with the cache and minimizing major updates of main memory. Just four octal bus-transceiver chips are needed to tie the 395e into a personal-computer chip set.

The larger cache-address space made possible by the C395e lets users implement larger caches, which lessens the chances of a cache miss. This, in turn, improves the hit ratio. And, although two-way set associativity prevents cache misses and thrashing if the program jumps between two main-memory addresses at the same page offset, the C395e's four-way set associativity doubles the number of locations that can have the same page offset. That reduces cache-data replacement and also means a 99% hit ratio when all improvements are put to work.

A second version of the control chip, the MDS-C395i, is a direct replacement for the 82385 and doesn't pack the superset features. However, like the Intel chip, the 395i handles direct-mapped and two-way set-associative cache organizations. Both controllers come in versions that can be used with systems that operate at clock frequencies of 20, 25, or 33 MHz.

The MDS-C395e controller comes in a 164-lead Jedec quad-sided flat

package while the C395i comes in a 132-lead pin-grid-array package. In lots of 100, the 25-MHz versions of both chips sell for \$174 and \$142, respectively. Both 20- and 25-MHz versions are immediately available and 33-MHz units will be ready in early

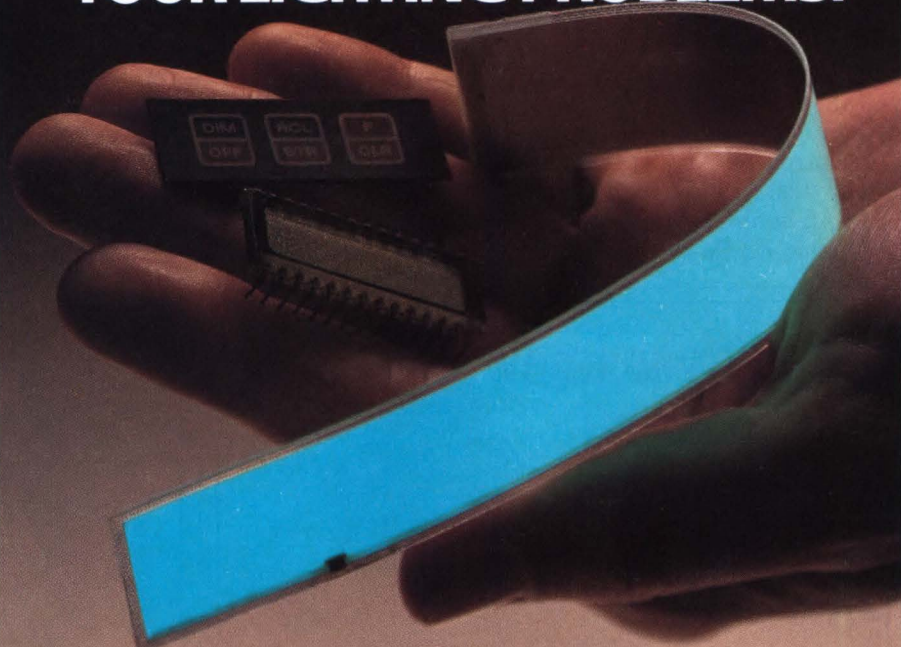
1990. A 42-MHz option will be ready by the middle of 1990.

Matra Design Semiconductor, 2895 Northwestern Parkway, Santa Clara, CA 95051; Pradip Madan, (408) 986-9000.

CIRCLE 308

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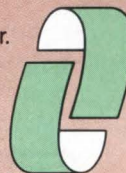
Instead of bulk, we give you a lamp so thin, it's barely three-dimensional. We can make our lamps in all kinds of sizes and shapes—with cutouts and holes.

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And with our lamps, we give you solid-state-of-the-art construction backed with our Loctite applications know-how. So for solutions to any problem, we're here. To learn more, send for our DESIGN GUIDE, the definitive reference on electroluminescence. Because the solution to your lighting problem may be as simple as seeing it in a new light.



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CIRCLE 107

NEW PRODUCTS

DIGITAL ICs

EMBEDDED MICRO CHANNEL INTERFACE CUTS AREA FOR DISK-DRIVE CONTROLLER

By embedding the IBM Micro Channel interface into its disk-drive controller chip, Adaptec has shrunk the board area needed to add a disk controller to an IBM PS/2-compatible system. The AIC-6190 handles complex I/O routines for communication over the Micro Channel and the control of "dumb" peripherals such as disk drives, tape, or optical-storage subsystems.

Also, the chip emulates three distinctly defined PS/2 disk-control register sets. As a result, it can implement the disk-control interface of any PS/2 system from the Model 50 through the Model 80. The circuit controls buffer memories of up to 64 kbytes. In addition, it generates the CAS-before-RAS signals for the dynamic RAMs that have internal re-

fresh counters. This means that buffers can be made up of low-cost dynamic memories.

The AIC-6190 comes in a 100-lead plastic quad-sided flat package, consumes about 500 mW, and sells for \$30 in production quantities. Samples are available from stock.

Adaptec Inc., 691 S. Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600.

CIRCLE 309

DAVE BURSKEY

PC CHIP SET TAKES ON THE HIGH END WITH LOCAL BUS ARCHITECTURE

Built from the ground up to deliver top performance from non-cached 80386 systems, ZyMOS' System 90 three-chip set puts a novel local-bus and intelligent-coprocessor scheme to work. The local-bus approach removes slow address and data paths while maintaining full

IBM-PC/AT compatibility. In addition, the P90 peripheral coprocessor and the P91 intelligent look-ahead memory controller minimize memory wait states so that an 80386SX system operates with just a 0.2-wait-state penalty. The third chip is the P92 bus-interface circuit.

The P90/SX, which is the first version of the chip set, will implement 80386SX-based systems. To build a PC, the P90/SX set is tied into the 386SX CPU, a keyboard controller, a system BIOS ROM, and the main memory.

In quantities of 1000, the three-chip set sells for \$96.50. A fourth chip that will add DMA channels and serial and parallel ports is now in development.

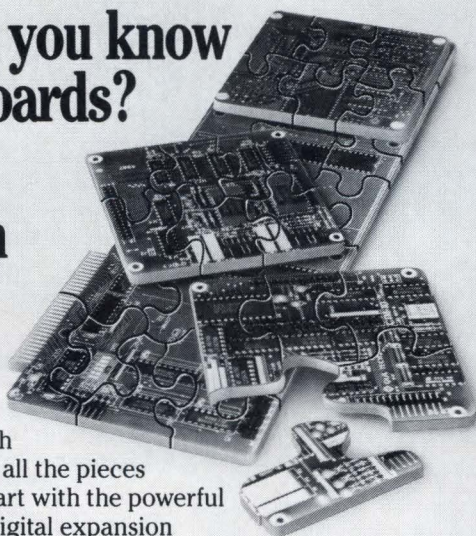
ZyMOS Inc., 477 N. Mathilda Ave., Sunnyvale, CA 94086; Lou Williams, (408) 730-5400.

CIRCLE 310

DAVE BURSKEY

Think you know I/O boards?

Then design one.



The Qua Tech PXB-721 has all the pieces you need. Start with the powerful 72 channel digital expansion card and connect up to three data acquisition modules—counter-timer, D/A converters, or A/D converters.

The single-slot, modular system keeps your flexibility up. And it keeps your cost down because you pay for only as much board as you need.

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CIRCLE 108



"Something's got to go, Fenton.
You, me or this inventory—and it's not going to be me."

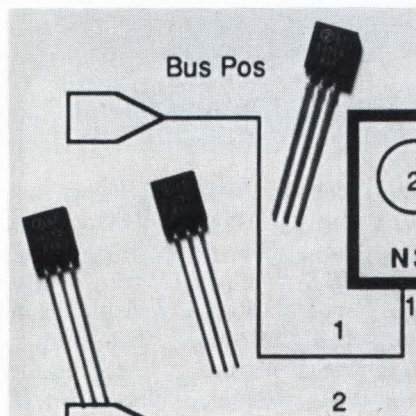
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NEW PRODUCTS

ANALOG

MULTIPLE HALL-SENSOR ICs TALK TO HOST VIA 2-WIRE, 2-WAY POWER-SIGNAL BUS



Up to 30 Hall-effect-sensor ICs can be connected on a time-division multiplexed, two-wire serial bus and all can be individually queried at up to 10 kHz by a host microprocessor.

Sprague's UGGN3055U and UGS3055U Hall-sensor ICs were designed for automotive applications in which they detect the presence or absence of a small permanent magnet. But they lend themselves to many industrial and consumer jobs. Some of these are liquid-level sensing, burglar-alarm systems, major appliances, and virtually any automated assembly line or storage system.

When the sensors' factory-programmed address appears on the bus, the IC first transmits a diagnostic signal to declare that it is working properly. This signal is followed by one indicating the presence or absence of the magnetic field it is monitoring.

Two of each chip's three pins connect to the bus, while the third is available for an alternative application, such as sensing an open or closed switch in lieu of a magnetic field. If used in this manner, the switch is connected between pins 2 and 3. Besides handling the two-way signals, the two-wire bus powers up to 30 of these ICs at 2.5 mA each.

Each chip is addressed by the host by switching the supply rail between 6 and 9 V to form a serial-pulse train. When the sensor detects that it has been addressed, it increases its quiescent

current by 300 μ A when the rail is 9 V if it is working. Then, if sensing a magnetic field, the current increase is continued when the rail falls to 6 V.

In quantities of 1000, the -20-to-+85°C UGN3055U goes for \$1.60

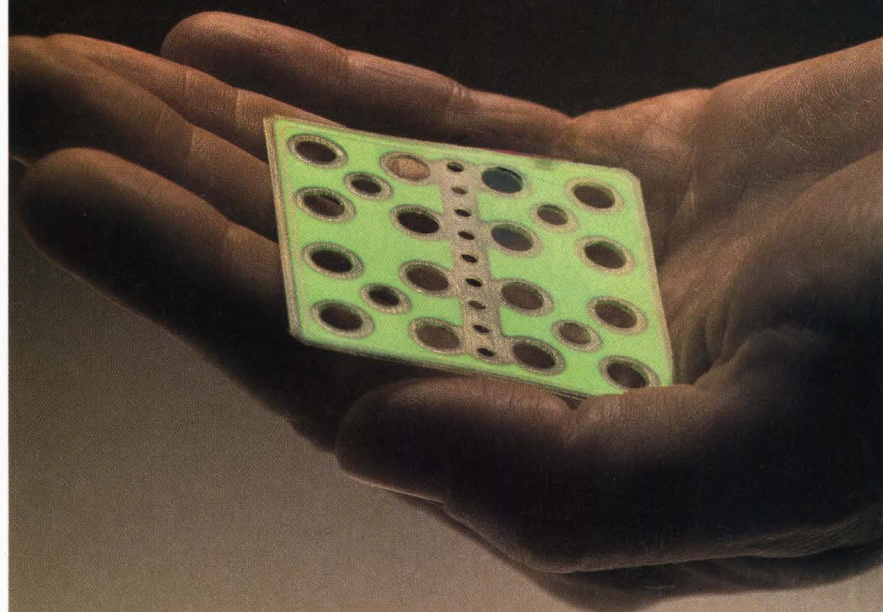
each, while the -40-to-+125°C UGS3055U costs \$1.79 each. Delivery is from stock.

Sprague, 363 Plantation St., Worcester MA 01605; Ravi Vig, (603) 224-1961.

CIRCLE 311

FRANK GOODENOUGH

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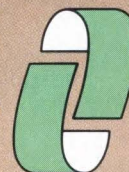
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CIRCLE 110

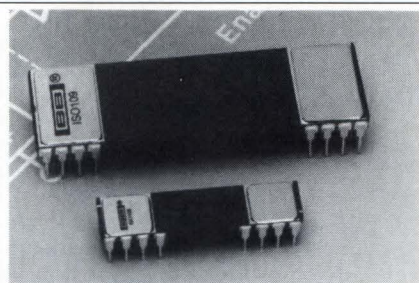
NEW PRODUCTS

ANALOG

1-MHz V-F CONVERTER ICs TAKE 12-BIT DATA ACROSS 5000-V ISOLATION BARRIERS

A pair of voltage-to-frequency converters (VFCs) from Burr-Brown combine the functions

of a VFC, a high-voltage opto-coupler, and a logic gate in single, low-cost ceramic DIPs. The ISO108 and ISO109 incorporate the company's unique high-voltage isolation technology, which uses 1-pF metal-film capacitors, embedded in a her-



metic ceramic sandwich. The capacitors pass pulses from a VFC across a high-voltage barrier while providing up to 5000 V dc (3500 V rms) of true galvanic isolation between analog input and digital pulse-train output.

The ISO109, the larger of the pair, comes in a 40-pin double-width DIP. It's aimed at medical applications and is rated for continuous operation at 5000 V dc from -55° to $+125^{\circ}\text{C}$. Its smaller sibling comes in a 24-pin DIP and is aimed for industrial tasks. It's rated at 2121 V dc (1500 Vrms) for similar operating conditions.

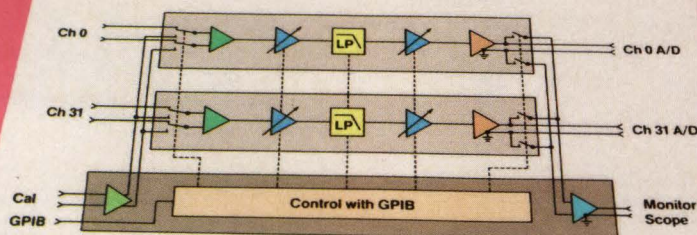
The VFC chip on the devices' input side can operate at full-scale (FS) frequencies as high as 3 MHz while providing a typical linearity error of 0.5% of a 10-V FS signal. At 1-MHz FS, linearity error is 0.025% at most and is typically under 0.01%. At 10-kHz FS, typical linearity can exceed 16 bits. Besides the VFC, the input chip has a 5-V reference which may be used to provide an offset for bipolar input signals. Pulse-to-pulse jitter is typically under 200 ppm at a full-scale frequency of 1 MHz, and half that at 100 kHz. Transient immunity without signal loss is typically better than $10,000\text{ V}/\mu\text{s}$. Isolation-mode rejection is better than 130 dB at 60 Hz. Barrier leakage current is a maximum of $0.5\text{ }\mu\text{A}$. Moreover, that's at 2500 and 3500 V rms for the 108 and 109, respectively.

The pulse-train output is provided by an open-collector transistor rated at 20 V and 10 mA. An output-enable pin permits multiple VFC outputs to be multiplexed on the same line.

In quantities of 100, ISO109 and ISO108 ICs cost \$19.80 and \$16.25, respectively. Delivery is from stock.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; Barry Ehrman, (800) 548-6132. **CIRCLE 312**
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CIRCLE 111

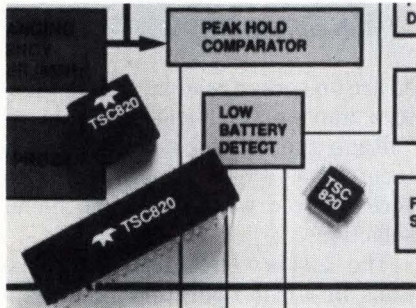
NEW PRODUCTS

ANALOG

3-3/4-DIGIT DATA SYSTEM ON A CHIP GIVES VOLTS, AMPS, OHMS, AND FREQUENCY

Designers now can get a complete measurement system on one chip. At the heart of Tele-dyne Semiconductor's TSC820 lies a 3-3/4-digit (3999-count) integrating analog-to-digital converter, a 4-MHz frequency counter with four decades of autoranging, a logic probe, and a driver for liquid-crystal displays. It also includes functions not usually found on a converter chip, such as decimal-point drivers, a low-battery detector, a buzzer driver, and a peak-read-and-hold circuit.

While aimed at portable test instruments, the TSC820 also gives system designers the basis of a versatile, built-in diagnostic tool for both analog and digital circuitry. The chip's converter boasts ten times the resolution of available devices with a full-scale range of 200 to 400 mV.



Moreover, it provides 100 μ V of resolution in the 400-mV range. The converter also offers a guaranteed zero reading and a zero-integrator cycle to ensure fast overload recovery. Unlike most low-cost CMOS integrating a-d chips, the TSC820 IC's has a temperature coefficient of 35 ppm/ $^{\circ}$ C.

Logic-level measurements are easily made with the chip's logic-probe inputs while external level shifters adjust for logic families.

The TSC820 comes in 40-pin DIPs, 44-pin PLCCs, and flat packages. Pricing in quantities of 100 starts at \$6. Delivery is from stock.

Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, CA 94039-7267; Wes Freeman, (415) 968-9241.

CIRCLE 313

FRANK GOODENOUGH

SAMPLING-AMP PAIR MIXES TRUE 16-BIT ACCURACY WITH SPEED AND LOW COST

At first glance, Analog Devices' AD386 and AD1154 hybrid sampling amplifiers may look like fraternal twins, but kissing cousins would be a better description. Both provide true 16-bit accuracy, and they can't be beat for price-performance ratio. Not only that, both provide a dielectric-absorption spec, because their hold capacitor is internal and their very good droop specs (20 μ V/ms) are identical. But the amplifiers differ in dynamic specs as well as architecture, size, cost, and features.

A comparison of the amplifier's dynamic specs should be prefaced by noting that the AD386 shows an inverting design with a gain of -1 and an input impedance of 5 k Ω , while its cohort looks like a buffer with a gain of +1 and a multimegohm JFET input impedance. The AD386, however, carries an undedicated, high-speed op amp connected for a differential gain of 1. It can invert the signal, provide ground sensing, and take signals from balanced lines.

The faster AD386 grabs a 20-V-step change to 16-bit accuracy in just 4.5 μ s maximum. The AD1154 takes 5 μ s to do that job. The AD386 will also grab a similar voltage to 14-bit accuracy in 1.5 μ s. Aperture uncertainty (jitter), which determines the highest-frequency sine wave that can be sampled, is 40 ps for the AD386 and 150 ps for the AD1154.

If size and cost are critical, the AD1154 is the way to go. It comes in a 0.3-in.-wide, 14-pin metal DIP and starts at \$42 in lots of 100. The AD386's metal DIP is 0.6 in. wide and has 24 pins. It starts at \$79 for similar lots. Small quantities are delivered from stock.

For the AD1154: Analog Devices Inc., P.O. Box 9106, Norwood, MA 02062-9106; (617) 461-3552.

CIRCLE 314

For the AD386: Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; (508) 658-9400.

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CIRCLE 112

NEW PRODUCTS

INSTRUMENTS

TWO 100-MHz DSOS OFFER CHOICE OF PERFORMANCE, CONVENIENCE FEATURES

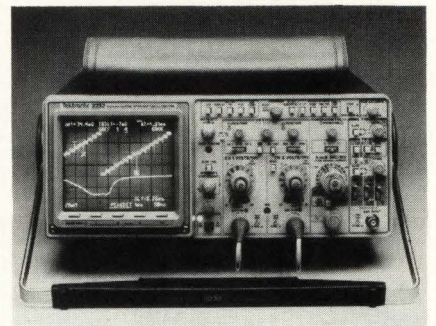
A pair of 2-channel digital storage oscilloscopes from Tektronix offer 100-MHz sam-

pling rates, 4-ksample record lengths, 10-ns glitch capture, and 8-bit vertical accuracy. The 2232 uses custom digital ICs to deliver a 10-MHz single-shot bandwidth, repetitive sampling, and a 100-MHz analog-scope capability. The 2224 fea-

tures a 10-MHz digital storage bandwidth and a 60-MHz analog bandwidth.

Besides its standard triggering capabilities, including pre- and post-trigger features, the 2232 adds trigger-level readout. Users can set the voltage level for triggering and read it on the screen. This can save time in single-shot capture and babysitting applications. To ensure stable triggering on noisy or complex signals, the scope, which can store 29 waveforms, can reject unwanted high- and low-frequency signals.

Extensive ease-of-use features enhance the 2232's capabilities. Includ-



ed are on-screen readout of scale factors and cursor measurements of voltage and time. A new user interface employs CRT bezel buttons to access saved waveforms and menu selections.

The 2224 is well-suited for applications in which operators must capture lower-frequency signals and single-shot events without the need for repetitive sampling to make use of the scope's full front-end bandwidth. In addition, roll and scan modes can display slow events down to 5 s/div. The unit's measurement cursors automatically calculate and display delta time and voltage measurements on the screen. Using its simultaneous sampling feature, the 2224 can capture stimulus and response signals at the same time.

The 2232 and 2224 cost \$5495 and \$4495, respectively, and are available immediately. RS-232C and GPIB communications options cost \$300 each.

Tektronix Inc., P.O. Box 1700, Beaverton, OR 97075; (800) 426-2200.

CIRCLE 315

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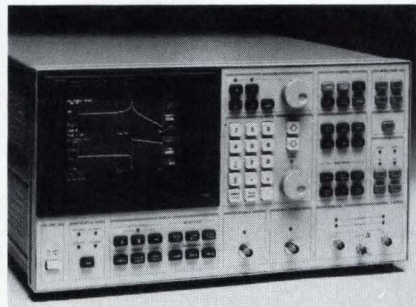
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Fax. (408) 378-7869

CIRCLE 113

NEW PRODUCTS

INSTRUMENTS

ANALYZER HANDLES ANALOG AND DIGITAL SIGNALS FROM CONTROL SYSTEMS



Advanced closed-loop control systems that use both analog and digital signals are easier to develop and test with the HP 3563A control-system analyzer. A built-in signal generator produces analog and digital stimulus signals for network analysis. On the input side, the instrument accepts analog and digital response signals directly.

Using internal digital-signal-processing capability, the HP 3563A makes network, spectrum, and time measurements on analog signals from dc to 100 kHz and on digital signals with clock rates to 256 kHz. The analyzer also performs network-modeling and parameter-estimation tasks that typically require an external computer. The unit's measurement and marker capabilities make it easy to evaluate signal level, power-spectral density, distortion, and drift.

The instrument simplifies the characterization of digital filters. Rather than adding analog-I/O circuitry to evaluate the filter's response, designers can measure magnitude and phase directly by applying a digital stimulus and reading the digital output of the filter integrated circuit. The analyzer displays the resulting frequency response directly on its screen.

A nonvolatile memory stores five sequences of front-panel operations for call-up with one keystroke. Operators can use this capability to control external HP-IB (GPIB) devices. The two-channel HP 3563A itself is fully programmable over the HP-IB and is compatible with digital plotters that work with the HP Graphics

Language.

The HP 3563A control-systems analyzer costs \$24,900 and has an estimated delivery of 6 weeks after receipt of order. Also, Hewlett-Packard will convert HP 3562A dynamic-signal analyzers to HP 3563A

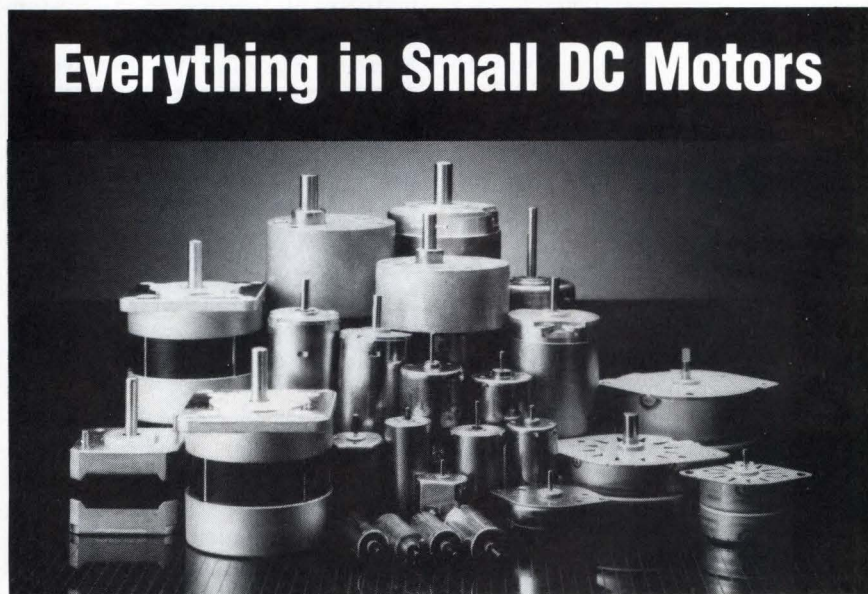
functionality for \$9900. The conversion takes an estimated 4 weeks.

Hewlett-Packard Co., Lake Stevens Instrument Div., 8600 Soper Hill Rd., Everett, WA 98205-1298; (800) 752-0990.

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CIRCLE 114

NEW PRODUCTS

INSTRUMENTS

MODULE ADDS FULL SCAN TEST CAPABILITY TO ASIC TESTER-VERIFIER

Owners of the Logic Master XL series of ASIC test and verification systems from IMS can take advantage of new scan testing techniques by adding a Logic Master XL Scan Test Module to their testers. The module offers hardware and software support for any of the numerous techniques available, including the proposed IEEE P1149.1 JTAG standard, scan path, scan set, random-access scan, and level-sensitive-scan design.

Users can add up to seven modules to any XL 60, XL 100, or XL2 system. Each module has four I/O channels with a total of 4 Mbits of memory. The built-in scan-test software lets operators configure the module for four channels with 1 Mbit each, two channels with 2 Mbits behind each pin, or one channel with a 4-Mbit memory. Regardless of configuration, all tests can be run at up to 60 MHz.

The software creates an easy-to-interpret display of the scan input and output data. Designers can specify unformatted data, raw data, error-only scan frames, or user-defined groups of bits. In addition, scan data patterns from leading scan-simulation companies can easily be loaded in the XL system for use during ASIC-design verification. Furthermore, the operator can move back and forth between scan, functional, and parametric operations in real time.

Using the module to test a scan-based device, designers can obtain a large amount of data from only a few dedicated I/O pins. The JTAG proposal, for example, calls for a 4- or 5-pin boundary scan bus.

The XL Scan Test Module, which will be available in the fourth quarter, costs \$33,000. The price includes hardware and the operational software for scan data analysis.

Integrated Measurement Systems Inc., 9525 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-7117.

CIRCLE 316

JOHN NOVELLINO

DATA-ACQUISITION SYSTEM ACCEPTS ANALOG, DIGITAL, AND FREQUENCY INPUTS

High-speed sampling, high accuracy through on-line calibration, digital compensation, and extensive data-reduction capability are all features of the System 8400 data-acquisition system from Pressure Systems Inc. The system



serves a broad range of measurement applications by accepting analog, digital, and frequency inputs. It is capable of all media pressure, force, flow, temperature, and acceleration measurements.

Through the use of a dedicated microprocessor for each physical parameter to be measured, data-acquisition speed is maximized and added flexibility for system configuration is possible. Digital compensation and on-line calibration provide high accuracy and elimination of frequent, costly lab calibration. The system incorporates programmable pressure generation capable of full-scale ranges from 1 to 500 psi. As a result, the system lends itself to simplified, accurate, high-speed calibration of multiple discrete pressure transducers.

The basic system consists of a mainframe and one input unit of four channels. This delivers sampling capability of up to 20,000 channels/s. Convenient, on-site expansion to up to 64 input units provides 4096 channels for data acquisition at up to 400,000 channels/s.

System prices start at \$14,700. Delivery is in 4 months after receipt of order.

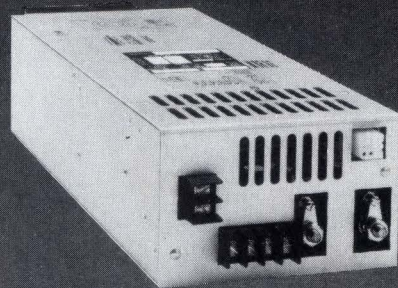
Pressure Systems Inc., 34 Research Dr., Hampton, VA 23666; (804) 766-2644.

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CIRCLE 115

NEW PRODUCTS

COMPUTERS & PERIPHERALS

MODULAR, HIGH-CAPACITY STORAGE SYSTEM WORKS WITH PCS, NETWORKS

Designed for use with standalone personal computers, multiuser systems, or local-area networks, the StorEdge family of data-storage subsystems from Fujitsu America Inc. lets designers increase storage capacity in a modular fashion. The initial family members will support systems running Novell Advanced Netware 286, or MS-DOS 2.0 or higher.

The modular product can be configured with any combination of up to three Fujitsu 320-Mbyte, 5.25-in. hard disks and/or 220-Mbyte tape drives. In addition, up to three subsystems can be daisy-chained and used on a Netware fileserver for up to two Gbytes of on-line storage.

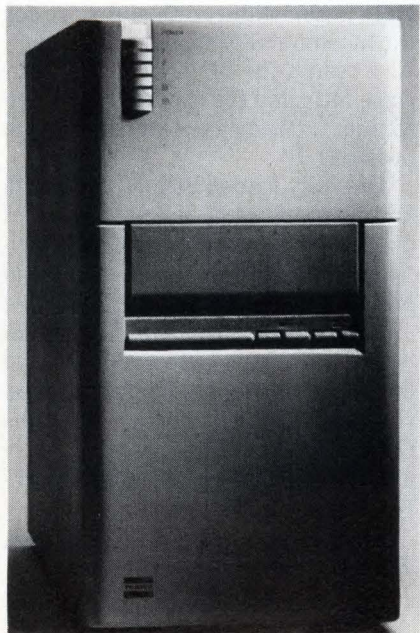
StorEdge also features MS-DOS 1/2-in. tape backup. The backup is fast: in less than 15 minutes, 140 Mbytes of data can be backed and stored on a single 1/2-in. cartridge with a 220-Mbyte capacity.

The Novell- and DOS-compatible versions of StorEdge are available now, starting at \$4595.

Fujitsu America Inc., Computer Products Group, 3055 Orchard Dr., San Jose, CA 95134; (408) 432-1300.

CIRCLE 319

LISA GUNN



COLOR, MONOCHROME X-STATION TERMINALS WED X-WINDOWS WITH NETWORKING



Two X-Window terminals from Tektronix combine the X-Window System 11.3 with Tek's terminal-networking capabilities. The color (XN11) and monochrome (XN5) X-stations are low-cost entry points into the X11 window system. Both terminals are cost-effective alternatives to workstations for users who don't need desktop-applications processing.

The XN11 is a high-resolution display station with a standard 15-in. display, 1024-by-768-pixel addressability, and a palette of 4096 colors. Sixteen different colors can be displayed at once. A 19-in. display and an increase to 256 displayable colors out of a possible 16.7 million colors are optional. The dual-processor architecture has memory that is expandable up to 8 Mbytes.

The lower-cost XN5 is a 16-in., high-resolution monochrome display that can address 1024-by-1024 pixels. It is powered by a 12.5-MHz Motorola 68000 processor and a graphics coprocessor. The 1-Mbyte RAM is expandable to 4.5 Mbytes.

Connectivity options let the two X-stations fit into work environments including workstations, minicomputers, mainframes, and supercomputers.

In its standard configuration, the XN11 display station costs \$7495, with a special introductory price of \$6995 through November. The monochrome XN5 display station costs \$2795. The XN11 will ship in November, and the XN5 is shipping now.

Tektronix Inc., P.O. Box 14689, Portland, OR 97215; (800) 225-5434.

CIRCLE 320

LISA GUNN

UNIQUE LCD, INFRARED TECHNOLOGY DELIVERS STEREO 3D-VIEWING GLASSES

Achromatic liquid-crystal lenses and a unique infrared broadcasting technique lets a pair of glasses emulate the way human eyes work, creating a vivid, stereo 3D depth effect. CrystalEyes is a field-sequential, electro-stereoscopic system that produces flickerless, 3D stereo viewing by alternating left and right views at 120 Hz.

The CrystalEyes system consists of the eyewear and an infrared emitter, which must be used with a stereoscopic monitor and a 60-/120-Hz workstation. Stereo-ready (60-/120-MHz) workstations are manufactured by Apollo, Ardent, and Silicon Graphics, among others. A special controller (GDC-3) is available for workstations that run only at 60 Hz.

The battery-operated eyewear, which weighs only 85 g, runs for 90



hours of continuous operation. The device's dynamic range is over 100:1, creating a nearly ghost-free image. In addition, a bright image results from the lenses' 32% transmission.

The infrared emitter sits on top of the monitor. It broadcasts information that switches the eyewear lenses in precise synchronization with the images being presented on the monitor. Any number of users may wear CrystalEyes to view the display.

The CrystalEyes 3D viewing system, which consists of the eyewear and the infrared emitter, costs \$1995. A system with the GDC-3 workstation controller goes for \$3990. All products are available now.

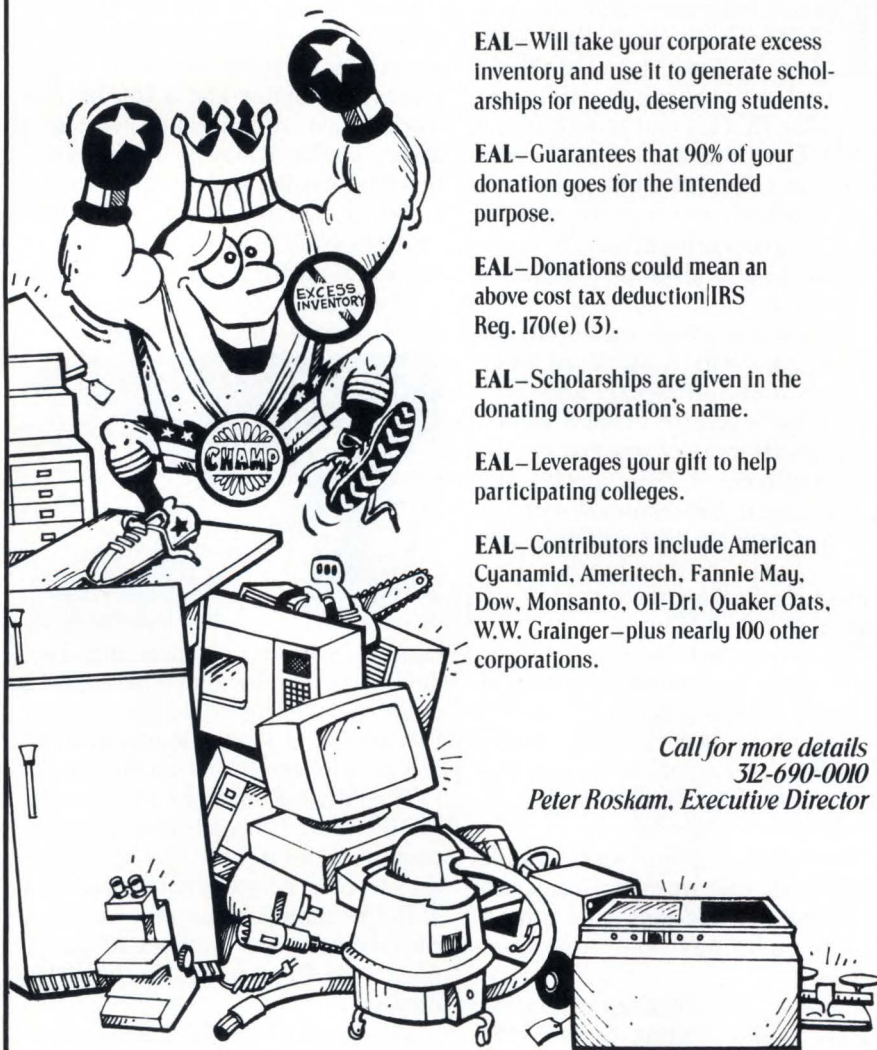
StereoGraphics Corp., 2171-H East Francisco Blvd., San Rafael, CA 94901; (415) 459-4500.

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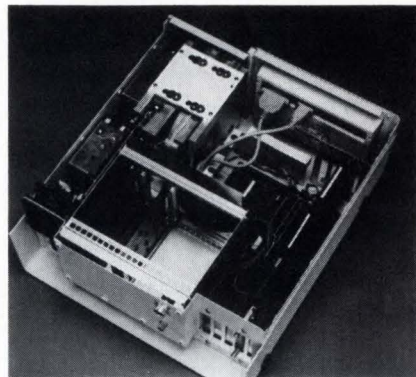
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NEW PRODUCTS

COMPUTERS & PERIPHERALS

PC/AT-CLASS EMBEDDED COMPUTER SUITS INDUSTRIAL- CONTROL APPLICATIONS



The foundation for a system or a part of a larger system, the VIPc embedded PC from Burr-Brown has the features of a powerful PC/AT-class machine. The industrial-grade PC can be thought of as a standard component that can take on a wide range of applications from a lab data-acquisition system to a factory-floor programmable controller.

The machine is an adaptable intelligent instrumentation platform that can accept up to four of the company's PCI-20000 data-acquisition and control boards in its expansion slots. An internal shielded card cage holds up to 10 signal-conditioning and field-wiring Euro-style termination panels.

Operation at either 6.25 or 12.5 MHz is selectable with software for the machine's 80286 microprocessor. As a result, the PC can run any software intended for the MS-DOS environment. Many configurations are possible.

The fully-loaded PCI-5001H-1 with 2 Mbytes of RAM, a 40-Mbyte hard disk, a 1.2-Mbyte floppy drive, keyboard, 80287 math coprocessor, and MS-DOS version 3.3 costs \$7435. The entry-level PCI5004H-1, which comes with 512 kbytes of RAM and omits the hard disk, math coprocessor, and MS-DOS, goes for \$3995. Other intermediate versions are available. Delivery of small quantities is from stock.

Burr-Brown, 1141 W. Grant Rd., Tucson, AZ 85705; (602) 746-1111.

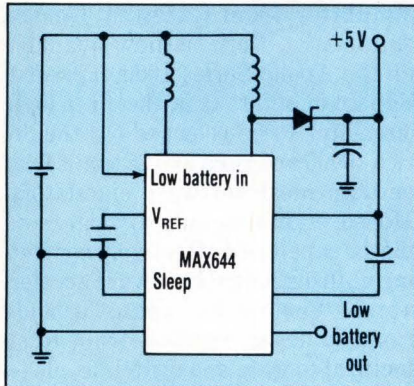
CIRCLE 322

DAVID MALINIAC

NEW PRODUCTS

POWER

BOOST-TYPE SWITCHING REGULATORS PULL 5 V FROM A SINGLE 1-TO-1.5-V CELL



A switching-regulator family from Maxim squeezes out usable power for hand-held electronic systems from one alkaline, nickel cadmium, or lithium battery. The MAX644/5/6/7 regulators serve pocket pagers, bar-code readers, palm-sized instruments, and patient monitors. All four are guaranteed to start at voltages as low as 1.15 V, but will continue to run at voltages as low as 1.0 V. Each fits a slightly different application. The MAX647 puts out 3 V and the rest deliver 5 V.

All control functions, plus a power FET capable of passing 40 mA, are contained within the MAX644, MAX645, and MAX647, while the MAX646 is designed to drive an external power MOSFET. All but 80 μ A is available to the load. The MAX644, MAX646, and MAX647 are optimized for single 1.15-to-1.5-V-cell operation. The MAX645 is for 3 V from two cells or one lithium cell. In a typical maximum-output operation, the chips use 40 mA from the supply but may be put to sleep, which drops their supply draw to 500 μ A.

The chips come in plastic and ceramic 14-pin DIPs and plastic SOICs. Commercial, extended industrial, and MIL-grade units are available. In quantities of 10, prices range from \$3.08 to \$7.70. Delivery is from stock.

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; Jim Dekis, (408) 737-7600.

CIRCLE 323

FRANK GOODENOUGH

KITS BUILD THIN, DENSE SWITCHING REGULATORS WITH 5-V OUTPUTS

There's no longer any reason to avoid resonant-mode switching regulator techniques. Cherry Semiconductor now offers a simple kit that builds the CS-3805A 100-W dc-to-dc resonant-mode switching regulator. Rated at 5 V and 20 A, the kit includes Multisource Technology's proprietary "Planer Magnetics" for major inductances to keep the supply's thickness to just 0.625 in.

Meanwhile, Multisource offers a kit for a 5-V, 40-A current-mode pulse-width-modulated supply that measures an even thinner 0.5-in. thick. Both regulators have footprints that cover a 3-by-5-in. index card. Cherry's supply runs at 600 kHz, while Multisource's runs at 300 kHz.

While the Cherry kit is basically for evaluating its CS-3805A resonant-mode controller IC, Multisource considers its 200-W MTC200W supply to be a viable one for production systems. It is also available in finished form. For power-supply designers, both kits aid in evaluating the performance of "Planer Magnetics."

The Cherry supply handles an input-voltage range of 36 to 60 V and provides an output from 2 to 20 A. For those input and output ranges, line and load regulation are $\pm 0.1\%$ and $\pm 0.5\%$, respectively. Output voltage ripple is typically 50 mV pk-pk while I/O isolation is 500 V. The MTC200W current-mode PWM supply has similar ripple and isolation specs.

In single quantities, Cherry's kit costs \$149.95 plus a \$2.50 shipping charge. The Multisource kits go for \$250 each and finished units for \$500 each. Both are delivered from stock.

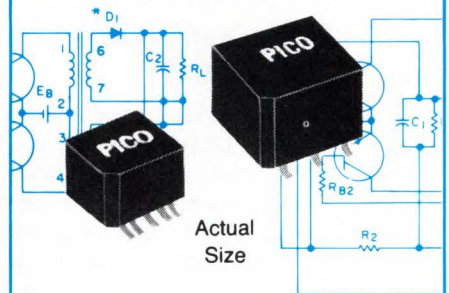
Multisource Technology Corp., 393 Totten Pond Rd., Waltham, MA 02154; (617) 890-1787. CIRCLE 324

Cherry Semiconductor Corp., 2000 S. County Trail, E. Greenwich, RI 02818; (401) 885-3600.

CIRCLE 328

FRANK GOODENOUGH

ULTRA-MINIATURE SURFACE MOUNT



DC-DC Converter Transformers and Power Inductors

These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The Inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

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- All units are magnetically shielded
- All units exceed the requirements of MIL-T-27 ($+130^{\circ}\text{C}$)
- Transformers have input voltages of 5V, 12V, 24V and 48V. Output voltages to 300V.
- Transformers can be used for self-saturating or linear switching applications
- Schematics and parts list provided with transformers
- Inductors to 20mH with DC currents to 5.4 amps
- Inductors have split windings

Delivery—stock to one week

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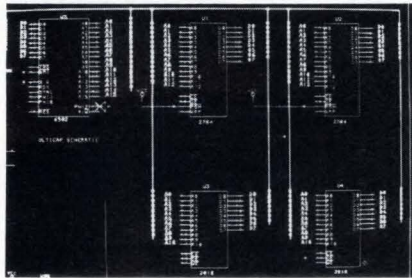
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IN NEW YORK CALL 914-699-5514

CIRCLE 112

LOW-COST SCHEMATIC-CAPTURE PACKAGE BOOSTS SPEED, VERSATILITY

To most designers, a schematic is considered the nucleus of a design, and it's the easiest point at which to enter most of the technical data. This means a quality schematic-capture package is essential to a first-rate design. Ulticap, from Ultimate Technology, lets designers add the technical details that



will be required in the later stages of design as well as handling standard component entry.

Ulticap runs on IBM PC/XT, PC/AT, PS/2, or compatible computers and boasts such features as automatic bus labeling, component and block dragging with auto reroute, back annotation with pin and gate swap, and library-independent design files. An autowire capability routes connections automatically by snapping to the points where connections are to be made. Invisible symbol boundaries guide the wire through the schematic.

Unlimited hierarchical drawing levels can be maintained with full automatic back annotation through all the levels. EDIF and Spice netlist formats are supported. Also, designers can browse through the graphic and alphanumeric on-line libraries. Data can be entered with a mouse. The user interface is consistent with Ultimate's Ultiboard pc-board design package.

Two versions are available immediately. One runs under DOS (\$595) and the other under OS/286/386 (\$790).

Ultimate Technology, 5955 Jimmy Carter Blvd., Suite 20, Norcross, GA 30071; (404) 242-0125.

CIRCLE 325

RICHARD NASS

IC SOFTWARE OFFERS TIMING-DRIVEN LAYOUT

SC II Release 2.0, a CAE system for the design of cell-based and structured custom ICs, integrates true floorplanning of blocks and cells with placement and routing that is timing-driven and global. Along with soft partitioning of cells, it virtually eliminates the need for multiple placement and routing iterations, significantly reduces die size, and increases chip performance. Timing-driven layout allows users to specify maximum and minimum net thresholds for all nets prior to placement and routing. SC II's global placement algorithm makes use of the structure embedded in the design, enabling it to reduce die sizes by up to 15%. The hardware-independent CAE system runs on Digital, Sun, and Apollo platforms.

Silvar-Lisco, 1080 Marsh Rd., Menlo Park, CA; (415) 324-0700.

CIRCLE 331

CAE SYSTEM RUNS ON UNIX WORKSTATIONS

A Unix-based CAE software system provides a complete framework to integrate CAE and CAD tools from third-party vendors and in-house proprietary applications. Called Workview Series II, the system runs under Unix on powerful hardware platforms from Sun Microsystems and Digital Equipment Corp. It offers an open architecture of standard interfaces, a data-base query language, and a programmatic data-base interface. The backbone of the system is Viewsim/SD, a simulator for system-wide development. In the Unix environment, Workview Series II supports such features as multitasking, networking, virtual memory, and X Windows. It also supports EDA industry standards (EDIF and VHDL). Pricing starts at \$10,000. Workview Series II is available immediately on Sun-3, Sun-4, and SPARCstations; delivery for DECstations takes 120 days.

Viewlogic Systems Inc., 313 Boston Post Rd. W., Marlboro, MA 01752; (508) 480-0881.

CIRCLE 332

SIMULATOR RUNS ON APOLLO SERIES 10000

The Verilog-XL mixed-level logic simulator from Gateway Design Automation Corp. is now available on the Apollo Series 10000 Personal Supercomputer. It is the first logic simulator to be released for the Series 10000 and runs 3 to 25 times faster than most software simulators. Moreover, it is the only software simulator capable of effectively competing with dedicated hardware accelerators. Verilog-XL spans a wide range of design levels — from architectural to gate and switch levels — and allows designers to use one language for the full range of mixed-level design. Equipped with up to four CPUs, the Series 10000 permits simulation, design verification, and routing to occur simultaneously, dramatically improving design throughput. Its processing power and virtual-memory capacity are ideal for large, complex designs.

Apollo Computer Inc., 330 Billerica Rd., Chelmsford, MA 01824; (508) 256-6600.

CIRCLE 333

SOFTWARE ROUTES MIXED BLOCKS, CELLS

The latest version of the Compose chip assembly environment is one of the first IC design tools to automatically handle mixed blocks and cells without restricting the design. Version 2.0 improves chip performance and reduces the design cycle by automatically placing and routing standard cells and custom blocks simultaneously. It analyzes every element of the design to create shorter interconnects and denser chip layouts. Compose 2.0 also includes new analog and mixed analog-digital capabilities. The software runs on Sun-3 and Sun-4 workstations. Priced at \$50,000, the package comes with a block placer, block router, compactor, interactive editor, and footprint generator. The standard cell placer and global router are optionally available for \$15,000.

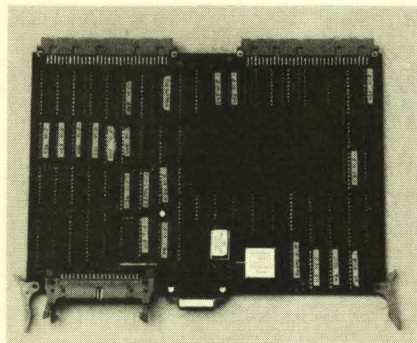
Valid Logic Systems, 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400.

CIRCLE 334

NEW PRODUCTS

COMPUTER BOARDS

VMEBUS FLOATING-POINT ACCELERATORS PACK 25 TO 100 MFLOPS OF MUSCLE



Popular VME-based platforms such as the Sun workstation can use the 25 to 100 MFLOPS of floating-point power in the Racer series of accelerator boards from Transformation Systems Inc. The boards are based on AT&T's DSP32C 32-bit DSP chip.

Single- and four-processor boards are now offered in the series. The VM1 single-processor model is targeted at memory-intensive applications. Its peak performance of 25 MFLOPS features a three-tier memory architecture that maximizes memory price-performance ratio. The first tier is the DSP chip's internal 6-kbyte static RAM. The second is 32 kbytes of fast, dual-ported static RAM, and the third is 1 Mbyte of static-column dynamic RAM, which is dual-ported between the DSP32C and the VMEbus.

To support I/O, the VM1 has a 16-bit parallel port and a buffered, bidirectional serial port. Both ports feature an independent DMA capability.

With its four DSP32C processors, the VM4 board peaks at 50 MIPS and 100 MFLOPS. By using up to 16 boards in one enclosure, system designers can achieve peak performance of 1.6 GFLOPS. Each of the board's four processors includes 512 32-bit words of zero-wait-state RAM. The board also carries from 32 to 128 kbytes of single-wait-state external static RAM for each processor. Programs executed out of the internal RAM achieve peak performance of 100 MFLOPS, while those executed out of external memory peak at 80 MFLOPS.

With 25-MFLOPS capability, 32 kbytes of static RAM, 1 Mbyte of dynamic RAM, and 512 kbytes of FIFO buffering, the VM1 board goes for \$6885. The VM4 board with 100-MFLOPS computing power, 32 kbytes of static RAM, and 1 Kbyte of

buffering costs \$8500. Delivery is in 30 days after receipt of order.

*Transformation Systems Inc.,
576 Fifth Ave., Suite 1103, New
York, NY 10036; (212) 221-5000.*

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CIRCLE 117

SMART DATA-COMMUNICATION PROCESSOR HANDLES MULTIPLE PROTOCOLS

Packing the intelligence of a 16-bit 68000 microprocessor, the 68302 integrated multiprotocol processor handles multichannel communication with HDLC/SDLC, Asynch, Bisynch, DDCMP (DECnet), and V.110/V.120 (CCITT) protocols as well as ISDN standards. Motorola's 68302 combines a 68000 CPU core for the system interface and a RISC-based processor to control serial-data transfers. Thanks to the fast RISC processor, any three protocols can be active simultaneously—one on each of the chip's three serial-communication channels.

When operating at a clock rate of 16 MHz, the 68302 transfers data at rates of 512 kbits/s over each of the three serial channels, with all channels operating independently. Higher rates are possible on one channel if one or both of the other channels isn't used. The RISC engine manages the three general-purpose multiprotocol serial-communication channels, and has six local DMA controllers to support the data streams going to and coming from the serial ports. Data transfers controlled by the DMA circuit can take place at up to 4 Mbytes/s.

The 68302 integrates most of the functions needed by any communication system. Its CMOS construction holds power consumption to just 400 mW when active and 50 mW when standing by. An 1152-byte dual-port RAM serves as a memory-mapped register bank through which the 68000 core communicates with the serial channels and other on-chip functions. Some of those functions include a DMA controller, two timers, and a watchdog timer.

Housed in a 132-lead surface-mountable flat package or pin-grid array, the 68302 costs less than \$55 in sample quantities (flat-pack) and is available from stock.

Motorola Inc., Microprocessor Products Group, 6501 William Cannon Dr. W., Austin, TX 78735-8598; (512) 891-2140.

CIRCLE 327

DAVE BURSKY

IC CONNECTS TO TWISTED-PAIR ETHERNET

Used to connect Ethernet LAN controllers directly to twisted-pair wire connectors, the 82521TA serial "supercomponent" (SSC) combines custom magnetics and discrete devices in a single dual-in-line package. The part contains the serial interface-transceiver, Manchester decoder, line drivers and receivers, analog filters, protection circuitry, isolation transformers, and other analog circuitry. By using industry-standard Ethernet controller and twisted-pair Ethernet (TPE) signals, Intel has the option to modify the SSC to conform to IEEE 10Base-T TPE standards once they are adopted by the IEEE committee. Thus, board vendors are assured of an upgradable, plug-in replacement that conforms to the 10Base-T standard. The price of the 82521TA SCC in 1000-unit quantities is \$66.

Intel Corp., Literature Dept. Y-P07, P.O. Box 58065, 3065 Bowers Ave., Santa Clara, CA 95051; (800) 548-4725.

CIRCLE 335

BOARD LINKS STEBUS WITH ARCNET LAN

An interface board provides STEbus system integrators with a communication structure for linking their systems with any of the more than 1.5 million installed Arcnet nodes. Designated the S-ARC-01, the board acts like an intelligent slave in the system. The base address can be selected to any 4-kbyte boundary within the short I/O base. Firmware provides sophisticated token-passing media-access control, as well as data link functions. These include CRC-16 check summing, buffer-free inquiry, and hardware acknowledge functions. Use of its 2.5-Mbit/s bandwidth approaches 98% under heavy data traffic conditions. The S-ARC-01 will also support future networks using the recently announced 20-Mbit/s Arcnet standard. Network drivers running under MS-DOS are included with the board. An optional NetBIOS implementation is also available. Single-unit pricing is \$858.

Delivery takes three to four weeks.

C&C Technology Inc., Bldg. 9, Unit 60, 245 W. Roosevelt Rd., West Chicago, IL 60185; (312) 231-0015.

CIRCLE 336

LAN IC DRIVES TWISTED-PAIR CABLE

An Arcnet LAN driver permits networking across standard twisted-pair cable at a fraction of the cost of Ethernet devices. Designated the HYC9088, the device can drive up to 400 ft of standard twisted-pair telephone cable. It attaches to the cable without disturbing its characteristic impedance, a fact that enables it to drive twisted-pair or coaxial cable in either star or bus configurations. The driver IC also includes an advanced filter circuit that reduces electromagnetic interference. In quantities of 5000, the HYC9088 costs \$14.50.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11788; (516) 273-3100.

CIRCLE 337

TRANSCEIVERS MEET MIL-STD-1553

Available in eight standard versions, a family of monolithic single- and dual-channel transceivers conforms to MIL-STD-1553A and 1553B requirements. The UT63M100 series is a fit- and function-compatible monolithic second source for the industry-standard 63100-series transceivers. Separate transmit and receive inhibit inputs allow independent control of each function. Receiver sections are compatible with MIL-STD-1553 levels from 0.86 to 14.0 V, and the power-supply voltage can range from 5 to 12 V or 5 to 15 V. Single-channel transceivers in 24-pin ceramic DIPs are priced at \$236 in lots of 100 units. In like quantities, the dual-channel versions cost \$367 in ceramic DIPs, \$378 in flat packs, and \$388 in small-outline configurations.

United Technologies Microelectronics Center Inc., Military-Standard Products Dept., 1575 Garden of the Gods Rd., Colorado Springs, CO 80907; (800) MIL-UTMC or (719) 594-8259.

CIRCLE 338

SWITCHES, SENSORS, AND ENCODERS

Presenting information on more than 35,000 items, this 200-page catalog covers six major product lines including inductive proximity switches, photoelectric sensors, ultrasonic sensors, encoders, capacitive sensors, and the patented My-Com mechanical switch. Technical specifications are given for each device, along with engineering diagrams, photographs, and part numbers.

Baumer Electric Ltd., 122 Spring St., Southington, CT 06489; (800) 937-9336 or (203) 621-2121.

CIRCLE 339

DATA BASE PERMITS COMPONENT SELECTION

An information system that can be interfaced with electrical CAE, CAD, CAM, and CAT systems provides a centralized bank of electronic component data. It consists of three products: DataMaster, Component Manager, and ViewMaster. DataMaster is a comprehensive data base of electronic components and attributes. Component Manager is a preferred component management system that restricts engineers to selecting only those components approved for their projects. ViewMaster enables component selection and retrieval from a listing of millions of components in just seconds. The system can be installed on most Unix, VMS, and DOS-based hardware platforms. It carries a base price of \$75,000, plus data subscription fees of \$50,000 per year per server.

Expert Views Inc., 175 Cabot St., Lowell, MA 01854; (508) 970-0880.

CIRCLE 340

ASICs PERMIT SURFACE-MOUNTING

To better illustrate its products, Motorola's MOS Digital-Analog Division is offering an informative catalog (BR503/D) featuring the company's extensive line of high-performance ICs in PLCC and SO packages. Listings cover surface-

mounted packages for both application-specific and telecommunication devices. These include analog-to-digital and digital-to-analog converters, decoders, display drivers, op amps, comparators, remote control functions, real-time clocks, and various telecommunication devices.

Motorola Inc., MOS Digital-Analog Integrated Circuits Division, P.O. Box 6000, Austin, TX 78762; (512) 928-6880 or call local sales office.

CIRCLE 341

INSTRUMENTATION DESIGN GUIDE

Complete with single-piece pricing and ordering information, an 84-page design guide and catalog presents information on 54 different instrumentation products. Devices covered include instrumentation amplifiers, operational amplifiers, an ac line voltage monitor, a constant-current module, and strain-gauge bridge signal-conditioning modules. The booklet also contains information on 97 different ac-dc modular encapsulated power supplies and dc-dc converters for use in instrumentation systems. Complete detailed specifications, circuit descriptions, a selection guide, 56 outline drawings, 82 block diagrams, and 22 performance curves are provided.

Calex Manufacturing Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523; (415) 932-3911.

CIRCLE 342



TEXT ADDRESSES NETWORK THEOREMS

A comprehensive textbook on network theorems is one of the first of its kind, discussing 45 theorems in its 160 pages. The presentation is divided equally between the periodic steady state and transients. Many of the problems are applied in the cisoidal state, with complex frequency aiding a quick solution. For fast reference, each problem solution is indexed with the list number of each

theorem used. The appendix centers on a number of useful techniques, including topics on matrices, two ports, initial conditions, and similar tabulations. *Useful Network Theorems With Applications* costs \$9.75, plus \$1.50 for shipping.

Sercolab USA, Box 767, E. Dennis, MA 02641;

CIRCLE 343

ICS PERFORM DSP, DATA CONVERSION

A 12-page short-form catalog provides a comprehensive overview of all of TRW LSI's monolithic and hybrid integrated circuits for video data conversion and digital signal processing. Separate sections within the publication detail the specifications for analog-to-digital converters, digital-to-analog converters, linear products, advanced arithmetic devices, imaging devices, correlators, transform products, and memory and storage components. Product listings specify key performance parameters, as well as operating temperature range, packaging, and screening options.

TRW LSI Products Inc., P.O. Box 2472, La Jolla, CA 92038; (619) 457-1000.

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DC POWER SUPPLIES AND ELECTRONIC LOADS

To help designers choose the right product for a given system or laboratory application, Hewlett-Packard's 144-page catalog provides full descriptions of the company's manual and computer-controlled dc power supplies and electronic loads. Supplies are grouped into three types: system, laboratory and industrial, and special-purpose. The section on system power supplies covers single- and multiple-output models capable of delivering up to 200 V, or up to 120 A and 1000 W, over the HP-IB interface. Electronic loads, used for power-supply, battery, and power-component testing, offer ratings from 300 to 1600 W.

Hewlett-Packard Co., Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; call local sales office.

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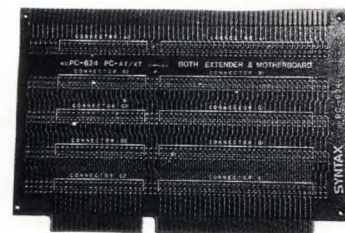


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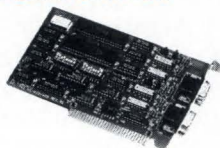
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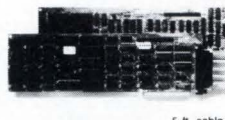
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See EEM 88/89
Page D-1304

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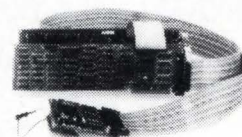
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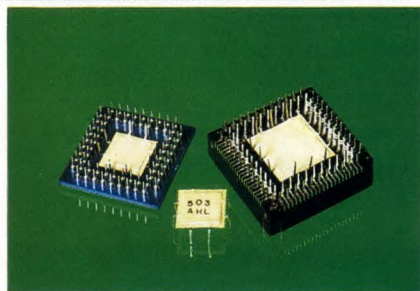
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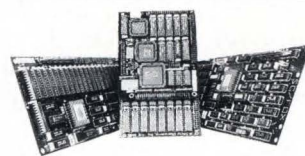
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NEW TOOLS FOR SIMULATION PRODUCTIVITY ENHANCEMENT

As seen in July 13 Electronic Design (pg. 101)

Sim-P/L - a Pascal-like behavioral language for generating stimulus files for simulators from Mentor Graphics, DASIX, Valid, OrCAD and others with extensions for test vector generation; and

SimComp - a program for complete functional and timing comparison of two simulation runs for best/worst-case and/or pre/post-simulation analyses.

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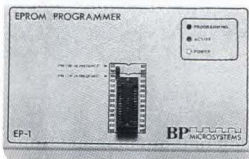
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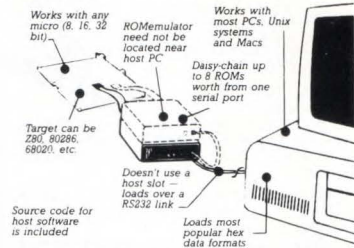
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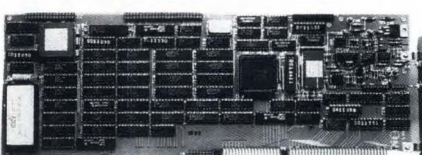
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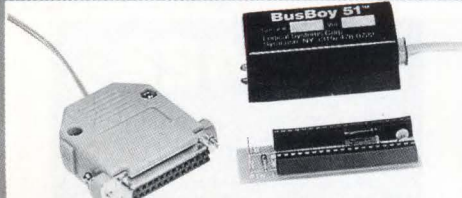


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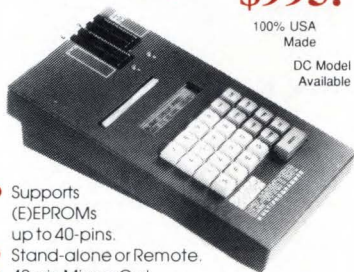
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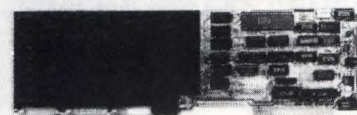
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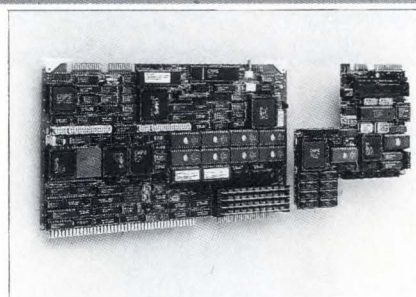
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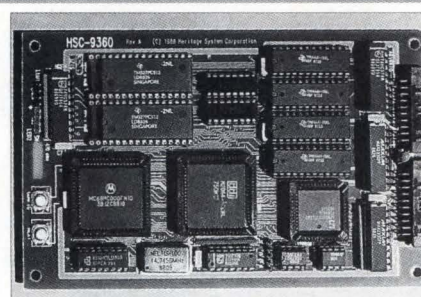
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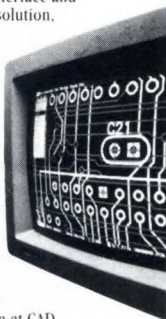
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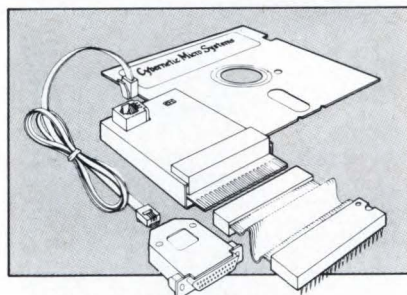
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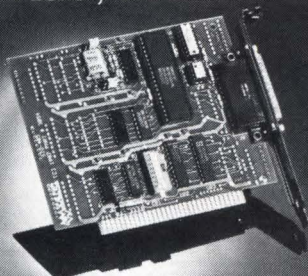
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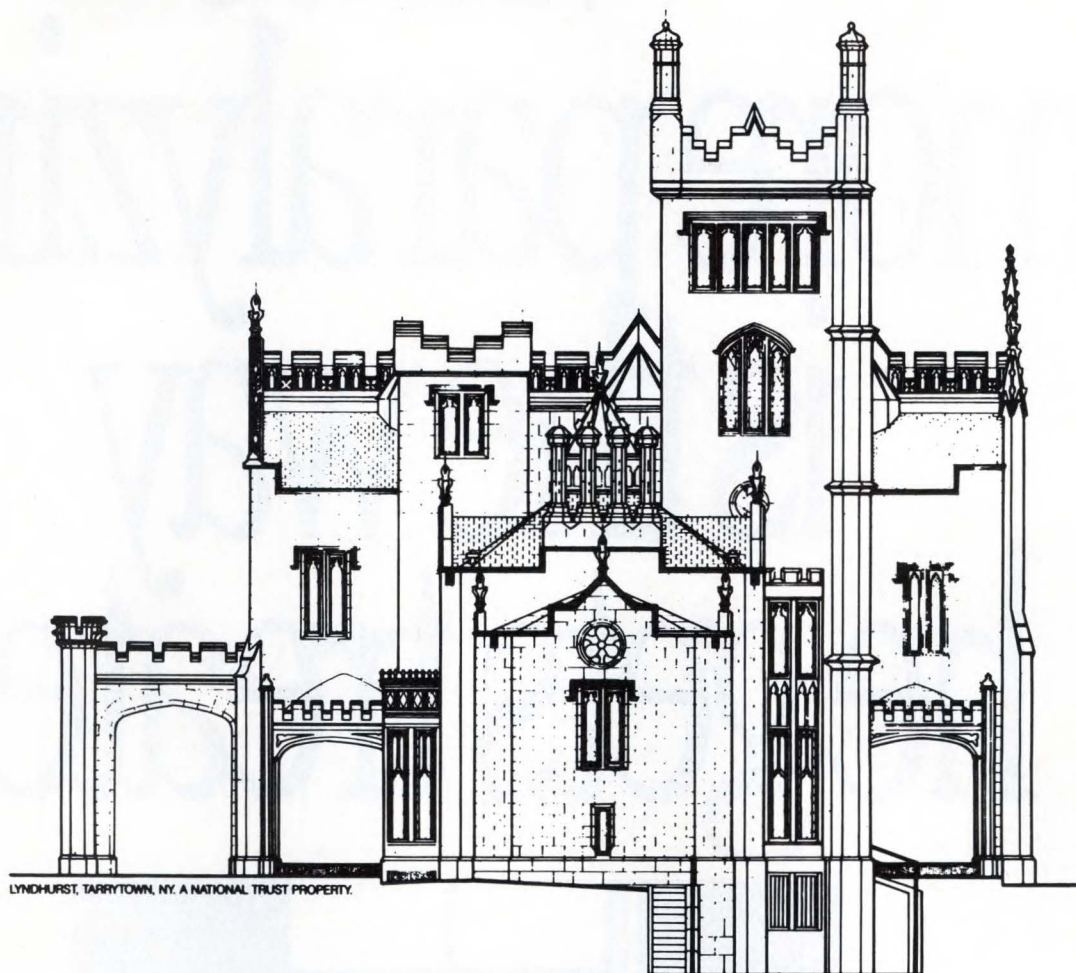


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LT1132	5	3	+5V	NO	YES	1µF
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ABSORPTIVE... REFLECTIVE

dc to 4.6 GHz from \$32⁹⁵₍₁₀₋₂₄₎

Tough enough to pass stringent MIL-STD-883 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only \$32.95, and the KSWA-2-46, at \$48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model	KSW-2-46	KSWA-2-46
Connector Version	ZFSW-2-46	ZFSA-2-46
FREQ. RANGE	dc-4.6 GHz	dc-4.6 GHz
INSERT. LOSS (dB)	typ max	typ max
dc-200MHz	0.9 1.1	0.8 1.1
200-1000MHz	1.0 1.3	0.9 1.3
1-4.6GHz	1.3 1.7	1.5 2.6
ISOLATION (dB)	typ min	typ min
dc-200MHz	60 50	60 50
200-1000MHz	45 40	50 40
1-4.6GHz	30 23	30 25
VSWR (typ)	ON 1.3:1 OFF —	1.3 1.4
SW. SPEED (nsec)		
rise or fall time	2(typ)	3(typ)
MAX RF INPUT (bBm)		
up to 500MHz	+17	+17
above 500MHz	+27	+27
CONTROL VOLT.	-8V on, OV off	-8V on, OV off
OPER/STOR TEMP.	-55° to +125°C	-55° to +125°C
PRICE (10-24)	\$32.95 \$69.95	\$48.95 \$79.95

finding new ways ...
setting higher standards

Mini-Circuits

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P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500

Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

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