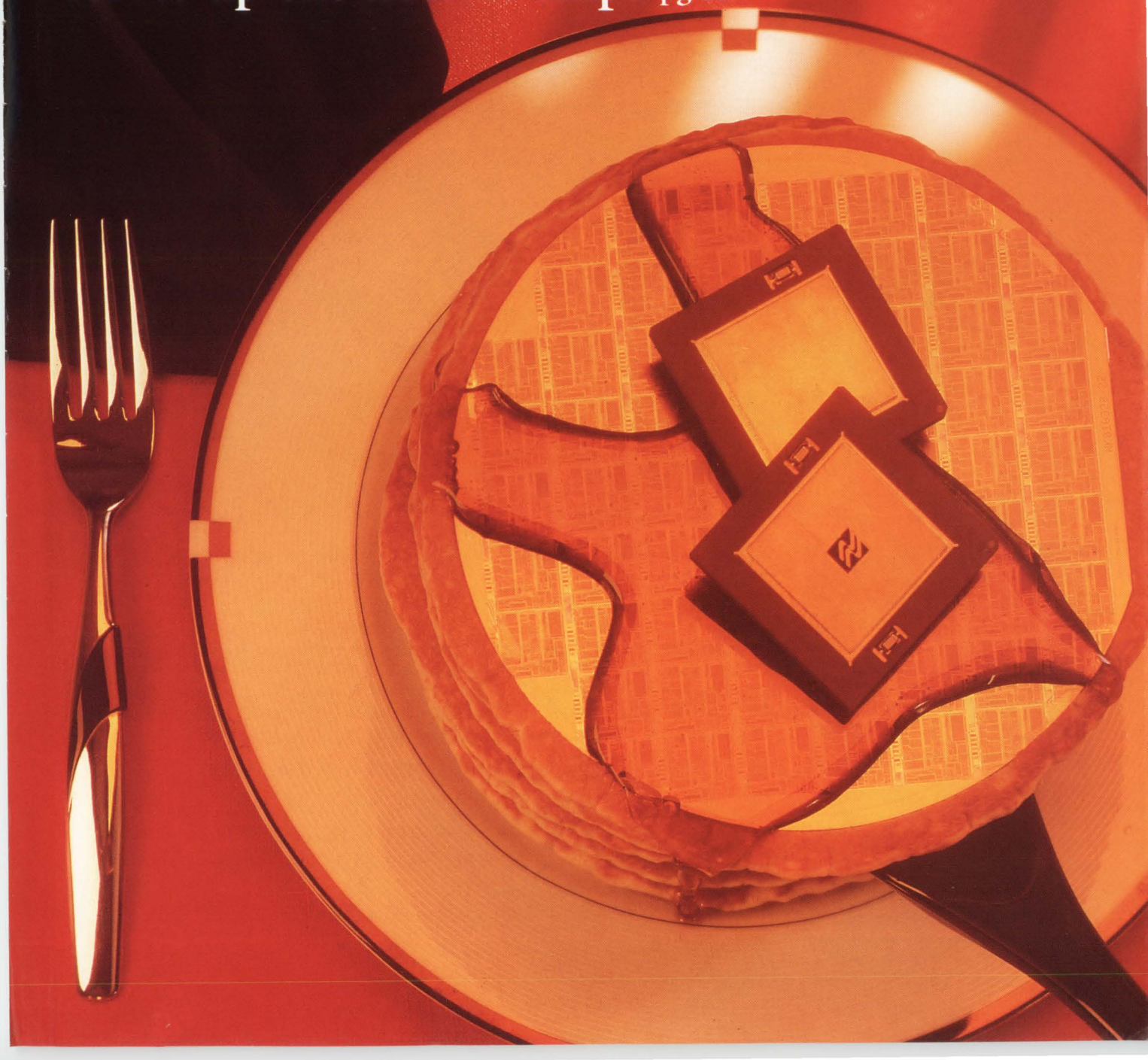
A CAHNERS PUBLICATION INTERNATIONAL EDITION NOVEMBER 21, 1991

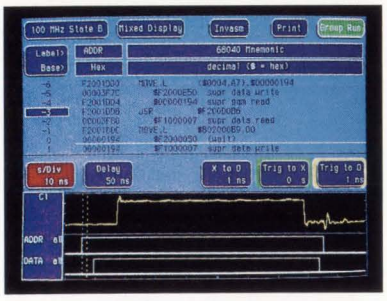
EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:
18th annual µP/µC directory serves up the hottest chips pg 82



Now catch the bugs that defy logic.



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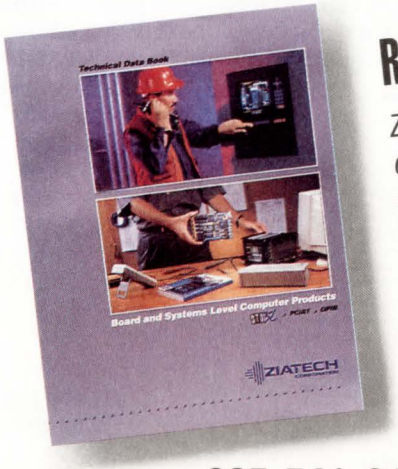

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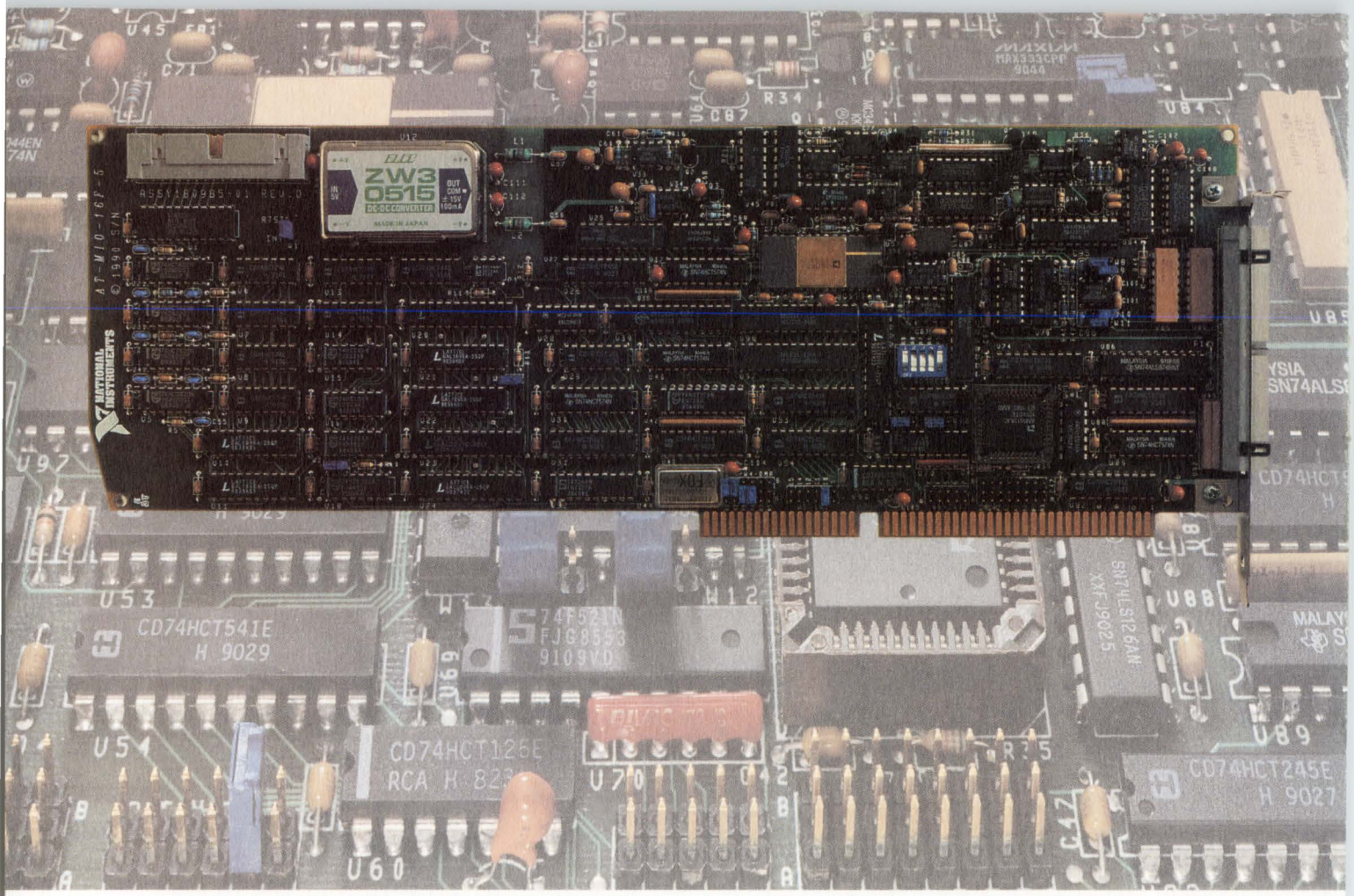

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Data Acquisition Board	Computer Bus	Channels*	Max Sampling Rate (samples/sec)	Analog Input: Resolution (bits)	Analog Input: Ranges (V)	Analog Input: Gains	Analog Output: Channels	Analog Output: Resolution (bits)	Digital I/O Channels	Counter/Timers	Software: LabWindows	Software: LabDriver for DOS	Software: LabDriver for Windows	Software: Measure	Software: VisionScope	Software: Third Party
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	–	–	–	–	✓	✓	✓		✓	
AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	✓	✓	✓			✓
AT-MIO-16H-9 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	✓ ✓	✓ ✓	✓ ✓	✓ ✓		✓ ✓
AT-MIO-16L-9 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	✓ ✓	✓ ✓	✓ ✓	✓ ✓		✓ ✓
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	✓	✓	✓	✓		✓
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	–	–	16†	3	✓	✓	✓			
AT-DIO-32F PC-DIO-96 PC-DIO-24	AT XT XT	– – –	– – –	– – –	– – –	– – –	– – –	– – –	32 96 24	– – –	✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓			✓ ✓
PC-TIO-10	XT	–	–	–	–	–	–	–	16	10	✓	✓	✓			

* SE – Single-Ended, DI – Differential, SS – Simultaneous Sampling † 8 Channels In, 8 Channels Out

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About all it doesn't do is generate arbitrary waveforms, but there's the Wavetek Model 95 Synthesized Arbitrary Function Generator for that.

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For more information about our multi-purpose function generators, high performance pulse generators, or test development and arbitrary waveform software, call Wavetek at 1-800-874-4835.

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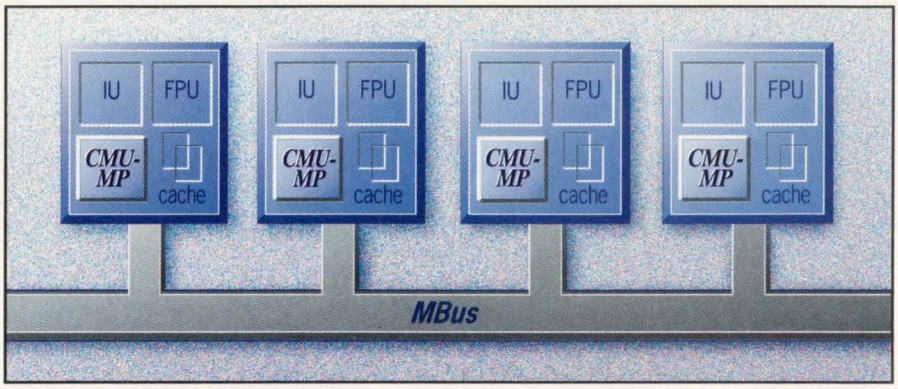
Multiprocessing RISC design is not simple. There are substantial technological challenges, particularly in the area of multi-level memory systems.

Now we offer a breakthrough to help you implement multiprocessing systems rapidly.

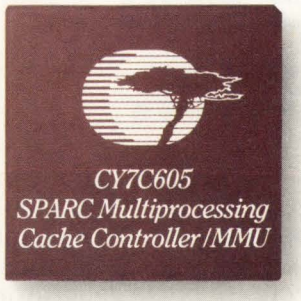


SPARC multiprocessing is now enabled. Now you can design-in multiple high-performance SPARC chipsets. Our revolutionary Multiprocessing Cache Controller and Memory Management Unit (CMU-MP/CY7C605) provides memory management facilities and a unique cache architecture for higher performance. Our complete SPARC chipset solution shortens your time to market.

Cache coherency without stealing processor cycles — a leap in performance.

Maintaining cache coherency is one of the biggest problems to solve in shared memory multiprocessing systems.

This approach solves it.



Pin compatible with our CY7C604 Uniprocessing Cache Controller/MMU, this new device lets you cascade to build cache size to 256K.

It is the only VLSI solution that performs concurrent bus snooping and processor execution.

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You get multiprocessing with the most efficient cache coherency protocol available, allowing data to pass from CPU to CPU in a single clock cycle. That translates directly to higher performance systems.

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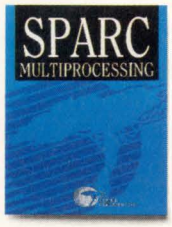
This VLSI solution means you don't have to design and pay for boards full of logic to accomplish fast multiprocessing.

It is all available now.

For more information on the industry's most complete multiprocessing solution, please call for our literature package today.



Multiprocessing Information Hotline: 1-800-952-6300.*
Ask for Dept. C4V.

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Volume 36, Number 24

EDN Magazine Edition

November 21, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Dig into EDN's 18th annual chip directory and find out how emerging chips use super techniques to surpass the performance of RISC processors. See our Special Report on pg 82. (Photo courtesy National Semiconductor; design and photography by Imagination)*

SPECIAL REPORTS

INNOVATION™ Driving Electronic Technology Into The Next Century

TECHNOLOGY UPDATES

Continued on page 7

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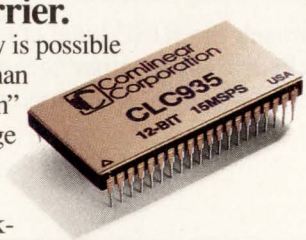
VBPA ABP

Because you're thinking fast...

Off-the-chart performance in a new 12-bit, 15MSPS A/D converter.

This one breaks the 74dB barrier.

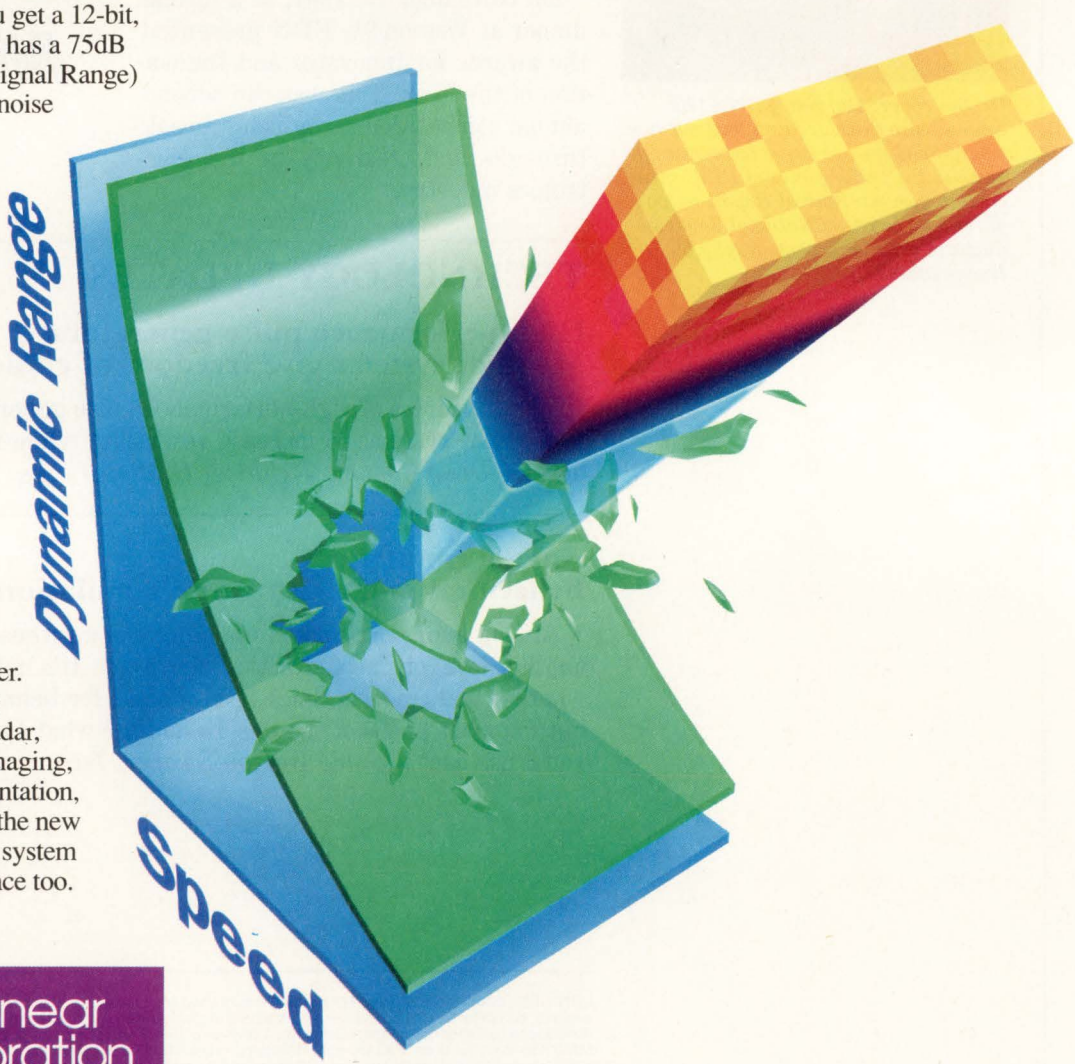


Yes, it really is possible to get more than 74dB of "clean" dynamic range from a 12-bit converter... without breaking the laws of physics.

The secret is in the track-and-hold design. And that's where the CLC935 excels. So you get a 12-bit, 15MSPS converter that has a 75dB SFSR (Spurious Free Signal Range) at 7.5MHz, a signal-to-noise ratio of 67dB out to Nyquist, 0.35 LSB differential non-linearity, and a 135MHz small-signal bandwidth. Now that's a true performance breakthrough in an A/D.

Before now, the only way you could get this performance was with large, expensive board designs. Now, it's available in a 40-pin DIP that takes less than 2.3 square inches of board space. And only 5.2W of power.

So if you're bumping against A/D limits in radar, infrared and medical imaging, ultrasound, or instrumentation, call for details. Maybe the new CLC935 can give your system off-the-chart performance too.



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EDITORIAL 35

Although electronics hardware from the Soviet Union is primitive by Western standards, there may be opportunities for the venturesome in software.

NEW PRODUCTS

DEPARTMENTS

NEXT IN EDN

In the November 28 EDN News Edition, look for a Product Watch on disk-controller ICs and a Career Opportunities article on Futurebus+ boards.

Then, get ready for products. And more products. It's that time again at EDN Magazine—time to review and evaluate the products and technological developments that have affected the electronics industry over the last half year. In EDN's two December International Product Showcase issues, we summarize the most significant products introduced since the July Showcases—some are new, some we've covered before in EDN.

The December 5, 1991, Showcase will cover products and issues in four technology areas: hardware and interconnect devices, integrated circuits, power sources, and software. In our second Showcase, December 19, 1991, we'll switch the focus to components, computer-aided engineering, computers and peripherals, and instruments.

You'll also find many of our regular departments as well as expanded literature coverage.

It's Also More Power

Introducing The 40MHz Am386™ Microprocessor— The Speediest 386 On The Planet.

It looks like a mild mannered 386. In fact, it is: A genuine, plug-in replacement for the i386. Except it's faster. Burns less power. Costs no more. And it's available now.

The Am386DX-40 microprocessor can transform any ordinary 33MHz system into an invincible, 25% faster, 40MHz Am386 system. So you can easily offer the world's fastest 386 performance.

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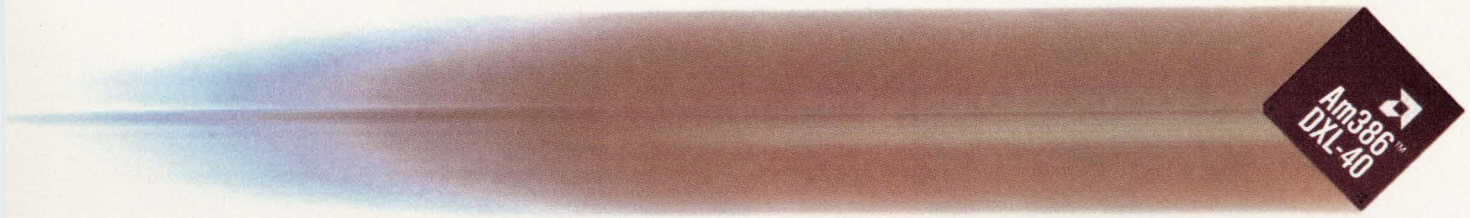

ful Than A Locomotive.

operation. That means even notebooks and palmtops can attain breakthrough performance.

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So find a phone booth and call AMD at **1-800-222-9323.** And let the world's fastest 386 come to your rescue.

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If you think DSPs are priced Our TMS320 family starts at

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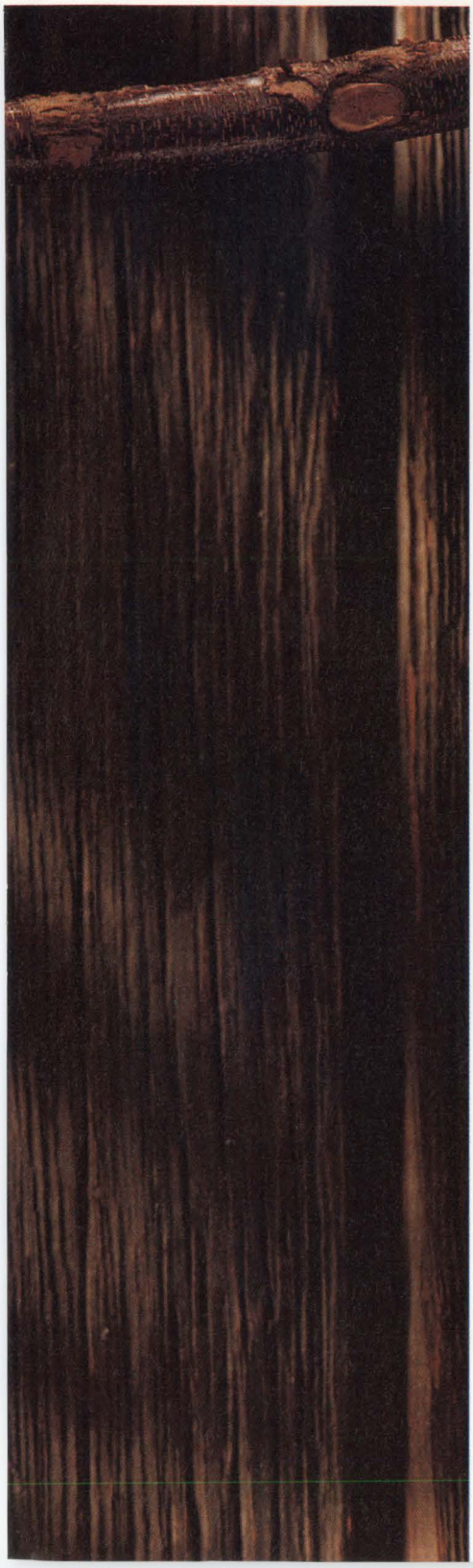

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16-bit DSPs as low as $3

Our 16-bit, fixed-point solutions begin at $3. At that, they are on a price par with microcontrollers and are as easy to use, yet give you 10X the performance.

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32-bit DSPs starting at $25

You can get floating-point performance at a fixed-point price. Starting as low as $25, our 32-bit floating-point DSPs are finding widespread use in embedded, cost-sensitive applications. Performance is superior to RISC processors because of highly paralleled architectures.

In addition to a low unit price, several features contribute to overall cost-effectiveness. These devices are inherently easy to use and are optimized for use with high-level-language compilers, which helps you get to market faster.

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In the 10 years since TI introduced its first single-chip DSP, we have shipped tens of millions of these devices worldwide. And we have applied the principles of manufacturing excellence learned from our commitment to DRAM manufacturing. This has resulted in the economies of scale that enable us to provide you with true value and dependable prices.

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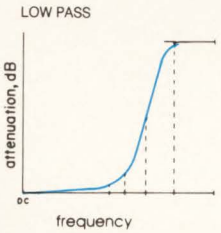

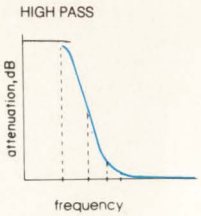

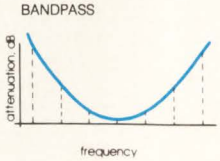

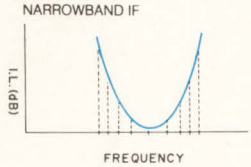

low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz (loss <1dB) Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	STOP BAND, MHz (loss > 10 dB) Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	STOP BAND, MHz (loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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Francois Grillot,
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Sandy Hirschhorn,
Director, Design Automation and Diagnostics
Stratus Computer

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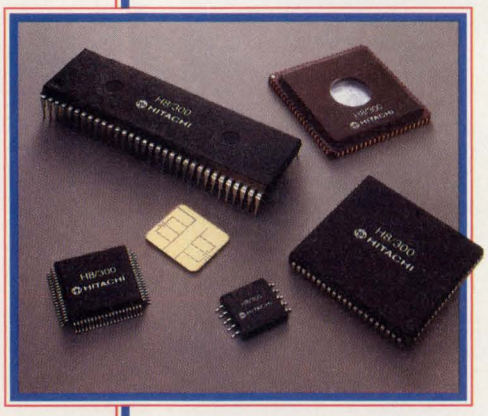

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ROM/RAM/EEPROM	10K/256/8K	8K/256/0	16K/512/0	24K/1K/0	32K/1K/0	16K/512/0	32K/512/0
Timers		3				5	10
Serial Channel		2				1	2
A/D Converter						8-Bit, 8 Channel	8-Bit, 16 Channel
Interrupts		4 External 16 Internal				9 External 19 Internal	9 External 47 Internal
I/O Ports	1-Bit I/O Common	47 I/O 4 Input Only				58 I/O 8 Input Only	50 I/O 16 Input Only
Other Features	Security Function	Parallel Handshake Port Programmable Pull-up for All I/O				15-Byte DPRAM, Prog. Pull-up for I/O	One 19-Bit Timer, Timer Network
Package	Die Form COB* SOP-10	DP-64S QFP-64 DC-64S w/Window				PLCC-84 QFP-80 LCC-84 w/Window	PLCC-84 QFP-80 LCC-84 w/Window

*Call your Hitachi representative for availability.

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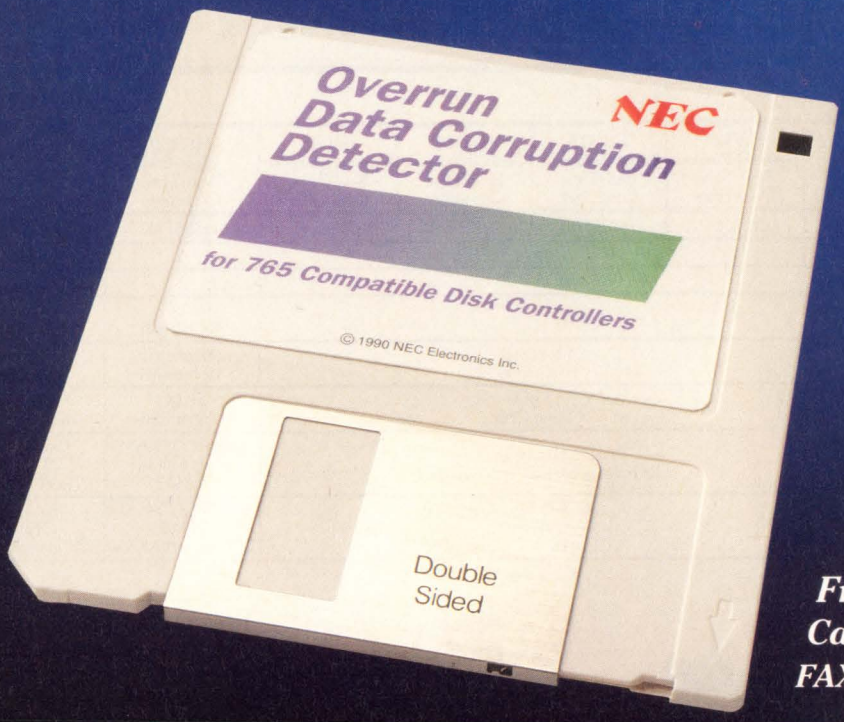

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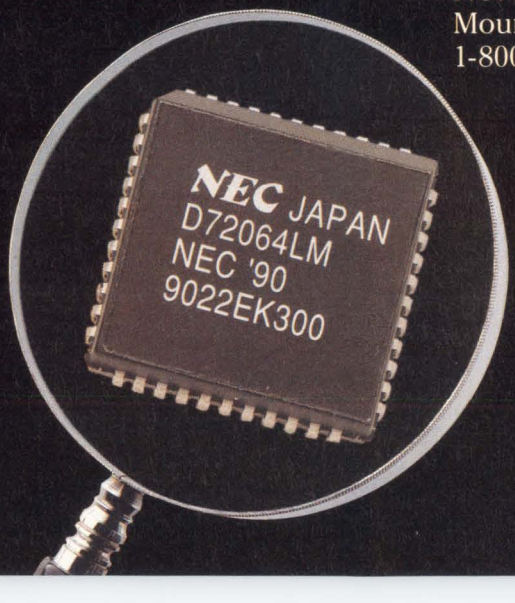


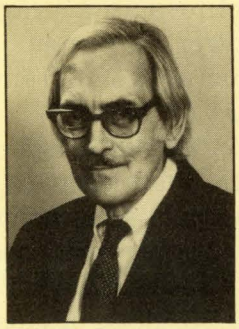
CIRCLE NO. 26

NEC

NEWS BREAKS

EDITED BY SUSAN ROSE

EDN LOSES AN EDITOR AND FRIEND



Chris Terry, EDN technical editor, died in late October after a 9-month fight with cancer. Chris came to EDN in January of 1985 as EDN's software editor, the last stop in his 25-year technical-writing career. He wrote articles for Microsystems, Creative Computing, and PC Magazine, as well as technical documentation for a number of private companies. Born near London, England, Chris grew up in Cambridge and graduated from Queen's College. In 1958, Chris visited the United States and immigrated four months later.

Chris was a fan of Monty Python movies and Far Side cartoons and extended his love of humor to those around him. He was always happy to take the extra time to help out his colleagues. Not only was Chris knowledgeable and articulate about the subjects he covered, but he was also a good friend to everyone on the EDN staff. His presence will be sorely missed.—EDN Staff

8-BIT RISC μC OFFERS SPEED AT LOW COST

The PIC 17C42 8-bit microcontroller (μC) from Microchip executes most of its 55 instructions in a single 250-nsec cycle on the 16-MHz version. Program branches and special instructions for transferring data between program and data memory take more than one cycle. The μC uses a pipelined, dual-bus, modified Harvard architecture with an 8-bit data word and a 16-bit instruction word. Program memory on chip is 2k × 16 bits, and you can add as much as 64k × 16 bits off chip. There are 280 data-memory locations available on chip in static RAM. The chip offers as many as 33 user-configurable I/O pins and includes two PWM outputs, 11 interrupts, three 16-bit counters, and a USART serial port. The μC is available as a CMOS EPROM or in a one-time-programmable plastic package. Samples are available now and production quantities will be available in February 1992 for $6.25 (10,000).

The company is also introducing the Picmaster development system, which supports the new chip and previous μCs from the company. The development system runs under Microsoft Windows 3.0 and provides real-time in-circuit emulation. The complete development system, including device programmer, is $2995. Microchip Technology Inc, Chandler, AZ, (602) 963-7373, FAX (602) 899-9210.—Doug Conner

ACCELERATOR SPEEDS VHDL

You can couple Vantage Analysis Systems' VHDL (VHSIC Hardware Description Language) simulator to Zycad's XP hardware accelerator under an agreement between the companies, improving your gate-level VHDL-model simulation. The agreement is effective as of December 1991. The agreement shows a continued move toward tighter integration between software simulators and hardware accelerators. Such integration began over the summer with agreements between Cadence, Synopsys and Zycad, and Racal-Redac and Ikos (EDN, June 20, 1991, pg 20). A word of caution about having reasonable expectations, though: Hardware acceleration is most effective on gate-level models; its impact on behavioral models is minimal. Vantage Analysis Systems, Fremont, CA, (415) 659-0901. Zycad Corp, Menlo Park, CA, (415) 688-7400.—Michael C Markowitz

NEWS BREAKS

LOW-POWER RISC TARGETS EMBEDDED CONTROL

VLSI Technology is now offering both stand-alone devices and ASIC cores based on the low-power ARM6 (advanced RISC machine) 32-bit processor developed by ARM Ltd (Cambridge, UK). The core processor uses a 20-MHz clock to achieve an average 14-MIPS performance, yet consumes only 0.2W. You can further lower its power consumption by freezing the clock when the processor is idle, reducing its current draw to <10 μA. The company is offering the core processor as part of its ASIC library. It is also offering two stand-alone products: The ARM60 (VY86C060) is a $26.75 (10,000) packaged version of the core processor in a 100-pin quad flatpack (QFP). The ARM600 (VY86C600) contains the processor, 4 kbytes of cache memory, a write buffer, and a memory-management unit designed to support object-oriented programming. It also offers a coprocessor interface, letting the devices work with floating-point units. It is packaged in a 160-pin QFP and costs $65.25. Both devices feature JTAG boundary-scan on the I/O pins.

ARM Ltd will license its design to OEMs wishing to design custom controllers. The company also offers development tools that run on the SPARC workstation. VLSI Technology, San Jose, CA, (408) 434-7877, FAX (408) 434-7931, contact John Haller. ARM Ltd, (408) 399-5195, FAX (408) 399-5196, Tim O'Donnell, or in the UK, 223-813000, FAX 223-812800, Robin Saxby.—Richard A Quinnell

SWIVELING CURSOR POSITIONER MATCHES LAPTOP ERGONOMICS

Zirco's Palmpoint cursor-positioning device employs a swiveling design to translate operator movements into cursor-positioning information. The device tilts side to side and front to back, creating a 2-D control plane. Because it employs tilt angles instead of translational movement, the Palmpoint uses far less desk space than a mouse. Unlike a trackball, the Palmpoint provides you with absolute-positioning feedback: its tilt angles indicate the cursor's position. The initial version is designed for PCs. It has a 4-ft cord that plugs into a 9-pin serial port and draws less than 7 mA from either a 5 or 12V power supply. The positioner costs $169.95 with software drivers. Zirco Inc, Wheat Ridge, CO, (303) 421-2013, FAX (303) 423-8346.
—Steven H Leibson

SOFTWARE SUITE SYNTHESIZES VHDL AND TEST LOGIC

The ASIC Navigator from Compass Design Automation synthesizes logic for implementation and behavioral VHDL (VHSIC Hardware Description Language) for documentation. The software synthesizes the logic by accepting circuit descriptions in forms ranging from Boolean expressions, bubble diagrams, schematics, architectural block diagrams, and VHDL statements. The logic synthesizers come in flavors optimized for specific functions; ROM and RAM compilers, datapath compilers, and state-machine compilers. Using your recommendations, the software also synthesizes and inserts test structures that enable such test methods as boundary scan, internal scan, built-in self-test, and multiplexed isolation. Using these structures, the software can create test vectors to adequately evaluate the design's manufacture. The software assists in partitioning your design across multiple packages using such constraints as gate- and pin-count, packaging alternatives, and board limitations. Including the optional test assistant, the software costs between $140,000 and $150,000 and runs on DEC, HP, and Sun workstations. Beta software will be available in early 1992; full release is scheduled for the second quarter. Compass Design Automation, San Jose, CA, (408) 434-7943, FAX (408) 434-7820.—Michael C Markowitz

New Schematic Capture Front End for PSpice

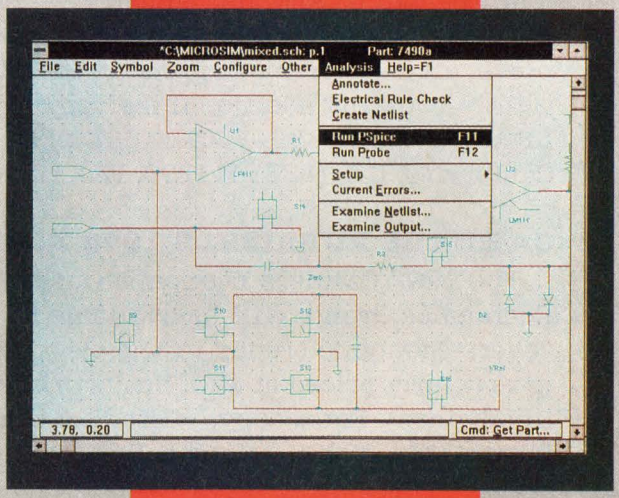
MicroSim Corporation now offers a versatile schematic capture front end, called Schematics, to our popular Circuit Analysis programs, PSpice and Probe. Schematics provides a unified system for designing and editing schematics, running analyses using PSpice, and viewing the results using Probe, all without leaving the Schematics environment. Any mix of analog and digital components can be used when defining a schematic for simulation.

Schematics provides a menu-driven interface for specifying analysis parameters and running simulations directly from the schematic display. If device simulation parameters need adjustment after running a simulation, they can be easily modified and the simulation rerun. Netlists for PSpice are generated automatically and can be examined on the screen.

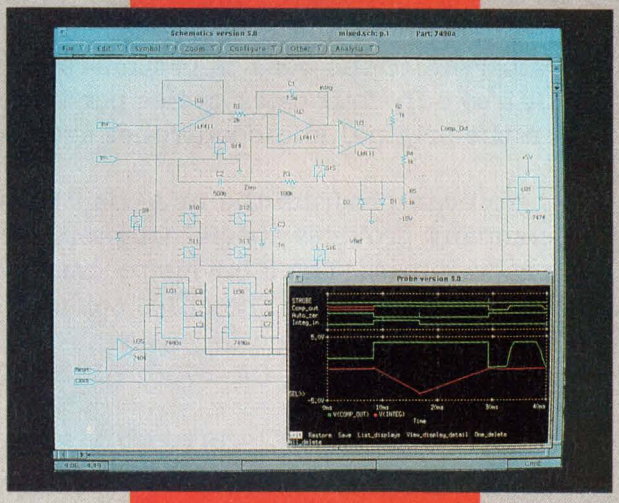
Schematics was designed and written as a native Windows 3.0 application for the PC and is also available as an OpenWindows application for the Sun-4 and SPARCstation. Both packages include the Schematics library with symbols for all parts contained in the PSpice libraries— over 3,500 analog and 1,500 digital components. An integrated symbol editor with full editing capability allows new symbols to be created and new part attributes to be defined while working on a schematic.

Schematics is sold as part of the Genesis package and comes with MicroSim Corporation's extensive customer/product support. Our expert engineering team is always on hand to answer your technical product questions.

For further information on Schematics, or any other MicroSim Corporation product, call toll free at (800) 245-3022 or FAX at (714) 455-0554.



Schematics as a Windows 3.0 application



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NEWS BREAKS

VMEBUS PROCESSOR TARGETS REAL-TIME APPLICATIONS

The VSCIM486 from Arcom is a VMEbus processor board that uses either a 20-MHz 80486SX or a 25- or 33-MHz 32-bit 80486DX CPU. The board is compatible with VMEbus and STEbus systems. The computing subsystem includes 4-Mbytes of dynamic RAM (DRAM) as standard, which is expandable to 64-Mbytes using a local module interface. 2-Mbytes of the DRAM is dual-ported to a VME bus. Another local module interface lets you build-in a direct-mapped memory cache of as much as 256 kbytes. Other hardware includes 128 kbytes of battery-backed static RAM (SRAM) (dual-ported to STEbus), super VGA controller with 1-Mbyte video RAM, floppy- and hard-disk controllers, and battery-backed clock. In addition to standard PC-type I/O ports, an 8- or 16-bit expansion interface is accessible via on-board connectors for tightly coupling additional memory or I/O peripheral hardware. VSCIM486SX (4-Mbyte DRAM) costs £1850, VSCIM486DX (33 MHz) costs £2890. Arcom Control Systems, Cambridge, UK, (223) 411200, FAX (223) 410457. In US, (816) 941-7025.—Brian Kerridge

CAHNERS PUBLISHES 1992 ECONOMIC OUTLOOK

The 1992 Cahners Economic Outlook, a yearly industry forecast from Cahners Economics Group, will be available to EDN readers in mid-December. The publication covers economic trends in the electronics and other technical industries. The booklet is regularly priced at $75, but is offered to readers for $21 (paid to Cahners Economics in advance). For a copy, write to Cahners Economics, Box 59, New Town Branch, Boston, MA 02298.—Susan Rose

ONE-TIME-PROGRAMMABLE MICROCONTROLLER JOINS FAMILY

Oki Semiconductor is extending its nX microcontroller line by adding a one-time-programmable version. The MSM65524/65P524 is built around the company's nX850 8-bit core processor, and it adds the one-time programming ability to the already available ROM and ROMless versions of the controller. The CPU is an extension, or superset, of the 8051 microcontroller architecture. The redesigned processor requires only four clock cycles per instruction cycle, as compared with 12 clock cycles in the original microcontroller architecture.

You can program the microcontrollers with standard device programmers. The company provides special adapters for programming the chips in standard PROM programmers. The 8-bit microcontrollers have 4-, 8-, or 16-kbyte ROMs, and 128 or 384 bytes of RAM. The chips come in 40-pin DIPs, 44- and 68-pin plastic leaded chip carriers, and 44- and 64-pin quad flatpacks. Prices start at $6.51 (1000). Oki Semiconductor, Sunnyvale, CA, (408) 737-6352, FAX (408) 720-1918.—Ray Weiss

DUAL-CHANNEL SCSI IC SUPPORTS WIDE AND FAST TRANSFERS

The AIC-7770 SCSI-I/O channel IC targets EISA- and ISA-based PC-mother-board applications. Adding the IC to a mother-board design requires no glue logic. The IC can handle data transfers to the host CPU at the EISA bus' maximum rate of 33 Mbytes/sec. The IC includes a dual-channel SCSI implementation that you can use as two independent 8-bit SCSI ports operating as fast as the 10-Mbyte/sec synchronous rate. You can also combine the two channels to implement a 16-bit SCSI port. The CMOS device comes packaged in a 160-pin quad flatpack and costs $55 (100). The company also has driver-software modules that provide compatibility with MS-DOS, Novell Netware, Unix, and OS/2 operating systems. Adaptec Inc, Milpitas, CA, (408) 945-8600, FAX (408) 262-2533.—Maury Wright

PROFILES IN PARTNERING

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UNITS INVOLVED: TTI, Inc., Angstrohm, Dale Electronics, Jeffers, Nytron, Ohmtek, Techno, Ultronix and Vishay Resistors.

In recent years, distributors have assumed greatly increased responsibility in the electronic component supply chain. Because of this, their ability to monitor, control and improve quality has become a pivotal factor in the cost of acquisition. These facts are well recognized in the successful distributor/manufacturer partnership which exists between Vishay Electronic Components (VEC) and TTI.

The two organizations have a close working relationship dating back to 1974 when Dale® resistors became one of the first products distributed by TTI. Since then, Dale together with Vishay Resistors, Angstrohm, Ohmtek, Techno and Ultronix have become part of VEC—and part of TTI's growth pattern as well.

VEC centralized its distribution headquarters for all six companies in Columbus, Nebraska, to make this consolidation more efficient for its distributors and customers. Concurrently, TTI and VEC accelerated work on standardizing packaging and other labor-intensive areas which could provide more efficient product flow-through at the distributor level. As part of this, use of electronic data interchange (EDI) was expanded together with a system for verifying the accuracy of order entry and processing.

In assessing the results of this activity, a VEC spokesperson commented: "In many cases, it's administrative errors, rather than product defects, which create major 'spikes' in cost of acquisition. So we work closely with all our distributors to support their ability to deliver the specified part in the right quantity with the correct packing at the right time."

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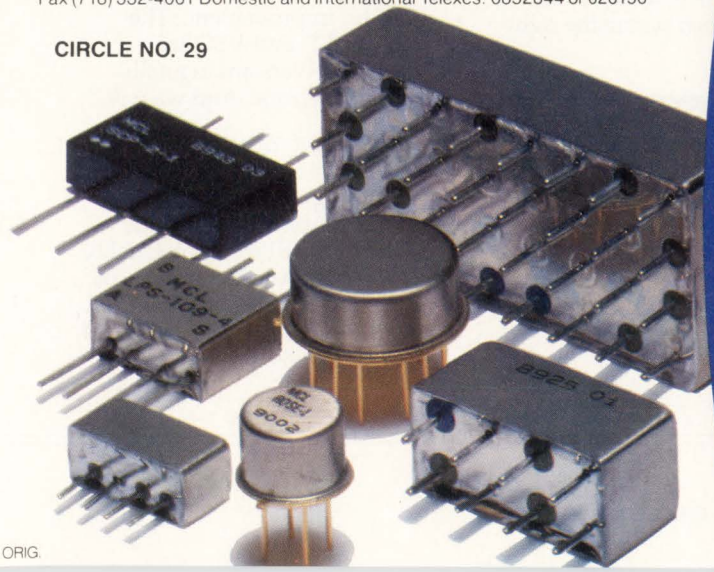

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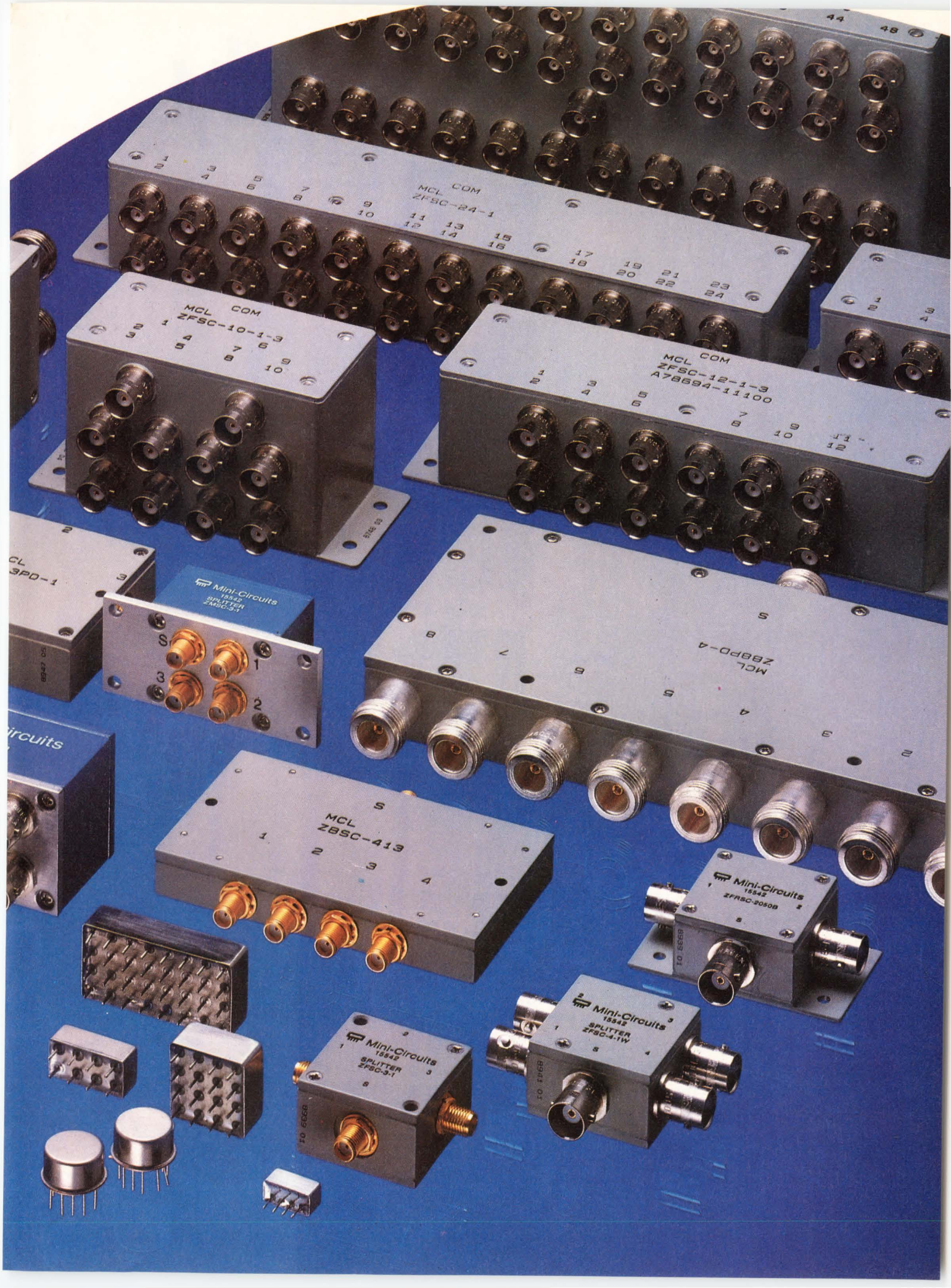
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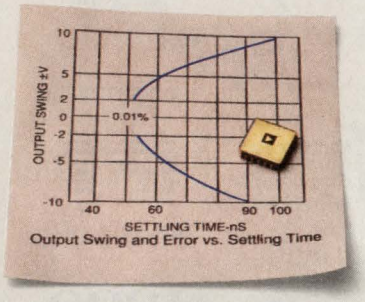

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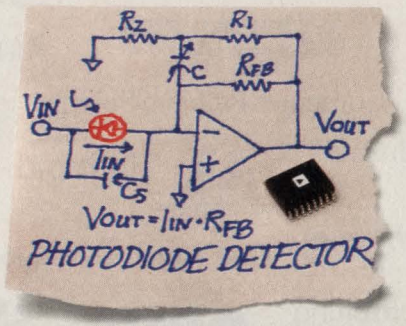
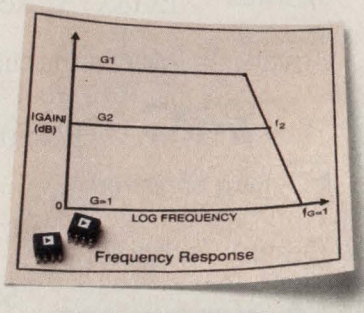
With the AD840, AD841 and AD842, there's no need to trade speed for accuracy. All three settle to 0.01% within 100 ns (840/842) and 110 ns (841) – critical in data acquisition and instrumentation applications – and offer low offset voltages and drifts, and fast slew rates.



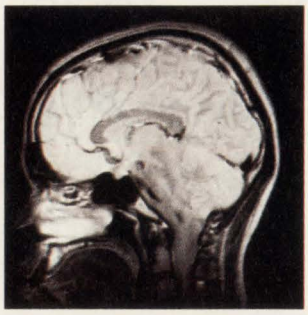
FET Input

For op amps requiring low input current, the OP-42, OP-44, AD845 and AD843 are all remarkably fast – slew rates are 58, 120, 100 and 250 V/μs, respectively. In addition, they offer offset voltages of less than 1 mV and extremely low current noise.



Transimpedance Amplifiers

The OP-160, OP-260, AD844, AD846, AD9617 and AD9618 all utilize a current feedback architecture to achieve slew rates from 450 to 2000 V/μs without compromising stability – even in hostile environments. Other benefits include low power dissipation and high unity-gain bandwidth.



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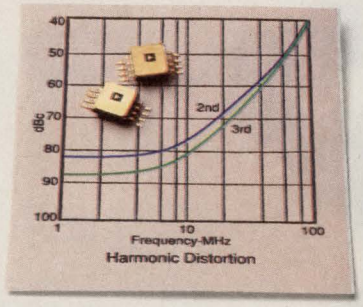
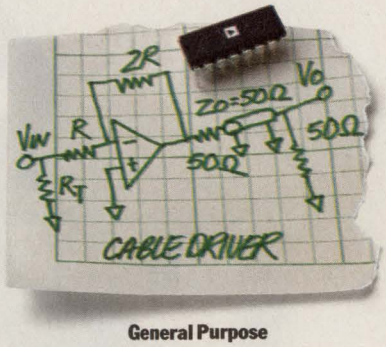
high-speed op amps.



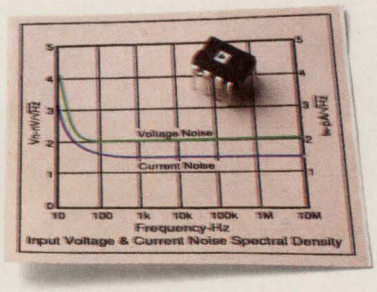
Buffers

If you're looking for extremely low distortion buffers, look at the specs of the AD9620 and AD9630 – distortion at 20 MHz: −73 dBc and −66 dBc, respectively; fast settling time: less than 8ns to 0.02%; and extremely low noise: 2.2 nV/√Hz.



General Purpose

With the right combination of speed, precision, power dissipation and high output drive capability, the AD827, AD829, AD847, AD848, AD849 and OP-64 are ideal general purpose solutions. And they're ideally priced solutions – most singles are under $3, and duals are under $5.



Low Noise

It used to be you had to choose between speed or low noise. But with the AD829, you get both. It features voltage noise of 2 nV/√Hz and current noise of 1.5 pA/√Hz with a 50 MHz unity-gain bandwidth. Those specs, combined with the low price of $2.95/100s, make it ideal for both audio and video applications.

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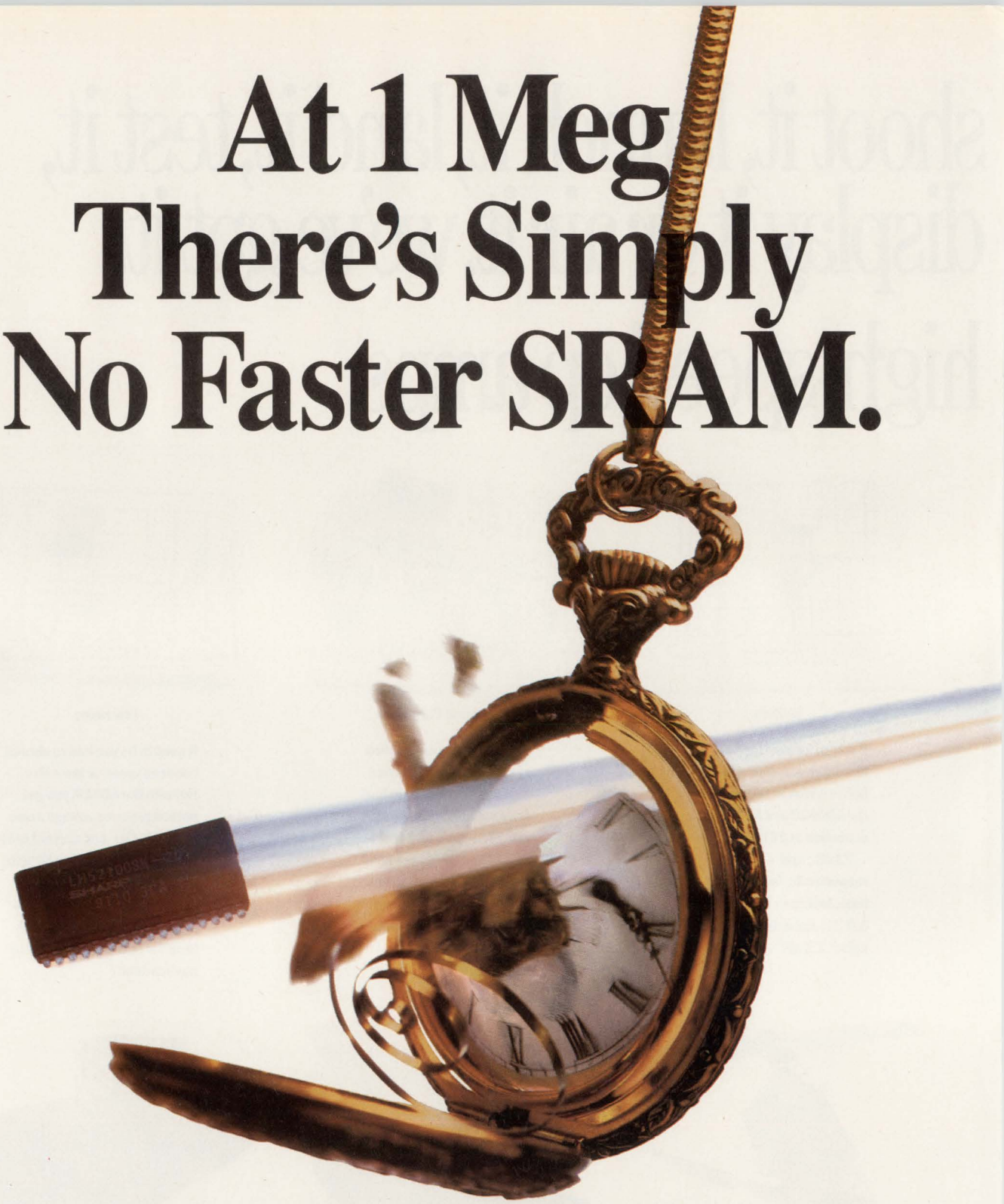

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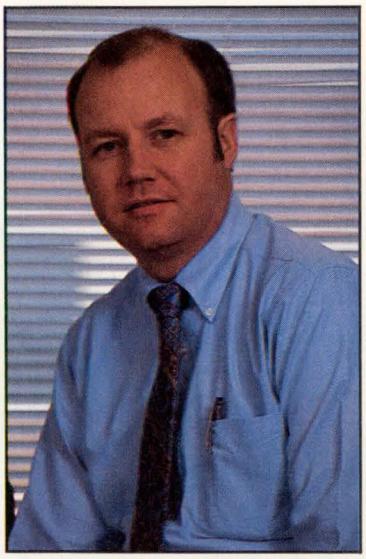
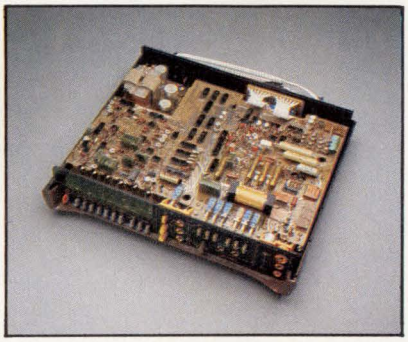
EDITORIAL

USSR electronics; it's not hardware



A few days ago I listened to Lester Thurow, an economist from the Massachusetts Institute of Technology, tell an audience about the state of private farms in the Soviet Union. Recently, Ukrainian agricultural administrators asked farmers if they wanted to run their own farms. Almost all of the responses were "No." Puzzled, the administrators asked why not. The farmers responded that they could not get any tractors, so they wouldn't be able to farm. "Even if tractors were available, where would we get the gasoline, the tires, and the spare parts?" they asked. In short, the Soviet's farming infrastructure is a mess.

The Soviet Union's electronics industry may have progressed further than farming, but it, too, still has a long way to go. During the summer, a friend of mine returned from the Soviet Union bearing an electronic instrument (photo). Several would-be entrepreneurs gave it to him and asked him to find a market for it in the US. The instrument does a credible job of measuring frequency, voltage, resistance, current, impedance, and other electrical quantities.



Unfortunately, the innards of the instrument appear to be relics of the late 60s or early 70s. Almost all of the circuitry uses discrete components—op amps and small-scale integrated circuits. At first, the circuit looks deceptively simple. Then it becomes clear that the control and display circuits require an additional pc board located below the top board that supplies the analog circuits.

In addition to the "low-tech" circuits, there are other features worth observing. Today's instruments routinely use liquid-crystal displays, but the Soviet instrument employs discrete vacuum-fluorescent tubes, each of which has been hand soldered to the circuit board. The injection-molded plastic case is primitive as are the push-button switches and other controls. Obviously, few Western engineers, technicians, or students will give up their modern instruments for primitive ones. The Soviet entrepreneurs face a difficult time locating markets.

In the same vein, many Western companies find it primitive doing business in the USSR—or what will be left of it. However, all may not be gloom and doom; there are islands of commercial hope. The USSR has some top-notch computer programmers, and it's possible for innovative companies to tap those resources. Given the shifting Soviet emphasis from defense to consumer products, more excellent programmers could be available for contract work. Software crosses international boundaries easily, and the initial investment in capital equipment for programmers is modest.

We don't see a wholesale shift of programming projects from Western countries to the USSR, but we do see the opportunity for entrepreneurs to make money by organizing programming ventures. US programmers shouldn't worry, however. With the increasing software content of all products, there should be plenty of work to go around.

Jon Titus
Editor

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.

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1990 Certificate, Best Series
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1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

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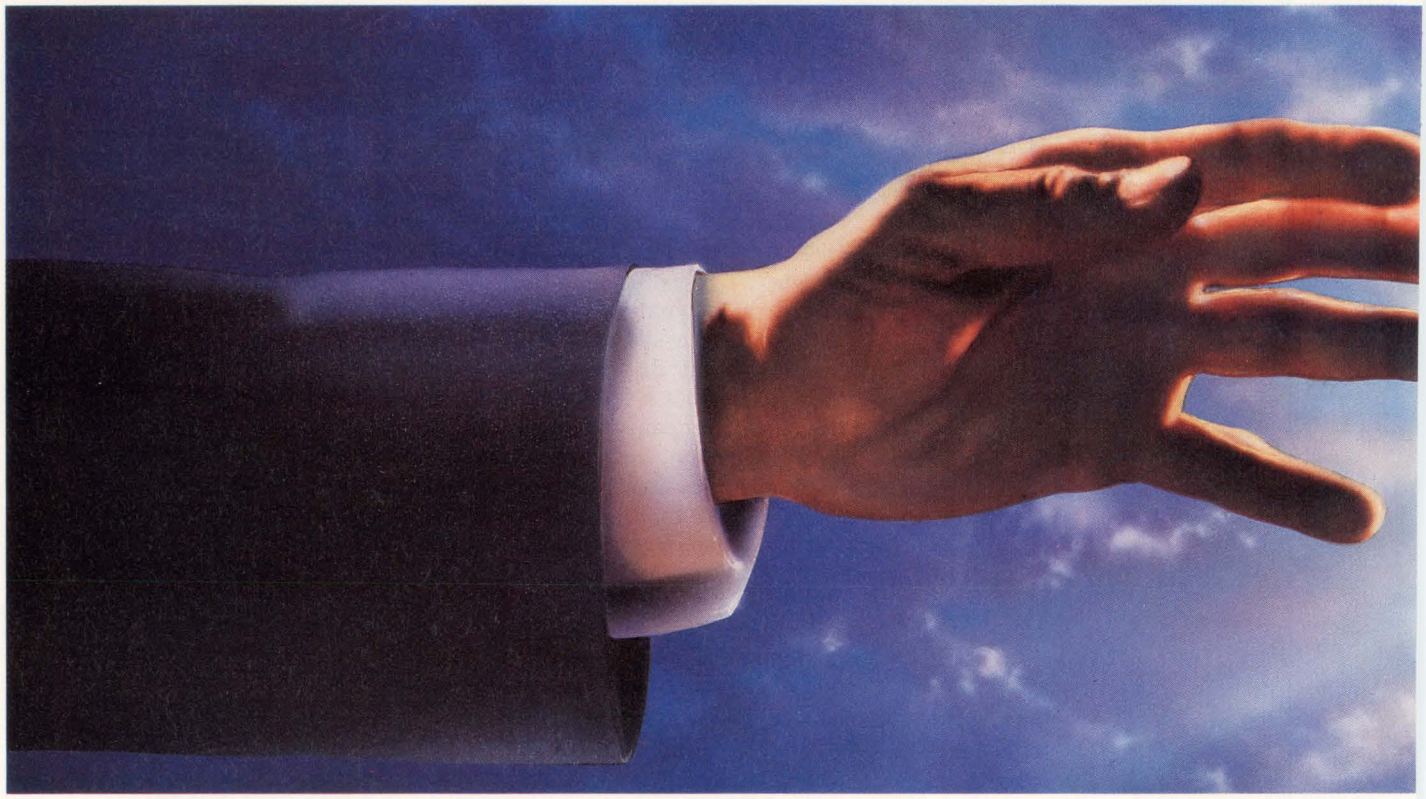

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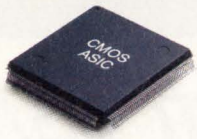

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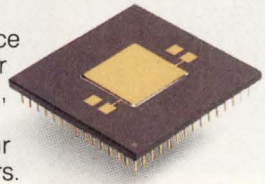

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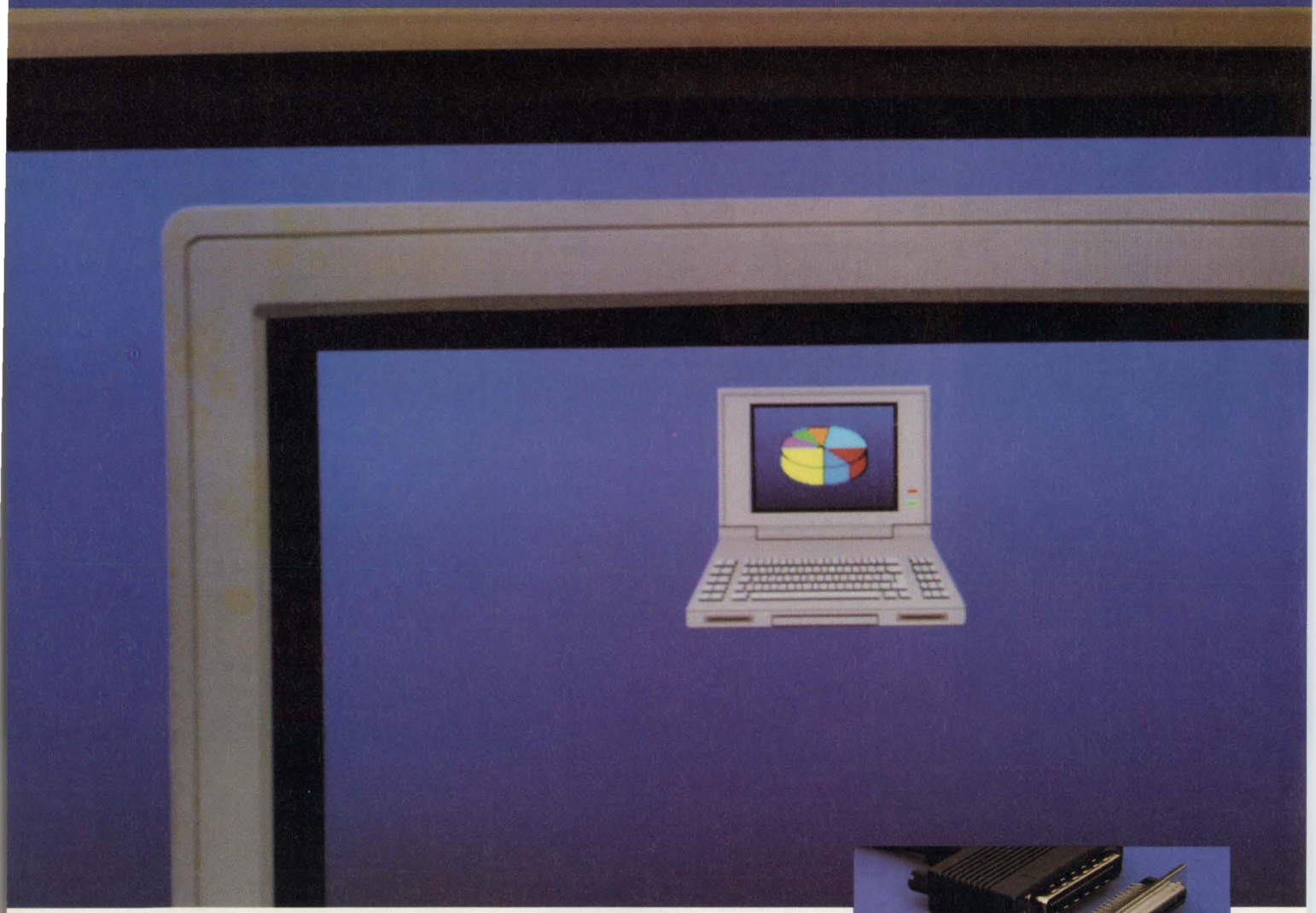
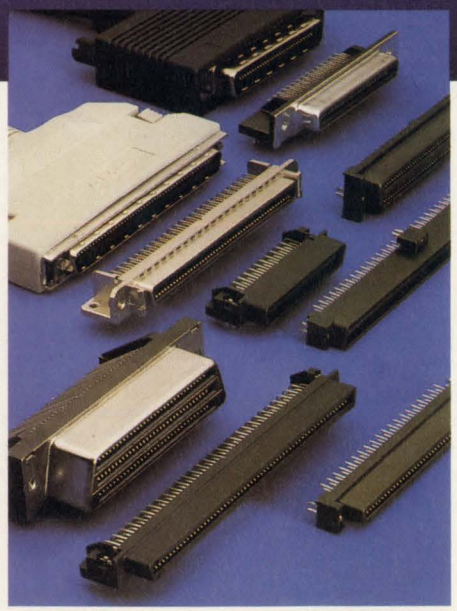


THIS IS AMP TODAY.



.050 CL, leaf-contact design

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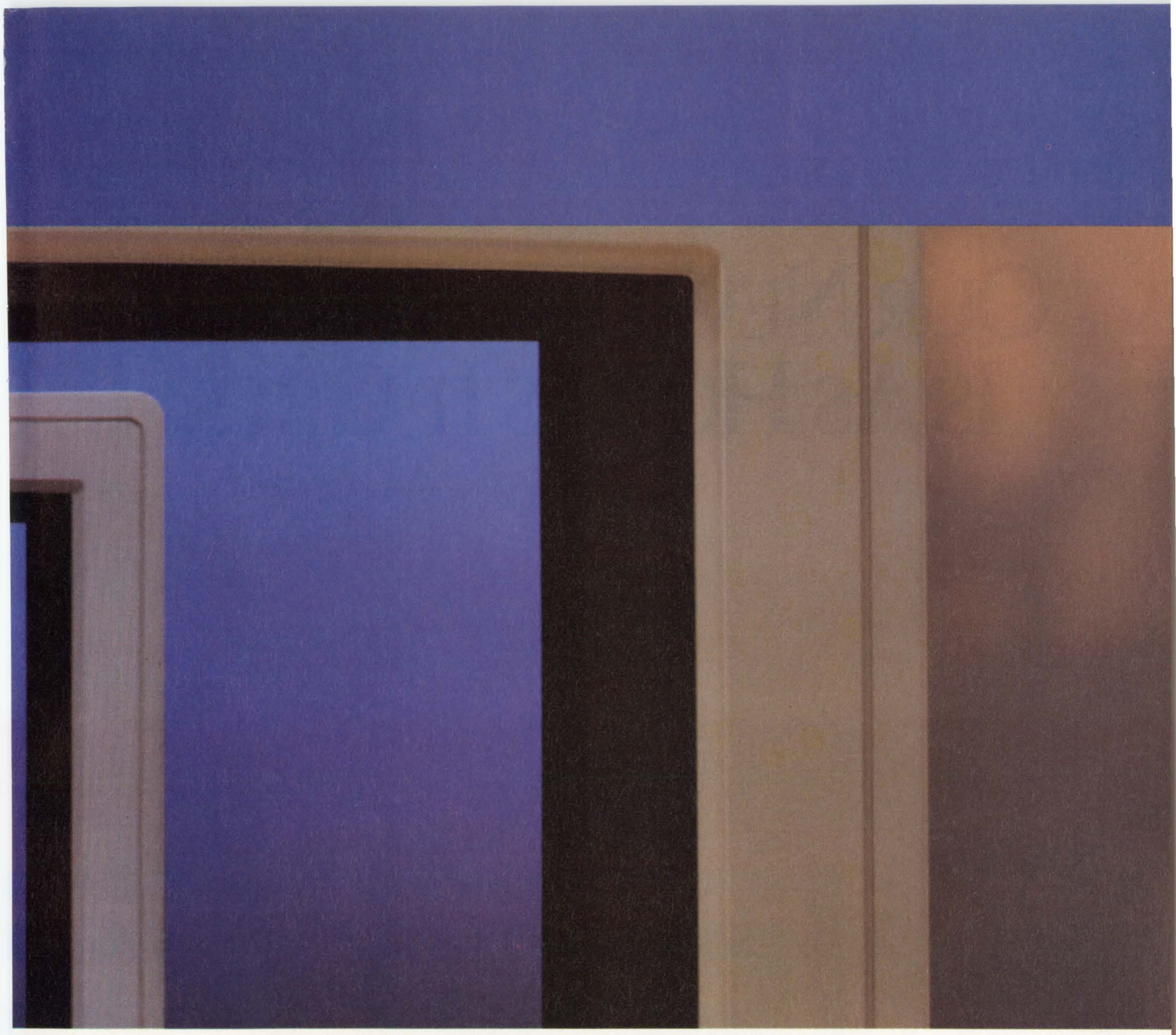

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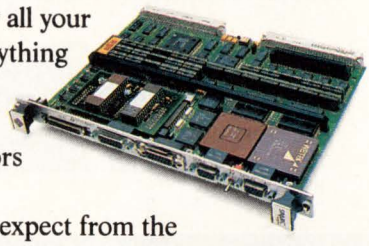

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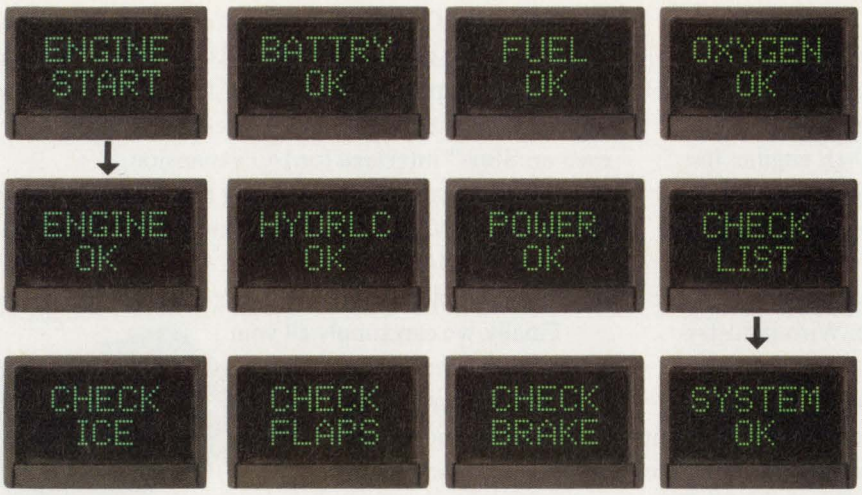

AN APPLICATIONS EXAMPLE. While the following example is for aircraft, it could apply to any air, land, sea or space system.

SEQUENCE ONE: The four-pushbutton display reads "ENGINE START," "BATTERY OK," "FUEL OK," OXYGEN OK." The operator selects "ENGINE START."

SEQUENCE TWO: The four-pushbutton display now changes to read "ENGINE OK," "HYDRLC OK," "POWER OK," "CHECK LIST." The operator selects "CHECK LIST."

SEQUENCE THREE: The four-pushbutton display now reads "CHECK ICE," "CHECK FLAPS," "CHECK BRAKE," "SYSTEM OK." In this manner, the designer can program in as many sequences as required.

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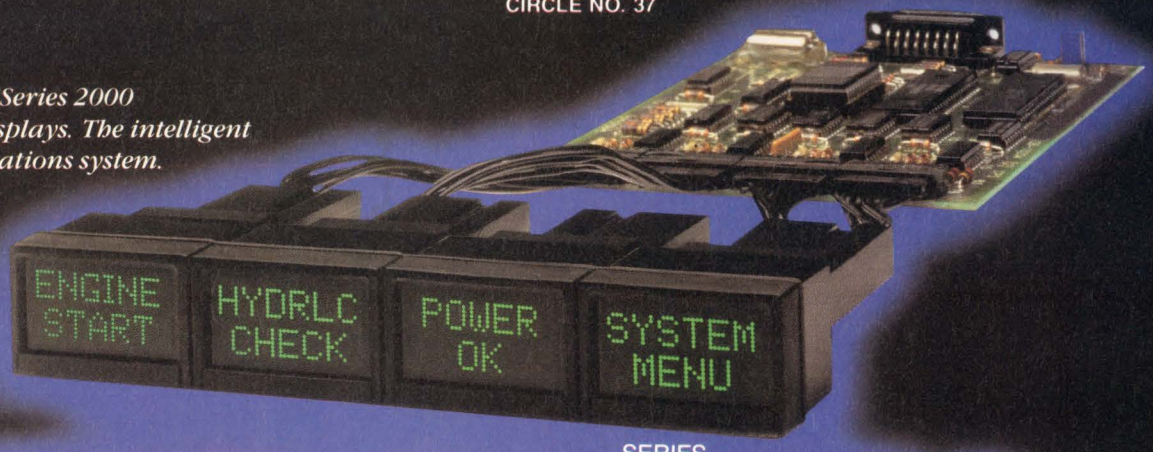

SERIES
VIVISUN 2000™

INNOVATION™

EDN's second annual Innovator and Innovation Crusade came to a close on November 19 during the Wescon/91 show. At a black-tie banquet and reception, the EDN staff presented the awards for the Innovations of the Year—one winner in each of seven product categories—and the Innovator of the Year—the team of Paul Gulick and Arlie Conner from In Focus Systems Inc. EDN will present a check for $10,000 in Gulick's and Conner's names to the university of their choice. All of the winners were selected by votes from our readers.

INNOVATOR OF THE YEAR
Paul Gulick and Arlie Conner
In Focus Systems Inc, Tualatin, OR

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INTEGRATED CIRCUITS AND SEMICONDUCTORS
ISD10xx Analog Storage ICs
Information Storage Devices Inc, San Jose, CA

INNOVATION OF THE YEAR
TEST AND MEASUREMENT
HP54600A 100-MHz Digital Storage Oscilloscope
Hewlett-Packard Co, Colorado Springs, CO

INNOVATION OF THE YEAR
CAE/CAD
Falcon Framework For Concurrent Design
Mentor Graphics Corp, Wilsonville, OR

INNOVATION OF THE YEAR
COMPUTERS AND PERIPHERALS
Color LCD Technology
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Isocon Interconnection System
Rogers Corp, Tempe, AZ

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SOFTWARE
IRMX For Windows
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INNOVATION OF THE YEAR
POWER SOURCES
Genesis High-Power-Density Battery
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Congratulations to the winners and the finalists, and thanks to all who took the effort to bring their products and people to the attention of EDN readers in the 1991 Innovation Crusade. The rules and instructions for next year's competition will be ready at the end of winter. If you'd like to order a nomination kit, Circle No. 410 on our reader service card or fax us at (617) 558-4470 and we'll put you on our mailing list. Good luck!

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Tualatin, OR
(503) 692-4968

Defying the conventional additive-color approach to creating color displays, Paul Gulick and Arlie Conner labored on a subtractive approach to creating a color LCD projection panel built from three stacked monochrome panels. They exploited the birefringence effect, once perceived as one of the LCD's drawbacks, to create this breakthrough technology. The resulting triple supertwisted nematic (TSTN) LCD furnishes color pixels that emit smooth, continuous colors, brighter images, and higher quality images than other color LCD modules.

Conventional color LCD techniques mimic the additive-color triads used in CRTs, using additive-color filters over individual pixels, which reduce transmittance. The TSTN Color LCD module avoids the use of additive filters (red, green, and blue), thereby letting more light pass through. Instead of additive-color filters, the TSTN display employs polarizers and LCD panels tuned to three subtractive colors (yellow, cyan, and magenta), which produce the multicolor, single-element pixel and permit the brighter display.

INTEGRATED CIRCUITS AND SEMICONDUCTORS WINNER

ISD10xx Analog Storage ICs

Information Storage Devices Inc
San Jose, CA
(408) 428-1400

The ISD10xx family of 28-pin nonvolatile CMOS ICs record, store, and reproduce from 12 to 20 seconds of analog information. In addition to speech and music, these ICs can store test waveforms, store correlation data, sample analog signals, and hold filter coefficients. For certain applications, these chips can replace ADC, memory, and DAC functions. Each chip processes and stores analog samples in a 128k-cell EEPROM array and can reconstruct and amplify linear outputs in real time. Two key features are reproduction quality and nonvolatility. For example, the ISD1016 features an S/N ratio of 40 dB and has a 3-dB bandwidth of 3.4 kHz, slightly above telephone-grade specifications. Because the EEPROM array consists of nonvolatile memory cells that use a proprietary CMOS EEPROM technology to store charges, the chip requires no backup supply to maintain its analog information. Each device operates from a 5V power supply and requires few external passive components—resistors and capacitors that control filtering and automatic gain control.

The key to the ICs' storage feature is the physics of nonvolatile floating-gate CMOS EEPROM cells, which are inherently capable of storing "gray scale" voltages that lie between hard-programmed digital states. Each gate acts as a capacitor with an extremely long decay time. These cell features are well known, but these ICs incorporate novel analog transceivers, supporting analog and digital circuits, and high-voltage and -frequency references to control storage and retrieval functions. Typical applications include voice-output products: phone-answering equipment, portable telephones, pagers, emergency equipment, and alarms. The ISD1012, 1016, and 1018 can store 12, 16, and 20 seconds of information, respectively. The devices cost $15, $18, and $20 (1000), respectively.

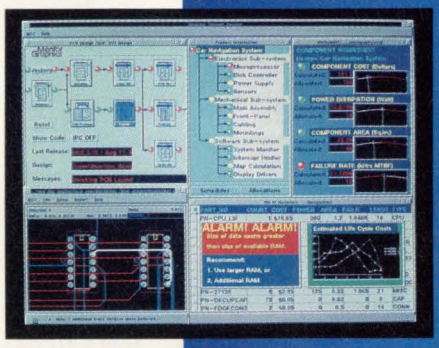
INNOVATION™

Falcon Framework For Concurrent Design

The Falcon Framework for Concurrent Design is the foundation of Mentor Graphics Corp's next-generation software suite, System 8.0. Falcon helps engineering organizations plan and coordinate product development in the following ways: it provides a consistent user interface for all design tools; it stores all project-related information and design data in a unified database; it provides ready and controlled data access; and it monitors all design activity to ensure fulfillment of project goals.

The framework comprises an extended version of the Open Software Foundation's Motif interface for Unix; a database manager that stores all design data in object-oriented data structures; a design-management environment that represents software and designs as hierarchical icons and includes version-control, configuration-management, and product-release facilities; and the Decision Support System.

The Decision Support System enables a design team to simulate a product's behavior based solely on specification parameters entered into its spreadsheet. You enter the equations that describe the desired model, and, based on the parameters, the spreadsheet calculates such factors as cost, power dissipation, and reliability. It can even perform preliminary thermal analyses. The software automatically extracts the data needed for the calculations from the framework's database and from other, linked databases—a purchasing department's list of sanctioned components, for example.



Resulting design models become a sort of living specification: ongoing design information and predetermined parameters are treated as a working body of knowledge. If at any point in the cycle the parameters are violated, the system sends out an alarm to the appropriate project-team members.

The Falcon Framework is shipped free of charge as part of Mentor's System 8.0.

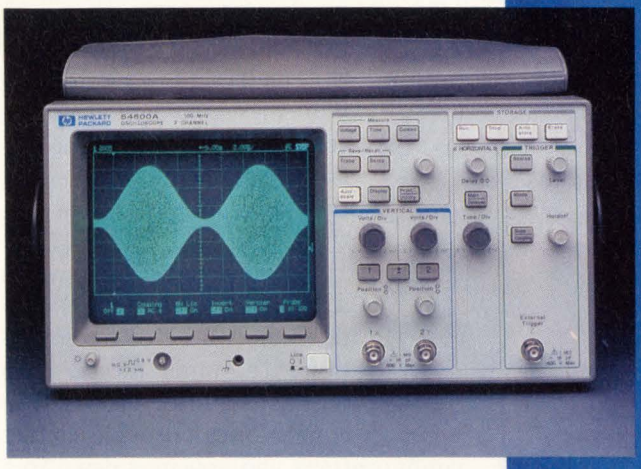
CAE/CAD WINNER

Mentor Graphics Corp
Wilsonville, OR
(503) 685-7000

HP54600A 100-MHz DSO

The $2395 2-channel HP54600A and $2895 4-channel HP54601A digital-storage oscilloscopes (DSOs) couple analog-style controls—separate knobs for such functions as gain, position, and sweep speed—with real-time performance. No perceptible lag occurs when you observe the output of a circuit under test and manually adjust the parameters of that circuit. With the exception of a few expensive scopes that incorporate high-speed DSP μPs, nearly all DSOs exhibit a noticeable lag in display updates.

The scopes have an analog bandwidth of 100 MHz. You can use the entire bandwidth when viewing repetitive waveforms. The scopes have a resolution of 8 bits and a maximum vertical sensitivity of 2 mV/div.



TEST AND MEASUREMENT WINNER

Hewlett-Packard Co
Colorado Springs, CO
(800) 752-0900

INNOVATION™

COMPUTERS AND PERIPHERALS WINNER

Color LCD Technology

Triple supertwisted nematic technology (TSTN) yields an economical true-color LCD display. The display uses a subtractive system, bypassing additive systems' color filters and yielding a brighter screen, fewer "jaggies," and clearer images.

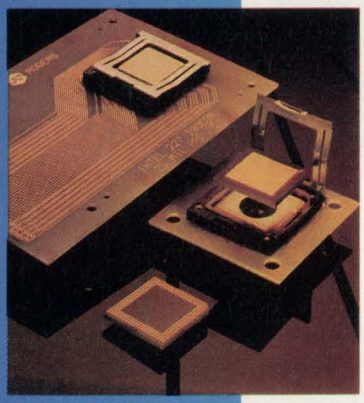
In Focus Systems Inc
Tualatin, OR
(503) 692-4968

The widely accepted approach to obtaining color from an LCD display is to concentrate first on a good black-and-white image, and then to apply color filters in an additive color system. This system, based on supertwisted-nematic or active-matrix technology, has entailed great efforts to get rid of the inherent coloration of the displayed image. The TSTN technology takes the opposite approach of stacking magenta, cyan, and yellow color cells on top of one another to exploit the inherent coloration of the image in a subtractive color process, like that used in photography. This process yields higher transmission and better contrast than the additive process and, despite early doubts about its viability, is manufacturable at an economic price.

Four products currently use TSTN technology. A 10½-in. backlit monitor for desktop computers has 640 × 480-pixel screen resolution and 64 (Model 64M) or 4913 (Model 5000M) addressable colors. The display is compatible with CGA, MCGA, EGA, VGA, Macintosh SE, and Macintosh II graphics adapters. The 480CX and 5000CX are heat-resistant display generators that you place on the platform of an overhead projector for display on a screen, provided the lamp power does not exceed 600W. Prices of all modules are $1500 (OEM qty).

COMPONENTS, HARDWARE, AND INTERCONNECTS WINNER

Interconnection System



Rogers Corp
Circuit Components Div
Tempe, AZ
(602) 967-0624

The Isocon connector is a pressure-mated device that interconnects arrays of contact pads. The unit consists of flat, S-shaped beryllium copper conductors (nickel- and gold-plated) suspended in a high-stress-retention microcellular silicone. Applying downward force causes the conductors to rotate, providing a wiping action at each contact point. The microcellular silicone maintains the contact force and provides a gas-tight seal.

Isocon connectors provide a solderless demateable interconnect for electronic components, such as IC chip packages and pc boards. The connector can provide contact configurations and spacings down to a 50-mil pitch in grid—as many as 400 contacts per in.^{2} of board surface. The connector can accommodate large variations in compression levels, so its performance is not adversely affected by diverse package and board tolerances. Because it has a lifetime in excess of 10,000 mate/unmate cycles, this connector is compatible with test and burn-in applications.

Isocon connectors consist of the conductor-populated silicone material permanently attached to a socket that aligns the IC of a multichip module package with the pc-board contact pads. The socket also controls compression in the silicone material. In most cases, the system is custom designed for each application. However, there is very little tooling cost associated with the Isocon array. Hardware costs depend on customer requirements and final contact-array complexity. Including socket hardware, the product is priced at $0.05 to $0.15 per contact.

INNOVATION™

IRMX For Windows

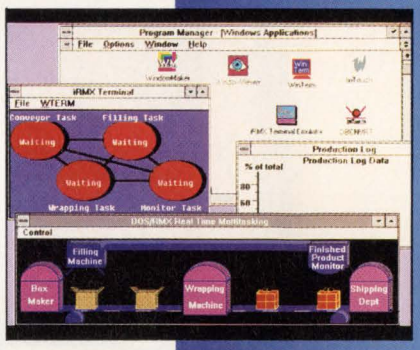
SOFTWARE WINNER

The IRMX for Windows operating system lets real-time software and DOS and Windows application programs run simultaneously on the same IBM PC/AT processor. The operating system also provides DOS extensions for real-time DOS or Windows program development.

Standard, unaltered DOS runs as a task under the operating system; Windows 3.0, also unaltered, runs as a DOS application. The operating system's real-time control comes from the multitasking kernel of IRMX, a real-time operating system that was previously limited to Multibus boards and systems.

Initially, DOS loads IRMX as an application program. This "application" then seizes control, switching the processor into protected mode and encapsulating DOS as a task under IRMX. DOS then resumes operation, unaware of its new environment. A DOS or Windows application program thus runs as an IRMX task and can communicate with other IRMX tasks.

The combined DOS and IRMX operating system has multiple layers. The nucleus is a 32-bit, real-time kernel that has 255 task-priority levels, preemptive scheduling, prioritized interrupt management, timer management, semaphores, mailboxes, and other means of intertask synchronization and communication. Other layers include an I/O system layer and a human-interface layer. The operating system, with libraries and documentation, costs $1995. Run-time disks are $150 each.



Intel Corp
Hillsboro, OR
(503) 696-2441

Genesis High-Power-Density Battery

POWER SOURCES WINNER

In designing the Genesis battery, Gates Energy Products has accomplished an objective that has eluded lead-acid-battery designers for decades: reducing by approximately 40% the size and weight of a battery that delivers high power (720W) for approximately 15 min. Indeed, when called upon to deliver 1800W, the battery operates for 5 min vs as little as 30 sec for more conventional batteries of the same size.

Certain immutable rules constrain the design of lead-acid batteries. Obtaining higher current requires increasing the area of the battery plates. But increasing the plate area while holding the battery's size constant requires making the plates thinner. Previous attempts to make thinner plates resulted in reduced physical strength and shortened battery life. But the manufacturer's improvements in processes and materials have overcome those problems.

Having created a battery specifically for low- and medium-power uninterrupted power supplies, the manufacturer has tailored the battery's characteristics to that application—a feat not possible in a battery intended for a range of uses. For example, the hardened terminals eliminate the need to periodically tighten cable clamps. The batteries are sealed and require no maintenance; under normal operating conditions, their electrolyte system eliminates venting of hydrogen into the atmosphere. Their flame-retardant cases conform to UL standard 94V-0 and have built-in carrying handles. The batteries cost $94.50.

Gates Energy Products Inc
Gainesville, FL
(904) 462-3911

FLUKE®

All logic analyzers give you integrated state and timing, sooner or later.

Why not now?

Introducing the new Philips PM 3580 family of logic analyzers from Fluke: the first instrument architecture to give you state and timing together on each channel—with a single probe.

Connect the probe to your board for state and you're automatically hooked up for timing. Or vice versa.

This means no more dual probing—a pain anytime and the source of loading problems—and no reconfiguration between state and timing. Which makes these analyzers simple to learn and use.

A basic comparison: Record all state and timing data on an 8-bit microprocessor with multiplexed bus, 8-bits for address, 3 control signals and a clock.	HP 1654B	Tek PRISM/MPM	Philips PM 3580/30
Probing: Channels used	48[1]	48[2]	20
One connection	No	No	Yes
Setups	Two	Two+	One
Interfaces to learn	Two	Two+	One
Integrated state & timing triggering	No, only one arming condition	No, only indirect 4-bit Teklink	Yes, 8 levels
State & timing data per pin	No	No	Yes
Price	$6700	$8600	$4250

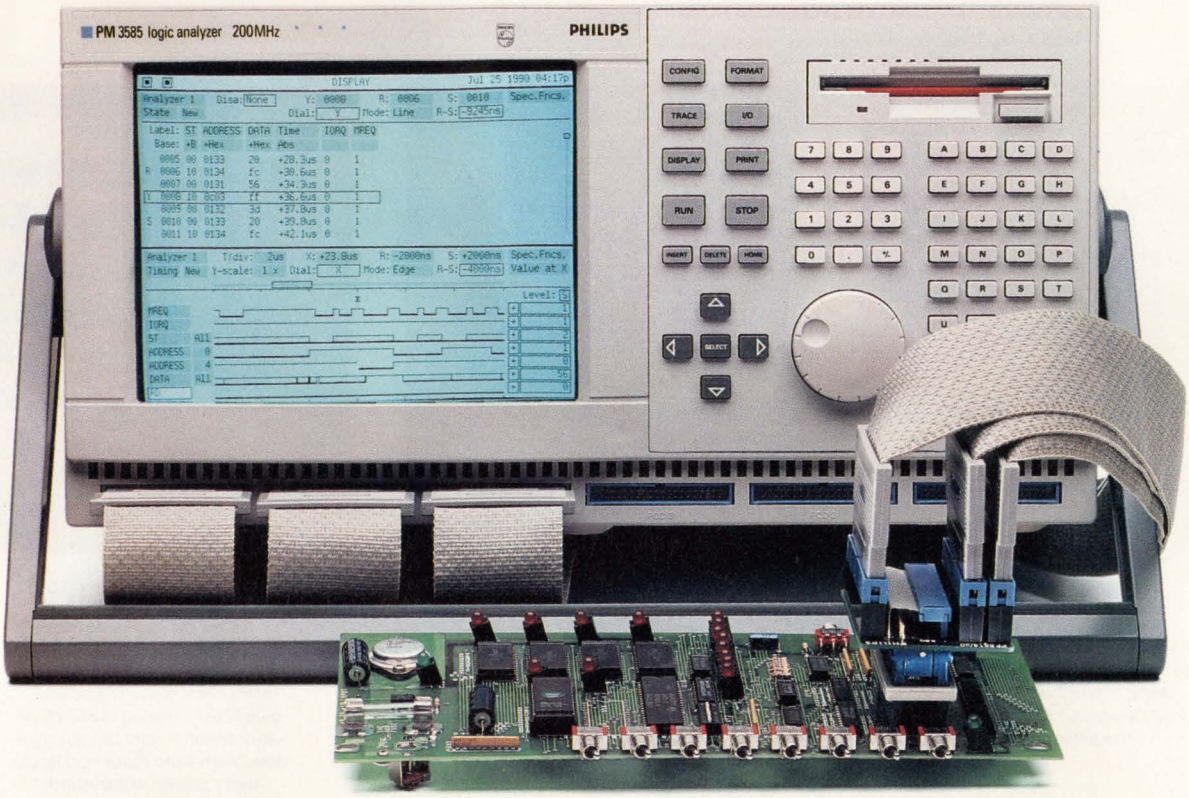
Footnotes: 1) 8 channels lost to de-multiplexing
2) De-multiplexing requires double probing and only nine high-speed channels on basic unit

Plus, the pop-up menus and keyboard shortcuts guide you quickly through setup and data analysis. No matter if you use it every day or once a year.

What's more, capturing an elusive bug has never been easier with eight unrestricted trigger levels that let you select from state and

PHILIPS

PHILIPS



Why not sooner?

timing trigger conditions on each level.

But being simple doesn't mean simplistic. Basic performance of the PM 3580 family ranges from 32 to 96 channels, each with 50 MHz state and up to 200 MHz timing, plus 3 nanosecond glitch capture and 2K of memory per channel. For 8-, 16- and 32-bit processors.

And you get all this for nearly half the cost of comparable analyzers.

We'd like to send you a video. Or show you how to make state and timing measurements at your workplace—in 30 minutes or less.

We'll even bring the stopwatch so you can time us. And you can keep it to time the competition.

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Ask for extension 720.
Because sooner is better.

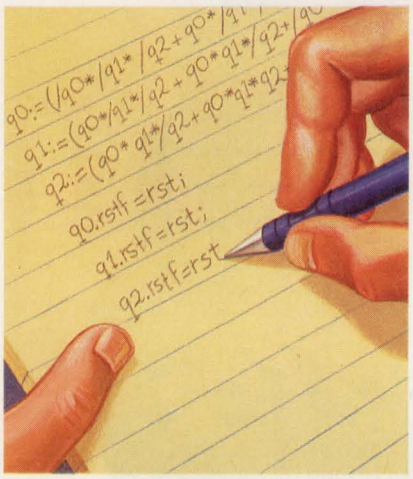
John Fluke Mfg. Co., Inc., P.O. Box 9090, M/S 250C, Everett, WA 98206-9090. U.S. (206) 356-5400. Canada (416) 890-7600. Other countries: (206) 356-5500. ©1990. All rights reserved. Ad No. 00001.

FAST ANSWERS.

FLUKE®

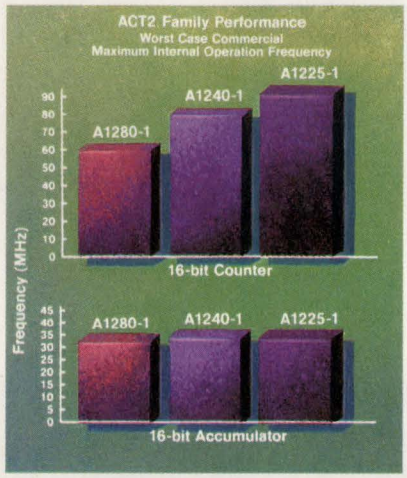
CIRCLE NO. 38

You Design Actel FP You Do A PLD. But Th



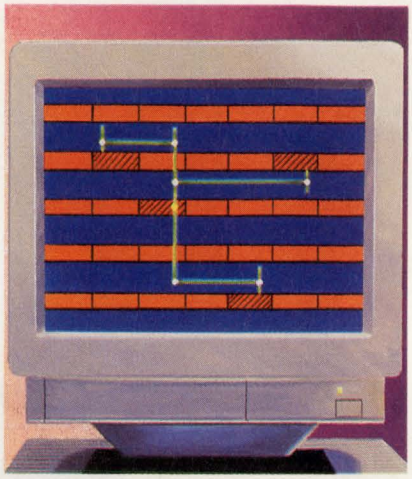
Use PLD Tools.

You design Actel FPGAs using the same tools as you would a PLD: ABEL,™ CUPL,™ LOG/iC™ and PGADesigner.™ But that's where the similarity ends.



Fast. Fast. Fast.

Our FPGAs are real speed demons. Whatever application you may be working on, our parts will give you the kind of performance you're looking for.



100% Automatic Place And Route.

Coupled with your PLD tools, Actel's Action Logic™ System (ALS) software lets you create your own FPGAs—using a 386 PC or workstation—right at your own desk. With Auto Place and Route that's proven in thousands of applications.

Announcing A Simple Way To Get From PLDs To FPGAs.

If you're a PLD designer with an interest in fast, flexible FPGAs, but you think you don't have time to learn new design techniques, we'd like to change your mind.

First of all, you don't have to give up your existing PLD design tools or Boolean equations. Actel's ALES™ 1 program translates the output of PLD tools like CUPL™ and LOG/iC™ into logic optimized for our ACT™ devices. ABEL™ 4.0 includes optimization for Actel devices. Entire FPGA designs can be developed with PGADesigner.™

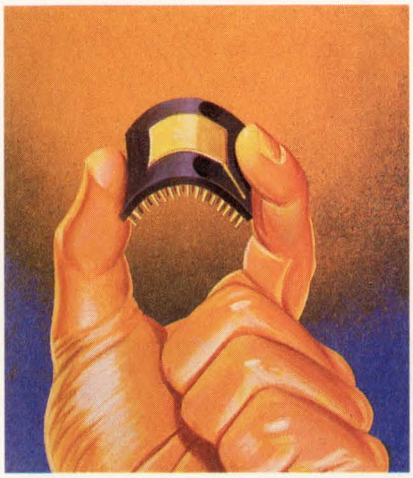
Actel devices offer everything you want in an FPGA. Like high I/O and flip-flop counts. And 100% automatic place and route gets you to market fast.

Once your FPGA is designed, our Action Logic™ System (ALS) converts the captured design into a completed device in minutes. To give you true, high-density, field-programmable, channeled gate arrays.

Other FPGA manufacturers fall short on design verification. Our exclusive Actionprobe® diagnostic tools, give you 100% observability of internal logic signals. So you don't have to give up testability for convenience.

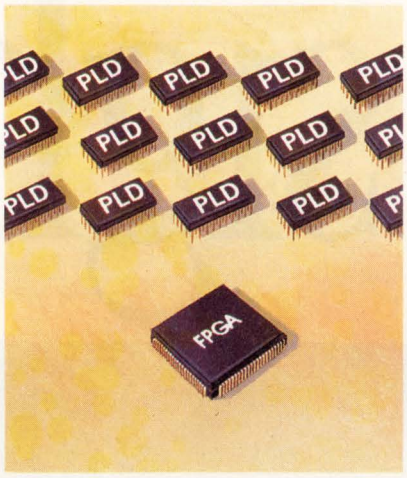
It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546 latches. And the first member of our ACT 2 family, the power-

GAs The Same Way e Similarity Ends There.



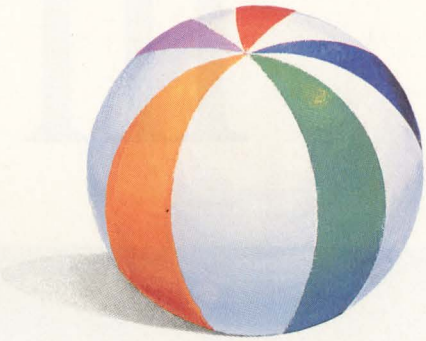
More Flexibility And Capacity.

Designing with Actel FPGAs gives you more freedom than you ever imagined. More gates. More flip-flops. More I/O. In fact, our new A1280 is the largest FPGA in the world.



Small Footprint.

Actel FPGAs give you far more gates per square inch. As much as ten times as many as the densest PLDs. That can save a lot of real estate.

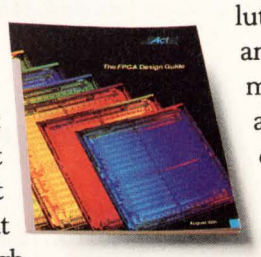


More Fun.

Designing Actel FPGAs is so simple that you'll have more time to do the things that made you want to become an engineer in the first place. Or just relaxing. You've earned it.

ful A1280. With 8,000 gates, up to 998 flip-flops, and 140 I/O pins, it's the highest capacity FPGA today. And our A1240-1 is the fastest. In the A1240-1, 16-bit counters run at 75 MHz, 16-bit accumulators at 33 MHz. Enough capacity and speed to handle almost any application.

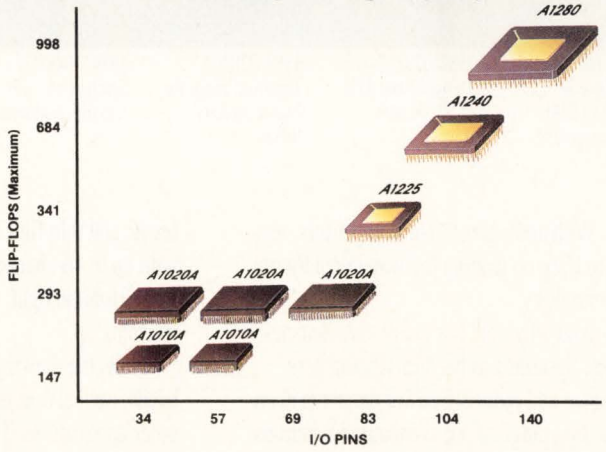
The superior speed, capacity, and auto place and route capabilities of our FPGAs are made possible by Actel's revolutionary PLICE® antifuse programming element. The advanced technology that makes our family of FPGAs an ideal way to unleash your engineering creativity.



The FPGA Design Guide

Call **1-800-228-3532** for your free FPGA Design Guide.

Broad Family With High Capacity



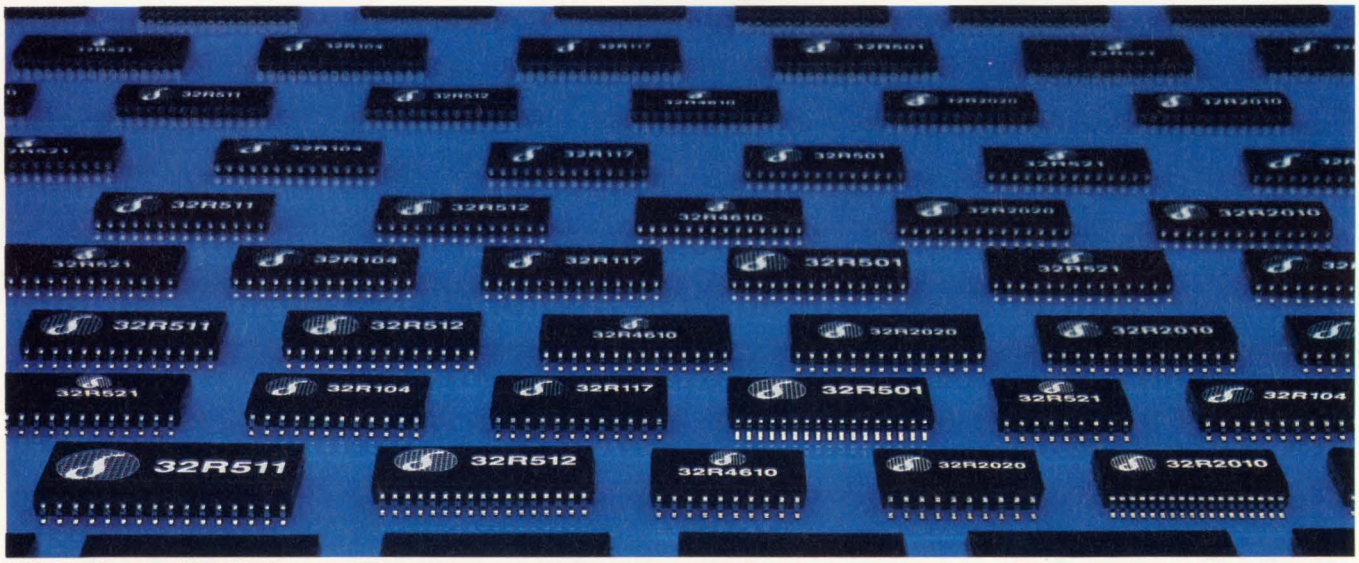
Actel

Risk-Free Logic Integration

CIRCLE NO. 56

Read/Write IC Solutions

No end in sight.



1978: 32R104
Propelled the growth of IBM plug-compatible drives.

1982: 32R117
Designed into 95% of ST506 type drives.

1984: 32R501
Improved things for higher capacity drives.

1989: 32R521
The first +5, +12v thin film read/write.

1990: 32R511/512R
A pin-compatible migration path from three- to two-terminal design.

1990: 32R4610
The first +5v only, two-terminal read/write device.

1991: 32R2020
New. The industry's highest performance +5v only read/write.

1991: 32R2010
New. The industry's highest performance +5, +12v read/write.

With apologies to our competitors, we plan to keep on leading the way in read/write IC technology.

And why not? For nearly two decades Silicon Systems has been increasing performance and reducing power demands in an expanding range of pin-compatible functions. All designed for a world of ever-shrinking form factors.

Current achievements include low-power, +5v only read/write devices that consume under 5mW in idle mode. Our new two-terminal read/write amplifier for thin film and MIG heads. A read/write device for both 3-terminal ferrite and thin film applications. And devices with up to 16-channel capability.

Hold on tight, though. We're just warming up.

On the drawing board are ICs for MR heads, optical disk drives and a variety of other applications. There's just no end to our involvement.

If you need flexible and far-reaching read/write IC solutions for your next generation of products, call us for literature package **SPD-15**. We'll send you our new **Read/Write IC Short Form Catalog**, give you the name of your nearest Silicon Systems representative and update you on our latest developments. **1-800-624-8999, ext. 151**

Circle #7 for Product Information

Circle #8 for Career Information

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Silicon Systems®
A TDK Group Company

HIGH-PERFORMANCE PULSE GENERATORS

Modular systems give freedom of choice

Manufacturers of high-performance pulse generators are turning to modular systems to increase versatility while keeping costs down.

Doug Conner,
Technical Editor

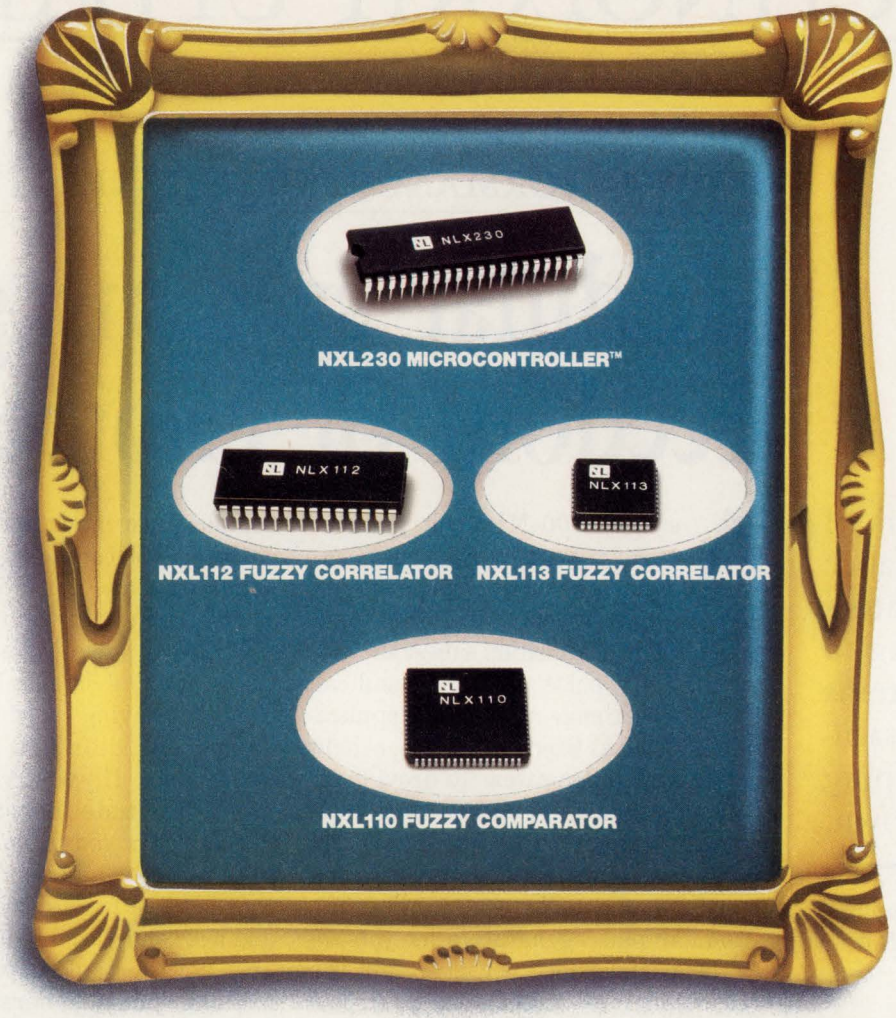
A single 100-MHz or greater pulse generator often can't satisfy every application. One engineer may need low-level pulses with sub-nanosecond transition times, another may need 10V pulse amplitudes and can tolerate slower edge rates. Some applications call for fast fixed edge rates, others need variable edge rates. To provide instruments that excel rather than compromise to meet these conflicting requirements, manufacturers are turning toward modular pulse generators.

Modular pulse generators let you select the performance you need and the right number of channels for your particular application. One channel is sufficient for you to test the maximum toggle rate of a flip-flop. Checking setup and hold times for a flip-flop requires two channels. Testing high-speed timing on complex ICs may take more than two channels. Fortunately, high-speed pulse generators are available with as many as 18 channels.

Modular pulse generators that support multiple channels offer you the choice of having more than one type of module for different performance requirements. If you have extra channels, you can dedicate them to other modules, which allows you to switch test parameters quickly. For example, you can choose a fast fixed-edge-rate module and add a second variable-edge-rate module. To have the same capability with nonmodular pulse generators, you would need two complete systems—a more expensive alternative.

Pulse generators typically have to make tradeoffs among the maximum pulse-repetition rate, variable transition

Touch-screen menus allow easy programming *of the 9210 pulse generator from LeCroy. The instrument provides one or two channels, which you can select from any of three module types.*



Fuzzy Logic's First Family

NeuraLogix proudly announces the first true family of standard fuzzy logic ICs. Now artificial intelligence applications are no longer constrained by high cost, long development cycles, and complex software.

This ground-breaking line of high-speed, low-power CMOS devices represents the leading edge of fuzzy logic technology, and provides all the options you need for such diverse applications as pattern recognition, robotic control, positioning systems and more.

Devices now available include:

NLX230 Fuzzy Microcontroller™ The first in a family of true hardware-based fuzzy logic controllers, this device makes artificial intelligence available for a wide range of consumer and industrial products at a price competitive with standard 8-bit microcontrollers. An applications development kit is available for only $395.

NLX110 Fuzzy Pattern Comparator. Specially designed for multiple pattern comparisons of serial real-time data, this device adds intelligence to video and speech recognition systems, as well as telemetry applications. An applications development kit is available for $395.

NLX112 and NLX113 Fuzzy Data Correlators. These chips are as simple to use as ordinary correlators, but are more than twice as fast and operate with noisy and incomplete data. The NLX112 performs 128-bit data comparisons with selective bit masking capability and easy word-length expansion via cascading devices. The more versatile NLX113 offers 32/64/128-bit selectivity, 50 mHz speed and separate clocking for data and reference patterns.

For a family portrait of detailed specifications and prices, contact NeuraLogix today!

NeuraLogix

American NeuraLogix, Inc.
411 Central Park Drive
Sanford, FL 32771
Telephone 407/322-5608
FAX 407/322-5609

CIRCLE NO. 57

High-performance pulse generators

speeds or edge rates, and output amplitude. You need high pulse-repetition rates to test the maximum toggle rates on flip-flops, maximum frequencies for counters, and general simulation of high-speed clocks or data. And high pulse-repetition rates require fast transition or edge rates.

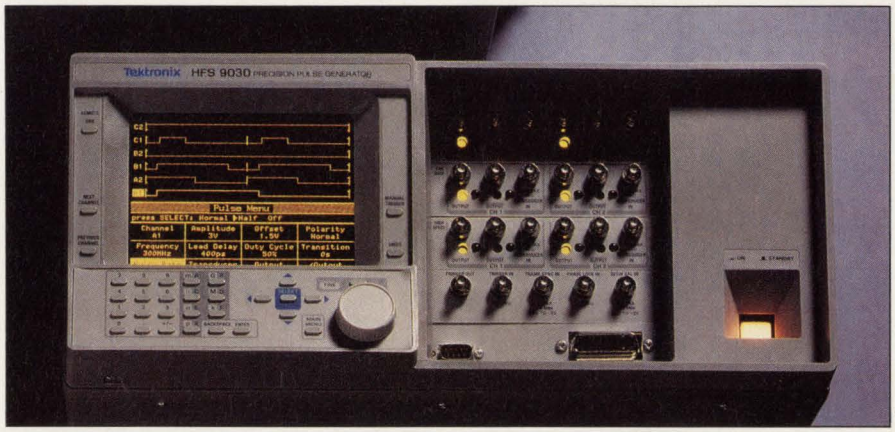
However, high pulse-repetition rates are difficult to maintain at high p-p output voltages because the voltage changes require extremely high slew rates. To keep slew rates reasonable, pulse-generator repetition rates and edge-transition rates go down as the output amplitudes go up.

Edge rates approximate reality

Variable transition rates are sometimes important for matching test inputs to actual circuit input characteristics. For example, a maximum-toggle-rate test may give different answers when stimulated by pulses with 200-psec transition speeds instead of a closer representation of what the circuit will see in practice, which might be a 2-nsec transition time.

Variable edge rates may also be important when using the pulse generator to stimulate circuit inputs that don't match the usual 50Ω source impedance of the pulse generator. You can adjust a variable-edge-rate pulse generator to a lower edge rate to minimize ringing in such cases. If you need variable edge rates, you'll probably have to settle for a lower maximum edge rate than fixed-rate machines can provide. Some pulse generators, such as the 9212 module from LeCroy (**Table 1**), offer fast variable edge rates, but they do so over a narrow range (350 psec to 1 nsec).

All the pulse generators listed in **Table 1** offer a double-pulse mode. As the name implies, the pulse generator produces two pulses for each period or trigger. You can use the double-pulse output to drive the clock of a flip-flop and a second channel running with a single pulse per period to drive the data, allowing you to clock alternating ones and zeros into flip-flops and other circuits.



Modular pulse generators let you choose the performance and number of channels *you need. You can choose two, four, or six channels for the instrument shown here from Tektronix. The two channel modules are available in two performance versions.*

A burst mode, available on most pulse generators, is similar to double-pulse mode but extends the number of pulses generated after a trigger. The maximum number of pulses in a burst is programmable from 9999 up, depending on the instrument.

Tektronix's HFS 9000 series pulse generators offer the unique capability of having channel frequencies selectable at one-half, one-quarter, or one-eighth the base frequency. The different frequencies are useful for driving address lines when testing circuits such as multiplexers, demultiplexers, and memories, and for driving data lines when testing D/A converters.

Whenever you are using a pulse generator setup with more than one channel, you'll want to be able to vary the timing between the channels. You may need to remove the skew between channels or set up special timing relationships between waveforms. It's important that the pulse generator offers a sufficient delay range and provides adequate resolution in the size of the delay increments to perform these time-delay operations.

For example, if you want to test the setup- and hold-time requirements of a circuit, you'll want to vary the timing relationship between clock and data in small increments to find where the circuit fails. Resolution of 10 or even 100 psec might be adequate, but 1-nsec resolution probably is too coarse for most applications.

Although the above example looks at pulse delay, you may also have similar resolution requirements for pulse width. Often you'll find pulse generator timing specifications such as resolution are the same for pulse width and pulse delay.

Some pulse generators list a monotonicity timing specification. The maximum specification for monotonicity may be greater than one increment of resolution, indicating that an incremental increase in pulse delay may actually result in a delay that is *shorter* or unchanged from the previous value.

For example, Wavetek's model

Text continued on pg 58

High-performance pulse generators

Table 1—Representative high-performance pulse generators

Manufacturer	Product	Description	Maximum channels	Channels as priced	Price	Pulse-repetition rate		Pulse width		Delay	
						Maximum (MHz)	Accuracy (±)	Resolution (psec)	Accuracy (±)	Resolution (psec)	Accuracy (±)
Berkeley Nucleonics	6040	Mainframe	1	0	$4250	100	0.01%	1000	1 nsec	±1 nsec	500 psec +0.2%
	201E	Module	1	1	$2900	100 (or 300 external)	0.01%	1000	1 nsec	±1 nsec	500 psec +0.2%
Hewlett-Packard	8130A	Mainframe	2	1	$12,700	300	5% +100 psec	10	5% +250 psec	10	5% +1.5 nsec
	2nd channel	Factory option	1	1	$6600						
	8131A	Mainframe	2	1	$16,000	500	5% +100 psec	10	5% +250 psec	10	5% +1.5 nsec
	2nd channel	Factory option	1	1	$8250						
LeCroy	9210	Mainframe	2	0	$5900						
	9211	Module	1	1	$1600	250	0.5% +200 psec	10	0.5% +300 psec	10	0.5% +1 nsec
	9212	Module	1	1	$2200	300	0.5% +200 psec	10	0.5% +300 psec	10	0.5% +1 nsec
	9213	Module	1	1	$1000	100	0.5% +200 psec	10	0.5% +300 psec	10	0.5% +1 nsec
Philips	PM5781	Fixed system	1	1	$9785	125	0.1%	10	3% +1 nsec	10	3% +1 nsec
	PM5781 and Calibrator	Fixed system with calibrator	1	1	$11,185	125	0.1%	10	1% +1 nsec	10	1% +1 nsec
Tektronix	HFS9009	Mainframe	18	0	$19,995						
	HFS9010	Mainframe and two 9PG1 modules	6	4	$37,500						
	HFS9020	Mainframe and two 9PG2 modules	6	4	$36,500						
	HFS9030	Mainframe, one 9PG1, and one 9PG2	6	4	$37,500						
	HFS9PG1	Module	2	2	$11,000	630	1%	10	1% +300 psec	10	1% +300 psec
	HFS9PG2	Module	2	2	$7900	300	1%	10	1% +300 psec	10	1% +300 psec
	TM502A	Mainframe	2	0	$395						
	PG502	Module	1	1	$3495	250	NA	NA	NA	NA	NA
	PG503	Module	1	1	$5250	250	NA	NA	NA	NA	NA
Wavetek	869	Mainframe	4	1	$16,095						
	869-C	Module	1	1	$8620	100	5 PPM	100	1% +1 nsec	100	1% +2 nsec
	2000	Mainframe	4	0	$9980						
	2002FE	Module	1	1	$8770	200	2%	100	2% +1 nsec	100	2% +1 nsec
	2005FE	Module	1	1	$9465	200	2%	100	2% +1 nsec	100	2% +1 nsec
	2005	Module	1	1	$8840	200	2%	100	2% +1 nsec	100	2% +1 nsec
	2010	Module	1	1	$9890	200	2%	100	2% +1 nsec	100	2% +1 nsec

Notes:
*Full range if not specified.
NA=Not applicable.
NS=Not specified by manufacturer.

Pulse amplitude						Transition times					
			Accuracy (±)								
Range	p-p	Resolution (mV)	% Level	% Amplitude	Offset (mV)	10%–90% minimum (psec)	At V p-p*	20%–80% minimum (psec)	At V p-p*	Maximum	Comments
Fixed	5V	NA	NS	NS	NS	1000	5	700	1.0	Fixed	
–5, 5V	5V	20	NS	0.1	15	NS		150	5.0	Fixed	Optical module options and amplitude to 300V.
–5, 5V	5V	10	1	3	40	1000		600		100 μsec	
–5, 5V	5V	10	1	3	40	200	3	200	5	Fixed	
–5, 5V	5V	5	1	1	5	1200		NS		1 msec	
–5, 5V	5V	5	1	1	5	NS		300		1 nsec	
–8, 8V	16V	5	1	1	5	6500		NS		95 msec	
–10, 10V	10V	10	1	2.5	40	2000		1400		100 msec	
–10, 10V	10V	10	1	2	20	2000		1400		100 msec	Includes internal calibrator.
–2, 2.6V	3.0V	10	2	2	50	NS		200	1	Fixed	
–2, 5.5V	5.5V	10	2	2	50	NS		1000		5 nsec	
–5, 5V	5V	NA	NA	NA	NA	NS		1000		Fixed	Not programmable.
–2.5, 2.5V	2.5V	NA	NA	NA	NA	NS		200		Fixed	Not programmable.
											Includes 869-C module.
–5, 10V	10V	5	0	2	50	2000		1200		20 μsec	
–3, 4V	3V	5	0	2	15	NS		320	2	Fixed	
–5, 10V	5V	5	0	2	25	550	5	NS		Fixed	
–5, 10V	5V	5	0	2	25	1000	5	NS		2 μsec	
–5, 15V	10V	5	0	2	50	2000	10	NS		2 μsec	

869 has a pulse width and delay resolution of 100 psec and a monotonicity specification of 500 psec. If you don't measure the timing characteristics of the pulse generator's output, you won't be sure about the result of incremental timing changes.

If you need timing resolution of around 100 psec or less, the pulse generator's timing jitter is also an issue to consider. Timing jitter is a measure of the pulse-to-pulse timing variation. Although the less jitter the better, you can compensate for jitter much larger than the resolution by repeating the measurement many times and using statistical methods.

Buy accuracy or measure it

Accuracy specifications for both timing and voltage vary widely, as **Table 1** shows. Programmable pulse generators specify their accuracy levels. Manual pulse generators, such as the PG502 and PG503 from Tektronix, and older units from some other manufacturers, have few accuracy or resolution specifications. They depend on you to use a separate oscilloscope, timer-counter, or other instrument to set and measure their timing and voltage outputs.

Programmable pulse generators may save you considerable time by not requiring you to measure their outputs to set timing and voltage values accurately. If you are going to depend on the accuracy of the pulse generator when setting parameters, however, pay careful attention to the accuracy specifications of the instruments. Internal self-calibration allows some instruments to offer much better accuracy than others.

Any time you need a pulse generator for use in an automated or semi-automated test setup using the IEEE-488 bus, you'll need a programmable one. Also, programmable pulse generators offer other benefits, such as the ability to store multiple setups for fast recall.

Some programmable pulse generators let you use multiple methods to set parameters. This feature lets you use whichever method is easiest for the type of tests you are making, but its implementation varies somewhat among the different manufacturers. Pulse generators that don't offer multiple parameter entry methods may force you to use a calculator to convert the settings you want into parameters the instrument will accept.

For example, when setting the voltage levels, you might prefer to set amplitude and offset for one test, whereas high and low values might be more appropriate for another test. For setting pulse-timing parameters, you may wish to set the period and vary pulsewidth for some tests. For other tests, you

Who needs a pulse generator?

Pulse generators fill an important instrument niche surrounded by function generators, data or word generators, and arbitrary waveform generators.

Function generators typically provide sine, triangle, square, and often other waveforms such as sawtooths. Rise and fall times of the square waves on function generators are not particularly fast, and function generators usually limit their pulses to 50% duty cycles (square waves).

Data or word generators provide a programmable sequence of digital states across many channels. Pulse edge rates and delay characteristics aren't typically programmable on digital word generators.

Although you have the ability to create any shape of waveform with an arbitrary waveform generator, you can't approach the short rise and fall times and high pulse-repetition rates possible with pulse generators.

Pulse generators concentrate on pulses and typically allow a wide variation in duty cycle. You usually have considerable range over which you can adjust frequency, pulsewidths, and delays with good timing resolution. Rise and fall times on pulse generators are fast and, depending on the pulse generator, may also be adjustable.

Pulse generators find application in many high-performance, analog and digital research, design, and verification operations. Many pulse generator applications require only fast fixed transitions, although some may benefit from variable transition rates.

Examples of pulse generator applications include measuring rise and fall times, transistor switching times, propagation delay times, output skew, and setup and hold times. Pulse generators can also help test metastability and duty cycle effects and measure maximum toggle rates for flip-flops, maximum frequencies for counters, general clock simulation for maximum frequency tests, input capacitance from RC time constants, comparator switching times, and slew rates.

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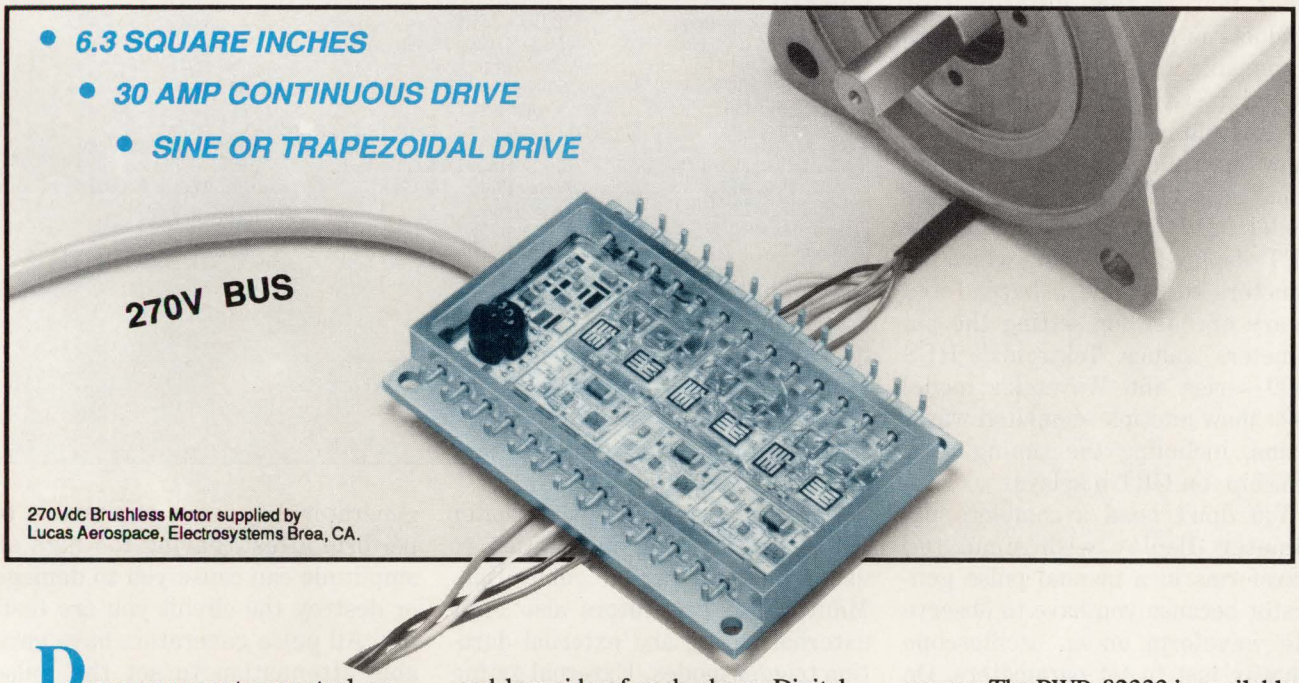

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may want to set the duty factor and vary the period. When setting the pulse edge-transition rates, you may want to specify the value in rise time from 10% to 90%, or you may want to specify the slew rate.

When setting parameters, another feature that differentiates products is the display. Some programmable instruments show a single parameter readout on a numeric or alphanumeric display. Others show multiple parameters, sometimes on a CRT display. LeCroy's model 9210 has a touch-sensitive CRT display for selecting which parameters to set and a keypad and rotary encoder for setting the parameters' values. Tektronix's HFS 9000 series and Wavetek's model 2000 show multiple simulated waveforms, including the timing relationship, on CRT displays.

You don't need a complete parameter display with simulated waveforms in a manual pulse generator because you have to observe the waveform on an oscilloscope anyway just to set parameters. On programmable pulse generators with more than two channels, it's necessary to have the simulated waveform display to avoid errors and keep track of what you have programmed. Without the simulated waveform display, you would probably need to have enough oscilloscope channels to cover all of the pulse generator channels, or you would have to waste time moving scope probes around.

For more information . . .

For more information on the pulse generators discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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1121 Regatta Square
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FAX (510) 236-3105
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Chestnut Ridge, NY 10977
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Building HKF
5600 MD Eindhoven
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Phone local office
Circle No. 719

In North America, contact:
John Fluke Mfg Co
Box 9090
Everett, WA 98206
(206) 347-6100
Circle No. 720

Tektronix
Box 500
Beaverton, OR 97077
(800) 835-9433
Circle No. 721

Wavetek San Diego
9045 Balboa Ave
San Diego, CA 92123
(619) 279-2200
TWX 910-335-2007
Circle No. 722

Pulse generators typically offer external triggering in addition to using internal period generation. Many pulse generators also offer external gating and external duration trigger modes. External gating enables the pulse generator to produce pulses when the gate signal is present. External duration uses the trigger-input pulsewidth to determine the pulsewidth of the output waveform, but the amplitude and edge rates are those programmed on the pulse generator. External duration essentially works as a signal-conditioning mode.

Although not having a high enough output amplitude on a pulse generator may leave you unable to perform a test, having too high an amplitude can cause you to damage or destroy the circuit you are testing. All pulse generators have variable attenuation to set the pulse amplitude and offset to a value within the pulse generator's limits. To prevent inadvertent overvoltage accidents, most pulse generators also let you set a voltage limit.

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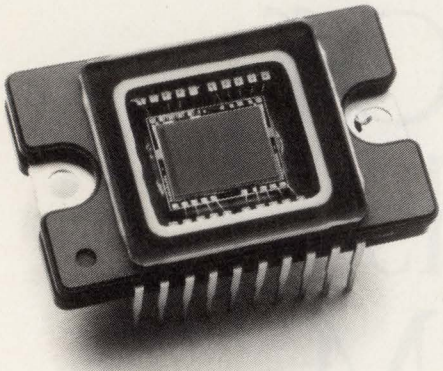

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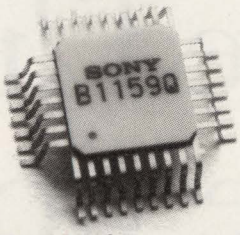

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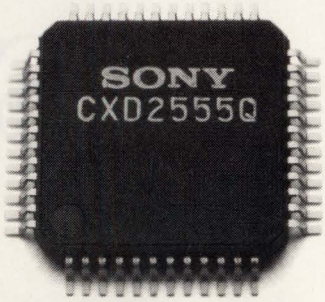

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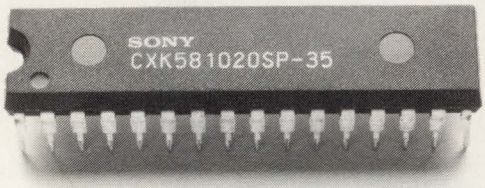

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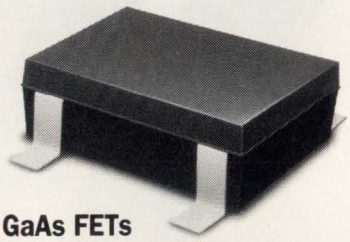

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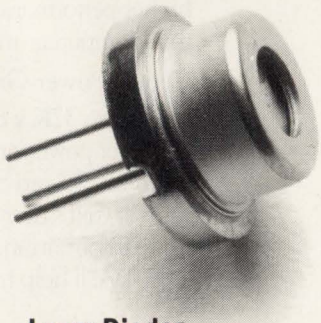

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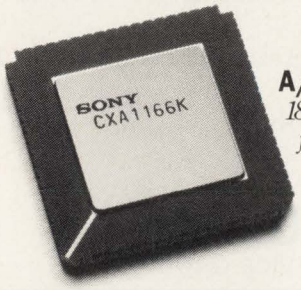

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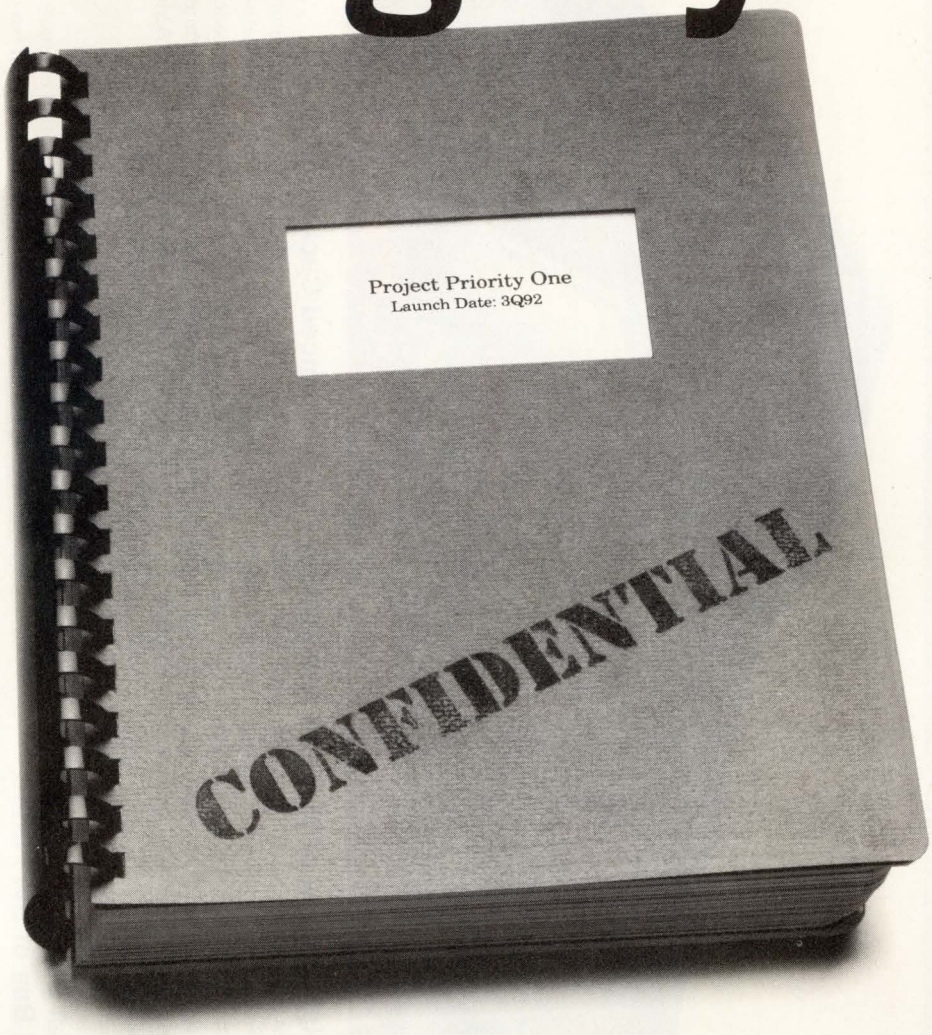

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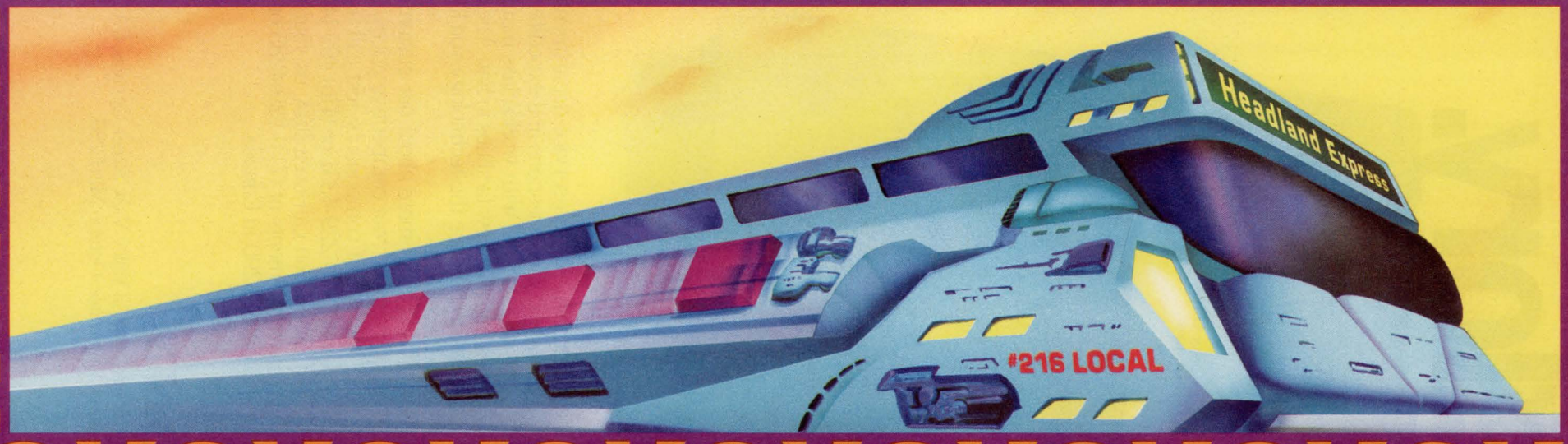

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The industry's first local bus VGA controller, the HT216, dramatically improves the performance of all graphics applications.

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HTK320—A 386DX-based High Performance Chip Set

The HTK320 significantly improves 386DX systems performance with a high degree of systems integration and support for local bus peripherals.

A High Degree of Systems Integration

This two-chip set design, which supports internal tag RAMs and reaches systems frequencies of up to 40MHz, consists of an ISA Bus controller chip and a Memory Controller Unit (MCU). With many features integrated directly into the chip set, a high performance, fully compatible IBM PC/AT can be developed with only four external TTL devices.

Local Bus CPU Implementation—The Bus of the Future

The chip set architecture supports the connection of high-speed I/O devices such as VGA, SCSI and LAN controllers directly on the 386DX local processor bus. This design eliminates the 8MHz ISA Bus bottleneck.

Advanced Cache Design

The cache controller of the HTK320 features integral tag RAMs, which allow for two-way set associativity for higher performance, while reducing component count and cost. A unique supporting feature of the cache architecture is a five-deep write buffer with byte gathering. DRAMs may be freely configured using 256K to 16MB devices.

Catch the Bus of the Future

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ANALOG SIMULATION

Behavioral models expedite simulation

Analog behavioral modeling is not the antithesis of Spice, but another level on the simulation hierarchy. It's not a question of whether you trade in Spice-level models for behavioral models, but for what phase of the design and for what types of circuits you'll use each.

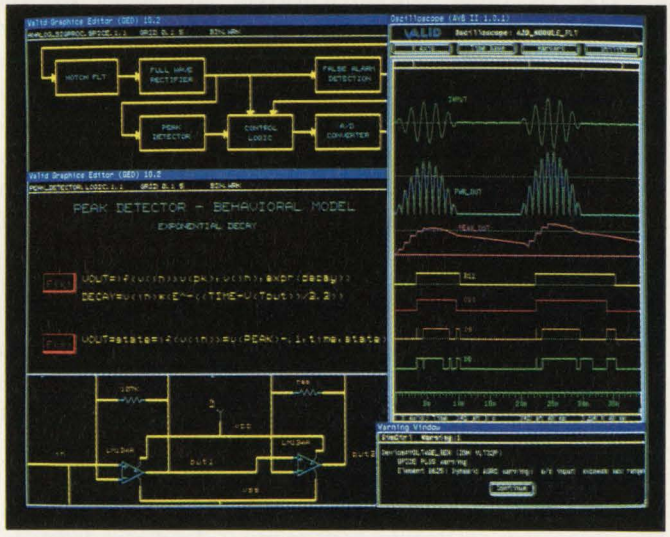
Anne Watson Swager,
Technical Editor

After finally conquering doubts and difficulties associated with simulating complex circuits with Spice, advancing to analog behavioral models may seem like too big a step, too fast. However, without using some form of behavioral modeling, reaching the end of a complete simulation can be difficult. Chances are very high that at some point during the simulation you'll hit a brick wall: no model for a crucial component exists, the circuit is too complex to simulate in a reasonable amount of time, or you simply can't model a certain part of the system using the basic electrical Spice elements.

These problems—lack of models, slow simulation speeds, and nonelectrical characteristics—are exactly what behavioral modeling can alleviate. Behavioral modeling is an attempt to capture a component's actions, without specifying that component's structural details. It lets you build models for components more easily, and speeds up simulation times.

Using behavioral modeling can be as simple as manipulating basic Spice primitives and polynomial statements or using an actual behavioral simulator, such as Analogy Inc's Saber. More often than not, you'll write your own behavioral models or statements. However, the macromodels available from IC vendors are a type of behavioral model, and you can obtain models from independent consultants. As part of a Spice course he teaches for RCG Research, Ron Kielkowski presents behavioral models for devices ranging from adders and subtracters to 555 timers.

One example of how behavioral models can expedite simulation is in emulating the behavior of a complex load. You may know certain mathematical or transfer-function characteristics of that load, but there may be no circuit equivalent. Thus, it is a futile exercise to develop a model using Spice primitives. It is also futile to run a simulation without taking into account the load's effect. Using a behavioral model of the load makes the simulation more realistic and saves unnecessary modeling time.



***Behavioral modeling isn't necessarily synonymous with** ideal modeling. This model of a peak detector, implemented with Valid's Profile option, includes decay effects. The software also notifies the user that the ADC's input exceeds its input range.*

Analog Simulation

Behavioral modeling can exist both within and outside the realm of circuit simulation. Most of the software in **Table 1** is circuit-design and -verification oriented, but software also exists that purely serves block-level simulations. Because of its conceptual/analytical nature, behavioral modeling is a good tool with which to simulate your overall system. Then, when simulating circuit detail, these models can substitute for peripheral components while you are concentrating on others to speed the simulation.

Behavioral models don't necessarily emulate only a component's *ideal* characteristics. Although many of the Spice behavioral features model only ideal summers or integrators, table look-up features let you insert real data. And, using hardware-description languages, you can include as much detail as necessary to capture those component effects that have the greatest bearing on your design. Ian Getreu, Analogy Inc's VP of Modeling, emphasizes that behavioral modeling of analog components is a technique, *not* a level of accuracy. According to Getreu, behavioral models implemented with a hardware-description language "can be more accurate, just as accurate, or less accurate than models obtained from primitive or functional approaches." It's up to you to decide how many real effects are necessary for your simulation.

Drawbacks exist

Despite its advantages, behavioral simulation is not a panacea for all modeling problems. Some effects are impossible to model. Some expressions have no solution, or have solutions that are infinitely large. Any simulator will still have to deal with the stiff mathematical problem of discontinuities. According to Dick Akers, director of Mentor Graphics' analog business unit, the more discontinuities, the more difficulties any analog simulator will have. A behavioral simulation can still have convergence problems when modeling a truly general nonlinearity.

> Behavioral modeling's conceptual/analytical nature makes it a good tool for simulating your system.

Thus, it's important to take a good look at what you really need to accomplish and pick the appropriate tools. Do you need to be able to write your own models? Is model accuracy or model speed more important? Do you need both fast and accurate models for different phases of the design process? Do you simply want to augment your existing library of Spice models with a few behavioral ones?

Unfortunately, matching your requirements with the available software requires wading through vendor rhetoric. There is not a single definition of behavioral modeling. One broad definition of a behavioral model is any model that is more abstract than a transistor-level model. Another definition is the ability to model a component using mathematical equations. Macromodels are also often loosely called behavioral—they still use the basic Spice set of electrical elements, but instead of trying to implement an IC's function exactly, a macromodel uses electronic components to mimic other components' functions.

In some cases, Spice vendors' behavioral models are macromodels that implement certain functions, such as ideal integrators and summers. Other upgraded Spice software includes features that let you directly input equations and table-look-up features in Spice text files. Still other behavioral models are based on hardware-description languages, which provide the greatest flexibility, to describe both electrical and nonelectrical components.

The various definitions and implementations of behavioral modeling don't oppose one another, but refer to different levels in the simulation hierarchy. Understanding the limits of each step in the hierarchy will help determine whether the models available at each step are sufficient for your simulation task.

Fit modeling into a hierarchy

There are essentially three analog-simulation levels: structural, functional/macromodel, and pure behavioral. The structural level, often called the primitive level, is exemplified by Spice. At the structural level, the simulator uses a basic set of components, which in Spice is a set of about 30 devices including resistors, capacitors, inductors, transistors, and various voltage and current sources. A structural-level simulation implements an entire circuit in terms of these basic elements.

One step up from the structural level is the functional level. At this level, the model omits certain structural details to speed up the simulation. An example of a functional-level model is the Boyle op amp. This model still uses basic structural elements, but isn't an exact replica of any particular op amp. Instead of exactly mimicking a circuit, this model uses predefined building blocks, such as current sources, to model the circuit's action.

All macromodels are essentially functional-level models. Some CAE vendors would argue that macromodels are behavioral because they omit structural detail. Others claim

Analog Simulation

Table 1—Analog behavioral modeling features of representative simulators

Company	Simulator and option name	General description	Key behavioral modeling features	Hardware platforms	Starting price
Anacad	Eldo simulator with Eldo-Fas	Proprietary simulator and modeling language aimed primarily for large-IC designers.	Capable of time- and frequency-domain simulation of any lumped parameter, linear, or nonlinear system.	Sun, HP/Apollo, DEC, IBM	$30,000
Analogy	Saber simulator with Mast language	Proprietary simulator based on Mast hardware-description language.	Flexible language lets you model real behaviors, nonelectrical components, and mixed analog/digital systems. Optional graphics package lets users implement functions without writing Mast code. Includes Spice-level simulation capability.	Sun, HP/Apollo, DEC, SolBourne, and Intergraph	$15,000
Cadence Design Systems	Analog Artist with analog functional blocks library	Complete front-to-back design system including Cadence Spice.	Analog functional blocks library includes higher-level functions such as dividers, multipliers, poles, and level shifters.	Sun, HP/Apollo, DEC	$30,000 (Analog Artist) $5000 (library)
Contec Microelectronics	ContecSpice 1.1 with analog and digital behavioral options	Spice 3C.1-based, mixed-level circuit simulator.	Includes analog modeling options for digital and analog circuits. Models transfer functions, differential equations, and nonlinear functions.	PC, Sun	$4700 (PC) $9100 (Sun) $4500 (each option, PC) $8500 (each option, Sun)
Deutsch Research	TurboSpice	Spice 3E.2-based circuit simulator with backwards compatibility to Spice 2G.6.	Includes general functions blocks for which users supply defining set of equations.	PC, Mac	$1995
Electrical Engineering Software	Precise 4.0	Spice 2G.6-based circuit simulator.	Lets users write expressions using built-in math functions. Allows use of if-then-else constructs using a subset of the C programming language.	Sun, HP/Apollo, DEC, IBM, and Cray	$19,500
Harris Semiconductor	Mixed-Signal Fastrack with Asim	Complete design system linked to company's fabrication processes. Asim linked to cdsSpice using subroutine calls.	Automatically generates macro and behavioral models using mathematical expressions, tabular look-up models, and s-domain models.	Sun, HP/Apollo	$30,000 (Fastrack with cdsSpice) $10,000 (Asim)
Intusoft	IsSpice	Spice 2G.6-based circuit simulator.	Includes math functions built from Spice primitives.	PC	$95
Mentor Graphics	Analog Station with Accusim 7.1	Spice 2E and 2G.6-based circuit simulator.	Library of system modeling blocks includes mathematical, frequency-domain, and time-domain models. Predefined models include dc motors and tachometers.	HP/Apollo	$24,900 (simulator) $7900 (parts library)
Meta-Software	HSpice	Spice 2G.6-based circuit simulator.	Enhanced voltage- and current-controlled sources let users describe functions with equations, tables, and delay elements.	PC, Sun, HP/Apollo, DEC, Cray	$2800 (PC) $20,000 (average workstation)
MicroSim	PSpice with analog behavioral option	Spice 2G.6-based circuit simulator.	Enhanced voltage- and current-controlled sources let users describe functions with equations, tables, and transfer functions. Also lets users enter a set of filter parameters.	PC, Mac, Sun, VAX/VMS	$950 (PSpice) $450 (option)
Spectrum Software	Micro-Cap III	Proprietary equation solver uses Spice-like device models. Includes schematic-based editor and window-based user interface.	Enhanced controlled sources let users enter mathematical expressions and use look-up tables.	IBM PC/XT/AT and compatibles	$1495
Tesoft	Tesla and Modgen model generator	Proprietary block-diagram simulator.	Models circuits at the block level only, using a model library consisting of 50 blocks, which include analog functions, digital functions, and test and measurement blocks.	PC/XT	$695 (simulator) $495 (model generator)
Valid Logic Systems	Analog Workbench II with profile option	Complete design system with enhanced Spice-based simulator.	Complete design system includes piece-wise linear analysis and enhancements to the company's Spice Plus. Lets users enter designs at the block-diagram level using basic analog blocks. Includes if-then-else constructs.	Sun, Dec, IBM	$17,000 (Analog Workbench II) $15,000 (Profile)

Note:
Price includes all software necessary to use behavioral modeling features.

Analog Simulation

that macromodel is just a fancy name for a subcircuit. Semantics aside, the bottom line is that macromodels are built from the same primitive-level blocks, and are thus subject to whatever benefits or limitations those blocks have. Macromodels can be quite complex and offer a great degree of flexibility.

The most abstract level of analog modeling is behavioral. A purely behavioral model doesn't contain any information about actual physical structure. A behavioral model doesn't have to convert models to fit a set of predefined primitives.

You'll find so-called behavioral features implemented at each level of this hierarchy. For example, the ability to model circuits behaviorally exists even in the most basic Spice package. You could argue that modeling an ideal op amp using a voltage-controlled voltage source is one example of a behavioral model. In fact, most behavioral features of Spice and Spice upgrades are related to manipulating the control sources.

One of the most basic forms of behavioral modeling at the structural level is the use of Spice's polynomial source. You can use the polynomial source to implement functions, such as summers and multipliers involving one or two controlled sources. These 1-D and 2-D polynomial sources solve for a function according to equations of the following respective forms:

$$V_{OUT}=P_0+P_1V_1+P_2V_1^2+P_3V_1^3\ldots$$

and

$$V_{OUT}=P_0+P_1V_1+P_2V_2+P_3V_1^2+P_4V_1V_2+P_5V_2^2\ldots$$

By selecting constants for the various P coefficients, you can create a variety of functions, including a squarer, a multiplier, and a summer. To square a single voltage or current, use the 1-D poly statement. Set the P_2 coefficient to 1 and set all others to zero. To create a summer that adds V_1 and V_2, simply

For more information . . .

For more information on the analog-behavioral-modeling software discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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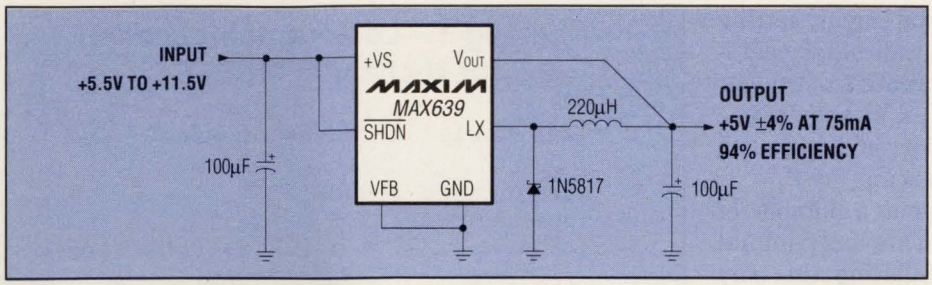

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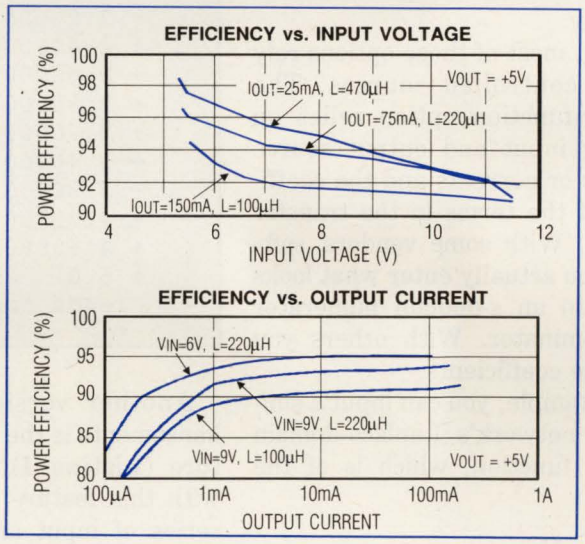


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use the 2-D poly statement, setting P_1 and P_2 to 1 and all other coefficients to zero. To create a multiplier that computes $V_1 \times V_2$, again use the 2-D poly source and make all coefficients zero, except for P_4.

You can implement a number of functions using this polynomial source, but manipulating the poly statement can only go so far. For example, it's not nearly as straightforward to take the square root of a voltage as it is to square that voltage. Thus, much of the software listed in **Table 1** goes beyond basic Spice by including transfer and equation-based functions. These upgrades fit into the functional/macromodel level in the simulation hierarchy.

Again, most of these options rely on the controlled sources. The transfer-function option relies on defining input and output source voltages or currents and the coefficients of the terms in the transfer function. With some vendors' software, you actually enter what looks similar to an s-domain numerator or denominator. With others you enter the coefficients.

For example, you can input a simple RC network's Laplace-domain transfer function, which is of the form

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1}{sRC+1}.$$

Using R = 1 kΩ and C = 1 μF, the corresponding PSpice text code looks like

```
ERC 5 0 LAPLACE {V(10)}= {1/(1+ .001*s)}.
```

In ContecSpice, the text code would look like

```
erc out 0 in 0 dncoeffs=1e-3 1
```

where *dncoeffs* stands for the denominator coefficients.

Listing 1—Look-up table model for N-channel MOSFET

```
*
* behavorial n-channel mosfet
*
* drain gate source
.subckt nmos 1 2 3
gn 3 1 npwl(1) 2 3 scale=0.008 level=1
* VOLTAGE        RESISTANCE
+ 0.             495.8840g
+ 200.00000m     456.0938g
+ 400.00000m     141.6902g
+ 600.00000m     7.0624g
+ 800.00000m     258.9313meg
+ 1.00000        6.4866meg
+ 1.20000        842.9467k
+ 1.40000        21.6882k
+ 1.60000        170.8367k
+ 1.80000        106.4944k
+ 2.00000        72.7598k
+ 2.20000        52.4632k
+ 2.40000        38.5634k
+ 2.60000        8.8056k
+ 2.80000        5.2543k
+ 3.00000        4.3553k
+ 3.40000        3.4950k
+ 3.80000        2.0534k
+ 4.20000        2.7852k
+ 4.60000        2.5k
+ 5.0            2.3k
 .ends nmos
 *
```

Another version of Spice enhancements is the table look-up feature (**Listing 1**). Using software with this feature, you can enter a series of input and output values in a table. During the simulation, the program compares an expression that you define to this set of values, and linearly interpolates between the entries. **Listing 1** is one example and shows the HSpice code for a behavioral N-channel MOSFET model. Although most of the features described up to this point model ideal behaviors, this table feature lets you use real data from either a data-sheet curve or actual test data.

Few of the Spice vendors have added language-type constructs to their packages. Exceptions are Electrical Engineering's Precise version 4.0 and Valid Logic System's Profile, which let you use if-then-else statements. Profile builds on the company's Spice Plus simulator, and includes various enhancements and piece-wise linear models.

Hardware-description languages represent the most abstract way to model a circuit and a high-level function. Currently, it's difficult to speak of analog hardware-description languages without almost exclusively referring to Analogy's Saber simulator and Mast language. However, other languages exist, and more are starting to appear, such as Dazix/Intergraph's Diablo, which is currently in beta testing and will be available in the first quarter of 1992.

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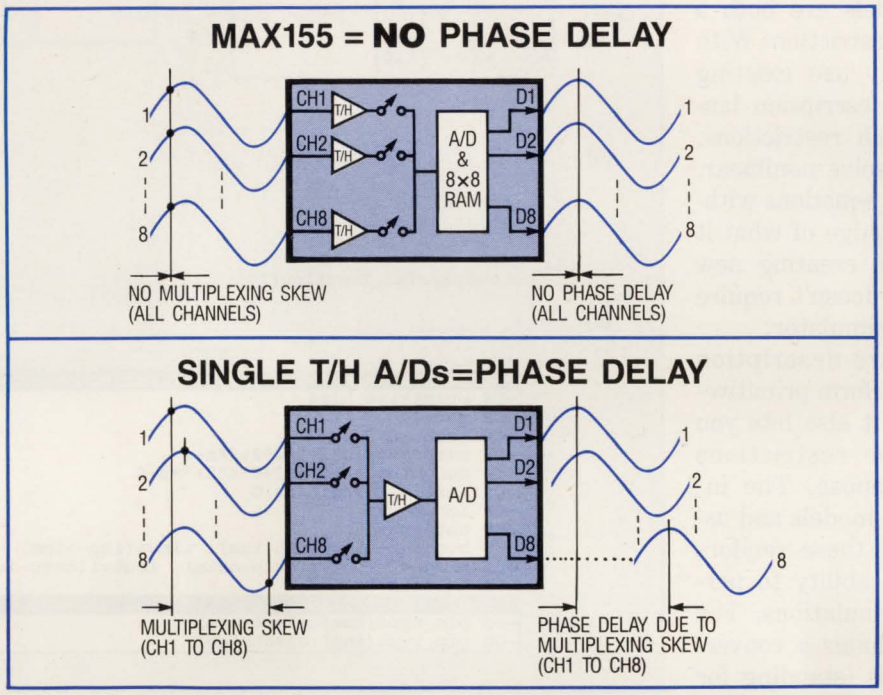

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Analog Simulation

The major difference between a hardware-description language and Spice-level simulators is the coupling between the simulator and the models. Saber for example, unlike Spice, has no built-in models. Spice's built-in models are both a convenience and a restriction. With Spice, you can only use existing models. Hardware-description languages have no such restrictions. Saber's algorithms solve nonlinear, ordinary differential equations without any prior knowledge of what it is simulating. Thus, creating new or different models doesn't require any changes to the simulator.

Using a hardware-description language lets you perform primitive-level simulations, but also lets you get away from the restrictions those primitives impose. The installed base of Spice models and users is so great, that these vendors have to include the ability to perform Spice level simulations. For example, Saber includes a conversion program, Spitos (standing for Spice to Saber), that lets you input Spice code.

The one catch with hardware-description languages is the language itself. Although Saber includes a large library of function blocks, to create new models you may have to learn the Mast language. Unfortunately, Mast doesn't conform to any familiar syntax. Because engineers don't want to learn yet another language, Analogy has added some graphical design features to make it easier for users to generate Mast code (**Fig 1**). Diablo, which runs on Dazix's Apex simulator, has a C-like syntax and includes a graphical interface.

A discussion of languages invariably leads to a discussion of the development of a standard analog hardware-description language. A volunteer committee of analog simulation software vendors is actively evaluating various approaches and features of a standard language. However, a standard language is clearly in its formative stages. CAE vendors themselves admit that any agreed-upon standard for an analog hardware-description language is a way off.

Despite the lack of common definitions and standards, behavioral modeling has some real benefits now. If you need to take advantage of the current crop of behavioral tools, be aware that they won't necessarily become part of any standard. Be aware also that you may have to modify your tool set down the line. The safest bet is to stay with a standard set of primitive-level models, such as Spice, simply because of the current installed base. Vendors definitely respect Spice's usefulness and pervasiveness. Any models you develop or obtain as part of a library, if Spice compatible, will run in some form on the simulators of the future. EDN

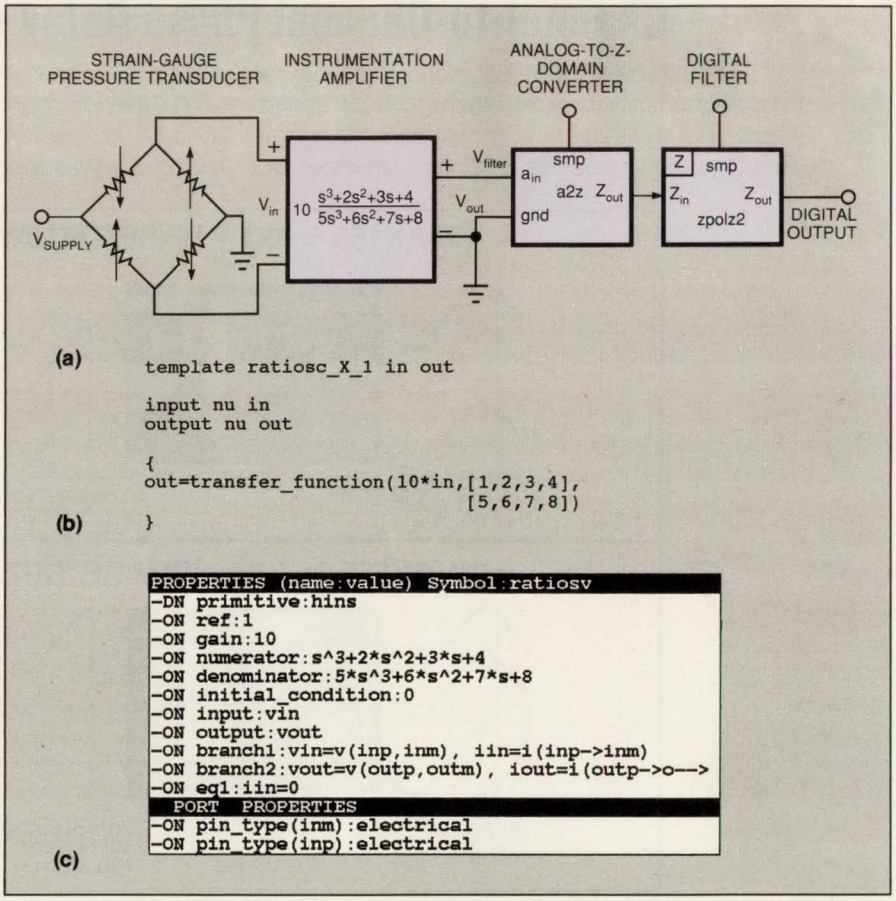

***Fig 1—Graphical design software makes** using a hardware-description language easier. For this pressure sensing circuit (**a**), Analogy's Design Star front end generates the underlying code (**b**) for the transfer-function instrumentation amplifier based on user-supplied parameters and equations (**c**).*

Reference

1. Kerridge, Brian, "Accurate models mirror extremes of operation," *EDN*, May 9, 1991, pg 61.

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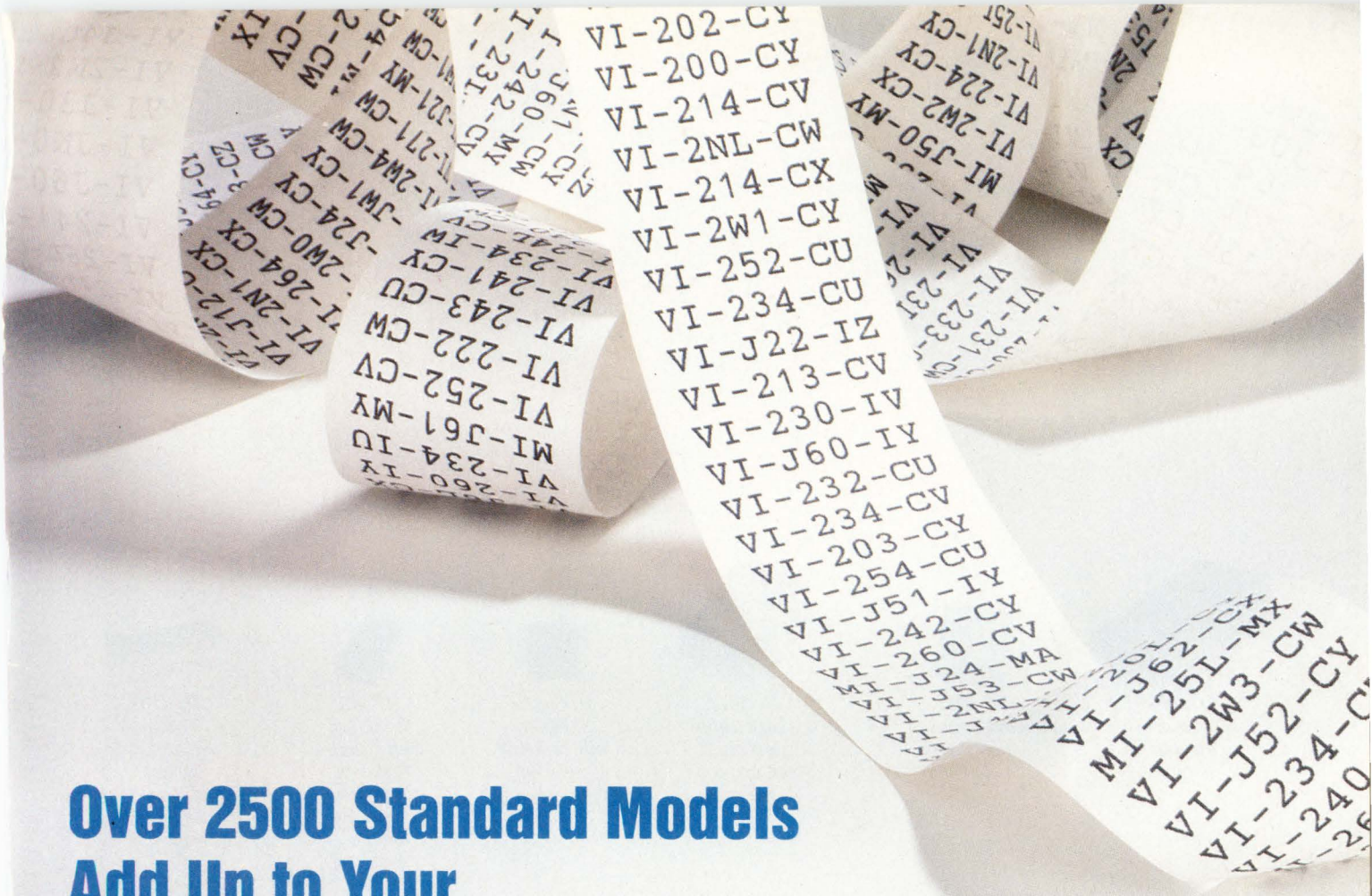

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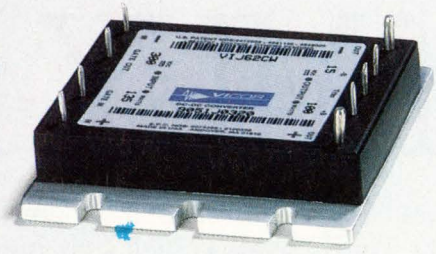

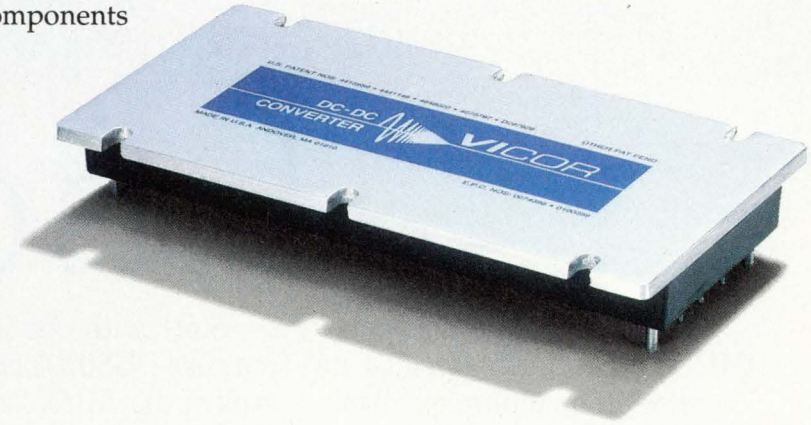

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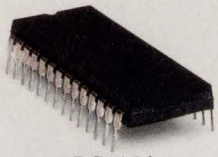
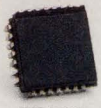
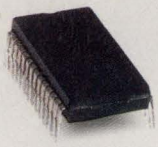


DG506A. 16-channel with junction isolation.



HI-506. 16-channel with dielectric isolation.



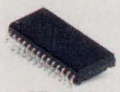
DG507A. Differential 8-channel with junction isolation.

HI-508A. 8-channel with dielectric isolation and overvoltage protection.

HI-548. 8-channel with dielectric isolation, overvoltage protection, and Rds_{ON} matching.

IH-5108. 8-channel with dielectric isolation, fault protection and Rds_{ON} matching.

HI-506A. 16-channel with dielectric isolation and overvoltage protection.



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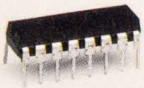
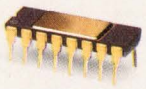


DG508A. 8-channel with junction isolation.

HI-508. 8-channel with dielectric isolation.



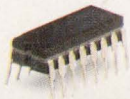
DG509A. Differential 4-channel with junction isolation.

HI-509. Differential 4-channel with dielectric isolation.

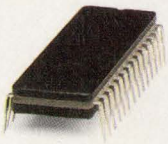
HI-507. Differential 8-channel with dielectric isolation.

HI-509A. Differential 4-channel with dielectric isolation and overvoltage protection.

HI-549. Differential 4-channel with dielectric isolation, overvoltage protection, and Rds_{ON} matching.



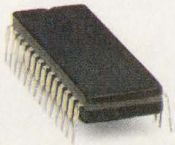
IH-5208. Differential 4-channel with dielectric isolation, fault protection, and Rds_{ON} matching.



IH-5116. 16-channel with dielectric isolation, fault protection, and Rds_{ON} matching.

HI-507A. Differential 8-channel with dielectric isolation and overvoltage protection.

HI-547. Differential 8-channel with dielectric isolation, overvoltage protection, and Rds_{ON} matching.



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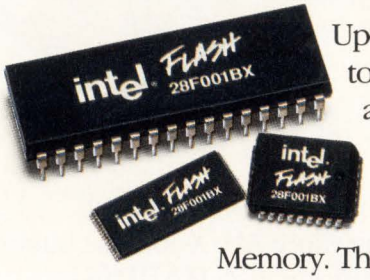

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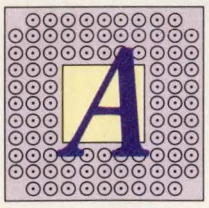
As current-generation μPs approach the RISC ideal of executing one instruction per cycle, some μPs are using super techniques to achieve even higher performance.

Michael Markowitz, Technical Editor



mong recently announced and released high-end processors, three approaches threaten to supersede current RISC processors. The emerging superlative μPs attain their superb performance via superscalar, superpipelined, and very-long-instruction-word (VLIW) techniques. One of the fundamental tenets of RISC (reduced-instruction-set computer) based architectures is that high performance results from single-cycle execution of most instructions. As basic RISC implementations approach that barrier—vendors claim many RISC processors operate in the range of 1.2 to 1.5 instructions per cycle, depending on the instruction mix and cache size—μPs that use these advanced scheduling techniques are breaking through it.

Though more complex in implementation, the superscalar approach to high performance is conceptually simpler than the superpipelined approach. Superscalar processors contain multiple execution units. During each clock cycle, a superscalar μP can theoretically execute as many instructions as it contains execution units because each execution unit operates independent of the others. These execution units can perform integer, floating-point, or fixed-point operations or specialized functions such as multiplication or barrel shifts. Among the available crop of superscalar implementations are Intel's i960, National's 32SF641, and SGS Thomson-Inmos' T9000. IBM's RS/6000 and Intergraph's C4 Clipper are multichip superscalar processors.

In contrast, a superpipelined approach, as found in the C4 and in the R4000, which will soon be available from several vendors, refines the existing RISC pipeline by breaking each stage of the pipe into m latched substages. As a result, the superpipelined processor's internal circuits can operate at (cycle time)/m. In practice, both the C4 and the R4000 use two substages that allow them to run the fetch, decode, and execution stages twice as fast as the system clock.

As their name implies, VLIW μPs' instructions are wide enough to specify multiple instructions. The VLIW μP, is, in some senses, a subtype of superscalar processors. For greatest performance, these processors, like superscalar processors, rely on multiple execution units. According to **Ref 2**, one difference between VLIW and superscalar processors is that VLIW instructions are easier to decode and schedule because each part of an instruction is mapped to its own subprocessor with its own decodes. Superscalar processors, on the other hand, must dynamically select and issue instructions at run time based on what resources are already being used and whether the necessary operands are available. The only current commercial VLIW implementation is Intel's i860 μP.

All three techniques have advantages and disadvantages. Superscalar's advantage is that, in theory, the architecture scales well; to increase performance further, just add another functional unit. The benefit of

Superpipelined, superscalar, and very-long-instruction-word (VLIW) μPs can speed information flow to a torrent compared to the trickle of conventional μPs. (Photo courtesy Intergraph Corp, Advanced Processor Div; photography, Tim Tabke, Phoenix Productions; design, Greg Meadows, Meadows Graphic Arts; model making, Steve Pombo, Pombo Enterprises.)

Superscalar μPs require complicated scheduling and scoreboarding to ensure proper instruction issue.

superpipelining is its ability to increase the throughput of existing code without recompiling. VLIW machines stand out for the density of their code resulting from the ease of parallel scheduling in hardware, provided the parallelism of the application code meets or exceeds the parallelism of the processor.

All of these approaches suffer from a common problem. Because these techniques execute instructions in parallel, the applications they are running must have high instruction-level parallelism. Applications with such parallelism have three characteristics: They have few conditional branches or jumps; instructions don't depend on the results of other, immediately preceding instructions; and proximate instructions don't compete for the same hardware resources.

Conditional branches and jumps can stall the pipelines of all of these super processors as the pipes are flushed and refilled. Anecdotal data suggests that these branches and jumps occur, on average, every six to nine instructions, depending on the application. An often-discussed technique to alleviate some of these stalls is branch prediction or speculative execution, where the processor makes educated guesses about whether a branch is or isn't taken. National's Swordfish uses branch prediction. The AMD29000 has a Branch Target Cache that caches the taken branches in the expectation that taken branches are likely to be taken in subsequent iterations.

Superpipelined processors suffer from conditional branches and jumps as a result of greater startup times. In **Fig 1**, adapted from Jouppi's research (**Refs 1, 2,** and **3**), notice how long it takes to begin execution of two instructions using the various techniques. An ideal base machine starts processing the second instruction on cycle 1. Both the ideal 2nd-degree superscalar processor and the VLIW processor, which, in this example, contain two functional units, start the second instruction as soon as they begin operating. The 2nd-degree superpipelined processor, whose pipeline contains two substages, starts this instruction on cycle 0.5. This processor pays a similar half-cycle penalty on all subsequent conditional jumps and branches.

The instructions in many applications use the results of preceding instructions as operands. If subsequent instructions need these results before they are available, the μP must stall, crippling attempts at parallel execution. In some cases, compilers can reorganize the code to extract some additional parallelism, but compiler technology is not as efficient as it needs to be.

Jouppi defined a class conflict as occurring when succeeding instructions compete for the same hardware resources. Because superpipelining keeps instructions flowing through a single pipe, competing for resources isn't a problem in superpipelined μPs. And since VLIW instructions account for that processor type's resources, VLIW doesn't suffer from class conflicts either. Superscalar processors, though, may suffer performance degradation as a result of class conflicts.

The potential class conflicts of all superscalar devices lead to instruction-issue restrictions. The performance of each superscalar implementation degrades when instructions that violate these restrictions are fed into the devices. The only issue restrictions on superpipelined and VLIW processors are due to data dependencies—data must be available before the processor tries to use it—and delayed branch conditions.

The logic complexity of a superscalar design comes from the instruction-issue and scoreboarding features necessary to avoid class conflicts and unmet data dependencies. The scoreboard monitors when results and registers are available for successive operations. The in-

Text continued on pg 88

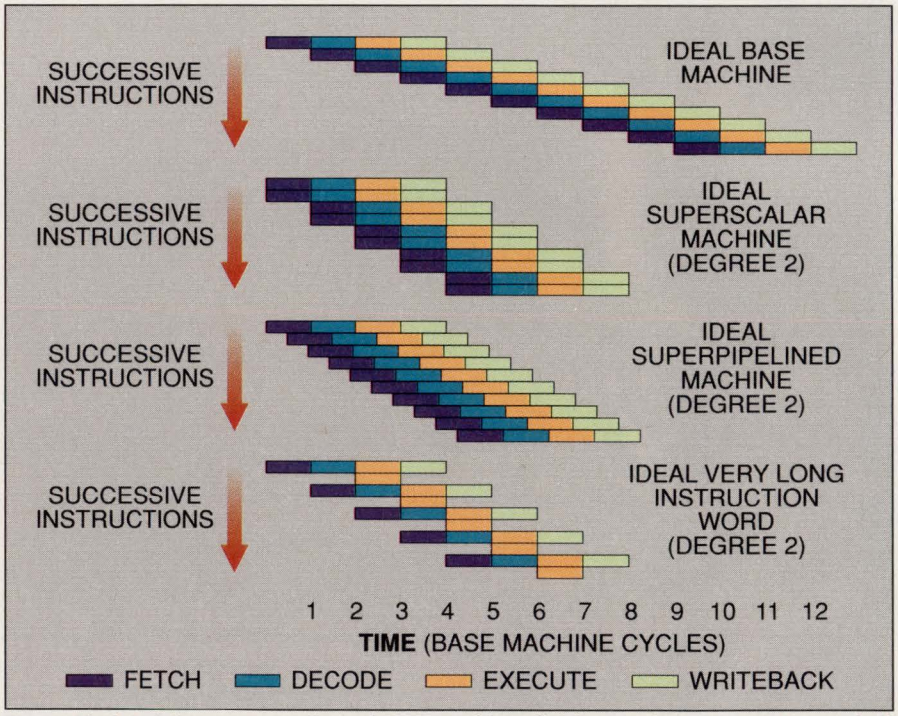
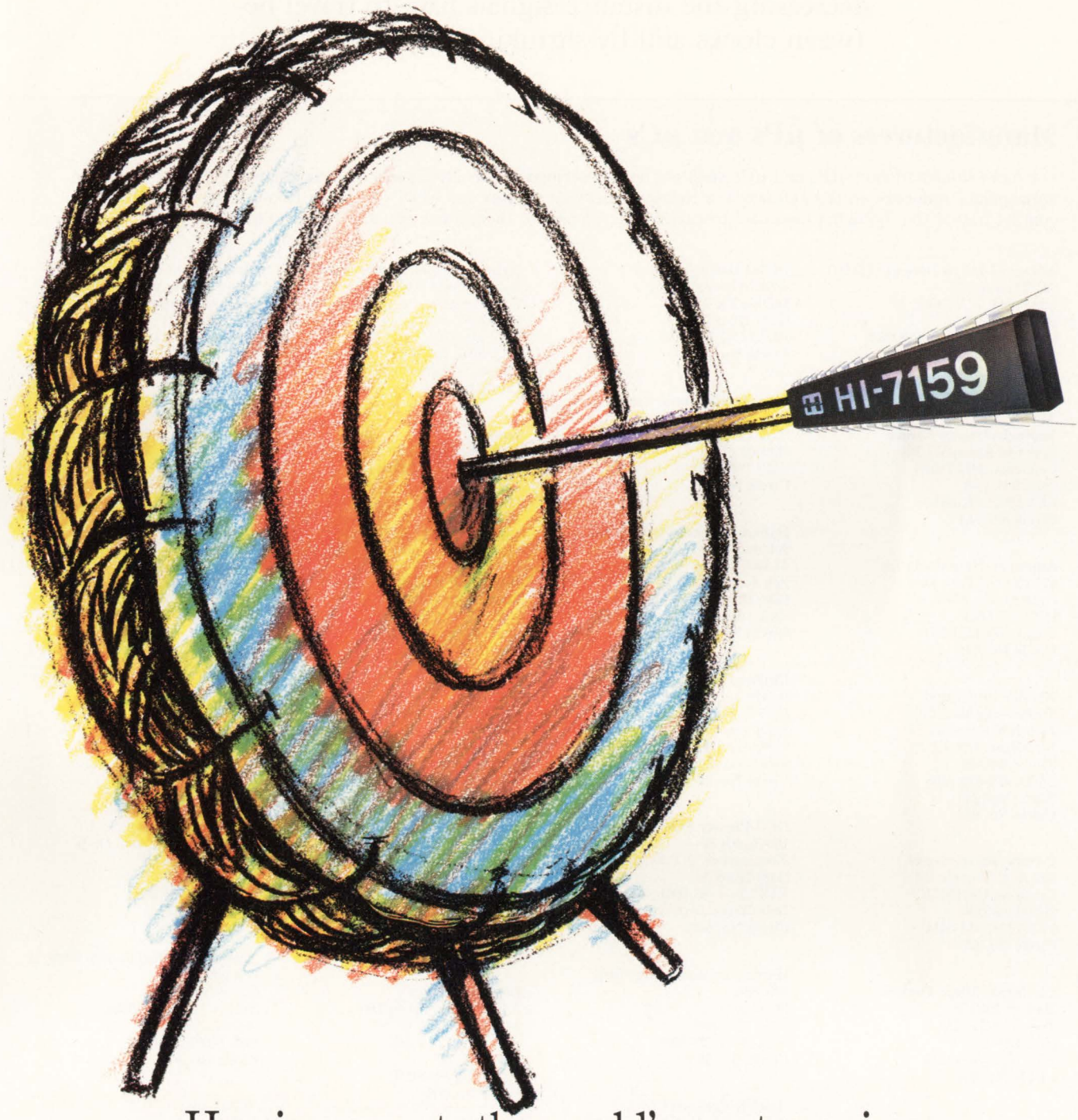


Fig 1—Ideal 2nd-degree superscalar and VLIW machines finish executing 10 instructions a half cycle faster than a 2nd-degree superpipelined CPU. Unfortunately, data dependencies, conditional branches, and instruction mixes cause deviations from the ideal.



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struction-issue logic acts as a traffic cop by tracking the hardware resources, instruction stream, and scoreboard. Knowing the processor's status allows the logic to issue instructions to use resources when they are ready.

Superpipelining's proponents have one major argument against the superscalar approach. The argument recognizes the impact of multiple execution units on floating-point and signal-processing-rich applications. These proponents claim though that superscalar techniques do little to improve the throughput of most programs. Existing code would need to be recompiled to take advantage of a superscalar processor's multiple execution units. In addition, most applications are heavily loaded with integer operations, and multiple execution units will do little to improve the performance of these programs.

As evidenced by the C4's architecture, there is nothing to preclude superscalar devices from implementing a superpipeline. Nor is there any impediment to superpipelined processors adopting multiple execution units, beyond physical and logical design issues. In fact, in response to the question of whether making the Mips II architecture a 2nd-degree superpipelined μP didn't provide simply a one-shot boost to performance, John Mashey, VP of systems technology at Mips Computer Systems, suggested that the logical evolution of superpipelined processors would be to add multiple execution units. EDN

Table 1—Index to μP and μC chips in EDN's annual directory

Application areas	Page	μP/μC
8-bit	89	COP800
	90	PIC 165x family
	91	TLCS-90
	92	8048 family
	93	8051/8052 family
	94	TMS370 family
	97	6805/68HC05
	98	6801/6301/68HC11
	103	6500/1, 65C134, 65C265, 38000, 37700
	104	Z8, Super8
	107	Z80
	108	ST9
	111	Z180/HD64180
	112	6800/6802, 6809/6309
	115	650x/65C0x
	116	8086/8088
	121	Z280
16-bit	122	H8/300 family
	125	78K series
	126	65C816/65C802
	129	80186/80188
	130	80286
	135	MCS-96 family
	136	HPC16000
	139	80C166
32-bit	140	1750A
	149	Transputer family
	150	Z8000, Z16C00
	153	340x0 Graphics μP family
	154	68000
	159	68300
	160	Series 32000
	165	VY86Cxxx ARM
	166	386
	171	486
	172	Clipper
	173	Hyperstone
	176	SPARC family
	177	Mips family
	178	29000
	179	88000
	180	i960 family
	181	i860 family

References

1. Jouppi, Norman, "Superscalar vs Superpipelined Machines," *Computer Architecture News*, June 1988, pg 71.
2. Jouppi, Norman, and David Wall, "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," Proceedings of the Third International Conference on Architectural Support for Programming Languages and Operating Systems, IEEE Computer Society Press, April 1989.
3. Jouppi, Norman, "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and its Effect on Performance," IEEE Transactions on Computers, December 1989, pg 1645.
4. Case, Brian, "Design Issues for Next-Generation Processors," Microprocessor Report, September 19, 1990, pg 8.

Article Interest Quotient
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COP800

8-BIT CMOS

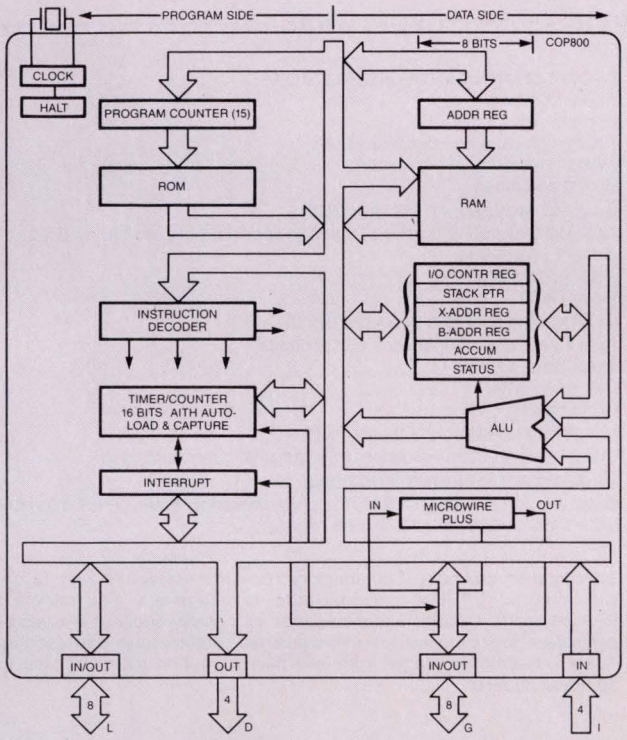
AVAILABILITY: Now.
COST: Less than $1 to $5 for standard parts in high volume.
SECOND SOURCE: Sierra Semiconductor.
CORE: Sierra uses the COP800 core for custom designs. National designs with a configurable-controller approach using a set of microcontroller building blocks.

Description: 8-bit CMOS single-chip family in which varying amounts of memory, peripheral functions, and I/O surround a purposely simple core μP. Some 20 parts exist. Initial core has provision for addressing 32-kbyte program memory. The program and data memory are treated separately, so the COP800 has a Harvard architecture.

National Semiconductor Corp
Phone (408) 721-5000
For more information, Circle No. 351

Status: Having gained one of the leadership positions in the 4-bit microcontroller field with its COP400 and 16-bit HPC, National introduced this 8-bit controller to fill the gap between those two devices. The architecture of the core μP seems quite simple—a bit like the Motorola 6805. The core-based parts, built on National's double-metal process, are shrinkable to submicron levels.

HARDWARE CHARACTERISTICS SOFTWARE



Hardware note:
1. Diagram shows basic COP800-family architecture. Each member of growing family has an emulator part that replaces standard masked-ROM with EEPROM or EPROM.

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, and subtract with borrow.
Logicals include rotates, shift compares, and conditionals.
Decimal correct.
Increment and decrement.
Bit manipulation: set, reset, and test individual bits in data memory, which includes those in data registers and I/O ports.

II—DATA-MOVEMENT INSTRUCTIONS
Load and exchange instructions with optional automatic post increment or decrement of the associated pointer. Most allow the use of either the B or X pointer. Decrement register and skip if zero.

III—PROGRAM-MANIPULATION INSTR
Jump instructions: relative, absolute, absolute long, and indirect.
Subroutine, subroutine long, return, and skip (only the amount of available RAM limits subroutine levels).
Push and pop.

IV—PROGRAM-STATUS-MANIP INSTR
ALU-driven decision bits in status register (PSW) appear to be limited to carry and half-carry flags. These, as well as interrupt control bits for various on- and off-chip interrupt sources, can be set and reset.

V—POWER-SAVING INSTRUCTIONS
Halt mode, which is entered by setting data bit and exited by reset or low-to-high transition on the CKO pin.

Note:
1. Program-branch decisions are implemented in skip-the-next-instruction manner.

Specification summary: 15-bit program counter can address 32-byte program memory, which can include data and data tables. All data, control, and I/O registers are mapped into data-side memory space. Two bidirectional 8-bit and two unidirectional 4-bit I/O ports max. Each I/O pin has software-selectable options to adapt the chip to specific applications. On-chip peripheral functions include software-selectable I/O of as many as 39 I/O pins, 3-wire serial I/O, 16-bit timer/counter with capture register and auto reload, and a multisource interrupt. Maximum speed is 1-μsec instruction cycle (most instructions take one cycle). Clock for 1-μsec cycle is 10 MHz. Operates over 2.5 to 6V range and draws 9 mA running full speed at 1-μsec cycles but is typically less than 1 μA when halted.

Industrial version (−40 to +85°C)	ROM/EPROM/ EEPROM (bytes)	RAM (bytes)	I/O pins	Interrupt (sources)	Timer base counters	Size (pins)	Other
COP820CJ	1.0k	64	24	3	2	28	Brown-out
COP822CJ	1.0k	64	16	3	2	20	protection, comparator, watchdog timer
COP8640	2.0k	64	24	3	1	28	64×8-bit
COP8642	2.0k	64	16	3	1	20	in RAM
COP8620	1.0k	64	24	3	1	28	64×8-bit
COP8622	1.0k	64	16	3	1	20	in RAM
COP840C	2.0k	128	24	3	1	28	
COP842C	2.0k	128	16	3	1	20	
COP880C	4.0k	128	36	3	1	40/44	
COP881C	4.0k	128	24	3	1	28	
COP8780C	4.0k EPROM	128	36	3	1	40/44	EPROM
COP8781C	4.0k EPROM	128	24	3	1	28	& OTP
COP8742*	2.0k	128	16	3	1	20	EPROM & OTP
COP884CG	4.0k	192	23	12	3	28	3 PWM & UART
COP884CL	4.0k	128	23	10	2	28	2 PWM
COP884CS	4.0k	192	23	12	1	28	1 PWM & UART
COP888CF	4.0k	128	33/37	10	2	40/44	2 PWM & A/D
COP888CG	4.0k	192	35/39	14	3	40/44	3 PWM & UART
COP888CL	4.0k	128	33/39	10	2	40/44	2 PWM
COP888CS	4.0k	192	35/39	14	1	40/44	1 PWM & UART
COP888EG	8k	256	35/39	14	3	40/44	3 PWM & UART
COP884EG	8k	256	23	12	3	28	3 PWM & UART

*Available in 1992
All devices implement their stacks in RAM and have at least 1 serial I/O port
MIL temperature range available

HARDWARE SUPPORT SOFTWARE

Supported on National COP800 Development Systems. The system can be used in conjunction with IBM PC as host. Applications Hotline: (408) 721-5582. Third-party support from Meta-Link Icemaster includes in-circuit emulator and symbolic debugger.

Cross-assembler for IBM PC and other computers. Form-fit emulators are available for every member of the family. These parts are 2-chip hybrids or single-chip EPROMs or EEPROMs. Assembler and simulator are part of National's Designer's Toolkit.

PIC 16C5X FAMILY

8-BIT CMOS

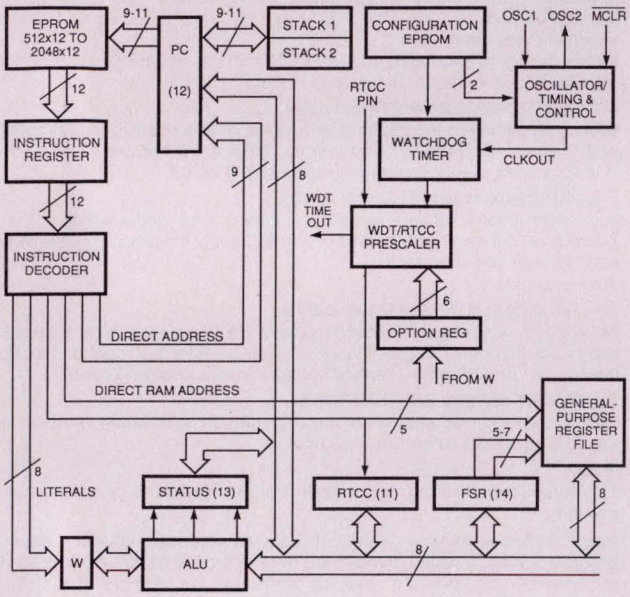
AVAILABILITY: Now.
COST: Less than $1.50 in volume.
SECOND SOURCE: None.

Microchip Technology Inc
Phone (602) 963-7373
For more information, Circle No. 352

Description: A family of single-chip CMOS EPROM-based microcontrollers that use only 33 single-cycle/single-word instructions. The family offers various amounts of I/O, RAM, and one-time programmable EPROM. Oscillator frequency ranges from dc to 20 MHz. Although it qualifies for the RISC moniker based on its 33 instructions, the label doesn't entirely fit. The family only has a 2-stage pipeline without delayed branches or load delay slots, rather than a 4- or 5-stage pipeline with delayed branches and load delay slots. The chips have a 2-address instruction format rather than the 3-address instruction format typical of RISC machines. Also, the PIC family must be programmed in assembly language—there are no high-level compilers.

Status: To date, 75 million PICs have been sold worldwide, generally in high-volume, low-end consumer, personal computer, and automotive applications. CMOS one-time programmable versions were introduced in 1989. Microchip has recently announced 3V one-time programmable versions. Derivatives containing analog and EEPROM are planned for winter release.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract.
Logicals.
Rotate right and left, decimal adjust.
Swap halves.
Bit set and clear.

II—DATA-MOVEMENT INSTRUCTIONS
All RAM (general- and special-purpose registers) accessible by direct or indirect addressing.
Page addressing.
Move file.

III—PROGRAM-MANIPULATION INSTR
Skip if zero (for comparisons and bit tests).
Move literal to W.
Call subroutine.
Go to routine.

IV—PROGRAM-STATUS-MANIP INSTR
Can bit test on status-register carry, decimal carry, and zero.

V—POWER-SAVING INSTRUCTIONS
Sleep stops oscillator, CLRWDT clears watchdog timer. TRIS instructs 3-state ports. Option loads option register.

Specification summary: Split-memory Harvard architecture with 12-bit-wide program EPROM and 8-bit-wide data registers. See table for EPROM and RAM sizes. Not expandable in memory because the microcontrollers are intended for self-contained, stand-alone applications. Power consumption ranges from less than 1 μA with the clock stop to 30 mA at 20 MHz.

Hardware notes:
1. 12-bit-wide instruction word allows single-cycle execution of all instructions.
2. All current devices are fully static, silicon-gate CMOS designs that feature an 8-bit real-time clock counter, watchdog timer, and 2-level program-counter-save stack for subroutine nesting.
3. Security EPROM fuse for user's code protection. Microchip also offers serialized coding in the EPROM.
4. A lower-cost RC-oscillator version is also available for applications that aren't timing critical.

HARDWARE SUPPORT SOFTWARE

Microchip offers two IBM PC-hosted development systems. One, the Pic-Pak II is a low-end development system that allows for assembly, execution, debugging, and analysis of microcode. The $495 price includes a PC-host or stand-alone programmer and UV-erasable samples. The Pic-ICE development system ($2495) offers full-speed emulation to support real-time code development. The system includes in-circuit emulation pod with an 8k capture-trace buffer, programmer, and diagnostic demo board. High-volume programming support is available from Microchip, Data I/O (Redmond, WA), and Logical Devices (Fort Lauderdale, FL).

Picalc cross-assembler is an IBM PC- or NEC 9801-hosted software tool that offers full-featured macro and conditional assembly capability. Picsim simulator software allows simulation of the PIC16C5X products on an instruction level. The simulator allows single-step, execute-until-break, and trace modes. Pic-ICE emulator software offers an interface with pull-down menus.

TLCS-90

8-BIT CMOS

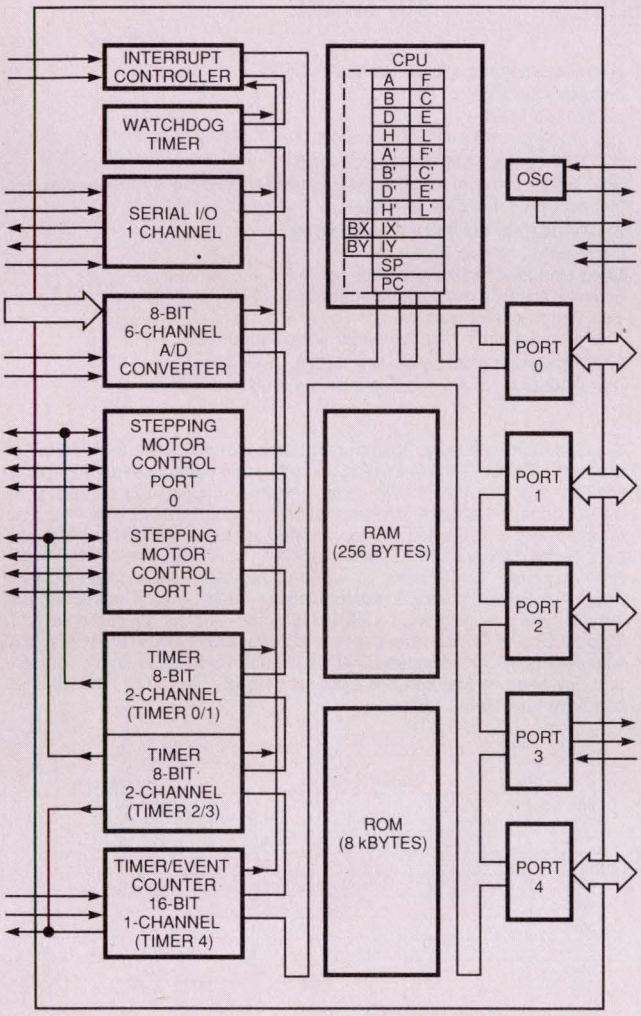
AVAILABILITY: Now.
COST: Prices range from $3.75 to $10 (10,000).
SECOND SOURCE: None.
CORE: The TLCS-90 family is based on a Toshiba proprietary core. The core will be used as a standard cell for building future devices.

Toshiba America Electronic Components
(714) 455-2000
FAX (714) 859-3963
For more information, Circle No. 353

Description: The TLCS-90 family consists of single-chip 8-bit μCs. Peripheral options include ADCs and DACs, PWM, stepper motor control, servo control, μDMA, memory management (to 8 Mbytes), zero cross detection, pattern generation, EPROM and OTP EPROM, masked ROM (to 32 kbytes), and internal RAM (to 1 kbyte). The architecture uses a pipelined instruction-fetch mechanism. 16-bit arithmetic operations allow the μC to perform high-precision calculations.

Status: Although the TLCS-90 family has been available in the Far East for several years, it has just recently been introduced in the US. The application base for the device includes such products as typewriters, coin changers, VCRs, and robotics. Toshiba is trying to expand the family's market position by expanding the range of on-chip peripherals, operating frequencies, packaging options, and customization.

HARDWARE CHARACTERISTICS SOFTWARE



Hardware note: The diagram reflects the TMP90C840AN, which shows some of the features available within this 8-bit device family. (Ports have a pull-up mask feature that the diagram doesn't demonstrate.)

I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logical operations. 16-bit arithmetic and data-movement loading capabilities. Bit-manipulation capabilities include set, reset, test, and test/set. Operations allowed on registers and memory (including ports and RAMs).

II—DATA-MOVEMENT INSTRUCTIONS
Pipelined architecture. μDMA: automatic interrupt-driven data transfer. 16-bit data movement. Memory-management unit expands addressable data locations to 8 Mbytes. Memory data exchange instructions. Block move and search instructions.

III—PROGRAM-MANIPULATION INSTR
Jump: direct, indirect, relative, and conditional. Call: conditional, relative, and direct. Branching: decrement and branch if not zero, absolute, conditional, and absolute return from subroutine.

IV—PROGRAM-STATUS-MANIP INSTR
Vectored interrupts; setting and clearing of condition codes; alternate register sets; halt and software interrupt instructions; increment and decrement of processor registers.

V—POWER-SAVING INSTRUCTIONS
Software selection allows for 4 operating modes: Run, Idle1, Idle2, and Stop.

Specification summary: 163 basic instruction types. Has built-in SIO (serial input/output), 8-bit and 16-bit timers, and separate watchdog timer. Uses as many as 14 interrupt sources. On-chip memory options include internal ROM (as much as 32 kbytes), RAM (as much as 1 kbytes), and external memory addressing (as much as 8 Mbytes with the memory-management unit). μDMA allows automatic data transfer upon receipt of an interrupt, reducing time requirements for interrupt servicing. Pipelining is transparent to the software; it is automatically available.

HARDWARE SUPPORT SOFTWARE

Toshiba provides an emulation system containing the controller, emulator, extension board, and experimental/evaluation board. The system uses a PC as a host. An emulation pod for the HP64000 system is available from Andover Systems.

To complement the emulation and hardware development tools, Toshiba offers an assembler, C compiler, and debugger.

8048 FAMILY

8-BIT NMOS AND CMOS

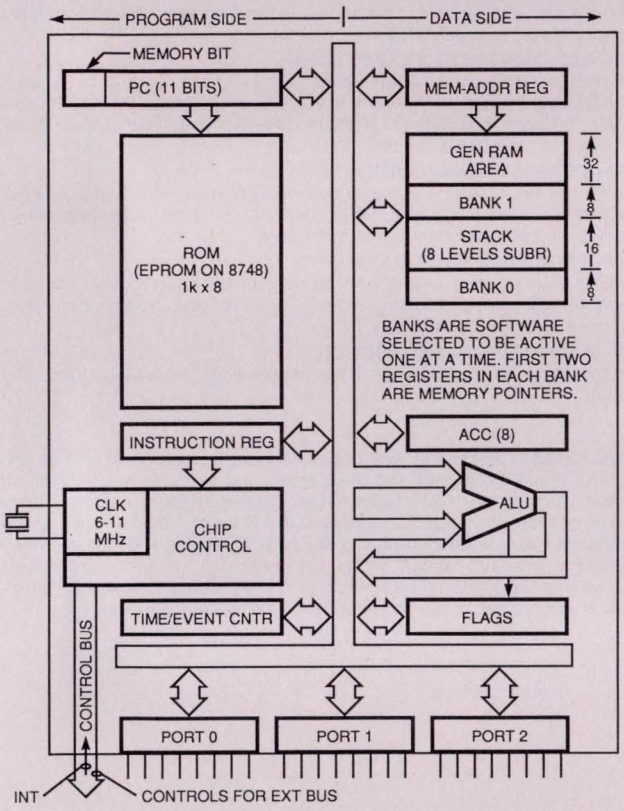
AVAILABILITY: Now.
COST: Masked-ROM parts are less than $1.20 in high volume (100,000). EPROM parts cost less than $6 (100). CMOS parts from second sources cost as little as $3 (100,000). Windowless-PROM parts cost $8 (5000).
SECOND SOURCE: Toshiba, NEC, Signetics/Philips, National Semiconductor, Oki, Fujitsu, UMC (Taiwan), with volume spread out among suppliers.
CORE: Zymos has been using 80C49 as a core for ASICs for several years. Others are following because 8048/49 combines popularity with small core size.

Description: Broad family of single-chip controller-type μCs, including a version that can function as a slave (8041). Basic models don't have serial communications ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

Intel Corp
Embedded Controller Operation
Phone (602) 961-8051
For more information, Circle No. 354

Status: Intel is still bullish about the 8048. However, Intel chose the 8051 over the 8048 as the kick-off core for ASICs and says it has no definite plans to use the 8048 as an ASIC core.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Bit set and reset.
Two working banks of 8-bit registers.

II—DATA-MOVEMENT INSTRUCTIONS
Both internal and external RAM are fully accessible by instruction set.
Indirect and direct data fetches.

III—PROGRAM-MANIPULATION INSTR
Decrement and skip if zero.
More than 20 conditional branches.
8-level stack with expansion capability.
Two vectored interrupts.
Two programmable flag bits under software control.

IV—PROGRAM-STATUS-MANIP INSTR
Status word is fully accessible and is stored in the stack.

Specification summary: Split-memory architecture with 1 to 4 kbytes of program ROM or EPROM on chip and 64 to 256 bytes in separate space, also on chip. I/O has its own space and instructions to operate directly on I/O ports. All spaces are expandable: program memory to 4 kbytes, data memory to 256 bytes, I/O to unlimited amounts. I/O can use 8080/85 peripherals. Devices have 8-level stack for subroutine nesting and interrupt response. Dual banks of working registers allow rapid context switching. Family members execute their 1- and 2-cycle instructions at 1-cycle times ranging from 1.36 to 15 μsec. NMOS 5V technology in 40-pin DIP and 44-pad chip carriers; UV-erasable ROMs (EPROMs) and windowless PROM parts are available. CMOS versions available with idle and power-down features and optional flatpack packages. The 8049KB can drive four 10-mA LEDs.

Part no.	Memory (bytes) ROM	EPROM	RAM	Package pins Parallel I/O	Total
8035	0	0	64	3×8	40
8048	1k	0	64	3×8	40
8748	0	1k	64	3×8	40
8039	0	0	128	3×8	40*
8049	2k	0	128	3×8	40*
8749	0	2k	128	3×8	40*
8040	0	0	128	3×8	40
8050	4k	0	256	3×8	40

*Also available in 44-lead PLCC package.

Hardware notes:
1. Diagram is for basic 8048. Table indicates some other basic parts, most of which exist in both NMOS and CMOS.
2. CMOS parts are designated 80C48, 80C49, 80C50, etc.
3. There are many other variations of the basic 8048 among the many suppliers. For example, Intel's 8041/42 chips are software compatible but are configurable as slaves to host μPs for interface applications. The National NS 405/455 uses the 8048 core as the basis of a terminal controller. Siemens has the telecommunications-oriented 80C382/482. A number of semicustom houses use the 8048 as a core processor in their libraries.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Intel plays down 8048 support, saying that there are now numerous third-party OEM suppliers of PC-hosted emulators for the 8048 family.
From NEC: Ekakit 84C-1 stand-alone emulator (less than $2000).

From others: Because of the broad-based popularity of this family, dozens of independent sources of development and application software exist, including support on universal development systems from Tektronix (Beaverton, OR) and Applied Microsystems (Redmond, WA).
Program library: Insite Library contains a variety of application programs.

8051/8052 FAMILY

8-BIT NMOS AND CMOS

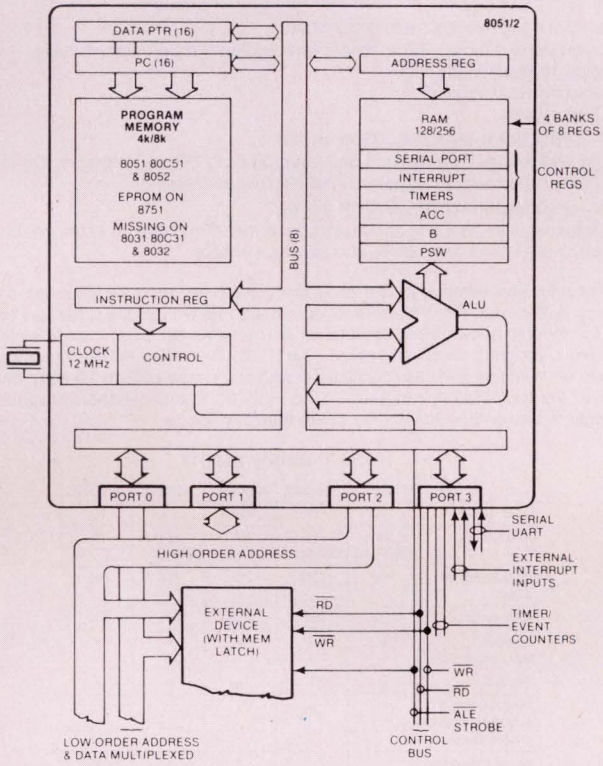
AVAILABILITY: A variety of devices is available from Intel and all of the second sources.
COST: In 10,000 qty, $1.60 for 8051; $14.50 for 8751; $2 for 80C51; $13.50 for 87C51; $16 for 8752; $3 for 80C52; $4 for 83C51FA; $20 for 87C51FA; $5.20 for 83C51FB; $24 for 87C51FB; $4.60 for 80C54; $22.50 for 87C54; $6.50 for 83C51FC; $30.35 for 87C51FC; $5.80 for 80C58; and $26.40 for 87C58.
SECOND SOURCE: Siemens, Signetics/Philips, Fujitsu, Oki, and Harris-Matra (France) licensed.
CORE: Intel's ASIC Components Group is using the 80C51 as its starting μP core. Signetics/Philips has the 80C51 core in its ASIC library. Similarly, Siemens is using the core to spawn a range of microcontrollers.

Description: Expandable single-chip controller, an enhanced version of the same supplier's widely used 8048 family. Architecturally, it features nonpaged addressing for easier programming; more interrupts with extra RAM-register banks to service them; increased stack depth; and new instructions, such as multiply, divide, and compare.

Intel Corp
Embedded Controller Operation
Phone (602) 961-8051
For more information, Circle No. 355

Status: Generally thought of as the leader among the more powerful 8-bit single-chip μCs. This family faces stiff competition from high-end 8-bit μCs, such as Mitsubishi's 50740 version of the 6500/1, Motorola's 68HC11, NEC's 7811, Hitachi's 647180, and National's COP800, as well as from 16-bit μCs, such as Intel's own 8096 and National's 16040. The 8051 is among the most widely used cores in market-specific μCs.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, multiply, and divide.
Bit manipulation, including complex tests on bits and branching on results.

II—DATA-MOVEMENT INSTRUCTIONS
Register addressing for the 8 working registers in the 4 register banks.
Direct, immediate, and indirect data addressing for more general data accessing.
Table look-up in ROM via data pointer.

III—PROGRAM-MANIPULATION INSTR
Depth of subroutining limited only by available space in 128- or 256-byte on-chip RAM.
Conditional jumps on status-register flags.
Conditional jumps on comparisons.
Vectored interrupts to service 2 external interrupts, timers, and a UART.

IV—PROGRAM-STATUS-MANIP INSTR
CPU's program-status word is fully accessible via software. Status bits in timer and UART are also software accessible.

Specification summary: Expandable single-chip μC. Split-memory architecture has 2 to 32 kbytes of ROM on chip and 128 bytes to 2 kbytes of RAM on chip. Each memory is expandable externally to 128 kbytes. Four to seven 8-bit ports on chip, but only one of these remains a port when you use all off-chip expansions and on-chip special functions. On-chip special functions include full-duplex hardware UART (to 500 kbaud), one to four 16-bit timer/counters, and as many as 17 interrupts with four priority levels to service these internal functions. Instructions are a superset of the 8048's, with paged addressing eliminated. At 12-MHz clock frequency, most instructions take 1 μsec; multiply or divide requires 4 μsec. 8051 is also available in CMOS (80C51) with 12- or 16-MHz performance and idle/power-down modes.

Notes:
1. The 14 members of the 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip ROM.
2. The 8051's Boolean-processor capabilities refer to the way instructions can single out bits in RAM, accumulators, I/O registers; perform complex bit tests and comparisons; then execute relative jumps based on results.
3. Intel has one 8052 model preprogrammed with a full Basic interpreter.
4. Dallas Semiconductor (Dallas, TX) offers an 8051-instruction-code-compatible μP ($9.70 (1000)), which converts as much as 64 kbytes of SRAM into lithium-backed nonvolatile memory. The chip also provides a serial bootstrap loader for initialization, crash-proofing circuitry to save current state, and on-chip software encryption that loads and executes the application in unintelligible form.

HARDWARE — SUPPORT — SOFTWARE

From Intel: ICE-51/PC in-circuit emulator ($5495) supports the entire MCS-51 family including 8051, 8052, 8XC51FX, and 80C52. Comes with macroassembler and editor. PCs, running DOS 3.1 or later versions, and Intellec Series III/IV development systems host the emulator. Nohau (Campbell, CA) and MetaLink (Chandler, AZ) provide PC-hosted emulation systems for Signetics/Philips standard and derivative μCs.

From Intel: ASM-51 and PL/M-51, both containing a relocation and linkage utility, are available for the IBM PC and Intel microcomputer development systems.
From others: Many third-party software suppliers offer C compilers for 8051 with special features suited to microcontroller applications. Three such compilers are Micro Computer Control's (Hopewell, NJ) for $1495, Archimedes Software's (San Francisco, CA) for $851, and Franklin Software Inc's (San Jose, CA) for $895. All are hosted on IBM PC.

TMS370 FAMILY

8-BIT CMOS

AVAILABILITY: Now.
COST: ROM-based devices range from less than $3 to less than $10 (100,000) depending on program memory, peripherals, and on-chip EEPROM mix.
SECOND SOURCE: None.

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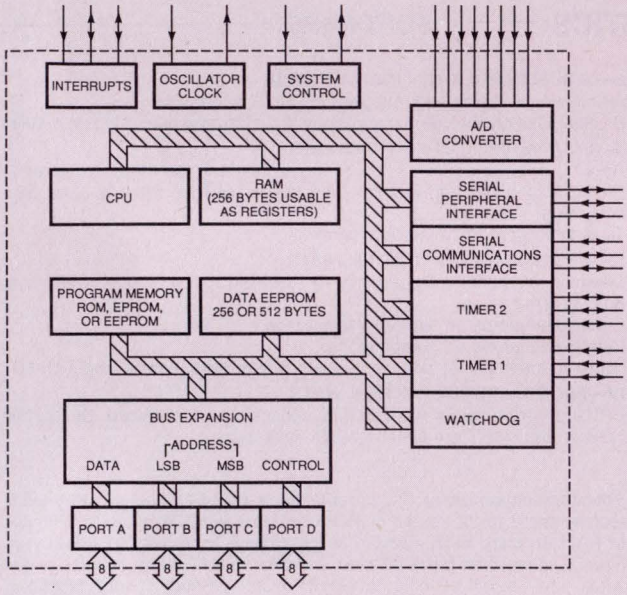
Description: Software-compatible family of CMOS μCs with on-chip EEPROM and peripheral support functions. Modular design architecture provides flexible reconfiguration and reduction in product design time. Various family members incorporate an 8-channel, 8-bit A/D converter, enhanced timers, serial peripheral interface, serial communications interface, EPROM, EEPROM, and ROM. Instructions typically perform combined load, operation, and store functions, increasing system performance and code efficiency. One-time programmables and form-factor emulator versions replace ROM with EPROM or EEPROM and allow prototyping and small production runs.

Status: Supports real-time applications that may previously have required analog, bit-slice, or multiple controllers. The alterable nonvolatile memory allows the μC to retain critical data without power. The vendor offers 16 function modules that it will configure for your application if your volumes exceed 200,000.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware note:
Diagram reflects the TMS370x5x, which supplements the 370Cx1x's single 16-bit timer, serial peripheral interface, programmable timer, 128-bit SRAM, and optional 256-bit EEPROM with a second 16-bit timer, a serial communications interface, memory-expansion ports, another 128 bits of SRAM, and an 8-channel, 8-bit ADC. The 370Cx3x contains a programmable timing module with watchdog timer, a miniserial communications interface, an 8-channel, 8-bit ADC, 256-bit SRAM, and optional EEPROM.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8×8-bit multiply, 16×8-bit divide, and BCD.
Logicals, increment, and decrement.
Rotates right and left. Bit test. Set bit.

II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Apply to many instructions.
Indexing via B register.
16-bit moves.

III—PROGRAM-MANIPULATION INSTR
Call and return. Trap. Bit test and jump on both I/O and memory. Conditional jumps using program-counter-relative addressing.

IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, overflow, and interrupt enable. Instructions to change carry and interrupt enable.

Specification summary: The programmable timer module uses the on-chip dual-ported RAM to store its commands as well as the timer values. This module allows input capture on as many as six pins, four of which have a programmable prescaler. The TMS370 CMOS family members use a 5V supply over the oscillator frequency range of 2 to 20 MHz and over the temperature range of -40 to +85°C. The application program, register file, and peripheral file share memory space.

TMS370 family matrix

	370Cx10	370Cx32	370Cx50	370Cx52	370Cx56
ROM (bytes)	4k	8k	4k	8k	16k
FFE (bytes)	4k EEPROM	8k EEPROM	16k EEPROM	16k EPROM	16k EPROM
Data EEPROM (bytes)	256	256	256	256	512
RAM (bytes)	128	256	256	256	512
Timer 1, watchdog timer	•		•	•	•
Timer 2			•	•	•
Programmable acquisition and control timer		•			
Serial peripheral interface			•	•	•
Serial communications interface		•	•	•	•
A/D port		•	•	•	•
I/O links	22	36	55	55	55
Package	28 DIP/PLCC	44 PLCC	68 PLCC	68 PLCC	68 PLCC

Note: PLCC=plastic leaded chip carrier

HARDWARE — SUPPORT — SOFTWARE

From TI: XDS/11 is a PC-driven interactive development system ($2850). It provides full-speed, in-circuit emulation and debugging functions. XDS/22 development system ($8250) adds extended breakpoint, trace, and timing functions to the XDS/11 system. A design kit ($370) lets you analyze the feasibility of using the TMS370 family for your application. EEPROM programmer ($1250) comes with power and interface cables, software, and sockets for the 370 family and EPROMs such as the 2732, 2764, 27128, and 27256. A Gang Programmer head attachment ($2550) allows you to program as many as 16 devices concurrently.
From others: Electrorent provides rental use of TI tools for PCs. Logical Devices (Fort Lauderdale, FL) has a TMS370 microcontroller module for Allpro programmers.
Evaluation Boards: The TMDS3770110 is available from TI.

From TI: Cross-assembler, linker, full ANSI C compiler, and C source debugger available on IBM PCs under DOS or OS/2, Sun-3, Sun-4, and DEC VAXs under VMS.
From others: Allen Ashley (Pasadena, CA) supplies an assembler/linker and Intermetrics (Cambridge, MA) offers a C compiler that runs on IBM PCs. Macrochip Research (Carrollton, TX) has an assembler and midrange emulator for both IBM and Macintosh personal computers. P&E Microcomputer Systems (Woburn, MA) provides an integrated assembler and simulator for IBM PCs.

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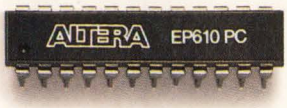

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CIRCLE NO. 67

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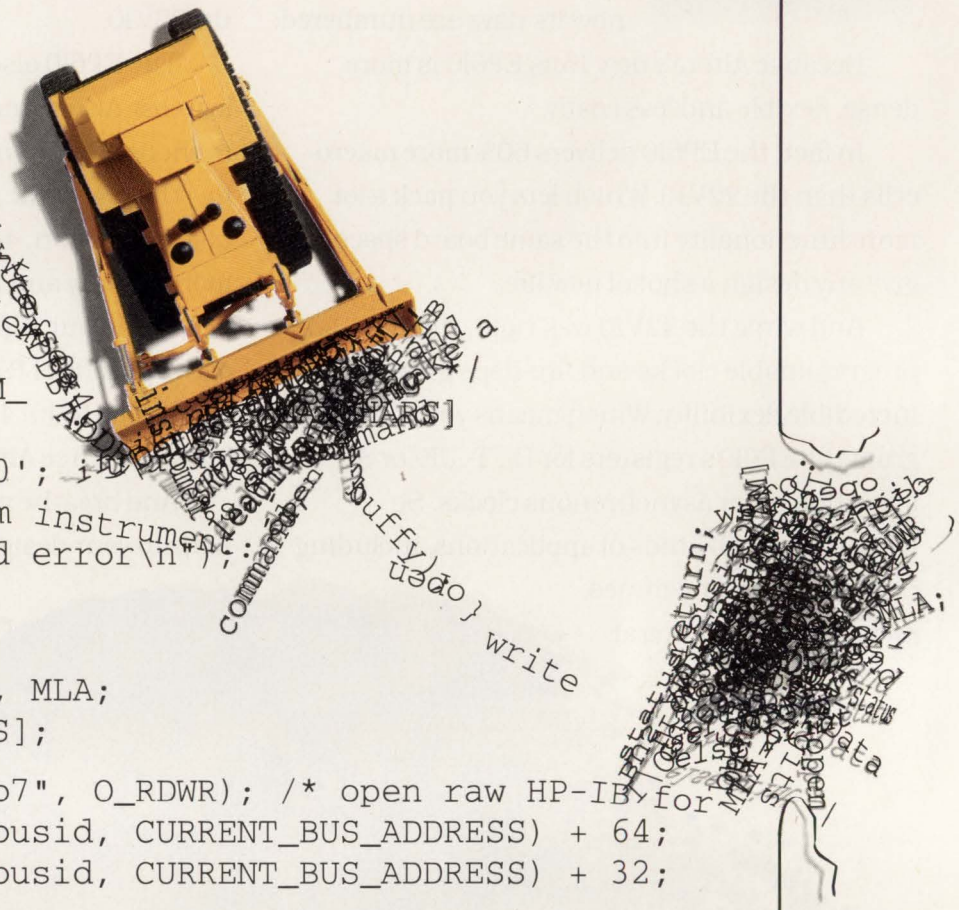
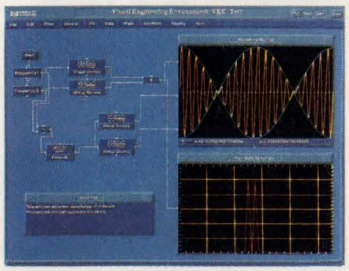


```
void service(eid)
int eid;
{ int stat, byte;
/*serial poll
byte=hpib_spoll(
if ( (byte<0)||! (b
    printf("SRQ Prob
   return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0';
    printf("Data from instrument:
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
```



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6805/68HC05 — 8-BIT NMOS AND CMOS

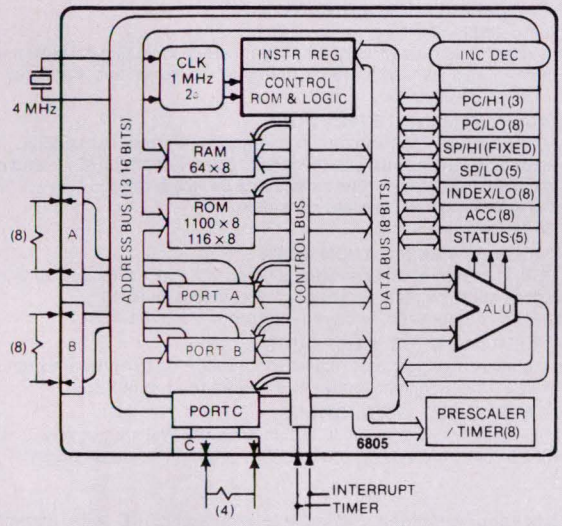
AVAILABILITY: Motorola can build customer-specified versions in less than six months.
COST: $1 to $8. CMOS parts are more expensive than NMOS ones.
SECOND SOURCE: Harris, Hitachi, and SGS Thomson.
CORE: Motorola and NCR have a joint ASIC pact to use CMOS 6805 as a core along with NCR's similar 6502 μP core. SGS Thomson calls its core the ST6.

Description: Family of single-chip μCs based loosely on 6800 architecture. Family offers various amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 4 MHz. Some parts contain an on-chip A/D converter, EEPROM, serial I/O, and software security. Customer-specified microcontrollers use this core for mixing and matching of peripherals to reduce cost for specific customer applications.

Motorola Microprocessor Products Group
Phone (512) 891-2000
For more information, Circle No. 357

Status: Motorola continues to expand the 6805 family, using its CSIC (customer-specified integrated circuit) concept.

HARDWARE CHARACTERISTICS SOFTWARE



Hardware notes:
1. Diagram is for nonexpandable Model P2 in a 28-pin package.
2. Comparison of 6805 with 6800: Stack is only 64 bytes deep. Only one accumulator. Index register can only span 256 memory locations. However, family supports a 16-bit offset addressing mode, thus the μP can access 256-byte tables anywhere within the memory space. Program counter is as long as 14 bits in some members of this family. Only one external interrupt is provided, but some models have timer-input capture pins, which may provide additional edge-triggered inputs.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Special pin initiates program.
4. Harris has ROMless emulator versions (68EM05/C4,D2) for prototyping and low-volume production. Harris brings all ROM access buses out for direct interfacing to industry-standard EPROMs. Available in 40-pin piggyback for 2764.
5. Motorola currently has five field-programmable 68HC05 versions with on-chip EPROM instead of masked ROM to permit development and low-volume production.

I—DATA-MANIPULATION INSTRUCTIONS
All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test. Bit tests can be made on all I/O and direct-page memory bits. 68HC05 has 8 × 8-bit multiply.

II—DATA-MOVEMENT INSTRUCTIONS
Relative addressing allows data relocation.
True indexing within the 256-location limits of 8-bit index.

III—PROGRAM-MANIPULATION INSTR
18 conditional branches, including branch of interrupt line test.
Mostly the same conditional branches as the 6800, but with more emphasis on branch-upon-bit and interrupt tests.
Only 15 levels of subroutine nesting, including interrupt returns; 31 levels on certain new parts.
Four sources of interrupts: external, timer, software, and reset. 68HC05 has vectored interrupts to service its serial-communications and peripheral interfaces.

IV—PROGRAM-STATUS-MANIP INSTR
Instructions for manipulating bits in status register and timer.

V—POWER-SAVING INSTRUCTIONS
CMOS 6805s have Stop and Wait instructions and will safely reset themselves when the clock is reapplied.

Specification summary: Common-memory architecture in which instructions, data, I/O, and timers all share the same memory space. This scheme allows bit manipulation and rotation of I/O. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most 6805 versions. New 68HC05s have a 2.1-MHz internal bus speed. Some, like the 68HC705C8, are available with a 4-MHz bus speed. Some parts offer program security, on-chip 5V EEPROM, A/D converter, serial peripheral interface, serial communications interface, timers, PWM D/A converter, LCD drivers, DTMF generators, and other customer-specified peripherals. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs, SOICs, and shrink DIPs; 44-, 52-, and 68-pin PLCCs; and other fine-pitch packaging options.

Family		Bus speed (MHz)	Instructions	On-chip ROM	RAM	I/O pins	Timer	Interrupts	Power consumption (mW)	Pins
6805	Min	.1	51	1k	64	16	—	3	0.01	28
	Max	2	59	4k	176	32	Yes	5	700	40
68HC05	Min	0	62	1k	96	32	Yes	2	0.25	40
	Max	4	62	16k	304	32	Yes	2	0.25	68

HARDWARE SUPPORT SOFTWARE

From Motorola: The less costly M68705EVM (HMOS) and M68HC05EVM (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.
From Harris: Single-board evaluation kit that interfaces to IBM PC via RS-232C line.
From SGS Thomson: INICE4-8 development and emulation system.
From others: A number of third-party companies, including Sophia Systems (Santa Clara, CA) and American Automation (Tustin, CA), provide hardware emulators for the 6805 family. Most of these emulators interface to IBM PCs.

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733.
From SGS Thomson: Interactive development software.
From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has cross-assemblers for 6805 that run on IBM PCs and compatibles. Introl (Milwaukee, WI) provides cross-compilers and cross-assemblers. C cross-compiler with macro cross-assembler from Bytecraft Ltd (Waterloo, ON, Canada).

6801/6301/68HC11

8-BIT NMOS AND CMOS

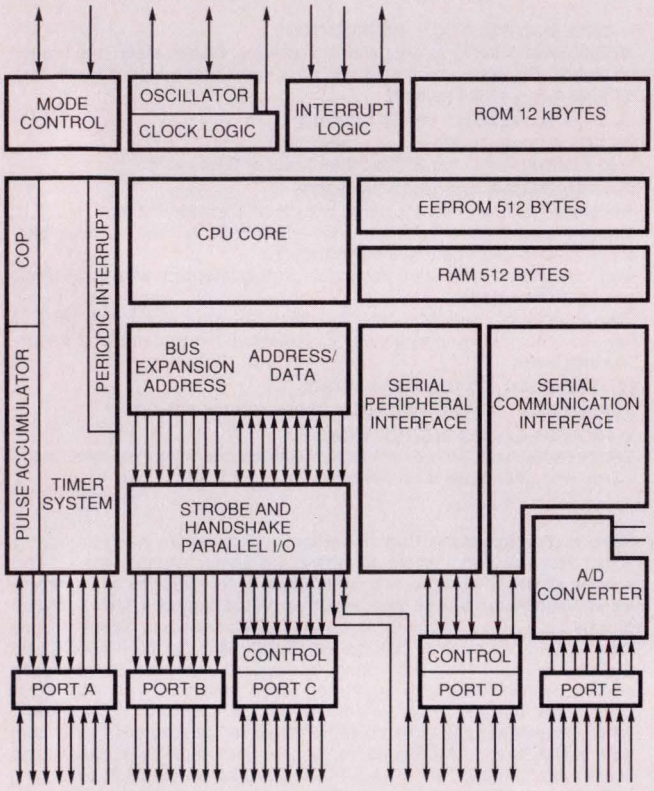
AVAILABILITY: Now.
COST: From less than $3 to $20 (1000).
SECOND SOURCE: Hitachi, SGS Thomson, and Toshiba. Hitachi second-sources the 6801 and calls the part 6301. SGS Thomson sources the 6801. Toshiba is a second source for 68HC11 devices.

Description: 6801 is a large, expandable, single-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8×8-bit multiplication, and a multifunction 16-bit timer. 68HC11 has a second 16-bit-wide register; an 8-function timer; a 2-function pulse accumulator; an enhanced UART (SCI); a 1-MHz serial shifter; an 8-channel, 8-bit A/D converter; and a 512-byte EEPROM. One-time-programmable/mask versions include as much as 24-kbit on-chip EPROM/ROM and built-in device selects and bank switching circuits for as much as 20-bit addressing.

Motorola Microprocessor Products Group
Phone (512) 891-2000
For more information, Circle No. 358

Status: This family has been well received. Motorola is now following migration of customers to more powerful single-chip devices and is concentrating on the 68HC11 enhancement of the 6801, such as increased on-chip EEPROM. The company is also adding various peripheral functions in many of the family derivatives.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of 2 accumulators, including 8×8-bit multiply. 68HC11 has additional 16-bit operations, integer and fractional divides, and bit manipulation.

II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
Can list-process efficiently with the index register (2 on 68HC11) and can add accumulator to index register within a 64-kbyte range.
Relative addressing allows data relocation.
Has 16-bit load and store.

III—PROGRAM-MANIPULATION INSTR
Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM.
Eight levels of prioritized, vectored interrupts (21 on 68HC11).

IV—PROGRAM-STATUS-MANIP INSTR
Instructions for storing status register or transferring to or from accumulator. 68HC11 has additional active bits related to stop mode.

V—POWER-SAVING INSTRUCTIONS
6301 has sleep instruction. 68HC11 has Stop and Wait instructions similar to 146805 but with disabling provision via a bit in the status register.

Specification summary: Expandable single-chip μC with common-memory architecture in which all instructions, data, I/O, control, and data registers share the same memory space. This scheme allows I/O to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and 88 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in the table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 4 MHz for 68HC11. The 6801 is fabricated in NMOS, the 6301 is fabricated in CMOS, and the Motorola 68HC11 is fabricated in static CMOS to allow dormant, micropower "asleep" state. 6801 in 40-pin DIP, 6301 in 64-pin DIP and flatpack, and 68HC11 in 48-pin DIP and 52-, 68-, and 84-pin PLCCs.

Hardware notes:
1. Diagram is for 68HC11E9. The A-, D-, E-, and L-series devices multiplex the data and address buses. The F-, G-, J-, and K-series devices offer separate address and data buses. Most ROM-based 68HC11 devices are also available in UV EPROM and one-time-programmable versions.
2. Motorola provides one-time-programmable versions of some HC11 family members that have EPROM program memories in inexpensive windowless packages for one-time programming in moderate-volume production (to 10,000).
3. Motorola's 68HC11 is a much enhanced 6801 that runs at 3 and 4 MHz. 68HC11A8 has a 512-byte EEPROM; 68HC811E2 has a 2-kbyte EEPROM; 68HC711E9 has a 12-kbit EPROM; 68HC711K4 has a 24-kbit EPROM.

Software notes:
1. 6801 has all 6800 μP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set with 88 additional op codes.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: For 6801 family, M68701EVM is an evaluation module that has a port for terminal and a port for any RS-232C host and will program 68701 EPROM parts. For 68HC11, the similar M68HC11EVM. Also M68HC11EVB boards ($168.11) for evaluating single-chip configuration of HC11s. For both 6801 and 68HC11, the less-than $3000 PC-based CDS8 Jewelbox series of development systems features real-time, noninvasive in-circuit emulation with real-time tracing and other debugging capabilities.
From SGS Thomson: INICE4-8 development and emulation system.
From others: Third-party hardware development systems, such as CT68HC11 ($5000 to $6000) from Ashling Microsystems Ltd (Limerick, Ireland).

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733. C compiler runs on Unix System V for 68HC11. For the least expensive approach, use 6801 parts with Lilbug monitor in on-chip ROM (MC6801L1).
From SGS Thomson: Interactive development software.
From others: Cross macroassemblers and linking loaders, some relocatable, run on popular minis and personal computers. For example, C compiler from Archimedes (San Francisco, CA) runs on the IBM PC ($995) and DEC VAX ($3995 to $5995).

Text continued on pg 103

Oh no. Please, not now. Not with manufacturing release next week.

THE PROTOTYPE DOESN'T WORK.

Six ASICs, fifteen PLDs and the whole thing's gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

THE PROTOTYPE DOESN'T WORK.

Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

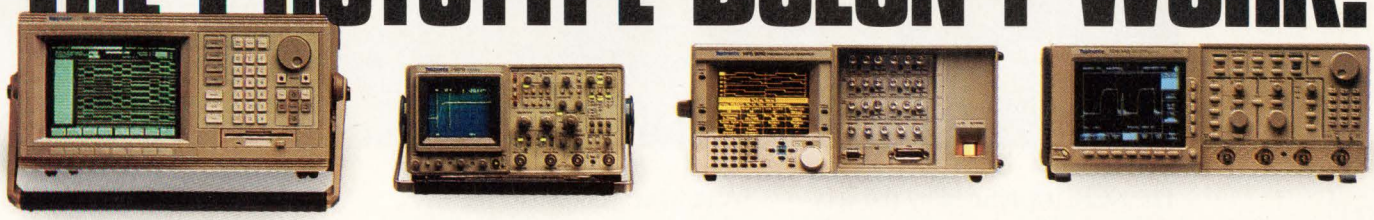
THE PROTOTYPE DOESN'T WORK.

And my performance review comes up next month. Maybe they'll just forget about all this, right? Yeah. Sure.

THE PROTOTYPE DOESN'T WORK.

Wait. What about that glitch in the handshake on the first pass? Couldn't reproduce it. Maybe it just reproduced itself.

THE PROTOTYPE DOESN'T WORK.



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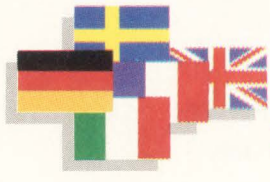

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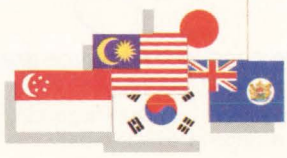

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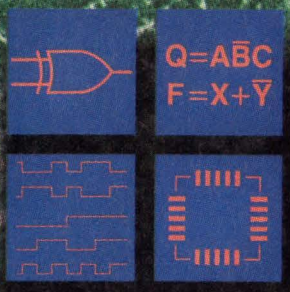

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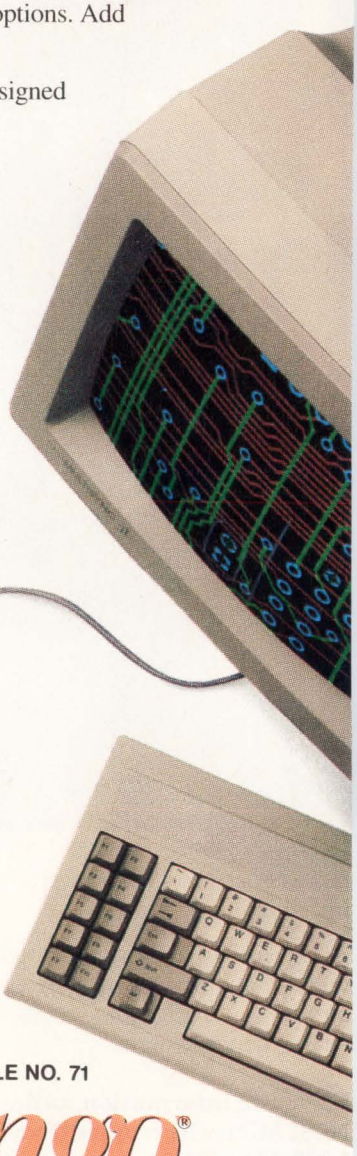

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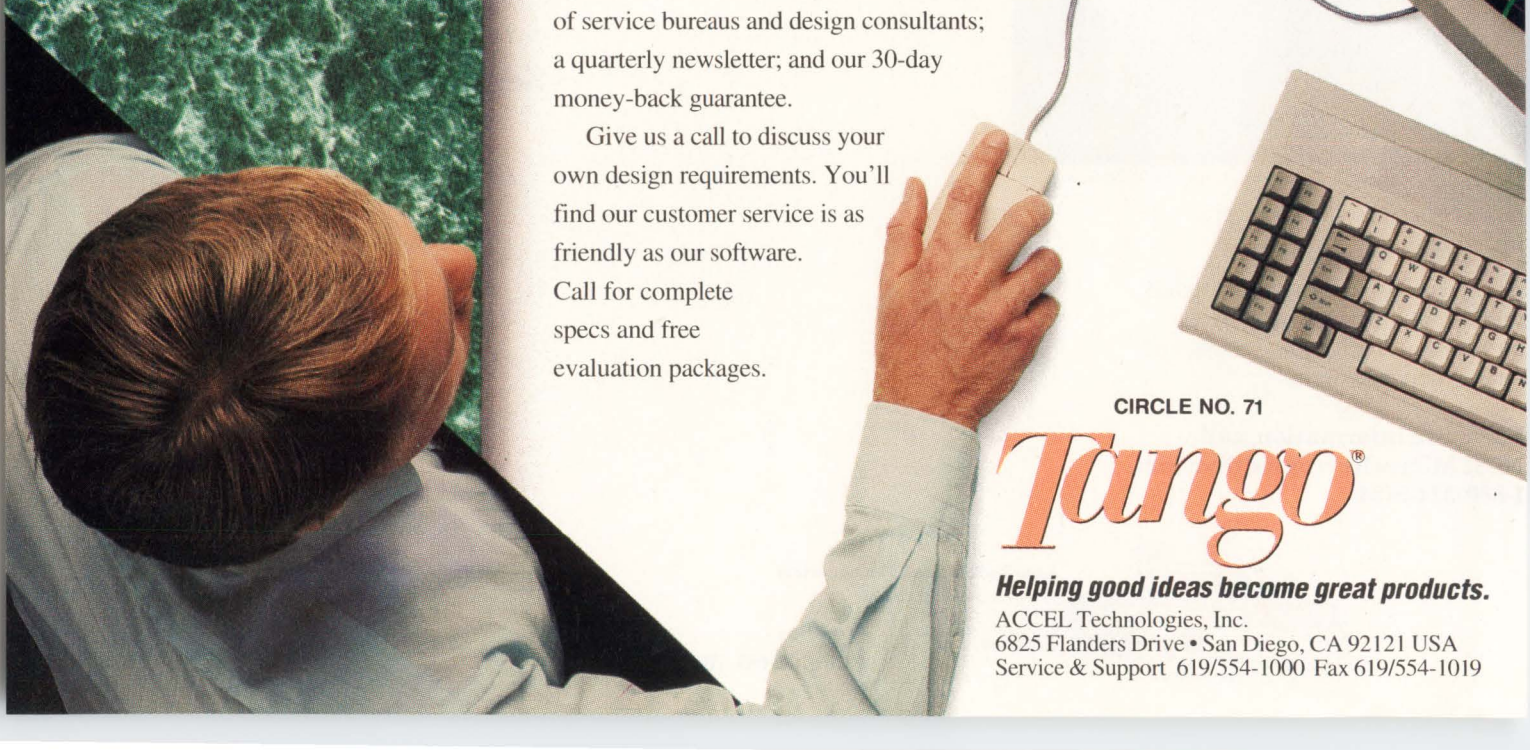

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6500/1, 65C134, 65C265, 38000, 37700

8-BIT (AND 16-BIT) NMOS AND CMOS

AVAILABILITY: Now for all NMOS and most 8-bit CMOS parts.
COST: WDC's 65C134 costs $28 (1000), and the 65C265 costs $50 (1000). Mitsubishi's prices range from $4 to $60.
SECOND SOURCE: NCR (licensed) and California Micro Devices for Rockwell NMOS parts. Western Design Center (WDC) has licensed a number of suppliers worldwide for its CMOS designs.
CORE: Standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, and several others. Widely used because of compact 6502 die size.

Description: There are three different sources for single-chip versions of the 6502 μP: the original 6500/1 NMOS family from Rockwell, the new 65C134 and -265 CMOS family from WDC, and the 50740 CMOS family from Mitsubishi. Most parts are 100% software compatible with 6502, although in some cases enhanced instructions such as bit manipulation have been added. Because of the small size of the 6502 core, many parts take a standard-cell ASIC approach. Vendors claim these 1-chip sets have a speed advantage over competing single-chip devices due to the 6502's 2-cycle bus and pipelining.

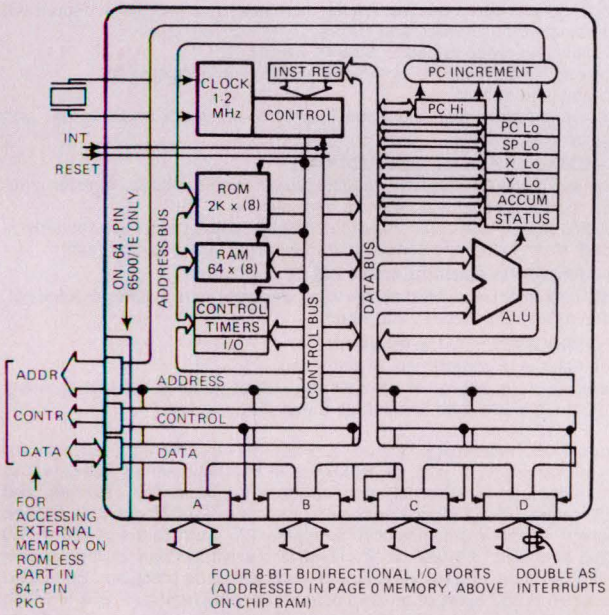
Rockwell International
Digital Communications Div
Phone (800) 854-8099; in CA (800) 422-4230
For more information, Circle No. 359

Mitsubishi Electronics America Inc
Phone (408) 730-5900
For more information, Circle No. 360

Western Design Center Inc
Phone (602) 962-4545
For more information, Circle No. 361

Status: Mitsubishi has replaced their M50740 series with the M38000 family of 8-bit μPs. These processors are software compatible with the 50740s and offer low power dissipation.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports.
Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset.

II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset is limited to 8 bits in 2 CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables.

III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses.
Nonmaskable and/or maskable interrupt, depending on model.

IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits.

Specification summary: Single-chip nonexpandable and expandable versions of 650X family. Have 2- to 16-kbyte ROM, 64- to 512-byte RAM, as many as 52 I/O lines, and one or more 16-bit programmable interval timers, as well as two or more programmable interrupts (plus the 650X's NMI interrupt). Family options (Rockwell) include RS-232C port and bus expansion. Operates from 5V, 500 mW and has separate 5V supply to keep 64 static bytes of RAM alive (50 mW required). Variety of package types and sizes from various suppliers. Full MIL-spec temperature-range devices from WDC.

Hardware notes:
1. Diagram favors initial Rockwell 6500/1 version. Most other versions are more complex.
2. Mitsubishi 740 Series parts are all CMOS and have as many as 16 kbytes of ROM and 512 bytes of RAM. Some models have special functions such as UARTs, 8-bit A/D converters, LCD drivers, or high-voltage (−35V) outputs. Some have 56 pins of I/O.
3. Mitsubishi's new CMOS M37700 version has an 8-bit external/16-bit internal data bus, much like the 68C816 version of the 6502 μP. On chip, it can have as many as 32 kbytes of ROM, 2 kbytes of RAM, eight 16-bit timers, 2 UARTs, 1 watchdog timer, and an 8-channel 8-bit ADC. Memory is expandable to 16 Mbytes off chip. New members of this family will offer DMA and DRAM controllers and real-time I/O ports.
4. The W65C265 has a 65C816 (static) core, UART, four 16-bit timers, 4k×8-bit ROM, 192×8-bit RAM, 56 I/O pins, and low-power features.

Software notes:
1. 6500/1 instruction set is identical to that of previous 650X family devices such as 6502, with the exception of bit-manipulation instructions for some devices. No new instructions added to handle new on-chip features such as timers and I/O because the μP handles them as if in external memory space.
2. Mitsubishi chips have some added instructions.
3. WDC's 65C134 adds some instructions and an operating voltage range of 1.8 to 5.25V.

HARDWARE SUPPORT SOFTWARE

From Rockwell: Emulator system available from Orion Instruments (Menlo Park, CA). Backpack part will be ROMless EPROMs.
From Mitsubishi: Debugging machine PC4000E ($1000) with in-circuit-emulator (ICE) cards for each device model ($750 to $1500). The PC4600 ICE costs $5000. Special evaluation chips offer ROM emulation.
From WDC: Toolbox Design System ICE for all WDC processors with an IBM PC host ($4995).

From Rockwell: Cross software available from 2500 AD Software (Buena Vista, CO).
From Mitsubishi: Cross software for MS-DOS. (Has plans for a C compiler and Forth interpreter.)
From WDC: Many software packages available from third parties for the W65C02/W65C816 μPs.

Z8, SUPER8

8-BIT NMOS AND CMOS

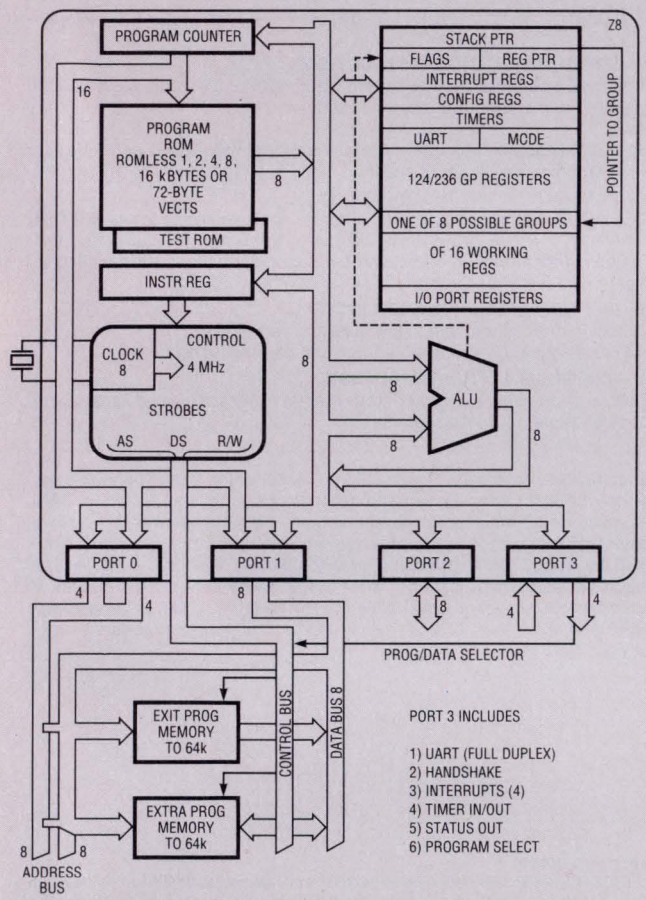
AVAILABILITY: Now for ROMless and 1-, 2-, 4-, 8-, and 16-kbyte parts; 2-, 4-, and 8-kbyte EPROM; and one-time programmables at 8, 12, 16, and 20 MHz. SGS Thomson has a 4-kbyte EPROM and an 8-kbyte ROM.
COST: Less than $3.50 for NMOS Z8 in volume. $4.95 for NMOS Super8 in volume. (28-pin version for $1.) Less than $5 for CMOS Z8.
SECOND SOURCE: SGS Thomson (licensed); Sharp for both NMOS and CMOS; VLSI Technology for CMOS.
CORE: From Zilog and VLSI Technology. SGS Thomson aims to convert NMOS Z8 designs to its CMOS ST9 core.

Description: Z8 is a single-chip μC that is a composite of many machines. You can't necessarily use its powerful features simultaneously, a common problem with single-chip units. Not really compatible with supplier's Z80 or Z8000 because architecture is so different; closest to Z8000. However, slave Z8 versions interface to Z80 and Z8000 buses. Super8 version has more of everything: more data and program memory, more on-chip peripherals, more instructions.

Zilog Inc
Phone (408) 370-8000
For more information, Circle No. 362

Status: According to Zilog, Z8 volume is growing rapidly. Meanwhile, second-source SGS Thomson has turned its CMOS efforts to its ST9 μP (featured elsewhere in the directory), a proprietary enhancement of the Z8 that SGS Thomson uses for an ASIC building block.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram applies to basic NMOS/CMOS version. Many other versions exist.
2. The 124/236 working registers (272 on Super8) are truly general purpose. Any one can be used as an accumulator or indexer.
3. The register pointer singles out a "workspace" of 16 working registers for fast access. Eight such workspaces are possible in the 124/236-register space (16 in Super8) and provide a mechanism for fast context switching upon interrupt.
4. SGS has not announced any CMOS Z8s. Instead it has introduced an ST9 ASIC core in 1.5-μm CMOS. According to SGS, this core reaches 12 MHz (24-MHz external clock). (Find a description of this ASIC core elsewhere in the directory.)

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, and subtract with borrow.
Multiply and divide added to Super8 version.
Logicals: AND, compare, complement, OR, and exclusive OR.
Rotates and swaps.
Bit manipulation: test under mask, test complement under mask, and logical tests of bits.

II—DATA-MOVEMENT INSTRUCTIONS
Address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative.
Block transfer: load constant autoincrement, load external autoincrement.
Load: clear, load, load constant, load external, and pop and push.

III—PROGRAM-MANIPULATION INSTR
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, jump relative conditional, and return.

IV—PROGRAM-STATUS-MANIP INSTR
Set, reset, and complement of carry flag.
Note: Ability to set, reset, and test any bit or combinations of as many as 8 bits lets any byte function as a user flag register.

Specification summary: Unique architecture with 3 memory spaces: program memory (0, 2, 4, 8, or 16 kbytes in internal masked ROM; rest to 64 kbytes can be external), data memory (to 64 kbytes external), and CPU register file (256-byte space that includes 124/236 general-purpose working register/accumulators). Executes 129 instructions at 0.6 to 3.0 μsec at 8-MHz internal clock (16-MHz oscillator). Has built-in duplex UART (96 kbps) and two 8-bit timers, each with 6-bit prescaler. Enhanced Super8 has 352 bytes of on-chip data and control registers, 256 of which are general purpose. New multiply and divide instructions on Super8. Its on-chip peripheral functions include DMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has 600-nsec interrupt response with 37 interrupt sources.

Software note:
The data- and program-manipulation instructions use the working registers in the CPU. The instructions that apply to the external data RAM are essentially just loads and stores. (There is a similarity to RISC philosophy.)

HARDWARE — SUPPORT — SOFTWARE

Development packages are available from JK Engineering (Singapore, 65-744-8414). In the US, IAM (Sacramento, CA) distributes JK Engineering's products. Development packages in various configurations are also available from Zilog Inc (Campbell, CA) and Inner Access (Belmont, CA). Emulation packages are available from Orion Instruments (Redwood City, CA), Microtek (Beaverton, OR), Creative Technology (Atlanta, GA), and Sophia Systems (Santa Clara, CA). This list isn't exhaustive.

Software development tools are available from Allen Ashley (Pasadena, CA), Avocet (Rockport, ME), Relational Memory Systems (San Jose, CA), and Western Wares (Norwood, CO). You can purchase compiler software from Micro Computer Compilers (Hopewell, NJ), 2500 AD (Buena Vista, CA), and Inner Access (Belmont, CA). This list isn't exhaustive.

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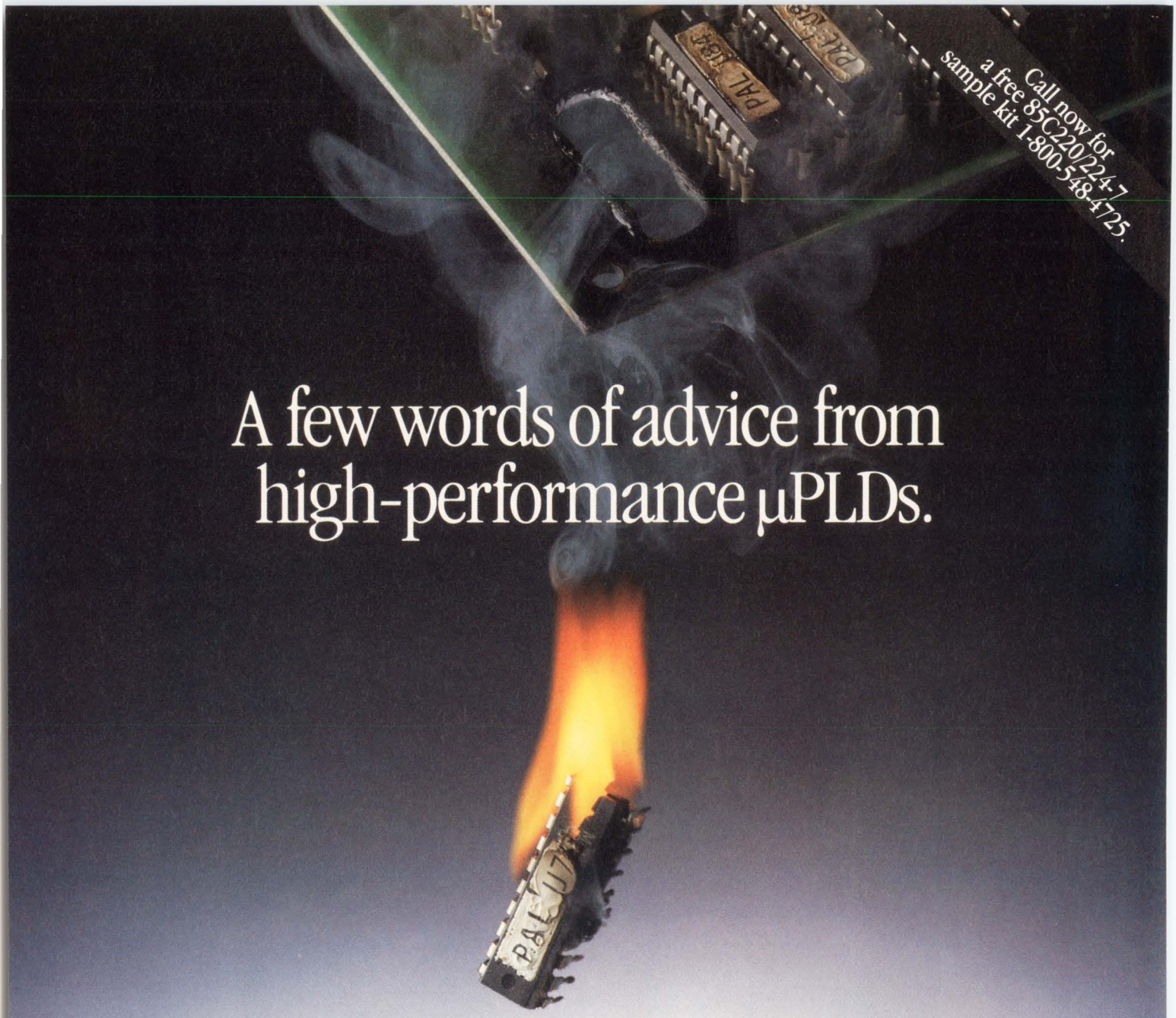

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CIRCLE NO. 73

Z80

8-BIT NMOS AND CMOS

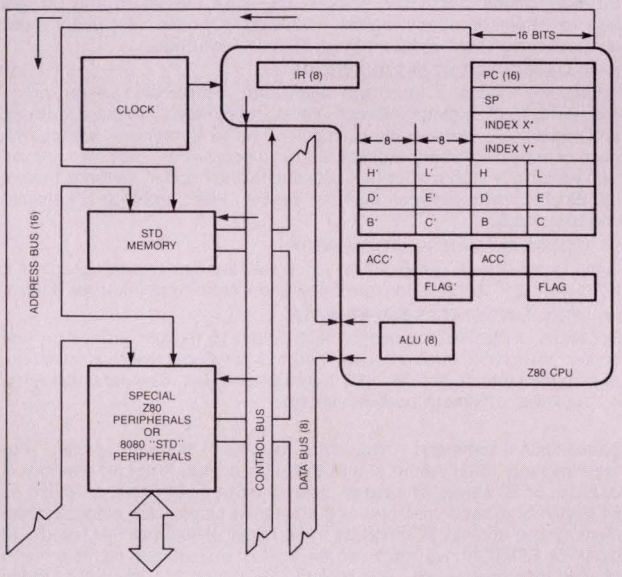
AVAILABILITY: Now for 6-, 8-, 10-, and 20-MHz CMOS and 4-, 6-, and 8-MHz NMOS.
COST: Because of the many aggressive second sources for this most widely used part, NMOS prices have dropped to between $0.80 and $1.10; CMOS prices have dropped to between $1 and $1.20 in high volume. The 10-MHz CMOS part costs $2.50 (100).
SECOND SOURCE: Goldstar, NEC, SGS Thomson, Sharp, and Toshiba. Goldstar, SGS Thomson, Sharp, and Toshiba, as well as Zilog, have CMOS versions. Additional sources mentioned by Zilog are VLSI Technology and Rohm.
CORE: Zilog and Hitachi use the Z80 μP as an ASIC core in their enhanced versions of this core, the 64180 and Z280. Zilog, Hitachi, and Toshiba all offer a range of specialized processors built around the Z80 core.

Description: Superset of widely used 8080/85; adds hardware and software features. Not pin-for-pin compatible with 8080 or 8085 but can use 8080 software and peripherals—although to do so would not take full advantage of Z80 and its peripherals, and it might require additional logic for interfacing. The Z80 and its peripherals are now available in quad flatpacks and all peripherals have been upgraded to run at 10 MHz. The 20-MHz version is only available from Zilog.

Zilog Inc
Intelligent Peripheral Controllers Product Line
Phone (408) 370-8000
For more information, Circle No. 363

Status: By far the most successful 8-bit μP. The Z80 is still being used in new designs but may be superseded by the new enhanced versions. Of these, the Zilog Z180/Hitachi 64180 seems to be the most popular, but the Zilog Z280 represents the greatest Z80 enhancement. The Z80's momentum will probably last for the rest of this century, especially in ASIC-core form, which allows the company to execute its superintegration strategy of building highly specialized microcontrollers around the Z80 core.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logic.
16-bit arithmetic BCD add and subtract.
Nine types of rotate and shift directly on any register or memory location.
Can set, reset, or test bit in any register or memory location.

II—DATA-MOVEMENT INSTRUCTIONS
8- or 16-bit register or memory loads.
Two index registers allow indexed addressing.
Extensive memory-block move/search commands.

III—PROGRAM-MANIPULATION INSTR
Uses 16-bit stack pointer with LIFO stack with RAM.
Relative-jump capability. Interrupt capability with three types of selectable response.

IV—PROGRAM-STATUS-MANIP INSTR
Seven flag bits, including arithmetic and overflow, can be stored and tested.

Specification summary: Upwardly compatible with 8080A software, but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 0.5 to 1.8 μsec (1.5 μsec avg) for 8-MHz Z80 and 1.0 to 5.5 μsec (2 μsec avg) for 4-MHz Z80. 6-, 8-, 10-, and 20-MHz versions are also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires a single-phase clock and one 5V supply at 60 mA for a 2-MHz Z80 and 90 mA for a 4-MHz Z80. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. MIL-temperature parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 μA in power-down (clock-stopped) mode. NMOS and CMOS versions available in DIP, quad flatpack, and PLCC.

Hardware notes:
1. Support chips include peripheral interface, timer, serial communications, and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. All Z80 enhancements are in CMOS. The first is the Zilog Z180/Hitachi 64180, to which many Z80 designers are converting. The second is the supplier's Z280, which boosts the Z80 into minicomputer performance. In addition, the NEC 78XX single-chip device is similar. Most are covered elsewhere in this directory.

HARDWARE — SUPPORT — SOFTWARE

Some of the many third parties that supply Z80 hardware support are Applied Micro, Boston Systems, Emulogic, Hewlett-Packard, Huntsville Microsystems, Nicolet, Orion, Sophia Systems, Tektronix, Zax, and Z-World. Contact nearest Zilog sales office for more information.

A variety of software supports the Z80 including assemblers and cross-assemblers, software simulators, high-level-language compilers, the venerable CP/M operating system (Digital Research), and the MS/X operating system, which is popular in Japan. Other third-party suppliers include 2500 AD, Archimedes, Avocet Systems, Enertec, Huntsville Micro, Softaid, Software Development Systems, Microtec Research, and Z-World.

ST9

8/16 CMOS

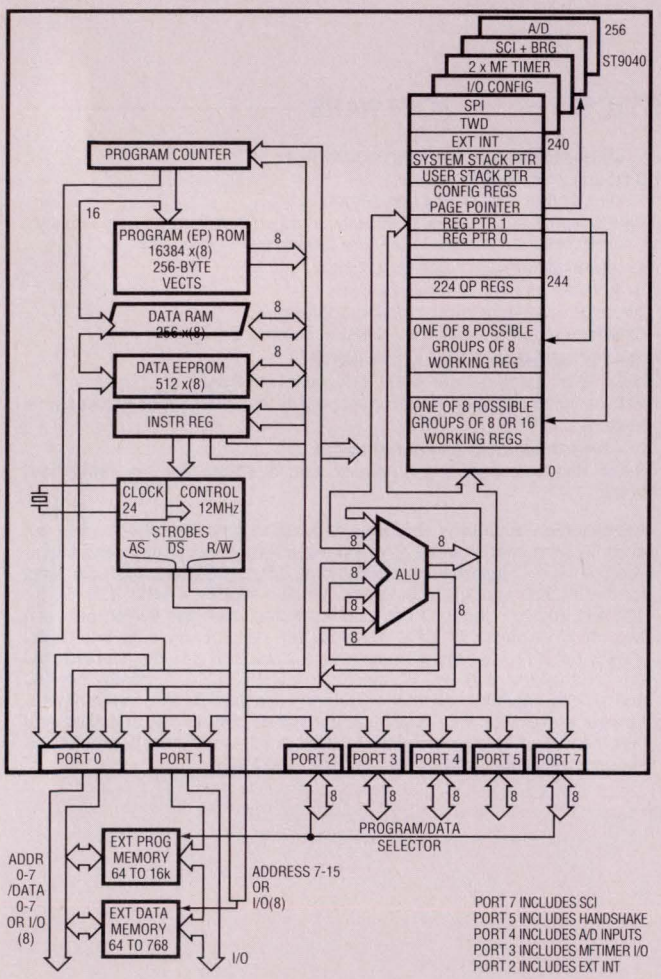
AVAILABILITY: Now for ROMless, ROM, EPROM, and one-time programmable parts to 24 MHz (external).
COST: From $3.70 to $11 in volume (with ROM).
SECOND SOURCE: Siemens (announced).
CORE: SGS Thomson is building the family around its proprietary core.

SGS-Thomson Microelectronics
Phone (602) 867-6100
For more information, Circle No. 364

Description: The ST9 microcontroller family is built around the combination of the ST9 register-file-based CPU, of memory options including ROM, RAM, EPROM, and EEPROM, and intelligent peripheral modules. Among these peripherals functions include vectored interrupts and DMA. The register-file architecture lets you split memory into Data and Program sections and offers flexible operation in embedded control applications.

Status: The emphasis for this family has been to grow based on focused development. Currently, the family contains six members in ROMless, EPROM, and one-time programmable configurations.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, subtract, subtract with borrow on both 8- and 16-bit data. Decimal adjust, Increment, and Decrement of byte and word. 8×8 multiply, 16÷8 divide, and stepped 32÷16 divide.
Logicals: 8- and 16-bit AND, OR, XOR, and Compare, Compliment, and Rotate and Shift byte and word.
Bit manipulation: Set, reset, compliment, AND, OR, XOR, and Bit test and set of any bit of any register (including I/O) data. Test under mask and test compliment under mask of 8- and 16-bit data.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes of load byte and word: immediate, register direct, register indirect, register indirect with post-increment, register-indexed, and register bit. Memory direct, memory indirect, memory indirect with post-increment, memory indirect with pre-decrement, memory indexed with immediate short and long offsets and register offset, memory indirect bit. Block transfer between memory spaces. Push and Pop for system and user stack.

III—PROGRAM-MANIPULATION INSTR
Jump Unconditional and Relative, Jump Relative Conditional, Decrement Byte/Word and Jump if Non-zero, Call and Return, and Interrupt Return.

IV—PROGRAM-STATUS-MANIP INSTR
Set Register Pointers for independent 8- and 16-register groups for fast context switching. Push effective address for C compiler optimization. Sign Extend 8 to 16 bits. Wait for Interrupt and Halt. Compare and Jump if True/False, otherwise post-increment.

Specification summary: Architecture features 3 memory spaces: program memory, data memory, and the register file. Program memory is 0, 8, 16, or 32 kbytes of internal masked ROM or EPROM; as much as 64 kbytes of external memory; or 8 Mbytes of bankswitch memory. Data memory can contain as much as 1280 bytes of internal RAM and 512 bytes of EEPROM; as much as 64 kbytes of external memory; or 8 Mbytes with bankswitch. The register file offers 224 general-purpose registers. All devices include an SPI interface, and a Timer/Watchdog. On-chip peripheral functions can include 16-bit multifunction timers, 8-bit A/D converters with watchdog, full-duplex UART with Baud Rate Generator and as many as nine 8-bit I/O ports. The devices are available in 40- and 48-pin DILs and 44-, 68-, and 84-pin PLCCs.

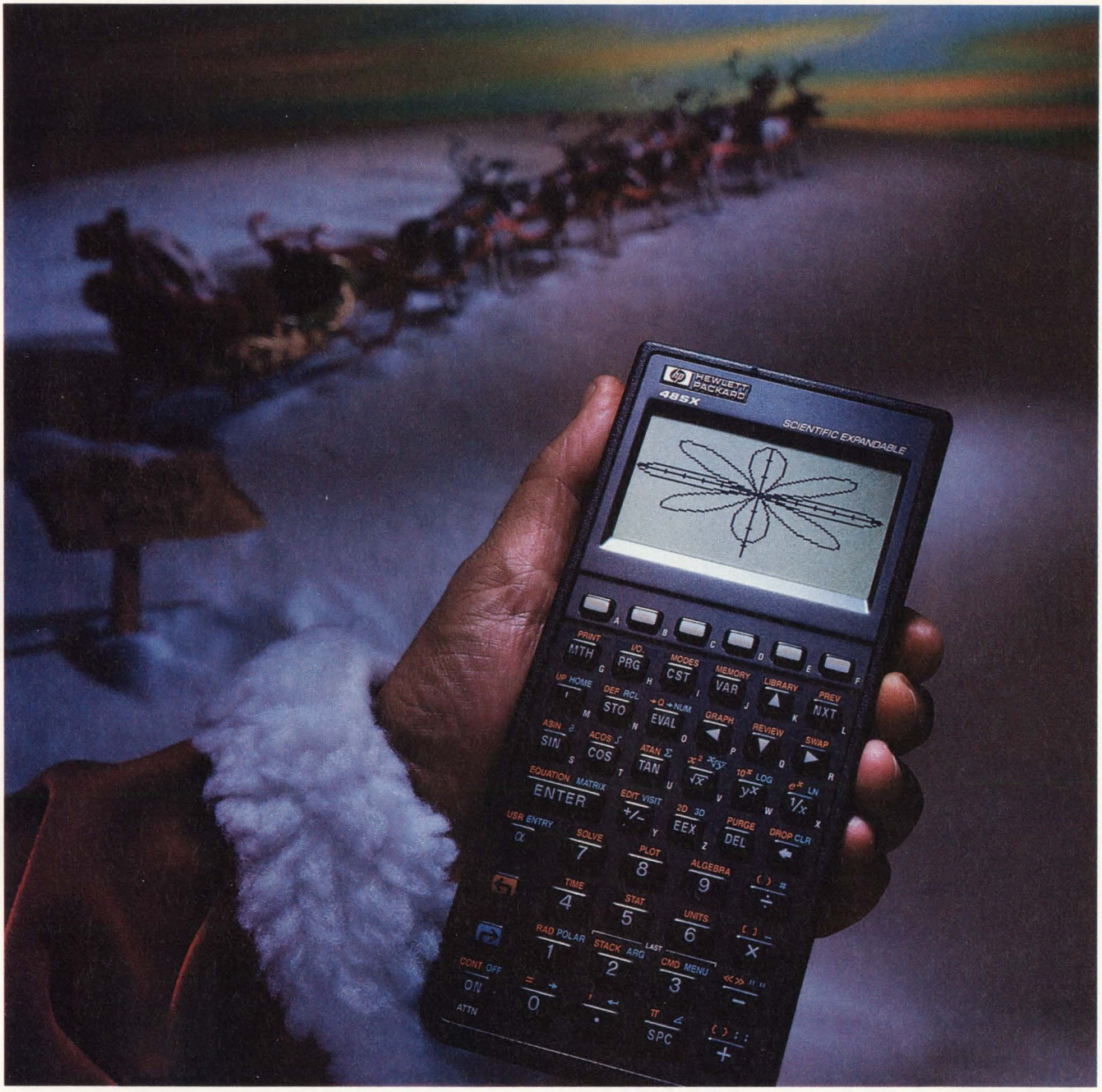
Hardware notes: 1. Diagram is of the company's ST9040.
2. All peripheral-control registers are placed into pages within the register file, allowing a complete upgrade path between family members. This upgrade path is based on common code and the retention of all of the 224 general-purpose registers.
3. You can group all registers in two banks of eight registers or one group of 16, allowing fast context switching upon interrupt.
4. The CPU lets you assign each peripheral its own interrupt and DMA priority level.

Software notes:
1. The microcode of the ST9 instruction set is optimized to operate on 16-bit data through the 8-bit ALU (8-bit ADD executes in 500 nsec and a 16-bit ADDW requires 830 nsec at the maximum 12-MHz internal speed using a 24-MHz external oscillator).
2. Instructions affecting memory require a working register pair as a pointer and operate in the memory space selected (either the program or data memory.)

HARDWARE — SUPPORT — SOFTWARE

From SGS-Thomson: Development package includes real-time emulators, adaptable to all present and future ST9s.
Evaluation Boards: The EVMST9 is adaptable to all present and future family members.

From SGS-Thomson: PC- and Sun-3 and Sun-4-hosted software development tools (including high-level macro-assembler, incremental linker, archiver, and software simulator). ANSI C compiler.
From Others: Verilog USA (Dallas, TX) offers the Logiscope Software Quality Auditing Tool for the macro-assembler.



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SPECIFICATIONS

MODEL	SCM-1	SCM-2	SCM-5	SCM-2500
Freq. Range (MHz)				
LO, RF	1-500	10-1000	1250-1800	500-2500
IF	DC-500	DC-500	DC-500	DC-500
Conversion Loss (dB)				
mid-band	6.0	6.0	5.5	5.7
total range	6.5	7.0	5.5	6.4
Isolation (dB)	(L-R) (L-I)	(L-R) (L-I)	(L-R) (L-I)	(L-R) (L-I)
low-band	60 50	50 55	28 18	35 18
mid-band	45 45	40 40	28 18	35 18
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C115 REV. F

Z180, HD64180 — 8-BIT CMOS

AVAILABILITY: Now for 6-, 8-, and 10-MHz parts.
COST: For 10-MHz Z180, $12 (100) and $8 (1000). For 6-MHz HD64180, $6 (100) and $5 (1000).
SECOND SOURCE: None.
CORE: Zilog and Hitachi consider the basic Z180 and 64180 a standard cell for building high-integration μPs and microcontrollers.

Description: Jointly developed enhancement of Z80 with various peripheral functions such as memory management (to reach larger, 1M-byte memory space), 2 DMA channels, 2 serial ports, and timers added on CMOS CPU chip. Z-suffix versions are totally compatible with Z80-family peripherals chips. Both Z- and R-suffix devices interface to the 6800 and Intel 80xx series buses.

Status: CMOS enhancements to the widely used Z80. Has on-chip memory-management unit (MMU), multiple DMA channels, and UART. These chips don't have sophisticated big-computer features, such as separate privileged "system" control registers, nor do they have a cache. Both the Z180 and 64180's MMUs translate between the Z80 64-kbyte address space and their own 1M-byte space. These families have received a boost from all Z80 users and third-party supporters of the venerable Z80.

Zilog Inc
Intelligent Peripheral Controller Product Line
Phone (408) 370-8000
For more information, Circle No. 365

Hitachi America Ltd
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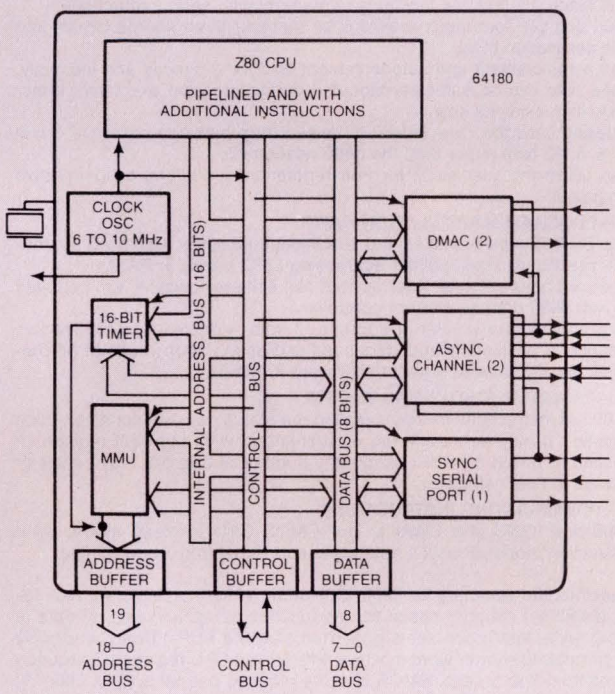
HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for basic core. Both Zilog and Hitachi are expanding upon this core.
2. The 647180x is a single-chip version of the 64180 and adds 16 kbytes of one-time-programmable EPROM, 512 bytes of RAM, 54 I/O pins, a 16-bit timer, and a 6-channel analog comparator. It comes in 84-pin PLCCs, 80-pin flatpacks, and 90-pin shrink DIPs. Because of EPROM, Hitachi bills this style μC as a zero-turnaround-time part, saying it is cost-effective in volumes as great as 10k. Hitachi also sells the part in windowed 84-pin leadless chip carriers to aid development.
3. The 648180W is another single chip version of the 64180 and adds 256 bytes of EEPROM, 1 kbyte of ROM, 35 I/O pins, and an ADC.

I—DATA-MANIPULATION INSTRUCTIONS
Unsigned 8 × 8-bit = 16-bit multiply.
Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator.

II—DATA-MOVEMENT INSTRUCTIONS
Immediately addressed locations.
Block output to I/O. Must set up MMU bank registers to translate between 64 kbytes of Z80 and 512 kbytes external.

V—POWER-SAVING INSTRUCTIONS
Sleep command disconnects processor from clock. Interrupt or reset will reconnect.

Specification summary: Object-code compatible with Z80 (and 8080, 8085). Pipelined CPU. On-chip MMU generates 19 bits (512 kbytes external physical address space) in the DIP package and 20 bits (1M byte external) in surface-mount packages. 2-channel direct-memory-access controller, 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (Z-suffixed versions are matched to Z80-family peripherals). CMOS versions provide 50 mW at 4-MHz operation; lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

Software notes:
1. Only new instructions beyond Z80 instructions listed.
2. The MMU adds base registers to Z80 16-bit addresses to produce the 20-bit addresses needed externally.
3. Trap interrupt can be used both for catching undefined op codes and for letting users extend instruction set.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Zilog offers a Z180 and serial communications controller (SCC) applications board to test and evaluate the chips.
From Hitachi: ASE Adaptive System Emulator ($7000) plus H6805M01S, a 256-kbyte memory board for use with IBM PC, HP6400, or DEC VAX as host. Real-time operation as fast as 8 MHz and real-time tracer buffer for 2048 machine cycles. All hardware lines are captured, and the trace is automatically disassembled.
From Others: Several companies offer hardware support for the family. Among these suppliers are American Automation, Huntsville Microsystems, Sophia Systems, Z-World, Softaid, Zax, and Orion.

Microtec Research (Santa Clara, CA) supplies macroassembler, utilities, Pascal, and C compilers (to run on IBM PC and DEC VAX hosts). Avocet (Rockport, ME) and Allen Ashley (Pasadena, CA) have announced IBM PC-based assemblers. Hitachi provides help so that the additional 64180 instructions can be treated as macros on a Z80 macroassembler. Boston Systems Office (Waltham, MA) offers a VAX-hosted assembler ($1200). Software compatible with CP/M (Digital Research) and MSX (Microsoft) operating systems (latter being result of project for Japanese market). American Automation has cross software to go with development hardware (assembler, C compiler, and debugger).
Archimedes (San Francisco, CA) offers a C compiler ($995 for IBM PC; $3995 for MicroVAX; and $7995 for VAX).

6800/6802, 6809/6309

8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: As with other mature μPs, costs have dropped, in this case to a couple of dollars per μP), except when a part is at end of its life, in which case prices might rise again.

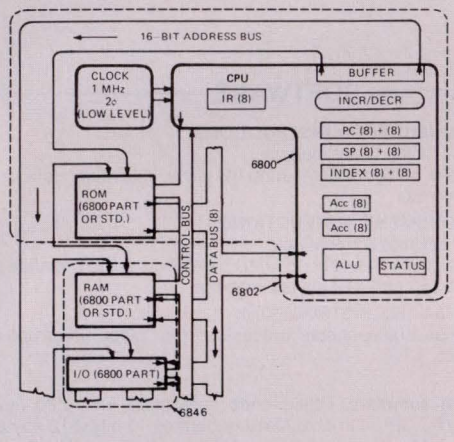
SECOND SOURCE: Hitachi and SGS Thomson.

Motorola Microprocessor Products Group
Phone (512) 440-2000
For more information, Circle No. 367

Description: The 8-bit 6800 CPU was the original part in the family named after it. That family has been broadened to include not only the 2-chip 6802/6846 and 6809 covered here but also the single-chip 6801, the low-end single-chip devices, and the 6804 and the 6805. Note, however, that new CPU members are precisely compatible with the original 6800, especially at the low and high ends. Even the 6809 is only software compatible with the original 6800 at source-code level.

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest μP families. Among its progeny are the 6809 covered here and the following Motorola μPs and μCs, which are described elsewhere in this directory: the 6805, 6801, and 68HC11. The 6800 is now past its prime and is not recommended for new designs; we retain it in the directory for reference. But the newer 6802 and 6809 continue to be shipped in volume. For new designs, Motorola steers designers to the 16- and 32-bit 68000 family (68008 has an 8-bit bus) or to the 68HC11.

HARDWARE — CHARACTERISTICS — SOFTWARE



Part	Description	Clock speed (MHz)	ROM ×(8)	RAM ×(8)	Cost (100 qty)
6800	CPU needs 2-phase clock	1–2	—	—	$4–$5
6802	CPU clock & RAM	1–2 (4-MHz ext)	—	128	$4–$5
6809	CPU	2	—	—	$5–$6
6309	CPU CMOS	3	—	—	$9.50

Hardware notes:
1. Diagram shows 6800 and 6802. The 6809 has another 16-bit index and a second "user" stack pointer, which makes the 6809 more powerful than the 6800; these additional resources give the 6809 many more instructions. On simple benchmarks, the 6809 is 270% faster than the equivalent speed 6800, programs in 42% fewer instructions, and uses 33% less code.
2. Basic 6809 version has on-chip clock. Minimum system results with the following parts: 6809, 6810, and 6846. 6809E version has off-chip clock. An early valid-memory-address (VMA) signal on 6809E allows 3-MHz bus operation with a 2-MHz memory. External clock permits multiprocessing.
3. The MMU (6829) allows the 6809 to run 32 concurrent protected tasks per management unit in a 2M-byte address space.
4. Hitachi CMOS version (6309) has 2-, 2.5-, and 3-MHz bus timing; the Sync and CWAI instructions allow a low-power sleep mode.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of two accumulators.
6809 has unsigned 8 × 8-bit multiply with 16-bit product.

II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
6809 can use four index registers for merging three source blocks into one destination block.
Can autoincrement and autodecrement by 1 or 2 directly and indirectly.
Page zero can be software relocated during program execution, effectively increasing its size.
Indexing uses the "true indexing" relationship between base and offset (0, 5, 8, 16 bits) rather than the 6800 relationship.
Can utilize the user stack for Polish-notation operations or interpretive languages.

III—PROGRAM-MANIPULATION INSTR
Has PDP-11-type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM.
Does not have vectored interrupt but can achieve function with software or with 6828 priority interrupt controller.
6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs.

IV—PROGRAM-STATUS-MANIP INSTR
6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction.

V—POWER-SAVING INSTRUCTIONS
6309 has SYNC and CWAI to put CMOS CPU in sleep mode. Sync instruction stops μP until it gets go-ahead signal from interrupt line.

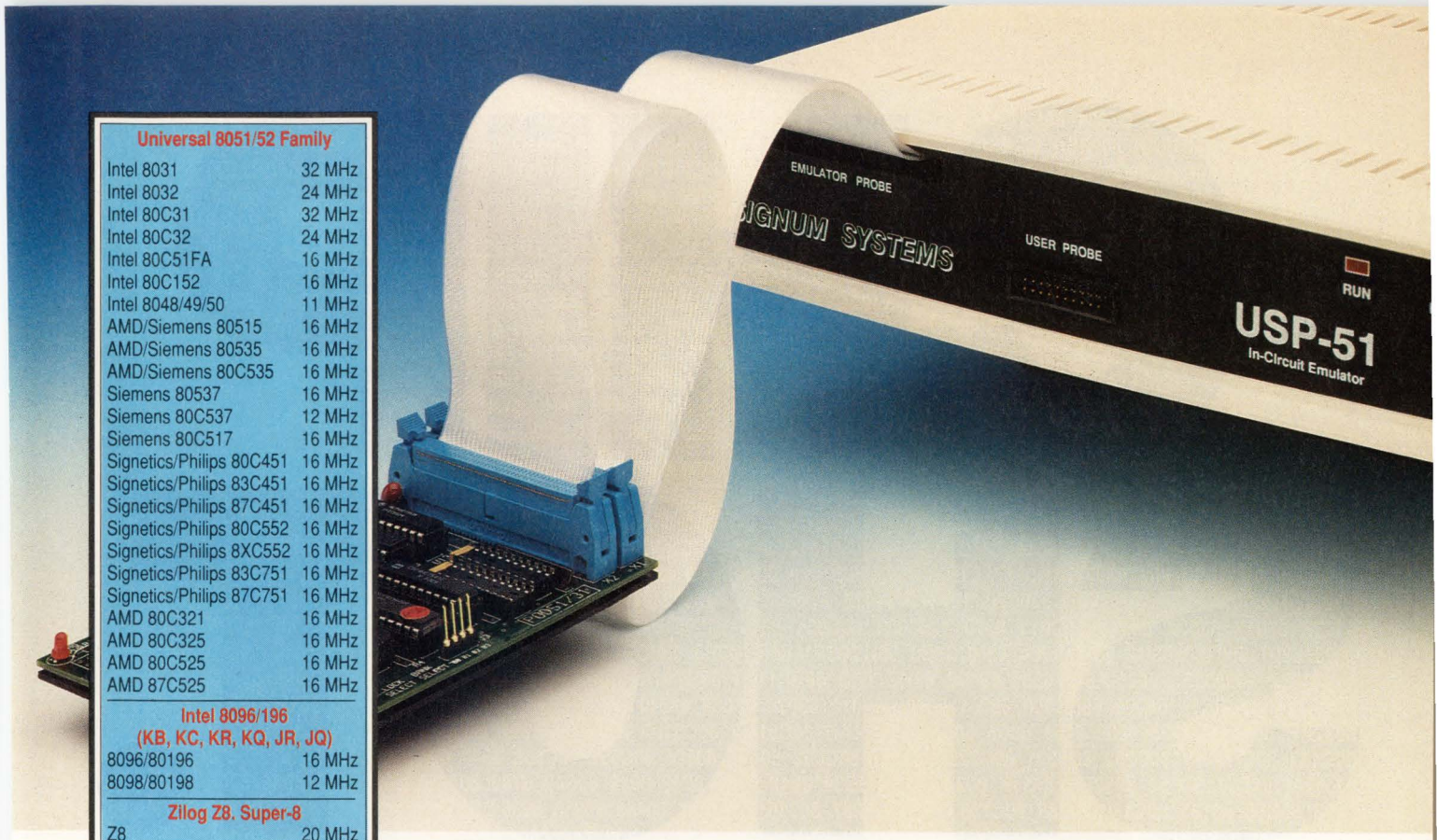
Specification summary for 6800: Common-memory architecture with 16-bit (64-kbyte) memory space for instructions, data, and I/O; all data is 8-bits wide. Instruction set is patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 μsec. NMOS circuitry requires one 5V supply, 500mW; housed in 40-pin DIP. Versions with −55°C to +125°C range also available.

Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upwardly compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing increases throughput. Instruction set has 59 mnemonics and 7 addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-inherent operations executing in 1 μsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page-zero register is retained but can be software relocated anywhere in memory via programmable register. The chip requires one 5V supply. Two versions, each in 40-pin DIP.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: Emulators range from low-cost (hundreds of dollars) boards to HDS-300 system (about $5000) plus personality modules ($5000).
Support systems and OEM boards available from Motorola Semiconductor Div, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-6900 or (602) 438-3500.
From others: Tektronix and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola's "Micromodule" 8-bit boards.

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733. The basic assemblers and other tools are for IBM PC.
Two versions of Basic are available for the 6809: Basic-M and Basic09. The latter is designed to be fast and to permit structured programming. A Pascal compiler diskette is available.



Universal 8051/52 Family	
Intel 8031	32 MHz
Intel 8032	24 MHz
Intel 80C31	32 MHz
Intel 80C32	24 MHz
Intel 80C51FA	16 MHz
Intel 80C152	16 MHz
Intel 8048/49/50	11 MHz
AMD/Siemens 80515	16 MHz
AMD/Siemens 80535	16 MHz
AMD/Siemens 80C535	16 MHz
Siemens 80537	16 MHz
Siemens 80C537	12 MHz
Siemens 80C517	16 MHz
Signetics/Philips 80C451	16 MHz
Signetics/Philips 83C451	16 MHz
Signetics/Philips 87C451	16 MHz
Signetics/Philips 80C552	16 MHz
Signetics/Philips 8XC552	16 MHz
Signetics/Philips 83C751	16 MHz
Signetics/Philips 87C751	16 MHz
AMD 80C321	16 MHz
AMD 80C325	16 MHz
AMD 80C525	16 MHz
AMD 87C525	16 MHz
Intel 8096/196 (KB, KC, KR, KQ, JR, JQ)	
8096/80196	16 MHz
8098/80198	12 MHz
Zilog Z8. Super-8	
Z8	20 MHz
86C94	30 MHz
Super-8	20 MHz
Texas Instruments DSP's	
320C10/15	33 MHz
320C16	35 MHz
320C17	20 MHz

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* System capable of 32 MHz; actual emulation speeds limited by currrent device speeds.

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Circle #13 for Logic Analyzer info

Circle #14 for Development Systems info

650X/65C0X — 8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: WDC's CMOS prices range from $2 in lower speed, high volume to $50 for high speed, lower volume.
SECOND SOURCE: WDC created and licensed most of the CMOS designs. It has licensed Rockwell, California Micro Devices, ITT-Intermetall in West Germany, and about 20 other companies.
CORE: WDC has developed the semicustom 6502 core as NCR and others now use it. Many suppliers now specify it as part of their cell libraries.

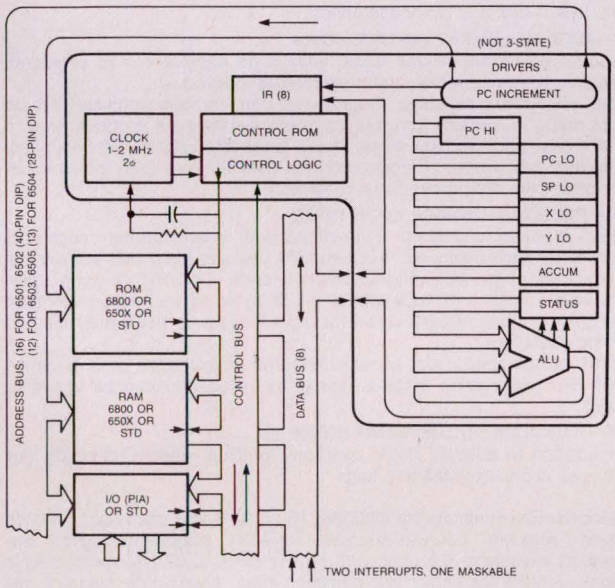
Originator of 6502 Commodore (Westchester, PA) no longer sells chips to the merchant market. WDC developed CMOS version.

Western Design Center Inc
Phone (602) 962-4545
For more information, Circle No. 368

Description: Original design team's goal was to achieve as much PDP-11-style addressing capability as would fit in an economical chip. Because of the μP's short 8-bit index registers, it is optimally suited only to applications requiring access of smaller blocks of memory, although it benchmarks ahead of most other 8-bit μPs with respect to its speed of execution of high-level languages, such as Basic and Pascal. New CMOS parts consume little power and have small economical die that gets still smaller with today's finer geometries. See 6500/1 for single-chip versions and 65SC816/802 for 16-bit-internal version.

Status: The falling share of market for this μP appears to indicate that it has reached the end of its life cycle. However, the architecture lives on in the form of single-chip versions (see 6500/1 and especially the 50740 in this directory) and ASIC versions. Some of these have very large unit volumes, so the 6502 architecture may remain, by volume, the leading 8-bit architecture in the world.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes on CMOS versions:
1. CMOS 65CXX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are a new 4-phase clock that gives decreased memory access time and a memory-lock output and bus-enable input that simplify multiprocessor designs.
3. Among the software enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
4. Decimal mode is automatically set off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
5. A BRK followed by interrupt is executed.
6. See instruction set for comments on new instructions.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports. CMOS parts have bit manipulation.

II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, although index offset is limited to 8 bits in 2 CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables. CMOS parts have indexed-absolute indirect and zero-page indirect.

III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model. CMOS parts have branches on bit test.
Stack pointer for implementing 256-byte LIFO in external RAM.

IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits. 6502 and 6512 have external input to one status bit, useful for handshaking with peripherals.

V—POWER-SAVING INSTRUCTIONS
Wait and Stop on 65C02, respectively, stop processor and disconnect clock to lower power consumption. New operating voltage range of 1.2 to 5.25V with an I_{DD} of 0.1 μA/kHz at 2.8V.

Specification summary: Common-memory architecture with instructions, data, and I/O in same 64-kbyte space; 57 instructions (68 for CMOS). Many instructions provide choice of 13 PDP-11-type addressing modes (15 for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mV supply. Some CMOS parts can run at 8-MHz clock frequency (125 nsec/cycle). CMOS parts require 4 mA/MHz for operation and 10 μW for standby. Although it supplies the μPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: LCE emulator ($1250), which interfaces to IBM PC host.
Western Design Center recommends using Hewlett-Packard (Colorado Springs, CO) logic analyzers and WDC Toolbox ICE with IBM PC host ($4995).
From California Micro Devices: GEM-I ICE package ($3750) capable of interfacing with a variety of host computers including ISIS development system and Apple. Functions as a stand-alone assembler and disassembler using a nonintelligent terminal. Evaluation board for 65SC150 ($499) that functions as in-circuit system when coupled with GEM-I.
From NCR: Hardware emulator interfaces to Apple IIe through RS-232C port. Allows complete in-circuit software debugging.
From Dynatem (Irvine, CA): AIM-65 single-board computer and RM industrial modules.

From California Micro Devices: 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).
From NCR: Monitor for use in conjunction with emulator. Supports breakpoint, change memory and registers, software trace, and real-time execution.
From others: Because the 6500 has been so widely used, there are innumerable sources of software at different language levels: for example, Byte Works (Albuquerque, NM), Roger-Wagner Publishing (El Cajon, CA), and 2500 AD (Aurora, CO), Avocet (Rockport, ME), California Microsystems (Union City, CA), and American Automation (Tustin, CA).

8086/8088

8/16-BIT NMOS AND CMOS

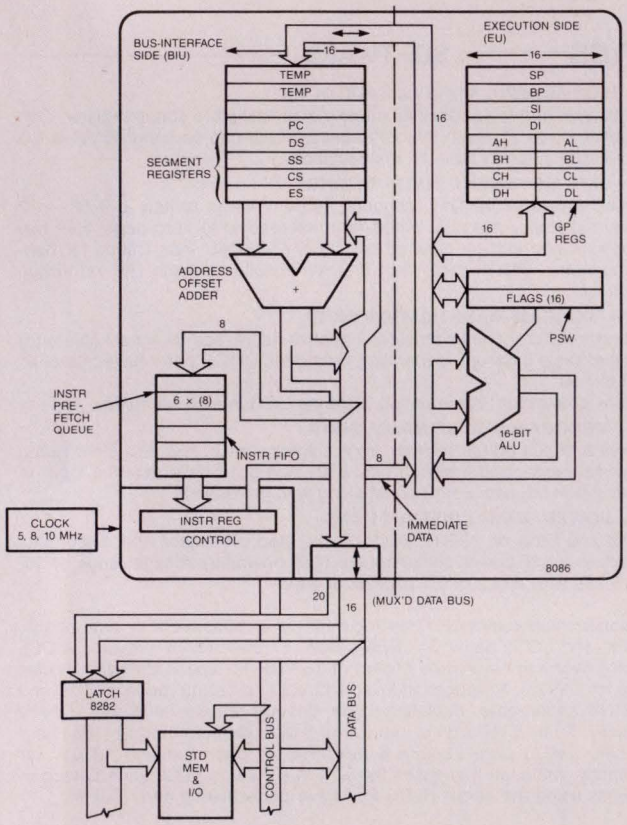
AVAILABILITY: Now.
COST: Under $10 (1000) for NMOS 8086/88, under $15 (1000) for CMOS 8086/88. Siemens' NMOS parts are under $4.50 (1000). Chips and Technologies 8680 single-chip PC costs $35 (10,000).
SECOND SOURCE: For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, and OKI. Chips and Technologies' 8680 single-chip PC is source-code compatible with the 8086.

Description: The 8086, 8088, and their low-power CMOS implementations (80C86/80C88) share a 16-bit internal architecture that has a software base of more than 10,000 DOS applications. The 8088 (used in the original IBM PC and its clones) has an 8-bit external data bus to allow the manufacture of lower cost systems with full 16-bit software capability. C&T's 8680 combines an 8086-compatible core with CGA-compatible graphics, power management, a memory controller, device emulation, a serial port, and system logic.

Intel Corp
Embedded Controller Operation
Phone (602) 961-8051
For more information, Circle No. 369

Status: Next to the 8080/Z80 family, the 8086 family has been the most successful μP family. Its most visible application has been in the IBM PC and its many clones. The newest implementation, from Chips and Technologies, recently began shipping.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for initial family member, 8086.
2. 8088 is downgraded version of 8086. It has only 8-bit-wide external data output bus (only 8 lower bits of address bus are multiplexed for data). Some pin functions have been changed. Prefetch queue is only 4 bytes (to prevent overuse of bus). Instruction execution is slower because all 16-bit fetches and writes take 4 extra cycles.

I—DATA-MANIPULATION INSTRUCTIONS
8-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
Logicals.
Bit, byte, word, and block operations.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base-plus index, and base-relative indexed.
Use of segment registers: Programmer can, through software, set up four areas in memory with four segment registers—a program area, a stack area, and two data areas. These areas need not be full 64 kbytes, and they can overlap. Programmer can alter the four area locations by modifying the segment-register contents.

III—PROGRAM-MANIPULATION INSTR
Has call, jump, and return instructions both inside program segments and to different segments. Intrasegment call and jump use self-relative displacement for position-independent code. Conditional jump upon Boolean functions of flags within ±128 bytes of instruction. Iteration control of loops, a repeat prefix for rapid iteration in hardware-repeated string operations.
Note: Jumps can occupy varying amounts of execution time, because with BIU's instruction prefetch, the program counter can be ahead of itself.

IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8080/85 flags: overflow, interrupt enable, direction (for strings), and single-step trap flags.

Specification summary for 8086/88: 16-bit CPU that can reach 1M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 μsec with 5-MHz clock (0.37 μsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry; requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch eight pins from minimum to maximum external system mode. Harris CMOS 8086 dissipates only 10 mA/MHz when running; clock can be stopped for 500 μA standby.

Specification summary for 8680: This implementation operates over a 3 to 5V range and uses a 4-stage pipeline and 14-MHz clock to improve performance. A 26-bit address bus provides 64-Mbytes of address space and supports PCMCIA (Personal Computer Memory-Card International Association) memory cards. The memory manager supports as many as three banks of pseudo-static RAM, SRAM, and/or DRAM. In addition to 8086 compatibility, the 8680 includes Chips and Technologies' Superstate,which enables I/O and interrupt monitoring without BIOS modification. Additional capabilities of Superstate include device emulation, power management, and redirection of interrupts before recognition by the OS, application program, or TSR (terminate-stay-resident) programs.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE in-circuit emulator ($8495) supports 8086/8088 to 10 MHz. Emulators are hosted on IBM PC. All ICEs provide windowed, menu-driven, source-level display and μP debugging. Performance analysis tool (iPAT) consists of a hardware base unit, an interface to ICE, and host software for the IBM PC/XT and PC/AT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 8086/8088.
From others: Because of popularity, family is widely supported by third-party universal development systems. Contact Chips and Technologies for support information for its 8680.

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. DB-86 software debugger provides windowed, menu-driven, source-level debugging with full source-code display. Hosts include PC-DOS and VAX/VMS. Prices start at $750 (for DOS versions).
From others: Because of wide base of 8086/8088-based systems, particularly the IBM PC, there exists third-party software of all sorts, enough to fill whole catalogs. Check with Intel and various trade journals.

Text continued on pg 121

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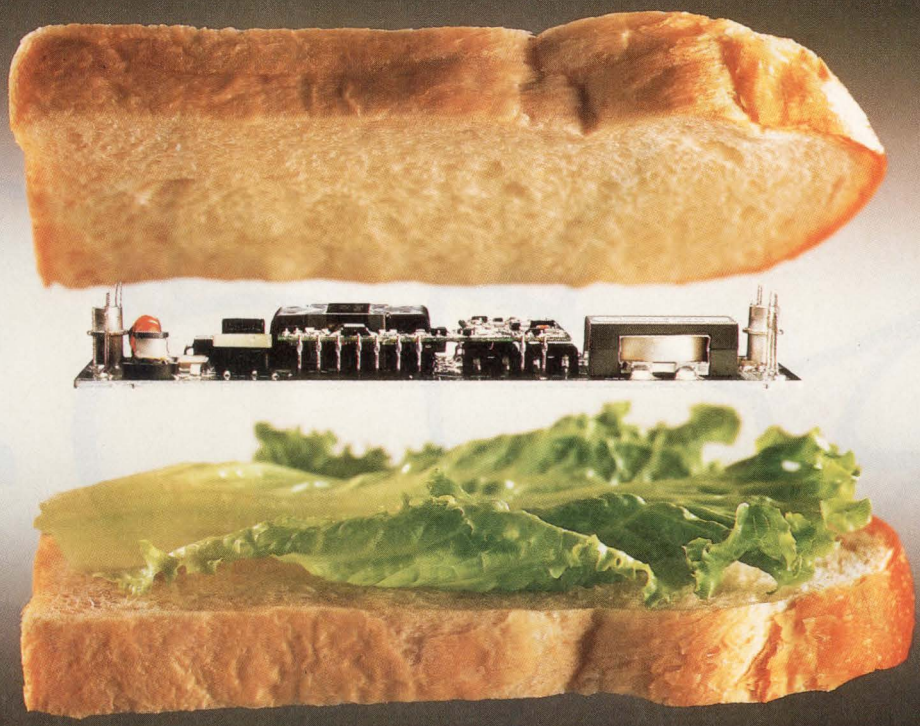

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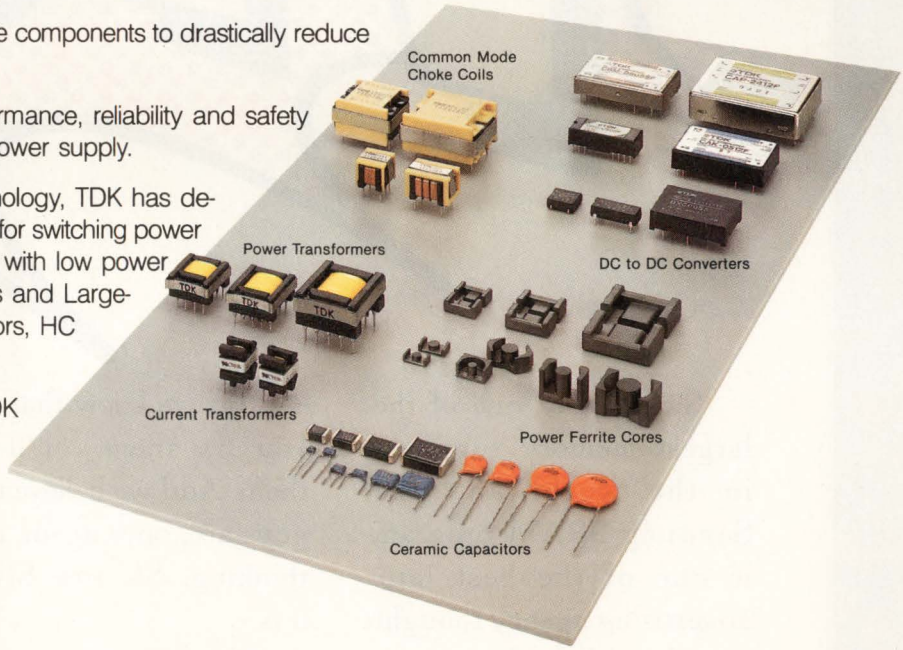

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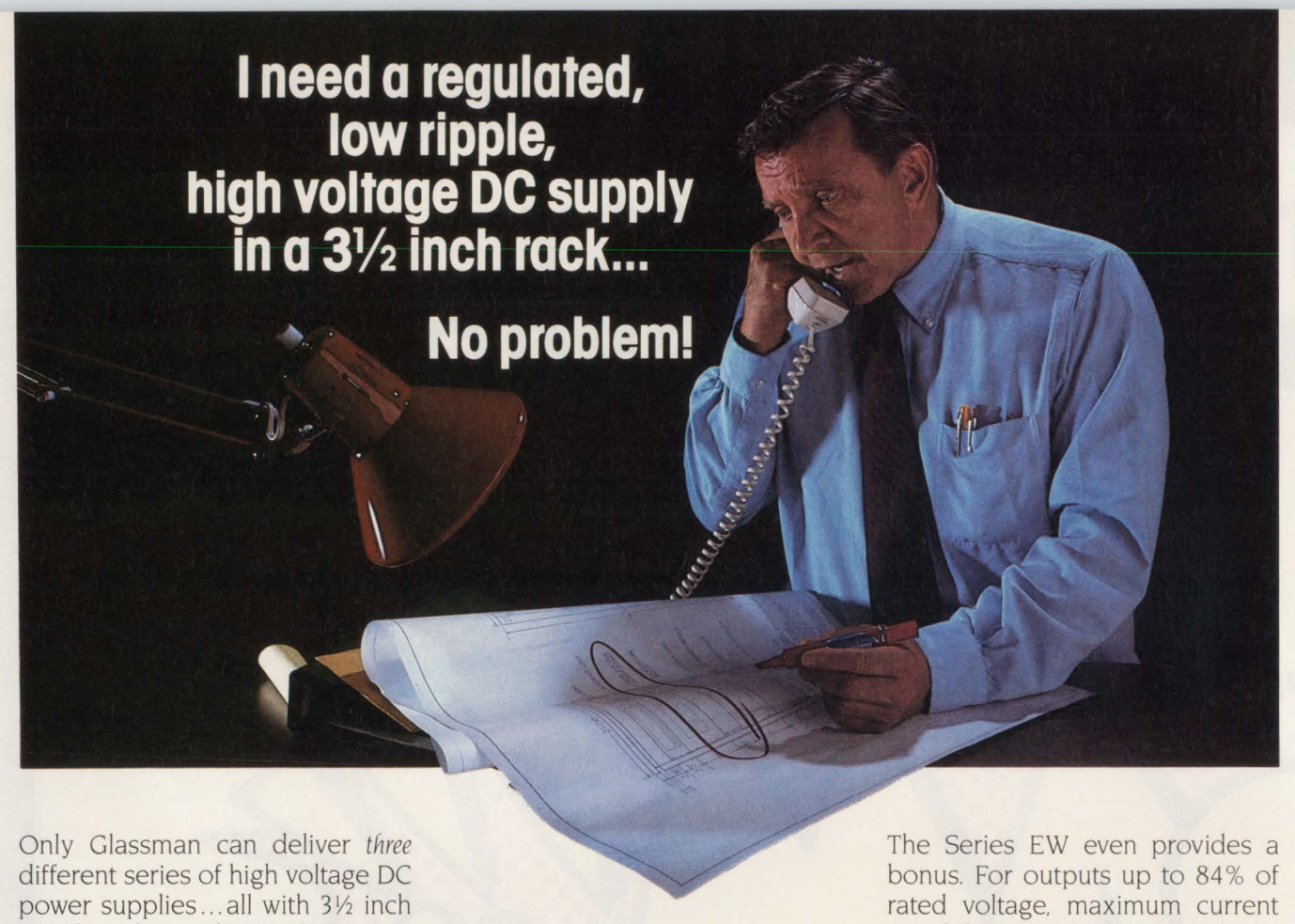

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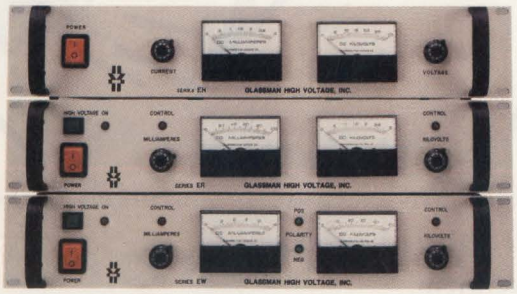

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Japan
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FAX: (044) 877-3395

CIRCLE NO. 79

Z280

8/16-BIT CMOS

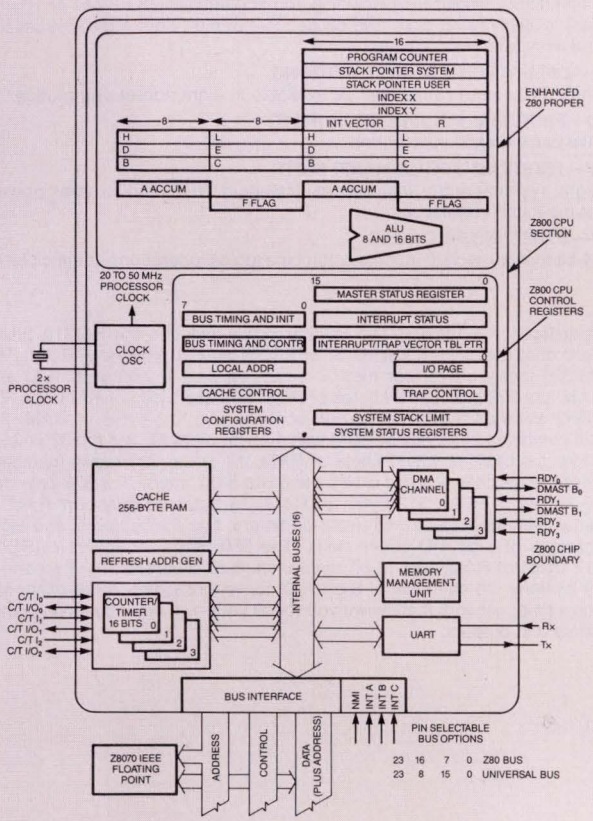
AVAILABILITY: Now for 10- and 12.5-MHz versions.
COST: About $18 in large volumes.
SECOND SOURCE: None.
CORE: Zilog is incorporating elements of Z280 in its megacell library, so it can rapidly put together new combinations. The company claims it can turn around a semicustom design using its megacells in a matter of days. However, it does not plan to offer ASIC tools to customers.

Description: Enhanced Z80 μP, upgraded to the point that it has most of the features of larger 16/32-bit machines. It has "privileged" system-control hardware and associated software for multiuser, multitasking operating systems. It has memory management for virtual memory and incorporates cache to achieve high throughput with moderate-speed external memories.

Zilog Inc
Phone (408) 370-8000
For more information, Circle No. 370

Status: The Z280 became available in late 1987. The Z280 lets designers upgrade Z80-based PCs into multiuser systems that have large virtual memories and, claims Zilog, high performance. Compared with other Z80 enhancements, such as the Zilog Z180/Hitachi 64180, the Z280 offers a greater performance edge. Zilog is also pushing the Z280 as an upgrade for dedicated systems using Z80s as embedded controllers.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
16×16-bit=32-bit multiply and 32/16-bit=16-bit divide.
Extended block mode manipulates data in blocks.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes for more general 16-bit use of Z80's 16-bit registers (HL, DE, BC pairs).
Instructions to communicate with coprocessors.

III—PROGRAM-MANIPULATION INSTR
Jump on auxiliary accumulator/flag.
Jump on auxiliary register file in use.
System call.

IV—PROGRAM-STATUS-MANIP INSTR
Master status register; see category V instructions.

V—SYSTEM-CONTROL INSTRUCTIONS
Instructions for added system-control registers. These are privileged instructions to permit operating system to define the system configuration upon start-up, to use the new system stack pointer, master status register, and to set up the cache's operation mode.

Specification summary: The Z80 is upwardly enhanced toward a general-register 16-bit minicomputer. On-chip memory management addresses as much as 16 Mbytes of external memory. CPU is 3-stage pipelined with on-chip 256-byte program-and-data cache to keep recently used instructions on chip for fast execution at 10-MHz internal bus clock. The I/O is pin programmable to match either 8-bit Z80 bus or 16-bit "universal" bus. Also included on chip are four 16-bit timer/counters, 4 DMA channel controllers, dynamic-memory refresh control, and a serial UART port. The Z280 is fabricated in static CMOS and housed in 68-pin PLCC; Zilog will offer other options as requested by customers.

Hardware notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. The integration not only lowers system cost, but provides a speed advantage: When all subsystems are on chip, the system speed automatically increases.

Software note:
Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).

HARDWARE — SUPPORT — SOFTWARE

From others: Softaid (Columbia, MD) has a low-cost real-time development system, and CDS ((704) 876-2346) offers evaluation boards for several popular buses. Logic analyzers are sold by Hewlett-Packard and Tektronix.

From Zilog: You can obtain a debug monitor program and a cross-assembler with Zilog's evaluation board. Zilog plans no other software support.
From others: 2500 AD is shipping a cross-assembler and is reported to be working on a C compiler. CDS offers both a cross-assembler and a C complier.

H8/300 FAMILY

8/16-BIT CMOS

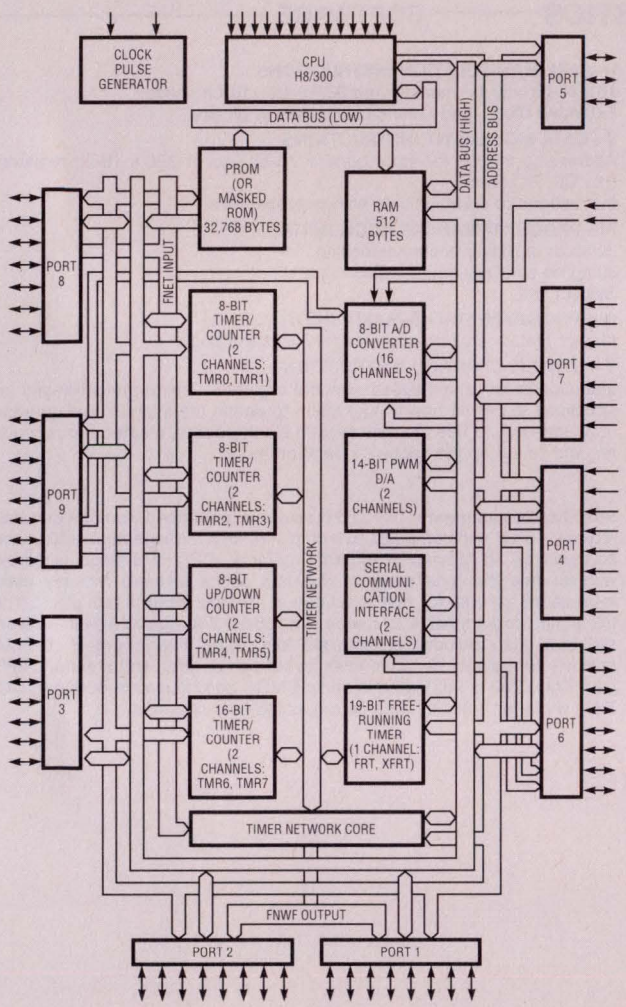
AVAILABILITY: Now.
COST: In large volumes, the H8/310 naked die costs less than $10. Other devices, in 100 qty, range from $14.25 for the H8/322 to $25 for the H8/350.
SECOND SOURCE: None.
CORE: Hitachi considers the basic H8/300 CPU as a standard cell for building high-integration μPs and μCs.

Description: The H8/300 family of single-chip microcontrollers offers 16-bit internal data paths with an 8-bit ALU and external data bus. The family shares the 8/16-bit core CPU, which features a general-purpose register architecture that allows any register to act as an accumulator.

Hitachi America Ltd
Semiconductor and IC Div
Phone (415) 589-8300
For more information, Circle No. 371

Status: Seven devices in the family are currently in full production. These devices range from the H8/310 (tailored for Smart-card applications) to the H8/350. The microcontrollers are available in one-time programmable versions from stock.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
14 arithmetic instructions including add and subtract (8 ± 8 bits or 16 ± 16 bits), multiply (8 × 8 bits), and divide (16 ÷ 8) bits. Four logic instructions and eight shift instructions.

II—DATA-MOVEMENT INSTRUCTIONS
Three MOV instructions that are available in eight addressing modes.

III—PROGRAM-MANIPULATION INSTR
Five basic branch instructions.

IV—PROGRAM-STATUS-MANIP INSTR
Eight system-control instructions including NOP and special power-saving-mode instructions.

V—OTHER INSTRUCTIONS
14-bit manipulation instructions combine logical operations at the bit level.

Specification summary: The H8/300 family includes the H8/310 Smart Card controller with 8 kbytes of EEPROM and 10 kbytes of ROM. The H8/320 family offers four members with varying amounts of ROM and RAM: the 322 provides 8 kbytes of ROM and 256 bytes of RAM; the 323 offers twice as much—16 kbytes of ROM and 512 bytes of RAM; the 324 combines 24 kbytes of ROM with 1 kbyte of RAM; and the 325 mixes 32 kbytes of ROM with 1 kbyte of RAM. All of the 320 family members offer 2 serial channels and a 16-bit and two 8-bit timers. The 330 provides 16 kbytes of ROM, 512 bytes of RAM, 15 bytes of dual-port RAM, 1 serial channel, a 16-bit and two 8-bit timers, two PWM timers, and eight channels of 8-bit A/D conversions. The 350 offers 32 kbytes of ROM, 512 bytes of RAM, two 16-bit timers, six 8-bit timers, 2 PWM timers, a 19-bit timer, 16 channels of 8-bit A/D conversions, two serial channels, and a timer network that allows you to roll your own timer by mixing timer inputs and outputs.

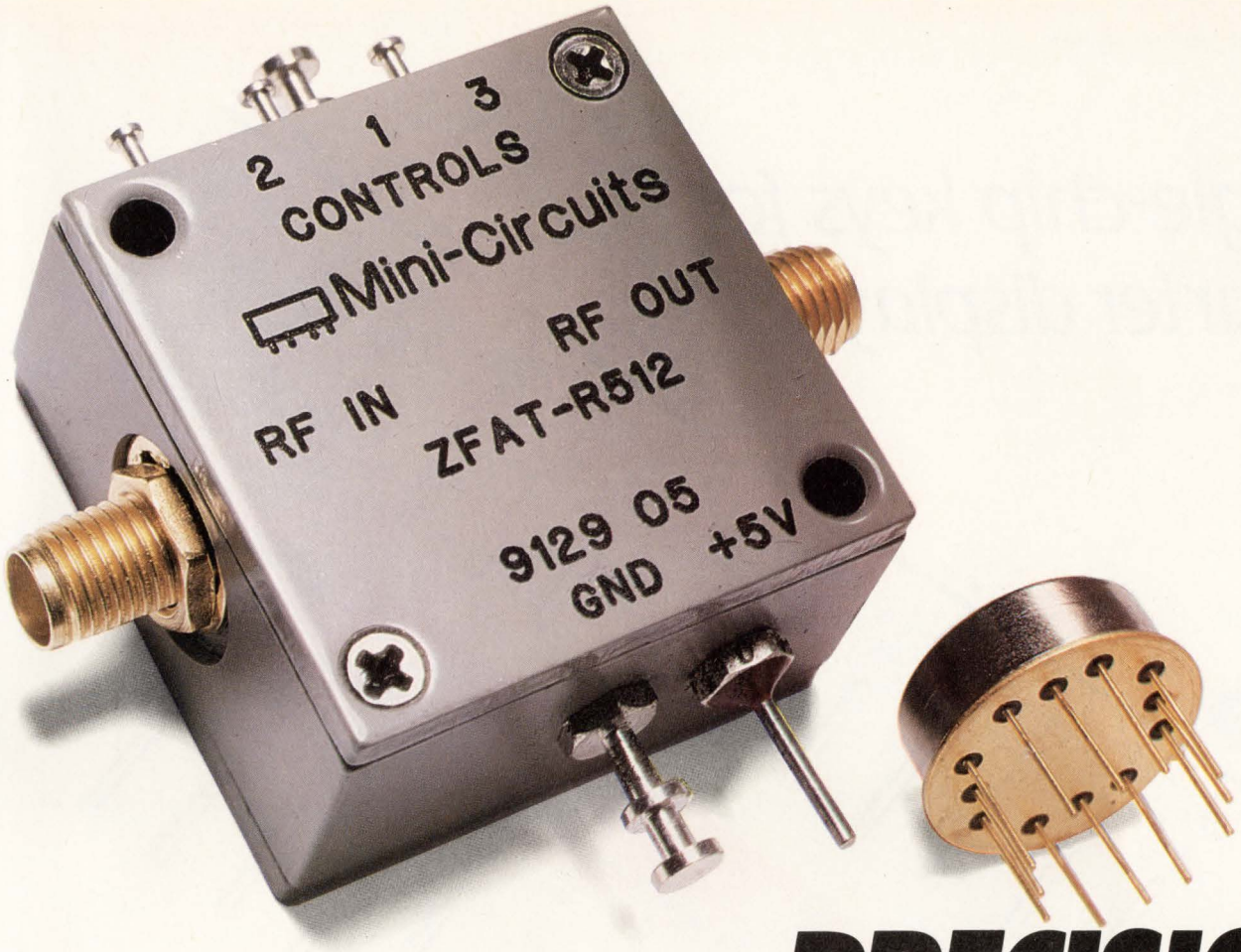
Hardware note:
The H8/300 CPU is register based and allows 200-nsec instruction execution. This family provides sixteen 8-bit registers, which you can concatenate into eight 16-bit registers. All instructions are either 2 or 4 bytes. The 16-bit data paths facilitate arithmetic operations for address calculations. Both the 330 and 350 devices include an on-chip A/D converter with 12.2-μsec conversion time.

Software note:
Arithmetic and logic instructions are performed as register-to-register operations or with immediate data. There are 8 addressing modes: register direct, register indirect, register indirect with displacement, register indirect with post-increment or predecrement, absolute, immediate, pc-relative, and memory indirect. All instructions are either 2 or 4 bytes long.

HARDWARE — SUPPORT — SOFTWARE

Hitachi supplies a common base unit and personality modules for in-circuit emulation of all H-series devices (about $6000). Hewlett-Packard (Palo Alto, CA) and Sophia Systems (Palo Alto, CA) also offer development systems.
Evaluation Boards: Hitachi supplies boards (about $400) for evaluation and limited program development. The boards offer an in-line assembler and limited debug monitor. A consistent interface is provided by an XRAY software module to the simulation/debugger, evaluation board, and in-circuit emulator.

Hitachi supplies a complete tool chain consisting of an ANSI C compiler, assembler, linker, loader, utilities, and a software simulator/debugger for workstation and PC hosts. Third-party vendors Microtec Research (Santa Clara, CA), Avocet (Rockport, ME), and Software Environments (Dallas, TX) supply similar products. Special software, such as a Fuzzy Logic compiler and a real-time operating system, is provided by Togai Infralogic (Irvine, CA) and Byte-BOS (San Francisco, CA), respectively.



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NEC

CIRCLE NO. 81

78K SERIES

8/16-BIT CMOS

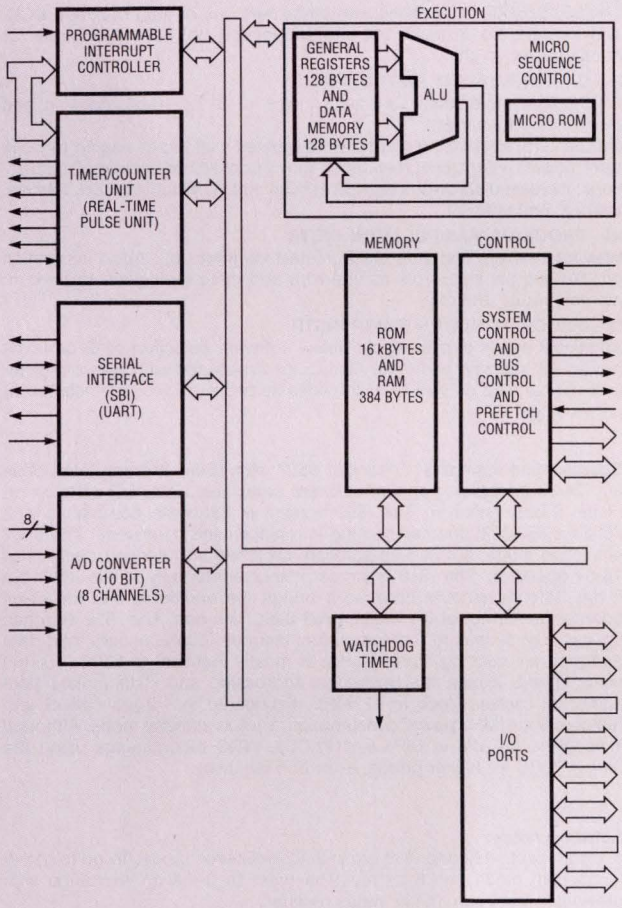
AVAILABILITY: Now.
COST: $6 to $20 (1000).
SECOND SOURCE: None.

Description: The 78K2 Series is a family of 8-bit microcontrollers, whereas the 78K3 Series is a 16-bit family. Both offer features for real-time applications. These μCs feature a Peripheral Management Unit which handles many of the repetitive interrupt requests without CPU intervention. The family has a 3-byte prefetch to reduce external program-fetching latency. Available peripherals include DACs and ADCs, timers, serial I/O ports, UARTs, and real-time output ports. On-chip memory can include as much as 2 kbytes of RAM, as much as 32 kbytes of ROM or OTP EPROM, and as much as 512 bytes of EEPROM.

NEC Electronics
Phone (415) 969-6000
FAX (415) 965-6130
Literature (800) 632-3531
Technical support (800) 366-9782
For more information, Circle No. 372

Status: The K series of microcontrollers is currently used in applications such as hard-disk drive control, audio, communication, and environmental control.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logic instructions. 16-bit ADD, SUB, and Compare. 8×8-bit and 16×16-bit multiply. Divides of 32-bit and 16-bit numbers. Increment and decrement bytes of 16-bit words. Bit manipulation of memory and I/O.

II—DATA-MOVEMENT INSTRUCTIONS
8- and 16-bit transfers, including Moves and Exchanges, Shifts, Rotates, and Push and Pop on stack.

III—PROGRAM-MANIPULATION INSTR
Subroutine calls and returns, break, unconditional and conditional branches, select register bank, and context switching.

IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition.

V—SYSTEM-LEVEL INSTRUCTIONS
Accumulator-oriented set, multiple register banks, condition flags. CALLF and CALLT provide compact subroutine calls to save memory space.

Specification summary: The intelligence of the peripheral-management unit lets the chip handle many interrupt events without processor intervention. Instruction cycle times can be as long as 125 nsec at 32 MHz.

	RAM (bytes max)	ROM OR OTP/EPROM (bytes)	Interrupts (Internal/ external)	I/O lines	ADC (channels/ bits)	DAC (channels/ bits)	Assorted timers
78k2							
7821x	1024	8 to 32k	12/7	54	8/8	N/A	4
7822x	640	16k	9/8	71	N/A	N/A	3
7823x	1024	16 to 32k	12/7	64	8/8	2/8	4
7824x	512	16k	14/7	54	8/8	N/A	4
78k3							
78320-4	1024	32k	13/8	39	8/10	N/A	2
78327/8	512	16k	11/4	23	8/10	N/A	3
78350/2	640	32k	4/5	24	N/A	N/A	2

Hardware note:
Diagram favors μPD7821x, which features synchronous and asynchronous serial I/O, counter/timers with compare and capture registers, multichannel ADCs, DACs, and a peripheral-management unit.

Software note:
The 78K series has eight 8-byte register banks mapped in RAM. You can use each bank either as 8 bytes or four 16-bit words. Switching banks provides a fast method for switching contexts when interrupt service routines are entered. Context switching also utilizes the register banks as separate working registers for multitasking operations.

HARDWARE — SUPPORT — SOFTWARE

The IE-7832X and IE-7835X provide full-feature in-circuit emulation for the K3 Series. Individual package types require optional probes.
Evaluation Boards: EB-7832X-PC and EB-7835X-PC accept optional probes for target emulation.

The RA78K is the relocatable macro assembler for the 78K Series. The assembler includes a structured assembler preprocessor that provides many of the control and assignment features found in C compilers. A C compiler is also available.

65C816/65C802 — 8/16-BIT CMOS

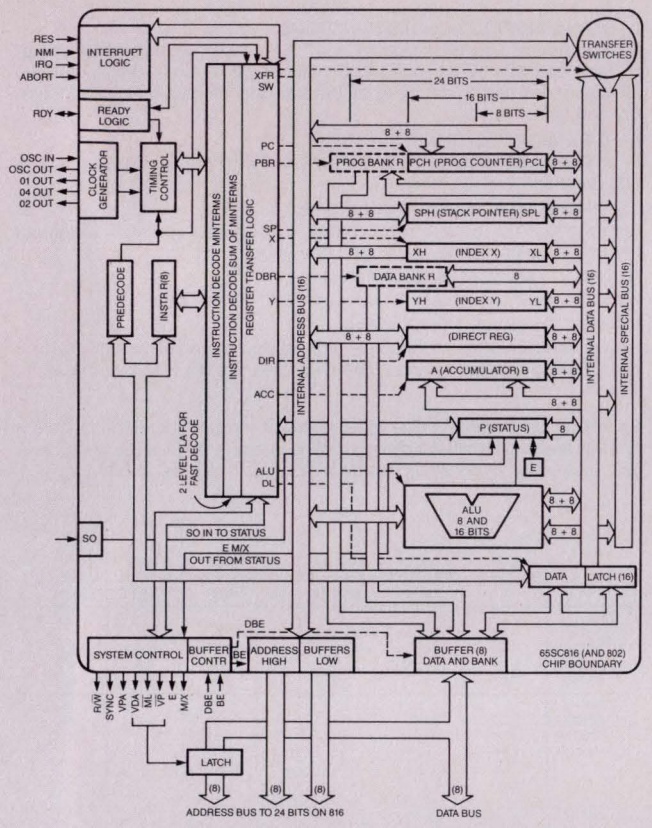
AVAILABILITY: Now.
COST: Prices range from about $2 to $50.
SECOND SOURCE: VLSI and California Micro Devices said to be main sources, but WDC says it has licensed others in US and abroad.
CORE: All suppliers are considering this as a μP megacell in their libraries.

Description: CMOS 8/16-bit μPs featuring software compatibility with 8-bit 6502 (both original NMOS 6502 and enhanced CMOS 65C02). The -802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The -816 has a different pinout, but expands the addressing range of the 6502 from 64 kbytes to 16 Mbytes. Additional hardware enhancements on the -816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

Western Design Center Inc
Phone (602) 962-4545
For more information, Circle No. 373

Status: Apple's use of the 65C816 in the IIGS upgrade provides a firm basis for hardware and software availability. Software support is growing as third-party houses that have supported the 6502-based Apple computers convert software to take advantage of the expanded memory and other capabilities of the 65C816.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
The 6502/65C02 instructions with 16-bit versions of add, subtract, BCD, and logicals. No multiply, but 65C832 version will have provisions for floating point on chip.

II—DATA-MOVEMENT INSTRUCTIONS
6502/65C02 instructions, but with choice of 8- or 16-bit indexing and 8-or 16-bit data widths.
On the -816, addressing can span 16 Mbytes with aid of paging through new register extensions. New block-move (forward or backward) instructions. Increased stack-pointer addressing modes, including stack relative, indirect, and indexed.

III—PROGRAM-MANIPULATION INSTR
Wait for interrupt and stop clock (restart via interrupt). Abort instruction on -816 via pin input acts as interrupt and directs program to perform memory repair and retry.

IV—PROGRAM-STATUS-MANIP INSTR
Additional bits in status register allow software selection of 8- or 16-bit modes for indexing and data. Also, E bit associated with status register (but not handled as part of it) provides software choice of emulation or native mode.

Specification summary: Enhanced 6502 with 16-bit internal data option and 24-bit addressing option, software selectable. Data I/O off chip remains 8 bits, however. The -802 version is hardware compatible with 6502 (or 65SC02) and can be plug-in replacement. It will reset into 6502 emulation mode, but can be software-switched into varying degrees of 16-bit operation. The -816 is almost identical internally to the -802, but it has different pinouts because it brings the additional bits for 24-bit address space out of the multiplexed 8-bit data-bus. The -816 also has special control lines to facilitate virtual memory, coprocessors, and data and program caching. Performance is mostly identical to 6502 of same clock speed, except that extended addressing and data modes take additional cycles. Clock to 12 MHz. Fabricated in 1.2-μm CMOS and features 3-mA/MHz power consumption, 1 μA in standby mode. Although it supplies the μPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

Hardware notes:
1. Compare diagram with previous 6502/65C02 (see diagram, pg 115) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits, and the 16-bit registers widened to 24 bits.
2. The -816's control-bus outputs facilitate multiprocessing, caching, and virtual memory. The control-bus inputs let you abort instructions for virtual memory as well as control-bus access.

Software notes:
1. Upon reset, -802 and -816 are in 6502 emulation mode. To go to native (enhanced) mode, the E-bit must be reset to 0 via an exchange with previously reset carry-bit in status register.
2. Full-sized 16-bit registers may facilitate high-level-language compiler-writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help facilitate compiler writing. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Tendency of native (enhanced) mode coding to become trickier than 6502 due to tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

HARDWARE — SUPPORT — SOFTWARE

WDC recommends Hewlett-Packard (Colorado Springs, CO) logic analyzers and WDC Toolbox ICE with IBM PC host ($4995).

From Byte Works (Albuquerque, NM): The ORCA/M cross-assembly and utility package. C and Pascal compilers are also available.
From Apple (Cupertino, CA): Assembler and debugger ($100) and C compiler.
From others: Supporting products are also available from S-C Software (Dallas, TX); Roger-Wagner Publishing (El Cajon, CA); 2500 AD (Aurora, CO); California Microsystems (Union City, CA); and American Automation (Tustin, CA).

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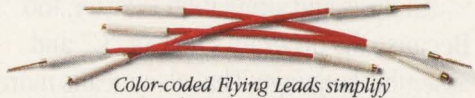
5515A PLCC Clip Kit contains seven Pomona Quad® Clip Adapters from 20-84 pins.



Color-coded Flying Leads simplify interconnections between PLCC or SOIC test clip and logic analyzer sockets or emulator pods; 3 inches long, with female socket one end to .79 dia. pin, 25 leads per pack.

See your Authorized Pomona Distributor or contact POMONA ELECTRONICS, 1500 E. Ninth St., P.O. Box 2767, Pomona, CA 91769. (714) 623-3463. FAX (714) 629-3317.

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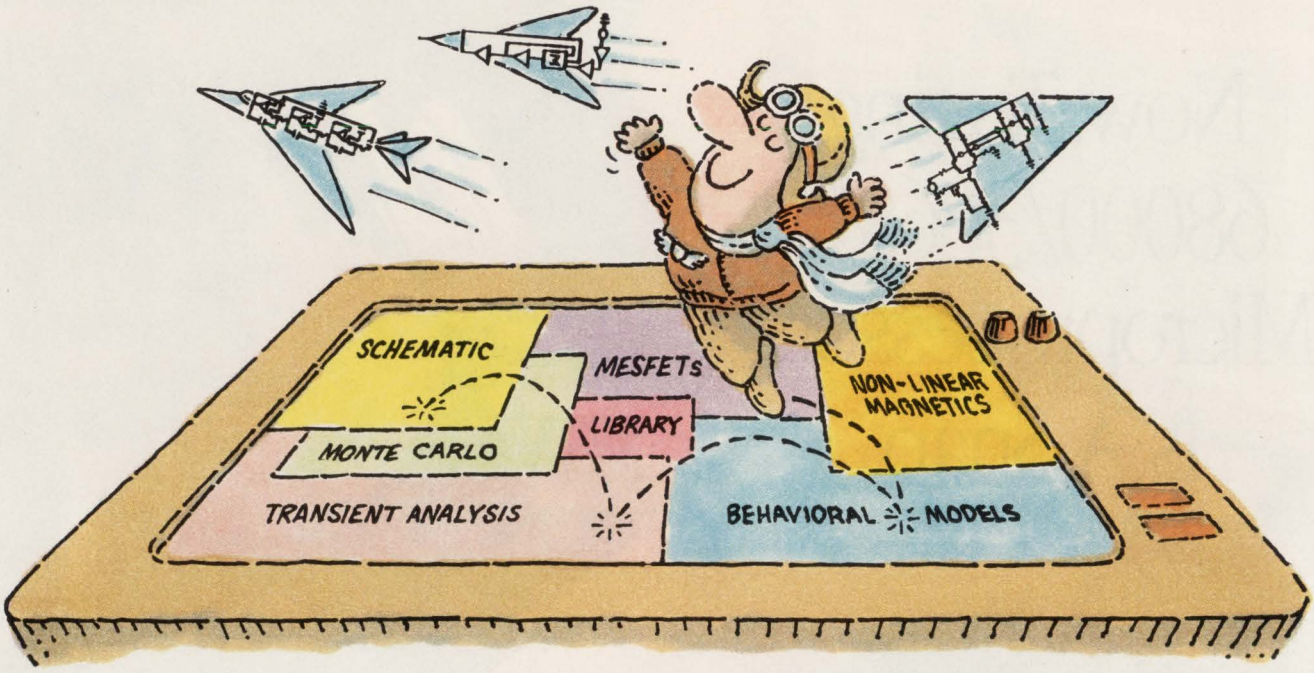
CIRCLE NO. 82



THE NEW MICRO-CAP III.™ SO YOU CAN TEST-FLY EVEN MORE MODELS.

It wasn't easy. But we did it. Made the long-time best-selling IBM® PC-based interactive CAE tool even better.

Take modeling power. We've significantly expanded math expression capabilities to permit comprehensive analog behavioral modeling. And, beyond Gummel Poon BJT and Level 3 MOS, you're now ready for nonlinear magnetics modeling. Even MESFET modeling.

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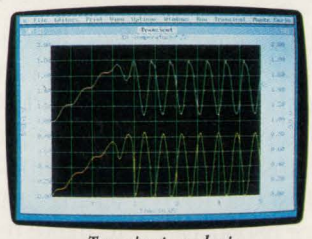
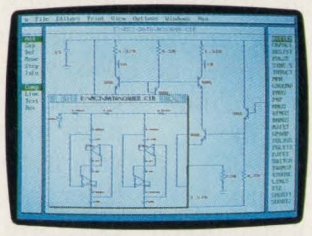
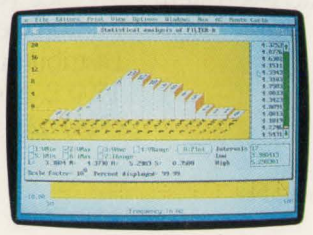


Transient analysis



Schematic editor



Monte Carlo analysis

And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

Cost? Still only $1495. Evaluation versions still only $150. Brochure and demo disk still free for the asking. Call or write for yours today. And see how easily you can get ideas up and flying.

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CIRCLE NO. 83

80186/80188

8/16-BIT NMOS AND CMOS

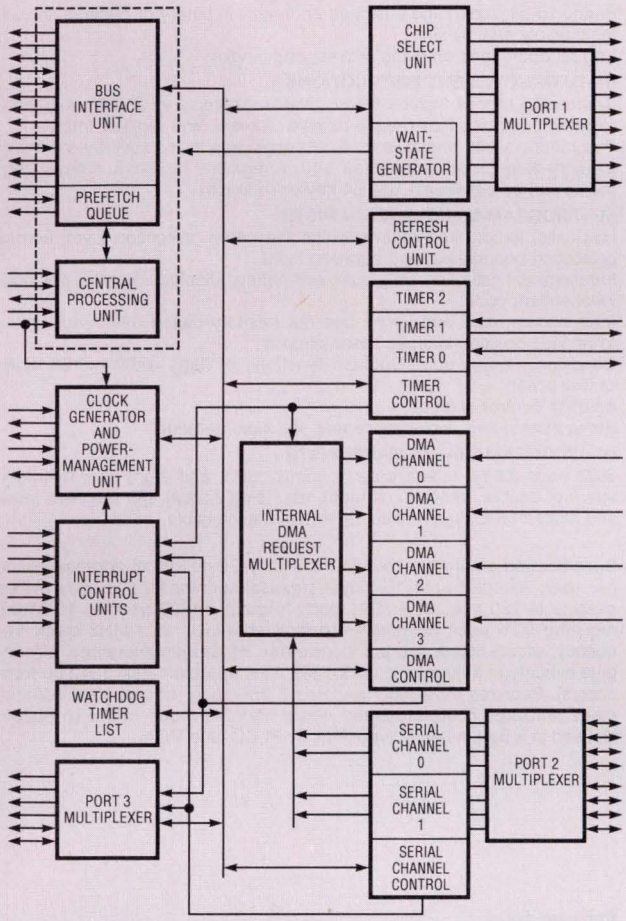
AVAILABILITY: Now for NMOS and CMOS 80186/188.
COST: $8.45 to $17.70 (1000).
SECOND SOURCE: AMD and Siemens.
CORE: Intel's ASIC group has incorporated the 80C186 in its cell library.

Intel Corp
Embedded Controller Operation
Phone (602) 961-8051
For more information, Circle No. 374

Description: This family uses a modular, static, low-power core to which Intel has added an interface bus. Currently, the most highly integrated family member is the 80C186EC, which includes a clock generator, 4 independent DMA channels, 2 serial communications channels, a programmable interrupt controller, 3 programmable 16-bit timers, 22 I/O pins, chip-select logic, a programmable wait-state generator, a watchdog timer, a direct numerics interface, DRAM refresh control, and a power-management unit. Other devices provide a subset of these functions.

Status: The 186 family is used in more than 6000 customer applications. The vendor intends to provide further enhancements and higher integration to satisfy future demand.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for 80C186EC. As with the 186EA and EB versions, the EC incorporates several power-saving features. These devices are fully static and offer a power-management unit with idle and powerdown modes. Powerdown mode turns off power to both the CPU and the on-chip peripherals, idle mode keeps the CPU active. The XL offers a powerdown mode but sacrifices the idle mode.
2. The 188 is the 8-bit external-data-bus version of the 186. All devices in the family are available with either an 8- or a 16-bit external data bus. The 188 has all other 186 features except for the numerics interface.

I—DATA-MANIPULATION INSTRUCTIONS
Includes addition, subtraction, multiplication, and division. Arithmetic operations may be performed on 4 types of numbers: unsigned binary, signed binary (integers), unsigned packed decimal, and unsigned unpacked decimal. Binary numbers may be 8 or 16 bits long. Decimal numbers are stored in bytes: 2 digits per byte for packed decimal, and 1 digit per byte for unpacked decimal.

II—DATA-MOVEMENT INSTRUCTIONS
Data-transfer instructions move single bytes, words, and double words between memory and registers, as well as between register AL or AX and I/O ports. Stack manipulation instructions are also included, as are instructions for transferring flag contents and for loading segment registers. Subgroups of the data transfer instructions are general-purpose data, I/O, address-object, and flag-transfer instructions.

III—PROGRAM-MANIPULATION INSTR
Includes unconditional transfers, conditional transfers, iteration controls, and interrupts. Unconditional transfers include call, jump, and return instructions, which may transfer control to a target instruction within the current code segment (intersegment transfer). The conditional transfer instructions are jumps that may or may not transfer control, depending on the state of the CPU flags at the time the instruction is executed. You can use the iteration control instructions to regulate the repetition of software loops. The interrupt instructions let programs, as well as external hardware devices, activate interrupt-service routines.

IV—PROGRAM-STATUS-MANIP INSTR
Flag operations include carry, direction, and interrupt enable, all of which let programs control various CPU functions.

V—SYSTEM-LEVEL INSTRUCTIONS
The processor controls instructions responsible for external synchronization, which include halt, wait, escape, and lock.
The 186 family adds 10 instructions to the core instructions of the 8086/8088. Sharing the basic instructions ensures upward code compatibility within the processor family.

Specification summary: 16-bit CPU with direct-addressing capability to 1 Mbyte memory and 64 kbyte I/O with 6 address modes. There are fourteen 16-bit registers. Register-to-register operations execute at 125 nsec for the 16-MHz device. Some family members are available in speeds ranging from 8 to 20 MHz. The typical power consumption for the 80C186EB is 115 mW at 8 MHz in active mode, 80 mW at 8 MHz in idle mode, and 50 μW in powerdown mode. Package options include PGAs, LCCs, QFPs, PQFPs, and PLCCs, depending on the device selected.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE186 in-circuit emulator ($10,618) supports 80186 to 10 MHz. ICE186 in-circuit emulator ($15,995) supports 80186/80C186 to 16 MHz. I²ICE188 ($8495) and ICE 188 ($9995) support 8-bit bus versions of the 80186 (80188/80C188).
From others: The family is widely supported by third-party universal development systems.
Evaluation Board: An evaluation board ($400) is also available from Intel.

From Intel: Macroassembler, including linker, locator, mapper, and librarian and high-level-language compilers, including PL/M, C, Fortran, and Pascal. The Zcon code converter is a stand-alone program that converts from Z80 source code to 8086 source code.
From others: Because of a range of 8086- and 8088-based systems, in particular the IBM PC, there is third-party software of all sorts, enough to fill catalogs. Check with Intel and various trade journals.

80286

16-BIT NMOS AND CMOS

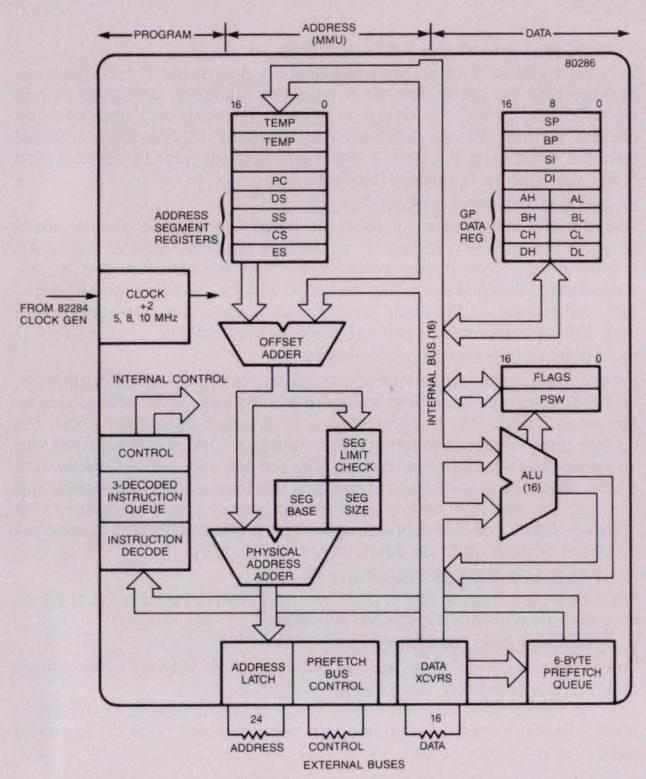
AVAILABILITY: Now for all devices to 25 MHz.
COST: $10 (1000) for 8-MHz device; $13.50 (1000) for 12.5-MHz device. $30 (1000) for 12.5-MHz 80C286. Siemens charges $8, $12, and $21 (1000) for 8-, 12.5-, and 16-MHz devices, respectively.
SECOND SOURCE: AMD and Siemens. Harris for CMOS 80C286.

Description: The 80286 is upward compatible with the 8086 and 80188 and includes on-chip memory management and hardware support for multiuser, multitasking systems. A 4-level protection model provides task/task and user/operating-system protection. The 8-MHz 80286 is 6 times faster than the 5-MHz 8086 due to its pipelined architecture, 8-Mbyte/sec bus and 3.5-nsec interrupt time. Used in the IBM PC/AT and its clones.

Intel Corp
Phone (408) 987-8080
For more information, Circle No. 375

Status: Intel has deemphasized the 80286 in favor of its 32-bit siblings, the 80386SX, 80386, and 80486. However, in spite of very low growth, the 80286 still has the highest volume in the 8086 family. Its popularity has been based on the IBM PC/AT. Unfortunately for the second sources, the 80286's big sisters, the 80386SX, 80386, and 80486, are taking over many of its applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
Logical operations on bytes, words, and blocks.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base plus index, base relative indexed, and register indirect.
Programmers can manipulate 16,383 segments in memory by means of memory-base descriptor tables and 4-segment registers. These segments can be between 1 and 64 kbytes in length.

III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks.
Intrasegment calls and jumps use self-relative displacement for position-independent code.
Intersegment calls and jumps use the memory-based descriptor tables to provide position independence of code.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.
String instructions, including repeat, for rapid iteration.

IV—PROGRAM-STATUS-MANIP INSTR
8085 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible.

Specification summary: 16-bit CPU with 1-Gbyte virtual-address space per user, mapped onto 16-Mbyte physical-address space. Bus cycles execute in 250 nsec at 8-MHz clock frequency (200 nsec at 10 MHz), requiring 0.25 μsec for register-to-register moves at 8-MHz clock frequency, with 8-Mbyte/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry in a large chip (335 × 339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has 2 operating modes: Real-address mode emulates 8086; protected virtual-address mode native to 80286. Housed in a 68-pin Jedec type-A LCC, PLCC, and PGA.

Hardware notes:
1. Support chips for 80286: 82C284 clock, 82288 bus controller, 80287 floating-point numeric processor ($187.15 (1000) for 10-MHz version), and 82258 advanced DMA coprocessor.
2. High-integration chip sets for the IBM PC/AT are being offered by Chips and Technologies (San Jose, CA), Zymos (Sunnyvale, CA), VLSI Technology (Phoenix, AZ), Hudson & Supinger (Santa Clara, CA), Capital Equipment Corp (Burlington, MA), and Via Technologies Inc (Sunnyvale, CA), as well as by Intel. These chips consolidate devices used around compute engines for the 80286.

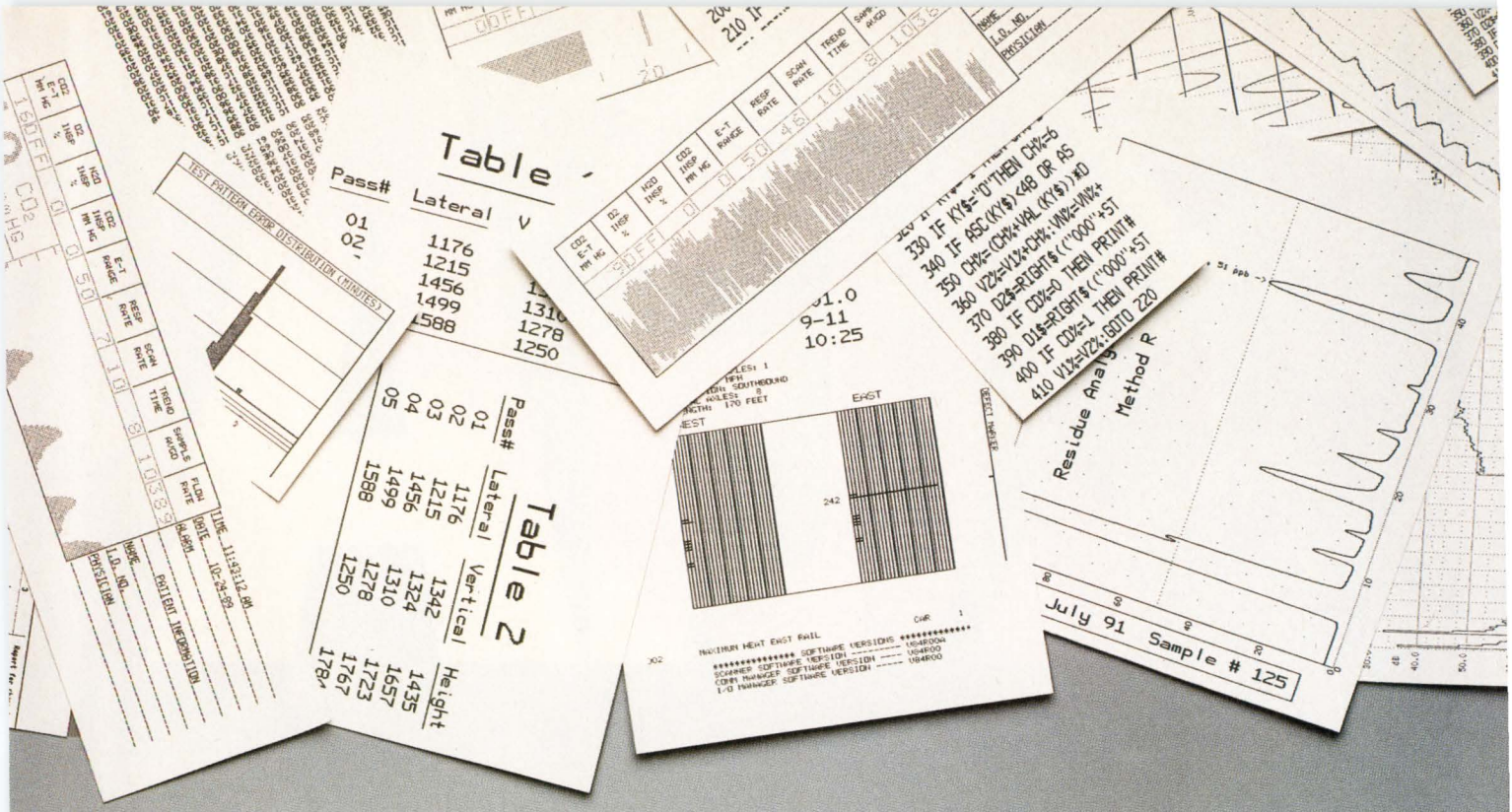
Software notes:
1. Has high-level-language support instructions.
2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.
3. Trusted instructions can only be executed at highest protection levels.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE-286 in-circuit emulator ($12,494) supports 80286 at 8 and 10 MHz. It is hosted on IBM PC/AT and PC/XT. ICE286 ($12,495) supports 80286 at 12.5 MHz. iPAT performance analysis tool includes a hardware base unit, an interface to the in-circuit emulator, and host software for the PC/AT and PC/XT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 80286 in real and protected mode.
From others: A number of third-parties support the 80286 on their universal development systems.

From Intel: Macroassembler (ASM 286), which includes systems builder, binder, mapper, and librarian. Compilers for C, Pascal, PL/M, and Fortran. For applications running in virtual 8086 mode, any of Intel's 8086 software tools can be used. Hosts include PC-DOS and VAX/VMS. $750 for DOS version. Real-time operating systems (Intel's iRMX 286) available.
From others: Other operating systems and compilers being developed by third-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Coherent 286 (Mark Williams), Concurrent DOS (Digital Research), Unix System V (Digital Research), and OS/2 by Microsoft (Redmond, WA).

Text continued on pg 135

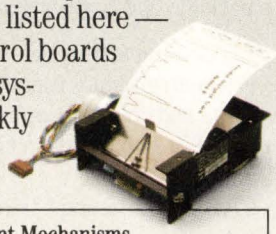


Hard Copy Was Never Easier.

Here's how B-G Instruments' OEM printer family can simplify production of high-quality data printout.

Simple from the start. Our unique DataPlot software cuts development time and effort to a minimum. Just 14 commands let you create printouts with multiple columns, orientations, fonts and graphics. And if you'd prefer, we'll write a custom program for you.

Multiple choices. Hardware options include print mechanisms like those listed here — plus a powerful array of control boards and accessories. So custom systems can be configured quickly and easily to meet your precise needs.

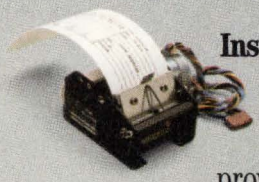


DataPlot Thermal Print Mechanisms

Model Number	Paper Width	Columns Across[2]	Dots / Inch	Dots / Line	OEM Price[1]
PM1224	2.6 inches	18 to 37	100	224	$311
PM1320	2.6 inches	23 to 53	150	320	$296
PM1416	4.5 inches	29 to 69	100	416	$443

1 This is the 300-piece OEM price. It is subject to change without notice.

2 The maximum number of columns depends on the font and size selected. The higher number is for 5 x 7 characters, approximately 16 characters/in.



Instantly apparent quality. Features like thick-film printheads, high-torque stepper motors and heavy-gauge construction provide long life. While permanently lubricated gear trains and gold-plated connectors ensure reliable operation. And special touches such as automatic paper loading simplify operation.

Smart solutions. The power of our software and microprocessor control electronics have helped many customers use our printers to create smart instrument systems. So the same basic tools can serve a variety of different applications.

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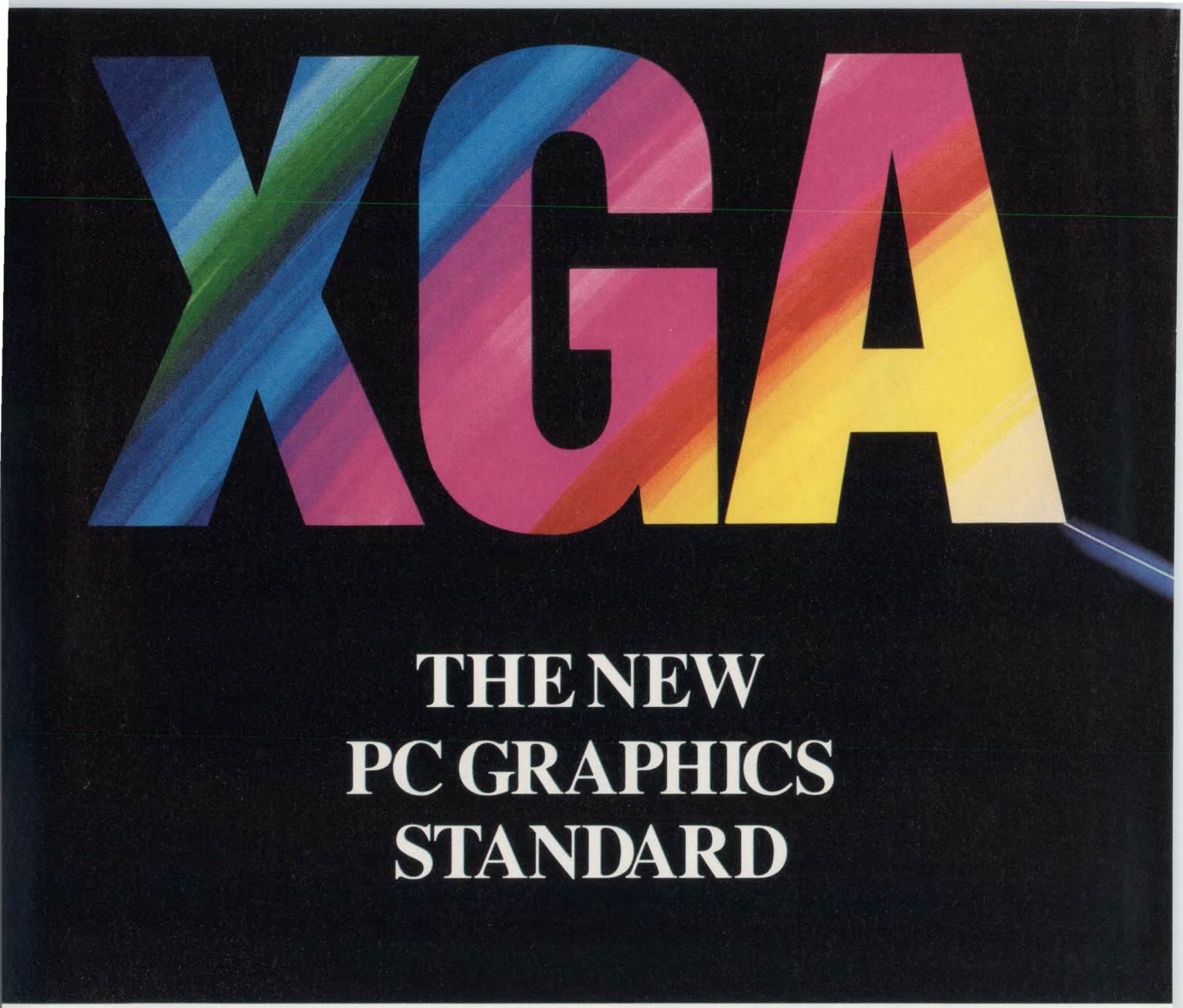
B-G INSTRUMENTS



THE NEW PC GRAPHICS STANDARD

The new XGA standard has opened up an era of higher performance for PC graphics. And when IBM licensed their technology to INMOS, a division of SGS-THOMSON Microelectronics, as manufacturer and sole supplier of the IBM XGA chipset, they did it to ensure that the XGA parts got to the market quickly and reliably, setting the stage for XGA to become the next volume standard in PC graphics. Specifically designed for PCs, XGA is already available to support the MicroChannel Architecture bus, and an AT bus-compatible version is under way. The new XGA standard offers significant enhancements over VGA with:

- higher speed
- higher resolution (up to 1024 × 768)
- more colors (256 up to 64K) giving photo-realistic multimedia-style images
- optimized graphics interface for better windowing
- optimization for use with latest generation processors

Fully VGA compatible, XGA performance specs offer a package that is way ahead:

- 132 column text mode
- extended graphics function mode, including hardware sprite and coprocessor hardware drawing assist
- 90% faster than IBM VGA under DOS, 55% faster under OS/2
- 67% faster running Microsoft Windows applications

TWO CHIPS THAT SET THE STANDARD

The IBM compatible XGA chipset consists of two advanced VLSI chips, the INMOS IMS G190 XGA Serializer Palette DAC in a 144 pin CQFP and the INMOS IMS G200 XGA Display Controller in a 184 pin PQFP. A major advantage of the IMS G200 is its on-chip coprocessor which offloads tasks from the host processor and allows it to support:

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- 1, 2, 4, and 8 bit pixel and bit block transfers
- line draw
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- logical and arithmetic pixel mixing
- map masking
- scissoring
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FULL SOFTWARE SUPPORT is offered for the IBM compatible XGA chipset with the following drivers available:

- DOS Application Interface (DOS AI)
- OS/2 Presentation Manager (OS/2 PM)
- Windows 3.0
- Double Byte character set

Plus a programmer's guide so you can develop your own BIOS software.

AVAILABLE NOW

Yes, the standard IBM MicroChannel Architecture-compatible XGA chipset is available right now. Just call or fax one of the SGS-THOMSON locations listed below and get details on delivery and price.

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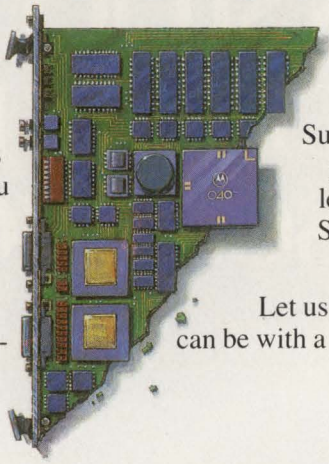
Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

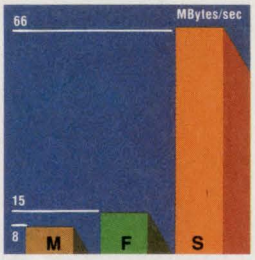
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.



Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

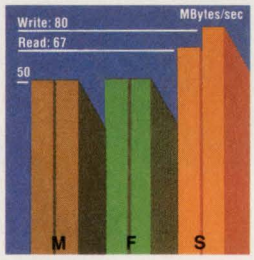
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



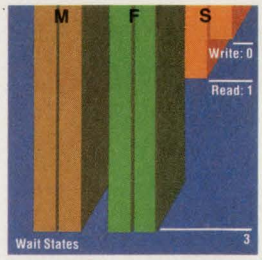
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



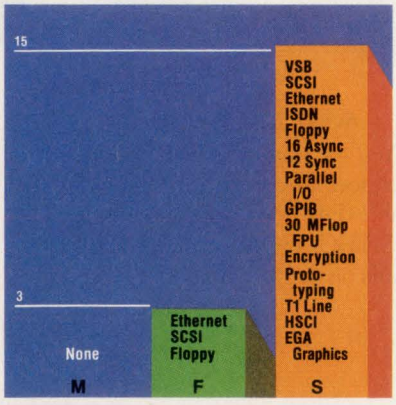
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



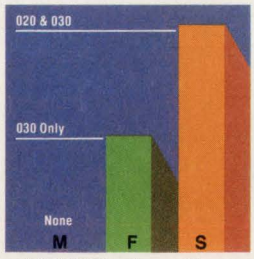
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



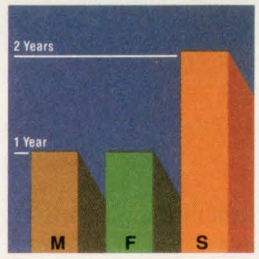
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



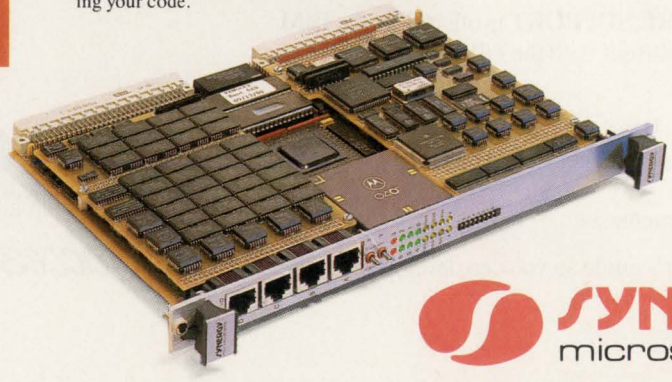
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

MCS-96 FAMILY

16-BIT NMOS AND CMOS

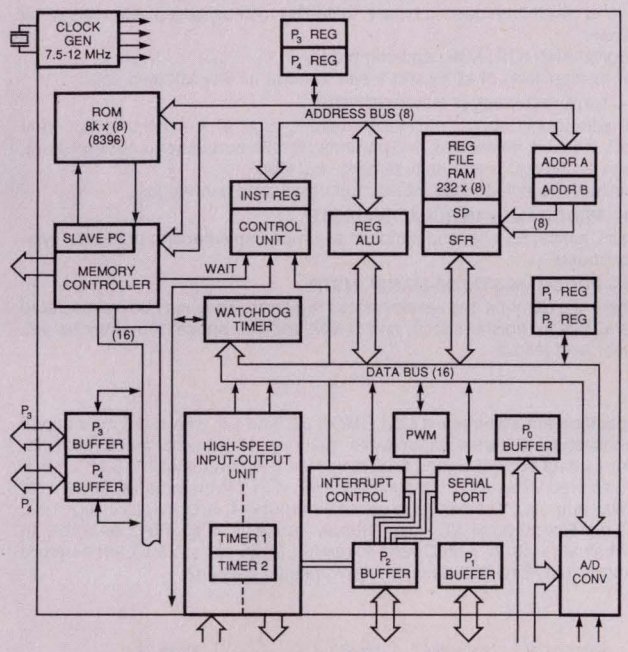
AVAILABILITY: Now for all devices.
COST: $5 to $25.
SECOND SOURCE: None.

Intel Corp
Chandler Microcontroller and ASIC Div
Phone (602) 961-8051
For more information, Circle No. 376

Description: Highly integrated, high-performance CMOS 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes as much as 16 kbytes of ROM/one-time programmable EPROM, 488 bytes of register RAM, and 256 bytes of code RAM. I/O capabilities include as much as 10 channels of high-speed I/O, ten 8-bit A/D converters, seven 8-bit I/O ports, and a watchdog timer. The KC and KR families also include a high-speed peripheral transaction server (PTS).

Status: This earliest of the 16-bit μCs continues to maintain a large share of the 16-bit market. Intel has expanded the MCS-96 family to suit various segments of the market.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide.
Logicals.
Bit, byte, word, and double-word operations.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include direct, immediate, indexed, indirect, and indirect with autoincrement.
Load and store, push and pop.

III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.

IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, and sticky bit (records previous value of carry during right shifts).
Can set and clear some bits.

Specification summary: 16-bit μC with split-memory architecture; 8-kbyte ROM or EPROM and 232 bytes of register-file RAM on 8096BH, 8097BH, and 8098; the 8097JF adds another 8 kbytes of ROM or EPROM and 255 bytes of RAM. External memory expandable to 64 kbytes with data-bus dynamically programmable as 8 or 16 bits. Register-to-register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter; four 16-bit software timers; PWM output; five 8-bit I/O ports; full-duplex serial port; and high-speed pulse I/O ports. 16×16-bit multiply as fast as 1.75 μsec and 32/16-bit divide as fast as 3 μsec. Average instruction executes in 500 to 1000 nsec.

Hardware notes:
1. The 80C196 family is available in various packaging and memory options. Among the package types are 68-lead PLCC, 64-lead shrink DIP, 80-lead QFP, and 52-lead PLCC.
2. I/O subsystem has 4 high-speed capture inputs and 6 high-speed pulse outputs. Storage in 8-deep FIFO (inputs) and content addressable memory (outputs).
3. The KR family replaces the I/O subsystem with an event processor array (EPA), a dedicated capture/compare unit with an individual register for each channel.
4. The KC and KR families include a peripheral transaction server (PTS). This server is a hardware feature that lowers interrupt overhead by intercepting and performing interrupt servicing.

HARDWARE — SUPPORT — SOFTWARE

ICE-196HX ($13,250) and ICE-196MX ($10,250) advanced emulators, as well as ICE-196PC/KB ($3500) PC-based emulator. Programming support for EPROM versions supplied through Intel's line of universal PROM programmers as well as third-party programs from companies such as Data I/O, Stag, and Elan.
Evaluation Boards: Intel offers boards for many of the devices.
From Intel: Macroassembler (ASM-96), PL/M-96, and C-96 compilers. PL/M and C compilers supply hardware-control features such as interrupts. Each software package includes relocation/linkage utility (RL-96); library-management utility (LIB-96); object-to-hex conversion utility (OH-96); and FPAL-96, a 32-bit floating-point utility. Software packages run on IBM PCs and compatible computers. $750 for a single-user license. Intel offers PC-based ACE196 expert system software (free), an interactive learning tool for the architecture. The company also offers 8051 assembly-language translators for free.

From Archimedes (San Francisco, CA): ANSI C-8096 compiler with additional features, such as control of interrupt. Hosted on IBM PC ($995), MicroVAX ($3995), and VAX ($5995).
From Cybernetic Micro Systems (San Gregorio, CA): Graphics programming and simulation aids, which run on IBM PCs ($295 and $995, respectively).

HPC16000 FAMILY

16-BIT CMOS

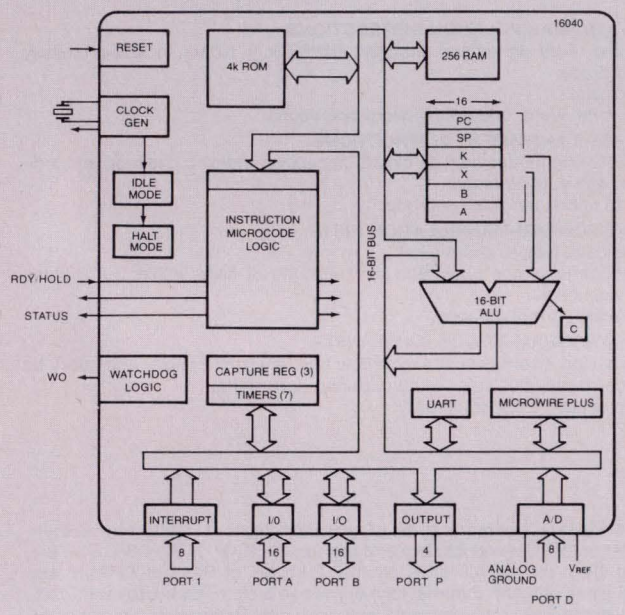
AVAILABILITY: Now for 20-, 30-, and 40-MHz parts.
COST: $5 to $25 in volume.
SECOND SOURCE: None.
CORE: The HPC family is core based. National says the family of standard parts is continually growing.

Description: Each member of the family contains the same 16-bit core. Versions are customized with unique combinations of memory, peripherals, and I/O. The newest member of the family is the 40-MHz 46100, which contains a multiply-accumulate unit and an 8-channel 8-bit ADC in an 80-pin QFP.

National Semiconductor Corp
Phone (408) 721-5000
For more information, Circle No. 377

Status: HPC is a family of industrial controllers. Supplier's benchmarks (August '86 with HPC at 17 MHz) indicate that HPCs outperform other similar 8- and 16-bit controllers, such as Intel 8096, Motorola 68HC11, and TI370 on both throughput and ROM-program efficiency. NEC 78XXX and Zilog Super Z8 weren't mentioned. Dataquest numbers show the HPC as the largest selling 16-bit CMOS μC.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results.
Logical AND, OR, XOR, and compares.
Bit manipulation of all registers and through all 64k address space.

II—DATA-MOVEMENT INSTRUCTIONS
10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip.
Instructions include load, store, push, pop, and exchange.

III—PROGRAM-MANIPULATION INSTR
Calls, jumps, returns, and conditional jumps implementing high-level-type constructs.

IV—PROGRAM-STATUS-MANIP INSTR
There is a carry-bit and several status registers. They may be manipulated as all bits in register space, and in 64k address space, they may be set, reset, and tested.

Specification summary: 16-bit CMOS μC and μP with memory-mapped architecture. External expandable memory. 16-bit-wide architecture includes data bus, ALU, and registers. Has 8 programmable 16-bit timers, 8 vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, 4 input-capture registers, 52 general-purpose I/O lines. Supply range is 4 to 5.5V. Available in industrial (−40 to +85°C) and extended (−55 to +125°C) temperature ranges (MIL-STD-883 now). In 68-pin plastic package.

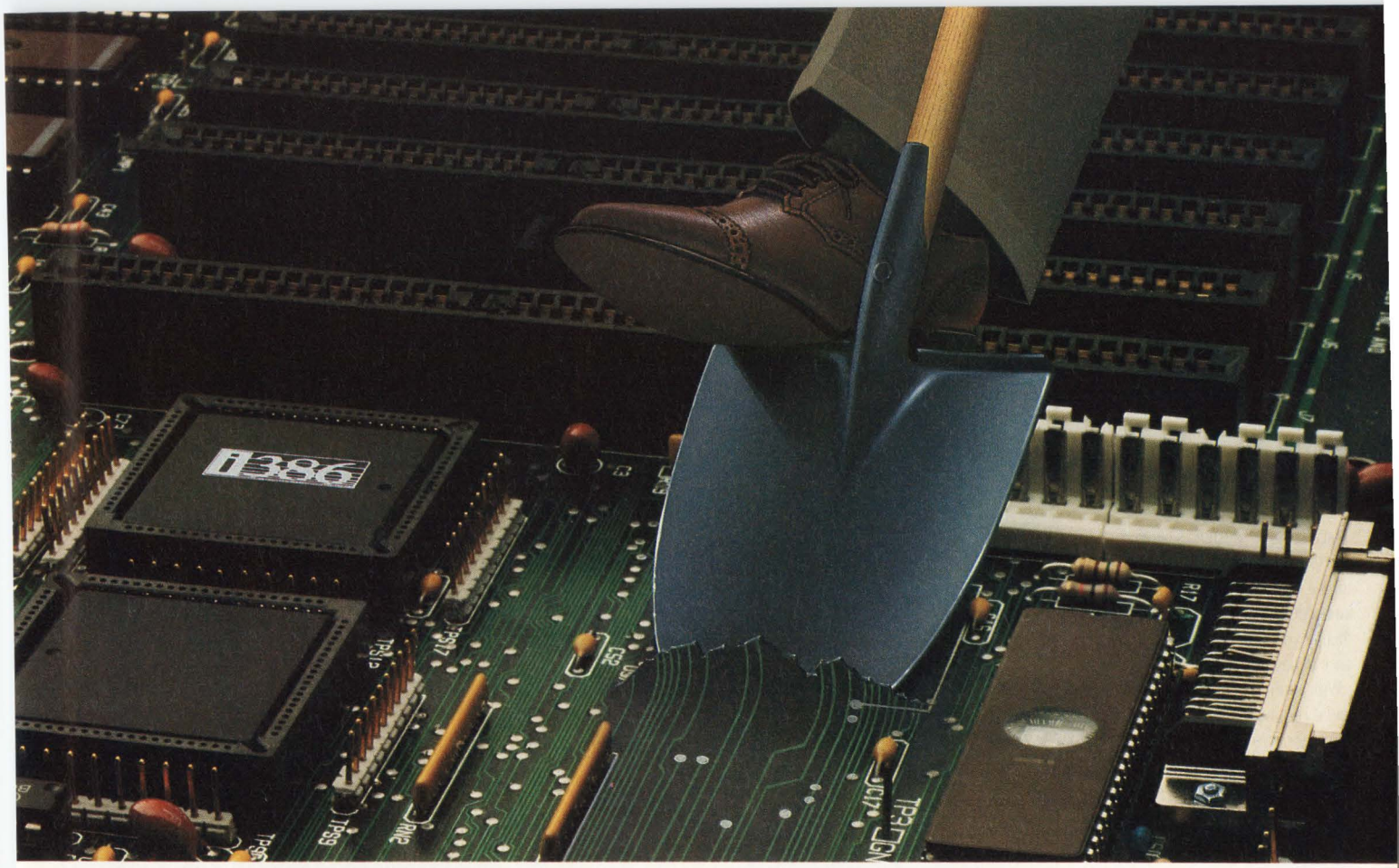
Commercial version (0 to 70°C)	Industrial version (−40 to +85°C)	ROM EPROM (bytes)	RAM (bytes)	I/O pins	Timer base counters	Other
HPC46003	HPC36003	ROMless	256	32	8	4 input capture registers
HPC46004	HPC36004	ROMless	512	32	8	4 input capture registers
HPC46064	HPC36064	16.0k	512	52	8	4 input capture registers
HPC46083	HPC36083	8.0k	256	52	8	4 input capture registers
HPC46100	HPC367064	ROMless	1k	32	7	Multiply and accumulate, 8-channel ADC
HPC46400E	HPC36400E	N/A	256	36	4	HDLC & DMA
HPC467064	HPC367064	16.0k	512	52	8	EPROM & one-time-programmable device
HPC46083MH		8.0k	256	52	8	EPROM

Hardware notes:
1. Family is designed around common μP core for instruction-set consistency, with different models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are ADCs, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPROMs.
2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (ADCs, display drivers, EEPROM), COPS 4-bit μCs, some other 8-bit μCs, and other HPCs for multiprocessing.
3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity, such as infinite loops.
4. Halt and idle modes provide additional power savings by stopping clock or disconnecting it.
5. Emulator parts are available for the HPC family.
6. HPC16083 and HPC16003 are MIL-883 and DESC-qualified.

HARDWARE — SUPPORT — SOFTWARE

A designer's kit is available for less than $500. Supplier's HPC development system costs approximately $7000 for the HPC family. A high-end development system will be available from Hewlett-Packard as part of the HPC64700 in 1990. Both development systems can be used in conjunction with various hosts like IBM PC/ATs or HP9000 Series 300s.
Dial-A-Helper is a 24-hr, on-line computer bulletin board serviced by National. It provides the latest information on all National μC chips (including development systems) and also specific application support. Call (408) 739-5582 for more information.

Cross-assembler and C compiler to run on IBM PC. VAX (Unix/VMS) support is available, as is a symbolic debugger. Floating-point math and general math packages are currently available. Extensive application software is available for ISDN and SCSI.



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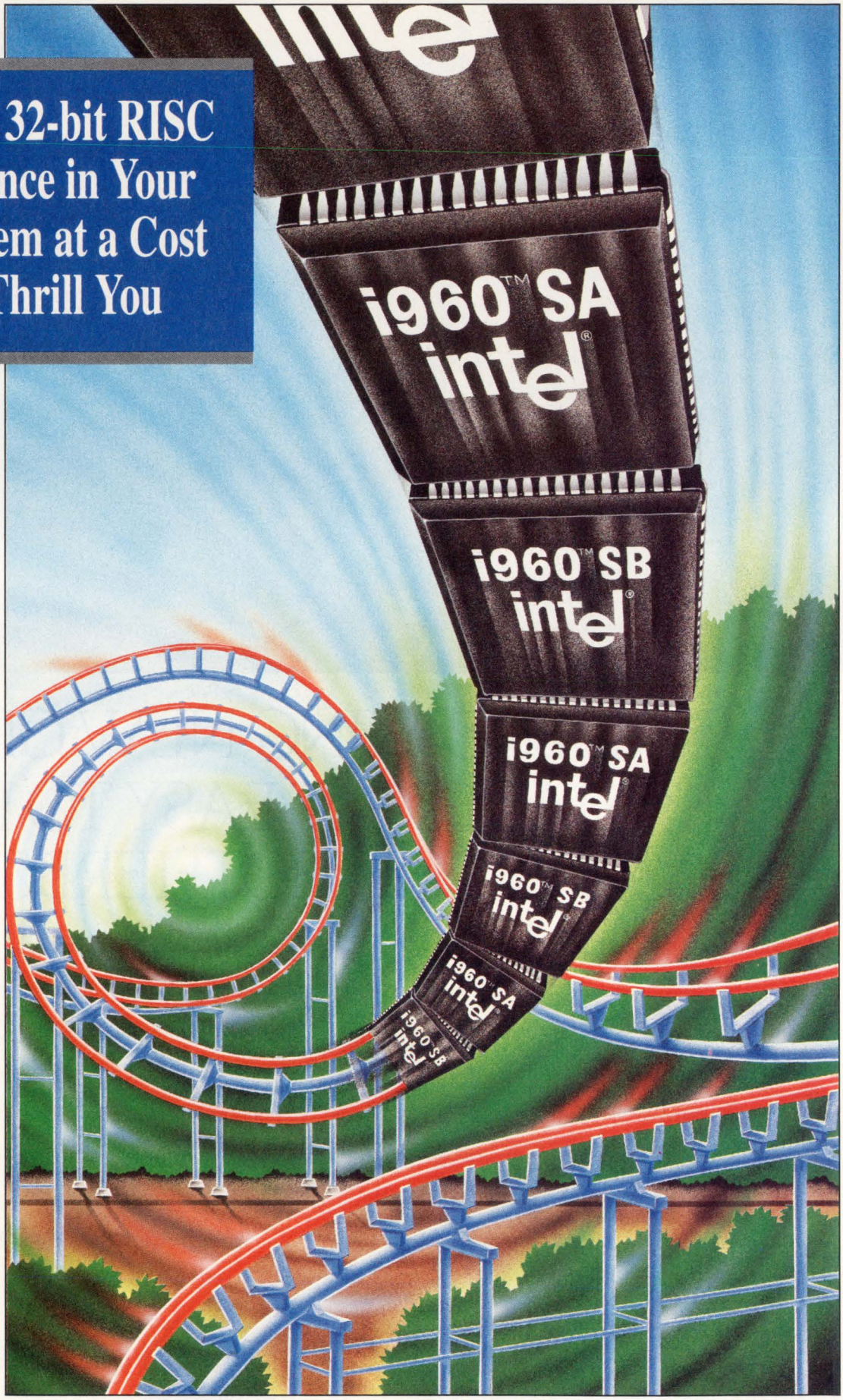

VALUE
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CIRCLE NO. 88

80C166

16-BIT CMOS

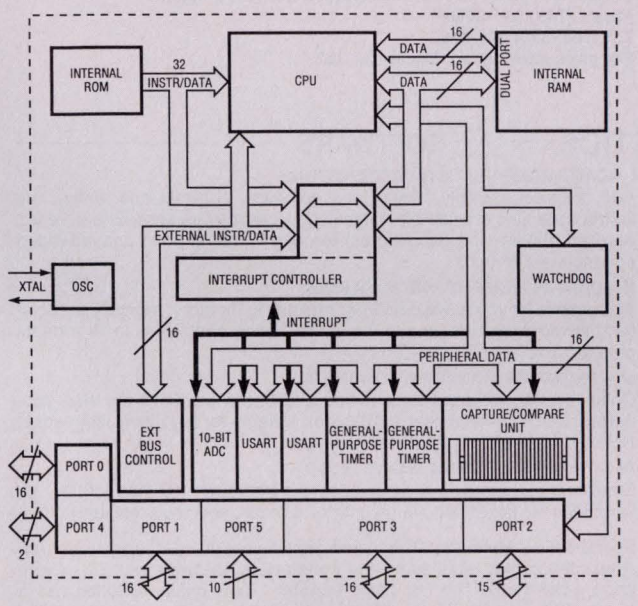
AVAILABILITY: Now.
COST: $25 (10,000)
SECOND SOURCE: SGS-Thomson.

Siemens Components Inc
Integrated Circuits Div
Phone (408) 980-4518
For more information, Circle No. 378

Description: The 80C166/83C166 is a 16-bit microcontroller for real-time applications. It uses a pipelined architecture and performs 8-, 16-, and 32-bit arithmetic and bit, byte, and word manipulations. You can freely allocate, within the internal RAM, any number of register banks with as many as 16 general-purpose registers. An interrupt controller with a peripheral-event controller provides fast response to external events.

Status: Siemens claims its 16-bit modular design works well in automotive, industrial-control, and data-communications applications. The 80C166 uses the vendor's experience with highly integrated derivatives of the 8051. Changing peripheral modules and on-chip RAM and ROM sizes to suit particular applications will help the family grow.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8-, 16-, and 32-bit signed and unsigned arithmetic instructions including fast multiply and divide. Multiple-bit shift and rotate in one machine cycle. Direct bit-to-bit manipulation in internal RAM. Various loop-control instructions.

II—DATA-MOVEMENT INSTRUCTIONS
Move instructions of byte or word in direct, immediate, indexed, and indirect with autoincrement or -decrement addressing modes. Flexible byte-to-word movements, system-stack and user-stack instructions.

III—PROGRAM-MANIPULATION INSTR
Intersegment and intrasegment calls and jumps. Conditional jumps on 16 different conditions (including semaphore support). Software traps.

IV—PROGRAM-STATUS-MANIP INSTR
You can change the current CPU priority to mask reactions on interrupts of lower priority. Hardware traps are issued on detected errors. A system-configuration register allows adjustment of the μP to various system requirements.

Specification summary: Single-chip microcontroller with external bus interface, as much as 32 kbytes of ROM or flash EPROM, and 1 kbyte of RAM. Selectable 8- or 16-bit external data bus with programmable wait states or ready function. Chip uses 40-MHz crystal to run at 20 MHz. Most instructions execute in one machine cycle (100 nsec). Interrupt response takes 3 to 5 cycles. You can allocate 32 interrupt sources to 16 priority levels. The peripheral-event controller steals cycles to implement fast, asynchronous data transmissions. The capture/compare unit consists of two 16-bit timers with 400-nsec resolution. A general-purpose timer unit contains three 16-bit up/down timer/counters with 400-nsec resolution. Another general-purpose timer unit offers two 16-bit up/down timer/counters with 200-nsec resolution. The 80C166 provides 76 I/O lines in four 16-bit bidirectional ports, one 2-bit bidirectional port, and a 10-bit input port. Two USART channels provide 625k-baud serial communication. An on-board ADC provides 10-bit resolution and 9.7-μsec conversion time.

Hardware notes:
1. The peripheral event controller services peripherals independent from the CPU. This controller module acts as an interrupt-driven DMA function between the CPU and peripherals.
2. The 80C166 is a task-oriented machine. The programmable interrupt priorities, a number of hardware and software traps, fast interrupt response time, and programmable register-bank allocation allow fast-task switches.

HARDWARE — SUPPORT — SOFTWARE

Siemens supplies an 80C166 evaluation board with monitor and an emulator based on a bond-out chip. The board uses the IBM PC as a host.
From others: Kontron supplies a full-featured emulator using the bond-out chip. Ertec supplies an EPROM emulator and an evaluation board. Several other third-party vendors support the family with hardware products.

From Siemens: A development package that includes a macro assembler, linker, locator, and library. A C compiler for ANSI standard-compatible C with additional support for 80C166-specific features. A software simulator that can simulate on-chip peripherals and an interrupt system allows debugging and software development. All software tools are IBM PC-based and are currently available.
From others: Several companies supply tools such as assemblers, compilers, and real-time operating systems. Contact the chip vendor for more information.

1750A

16/32-BIT CMOS

AVAILABILITY: Now from Allied-Signal Microelectronics Center, GEC-Plessey Semiconductors, LSI Logic, and United Technologies Microelectronics Center (UTMC).
COST: See Table
SECOND SOURCE: None. Each vendor sells its own implementation.
Core: LSI Logic offers its 64500 as a hard macro

Description: MIL-STD-1750A defines instruction-set architecture for airborne computers. The standard leaves implementation to discretion of chip vendors. Allows use and reuse of available software—though obviously hardware support is implementation dependent. Radiation-hardened and 883C class-S versions of many 1750A implementations available.

Status: Allied-Signal is in production with its 1750A-1 and -3 devices. Both are available to a total dose rate of 100,000 Rads (Si) and single-event upset of less than 4E-5 upsets/device-day in geosynchronous orbit. GEC-Plessey offers a 3-chip version available to Class S and 883C; a 1-chip implementation is sampling now. UTMC's single-chip implementation is available in either 100,000 and 1,000,000 Rads (Si) total dose. All vendors offer a memory-management unit that expands the available address space from the specified 64 kbytes to 1 Mbyte.

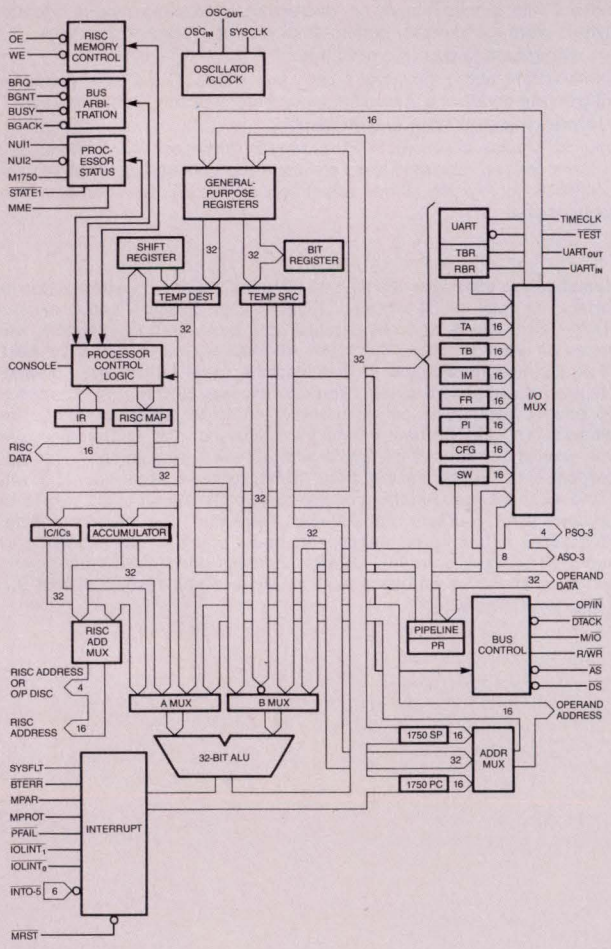
Allied-Signal Microelectronics Center
Phone (301) 964-4047
For more information, Circle No. 379

GEC-Plessey Semiconductors
Phone (516) 293-8686
FAX (516) 293-0061
For more information, Circle No. 380

LSI Logic
Phone (408) 433-7557
FAX (408) 433-7447
For more information, Circle No. 381

United Technologies Microelectronics Center (UTMC)
Phone (719) 594-8000)
Toll free (800) 645-8862
For more information, Circle No. 382

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS

Add, subtract, multiply, divide, and compare. Logicals and shifts. The instructions also provide bit-manipulation capabilities such as set, reset, and test. Single- and double-precision fixed floating-point and extended floating-point formats.

II—DATA-MOVEMENT INSTRUCTIONS

Instructions let you move data from register to memory, memory to register, between registers, and to the stack. Loads and stores in all formats plus test and set-bit operations.

III—PROGRAM-MANIPULATION INSTR

Conditional and unconditional jumps and branches. Calls are also supported. Stack management instructions suitable for high-level languages. Handles 16 levels of prioritized interrupts.

IV—PROGRAM-STATUS-MANIP INSTR

Emulation-mode status register accessible through I/O instructions. Instructions for accessing status, interrupt-mask, and fault registers.

Specification summary: The Allied-Signal version is a single-chip implementation that includes timers, counters, a hardware multiply, and a floating-point unit. The LSI Logic L64500 1750A implementation has a 16-bit CPU, expandable to 32 bits depending on the operation. The L64550 includes MMU with memory expansion to 1M words, block-protect unit, memory-fault status register, bus-arbitration unit with 6 bus masters, start-up ROM interface, I/O port, trigger-go counter, and other options. GEC-Plessey's MAS281 is a radiation-hardened 3-chip silicon-on-sapphire (SOS) module. The MAS31750 is a single-chip SOS version.

Hardware notes: 1. Diagram is for the UTMC 1750AR. Functions as a stand-alone RISC processor providing 8 MIPS at 16 MHz. In the 1750A operation mode, a throughput of 750 kIPS at 16 MHz is achieved using the DAIS mix. 2. GEC-Plessey's implementations are radiation hardened and offer full performance over the military temperature range. The MAS281 3-chip version achieves 700 kIPS DAIS throughput at 20 MHz where the MAS1750 1-chip version reaches 3 MIPS DAIS at 22 MHz.

Representative 1750A microprocessors

Part number	Vendor	Technology	Price (883C)	Price (class S)
BX1750A	Allied Signal Microelectronics	CMOS	$750 (100)	Dependent on requirements
L64500	LSI Logic	CMOS	$1334 (1000)	$4406 (1000)
MAS281	Marconi	CMOS/SOS	$1400 (1000)	$8000 (20)
MAS31750	Marconi	CMOS/SOS	$2000 (1000)	$10,000 (20)
1750AR	United Technologies Microelectronics	CMOS on EPI	$565 (1000)	$1976 (100)

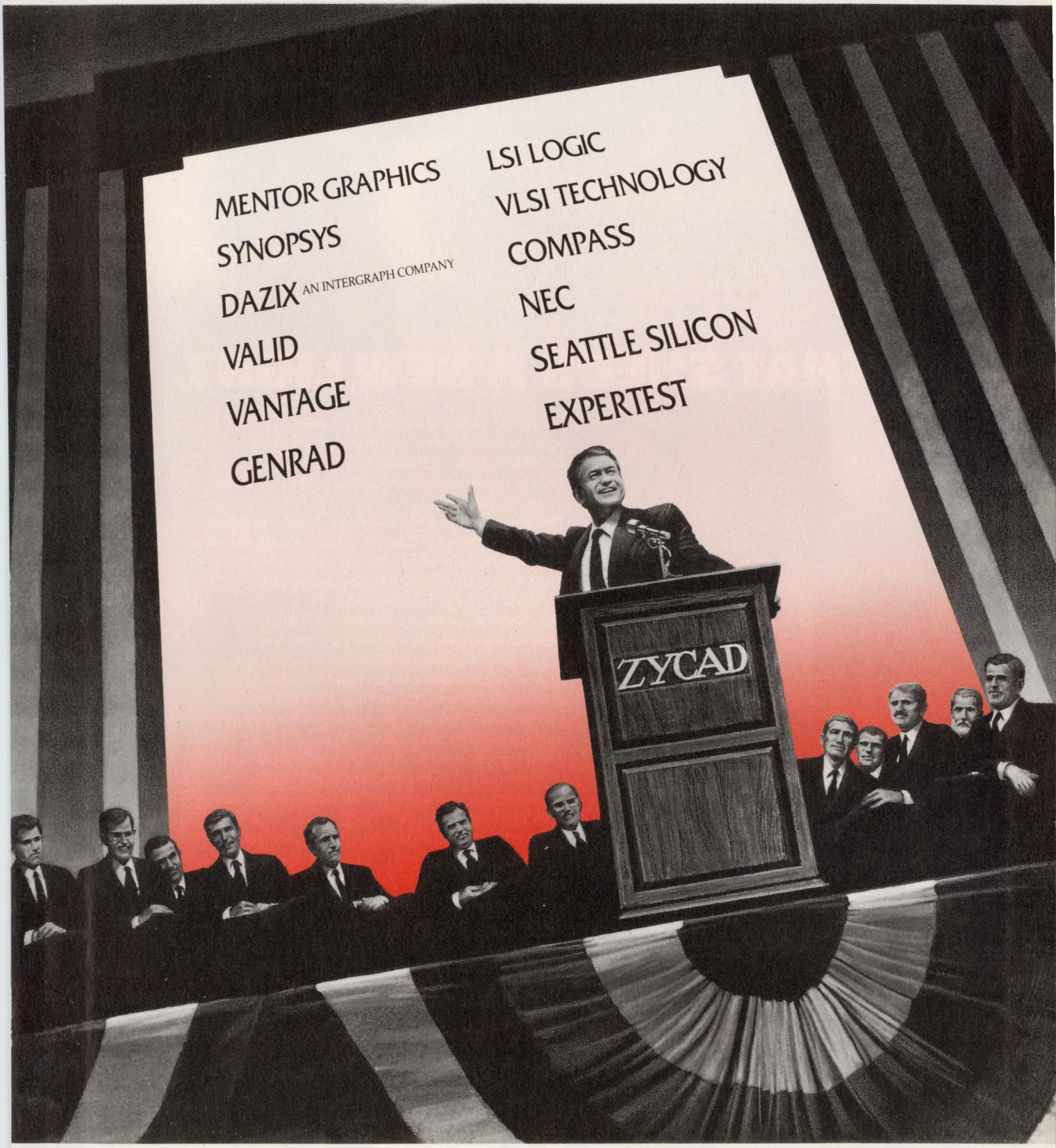
HARDWARE — SUPPORT — SOFTWARE

Allied-Signal Microelectronics Center offers a development system for the A-S BX1750A that converts an IBM PC into a real-time, mappable monitor/debugger. GEC-Plessey's devices are supported by emulators from Tasco (Anaheim, CA), HP (Palo Alto, CA), and Tektronix (Wood bridge, NJ). Tasco also offers a single-board computer and has an ICE pod for the HP 64000 development system. Call any of the IC vendors for contact phone numbers or availability of other tools.
Evaluation Boards: GEC-Plessey offers a board for its 3-chip μP; a similar board for the single-chip version is under development.

Assemblers and compilers in C and Ada are available from several outside sources. Mikros Systems offers high-level debug software for its single-board computer/IBM PC system.
UTMC offers a software package to aid in the development and debugging of system software and hardware. The software tool kit consists of a RISC or 1750 monitor, along with an interactive RISC simulator.

Text continued on pg 149

Who's Behind The Simulation Acceleration Movement?



And Who's Leading It?

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TRANSPUTER FAMILY

16/32/64-BIT CMOS

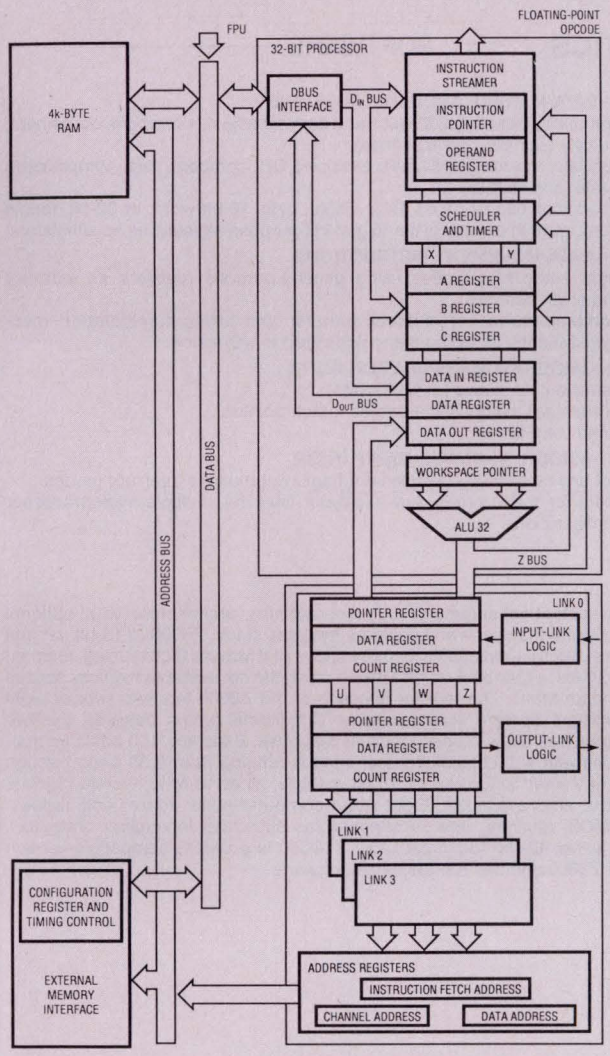
AVAILABILITY: Now for all devices except the T9000, which should ship in the first quarter of 1992.
COST: In 1000 qty PGAs: T222, $32; T22, $31; T400, $50; T425, $93; T801, $248; T805, $150.
SECOND SOURCE: None.

Description: The Transputer family is a range of software-compatible 16- and 32-bit μPs. T2, T4, and T8 Transputers have a CPU, on-chip SRAM (2 or 4 kbits), timers, external memory interface, and 2 or 4 serial links. The links are 20-Mbps DMA channels into the Transputer memory system and allow software processes running on independent Transputers to communicate directly. T8xx devices have an on-chip 64-bit FPU. The T9 has a 32-bit CPU, a 64-bit FPU, 16 kbytes of cache memory, a communications processor, and four 100-Mbps serial links.

Inmos
a member of the SGS-Thomson Microelectronics Group
Phone (214) 466-8844
FAX (214) 466-7352
For more information, Circle No. 383

Status: Volume buildup has been slow. One possible explanation is that most of the applications have been for multiprocessor configurations (typically 4 to 10 Transputers), so designers have been engrossed by the challenge of developing practical parallelism. According to market researcher Dataquest (July 1990), the Transputer has the largest number of design wins in Europe.

HARDWARE CHARACTERISTICS



I—DATA-MANIPULATION INSTRUCTIONS
Integer arithmetic, including multiply and divide. Logicals, shifts, and comparisons. T8 has on-chip IEEE floating-point add and subtract, multiply and divide, and square root, both 32 and 64 bits.

II—DATA-MOVEMENT INSTRUCTIONS
Memory-bandwidth block moves for graphics bitblt. Load/store of local variables done relative to workspace pointer. Indexed load/stores available from address in A register. Immediate loads done 4 bits at a time. Large immediate values loadable from tables, instruction stream, or a sequence of special instructions.

III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional jumps. Procedure call and return. Subroutine call and return. Computed jumps. Process (task) creation and deletion. 2-level priority and time-sliced scheduling with message passing and time events using built-in hardware. One level of interrupt.

IV—PROGRAM-STATUS-MANIP INSTR
Error flag detects overflow. Test, set, clear, stop-on-error instructions. One error flag per task priority level. Instructions for checking array bounds.

Specification summary: Family of 16- and 32-bit μPs designed for multiprocessing. Unique in that they have the hardware and software links that allow them to be hooked to each other for parallel processing. Four full-duplex, 20-Mbps serial links driven by on-chip, 8-channel DMA provide basic multiprocessor communication links as well as I/O. On-chip PLL multiplies 5-MHz external clock to generate chip clocks. Submicrosecond interrupt latency, procedure call, and task switch. Most instructions take 1 or 2 cycles. Integer multiply takes 38 cycles; divide takes 39 cycles (less than 2 μsec). Single-precision floating-point add takes 7 cycles (350 nsec), floating-point multiply takes 11 to 18 cycles (550 to 900 nsec), and floating-point divide takes 16 to 28 cycles (800 to 1400 nsec).

Hardware notes: 1. Diagram is for T425. T805 adds an FPU. T801 is the same as the T800 except that the external memory interface is a nonmultiplexed data/address bus instead of the T800 multiplexed bus. T222 has a 16-bit internal architecture and no FPU. The T400 is a low-cost variant with two links and 2 kbytes of on-chip memory. The T9000 offers a 32-bit CPU, a 64-bit FPU, and 16 kbytes of cache memory.
2. Unlike most 32-bit machines, there is no group of general-purpose registers. Instead, substantial on-chip RAM plays an equivalent role on the T2/T4/T8. The T9000 has a 32-word workspace cache for fast access to frequently used data.
3. ALU fed from 3 accumulators forming a small 3-deep stack, allowing compact implied addressing.
4. The four serial links allow arrays of Transputers in multiprocessing systems with no bus saturation, which is the reason speed increase is said to be linear when more μPs are added.

Software notes:
1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack.
2. Two priority-ordered process queues are each supported by front and back registers, indicating a linked list of processes ready to run. Event-based multitasking is fully supported by a real-time kernel in microcode.
3. Compilers for ANSI C, C++, Fortran, and Ada are available. Supplier's Occam language said to facilitate programming multiple Transputer systems, but programmer must still study how best to partition task. Third parties have announced extensions to C to accomplish same ends.

HARDWARE SUPPORT

Inmos offers mother-board-based development systems for the IBM and NEC PCs, Sun-3 and Sun-4, and DEC/VAX hosts. Each mother board can accommodate Transputer Modules (TRAMs), which contain Transputer, memory, and specialized functions. You can build multiprocessor systems by plugging multiple TRAMs into the mother board. Software controls the configuration. Third parties support the modules, which have industry standard pinouts. Memory sizes range from 32 kbytes to 8 Mbytes.
Evaluation Boards: Inmos supplies evaluation boards for Transputers and Transputer modules using PCs and Sun-3, Sun-4, and 386i hosts.

SOFTWARE SUPPORT

Inmos supplies compilers for hosts such as IBM and NEC PCs, PS/2, VAX (VMS), and Sun systems. ANSI C, C++, Fortran, Ada, and Occam are the languages that Inmos supports. Available software-debugging tools include network debugger, breakpoint, and trace facilities. Third-party vendors support operating systems such as Chorus, Helios, Linda, and Transidris and real-time kernels VRTX and C-Executive.

Z8000/Z16C00

16/32-BIT NMOS AND CMOS

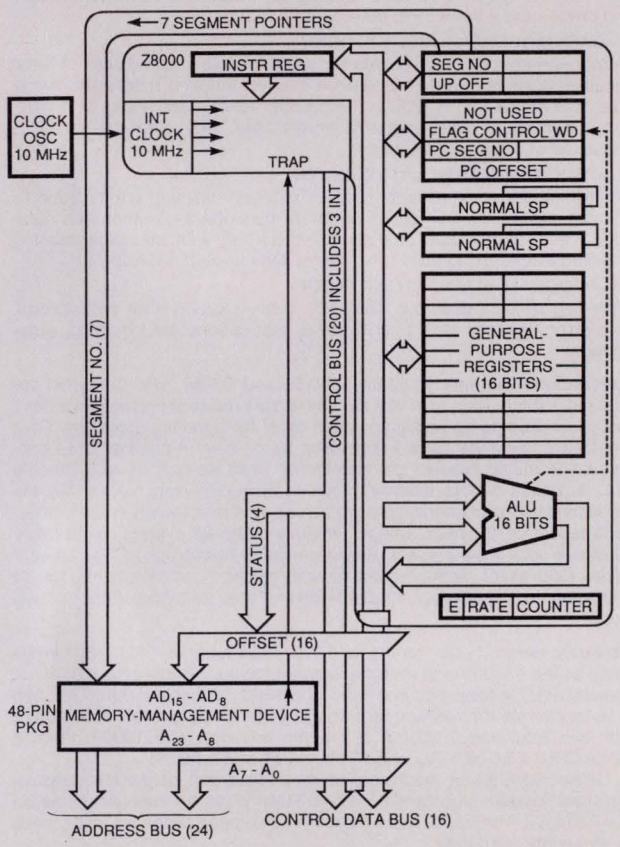
AVAILABILITY: Now for 6- and 10-MHz NMOS Z8000 and for 10- and 16-MHz CMOS Z16C00.
COST: $4.20 (10k) for Z8000 in PLCC package.
SECOND SOURCE: SGS-Thomson, and Sharp for Z8000.
CORE: Zilog has both Z8000 and Z16C00 as cores in its in-house ASIC library and plans to use Zbus for its systems on silicon. The company says that 160×160-mil Z8000 core is small enough to leave room for other functions on practical 400×400-mil ASIC.

Zilog Inc
Phone (408) 370-8000
For more information, Circle No. 384

Description: One of the first μPs to have architectural features of a modern minicomputer. Original 16-bit Z8000 comes in 40-pin package for addressing 64-kbyte memory or in 48-pin package for addressing 8-Mbyte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit μP, offering best CPU speed, interrupt handling, character-string search, and block moves.

Status: The Z8000 has found most acceptance in real-time control applications, particularly military, according to Zilog. The company has added the Z16C00 16-bit CMOS microcomputer to the family for real-time embedded control applications. The company is licensing its 16-bit core for customer applications.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed).
Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n).
Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulators.

II—DATA-MOVEMENT INSTRUCTIONS
Eight addressing modes using general-purpose registers as indexers and stack pointers.
Comprehensive set of block-transfer and string-manipulation macroequivalents, including many dedicated to I/O space.

III—PROGRAM-MANIPULATION INSTR
Call and call relative (±4096 bytes).
System call using special system-stack pointer.
Jump conditionals.

IV—PROGRAM-STATUS-MANIP INSTR
Set and reset flags, complement flags. Set-multiple-interrupt modes.
Tests for the micro-in and micro-out lines for multiple-microprocessor configurations.

Specification summary: Common-memory architecture with optional separate I/O space and separate systems stack. Z8000 is 16-bit μP that has directly addressable memory space of 8 Mbytes (8001) using segment pointers, expandable to 48 Mbytes using the six available memory spaces and an MMU. The register handling of the Z8000 lets two sets of eight registers operate simultaneously. Conditional jumps between the two processes allow 2-μsec interrupt response. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 μsec through 1 or 2 μsec to 7 μsec for 16-bit multiply, all at 10-MHz system clock (6 MHz also available). Eight large-computer-style addressing modes. NMOS, requiring one 5V supply (plus substrate-decoupling capacitor), in either 40- or 48-pin package. Z16C00 is a CMOS-compatible version of Z8000 and can run the same software.

Hardware notes: Supplier has companion peripherals suitable for both processors: For Z8000, a range of DMA, FIFO, data ciphering (NBS), communications, and counter/timer parts.
For Z16C00, a system general-logic unit—16C20—contains memory support, DMA, interrupts, and I/O. For 16C01, a CMOS dual MMU80210 addresses 128 segments compatible with the 8010 NMOS MMU.

HARDWARE SUPPORT SOFTWARE

From Zilog: Z16C00 development board ($250). 500-pg Z8000 technical manual.
From others: Tools available from Applied Micro, Boston Systems, Kontron, Orion, 2500 AD, and Microtec. Contact supplier for addresses.

From Zilog: Real-time application software (IBM PC based). C compilers and cross-assemblers. Contact supplier for names and addresses of software-support vendors.

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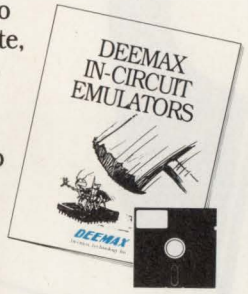

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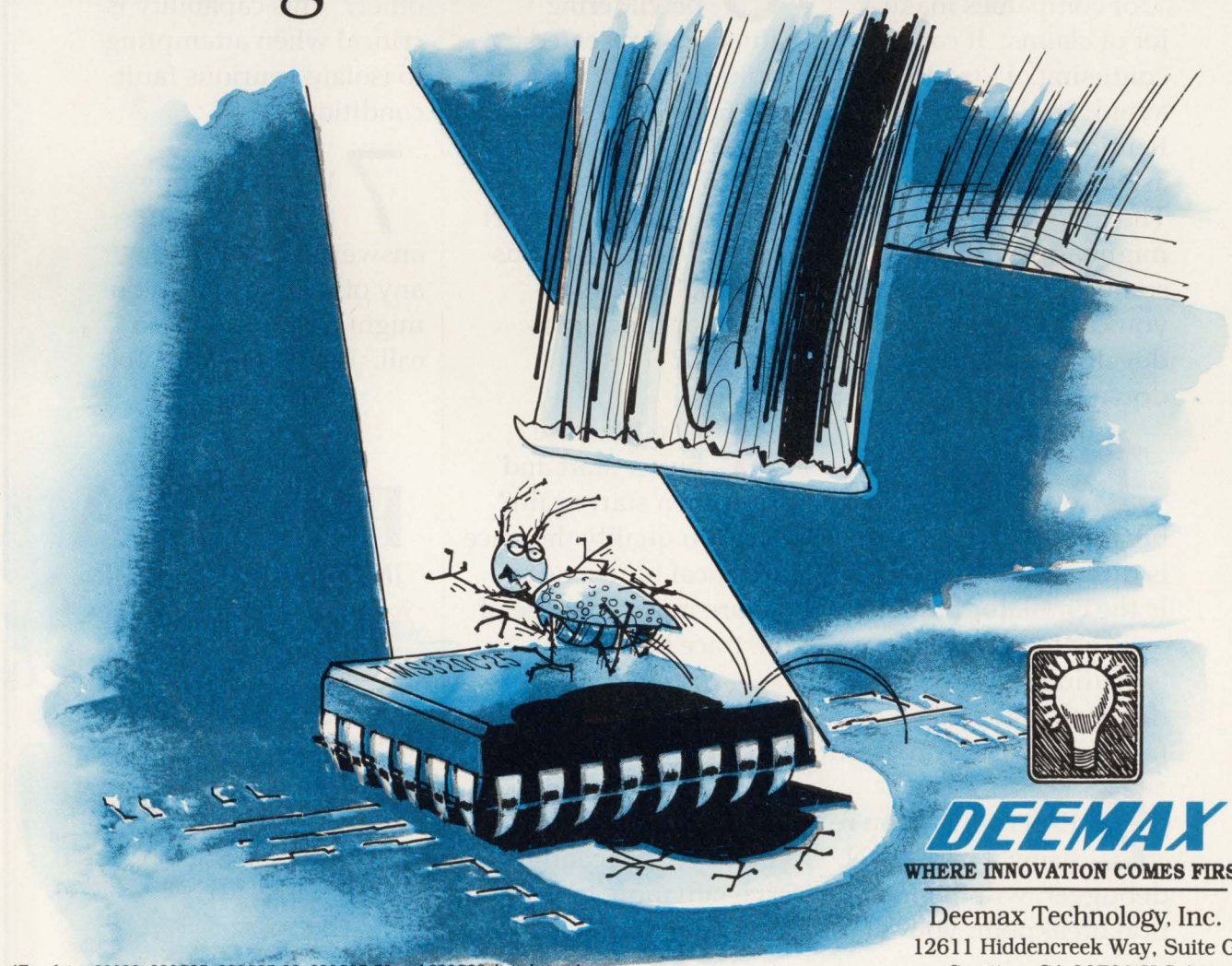

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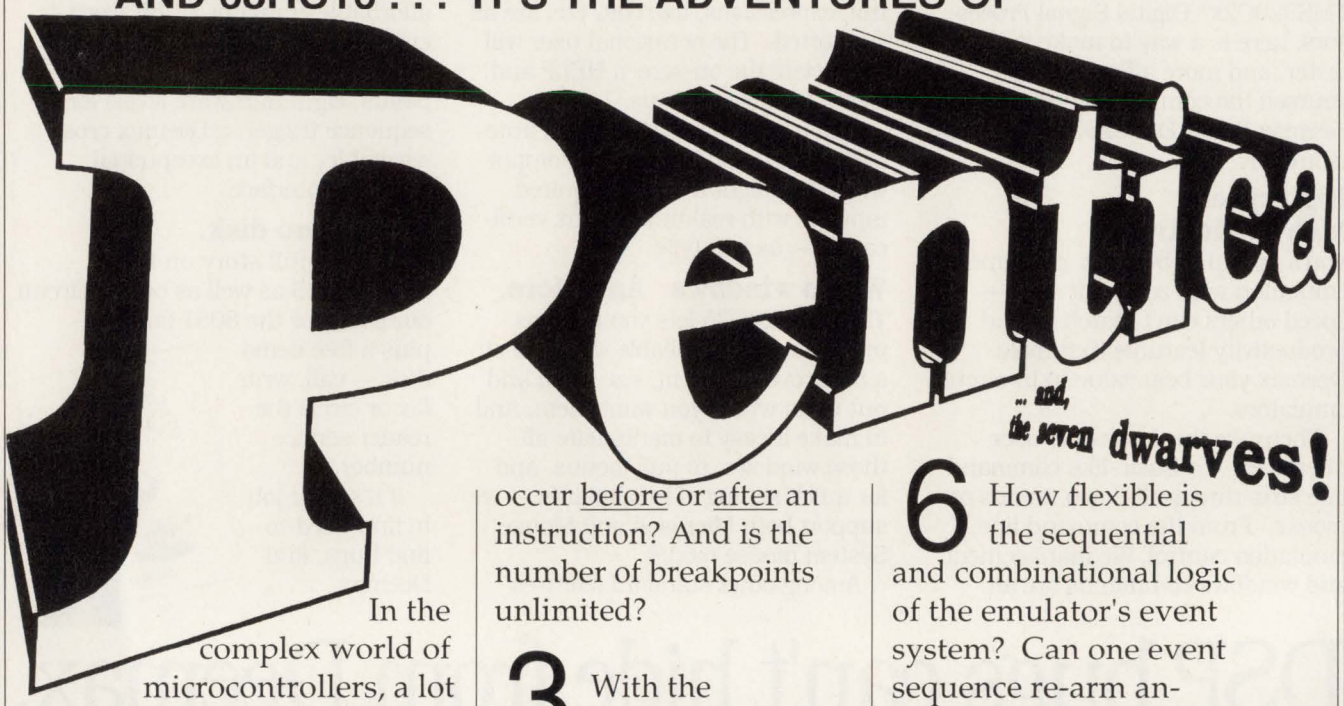
CIRCLE NO. 90

FOR EMULATING THE MOTOROLA 68302, 68332*, AND 68HC16 . . . IT'S THE ADVENTURES OF



In the complex world of microcontrollers, a lot of companies make a lot of claims. It can be confusing. How do you avoid a poisoned apple? Pentica suggests that you ask a few basic questions. The following seven might appear gigantic to some, but we can help you cut them (and your development problems) down to size.

1 Setting a true execution breakpoint on the 68302 is difficult but necessary. Is the emulator precise enough to break only on execution of instruction rather than when it's fetched from the program?

2 Especially if you're using a high-level debugger, will the execution breakpoint you set occur before or after an instruction? And is the number of breakpoints unlimited?

3 With the bewildering situations presented by multi-use pins, the 68332 and 68HC16 challenge an emulator to be nearly clairvoyant. For instance, when using port E as I/O instead of bus control, how much emulator function is retained?

4 Can the trace buffer start and stop...then start again? Can you qualify the trace to critical functions to ensure maximum use of the trace buffer?

5 Is the emulator's event system independent of the breakpoints? Or do you have to reconfigure each situation, losing flexibility?

6 How flexible is the sequential and combinational logic of the emulator's event system? Can one event sequence re-arm another? This capability is critical when attempting to isolate spurious fault conditions.

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*Support for the 68332 will be available Q2 1992.

340X0 GRAPHICS μP FAMILY

32-BIT CMOS

AVAILABILITY: Now for 34010 and 34020 CPUs and the 32-MHz 34082 floating-point unit. Engineering samples of the 40-MHz 34082 are available now.
COST: The 34010 costs $23 (10k), the 34020 costs $89 (10k), and the 34082 floating-point unit costs $125 for 32-MHz parts and $350 for 40-MHz samples.
SECOND SOURCE: Under active consideration.

Texas Instruments Inc
Application Specific Products Div
Phone (713) 274-2340
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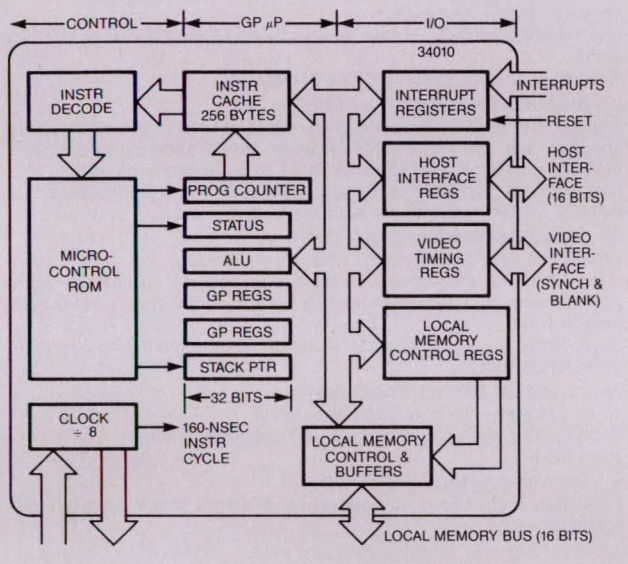
Description: This 32-bit CMOS μP family is optimized for graphics-display systems. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular μP instructions, it has specialized instructions for pixel manipulation. 1-Gbyte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits). The 34010 has a multiplexed, external 16-bit address/data bus; the 34020 is a full 32-bit machine. The 34020 is upwardly object-code compatible with the 34010 and features additional graphics-specific instructions. The 34082 is a graphics floating-point coprocessor for the 34020.

Status: Despite this μP family's specialized slant toward CRT graphics, it does have a general-purpose Von Neumann architecture and instruction set. Also, some of its attributes can be equally applied to other, nongraphics applications. In particular, the μP can do rapid bit manipulation of a large local-address field. A number of IBM PC-based board-level products incorporate this part. X-Window terminals are an example of an application in which this family's graphics and general-purpose capabilities are utilized. One nongraphic area users are exploring is industrial control. In this area, the 340X0's bit manipulation and low cost relative to other 32-bit μPs are attractive, according to TI (even for consumer-oriented uses such as arcade games).

HARDWARE CHARACTERISTICS SOFTWARE



Hardware notes:
1. Diagram represents 34010.
2. Added graphics features are embodied in the second 16×32-bit register file and among 28 16-bit I/O control registers. They allow programmable pixel and pixel-array processing for both monochrome and color systems of variable pixel sizes. Hardware incorporates 2-operand raster operations with Boolean and arithmetic operations, x-y addressing, window clipping, window pick operations, 1- to n-bit/pixel transforms, transparency, and plane masking.

I—DATA-MANIPULATION INSTRUCTIONS
General-purpose μP instructions: add and subtract, multiply and divide, rotate and shift, compare and logicals.
Special graphics instructions: add, subtract, and comparisons relating to x-y coordinates.

II—DATA-MOVEMENT INSTRUCTIONS
General purpose: move byte, move field, move register.
Special graphics instructions: move x half of register, move y half of register, pixel transfer, pixel block transfer.

III—PROGRAM-MANIPULATION INSTR
Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt.

IV—PROGRAM STATUS-MANIP INSTR
Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions.

Specification summary: 32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16×32-bit register files, hardware stack pointer, and 256-byte instruction cache. One of the 16-word register files contains a stack pointer and 15 general-purpose registers (the equivalent of the general-purpose registers found in nonspecialized μPs). Addressing modes of these registers are tuned to support high-level languages. Other register file is dedicated to CRT control as described in hardware note. Has 32-bit-wide address-data bus to support 1 Gbyte of off-chip local-memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A microcoded local-memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host μP. Fabricated in 5V CMOS and packaged in 68-pin PLCC. The 34020 is compatible with the 34010, but provides a 512-byte cache and supports 1-Mbit video-RAM chips.

HARDWARE SUPPORT SOFTWARE

From TI: TMS34010 software development board ($1495), which plugs into IBM PC or compatible. Used for evaluation, familiarization, and software development, and comes with user interface and debugger software. TMS34010 XDS/22 emulator box ($14,995) operates as a stand-alone unit with nonintelligent terminal or with IBM PC or compatible as host. The TMS34020 software development board and hardware emulator system provide the same development functions for the 34020. The 34082 SRAM upgrade kit ($995) is a business-card-sized daughter board that includes an 34082 and four 32 kbyte×8-bit SRAMs and installs directly into the pinout of the stand-alone 34082.
From others: Board-level and other hardware support now available from numerous sources. See TI's *TMS 34010 3rd-Party Guide* (call (800) 232-3200, ext 701, and ask for literature No. SPVB066C).

From TI: TMS34010 code-generation tools include assembler, linker, and compiler for IBM PC, VAX, Apollo, and Sun-3 and Sun-4 ($1250 to $5000). Texas Instruments has developed TIGA-340, a standard software interface for the TMS340 family of graphics processors. Development tools for TIGA (Texas Instruments Graphics Architecture) include a $340 driver developer's kit, which helps software developers make existing software run on TIGA-compatible 34010 boards; a $1500 software developer's kit for those who want to develop direct 34010 code or custom downloadable extensions to TIGA, includes a 34010 C compiler, an assembler, bit-map font and math/graphics source-code libraries; and a $15,000 software-porting kit for hardware developers to make 34010-based systems TIGA compatible. The 34082 Software Tool Kit ($1495) includes an optimizing C compiler, a macroassembler, a linker, an object code librarian, and a functional simulator. A 3-D graphics library costs $1395.
From others: See the TI TMS 34010 Third-Party Guide.

68000 FAMILY — 8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

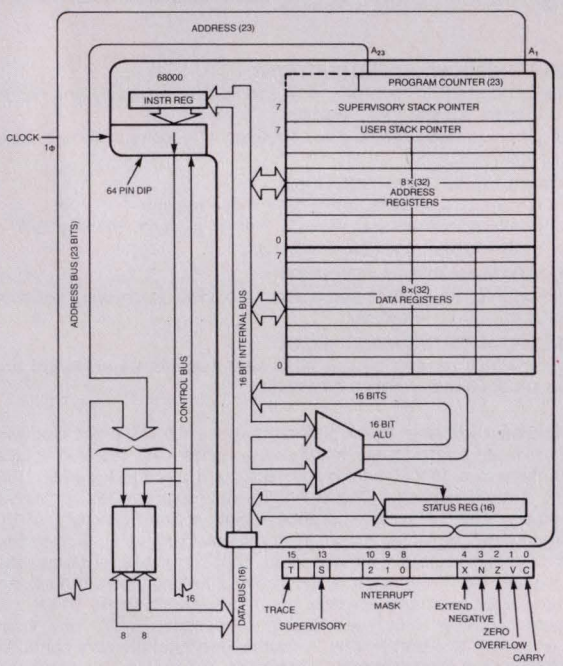
AVAILABILITY: Now for 68EC000 at 8 MHz, 68EC020 to 25 MHz, 68EC030 to 40 MHz, 68000 to 12 MHz, 68HC000 to 16 MHz, 68HC001 to 16 MHz, 68020 to 33 MHz, 68030 to 50 MHz, and 68040 at 25 MHz. The 20- and 25-MHz 68EC040 is currently sampling and should go into production by early 92.
COST: In 10,000 qty, prices for 68EC0X0 devices range from $2.95 for 8-MHz 68EC000 to $140 for 20-MHz 68EC040. The 68000 family, in similar quantities range from $4.10 for an 8-MHz 68000 to $495 for a 25-MHz 68040. Also in 10,000 qty, the 68300 family ranges from about $17 to $30 for 16.7-MHz parts.
SECOND SOURCE: Hitachi, SGS-Thomson, and Signetics/Philips all licensed with mask interchange for 16-bit parts. No second sources for 68020, 68030, or 68040 or any of the derivative families (68300 or 68EC0X0).
CORE: Motorola is using core with a mix of peripheral functions and glue logic in its 68300 family for embedded control. Signetics/Philips has the 68000 core in its ASIC library.

Description: 68000 architecture combines flexible 32-bit register set and large linear address space with powerful instruction set and flexible addressing modes. The 68040 is a full 68000-compatible μP containing an integer unit, floating-point unit (FPU), MMU, and instruction and data caches. The 680x0 family will get a boost from its 68300 derivatives in embedded control. 68300 family based on 68000 core and is software compatible. The 68EC0X0 family includes lower-cost versions of the 680x0 designs aimed at maintaining Motorola's strength in embedded control in the face of increased competition from RISC-based alternatives.

Motorola Microprocessor Products Group
Phone (512) 891-2000
For more information, Circle No. 386

Status: The success of the 68000 family is largely due to the Apple Macintosh II and the family's popularity in Unix-based workstations. Additionally, the family has enjoyed great success in midrange embedded control applications, which are typically higher volume but lower visibility than workstations. As workstations shift toward RISC-based CPUs, Motorola has adapted well by strengthening the family's focus in embedded control. Both the 68300 family and the 68EC0X0 family result from this focus.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes: 1. Diagram of basic 16-bit 68000. Family offers growth path from 8- to 16- to 32-bit μPs. Performance results from multiple ALUs, 32-bit internal operation, and nonmultiplexed address and data buses.
2. Because the EC000 and EC020 removed some signals, these devices are not pin compatible with the 68000 and 68020. The low-end EC μPs use a 2-wire-bus arbitration scheme rather than the 3-wire scheme of their predecessors. The EC000 also eliminates the synchronous 6800-style interface signals, but adds four supply pins for greater noise immunity. The EC020 reduced the address width to 24 bits and eliminated four control signals (ECS, OCS, DBEN, and IPEND).
3. Both the EC030 and EC040 are pin compatible with the 030 and 040. Although the EC040 will not contain either the memory management unit (MMU) or the floating point unit (FPU) of the 040, the 68EC030 is simply a 68030 with a disabled MMU. Presumably, Motorola will redesign the EC030 and remove the MMU in the future.
4. Signetics/Philips 68070 includes 68000 CPU, two DMA channels, counter/timers, and an IC bus interface.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply and divide (signed and unsigned).
Logicals, rotates, and shifts.
Can handle bits, BCD nibbles, bytes, short (16 bits) and long (32 bits) words.
Floating-point coprocessors 68881/2 available.

II—DATA-MOVEMENT INSTRUCTIONS
Five basic address modes are register direct, register indirect, immediate, absolute, and program-counter relative. Postincrementing, predecrementing, offsetting, and indexing can be added to these models.
Can use eight 32-bit address registers as indexes or stack pointers. The eight 32-bit data registers can also serve as indexes.

III—PROGRAM-MANIPULATION INSTR
Branch and jump to subroutine. Branch conditionally.
Link and unlink instructions invoking one address register as frame pointer (used to establish temporary local environments in structured programming).
Seven levels of priority interrupts, including nonmaskable, with 256 possible interrupt vectors.

IV—PROGRAM-STATUS-MANIP INSTR
16-bit status register is software accessible.
Sophisticated trap operations help user debug programs.
Trace mode.

V—SYSTEM-CONTROL INSTRUCTIONS
Privileged instructions for operating systems and multiprocessor communication.

Specification summary: 68040 is the highest-performance 68000 family member. This device is a 32-bit CMOS virtual-memory μP with multiple concurrent execution units. You can access the 4-way set-associative 4-kbyte instruction and data caches simultaneously. The caches are organized in 64 sets of four 16-byte lines. The autonomous nature of the caches allows instruction-stream fetches, data-stream access, and third external access to occur during instruction execution. The 68040's parallelism allows multiple instructions that don't require external accesses to execute concurrently while the processor executes an external access for a previous instruction. The 68040 provides multimaster and multiprocessor support. Additionally, the processor can snoop the external bus during accesses by other bus masters to maintain coherency between the 68040 caches and external memory systems.

HARDWARE — SUPPORT — SOFTWARE

HDS-300 hardware/software development station ($15,000 to $20,000) provides real-time emulation of 68000-family μPs with bus-state-analyzer support and source-level debugging. MEX68KECB educational computer board is based on 68000. VM04 is a 68020-based 32-bit Versamodule interconnected within a target system using the 32-bit, asynchronous, Versabus interconnect standard. VME130 is a 68020-based, 32-bit VMEbus module using Eurocard mechanical format.
From third parties: Family widely supported by makers of universal μP development systems. Also, VMEbus system architecture is used in a range of applications with more than 150 independent suppliers of compatible products.

VersaDOS real-time operating system, system V/68 OS, CP/M-68K OS, concurrent DOS-68K OS, and VRTX real-time OS ($6775 from Hunter Systems). Unix support from Motorola includes direct ports of Unix System V. X assembler for Exormax and VME/10, X-C compiler VME/10, and Exormax for VAX/780 available.
From third parties: Supplier has catalog listing outside support for family. New type of support software lets 68000 run MS-DOS (8086) programs using emulation from Phoenix (Norwood, MA) and Insignia (London, UK; offices in San Francisco) or by using binary translation from Hunter Systems (Palo Alto, CA).

Text continued on pg 159

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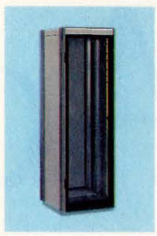

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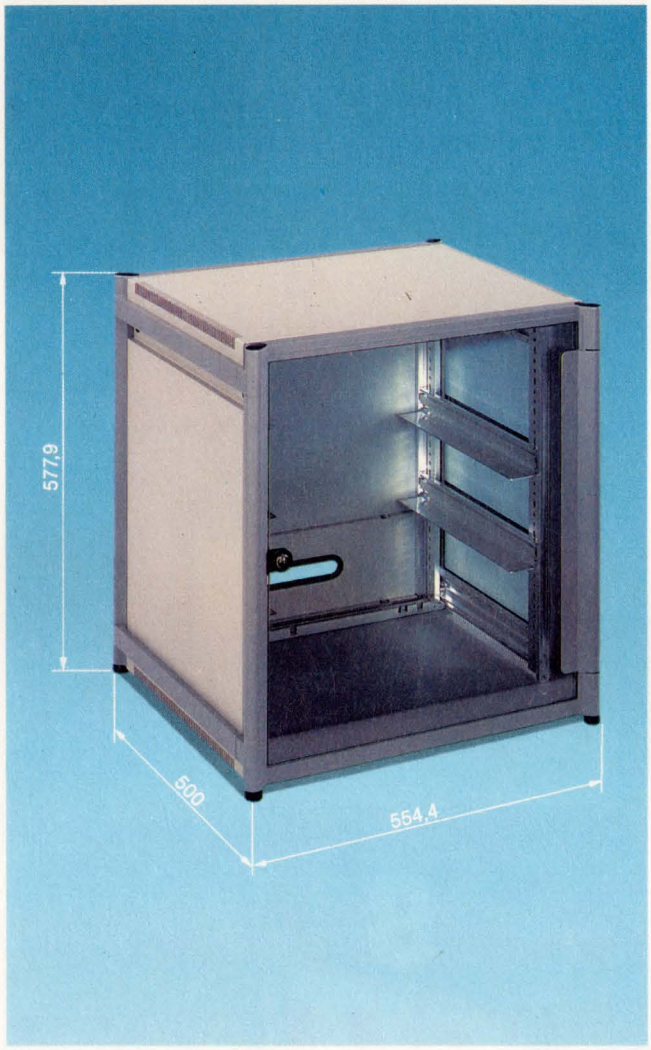

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0.68					A_2	A_2·A		A·B_2·B	C
1.0				A_2	A_2·A		A	B_2·B	C
1.5			A_2	A_2·A	A	A	B_2·B·	B_2·B·C	
2.2		A_2	A_2·A	A	A	B_2·B	B_2	B_2·B·C	D
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4.7	A_2	A	A	A·B_2·B	B_2	B_2·B·C	C	D_2·D	
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10		A·B_2·B	B_2	B_2·B·C	C	C·D_2	D_2·D		
15	A	B_2	B_2·B·C	C	C·D_2	D_2·D			
22		B_2·B·C	C	C·D_2·D	D_2·D	D_2·D			
33		C	C·D_2·D	D_2·D	D_2·D				
47		C·D_2·D	D_2·D	D_2·D					
68		D_2·D	D_2·D						
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A case	1.6 (.063)	3.2 (.126)	1.6 (.063)
B_2 case	2.8 (.110)	3.5 (.138)	1.9 (.075)
B case	2.6 (.102)	4.7 (.185)	2.1 (.083)
C case	3.2 (.126)	6.0 (.236)	2.5 (.098)
D case	4.3 (.169)	7.3 (.287)	2.8 (.110)
D_2 case	4.6 (.181)	5.8 (.228)	3.2 (.126)

mm (inch)

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NEC

68300

16/32 CMOS

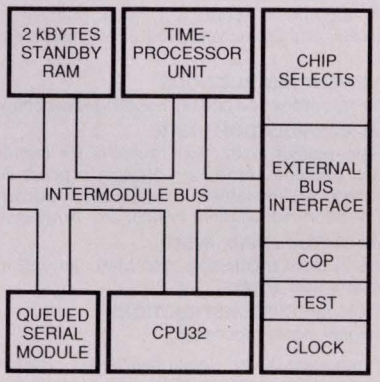
AVAILABILITY: Both the 68331 and 68332 are available now.
COST: Under $35 (1000).
SECOND SOURCE: None.
CORE: Motorola is building the family around a core that is derived from its 68020-family CPU.

Motorola Microprocessor and Memory Technologies Group
(512) 891-2990
FAX (512) 891-2651.
For more information, Circle No. 387

Description: Based on the 68020, the 68332 consists of a CPU using a basic group of 16 general-purpose, 32-bit registers and 2 kbytes of zero wait-state SRAM, a clock module, programmable chip-select logic, a serial-communications port, queued synchronous serial-peripheral interface, and a microcoded timer system with 16 orthogonal channels. Modular design concepts and the Inter Module Bus speed the development of derivative designs.

Status: Originally developed for the automotive market, the 68332 and its companion part, the 68331, are currently being used in numerous computer peripheral applications. Both devices are in production. Future derivatives will likely contain 8 channels of ADC and various configurations of Flash/EEPROM.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply/divide (signed and unsigned with 64-bit result). Logicals, rotates, and shifts. Can handle six data types: bit, byte, BCD, Word, Long Word, and Quad Word (64 bits).

II—DATA-MOVEMENT INSTRUCTIONS
Supports seven addressing modes: Absolute, Register (Direct and Indirect), Program-counter indirect with (index and displacement) and Register Indirect with index. Can use eight 32-bit address registers as indexers or stack pointers. The eight 32-bit data registers can also serve as indexers. All data movement is based on memory-mapped I/O. No special I/O or Load and Store instructions needed. A series of simple, efficient Move instructions handle all data movement and input/output.

III—PROGRAM-MANIPULATION INSTR
Subroutine call and return instructions, conditional and unconditional branches plus link and unlink instructions invoking address registers as frame pointers serve as program control. Seven levels of hardware priority interrupt with 16 software levels each for a total of 256 priority interrupt vectors.

IV—PROGRAM-STATUS-MANIP INSTR
A 16-bit Status register is software accessible. Special instructions TRAP, BKND (background), STOP, LPSTOP, and RESET along with separate SUPERVISOR and USER modes provide comprehensive system control.

V—OTHER INSTRUCTIONS
Table look-up and interpolate instruction will perform a look-up in a data table and calculate (y') for any given (x'). LPSTOP permits you to place the CPU in a low-power standby mode under software control. BKND instruction lets you put the system into background mode from your application software.

Specification summary: The 68300 family uses Motorola's Intermodule bus to tie together a 32-bit internal CPU with a range of peripherals. A clock-generator module is a PLL frequency synthesizer that generates a 16.78-MHz bus clock from a low-frequency, low-cost stable crystal such as a 32.768-kHz watch crystal. The time processor unit (TPU) is powered by a RISC-like micro-engine that reduces interrupt service overhead required by the host. The TPU performs such tasks as input capture, output compare, PWM, and stepper-motor control. An on-chip SRAM contains 2 kbytes of zero-wait-state memory for system variables and the stack. Packaging options include a 132-pin plastic QFP.

Hardware notes: 1. Diagram reflects 68332, which uses 24 bits of address and 16 bits of data.
2. Among the peripheral functions offered with the family are a clock-generator module; twelve independent programmable chip selects that let you adjust block size, wait states, and autovectoring to interrupt-service routines; and a time processor module that provides 16 orthogonal timer channels, which you can mix and match to build timers of many lengths; a queued serial module that provides both a full-duplex asynchronous serial-communications interface and a synchronous serial-peripheral interface transfers as much as 16 words without CPU intervention.

Software Note:
1. CPU 32 is object-code compatible with the 68000 CPU. This processor also includes many of the features of the 68010 and 68020 processors.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: CDS32 provides PC-hosted software and hardware development (about $5000) and includes hardware breakpoint and source-level debug. Less sophisticated, quick set-up development system is provided by the M68332EVS evaluation system ($500). Requires host computer with RS-232C and an assembler.
From others: Hewlett-Packard supplies the HP64700 (about $20,000) development station, which supports SDL and full-speed emulation. HP and Tektronix offer logic-analyzer support.

From Motorola: Assembler, C-compiler, and SDL for PC and Macintosh hosts.
From others: Introl (Milwaukee, WI) offers cross-assemblers, C cross compilers, and Modula-2 compiler for a variety of hosts including VAX/VMS, Unix, Apollo, Sun, HP, Mac, and PCs. Intermetrics (Cambridge, MA) also supports cross development on PCs, and VAX/VMS/Unix systems. Ready Systems (Dallas, TX) and SCG (San Jose, CA) offer real-time OSs. Microware (Des Moines, IA) offers OS9.

SERIES 32000

8, 16, 32/32, 32/64-BIT CMOS

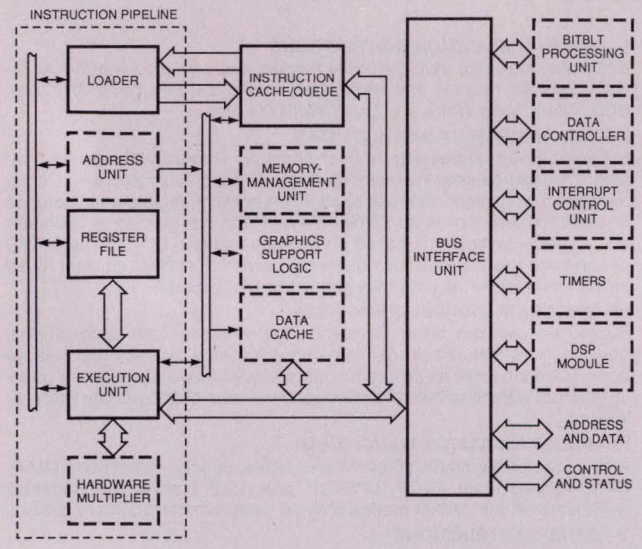
AVAILABILITY: Now.
COST: $11.50 to $600 (1000) (see table).
SECOND SOURCE: None.
CORE: National Semiconductor is using the 32000 as the basis for its application-specific embedded processors.

Description: A 32-bit μP family in which various models feature different-sized address and data buses. The 32-bit core processor is highly symmetric; that is, its instructions and addressing apply regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It also has reputation for needing less memory space for programs. Some models offer instructions to support graphics and DSP. A slave processor interface lets you expand the CPU's capabilities.

National Semiconductor Corp
Phone (408) 721-5000
For more information, Circle No. 388

Status: The vendor recently added the high-end Swordfish, which features DSP functions. Hardware and software integration techniques suit the family's processors for embedded applications such as page printers, facsimile machines, and multifunction office peripherals.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals, and bit manipulation throughout memory space and CPU registers.

II—DATA-MOVEMENT INSTRUCTIONS
Intelligent string operations and bit-field handling allow efficient movements.

III—PROGRAM-MANIPULATION INSTR
Stack- and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions.

IV—PROGRAM-STATUS-MANIP INSTR
Status registers in slave processors and MMU as well as in CPU, with both privileged and user access.

V—APPLICATION-SPECIFIC INSTRUCTIONS
Graphics and digital signal processing.

Specification summary: 32-bit, "maxi-mini"-type pipelined architecture. Uniform addressing of as many as 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, 32, 64 bits, etc) and all register and memory locations. Performance of family ranges from ¾ to 100 MIPS (sustained).

Series 32000/EP family chips

Device	DSP features	Bitblt support	On-chip peripherals	Buses	Cache	MMU	Clock rates	Price (1000)
32FX16	DSP accelerator	Microcode	DMA	24 address 16 data multiplexed	None	No	15 20 25	$23.20 $33.60 $40.80
32CG160	Multiplier	Microcode and hardware	DMA interrupt timers	24 address 16 data multiplexed	None	No	15 20 25	$38.90 $40.70 $48.40
32GX320	Multiplier DSP instructions	None	DMA interrupt timers	32 address 32 data	Instruction and data	No	20 25 30	$83 $100 $137
32GX32	None	None	None	32 address 32 data	Instruction and data	No	20 25 30	$58 $63 $78
32CG16	None	Microcode	None	24 address 16 data multiplexed	None	No	10 15	$11.50 $21.70
32532	None	None	None	32 address 32 data	Instruction and data	Yes	20 25 30	$465 $535 $600
32SF641	Multiplier DSP instructions	None	DMA interrupt timers	32 address 64 data	Instruction and data	No	25	$500

Hardware notes: 1. Dashed lines in diagram indicate optional modules for the 32000 family.
2. Floating-point chips (32081, 32181, and 32381) are examples of slave-type processors that vendor uses to extend CPU. These processors will be integrated on CPU when VLSI processing technology permits; they are transparent to programmer and recognize op codes not used by CPU.

HARDWARE SUPPORT SOFTWARE

From National: SYS32/20 converts IBM PC/AT into a Series 32000/EP development tool (from $7000). Development/evaluation boards are also available for each of the processors. Tools run on both Sun-4 and HP9000 workstations.
From others: ISE support for all the Series 32000/EP processors is available from Hewlett-Packard. Various vendors also offer turn-key solutions and/or design support for National Semiconductor's processors. Contact Series 32000/EP Marketing for details.
Evaluations Boards: $1190 for the NS32FX16 and NSV-FX-CG-EDB; $1495 for the NS32CG160 and NSV-CG160-EDB; $2995 for the NS32GX320 and NSV-GX320-EDB; and $10,000 for the NS32SF641 and NSV-SF641EDB.

From National: GNX (Genix Native and Cross) development-tool software includes assembler package and choice of C, Pascal, or Fortran compilers available for native (Sys32/50) Sun-4 environments. Software that enables the 32FX16 and 32GX320 to operate as either a FAX modem, data modem, and voice processor is also available.
From others: Various Postscript and Postscript-compatible language interpreters, as well as related software support (fonts, PCL, etc) are available for laser-printer-controller designs.

Text continued on pg 165

When it comes to memory, single-chip microcontroller designs have always been compromises. Use RAM, and you'd lose data on power down. Use ROM, and you couldn't alter your program. Now Xicor is introducing an uncompromising E^2PROM micro-peripheral, the X88C64.

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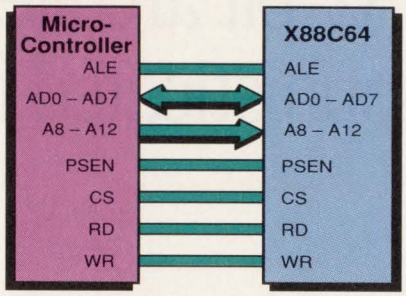

For reprogrammable microcontroller designs—such as automotive engine controllers, digital televisions and cellular telephones—the X88C64 offers an exceptionally cost-effective solution. And it's available in popular through-the-hole and surface-mount packages. Call or write today for details. Xicor Inc., 851 Buckeye Court, Milpitas, CA 95035. Phone (408) 432-8888.

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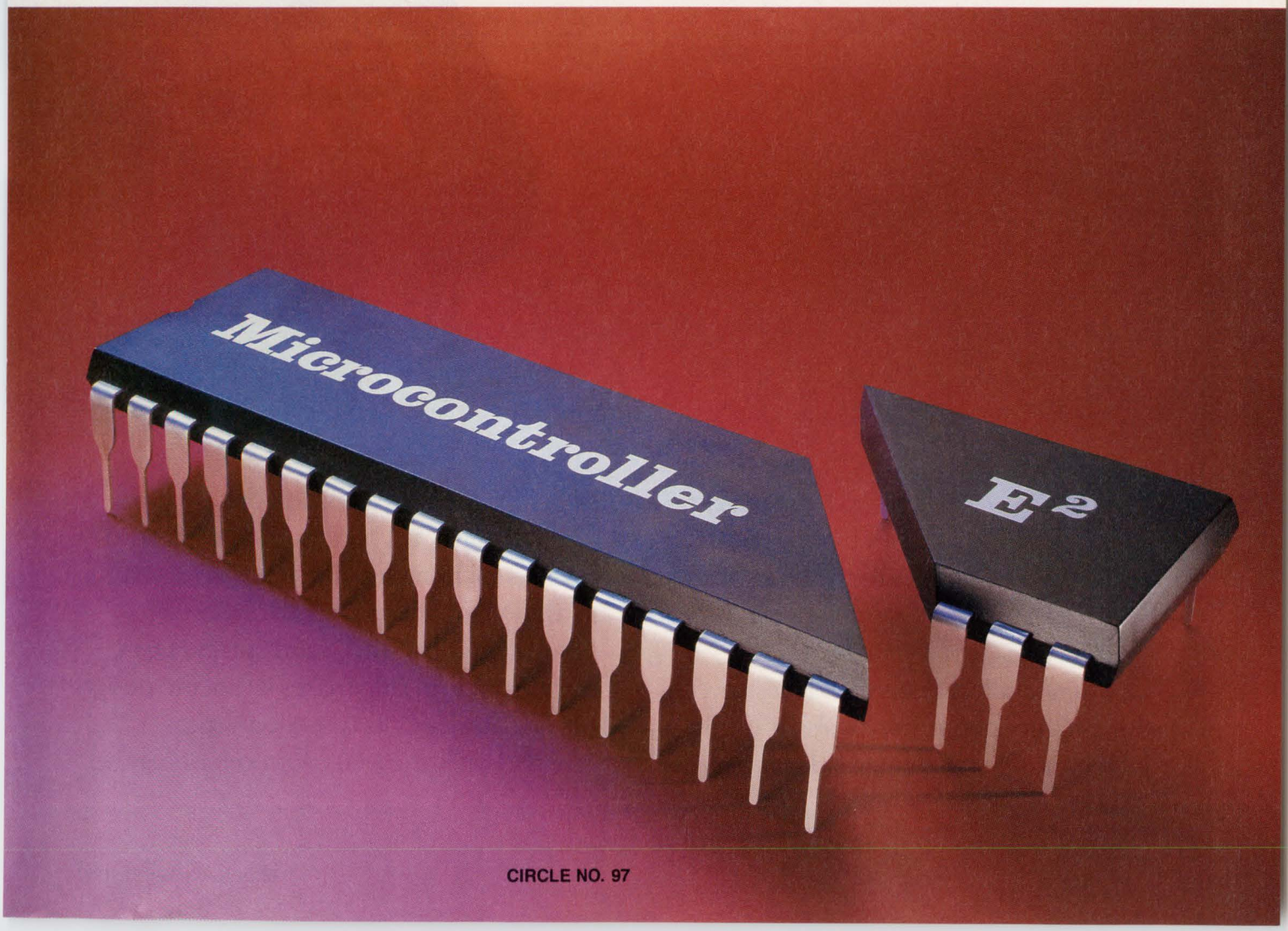

CIRCLE NO. 97

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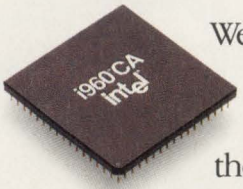

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CIRCLE NO. 99

VY86Cxxx ARM

32-BIT CMOS

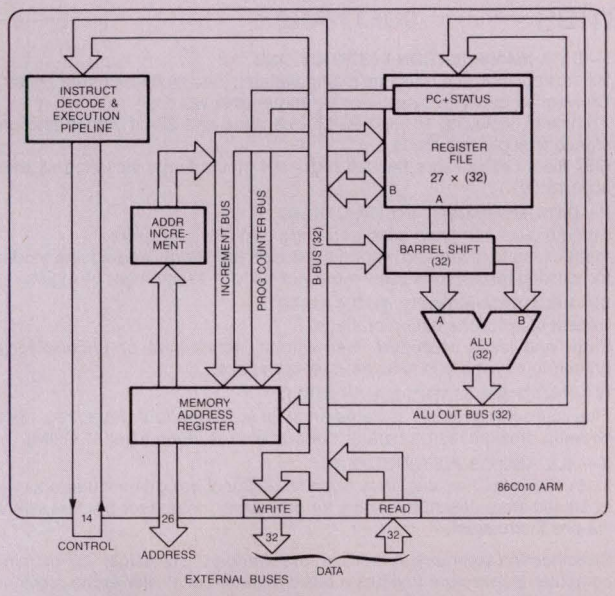
AVAILABILITY: Now for 86C010 and 86C020. 86C060 and 86C600 samples available late 1991.
COST: In 1000 qty, $25 for 86C010; $72 for 86C020; $35 for 86C060; $125 for 86C600.
SECOND SOURCE: Sanyo Semiconductor Ltd sources the 86C010.
CORE: Part of VLSI's cell library. All variations are available as functional blocks for ASICs.

VLSI Technology Inc
San Jose, CA 95131
Phone (408) 434-3000
FAX (408) 434-7926
For more information, Circle No. 389

Description: ARM stands for Acorn-RISC machine. The 86C010 has found application in home computers and drawing accelerators. Upgrade features of the -020 include a 4-kbyte unified cache. The -060 increases the address range to 4 Gbytes. Stepping up to the -600 adds a 4-kbyte cache, an 8-byte-deep write buffer, and memory management to the -060. Support chips include a memory/DMA controller, a video control/sound output chip, and an I/O controller.

Status: The company supplies evaluation boards, assemblers, and C compilers directly. The architecture of the chip is targeted at the embedded-controller market and provides performance similar to most competing RISC processors at lower cost. Cost is kept low because of small die size (approximately 280 mils square in a 1.0-μm process) and 160-pin plastic quad flatpack packaging. A dedicated coprocessor bus necessitates the high pin count. The 86C020 has found application in laser printers, network controllers, disk controllers, and graphics subsystems.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
As is common in RISC machines, two source registers and a destination register are specified in most instructions. Add, subtract, logicals, bit clear, and embedded immediate operands.

II—DATA-MOVEMENT INSTRUCTIONS
Register moves with optional shift. Load/store word (32-bit) or byte with base-register/offset or base register and index register addressing modes. Load/store multiple register instructions offer fast stacking and procedure switching. Swap register with memory added in -020, -060, and -600.

III—PROGRAM-MANIPULATION INSTR
All instructions are conditional, which offers a skip option and reduces instruction count and branching. Branch and branch-and-link (program counter to Reg14) is relative, with a ±32-Mbyte range. Absolute jumps are also possible. Software interrupt provides trap door to system services.

IV—PROGRAM-STATUS-MANIP INSTR
Status setting is optional on data-manipulation instructions. Status bits are included in program counter in -010 and -020, but 32-bit addressing in -060 and -600 requires adding separate program-status-word (PSW) registers (one for each mode).

Specification summary: 32-bit data and 26- or 32-bit address CMOS Von Neumann (common memory) μP with RISC-style architecture. Uses a 2-level pipeline with interlocks. Supports large linear memory addressing with optional memory management (86C600). I/O is memory mapped. Instruction set is expandable using internal or external coprocessors. Has simple ALU with associated barrel shifter and set of 27 registers (31 on -060 and -600). Processors have several operating modes with partially overlapping register sets. Modes in the -010 and -020 are user, supervisor, interrupt, and fast interrupt. The -060 and -600 add abort and illegal-instruction trap modes. Instructions specify registers in groups of 16 with 4-bit fields. Each mode has a unique R14 (link) and R13 (stack pointer), and fast-interrupt mode adds unique R12 through R8 to improve interrupt response without user-register stacking. As with all simple RISC processors, performance in the -010, -020, and -060 is limited by memory-access bandwidth. Surrounding the processor with faster SRAM enables faster operation.

Hardware notes:
1. In addition to the 86C010 μP, VLSI has an associated set of chips for memory (86C110), video (86C310), and I/O (86V410). For floating-point math, VLSI suggests one of the commercially available coprocessors.
2. Note the 27 registers. This number is less than on some RISC machines, but the registers do overlap, as is common in RISC, to speed interrupt service (overlapping yields automatic saving of data). Thus, a programmer sees 16 registers at most, and of these, 15 are general purpose.
3. Some provisions for memory management, including cache and virtual memory through abort-signal, mode-control bits.

Software notes:
1. Only 44 instructions, supporting the literal RISC concept.
2. Simple RISC instructions ease the task of writing efficient high-level-language compilers.
3. User and supervisory modes; supervisory mode entered by software interrupt.

HARDWARE CHARACTERISTICS SOFTWARE

VLSI supplies a PC evaluation board (Blue Streak) with an -010, -110, and -410 operating at 8 MHz. An -020 daughter board is also available. A stand-alone evaluation board that operates to 50 MHz with -010 or -020 processors is under development. This board includes a 110 memory and DMA controller, 410 I/O controller, IDE interface, 106 keyboard controller, and real-time-clock interface.

Assembler and C compilers on PC, Sun, and Macintosh computers and workstations. A real-time operating-system kernel should be available early in 1992.

386 FAMILY

32-BIT CMOS

AVAILABILITY: 16-, 20-, 25-, and 33-MHz versions in production from Intel. AMD is shipping its 40-MHz version. Chips and Technologies will be production shipping its μPs early in 1992; all are sampling now.

COST: In 1000 qty, Intel's prices are $58 to $98 for the 386SX; $161 to $202 for the 386DX. The 20-MHz Intel 386SL costs $135. AMD charges $199 for 40-MHz standard and low-power 386DX. C&T prices are $70 to $110 for its SX versions and $150 to $215 for its DX versions.

SECOND SOURCE: None licensed. AMD is the first of several vendors to develop clean-room versions of the family. Barring legal complications, Chips and Technologies will offer two versions.

Description: The 32-bit 386 family of μPs is compatible with the 8086 and 80286 families. Included are address-translation registers and a 32-bit address bus for as many as 4 Gbytes of physical memory and 64 Tbytes of virtual memory (the SX and 376 processors have only a 24-bit address bus). Runs DOS, Windows, OS/2, Unix, iRMX, and iRMK. The 386SX permits manufacturing of less expensive systems with full 386 software capability. The 386SL integrates a fully static CPU core with cache and main memory controllers, bus and coprocessor interface logic, and power-conservation and extended-memory mapping logic. AMD's low-power versions also utilize a fully-static CPU. C&T's 38605s include a feature the company calls Superstate that operates as a supervisory layer between the system hardware and BIOS.

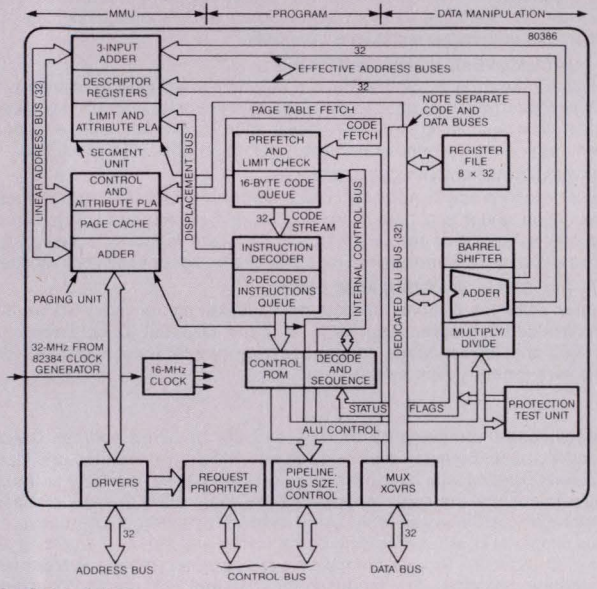
Intel Corp
Phone (408) 765-8080
For more information, Circle No. 390

Advanced Micro Devices
Phone (408) 732-2400
Literature (800) 292-9323
For more information, Circle No. 391

Chips and Technologies
Phone (408) 434-0600
for more information, Circle No. 392

Status: The 386 will remain the dominant 32-bit μP, certainly for the next several years. The 386 is the sole μP family carrying the IBM PC momentum into the 32-bit world. Intel is in production with the 80376—a version of the 386 aimed at the embedded-controller world. Intel also offers the 386SX, a version of the 386 that supplies a 16-bit data bus and a 24-bit address bus in standard and low-power versions. Several vendors are struggling to develop instruction-set-compatible versions of the 386 family to capitalize on the family's success. AMD is the first vendor to effectively clone the 386 and offers low power, higher-speed versions of the 386. C&T is sampling devices that are either pin compatible or offer additional features to the 386.

HARDWARE CHARACTERISTICS SOFTWARE



Hardware notes:

1. No on-chip cache, but the 33-MHz 82385 cache controller ($80 (1000)) and the 82395DX cache controller ($78 (1000)) provide external cache implementations.
2. On-chip MMU chip allows memory management with no penalty in bus bandwidth (if off chip, supplier says, an extra cycle would be needed). Allows choices of segmentation or paging singly or in combination for multiuser protection and for virtual memory.
3. Along with the 80387 math coprocessor ($299) and 82385, the 386's performance is enhanced by the 82380 32-bit peripheral combination chip.
4. C&T's 38605 devices provide a 512-byte instruction cache and a transparent hardware and software layer that permits, among other things, running two operating systems on one processor, I/O emulation, and software-specific acceleration.
5. The 386SL offers four power-management modes. An RSM instruction allows the system to transparently return from suspend mode to the interrupted program.

I—DATA-MANIPULATION INSTRUCTIONS
Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter). Conversion between bytes, words, and double words.
Arithmetic, including 16- and 32-bit operands and 32-bit signed and unsigned multiply and divide.
(387 math coprocessor has full IEEE-754 instructions, including all transcendentals.)

II—DATA-MOVEMENT INSTRUCTIONS
String moves and gang push and gang pop of all registers.
Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers).

III—PROGRAM-MANIPULATION INSTR
Repeat instructions based on flags.
Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4-Gbyte memory space.

IV—PROGRAM-STATUS-MANIP INSTR
Flag instructions mostly same as on 8086 (contains four debug registers, allowing breakpoints on data or code accesses, even when in ROM).

V—HLL AND OS INSTRUCTIONS
Instructions for checking array bounds; segment assignment instructions. Load and store descriptor tables for protection (processor context switch via one instruction).

Specification summary: A more or less standard, "classical" 32-bit minicomputer architecture that has a basic register set similar to the previous 16-bit members of 8086 family so that it can directly run their machine code. It has added features that make it more general and suited to larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. C&T's versions incorporate a 5-stage pipeline to improve instruction throughput. Intel, AMD, and C&T offer devices packaged in 132-lead ceramic PGA. AMD also offers 132-lead PQFP for the DX/DXL and 100-lead PQFP for the SX/SXL. C&T's 605 versions are not pin compatible with standard 386 devices; the SX comes in 132-pin PQFPs, and the DX comes in 144-pin CPGAs.

Software notes:

1. Only those instructions beyond basic 8086 instructions described.
2. 386 said to be object-code compatible with previous members of 8086 family and can run their operating systems. There is a "virtual 8086" mode in which 8086 (and 8088) code can be run within the protected 386 environment.

HARDWARE CHARACTERISTICS SOFTWARE

ICE386DX25DZ in-circuit emulator ($22,495) supports 386DX μP to 25 MHz; ICE386DX33D ($29,500) supports to 33 MHz. ICE386SX in-circuit emulator ($18,495) supports 386SX to 20 MHz. ICE376D in-circuit emulator ($18,495) supports 80376 to 16 MHz. All Intel ICE in-circuit emulators for the 386 family operate on a common emulator base. They provide control and display software with a common Intel windowed user interface with drop-down menus and source-code display hosted on DOS on PC and PS/2 systems. Various Multibus I and II single-board computers are also available from Intel and other vendors for the 386DX μP.

From Intel: ASM-386 macroassembler ($600), RLL-386 binder and system software builder utilities ($600). The C-386, Fortran-386, and PL/M-386 compilers (each $900) support 386-μP-family protected-mode software cross development on DOS hosts. VAX/VMS kit support including ASM, RLL, and compilers of choice is also available on Micro VAX ($8,000) and VAX ($13,000) systems for cross development.

From others: Widespread third-party support. Most important are MS-DOS, Windows, and OS/2. (There are variations in DOS such as Concurrent DOS by Digital Research (Monterey, CA). Unix V from AT&T (Morristown, NJ) and Zenix from Microsoft also available. Real-time executives offered by Ready Systems (Palo Alto, CA), JMI Software (Spring House, PA), and others. In addition, there are dual combinations of operating systems such as Unix-DOS, CTOS-DOS, and DOS-DOS.

Text continued on pg 171

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In addition to the Ultra-Rel diodes, each SBL contains components that can withstand the strenuous shock and vibration requirements of MIL-STD-28837 along with more than 200 cycles of thermal shock extending from -55 to +100°C. Every Ultra-Rel™ SBL-mixer carries a five-year guarantee.

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SBL SPECIFICATIONS (typ).

Model	Frequency (MHz)	Conv. Loss (dB)	Isolation (dB) L-R	Isolation (dB) L-I	LO Level (dBm)	Price, $ ea. (10 qty)
SBL-1	1-500	5.5	45	40	+7	4.50
• SBL-1X	10-1000	6.0	40	40	+7	6.25
SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
• SBL-11LH	5-2000	7.0	45	30	+10	19.75
SBL-1MH	1-500	5.5	45	40	+13	9.80
SBL-1ZMH	2-1100	6.5	40	25	+13	11.70

• IF not DC coupled

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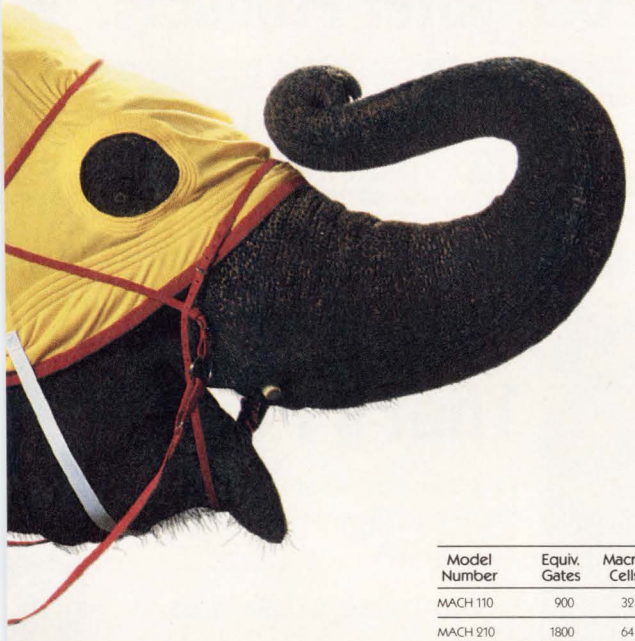
F143 REV. ORIG.

CIRCLE NO. 100

Until Now, Density A Pretty Awkwa

And Speed Were rd Combination.



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Nothing can squash an elegant, high density design faster than a slow, unpredictable and expensive PLD. That's why we've developed the MACH PLD family—for both density, and speed.

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And they work for peanuts. The MACH family can bring your costs down as low as a penny per gate—up to 40% less than other high density PLDs.

Model Number	Equiv. Gates	Macro Cells	Max. Delay	System Speed	I/O Pins	Hard-Wired Option
MACH 110	900	32	12ns	66.7 MHz	44	MASC 110
MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230*	3600	128	15ns	50 MHz	84	MASC 230

* Available Q1 1992.

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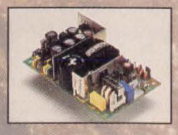

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CIRCLE NO. 102

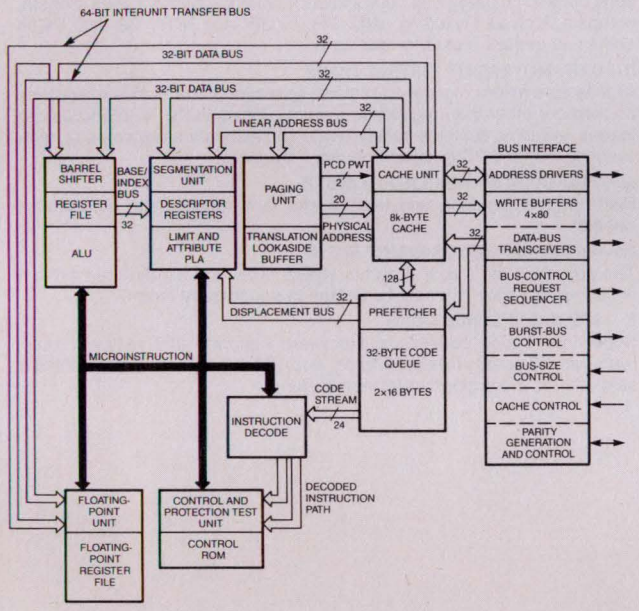
AVAILABILITY: 25-, 33-, and 50-MHz 486 and 20-MHz 486SX are now in production.
COST: In 1000 qty, the 486SX, $247 (20 MHz) in PGA; for the 486, $445 (25 MHz and 33 MHz) and $665 (50 MHz).
SECOND SOURCE: None.

Intel Corp
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 393

Description: The 486 CPU comprises an enhanced 386 CPU, an enhanced 80387 math coprocessor (though still fabricated in the silicon, the coprocessor in the 486SX is disabled), an 82385 cache controller, an 8-kbyte combined code and data cache, and a paging and memory-management unit. The 486 is binary compatible with '386/'387 processor software but is 2 to 4× faster because of enhanced execution pipelining and higher integration. The 486 CPU adds several new instructions that support caches and multiprocessor operating systems. A byte-swap instruction allows the 486 CPU to read data in either big- or little-endian format. A burst bus allows the 486 to fill the on-chip cache with 16 bytes of data in five clock cycles.

Status: Intel introduced the 50-MHz version in June of this year in both component and CPU-cache modules. The 33-MHz version has been in production since May 1990. Other family members include the 486SX, which features a disabled math coprocessor, allowing fewer pinouts and cheaper packaging. The 487 "coprocessor" is a repackaged, healthy 486 that, when properly designed into systems, completely disables the already crippled 486.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Byte swap for converting between little- and big-endian data. Compare and exchange instruction. Exchange and add instruction. Floating-point instruction set from 387 math coprocessor added to 486 CPU.

II—DATA-MOVEMENT INSTRUCTIONS
Information not provided by manufacturer.

III—PROGRAM-MANIPULATION INSTR
Information not provided by manufacturer.

IV—PROGRAM-STATUS-MANIP INSTR
Information not provided by manufacturer.

V—HLL AND OS INSTRUCTIONS
Instructions for flushing and invalidating the caches.

Specification summary: A standard 32-bit architecture containing the same register set as its predecessor, the 386DX CPU. The 486 adds a small cache and floating-point processor as well as the instructions and control bits to support these features. The 50-MHz part is fabricated using a 0.8-μm process and consumes less than 1000 mA. The μP is packaged in a 168-pin ceramic PGA.

Hardware notes:
1. 8-kbyte unified instruction and data cache is located on chip. The cache lets the CPU read 16 bytes of code into the prefetch queue in one clock. A cache hit rate of better than 90%, for most applications, greatly reduces memory bus utilization for memory reads and improves system performance.
2. The 82495DX/82490DX cache subsystem provides a complete second-level cache for the 50-MHz CPU. You can configure the subsystem as a 128-, 256-, or 512-kbyte 2-way, set-associative, write-back cache. The system can run this cache synchronous, divided synchronous, or asynchronous to the memory bus.
3. The Turbocache486 module ($299 for 64-kbyte version and $399 for 128-kbyte version at 33 MHz in 1000 qty; 25 MHz also available) is a complete second-level write-through cache controller and SRAM. The module contains the 82485 cache controller ($89 (25 MHz) and $99 (33 MHz) in 1000 qty). The module's look-aside design lets you add the module as an option much as the 387 was an option to 386 systems.
4. An on-chip MMU allows memory management identical to the 386DX CPU. The MMU allows segmentation, paging, or a combination of both for multiuser protection and for virtual memory.
5. The 50-MHz version of the 486 CPU and the cache subsystem support the IEEE 1149.1 boundary-scan specification.

HARDWARE — SUPPORT — SOFTWARE

ICE48633D in-circuit emulator ($38,000) supports the 486 μP to 33 MHz with real-time execution control over prototype 486-based systems. ICD48633D in-circuit debugger ($11,500) is a hardware-assisted real-time debug monitor supporting 486 μP to 25 MHz. ICD48625D supports execution breakpoints, including cached breaks, control of 486 μP execution, and access to registers and system memory. A standard logic-analyzer interface supports cross triggering between ICD486 and a high-speed logic analyzer. The ICD48625D in-circuit debugger is hosted on DOS PC and PS/2 systems. Host software uses the common Intel windowed interface model with drop-down menus and source-code display.

From Intel: Intel's 486 assembler, compilers, system utilities, and software debuggers are intended for computer-system software development requiring access to the full native-mode architecture models of the 486 μP. ASM macroassembler ($600); RLL binder and system-software-builder utilities ($600); and C, Fortran, and PL/M compilers (each $900) support 486-family protected-mode software cross development by generating 486 instructions in code developed on DOS hosts. Language kits ($4500) including ASM, RLL, a compiler of choice, and the DB debugger are also available. VAX/VMS kit support including ASM, RLL, and a compiler of choice is available on MicroVAX ($8,000) and VAX ($13,000) systems for cross development.

CLIPPER

32-BIT CMOS

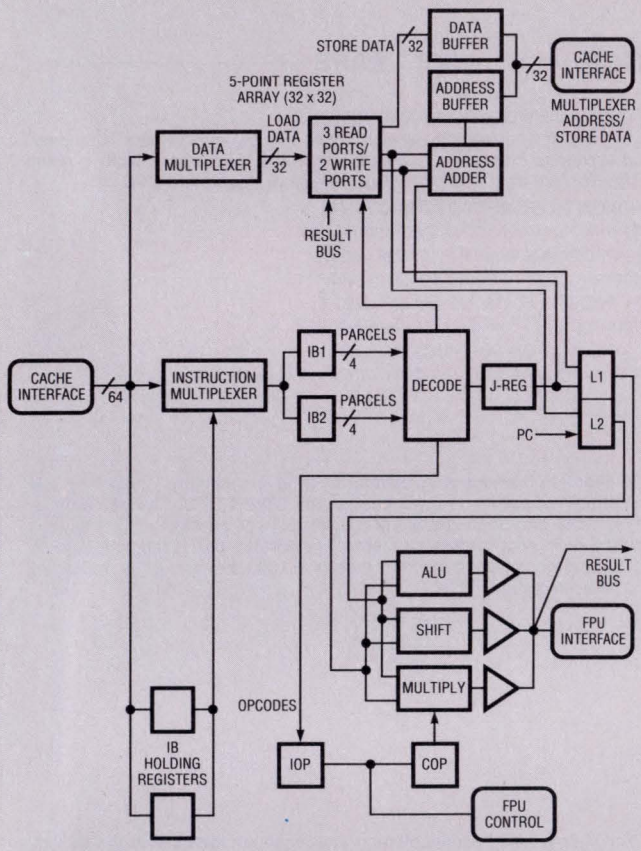
AVAILABILITY: Now for 40- and 50-MHz C300 chips ets and modules, and the C311 CPU/FPU. Now for the 40- and 50-MHz C4 CPU and FPU chip set.
COST: All 1000 qty: At 40 MHz, the C311 CPU/FPU costs $160, the C300 chip set costs $336, and the module costs $536. At 50 MHz, the C311 CPU/FPU costs $191, the C300 chip set costs $495, and the C300 module costs $695. The 40-MHz C4 CPU and FPU chip set costs $795, and the 50-MHz chip set costs $895.

Intergraph Corp
Advanced Processor Div
Phone (415) 494-8800
For more information, Circle No. 394

Description: The CMOS RISC-based C411 CPU uses superscalar instruction issue and superpipelining to speed execution. Binary compatibility exists between the C400 and the C300. The C421 is the floating-point coprocessor for the C411 CPU.

Status: The company claims to have shipped over 70,000 modules through July 1991, giving Clipper a large, but narrow, installed base—Intergraph accounts for most of the Clipper sales.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, divide (32- and 64-bit IEEE floating-point operations done in floating-point coprocessor), floating-point converts, negate, compare, logicals (including AND, OR, EXOR, and NOT), 32- and 64-bit shifts and rotates, including floating point.

II—DATA-MOVEMENT INSTRUCTIONS
Architecture favors register-to-register operations and avoids operations on memory other than register-to-memory movements. Nine addressing modes, including absolute, relative (with and without displacements), relative indexed, and PC (program-counter) indexed.

III—PROGRAM-MANIPULATION INSTR
Push, pop, supervisor, and user stacks (any register can be used as pointer).

IV—PROGRAM-STATUS-MANIP INSTR
Two status words, a user-program status word, and a privileged system status word, which can only be written in supervisory mode.

V—SPECIAL INSTRUCTIONS
Supervisory mode commands. Hardware supports 256 vectored interrupts with 16 priority levels, 57 traps, and 128 supervisory calls. Software semaphores are supported for multitasking.

Hardware notes:
1.The C411 CPU features separate ALU, barrel shifter, and multiplier operating in parallel.
2. The C411 has two high-speed buses: a 64-bit, 800-Mbyte/sec input bus and a 32-bit multiplexed address/data bus that uses differential drivers for fast, low-voltage swings.
3. Improved input bus architecture alternates data fetch with instruction fetch on every half-clock cycle.

Software notes:
1. Despite the vendor's insistence on calling the processor a RISC machine, the C300's 164 instructions include both single-cycle (RISC-like) and multicycle (CISC-like) commands. Hardwired architecture in the C400 allows most instructions to execute in one clock cycle. C400 superscalar operations can issue multiple instructions on each clock cycle.
2. The C411 CPU and C421 FPU instructions are compatible with the C300.
3. The C421 is compatible with the IEEE-754 floating-point standard.For optimum performance, the C411 utilizes a large external cache to supply instructions and data on every clock cycle at 50 MHz. The processor uses separate 64-bit input and 32-bit output buses to support the CPU's data and instruction bandwidth requirements. Fast IEEE-754 floating-point operations are executed by the C421 coprocessor also running at 50 MHz. The C411 CPU can be purchased individually or as a pair with the C421 FPU. Both are available in 299-pin PGA packages. Future versions of the C400 family are planned to operate at speeds in excess of 50 MHz.

HARDWARE — SUPPORT — SOFTWARE

The C300 Clipper Module integrates three Clipper chips into a functioning CPU. Intergraph offers Clipper development systems that provide 8 Mbytes of RAM, 156 Mbytes of hard-disk storage, and an Ethernet interface. Software includes CLIX (based on Unix System V), a C compiler, a loader/debugger, and utilities.

Intergraph offers a set of optimizing compilers for C and Fortran and a performance-tuned operating-system kernel for the C411/421. More than 750 third-party packages are available, including compilers for Lisp, Ada, and other languages; tools and utilities; and end-user application packages.

HYPERSTONE

32-BIT CMOS

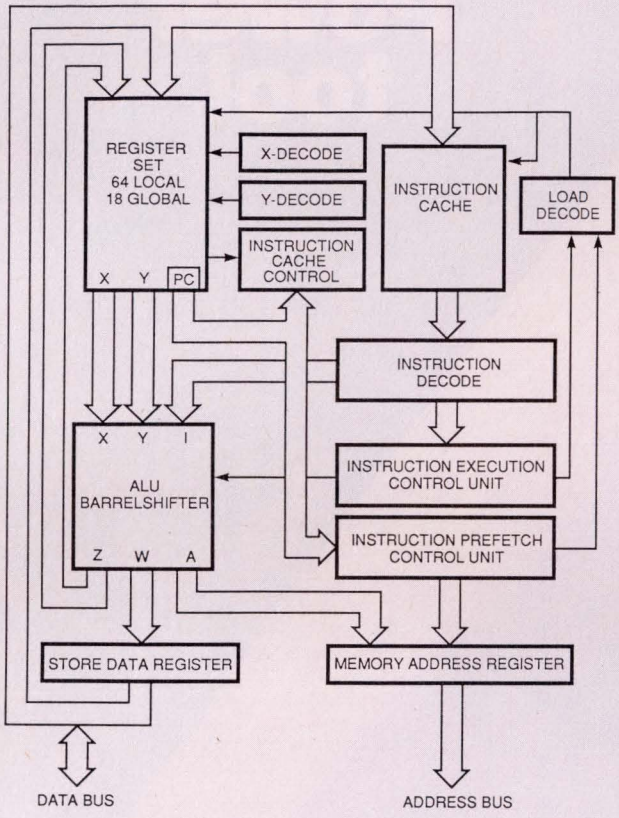
AVAILABILITY: Now for 25-, 33-, and 40-MHz parts in 144-pin plastic PGA and 25-MHz devices in 132-pin QFP.
COST: $77 (1000) for the 25-MHz part.
SECOND SOURCE: Zilog.
CORE: Zilog will use the Hyperstone μP as a 32-bit core in its library of μP cores.

Hyperstone Electronics GmbH
Phone (011) 49 075 316-7789
FAX (011) 49 075 315-1725
For more information, Circle No. 395

Description: Hyperstone combines features of both RISC and CISC architectures. Although most instructions are 16 bits wide, some are 32 or 48 bits wide. Almost all instructions execute in a single cycle. The vendor claims that Hyperstone program code will be more compact than many CISC-architecture programs. The microprocessor uses a combination of pipelined load instructions, an internal decode/execute pipeline of two stages, and a proprietary look-ahead instruction cache to achieve high performance. In addition, on-chip DRAM and bus control simplify the interface between the μP, memory, and peripherals.

Status: The Hyperstone suits embedded-systems applications. Zilog has announced its intention to use the Hyperstone in its library of μP cores. These cores form the base for microcontrollers for data communications, intelligent-peripheral-control, and disk-control applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on 32- or 64-bit data. Most instructions are single cycle, but multiply and divide are multicycle. A barrel shifter provides left/right and signed/unsigned shifts. Two sets of arithmetic instructions are available: One set traps on overflow; the other only flags overflow. Logic instructions are AND, AND NOT, OR, XOR, and NOT. More powerful instructions include scaled index move, bound check, and scan leading zeros. IEEE-floating-point instructions execute by emulation.

II—DATA-MOVEMENT INSTRUCTIONS
Pipelined load/store architecture. Data types are byte and halfword (both signed and unsigned), 32-bit words, and 64-bit double words. Hyperstone contains single- and double-word move instructions.

III—PROGRAM-MANIPULATION INSTR
One unconditional and 12 conditional branch instructions provide program-counter relative delayed/undelayed branches. The μP executes dynamic branches via move or add instructions to the program counter. A call instruction creates a new variable-length stack frame in the register stack. A frame instruction restructures the stack frame for parameter passing. A return instruction returns control and restores the old stack frame. The μP handles overflow or underflow automatically.

IV—PROGRAM-STATUS-MANIP INSTR
One unconditional and 11 conditional trap instructions trap to supervisor state via a 64-entry table.

V—SYSTEM-LEVEL INSTRUCTIONS
Moves to special registers and setting the interrupt mask bit are only possible in supervisor mode.

Specification summary: The Hyperstone μP has a balanced set of instructions that make it useful as a universal processor. Since virtual memory is rarely used in embedded systems, Hyperstone doesn't include on-chip memory management. Demand paging via an off-chip memory-management unit is assisted. The architecture supports seven types of addressing, including post-increment and post-increment with variable increment.

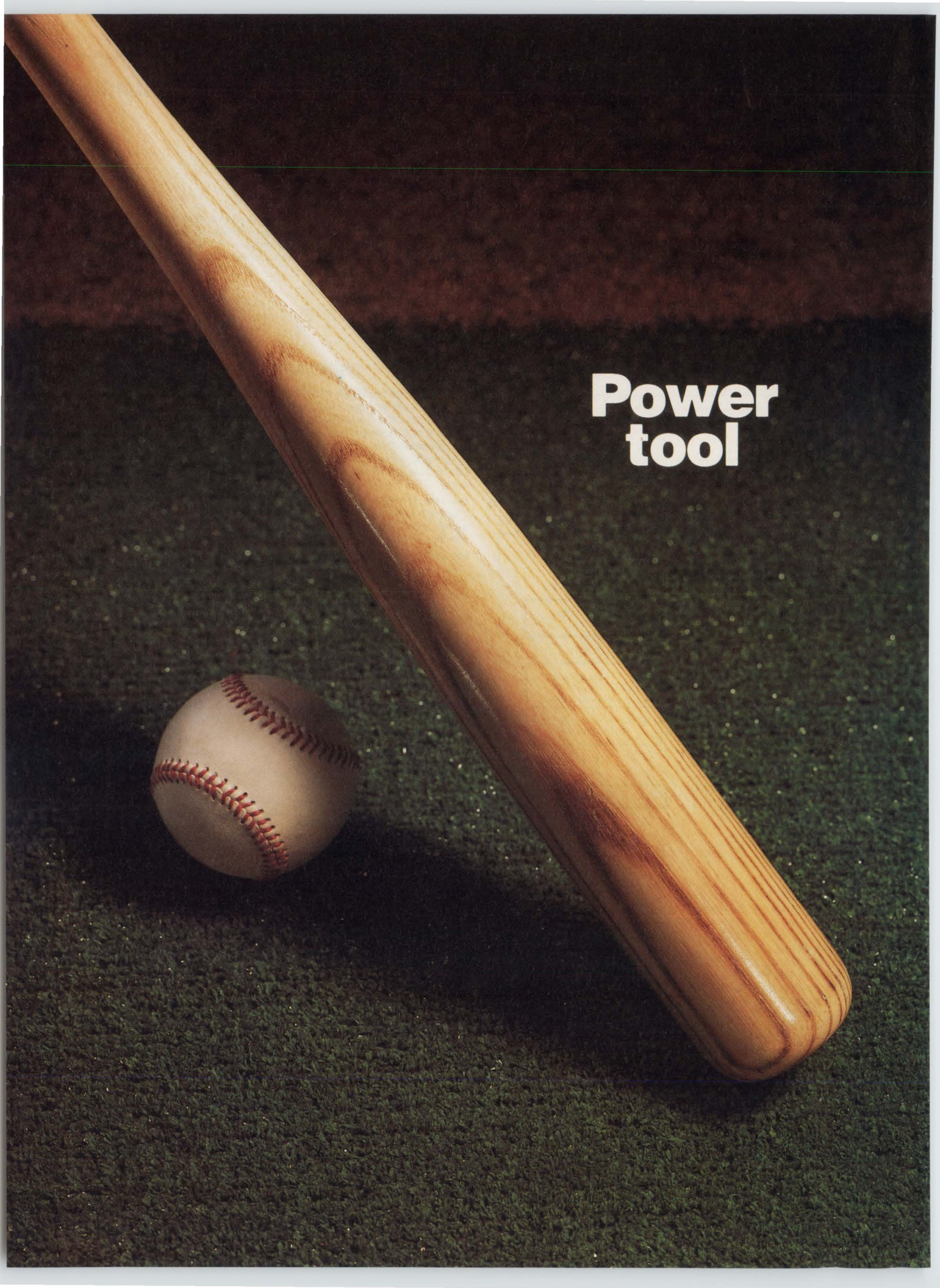
Hardware notes:
1. The μP has separate 32-bit address and data buses. The μP's 64 local registers are arranged in a register stack that contains stack frames of variable length—2 to 16 registers. Overlapping stack frames (windows) allow parameter passing. Because of the code compaction of mostly 16-bit instructions, the 128-byte instruction cache achieves hit rates comparable to larger caches on other devices.
2. The μP contains all the logic to directly control DRAMs, SRAMs, ROMs, and other peripherals. The Hyperstone also performs parity generation and parity check.
3. The processor also contains a 32-bit timer.

HARDWARE — SUPPORT — SOFTWARE

In-circuit emulator via an add-on board to the IBM PC. Add-on boards to the IBM PC and evaluation boards via an RS-232C port.
Evaluation Boards: You can connect the hyEVAT 25 software-development board to a personal computer host for processor evaluation and software development.

Hyperstone Electronics supplies pc-based macroassembler, C compiler, and source-level debugger. A real-time kernel, hyRTK, is also available. The source-level debugger includes real-time debugging facilities. Zilog is developing a behavioral model.

Text continued on pg 176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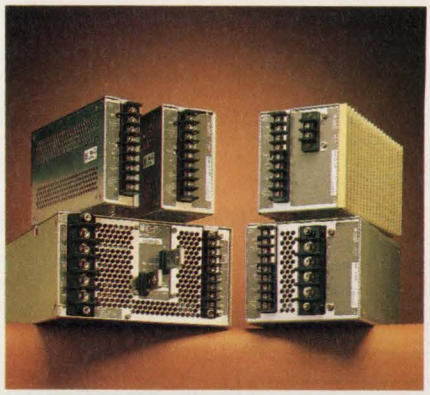

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- ☐ Tested to MIL STD 810D
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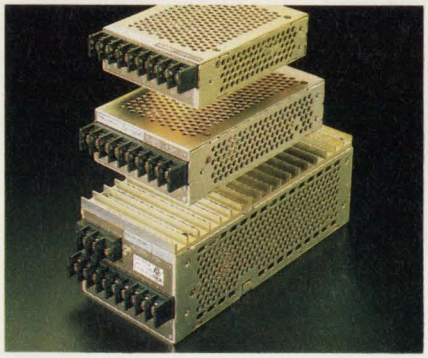
ac to dc power single output 600W

- ☐ 2V-48V dc output
- ☐ Jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
- ☐ Fully enclosed
- ☐ UL/CSA
- ☐ Tested to MIL STD 810D

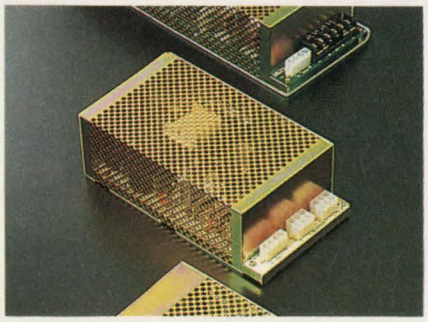
Kepco Group RBX Power Supplies



dc to dc power single output 30W, 60W, 150W

- ☐ 5V-48V dc output
- ☐ 24 and 48V input (60V available on some models)
- ☐ Fully enclosed
- ☐ UL/CSA
- ☐ MIL STD 461B EMI filtering
- ☐ Tested to MIL STD 810D

Kepco Group ERD Power Supplies



ac to dc power single output 30W, 60W, 120W, 240W

- ☐ 5V-24V dc output
- ☐ Jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
- ☐ PC card, L-chassis, optional enclosure
- ☐ UL/CSA/TÜV
- ☐ FCC Class B EMI filtering

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CIRCLE NO. 103

SPARC FAMILY

32-BIT CMOS

AVAILABILITY: See table.
COST: See table.
SECOND SOURCE: Fujitsu's MB86903 and Weitek's W8701 are pin compatible, as are Fujitsu's 86901 and 86902 and LSI's L64801 PGA and QFP, respectively. LSI Logic makes a version that is pin compatible to the Cypress implementation. All versions must run Sun Microsystems Inc (Mountain View, CA) SPARC software. Fujitsu, Cypress, LSI, and Philips/Signetics also provide SPARC embedded controllers. TI provides a floating-point unit.
CORE: Fujitsu has designed a full-custom modular core for ASIC implementations. LSI Logic also offers RISC elements in its ASIC library.

Fujitsu Microelectronics Inc
Advanced Products Div
Phone (800) 523-0034
FAX (408) 943-9293
Circle No. 396

LSI Logic Corp
Phone (408) 954-4985
Circle No. 398

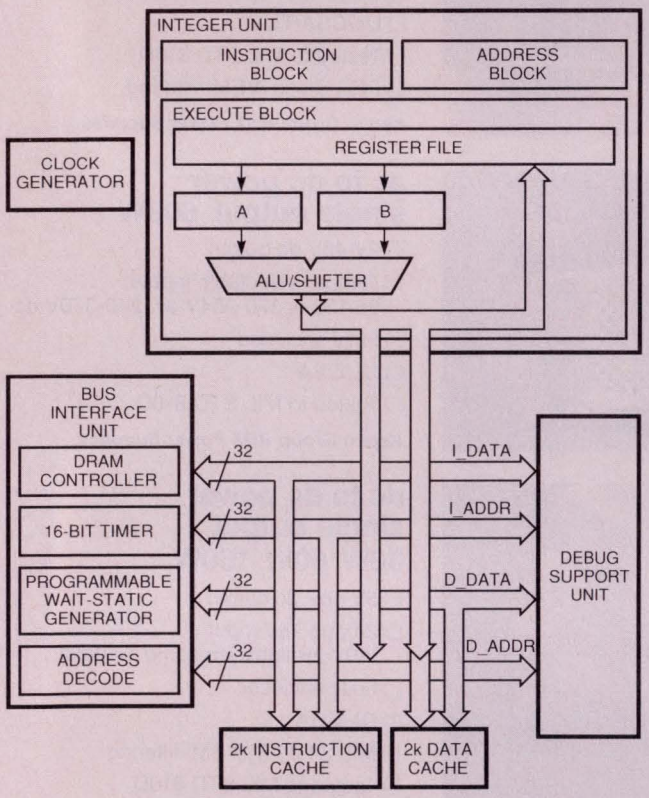
Cypress Semiconductor
Phone (408) 943-2852
Circle No. 397

Weitek Corp
Phone (408) 738-8400
Circle No. 399

Description: Sun Microsystems defined SPARC at instruction-set and programmer's model level and then entered into entirely separate joint agreements with silicon vendors with the intent of creating an open architecture.

Status: At least 25 vendors have signed up to produce SPARCstation 1 compatibles—it will be interesting to see how many actually deliver and succeed. Currently, more than 2000 applications run on SPARC hardware, and numerous Sbus plug-in cards are available. SPARC International (Sunnyvale, CA), a consortium of hardware and software vendors, creates and maintains open standards and multivendor compatibility of both SPARC-based machines and applications. Despite the growth in the workstation market, Bipolar Integrated Technology's (BIT) decision to discontinue general marketing of its ECL SPARC processor in favor of the Mips architecture is a blow. BIT will continue to support Floating Point Systems' integration of its ECL SPARC in the latter's supercomputer. BIT does plan to continue to entertain custom business using its SPARC core.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step). Logicals and shifts.

II—DATA-MOVEMENT INSTRUCTIONS
Load and store to memory (in RISCs, only simple loads and stores used to external memory). Load and store to CPU registers. Load and store to floating-point registers. Load and store to coprocessor registers.

III—PROGRAM-MANIPULATION INSTR
Call subroutine, branch conditional, save and restore, jump and link (128 hardware and 128 software traps, mostly user definable).

IV—PROGRAM-STATUS-MANIP INSTR
Read and write processor state register.

V—SYSTEM-LEVEL INSTRUCTIONS
Instruction-cache flush. Can set up system and user modes and associated protection. Fujitsu's core provides a SCAN instruction that performs post-normalization of FPU operations, interrupt handling, and compression.

Specification summary: Follows RISC philosophy of single-cycle instruction execution (averages 1.08 to 1.7 clocks per instruction). Family has a large number of on-chip registers to hold data being processed for rapid access, which also permits the fixed-length instructions to carry the two source and one destination addresses needed for single-cycle operations (register file has 3-port structure). On-chip registers are partitioned into 8 24-register groups that are overlapped at edges so CPU can pass parameters between them. There are also eight global registers.

Representative SPARC family microprocessors

Part Number	Vendor	Function	Speed (MHz)	Available	Price
CY7C605	Cypress	MMU and multiprocessor cache controller	25,33,40	Now	$1200 (100)
CYM6001	Cypress	MBus uniprocessor module	25,33,40	Now	$1400
CYM6003	Cypress	Multiprocessor MBus module —single CPU	25,33,40	Now	$1800
MB86902	Fujitsu	Embedded integer unit	20 and 25	Now	$87 (1000)
MB86930	Fujitsu	Embedded integer unit with cache, DRAM support	20,30,40	Now	$50 (1000)
MB86903	Fujitsu	Integrated SPARC with integer and floating-point units	33,40	Now	$275 (1000)
L64811	LSI Logic	Cypress-compatible integer unit	25, 40	Now	$160 (1000) $223 (1000)
L64815	LSI Logic	MMU, cache controller, cache-tag unit	25,33,40	Late '91	$177 (1000)
L64850	LSI Logic	MBus DRAM controller	25,33,40	Late '91	$149 (1000)
TMS390C602A	Texas Instruments	Floating-point unit	40	Now	$295 (1000)
W8701	Weitek	Integrated integer and floating-point unit	33,40	Now	$240 (5000)

Software note: There are four stages (five in Fujitsu's ASIC core) of pipelining. Optimizing compiler prevents pipeline breaks by inserting a delay instruction before branch instructions.

Hardware notes:
1. Diagram is for Fujitsu 86930 for embedded control. This device includes a hardware multiply and divide—overcoming the SPARC specifications failure to include such instructions. The vendor's 86903 offers an on-chip FPU.
2. Cypress's SPARC embedded controller eliminates the user-defined coprocessor port and several control signals in addition to reducing the address bus to 24 bits and the address-space identifier to 3 bits.
3. LSI Logic's embedded SPARC comes without coprocessor ports.
4. The W8701 features an on-chip floating-point coprocessor—it doesn't support external coprocessors. This version is available in 25-, 33-, and 40-MHz versions.

HARDWARE — SUPPORT — SOFTWARE

Sun workstations are adequate because Sun maintains software compatibility. Definicon (Newbury Park, CA) supplies development boards, Ironics (Ithaca, NY) offers a VMEbus board that supports multiprocessing. Cypress/Ross, Fujitsu, and LSI Logic have hardware-support programs that offer various levels of development support.
Evaluation Boards: Available from Cypress and Fujitsu.

Vendors say they'll pass along Sun's optimizing compilers for C, Pascal, and Fortran as well as Sun's Unix operating system. Wind River Systems (Emeryville, CA) will provide a real-time operating system. A SPARC monitor is available from Bradley Forthware (Sunnyvale, CA). Microtec Research (Santa Clara, CA) offers optimizing compilers, one of which is tuned for Fujitsu's ASIC core.

MIPS FAMILY

32-BIT CMOS

AVAILABILITY: See table.
COST: See table.
CORE: LSI Logic uses an ASIC implementation of the R3000A and offers the core in its standard-cell library. The core is binary-code compatible but adds a trace register and two breakpoint registers to assist software development.

Description: This RISC architecture was initially developed at Stanford University under the auspices of DARPA (Defense Advanced Research Projects Agency). The architecture supports as many as three tightly coupled processors. The R2000, R3000, R4000, and R6000 were developed by systems vendor, Mips Computer Systems. Although Mips doesn't sell the chips, standard and derivative μPs are available from five semiconductor suppliers.

Status: The R2000, R3000, R3000A, and R4000 are multisourced, specification-compatible RISC μPs. Such workstation companies as Digital Equipment Corp, Silicon Graphics, Sony, Mips, and the Advanced Computing Environment (ACE) have selected the architecture as the one to build their RISC-based hardware on. The R3000 was selected by JIAWG (Joint Internal Avionics Working Group) as a standard for military avionics programs such as the Advanced Tactical Fighter. The R6000 is available from BIT, although NEC and Sony are also R6000 licensees.

Bipolar Integrated Technology
Phone (503) 629-5490
Circle No. 400

Integrated Device Technology
Phone (408) 492-8333
Circle No. 401

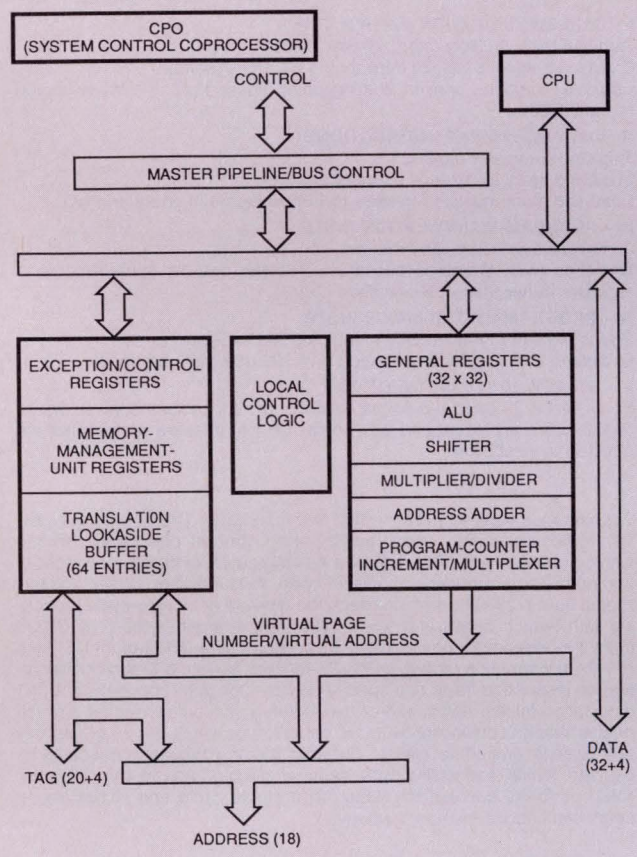
LSI Logic Corp
Phone (408) 433-8000
(800) 232-6477
FAX (408) 433-7447
Circle No. 402

NEC Electronics Inc
Phone (415) 960-6000
(800) 632-3531
FAX (408) 433-7447
Circle No. 403

Performance Semiconductor
Phone (408) 734-8200
Circle No. 404

Siemens Components Inc
Phone (408) 980-4500
Circle No. 405

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram reflects R3000 architecture.
2. LSI Logic's LR33000 offers two 24-bit down counters that are reloaded and restarted upon reaching zero. Both counters can trigger interrupts. You can enable one counter to count external events. An internal 12-bit counter is useful as a DRAM-refresh counter. The chip also features a write buffer, two chip selects, two programmable wait-state generators, an integrated DRAM controller, byte-gathering logic, and a 1x clock input.
3. The R6000 has a 5-stage, fully interlocked pipeline and supports cache control and memory management on chip. A tightly coupled coprocessor interface supports the R6010/B3110 floating-point coprocessor chip set.

I—DATA-MANIPULATION INSTRUCTIONS
Implements classic RISC load-store architecture where all data-manipulation operations occur on data in internal registers at the rate of one operation per cycle. Add, subtract, and logical operations, as well as multibit shifts, comparisons, and multiply and divide operations are in 3-operand format. The R6000 adds SQRT and rounding instructions.

II—DATA-MOVEMENT INSTRUCTIONS
External memory is only accessed for simple loads and stores. Load and store to CPU registers. Processor supports loading and storing of unaligned 32-bit data. The R6000 adds Load and Store Double Word to Floating-Point Coprocessor.

III—PROGRAM-MANIPULATION INSTR
Processor contains a rich set of instructions for program manipulation and operating-system kernels. Has coprocessor interface to the MMU to support the virtual-memory system. The processor also contains instructions to manage program-control flow. The R6000 supports Trap Conditional and Branch Conditional Likely instruction.

IV—PROGRAM-STATUS-MANIP INSTR
Exceptions can be initiated by interrupt, memory-access faults, and the floating-point coprocessor and are tracked by in-system control registers.

V—SYSTEM-LEVEL INSTRUCTIONS
Bits in the status register let the processor modify the system interface in order to perform memory-system diagnostics.

Specification summary: The R2000/R3000 implements a 5-stage pipeline to achieve a low average-clocks-per-instruction rate. Rich instruction set, sophisticated compilers, and high-frequency operation help the R2000/R3000 family achieve high performance. The IDT 79R3000 features a full cache controller, including on-chip tag comparison and direct control of the cache RAMs. LSI Logic's LR2000/3000/3000A includes 32 32-bit general-purpose registers, on-chip cache control, on-chip memory management, and coprocessor interfaces for as many as three external coprocessors. LR33000 offers 8-kbyte instruction cache and 1-kbyte data cache.

R2000/R3000 family microprocessors

Part Number	Vendor	Speed (MHz)	Price
79R3000	Integrated Device Technology (IDT)	12.5-33	As low as $50
LR3001	IDT	12.5-33	As low as $50
LR2000	LSI Logic	12.5-16	$99 (100)
LR3000*	LSI Logic	16-25	$144 (100)
LR3000A	LSI Logic	To 33	$400 (100)
VR3000A	NEC	33-40	$350 (1000)
VR3600A	NEC	33-40	$300 (1000)
PR3010A	Performance	25-40	$69 (100)
PR3400	Performance	25-40	$298 (100)
R3000	Siemens	20-25	$215 (100)
R3010A	Siemens	20-25	$215 (100)

HARDWARE — SUPPORT — SOFTWARE

MIPS Computer Systems offers several machines for system development. The architecture is supported by a variety of tools, including logic-analysis tools from Tektronix, Arium, and Gould. IDT offers a line of CPU subsystems. IDT and LSI Logic also offer a range of development systems. For the LR33000, Logic Modeling (Milpitas, CA) offers a hardware model, Embedded Performance (Santa Clara, CA) offers an ICE, and Neocad (Boulder, CO) supplies an AT board. NEC provides CPU module of pc board and TAB-based multichip module.
Evaluation Boards: LSI offers the Pocket Rocket self-contained evaluation board for 25-MHz development. The Speed Racer is an evaluation board that transforms the Pocket Rocket into a graphics terminal.

LSI Logic and IDT provide C, Ada, Pascal, Fortran, Cobol, and PL/1 compilers for their CPUs. LSI also offers the System Programmers Package, an integrated tool kit for software and hardware development.
The operating system RISC/OS is a merged AT&T System V.3 and Berkeley BSD 4.3 Unix including TCP/IP and NFS networking software. It includes the Mips optimizing compiler as well as the Mips symbolic debugger.
Refer to the RISCware directory from Synthesis Software Solutions Inc for a complete list of third-party software vendors.

29000 FAMILY

32-BIT CMOS

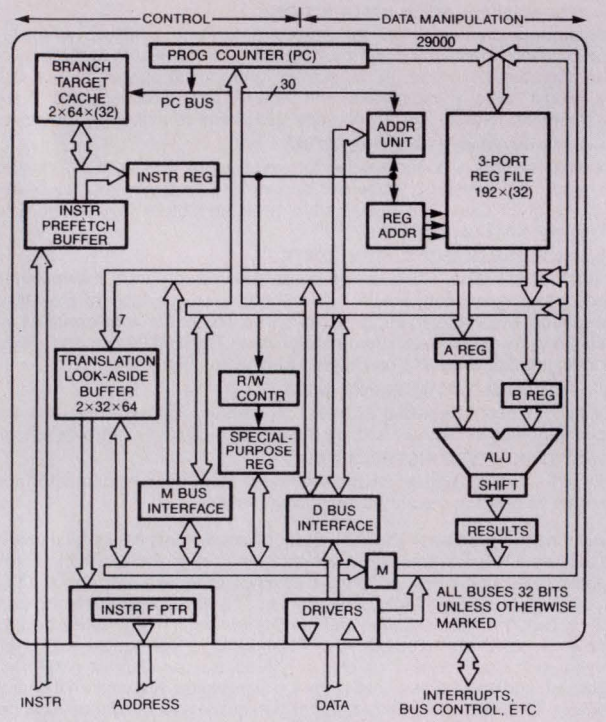
AVAILABILITY: Now for the 29000, 29050, and 29005. Both the 29030 and 29035 are scheduled for January 1992.
COST: $50 for the 16-MHz 29005, $79 for the 16-MHz 29000, $198 for the 20-MHz 29050, $89 for the 16-MHz 29035, and $130 for the 25-MHz 29030 (1000).
SECOND SOURCE: Under negotiation.

Advanced Micro Devices (AMD)
Phone (408) 732-2400
For more information, Circle No. 406

Description: State-of-the-art implementation of RISC μP concepts with expected stress on obtaining as close to single-cycle operation as possible (even with branching). The family also emphasizes keeping users' system costs down by using slower bus timing, etc, to lower memory-subsystem cost. Although their names are similar, the 2900 and 29300 building-block families are intended for user-defined (microcoded) complex instruction sets. The 29000 μP family has a regular, fixed, and purposely simple instruction set; moreover, the instruction set is decoded by logic. Companion compilers are an essential part of family.

Status: In the 3½ years since its introduction, the 29000 has accumulated over 350 design wins. Areas of particular success for the RISC μP are high-end laser printers; X-terminals; graphics, including graphics controller boards, graphics accelerators, real-time image processing, and medical imaging; and network products, including protocol converters, network node controllers, FDDI networks, and ISDN-related systems.

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step), divide (step).
Extract contiguous 32 bits from the 64-bit funnel shifter.
Logicals, compare, convert floating point (floating point is implemented in the 29050).

II—DATA-MOVEMENT INSTRUCTIONS
Register-to-register moves.
Load and store to external memory and I/O.
Load and store multiple registers to/from external memory and I/O.

III—PROGRAM-MANIPULATION INSTR
Jump, call subroutine, and returns.
Branches (with decisions based on Boolean data in general-purpose registers rather than ALU condition codes).

IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition.
Exception handling for 64 reserved and 192 user-defined traps.

V—SYSTEM-LEVEL INSTRUCTIONS
Some of the 23 special-purpose registers are for system control. These registers are protected and can be set up via software (some also are affected by execution).

Specification summary: 32-bit CPU fashioned after RISC concepts; performs most frequently used, simple instructions in one cycle. Offered with companion compilers that take advantage of architectural simplicity and produce performance-optimized code. Features that ensure uninterrupted flow in 29000's 4-stage execution pipeline are single-cycle branching with branch delays and a 512-byte branch-target cache (The 29030 uses a more-conventional 8-kbyte instruction cache and the 29035 uses a 4-kbyte instruction cache). Main 192-register file has a 3-port configuration so instruction fields can specify sources for both operands and the destination for the result. 128 of the registers are addressed by a stack pointer that (in conjunction with the compiler) provides a type of caching that speeds procedure calling. External memory space is reached by 4-Gbyte virtual addressing with demand paging. An on-chip 64-entry MMU performs address translation in a single cycle and is flexible so users can choose memory strategy.

Hardware note:
1. Burst-mode addressing allows use of lower-cost video RAMs to replace more-expensive, high-speed, static CMOS RAMs, with only moderate loss in performance (14 MIPS sustained vs 17 MIPS).

Software notes:
1. Total of 115 (117 in the 29030) instructions. All are not yet implemented in hardware; those that aren't cause traps.
2. Multiply and divide on the 29000 only does one step. The full multiply and divide instruction causes a trap operation at which a compiler can insert a software routine.

HARDWARE SUPPORT SOFTWARE

The EB29k is a PC plug-in execution board with software-development tools. **From others:** Embedded Performance Inc, Hewlett-Packard, and Step Engineering all provide real-time in-circuit emulators for the 29000 family. Logic Analyzer interface is available from Biomation or Hewlett-Packard. Various VMEbus board products based on the 29000 are available from Ironics. Behavioral simulation models are available from Logic Automation and Mentor Graphics. Design-verification and test-generation models are available from Teradyne. A list of third-party support products appears in the biannual Fusion29K Catalog published by AMD.

AMD supplies the complete software tool chain. These tools include the ANSI standard HighC29k optimizing compiler with an assembler, linker, and ANSI standard libraries; floating-point-math libraries; and architectural and instruction-set simulators. The Xray29k source-level debugger is also available for the 29000 and the 29030. The Mon29k is a target debug monitor for system developers. All software support tools run on IBM PC/ATs and Sun-3 and Sun-4 workstations.
Other C compilers are available from Embedded Performance Inc, Metaware, Microtec, and Intermetrics. Pascal compilers are available from Metaware. The GNU tool chain, including the C++ and the debugger are available from Cygnus. Ada is available from Verdix Systems. Fortran is available from Yarc. Ready Systems, JMI, and Telenetworks provide real-time operating systems. A complete guide to third-party software products is published in the biannual AMD Fusion29k catalogue.

Text continued on pg 179

i960

32-BIT CMOS

AVAILABILITY: Now for 10-, 16-, 20-, and 25-MHz 960KA and KB in PGAs; 16- and 20-MHz plastic quad flatpack (PQFP); 16-, 20-, and 25-MHz 960MC in PGAs and QFPs; 16-, 25-, and 33-MHz 960CA in PGA; 16- and 25-MHz 960CA in PQFP; 10- and 16-MHz i960SA and SB in PQFPs and 10-MHz devices in QFPs; and 16-, 20-, and 25-MHz MCs and XAs in PGAs and QFPs.

COST: Prices depend upon speed, package, and temperature range. In 1000s, prices range from $19 to $23 for the SA, $25 to $31 for the 960SB, $27 to $56 for the 960KA, $35 to $73 for the 960KB, $638 to $1040 for the 960MC, and $81 to $122 for the 960CA.

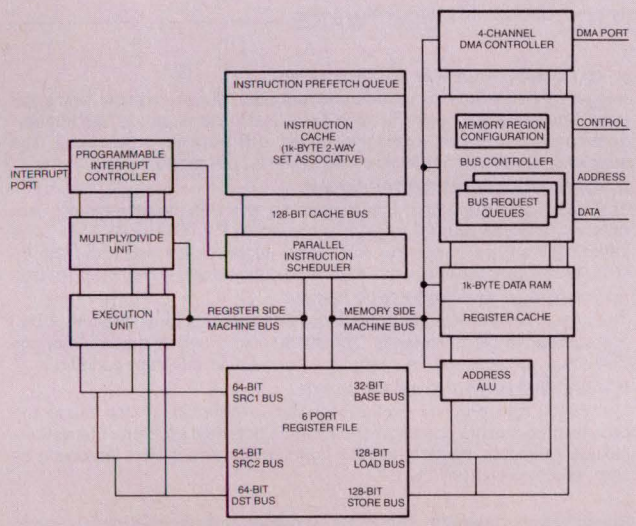
SECOND SOURCE: Internally sourced from three different Intel facilities.

Description: The 960 is Intel's 32-bit family of μP chips that has been designed specifically for embedded-control applications. There are seven upwardly compatible versions of the RISC-based architecture. The SB and KB versions add on-chip floating-point units to the basic capabilities afforded by the SA and KA. The CA features a software-configurable pipelined bus; 1.5 kbytes of data RAM; a 1-kbyte, 2-way set associative instruction cache; and a 4-channel DMA controller. The MC offers a floating-point unit, a virtual-memory-management unit, Ada tasking and multiprocessor support. Finally, the XA adds data security and an object-oriented addressing scheme.

Intel Corp
Embedded Controller Operation
Phone (602) 961-8051
For more information, Circle No. 408

Status: Since its introduction, the 960 family has enjoyed widespread acceptance in a broad spectrum of commercial and military designs. The 960 family played a role in legitimizing the 32-bit embedded-control market, finding application in X terminals, laser printers, and communications systems. Selection of the architecture as the 32-bit standard for military avionics has also fueled the family's growth. Intel's approach is family oriented; not only is there a range of 32-bit CPU chips at different price and performance levels, but there are also 960-specific support components such as the 27960 burst EPROM and 85C960 bus control component. Intel claims the total kit approach exists to serve embedded-control customers with an easy-to-design-with set of CPU and peripheral parts.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The 960 provides only one data bus for instructions and data. The bus multiplexes address and data information. The basic 960 chip includes sixteen 32-bit global registers and sixteen 32-bit local registers. The stack requires one global and three local registers for housekeeping operations. 2. The floating-point unit also includes four 80-bit registers, but can use any register. 3. On the CA, an on-chip 4-channel DMA controller and programmable wait-state generator allow reductions in system logic and cost.

I—DATA-MANIPULATION INSTRUCTIONS
Bit operations, unsigned and signed byte, unsigned and signed half-word (16-bit quantity), unsigned and signed word operation. All CPUs have hardware multiply/divide unit. Extended arithmetic support allows math operations on operands larger than one word. Floating-point operations on single-, double-, and extended-precision operations are supported in hardware on the -KB and -MC versions.

II—DATA-MOVEMENT INSTRUCTIONS
Bytes, half words, words, double words, triple words, and quad words can be moved to and from memory. Memory operations are supported by a full complement of addressing modes, including IP relative. All CPUs support unaligned memory operations.

III—PROGRAM-MANIPULATION INSTR
Both Berkeley and Stanford forms of subroutine call, return; several types of branch instructions. Full set of conditional tests.

IV—PROGRAM-STATUS-MANIP INSTR
Process control word and arithmetic controls can be modified under program control.

V—SYSTEM-LEVEL INSTRUCTIONS
Seven different types of trace controls. Hardware and software breakpoints. 960CA has operations to program DMA channels and control hardware features such as locking the cache. 960MC has operations to support shared-memory multiprocessing directly.

Specification summary: The 960SA and KA have a 512-byte instruction cache, a 256-byte register cache, and a 4-input interrupt controller. The 960SB and KB are socket compatible with the SA and KA, respectively, but feature an on-chip IEEE-P754-compatible floating-point unit. The CA allows multiple instruction-per-clock execution and offers a 4-clock-cycle, 32-bit multiplier, 8 interrupt inputs, a 1-kbyte lockable instruction cache, 1.5 kbytes of on-chip RAM, register cache configurable to 15 levels, 4 DMA channels, and a software-configurable bus. The MC adds an MMU and multiprocessing support to the features of the -KB. The XA adds to the MC hardware-enforced data security through the use of the object-oriented addressing.

Software notes:
The 960 architecture is based on a single flat address space with all I/O memory mapped. All 960 processors feature thirty-two 32-bit orthogonal registers and utilize a load-store architecture with 3-operand instructions plus complex addressing modes. The architecture is based on scoreboarding techniques permitting object-code compatibility across a range of implementations with no branch delay or load delay slot padding.

HARDWARE — SUPPORT — SOFTWARE

From Intel: The ICE960SB and KB in-circuit emulator (both $16,495) are available for the 960SA/SB and KA/KB. The ICE960MC ($24,995) supports both the 960MC and XA.
The 85C960 is a bus-control chip for the KA/KB; the 27960CX/KX are high-speed burst EPROMs for the 960KA/KB/CA; the 27C202 is a high-speed, 16-bit-wide EPROM for the 960KA/KB/CA. The 82380 is a multifunction peripheral with timer-counters, eight channels of DMA, and 15 interrupt inputs that can interface to the 960KA/KB/MC.
From others: 960CA Multibus II boards are available from Micro Industries. 960CA VME boards are available from Heurikon and Tadpole.
Evaluation Boards: The EVQT960E ($960) with 256 kbytes of 2-wait-state memory and the EVQT960F ($1960) with 256 kbytes of zero-wait-state memory are serially hosted evaluation and prototyping boards for the 960KA/KB. The EVA960KB ($4500) is IBM PC/AT compatible with on-board debug monitor and as much as 4 Mbytes of DRAM. The EXV960MC ($9000) is a 25-MHz Multibus I development board for military and Ada applications. The EV960CA ($3500) is an evaluation board for the 960CA.

From Intel: ASM960 ($900 for the IBM PC/AT) includes an assembler and linker for the 960 family. C tools 960D ($2000) includes the ASM960. Hosts include the IBM PC/AT, Sun-3, VAX/VMS VAX/Ultrix and HP9000. Ada960 (from $28,000) is available for VAX/VMS. DBSIM960 ($3500) is a real-time kernel for 960SA/KA/CA. SIM960CA ($750, IBM PC/AT) is a software simulator for the 960CA. DB960 ($2500) is a C source-level debugger hosted on a IBM PC/AT for the 960SA/KA/CA.
From others: Wind River Vxworks provides a full-featured operating environment that includes file-system support and TCP/IP networking. Ready Systems VRTX32 provides a deterministic real-time kernel for the 960 family. Microtec Research provides a complete 960 tool chain—C compiler through XRay debugger. QTC provides an instruction scheduler/optimizer for the 960CA. The Solutions960 catalog from Intel describes additional 960 tools and applications.

88000

32-BIT CMOS

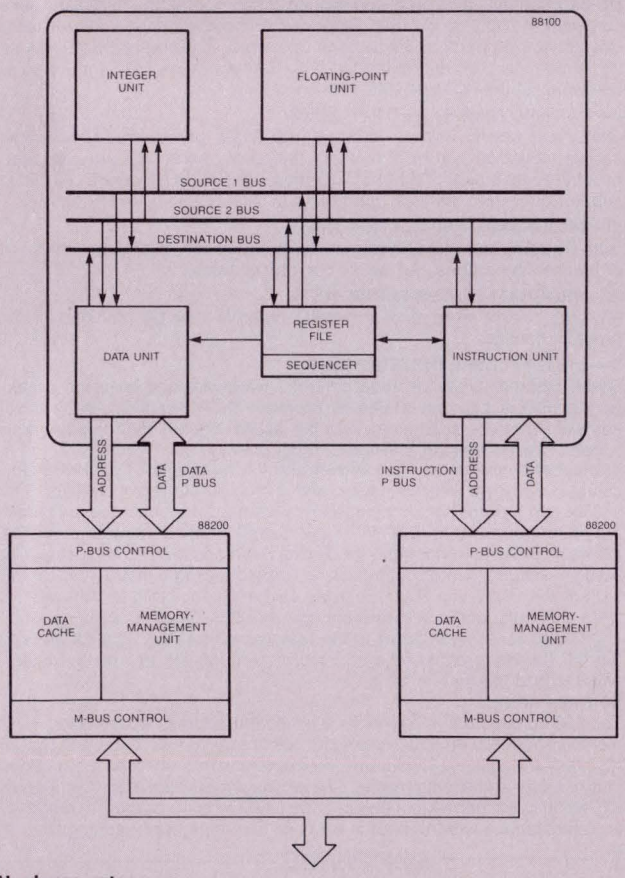
AVAILABILITY: Both the 88100 CPU and the 88200 cache/memory-management unit (CMMU) are available now in 16-, 20-, 25-, and 33-MHz versions. The 88204 is available at 25 MHz.
COST: In 1000 qty, the 16-MHz 88100 costs $49; the 88200 costs $75. The 33-MHz 88100 costs $150 and the 88200 costs $199. The 88204 costs $495.
SECOND SOURCE: None.
CORE: Motorola's architecture can incorporate as many as six special-function units into the 88100 chip.

Motorola Inc
Microprocessor Products Group
Phone (512) 928-6000
For more information, Circle No. 407

Description: The 88000 RISC family encompasses the 88100—the CPU and FPU—and the 88200 and 88204—the memory-management units. The 88100 chip supplies full 32-bit registers, data paths, and addresses. Most instructions, including standard IEEE-P754 floating-point math operations, execute in one cycle or are put in a concurrent execution pipeline in one cycle. The corresponding 88200 cache/memory-management unit supports a demand-paged virtual-memory environment. Where the 200 offers 16-kbyte, 4-way set associative cache support, the 204 extends the support to 64 kbytes of cache. Both MMU chips control two 4-Gbyte logical address spaces—one for the user and one for the supervisor. The chip's architecture supports multiprocessor operations.

Status: The 88000 μP family is designed into such applications as PC add-in cards, disk controls, imaging systems, and real-time controllers. An independent group of manufacturers has founded the 88open Consortium Ltd (San Jose, CA) to support and promote the μP family. The consortium develops standards such as the Binary Compatibility Specification, which allows applications written for the 88000 to execute on all 88000 hardware. The architecture suffered a big blow when Apple Computer, which was considering the 88000 family for its future RISC-based products, entered into an agreement with its Big Blue competitor (IBM) to use IBM's RISC processor.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Architecture shown is for the 88100. The CMMUs are shown in block-diagram form.
2. The P bus supplies the interface between the 88100 and either local memory or an 88200 CMMU. The synchronous P bus operates at the same clock rate as the 88100. Peak data rate is 80 Mbytes/sec.
3. The 88100 includes 32 general-purpose registers.

I—DATA-MANIPULATION INSTRUCTIONS
Integer-math instructions include add, subtract, divide, multiply, and compare. There are equivalent floating-point instructions as well as integer-float conversion, store, exchange, round, and truncate instructions. The instructions also provide logical and bit-field operations.

II—DATA-MOVEMENT INSTRUCTIONS
The basic data-movement instructions let the CPU load registers, addresses, and the control register's contents. The CPU can also store information and exchange the contents of registers and memory. The instruction set includes operations that move data within the floating-point unit.

III—PROGRAM-MANIPULATION INSTR
These instructions include conditional and unconditional branch, jump, and subroutine-call commands. The 88100 also provides trap instructions that check bit locations, memory boundaries, and interrupt conditions.

IV—PROGRAM-STATUS-MANIP INSTR
The 88100 can process exceptions—those conditions that cause the processor to stop its operation and locate a potential problem. Exceptions include interrupts, memory-access faults, math errors such as divide by zero, and trap instructions.

Specification summary: The 88100 provides register-to-register operations for all data-manipulation instructions. Separate source and destination registers are available. The CPU supports register-to-register and register-plus-immediate-value address modes. Because address calculations are quick, memory-access operations are speedy, in keeping with the RISC philosophy. The CPU employs delayed branching, which reduces pipeline delays caused by a change in program flow. The 88200 incorporates 16 kbytes of cache memory as well as cache-control logic, memory-management logic, and bus-control circuits. Multiple CMMUs can operate in parallel. Both the 88100 and 88200 come packaged in 180-pin PGA packages. The chips operate over the 0 to 70°C temperature range.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: The company has announced a variety of VMEbus-based boards and systems.
From others: Add-in boards are available for the IBM PC/AT from Opus (Cupertino, CA), for the IBM PS/2 from Prometa (Gainesville, FL), for the Apple Macintosh from Tektronix (Beaverton, OR), for the VMEbus from Force (Campbell, CA) and Tadpole (Cambridge, UK), and for the VAX from Avalon (Santa Barbara, CA).

From Motorola: 88000 systems run Motorola's BCS/OCS Unix System V, Release 3 as well as System V, Release 4, both of which are supported by optimizing C and Fortran compilers and associated development tools for complete software development.
From others: Various compilers and applications are available for the 88000. See the 88open software catalog.

i860

64/32-BIT CMOS

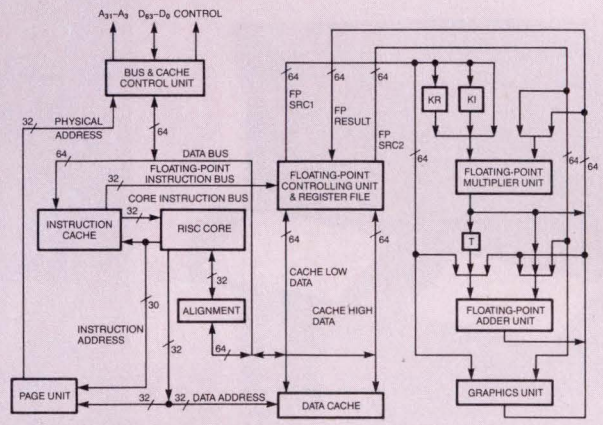
AVAILABILITY: The 25-, 33-, and 40-MHz 860 XR versions are available now. The 40- and 50-MHz i860 XP, 82495 cache controller, and 82490 cache RAM will be in production late this year.
COST: The cost of the i860 XR ranges from $172 for the 25-MHz XR to $495 for the 40-MHz i860 (1000). The i860 XP ranges from $560 to $699 (1000). The 82495 XP costs $176 (1000). The 82490 costs $40 (1000).
SECOND SOURCE: None.

Intel Corp
Supercomputing Components Operation
Phone (408) 987-8080
For more information, Circle No. 409

Description: The i860 CPU is a 64-bit μP designed to provide balanced performance across integer, floating-point, and 3-D graphics operations. The μP incorporates a RISC integer unit, a floating-point adder, a floating-point multiplier, an 8-kbyte data cache, a 4-kbyte instruction cache, paging functions, an MMU, and a 3-D graphics unit. The i860 runs Unix but is not designed to run 386 software. The 82495 XP provides bus snooping hardware and a cache protocol that enables cache consistency between multiple processors, as well as between primary and secondary caches. The 82490 32-kbyte cache RAM integrates write-back and snoop buffers.

Status: The i860 has amassed more than 250 design wins to date in supercomputer, minicomputer, 3-D graphics workstation, and application accelerator designs. Unix System V, Release 4.0, as well as hardware and software development tools for the 860 XR CPU are available now and will support 860 XP software development. Unix tools and compilers specifically designed for the 860 XP processor will be available later this year.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Integer arithmetic, logicals, and shifts. Integer multiply. IEEE-754 floating-point add, subtract, multiply. Single and double precision, and conversions between. Reciprocal and square-root seed instructions. Special "dual operation" floating point allows two operations per clock. Graphics instructions for pixel interpolation and Z-buffer check.

II—DATA-MOVEMENT INSTRUCTIONS
Floating-point 16-, 8-, and 4-byte loads and stores with variable strides and autoincrement. Four-, 2-, and 1-byte integer loads and stores. Transfers between integer and floating-point registers. Special load instruction assists data caches. Pixel-store operation of 8 bytes.

III—PROGRAM-MANIPULATION INSTR
Unconditional and conditional branches, both delayed and nondelayed forms. Single-cycle loop-control operation. Indirect call and indirect branch. Dual-instruction mode allows execution of two instructions per clock.

IV—PROGRAM-STATUS-MANIP INSTR
Data-breakpoint register for breakpoint debugging. Big-endian mode bit switches between access modes. Cache-control bits for cache locking and testing.

V—SYSTEM-LEVEL INSTRUCTION
Lock/unlock instructions for semaphores. Flush instruction for write-back data cache. Single-cycle translation look-aside buffer and instruction cache invalidate.

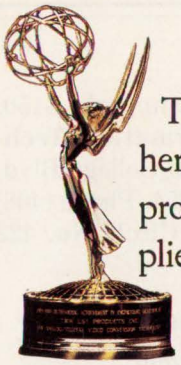
Specification summary: The i860 is a superscalar μP that contains three execution units: an integer unit and two floating-point units. The processor features two caches: a 4-kbyte instruction cache and an 8-kbyte data cache on the XR and two 16-kbyte I and D caches on the XP. The XP supports the MESI (modified, exclusive, shared, invalid) protocol for multiprocessing-system cache coherency. The family uses an external 64-bit data bus and internal instruction-cache bus and an internal 128-bit data-cache bus. Both processors meet ANSI/IEEE 754-1985 for binary floating-point arithmetic. The XR contains an on-chip debug register. The 860 XP adds a memory-management unit (MMU) that handles 80386-and 80486-compatible 32-bit addressing, a 64-bit external data path, supported by posted writes, a three-stage read pipeline, and a one-clock burst bus. A concurrency control unit permits applications compiled for parallel execution to run on either single or multiple 860-based systems.

HARDWARE — SUPPORT — SOFTWARE

From others: Logic Automation (Beaverton, OR) provides a software model, and Logic Modeling (Milpitas, CA) and Racal Redac (Westford, MA) offer hardware models.
From Intel: ASM/Tools, C compiler with vectorizer, PAX C, PAX Fortran, Debugger, IGL Graphics Library. C compiler, assembler, utilities, and retargetable symbolic debugger sell for $4000. Macro assembler with utilities and retargetable symbolic debugger costs $2000.

From others: C compilers are available from Metaware (Santa Cruz, CA), Microway (Kingston, MA), and ATT PCC (Warren, NJ). Lahey, Microway, PGI, Green Hills, Compass, and Hipersoft supply Fortran compilers. Microway also offers Pascal and C++ compilers. An Ada compiler is available from Verdix. Magnus, K&A, and ATC Grafpak supply numerical libraries.

WITH TRW'S VIDEO ENCODER, ANYONE CAN PRODUCE PROFESSIONAL VIDEOS WITHOUT HOLLYWOOD BUDGETS.

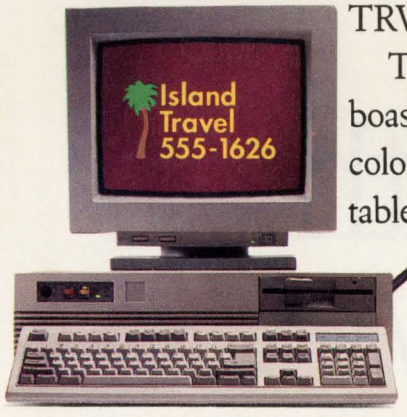


1988-1989 Emmy Award

Lights. Camera. Action. The monolithic Video Encoder is here. Created by TRW, the film and production industry's leading supplier of high-performance ICs. And the only company ever to be awarded an Emmy for its video IC technology.

Now, TRW brings you the first in its new line of affordable multimedia ICs for desktop video: The TMC22090.

And that means converting RGB, YUV or color-indexed computer images and graphics into studio-quality NTSC, PAL or S-Video signals can now be done with a single, low-cost chip. One fabricated in TRW's Omicron-C™ 1 μ CMOS process. Packaged in an 84 lead PLCC. And, of course, designed with the full-spec performance that is synonymous with TRW standards.



The TMC22090 boasts a 256x8x3 color lookup table, a pixel mask register and compatibility with 171 and 176 RAMDACs. All of which means transparent interface with existing device drivers.

Better still, the high performance Hollywood has come to rely on is provided by 4:4:4 digital encoding, oversampled 10-bit outputs, and built-in test signals. The TMC22090 even gives you a JTAG interface for low cost production testing. So for everything from simply providing an affordable video output for computer display boards, to developing complex desktop video workstations, you can design in confidence. With the video encoder from the leader in video ICs: TRW.

Overlay graphics and titles onto video by selecting a transparent color for the Video Encoder chroma key.

And you can count on TRW to keep you at the forefront of multimedia, too. This Video Encoder, after all, is just our debut. We've got some great sequels in development.

For data sheets, applications and other information on TRW's TMC22090 Video Encoder, as well as to be first in line for coming attractions, call or write today:

TRW LSI Products Inc.,
P.O. Box 2472, La Jolla, CA 92038
(619) 457-1000, FAX (619) 455-6314
(800) TRW-LSIP (800) 879-5747

TRW

TRW LSI Products Inc.

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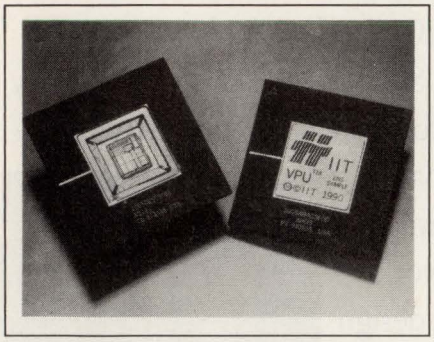
CIRCLE NO. 104

NEW PRODUCTS

INTEGRATED CIRCUITS



Video Compression Chip

- *Microcode programmable*
- *Handles JPEG, MPEG, and CCITT standards*

Featuring a microcode-programmable architecture, the Vision Processor (VP) can execute a variety of still-frame and motion-compensated compression and decompression standards. The VP handles standards such as JPEG (Joint Photographic Experts Group) for still images, MPEG (Motion Picture Experts Group) for high-quality full-motion video, and CCITT Px64 for video communications. The chip is optimized to perform the discrete cosine transform (DCT) and motion compensation. It executes all forward and inverse stages of the algorithms including DCT, quantization, zig-zag scanning, run/amplitude coding, motion estimation and compensation, and image filtering. The company provides the microcode to support JPEG, MPEG, and Px64 standards. In communications applications such as video conferencing, the processor can perform real-time encode/decode using the Px64 standard for 2000:1 compression ratios of full-motion video at 30 frames/sec. The VP is available in 144-pin pin-grid arrays and plastic quad flatpacks (PQFP) and 84-pin PQFPs. VP for JPEG-only operation, \$60; for JPEG, MPEG, and Px64 support, \$150.

Integrated Information Technology, 2445 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 727-1885. **Circle No. 422**

Low-Power Static RAMs

- *1-μA standby current*
- *0.6-μA data-retention current*

The LH5168 8k×8-bit and LH51256 32k×8-bit low-power static RAMs (SRAMs) feature a maximum standby current of 1 μA and a data-retention current of less than 0.6 μA. When used in battery-back-up applications, the SRAMs can provide standby storage for 10 years or more from a single button-cell lithium battery. Both chips have an access time of 100 nsec. The LH5168 is available in 300- and 600-mil DIPs and 450-mil SO packages. The LH51256 is available in a 600-mil

DIP and 450-mil SO packages. LH5168, $2.54; LH51256, $14.46 (1000).

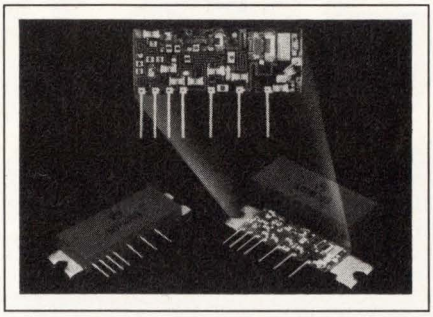
Sharp Electronics Corp, 5700 Pacific Rim Blvd, Suite 20, Camas, WA 98607. Phone (206) 834-8909.

Circle No. 423

UHF Power Module

- *Power output is 2.3W*
- *Needs only 2 mW of drive*

Designed for use in portable cellular radios such as the C-NETZ cellular system in Europe, the MHW703 UHF power module operates from a 7.5V supply. The module is also applicable to other communications systems that require power amplification at 450 to 460 MHz. It features an output power of 2.3W and needs only 2 mW of input drive. Samples and small quantities of the module are available from stock; production quantities have a 12-week lead time. $43.90 (25).



Motorola Inc, E-114, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3818. FAX (602) 244-4597. **Circle No. 424**

Monolithic Diode Array

- *Provides 8-kV ESD protection*
- *Replaces RC/diode networks*

Packaged in a 16-pin DIP, the SP270 provides 8-kV ESD and overvoltage protection for as many as 14 inputs. Conventional RC/diode networks, which provide only 2-kV protection, typically require 28 discrete diodes, 14 resistors, and 28 capacitors. The diodes have SCRs that activate in an electrostatic discharge event and dissipate very little energy. In addition, the SCRs speed up the response of the protection diodes, which exhibit a typical rise time of 6 nsec. The diodes provide protection by clamping the inputs to $1V_{be}$ above the supply voltage for positive overvoltage, or $1V_{be}$ below ground for negative overvoltage. The monolithic array of 14 diode pairs features a 1A current rating and a 5 to 28V supply-voltage range. $1.10 (1000).

Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1250; (407) 724-3704.

Circle No. 425

Killer Specs.

Panther® SCSI

Stalking system performance is your goal. That's why Maxtor's 1.2GB SCSI Panther was designed to perform a data seek in just 13ms. No other drive in its class features such lightning speed.

Panther's hunting prowess of 2ms track-to-track seek time stands out compared to Seagate's Wren 7 seek time of 2.5ms. And Panther outruns the competition with a 30Mb/sec. internal transfer rate.

Experience counts. Panther uses the reliable head disk assembly used in the Maxtor XT-8000, which boasts more than 300,000 units in the field. Panther shreds the competition with the widest range of available controllers, an MTBF of 150,000 hours, Novell certification and a highly competitive price.

Call about the full line of Panther drives that range from 1.2GB to more than 1.7GB capacity. If you're stalking performance, check out Panther's killer specs. *Call your nearest Authorized Maxtor Distributor.*

1GB-plus Disk Drive Comparison Criteria	Maxtor Panther P0-12S	Seagate Wren 7
Capacity (unformatted)	1.2GB	1.2GB
Seek Time	13ms	15ms
Track-to-Track	2ms	2.5ms
Internal Transfer	17.4 to 29.7Mb/s	15-23Mb/s
Maximum Seek	26ms	34ms

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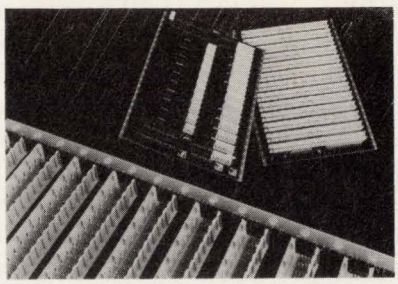
CIRCLE NO. 105

NEW PRODUCTS

COMPUTERS & PERIPHERALS



Futurebus+ Backplane

- *Conforms to the Profile F, IEEE P896.2 specification*
- *Supports 128-bit data transfers*

The Futurebus+ backplane conforms to the Profile F, IEEE P896.2 specification. The 16-layer backplane has 13 slots on a 30-mm pitch and supports 128-bit data transfers and central arbitration. The board arranges surface-mount, 33Ω resistors and high-speed capacitors to compensate for varying signal-path trace lengths and to minimize skew. Multiple power and ground planes protect bus circuitry from ground bounces. The backplane supports central arbitration by interconnecting the lower pins of connector E and all the pins through connector X of slot 1 to the respective pins on all the other slots. The board conforms to the mechanical specifications of IEEE 1301.1 and accepts hard-metric Futurebus+ cards measuring 265 × 288 mm. $2000.

Bicc-Vero Electronics Inc, 1000 Sherman Ave, Hamden, CT 06514. Phone (203) 288-8001. FAX (203) 287-0062. **Circle No. 426**

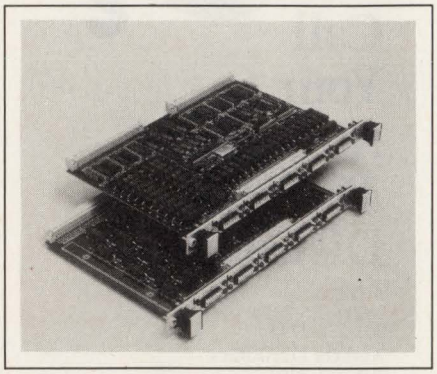
STD 32 Bus System

- *Has multiple DOS SBCs sharing a single backplane*
- *Virtual Video gives user access to several CPUs*

The STD 32 Star System allows multiple DOS-based single-board computers (SBCs) to share periph-

erals on a common STD32-compatible backplane. The system contains the company's ZT 8910 SBC, which has a 16- or 20-MHz 386SX μP, one parallel port, two serial ports, and 2 or 4 Mbytes of RAM. The chassis can also house as many as six ZT 8901 SBCs, having a 16-MHz V53 μP, three serial ports, 48 digital I/O lines, 1 Mbyte of RAM, and 512 kbytes of PROM. A Virtual Video feature permits the terminal and keyboard interfaces to be switched from one CPU to another by means of a "hot key" sequence. Virtual Video gives the user access to any of the CPUs. For example, a user can toggle from one CPU running Borland's turbo debugger and another running Microsoft QuickBasic. From $4015.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088.
Circle No. 427



VMEbus Test Boards

- *Package consists of load boards and slot-bypass cards*
- *Vary the current in each voltage line from 0.5 to 2A.*

A family of load boards and slot-bypass cards are available for testing a VMEbus system. The load boards can vary the current on each VMEbus voltage line from 0.5 to 2A. The front panel has LEDs and test points for each voltage line. Programmable drivers on the

boards send arbitrary signal waveforms over the backplane. An active version can switch the system-clock frequency to 8, 16, 32, or 64 MHz via front-panel control. You can direct the clock frequency to any line on the backplane. The slot-bypass cards are available in 3U, 6U, and 9U sizes and have E-Z-Ject handles for quick ejection. The cards provide a bypass of the Bus Grant signal and interrupt jumpers for any unoccupied VMEbus slot. The cards have an RFI shield on both sides, and an Air Dam restricts air flow through the empty slot. Load boards, from $249; slot-bypass cards, from $33.

Electronic Solutions, 6790 Flanders Dr, San Diego, CA 92121. Phone (800) 854-7086; (619) 452-9333. **Circle No. 428**

SPARC Processor Board

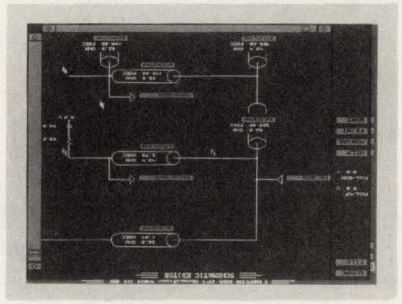
- *Provides 2-D and 3-D color graphics*
- *Contains 40-MHz SPARC μP and 16 Mbytes of RAM*

The SPARCengine IPX SPARC processor board contains a 40-MHz SPARC μP, network functions, and a graphics accelerator. It delivers 28.5 MIPS and 4.2 Mflops, which are equal to 24.2 SPECmarks. The company integrated its GX accelerated graphics hardware in an ASIC to provide 2-D and 3-D color graphics in embedded and real-time applications. The board contains a cache memory, two SBus expansion slots, a SCSI port, an audio port, two RS-232C ports, a floppy-disk-drive port, and an Ethernet port. The 9×9.7-in. CPU board comes with 16 Mbytes of RAM, which is expandable to 64 Mbytes. The board runs the Solaris operating system, the company's ONC networking software, and Openwindows software. $9000.

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (800) 821-4643; (415) 960-1300. **Circle No. 429**

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS



Interactive Transmission-Line Simulator

- *Analyzes critical traces before layout*
- *Graphical interface*

Linesim Pro provides a highly interactive tool for critical path analysis for transmission line effects. Running on a 386/486 PC, the tool provides a pop-up graphical interface to a transmission line simulator. With Linesim Pro's graphical, pop-in schematic, engineers can define their critical nets and then simulate them to predict transmission line behavior. This enables engineers to test their circuits before pc-board layout and modify the layout design as needed. The interface includes interactive, popup tools for calculating board trace impedances, creating or modifying circuit models, and adding terminators. The tool can handle large clock nets and backplanes, and it models microstrip, stripline, and asymmetric stripline geometries. For ease of use, the simulation results are displayed in an oscilloscope-like form. It requires 2 Mbytes of extended memory. $995.

HyperLynx, Box 3578, Redmond, WA 98073. Phone (206) 896-2320. **Circle No. 419**

Visual Programming Kit For Industrial Control

- *Graphic, object-oriented control language*
- *Develops control programs with no coding*

The Gello (Graphically Enhanced Ladder Logic) system overcomes traditional programming barriers with a fully graphical, visual programming system. Gello is aimed at industrial control applications and comprises an interactive, graphical programming environment and a run-time execution engine, Gellix. Using predefined function blocks, engineers can define programs as collections of graphic elements; each collection breaks down into sets of linked functional blocks. These blocks are executed by the Gellix engine, which functions much

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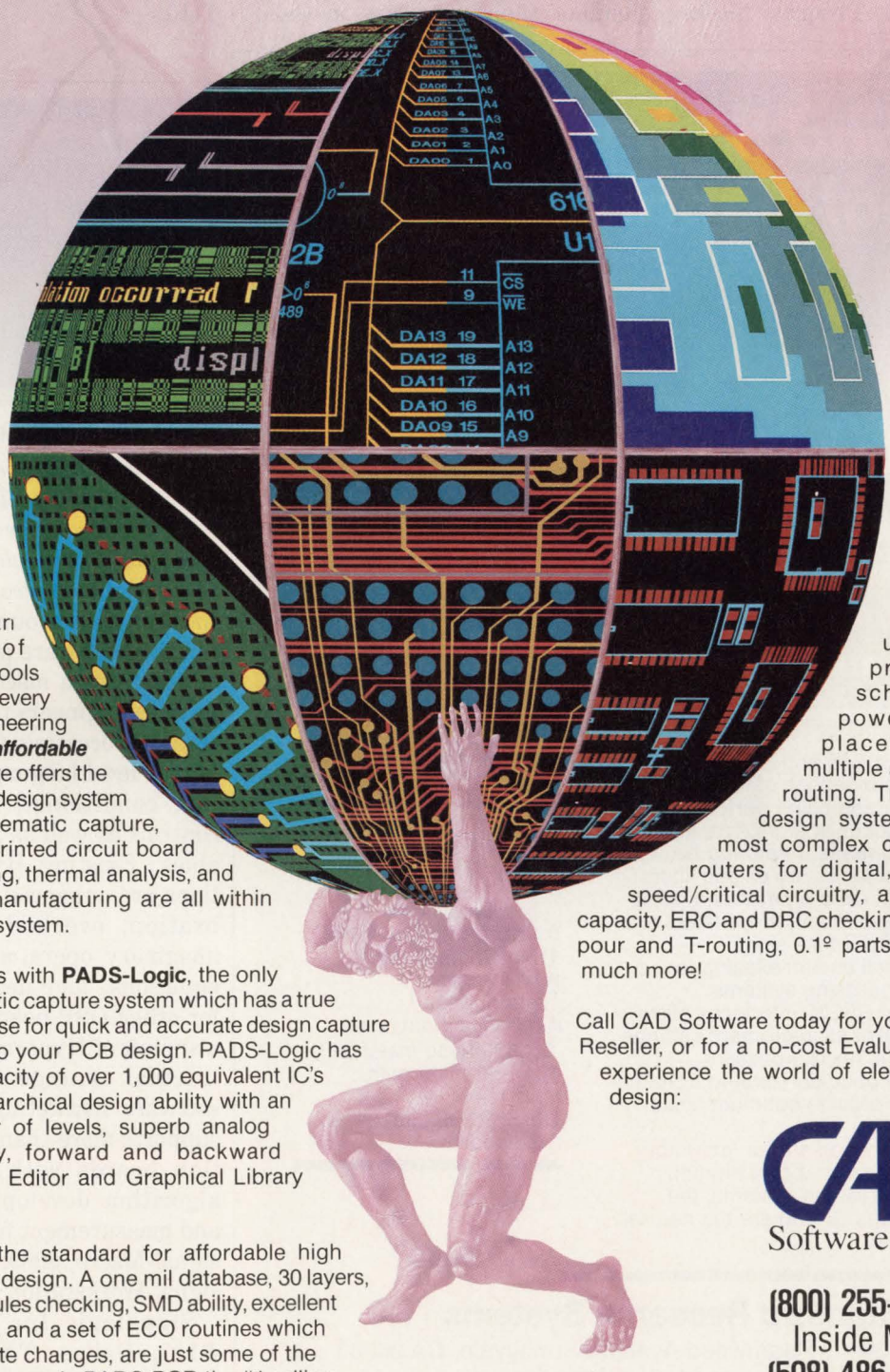

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You asked for an integrated set of CAE/CAD design tools which could deliver every aspect of your engineering design needs ***at an affordable price.*** CAD Software offers the highest performing design system for your PC. Schematic capture, logic simulation, printed circuit board design, auto-routing, thermal analysis, and computer aided manufacturing are all within the PADS Design system.

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PADS-PCB sets the standard for affordable high performance PCB design. A one mil database, 30 layers, automatic design rules checking, SMD ability, excellent interactive routing, and a set of ECO routines which ensure fast accurate changes, are just some of the features which have made PADS-PCB the #1 selling PC based PCB design system.

NEW! PADS-UNIX operates on the Sun Sparc Station family and contains all of the advanced features of the widely used **PADS 2000** product, including schematic capture, powerful component placement aids, and multiple approaches to track routing. This advanced PCB design system can handle the most complex designs, with auto-routers for digital, analog and high speed/critical circuitry, an unlimited design capacity, ERC and DRC checking, intelligent copper pour and T-routing, 0.1º parts/pads rotation, and much more!

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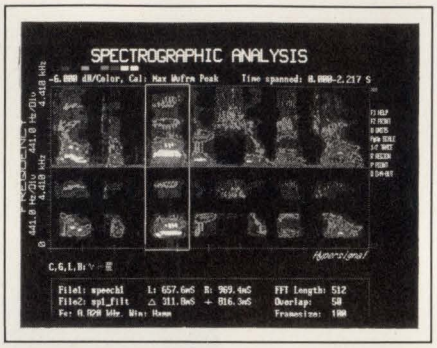
like a Forth inner interpreter, linking to the next block to be executed (Gello is compiled). A package named Threads introduces a powerful data flow, concurrent processing design, and execution mechanism. With Threads, designers can detail multiple execution paths that execute concurrently. Program blocks are supplied for standard industrial control functions, including data collection, signal analysis, real-time event processing, and device control. Gello introduces an open programming mechanism, where each block has visible, global variables and is limited in size. Users can simulate their programs in Gello, picking up errors before running the program in the Gellix engine. Gello development editor, $6500; Gellix run-time, from $900 (lower in volume); Threads/Gello, $8500.

Event Technologies Inc, 7210 Georgetown Rd, Suite 100, Indianapolis, IN 46268. Phone (317) 291-1110. **Circle No. 420**



DSP Development Software

- *Superset of Hypersignal DSP development tools*
- *Macro language automates processing and display functions*

Hypersignal-Macro is an enhanced tool set built around the Hypersignal DSP software package. The tool set features a macro language that enables engineers to specify Hypersignal processing functions with a higher-level language that has looping, conditional, and scheduling controls as well as automation variables. Existing Hypersignal functions are enhanced, adding dB calibration, overlaid trace display, imaginary operators for difference equations, and new board drivers for other DSP boards. Signalogic is a spinoff of Hypersignal with a contractual arrangement for shared software marketing. The software supports more than 30 DSP/acquisition boards with real-time data algorithm development, analysis, and measurement functions. Hypersignal-Macro, $989; existing Hypersignal-Workstation upgrade, $495.

Signalogic Inc, 9704 Skillman #111, Dallas, TX 75243. Phone (214) 343-0069. FAX (214) 343-0163. **Circle No. 421**

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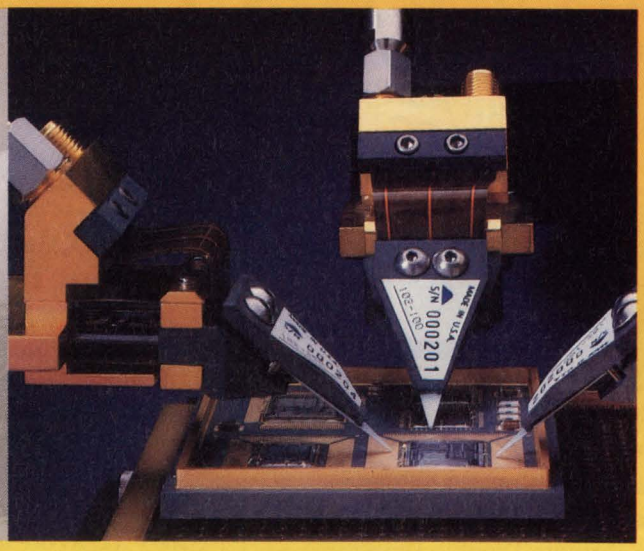

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The hand-held probe you've always trusted just can't keep pace in today's sub-nanosecond world. Speeds are too fast. Traces are too small. Circuits are just too sensitive.

The new 10× Probe from Cascade Microtech extends the accuracy of your high frequency test equipment right down to the circuit. To help you speed development, reduce design turns, and produce faster, more reliable circuits.

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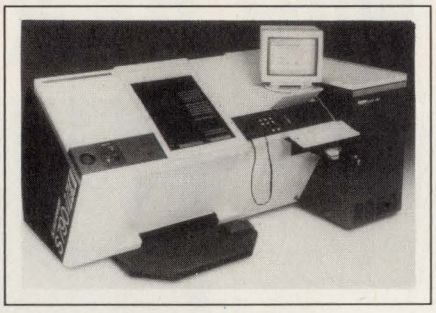
Circle #3 for Information only

Circle #4 Have a Sales Engineer contact me

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS



Three VXIbus-Based PC-Board Test Systems

- *Include a mixed-signal tester and a core architecture*
- *Also include application-specific configurations*

Three pc-board test systems use the VXIbus modular-instrumentation standard. The systems are the S760VXI, a core architecture for system integrators and value-added resellers; the S765VXI, available in custom configurations for specific high-volume applications; and the S790VXI, a mixed-signal tester. The S765VXI is based on the S760VXI and adds a test-head interface, a control console, power supplies, IEEE-488 instruments, and custom-designed VXI modules. The S790VXI combines the vendor's universal digital pin electronics with VXI instruments in a synchronized configuration built around a single high-speed backplane. S760VXI, from below $75,000; S765VXI, from $150,000; S790VXI, from $275,000; expected cost of typical configurations, $750,000. Delivery, 60 to 120 days ARO.

Schlumberger Technologies, ATE Div, 1601 Technology Dr, San Jose, CA 95110. Phone (408) 437-5129. FAX (408) 453-0137.

Circle No. 415

660-MHz Digital-IC Tester

- *Tests devices with 512 pins*
- *Has 80-psec skew*

The 83000 Model F660 is perhaps the highest speed digital-IC tester that any firm offers as a standard product. You can use the tester for device characterization or for production testing. Its clock rate is as high as 660 MHz, and it works with devices (including GaAs and ECL parts) that have as many as 512 pins. It achieves its speed without multiplexing (a technique that, to improve speed, sacrifices channel capacity). The system—which uses "tester-per-pin" architecture and backs each pin with as much as 4 Mbits of memory—has a pin-to-pin skew of 80 psec. All of the test electronics of the 28 ft^2 system reside in the test mainframe (the unit to which you attach a device handler). The controlling workstation stores data in compressed form and communicates with the mainframe over a fiber-optic link. Tester for 256 channels, approximately $1,600,000; additional channels, $5500 each.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 416

VXI C-Size Mainframes

- *Have 12-layer segregated backplanes*
- *All power supplies are current limited*

The 120 Series 12350 is a 13-slot C-size VXIbus mainframe. The 12260 is a portable, 6-slot C-size VXIbus mainframe. Both units include power supplies that have current-limited outputs and use 12-layer, segregated backplanes that maintain 50Ω impedance to 100 MHz. The backplanes incorporate jumpers for configuring the bus-grant and acknowledge functions. They incorporate circuits and indicators that monitor the function of each slot. The 13-slot unit measures 15.75×19×24 in. and weighs 48 lb; the 6-slot unit measures 13.5×8.6× 26 in. and weighs 28 lb.

Text continued on pg 195

CIRCLE NO. 47

INSTRUMENTS

Model 12350, $5500; model, $3400. **Mac Panel Co,** Box 7728, High Point, NC 27264. Phone (919) 861-3100. **Circle No. 417**

Telecommunications Board-Test System

- *Uses D-size VXI modules*
- *Incorporates multiple array processors*

The GR9000 test system for complex mixed-signal pc boards achieves some of its capabilities by harnessing a heretofore little-used feature of the VXIbus modular-instrument standard. To minimize cabling and to accommodate large amounts of computing power, this telecommunications test-and-measurement system uses the largest VXI boards, the so-called D size. Because the VXI modules mount in the system's test head and contain connectors not found on smaller VXI boards, the system needs a minimum of cabling to connect to a unit under test—regardless of whether pogo pins or edge connectors make the connections. The large VXI boards enable each system to include multiple array processors. Adapters accommodate smaller VXI units for specific applications. From $120,000; typical configuration, $225,000.

GenRad Inc, 300 Baker Ave, Concord, MA 01742. Phone (508) 369-4400. **Circle No. 418**

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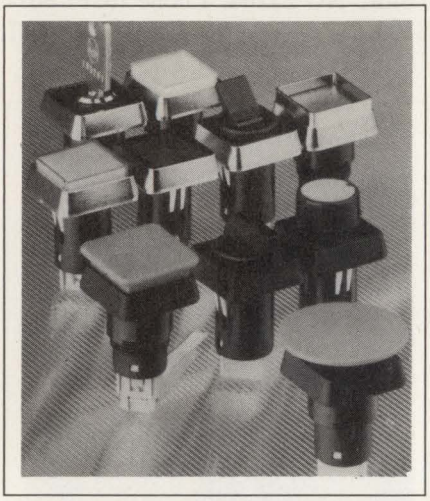
Advanced Power Solutions, 5994 W Las Positas Blvd, Suite 211, Pleasanton, CA 94588. Phone (415) 734-3060. FAX (415) 460-5498.

Circle No. 411



Pushbutton Switches

- *Have a 25-mm-square actuator*
- *Handle 100 mA at 24V loads*

Series 25 lighted pushbutton switches are designed to mount in a 16-mm-diameter panel cutout and feature a 25-mm-square actuator. They're designed for maximum loads of 100 mA at 24V. The units are available with red, green, blue, yellow, and white interchangeable lenses. Lamp options include a choice of bi-pin T1 incandescents or multichip LEDs. Bezels are available in black matte or chrome-plated finishes in three configurations—recessed button, flush button, or long-travel protruding button. The gold-plated silver contacts are rated for 10^6 operations min. Electrical connections are made via a plug-in socket designed for 4-conductor flat cable. The switches are designed to meet IP65 water-tight sealing requirements. $7.80 (100).

Unimax, Box 152, Wallingford, CT 06492. Phone (203) 269-8701. FAX (203) 265-5398. **Circle No. 412**

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- *Have 0.75-in. diameters*
- *Handle 60W*

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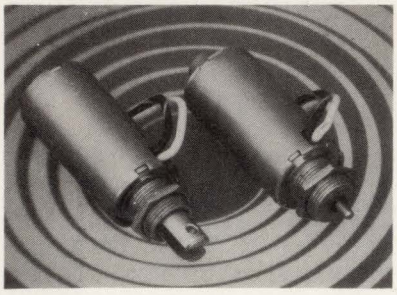

110V dc as standard. Other voltages are available as an option. Standard power ratings range from 4W continuous to 60W pulse duty. The solenoids feature brass guide tubes and a novel soft-stop design, which maximizes operating lifetime—10^7 cycles. $8 (OEM qty). Delivery, six to eight weeks ARO.

Liberty Controls Inc, 500 Brookforest Ave, Shorewood, IL 60435. Phone (815) 725-2241. FAX (815) 725-6571. **Circle No. 413**

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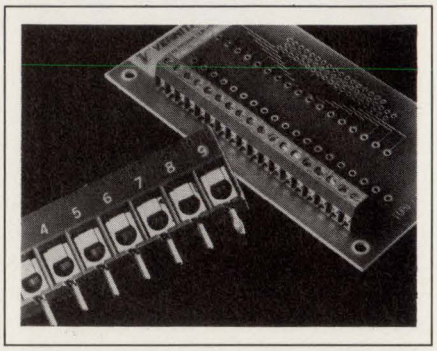
- *Have a 5-mm contact spacing*

Series 85K terminal strips are available in versions that have 2 to 24 positions. They have a 0.197-in. contact spacing, and they are available in straight-through, 90°, and 45° styles. The unique shape of their Snap-Loc terminals makes it possible to snap and lock the terminal strips onto the pc board prior to soldering. The terminal-strip footprint is identical to designs that have no Snap-Loc terminals so there's no need to redesign the pc board. All terminal strips have a Snap-Loc terminal on each end. Versions with 12 to 24 positions have an additional Snap-Loc terminal in the center. Strip with straight-through leads, $0.12/circuit (500).



Vernitron Corp, Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. FAX (603) 524-1627. **Circle No. 414**

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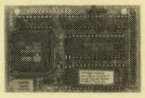

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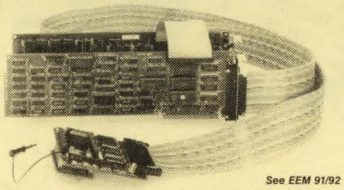

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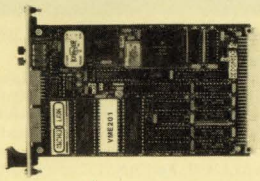

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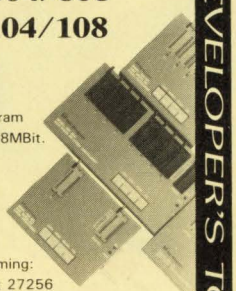

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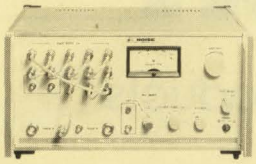

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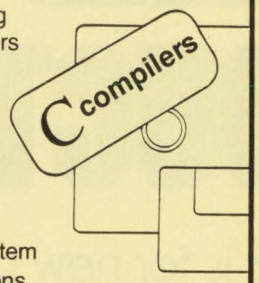

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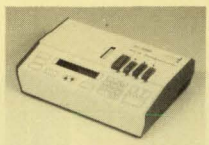

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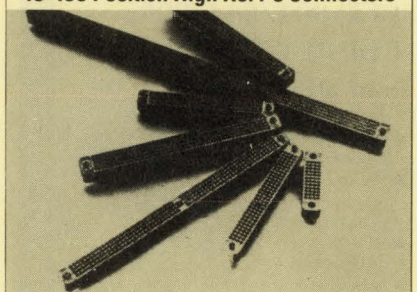

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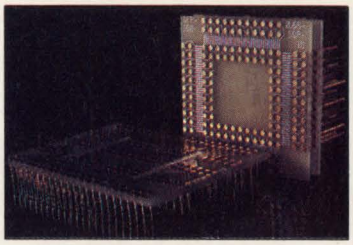

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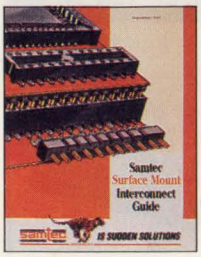

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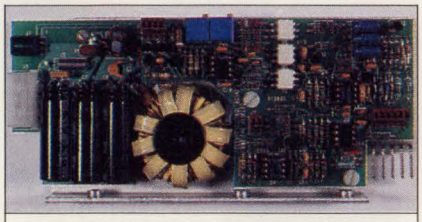

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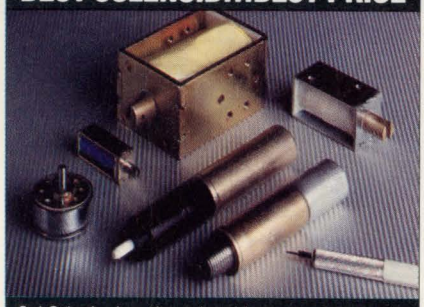

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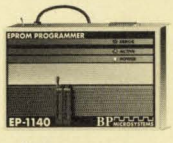

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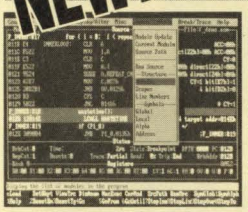

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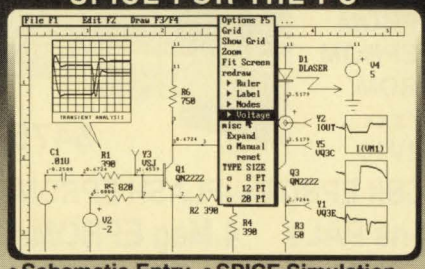

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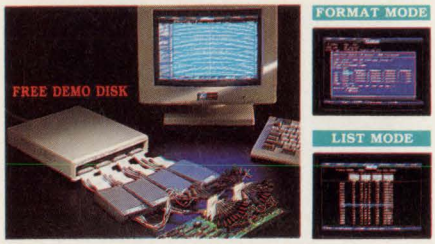

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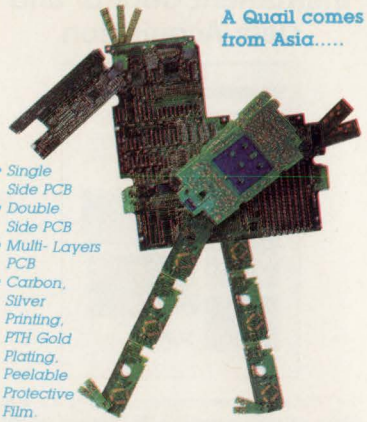

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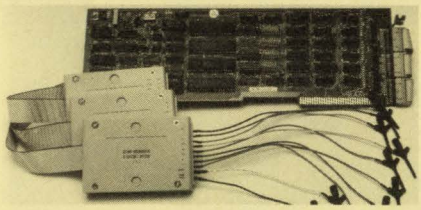

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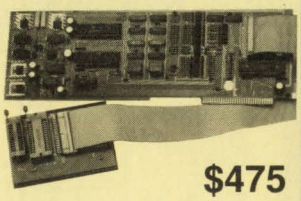

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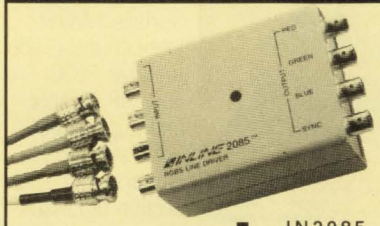

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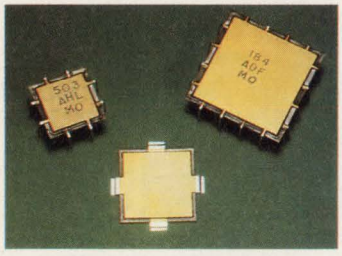

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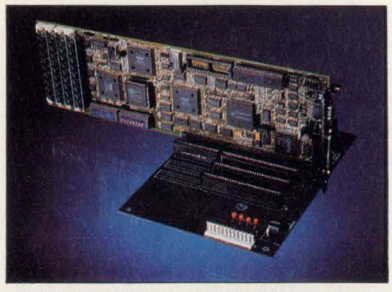

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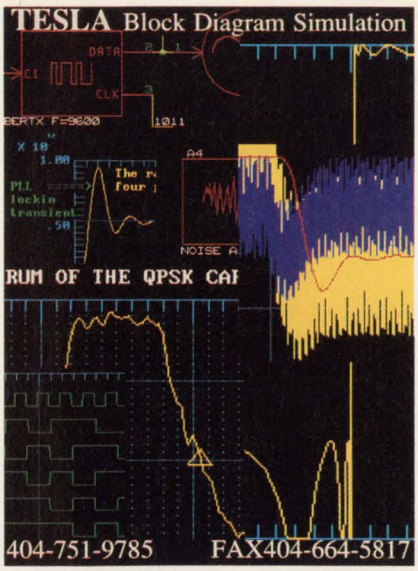

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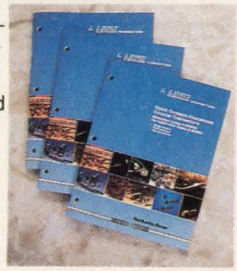

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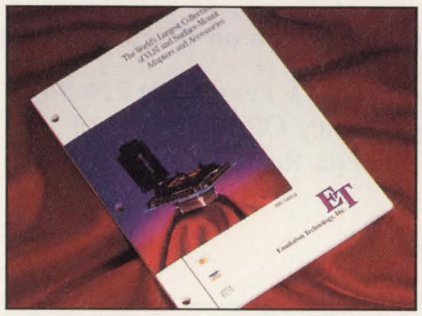

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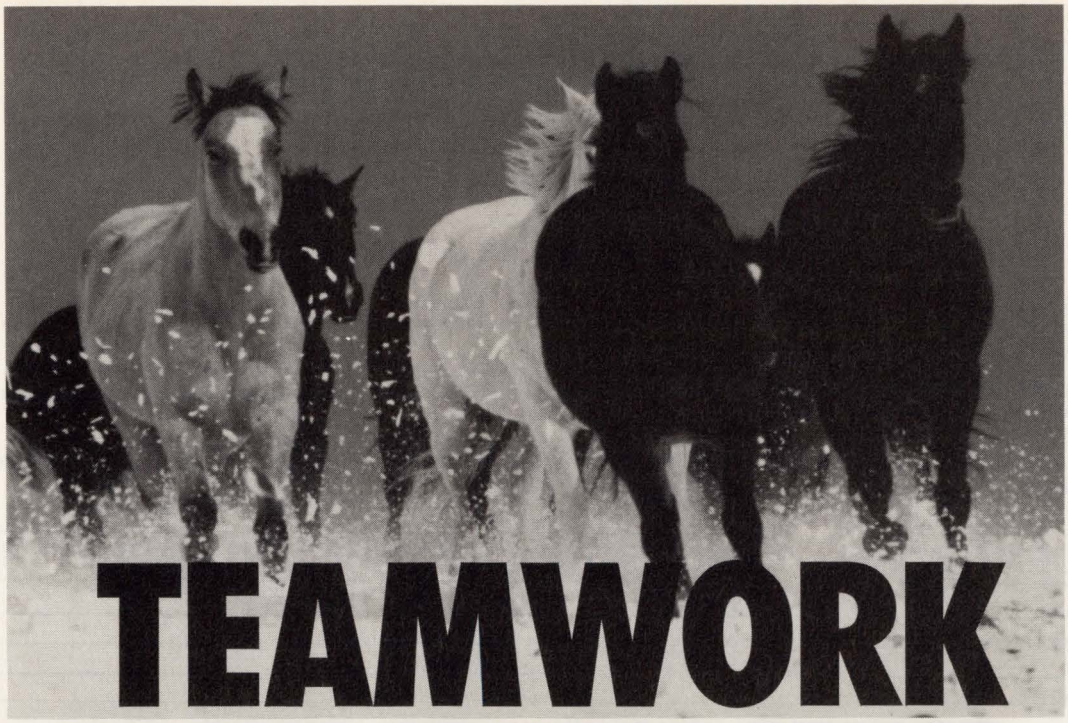

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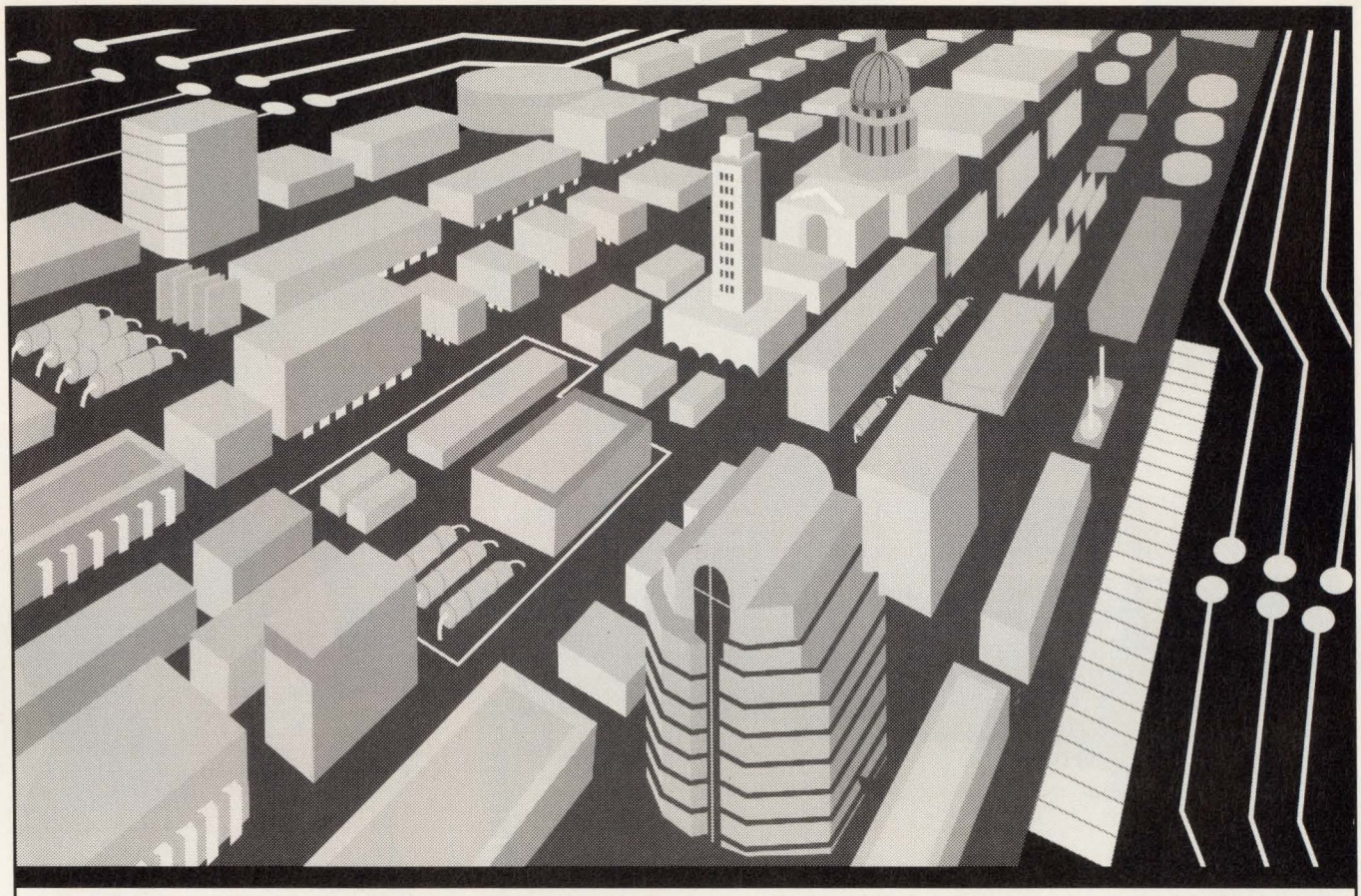

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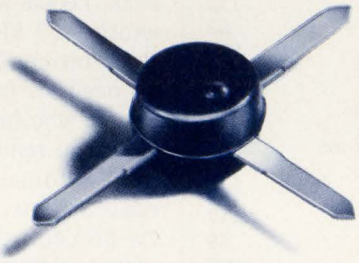


dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	•MAX. PWR. dBm	NF dB	PRICE Ea.	$ Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

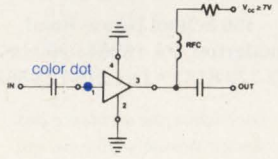
NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

Unbelievable, until now...tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers only $59.95



Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 220, 470, 680, 1000 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047, .068, .1 μf

† Minimum Order 50 per Value
• Designers kit, kcap-1,50 pieces of each capacitor value, only $99.95

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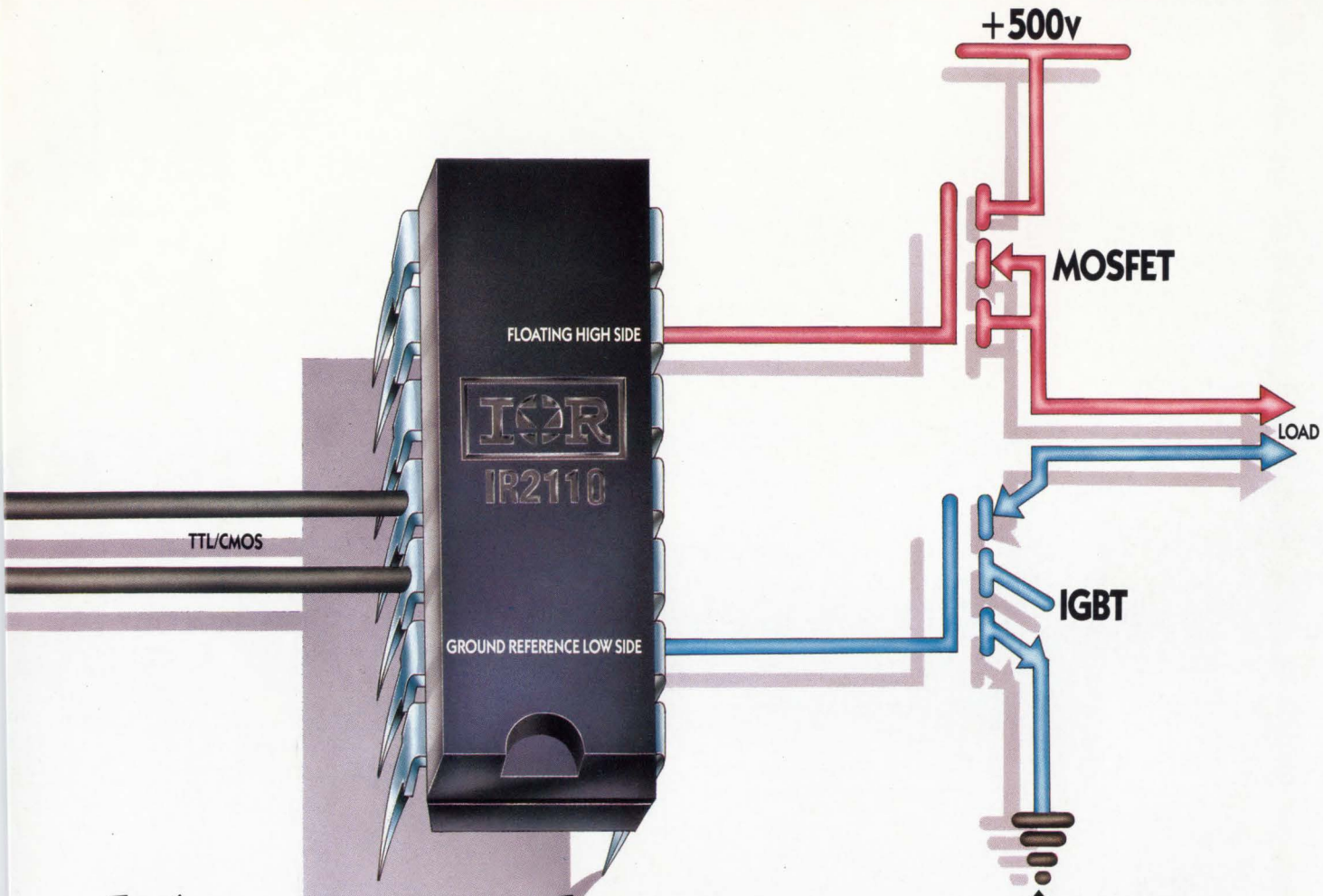
C113-Rev. D



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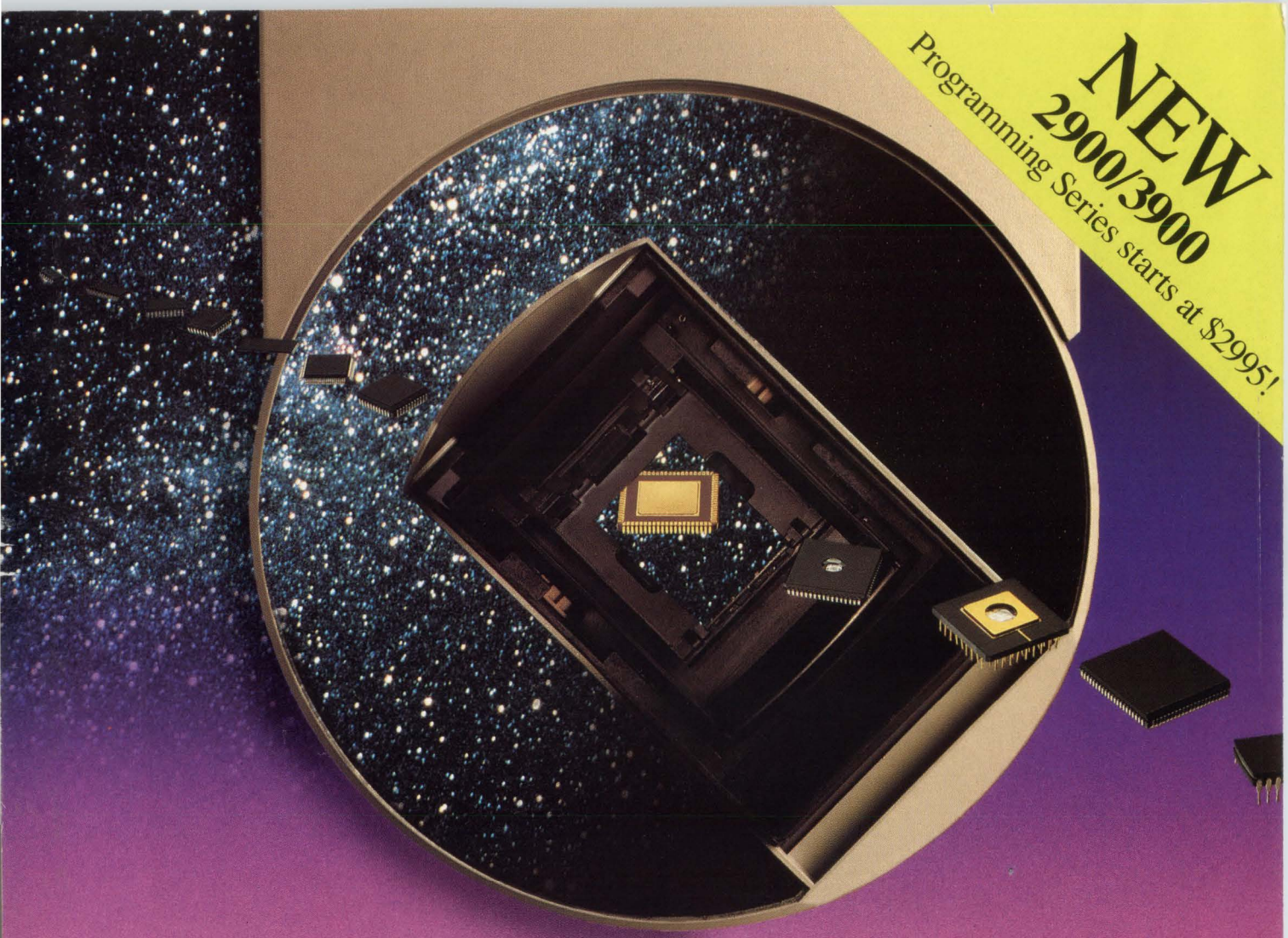

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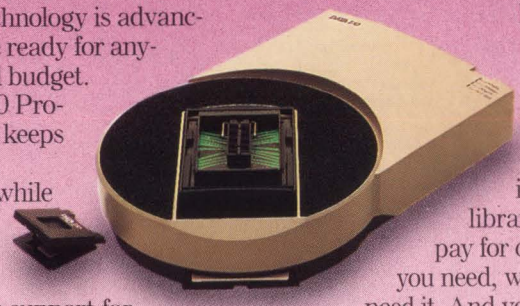

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