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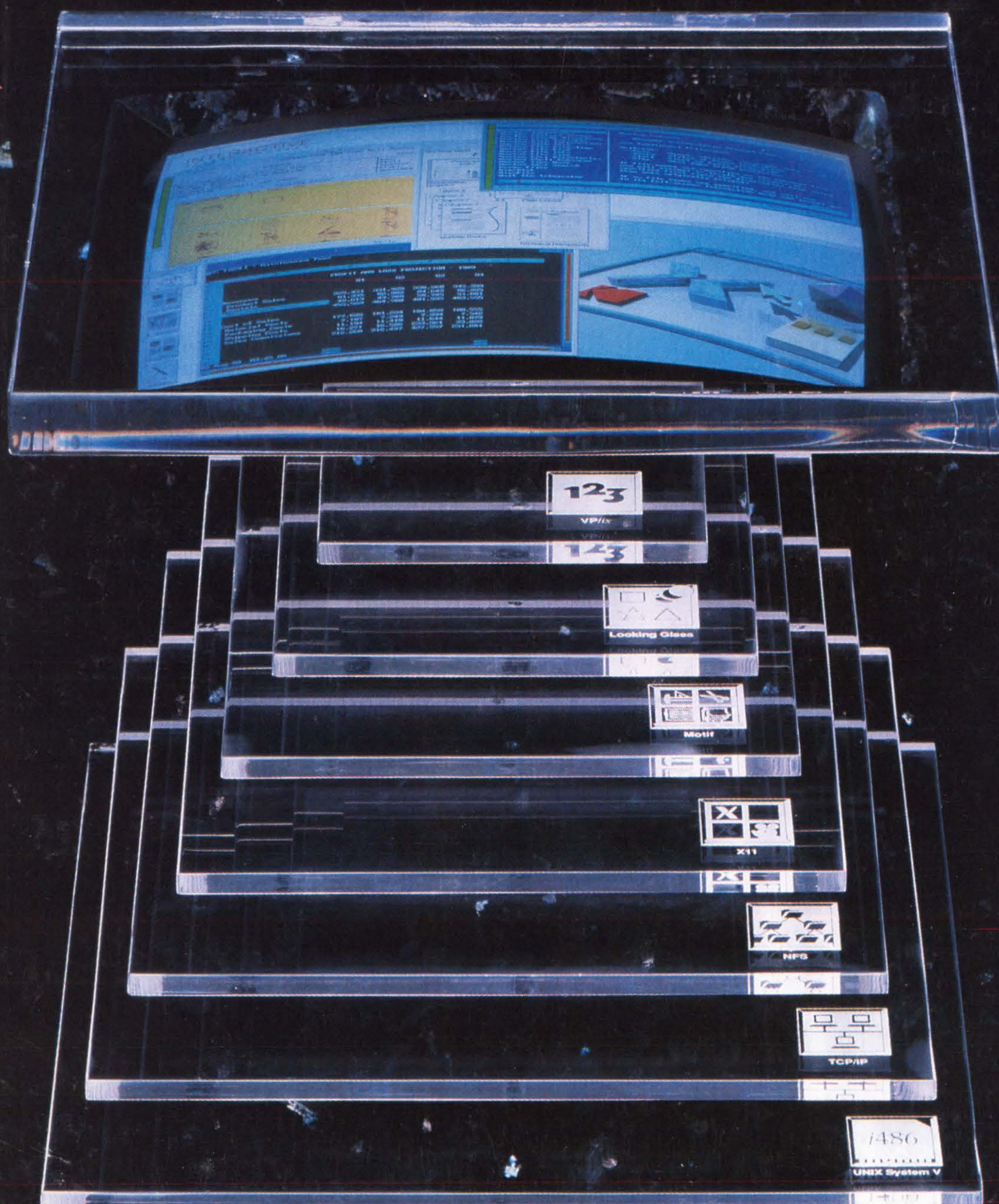
SEPTEMBER 17, 1990

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

PC Unix transparently supports networking and graphics pg 132



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SPECIFICATIONS

	TOSW-230 ZSDR-230		TOSW-425 ZSDR-425	
Freq. Range(MHz)	10-3000		10-2500	
Insert. Loss (dB)	typ.	max.	typ.	max.
10-100MHz	1.3	1.9	1.3	1.7
100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
Oper. Temp.(°C)	-55 to +100		-55 to +100	
Stor. Temp.(°C)	-55 to +100		-55 to +100	
Price (10-24) (1-9)	$39.95 $89.95		$59.95 $109.95	

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F126 REV.A

Volume 35, Number 19

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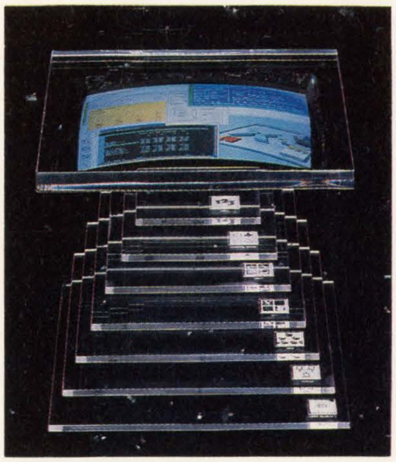
September 17, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:** Unix for the personal computer supports enough standard networking and graphics capabilities to solidify the PC's ascension into the workstation market. See the Special Report on pg 132. (Photo courtesy Interactive Systems Corp; photography by Mark McIntyre; art direction by Mike Pitzer, Bozell Inc)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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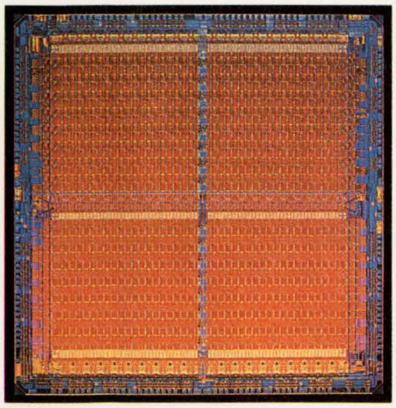
Circle 55 For Literature

Continued from page 5



By the time you evaluate the merits of an FPGA, *its manufacturer will probably have introduced an upgrade (pg 57).*

Continued on page 9

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Continued from page 7

DESIGN IDEAS

EDITORIAL

Companies that want to do business in the USSR should approach the country with great caution. Staying at home may make even more sense.

NEW PRODUCTS

DEPARTMENTS

MAKING THE SWITCH TO HIGH PERFORMANCE? OUR 68331 PUTS YOU ON THE RIGHT TRACK.

Considering a move up in power? Now you can switch to the 32-bit performance track that's parallel with all your future needs. Thanks to Motorola's new, surprisingly affordable 68331 microcontroller.

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THE PATHWAY TO PERFORMANCE.

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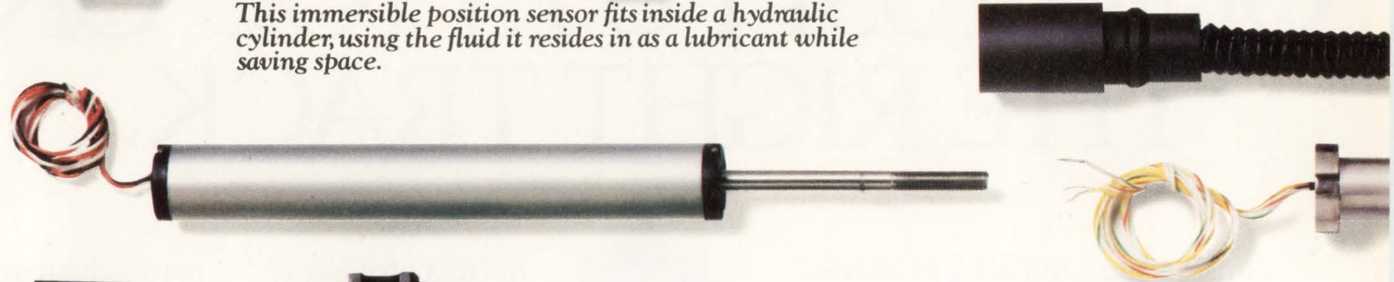
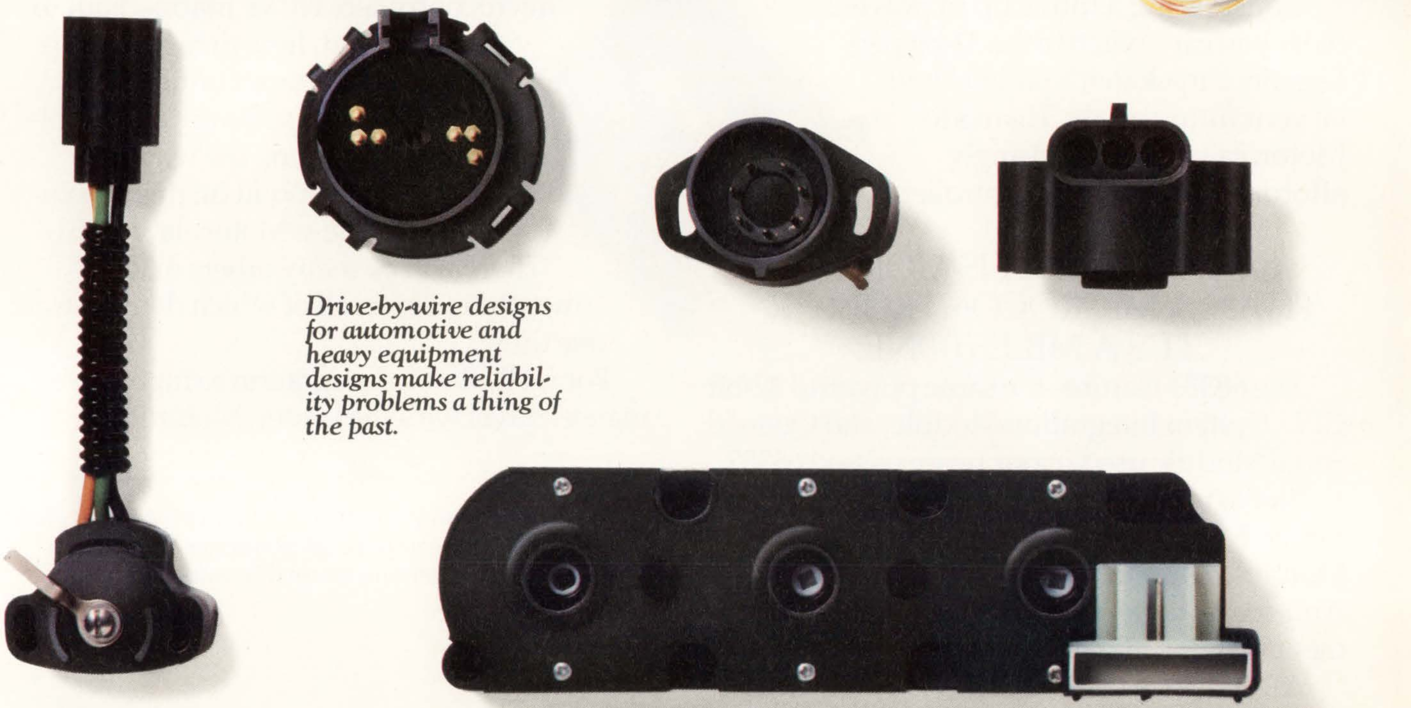
This immersible position sensor fits inside a hydraulic cylinder, using the fluid it resides in as a lubricant while saving space.





Drive-by-wire designs for automotive and heavy equipment designs make reliability problems a thing of the past.

Both spring-loaded and magnetically coupled position sensors for truck engine applications must withstand extremes of vibration, temperature and exposure to highway dirt and grime.

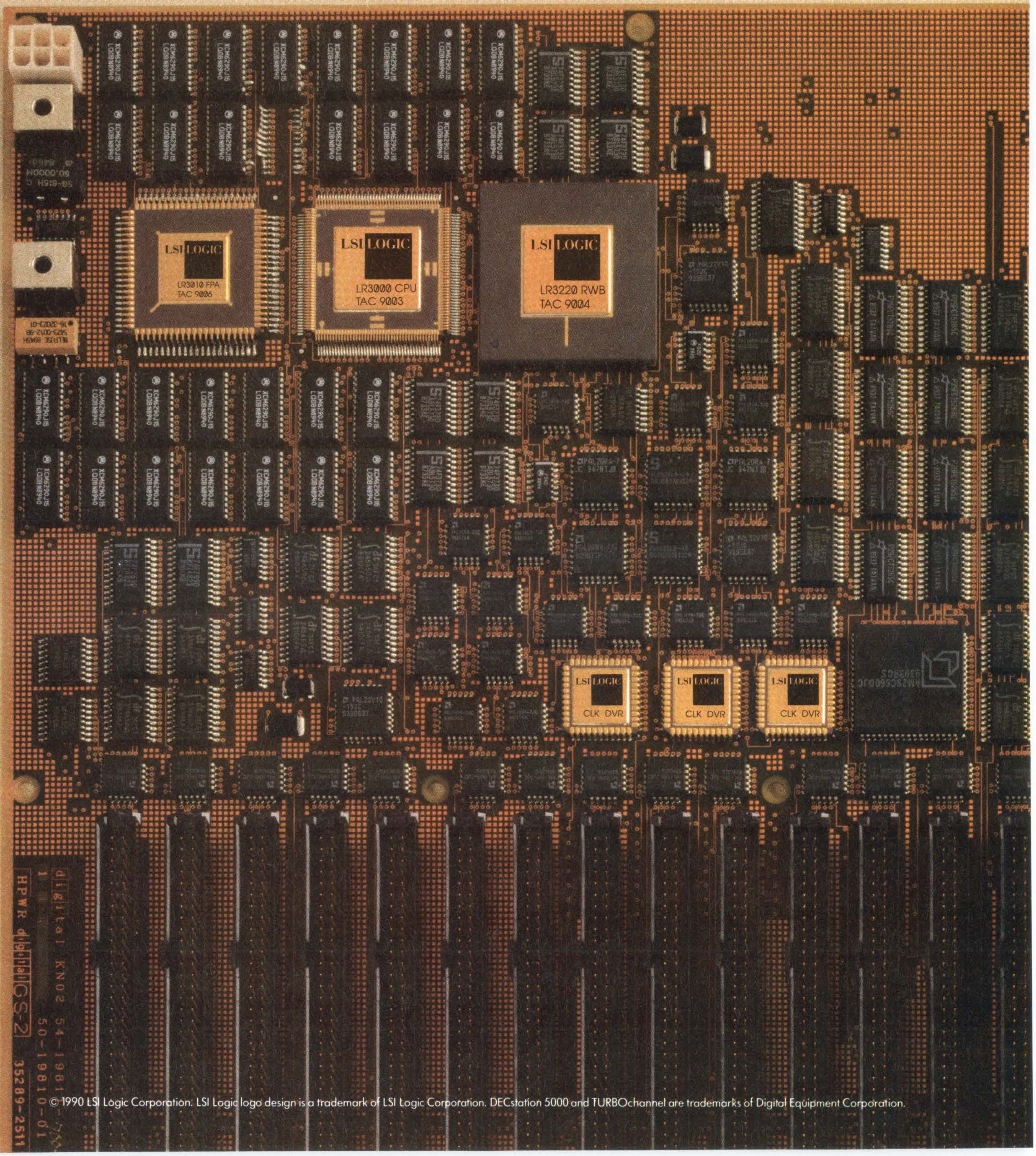
We've modified a famous phrase to make a point: no matter what the application, Duncan can design a specific-use potentiometric position sensor that fits in. Whether the challenge comes from the physical environment, space limitation, form or function, you can have whatever you want... just by telling us what you need. Get started now. FAX us your requirements at (714) 557-6420. We'll give shape to your ideas in a hurry.

HOW A STRATEGIC PARTNERSHIP WROTE A NEW CHAPTER ON SYSTEM PERFORMANCE:

DECstation 5000 AND LSI LOGIC.

Achieving 24.2 MIPS at 25 MHz was no small task. Even for Digital.

So they designed-in LSI Logic's unique read-write buffer and MIPS-based chipset that optimized the processing power of the LR3000 CPU. And consolidated the read-write buffer functions of 17 chips into a single chip. Putting far more performance into far less real estate. And making the new DECstation 5000 workstation a



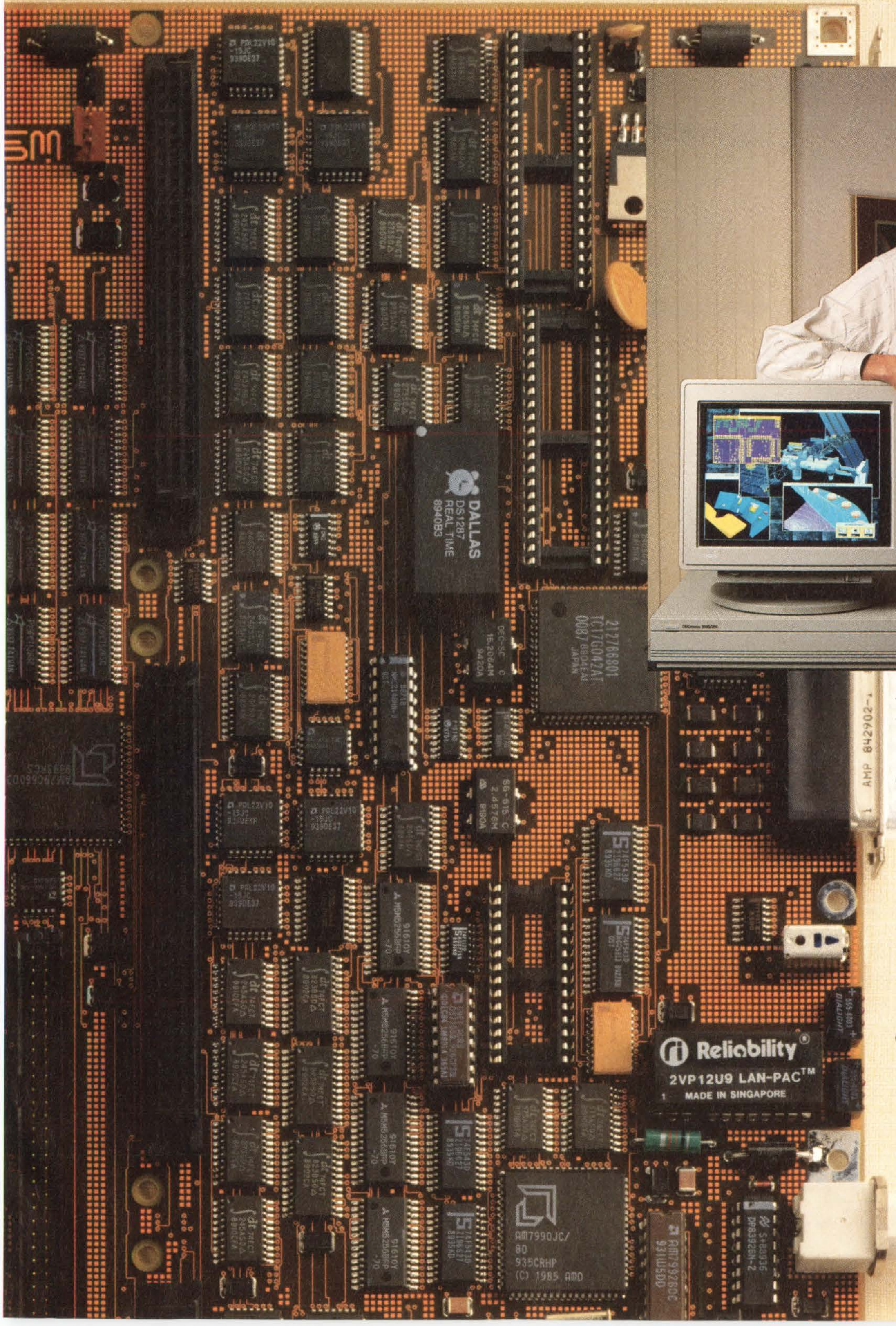
reality. In less than 11 months.

LSI's proprietary LR3220 read-write buffer performs memory write operations at the CPU clock rate, practically eliminating the bottleneck between the CPU and main memory. Boosting the processing power of the DECstation 5000 workstation to the limits of the price performance curve. A novel idea that delivers 120 Mbytes of main memory, dazzling high-end graphics and the new TURBOchannel I/O interconnect to the desktop, for under $15,000.

If you'd like to write the next chapter in the workstation wars, call us. We'll help you quickly turn your technology into a best seller.

LSI LOGIC

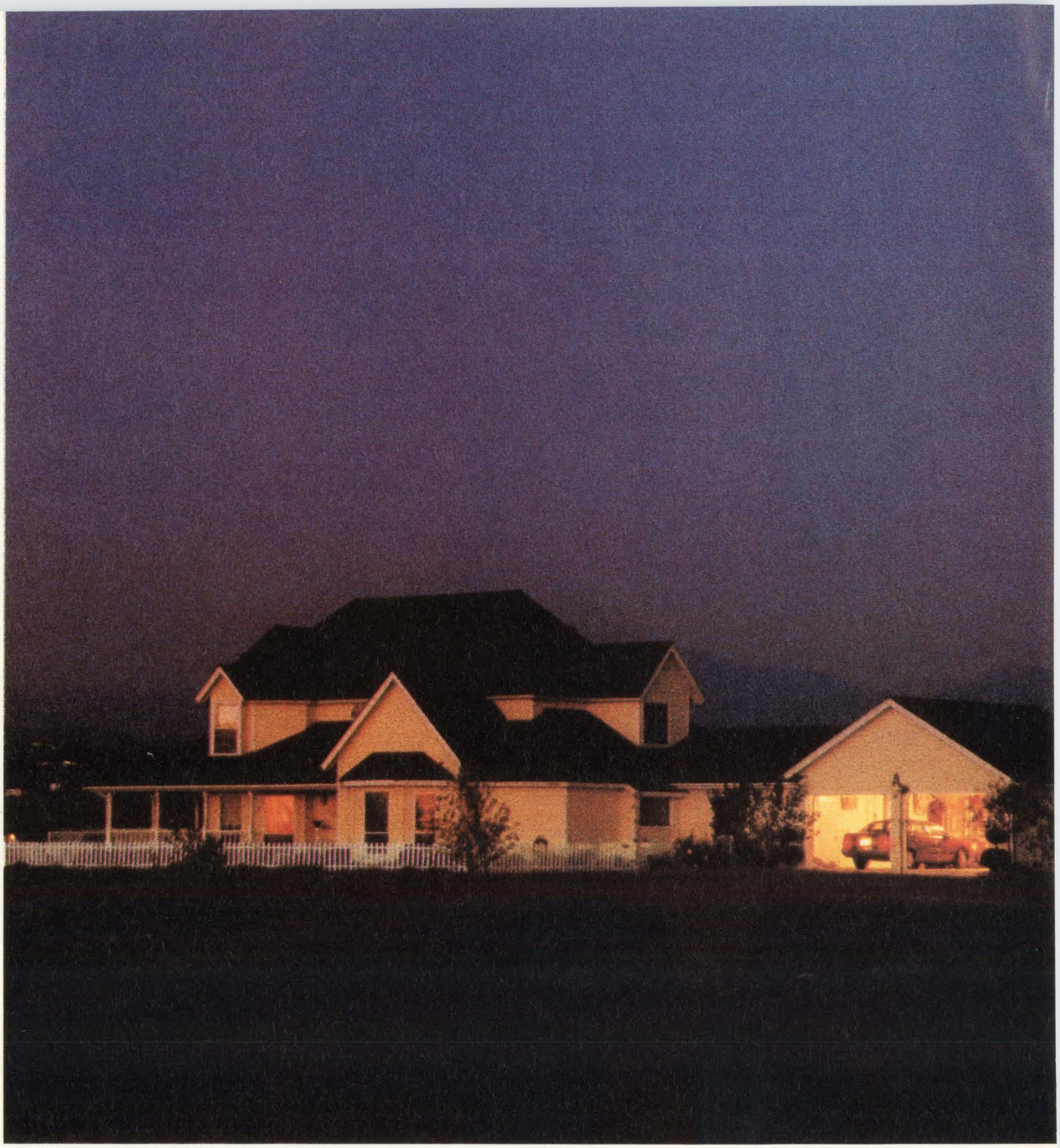
ACROSS THE BOARD



According to Tom Furlong, Manager of Digital Equipment Corporation's RISC Workstation Group, "The level of performance achieved on the DECstation 5000 workstation simply wouldn't have been possible without LSI's ASIC methodology and their MIPS microprocessor expertise."

For the whole story call 408.433.7556, or write for a free white paper, "Writing a new chapter in workstation performance: DECstation 5000," LSI Logic, 1551 McCarthy Blvd, MS D102, Milpitas, CA 95035.

CIRCLE NO. 81



Even though our products have been to Jupiter and beyond, you can still find them out in your garage.

NEWS BREAKS

EDITED BY SUSAN BUREAU

THREE DSP CHIPS FOR DIGITAL-RECEIVER APPLICATIONS . . .

Plessey Semiconductors (Scotts Valley, CA, (408) 438-2900) recently announced three DSP chips designed especially for digital-receiver applications. The $395 PDSP16350 generates simultaneous 20-MHz sine and cosine waveforms using a Cordic (Coordinate Rotation Digital Computer) processor. The 16-bit waveforms have an accuracy of 0.001 Hz. They feed a pair of 16-bit multipliers, which multiply a 16-bit input signal to produce in-phase and quadrature output channels. The $395 PDSP16256 programmable, variable-length finite-impulse-response filter has 16 16×12-bit multiplier/accumulators, which can be used reiteratively to provide 16 to 128 digital-filtering stages at sample rates of 2.5 to 20 MHz. You can cascade this device at all speeds. The chip can accept as many as 128 coefficients from a host CPU and store them internally. The $439.36 PDSP16116A, a 20-MHz version of the company's 10-MHz PDSP16116 complex multiplier, can multiply two complex 16-bit words every 50 nsec.

. . . A FOURTH PERFORMS 1024-POINT TRANSFORMS IN 96 μSEC

A fourth DSP chip from Plessey Semiconductors (Swindon, UK, (793) 518000), the PDSP16510 FFT processor, performs real-time, forward or inverse FFTs on real or complex 1024-point data sets in 96 μsec. Block floating-point arithmetic is standard. Data and coefficient words are each 16 bits. The chip stores the data sets internally in its 32k-byte memory, which eliminates the need for external dual-port RAM and minimizes pin count to 84. Hamming and Blackman-Harris window-operator functions reside on the chip to provide 67 dB of side-lobe attenuation. Connecting multiple devices boosts performance; operation with six chips allows data sampling at 40 MHz with 1024-point complex transforms. Packaged in pin-grid arrays, samples will be available in the fourth quarter for $2100.—John Gallant and Brian Kerridge

4-CHANNEL WAVEFORM GENERATOR OFFERS 16-BIT PRECISION

The Model 2201A arbitrary-waveform generator includes three phase-coherent channels and a built-in noise-generation channel. The unit from Pragmatic Instruments Inc (San Diego, CA, (619) 271-6770) can generate standard waveforms such as sine, triangular, and square waves. It samples at 2 MHz and features 16-bit precision. To create waveforms, you can use either a mouse or the front-panel controls for the three phase-coherent channels. The generator includes 64k words of battery-backed static RAM for each of the three main output channels. An interface on the generator accepts credit-card-size, removable, static-RAM memory modules, each of which has 32k bytes of memory and a battery that makes it nonvolatile. You can use these cards to store libraries of waveforms. The unit costs $9985, including the mouse and one memory card.—Maury Wright

DVM REPLACES THERMAL-TRANSFER INSTRUMENTS

The 4920 Alternating Voltage DVM from Datron Instruments (Norwich, UK, (603) 404824) boasts enough accuracy for calibrating premium ac calibration instruments. The digital voltmeter displays 7½-digit resolution on ranges of 300 mV to 1 kV and for input frequencies of 1 Hz to 1.25 MHz. Its total measurement uncertainty is ±28 ppm for input levels of 0.9 to 11V and frequencies of 40 Hz to 30 kHz. This accuracy holds for one year and ±5°C ambient temperature changes from the calibration point of the meter itself. Unlike its thermal-transfer counterparts, the voltmeter is portable. It has a settling time of <2.5 sec for frequencies greater than 100 Hz and a read rate of 3 readings/sec. Operation is programmable with an IEEE-488.2 interface. For increased accuracy, you can select an ac/dc transfer mode of operation, which reduces total measurement uncertainty to 14 ppm (7 ppm of this figure is traceability uncertainty to the National Institute of Standards and Technology). The meter costs $9995; a 1-mV-range option costs $1495 more.—Brian Kerridge

IEEE REFORMER IRWIN FEERST DEAD AT 62

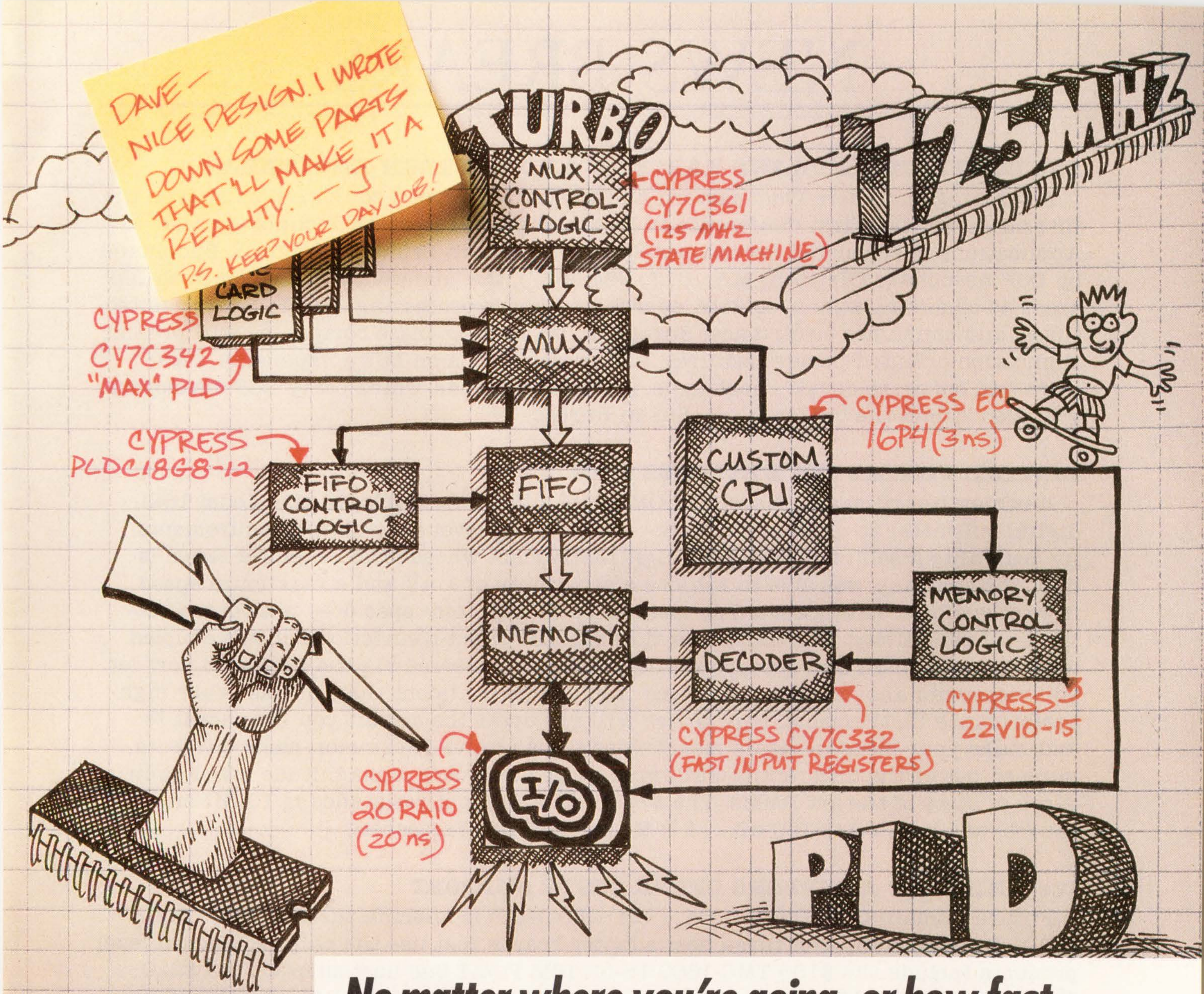
Irwin Feerst, a long-standing member of the IEEE, died last month in Plainview, NY. He had been ill for about 1½ years with ALS (Lou Gehrig's disease). Mr Feerst's career was varied; he worked as a company EE, a teacher of physics and electronics at Adelphi University in Garden City, NY, and an independent consultant. He was most known, however, for his attempts to reshape the IEEE's goals to better represent the working engineer. He often argued that the organization was over-represented by educators and upper-level managers, which caused the IEEE to drift away from its original purpose of supporting the engineer. In 1973, Mr Feerst founded the Committee of Concerned EEs, which circulated a monthly newsletter to formalize complaints from IEEE members. In 1986, he earned a place on the ballot for IEEE president by gathering signatures from over 2000 members. Mr Feerst is survived by his wife, Dr Francis Feerst of Massapequa, NY, his son, Dr David Feerst of Chicago, and his grandson, Daniel.—John Gallant

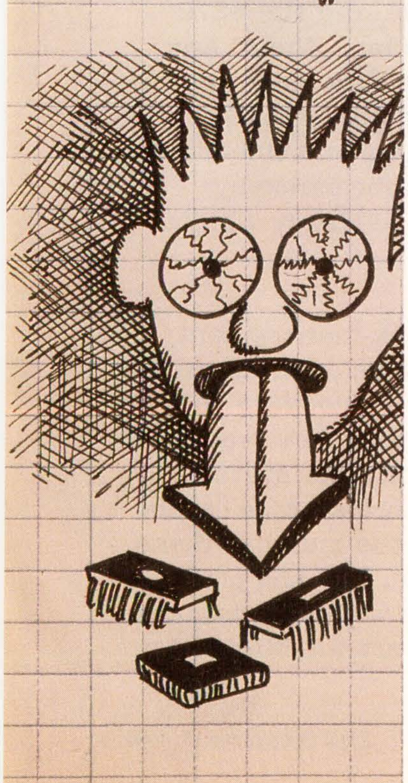
HOW MANY PINS DOES AN ID CHIP NEED

An identification chip can identify pc-board assemblies, provide a network address, or provide an access code. If you think such a chip needs pins for power, ground, an input, and an output, then you've counted two pins too many. Dallas Semiconductor (Dallas, TX, (214) 450-0400) offers a 2-pin Serial Number chip that uses an internal timebase to multiplex data, control, and power to a single pin. The timebase uses pulse width to distinguish between ones and zeros. Internal capacitance stores charge when the input signal is high and powers the chip when the input signal is low; power refresh occurs whenever the input goes high. The chip's 64-bit serial number, laser-written by the vendor, comprises an 8-bit model number, a 48-bit serial number, and an 8-bit CRC (cyclic redundancy check) number you can use to ensure data integrity and proper data transmission. The plastic TO-92-packaged chip costs $0.35 (100,000).—Michael C Markowitz and J D Mosley

REWRITABLE OPTICAL DISK DRIVE SEEKS IN 30 MSEC

The Model RMD-5100-S rewritable optical disk drive takes advantage of a low-mass head and 3½-in. media to provide an average seek time of 30 msec. Offered by Mass Optical Storage Technologies (Cypress, CA, (714) 898-9400), the drive includes a scanning/short-seek capability that makes data within a 128-track band available in 7 msec. A 128k-byte read-ahead cache reduces seek time to the 1-msec range on cache hits. The drive stores 133M bytes of data and features a 30,000-hour MTBF. It includes a SCSI controller and is compatible with the SCSI common-command set. The drive produces a sustained transfer rate of 512k bytes/sec; the on-board buffer lets the SCSI controller perform burst transfers at 1.5M bytes/sec in asynchronous mode and 3M bytes/sec in synchronous mode. Samples of the drive are available for $2425.—Maury Wright





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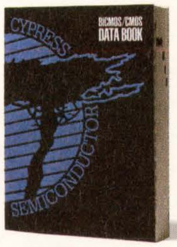

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NEWS BREAKS

DSP CONFERENCE DRAWS EASTERN AND WESTERN ENGINEERS

Attracting engineers from eastern and western European countries, as well as the US and Japan, the First Conference in Digital Signal Processing Technology and Applications is scheduled for October 22 to 25, 1990, in Brussels, Belgium. Sponsored by DSP Associates (Newton, MA, (617) 964-3817), the conference will cover such DSP areas as communications, control, speech and image processing, HDTV, VLSI architectures, and consumer electronics. European, US, and Japanese companies will present application-oriented papers, lectures, and presentations on DSP components, hardware and software development tools, and future trends. Third-party DSP developers will also attend the conference.—Susan Bureau

DIGITAL VOLTMETER RESOLVES 1 nV

Keithley Instruments (Cleveland, OH, (216) 248-0400) developed the Model 182 digital voltmeter to excel at one task—making low-level dc voltage measurements. By designing a self-calibrating 6½-digit instrument whose least sensitive range is 30V, the company was able to achieve a sensitivity of 1 nV and a maximum speed in excess of 50 readings/sec. The meter's 15-nV p-p noise spec does not contradict the 1-nV sensitivity. The unit's low-thermal-EMF input-connection scheme coupled with internal math and postprocessing of data transferred via the IEEE-488 port let you measure nanovolt signal changes. You can be confident that, unlike other high-performance instruments, this device will not upset the circuit you connect it to and make your measurements meaningless. The ac and dc common-mode currents pumped out of the differential FET input stage are orders of magnitude lower than those of state-of-the-art DMMs. The $3695 meter's input resistance is 10 GΩ on all ranges, and its CMR is 160 dB.—J D Mosley and Dan Strassberg

ICs AND HOST ADAPTERS OFFER SCSI-2 SUPPORT

Future Domain Corp (Irvine, CA, (714) 253-0400) is offering the $66 TMC-1800 SCSI-2 interface chip and three host adapter boards that use the chip. The board-level products include the $180 TMC-1680 16-bit IBM PC/AT-bus host adapter, the $220 TMC-1680 IBM PC/AT-bus host adapter with a floppy-disk controller, and the $279 MCS-700 16-bit host adapter for IBM's Micro Channel Architecture bus. The IC and the host adapters support the 10M-byte/sec "fast synchronous" data-transfer option introduced in the SCSI-2 specification. The boards employ a dual-adaptive FIFO-buffering scheme that takes advantage of the IC's 8k-byte FIFO buffer and the buffers located on the host adapters. A device driver can optimize SCSI performance by setting interrupt levels in conjunction with the dual FIFO buffers.—Maury Wright

DISK-MANAGEMENT SOFTWARE FOR SPARCSTATIONS

Interphase Corp (Dallas, TX, (214) 919-9200) is now bundling disk-management software called Softarray with its disk-drive controllers. The software ensures uninterrupted availability of critical data on Sun-3 or -4 SPARCstations by copying the critical data to multiple disk drives. The program also lets you spread data evenly across several drives to provide simultaneous access to data in multiuser systems. If you have an application, such as video imaging, that requires more storage capacity than any one of your drives can provide, the software can use the multiple disks as if they were a single, larger disk. Depending on the controller you use, the program will work with as many as 28 disk drives. The software only comes with the manufacturer's disk-drive controllers, however. For $3900 you get a dual-port V/SCSI 4210 Jaguar SCSI disk controller and the software.—J D Mosley

Rugged Solutions to Tough Design Problems.

Portable data products from Datakey are meeting the needs of electronic OEM design engineers in a wide range of commercial and military applications. They can help you:

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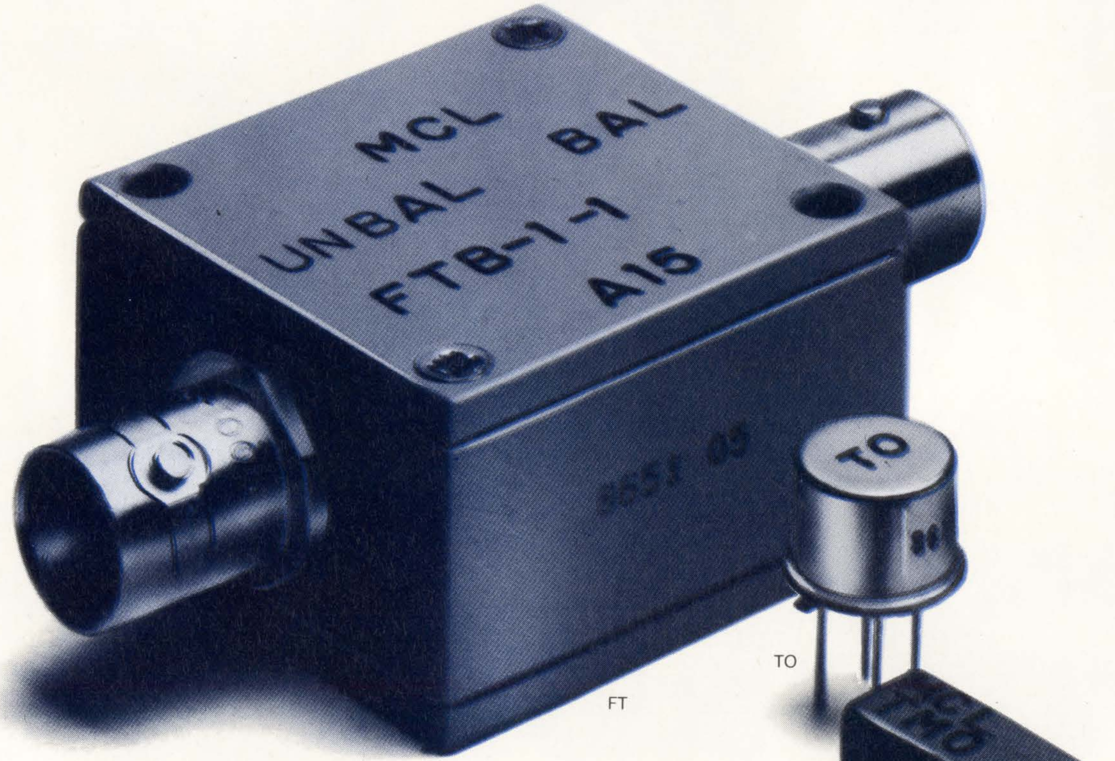
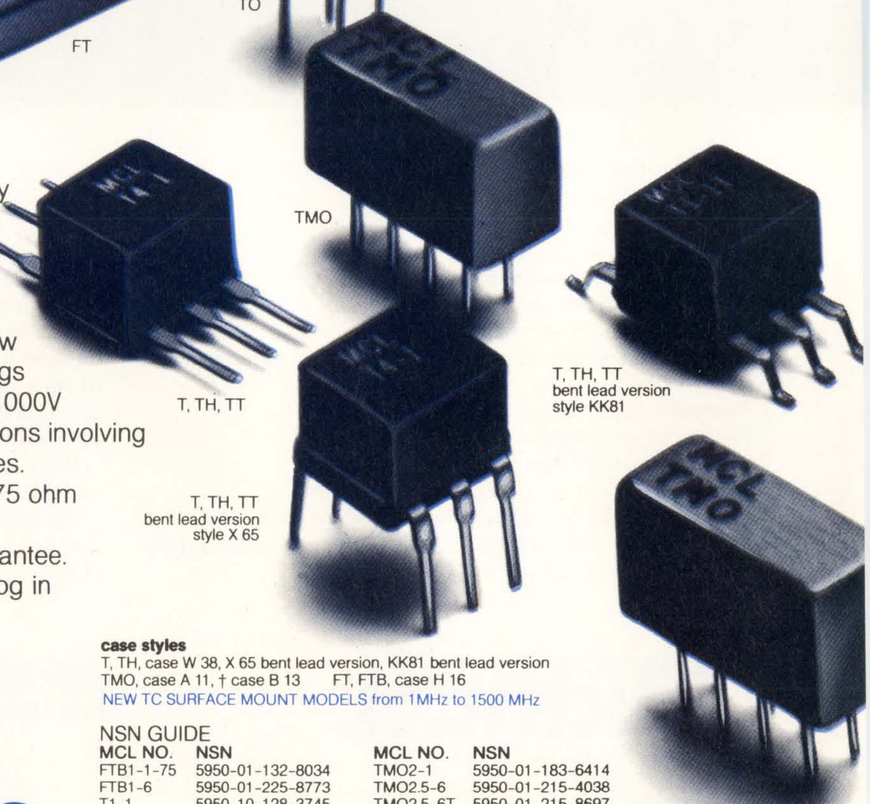
RF TRANS

Over 50 off-the-shelf models...





Having difficulty locating RF or pulse transformers with low droop, fast risetime or a particular impedance ratio over a specific frequency range?... Mini-Circuits offers a solution.

Choose impedance ratios from 1:1 to 36:1, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55831 requirements*). Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000M ohms insulation resistance and up to 1000V dielectric voltage. For wide dynamic range applications involving up to 100 mA DC primary current, use the T-H series. Coaxial connector models are offered with 50 and 75 ohm impedance; BNC standard; request other types. Available for immediate delivery with one-year guarantee.

Call or write for 68-page catalog or see our catalog in EEM, or Microwaves Product Data Directory.

*units are not QPL listed

case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
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NSN GUIDE

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T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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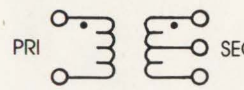
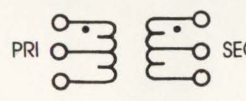
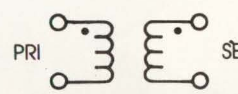
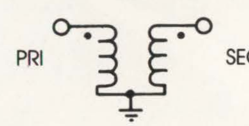
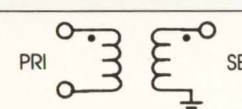
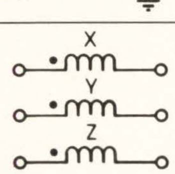
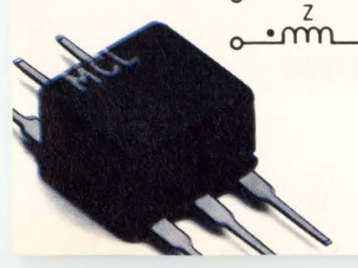
C72-1 REV. B

FORMERS

3KHz-800MHz from $3^{25}

case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS

Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range

For Designs That Demand a Lot of Memory,

When it comes to PCs, workstations, printers, and other computer-related products, end-users want smaller systems, maximum memory storage, and minimum power consumption. And they want it now. Which creates several problems for you. How do you reduce system size *and* power consumption yet increase memory capacity? *And* be first to market with your product? Oki offers some flexible solutions.

To begin with, our pin-for-pin compatible 4-Megs provide 4X the memory storage of a 1-Meg —without increasing space. Plus our 4-Megs have the lowest power consumption of any 4-Meg, making them ideal for laptops and other memory-intensive, power-hungry systems. Choose from a variety of packages too: DIP, SOJ, ZIP—and, later in 1990, an ultrathin TSOP, for even more space-saving advantages.

For higher density applications, select from Oki's package-efficient family of SIMMs: 4-Megx8s, 4-Megx9s, and 1-Megx36s. Or we'll work with you to design a custom SIMM that meets your unique specifications. All our 4-Megs and SIMMs are available *now,* so we're ready to help accelerate your design time and your product's time-to-market.

Call Oki today for qualification samples. See why so many companies are demanding Oki's low-power, space-saving 4-Megs and SIMMs—and getting their leading-edge computer products to market so quickly.

Transforming technology into customer solutions

Demand Oki 4-Megs and SIMMs

Oki's 4-Meg Product Line-Up

Device	Organization	Access Mode
MSM514100-XXYY	4M x 1	Fast Page
MSM514101-XXYY	4M x 1	Nibble
MSM514102-XXYY	4M x 1	Static Column
MSM514400-XXYY	1M x 4	Fast Page
MSM514402-XXYY	1M x 4	Static Column

Speed Options (XX) Include:
70 = 70ns (t_{RAC})
80 = 80ns (t_{RAC}) 20ns (t_{CAC})
8A = 80ns (t_{RAC}) 25ns (t_{CAC})
10 = 100ns (t_{RAC}) 25ns (t_{CAC})

Packaging Options (YY) Include:
JS = 350 mil SOJ
RS = 400mil DIP
ZS = 400mil ZIP

SIMMs

MSC2341-XXYS8	4M x 8	Fast Page
MSC2340-XXYS9	4M x 9	Fast Page
MSC2350-XXYS12	1M x 36	Fast Page

Speed Options (XX) Include:
70 = 70ns (t_{RAC})
80 = 80ns (t_{RAC}) 20ns (t_{CAC})
10 = 100ns (t_{RAC}) 25ns (t_{CAC})

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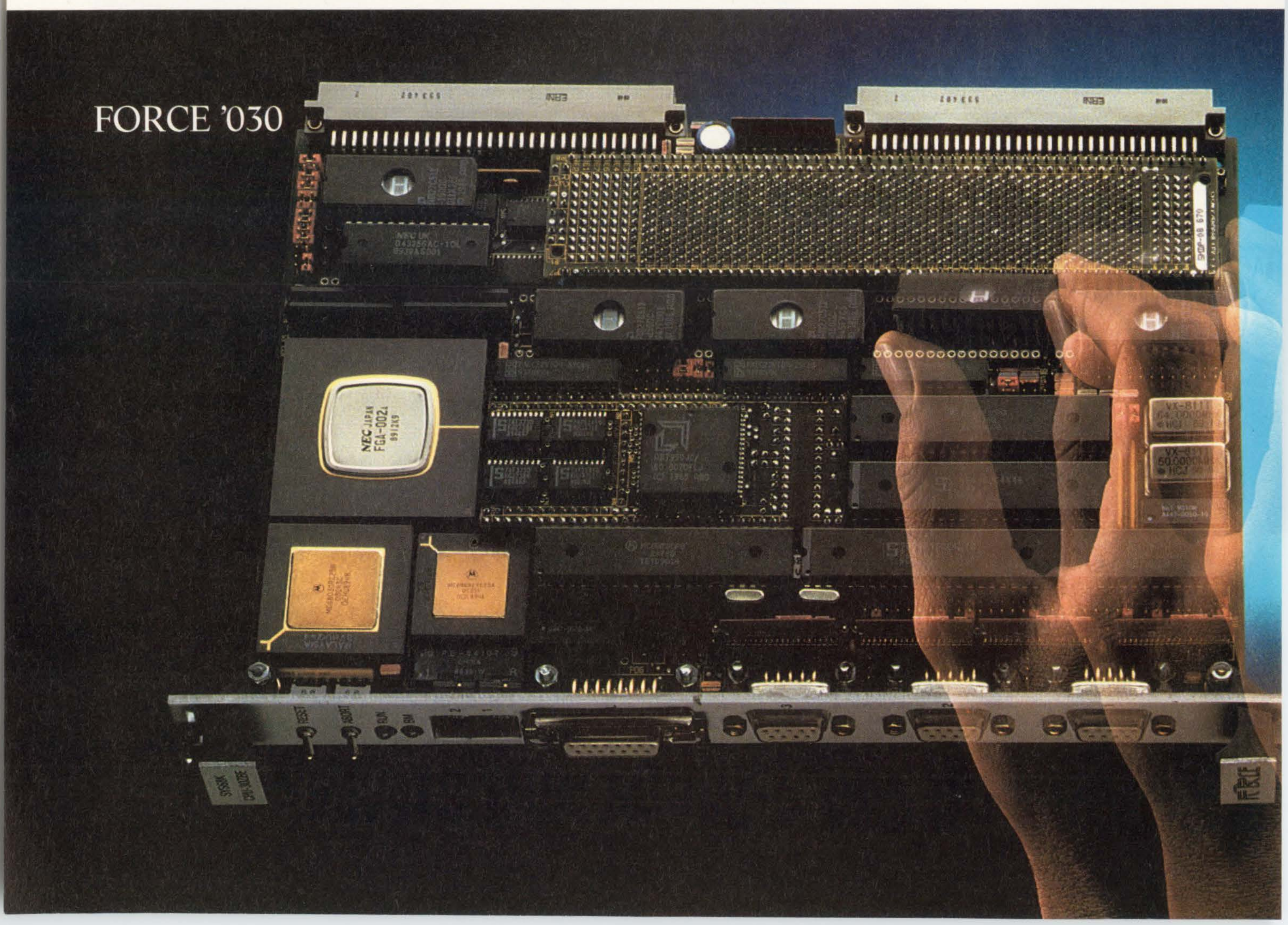
GA Norcross 404/448-7111 **IL** Rolling Meadows 708/870-1400 **MA** Stoneham 617/279-0293 **MI** Livonia 313/464-7200
NC Morrisville 919/469-2395 **NY** Poughkeepsie 914/473-8044 **PA** Horsham 215/674-9511 **TX** Richardson 214/690-6868

CIRCLE NO. 86

HOW TO TURN 040 WITHOUT LOSING A STEP.



Turning 040 doesn't mean you have to give up the code you lived by when you were 030. Although that's what some manufacturers expect you to do.

But not FORCE. We guarantee that applications written for our 68030 VME boards will run on our 68040 boards. That's because we've built compatibility into our 030 and 040 address maps and on-board device drivers.

In fact, no one makes it easier to move your software from 030 to 040. The competition can't even come close. Just ask them.

68030 CPU	COMPATIBILITY	68040 CPU
CPU-30	DMA, SCSI, Floppy, Ethernet, Serial I/O	CPU-40 + EAGLE I/O Module
CPU-31	DMA, SRAM, VSB, Serial I/O	CPU-41 + EAGLE I/O Module
CPU-33	DMA, DRAM, Serial I/O	CPU-40

Then ask us. We'll keep you from spending months writing new software drivers. So you can spend your time improving performance and functionality. Or getting to market months ahead of the competition.

What's more, you can start today on your 040 applications. Just develop them on a FORCE 030 board. When you're ready, we'll upgrade you to the highest performance 040 board you can buy.

So you can speed up your software without missing a step.

Of course, we have all the tools you need to get started. Choose from the broadest range of real-time operating systems and kernels, including PDOS, OS-9, VxWorks, VRTX32 and pSOS+. We even give you VMEPROM, free of charge.

You can also take advantage of XRAY and the entire Microtec family of software tools. Including cross, native and embedded development environments.

Our performance advantage even extends to UNIX.® With the industry's top-rated Unisoft UNIX 5.4.

Finally, you get the industry's best-rated documentation, integration support, regional technical staff and a full one-year warranty.

Here's your next step: call 1-800-BEST-VME ext. 40 for details on our 030 to 040 upgrade offer. Or fax a request to (408) 374-1146 for an immediate response.

Because turning 040 doesn't have to slow you down.

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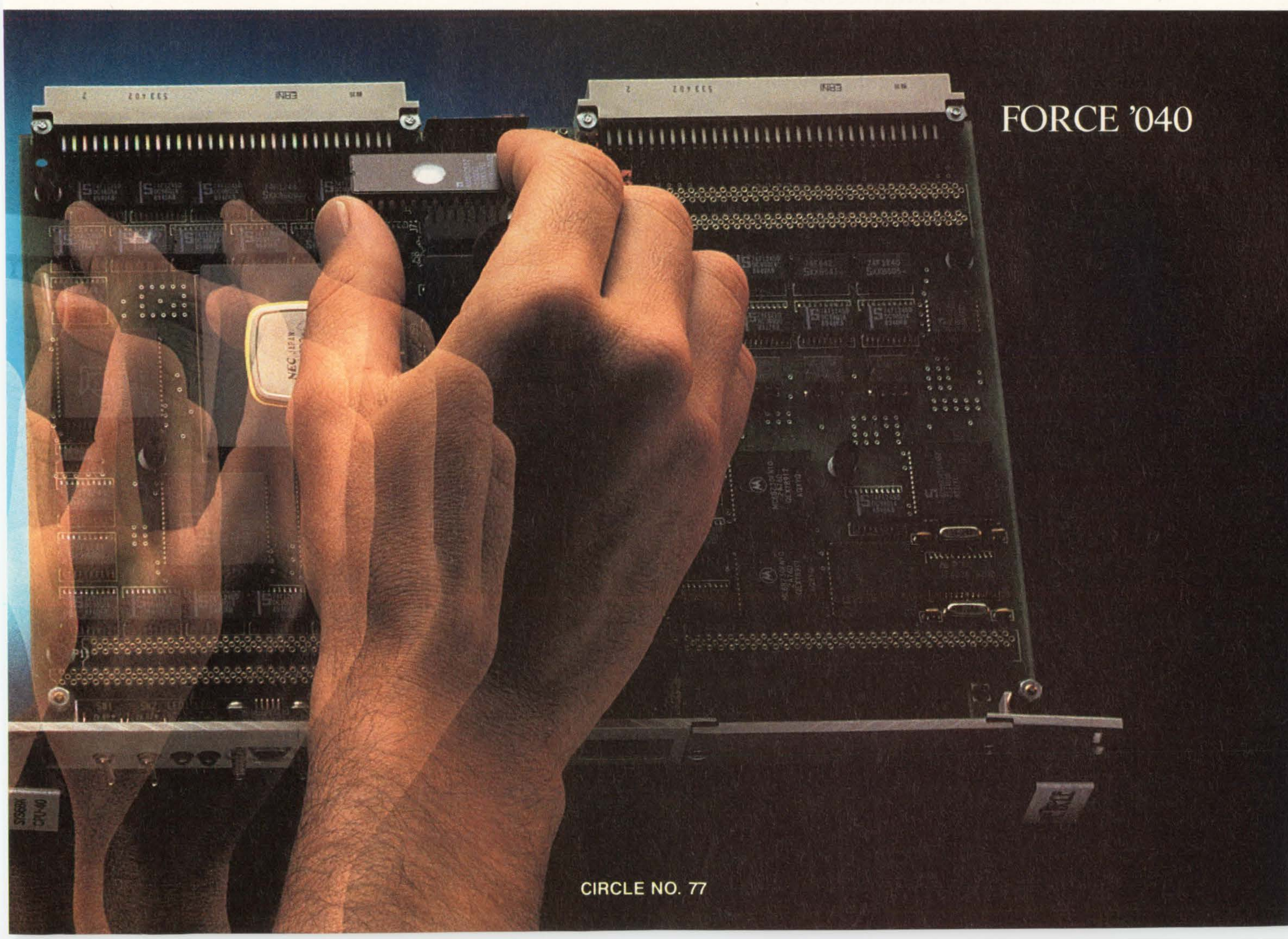


CIRCLE NO. 77

SIGNALS & NOISE

Why don't we try "foreign" approaches to education?

In response to Jon Titus's editorial (EDN, June 7, 1990, pg 41) concerning the education "crisis," it's true, we all bemoan the fact that America seems to be falling behind, compared with some other countries, in providing our children with a sufficient level of "education" skills.

However, if it's so clear that these other countries are doing a better job than we are, why is it that we cannot adopt some of their educational and curricular approaches? I would imagine these to be transferable in some form, even if complicated by cultural differences.

As Jon points out, any changes must ultimately be implemented at the local level, but it would still seem desirable for our national government to provide the necessary leadership, investigation, and guidance for use of approaches from other countries. An evaluation of why some of these approaches might not be viable for us may also provide valuable insight. Surely, someone must have thought along these lines before, but evidence of any action on it is not generally apparent.

Barrie W Witty
Mount Laurel, NJ

Program for improving our children's education

It is very popular in the US media these days to cite declining test scores of US students or to contrast the achievements of US students with those of their foreign counterparts (EDN, June 7, 1990, pg 41). Politicians are quick to seize the issue as a plank in their campaign platforms. Teachers' unions and school administrators are equally quick to use these data as the basis for more appeals for public money.

The real problem lies not in our teachers or our funding but in ourselves. We as parents are to blame. Our lifestyles and our choice of toys and entertainment for our children are working against academic achievement.

Here are some starting guidelines for raising above-average children:

1. Love, respect, honor, and be faithful to your spouse. Fighting, contempt, and infidelity between spouses do not create a healthy atmosphere for children.
2. Dare to be different. Instead of you and your children watching TV shows (serious educational shows are an exception), play cards, dice, and board games together as a family. Pick games that have a measure of intellectual content to them.
3. Get (buy new or used, or borrow) books on subjects your children are interested in and read together. The younger the child, the more pictures the book should have.
4. Let your children pick a hobby and work with them on it. Build models, grow things, or paint.
5. Demand respect from your children and their friends and demand that they give it to their teachers.

The important thing is to be involved with your children. Spend at least 15 minutes a day with them (instead of watching TV), insist on educational entertainment instead of fad toys, and don't be content with being like everyone else.

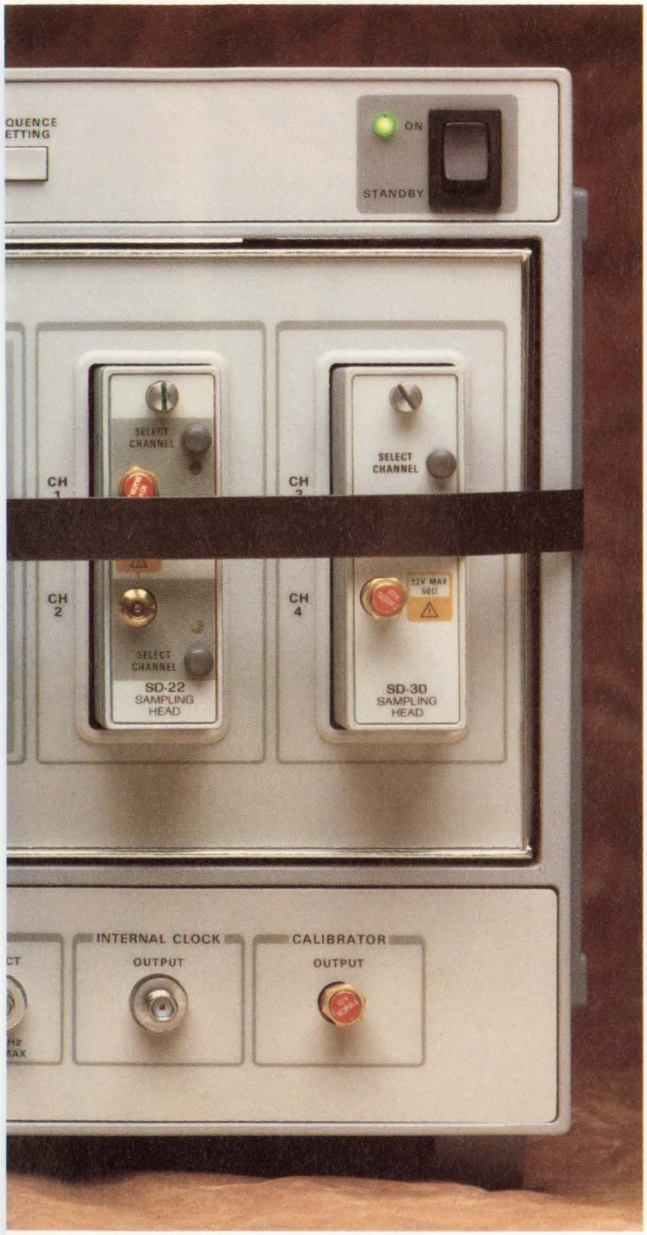
Gary Carlson
Hewlett-Packard Co
Boise, ID

Correction

In Richard Quinnell's article on 32-bit embedded controllers (EDN, May 24, 1990, pg 132), Wind River Systems' VxWorks Real-Time Operating Systems were incorrectly listed as running on the Intergraph Clipper RISC processor architecture. Although VxWorks currently supports target systems based on the Motorola 680x0 series, Sun SPARC, and Intel 80960, none of the software has been ported to the Intergraph Clipper. EDN

Tek's 40 GHz
All tied

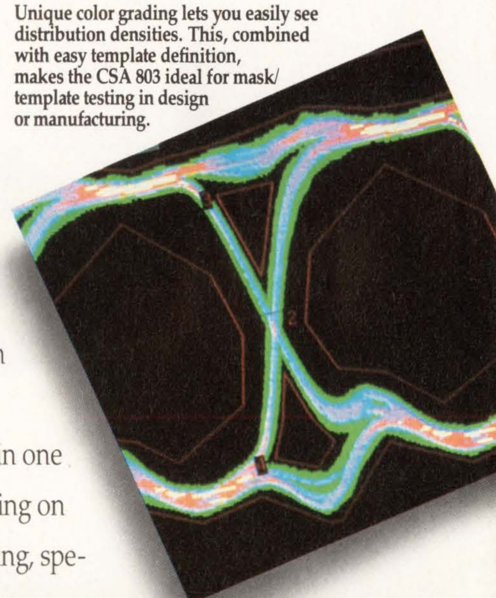
communications test system. up in one neat package.



Introducing the Tek CSA 803 Communications Signal Analyzer. As of now, working with high-speed optical and electrical signals is no reason to go to pieces.

Now you can fully experience a real-time feel for waveform throughput and manipulation. Do in-depth statistical analyses of noise and jitter. Trigger on signals of up to 10 GHz. Do on-board mask testing, constellation diagrams, and more.

And, you do it all from within one tailored instrument, without calling on external computers, clumsy cabling, specialized software or costly add-ons.



Unique color grading lets you easily see distribution densities. This, combined with easy template definition, makes the CSA 803 ideal for mask/template testing in design or manufacturing.

A powerful on-board statistical data base lets you easily see data distribution densities via color-graded displays. For the first time, you can generate jitter and noise histograms without reacquiring data... and enjoy continuously updated statistical readouts of mean, RMS deviation and p-p at the same time. A sample rate 20 times faster than its nearest competitor lets you analyze data concurrent with acquisition.

You can define, edit and store masks for tolerance testing: the CSA 803 automatically counts the samples that fall within each mask. Constellation diagrams, for qualitative digital RF testing, are also provided.

Easily expand to meet your needs and new evolutions of technology. Start with one channel if you wish, and add more channels up to a total of four. Choose from a large and still-growing selection of plug-in sampling heads, optimized for your application. The CSA's modular design lets you upgrade without adding an inch to its footprint.

Call 1-800-426-2200 for the complete CSA 803 story. Or let your Tek sales engineer show you the whole package soon.

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CIRCLE NO. 87

FILTERS

dc to 3GHz from $11^{45}

lowpass, highpass, bandpass, narrowband IF

- less than 1dB insertion loss • greater than 40dB stopband rejection
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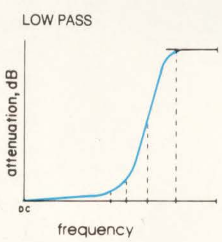
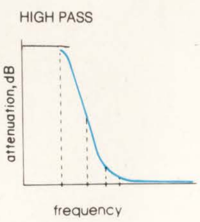
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery



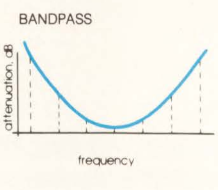
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



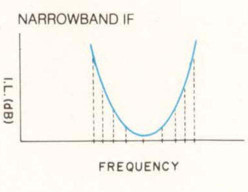
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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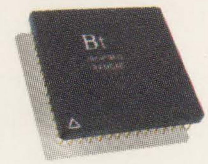
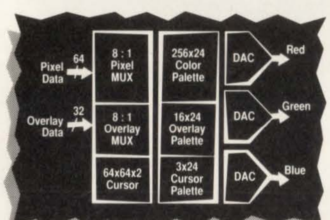
F132-2 REV. ORIG.

When a Picture is worth 1600x1280 Pixels.



Our new 200 MHz RAMDAC, with 8:1 MUX and 2-plane cursor makes it easier than ever to design new 1600x1280 graphics systems.

When's the time to make the move to higher resolution 1600x1280 monitors? NOW! Our new Bt468 triple 8-bit RAMDAC delivers the functional richness and pure performance you need to tackle next-generation designs.



To begin with, it's a 200 MHz monolithic CMOS device. And while we could wax rhapsodic on our technical achievements in pushing CMOS to such an unprecedented speed, we recognize that such data rates are absolutely necessary for high performance color graphics.

So we also gave the Bt468 multiple pixel ports and internal multiplexing to enable a direct TTL-compatible interface to the frame buffer. On-chip 8:1 multiplexing reduces external logic and means you can design your system with low cost 25 MHz VRAMs.

We've given the Bt468 its own user-definable 64x64 hardware cursor to further simplify your design. And our exclusive Pixel Panning feature lets you add smooth image panning without any additional overhead for your graphics processor. By the way, the Bt468 is also available in a lower cost **170 MHz** version, so your board design will be compatible with lower refresh rates, too.

So if your system is worth 1600x1280 pixels, now's the time to **call Brooktree at 1-800-VIDEO IC.**

Brooktree®

CIRCLE NO. 90

THE NEW MAGIC NUMBERS IN DATA CORRELATION

Micro Devices' new MD1212 Fuzzy Data Correlator brings a new set of realities to real-time data analysis and signal processing.

Limited to 64-bit word length? Not any longer! A single MD1212 can perform a 128-bit correlation — and the units can be cascaded to process data segments of any length.

Restricted by response time that's too slow for meaningful real-time work? No longer! The MD1212 operates at a 50 MHz clock rate. Exact matches are verified in one clock cycle; close matches (determined by Hamming distance measurement) are available in three clock cycles.

Perplexed by exotic interfaces? Unlike similar devices, the MD1212 can be controlled via a standard 8-bit microprocessor interface.

Frustrated by budget-bending device prices? Order the MD1212, in 1000-piece lots, at just $29 each (single quantity only $35).

For image recognition, radar/sonar pattern matching, error detection, video frame synchronization, spread spectrum, flag word detection and other critical correlation applications, the MD1212 is the high-performance, low-priced solution. For technical details, contact:

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Lake Mary, FL 32746-6201 USA
Telephone 407/333-4379
FAX 407/333-4479

CIRCLE NO. 91


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For now, forget the USSR

The opening of trade barriers with Eastern European countries and the liberalization of their governments is encouraging companies to see these areas as untapped markets. Many people are also looking at the USSR as a market of vast potential—much as people viewed China in the 1980s. Although the USSR's former satellite countries may prove to be lucrative markets, don't rush into the USSR. It will get harder and harder for businesses to work in the USSR for many reasons. We advise using a great deal of caution.

Now that trade with the USSR can involve deals between individual companies, many western businesses are finding it hard to get paid for shipments to the USSR. Prior to the spring of 1989, the USSR guaranteed payments for all imports. Now, individual companies and enterprises are responsible for their own bills. Many aren't paying regularly; some aren't paying at all. The *Wall Street Journal* estimates that the USSR's total of unpaid import bills reaches \$2 billion.

The Soviet Union is woefully short of hard currency with which to conduct its trade, and some companies have to resort to taking payment in kind—exports which may have little market value in western countries. The USSR is also short of business managers, economists with market-economy experience, and bankers who can handle the hundreds-fold increase in commercial transactions. Anyone contemplating business with a company in the USSR should think long and hard about the venture.

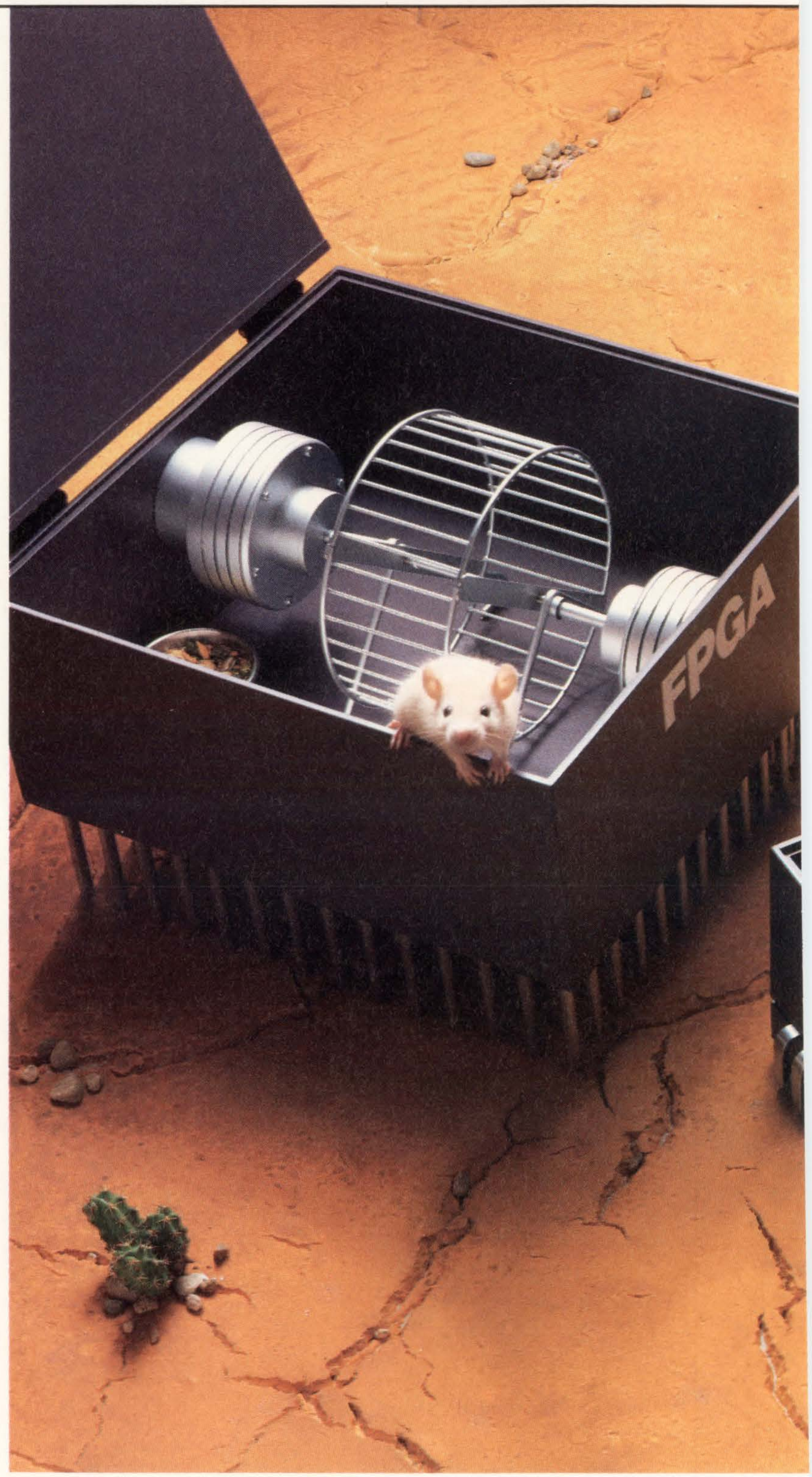
Unlike its former European satellites, the USSR has yet to restructure its economy to account for unemployment and bankruptcy. Thus, scarce monetary and material resources drain the USSR's reserves by continuing to flow into dead businesses. A recent spending spree on imported consumer goods did little to ease the demand for such goods, but it damaged the USSR by causing a liquidity crunch. These events and conditions should harden our attitude toward doing business in the USSR.

Meanwhile, inflation is starting to rear its ugly head in the USSR. Wages are rising at a rate approaching 15% while the country's GNP decreases. The result is a reported 20% inflation rate. As prices rise, farmers and manufacturers are reluctant to turn over their produce and products to state organizations that pay them at an official rate. They can make more money selling goods on the black market where goods command freer-market rates.

Karl Marx's mother is reported to have said, "If Karl, instead of writing a lot about capital, made a lot of capital, it would have been much better." No doubt many in the USSR today would agree.

Jon Titus
Editor

BEFORE YOU CHOOSE P
BETTER CHECK



Things aren't always what they seem.

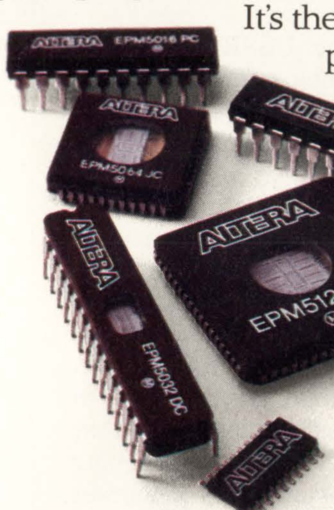
Some people would have you believe FPGAs are faster and denser than MAX™ EPLDs.

Funny how they never mention *in-system* performance, though. When they talk about speed, they quote 100MHz flip-flop toggle rates. When they talk about density, they recite raw gate counts.

Which could make your high-performance design highly disappointing.

But if you want to do more than just spin your wheels, consider MAX.

It's the first family of programmable logic

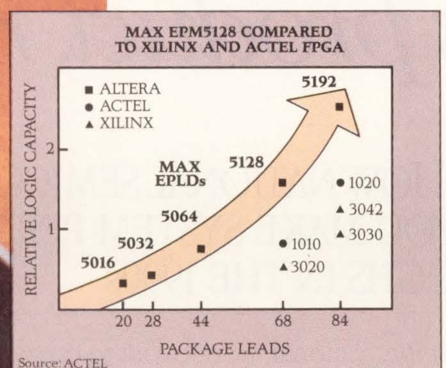


devices to provide both high speed and high logic density where it counts. At the system level.

Which means MAX can handle just about all your logic needs. In fact, a single 64-macrocell EPM5064

ROGRAMMABLE LOGIC, UNDER THE HOOD.

can integrate anything from simple system glue logic right up to complex graphics coprocessors and LAN and memory controllers.



Or take the 68-pin MAX EPM5128. It's up to 50% faster and 100% denser than comparable FPGAs, thanks to its high-performance architecture and superior logic routability. But don't take our word for it—just take a look at the competition's benchmarks.

Best of all, MAX gives you this unbeatable performance in record time. With powerful, easy-to-use MAX+PLUS™ software, design compile times are measured in minutes. Not hours or days.

So if you're looking to redefine system performance, talk to the folks who invented the EPLD. Call Altera today at (408) 984-2800.

We'll make sure you've got plenty of horses under the hood.

ALTERA

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National Semiconductor

"Everyone today is and digital on the same chip–but That's product, not promises."

HOW NATIONAL SEMICONDUCTOR IS HELPING YOU MAKE SYSTEM-PERFORMANCE BREAKTHROUGHS IN THE 1990s.

Graham Baskerville, National Semiconductor's Vice President, Linear Product Development, and *Charlie Carinalli,* Vice President, Integrated Systems Group, talk about the challenges of mixed analog+digital technology.

Breaking the ISDN logjam at the U interface.

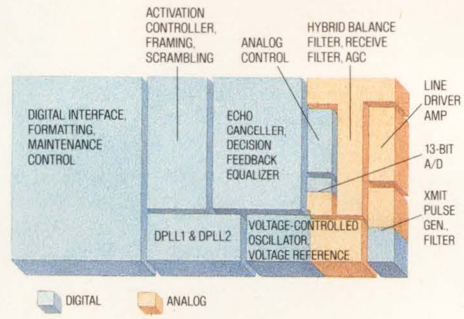
"This may be the most technically complex integrated-analog-and-digital device ever designed. It's our TP3410 U-interface transceiver for ISDN."

"It's the missing link that allows the twisted-pair telephone network to carry simultaneous voice and high-speed data across the subscriber loop to the telco central office."

"It's all CMOS, for high density, low power, and scalability—it's at 1.2μm, but we're already planning a shrink to 0.8μm."

"And we can control that shrink because we designed the die in modules, separating the analog and digital functions. We even gave them their own power and ground supply pins to isolate the noisy rail-to-rail switching of the digital from the sensitive circuits of the analog."

"Over 100K transistors with a single +5V supply, all in a 28-pin DIP that dissipates 300mW. Nobody else has a solution this advanced."



Setting a new standard in A-to-D conversion.

"Our ADC1241 is another example of our unique strength in combining complex analog and digital functions on the same substrate."

"It has an analog front end for data acquisition, but then we've implemented a powerful self-calibration function in digital. During each conversion, it performs a self-correction cycle, reducing nonlinearity errors to less than ±½ LSB."

"So we get 12-bit-plus-sign resolution with an accuracy that's guaranteed over the full mil temp range. Nobody else can do this."

ASIC D/A Converter

ISDN U Interface

Super I/O

Hard Disk Synchronizer/ENDEC

Custom Linear ASICs

A/D Converter

talking about integrating analog we've been doing it for years.

Pushing the limits of PC integration.

"Here again, in our new Super I/O chip, PC87310, we've integrated analog and digital to a level that's never been achieved before."

"Industry-standard floppy-disk controller and UARTs, a parallel port, IDE hard-disk address decode,..."

"With analog PLLs in the floppy controller for pulse detection and data separation."

"All-digital is easier to build, but the performance suffers. And that's not a compromise we're willing to make."

Meeting our customer demand for mixed analog+digital ASICs.

"We call this CLASIC — Custom Linear ASIC. We use standard-cell methodology and optimized process technologies to offer high-performance VLSI solutions combining analog and digital functions."

"The CLASIC library right now has more than 500 analog cells and a good selection of digital building blocks."

"But again, it's not just functions, it's processes. We can fab in the process best suited to your design — linear bipolar, linear CMOS, BiCMOS."

"True customer focus."

continued next page

National Semiconductor

The challenge of integrating analog and digital functions onto the same chip.

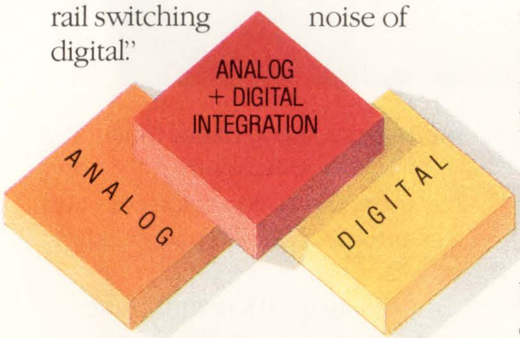
"The demand for mixed analog+digital really is customer-driven. Our customers need to build systems with higher performance because their customers are demanding it. Because their applications need it."

"And the way to achieve higher levels of performance is through higher levels of integration. Which, at the chip level, ultimately demands that analog and digital functions be pulled together onto the same substrate."

"And this is like trying to merge two incompatible universes."

"Digital's goal is smaller, faster, denser. The world turns on lithography. It lives for the shrink."

"Analog, on the other hand, is concerned with precision, linearity, dynamic range, bandwidth, phase shift, component matching, microvoltage sensitivity. And it simply can't tolerate the clanging rail-to-rail switching noise of digital."



Meeting the challenge with world-class products.

"Our U interface is a perfect example of how difficult this really is. ISDN is digital, but it has to operate over the existing telephone wiring using analog signals. And there's only one twisted pair. So your transmit and receive signals appear on the same terminals. You send 160Kbits/sec digital pulses at 2.5V and it has to travel maybe three or four miles over the subscriber loop without repeaters or amplifiers. Over that distance, you're getting up to 40dB attenuation, so it arrives at about 25 *milli*volts. So the problem is, how do you pick that signal out of all the noise and the local transmit signal, which is 100 times more powerful?"

"You need low power, so if you tried to do it just with analog filters, it would be too complicated and too sensitive to process variations. But if you tried all-digital, it would be too complex to compensate for the limitations of the analog front end. So we combined analog filtering and a 13-bit A-to-D converter onto a single chip with dedicated DSP."

"The point is, we did it."

Meeting the challenge with world-class analog and digital designers.

"Building something like the U-interface transceiver demands some of the most sophisticated design techniques in the world."

"And not only are the individual analog and digital functions difficult to design, but then you have to integrate them onto the same chip."

"So you need world-class digital designers, world-class analog designers, and strategic partners who know how to work together."

"We've got them all. And they've been working on joint designs for many years."

"That's how we do it."

Meeting the challenge with world-class process technologies.

"Another problem for chip designers is that they are limited to the process technologies available to them."

"But, because of our heritage in both analog and digital, we've developed probably the broadest range of process technologies of any company in the industry, including bipolar, CMOS, and BiCMOS."

"We employ a 'core-process' concept. We have six basic core flows, then we add modules for specific functions."

"We can take our advanced M²CMOS core, for example, and add a bipolar module. Or a linear capacitor module. Or EEPROM. Or we can do a bipolar core with a CMOS module. Or we can go to BiCMOS. Or LFAST or LMCMOS or DMOS or JDMOS."

"The key is, our designers have the freedom of selecting the best combination of processes for every analog and digital chip. The application drives the process choice. Not the other way around."

Meeting the challenge with world-class design tools.

"When you try to put analog and digital together, all the existing simulators, place-and-route CAD software, and behavioral models fall apart."

"So we've developed our own. And we're working closely with one of the world's leading CAD-tools companies to create a universal, end-to-end design environment."

"But already our ASIC Division has used our DA4 tools to introduce significant new standard cells, some of which allow high-voltage outputs to be combined with +5V CMOS to 30,000 gate densities."

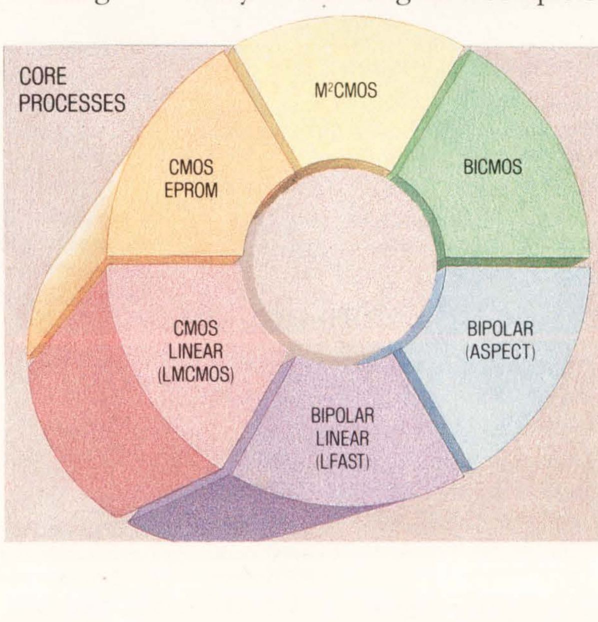
"So now, for example, you can put logic, RAM, ROM, or EEPROM on the same chip with D-to-A converters and high-voltage drivers."

"No one has ever done this before."

"And it's only the beginning."

Putting the pride of National to work for you.

"The point is, our customers *need* mixed analog+digital capabilities. And we can offer that to them today. We can integrate a complete system solution for them. Or we can work with them at a particular phase in their design. We have the right products, the right processes, the right tools, the right people. And we're putting all of it just a simple phone call away."



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National Semiconductor

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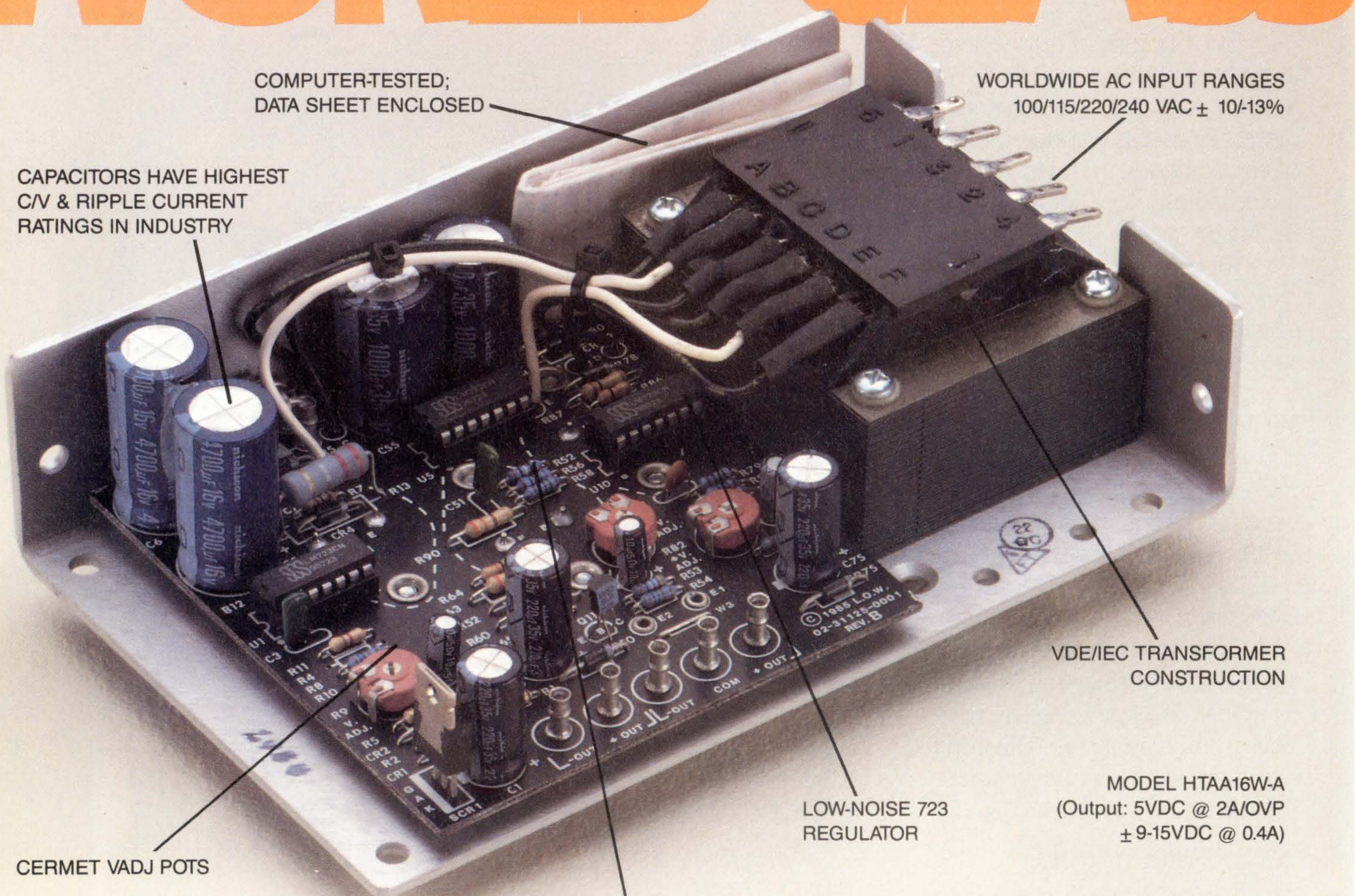

Condor's International linear power supplies — certified to UL544.

Condor's *International Series II* D.C. power supplies virtually eliminate primary-secondary shorting because each coil uses a separate bobbin surrounded by two layers of glass-impregnated plastic, giving complete mechanical and electrical isolation.

The best low-noise 723 regulator chips are used throughout the line, together with proven, reliable semiconductors. TO3-cased pass elements are hermetically sealed, and the latest high-density, high-ripple current rating capacitors from proven, high-quality vendors ensure long life and reliability.

International Series II features:

- 7 power levels — 3 to 150W
- 70 models (single, dual & triple output)
- OVP on all 5V outputs
- Meets EMI per FCC/VDE B (most units)
- Hermetically sealed power transistors
- MTBF 200,000 + hours per Mil Hndbk 217D
- 2-hour burn-in with cycling
- Full 3-year warranty
- 5th-generation design by Tom Ingman — most copied designer in the power supply industry

Sixty-five *International Series II* models are approved to UL478/1012; CSA C22.2 and TUV certified to VDE 0806 and IEC 435, 1 & 2. Twenty-six models are also approved to UL544. Call us today and put Condor's world-class power supplies to work for you!

Send for our free catalog!

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Switchers and linears!
Open frame and enclosed!
Custom capability!

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CIRCLE NO. 93

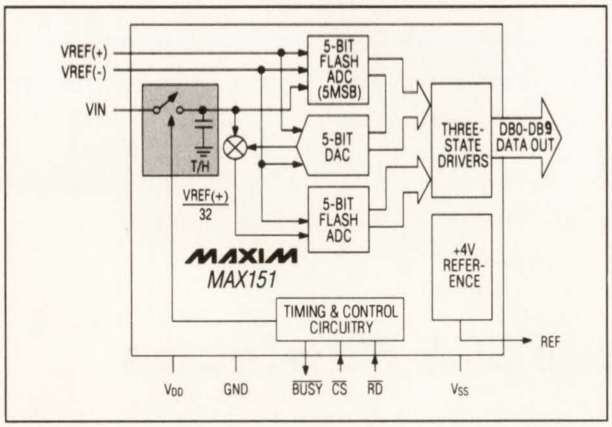
MAXIM DESIGN NEWS

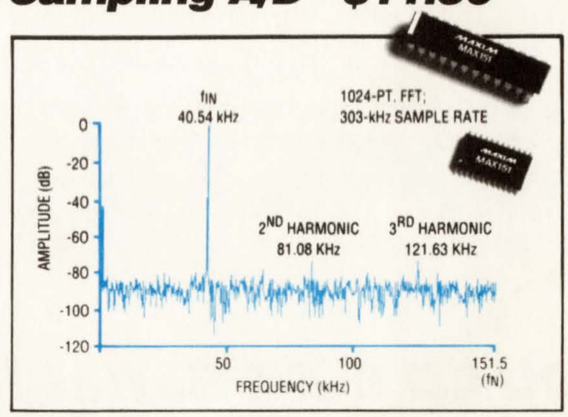
Analog Design Insights from Maxim Integrated Products

Fast 10-Bit Sampling A/D Converters Include Reference, DC and Dynamic Specs

Maxim's new 10-bit analog-to-digital converters come complete with internal voltage reference, track/hold, and clock - *saving valuable board space*. The MAX151 and MAX177 are ideal for applications such as digital-signal processing, audio and telecom processing, high-accuracy process control, electro-mechanical systems and high-speed data acquisition.

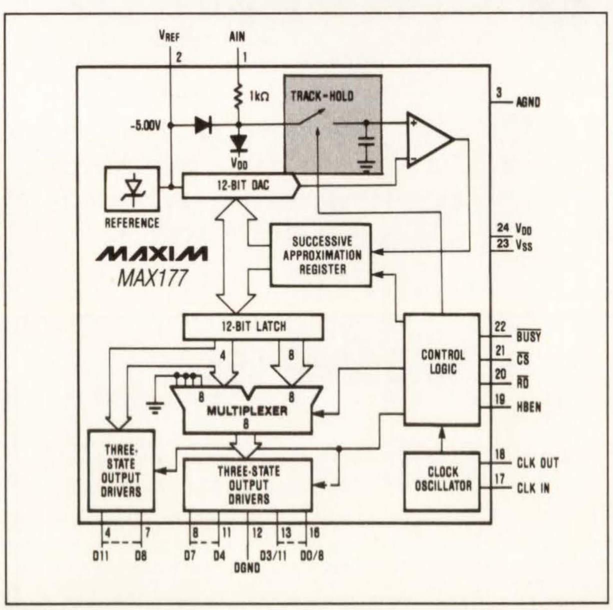
MAX151 - 300kHz/2.5μs 10-Bit Sampling A/D - $11.50*





- ♦ 100% Tested for DC and Dynamic Accuracy
- ♦ ±1 LSB Total Unadjusted Error
- ♦ Internal ±60ppm/°C Voltage Reference
- ♦ No Missing Codes
- ♦ 0 to +5V Input Range with ±5V Supplies
- ♦ 5MHz Full Power Bandwidth
- ♦ ±1ppm/°C Gain and Offset Drift
- ♦ Complete with Internal Track/Hold, Clock, Ref
- ♦ 275mW Power Consumption, Including Ref
- ♦ Small Footprint SO and DIP Packages

MAX177 - 100kHz/8.33μs 10-Bit Sampling A/D - $7.90*

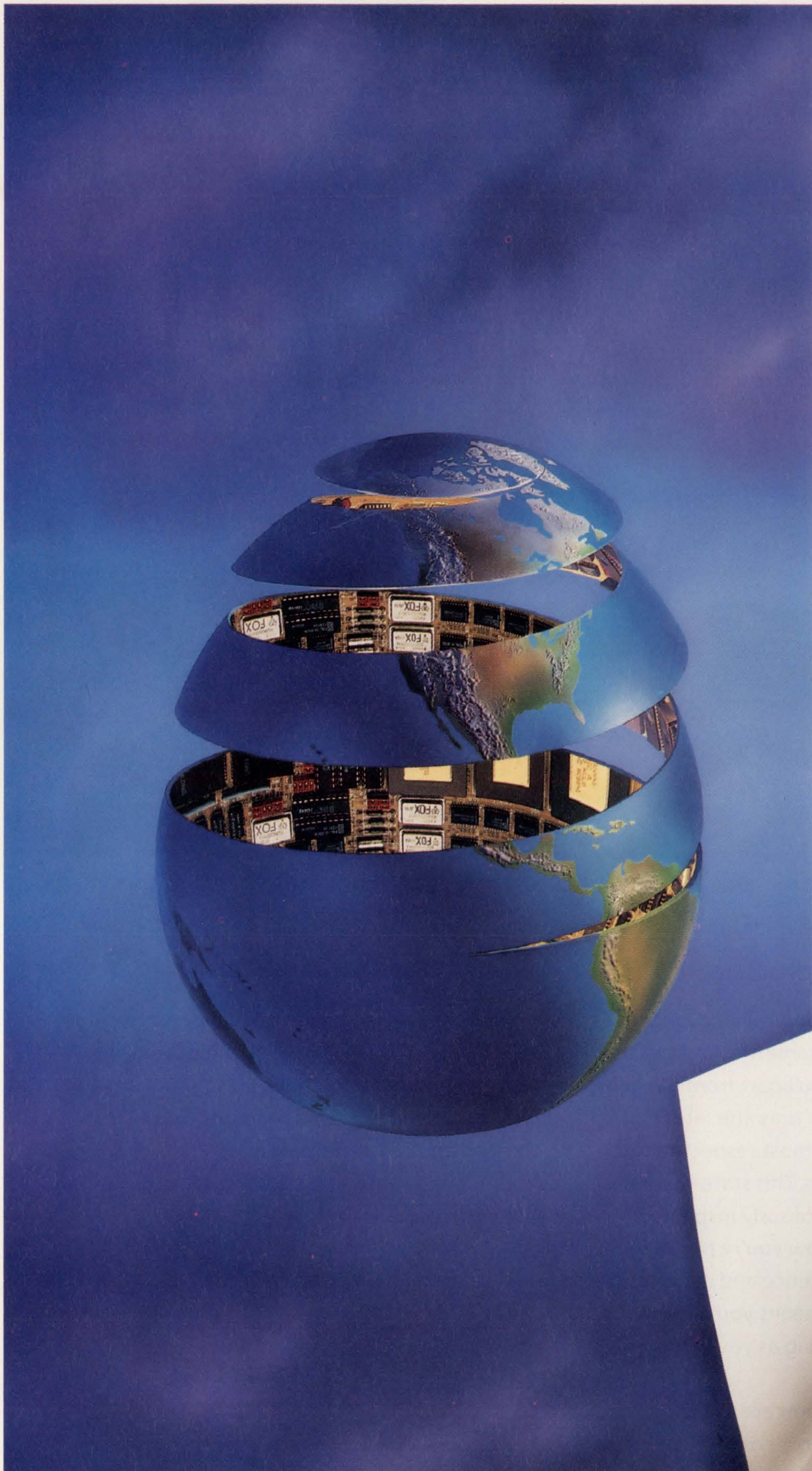


- ♦ 100% Tested for DC and Dynamic Accuracy
- ♦ Internal ±40ppm/°C Voltage Reference
- ♦ No Missing Codes
- ♦ -2.5V to +2.5V Input Range
- ♦ 6MHz Full Power Bandwidth
- ♦ High Input Impedance (500MΩ)
- ♦ Complete with Internal Track/Hold, Clock, Ref
- ♦ 8- or 16-Wide μP Interface
- ♦ 180mW Max Power Consumption, Including Ref
- ♦ Small Footprint SO and DIP Packages

For applications that don't need the track/hold function, Maxim offers the MAX173, essentially a MAX177 but with 5μs speed, +5V input range at $7.00*.

* Price 1000-up FOB USA

SBE...At the Core of WAN Interface Solutions



The SBE VCOM-4 Multiprotocol Communications Controller ... *today's high-performance, cost effective WAN interface.* For price-performance in a *single* VMEbus communications controller, nothing equals the new SBE VCOM-4.

This exclusive SBE card features *four* full-duplex, independently programmable serial channels. Yet, it takes up only one VMEbus slot and provides twice the throughput of conventional boards. A complete implementation of X.25 is available ported to the VCOM-4, which speeds your product to market.

The result: an unmatched WAN interface for VME-based hosts, front-end processors, and data/voice networking systems, including: ▪ Two channels at T1 speeds. ▪ All four channels can operate with *sustained* throughput at speeds up to 768 Kbps, interfacing to fractional T1 services or 56/64 Kbps lines. ▪ Each communications channel can be *independently* configured to support HDLC, SDLC, Bisync, Async.

Turn to SBE and the VCOM-4 for the core of your VMEbus WAN product design application. For fast action, contact SBE, Inc., 2400 Bisso Lane, Concord, CA 94520, or call **1-800-347-COMM.**

CIRCLE NO. 95

SBE
Communications & Real-time Solutions

FPGA vendors race to upgrade products

Inevitably, field-programmable gate arrays are luring digital engineers to a design realm where ideas become real immediately and design iterations are effortless. But making sense of the goings on in the FPGA industry isn't easy.

Charles H Small,
Senior Editor

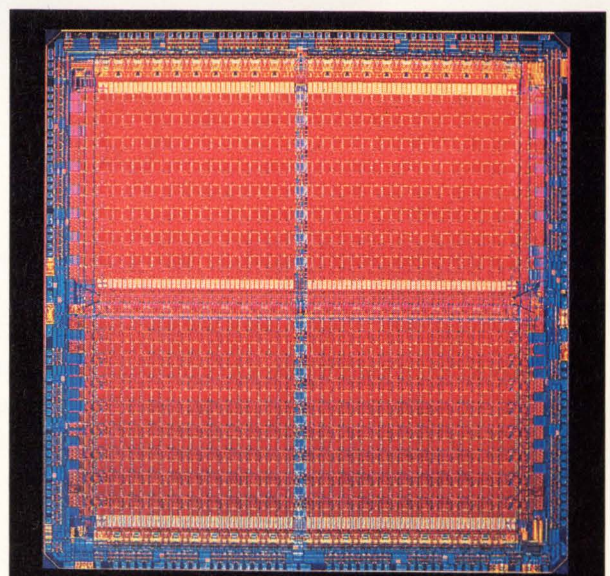
One look at a function-packed pc board bearing a field-programmable gate array (FPGA) should be enough to convince all digital designers to usher these devices onto their pc boards. You can expect to consolidate as many as 10 PAL-device chips or 50 TTL-device chips into a single FPGA (**Fig 1**). Such a reduction makes a dramatic, immediately perceptible difference in the layout of a digital pc board.

A second, closer look at FPGAs discloses, however, a bewildering blizzard of issues and "advantages." Making sense of the goings on in the FPGA field is a trying task because several innovative, highly competitive companies are constantly working and reworking their wildly different approaches—so different, that even giving these parts a name is problematical (see **box,** "Nomenclature: the pesky problem that won't go away"). However disparate their paths, these companies all have a common goal: to sell you large devices that you can program, on site, to hold *big* digital designs.

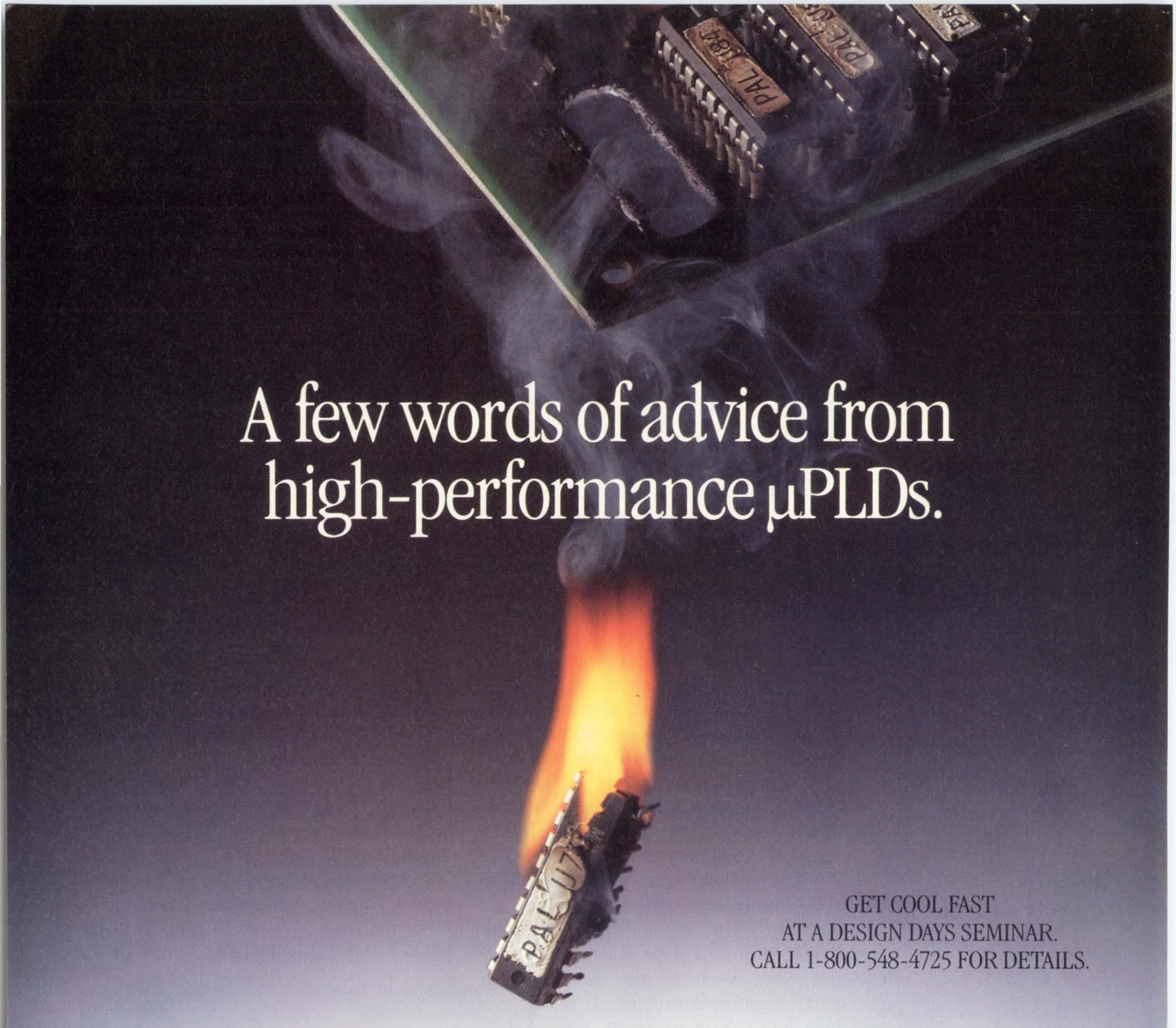
But any reckoning you make today of the relative merits of these devices could be wrong tomorrow. Judging from their records to date, FPGA vendors will do whatever it takes to make their parts and software work. For example, Altera has already altered the classical PAL-device architecture twice in the company's efforts to scale the basic design up in size and make its architecture less rigid.

Their first EP-series devices vacuumed up a handful or two of 22V10-like devices onto a single chip and added an interconnection array to link the devices' inputs and outputs. But these chips retained the classical PAL devices' characteristic of having a fixed number of product terms per output macrocell. The architecture of the company's second-generation Max PAL-like FPGAs has, in addition to a small number of fixed product terms, floating product terms that you can allocate at will to any macrocell.

Despite these architectural improvements, some designers fault the Max devices for their power consumption, expense, and lack of speed. But Altera



With a claimed equivalent of 8000 gates, *the Actel A1280 second-generation FPGA differs significantly from the company's first-generation devices.*



Chill out, PAL.

Many designers have hot, high-performance designs. Literally.

Fortunately, Intel has a simple way to reduce system heat and still get incredible performance. The μPLD Family of programmable logic devices.

Take, for example, the 85C220 and 85C224. They operate at 80MHz (100 MHz internally) with only a 10ns total propagation delay.

And since μPLDs are manufactured using Intel's CHMOS* technology, they require just 1/4 the power of their pin-compatible bipolar PAL* alternatives. Which means they can lower system heat by 35 percent and help reduce board-level failures, too. So they're certain to give your high-performance system a boost. And send chills up the spine of your motherboard.

Learn more about Intel μPLDs and receive a μPLD/PAL heat comparison. Call (800) 548-4725 and ask for Literature Packet #IA28.

Otherwise, you could take some heat over your system design.

intel®

CIRCLE NO. 96

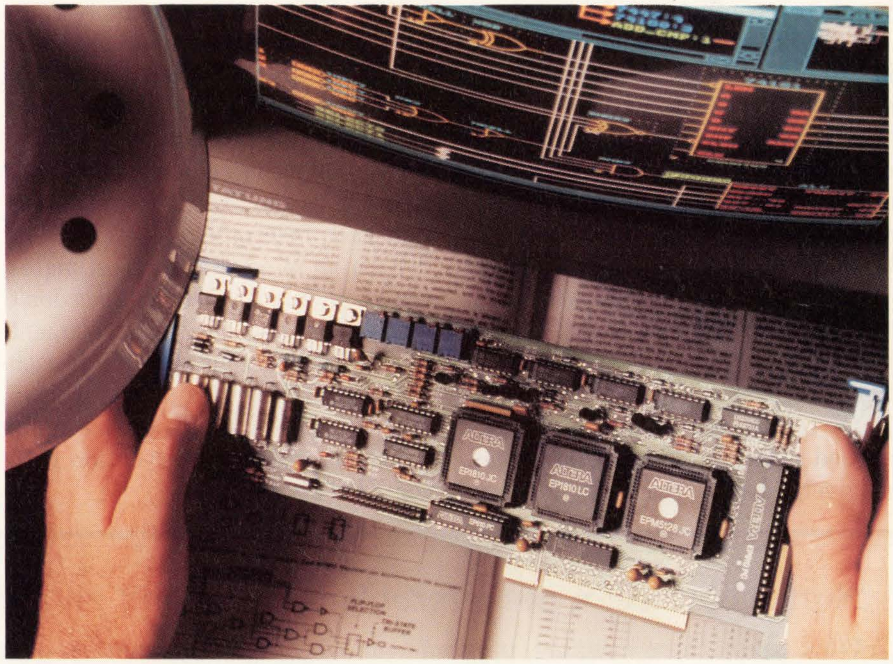
continues to field faster, as well as larger, devices.

The architecture of Plus Logic's Plus FPGAs has evolved far beyond that of conventional PAL devices. Yet some flavor of the original remains. The Plus FPGAs still have a plane of combinatorial logic that sums into programmable macrocells. To eliminate layout-dependent timing variations, the device's designers strove to make every path through the device have the same delay.

The recently announced Mach series of PAL-like FPGAs from Advanced Micro Devices (AMD) takes another tack to solve the problem of enlarging the classical PAL-device architecture. Using a scheme reminiscent of Intel's 5AC312, the Mach devices allow you to rob bundles of product terms from one macrocell and divert them to an adjacent macrocell.

In addition to the three PAL-like FPGAs already being offered, look for two more variations on this basic theme from Atmel and Lattice at the end of the year.

The pace of architectural change is also rapid in logic-cell FPGAs. In scaling up its devices, Xilinx has increased both the routing resources between logic cells and the amount of logic in each logic cell. Increasing the logic in each cell reduces the need to map a function over several cells, thereby decreasing the strain on logic-cell interconnections. Increasing the number of interconnections obviously makes routing a design easier.



FPGAs allow you to dramatically increase *the amount of logic on your pc boards. (Photo courtesy Altera Corp)*

Actel's recently announced Act 2 logic-cell FPGAs differ significantly from the company's Act 1 devices. In addition to more interconnection lines and more inputs per logic cell, the new devices have a checkerboard of combinatorial and sequential logic cells. In other words, now half of the devices' logic cells have flip-flops in them.

Plessey's Era logic-cell FPGAs have not been around long enough to get an update. Only one member of the announced family is actually available. The devices exhibit the least amount of logic—or finest "granularity"—per logic cell of any logic-cell FPGA. Plessey states that this fine granularity will make upgrades to mask-programmed gate arrays easy.

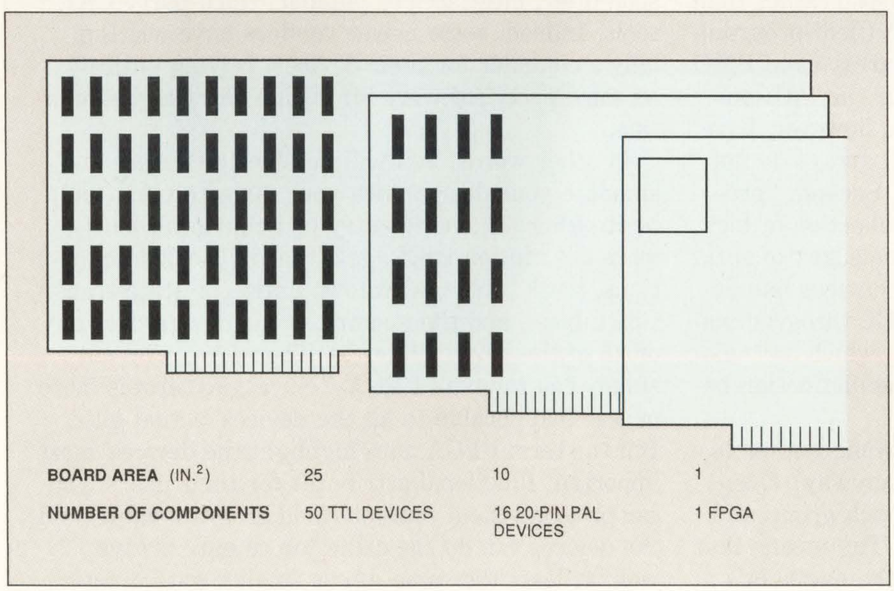


Fig 1—Field-programmable gate arrays *(FPGAs) can vacuum up a dramatic amount of logic. (Courtesy Altera Corp)*

Will it fit?

Given the rate of change of each company's devices and the new companies entering the fray, the jungle of conflicting claims about FPGAs is sprouting and thickening at rain-forest rates. Rather than immediately trying to hack through the tangle of claims and counterclaims about the various FPGAs, step back a pace and consider that, above all else, you need to know three things about an FPGA: Will your design fit? If it fits, will it run fast enough? If it fits and runs, can you afford it?

FPGA users polled informally by EDN report few problems getting a good estimate of whether or not a given design will fit into an FPGA. The engineers simply compare the gates and functions they estimate that their proposed design will need to the so-called macromodels in an FPGA maker's library. These library models list the amount of an FPGA's resources that each macromodel uses up.

Keep in mind that such estimates are good only for designs that don't attempt to use every last element in an FPGA. Designs that approach 100% utilization of a device still require careful planning and a certain degree of manual intervention with the FPGA's software.

Relying on each manufacturer's own estimate of their devices' "equivalent gates," instead of doing your own estimate, is risky. The equivalent-gate spec is rapidly approaching the stature—or lack thereof—of the MIPS spec in the computer world. **Refs 1** through **4** typify the tendentious nature of equivalent-gate claims. In one paper, an application engineer makes his company's devices suddenly grow in capacity by a factor of four by employing his competitor's method of counting gates.

Getting a good specification for

Nomenclature: a pesky problem that won't go away

What to call these new, big, programmable devices? The common sense or familiar names are all locked up under copyrights, not available to general use. Some of the devices comprise arrays of logic cells surrounded by a matrix of programmable interconnections. But you can't call them LCAs (logic-cell arrays) because Xilinx owns the term. Other devices are very reminiscent of PAL devices. But when AMD bought MMI, the company also got the jealously guarded trademark for PAL. Consequently, something like BPAL (big PAL) or RBPAL (really big PAL) is out of the question.

One industry pundit, taking a physical rather than functional approach, suggests FPGA (field-programmable gate array) for the logic-cell arrays and PMD (programmable multilevel device) for the PAL-on-steroids types. Both of those terms, however, have major problems. First, the logic-cell arrays do not, in fact, resemble gate arrays at all. Second, "programmable multilevel device" is a collection of big words that suggests little beyond some sort of automated-warehousing system. Third, devices like International CMOS Technology's PEEL (programmable electrically erasable logic) array, which have elements of both categories, muddy the distinction between the two groups.

More to the point, why should anyone bother to divide the devices into two groups anyway? Even after grouping, the devices within each group still have wildly different architectures. The means that the devices' designers use to meet the engineer's goals are moot so long as the devices measure up. In other words, the grouping is a distinction that makes no difference.

What's more, trends in software are indeed making pointless any distinguishing between devices' basic architectures. When the devices first came out, no third-party software existed for them. Consequently, most device makers also offered custom software for their devices. You had to master a separate software suite to work with each device. And, in some cases, you had to be intimately familiar with a device's architecture to use its software. But gradually, all device makers are offering, or will soon offer, interfaces to popular, third-party CAE tools. Indeed, some newer vendors have written only a compiler for their devices, relying entirely on third-party software for design entry and simulation.

In other words, you will be able to express and simulate your design with your favorite CAE tool, be it either schematic entry or behavioral, hardware-description languages (that is, Boolean equations, truth tables, waveform entry, or state-transition tables), and then compile your design over any or all of the devices **(Ref 5)**. Therefore, why not simply call them all FPGAs? Sure, the term is more or less inapplicable to all the devices' actual guts. But the term FPGA does highlight the devices' most important functional attributes for their users: you can program them yourself (field programmable) and the devices can do the same job as gate arrays . . . well, at least the same job as smaller gate arrays.

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the operating speed of a programmed FPGA is not only one of the most important problems in this newly emerging field, it's also one of the murkiest. Internal toggle rates—another widely touted spec—make the same empty, insincere promises as equivalent gates. Users report real pain when trying to achieve even a fraction of the quoted toggle rates. However accurate any manufacturer's equivalent-gate estimates or internal flip-flop toggle rates are, the problem is that you cannot use specs in your design process.

Predictable timing is, in fact, one area where the PAL-like FPGAs have an advantage over logic-cell FPGAs. The PAL-like FPGAs' regular, precast architecture yields predictable timing. Depending on layout and routing, a logic-cell FPGA's timing for a given function can be faster or slower than that of a PAL-like FPGA. Note that the advantage extends only to predictability; achievable performance is application dependent.

The bottom line is that you're not going to be able to figure out which device to use by reading manufacturers' spec sheets—or reading articles like this one, for that matter. Instead, the best first move you can make is to take advantage of each vendor's offer to compile some test cases for you. Select some of your recent designs and let each vendor's application engineers run them through the mill for you. Then compare the results.

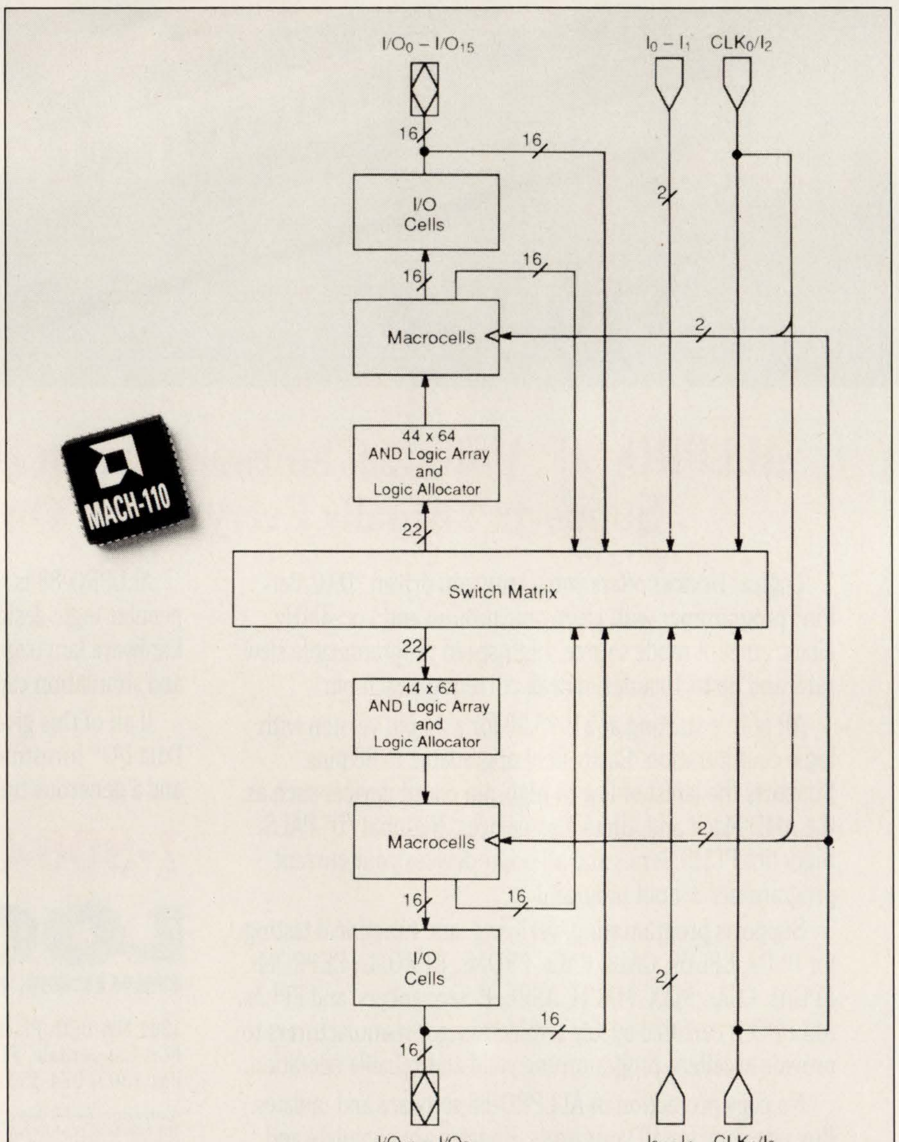
Diverting attention from engineers' primary concerns are a fog bank of secondary issues. Beyond architecture, topics you can ponder are

- In-circuit reprogramming
- Testing
- Upgrade paths to gate arrays
- Reduced-pin-count packages
- Hardware-debugging aids.

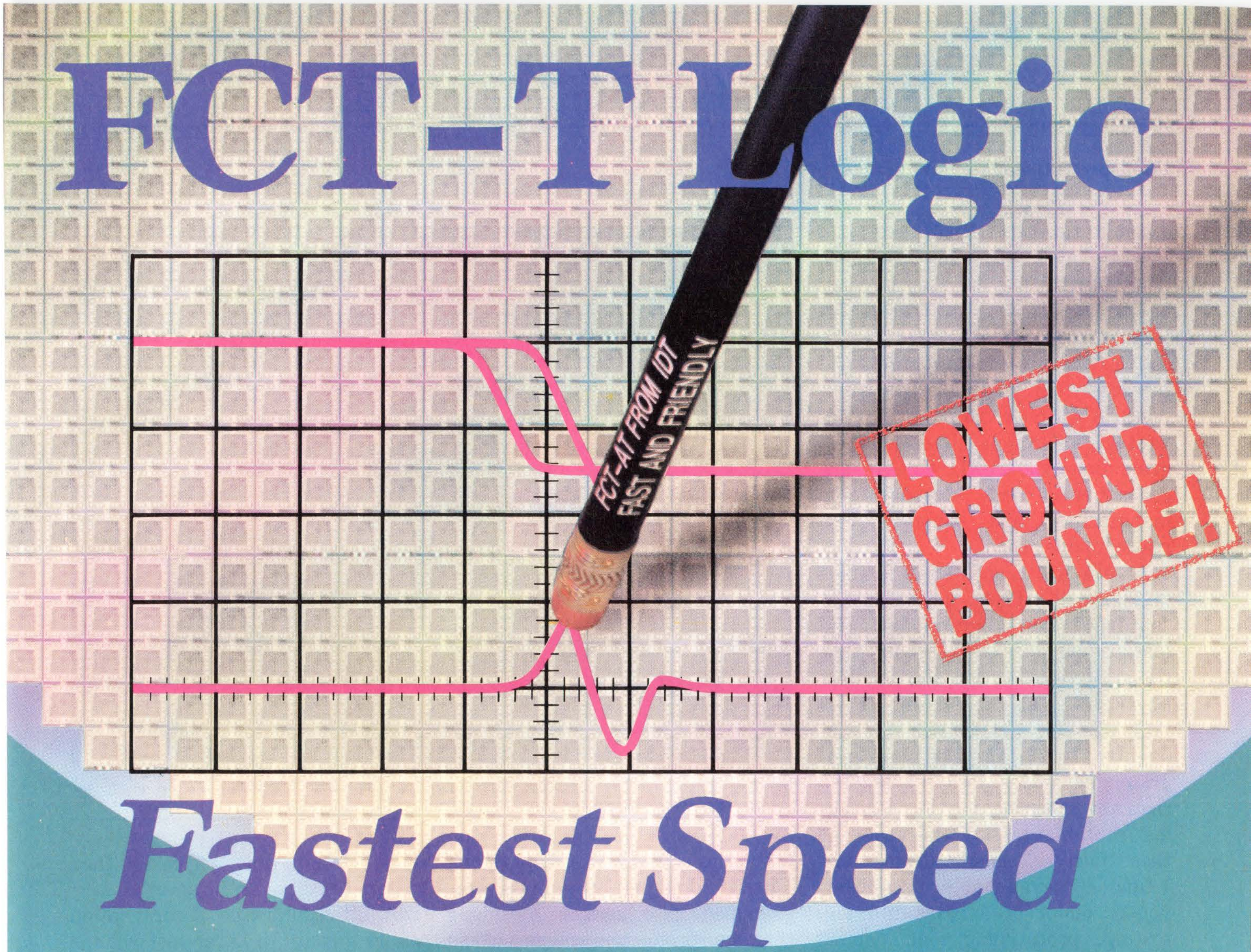
In addition to their slight architectural similarities, both Xilinx and Plessey logic-cell FPGAs use static RAMs as programming elements. The upside is that such parts are easy to subject to a suite of tests because you can program them in a variety of configurations quickly.

Further, you can reprogram them in circuit. Plessey has coined the thought-provoking term "hardware multitasking" to describe reconfiguring logic circuits on the fly. Pulling a number out of the air, some industry experts estimate that 10% of all FPGA users will employ hardware multitasking. But the question that you must ask about every new development, "Is it a feature or is it a bug?" has a flip side for hardware multitasking. If your system doesn't have off-line storage, then you'll have to add an extra ROM to hold these RAM-programmed FPGAs' programming patterns.

AMD chose electrically erasable memory cells as the programming



With combinatorial logic feeding I/O macrocells, *AMD's Mach devices reveal their PAL-device ancestry.*



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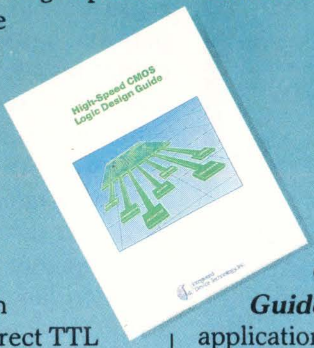

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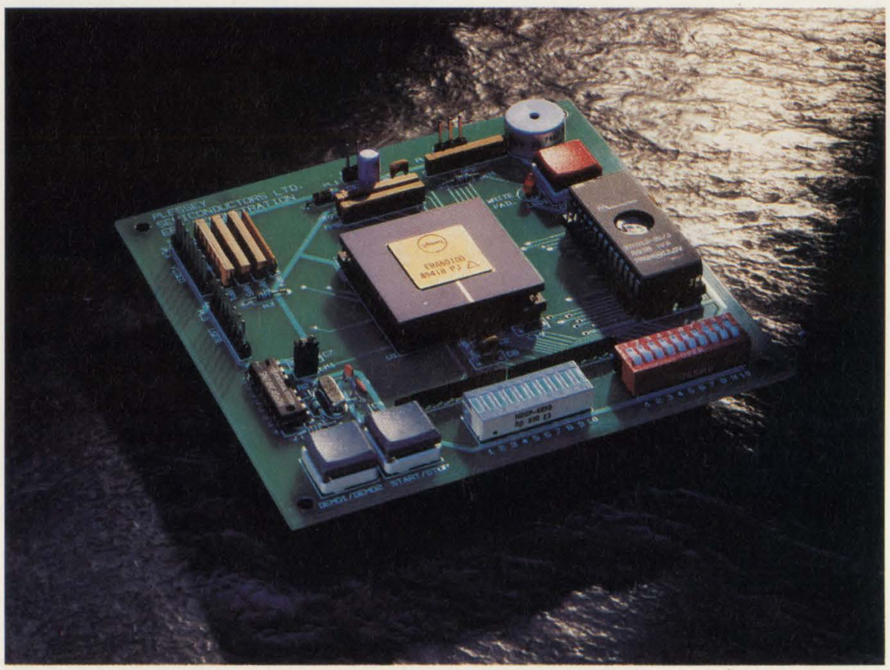
element for its Mach PAL-like FPGAs. This technology is more testable than UV-erasable technology but less easy to test than RAM-based technology. Although electrically erasable technology offers the possibility of in-circuit programming, AMD chose to punt this "advantage." Foregoing in-circuit programming, the AMD FPGAs are consequently less expensive to manufacture and consume less power in operation.

Actel's Act 1 and Act 2 families of logic-cell FPGAs use a unique "antifuse" for programming. The feature/bug dichotomy here is that the antifuse is, by far, the smallest physically of all the current FPGA programming elements. Consequently, Actel can pack more programming nodes into its FPGAs than any other maker, thus enhancing routability. But the fuses of these fairly expensive devices are 1-time programmable, requiring you to adopt profoundly different testing, prototyping, and debugging strategies than you would adopt for reprogrammable devices.

Only time will still the winds of contention that have whipped up over the question of upgrading FPGA designs to mask-programmed gate arrays. Assuming that your production volumes would justify locking an FPGA design into a gate array, no such transition will be painless because no FPGA is exactly like a gate array. Some devices' designs may be easier than others to roll over, however.

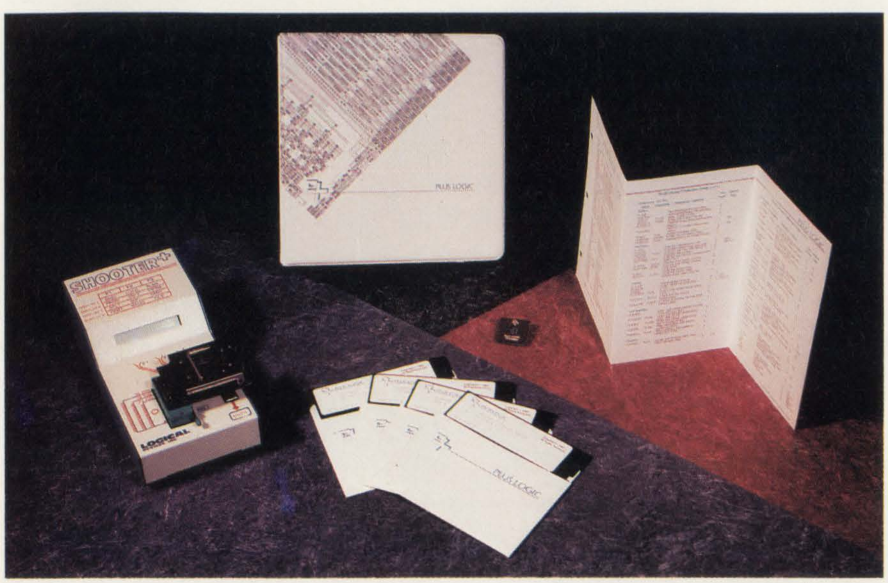


***Because of its RAM-based programming,** the Plessey Era requires a PROM if off-line storage isn't available for the chip's configuration file.*

A little-publicized Altera option offers a route to lower-cost volume production other than gate arrays: the company offers mask-programmed versions of its UV-erasable PAL-like FPGAs. If this option proves popular, expect the other FPGA vendors to follow suit.

Another minor footnote to device architecture is the emergence of reduced pin-count packages. For certain designs that use many buried registers and logic but have few inputs and outputs, makers are developing less-expensively packaged versions of their FPGAs that have a full complement of internal logic but fewer I/O pins.

Most vendors' development tools leave you designing like a PAL-device designer (using hardware-description languages) or like a gate-array designer (using schematic entry). Only Plessey and Xilinx have developed hardware-emulation tools so that you can work like a microprocessor designer. Which-



***Unlike the established FPGA vendors,** recent entrants, such as Plus Logic, rely on third-party software and programming tools.*

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CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
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TECHNOLOGY UPDATE

Field-programmable gate arrays

ever device and design methodology you eventually adopt, with FPGAs you can singlehandedly tackle bigger designs, and finish them more quickly, than you ever could before.

The June 28, 1990, edition of EDN News (pg S57) carried a series of interviews of industry managers, some of whom outlined their visions of a regimented future for design engineers. These managers envision engineers working like ants in large teams, hemmed in on every side by computer-enforced fiats while working on tiny segments of an overall design. With FPGAs in your future, your design environment need not become so Orwellian. As one experienced FPGA user put it, "With FPGAs, two guys in a garage can be their own semiconductor company." EDN

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For more information . . .

For more information on the field-programmable gate arrays discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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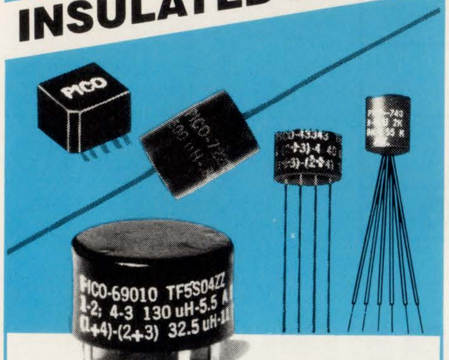


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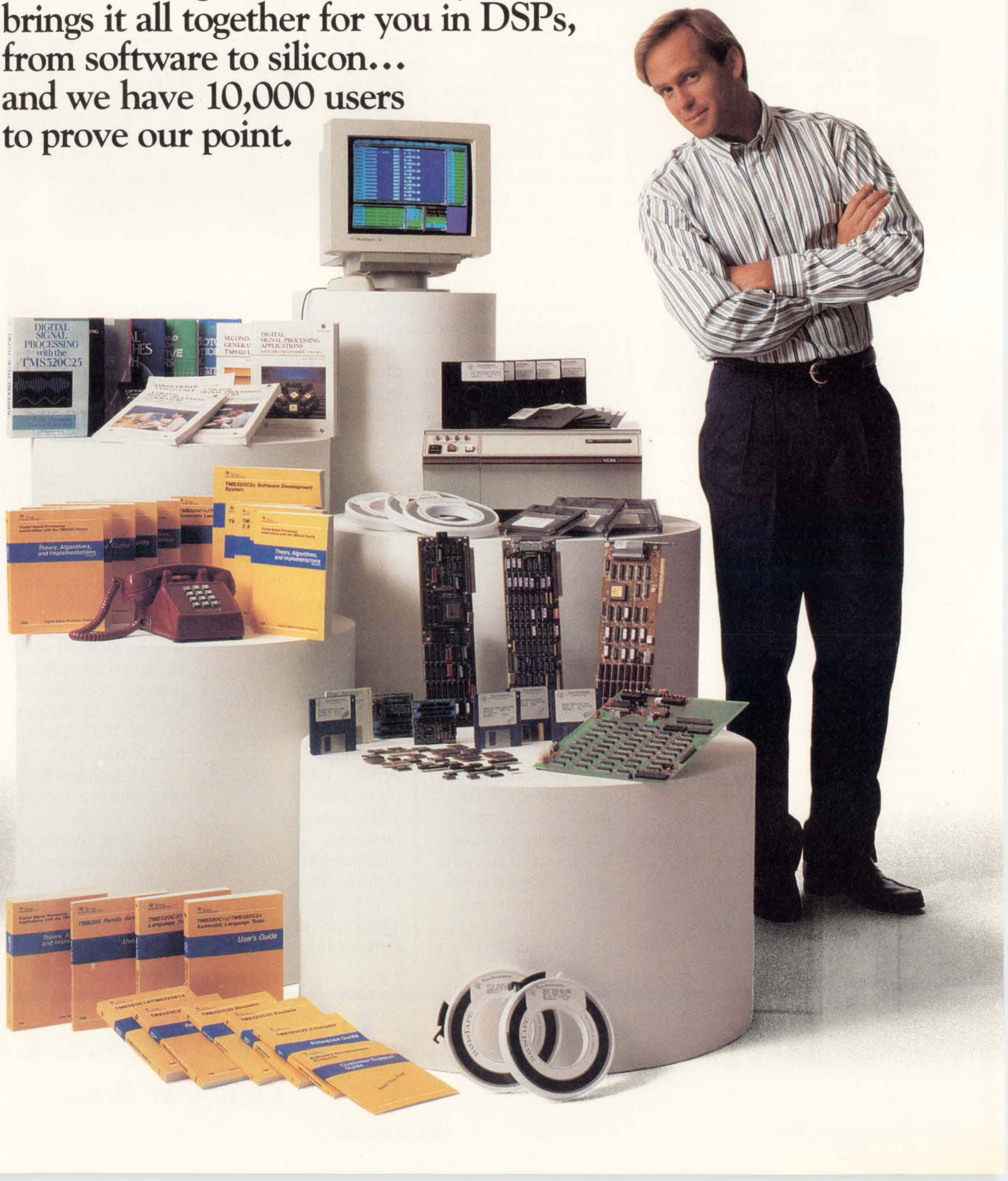

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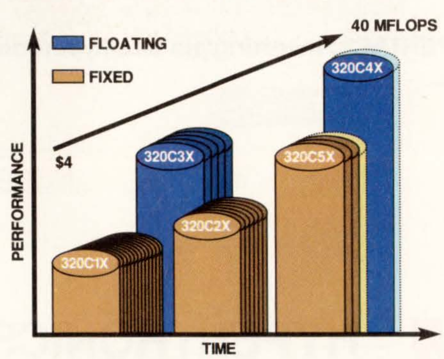

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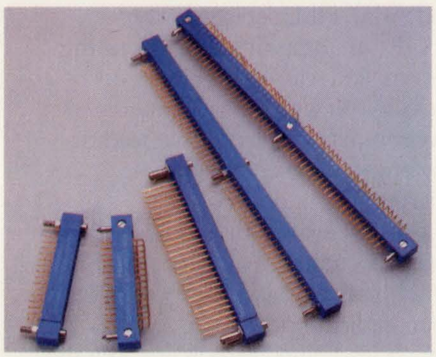

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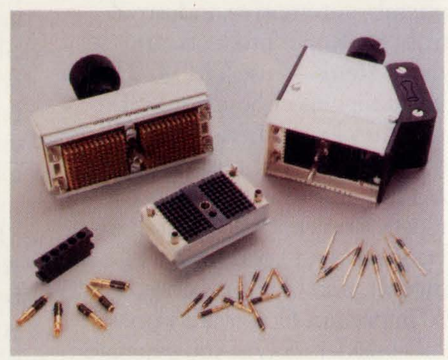

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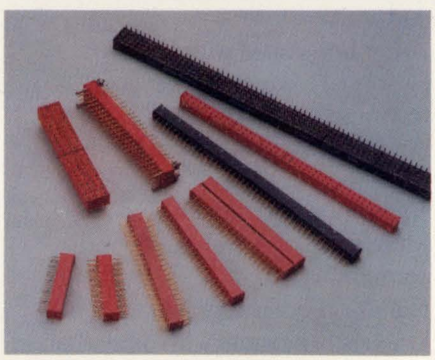

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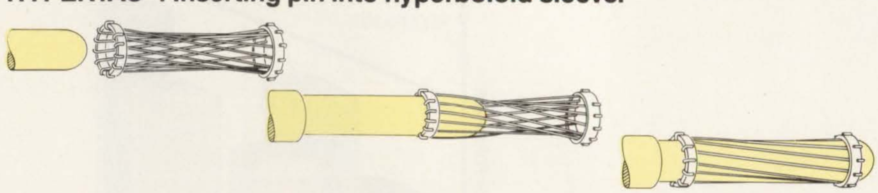

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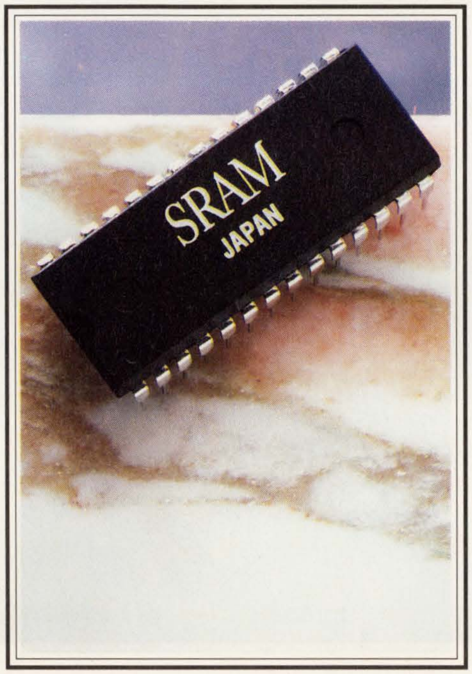

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64K	UM61165	2 x (2K x 16)	25/35/45
64K	UM6264AL	8K x 8	70/100/120
128K	UM61168	8K x 16	25/35/45
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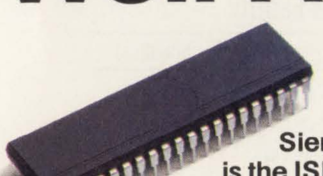

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NEWS

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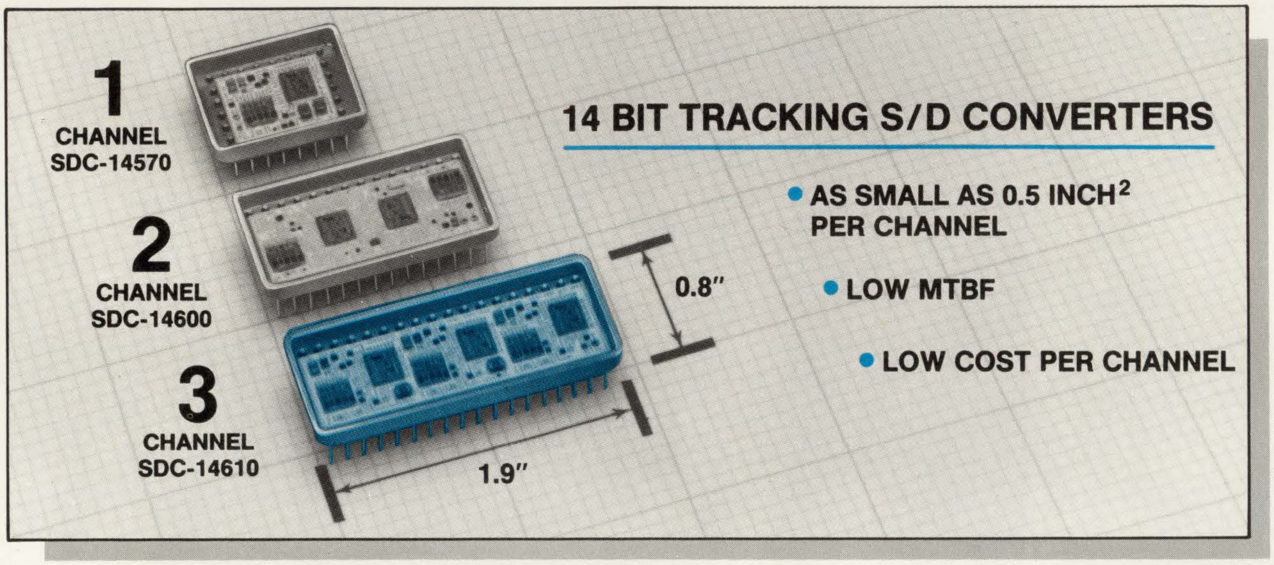

Expanding our present family of 1- and 2-channel Synchro- or Resolver-to-Digital converters, DDC introduces the 3-channel SDC-14610 Series.

Based on a custom monolithic chip design, the SDC-14610 Series offers dramatic improvements in size, MTBF, and cost per channel.

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All converters in the family use a type II servo loop for superior dynamic performance. There are no additional errors due to shaft velocity; just momentary errors caused by acceleration and deceleration.

The velocity output (VEL) is a dc voltage proportional to shaft speed that can be used to replace the tachometer. VEL output is a 4V signal referenced to ground with a linearity of 1% of output voltage.

The three channels share a common AC reference. Digital outputs are paralleled with 8 lines in two bytes, and are natural binary angle.

SDC-14610 Series converters are available with operating temperature ranges of 0° C to +70° C and –55° C to 125° C. All parameters are maintained over temperature.

Power supplies are ±5Vdc. Maximum worst case power dissipation is a low 170 mW per channel. For optimum performance capacitive bypassing should be used on power supplies.

With its low cost, small size, high accuracy, and versatile performance, the SDC-14610 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

For additional product or application information contact Bill Cullum at 516/567-5600 (1-800-DDC-1772 outside N.Y.). □

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MICROPOWER OP AMPS

Low-current devices offer high performance

Combining accuracy and good dynamic performance with low-current operation is not an easy task, but many of today's micropower op amps succeed remarkably well.

Dave Pryce,
Associate Editor

Numerous op amps on the market perform well at supply currents in the 500-μA to 1-mA range, but certain applications require devices that operate at even lower currents. For example, applications that rely on batteries or solar cells need to keep current drain to a minimum. Low-current operation is also essential for minimizing power dissipation in equipment containing large quantities of tightly packed active components.

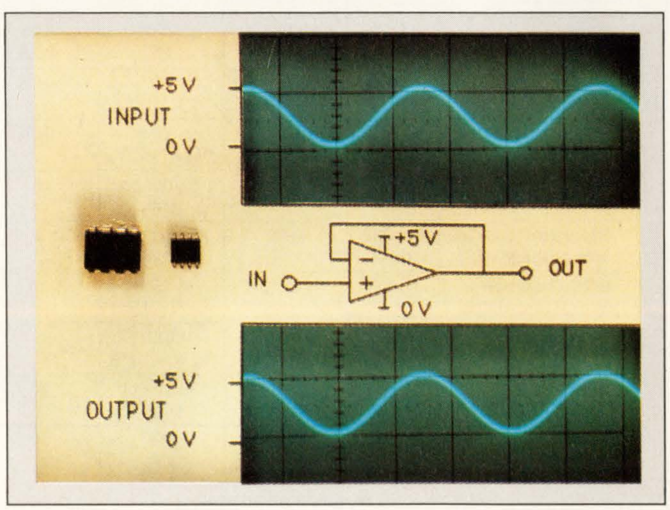
Micropower op amps can meet these needs. Though definitions of the term vary, all micropower devices perform at currents lower than the 500-μA minimum of "low-power" devices. Purists demand that for an op amp to qualify as a micropower device, it must operate with a maximum supply current of 100 μA, and preferably less. Others maintain that a device operating in the broad area between 100 and 500 μA should also qualify. Taking both viewpoints into account, this article focuses on op amps that operate at currents as high as 250 μA.

As a consequence of their low-current operation, micropower op amps are not stellar performers when it comes to exhibiting high unity-gain bandwidths or fast slew rates. With one or two exceptions, most devices—particularly those that operate at currents of less than 100 μA—have a unity-gain bandwidth in the kilohertz range rather than in the more common megahertz range. Slew rate is similarly affected; typical specifications run well under 1V/μsec.

Because of the difficulty of matching the individual characteristics of op amps' input devices at low currents, you'll also find compromises in dc specifications. For example, input offset voltages less than 500 μV, which are easily obtained in precision op amps that run at "high current," are difficult to achieve in micropower devices.

Lower your power needs further

Despite these intrinsic drawbacks, micropower op amps play a vital role in applications that demand very low power consumption. In addition to their ability to operate at low currents, sev-



For maximum dynamic range, *both the input and output of an op amp should be able to swing to the supply rails. The ALD-1706 from Advanced Linear Devices swings to within 0.1V of a ground-referenced 5V supply.*

eral devices accept low-voltage supplies, which helps alleviate the power-consumption problem. A 5V supply, for example, not only cuts down on required power, but also offers other advantages. You can run the op amp from the same supply that runs logic circuitry. Also, an op amp specified for single-supply operation has a common-mode input-voltage capability that includes ground. As a result, the op amp allows input signals to swing down to ground potential.

This swing-to-ground capability does not always extend to the output, however. Some op amps require a power-consuming pull-down resistor to achieve a 0V output. In many cases, the external load—even a light load of 1 MΩ—takes care of this problem. Often, the op amp's output *will* swing to ground, but you should check its data sheet to be sure.

Other parameters worth checking, particularly for multistage applications operating at low voltages, are an op amp's common-mode input- and output-voltage ranges. For maximum dynamic range, these ranges should come as close as possible to the supply-rail voltages.

The voltage ranges of the ALD-1706 from Advanced Linear Devices come very close to the supply-rail voltages. Operating from a ±2.5V supply, for example, the CMOS device has an output-voltage range that usually comes within 0.1V of each supply rail. The op amp typically needs only 20 μA of supply current and can operate from dual supplies of ±1 to ±6V or a single supply of 2 to 12V.

The device offers a respectable 400-kHz unity-gain bandwidth in spite of its very low operating current. Other characteristics include a 0.17V/μsec slew rate, a settling time of 10 μsec to 0.1%, and a large-signal voltage gain of 100,000. Dual and quad versions (ALD-2706 and ALD-4706, respectively) are also available.

Bandwidth and slew rate

At the opposite extreme in terms of supply-current requirements are the AD548 and AD648 (dual) from Analog Devices, and the OP-282 (dual) and OP-482 (quad) from Precision Monolithics. These devices operate at supply currents in the 200- to 250-μA range, which barely lets them qualify as micropower devices. However, their relatively high operating currents produce dynamic characteristics that are quite impressive.

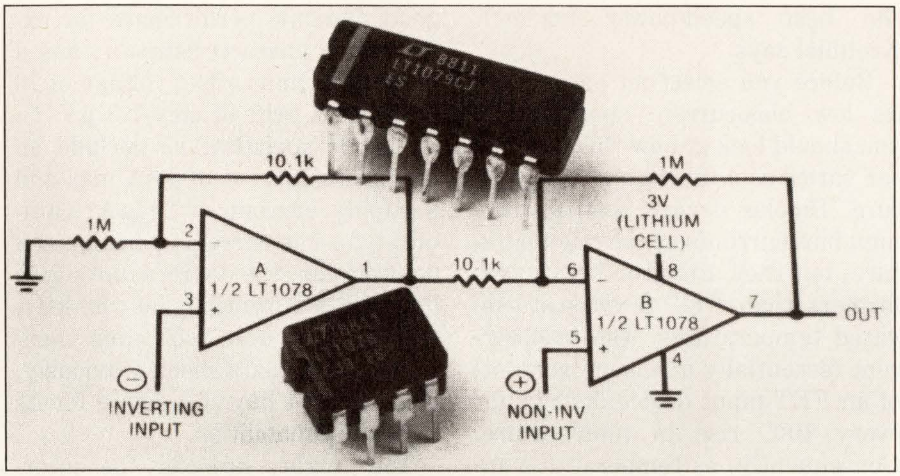
Table 1—Representative micropower op amps

Manufacturer	Type number	Supply voltage (V)	Supply current (μA)[1]	Input offset voltage (mV)[1]	Input bias current (nA)[1]	Input offset current (nA)[1]	Common-mode input-voltage range (V)	Output-voltage range (V)
Advanced Linear Devices	ALD-1706	±1 to ±6 2 to 12	40	4.5	0.03	0.025	$+V_S$ to $-V_S$	Within 0.2V of $\pm V_S$
Analog Devices	AD548	±4.5 to ±18	200	2	0.02	0.01	±11 at V_S = ±15V	±12 at V_S = ±15V
Harris Semiconductor	HA7711 HA7712	±2 to ±8 ±2 to ±8	200 25	0.25 0.25	0.02 0.02	0.01 0.01	−5 to +3.8 (V_S = ±5)	Within 0.1V of $\pm V_S$
Linear Technology	LT1077	5	60	0.06	11	0.45	0 to 3.5	0.006 to 4.2
Maxim Integrated Products	Max480	±0.8 to ±18 1.6 to 36	20 (V_S = ±15V)	0.07	3	1	−15 to +13.5 (V_S = ±15V)	±14 (V_S = ±15V)
National Semiconductor	LPC662 (dual)	5 to 15	70 (per op amp)	6	0.020	0.020	0 to 2.7 (V_S = 5V)	0.06 to 4.94 (V_S = 5V)
Precision Monolithics	OP-282 (dual)	±15	250 (per op amp)	2	0.1	0.05	+13 to −11	±13
SGS-Thomson Microelectronics	TS-271	4 to 10	15	10	0.15	0.1	—	0.05 to 8.8 (V_S = 10V)
Signetics	NE5230	±0.9 to ±7.5 1.8 to 15	160 (V_S = ±0.9V)	3	60	30	$+V_S$ to $-V_S$	+7.25 to −7.3 (V_S = ±7.5)
Siliconix	L144 (triple)	±1.5 to ±15	133 (per op amp)	10	250	70	—	±10 (V_S = ±15)
Texas Instruments	TL251C	1.4 to 16	20	10	0.6	0.3	−0.2 to 9 (V_S = 10V)	0 to 8 (V_S = 10V)

Notes: 1. Values shown are maximum.
2. Prices shown are for lowest cost device.

Analog's AD548 and AD648 have unity-gain bandwidths of 1 MHz and slew rates of 1.8V/μsec. Operating at 200 μA, these devices also feature respectable dc characteristics. Worst-case maximum values include an input offset voltage of 2 mV, and input bias and input offset currents of only 20 pA and 10 pA, respectively.

Operating at a somewhat higher current of 250 μA, the OP-282 and OP-482 from Precision Monolithics have even better dynamic characteristics. The devices feature unity-gain bandwidths of 4 MHz, slew rates of 9V/μsec, and settling times of 1.5 μsec to 0.01%. This level of performance puts the 282/482 head and shoulders above most other micropower op amps and on par with many amplifiers that operate at supply currents in the milliampere range.



Op amps are available in single, dual, triple, and quad versions. *These 8- and 14-pin devices from Linear Technology are dual and quad op amps, respectively.*

Another micropower device that exhibits better-than-average performance in at least one parameter is the HA7711 from Harris Semiconductor. With a supply current of 250 μA max, the device features an offset voltage of only 250 μV max. A companion device, the HA7712, operates at only 25 μA and has the same offset voltage.

Typical gain×bandwidth (kHz)	Typical slew rate (V/μsec)	Package types	Price (quantity)²	Comments
400	0.17	DIP-8, S0-8	$0.89 (10,000)	Dual and quad versions also available
1000	1.8	DIP-8, TO-99	$0.75 (100)	Dual version is AD648
800 100	0.45 0.04	DIP-8, SO-8	$1.25 (100)	
230	0.08	DIP-8, SO-8	$1.65 (100)	Also characterized for ±15V operation
20	—	DIP-8, SO-8	$3.95 (1000)	
350	0.11	DIP-8, SO-8	$1.30 (1000)	Quad version is LPC660
4000	9	DIP-8, SO-8	$1.50 (100)	Quad version is OP-482
100	0.04	DIP-8, SO-8	$0.46 (1000)	Supply current is programmable
250	0.09	DIP-8, SO-8	$0.92 (100)	Supply current is programmable
600	0.4	DIP-14, FP-14	$6.94 (100)	Supply current is programmable
100	0.04	DIP-8	$0.79 (1000)	Supply current is programmable

The principal difference between the two devices lies in their dynamic characteristics. The HA7711 has a unity-gain bandwidth of 800 kHz and a slew rate of 0.45V/μsec. On the other hand, as a result of its much lower operating current, the HA7712 has a bandwidth of only 100 kHz and a slew rate of 0.04V/μsec. This tradeoff of dynamic performance for operating current is important to consider when choosing the best micropower op amp for your application.

Lowering the bias current

Other tradeoffs must be weighed when selecting a micropower op amp. John Krehbiel, a marketing manager for Harris Semiconductor, points out that bipolar op amps are sometimes applications-limited because of their high input bias current. In contrast, CMOS-input devices can have bias currents 1000 times lower than those of bipolar-input devices—an important feature for minimizing total system current. However, a *complementary* bipolar process often provides the best speed/power tradeoff, Krehbiel says.

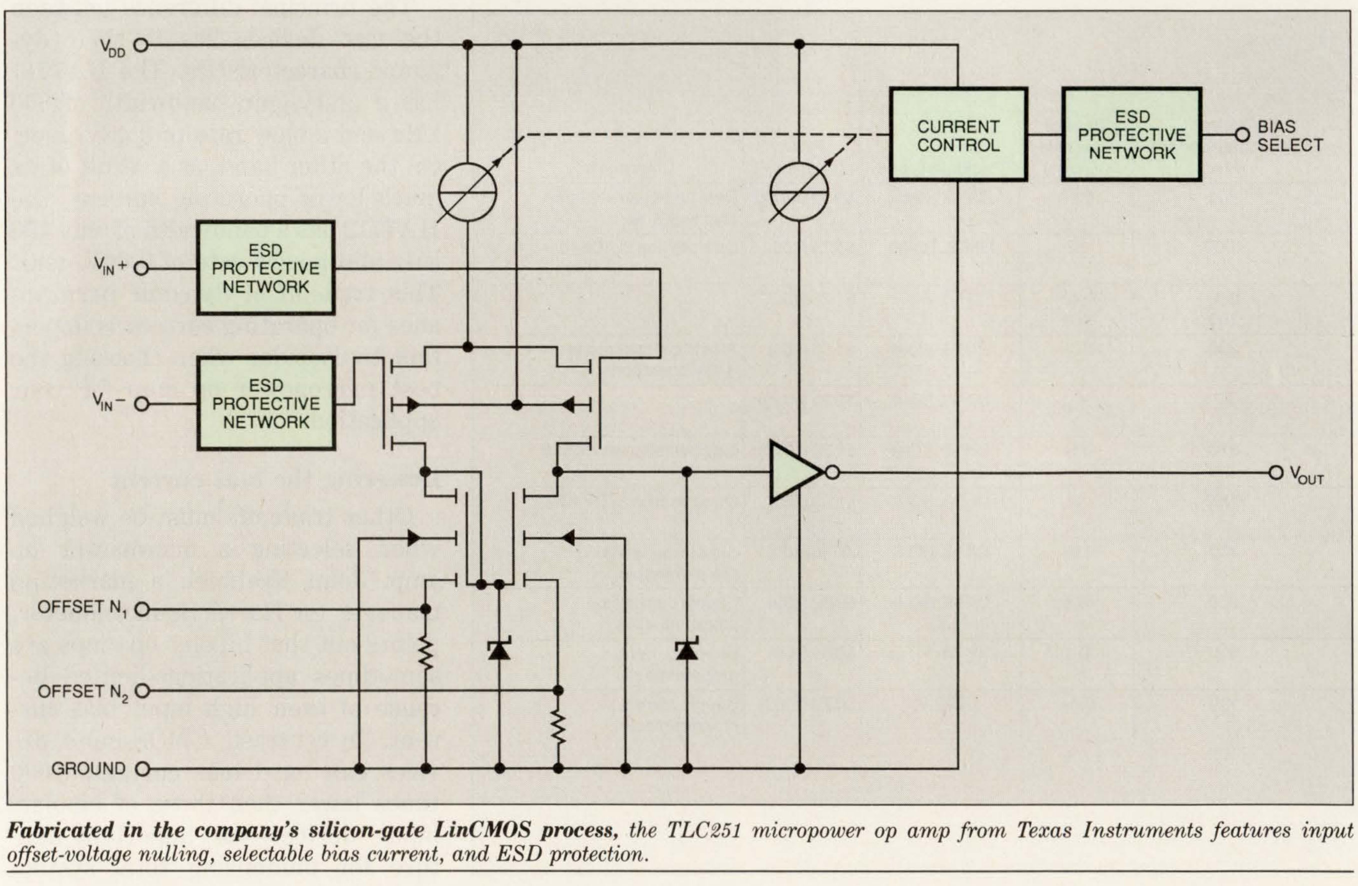
Before you select an op amp for its low bias-current specification, you should look at how this parameter varies as a function of temperature. Bipolar devices tend to have high bias currents at room temperature, but they are often better performers than FET devices at elevated temperatures. The bias current (essentially a leakage current) of an FET-input device doubles for every 10°C rise in temperature. Consequently, as temperatures approach 100°C, the bias current of an FET-input op amp can be greater than that of a bipolar-input device. This behavior should be a prime consideration in choosing op amps for applications that operate at temperatures above 85°C.

Another tradeoff is apparent in the Max480 from Maxim Integrated Products; the op amp sacrifices good dynamic performance for excellent dc characteristics. It has a maximum input offset voltage of 70 μV with a drift of only 1.5 μV/°C. Other dc specifications include an input bias current of 3 nA max and a supply current of 20 μA. Optimized for low-current operation and dc precision, the device's unity-gain bandwidth is typically only 20 kHz, and its slew rate isn't even mentioned in the data sheet. Obviously, you wouldn't buy this device for its dynamic capabilities.

You might, however, be interested in the Max480 for such applications as voltage references, remote thermocouple conditioners, and current monitors. You can operate the device from a single supply of 1.6 to 36V or from dual supplies of ±0.8 to ±18V. The op amp is particularly useful in battery-powered applications. For example, the device's 15-μA maximum supply current from a 3V supply allows more than 16,000 hours of operation from a 250-mA/hour lithium cell.

Another device that offers excellent dc performance is the LT1077 from Linear Technology. Because it operates at a higher supply current of 60 μA, the device's dynamic performance doesn't suffer quite as much as that of the Max480. It offers a reasonably high unity-gain bandwidth of 230 kHz and a slew rate that, at 0.08V/μsec, is at least measurable.

The op amp's real claims to fame, however, are its dc precision and its output-drive capabilities. Operating with a single 5V supply, the op amp's lowest grade version features a maximum input offset voltage of only 60 μV and an input offset current of less than 0.45 nA. The device's common-mode input-



Fabricated in the company's silicon-gate LinCMOS process, *the TLC251 micropower op amp from Texas Instruments features input offset-voltage nulling, selectable bias current, and ESD protection.*

voltage range extends from 0 to 3.5V, and its output voltage extends from 6 mV above ground to 4.2V. In addition to its 5V characterization, the op amp comes with a full set of specifications for ±15V operation. It is available in single, dual (LT1078), and quad (LT1079) versions.

Table 1 shows the basic characteristics of several micropower op amps. This brief listing does not do justice to the large numbers of available products. In particular, companies such as Linear Technology, National Semiconductor, Precision Monolithics, and Texas Instruments offer a wide range of micropower devices.

Many of the op amps in the table are also available in dual and quad versions. In addition, several of the devices have a programmable feature that lets you adjust the supply current over a range of operating points. By adjusting the supply current to a value higher than that shown in the table, you can usually enhance the device's unity-gain bandwidth and/or slew rate. Be careful not to set the current so high that it exceeds the value your application can accept.

Micropower op amps are certainly not a panacea for every application. Their low-power operation and improved dc specifications are generally offset by weaker dynamic characteristics. But if 200 to 250 μA of supply current fall under your definition of micropower, a couple of devices are available that break the 1-MHz gain-bandwidth and 1V/μsec slew-rate barriers. Despite inherent tradeoffs, micropower op amps are the best game in town for current-sensitive applications.

EDN

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For more information . . .

For more information on the micropower op amps discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Melbourne, FL 32902
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Linear Technology Corp
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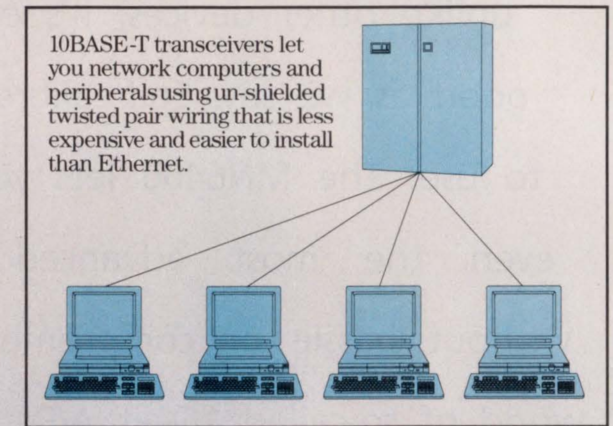

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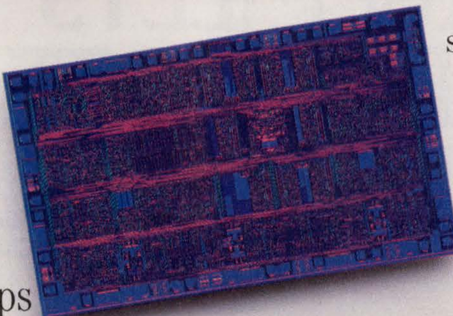

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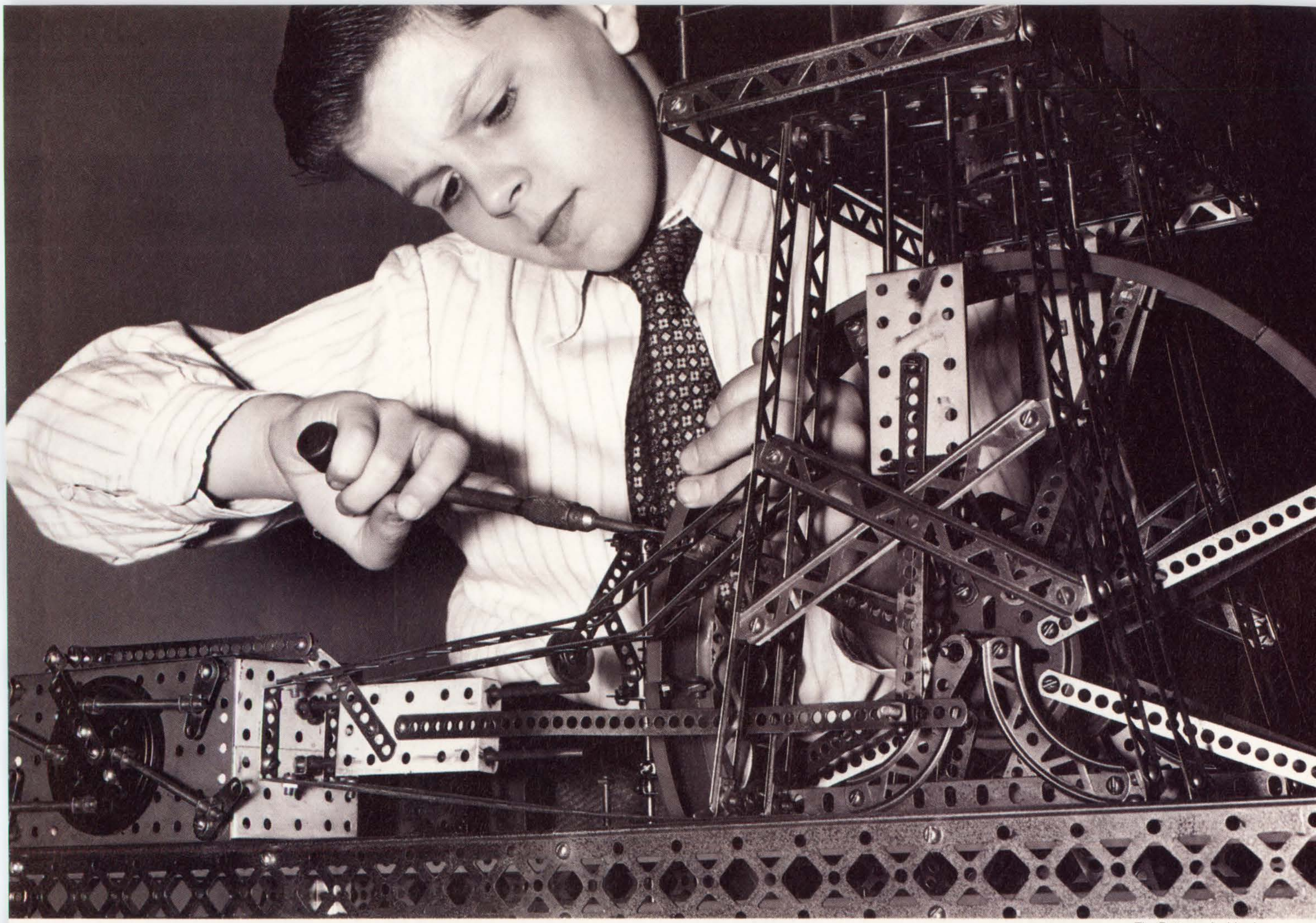

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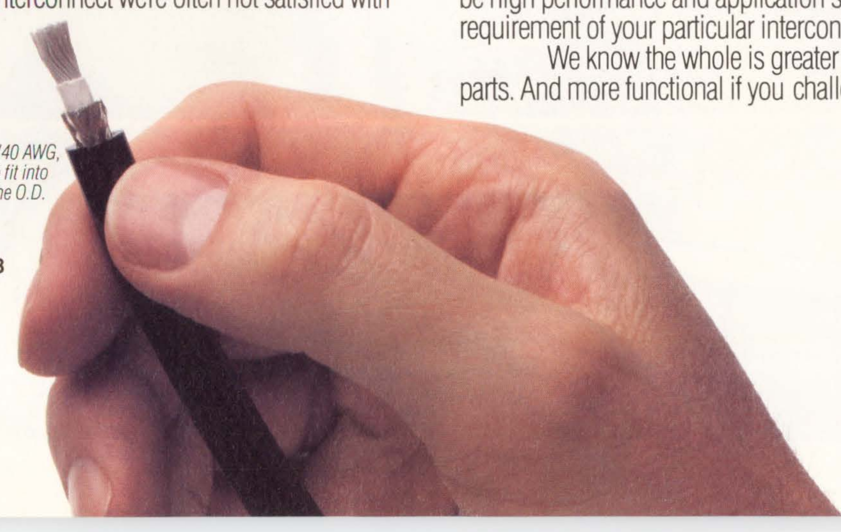

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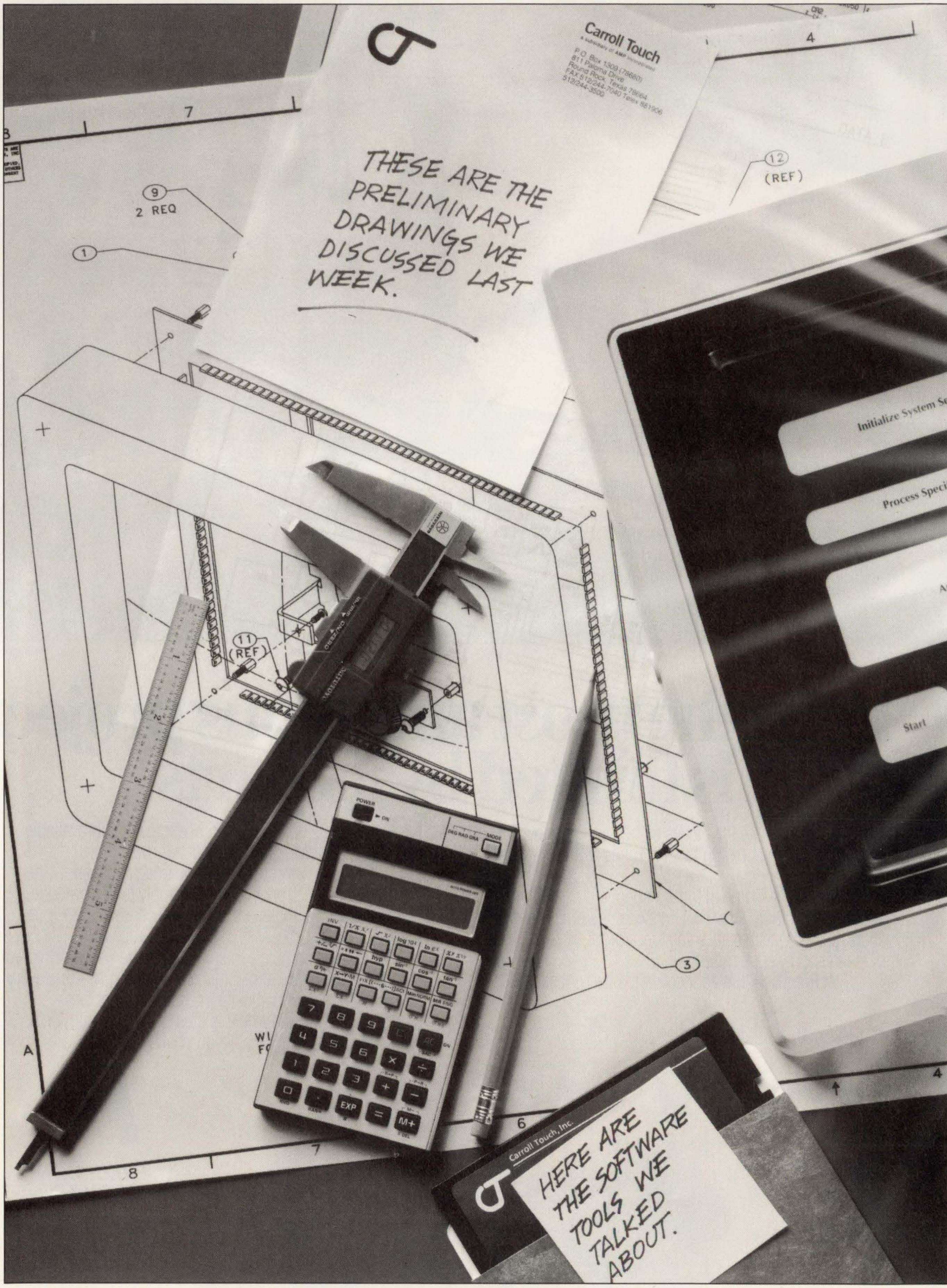

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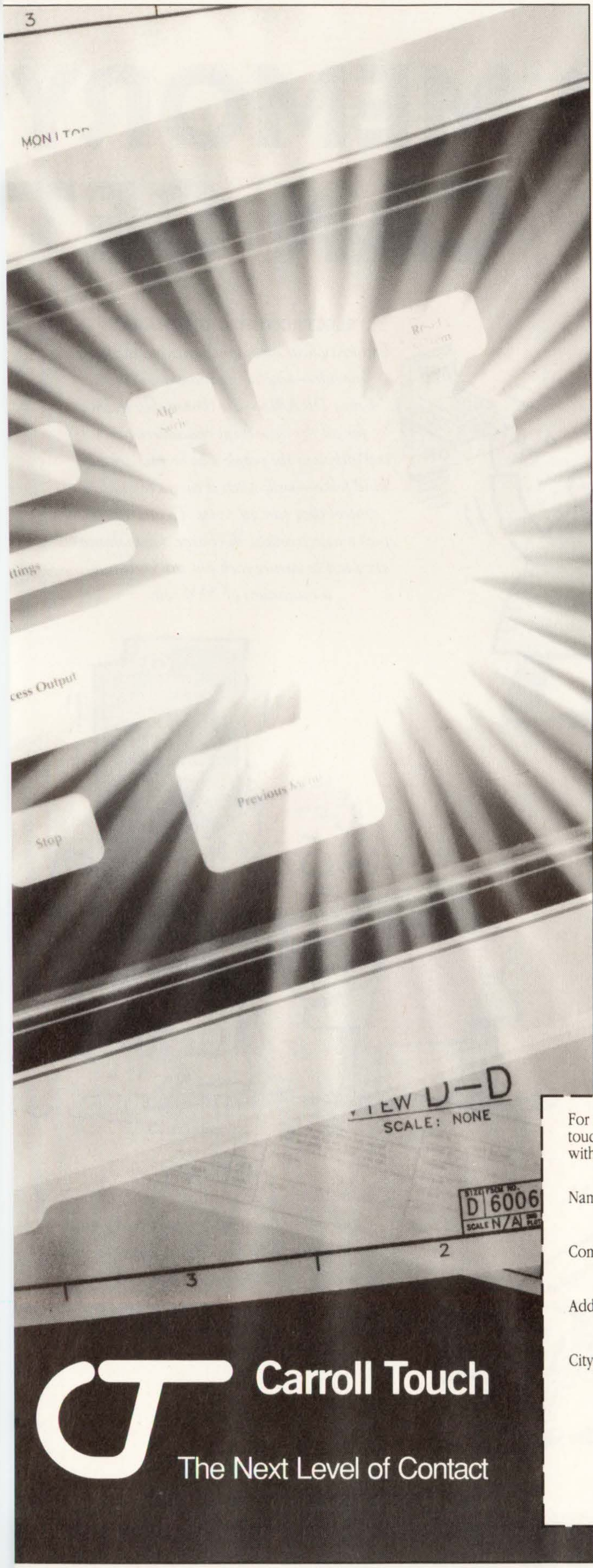

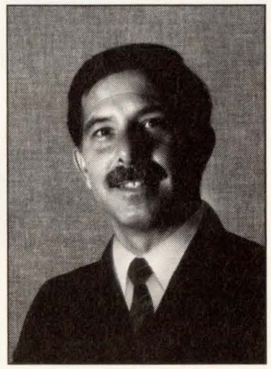

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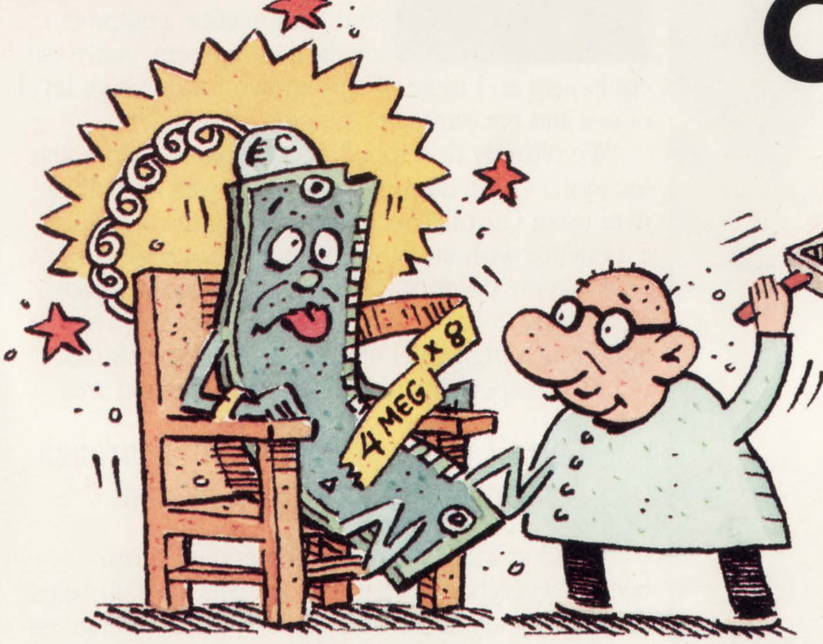

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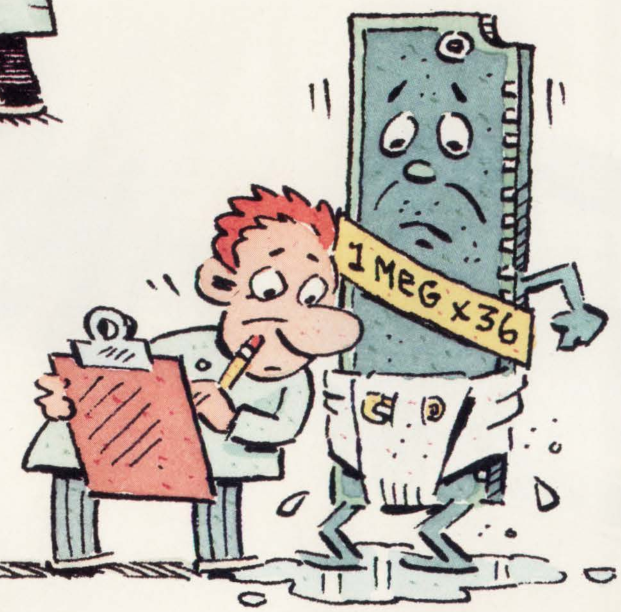

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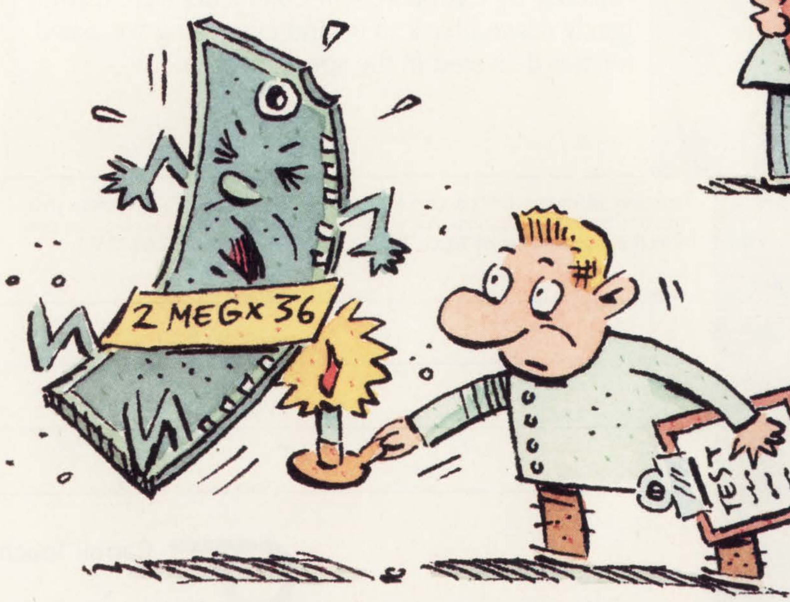

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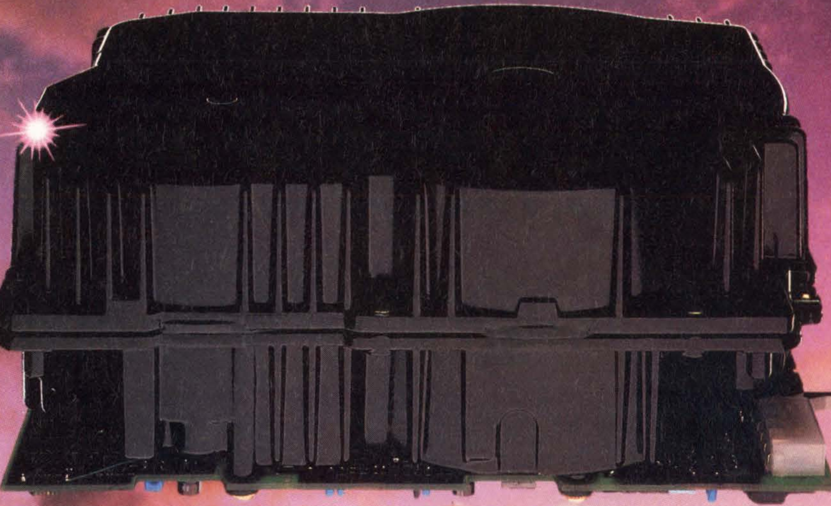

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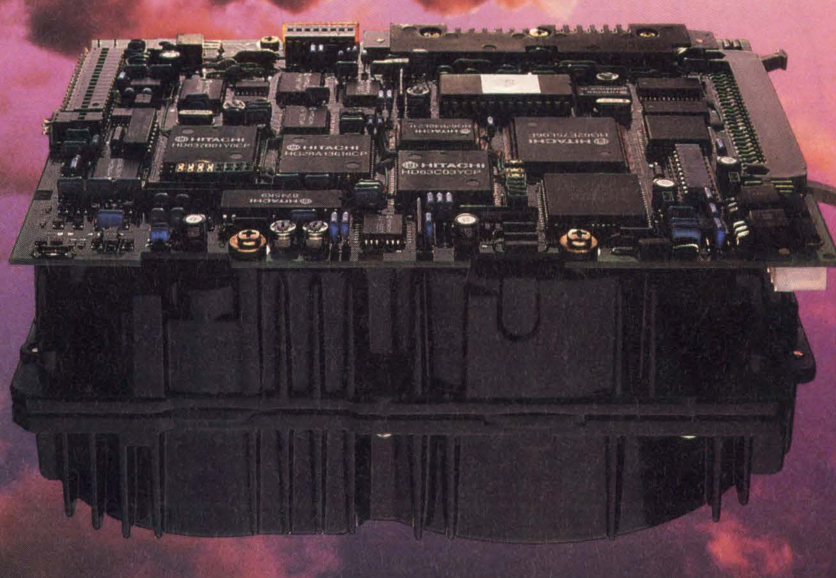

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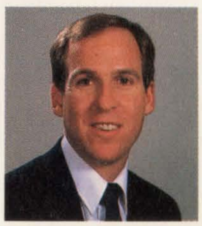
Logic-synthesis tools speed ASIC designs



Logic-synthesis tools for ASIC design help you save time while meeting your functional, area, and performance design goals.

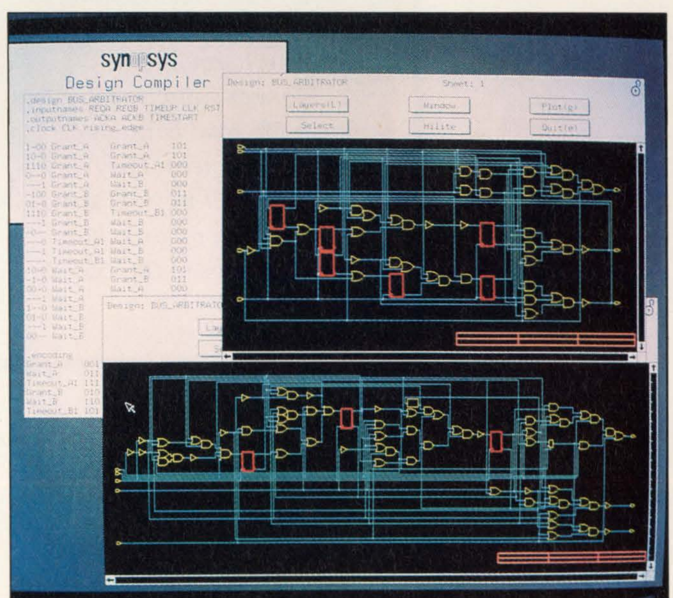
Doug Conner,
Regional Editor

Designing a 100,000-gate ASIC is a big job and usually needs to be done quickly. If a team of designers can generate 2000 gates a week, they've still got a 1-year effort ahead. Even a modest 15,000-gate ASIC is a large undertaking—especially if one engineer is going to design it. Rather than working unreasonable hours to meet impossible deadlines, you can use logic-synthesis tools to automate some of the design process and reduce your design time.

To use logic-synthesis tools, input an ASIC design description and design constraints that describe your design goals (**Fig 1**). The tool produces a net list, a design report detailing general information about your design, and other types of information, depending on the particular tool.

Besides synthesizing your ASIC design, these tools also optimize designs, usually for speed, area, or both. Optimization works best on control logic, including random logic and state machines. Control logic might be 20% of an ASIC's design, yet it can consume more than that percentage of your design time. Highly structured designs such as RAMs and ROMs aren't good candidates for optimization.

Another benefit of logic-synthesis tools is that they let you synthesize designs from a high-level description. Hardware description languages (HDLs) such as VHDL (VHSIC hardware description language) and Verilog from Cadence (San Jose, CA) let you describe circuits at a level higher than that of a gate-level description. Using an HDL, you can describe an ASIC in terms of the functions it performs or the behavior you expect from the device. The higher-level description lets you avoid implementation details and concentrate on what you want the circuit to do. By using an HDL as an input to the logic synthesizer, you also avoid having to describe a design twice: once



Extracting a state table from a net list *(upper left corner) is one of many input methods you can use with Synopsys's Design Compiler. The tool optimizes the state assignment and then synthesizes the logic necessary to implement it. The top schematic shows the 6-state machine optimized for speed with six flip-flops; the bottom schematic shows an area-efficient design using three flip-flops.*

at the behavioral level before simulation and then again at the schematic level.

However, the ability of HDLs to model unsynthesizable characteristics such as user-defined data types limits logic-synthesis tools to working with a subset of HDLs. What constitutes a synthesizable subset varies among logic-synthesis tools.

Some logic-synthesis tools let you use a variety of input formats in the same design, so you can use the format that is best for the particular part of a circuit you're working on. Designers can use Boolean equations, truth tables, and state machines at different times when developing design descriptions. You'll save time and avoid errors if you use your original design description format as the input for your logic-synthesis tool. You may need to run the logic-synthesis tool before simulation if you've chosen a combination of design input formats that your simulator won't accept. Logic-synthesis tools can synthesize your design into a format that is compatible with your simulator.

Other benefits of logic-synthesis tools include the fact that you won't need to become intimately familiar with a particular ASIC foundry's logic library because you can just feed that information to the tool. The tool takes care of translating your logic to make the best use of the foundry's library. Some logic-synthesis tools add test structures to the synthesized design; some products can also automatically generate test vectors.

Defining a design

Developing an ASIC with logic-synthesis tools differs somewhat among the various tools. **Fig 2** shows the general steps for developing an ASIC using a logic-synthesis tool. The first step is developing a design description and then functionally simulating it to verify that your design performs the way you want it to. Next, transfer the design to the logic-synthesis tool. You can use any combination of input formats that are acceptable to the synthesis software, such as EDIF (Electronic Design Interchange Format), VHDL, or proprietary schematic and net-list formats. **Table 1** shows the input formats typically acceptable to logic-synthesis tools.

Although some logic-synthesis tools work from the structural descriptions that HDLs provide, other tools can work from structural or behavioral ASIC descriptions. In the description hierarchy, behavioral descriptions are the most abstract, structural descriptions such as register-transfer-level (RTL) descriptions are more concrete, and gate-level descriptions are the most concrete. The more abstract your design description, the further you are from the details of implementation. A more abstract (as opposed to concrete) design is easier for de-

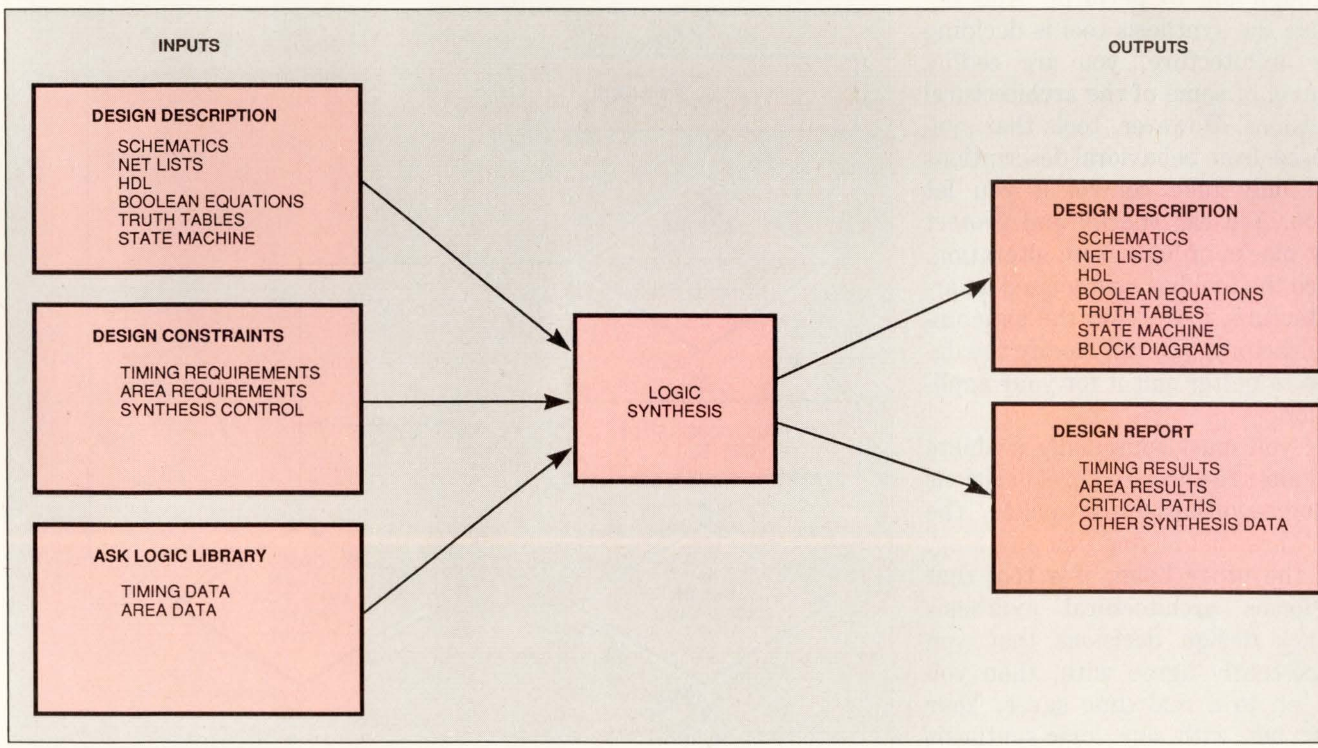


***Fig 1—Logic-synthesis tools typically require** a variety of input information to optimize and synthesize a design. The tools output a design description that includes a net list; other formats may also be available.*

signers to create because they don't have to worry about details. Such a design is more difficult for a logic-synthesis tool to create because it does have to sweat the details.

Logic synthesis is more controlled when working from a structural ASIC description than it is given a behavioral description. An RTL description already has an implied architecture; a behavioral description does not imply a structure. You might think of logic synthesis from an RTL description as optimizing the combinatorial logic between registers. As your descriptions become more behavioral, they imply less of the architecture. Synthesis at the behavioral level is sometimes referred to as architectural synthesis, which is a subset of logic synthesis. Tools that can work at higher behavioral levels synthesize an architecture then perform logic synthesis on that architecture.

Tools that synthesize designs from behavioral descriptions have a tough job to perform. And because the synthesis tool is deciding the architecture, you are ceding control of some of the architectural decisions. However, tools that synthesize from behavioral descriptions will only take control if you let them. You can specify and protect any blocks of logic from alteration. Once the tool has synthesized an architecture, if you find the logic unsatisfactory, you can modify the design to better suit it for your application.

If you must continually evaluate and alter the architectural decisions a logic-synthesis tool makes, the software isn't saving you anything. On the other hand, if a tool that performs architectural synthesis makes design decisions that you consistently agree with, then you are on to a real time saver. Your best bet with any logic-synthesis tool—especially those that perform architectural synthesis—is to benchmark the tools on designs or portions of designs that represent your typical work.

With most synthesis tools, you'll elect to partition your design into blocks. Hierarchical blocks are a common way to rough out a design. Work from the top down, specifying the function of each block. Without synthesis tools, you'd proceed to detailed design of what goes into each block, and logic synthesis lets you take much the same approach. Logic synthesis can support a design method that is similar to what many designers use without these tools.

Synopsys says that many users of its logic-synthesis tool work with blocks that represent 300 to 5000

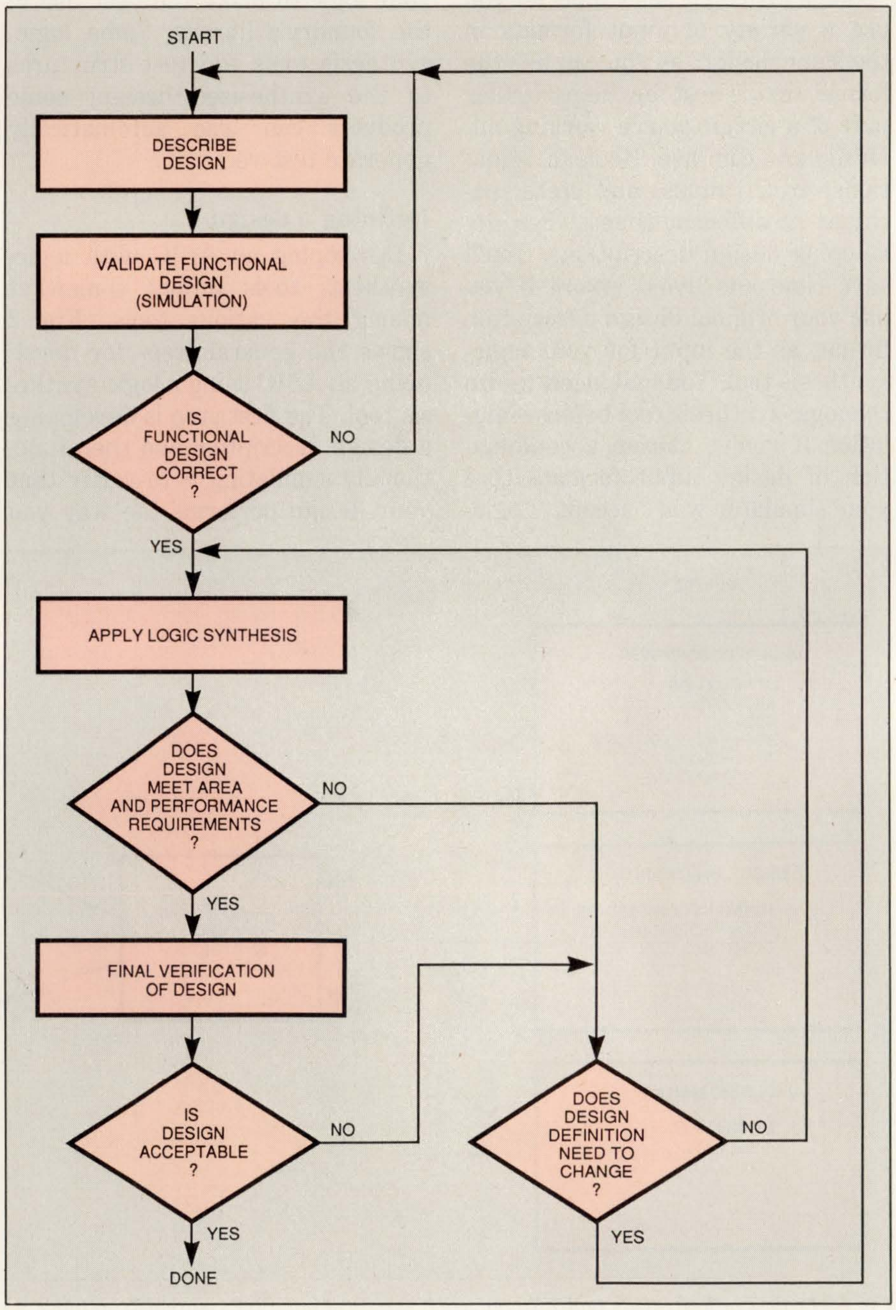


Fig 2—Designing an ASIC using logic synthesis *starts with describing the design.*

Logic-synthesis tools

gates. Synopsys's Design Compiler can accommodate larger designs, but users find the 300- to 5000-gate size convenient for several reasons. Blocks of less than 5000 gates usually cover a well-defined part of a design. During the development phase, the synthesis and simulation cycles will be shorter than they would be with larger design blocks. Finally, by keeping blocks small, you can explore other design configurations by simply rearranging blocks.

Partitioning a design into small blocks can cause a number of problems, however. Partitions that make sense for logical development may not be optimum for synthesizing a fast, area-saving design. You may end up moving block boundaries around to help the synthesis tool create the optimum design. SilcSyn from Racal-Redac lets you organize your design into blocks and then designate boundaries around the blocks as permeable or impermeable. With these boundaries, you maintain a logically organized design while allowing the synthesis software to cross the permeable boundaries during optimization.

Tools such as the ASIC Synthesizer from VLSI Technology work on the entire design at once. It performs automatic partitioning as part of architectural synthesis.

In addition to providing your design description to the synthesis tool, you need to enter design constraints. These constraints provide the software with guidelines for performing area-speed tradeoff analysis. For example, you can provide minimum and maximum signal-arrival-time bounds on inputs, a clock profile for synchronous designs, output-port loading, input-port drive, setup and hold times, maximum allowable area, and keep-out zones—networks or cells you don't want the logic synthesizer to alter.

Logic-synthesis tools can work with synchronous and asynchronous designs. The timing-sensitive nature of asynchronous designs re-

Table 1—Representative logic-synthesis tools

		Design input formats*								Design output formats*								Optimization parameters					
Manufacturer	Product	Net lists	Schematics	Boolean equations	PLA truth tables	State machine	VHDL	Verilog	Proprietary HDL	Net list	Schematic	Boolean equations	PLA truth tables	State machine	VHDL	Verilog	Proprietary HDL	Speed	Area	Power	User programmable	Price	Notes
Dassault Electronique	Frenchip	✓					✓			✓								✓	✓			$75,000 to $100,000	Available first quarter 1991; test synthesis.
LSI Logic	LES	✓	✓	✓	✓	✓	O		✓	✓	✓				O	O	✓	✓	✓			$30,000 to $90,000	Includes memory, data-path optimizers; test synthesis optional.
Mentor Graphics	Autologic	✓	✓	✓	✓	✓			✓	✓	✓							✓	✓		✓	$35,000 to $45,000	Accepts parameterized logic blocks.
	Design Consultant						✓			✓	✓							✓	✓			$22,000 to $28,000	Available fourth quarter, 1990.
	ASIC Consultant	✓	✓	✓	✓	✓	O		✓	✓	✓							✓	✓		✓	$33,000 to $41,000	Available fourth quarter, 1990; accept parameterized logic blocks.
Racal-Redac	SilcSyn 2.0	✓	✓	✓	✓				✓	✓	✓							✓	✓			$50,000 to $70,000	VHDL input available fourth quarter, 1990; test synthesis options.
Seattle Silicon	Finesse	✓		✓	✓				✓	✓								✓	✓			$59,000	Price is for complete Chip Crafters ASIC design package. Outputs a silicon layout; includes test synthesis.
Synopsys	Design Compiler	✓	✓	✓	✓	✓	O	O		✓	✓	✓	✓	✓	✓	O	O	✓	✓			$35,000 to $100,000	HDL compiler optional; test synthesis optional.
	ECL Compiler	✓	✓	✓	✓	✓	O	O		✓	✓	✓	✓	✓	✓	O	O	✓	✓	✓		$35,000 to $100,000	HDL compiler optional; test synthesis optional.
Viewlogic	VHDL Designer		✓				✓			✓	O				✓			✓	✓			$15,000 to $20,000	Viewgen option for schematic-output generation.
VLSI Technology	ASIC Synthesizer						✓	✓		✓	✓							✓	✓			$100,000	Outputs silicon layout; test synthesis optional.

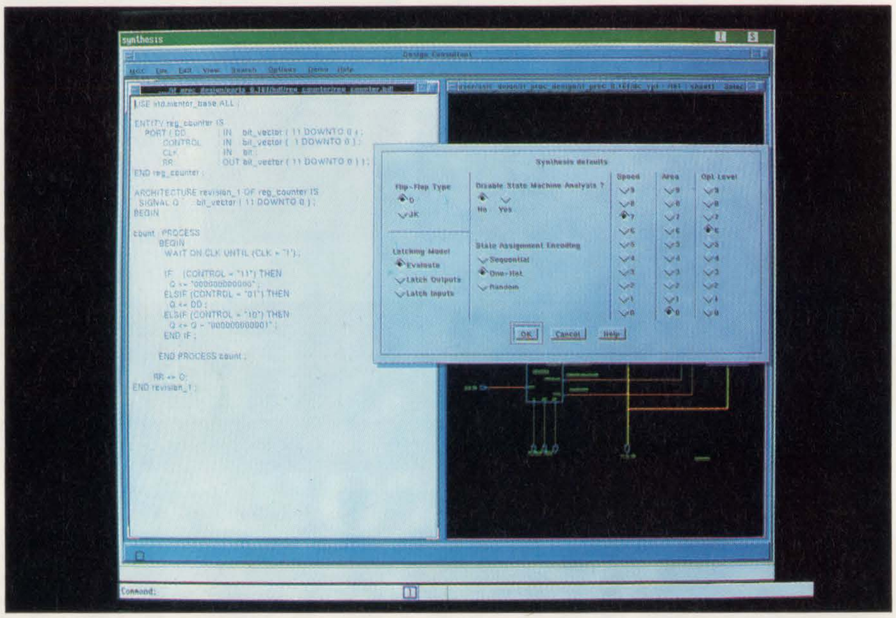
Notes: O = Optional.
* = Consult manufacturer for compatibility of logic-synthesis tool with other CAE tools.

quires that you use detailed timing constraints. Controlling the logic synthesizer by entering the appropriate design constraints is vital to achieving optimum speed and timing results for your specific application.

Optimizing for a foundry

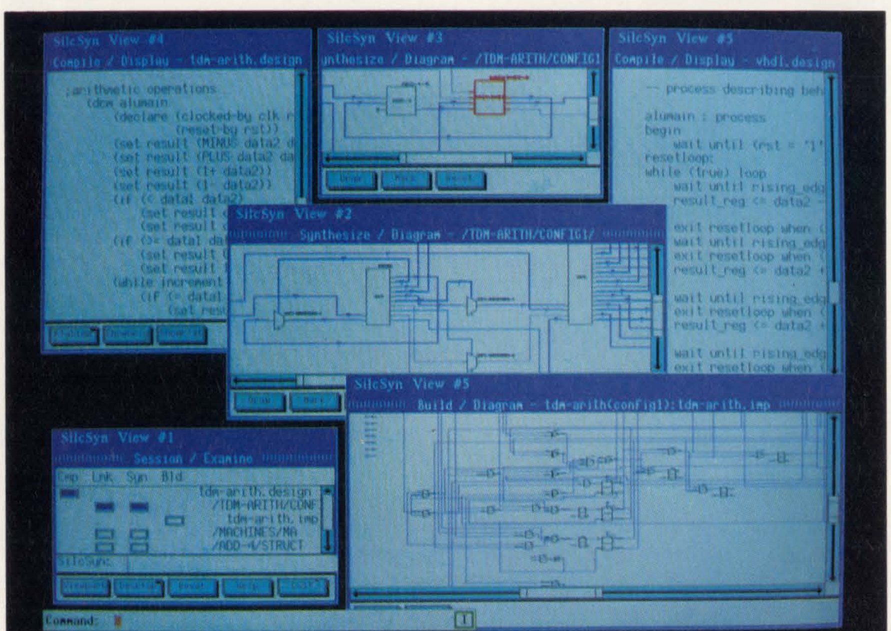
After you enter the design description and design constraints, the logic-synthesis tool should have one more type of design-specific information before it goes to work—the foundry's logic library.

Even without a foundry-specific logic library, a logic-synthesis tool can perform a limited area optimization by minimizing generic gates, a timing optimization by minimizing logic levels, or some combination of the two. However, to evaluate how much area each particular gate or library element requires, the logic-synthesis tool requires the foundry's library, which contains essential area and timing information.



Before using logic synthesis, *you need to specify synthesis options. These are the synthesis options you'd select from before running VHDL Synthesis with Mentor Graphics's Design Consultant.*

The foundry's logic library provides timing data for accurate timing estimates and circuit optimization. Not only can the foundry supply intrinsic gate delays, but foundry-specific libraries also provide data for wire-length models to estimate interconnect delays, input slope-dependent delays, RC interconnect delays, output load-dependent delays, and scaling delays for temperature, supply voltage, and process variations. A logic-synthesis tool should take advantage of the foundry models to evaluate timing if the tool is going to perform accurate area and timing optimization.



Logic-synthesis tools use a variety of graphic and textual information *for both inputs and outputs. This screen shot from Racal-Redac's SilcSyn 2.0 shows some of the information available to users.*

To make use of all the timing information, the logic-synthesis tool needs to incorporate a static timing analyzer. The static timing analyzer should be compatible with the timing analyzer you'll be using to perform your post-synthesis timing verification. Because timing analyzers are dependent on the foundry's library data, you shouldn't have correlation problems, but you should verify that you don't. In many cases, the timing analyzer you'll be using will be the same one the synthesis tool uses. For example, if you're working with Mentor Graphic's Autologic tool, you'll probably be using the company's

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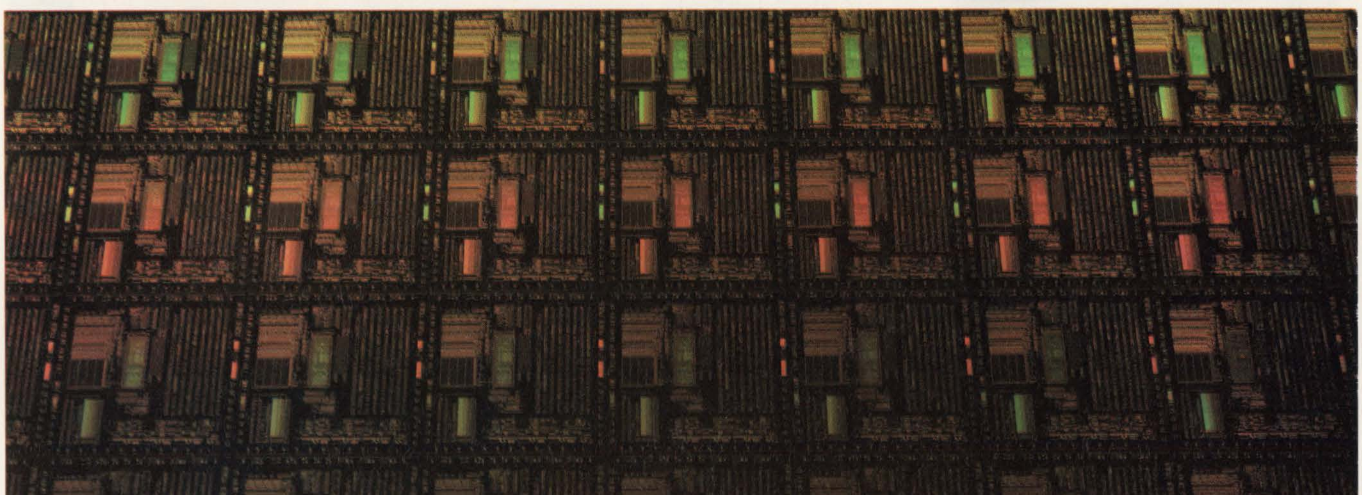

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Logic-synthesis tools

QuickSim II simulator. Similarly, Racal-Redac's SilcSyn uses the timing analyzer from the company's Cadat simulator.

After you've let the logic-synthesis tool synthesize your ASIC design, you can view and evaluate the results. Logic-synthesis tools always provide a net list, and most tools also generate a schematic of the synthesized design. Some tools can also provide a block diagram of the synthesized design. The design report provides such information as the chip area, critical-path timing, timing violations, and other pertinent statistics and information about the design.

If the synthesis results are acceptable, then verify the design completely with the appropriate simulation tools, just as if you had developed the design manually. If the synthesis results aren't acceptable, either iterate another logic-synthesis cycle, changing the design input or design constraints as appropriate, or make the appropriate design changes manually.

If your design doesn't account for testability, you may be able to take advantage of one of the logic-synthesis tools with test-synthesis capability. Otherwise, you should design for testability from the very beginning of your design. Trying to manually wend your way around a synthesized schematic maze to add test structures is painful and wastes much of the precious time logic synthesis should be able to save. EDN will cover test synthesis in more detail in the October 11, 1990, issue.

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For more information . . .

For more information on the logic-synthesis tools discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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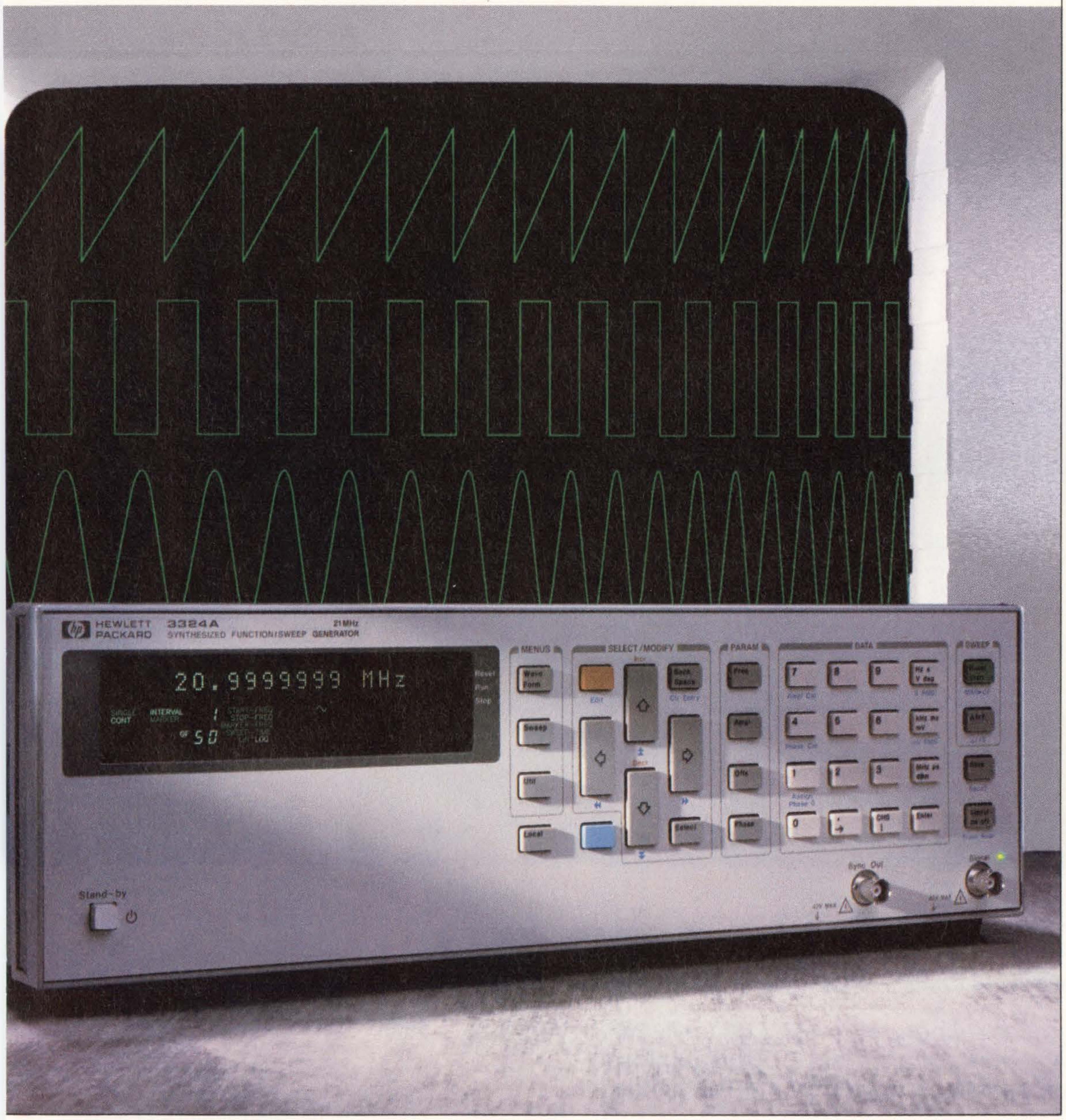

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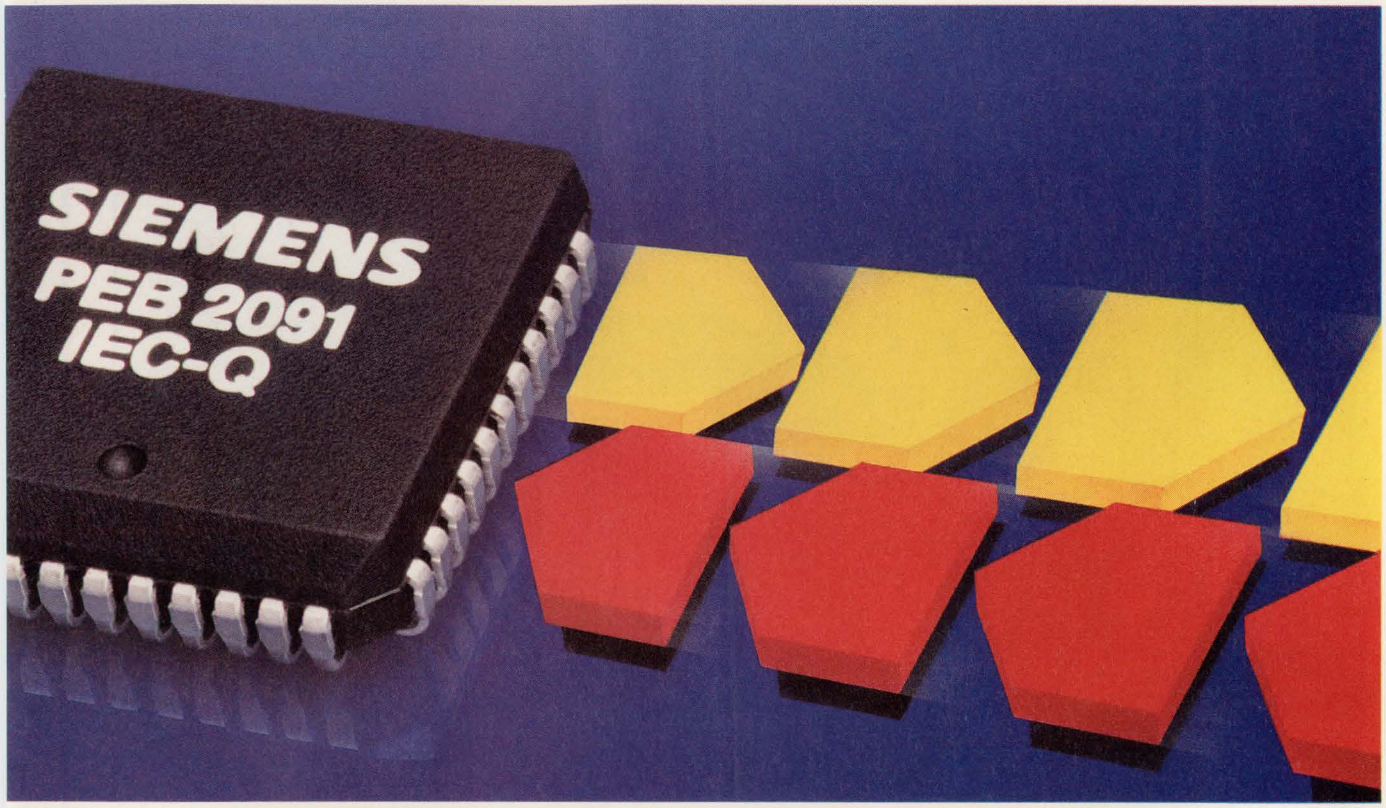

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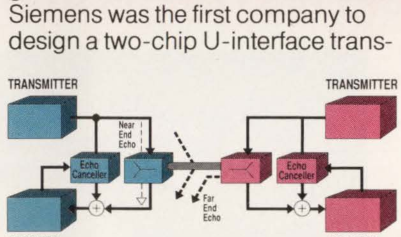

Siemens uses CMOS technology to provide a superior echo cancellation solution with the lowest power consumption requirements.

ceiver for the 4B3T block code used in Europe, and developed the first single-chip device for the 2B1Q code established in North America. And the PEB 2091 meets the requirements of the American National Standard for Telecommunication.

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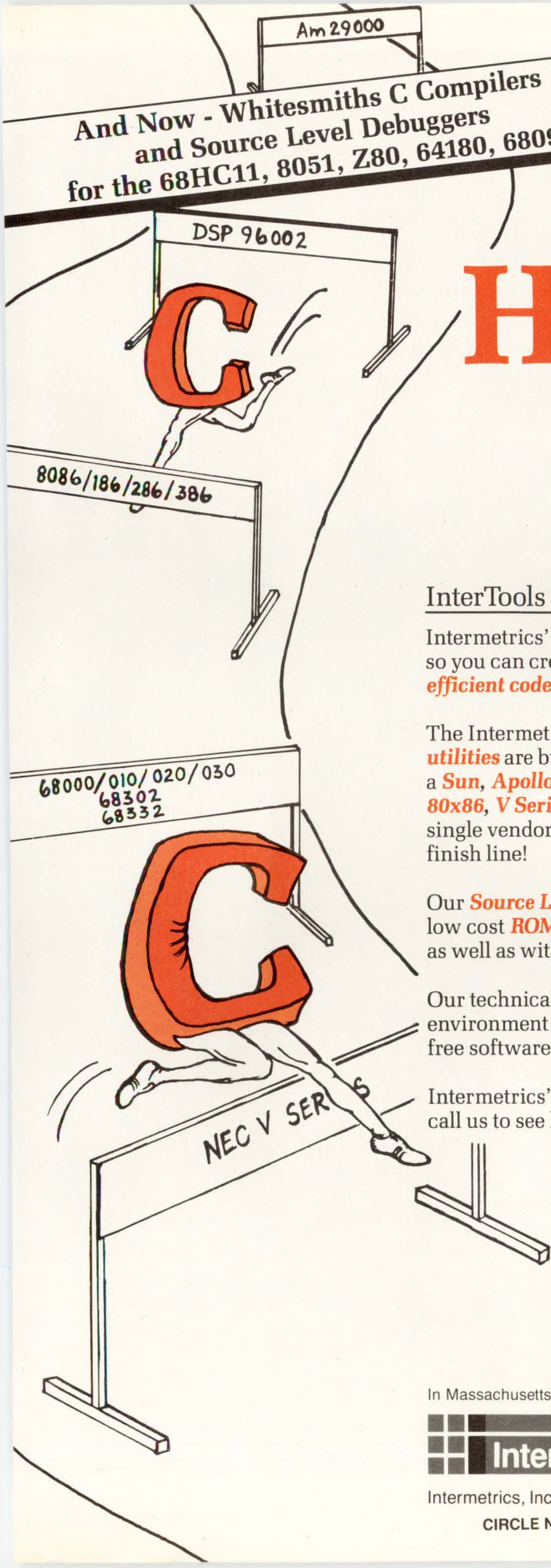

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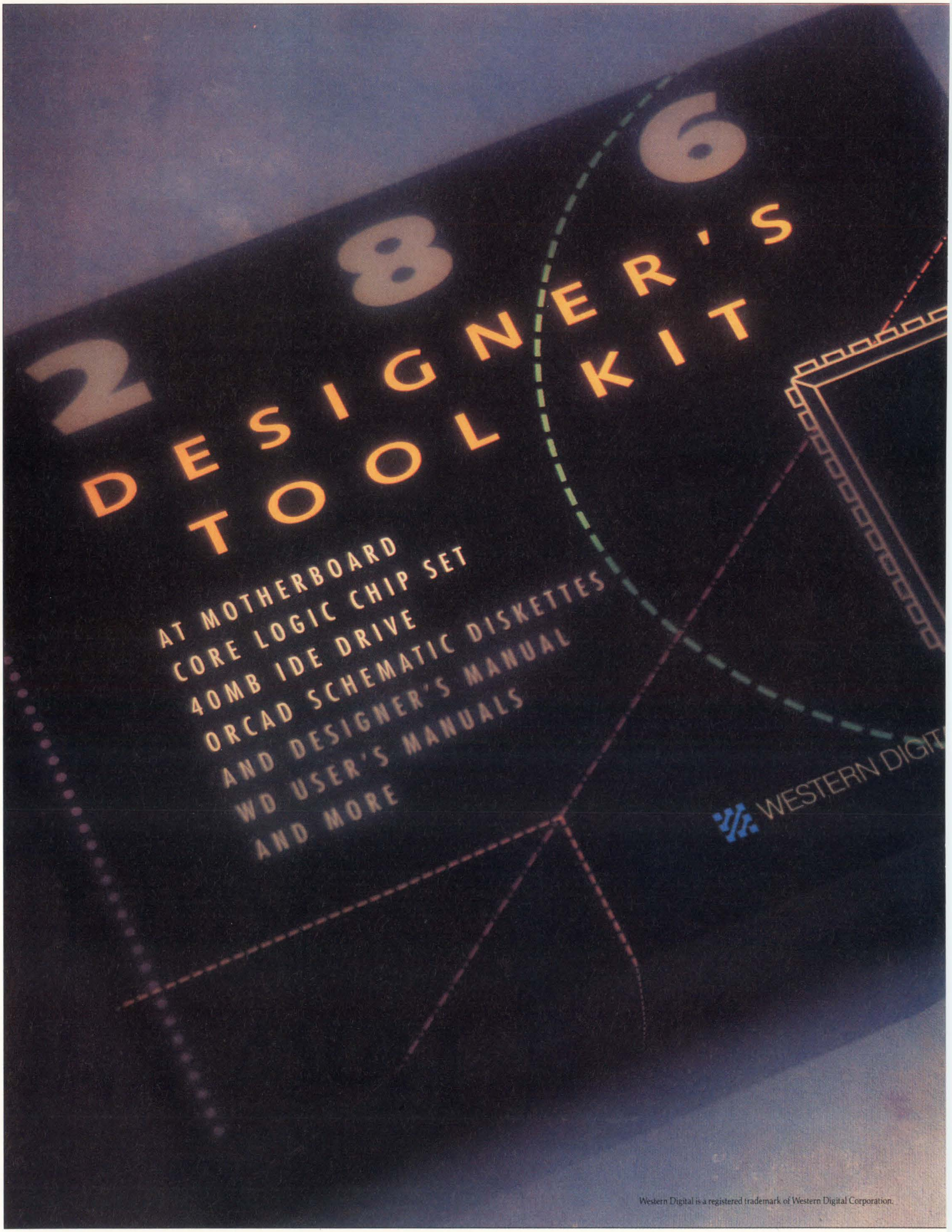
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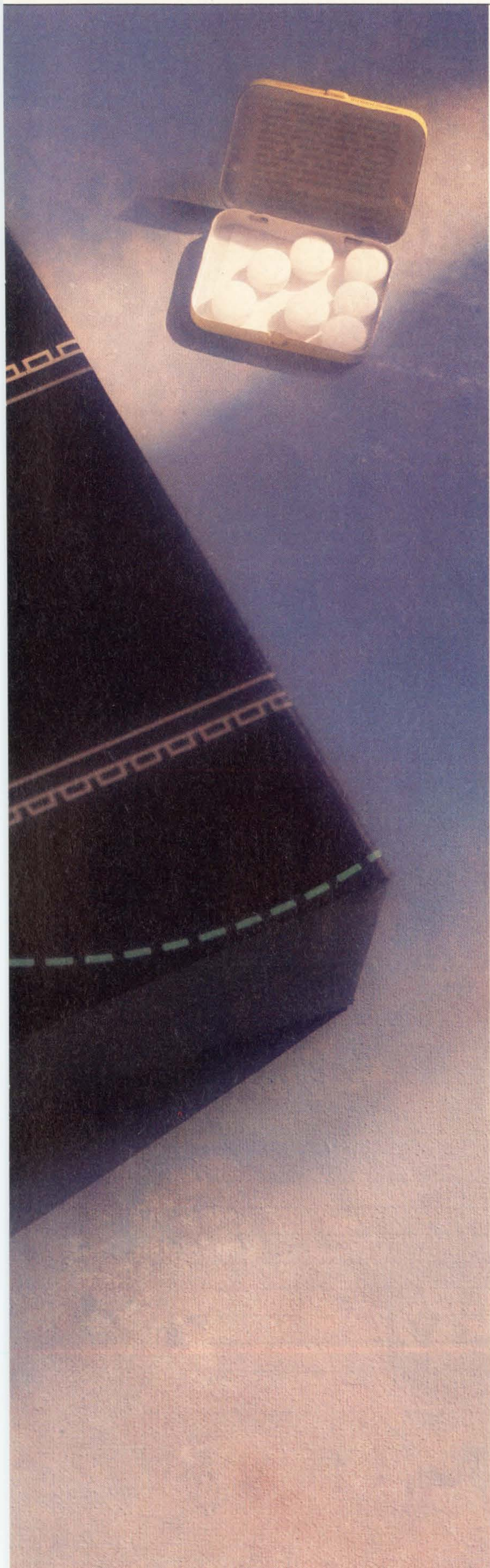

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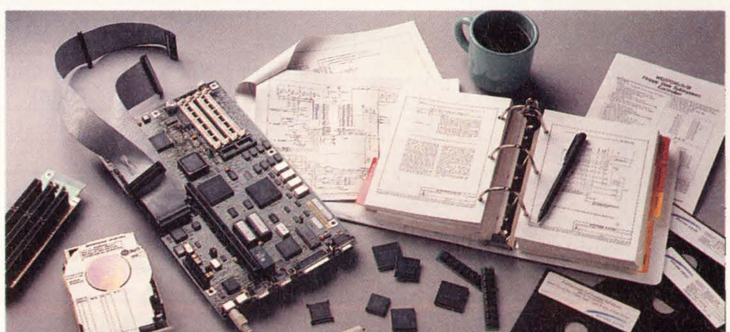

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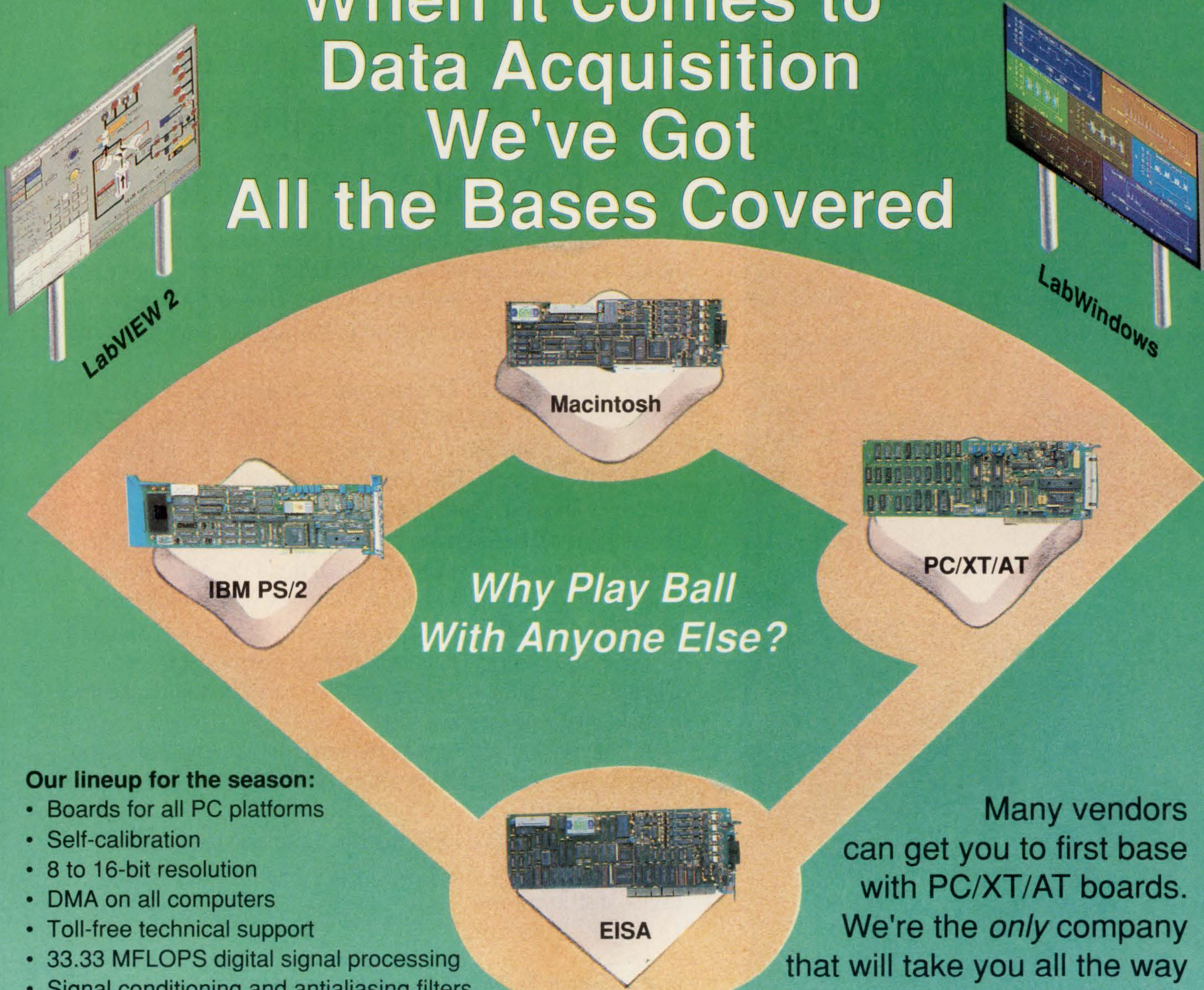

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Lab-SE	Macintosh SE	8	125k	8	2	24	3	–
AT-MIO-16	PC/AT	16	100k	12	2	8	3	√
MC-MIO-16	IBM PS/2	16	100k	12	2	8	3	√
NB-MIO-16X	Macintosh II	16	55k	16	2	8	3	√
NB-A2000	Macintosh II	4	1M	12	–	–	–	√
EISA-A2000	EISA	4	1M	12	–	–	–	√

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CIRCLE NO. 118

Rugged IBM PC-compatible single-board computer for industrial tasks costs $199

Combining low-cost and sturdy design, the 4.5×6.5-in. MCM-SBC41 single-board computer (SBC) gives you IBM-PC compatibility in a form-factor that's small enough for many embedded applications. This board's CPU is based on a 16-bit NEC V40, an 8088-compatible μP. The V40 operates at 8 or 10 MHz and incorporates a serial I/O channel, a DMA, three 16-bit counter/timers, an 8-channel interrupt controller, wait-state generators, and a refresh generator.

You can plug as much as 1M byte of memory into the board's three 32-pin memory sockets. This SBC also comes with three RS-232C channels and a Centronics-compatible parallel port. You can use the board's STD Bus interface to provide additional I/O capability, or you can let the MCM-SBC41 operate independent of the bus. A watchdog timer, power-failure reset circuit, activity LED, and low-power sleep mode make the SBC useful for unattended operation.

Consuming less than 3W, this computer costs $199 (500) or $295 for single units. If you need a low-power CMOS version of this single-board computer, the LPM-SBC41-8 sells for $320 and draws 750 mW.

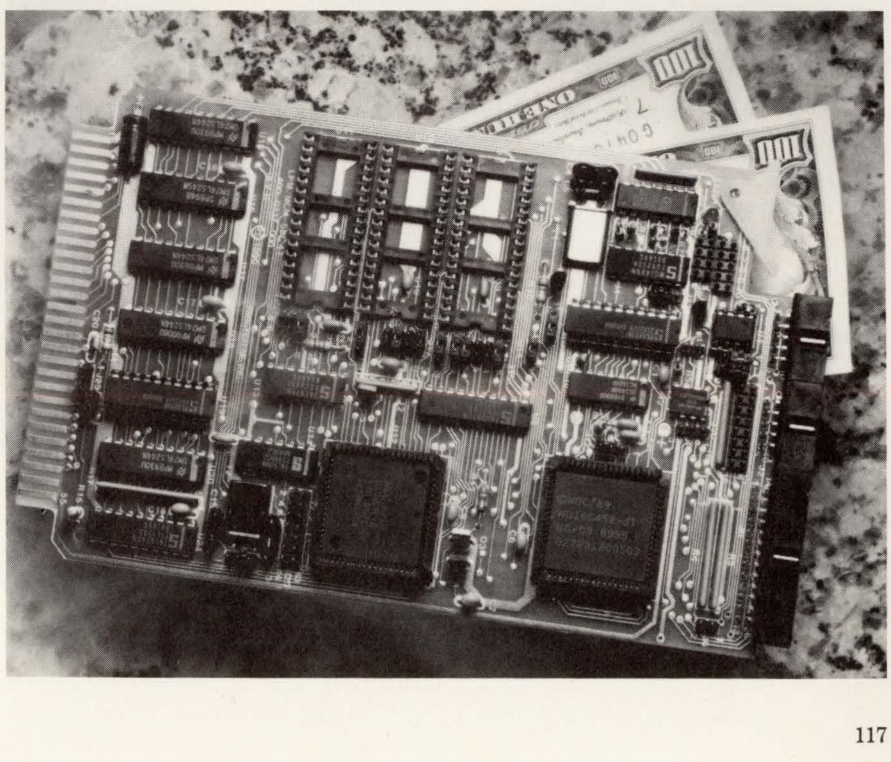
For $195 you can order a development kit for ROM-DOS, an MS-DOS 3.2-compatible ROM-based operating system for embedded applications. By providing hardware initialization code, file support, and software drivers, ROM-DOS lets you run an MS-DOS application in a diskless embedded system. The application starts running as soon as the system obtains operating power.

Optimized for the SBC, ROM-DOS resides in 29k bytes of ROM and uses as little as 5k bytes of RAM. In comparison, MS-DOS requires more than 75k bytes of ROM and takes 75k bytes of RAM to boot the processor. ROM-DOS lets you run programs written in such languages as assembler, C, Pascal, and compiled Basic.

A $495 C-language source-level debugger called C-Thru-ROM is also available. This debugger lets you use Microsoft C or Borland Turbo-C to generate stand-alone ROMable programs for this board. Using this debugger, you can use a PC-compatible computer as a development workstation to debug C source code, assembly language, or mixed code for your embedded application. The debugger provides windows for source code, commands, registers, and expressions.—***J D Mosley***

WinSystems Inc, Box 121361, Arlington, TX 76012. Phone (817) 274-7553. FAX (817) 548-1358.

Circle No. 730



For $195, you can give your embedded-system application an 8088-compatible SBC. *Options for the MCM-SBC41 include a CMOS version, a ROM-based MS-DOS 3.2-compatible operating system called ROM-DOS, and an optional source-level C language debugger named C-Thru-ROM.*

Software offers programmable-device freedom and helps select alternatives

Providing device independence is the goal of Abel-4 software for field-programmable gate arrays (FPGAs) and programmable logic devices (PLDs). The software uses the recently liberated Abel-HDL—the vendor removed the proprietary label at this year's Design Automation Conference—to describe designs without specifying a targeted device or architecture.

Using this software, your only initial concern is your design. You create and simulate your design until you're convinced that it performs correctly. Then the software chooses a list of appropriate programmable devices, based on such constraints as performance, gate resources, and technology and such user-specified data as device cost and stock.

You then use device-specific software called a "fitter" to place and route your design in alternative device architectures. Unlike some other programmable-device tools, though, this one cannot partition a design among multiple devices; it will choose only single-device options from its 300-architecture, 6000-part library.

The software offers device-specific simulation libraries to permit accurate simulation after place and route. Simulation and place-and-route results let you choose the most efficient device.

The software synthesizes logic from equations, state diagrams, and truth tables. A reduction algorithm eliminates redundant logic and therefore simplifies final testing. If your interface logic levels aren't fixed, the software can provide you with either active-low or active-high device alternatives, using a feature called SmartPart intelligent device selection. Similarly, because some device architectures use T-flip-flops and others use D-flip-flops, the software allows you to evaluate your design in both types of devices, without requiring you to modify your HDL description.

The user interface allows you to perform operations out of sequence—the software executes intermediate operations to ensure proper data consistency. Context-sensitive help provides on-line reference manuals.

Currently available device-specific fitters include a generic fitter for traditional PLA/FLPA architectures. (Data I/O claims this fitter supports 150 architectures: two for the Altera EP1800 and the MAX 5032 and 5016; and another for the Cypress Programmable Sequencers 330, 331, and 332. According to the company, additional fitters will be written and provided by both Data I/O and programmable device vendors.

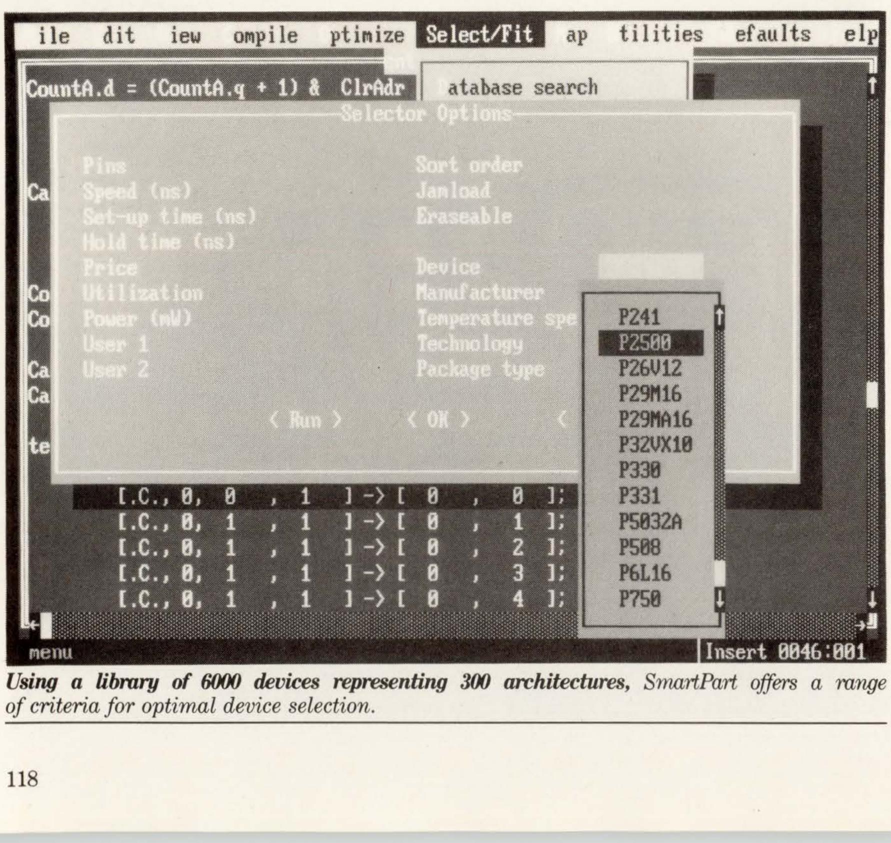
Abel-4 with the four available fitters, SmartPart, and PLDgrade, a fault grader and testability analyzer, running on an IBM PC, PC/XT, PC/AT, and PS/2 costs approximately $3500; SmartPart, including the generic fitter, and PLDgrade each sell for $495. The price of the other three fitters is $295 each.

The complete workstation packages cost $3490 running on Sun-3 and SPARCstations, and $5495 on VAX/VMS workstations. With the exception of the workstation version of PLDgrade, which will be available next month, you can order all software from stock.

—Michael C Markowitz

Data I/O, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 882-1043.

Circle No. 731



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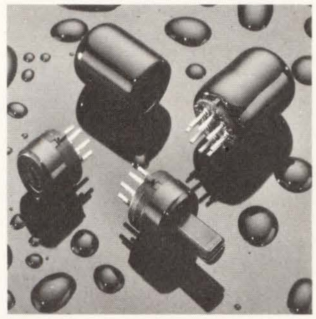

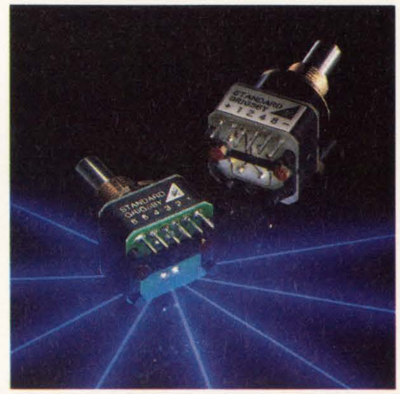

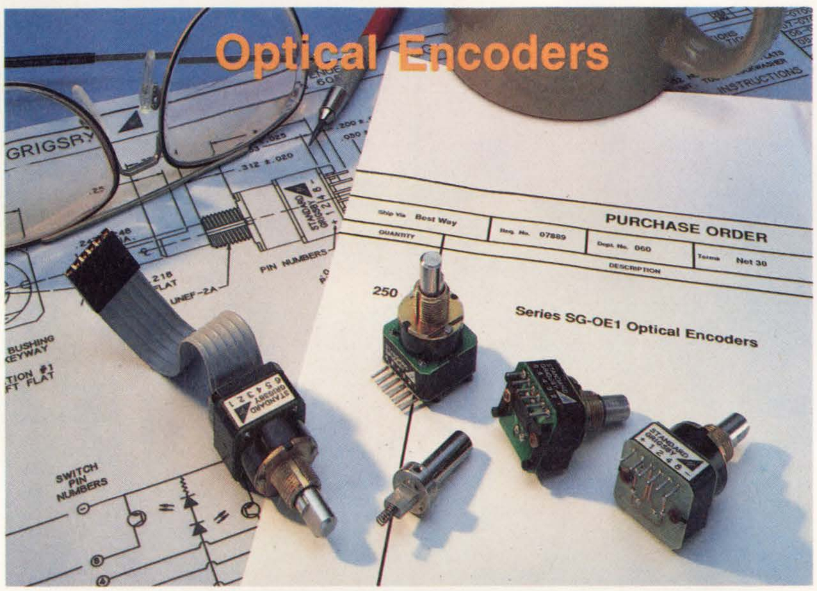

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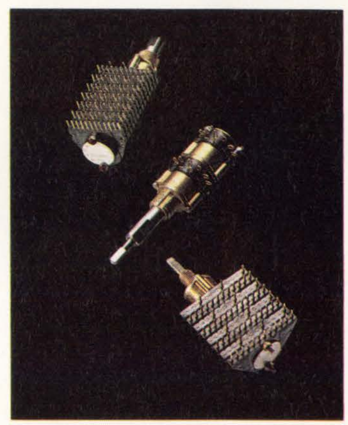
CIRCLE NO. 63

Choose Binary Or Gray Coded. Sugar Grove, IL—Binary and Gray coded optical encoders are available from Standard Grigsby, Inc. Ideal for use in robotics, medical instrumentation, communications, computer peripherals and avionics, the 16-position encoder is available with integral cable or connector. Users may specify custom shaft lengths and diameters.

Priced at $29.10 each in 100-piece lots, the encoders are available in 6 weeks. Standard Grigsby, Inc., 88 N. Dugan Road, Sugar Grove, Illinois 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 61

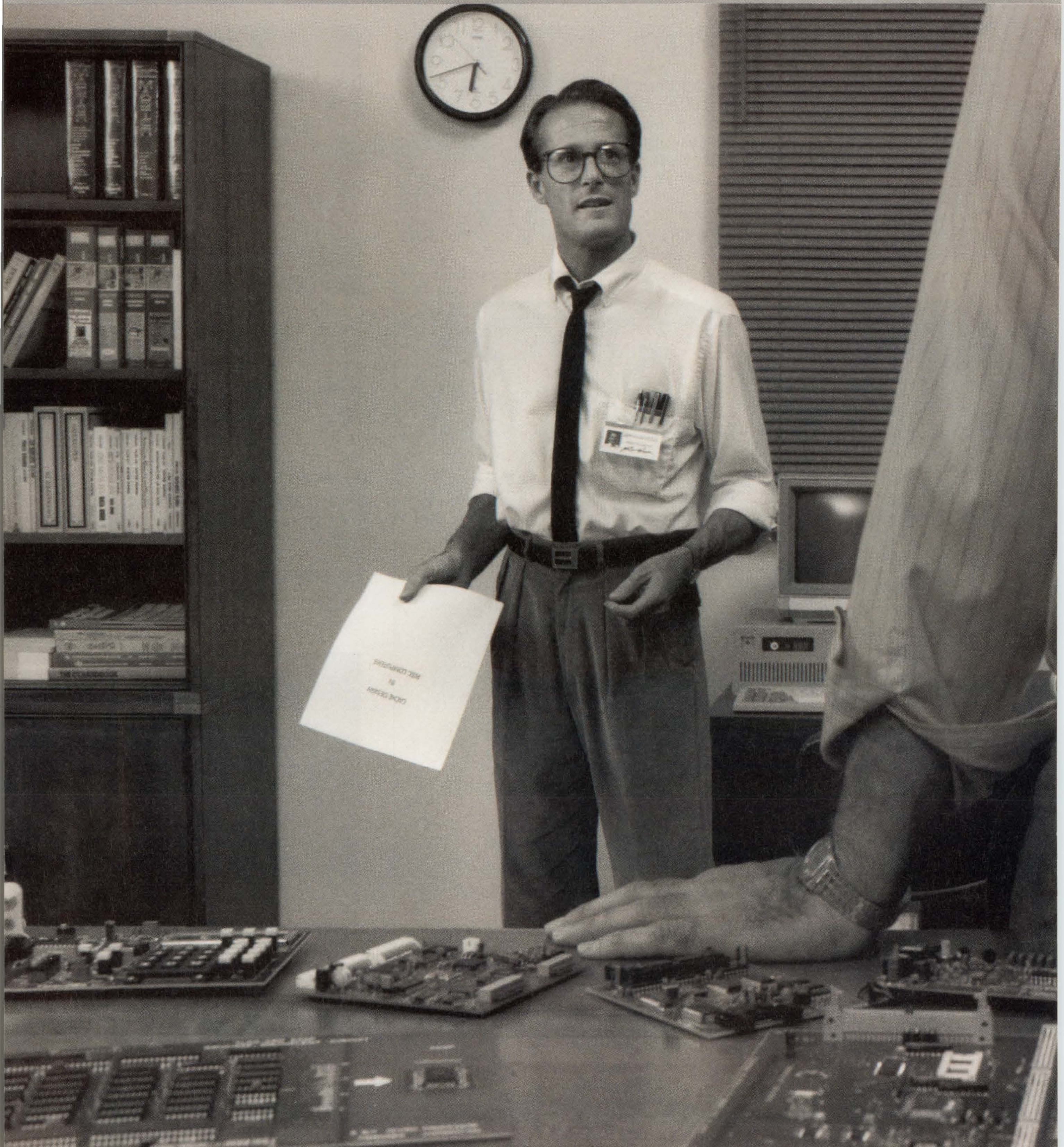


Multi-deck, Multi-options. Sugar Grove, IL—Standard Grigsby's multi-deck rotary switches offer reliability and long life, and retrofit other manufacturers. Measuring approximately ½" in diameter, the switches are available with PC or solder lug terminations, fixed or adjustable stops; 30° or 36° indexing angles; commercial or military finishes.

Priced at $4.50 each in lots of 500, the switches are available in 6 to 8 weeks. For more information, contact Standard Grigsby, Inc., 88 N. Dugan Road, Sugar Grove, IL 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 62

"Have you heard? Toshiba has a full line of high speed



Toshiba semiconductor products are available from a distributor near you. You can reach the distributor of your choice by calling one of the central numbers: Active Electronics, **1-800-388-8731;** Cronin Electronics, Inc., **1-800-5CRONIN;** General Components, Inc., **1-800-524-1463;** Goold Electronics, **1-800-323-6639;** Insight Electronics, **1-800-677-7716;** Itt Multicomponents Corp., **1-800-387-3687;**

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Toshiba high speed CMOS SRAMs are not only fast, they're reliable. And Toshiba has more than 20 years of CMOS experience.

You can cut qualification costs with Toshiba SRAMs, too. All the devices employ the same 1.0μ CMOS process and aluminum master slice that's common to all configurations within each density. So you can qualify by family.

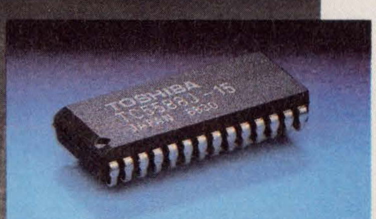
The 20ns Cache Data RAM is the fastest on the market. (25ns and 30ns versions are also available.) The devices are user configurable to either 4K × 18 × 2, or 8K × 18. The × 18 organization gives you two extra bits to support the parity check required in specific applications like Intel's 80486™ Both devices are provided with byte control, and on-chip address latches are designed to interface directly with the Intel 82385™ cache controller. Pinout is compatible with other suppliers.

Toshiba High-Speed SRAMs						
Configuration	Density	Speed (ns)				Availability
64K x 1	64K	35	45	55		Now
16K x 4	64K	15	20	25	35	Now
16K x 4 (OE)	64K	15	20	25	35	Now
8K x 8	64K	15	20	25		Now
8K x 9	72K	15	20	25		Now
4K x 18 x 2	144K	20	25	30		Now
8K x 18	144K	20	25	30		Now
64K x 4	256K	17	20	25	35	Now
64K x 4 (OE)	256K	17	20	25	35	Now
32K x 8	256K	17	20	25	35	Now
32K x 9	288K	17	20	25	35	Now
16K x 12	192K module	25	35			Now
16K x 16	256K module	25	35			Now

PART	$\overline{CE}$	A12	t_{acc}	t_{OE}	V_{CC}	PACKAGE
TC55187	unlatched	unlatched	20/25/30	10/10/12	± 10%	PLCC
TC55188	latched	latched	20/25/30	10/10/12	± 10%	PLCC

Toshiba high speed SRAMs are ideal for high-end system designs. Anywhere you need top speed and fully static operation, Toshiba has a high performance solution.

They offer a wide range of packaging options, too. Why not call today for a complete set of data sheets? Call 1-800-888-0848, ext. 517. *Service is our key component.*



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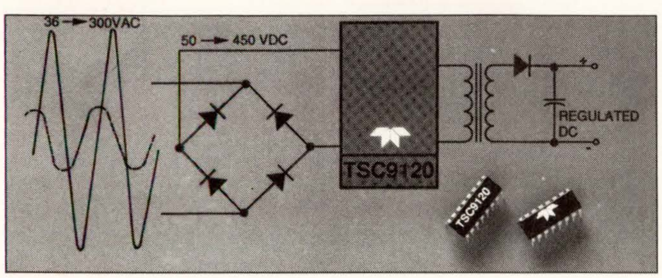
CIRCLE NO. 122

READERS' CHOICE

Of all the new products covered in EDN's **June 7, 1990** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our **June 7, 1990**, issue.

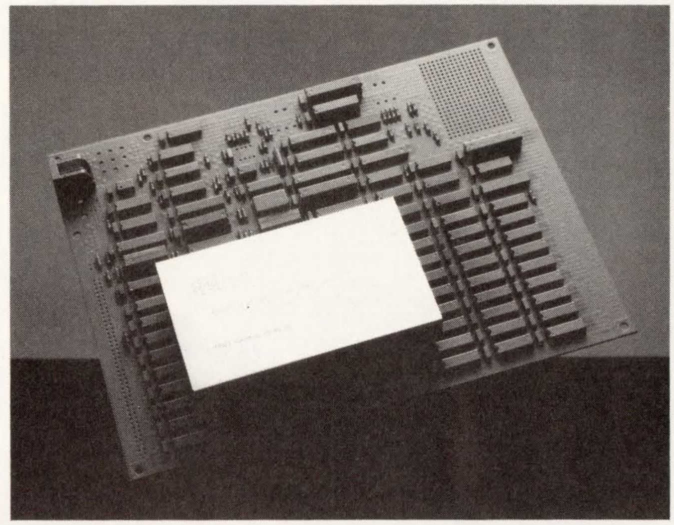
Current-Mode PWM Chip ▼

Featuring self-start at any input voltage from 50 to 450V dc, the TSC9120 PWM controller can operate from any rectified ac power line. The device can implement all popular single-ended, current-mode switch-mode power-supply topologies. It contains an oscillator, voltage reference, error amplifier, and a pulse-modulating comparator. In addition, it does not require a low-voltage power supply for housekeeping/protective functions (pg 175).
Teledyne Semiconductor.
Circle No. 661



Circuit Module ▶

The rtVAX 300 application processor is a 3.1×4.6×0.54-in. circuit module that plugs onto a pc board in your embedded real-time system. The module, with peripheral control circuits and as much as 8M bytes of memory, gives your system 2.7 times the computing power of a VAX computer. Surface mounted within the module are a CMOS CPU, a RAM cache, a floating-point math coprocessor, and an intelligent communications controller (pg 76).
Digital Equipment Corp.
Circle No. 662

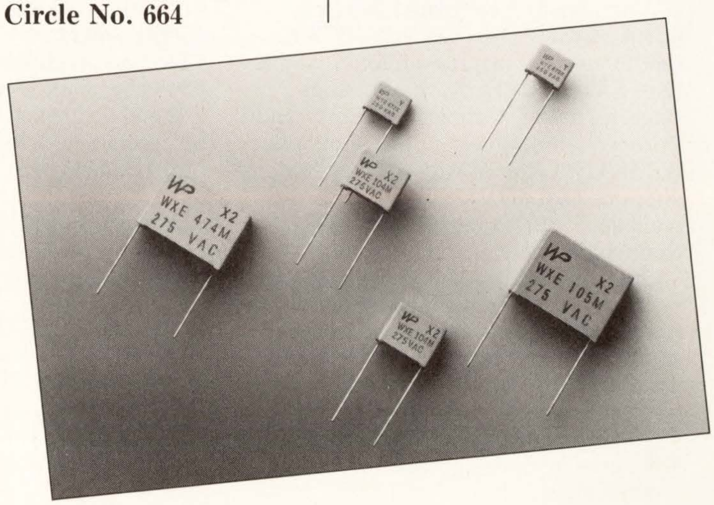


Programmable Disassembler

The programmable disassembler for the vendor's IBM PC-based logic-analysis system provides support for the 6800, Z80, 8088, 78C10, and 8031 μP families. If you're not working with an explicitly supported IC, you can modify the tables to enable the disassembler to handle application-specific devices, including those with embedded μP cores. (pg 146).
BitWise Designs Inc.
Circle No. 663

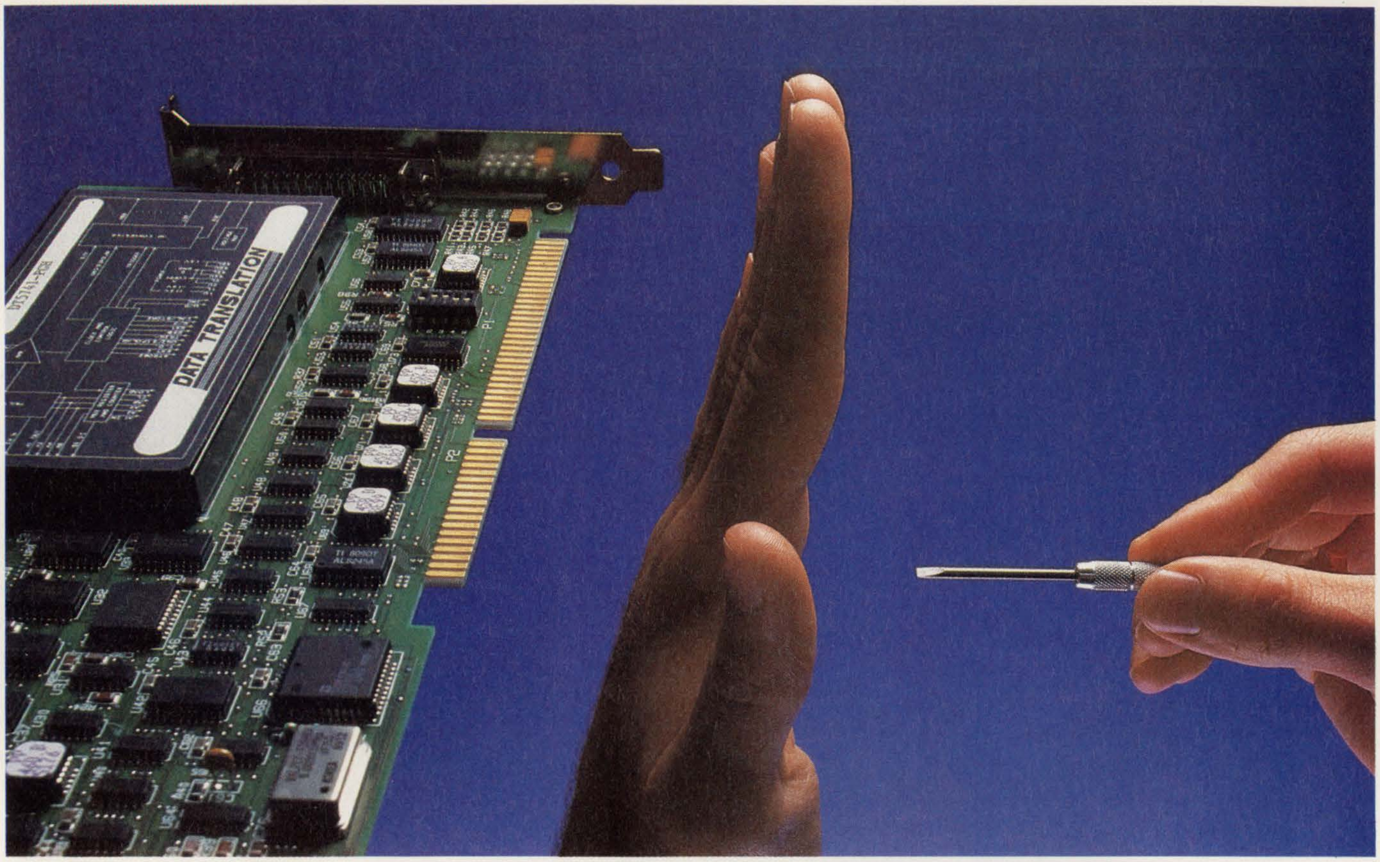
RFI Suppressors ▼

Designed to protect sensitive equipment from RFI, the WXE and WYE series of polyester capacitors accommodate line-to-line and line-to-ground ac-main applications, respectively. The capacitance values range from 0.01 to 2.2 μF for WXE devices and from 0.001 to 0.022 μF for WYE styles. Housed in flame-retardant cases, the WXE and WYE units have dV/dt ratings as high as 1200V/μsec and 2000V/μsec, respectively, and operate to 85°C. (pg 158).
World Products Inc.
Circle No. 664



C++ Compiler

Oregon C++ version 2.0, an object-oriented software-development package, is fully compatible with and provides all features of AT&T's C++ version 2.0. The software, which runs on a variety of workstations, compiles source code directly to the native object code of the host computer without any intermediate translation to C. It comes with an ANSI C library, a library compatible with AT&T's stream-I/O library, and a source-level debugger (pg 178).
Oregon Software Inc.
Circle No. 665



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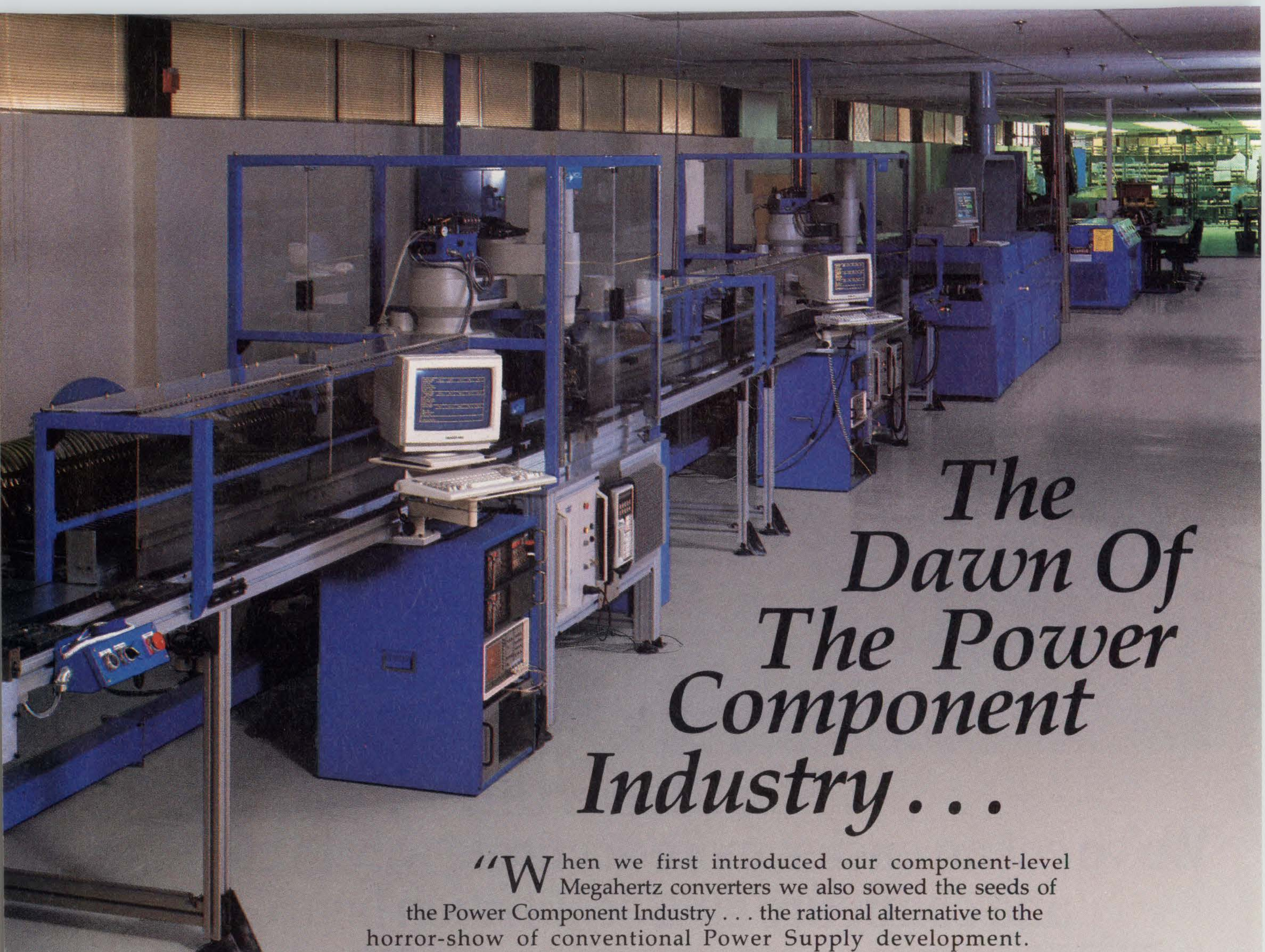

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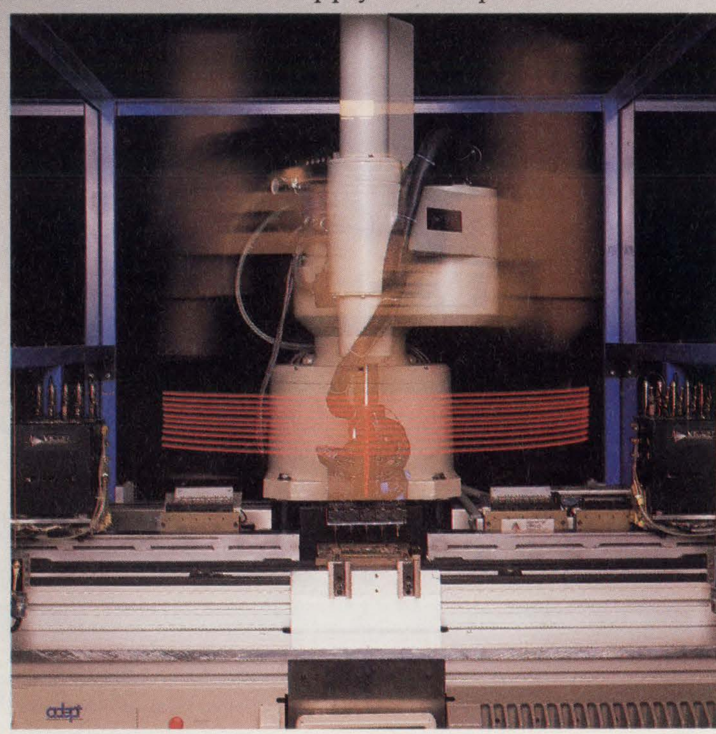

Offering repeatable and predictable performance, and exhibiting power density, efficiency, reliability, and "instant expandability" unachievable with conventional power supplies, Power Components revolutionized the power system design process in much the same way that integrated circuits revolutionized circuit design. Since then, our evolving product line of power building blocks has grown to include high power Mega and Master Modules, off-line Front Ends, FlatPACs, StakPaks, and PowerCages: user-definable, single or multiple-output off-line solutions with outputs from 50 to 7200 Watts . . . offering the highest power densities in the industry. Power Systems Architects have enthusiastically embraced the Power Component concept . . . so many, in fact, that nearly half a million of our expanding line of off-the-shelf component-level power products have gone into service worldwide.

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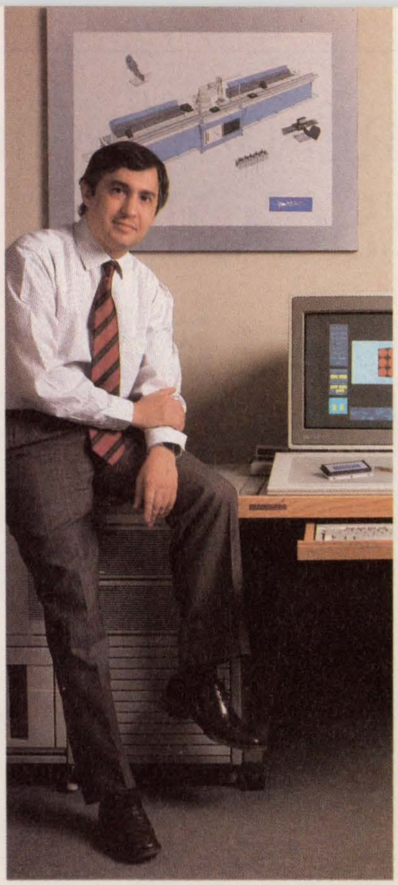

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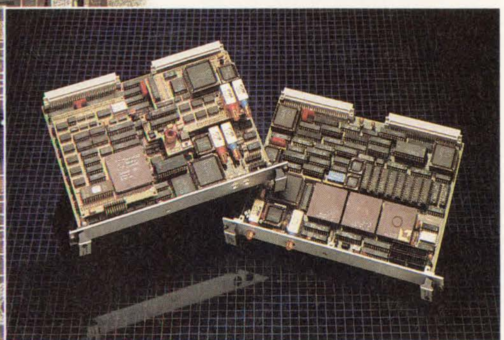
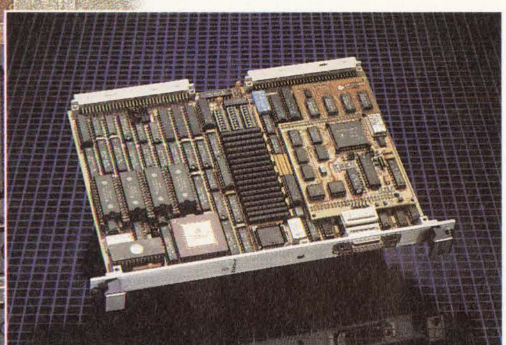
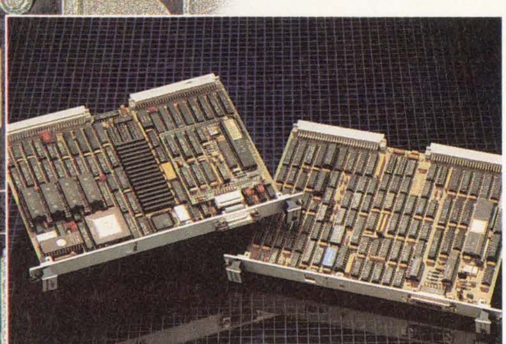


V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon



V/Token-Ring 4212 Owl



V/Ethernet 4207 Eagle
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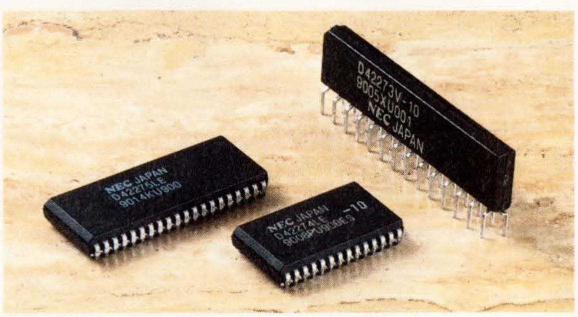

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256K x 4	O	O	
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Special Features			
Fast Page Mode	O	O	O
Flash Write		O	O
Split Buffer			O
Block Write			O
Persistent Write Per Bit			O
Packages			
SOJ	O	O	O
ZIP	O	O	

Major Characteristics	μPD4227X—80	—10	—12
RAS Access Time (Max)	80ns	100ns	120ns
CAS Access Time (Max)	20	25	30
Fast Page Mode Cycle Time (Min)	50	60	70
Serial Access Time ((Max)	25	30	40
Serial Cycle Time (Min)	25	30	40

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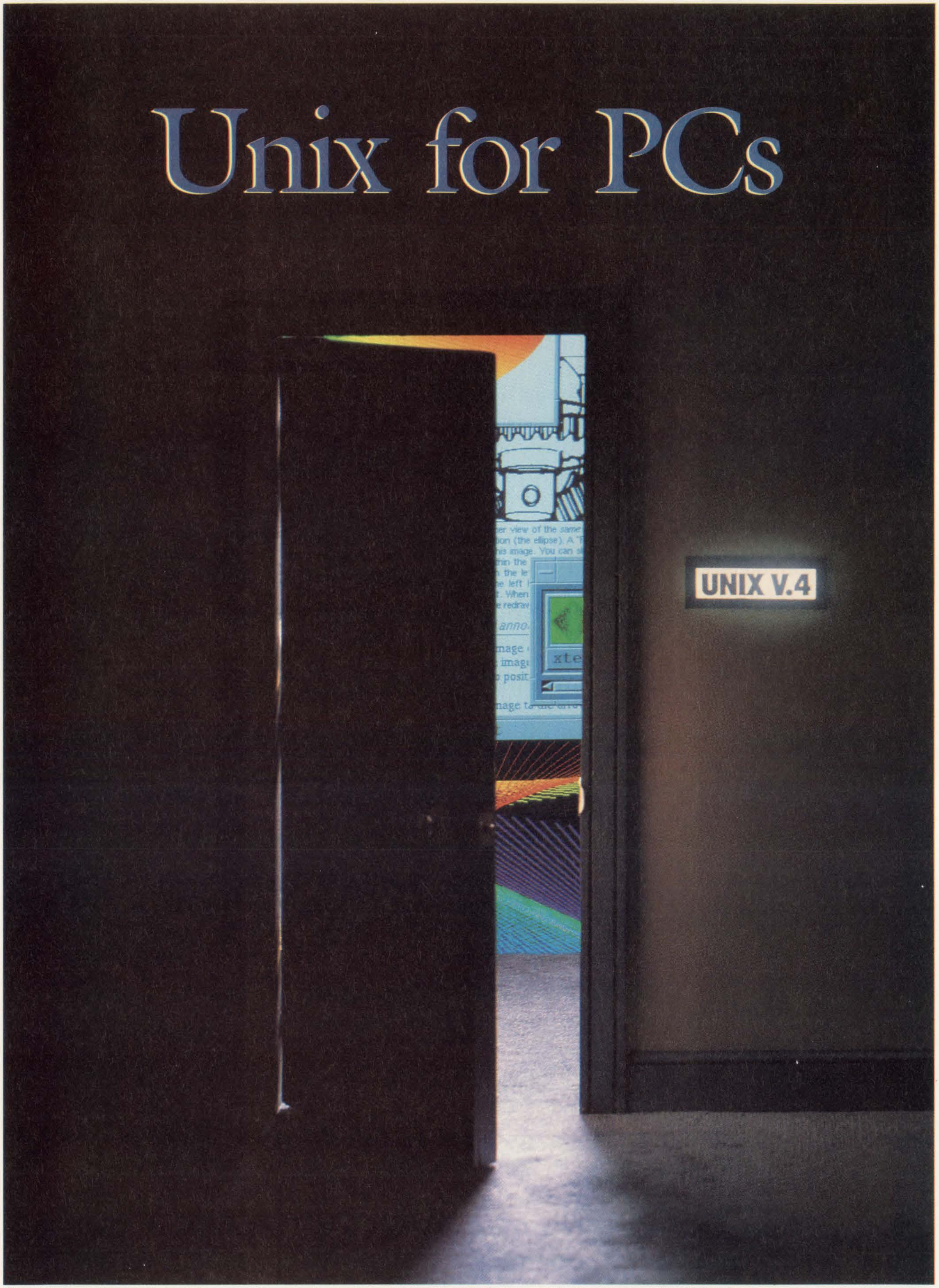
Unix for PCs



New Unix packages help PCs enter the performance realm of workstations. (Photo courtesy Intel Corp)

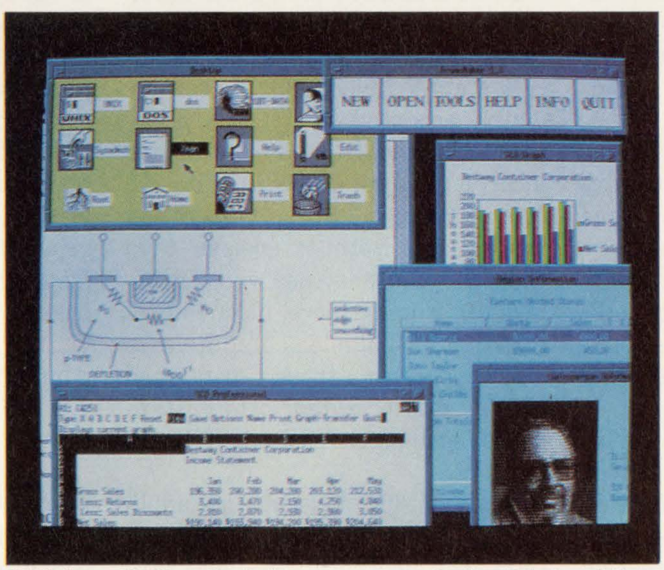
Unix is helping to bridge the gap between PCs and workstations. New Unix offerings for PCs now make available standard graphics and networking capability that was previously available only on workstations. And support of emerging standards in Unix will further aid the PC's progress in the workstation market.

Maury Wright, Regional Editor

Shrink-wrapped Unix for IBM-compatible 80386/486-based or Apple Macintosh PCs offer all of the operating-system features that you'll find on a workstation from Sun or HP/Apollo. And Unix-based PCs maintain compatibility with MS-DOS software without help from simulators, add-in processors, or binary compilers. The newest PC Unix offerings also support de facto network standards such as TCP/IP (transmission control protocol/internet protocol) and NFS (network file system).

The packages also support GUIs (graphical user interfaces) and the X-Windows network graphics standard developed at MIT. Therefore, software developers can easily port software to any system that supports these graphics and network standards. Unix System V Release 3.2 from Unix System Laboratories (formerly AT&T's Unix Software Operation and now a subsidiary of AT&T) provides a temporary standard software base for PCs, workstations, minicomputers, and even many mainframes—but don't get too used to it. A new release of System V—Release 4—just arrived. And, the OSF (Open Software Foundation) plans to release its Mach-based OSF/1 operating system in November.

Unix has been more popular on IBM-compatible PCs than you might think. According to Maggie Conner, an analyst with International Data Corp (Framingham, MA), approximately 200,000 IBM-compatible PCs shipped in 1989 were dedicated to Unix applications. Conner believes that shipments targeted for Unix will grow to 1.5-million units a year by 1994—50% annual growth over five years.



X-Windows, Motif, and a desktop manager make the Unix-based Open Desktop from SCO simple to use and provide the multitasking capability that engineers require of CAE workstations.

Dimitri Rotow, the general manager of Intel's integrated microsystems operation, claims that by the end of 1989, 57% of all Unix installations worldwide had an Intel 80X86 processor. George Meyer, director of product marketing at Interactive systems, believes that a more accurate figure is just over 40%. In either case, the 80X86 is a significant and potentially dominant μP in the Unix business.

To date, Unix has been used with IBM-compatible PCs and other 80X86 systems as a cost-effective multiuser system. To run office applications, a single CPU plays host to numerous RS-232C terminals. The IBM-compatible systems offer tremendous hardware cost savings compared to other systems that don't enjoy the economies of scale the personal-computer business offers.

There are catalogs from Intel, ISC (Interactive Systems Corp), and SCO (The Santa Cruz Operation) that list thousands of applications that run on 80X86-based Unix.

Unix System V Release 3.2 offers the open-systems computer industry a stable standard software-technology base for the first time.

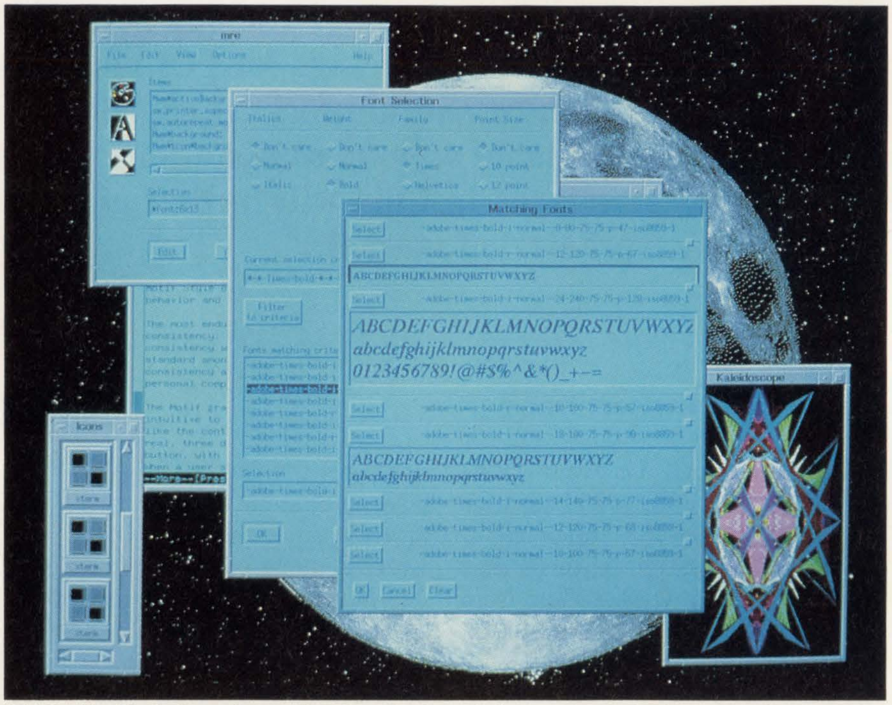
Among the applications are horizontal office software such as spreadsheets, database managers, and word processors—for example, Microsoft Word for Unix. In addition, vertical applications, such as packages for medical or legal offices, abound.

Most of the available technical Unix software targets civil-, mechanical-, and structural-engineering applications. A good example is the popular AutoCAD program from Autodesk (Sausalito, CA). It suits applications in all three engineering disciplines. A smaller number of companies offer engineering and scientific software for 80X86-based systems, such as math and simulation packages, that are useful to electronic engineers.

Unix on the Macintosh has not enjoyed the success that Unix for IBM-compatible PCs has. Macintosh computers use the 680X0 processor family. 680X0-based systems have been second in popularity to 80X86-based units as Unix hosts, but Macintosh has not provided the cost benefits for value-added resellers selling multiuser systems that IBM-compatible PCs do.

Standards will spearhead the Unix market's growth for IBM-compatible and Macintosh PCs. Just two years ago, different system manufacturers took vastly different routes to offer Unix. Some used System V as a technology base. Some used Berkeley Unix, from the University of California—Berkeley. Other companies offered proprietary Unix-like operating systems.

System manufacturers worldwide, however, have been driven by customer demand toward standards and open systems. The standards movement led to the creation of industry organizations such as X/Open (San Francisco, CA) to establish international standards for software portability. The OSF has evolved to develop standard operating systems; Unix International has evolved to assist and to guide development of standard operating systems (**Ref 1**).



OSF/1 will ship in November and add to the Open Software Foundation's product family, which includes the X-Windows-based Motif GUI.

System V Release 3.2 has become widely accepted as a standard. Intel, ISC, and SCO products have incorporated compatibility with Microsoft's Unix-like Xenix operating system and with extensions from the BSD (Berkeley Software Distribution). Furthermore, most companies that have implemented Release 3.2, including those mentioned above, have added other standards, such as X-Windows, TCP/IP, and NFS.

Many of 80X86-based Unix applications are text based. The applications that incorporate graphics have done so without the benefit of standards. Release 3.2 with X-Windows, however, offers software developers a stable graphics platform to develop software for. And even Release 4 and OSF's planned operating systems depend on X-Windows to ensure portability of graphics applications.

The move to an industry standard graphics-based Unix implementation will certainly benefit users of business and vertical-market software on Unix-based systems, a group that includes PC users. In fact, the explosion of graphics-based applications software for Unix systems should feed off the popularity of Microsoft Windows 3.0 for PCs and the Apple Macintosh.

CAE applications need graphics

Standard graphics-based Unix will also be a boon to people who use PCs for CAE applications. The large CAE software companies all use one or more of the same group of hardware platforms to host software. For example, until recently Mentor Graphics (Beaverton, OR) only sold its software bundled with Apollo workstations. Mentor offers a full suite of integrated CAE tools that facilitate designing ICs, boards, and systems.

Mentor developed a proprietary graphical interface for its entire software base, thereby making its software easy to use. But now it offers its software based on X-Windows and OSF's Motif GUI because these industry standards also offer ease-of-use features. End users will benefit from the standard look and feel of software from different vendors and from the ability to run the same applications software on vastly different hardware. Companies such as Mentor can now offer software on more hardware platforms with far less effort.

Unix International plans to standardize an ABI (application binary interface) for each processor family. If that happens, X-Windows-based applications software (in binary executable form) written for a 680X0-based Hewlett-Packard/Apollo system would run equally well on a Macintosh or other 680X0-based system that implements X-Windows. Furthermore, the software developer would only need to recompile the program to move the software to a new processor.

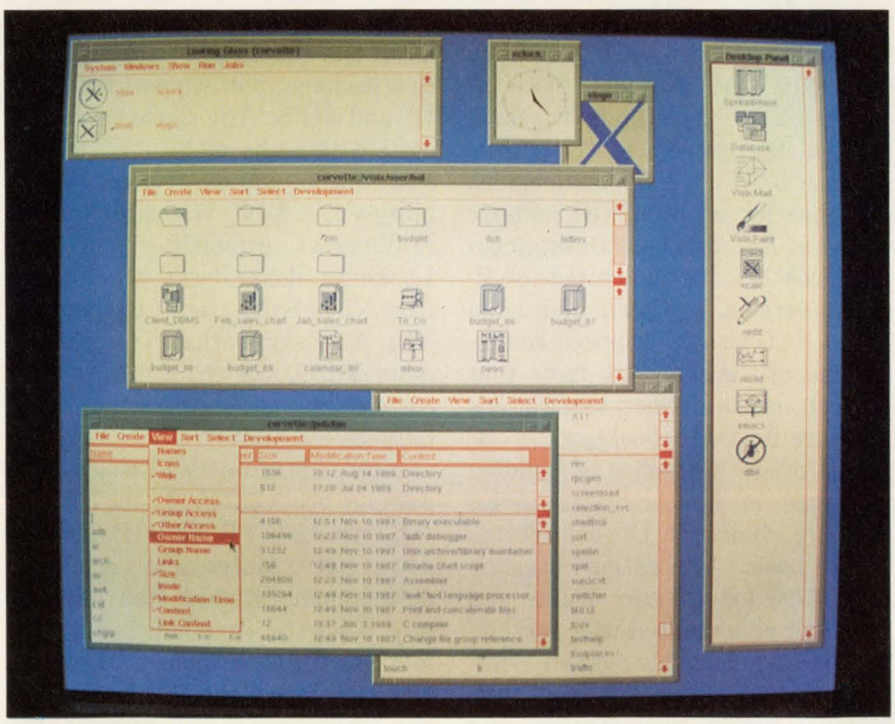
The ABI scenario depends only on system manufacturers implementing standard X-Windows and Unix. OSF has proposed taking portability a step further by using some type of ANDF (application neutral distribution format) technology. The company has studied ways to distribute software in some intermediate format so that final compilation or conversion to binary form can occur on any host processor. A successful ANDF technology would allow software developers to distribute one shrink-wrapped package for all hardware platforms.

ABI standardization will happen and ANDF technology, if it becomes a workable standard, will make things even better. But for now, simply making X-Windows standard already gives software developers a huge incentive to port applications software. Over the next year or two, expect CAE software vendors to rush to offer software for PCs. The installed software base plus new sales of PCs dwarfs the number of workstations sold. High-end PCs offer a suitable platform for CAE from a hardware standpoint (see **boxes**, "Systems components suit MS-DOS and Unix," and "Unix erases the line between PCs and workstations"). And software vendors are certainly in the business to sell as many packages as possible.

Unix moves PCs to workstations

The availability of full-featured Unix provides the missing link that moves high-end PCs into the workstation market. Intel, ISC, and SCO offer such Unix versions for 80386- and 80486-based machines. The vendors feel that the 80286 and earlier processors don't offer the performance needed to host Unix, although SCO does market its Xenix product for 80286 systems and claims to have substantial demand in the multiuser vertical markets.

Intel's, ISC's, and SCO's products, in addition to being based on System V Release 3.2 and offering X-Windows, TCP/IP,* and NFS bundled with the operating system, also have backward compatibility



The Looking Glass desktop manager, from Visix Software, comes standard with ISC's Architect Workstation package. You can also purchase the popular software for SCO and Intel Unix systems.

Bundled Unix packages that include GUIs and desktop managers offer similar capabilities as CAE workstations packages.

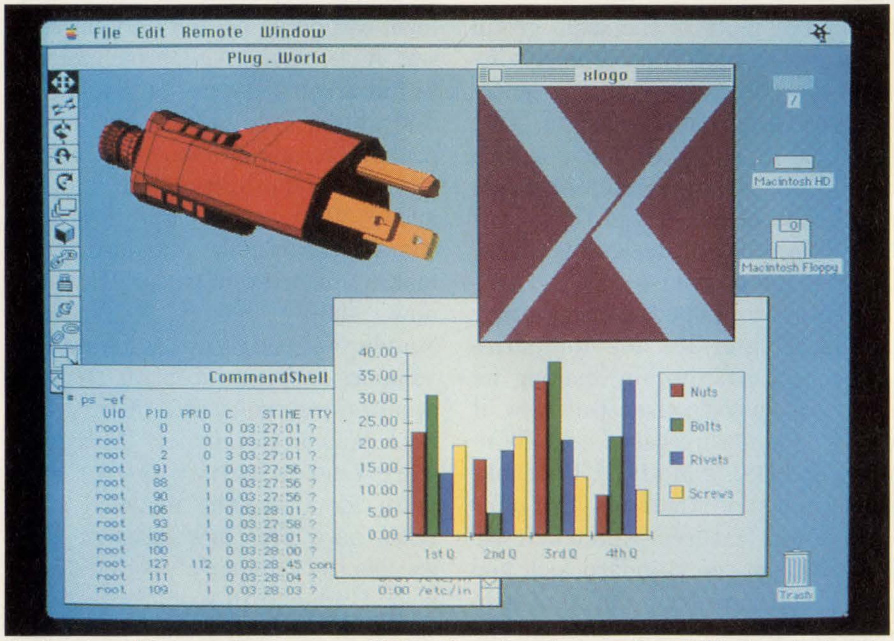
with Xenix. SCO set a new price point with its $995 Open Desktop package it introduced about a year ago. The package includes the X Library routines, X Toolkit Intrinsic routines, the Motif Toolkit and Styleguide, and a desktop manager called X.Desktop from IXI Ltd (Cambridge, UK).

Package has network support

Open Desktop also includes implementations of TCP/IP and NFS and an implementation of LAN Manager Client. The package integrates the capabilities of Locus Computing's (Santa Monica, CA) DOS Merge package. DOS Merge lets you run MS-DOS software under Unix's control. You can install DOS software in the Unix file system using Merge, or Merge can read a DOS partition on any system disk drive.

The Open Desktop bundle also integrates the SQL-based Ingres relational database from Ingres Corp (Alameda, CA). The base price includes a 2-user license. SCO sells a stand-alone version of System V Release 3.2 for $895 that includes a license for an unlimited number of users. Adding Open Desktop capabilities to the unlimited-use-license version costs an additional $1500. SCO also sells various combinations of development tools that you can use to develop applications software for Open Desktop.

ISC offers a number of bundled packages in its Architect Series that are similar to Open Desktop. ISC's basic Application package costs $795 for a 2-user license and $1795 for an unlimited-user version. The package includes System V Release 3.2, ISC's Ten/Plus user interface, electronic mail system, and VP/ix, which offers MS-DOS compatibility similar to the DOS Merge.



Macintosh and Unix applications run side-by-side under the control of X-Windows in Apple's A/UX 2.0 Unix based on System V Release 3.2.

You can add full development capabilities for $900.

ISC's Network package includes all of the functions of the Application package, plus support for TCP/IP and NFS. The 2-user package costs $1095, the multiuser package costs $2095, and development capabilities cost $700. Workstation adds X-Windows capabilities and the Looking Glass desktop manager from Visix Software Inc (Arlington, VA). A 2-user Workstation package costs $1295, the multiuser version costs $2295, and development capabilities cost $700.

Intel's System V Release 3.2 package costs $2745 (2-user license) and includes NFS, TCP/IP, X-Windows, Locus Merge, and a complete development system. You have to buy separate capabilities such as Motif or the Open Look GUI, which was developed separately by Sun and Unix System Laboratories. Intel developed the 80X86 version of Release 3.2 and the ABI in partnership with Unix System Laboratories. This shrink-wrapped package is Intel's first venture into reselling Unix. Unix System Laboratories sells Release 3.2 source code for 80X86 systems for $100,000.

Installation software eases start

The offerings from Intel, ISC, and Unix look similar on the surface, but there are differences, most notably the installation procedures. SCO's Open Desktop offers the simplest installation. You can install it in a default configuration on a standard system by doing practically nothing more than feeding the system the 25 floppy disks containing the programs in compressed form. The installation creates a user account and a default configuration comes up and runs in graphics mode. Few people probably really need the exact default configuration, but it gives you a working system that you can then modify.

ISC's installation requires a little

more effort. The Workstation Developer package includes 66 floppy disks (by press time, the company plans to be shipping a compressed version that uses about half as many disks). Installing a basic kernel is simple, and the installation package allows you to then add options such as network and X-Windows support. The installation software does instruct you in the general order that you should add options. You'll still need some expertise or help to get the full package installed on the first try.

Intel's package, which is the newest, includes by far the most cryptic installation instructions. You can simply install and build a basic kernel, but adding options requires that you go it alone. Each option

Systems components suit MS-DOS and Unix

Choosing a system and components to run Unix mandates choosing a fast processor. You should also choose disk drives and graphics boards that offer suitable performance—but make sure the system components you choose can also serve your MS-DOS needs, because you don't want your components to be incompatible with the world's largest software base.

At a minimum, you'll require a system based on the Intel 80386SX processor. More practically, a 25-MHz or faster 80386-based system with a static RAM cache will provide suitable performance. And any 80486-based system will prove to be a suitable system for Unix.

In evaluating the available Unix packages, I used a system based on Micronics Computers' (Fremont, CA) Model 80386 ASIC Cache System board. The mother board operates at 33 MHz and features a 64k-byte, 2-way-set-associative cache. The PC/AT bus board includes sockets for as much as 4M bytes of dynamic RAM; you can add 16M bytes of additional memory via a proprietary 32-bit memory board. The Micronics board provided power aplenty to run Unix.

I used IDE (integrated device electronics) disk drives to host Unix. IDE drives include an embedded controller, yet offer complete compatibility with the standard Western Digital ST-506/412 controller that IBM used in its PC/AT computers. The drives therefore offer some of the benefits of intelligent SCSI drives such as on-drive cache, but do not require special drives to work with operating systems other than MS-DOS. I felt that IDE drives would eliminate the compatibility problems inherent in finding a single SCSI host adapter that would support multiple peripherals and multiple operating systems.

The Unix packages were tested with Conner Peripheral (San Jose, CA) 3104 (100M bytes) and 3204 (200M bytes) drives. The intelligent Conner drives can adapt and operate transparently as virtually any drive geometry (the number of heads, cylinders, and sectors). Therefore, you need only choose an entry in a PC's BIOS drive table of the same or slightly lower capacity to make an IDE drive work flawlessly. The drives proved to be solid performers running Unix.

A 34010-based board provided intelligent 1024×768-pixel graphics for the test. Graphic Software Systems (GSS) (Beaverton, OR) designed and built the AT-1000 board, but only sells the board on an OEM basis. NEC sells a shrink-wrapped version under the name Multisync Graphics Engine. The board also includes an integrated VGA controller to ensure compatibility with a wide variety of software. GSS, however, offers drivers compatible with the Unix packages I tested, so I was able to take advantage of the on-board graphics processor.

My test system can match any low-end workstation. The 200M-byte drive provides 120M bytes for Unix and an 80M-byte MS-DOS partition that ensures full compatibility with all MS-DOS software.

The system proves economical for do-it-yourselfers, too. You can buy the Micronics mother board for a discount price of about $1500. Add $1000 for the 200M-byte disk drive, $1000 for the graphics controller, $1000 for a monitor, $500 for a network card, and $300 for case, power supply, I/O ports, and keyboard. The $5000 to $6000 price tag with RAM added matches Sun's new low-end 25-MHz diskless SPARCstation with a monochrome monitor. You can add 25 to 50% to the price to buy it assembled and tested, and even more to have a value-added reseller install it in your office. But you have to pay the value-added reseller to configure and install a workstation as well.

Vendors of Unix for PCs all have interest in OSF/1 because major system vendors such as IBM, DEC, and HP/Apollo have voiced support.

includes separate installation instructions, and you must figure out the proper sequence of installation alone.

Intel, ISC, and SCO all also offer their software on QIC-24 magnetic tape. You can simplify the process of swapping floppy disks greatly if your system includes such a tape drive. Furthermore, you can install Unix on one system and move the fully configured package to other systems via tape drives if you purchase the appropriate licenses.

All three packages include support for popular IBM-compatible peripherals such as VGA graphics and Western-Digital-compatible (Irvine, CA) ST-506/412 drives, IDE (integrated drive electronics) drives, and ESDI (enhanced small device interface) disk controllers. The packages all support the Adaptec (Milpitas, CA) 1540 SCSI host adapter as well. Make your choice of a hard disk for Unix carefully, however. A SCSI drive will probably provide the best performance. But bus-master SCSI host adapters, such as the Adaptec 1540, can conflict with some 80386/486-specific MS-DOS software that uses expanded memory—and you may not want to risk compatibility problems with DOS (**Ref 2**).

You may also need to choose ST-506/412, IDE, or ESDI drives that match entries in the BIOS drive table on your system. You can buy utility software for MS-DOS that can adapt to any disk drive. Only SCO's Unix product allows you to enter drive parameters that differ from the ones your system BIOS support, however. With the Intel or ISC product, you have to settle for less capacity than your drive is capable of if it doesn't match a table entry.

All of the products support standard VGA, but ISC's product in-

Unix erases the line between PCs and workstations

Technically, workstations and high-end PCs are the same—despite any list of differences you may have seen. They both have fast μPs, many megabytes of memory, large, fast disk drives, network capabilities, and intelligent, high-resolution graphics. As the saying goes, "if it looks like a duck, walks like a duck, and quacks like a duck, then it's probably a duck."

Articles that say workstation graphics are superior to PC graphics abound. Yet every time a workstation vendor introduces a new product, it includes a medium-resolution monochrome monitor—and therefore features a low base price. In 1983, for instance, you could get an IBM PC-compatible board that supported 256 colors and 1600×1200-pixel resolution.

You can now buy intelligent graphics boards for PCs that support 1280×1024- or 1024×768-pixel resolution and 256 to 16.8 million colors from more than 50 vendors. Likewise, Apple introduced a similar NuBus product recently for Macintosh. You simply have to buy high-resolution graphics for PCs or workstations.

Sun Microsystems started a trend by including network hardware and TCP/IP (transmission control protocol/internet protocol) and NFS (network file system) software as a standard system feature. Other workstation vendors have followed suit. You can purchase equivalent Ethernet network hardware for PCs, however, for $500 or less. And Unix packages for PCs include network software. As an alternative, you can buy software for less than $1000 that adds TCP/IP and NFS capabilities to MS-DOS-based systems.

PCs and workstations share the same disk- and tape-drive technology. Even power users of PCs regularly equip their machines with 8M bytes of memory. Most 386/486-based mother boards directly support at least 16M bytes of memory, and some new ones can handle 64M bytes. You can argue the performance merits of the RISC (reduced-instruction-set computer) processor technology used in some workstations compared to the 386 and 486 processors. In reality, either choice offers sufficient power to efficiently handle desktop CAE tasks.

It's not clear whether RISC systems will offer substantially better performance than systems based on Intel or Motorola CISC (complex-instruction-set computer) μPs anytime soon. Intel plans to offer a 50-MHz 80486, and has talked in general about 80586, 80686, and 80786 chips. Expect these chips, and new Motorola 680X0 chips, to maintain code compatibility with older chips, and to incorporate some of the performance enhancements used in RISC processors.

From a hardware standpoint, the system bus has cludes support for the widest selection of VGA adapters. All three vendors have been slow to include support for graphics boards based on auxiliary graphics processors such as the TI 34010 and 34020. Each of them plans support in the future, however. In the interim, vendors such as Graphic Software Systems (Beaverton, OR) offer Unix drivers for their intelligent graphics boards.

The three products require varying amounts of memory to install the various options they offer. You can typically install character-based Unix on a system that has as little as four megabytes of main memory. But, as a rule of thumb, you'll need a minimum of eight megabytes to both load a full implementation of Unix that matches the capabilities of a typical workstation and to run graphics-based applications software.

Processor keys portability

Apple Macintosh fans should also rejoice at having a complete Unix package available. The 680X0-based Macintosh products should gain compatibility with applications software that runs on 680X0-based systems from Sun, HP/Apollo, and others. Apple's A/UX 2.0 Unix release is based on Unix System V Release 3.2, as are IBM-compatible packages. The A/UX package includes TCP/IP and NFS as standard features.

Apple offers its 2-user A/UX 2.0 on floppy disk or magnetic tape for \$995; the release on CD-ROM costs \$795. The software costs \$600 if you buy it bundled, preinstalled on the hard disk, with a Macintosh. You can purchase rights to copy AU/X for \$495 per copy.

A \$350 option for AU/X allows you to run X-Windows applications on the Macintosh. Furthermore,

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been the only technical shortcoming for IBM-compatible PCs. The PC/AT bus (also called the industry-standard-architecture (ISA) bus) lacked features such as arbitration and the ability to let multiple masters control the bus. The bus also limited I/O bandwidth to well less than 10M bytes/sec. Yet the PC/AT bus doesn't terribly hamper performance in a single-user multitasking application, such as a CAE workstation. Users that need to maximize I/O performance, however, now have the option of systems based on the Microchannel or EISA (enhanced industry standard architecture) buses—and both of them support multiple bus masters and transfer rates faster than 30M bytes/sec.

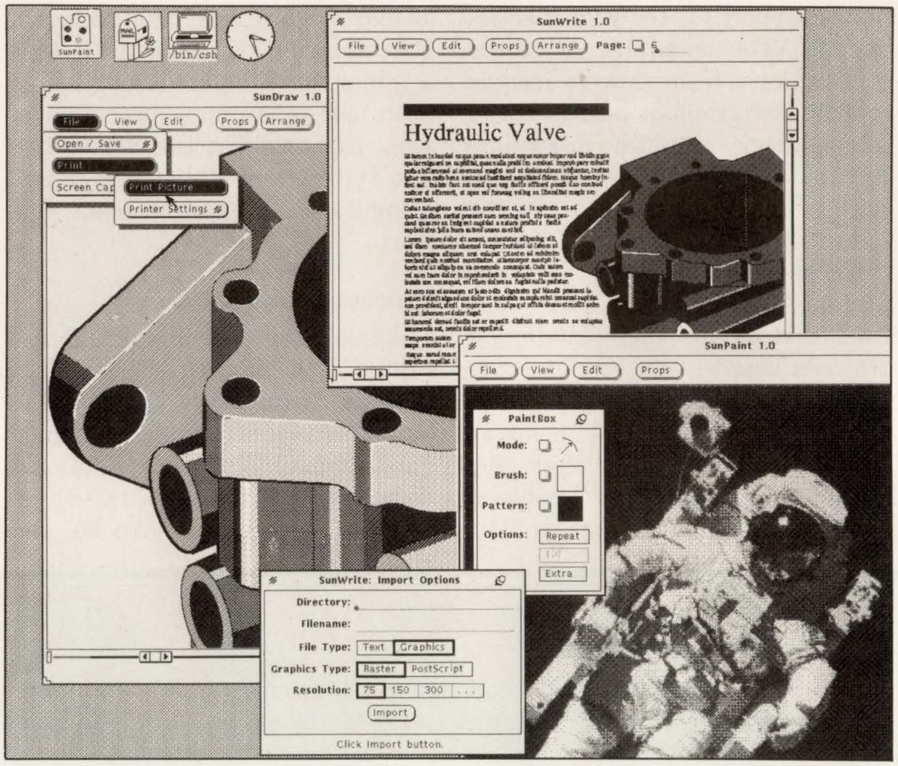
Software is the main technical difference between PCs and workstations. Now, however, you can buy a Unix package for Macintosh and 386/486-based systems that rivals the implementations sold on workstations. Furthermore, standardization efforts in the Unix community should shortly result in a host of hardware-independent Unix-based application packages. The Unix operating-system packages for PCs offer compatibility with PC application software. As a result, users of high-end PCs get the best of both worlds.

A couple of final logistic issues separate PCs from workstations—cost and distribution channels. In general, workstations cost more than PCs. Typically, engineers buy workstations from technical value-added resellers. Most people buy PCs from discount sources. Unix software costs substantially more than MS-DOS or Macintosh software does, but prices should drop as the market for Unix software widens.

Make sure you read between the lines when you see cost comparisons of workstations and PCs. The workstation advocates tend to compare a diskless system with no color graphics to the retail price of a fully configured PC from Compaq or IBM. Likewise, PC vendors will compare the discounted price of a PC with no network hardware to the price a value-added reseller might charge for a decked-out workstation.

A technical value-added reseller would be the likely outlet to purchase a PC or a workstation fully configured with graphics, network capabilities, and CAE software. So compare a CAE value-added reseller's prices of similarly configured 386/486-based systems with name-brand workstations. You will find that the PC typically cost half what a workstation does. And, you always have the option of buying your PC through a mail-order house, or building it yourself.

you can also run some Macintosh operating-system applications in windows under control of X-Windows and Unix. An application must be "32-bit clean" (meet the development specification published by Apple) to run under X-Windows. You can buy Motif or Open look from third parties, and you can buy products from third parties that allow you to run IBM-compatible MS-DOS software on a Macintosh. Conceivably, you could combine a Macintosh application, a text-based Unix application, an X-Windows application, and an MS-DOS application all on one screen using A/UX 2.0.



The Open Look GUI, demonstrated here on a Sun workstation, comes as a standard part of the Unix System V Release 4 package that Intel just began shipping.

Now that System V Release 3.2 has been established as a standard software base, OSF and the combined forces of Unix System Laboratories and Unix International plan to shake things up. Unix System Laboratories shipped source code for Unix System V Release 4 at the end of last year. Release 4 integrates Xenix, BSD, and Sun Microsystems extensions to Unix as standard features. Release 4 also includes NFS, TCP/IP, X-Windows, and Open Look as standard features. Other enhancements include a fast file system and a modular structure that simplifies device-driver development.

Intel has begun shipping an 80X86 shrink-wrapped Release 4 package for $995. Release 4 doesn't require that the vendor add many enhancements, and it essentially offers the same features that Intel, ISC, and SCO have offered in Release 3.2. Therefore, Release 3.2 software should run on Release 4 with few changes.

Intel's Rotow expects Unix users to move to Release 4 immediately. He claims that Release 4 runs faster than Release 3.2 and includes all of the features users need. ISC's Meyer agrees that Release 4 will be important, but that mid-1991 might be a better time for users to consider an upgrade. Meyer claims that ISC's Release 3.2 package already includes file-system enhancements that provide performance that equals Release 4's. He thinks the new release needs time to mature, and that there is no reason for users to upgrade until a significant amount of the applications-software vendors offer Release 4 packages. Dave Sandel, vice president of marketing at Unix International, claims that two out of three of all major open system vendors will be shipping Release 4 by year's end.

According to Watkins, SCO plans to wait before committing to a new software technology base. Watkins states that SCO will offer the products that customers demand, but that customers haven't asked for Release 4 yet. Watkins also plans to keep a close eye on OSF's upcoming operating-system release. He believes that it might become the next industry-standard technology base.

OSF plans to ship the OSF/1 operating system this November. The product uses the Mach kernel developed at Carnegie Mellon University (Pittsburgh, PA) as a base. Mach inherently includes multiprocessor capabilities—a feature Unix System Laboratories and Unix International are busily planning as Unix extensions.

Jack Dwyer, OSF technology manager, claims that the multiprocessing capability played the dominant role in OSF's decision to base its software on Mach rather than IBM's AIX as previously planned. OSF/1 will include compatibility

with System V Release 3.2, Xenix, and BSD extensions. Like Unix System Laboratories, OSF will sell source code only. The company has developed versions of OSF/1 for three reference platforms, one of which is 80386- and 80486-based systems.

A license for OSF/1 costs $50,000. After you buy the initial license, you can buy licenses for additional CPUs for $3000 each. The basic package includes NFS and TCP/IP; you have to license Motif separately. To run Motif, you have to have X-Windows on your system.

A number of major system vendors, including IBM, DEC, and HP/Apollo, plan to make OSF/1 their standard operating system. Therefore the operating system could become the next key industry standard, despite coming to market almost a year after System V Release 4. Intel, ICS, and SCO all have an interest in OSF/1, but none of them have announced products yet. Apple claims only to be watching the industry closely.

Despite changes that are sure to come, you can buy into a stable Unix operating system today. The combination of Windows 3.0 and the Macintosh offer good entry-level platforms for CAE work, and you can expect more and more CAE software vendors to offer such tools. But Unix with Motif, X-Windows, TCP/IP, and NFS, combined with ABI standards, will surely lead personal computers to substantial success in the workstation business. EDN

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Manufacturers of Unix for 80386/486 µPs

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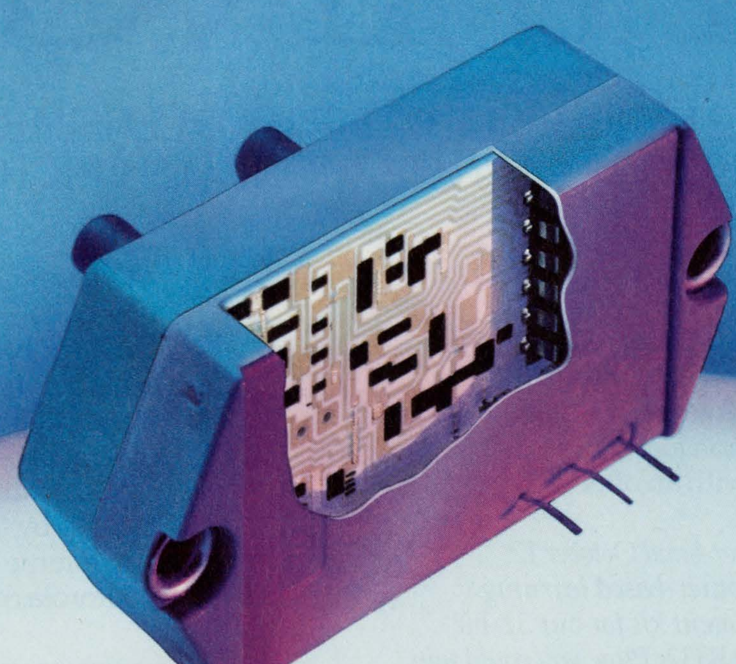

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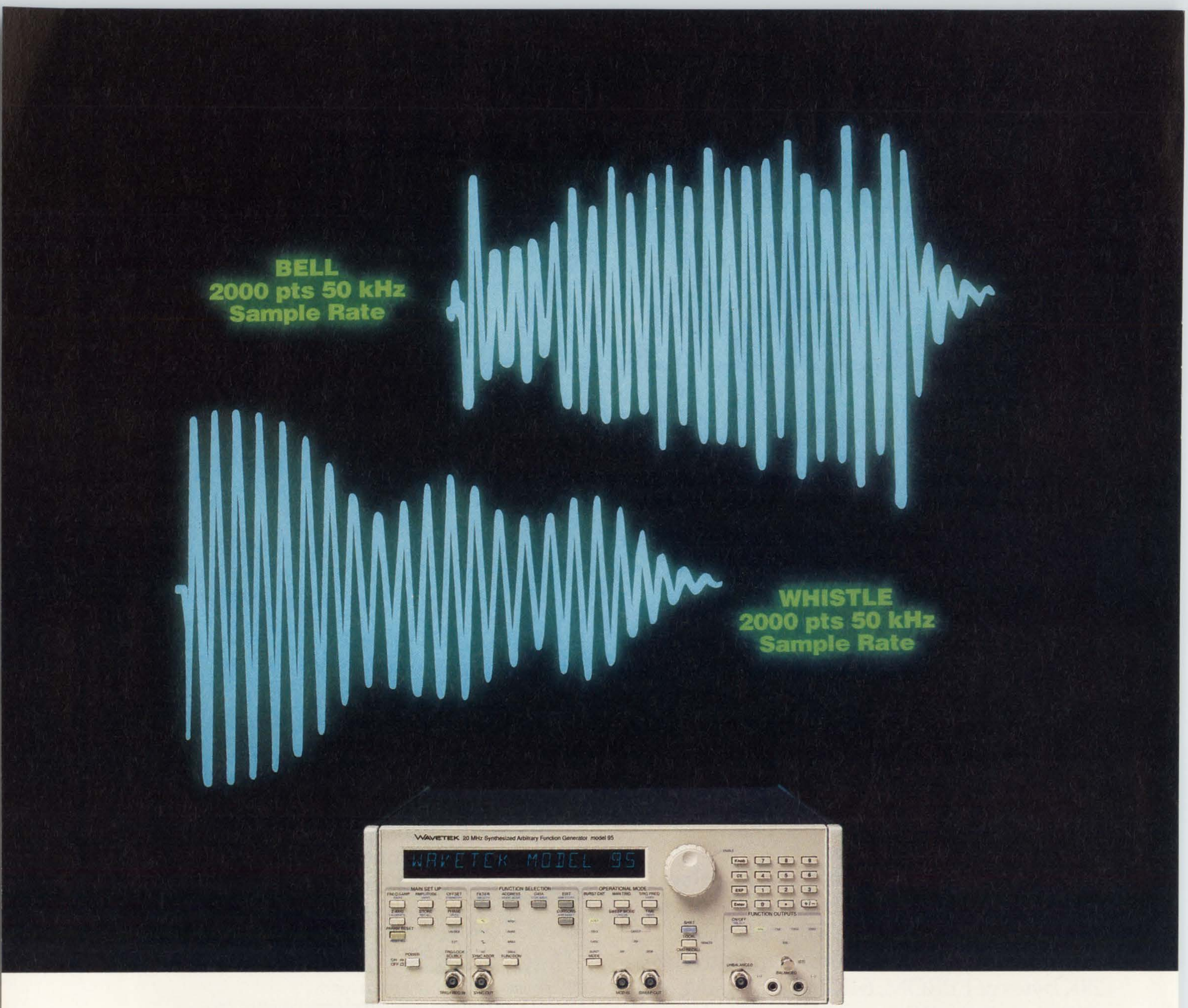

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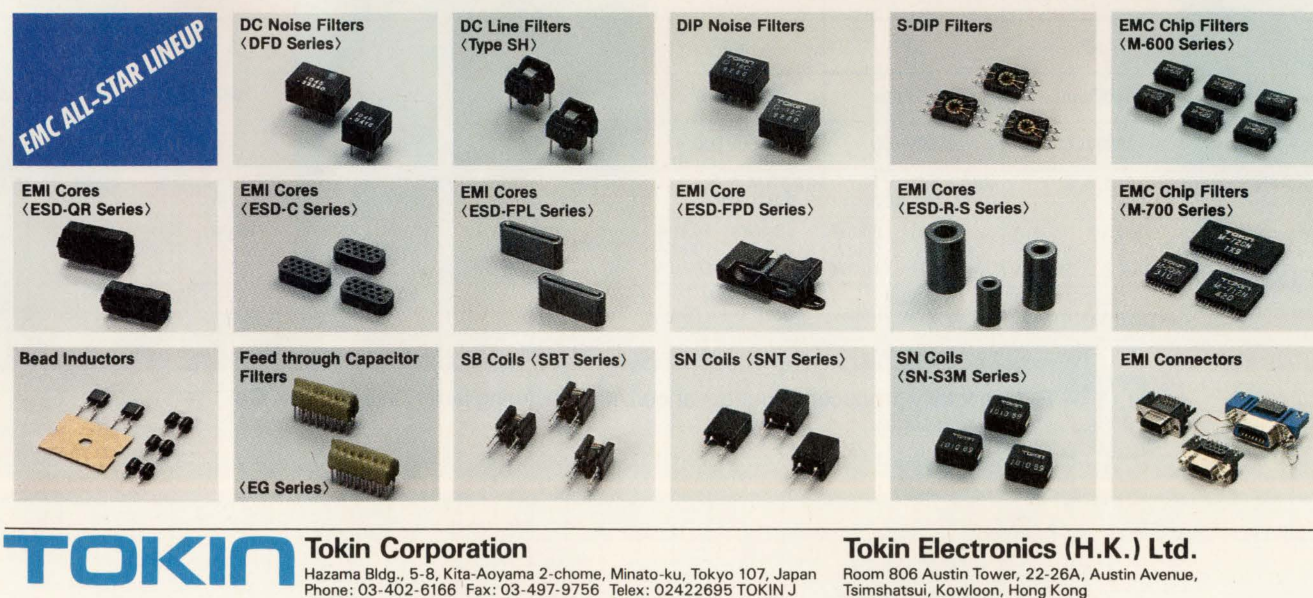

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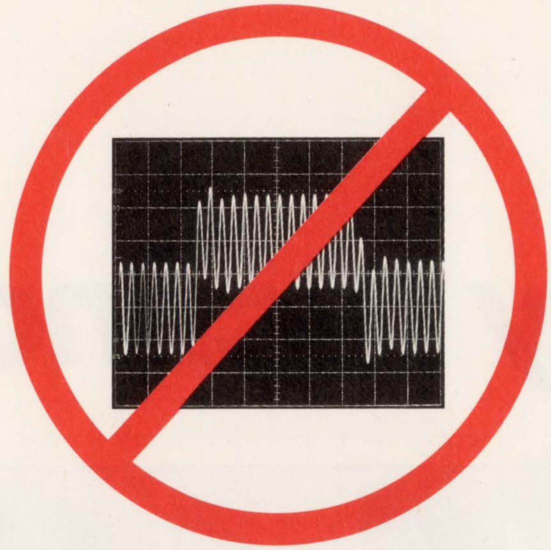

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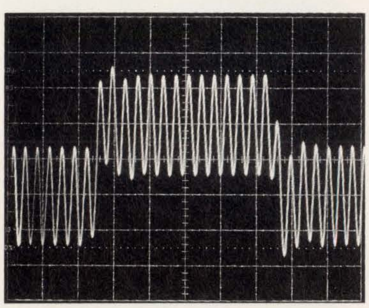

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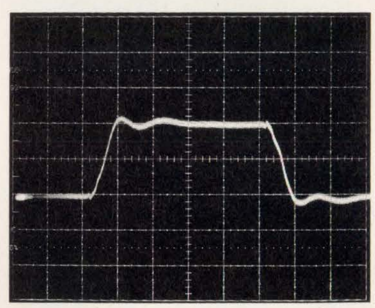

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Benjamin M Brosgol, *Alsys Inc*

The best programming language in the world won't help you design embedded systems if it ignores hardware considerations. Ada's designers walked a tightrope when adding hardware-specific features to the language. On one hand, the designers wanted to maintain the general-purpose nature of the language. On the other, they knew that software must eventually run on real machines, so programmers would need ways to link their code to the hardware. Ada's interrupt and low-level facilities provide that link.

Orderly interactions between cooperating parallel activities are the basis for Ada's tasking model. For two tasks to synchronize or communicate, each must take explicit action by either accepting or calling an entry. In addition, Ada programming style encourages you to use parameter passing rather than shared data for intertask communications to avoid error-prone coupling between modules. Any number of rogue routines, including modules that service interrupts, can easily corrupt shared data.

The interrupt structures built into most computing hardware do little to support good programming style. A hardware interrupt acts like a procedure call issued at some arbitrary (and thus uncontrolled) point in a program. This haphazardness does not match Ada's concept of cooperating parallel activities. Further, hardware devices vary widely in the way they enable and disable interrupts and the way they implement hardware priorities, which encourages and even forces you to create nonportable code. These real-world computing considerations complicate the mating of a general-purpose, high-level language such as Ada to various types of target hardware. The job becomes even more difficult when dealing with the special-purpose hardware used to create embedded systems.

Ada accommodates the interrupt-handling requirements of embedded applications despite the nonportability of embedded systems. The language also resolves the clash between the unstructured nature of interrupt-handling semantics and Ada's more orderly rendezvous model. Yet Ada's direct support of interrupts is minimal by necessity; hardware idiosyncrasies can easily stymie predefined solutions embedded in a programming language. Instead of special-purpose language structures, Ada provides a framework for dealing with interrupts in a high-level manner and relies

Hardware devices vary widely in the way they enable and disable interrupts. This dissimilarity encourages and even forces you to create nonportable code.

on a machine-specific, runtime implementation to efficiently and correctly map high-level code to the underlying hardware.

Ada uses its tasking model to manage the asynchronous nature of hardware interrupts. The interrupting device acts like an external Ada task with a priority higher than any software task. The interrupt instigates a call to an "interrupt entry" in an Ada server task supplied by the programmer. You associate the server task's interrupt entry with the actual hardware interrupt through a machine-dependent feature called an "address representation clause." The server task accepting the interrupt performs the interrupt handling.

An example of such an interrupt handler appears in **Fig 1.** The task SENSOR_INTERRUPT_SERVER designates memory location $A0_{HEX}$ as the address to which control passes when the sensor hardware interrupts. The interrupt signals that new data is available for processing, and it results in an entry call to SENSOR_DATA_AVAILABLE with the data passed as a parameter. If the interrupt processing can keep pace with the interrupts, this scheme works well. However, interrupts may occur too often for the processing to keep up.

The hardware and software design of a system can also cause complications in interrupt handling. For example, in the interrupt structure of Intel's 8086 µP and 8259A interrupt controller, a maskable or nonmaskable interrupt that occurs with interrupts enabled will cause the hardware to perform a CLI (disable interrupts) instruction. The hardware will then call a routine located at an address given in a dispatch table. This routine should perform several functions: re-enable interrupts by executing an STI (enable interrupts)

```
with SYSTEM;

task SENSOR_INTERRUPT_SERVER is

     entry SENSOR_DATA_AVAILABLE ( DATA : SENSOR_DATA_TYPE );

     for SENSOR_DATA_AVAILABLE use at SYSTEM.TO_ADDRESS(16#A0#);

     ...

end SENSOR_INTERRUPT_SERVER;



task body SENSOR_INTERRUPT_SERVER is

     SENSOR_DATA : SENSOR_DATA_TYPE;

begin

     loop

          ...

          accept SENSOR_DATA_AVAILABLE ( DATA : SENSOR_DATA_TYPE ) do

               SENSOR_DATA := DATA;

          end SENSOR_DATA_AVAILABLE;

          -- Send the data to a monitor task:

          SENSOR_DATA_MONITOR.SET(SENSOR_DATA);

          ...

     end loop;

end SENSOR_INTERRUPT_SERVER;
```

Fig 1—Ada's entry calls handle interrupts *just as they handle other Ada tasks. In this example, the low-level interrupt routine passes parameters to the called task through the SENSOR_DATA_AVAILABLE entry.*

instruction as soon as possible; process any data associated with the interrupt; re-enable the interrupt hardware that triggered this routine; and finally return from the low-level interrupt-processing routine. In the context of Ada's interrupt entry model, this sequence of events raises several questions:

- Which code performs the hardware-specific aspects of handling the interrupt—the application program or Ada's runtime executive?
- What priority should the system use to execute the accept statement for an interrupt entry—a hardware priority or the task's software priority? In other words, can the interrupt service routine be pre-empted by another hardware interrupt? By a software task?
- Are there restrictions, for efficiency or semantic reasons, on the kinds of statements that can be executed during interrupt handling?
- What happens if an interrupt occurs but the handler task is not ready to accept the entry call? Is the interrupt lost, or is it somehow queued?
- Can a software task explicitly call an interrupt entry instead of the hardware calling it implicitly?
- How do you avoid the overhead of scheduler intervention and context swapping to get the interrupt handled?

To summarize, do Ada's interrupt structures provide the necessary expressive power to write practical interrupt handlers and can those structures be implemented efficiently? The answer to both questions is yes, because an Ada implementation can separate "immediate processing," which must be carried out at the hardware level, from "deferred processing," which an Ada task can perform.

Call the exec for immediate service

When an interrupt occurs, it causes a call on an assembler routine that is part of the Ada runtime executive. Under Alsys' implementation of Ada, this routine enables higher-level interrupts and then calls a user-provided routine that performs any required immediate processing. The user-provided routine can be written in assembly language or, with some restrictions because of the desire to minimize interrupt latency, in Ada. This routine performs all hardware-level manipulation and is responsible, in particular, for obtaining any data associated with the interrupt, buffering the data, calling an interrupt entry if appropriate, and re-enabling interrupts at the same hardware priority level.

When the immediate-processing routine calls an interrupt entry, the runtime executive checks to see if the called task is ready to accept the call. If it is, the executive pre-empts the currently executing task (unless it is of higher priority), and the called task accepts the call. If the called task is not ready to accept the call, the executive saves any parameters passed by the call in a user-defined buffer. The rendezvous will take place later using normal Ada tasking rules (see Part 1 of this series, *EDN*, September 3, 1990, pg 153). The parameter buffer ensures that interrupts are not lost, because the immediate-processing routine making the call does not suspend. The immediate-processing routine is not an Ada task; it must complete its run if all interrupts are to be acknowledged.

Deferred processing, which is optional, takes place in the task containing the accept statement for the associated interrupt entry. This processing occurs with interrupts enabled, and at a software priority higher than Ada tasks that do not service interrupts. Thus deferred processing can be pre-empted for the immediate processing of another interrupt or to allow deferred processing by another Ada task with a higher task priority. Deferred processing lets you use any Ada statements to service the interrupt's needs because interrupt latency is not a problem while this code is executing.

When you write interrupt service routines in Ada, you must decide whether to perform all interrupt handling in the immediate-processing step or use the 2-step (immediate and deferred processing) approach. You achieve greater efficiency if you perform all the processing in the immediate step because you incur no task-switching overhead. However, you lose generality with this approach because of the restrictions on the Ada statements you can use. Deferred processing through an interrupt entry places no restrictions on the kinds of statements it can execute because interrupt latency is not a problem; the hardware interrupts are always enabled during execution of the deferred-processing task. In addition, a normal Ada task can call an interrupt entry. This feature is useful during program simulation or debugging because you can call the deferred-processing task from another task and simulate the interrupt and the immediate-processing routine's call.

Thus, although interrupt handlers are heavily machine dependent, you can program them in Ada to take advantage of the language's tasking model. **Fig 2**

Text continued on pg 157

```
package SENSOR_PACKAGE is

        type SENSOR_DATA_TYPE is range 0 .. 2 ** 16 - 1;

        for SENSOR_DATA_TYPE'SIZE use 16;

        SENSOR_INTERRUPT : constant := 16#A0#;

        procedure IMMEDIATE_PROCESSING; -- Hardware interrupt handler

        task SENSOR_INTERRUPT_SERVER is

                entry DATA_AVAILABLE (DATA : SENSOR_DATA_TYPE);

                    -- Called from IMMEDIATE_PROCESSING

                for DATA_AVAILABLE use at SENSOR_INTERRUPT;

                entry SHUTDOWN;

        end SENSOR_INTERRUPT_SERVER;

        task SENSOR_DATA_MONITOR is

                entry SET (ITEM : in SENSOR_DATA_TYPE);

                entry GET (ITEM : out SENSOR_DATA_TYPE);

        end SENSOR_DATA_MONITOR;

end SENSOR_PACKAGE;

with INTERRUPT_MANAGER, ARTK; -- Alsys packages
package body SENSOR_PACKAGE is

        PORT_8259 : constant := 16#20#;
        procedure IMMEDIATE_PROCESSING is separate;

        task body SENSOR_DATA_MONITOR is
                SENSOR_DATA : SENSOR_DATA_TYPE;
        begin
                accept SET (ITEM : in SENSOR_DATA_TYPE) do
                        SENSOR_DATA := ITEM;
                end SET;
                loop
                        select
                                accept SET (ITEM : in SENSOR_DATA_TYPE) do
                                        SENSOR_DATA := ITEM;
                                end SET;
                        or
                                accept GET (ITEM : out SENSOR_DATA_TYPE) do
                                        ITEM := SENSOR_DATA;
                                end GET;
                        or
                                terminate;
                        end select;
                end loop;
```

Fig 2—Through immediate and deferred processing, *Ada lets you use low-level code to immediately perform time-critical tasks associated with an interrupt. You can perform any extended processing required by your application in an Ada task that the immediate-processing routine calls.*

```
     end SENSOR_DATA_MONITOR;

     task body SENSOR_INTERRUPT_SERVER is
          SENSOR_DATA : SENSOR_DATA_TYPE;
     begin
          INTERRUPT_MANAGER.INIT_INTERRUPT_MANAGER
               ( NUMBER_OF_BUFFERS  => 1, -- One buffer, 2 bytes
                 MAX_PARAM_AREA_SIZE => 2 );
          INTERRUPT_MANAGER.INSTALL_HANDLER
               ( HANDLER_ADDRESS => IMMEDIATE_PROCESSING'ADDRESS,
                 INT_NUMBER   => SENSOR_INTERRUPT );
          -- Unmask Programmabale Interrupt Controller:
          ARTK.CLI;
          ARTK.OUT_BYTE ( PORT => PORT_8259,
                          DATA => ARTK.IN_BYTE(PORT_8259) and 2#1101_1111# );
                          -- Using IRQ5
          ARTK.STI;

          loop
               select
                    accept DATA_AVAILABLE (DATA : SENSOR_DATA_TYPE) do
                         SENSOR_DATA := DATA;
                    end DATA_AVAILABLE;
               or
                    accept SHUTDOWN;
                    exit;
               end select;
               -- Send the data to a monitor task:
               SENSOR_DATA_MONITOR.SET (SENSOR_DATA);
          end loop;
          INTERRUPT_MANAGER.REMOVE_HANDLER( SENSOR_INTERRUPT);
     end SENSOR_INTERRUPT_SERVER;
end SENSOR_PACKAGE;

with ARTK; -- Alsys Run-Time Kernel

with UNSIGNED;

separate (SENSOR_PACKAGE)

procedure IMMEDIATE_PROCESSING is

-- ---------------------------------------------------------------------------

--  This is the hardware interrupt handler. This procedure receives

-- control with interrupts disabled and must not do any heap allocation, etc.

--  This handler directly calls the server task for each received sensor value.

-- In case the previously read sensor value has not yet been processed, it is

-- overwritten by the current value.

-- ---------------------------------------------------------------------------

     SENSOR_DATA : SENSOR_DATA_TYPE;

     SENSOR_PORT : constant := ... ; -- implementation-dependent

     EOI      : constant := 16#20#;

begin

     -- Read the data from port SENSOR_PORT and pass it to the the server task:

     SENSOR_DATA := ARTK.IN_WORD(SENSOR_PORT);
```

Listing continued

```
        SENSOR_INTERRUPT_SERVER.DATA_AVAILABLE(SENSOR_DATA);

        -- Check if the entry called failed because the data buffer is occupied

        -- If so, overwrite the value in the buffer

        if INTERRUPT_MANAGER.NO_FREE_BUFFERS then

             ... -- Code that overwrites buffer value with SENSOR_DATA

        end if;


        -- Send EOI to interrupt controller:

        ARTK.OUT_BYTE (PORT_8259, EOI);

             -- Assumes the sensor generates an IRQ on master PIC


   end IMMEDIATE_PROCESSING;

   with CALENDAR;
   with SENSOR_PACKAGE; use SENSOR_PACKAGE;
   with TEXT_IO; use TEXT_IO;
   procedure DRIVER is
        task SENSOR_DATA_REPORTER is
             entry SET_PERIOD (INTERVAL   : DURATION;
                               ITERATIONS : INTEGER);
        end SENSOR_DATA_REPORTER;

        task body SENSOR_DATA_REPORTER is
             CURRENT, MAX, MIN   : SENSOR_DATA_TYPE;
             INTERVAL            : DURATION;
             ITERATIONS          : INTEGER;
             NEXT_TIME           : CALENDAR.TIME := CALENDAR.CLOCK;
        begin
             MAX := SENSOR_DATA_TYPE'FIRST;
             MIN := SENSOR_DATA_TYPE'LAST;

             accept SET_PERIOD (INTERVAL   : DURATION;
                                ITERATIONS : INTEGER) do
                  SENSOR_DATA_REPORTER.INTERVAL   := INTERVAL;
                  SENSOR_DATA_REPORTER.ITERATIONS := ITERATIONS;
             end SET_PERIOD;

             for I in 1 .. ITERATIONS loop
                  SENSOR_DATA_MONITOR.GET (CURRENT);
                  if CURRENT < MIN then
                       MIN := CURRENT;
                  end if;
                  if CURRENT > MAX then
                       MAX := CURRENT;
                  end if;
                  PUT_LINE ("Current: " & SENSOR_DATA_TYPE'IMAGE (CURRENT));
                  PUT_LINE ("Max:    " & SENSOR_DATA_TYPE'IMAGE (MAX));
                  PUT_LINE ("Min:    " & SENSOR_DATA_TYPE'IMAGE (MIN));

                  NEXT_TIME := NEXT_TIME + INTERVAL;
                  delay NEXT_TIME - CALENDAR.CLOCK;
             end loop;

        end SENSOR_DATA_REPORTER;

   begin
        SENSOR_DATA_REPORTER.SET_PERIOD (INTERVAL   => 2.0, -- seconds
                                         ITERATIONS => 100.0);

   end DRIVER;
```

Deferred processing occurs with interrupts enabled, and at a software priority higher than Ada tasks that don't service interrupts.

Text continued from pg 153

shows an interrupt handler with both immediate and deferred processing. This handler periodically outputs statistics on sensor data supplied by an external device. Every two seconds, the program outputs the current sensor value together with the maximum and minimum values read since the program started execution. The program performs this processing 100 times. The sensor device signals an interrupt at level $A0_{HEX}$, and the data associated with the device is available as a 16-bit quantity at some port whose location is implementation dependent. The incoming data is sent to a monitor task. The program makes no assumption about the relative frequency of sensor interrupts versus sensor value retrievals. However, if the sensor interrupts arrive faster than the data can be processed, old values are discarded in favor of more recent ones. When the last statistic has been dispatched, the system shuts down by terminating all of its tasks.

A block diagram of this system's tasking structure appears in **Fig 3.** SENSOR_PACKAGE encapsulates the SENSOR_INTERRUPT_SERVER and SENSOR_DATA_MONITOR tasks as well as the IMMEDIATE_PROCESSING procedure. DRIVER is the main procedure for the program; it contains the SENSOR_DATA_REPORTER task that periodically obtains sensor data values and outputs the statistics.

This program uses several auxiliary packages. *TEXT_IO* and *CALENDAR* are standard Ada packages. *TEXT_IO* supplies subprograms for performing simple character I/O. *CALENDAR* provides the private type *TIME*, the *CLOCK* function for delivering the current *TIME* value, and several subprograms for manipulating *TIME* values such as adding a *TIME* and a *DURATION* to compute another *TIME*.

In addition to these predefined packages, the program employs several packages specific to Alsys' Ada implementation. *UNSIGNED* declares operations for unsigned integer arithmetic and types such as the 8-bit *BYTE* and 16-bit *WORD*. *ARTK* provides access to Alsys' runtime kernel services. For example, *IN_WORD* reads a word from a specified port address and *OUT_BYTE* outputs a byte. *INTERRUPT_MANAGER* is an Alsys package that lets you install user-supplied interrupt handlers.

Several subprograms defined in *INTERRUPT_MANAGER* are called from the body of SENSOR_INTERRUPT_MANAGER. *INIT_INTERRUPT_MANAGER* establishes a buffer area for the parameters that need to be queued for later access to the interrupt entry. *INSTALL_HANDLER* arranges for the immediate-processing routine supplied by the user to be called during the hardware-level interrupt handling. *REMOVE_HANDLER* disables and removes the immediate-processing routine that handles the given interrupt.

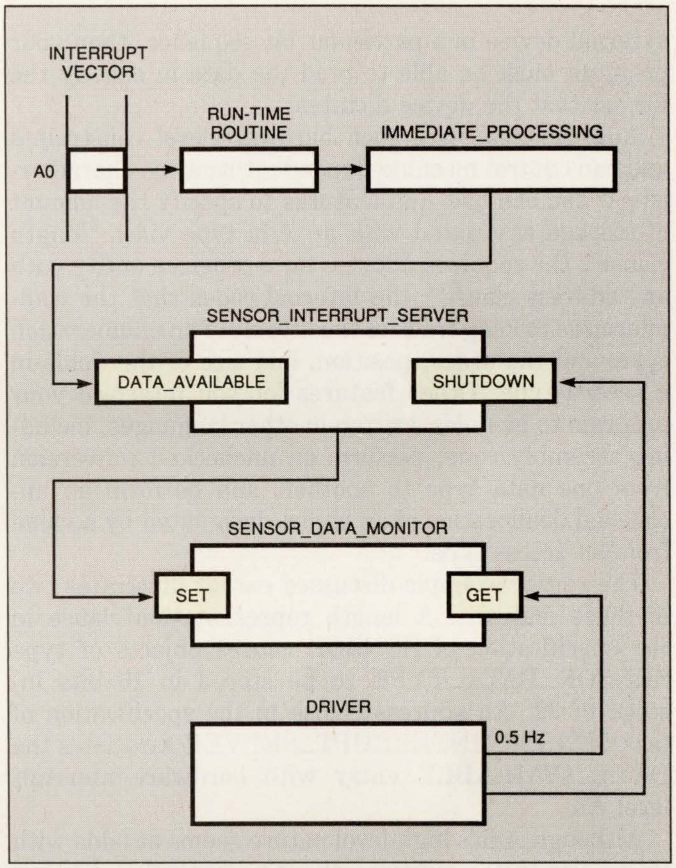


Fig 3—Tasks in an Ada program cooperate *to perform periodic real-time data acquisition. By separating the low-level interrupt-driven processing from the higher-level logic, you can simplify your program's structure and make it easier to maintain.*

Low-level features link to hardware

In addition to interrupt support, Ada provides features that map language structures to the hardware these structures represent. In general, you need not be concerned with an Ada compiler's particular mapping choices; good compilers perform optimizations that produce excellent runtime efficiency. In some situations, however, you cannot leave these decisions to the compiler. For example, if data arrives from an

Although interrupt handlers are heavily machine dependent, you can program them in Ada to take advantage of the language's tasking model.

external device in a particular bit sequence, then your program must be able to read the data in exactly the format that the device dictates.

Ada can deal with such hardware-level constraints and can control machine-dependent runtime characteristics. You can use Ada features to specify the amount of storage associated with an Ada type via a "length clause"; the required address for a program entity with an "address clause"; the internal codes that the compiler uses to keep track of the literals of an enumeration type; and the order, position, and size of the fields in a record type. Other features let you interface your program to modules written in other languages, including assembly code, perform an unchecked conversion from one data type to another, and perform an unchecked deallocation of an object designated by a value from an access type.

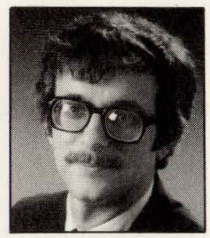
The sensor example discussed earlier illustrates two of these features. A length representation clause in the specification of SENSOR causes objects of type SENSOR_DATA_TYPE to be stored in 16 bits instead of 32. An address clause in the specification of task SENSOR_INTERRUPT_SERVER associates the DATA_AVAILABLE entry with hardware-interrupt level A0.

Although Ada's high-level nature seems at odds with these low-level facilities, the two actually combine rather smoothly. Ada separates the logical, high-level characteristics of a program entity from the lower-level, representational details. In any Ada program, you must specify at least the high-level, logical characteristics such as a record's type declaration. As an option, you can also specify representational details such as the layout of the record's fields. If you don't provide such information, the compiler chooses a representation for you. If you do provide representational details, they will override the compiler's default choices.

And you don't have to worry that programmers who subsequently modify, maintain, or reuse your program will miss any low-level customizing you have done. You must use instantiations of separately compiled, predefined generic units to obtain shortcuts such as unchecked type conversions and unchecked deallocations. This use of generics forces any program unit that needs these services to incorporate a *with* clause at its beginning that names the required generic unit(s). This rule exposes potentially dangerous programming practices because anyone reading the unit's source code will immediately see the situation.

Ada's low-level features for real-time programs minimize interference with Ada's strong typing model. Their use is consistent with software engineering principles such as information hiding and modular programming. Using the language-defined features and the mechanisms offered by compiler vendors, programmers are developing more of their real-time systems in Ada. **EDN**

Author's biography



Benjamin Brosgol is vice president and technical director at Alsys Inc (Burlington, MA). He is in charge of the company's Ada training and consulting, has helped develop Ada compilers and computer-based training products, and is chairman of the Commercial Ada Users Working Group of the SIGAda professional society. Benjamin holds an MS and PhD in Applied Mathematics from Harvard University in Cambridge, MA, and is a member of both the IEEE and the Association for Computing Machinery.

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WHAT'S COMING IN EDN

EDN Magazine's October 1, 1990, issue will feature a staff-written Special Report on Futurebus+. Our designers' guide to real-time Ada will conclude with Part 3. EDN's real-time programming series will continue with Part 2, which will discuss operating-system concepts and services. Staff-written Technology Updates will cover optoelectronic sensors, 32-bit development tools, and PC chip sets.

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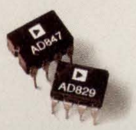

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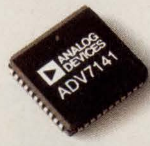

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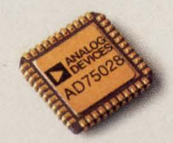

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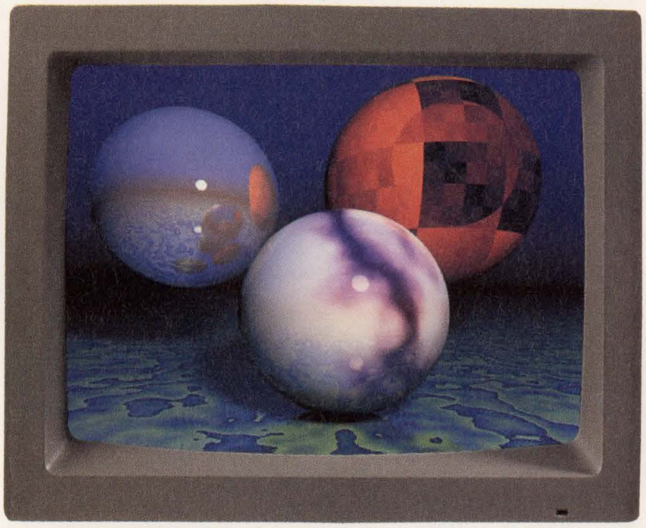

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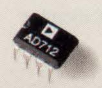

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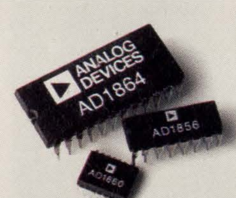

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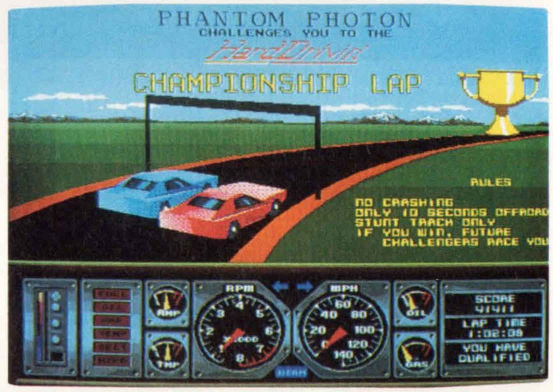

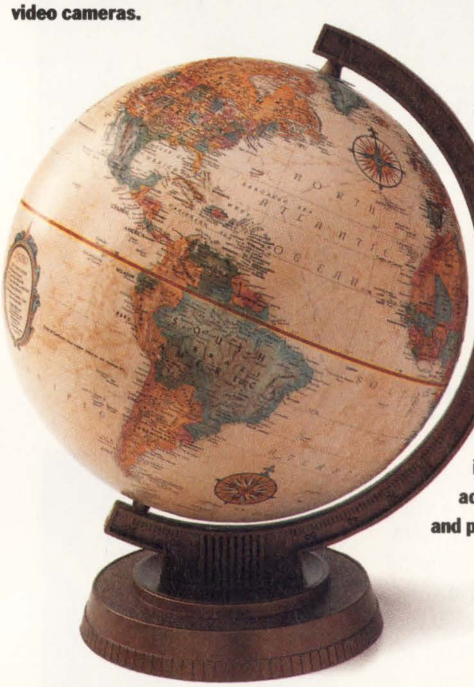

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CIRCLE NO. 69

Current-feedback amps enhance active-filter speed and performance

In the past, off-the-shelf high-frequency active filters were rarely available because high-frequency, high-performance voltage-feedback amplifiers were simply too expensive. Active filters built around current-feedback amplifiers offer designers high performance without many of the disadvantages associated with passive filters.

Doug Smith, *Burr-Brown Corp*

Analog designers have historically relied on passive filters for applications with frequencies greater than 1 MHz. Until recently, designing viable active filters with cutoff frequencies at 1 MHz or greater was difficult because voltage-feedback amplifiers with sufficient gain-bandwidth products and short propagation delays were simply too expensive. The emergence of current-feedback, or transimpedance, amplifiers has significantly changed this picture. With these amplifiers and a conscientious design and pc-board layout, you can design active filters that operate at high frequencies. Active-filter applications are no longer restricted to the audio frequency range.

Active RC filters have many advantages over passive filters, and many of these advantages become increasingly important as the frequency increases. For example, there is no insertion-loss penalty, and you can even have power gain if needed. A doubly terminated passive filter would decrease the signal by at least 50%. The elimination of inductors is the biggest advantage offered by active filters. This advantage doesn't involve size considerations alone.

Passive inductors are only linear for low power levels, much like transistors with no negative feedback. As you pump more current through the inductor, the magnetic core material begins to saturate and the inductor generates its own harmonic-distortion terms. The filter's transfer response will not necessarily suppress these signals. In an active RC filter, the amplifier quality and the sophistication of the design set the dynamic range. Theoretically, designers have a good deal of control over both of these parameters.

As a case study, consider three situations—a low-pass antialiasing filter, a bandpass filter, and a high-Q notch filter—in which active filters that incorporate current-feedback amplifiers provide a viable alternative to passive filters. All three filters will be designed around the Burr-Brown OPA603. You could implement the three designs using carefully selected, video-speed conventional op amps. However, current-feedback amplifiers more readily satisfy the low transit time and large bandwidth at high gain requirements for the example circuits. Let's start with the design of an antialiasing filter to drive the input of an ADC603—a 12-bit, 10-MHz A/D converter.

Many of the advantages of active RC filters become increasingly important as the frequency increases.

When dealing with A/D converters in filter work, the Nyquist theorem states that if any converter input harmonic frequency is greater than half the sampling rate, those frequencies must alias, or fold back, into the passband. Normally, this condition is not desirable. To skirt the issue, you must suppress any input frequencies that exceed the Nyquist rate before the converter sees them. The result of this maneuver is that the required attenuation becomes a function of converter resolution. It's also important for the filter to roll off as fast as possible. An elliptic response is the best choice because the addition of transmission zeros in the stopband creates the sharpest roll-off theoretically possible for a particular number of poles without having to rely on mutual inductance.

The first step in designing the filter is calculating the attenuation requirements. You can do so by estimating the theoretical signal-to-noise ratio (SNR) using the expression

$$SNR = 6.02N + 1.8 \text{ dB},$$

where N is the number of bits. For the ADC603, the expression yields

$$SNR = 6.02 \times 12 + 1.8 = 74.04 \text{ dB}.$$

Making the case for current feedback

Don't get the idea that something is inherently wrong with voltage feedback, even at high speed. In fact, voltage-feedback amplifiers generally have a lower noise-floor specification than do current-feedback amplifiers. However, when comparing voltage- and current-feedback amplifiers, you must take the application into consideration. Current-feedback, or transimpedance, amplifiers have some distinct performance advantages as waveform speed gets higher and higher. These advantages can translate into higher-performance active filters.

The most striking difference between voltage-feedback and transimpedance op amps is that with a fixed-feedback resistor, the current-feedback amplifier has very low gain-bandwidth tradeoff. A transimpedance amplifier maintains its bandwidth at high gain settings—an advantage in active-filter topologies because a large gain is necessary to minimize sensitivity.

In addition, transimpedance amplifiers have very high slew rates compared with those of conventional voltage op amps. A typical slew rate for a video-speed voltage-feedback amplifier is in the 200 to 300V/µsec range; a comparable current-feedback amplifier might slew as fast as 2500V/µsec. This slew-rate disparity is simple to explain. In a conventional amplifier, the slew rate is the ratio of the bias current flowing through the slewing node to the capacitance that can be referred back to that node. In a transimpedance amplifier, the feedback current mirrors and adds to the bias current flowing through the slew-rate-limiting node. Because more current is available to charge the capacitance, the slew rate increases. The feedback current is proportional to V^{OUT}, which is proportional to V^{IN}. So the harder you drive a current-feedback amplifier, the faster it slews. In practice, this fact effectively eliminates slew rate as a limiting factor in high-speed, active-filter design.

One final factor favors the transimpedance amplifier—settling time. Designers often choose a filter's transfer function for best time-domain response. Therefore, ensuring that the amplifier settles to the required level substantially faster than the filter has to settle is crucial.

High-speed amplifiers are complicated devices and acceptable ac response does not necessarily ensure an acceptable settling time. Many conventional voltage-feedback op amps use internal pole-zero cancellation to increase their bandwidths. Analysis shows that a small mismatch in the pole-zero cancellation has a negligible effect on frequency response, but the scheme can dramatically boost settling time.

Transimpedance amplifiers have settling-time problems, too. Although transimpedance amplifiers settle to 0.1% (10 bits) or 0.02% (12 bits) in as little as 15 nsec, the settling time to 0.01% can be relatively long. The same current flow that increases the slew rate of a transimpedance amplifier also upsets the amplifier's bias point slightly, and a finite amount of time is required for the bias point to return to equilibrium. This effect is small, but it can often extend the 0.01% settling time to several microseconds.

The calculation shows that the guaranteed stopband attenuation must be greater than 74 dB. A search of standard design tables shows that a fifth-order elliptic lowpass response is a reasonable compromise between the transition width and the filter order. The general transfer function for this filter is

$$T(s)=\left(H_a\,\frac{s^2+b_{0a}}{s^2+a_{1a}s+a_{0a}}\right)\left(H_a\,\frac{s^2+b_{0b}}{s^2+a_{1b}s+a_{0b}}\right)\left(\frac{a_0}{s+a_0}\right).$$

You can now form the filter by cascading two second-order sections and one first-order section **(Fig 1b)**. The essential equations **(Ref 1)** for the second-order sections are

$$T(s)=H(s^2+b_0)/s^2+a_1s+a_0$$
$$p=1/\sqrt{b_0}$$
$$q=((b_0/a_0)-1)/2\sqrt{b_0}$$
$$K=2+(1/2)((b_0/a_0)-1)-\ (a_1\sqrt{b_0}/a_0).$$

The essential equations for the first-order section are

$$T(s)=a_0/s+a_0$$
$$a_0=1/RC.$$

The task is to design a fifth order elliptic antialiasing filter **(Fig 1a)** with a guaranteed stopband attenuation of 75 dB and no more than 3 dB of passband ripple. In addition, the maximum attenuation should begin at 5 MHz—half the sampling rate.

The transfer coefficients **(Ref 1)** for this case are

$$a_{1a}=0.096035$$
$$a_{0a}=-0.945044$$
$$b_{0a}=10.47185$$
$$a_{1b}=0.285481$$
$$a_{0b}=0.413907$$
$$b_{0b}=4.328514$$
$$a_{0c}=0.191095.$$

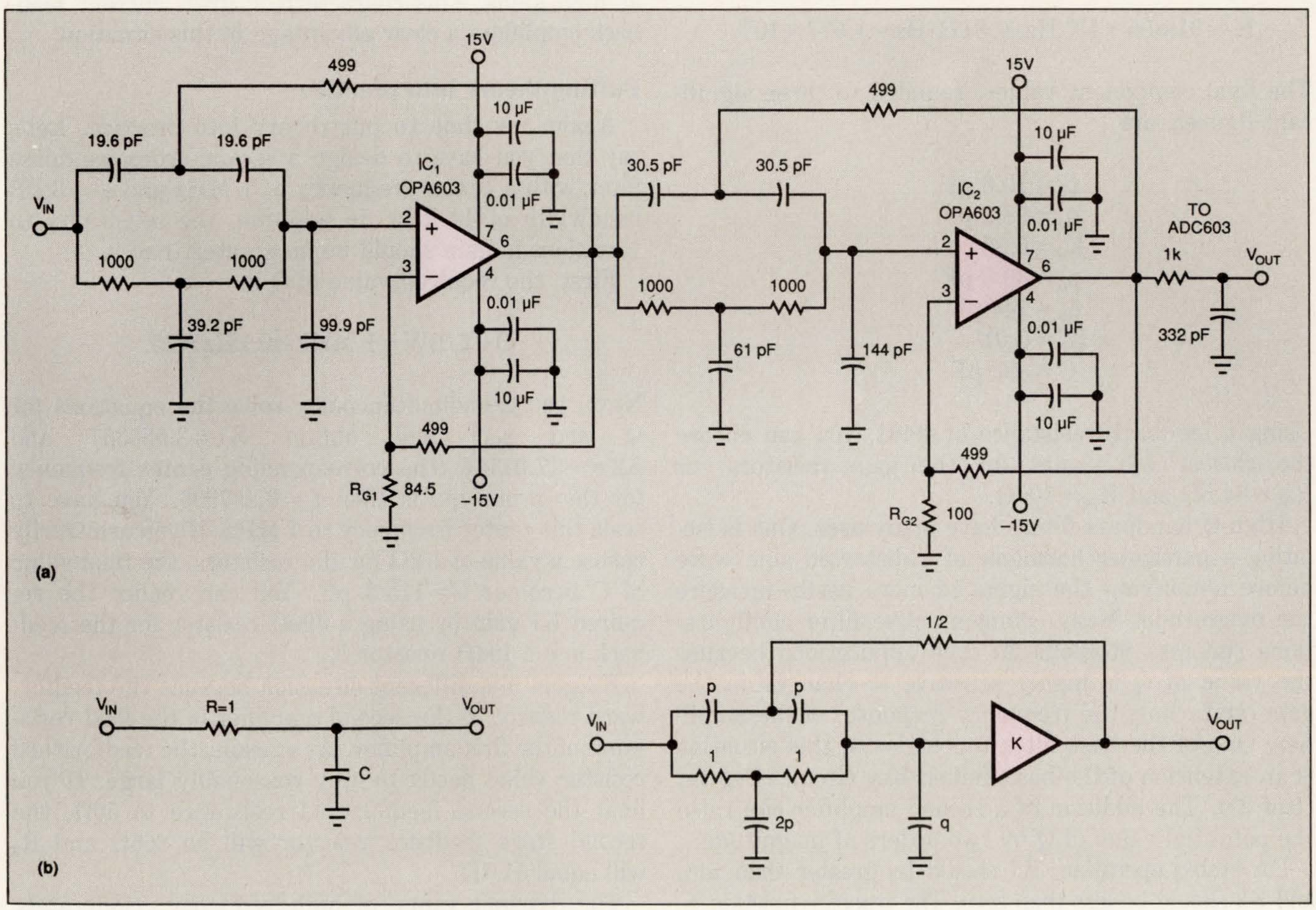


Fig 1—You need an antialiasing lowpass filter *when you're driving an A/D converter. A fifth-order elliptic design **(a)** proves to be the best choice in such an application. You can use two second-order sections and one first-order section **(b)** to form the necessary filter.*

Transimpedance amplifiers maintain their bandwidth at high gains—a definite advantage in bandpass-filter designs.

The corresponding component values are

$$p_a = 0.309021$$
$$q_a = 1.557592$$
$$K_a = 6.875982$$
$$p_b = 0.480652$$
$$q_b = 2.272930$$
$$K_b = 6.011362$$
$$R = 1$$
$$C = 5.232999.$$

This filter prototype has an f_3 bandwidth of 0.15912 (1 rad/sec), and its maximum attenuation begins at $f_{STOPBAND} = 0.3171$. In this case, you have to scale the frequency to $f_{STOPBAND}$ rather than f_3. In addition, you can arbitrarily scale the impedance to 1 kΩ. Multiply each resistor by this impedance value; divide every capacitor value (p, q, and C) by the frequency-impedance scaling factor, K_f :

$$K_f = 91k(95 \times 10^6 \text{ Hz})/0.3171 \text{ Hz} = 1.577 \times 10^{10}.$$

The final component values, rounded to three significant figures, are

$$p_a = 19.6 \text{ pF}$$
$$q_a = 98.8 \text{ pF}$$
$$K_a = 6.88$$
$$p_b = 30.5 \text{ pF}$$
$$q_b = 144 \text{ pF}$$
$$K_b = 6.01$$
$$C = 332 \text{ pF}.$$

Using a feedback resistance of 499Ω, you can choose the closest 1% values for the gain resistors, or $R_{G1} = 84.5\Omega$ and $R_{G2} = 100\Omega$.

High-Q bandpass filters have many uses. One is isolating a particular harmonic of a distorted sine wave before amplifying the signal to more easily measure the magnitude. Many common active filter configurations run into problems in such applications because the value of Q is highly sensitive to changes in the gain (and, thus, the frequency response) of the amplifier. One of the best filter topologies in this situation is an extension of the basic Sallen-Key circuit **(Fig 2a, (Ref 2))**. The addition of a second amplifier can raise the potential value of Q by two orders of magnitude.

For stable operation, K1 should be greater than zero and K2 should be less than zero. The transfer function is

$$T(s) = K1 \times K2s/(1 - K1K2)s^2 + (4 - K1)s + 2.$$

From this expression, you can determine that

$$Q = \sqrt{2(1 - K1K2)/4 - K1}$$
$$\omega_o = \sqrt{2/(1 - K1K2)}.$$

The sensitivities of most concern involve the variations of Q when the gain of either amplifier changes. Analysis shows that

$$s_{K1}{}^Q = K1(1 - 4K2)/(4 - K1)(1 - K1K2)$$
$$s_{K2}{}^Q = K1K2/1 - K1K2.$$

You can neglect $s_{K2}{}^Q$ because it is approximately equal to 1 and is not a serious limitation. Although it's probably not obvious, there's a tradeoff between K2 and $s_{K1}{}^Q$. The higher the gain of K2, the lower the value of $s_{K1}{}^Q$. In a voltage type op amp, higher gain inherently means lower bandwidth. However, a transimpedance amplifier has the ability to maintain its bandwidth at high gains. This characteristic gives current feedback amplifiers a clear advantage in this situation.

Putting theory into practice

Again, it's time to put theory into practice. Let's say that you have to design a second-order bandpass filter with a center frequency of 1 MHz and a −3 dB bandwidth of 40 kHz. In addition, the sensitivity to variations in gain should be no greater than 9.

First, the required value of Q is

$$Q - f_0/BW = 1 \text{ MHZ}/40 \text{ kHz} = 25.$$

Next, you can simultaneously solve the equations for Q and $s_{K1}{}^Q$ and obtain $K1 = 3.556357$ and $K2 = -17.01347$. The corresponding center frequency for this prototype is then $f_0 = 0.287996$. You have to scale this center frequency to 1 MHz. If you arbitrarily choose a value of 1 kΩ for the resistors, the final value of C becomes C = 115.3 pF. You can realize the required K1 gain by using a 499Ω resistor for the feedback and a 196Ω resistor R_1.

K2 gain is a different situation because the feedforward resistor of the second amplifier is the load resistance of the first amplifier. As a result, the feedforward resistor value needs to stay reasonably large. If you limit the second feedforward resistance to 50Ω, the second stage feedback resistor will be 866Ω and R_2 will equal 51.1Ω.

The dynamic range of high-frequency, moderately priced spectrum analyzers is often less than 80 dB. However, you can effectively increase the measurement range by suppressing the fundamental frequency of the input signal by a known amount without affecting the rest of the frequency spectrum. This application doesn't require a high-order, band-reject filter—a low-order, high-Q notch filter will work quite well.

The classic twin-T network (**Fig 3a**) is a promising candidate for the job. The transfer function of this network is

$$T(s) = s^2 + \omega_0^2/s^2 + 4\omega_0 s + \omega_0^2,$$

and the attenuation at any bandwidth equals

$$A_{dB} + 10 \cdot \log(1 + (4f_0/BW_{x\ dB})^2).$$

This circuit has two drawbacks—it is somewhat sensitive to passive-component tolerances, and it has an intrinsic Q value of 0.25. The first drawback creates no problem but the second drawback must be overcome. You can substantially increase circuit Q value by adding a second amplifier to the network (**Ref 3**). The new transfer function is now

$$T(s) + s^2 + \omega_0^2/s^2 + 4\omega_0(1 - K)s + \omega_0^2,$$

and the Q value is now a function of K:

$$Q = 1/4(1 - K).$$

As K approaches 1 from below, Q increases in an unlimited fashion. If K is greater than 1, however, the circuit is unstable. Although wide bandwidth at high gain is not as important here as it was in **Fig 2**'s example, the comparatively lower transit time of a current-feedback amplifier should yield superior performance in this application.

A specific example will prove the point. The task is to design a 1.5 MHz notch filter that has a −3 dB bandwidth of 225 kHz. The first step is to calculate Q using the expression

$$Q = f_0/BW_{-3\ dB} = 1.5\ \text{MHz}/225\ \text{kHz} = 6.66.$$

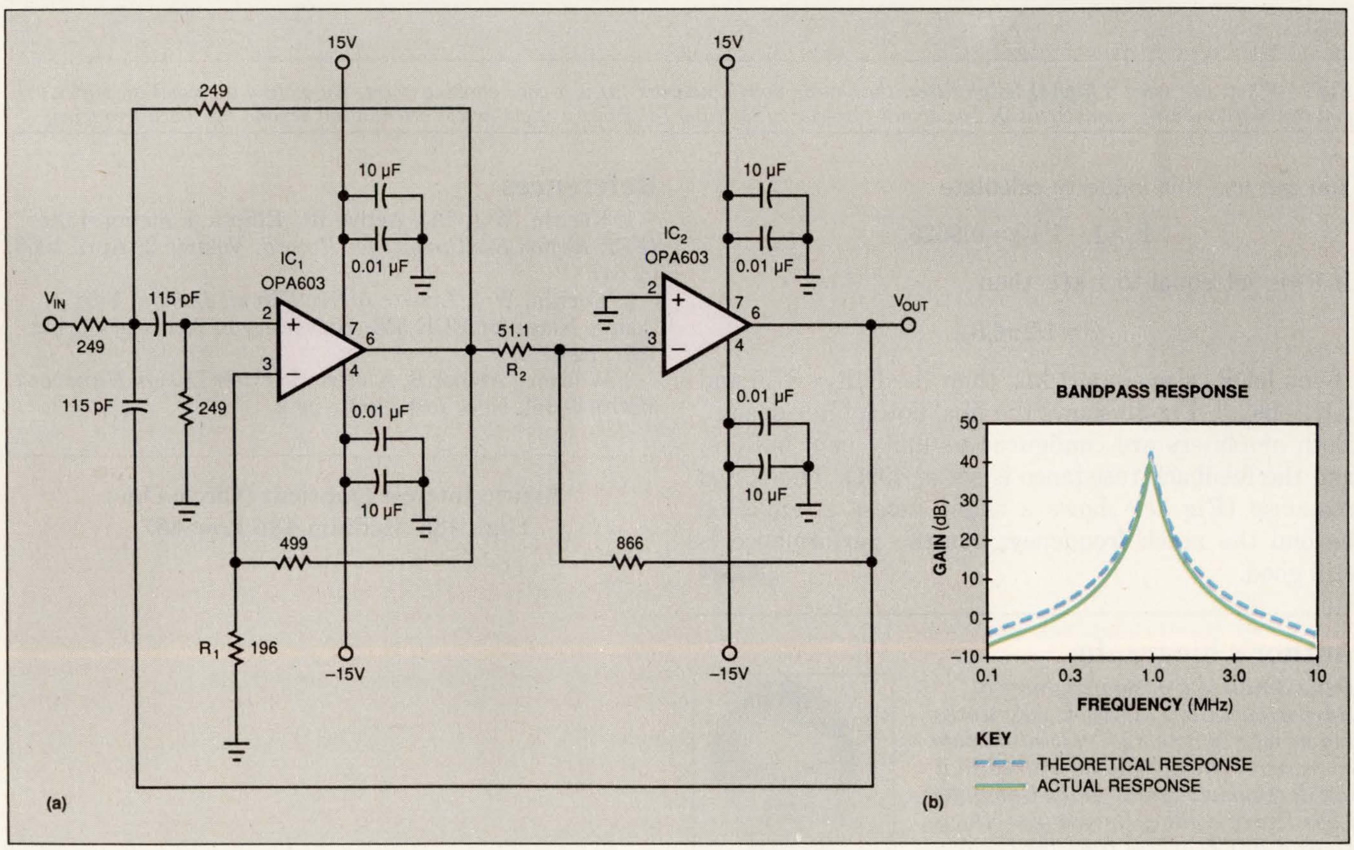


Fig 2—To develop high-Q bandpass filters, *you can add a second amplifier to the basic KRC circuit* ***(a)*** *to raise the potential Q by orders of magnitude. The actual bandpass response of the filter is very close to the theoretical value* ***(b)****, although the response shows a slightly lower gain.*

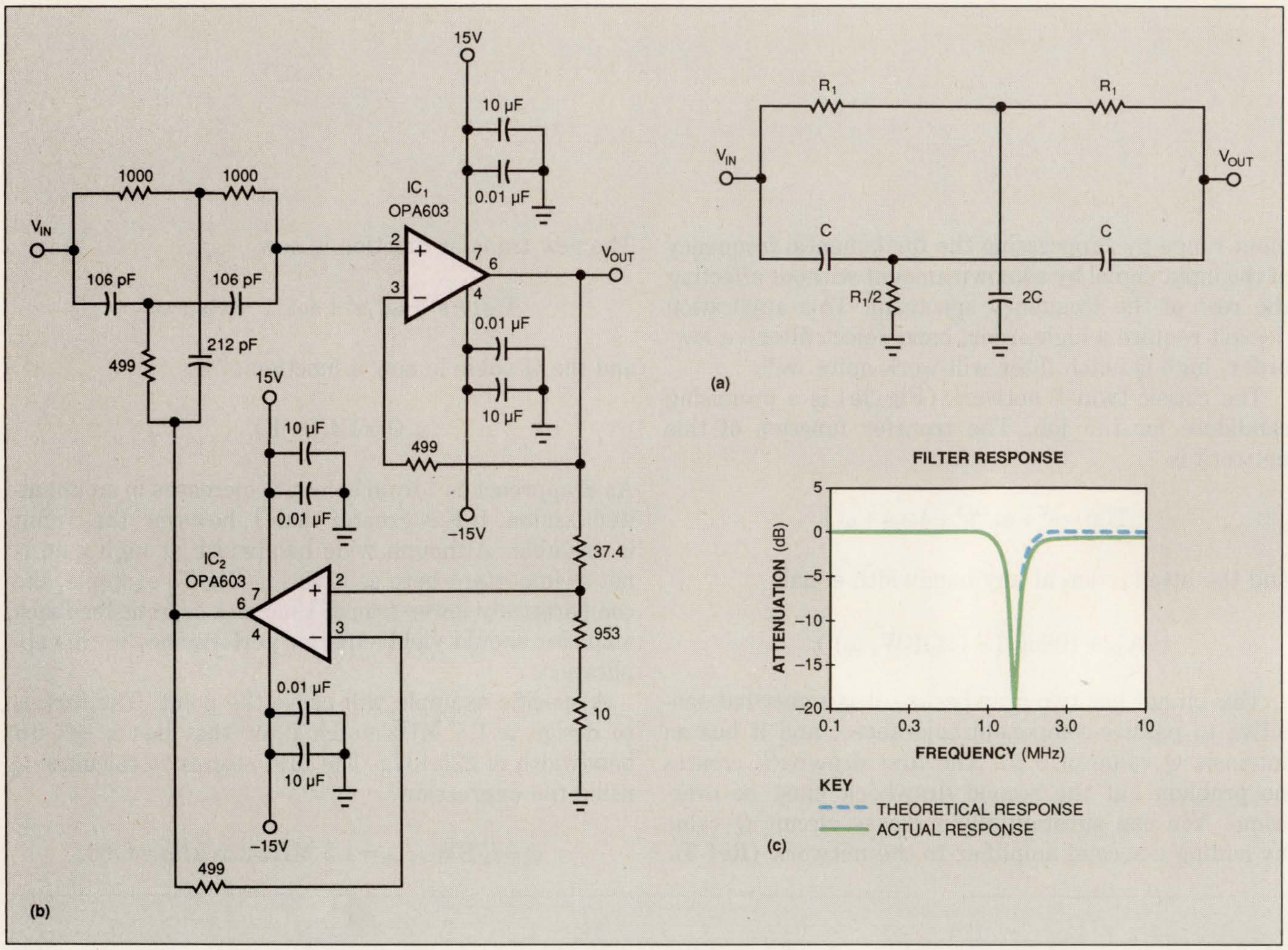


Fig 3—When you need a high-Q notch filter, *the classic twin-T network* ***(a)*** *is a good starting point. By adding a second amplifier* ***(b)****, you can substantially raise circuit Q. The actual response of the filter* ***(c)*** *shows a slight excess attenuation beyond the notch frequency.*

You can use this value to calculate

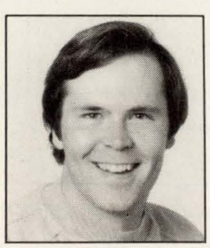
$$K = 1 - 1/4Q = 0.9625.$$

If R_1 is set equal to 1 kΩ, then

$$C = 1/2\pi f_0 R_1.$$

If you let R_2 also equal 1 kΩ, then $(1-K)R_2 = 37.5$ and $KR_2 = 962.5$. **Fig 3b** shows the final notch filter design. Both amplifiers are configured as unity gain buffers, and the feedback resistance is set at 499Ω. The actual response **(Fig 3c)** shows a slight excess attenuation beyond the notch frequency, but the performance is still good. EDN

Author's biography



Doug Smith is a design engineer at Burr-Brown Corp (Tucson, AZ) working primarily with high-resolution data converters. Previously, he worked in a test development group at the Computer Labs Div of Analog Devices Inc. Doug holds a BSEE degree from the University of Arizona and is a member of Tau Beta Pi and Eta Kappa Nu. He enjoys mathematics, optics, and guitar playing.

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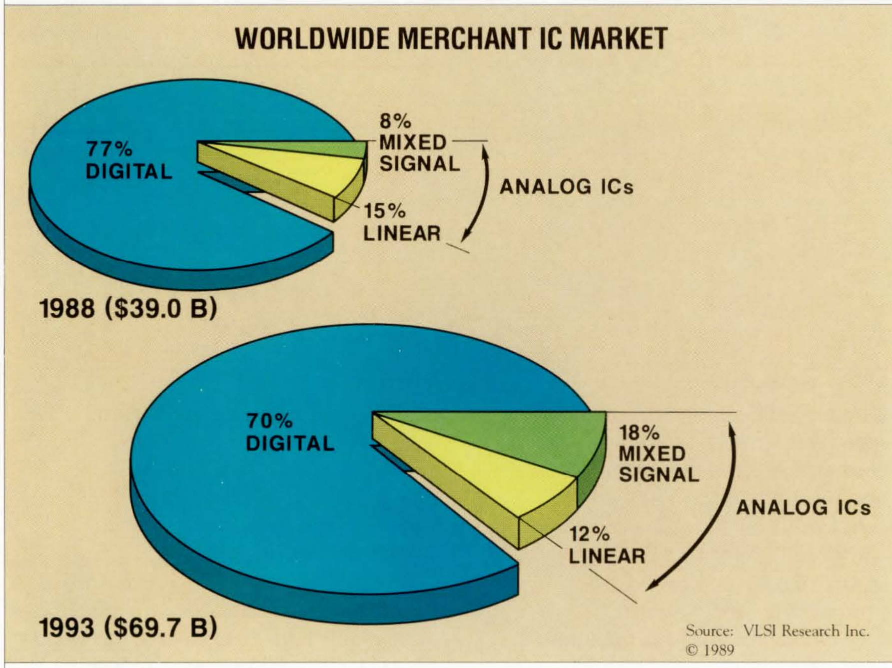

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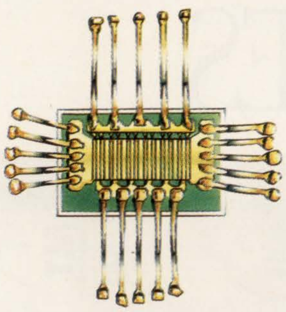

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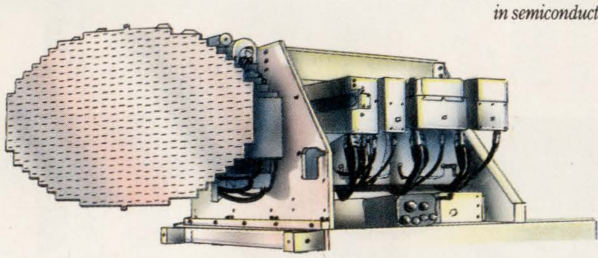

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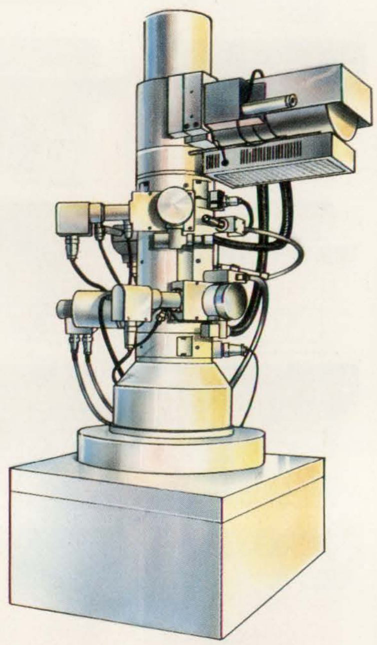

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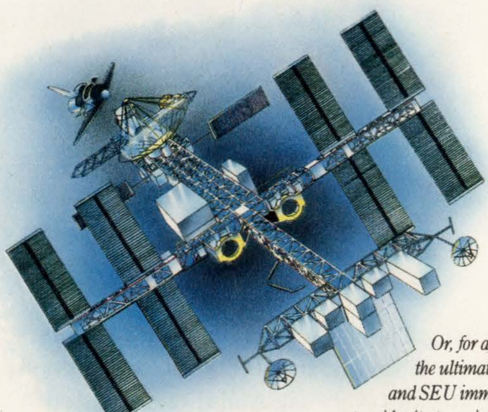

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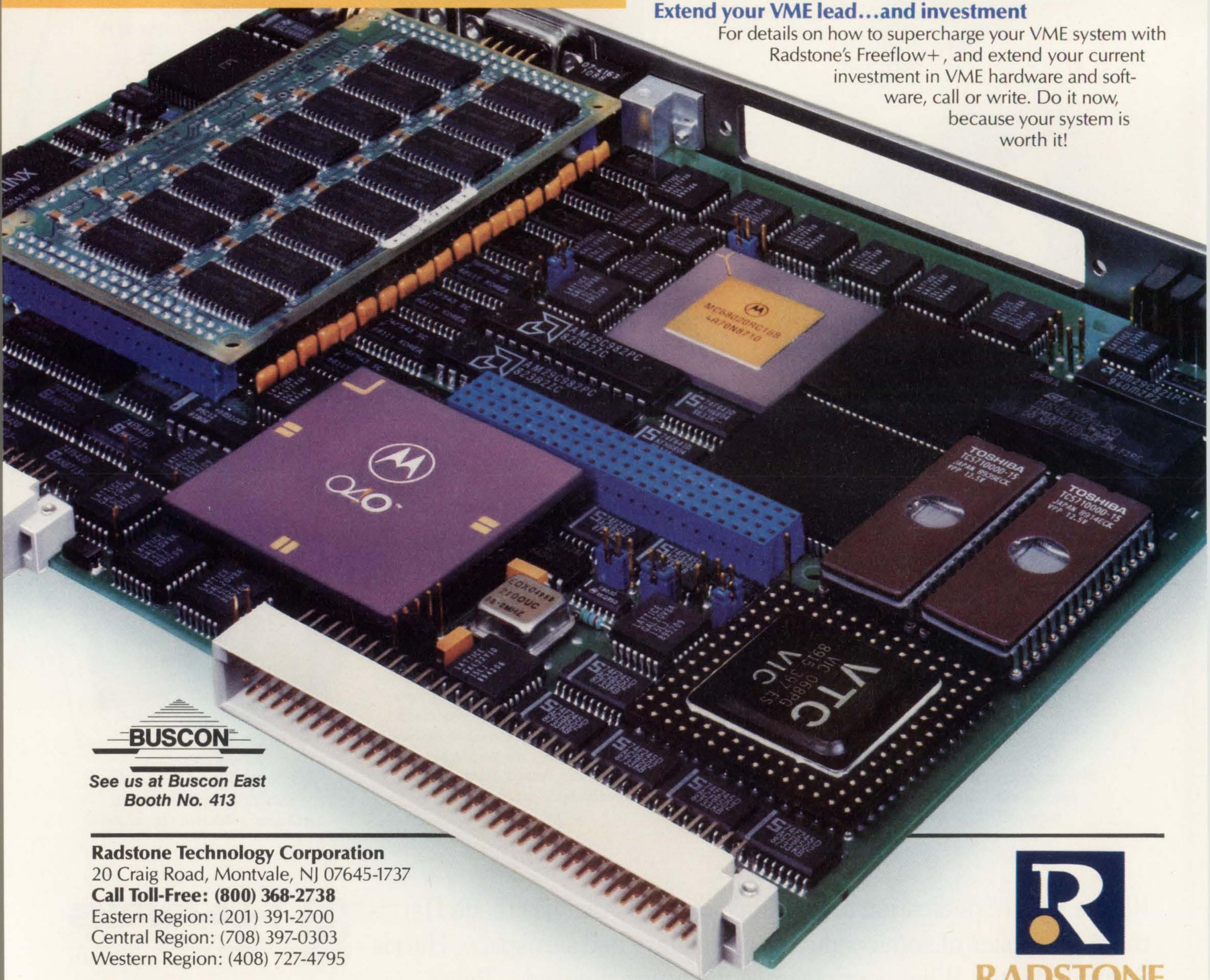

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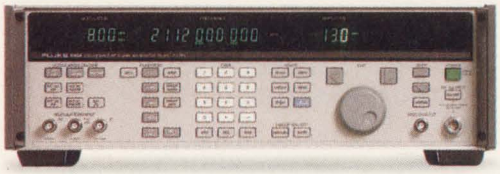

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Residual FM @1 GHz	1.5 Hz	2 Hz	2 Hz
Modulation	AM, FM, øM, Pulse	AM, FM, øM, Pulse	AM, FM, øM, Pulse
Pulsed RF			
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CIRCLE NO. 139

Sampling tracker makes short work of 0.01% settling-time test

The sampling voltage tracker, a distant relative of the sample-and-hold circuit, is the heart of a scheme for 100% testing of precision high-speed op amps' 0.01% settling time. The measurement, which is daunting enough on the bench, works reproducibly in the much tougher production environment—thanks to this little-known circuit.

Ralph Andersson, *National Semiconductor Corp*

For manufacturers of high-speed IC op amps, difficulties in measuring the devices' settling time in production have restricted the measurement to design labs and kept many manufacturers from guaranteeing the parameter. In other cases, vendors have required customers to pay a substantial premium for manually tested devices with guaranteed settling times. A new measurement approach based on a sampling-voltage-tracker (SVT) circuit at last permits automated, high-speed production tests of settling time. The technique is potentially useful outside of semiconductor manufacturing too—wherever an application demands quick, accurate measurements of signals that change rapidly over a wide dynamic range.

The technique results from adopting a systems point of view: What types of functional blocks would solve the measurement problems without causing difficulties elsewhere in the system? The SVT that lies at the heart of the system can determine within 50 μV the analog voltage at discrete points of a waveform. Similar approaches work with sample-and-hold circuits and D/A converters.

Fig 1 shows the SVT. It consists of a latchable high-speed comparator, an integrator, and a buffer. The noninverting input of the comparator is the SVT's input. The comparator's output drives an integrator whose buffered output feeds back to the comparator's inverting input.

To examine how the SVT works, assume that there is a dc level at the SVT's noninverting input, that the inverting input is a smaller dc voltage, and that the latch control is high, allowing the SVT to free run. The comparator's output will be high and will cause the integrator's output to ramp up towards the positive rail. The voltage ramp feeds back to the inverting input of the comparator via the closed-loop feedback path. The integrator will ramp up until its output passes the voltage level at the comparator's noninverting input. At this point, the comparator output switches to its low state and the process repeats, with the integrator output ramping downward. Thus the comparator forces the integrator to ramp up or down to the voltage at its noninverting input. The SVT's steady-state output is a dc voltage equal to the circuit's input plus the

Settling time is the interval that a device's output needs following a step change to reach (and remain within) a small error band surrounding the final value.

offset voltage of the comparator and an ac component, which is caused by the integrator ramping around that point.

In the free-running mode, the SVT can accurately track any input waveform that has no transitions faster than the integrator's RC time constant permits. Though this configuration can yield useful dc information such as V_{OS}, CMRR, and PSRR, it is not particularly helpful for measuring settling time. With a latch control, however, the SVT can measure the instantaneous voltage at a point in a repetitive waveform **(Fig 2a)**. By disabling the SVT's latch and repeatedly enabling it with a narrow pulse at a desired point, the SVT will provide the corresponding dc level. The voltage at the output of the SVT now consists of the dc voltage at the selected point plus the V_{OS} of the comparator and an ac component whose amplitude is inversely proportional to the sampling frequency and the RC time constant of the integrator. By increasing the time constant and the sampling rate, you can make the amplitude of the ac component arbitrarily small. Larger time constants prevent the SVT from responding to fast transitions of the input waveform, however.

An alternative to using a pulse for latching uses a high-speed comparator with its latch control held high. A D flip-flop controls latching and makes possible triggering of the SVT with an edge rather than with a pulse **(Fig 3)**. This idea is functionally equivalent to the SVT shown in **Fig 1**. Although the edge-triggered SVT is easier to interface with TTL circuits, its power consumption is higher than that of the circuit of **Fig 1**.

Fig 2a shows that under certain conditions the SVT's output can contain an erroneous offset, making the average value differ from the voltage the SVT is sampling. For the offset to exist, the peak of the ramp superimposed on the output simply needs to be great enough to exceed the comparator threshold. The direction of the ramp will then reverse at each SVT-trigger pulse, and the offset will exist in the steady state. The maximum amplitude of the offset is

$$V_{MAX} = (I_{IN}/C_F)\cdot(T_{SAMP}/2),$$

where C_F is the integrator's capacitor value, I_{IN} is the peak current through C_F, and T_{SAMP} is the SVT's sampling period. Note that in the steady state, the current through C_F is a square wave and I_{IN} is the wave's peak amplitude of either polarity.

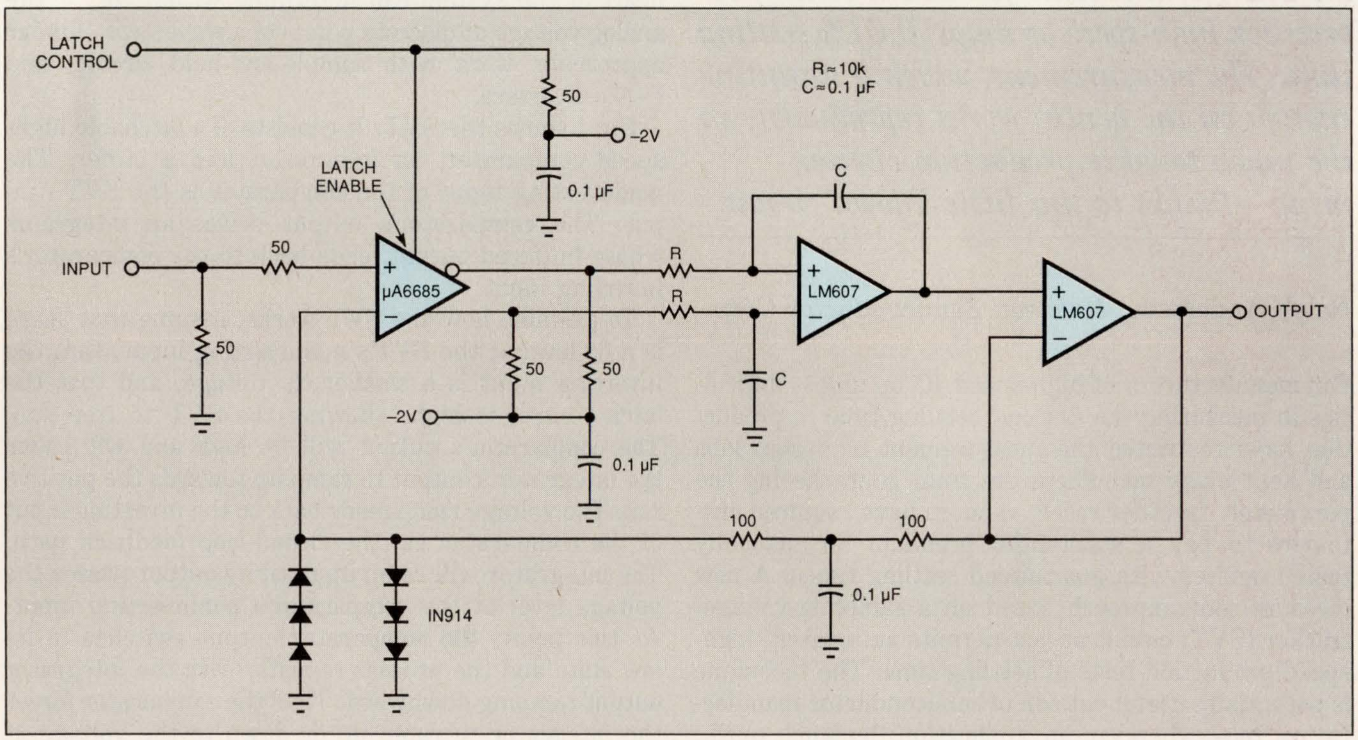

***Fig 1—The sampling voltage tracker** is conceptually straightforward. But, as with any extremely accurate wideband analog circuit, design and construction details can profoundly affect its performance.*

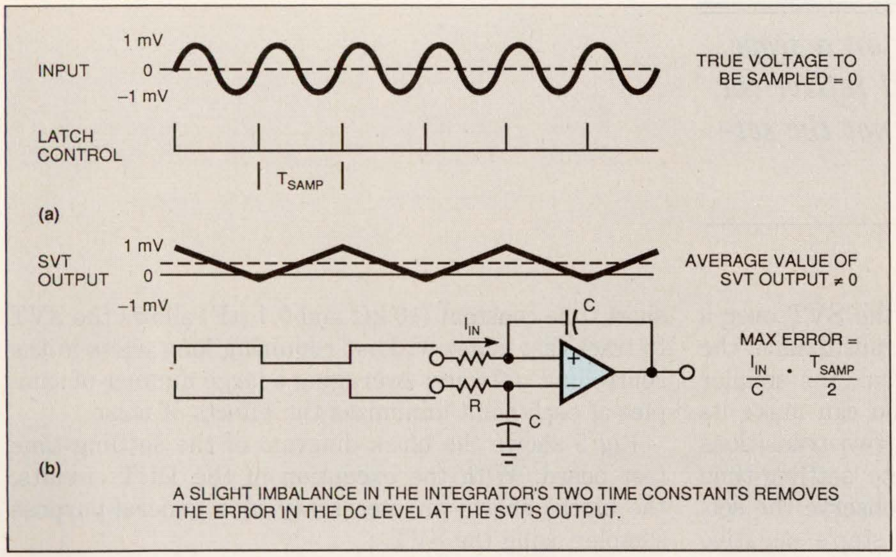

Fig 2—By repeatedly sampling a waveform *at a single point and gradually moving the point, the SVT can reconstruct the waveform* ***(a)****. The circuit's output has a dc component equal to the voltage at the sampled point plus the offset of the comparator. A slight imbalance in the integrator's input networks* ***(b)*** *minimizes the chance of error.*

You can keep this error arbitrarily small by increasing the SVT's integration time constant. There is, however, another way of solving this problem without sacrificing the response time of the SVT. Note that both inputs of the integrator in **Fig 1** contain the same time constant. Changing the resistance (or capacitance) in one of the inputs will prevent the SVT from assuming the erroneous steady-state-stable condition of **Fig 2a** and will force the circuit to find the correct sampled-voltage value. As the circuit approaches the steady-state, the integrator output will not cross the comparator threshold at every sample point until the output ramp's peak positive and negative excursions about the SVT input level are equal. As a result, the integrator will continue ramping in the same direction until its output reaches an average value equal to the voltage on the SVT's input. The ratio of the time constants need not be large. A 5 to 10% imbalance works well **(Fig 2b)**.

Repetitive measurements offer advantages

Using the SVT to make repetitive measurements has several advantages. The first is that such measurements tend to average out random noise and sporadic phase-noise errors. The integrator's time constant and the number of samples taken at each point determine the effectiveness of the averaging. Second, the op-amp integrator operates at low frequencies.

The pulse-position vernier is the circuit that selects the exact point at which the SVT samples the input

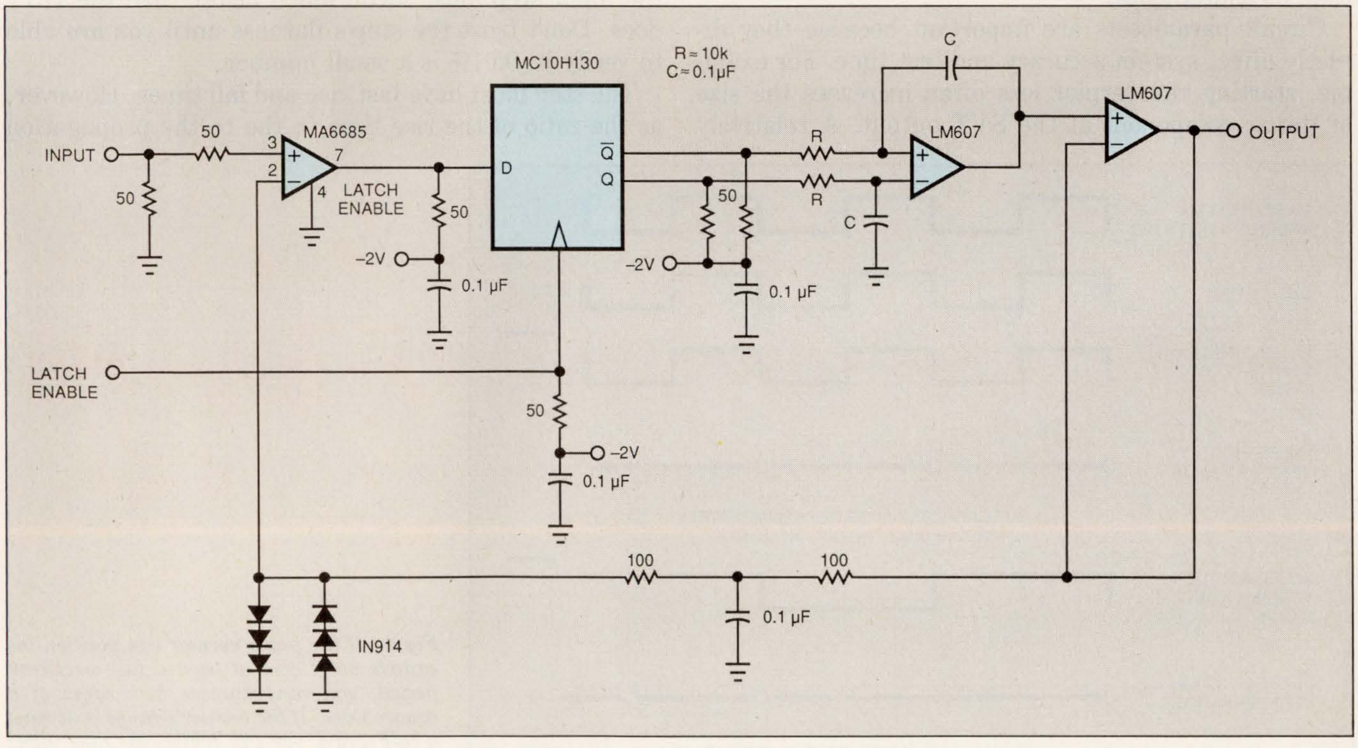

Fig 3—If you add a D flip-flop *between the output of the comparator and the input of the integrator, you can use a square wave instead of a train of narrow pulses to make the SVT sample its input.*

If you view the output directly on a scope, the measured settling time will reflect the recovery time of the scope and not the settling time of the DUT.

waveform. The vernier must trigger the SVT over a time range that includes at least two transitions of the input step. Everything else being equal, the smaller the vernier's time range, the finer you can make its time resolution. However, examining two transitions does not guarantee obtaining complete settling-time information. In **Fig 4a**, you can only observe the settling time associated with the input step's negative transition; you can't view the voltage step's positive transition because that transition is the one that starts the pulse vernier. To solve this problem, you can use a step inverter to examine either a positive- or a negative-going input step even though the vernier's starting point is fixed. Alternatively, you can extend the vernier's range (and compromise its time resolution).

Fig 4 shows that you can add a 2:1 frequency divider (that is, a D flip-flop) so that the vernier starts on every second edge of the master clock instead of on every edge. With this arrangement, the SVT can examine events before, during, and after the input step of the device under test, albeit with somewhat degraded time resolution and a somewhat greater ac component at its output. However, because you can use a step inverter, the divider is not essential for settling-time measurements.

Circuit parameters are important because they directly affect system accuracy and test time. For example, starting the vernier less often increases the size of the ac component at the SVT output. A relatively short time constant (10 kΩ and 0.1 μF) allows the SVT to track fast edges without requiring long waits in the controlling software. Averaging a large number of samples of each point minimizes the effects of noise.

Fig 5 shows the block diagram of the settling-time test board. With the exception of the DUT circuits, the blocks shown are necessary in a general-purpose sampler using the SVT.

The master clock block is the reference for calculating settling time. If you know the exact clock frequency, you can determine the exact position of a sample point. The heart of the master clock is a crystal oscillator. The DUT must settle fully in no more than half the clock period. If you expect the settling time of the DUT to 0.01% to be 400 nsec, a reasonable choice for half the clock period is 1 μsec. This choice sets the clock frequency at 500 kHz. Clock accuracy directly affects the measured settling time; a clock inaccuracy of 0.01% will result in a 0.01% error in the measured settling time.

In any settling-time-measurement setup, the step generator can cause serious errors, so you should take great care in its design and layout. No device can settle faster than the signal that drives it. Therefore, the input step must settle much faster than the DUT does. Don't trust the step's flatness until you are able to verify it; 0.01% is a small number.

The step must have fast rise and fall times. However, as the ratio of the rise time to the to the propagation

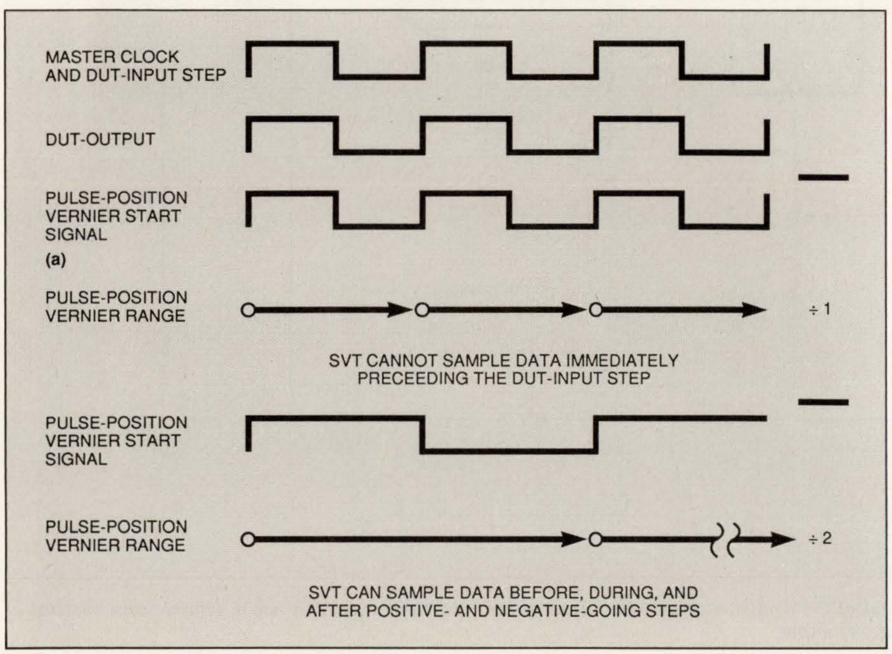

*Fig 4—**If the pulse vernier** can position the sample point over at least a full waveform period, you can examine both edges of a square wave. If the vernier's range is at least a half period, you can achieve the same effect provided you have the option of inverting the step input that drives the DUT.*

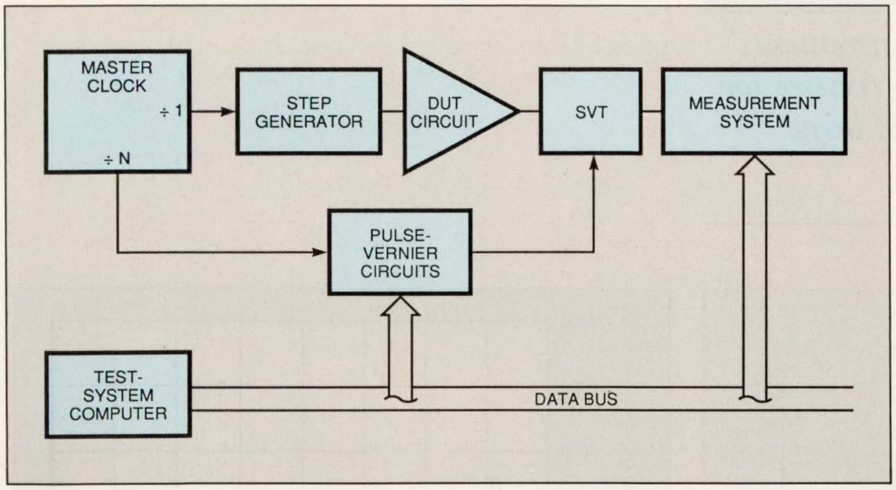

***Fig 5—The settling time test board** contains several circuit blocks in addition to the SVT.*

delay of the transmission line between the step generator and the DUT becomes large, fast edges can cause problems with reflections. When checking step integrity, a good rule of thumb is that the rate of change of the step edges must be twice the DUT's maximum slew rate. Avoid inductive and capacitive elements in the step's output path. Keep the lead lengths short and avoid inductive resistors in the terminating load. Thermal tails are always a worry with step generators, but as you will see, they are not usually a major consideration.

The false-summing-node approach (**Fig 6**) has been used for many years to measure the settling time of op amps connected as inverters. The approach's popularity is well deserved. Adding the DUT's inverted output to the input signal at a false summing node results in a signal that contains error information only. Viewing only the errors simplifies optimizing the circuits that surround the DUT because, without overdriving your scope, you can directly view the DUT's step response with high resolution. An unfortunate effect of using the false summing node, however, is that the resistive divider that connects the DUT's input and output causes the observed error band to shrink

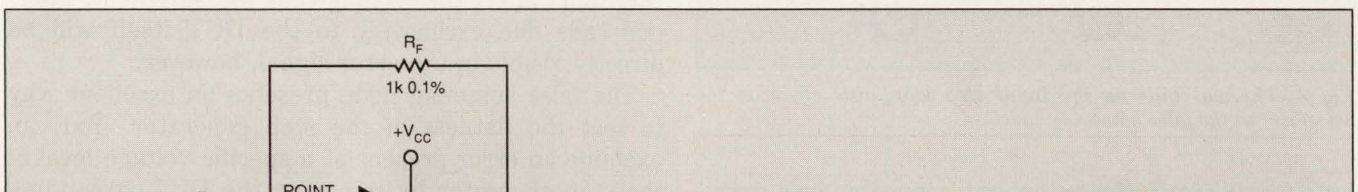

***Fig 6—A false summing node** lets you test settling time of an op-amp inverter without forcing the measurement circuits to withstand the DUT's full output. The drawback is that with a unity-gain inverter you see only half of the full error.*

The inability to reproduce measurements either limits testing to a single fixture for quality assurance or necessitates large guard bands.

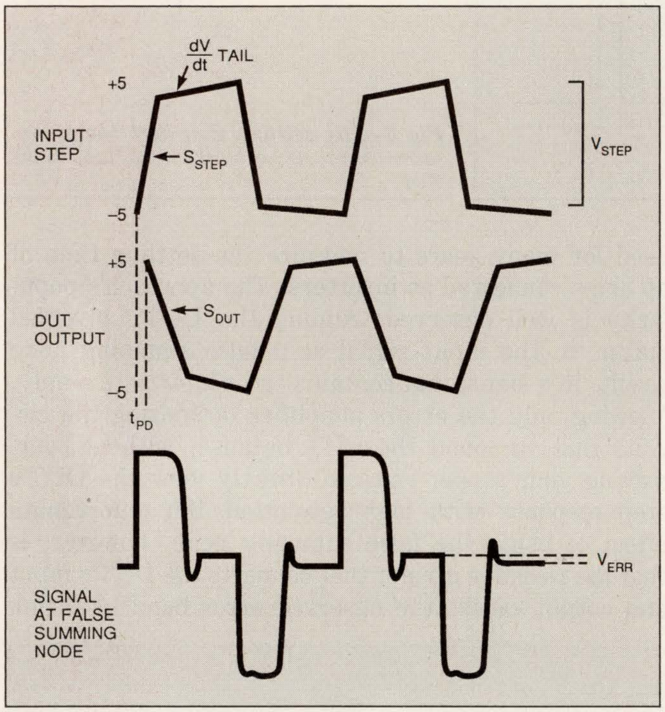

Fig 7—Thermal tails on the input step *have little effect on the waveform at the false summing junction.*

by a factor of two (for an op amp connected as a unity-gain inverter).

The false summing node mitigates problems with thermal tails in the step generator. Connecting the DUT as a unity-gain inverter cancels all of the effects of a fairly linear thermal tail at its input—except for the part that occurs while the DUT's output is slewing towards its final value. The equation

$$V_{ERR} = T_{TAIL}(((V_{STEP}/S_{DUT}) + t_{PD}) - (V_{STEP}/S_{STEP})),$$

where T_{TAIL} = dV/dt of thermal tail, V_{STEP} = amplitude of step, S_{DUT} = slew rate of DUT, S_{STEP} = slew rate of step, and t_{PD} = propagation delay of DUT, shows the error that a thermal tail causes in the waveform at the false summing node. Suppose that the thermal tail ramps at 10 mV/μsec, the DUT's propagation delay is 20 nsec, the DUT's slew rate is 70 volts/μsec, and the step's slew rate is 250 volts/μsec. The resulting error will be 1.23 mV. This error is relative, however—it is 1.23 mV with respect to the error signal's level before the transition (**Fig 7**). Thermal tails are only one reason why V_{ERR} in **Fig 7** can exist.

Another reason is gain inaccuracy in the DUT. Nonlinearities in thermal tails are usually so slight that

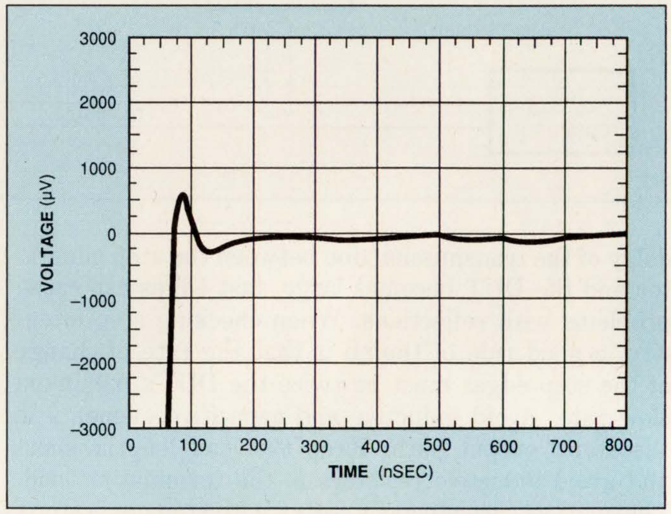

Fig 8—The SVT reconstructs *the settling of a −5 to 5V step applied to an op-amp input.*

they don't affect the settling-time measurement. Thermal tails due exclusively to the DUT itself will be directly visible in the error signal, however.

The false summing node presents an excellent way to test the flatness of the step generator. You can examine an error present at a specific voltage level of the step generator by removing the DUT, grounding point 1 of **Fig 6**'s circuit and driving point 2 to the opposing voltage level. For example, to examine the error present in the transition from −5V to 5V, you would ground point 1 and drive point 2 to −5V. The waveform at the false summing node will reveal all the overshoot, ringing, and thermal tails present in that transition. This test, as sampled by the SVT, is shown in **Fig 8**. Time t_0 on the plot is the point at which the input step began its transition from −5V to 5V.

In the false-summing-node circuit, select R_{IN}, R_{IN}', R_F, and R_F', so that $R_{IN} = R_F$ and $R_{IN}' = R_F'$ to within 0.1%. The values of these resistors depend strongly on the DUT. Consult the device manufacturer's data sheets for optimum loading values. The effects of loading on the settling-time measurement are extremely important. **Figs 9a** and **b** show, respectively, the error signal with the correct loading and with an incorrect capacitive load. The DUT used to produce these plots is an LF401, a fast-settling, FET-input op amp. A careful accounting of circuit loading, including parasitic elements, is vital to making valid measurements.

Capacitance is the factor that most often affects the performance of a fast-settling op amp. Although a feedback capacitor in parallel with the feedback resistor

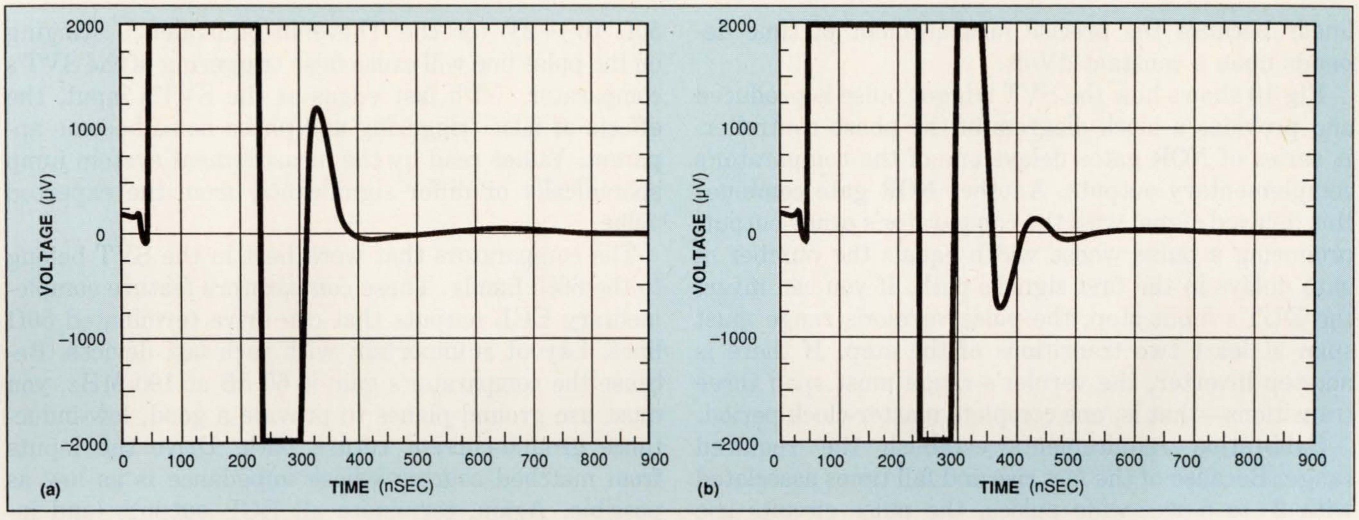

***Fig 9—When a correctly loaded LF401** settles from a −5 to +5V input step **(a)**, all transients disappear within 400 nsec. Adding load capacitance **(b)** produces a slowing of the settling that is noticeable because of the SVT's resolution.*

is usually beneficial, any capacitive loading can have devastating effects (**Fig 9b**).

The two Schottky diodes at the false summing node in **Fig 9b** act as limiters. They prevent the error signal from overdriving the buffers and the measuring equipment in the circuits that follow. A JFET and a buffer send the signal at the capacitance-sensitive false summing node to the SVT. A 2N4416 JFET was chosen because its high input impedance and low input capacitance make it an ideal follower. The buffer drives the 50Ω input impedance of the SVT and provides a place for the ac coupling that defeats the JFET's thermal drift. Choose the coupling capacitors carefully. Because of problems with dielectric absorption, avoid ceramic and tantalum capacitors; polystyrene capacitors work best.

If the settling-time-measurement setup is ever to go from the prototype stage to a production test system, it must use the correct device contactor. (The contactor is a unit that mounts on an automatic device handler and makes the electrical connections to the DUT.) For several reasons, contactors have always caused problems in settling-time setups.

The majority of contactors offer no method of placing decoupling capacitors closer than one inch from the DUT's power-supply pins—an unacceptable distance when large, rapid voltage transitions occur at the device's output. Contactors also have problems with isolation between pins, and often present a capacitive load to the DUT.

The settling-time test board uses a contactor made by Sym-tek (San Diego, CA) for applications at frequencies in excess of 2 GHz. This contactor has a characteristic impedance of 50Ω, a rise time of 140 psec, and a lead-to-lead isolation resistance of 1 GΩ. The most important feature of the contactor for this application, however, is that it allows placement of decoupling capacitors as large as 0.1 µF within 0.2 in. of the DUT's power-supply pins.

You can locate the pulse vernier on the board or externally. The vernier's resolution is an important system parameter because it establishes the effective bandwidth of the SVT, determines the maximum measurement accuracy, and affects other modules within the system. For example, it determines whether the system needs a step inverter to adequately resolve details of positive- and negative-going steps at the DUT output.

Ramp generator is heart of pulse vernier

To generate the SVT trigger pulse, the settling-time test board's pulse-position vernier generates complementary voltage steps that follow the DUT input step by a controllable delay. The vernier uses a current source that, upon the application of a rising edge, charges a capacitor to generate a voltage ramp. This ramp drives the noninverting input of a comparator whose inverting input comes from a DAC. The comparator's complementary output steps produce the SVT trigger pulse. The DAC controls the phase difference between the comparator output and the edge that triggers the ramp. It is important that the ramp be

The sampling voltage tracker that lies at the heart of the system can determine within 50 μV the analog voltage at discrete points of a waveform.

linear because the precise measurement of time depends upon a constant dV/dt.

Fig 10 shows how the SVT trigger pulse is produced and provides a block diagram of the phase controller. A series of NOR gates delays one of the comparator's complementary outputs. Another NOR gate combines this delayed signal with the comparator's other output, producing a pulse whose width equals the number of gate delays in the first signal's path. If you can invert the DUT's input step, the pulse vernier's range must span at least two transitions of the step. If there is no step inverter, the vernier's range must span three transitions—that is, one complete master-clock period.

Calibration requirements establish the required range. Because of the fast rise and fall times associated with 2- to 5-nsec-wide pulses, the pulse circuits use emitter-coupled logic (ECL). To prevent reflections, you must terminate lines driven by ECL outputs with 50Ω to −2V (or the Thevenin equivalent). Ringing on the pulse line will cause false triggering of the SVT's comparator. With fast edges at the SVT's input, the effects of false triggering and phase noise become apparent. Values read by the measurement system jump sporadically or differ significantly from the expected value.

The comparators that work best in the SVT belong to the 6685 family. These comparators feature complementary ECL outputs that can drive terminated 50Ω lines. Layout is important with such fast devices. Because the comparator's gain is 60 dB at 100 MHz, you must use ground planes to provide a good, low-inductance ground-current return path. Drive the inputs from matched sources whose impedance is as low as possible. Again, terminate all ECL outputs (and inputs) with 50Ω to −2 volts. The latch enable is the most critical signal—an improperly terminated line will

A settling-time primer

Settling time is the interval that a device's output needs following a step change to reach (and remain within) a small error band surrounding the final value. For example, if you apply a voltage step of V volts to the input of a unity-gain op-amp inverter, you can consider the circuit's output to be fully settled at the first point after which its departures from the final, steady-state value remain within $\pm[(V \cdot P)/100]$. P is a specified percentage of the step amplitude. In **Fig A**, the settling time of a 10V step to 0.01% is the time interval between t_0, the beginning of the step, and t_1, the point at which the signal crosses into a ±1-mV error band for the last time. Several aspects of settling time make the measurement difficult to obtain.

Most op-amp manufacturers specify settling time of their fast-settling devices to 0.01% of a 10V step. This definition, as **Fig A** shows, produces a ±1-mV error band. Because most scopes offer only 5-mV/div voltage resolution, accurately determining where the device under test's (DUT's) output crosses into the error band is difficult. Moreover, if you view the DUT's output directly

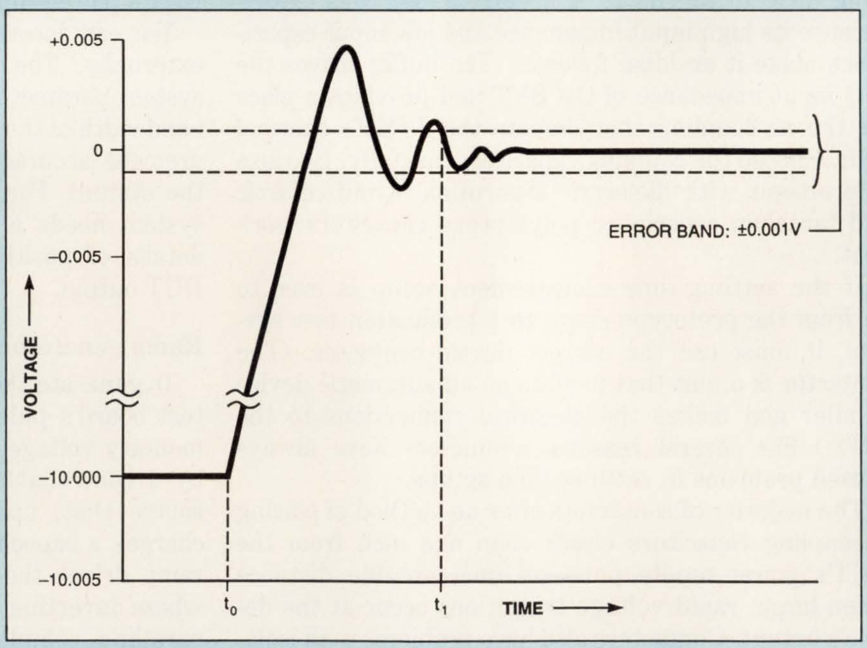

***Fig A—After a step change, settling is complete** when an op amp's output no longer leaves a specified error band surrounding its final, steady-state value.*

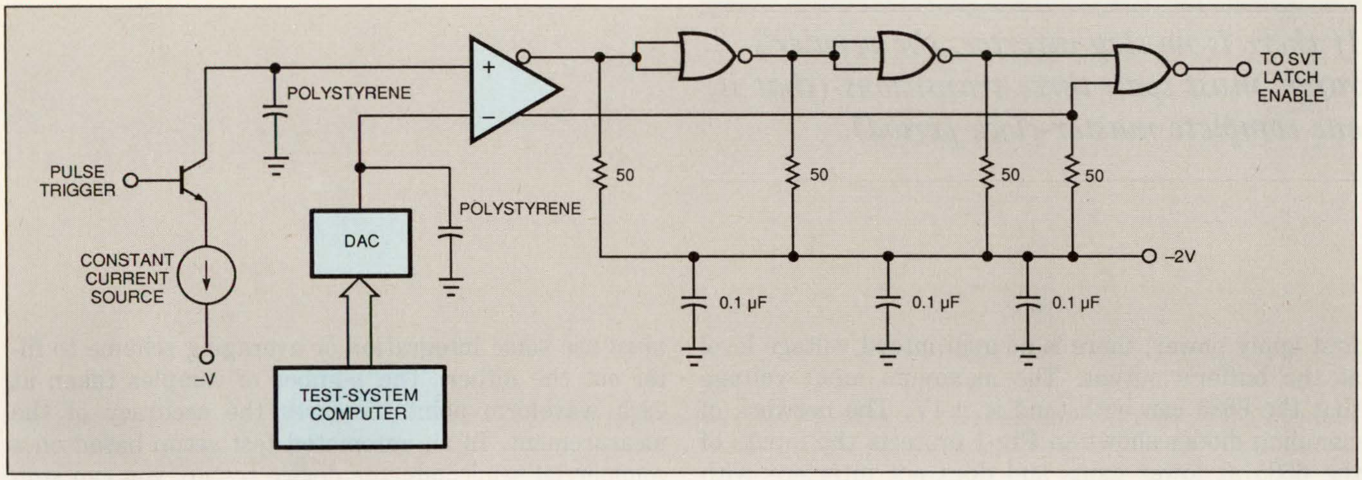

***Fig 10—The pulse-position vernier** consists of a ramp generator, a DAC, and a series of NOR gates that constitute a pulse stretcher.*

cause false triggering. The 6685's outputs, on the other hand, are essentially dc and are not as critical.

The primary consideration in selecting an integrator and a buffer is the devices' ability to drive capacitive loads. The settling-time test board uses an LM607 precision op amp for both applications. The buffer isolates the integrator from the comparator's input. The offset voltages of the buffer and the integrator are immaterial because feedback drives the buffer's output to a voltage equal to the comparator's offset plus the voltage at the comparator's noninverting input.

Keep in mind that the SVT contains a closed feedback path and that it has a closed-loop gain. **Fig 1** shows the SVT set for unity gain. Changing the gain is straight-forward. **Fig 11** shows an SVT set for a gain of 10. At all values of gain, you must observe some restrictions imposed by the 6685.

After you apply power, the voltage at the SVT's output will eventually reach a value proportional to the voltage at the circuit's input. However, when you

with a scope at 5 mV/div, you can only see the signal edge where the output settles to ground—most scopes will not provide enough offset to let you view the settling to 10V. Even if you view only the edge where the DUT output settles to ground, the signal will badly overdrive the scope's input amplifier and will cause the measured settling time to reflect the recovery time of the scope and not the settling time of the DUT.

Factors in the DUT's environment also strongly affect the measurement. The effects of loading, both resistive and reactive, can cause large settling times or ringing by introducing an unwanted pole in a device's closed-loop transfer function. The PSRR of high-speed amplifiers usually ranges from 80 to 100 dB. These values apply only at low frequencies, however. Because PSRR falls with increasing frequency, at frequencies as low as 1 MHz the PSRR will drop to nearly 0 dB. As a result, power-supply decoupling capacitors are essential for isolating the device's output from power-supply noise. However, distances greater than an inch between the DUT and the decoupling capacitors can be too great for settling measurements, so most device contactors used in semiconductor manufacturers' test departments become unusable. Most attempts at making an automated production test for settling time end here.

If those complications aren't daunting enough to the test engineer, other problems can arise from such effects as noise variations in the DUT power supply. As the DUT's output swings over a 10V range, its supply current can change substantially. As it does, supply noise can vary significantly. Moreover, the transition from a prototype board used to validate a proposed test method to a production-test department's contactor and handler often introduces additional unknowns into an already complex measurement.

Usually, settling-time measurements are restricted to bench setups with custom-built test fixtures operated by skilled technicians. One drawback of this approach is that the results are often unreproducible on different setups. The inability to reproduce measurements either limits testing to a single fixture for quality assurance or necessitates large guard bands. Large guard bands force conservative and possibly uncompetitive specs, or they lower yields and raise product cost. Test time is another drawback; manual settling-time measurements can take 20 sec or longer, making the test expensive.

If there is no step inverter, the vernier's range must span three transitions (that is, one complete master-clock period).

first apply power, there is no guaranteed voltage level at the buffer's output. The maximum input voltage that the 6685 can withstand is ±4V. The network of clamping diodes shown in **Fig 1** protects the inputs of the 6685 at lower gains and does not interfere with circuit operation. At gains greater than 4, the divider resistor that sets the SVT's gain (**Fig 11**) is sufficient to prevent large input voltages.

The 6685 should have matched impedances at its inputs, though an absolute match is unnecessary. Examining **Fig 1** from an ac point of view shows 100Ω to ground at both inputs. Likewise, the circuit in **Fig 11** splits the feedback resistors to achieve 100Ω at the comparator's inverting input while providing the desired gain of 10.

The SVT measures relative changes in its input signal; it can't make absolute measurements. Therefore, voltage offsets added to signals are immaterial. The SVT on the settling-time test board can resolve 50-μV changes with a bandwidth exceeding 300 MHz. On the advance data sheet of the LH4810, a hybrid version of the SVT described here, National Semiconductor's Hybrid Div reports a bandwidth greater than 1 GHz.

There are several ways to measure the dc component of the SVT's output voltage—despite the ac component caused by the integrator "dithering" around its average output level. The method of measuring the dc level *must* use some integration or averaging scheme to filter out the dither. The number of samples taken at each waveform point increases the accuracy of the measurement. In an automated test setup based on a commercial semiconductor device tester, you can simply use the tester's resident voltmeter. Adding a small number of components can provide the necessary filtering.

Another measurement technique uses a voltage-controlled oscillator (VCO). The ac components of the SVT's output will cause the VCO's output to vary about some center frequency. By determining the period of a large number of VCO cycles and then dividing by the number of cycles, you can find the average period and hence the average voltage. (For example, if 10,000 cycles take 1 msec, the average period is 100 nsec.) This method is much faster than using a voltmeter with a large integration time constant. But, VCOs are not all that linear over a large voltage range, so you must calibrate them to obtain the correct values of voltage vs frequency.

The first value of interest in a settling-time measurement is the point at which the DUT input step occurs. You can find this point by varying the pulse position and looking for a voltage difference between a settled portion of the waveform and subsequent points. This point, shown in **Fig 12**, is called t_0. The settling-time test

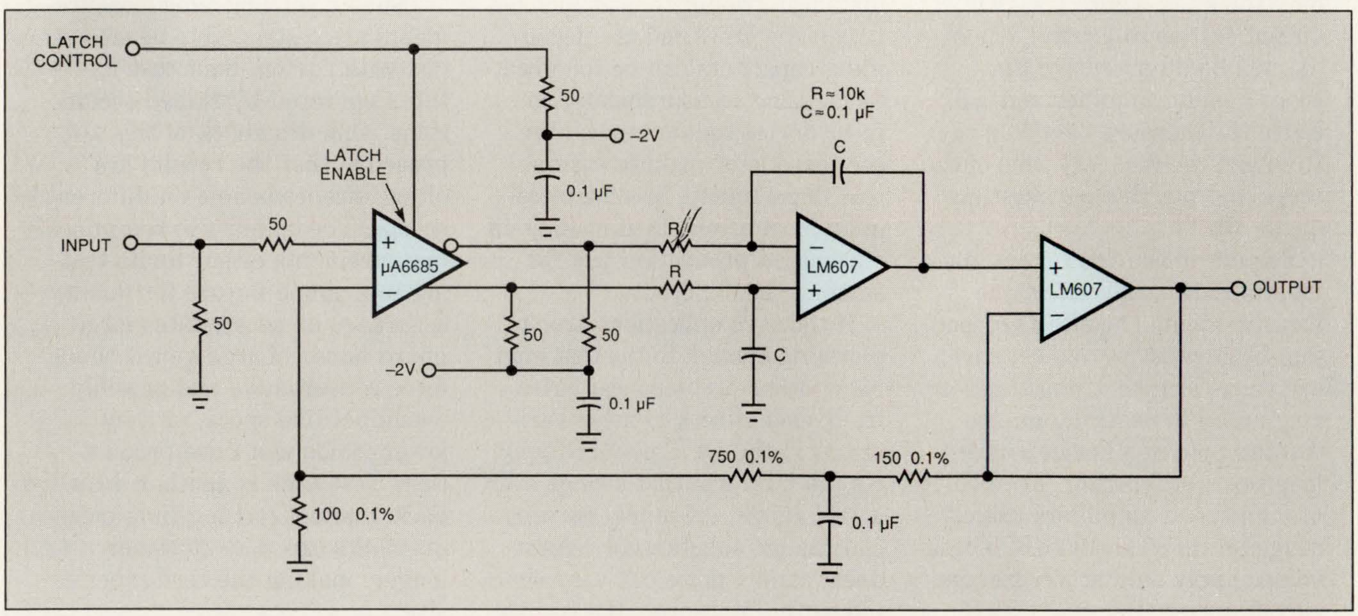

***Fig 11—Adding a gain of 10 to the SVT** involves a simple change—adding a 9:1 divider in the feedback loop. The divider permits the removal of the diode clamping network used by the unity-gain SVT.*

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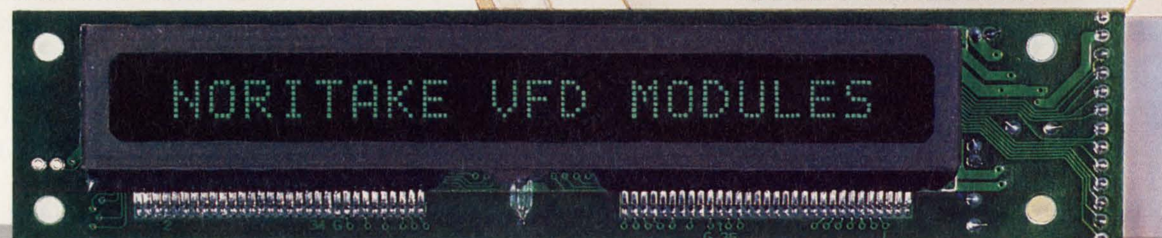

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	CU169SCPB-L	1 × 16	9.0	P	x	
	CU205SCPB-S	1 × 20	5.0	S/P		
	CU209SCPB-L	1 × 20	9.2	P	x	
	CU2015SCPB-L	1 × 20	15.1	P	x	
5 x 7 DOT MATRIX PLUS CURSOR	CU406SCPB-S	1 × 40	5.0	P	x	
	CU20026SCPB-S	2 × 20	5.1	P	x	x
	CU40026SCPB-S	2 × 40	5.0	P	x	x
	CU40046MCPB-S	4 × 40	5.0	S/P	x	x
	CU40066MCPB-S	6 × 40	5.0	S/P	x	x
	CU40086MCPB-S	8 × 40	5.0	P	x	x

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The method of measuring the dc level must use some integration or averaging scheme to filter out the dither.

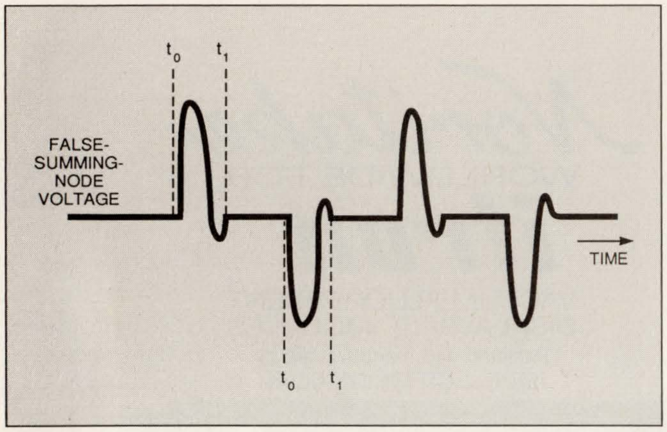


***Fig 12—The waveform** at the false summing node consists of a series of pulses. The waveform drops to zero whenever the op amp's output has settled to its steady-state value.*

board records t_0 by storing the input code of the D/A converter that (indirectly) positions the sampling pulse.

You then move the pulse to a portion of the waveform where the DUT output has settled. This voltage serves as a reference for finding t_1, the point where the error signal passes outside of the 500 μV error band (actually, the point where the error signal enters the error band for the last time). When you have positioned the pulse at t_1, you subtract from the DAC input the number representing the DAC input at t_0.

Calculate time by manipulating DAC inputs

To equate this calculated difference to an actual time in nanoseconds, you must know how much the sample point moves for each LSB change in the D/A converter's input. The pulse vernier must be able to strobe the SVT at any point in a full period of the DUT input step. If you can invert the step, the vernier only needs to strobe the SVT over a range covering a little more than two step transitions. In **Fig 12**, the error signal at the false summing node clearly shows these transitions. By finding the DAC input values at each of the step period's three transitions (at the beginning, middle, and end of the period), you know how much you must change the DAC input to position the strobe pulse over a full step period. If you divide the step period (in nanoseconds) by this number, you have dt/dN—nanoseconds/bit. Multiplying this quantity by the difference between the t_1 and t_0 DAC inputs yields the settling time.

You can measure settling time in many ways. The measurement is rarely trivial, but when you must perform it at high speed to 0.01% in a production environment, it can become a nightmare. One of the outstanding features of the SVT described here is its ability to resolve small voltage changes. The SVT's sensitivity lets it measure the error signal at the false summing node without amplification. Another of the SVT's advantages is reproducibility. Different samples of the settling-time test boards described here make measurements that correlate within 10 nsec. On any one board, a 350-nsec measurement is repeatable within 5 nsec. The system is self-calibrating; its measurement speed depends on the speed of the automatic test system with which you use it.

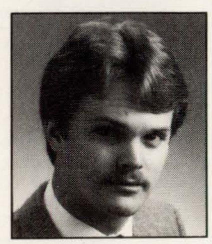
The SVT can do much more than test settling time; it can characterize waveforms from dc to RF. Other SVT applications include measuring propagation delay, slew rate, rise time, fall time, and acquisition time. Because of its extreme speed and accuracy, quantifying the circuit's performance is difficult, but in two of its key parameters, the settling-time test board's SVT is at least this good: Its bandwidth is more than 300 MHz and its voltage resolution is less than 50 μV.

EDN

Reference

1. Halbert and Koen, *A waveform digitizer for dynamic testing of high-speed data-conversion components*, Burr-Brown Corp, Tucson, AZ.

Author's biography



Ralph Andersson is an ASIC design engineer with National Semiconductor Corp in Santa Clara, CA. He has worked at NSC since obtaining his BSEE from the University of California—Davis three years ago. In his first assignment at National, he worked in test development, where he developed the techniques discussed in this article. His hobbies include scuba diving and skiing.

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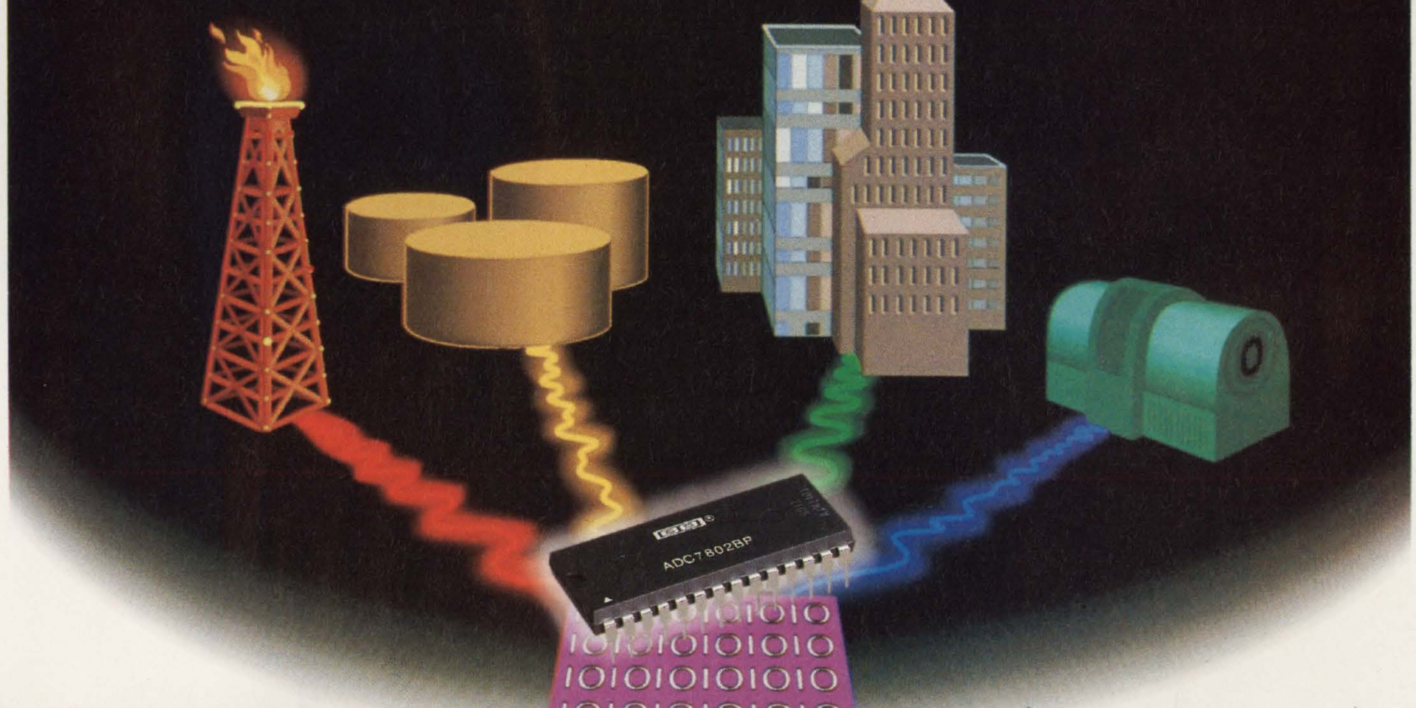

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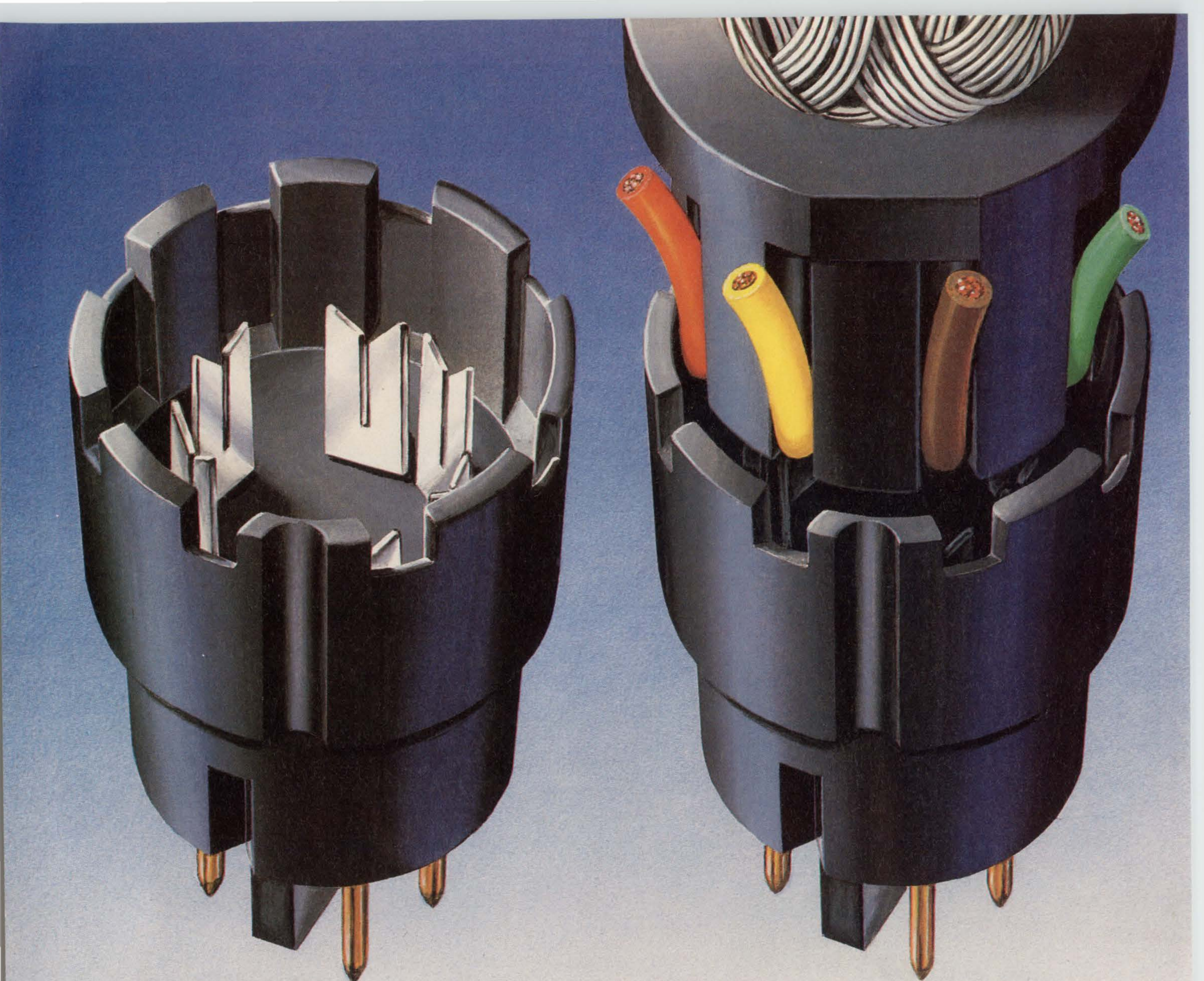

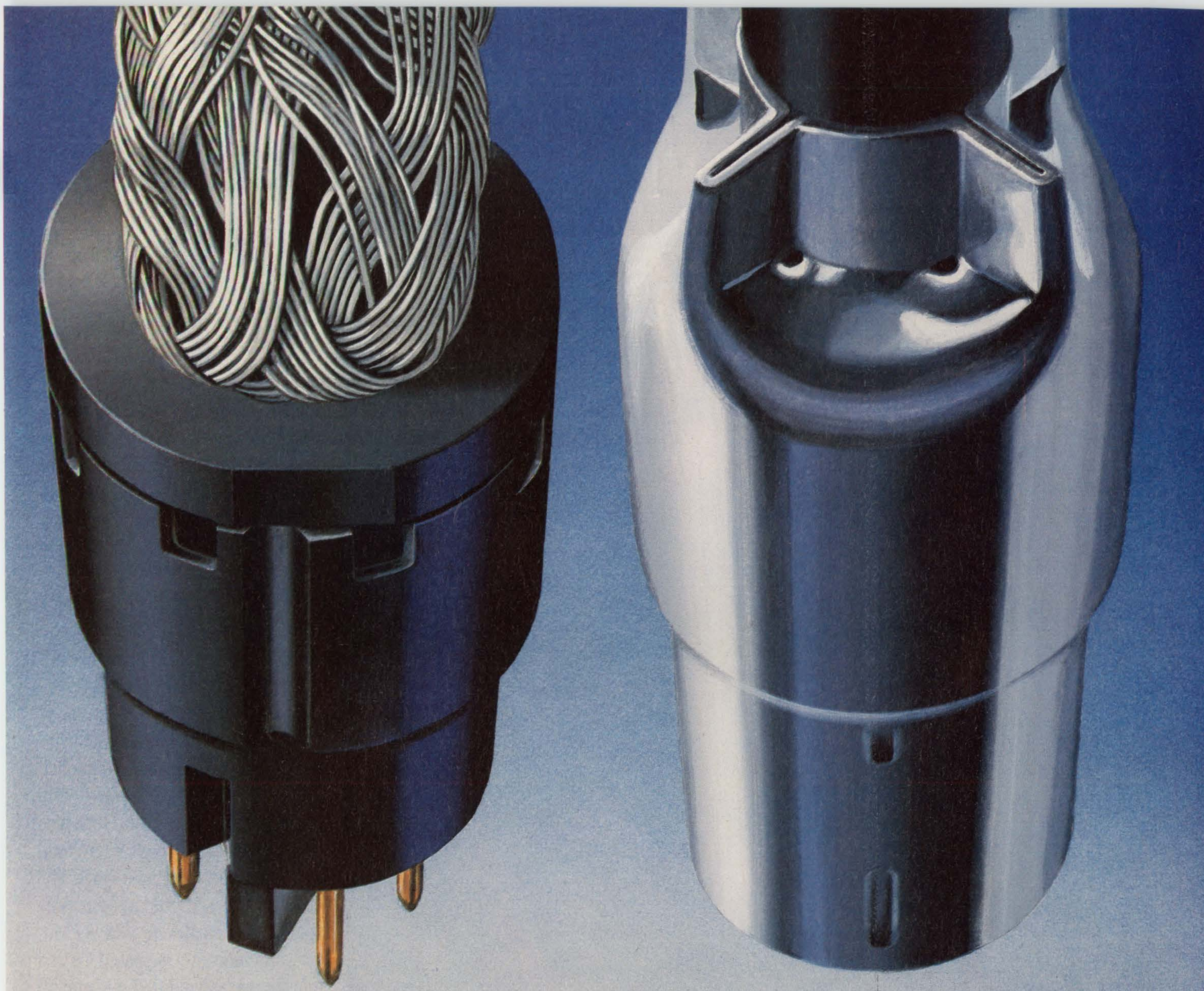

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***SMC6235	4096 x 12	574 x 4	3 or 4	48	Sound Generator Counter, BLD, AC
SMC6246	6144 x 12	640 x 4	8 or 16	40	Sound Generator Twin Clock, BLD
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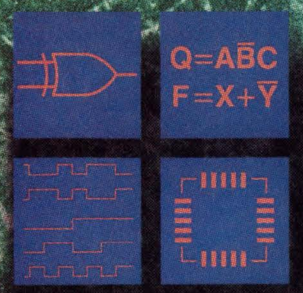

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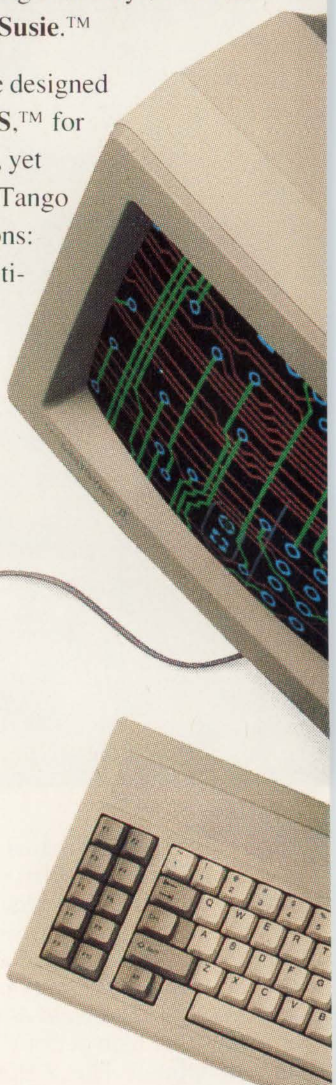

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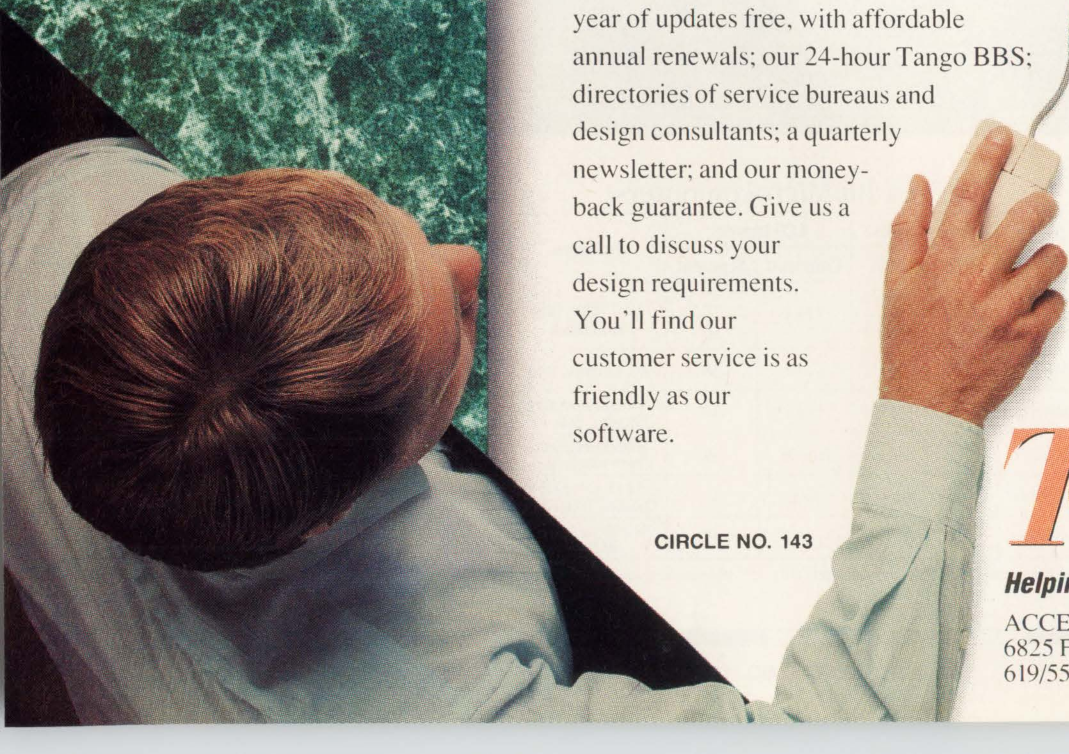

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General-purpose languages simulate simple circuits

Although you can spend lots of money on commercial simulators, inexpensive alternatives exist that will enable you to build and experiment with behavioral-simulation models.

Jozef Kalisz, *Associate Professor,*
Warsaw Academy of Technology

Many logic simulation programs are capable of solving virtually any logic-, timing-, and fault-simulation problems (**Ref 1**). However, these programs are expensive—$1000 to $50,000 or more—and use proprietary and sometimes peculiar modeling languages. Often the more expensive and powerful the simulator, the harder it is to use. In addition, you usually receive these programs in object (binary) code which is practically impossible to understand or modify.

The recently adopted VHDL (VHSIC hardware description language) (IEEE-1076-1987), mandated by the US Dept of Defense, provides a comprehensive basis for developing powerful software tools for logic simulation and design (**Refs** 2 and 3). VHDL also offers a way to formally describe and document electronic circuitry. The language's proponents claim that such standardization also allows full compatibility of electronic documentation among different manufacturers. By precisely defining the initial specifications, you can perform a more detailed verification of the final product.

VHDL also has its detractors (**Refs** 4 and 5). They claim that it is complex, verbose, and requires great computational effort. Some hardware designers say VHDL is cumbersome and that its definition does not include a clear method for the integration of the design environment, unless the language is supported by comprehensive software systems. Although VHDL is the only prospective industry standard, the software packages currently available for simulation and design are expensive ($25,000 to $50,000) and generally require a similarly expensive workstation.

A simple "software breadboard" called Turbo-Logic Simulator (TLS) uses algorithmic behavioral models of logic circuits as functions or procedures to describe relevant micro-operations. You can model complex devices much more rapidly using behavioral language modeling than you can using structural-level modeling. In addition, because behavioral language lets you model the devices at various levels, it is well suited for use in hierarchical design. In fact, VHDL allows you to use behavioral models.

If you are starting to simulate modest designs, a general-purpose high-level language such as Borland's (Scotts Valley, CA) Turbo Pascal offers functional simulation and a means to understand the simulation models. In addition, the user-friendly interfaces of the compiler simplify customization of the simulation pro-

You don't have to spend thousands of dollars on software if you want to learn about logic simulation.

gram. If you know the basics of Turbo Pascal and have the compiler at your disposal, you can create a simple simulator in a few days.

TLS, in the source language Turbo Pascal 4.0, 5.0, or 5.5, comes on a set of disk files. Some files, such as the general declaration file and the function/procedure libraries, are already compiled and represented on the disks by separate titles with the extension .TPU in their names. The files are contained in the directory TLS, along with the main Turbo Pascal compiler files (TURBO.EXE and TURBO.TPL).

In a typical application on a personal computer with a hard disk, you simulate a logic circuit by writing and executing the simulation program. For this type of simulation, you'd select and use the library functions or procedures that serve to describe the circuit network, generate input test vectors, and display results. Select the files that you need for realization of the program by using the clause USES (for compiled units) or the directive $I (for source code files).

The unit Dec (general declaration file), which **Listing 1** shows in a simplified form, contains the declarations of the most frequently used array and string types, plus the declarations of some variables. The declaration of global variables simplifies writing the actual simulation programs. The variables m, n, and l are tailored for applications in iterative instructions. The variables v1 through v30 and f1 through f30 can be used when you need variables that require temporary storing of their values during execution of the programs. The simple function Ran allows for generation of random bit values from the set B = {0, 1}. In an actual program,

Listing 1

```
unit Dec;
  {  General declaration file  }
interface
type       B = 0..1;
          r2 = array[0..1] of B;
          r3 = array[0..2] of B;
          .....................
          .....................
         r16 = array[0..15] of B;
         br4 = array[0..3] of boolean;
         br8 = array[0..7] of boolean;
          s2 = string[2];
          s3 = string[3];
          .............
          .............
         s16 = string[16];
var      m, n, l  :  shortint;
         v1, v2, ..., v30  :  B;
         f1, f2, ..., f30  :  boolean;
function Ran : B;
implementation
function Ran;     {  Generate random bit walues  }
  var  u  :  real;
  begin
    u := Random;
    if u < 0.5 then Ran := 0 else Ran := 1
  end;
end.
```

the initializing procedure Randomize, which is inherent in Turbo Pascal, precedes this function.

You have to describe the simulated circuit by a set of equations in accordance with the Turbo Pascal syntax. In the simplest cases, you represent the input and output data of each logic element as a single-bit variable with values from set B or as a multibit variable in the form of a 1-dimensional array (vector). For representation of binary numbers of the form

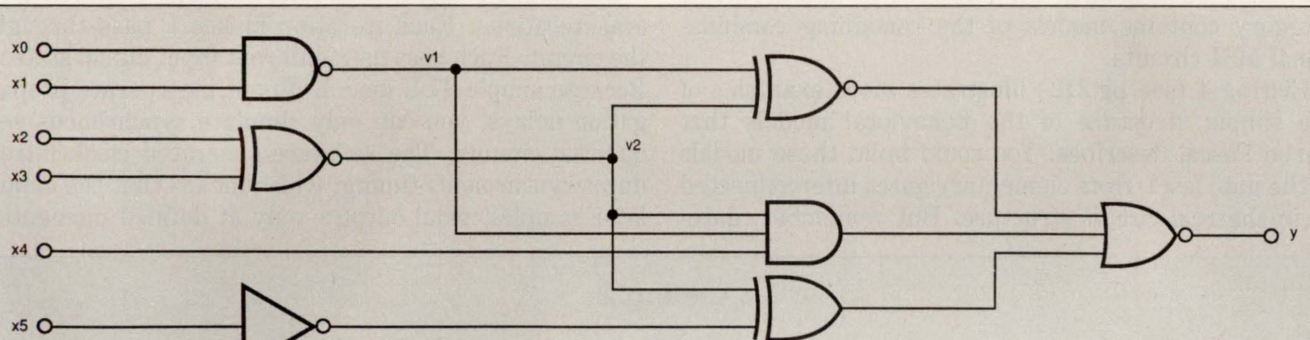
$$a_{n-1}, a_{n-2}, \ldots a_1, a_0$$

use the subscript numbers to index the elements in the array. For example, the binary number 10110 can be represented by the array A[:]r5=(0,1,1,0,1) or $A[0]=a_0$, $A[1]=a_1$, and so on. Your input data will usually be the string type, like the output data resulting from the simulation. You can use simple Pascal procedures for appropriate conversion of types.

In general, you can represent any combinational circuit as a network of appropriately connected single-output gates, such as AND, NAND, OR, NOR, XOR, and INV. You can describe this gate network by functions—a single function for each output of the circuit. If the output signal of any gate drives more than a single gate that signal should bear the name of some intermediate variable, such as v1. The precedence of the circuit description follows the direction of the signal flow within the circuit. **Fig 1a** illustrates this precedence where the program NetSim simulates the gate circuit.

To simulate other single-output networks, you need only modify the parts of this program that have been tinted in **Fig 1b.** The predefined library units Gate and Gater, which come with the software, contain functions corresponding to elementary gates. **Listing 2** provides some examples of individual functions. These examples are similar to the corresponding VHDL descriptions (**Ref 2**) but are much simpler.

The procedure State, in **Listing 3**, can display the



(a)

```
program NetSim;
uses Dec,                { General declaration file }
     Gate,               { Library of gate models }
     Crt;
var   X : r6;            { Input vector }

function Net(X : r6) : B;       { Describe the gate network }
begin
  v1 := NAND2(X[0], X[1]);
  v2 := XNOR2(X[2], X[3]);
  Net := NOR3(XNOR2(v1, v2), AND3(v1, v2, X[4]), XOR2(v2,
                                                     INV(X[5])))
end;

{$I State }    { Generate test vectors and display state table }
begin State end.
```

(b)

STATE TABLE   X:y

000000:0	010000:0	100000:0	110000:0
000001:0	010001:0	100001:0	110001:0
000010:0	010010:0	100010:0	110010:0
000011:1	010011:1	100011:0	110011:0
000100:0	010100:0	100100:1	110100:1
000101:0	010101:0	100101:1	110101:1
000110:0	010110:0	100110:1	110110:1
000111:0	010111:0	100111:0	110111:0
001000:0	011000:0	101000:1	111000:1
001001:0	011001:0	101001:1	111001:1
001010:0	011010:0	101010:1	111010:1
001011:0	011011:0	101011:0	111011:0
001100:0	011100:0	101100:0	111100:0
001101:0	011101:0	101101:0	111101:0
001110:0	011110:0	101110:0	111110:0
001111:1	011111:1	101111:0	111111:0

(c)

Fig 1—You can simulate a 6-input, single-output gate network (a) *by using a simple Turbo Pascal program such as NetSim **(b)**. The state table that will result is shown in **c**.*

Behavioral language is well suited to hierarchical design because it lets you model devices at various levels.

state table of the simulated logic network as long as the number of input variables is not greater than seven. The display is formatted automatically. If the logic network requires more than seven inputs, then you need to modify the procedure.

Fig 1c shows the result of a simulation of the logic network of **Fig 1a.** The program provides the bare state table, without bells and whistles such as a frame or colors. You can add these features if you like, but only at the expense of greater program length.

The models of typical integrated circuits from the popular TTL and CMOS HC families are grouped by the vendor into common categories such as those you'd find in catalogs of ICs. Thus the categories named Gate and Gater, which contain models of integrated gates with two, three, four, and eight inputs, correspond directly to the types of the device. For example, the function G_10(in1, in2, in3) represents a 3-input NAND gate (1/3 7410). More complex MSI circuit models are grouped in a similar way. The Arit category contains models of all arithmetic circuits, and the Logic category contains models of the remaining combinational MSI circuits.

Listing 4 (see pg 212) illustrates more examples of the simple structure of the behavioral models that Turbo Pascal describes. You could build these models at the gate level, from elementary gates interconnected as in the real circuit structure. But remember, gate-level models are more complicated and require more memory space than behavioral-level models, plus they slow the running of the program.

Using this behavioral method, you can create models of more complex circuits such as ALUs and PLDs. You can customize your simulation program by designing the proprietary models of only those devices you actually use. Your library of models will grow gradually as you design.

You can estimate maximum propagation time by determining the longest path of the signal flow inside the circuit under development. This won't hold true when you have specifically designed a circuit to produce output pulses caused by a hazard condition that you intentionally introduced. Such edge detectors are usually so simple, however, that a timing simulation isn't necessary. On the other hand, some timing is a must for the simulation of sequential circuits because they possess memory. Only rarely will you need timing simulations of typical modest combinational circuits.

Simulating sequential circuits normally requires several iterations. Each iteration makes a pass through the circuit. Each pass uses different input signal states. Because simple TLS models do not incorporate propagation delays, you can only simulate synchronous sequential circuits. The software-generated clock introduces synchronous timing, which means that the simulator samples nodal outputs only at defined moments.

Listing 2

```
function AND2(d1, d2 : B) : B;          { 2-input AND gate }
  begin  AND2 := d1 and d2  end;
function NAND2(d1, d2 : B) : B;         { 2-input NAND gate }
  begin  NAND2 := AND2(d1, d2) xor 1  end;
function XOR2(d1, d2 : B) : B;          { 2-input XOR gate }
  begin  XOR2 := d1 xor d2  end;
function INV(d1 : B) : B;               { Inverter  }
  begin  INV := d1 xor 1  end;
```

(a)

```
function ORr4(D : r4) : B;            { 4-input  OR gate  }
  begin  ORr4 := D[0] or D[1] or D[2] or D[3]  end;
```

(b)

For example, timing of the edge-triggered D flip-flop begins when the clock signal changes from the 0 state to the 1 state. The simulator memorizes present-state values automatically while the program runs if you define the global variables in the unit Dec.

The first step in creating a simulation is initializing all the memory elements of the circuit. Ideally, you should set up the initial logic states of the memory elements as if you were actually operating a real IC. The simulation programs of simple circuits at the gate and flip-flop level utilize:

- the previously introduced units Dec, Gate, and Gater,
- the library unit FF containing the flip-flop models,
- some files with test/display procedures.

Fig 2a shows an example of a synchronous sequential circuit. The circuit's design specification requires that the output $y=1$ occur only during the input state $x_1,x_2=1,0$ if both of the two preceding input states have been equal to 0,1. In all other situations, the output should be low. **Fig 2b** shows the circuit's simulation program. The program utilizes a model of the pulse-triggered JK flip-flop (with reset at $R=0$) that procedure JK1 (**Listing 5a**, see pg 213) describes. The variable f detects the transition of the control (clock) signal from $C=1$ to $C=0$. The procedure Tab21 (**Listing 5b**) displays the state-transition table (**Fig 2c**) of the simulated circuit using the predefined sequence of the input states $x_1=i_1$ and $x_2=i_2$. **Fig 1c** presents the results of this simulation.

You may also modify the circuit simulation to allow the function Ran, contained in the unit Dec, to randomly generate input signals. Simply replace i1[n] and i2[n] in the SNet expression within the "repeat...until" loop with the variables a := Ran; and b := Ran;, then insert the initializing procedure Randomize before the loop. Note that the sequence of the input states i1[n], i2[n] in the program SNetSim **(Fig 2b)** is no longer necessary. The random number generator usually generates the input sequence, which results in $y=1$ after a few program runs. If you'd like to run a larger number of loop iterations, increase the loop-control variable n in procedure Tab21 **(Listing 5).** This variable corresponds to the number of simulated clock cycles.

Listing 6 (see pg 214) is a model of the popular '164 8-bit shift register. It illustrates TLS models and their

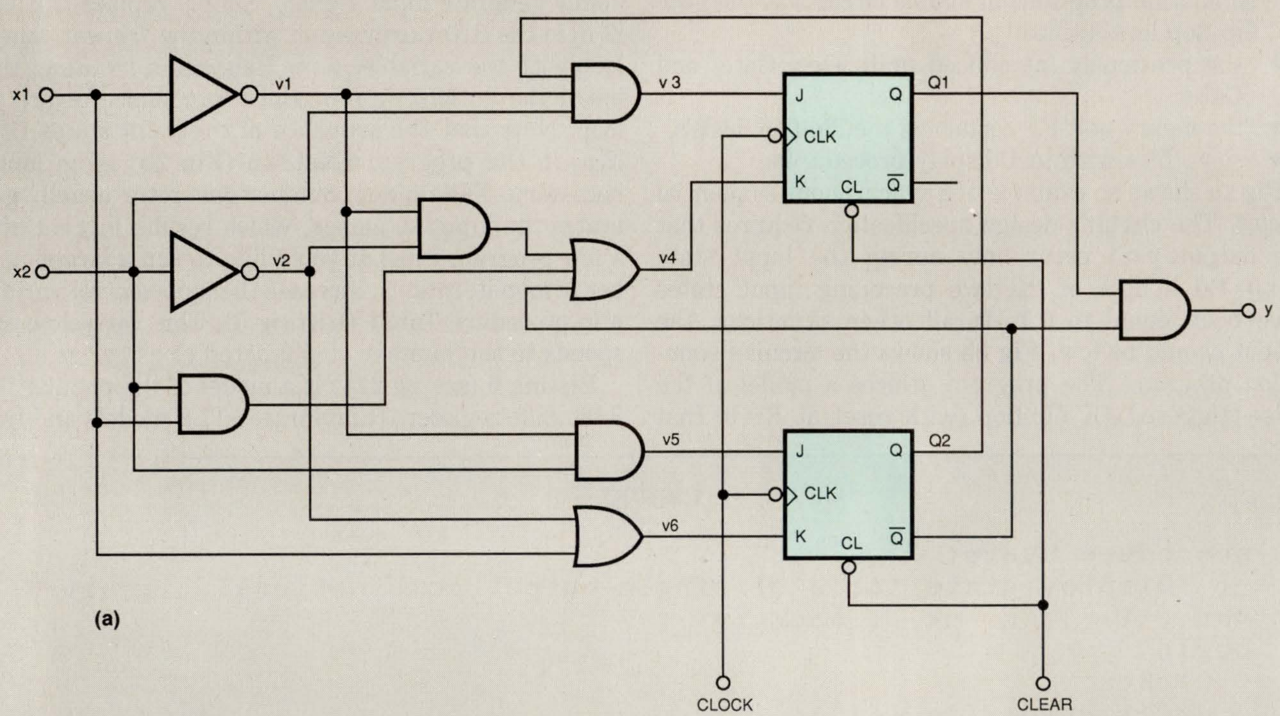
Listing 3

```
procedure State;
 {  Display state table of single-output combinational circuit }
var    i, j, k, ux   : shortint ;
begin
  ClrScr;
  ux := Pred(SizeOf(X));
  FillChar(X, SizeOf(X), 0);
  Writeln('STATE TABLE  X:y'); Writeln;
  for i := 0 to Pred(2 shl ux) do
  begin
    GoToXY(i div 16*10 + 1, (i mod 16) + 4);
    for j := ux downto 0 do Write(X[j]);
    Write(':', Net(X));
       {  Generate test vectors X  }
    k := -1;
    repeat
      k := Succ(k);
      X[k] := X[k] xor 1;
    until (X[k] = 1) or (k = Succ(ux))
  end
end;
```

Signal flow within your circuit determines the precedence of your description.

application to more complex MSI sequential circuits. All models of the register circuits have been incorporated in the library unit Reg. Applying this model to simulation of the 8-bit self-starting ring counter (**Fig 3a**) lets you test the feedback arrangement, which ensures that the register returns to the valid sequence after any arbitrarily chosen initial state (**Fig 3b**).

The model of the T flip-flop in **Listing 7a** (see pg 214) helps describe the '93 counter at the flip-flop level (**Listing 7b**). The first procedure is in the library unit FF and the second is in the unit CTR. The procedure in **Listing 7c** illustrates the behavior of the '93 counter operating as a modulo-6 counter, that is, with outputs Q_B and Q_C connected to the reset inputs $R_{O(1)}$ and $R_{O(2)}$, respectively. These examples illustrate the usefulness of Borland's Turbo Pascal compiler when you want to



(a)

```
program SNetSim;
uses Dec, Gate, FF, Crt;
    { Arbitrary sequence of input signals  }
const         i1 : r10 = (0, 0, 0, 1, 1, 0, 1, 0, 0, 0);
              i2 : r10 = (0, 1, 1, 0, 0, 1, 0, 1, 1, 1);
    { Describe the sequential circuit  }
procedure SNet(x1, x2, c, r : B; var Q1, Q2, y : B);
begin
  v1 := INV(x1);
  v2 := INV(x2);
  v3 := AND3(v1, x2, Q2);
  v4 := OR3(AND2(x1, x2), AND2(v1, v2), INV(Q2));
  v5 := AND2(v1, x2);
  v6 := OR2(x1, v2);
  JK1(c, r, v3, v4, Q1, f1);
  JK1(c, r, v5, v6, Q2, f2);
   y := AND2(Q1, INV(Q2))
end;
{$I Tab21 }         { Display the state-transition table  }
begin  Tab21  end.
```

(b)

n	x1	x2	Q1	Q2	y
0	0	0	0	0	0
1	0	1	0	1	0
2	0	1	1	1	0
3	1	0	1	0	1
4	1	0	0	0	0
5	0	1	0	1	0
6	1	0	0	0	0
7	0	1	0	1	0
8	0	1	1	1	0
9	0	1	1	1	0

(c)

***Fig 2—The sequential circuit in (a)** produces the state table **(c)** when you use the procedure SNet in the program SNetSim **(b)**.*

create a very simple logic simulator. Although TLS is less powerful than its commercial brothers, it may solve many of your design problems. EDN

Listings continued on next page

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Author's biography

Jozef Kalisz is an associate professor of electronics at the Warsaw Academy of Technology (Warsaw, Poland). He has taught digital microelectronics and conducted research in precision time-resolving instrumentation. He earned his MSEE at Silesian Technical University and his PhD in applied sciences at the Institute of Nuclear Research in Swierk, Poland. His leisure activities include walking, bicycling, skiing, swimming, and listening to music.

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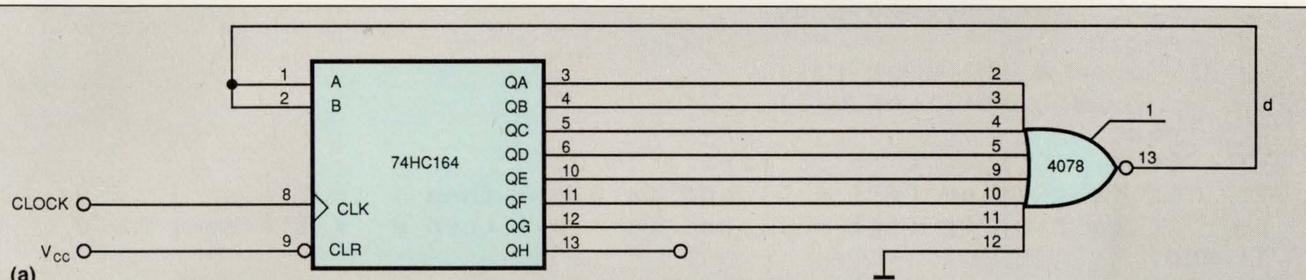

(a)

```
program RingCtr;
uses Dec, Gater, Reg, Crt;
    {  Assume arbitrary initial state  }
const    S   :  r8 = (1, 1, 1, 0, 1, 0, 1, 1);
var      T   :  r8;
      c, d   :  B;
begin
  ClrScr;
  c := 1; T[7] := 0;
  Writeln(' State S'); Writeln;
  for m := 1 to 40 do   {  Sequence of 20 clock pulses  }
  begin
    c := c xor 1;        {  Clock  }
    for n := 0 to 6 do T[n] := S[n];
    d := NORr8(T);
    SRG_164(c, d, d, 1, S, f1);
    if c = 1 then
    begin
      for n := 7 downto 0 do Write(S[n]);
      Writeln
    end
  end
end.
```

(b)

Fig 3—The RingCtr program (b) simulates the behavior of the 8-bit self-starting ring counter (a) *for any arbitrary initial state. The feedback gate forces a valid sequence after a maximum of seven clock cycles.*

You'll need timing information to design a circuit to produce output pulses caused by hazard phenomena.

Listing 4

```
procedure MUX_151(A : r3; D : r8; e : B; var y, w: B);
begin
  if e = 1 then y := 0
  else  y := D[(A[2] shl 1 or A[1]) shl 1 or A[0]];
  w := y xor 1
end;
```

(a)

```
procedure Comp_85(P, Q : r4; gi, ei, li : B; var  g, e, l : B);
var     a, b, i   :   byte;
begin
  a := 0;  b := 0;
  for i := 3 downto 0 do
  begin
    a := a shl 1 or P[i];
    b := b shl 1 or Q[i]
  end;
  if a = b then e := ei else e := 0;
  if (a < b) or ((li = 1) and (a = b)) then l := 1 else l := 0;
  if (a > b) or ((gi = 1) and (a = b)) then g := 1 else g := 0
end;
```

(b)

```
procedure Add(p, q, ci : B; var s, co : B);
var   u : B;
begin
  u := p xor q;
  s := u xor ci;
  co := p and q or ci and u
end;
```

(c)

```
procedure Adder_83(P, Q : r4; CI : B; var S : r4; var CO : B);
var   j  :  byte;
begin
  for j := 0 to 3 do
  begin
    Add(P[j], Q[j], CI, S[j], CO);
    CI := CO
  end
end;
```

(d)

Listing 5

```
procedure JK1(C, R, J, K : B; var Q : B; var f : boolean);
  {  Pulse-triggered JK flip-flop with reset at R = 0  }
var    u : byte;
begin
  if R = 0 then Q := 0
  else if (C = 0) and f then
  begin
    u := J shl 1 or K;
    case u of
      1 : Q := 0;
      2 : Q := 1;
      3 : Q := Q xor 1
    end
  end;
  if C and R = 1 then f:= true else f:= false
end;
```

(a)

```
procedure Tab21;
  {  Display state-transition table  }
var    c  :  B;
begin
  ClrScr;
  SNet(0, 0, 0, 0, v7, v8, v9);      {  Initialize  }
  n := 0; c := 1;
  Writeln('  n      x1    x2    Q1    Q2    y');
  Writeln('___________________________________');
  Writeln;
  repeat
    c := c xor 1;                      {  Clock  }
    SNet(i1[n], i2[n], c, 1, v7, v8, v9);
    if c = 0 then
    begin
      Writeln('  ', n, '      ', i1[n], '     ', i2[n], '     ',
              v7, '     ', v8, '     ', v9);
      n := Succ(n)
    end;
  until n = 10
end;
```

(b)

Listings continued

Listing 6

```
procedure SRG_164(C, d0, d1, R : B; var Y : r8; var f : boolean);
var     d  :  B;
        i  :  byte;
begin
  if R = 0 then FillChar(Y, 8, 0)       {  Reset  }
  else if (C = 1) and f then
  begin
    d := d0 and d1;
    for i := 7 downto 1 do Y[i] := Y[i - 1];
    Y[0] := d
  end;
  if (C = 0) and (R = 1) then f := true else f := false
end;
```

Listing 7

```
procedure FFT(C, R : B; var Q : B; var f : boolean);
  {  Pulse-triggered toggle flip-flop with reset at R = 0  }
begin
  if R = 0 then Q := 0
  else if (C = 0) and f then Q := Q xor 1;
  if C and R = 1 then f := true else f := false
end;
```

(a)

```
procedure CTR_93(c1, r1, r2 : B; var Q : r4; var F : br4);
     {  Counter '93 with connection Q0-c2 (modulo 16) }
var R : 0..1;
begin
  R := r1 and r2 xor 1;
  FFT(c1, R, Q[0], F[0]);
  FFT(Q[0], R, Q[1], F[1]);
  FFT(Q[1], R, Q[2], F[2]);
  FFT(Q[2], R, Q[3], F[3])
end;
```

(b)

```
procedure CTR_93_mod_6(c1 : B; var Q : r4; var F : br4);
var R : 0..1;
begin
  R := Q[1] and Q[2] xor 1;      {  Operate modulo 6  }
  FFT(c1, R, Q[0], F[0]);
  FFT(Q[0], R, Q[1], F[1]);
  FFT(Q[1], R, Q[2], F[2]);
  FFT(Q[2], R, Q[3], F[3]);
  if Q[1] and Q[2] = 1 then      {  Complete cycle  }
  begin
    FillChar(Q, 4, 0);
    FillChar(F, 4, false)
  end
end;
```

(c)

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5-2-2-2	80 ns	25
6-2-2-2	120 ns	25
6-2-2-2	80 ns	33
7-2-2-2	100 ns	33

68040 PERFORMANCE SUMMARY

Access Clocks	*DRAM Speed*	*Frequency (Mhz)*
3-2-2-2	80 ns	25
5-2-2-2	100 ns	25
6-2-2-2	120 ns	25
5-2-2-2	80 ns	33
6-2-2-2	100 ns	33

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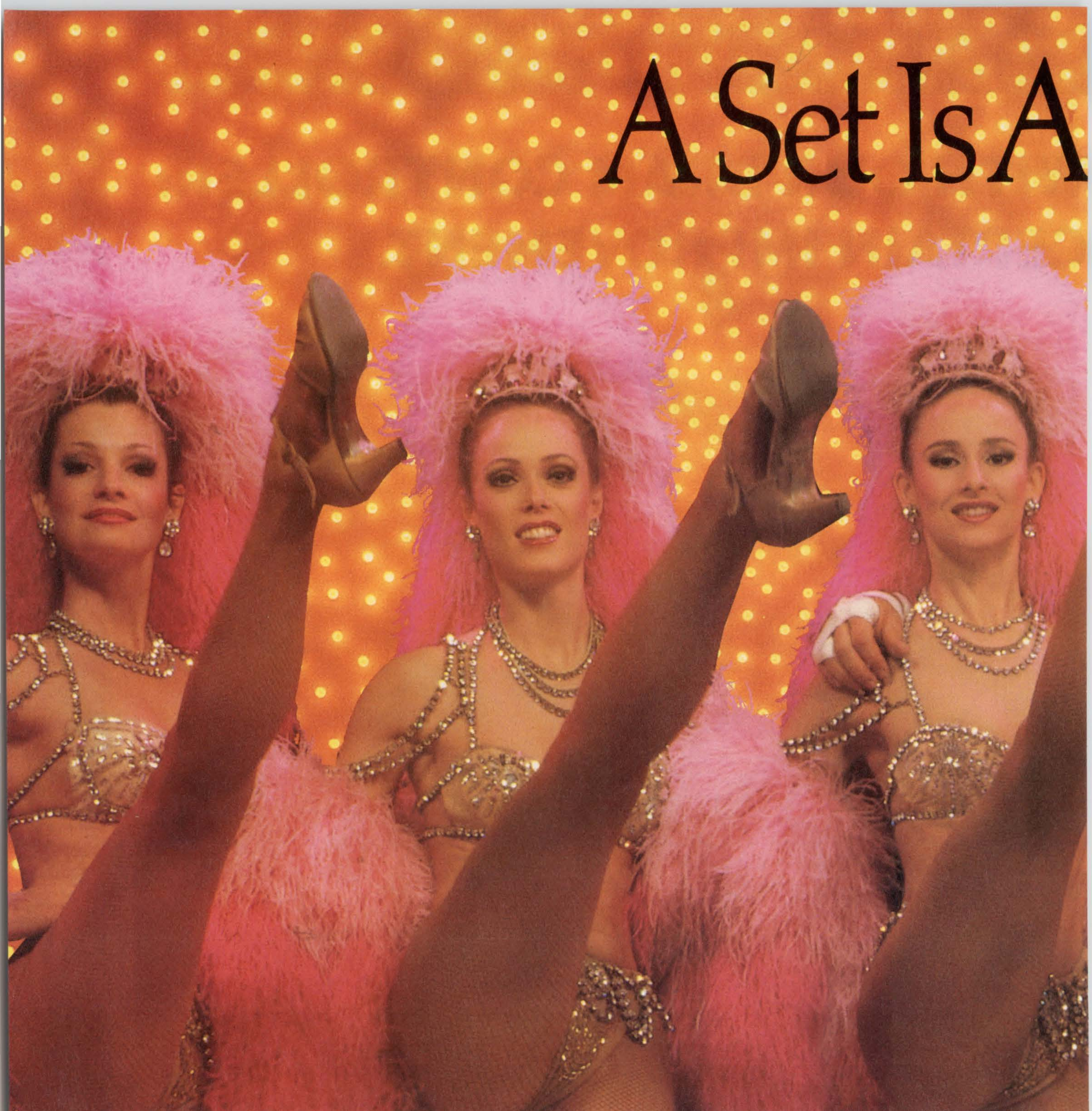

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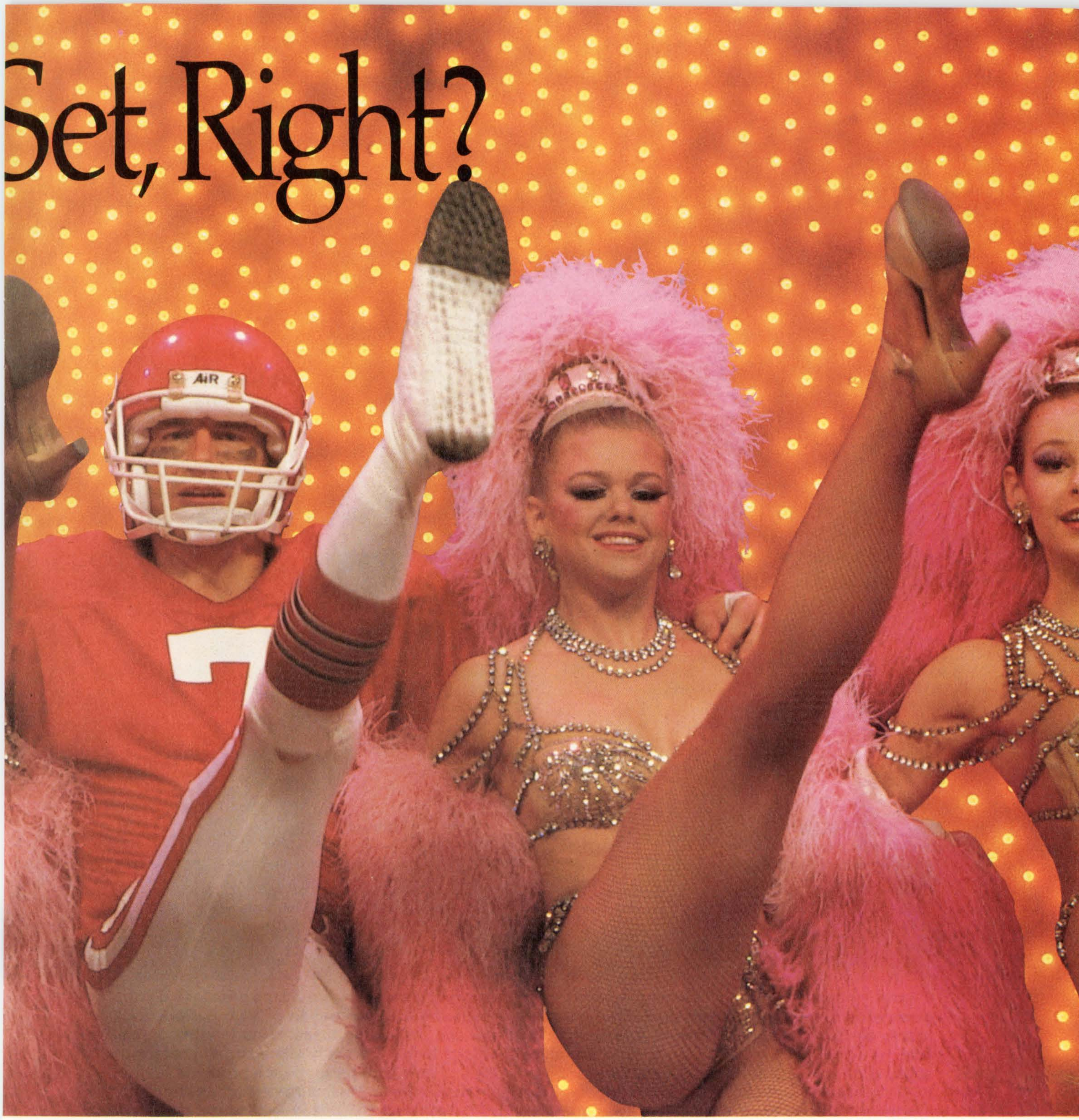

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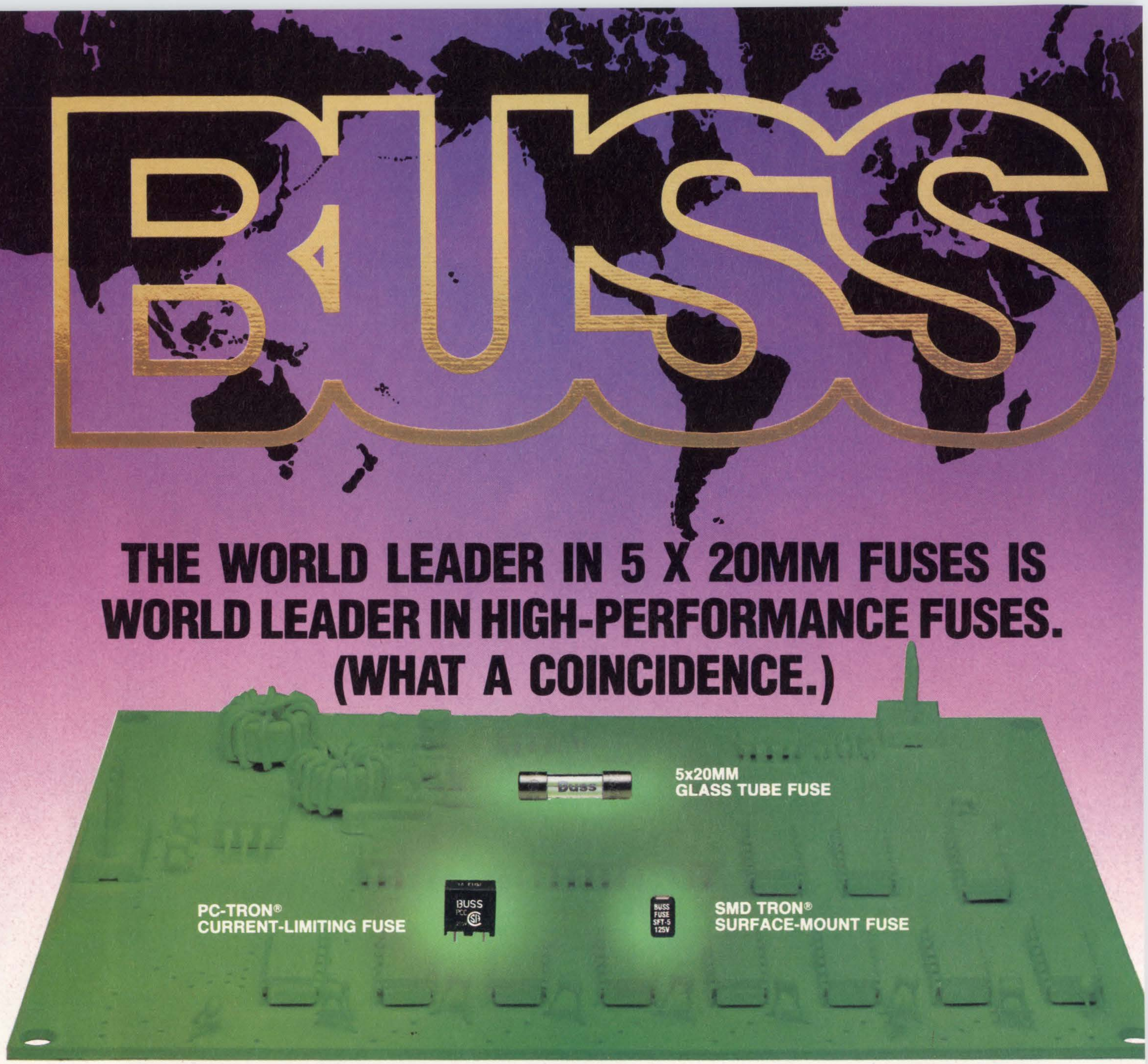

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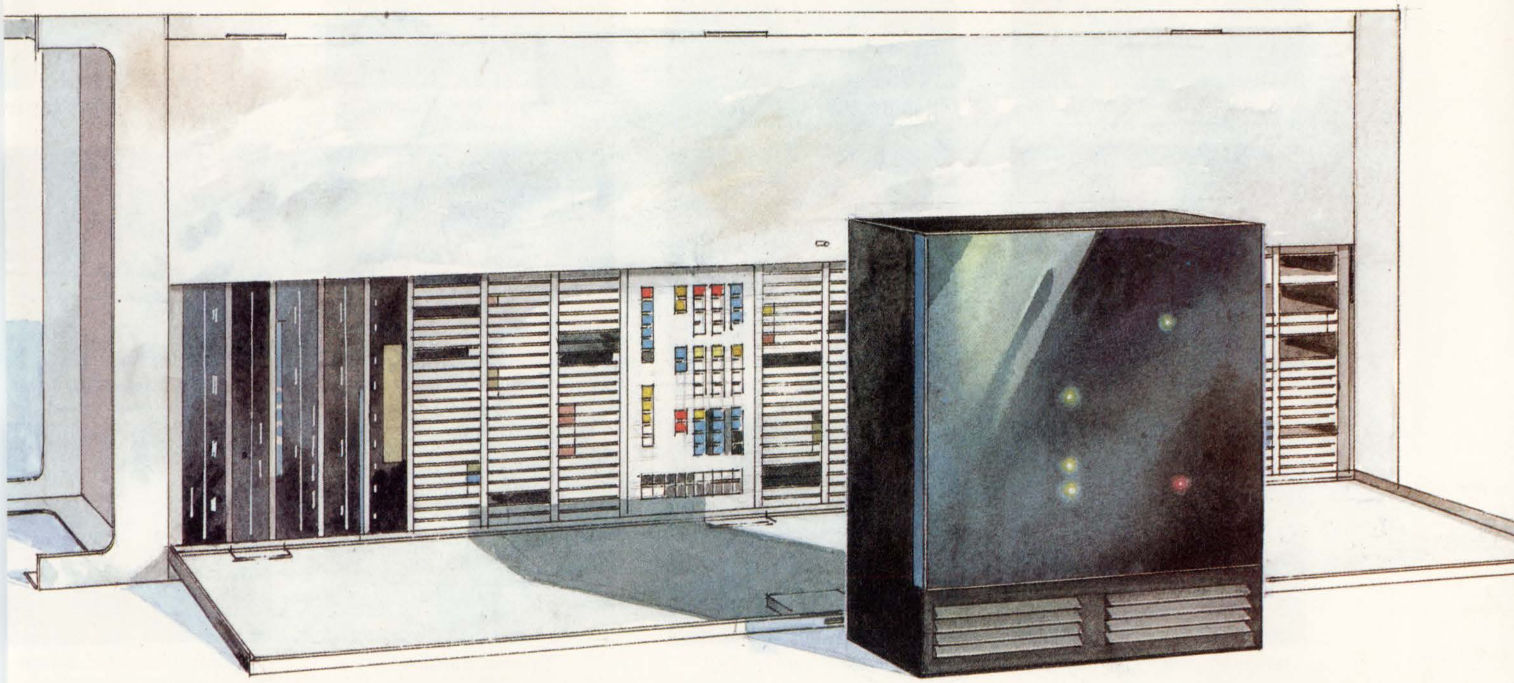

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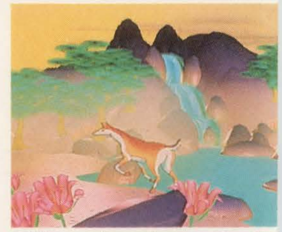

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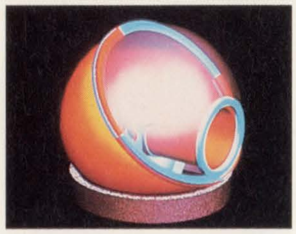
Video animation



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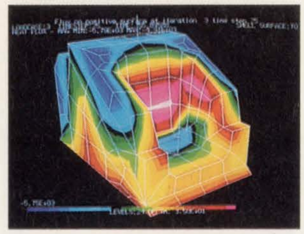
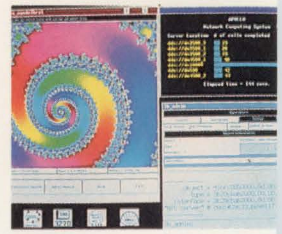


Finite element modeling and analysis



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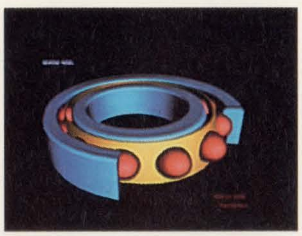

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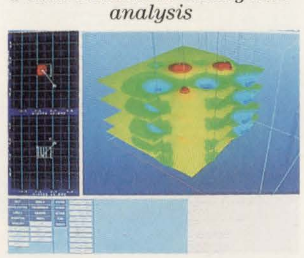

Seismic analysis

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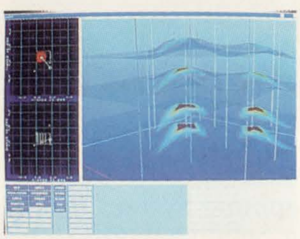
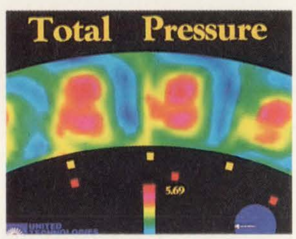


Reservoir analysis



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Industrial design

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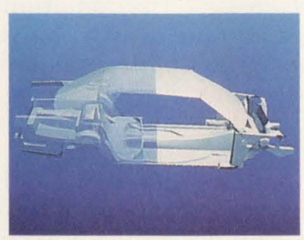
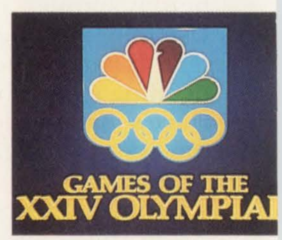
Computer-aided engineering and industrial design

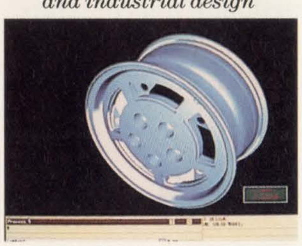
Mechanical computer-aided engineering



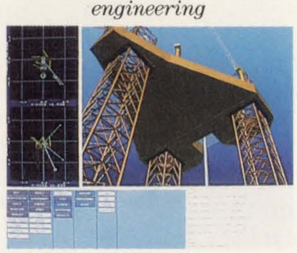
Automotive industrial design



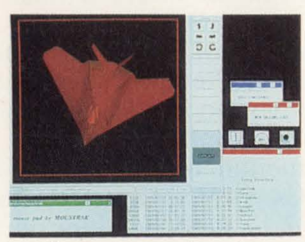
Animation



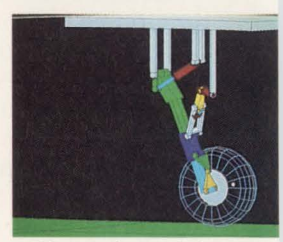
Mechanical design



Scientific visualization



Aerospace engineering



Kinematics and dynamics

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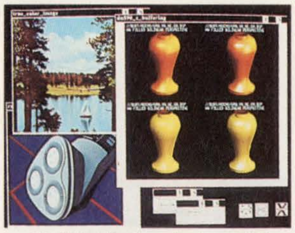
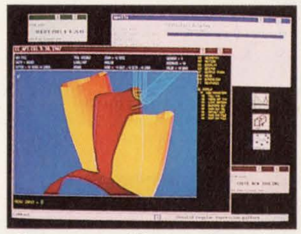
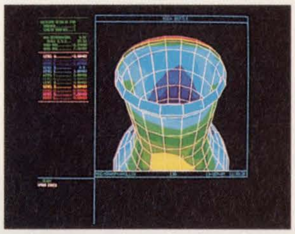


Multi-window industrial design

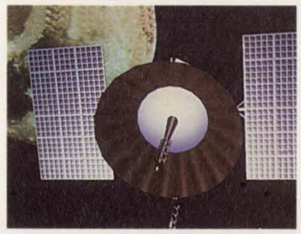


Computer-aided engineering and design

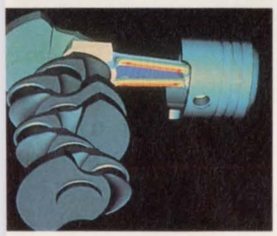
Industrial design



Structural analysis using finite element analysis



Aerospace engineering



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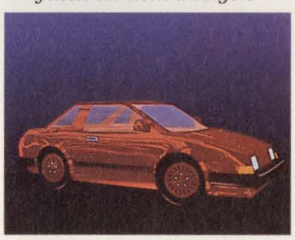
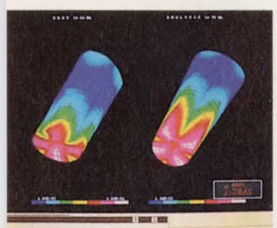
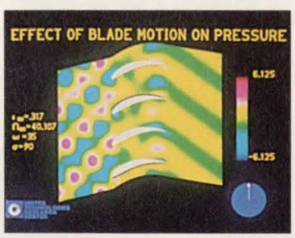


Automotive engineering

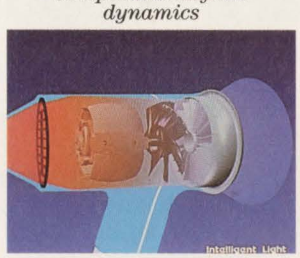
Computational fluid dynamics



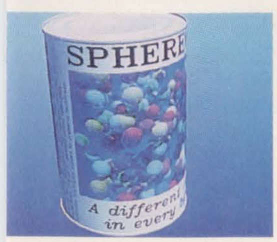
Thermal analysis



Computational fluid dynamics



Industrial design



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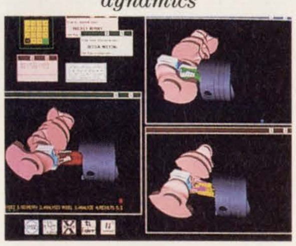
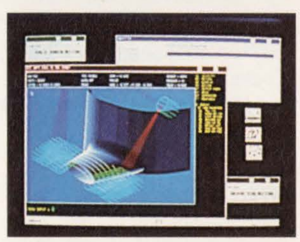


Computer-aided engineering



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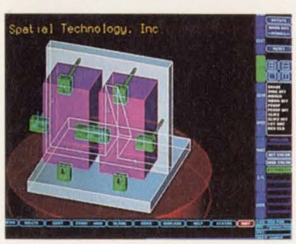
Scientific visualization



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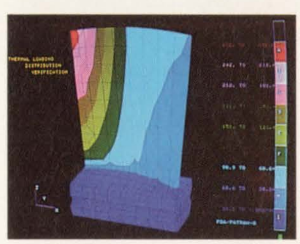

Finite element analysis

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Ninth bit keys multiple microcontrollers

K Ramamurthy, M Venkateswarlu,
and Nagender Prasad
Hindustan Aeronautics Ltd, Hyderabad, India

An obscure feature of 8051-family single-chip μPs provides the key to master-slave multiprocessor communication. Specifically, when an 8051 is in communications mode 2 or mode 3, its serial port will not raise a serial-port interrupt unless the ninth bit of an 11-bit, received serial word is set. You enable this feature by setting the SM2 bit in the chip's SCON register.

In operation, the master processor first broadcasts, over a serial link to all slave processors, the address of the slave processor it wishes to communicate with. The address word has its ninth bit set. Initially, all the slave processors have their SM2 bit set. Consequently, they will all raise an interrupt. Each slave processor's interrupt handler examines the received address word. The slave processor whose address matches the received address will clear its SM2 bit; the unaddressed slaves leave their SM2 bits set.

For as long as the master subsequently emits words with their ninth bit cleared, the addressed slave will process the words and the unaddressed slaves will ignore them. When the master sends an end-of-file sequence, the slave sets its SM2 bit.

In addition to the processors' internal software, you will need eight external connections for communication and control between the processors. You can use the single-chip μP's ports (and some additional software) or external hardware for the control functions.

Specifically, in addition to the transmit- and receive-data lines (TxD and RxD), you also need a $\overline{\text{BUSY}}$ line, a $\overline{\text{BUS\_REQUEST}}$ line, a $\overline{\text{DATA\_ACK}}$ line, and enough polling lines, P_0 through P_n, to uniquely identify 2^n slaves.

The master processor asserts $\overline{\text{BUSY}}$ whenever communication is occurring. The slave processors all use the wired-OR $\overline{\text{BUS\_REQUEST}}$ to request service. An addressed slave processor asserts its address on the polling lines, P_0 through P_n, in response to a poll by the master if that slave is requesting service. Your priorities will determine in what order the master processor polls the slaves after one or more of them request service.

Further, a communicating slave processor asserts $\overline{\text{DATA\_ACK}}$ when it successfully receives a message block from the master. If the master does not see $\overline{\text{DATA\_ACK}}$ in response to a transmitted message, the master can retransmit the message. EDN

To Vote For This Design, Circle No. 746

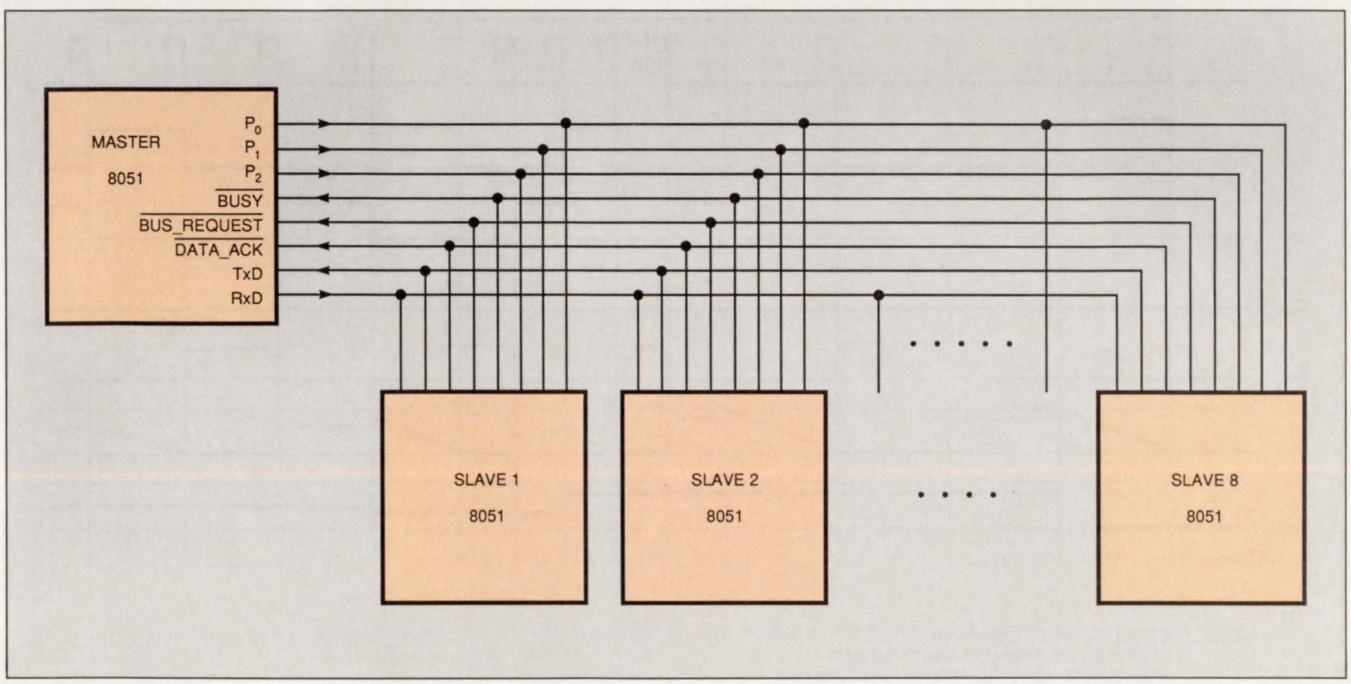


Fig 1—Combining an obscure 8051-family *communications mode and some hardware-handshake lines results in a multiprocessor master/slave communications protocol.*

Period-to-voltage converter locks quickly

Tian Jin-Qin
Shanxi Electronic Industry Research Institute, Taiyuaun, China

Unlike simple, but slow, voltage-to-frequency converters formed from monostable vibrators, the period-to-voltage converter in **Fig 1a** needs only three periods of an input signal to develop a stable output. And this circuit's output ripple does not increase with lower-frequency inputs.

Fig 1b shows the timing waveforms for the circuit. With the first pulse of the input signal, f_{IN}, at IC_1's pin 14, IC_1 resets its outputs to zero and begins counting. IC_1's Q_1 turns on S_1 in analog switch IC_2, charging

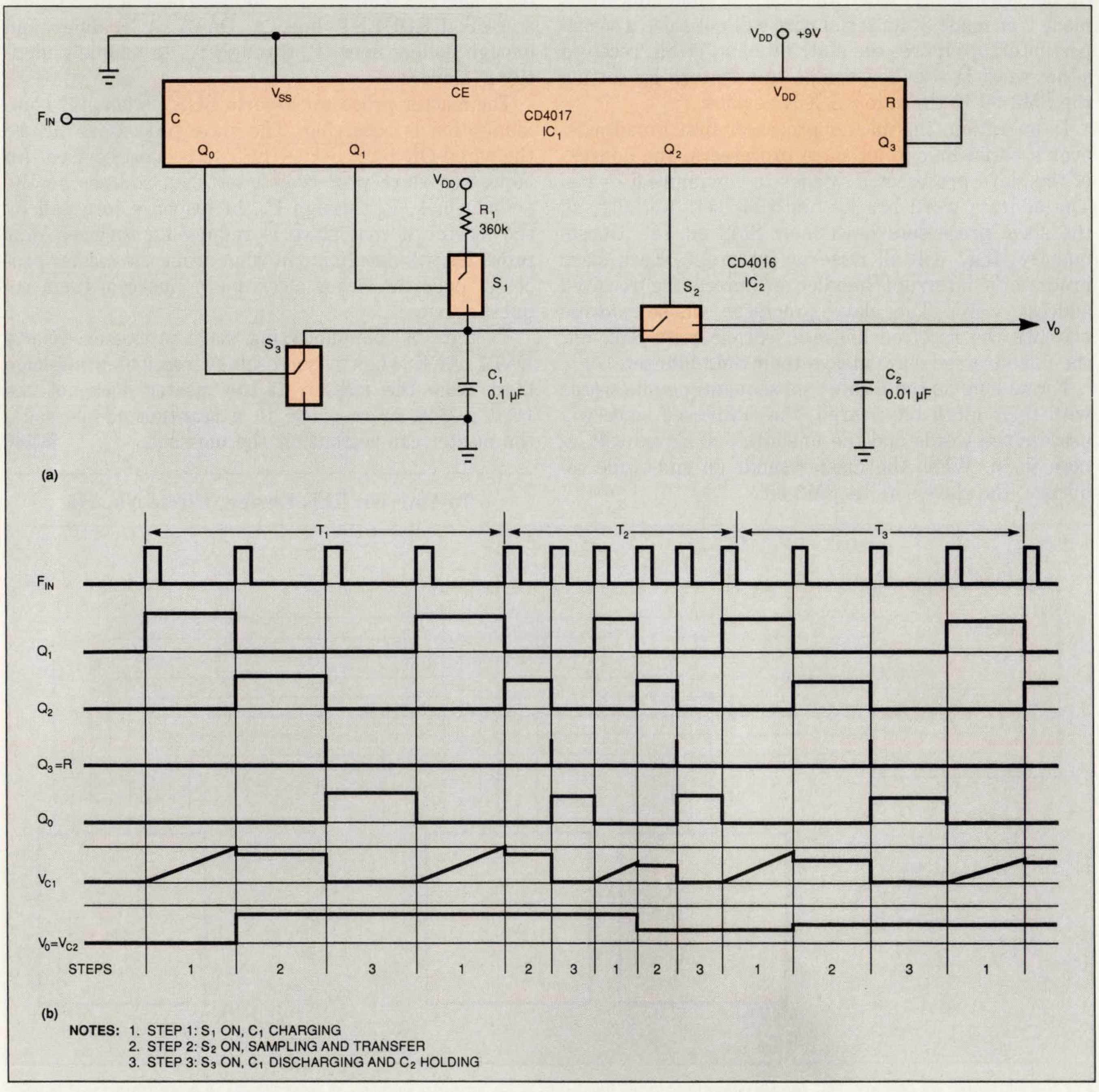


***Fig 1—This period-to-voltage converter (a)** needs only three input-signal periods **(b)** to reach a stable output.*

capacitor C_1 via resistor R_1. C_1's voltage will be proportional to S_1's on-time and f_{IN}'s period. At f_{IN}'s second pulse, S_1 turns off and S_2 turns on, transferring C_1's voltage to C_2. The third count of f_{IN} opens S_2, isolating C_2, and closes S_3, shorting C_1 to ground. C_1 is now ready to repeat the 3-pulse conversion cycle.

Obviously, you must buffer C_2 with a high-impedance amplifier. For greater precision, replace R_1 with a current source. Select C_1, C_2, and R_1 according to your input frequency. For the audio range, try $R_1 = 269\ k\Omega$, $C_1 = 0.1\ \mu F$, $C_2 = 0.01\ \mu F$, and $V_{DD} = 9V$. EDN

To Vote For This Design, Circle No. 747

Booster powers low-dropout reference

Bob Underwood
Maxim Integrated Products, Santa Clara, CA

Positioning a step-up switching regulator in front of a precision voltage reference yields a circuit with a mere 0.1V dropout voltage (**Fig 1**). Regulator IC_1's fixed 15V output easily satisfies the 13.5V minimum input that voltage reference IC_2 requires. And, by acting as a preregulator, IC_1 enhances the reference's line regulation.

The circuit supplies 100 mA while maintaining a 10.000V output from inputs ranging from 10.1 to 18V. IC_2's Kelvin connections across the load enable you to power the load via the booster transistor Q_1. Note that Q_1 connects directly to the input supply rather than to IC_1's boosted power. This setup reduces IC_1's power dissipation.

The circuit's dropout voltage depends on Q_1's saturation voltage. A medium-power npn transistor such as the 2N3054 can pass 100 mA with a V_{CE} drop of only 100 mV. Eliminating Q_1 and using the dotted-line connections improves the circuit's input voltage-range to 8 to 18V at the expense of limiting output current to ±10 mA. EDN

To Vote For This Design, Circle No. 748

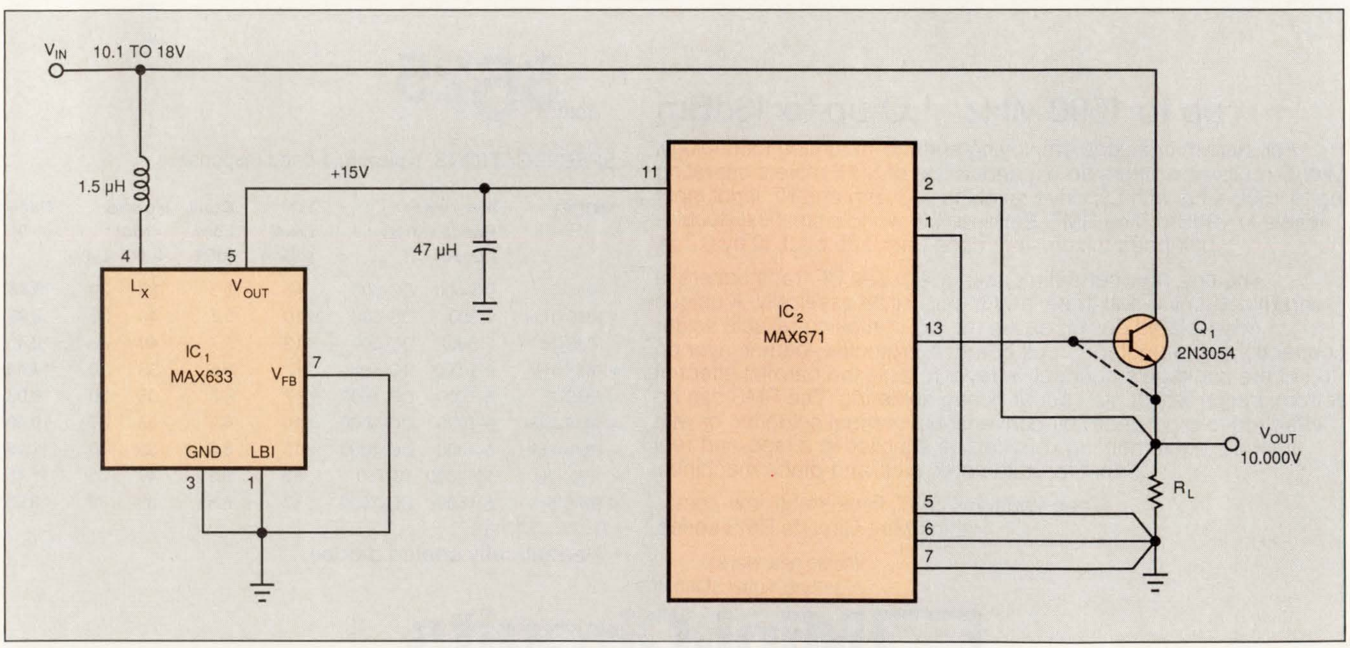


Fig 1—Showing the virtue of selectively boosting supply voltages within an analog circuit, *the 15V-output preregulator, IC_1, allows the 10.000V precision voltage source, IC_2, to operate over a 10.1 to 18V input-voltage range. Note the Kelvin connections around the load.*

CIRCLE NO. 151

Switcher babies power MOSFET

K C Herrick
ESI Electronics Corp, San Francisco, CA

The bare-bones switching regulator in **Fig 1** will deliver a selected low-voltage-dc output, at 50 mA, from a 50 to 300V dc supply. Its output ripple and noise total approximately 20 mV p-p. The circuit withstands momentary short circuits.

The power MOSFET, Q_1, free-wheel diode, D_2, and inductor, L_1, form a basic step-down switching regulator. Note that the zener diode, D_1, clamps Q_1's gate voltage to a maximum of 10V above the MOSFET's source voltage. The LED of optoisolator Q_2 is in series with voltage-setting zener diode D_3. Whenever the regulator's output voltage exceeds D_3's zener voltage (plus the LED's forward drop), Q_2 turns on. When Q_2 turns on, it shorts Q_1's gate to its source, turning the power MOSFET off.

At that point, D_2 begins to conduct and the magnetic energy stored in L_1 maintains the regulator's output. When L_1's current drops to zero, the output voltage begins to sag. When the output voltage sags low enough, Q_2 turns off, allowing the power MOSFET to conduct once more.

The key to this design is that Q_1 will turn on fully despite not having a gate-bias source. Q_1 does not conduct long enough for its source voltage to rise to the positive rail. In fact, Q_1's source rises to only 100V during its normal, rather short, on-time of approximately 1 μsec. Therefore, during conduction, Q_1's gate is always 10V above its source, turning the power MOSFET on fully.

Choose D_3's zener voltage to set your output-voltage level. You can use a power MOSFET of higher voltage rating than the IRF730 if you increase R_1's value to keep the transistor's power dissipation modest.

R_2 and R_3 limit short-circuit current to 150 mA upon momentary overloads by turning on the power MOSFET independently. Q_1 will easily withstand the resulting overload for short periods if you mount it on a heat sink. EDN

To Vote For This Design, Circle No. 749

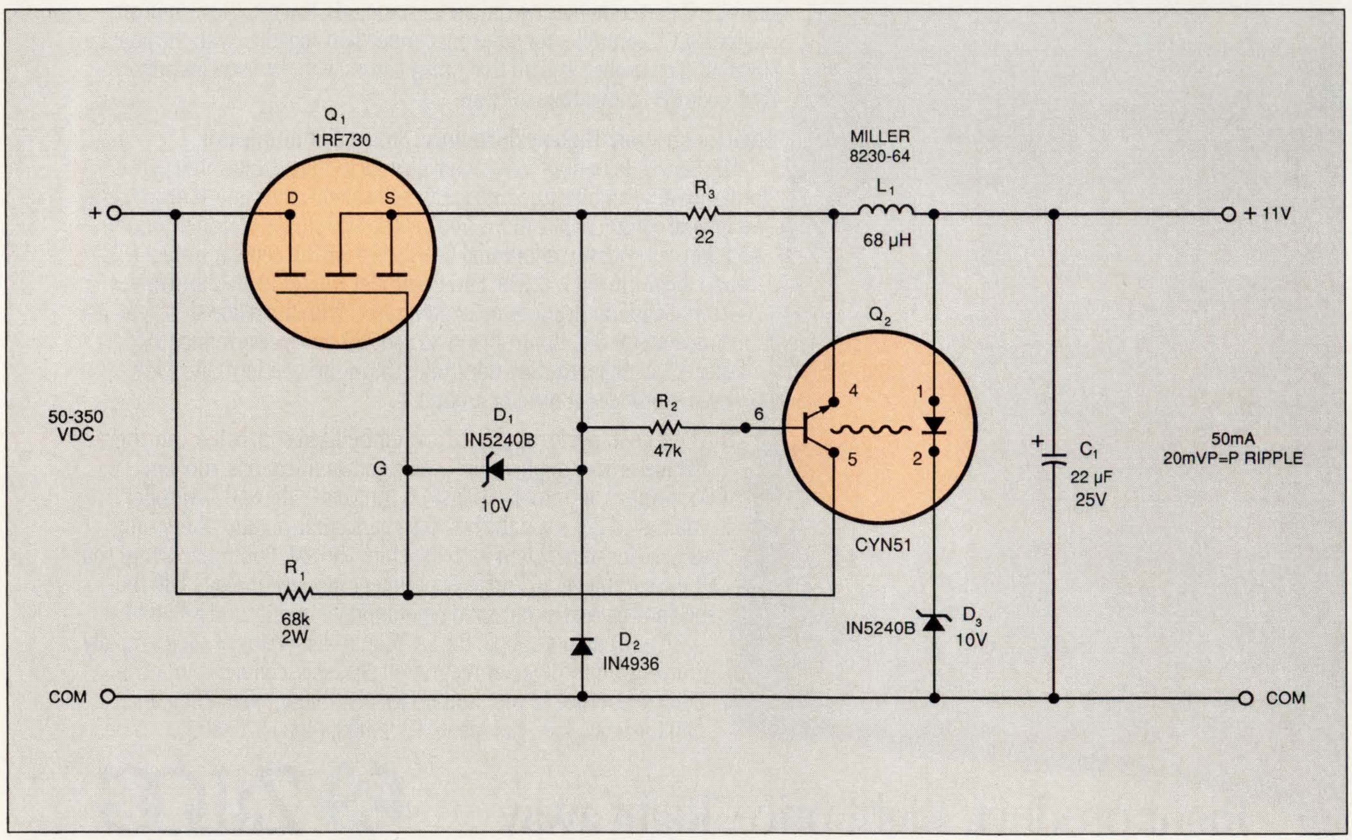


Fig 1—This simple switching regulator *needs no gate-bias circuit because its power transistor's short conduction period keeps its source from ever rising to the positive rail.*

ISSUE WINNER

The winning Design Idea for the May 24, 1990, issue is entitled "Current sink widens VCO's frequency range," submitted by Antonio Tagliavini of Applicazioni Digitali e Analogiche (Bologna, Italy).

ISSUE WINNER

The winning Design Idea for the June 7, 1990, issue is entitled "Mapper flags dead code," submitted by Brian P Courtnage and Theo A De Oliveira of Telephone Manufacturers of SA (Johannesburg, South Africa).

PAL enables DIP-switchless addressing

Robert K Breuninger
Texas Instruments, Dallas, TX

Using one level of hardware indirection, you can configure a software-programmable address decoder with a 16L8 PAL device and a 74ALS6311A (**Fig 1**). Don't confuse the circuit with a hard-wired PAL-device decoder; the 16L8 does not generate the enable signals, EN and $\overline{EN}$, directly. Instead, the PAL device decodes an address that enables you to program the 6311A's 14 D-type registers. Once programmed, the 6311A compares input addresses to its internal registers and asserts the enable signals when it sees a match. EDN

To Vote For This Design, Circle No. 750

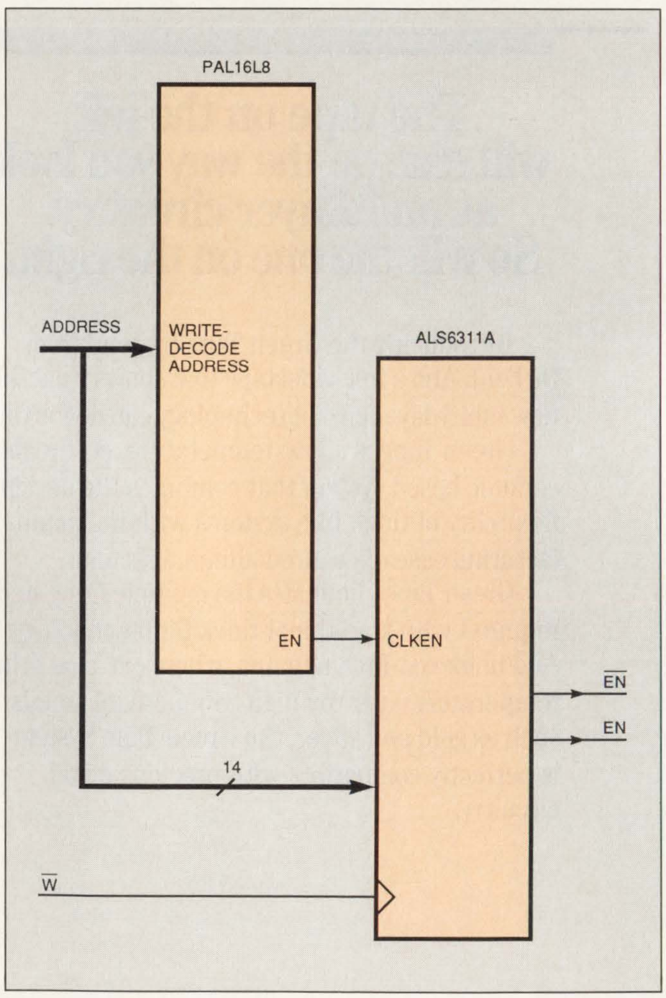
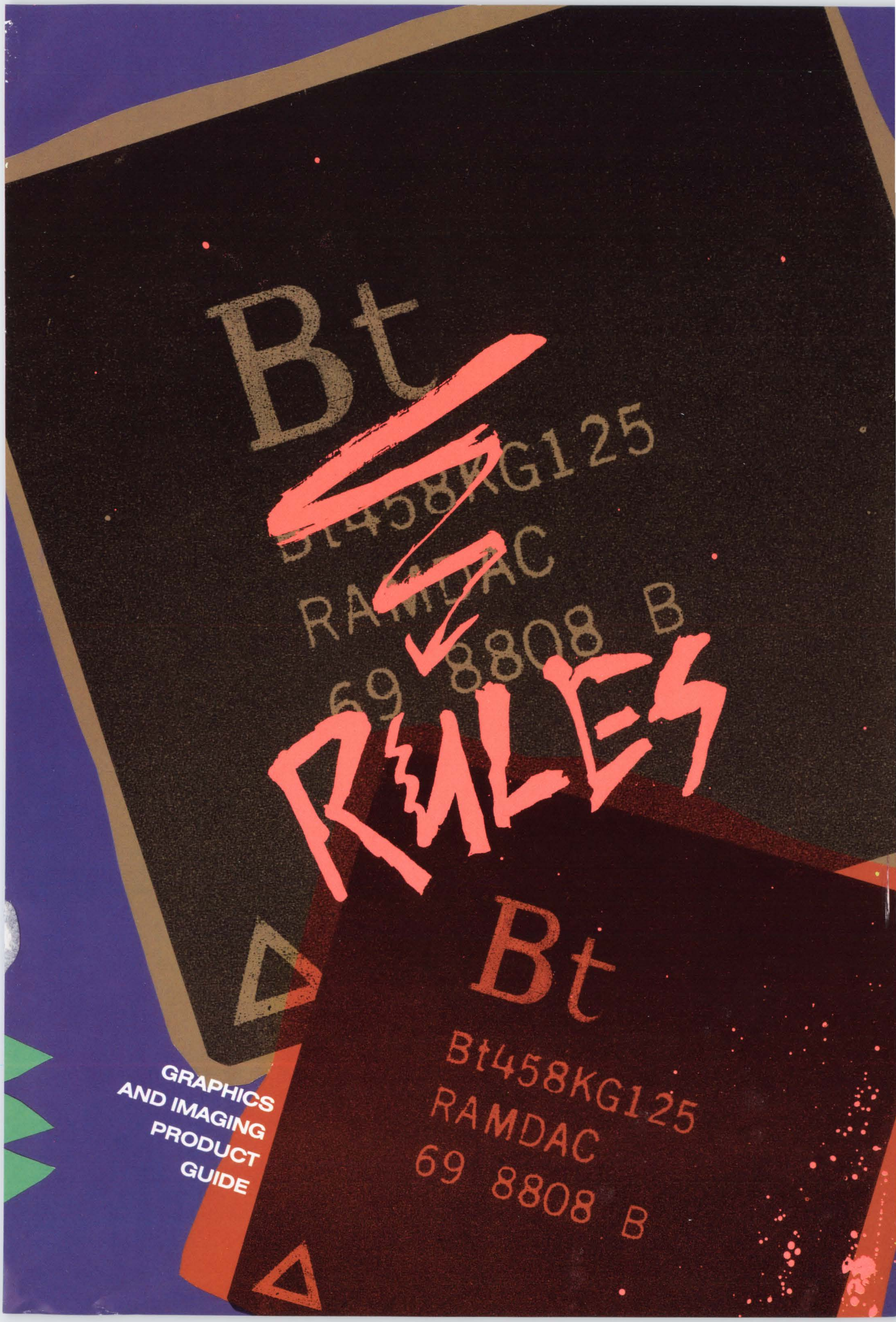


Fig 1—This 2-chip circuit comprises a DIP-switchless, programmable, address decoder.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PART NUMBER	CLOCK RATE (MHz)	D/A ORGANIZATION	RAM SIZE	OVERLAYS	COMMENTS	PACKAGE
Bt450	66, 50, 30	triple 4-bit	16 x 12	3 x 12	Dual-port RAM and overlays.	28-pin 0.6″ CERDIP
Bt451	125, 110, 80	triple 4-bit	256 x 12	4 x 12	Pin compatible with Bt457 and Bt458.	84-pin Ceramic PGA 84-pin PLCC
Bt453	66, 40	triple 8-bit	256 x 24	3 x 24	First triple 8-bit RAMDAC.	40-pin 0.6″ Plastic PGA 44-pin PLCC
Bt454	170, 135, 110	triple 4-bit	16 x 12	1 x 12	Multiplexed pixel ports.	44-pin PLCC
Bt455	170, 135, 110	single 4-bit	16 x 12	1 x 12	Multiplexed pixel ports.	44-pin PLCC
Bt457	125, 110, 80	single 8-bit	256 x 8	4 x 8	Pin compatible with Bt451 and Bt458.	84-pin Ceramic PGA 84-pin PLCC
Bt458	165, 125, 110, 80	triple 8-bit	256 x 24	4 x 24	Multiplexed pixel ports.	84-pin Ceramic PGA 84-pin PLCC
Bt459	135, 110, 80	triple 8-bit	256 x 24	16 x 24	On-chip three-color cursor.	132-pin Ceramic PGA 132-pin Plastic Quad Fltpk
Bt460	135, 110, 80	triple 8-bit	512 x 24	16 x 24	512 x 24 color palette.	132-pin Ceramic PGA
Bt461	170, 135, 110, 80	single 8-bit	1024 x 8	32 x 8	256 x 8 alternate color palette.	132-pin Ceramic PGA
Bt462	170, 135, 110, 80	single 8-bit	1024 x 8	32 x 8	256 x 8 alternate color palette.	132-pin Ceramic PGA 132-pin Plastic Quad Fltpk
Bt468	200, 170	triple 8-bit	256 x 24	16 x 24	8:1 multiplexed inputs.	145-pin Ceramic PGA
Bt471	80, 66, 50, 35	triple 6-bit	256 x 18	15 x 18	Bt478 pin compatible	44-pin PLCC
Bt473	80, 66, 50, 35	triple 8-bit	(3) 256 x 8	(3) 15 x 8	True-color RAMDAC.	68-pin PLCC
Bt474	85, 66	triple 8-bit	256 x 24	15 x 24	4:1 mux w/ VGA pass-through	84-pin PLCC
Bt475	80, 66, 50	triple 6-bit	256 x 18	15 x 18	Power-down RAMDAC.	44-pin PLCC
Bt476	80, 66, 50, 35	triple 6-bit	256 x 18	—	Pin compatible with IMSG176*.	44-pin PLCC 28-pin 0.6″ Plastic DIP
Bt477	80, 66, 50	triple 6/8-bit	256 x 24 (18)	15 x 24 (18)	Power-down RAMDAC.	44-pin PLCC
Bt478	80, 66, 50, 35	triple 8-bit	256 x 24	15 x 24	6-bit mode.	44-pin PLCC
Bt479	80, 66, 50, 35	triple 8-bit	1024 x 24	15 x 24	16 window priority encoder.	44-pin PLCC
Bt492	360	single 8-bit	256 x 8	16 x 8	2:1 multiplexed inputs.	68-pin Ceramic PGA w/ Alignment Pin & Heatsink

VIDEODACS

PART NUMBER	CLOCK RATE (MHz)	D/A ORGANIZATION	COMMENTS	PACKAGE
Bt121	80, 66, 50, 35	triple 8-bit	Monolithic CMOS. On chip Vref and output comparators.	44-pin PLCC
Bt102	75	single 8-bit	Monolithic CMOS. 0, 7.5 or 10 IRE blanking pedestal.	24-pin 0.3″ CERDIP
Bt103	75, 30	triple 4-bit	Monolithic CMOS.	28-pin 0.6″ CERDIP
Bt106	50, 30	single 8-bit	Monolithic CMOS.	20-pin 0.3″ CERDIP
Bt107	400	single 8-bit	0 or 7.5 IRE blanking pedestal. 2:1 multiplexed pixel inputs.	32-pin Ceramic Flatpack w/Heatsink
Bt109	250	triple 8-bit	10KH ECL compatible. TDC1318 pin compatible.	40-pin 0.6″ Ceramic Cavity Down DIP

*IMS is a trademark of INMOS Corporation.

RULE #1. THERE ARE NO RULES.

At Brooktree, we set standards by breaking rules. For us, "conventional wisdom" is oxymoronic.

Like, **who says?** you can't create high speed, highly integrated monolithic ICs that marry analog and digital circuitry?

Why not? put the DAC on the RAM and create a whole new class of video ICs?

How come? CMOS can't be pushed to 200 MHz? Or beyond?

Why shouldn't? desktop systems be able to economically display 16 million colors at 1600x1280 pixel resolution?

Where's it written? that an IC company can't accomplish system-level integration, putting windowing, input shift registers and four separate color look-up tables onto a triple 8-bit VGA RAMDAC?

On the following pages, there are 47 fine examples of where this kind of thinking has gotten us. In fact, we created this convenient graphics and imaging resource guide to prove our point. Sure, it's an easy-to-keep, quick reference to the full range of Brooktree ICs. But it's also living proof that good things happen when you shed conventional thinking.

If we're going to push designers to use higher and higher performance components, we feel some responsibility for making it possible to test them. So we've included our exciting ATE devices in this brochure, too.

ATE PRODUCTS

PIN TIMING

PART NUMBER	COMMENTS	PACKAGE
Bt604	Dynamically Programmed Timing Edge Vernier. 15 ps resolution. 10KH ECL compatible.	28-pin PLCC
Bt605	Programmable Timing Edge Vernier. 15 ps resolution. 10KH ECL compatible.	28-pin PLCC
Bt622	Dual Channel Delay Line. Leading and trailing edge independently adjustable.	28-pin PLCC
Bt624	Quad Channel Delay Line. Leading and trailing edge independently adjustable.	44-pin PLCC

PIN ELECTRONICS

PART NUMBER	COMMENTS	PACKAGE
Bt681	Ultra Fast, High Voltage (+8v, −4v) Comparator. Input power down and level select features.	28-pin PLCC
Bt687	Ultra Fast ECL Dual Comparator. Pin compatible to industry standard '687 devices.	16-pin SOIC 16-pin CERDIP 20-pin Ceramic Leadless Chip Carrier
Bt688	High Speed Dual Comparator. Wide input voltage (+8v, −2v). 10KH ECL compatible. Pin compatible to industry standard '687 devices.	16-pin SOIC 16-pin Plastic DIP
Bt689	Pin Electronics Load or Driver. >100 MHz operation. 10KH ECL compatible.	32-pin Ceramic Flatpack w/Heatsink 44-pin PLCC

SUPPORT PRODUCTS

PART NUMBER	COMMENTS	PACKAGE
Bt110	100 ns, Octal 8-bit DAC. Standard MPU bus interface. Monolithic CMOS.	44-pin Plastic J-Lead
Bt501	10KH Octal ECL/TTL Bidirectional Transceiver/Translator.	24-pin 0.3″ CERDIP
Bt502	100K Octal ECL/TTL Bidirectional Transceiver/Translator.	24-pin 0.3″ CERDIP

Bt468, the fastest CMOS RAMDAC yet, 200 MHz!

Bt622/624, very high speed delay lines, perfect for ATE and CPU system timing!

systems!

IMAGING PRODUCTS

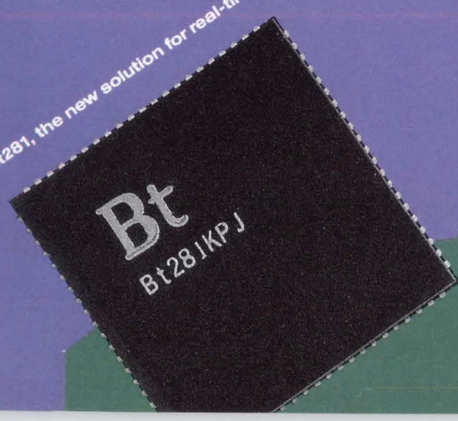
PART NUMBER	SPEED	A/D ORGANIZATION	COMMENTS	PACKAGE
Bt208	18 MSPS	single 8-bit	Flash Converter. Monolithic CMOS. On-chip reference and DC restoration.	24-pin 0.3″ Plastic DIP
Bt251	18 MSPS	single 8-bit	Single Channel Image Digitizer. Single 8-bit flash A/D, sync detect circuitry, adjustable gain/offset, 4:1 analog mux, lookup table RAM.	44-pin PLCC
Bt253	18 MSPS	triple 8-bit	Triple Channel Image Digitizer. Three 8-bit flash A/Ds, sync detect circuitry, adjustable gain/offset, 2:1 analog mux, flexible color output formats.	84-pin PLCC
Bt261	30 MHz	—	MPU programmable video timing parameters, sync noise gating. Video or TTL sync inputs.	28-pin PLCC
Bt281	36 MHz	—	3 x 3 matrix multiplier with MPU programmable coefficients, lookup table RAMs, optional 16-bit color format I/O capability.	84-pin PLCC

GRAPHICS PERIPHERAL PRODUCTS

PART NUMBER	CLOCK RATE (MHz)	COMMENTS	PACKAGE
Bt424	250	40-bit multi-tap shift register. 10KH ECL/TTL compatible.	68-pin Ceramic PGA w/ Alignment Pin
Bt431	35 MHz per 5 pixels	Cursor generator. 64 x 64 user definable cursor, cross hair cursor. Monolithic CMOS. 175 MHz pixel rates.	24-pin 0.3″ CERDIP 28-pin PLCC
Bt438	250	Clock generator chip for CMOS RAMDACs up to 250 MHz	20-pin 0.3″ CERDIP 28-pin PLCC
Bt439	200	Clock generator/synchronizer chip for single-channel 80+ MHz CMOS RAMDACs.	28-pin 0.6″ CERDIP

RULE #2. SEE RULE ONE.

Bt281, the new solution for real-time color space conversion!



Bt261, the HSYNC genlock answer for video capture

SOURCEGATE

integrating high level language debugging with in-circuit emulators.

SourceGate is a window driven high level language debugger designed to support the Huntsville Microsystems 200 series of in-circuit emulators.

- User configurable windows can be sized, moved and duplicated anywhere on the screen.
- Code can be viewed in all displays (trace, single step, etc.) in one of three modes: Source only, Assembly only or both Source and Assembly.
- Watch windows display and monitor code variables.
- Optional Performance Analysis Card for real-time software performance analysis and real-time software test coverage.
- Available for IBM PC family and UNIX systems including Apollo and SUN.

For more complete technical information, write to Huntsville Microsystems Inc., 4040 South Memorial Parkway, Huntsville, AL 35802 or call (205) 881-6005.

IBM is reg. T.M.
International Business Machines, Inc.
Unix is reg. T.M.,
Bell Laboratories, Inc.

Available Emulators

8051 Family	68HC11 Family including F1 and D3
DS5000	68000
8096/80196	68008
Z80	68010
64180/Z180	68020
8085	68030
6809/6809E	68302

HMI

CIRCLE NO. 152

C A D R E

The Ultimate 386 Debugger.

Terminate difficult debug problems fast. And do it remotely. From your Ethernet®-based workstation you're now in total control with the new **386 SmartProbe**™ from CADRE.

Think of it. Your favorite Sun™ or VAX™ software development environment now controls your 386 hardware environment. Develop programs on your Sun or VAX. Download via Ethernet to the 386 SmartProbe. Execute in real-time and start eliminating problems fast. And the best part is, you control the entire process without ever leaving your desk.

You'll call the 386 SmartProbe the ultimate 386 development tool because we've included all of the high performance features you need for rapid hardware/software integration and test.

386 SmartProbe includes comprehensive hardware and software breakpoints, source-level debug capability for C and ADA,® sophisticated single stepping facilities and, of course, full-speed transparent emulation to 25 MHz. It even supports the development of protected mode programs.

So get the ultimate 386 debugger. The one designed to work with your favorite tool: your workstation. Call **1-800-283-5933** for more information about 386 SmartProbe and other CADRE Unified CASE products.

CADRE
SARATOGA DIVISION

Saratoga Office Center
12950 Saratoga Avenue
Saratoga, CA 95070

CIRCLE NO. 153

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• Sun is a trademark of Sun Microsystems.
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• Ada is a registered trademark of the Dept. of Defense.
• Ethernet is a trademark of Xerox Corporation.

16-bit PC/AT Data Acquisition from Analogic!

LSDAS-16 Brings New Price/ Performance Levels to PC Instrumentation

The new LSDAS-16 from Analogic sets new price/ performance standards for 16-bit multifunction data acquisition plug-in boards for the IBM PC/AT™ and compatibles, including:

- 16-bit 50 kHz A/D converter
- 16 analog inputs
- Shielded for less than 1 LSB of noise *in the PC*
- Programmable input modes and ranges
- Full analog triggering
- Dual deglitched DACs
- 32K-sample DAC RAM
- High speed DMA
- Menu-driven setup and data acquisition utilities
- C, Basic, FORTRAN, and Pascal libraries
- Third party support for Snapshot Storage Scope™, DADiSP™, and LabTech Notebook™
- Expansion multiplexers for up to 256 analog inputs
- Prices starting at $1,395 in unit quantities, with volume discounts available.

For applications from spectroscopy and chromatography to digital audio and speech analysis, step up to Analogic, the world leader in precision data conversion technology for more than 20 years.

For Applications Assistance, call or write David Wilson,
Analogic Corporation, 360 Audubon Road, Wakefield, MA 01880
Telephone: (800) 446-8936, Telex: 466069, Fax: (617) 245-1274

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ANALOGIC®
The World Resource for Precision Signal Technology

CIRCLE NO. 154


MC145407 DRIVER/RECEIVER
Low Power CMOS Technology
Three Drivers, Three Receivers
On-Chip Slew Rate Limiting
MC145407
On-Chip Charge Pump
Latch-Up Proof
Single 5 Volt Suppl

The five-volt standard.

MC145407 combines 3 drivers, 3 receivers and a charge pump on a single 5-volt CMOS chip. Try a free sample.

Motorola pioneered the EIA-232 market four years ago with the introduction of the first CMOS-based EIA-232 driver/receiver. That device, the MC145406, has become the industry standard with over 20 million units in operation. Now Motorola does it again by introducing the five-volt standard, the MC145407.

The MC145407 combines three drivers, three receivers and an on-board five volt charge pump to meet EIA-232 and CCITT V.28 specifications. Anyone designing computer or communication equipment such as digital telephones, portable computers or line-powered modems will appreciate our low power requirement.

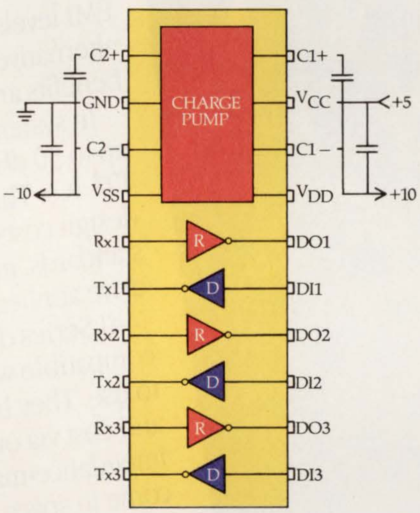
Charge pumps and more.

There's features to make your design tasks easier. The on-board charge pump generates ±10 volts from a single 5 volt power supply for driving the on-board receivers and drivers plus additional peripheral devices.

The Slew Rate Transition Signal offers clean, bounce-free operation through the entire threshold region.

You also get a typical 2Kv per I/O pin of ESD protection, with a latch-up-free design and advanced CMOS technology.

The three receivers offer true TTL capability without external capacitors, and feature impedance over a 3-to-7 kilohm range while handling up to ±25 volts.



D = Driver
R = Receiver

MC145407 Pin Assignment

The obvious choice.

The MC145407 is the perfect choice. It provides all the necessary level-shifting between TTL logic levels and high-voltage EIA-232 equipment. It's the smart decision for applications like lap-top computers, printers, modems, PABXs, remote telebanking, key systems, multiplexes, limited distance modems, and computer networks.

Try a free sample.

The only way to fully appreciate the new MC145407 is to try one. You can get a free sample, along with all the supporting literature you need, by simply filling out and returning the coupon below. Send it to Motorola Semiconductor Products, Literature Distribution Center, P.O. Box 20912, Phoenix, AZ 85036. Or call toll-free any weekday, 8:00 a.m. to 4:30 p.m. (MST) 1-800-521-6274.

Winner 1988 Malcolm Baldrige National Quality Award

MOTOROLA

To: Motorola Semiconductor Products, Literature Distribution Center, P.O. Box 20912, Phoenix, AZ 85036

☐ Please send me the MC145407 sample kit. EDN091790

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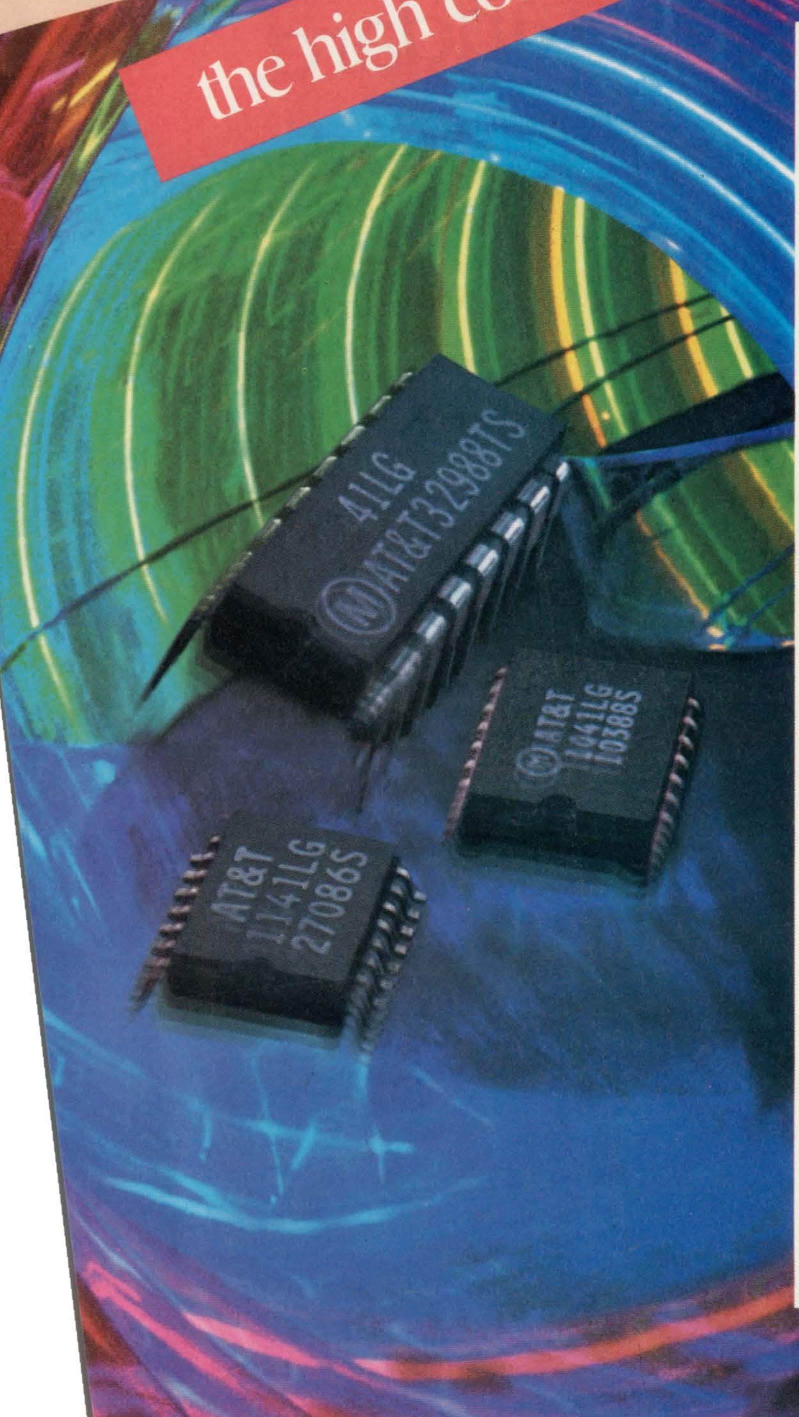
Address ______

City ______ State ______ Zip ______

Call me (______) ______

AT&T's new datacom ICs take the high cost out of high speed.



AT&T's new 41 Series of differential quad line drivers/receivers and dual transceivers reach 400 Mb/s with substantially reduced EMI.

Our new datacom ICs do more than offer one of the industry's highest data rates and shortest propagation delays.

Their unique design can take you to 400 Mb/s on common twisted pair—at low EMI levels. This makes them an affordable alternative to fiber, when fiber's other benefits aren't needed.

In system use, they decrease EMI levels up to 30 db compared with standard 26LS TTL ICs. This sharply reduces cabinet design costs. And they meet ESDI standards, making them ideal for disk drive applications.

41 Series devices are pin-for-pin compatible with 26LS ICs—so they're easy to use. They help reduce board complexity and cost via on-chip termination and line-impedance-matching resistors. And they come in space-efficient, surface-mount SOJ and SOIC packages as well as standard DIPs.

Not exactly what you need? Create your own custom version quickly and easily by using our standard cell library.

Call **1 800 372-2447** for our databook on 41 Series components, in stock today at Hamilton/Avnet and Schweber.

The components of success.

AT&T
The right choice.

CIRCLE NO. 155

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

Transient-Waveform Recorder

- *Uses IBM PC for control*
- *Samples two, four, or eight channels at 100-nsec intervals*

The SDA2000A transient-waveform recorder uses an IBM PC-compatible computer for control. The recorder can capture data and simultaneously place it on the IEEE-488 bus at 1M byte/sec for further processing by the PC. The vendor can configure the unit with two, four, or eight channels. By using multiple units, you can create systems with as many as 64 channels. Resolution is 12 bits, and the minimum sampling interval is 100 nsec. The device features 33 programmable-gain ranges that cover 50 mV to 80V. $9995.

Soltec Corp, 12977 Arroyo St, San Fernando, CA 91340. Phone (800) 423-2344; in CA, (818) 365-0800. FAX (818) 365-7839.

Circle No. 351

4-Channel, 500-MHz Amplifier/Attenuator

- *Has 100-μV sensitivity*
- *Has 200 μV sensitivity with 1-MΩ impedance*

The 2004A 4-channel, 500-MHz amplifier/attenuator is a VMEbus module that works with the vendor's waveform digitizers. At a 50Ω input impedance, it has 100-μV sensitivity, a 500-MHz bandwidth, and gains from 0.01 to 10. With a 1-MΩ input impedance, its bandwidth is 250 MHz, its sensitivity is 200 μV, and its gains are 0.02 to 5. DC offset is programmable, maximum output is 17 dBm, and distortion is −45 dBc (dB below carrier) at 250 MHz. $3950. Delivery, 10 weeks ARO.

Analytek/Tektronix, 365 San Aleso Ave, Sunnyvale, CA 94088. Phone (800) 835-9433; in CA, (408) 745-1114. FAX (408) 745-1894.

Circle No. 352

Dynamic-Signal Analysis Software

- *Displays data in time and frequency domains*
- *Display marks each harmonic through the ninth*

ZPA1000 dynamic-signal analysis software converts an IBM PC-compatible computer equipped with the vendor's ZPB34-004 DSP board and one or more data-acquisition cards into a low-frequency digital oscilloscope, a histogram analyzer, and an FFT spectrum analyzer. The histogram function is useful in characterizing the integral and differential nonlinearity of A/D and D/A converters. With the FFT capability, you can characterize such converters for digital-audio applications; the display marks each harmonic through the ninth. The vendor supplies compatible A/D converters that serve as input devices. Among such units are a 12-bit converter that takes 10M samples/sec and a 16-bit converter that takes 150k samples/sec. $995; DSP board, $4995.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132.

Circle No. 353

Experiment-Control-And-Analysis Software

- *Performs math on waveforms*
- *Lets you define experiments*

DataWave software lets you use your 80286- or 80386-based IBM

Why your best choice for SCSI-II connectors may not be a connector company at all.

If you need SCSI-II connectors, you can buy them from a company that makes connectors. But an even better idea may be to buy your SCSI-II connectors from a company that makes computers.

Last year we made about $10 billion worth of computers and peripherals. Ranking us among the top four computer manufacturers in the world. And every Fujitsu computer was chock full of Fujitsu connectors.

Our reputation for quality and reliability depends on the reliability of every single component including connectors.

So we've learned to make components of uncompromising quality. And we've learned that the best way to make them economical for our own systems is to supply them at reasonable prices to companies like yours as well.

Today, components—along with computers and communications—are an important part of our $16 billion annual sales.

So when you need connectors, even hard-to-find connectors like half-pitch SCSI-II PCB-to-cable connectors, your best supplier may be a connector company that's also something more.

FCN-230 SERIES CONNECTORS

ITEM:	SPECIFICATIONS:
Operating Temperature	−55°C to +105°C
Current Rating	1 ADC
Voltage Rating	240VAC
Contact Resistance	30mΩ max. at 6VDC, 0.1A
Insulation Resistance	1000MΩ min. at 500VDC
Dielectric Strength	750VAC for 1 minute
No. of Contact	50, 68

For more information write Fujitsu Component of America, Inc. 3330 Scott Blvd., Santa Clara, CA 95054 or call 408-562-1000.

FUJITSU

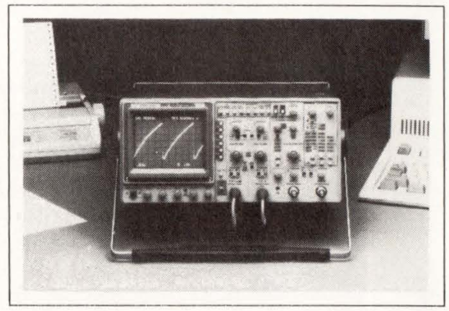
CIRCLE NO. 156

PC-compatible computer or PS/2 to design and control experiments, collect data, and display and analyze the data. Experiment design uses pull-down menus and fill-in-the-blank forms. You can repeat experiments at will by running stored experiment-definition files. While an experiment is running, you can choose to have it repeat continuously, run once, or run in a "burst" mode. A waveform calculator lets you perform mathematical operations on waveforms. Other data-manipulation functions include FFT analysis, extraction of waveform parameters, curve fitting, event detection, and waveform smoothing. You can define your own functions and add them to the menus. The program requires a PC with 1M byte of main memory and 1M byte of extended memory, a 40M-byte hard disk, and a video adapter that conforms to IBM EGA or VGA standards. MS-DOS must be version 3.3 or higher. A math coprocessor is supported if present. $1995.

BrainWave Systems Corp, 3400 Industrial Lane, Suite 3, Broomfield, CO 80020. Phone (800) 736-9283; in CO, (303) 466-6190. FAX (303) 465-5292. **Circle No. 354**

4-Channel Scope With Printer Interface

- *Has 100-MHz bandwidth*
- *Sends printouts through parallel and IEEE-488 ports*



The 2252 portable, 100-MHz-bandwidth, 4-channel scope has dual timebases and automatic setup. You can control it completely over the IEEE-488.2 bus. Though it is an analog instrument, the scope can digitize repetitive waveforms with 12-bit precision and with a record length of 500 points. By connecting an Epson-compatible printer to the Centronics-compatible parallel port, you can obtain waveform printouts. You can also transfer the digitized waveforms to a printer or a computer using the IEEE-488.2 bus. The scope also makes cursor-controlled voltage and time measurements; its 200-MHz counter/timer has a timebase stable to 10 ppm. In averaging mode, the counter's resolution is 10 psec. $3495.

Tektronix Inc, Box 1700, Beaverton, OR 97075. Phone (800) 426-2200. **Circle No. 355**

The ten years battery that offers you even more capacity.

Modern micro-electronics now have a clear pace setter where high capacity Lithium Cells are concerned - the Varta CR Cylindrical cell specially developed for the specific demands of the computer age.
For long life and high reliability.
With capacities second to none worldwide: 2.0 Ah for the AA, 1.4 Ah for the 2/3 AA, 1.0 Ah for the 1/2 AA and 360 mAh for the 1/4 AA, the smallest type in the range.
Laser welding and a self-discharge of less than 1 % per year means that the Varta Lithium cells achieve a lifetime of 10 years. They can be wave-soldered without any additional precautions.
If the needs of your memory backup is for an environmentally friendlier cell with a high energy density, then it is time to start thinking about an improved product for the future. Just call us for your free samples.

VARTA

CIRCLE NO. 158

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D-7090 Ellwangen - Jagst
W.- Germany · Tel. (07961) 831

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300 Executive Boulevard
Elmsford · N.Y. 10523-1202
USA · Tel. (0914) 59 22 500

Varta Batteries Pte. Ltd.
P.O.Box 55
Bedok North Post Office
Singapore 9146 · Tel. (02 41) 26 33

16-Channel Simultaneous S/H Board

- *Compatible with 12-bit, 100k-sample/sec A/D converter*
- *Works with seven software packages*

The CIO-SSH16 is a 16-channel simultaneous S/H board. The externally mounted unit works with the vendor's CIO-AD16, a 12-bit IBM PC bus A/D converter board. One version of the ADC board makes 100k conversions/sec. Both units are 100% hardware and software compatible with popular boards from a competitor, but provide additional features. The compatible boards have a broad base of software support from suppliers of at least seven application packages. They are also supported by drivers for C, Basic, Pascal, and Fortran. In comparison with competitive products, these boards provide more convenient access to the switches that control gain and bipolar offset. CIO-SSH16, $399; CIO-AD16, from $799.

Computer Boards Inc, 44 Wood Ave, Mansfield, MA 02048. Phone (508) 261-1123. FAX (508) 261-1094.

Circle No. 373

88-Pin Universal Device Programmer

- *Programs and tests in one insertion*
- *Supports 2800 IC types*

The Allpro-88 device programmer supports PLDs, PROMs, field-programmable gate arrays, and µPs with embedded ROM. It programs and tests the devices in a single insertion. The programmer's library of supported ICs includes 2800 devices in packages having as many as 88 pins. The programmer also supports ICs based on avalanche-induced migration (AIM) technology. For programming, these devices require pulsed current rather than pulsed voltage. The programmer's 88 pins are under software control. Each one has its own DAC and its own voltage and current sensors. Each pin can perform any programmer function: The functions include slewing or sensing of voltage or current and driving device clock pins at rates to 4 MHz. The programmer accepts data as JEDEC files and allows full editing of any file. The standard test head includes a 48-pin DIP socket and seven plastic LCC sockets with 20 to 84 pins. The vendor can also furnish sockets for other types of surface-mount devices. $14,950.

Logical Devices Inc, 1201 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (800) 331-7766; in FL, (305) 974-0967. FAX (305) 974-8531.

Circle No. 374

INTERNATIONALLY APPROVED CIRCUIT BREAKERS

When you're designing your product for global markets, take steps to protect it right. Choose Airpax. We build in the quality, performance and reliability you demand as well as the required international certification that will assist you in marketing your product anywhere in the world. From initial design through final shipment we can help you every step of the way.

Step-by-step help on three continents.

Engineers at our design/manufacturing centers in Belgium, Japan and the U.S. will assist in your design requirements by recommending the correct magnetic circuit breaker. When you're ready to manufacture, we're strategically located to provide on-time/just-in-time delivery anywhere.

50 milliamps to 100 Amps, 1 to 6 poles and more.

Consider your choices: SNAPAK® in rocker, toggle, paddle, baton, push-pull or push-to-reset styles; IEL, DIN rail mount in single or multi-handle; IEG in a toggle and snap-in mount; and E-Frame branch circuit protectors. Designed to withstand shock, vibration and temperature variances.

Wherever You Design Your Product, We're With You Every Step Of The Way.

UL, VDE, CSA, TUV and SEV approvals.

For any international marketer, it can be a maze of acronyms out there. Not for Airpax, because ours is the broadest line of magnetic circuit breakers fully accepted for international applications in marine, instrumentation, medical systems, appliances, power supplies, information processing systems, industrial controls, HVAC equipment and other devices that demand reliable circuit protection.

The next step is up to you.

To find out more, write us. Or to secure prototypes fast for testing, built to your requirements at no extra cost, call our HOTLINE (301) 228-4600. Airpax, Woods Road, Box 520, Cambridge, MD 21613. FAX (301) 228-8910.

CIRCLE NO. 157

AIRPAX®

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NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

VHDL Design Suite

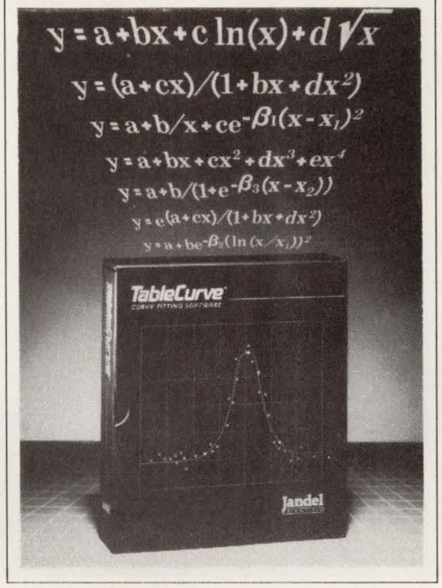
- *Window-based design and simulation tool set*
- *Runs on Sun, Apollo, DECstation, and VAX/VMS*

The VHDL (VHSIC Hardware Description Language) Design Environment (VDE) graphical suite of design tools includes an analyzer, debugger, simulator, waveform viewer, and navigator. The analyzer allows semantic and syntactic verification of your design descriptions. A source-level debugger lets you edit design descriptions during simulation as errors are uncovered. The waveform viewer displays current-signal values and permits timing and state comparisons between current and past values. The navigator gives you a VHDL view of your elaborated models with objects displayed either as icons or through menus. From $12,000 for a 1-year, single-user license on a Sun-3.

Intermetrics Inc, 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-1840. **Circle No. 356**

Curve-Fitting Software

- *Provides F-statistic and standard errors*
- *Outputs to SigmaPlot, 1-2-3, dBase, and others*



TableCurve performs 1-pass least-squares curve fitting to 221 candidate equations. The software selects equations that it ranks by r^2 coefficients; you can then graphically examine these equations and their coefficients. Features that aid this examination include zoom in/out and the display of prediction and confidence bands. The software includes 60 first-order equations,

such as power, log, inverse, and positive and negative exponential; 66 second-order and 55 third-order equations; and rational polynomials and polynomials. Functions such as Gaussian, log normal, sigmoidal, and sine are provided; you can also define your own. $395.

Jandel Scientific, 65 Koch Rd, Corte Madera, CA 94925. Phone (415) 924-8640. FAX (415) 924-2850.

Circle No. 357

DSP Design Software

- *Runs on IBM PC*
- *Allows integration of C- or Pascal-based routines*

DSP Headquarters (DspHQ) allows you to develop and study DSP algorithms. The software lets you integrate functions that the vendor provides, separate function libraries, or your own C and Pascal routines into the algorithms. The algorithms pass and share data structures. The host PC can perform calculations, or you can download the algorithms to signal-processor boards based on the ATT DSP32 chips. The software includes a menu interface, command interpreter, batch-command processor, file- and memory-management capabilities, and hard-copy support for dot-matrix, laser, PostScript, and HPGL devices. $495.

BittWare Research Systems, 400 E Pratt St, 8th Floor, Baltimore, MD 21202. Phone (800) 848-0436; in MD, (301) 879-7274. FAX (301) 879-4465. **Circle No. 358**

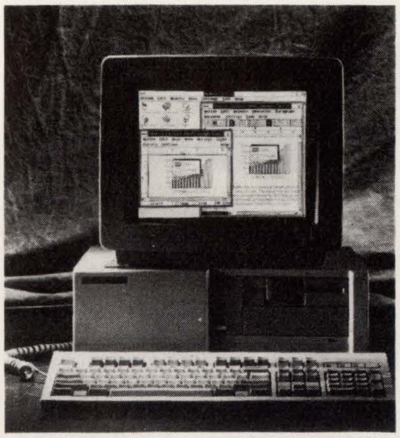
Real-Time O/S

- *Supports Ada on 88000-based systems*
- *Includes VAX/VMS-based host and cross-compilers*

The RTAda/88K is a real-time operating system for embedded 88000-based applications. The package contains a comprehensive development system, including the ARTX real-time multitasking kernel; TeleGen2 host- and cross-compilers running under VAX/VMS; the RTAda/88k source- and system-level debugger; a global optimizer; language tools; foreign object-code importer; and a VAX-hosted cross-assembler. Based on the vendor's Ada real-time kernel, the RTAda/88k offers documented system-call timing so you can evaluate critical path timing. Development license, from $18,000, depending on number of users and VAX host model.

Ready Systems, Box 60217, Sunnyvale, CA 94086. Phone (800) 228-1249; in CA, (408) 736-2600. FAX (408) 736-3400.

Circle No. 359



Desktop PC

- *Uses a 25-MHz 80386 μP and 2M bytes of RAM*
- *Option for hard-disk drive with as much as 340M-byte capacity*

The Vectra 386/25 PC desktop PC uses a 25-MHz 80386 μP. The unit comes with 2M bytes of RAM and a 32k-byte cache memory. The computer provides an upgrade path from the base 2M to 32M bytes of RAM. The memory operates at 25 MHz with near-zero wait states. In addition, the computer has a serial, a parallel, and a mouse port. Its flexible disk drive comes in two versions: 5¼-in., 1.2M-byte and 3½-in., 1.44M byte. You can opt for a hard-disk drive with 42M-, 84M-, 170M-, or 340M-byte capacities and 17- to 19-msec access times. The computer also has a super VGA board that supports 800×600 and 1024×768 pixels as well as being compatible with MDA, CGA, Hercules, and EGA graphics modes. The system runs on OS/2, MS-DOS 3.3, and SCO Unix System V/386 operating systems. Unit without hard disk, $5399; with 84M-byte hard disk, $6999; with 170M-byte hard disk, $7999.

Hewlett Packard, 19310 Pruneridge Rd, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 360

Pattern-Recognition Board

- *Has an 8255 IC driving three separate byte-wide ports*
- *Circuitry can generate an interrupt on any bit of the ports*

The PIO-INT digital I/O board is designed for pattern-recognition applications. It contains an 8255 programmable peripheral interface IC that communicates with three separate byte-wide ports PA, PB, and PC. Circuitry can generate interrupts on any bit change on the

Crystal Clear LCD Modules

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	4 x 16	4 x 20			4 x 40	

Also available are:

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CIRCLE NO. 43

SPOTLIGHT: DESIGN & DEVELOPMENT ■

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CIRCLE NO. 40

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RAF Electronic Hardware
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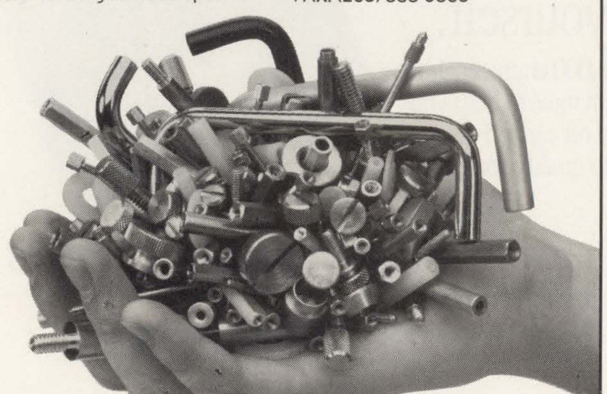
Seymour, CT 06483
(203) 888-2133
FAX: (203) 888-9860



CIRCLE NO. 44

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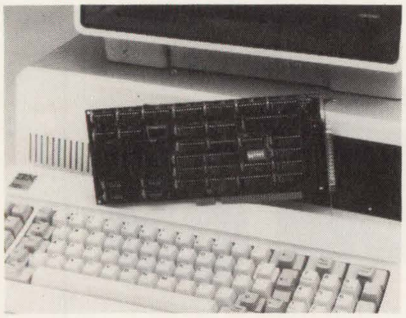
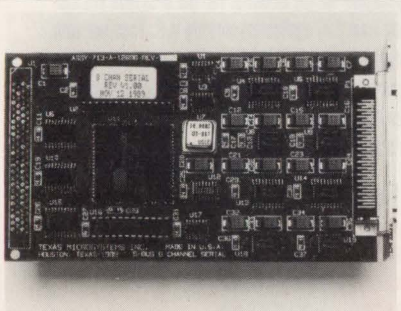
CIRCLE NO. 45



PA or PB ports. The PC port can be split into two nibble-wide ports. You can configure all of the ports as inputs or outputs, using the 8255 control register. The board has two interrupt operations for the PA and PB ports. A bit interrupt, which is a change of any unmasked bit from a 0 to a 1, is stored in a status register. A pattern interrupt occurs when a given pattern of bits changes at a given port. Two mode bits in the interrupt-control register select the type of interrupt. The board uses a contiguous block of 16 I/O addresses on the ISA bus. To prevent spurious interrupts, a digital filter delays an interrupt. $399.

Metrabyte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 361**

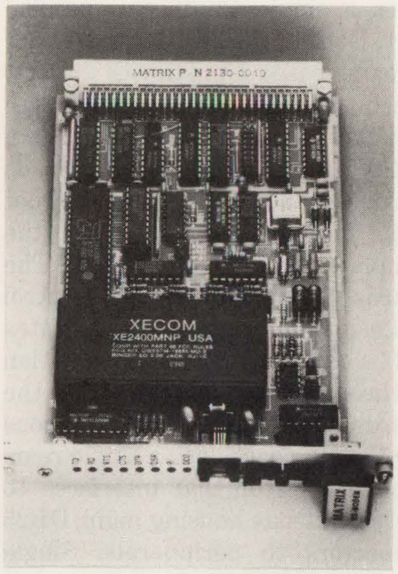


Serial Card

- *Provides eight RS-232C ports for the Sbus*
- *Has 8-byte receive and 8-byte transmit buffer on each port*

The Model SSC-80 serial board for the Sbus in SPARCstations provides full-modem handshake lines for eight RS-232C ports. You can install two boards in a single Sbus to provide 16 RS-232C ports. The board performs flow control (X-on, X-off, and RTS/CTS) in hardware. The serial card has 8-byte receive and 8-byte transmit FIFO buffers on each port. The aggregate throughput is 36,000 cps. You install the board, using menus that prompt you to follow procedures. Software drivers for the Sun Unix operating system are included with the board. $995.

Texas Microsystems Inc, 10618 Rockley Rd, Houston, TX 77099. Phone (800) 627-8700; in TX, (713) 933-8050. FAX (713) 933-1029. **Circle No. 362**



Modem For VMEbus

- *Contains DTE or DCE configurable serial port*
- *Uses MNP Class 5 ECC for errorless transmission*

The 2400-bps MS-Modem board for the VMEbus operates with the industry-standard AT command set. You can configure the serial port for data-communications- or data-terminal-equipment operation. The board handles full-duplex synchronous and asynchronous communications, and it contains a data-access arrangement or direct telephone connection. For error-free communications, the modem provides Microcom Networking Protocol (MNP) class 5 error-correction code. The modem implements autodialing and autoanswering in either pulse or tone mode. It is compatible with CCITT V.22bis, V.22, and V.21 and Bell 212A and 103 specifications. It also adjusts its speed to that of the calling or answering modem. The modem's VMEbus interface maps the board's Z8530 communications controller onto odd bytes in the short address space (A16) at any 256-byte boundary. $895.

Matrix Corp, 1203 New Hope Rd, Raleigh, NC 27610. Phone (919) 231-8000. FAX (919) 231-8001.

Circle No. 363

Color Printers

- *A- and B-size print on paper and transparencies*
- *Use 80960 μP as a controller to print at 300 dpi*

ColorPoint PS is a series of color printers; the model 4 prints on 8.5×11-in. A-size paper, and the model 14 prints on A-size and 11×17-in. B-size. Both printers use an 80960 μP, which provides 300 dpi, as a print controller. The thermal-transfer printers can print Postscript-compatible files, using the PhoenixPage Postscript Printer Language Interpreter from Phoenix Technologies (Norwood, MA). The interpreter is also compatible with Adobe Postscript color version 50.3. The printers use roll-feed media; their automatic cutter with a double-cut feature lets the user produce color prints having the same image size as LaserWriter fonts. Ports for the printers include standard Appletalk, Centronics parallel, RS-232C, and SCSI. Model 4 and model 14 have 6M- and 10M-byte buffers, respectively. Both printers are Pantone certified. Model 4, $6999; model 14, $9999.

Seiko Instruments Inc, Graphic Devices and Systems Div, 1130 Ringwood Ct, San Jose, CA 95131. Phone (408) 922-5800. FAX (408) 922-5840. **Circle No. 375**

Sbus Multiplexers

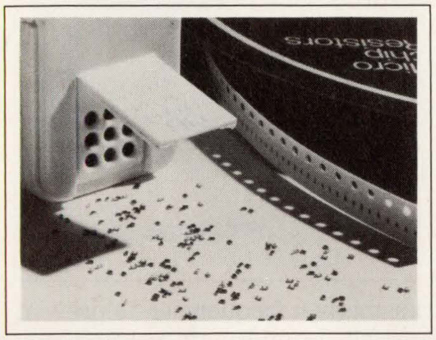
- *Come with Streams-based Unix device drivers*
- *Provide baud rates as fast as 64k baud*

Four add-in multiplexer boards are available for the Sbus in the SPARCstation. Three of the boards are available with two, four, and eight serial ports, respectively. The 2-port version also has a Centronics parallel port. The fourth board provides a single Centronics parallel port. Each of the boards comes with Streams-based Unix device drivers, which provide compatibility with Sun O/S versions 4.0.3 and 4.1. An install program automatically loads the driver and modifies system boot files. The driver works with the complete set of "ioctl" calls. The boards provide full-modem control and can transfer data at baud rates as fast as 64k baud. The installation of three 8-port versions allows the boards to support 24 simultaneous users. The boards use a single rear-panel connector that interfaces to a breakout box housing eight DB25 connectors to peripherals. Single parallel port, $395; eight serial ports, $1495.

Artecon, Box 9000, Dept 5500, Carlsbad, CA 92008. Phone (800) 872-2783; in CA, (619) 931-5500. FAX (619) 931-5527.

Circle No. 376

COMPONENTS & POWER SUPPLIES



Chip Resistor

- *Smallest in industry*
- *Handles 25V*

Measuring just 1×0.5 mm, the MCR 01 chip resistor occupies 60% less board area than the MCR 03. The chip has resistance values ranging from 5.6Ω to 1.5 MΩ, can handle 25V, and dissipates 0.032W at 70°C. Resistance tolerance measures ±5%. Internally, the unit's thick-film metal resistive element is sintered to an alumina ceramic substrate. A protective film covers the element and completely encapsulates the trimming groove, thus effectively sealing out moisture and temperature extremes. The operating range spans −55 to +125°C. Packaged on 8-mm-wide paper-tape reels, the chip is available only in 1-reel, 5000-piece minimum orders. $0.035 (1000). Delivery, 12 weeks ARO.

Rohm Corp, 8 Whatney, Irvine, CA 92718. Phone (714) 855-2131. FAX (714) 855-1669.

Circle No. 377

Electroluminescent Lamps

- *Have 10-fL brightness*
- *Feature 40,000-hour life*

ELCR-4 thick-film electroluminescent foil lamps provide initial brightness levels of between 8 and 10 fL at 115V ac. In an exit-sign lighting application, the lamps have an average life in excess of 40,000 hours. The lamps are constructed with an electroluminescent phosphor mix on a foil base with a screened, transparent front-electrode image and an encapsulant/fusion seal. Because the lamps have no filaments, they are immune to problems due to vibration. The lamps have a 0.032-in. nominal thickness, and they provide a uniform light source with less than ±10% variance in brightness across the entire active area. $25 to $50. Delivery, eight to 10 weeks ARO.

Eltech, 181 Gibraltar Rd, Horsham, PA 19044. Phone (215) 441-0404. FAX (215) 441-8299.

Circle No. 378

Surge Protector

- *Has 1-nsec reaction time*
- *Can handle 180A*

The DLP-4.3 surge protector provides protection from lightning, transients, and surges on dial-up telephone lines. It plugs into the same local ac outlet as the equipment being protected. Vulnerable equipment is then plugged directly into the unit's RJ11 jacks. The device reacts in <1 nsec. It combines fast-acting avalanche diodes and brute-force gas tubes and can handle numerous hits without degrading. The protector handles 180A current levels on an 8×20-μsec waveform and 40A on a 10×1000-μsec waveform. The unit exceeds all pertinent industry standards including UL497A. From $49.

MCG Electronics Inc, 12 Burt Dr, Deer Park, NY 11729. Phone (516) 586-5125. FAX (516) 586-5120.

Circle No. 379

Rack System

- *Has 1100-lb capability*
- *Available in three depths*

The IMRAK 1400 19-in. enclosure can handle loads ranging to 1100 lbs. Fully compliant with IEC 297-2, the units are available in three standard depths—800, 600, and 400 mm—and in heights ranging from 12U to 57U. A range of accessories is available including swing frames and cable-management components such as hoops and cross bars. The rack comes fully assembled. Four sizes are available from stock—32U, 37U, 42U, and 47U. From $750.

Bicc-Vero Electronics, 1000 Sherman Ave, Hamden, CT 06514. Phone (203) 288-8001. FAX (203) 287-0062.

Circle No. 380

Autoranging Switchers

- *Have 1000W output*
- *Have a 4W/in.^{3} power density*

Series R switching power supplies deliver as much as 4 W/in.^{3} in a 5×5×10-in. package. Autoranging circuitry allows the units to operate worldwide without the need for a switch or jumper. An optional 42 to 56V dc input allows the supplies to accommodate telecommunications applications. The line includes models that have from three to seven outputs in 800 and 1000W configurations. Supply features include current sharing, overload and overvoltage protection, inrush current limiting, remote sense, remote inhibit, remote margin, EMI input filter, and full safety-agency approvals. A forced current-share option for all outputs provides paralleling that is essential for redundant (N+1) power systems. From $762 (100). Delivery, eight to 10 weeks ARO.

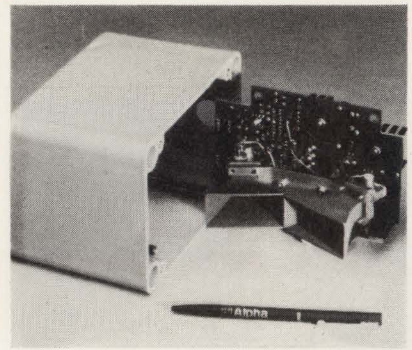
Unipower Corp, 2981 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-2442. FAX (305) 971-1837.

Circle No. 381

Level-Sensor Module

- *Has 8-in. sense-distance capability*
- *Operates to 85°C*

The MSM20100 is a noncontact-point level sensor. It has a 0- to 8-in. detection range, 0.1-in. repeatability, and 0.125-in. hysteresis. The unit operates from inputs of 10 to 28V dc or 115/230V ac. The operating range spans −40 to +85°C. The sensor uses a microwave transmitter/receiver to detect the presence of liquids or solids at a set height in bins or tanks. You can also use the unit as a near-field object-proximity sensor. You can set each unit to operate on one of four coded



transmission frequencies to prevent crosstalk in multiunit applications. LEDs indicate power connection, level/object sense, and output trigger; you can set three switches for code, pulse, or continuous output or fail-safe conditions. $395

Alpha Industries, 20 Sylvan Rd, Woburn, MA 01801. Phone (617) 935-5150. FAX (617) 935-4939.

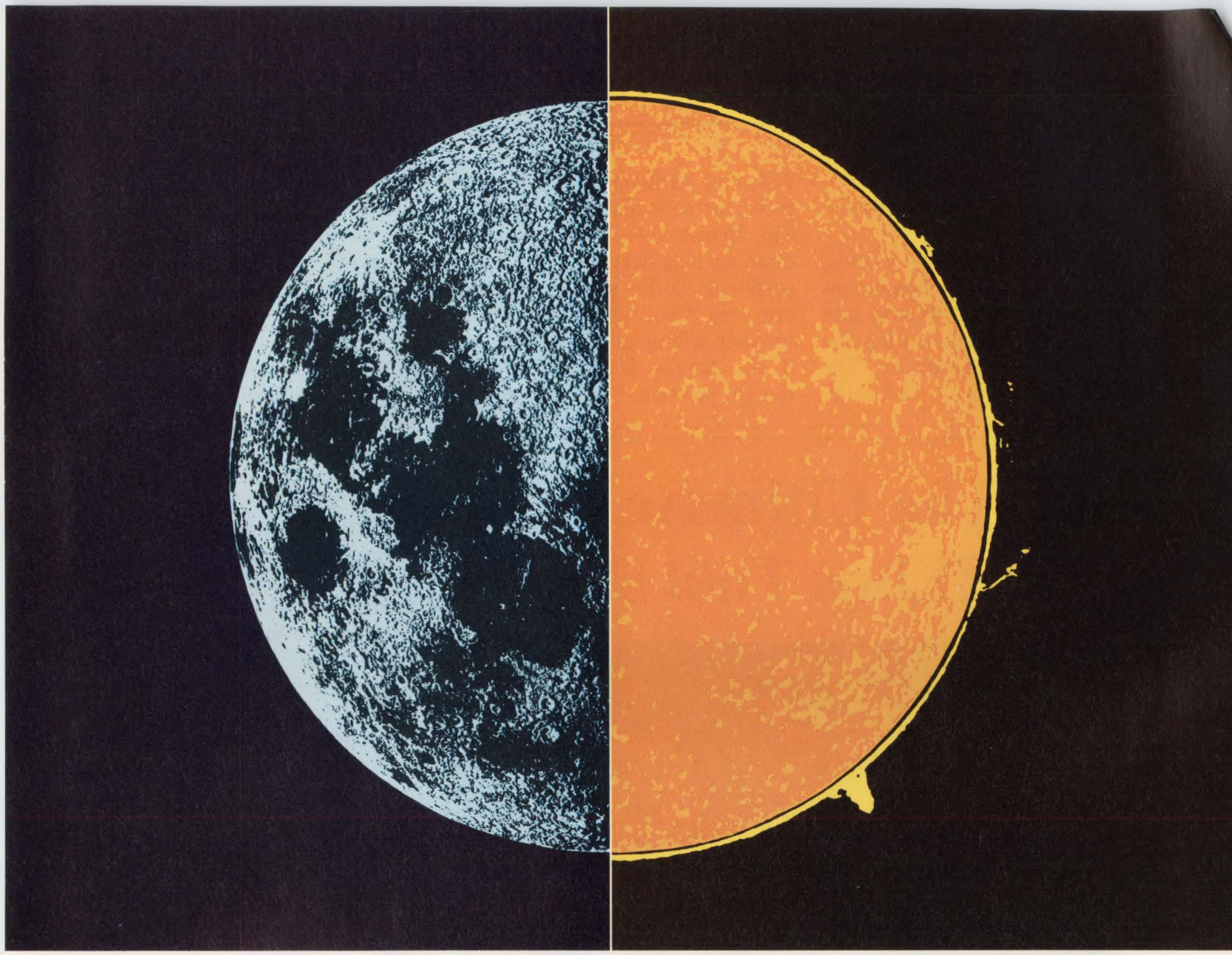
Circle No. 382

Diode Arrays

- *Have 0.1A current-carrying capability*
- *Feature seven or eight diodes*

The SG6100 and SG6101 feature seven and eight straight-through diodes, respectively. Each diode features a 75V min breakdown voltage, 100-mA current capability, 5-nsec max switching speed, and 25-nA max leakage current. The arrays are qualified to MIL-S-19500/474 and use silicon-on-insulator technology to maximize density. Because the arrays are monolithic devices, the electrical parameters are very closely matched—an important feature in many military applications. Both devices are available in ceramic DIP and flatpack housings. The arrays can be processed to JANTXV, JANTX, or the manufacturer's S-level equivalent flow. $20.25 (OEM qty). Delivery, 16 weeks ARO.

Silicon General Semiconductor, 11861 Western Ave, Garden Grove, CA 92641. Phone (714) 898-8121. FAX (714) 893-2570. TWX 910-596-1894. **Circle No. 383**



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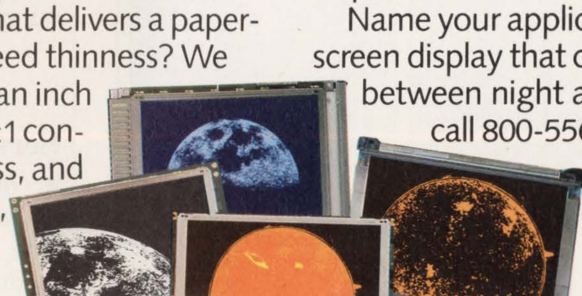

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Magnetic Circuit Breakers

- *Require no mounting hardware*
- *Rated for 50A*

Available in 1- to 4-pole models, IEGS and IEGHS magnetic circuit breakers are designed to snap into the panel, thereby eliminating the need for mounting hardware. The units are UL recognized, CSA certified, and VDE approved. They are rated for as much as 50A, and you can furnish them with short, medium, or long delays for 400 Hz, dc, or 50- or 60-Hz signals. All units are trip free, ensuring that the breaker will open on overload even if the handle is forcibly held in the On position. Temperature variations don't affect the units, which have a black matte face plate, measure about 3 in.^{3}, and weigh 2.2 oz. Single-pole model, \$8 to \$10 (500). Delivery, stock to eight weeks ARO.

Airpax, Woods Rd, Cambridge, MD 21613. Phone (301) 228-4600. FAX (301) 228-8910.

Circle No. 370

DIP Sockets

- *Feature dual-beam contacts*
- *Compatible with wave soldering*

Series 400C DIP sockets feature stamped dual-beam contacts, which provide two independent electrical connections. A nonwicking, closed-bottom design allows you to insert ICs before wave-soldering and protects against flux and solder contamination. The sockets feature an X- and Y-stackable insulator to maximize packing density. Dual-tapered leads provide easy alignment during automatic insertion operations. The sockets have an autoinsertion rail for smoother travel down feeder tubes. Anti-overstress wings protect the contacts and help prevent damage from oversized leads. Available in 8- through 40-position versions, the sockets meet military standards. Contacts are available in beryllium copper or phosphor bronze material and feature either selective gold or tin-lead plating. \$.0034 to \$0.005/ position.

Augat Interconnection Products Group, 33 Perry Ave, Attleboro, MA 02703. Phone (508) 222-2202. FAX (508) 222-0693.

Circle No. 371

Servoamplifier

- *Operates on battery power*
- *Outputs ±12V at ±2A*

The model 201-13 pulse-width-modulated servoamplifier operates from a 12 to 16V battery power source. The unit develops ±12V at ±2A continuous output and outputs ±5A peak. An internal MOSFET bridge circuit provides the bipolar output capability. The amplifier switches at 22 kHz, allowing it to drive servomotors with armature inductance as low as 500 mH without the need for series inductors. The amplifier has built-in protection against short circuits, overcurrent, excessive temperature, and incorrect or reversed supply voltage. A current sensor permits peak-current adjustment for protecting the motor load against overload or from being driven with excessive acceleration. The amplifier also provides end-of-travel and beginning-of-travel controls as well as emergency shutdown. The amplifier has a 1-kHz bandwidth and is housed in a pc-board-mountable package measuring $5 \times 3.28 \times 0.8$ in. $295.

Copley Controls Corp, 375 Elliot St, Newton, MA 02164. Phone (617) 965-2410. FAX (617) 965-7315. TLX 285975. **Circle No. 372**

INTEGRATED CIRCUITS

14-Bit ADC With 10M-Sample/Sec Speed

- *Spurious-free dynamic range is 90 dB*
- *Intermodulation distortion is −90 dBc*

Offering encode rates to 10M samples/sec, the AD9014 14-bit A/D converter also features a 90-dB spurious-free dynamic range (SFDR) at test frequencies of 540 kHz and 2.3 MHz. The SFDR is 86 dB and 72 dB at 4.3 MHz and 10 MHz, respectively. The device's S/N ratio is 75 dB, and intermodulation distortion is −90 dBc. Other guaranteed dynamic specifications include a 40-nsec transient response to within 0.01%, and no-missing-code differential and integral nonlinearity of ½ LSB and 1 LSB, respectively. Digital correction circuitry and decoupling capacitors minimize output errors at major code transitions as well as limiting gain and offset errors to 0.5% and 0.25%, respectively. The AD9014, which operates from ±5 and ±15V supplies, is a complete A/D subsystem. The ADC is composed of two hybrids mounted on a 13.7-square-in. multilayer pc board. From $2800 (100).

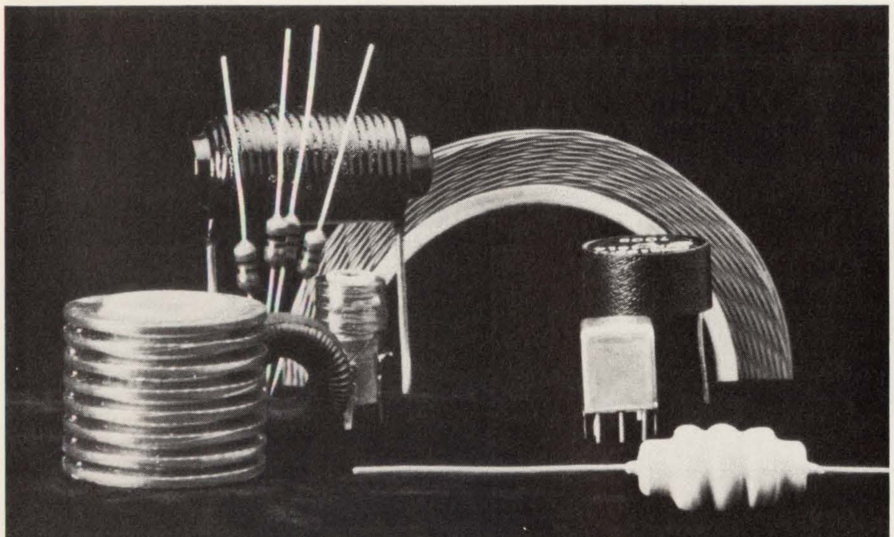
Analog Devices, 7910 Triad Center Dr, Greensboro, NC 27409. Phone (919) 668-9511.

Circle No. 364

Cache-Memory Controller

- *Features 16k-byte static RAM*
- *Has 100 cache tags*

The 82395 DX 386 Smart Cache controller integrates cache control logic, 16k bytes of static RAM, and 1000 cache tags in a single package. The controller expands the architecture of the i486 CPU on-chip cache into a stand-alone device designed for 386 DX CPU-based systems. The device uses a sophisticated cache architecture to outperform cache subsystems with a 4× to 6× larger RAM. In a Power Meter MIPS version 1.5 benchmark run on a 33-MHz 386 CPU-based EISA system, the controller oper-



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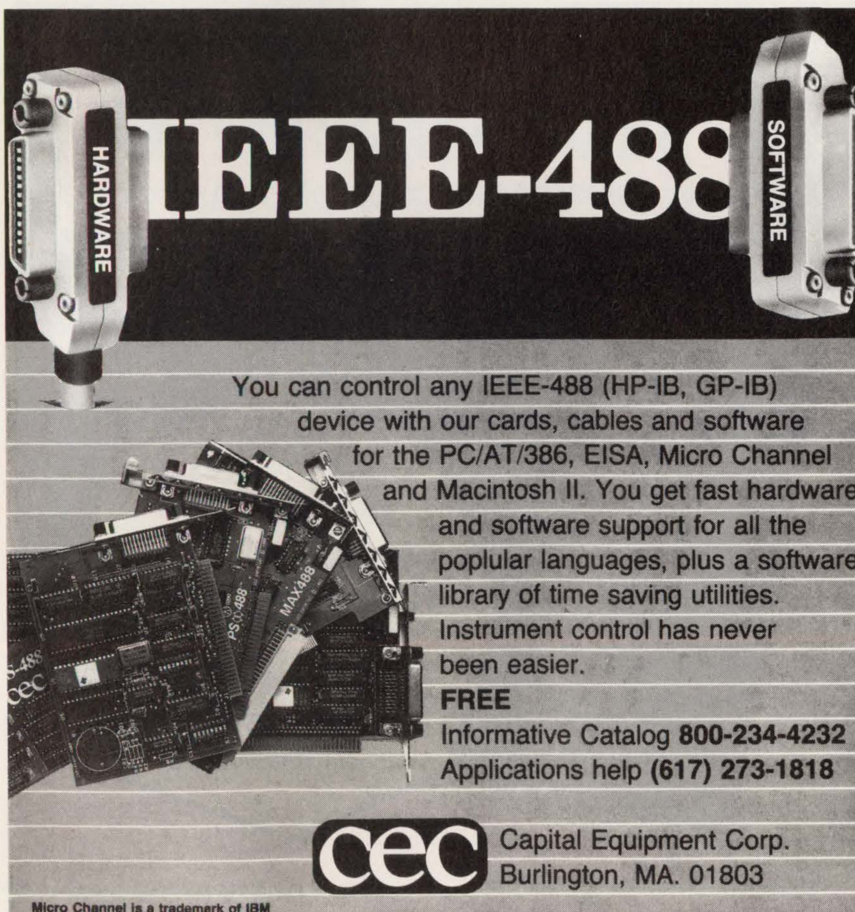

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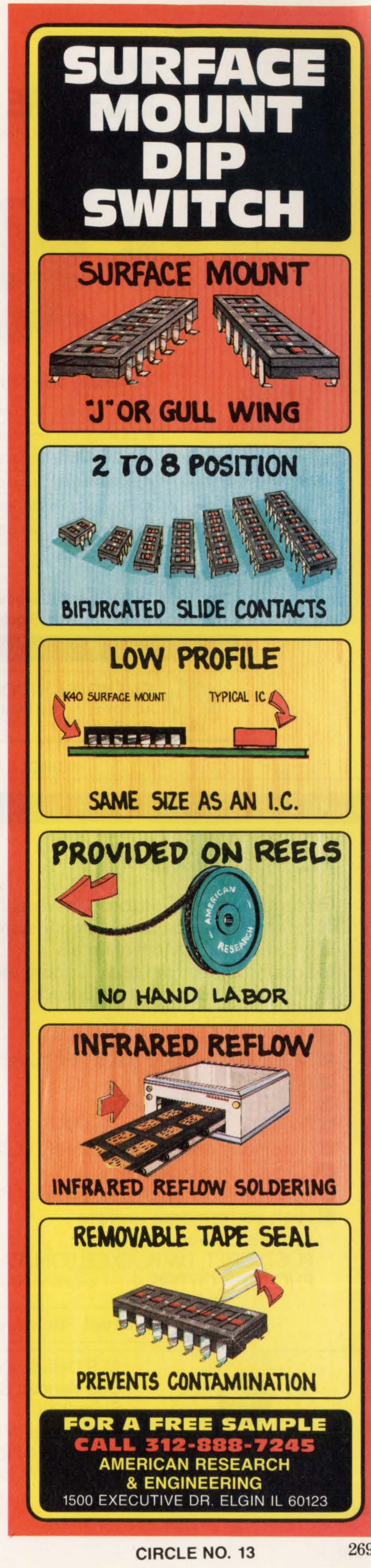

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ated at 8.3 MIPS. The 82395 DX is available in a 196-lead plastic quad flatpack. 25-MHz version, $90; 33-MHz version, $109 (1000).

Intel Corp, #HP-27, Box 58065, Santa Clara, CA 95052. Phone (800) 548-4725; in CA, (916) 351-2747.

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Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. TLX 174388. **Circle No. 366**

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Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 562-7181. FAX (408) 727-1550. **Circle No. 367**

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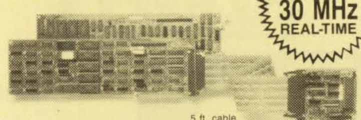

8051

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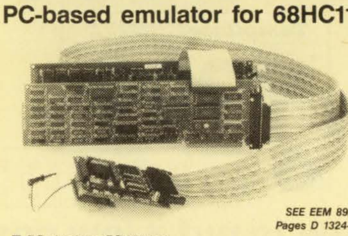

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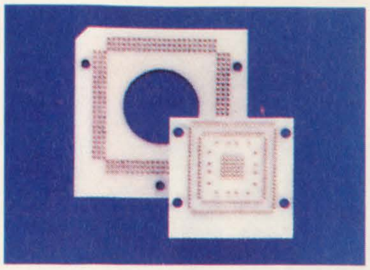

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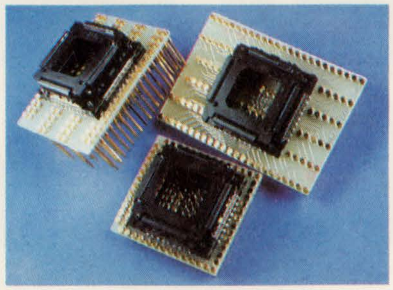

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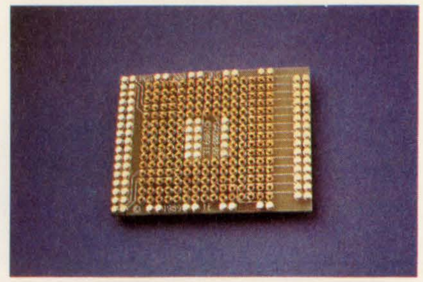

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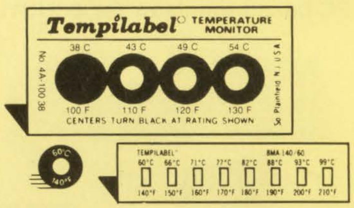

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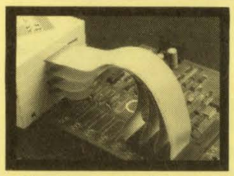

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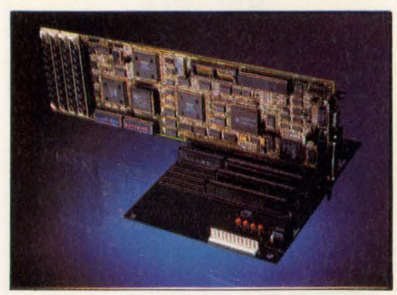

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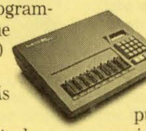

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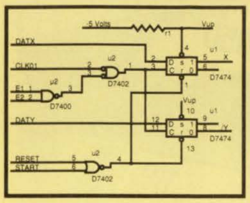

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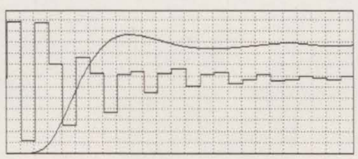

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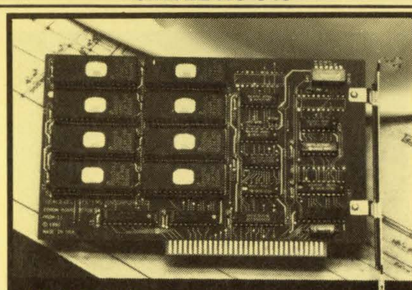

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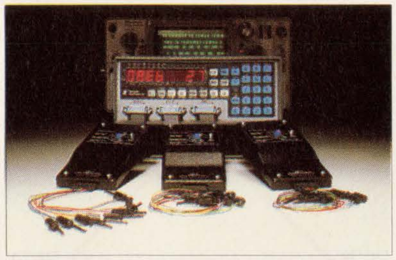

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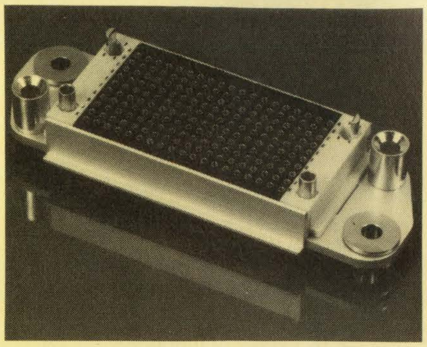

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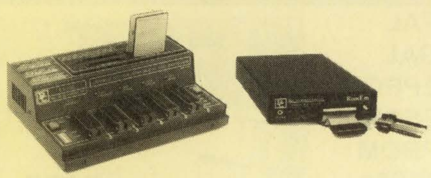

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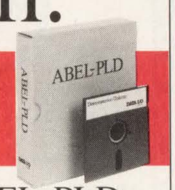

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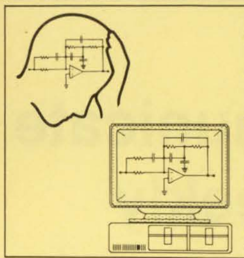

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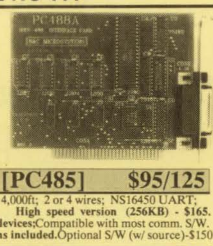

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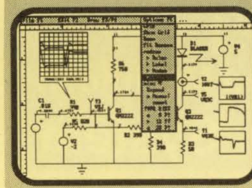

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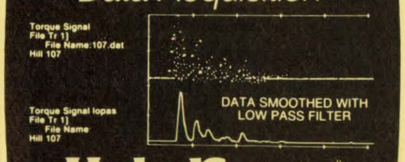

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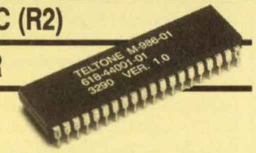

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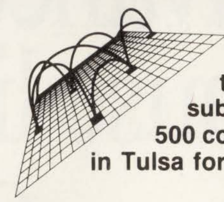

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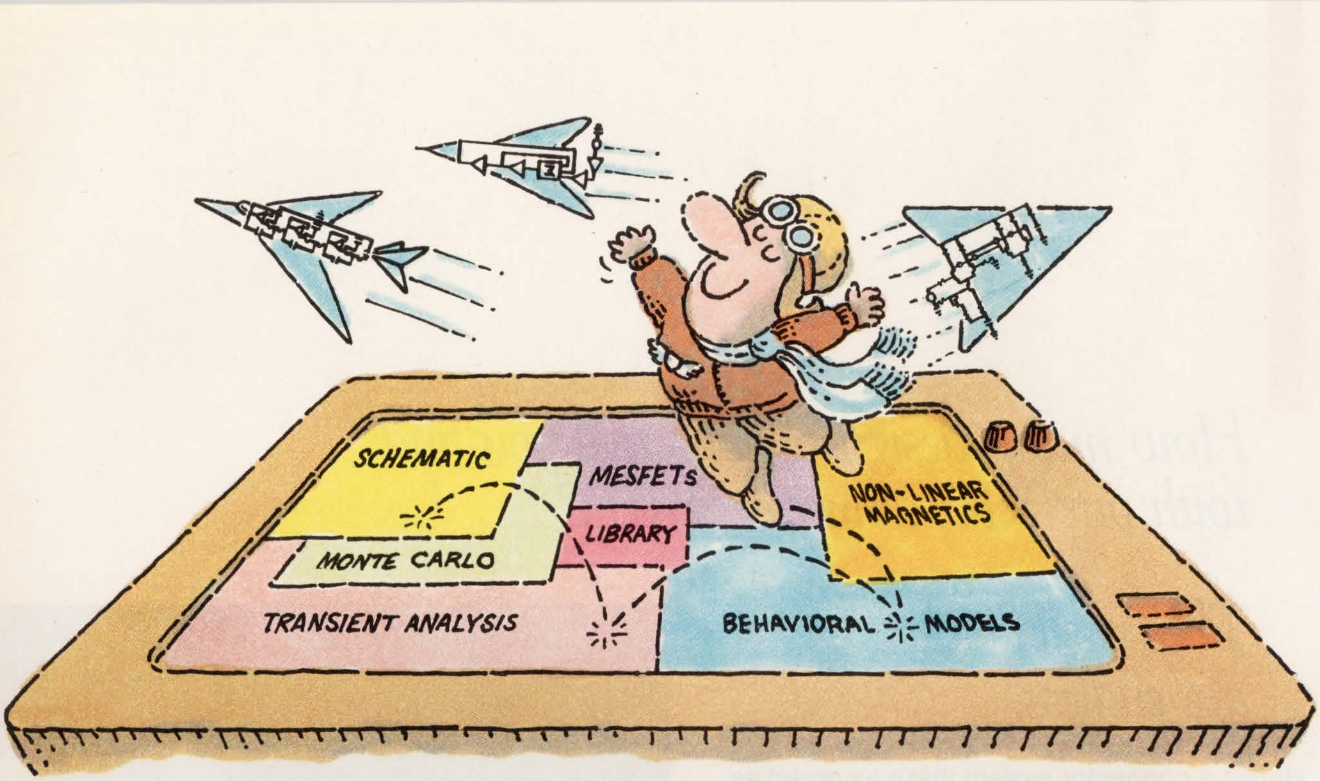

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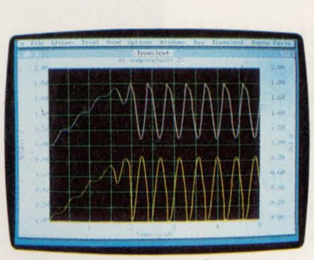
Take modeling power. We've significantly expanded math expression capabilities to permit comprehensive analog behavioral modeling. And, beyond Gummel Poon BJT and Level 3 MOS, you're now ready for nonlinear magnetics modeling. Even MESFET modeling.

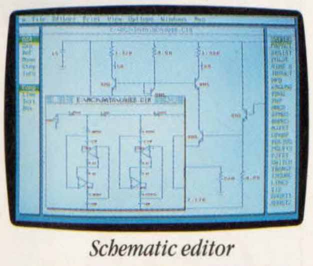
Analysis and simulation is faster, too. Because the program's now in "C" and assembly language. That also means more capacity—for simulating even larger circuits.

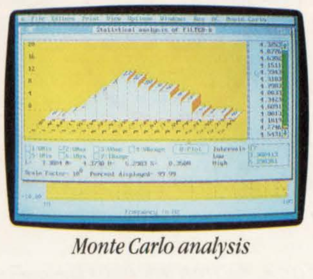
As always, count on fast circuit creation, thanks to window-based operation and a schematic editor. Rapid, right-from-schematics analysis—AC, DC, fourier and transient—via SPICE-like routines. The ability to combine digital/analog circuit simulations using integrated switch models and parameterized macros. And stepped component values that streamline multiple-plot generation.

And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

Cost? Still only $1495. Evaluation versions still only $150. Brochure and demo disk still free for the asking. Call or write for yours today. And see how easily you can get ideas up and flying.


Transient analysis


Schematic editor


Monte Carlo analysis

spectrum

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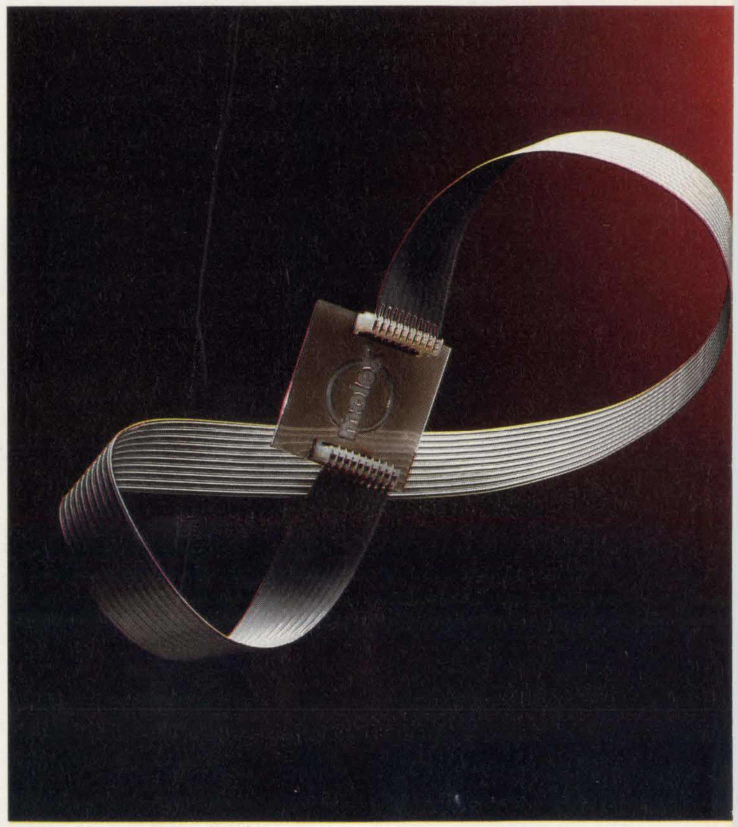
How many design options will you find with our KK® connector system?

The possibilities are endless.



Here's a connector system that's as broad as your imagination. The Molex family of KK® connectors includes 15 basic units. You can combine these in an almost endless number of reliable, cost-efficient board-board and wire-board system designs. Look at the possibilities:

Specify KK connectors with .100" or .156" center spacing...top, side or bottom pin entry PC board connectors...tin, gold, or surprisingly low cost selective gold plating...crimp, solder tail or insulation displacement terminations.

KK connectors give you still another choice: standard KK dual cantilever or unique Trifurcon® terminals with 3 contact points for highest reliability in tough operating conditions.

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