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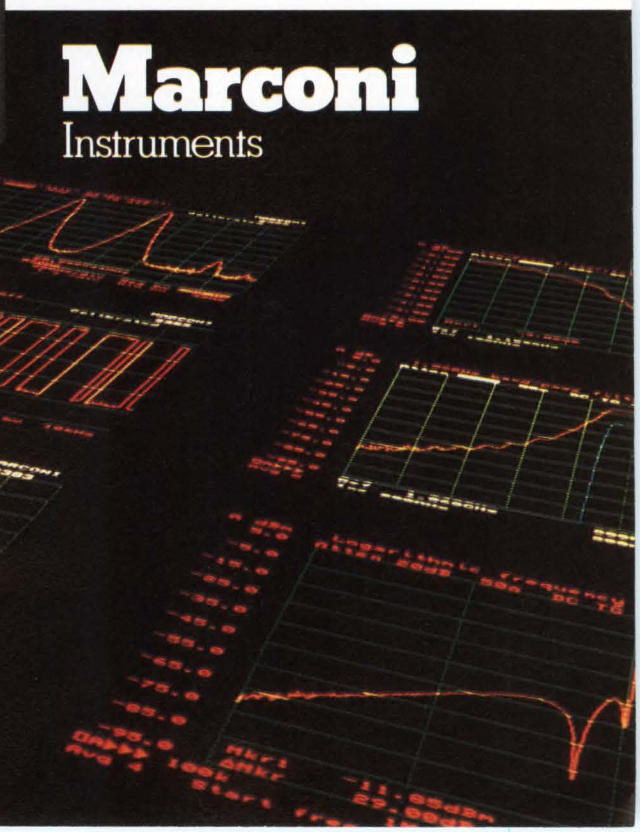

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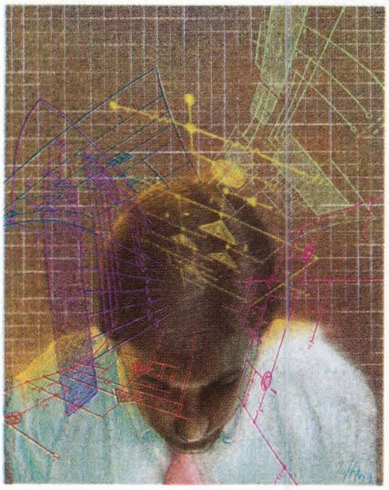
Volume 34, Number 15A July 20, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



(Illustration by Bruce Gilfoy; art direction by Chinsoo Chung)

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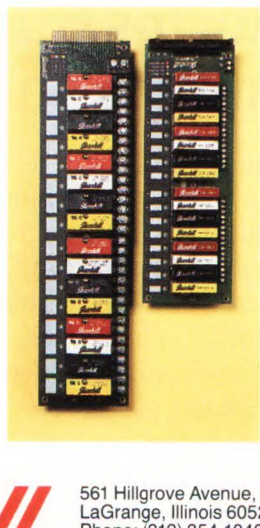

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CIRCLE NO 5

INTRODUCTION

Over the years, our readers have continually used the Information Retrieval Service cards to suggest that EDN should offer a compendium of Design Ideas. In an effort to satisfy these requests, EDN published three Design Ideas Special Issues in 1988. Reader response to these supplements was overwhelmingly positive. It was so favorable, in fact, that EDN editors decided to publish another Special Issue—this collection of more of the best Design Ideas published in EDN between 1985 and 1988.

This collection of designs reflects your needs and not the preferences of our technical editors. In fact, you and your colleagues voted for these winning ideas by circling the "bingo card" numbers that appear at the end of each Design Idea we publish. Of the circuit-design tips in this Design Issue, half garnered Best-of-Issue honors based on reader preference. The remaining Design Ideas received the second highest number of reader votes over the 1985 to 1988 time frame.

To achieve some semblance of order, we've divided the ideas into some generic categories and provided an index that lists design and circuit categories. Although the index is a handy place to look for a special circuit, we'll bet most readers will want to read the ideas one by one, just to see what circuits are available.

As you read these Design Ideas, remember that each one came from a reader who thought someone else might benefit from his or her work. So, if you find this issue helpful, thank your fellow engineers who submitted the ideas we've published over the years. And the next time you have an interesting and useful circuit, consider sharing it with other engineers by submitting it for use in EDN's regular Design Ideas section.

Besides seeing your name in print and gaining an extra $100, you might find your idea has been selected as the issue winner. Each issue winner collects an extra $100. Keep in mind, too, that EDN's editors also choose a grand-prize winner each year. The grand prize includes a check for $1500. You might also see your idea published in a future EDN Design Ideas Special Issue. You'll find an entry form in the Design Ideas section in most issues of EDN.

If you enjoy this Design Ideas Special Issue and find it useful, we'd like to hear from you. If you have suggestions for improvements and changes, we'd like to hear those, too. Just send us a note or give us a call. We'd also like to thank all the readers who have submitted Design Idea entries over the years.

Enough introduction. Here are the ideas you've been clamoring for. Good reading. EDN

Tom Ormond

Tom Ormond
Senior Editor

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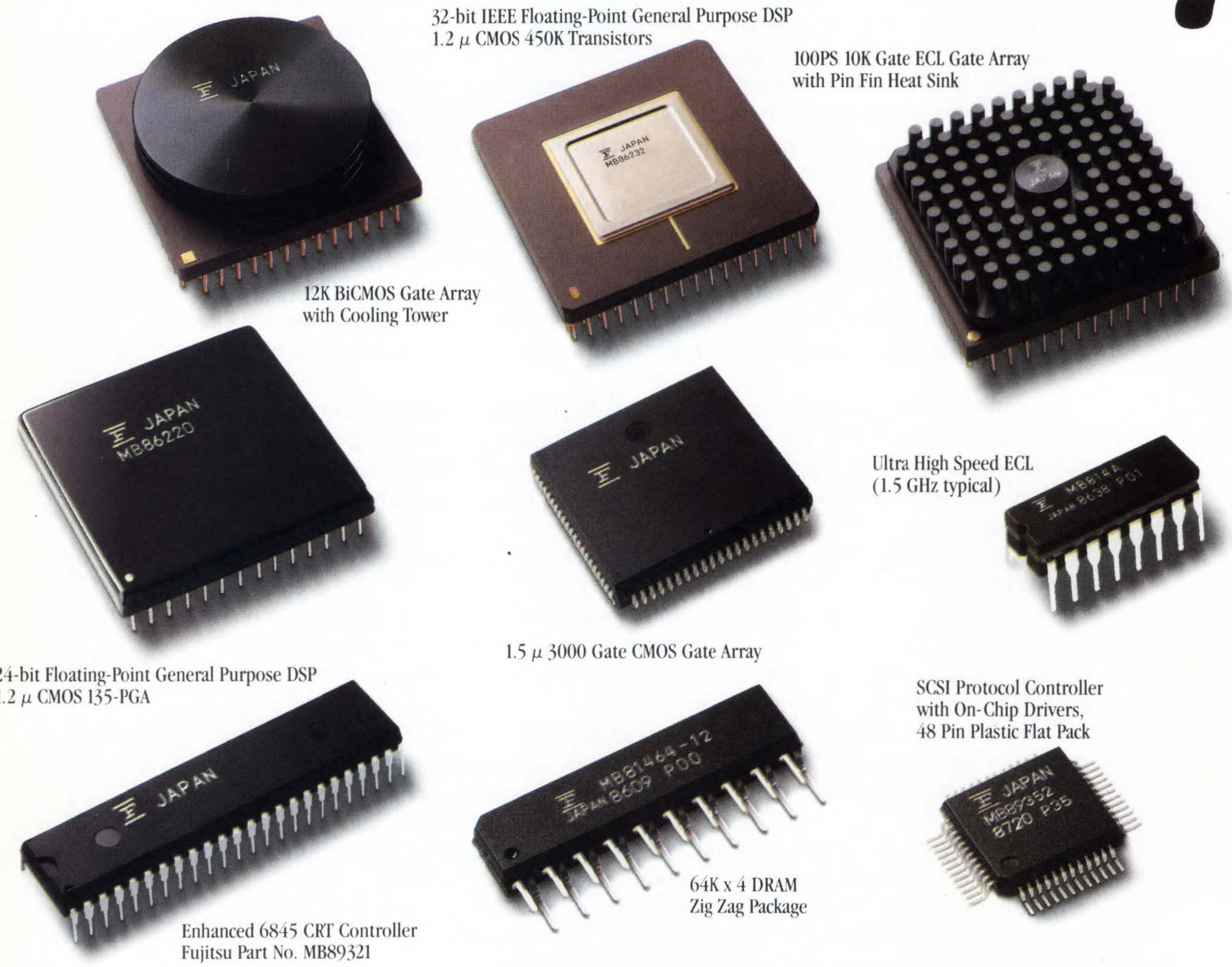

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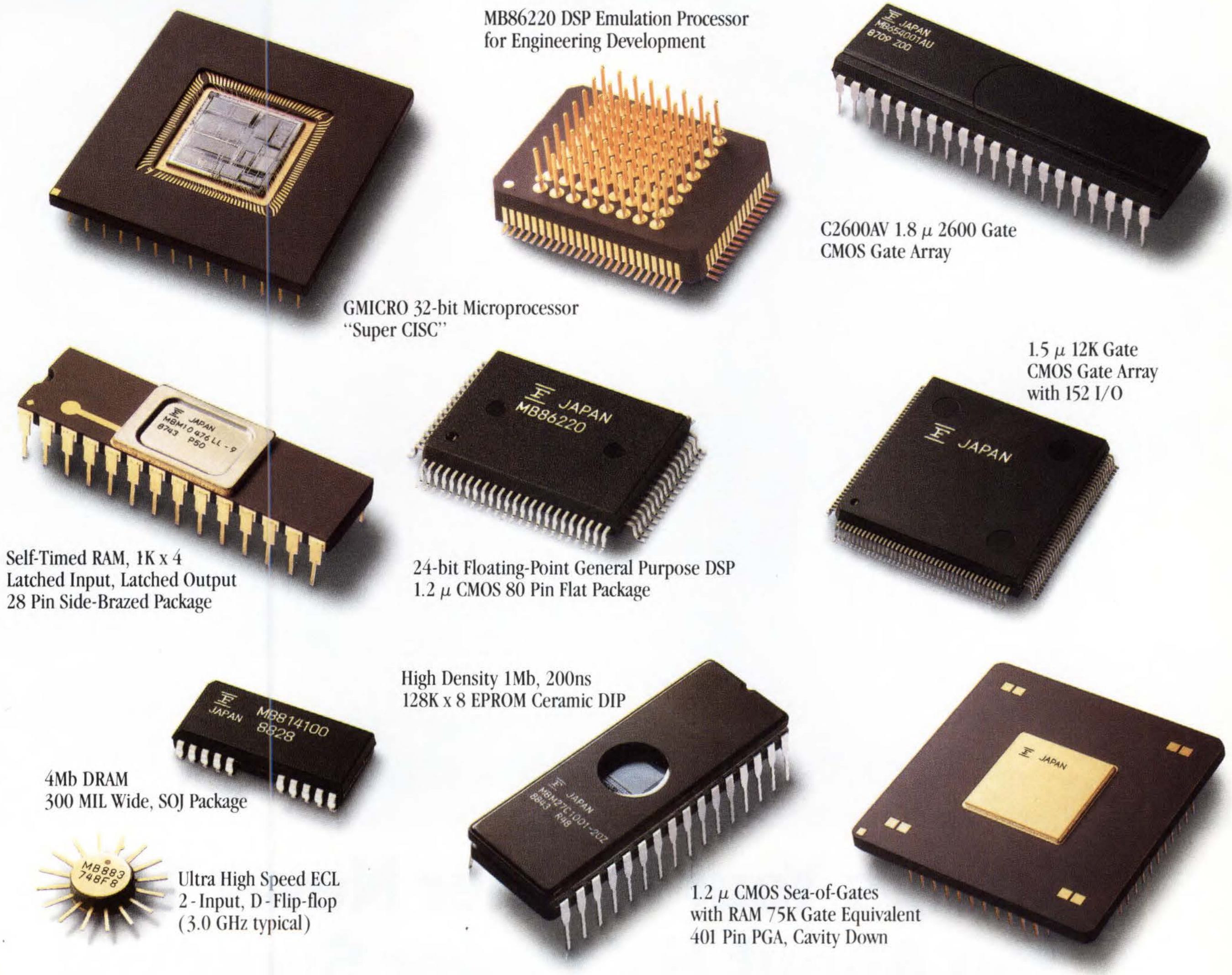

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CIRCLE NO 6


GLASSMAN HIGH VOLTAGE, INC.

Power MOSFETs yield efficient power supply

Marek Gajewski
Litton Industries, Woodland Hills, CA

Using seven power MOSFETs in various capacities, the switch-mode power supply in **Fig 1** offers a 15V output and a 20A, 5V regulated output featuring 90% efficiency and low output noise. Further, the output impedance is determined primarily by coil resistance and MOSFET on-resistance; in contrast, a switcher based on duty-cycle modulation exhibits an output impedance that's higher by a factor inversely proportional to the duty cycle.

Duty-cycle modulation is used on the input side of transformer T_1, however, where transistors Q_1 through Q_3 and the duty-cycle modulator make up a buck-type preregulator (the regulated 5V output bucks against a 5V reference). Q_3 completes a path to ground for transistors Q_1 and Q_2, which then can alternately ground the ends of T_1's primary. The primary of saturable-core transformer T_2 is connected to the secondary of T_1 in a free-running loop, which provides 30-kHz gate-switching signals to Q_1, Q_2, and the output synchronous-rectifier transistors Q_4 and Q_5.

Transformer T_3 transfers the regulated 5V output back to the input-ground-referenced preregulator circuit to provide isolation between the input and output grounds. T_3's primary is driven by a 4041-type true/complement buffer. Unlike optoisolators, this isolation module provides a near-unity transfer function that's insensitive to temperature and production tolerances.

To prevent power dissipation due to overlapping gate-drive signals to Q_1 and Q_2, diodes D_6 and D_7 clamp T_2's center tap near the output ground potential (the MOSFETs require at least 3V to turn on). Loop compensation is simplified by the absence of a filter capacitor following inductor L_1, which would form a second-order pole in the regulator's transfer function. On the other hand, transformed load capacitance forms a virtual capacitor at this position, providing energy storage during the preregulator's off cycle. **EDN**

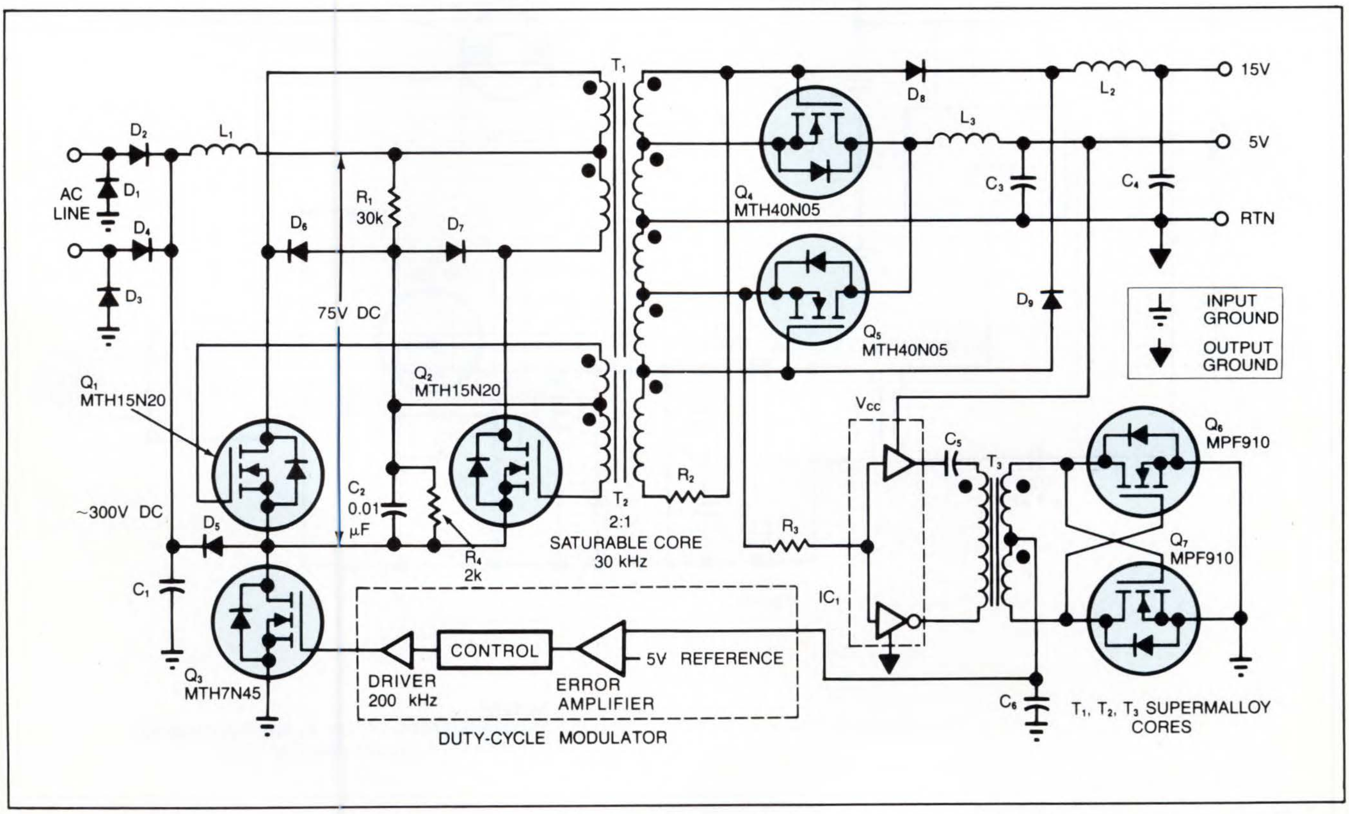


Fig 1—This switching regulator based on power MOSFETs *includes a 200-kHz duty-cycle-modulated preregulator and a full-wave synchronous-rectifier output.*

Solid-state switch offers fast interrupt

Geoffrey N Drummond
Hughes Aircraft, Torrance, CA

Based on a diode bridge and a VMOS power transistor (Q_1), a solid-state switch **(Fig 1)** acts as a circuit breaker, sensing and interrupting an overcurrent condition within 2 μsec. The circuit's isolation transformer, T_1, allows the switch to float. The components shown are capable of handling 1A rms or 8A pk. However, if your application requires the handling of more current, you can change R_1, Q_1, and the bridge.

Compared with a thyristor, a VMOS transistor has higher saturation voltage—6 to 10V—and is less rugged—peak- to continuous-current ratio is about 4:1, vs 20:1 for a thyristor. To protect the MOSFET in the case of fault conditions, SCR Q_2 exerts a crowbar action on the Q_1 gate, minimizing power dissipation by forcing the transistor to turn off rapidly. The 555 timer forms an astable multivibrator that drives T_1 at 150 kHz. A full-wave voltage doubler at the T_1 secondary then provides 15V to the Q_1 gate, which turns on the transistor and switch for normal operation.

Three overcurrent conditions will short circuit the transistor and turn off the switch. First, if resistor R_1 senses excessive steady-state rms current, it will cause the switch to open at a threshold of R_1=0.6V/I rms.

Second, the circuit will accommodate time-variant currents (such as those encountered in a lamp or motor,

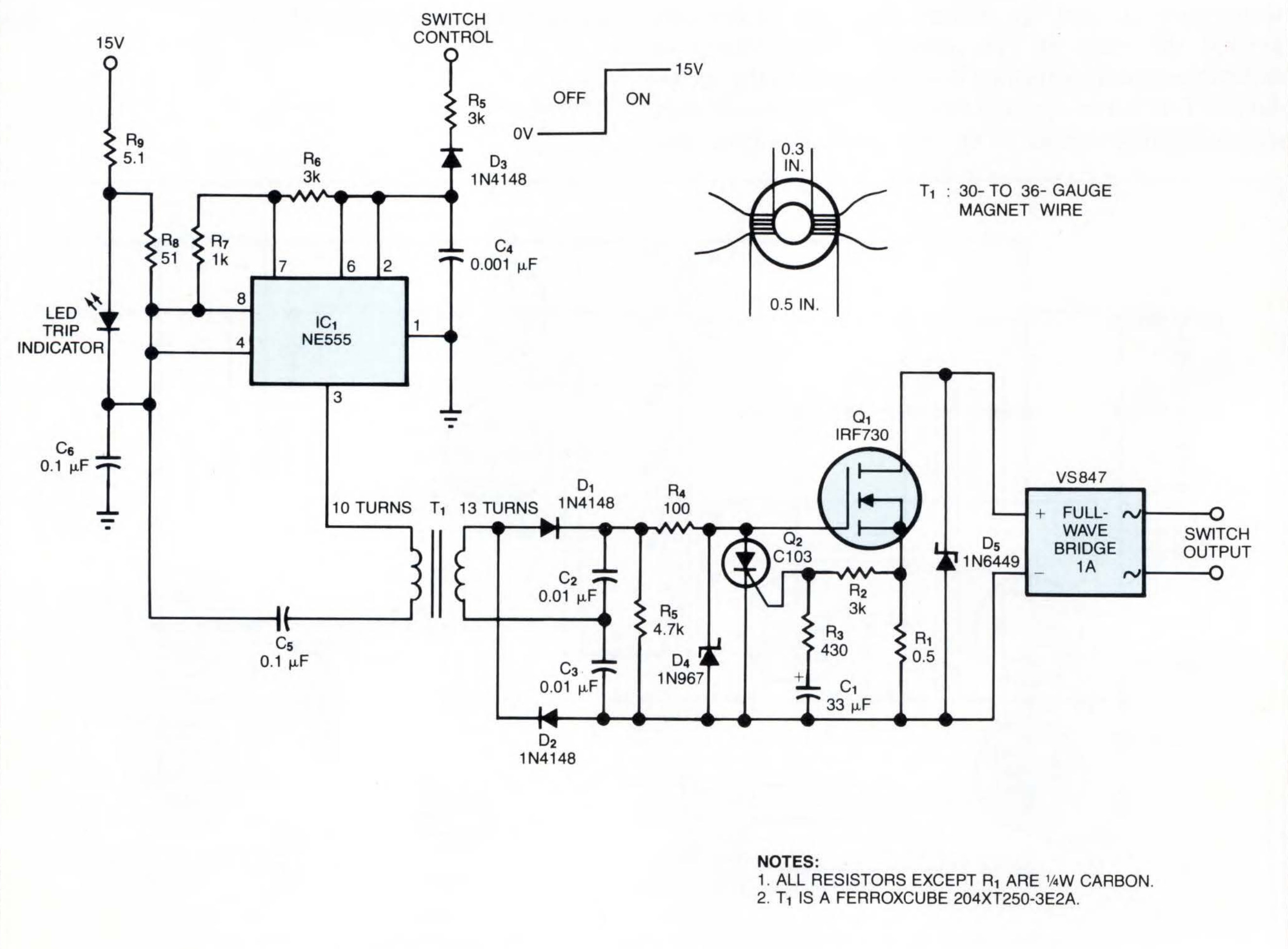


Fig 1—A floating, isolated solid-state switch *interrupts fault currents in about two microseconds.*

for example) in which the initial surge current is greater than the steady-state current. In this case, capacitor C_1 limits the surge value by setting a limit on the ampere×second product (I×t) for currents between steady state and peak. This threshold is approximately

$$C_1 = I \times t \times R_1 / (0.6V \times R_2).$$

Third, you can set R_3 to limit the peak current I_P, according to the relation

$$R_3 = 0.6V \times R_2 / (I_P \times R_1 - 0.6V).$$

After a delay of 0.5 μsec, a peak current causes the switch to open completely in about two microseconds. In addition, the transient suppressor D_5 limits peak voltage to 200V. Once tripped, the switch will remain off until the timer is gated off (Switch Control), or until you remove the timer's power for at least one second.

Fig 2b shows the results of a peak-current test (**Fig 2a**). The solid-state switch opened fully in 2.25 μsec; a 1A fast-blow fuse, on the other hand, passed 300A for 10 μsec before opening, which welded the mercury relay's contacts together. **EDN**

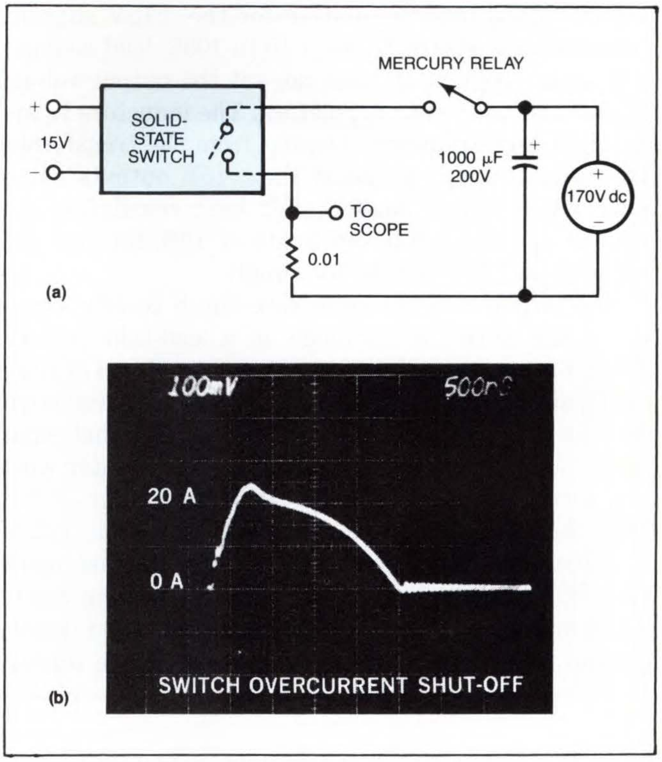


*Fig 2—**This test circuit (a) allows you to measure** the delay and response time of the circuit breaker. The results are presented in **b**.*

Derive ±15V and 5V from a 12V battery

Andy Jenkins
Maxim Integrated Products, Sunnyvale, CA

Parts for the triple-output dc/dc converter shown in **Fig 1** cost about $11 in 100-piece quantities. The circuit converts the 12V output of a lead-acid battery to isolated ±15V supply voltages plus a nonisolated 5V supply voltage.

IC_1 is a switching-regulator chip normally used in step-up applications, but the transformer and circuit shown allow the device to provide a step-down function as well. The chip generates a 45-kHz signal that drives the gate of MOSFET Q_1.

Q_1 turns on when the gate voltage is high, causing a linear increase in T_1's primary current, which stores energy in a magnetic field. The field starts to collapse as Q_1 turns off, reversing the voltage polarity on all windings and causing the voltage on each secondary winding to increase. These secondary voltages then deliver energy to the outputs by forward-biasing the Schottky diodes D_1, D_2, and D_3. When the 5V output rises above a desired level, feedback to the chip causes an internal error comparator to turn off the gate signal to Q_1.

The secondary-winding ratios set the output-voltage levels, and close coupling between the trifilar windings assures good load regulation for the ±15V supplies (regulation is about 2% for a 10 to 100% load change). For better regulation, you can set the output voltage higher and add linear regulators. The inductors L_1 and L_2 block high-frequency ringing from the transformer that would otherwise boost the ±15V outputs out of spec when lightly loaded. For best regulation, you should provide minimum loads of 10% for the 15V supplies and 20% for the 5V supply.

The circuit can accommodate the 8 to 16V range associated with the terminals of a lead-acid battery. What's more, the protection network made up of resistor R_1 and zener diode D_4 allows the circuit to withstand 50V for 1 msec—a classic overvoltage test that simulates the load dump of an automobile's alternator when you turn off the ignition. For an input change of 8 to 16V, the 5V output's line regulation is typically 0.2%.

Battery current is about 600 mA for nominal operation, but current peaks in the primary winding can be 4A or more. Therefore, you should provide good-quality ground connections and short, low-impedance connections to the transformer and the MOSFET. Close decoupling using ceramic and electrolytic capacitors also reduces output noise. With proper circuit layout, the output noise is about 50 mV at the 5V output and 30 mV at the 15V outputs.

The transformer, constructed with a ferrite pot core that offers low loss and minimal magnetic leakage, has a primary inductance of about 21 μH for the power levels shown. You must choose a core size and material that will handle the 4A peak currents without saturation. The 15V secondaries have 2.9:1 turns ratios, which provide the desired 3:1 voltage ratio after covering the rectifier losses. Actual turns are as follows: the primary, 11½ turns; the 15V secondaries, 11½ turns each; the 5V secondary, four turns. High circuit efficiency (about 75% at full load with a 12V input) eliminates any need for a heat sink on the MOSFET. EDN

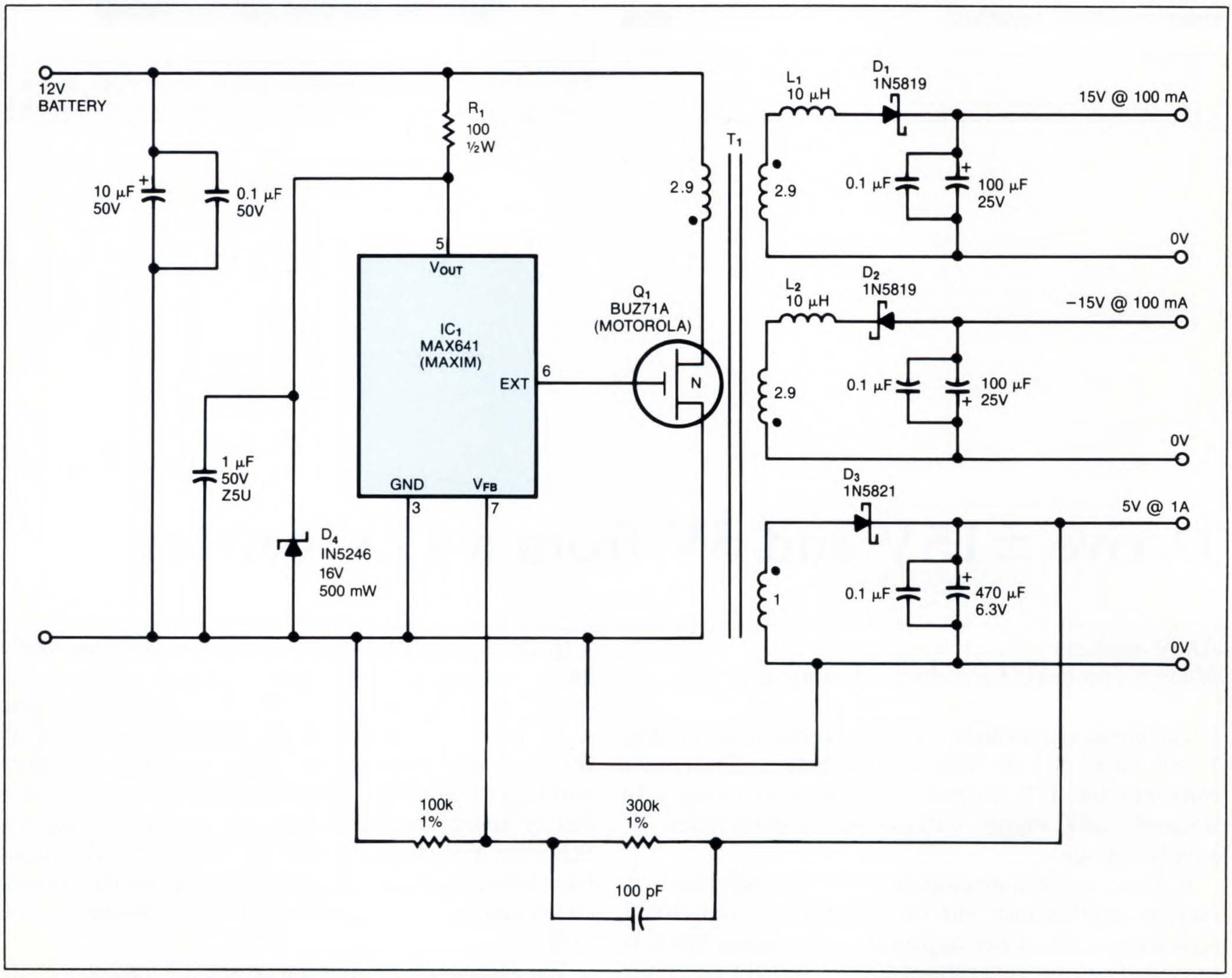


Fig 1—This triple-output dc/dc converter *requires only one IC.*

CIRCLE NO 8

Low-current voltage tripler is inexpensive

Henry Yiu
Endevco, San Juan, CA

You can expand the low-cost ($2.25) voltage tripler of **Fig 1** by adding more stages, and you can lower the circuit's output impedance by adding more buffer inverters in parallel. To obtain a negative-voltage converter, simply reverse the diode and capacitor polarities and connect the V_{IN} terminal to ground. The circuit oscillates at approximately 350 kHz when R_{OSC}=1 kΩ and at approximately 4 kHz when R_{OSC}=100 kΩ. For the circuit as shown, **Fig 2** charts the efficiency and the load voltage vs load current. **EDN**

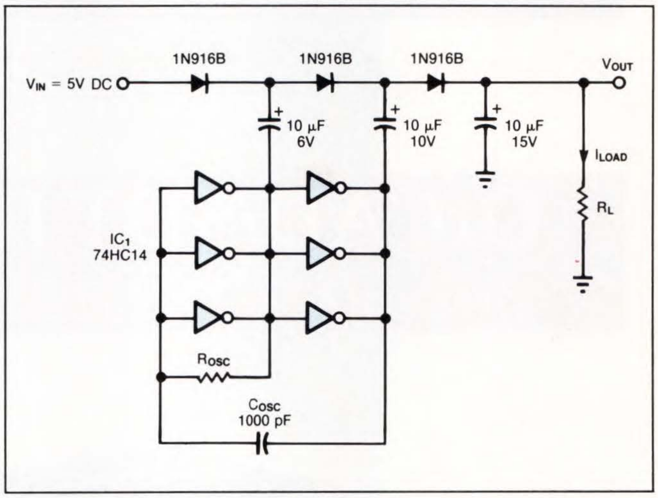


***Fig 1—This circuit generates** a 15V output by tripling V_{IN}.*

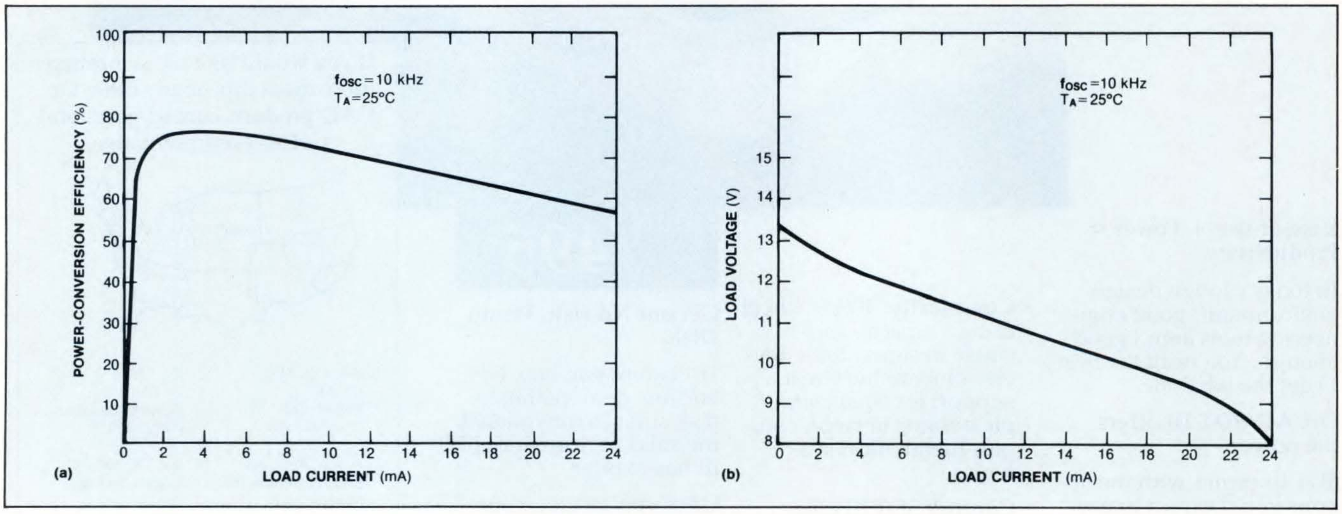
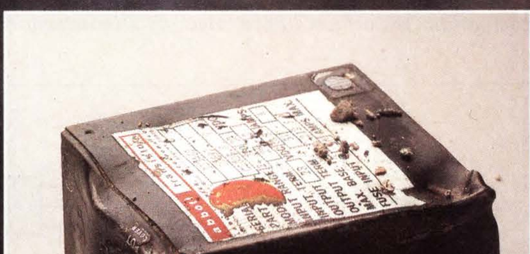


***Fig 2—These curves show Fig 1's** power-conversion efficiency **(a)** and load voltage **(b)** vs load current.*

Sampling phase detector simplifies a PLL

Russell Kautz
Texas Instruments, Plano, TX

Phase-locked loops can include an analog frequency-mixing circuit **(Fig 1a)** or a digital divider **(Fig 1b)** to accomplish synchronous down-conversion of the reference and input frequencies. An alternative, the sampling system in **Fig 1c**, reduces parts count and cost by a factor of eight. Moreover, the sampling approach removes frequency-conversion circuitry from the signal



In a Navy test, a Tomahawk cruise missile exploded into a concrete building. When the dust settled, little remained but gravel and fragments of casing.

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path, which provides improved short-term stability for the local oscillator, excellent temperature stability, and a thirtyfold decrease in lock-in time.

Fig 2 demonstrates a sampling phase-detector loop that locks the output of a crystal oscillator to that of a rubidium standard. First, the zero-crossing detectors

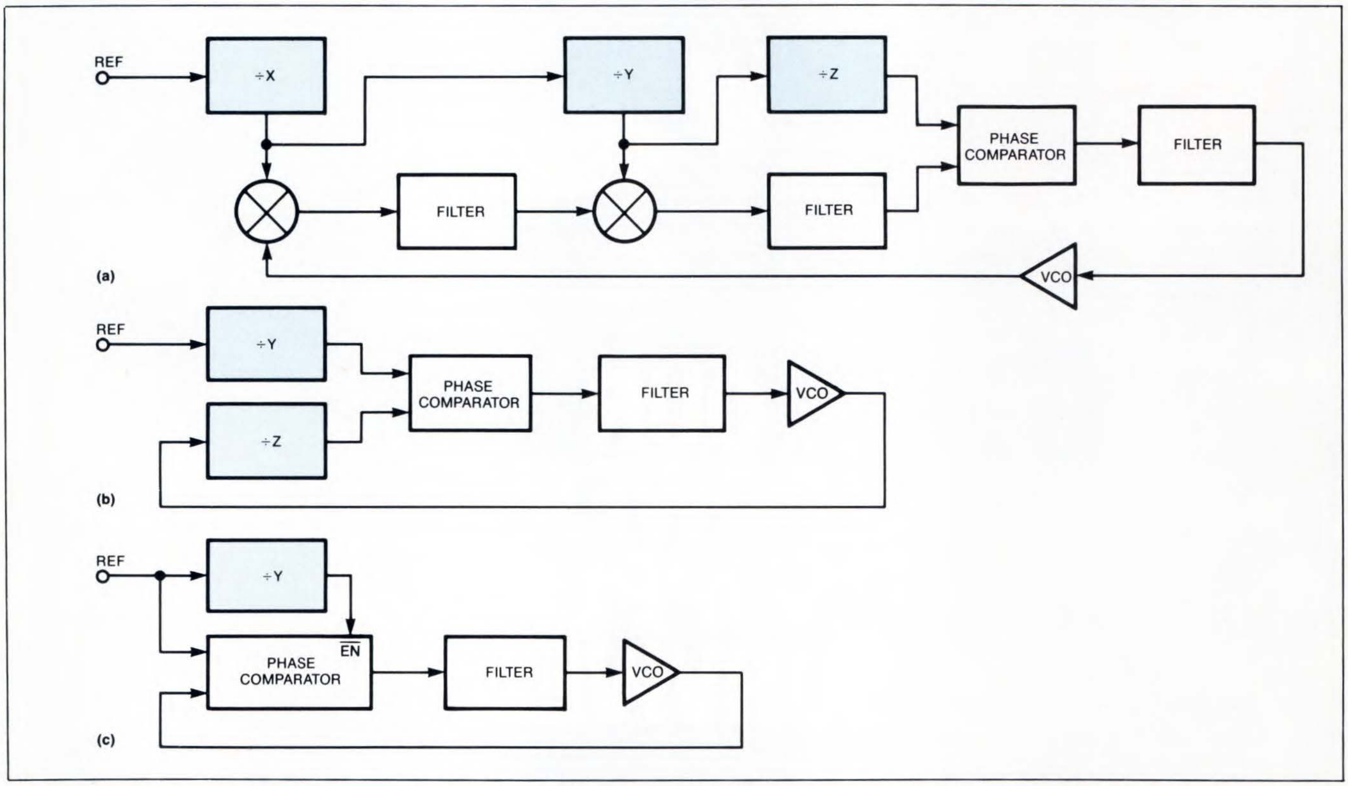

Fig 1—Some phase-locked loops *use analog frequency-mixing techniques* ***(a)****, and some divide both inputs to the phase comparator using digital dividers* ***(b)****. The sampling phase comparator* ***(c)*** *achieves advantages by eliminating down-conversion circuitry from the signal paths.*

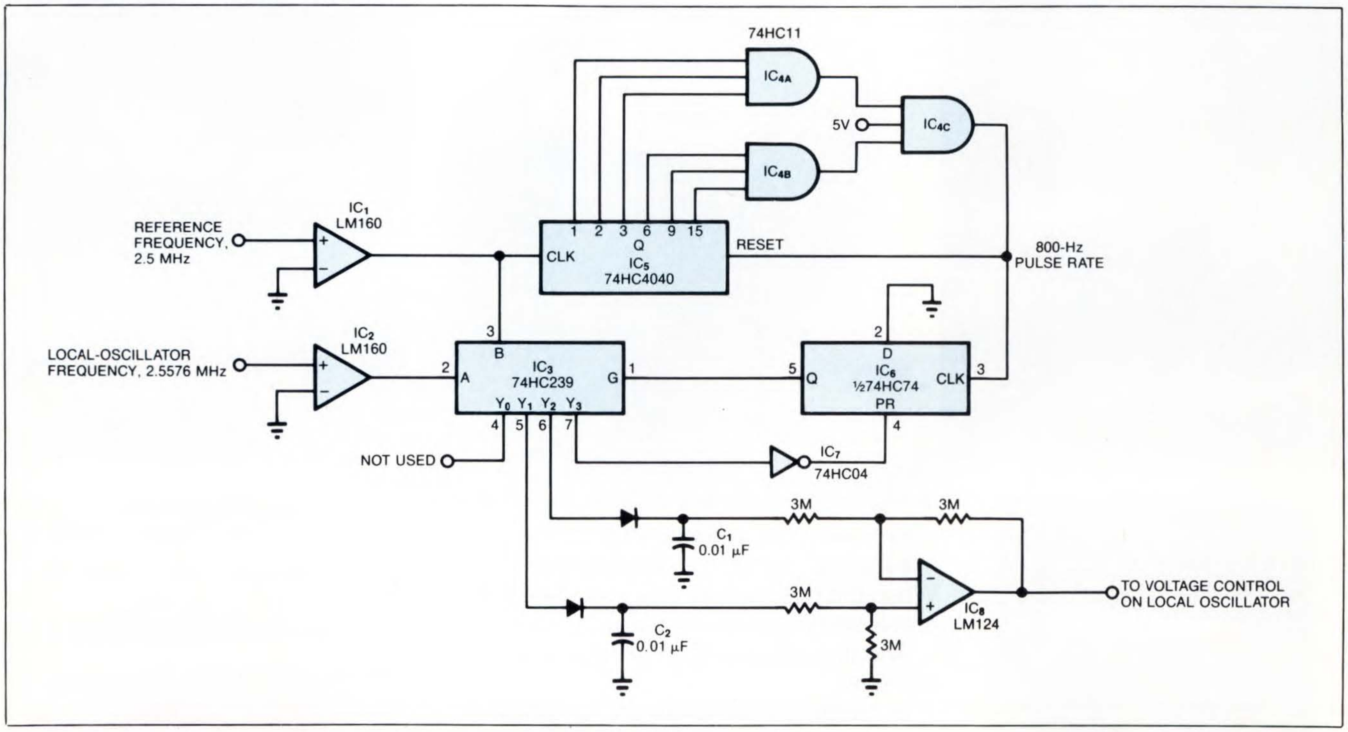

Fig 2—This sampling phase-locked loop *generates a voltage output whose polarity and magnitude represent the local oscillator's phase error.*

IC_1 and IC_2 convert the reference and local-oscillator (LO) frequencies to digital signals. The 2-to-4-line demultiplexer IC_3 then samples these frequencies at 800 Hz (every 1.25 msec). The reference and LO frequencies may differ, but each must be an integral multiple of the sampling rate if the system is to achieve lock.

To set the sampling period, IC_{4A} and IC_{4B} wait for the output 110000110101 (count of 3125) from the 12-bit counter IC_5. When that output occurs, IC_{4C} issues a brief positive pulse that resets the counter and toggles the flip-flop IC_6.

Fig 3 illustrates the digital phase detection that the IC_3 demultiplexer performs. The presence of Y_1 indicates a phase lead between the LO and reference frequencies, and the duration of Y_1 indicates the amount of phase lead. Similarly, Y_2 indicates phase lag. Y_3 goes high when both inputs are high, which ends the sample period by setting the flip-flop.

Note that in **Fig 2** C_1 and C_2 convert the Y_1 and Y_2 pulses to voltage inputs for the differential amplifier IC_8. The amplifier in turn produces a dc voltage representing polarity and magnitude of the local oscillator's phase error. When locked, the loop produces narrow Y_1 and Y_2 pulses (less than 1 nsec) of equal magnitude and duration. The amplifier rejects common-mode signals such as digital noise from the demultiplexer. **EDN**

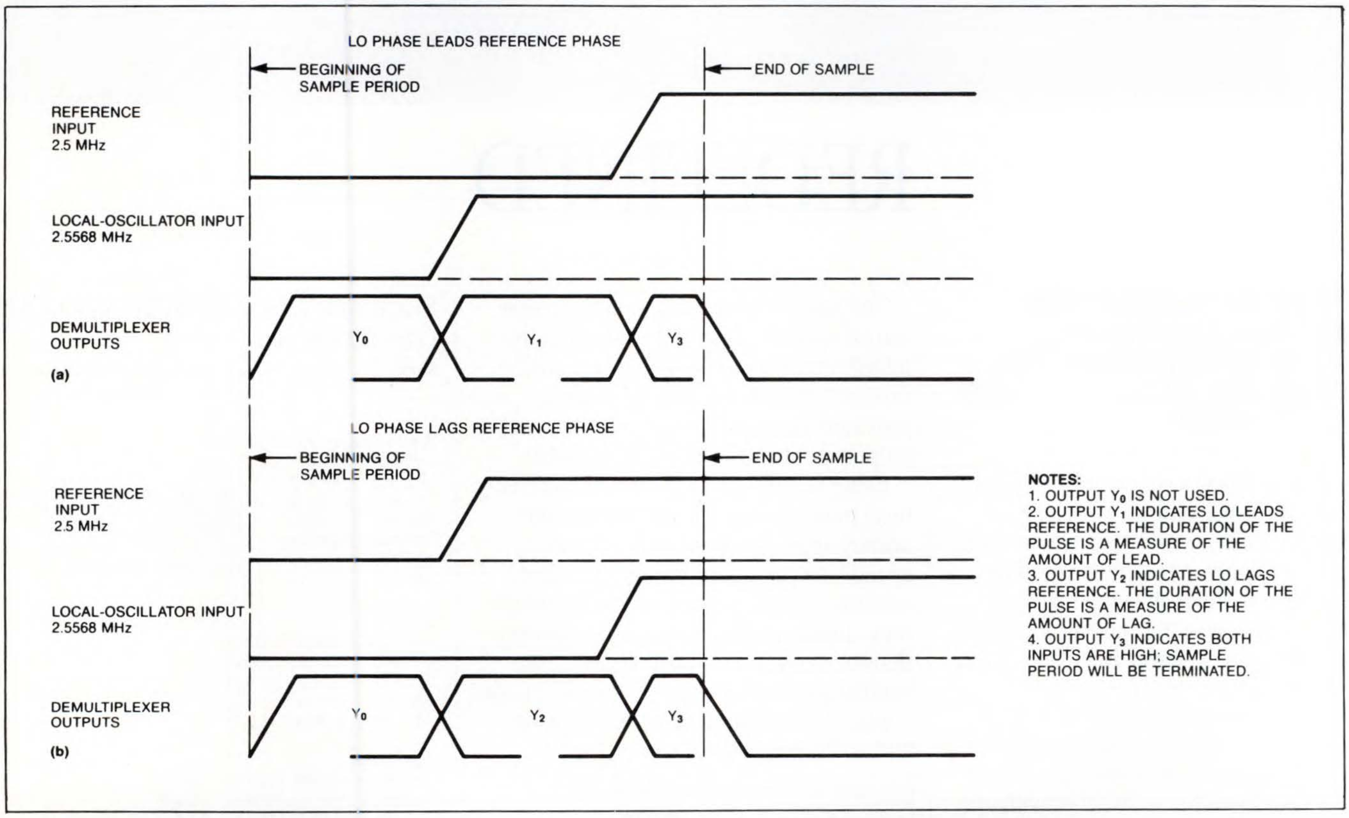

Fig 3—These waveforms depict Fig 2's operation *for the cases of leading phase **(a)** and lagging phase **(b)**.*

Zero-current sensor protects relay contacts

B Erik Valeur
Electronic Instrument & Specialty Corp, Stoneham, MA

The **Fig 1** circuit extends the life of a reed relay by allowing the relay's contacts to open only at moments of zero current. (Destructive arcing can cause rapid contact wear if the contacts open repeatedly while conducting current.) Unlike zero-crossing circuits that predict the zero-current moment, this circuit senses that condition and responds immediately, using a fast relay (K_1, 100 μsec).

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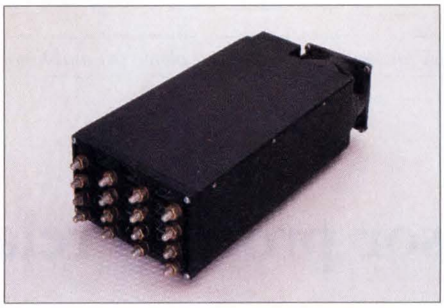

STANDARD 1200 WATT STAKPAK MODELS (110/220 VAC input)

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SP1-1802	5 @ 240				
SP1-1803	12 @ 100				
SP1-1804	15 @ 80				
SP1-1805	24 @ 50				
SP1-1806	28 @ 42				
SP1-1807	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8

Total output power may not exceed 1200 watts for any model, single or multiple output. Lower power StakPak models are available. Please contact the factory.

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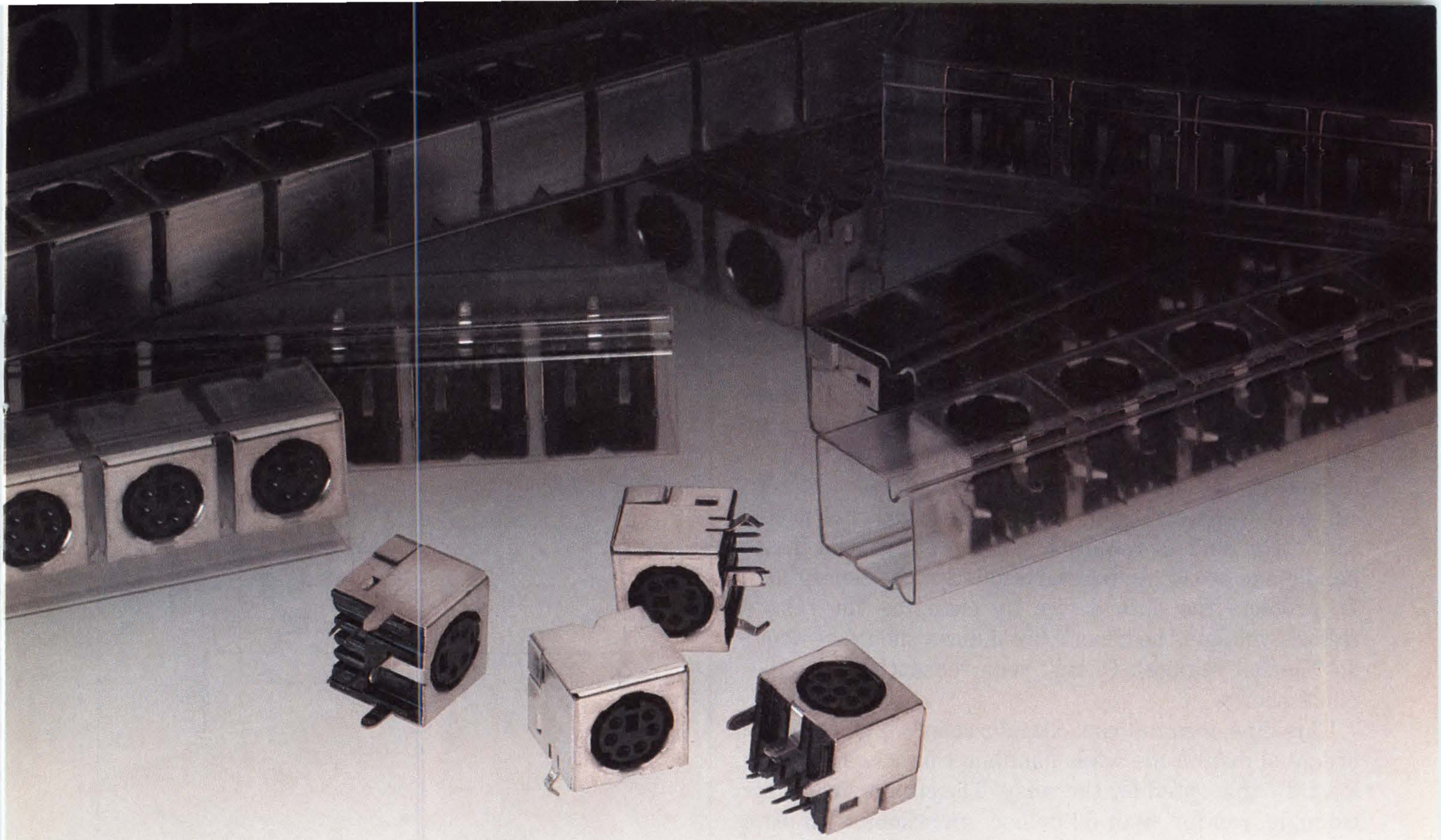
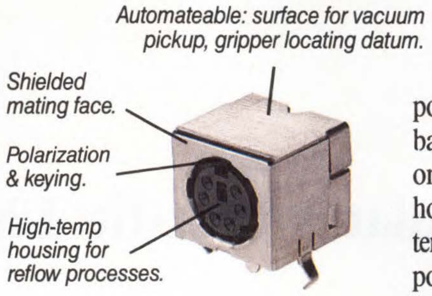
CIRCLE NO 21



Many minis. Mini wait.



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The one-piece shield (in tin-plated copper alloy) uses cantilever beam contacts to provide an uncomplicated low-impedance path from plug shield to pcb ground. An optional hold-down feature secures connector to board during processing.

Available in 3 through 8 positions, these right-angle pcb-mount receptacles feature precision-formed, gold-plated contacts for long life and max reliability, and tin-plated tails for easy soldering. They mate with standard or latching cable connectors, and have built-in polarization and keying.

Design highlights: no stubbing, positive contact retention prevents backout, and the envelope is a cube only ½″ to a side. Plus: 94V-0 rated housing material (tolerates high-temp solder reflow procedures), positioning datum and surface area for vacuum pickup, and packaging for robotic applications.

Call 1-800-522-6752 for product information and the name of your nearby AMP Authorized Distributor. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

CIRCLE NO 10

The on/off switch S_1 controls the application of V_{SUPPLY} to the load by controlling K_1. Load current biases one of the diode pairs on, which in turn activates one of two LEDs in the optocoupler. This action turns on the phototransistor, ensuring that the relay remains closed while load current is flowing regardless of the state of S_1.

Conventional 60-Hz ac current, however, goes through zero twice per cycle, about every 8 msec. At that time the phototransistor turns off, and (if you have opened S_1) K_1 opens, at or near the moment of zero current. Resistor R_1 limits the LED current if necessary. (No limit is required in this circuit, which can handle one or two amperes.) Similarly, the zener diode D_1 protects the opto device by clamping the relay's flyback voltage (the zener's breakdown should be about 4× the coil voltage). D_1 isn't required with the components shown.

This type of circuit can extend a relay's life by several orders of magnitude while handling contact currents at least 2× that rated for the relay. The circuit shown, for example, ran for 40 or 50 million operations with little evidence of wear and no signs of contact breakdown.

EDN

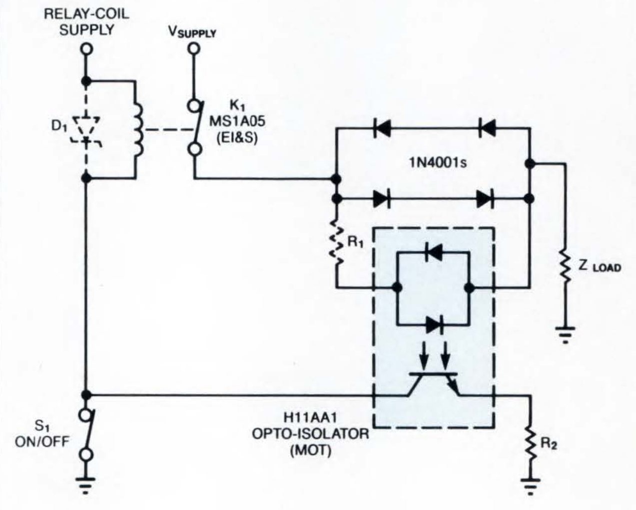


*Fig 1—**You control this power circuit** by operating the S_1 switch; the diodes and the optoisolator prevent a response in the relay except when the relay contacts' current is near zero.*

Program calculates best-fit 1% resistors

Mick Murray
Lab-Line Instruments, Franklin Park, IL

When designing a voltage divider to establish a critical reference voltage in circuits such as comparators and offset-voltage sources, engineers commonly use a non-optimum trial-and-error approach for choosing an acceptable combination of resistors. The Basic program shown in **Fig 1a** calculates the best possible combination of 1% resistors for the voltage-divider circuit in **Fig 1b.** It takes about 11 minutes to run on the Intel MDS-230 computer.

The program prompts you for the most positive string voltage (V_1), the most negative string voltage (V_2), and the voltage that you want the divider to generate (V_3). Once you've entered these values, the program calculates R_1 and R_2 using a table of standard, precision, 1% resistance values (96 values per decade). The program can handle resistor ratios as large as 1000:1. V_1, V_2, and V_3 may be any combination of positive and negative voltages.

To determine the best possible resistor values, the program calculates the voltage divider's output for every combination of the 96 resistor values stored in its table. As the program tests each resistor combination, it stores the best combination that it has found to that point. Each time the program finds a better combination, it stores that combination and prints it out on the screen. The program also displays its progress on the screen.

When the program is finished, it displays values for R_1 and R_2 and the actual voltage that R_1 and R_2 generate when used in the circuit's configuration. You can scale these values to meet your impedance needs. Line 1180 sounds a bell to let you know that the program is finished. **EDN**

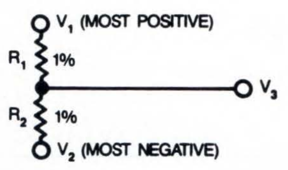
(a)

```
10 REM ******************************************************
20 REM
30 REM      1% PRECISION RESISTOR FINDING PROGRAM
40 REM      COPYRIGHT 1984 MICK MURRAY
50 REM      LAB-LINE INSTRUMENTS INC.
60 REM
70 REM ******************************************************
80 REM
90 FOR T=1 TO 24:PRINT:NEXT
100 PRINT"******************************************************"
110 PRINT:PRINT"     1% PRECISION RESISTOR FINDING PROGRAM"
120 PRINT:PRINT"******************************************************"
130 PRINT:PRINT
140 PRINT"THIS PROGRAM WILL FIND THE TWO CLOSEST VALUES OF"
150 PRINT"THE 96 STANDARD 1% RESISTOR DECADE, TO GENERATE"
160 PRINT"A SPECIFIED VOLTAGE ('V3') DETERMINED BY THE "
170 PRINT"GIVEN STRING VOLTAGES ('V1'&'V2'). IT WILL ASK
180 PRINT"YOU FOR THE STRING VOLTAGES, AND WHAT THE"
190 PRINT"GENERATED (V3) VOLTAGE THAT YOU WISH TO OBTAIN"
200 PRINT"IS. IN ALL CASES, V1 SHOULD BE GIVEN AS THE MOST"
210 PRINT"POSITIVE, V2 THE MOST NEGATIVE, AND V3 ANYWHERE"
220 PRINT"BETWEEN THE TWO."
230 PRINT"     R1 & R2 WILL CONTINUALLY BE DISPLAYED "
240 PRINT"DURING THE COURSE OF COMPUTATION, AS THE"
250 PRINT"TWO CLOSEST VALUES FOUND UP TO THAT TIME."
260 PRINT"     R1 IS THE RESISTOR TIED TO THE MOST POSITIVE VOLTAGE,"
270 PRINT"AND R2 IS THE RESISTOR TIED TO THE MOST NEGATIVE VOLTAGE."
280 PRINT:PRINT:PRINT
290 INPUT"TYPE <RETURN> TO CONTINUE...";BG$
300 FOR J=1 TO 5:PRINT:NEXT J
310 DIM D(96)
320 DIM F(96)
330 INPUT"INPUT V1 (MOST POSITIVE STRING VOLTAGE): ";V1
340 INPUT"INPUT V2 (MOST NEGATIVE STRING VOLTAGE): ";V2
350 IF V2>=V1 THEN 1290
360 INPUT"INPUT V3 (DESIRED GENERATED VOLTAGE): ";V3
370 IF V3=<V2 OR V3>=V1 THEN 1310
380 X=((V1-V2)-V3+V2)/(V3-V2)
390 PRINT "RATIO FOR COMPUTATION =";X
400 REM 'T'IS 1 IF R1>R2;T=2 IF R1<R2
410 IF X<1 THEN 440
420 T=1
430 GOTO 450
440 T=2
450 REM T=1 IF R1>R2 : T=2 IF R2>R1
460 FOR I=1 TO 96
470 READ D(I)
480 NEXT I
490 RESTORE
500 FOR I=1 TO 96
510 READ F(I)
520 NEXT I
530 R1=1
540 R2=1
550 IF X>1 THEN 580
560 A1=1
570 GOTO 590
580 A1=X
590 FOR I=1 TO 96
600 IF Y=0 THEN 690
610 FOR W=1 TO 5:PRINT:NEXT W
620 PRINT Y "OUT OF 96 COMPUTATIONS DONE: BEST SO FAR ARE:"
630 M$="**************************************************"
640 PRINT M$
650 PRINT "R1=" R1", & R2=" R2
```

*Fig 1—**Choosing the best possible resistor combination** for a voltage divider **(b)** is a tedious trial-and-error process. A Basic program **(a)** helps alleviate this tedium by automatically choosing these values for you.*

```
660 PRINT "RATIO OF R1/R2=" R1/R2 ":: DESIRED RATIO IS "X"."
670 PRINT M$
680 PRINT TAB(30);"PLEASE HOLD..."
690 Y=Y+1
700 FOR M=1 TO 96
710 IF T=1 THEN 740
720 Z=F(M)
730 GOTO 750
740 Z=D(I)
750 IF X>9.760002 THEN 780
760 IF X<.102459 THEN 780
770 GOTO 870
780 IF X>97.6 THEN 820
790 IF X<.0102459 THEN 820
800 Z=10*Z
810 GOTO 870
820 IF X>976 THEN 860
830 IF X<1.02459E-03 THEN 860
840 Z=100*Z
850 GOTO 870
860 Z=1000*Z
870 IF T=1 THEN 900
880 A2=D(I)/Z
890 GOTO 910
900 A2=Z/F(M)
910 A3=ABS (A2-X)
920 IF A3 A1 THEN 1000
930 A1=A3
940 IF T=1 THEN 980
950 R1=D(I)
960 R2=Z
970 GOTO 1000
980 R1=Z
990 R2=F(M)
1000 NEXT M
1010 NEXT I
1020 PRINT "DESIRED R1/R2 RATIO WAS ";X
1030 PRINT"THE BEST THAT I CAN DO FOR YOU WITH"
1040 PRINT"THE STANDARD 96 1% RESISTER VALUES"
1050 PRINT"ARE:"
1060 PRINT "R1=   ";R1" OHMS"
1070 PRINT "R2=   ";R2" OHMS"
1080 PRINT "RATIO OF R1/R2 = ";R1/R2
1090 PRINT "FOR V1="V1 "VOLTS; V2="V2 "VOLTS; &V3="V3" VOLTS."
1100 PRINT"**************************************************************"
1110 PRINT"*                                                            *"
1120 PRINT"********* USE R1="R1" OHMS, & R2="R2" OHMS! ********"
1130 PRINT"*                                                            *"
1140 PRINT"**************************************************************"
1150 PRINT"RESULTS IF R1=" R1 ", AND IF R2=" R2 "IS:"
1160 PRINT"V3 WILL BE:   "(((V1-V2)*R2)/(R1+R2))+V2 "VOLTS!!"
1170 PRINT"
1171 REM SOUND ROUTINE: FINISHED CALCULATIONS
1179 PRINT"CALCULATIONS COMPLETED. "
1180 PRINT CHR$(7);:FOR T=1TO1000:NEXT:GOTO1180
1190 END
1200 DATA 1.00,1.02,1.05,1.07,1.10,1.13,1.15,1.18,1.21,1.24
1210 DATA 1.27,1.30,1.33,1.37,1.40,1.43,1.47,1.50,1.54,1.58
1220 DATA 1.62,1.65,1.69,1.74,1.78,1.82,1.87,1.91,1.96,2.00
1230 DATA 2.05,2.10,2.15,2.21,2.26,2.32,2.37,2.43,2.49,2.55
1240 DATA 2.61,2.67,2.74,2.80,2.87,2.94,3.01,3.09,3.16,3.24,3.32
1250 DATA 3.40,3.48,3.57,3.65,3.74,3.83,3.92,4.02,4.12,4.22,4.32,4.42
1260 DATA 4.53,4.64,4.75,4.87,4.99,5.11,5.23,5.36,5.49,5.62,5.76,5.9
1270 DATA 6.04,6.19,6.34,6.49,6.65,6.81,6.98,7.15,7.32,7.5,7.68,7.87
1280 DATA 8.06,8.25,8.45,8.66,8.87,9.09,9.31,9.53,9.76
1290 PRINT:PRINT"V1 MUST BE THE MOST POSITIVE VOLTAGE, AND"
1300 PRINT"V2 MUST BE THE MOST NEGATIVE VOLTAGE! PLEASE RE-INPUT:":PRINT:GOTO 33(
1310 PRINT:PRINT"V3 IS THE DESIRED GENERATED VOLTAGE DETERMINED BY R1 AND R2,"
1320 PRINT"AND MUST LIE BETWEEN V1 AND V2!"
1330 PRINT"   PLEASE RE-ENTER DESIRED V3 VOLTAGE:":PRINT:GOTO 360
```

(b)



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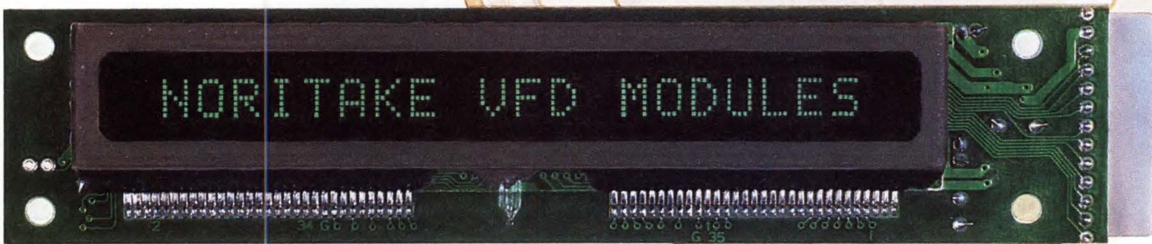


Model CU205SCPB

DOT CHARACTER DISPLAY MODULES

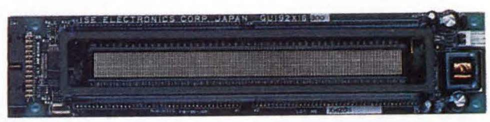
CHARACTER FORMAT	MODEL NUMBER	NUMBER OF CHARACTERS	CHARACTER HEIGHT (MM)	INPUT (SERIAL/ PARALLEL)	BI-DIRECT BUS
5 × 7 DOT MATRIX	CU165SCPB-S	1 × 16	5.0	S/P	
	CU169SCPB-L	1 × 16	9.0	P	X
	CU205SCPB-S	1 × 20	5.0	S/P	
	CU209SCPB-L	1 × 20	9.2	P	X
	CU2015SCPB-L	1 × 20	15.1	P	X
5 × 7 DOT MATRIX PLUS CURSOR	CU406SCPB-S	1 × 40	5.0	P	X
	CU20026SCPB-S	2 × 20	5.1	P	X
	CU40026SCPB-S	2 × 40	5.0	P	X
	CU40046SCPB-S	4 × 40	5.0	S/P	X
	CU40066SCPB-S	6 × 40	5.0	S/P	X
	CU40086SCPB-S	8 × 40	5.0	P	X

The models shown are typical examples of the broad selection available for immediate delivery. Contact our nearest Sales Office or Representative to help select the right Noritake VFD for your application as well as for details on costs, custom designs, etc.

DOT MATRIX DISPLAY MODULES

DOT MATRIX FORMAT (DOTS/LINE × NO. OF LINES	MODEL NUMBER	NO. OF LINES AND CHARACTERS/LINE (5 × 7 DOT CONFIGURATION)	GRAPHICS CAPABILITY
192 × 16 (3072 DOTS TOTAL)	GU192X16	2 × 32	YES
256 × 16 (4096 DOTS TOTAL)	GU256X16	2 × 42	YES
256 × 64 (16,384 DOTS TOTAL)	GU256X64	8 × 42	YES

Model GU192X16



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CIRCLE NO 11

One supply powers precision bridge circuit

Jerry Graeme
Burr-Brown Corp, Tucson, AZ

Precise amplification and a high common-mode rejection ratio make an instrumentation amplifier well suited to the task of monitoring the output of a resistive transducer bridge. For systems with only one power supply, **Fig 1** shows how you can connect the bridge, the instrumentation amp, and an op amp to provide a buffered reference for the instrumentation amp's output.

For linear operation, the amplifier inputs (and outputs) must come within no more than several volts of either ground or V^+. Accordingly, the bridge properly biases both amplifier inputs, and the instrumentation amp's high CMRR ensures little error from this large offset.

The OPA111AM buffers the reference node of the bridge and applies that voltage to the instrumentation amp's REF terminal. (Most instrumentation amplifiers include a REF terminal, which may be biased to offset the output.) You measure between the amplifier outputs to exclude the fixed output offset.

The op amp output can serve as a reference common for all connections following the instrumentation amp—this output provides low impedance over a frequency range well beyond that of the bridge signal. To handle higher-frequency currents, connect capacitance between the op amp output and ground; if necessary, decouple this capacitance with a small resistor within the op amp's feedback loop.

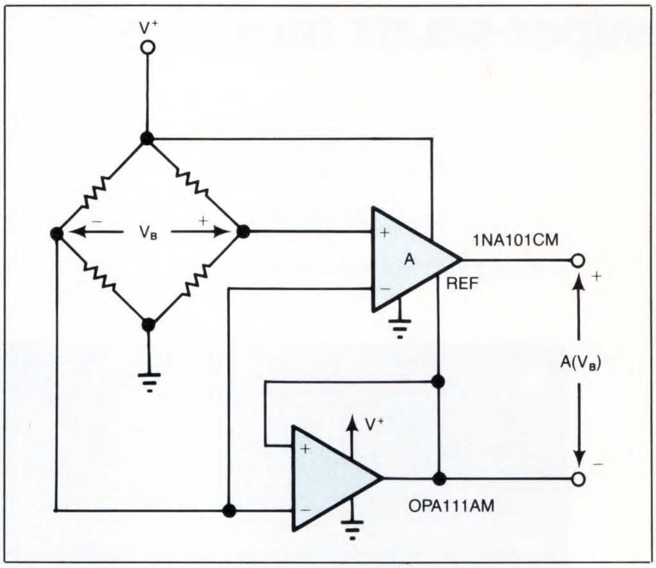


Fig 1—Use one power supply *to excite the bridge and to develop a buffered output signal in this precision circuit.*

The error introduced by the additional op amp is small. The input bias current I_B of the op amp creates a bridge error of $I_B \times R/2$, where R is the resistance of one leg of the bridge. Input offset voltage has no effect on the output voltage; it adds to the output offset with respect to ground, which is excluded from the measurement. **EDN**

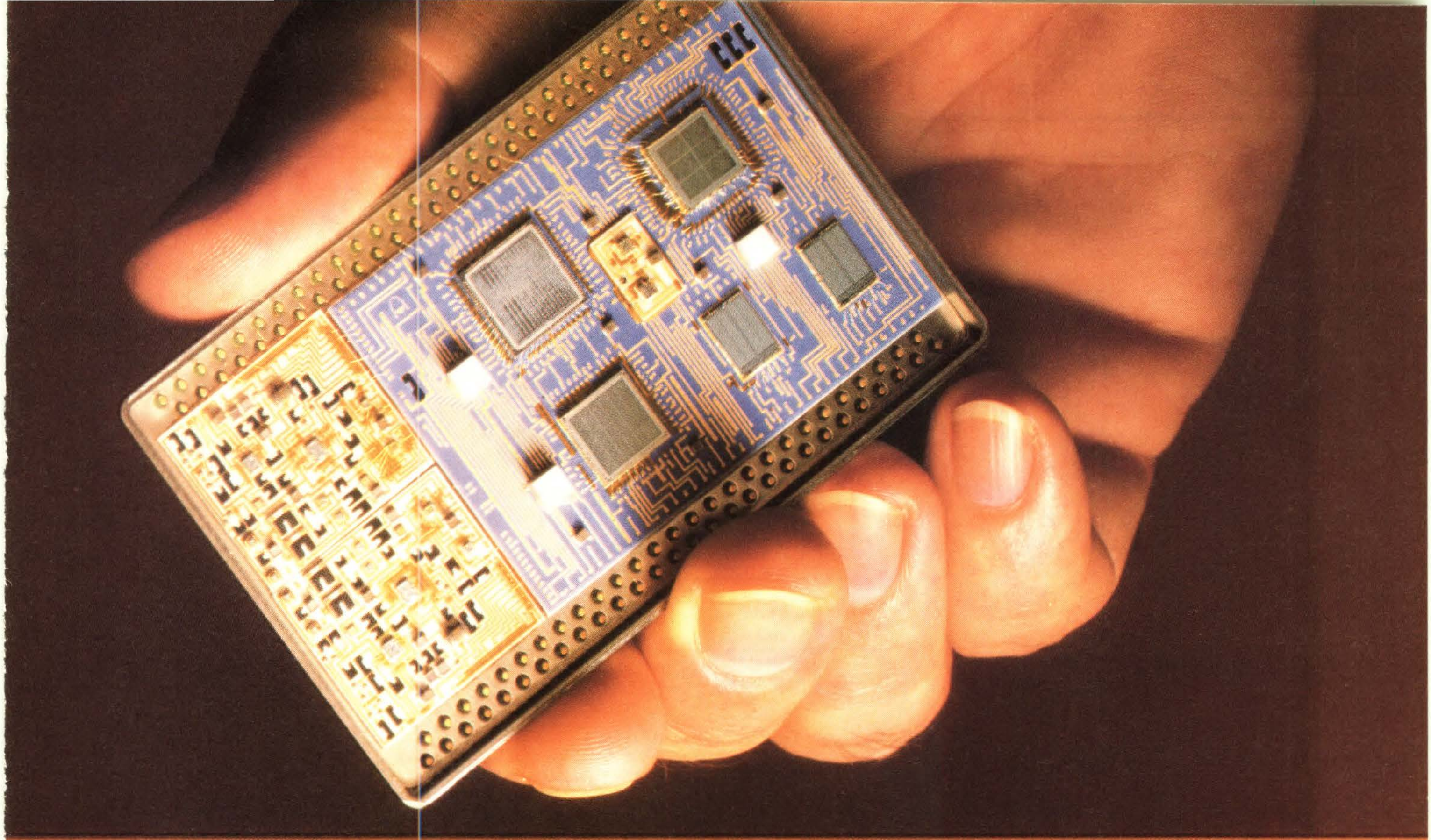
Switching improves regulator efficiency

Fran Hoffart
National Semiconductor Corp, Santa Clara, CA

By using **Fig 1**'s circuit to lower the input voltage to a series-pass regulator when its output voltage is adjusted to a low value, you can minimize the voltage drop across the regulator. This decreases the regulator's dissipation and improves its efficiency.

The problem of large voltage drops across regulators occurs in linear power supplies whose output voltages are adjustable over a wide range. Low-voltage settings can impose high power-dissipation requirements on series-pass regulators; you'd have to attach large heat sinks to keep the regulator from overloading. Also, many regulators have foldback-current-limiting circuits, which decrease the amount of current the regulator can deliver as the difference between the input and output voltages increases.

As one solution, when the regulator's output voltage is adjusted to a low value, you lower its input voltage by manually switching between secondary taps on a power transformer. Alternatively, you can switch from a full-wave center-tap rectifier circuit to a full-wave bridge rectifier circuit when you need higher output voltages. This method also uses the transformer more efficiently than the tap-switching method, allowing higher load currents in the full-wave center-tap circuit. **Fig 2** shows how to use an spdt switch or relay to select



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CIRCLE NO 12

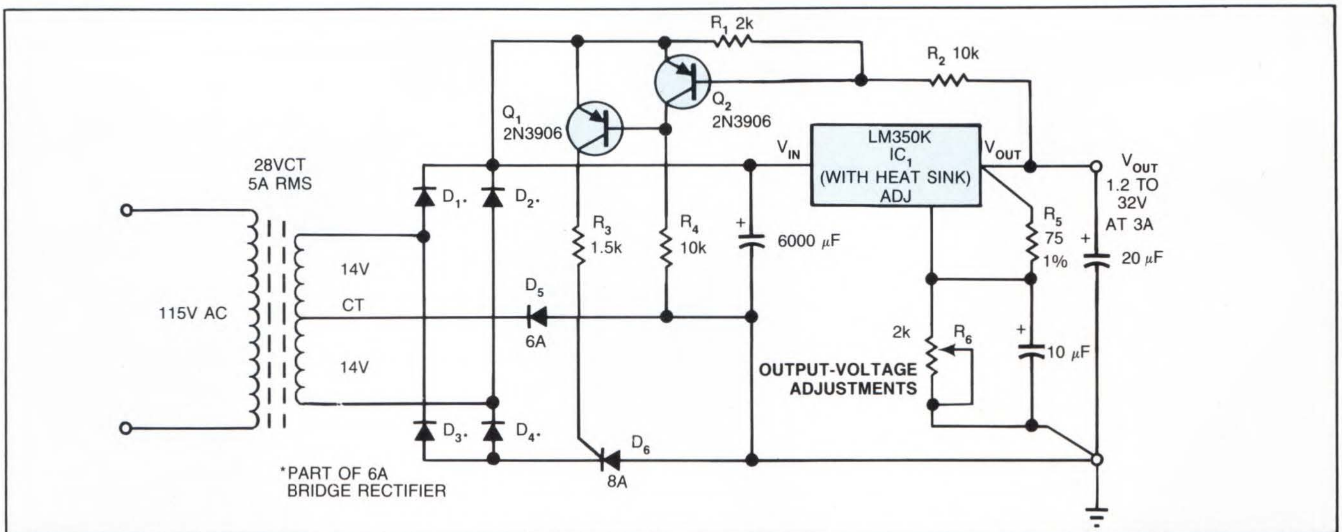

Fig 1—***Electronically switching from a full-wave bridge*** *to a full-wave center-tap circuit in this series-pass regulator* ***lowers the voltage*** *across a rectifier, reduces its dissipation, and eliminates the need for a large heat sink.*

one of the rectifier circuits; the output voltage of the full-wave bridge circuit is twice that of the full-wave center-tap circuit.

Fig 1's circuit switches between rectifier circuits automatically and in proportion to the output-voltage setting and the load. **Fig 3** shows the circuit's performance for three output-voltage settings and each setting's respective input voltage. As the output voltage increases, so does the input voltage. This effect greatly decreases power dissipation in the regulator and lets the regulator supply more current to the load.

In detail, the operation proceeds as follows. SCR D_6 switches between the two rectifier configurations. When D_6 is off, the circuit functions as a full-wave center-tap rectifier using diodes D_1, D_2, and D_5. It applies 17V plus any ripple to the regulator's input. The

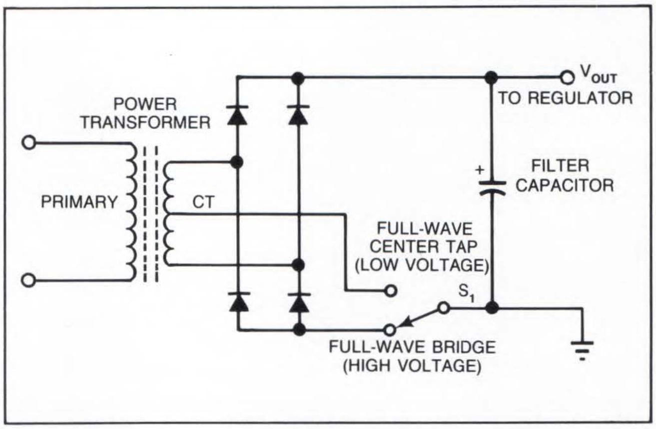

Fig 2—This manual-switching circuit *shows how lifting one point above ground changes a full-wave bridge to a full-wave center-tap rectifier circuit.*

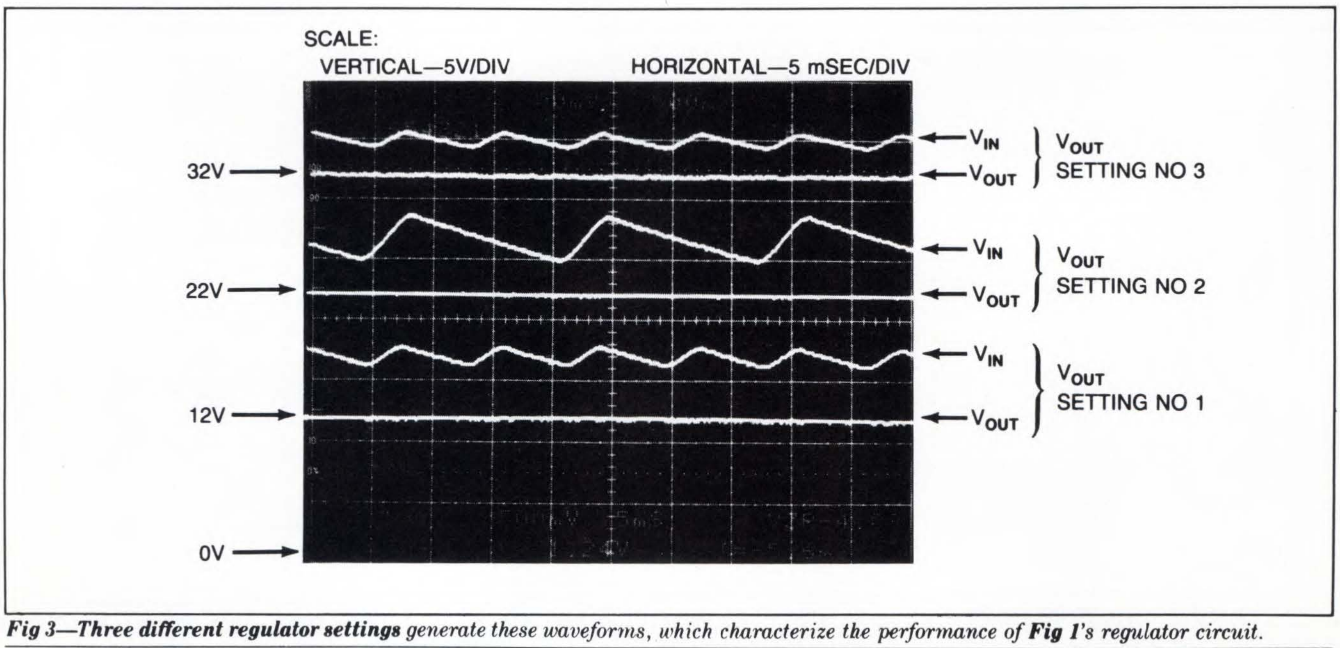

Fig 3—Three different regulator settings *generate these waveforms, which characterize the performance of* ***Fig 1****'s regulator circuit.*

voltage across the regulator's input and output supplies base drive to Q_2. As long as this voltage is high enough (approximately 3V) to keep Q_2 on, Q_1 and SCR D_6 remain off. (When Q_2 is on, it removes the drive from Q_1, thereby turning it off and preventing the SCR from being switched on.)

When you increase the regulator's output voltage, the voltage across the regulator drops below 3V and Q_2 turns off. This action turns Q_1 on, supplying gate drive to the SCR and changing the rectifier circuit from a full-wave center tap to a full-wave bridge using diodes D_1, D_2, D_3, and D_4. The voltage at the regulator's input increases on a cycle-by-cycle basis, depending on the load current needed.

If you're using a light load, the circuit may switch rectifiers every 10 or 20 cycles, depending on demand **(Fig 3)**. With heavier loads, the circuit will switch more often. For high output voltages, the SCR is on every cycle and the input voltage is at its 35V maximum.

When you build this circuit, keep a few points in mind: In the intermediate voltage settings, the SCR doesn't conduct every cycle, and the peak diode currents are higher than they would be if the diodes conducted every cycle. Thus you'll have to choose diodes with a current rating that's two or more times higher than would normally be required. Also, when choosing a transformer, remember that you get less output current from the transformer when using a full-wave bridge, so specify the current rating accordingly. **EDN**

XOR gate doubles counting frequency

Andrew Gorajek
Adelaide Microelectronics Centre, Technology Park, The Levels, South Australia

Suitable for noisy industrial environments and requiring no passive components, the frequency doubler in **Fig 1** inserts an XOR gate into the first stage of a digital counter. The circuit works with virtually any counter and XOR gate. An XOR gate, in series with the counter's clock input, works as a digitally controlled inverter. The gate gets its control signal from the counter's first-stage output, Q_0.

After resetting, output Q_0 is low and the MC14070B XOR gate, IC_1, acts as a noninverting buffer. Because the MC14518 counter, IC_2, counts on the rising edges of the clock signals, the first positive-going transition of the input signal makes IC_2's Q_0 output go high **(Fig 1b)**, which makes IC_1 an inverter. The next negative-going transition of the input signal appears to the counter's clock input as a positive-going transition and change's Q_0 to low. Further transitions of the input signal will cause this sequence to repeat. The resulting clock signal has twice the frequency of the input and consists of short pulses whose width is the sum of the propagation delays introduced by the counter and the XOR gate (t_{P1} and t_{P2}). **EDN**

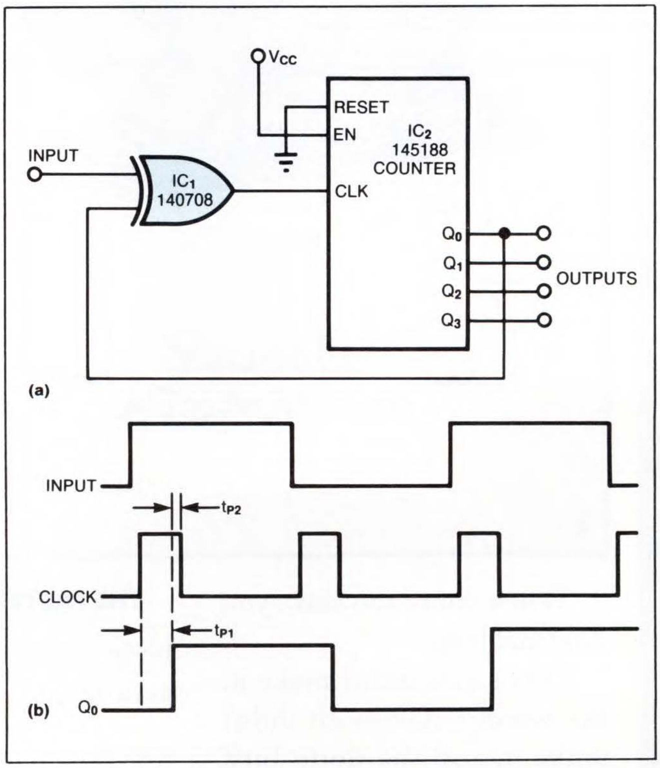

Fig 1—An XOR gate in series with a counter's clock input *effectively doubles the input-clock rate. The XOR gate transforms the input signal into a series of short pulses whose width is the sum of the gate's and the counter's propagation delays. Feeding back the counter's Q_0 output to the XOR gate makes the gate a controlled inverter. Inverting the negative-going input transitions allows the counter to count both positive- and negative-going edges.*

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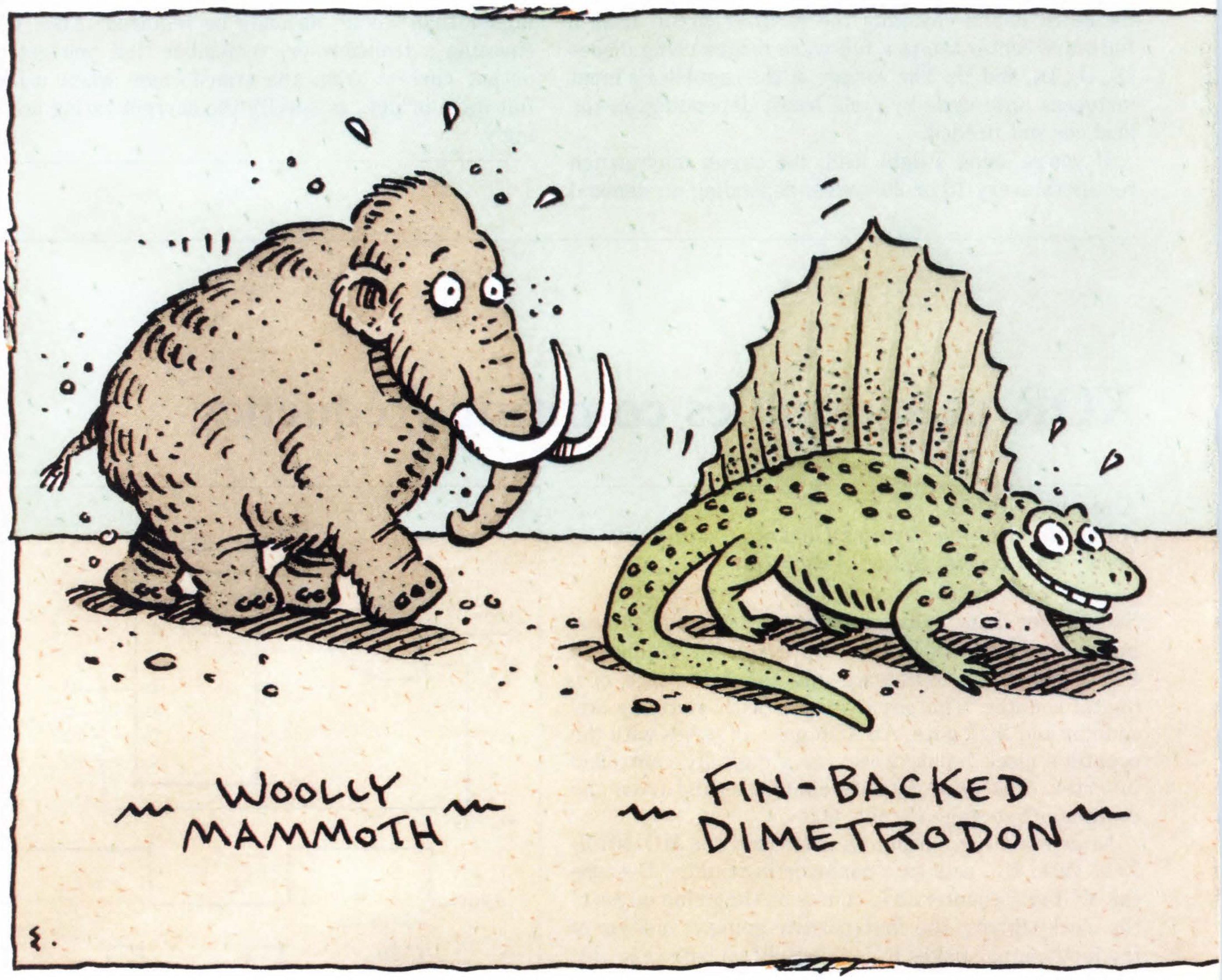

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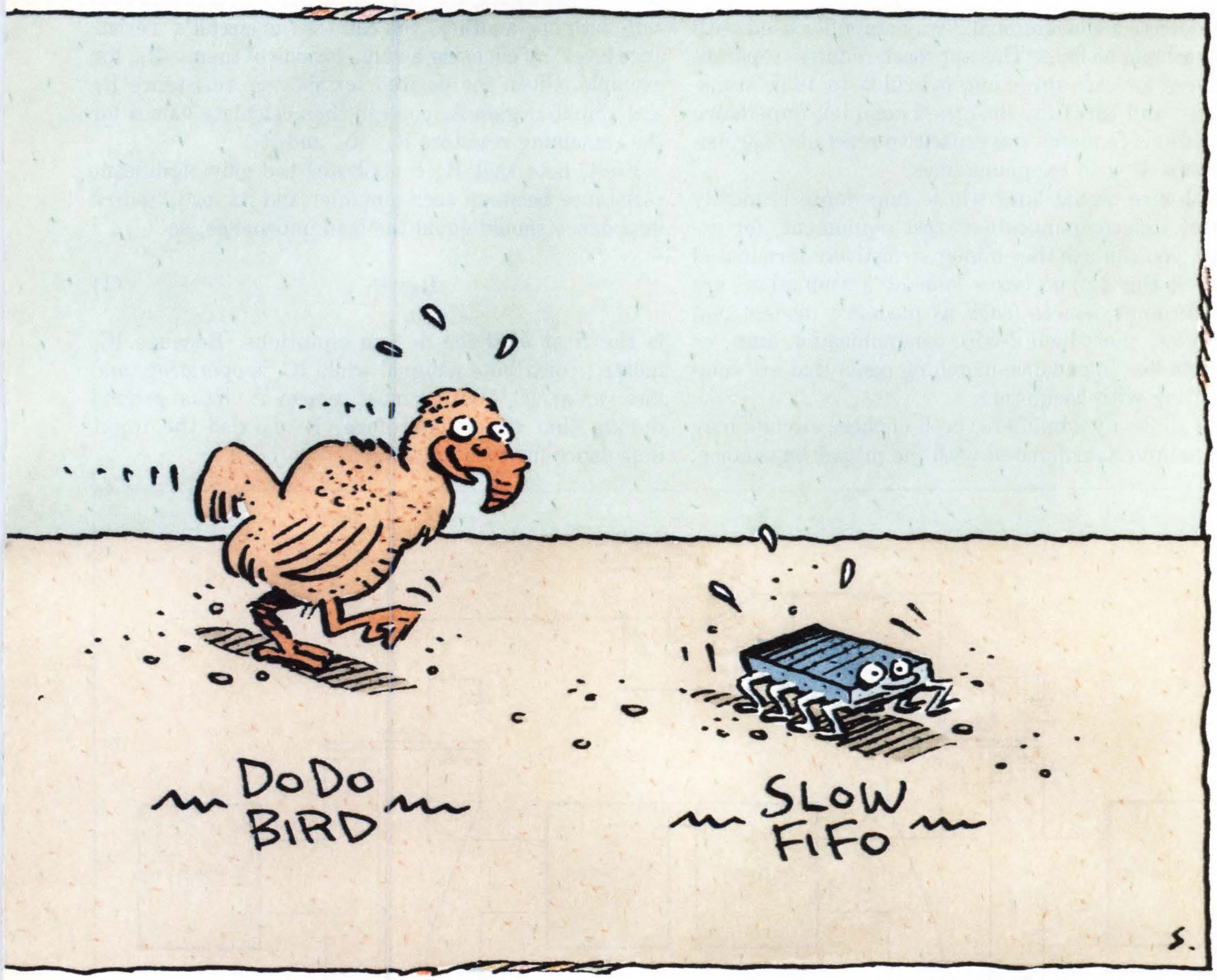

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Two-way amplifier uses few parts

Rudy Stefenel
Luma Telecom, Santa Clara, CA

Fig 1 depicts a conventional 2-way amplifier used with 2-wire telephone lines. This approach requires separate amplifiers for each direction, hybrid 2- to 4-line transformers, and carefully designed complex-impedance terminations to match the capacitive reactance normally associated with telephone lines.

For 2-wire signal lines whose impedance is mostly resistive (telecommunications test equipment, for example), you can use the simpler, resistively terminated circuit of **Fig 2.** The boxes labeled "termination" are two telecomm devices (such as modems, modem test equipment, short-haul 2-wire communication lines, or minimum-loss impedance-matching pads) that are communicating with each other.

Like all 2-way amplifiers, both of these circuits may oscillate unless terminated with the proper impedance. Moreover, higher audio gain imposes greater accuracy constraints on the terminating impedance values. Because resistors R_A, R_B, R_C, and R_D have a fixed relationship with one another, you can set the circuit's "resistance level" by choosing a value for one of them—R_D, for example. Given the desired termination resistance R_L and amplifier gain A, you can then calculate values for the remaining resistors R_A, R_B, and R_C.

First, note that R_A contributes the only significant resistance between each amplifier and its load. Source impedance should equal the load impedance, so

$$R_A = R_L \quad (1)$$

is the first of three design equations. Because IC_2 mustn't contribute a signal while IC_1 is operating (and vice versa), IC_2's output must remain at virtual ground during that time. Therefore, R_A is also the input impedance for each amplifier.

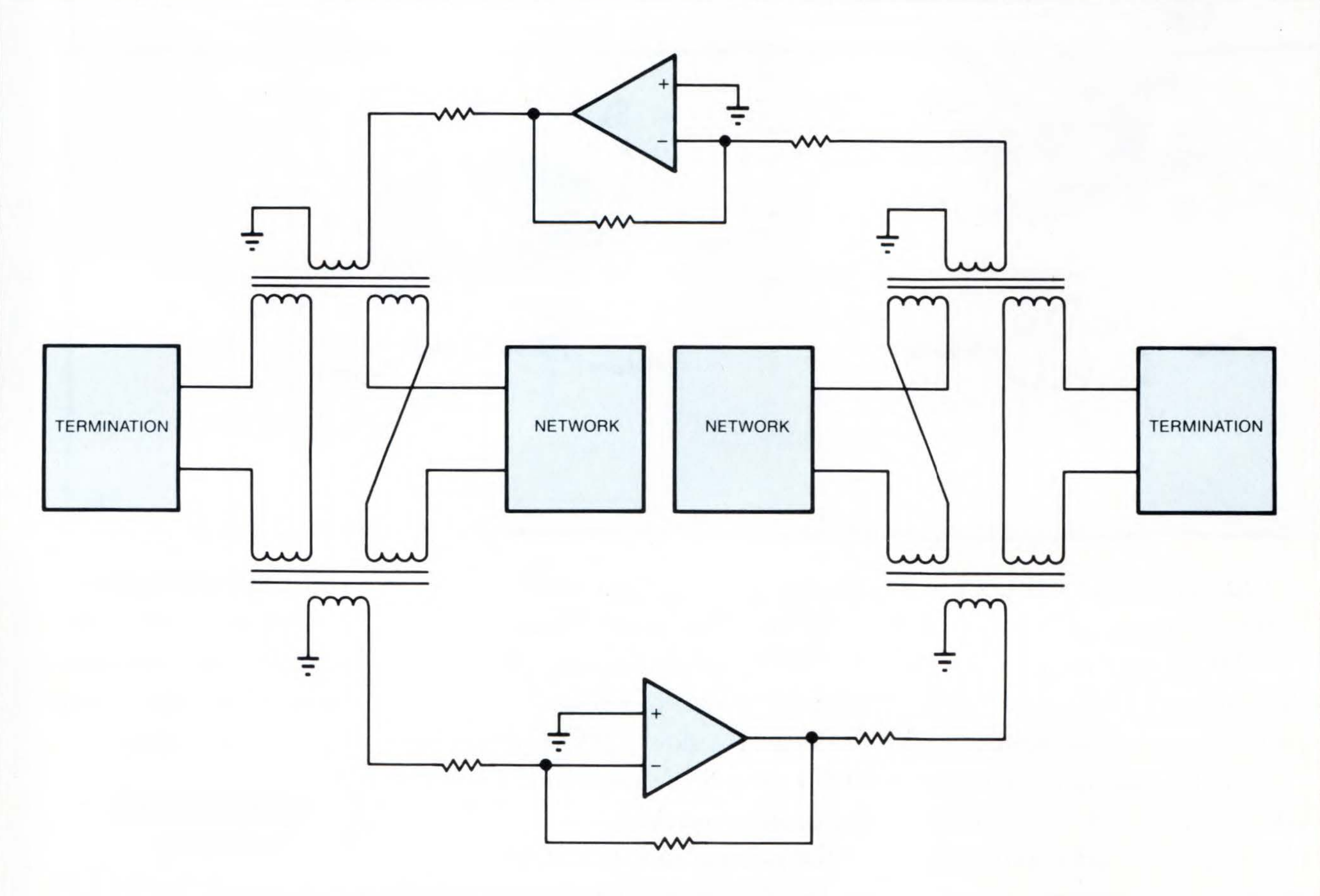

Fig 1—This schematic shows a typical 2-way amplifier *used with telephone lines.*

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Next, the gain from IC_1's noninverting input to its output is

$$\frac{R_D+\dfrac{R_CR_B}{R_C+R_B}}{\dfrac{R_CR_B}{R_C+R_B}},$$

and the gain from IC_1's output to R_L is ½ because $R_A=R_L$ (**Eq 1**). The product of these gains must equal the given gain A:

$$A=\frac{1}{2}\left[\frac{R_D+\dfrac{R_CR_B}{R_C+R_B}}{\dfrac{R_CR_B}{R_C+R_B}}\right]. \quad (2)$$

To ensure that no signal is emitted from IC_2 when only the lefthand signal source is active, IC_2's differen-

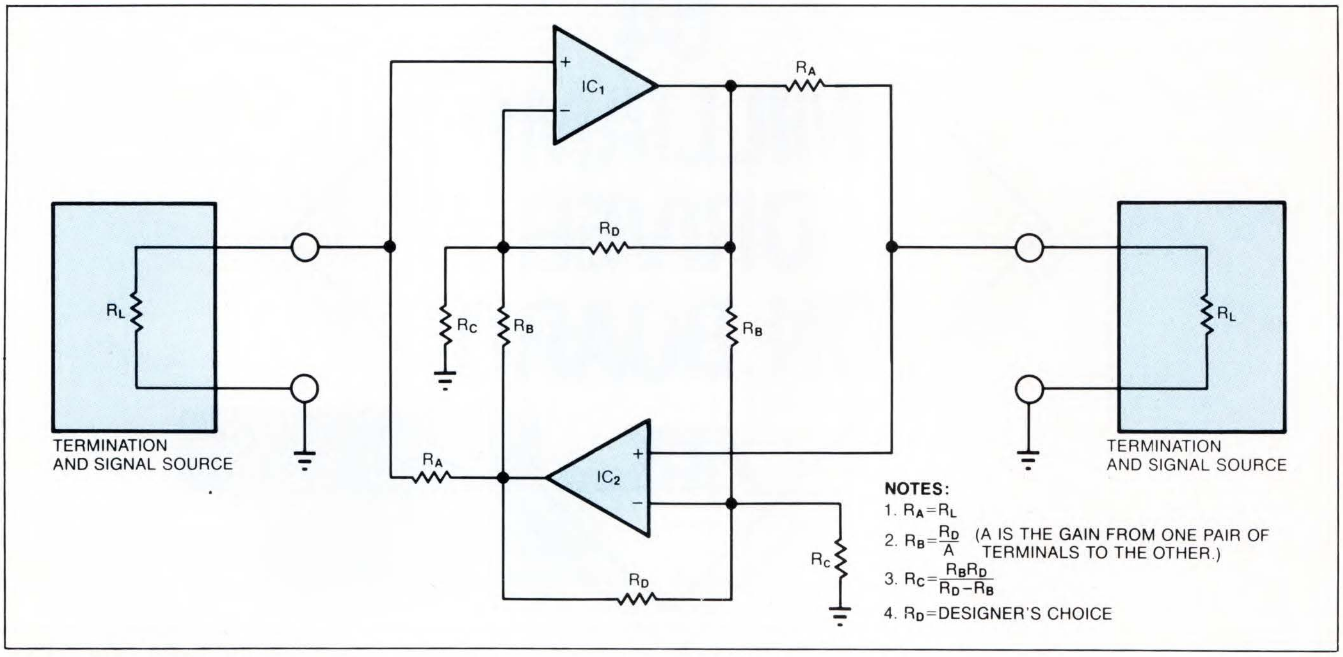

Fig 2—This simpler 2-way amplifier *is suitable for lines whose impedance is primarily resistive.*

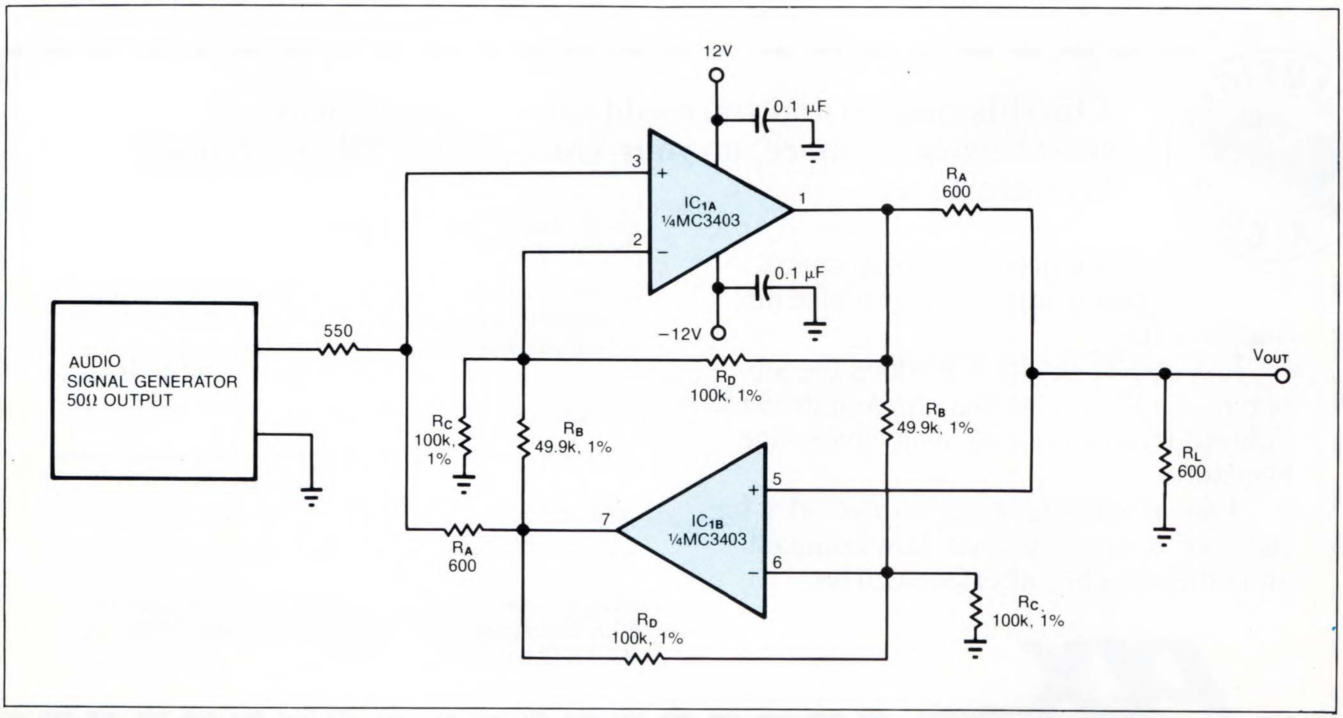

Fig 3—Based on the circuit of Fig 2, *this 2-way amplifier provides a gain of 2 between 600Ω terminations.*

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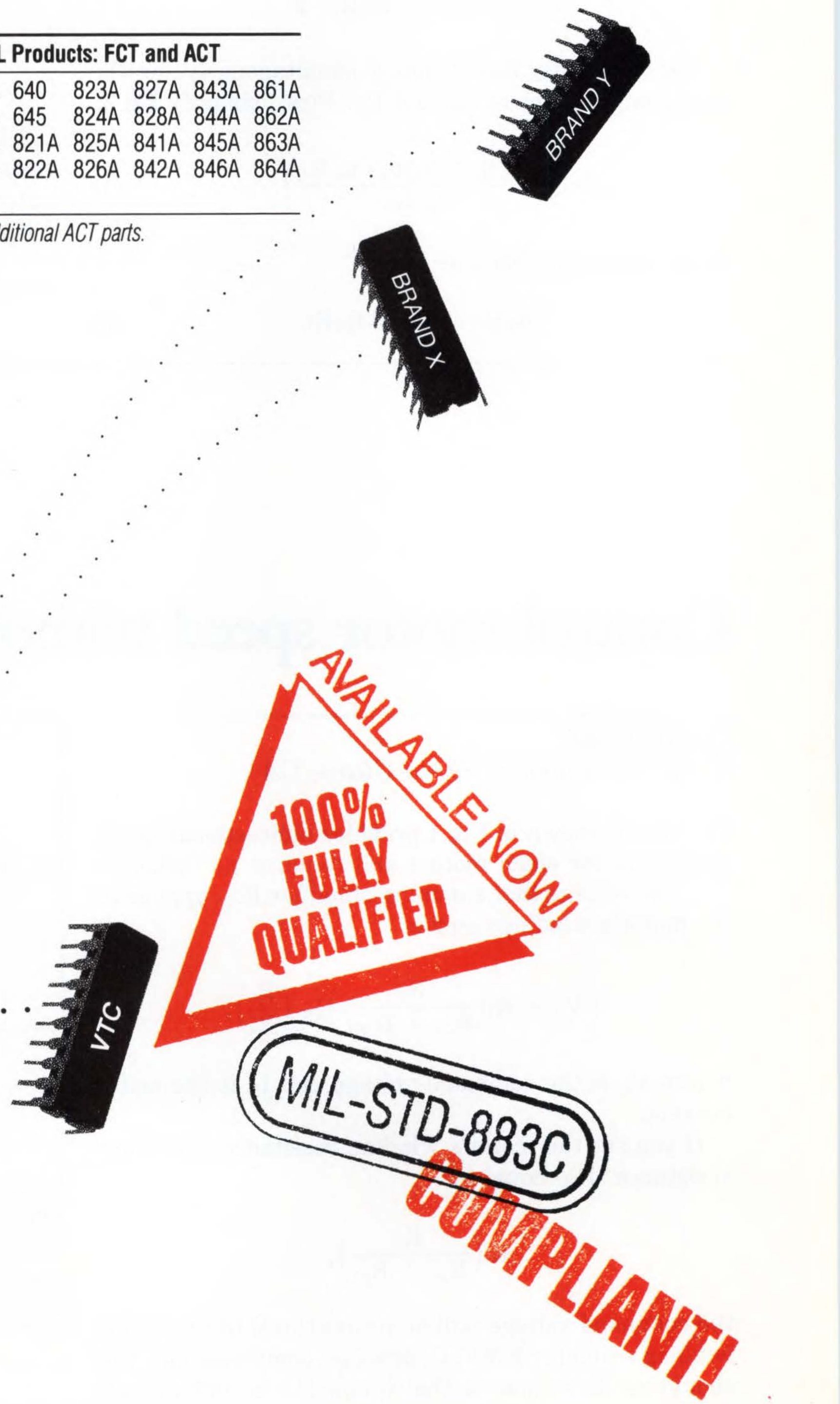

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tial input must be zero. This is so if IC_2's inputs are equal, which implies equal voltage dividers:

$$\frac{\frac{R_C R_D}{R_C+R_D}}{R_B+\frac{R_C R_D}{R_C+R_D}}=\frac{R_L}{R_A+R_L}=\frac{1}{2}.$$

Simplifying this equation yields

$$\frac{R_C R_D}{R_B R_C+R_B R_D+R_C R_D}=\frac{1}{2}. \quad (3)$$

You can solve **Eqs 2** and **3** simultaneously for the remaining unknowns R_B and R_C. First, simplify **Eq 2:**

$$A=\frac{1}{2}\left(\frac{R_D R_C+R_D R_B+R_C R_B}{R_C R_B}\right) \quad (4)$$

Next, rearrange **Eq 3** as

$$R_B R_C+R_B R_D=R_C R_D, \quad (5)$$

and substitute into **Eq 4:**

$$A=\frac{1}{2}\left(\frac{R_D R_C+R_C R_D}{R_C R_B}\right)=\frac{R_D}{R_B}.$$

Therefore,

$$R_B=\frac{R_D}{A}$$

is the second design equation.

For the last design equation, solve **Eq 5** for R_C:

$$R_C=\frac{R_B R_D}{R_D-R_B}.$$

Fig 3 shows an example of a circuit using 600Ω resistive loads and a gain of 2. The signal at IC_{1B}'s output measures only 2 to 3% of the signal-generator output. **EDN**

Control motor speed without tachometer

David Wolze
KLA Instruments, Santa Clara, CA

The circuit shown in **Fig 1** provides bidirectional speed regulation for small motors and requires no tachometer. The voltage that summing amplifier IC_{1A} applies to the motor's windings equals

$$\left(V_C + R_1\left(\frac{R_3}{R_{2A} + R_{2B}}\right)\right)I_M\left(\frac{R_6}{R_5}\right),$$

where V_C is the command voltage and I_M is the motor current.

If you set the motor's winding resistance and brush resistance (R_M) equal to

$$R_1\left(\frac{R_3}{R_{2A} + R_{2B}}\right),$$

the command voltage will be proportional to the motor winding's counter EMF. C_1 provides compensation. You should set R_1's value so that it equals 5 to 10% of R_M's value. You can generally find R_M's value in a motor's spec sheet. **EDN**

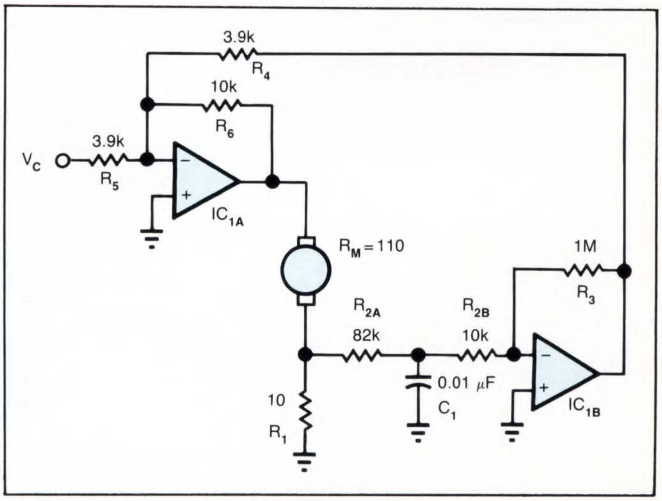

Fig 1—This dc servo-motor circuit *provides bidirectional motor-speed control without requiring a tachometer.*

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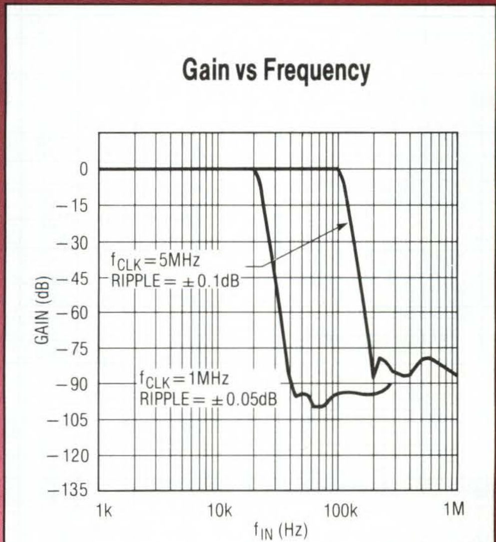

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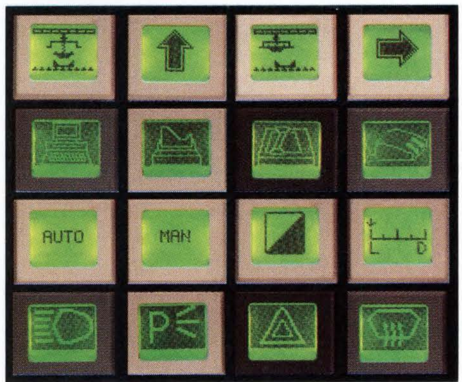

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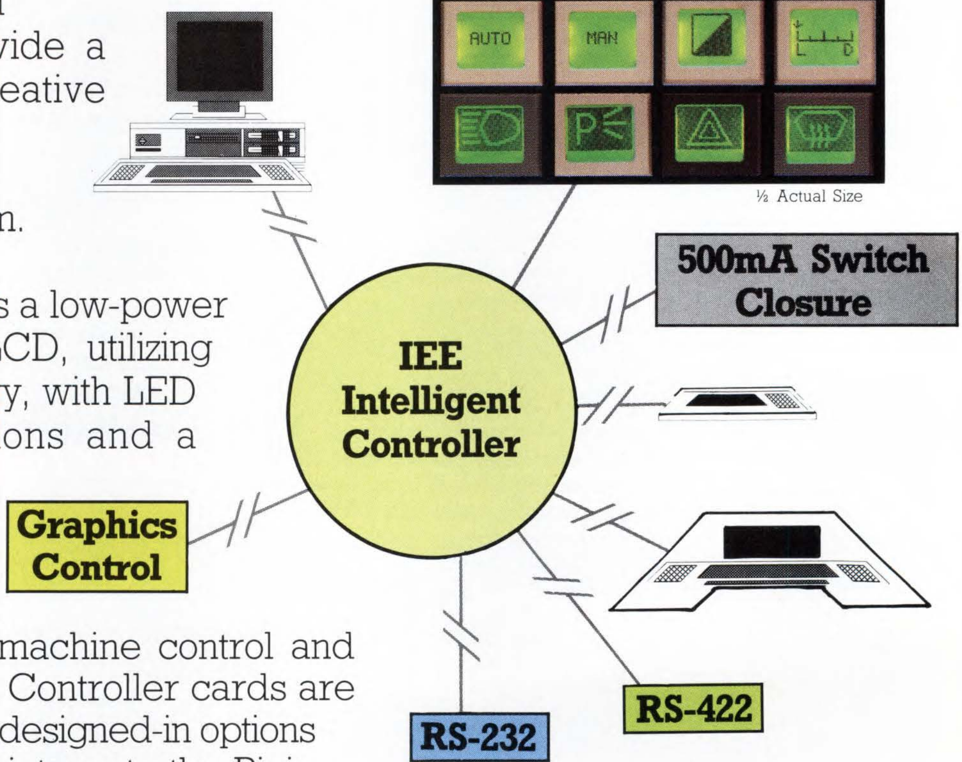

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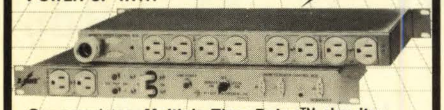

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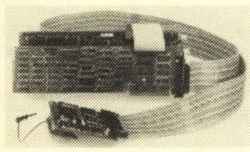

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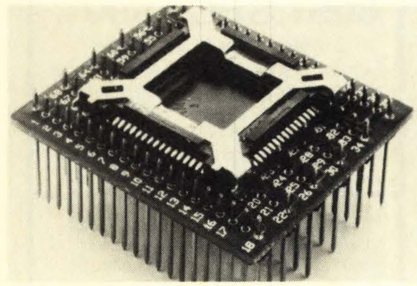

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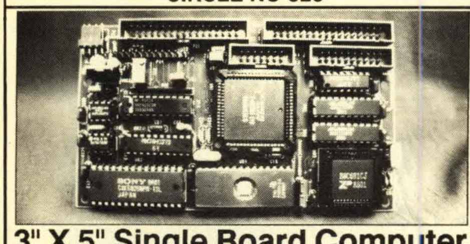

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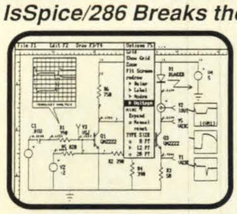

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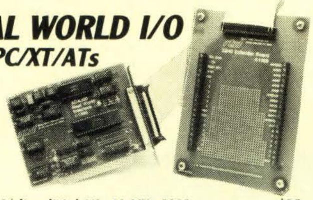

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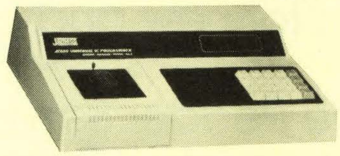

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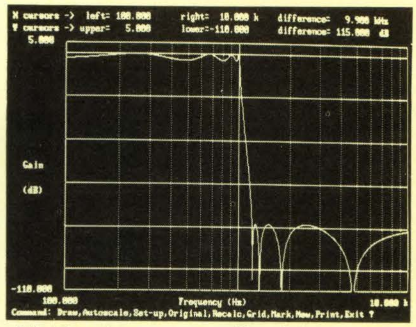

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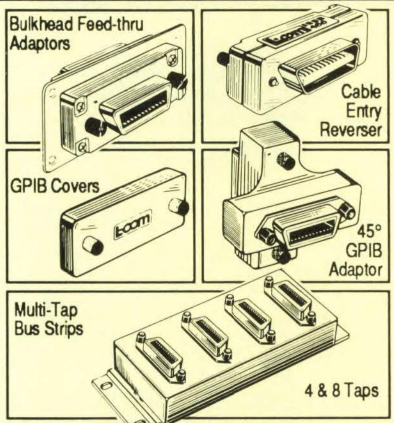

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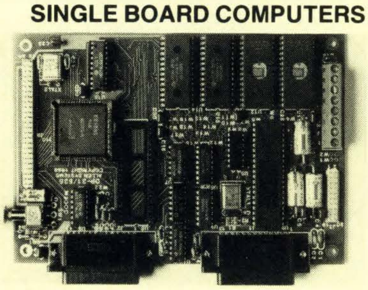

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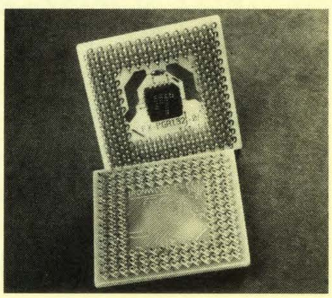

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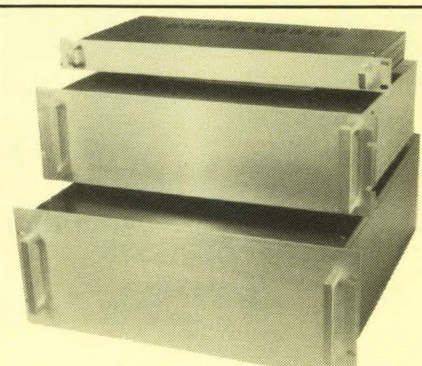

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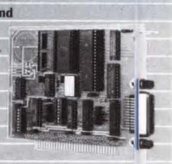

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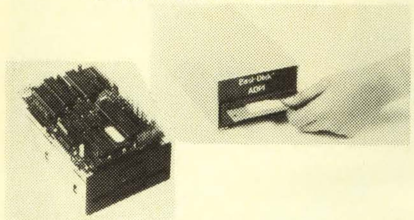

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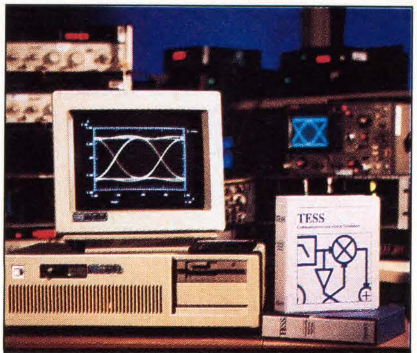

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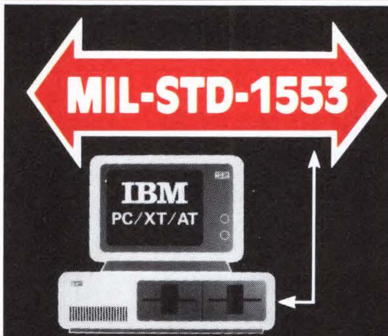

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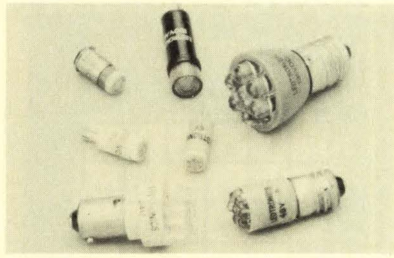

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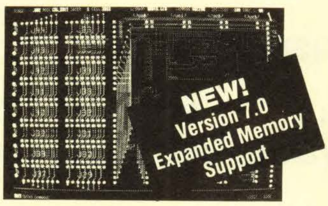

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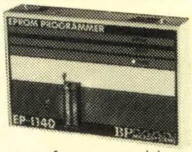

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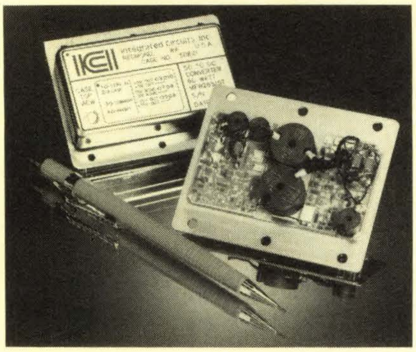

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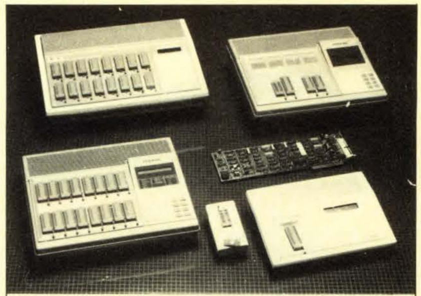

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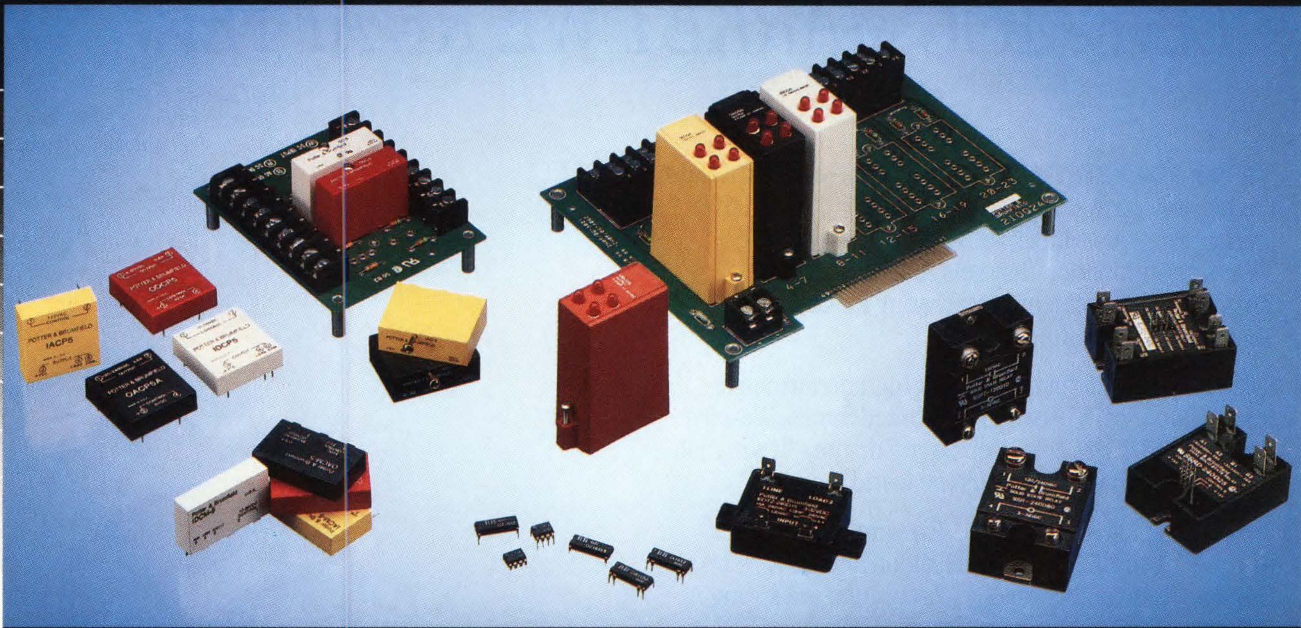

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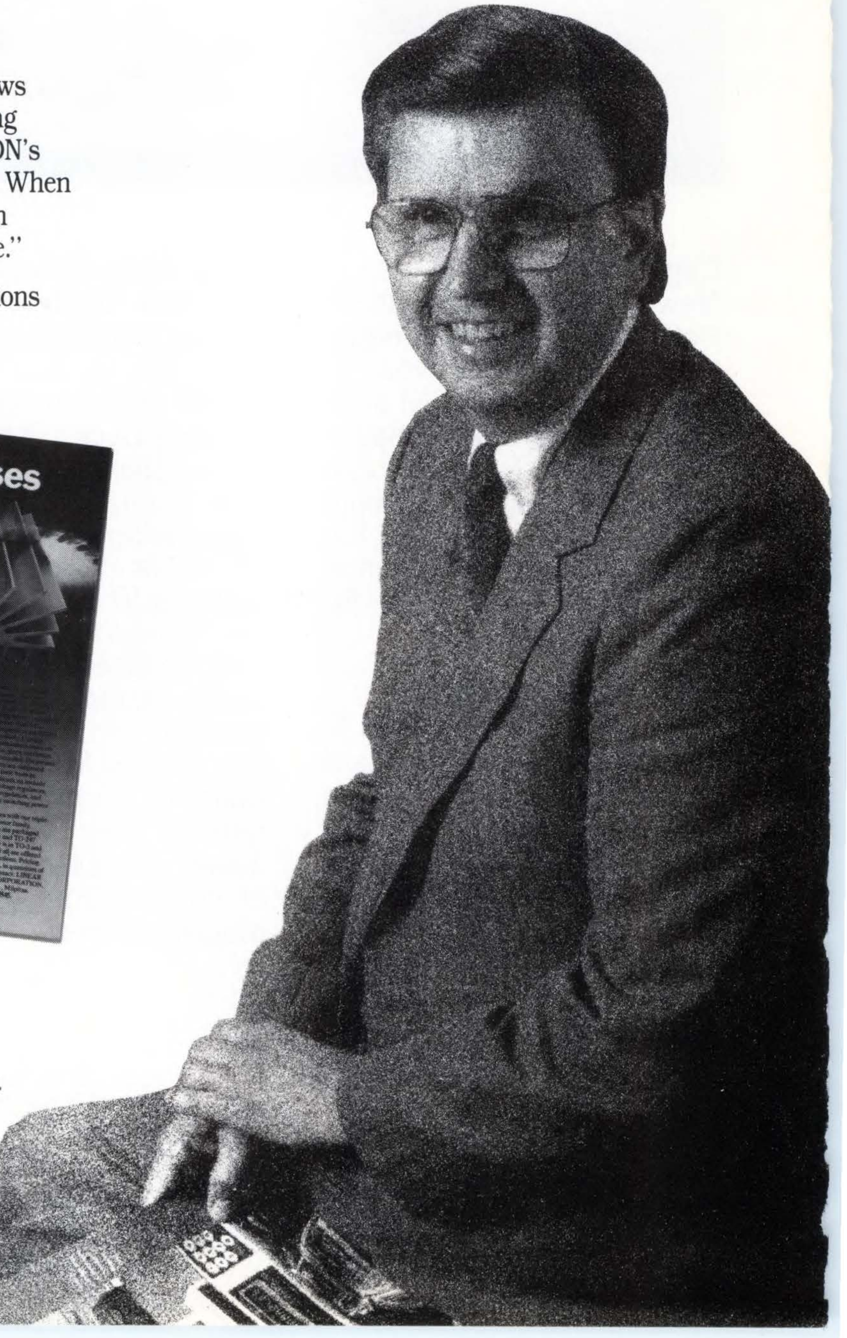

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SCANDINAVIA
Stuart Smith
27 Paul St
London EC2A 4JU UK
01-628 7030
Telex: 914911; FAX: 01-628 5984

FRANCE/ITALY/SPAIN
Alasdair Melville
27 Paul St
London EC2A 4JU UK
01-628 7030
Telex: 914911; FAX: 01-628 5984

WEST GERMANY/SWITZERLAND/AUSTRIA
Wolfgang Richter
Sudring 53
7240 Horb/Neckar
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49-7451-7828; Telex: 765450

EASTERN BLOC
Uwe Kretzschmar
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HONG KONG
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JAPAN
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8-12-1 Nishishinjuku, Shinjuku-ku
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KOREA
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Won Chang Bldg, 3rd Floor 26-3
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Roseland, NJ 07068
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Paula Compton, Western Sales Manager
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Irvine, CA 92715
(714) 851-9422

Diane Philipbar, Sales Assistant
103 Eisenhower Parkway
Roseland, NJ 07068
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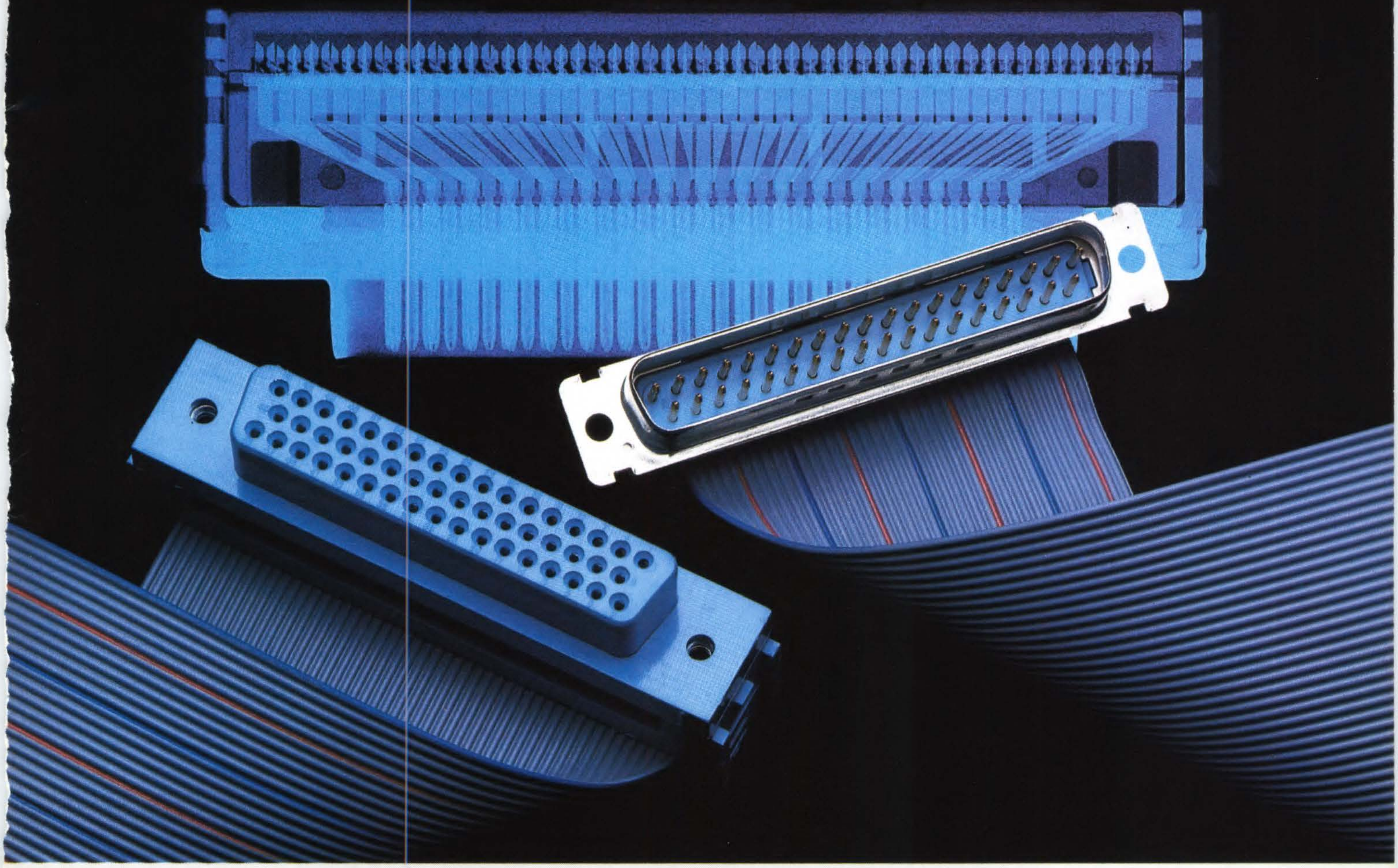

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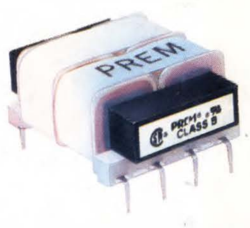

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