Designer's guide to fine-tuning $\mu P/\mu C$ code

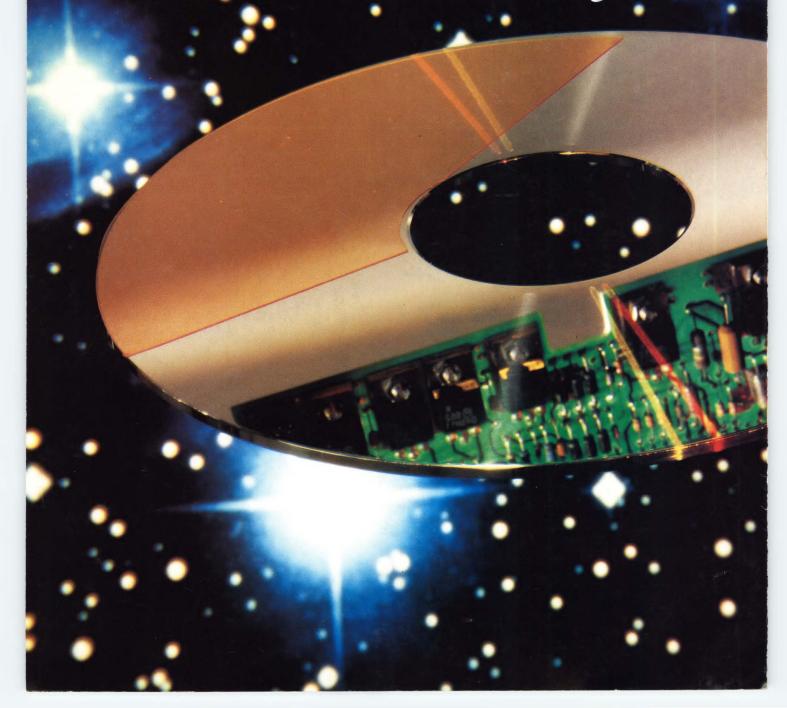
Flash A/D converters push performance limits

Thermal mass-flow transducers

Uninterruptible power supplies protect computer equipment

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Improved performance propels Winchester disk drives to new heights



e into it.

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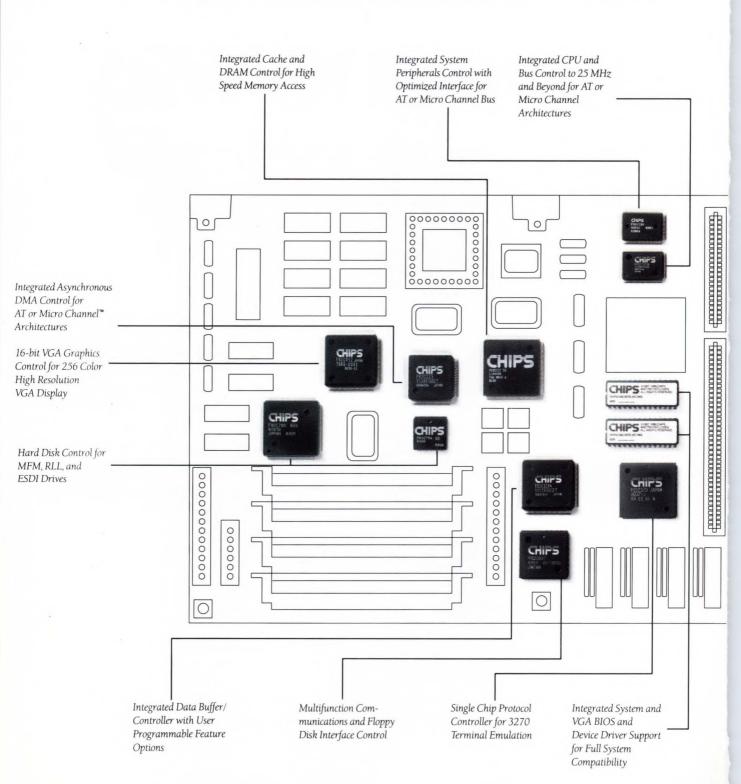
So if you want to get more out of your systems, call 800-323-4477 and put more into your design where it really counts.

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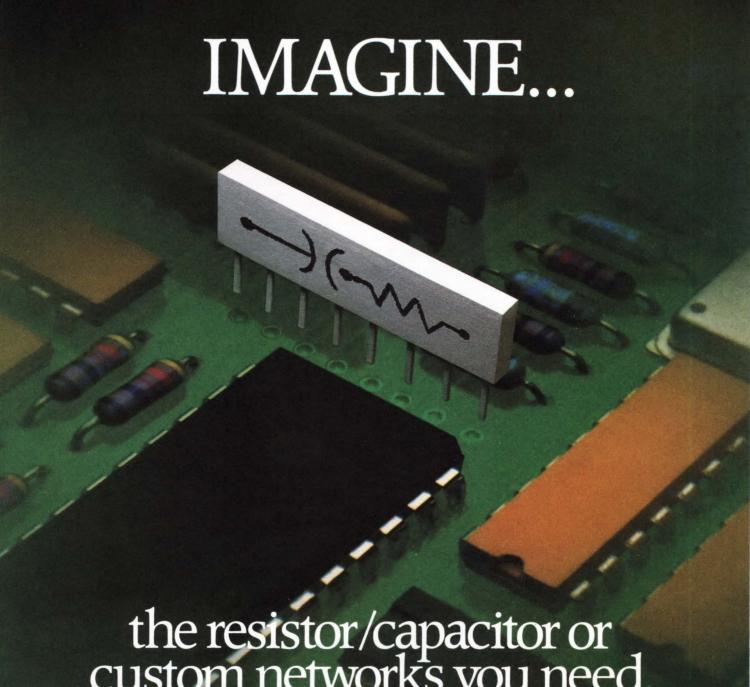


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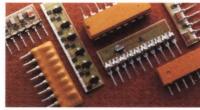
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Dale Makes Your Basics Better

CIRCLE NO. 3

Seagate's 3.5" drives Now with AT interface

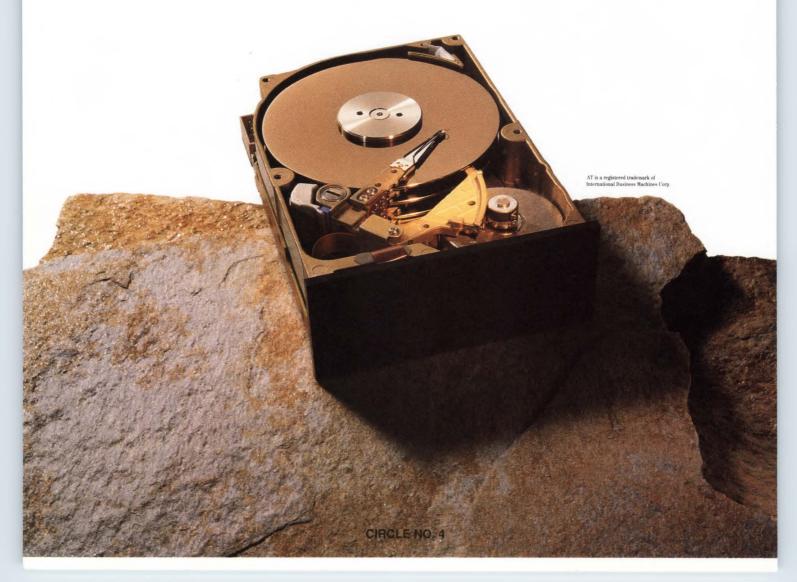
Seagate's field proven ST157 product line now features embedded controllers with an AT® interface. These reliable to-the-bus solutions offer improved cost/performance over non-integrated solutions.

The ST125A, ST138A and ST157A provide 21, 32 and 43 megabytes of formatted capacity respectively, and feature 28 or 40 msec typical access times, with an impressive 50,000 hour MTBF. All

models support the standard 16-bit AT task file interface, 1:1 interleave capability, and an internal data rate of 7.5 megabits/second.

For more information on the drives that offer a lower cost of connection and higher system performance for OEMs and systems integrators, call your nearest Seagate sales office, or call Seagate directly at 800-468-DISC or 408-438-6550.







SPECIFICATIONS

SPECIFICATIONS				
		/-230DR /-230DR		/-425DR -425DR
Freq. Range(MHz)	10-300	00	10-250	00
Insert. Loss (dB) 10-100MHz 100-1500MHz 1500-3000MHz	typ. 1.3 1.1 1.8	max. 1.7 1.7 2.5	typ. 1.3 1.1 1.8	max. 1.7 1.7 2.5
Isolation(dB) 10-100MHz 100-1500MHz 1500-3000MHz	typ. 60 40 35	min. 40 30 22	typ. 60 40 35	min. 40 30 22
1dB Compression(dBm) 10-100MHz 100-1500MHz 1500-3000MHz	typ. 17 27 30	min. 6 19 28	typ. 17 27 30	min. 6 19 28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
Switching Time (µsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
Oper. Temp.(°C)	-55 to	+100	-55 to	+100
Stor. Temp.(°C)	-55 to	+100	-55 to	+100
Price (10-24) (1-9)	\$39.95 \$89.95		\$59.95 \$109.9	

Now, high-speed, high-isolation switches with with built-in drivers, tough enough to pass stringent MIL-STD-202 tests. There's no longer any need to hassle with the complexities of designing a TTL driver interface and then adding yet another component to your subsystem...it's already included in a rugged, low-cost, compact assembly. Available in the popular hermetically-sealed

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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: Factors such as cost, reliability, and performance will guide you to a choice among the myriad new, higher-performance Winchester disk drives. See the Special Report, which begins on pg 122. (Photo courtesy Imprimis Technology Inc)

SPECIAL REPORT

Winchester disk drives

122

As always, 3½- and 5¼-in. Winchester manufacturers offer new drives with specs even more impressive than last year's models. These new drives feature decreased latency and faster data-transfer rates, and some manufacturers offer drives reduced in size, weight, and power.

—Maury Wright, Regional Editor

DESIGN FEATURES

External compensation boosts op-amp performance

143

Although op amps typically include internal compensation, the resulting performance isn't always satisfactory. You can significantly enhance a circuit's performance by using op amps that also accommodate external compensation.—Charles Kitchin and Scott Wurcer, Analog Devices Inc

Chirp-Z transform efficiently computes frequency spectra

161

The chirp-Z-transform (CZT) algorithm, which is used to transform information between time and frequency domains, is both efficient and fast, and it lets you select any convenient size for your data sequences.

—Timothy D Lyons, Teradyne Inc

Designer's guide to fine-tuning $\mu P/\mu C$ code—Part 1

177

If you want your program to handle real-time interrupts, it will have to run fast; if you want to cram it into a PROM, you'll have to minimize the code size. You can't optimize your code for both conditions at the same time, however. This article, part 1 of a 2-part series, presents coding techniques that will increase your code's execution speed. Part 2 will offer methods for decreasing code size.—Peter S Gilmour, Motorola Inc

TECHNOLOGY UPDATES

Thermal mass-flow transducers: Sensors offer fast response times

55

Recent improvements have allowed the latest thermal mass-flow transducers to provide response times in the millisecond range.

—John Gallant, Associate Editor

Continued on page 7

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THE WESTCOR STAKPAKTM. NEW **GENERATION 250 TO 1200 WATT** SINGLE OR MULTIPLE OUTPUT OFF-LINE SWITCHER. 3.2 X 5.5 X 11.4 INCH CASE. FAN-COOLED.

Stack the odds in your favor by designing-in Westcor's 6 watt/cubic inch high power megahertz switcher. Capitalizing on patented and proven megahertz module technology and innovative thermal management techniques, the StakPak provides up to 1200 watts of power at 50°C with 1 to 8 isolated and fully regulated outputs.

For existing designs the StakPak's small size and low profile allow system enhancement without mechanical redesign. Simply replace your open frame switcher with up to 1200 watts of StakPak power or replace your "box switcher" with 2 StakPaks and realize up to twice the power without losing additional space. StakPak power factor correction provides 850 watts of output power from a standard 115 VAC wall outlet. In new designs, more space can be devoted to functionality or the system can be downsized.

The StakPak's 8 module output section can be factory configured in virtually an infinite number of voltage, current and power combinations. Special models providing between 250 to 1200 watts and outputs from 2 to 95 VDC are available.

Other features include outstanding electrical performance; UL, CSA, VDE safety agency approval (in process); variable speed fan option for low ambient noise enviroments and 3 phase or DC input options. Indeed, with unprecedented power density, versatility and new features, the StakPak redefines power packaging. Please contact Westcor for a data sheet, pricing and additional information.



STANDARD 1200 WATT STAKPAK MODELS (110/220 VAC input)

Output Voltage (VDC) and Maximum Current (amperes) per Channel

Single Outp	ut			
SP1-1801	2@240			
SP1-1802	5 @ 240	T .		T
SP1-1803	12@100			may not exceed
SP1-1804	15 @ 80		watts for any ultiple output.	
SP1-1805	24@50		uitipie output. Pak models are	
SP1-1806	28 @ 42		se contact the	
SP1-1807	48 @ 25	Tica	se contact the i	actory.
Dual Outpu	t			
SP2-1801	2@120	5@120		
SP2-1802	5@120	5@120		
SP2-1803	5@120	12@66		
SP2-1804	12@66	12 @ 66		
SP2-1805	15 @ 53	15 @ 53		
Triple Outp	ut			
SP3-1801	5 @ 180	12@16	12@16	
SP3-1802	5 @ 150	12@33	12@16	
SP3-1803	5@180	15@13	15 @ 13	
SP3-1804	5 @ 150	15 @ 26	15 @ 13	
Ound Outpu				

SP4-1801

SP4-1802 SP4-1803

SP4-1804

Five Output





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73

93



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Uninterruptible power supplies: Units help PCs through rough spots

By protecting your computer equipment from line-supply disturbances, uninterruptible power supplies can repay their capital cost the first time they prevent the loss of valuable data.—Peter Harold, European Editor

Flash ADCs push speed and bandwidth limits

The newest high-speed flash A/D converters feature sampling rates from 100M to 500M samples/sec with high input bandwidths.

—Anne Watson Swager, Associate Editor

PRODUCT UPDATES

A/D converter	109
CMOS A/D converter	112
Electronic log and sensor	114
Source/measurement units	116
CAE software tool	118

DESIGN IDEAS

197-204

Photoconductor closes AGC loop; Digital pot simulates strain gauge; Circuit transforms PC into data analyzer; Feedback and amplification.

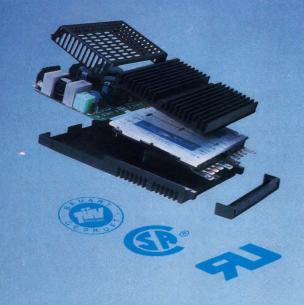
NEW PRODUCTS

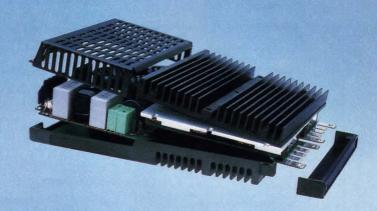
Components & Power Supplies											213
Integrated Circuits											227
Computers & Peripherals											236
CAE & Software Development	To	00	ls								250
Test & Measurement Instrume											

DEPARTMENTS

News Breaks	10
News Breaks International	. 22
Signals & Noise	. 33
Calendar	. 42
Editorial	47
Literature	280
Career Opportunities	286
Business/Corporate Staff	290
Advertisers Index	291
Looking Ahead	295

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Celebrating The New Profile

Introducing the FlatPAC[™]... Vicor's Family of User Definable, Multiple Output, Switching Power Supplies

Until now, your power system decision meant choosing between costly and unpredictable custom development, or bulky and inflexible catalog supplies...or you had to design and manufacture it yourself. Taking the next step in the power-component revolution, Vicor introduces FlatPAC, the user-definable, "off-the-shelf" alternative to customs that's economical from single units to OEM quantities...and which fits in a fraction of the space required by conventional off-line supplies!

The Off-The-Shelf Alternative

FlatPAC's unique modular design allows Vicor to provide next day delivery on over 10,000 different FlatPAC configurations. You define your power requirements...

Vicor does the rest —

while eliminating the nonrecurring costs, unpredictable lead times, risk, inflexibility, and reliability uncertainties associated with conventional solutions. No other power product offers FlatPAC's combination of power density, economy, and "off-the-shelf" flexibility!

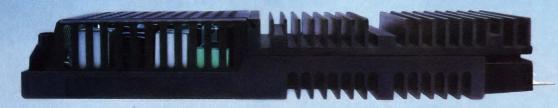
Power Cells

Sharing a distinctive, space saving flat package profile (1.37" high x 8.6" long), FlatPACs come in widths of 2.5", 4.9", and 7.4", and supply up to 200, 400, and 600 Watts of total output power...an unprecedented 7 Watts per cubic inch in an off-line switching power supply!

The three different packages provide one, two, or three user definable "Power Cells". Each Power Cell may be specified to be an independent, isolated output with a power rating of 50, 75, 100, 150, or 200 Watts, or cells may be combined to form higher power outputs...up to 600 Watts from a single output. Standard output voltages are 5, 12, 15, 24, and 48 Volts — and because all

FlatPAC outputs are field trimmable down to zero and up to 110% of nominal, a standard output can likely

FLATPAC



In Off-Line Switchers.

take care of even your most unusual voltage requirements. For special requirements, outputs as low as 2 Volts, and as high as 95 Volts can be provided.

And you don't give up features to get FlatPAC's advantages: besides being trimmable, all FlatPAC outputs have remote sensing and overvoltage and overcurrent protection. Individual FlatPAC outputs are totally isolated: there are no cross regulation issues; any output can be positive or negative; and output returns can float up to 500V, rms, apart. FlatPAC's run on either 110 or 220 Volt lines, meet "Class A" interference specs, have built in fusing, and conform to UL, CSA, and TUV safety agency requirements. Two and three cell units also provide two isolated, sequenced, logic outputs to indicate pending loss-of-output for system housekeeping during power cycling or brownouts.

The key to FlatPAC's flexibility and power density is Vicor's VI-200 family of high density, high efficiency, UL, CSA, and TUV recognized, component level DC-DC converters. When you specify a FlatPAC, you benefit from the field reliability and predictability that's been established in an installed base approaching half a million units.

Join The Celebration Now

Call Vicor now to discuss your special needs...you'll be celebrating when you find how quickly Vicor can ship you the smallest, most efficient, most cost effective solution to your power system requirements...at prices as low as 85¢/Watt in OEM quantities.

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Component Solutions For Your Power System

COK...SO THE TRAN BUT WHAT ABOUT R

They're everywhere. Worldwide over a thousand Transputer designs are in today's marketplace or are entering production. Some belong to Fortune 500 companies committed to using Transputers to build their next-generation products.

Although Transputer applications are diverse, the theme for each is the same – combining the power of individual Transputers with the unique architectural benefits of parallelism to achieve results that cannot be obtained as economically any other way.

Data Compression

Transputers are being used in the Generic Checkout System at the NASA Kennedy Space Center.



They are embedded within VME based front-end Data Acquisition Modules to provide data filtering for the system.

These modules pre-process data for a network of Unix based workstations that provide real-time control and monitoring of ground and flight equipment, like that used by the Space Shuttle. Only Transputers offered the degree of parallelism needed for this application.



Medical Imaging

University College London is using the parallel processing power of Transputers to convert CAT, NMR and laser scans into rotating 3-D images. These facial, skeletal, and soft-tissue images provide accurate computerized measurements to assist doctors with each step of an operation, and are also used by plastic surgeons to 'rehearse' operations for reconstruction.

Data Collection

British Steel is implementing an intelligent system that is designed to dramatically cut its multimillion dollar annual energy costs. It is built around T800 floating point microprocessors which process information from a highly complex data gathering system. These Transputers operate in parallel, condensing enormous amounts of data into information which helps energy management decide how to respond to a plant's changing demands for different fuels.



Data Transmission

Kokusai Denshin
Denwa (KDD), the
Japanese international
telecommunications
company, has developed an imageprocessing video
telephone using
Transputers to manipulate and condense
images for transmission
over telephone links.

This image communications system uses 32 Transputers operating in parallel

for ultrafast image processing. It can be connected to PC's to transmit images over telephone lines, function as a video phone, or be programmed to match the specifications of other receiving equipment, such as

facsimile machines and TV monitors.

Space

The European Space Agency is using Transputers to build a light-weight, radiation-tolerant, on-board computer for spacecraft. Programs which utilize Transputers in scientific computing and spacecraft control applications are also being developed in the U.S.

Transputers are manufactured on epitaxial silicon and have been shown to withstand aggressive tactical radiation levels

SPUTER'S TERRIFIC, 1995 EAL APPLICATIONS?

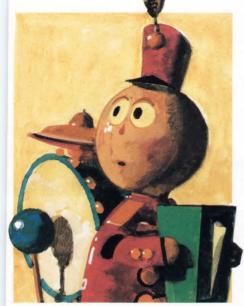
Flight Simulation

British Aerospace have used
Transputers to develop a low-cost
flight simulator comprising a flat
world, groundgrid, buildings,
trees and mountains –
with an optional Headup display. Future enhancements
will include the addition of undulating
terrain and a single or triple window
display option.

American companies are also using Transputers to build high-performance flight simulators more cheaply. One U.S. manufacturer utilizes over one thousand T800 processors per system.

3-D Rendering

Pixar in the US has developed a
Transputer-based rendering system which
quickly renders photorealistic images from
3-D models. The system consists of
Transputer boards for VME and AT-bus
systems optimized to run
Pixar's
sophisticated rendering
software.



The system holds great promise for such applications as architecture, automobile styling, package design, simulation as well as animation. Pixar's recent computer generated film 'Tin Toy' could not have been done without using this Transputer-based accelerator.



As the number of Transputers in a system design are increased, a proportional increase in performance can be achieved.

In West Germany, Parsytec GmbH is using this principle in their Megaframe Superclusters. Superclusters represent a complete series of reconfigurable industrial control boards as used in the automotive industry, which exploit the Transputer's parallel processing capability.



The basic Model 64, built with T800's, has a performance of 640 MIPS and 96 MFLOPS. The Model 256 comprises four Model 64 cabinets connected by cables and provides 2,560 MIPS and 384 MFLOPS.

Parsytec believes there is no limit to the size Superclusters can grow to. Two Model 256s can be combined easily to realize twice the raw performance of one system.



Robotics

Transputers are ideally suited for robotics applications because their special on-chip links make communication between control centers naturally easy. They are often used in the central control area for dumb robots, in multi-jointed robots, and in machine vision systems.

At the Houston Space Center, NASA and Lockheed are using Transputers in the development of an intelligent, self-manoeuvering, voice-controlled robot named EVA Retriever. EVAR is being built to investigate the autonomous retrieval of objects and astronauts that become detached from the Space Station.



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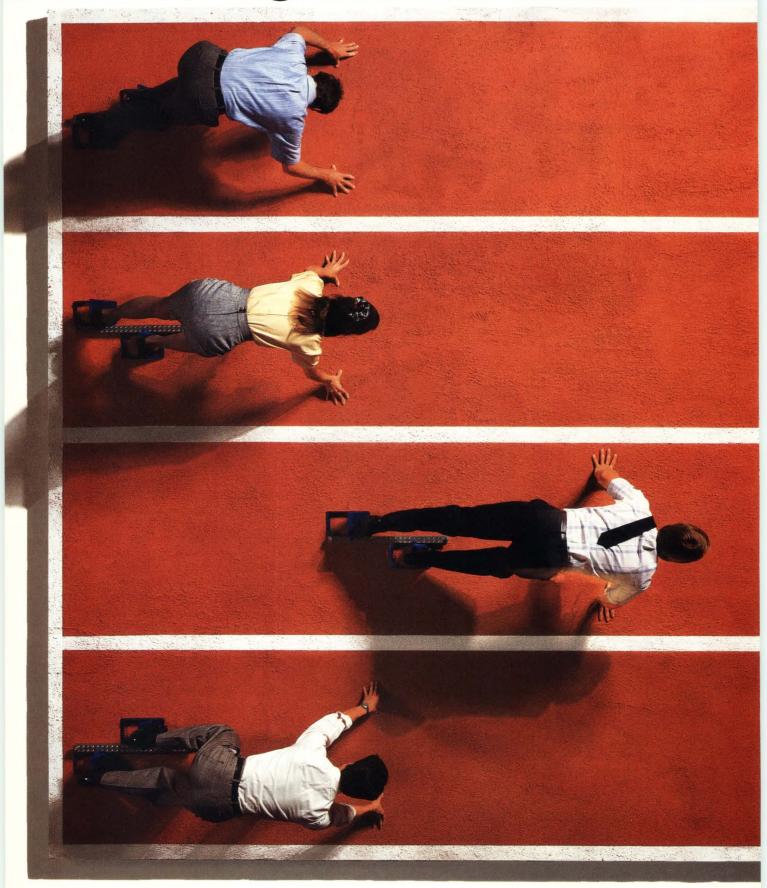
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CIRCLE NO 9

11

Finishing first has a lot to



do with where you start.



If there are head starts to be had, they ought to be yours.

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Our CMOS Programmable Gate Arrays can translate into a six month lead if you were planning on designing a gate array the conventional way.

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13

Be Brilliant At In Productio



7:05 am : Breakfast

Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design

You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.



11:00 am : Place & Route

You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch

Remember lunch? Normal people actually stop working and have a nice meal — right in the middle of the day! With Actel's logic solution, this could become a habit.

ACTEL FIELD PROGRAMMABLE GATE ARRAYS

They're a feast for your imagination.

Actel's ACT™1 arrays bring you a com-

pletely new approach to logic integration. Not just another brand of EPLD, PAL, or LCA™chips. But true, high density, desktop configurable, channeled gate arrays.

They're the core of Actel's comprehensive design and production system for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic, OrCAD™ and Mentor. OrCAD™

And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic

Breakfast And n By Dinner.



1:15 pm: Program You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete,
real-time performance check,
with built-in test circuits that
provide 100% observability of
all on-chip functions. Without
generating any test vectors.



4:00 pm: Production
Your pride and joy is
designed, created, tested, and
off to the boys in Production.
And you're finished way ahead
of schedule! Better think of
something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal
people actually go home and
eat with their families. On your
way, start thinking about how
Actel's logic solution can help
you be brilliant tomorrow.

placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most tedious part of the job by hand. And design verification is quick and easy, with on-chip Actionprobes™ that work with

your logic analyzer to provide 100% observability

of internal logic signals. Guaranteed.

All this is made possible by Actel's invention of the revolutionary PLICE™ antifuse programming element. Developed specifically for logic integration, PLICE antifuses and Actel's gate array architecture let you pack more functionality into much smaller spaces. No more splitting



equations across multiple PLDs. Or being short on flip flops. Or running out of connections halfway through routing.

> Every Actel part is fully tested at the factory, and each antifuse is verified during programming. So you don't have to give up testability for convenience.

You can be brilliant right now with 1200- and 2000-gate devices, and

6000-gate parts are on the way.

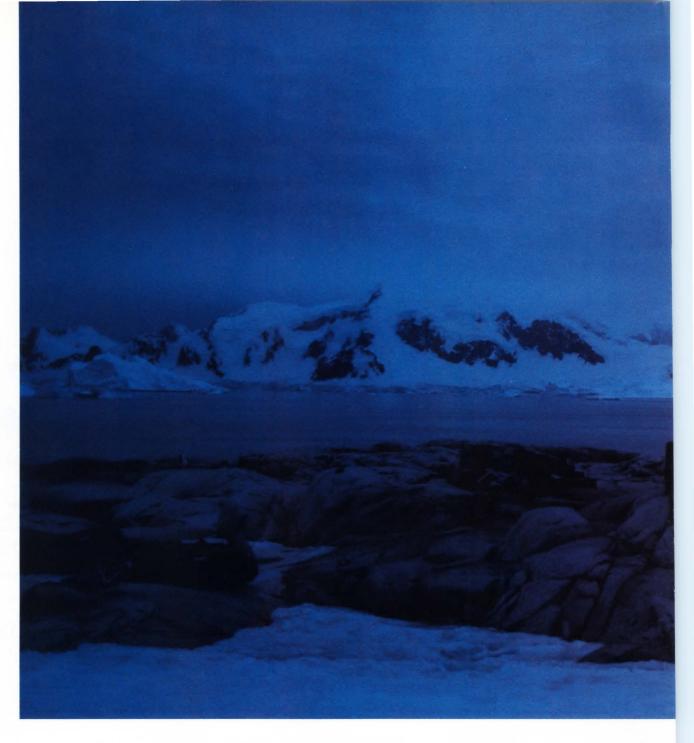
Call 1-800-227-1817, ext. 60 today for a free demo disk and full details about the whole Actel logic solution.

It could make your whole day.

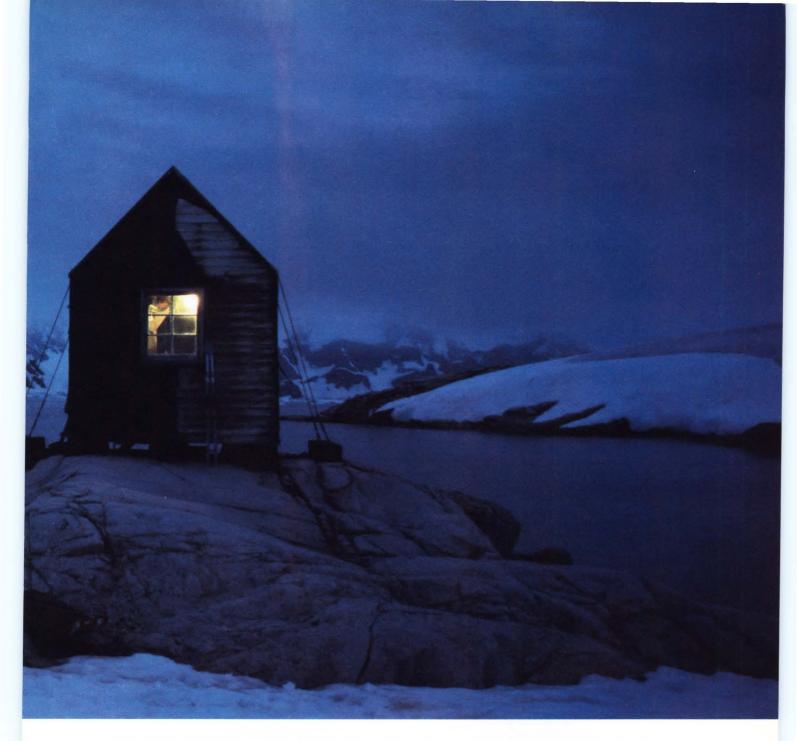


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EDN May 25, 1989



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NEWS BREAKS

EDITED BY JOANNE DE OLIVEIRA

LOW-POWER ECL PROCESS ACHIEVES 80 mW/GATE

AT&T Microelectronics (Berkeley Heights, NJ, (800) 372-2447) announced at ISSCC its BEST-I (bipolar enhanced self-aligned technology) process. The process allows for the fabrication of gates with speed/power combinations ranging from 80 psec at 2 mW/gate to 200 psec at 0.75 mW/gate. The transistors' toggle frequency is 3 GHz, and their gain is 100. The process will be offered to customers in the form of gate arrays having as many as 20,000 gates; more than 200 cells are available in the BEST-I library. The company will begin to accept designs in July; delivery is nine weeks. NRE costs range from \$45,000 to \$100,000.—Richard A Quinnell

LOW-COST SOURCE-MEASUREMENT UNIT SPEEDS TEST RESULTS

You can now source and measure voltage or current simultaneously by using Keithley Instruments' (Cleveland, OH, (216) 248-0400) Model 236 or 237 Source-Measurement Unit (SMU). These units combine four instruments—a digital multimeter, electrometer, voltage source, and current source—in one. The \$4900 Model 236 SMU can source as much as 110V, and the \$6200 Model 237 can source 1100V. Other specs include a 500μ-sec settling time, 1000 source/measurements per sec, current measurement to 10 fA, and an internal memory that can retain 1000 measurements. Both units let you program a delay from 0 to 65,000 msec, and a pushbutton lets you suppress background signals or make relative measurements with respect to a baseline signal. The SMUs measure voltage and current linearly and logarithmically; they also let you create a custom waveform.—J D Mosley

PERFORM ARCHITECTURAL DESIGN AT YOUR WORKSTATION

SES/workbench from Scientific and Engineering Software (Austin, TX, (512) 474-4526) is a graphical-design software system that allows you to create your system designs from the top down. You work with a graphical user interface that lets you construct models of your system by using icons to specify components at multiple levels of design. After capturing the design, you can use SES/workbench to translate your specifications into a declarative, object-oriented simulation language that is a superset of ANSI C and C++. You can simulate the system design with the company's PAWS/GPSM simulator. On the basis of the simulation results, you can evaluate alternative architectural solutions to your design dilemmas at the system level before making lower-level design decisions.

After you've justified an architectural design, you can iteratively refine your choice at lower design levels. Additionally, you can jump to any point in the design hierarchy, compile the system design, and perform a simulation to verify the accuracy of your architecture. SES/workbench features program-library management capabilities, an on-line reference manual, and hypertext-based help features. You can run the software on Sun, DEC, and Apollo workstations; DEC minicomputers; and Cray supercomputers. Prices start at \$26,000.—Michael C Markowitz

SYSTEM LETS YOU DESIGN MIXED ANALOG-DIGITAL ASICS

The ChipCrafter Mixed ASIC Expert option (ChipCrafter/MAX) from Seattle Silicon (Bellevue, WA, (206) 828-4422) provides a complete software package for designing mixed analog-digital ASICs. The package includes foundry-specific libraries of common analog functions, which the company offers for the same 1.25- to 1.5-µm CMOS

EDN May 25, 1989

NEWS BREAKS

manufacturing processes that the digital ChipCrafter design system supports. The analog functions consist of both basic analog standard cells and user-configurable components. The set includes op amps, comparators, a voltage reference, switches, resistors, capacitors, and FETs.

The software package's automatic-place and -route capability isolates analog circuitry from digital sections of the chip, dividing the analog functions into one or more blocks. The software automatically identifies and separates high- and low-sensitivity analog nets, and digital nets. The software provides links to the digital-simulation tools of Mentor Graphics and Valid Logic Systems. Spice net lists that include delay information are available for analog simulation. ChipCrafter/MAX costs \$29,000 and requires ChipCrafter digital-design software, which starts at \$49,000.—Doug Conner

VMEDUS BOARD INCLUDES ADC, DAC, AND PARALLEL I/O

The MD-DAADIO VMEbus board from Matrix Corp (Raleigh, NC, (919) 833-2000) includes both A/D- and D/A-conversion capabilities, and six 8-bit parallel-I/O ports. The 12-bit DAC module provides as many as eight channels of analog output. The DAC settles in 25 μ sec, and the converter has output-voltage swings as wide as $\pm 24 \text{V}$. Input to the ADC module can vary over the $\pm 10 \text{V}$ range. The 32-input ADC module operates at 125 kHz—8- μ sec conversions—and features 12-bit resolution. In the parallel-I/O section, you can configure the data direction of each of the six ports individually, and you can individually set input-enable and output 3-state conditions. You can configure the first port to interrupt the VMEbus on change of state or byte recognition, and you can mask each bit of the port individually. The board costs \$1495 and is available now.—Maury Wright

COMPANY SPECIFIES WRITE-TO-READ RECOVERY TIME

Filling what it believes is a longstanding specification gap, Micro Linear Corp (San Jose, CA, (408) 433-5200) specifies a write-to-read recovery time for its ML4041 read-data processor. The spec refers to the time the IC requires to switch from a write operation to a read operation—a recurring function that has an impact on hard-disk access time. The write-to-read recovery time includes both the switching time and the automatic-gain-control (AGC) acquisition time.—Michael C Markowitz

USER-PROGRAMMABLE ROMS NOW COME IN SMT PACKAGES

For those designs that require low power consumption and offer little board space for discrete components, Texas Instruments (Dallas, TX, (200) 232-3200 ext 700) now provides surface-mount versions of its one-time user-programmable ROMs. These CMOS PROMs offer reliability specs that compare favorably with those of more costly ceramic UV EPROMs. You can order a 128k-, 256k-, or 512k-bit version for \$5.20, \$5.45, or \$9.85 (1000), respectively.—J D Mosley

GATE-ARRAY FAMILY WELCOMES NEW MEMBERS

LSI Logic Corp (Milpitas, CA, (408) 433-8000) has expanded its LCA 100K gate-array family to include smaller gate-count devices. The additions range in size from 3788 to 100,636 gates and support designs with 64 to 278 I/O signals. NRE charges for the 0.7- μ m HCMOS array family begin at \$10,000; unit costs begin at \$5 in production volumes.—Richard A Quinnell



NEWS BREAKS: INTERNATIONAL

SEALED KEYBOARD SURVIVES EXTREME ENVIRONMENTS

Capable of withstanding immersion in 3 ft of water for 1 hour, altitude changes of 2000 ft/minute, rapid temperature cycling, and attack by most chemicals, the SF62091-KB1 fully sealed IBM PC-compatible computer keyboard is suitable for use in the harshest of industrial and military environments. It exceeds MIL-STD-810 requirements for resistance to shock and vibration. The 91-key keyboard, which is manufactured by Marconi Electronic Devices Ltd (Swindon, UK, FAX 0793-723348; in the US: Marconi Circuit Technology Corp, Hauppauge, NY, (516) 231-7710) employs 1-piece silicone-rubber keypads that provide 2 mm of key travel, tactile feedback, and a keypad lifetime in excess of 4 million operations. An integral pressureequalizing system relieves internal pressure changes that occur when the keyboard is subjected to extreme temperatures or altitude changes, and the aluminum casing provides RFI protection. By changing internal DIP-switch settings, you can configure the keyboard to generate IBM PC/XT or PC/AT codes, IBM PS/2 codes, or standard serial ASCII codes at RS-232C or RS-423 levels. The standard keyboard has an operating-temperature range of -25 to $+85^{\circ}$ C, but a full military-temperature-range version is also available. You can also obtain a rack-mounting version. The keyboard starts at around \$625.—Peter Harold

μP COMBINES THE ADVANTAGES OF RISC AND CISC

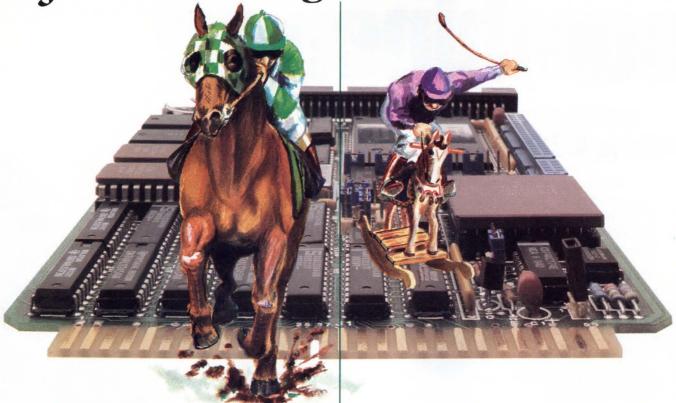
By combining the single-cycle instruction execution of RISC μ Ps with some of the complex instructions you'd expect to find in a CISC processor, the designers of the Hyperstone 32-bit μ P—Ingenieurbüro Otto Müller (Konstanz, West Germany, FAX 07531-51725)—claim to have produced a processor that runs at around 40,000 Dhrystones/sec. The μ P has a 128-byte on-chip instruction cache, and it uses only a 2-stage (decode/execute) instruction pipeline that eliminates wait states when it executes branch instructions. It can operate at full speed, using standard dynamic RAM with a page-mode cycle time of 40 nsec, and it has a linear address space of 4G bytes. The majority of its instructions are only 16 bits in length, which reduces the amount of program memory required and speeds instruction fetches. In addition, the μ P performs the range and pointer checks required by languages such as Pascal, Modula-2, and Ada without any speed penalties. The Hyperstone, which is expected to sell for around \$100 in medium volume, is currently manufactured in a 1.5- μ m CMOS process that allows it to execute 25M instructions/sec. Its core occupies only 40 mm² of silicon. A 1- μ m version of the part is under development.—Peter Harold

JAPANESE IC ASSEMBLER OFFERS SERVICES TO US COMPANIES

For the first time, Aoi Electronics Co (Takamatsu, Japan; in the US: San Jose, CA, (408) 922-0133) is making its IC-assembly services available to US IC designers and manufacturers. According to Shuichi Sato, managing director and general manager of the company's US and Canada sales office, this move represents "possibly the first time that any Japanese IC-assembly house in public has opened its services to companies outside Japan." Aoi Electronics offers highly automated, volume assembly of standard DIPs, SIPs, ZIPs, small-outline packages, and quad flatpacks. It can assemble almost any type of IC package in its class 100 clean-room environment. The company plans to offer surface-mount packages and plastic leaded chip carriers in the near future. Aoi also performs some functional, aging, and burn-in tests, and it offers environmental quality-assurance and open/short tests for assembled parts. The company offers a turnaround time of two weeks.—Joanne De Oliveira

STD Bus Software Challenge:

CµBIT's C-Engine vs STD-DOS



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- Efficient Embedded System Code

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Turbo C includes the compiler, assembler, editor, source level debugger, error checking with built-in Lint and a large library of functions with source code. Code runs faster and is more compact than code written with leading competitive C compilers. Thorough documentation gets you started fast.

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Real OEM's Don't Use DOS. You want to use DOS as a development tool, but when you complete your development, DOS sticks around. Since your application runs under DOS, you will need to ship DOS with every system. OEM's can save big money by ditching DOS.

DOS is great if your system needs to run Flight Simulator. But for embedded control system development, keep DOS on your PC where it belongs. Cubit's C-Engine lets you develop code using DOS and Turbo C on your PC, while keeping the final code fast, clean and without DOS clutter.

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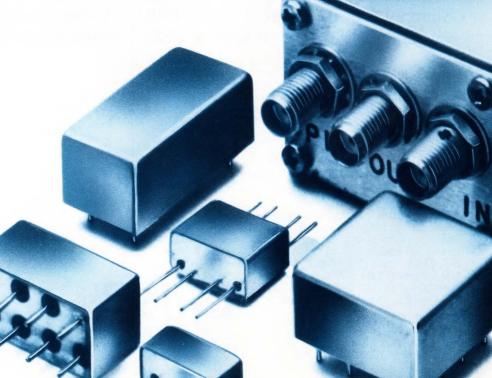
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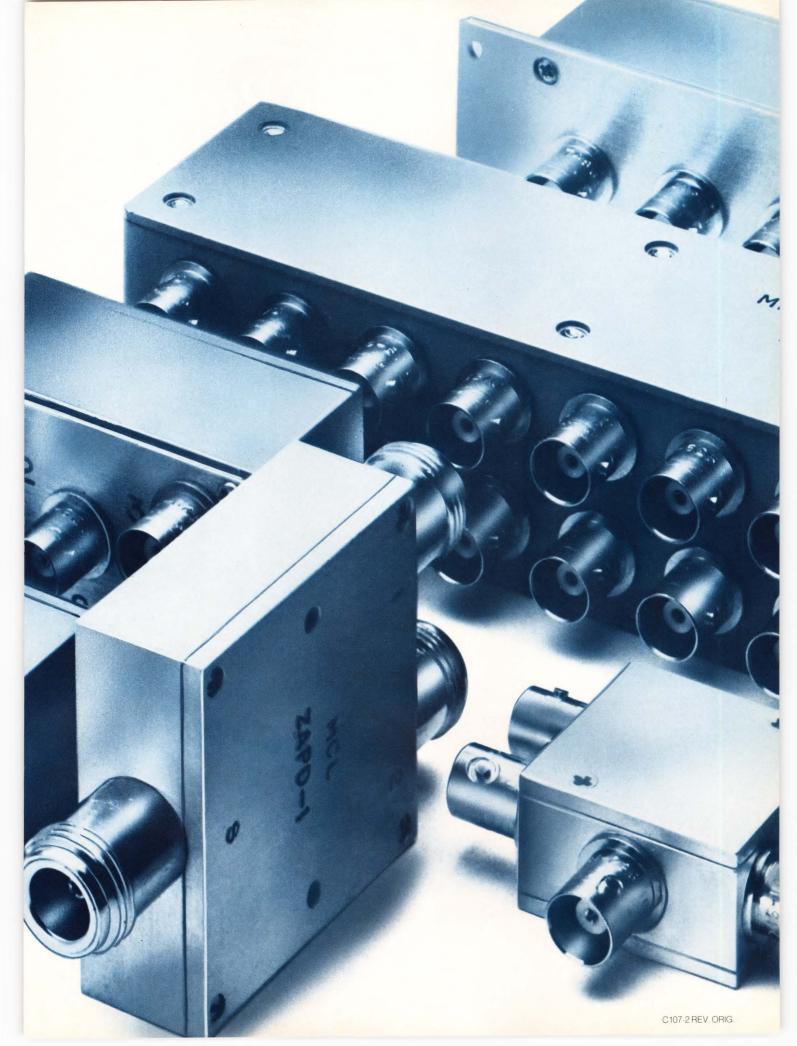
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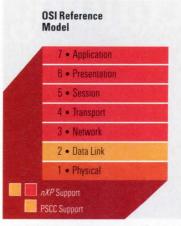
Integrated functions

The PSCC combines a full-duplex HDLC channel, on-board DMA controller, and 520 bytes of internal RAM. It allows you to send and receive messages directly from memory and frees system intelligence for higher level functions. It automatically supports the update and comparison of state variables for multiframe transmission. In addition, the PSCC supports collision and priority detection.

For even greater integration, the PSCC will be imbedded in Oki's high-performance 16-bit *nXP* microcontroller which will support all seven OSI levels of the ISDN.

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4250	Dual SCSI	Half Ht.	8 to 24 MBytes	N/A
5150	One SCSI	Full Ht.	8 to 80 MBytes	8 to 40 MBytes
5250	Dual SCSI	Full Ht.	8 to 72 MBytes	8 to 32 MBytes

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SIGNALS & NOISE

Sending alien EE grads home doesn't serve the US

Regarding Jon Titus's unbelievable editorial "Send alien graduates home" (EDN, October 27, 1988, pg 57): Our country will not be well served by such "employment protectionism"-not even when thinly disguised as superpower charity. Perhaps I will agree with Jon's sentiment on the day that the US is awash in a surplus of world-class native-born and -trained engineers and scientists. I'll bet that's a cold day in a hot place.

Kevin G Smith Palo Alto, CA

Foreign students came to US seeking freedom

In the editorial "Send alien graduates home." Jon Titus restates an old twist on Irwin Feerst's "send 'em back where they came from" theme: the idea that "their country needs them," therefore they should be forced to return. The assumptions that Jon makes are both naive and disturbing.

He assumes that a state, in essence, owns an individual, whose own political and economic desires are irrelevant.

He assumes that an individual should study what some society demands of him or her, rather than what the student is good at or is most interested in.

He assumes that an individual who is fully desirous of improving things back home has any chance of doing so in the face of corruption, bureaucracy, special interests, politics, and cultural attitudes.

He assumes that an individual would ever be allowed to emigrate to the US once his country realized his "worth."

The foreign-born engineers I know have come to America because it's the last bastion of freedom and opportunity, escaping not only poverty, but political repression and a military-industrial bureaucracy that assigns a place in the state machinery to every interchangeable citizen-part. These immigrants want the blessings of freedom, not only for themselves, but for their children.

Yes, they would also like to be able to return home, but to a home with the freedoms they had to come to America to find. Unless Jon is willing to add one more proviso to his "engineer repatriation" scheme—that the returning graduates also be provided with the tools needed to rebuild free societies back home—he is just putting a socialist gloss on Irwin Feerst's xenophobic rantings.

William D A Geary Design Engineer Wardenclyffe Microtechnology Deer Park, NY

Send out-of-state graduates home to the farm

Congratulations to Jon Titus on his October 27th editorial "Send alien graduates home." I suggest that the US mandate a law that would require all out-of-state engineering graduates to practice in their respective home states for two years before they are allowed to seek jobs in the states where they graduated. For example, a student from Maine, after completing a BSEE at Caltech, would have to go back to Maine for two years and apply his expertise in that state before he could seek any high-tech job in California. This way, we Californians won't lose any jobs to out-of-state foreigners. And farm states will benefit from the high-tech growth introduced there by the people who know those states best.

Knowing that they would be required to return to their home states for two years before emigrating to any high-tech state might push many young out-of-staters to study agricultural science instead of



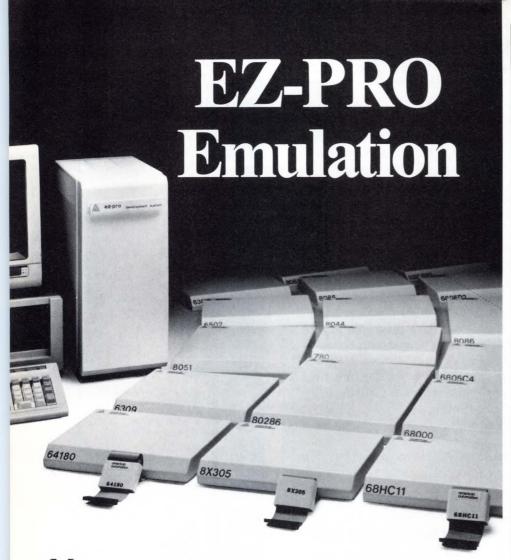
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CIRCLE NO 21

SIGNALS & NOISE

computer science, or to study electrical engineering. Why electrical engineering instead of another discipline? Well, with an electrical engineering degree, one thing they can do is to maintain and update television and radio stations in the farm states, while craving (but not participating in) the technical opportunities in high-tech states. Anyway, two years is not a long time.

It's not hard to tell an out-ofstater or a foreigner from a native Californian by judging physical appearance, the way he handles his car, or his participation in outdoor activities. Just as British, Australians, Indians, New Zealanders, Irish, Swedish, Taiwanese, New Yorkers, Southerners, and so forth, speak with accents, we native Californian engineers have our own accent. It would be best to develop a state testing system that could tell whether a person is an out-of-stater by the way he designs electronic circuits.

I hate to see our electrical engineering jobs here in California taken by out-of-state foreigners. I have seen some of them accepting wages that are much lower than those that electrical engineers here are being paid. Why don't Texas's electrical engineering graduates stay in Texas, or Utah's engineering graduates work in Utah, or graduates from New Jersey stay in New Jersey instead of getting California's jobs? Those states aren't poor. There are companies such as Compaq, Texas Instruments, and Motorola in Texas; National Semiconductor and Unisys in Utah; and General Instruments and AT&T in New Jersey. Why bother to travel all the way to California? I hope Jon Titus knows the answer and the reason why.

Mike Lynn Torrance, CA

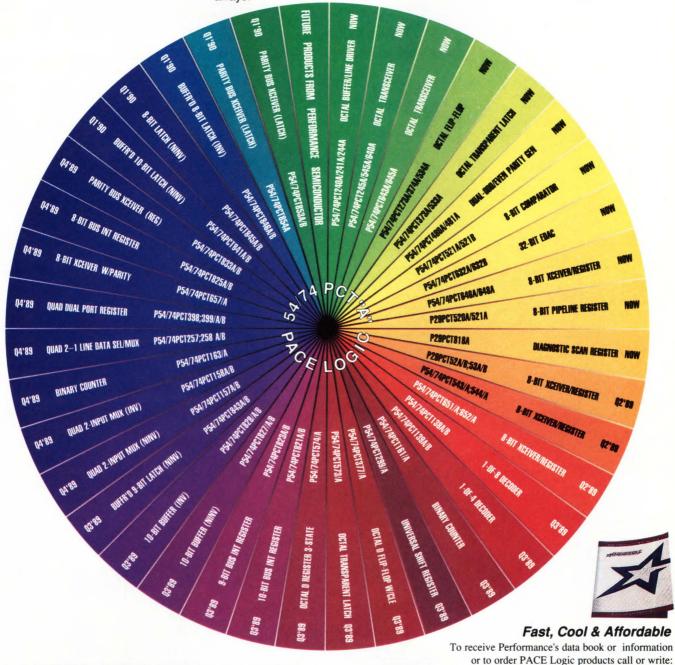
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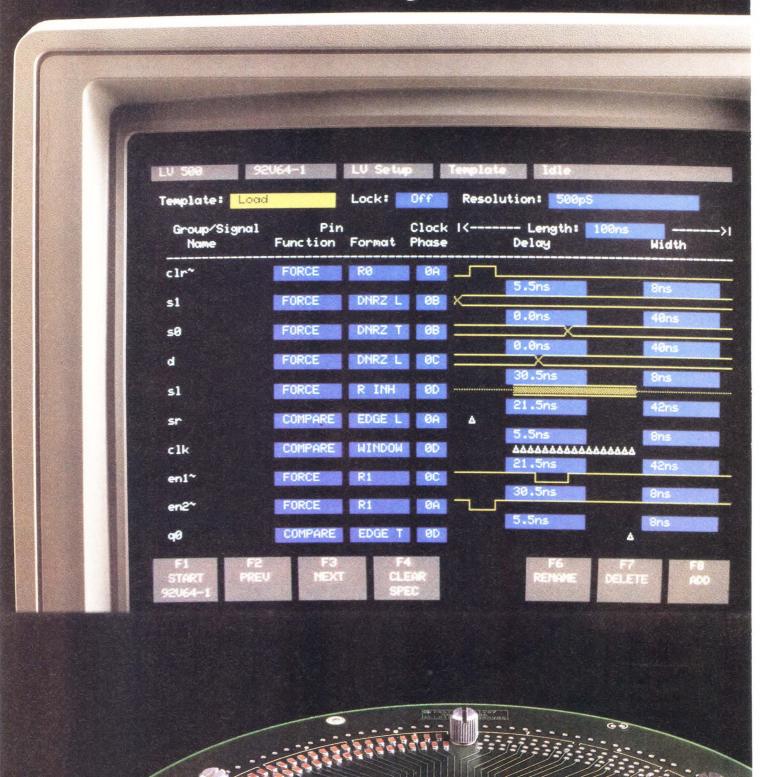
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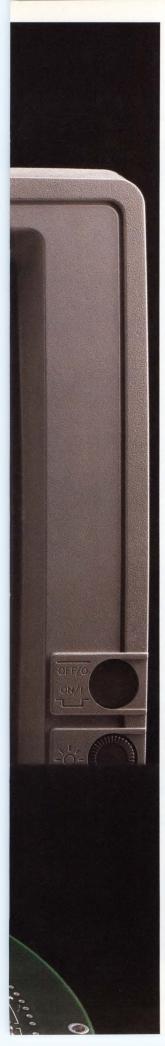
For commercial temperature applications, PACE LOGIC is available in DIP and SOIC. MIL-STD-883 Rev C Class B compliance is offered in ceramic DIP and LCC.



Tek's New ASIC Verification System.



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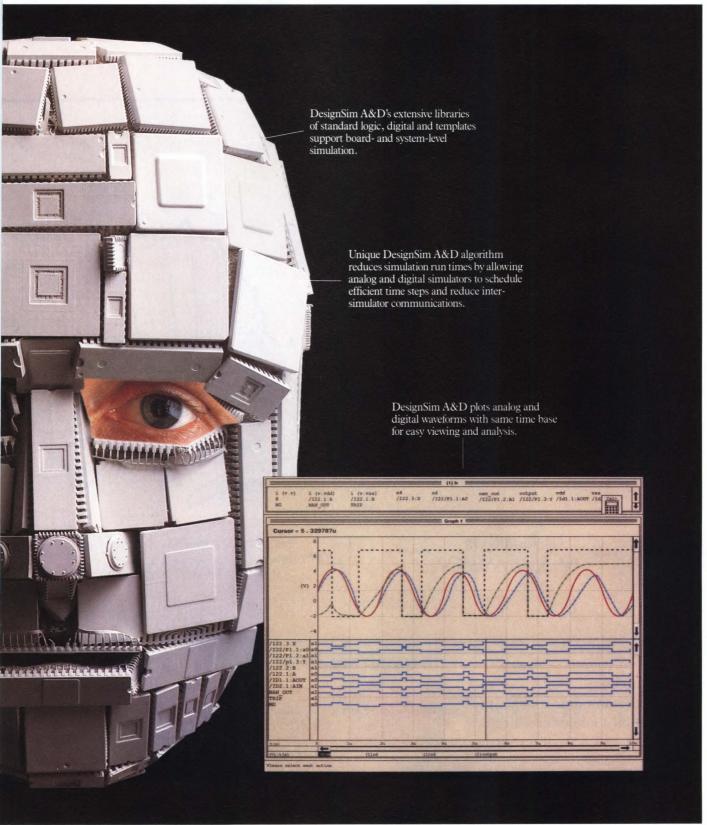
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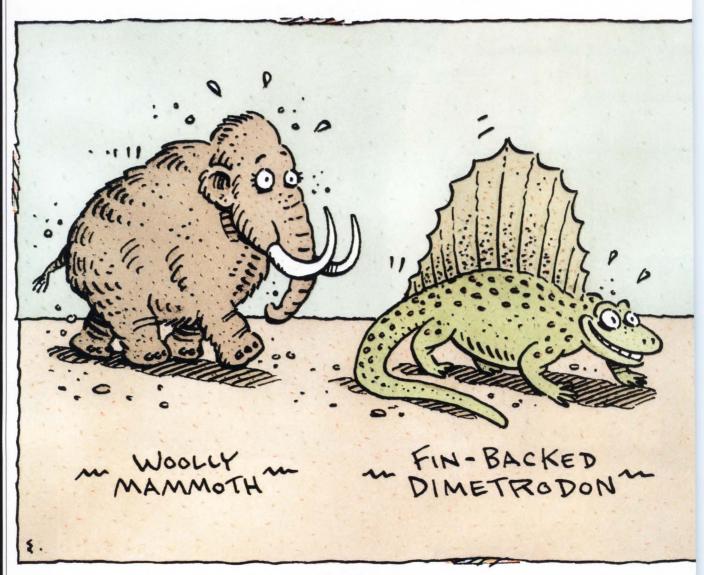
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		80 ns	32-pin PLCC

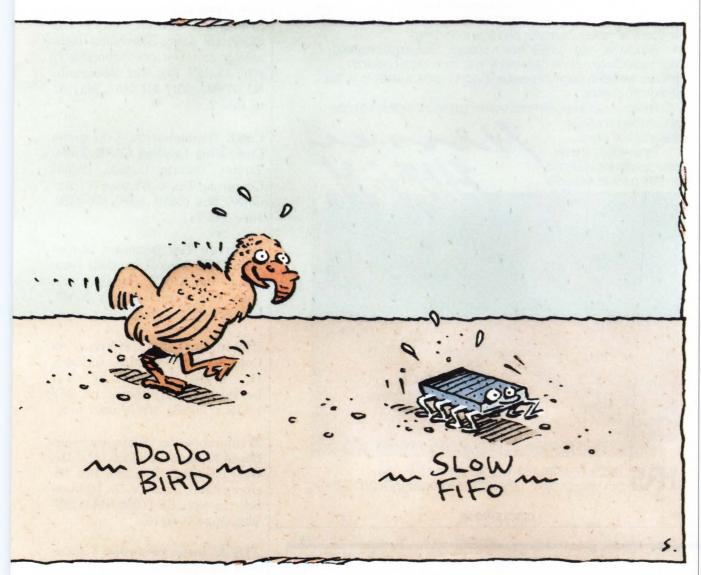
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CIRCLE NO 29

DID YOU KNOW?

Half of all EDN's articles are staff-written.

EDN

CALENDAR

Tape Automated Bonding (TAB) Workshop, Sunnyvale, CA. Dr Subash Khadpe, Semiconductor Technology Center, Box 38, Neffs, PA 18065. (215) 799-0919. May 25 to 26.

43rd Annual Frequency Control Symposium, Denver, CO. Dr R L Filler, US Army Electronics Technology and Devices Laboratory, attn: SLCET-EQ, Fort Monmouth, NJ 07703. (201) 544-2467. May 31 to June 2.

CASE Benchmarks: A Seminar Comparing Leading CASE Tools, Toronto, Ontario, Canada. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3880. June 5 to 7.

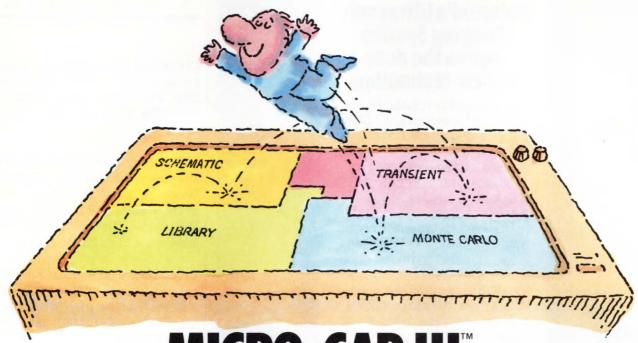
Design to Test (seminar), Minnetonka, MN. Logical Solutions Technology Inc, 310 W Hamilton Ave, Suite 101, Campbell, CA 95008. (408) 374-3650. June 6 to 7.

1989 International Conference on Consumer Electronics, Chicago, IL. Diane D Williams, 131 Ledgewood Dr, Rochester, NY 14615. (716) 865-2938. June 7 to 9.

Troubleshooting Microprocessor-Based Equipment and Digital Devices (seminar), Portland, OR. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (913) 898-4695. June 13 to 16.

ATE & Instrumentation Conference East, Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. June 19 to 22.

Introduction to X.25 (short course), College Park, MD. University of Maryland University College Center for Professional Development, University Blvd at Adelphi Rd, College Park, MD 20742. (301) 985-7122. June 20 to 22.



MICRO-CAP III. THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

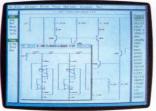
MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

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CALENDAR

COMPASS '89 Conference, Gaithersburg, MD. Nettie Quartana, 2100 Washington Blvd, Arlington, VA 22204. (703) 486-3500. June 20 to 22.

VHDL and Modeling in the DoD Procurement Process (seminar), Washington, DC. Paul Hunter, Program Chair, NRL, Code 5305, Washington, DC 20375. (202) 767-3264. June 21 to 23.

Fiber Optics in Local Communications (seminar), New York, NY. Raycom Systems Inc, 6395 Gunpark Dr, Boulder, CO 80301. (800) 288-1620. June 22.

26th Design Automation Conference, Las Vegas, NV. MP Associates, 26th Design Automation Conference, 7490 Clubhouse Rd, Suite #120, Boulder, CO 80301. (303) 530-4333. June 25 to 29.

Knowledge Engineering Today's Marketplace, The Annual Conference of the International Association of Knowledge Engineers, College Park, MD. Fred Whiting, IAKE Conference, Georgetown Box 25461, Washington, DC 20007. (301) 231-7826. June 26 to 28.

OS/2: A Comprehensive Hands-On Introduction (short course), Ottawa, Ontario, Canada. John Valenti, Integrated Computer Systems, 5800 Hannum Ave, Culver City, CA 90231. (800) 421-8166; in Canada, (800) 267-7014. June 27 to 30.

Quality Management Conference, Denver, CO. Pam Frye, Quality Management Conference, ACEC, 1015 Fifteenth St NW, Washington, DC 20005. (202) 347-7474. July 12 to 14.

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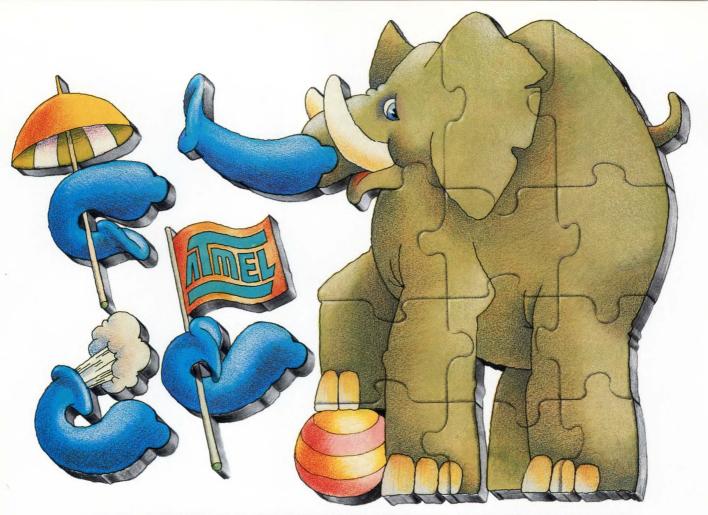
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The people who make the difference

EDITORIAL

Design for fixability



Most engineers would agree that they should design products so that their companies can manufacture and test them. After all, if you can't manufacture a product and then make sure it works, it's no good to your customers. But when it comes to designing products so that when something goes wrong, someone can fix them, we often do a poor job. Too many products are unfixable or at least very difficult to repair.

Here's an example. Over my electric range I have a microwave oven that includes two lamps. The lamps shine down to illuminate the range top. Last week when both lamps burned out, I thought that replacing them would be a fairly easy after-dinner job: Just remove the frosted-glass panel and pop in two new bulbs. I wasn't that lucky. It turned out that the microwave oven wasn't designed to be fixed. First, two air-filter screens had to come out—the oven includes a fan. Then, I had to extract five screws to remove the large metal plate that covers the entire bottom

The two bulbs were finally accessible, but they were hard to unscrew. In fact, turning the bulbs broke the glass globes free from their bases. As the bulbs twisted free, the bases stayed firmly in the sockets. Luckily, I was able to remove the socket mounts and detach the wires—they at least had quick-disconnect fittings. Even with the sockets in hand, the job was a nightmare. It turned out that the bulbs were glued into the socketsprobably to keep them from vibrating loose during shipment. All in all, replacing the bulbs took several hours.

This isn't an isolated example. I've also seen inaccessible trimmers, hidden DIP switches, soldered-in fuses, mislabeled test points, incorrect

schematic diagrams, and faulty diagnostic software.

However, the American electronics industry does have a shining example of a company that knows the value of fixability. Over the years, I've been very partial to the Heath Company, and I've built many Heathkits. I doubt that I've saved much money by building the kits rather than buying assembled units; but the kits were an enjoyable pastime, and the designs were buildable, testable, and fixable. Also, the documentation was clear, and I always got a schematic diagram for later reference. If a kit had to be fixed, the unit came apart easily, the part labels were where I could see them, and there was a flowchart of problems and solutions. Heath always identified the parts and suggested equivalent replacements.

I own a Heath/Zenith PC-compatible computer. Today as I started this editorial, I got a memory-parity error message instead of the usual MS-DOS prompt. If I were using almost any other PC, it would have been time to panic. However, the Zenith computer includes diagnostic routines that test internal operations. I chose the memory test and got a message that pointed to the defective memory chip. It took me about ten minutes to replace the defective chip and get the computer back together.

You may be thinking that kits are for hobbyists and hackers; but the Heathkits I've seen contain some remarkable circuitry, and their manuals can give you a quick course in designing repairable products. From what I've seen of most other manufacturers' electronic products, we have a lot to learn. Heath's manuals are about \$8 each. You can write to the company in Benton Harbor, MI 49022, or phone it at (616) 982-3200 to ask for a catalog. Reading a few manuals should put you on the road to designing fixable products.

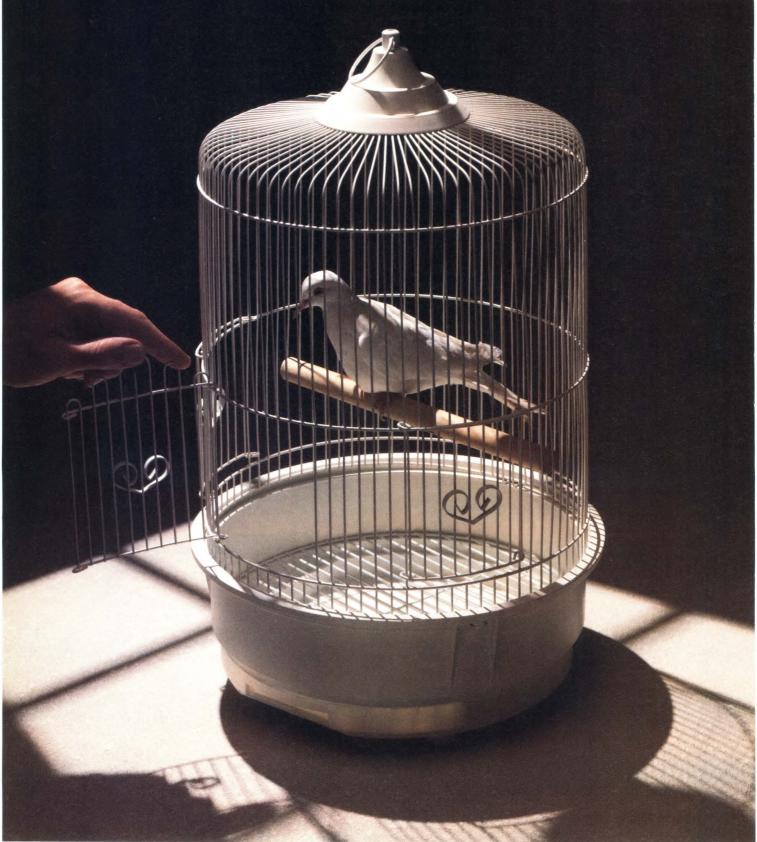


Jesse H Neal **Editorial Achievement Awards** 1987, 1981 (2), 1978 (2), 1977, 1976, 1975

American Society of **Business Press Editors Award** 1988, 1983, 1981

Jon Titus **Editor**





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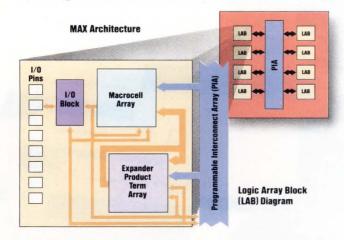
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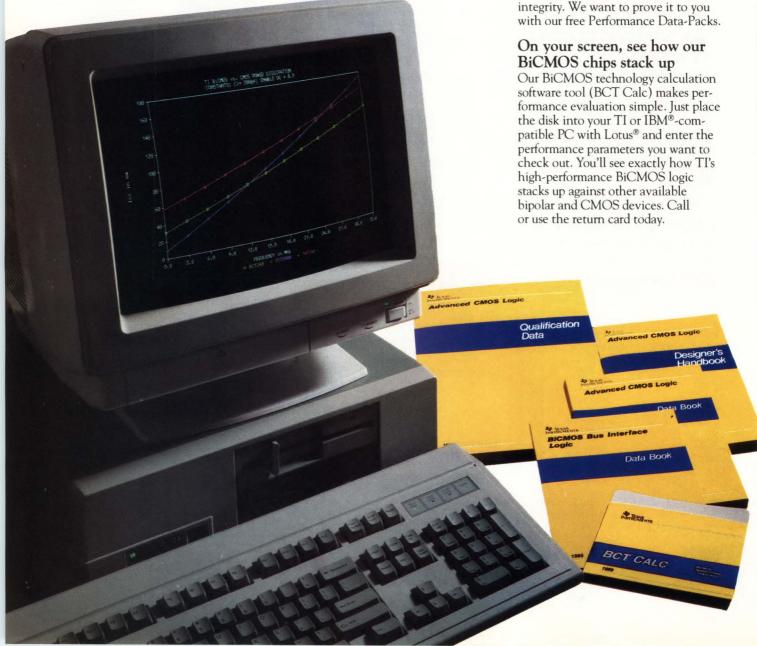
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Performance is comparable to advanced bipolar devices, supporting frequencies up to 125 MHz and providing the 24-mA output capable of driving 50-ohm transmission lines. It's a perfect match for core and local bus interface.

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A unique pinout arrangement creates a "flow-through" architecture. This simplifies board design and can save up to 32% in board space because you don't need passive components to control noise as you usually do with

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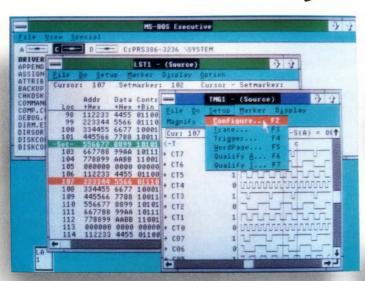
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CIRCLE NO 36 EDN May 25, 1989

THERMAL MASS-FLOW TRANSDUCERS

Sensors offer fast response times



Recent improvements have allowed the latest thermal mass-flow transducers to provide response times in the millisecond range.

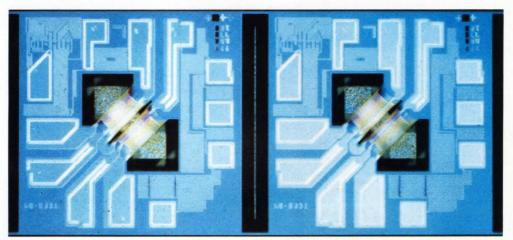
> John Gallant, Associate Editor

esigners of semiconductor process-control equipment or chemical process-control equipment will want to take a look at the latest thermal mass-flow transducers. Recent improvements have given the devices faster response times. These times are now on the order of hundreds of milliseconds: only 10 years ago, response times were around one minute. And there's a new development that may have wide-ranging effects: The fastest of these sensors, a semiconductor version, is currently under investigation by automotive manufacturers, who are trying to determine whether the device can withstand the automobile environment, so it can be used in electronically controlled carburetion systems.

Devices that measure and control the mass flow of substances are critical elements of many process-control applications in a number of industries. Chemical companies, for instance, must blend substances precisely in a thermodynamically controlled manner in order to achieve accurate and repeatable chemical reactions. Semiconductor manufacturers must accurately control deposition and etching materials in order to create the geometries of today's VLSI devices. Makers of combustion engines must provide a way for the engines to control the mixture of gasoline and air entering them so they'll run smoothly. Various types of mass-flow sensors and controllers are available for these different applications, and the type you'll choose depends on the nature of the substance you want to measure. For accurately measuring the mass flow of a pure gaseous substance, the technology of choice is the thermal mass-flow sensor.

Transducers count calories

One type of thermal mass-flow sensor is the calorimetric mass-flow sensor, which uses heated sensing elements that are isolated from the flowing gas. The



The microbridge airflow sensor from Micro Switch consists of a thermally isolated bridge comprising two detector elements and a heater element. The bridge is suspended over an anisotropically etched silicon chip.

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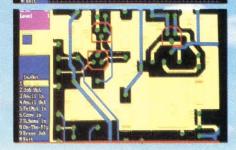
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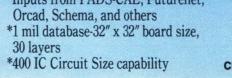
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Mass-flow transducers

flowing gas absorbs heat (measured in calories) from one of the sensing elements and transfers heat to another. The difference in heat transfer is directly proportional to the mass flow of the gas (see box, "A brief tutorial on thermal mass flow"). The transducer's two sensing elements usually lie in the arms of a Wheatstone bridge, so you can derive a usable signal from the device. A linearized amplifier provides a dc output signal that's proportional to the error signal in the bridge for measuring the mass-flow rate.

The mass-flow controller adds a voltage comparator to the measuring unit. The comparator compares the dc output signal with an external control signal to provide a set point for turning on a control valve. Many mass-flow controllers have a solenoid-controlled valve that is in-

tegral to the unit. Both mass-flow meters and mass-flow controllers sometimes include bypass elements that ensure that the flow will be "laminar," or smooth-layered. The heated sensor channel for these devices is well defined: It has a lengthto-diameter ratio of at least 100, so the gas flows in a viscous manner.

Datametrics' line of calorimetric mass-flow transducers illustrates the thermal-measurement principle. The company's Type 831 is a typical calorimetric mass-flow meter. The company adds a comparator and a solenoid valve to create the Type 825 mass-flow controller (Fig 1). When gas enters the device, most of it passes through a bypass element. The pressure drop across the bypass element diverts a small portion of the gas through a thin sensor tube.

The stainless-steel sensor tube

has two resistive coils of wire wound around it. The coils connect to two resistors to form a Wheatstone bridge. A power supply drives constant current into the resistive coils, heating the walls of the sensor tube. An amplifier determines whether the bridge is balanced. A volume of gas flowing through the tube absorbs heat from the tube and the upstream coil, causing the Wheatstone bridge to be unbalanced.

Keep Reynolds number under 2000

For a mass-flow transducer to operate predictably, the gas flow must be laminar. When the flow is turbulent, it breaks into eddies. A dimensionless number, called the Reynolds number, characterizes the way a gas flows in a tube. The number is essentially a ratio of the gas's inertial forces to the tube's drag

A brief tutorial on thermal mass flow

The underlying principle of the thermal mass-flow transducer is the ideal gas law:

PV=NRT, (A) where P is the gas pressure, V is the volume of the gas, N is the number of gas molecules in the volume, R is the universal gas constant, and T is the temperature of the gas.

Around the year 1800, Avogadro introduced the idea that the molecular weight of any element contains the same number of atoms. In other words, for any element,

N = m/M = a constant, where m is the mass of one gas molecule and M is the molecular weight of the gas. Therefore, the ideal gas law (Eq

A) can be expressed as PV = (m/M)RT.

Rearranging this expression to

solve for the mass of the gas yields

 $m = M \times (P/RT) \times V$.

Because the gas pressure and temperature are held constant while the transducer measures mass flow, a device that measures the volumetric flow rate of a gas actually measures the mass-flow rate of the gas passing through a plane in the pipe. In other words,

 $dm/dt = K \times dV/dt,$

where

 $K = M \times (PV/RT) = constant.$

When a volume of gas under constant pressure flows through a pipe with a temperature gradient, the molecules absorb heat from the vessel. If the molecules experience a temperature rise from T_1 to T_2 , the power (heat/time) absorbed by the molecules is

 $P = dQ/dt = (dm/dt) \times C_p \times (\Delta T),$

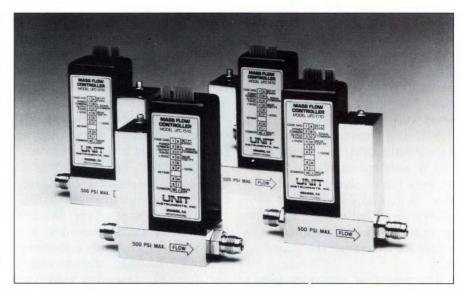
where P is the power supplied by the heater (calories/time), C_p is the specific heat of the gas (calories/grams°C), dm/dt is the massflow rate (grams/time), and ΔT is (T_2-T_1) in °C.

Obviously, a volume of gas flowing through a vessel at the same temperature absorbs no power from the vessel. However, when the gas passes through a portion of the vessel that is heated by a resistive element, the gas molecules absorb power proportional to the temperature differential (ΔT) and the specific heat of the gas (C_p). The electric circuit that's delivering electric power to the resistive element's wires detects the heat-power loss and generates a signal proportional to the flow rate.

Mass-flow transducers

forces. A Reynolds number below 2000 implies laminar flow; a Reynolds number above 3000 implies turbulent flow. The range between these values—2000 to 3000—is a transition zone, in which the flow is not distinguishably laminar or turbulent. The conventional method for reducing the Reynolds number of a turbulent gas to that of a laminar gas is to pass the gas through a laminar-flow element, which is a large number of thin capillary passages.

The laminar-flow element in the 831 and 825 transducers consists of etched channels in a stack of stainless-steel disks. The transducers accommodate a varying number of disks, so they can handle a wide variety of flow ranges. You can easily disassemble the disk stack to change flow ranges or clean the channels. The transducers come in a wide variety of maximum flow ranges, extending from 5 SCCM (standard cubic centimeters/minute) to 20 SLM (standard liters per



Thermal mass-flow controllers come with a variety of enhancements. Some of Unit Instruments' line controllers have upstream buffers to maintain repeatable manifold pressures and automatic zeroing circuitry.

minute), calibrated with nitrogen (N_2) gas. The units are specified to operate with gas pressures ranging from 80 torr (1 torr=760 mm of mercury at atmospheric pressure; 760 torr=1 atmosphere) absolute to 500 psig (psi gauge) and can with-

stand gas pressure of 2500 psig without leakage.

The 831 and 825 provide a 0 to 5V dc or 0 to 10V dc output level for measuring mass flow. The 825 has an external control signal that can set a mass-flow setpoint for its

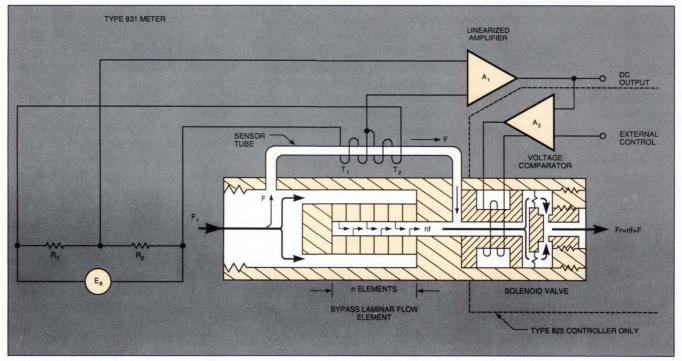


Fig 1—By adding a voltage comparator, an external control input, and a solenoid control valve, Datametrics transforms its calorimetric mass-flow meter into a mass-flow controller.

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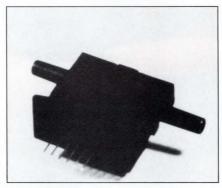
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Mass-flow transducers

internal solenoid control valve. The unit specifies a 6-sec step-response time for the gas flow to settle to within 2% of its steady-state setpoint. A 600-msec version is optional. In addition, it specifies $\pm 1\%$ accuracy, $\pm 0.15\%$ repeatability, a 5 to 40°C temperature range, and a zeroing temperature coefficient that is less than 0.05% of full scale/ °C. The unit also has a valveoverride input that can shut off the valve in an emergency. The 825 costs between \$600 and \$1500, depending on the options and the type of hermetic seal you choose.

Brooks Instrument (a division of Emerson Electric Co) and Omega Engineering offer calorimetric mass-flow transducers that have a slightly different arrangement for the resistive coils surrounding the sensor tube. Both companies use a 3-coil arrangement whereby a center coil supplies additional heat to the sensor tube. Besides supplying heat, the two end coils also act as resistance-temperature-detector (RTD) sensors (Fig 2). When there is no flow, the heat reaching each RTD is equal. When the molecules of the gas flow through the upstream RTD, they carry away an



The microbridge airflow sensor from MicroSwitch is small enough to be mounted on a circuit board.

amount of heat that is proportional to the mass-flow rate. The process is repeated at the downstream RTD, except that less heat is transferred, because the gas is preheated by the center coil. To measure the flow rate, a Wheatstone bridge senses the temperature differential between the upstream and downstream coils.

The Brooks 5850E series of massflow controllers features adjustable laminar-flow elements that accommodate maximum nitrogen flow ranges from 3 SCCM to 100 SLM. The units provide a 0 to 5V dc output signal and accept a 0 to 5V dc setpoint command. They specify a step-response time of 3 sec to settle to within 2% of the steady-state flow, $\pm 1\%$ accuracy, 0.25% repeatability, an analog setpoint command input from 0 to 5V, and a zeroing temperature coefficient of less than $\pm 0.075\%$ of full scale/°C. The units can operate with a maximum pressure of 1500 psig, and their integral solenoid-controlled valve can be closed by an override command. Model 5850EM, which sells for \$22, specifies leak integrity of less than 1×10^{-10} atmospheres-cc/sec of helium (He).

Omega offers an optional laminarflow bypass set for its FMA-5000 series of mass-flow meters. The option has two bypass elements, each consisting of a cylinder on whose circumference you can cut rectangular slots to adjust for laminar flow. You can easily install the elements in an FMA-5000 Series flow meter in the field. The standard flow meters provide a 0 to 5V dc output and come in a maximum nitrogen flow range of 10 SCCM to 40 SLM. The FMA-5600 flow meter comes with an LCD digital display and costs \$495. The optional laminarflow bypass set costs \$30.

Most manufacturers use nitrogen

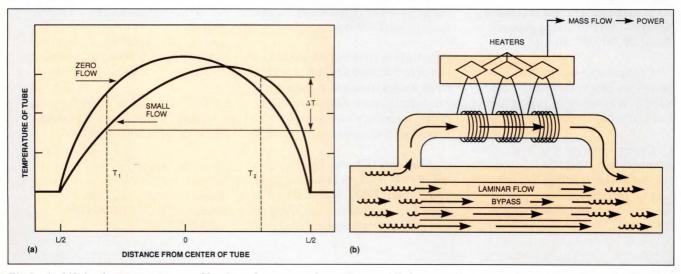
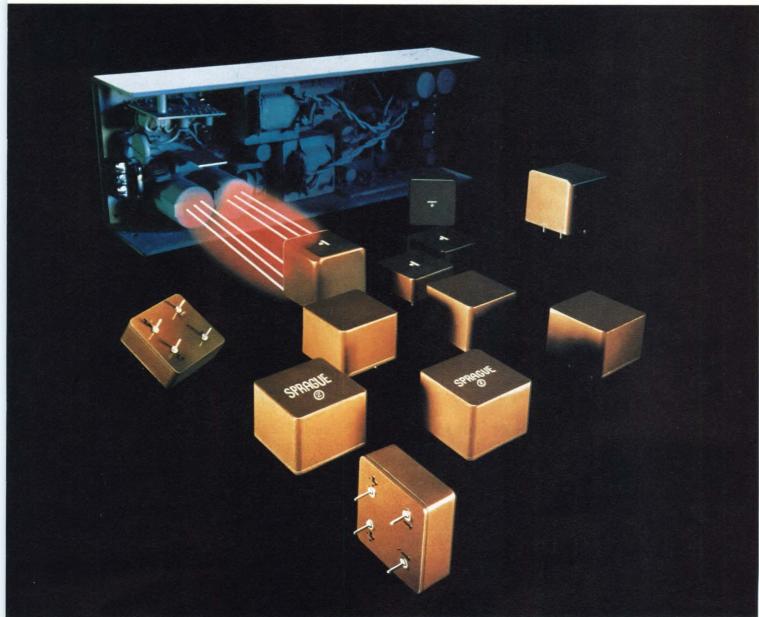


Fig 2—A shift in the temperature profile along the sensor tube produces a ΔT that you can use to measure mass flow (a). The MKS Instruments units, however, apply electrical power to three heaters to maintain a constant profile along the tube (b). The additional power represents the mass flow.

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Mass-flow transducers

or air to specify a transducer's standard flow range. When you use the mass-flow meter to measure other gases, you must apply a correction factor to the full-scale reading. The correction factor is a ratio of the specific-heat coefficient (C_p) and the molecular weight (M) of the reference gas to those of the actual gas. For example, to determine the flow rate of CO_2 when the flow transducer is calibrated for 100 SCCM of nitrogen, you apply the following correction factor:

$$\begin{split} & \mathrm{Q(CO_2} \, = \, \frac{M(\mathrm{N_2})}{M(\mathrm{CO_2})} \, \, \times \\ & \frac{\mathrm{C_p(\mathrm{N_2})}}{\mathrm{C_p(\mathrm{CO_2})}} \, \, \times \, \, \mathrm{Q(\mathrm{N_2})} \end{split}$$

where $Q(CO_2)$ is the flow rate of CO_2 , $M(N_2)$ is the molecular weight of N_2 , $M(CO_2)$ is the molecular weight of CO_2 , $C_p(N_2)$ is the specificheat coefficient for N_2 , $C_p(CO_2)$ is the specific-heat coefficient for CO_2 , and $Q(N_2)$ is the flow rate of N_2 .

Unit Instruments Inc, which manufactures a line of calorimetric mass controllers for controlling gas flow during semiconductor-wafer fabrication, points out that the closer in density and specific heat the reference gas is to the gas being measured, the more accurate the calibration. To calibrate its controllers, therefore, the company uses nine different reference gases and closely matches the molecular characteristics of the reference gas to the gas being measured. In this manner, the company reduces correction-factor errors from typically 5% to 2%.

The Unit Instruments mass-flow controllers have flow ranges from 20 SCCM to 10 SLM. Both the output dc signal and the setpoint input signal have 0 to 5V dc ranges. The units specify $\pm 1\%$ accuracy, $\pm 0.15\%$ repeatability, a zeroing temperature coefficient of 0.02%



By maintaining a constant profile on a calorimetric flow sensor, MKS Instruments' controllers achieve response times of less than 500 msec.

full scale/°C, leak integrity of 1×10^{-9} atmospheres-cc/sec of He, and maximum operating pressure of 500 psi. An automatic zeroing feature is standard on the UFC-1200 and UFC-1500 and is optional on the other models. The UFC-1400 and UFC-1500 use a pressure regulator to compensate for upstream pressure changes.

Response-time improvements

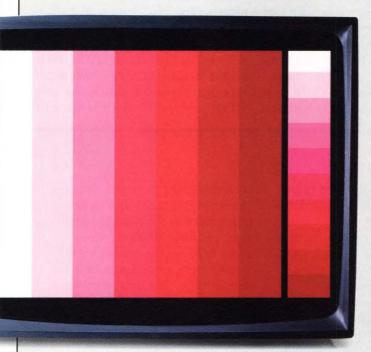
All of the Unit Instruments controllers specify response times (to 2% of the setpoint setting) from 400 to 800 msec. Although controllers with response times of less than 1 sec are becoming more common, it's significant to note that as recently as 1979 a mass-flow controller very often required 1 minute to settle after receiving a command. A slow reponse time means that the process is out of control for a long period, which seriously degrades its repeatability specification.

MKS Instruments, another manufacturer of mass-flow controllers for the semiconductor industry,

also offers some fast items in its product line. The 1359A specifies a response time (to within 2% of the setpoint) of less than 500 msec. Both the dc output signal and the setpoint signal have 0 to 5V dc ranges. The \$945 controller comes with full-scale ranges from 10 SCCM to 50 SLM and specifies $\pm 0.5\%$ accuracy, $\pm 0.5\%$ repeatability, a zeroing temperature coefficient of less than 0.02% of full scale/°C, maximum operating pressure of 150 psig, and leak integrity of less than 10⁻⁹ atmospheres-cc/sec of He. The unit operates with a minimum pressure drop of 5 torr at standard conditions and has an override-signal input to control the valve.

The MKS units employ a controlled temperature profile to measure gas flow. In all of the devices previously mentioned, the temperature profile along the sensor tube shifts as gas flows through the tube (**Fig 2a**). Because the profile shift produces a temperature differential that is nonlinear with mass flow,

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Mass-flow transducers

these transducers must have some linearization method to generate the dc output signal. But MKS Instruments' controlled-profile technique makes it unnecessary for the manufacturer to perform linearization. The MKS units use three nulling Wheatstone-bridge heaters, which keep the temperature profile constant as gas flows through the sensor tube. The technique automatically compensates for any temperature shift by driving more power into the bridges as the massflow rate increases. Therefore, the temperature profile remains constant and the additional power is proportional to the mass-flow rate. This method is inherently fast, because the controllers don't have to wait for the sensor tube to reach thermal equilibrium.

Using a calorimetric mass-flow transducer is not the only way to measure mass flow by thermal means. The immersion mass-flow transducer measures the amount of cooling the gas velocity produces on a heated sensor immersed in the flow stream. The mass-flow meters from Kurz Instruments Inc., for example, measure mass flow with two RTDs that are perpendicular to the gas flowing in a pipe. The upstream RTD, R_{tc}, detects the ambient temperature of the gas; the downstream RTD, Rp, is heated to a temperature that maintains a constant

differential above R_{tc}.

The RTDs operate as resistive legs in a nulling Wheatstone bridge, which attempts to maintain a constant temperature differential between the RTDs when gas flows through the pipe. The faster the gas flows past the R_p sensor, the more power is required to maintain a constant temperature differential between the RTDs. The additional power delivered to the sensor is a measure of heat loss and, consequently, of the mass flow of the gas.

The Kurz flow meters have two different RTD housings. The MetalClad housing consists of two separate mandrels on which the two RTDs are wound. Both sensors fit

Setting a mass-flow standard

The problem of defining a set of standards for specifying a massflow transducer has plagued the semiconductor-equipment industry seemingly forever. For example, mass-controller manufacturers have only recently agreed on a standard pressure and temperature condition. Manufacturers of mass-flow transducers use a standard condition to calibrate their devices. They specify volumetric flow with terms such as SCCM (standard cubic centimeters per minute) and SLM (standard liter per minute), which both assume that a standard temperature and pressure condition exists. To use these devices under other conditions, you must modify the flow readings by using the following formula:

 $Q_a = Q_s \times (P_a/P_s) \times (T_s/T_a)$, where Q_a is the actual flow rate, P_a is the actual pressure condition, T_a is the actual temperature condition, Q_s is the standard flow rate (for example, SCCM or

SLM), P_s is the standard pressure, and bT_s is the standard temperature.

Some vendors specify the standard condition as 70°F (21.1°C) and 1 atmosphere (14.7 psia) of pressure; others say it's 0°C (32°F) and 1 atmosphere of pressure. The discrepancy causes headaches for people who use transducers from different vendors. In addition, methods for specifying such parameters as accuracy, repeatability, response time, input and output pressure, differential pressure, and linearity have a wide variety of interpretations throughout the industry.

To bring some order out of this chaos, the mass-flow controller committee of the Semiconductor Equipment and Materials International (SEMI) group have been holding a series of meetings to establish some industry standards on these issues. According to Joe Dille, a co-chairman of the

committee, the members have established 0°C and 1 atmosphere of pressure as the standard condition, and have drafted a document defining the guidelines for measuring a mass controller's response time. The draft has been sent to committee members for ballot approval. (The deadline for voting coincides approximately with the publication of this article.)

Various other issues remain on the docket, however. Joe Dille and other committee members are concerned that the standards being set by the SEMI committee lack the user's point of view. Users of mass-flow meters and controllers who are interested in participating are encouraged to contact Sarah A Ferguson, Standards Coordinator, at 805 E Middlefield Rd, Mountain View, CA 94043. Phone (415) 964-5111. FAX 415-967-5375. TLX 856777.



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Mass-flow transducers

inside an open sensor window in a steel block through which gas flows. In the DuraFlo housing, the separate mandrels are encased in epoxy. The RTDs connect to a circuit board containing the nulling Wheatstone bridge and a linearized amplifier. Both housings are installed in a pipe section with a fixed diameter to measure the gas velocity. The massflow rate is determined by muliplying the standard velocity of the gas by the area of the pipe, according to the equation:

$SCFM = SFPM \times A$,

where SCFM is the volumetric flow of the gas in standard cubic feet per minute; SFDM is the velocity of the gas in standard feet per minute; and A is the cross-sectional area of the pipe.

The flow pipe has an upstream nozzle to correct for wall effects. The Model 565 has a DuraFlo housing for the sensors and comes in flow ranges from 50 SCCM to 50 SCFM. It specifies accuracy of $\pm 3\%$ of full scale, $\pm 0.25\%$ repeatability, a maximum operating pressure of 100 psia, and a typical response time of 1 sec (a 35-msec version is optional). Unlike the bypass-

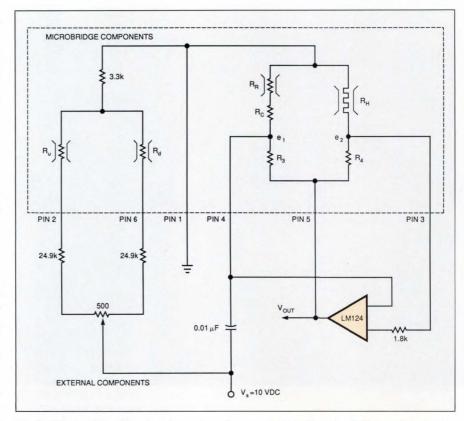
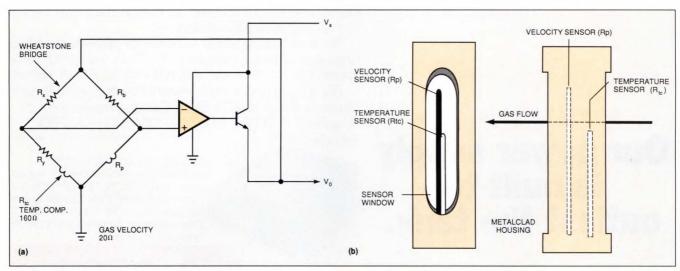


Fig 3—You need to add only a few external components to the microbridge airflow sensor to measure mass flow. The circuitry shown provides a 45-mV output for 200 SCCM of gas flow.

sensor-tube arrangement, the immersion method is sensitive to the sensor orientation. The two coils are perpendicular to the gas flow; the $R_{\rm tc}$ coil is located upstream for

calibration purposes. Deviations from this arrangement in pitch or yaw can cause reading errors.

The FMA-600 series of mass-flow meters from Omega operate on the



An immersion mass-flow transducer places a temperature-compensating resistor and a gas-velocity-measuring resistor in the arms of a nulling Wheatstone bridge (a). In Kurz Instrument's MetalClad housing, the sensors are perpendicular to the flow direction (b).

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Applications-Driven Microcontrollers

Mass-flow transducers

same immersion principle as that of the Kurz models. The heated sensor maintains a constant 60°F temperature differential between the temperature-compensating coil and the heated probe. One feature of the immersion method is its low sensitivity to particle contamination. The immersion method is resistant to particle contamination, because the upstream coil creates a bow wave in the gas-flow stream. The bow wave prevents particles from adhering to the sensor coil.

A sensor for circuit designers

The flow meters and controllers mentioned thus far operate from either $+15\mathrm{V}$ or $-15\mathrm{V}$ dc power supplies or a combination of the two. Their power consumption can range from 1.5W for the Datametrics 831 mass-flow meter to 10.5W for Brooks' 5860E flow meter.

Although it's based on the same thermal mass-flow principle as those devices, the microbridge mass-airflow sensor from Micro Switch (a division of Honeywell) doesn't really fit into the same category. The product is a unique (and patented) thermal mass-flow sensor on a silicon chip that operates from a +10V dc supply and consumes only 30 mW. To make the sensor a usable mass-flow monitoring device, you have to add some supporting circuitry. The sensor consists of a thin-film, thermally isolated bridge structure that contains a heater element and two temperature-sensitive resistors. The company suspends the structure over an anisotropically etched silicon chip to produce a calorimetric massflow sensor.

During the AWM2100V microbridge sensor's operation, gas flows laterally across the bridge, cooling the upstream resistor and transferring heat to the downstream resistor. By adding a few external components, you can build a nulling-Wheatstone-bridge circuit to monitor the mass-flow rate of the gas (Fig 3). The circuit delivers approximately 45 mV for a gas-flow rate of 200 SCCM. The trimming potentiometer provides 30-mV adjustment range at 100 SCCM. The sensor can operate over -25to 85°C with a maximum shift of 2 mV from 25°C to either temperature extreme. Because of its small size and thermal isolation, the AW2100V has a time-response specification of 5-msec max. The \$70 unit weighs 13g and can withstand 5 psi pressure and 100g peak shock. The sensor is currently in use in the medical and energy-management fields. In addition, automotive manufacturers are investigating the possibility of using the sensor in electronically controlled carburetion systems for automobiles.

EDN

Article Interest Quotient (Circle One) High 515 Medium 516 Low 517

For more information . . .

For more information on the thermal mass-flow transducers discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Brooks Instrument 407 W Vine St Hatfield, PA 19440 Phone (215) 362-3500 TLX 846181 Circle No 710

Datametrics 340 Fordham Rd Wilmington, MA 01887 Phone (508) 658-5410 FAX 508-658-7969 TWX 710-347-7672 Circle No 711

Kurz Instruments Inc 2411 Garden Rd Monterey, CA 93940 Phone (408) 646-5911 FAX 408-646-8901 TLX 172275 Circle No 712 Micro Switch 11 W Spring St Freeport, IL 61032 Phone (815) 235-6600 Circle No 713

MKS Instruments Inc 6 Shattuck Rd Andover, MA 01810 Phone (617) 975-2350 FAX 617-975-0093 TLX 17-975-0094 Circle No 714

Omega Engineering Inc 1 Omega Dr Box 4047, Stamford, CT 06907 Phone (800) 826-6342 FAX 203-359-7700 TLX 996404 Circle No 715 Unit Instruments Inc 1247 W Grove Ave Orange, CA 92665 Phone (714) 921-2640 FAX 714-921-0804 TLX 183439 Circle No 716 Analog Design Insights from Maxim Integrated Products

June '89

Serial 5µs 12-Bit A/D Converter Fits In Space Saving 8-Pin DIP

In real-world data acquisition applications, constraints such as on board space, system cost and the need for electrical isolation often make serial data interfaces an attractive alternative to "broadside" parallel interfaces. This is especially true in high resolution A/D systems due to the number of data lines involved. A 12-bit parallel interface uses up to 15 circuit board traces and consumes significant board area. In contrast, the same converter with a serial interface requires only three interface traces. Additionally, 12-bit parallel converters are often housed in large double-width 28- or 40-pin packages, whereas serial devices are far smaller.

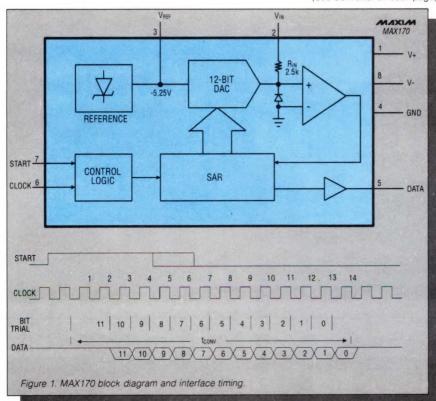
The new MAX170 CMOS 12-bit A/D from Maxim saves considerable space and cost with its serial interface and small footprint. This A/D also reduces component count by including a precision internal reference in its 8-pin DIP (or 16-pin small outline (SO)) package (Figure 1). Although the MAX170 has a serial architecture, it retains one advantage typically associated only with parallel interfaces— high conversion speed. Data is transmitted without delay while the con-

version takes place. Thus a complete 12-bit result appears at the receiving end of the serial link, at the microprocessor, in as little as $5\mu s$.

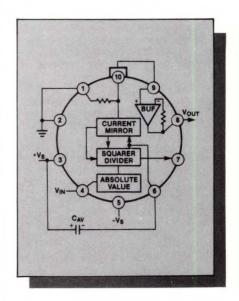
The MAX170 interface requires only a clock, a Start Conversion (START) input, and one serial data (DATA) output. This allows the A/D to conveniently communicate with digital signal processors such as the TMS32020, $\mu P32020, \mu P7720$ and the DSP56000. It also works with general purpose serial-to-parallel converters such as the 74HC595 in designs where serial data is converted to parallel format at the receiving end.

Each rising edge at START starts a new conversion. The MAX170's successive-approximation-register (SAR) and DATA output are reset on the next rising CLOCK edge. The MSB appears at DATA on the next CLOCK cycle, and subsequent bits follow on succesive clock cycles. At the end of the conversion, DATA goes high until the next conversion. The MAX170 also operates in a free running mode where START, as an EOC output, indicates when conversions start and end. This is useful in stand alone applications that are not under μP control.

(See Converter on back page)

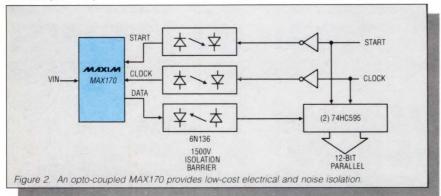


True RMS-TO-DC Converters Work With Any Signal Type



The root-mean-square (RMS) value of a waveform is used when measuring the power of signals which are likely to be something other than pure sine waves. Average responding measurements are simpler to make, but provide significant errors for non-sine signals. Maxim's AD536A and AD636 compute the true RMS value of complex AC signals, with or without DC components. These RMS converters also complement display-oriented A/D converters from Maxim, such as the industry standard ICL7106/7107, or new generation integrating converters such as the MAX130/131, MAX138/139/140, and the 40,000 count MAX133/134.

Low supply current (800µA to 1.2mA) allows Maxim's AD536A and AD636 to be used in hand-held instruments. A single external averaging capacitor is required to perform measurements to the specified accuracy. This capacitor is selected to trade-off low frequency accuracy, ripple, and settling time. Laser trimming at the factory means that no external trims are required to achieve the fully rated accuracy. An auxiliary dB output is also available, representing the logarithm of the DC output voltage. The AD536A and AD636 differ primarily in their maximum error, bandwidth, and crest factor specifications, with the AD536A being the higher performance part. For applications not requiring premium specifications, Maxim's AD636 offers a lower cost alterConverter (continued)



A serial interface is especially handy in opto- or transformer- isolated A/D applications. For example, transducer outputs often require electrical isolation to separate sensitive electronics from hazardous electrical conditions, provide noise immunity or bridge large differences in ground potential. Analog isolation amplifiers typically used for this function often add up to \$100 per channel to the system cost. The MAX170 provides a low cost alternative to isolation amplifiers, and performs the A/D conversion as well (Figure 2). Data is transmitted across a 1500V isolation barrier by three 6N136 optoisolators. Shift registers then reconstruct a 12-bit parallel output. Conversion time is limited by the speed of the optoisolators and is 100µs with a 140kHz clock. For those who prefer even greater space savings, a new part that combines the MAX170, three opto-isolators and load resistors in a 16-pin package will be introduced by Maxim soon.

The MAX170 maintains state-of-theart electrical specifications despite its small package size. Integral linearity error is guaranteed to be less than 1/2LSB, with no missing codes over the parts' temperature ranges. The on-chip buried zener reference is drift tested to be better than 20ppm/°C, and can sink up to 5mA of external load current. The MAX170 works with +5V and -12V to -15V supplies, dissipating only 115mW.

Maxim also supplies the following serially interfaced DACs that are counterparts of the MAX170: the MAX543, a 12-bit multiplying D/A converter in an 8-pin package, and the MAX500, a quad 8-bit voltage output D/A converter. Both are low power CMOS devices as well.

5µs 8-Bit A/D Converter With Track/Hold Samples 50kHz Full Power Signals

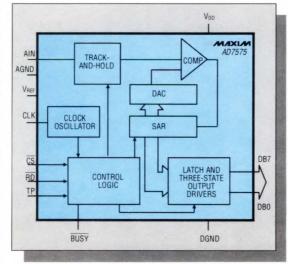
Maxim's AD7575 high-speed A/D with built-in track-and-hold (T/H) effectively replaces older generation 8-bit A/Ds by providing faster conversion times while eliminating external track/hold circuitry. Successive approximation provides a 5μs conversion time, and the T/H accurately samples full scale signals to 50kHz (386mV/μsec slew-rate). The T/H is completely self-contained including an on-chip hold capacitor. The AD7575 needs

only a single +5V supply (dissipating 125mW) and an external, low-cost 1.23V bandgap reference (such as Maxim's 8069). The converter's input span ranges from 0V to twice the reference voltage (2.56V). Offset, gain and linearity errors are minimized so that a total accuracy of 1 LSB is maintained without adjustments.

The AD7575 interfaces with all popular 8-bit microprocessors using only CS, RD, and latched three-state data outputs to start a conversion and to read data. The A/D looks like a memory-mapped device, and interfaces as a slow memory or ROM. Fast interface timing allows the part to converse with

microprocessors such as Z80H, 8085A-2, 6502B, and 68B09 as well as DSP processors like the TMS32010.

A sister part, Maxim's AD7576, offers a lower cost alternative and differential inputs for applications that do not require an on-chip track-and-hold and can work with a slower 10µs conversion time. All other features of Maxim's AD7575 are contained in its AD7576.



High-Speed 12-Bit D/A Converters Settle In 250ns

Maxim's AD565A and AD566A are 12-bit monolithic digital-to-analog converters (DAC) built with bipolar technology to offer an excellent combination of high speed and 1/2 LSB linearity. One advantage that bipolar DACs have over CMOS current output DACs is a wide output compliance range of -1.5V to +10V. This means that their current output is simply converted to a voltage by terminating the current output with a resistor. A second advantage of bipolar is output settling speed. Output settling to within 1/2 LSB, for a full scale change in code, occurs in less than 250ns for Maxim's AD565A and 350ns for Maxim's AD566A. This performance makes these 12-bit monolithic DACs ideal choices for video displays and high speed control applications. The AD565A includes a precision 10V reference, while the AD566A requires an external reference. This reference uses a buried-zener diode and laser-trimmed thin-film resistors to minimize temperature drift. Drift limits range from 15 to 50ppm/°C depending on device grade. Laser trimming also results in better than 1/4 LSB linearity at wafer level.

Maxim's AD565A and AD566A also include precision on-chip resistors which can be connected as feedback and/or offset resistors using an external amplifier to obtain unipolar and bipolar output swings. They can also be used as the input resistors when building high speed A/D converters. Excellent resistor matching and tracking assures gain and offset stability over time and temperature. The AD565A operates with ±12V to ±15V supplies, dissipating 225mW, whereas the AD566A requires only a single -12V to -15V supply and consumes 180mW.



1988/89 Analog Applications Handbook

(CIRCLE 15)

Data Sheets

(CIRCLE 10) MAX500/543 (CIRCLE 11) MAX170 (CIRCLE 12) AD536A/636 (CIRCLE 13) AD7575/76 (CIRCLE 14) AD565/6

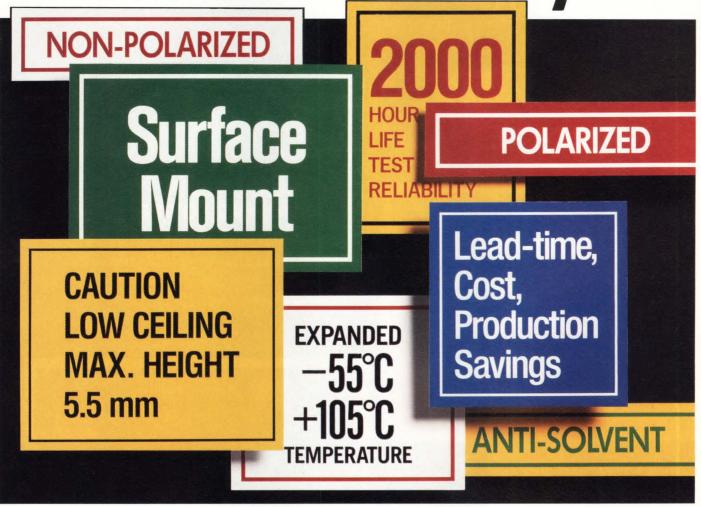


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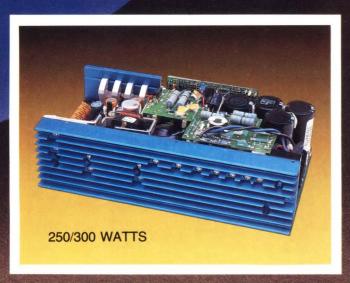
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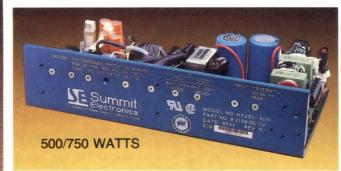
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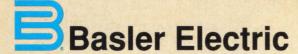
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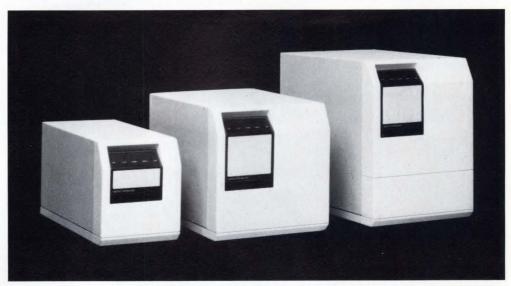
By protecting your computer equipment from line-supply disturbances, uninterruptible power supplies can repay their capital cost the first time they prevent the loss of valuable data.

Peter Harold, European Editor rotecting a personal computer, network file server, or small LAN from inadvertent line-supply failure or damaging line-borne interference is one way in which you can help preserve your computer hardware and the data contained within it. Modern uninterruptible power supplies capable of supplying a PC and several peripherals are small enough to fit unobtrusively alongside your PC or under its desk. Some versions even fit under a computer's monitor.

Although a PC or small CAD workstation may represent only a few thousand dollars worth of hardware, the data residing on its hard disk can represent tens of thousands of dollars worth of engineering effort. The risk of losing that work because of a hardware failure or data corruption shouldn't be overlooked. Even if you adhere to rigorous

backup procedures—and many of us don't—the loss of a few hours worth of work on the computer because a road digger severs an electricity supply cable is at the very least a severe psychological setback.

Temporary blackouts, however, are only one of the hazards that your computer can encounter when it's directly connected to a raw line supply. Voltage dips and short-term outages, which are generated by protection equipment on the ac-line distribution system, are relatively common occurrences. Together with brownouts, which are caused by the supply company's having insufficient generating capacity, these disturbances force your computer's switch-mode power supply to run dangerously close to its minimum input voltage rating or deprive it completely of a few cycles of input power. Overvoltages caused by switching transients, lightning bolts, or



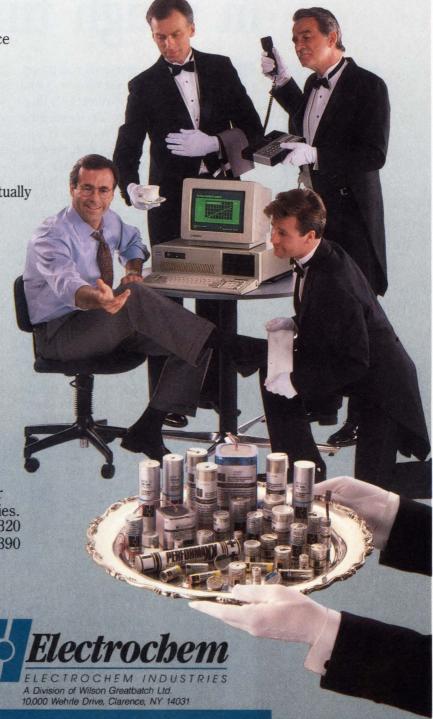
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Uninterruptible power supplies

noisy electrical equipment are potentially more hazardous because they pose a threat to your computer's hardware.

The degree of protection your computer requires depends on how clean your line supply is—in the absence of hard information, assume it's bad—and on how critical it is that your computer, file server, or network stays in operation. As with most things in life, the degree of protection your equipment gets depends on how much you're prepared to pay.

On-line or off-line?

In general, an uninterruptible power supply (UPS) falls into one of two categories—a true on-line UPS or an off-line standby power supply (SPS) with line-conditioning circuitry. This article refers to both

types as uninterruptible, although there is some debate within the industry about whether the SPS type exactly meets this definition.

True on-line UPSs tend to be the most expensive type but provide a high degree of protection. In this type of UPS (Fig 1a), the load is continuously supplied from an inverter that generates a sinusoidal output from a dc input. Whenever the line input is within specified limits, this dc input is provided by the UPS's input rectifier. When the line input falls outside these limits, the dc input to the inverter automatically commutates to the UPS's standby batteries.

Theoretically, on-line UPSs provide near-perfect isolation between the line input and the load for all types of line disturbance. However, this isolation may be compromised because most on-line UPSs incorporate a static bypass switch (Fig 1b), which under certain circumstances connects the load directly to the line input, thus bypassing the unit's rectifier and inverter.

Bypassing the rectifier and inverter is necessary to cope with high transient load currents, such as the inrush current drawn by equipment each time you switch it on. On its own, the inverter is usually unable to cope with these transient currents. The static bypass switch is also activated if the inverter itself fails for any reason. While this switch is activated, the load is unprotected from any line disturbances unless the bypass circuit itself includes line-conditioning circuitry. In addition, most static bypass switches have a transfer time of a few milliseconds, so that

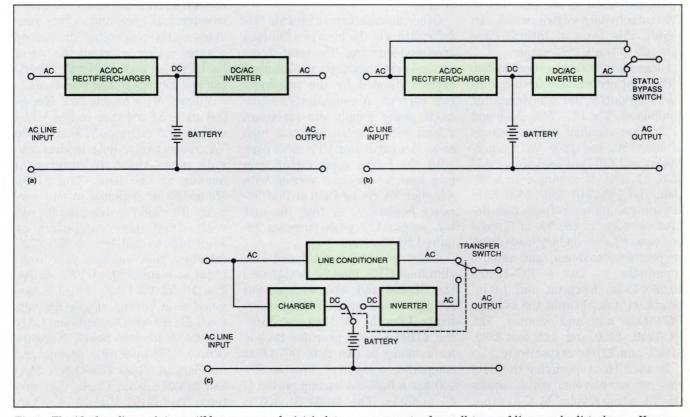


Fig 1—The ideal on-line uninterruptible power supply (a) isolates your computer from all types of line supply disturbance. However, many on-line UPSs require a static bypass switch (b) to cope with high transient load currents. In a UPS based on the standby-power-supply principle (c), the inverter is only activated when the line supply falls outside predefined limits. Its performance depends very much on the effectiveness of the line conditioner and on the speed of the transfer switch.

Uninterruptible power supplies

each time the switch is activated, your computer may be deprived of part of an input cycle.

In general, on-line UPSs provide excellent protection against momentary line disturbances—for example, flicker, voltage dips, voltage surges, voltage spikes, and shortterm outages-as well as brownouts, blackouts, and frequency variations. In addition, their static bypass switches let them maintain their output voltage while delivering surge currents many times greater than their nominal output rating. This characteristic suits online UPSs for use in situations several independently where switched loads are connected to a single unit. However, their effectiveness in protecting a load from high-frequency transients, such as voltage impulses and spikes, may be compromised by the presence of the static bypass switch, which can couple this type of interference through to the UPS's output.

Clary Corp makes several on-line UPSs that are suitable for use with microcomputer and minicomputer equipment. The PC-1240, -2400 and -1.2k have nominal output ratings of 360, 750, and 1200 VA, respectively, and full-load backup periods of 5, 12, and 12 minutes. In addition, the PC-1240 and -2400 have separate ac power outputs that deliver as much as 480 VA of filtered line power for secondary loads, such as printers, modems, and remote terminals. The PC-1240's 15.75×15 -in. footprint and 1.9-in. height let it fit between the average PC's base unit and monitor. The PC-1240, -2400, and -1.2k cost \$890, \$1490, and \$2790, respectively.

In addition to specifying the UPS rms output current, which equals the VA rating divided by the output voltage, Clary specifies peak repetitive output currents of 8, 16, and 24A for the PC-1240, -2400, and -1.2k, respectively. This spec is im-

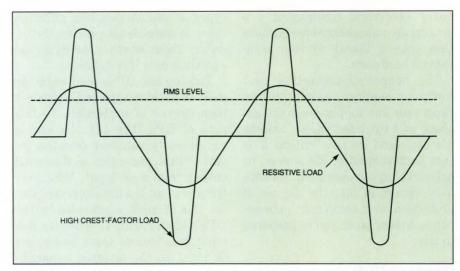


Fig 2—Your computer's switch-mode power supply doesn't present a UPS with a resistive load. Instead, it draws a current with a high crest factor—sometimes as high as 3.

portant because it indicates how well the UPS can drive the non-linear loads presented by a computer's switch-mode power supply (Fig 2).

Other manufacturers provide this information in the form of a full-load crest-factor rating. The crest-factor rating is the maximum peak output current divided by the maximum rms current. A computer's switch-mode power supply can represent a load with a crest factor as high as 3. If a particular UPS can't cope with the load's crest factor, you may have to choose a version with a higher VA rating than at first appears necessary, so that the unit can output the peak currents required by the load.

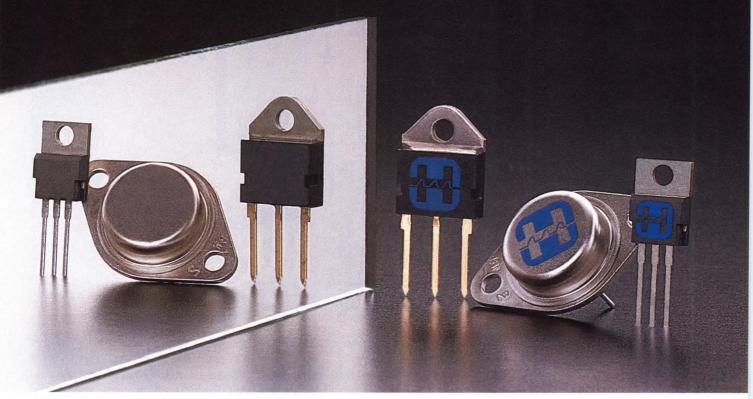
Clary recently introduced two slim-line UPS models designated the SL-400 and -800 with output ratings of 400 and 800 VA, respectively. Like the PC-1240 and -2400, the \$1290 SL-400 provides backup for as many as two IBM PC/AT or compatible computers, but the SL-400 has a full-load backup period of 30 minutes. The \$1690 SL-800 is targeted for use with small PC networks or network file servers and has a full-load backup period of 10 minutes. Both units also provide

480 VA of filtered line power for the computer's peripherals. Despite the extra battery capacity required by these units, they're still small enough to sit between a computer's monitor and base unit. Clary provides a universal voltage/frequency adapter option to permit the use of its UPSs at various North American and European line standards.

Viteg Corp's Benchmark Model-386 and -15A are true on-line UPSs with output ratings of 750 and 1500 VA, respectively. Both models provide more than 10 minutes of backup at full load. The \$1895 Model-386 is available in two versions. The 386/I is designed for use with stand-alone computers or workstations and has an RS-232C interface that enables your computer to monitor the UPS's status. The Model-386/LAN, which is targeted as a backup supply for network file servers, has optional LAN interfaces for the Novell Netware (Provo, UT) operating system and for Banyan Vines (Westboro, MA) and 3COM (Santa Clara, CA) systems. The \$3195 Model-15A is targeted at minicomputer users who want to power their units from standard 15A wall receptacles.

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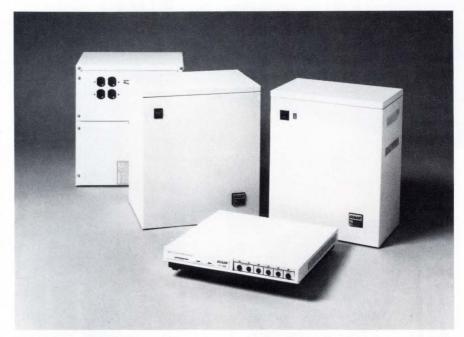
solid-state static bypass switch, which enables them to deliver single-cycle surge currents of 20 times their nominal output current and 0.5-sec surge currents of 10 times their nominal output current.

Sola Electric's PWM-series of online UPSs includes three models that are suitable for use with microcomputers and minicomputers. Generation-2 PWM Mini-UPSs are available with output ratings of 500 and 1000 VA, and both provide a full-load backup period of eight minutes. They are priced at \$2224 and \$3712, respectively. Unlike the company's earlier 750 VA and 1000-VA Mini-UPSs, these models have internal batteries rather than external add-on battery packs.

However, the \$4857, 1500-VA PWM-series UPS still uses either one or two add-on battery packs. A single battery pack provides the UPS with 10 minutes of backup; two battery packs provide 22 minutes of backup. Battery packs are priced at \$1130. This UPS incorporates a mimic diagram and output meters to let you accurately monitor its status. All of Sola Electric's UPSs can be used for both North American and European line voltages and frequencies.

Off-line costs less

UPSs that combine an SPS with line-conditioning circuitry are generally cheaper than on-line UPSs but still offer fairly comprehensive protection. Their input filters suppress input transients, pulses, and spikes. And provided they incorporate some form of voltage regulation, these units can compensate for voltage dips and sags, surges, overvoltage conditions, and brownouts. The inverter of an SPS-type UPS is normally off-line (Fig 1c). It is only activated during blackouts, short-term outages, excessive frequency variation, and brownouts that cause the input voltage to fall



The IPS range of uninterruptible power supplies from Elgar Corp includes models with output ratings between 400 and 1600 VA. The 400-VA model includes an auxiliary output that delivers 600W of conditioned line power.

below the range of the voltageregulation circuitry.

The transfer time—the time taken for the unit to detect an out-of-limit line input, run up its inverter within specified output conditions, and switch it onto the load—should be as short as possible, so that the load is subjected to the minimum possible disturbance. In practice, the transfer time can be in the order of 2 to 10 msec for off-line SPSs.

Although this type of UPS appears to cope with nearly all types of line disturbance, the degree of protection from each type may be limited. For example, if a unit doesn't include voltage-regulation circuitry, it may let wide output voltage excursions occur before it switches over to inverter/battery operation. In addition, flicker and short-term outages that are too short for the unit to detect or shorter than the unit's transfer time will be transferred to the load.

Despite their limitations, SPStype UPSs are the cheapest way to prevent a sudden loss of power to your computer. American Power Conversion Inc's range of UPSs includes 330-, 450-, 520-, 800-, and 1200-VA models, which range in price from \$399 to \$3195. Models with output ratings of 450 VA and above are available for use at North American and European line voltages and frequencies. The 520-, 800-, and 1200-VA models include a computer interface that signals to the computer that line power has failed, so that the computer can go through an orderly shutdown procedure. The maximum transfer times for these UPSs are between 2 and 4 msec. The company also produces a special version for Apple Macintosh computers. The \$399 UPS-110SE is designed to sit underneath a Macintosh and is available for both North American and European line standards.

Although these UPSs clean up the incoming line supply with RFI/ EMI noise filters and surge arresters before passing it on to your computer, they don't regulate the

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CIRCLE NO 47

Uninterruptible power supplies

line-derived output voltage. As a result, the output voltage will drop to approximately 103V before the inverter cuts in to take over from the line input. Most computer equipment will continue to operate satisfactorily with a supply voltage of 103V, but it's worth your time to check the input voltage ranges of all the equipment you intend to back up with these supplies before you buy.

Exide Electronics' MicroUPS series of UPSs includes models with specs similar to those of American Power Conversion Inc. MicroUPS models range in price from \$439 to \$1539.

AT&T's 500-VA UPS is also an SPS-based UPS and produces a line-derived output voltage between 103 and 136V at 60 Hz. The inverter cuts in at 103V or when the line frequency deviates by more than ± 1 Hz. The \$795 unit provides seven minutes of backup at full load, can drive loads with a crest factor as high as 3, and has a typical transfer time of 2 msec.

Elgar Corp's IPS family of SPSbased UPSs is available with output ratings of 560, 1100, and 1600 VA and full-load backup periods of 10, 8, and 15 minutes, respectively. The \$995 560-VA and \$1295 1100-VA models have an internal battery option that doubles their backup period. Typical transfer times for the changeover to and from inverter operation are less than 4 msec. In addition, Elgar produces a \$745 400W model, which provides five minutes of full-load backup. This model is small enough to fit under your PC's monitor and includes a 600W output that feeds conditioned line power to peripheral devices. All the Elgar units are available for use at North American and European voltages and frequencies.

Sola Electric's SPS-range of standby power supplies includes 330-, 450-, 800-, 1200-, and 1800-VA



Fitting between a PC's monitor and base unit, the SL-400 uninterruptible power supply from Clary Corp provides 30 minutes of backup power for two IBM PCs or compatibles.

models, which range in price from \$482 to \$1995. Full-load backup periods for these models are 5, 6, 12, 8, and 10 minutes, respectively. They switch to inverter operation when the line input, and hence the unit's output, drops by 15%.

Models in the company's SPSR-series incorporate an electronic power conditioner that regulates the output within +5% to -8% of the unit's nominal output voltage, which results in line input variations of +15% to -30%. These models also feature a transfer switch with a transfer time of 1 msec. The range includes 500-, 1000-, and 1500-VA models with full-load backup periods of 10, 7, and 5 minutes and price tags of \$1517, \$2331, and \$3149, respectively.

Some manufacturers have improved on the performance of low-cost SPSs by using a ferroresonant transformer as the line-conditioning element. The ferroresonant transformer has an LC tank circuit, which is tuned to the line fre-

quency. When the line input to the transformer fails, this tank circuit continues to oscillate, thus using up its stored energy to maintain the output at the transformer's secondary winding.

The ferroresonant transformer's ability to continue supplying the load for several cycles—even after the complete collapse of the line input—is used to support the load while the UPS's inverter is powered up and switched into the transformer's primary winding circuit. Hence, UPSs that employ ferroresonant transformers appear to the load as having a zero transfer time. The ferroresonant transformer also has other advantages. It provides high attenuation of both commonmode and normal-mode spikes and noise; corrects for sags, surges, and brownouts; and provides output short-circuit protection. In addition, a ferroresonant transformer provides complete isolation—of both the line and the neutral between the UPS's input and output.



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EDN May 25, 1989

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V E N A B L E

CIRCLE NO 48 81

Uninterruptible power supplies

On the downside, UPSs based on ferroresonant transformers have a limited ability to cope with linefrequency variations. Typically, they can only cope with a ± 0.5 -Hz frequency deviation in the line input before their inverter has to take over from the line supply. If your computer is unfortunate enough to have to survive large frequency variations—as might be the case if your equipment is on generator power—a ferroresonant UPS could spend much of its time switching in and out of backup mode. In such situations, an on-line UPS, which can cope with much greater line frequency variations, may be a better choice.

Best Power Technology Inc offers a complete range of ferroresonanttransformer-based UPSs. Designated Micro-Ferrups, the range includes models with output ratings of 350, 500, 750, 1000, 1500, and 2000 VA. Minimum standby periods at full load for these UPSs are 22, 13, 9, 9, 23, and 15 minutes, respectively; and they're available with inputs and outputs to suit North American and European line voltages and frequencies. Prices range from \$895 to \$3695 for 60-Hz models and \$1050 to \$4250 for 50-Hz models.

Unlike some other UPSs, Micro-Ferrups supplies have an output power rating that is equal to their VA rating, so you won't have to determine the power factor of your load. The supplies provide 2000:1 attenuation of voltage spikes-a figure that exceeds the requirements of the IEEE-587-A and IEEE-587-B lightning test standards. Best Power Technology also can supply special versions of the Micro-Ferrups units that can withstand ±3-Hz variations in line frequency before they activate their inverter.

Although they derive their output directly from the line input, Micro-Ferrups supplies provide an output regulation of $\pm 3\%$ down to line voltages of 95V. At this point, the inverter cuts in. However, during certain types of line-supply failure, the output is likely to experience single-cycle excursions outside this 3% limit, which would be equivalent to a single-cycle line dip.

Elgar's \$1295 Ferro-IPS-500 and \$1795 Ferro-IPS-1000 are also based on ferroresonant transformers. With specifications similar to Best Power's 500-VA and 1000-VA Micro-Ferrups but available for use only at North American line voltages and frequencies, the units provide 10 minutes of backup at full load. Both the Best Power and the Elgar units feature a serial interface, and both companies can provide automatic shutdown and reboot software packages for a number of operating systems.

If experience or hard evidence suggests that your line supply is reasonably clean and if your computer isn't used for particularly critical tasks, then a simple SPStype UPS is probably all you need. In addition to protecting your computer from line-borne RFI/EMI and lightning spikes, it will provide you with enough time to end a session and save your files to disk in an orderly manner should someone inadvertently pull the plug or the line supply fail. Priced at well below

For more information . . .

For more information on the uninterruptible power supplies described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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AT&T 2 Oak Way Berkeley Heights, NJ 07922 (201) 771-2825 Circle No 701

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Exide Electronics 3301 Spring Forest Rd Raleigh, NC 27604 (919) 872-3020 FAX 919-878-1541 Circle No 705

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UPDATE

Uninterruptible power supplies

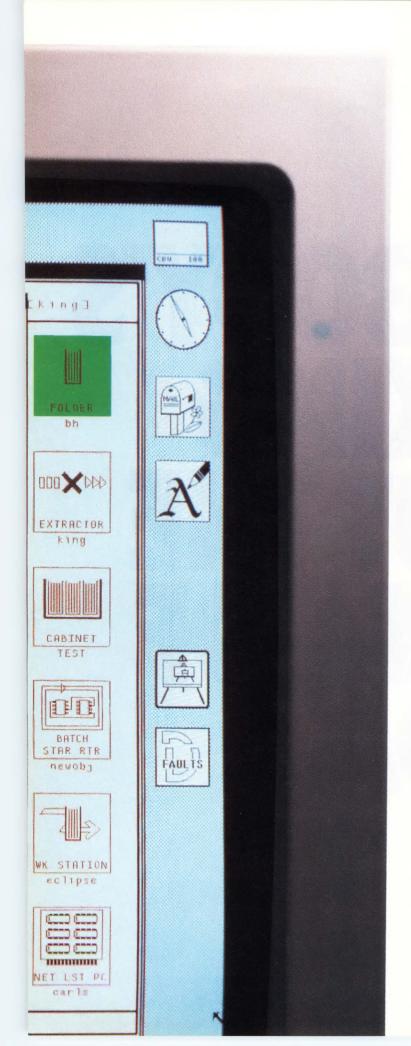
\$1000 for a model capable of supporting a PC and several peripherals, this type of UPS should be easy enough to requisition without having to go much beyond your engineering manager for authorization.

However, if you know that your line supply has problems or it is critical that your computer stay in action, you'll have to make the more difficult choice between a ferroresonant-transformer-based UPS and a true on-line UPS. If your computer and its peripherals are always on, then an on-line UPS will give you the peace of mind that they'll never be subjected to any linesupply disturbances unless the UPS's inverter fails—be sure to get an MTBF figure from the manufacturer. Alternatively, you may be forced to rely on an on-line UPS's static bypass switch if you have several independently switched loads, each with a high inrush current requirement, connected to a single unit.

Because a UPS contains a good deal of copper and iron and a leadacid battery, its shipping costs tend to be high. Although these costs have discouraged UPS manufacturers from serving international markets in the past, recent dollar exchange rates have allowed many US manufacturers to actively compete with indigenous European suppliers, such as Claude Lyons Ltd (Hoddesdon, UK), Dowty Power Conversion Ltd (Salisbury, UK), Fiskars Electronics Ltd (Wokingham, UK), and Merlin Gerin (Grenoble Cedex, France). However, the strong European currencies make it difficult for European suppliers to compete in the US market unless they're prepared to set up local manufacturing and support facilities. EDN

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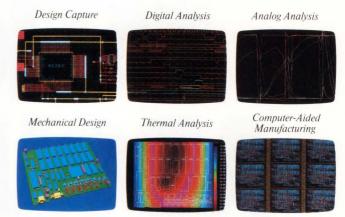
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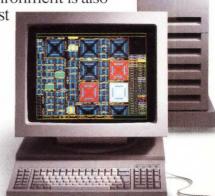
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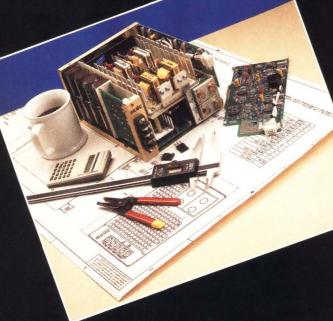




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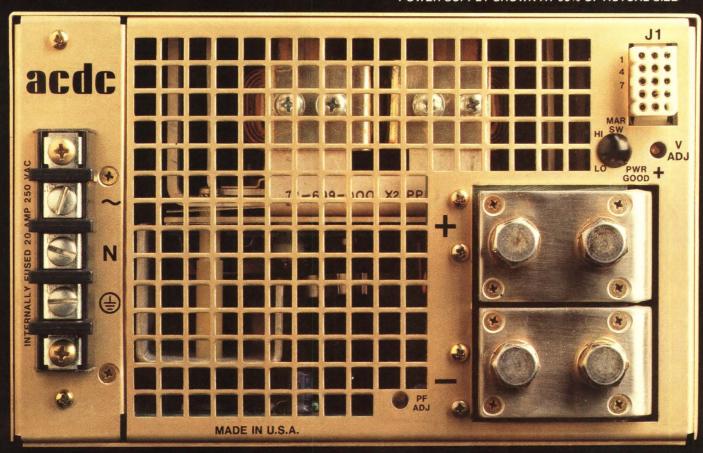
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Flash ADCs push speed and bandwidth limits



To evaluate the performance of ultrafast converters, you need to read between the datasheet lines.

Anne Watson Swager, Associate Editor he newest high-speed flash A/D converters continue to extend the sampling rate and bandwidth limits. These 6-and 8-bit converters feature sampling rates from 100M to as fast as 500M samples/sec and offer high input bandwidths, low input capacitance, and few output code errors.

If your application demands such high sampling rates, give these devices a good look. However, allow yourself plenty of time to review the A/D converters and their options. Designing a data-acquisition system with high-speed converters is extremely difficult, and your work begins with the selection process.

When evaluating the various devices, you have to weigh huge price and performance tradeoffs and make decisions about the necessity of certain external components, such as track-and-hold (T/H) amplifiers and buffer amplifiers. Furthermore, you need to make sure

that your choice is based on an ADC's true performance and not on misinterpreted specs. Evaluating the data sheets requires some expertise because manufacturers use different definitions and test methods to describe each device's performance. Therefore, you must dig beneath the surface of the data sheets to get the information you need to evaluate and compare the ADCs fairly.

To select an ADC that suits your application, you must consider the potential design difficulties associated with high-speed data-acquisition systems (Fig 1). At each stage in the conversion process there is the potential for speed-related errors. At the analog input, for example, drive requirements must be met, and at the digital output, metastable states and false output codes must be prevented.

Depending on your application, the importance of each high-speed effect shown in Fig 1 varies. If you're design-

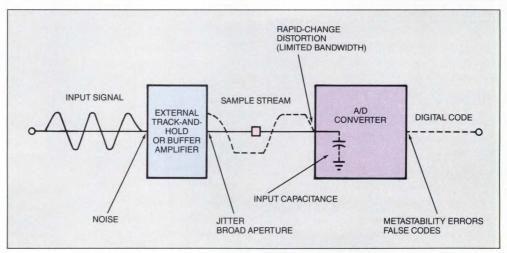
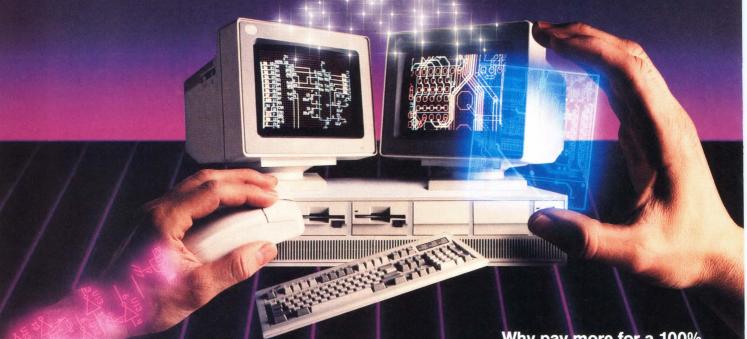


Fig 1—Minimize the hazards of data-acquisition-system design by selecting the right high-speed A/D converter for your application.

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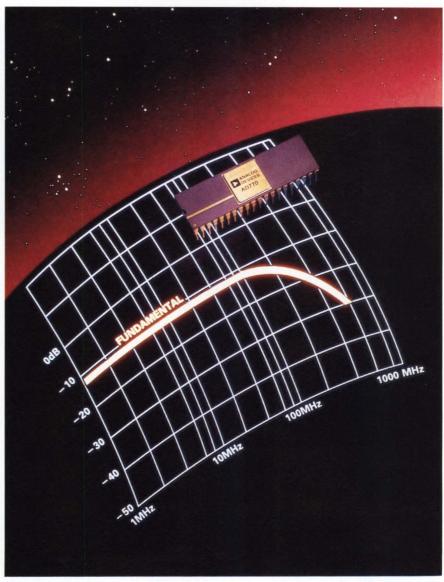
ing a system for time-domain applications, such as digital oscilloscopes, you should be particularly concerned with bandwidth and error rate. Error rate refers to the possible metastable and false code errors due to propagation and timing delays in the chip. If you work primarily with the converter in frequency-domain applications, such as digital signal processing, you also must be concerned with bandwidth. In addition, you need to examine other dynamic specs, including harmonic distortion and the signal-tonoise ratio (SNR), often expressed in terms of effective number of bits.

Three manufacturers stand out as the front runners in the high-speed-converter market. Analog Devices, Sony, and Tektronix each released ultrafast A/D converters within the last two years. Tektronix's presence in this market might surprise you—the company is more known for its test instruments. However, Tektronix recently began offering off-the-shelf converters from its Integrated Circuits Operations Division.

New designs, faster rates

Flash ADC manufacturers attribute the speed and performance improvements to their enhanced bipolar fabrication processes and IC design techniques. The vendors are also implementing their own design approaches. For example, in an effort to provide a complete solution for data-acquisition designers, Tektronix developed the first ultrafast A/D converter with an on-chip T/H amp (Fig 2). As a result of this design, Tektronix's ADCs have the highest combination of sampling rate and bandwidth currently available.

All the converters presented in **Table 1** share the same basic flash architecture: a bank of at least $2^{N}-1$ comparators, priority encoding logic, and output latches. In



The AD770 is an 8-bit flash ADC offered by Analog Devices. It provides 200M samples/sec with a full-power bandwidth of 250 MHz and a small-signal bandwidth of 400 MHz.

most cases, the inputs and outputs are ECL compatible, though the AD9012 provides TTL-compatible outputs. Some provide output-format controls that let you stack two devices to achieve 9-bit resolution. Many of the ADCs also feature underrange and overrange outputs, demultiplexed outputs, and selectable output-data formats, which include true- or inverse-binary and offset two's-complement formats.

A cursory glance at the numbers in **Table 1** reveals impressive per-

formance data. The question that you as a skeptical ADC user must invariably ask is whether these specs can be taken at face value. The answer is yes, once you completely understand the manufacturers' test conditions and definitions of the specs. In some cases, the definitions are printed on the data sheet. In other cases, numbers may appear without any explanation of how the manufacturer arrived at the results.

To evaluate a device and get an

Flash A/D converters

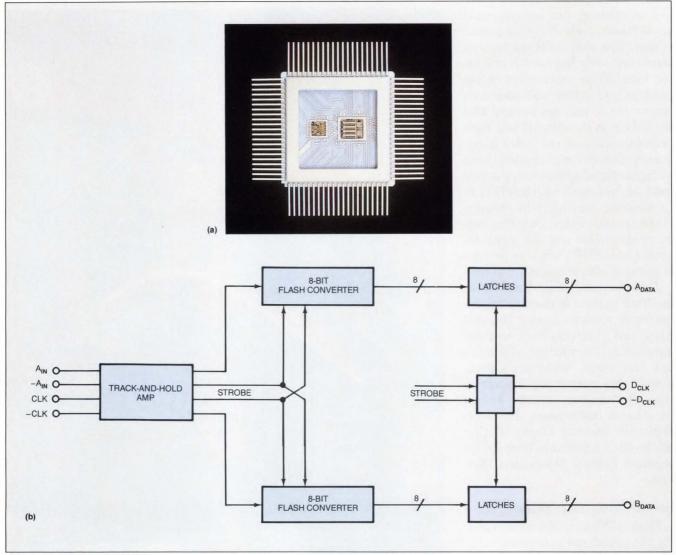


Fig 2—The Tektronix TKAD10C is a hybrid ADC that includes a monolithic T/H amp and a monolithic-converter section (a); the converter section consists of two flash converters (b). Each converter is triggered from opposite phases of the sampling clock pulse. This "ping-ponging" action doubles the effective sampling rate, allowing the TKAD10C to achieve a rate of 500M samples/sec with an internal clock speed of 250M samples/sec.

idea of how it will perform in your application, you need to know the conditions under which the manufacturer tested the converter. Failing to note the test conditions yields device comparisons that are meaningless or, even worse, highly misleading. You should never assume that a device was tested at its most extreme performance levels, and you should be prepared to make some phone calls to get the performance data you need.

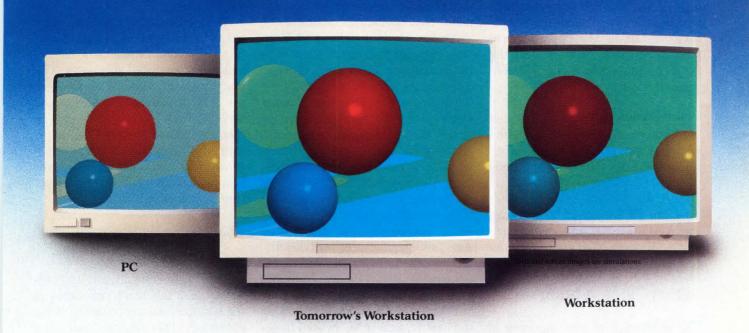
To understand how nonstandard

test conditions can affect your performance evaluation, consider an ADC's effective number of bits (ENOB). ENOB (sometimes simply called "effective bits") is a new way of describing A/D converters. This spec has become more popular among designers because it is a single number that you can use to determine a converter's dynamic error.

The general definition of ENOB is fairly consistent from manufacturer to manufacturer. You can

think of ENOB as an indication of dynamic accuracy or as accuracy in the ac sense. The definition is based on the fact that every A/D converter has a certain amount of quantization error associated with the digitization process. ENOB equates the performance of the device under test (DUT) to a lower-resolution converter that has a calculated ideal quantization error equal to the real measured error of the DUT. More specifically, ENOB is the number of bits of an ideal but

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Flash A/D converters

lower-resolution A/D converter that has the same signal-to-error ratio as the DUT. Analog Devices refers to ENOB as "the ratio of the signal to total error of the A/D converter."

Test methods vary

Although the three manufacturers agree quite closely on the definition of ENOB, the test methods they use to determine ENOB differ. To test the AD770, Analog Devices uses the FFT method to measure the AD770's SNR and then translate SNR into ENOB with the equation:

 $ENOB = (SNR - 1.76 dB) \div 6.02.$

The derivation of this equation is based on a full-scale sine-wave input; thus, the equation applies only under that operating condition.

Analog Devices defines SNR as "the ratio of the signal amplitude to the rms sum of all other spectral components, including harmonics." According to this definition, Analog Devices' ENOB measurement includes all device nonlinearities, aperture error and jitter, and distortion effects caused by slew-rate limiting. Because ENOB and SNR are so tightly linked, you must note each manufacturer's definition of SNR. Specifically, you must make sure the manufacturer includes distortion effects in its measurement. Otherwise, your device comparisons won't be accurate.

Tektronix uses what's known as the best-fit sine-wave method to determine the ENOB of the TKAD10C and TKAD20C. This method compares the converter's output (based on an antialiasing-filtered analog input) to a mathematically generated sine wave. The mathematical model's parameters are adjusted until a best-fit sine wave is found. This sine wave is then subtracted from the digital record; the remainder is the residual error. The rms value of this error is applied to the following equation, from which ENOB is calculated:

ENOB = N - log 2(measured rms error \div ideal rms error),

where N is the resolution of the converter and the ideal rms error is the quantization error for the N bit converter. This equation considers only the noise—it doesn't depend on

TABLE 1—DYNAMIC SPECS OF HIGH-SPEED FLASH A/D CONVERTERS

MANUFACTURER AND MODEL	RESOLUTION	SAMPLING RATE (MSPS)	INPUT BANDWIDTH ¹ (MHz)	EFFECTIVE BITS ²	CAPACITANCE (pF)	POWER DISSIPATION (W)	INPUT-VOLTAGE RANGE	
ANALOG DEVICES COMPUTER LABS DIV AD9002	8	150	160	5.5 (CALCULATED FROM SNR AT A _{IN} =40 MHz)	17 (TYP)	0.75	0 TO -2	
AD9012	8	100	180	6.4 (CALCULATED FROM SNR AT A _{IN} =20 MHz)	16 (TYP)	1.0	0 TO -2	
AD9006/16	6	500	550 (INPUT SCALE NOT SPECIFIED)	4.8	8 (TYP)	<2.0	± 1.0	
SEMICONDUCTOR DIV AD770	8	200	250 400 (SMALL SIGNAL)	3.9	19 (TYP)	1.7	± 2V	
CXA1076K	8	200	150	4	25 (TYP)	0.72	0 TO -2	
CXA1176K	8	300	180	4.4 (A _{IN} =120 MHz)	25 (TYP)	1.3	0 TO -2	
TEKTRONIX TKAD10C	8	500	1200	7.0	1 (CALCU- LATED)	7.5	± 0.27	
TKAD20C	8	250	1200	6.8	3 (CALCU- LATED)	5.0	± 0.27	

NOTES

1. FPBW UNLESS OTHERWISE SPECIFIED.

^{2.} MEASURED AT FULL SCALE AND AT NYQUIST FREQUENCY UNLESS OTHERWISE SPECIFIED.

the amplitude or shape of the input signal.

According to Tektronix, the sources of error that influence the company's ENOB measurement include all dc and ac nonlinearities, clock and aperture jitter, missing output codes, and noise. The curves in the TKAD20C data sheet show that even down near dc, the ADC won't have more than $7\frac{1}{2}$ effective bits because the device's differential linearity error is $\pm \frac{1}{2}$ LSB.

Be aware of test conditions

Clearly, Tektronix and Analog Devices use different methods to determine ENOB. However, both methods will yield comparable results if the manufacturers test the devices under specific conditions. Three test conditions determine ENOB: sampling rate, analog input frequency, and analog input level.

The FFT method that manufacturers use to calculate ENOB relies on the signal-to-noise ratio and thus depends directly on input amplitude. The sine-wave method, on the other hand, relies on noise; the measurement isn't directly affected by the input amplitude. Chris Manglesdorf of Analog Devices says that if you don't compare measurements taken at full scale, the company's test is at a disadvantage and the results may make other converters look better. Therefore, you must be sure that the test conditions are equivalent for all the ADCs you compare: The measurement should be made at the device's maximum sampling rate, the peakto-peak value of the ac input signal

should approximately equal the converter's full-scale range, and the input signal's frequency should be close to the ADC's Nyquist frequency. The numbers resulting from tests with these parameters represent the worst-case performance of the A/D converter.

Sony uses the FFT method to determine ENOB. The company's data sheets provide curves showing ENOB vs frequency (Fig 3). These curves illustrate the impact that input voltage level has on ENOB; note the improvement in ENOB as $V_{\rm IN}$ decreases.

Like ENOB, the input-bandwidth specification can be specified at full-scale inputs or at inputs less than full scale. Some manufacturers quote bandwidth for both conditions (note the AD770 in Table 1). No industry-standard definition exists, but full-power bandwidth is generally defined as the input frequency at which the amplitude of the reconstructed output signal is reduced by 3 dB for a full-scale input. Thus, the full-power bandwidth spec represents a worst-case value. Again, check the sampling rate at which the manufacturer ran the test.

You can use the bandwidth spec to get a general idea of an ADC's dynamic performance at its Nyquist frequency. That is, the higher the bandwidth in relation to the sampling rate of the converter (and thus the Nyquist rate), the lower the loss in gain (SNR) and the lower the distortion at the Nyquist rate.

Undersampling made easy

You can see from Table 1 that some converters have input bandwidths significantly higher than their Nyquist frequencies. An extremely high bandwidth lets you use a technique called undersampling to perform conversion and demodulation in one step. Undersampling is the intentional use of aliasing to convert to carrier or in-

POWER SUPPLY (V)	PACKAGE	PRICE	COMMENTS
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5, -5.2	40-PIN DIP	\$175 (100)	UNIPOLAR AND BIPOLAR INPUT RANGE, OVERFLOW AND UNDERFLOW SIGNALS
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-5.2V	68-PIN LCC	\$490 (1-9)	SAME AS CXA1076K
5, -5.2	84-PIN STRIP LINE	\$2500 (1-9)	INTERNAL T/H AMP, INTERNAL 50Ω TERMINATION, TIME-INTERLEAVED OUTPUT DATA PATHS
5, -5.2	84-PIN STRIP LINE	\$850 (1-9)	INTERNAL T/H AMP, INTERNAL 50Ω TERMINATION

Flash A/D converters

termediate frequencies. To perform undersampling, you must use a converter that has an input bandwidth higher than its Nyquist rate.

Some manufacturers print bandwidth specifications on the data sheet to assist you in performing undersampling. Under the large-signal bandwidth spec of 180 MHz, for example, the AD9012's data sheet states that the bandwidth is intended for undersampled applications and not for Nyquist operation.

The bandwidth specification can be somewhat misleading when interpreted as a stand-alone number; you must use it in conjunction with ENOB to get a better overall picture of an ADC's performance. For example, note from Table 1 that the AD770 has a full-power bandwidth of 250 MHz, which is much higher than the device's Nyquist frequency. Also note that at the Nyquist frequency, ENOB is 3.9. You might ask why anyone would run an input signal through this device when the ac accuracy would be less than 4 bits. The answer lies in the application: If you're performing spectrum analysis, you may not be as concerned with accuracy as

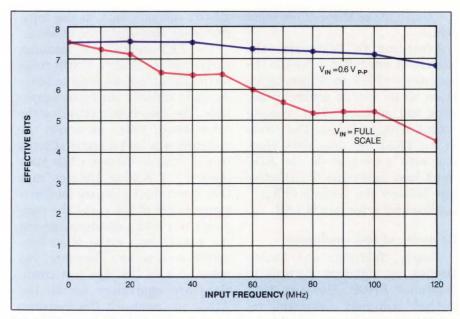


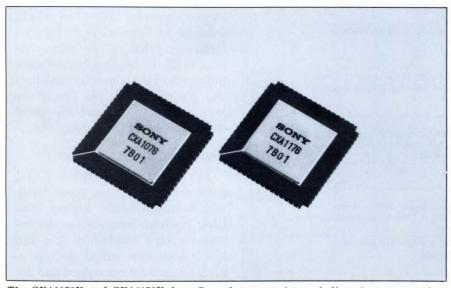
Fig 3—Be sure to check the data sheet for the conditions under which ENOB is determined. This curve for the Sony CXA1176K converter shows the dramatic difference between full-scale effective-bit measurements and those made at less than full scale.

you are with the ability to resolve certain spectral components—even if the peaks are 35-dB down.

Closely coupled to the interpretation of the bandwidth spec is the issue of whether or not to use an external T/H amp; the higher the converter's bandwidth, the less stringent your T/H needs will be. The kind of dynamic accuracy your application requires determines if you need a T/H amp. When evaluating external T/H requirements, you must consider the aperture width, aperture jitter, and slew rate of the input signal. Aperture jitter is the uncertainty in the input sampling time. The aperture-jitter spec isn't included in Table 1 because the ENOB spec takes the effects of aperture jitter into account. Also, manufacturers claim that the frequency-limiting effects caused by aperture jitter are overshadowed by other dynamic effects.

In some cases, the performance of high-speed A/D converters may allow you to get by without a T/H amp. Some data sheets state that the device's wide bandwidth allows you to acquire high-speed pulse inputs without an external T/H amp.

Considering the high speeds that the ADCs exhibit, designing a T/H amp that is compatible with your ADC can be difficult. Matching the characteristics of the T/H amp to the A/D converter presents another design challenge. To lessen the ex-



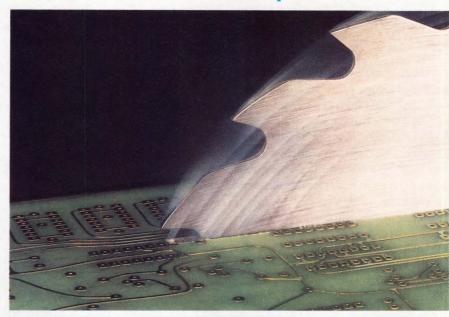
The CXA1076K and CXA1176K from Sony feature an internal, linearity-compensation circuit, an overrange output, and two digital inputs that enable you to select output formats, including true- or inverse-binary and offset two's-complement formats.

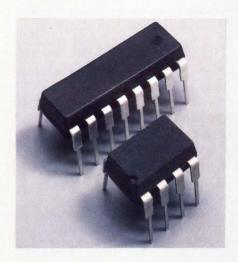
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Type: Darlington	or the second se					
400 (TYP) (2) 400 (2) 400 (3) 800 800	IL30/HIIB3 IL31/HIIB2 IL55 4N32 4N33	ILD30 ILD31 ILD55 ILD32 ILD33	ILQ30 ILQ31 ILQ55 ILQ32 ILQ33			

Footnotes: (1) bidirectional input; (2) BV_{CEO} = 30V; (3) BV_{CEO} = 55V

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Flash A/D converters

tra work needed to design a T/H amp, Tektronix includes an internal, on-chip T/H amp. The high cost of both the TKAD10C and TKAD20C is mainly due to this added feature; the cost of the TKAD10C also reflects the complexity of the device's dual flash-converter design.

It's unclear whether other manufacturers will follow Tektronix by including on-chip T/H amps. Because of the high price and the power demands associated with on-chip T/H amps, some manufacturers bet that A/D-converter customers will opt to continue using their own T/H designs. Even with the increased engineering time, designing your own T/H amp may be less expensive. Other manufacturers recommend that you try to use a device that doesn't need a T/H amp.

The drive requirements of a converter, manifested primarily in the input capacitance, also affect the conversion bandwidth. Thus, in addition to deciding whether you need

an external T/H amp, you must decide if you need a buffer amplifier. In general, most manufacturers recommend that you use a buffer amp.

You can quantify the lowpass-filtering effect of the input capacitance simply by calculating the cutoff frequency. This calculation depends on the configuration of the termination. Most of the flash converters shown in **Table 1** are driven from 50Ω sources and require 50Ω terminations. This termination resistor is in parallel with the converter's input capacitance. In most cases, you need to provide the external termination. The TKAD10C and TKAD20C, however, include the termination on the ADC.

The data sheet for the AD770 includes some recommended passive terminations and their corresponding -3-dB frequencies. According to Analog Devices, you can use the passive terminations and achieve the same performance that a buffer amplifier affords.

When deciding whether or not to

use a buffer amplifier, you should know that the input capacitance may exhibit nonlinear characteristics. As the input changes voltage levels, the capacitance at the base-emitter junction of the input transistors also changes. Many data sheets illustrate these characteristics with curves showing the capacitance vs the input voltage. Because you can't minimize the nonlinearities, make sure the ADC designers took precautions to prevent any negative effects.

The final factor that you must consider in the conversion process is the error rate of the converter. Internal signal delays cause each comparator to sample the input data at slightly different times. As a result, an individual comparator may produce a false output. This error in the thermometer code—named for the comparator outputs that look like a thermometer whose level is moving up and down—can cause an error in the encoding logic. The result is a false output code.

IEEE takes step toward spec standardization

The difficulty of sorting through ADC specifications has become an industry-wide topic of discussion. In recent years, much has changed and much hasn't with regard to this topic. What has changed is that you've had the opportunity to digest article after article published in the trade press on the subject of spec interpretation; this extensive coverage should tell you a lot about the clarity of the subject. Fortunately, these articles have increased awareness of the specs' subtleties, enabling engineers to evaluate ADC performance on a more sophisticated level.

What hasn't changed is the data sheets themselves. They are just as confusing as ever; they don't always lead you down a clear path of performance evaluation. However, help may be on the way. The Waveform Measurements and Analysis Committee of the IEEE Instrumentation and Measurement Society is close to submitting standard number P1057 for final approval—a trial standard for digitizing waveform recorders. The standard deals with A/D converter specifications, and it addresses definitions and testing parameters. If you're interested in an advanced copy, or if you're involved with ADC design and you have an interest in serving on a committee to develop a new standard written exclusively for A/D converters, contact Thomas Souders at the National Institute of Standards and Technology (formerly the National Bureau of Standards). You can contact him at B162MET, Gaithersburg, MD 20899, phone (301) 975-2406.

If the IEEE standard causes manufacturers to agree on test procedures and specification definitions, in the future you may be able to read ADC data sheets and get complete and useful information without additional effort.

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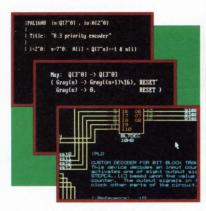
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Flash A/D converters

The extent to which manufacturers can reduce output errors is difficult to quantify and test; specific numbers don't often appear on data sheets. Tektronix does quote an error rate of less than 10^{-15} and states that it has reduced the magnitude of this error to less than 1 LSB in both the TKAD10C and TKAD20C. The other manufacturers generally don't quote an error rate. They simply use design techniques to minimize metastable-state-induced errors. For example, Sony uses errorsuppression circuitry, and Analog Devices uses a proprietary errorcorrecting scheme.

Once you select an A/D converter, testing it in your own system answers the ultimate performance-related questions that you can't resolve by looking at a data

sheet. To make your final evaluation as simple as possible, each manufacturer offers evaluation boards. The boards help you avoid mistakes in circuit layout and interfacing that could obscure the true performance of the ADC.

These boards include most of the necessary circuitry for driving the A/D converter, including reference generators, data latches, and output buffers. Some also include onboard reconstruction DACs, so you can directly compare your analog input with the analog output. You should check the board's data sheet to see the exact circuitry included in its evaluation board.

The ADEB770 evaluation board for the AD770, which sells for \$635, lets you enter your analog data through either a direct input or a buffered input. The Computer Labs Division of Analog Devices sells boards for the AD9002/12 and the AD9006/16 for \$300 and \$450, respectively. Tektronix offers the TKAD20EB1 evaluation board for \$950. This board includes connectors that are compatible with the company's digital-acquistion-system instruments. Tektronix also offers a similar version for the TKAD10C converter. Sonv's evaluation boards for the CXA1076 and CXA1176 are priced at \$690 and \$850. They don't include reconstruction DACs. Note that the above prices may not include the price of the A/D converter itself.

If you want to make more of an investment in converter testing, consider Tektronix's PTS101 ADC characterization test system. This

This is how others see LCDs.



PC-based tester provides dynamic testing and characterization of ADCs that are located either on an evaluation board or in the final system configuration. Proprietary soft-

ware lets you conduct a variety of tests: effective bits and ENOB vs frequency, FFT, SNR, histograms, and transfer-curve generation. The basic model of the test system, which sells for \$18,950, works with sampling rates as fast as 20M samples/sec. You can upgrade the PTS101 to test converters at rates as high as 300M samples/sec. The PTS101H upgrade demands additional hardware: a signal generator, a filtering system, and a Tektronix DAS 9129 digital-analysis unit. The entire package costs around \$60,000.

For more information . . .

For more information on the A/D converters discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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EDN May 25, 1989

CIRCLE NO 62

107

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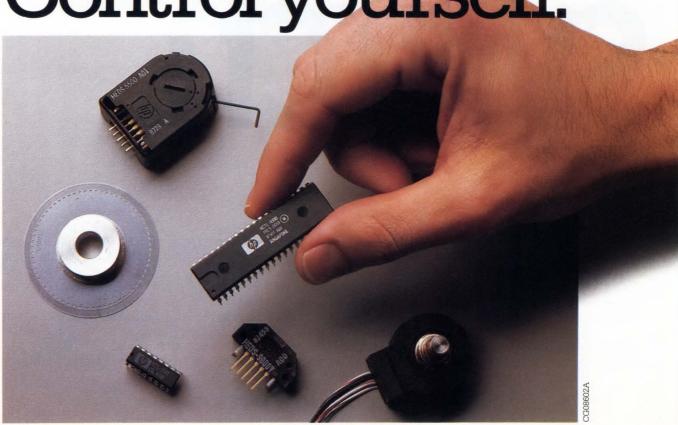
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PACKARD

CIRCLE NO 63

A/D converter uses sigma-delta modulation to resolve 16 bits at 100 kHz

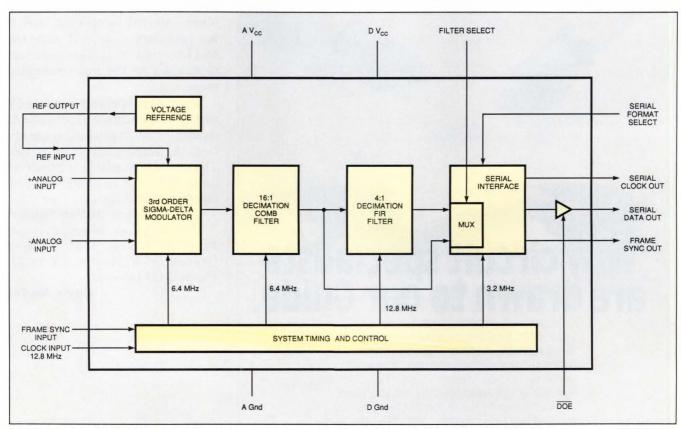
The DSP56ADC16 100-kHz 16-bit A/D converter implements sigmadelta modulation technology on a single chip. The sigma-delta conversion technique's inherent filtering eliminates the need for external filtering. This conversion process also has inherent oversampling and noise-shaping capabilities, which enable the converter to exhibit 90dB signal-to-noise and signal-to-THD ratios for input signals from 0 to 45.5 kHz, with an in-band ripple of less than 0.001 dB. In addition to the 16-bit output, the 56ADC's architecture lets you select an intermediate filter output to

obtain 12 bits of resolution at 400 kHz.

The sigma-delta conversion technique is based on quantization-noise-shaping and digital-filtering techniques and is vastly different from the familiar flash or successive-approximation approaches. The 56ADC's conversion process involves two basic steps: a 1-bit quantization and noise-shaping stage, and a digital lowpass-filtering stage. A 1-bit quantization may sound strange, but by sampling the input signal at a very high rate, the large amount of quantization noise that results from this 1-bit conver-

sion is spread over a large spectral area. Subsequent shaping of this noise pushes it into a higher frequency band so that lowpass filters can remove it altogether.

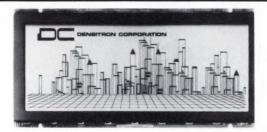
In order to spread the quantization noise over a broad spectrum, the 56ADC oversamples the incoming data at 64 times the output sampling rate, or 6.4M samples/sec. A third-order modulator then shapes the spectral weighting of the noise so that it is pushed to the higher end of the frequency spectrum. The third-order noise-shaping curve and its associated 18 dB/octave slope ensure that very little of the noise



The first step of the 56ADC's conversion process takes place in the sigma-delta modulator. The modulator block oversamples the incoming data and shapes the quantization noise so that it is pushed into a higher frequency band. The second step of the conversion removes the noise in two stages of digital filtering.

EDN May 25, 1989

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UPDATE

power remains in the passband.

The 56ADC implements the digital lowpass filters in two stages; a comb filter performs 16:1 decimation on the modulator output, and a FIR filter performs 4:1 decimation on the comb-filter output. You can connect the output of either of these two filters to the 56ADC's serial output to achieve a 16-bit 100-kHz output or a 12-bit 400-kHz output.

The advantages of this converter over other converter types are in the areas of performance and external circuitry requirements. Because of the internal lowpass filters, a front-end antialiasing filter-normally an eighth- or ninth-order elliptic filter-is no longer necessary. You can think of the digital filters as back-end filters. Because this filtering is implemented digitally in the 56ADC, the phase linearity is more tightly controlled than it is with elliptic filters. Another external component that is not necessary is an S/H amp; the 56ADC uses switched-capacitor techniques in the input sampling stage.

The 56ADC operates from one 5V supply, and nominally draws 30mA. Available now in production quantities, the single-piece price is \$50. The device is available in 20-pin ceramic DIPs and in plastic and surface-mount packages.

-Anne Watson Swager

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 440-2039.

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CXX5464AJ	16K x 4	25/30/35	SOJ 300 mil						
CXX5465P*	16K x 4	25/30/35	DIP 300 mil						
CXX5465J*	16K x 4	25/30/35	SOJ 300 mil						
CXX5164P	64K x 1	25/30/35	DIP 300 mil						
CXX5164J	64K x 1	25/30/35	SOJ 300 mil						
CXX5971P	8K x 9	25/30/35	DIP 300 mil						
CXX5971J	8K x 9	25/30/35	SOJ 300 mil						
CXX58255AP	32K x 8	25/30	DIP 300 mil						
CXX58255AJ	32K x 8	25/30	SOJ 300 mil						
CXX58258P	32K x 8	35/45	DIP 600 mil						
CXX58258SP	32K x 8	35/45	DIP 300 mil						
CXX54256P	64K x 4	35/45/55	DIP 300 mil						
CXX51256P	256K x 1	35/45/55	DIP 300 mil						
*0/E									

Complete 10-µsec CMOS 12-bit ADCs include fast track-and-hold amplifier

It is much easier to use an A/D converter (ADC) when all the required circuit functions are included in a single package. The MAX163, MAX164, and MAX167 are complete 10-µsec CMOS 12-bit ADCs. The chips include everything except some external decoupling capacitors. All three ADCs include a successive-approximation 12-bit converter, a track-and-hold (T/H) amplifier, a buried-zener voltage reference, a 16- or 8-bit µP interface, and a crystal or an external clock-driven oscillator.

Often, internal T/H amplifiers are slew-rate limited, thus limiting the input signal to a frequency that can be much less than the sample rate. In the sample mode, the full-power bandwidth of the T/H amplifier within the MAX163/164/167 ADCs is typically 6 MHz. Such a wide bandwidth allows you to use these ADCs for undersampling applications where you can convert a band-limited signal at a higher frequency than the sample rate.

The wide-input bandwidth is advantageous even if you're not planning on undersampling. It's best to have an external antialiasing filter as the only filter to affect the input signal. If the input bandwidth of the ADCs is low, it may affect the signal and therefore the accuracy of the conversion. Because the input bandwidth of these ADCs is more than 10 times the sample rate, you can be sure that the input section will not cause any frequency roll-off of the signal you're converting.

Aperture jitter is another problem that can limit the maximum frequency at which the system can accurately convert. The MAX163/164/ 167 ADCs have an aperture jitter of less than 100 psec. This parame-

AGND TRACK/HOLD 12-BIT DAC SUCCESSIVE-APPROXIMATION REGISTER REFERENCE 12-BIT LATCH 21 CONTROL CS 20 RD MULTIPLEXER CLK OUT 17 CLK IN

The track-and-hold amplifier built into these ADCs has a bandwidth of 6 MHz. The only external components required to use these 10-usec ADCs are a few decoupling capacitors.

ter allows accurate conversion of 12 bits at a rate as high as 777 kHz, more than seven times the 100-kHz-max sample rate.

The three different versions of the ADC differ only in the input range. The MAX163 accepts 0 to 5V inputs, and the MAX164 and MAX167 accept -5 to +5V and -2.5 to +2.5V inputs, respec-

tively. The ADCs are powered by 5 and -12 or -15V, consume a maximum of 180 mW, and are packaged in a 24-pin 300-mil DIP. \$21.25 (100). —*EDN Staff*

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 732

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Electronic log and sensor automate record maintenance

If you need to consider periodic maintenance when designing a piece of equipment, you may want to consider adding a Sensor Tag System to your parts list. You can tap the sensors of each Sensor Tag into your equipment's pulse-input signal lines to record such data as hours of use, power applications, distance traveled, or frequency of occurrences. Each Sensor Tag includes at least 2k bytes of EEPROM and an 8-bit µP housed in a standard connector shell that you can permanently affix to your equipment.

To read the data stored in a Sensor Tag, a maintenance person merely needs to unscrew the hermetically sealed connector cap and plug in a handheld computer with a 32-character LCD. This ruggedized computer also has an 8-bit μP , a minimum of 32k bytes of RAM (expandable to 128k bytes), and 32k bytes of burned-in ROM containing system software.

The computer operates from 6 to 8 hours on rechargeable batteries. You can connect this handheld unit to another computer or modem via its built-in RS-232C port. The unit's Centronix-compatible parallel port lets you hook the computer to a printer or larger display. You can also use the computer to read, write, and instruct the manufacturer's Memocard smart cards. These credit-card-size Memocards also contain 2k or 8k bytes of EEPROM and an 8-bit μP.

Pricing for the Sensor Tags starts at \$34 (OEM atv), and the handheld computers sell for \$900. The computers come with system software, cables, power supply, and a 1-year warranty.—J D Mosley

Multimil Inc, 670 International Parkway, Richardson, TX 75081. Phone (214) 644-7724. FAX 214-644-7770.

Circle No 733



Designed to simplify record keeping for equipment that requires periodic maintenance, Multimil's Sensor Tag System lets you download data stored in connector sites on the equipment into a handheld portable computer with an 8-bit μP .

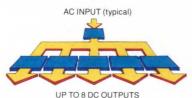


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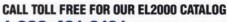
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Instruments combine 4-quadrant source, electrometer, and multifunction meter

Keithley Instruments is well known among materials researchers and engineers who monitor semiconductor manufacturing processes. These were the people Keithley's engineers originally had in mind when they conceived the Model 236 and Model 237 source/measurement units. As the products developed, however, the company recognized that there was another, even larger market: most engineers who design equipment to test electronic products can also use an instrument that simultaneously acts as a DMM and a power supply capable of sourcing or sinking voltage or current (a socalled 4-quadrant supply). To make the instruments useful in still more applications, Keithley's engineers provided well-thought-out frontpanel and IEEE-488 programming capabilities that enable the units to generate arbitrary waveforms as well.

The new instruments provide an impressive combination of capabilities in small and attractively priced packages. You can use them on a benchtop or mount them in an equipment rack; they are just 3½in. high. Almost from its inception, Keithley's forte has been low-current measurements, so each unit features, in addition to the usual DMM functions, an electrometer capable of measuring currents as small as 10 fA. The units can force currents as small as 100 fA. Voltage-measurement resolution is 10 μV, voltage-forcing resolution is 100 µV, and basic accuracy is 0.03% of reading. To reduce noise, the units permit guarded 4-terminal operation and can both integrate and average measurements. To find small deviations about a large value, the units suppress (automati-



Combining a 4-quadrant V/I source with an electrometer and a DMM in a 3½-in.-high single-channel package, Keithley's Model 236 and Model 237 source/measurement units are fully programmable via IEEE-488. They provide an economical solution to many test problems.

cally subtract) offsets as large as 1100V or 110 mA.

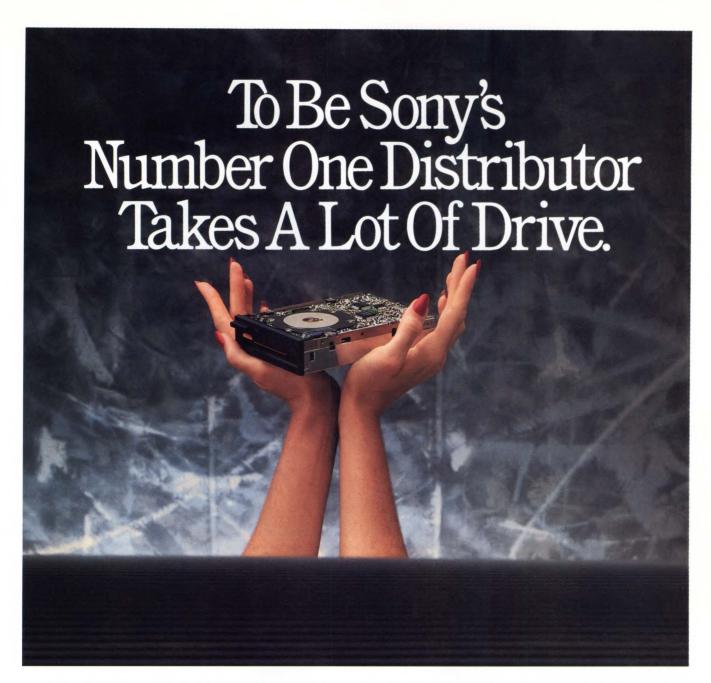
Frequently, instruments that offer low-level measurement capability sacrifice speed of operation. The 236 and 237 force no such compromises. These units can acquire 1000 values/sec and store them in an internal memory. You can then empty the memory via IEEE-488 at a rate of 125 measurements/sec. Similarly, you can update the source output from the internal memory at 1000 points/sec. Source settling time is 500 µsec, and the units' outputs are transient free when you turn power on or off.

Unlike competitive units, some of which are packaged as modules that slip into expensive mainframes, the 236 and 237 are complete, standalone instruments. The company claims that this packaging approach is cost effective regardless of the

number of channels you need and is particularly effective if you need fewer than four channels—a common situation. The 237 costs \$6200; the 236, which is similar but has a 110V-max voltage-forcing capability (as opposed to the 237's 1100V), costs \$4900.—Dan Strassberg

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. (800) 552-1115; in OH, (216) 248-0400. TLX 985469.

Circle No 730



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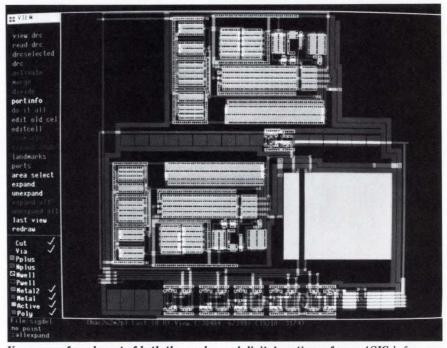
PRODUCT UPDATE

CAE tool automates composition of mixed-signal ASIC chip

ChipCrafter release 2.0 features an option that allows you to perform automated physical design on circuits that contain a combination of analog and digital functions. Typically, mixed-signal ASICs have been custom-design tasks that the ASIC vendor performed to your specification, a process that often bogged down the design schedule. ChipCrafter/MAX (Mixed ASIC eXpert) is a \$29,000 option to the \$49,000 base software that speeds the layout process of mixed-signal circuits and runs on Mentor/Apollo and Valid/Sun workstations.

The vendor estimates that the cost of vendor-provided placement and routing for a mixed-signal ASIC exceeds \$1 per gate. It could take a month or more to complete the iterative process of sending the ASIC vendor your net list, having the vendor place-and-route and back annotate your circuit models, and sending the net list back to you so you can resimulate. By performing these operations yourself, you can reduce both the time and the expense of designing mixed-signal ASICs.

The place-and-route tool, Analog/ APAR +, can lay out the entire chip or work hierarchically on subsections. The software isolates analog from digital circuitry, dividing the analog portions into macroblocks and providing separate power supplies when necessary. Inside the analog blocks, Analog/APAR + differentiates between digital, neutral, high-sensitivity, and lowsensitivity nets; separates them to control crosstalk; and minimizes net length for high-sensitivity analog nets. The software automatically sizes the power rails by using feedback on power requirements from the design. A similar feedback



You can perform layout of both the analog and digital portions of your ASIC before you ship the design off for prototyping. ChipCrafter sizes power rails and the digital cell's output buffers to maximize circuit and silicon efficiency.

mechanism provides information that allows the software to size the output buffers of the digital cells. Analog/APAR + currently supports only one layer of polysilicon; a 2-layer polysilicon version that supports custom switched-capacitor design is scheduled for release later this year.

The libraries for ChipCrafter/MAX contain common analog circuit elements like op amps, voltage references, analog switches, resistors, and capacitors from the 1.25-and 1.5-\mu CMOS processes of both U.S. and international ASIC vendors. The libraries cost \$19,000.

Additional features of ChipCrafter are library elements that allow you to build testability into your ASIC and other elements that contain configurable "soft-cores." These soft cores let you select the number of words and bits per word

for memories and choose bit widths for adders and multipliers. The software updates the simulation modules as you configure the models.

ChipCrafter also provides mixed-mode simulation capability. You can use digital simulators to model the behavior of your mixed-signal design by utilizing digital-equivalent behavioral models for all the library elements. After simulating, you can convert the results to test patterns, allowing digital testers to perform the initial screening of finished devices. A Spice simulator gives you transistor-level simulation capability for detailed analog-circuit modeling.—*Michael C Markowitz*

Seattle Silicon Corp., 3075 112th Ave NE, Bellevue, WA 98004. Phone (206) 828-4422.

Circle No 740

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EDN May 25, 1989

Winchester DISK DRIVES

Maury Wright, Regional Editor

he state-of-the-art in Winchester disk drives changes constantly, and in 1989 you have higher-capacity drives to choose from in every form factor. Several companies ship 5¹/₄-in., full-height, 760M-byte products; and two have introduced 1.2G-byte drives. Half-height, 5½-in. offerings include 380M-byte drives, and the capacities of 3½-in. drives exceed 200M bytes. You can buy a

drive with an average seek time in the 10msec range and several featuring 20M-bps data rates. Developments in drives targeted at the laptop market include a 2½-in., 40Mbyte drive and a 1-in.-high, 3½-in., 100M-byte drive. Ultimately, factors such as cost, reliability, performance, and interface should guide you to a choice among the myriad of

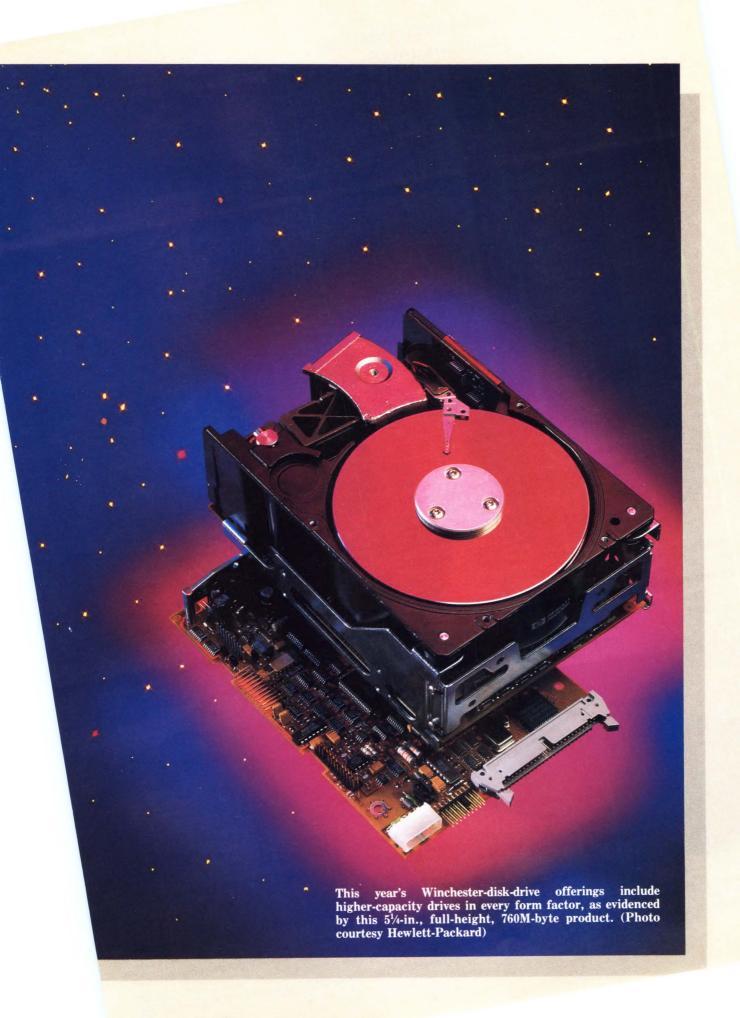
available products.

You will most likely confront one of two scenarios when considering Winchesters for a specific system application. In the first case, your application calls for or would benefit from a specific nonmainstream feature, such as power consumption of less than 1W, or a specific interface feature, such as a multisegment read-ahead cache. In this scenario, the application requirements limit your choice to drives offered by a few, or maybe even one,

vendor. You may have to evaluate the ramifications of buying from a sole source. You may also find that you can't justify paying a premium price for such a feature in your application. More Winchesters than ever before offer application-specific capabilities.

Choosing a drive for a general-purpose application—the second scenario—may try your patience more, however. As a customer you need multiple sources, and as a disk-drive customer you have many sources to choose from. Yet the standardization present in 3½-and 5¼-in. drives makes differentiating competing

As always, $3\frac{1}{2}$ and $5\frac{1}{4}$ in. Winchester manufacturers offer new drives with specs even more impressive than last year's models. These new drives feature decreased latency and faster data-transfer rates, and some manufacturers offer drives reduced in size, weight, and power.



Manufacturers of drives with embedded SCSI or AT-compatible controllers can offer value-added features, such as readahead caches and zoned-bit recording.

products difficult. For example, the products all meet standard form factors and include standard interfaces. Despite list prices, drive manufacturers price products competitively or identically to each other during OEM negotiations. And finally, most drive manufacturers competing in a given market segment typically offer drives with virtually identical storage capacity.

Consider the interfaces available for 3½- and 5¼-in. Winchesters. You can choose drives with device-level interfaces—ST-506/412 or ESDI (Enhanced Small Device Interface)—or intelligent embedded controllers—SCSI or AT compatible. Drive manufacturers have no way to add value to ST-506/412 drives and can only offer a choice of 10M-, 15M-, or 20M-bps transfer rates for ESDI drives. Manufacturers of drives that include an AT-compatible or SCSI controller can add value with features such as read-ahead caches. And the popularity of AT-compatible drives is growing fast. In fact, many new personal computers include an AT-compatible disk-controller connector on the mother board. SCSI drives represent the most popular choice for applications such as high-end PCs and workstations.

Intelligent controllers such as SCSI offer drive manufacturers the greatest leeway in adding value to their product via the interface. For example, consider a read-ahead cache. Quantum pioneered the drive-based cache and still offers the most complex and effective implementation available. Quantum's DisCache feature allows its drives to store in RAM as many as 12 different buffers of data read ahead during previous operations. Most SCSI-drive manufacturers now include cache support but typically only provide one or



The 14-msec average seek time achieved by Priam's 760M-byte ESDI (Model 676) and SCSI (Model 776) Winchesters make the drives ideal for applications such as transaction-processing systems.



A multisegment caching capability effectively reduces the average seek time by as much as 50% in Quantum's ProDrive series of 3½-in. drives, which range in capacity from 40M to 170M bytes.

two segments. This provision makes the cache less effective, especially in multiuser and multitasking applications.

Cache supports multiple segments

The Quantum drives include a 64k-byte cache, and you can optionally specify a cache expansion to 256k bytes. On host request for data present in the cache, the drive responds immediately with no seek delay. Furthermore, the drive controller can transfer data from cache memory at 4M bytes/sec rather than at the drive rate of 10M bps. The controller replaces segments based on a least-recently-used algorithm after all segments are filled. A system programmer can control cache allocation parameters, such as the number of segments allocated and the size of the segments. Quantum offers the DisCache feature on its ProDrive series of 3½-in. products with SCSI or AT-compatible interfaces. The family includes 40M- and 80M-byte products and the recently introduced Model 105S, which stores 105M bytes and costs \$1050 (2000).

Because an intelligent interface decouples the host from the heads and media, manufacturers can also use a technique called zoned-bit recording (ZBR) to increase the capacity of SCSI drives. Drives that employ ZBR store more data on the outer tracks of the drive than on the inner tracks. The concept makes perfect sense because the outer tracks obviously have larger circumferences than do the inner ones.

ZBR boosts capacity and performance

Imprimis Technology (previously Control Data's disk division) introduced the ZBR concept in 1987 and has used the technology extensively in its 5½-in. drives. Imprimis designers partition a 5½-in. drive into 19 zones. Within each zone, the tracks include a constant number of sectors. But each zone—moving from the center to the outside of the disk—includes more sectors per track than does the previous zone. This technique results in an increased data transfer rate each time the drive heads move outward to a new zone. ZBR has enabled Imprimis to offer high-capacity drives with designs less complex than those of its competitors. ZBR has also enabled the company to produce higher-capacity drives sooner than its competitors.

The large command set defined by the SCSI spec also offers drive manufacturers ways to add value. Most manufacturers include a base set of commands that comply with the CCS (Common Command Set) in SCSI-2 (for more information on SCSI-2, see the box, "Committees refine SCSI and define CAM"). But often the drive manufacturers include a proprietary set of optional commands in their SCSI implementation. You may find an optional command that fits your needs.

You only need to evaluate a few characteristics of SCSI drives for most system designs. SCSI-2 compatibility ensures that a drive meets the CCS, but non-SCSI-2 drives can also include a valid CCS implementation. In fact, a drive manufacturer can update a CCS-compliant drive to SCSI-2 compatibility with a simple firmware change. A SCSI-2 drive can also include advanced features such as command queuing, 16- and 32-bit transfers, and a 10-MHz bus bandwidth. You probably won't implement such features in a system for several years, but if you need the features check with the drive manufacturers for compliance. And make sure that the drive you choose offers a reasonably low SCSI-command overhead. Newer drives typically decode any SCSI command in less than 1 msec.

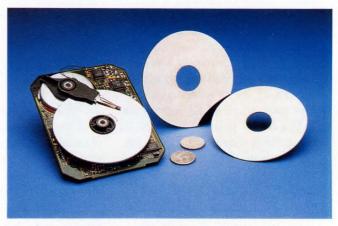
Toshiba, in particular, has taken an innovative approach to implementing the SCSI command set. This approach, called "Virtual SCSI," is used in the company's new MK-350 family of drives, which offer unformatted capacities of 760M bytes. These SCSI drives

cost \$2645 (2000); the company also offers an ESDI version for \$2495 (2000). Toshiba first developed a robust SCSI-2 command-set implementation that includes virtually any command a customer might request, including support for command queuing.

Customers can pick and choose among the commands Toshiba has implemented to create a custom SCSI command set. The customer can also create a version of the Toshiba drive that mimics the command set of a drive from another manufacturer, thus immediately creating a second source. Toshiba stores the command-set implementation on unused portions of the drive, and the drive downloads the proper command set into RAM on power-up. The "soft" command set simplifies inventory logistics, and customers can download command-set updates from floppy disks. Toshiba plans to migrate the technology to its other SCSI drives, and Seagate has used a similar technique in its SCSI drives.

An examination of reliability and performance characteristics will also help you differentiate products from different manufacturers. Unfortunately, you have to look past spec sheets to accurately analyze either set of characteristics. For example, the MTBF spec exclusively defines reliability on the data sheet. But no standard for rating MTBF exists, and most drive manufacturers have their own method for deriving the spec. All manufacturers perform extended-life testing to establish the spec initially, but they have an MTBF goal in mind when they start testing.

Two years ago, typical spec sheets listed an MTBF of 30,000 hours. Today, you'll see figures as high as 60,000 hours. But ask manufacturers to show you just cause for an increased MTBF. You might also ask about



The 3½-in., 100M-byte, single-platter BP-100 from Areal Technology stands 1-in. high, requires less than 1W of power, and targets applications such as high-performance laptop computers.

The SCSI-2 spec formalizes the CCS and adds performance enhancements, such as wide and fast data transfers and command queuing.

which test the manufacturer runs during production, such as the head flying-height test or the media-scan test. Such tests provide clues to the prospect of long-term, error-free operation. You should also consider a manufacturer's reputation for reliable products.

Hewlett-Packard takes an unusual approach to dealing with the MTBF spec in its 5½-in. drives. The company has published in detail the method it uses to initially calculate the spec and how the company tracks real failures in the field. The HP 97540 family, which includes drives with unformatted capacities of 380M-and 760M-bytes, has an MTBF of 60,000 hours. The company has documented evidence of achieving an MTBF in excess of 100,000 hours in the field.

Fully understanding drive performance will also require that you dig past the spec sheets. Furthermore, you must understand performance as it relates to your specific application. Overall disk-drive performance depends on the latency, or delay, added by the mechanical

nature of disk drives and by the speed at which a drive can transfer data.

Two mechanical characteristics of disk drives—the seek time and the rotational latency—add to the total drive latency. The drive has to seek to the proper track on a disk to read or write data. Drive manufacturers typically list an average seek time based on a head movement equal to one-third the width of the band of data on the drive. Most spec sheets also list track-to-track seek time and worst-case seek time. All drive manufacturers don't measure average seek time in the same way, however; and many industry experts claim that a ½-stroke seek doesn't accurately measure the performance potential of a given drive.

Reconsider the average-seek-time spec

Al Sharon, manager of strategic programs at Imprimis, has strong feelings about the seek-time spec. He claims that a better test might be seek time within a

Committees refine SCSI and define CAM

ANSI committee X3T9.2 recently completed the job of developing the SCSI-2 specification. The new spec both resolves ambiguities present in the original SCSI spec and adds features such as command queuing and faster data transfers. Meanwhile, the Common Access Method (CAM) committee plans to produce a specification that defines the software interface between an operating system and a SCSI host adapter. The CAM committee is a relatively new committee, which is funded by its members and not now part of an ANSI committee.

Dal Allan, president of ENDL Consulting (Saratoga, CA), vice chairman of X3T9.2, and chairman of the CAM working group, lends insight into the SCSI-2 spec. Allan claims that the new spec offers three key improvements to system designers. First,

the spec makes the disk-drive Common Command Set (CCS) legitimate and fully defined. Manufacturers have offered CCS-compatible drives for two years. But prior to the SCSI-2 spec, the disk CCS definition was essentially a de facto standard based on the output of a X3T9.2 working group. The SCSI-2 spec also includes a CCS for tape drives. Lastly, the new spec includes more precise documentation and therefore less ambiguity than the original spec.

SCSI-2 adds devices

Allan also points out other advantages to the new spec, including support for new devices, such as scanners and CD-ROMs, and improved error-recovery features. But the features of the SCSI-2 spec most discussed in the press are performance enhance-

ments, such as command queuing, wide data paths, and faster data rates. Allan believes these features will not be widely implemented for five years, except in specialized system designs.

For example, command queuing alleviates the need for a drive to complete a command before the system issues more commands to the same drive. But as Allan points out, Unix-based systems generally implement queuing and caching features in system RAM. Some implementations also queue commands on the host bus adapter. And although Allan agrees that moving the queue even closer to the media offers potential improvement in system I/O performance, he also claims that it makes error recovery much more complicated. Allan also claims that faster data rates—SCSI-2 offers rates as

100M-byte band of data and also proposes a measurement of seek time over a small range, such as three tracks. Sharon believes that such tests would more accurately mimic real operating conditions than does average seek time.

You should also consider the different techniques drive manufacturers can use to manipulate the average-seek-time spec. For example, most seek-time specs include a delay of 3 to 4 msec to allow the head to settle after the actual seek is completed. The drive actually waits through the delay before trying to read or write data. By trimming the settling-time delay by a second, a manufacturer can decrease the average seek time by a second. However, this trimming can occasionally cause 1-revolution latencies due to the misreading of data before the head completely settles.

The type of servo system employed in a disk drive can also affect the seek time. Typically, high-performance drives have employed a dedicated servo head and



You can choose an embedded AT-compatible or SCSI controller with the 3½-in., 200M-byte CP-3200 from Conner Peripherals.

high as 40M bytes/sec—only benefit systems that implement semiconductor drives, drives with large caches, or drive arrays.

Despite the improvements offered by SCSI-2, SCSI-based products still do not offer plugand-play compatibility. The spec includes a well-defined electricalinterface section, but also defines many commands and variations, some of which are optional. Therefore, you'll find plug-andplay capability only in devices designed for closed system architectures such as Apple Macintosh computers or Sun workstations. No standard SCSI implementation exists for IBM-compatible personal computers because IBM has never offered SCSI on a PC.

The CAM committee intends to develop a specification that makes plug and play possible for any SCSI-based system or peripheral. And unlike reports you may have read, no one company's products or ideas form the basis of the spec. Rather, the members have held open forums and taken ideas and features from many people. You can expect the finished spec to be a workable general-purpose definition for integrating SCSI systems. According to Allan, the committee includes members from major companies that make peripherals, peripheral controllers, systems, and software, such as IBM, AT&T, Adaptec, Seagate, Micropolis, NCR, Western Digital, and Sun Microsystems.

The CAM spec has evolved into three modules. The OSD (Operating System Dependent) module describes the interface to specific operating systems and specific CPUs. The SIM (SCSI Interface Module) describes a software interface to a host-bus adapter. Finally, the transport module describes initialization routines and an interface to nonSCSI devices.

Anyone interested is welcome to attend CAM committee meetings. A subscription to receive CAM documentation costs \$200; membership with voting privilege costs \$2000. Contact Dal Allan at (408) 867-6630 for more information. Allan expects to see the first CAM-compatible products at Comdex this fall. You can obtain X3T9.2 documents from Computer Business Equipment Manufacturers Association (CBEMA) in Washington, DC. (202) 626-5741.

Each manufacturer differs in how it derives the MTBF reliability spec; but, in some cases, manufacturers will reveal actual statistics compiled in the field.

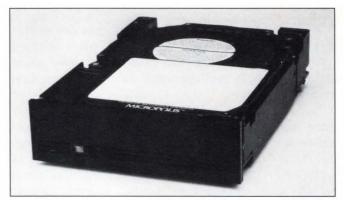
media surface to control the operation of the voice-coil actuator. The dedicated surface provides constant feedback to the control circuit as the actuator moves the heads across the disk. Embedded or sector servo systems have also been used in some cases. The embedded servo schemes depend on bursts of servo information stored at the start of each sector for positioning information. Dedicated servos certainly offer better seektime performance potential than embedded servo systems do, but embedded servo systems offer better tracking performance because the actual data head reads both data and servo information to update its own position each sector. Basically, an embedded servo system eliminates off-track conditions caused by thermal expansion.

Dedicated and embedded servos combined

Toshiba envisioned these servo tradeoffs several years ago and has always provided a hybrid (dedicated and embedded) servo system with its Winchesters.



The 5¹/₄-in., 760M-byte MK-350 drive from Toshiba employs a highly customizable SCSI command set that the controller loads from the disk into RAM at power-up.



Storing 380M bytes in a half-height package, the 5¹/₄-in. Micropolis 1660 (ESDI) and 1860 (SCSI) perform average seeks in 14 msec.

Dave Tovey, director of marketing at Toshiba, claims that the hybrid system offers the best of both worlds. For example, the company's MK-350 products mentioned previously offer a 16-msec average seek time. After reaching the correct track, the drive must rotate through one to three sector boundaries before accessing data. The latency caused by checking the sector servo totals 1 msec worst case. But the drive learns correction factors each time it seeks to a specific track and often incurs a latency of as little as 150 μsec .

Siemens, once a champion of embedded servos, now offers its drives with a hybrid servo. However, you can disable the embedded servo feature after testing the device. Other companies, such as Micropolis, plan to stay with a strictly dedicated servo system for now. Micropolis president Stuart Mabon points out that all Micropolis drives include a thermal calibration feature, which eliminates the need for embedded servo information. And a drive with a sector servo does suffer some latency on seeks and head swaps. Furthermore, the embedded servo uses media space that could otherwise store data.

Drive offers 10.7-msec average seek

The seek-time specs for typical high-performance drives range from 14 to 18 msec. Hewlett-Packard's 97540 drive family offers a 17-msec seek time despite the fact that the product uses an embedded-only servo system. Imprimis employs a hybrid servo system and overall offers the products with the fastest seek times. The company's full-height, 5½-in. Wren V has an average seek time of 14.5 msec and offers an unformatted capacity of 383M bytes. Even more impressive, the SCSI-only, full-height, 385M-byte (unformatted), 5½-in. Wren Runner uses ZBR to offer a 10.7-msec aver-

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age seek time. Only the outer portion of the disks stores data, since the zones there can store the greatest amount of data. ZBR reduces the width of the data band and, therefore, the stroke of the actuator to offer the 10.7-msec seek time. Furthermore, Imprimis sells the Wren Runner for \$1595 (1000)—a price competitive with most mainstream 380M-byte drives.

Once a drive performs a seek to a track, the drive must wait for the sector in question to rotate to the heads—the rotational latency. Disk manufacturers simply list the average rotational latency as half the time it takes the disk to make a single revolution. Most drives rotate at 3600 rpm and therefore have a 8.33-msec average latency.

Rotational latency is a straightforward spec. Some controllers, especially host-resident ESDI controllers,

reduce their rotational latency by beginning to read data as soon as they come on track. This method is called a zero-latency read. The controller then simply orders the data properly during the DMA transfer from controller to main memory. Manufacturers of SCSI-based drives have also improved the way embedded controllers handle rotational latency during routine reads and writes. But all systems occasionally suffer from the latency of a full revolution due to special circumstances such as an off-track condition. Hewlett-Packard took a step to absolutely reduce rotational latency in its 97540 family of products: The drive designers boosted the rotational speed of the drives to 4002 rpm, thus decreasing the average rotational latency to 7.47 msec.

SCSI drives add an additional source of latency. The

EDN May 25, 1989

Seek time, latency, and transfer rate primarily define the performance of a drive, yet each spec should be considered relative to a specific application.

SCSI controller takes some amount of time, called command overhead, to process commands. SCSI transactions also include connecting to and disconnecting from the bus. In total, the overhead from using SCSI should total more that two milliseconds. And even host-resident ST-506 and ESDI controllers add some overhead.

The data-transfer rate of a disk drive also affects its performance. Drives with device-level controllers simply transfer data at the same rate that the read channel operates. ESDI drives, for example, transfer data at 10M bps for prior-generation products, 15M bps for current-generation products, and 20M bps for next-generation products. You can buy a couple of ESDI drives from Hitachi and Hewlett-Packard that offer 20M-bps read channels, but no company currently ships compatible controllers.

Separate system and drive data rates

Drives with intelligent controllers often specify two data rates: the drive read-channel rate and the interface rate. For example, newer SCSI drives support SCSI transfers as fast as 4M bytes/sec. A 20M-bps drive can't continuously feed a 4M-byte/sec interface, but a drive can fill its buffer and then match the faster 4M-byte/sec rate of the interface.

To put drive performance into perspective, consider some typical applications. An application such as imaging and real-time video benefits from high raw read-channel data rates. The imaging program needs to receive data continually to update the video image in real time. A cache doesn't hold sufficient data to be used in imaging. In fact, disk arrays may best serve such applications (for more information on disk arrays, see **box**, "Drive arrays boost reliability and performance").

A large percentage of the market for the drives discussed here includes applications in both file servers and computers used in transaction processing. Transaction-processing systems require drives with minimal latency. These systems also require fast system transfers but not necessarily superfast raw-data rates. A

Drive arrays boost reliability and performance

Subsystems built around arrays of 3½- or 5½-in. Winchester drives can offer reliability and performance specs that exceed the capability of one or more individual drives. For example, a 4drive array can break incoming data up and stripe it across the array, thus virtually quadrupling the transfer rate. Other array configurations simply offer lower subsystem latency because the array can overlap seeks to several drives. Typically, arrays include one or more parity or ECC drives, which let the array continue to operate after a singledrive failure.

Micropolis first offered an array of drives as an OEM product about 18 months ago. The array included four data drives and a single parity drive. According to company president Stuart Ma-

bon, Micropolis has shipped a number of the arrays, but the company recently canceled the program. Mabon claims that system manufacturers in general wish to design their own arrays. Most other drive manufacturers agree with Mabon; and, in fact, most drive manufacturers now offer features, such as a synchronization signal on ESDI drives, that help system designers implement arrays.

You can, however, still buy an array or design one with off-the-shelf products. And you can expect more of such products in the near future. For example, Ciprico Inc (Plymouth, MN), a well-known controller-board manufacturer, recently introduced a single-board array controller. The Ciprico Rimfire 6600 includes a SCSI-2 interface on the host side

and ESDI interfaces to the five drives in the array.

You can use the Rimfire 6600 to implement an array that works very much like the array Micropolis offered. The board stripes data across four drives and stores parity data on the fifth. The SCSI implementation supports data transfers as fast as 20M bytes/sec out of cache, and transfers directly to and from disk occur at a rate four times faster that the rate of a single drive. The array also offers a subsystem capacity four times the capacity of a single drive.

Subsystems based on this board can continue to operate after a single-drive failure. After a failure, you can replace the failed drive, and the subsystem can regenerate the appropriate data in a background mode. The Rimfire

typical transaction-processing request results in a transfer of 2k to 8k bytes of data, much less than a single track. The key to transfer rate in such an environment is to keep the system I/O bus free, so that no operations wait long for access to the bus. Therefore, a fast SCSI transfer capability fills the need to transfer buffered data quickly.

1.2G-byte drives emerge

Now consider some of the new products available in different form factors and product classes. Both Micropolis and Imprimis have announced 1.2G-byte (unformatted), 5½-in., full-height drives. Micropolis plans to ship the SCSI and ESDI members of its 1510 series in the third quarter of this year. The drives will sport 20M-bps read channels, and the company plans to offer production quantities of the products for less than \$2 per megabyte in the fourth quarter. Imprimis has yet to announce shipping information or pricing for the 1.2G-byte drive it has designated Wren VII.

A number of companies now ship 760M-byte-class



With the announcement of the 1.2G-byte Wren VII, Imprimis again demonstrated the performance and capacity advantages of zoned-bit recording.

6600 measures 16×16.5 in. (suitable for rack mounting) and costs \$5995.

You can also buy an off-the-shelf array subsystem from Pacstor Inc (Los Gatos, CA). The company's first product, the Integra I, includes six 3½-in. drives in an IBM PC/AT-style enclosure. The array subsystem actually interfaces to the host as six individual drives at six SCSI addresses. But the product includes a SCSI host adapter and driver software. You can use the product with MS-DOS, OS/2, or Xenix operating systems and with the IBM PC/AT or Microchannel bus.

Pacstor targets the Integra I at applications, such as file servers, that benefit from overlapped seeks to multiple drives and require data integrity and fault tolerance. The host-based driver

software reads and writes data to a single drive during a transaction. However, data is spread across all five drives over time.

The software also stores ECC information on the sixth drive each time a write occurs on one of the data drives. The ECC drive ends up with data in each sector that can be used to correct data stored in the same sector on any one of the data drives. Pacstor offers two MTBF specs for the drive. The mean time between loss of access to the subsystem is 150,000 hours; the mean time between loss of data is 1 million hours. The Integra I costs \$9880 with 40M-byte drives and a 200M-byte subsystem capacity and \$13,780 with 100Mbyte drives and a 500M-byte subsystem capacity.

Pacstor has also begun ship-

ping the Integra III in evaluation quantities. This new array employs 12 drives-10 data and two ECC—and includes all array software in the subsystem, so you can use the array with any SCSIbased system. You can buy the subsystem with 100M-byte or 200M-byte drives for a total capacity of 1G or 2G bytes. You can also order configurations of the Integra III that stripe data across groups of drives the same way the Ciprico controller does to increase the data rate. And Pacstor offers the new array with optional dual power supplies and dual data paths that result in a mean time between loss of access or data of greater than 1 million hours. The Integra III costs in the \$30,000 range.

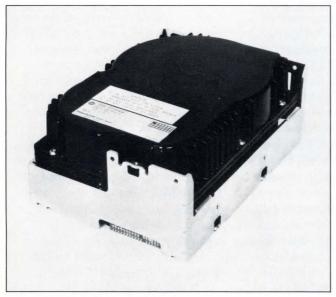
Several manufacturers have adopted a hybrid servo system to ensure a fast seek-time spec and maintain accurate tracking in adverse thermal conditions.

(unformatted) products, and over the summer expect these companies to try to sew up OEM customers. Maxtor has been shipping the products the longest and has a substantial advantage in terms of units shipped. Other potential players include Fujitsu, Hewlett-Packard, Hitachi, Imprimis, Micropolis, Miniscribe, NEC, Priam, Siemens, and Toshiba. Obviously, the 760M-byte market can't, at least initially, support all of these participants.

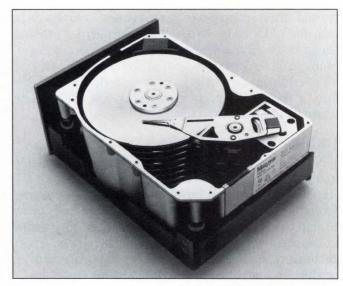
760M-byte drive offers 14-msec seek time

Only three of these companies offer performance specs that set their products apart from the rest. Priam's Models 676 and 776 offer 14-msec average access times. The ESDI-based 676 costs \$3675; the SCSI-based 776 costs \$4550. The Hewlett-Packard 97540 series of drives supports 20M-bps read channels because the drives employ a faster rotational speed than do standard drives. Available in both SCSI and ESDI versions, the drives cost \$2130 (1000). Hewlett-Packard also offers 380M-byte depopulated versions of this family of drives for \$1450 (1000). Hitachi offers a 20M-bps read channel on its DK515-78 products. The SCSI version costs \$3200 (100); the ESDI version costs \$3100 (100).

The same companies that offer 760M-byte products also offer 380M-byte (unformatted), full-height, 5¹/₄-in. drives. Imprimis by far offers the most diverse range



A 20M-bit/sec read-channel data rate makes Hitachi's 780M-byte DK515 a good choice for applications, such as imaging systems, that require high transfer rates.



The SCSI-2 command-queuing feature has been added to all of Maxtor's embedded-controller drives, including the XT-8000 380M-and 760M-byte offerings.

of products. Expect the 380M-byte class of products to move heavily into the distributor channel this year.

In the half-height class of 5½-in. drives, Imprimis and Micropolis have introduced 380M-byte (unformatted) products. Both companies will be shipping the drives by the time this article appears. The Imprimis Wren VI Half-Height stores 383M bytes and has an average seek time of 16 msec. You can specify the drive in AT-compatible, ESDI, and SCSI versions that cost \$1495, \$1395, and \$1495 (1000), respectively. The half-height 380M-byte offerings from Micropolis offer average seek times of 14 msec. The 1660 ESDI model sells for \$950 (100); the 1680 SCSI version sells for \$995 (100).

Micropolis, Imprimis, Microscience, and Rodime have all had success selling half-height drives in the 170M-byte class. Yet, Microscience and Rodime have decided not to build 380M-byte half-height drives. Bob Oakley, Director of Sales and Marketing at Microscience, believes that customers for 380M-byte drives don't care if the form factor is full or half height. Furthermore, Oakley claims that few customers will pay a premium for a half-height product. Rodime, meanwhile, has decided to invest its energies in 3½-in. projects.

Conner Peripherals led the bandwagon by introducing a 3½-in., 209M-byte (formatted) drive, the CP-3200, at Comdex last fall. And you'll probably see 400M-byte products announced at Comdex this fall.



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Nearly a dozen companies now offer 760M-byte drives, and each will attempt to carve out its share of the market during the course of this summer.

The CP-3200 has established a standard formatted capacity level at 200M bytes. Furthermore, these products quickly established market share in high-end personal computers and low-end workstations. The Conner drive offers an average seek time of 19 msec, has a read-channel data rate of 12M bps, and costs \$1150 (500). You can specify the CP-3200 with SCSI or AT-

compatible interfaces.

Maxtor also offers a 3½-in. drive with a formatted capacity greater than 200M bytes. The LXT-200S drive with an embedded SCSI controller costs less than \$1100 (1000). This drive features a 15-msec average seek time and employs a 3-band implementation of ZBR. The read-channel data rate varies by zone from 9.2M to

Manufacturers of Winchester disk drives

For more information on disk drives such as those described in this article circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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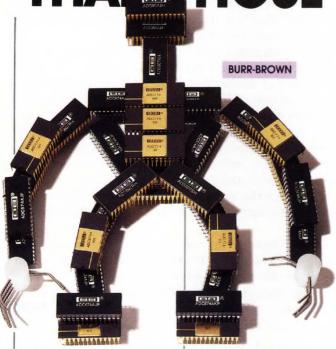
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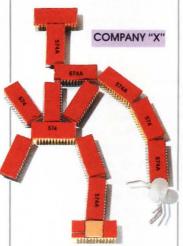
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Hot competition exists in the 200Mbyte class of 3½-in. drives that target applications such as high-end personal computers and low-end workstations.

14.8M bps. Rodime also chose to employ ZBR in its 216M-byte (formatted), SCSI- and AT-compatible Model RO 3259A drives. The products offer 18-msec average access times and cost less than \$950.

Hitachi recently introduced some 200M-byte-class, 3½-in. products as well. The DK312C-20 offers a formatted capacity of 209M bytes; the DK312C-25 offers a formatted capacity of 251M bytes. The drives transfer data at 1.77M bytes/sec and have 20-msec average access times. With a SCSI controller, the DK312C-20 sells for \$1500 (100) and the DK312C-25 for \$1500 (100). Imprimis offers a 3½-in. drive with a formatted capacity of 172M bytes but plans to offer a 200M-byte model soon.

Laptop drive market awakens

The market has also heated up for drives that target laptop applications. Conner currently controls much of the market with its 1-in.-high, 3½-in., 20M-byte CP-3020 and 40M-byte CP-3040. But several other manufacturers have plans to take a share of the small low-power, low-weight market. Sony, for example, just entered the US Winchester market with a commodity 3½-in. drive. And now Sony has introduced a 1-in.-high product that consumes less than 2W. The as-yet-unnamed drive will be available this summer in a single-platter, 40M-byte version. A 2-platter, 80M-byte version will follow later this year. The drives offer a choice of AT- or SCSI-compatible controllers and feature a 19-msec access time. The 40M-byte drive will cost \$325 (10,000) initially.

PrairieTek and Areal Technology have taken even bolder steps to reduce size and power. Last fall, PrairieTek introduced a 20M-byte drive in a 2½-in. form factor. The company has begun shipping the \$400 Prairie 220 in AT-compatible and SCSI versions. The drive consumes 1.5W and weighs 9 oz. The 2½-in. form factor occupies only 30% of the space that a standard 3½-in. product does. PrairieTek has plans for a similar 40M-byte product.

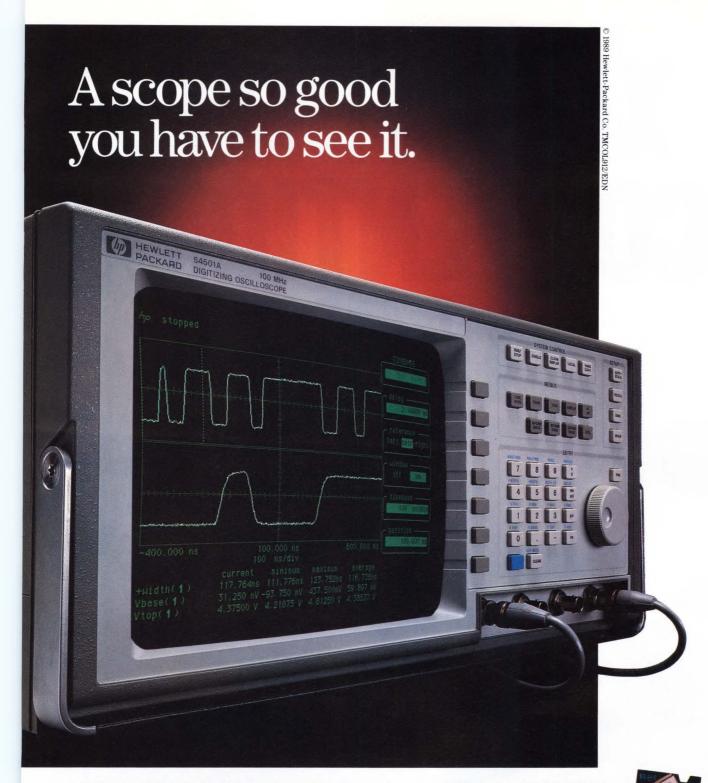
Areal Technology, meanwhile, offers a 1-in.-high, $3\frac{1}{2}$ -in. drive that stores 100M bytes on a single platter. The company has also announced 50M- and 200M-byte versions of the product. Areal employed innovative features, such as glass-substrate media and a plastic enclosure for the heads and media, which resulted in a 9-oz package. The BP-100 includes an AT-compatible

interface, uses less than 1W, has a 29-msec average seek time, and costs \$595 (1000).

Other companies still aren't sure that any of the announced products truly fill the need for the next generation of smaller Winchesters. Timothy Mahoney, Vice President of Marketing and Sales at Rodime, remembers the transition from the 5^{1} /4-in. to the 3^{1} /2-in. form factor in which Rodime played a major part. He claims that the low-profile, 3^{1} /2-in. drives will serve the laptop industry well as a stopgap until a smaller standard emerges. And he believes that a new standard will emerge the same way the industry defined the 3^{1} /2-in. form factor—as 25% of the size of the larger standard.

In any case, everyone involved sees a need for smaller drives. And the potential competitors seem intent on chasing the heels of $3\frac{1}{2}$ -in. products the same way that manufacturers of $3\frac{1}{2}$ -in. products chased $5\frac{1}{4}$ -in. drives.

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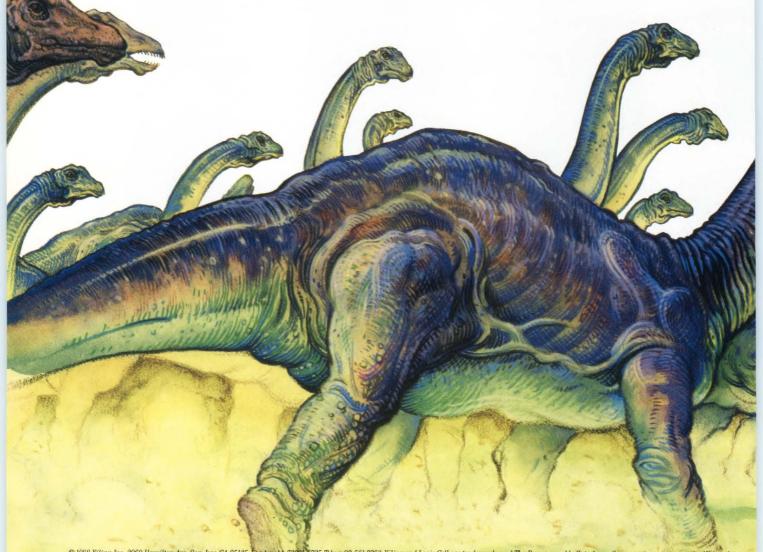
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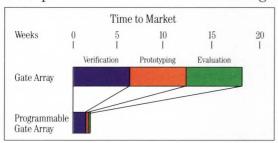
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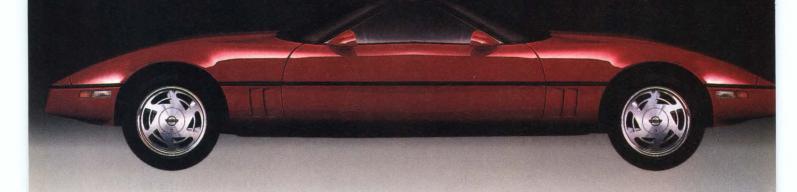


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External compensation boosts op-amp performance

Although op amps typically include internal compensation, the resulting performance isn't always satisfactory. You can significantly enhance a circuit's performance by using op amps that also accommodate external compensation.

Charles Kitchin and Scott Wurcer, Analog Devices Inc

Although most high-speed op amps feature built-in compensation, some new devices also provide optional external compensation. This additional compensation lets you use an op amp to perform functions that aren't possible with standard op amps—such as driving high capacitive loads while maintaining a fast settling time. By adding the proper external capacitor to an amplifier, you can also improve your op amp's slew rate and bandwidth in a variety of circuit configurations. To apply external compensation to the AD744 bipolar FET (BiFET) op amp, for example, you connect the proper capacitor between pin 5 and pins 1 or 8, depending on the application. The schematic of the AD744 (Fig 1) details where these pins connect internally. As shown, the external capacitor is in parallel with the 5-pF internal compensation capacitor.

Both the slew rate and the gain-bandwidth product of a high-speed amplifier are inversely proportional to the value of the external-compensation capacitor, C_{ext} . Therefore, to maximize an amplifier's speed, you should try to minimize the value of the compensation capacitance. Conversely, use large values of C_{ext} to slow an amplifier to a point at which the slew rate is perfectly symmetrical and well controlled. The table

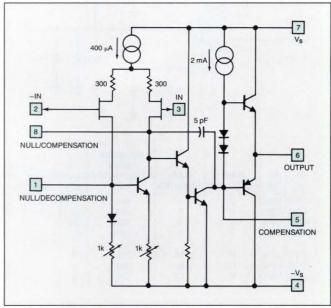


Fig 1—In addition to containing 5 pF of internal compensation, the AD744 BiFET op amp can accommodate external compensation.

in Fig 2 summarizes the effects of external compensation on the AD744's slew rate and bandwidth under three different load conditions.

Amplifiers that provide optional external compensation also give you the flexibility to implement a variety of designs without sacrificing performance. If you configure the AD744 as a unity-gain voltage follower and add external compensation (Fig 2), for example, the op amp can drive capacitive loads in excess of 2000 pF and maintain a 1.5-µsec settling time to 0.01%. For stable operation, this configuration requires a minimum external-compensation capacitance of 5 pF.

Fig 3 shows the AD744 as a voltage follower with gain (a) and as an inverting amplifier (b). In these applications, external compensation isn't necessary for stable operation. However, external compensation might be appropriate for driving capacitive loads in the range of 50 to several thousand picofarads.

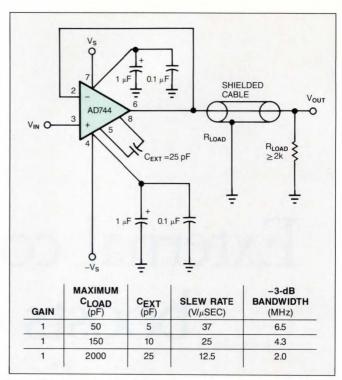


Fig 2—Configured as a unity-gain voltage follower with external compensation, this circuit can drive long shielded cables. The table gives the recommended compensation-capacitance values and the typical performance of this circuit under three different load conditions.

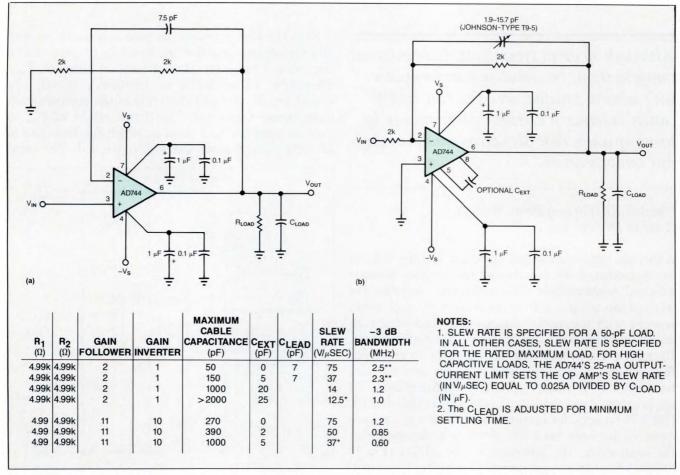


Fig 3—When you use the AD744 as a unity-gain inverter (b) or use it to drive high capacitive loads, you should employ the amp's optional compensation feature.

Both the slew rate and the gain-bandwidth product of an amplifier are inversely proportional to the value of the compensation capacitor.

The ability to provide external compensation is particularly useful when you are driving high capacitive loads such as long commercial shielded cable. Cable capacitance varies widely, but it generally ranges from 9 pF/ft for low capacitive audio cable to as much as 50 pF/ft for standard computer wiring. Driving a 100-ft cable with a total capacitance of 900 to 5000 pF isn't possible with most fixed-compensation op amps; the excessively high capacitive load reduces the op amp's phase margin, often causing oscillation.

The table in Fig 3 lists the recommended compensation-capacitance values for driving cable loads of various capacitances. In each case, the recommended $C_{\rm ext}$ is a minimum value. You can use a larger value, but doing so degrades the slew rate and the bandwidth.

Extend gain bandwidth with decompensation

When you use the AD744 in applications that have a closed-loop gain greater than 10, you can enhance the gain-bandwidth product by connecting a small capacitor between pins 1 and 5 (**Fig 4**). At low frequencies, this capacitor cancels the effects of the chip's internal-compensation capacitor, $C_{\rm int}$, effectively decom-

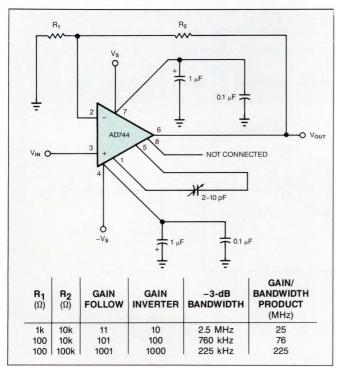


Fig 4—For applications involving a closed-loop gain greater than 10, you can connect a decompensating capacitor between pins 1 and 5 on the AD744 to extend the circuit's gain-bandwidth product. The table summarizes this circuit's performance.

pensating the amplifier. The table in Fig 4 provides a gain-vs-performance summary of the AD744 in this decompensation configuration.

When implementing decompensation, however, remember that manufacturing conditions cause the value of internal capacitance to vary among amplifiers. You should therefore optimize your amplifier's response for the desired gain by using a 2- to 10-pF trimmer capacitor, rather than a fixed-value capacitor. If you modify the commonly used 3-op-amp instrumentation-amplifier connection to include decompensation, you can substantially increase the circuit's bandwidth.

In addition to having high bandwidths and fast slew rates, some amplifiers, such as the AD744, feature single-pole responses to allow the fastest true settling times. Amplifiers that use a pole-zero mismatch in their compensation network (to increase the phase margin at the crossover point) usually have long settling tails. These tails aren't present, however, in single-pole amplifiers.

Fig 5 depicts the computer-generated responses of two idealized single-pole-compensated, FET-input op amps. The inverting amplifiers have a 13-MHz unity-gain crossover frequency. One response is from an amplifier with a 50-V/μsec slew rate and the other is from an amplifier with an infinitely high slew rate. As the outputs approach their final values, the two responses

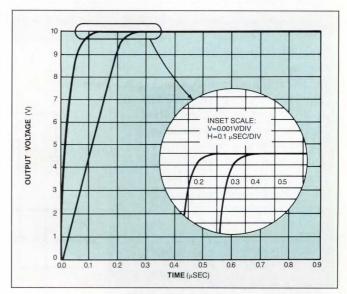


Fig 5—The responses of the two 13-MHz unity-gain inverting amplifiers approach their final value. The responses of the limited-slew-rate and infinite-slew-rate devices begin to look the same, but the limited-slew-rate device's response is delayed by approximately 125 nsec.

Driving a 100-ft cable with a capacitance of 1000 to 5000 pF is beyond the capabilities of many fixed-compensation op amps.

begin to look the same. However, the response of the limited-slew-rate amplifier is delayed by approximately 125 nsec. The magnified inset in Fig 5 provides details of the settling time.

Build a fast-settling inverter

The fast-settling inverter circuit in **Fig 6a** combines the virtues of a precision bipolar amplifier with the rapid slew rate and the wide bandwidth of a high-speed BiFET op amp. In addition to exhibiting a 900-nsec settling time to 0.01%, this composite amplifier features the high dc precision associated with a quality bipolar amplifier.

This circuit takes advantage of a novel compensationtrim scheme that uses the AD744's external-compensation pin to null the long tails typically associated with composite amplifiers operating as integrators. Amplifier IC₁ senses IC₂'s input offset voltage (via IC₂'s sum-

The mathematics of external compensation

An amplifier with a single-pole or ideal-integrator open-loop frequency response will achieve the minimum possible settling time for any given unity-gain bandwidth. However, when this socalled ideal amplifier is used in a practical circuit, the actual settling time increases above the minimum value because the external circuity introduces additional time constants. These time constants are often caused by additional capacitance on the amplifier's summing junction. You can minimize this increase in settling time by selecting the proper value for the feedback capacitor, C_f.

The integrator circuit in **Fig A** shows an op amp connected as an I-V (current-to-voltage) converter. For an op amp configured as an ideal integrator with a unity-gain crossover frequency, use the following equation to determine the circuit's small-signal behavior.

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} \!\!=\!\! \frac{-R}{\frac{R(C_f\!\!+\!C_x)S^2}{2\pi\!f_{\text{o}}} \!\!+\!\! \frac{G_n}{2\pi\!f_{\text{o}}} \!\!+\!\! (RC_f\!S) \!\!+\! 1},$$

where S = the LaPlace operator, $f_0 = the$ op amp's unity-gain crossover frequency, and $G_n = the$ circuit's noise gain $(1 + (R/R_0))$.

Solving the above equation for C_f yields:

$$C_f \!\!=\!\! \frac{2\!-\!G_n}{R2\pi\!f_o} \!\!+\!\! \frac{2\sqrt{RC_x\!2\pi\!f_o\!+\!(1\!+\!G_n)}}{R2\pi\!f_o}$$

The first equation would completely describe the output of the system if the op amp didn't have a finite slew rate and other nonlinear characteristics. Even if you consider these effects, the finescale settling to less than 0.1% is determined by the op amp's small-signal behavior.

In these equations, the capaci-

tance, C_x , is the total capacitance that appears at the op amp's inverting terminal. This capacitance is the sum of the output capacitance of the current source and the input capacitance of the op amp, which includes any stray capacitance at the op amp's input. When modeling an I-to-V converter, you can use the Norton equivalent circuit in **Fig A**.

Replacing R_o and I_o with their Thevenin V_{in} and R_{in} equivalents creates the general-purpose inverting amplifier in Fig B. Here, C_x represents the AD744's input

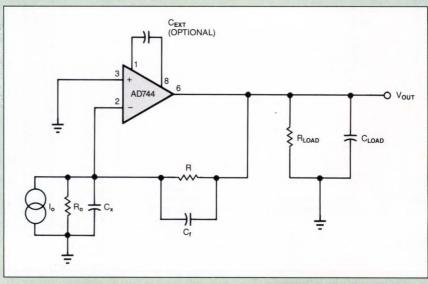


Fig A—In this simplified model of an ideal integrator, an op amp is configured as a current-to-voltage converter.

ming junction) and nulls the input offset voltage by applying an offset voltage to IC₂'s noninverting input.

Normally, this approach yields a circuit that has both a fast slew rate and a high degree of dc precision but suffers from long, slow settling tails (settling times of 5 to $10~\mu sec$ are typical). These long settling times occur because the circuit's net response has a pole and a zero that aren't coincident. However, in **Fig 6a**'s circuit, a small trimmer capacitor applies feedback via

the AD744's external compensation pin. When correctly adjusted, this capacitor moves the pole and the zero back together, thereby removing the troublesome tail from the circuit's response.

The oscilloscope photo in **Fig 6b** illustrates this circuit's rapid settling characteristics. To adjust the compensation, drive the circuit's input with a 1-kHz square wave and adjust the trimmer capacitor for a minimum settling time.

capacitance (5.5 pF) plus any stray capacitance due to the wiring and the IC package.

In either case, the capacitance causes the system to change from a 1- to a 2-pole response. The additional pole increases the settling time by introducing peaking or ringing in the op amp's output. If you can estimate the value of C_x with reasonable accuracy, you can use the second equation to determine the correct value for C_f and use a small capacitor that optimizes the amplifier's response. Usually, you can adjust the response to that of a critically damped 2-pole system with a

quality factor of 0.5 and a -3-dB bandwidth equal to:

$$f(-3dB){\approx}0.64\ \sqrt{(f_{\text{o}})\,\frac{1}{2\pi R_{2}\ (C_{\text{f}}+C_{x})}}.$$

Note that when resistor R is greater than 1.6 k Ω , the amplifier's response is improved by the addition of a small capacitor, C, that has the proper value. For critical applications in which the maximum possible bandwidth is desired (or the value of capacitor C_x isn't known), you should make C_f a variable. C_f should be a trimmer capacitor whose range centers around the ideal calculated value. Use the previous equation

to calculate the system's resulting response.

In some cases, the frequency response is greater than basic theory $(f=f_{\text{o}}/G_{\text{n}})$ predicts. Above a certain impedance level, the time constants introduced by external components limit the bandwidth to less than the theoretical value.

The AD744 lets you directly modify its open-loop frequency response via an external capacitance connected between pins 5 and 8 of the op amp. The major benefit of this feature is an improved phase margin-and therefore greater stability—when the amplifier is driving a high capacitive load or when it's operating at a noise gain of less than two. Use the following three equations to calculate the AD744's resultant slew rate, crossover frequency, and compensation capacitance. Note that in each equation, C_{ext} is measured in farads.

Fig B—In this general-purpose inverting amplifier, the current source of Fig A is replaced with an input-voltage source.

$$\begin{split} \text{SLEW RATE} &= \frac{3.0 \times 10^{14} \text{ V/}\mu\text{SEC}}{\text{C}_{\text{EXT}} + (5 \times 10^{-12})} \,. \\ &\quad \text{CROSSOVER} \\ &\quad \text{FREQUENCY} \text{ (Hz)} = \\ &\quad \frac{1}{2\pi (2450) \text{ C}_{\text{EXT}} + (5 \times 10^{-12})} \,. \\ &\quad \text{C}_{\text{EXT}} \\ &\quad \text{(FARADS)} = \frac{1}{\text{f}_{\text{c}}(2\pi)2450} - (5 \times 10^{-12}). \end{split}$$

External compensation lets you perform functions with an op amp that aren't usually possible with standard op amps.

Fig 7 presents another configuration that uses external compensation to increase a circuit's performance. This design is a variation of the 1-op-amp instrumentation-amplifier principle. The capacitor in Fig 7 applies feedback to the FET op amp's offset pins, rather than

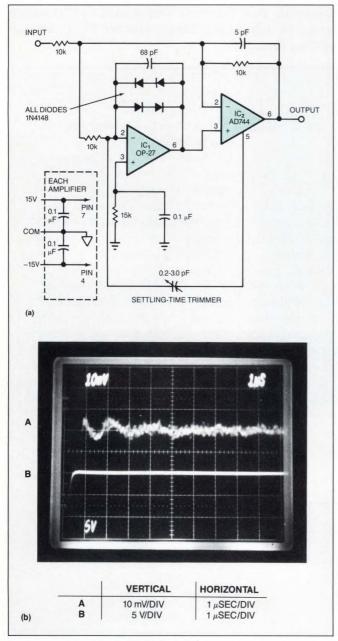


Fig 6—By combining the virtues of a precision bipolar amplifier with the rapid slew rate and wide bandwidth of a high-speed BiFET op amp, you can configure a fast-settling inverter circuit (a). This circuit's rapid settling characteristics are illustrated in the oscilloscope photo (b).

to its inverting-input terminal. Because feedback is applied directly to the input FETs' drains, both the inverting and noninverting inputs form a true high-impedance differential-input section.

This circuit offers significant improvements over previous designs because it lets you either enhance or degrade the bandwidth by connecting a single external capacitor between pin 5 and pin 8 or 1 of the AD744. A circuit's gain equals the ratio of the value of the two external resistors to the transconductance of the input FETs. Within an accuracy of $\pm 10\%$, the gain is:

gain
$$\approx R/2430\Omega$$
,

where R is measured in ohms. At a gain of $100~(R=243~k\Omega)$, the circuit's bandwidth will be 750 kHz if you connect a 2- to 10-pF bandwidth-enhancement capacitor between pins 5 and 1. Under these conditions, the circuit's total harmonic distortion is less than 0.01%

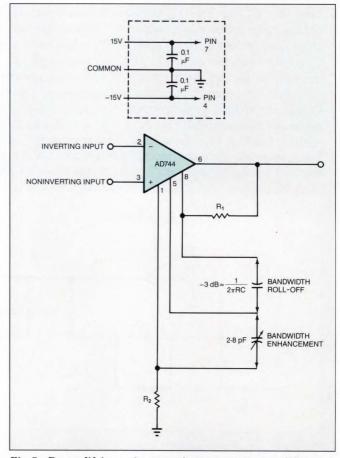


Fig 7—By modifying a 1-op-amp instrumentaion amplifier, you can enhance a circuit's bandwidth and roll-off.



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Using the decompensating pins of an op amp, you can cancel the effects of the internal compensation capacitor and extend the amplifier's gain-bandwidth product.

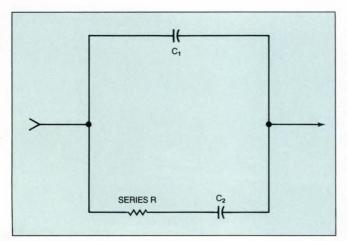


Fig 8—Effective series resistance can increase the time required for a capacitor to charge and discharge and therefore significantly increase an op amp's overall settling time.

with a 3V output and a 1-kHz sine wave. The circuit exhibits little distortion because feedback is applied directly to the FETs' drains, rather than to the amplifier's offset-null pins. Also, the AD744 has an inherently low level of distortion.

Because the circuit's closed-loop gain is set between the drains of the input-stage's FETs and the amplifier's output, the input stage's gain is completely independent of the ratio of external resistor values. The input stage's gain is determined solely by the input stage's transconductance. However, because the input stage's gain varies with temperature, the circuit's overall gain also varies slightly with temperature.

Choose capacitors carefully

Because some amplifiers, such as the AD744, have inherently high bandwidths, you should exercise care when selecting external components. The simple model in the **box**, "The mathematics of external compensation," explains how to deal with a high-speed op amp's external time constants. The passive devices you use in a design can greatly affect your circuit's performance. The chief villain to guard against when selecting a capacitor is dielectric absorption; it can greatly increase an amplifier's settling time.

The capacitor in **Fig** 8 illustrates how dielectric absorption can affect a circuit. As shown, there are effectively two capacitors connected in parallel. The principal capacitor, C_1 , is easily charged or discharged. However, the voltage across the smaller capacitor, C_2 , can't change quickly because of the effective series resis-

tance. The increased charge/discharge time required by a capacitor with high dielectric absorption significantly contributes to an op amp's overall settling time. For example, if the optional external capacitor in Fig 3b is a high-K ceramic trimmer, the amplifier's overall settling time will be much greater than the AD744's typical 500-nsec settling time. You can minimize this problem by selecting external components that exhibit low dielectric absorption, such as polypropylene, polystyrene, and mica capacitors.

Authors' biographies

Charles Kitchin is a technical writer for the Semiconductor Div of Analog Devices (Wilmington, MA) and has been with the company for 13 years. His responsibilities include preparing data sheets and writing technical articles and application notes to support new products. Charles has an ASET degree from Wentworth Institute and is currently working toward a BSET degree at the University of Lowell. His personal interests include constructing amateur telescopes and restoring WWII military radios.



Scott Wurcer is a senior design engineer at the Semiconductor Div of Analog Devices and has been with the company for 15 years. His major responsibilities are designing op amps and other linear ICs. He designed the company's AD711 family of op amps, the AD744 op amp, and the AD524 and AD624 instrumentation amplifiers. Scott has a BSEE from the Massachusetts Institute of Technology and is a member of the IEEE and the AES. In his spare time, Scott enjoys carpentry and music.



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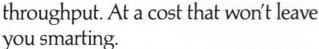
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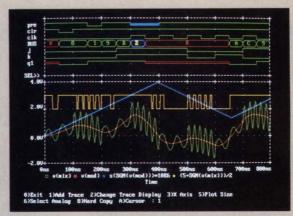
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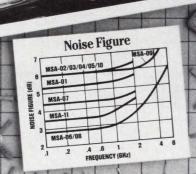
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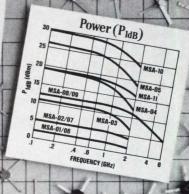
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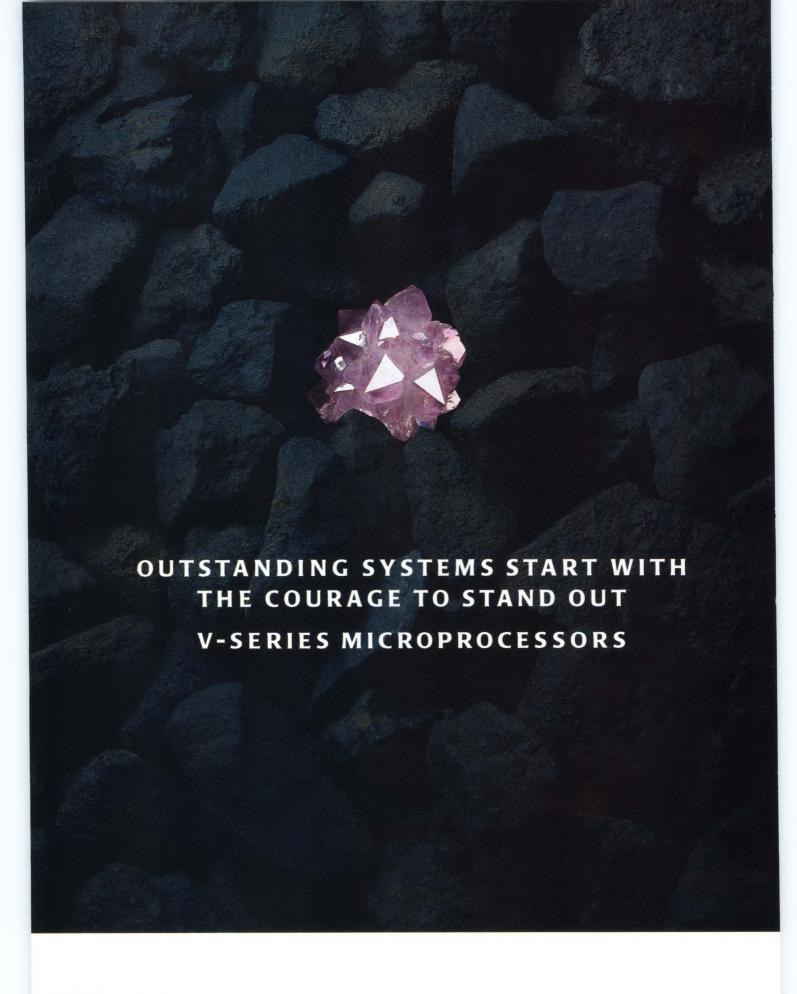
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Analog and mixed-signal (analog/digital) devices continue to grow in speed, complexity, and accuracy. To characterize and test these increasingly intricate products, engineers must use techniques that provide more detailed and precise information than do approaches that worked well with simpler devices. Opposing the desire for more exhaustive analysis is a constant demand for higher testing speed. Test methods for new mixed-signal devices not only must meet strict accuracy and throughput requirements, but must also work within the constraints imposed by the capabilities of the automatic-test hardware and software. By developing techniques that satisfy all of these criteria, test engineers are pushing forward the state of the art of automatic test.

Fourier spectrum analysis is a fundamental tool used to characterize linear and mixed-signal devices. Calculating the frequency components from a sequence of data samples (a data set) reveals a signal's frequency-

domain parameters, such as signal-to-noise ratios, harmonic distortion, differential phase and gain, jitter, and other spectrum-analysis measurements. Knowing these values is essential when you're testing video components and such devices as A/D and D/A converters, modems, ISDN (integrated-service digital network) devices, and filter/CODECs (coder/decoders). The two techniques most often employed in computing the Fourier components of a data sequence are the discrete Fourier transform (DFT) and a more efficient but limited algorithm known as the fast Fourier transform (FFT) (see Ref 1). Both techniques produce equivalent results by transforming data from the time-sample domain to the discrete Fourier frequency domain. The speed of calculation and the restrictions placed on the data to be analyzed reveal the differences between these two techniques. A less well-known technique, the chirp-Z transform, computes identical results and offers advantages over both the DFT and the FFT.

Sine on the x axis, please

All Fourier frequency transforms are based on the fact that you can completely represent an arbitrary real waveform as an integration of cosines across the entire frequency spectrum. Because each of these cosines is at a specific phase, the cosine is often represented as the sum of a cosine and a sine—each with an appropriate amplitude and a phase of zero. The amplitude of the transform's calculated cosine and sine components is a representation of the content of each

Calculation intensity limits the usefulness of the DFT as the number of samples in the data sequence becomes large.

frequency contained in the sampled data. The sum of the entire series of amplitude and phase terms for all frequencies completely and uniquely determines the sampled waveform. The simplest way to reconstruct a waveform is to sum the series of cosines from a discrete Fourier transform.

The DFT algorithm calculates the frequency components directly from a cosine/sine series. A DFT is a literal and direct calculation of the frequency content of a sequence of data. Each point from the sampled data sequence is multiplied by a sample from a sine and a cosine of the frequency being analyzed. The sum of the cosine products is defined as the "real" component of the spectrum, and the sum of the sine products is defined as the "imaginary" component of the spectrum (Fig 1). The sum of the squares of the real and imaginary components at a particular frequency is termed the "spectrum power" at that frequency. The arctangent of the quotient of imaginary component divided by the real component at a particular frequency is called the "phase." To obtain a plot of the power at all the pertinent frequencies (a "spectrum" plot), you must add the products of the cosines and the data to the products of the sines and the data at all the cosine and sine frequencies. You can then make a graph of the power and the phase vs frequency. Fig 2 includes pseudocode for calculating the DFT.

To understand the equations that appear in the figures, you need to be familiar with the definitions of the symbols: The quantity "x_n" is the nth sample in a data sequence in the time domain. "N" represents the total number of samples in a data sequence, and "X_k" denotes the kth frequency term in a Fourier series. (A zero value of the index, k, denotes the dc term; k=1 denotes the fundamental-frequency term, and so on.) The quantity "v_n" is the nth term in a summation of exponential terms. "Vk" is the kth member of the Fourier series, which you obtain by transforming the summation of v_ns. "W_k" is the weighting of the kth frequency component of the series of Vk terms. The Greek letter "0" denotes an arbitrary phase angle, and the Greek letter " Σ " denotes the summation operation. The expression "Φ(h)" is the Fourier transform of the time function h; the expression " $\Phi^{-1}(h)$ " is the inverse Fourier transform of the frequency function h. Lowercase "j", of course, represents $\sqrt{-1}$. The prefix "RE"

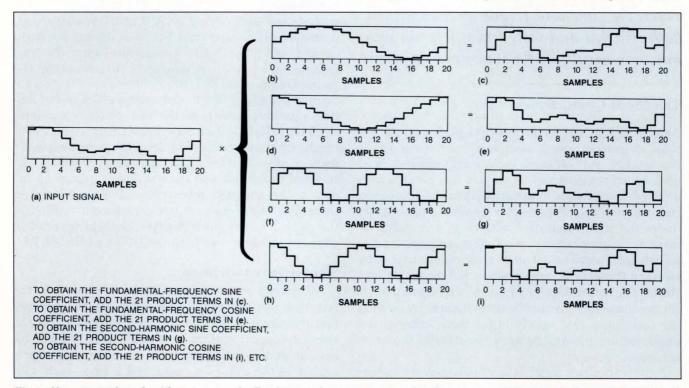


Fig 1—No matter what algorithm you use, the Fourier transform represents a signal as a summation of single frequency components. To begin the process of obtaining these components, multiply the data sequence of N points by sines and cosines at all significant harmonically related frequencies. To obtain the k^{th} sine coefficient, for example, you sum all N products that involve $\sin(k\omega t)$.

indicates the real part of a complex number, whereas the prefix "IM" denotes the imaginary part. A complex quantity, which is denoted by a variable name followed by an asterisk (*), is the complex conjugate of the same variable not followed by an asterisk; that is, if Q = RE(Q) + IM(Q), then $Q^* = RE(Q) - IM(Q)$.

Floating-point calculations abound

If you have acquired data samples at N points spaced equally in time, you can determine all the frequency components with the discrete Fourier transform. To do so, separately multiply the data by both the cosine and the sine of each of the N/2 frequencies that such data can contain. Therefore, to calculate each component of the Fourier frequency spectrum using the DFT algorithm, you must perform a total of N·N floating-point multiplications, and you must separately sum the N/2 cosine products and the N/2 sine products. As you take more samples to increase the spectrum resolution

```
THE DISCRETE FOURIER TRANSFORM: X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi nk/N} EULER'S IDENTITY: e^{j\theta} = \cos(\theta) + j\sin(\theta) COMBINING THE TWO EQUATIONS YIELDS: X_k = \sum_{n=0}^{N-1} x_n \left(\cos(2\pi nk/N) + j\sin(2\pi nk/N)\right) DFT ALGORITHM: for \ k = 0 \ to \ N-1 \\ trig_argument = 2*P!*k*n/N \\ DFT_output_RE(k) = DFT_output_RE(k) + \\ \cos(trig_argument)*input_data(n)/N \\ DFT_output_IM(k) = DFT_output_IM(k) - \\ sin(trig_argument)*input_data(n)/N \\ next \ n
```

Fig 2—The DFT uses Euler's identity to represent an exponential function as the sum of the sine and cosine terms.

or as you raise the sample rate to increase the Nyquist aliasing frequency (see **box**, "Sampling rate is the key to resolution"), the DFT calculation time increases approximately in proportion to the square of the number of samples taken.

This "calculation intensity" limits the usefulness of the DFT as the number of samples in a data sequence

Sampling rate is the key to resolution

When you're sampling data, the highest frequency that the DFT (or the FFT or the CZT) can measure is the Nyquist frequency or the Nyquist rate. The Nyquist frequency equals half of the sampling rate. If the data contains components at frequencies higher than the Nyquist rate, those components are aliased or undersampled. Unless you can use information that isn't present in the sampled data, the aliased terms appear as spurious frequency components and are indistinguishable from real data. Thus, the aliased terms corrupt the power calculations for lower frequencies.

To use the DFT, or any other Fourier analysis technique, you must limit the frequency content of the sampled data to less than the Nyquist rate. To measure higher frequencies, you must sample the data faster. The amount of data sampled deter-

mines the resolution of the spectrum. The spectrum is divided into N/2 frequency "bins;" hence, the spectrum resolution equals 2/N times the Nyquist frequency. To obtain better frequency resolution, you must take more samples.

To the DFT, data is periodic

The DFT also assumes that any data sequence it operates on is periodic. Therefore, any data sequence you analyze with the DFT, FFT, or CZT techniques must represent an integer number of periods of the sampled process. For example, to sample a 10-Hz sine wave, the sampling period (the time required to take one complete set of samples) must be an integer multiple of 1/10 sec. When you're analyzing broadband sources, there shouldn't be a large jump in value between the first and last samples. If such a

jump exists, the DFT sees it as a step in the data and incorrectly includes the step in the frequency analysis.

To eliminate the "end effect" of such a step, you must apply "windowing" to the sampled data. The raised-cosine filter, for example, provides this windowing function. The filter multiplies each data point by a cosine that has a dc offset and a phase shift. The endpoints of the window, which are at zero amplitude, correspond to the lowest points of the cosine. The objective is to soften or smooth the endpoints of the data and to minimize the effects of the edge. This smoothing, however, decreases the resolution of the frequency spectrum because it reduces the detail of the sampled data. In most analyses of sampled data, windowing is therefore used as a last resort.

The FFT operates on the same sampled data and produces the same results as the DFT.

becomes large. The DFT does let you calculate a single-frequency component, independent of other frequency calculations, though. This ability greatly increases the speed for analyses that involve only a single harmonic. However, single-frequency analyses are usually insufficient for actual sampled data, because the typical "spreading" of spectral components into adjacent frequency bins lets some harmonic power remain unaccounted for by the DFT. Hence, the DFT is either slow in calculating all the frequency components of an entire spectrum, or it's potentially misleading in calculating single frequencies.

A more common method used to calculate the power and phase vs frequency plot, the fast Fourier transform (FFT) "butterfly", utilizes the symmetry of the DFT calculation. The FFT operates on the same sampled data and produces the same results as the DFT method. The DFT, however, repeats a number of multiplications to determine the intermediate results for different frequencies. Operating with a technique referred to as "decimation in time," the FFT doesn't repeat calculations. As a result, the FFT produces the same results as does the DFT but in fewer operations. To obtain the inverse FFT, you can use a butterfly similar to the forward FFT's butterfly, or you can use the forward FFT algorithm to calculate the inverse FFT in the manner described for the DFT in Figs 3 and 4 (see box, "Simplify the inverse transform").

```
THE INVERSE DISCRETE FOURIER TRANSFORM:  X_n = \frac{1}{N} \sum_{k=0}^{N-1} X_k \ e^{+j2\pi kn/N}  EULER'S IDENTITY:  e^{j\theta} = cos(\theta) + jsin(\theta)  COMBINING THE TWO EQUATIONS YIELDS:  X_n = \frac{1}{N} \sum_{k=0}^{N-1} X_k \ (cos(2\pi kn/N) + jsin(2\pi kn/N))  INVERSE DFT ALGORITHM:  for \ k = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N-1   for \ n = 0 \ to \ N
```

Fig 3—The mathematics for calculating the inverse DFT, like those for the forward DFT, involve multiplication, summation, and the use of Euler's identity.

Simplify the inverse transform

The inverse of the discrete Fourier transform takes the real and imaginary components generated by the DFT and reconstructs the sampled data sequence. The form is very similar to that of the forward DFT (Fig 3). Essentially, the inverse DFT sums cosines and sines whose magnitudes are those of the real and imaginary DFT components. The result is a reconstructed data sequence. Fig 3 includes a pseudocode of the inverse DFT.

Alternatively, you can consider the inverse transform as the complex conjugate of the result of a DFT performed on the complex conjugates of a spectrum's real and imaginary frequency components (Fig 4). In this case, you can use any given forward DFT (or FFT or CZT) algorithm to calculate the inverse DFT. To do so, you must find the conjugates of the frequency terms, use the DFT, and find the conjugates of the result.

From Fig 5, you can see that N data points require log₂(N) stages in the FFT butterfly. Each stage performs N multiplications and additions. The FFT produces the spectrum of N data points by performing only N·log₂(N) floating-point operations. Although this algorithm is more complicated than the DFT is, the FFT requires fewer multiplications and is much more efficient for large values of N. The FFT usually requires the same memory storage as does the DFT: an array for the input data and an array for the output data.

Note that the butterfly is structured as a series of parallel operations in sequential stages. Because this structure is well suited to a parallel-pipelined processor architecture, it can further speed the calculation of the FFT. Unlike the DFT, however, the FFT algorithm can't independently calculate the value of a single frequency component; to obtain a single component using the FFT, you must calculate the entire frequency spectrum. For examples of the FFT and the inverse FFT code, see **Ref 2**.

The major limitation of the FFT algorithm is that it frequently requires data sequences that contain an inconvenient number of samples. For example, if you employ the widely used Cooley-Tukey FFT algorithm (**Ref 2**), the length of the data sequence must be an integer power of two for the butterfly to have an inte-

ger number of stages. To analyze captured data, you must adjust the sampling frequency and the data-sequence size to accommodate this restriction.

When you choose a sample size, you must make sure that the sequence of samples in the captured data exactly spans an integer number of wave periods. In addition, you must select either the sample rate or the resolution of the calculated spectrum. For example:

 $f_i = \text{frequency of input wave} = 1020 \text{ Hz},$

 $f_s = sample frequency = 8000 samples/sec,$

 $f_{res} = frequency resolution,$

p=number of sampled input-wave periods (must be an integer), and

N = sample size (must also be an integer).

By definition, $f_{res} = f_s/N = 8000 \text{ sec}^{-1}/N$. You can determine the required integer number of input-wave periods as follows: $f_i = p \cdot f_{res} = 1020 \text{ Hz}$. Combining the two

equations yields p.8000/N = 1020. Rewriting the last equation and reducing the ratio simplifies the equation to N = p.8000/1020 = p.400/51 or N/p = 400/51, where N = 400 and p = 51. Note that 400 and 51 have no common factors. Thus, the smallest sample size that samples an integer number of input-wave periods is 400 samples over 51 input-wave periods.

If you use the FFT, your sample size must be an integer power of two; if it isn't, you have a few alternatives. Your first choice is to collect extra samples—make the number of samples in the set equal the next larger integer power of two—and "window" them. (Windowing, which is discussed in greater detail in the box, "Sampling rate is the key to resolution," is a data-smoothing technique usually used as a last resort.) Your second option is to lower the sampling frequency. However, doing so reduces the resolution of the frequency spectrum.

For instance, in the previous example, the process

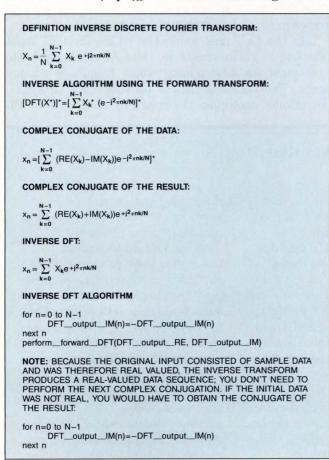


Fig 4—You can use the forward DFT to obtain the inverse DFT by taking conjugates of complex quantities.

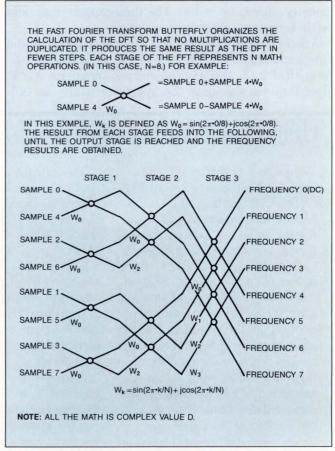


Fig 5—To understand the operations involved in calculating a DFT, you can use this butterfly diagram as a guide.

The FFT produces the spectrum of N data points by performing only $N \cdot \log_2(N)$ floating-point operations.

that produces the sampled data requires 400 samples. Because 400 isn't an integer power of two, you can extend the data-collection interval to more than 65 input-wave periods so that you can collect 112 extra samples for a total of 512 samples (that is, 29), without affecting the sampling rate. However, because the samples no longer cover an integer number of inputwave periods, you must employ windowing. Alternatively, you can compromise the test and use only 256 samples (28) that are spaced further apart in time. Or, if your A/D converter permits, you can take samples that are spaced closer in time than the samples you originally planned to use. Because the resolution of the frequency spectrum is defined as the sample frequency divided by the number of samples, the FFT sets the maximum resolution of the measured spectrum. In short, if you use the FFT, you may have to either use a longer-than-minimum data-acquisition time (or use a faster and more expensive A/D converter than you would otherwise need) and therefore waste capturememory space, or reduce the data-capture rate and settle for poorer spectrum resolution.

Another algorithm that you can use to compute the power and phase vs frequency plot is the chirp-Z transform (Ref 2, 3, and 4). The chirp-Z-transform (CZT) algorithm can calculate the spectrum nearly as effi-

ciently as the FFT. Furthermore, the CZT lets you use data sequences with any number of samples. The CZT operates on the same sampled data as do the DFT and the FFT. All three algorithms produce equivalent results. However, the CZT doesn't force you to choose a data-sequence length that suits the limitations of the mathematics; it lets you select a sequence length that meets the requirements of both the device under test and the desired resolution of the spectrum. (For the details of the calculations, see box, "CZT calculations don't have to be convoluted.")

The chirp-Z transform rewrites the DFT as a convolution and performs the mathematical operations much as the FFT does. Although the CZT requires capture memory only for the number of captured samples, the algorithm does require CPU memory for two arrays. Each array must be an integer power of two in length and must include enough elements to contain all the samples in the acquired data sequence. For example, if the data sequence contains 3000 samples, the internal arrays must each contain 4096 elements.

Like the FFT (and unlike the DFT), the CZT must calculate an entire spectrum; the CZT doesn't provide a shortcut for determining single frequency components. The CZT executes a forward FFT (Nlog₂(N) operations), multiplies the result by a set of N coeffi-

CZT calculations don't have to be convoluted

The chirp-Z transform (CZT) uses the identities shown in Fig 6. The CZT expands the DFT's exponential argument into a polynomial, breaks it into separate terms, and moves the independent weighting factor (Wk in Eq 1 in Fig 6) outside the summation. Remaining inside the summation are the product of the data sequence, another weighting factor similiar to the first, and an exponential function with a difference term in its argument. As an examination of Fig 6 indicates, the correct defininition of terms reveals that the summation performs a convolution of the second two terms.

The chirp-Z algorithm gets part of its name from the last term's similarity to a "chirp" (a sine wave of increasing frequency—traditionally used to test the response of a device or a system). The "Z" comes from the chirp-Z's ability, when generalized, to calculate an arbitrary Z-transform (Refs 3 and 4). In this case, the particular Z-transform calculated is the Fourier transform.

Because you can evaluate a convolution by multiplying the Fourier transforms and calculating the inverse transform of the product, you can implement the CZT by using convolution. To do

so, you add zeros to "pad out" the data sequence and the coefficients to the power-of-two length required by the efficient FFT algorithm, calculate the transforms, find their product, and calculate the inverse transform. You then truncate the resultant sequence to the length of the original sampled-data sequence and obtain a DFT sequence of arbitrary length. The CZT avoids the lengthy time penalty associated with the DFT by using the highly optimized Cooley-Tukey FFT algorithm. Because the FFT algorithm is available on almost every computer system, you can easily utilize the efficient CZT.

cients (N operations), computes an inverse FFT of the result ($Nlog_2(N)$ operations), and multiplies this intermediate result by a scalar quantity (N operations). The entire calculation requires $2 \cdot N(1 + log_2(N))$ operations, which is about twice the number of floating-point operations needed to compute an FFT. Calculating a CZT requires far fewer operations than does calculating a DFT, though. (See **Table 1** for examples of typical execution times.) The inverse CZT must be computed using the forward CZT algorithm, as described for the DFT. (See **box**, "Simplify the inverse transform".)

The chirp-Z-transform technique evaluates the DFT by convolving the data sequence with a precalculated

set of coefficients. The length of the convolved sequence is an arbitrary value greater than or equal to the length of the data sequence. It's convenient to make the length of the convolved sequence equal to an integer power of two. The optimal value is the smallest such power of two that's equal to or larger than the number of samples in the data sequence. Because convolution in the time domain is equivalent to multiplication in the frequency domain, you can calculate the DFT by following these steps:

1. Calculate the coefficients—the V_k terms shown in Fig 6 and in the pseudocode of Listing 1.

TABLE 1—TIME CALCULATION EXAMPLES

ASSUME THAT YOUR ANALYSIS SUGGESTS THAT 400 8-BIT SAMPLES TAKEN AT A RATE OF 8000 SAMPLES/SEC ARE NEEDED TO CHARACTERIZE THE OUTPUT OF A DEVICE. A PROCESSOR CAPABLE OF 2M FLOATING-POINT OPERATIONS/SEC (M FLOPS) IS AVAILABLE TO CARRY OUT THE ANALYSIS OF THE CAPTURED DATA. ALL ALGORITHMS USE ROUGHLY THE SAME AMOUNT OF PROCESSOR MEMORY.

(a) DFT

 400 SAMPLES/8000 SAMPLES/SEC
 = 50 nSEC

 400×400 OPERATIONS/2M FLOPS
 = 80.0 nSEC

 TOTAL
 = 130.0 mSEC

 CAPTURE MEMORY USED
 = 400 BYTES

APPROXIMATE CPU MEMORY = 800 FLOATING-POINT QUANTITIES (FLOATS)

(b) FFT OF THE NEXT LARGER POWER OF TWO WITH WINDOWING (NOTE: LOG IS LOGARITHM BASE 2)

 512 SAMPLES/8000 SAMPLES/SEC
 =
 64 mSEC

 512log(512) OPERATIONS/2M FLOPS
 =
 2.3 mSEC

 TOTAL
 =
 66.3 mSEC

 CAPTURE MEMORY USED
 =
 512 BYTES

 APPROXIMATE CPU MEMORY
 =
 1024 FLOATS

(c) CHIRP-Z TECHNIQUE

 400 SAMPLES/8000 SAMPLES/SEC
 =
 50 mSEC

 2×512log(512) OPERATIONS/2M FLOPS
 =
 4.6 mSEC

 TOTAL
 =
 54.6 mSEC

 CAPTURE MEMORY USED
 =
 400 BYTES

 APPROXIMATE CPU MEMORY
 =
 1024 FLOATS

ASSUME THAT YOUR ANALYSIS SUGGESTS THAT YOU SHOULD TAKE 800 SAMPLES AT A RATE OF 8000 SAMPLES/SEC TO CHARACTERIZE THE OUTPUT OF A DEVICE. A 5M-FLOP PROCESSOR IS AVAILABLE TO CARRY OUT THE ANALYSIS OF THE CAPTURED DATA. ALL ALGORITHMS USE ROUGHLY THE SAME AMOUNT OF PROCESSOR MEMORY.

(a) DFT

 800 SAMPLES/8000 SAMPLES/SEC
 = 100 mSEC

 800×800 OPERATIONS/5M FLOPS
 = 128 mSEC

 TOTAL
 = 228.0 mSEC

 CAPTURE MEMORY USED
 = 800 BYTES

 APPROXIMATE CPU MEMORY
 = 1600 FLOATS

(b) FFT OF THE NEXT LARGER POWER OF TWO WITH WINDOWING

 1024 SAMPLES/8000 SAMPLES/SEC
 =
 128 mSEC

 1024log(1024) OPERATIONS/5M FLOPS
 =
 2.0 mSEC

 TOTAL
 =
 130.0 mSEC

 CAPTURE MEMORY USED
 =
 1024 BYTES

 APPROXIMATE CPU MEMORY
 =
 2048 FLOATS

(c) CHIRP-Z TECHNIQUE

ECHNIQUE

800 SAMPLES/8000 SAMPLES/SEC = 100 mSEC

3×1024log(1024) OPERATIONS/5M FLOPS = 6.1 mSEC

TOTAL = 106.1 mSEC

CAPTURE MEMORY USED = 800 BYTES

APPROXIMATE CPU MEMORY = 2048 FLOATS

LISTING 1

PSEUDOCODE EXAMPLE OF THE CHIRP-Z TRANSFORM

GENERATE THE COEFFICIENTS:

for i=0 to N-1
W(i)=cos(M_PI * i * i/N)+j * sin(M_PI * i * i/N)
V(i)=cos(M_PI * i * i/N)-j * sin(M_PI * i * i/N)
next i

for i=N to L $V(i)=cos(M_PI*(L-i)*(L-i)/N)+j*sin(M_PI*(L-i)*(L-i)/N)$ next i

Take_complex_FFT_of_V_length_L:

for i=0 to N-1
Y(i)=input__data(i) * W(i)
next i

Take_complex_FFT_of_Y_length_L:

for i=0 to L G(i)=Y(i) * V(i) next i

Take_inverse_FFT_of_G_length_L:

for i=0 to N output_data(i)=G(i) * W(i) next i

NOTES:

1. ALL MULTIPLICATIONS AND FFTs ARE FOR COMPLEX DATA.

2. N=LENGTH OF THE DATA SEQUENCE.

3. L=THE NEXT-LARGER-THAN-N POWER OF 2 (FOR EXAMPLE, IF N=400, L=512).

4. i=A LOOP COUNTER OR AN INDEX.

5. G=AN INTERMEDIATE ARRAY.

DFT DEFINITION:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N}$$

POLYNOMIAL EXPANSION:

 $nk=[n^2+k^2-(k-n)^2]/2$

REWRITTEN DFT:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi n^2/2N} e^{-j2\pi k^2/2N} e^{j2\pi (k-n)^2/2N}$$

EQUATION 1:

$$X_k = e^{-j2\pi nk^2/2N} \sum_{n=0}^{N-1} x_n e^{-j2\pi n^2/2N} e^{j2\pi(k-n)^2/2n}$$

DEFINITION OF TERMS: y_n = x_ne -j2 x n²/2N

 $V_n = e^{-j2\pi n^2/2N}$

 $V_k = \Phi[v_n]$

 $W_k = e^{-j2\pi k^2/2N}$

CHIRP-Z TRANSFORM:

$$X_k = W_k \sum_{n=0}^{N-1} y_n v_{(n-k)}$$

 $X_k = W_k[y_n \cdot v_n]$

 $X_k = W_k \Phi^{-1} [V_n \Phi[y_n]]$

Fig 6—The chirp-Z transform involves convolution in the time domain—an operation that's analogous to multiplication in the frequency domain.

- 2. Multiply the input data by the appropriate weighting factors—the W_k terms in Eq 1 in Fig 6 (see Fig 7 also). Pad the coefficients and the data with zeros and calculate the FFT.
- 3. Multiply the FFT by the coefficients (V_k values) that you calculated in step 1.
- 4. Calculate the inverse FFT of the result.
- 5. Multiply the inverse FFT by the weighting factor; ignore any extra data.

Note that for a given data-sequence length, the coefficients and the weighting remain constant; you don't need to recalculate the coefficients or the weighting. Listing 1 presents a possible implementation of these steps in pseudocode.

A few extra calculations yield many benefits

The chirp-Z method requires approximately twice the number of mathematical operations as does the FFT. However, the number of operations that both methods require is proportional to N·log₂(N) (Ref 4). Because you can often perform the spectrum analysis while you're acquiring new data, the time required to perform the chirp-Z transform may not be significant. Compared with the CZT, the FFT may require a larger number of samples to completely characterize the spectrum of a data sequence. For low sampling rates, taking these additional samples can greatly increase the acquisition time (Table 1). As the size of the sample-set



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The CZT algorithm can calculate the spectrum nearly as efficiently as the FFT, and the CZT lets you use data sequences with any integer number of samples.

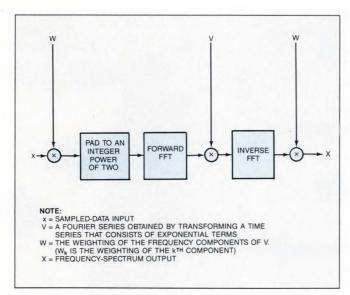


Fig 7—The process of performing a CZT calculation illustrates that the price you pay for the CZT's flexibility is the use of twice as many mathematical operations as does an FFT calculation.

TABLE 2—SUMMARY OF CZT, DFT, AND FFT CHARACTERISTICS

ALGORITHM	SAMPLE SIZE (N)	EXECUTION TIME (NUMBER OF OPERATIONS)	RESOLUTION		
DFT	ANY	N•N (SLOW)	ANY		
FFT	INTEGER POWER OF TWO	Nlog N (FAST)	LIMITED BY SAMPLE-SIZE RESTRICTIONS		
CZT	ANY	2Nlog N (FAST)	ANY		

NOTES:

- 1. THE CZT CAN OPERATE ON A DATA SEQUENCE OF ANY LENGTH.
- THE RESOLUTION OF THE CZT IS DETERMINED BY THE LENGTH OF THE DATA SEQUENCE; HENCE, WINDOWING, WHICH CAUSES RESOLUTION LOSS AND SPECTRUM SPREADING, ISN'T NECESSARY.
- 3. THE CZT RETAINS NEARLY THE SPEED OF THE FFT.
- TYPICALLY, THE CZT USES APPROXIMATELY THE SAME AMOUNT OF PROCESSOR MEMORY AS THE DFT AND THE FFT.
- 5. THE RESULTS OF THE CZT ARE MATHEMATICALLY IDENTICAL TO THOSE PRODUCED BY THE DFT AND THE FFT.

increases, the FFT's requirement that the number of samples in the set be an integer power of two can force you to use significantly larger data sets. The larger data sets, in turn, require significantly more capture memory. The CZT uses the available data and calculates a spectrum at the full resolution of that data.

The CZT algorithm calculates a DFT on a data sequence of any length by using FFT algorithms that are present in any good library of mathematical subroutines. Using the CZT algorithm doesn't significantly

slow down or increase the complexity of a spectrum calculation or increase the use of memory. (See Table 2.) The CZT, the DFT, and the FFT produce identical results; any differences will be smaller than the mathematical error limits of the computer on which you implement these algorithms. Because the CZT accepts acquired data sequences of any length, it gives you the maximum flexibility in selecting sample rates, sample sizes, and spectrum resolution. If you use the CZT, instead of accepting undesirable tradeoffs associated with the mathematical requirements of the DFT or the FFT algorithms, you can select parameter values that let you rapidly and completely characterize the device under test.

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Author's biography

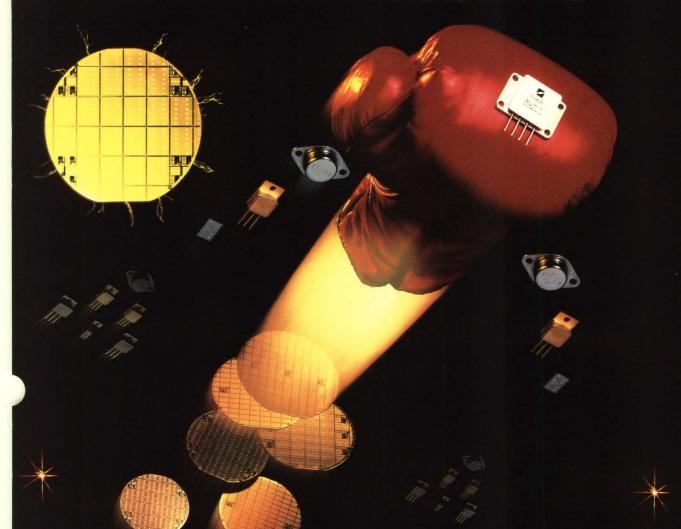
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0.021 - 0.21	95.0 - 39.0	380 - 156	9000 - 13000	360 - 675	0.738×0.585 (108)
0.04 - 0.40	83.0 - 20.5	332 - 82	4500 - 6500	160 - 370	0.588 × 0.388 (107)
0.20 - 1.30	26.0 - 8.5	104 - 34	1800 - 2950	60 - 130	0.414 × 0.254 (106)
0.30 - 2.40	18.5 - 5.0	74 - 20	1300 - 1800	45 - 105	0.290 × 0.250 (105)
0.65 - 4.20	11.0 - 3.0	44 - 12	650 - 950	20 - 55	0.199 × 0.203 (104)

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		*I _D (Amps) vs Package Style									
BV _{DSS} Volts	RDS(ON)	TO-3 [A]	TO-247 [B]	TO-254 [C]	MODULE [SAE][HBE] [HCE][PBE] [PCE]	F-PACK [AF] - [DF] TO-257 [G] TO-258 [H]	P _D Watts	C _{iss} pF (Max)	Q _g nC (Max)	** DIE NO. [D]	***APT PART NO.
1000	0.110				76.0[PCE]		1560	26000	1350	108	10011PCEN
1000	0.200				41.0[PBE]		800	13000	740	107	10020PBEN
1000	0.210				39.0[HCE]	40.0[DF]	830[F] 780[HCE]	13000	675	108	10021[]N
1000	0.400				20.5[SAE]	24.5[CF]	595[F] 400[SAE]	6500	370	107	10040[]N
1000	0.400				20.5[HBE]		400[HBE]	6500	370	107	10040[]N
1000	1.100	9.5	10.5			9.5[H]	310[B] 250[H]	2950	180	106	1001R1[]N
1000	1.300	8.5	10.0			9.0[H]	230[A]	2950	180	106	1001R3[]N
1000	2.000	6.0	7.0	5.5		1	240[B] 198[A]	1800	105	105	1002R[]N
1000	2.400	5.5	6.5	5.0			150[C]	1800	105	105	1002R4[]N
1000	4.000	3.9	4.4	3.6		3.3[G]	180[B] 150[A]	950	55	104	1004R[]N
1000	4.200	3.5	4.0	3.3		3.0[G]	125[C] 100[G]	950	55	104	1004R2[]N
900	0.110			-	76.0[PCE]	5.5[5]	1560	26000	1350	108	9011PCEN
900	0.200				41.0[PBE]		800	13000	740	107	9020PBEN
900	0.210				39.0[HCE]	40.0[DF]	830[F] 780[HCE]	13000	675	108	9021[]N
900	0.400				20.5[SAE]	24.5[CF]	595[F] 400[SAE]	6500	370	107	9040[]N
900	0.400				20.5[SAL]	2 7.0[01]	400[HBE]	6500	370	107	9040[]N
900	1.100	9.5	10.5		20.5[115]	9.5[H]	310[B] 250[H]	2950	180	106	9040[]N
900	1.300	8.5	10.0			9.0[H]	230[A]	2950	180	106	
900	2.000	6.0	7.0	5.5		9.0[11]		1800	105	105	901R3[]N
900	2.400	5.5	6.5	5.0			240[B] 198[A]	1800	105	105	902R[]N
	10-30-00-00-0					0.0(0)	150[C]	100000000000000000000000000000000000000	200000	-	902R4[]N
900	4.000	3.9	4.4	3.6		3.3[G]	180[B] 150[A]	950	55	104	904R[]N
900	4.200	3.5	4.0	3.3	04.0(005)	3.0[G]	125[C] 100[G]	950	55	104	904R2[]N
800	0.080				91.0[PCE]		1560	26000	1350	108	80M80PCE
800	0.150				47.0[PBE]		800	13000	740	107	8015PBEN
800	0.160				45.0[HCE]	47.0[DF]	830[F] 780[HCE]	13000	675	108	8016[]N
800	0.300				23.5[SAE]	29.0[CF]	595[F] 400[SAE]	6500	370	107	8030[]N
800	0.300				23.5[HBE]		400[HBE]	6500	370	107	8030[]N
800	0.750	11.5	13.0			11.5[H]	310[B] 250[H]	2950	130	106	8075[]N
800	0.900	10.5	12.0			10.5[H]	230[A]	2950	130	106	8090[]N
800	1.200	8.0	9.0	7.0			240[B] 198[A]	1800	105	105	801R2[]N
800	1.400	7.5	8.5	6.5			150[C]	1800	105	105	801R4[]N
800	2.400	5.0	5.5	4.5		4.3[G]	180[B] 150[A]	950	55	104	802R4[]N
800	2.800	4.5	5.0	4.0		4.0[G]	125[C] 100[G]	950	55	104	802R8[]N
750	0.080				91.0[PCE]		1560	26000	1350	108	75M80PCEN
750	0.150				47.0[PBE]		800	13000	740	107	7515PBEN
750	0.160				45.0[HCE]	47.0[DF]	830[F] 780[HCE]	13000	675	108	7516[]N
750	0.300				23.5[SAE]	29.0[CF]	595[F] 400[SAE]	6500	370	107	7530[]N
750	0.300				23.5[HBE]		400[HBE]	6500	370	107	7530[]N
750	0.750	11.5	13.0			11.5[H]	310[B] 250[H]	2950	130	106	7575[]N
750	0.900	10.5	12.0			10.5[H]	230[A]	2950	130	106	7590[]N
750	1.200	8.0	9.0	7.0			240[B] 198[A]	1800	105	105	751R2[]N
750	1.400	7.5	8.5	6.5			150[C]	1800	105	105	751R4[]N
750	2.400	5.0	5.5	4.5		4.3[G]	180[B] 150[A]	950	55	104	752R4[]N
750	2.800	4.5	5.0	4.0		4.0[G]	125[C] 100[G]	950	55	104	752R8[]N
600	0.045				122.0[PCE]		1560	26000	1350	108	60M45PCEI
600	0.085				64.0[PBE]		800	13000	740	107	60M85PBEN
600	0.090	A			61.0[HCE]	63.0[BF]	830[F] 780[HCE]	13000	675	108	60M90[]N
600	0.170				32.0[SAE]	39.0[AF]	595[F] 400[SAE]	6500	370	107	6017[]N
600	0.170				32.0[HBE]		400[HBE]	6500	370	107	6017[]N
600	0.400	15.5	18.0			16.5[H]	310[B] 250[H]	2950	130	106	6040[]N
600	0.450	14.5	17.0			15.5[H]	230[A]	2950	130	106	6045[]N
600	0.600	11.5	13.0	10.5			240[B] 198[A]	1800	105	105	6060[]N
600	0.700	10.5	12.0	9.5			150[C]	1800	105	105	6070[]N
600	1.300	6.5	7.5	6.5		5.5[G]	180[B] 150[A]	950	55	104	601R3[]N
600	1.600	6.0	6.5	5.5		5.0[G]	125[C] 100[G]	950	55	104	601R6[]N

Notes:

*Package style is defined by letters in brackets (to be included in APT part number).

The only available package styles are those shown with specific values for lo (amps); IDM = 4 X ID.

**Die products are offered in individual die and whole wafer forms. Maximum continuous current (ID) for dice depends on packaging conditions (thermal resistance).

***Complete part number requires "APT" prefix and package style, i.e., APT1001R3BN (for package style [B]).

			* ID	(Amps) vs	Package Style	1					
BV _{DSS} Volts	RDS(ON) Ohms	TO-3 [A]	TO-247 [B]	TO-254 [C]	MODULE [SAE][HBE] [HCE][PBE] [PCE]	F-PACK [AF] - [DF] TO-257 [G] TO-258 [H]	P _D Watts	C _{iss} pF (Max)	Q _g nC (Max)	** DIE NO. [D]	*** APT PART NO.
550	0.045				122.0[PCE]		1560	26000	1350	108	55M45PCEN
550	0.085				64.0[PBE]		800	13000	740	107	55M85PBEN
550	0.090				61.0[HCE]	63.0[BF]	830[F] 780[HCE]	13000	675	108	55M90[]N
550	0.170				32.0[SAE]	39.0[AF]	595[F] 400[SAE]	6500	370	107	5517[]N
550	0.170				32.0[HBE]		400[HBE]	6500	370	107	5517[]N
550	0.400	15.5	18.0			16.5[H]	310[B] 250[H]	2950	130	106	5540[]N
550	0.450	14.5	17.0			15.5[H]	230[A]	2950	130	106	5545[]N
550	0.600	11.5	13.0	10.5	The state of the s		240[B] 198[A]	1800	105	105	5560[]N
550	0.700	10.5	12.0	9.5			150[C]	1800	105	105	5570[]N
550	1.300	6.5	7.5	6.5		5.5[G]	180[B] 150[A]	950	55	104	551R3[]N
550	1.600	6.0	6.5	5.5		5.0[G]	125[C] 100[G]	950	55	104	551R6[]N
500	0.030				152.0[PCE]		1560	26000	1350	108	50M30PCEN
500	0.055				80.0[PBE]	70.0/55	800	13000	740	107	50M55PBEN
500	0.060				76.0[HCE]	78.0[BF]	830[F] 780[HCE]	13000	675	108	50M60[]N
500	0.110				40.0[SAE]	49.0[AF]	595[F] 400[SAE]	6500	370	107	5011[]N
500	0.110	20.0	00.0		40.0[HBE]	04.00.0	400[HBE]	6500	370	107	5011[]N
500	0.250	20.0	23.0			21.0[H]	310[B] 250[H]	2950	130	106	5025[]N
500	0.300	18.0	16.0	13.0		19.0[H]	230[A]	2950 1800	130 105	106	5030[]N
500	0.400	13.0	14.0	11.5			240[B] 198[A]	1800	105	105	5040[]N
500	0.850	8.5	9.5	8.0		7.0[0]	150[C] 180[B] 150[A]	950	55	105	5050[]N
500	1.100	7.5	9.0	7.0		7.0[G] 6.5[G]	125[C] 100[G]	950	55	104	5085[]N 501R1[]N
450	0.030	7.5	3.0	7.0	152.0[PCE]	0.5[G]	1560	26000	1350	108	45M30PCEN
450	0.055				80.0[PBE]		800	13000	740	107	45M55PBEN
450	0.060				76.0[HCE]	78.0[BF]	830[F] 780[HCE]	13000	675	108	45M60[]N
450	0.110				40.0[SAE]	49.0[AF]	595[F] 400[SAE]	6500	370	107	4511[]N
450	0.110				40.0[HBE]	40.0[/11]	400[HBE]	6500	370	107	4511[]N
450	0.250	20.0	23.0			21.0[H]	310[B] 250[H]	2950	130	106	4525[]N
450	0.300	18.0	21.0			19.0[H]	230[A]	2950	130	106	4530[]N
450	0.400	14.5	16.0	13.0			240[B] 198[A]	1800	105	105	4540[]N
450	0.500	13.0	14.0	11.5			150[C]	1800	105	105	4550[]N
450	0.850	8.5	9.5	8.0		7.0[G]	180[B] 150[A]	950	55	104	4585[]N
450	1.100	7.5	9.0	7.0		6.5[G]	125[C] 100[G]	950	55	104	451R1[]N
400	0.021				183.0[PCE]		1560	26000	1350	108	40M21PCEN
400	0.040				95.0[PBE]		800	13000	740	107	40M40PBEN
400	0.042				92.0[HCE]	95.0[BF]	830[F] 780[HCE]	13000	675	108	40M42[]N
400	0.080				47.0[SAE]	58.0[AF]	595[F] 400[SAE]	6500	370	107	40M80[]N
400	0.080				47.0[HBE]		400[HBE]	6500	370	107	40M80[]N
400	0.200	22.5	26.0			23.5[H]	310[B] 250[H]	2950	130	106	4020[]N
400	0.250	20.0	23.0			21.0[H]	230[A]	2950	130	106	4025[]N
400	0.300	17.0	18.5	15.0			240[B] 198[A]	1800	105	105	4030[]N
400	0.400	14.5	16.0	13.0			150[C]	1800	105	105	4040[]N
400	0.650	10.0	11.0	9.0		8.5[G]	180[B] 150[A]	950	55	104	4065[]N
400	0.800	9.0	10.0	8.0	102 010051	7.5[G]	125[C] 100[G]	950	55	104	4080[]N
350 350	0.021				183.0[PCE]		1560 800	26000	1350	108	35M21PCEN 35M40PBEN
350	0.040				95.0[PBE] 92.0[HCE]	95 OF DET		13000 13000	740 675	107	
350	0.042				47.0[SAE]	95.0[BF] 58.0[AF]	830[F] 780[HCE] 595[F] 400[SAE]	6500	370	108	35M42[]N 35M80[]N
350	0.080				47.0[SAE] 47.0[HBE]	30.0[AF]	400[HBE]	6500	370	107	35M80[]N
350	0.000	22.5	26.0		47.U[TIDE]	23.5[H]	310[B] 250[H]	2950	130	107	3520[]N
350	0.250	20.0	23.0			23.5[H] 21.0[H]	230[A]	2950	130	106	3525[]N
350	0.300	17.0	18.5	15.0		21.0[11]	240[B] 198[A]	1800	105	105	3530[]N
350	0.400	14.5	16.0	13.0			150[C]	1800	105	105	3540[]N
350	0.400	10.0	11.0	9.0		8.5[G]	180[B] 150[A]	950	55	103	3565[]N
350	0.800	9.0	10.0	8.0		7.5[G]	125[C] 100[G]	950	55	104	3580[]N
200	0.000	0.0	10.0	0.0	257.0[PCE]	7.0[0]	1560	26000	1350	108	20M11PCEN
200	0.020				137.0[PBE]		800	13000	740	107	20M20PBEN
200	0.020				131.0[HCE]		780[HCE]	13000	675	107	20M20FBEN 20M21[]N
200	0.040				68.0[SAE]	83.0[BF]	595[F] 400[SAE]	6500	370	107	20M40[]N
200	0.040				68.0[HBE]	00.0[DI]	400[HBE]	6500	370	107	20M40[]N



[A] TO-3 (TO-204AA) $1.54 \times 1.050 \times 0.360$ Steel, Non-Isolated

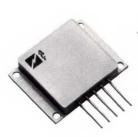
[B] TO-247 Plastic, Non-Isolated

TO-254 $0.845 \times 0.640 \times 0.208$ $0.800 \times 0.545 \times 0.255$ $0.655 \times 0.420 \times 0.185$ $0.800 \times 0.695 \times 0.255$ Hermetic, Isolated

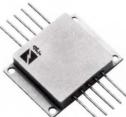
G TO-257 Hermetic, Isolated

TO-258 Hermetic, Isolated

[PBE] [HBE] $3.70 \times 1.34 \times 1.38$ Plastic, Isolated [HCE] [PCE] $4.25 \times 2.44 \times 1.457$ Plastic, Isolated



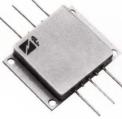
[AF] F-PACK (350-600V) $1.506 \times 2.006 \times 0.360$ Hermetic, Isolated



[BF] F-PACK (350-600V) $1.506 \times 2.006 \times 0.360$ Hermetic, Isolated



[CF] F-PACK (750-1000V) $1.506 \times 2.006 \times 0.360$ Hermetic, Isolated



[DF] F-PACK (750-1000V) $1.506 \times 2.006 \times 0.360$ Hermetic, Isolated

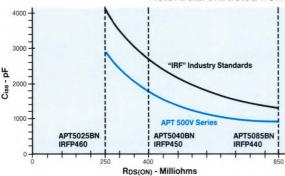


[SAE] $2.11 \times 1.44 \times 1.11$ Plastic, Isolated

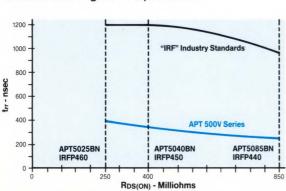
APT Power MOSFETs Provide the Most Efficient Electrical/Mechanical Designs

Comparisons of 500V APT and "IRF" Standard Parts for RDS(ON) vs Ciss, Qg, trr, and Rθic

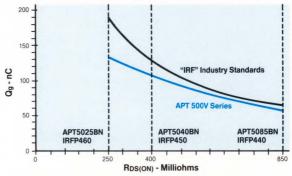
Note: Data extracted from current manufacturers' data sheets.



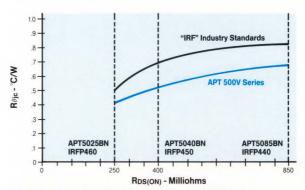
APT Advantages: Simpler, Less Costly Drive Circuits and Higher Frequencies.



APT Advantages: Lower Switching Losses, Lower Recovery Transients and Less Heat.



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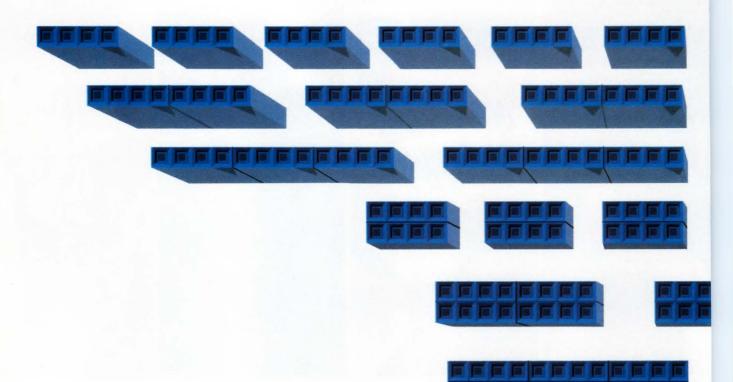
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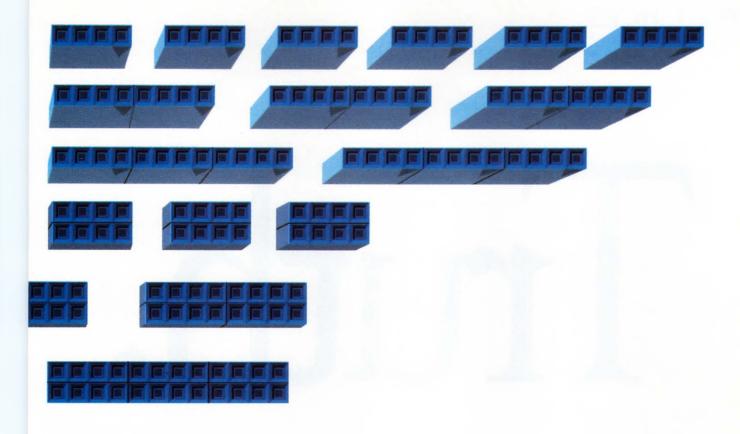
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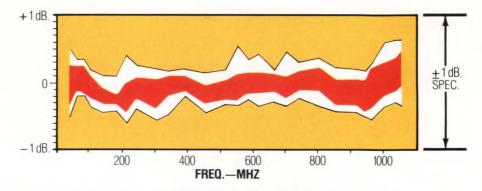
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6060B typical level accuracy vs. frequency at -127 dBm.

Sample: 38 units. Solid line: worst case. Shaded: Typical (75%).

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Fine-tuning $\mu P/\mu C$ code Part 1

Speed the execution of your \mu P/\mu C software

If you want your program to handle real-time interrupts, it will have to run fast; if you want to cram it into a PROM, you'll have to minimize the code size. You can't optimize your code for both conditions at the same time, however. This article, part 1 of a 2-part series, presents some coding techniques that will increase your code's execution speed. Part 2 will offer methods of decreasing the size of your code.

Peter S Gilmour, Motorola Inc

Optimizing program code for speed and optimizing it for size are mutually exclusive goals. The fastest code generally entails a large increase in code size. You may never need to optimize a whole program for speed, but there are sure to be occasions when you need to speed up routines that are heavily used by the rest of the program.

When execution speed is critical, your first line of attack will be to minimize the number of execution cycles needed to do the job. You can achieve this goal by picking the most time-efficient instructions from the instruction set of your μP ; by avoiding loops and subroutine calls, which introduce unproductive time overhead; and by using macros judiciously.

You'll make most of these improvements at the assembly-language level, although it's also useful to look at the C preprocessor in connection with macros. It's essential, therefore, that you become thoroughly familiar with all the details of the target processor's instruction set. You should obtain the manufacturer's reference card, which shows the complete instruction set as well as the number of execution cycles and the number of bytes for each instruction. On this card, use a highlighter to mark the instructions that have the fewest execution cycles. Those instructions will be the most useful for fine-tuning your code for maximum speed.

The fastest code is direct in-line code that contains no loops or subroutine calls. Loop overhead costs time, as does subroutine-linkage overhead. In fact, replacing subroutine calls or loops with in-line code is one of the easiest ways to achieve faster execution speed. For example, the fastest way to initialize a 128-byte memory area is to use 128 instructions to store the required value. Unfortunately, this method uses at least $128 \times N$ bytes of memory, where N is the number of bytes per instruction. For example, a Motorola MC6809 "store accumulator A" instruction (STA), using extended addressing, occupies 3 bytes and consumes five execution cycles. Thus, initializing a 128-byte area would take $128 \times 3 = 384$ bytes and consume $128 \times 5 = 640$ execution cycles.

If you use a loop to do the same job (Listing 1), the program must decrement a loop counter, test the counter, and branch back, 128 times. Each line of Listing 1 is numbered for easy identification, and the execution-cycle count (u) and number of bytes (b) for each

EDN May 25, 1989

You can optimize programs either for maximum execution speed or for minimum code size, but not both at once—these goals are mutually exclusive.

instruction are shown as part of the comments (each line of which is introduced by a semicolon).

The total number of cycles (u) and bytes (b) used is the sum of the loop initialization (lines 100 through 110) plus the loop itself (lines 120 through 140). Note that line 120 stores the initialization value and also autoincrements the buffer address in the X register, thus avoiding any need for a separate instruction to increment the address. The loop initialization uses 2+4=6 cycles and 2+4=6 bytes. The loop is traversed 128 times; a total of $128 \times (6+2+3) = 1408$ cycles and 5 bytes is used. Thus, initializing the memory area requires a grand total of 6+1408=1414 cycles and 6+5=11 bytes. You can see that the "in-line code" technique is about 55% faster than the loop, but consumes 3490% more memory, and is best used in timecritical, high-usage tasks, such as managing disk-I/O buffers, for which memory size is not critical.

Addressing mode affects efficiency

Using the most efficient addressing mode is a very important code-acceleration technique, so look first at the entries you've highlighted on the reference card. Indexed-addressing modes are generally (though not always) the most efficient. For example, if you were to replace the 128 extended-addressing STA instructions of the in-line code above with 128 "STA 0,X+" instructions plus an "LDX #BUFR" instruction for initialization, the totals would be $4+(128\times6)=774$ cycles and $4+(128\times2)=260$ bytes. In this case, indexed addressing would use 134 more cycles but 124 fewer bytes.

Most assemblers will automatically do some optimization of addressing modes if you give them sufficient information. For example, if the MC6809 assembler knows during the first pass that the operand will fit into one byte, it then generates a 2-byte instead of a 3-byte instruction. To take advantage of this kind of optimization, you have to follow the good programming

practice of placing all constant definitions (or equates) at the beginning of the source file. Some assemblers will even optimize the instruction itself, as the M68000-family assemblers do. For example, "MOVE.L #VALUE,D0" is assembled as "MOVEQ.L #VALUE,D0" when VALUE fits into one 8-bit, sign-extended byte. The "move quick" instruction (MOVEQ) is preferred because it is faster (4 cycles instead of 12) and shorter (2 bytes instead of 6). In this instance, you get both greater speed and smaller code size.

Another technique for obtaining faster execution is to keep operands in registers when possible. Registeraccess time is virtually instantaneous in comparison with memory-access time; therefore, keeping an operand in a register while you're manipulating it will help you avoid spending time on memory accesses. The improvement in execution speed will be particularly noticeable in a loop.

An implication of this technique is that you should preload all constants and do all the calculations you can outside the loop. The time wasted inside a loop by reloading a constant, or redoing a calculation that doesn't change, increases in proportion to the number of passes through the loop. If there aren't enough registers available to hold all the operands, it may be possible to consolidate multiple memory accesses into one. The loop shown in Listing 2a performs a transformation on all elements of an array (buffer) as shown by the comments in lines 120 through 130. This example of MC68000 code assumes that all addresses are of the long-word type (which is the worst case). To simplify the execution-cycle calculations, the example also assumes that there are zero wait states for all memory accesses.

An improved routine is shown in **Listing 2b**. The constant 22 is now loaded only once (line 10), outside the loop. Because neither VAR1 nor VAR2 is altered by the loop, these two values now become constants.

LISTING 1—INITIALIZATION VIA A LOOP (MC6809 CODE)

0100 0110		LDB LDX	#128 #BUFR	707 10 10	B= loop counter/buffer size X= buffer address
0120 0130	LOOP	STA DECB	0,X+	6u, 2u,	Store value & increment.
0140		BGT	LOOP		Process entire buffer.

The value of VAR2 is calculated outside the loop (line 30) and the result (v1-v2) is kept in a register (D2) for faster access (line 110). The loop-control structure is now of the "decrement-and-branch" (DBRA) type; it uses D3 as the loop counter. When D3.W decrements to -1 (\$FFFF), the loop will terminate, so the count must be set to the desired value minus one, as shown in line 40, which is outside the loop. Notice that the order of the register operands in line 140 is now interchanged, so that D1 does not have to be reloaded; the result of the unsigned-multiply instruction (MULU) is now placed into D0 and stored (line 150).

You'll see from the notes on **Listing 2** that both loops use the same number of bytes, but the optimized loop (**Listing 2b**) is 33% more efficient: It uses 50 fewer cycles per loop at a one-time cost of only 48 cycles for initialization. The total savings in cycles is the number

of cycles saved per loop, times the number of passes through the loop, minus the cycles required for initialization outside the loop, or $(50 \times BUFSZ)-48$. If the buffer size (BUFSZ) were 128 entries (words), the savings would be $(50 \times 128)-48$, or 6352 cycles.

Loop-control optimization

The preceding example illustrates an important fine-tuning technique: loop-control optimization. Comparing two addresses (line 160, **Listing 2a**), is a poor method of loop control. Generally speaking, a method that counts down to zero is more efficient, because most computers can easily test for the zero condition, whereas counting up to N requires a special "compare-to-N" instruction that is more costly in both size and speed. Another method that sometimes yields better loop control is to process the memory locations of the

LISTING 2A—BEFORE REGISTER OPTIMIZATION (MC68000 CODE) 0100 LOOP MOVE.W (A0), D0 ; 8u, 2b: Get old table entry. 0110 ADD.W VAR1, DO ;16u, 6b 0120 SUB.W VAR2, DO ;16u, 6b: Calculate new value. 0130 MOVE.W #22,D1 ; 8u, 4b: new = 22*(old+vl-v2)0140 MULU D0, D1 ;70u, 2b ; 8u, 2b: Store new entry. 0150 MOVE.W D1, (A0)+ 0160 #BUFR+BUFSZ,A0 ;14u, 6b CMPA.L 0170 LOOP BNE ;10u, 2b: Process entire buffer. Cycles/loop = 8 + 16 + 16 + 8 + 70 + 8 + 14 + 10 = 150 cycles = 2 + 6 + 6 + 4 + 2 + 2 + 6 + 2 = Bytes used 30 bytes

```
LISTING 2B—AFTER REGISTER OPTIMIZATION (MC68000 CODE)
0010
            MOVEO
                                 ; 8u, 2b: Set Dl.W= 22.
                     #22,D1
0020
            MOVE.W
                     VAR1, D2
                                 ;16u, 6b
                                 ;16u, 6b: Set D2.W= v1-v2.
0030
            SUB.W
                     VAR2, D2
0040
                     #BUFSZ-1,D3; 8u, 4b: Set D3.W= loop count.
            MOVE.W
0100
      LOOP
            MOVE.W
                     (A0), D0
                                 ; 8u, 2b: Get old table entry.
0110
            ADD.W
                     D2, D0
                                 ; 4u, 2b: Calculate new value.
                     D1, D0
0140
            MULU
                                 ;70u, 2b: new = 22*(old+vl-v2)
0150
            MOVE.W
                     DO, (AO)+
                                 ; 8u, 2b: Store new entry.
0170
            DBRA
                     D3, LOOP
                                 ;10u, 4b: Process entire buffer.
  Cycles/init = 8 + 16 + 16 + 8
                                                         48 cycles
  Cycles/loop = 8 + 4 + 70 + 8 + 10
                                                     = 100 cycles
                 2 + 6 + 6 + 4 + 2 + 2 + 2 + 2 + 4 =
```

EDN May 25, 1989

When execution speed is critical, select the most time-efficient instructions that will do the job at hand.

data in reverse order; that is, from high to low rather than the usual low to high. You'll need to analyze each loop to determine the most efficient method.

Listing 2b illustrates a most important point. All of these techniques for speeding execution have the maximum effect when you use them inside software loops. They're especially effective when you use them inside the innermost loops of a group of nested loops, because the innermost loops are executed the greatest number of times. Saving one execution cycle in a section of in-line code simply saves one execution cycle, which will hardly be noticed in the program's execution. But if you save one cycle in an inner loop that is executed a million times, you'll save one million execution cycles, which certainly will be noticed. Thus, to fine-tune a program for speed, you should first identify the inner loops and concentrate on making them faster to obtain the most noticeable improvements.

Be careful not to fall into the trap of testing for special conditions to save a few instruction cycles. If the special case does not occur frequently enough, the occasional savings will be more than eaten up by the cost of the test times the number of "misses." It is always more efficient to avoid special-condition testing and instead integrate the conditions into the algorithm. The moral here is this: If the algorithm requires special-case testing, you need a better algorithm.

One of the most powerful, but least used, fine-tuning techniques is instruction modification. In this technique, the program actually constructs an instruction based on current information and stores it in programmemory space, ahead of the current address, for later execution. Instruction modification is more risky than the other techniques because an error could cause the

program to go out of control.

It's impossible to modify code that is resident in ROM, so when you're writing firmware (ROM code), your routine must store the modifiable instructions in RAM. The RAM-resident, modifiable part of the code must terminate with an appropriate Jump or Return instruction that returns control to the ROM-resident part. The ROM-resident routine must contain facilities for constructing not only the modifiable instructions, but also the proper return instruction, in RAM.

Because of the inherently high risk, you must document self-modifying code very thoroughly and carefully. Use a unique and easily visible null expression (say, "0-0") in the operand field of every instruction that the program will modify. Make sure that self-modifying routines are thoroughly tested before you commit them to ROM, because self-modifying code is extremely difficult (and sometimes impossible) to debug. Sometimes, using self-modifying code is the only way to accomplish certain tasks—especially when the instruction set and/or register set of the MPU/MCU is limited—but you should avoid the technique unless it's absolutely necessary.

Listing 3 gives an example of instruction modification. This sample routine (written in MC6800 code) copies all bytes (FBUFSZ in number) from a source buffer (at location FBUFR) to a destination buffer (at location TBUFR). Because the MC6800 MPU has only one 16-bit index register (X), the routine modifies the instruction in line 140 so as to store data bytes to consecutive destination addresses. Line 140 includes the null expression "0-0" to denote instruction modification, but the expression also specifies the addition operation "+\$FFFF," so that the assembler will con-

LISTING 3—INSTRUCTION MODIFICATION (MC6800 CODE) 0100 LDX #TBUFR ; Init. TO buffer loca. 0110 STX TLOCA 0120 ; Init. FROM buffer loca. LDX #FBUFR 0130 LOOP LDA 0,X Get FROM data byte and 0140 STA 0-0+\$FFFF store into TO buffer. **** INTSTR. MODIFY **** 0150 TLOCA EQU *-2 0160 INC TLOCA+1 Incre. TO loca. 0170 BNE NOLSB 0180 INC TLOCA (do LS byte also!) 0190 NOLSB INX Incre. FROM loca. #FBUFR+FBUFSZ 0200 CPX 0210 BNE LOOP ; Exit when all data copied!

struct a 3-byte extended-address instruction. Failure to add the "+\$FFFF" would cause the assembler to construct a 2-byte direct-address instruction.

Lines 100 through 110 initialize the effective address portion of the instruction in line 140, because line 150 defines TLOCA as the address of the second byte of the 3-byte instruction in line 140. Lines 160 through 180 increment the destination address inside the instruction of line 140. The only alternative to using self-modifying code is to load/increment/save each buffer address in the X register for each loop iteration that moves a data byte; that procedure would contain more instructions and, because of the extra memory accesses involved, would also be slower than the self-modifying code.

One of the most efficient ways to generate in-line code is to use macros. Generally speaking, a macro is a named sequence of text that the assembler inserts into the assembly stream when it finds the macro name in the opcode field of a source-code line. The operand field may specify parameters that the macro body will process.

Macros tend to enlarge the code size, because each

time you invoke a macro, it inserts a predefined sequence of instructions into the assembly stream. By contrast, a code section that is structured as a subroutine appears only once in a program; however, it carries a penalty of subroutine-linkage overhead in the form of the call instruction, the return instruction, and the execution cycles consumed by these instructions, as well as by the storage and retrieval of the return address on the stack.

You'll probably want to use the macro form when execution speed is the primary consideration. You may prefer the subroutine form when the body of the subroutine is large, there are many calls to it, and space is the primary consideration. There are borderline cases, too, in which neither form yields a clear advantage; in such cases, you'll have to make your decision on the basis of all the circumstances.

Listing 4 gives an example of macro usage. This macro (written in M68000-family code) copies a block of bytes, words, or long words from a source address to a destination address. Lines 100 through 250 form the descriptive-comment header describing the COPY macro. The MACRO directive on line 260 defines a

```
LISTING 4—MACRO USAGE (M68000-FAMILY CODE)
0100
        Copy Memory Macro:
0110
0120
           Calling Sequence:
0130
                  COPY[. (size)]
                                    <source>, <destination>, <count>
                where: . <size>= is the optional data size
0140
0150
                                   parameter (size of items
                                   to copy), as follows;
0160
0170
                                      .B = byte
                                      .W = word
0180
                                      .L = long word (default)
0190
0200
                       <source>= "from" location address.
ination>= "to" location address.
                  <destination>= "to"
0210
                                          location address.
                         <count>= number of items to copy
0220
0230
0240
                             Destroys Al, A2, and D0!
0250
0260
      COPY
                 MACRO
0270
                 LEA
                            (®1),A1
                            (®2),A2
                 LEA
0280
0290
                 MOVEO
                            #(®3)-1,D0
0300
      ® a
                 MOVE. ®O
                            (A1)+,(A2)+
                            DO, ®@
0310
                 DBRA
                 ENDM
0320
                           JMP ROM, JMP RAM, JMP SIZE/2
0400
                 COPY.W
                           BLK ROM, BLK RAM, BLKSZ.L
0410
                 COPY.L
0420
                 COPY
                           ID ROM, ID RAM, ID SIZE.W
```

Loops and subroutine linkages entail a substantial time overhead, so when speed is vital, substitute macros and direct in-line code whenever possible.

macro named COPY. The macro body comprises the instructions in lines 270 through 310 and is terminated by the ENDM directive in line 320. The optional datasize parameter is denoted by "\0" in the macro body; "\1" denotes the source parameter, "\2" denotes the destination parameter, and "\3" denotes the count parameter.

Lines 270 through 290 set up the variables for the copy loop formed by lines 300 through 310, which moves the data. The parameters used in lines 270 through 290 are surrounded by parentheses to ensure that they will be evaluated properly in case a calling routine passes an expression as a parameter. The "-1" in line 290 is required because the DBRA instruction in line 310 terminates when D0.W decrements to -1 (\$FFFF), not 0. The "\@" in lines 300 through 310 references an assembler-generated label; that is, each invocation of the COPY macro generates a new, unique label.

Lines 400 through 420 are examples of how to invoke the COPY macro. Line 400 invokes the COPY macro to move a block of JMP_SIZE/2 words from location JMP_ROM to location JMP_RAM. Line 410 moves a block of BLKSZ.L long words from location BLK_ROM to location BLK_RAM; and line 420 moves a block of ID_SIZE.W words from location ID_ROM to location ID_RAM. Once you have fully debugged the COPY macro, these three lines will always generate error-free code.

Macros aid in productivity, speed, and maintenance

The use of macros has many advantages, among which are productivity, speed, and maintenance. They afford higher productivity because you need only debug the macro once; thereafter, each invocation of the macro will generate error-free code. This procedure conforms to the familiar structured-coding technique of debugging each module or subroutine before incorporating it in a program. Thus, macros not only eliminate repetitious entry of instructions (which are always subject to human error), but allow the programmer to concentrate more on the logic of the task at hand rather than on the details. That is, they allow the programmer to program at a higher level.

Macros give you better execution speed because they generate in-line code, whereas subroutines entail linkage overhead. And it's easier to maintain programs that use macros, because if the macro function changes, you fix only the macro itself, not all the separate occurrences of the code segment that performs that function.

A side benefit of using macros is that it's easy to port them to a new processor. Macros can be rewritten easily in the instruction set of the new target machine. Thus, macros isolate the function of the code from the processor resources with which you achieve that function. In rewriting macros, you can take advantage of new processor resources, such as additional registers. For example, a COPY macro written in MC6800 code could be rewritten in MC6809 code to take advantage of the second index register (Y) that the MC6809 provides. Conversely, you can cover up or work around disadvantages of the new target machine.

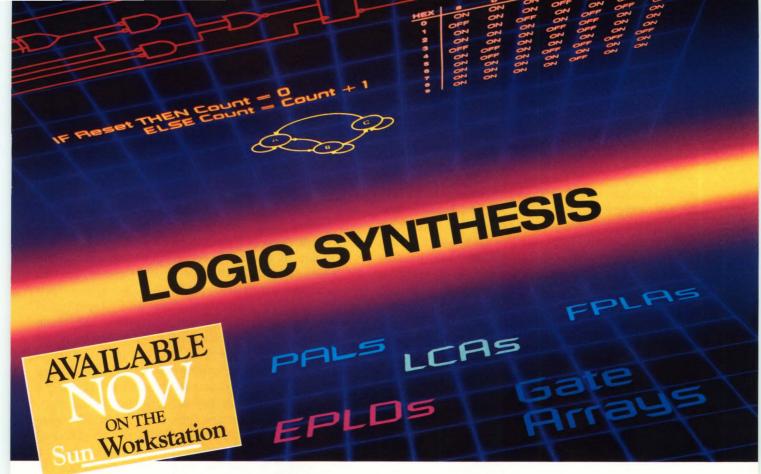
The C preprocessor provides macro facilities

When you're writing in the C language, you can create macros by means of the "#define" statement. The "#define" statement is a feature of the C preprocessor that performs text substitution; that is, it replaces the defined name with a string of characters. Normally the replaced characters terminate with the end of the line, but by using "\" as the last character of the line, you can continue the "#define" statement onward for as many lines as necessary.

Listing 5 gives an example of a C-language macro that mimics the MC68000 COPY macro (Listing 4). Lines 100 through 230 contain the descriptive-header comments for the COPY macro defined by lines 240 through 280. Line 240 starts the definition of the COPY macro and allocates three parameters, "from," "to," and "count". To ensure maximum efficiency, the copy function uses three register variables (fptr, tptr, i). Lines 250 through 260 initialize the source and destination pointers; the FOR loop (lines 270 through 280) does the actual copy work. Line 400 is an example of how you would use the macro. Note that although the call looks like a standard function call, the macro causes the preprocessor to generate in-line code for subsequent compilation.

In fact, some of the other speed techniques discussed here also apply to the C language. Calculating constants outside loops, recoding functions as macros, replacing loops with in-line code, and declaring heavily used variables (especially those inside loops) as register variables are all techniques that can make code execute faster. A good C compiler that has an efficient code optimizer may already make use of some of these techniques.

High-performance μPs, such as the MC68020 and MC68030, have built-in instruction and/or data caches with access times of 35 nsec or less (their main-memory



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DATA I/C Corporation Most assemblers will automatically do some optimization of addressing modes if you give them enough information.

access times are usually 100 nsec or more). Make sure that your program enables these caches, because they can dramatically improve the program's execution speed. Both the MC68020 and the MC68030 have 256 bytes of instruction cache; the MC68030 also has 256 bytes of data cache. When the instruction cache is enabled, loops that fit entirely within the cache will execute extremely fast because all of the instructions will be loaded into the cache during the first pass through the loop; subsequent passes don't have to spend any time at all on accessing the main memory. Likewise, data operands that are cached do not have to be refetched from main memory.

If the loop is longer than the available instruction cache (including prefetches), execution becomes somewhat slower. The reason is that by the time execution reaches the top of the loop for the second time, the instructions from the beginning of the loop have been replaced in the cache by others from a later portion of the loop. Thus, there will still be bus activity while the program is refetching the instructions for each iteration of the loop. However, refetching is minimized by the advanced pipeline architecture of the MC68020 and MC68030, which prefetch instructions into the cache and thereby cause future hits for in-line code.

The MC68030 has an additional feature that accelerates execution: burst-mode filling of the data and/or instruction caches. When burst filling is enabled and

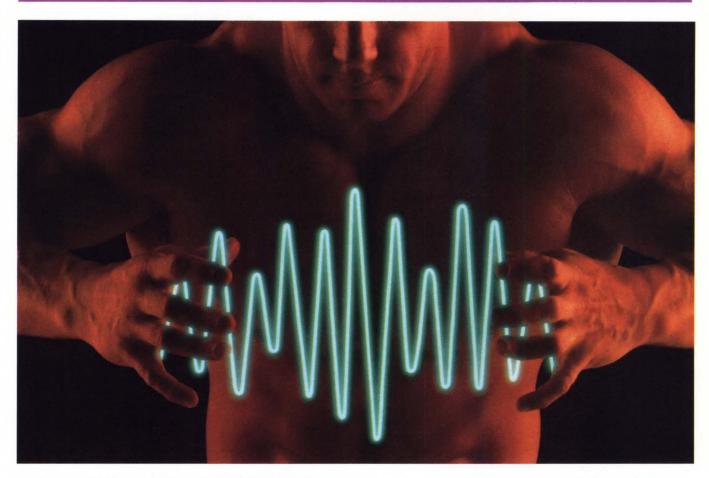
a cache miss occurs, the bus controller requests a burstmode fill operation. The responding device (which in this case is main memory) then supplies one to four long words (4 to 16 bytes) to be cached.

Because of the advanced design features of the MC68020 and MC68030 caches, you'll rarely need to exercise any external control over the caches—they work best if you leave them alone. In systems based on other processors, however, controlling the cache may improve system performance. For example, if you know how large the cache is, you can place a "freeze cache" instruction at an appropriate point inside a large loop to ensure that prefetches won't load the cache with instructions from beyond the end of the loop. This procedure eliminates time that would otherwise be lost in fetching instructions that won't be executed until the loop terminates. However, because the "freeze cache" instruction is usually a privileged instruction, you can use this technique only when the processor is in supervisor state. Supervisor-state routines, especially library routines, that use this technique can experience a significant increase in execution speed.

A less-obvious benefit is that using cache memory reduces external bus activity on the part of the processor. The reduction can be significant in systems that have multiple bus masters, or in tightly coupled multiprocessor systems, because more of the bus bandwidth

```
LISTING 5—C-LANGUAGE MACRO
0100
0110
       Copy Memory Macro:
0120
         Calling Sequence:
0130
               copy(source, destination, count);
0140
               0150
0160
0170
                     <count>= number of bytes to copy
0180
0190
                Uses the following variables;
0200
                                   *fptr, *tptr;
                    register char
0210
                    register int
0220
0230
                                    R
0240
      #define copy(from, to, count)
                                    R
0250
             fptr = (char *)from;
             tptr = (char *)to;
0260
0270
             for(i=count; i>0; i++)
                *tptr++ = *fptr++;
0280
0400
             copy(&jmp rom, &jmp ram, jmp size);
```

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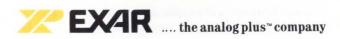
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Saving one cycle in in-line code won't be noticed; but if the cycle is in a loop, the saving is multiplied by the number of passes through the loop.

becomes available to the alternate bus masters.

Miscellaneous acceleration techniques

Another acceleration technique, albeit one that has somewhat limited usefulness, is to use registers as "switches." The program evaluates a switch value to determine which section of code is to be executed next, and places the starting address of that code section in an index register. The operation is similar to that of the C-language "switch" or Basic ON . . . GOTO statement. When the switch value is a constant for the duration of a loop, the program should evaluate the switch value outside the loop and preload the destination address of the switch into a register. This procedure saves the time that would otherwise be wasted in re-evaluating the switch value during each loop iteration, at the cost of one dedicated index register. If the switch value was already in a register, the procedure will free that register for other uses during the loop. In systems based on the MC68000 family, the procedure would usually free up a data register (Dn) for the cost of an address register (An). Because MC68000 code tends to use up all the data registers before using up all the address registers, this technique may prove useful in special situations.

Select the fastest algorithm for the job at hand

All the code-optimization techniques in the world won't produce the maximum possible throughput if you're applying them to inherently slow or inefficient algorithms. If that is the case, time spent searching in computer and/or math books for a better algorithm may bring far greater rewards than painstaking codetweaking. For example, the bubble-sort algorithm is simple and compact, but if you use it to sort more than 50 items or so, it's notoriously slow in comparison with other sorting algorithms.

You have several tradeoffs to consider when you're trying to select the best algorithm for the job at hand. The first tradeoff is the complexity of the algorithm versus the amount of data it must process and the frequency with which the application will use it—the efficiency of a given algorithm may not become apparent until the quantity of data per pass reaches a certain level.

Another tradeoff will be efficiency versus versatility. For example, the Quicksort algorithm far outperforms most others for large random lists, but its worst-case performance (on mainly sorted data) is not much better than that of the bubble sort. You can optimize it for

mainly random or mainly sorted input, but not both. If you don't know what kind of data the sort will have to handle, you may want to use a less-sensitive algorithm such as the Shell-Metzner sort. This algorithm doesn't yield the best-case speed of the Quicksort, but its worst-case speed is only a small percentage lower than its best-case speed, and its shorter, less-complex code makes it worthwhile even for short lists (those having a few tens of elements).

Finally, you should check to see that the instruction set of the target machine doesn't make it awkward to implement the algorithm you'd like to use. If the algorithm and the instruction set don't make a good match, look for another algorithm. An algorithm that would make better use of the same instruction set will probably prove faster.

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Author's biography

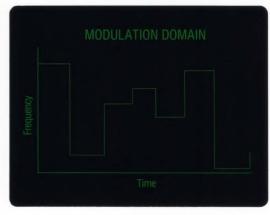
Peter S Gilmour is a senior systems analyst at the Motorola Microprocessor Group (Austin, TX) where he currently works on the company's HDS-300 line of real-time emulators. He holds a BS in engineering from Case Institute of Technology and an MS in engineering from Arizona State University. Peter's interests include tennis, golf, and personal computing.



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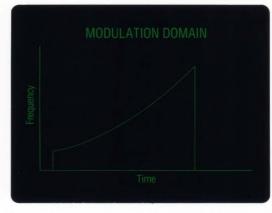




hop

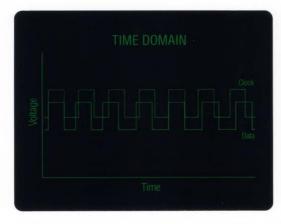
...a time-domain view of a frequency-agile signal (left) reveals little useful information. The new modulation-domain view on the right clearly shows the hopping sequence, settling times, and channel frequencies.





chirp

...no quantitative data is available from the time-domain view of a radar chirp on the left. However, the frequency vs time display of this single-shot event clearly shows chirp linearity and frequency.





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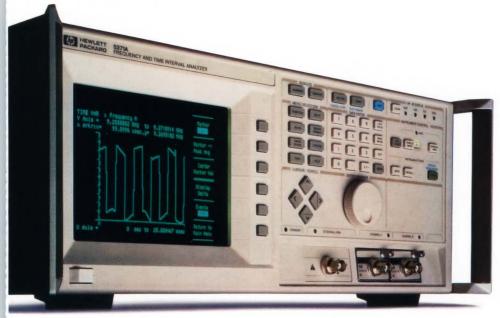
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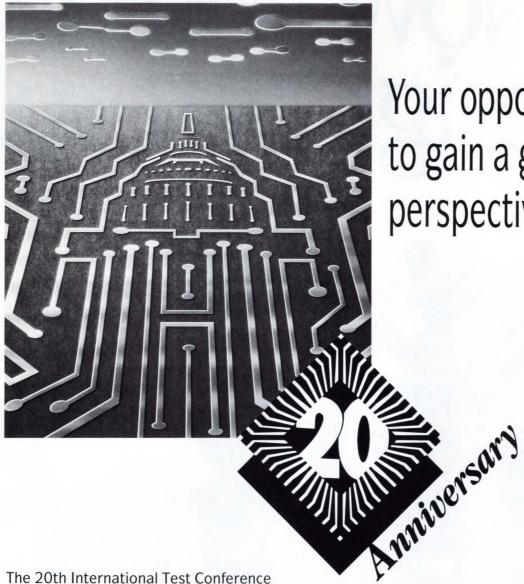
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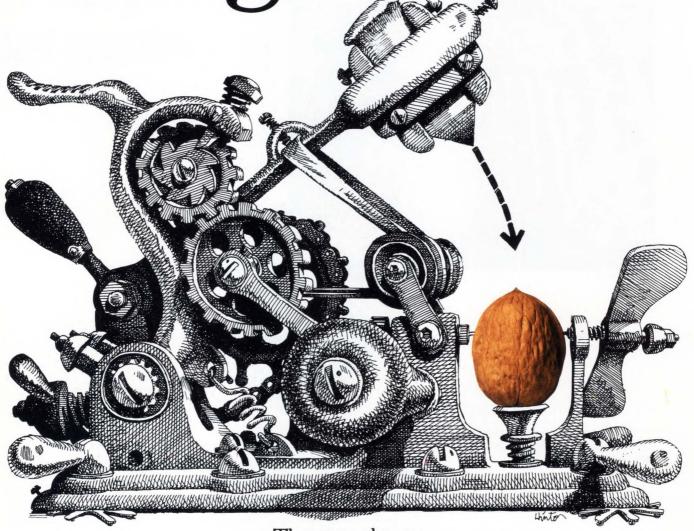
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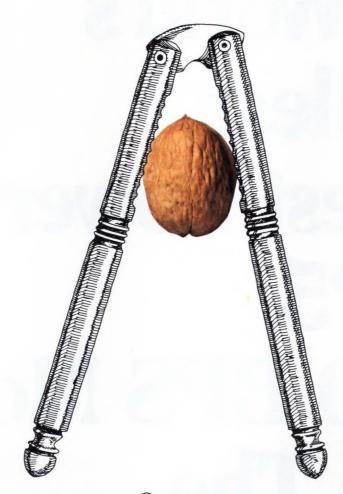
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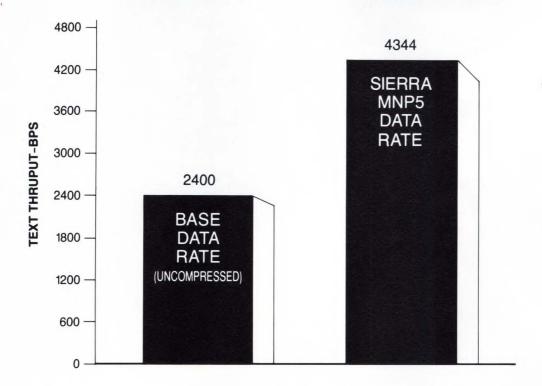
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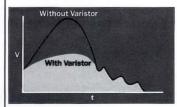
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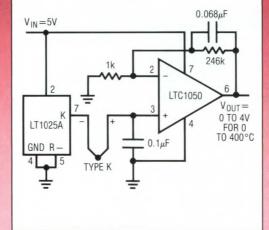
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DESIGN IDEAS

EDITED BY CHARLES H SMALL

Photoconductor closes AGC loop

John Forte Motorola Information Systems, Brampton, Ontario, Canada

The circuit shown in Fig 1 uses a photoconductor isolator to perform automatic gain control over a dynamic range of 60 dB. Amplifier IC₁ and the CLM51 photoconductor operate as a voltage-controlled amplifier (VCA); the control voltage is $V_{\rm AGC}$. The resistance of the CLM51 is inversely proportional to the current driven through its LED. The 2.2-M Ω resistor in the feedback path of IC₁ prevents the feedback path from opening and causing instability. This large resistance also puts an upper limit on the gain of the VCA. IC₂ and diodes D_1 and D_2 perform full-wave rectification of the output signal.

 IC_3 is an integrator; to describe it's operation, it's best to consider input currents rather than the input voltage. When I_1 is too high—that is, V_{LVL} is too high— C_1 charges up, causing V_{AGC} to go more negative. This V_{AGC} change causes more current to flow through the LED, which in turn causes the resistance of the CLM51 and the gain of the VCA to decrease. Likewise, if I_1 is too low—that is, V_{LVL} is too low— C_1 will charge in the opposite direction, which eventually causes the gain of the VCA to increase. When V_{LVL} is such that

 $I_1 = I_2$, C_1 will maintain its charge to keep the gain of the VCA constant.

You can adjust the output level of the AGC circuit by varying R_{LVL} according to the following equation: $R_{\text{LVL}}{\approx}(V_{\text{OUT}}/6)(220\times10^3\Omega/12V).$

Using the components shown in Fig 1, the circuit maintains an output voltage of 350 mV_{RMS} over a 60-dB range. The I/O measurements in Table 1 were taken with an input signal of 5 kHz with respect to 600Ω ; therefore, $0 \text{ dBm} = 775 \text{ mV}_{rms}$.

To Vote For This Design, Circle No 746

INPUT (dBm)	OUTPUT (dBm)
12.5	-3.5
10.0	-3.5
0.0	-3.5
- 10.0	-3.5
-20.0	-3.5
-30.0	-3.5
-40.0	-3.5
-50.0	-3.5
-60.0	- 12.5

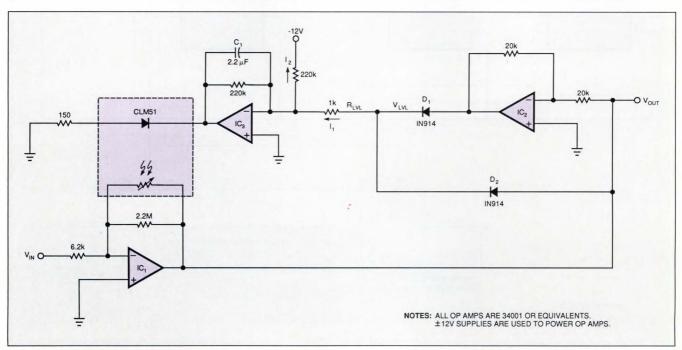


Fig 1—A photoconductor provides the feedback for this AGC circuit. The CLM51's resistance is inversely proportional to the current passed through it, which is in turn dependent on V_{AGC} .

EDN May 25, 1989

Digital pot simulates strain gauge

T G Barnett The London Hospital Medical College, London, UK

The circuit shown in Fig 1 simulates small strain-gauge resistance changes, thus enabling you to test strain-gauge amplifiers simply. It's particularly useful in multichannel systems in which each channel has separate gain and offset controls.

The circuit implements a controlled resistance network and is centered around IC3, a digitally controlled solid-state potentiometer from Xicor Inc (Milpitas, CA). The control circuit consists of a 10-Hz crystal oscillator, IC1, which drives both the 12-stage ripple-carry binary counter, IC2, and the increment terminal of the X9102, 1-k Ω , digitally controlled potentiometer. The Q8 output of the counter is tied to the UP/DOWN

terminal of the potentiometer; this line changes state every 12.8 sec. Thus, this UP/DOWN control changes the wiper direction every 128 increments. The low and high input terminals of the potentiometer are tied to opposing ends of the 2.01 Ω resistor. Four 1.25V nickel cadmium batteries power the circuit.

A simple model of this resistive circuit is shown in Fig 2. This resistor chain is the equivalent of two 350Ω strain gauges wired in series and mounted back to back. The strain-gauge amplifier connected to this network will sense voltages that correspond to straingauge resistances that change value between 349 and 351Ω .

You should note that this Xicor potentiometer has only 100 wiper positions. When the wiper is at position 99, additional increments will not move the wiper; when the wiper is at position 0, additional decrements

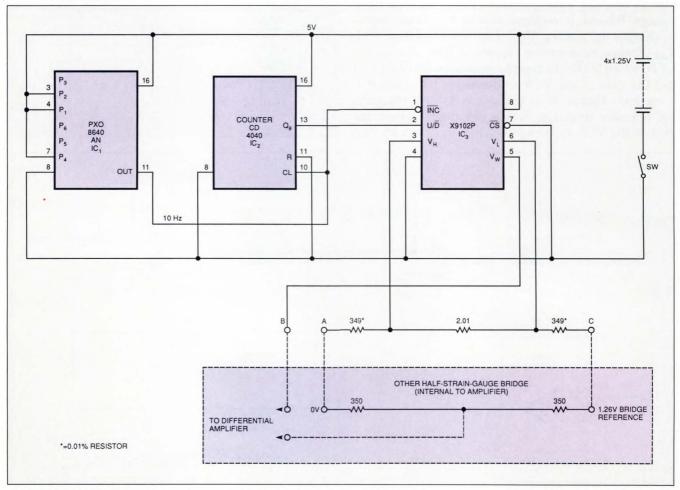


Fig 1—You can use this strain-gauge simulator to test strain-gauge amplifiers. This circuit uses a digitally controlled potentiometer to model strain-gauge resistance changes between 349 and 351Ω .



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Pass Danu (IVITZ	2)	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
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CIRCLE NO 92

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199 EDN May 25, 1989

DESIGN IDEAS

will not move the wiper. This design increments and decrements in groups of 128 purely for design convenience, but the result is that for 28 counts of the cycle the resistance doesn't change. You can easily change this characteristic by using a decade counter in place of the binary counter. Also, you can replace IC₁ with any one of a variety of simple clock sources.

To Vote For This Design, Circle No 749

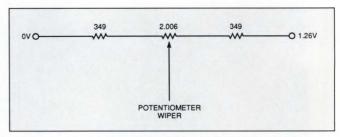


Fig 2—The strain-gauge simulator implements this resistive network, whose resistance is controlled by a digital potentiometer.

Circuit transforms PC into data analyzer

Allan W Overcast Montana State University, Bozeman, MT

You can transform your IBM PC or compatible computer into a complete 8-channel, 12-bit data analyzer

by using the circuit in **Fig 1**. This circuit in conjunction with the Basic program in **Listing 1**, can convert one out of eight analog inputs into a digital word. The program then reads the ADC's output, converts its 2's complement value to a positive or negative binary num-

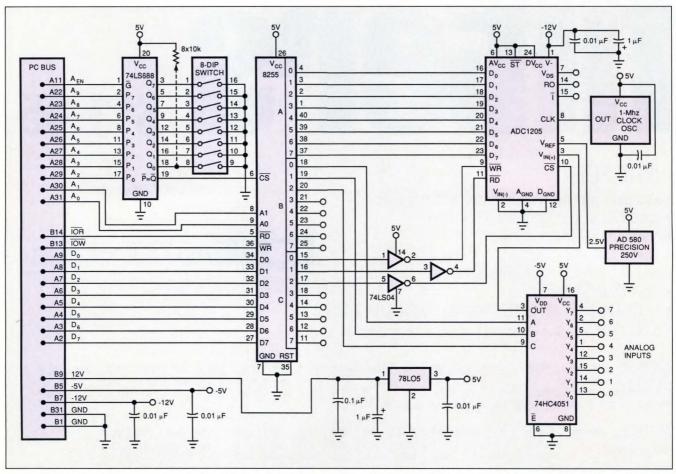


Fig 1—The important components of this PC data-aquisition circuit are the 12-bit ADC and the 8255 peripheral interface. The ADC converts the analog input of your choosing, and the 8255 directs data based on Listing 1's control of address lines A_1 and A_2 .



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EDN May 25, 1989

DESIGN IDEAS

ber, and prints the result. The heart of the circuit is National Semiconductor's ADC1205 12-bit ADC. This converter outputs 13-bit data in two 8-bit bytes: the lower eight bits, the upper four bits, and one sign bit.

The circuit in Fig 1 uses A_0 through A_9 and the address-latch-enable signal ($A_{\rm EN}$) to control the 8255 programmable peripheral interface. The 74LS688 digitally compares address lines A_2 through A_9 to the DIP-switch values that you select. When the two sets of data are equal, the 8255's chip-select line goes low, which enables the active state. A_1 and A_2 control the movement of data through the 8255. The program in Listing 1 uses address 0300H—0011 0000 00XX in binary—to communicate with the 8255. However, you can set the DIP switches and modify the Basic program to use any address from 0000H to 03FFH.

Based on the analog channel you select, the 8255 places the necessary logic levels on the 74HC4051 analog multiplexer's control lines. The output of the multiplexer is tied to the ADC1205, which accepts an analog input voltage from -2.5 to +2.5 V. An AD580 2.5 V precision voltage reference supplies the ADC's $V_{\rm REF}$, which sets the resolution at 610 $\mu V/{\rm bit}$. The ADC1205 conversion takes 100 $\mu {\rm sec}$ after which the data is read out in two consecutive bytes: the lower bits and the upper bits. The ADC's raw code is in 2's-complement format, which the PC converts into a number ranging from -4096 to +4096.

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LISTING 1—ANALOG DATA ANALYZER

```
10
        12 BIT
20
        8 CHANNEL ADC SAMPLER
30
        BY ALLAN OVERCAST
40
     OUT 771,144 : '8255 PTO INITIALIZATION
60
70
     ' 8255 INITIALIZED A = IN, B = OUT, C = OUT
80
     CLS
100
     INPUT"INPUT CHANNEL TO BE READ"; CHANNEL
110
     IF CHANNEL <1 OR CHANNEL >8 THEN PRINT"ERROR " ELSE 150
120
     GOTO 100
150
     OUT 769, (CHANNEL - 1): SELECT THE ANALOG SIGNAL
160
     OUT 770,5 : BEGIN ADC CONVERSION
170
     OUT 770,0 : DESELECT THE ADC
180
     'A 100 µS DELAY IS NEEDED IF A COMPILED PROGRAM IS USED
190
     OUT 770,6 : PREPAIR TO READ THE ADC
200
     ADATA = INP(768) : READ IN THE FIRST BYTE
210
     OUT 770,4 : TURN OFF THE READ LINE
220
     OUT 770,6 : PREPAIR TO READ IN THE HIGH 4 BITS/SIGN
230
     BDATA = INP(768) : READ IN THE UPPER 4 BITS/SIGN
240
     OUT 770,0 :TURN OFF THE CS AND READ LINES
250
       NOW TO COMBINE THE TWO PIECES OF DATA
260
     TOTAL = (BDATA * 256) + ADATA : ' COMBINING
270
     IF BDATA > 240 THEN 280 ELSE 310 : CONVERSION
280
     BDATA = BDATA - 240 : CONVERSION
290
     TOTAL = (BDATA * 256) + ADATA : CONVERSION
300
     TOTAL = TOTAL - 4096 : CONVERSION
     PRINT" YOUR ANALOG VOLTAGE IS "; TOTAL; " IN DIGITAL";
310
     LOCATE 23,2: INPUT" <ENTER> TO CONTINUE..."; CONT
320
330
     GOTO 80 : 'RETURN TO DO IT AGAIN
```

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STR

CIRCLE NO 94

DESIGN IDEAS

Design Entry Blank

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Titlo

_ Phone _

Company ___

Division (if any)

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(Must accompany all Design Ideas submitted by US authors)

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Date

ISSUE WINNER

The winning Design Idea for the February 16, 1989, issue is entitled "Equations yield hysteresis values," submitted by Art Vaughn of Ajax Magnethermic Corp (Warren, OH).

Your vote determines this issue's winner. All designs published win \$100 cash. All issue winners receive an additional \$100 and become eligible for the annual \$1500 Grand Prize. Vote now, by circling the appropriate number on the reader inquiry card.

FEEDBACK AND AMPLIFICATION

Data strobe timing correction

Ron Kumetz, Project Engineer Charles Beseler Co, Linden, NJ

The Design Idea "UART forms RS-232C/Centronics interface" (EDN Design Ideas Special Issue, Vol I, pg 122) incorrectly specifies the minimum width of the STB pulse as 500 nsec. According to a Centronics engineering standards document, the minimum length of this pulse is 1 $\mu sec.$

Typographical error

Art Vaughn, Senior Development Engineer Ajax Magnethermic Corp, Warren, OH

My Design Idea, "Equations yield hysteresis values," (EDN, February 16, 1989, pg 153) contains a typographical error. The numerator of the equation for R_3 contains the term $V_{\rm RI}$; it should be $V_{\rm RL}$.

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256

8 CH A/D

8 CH A/D

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Yes 52

No 52

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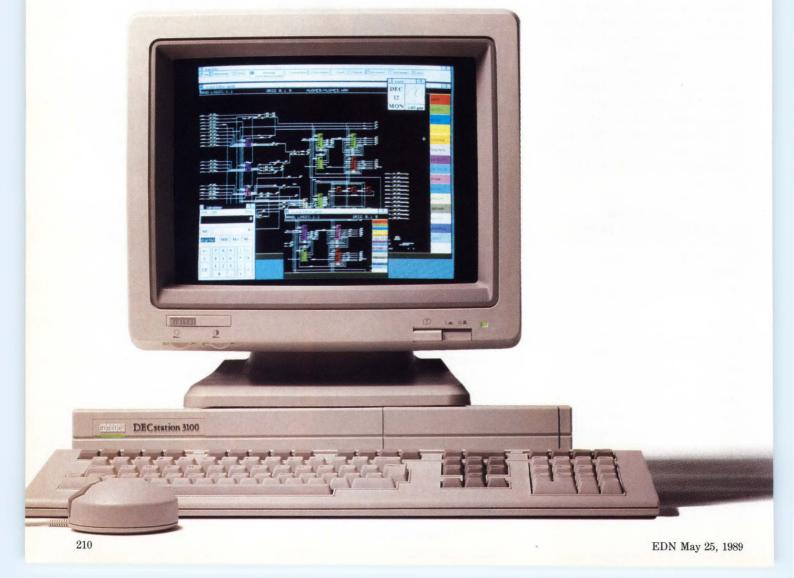
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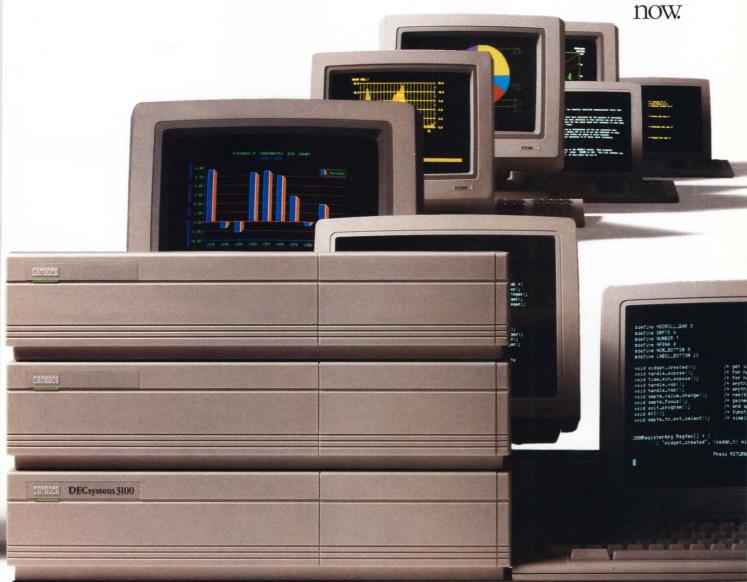
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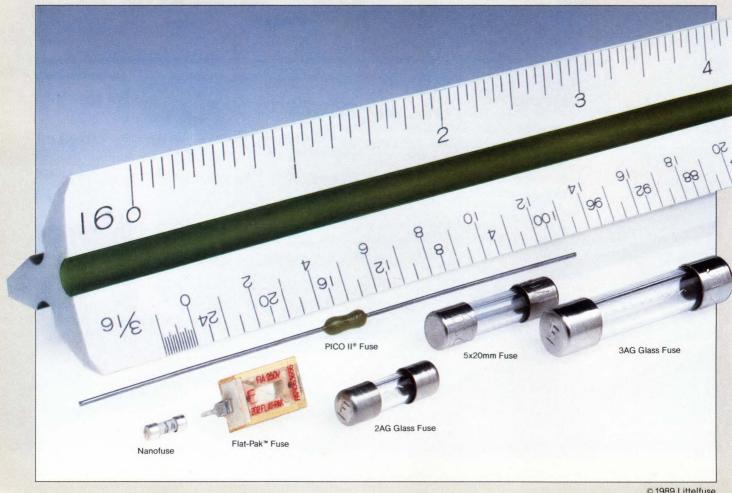
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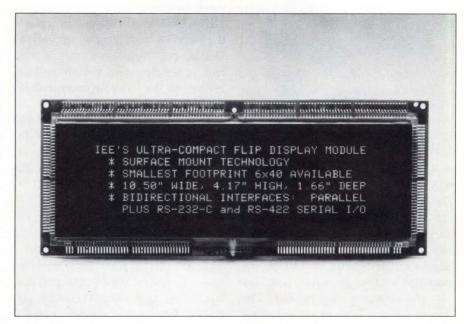
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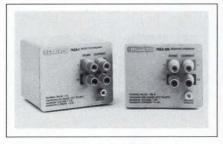


user, measures 185-fL typ. \$478 (100). Delivery, four to six weeks ARO.

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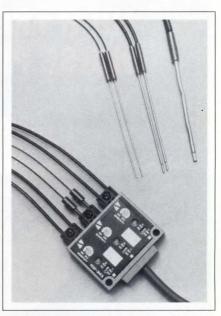
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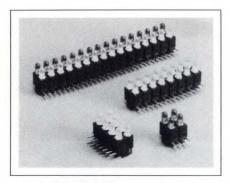
trols are available in single-, dual-, and triple-output versions. The dual-output models are available with AND/OR, delay, or self-diagnostic outputs. All models feature a visible red LED source; protection against false pulse trigger, short circuit, and reverse polarity; and an optional light-operate/dark-operate switch. The durable plastic housings are designed to meet IP60 sealing standards. The controls op-



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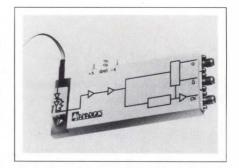
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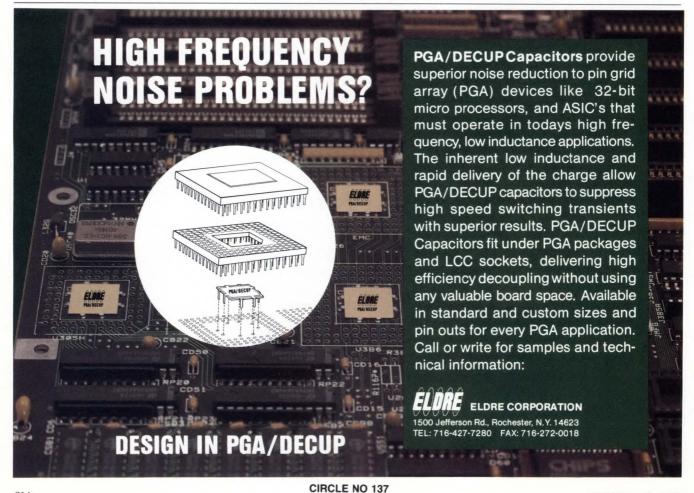
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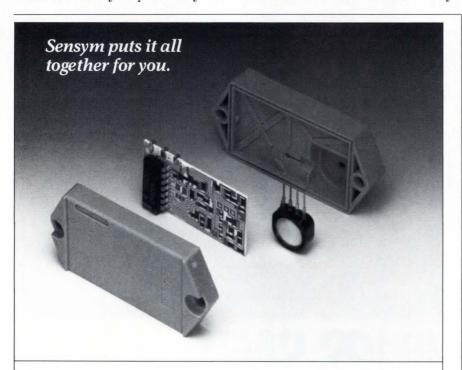
drive, preprocessing, video processing, and power-supply circuits to produce a 525- or 625-line 1V p-p composite video output that's compatible with NTSC or PAL TV standards. In NTSC mode the camera output comprises two interlaced fields with a displayable resolution of 796 × 245 pixels. In the PAL mode the interlaced fields have a displayable resolution of 780 × 288 pixels. You can also select a noninterlaced output. Other user-selectable functions include automatic or computer-controlled gain, automatic iris control, internal or external gen-locked synchronization, and white balance control via throughthe-lens sensing or via an external de input. The flexirigid pe boards fold to produce overall assembly dimensions of $195 \times 42 \times 48$ mm. The unit operates from a 12V supply and draws approximately 325-mA max current. Approximately Gld 1150 to Gld 1270.

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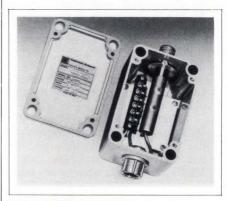
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WREN VI H/H	383/338	*SCSI	15.0	18-20
	383/338	ESDI	16.0	15
	383/338	AT	16.0	15
	274/242	AT	16.0	15
	164/145	AT	16.0	15
WREN V	702/613	*SCSI	16.5	12-16
	385/339	*SCSI	10.7	15-16
	442/390	ESDI	16.0	10
	383/338	ESDI	14.5	10
WREN V H/H	209/183	*SCSI	18.0	9-15
WREN IV	376/330	*SCSI	17.5	10-15
	350/307	*SCSI	16.5	9-15
WREN III	182/160	*SCSI	16.5	10
	182/160	ESDI	16.5	10
WREN III H/H	106/94	*SCSI	18.0	10
	106/94	ESDI	18.0	10
WREN II	135/115	RLL	28.0	7.5
	96/80	ST506	28.0	5
	86/71	ST506	28.0	5
	85/71	ST506	28.0	5
	86/71	ESDI	28.0	5
	81/74	AT	28.0	7.5
WREN II H/H	74/65	AT	28.0	7.5
VY 1612/1 11 11/11	77/65	RLL	28.0	7.5
	51/41	ST506	28.0	5

at 512 Bytes/Sector. All WREN Disk Drives have 40,000 hours MTBE. *Apple compatible interface available.



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RII O		A 410 COT 4021		

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Arrow 416-672-7769



North Carolina Raleigh Arrow 919-876-3132

Winston-Salem Arrow 919-725-8711

A Subsidiary of Control Data **CIRCLE NO 141**

COMPONENTS & POWER SUPPLIES

rough indoor and outdoor environments. The seven models in the line can measure liquid or gas pressures from 200 to 5000 psig. You can compress the calibrated range from 100 to 25% of the rated range—equivalent to a 4:1 turn-down ratio. Depending on the amount of compression, you can suppress zero from 0 to 75% of the rated range. Accuracy equals $\pm 0.5\%$ of the user's calibrated range. The transducers have a 2-wire, 4- to 20-mA current-loop output. The operating range spans -15 to +150°F. \$350.

Robinson-Halpern Co, Box 248, Plymouth Meeting, PA 19462. Phone (215) 825-9200.

Circle No 358



TRANSDUCERS

- Feature a 100-mV output
- Have 0.5% accuracy

PT-300 Series pressure transducers offer a 0.5% accuracy (including linearity, hysteresis, and repeatability) over a full-scale input range of 50 to 3000 psig. At 75°F, they are zero balanced within ±1 mV. All units feature a 100-mV full-scale output and are designed to operate from a 10V dc source. The transducers are protected against 2× rated pressure. The operating range spans -50 to +125°F; the compensated operating range equals 30 to 110°F. \$235 to \$247.

Acculex, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3660. TLX 503989.

Circle No 359

PANEL CONTROLS

- Have 50,000-cycle life
- Tolerances to ±5% available

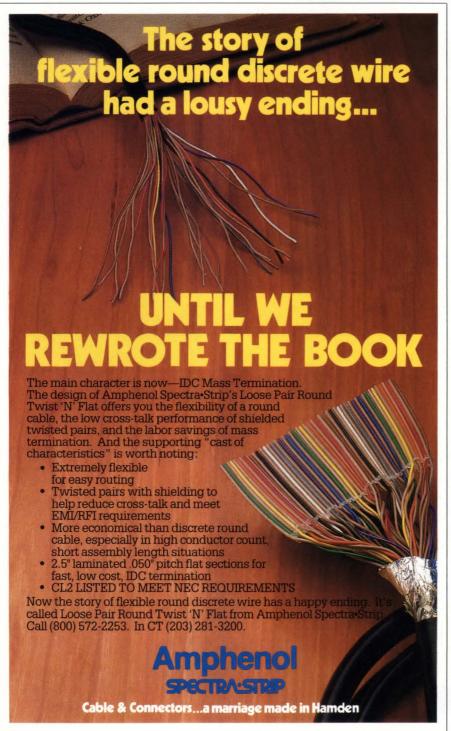
Featuring a 0.5-in. square package, the sealed Model 50 panel controls can accommodate wave-soldering and board-washing procedures. The devices are available in values ranging from 150Ω to $1~M\Omega$, and all have

a rotational life of 50,000 cycles. The controls are available with either linear or audio tapers, and the resistance tolerance can range as low as $\pm 5\%$, depending on element type. Independent linearity is $\pm 5\%$, and contact resistance variation measures 2%. A choice of cermet or conductive plastic elements

is available as are shaft-size and bushing-material options. Termination choices include pc-board or solder-lug configurations. From \$1.75 (1000). Delivery, stock to eight weeks ARO.

Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5500. TLX 676423.

Circle No 360





PROCESS MONITOR

- Features two isolated signal inputs
- Has a 6-character display

The PM-5080 process monitor/controller features two voltage/current signal inputs—0 to 100 mV (or 0 to 20 mA) and 0 to 10V; four programmable setpoint relays for on/off control; and an optional analog output for linear control. Input signals are easily scaled to engineering units for display on the 6-character fluorescent display, which can also include any 2-character unit descriptor. You can configure the display to alternately display as many as eight different system variables at 2-sec intervals. The setpoint relays will switch 300V/100-mA loads. You can use either the keypad or the serial port to enter all configuration information. The unit is housed in a compact \(\frac{1}{8} \) DIN package and operates on supplies of 100, 115, or 230V ac. From \$395.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. TLX 174388. FAX 508-339-6356.

Circle No 361

This tiny vibration is about to give your customer the shakes.

Put a damper on vibration with 3M Scotchdamp[™] Vibration Control Systems.

It's a fact of science. As materials become lighter, they are increasingly prone to the disruptive effects of vibration. Now there's a solution that makes life a lot easier for today's design engineers—Scotchdamp Vibration Control Systems.

Custom designed to your exact specifications, these systems combine energy dissipating polymers with other key materials to solve specific vibration problems. For example, stainless steel dampers, now being used on hard disk drive suspension assemblies, virtually eliminate vibration and thereby reduce data errors.

If you're designing electromechanical devices of any kind, Scotchdamp Vibration Control Systems can help you eliminate troublesome vibrations. Team up with 3M, a world leader in vibration control materials, to increase your customers' satisfaction—and yours—through vibration-free product performance. Circle the reader service number or write: 3M Industrial Specialties Division, Building 220-7W-04, 3M Center, St. Paul, MN 55144-1000. Better yet, call (612) 733-7411 today.



WHEN THERE'S NO ROOM FOR ERROR:



INTRODUCING TEK'S 20 GHZ, MULTICHANNEL COMPREHENSIVE MEASUREMENT SYSTEM.

Imagine characterizing GaAs, ECL, or high-speed TTL circuits with 1 picosecond repeatability and .01 picosecond sample interval.

Or acquiring not one or two, but up to 68 channels of waveform data simultaneously. All under manual or program control.

Imagine reducing propagation delay measurements to the push of a button. Or performing single-ended TDR and for the first time—true differential TDR, with unprecedented accuracy.

Nothing else lets you work at the leading edge with so much confidence.

The new Tektronix 11800 Series makes previously difficult measurements routine. Even if you use it infrequently, you'll find its operation straightforward and unforgettable.

Measurement readouts on the 11800 Series are continuous—not just misleading "snapshots." Mean and standard deviation statistics on each measurement give you a true picture of measurement integrity. With its maximum 136 acquisition channels, complete programmability, extensive onboard waveform processing and unparalleled accuracy, the 11800 Series is the clear choice for designers and engineers working at the leading edge of technology.

When there's no room for error, count on Tek.
For more information on these and other Tek scopes, contact your local Tek sales representative, or call 1-800-835-9433, X170.



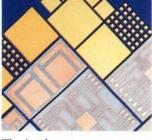
BEAT THE HEAT

with TOKIN A&N SUBSTRATES



Tokin has developed a film metallization technique for creating AlN heat sinks with outstanding insulation and heat dissipation properties.

Designing a transistor without the insulation and heat dissipation properties that let you take full advantage of its capabilities is like building a sports car without a cooling system.



That's why we want you to know what TOKIN's AlN (Aluminum Nitride) substrate material has to offer.

- Thermal conductivity eight times higher than alumina
- Dielectric constant. insulation features, and mechanical strength as high

as alumina

- Thermal expansion coefficient comparable to silicon
- Available in 120, 160 and 200 W/mk (RT) thermal conductivity

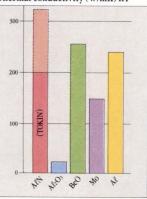
One note worthy application for AlN substrate is TOKIN's own line of Static Induction Transistors (SIT). By using SIT in combination with AlN heat sinks, we are to able provide power levels of 50 W

to 3 KW and breakdown voltages ranging to 1500 V. SIT power modules have been used to manufacture 2 MHz, 2 KW RF induction heating generators with a 70% reduction in size and 80% efficiency. And it couldn't be done without AlN substrate.

So don't leave the job half done. Discover how TOKIN's AlN can give a dramatic boost to transistors or power circuits (including those for auto ignitions).

It's truly an idea worth celebrating.

Thermal conductivity (W/mK) RT



AlN Properties		TOKIN A#N		AlN2O3	BeO	
		T-120	T-160	T-200	(96.0%)	
Density	g/cm ³	3.2		3.8	2.9	
Thermal conductivity	W/mK (RT)	120	160	200	20	260
Thermal expansion coefficient	$(\times 10^{-6}/^{\circ}\text{C})$ (RT ~ 400°C)	4.3		6.7	7.5	
Dielectric strength	KV/mm (RT)	15		15	10	
Volume resistivity	Ω-cm (RT)	>1013		>1013	> 1013	
Dielectric constant	(1MHz. RT)	8.9		8.9	6.7	
Dielectric loss	(1MHz. RT)		3		4	3

TOKI

226

Tokin Corporation

Hazama Bldg., 5-8, Kita-Aoyama 2-chome, Minato-ku, Tokyo 107, Japan Phone: 03-402-6166 Fax: 03-497-9756 Telex: 02422695 TOKIN J

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155 Nicholson Lane, San Jose, California 95134, U.S.A. Phone: 408-432-8020 Fax: 408-434-0375 Chicago Branch
9935 Capitol Drive, Wheeling, Illinois 60090, U.S.A.
Phone: 312-215-8802 Fax: 312-215-8804

Tokin Electronics (H.K.) Ltd.

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NEW PRODUCTS

INTEGRATED CIRCUITS

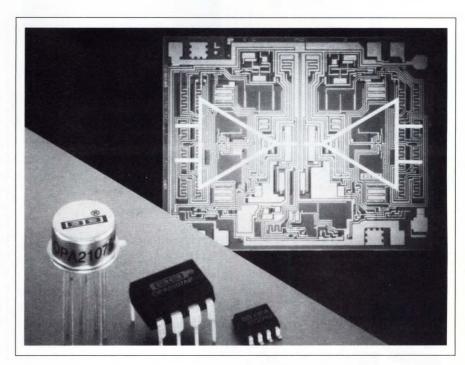
PRECISION OP AMP

- Has settling time of 2 µsec to 0.01%
- Drift is 5 µV/°C max

The OPA2107 precision dual op amp is unity-gain stable and features noise of 8 nV/ $\sqrt{\rm Hz}$ typ at 10 kHz, offset voltage of 500 μ V max, and input bias current of 5 pA max. The minimum slew rate for the OPA2107 is 13V/ μ sec. The vendor supplies the device in three packages: an 8-pin plastic DIP, a metal TO-99, and a plastic SOIC. You can specify temperature ranges of -25 to +85°C or -55 to +125°C. In a plastic DIP, \$5.60 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ, 85734. Phone (800) 548-6132.

Circle No 366





FAST OP AMP

- Achieves a 1-GHz gain bandwidth
- Has a slew rate of 1000V/µsec The EL2038 monolithic op amp for high-speed applications is internally compensated for closed-loop gains of at least 20 and good stability when driving capacitive loads. The op amp operates at a nominal 0.5-mV offset voltage, 5 µA of bias current, and 13 mA of supply current, and it achieves a 1-GHz gain bandwidth, a 1000V/µsec slew rate, and a 16-MHz power bandwidth. The op amp also provides open-loop gains of 15k V/V and supplies ±50 mA of output current to the load. You can purchase the EL2038 in 14pin plastic and ceramic DIPs, and

20-pin ceramic LCCs in either commercial or military temperature ranges. From \$3.90 (100).

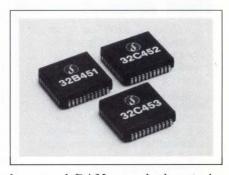
Elantec Inc, 1996 Tarob Ct, Milpitas, CA 95035. Phone (408) 945-1323. FAX 408-945-9305.

Circle No 367

SCSI CHIP SET

- Supports asynchronous transfers to 1.5M bps
- Delivers noninterleaved transfers as fast as 20M bps

The SSI 32B451, 32C452, and 32C453 compose a chip set that can be used in SCSI applications. The 32B451 is a controller device that adapts a peripheral-controller system to a SCSI bus. The 32B452 is a storage controller that operates with 16-MHz μ Ps. You can program an internal RAM-based control sequencer to support standard and custom interface protocols. You can download the controller firmware from an EPROM or host for flexibility. The 32C453 dual-port buffer controller allows you to configure



low-speed RAM as a dual-port circular FIFO buffer. This chip generates the required buffer-memory addressing and manages two ports: a synchronous peripheral device interface and an asynchronous host interface. The 32C453 has arbitration logic to support the SCSI protocol, host DMA transfers, and uninterruptible peripheral block transfers; it addresses as much as 64k bytes of buffer addresses in its multiplexed mode. 32B451, \$10.95; 32C452, \$16.19; 32C453, \$9.30 (5000).

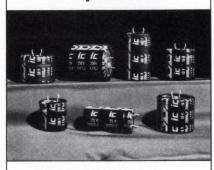
Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110.

Circle No 368

EDN May 25, 1989



Snap-Mount **Aluminum Electrolytic Capacitors**



Proven High Reliability ... 100% Burn-In Tested

- 100 Mfd. to 22,000 Mfd.
- 10 WVDC to 450 WVDC
- -40°C to +85°C
- ±20% Std. (±10% (K) Opt. or -10%, +30% (Q) Opt.)
- Low ESR, Low Impedance
- Solvent Tolerant Seal Std.

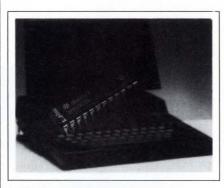


Type LPR and Type LUG Snap Mount electrolytic capacitors offer extremely high CV density and have very long operating life. The low ESR design allows for operation at maximum rated ripple current levels, enabling the designer to streamline circuitry with fewer devices. The modern rugged Snap Mount design allows quick and efficient attachment to a printed circuit board. These rugged capacitors are perfect for the latest design filters in both conventional and switch mode power supplies. The low profile mounting Type LPR is used for designs requiring minimal height above the board: Type LUG fits the more traditional applications where board space must be conserved. Designed with welded terminations, low ESR and low inherent inductance, Types LPR and LUG provide the range of configuration for present and future designs.



CIRCLE NO 148

INTEGRATED **CIRCUITS**



CMOS LAN CHIP

- Interfaces with 10BaseT transceivers
- Replaces higher-power bipolar IC

The DP83910 Serial Network Interface (SNI) is a pin-compatible replacement for the vendor's 8391 chip. This CMOS version uses less than one-third of the power its bipolar cousin consumes, and it meets the low-power requirements of Ethernet add-in boards for laptop computers. In addition, the chip provides the Manchester encoding and decoding functions for Ethernet LANs, which feature a 10M-bps data rate over thick or thin coaxial cable. Further, the SNI is compatible with the proposed 10BaseT Ethernet LAN standard, which features the same data rate over telephone-grade, twisted-pair wiring. In 24-pin DIPs, \$19.50; in 28-pin PLCCs, \$20.75 (100).

National Semiconductor Corp. Box 58090, Santa Clara, CA 95052. Phone (408) 721-2862.

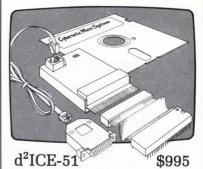
Circle No 369

CACHE RAM

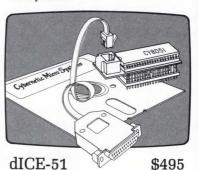
- Features 25-nsec access time
- Supports 33-MHz microprocessor

The IDT 71586, a $4k \times 16$ -bit static RAM with an on-chip address latch, has been optimized to work with Intel's 82385 cache controller. The SRAM offers 10-nsec output-enable time and incorporates separate byte-enable signals. You can implement a 32k-byte, 2-way set-associative cache in five chips: the Intel

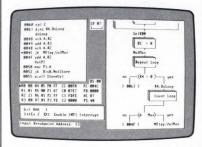
Low Cost 8051 Tools



This Real-Time ICE is the lowest cost and smallest sized full speed 8051 incircuit emulator. Full access to hardware I/O. Includes all debugging features of Sim and dICE below. Fits in shirt pocket.



This reduced-speed in-circuit 8051 debugger provides full access to I/O but will not run real-time. With the same user interface features as Sim8051 below, dICE-51 generates execution profiles during reduced speed execution. (CMOS and MIL also available.)



Sim8051

\$395

This software Simulator/debugger allows 'no-circuit', debugging of 8051 code on IBM-PCs. All Cybernetics 8051 debug tools offer multi-window source code displays, symbolic access to data, single key commands, breakpoints, trace, full speed and single step execution, execution profiler, and more.

Other 8051 tools include:

Cross Assembler 8751 Programmer Debugger Demo Disk

\$195 \$195-\$345 \$ 39







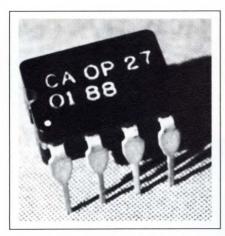


Cybernetic Micro Systems Box 3000 • San Gregorio, CA 94074 (415) 726-3000 • Telex: 910-350-5842

82385 cache controller and four IDT 71586 latched 4k×16-bit memory chips. The SRAMs come in 40-pin plastic and ceramic DIPs and in a 44-pin PLCC. In a plastic DIP, \$41.40 (100).

Integrated Device Technology Inc. 3236 Scott Blvd. Box 58015. Santa Clara, CA 95052. Phone (408) 727-6116. FAX 408-988-3029.

Circle No 370



LOW-NOISE OP AMP

- Features open-loop gain of 1.8 million
- Has gain-bandwidth product of 8 MHz

The OP-27 op amp has wideband noise of 3 nV/ $\sqrt{\text{Hz}}$ at 10 Hz and a 1/f noise corner frequency of 2.7 Hz. It features an 8-MHz gain-bandwidth product and a 2.8V/µsec slew rate. The OP-27 achieves an input bias current of 10 nA and an offset current of 7 nA using an internal bias-current-cancellation (BCC) circuit; this circuit typically holds I_B to ± 20 nA and I_{OS} to ± 15 nA over the military temperature range of -55°C to +125°C. PSRR and CMRR for the op amp exceed 120 dB. The OP-27 is available in five packages: an 8-lead hermetic TO-99, an 8-pin plastic DIP, an 8-pin hermetic DIP, an 8-pin SO package, or a 20-pin LCC. From \$0.54 (100,000).

Calogic Corp, 237 Whitney Pl, Fremont, CA 94539. Phone (415) 656-2900.

Circle No 371

PHONE CHIP SET

- Provides all processing for AMPS or TACS cellular phones
- Can be used in low-power cellular phone handsets

This chip set reduces the number of ICs required in cellular phones by approximately 60%. It comprises a UMA1000 data processor, NE5750 and NE5751 audio processors, a NE605 IF processor, a TDD1742 frequency synthesizer, and an 80C552 microcontroller. The CMOS UMA1000 handles all the data filtering associated with the cellular phone system's control, supervision, and signaling data. You can configure the device to operate according to the AMPS (advanced mobile phone service) or TACS (total access communication system) standards. The bipolar NE5750 audio processor provides compander, noise-cancellation, power-amplifier, and VOX control functions.

The CMOS NE5751 provides all the necessary audioband filtering, plus volume control and DTMF dial-tone generation functions. The NE605 FM IF mixer includes mixer/oscillator, amplifier, and demodulator functions; two limiting IF amplifiers; a quadrature detector; muting control; a received signal-strength indicator; and a voltage regulator. The CMOS TDD1742 frequency synthesizer features a high-gain phase comparator and an auxiliary digital phase comparator to provide fast frequency locking. The 80C51based 80C552 microcontroller provides overall control of the chip set via its on-chip A/D converter, PWM outputs, and I2C bus interface. Samples of the chip set are available now; available in September for under \$60 (OEM qty).

Philips, Components Division, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 757189.



This keyboard only feels expensive.

FKB4700 Series Keyboards



If you design PCs and workstations, you know how users like the crisp, clean feel of a tactile keyboard. But you also know hard it is to justify the added cost.

Now there is a way to specify a tactile keyboard — and save money, too. Just choose the new FKB4700 keyboard from Fujitsu.

Unique switch makes the difference

Only Fujitsu's FKB4700 keyboards incorporate a unique coil spring, rubber dome switch design. This design combines the simplicity of a membrane keyboard with a full 20-gram tactile response.

Compatible with industry standards

FKB4700 keyboards are available in standard 101- and 102-key layouts. Custom layouts, too. And all are UL478, CSA220 and FCC approved. So, make your customers happy — and your accounting department, too.

Ask your Fujitsu representative for complete information and specifications on the FKB4700, the tactile keyboard that only *feels* expensive. Please call Fujitsu Component of America at **408-562-1000**.

FKB4700 Keyboard Specifications				
Number of keys	101 (USA)/102 (Europe)			
Key arrangement	USA/UK/German/French/Italian/ Spanish/Swedish/Swiss			
Tactile	20 g typ.			
Keystroke/force	3.8±0.5mm/55±20g typ.			
Keytop	Rectangular cylindrical step sculpture			
Tilt	7°/12°			
Approval	UL478, CSA220, FCC Class B			



FUJITSU COMPONENT OF AMERICA, INC.: 3330 Scott Blvd., Santa Clara, California 95054-3197 Phone: 408-562-1000 Telex: 910-338-0190 Fax: 408-727-0355

FUJITSU LIMITED (Electronic Components International Sales Support Div.): Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211
International (Int'l Prefix) 81-3-216-3211 Telex: 2224361 Fax: (03) 215-1961

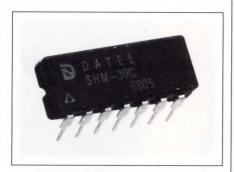
INTEGRATED CIRCUITS

TLX 51573.

Circle No 372 Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone

(408) 991-2000.

Circle No 373



SAMPLE-AND-HOLD IC

- Features 500-nsec acquisition time
- Packaged in a 14-pin ceramic DIP

The internal architecture of the SHM-30C monolithic S/H amplifier consists of an input amp that produces large charging currents, a low-leakage analog control switch, and an integrator that includes an on-chip 90-pF hold capacitor. The SHM-30C achieves its 500-nsec acquisition time to 12-bit, 0.01% accuracy. The chip features a droop rate of $0.01 \mu V/\mu sec$ typ. The SHM-30C also offers an aperture uncertainty time of 0.1 nsec, a slew rate of 90V/ µsec, and a fully differential input. It comes in a 14-pin ceramic DIP. \$29,45.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356.

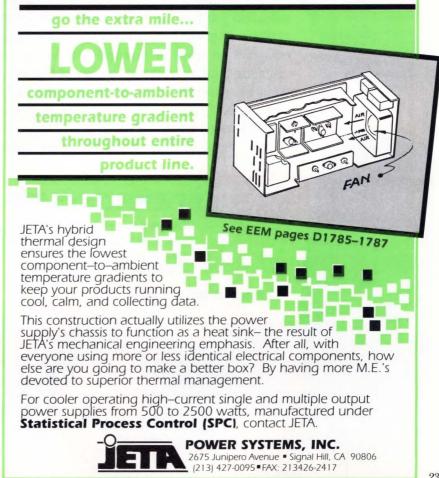
Circle No 374

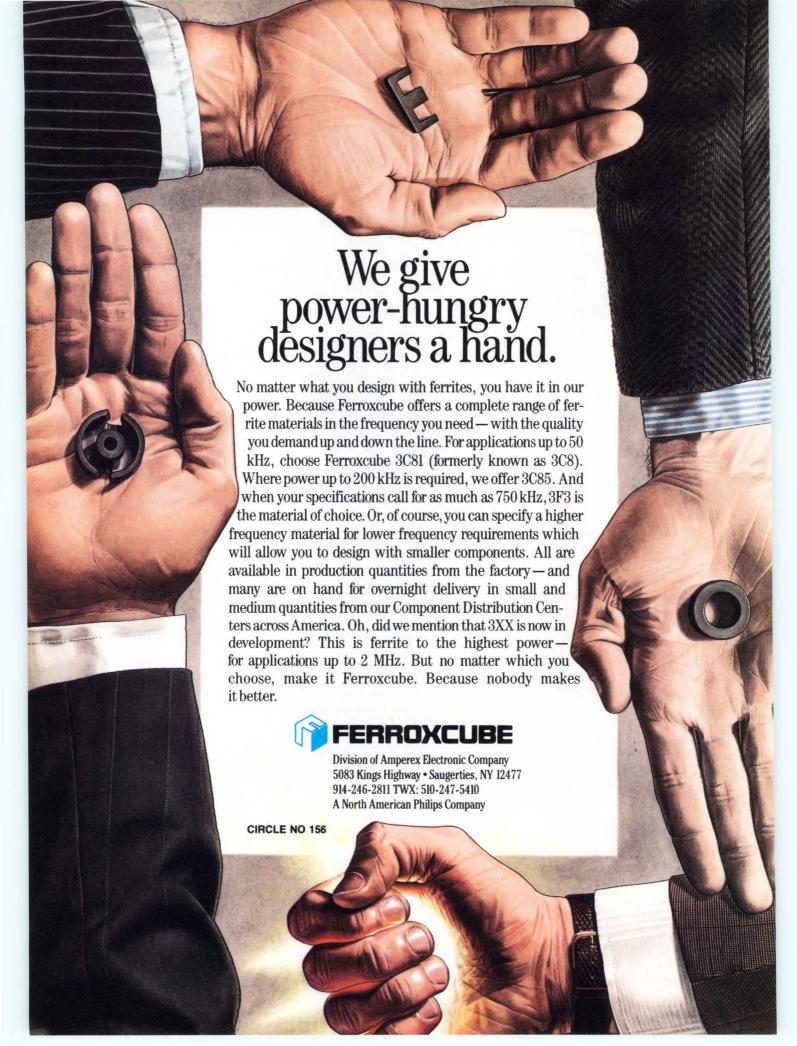
A/D CONVERTER

- Provides an 8-bit serial output
- Needs only three external passive components

The ZN-509 and -510 8-bit A/D converters fit into 8-pin DIPs by generating serial rather than parallel output data. You just need to add three passive components to make them fully operational. The ZN509 has a







INTEGRATED **CIRCUITS**

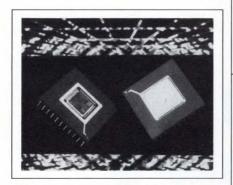
linearity error of $\pm \frac{1}{2}$ LSB; the ZN510 has a linearity error of ± 1 LSB. Both devices have a conversion time of 8 µsec and feature an on-chip 2.5V bandgap reference and a µP interface. The converters operate in either a single-shot or a continuous conversion mode and operate from one 5V supply. From £1.26 (1000).

Plessey Semiconductors Ltd. Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 518000. TLX 449637.

Circle No 375

Plessey Semiconductors, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900. TLX 4940840. FAX 408-438-5576.

Circle No 376



MICROCONTROLLER

- Provides 100-nsec machine cycle
- Is a functional subset of RTX

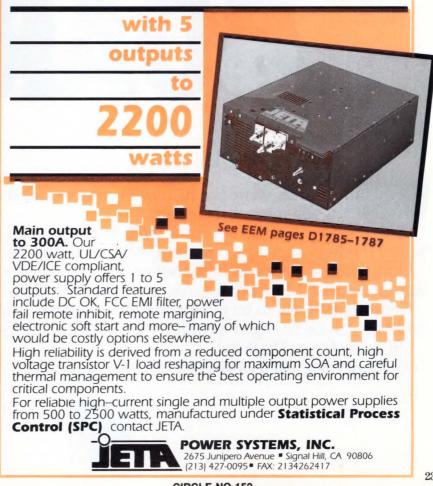
The RTX 2001 16-bit µcontroller incorporates many features of the RTX 2000, such as on-chip timers, an interrupt controller, and a stackoriented multiple-bus architecture. The architecture is responsible for instruction execution times of one or two cycles. A proprietary busthe ASIC Bus-permits extension of the architecture by using off-chip hardware acceleration logic and application-specific I/O devices. The RTX 2001 uses the Forth high-level language and offers single-cycle subroutine call/return, a four-cycle interrupt latency, two on-chip 64word stacks, 1M byte of total address space, and word and byte



CIRCLE NO 159

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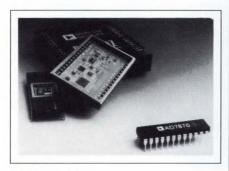


INTEGRATED **CIRCUITS**

memory access. The device sacrifices the RTX 2000's single-cycle multiplier but typically requires only 5 mA/MHz. It comes in either an 84-pin PGA package or a PLCC version in speeds of 8 or 10 MHz. Delivery, stock to eight weeks. From \$119.

Harris Corp, Box 883, Melbourne, FL 32901. Phone (407) 724-3800.

Circle No 377



12-BIT ADC

- Has an on-chip, 2-usec trackand-hold amplifier
- Dissipates 60 mW typ

The AD7870 combines a 3V buried zener reference, clock, bus interface logic, and an 8-usec A/D converter on a BiCMOS IC. The converter features three data-output formats—12-bit parallel, 8+4-bit parallel, or serial data—and a 60-nsec data-access time. It features a 72dB S/N ratio at 10 kHz, -80-dB THD, and -80-dB intermodulation distortion. The AD7870 provides $\pm \frac{1}{2}$ LSB integral nonlinearity, ± 1 LSB differential nonlinearity, ± 5 LSB bipolar zero error, and no missing codes at 12 bits of resolution. The chip accepts a ±3V fullscale input and operates from $\pm 5V$. The converter's typical linear input bandwidth (-0.1 dB) is 500 kHz. Available in 24-pin 300-mil DIPs, 28-lead PLCCs, and 28-lead LCCs. From \$20 (100).

Analog Devices Inc, 1 Technology Way, Box 9106, Norwood, MA 02062. Phone (617) 329-4700. TWX 710-394-6577. TLX 924491.

Circle No 378

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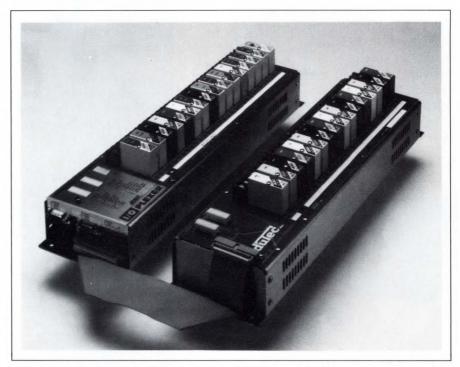
NEW PRODUCTS

COMPUTERS & PERIPHERALS

REMOTE I/O MODULE

- Executes input and output commands from a host
- Display indicates the unit's address and baud rates

The I/O Plexer remote I/O controller is controlled by a remote host via an RS-232C or RS-422 port at baud rates ranging from 300 to 19,200 bps. The base unit holds a combination of 16 analog and digital modules. Analog input modules accept inputs from 50 mV to 10V and 4 to 20 mA as well as inputs from thermocouples, RTDs, and 590 probes. Analog-output modules provide $\pm 5V$, $\pm 10V$, and 4- to 20mA outputs. A digital expander adds 16 additional lines to the base unit's 16 mixed analog and digital lines. The host can control as many as 2048 I/O lines from one RS-232C port and programs the controller using ASCII character strings. Once the host sets up a setpoint the unit can operate without host inter-



vention. An onboard display indicates the unit's address, baud rate, and detected faults. Without the I/O modules, \$425.

duTec Inc, Box 964, Jackson, MI 49204. Phone (800) 248-1632; in MI, (517) 750-4700.

Circle No 383

386 MOTHER BOARD

- Plugs into a Compaq 8086 Deskpro computer
- Has three 8-bit and four 16-bit expansion slots

The STD-386CP upgraded mother board for the Compag 8086 Deskpro computer contains either a 16- or 20-MHz 80386 CPU and a socket for an 8-MHz 80287 or a 16- or 20-MHz 80387 coprocessor. The board plugs directly into the computer's chassis and has three 8-bit and four 16-bit expansion slots. An additional "dual-personality" slot can be configured as either an 8-bit expansion slot or as a 32-bit memory slot. The board comes with 1M, 2M, 4M, 8M, or 16M bytes of memory and operates with all of the Deskpro's peripherals such as the hard- and floppy-disk controllers and the keyboard. To aid in installation, the company's \$29.95 kit includes all of

the mounting hardware, cables and connectors. 16-MHz version with 1M byte of memory, \$1695; 20-MHz version with same configuration, \$2195.

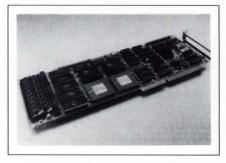
Seattle Telecom & Data, 2735 152nd Ave NE, Redmond, WA 98052. Phone (206) 883-8440.

Circle No 384

1750A COPROCESSOR

- Implements the MIL-STD-1750A specification
- Has 2M bytes of RAM

The Orbiter is a coprocessor board for the IBM PC/AT and compatible computers. The board uses LSI Logic's L64500/L64550 chip set to execute the complete MIL-STD-1750A Instruction Set Architecture. Standard features include 2M bytes of dual-port RAM, single-step operation under PC control, hard-



ware trace functions, a floating-point unit, a memory-management unit, and a write-protection unit. The board also contains two 50-pin connectors that give the user complete access to its CPU bus signals for prototype development. It can generate or accept two levels of software-selectable interrupts. A socketed oscillator lets the user manipulate the CPU's clock speed over a frequency range of dc to 20 MHz. The unit lets you model an aircraft's data flow in real time, including

COMPUTERS & PERIPHERALS

flight control, missile launching, and radio communications. \$8800; in Europe, \$11,440.

Sabtech Industries Inc, 3910-B Prospect Ave, Yorba Linda, CA 92686. Phone (714) 524-3299. FAX 714-524-3290.

Circle No 385



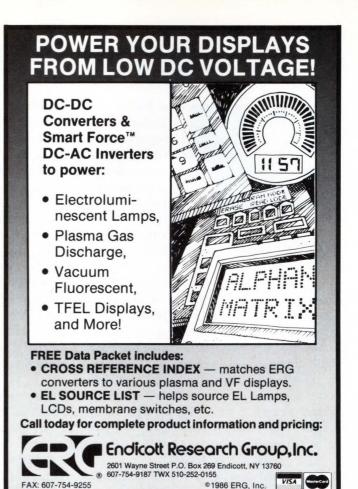
DEVELOPMENT SYSTEM

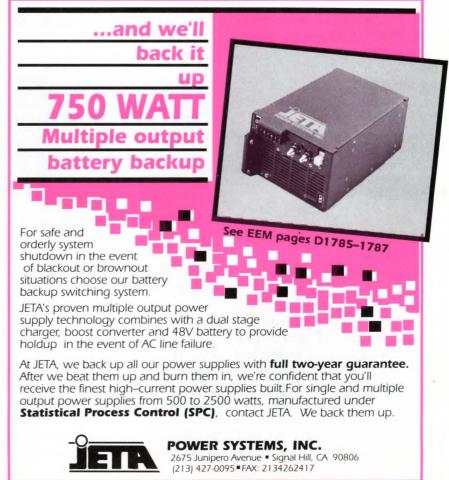
- Develops Ada code for real-time applications
- Development, real-time target system fit in one enclosure

The Hybrid Ada Development System development subsystem for real-time Ada applications is a stand-alone unit that consists of Sun-3 Eurocards. It includes a 20-MHz 68020 µP; 4M bytes of dynamic RAM; a 68881 floating-point unit; SCSI, Ethernet, and monochrome video controllers; a 141Mbyte hard-disk drive; a 65M-byte streaming tape; a black-and-white 19-in. monitor; a keyboard; and a mouse. The unit comes with the SunOS enhanced operating system and VADS/Works; this combination allows you to develop code using the Verdix Ada Development System (VADS) and download and debug the code on a µP running VxWorks on an enclosed real-time target subsystem. You can also develop code on a Sun-3 or -4 workstation and download it to the real-time target system via Ethernet. Real-time subsystem, \$6995; with complete development system, from \$58,095.

Mizar Inc, 1419 Dunn Dr, Carrollton, TX 75006. Phone (214) 446-2664. FAX 214-522-5997.

Circle No 386







ACQUISITION CARD

- Digitizes data at 60 kHz for the Mac II
- Multiplexes eight single-ended inputs to a 12-bit A/D converter

The Lab-NB data-acquisition board for the Macintosh II computer multiplexes eight single-ended analog inputs to a 12-bit A/D converter. The converter operates at a maximum sustained sample rate of 60 kHz. It accepts input voltages from 0 to 10V or ±5V and provides gain ranges of 1, 2, 5, 10, 20, 50, or 100. In addition, the board has two 12bit D/A converters with unipolar or bipolar voltage outputs and an onboard reference voltage of 10V. The board features three independent 16-bit counters that synchronize events and measure frequency and time; it also has 24 digital I/O lines that can be configured as three 8-bit input, output, or bidirectional ports. \$695.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (512) 794-0100. TLX 756737. FAX 512-250-9319.

Circle No 387

I/O BOARD

- Provides analog and digital I/O for Multibus II systems
- Has an onboard 80186 µP

The IO-186/070 intelligent I/O board for Multibus II systems provides a combination of analog and digital I/O functions, including 16 single-ended or 8 differential analog-input channels, six analog-output channels, and 48 digital I/O lines. The analog inputs are digitized by a 12-bit A/D converter with

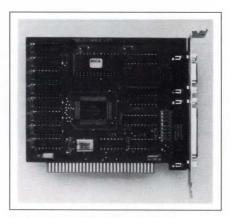
a 5-usec conversion time, and the analog outputs are driven by six separate 12-bit D/A converters with output settling times of 1.5 µsec. The analog inputs and outputs operate over 0 to +10V or 0 to -10V, and the digital I/O is TTL compatible. Subsystem intelligence is provided by an 80186 µP, as much as 512k bytes of EPROM, and as much as 512k bytes of dual-ported static RAM. The board's Multibus II interface supports message-passing, built-in self-test, and interconnectspace functions. The board also carries the company's cCBX interface for subsystem expansion. Approximately \$2700.

Concurrent Technologies Ltd, Fairfax House, Causton Rd, Colchester CO1 1RJ, UK. Phone (0206) 42996. FAX 0206-67333.

(619) 592-1479. FAX 619-673-9479.

Circle No 388 Concurrent Technologies Inc, 11545 W Bernardo Court, Suite 100, San Diego, CA 92128. Phone

Circle No 389



GRAPHICS ADAPTER

- Enhances the resolution of monochrome and CGA monitors
- Features automatic mode switching and a printer port

The Dual Graphics adapter is an IBM PC-, IBM PC/XT-, and IBM PC/AT-compatible board that enhances the resolution of both monochrome and CGA monitors. The board contains the functions for the IBM Color Graphics Adapter

(CGA), the IBM Monochrome Display Adapter (MDA), and the Hercules Graphics Card. The card can dispaly 80×25 lines of text and 720 × 348 pixels for Hercules graphics resolution on a TTL monochrome monitor. On a CGA, EGA, or other RGB-type monitor, the board displays 80×25 lines of text with 16 colors, 320×200 graphic pixels with four colors, and 640×200 graphic pixels with two colors. The adapter supports any software written for MDA, Hercules Graphics, or CGA displays such as WordPerfect and Lotus 1-2-3. The board also features automatic mode switching and has a 25-pin parallel printer port. The board switches to the correct display mode at boot-up, according to the switch settings. \$99.

Boca Research Inc, 6401 Congress Ave, Boca Raton, FL 33487. Phone (407) 997-6227. FAX 407-997-0918. TLX 990135.

Circle No 390

STAND-ALONE SBC

- Uses the Harris RTX 2000 Forth CPU in embedded systems
- Base system runs at 8 MHz and contains 32k bytes of static RAM The SC/FOX SBC stand-alone single-board computer for embedded applications uses the Harris RTX 2000 real-time processor, which operates with Forth microcode. The Eurocard-size board measures 4×6.3 in. The base system runs at 8 MHz and has 32k bytes of static RAM; you can upgrade the system to operate at 10 MHz and 12 MHz with either 64k, 128k, 256k, or 512k bytes of static RAM. The board has an RS-232C port, a parallel printer port, a reset switch, and 64k bytes of shadow EPROM. It features a native optimizing compiler, called FCompiler, for the RTX 2000. In EPROM, you can optionally get SC/ Forth language, an interactive multitasking version of Forth. Both software tools automatically opti-

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The ability to withstand high voltage transients is measured by a test called First self-healing. This is defined as a voltage drop of 5 V, and is executed periodically at the Rifa Laboratories in Kalmar, Sweden. For years, the outcome of this test has always been the same: 95% of metallized plastic film caps start self-healing at voltages lower than 3 kV; of

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mize Forth primitives into single-cycle machine instructions. You need only a 5V power supply, an RS-232C cable, and a terminal to develop code for the unit. 8-MHz system with 64k bytes of memory and the FCompiler software, \$1295. SC/Forth software in EPROM, \$995.

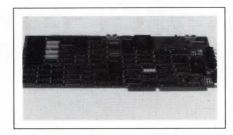
Silicon Composers, 210 California Ave, Suite K, Palo Alto, CA 94306. Phone (415) 322-8763.

Circle No 391

IMAGE BOARD

- Digitizes RS-170 format signals for the IBM PC/AT bus
- Uses TI's TMS-34010 Graphics System Processor chip

The MTIG-100 image-acquisition and -processing board for the IBM PC/AT bus digitizes as many as four RS-170 formatted video inputs at 30 frames/sec with 8 bits of resolu-



tion. The frame is stored in a video RAM buffer with 512×512-pixel resolution. The frame buffer retrieves real-time data from a 2k×8bit look-up table that can have eight different 256×8-bit data; this feature lets you create real-time video effects or perform adaptive imaging. The board uses TI's TMS-34010 IC as a graphics processor, and it contains a 512×512-pixel overlay buffer that lets you overlay as many as 15 color planes. A Bt-478 triple DAC provides the three RGB outputs with 256 colors from a palette of 16.7 million. The board has 384k bytes of RAM for program and data storage. Introductory price (valid until Sept. 30, 1989), \$1795.

Multisignal Technology Corp, 4662 Katella Ave, Suite J, Los Alamitos, CA 90720. Phone (213) 431-3503. FAX 213-598-1741.

Circle No 392

BUBBLE-MEMORY CARD

- Has 512k to 4M bytes of storage for IBM PC, PC/XT, and PC/AT
- Modular design allows as many as eight SBM-74 modules

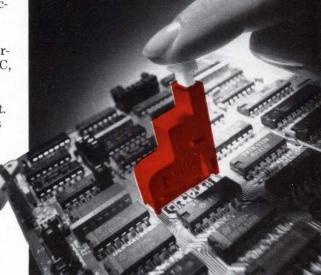
The PCB-74 is a bubble-memory board for the IBM PC, PC/XT, PC/AT and compatible computers. The board provides 512k to 4M bytes of nonvolatile mass storage and has a modular design that accommodates as many as eight of the company's SBM-74 bubble modules. Each module contains 512k bytes of bubble memory. The supplied firmware permits the board to emulate Text continued on pg 245

CARDGARD[®] 2. The Built-In Circuit Protector You Can Reset.

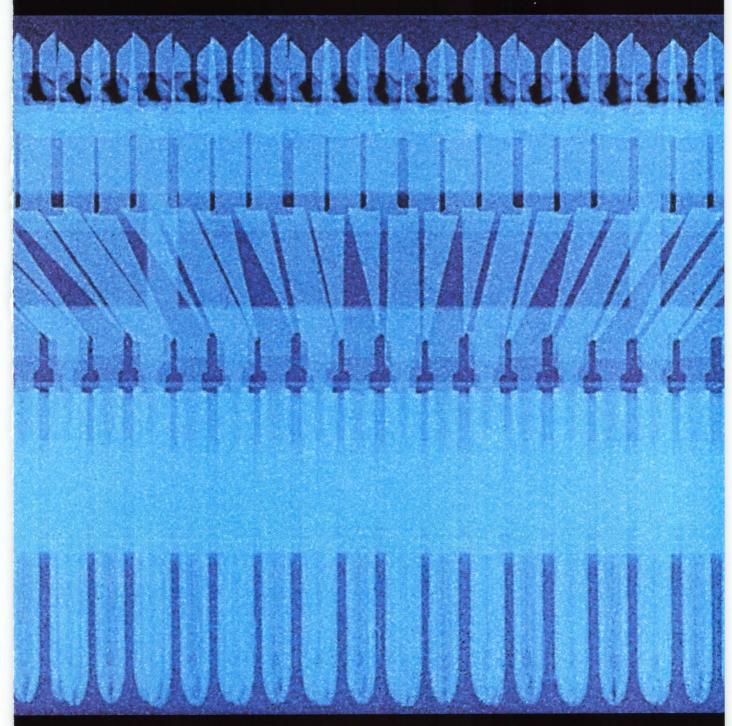
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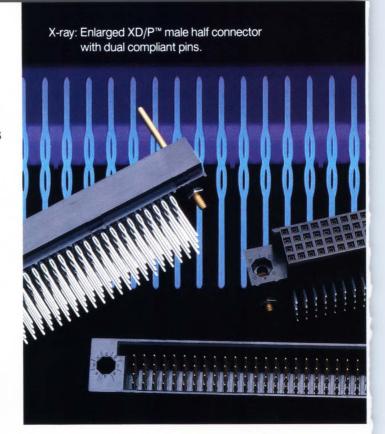
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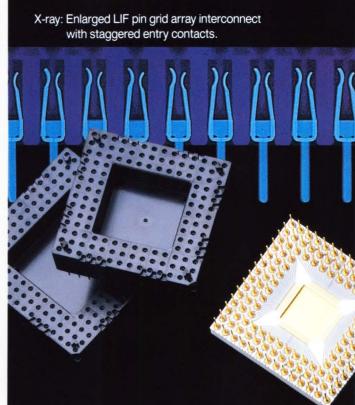
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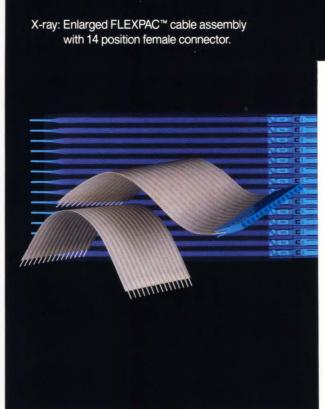
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COMPUTERS & PERIPHERALS

a hard-disk drive when the computer operates with MS-DOS or PC-DOS. The board boasts an MTBF of 10 years and an operating range of 0 to 60°C. \$250. 10-to-50°C-range module, \$400; 0-to-60°C-range module, \$600.

Memtech Technology Corp, 3000 Oakmead Village Ct, Santa Clara, CA 95051. Phone (408) 970-8900.

Circle No 393

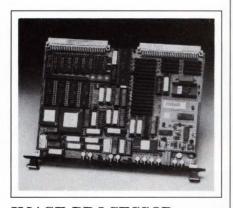


IMAGE PROCESSOR

- Digitizes four multiplexed video inputs for the VME Bus
- Buffer holds one 1024×512- or two 512×512-pixel pictures

The Image Processing Computer (IPC) is an image-processing unit on a double-height VME Bus board. It multiplexes four video inputs into an 8-bit ADC that has a maximum sample rate of 15M samples/sec. The high sample rate generates square pixels for standard video formats such as CCIR or EIA. The acquired data, which can be synchronized with external trigger signals, is sent to an onboard 512kbyte dual-port frame buffer. The frame buffer can store either one picture with a resolution of 1024 × 512 pixels or two pictures with a resolution of 512×512 pixels. One of the buffer's ports drives a video DAC that provides RGB and sync outputs. The computer includes a 68020 µP and a 68881 FPU for image-processing control, 1M byte of dynamic RAM for program and data storage, and space for as

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PROTECTION: Continuous Short Circuit

Overvoltage Protection and Transient Suppression Thermal Shut Down

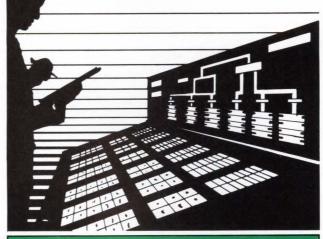
MTBF: 350,000 hours per MIL HDBK 217E at 40°C

BURN IN: 24 hours 70° C, full load

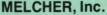
OPERATING TEMPERATURE: -55 . . . 85° C ambient -55 . . . 95° C case

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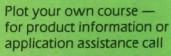
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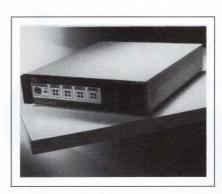
CIRCLE NO 96

COMPUTERS & PERIPHERALS

much as 512k bytes of EPROM. A 68681 DUART provides two channels of serial I/O. \$4300.

American Eltec Inc, 569 S Marengo Ave, Pasadena, CA 91101. Phone (818) 449-1558. FAX 818-578-0054.

Circle No 394



PHOTOPLOTTER

- Lets you produce pc-board photographic artwork in house
- Can be used with HPGL or Gerber file input

The Colourwriter-3030 is a flatbed photoplotter that allows you to produce pc-board artwork as large as 14×11 in. on photographic film. In addition, the plotter accepts ink pens so that you can produce draft plots. It accepts HPGL files using a standard HP7475 driver and accepts plots from standard software packages such as AutoCAD, Lotus 1-2-3, Supercalc, Racal Redboard/ CADStar, P-CAD, and Vutrax. Software supplied with the unit allows you to convert Gerber files to HPGL format using a PC. Positional accuracy is $\pm 0.1\%$ or 0.05mm, whichever is greater, and repeatability ranges from ± 0.05 mm in single-pen mode to ± 0.15 mm in multipen mode. The photoplotter has a lightproof lid that lets you load film in a dark room and then operate the unit in daylight. Light pens range in aperture size from 0.008 to 0.2 in. and are capable of flashing pads at 95 msec/pad. You can draw tracks of different widths in one pass. £4995.

Bryans Instruments Ltd, 14-16

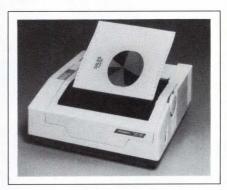
Wates Way, Mitcham, Surrey CR4 4HR, UK. Phone 01-640-5624. TLX 946097. FAX 01-648-4840.

Circle No 395

COLOR PRINTER

- Has a graphics controller for a variety of graphics systems
- Produces 256 colors from a pallette of 32,000 colors

The CHC 336 color thermal printer has a built-in intelligent graphics controller (IGC) that lets it interface without custom software drivers to the Hewlett Packard Graphics Language and the Direct Graphics Interface Standard graphics packages. The printer prints text and graphics on A-size paper or transparencies and contains a page buffer that lets you print multiple copies. Control-panel DIP switches

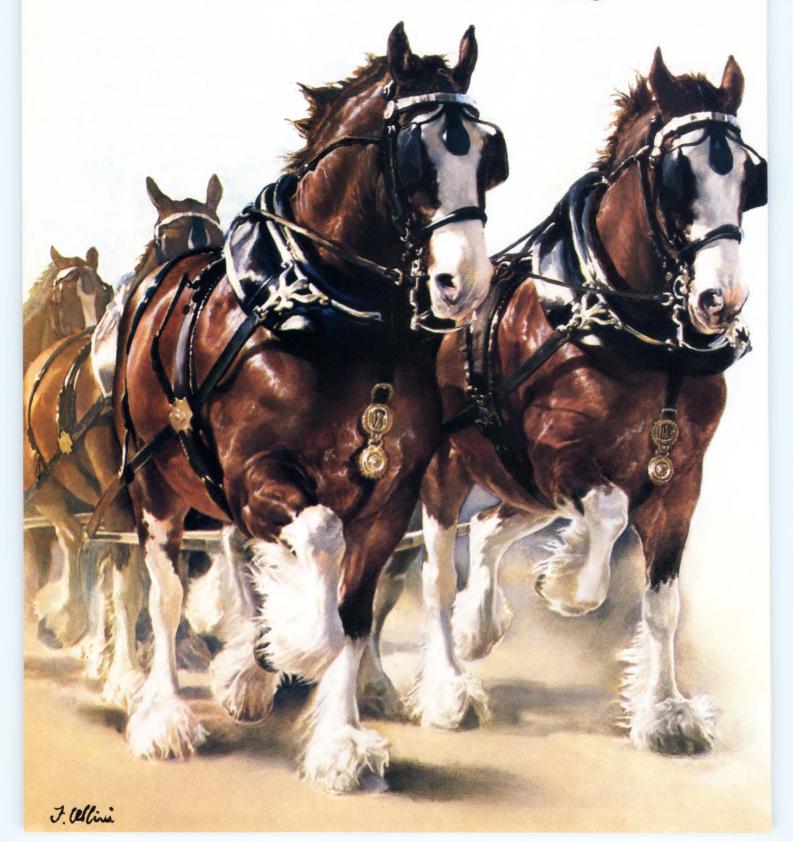


select either a yellow-magenta-cyan or a yellow-magenta-cyan-black color mode. In an IGC mode, the printer produces 256 colors from a palette of over 32,000 colors. It features 12- and 24-point roman resident fonts. The printer measures $16.1 \times 16.3 \times 7.0$ in. and weighs 38 lbs, and it interfaces with the host through either an RS-232C or a parallel printer port. \$6300.

Mitsubishi International Corp, Information Systems and Services Div, Computer Graphics Dept, 701 Westchester Ave, White Plains, NY 10604. Phone (914) 997-4999. FAX 914-997-4976.

Circle No 396

Bred for the Job



Hitachi's New H8/532 One-time-programmable 8-bit Microcontroller

Handles the Toughest Real-time Control Tasks with Ease

The Clydesdale. Superior strength and stamina, yet easy to work with. Created by man and nature to excel in a specific role...tackling heavy-duty work.

Handling tough jobs is the same idea behind Hitachi's newest workhorse: the H8/532 microcontroller—bred to excel at the most demanding real-time event control tasks.

This 8-bit microcontroller harnesses the power of a 10MHz CPU with a 16-bit internal architecture. It muscles its way through complex math problems with a 200ns minimum instruction cycle time, 2.3 µs 16 x 16-bit register multiplies, and 2.6 µs 32/16-bit register divides. In addition, the H8/532 supports "C", making it easier for you to put its power to work.

The H8/532 ZTAT™ (Zero Turn-Around Time) microcontroller features an unprecedented amount of one-time user-programmable EPROM...32 Kbytes. The ZTAT microcontroller gets you to market fast. The very day you finish development. No waiting for mask ROM parts. You get unbeatable flexibility—change code instantly without creating an inventory of obsolete devices. The ZTAT feature also saves you money by eliminating mask charges and minimum order quantities. For high volume, you can go to a mask ROM version of the H8/532 for the lowest high-volume unit cost.

The H8/532 contains a wagonload of on-chip peripherals; including 1 Kbyte RAM, 8-channel 10-bit A/D, 8 timers, a serial communications interface, 65 I/O pins, and a data transfer controller—all tightly packed in a small, surface-mount plastic package. This combination of high integration and large memory makes the H8/532 a true single-chip solution.

Now you have the right device for challenging office automation, automotive, industrial, and telecommunications applications. Applications requiring heavy-duty math, I/O, or timing control. The H8/532 provides the horsepower for a broader range of applications than you thought a single 8-bit microcontroller could ever manage.

Development with the H8/532 is easy, with our full stable of development tools running on IBM PC* or VAX* computers: a "C" compiler, a cross-assembler, a simulator/debugger, an in-circuit emulator, ZTAT programming socket adapters, and a low-cost evaluation board. The H8/532 has a familiar architecture, and its instruction set is similar to industry standards.

With the H8/532, you can harness a whole team of Hitachi devices to work together in your application: memories, peripheral devices, logic, LCD drivers, opto and analog ICs.

The H8/532 is the first in a long line of new H8 workhorses. Each created for a different cost/performance objective. All H8 devices have the bloodlines common to all Hitachi products—quality and reliability. For more information on the hardworking H8/532, contact your local Hitachi Sales Representative or Distributor Sales Office today.

Literature Fast Action: For product literature only, CALL TOLL FREE, 1-800-842-9000, Ext. 6809. Ask for literature number SB-110.

*IBM PC and VAX are trademarks of IBM Corp. and Digital Equipment Corporation, respectively.

Hitachi America, Ltd.

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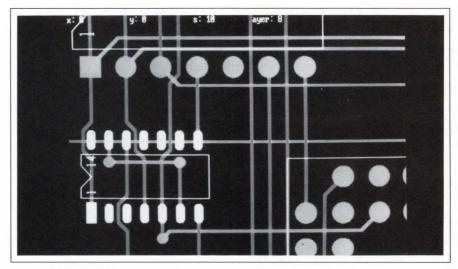
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

PC-BOARD AUTOROUTER

- Includes schematic-capture and layout features
- Handles 32×32-in. boards and 255 trace widths

DC/CADPAC is a pc-board design, layout, and routing package that runs on IBM PCs and compatibles. It includes a multipurpose graphics editor, an annotating design-rule checker, a rat's nest generator, and a rip-up-and-retry autorouter. The package can handle designs with as many as 64 layers, boards as large as 32×32 in., and as many as 255 trace widths. Features include route prioritizing for critical nets, user-defined pad shapes, square or round vias, and area-fill for analog requirements. You can obtain drivers for a wide variety of graphics



cards that provide resolution as great as 800×600 pixels; a driver is also available for the Metheus graphics card, which provides resolution of 1024×768 pixels. Com-

plete package, \$495.

Design Computation Inc, Sherman Sq, Route 33, Farmingdale, NJ 07727. Phone (201) 938-6661.

Circle No 401

LOGIC SIMULATOR

- Lets you specify timing via diagrams or text
- Provides a high-level language for stimulus definition

WEASYL (Waveform Editor And SYntax for Logic simulation) consists of four modules. The waveform editor is a graphics editor that lets you specify timing by means of diagrams or textual notation. A highlevel language, similar to C, allows you to describe stimulus sequences in terms of the mnemonics and waveform data. The stimulus generator generates signals that can be used by simulators from various vendors; after running the simulation, the comparison module compares expected output data to actual simulation results and reports mismatches. The waveform editor and logic language are simulatorindependent. The software runs on IBM PC, Sun 3, and Apollo 3000 hosts. On the IBM PC you need an EGA card and compatible monitor, and at least 640k bytes of RAM. From \$795 for the waveform editor,

\$695 for the logic language module, \$495 for the stimulus generator module, and \$695 for the comparison module (IBM PC versions).

Compass Development Inc, 2890 Zanker Rd, Suite 209, San Jose, CA 95134. Phone (408) 432-0715.

Circle No 402

COMPONENT MATCHER

- Matches components according to measured tolerances
- Selects group of components having largest number of matches

TQC 2120A Component Matching Software runs on HP 9000 Series 200/300 computers under Basic 5.0 or higher. The program accepts input in the form of a table of measured data that lists component identification numbers, measurement points, and matching tolerances. Using a 2-pass approach, the program first determines which components fall within the tolerance level you've specified. It then iteratively selects groups of matched component sets. You can specify the num-

ber of iterations, and when the program has completed this number of cycles or when it has determined the optimum match, it reports the component ID numbers of the set that contains the largest number of matches. \$2800.

Test Quality Co, 2316 Walsh Ave, Santa Clara, CA 95051. Phone (408) 986-8880.

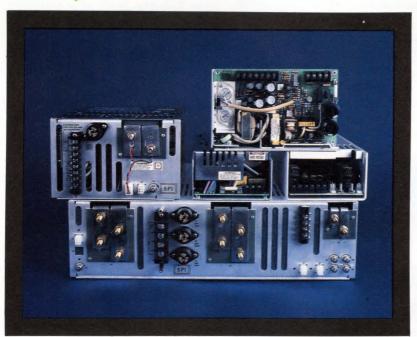
Circle No 403

LAYOUT SYSTEM

- Handles pc boards and hybrid circuits
- Provides resolution down to 0.001 mil

Omnicards Release 4 is a layout system for pc boards and hybrid circuits that provides both automatic and interactive operation. This release contains major enhancements such as all-angle trace routing for analog and dense digital designs; an improved rip-up-and-retry autorouter that achieves higher completion rates on very dense circuits; implementation of partial vias; in-

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CIRCLE NO 97

Bus-board development in miniature.

Adding to Dage's successful Foundation enclosure family is Fastframe, a completely selfcontained miniature bus-based board system. Fastframe offers a full-system capability while its compact design and low cost combine to make it ideal for bench-top prototyping, exhibitions, field service or as a 'one per student' training station.

Compatibility with VME, STE or Multibus II boards provides users with a comprehensive operating environment. Fastframe has its own integral power supply and backplane, and an open-sided construction allows easy access to boards under test or development. External devices are powered via rear-mounted 5 and 12V connectors.

Foundation Fastframe further enhances Dage's wealth of in-depth hardware and software expertise for real-time system builders. For a single source of standard products and full custom facilities make Dage your first choice.



Backplane Systems **Technology Division**

Dage Precision Industries Incorporated

46701 Fremont Boulevard, Fremont, California 94538, U.S.A. Telephone: (415) 683 3930

Telex: 4990512. Fax: (415) 683 3935



creased resolution of 0.001 mil to accommodate metric spacings and thin-film (chip-on-board) technologies; and additional plotter drivers for the Calcomp and Houston Instruments plotters. Enlarged system limits now allow the system to handle boards as large as 100 in. per side and as many as 1000 16-pin

IC equivalents, with as many as 500 pins per component. A GDS III Stream Output program allows you to generate masks for thin-film hybrids; other new utilities include design-verification and parameter-extraction programs. The system runs on Sun and Apollo workstations. The Omnicards software

costs \$12,000; price of a complete system (including workstation) is less than \$40,000.

Task Technologies Inc, 7635 Main St Fishers, Victor, NY 14564. Phone (716) 924-4180. FAX 716-924-4189.

Circle No 404



The SR560 Low-Noise Preamplifier

is the ideal voltage amplifier for the most demanding applications. With a low 2 nV/\Hz of input noise, even the smallest signals won't get lost. Two adjustable signal filters, each configurable as high or low pass, attenuate unwanted interference. Internal batteries provide operation isolated from the AC line.

And the best news of all, the SR560 is priced at only \$1695, including remote interface. Whether you need lower noise, higher gain, or greater bandwidth, call Stanford Research Systems and take a closer look at the SR560.

\$1695

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1MHz bandwidth
Gain variable to 50,000
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True differential or singleended input
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operation
Remote interface



SRS

Stanford Research Systems

1290 D Reamwood Avenue, Sunnyvale, CA 94089 TEL (408) 744-9040 FAX 4087449049 TLX 706891 SRS UD

CIRCLE NO 99

SIMULATOR

- Event queue permits mixed digital/analog simulations
- Provides behavioral modeling facilities

The addition of an integral event queue to Saber allows this simulator to handle mixed analog/digital designs. Analog models create new rows and columns in Saber's system-solution matrix: digital models are scheduled as events in the queue, but do not become part of the matrix. Thus, the program can, with some limitations, act as a stand-alone mixed-mode simulator. You can describe digital devices at the behavioral level or at the gate level; behavioral modeling lets you describe cells easily and accurately, yet at the same time provides a measure of control over proprietary information such as topology and process parameters. The event queue also allows you to use your existing Verilog, HILO, or CADAT digital simulator in conjunction with Saber, to provide facilities such as fault simulation and automatic testvector generation. A new algorithm lets you use either Saber or your digital simulator for primary control of the simulation. This algorithm allows Saber to take optimum timesteps until a digital event requires analog processing; Saber then re-evaluates its solution and either continues forward in time or adjusts backward to guarantee accuracy. Native mixed-mode capability is available as part of the Time Domain Modeling package for Sun, Apollo, or Vax hosts; prices start at \$5000. Saber/Verilog will be available later in 1989 for Sun and

Why our button makes the better rechargeable.



Today, Varta leads the world in for the smaller NiCd batteries. The reason lies in understanding the two ways cells are made. One is Varta's original development: the mass-plate NiCd button cell. Its electrodes are thick, solid masses with small surface areas. Result: a very low self-discharge which provides up to four times longer stand-by life and reduced charging current.

In the other cells, the long, thin, sintered electrodes, which are wrapped around in a cylindrical shape, have a large surface area. Result: cylindrical cells with an inherently fast self-discharge. Most of these NiCd batteries have a useful stand-by life of less than 3 months and, in use, require more frequent charging with "heavier" charging current.

Better operational characteristics. Mass-plate construction results in NiCd batteries with no "memory" effect, so they can be trickle-charged long-term without reduction in effective capacity. They have a longer, 1000-cycle life, according to IEC 509. And they can be stored in any state of charge

for over five years Self discharge comparison at 20°C without significant performance loss.

% ssol 40 Capacity |

Safer, tougher.

Mass-plate design protects against overcharge and/or overdischarge. Mass-plate cells perform better under vibration, as shown by MIL STD 810C. Key cell sizes are UL-recognized. They can be wavesoldered for up to 10 seconds in a fully charged state.

Electrodes in mass-plate button cells have far less surface area, so self-discharge is far less, stand-by life is up to four times longer, and charging requirements are much smaller.

More sizes and types for any application. Mass-plate cells range from 4 mAh (world's smallest) to 1000 mAh. Taking up to 40% less space, batteries are available flat or stacked with all types of connections. Safetronic and Mempac batteries are pin-equipped for easy plug-in.

New "high-temperature" types. The Varta DKT Series can operate up to 65°C, 15° higher than before.

Most cost-effective. Despite their advantages, mass-plate buttons are competitively priced. For more information, on Varta button cells and batteries, please ask for our booklet "Eight Reasons Why...". Call 1-800-431-2504, Ext. 260, or write below.





VARTA Batteries, Inc., 300 Executive Blvd., Elmsford, NY 10523, USA, Tel. 1-800-431-2504, Ext. 260 VARTA Batterie AG, Am Leineufer 51, D-3000 Hannover 21, West Germany, Tel. (49) 0511/79031 VARTA Batteries Pte Ltd., 1646 Bedok North P.O. Box 55, Singapore 9146, Tel. (65) 241-2633



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Glassman High Voltage Inc.

Route 22 (East) Salem Industrial Park, PO Box 551 Whitehouse Station, NJ 08889 Telephone (201)534-9007 TWX 710-480-2839 FAX: (201)534-5672

CIRCLE NO 102



CAE & SOFTWARE DEVELOPMENT TOOLS

Apollo hosts; prices will start at \$35,000. Price and availability of Saber/HILO will be announced later in 1989.

Analogy, 9205 SW Gemini Dr. Beaverton, OR 97005. Phone (503) 626-9700.

Circle No 405



DEBUGGER

- Allows you to debug software at source-code level
- Includes a C interpreter

Running on a PC, C-Spy allows you to debug at the source-code level software that's written for 8- and 16-bit microcontrollers in C. You can use it to view your code either at the source-code or machine-code level in user-configurable on-screen windows and with the assistance of help menus. You can single-step the software one C statement at a time while tracing any variable, or you can use advanced breakpoint logic. C-Spy fully supports local variables, including variable type recognition and recognition of the C "define" and "include" statements so that you have direct access to all the symbols used in the source code. In addition to a built-in assembler and disassembler for the target processor, the debugger also has a C interpreter that allows immediate execution of C statements. C-Spy is available either as a software de-

velopment tool that emulates your target processor, or as a version that operates with a range of incircuit emulators. The debugger works with the company's range of ANSI C cross-compilers, and is available for 8051, 68HC11, 80C196, Z80, 64180, and 6301 target processors. In addition to running under MS-DOS, C-Spy is also available for running under OS/2 and on VAX, HP, and Sun workstations. £700 for the PC-based software-development-tool version.

IAR Systems, Garden Studios. 11-15 Betterton St, London WC2E 9BP, UK. Phone 01-379-0344. TLX 265639. FAX 01-240-6093.

Circle No 406

BASIC FOR 8051

- Conforms to Intel's Basic-52 standard
- Supports in-line assembly-lanquage code

BXC-51 is a compiler that runs under PC-DOS or MS-DOS and accepts source-code written in Basic-52; it generates machine code for Intel's 8051-family µPs. Thus, you can do your development work on an 8052, which has the on-chip Basic-52 interpreter; when you've completely debugged your program, you can transfer the source code to an IBM PC or compatible for compilation. You can then run the compiled code on target systems that are based on the lowercost 8052/8032 processors, which don't have the on-chip interpreter. If you are willing to accept certain restrictions, you can use a compiletime switch that causes the compiler to generate code that you can run on the even less-expensive 8051/8031 chips. The compiler conforms strictly to the Intel Basic-52 standard, including all of the extensions such as interrupt support, I/O, and real-time clock support. The compiler output is in Intel hex format and is compatible with most PROM programmers, monitor/de-

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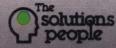
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Binary Technology Inc, Main St, Meriden, NH 03770. Phone (603) 469-3232.

Circle No 407

DATA COMPRESSOR

- Lets you double the capacity of hard and floppy disks
- Runs under PC-DOS 2.0 or higher on IBM PCs and PS/2s Squish Plus is a DOS logical-device driver that doubles the capacity of hard and floppy disks without the expense of installing new hardware. By adding a Device line to your Config.sys file, you define a Squish drive that has a new drive letter. The driver compresses data when you write to a Squish drive and expands the data in memory when you read from a Squish drive. Because the program does not use hot keys

or interrupt traps, the program is

always "well-behaved," and there are no potential conflicts with other

programs. The driver allows you to

protect your compressed files with encrypted passwords. The compres-

sion algorithm is very fast and handles small files and files as large as 512M bytes. \$99.95. Sundog Software Corp, 264 Court St. Brooklyn, NY 11231.

FAULT GRADER

Phone (718) 855-9141.

• Lets you develop and analyze test vectors as part of the design

Circle No 408

• Supports multilevel modeling technologies

QuickGrade is a statistical faultgrading tool for the rapid and thorough evaluation of simulation and test stimuli. The program provides a list of undetected faults and an estimate of overall test coverage; you can then use these results to develop effective test vectors, evaluate the testability of the design, and determine the comprehensiveness of current logic simulations. Because the program executes rapidly, you can make multiple runs to determine which testpoint placements yield the most complete fault-grading statistics. The program displays fault flags directly on the schematic, graphically pinpointing the location of untested or untestable circuitry. Once Quick-Grade reports that you've achieved your target fault coverage, you can analyze the test vectors to develop a diagnostic database for ATE and failure-effects analysis. The program is an integral part of the vendor's Idea Series of design and test tools, and works with all of the modeling methodologies available in the tool set; thus, you don't need to develop a model specifically for fault grading. From \$11,900.

Mentor Graphics Corp. 8500 SW Creekside Place, Beaverton, OR 97005. Phone (503) 626-7000.

Circle No 409

Z80 DEBUGGER

- Operates with both simulators and emulators
- Lets you debug C or Pascal source code

The XRAYZ80 Toolkit runs on IBM PCs and compatibles, and consists of a C or Pascal compiler, an assembler, a software Z80 simulator, and a source-level debugger. This toolkit is the first high-level debugger for the Z80 that operates with either a software simulator or an in-circuit emulator (ICE), according to the vendor. After preliminary debugging with the aid of the simulator, you can perform final testing of your software in the target system, using the vendor's ICE or one from Applied Microsystems Corp, Hewlett-Packard, or ZAX Corp. The debugger is compatible with the vendor's C and Pascal compilers, and it provides a programmable window interface that lets you separate the debugging information into meaningful groups. You can

lets you debug your software *before* target hardware is available. One that supports in-target

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CIRCLE NO 104

for PC/AT/386 & PS/2

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	Nat	ional Instruments PCIIA
\$395	\$395	IEEE 488 board with Quick BASIC & BASICA driver for PCs and compatible
1	1	BASIC ON SRQ GOSUB capability
1	√	IEEE printer/plotter redirection utilities
V	1	Compatible with Windows 286 & 386
√	√	Compatible with IBM GPIB board
√	N/A	DMA beyond 64K segment boundaries
√	N/A	BASIC ON ERROR GOSUB capability
V	N/A	Instrument control directly from DOS
√	N/A	Borland Quattro spreadsheet support
√	N/A	DADiSP waveform spreadsheet support
	+\$495	Lotus 1-2-3 spreadsheet support
	+\$495	Lotus Symphony spreadsheet support
V	+\$100	On-board crystal oscillator
V	+\$50	Turbo BASIC support
√	+\$50	True BASIC support
√	+\$50	Microsoft C support
1	+\$50	Microsoft Quick C support
√	+\$50	Aztec C support
√	+\$50	TURBO C support
√	+\$50	Microsoft FORTRAN 4.0 support
√	+\$50	TURBO Pascal support
V	+\$50	8086 assembler support

\$395 \$1,935 Total

Add \$100 to each for IBM Micro Channel PS/2 support.

If you already own a National Instruments PCII or PCIIA, IBM GPIB, or any NEC 7210-based IEEE board, Driver488 from 10tech provides the software features above for only \$195. Also, our GP488B IEEE board at \$295 is an economical



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CIRCLE NO 106

CAE & SOFTWARE DEVELOPMENT TOOLS

scan source code, monitor program variables and expressions, trace procedure calls, and set simple or complex conditional breakpoints. A macro feature allows you to associate a C function with an event such as a breakpoint or user-defined window; this feature also lets you patch source code, display data structures, and simulate hardware devices. Prices for a complete toolkit start at \$3500 for an IBM PC; the XRAY debugger is available separately for \$1750.

Microtec Research Inc, 2350 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 980-1300. FAX 408-982-8266.

Circle No 410

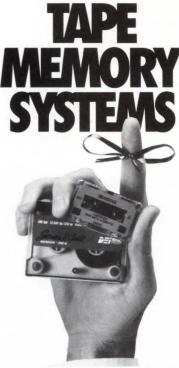
VAX/PC CONNECTION

- Lets you connect VAX computers to IBM PCs via Arcnet
- Allows access to VAX applications resident on a server

The VNBACP NetBIOS interface establishes a transparent communications link between tasks that reside on the same or different nodes of an Arcnet network. The package includes connections for popular terminal-emulation programs, thereby allowing an IBM PC to access any VAX computer connected to the network. VNBACP/SMB includes the Syntax SMBServer, which maps NetBIOS resource names onto VAX RMS directory trees, to allow access to VAXresident application programs. Single-license pricing starts at \$3000 for VNBACP and \$6000 for VNBACP/SMB. Arcnet interface boards cost extra.

C&C Technology Inc, Bldg 9, Unit 60, 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (312) 231-0015.

Circle No 411



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factor. Designed for the DC 2000 cartridge media. These drives represent a breakthrough in performance, ease of integration, and user convenience.



For more information call: 1-800-328-2719

CIRCLE NO 107

EDN May 25, 1989

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Kodak

Kodak is the name in high-performance batteries that designers and end users trust.

The Kodak Ultralife® lithium power cell is the 9-volt to specify for maximum long-life performance. With *twice* the service life of conven-

tional alkaline 9-volts, it reduces battery changes and equipment downtime. Its innovative design is right for your most innovative designs. Flat-folded ribbon electrodes utilize the full interior of the cell.

The 9-volt Kodak
Ultralife lithium power
cell is your choice for
longer life expectancy
and consistent discharge
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temperature performance. What's more, you can also choose the new 3-volt Kodak Ultralife lithium battery. This 3.6 ampere hour Ultralife

battery delivers high capacity at 3 volts. It makes an excellent backup power source for a wide range of applications, especially in computers and memory systems.

And where alkaline battery performance must be specified, depend on the full line of Kodak Supralife® alkaline batteries...just like millions of your end users do!

Typical Discharge Characteristics U9VL 1800 OHMS (4mA) CONTINUOUS DISCHARGE 9.0 7.0 6.0 9.0 4.0 6.0 0.20 4.0 6.0 8.0 100 120 140 160 180 200 220 240 260 280 SERVICE LIFE (HOURS)

KODAK BATTERIES DEPEND ON US.



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Eastman Kodak Company, c/o Ultra Technologies Inc. P.O. Box 267, Newark, NY 14513 1 800 242-2424, 315 332-7230

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

RISC DEVELOPER

- Supports 40-MHz systems based on Am29000
- Includes ROM simulator pod

The Adapt II 29K is a hardware/ software development system for the Am29000. The unit supports processor operation at clock rates as high as 40 MHz and includes a ROM-simulator pod that permits fast debugging and patching of ROM-based code. These capabilities make the system suitable for complex tasks; for example, debugging of interrupt-handling routines in ROM. The system hardware consists of an instrument chassis, cables, and pods; it includes a logicstate analyzer and provides triggerin and trigger-out connections to a second, external state analyzer. You provide the host PC or ASCII terminal. System software supports third-party tools and includes a



hexadecimal debugger, a macroassembler with linking loader, an ANSI C compiler, and the Xray29K source-level debugger. \$13,500.

Step Engineering, Box 3166,

Sunnyvale, CA 94088. Phone (800) 538-1750; in CA, (408) 358-7730. FAX 408-773-1073. TWX 910-339-9506.

Circle No 416



PROGRAMMER

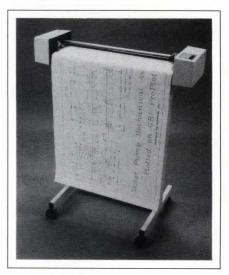
- Programs PALs, (E)EPROMs, PROMs, and µcontrollers
- Can have as much as 8M butes of RAM

The XP2M device programmer supports all current 24-, 28-, 32-, and 40-pin EPROMs, EEPROMs, flash EPROMs, and EPROM microcon-

trollers. By adding optional modules, you can also use the unit to program bipolar PROMs and PALs. The programmer supports fast programming algorithms and can gangprogram devices so they're identical or arranged as sets. Data integrity is checked by program verification and checksum checks after devices are programmed. The unit has 256k bytes of RAM, but you can expand this to 8M bytes if required. Other features include the protection of system parameters against operator modification and an 80-character display for memory editing and message display. The XP2M has parallel and serial communications ports that allow program downloading and full remote control of programming operations. £945.

Industrial Electronics Ltd, Unit E, Huxley Close, Newnham Industrial Estate, Plymouth PL7 4JN, UK. Phone (0752) 342961.

Circle No 417



PEN PLOTTER

- Produces drawings on 24×36 -in. paper
- Uses disposable liquid-ink or ballpoint pens

The ProPlotter pen plotter can reproduce the output of desktop CAD software. Using disposable liquidink, fiber-tipped, or ballpoint pens,

Text continued on pg 265

EDN May 25, 1989

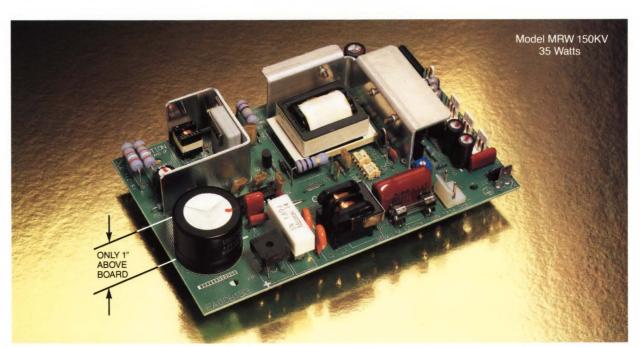


KEPCO TRIPLE OUTPUT,

LOW PROFILE, OEM a-c TO d-c

SWITCHING MODULES

SERIES MRW/35 AND 50 WATTS





- Current trade-off: Current may be increased from one of the outputs at the expense of the others, within the limits defined by Figure 1.
- Adjustable voltage: Internal trimmer accessible through the case allows manual adjustment of the voltage setting.
- Overvoltage protection for principal output shuts down all outputs if output voltage is forced beyond the set limit.
- Holding time: Output is sustained by internally stored energy for 30 milliseconds typically, 20 milliseconds minimum.
- Built-in EMI filter attenuates conducted noise below the requirements of FCC 20780 for Class B computing devices.
- Safety: All models recognized by UL, certified by CSA, and approved by TÜV Rheinland to meet VDE 0806/IEC 380.

SPECIFICATION	MRW 150KV	MRW 160KV	CONDITION	
Voltage range	95 to 264V a-c;	135 to 370V d-c		
Brownout voltage	85V a-c;	120V d-c	Maximum load	
Current	1.0A	1.3A	Typ load, 115V a-c	
	0.5A	0.9A	Typ load, 230V a-c	
Fuse value	2.5A	3A		
Initial, turn-on surge, first 1/2-cycle.	50A	50A max		
Frequency		50/60Hz nominal; range 47-440Hz ⁽¹⁾		
ЕМІ	Meets the co standard of FC0 and VDE 0			
Leakage current	0.5	115V a-c (UL method) 25°C		
	0.75mA		230V a-c (VDE method) 25°C	
Startup time	400msec (typ) 500msec (max)		Std.(2)	
Holdup time	20	Std.(2)		
Circuit type	Fly			
Switching frequency	~100KHz 80KHz typ		Operating	

- (1) At 440Hz the leakage current exceeds the UL/VDE safety specification limit.
- (2) Std conditions = nominal input, nominal load, 25°C

		MRW 150KV			MRW 160KV		
SPECIFICATION	OUTPUT #1	OUTPUT #2	OUTPUT #3	OUTPUT #1	OUTPUT #2	OUTPUT #3	CONDITION
Source effect	1% max	1% max	1% max	2% max	2% max	1% max	95-132V a-c or 190-264V a-c
Load effect	3% max	5% max	1% max	4% max	2% max	1% max	Minimum load to rated load
Temperature effect	2% max	2% max	1% max	2% max	2% max	1% max	Nominal input, rated load, 0-50°C
Combined effect (source, load, & temperature)	+ 4%-2% max	+ 4%-6% max	±6% max	± 4% max	±5% max	±6% max	Initial setting 5.00V ±20 mV
Time effect (drift)		0.5% max					0.5-8.5 hr; nom input, rated load, 25°C
Cross effect Output #1	_	4.0% max	0.5% max	_	4.0% max	1.0% max	Load change from minimum
Output #2	1.5% max	_	0.5% max	1.5% max	-	1.0% max	to typical, nominal input
Output #3	0.5% max	0.5% max	_	0.5% max	0.5% max	_	25°C
Recovery characteristics: Excursion	<4.0%						Step load change from 50% to 100%
Recovery (within ±1%)			<2n	nsec			of rated load. Nominal input, 25°C



MRW	MODE	L TABL	.E										
SPECIFICATION	OUT VOLT	TPUT TAGE	OVP SETTING	OUTPUT CURRENT	CURRENT		OUTPUT POWER		RIPPLE SOURCE SWITCHING		NOISE (SPIKE)	EFFICIENCY	
Units	Vo	olts	Volts	Amps			Wa	atts			mV	mV	Percent
Condition	Factory set ⁽¹⁾	Adjustment range	Nominal Input, 25°C	50°C (See Fig. 1)	Nominal input	40°C	50°C	60°C	71°C	OCCUPATION OF THE PARTY OF THE	nput, typ load p max	d-c to 20MHz p-p max	Nom input, rated load typ
MRW 150K	V (35 WA	TTS)											
Output #1	+ 5	4.75-5.25	5.8-6.9(2)	1.0-2.2 (typ) (4.0 max)	Total maximum					30	50	150	
Output #2	+ 12	-	_	0.6-1.8 (typ) (2.5 max)	output power no more than	35.0	35.0	24.5	14.0	30	50	290	70%
Output #3	- 12	_	_	0-0.1 (typ) 0.3 (max)	38.5 Watts					10	20	290	
MRW 160K	V (50 WA	TTS)											
Output #1	+ 5	4.75-5.25	5.8-6.9(2)	1.0-5.0 (typ) (6.0 max)	Total maximum					30	50	150	
Output #2	+ 12	-	-	0.6-2.0 (typ) (2.5 max)	output power no	output 50	50 35	50 35	35 20	30	50	290	72%
Output #3	- 12	_	_	0-0.1 (typ) (0.5 max)	more than 60 Watts				10	20	290		

⁽¹⁾ Nominal input, maximum load, 25°C (2) All outputs are shut down when OVP is activated

KEPCO TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES

SERIES MRW

These are the first models of a new series of switchers which employ advanced input and output capacitors and magnetics to achieve a very slim profile. In Model MRW 150KV (35 Watts) the overall thickness is 30mm and component length is only 1" (25.4mm) above the PC card. Both models are built on the same card footprint (100 x 160mm), and with the same plug pattern as our popular MRM 144KV, to allow users for whom low profile and/or a wide input range will be significant, to easily upgrade.

FEATURES:

- 115/230V a-c operation without user intervention: Special flyback circuit accepts any input voltage from 95V to 264V a-c.
- Power-OK logic (TTL compatible) signal may be used as power fail signal. Logic "1" is given when +5 output is above 4.5V.

SPE	CIFICATION	RATING/DESCRIPTION	CONDITION	
Temperature		0-71°C (see model table)	Operating	
		-40 to 85°C	Storage	
Humidity		95% RH	Non-condensing; operating & storage	
Shock		20g, 3 axes (11msec ± 5msec pulse duration)	Non-operating 3 shocks each axis	
Vibration		5-10Hz: 10mm amplitude	Non-operating 1 hour each axis	
		10-55Hz: 2g, 3 axes		
Isolation	Output to case	500V d-c, 100MΩ	25°C, 65% RH	
Withstand voltage	Input to output	3.75KV a-c for 1 minute	25°C, 65% RH Y capacitor removed	
	Input to case	2KV a-c for 1 minute	25°C, 65% RH	
Safety		UL 478 recognized, CSA C22.2 certified. VDE 0806/IEC 380 approved by TÜV Rheinland		
Type of construction		PC card		
Enclosure		Optional metal		
Cooling		Convection		









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KEPCO TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES

SERIES MRW





DIMENSIONS MRW 150KV:

inches — 1.12 x 3.93 x 6.3 mm — 28.5 x 100 x 160

MRW 160KV:

inches — 1.5 x 3.93 x 6.3 mm — 38 x 100 x 160

NET WEIGHT

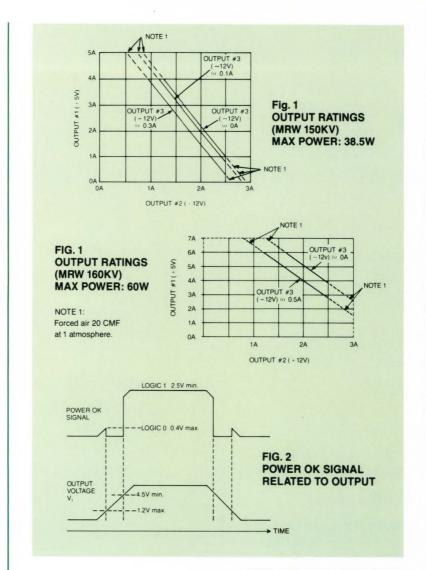
MRW 150KV: 12.35 oz, 350 gm MRW 160KV: 17.65 oz, 500 gm

OPTIONAL STEEL ENCLOSURES:

For MRW 150KV: CA 19 For MRW 160KV: CA 20

INPUT-OUTPUT CABLE KITS:

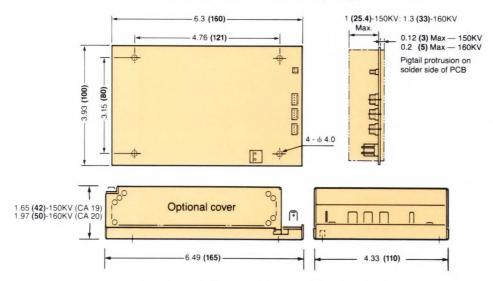
For MRW 150KV — 219-0184 For MRW 160KV — 219-0184





OUTLINE DIMENSIONAL DRAWINGS

Dimensions in light face type are in inches, dimensions in bold face type are in millimeters.



Mounting: 0.16" (4.0 mm) diameter holes — (4) bottom.

the plotter creates drawings on sheets of paper, vellum, or mylar film as large as 24 × 36 in. Maximum pen speed is 7 ips, and resolution is 0.004 in. whereas line width is typically 0.010 in. The supplied software is compatible with Houston Instruments' DMP-series plotters and runs the command set from that series' DM/PL language. \$2395.

Gerard Research Inc. 46745 Fremont Blvd, Fremont, CA 94538. Phone (415) 651-0217. FAX 415-651-0787.

Circle No 418

NETWORK ANALYZER

- Offers 80-dB dynamic range from 100 kHz to 60 GHz
- Provides fully annotated displays

The 2300 scalar network analyzer has four inputs, one of which offers a dynamic range of 80 dB-from



-60 to +20 dBm over a frequency range of 100 kHz to 60 GHz. You can select the reference value and, to improve the ratio of signal to noise, the unit can average signals. The display can appear in either monochrome or color on a composite-video monitor or an IBM PCcompatible RGB TTL monitor. Displays feature full annotation, min/max and delta cursors, and eight independent upper and lower breakpoints. The unit includes an

IEEE-488 port, a 9600-bps RS-232C port, and a private bus that sends graphical data to an HP Thinkjet or compatible printer. \$4000. Delivery, eight weeks ARO.

Boonton Electronics Corp. 791 Rt 10, Randolph, NJ 07869. Phone (201) 584-1077. FAX 201-584-3037. TWX 710-986-8215.

Circle No 419

SCSI BUS MONITOR

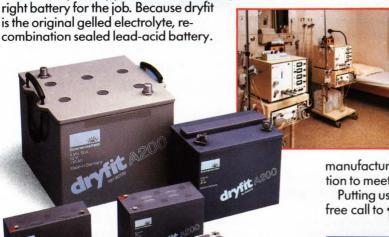
- Resolves 50-nsec events
- Displays trace data graphically or as listings

The Peer-0500 SCSI bus monitor lets you capture and analyze bus activity. Its principal hardware component is a full-sized board that plugs into the IBM PC bus and includes a 32k-word trace buffer whose contents you can display immediately or save on disk for subsequent analysis. Changes in the state

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CIRCLE NO 109

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of SCSI bus control signals or any combination of six external signals can cause the trace buffer to store data. The unit can resolve events as brief as 50 nsec, can time-stamp data with 100-nsec resolution, and can display data either as waveforms or listings. \$2995.

Peer Protocols Inc, 3176 Pullman, Suite 101, Costa Mesa, CA 92626. Phone (714) 662-1929.

Circle No 420



80188/186 EMULATOR

- Operates to 12 MHz
- Allows 217 hardware breakpoints The 80188/186 Icealyzer is an incircuit emulator for the 80186 and 80188 µPs. The emulator supports μP operation to 12 MHz. The unit allows 217 hardware breakpoints and includes a pass counter that can delay breakpoint execution for as many as 216 cycles. All units include a 64k-byte overlay memory that you can upgrade to 256k bytes and whose address range you can map anywhere in the CPU's address space. You can qualify trace data based on address ranges; for clarity, the disassembled output excludes prefetched-but-discarded instructions. A software performance analyzer with 8-byte resolution provides histograms of the percentage of time spent executing code segments. Including symbolic debugger and communications software, \$4495.

Softaid Inc, 8930 Rt 108, Columbia, MD 21045. Phone (800) 433-8812; in MD (301) 964-8455. FAX 301-596-1852. TWX 610-265-2092.

Circle No 421

ACQUISITION UNIT

- Digitizes 50k 12- or 16-bit analog samples/sec
- Compatible with IBM PC, PC/AT, and PS/2 computers

The Model 575 is a PC-based A/D data-acquisition instrument that takes 50,000 measurements/sec. The vendor supplies two versions:

the 575-1 that digitizes analog data with 12-bit resolution, and the 575-2 that provides a resolution of 16 bits. Both units provide two outputs from high-speed D/A converters and allow you to connect eight differential or 16 single-ended analog inputs. They also provide 32 digital I/O channels. The connection

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Amperex Electronic Company, A Division of North American Philips Corporation, Providence Pike, Slatersville, RI 02876. Phone: 401/762-9000 x328 FAX:401/762-9000 x404.

CIRCLE NO 111

TEST & MEASUREMENT INSTRUMENTS

scheme facilitates the use of 3B-series analog signal conditioners made by Analog Devices Inc. The supplied software drivers permit you to control the instruments from programs written in advanced PC Basic (Basica). An optional software package is compatible with several implementations of C and Pascal.



575-1, \$1300; 575-2, \$1600.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-1115; in OH, (216) 248-0400. TLX 985469.

Circle No 422



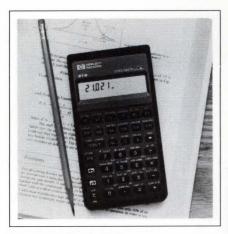


DMM/COUNTER/C METER

- Counts to 200 kHz
- Measures C from 1 pF to 20 \(\mu F\) The Rangemaster II is a voltmeter, ohmmeter, ammeter, frequency counter, capacitance meter, and diode/transistor tester. The yellowcased, handheld unit, whose basic error is 0.5%, is designed for use in rugged environments; it features a built-in tilt stand and sports a 0.7in. LCD. The meter incorporates five ranges each for ac and dc voltage and current. Maximum input is 1000V dc, 750V ac, and 20A ac or dc. The counter's maximum frequency is 200 kHz, and the C meter can measure from 1 pF to 20 μF. \$99.

Extech Instruments Corp, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. FAX 617-890-7864. TLX 940913.

Circle No 423



CALCULATOR

- Calculates statistical functions
- Stores 99-step programs with 16 user labels

The HP-21S Stat/Math (statistical/ mathematical) calculator contains all of the information found in statistical/distribution tables in college-level textbooks. When you work with tables, if the value you need isn't listed, you have to interpolate. The calculator, on the other hand, performs the interpolation for you. According to the vendor, the calculator's program library offers more statistical functions than any other calculator. Furthermore, the $3.1 \times 5.8 \times 0.6$ -in. unit permits algebraic entry, performs time-value-ofmoney calculations, and calculates logarithms and trigonometric functions. The unit includes 10 storage registers and allows programs with 99 steps and 16 user-defined labels. \$49.95.

Hewlett-Packard Co, 1000 NE Circle Blvd, Corvallis, OR 97330. See local dealer.

Circle No 424

TEST OPTIMIZER

- Algorithmically derives device timing
- Implements tests for mixed-signal devices

The Asix-TMP test macroprocessor is a software tool for the creation of optimized test programs that run on the vendor's Asix-2 production test system. The software increases

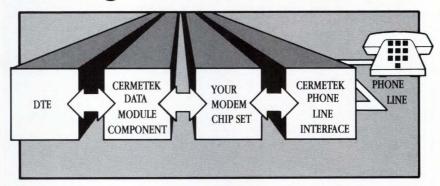
the number of tests that a program can perform and allows testing of additional device types. Included among the devices that the tester can handle with the aid of this software are mixed-signal (analog/digital) parts. Among the functions performed by the software are algorithmic derivation of device timing,

stress testing of CMOS devices, control of "super" voltages that allow initialization of certain PLDs, and generation of custom devicetest menus. \$8000.

Asix Systems Corp, 47338 Fremont Blvd, Fremont, CA 94538. Phone (415) 656-8664.

Circle No 425

Cermetek's Modem Components Are... Quick To Market



When considering a modem design, selecting the proper modem chip set is only part of the solution. You must consider the type of telephone interface used, what method of error control and agency approval needed, either domestic or international. Determining these factors is time consuming, costly and complex. The solution? Cermetek!

Our family of modem components allows the design engineer to surround a modem chip set, making it a complete modem, quickly and economically.

So when you need part of a solution, or the whole modem solution, Cermetek has the expertise and the right answers for you. Find out how Cermetek can enhance your existing or future modem design. Call Cermetek today for more information or write us at:



Modem Components

189X Data Module Features

X.25 LapB, MNP Class 4 and 5, error correcting and data compression, autobaud speed conversion, flow control, RS-232 interface, AT compatible command format driven—1890, 1891, 1892

MNP is a registered trademark of Microcom, Inc.

18XX DAA's Features

Telephone interface, Access Arrangement (DAA)—pre-approved domestic/international, voice data switch, 2- to 4-wire converter, surge protection, isolation, dialing feature, low cost and small size. 1810, 1811, 1812A, 1813, 1814, 1818, 1828

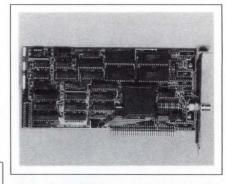
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- Creates 3270 coax-data stream
- Consists of IBM PC plug-in and software

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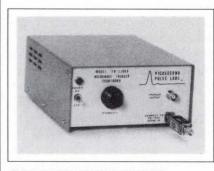
portable IBM PC-based protocol analyzer. The data streams can be as long as 16M bytes and include those required by SNA (systems network architecture), DFT (distributed function terminal), and 3279G graphics. The replay hardware is available as a self-contained IBM PC plug-in card. \$2995; as part



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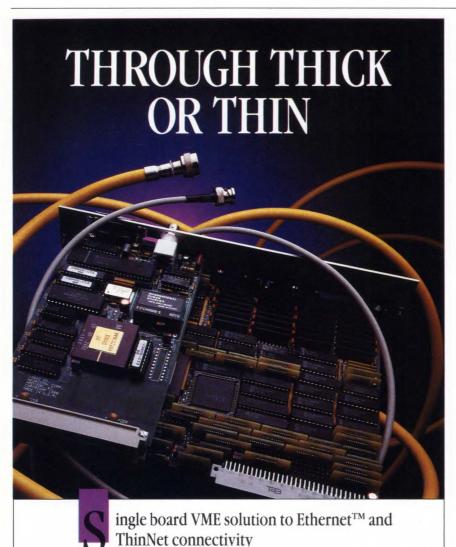
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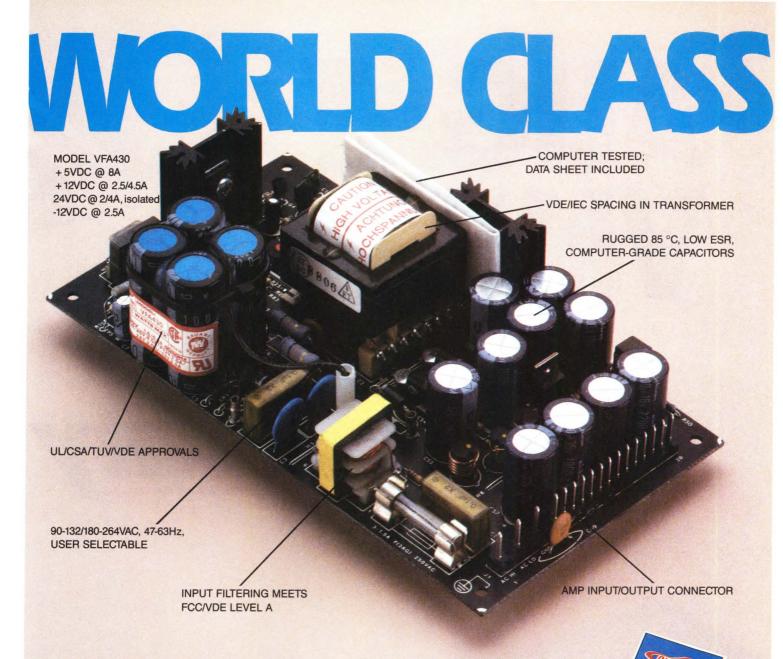
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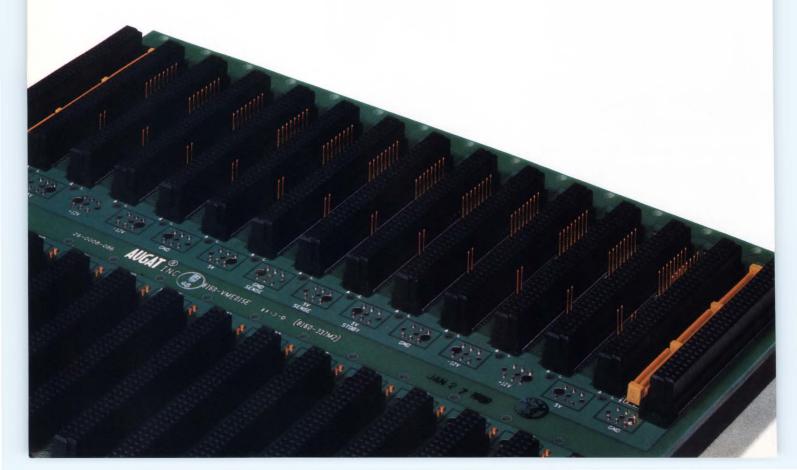
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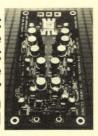
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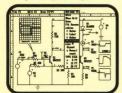
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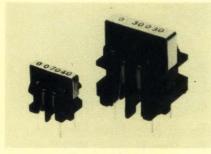
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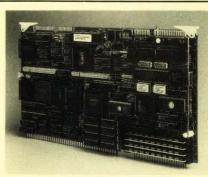
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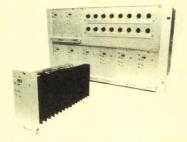
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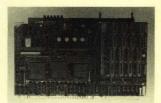
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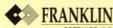
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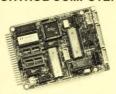
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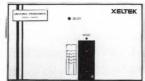
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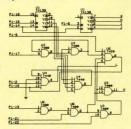
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10801-120th Avenue NE, Kirkland, WA 98033

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Data book features CMOS static RAMs

The company's 1989 Data Book describes its high-speed, high-performance military monolithic static RAMs. The publication also announces the company's intention to produce megabit-density monolithic SRAMs by 1990.

EDI, Literature Dept, 42 South St, Hopkinton, MA 01748.

Circle No 429

How to use the IEEE-1014 and IEC 821 bus

Written as a tutorial to accompany the VMEbus Specification, The VMEbus Handbook—A User's Guide to the IEEE 1014 and IEC 821 Microcomputer Bus follows the organizational sequence of the VMEbus Specification; it provides photos and more than 140 circuit diagrams, tables, and charts. The

book is aimed specifically at system integrator/programmers, hardware engineers, project managers, mechanical designers, and service and production workers. \$39.95.

VMEbus International Trade Association, 10229 N Scottsdale Rd, Suite E, Scottsdale, AZ 85253.

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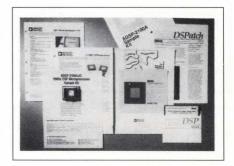
Answers to questions about pc-board CAD

This 36-pg booklet, Answers to the Most Commonly Asked Questions on PCB CAD, provides answers to more than 100 questions about pcboard CAD, compiled from hundreds of conversations with CAD users and potential buyers. Some of the topics include advantages of turnkey vs unbundled systems, pros and cons of different hardware-platform configurations, ways in which training requirements affect

the CAD investment, and how to set up a system for maximum efficiency.

Personal CAD Systems Inc, 1290 Parkmoor Ave, San Jose, CA 95126.

Circle No 430



Sample kit contains DSP information

The vendor's sample kit for evaluating the ADSP2100 digital signal processor includes a 10-MHz ADSP2100A, a simulator demon-

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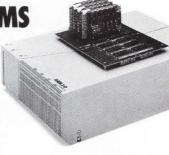
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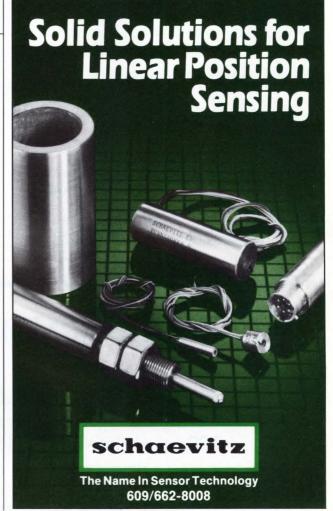
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INTEGRATED CIRCUITS

stration disk and manual, data sheets, and a listing of third-party development support tools. The manual describes how to use the simulation package; program examples include an FIR filter. \$49.95.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021.

INQUIRE DIRECT



Catalog presents electronic-product kits

The vendor's Spring 1989 *Heathkit* catalog offers electronic products in kits. This edition features a picture-in-picture TV kit that allows you to simultaneously monitor two TV programs. The 98-pg publication describes other electronic kits for constructing two airplane models and a sailboat model that are radio-controlled.

Heath Co, Dept 350-041, Benton Harbor, MI 49022.

Circle No 431

Brochure on system for test-process management

This 20-pg brochure discusses the capabilities and advantages of the BoardWatch test-process management system, version 2.0. The publication details the BoardWatch modules for job-plan management, paperless repair, real-time monitoring and alarms, and routing and work-in-process tracking in produc-

Germanium v. Silicon

With his customary eloquence, Oliver O. Ward, President of GPD Corporation and sometimes known as The Chief Justice of Germanium, restated a number of telling arguments:

"In Rectification, Germanium is not only superior to Silicon in both efficiency and forward voltage characteristics, but is particularly so at temperatures from -55°C to 110°C.

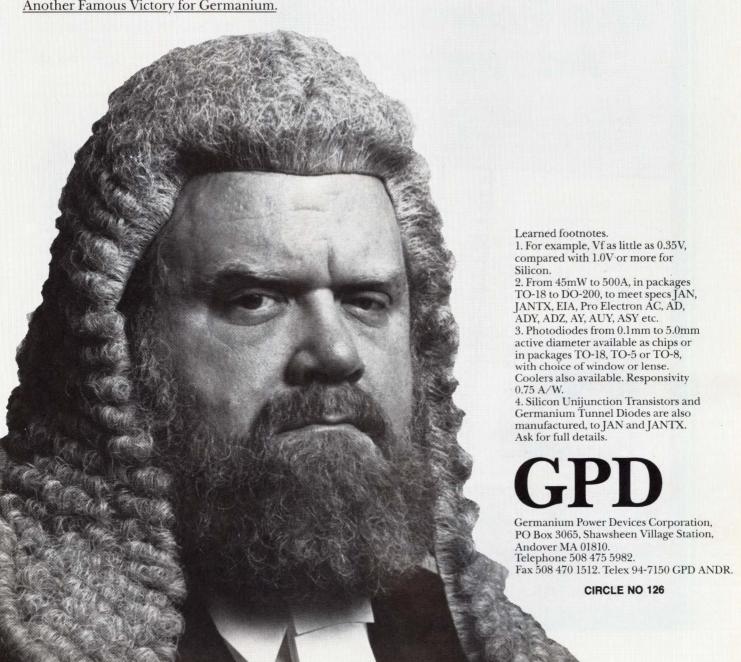
"In Amplification, from small signal to output power, Germanium devices, provide stable performance,

security of supply, and specifications to meet the world's leading technical standards. "In Photodetection, Germanium gives linearity of spectral response, peaking at 1550nm, and offers high-shunt resistance, when required.

"In short, gentlemen," His Honour concluded, "Germanium beats the daylight out of Silicon, in so many important engineering applications."

The Jury, composed of leading figures from the Electronics Industry, retired briefly and brought in a unanimous verdict:

Another Famous Victory for Germanium.



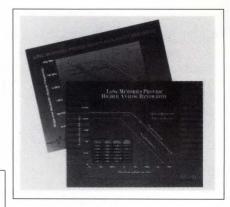
tion board-test environments. Also highlighted in the brochure are BoardWatch's flexible report generation, open architecture, and database integrity.

Teradyne Inc, Inquiry Systems & Analysis, 25 Drydock Ave, Boston, MA 02210.

Circle No 432

App notes emphasize memories of oscilloscopes

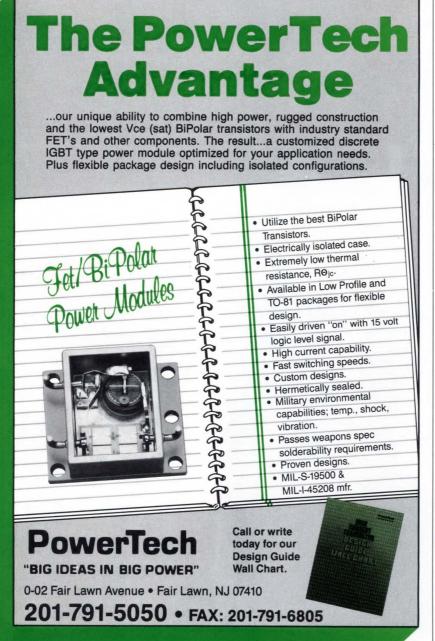
Long Memories Provide Higher Single-shot Bandwidth and Long Memories Provide Higher Analog Bandwidth deal with the benefits of long memories in oscilloscopes. The application notes demonstrate how long memories maintain high

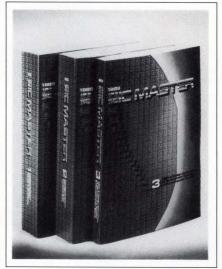


sampling rates and enable the analog bandwidth to remain high over a wide range of timebase settings.

LeCroy, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977.

Circle No 433





Three-volume set covers IC design specifications

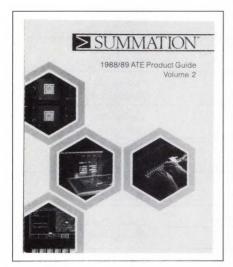
The 1989 IC Master 3-volume softcover set includes 12.000 new ICs and over 150,000 alternate source devices. Volume 1 covers 80,000 standard ICs grouped by basic categories—digital, microprocessor, linear, interface, and memory. This volume includes an alternate source directory, a parts number index, a parts number guide, an application note directory, and an expanded military section. Volume 2 is a stand-alone reference providing technical data for more than 1200 manufacturers' data sheets. It also contains a directory of manufactur-

LITERATURE

ers and distributors. Volume 3 is a systems-level reference for custom and semicustom ICs, including gate array, cell-based ASICs, and programmable logic. A design-automation section provides extensive listings of CAE and CAD design tools. \$140.

Hearst Business Communications, 645 Stewart Ave, Garden City, NY 11530.

INQUIRE DIRECT



Looking over automatic test equipment

The 1988/89 ATE Product Guide, Volume 2 sums up the vendor's 3000-Series functional board test systems that test μP -based boards. The catalog details the measurement, emulation, and pin systems and also focuses on hardware and software options and configuration.

Summation Inc, 11335 NE 122nd Way, Kirkland, WA 98034.

Circle No 434

Publication explains interoperability

Interlan on Interoperability explains how networking works with other devices. The book covers the history of networking, the International Organization for Standardization's 7-layer open-systems-interconnection model, operating systems, network architectures, stan-

dards, and network-management concepts. The text is divided into nine chapters and includes a glossary and an information section listing the various standards organizations and network-oriented publications, \$10.95.

Interlan Inc, 155 Swanson Rd, Boxborough, MA 01719.

INQUIRE DIRECT

Note on techniques for power conditioning

The application note AN8: Power Conditioning Techniques for Batteries examines a variety of voltage-regulation circuits for battery-powered applications. Several approaches for power conditioning are offered for both switching and linear regulators, with emphasis on efficiency and low-power operation. The note describes 14 circuits with schematics and performance data and includes a discussion of component criteria.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle No 435

Book helps you choose a flat-panel display

How to Select a Flat Panel Display, one of the selections for the 1989 Designer's Guide Series, provides both product and "how-to" information. The book contains product data for 290 models of flat-panel displays, database search procedures, worksheets for defining the search criteria, and definitions of terms and attributes. Further, it describes flat-panel graphics technologies and subtechnologies, pointing out the advantages and disadvantages of each. The company provides interim updates, and an optional PC-compatible disk is available. Book, \$95; disk, \$65.

Beta Review Inc, 19 Whichita Rd, Medfield, MA 02052.

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1989 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News Edition
June 22	June 1	Semicustom ICs, Computer Boards	Closing: June 9 Mailing: June 29
July 6	June 15	Product Showcase — Volume I, Power Supplies	Closing: June 22 Mailing: July 13
July 20	June 29	Product Showcase — Volume II, Components	Closing: July 21
Aug. 3	July 13	Integrated Circuits, Computer Boards	Mailing: Aug. 10
Aug. 17	July 27	Military Electronics, Special Issue Military Software	Closing: Aug. 4 Mailing: Aug. 24
Sept. 1	Aug. 10	Test & Measurement, Integrated Circuits	Closing: Aug. 18 Mailing: Sept. 7
Sept. 14	Aug. 24	Industrial Product Showcase, Digital ICs	Closing: Aug. 30 Mailing: Sept. 21
Sept. 28	Sept. 7	Integrated Circuits, Computer Peripherals	Closing: Sept. 15 Mailing: Oct. 5
Oct. 12	Sept. 21	DSP Chip Directory, Integrated Circuits	Closing: Sept. 28 Mailing: Oct. 19
Oct. 26	Oct. 5 T	est & Measurement, Special Issue, Computers & Peripherals	Closing: Oct. 27
Nov. 9	Oct. 19	CAE, Integrated Circuits	Mailing: Nov. 16
Nov. 23	Nov. 2	16th Annual μΡ/μC Directory, Integrated Circuits	Closing: Nov. 9 Mailing: Nov. 30
Dec. 7	Nov. 16	Product Showcase — Volume I, Power Supplies	Closing: Nov. 22 Mailing: Dec. 14
Dec. 21	Nov. 30	Product Showcase — Volume II, Components	

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	Duties and Accomplishments: Industry of Current Employer:	•
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	Reason for Change:	0
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EDN provides accurate, detailed, and useful information about new technologies, products, design techniques, and careers.

EDN covers new and developing technologies to inform its readers of practical design matters that will be of concern to them at once or in the near future.

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- that are immediately or imminently available for purchase
- that have technical data specified in enough detail to permit practical application
- for which accurate price information is available.

EDN's Magazine Edition also provides specific "how to" design information that its readers can use immediately. From time to time, EDN's technical editors undertake special "hands on" engineering projects that demonstrate EDN's commitment to readers' needs for useful design information.

EDN's News Edition also provides comprehensive analysis and news of technology, products, careers, and distribution.

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ADVERTISERS INDEX

Abbott Transistor Laboratories Inc 65	Harris Semiconductor	Powertech Inc 284
Absopulse	158-159, 194-195	Qua Tech Inc
ACCEL Technologies Inc 275	Heurikon Corp 270	Qualidyne Systems Inc 160
ACDC Electronics 88-89	Hewlett-Packard Co 108, 139	Radstone Technology 151
Acme Electric Corp 79	Hirose Electric 42	Raytheon
Active Electric Corp		naytheon
Actel 14-15	Hitachi America Ltd/Electron Tube Sales &	Ready Systems 190-191
Advance Power Supplies Inc 113	Service Div 104-105	Rifa Inc
Advanced Micro	Hitachi America Ltd/Semiconductor	R. O. Associates Inc 83
		그 회사에게 그렇게 되는데 어린 것을 때문에게 되었다면 되었다면 되는데 되었다. 그는 그렇게 되었다면 되었다면 되었다면 그렇게 그렇게 그렇게 되었다면 그렇게
Devices 12-13, 106-107	and IC Div* 248-249	Rogers Corp 276, 279
Advanced Power Tech 170A-D	Hypertronics Corp 278	Rohde & Schwarz** 41
Advin Systems 275	Illinois Capacitor	Samsung Semiconductor* 40-41
Airpax Corp 240	Imprimis Technology 218-219	Seagate Technology 2
Altera Corp 48-49	Inmos Corp 10-11	SenSym
American Automation	Integrated Device Technology Inc 97	SGS-Thomson Microelectronics 142
	0,	
AMP 172-173	Intel Corp 255, 257	Shaevitz Engineering 285
Amperex Electronic Corp* 215, 267	International Test Conference 189	Shelly Associates 279
Amphenol/Spectra-/Strip 220	Interpoint	Siemens Optoelectronics 101
Annapolis Micro Systems 276	Intusoft	Sierra Semiconductor 192-193
Applied Microsystems Corp 121	lOtech Inc	Single Board Solutions 276
Arnold Magnetics Corp 115	ITT ElectroMechanical Components	Softaid Inc 235
Asahi Glass EMP Corp 268	Worldwide 16-17	Sonnenschein Batteries Inc 265
Atmel Inc	Jameco Electronics 277	Sony Corp of America
Augat-Interconnection	Jeta Power Systems 229, 231,	Sorensen Co
Components 272-273	233, 235, 237	Spectrum Software 43
Avantek	John Fluke Manufacturing	Sprague Electric Co 61
Avanti Circuits 231	Co Inc* 174-175	Standard Telephon 203
Basler Electric	Keithley Instruments 176	Stanford Research Systems Inc 252
Bayer AG** 50-53	Kepco Inc** 260A-B	STD Mfg Group 285
B&C Microsystems 277	Kepco Inc*	Switching Power Inc 251
Belden Wire & Cable	Kontron Elec 54	TEAC Corp**
Bertan Associates Inc 266	K-Tronics 204	Tektronix Inc 36-37, 207, 222-225
BP Microsystems 278	L-Com Inc	Teltone Corp 277, 279
Bradford Electronics	Linear Technology Corp 196	Texas Instruments Inc* 50-53
Braemar Computer Corp 258	Littelfuse	Thomas and Betts Corp* 241-244
Burr-Brown Corp	Logic Devices outsert	Tokin America 276
Bytek Corp 233	Logical Advances 277	Tokin Corp
CAD Software Inc 56	Lorain Products 169	Toshiba America Inc 274
CDI Corp—West 276	LSI Logic Corp	Universal Data Systems
		Universal Data Systems
Cermetek 269	LWD Scientific 277	Unkel Software 278
Chips and Technologies	3M Co	UPS
Condor	Marshall	Varta Batteries Inc 253
Converter Concepts Inc 28-29	Mascot Electric**	Venable Industries 81
Corning Electronics 256	MathSoft Inc	Vicor
Cybernetic Micro Systems 228, 278	Maxell	Westcor 6
Cypress Semiconductor 21	Maxim Integrated Products* 69-70	Western Automation
Dage Precision Industries Inc 251	Melcher	Wickman Werke 280
Daisy/Cadnetix 85-87	Mepco/Centralab 171	Wintek Corp 94, 275, 278
Dale Electronics Inc	MetaLink Corp 266	Xeltek
Data I/O Corp 183, 275, 281	MicroSim Corp	Xentek
Datel 280	Mini-Circuits	Xilinx
Densitron Corp	Laboratories 3, 4, 24, 25, 199	Yamaha LSI
		Zendex
Digital Equipment Corp* 210-211	Mitsubishi Electronics America Inc 67	
Directed Energy Inc 275	Molex Inc	Zilog Inc 201
Eastman Kodak 259	Motorola Semiconductor	
Elantec	Products Inc* 251-253	
Eldre Components Inc 214, 278	National Semiconductor Corp 208-209	Recruitment Advertising 286-289
Electrochemical Industries 74	NCR Corp	
Electronic Measurements Inc 246-247	Nichicon Corp	GE Astro Space
		*Advertiser in US edition
Elmec Technology of America Inc 276	Nidec	**Advertiser in International edition
Emulation Technology Inc 279	NMB Technologies 45	Advortion in international outlon
Endicott Research Group 237	Octagon Systems 279	
Exar Corp	OKI Semiconductor	
Ferroxcube	Omation Inc	
Force Computers Inc 30-31	OrCAD Systems Corp 103	
Foxboro Co	Panasonic Industrial Co92	
Franklin Software Inc 279	Panel Component Corp 276	
Fujitsu Limited** 154-155	Performance Semiconductor Corp 35	
	Philips T&M**	
Fujitsu Limited*		
Gates Energy Products Inc 90-91	Pittman	TELL 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Germanium Power Devices 283	Polaroid Corp 44	This index is provided as an additional service. The publisher
Glassman High Voltage Inc 254	Powertec	does not assume any liability for errors or omissions.
Giassinali riigii voltage IIIC 204	10	

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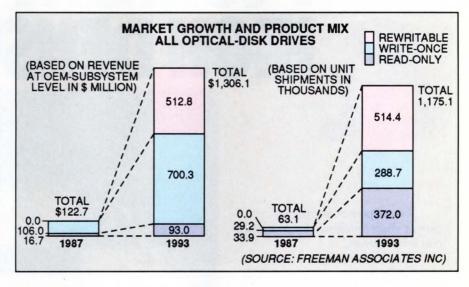
EDITED BY IULIE ANNE SCHOFIELD

Rewritable drives spark optical-drive market

Shipments of rewritable (erasable) optical-disk drives, which began in late 1988, will surge in 1989, predicts Freeman Associates, a Santa Barbara, CA, management consulting firm. It estimates that more than 5000 drives were shipped from three suppliers in 1988 and that more than 40,000 drives will be shipped from nearly a dozen manufacturers in 1989. Revenues from rewritable optical-disk drives are expected to grow dramatically as OEMs and system integrators start using these products.

The worldwide market for all types of optical-data disk drives will exceed \$1.3 billion at OEM price levels in 1993, according to the management consulting firm. This figure represents a 48% compound annual growth rate from the \$123 million value of the 1987 market. More than 1.1 million drives will be shipped in 1993, compared with 63,100 drives in 1987. This increase represents a compound annual growth rate of 63% during this 6-year period.

Write-once drives will lead the market for optical-data disk drives through 1993 in terms of revenue generation. Freeman Associates predicts that these products will account for more than 59% of the total



optical-drive revenue generated during the 6-year period beginning in 1987. Although 1987 unit shipments of write-once drives were only 86% of those of read-only drives, write-once drive revenues were six times those of read-only drives. Freeman Associates estimates that in 1993 write-once drive revenues will be more than seven times those of read-only drives.

Write-once drives in the 1G- to 3G-byte-capacity range will remain the largest revenue producer of any class of optical data disk drives through 1990, when rewritable drives with capacities of less than 1G-byte will dominate the market. Unit shipments of write-once drives with capacities of less than 1G byte

surpassed those of drives in the 1G-to 3G-byte range in 1987 and will widen that edge through 1993. But because of the aggressive price competition in the less than 1G-byte class, the management consulting firm predicts that they will earn less revenue than the larger-capacity write-once drives.

Almost all rewritable drives available between 1989 and 1993 will have capacities below 1G byte. Larger-capacity drives will enter the market in 1990 as specialized mainframe devices. Freeman Associates predicts that revenues from rewritable drives will overtake those of read-only drives this year and reach five times the revenue of read-only drives in 1993.

Market for engine-control chips to decline in '89

The market for semiconductors used to control automobile engines will shrink 11.5% in 1989 to \$232.6 million from \$262.7 million in 1988, according to In-Stat Inc (Scottsdale, AZ). The number of chips used in engine control will drop 9% to 873.1 million in 1989 from 955.2 million in 1988.

This drop in the market corresponds to the decline in the number

of vehicles to be produced in 1989, because all US-made automobiles contain semiconductors to regulate engine performance, fuel efficiency, and emissions. In-Stat expects the US to manufacture only 11.6 million vehicles this year, an 8.7% drop from the 12.7 million produced in 1988.

However, the information company considers the automotiveelectronics market to be a highgrowth area overall. Manufacturers are adding new electronics systems—from active suspension systems and antilock braking to amenities such as trip computers and intelligent climate-control systems—to more vehicles with each model year. In-Stat forecasts the number of electronics systems in US-manufactured vehicles to top 100 million in 1992, up from 51.9 million in 1988.

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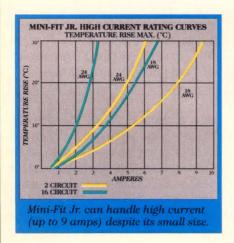
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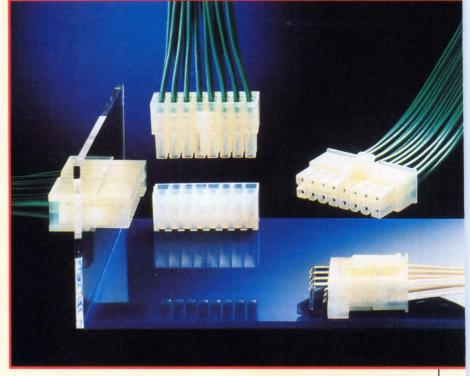
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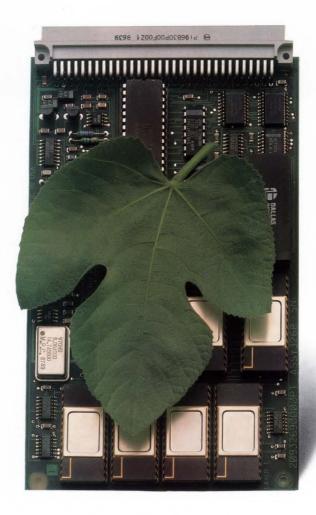
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For the bare facts about technical details and quantity pricing, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/721-8000; Telex 752602 UDS HTV.



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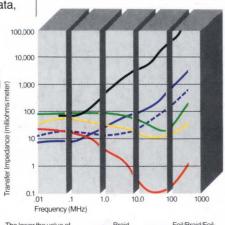
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