EDN

SPECIAL ISSUE: Communications Technology

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ISDN ICs

10M-bps twisted-pair Ethernet standard

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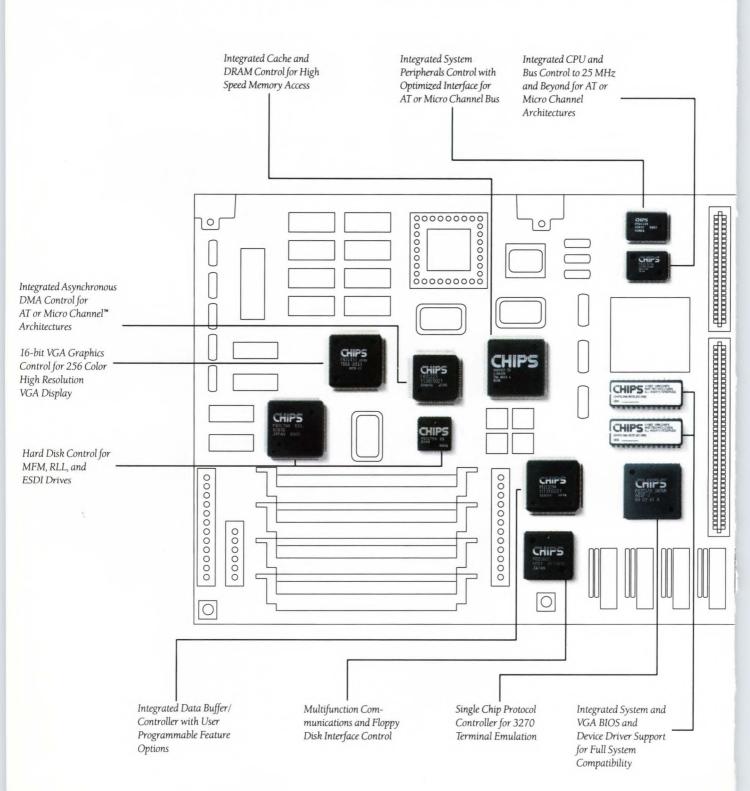
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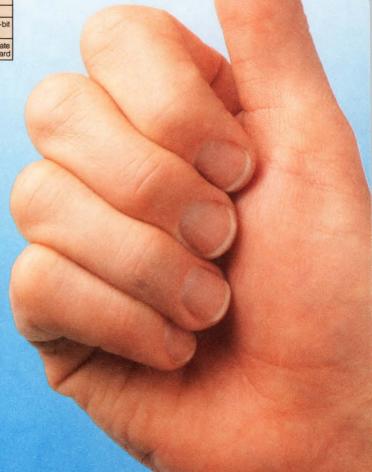
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SPECIFICATIONS

01 -011 10/11/014	_			
Pin Model			KSWA-	
Connector Version	ZFSW-2	2-46	ZFSW/	1-2-46
FREQ. RANGE	dc-4.6 (3Hz	dc-4.6	GHz
INSERT. LOSS (db) dc-200MHz 200-1000MHz 1-4.6GHz	typ 0.9 1.0 1.3	1.3	typ 0.8 0.9 1.5	1.3
ISOLATION (dB) dc-200MHz 200-1000MHz 1-4.6GHz	typ 60 45 30	50	typ 60 50 30	min 50 40 25
VSWR (typ) ON OFF			1.3 1.4	
SW. SPEED (nsec) rise or fall time MAX RF INPUT	2(typ)		3(typ)	
(bBm) up to 500MHz above 500MHz	+17 +27		+17 +27	
CONTROL VOLT.	-8V o	n, OV off	-8V c	n, OV off
OPER/STOR TEMP.	-55° t	o +125°C	-55°	to +125°
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On the cover: Using the latest generation of user-programmable logic devices could be the key to your next successful design. See the Special Report, which begins on pg 146. (Photo courtesy Actel; concept and photography by Imagination; keyboard provided by KeyTronic)

SPECIAL ISSUE: COMMUNICATIONS TECHNOLOGY

SPECIAL REPORT

User-programmable gate arrays

146

The first generation of programmable logic devices (PLDs) allowed you to vacuum up five or 10 TTL devices into one package. The latest programmable devices, FPGAs, can replace many more TTL devices.—Charles H Small, Associate Editor

DESIGN FEATURES

Design linear circuits that serve digital system needs

165

Digital circuits require a slew of analog support circuits to provide life support in the real world. Many of these functions are related to memory support and range from power-sense circuits to voltage supplies for programming onboard, nonvolatile memories.—Jim Williams, Linear Technology Corp

Designer's guide to dynamic RAMs—Part 3 183

To implement a DRAM system, you need a DRAM controller, which acts as a liaison between the CPU and the DRAM. This article, part 3 of a 4-part series, presents the basics of DRAMcontroller design. Parts 1 and 2 of this series introduced the fundamentals of DRAMs and the architectural options available to the DRAM-system designer. Part 4 will consider DRAM-board layout.—Robert Adams and Gregory Scavone, Texas Instruments

Hybrid-IC techniques increase power in motor-drive circuits

195

Thick-film, hybrid-circuit motor drivers not only let you save board space, but also preserve the motor-drive ICs' overtemperature protection and provide a high drive output.—Ed Goodell, Omnirel Corp

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You can now find U-interface ICs from a variety of manufacturers (pg 53).

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TECHNOLOGY UPDATE

ISDN ICs: The U interface comes of age

Most of the issues involving the U interface have been resolved by the standards committees. However, resolving the issues doesn't mean that there is a unifying standard.—*Michael C Markowitz*, *Associate Editor*

10M-bps twisted-pair Ethernet: An Ethernet LAN standard emerges

Before long, board and system designers may have to contend with designing local-area-network (LAN) interfaces based on the emerging IEEE-802.3 10BaseT standard, which will allow data transmission over standard phone lines at 10M bps.—David Shear, Regional Editor

Attenuators solve transmission problems

Digitally programmable attenuators are useful for almost any application in which you need to control signal-amplitude levels. —Tom Ormond, Senior Editor

Micropower op amps hit new lows

You no longer need to sacrifice dc performance for low power consumption when you design with micropower op amps. These devices are now available with input offset voltages as low as 5 μ V and input offset drifts of 0.05 μ V/°C.—Peter Harold, European Editor

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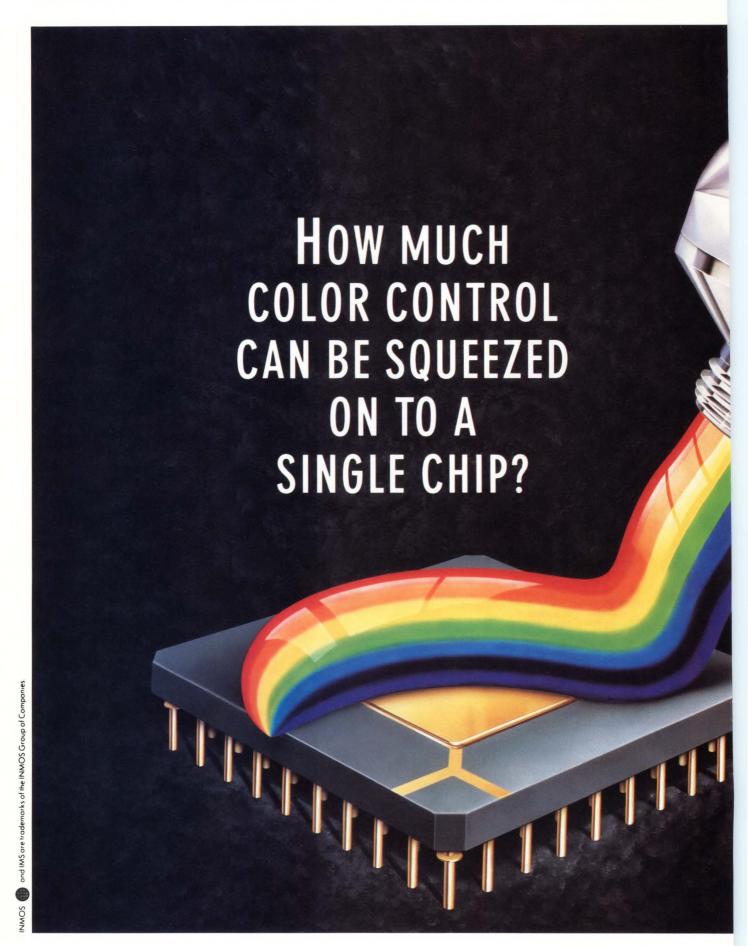
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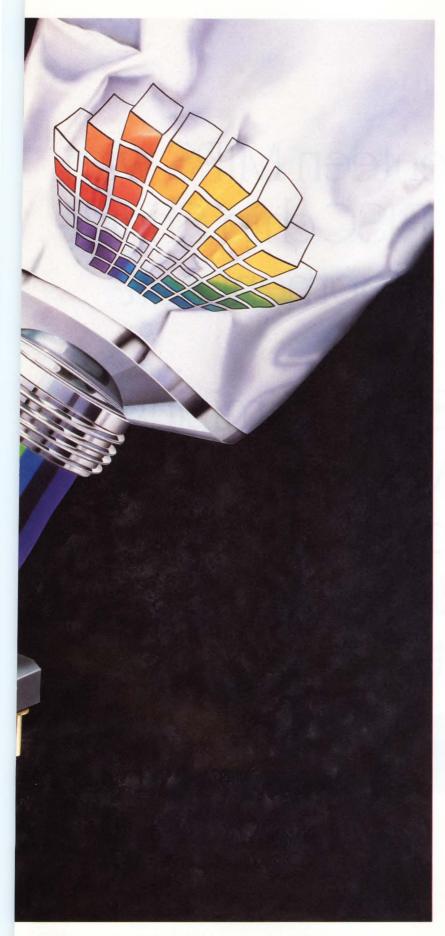
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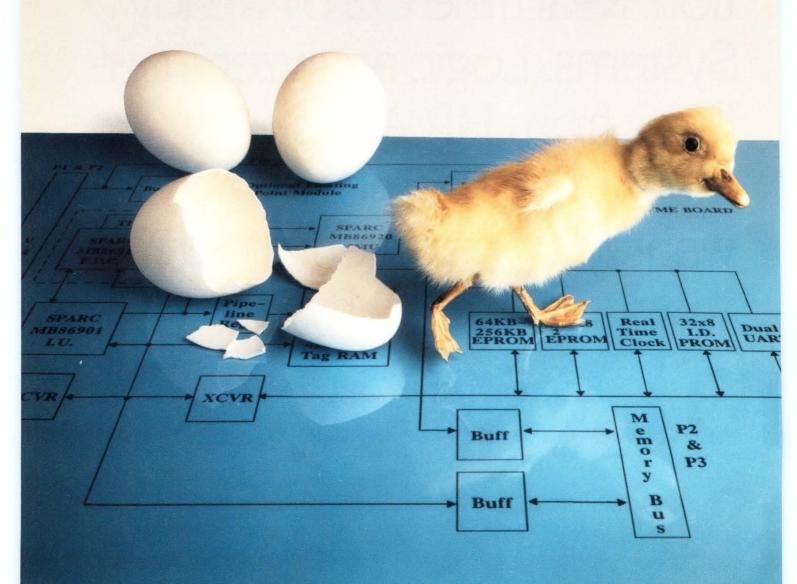
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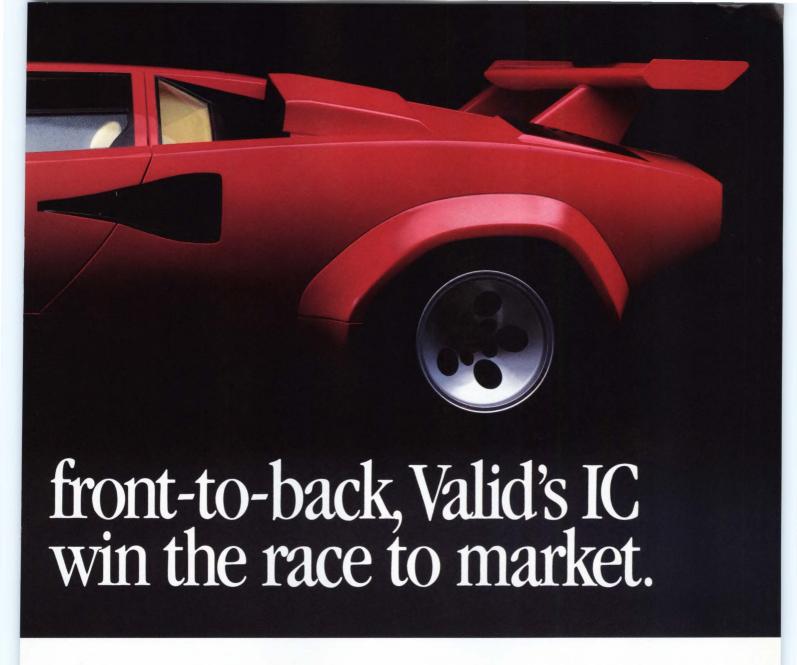
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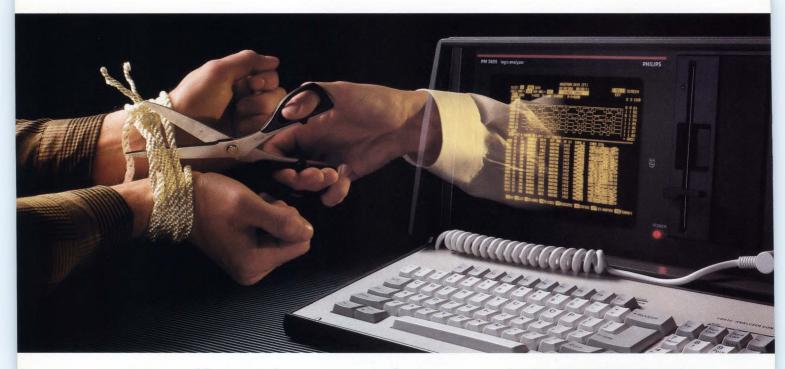
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NEWS BREAKS

EDITED BY JOANNE DE OLIVEIRA

INTEL INTRODUCES THE 80486 CPU

Soon after the release of its 80860 RISC processor, Intel Corp (Santa Clara, CA, (408) 987-8080) announced the availability of its long-awaited 80486 32-bit CISC processor. The 486 is 100% binary compatible with the existing 386 CPU. Implemented in 1-µm technology, the 486 contains over one million transistors and integrates the functions of a 387 numeric coprocessor and an 82385 cache controller as well as paging and memory management. Intel claims the chips offer a twofold to fourfold performance increase over the popular 386/387 combination. The 486 has a 32-bit internal architecture and 32-bit data and address buses. At 25 MHz, the 486 operates at 15 to 20 VAX MIPS and executes 37,000 Dhrystones/sec. Samples of the 486 will be available in the third quarter of 1989; production quantities will be available in the fourth quarter. Beta-site testing of first-run samples is now taking place. The 486, which will initially be available in a 25-MHz version, costs \$950 (1000) and comes in a 168-pin PGA package. Samples of a 33-MHz version will be available in the fourth quarter.

Along with the 486, the company has introduced the 82596 LAN coprocessor and the 85C508 programmable logic device (PLD). The 32-bit 82596 LAN coprocessor is optimized for file servers and single-user and multiuser workstations and minicomputers. The 82596CA (for the 486) costs \$88; the 82596DX (for the 386) costs \$65 (1000). Samples are available now; production quantities will be available in the fourth quarter. The 85C508 PLD provides high-speed, function-specific performance to reduce the interface-chip count in 486 and 33-MHz 386 systems. Packaged in a 28-pin PLCC, the 85C508 costs \$14 (1000); production quantities are available now.

—Dave Pryce

32-BIT CONTROLLER FEATURES INTELLIGENT 16-BIT TIMER

The 68332 32-bit microcontroller from Motorola's Microprocessor Products Group (Austin, TX, (512) 891-3260) is the first member of the 68300 family, a group of controllers specifically designed for embedded applications. The 68332's features were defined by a joint effort between Motorola and Delco Electronics, and General Motors has announced plans to utilize the 332 to manage a variety of automotivecontrol functions in its next generation of automobiles. The 332 consists of five modules: a processing core based on the 68020 microprocessor with additional instructions optimized for embedded-control applications, a second processing unit that services timing events, a module that provides full synchronous and asynchronous communication capability, a system-integration module that reduces external logic components and provides on-chip system-debugging capability, and 2k bytes of static RAM. The two processing units, the CPU and the TPU (time processing unit), are completely independent; the TPU's RISC-like instruction set can simultaneously service as many as 16 timing events without the CPU's intervention. The modular architecture of the 68332 enables Motorola to interchange a host of features and options for different applications. Future 68300 products that are currently under development include EEPROM, DMA, A/D, and ROM products. The 68332 is fabricated in 1-µm CMOS and operates from a 5V supply. The controller requires an input clock of 32.75 kHz; on-chip frequency-multiplication circuitry creates an internal clock of 16.77 MHz. The 68332 comes in a 132-pin plastic quad flat pack. Samples are available for \$125; volume production will begin in the fourth quarter of 1989. A hardware evaluation board is available for \$332.—Anne Watson Swager

EDN April 27, 1989 21

NEWS BREAKS

GRAPHICAL SOFTWARE LINKS ASIC DESIGN TO TEST

Tektronix (Beaverton, OR, (800) 245-2036) has announced a graphics-based software link between ASIC design and test. It allows you to display stimulus files as state or timing diagrams and to edit them extensively. In its initial release, the \$5000 Tekwaves package runs on Apollo workstations and supports Tektronix's LV500 ASIC verifier. The software can import files created by simulators from Mentor, Daisy, Valid, Teradyne, and GenRad. It uses tester-hardware description files in a not-yet-final version of EDIF (the Electronic Data-Interchange Format). Currently, only the LV500 is described in this format, but Tektronix expects that other ATE vendors will make EDIF tester-description files available as soon as the format becomes final. Furthermore, Tektronix plans to offer the software in versions that run on additional vendors' workstations. These enhancements should make Tekwaves suitable for use in almost any company that designs or tests ASICs.

—Dan Strassberg

INTEL WINS EPROM EXCLUSION ORDER

The International Trade Commission (ITC) has ruled that Intel's patents on EPROM technology have been infringed. ITC issued an exclusion order preventing seven companies from importing and selling certain EPROM devices in the US. The seven companies are All-American Inc, Atmel Corp, Cypress Electronics Inc, General Instrument Corp, Hyundai Electronics Industries Co Ltd, Microchip Technology Inc, and Pacesetter Electronics Inc. The ruling prohibits importing, assembling, testing, marketing, distributing, and selling of the affected EPROMs. The products in question are the 64k-, 256k-, 512k-, and 1M-byte EPROMs. The ruling further prohibits the importation of Hyundai electronic equipment containing such EPROMs.

—Richard A Quinnell

SUPPORT FOR SCANNABLE DESIGNS GROWS IN BOARD AND ASIC TEST

As final adoption of the IEEE P1149 testability-bus standard nears, two companies whose products are in the mainstream of board test and ASIC verification have announced products that support the testing of scannable designs. (The term "scannable" refers to several specific design-for-test methodologies.) Teradyne Inc (Boston, MA, (617) 482-2700) has announced a \$20,000 software package called BSD (boundary-scan diagnostics) that can be used with its L200 combinational (functional/in-circuit) board-test systems. The BSD package specifically addresses the problem of fault isolation. Asix Systems Corp (Fremont, CA, (415) 656-8664) has announced a scan-test module, a \$50,000 combination of hardware and software that can be used with its Asix-1 ASIC-development system and Asix-2 production test system. Teradyne and Asix join Gillytron Inc (San Jose, CA, (408) 435-3043), in supporting the testing of scannable parts. Several months ago, Gillytron, a relatively new company, announced complete, low-cost systems dedicated to the testing of scannable devices.

—Dan Strassberg



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NEWS BREAKS: INTERNATIONAL

100-MHz LOGIC ANALYZER BREAKS THE £1000 PRICE BARRIER

Including two TTL-level data pods, the LA3200 32-channel, 100-MHz logic analyzer from Thurlby Electronics Ltd (St Ives, UK, TLX 32475) costs £996. A 48-channel version of the analyzer, designated the LA4800, costs £1195. In synchronous (state-analysis) mode, the instruments provide three external clock inputs, each with a separate clock qualifier and a maximum input frequency of 25 MHz. In asynchronous (timing-analysis) mode, they can capture data on all input channels at an internal clock rate as high as 25 MHz, or data on eight of the input channels at a clock rate of 100 MHz. With suitable data pods, they can also capture glitches.

Each input channel is configurable to a memory depth of 1k or 8k bits, and you can transfer captured data into two nonvolatile reference memories. The logic analyzer's trigger facilities include four full-width trigger words that you can logically combine to produce trigger terms for the instrument's 4-step trigger sequencer. The trigger sequencer allows you to introduce conditional statements—for example, IF-THEN-ELSE commands—and includes event counting at each of its four steps. You can also AND glitch words with the trigger words. Trigger arming can be conditional on the result of a comparison between the trace and reference memories. The analyzers have a 640×200 -pixel, back-lit LCD on which you can display state information in a variety of formats, or display as many as 16 annotated timing traces. An RS-423 interface is standard. Options include an IEEE-488 interface and a range of disassemblers for 8- and 16-bit μ Ps.—Peter Harold

LCD-DRIVER CHIP SET OPERATES AT VERY LOW POWER

Capable of operating at a number of multiplex rates, and drawing only 20 μ A of supply current, the PCF8578 row/column driver can drive 8-row \times 32-column or 32-row \times 8-column dot-matrix LCDs. The chip set is equally suited to driving 7-segment LCDs, starburst LCDs, and LCDs of other formats. By adding PCF8579 column drivers, each of which typically adds only another 20 μ A to the total amount of current drawn, you can drive an LCD as large as 32 \times 1280 pixels at a multiplex rate of 1:32. Each PCF8579 controls 40 LCD columns.

The devices, manufactured by Philips' Components Div (Eindhoven, The Netherlands, TLX 35000; in the US: Signetics Corp, Sunnyvale, CA, (408) 991-2000, incorporate a pixel-mapped display RAM, which can, if required, double as scratch-pad memory. Display refreshing is automatic, and the on-chip display RAM features autoincrement addressing and display bank switching. The drivers have an I^2C bus interface for overall control of display-system parameters. They operate from a 2.5 to 6V supply over the -40 to $+85^{\circ}C$ temperature range. The drivers are available in 56-lead surface-mounting very-small-outline packages, or in a form suitable for tape-automated bonding or chip-on-glass assembly methods. Both devices are priced at around \$3.30 (50,000).—Peter Harold

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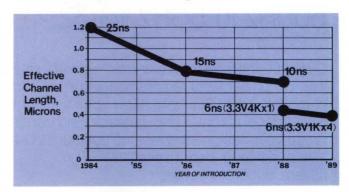
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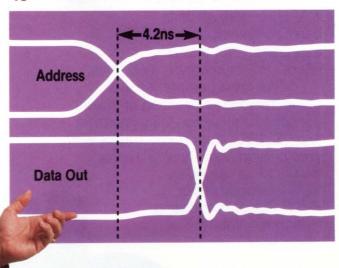
Tom Longo

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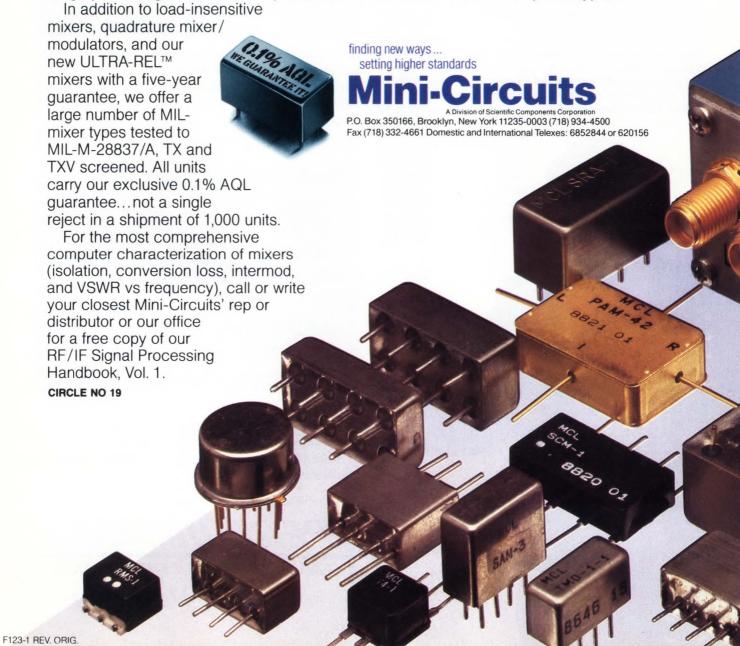
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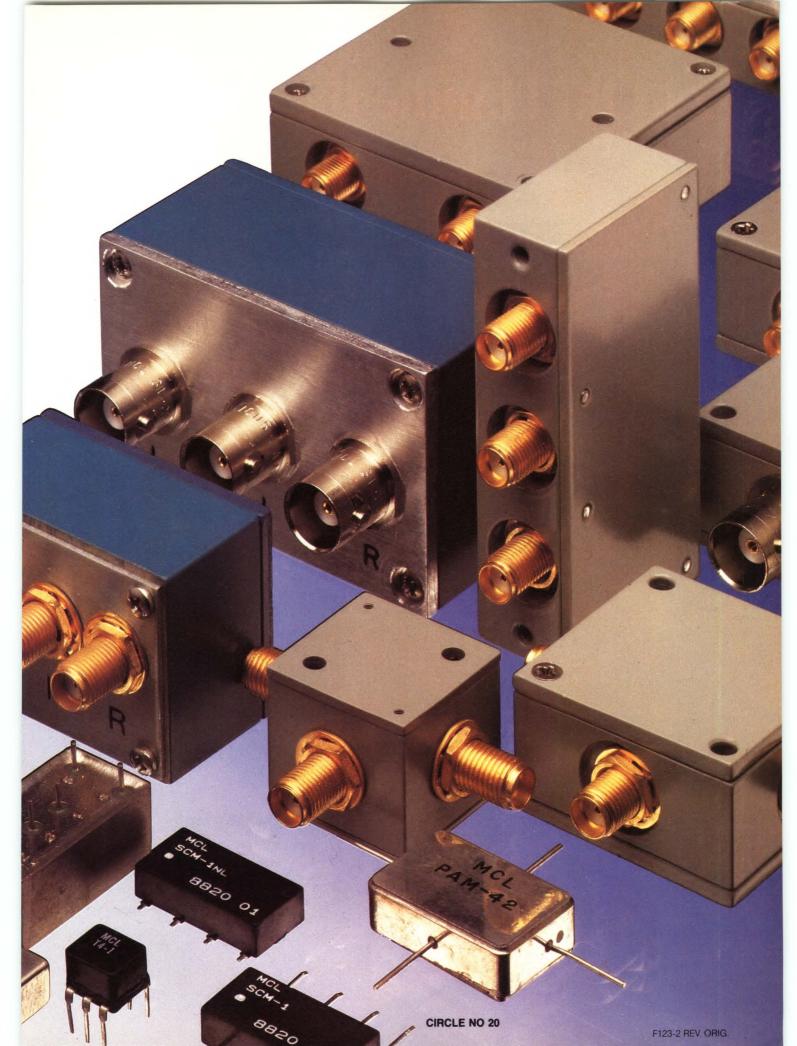
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one 2 Logical Link Control

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Oki's new PSCC provides automatic support for protocols—together with great networking flexibility

The new Protocol Serial Communications Controller (PSCC) from Oki Semiconductor is a highly innovative VLSI device which automatically supports LAPB and LAPD HDLC protocols and saves you from having to program and manage them. With a speed of 10 Mb/s, the PSCC also gives you great networking flexibility.

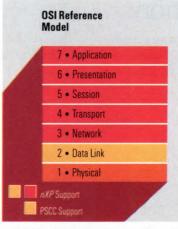
Integrated functions

The PSCC combines a full-duplex HDLC channel, on-board DMA controller, and 520 bytes of internal RAM. It allows you to send and receive messages directly from memory and frees system intelligence for higher level functions. It automatically supports the update and comparison of state variables for multiframe transmission. In addition, the PSCC supports collision and priority detection.

For even greater integration, the PSCC will be imbedded in Oki's high-performance 16-bit *nXP* microcontroller which will support all seven OSI levels of the ISDN.

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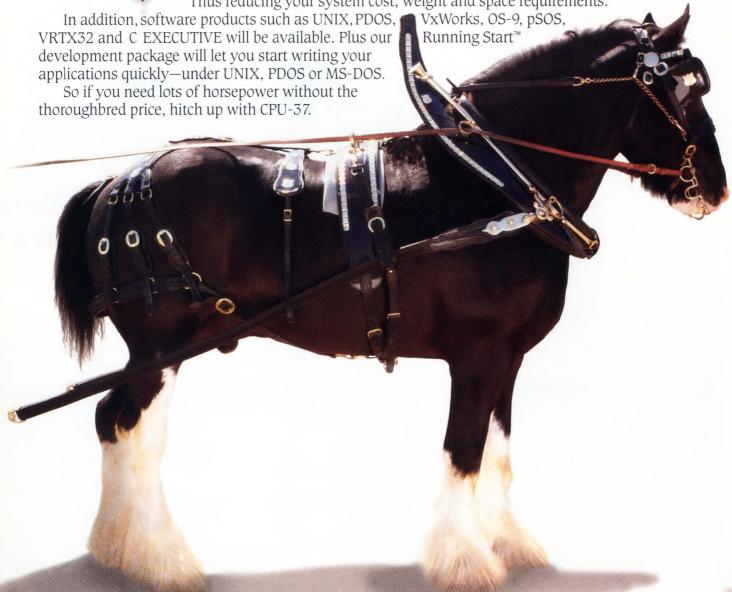
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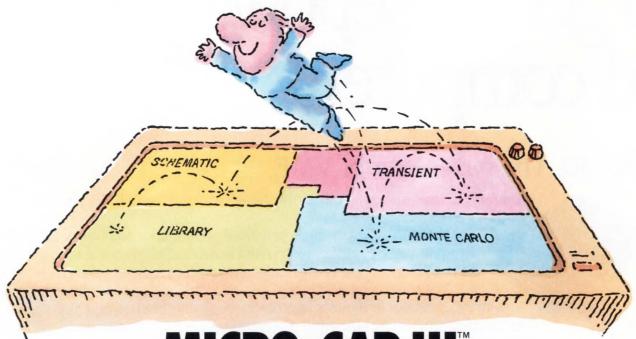
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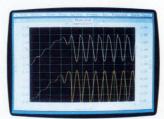


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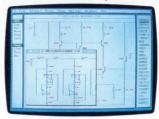
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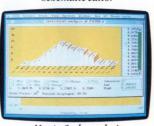
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SIGNALS & NOISE

Alien grads should be free to stay in the US

I read Jon Titus's editorial "Send alien graduates home" (EDN, October 27, 1988, pg 57), and I was surprised. As a former "alien graduate," I am very resentful of the fact that Jon's editorial advocated that foreign students should be forced to go home after graduation. If you walk into any high-tech business today, you will find a substantial number of engineers who were born abroad, many of them enjoying the wealth of this country. The opportunity to attend high-quality universities and to work in environments that offer professional development, challenges, and opportunities allows them to return some of the debt they owe this country for letting them reside here. Many of us have contributed heavily to the success of the industry in this country. Many innovations and inventions were developed by foreignborn scientists and engineers who selected this country as their new home.

Jon mentioned in his editorial that foreign-born engineers are taking jobs away from US citizens, but he did not mention that many of them opened businesses that employed many US citizens. Some examples are Dr Wang, Bose, and many other entrepreneurs. So please at least consider the positive aspect of having "foreigners" stay in the US.

I understand Jon's concern about the underdeveloped countries and the need for skilled people to help in their development; however, I do not feel that the US government should force professionals to become a foreign-policy tool. Let the people decide whether they want to help in the development of their countries of origin (by the way, some of those countries were hell on Earth for those people). In addition, I resent the idea that a country's need should dictate my profes-

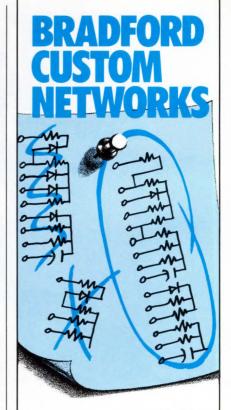
sional interests: If I would like to be an EE, CE, ChE, etc, I'll make the decision.

As an engineering manager, I have recruited engineers in the past, and it was next to impossible to find engineers with the skills and talent I needed. In spite of extensive advertising and the willingness to pay a fair wage, I could not find engineers to fill the jobs (many trade magazines were stating that there was a severe shortage of engineers).

I am just wondering about the quality of information available to Jon. He stated in the editorial that foreign engineers "often work for less." In 18 years of working in the US, I never experienced salary deprivation because I was a foreigner. Yes, there might be some businesses that practice discrimination toward foreigners, but any reputable one would not do it, and I can testify from my own experiences.

Jon also mentioned his summer visit to a developing country and his observations regarding the energy being used, and how wasteful it was compared to solar or wind energy. Without knowing the details of his trip or the depth of his investigation, I would venture to assume that the issue is more political than technical. Solar and wind power are well-established technologies, and the issue is how to introduce them, not how to engineer or invent them. You will find similar issues in many Third-World countries. We, the foreign-born engineers, can do very little to influence political issues. Our skills are in the technical field, and in the right environment, we can do miracles.

On behalf of all the foreign-born, American-educated engineers, I would like to state that we would like to have free choice in selecting our home. This country is a conglomeration of nationalities, religions, races, creeds, and professions,



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CIRCLE NO 26

SIGNALS & NOISE

and let it stay that way; that is what made this country great.

Amos Friedner Engineering Manager Digital Equipment Corp Marlboro, MA

Letting alien grads stay in the US benefits everyone

The advice to "send alien graduates home" (October 27, 1988, pg 57) ignores the larger perspective on immigration and naturalization. The current policy answers the basic US need for an optimal population base, while spreading benefits globally.

The US Department of Justice took a well-considered decision in 1966 to admit 200,000 foreign nationals yearly to the USA as immigrants. This decision was the result of a study on US demographics that projected the population growth to be insufficient to sustain the economy at a viable level beyond the vear 2000 or so. Immigrants thus provide that vital extra fodder needed for the insatiable economic and industrial giant that the USA will continue to be throughout the 21st century. To suggest that foreign graduates should be returning while the less-educated immigrants remain is unfair.

Returning home is not the only way an immigrant can help his or her native land. The US and the "donor" countries reap mutual long-term benefits from the immigrant population. Poland, Israel, and Japan are just a few of the countries deriving advantages through their native sons and daughters living in the USA. And the favor is by no means one-sided.

M K Sadagopan AT&T Bell Laboratories Naperville, IL

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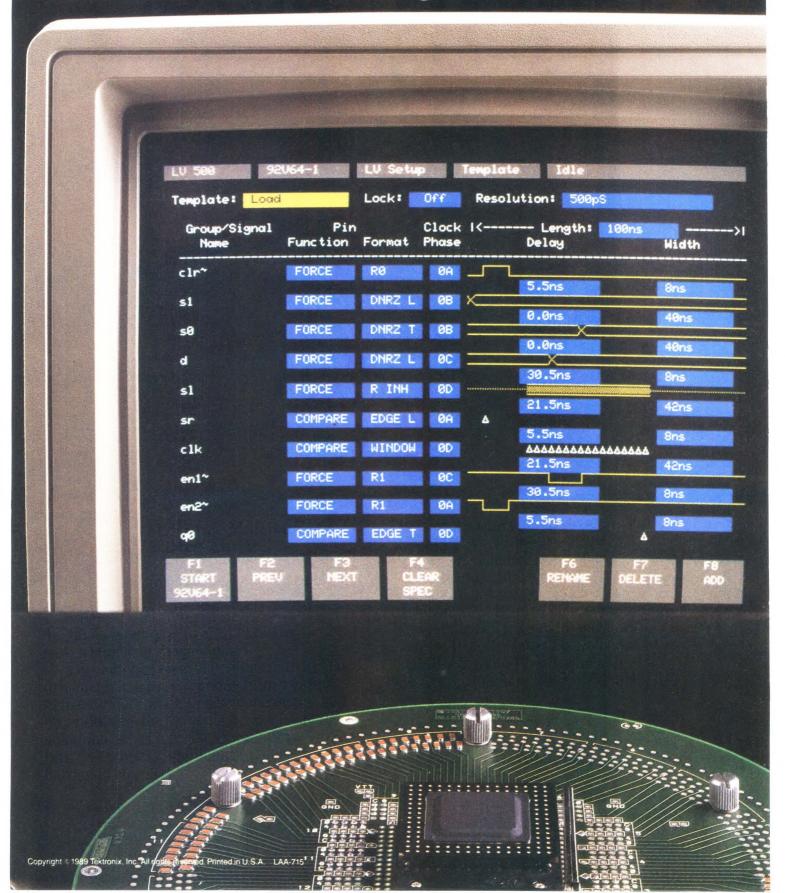
PLX packs everything into slim, 300-mil by 24-pin DIPs, or 28-pin LCC packages.

Suddenly, valuable board space is opened up, leaving you loads of extra room to implement that breakthrough design. Best of all, you'll finish way ahead of your competition.

Get on the fast track with bus interface chips from PLX Technology. Call us at 415-960-0448. Or write PLX Technology, 625 Clyde Ave., Mountain View, CA 94043.



Tek's New ASIC Verification System.





Big Tester Performance At A Benchtop Price.

or a fraction of the price of large production testers, designers can now easily perform timing verification and margin analysis on their own ASICs, using a turnkey system with the critical timing of the million-dollar machines.

Tek's new LV 500 ASIC Verification System is a true *designer's* solution, integrated into a 50 MHz, 256-channel, 64K deep benchtop system with a test head just 17 inches square.

Using a simple menu structure and concepts familiar to the designer, the LV 500 combines elementary operation with astonishing performance, made possible by integrating all 256 bidirectional channels onto a single PCB. Results include:

More accurate simulation, even for complex synchronous devices. The LV 500 lets you vary cycle length and timing for each of 16 clock generators on a cycle-by-cycle basis.

Familiar operation for example, template-based test cycles replicate the everyday timing diagrams of your IC book.

Graphic displays. See clearly when devices are operating too close to parametric boundaries.

Thanks to its high degree of integration, the LV 500 rarely needs calibration. DUT fixturing is simplified. And capacitance loading is reduced to about 25 pF, further contributing to the system's accurate results. And it is compatible with virtually all logic simulators.

Don't wait for chips to fail in production—or worse, for products to fail in the field.

Start putting ASIC verification where it does the most good: in the hands of the designers themselves. For more information or a demonstration, contact your Tek sales representative. Or call 1-800-245-2036.



You Know Mitsubishi.

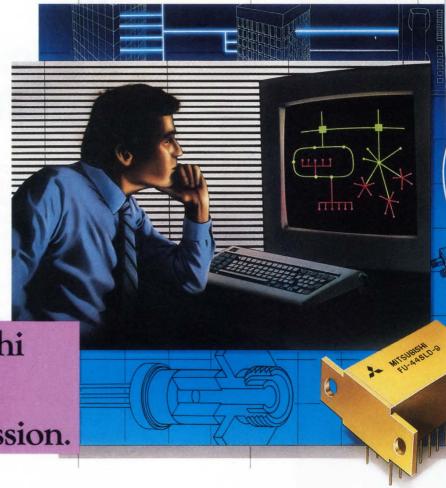
Fiber Optic Transmission...there are many possibilities. The marketplace will determine which designs and components succeed. But today, fiber optic system designers face many questions.

- How can fiber-to-the-home system costs be significantly reduced for commercial viability?

 Is it possible that FDDI-compatible LANs can become cost-effective for PCs and workstations?

 Are there components that meet CATV supplier requirements for AM transmission on fiber?

> Mitsubishi Knows Optical Transmission.



Addressing these issues requires a partnership with the right optoelectronic supplier. One with a broad, integrated product base and sensible solutions. That's what Mitsubishi Electronics offers. We view market needs from our customer's perspective. We understand the critical issues. And we're addressing them now.

We've pioneered many new ideas for the industry. In fact, Mitsubishi was the first company to connectorize (singlemode) 1300nm laser diodes, providing smaller, lower cost options to DIP packages. Then we replaced the 1300nm laser with a CD laser to reduce costs even more. These innovations are proving critical for the commercial realization of fiber-tothe-home and expansion of fiber LAN markets.

As a result, Mitsubishi's connectorized lasers are being successfully evaluated in fiber-to-the-home and computer LAN applications right

now. And, it appears that this package may become an industry standard since many users are beginning to specify connectorized laser packages.

Mitsubishi Electronics offers a broad range of laser transmitters and receivers in all three fiber windows. from 780nm to 1550nm. Our product line includes DFB lasers, PIN and APD detectors, SLEDs, ELEDs and data links...all available in a wide selection of packages.

As your design goals come into focus, working closely with Mitsubishi can result in sensible solutions. And, you'll have the assurance of commitment from a solid, integrated optoelectronic supplier who will be here for the long-term.

FIBER-TO-HOME. MAKING HIGH VOLUME **VIABLE**

Lowering fiber-to-the-home system costs requires lasers that can be produced in high volume production quantities. Traditional DIP packages with fiber pigtail cannot be mass produced costeffectively. So, Mitsubishi developed a singlemode. connectorized laser package specifically for automated high volume production.

With several fiber-to-home pilot programs in progress, Mitsubishi lasers offer extremely high reliability (>100 million hours MTTF) over a wide temperature range and rugged

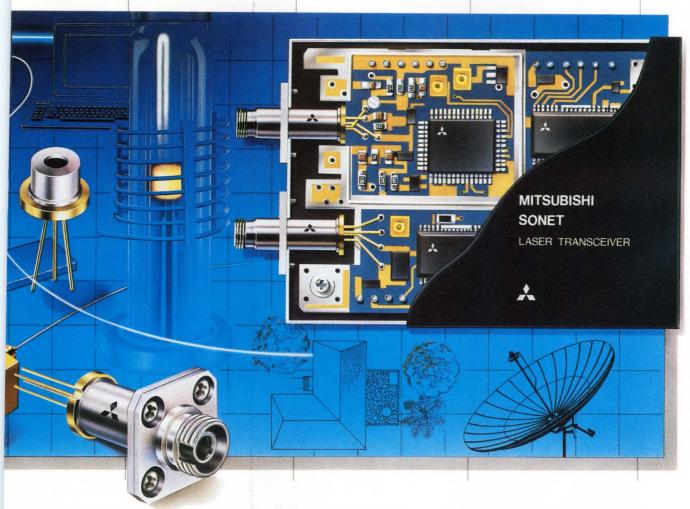
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DATA COMMUNICATIONS. FDDI AND ALTERNATIVES

FDDI-compatible LANs can work for PC and workstation applications. Mitsubishi is developing a new FDDI-compatible data link that will provide a cost-effective alternative to LEDs at both ends (transmitter and receiver) of a fiber link.

By using mass produced, CD lasers and Si PIN detectors, Mitsubishi has reduced fiber optic LAN system costs for more applications.

TELECOMMUNICATIONS

Mitsubishi developed Si ICs for laser transmitters and receivers, offering size reduction and improved performance. We're supplying InGaAs APDs and DFB lasers for high-performance transmission systems. We also offer 780nm, 870nm, 1200nm, 1300nm and 1550nm lasers for WDM designs and bi-directional transmission. And, we are developing a SONET transceiver to meet the emerging standards.

CATV: AM FIBER TRANSMISSION POSSIBLE

With experience in AM, FM and digital video applications, Mitsubishi offers some of the highest power devices available (>10mW from a singlemode fiber) for better S:N ratio in CATV transmission.

We have also developed a 1300nm DFB laser module with isolator that features low RIN and high linearity for AM transmission.

Application	Mitsubishi Part Number	Description
Fiber-to-the-home	FU-01SLD-N(4406)/FU-04PD-N	780nm laser and detector in singlemode connectorized modules.
Fiber-to-the-home and Telecommunications	FU-11SLD-N/FU-13PD-N	1300nm laser and detector in singlemode connectorized modules
AM CATV Transmission	FU-45SDF	1300nm DFB laser with opto-isolator and TE cooler.
Data Communications (FDDI)	MF-13125DF-T/R	1300nm LED/PIN 125MB/S transmitter/receiver
Data Communications	FU-01LD-N(4406)/FU-03PD-N	780nm laser and detector in multimode connectorized modules.
Telecommunications	FU-33AP	Long wavelength InGaAs APD module.

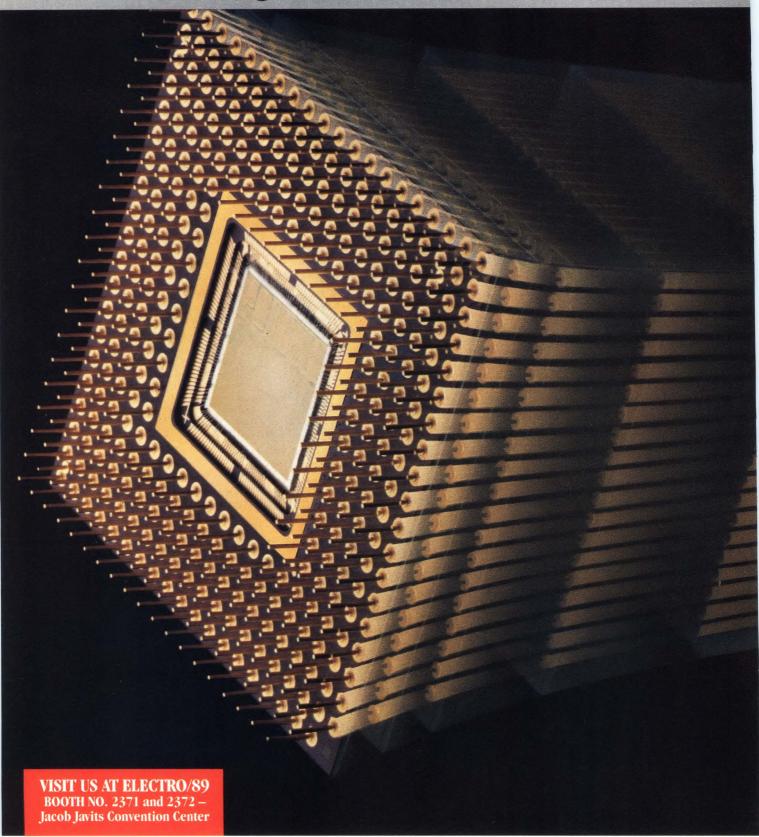




41

EDN April 27, 1989 CIRCLE NO 28

129,000 gates and 400 picosecond to none.



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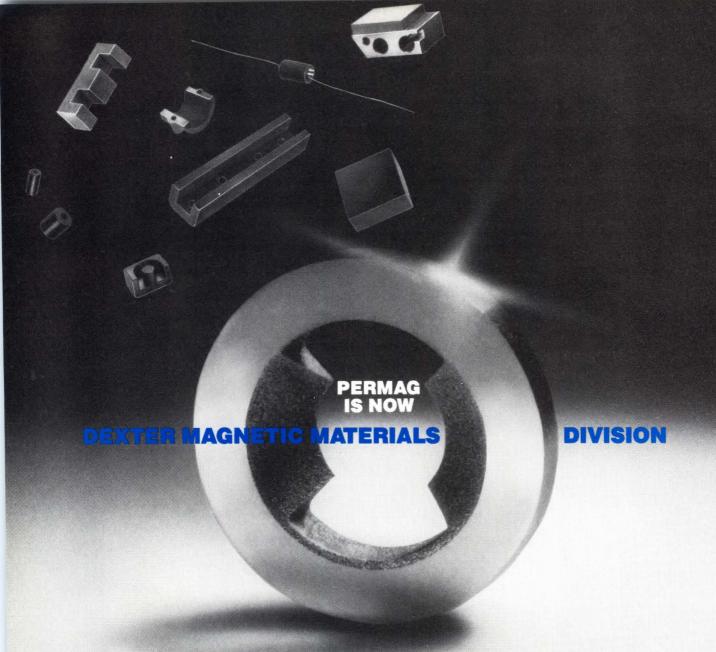
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EDITORIAL

$S(f) = \int_{-\infty}^{\infty} s(t) e^{-j2\pi ft} dt$

PATENT PENDING?



Thankfully, the Fourier integral above was never patented. It's probably safe to say that in the early 1800s, when J B J Fourier analyzed heat conduction, he never thought of applying for a patent on his formulas. Today though, many mathematicians are applying for and receiving patents for their work. Those patents may stifle many further developments.

Certainly new inventions, processes, and techniques should be able to take advantage of our patent system—a system that offers inventors the right to exclude others from using their invention for 17 years. (Keep in mind that the patent system itself offers no protection. Inventors must protect their patented inventions on their own either through licenses or infringement lawsuits.) However, until recently, the US Patent and Trademark Office has turned down patent applications that cover mathematical formulas or algorithms. It used to be that inventors couldn't patent processes that could be performed mentally or with paper and pencil. In short, you couldn't patent mental exercises.

But, you could patent an algorithm if it was tightly coupled to a piece of hardware. For example, if you implemented a new fast Fourier transform algorithm in a patentable circuit, the patent could cover both the hardware and the algorithm it implemented. So, as long as the algorithm was claimed as part of the circuit, you could patent it. Now however, the US Supreme Court is taking a more liberal view of what types of formulas and algorithms you can patent.

The New York Times reports that in 1981 the Supreme Court expanded patent coverage to include the application of a mathematical formula to a known process. In 1982, a lower court ruled that an algorithm could be protected as long as it applied to physical elements or process steps.

We take exception to the courts' rulings. Mathematical formulas and algorithms should remain unpatentable. Certainly, it is proper if someone wants to protect the *implementation* of an algorithm by placing it deep within an integrated circuit, by copyrighting program listings, or by licensing it as a trade secret. However, protecting the basic idea may bring many areas of mathematical research to a halt. Investigators who might benefit from patentable work will be reluctant to share their research results with fellow researchers. It's hard to imagine the state of the software industry if shell-sort, bubble-sort, and floating-point-math algorithms had received patents.

On the other hand, some might argue that there is little incentive to spend years of research and months of programming to develop an algorithm into useful form unless the algorithm can be patented. That's a valid point, but again, it should be the implementation that receives a patent, and not the underlying mathematical principle or process. To stay competitive, and to foster an exchange of mathematical thoughts and ideas, we need an atmosphere that's free of restrictive patent protection for underlying and electrent principles.

ing and abstract principles.



Jesse H Neal Editorial Achievement Awards 1987, 1981 (2), 1978 (2), 1977, 1976, 1975

American Society of Business Press Editors Award 1988, 1983, 1981 Jon Titus Editor

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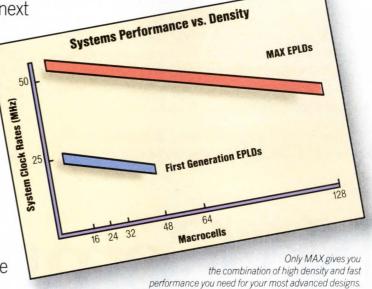
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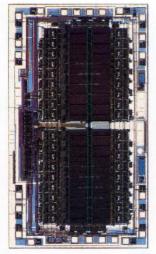
For example, with our EPM5032, you can design a bus controller that runs at 32MHz while utilizing 32 registers and up to 32 product terms feeding a single register.

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Hitachi's Hi-BiCMOS technology helps you eliminate frustrating design compromises. You can count on Hitachi's Hi-BiCMOS process to deliver the speed, density, and low-power performance in reliable, quality parts. For more information, call your local Hitachi Sales Representative or Distributor Sales Office today.

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For single-ended designs, the ML4823 is pin compatible with the UC1823 and adds all the enhancements of the ML4825.

A third new controller, the ML4809, is packed with extra features and functions for better compensation, easier starting

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Synchronization:

- separate clock I/O pins
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- on-chip programmable ramp compensation
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Start-up/Fault conditions:

- 7 V hysteresis on undervoltage lockout
- full reset with programmable delay

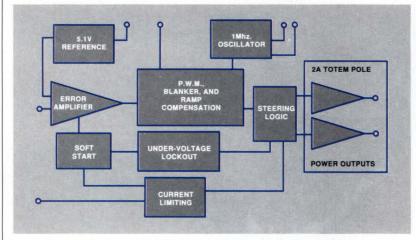
PART TYPE	SOFT START RESET	UNDER- VOLTAGE OUTPUT STATE	COMPARATOR TO OUTPUT DELAY
ML4825	COMPLETE	LOW	40 nS 👃
UC1825	PARTIAL	FLOAT	50 nS
ML4823	COMPLETE	LOW	40 ns
UC1823	PARTIAL	FLOAT	50 nS

Micro Linear/Unitrode Comparison

These three new standard single-chip controllers are so good, they'll easily satisfy the demands of most high-frequency SMPS designs.

For those power supplies with special needs that can't be met by an "off-the-shelf" IC, you'll need a semi-custom controller designed and built to exacting standards.

And we know just where you can find one.



Micro Linear Standard PWM Controllers Provide Maximum Performance

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Introducing the new FB3480, a semi-custom array specifically designed to meet more challenging demands of high frequency

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The FB3480 is a new concept in semi-custom IC technology. Most other analog semi-custom IC's are a collection of general purpose transistors, resistors and other components which can be connected in different ways to perform different IC functions. Not the FB3480. It's

specifically designed for SMPS control. This unique array contains high-performance internal core cells optimized to perform the functions found in all PWM controllers. In addition, the array contains a large area of uncommitted transistors and resistors which can be configured to your specifications

using Micro Linear's library of "soft macros." These macros implement a full complement of logic, comparator and other

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FB3480 Array Enables Easy Custom Design

functions to make your customized controller unique. This "core cell" and "soft macro" design approach provides a customized solution with a minimum of cost and effort.

The core cells feature a 1 Mhz oscillator, a 5 Mhz bandwidth 6V/µSec slew-rate error amplifier, a voltage reference

with a ± 2% tolerance over the full temperature range, and a programmable threshold under-voltage lockout circuit.

The chip also contains two totem-pole 2A output driver cells to quickly charge and discharge the high gate capacitance of power MOSFETs.

For more information on the new single-chip standard and semi-custom SMPS controllers from Micro

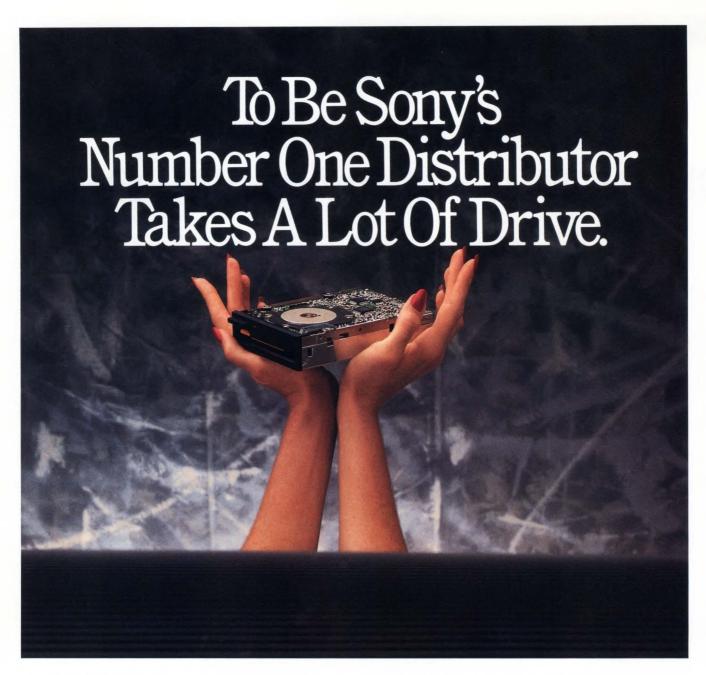
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CIRCLE NO 33





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TECHNOLOGY UPDATE

ISDN ICs

The U interface comes of age



Most of the issues involving the U interface have been resolved by the standards committees, and IC vendors are gearing up to supply the chips. However, resolving the issues doesn't mean that there is a unifying standard.

Michael C Markowitz, Associate Editor he Integrated Services Digital Network's (ISDN) U interface is, in the words of one IC vendor, "defined, but vulnerable." Some of the vulnerabilites revolve around the test and maintenance features and call set-up and tear-down. But most of these problems are addressable in software, and the committee charged with defining the U interface is committed to reverse compatibility. As a result, many IC vendors have begun to introduce their versions of U-interface ICs.

But all is not rosy and waiting for you to begin the design of your network termination (NT1) equipment or central office (CO) and private automatic branch exchange (PABX) line cards (LT) for

the U interface. The T1E1.4 (Telecommunications Interface) subcommittee of the Exchange Carrier Standards Association has issued and the American National Standards Institute (ANSI) has published T1.601-1988, which defines the U interface for North America. The specification, which is also being adopted in Japan, specifies a line code of 2B1Q (2 binary, 1 quaternary). According to Tom Starr, chairman of the T1E1.4 subcommittee, this line code offers maturity, the best technology, and the largest base of support. The

situation in Europe, however, is not as clear.

Unlike in the US, each European PTT (Post, Telegraph, and Telephone Administration) owns all of the NT1s tied to its network. As a result, the PTTs control both sides of the U interface. The monopoly exercised by each of the PTTs has manifested itself in conflicting line-code standards; there are currently six options offered in Appendix 6 of the CCITT Blue Book. The French and German PTTs have chosen 4B3T (four binary, three ternary); British Telecom is leaning toward 2B1Q (two binary, one quaternary).

Two other issues further confuse the European picture. First, the potential exists that all of the PTTs may become



Hardware- and software-development tools, like this PC-based ISDN evaluation system from Siemens, help you with code generation, chip emulation, and test-measurement requirements.

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part of the private sector or be deregulated, a la Ma Bell and British Telecom. Secondly, 1992, the year the European Community is scheduled to become a true common market, is looming large on the horizon and could hasten the privitization and deregulation efforts already underway.

Finally, Tom Starr indicated that the T1E1.4 subcommittee issued the T1.601.1988 specification with some areas of the U interface left for further study. For example, the T1M1.2 (Telecommunications Maintenance) subcommittee is looking at some potential changes to the physical layer of ISDN, which defines the R, S, T, and U interfaces. Any changes to the spec will appear in the form of an addendum to the ANSI standard. Although Starr expects some changes to impact the design of currently available Uinterface ICs, he promises that the committee is making every effort to provide downward compatibility.

The ISDN Basic Rate Network consists of a collection of ISDN-compatible and -incompatible equipment connected across interfaces.



A second-source agreement between AT&T and Intel for the 2-chip U-interface IC set, which is shown here in both vendors' packages, ensures the availability of the set.

For the uninitiated, ISDN is a virtual alphabet soup of abbreviations; therefore, a brief description should help clarify the network. Fig 1 might help you visualize what can be an incredibly confusing mess. Also see the box, "An ISDN glossary" for a more complete description of these ISDN terms.

Terminal equipment type 1 (TE1) is an ISDN terminal, like a digital telephone. You can connect TE1s directly to the ISDN at an S interface. Terminal equipment type 2 (TE2) is a nonISDN terminal, like

an RS-232C or X.21 terminal, that you connect through an R interface to a terminal adapter (TA). You can only connect nonISDN terminals to the S interface of the network through a terminal adapter (TA). The S interface connects to the T interface through a network termination type 2 (NT2) box. This box is an ISDN PABX that functions as a multiplexer concentrating two or more TE1s or TAs.

A network termination type 1 (NT1) box provides physical and electrical termination between the 4-wire S or T interface and the 2-wire U interface. The S and T interfaces are electrically identical, although the protocols that operate over them are slightly different. The T interface exists only to link NT2 boxes to an NT1 box. Finally, the U interface connects the local exchange termination (LT) at the central office (CO) to the NT1 box at the customer's location.

As specified by the T1E1.4 committee, the U-interface requires a single twisted-pair transmission medium. The interface standard provides for data transmission over

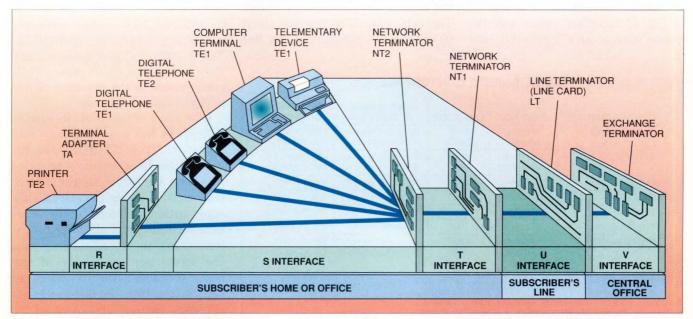


Fig 1—The ISDN consists of many different segments, which are called interfaces. To obtain maximum effectiveness at a particular interface, the ISDN terminators read a signal in one format and convert it to the proper format for the next step in the path.

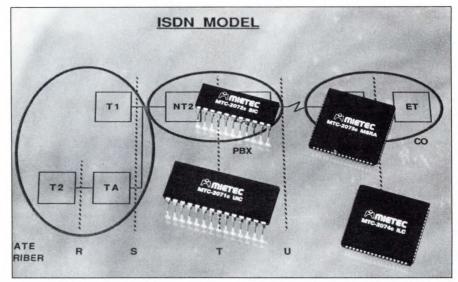
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5.5 km (18,000 ft) of 0.5-mm (24 AWG) cable. However, you can use ICs like Precision Monolithics' LIU-01 Serial Data Receiver (\$12 in 100piece quantities) to recover data over the U interface and act as repeaters for longer-distance transmission. The LIU-01 automatically adjusts for the signal attenuation and frequency distortion caused by long transmission lines. Another, more expensive, approach to longdistance transmission is to use Uinterface ICs in a back-to-back configuration as repeaters.

The digital subscriber line consists of the transceivers in the LT at the switch end of the U interface and those in the NT1 box at the subscriber's end of the interface. Full-duplex signals can be sent over the same pair of wires. The transceiver's job is to separate the signals traveling in both directions across the wires and to subtract the digital bit streams that it sends from the total bit stream, regardless of the corruption that might have occurred during the transmission of the signal. Corruption may result from bandwidth limitation, crosstalk, line echoing, or noise.

The U interface sends and receives data at an effective bit rate



The U-interface chip is only one piece of the ISDN puzzle. Each vendor supplies a number of other pieces, like this family of parts from Mietec.

of 160k bps: 144k bps for the 2B + Ddata, 4k bps for embedded-operation-channel (eoc) messages, and 12k bps for framing and maintenance functions. To correct for signal echoing at the terminations, the U interface uses echo cancellation.

The transceivers in the U interface use adaptive echo cancelers, equalizers, and line-code encoders and decoders to transport data over the copper arteries at high speed. The echo cancelers provide about 60 dB of echo cancellation. The line codes allow for the reduction of the transmitted data from two bits to one bit in 2B1Q and from four bits to three bits in 4B3T-but at the expense of some signal-to-noise bandwidth.

The MT8910 Quaternary Network Interface Circuit (QNIC) from Mitel uses the 2B1Q line code. An onboard Decision Feedback Equalizer (DFE) compensates for intersymbol interference (ISI) caused by bridged taps, gauge changes, and other impedance mismatches. The chip also includes nonlinear and jitter compensators to ensure high performance in the presence of imperfect implementations.

Like many of the ISDN IC suppliers, Mitel has a proprietary bus structure, the ST-BUS, for its ISDN ICs. Each vendor's proprietary bus conforms to the ISDN standards, but the standards only apply within an interface. To maximize flexibility and allow for future innovation, the specification treats the actual implementation of the boxes containing the interfaces as black boxes. Only the input and output data formats are specified by the CCITT and T1E1.4 committees. For example, any vendor's S inter-

TA	BI	F	1-	IS	D	N	U	-IN	IT	ER	FA	CE	ICs

COMPANY/PARTNER	PART NO.	LINE CODE	LINE LENGTH AT DIAMETER	PRICE AND QUANTITY
AMD/SIEMENS	Am2090 Am2091	4B3T 2B1Q	9.5 km AT 0.6 mm IN DEVELOPMENT	\$289 AT 100 \$121 AT 100
ATT/INTEL	T7262/T7263 T7260/T7261	2B1Q AMI	5.5 km AT 0.4 mm 5.5 km AT 0.4 mm	\$95 SAMPLES \$50 SAMPLES
INTEL/ATT	i89122/i89123	2B1Q	5.5 km AT 0.4 mm	\$130 AT 100
MIETEC	MTC2071	4B3T	8.2 km AT 0.8 mm	\$120 AT 1000
MITEL	MT8910	2B1Q	5.5 km AT 0.5 mm	\$61.10 AT 1000
PHILIPS/SIGNETICS	PCB2390	4B3T	8 km AT 0.6 mm	\$50 AT 1000
SIEMENS/AMD	PEB2090 PEB2091	4B3T 2B1Q	9.5 km AT 0.6 mm IN DEVELOPMENT	\$90 AT 1000 \$70 AT 1000

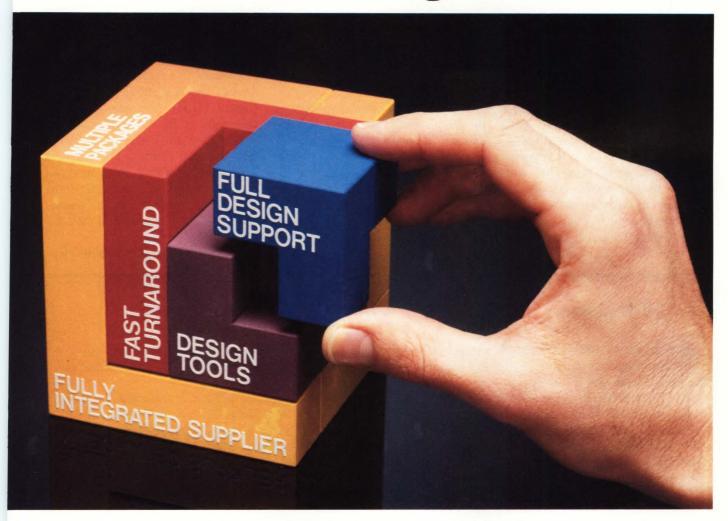
NOTES: ALL 2B1Q DEVICES PASS ALL BELLCORE LOOPS.

0.4 mm IS APPROXIMATELY EQUAL TO 26AWG. 0.5 mm IS APPROXIMATELY EQUAL TO 24AWG.

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face chip can talk to any other vendor's S interface chip. But if you're designing an NT1, you would want to use a single vendor's S- and U-interface chip set structured around that vendor's bus to simplify both the hardware and software designs.

Mitel's ST-BUS is a 2048k-bps bidirectional serial port that consists of 32 8-bit channels per 125-µsec frame. The frame pulse defines the frame boundaries, and the pulse repeats every 125 µsec. Each of the 32 channels is 3.9 µsec in length

with bit periods of 488 nsec. All data that the QNIC transmits across the U interface arrives via this bus.

You select the operating mode of the QNIC using three pins. You use one pin to put the chip into master or slave mode, another pin selects between single- and dual-port operation, and the third pin routes data through the Control/Data STBUS output in dual-port mode. Additionally, the QNIC has a provision for daisy chaining multiple devices

together, so you can utilize the 32-bit ST-BUS more efficiently.

Mietec's U-interface IC is a 4B3T device, the MTC-2071 U Interface Circuit (UIC). You can configure this chip in LT or NT mode, depending on which side of the interface the chip resides. Further, the architecture of the chip lets you time-multiplex as many as eight UICs in burst mode. In this mode, the chip multiplexes data in 32 1-bit wide time slots.

Perhaps due to the high develop-

An ISDN glossary

2B1Q LINE CODE—Line code in which two binary bits are converted into one quaternary bit for transmission across the U interface.

4B3T LINE CODE—Line code in which four binary bits are converted into three ternary bits for transmission across the U interface.

B CHANNEL—A switchable, optionally transparent, 64k-bps channel. Two B channels are included in the basic-rate service.

BASIC RATE—An ISDN access rate of 192k bps allocated as two B channels of 64k bps, one D channel of 16k bps, and 48k bps of overhead for framing and error detection.

CO—Central office. The telephone switching location nearest to the customer's premises.

D CHANNEL—A channel whose primary purpose is to convey signaling information between a terminal and the network switch but whose surplus capacity can be used for user-packet data and other data, such as telemetry. It operates at 16k bps for basicrate access and 64k bps for primary-rate access.

ISDN—Integrated Services Digital Network. ISDN supports both digitized-voice and data transmission. LT—Line Termination. A line card that provides termination of the subscriber loop at the PBX or central office.

NT1—Network Termination 1. A box that provides physical and electromagnetic termination of the 2-wire U-interface transmission line and conversion into the 4-wire S or T interface.

NT2—Network Termination 2. A box that provides switching and concentration of a subscriber's lines at the S interface.

PABX—Private automatic branch exchange. An automatic, private switchboard linked to the central office via a trunk line.

PRIMARY RATE—An ISDN access rate of either 1.544M bps—23 B channels and one D channel, which is the North American and Japanese standard—or 2.048M bps—30 B channels and one D channel, which is the European standard.

R INTERFACE—Connects a terminal adapter (TA) to nonISDN (TE2) equipment, often through an RS-232C port.

S INTERFACE—A reference point on the customer side of the NT2 to which you can connect either an ISDN terminal (TE1) or a TA; for example, the interface through which a digital telephone could connect to a PABX. This interface accommodates point-to-point and point-to-multipoint operation.

TA—Terminal Adapter. Connects nonISDN terminals (TE2) to the digital network via the S interface. The interface between the TA and the TE2 is the R interface.

TE1—Terminal equipment type 1. Standard ISDN terminal equipment that you can connect to the S or T interface.

TE2—Terminal equipment type 2. An analog or non-ISDN digital terminal.

T INTERFACE—Electrically identical to the S interface, the T interface has a different protocol than the S interface to link NT2 boxes to the NT1 box. U INTERFACE—A twisted-pair subscriber loop that provides basic-rate access to the NT1 reference point from the ISDN network. This interface only supports point-to-point operation.



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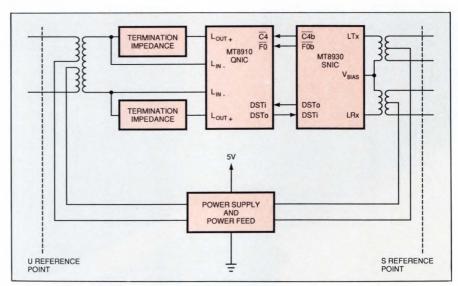
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ment costs associated with designing ISDN chips, many vendors have agreed to partnerships whereby they either split the engineering costs and agree to second-source each other's ICs or license chips in return for other considerations. Among the partnerships announced to date are those between Siemens and Advanced Micro Devices, Intel and AT&T, National Semiconductor and SGS-Thomson, and Philips and Signetics.

Siemens was one of the driving forces behind the Deutsche Bundespost's acceptance of the 4B3T line code. Needless to say, the company has a 4B3T U-interface chip, the PEB2090 ISDN Echo Cancellation Circuit (IEC). Siemens has organized the IEC to fit onto its ISDN-Oriented Modular (IOM) bus, which is similar to and compatible with the General Component Interface (GCI) bus. According to Dataquest, a market research firm in San Jose,



Due to proprietary bus structures, many ISDN chip families interface easily. Here, a Mitel 8910 acting in a slave mode terminates the subscriber line from the CO and extracts the clock from the data. The QNIC outputs a 4096k-bps bit clock and feeds an 8-kHz frame clock to the SNIC.

CA, the GCI bus has been adopted and is supported by such vendors as Siemens, AMD, National Semiconductor, SGS-Thomson, Plessey, Philips, and Signetics. Siemens is modifying its 2090 chip to transmit and receive 2B1Q line code; it's planning to name the new part the PEB2091.

A number of other 4B3T alterna-

For more information . . .

For more information on the ISDN U-interface ICs discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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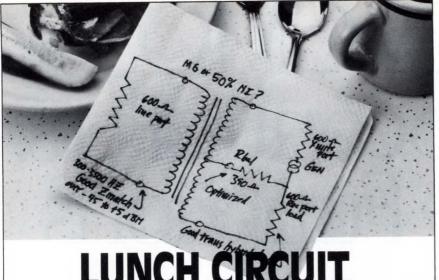
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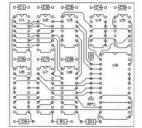
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tives are currently available, and the 2B1Q ICs will soon join the party. But be aware that the linecode disparity requires that you know where your design will operate and that you design flexibility into your product, so you can adjust the circuitry if the need arises. Additionally, although the U interface has been standardized, that standard is not yet etched in stone. You obviously don't want to have to redesign your NT1 or line card because you failed to properly analyze the market.

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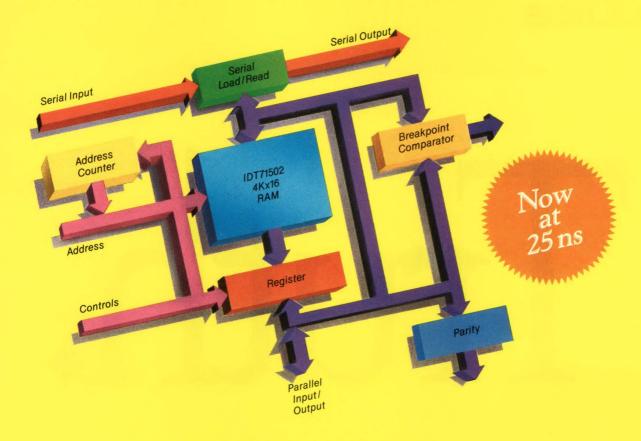
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Acknowledgment

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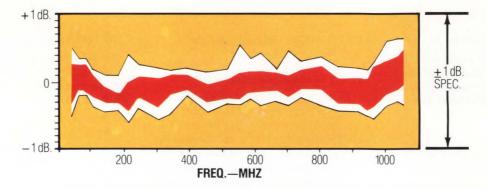
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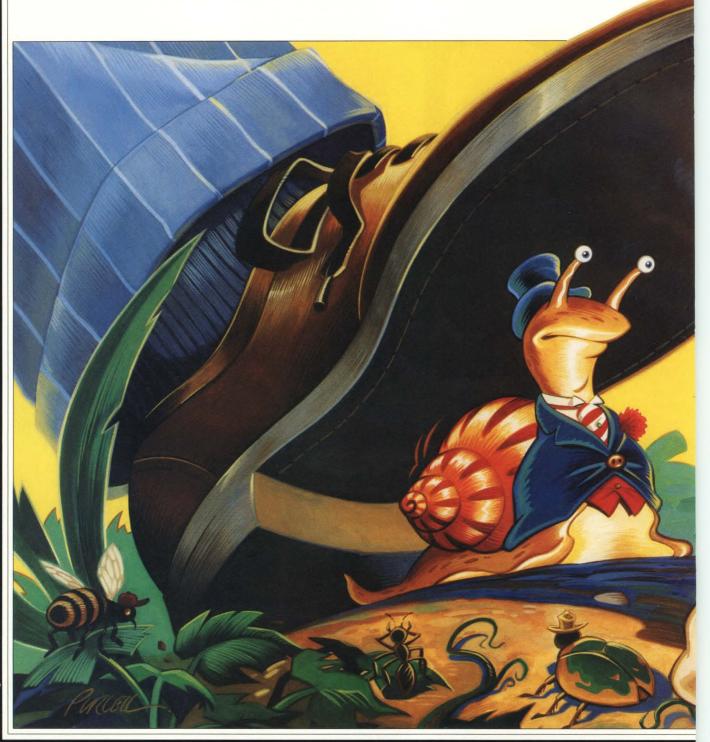
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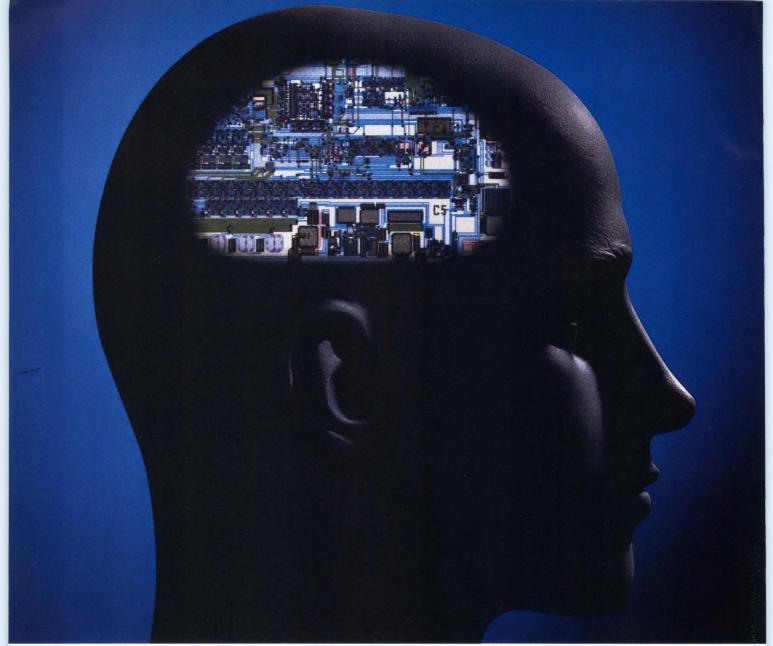
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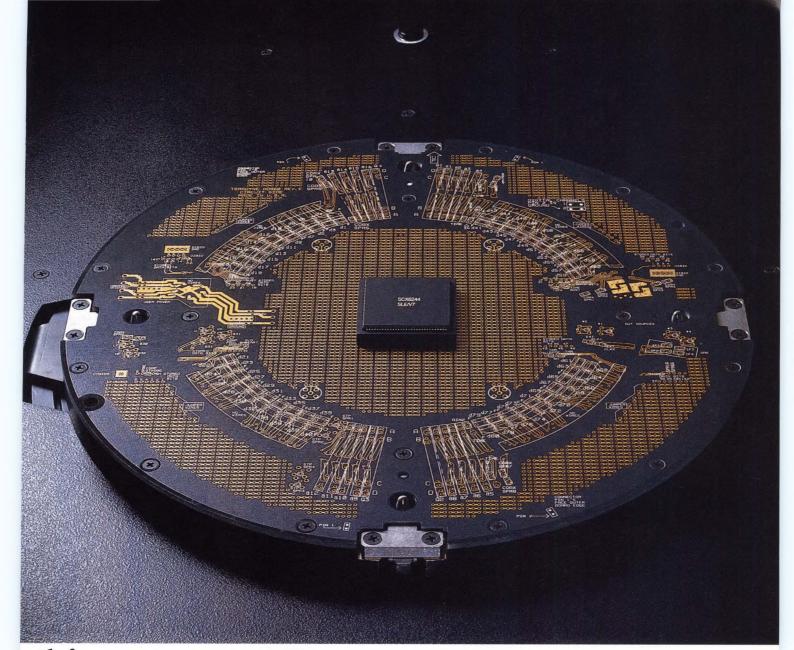
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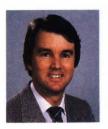
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10M-BPS TWISTED-PAIR ETHERNET

An Ethernet LAN standard emerges



The proposed IEEE-802.3 10BaseT standard will allow Ethernet LANs to transmit data over 99% of the installed telephone lines.

David Shear, Regional Editor

efore long, board and system designers may have to contend with designing local-area-network (LAN) interfaces based on the emerging IEEE-802.3 10BaseT standard, which will allow the transmission of data over standard phone lines at the full 10M-bps data rate. The standard is nearing ratification, and you may soon have to design a compatible LAN interface into almost any type of system you develop. Help is on the way. Many vendors are preparing 10BaseT-compatible transceiver chips, and some of the parts are already available.

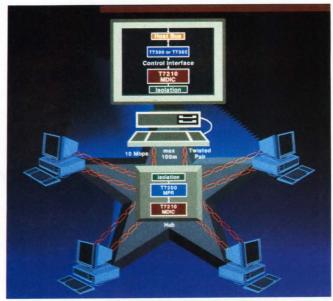
The maximum length of twisted-pair cable that the 10BaseT standard allows is 100m. Statistically, this length will allow you to use 10BaseT-compatible

equipment with 99% of the currently installed phone lines. This ability to use the phone lines instead of the expensive and cumbersome coaxial cables that the current 10M-bps Ethernet standard uses will increase the proliferation of Ethernet LANs. In some cases, a LAN interface will prove to be a better choice than either the RS-232C or the IEEE-488 type as a system's standard interface.

Ethernet is currently the most popular localarea network. Industry observers expect that Ethernet will remain the most popular LAN for the foreseeable future.

The IEEE-802.3 standard defines both the CSMA/CD and the physical layer. CSMA (carrier-sense multiple access) is the part of the standard that defines medium-access control. The CSMA standard uses a contention method that is probabilistic; in other words, it doesn't guarantee that any particular station will have access to the transmission medium. A station wishing to transmit must first listen to the channel. If the line is clear, it can send its message. Otherwise, it must wait for another opportunity to transmit.

Keep in mind that Ethernet in its present form may not meet your real-time needs, because it doesn't let you determine the worst-case data-transmission



The proposed 10BaseT standard will allow Ethernet systems to send data over 99% of the installed phone lines.



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10M-bps twisted-pair Ethernet

time. This situation can certainly be a problem for real-time applications. If you must be able to determine the worst-case response time in such an application, you may have to use other LANs.

The "CD" in CSMA/CD stands for collision detection. When two or more stations begin to transmit at the same time, they detect the message collision by seeing corrupted data on the bus. After detecting the collision, each station that is trying to transmit waits a random length of time and tries again.

Physical-layer options

IEEE-802.3 also defines the physical layer, or the medium over which the LAN transmits data (Fig 1). The original physical layer specified for Ethernet is 10Base5, which stands for 10M-bps baseband with a maximum segment distance of 500m. In this bus topology, each station connects to a transceiver module called a medium-attachment unit (MAU). The cable specified for 10Base5 is expensive and cumbersome.

To make Ethernet easier for end users to employ, the 10Base2 (Cheapernet) option was created. Cheapernet is also a bus topology, but it uses thinner, less-expensive coaxial cable. Its interconnections are inexpensive T connectors, and the MAU can be integrated into the station. 10Base2 provides for a maximum segment distance of 200m.

The 1Base5 (StarLAN) option was created to allow Ethernet systems to use existing phone lines. This option is a star topology that matches the way that telephones are wired into a building. The topology looks like that of any other busbased Ethernet LAN. 1Base5 LANs operate at only 1M bps, but their maximum distance between nodes is 500m.

Recognizing the need for a 10M-

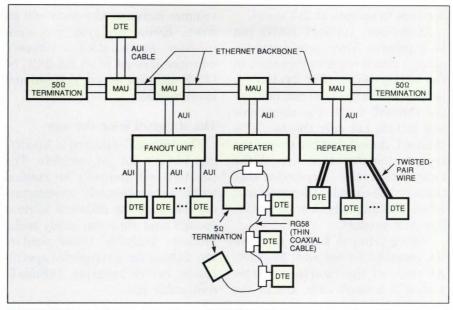


Fig 1—The IEEE-802.3 standard has many physical-layer options that you can mix and match to meet varying requirements.

bps twisted-pair Ethernet LAN that could operate at the same speed as the other physical-layer options, Synoptics, 3Com and other firms created a limited-distance version that could do just that. From these ideas came the standards effort for 10BaseT, or 10M-bps baseband on unshielded

twisted-pair lines (common telephone lines).

10BaseT LANs will be able to use existing phone lines to a maximum distance of 100m. Statistically, 99% of the installed phone lines fall within that limit. The limited distance will permit 10M-bps data rates, which will allow the entire

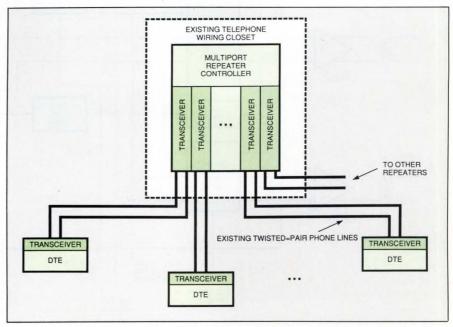


Fig 2—The 10BaseT standard uses a star topology that requires interface and control electronics at both ends of the twisted-pair cable.

10M-bps twisted-pair Ethernet

network to operate at full speed.

At present, 10BaseT LANs can be expensive. They have a star topology, which requires repeaters in the wiring closet (Fig 2); the repeaters add to the total cost of using the 10BaseT LAN. The user's cost will include not only the cost of a 10BaseT station, but the cost of the repeater on the other side of the twisted-pair cable. Remember that the user will consider the whole cost when deciding whether or not to buy your product.

10BaseT-based LANs do have the potential for low cost, however. As more of the interface is integrated in a single chip, and as the volumes increase, the costs will go down. Eventually, you may even consider incorporating a 10BaseT interface instead of an RS-232C or IEEE-488 type in your systems and instruments.

The standard is on the way

The 10BaseT standard is solidifying, but it's not yet complete. The standard will probably be ratified within a year. Some IC manufacturers feel that the standard is close enough that they can safely make products available. Other vendors are waiting for a completed specification before creating 10BaseT-compatible ICs.

One of the intrepid vendors to come out with a 10BaseT-compatible chip is NCR. The company offers the 92C02, a digital transceiver that uses external analog line drivers and receivers (Fig 3). The chip is intended for use with a LAN controller and a Manchester encoder/decoder. It includes digital preequalization, collision detection, SQE (signal-quality error) test, a jabber timer, and link-beat generation and detection for testing link integrity. The 92C02 costs \$15 (5000).

The 10BaseT standard specifies that transceiver chips use Manchester encoding, which makes it

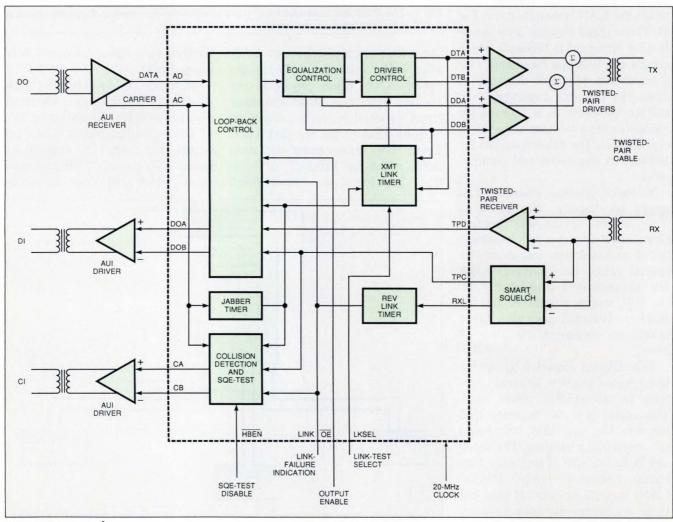


Fig 3—This digital transceiver interface, which uses the NCR 92C02 transceiver, contains all of the functions currently defined in the 10BaseT specification.

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possible to have a 5-MHz component in the signal. At other times the signal can be 10 MHz, depending on the data being sent. The signal's clock rate is 10 MHz. Manchester encoding allows you to send the data and the clock signal over the same wire.

Because the twisted-pair wire is similar to a lowpass filter, it has greater attenuation at 10 MHz than at 5 MHz. Therefore, the 5-MHz components of the signal must be attenuated prior to transmission so that they'll be at the same power level as the 10-MHz components when they reach the receiver.

To condition the signals prior to transmission, 10BaseT transceiver chips use pre-equalization or predistortion methods. This conditioning makes it easier to reconstruct signals correctly at the receiving end.

The 10BaseT transceiver chip implements the SQE test function after every transmission. This function tests the collision-detection circuitry. It must be disabled in applications in which the transceiver is used in a repeater.

Stop that runaway transmitter

A jabber timer monitors each transmitter and disables it if it continuously transmits for more than a preset amount of time. The link-integrity function uses a link-beat method. This method continually checks the integrity of the link between the station and the repeater. If no data is sent within a preset amount of time, a link pulse is sent along the twisted-pair wire. The interface at the other end of the twisted pair then responds. If the originator receives this response,

the integrity of the line is intact.

10BaseT transceiver chips also include a loop-back function, which makes 10BaseT equipment compatible with software written for other Ethernet physical layers. Some software expects to see the transmitted data come back through the receiver. When using a bus topology, you can easily see the data being transmitted, because your system is connected to the bus. A twisted-pair system isn't directly connected to a bus, however, so the interface must provide this loop-back feature.

The 92C02 is designed to use the Adapter Unit Interface (AUI), so you can incorporate the chip in an external Medium Attachment Unit (MAU). You can use this MAU to replace other 10M-bps MAUs when converting existing stations for use

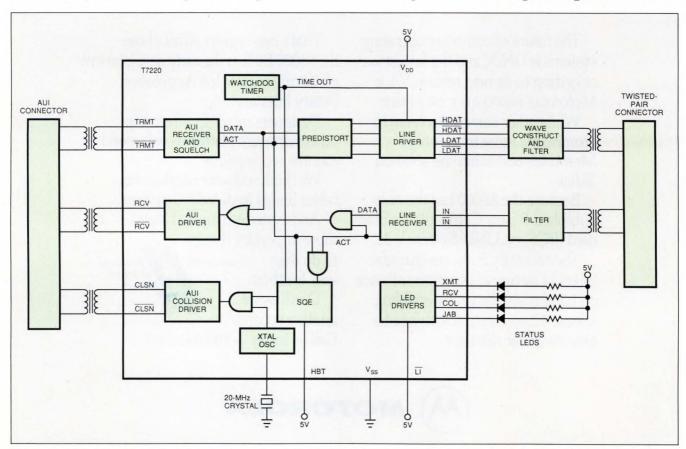


Fig 4—Because it has the AUI and twisted-pair line drivers and receivers on chip, the AT&T T7220 twisted-pair medium-attachment unit (MAU) provides a single-chip solution for replacing MAUs that are compatible with other versions of the Ethernet physical layer.

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with twisted-pair cable, or you can connect the 92C02 directly to the Manchester encoder/decoder and LAN controller when the system is not using an MAU.

The AT&T T7210 Manchester decoder and interface chip is based on a linear CMOS process. The T7210, which costs \$15 (10,000), includes predistortion control and a loopback function. It also has Manchester decoding, so it connects directly to a LAN controller. The LAN controller provides the Manchester-encoding function.

Currently, the T7210 doesn't include an SQE-test function, a jabber timer, or link-integrity functions. These functions were added to the specification after AT&T created the T7210. By the time the standard is completed, AT&T expects to offer a single-chip solution that includes the line drivers and receivers.

You can't easily use the T7210 to replace an MAU, because the chip lacks AUI signals and some other functions. The AT&T T7220 is designed to be a twisted-pair MAU (Fig 4). Like the NCR 92C02, the

T7220 includes pre-equalization, collision detection, an SQE-test function, a jabber timer, link-beat generation and detection, and a loop-back function. In addition, it includes line drivers and receivers for both the AUI and the twisted-pair cables, as well as four LED drivers for collision, transmit, receive, and jabber indicators. It sells for \$15 (10,000).

Intel has its own version of the T7210, thanks to an arrangement with AT&T. Intel and AT&T have signed a product- and technology-exchange agreement to develop LAN devices jointly. The Intel 82504TA is identical to the T7210 and costs \$30 (10,000).

Synoptics has had a VLSI transceiver available for some time; the product costs \$5.50 (10,000) plus a licensing fee. The transceiver is based on Lattisnet, the company's proprietary version of a 10M-bps twisted-pair Ethernet. Lattisnet is not compatible with the current version of 10BaseT. Furthermore, the part is available only via a licensing agreement.

Designing a 10BaseT interface

into your design is risky at present, because the standard is as yet unratified. It's quite possible that the standard could change enough to cause problems for anyone who designs with the 10BaseT information that's currently available.

Still, most IC manufacturers are claiming that they will have a 10BaseT-compatible product by the time the standard is completed. If you decide to design with one of these chips now, it's wise to put your Ethernet interface onto a plug-in board. That way, in the event that the standard requires major modifications, your redesign effort will be minimal.

In sum, LANs provide many advantages, such as increased communication within an organization, the common use of databases to make information widely available, and the sharing of resources throughout an organization. And they're rapidly becoming even more popular. You'd be wise to keep an eye on Ethernet LAN technology, therefore: Before long, you'll very likely be asked to design a LAN interface into your system. LANs are here to stay.

For more information . . .

For more information on the 10BaseT interface chips discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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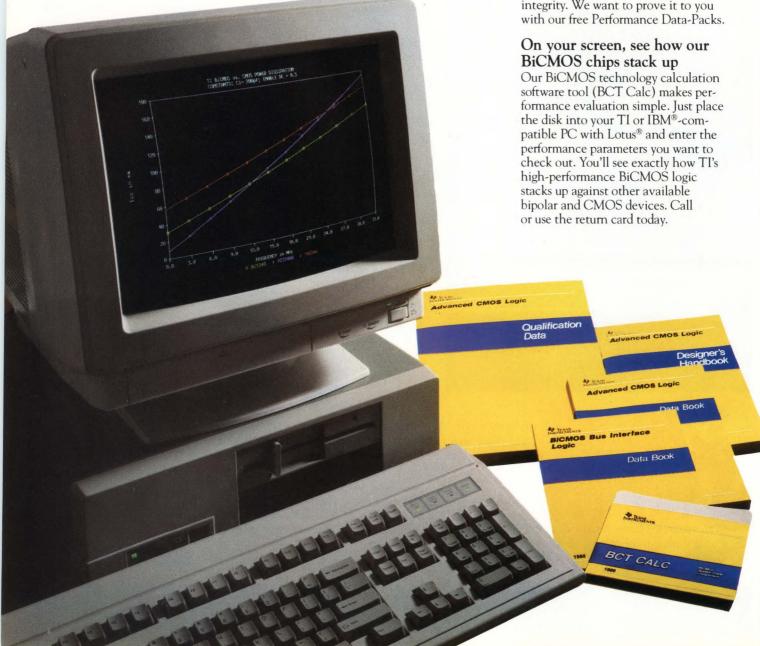
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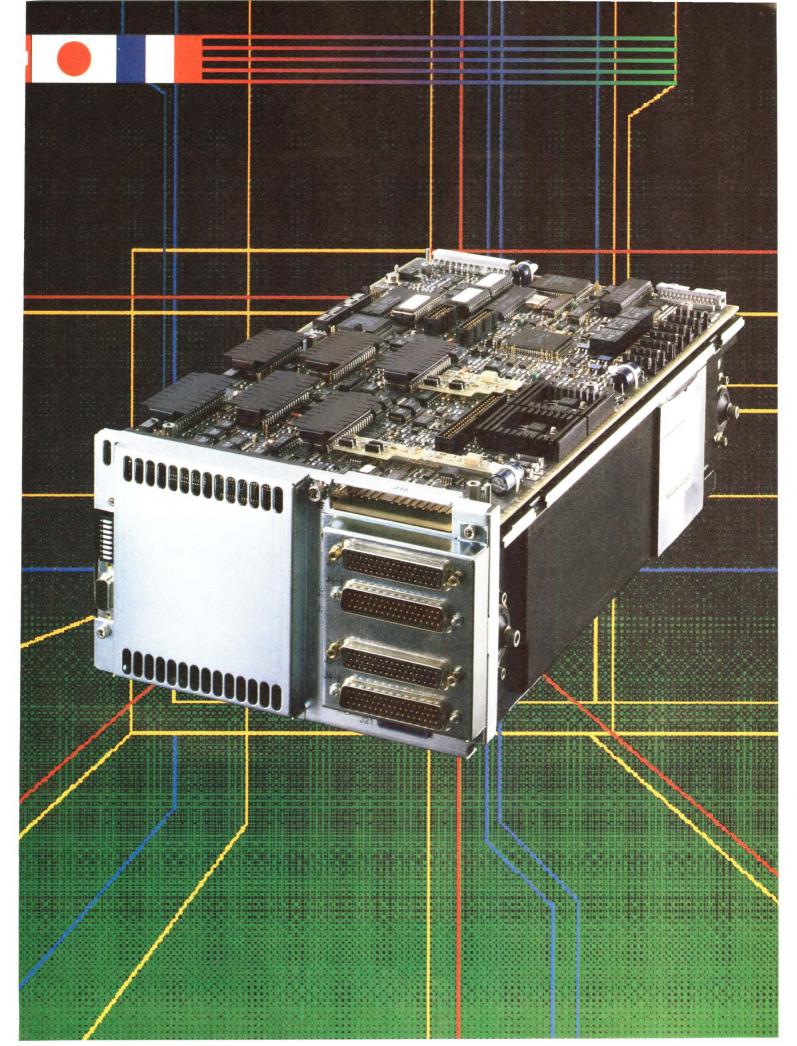
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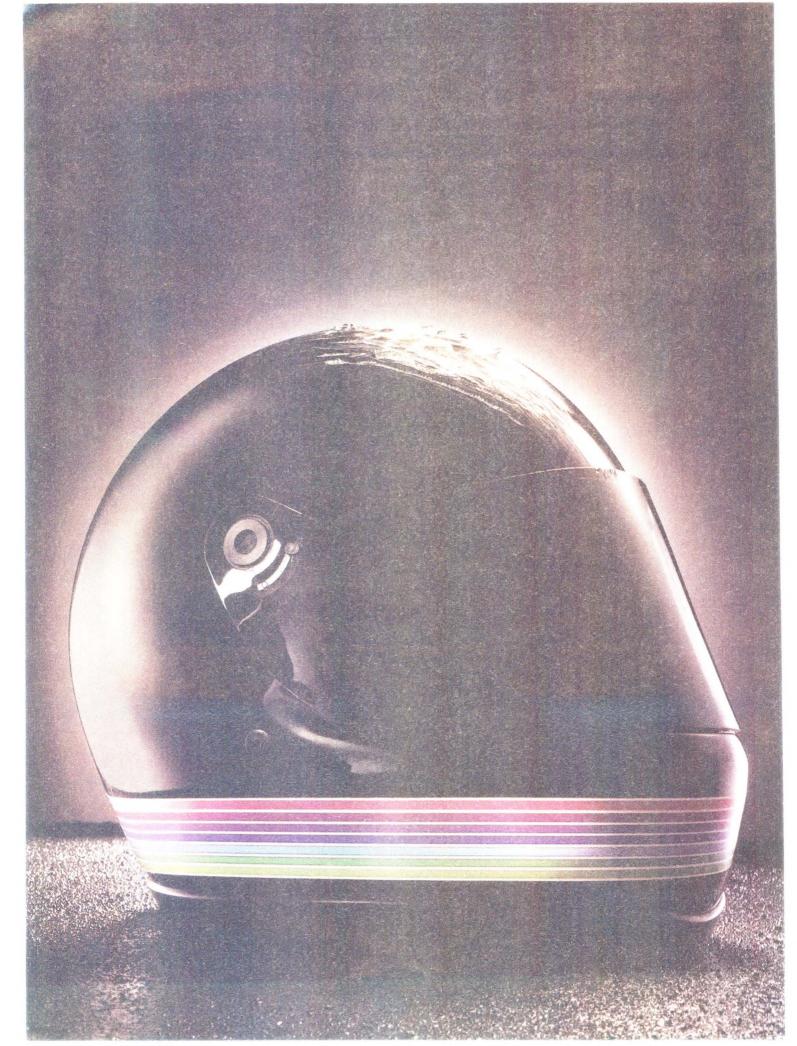


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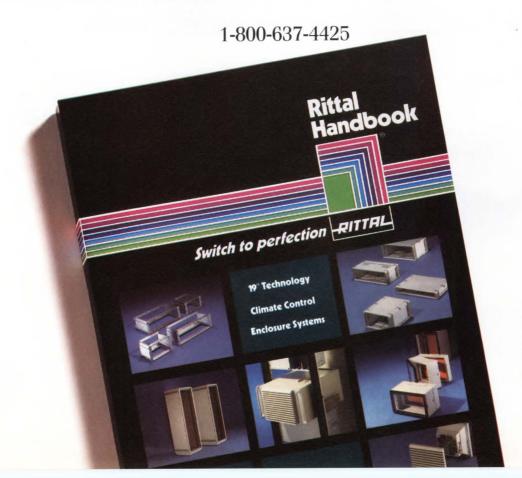
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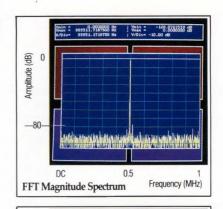
One company offers 1,2,5,&10MHz 12-bit sampling A/D converters. DATEL.

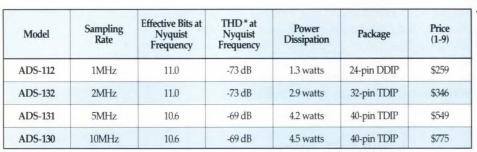
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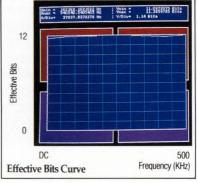
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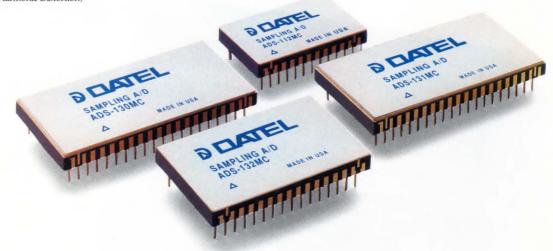
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Attenuators solve transmission problems



Digitally programmable attenuators let you automatically control signal amplitudes without introducing any impedance or phase distortion.

> Tom Ormond, Senior Editor

igitally programmable attenuators are useful for almost any application in which you need to control signal-amplitude levels. You can, for example, use them in application that involve radar signals, telecommunications networks, automatic test equipment, video attenuation, amplifier gain control, variable burst generation, logarithmic D/A conversion, and frequency synthesis. You can also use attenuators to extend the range of power meters, prevent burnout or overloading problems in sensitive equipment, and set standards for loss measurements. Today's programmable attenuators suit not only a variety of applications, but a wide range of frequencies as well: the selection of available programmable attenuators lets you accommodate frequencies from the kilohertz to the gigahertz range.

To understand how programmable attenuators can help you solve transmission problems and control signal amplitudes easily, consider the role that they play in a telecommunication system. In a typical telephone network, each link between a subscriber's home and the central office constitutes a local loop. The receiving equipment at the central office must interface with thousands of transmitter signals. These signals are sent over links that have widely varying lengths and loss characteristics. If the receiving equipment is calibrated to interface with the most remote transmitter in the system, the transmitters from closer sources overload the receivers.

To prevent this overload condition, you could use unique transmitters, which are designed to meet the minimum receiver requirements when they operate in a particular local loop. Although this scheme will work, it isn't a very viable solution from an economic standpoint. Using a digitally programmable attenuator at the receiving end of each local loop, however, is a less expensive and more effective solution. As each loop comes on line, the installers at the central office can adjust the attenuator to ensure that the incoming transmissions are well within the established limits of the receiving equipment.



Operating over dc to 1 GHz, the MDA Series attenuators from Alan Industries feature total attenuation specs ranging from 15 to 127 dB, a switching time of 6 msec, and a switch life of 10^7 operations per bit.



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Programmable attenuators

This system not only prevents signal-saturation problems, but also eliminates the need for custom receivers and transmitters.

Are you there, Watson?

Sierra's SC11310 programmable gain/loss circuit is just one of the attenuators that you can use to increase the efficiency of a telecommunication system. This device is designed to provide precise interface levels in telecommunication equipment and voice-line circuits. It is also well suited to diagnostic applications involving loopback control circuits. In this case, the SC11310 is usually located in front of the codec on the line card, which is in the central office.

The SC11310 features a 0.05-dB gain/loss error, -60-dB total harmonic distortion, 40-mW power dissipation, and a 10-dBrnCo idlechannel noise level ("dBrnCo" refers to decibels above reference noise, C-message weighted). The device works from supply levels of $\pm 5\mathrm{V}$ and has large- and small-signal bandwidths of 200 kHz and 1.5 MHz, respectively. The SC11310, which sells for \$4.92 (100), is housed in a 20-pin DIP.

Processed in low-power CMOS technology, the SC11310 consists of latch circuitry, control logic, and a gain/loss network that includes a string of four op amps that are connected in series. You control the circuit's operation by using 10 inputs: the G₀ through G₇ inputs, the Si/GL input, and the mode pin. The G_0 through G₇ inputs generate an 8-bit word that controls the magnitude of the gain/loss setting in 0.1-dB steps. The Si/GL input selects either the amplification or the attenuation, and the mode pin establishes one of two control modes.

When the mode pin is high, the circuit has 511 distinct setting steps, and the gain varies from -25.5 to +25.5 dB. The Si/GL pin



To accommodate high frequency and power needs, Daico Industries offers a line of 7-bit attenuators that operate over the 30- to 500-MHz range and accept input power levels of 13 dBm. They operate from a 5V supply.

selects the gain/loss function to provide a total dynamic range of 51 dB. When the mode pin is low, the SC11310 has 481 distinct setting steps, and the gain varies from -24 to +24 dB, resulting in a total dynamic range of 48 dB.

The PST (parallel/serial/through) pin lets you operate the SC11310 in one of three ways. If you apply 5V to the PST pin, you can control the chip over the parallel bus. The circuit will have gain when the Si/GL pin is at 5V, and it will have loss when the Si/GL pin is at -5V. The WR writes the data into the chip. Data latches into the SC11310 on the rising edge of WR, and the new gain/loss value is effective immediately.

If the PST pin receives 0V, you can interface the SC11310 through the serial port—the Si/GL pin in this case. The SC pin serves as the shift clock, and $\overline{\rm WR}$ acts as the enable clock. After nine SC pulses, data latches into the chip on the rising edge of $\overline{\rm WR}$, and the gain/loss status becomes effective. At the same time, the internal register holds the previous gain/loss value during the serial shift to prevent the output from making any unpredictable changes.

If the PST pin receives -5V, the SC11310 interface operates in the "through" mode. In this mode, the attenuator's internal circuitry ignores \overline{WR} and SC, and the data that you place on the parallel bus (using switches) is effective at all times. The through mode is essentially designed for applications that don't require a microcontroller.

Step up the frequency

Keep in mind that all IC-type attenuators aren't restricted to voice-frequency applications. Many of these devices, such as Topaz Semiconductor's CDG4460 and CDG4469, accept frequencies from 5 to 40 MHz.

The CDG4460 is a 6-bit, 40-MHz attenuator that is designed for video applications. It will attenuate signals over a 0 to 15.75-dB range in 0.25-dB increments. When operating in a 75Ω system, the unit maintains constant input and output impedance over the entire attenuation range. The onboard data latch lets you use predetermined attenuation settings or recall attenuation settings from memory. Housed in a 16-pin hybrid package, which occupies 1 in.² of board space, the CDG4460 operates from ± 6 to

Programmable attenuators

 ± 15 V supplies and dissipates 0.5 μ W typ.

The CDG4469, on the other hand, is an 8-bit attenuator that is designed for applications that require a wide range of attenuator settings. Featuring a usuable frequency range of 5 MHz, the unit attenuates signals over the 0 to 127.5-dB range in 0.5-dB steps. The attenuator can accommodate analog input voltages as high as 6V rms, and it has a constant input impedance of 650 Ω . The CSG4469 is housed in a 16-pin hybrid package. It operates from ± 6 to ± 15 V supplies and dissipates 0.5 μ W max.

Both of these digitally controlled attenuators are designed and fabricated with a combination of CMOS/

DMOS ("DMOS" is double-diffused MOS) integrated-circuit and hybrid technologies. The CMOS/DMOS portions consist of the CMOS input logic and the level translators that drive the DMOS FET switches. The attenuator ladder is made of thick-film resistors that are deposited on a ceramic substrate.

The attenuators' control logic accepts CMOS logic levels and provides internal level translation for the DMOS FET gates, which are tied to either the positive or the negative supply rail. The complementary logic controls the FET switches in pairs. The resistor attenuator ladder is designed to ensure that the series FETs and the thick-film resistors provide the ma-

jority of the attenuator level settings. The shunt FETs and the remaining thick-film resistors combine to maintain a constant attenuator input impedance. In addition, both devices contain diodes to protect the inputs against damage from high static voltages or electrical fields. The CDG4460 and the CDG4469 cost \$28.21 and \$23.50 (100), respectively.

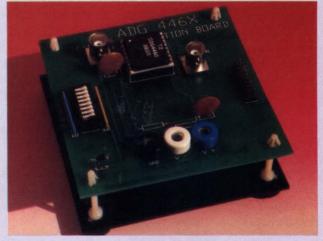
Attenuators that are based on IC technology work well in applications that involve frequencies ranging to tens of megahertz. However, you can also use attenuators for applications that demand even higher frequencies. Although the devices in this high-frequency category employ different fabrication tech-

Evaluation boards ease testing procedures

Evaluation boards are a vital factor in the acceptance of new ICs, because they provide designers with a complete, ready-to-use test system. Most semiconductor vendors acknowledge this fact, but few have the resources and/or the commitment to offer evaluation boards. EDI Corp tries to fill this void; the vendor's ADG446X-1 board lets you assess the attenuation performance of CDG4460 and CDG4469 programmable attenuators from Topaz Semiconductor before you incorporate the devices into your system.

When you test the 6-bit CDG4460, the board uses pin 5 for the latch-enable signal and pin 13 for the latch-reset signal. The board uses these two pins for attenuation control when you test the 8-bit CDG4469. You can use either onboard DIP switches or external logic to control all the attenuator pins, as well as the latch enable and the latch reset. The external logic accesses the board via a cable that's connected in parallel with the DIP switches through a double-row header connector. The header has only ground pins on the outer row to facilitate the cable-termination process.

The board's pullup resistors connect to a 5V supply that's generated by an onboard 3-terminal regulator; they guarantee that the DIP switches' Off position designates logic high. All the board's switches connect to ground through high-value pull-

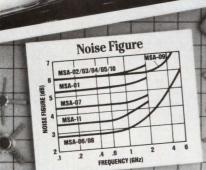


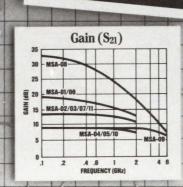
To facilitate the testing process, the ADG446X-1 evaluation board from EDI Corp lets you excercise the 6- and 8-bit attenuators from Topaz Semiconductor. The board can serve as a test fixture or a ready-made development vehicle for a variety of applications.

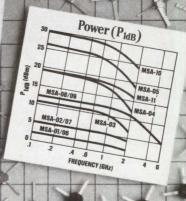
down resistors. This arrangement lets you safely transfer test-signal control to external circuits that automatically override the DIP-switch settings.

The board's power-input sockets are labeled V⁺ and V⁻. You can use the attenuators by applying ± 6 to ± 15 V to these pins. The ADG446X-1 is priced at \$105 and comes with one attenuator, data sheets for the board, and application literature.

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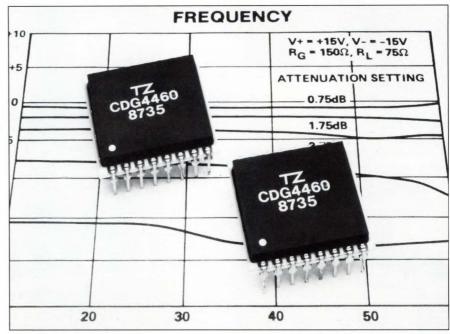
Programmable attenuators

niques, their performance levels are just as impressive as the IC-type attenuators' performance.

Daico Industries, for example, provides three attenuators that operate in the RF range; the 7-bit step attenuators operate over the 30- to 500-MHz range. The attenuators are available in 38-pin DIPs and in packages that include integral SMA-type connectors. They accept 13-dBm input power levels and operate over the full military temperature range $(-55 \text{ to } + 125^{\circ}\text{C})$.

Each of the seven control inputs includes a CMOS or a TTL driver. These drivers control the parallel PIN-diode switches, which activate or deactivate the resistor pads that make up the attenuation chain.

The CMOS-compatible DAO285 and the TTL-compatible DAO295 are low-power attenuators that feature a 63.5-dB total attenuation range, which you can select in 0.5-dB steps. Operating from 5V dc, the devices draw 30 and 50 mA, respectively. Their typical insertion loss is less than 6 dB, and their maximum VSWR is 1.35:1. Both models have a maximum switching speed of 5 µsec and an RF transient time of 3 µsec. Their attenuation accuracy varies with different settings; at a 0.5-dB attenuation setting, the



Suitable for portable applications, the 6-bit attenuator from Topaz Semiconductor consumes 0.5 μ A of current from supplies that can provide from ± 6 to ± 15 V. The CDG4460 features a total attenuation of 16 dB in 0.5-dB increments and operates over dc to 40 MHz.

attenuators' accuracy is 0.125 dB. At all other attenuation settings, their accuracy is $0.15 \, dB \pm 2\%$ of the attenuation setting.

The third model in the series, the DAO617, is designed for high-speed applications. Over the frequency range of 45 to 250 MHz, the unit provides 0 to 63.5-dB attenuation in 0.5-dB increments. The high-speed TTL drivers enable the

DAO617 to achieve a 7-nsec transition time and a 25-nsec total switching time.

The DAO617 has a second intercept point of 82 dBm and a third intercept point of 34 dBm. It also has a 50-mV transient voltage level and an 8-dB maximum insertion loss. Its VSWR measures 1.35:1 max. One drawback of this device, however, is that you trade power consumption for high speed; operating from a 5V supply, the 617 draws 640 mA. The DAO617 costs \$555; the DAO285 and the DAO295 are priced at \$511 (100).

Like Daico's high-frequency attenuators, the MDA Series of programmable attenuators from Alan Industries employ PIN-diode switches to activate or deactivate the π-type resistor pads in the attenuation network. This line of attenuators, however, is designed for ATE (automatic test equipment) applications and operates over dc to 1 GHz. The attenuators include one EMI/RFI filter for each control bit and a common filter for the

For more information . . .

For more information on the programmable attenuators discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Alan Industries Inc Box 1203 Columbus, IN 47202 (812) 372-8869 FAX 812-372-5909 Circle No 708

Daico Industries Inc 2351 E Del Amo Blvd Compton, CA 90220 (213) 631-1143 TWX 910-346-6741 Circle No 709 EDI Corp Box 366 Patterson, CA 95363 (209) 892-3270 Circle No 710

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UPDATE

Programmable attenuators

ground or negative rail.

The Series consists of four models that feature attenuation specs of 15 (Model 50MDA15), 31.5 (Model 50MDA31.5), 63 (Model 50MDA63), and 127 dB (Model 50MDA127). The 4-bit 50MDA15, the 6-bit 50MDA63, and the 8-bit 50MDA127 all feature 1-dB attenuation increments; the 6-bit 50MDA31.5 attenuates signals in 0.5-dB increments. At 500 MHz, the parts' attenuation accuracy is $\pm 0.5 \, dB \, (\pm 1 \, dB \, for \, the$ 50MDA127 when the attenuation level is above 32 dB). At 1 GHz, the accuracy is ± 0.75 dB for the 50MDA15 and 50MDA31.5, ±1 dB for the 50MDA63, and ± 0.7 dB for the 50MDA127 (± 1.5 dB for the 50MDA127 when the attenuation level is above 32 dB).

The units' maximum insertion loss ranges from 2 to 3 dB, and their switching speed is 6 msec max. The maximum VSWR for all four attenuators is 1.3:1 at 500 MHz and 1.4:1 at 1 GHz. The PIN-diode switches are rated for 10⁷ operations per bit. Their on- and off-level control signals are 17 to 26.5V dc and 0 to 5V dc, respectively. The RF connectors are available in SMA, SMB, and SMC styles. The prices for MDA Series attenuators range from \$220 to \$410.

Article Interest Quotient (Circle One) High 515 Medium 516 Low 517 Quick.

Name the three requirements for highest performance system design.



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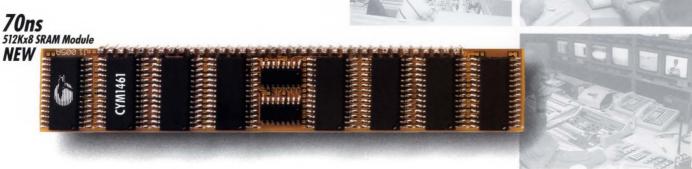
Tektronix also specifies our high speed, low power PROMs and SRAMs, to speed digital information through the system at broadcast video rates.

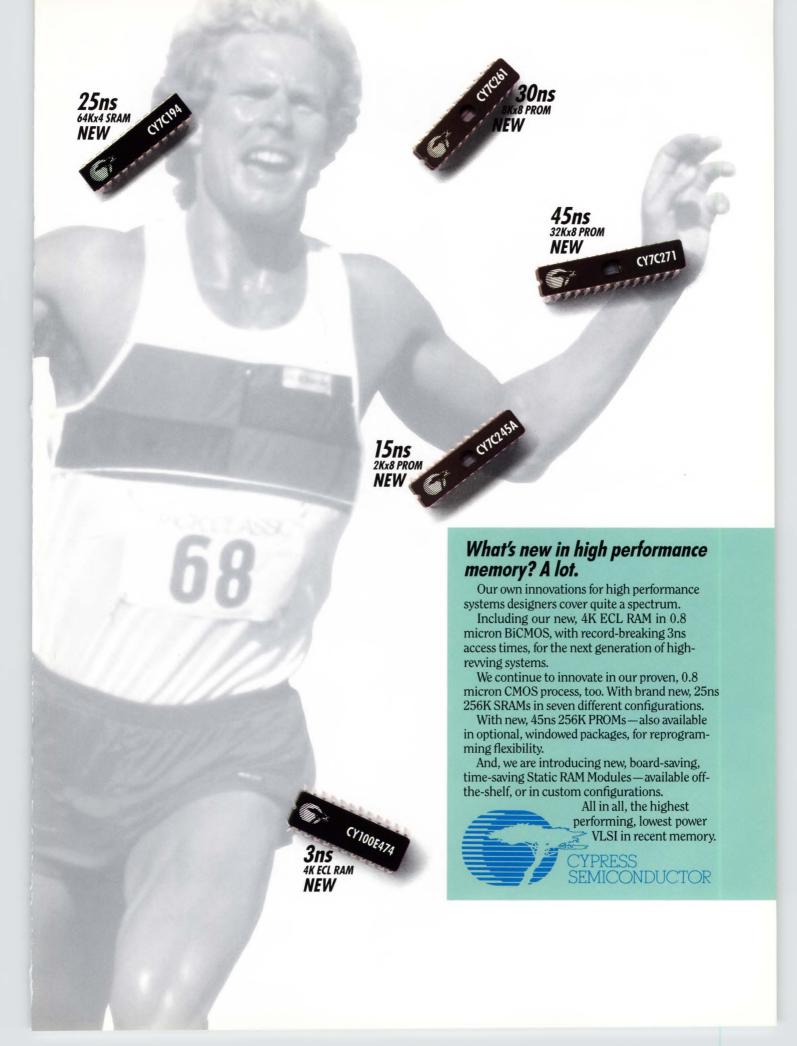
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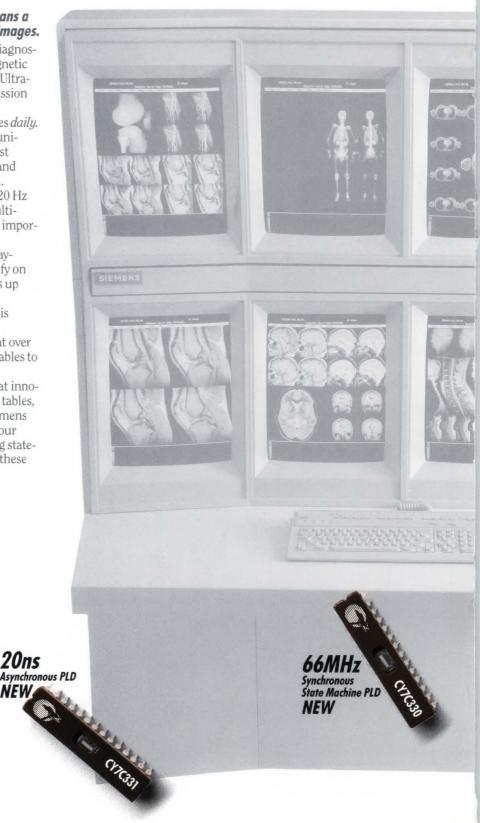
Whatever they need to perform diagnosis rapidly and accurately.

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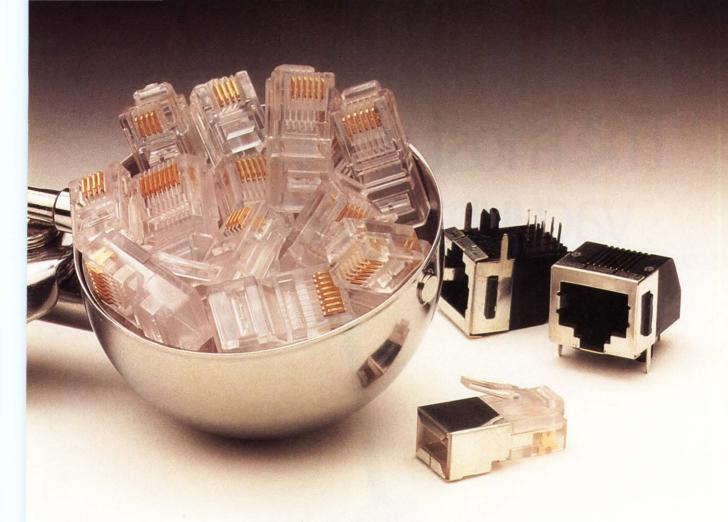


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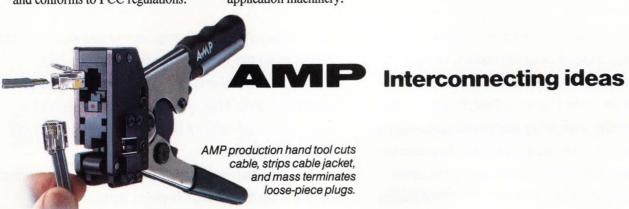


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EDN April 27, 1989

CIRCLE NO 58

111

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GRAPHIC DISPLAYS/MODULES

Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1013A	GP1013A02	64X34	200	3.35X2.95X0.7
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1018A	GP1018A01	400X240	40	7.10X6.30X1.61
GP1004C	GP1004C03	640X400	30	9.65X7.3X1.85
GP1019A	GP1019A03	640X400	35	7.10X6.70X2.56

*Different Versions Available

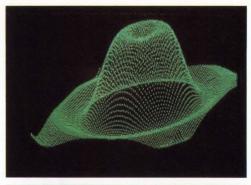
DOT MATRIX/CHARACTER DISPLAY MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
16LD03G	M16LD03B	16X1	5X7	0.433	8.90X1.95X.98
16SY03Z	M16SY03B	16X1	14 SEGMENT ALPHANUMERIC	0.200	4.92X1.32X.83
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90
MANY OTHER	NEW MODULES				

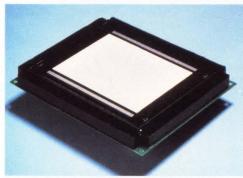


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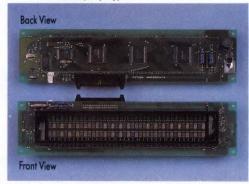


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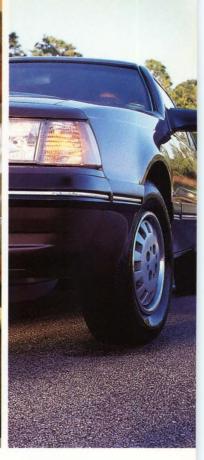
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DISPLAYS









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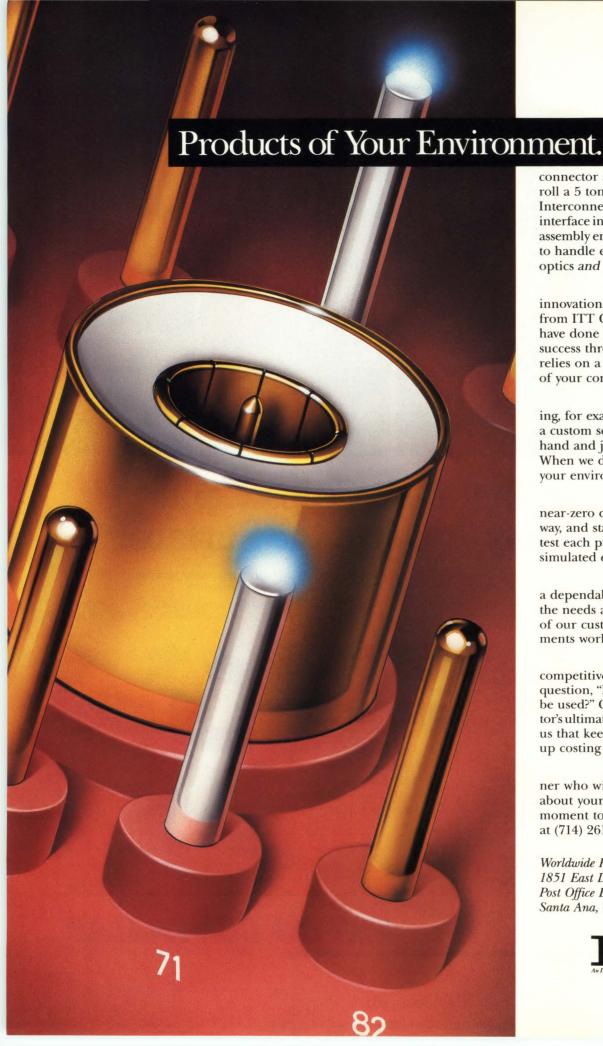
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CIRCLE NO 62

Micropower op amps hit new lows



The latest micropower op amps not only draw less current than their predecessors, they also operate from lower voltages.

> **Peter Harold,** European Editor

ou no longer need to sacrifice dc performance for low power consumption when you design with micropower op amps. These devices are now available with input offset voltages as low as 5 µV and input offset drifts of 0.05 μV/°C, and micropower op amps with 1-μV input offset voltages are already on the horizon. However, some performance tradeoffs, such as speed versus power, still remain. Table 1 (see pg 124) details the basic specifications of a range of op amps that have a maximum quiescent supply-current rating of 500 µA or less at 25°C.

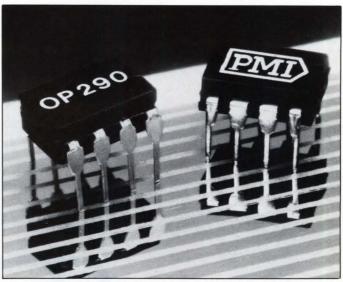
Op-amp manufacturers finally got the message that you don't always want to run micropower devices from $\pm 15 \mathrm{V}$ supply rails. You can now get guaranteed performance at low supply voltages. Low-voltage supplies are not only

desirable to save power consumption; but more often than not, they are all that's available in battery- or solar-powered equipment. In addition, low-voltage operation lets you power op amps from the same supply as logic circuitry. As a result, many manufacturers now provide full specifications for their devices at these low supply voltages—typically $\pm 2.5V$ but sometimes as low as ±1.5V. Thus, you can design them in with confidence.

Micropower op amps

are also increasingly specified for singlesupply operation instead of or in addition to split-supply operation. When you operate a conventional split-supply op amp from a single supply, you may be faced with having to generate an artificial ground that's midway between the supply's ground and positive rails. This step is usually necessary to ensure that the op amp stays within its commonmode input-voltage limitations. However, op amps that are specified for single-supply operation have a commonmode input-voltage capability that includes ground. These op amps can handle input signals that swing right down to ground potential.

Check carefully to ascertain whether the op amp's output has a similar capability. If the device won't drive its opencircuit output to ground, you'll have to add a power-consuming pull-down resis-



The OP290 precision, dual, micropower op amp from PMI is fully specified for supply voltages in the 1.5 to 15V and -1.5 to -15V ranges.

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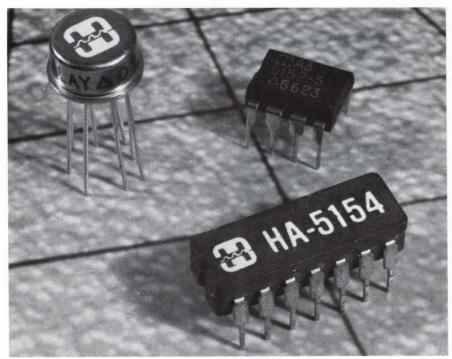
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TECHNOLOGY UPDATE

Micropower op amps



The HA5154 is a quad micropower op amp from Harris that achieves a $6V/\mu$ sec slew rate and a full-power bandwidth of 95 kHz.

tor to achieve a 0V output.

Ideally, the greater the commonmode input- and output-voltage ranges of the op amp, the greater the dynamic range you'll be able to use for your analog signals. When you're operating on supply voltages of 5V or less, maintaining dynamic range through several op-amp stages can be essential to ensure that your signal doesn't get lost in the noise. Advanced Linear Devices claims to be the first company to provide low-voltage, low-power op amps with common-mode input- and output-voltage ranges that include both supply-rail voltages. In the future, you'll see an increasing number of op amps with this rail-to-rail input and output capability.

Low Vos maintains precision

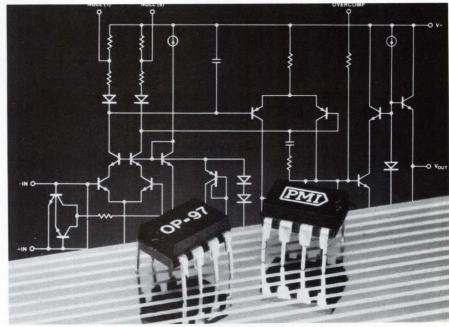
In the past, low power consumption and precision dc performance didn't go hand in hand. That situation is rapidly changing. Micropower op amps with maximum in-

put offsets of 1 mV are now commonplace, and several devices have maximum input offset-voltage specifications of 100 μV or less. But

the best input offset-voltage specifications—5 μV maximum at 25°C—are currently achieved by chopperstabilized devices. These devices include Maxim's MAX-422, MAX-423, and MAX-432, and Teledyne Semiconductor's TSC900 micropower op amps.

Maxim will add another lowpower precision op amp to its offerings later this year. Designated the MAX425 Superamp, it will employ two active error-correction schemes to keep all sources of input offsetvoltage error to less than 1 µV at 25°C. The device's input offsetvoltage drift will be a mere 0.05 μV/ °C over the full military temperature range. The input bias current will be 1 pA max at 25°C, rising to 100 pA max at 85°C. The powersupply current, however, will be as large as 1.2 mA for supply voltages in the 2.5 to 7.5V and -2.5 to -7.5V ranges. The lowest grade version of the MAX425 Superamp is expected to sell for around \$5 (100).

Although it's not included in the



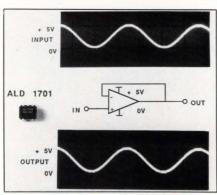
The OP97 precision op amp from PMI consumes 1/sth the power and 1/soth the input bias current of the company's OP07 device yet has the same dc performance.

TECHNOLOGY UPDATE

Micropower op amps

table because of its maximum supply-current specification of 600 µA, PMI's OP97 is a precision op amp that's close on the heels of currently available chopper-stabilized micropower devices. The device has a maximum input offset voltage of 25 μV at 25°C and an offset-voltage drift of 0.6 µV/°C. And because it doesn't employ chopper techniques to achieve these specifications, the OP97 won't introduce the clockrelated ripple and noise that often appears on the input and output of chopper-stabilized op amps. This factor is of particular significance if your design requires wide-band frequency response. The OP97 costs \$1.60 (100).

Another company attacking the market for precision micropower op amps is Raytheon. Later this year, the company's semiconductor division is set to introduce the RC4097,



Offering rail-to-rail common-mode inputand output-voltage ranges, the ALD1701 CMOS micropower op amp from Advanced Linear Devices suits low-voltage, singlesupply applications.

a micropower op amp with a maximum input offset voltage of 15 μ V and an input offset-voltage drift of 0.3 μ V/°C. The device's provisional data sheet also specifies a maximum input bias current of ± 100 pA at 25°C. The input bias current in-

creases to a maximum of ± 250 pA over the commercial temperature range and ± 600 pA over the military temperature range. Prices for the RC4097 are expected to start at around \$2.75 (100).

Some micropower op amps have extremely good input bias-current and input offset-current specifications. Analog Devices' best grades of the AD-548 and the AD-648, for example, have maximum bias currents and input offset currents of 10 pA and 5 pA, respectively, at 25°C. As a result, you can drive the inputs from high-impedance sources without incurring excessive dc errors. The AD-548 and the AD-648 cost \$0.75 and \$1.25 (100), respectively.

However, before choosing a micropower op amp for its bias current and input offset-current specifications, carefully check how these pa-

For more information . . .

For more information on the micropower op amps described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Advanced Linear Devices Inc 1180F Miraloma Way Sunnyvale, CA 94086 (408) 720-8737 FAX 408-720-8297 Circle No 661

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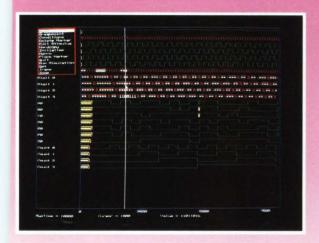
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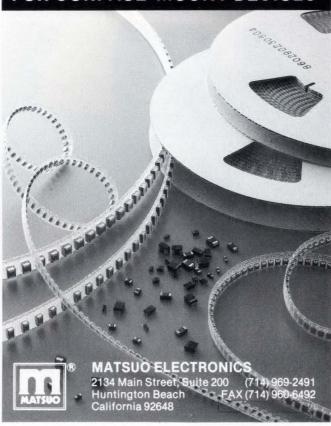
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UPDATE

Micropower op amps

rameters vary over the device's operating temperature range. The bias current of most FET-input op amps tends to double for every 10°C rise in temperature. Although bipolar-input op amps tend to have higher bias currents to begin with, their bias current varies with temperature at a much lower rate. For example, a bipolar-input op amp with a 25°C bias-current specification of 5 nA will exhibit a typical bias-current variation of only 1 or 2 nA over its entire operating temperature range.

Speed/power tradeoffs remain

Unfortunately, like all op amps, micropower op amps suffer from an inevitable speed-vs-power tradeoff. Even devices at the 500-µA limit for inclusion in the table don't have unity gain × bandwidths greater than 2 MHz. Although PMI's OP421 has a typical unity gain × bandwidth of 1.9 MHz, that figure only applies for supply voltages of ± 15 V. The device meets the 500-µA limit only if you operate it on ± 2.5 V supplies. At these supply voltages, its gain × bandwidth falls to around 1.6 MHz. The OP421 sells for \$1.80 (100).

Micropower op amps with a maximum supply current of 250 µA typically achieve unity gain × bandwidths of around 1 MHz. If you require very low power consumption and have to use op amps that draw only a few tens of microamperes from low-voltage supplies, you'll have to put up with unity gain × bandwidths of 100 kHz or less.

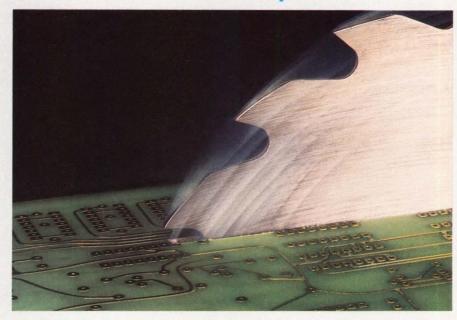
Article Interest Quotient (Circle One) High 518 Medium 519 Low 520

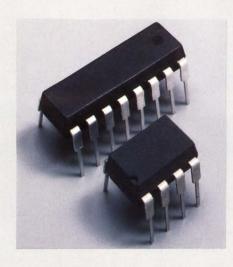
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CTR (%)	Industry Standard Single Channel	Dual Channel	Quad Channel	
Type: Phototrans	istor			
20 (Min) 10 50 100 40,63,100 & 160 50,20 & 100 (1)	4N25/4N26/IL1/HIIA2/AACT2 4N27/4N28 IL5/HIIA1 4N35/4N36/4N37 CNY 17 Series HIIAA3/HIIAA1/HIIAA4	ILCT6/ILD1/AACT6 ILCT6/ILD1 ILD5 ILD2 ILD610-1, -2, -3, & -4 ILD250/ILD251/IDL252	ILQ1 ILQ1 ILQ5 ILQ2	
Type: Darlington				
400 (TYP) (2) 400 (2) 400 (3) 800 800	IL30/HIIB3 IL31/HIIB2 IL55 4N32 4N33	ILD30 ILD31 ILD55 ILD32 ILD33	ILQ30 ILQ31 ILQ55 ILQ32 ILQ33	

Footnotes: (1) bidirectional input; (2) BV_{CFO} = 30V; (3) BV_{CFO} = 55V

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TABLE 1—REPRESENTATIVE MICROPOWER OP AMPS

		SUPPLY- VOLTAGE RANGE (V)	QUIESCENT SUPPLY CURRENT PER OP AMP ³ (µA)	MAXIMUM INPUT OFFSET VOLTAGE (mV)	MAXIMUM INPUT BIAS CURRENT (nA)	MAXIMUM INPUT OFFSET CURRENT (nA)	
ADVANCED LINEAR	ALD1701G	491		300 MAX, FOR V _S = ± 2.5V	10	0.050	0.030
DEVICES	ALD1701	1	±1 TO ±6 (ABS MAX)	250 MAX, 120 TYP FOR V _S = ±2.5V	4.5	0.030	0.025
	ALD1701B		2 TO 12 (ABS MAX)	250 MAX, 120 TYP FOR V _S = ±2.5V	2	0.030	0.025
	ALD1701A			250 MAX, 120 TYP FOR V _S = ±2.5V	0.9	0.030	0.025
	ALD1706G ALD1706		±1 TO ±6 (ABS MAX)	50 MAX, 20 TYP FOR $V_S = \pm 2.5V$ 40 MAX, 20 TYP FOR $V_S = \pm 2.5V$	10 4.5	0.050 0.030	0.030 0.025
	ALD1706B	1	2 TO 12 (ABS MAX)	40 MAX, 20 TYP FOR V _s = ±2.5V	2	0.030	0.025
	ALD1706A			40 MAX, 20 TYP FOR $V_S = \pm 2.5V$	0.9	0.030	0.025
	ALD2701	2701B 2 2 10 12 (ABS MAX) 250 MAX, 120 TYP FOR V _S = ±2.5V 5		0.050	0.030		
	ALD2701B				0.030 0.030	0.025 0.025	
	ALD2701A			9			
	ALD4701 ALD4701B	4	±1 TO ±6 (ABS MAX)	250 MAX, 120 TYP FOR $V_s = \pm 2.5V$ 250 MAX, 120 TYP FOR $V_s = \pm 2.5V$	10 5	0.030 0.030	0.025 0.025
	ALD4701A		2 TO 12 (ABS MAX)	250 MAX, 120 TYP FOR V _S = ±2.5V	2	0.030	0.025
ANALOG DEVICES	AD548-J, -A, -S			200 MAX, 170 TYP	2	0.020	0.010
	AD548-K, -B, -T	1	±4.5 TO ±18 (ABS MAX)	200 MAX, 170 TYP	0.5	0.010	0.005
	AD548C			200 MAX, 170 TYP	0.25	0.010	0.005
	AD648-J, -A, -S AD648-K, -B, -T	2	±4.5 TO ±18 (ABS MAX)	200 MAX, 170 TYP 200 MAX, 170 TYP	2	0.020 0.010	0.010
	AD648C	2	14.5 TO 1 16 (ABS WAX)	200 MAX, 170 TYP	0.3	0.010	0.005
BURR-BROWN	OPA21G	Berthall Co.		325 MAX	0.5	50	4
	OPA21E	1	±2.5 TO ±18 (ABS MAX)	230 MAX, 200 TYP	0.1	25	1
	OPA201-AG, -RG	1		500 MAX, 425 TYP	0.5	50	4
	OPA201-BG, -SG	SEE	±2.5 TO ±18 (ABS MAX)	500 MAX, 425 TYP	0.2	40	2
	OPA201CG	COMMENT		500 MAX, 425 TYP	0.1	25	1
HARRIS	HA5141	1		150 MAX, 100 TYP 80 MAX, 45 TYP FOR V _s = 5V	6	100	10
	HA5142	2	±1.5 TO ±15	150 MAX, 100 TYP	6	100	10
			3 TO 30	80 MAX, 45 TYP FOR V _S = 5V			
	HA5144	4		150 MAX, 100 TYP	6	100	10
	MAERES			80 MAX, 45 TYP FOR V _S = 5V		050	50
	HA5151	1		250 MAX, 200 TYP 250 MAX, 200 TYP FOR V _S =5V	3	250	50
	HA5152	2	±1.5 TO ±15	250 MAX, 200 TYP	3	250	50
	HAETEA	4	3 TO 30	250 MAX, 200 TYP FOR V _S =5V	3	050	50
	HA5154	4		250 MAX, 200 TYP 250 MAX, 200 TYP FOR V _S =5V	3	250	50
LINEAR	LT1078-M, -C	2		75 MAX, 47 TYP AT V _S = ± 15V	0.35	10	0.35
TECHNOLOGY				55 MAX, 39 TYP AT V _S =5V	0.12	10	0.35
	LT1078-AM, -AC	2	±0.9 TO ±15	65 MAX, 46 TYP AT V _S = ± 15V	0.25	8	0.25
	LT1079-M, -C	4	1.8 TO 30	50 MAX, 38 TYP AT $V_S = 5V$ 75 MAX, 47 TYP AT $V_S = \pm 15V$	0.07 0.35	8	0.25 0.35
				55 MAX, 39 TYP AT V _S =5V	0.15	10	0.35
	LT1079-AM, -AC	4		65 MAX, 46 TYP AT V _S = ± 15V 50 MAX, 38 TYP AT V _S = 5V	0.25	8	0.25
	1747014	0			0.10	8	0.25
	LT1178-M, -C	2		25 MAX, 17 TYP AT V _S = ±15V 21 MAX, 14 TYP AT V _S = 5V	0.48 0.12	6	0.35 0.35
	LT1178-AM, -AC	2		21 MAX, 16 TYP AT V _S = ± 15V	0.35	5	0.25
	1747044 0		±0.85 TO ±15	18 MAX, 13 TYP AT V _S = 5V	0.07	5	0.25
	LT1179-M, -C	4	1.7 TO 30	25 MAX, 17 TYP AT V _S = ±15V 21 MAX, 14 TYP AT V _S = 5V	0.48 0.15	6	0.35 0.35
	LT1179-AM, -AC	4		21 MAX, 16 TYP AT V _S = ± 15V	0.35	5	0.25
				18 MAX, 13 TYP AT V _S =5V	0.10	5	0.25
MAXIM	ICL76-1 × D, -2 × D	1, 2		250 MAX, 100 TYP AT I _{set} = 100 μA;	15	0.050	0.030
	ICL76-1 × B, -2 × B	1, 2	±1 TO ±8	20 MAX, 100 TYP AT $l_{set} = 100 \mu A$, 20 MAX, 10 TYP AT $l_{set} = 10 \mu A$	5	0.050	0.030
				FOR V _S = ±5V FOR ALL GRADES			
	ICL76-1 × A, -2 × A	1, 2			2	0.050	0.030
	ICL76-3×E, -4×E	3, 4		250 MAX, 100 TYP AT I _{set} = 100 μA;	20	0.050	0.030
	ICL76-3×C, -4×C	3, 4	±1 TO ±8	22 MAX, 10 TYP AT $I_{set} = 10 \mu A$	10	0.050	0.030
	101700.0			FOR V _S = ±5V FOR ALL GRADES		100	
	ICL76-3×B, -4×B	3, 4			5	0.050	0.030
	MAX422C MAX423C			500 MAX, 300 TYP 500 MAX, 300 TYP	0.010 0.010	0.100 0.100	0.200 0.200
	MAX422-E, -M	1	±2.5 TO ±16.5	500 MAX, 300 TYP	0.010	0.100	0.200
	MAX423-E, -M	P. 14.		500 MAX, 300 TYP	0.005	0.030	0.060
	MAX432-E	1	±2.5 TO ±16.5	500 MAX, 300 TYP	0.010	0.100	0.200
	MAX432-C		12.0 10 110.0	500 MAX, 300 TYP	0.005	0.100	0.200
NATIONAL	LF441	1	+5 TO +40 (150 1100	250 MAX, 150 TYP	5	0.100	0.050
SEMICONDUCTOR	LF441A LF442	1 2	±5 TO ±18 (ABS MAX)	200 MAX, 150 TYP FOR V _S = ±20V 250 MAX, 200 TYP	0.5 5	0.050 0.100	0.025 0.050
	LF442A	2	±5 TO ±22 (ABS MAX)	200 MAX, 150 TYP FOR V _S = ±20V	1	0.100	0.050
	LF444 LF444A	4 4	FOR A-SUFFIX VERSIONS	250 MAX, 200 TYP 200 MAX, 150 TYP FOR V _S = ±20V	10 5	0.100	0.050 0.025

1) THE TABLE LISTS OP AMPS THAT HAVE A MAXIMUM SUPPLY CURRENT SPECIFICATION OF 500 μ A OR LESS AT 25°C.

2) ALL LISTED SPECIFICATIONS ARE THOSE THAT APPLY FOR AN AMBIENT TEMPERATURE OF 25°C UNLESS OTHERWISE INDICATED.

3) LISTED SPECIFICATION APPLIES FOR V_S = ±15V UNLESS OTHERWISE STATED.

4) PRICE LISTED IS FOR THE LOWEST GRADE DEVICE.

	MINIMUM COMMON-MODE INPUT-VOLTAGE RANGE ³ (V)	MINIMUM OUTPUT- VOLTAGE RANGE ³ (V)	TYPICAL GAIN × BANDWIDTH ³ (kHz)	TYPICAL SLEW RATE ³ (V/µSEC)	PACKAGE TYPES	PRICE4 (100)	COMMENTS
	+V _s TO -V _s	+V _s TO -V _s	700 FOR $V_S = \pm 2.5V$ 1000 FOR $V_S = \pm 5V$	0.7 FOR $V_S = \pm 2.5V$ 1 FOR $V_S = \pm 5V$	DIP-8, SO-8, DICE	\$1.55	
	+V _s TO -V _s	+V _s TO -V _s	400 FOR V _S = ±2.5V 300 FOR V _S = ±1V	0.17 FOR $V_S = \pm 2.5V$ 0.17 FOR $V_S = \pm 1V$	DIP-8, SO-8, DICE	\$1.89	
	+V _s TO -V _s	+V _s TO -V _s	700 FOR V _S = ±2.5V 1000 FOR V _S = ±5V	0.7 FOR $V_S = \pm 2.5V$ 1 FOR $V_S = \pm 5V$	DIP-8, SO-14, DICE	\$1.90	
	+V _S TO -V _S	+V _S TO -V _S	700 FOR $V_S = \pm 2.5V$ 1000 FOR $V_S = \pm 5V$	0.7 FOR $V_S = \pm 2.5V$ 1 FOR $V_S = \pm 5V$	DIP14, SO-24	\$3.63	
	±11	± 12	1000	1.8	DIP-8, TO-99	\$0.75	
	±11	± 12	1000	1.8	DIP-8, TO-99	\$1.25	
	-12.5 TO +14.3	-13.7 TO +14	300	0.2	DIP-8	\$3.25	
	± 12.5	± 13.5	500	0.18	DIP-14	\$4.05	HAS TWO DIGITALLY SELECTABLE DIFFERENTIAL INPUT STAGES FEE ING ONE OUTPUT STAGE
	±10 0 TO 3 FOR V _S =5V	± 10 1.0 TO 3.8 FOR V _S =5V	400	1.5	SINGLE: DIP-8, TO-99 DUAL: DIP-8, TO-99 QUAD: DIP-14	HA5141: \$4.05	
	±10 0 TO 3 FOR V _S =5V	± 10 1.0 TO 3.2 FOR V _S =5V	1300	6 4.5 FOR V _S =5V	SINGLE: DIP-8, TO-99 DUAL: DIP-8, TO-99 QUAD: DIP-14	HA5151: \$4.05	
The second second second	-15 TO +135 0 TO 35 FOR V _S =5V	± 13 0 TO 4.2 FOR V _S =5V	200 FOR V _S =5V	0.1 FOR V _S = ±15V 0.07 FOR V _S =5V	DUALS: DIP-8, TO-5 QUADS: DIP-14	LT1078: \$2.80 LT1079: \$3.50	
	-15 TO +135 0 TO 35 FOR V _S =5V	±13 0 TO 4.2 FOR V _S =5V	85 FOR $V_S = \pm 15V$ 60 FOR $V_S = 5V$	0.04 FOR V _S = ±15V 0.025 FOR V _S =5V	DUALS: DIP-8, TO-5 QUADS: DIP-14	LT1178: \$3.00 LT1179: \$3.50	
	ICL7612: -5.1 TO +5.3 ICL7616-A, -B: -5.1 TO +3 ICL7616D: -5.1 TO +2.7 OTHERS: -4.0 TO +4.2 AT I _{Set} =100 µA FOR V _S = ±5V	±4.9 AT V _S = ±5V	480 AT I_{Set} =100 μ A FOR V_{S} = ±5V 44 AT I_{Set} =10 μ A FOR V_{S} = ±5V	0.16 AT I _{Set} =100 µA FOR V _S = ±5V 0.016 AT I _{Set} =10 µA FOR V _S ±5V	SINGLES: DIP-8, TO-99 DUALS: DIP-8, DIP-14, TO-99	ICL761x: \$0.75 ICL762x: \$1.20	SINGLES: AVAILABLE AS PROGRAM MABLE BIAS CURRENT AND FIXED 100-µA BIAS-CURRENT VERSIONS DUALS: HAVE FIXED 100-µA BIAS CURRENT
	ICL7642: -4.0 TO $+4.4$ FOR V _S = \pm 5V ICL7631, ICL7632: -4.0 TO $+4.2$ AT I _{Set} =100 μ A FOR V _S = \pm 5V	±4.9 AT V _S = ±5V	480 AT I_{Set} =100 μ A FOR V_{S} = ±5V 44 AT I_{Set} =10 μ A FOR V_{S} = ±5V	0.16 AT I_{Set} =100 μ A FOR V_{S} = ±5V 0.016 AT I_{Set} =10 μ A FOR V_{S} = ±5V	TRIPLES: DIP-16 QUADS: DIP-14	ICL763×: \$1.89 ICL764×: \$1.79	TRIPLES: HAVE PROGRAMMABLE BIAS CURRENT QUADS: AVAILABLE WITH FIXED 10-µA OR 1-mA BIAS CURRENT
	-15 TO +12	±14	125	0.125	MAX422: DIP-8, TO-99 MAX423: DIP-14, SO-16, DICE	MAX422: \$4.95 MAX423: \$5.45	CHOPPER STABILIZED
	-15 TO +12	± 14	125	0.125	DIP-8	\$6.22	CHOPPER STABILIZED; REQUIRES NO EXTERNAL CAPACITORS
	± 11 ± 16 ± 11 ± 16 ± 11 ± 16	±12	1000	1	SINGLES: DIP-8, SO-8, TO-99 DUALS: DIP-8, TO-99 QUADS: DIP-14, SO-14, SMD-14	LF441: \$0.50 LF442: \$0.90 LF444: \$1.45	

KEY:

"INDICATES A FIGURE THAT IS APPLICABLE OVER THE DEVICE'S FULL OPERATING TEMPERATURE RANGE
ABS MAX = ABSOLUTE MAXIMUM
COM = COMMERCIAL TEMPERATURE RANGE
DIP-xx = DUAL-IN-LINE PACKAGE (xx DENOTES NUMBER OF PINS)
FP-xx = FLAT PACK (xx DENOTES NUMBER OF LEADS)
IND = INDUSTRIAL TEMPERTURE RANGE
LCC-xx = LEADLESS CHIP CARRIER (xx DENOTES NUMBER OF LEADS)

TYP = TYPICAL

MAX =MAXIMUM
MIL =MILITARY TEMPERATURE RANGE
SO-xx =SMALL OUTLINE SURFACE-MOUNT PACKAGE (xx DENOTES NUMBER OF LEADS)
SMD-xx =0.3-in.-WIDE SURFACE-MOUNT PACKAGE (xx DENOTES NUMBER OF LEADS)
TYP =TYPICAL

TABLE 1—REPRESENTATIVE MICROPOWER OP AMPS (CONTINUED)

MANUFACTURER	TYPE NUMBER	OP AMPS PER PACKAGE	SUPPLY- VOLTAGE RANGE (V)	QUIESCENT SUPPLY CURRENT PER OP AMP ³ (μA)	MAXIMUM INPUT OFFSET VOLTAGE (mV)	MAXIMUM INPUT BIAS CURRENT (nA)	MAXIMUM INPUT OFFSET CURRENT (nA)
NATIONAL	LM146	D. T. S.	±1.5 TO ±22 (ABS MAX)	63 MAX, 35 TYP AT I _{set} = 1 μA	5	20	
SEMICONDUCTOR (CONTINUED)	LM246 LM346	4	±1.5 TO ±18 (ABS MAX) ±1.5 TO ±18 (ABS MAX)	75 MAX, 35 TYP AT $I_{\text{set}} = 1 \mu A$ 75 MAX, 35 TYP AT $I_{\text{set}} = 1 \mu A$	7 7	100 100	I I
	LM4250			100 MAX AT I _{set} = 10 μA	5	50	10
	1111000	1	±1 TO ±18 (ABS MAX)	11 MAX AT I _{sot} = 1 μA	3	7.5	3
	LM4250C			100 MAX AT I _{set} = 10 μA 11 MAX AT I _{set} = 1 μA	6	75 10	6
	LP124		±1.5 TO ±16 (ABS MAX)	32 MAX, 21 TYP AT V _S =5V	2	4	1
			3 TO 32 (ABS MAX)			14.5	
	LP324	4	±1.5 TO ±16 (ABS MAX) 3 TO 32 (ABS MAX)	38 MAX, 21 TYP AT V _S =5V	4	10	2
	LP2902		±1.5 TO ±13 (ABS MAX) 3 TO 26 (ABS MAX)	38 MAX, 21 TYP AT V _S =5v	4	20	4
PRECISION	OP20H		3 10 20 (ABO MIAN)	95 MAX, 60 TYP	11.15	40	4
MONOLITHICS	OP20-C, -G		±2.5 TO ±15	70 MAX, 45 TYP FOR V _S = ±2.5V 85 MAX, 57 TYP	0.5	30	2.5
		1	5 TO 30	55 MAX, 40 TYP FOR V _S = ±2.5V	Sala Sala		
	OP20-B, -F			80 MAX, 55 TYP 63 MAX, 44 TYP FOR V _S = ±2.5V	0.25	25	1.5
	OP21G	PT-Y		420 MAX, 250 TYP	0.5	150	6
	OP21-B, -F	1,121,47		300 MAX, 190 TYP FOR V _S = ±2.5V 360 MAX, 235 TYP	0.2	120	5
		1	±2.5 TO ±15	230 MAX, 170 TYP FOR V _S = ±2.5V			Author The
	OP21-A, -E			300 MAX, 230 TYP 275 MAX, 180 TYP FOR V _S = ±2.5V	0.1	100	4
	OP22-H			210 MAX, 180 TYP AT I _{set} = 10 μA	1	50	3
	OP22-B, -F	F2 # 1	±1.5 TO ±15	21 MAX, 18 TYP AT I _{set} = 1 μA 190 MAX, 160 TYP AT I _{set} = 10 μA	1 0.5	10 35	3 2
	UF22-B, -F	1	3 TO 30	19 MAX, 16 TYP AT I _{set} = 10 μA	0.5	7.5	2
	OP22-A, -E			170 MAX, 150 TYP AT Iget = 10 μA	0.3	30	1
	OP32G			17 MAX, 15 TYP AT I _{set} = 1 μA	0.3	50	3
	OF32G			200 MAX, 150 TYP AT I_{set} = 10 μ A 21 MAX, 15 TYP AT I_{set} = 1 μ A	1	10	3
	OP32-B, -F	1	± 1.5 TO ± 15	190 MAX. 150 TYP AT loot = 10 uA	0.5	35	2 2
	OP32-A, -E		3 TO 30	19 MAX, 15 TYP AT I _{set} = 1 μA 170 MAX, 150 TYP AT I _{set} = 10 μA	0.5 0.3	7.5 35	2
			对此对学师 的意思	17 MAX, 15 TYP AT I _{set} =1 μA	0.3	5	2
	OP220-C, -G			110 MAX, 103 TYP 67.5 MAX, 62.5 TYP FOR V _S = ±2.5V	0.75 0.75	30 30	3.5 3.5
	OP220-B, -F	2	±2.5 TO ±15	95 MAX, 75 TYP	0.73	25	2
	OP220 A E	2	5 TO 30	62.5 MAX, 57.5 TYP FOR V _S = ±2.5V	0.3	25	2
	OP220-A, -E			85 MAX, 70 TYP 57.5 MAX, 50 TYP FOR V _S = ±2.5V	0.15 0.15	20 20	1.5 1.5
	OP221-C, -G	F1 3/12		450 MAX, 425 TYP	0.5	120	7
	OP221-B, -F		±2.5 TO ±15	325 MAX, 275 TYP FOR V _S = ±2.5V 425 MAX, 400 TYP	0.5 0.3	120 100	7 5
	OTZET B, T	2	5 TO 30	300 MAX, 250 TYP FOR $V_S = \pm 2.5V$	0.3	100	5
	OP221-A, -E			400 MAX, 300 TYP 275 MAX, 225 TYP FOR V _S = ±2.5V	0.15	80 80	3 3
	OP420H			150 MAX, 98 TYP	0.15 6	40	6
				100 MAX, 50 TYP FOR V _S = ±2.5V	6	40	6
	OP420-C, -G	4	±2.5 TO ±15 5 TO 30	115 MAX, 90 TYP 75 MAX, 42.5 TYP FOR V _s = ±2.5V	4	30 30	2.5
	OP420-B, -F			90 MAX, 83 TYP	2.5	20	1.5
				50 MAX, 35 TYP FOR $V_S = \pm 2.5V$	2.5	20	1.5
	OP421H		±2.5 TO ±15	500 MAX, 225 TYP FOR V _S = ±2.5V	6 4	150 80	20
	OP421-C, -G OP421-B, -F	4	5 TO 30	375 MAX, 175 TYP FOR V _S = ±2.5V 450 MAX, 300 TYP	2.5	50	5
	OF421-6, 4			250 MAX, 150 TYP FOR $V_S = \pm 2.5V$	2.5	50	5
	OP90G OP90F		±0.8 TO ±18 (ABS MAX)	20 MAX, 14 TYP	0.45	25	5
	OP90-A, -E	1	1.6 TO 36 (ABS MAX)	15 MAX, 9 TYP FOR V _S = ±1.5V FOR ALL GRADES	0.25 0.15	20 15	5
(d)	OP290G		±0.8 TO ±18 (ABS MAX)	20 MAX, 12.5 TYP	0.5	25	5
	OP290F OP290-A, -E	2	1.6 TO 36 (ABS MAX)	15 MAX, 9.5 TYP FOR V _S = ±1.5V FOR ALL GRADES	0.3	20	5
	OP490G	The second		20 MAX, 15 TYP	0.2	15 25	5
	OP490F OP490-A, -E	4	±0.8 TO ±18 (ABS MAX) 1.6 TO 36 (ABS MAX)	15 MAX, 10 TYP FOR V _S = ±1.5V FOR ALL GRADES	0.75	20	5
SGS-THOMSON	TS271			200 MAX, 150 TYP AT I _{set} = 25 μA,	0.5	15 0.15 *	0.1
MICROELECTRONICS	TS271-I, -M	1	4 TO 10	V _S = 10V	10	0.3 *	0.1
	TS271A TS271B		7 10 10	15 MAX, 10 TYP AT I _{set} = 1.5 μA, V _S = 10V FOR ALL GRADES	5 2	0.15 *	0.1
SIEMENS	TAE1453	1			2	0.15 *	0.1
		SEE COMMENT	±1 TO ±18 (ABS MAX)	400 MAX, 250 TYP FOR $V_S = \pm 5V$ TO $\pm 15V$	5.5	150	15

NOTES:

1) THE TABLE LISTS OP AMPS THAT HAVE A MAXIMUM SUPPLY-CURRENT SPECIFICATION OF 500 μ A OR LESS AT 25°C.

2) ALL LISTED SPECIFICATIONS ARE THOSE THAT APPLY FOR AN AMBIENT TEMPERATURE OF 25°C UNLESS OTHERWISE INDICATED.

3) LISTED SPECIFICATION APPLIES FOR $V_S = \pm$ 15V UNLESS OTHERWISE STATED.

4) PRICE LISTED IS FOR THE LOWEST GRADE DEVICE.

MINIMUM COMMON-MO INPUT-VOLTAGE RANG (V)		TYPICAL GAIN × BANDWIDTH ³ (kHz)	TYPICAL SLEW RATE ³ (V/μSEC)	PACKAGE TYPES	PRICE4 (100)	COMMENTS
± 13.5	± 12	100	0.04	DIP-16	LM146: \$5.00 LF246: \$3.00 LM346: \$1.25	PROGRAMMABLE BIAS CURRENT
±13.5 ±0.6 FOR V _S = ±1.5\	± 12 ± 0.6 FOR V _S = ± 1.5V	200 AT I _{set} =10 μA 70 AT I _{set} =1 μA	0.2 AT I _{set} =10 μ A 0.03 AT I _{set} =1 μ A	DIP-8, SO-8	\$1.20	FULLY SPEC'D FOR V _S = ±1.5V
-V _S TO (+V _S -1.5)	0.8 TO 3.4 FOR V _S =5V	100 FOR V _S =5V	0.05 FOR V _S =5V	LP124: DIP-14 LP324: DIP-14, SO-14 LP2902: DIP-14, SO-14	LP124: \$2.75 LP324: \$0.57 LP2902: \$0.75	
-15 TO +135 0 TO 35 FOR V _S =5V	± 14.1 0.7 TO 4.1 FOR V _S =5V	100	0.05	DIP-8, TO-99, DICE	\$3.20	
-14.5 TO +13.5	-13.7 TO +13.9	600	0.25	DIP-8, TO-99, DICE	\$2.50	
-15 TO +13.5 0 TO 3.5 FOR V _S =5V		250 AT I _{set} =10 μA 15 AT I _{set} =1 μA	0.08 AT I _{set} =10 μA 0.008 AT I _{set} =1 μA	DIP-8, TO-99, DICE	\$2.50	PROGRAMMABLE BIAS CURRENT
-15 TO +13.5	$\begin{array}{c} \pm 13.8, \ \pm 0.75 \\ \text{FOR V}_{S} = \pm 1.5V \\ \pm 14, \ \pm 0.8 \\ \text{FOR V}_{S} = \pm 1.5V \\ \pm 14, \ \pm 0.8 \\ \text{FOR V}_{S} = \pm 1.5V \end{array}$	$\sim\!1000$ AT I $_{\mbox{set}}\!=\!10~\mu\mbox{A}$ 100 AT I $_{\mbox{set}}\!=\!1~\mu\mbox{A}$	-0.6 AT I _{set} =10 μ A -0.06 AT I _{set} =1 μ A	DIP-8, DICE	\$2.25	PROGRAMMABLE BIAS CURRENT
-15 TO +13.5 0 TO 3.5 FOR V _S =5V	±14, 0.8 TO 4 FOR V _S =5 ±14, 0.7 TO 4 FOR V _S =5V ±14, 0.7 TO 4 FOR V _S =5V	200	0.05	DIP-8, TO-99, DICE	\$3.50	
-15 TO +13.5 0 TO 3.5 FOR V _S =5V	±13.5, 0.8 TO 4 FOR V _S =5V ±13.8, 0.7 TO 4.1 FOR V _S =5V ±13.8, 0.7 TO 4.1 FOR V _S =5V	600	0.3	DIP-8, TO-99, DICE	\$3.50	
-15 TO +13.5 0 TO 3.5 FOR V _S =5V	± 13.8, 0.9 TO 3.8 FOR V _S =5V ± 14, 0.8 TO 4 FOR V _S =5V ± 14, 0.7 TO 4.1 FOR V _S =5V	150	0.05	DIP-14, LCC-20, DICE	\$1.80	
-15 TO +13.5 0 TO 3.5 FOR V _S =5V	$\begin{array}{c} \text{0.9 TO 3.8 FOR} \\ \text{V}_{\text{S}} = & \text{5V, 0.8 TO 3.9} \\ \text{FOR V}_{\text{S}} = & \text{5V} \\ \pm & \text{14, 0.7 TO 4} \\ \text{FOR V}_{\text{S}} = & \text{5V} \end{array}$	1900	0.5	DIP-14, DICE	\$1.80	
-15 TO +13.5 0 TO 4 FOR V _S =5V	± 14 0 TO 4 FOR V _S =5V	25	0.012	DIP-8, DICE	\$1.65	
-15 TO +13.5 0 TO 4 FOR V _S =5V	± 13.5 0 TO 4 FOR V _S =5V	20	0.012	DIP-8, SO-16, LCC-20, DICE	\$2.50	
-15 TO +13.5 0 TO 4 FOR V _S =5V	± 13.5 0 TO 4 FOR V _S =5V	20	0.012	DIP-14, SO-16, LCC-28, DICE	\$3.30	
0 то 9	8.7 AT I _{set} =25 μA 8.8 AT I _{set} =1.5μA	700 AT $I_{\text{set}} = 25 \mu \text{A}$ 100 AT $I_{\text{set}} = 1.5 \mu \text{A}$	0.6 AT I _{set} =25 μA 0.04 AT I _{set} =1.5μA	DIP-8, SO-8	\$0.29 (1000)	PROGRAMMABLE OP AMP
(-V _S -0.2) TO (+V _S -1.8)	-14.7 TO +14.9	-	1.0	DIP-6, SO-6	DM 1.40	AVAILABLE AS DUAL AND QUAD OP AMPS WITH A SUPPLY CURRENT OF 750 µA MAXIMUM PER OP AMP

KEY:

'INDICATES A FIGURE THAT IS APPLICABLE OVER THE DEVICE'S FULL OPERATING TEMPERATURE RANGE

ABS MAX = ABSOLUTE MAXIMUM

COM = COMMERCIAL TEMPERATURE RANGE

IP-xx = DUAL-IN-LINE PACKAGE (xx DENOTES NUMBER OF PINS)

FP-xx = FLAT PACK (xx DENOTES NUMBER OF LEADS)

IND = INDUSTRIAL TEMPERATURE RANGE

LCC-xx = LEADLESS CHIP CARRIER (xx DENOTES NUMBER OF LEADS)

TYP = TYPICAL

EMPERATURE RANGE
MAX = MAXIMUM
MIL = MILITARY TEMPERATURE RANGE
SO-xx = SMALL OUTLINE SURFACE-MOUNT PACKAGE (xx DENOTES NUMBER OF LEADS)
SMD-xx = 0.3-in.-WIDE SURFACE-MOUNT PACKAGE (xx DENOTES NUMBER OF LEADS)
TYP = TYPICAL

TABLE 1—REPRESENTATIVE MICROPOWER OP AMPS (CONTINUED)

MANUFACTURER	TYPE NUMBER	OP AMPS PER PACKAGE	SUPPLY- VOLTAGE RANGE (V)	QUIESCENT SUPPLY CURRENT PER OP AMP ³ (µA)	MAXIMUM INPUT OFFSET VOLTAGE (mV)	MAXIMUM INPUT BIAS CURRENT (nA)	MAXIMUM INPUT OFFSET CURRENT (nA)
SIEMENS (CONTINUED)	TAF1453	1 SEE COMMENT	±1 TO ±18 (ABS MAX)	350 MAX, 250 TYP FOR V _S = ±5V TO ±15V	4	100	10
SILICONIX	L144C LF144-A, -B	3	±1.5 TO ±15	133 MAX 117 MAX	10 5	250 200	70 50
TELEDYNE SEMICONDUCTOR	TSC900B TSC900A	TSC900A 400 MAX AT		400 MAX AT $V_S = \pm 5V$ 200 MAX, 140 TYP AT $V_S = \pm 5V$	0.015 0.005	0.080 0.050	0.0005 TYP 0.0005 TYP
TEXAS NSTRUMENTS	TLC251C TLC251AC TLC251BC	1	1.4 TO 16	20 MAX, 10 TYP AT LOW BIAS; 300 MAX, 150 TYP AT MEDIUM BIAS FOR $\rm V_S$ = 10V FOR ALL GRADES	10 5 2	0.600* 0.600* 0.600*	0.300 * 0.300 * 0.300 *
	TLC25L-2C, -4C TLC25L-2AC, -4AC TLC25L-2BC, -4BC	2, 4	1.4 TO 16	20 MAX, 10 TYP FOR V _S = 10V; 2 TYP FOR V _S = 1.4V FOR ALL GRADES	10 5 2	0.600* 0.600* 0.600*	0.300 * 0.300 * 0.300 *
	TLC25M-2C, -4C TLC25M-2AC, -4AC TLC25M-2BC, -4BC	2, 4	1.4 TO 16	300 MAX, 150 TYP FOR $V_S = 10V$; 2 TYP FOR $V_S = 1.4V$ FOR ALL GRADES	10 5 2	0.600* 0.600* 0.600*	0.300 * 0.300 * 0.300 *
	TLC271C TLC271AC TLC271BC TLC271I TLC271AI TLC271BI TLC271M	1	3 TO 16 FOR C-SUFFIX GRADES 4 TO 16 FOR I- AND M- SUFFIX GRADES	300 MAX, 143 TYP AT MEDIUM BIAS; 23 MAX, 14 TYP AT LOW BIAS FOR $\rm V_S=10V$ 280 MAX, 105 TYP AT MEDIUM BIAS; 17 MAX, 10 TYP AT LOW EIAS FOR $\rm V_S=5V$ FOR ALL GRADES	10 5 2 10 5 2	0.600* 0.600* 0.600* 2 * 2 * 2 * 35	0.300 * 0.300 * 0.300 * 1 * 1 * 1 * 1 * 15 * 15
	TLC27L-2C, -4C TLC27L-2AC, -4AC TLC27L-2BC, -4BC TLC27L-2I, -4I TLC27L-2AI, -4AI TLC27L-2BI, -4BI TLC27L-2M, -4M	2, 4	3 TO 16 FOR C-SUFFIX GRADES 4 TO 16 FOR I- AND M- SUFFIX GRADES	23 MAX, 14.5 TYP FOR V _S = 10V 17 MAX, 9.5 TYP FOR V _S = 5V FOR ALL GRADES	10 5 2 10 5 2	0.600* 0.600* 0.600* 2 * 2 * 2 * 35 *	0.300* 0.300* 0.300* 1 * 1 * 1 *
	TLC27L-7C, -9C TLC27L-7I, -9I TLC27L-7M, -9M	2, 4	3 TO 16 FOR C-SUFFIX GRADES 4 TO 16 FOR I- AND M- SUFFIX GRADES	23 MAX, 14.5 TYP FOR V_S = 10V 17 MAX, 9.5 TYP FOR V_S = 5V FOR ALL GRADES	$\begin{array}{c} 0.8 \; \text{FOR} \; \text{V}_{\text{S}} = 10\text{V} \\ 0.5 \; \text{FOR} \; \text{V}_{\text{S}} = 5\text{V} \\ 0.8 \; \text{FOR} \; \text{V}_{\text{S}} = 10\text{V} \\ 0.5 \; \text{FOR} \; \text{V}_{\text{S}} = 5\text{V} \\ 0.8 \; \text{FOR} \; \text{V}_{\text{S}} = 10\text{V} \\ 0.5 \; \text{FOR} \; \text{V}_{\text{S}} = 5\text{V} \end{array}$	0.600* 0.600* 2 * 2 * 35 * 35 *	0.300 * 0.300 * 1 * 1 * 1 * 15 * 15 * 15
	TLC27M-2C, -4C TLC27M-2AC, -4AC TLC27M-2BC, -4BC TLC27M-2I, -4I TLC27M-2AI, -4AI TLC27M-2BI, -4BI TLC27M-2M, -4M	2, 4	3 TO 16 FOR C-SUFFIX GRADES 4 TO 16 FOR I- AND M- SUFFIX GRADES	300 MAX, 143 TYP FOR V_S = 10V 280 MAX, 105 TYP FOR V_S = 5V FOR ALL GRADES	10 5 2 10 5 2 10	0.600* 0.600* 0.600* 2 * 2 * 2 * 35 *	0.300 * 0.300 * 0.300 * 1
	TLC27M-7C, -9C TLC27M-7I, -9I TLC27M-7M, -9M	2, 4	3 TO 16 FOR C-SUFFIX GRADES 4 TO 16 FOR I- AND M- SUFFIX GRADES	300 MAX, 143 TYP FOR $\rm V_S$ = 10V 280 MAX, 105 TYP FOR $\rm V_S$ = 5V FOR ALL GRADES	$\begin{array}{c} 0.8 \; \text{FOR} \; \text{V}_{\text{S}} = 10\text{V} \\ 0.5 \; \text{FOR} \; \text{V}_{\text{S}} = 5\text{V} \\ 0.8 \; \text{FOR} \; \text{V}_{\text{S}} = 10\text{V} \\ 0.5 \; \text{FOR} \; \text{V}_{\text{S}} = 5\text{V} \\ 0.8 \; \text{FOR} \; \text{V}_{\text{S}} = 10\text{V} \\ 0.5 \; \text{FOR} \; \text{V}_{\text{S}} = 5\text{V} \end{array}$	0.600* 0.600* 2 * 2 * 35 * 35 *	0.300 * 0.300 * 1
	TL03-1C, -2C TL03-1AC, -2AC TL03-1I, -2I TL03-1AI, -2AI TL034-C, -I TL034-AC, -AI	1, 2 1, 2 1, 2 1, 2 4 4	±5 TO ±15	280 MAX, 217 TYP 250 MAX, 192 TYP FOR V _S = ±5V FOR ALL GRADES	1.5 FOR $V_S = \pm 15V$ 3.5 FOR $V_S = \pm 5V$ 0.8 FOR $V_S = \pm 15V$ 2.8 FOR $V_S = \pm 15V$ 2.5 FOR $V_S = \pm 5V$ 3.5 FOR $V_S = \pm 15V$ 0.8 FOR $V_S = \pm 15V$ 4 FOR $V_S = \pm 15V$ 6 FOR $V_S = \pm 15V$ 1.5 FOR $V_S = \pm 15V$ 3.5 FOR $V_S = \pm 15V$	0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2	0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1
TES:	TLC1078C TLC1078I TLC1079C TLC1079I	2 2 4 4	1.4 TO 16 FOR C-SUFFIX GRADES 3 TO 16 FOR I-SUFFIX GRADES	23 MAX, 14.5 TYP FOR V_S = 10V 17 MAX, 9.5 TYP FOR V_S = 5V FOR ALL GRADES	0.6 FOR V _S = 10V 0.45 FOR V _S = 5V 0.6 FOR V _S = 10V 0.45 FOR V _S = 5V 1.15 FOR V _S = 10V 0.85 FOR V _S = 5V 1.15 FOR V _S = 10V 0.85 FOR V _S = 5V	0.600° 0.600° 2 ° 0.600° 0.600° 2 °	0.300 * 0.300 * 1 * 0.300 * 0.300 * 1 * 1

NOTES:

1) THE TABLE LISTS OP AMPS THAT HAVE A MAXIMUM SUPPLY-CURRENT SPECIFICATION OF 500 μ A OR LESS AT 25°C.

2) ALL LISTED SPECIFICATIONS ARE THOSE THAT APPLY FOR AN AMBIENT TEMPERATURE OF 25°C UNLESS OTHERWISE INDICATED.

3) LISTED SPECIFICATION APPLIES FOR V_S = \pm 15V UNLESS OTHERWISE STATED.

4) PRICE LISTED IS FOR THE LOWEST GRADE DEVICE.

	MINIMUM COMMON-MODE INPUT-VOLTAGE RANGE ³ (V)	MINIMUM OUTPUT- VOLTAGE RANGE ³ (V)	TYPICAL GAIN × BANDWIDTH ³ (kHz)	TYPICAL SLEW RATE ³ (V/µSEC)	PACKAGE TYPES	PRICE4 (100)	COMMENTS
	(-V _S -0.3) TO (+V _S -1.5)	-14.7 TO +14.9		1.0	DIP-6, SO-6	DM 2.00	AVAILABLE AS DUAL AND QUAD O AMPS WITH A SUPPLY CURRENT OF 750 µA MAXIMUM PER OP AMP
	±12	± 10	600	0.4	DIP-14, FP-14	\$15.90	PROGRAMMABLE BIAS CURRENT (FIGURES QUOTED ARE FOR AN R_{Set} = 3 Ω)
I	-5 TO +1.5 FOR $V_S = \pm 5V$	$-4.9 \text{ TO } +3.9 \text{ FOR}$ $V_S = \pm 5V$	700 FOR V _S = ±5V	0.2	DIP-8, DIP-14	\$2.17	CHOPPER STABILIZED
	-0.2 TO +9 FOR V _S =10V 0 TO 0.2 FOR V _S =1.4V	0 TO 8 FOR V _S =10V 0 TO 0.45 FOR V _S =1.4V	100 AT LOW BIAS SETTING 700 AT MEDIUM BIAS SETTING FOR V_S =10V	0.04 AT LOW BIAS SETTING 0.6 AT MEDIUM BIAS SETTING	DIP-8, SO-8	\$1.88	THREE PROGRAMMABLE BIAS CURRENT SETTINGS
	$-0.2~\mathrm{TO}~+9~\mathrm{FOR}~\mathrm{V_S}{=}10\mathrm{V}$ 0 to 0.2 FOR $\mathrm{V_S}{=}1.4\mathrm{V}$	0 TO 8 FOR V _S =10V 0 TO 0.45 FOR V _S =1.4V	100 FOR V _S =10V 12 FOR V _S =1.4V	0.04 FOR V _S =10V 0.001 FOR V _S =1.4V	DUALS: DIP-8, SO-8 QUADS: DIP-14, SO-14	TLC25L2: \$3.13 TLC25L4: \$5.21	
	-0.2 TO +9 FOR V _S =10V 0 TO 0.2 FOR V _S =1.4V	0 TO 8 FOR V _S =10V 0 TO 0.45 FOR V _S =1.4V	700 FOR V _S = 10V 12 FOR V _S = 1.4V	0.6 FOR V _S =10V 0.001 FOR V _S =1.4V	DUALS: DIP-8, SO-8 QUADS: DIP-14, SO-14	TLC25M2: \$3.13 TLC25M4: \$5.21	
	$\begin{array}{l} -0.2 \text{ TO } +9 \text{ FOR V}_S = 10 \text{V} \\ -0.2 \text{ TO } +4 \text{ FOR V}_S = 5 \text{V} \\ \text{FOR COM (-C) AND} \\ \text{IND (-I) GRADES} \\ 0 \text{ TO } 9 \text{ FOR V}_S = 10 \text{V} \\ 0 \text{ TO } 4 \text{ FOR V}_S = 5 \text{V} \\ \text{FOR MIL (-M) GRADES} \end{array}$	0.05 TO 8 FOR V_8 =10V 0.05 TO 3.2 FOR V_8 =5V	635 AT MEDIUM BIAS FOR $\rm V_S$ =10V 110 AT LOW BIAS FOR $\rm V_S$ =10V 525 AT MEDIUM BIAS FOR $\rm V_S$ =5V 85 AT LOW BIAS FOR $\rm V_S$ =5V	0.62 AT MEDIUM BIAS FOR $\rm V_S$ =10V 0.05 AT LOW BIAS FOR $\rm V_S$ =10V 0.43 AT MEDIUM BIAS FOR $\rm V_S$ =5V 0.03 AT LOW BIAS FOR $\rm V_S$ =5V	DIP-8, SO-8, LCC-20	\$0.47	THREE PROGRAMMABLE BIAS SETTINGS
	$ \begin{array}{l} -0.2 \text{ TO } +9 \text{ FOR V}_{\text{S}} = 10\text{V} \\ -0.2 \text{ TO } +4 \text{ FOR V}_{\text{S}} = 5\text{V} \\ \text{FOR COM (-C) AND} \\ \text{IND (-I) GRADES} \\ 0 \text{ TO } 9 \text{ FOR V}_{\text{S}} = 10\text{V} \\ 0 \text{ TO } 4 \text{ FOR V}_{\text{S}} = 5\text{V} \\ \text{FOR MIL (-M) GRADES} \end{array} $	0.05 TO 8 FOR V _S =10V 0.05 TO 3.2 FOR V _S =5V	110 FOR V _S =10V 85 FOR V _S =5V	0.05 FOR V _S =10V 0.03 FOR V _S =5V	DUALS: DIP-8, SO-8, LCC-20 QUADS: DIP-14, SO-14, LCC-20	TLC27L2: \$0.77 TLC27L4: \$1.25	
	$ \begin{array}{l} -0.2 \text{ TO } +9 \text{ FOR V}_{S} = 10 \text{V} \\ -0.2 \text{ TO } +4 \text{ FOR V}_{S} = 5 \text{V} \\ \text{FOR COM (-C) AND} \\ \text{IND (-I) GRADES} \\ 0 \text{ TO } 9 \text{ FOR V}_{S} = 10 \text{V} \\ 0 \text{ TO } 4 \text{ FOR V}_{S} = 5 \text{V} \\ \text{FOR MIL (-M) GRADES} \end{array} $	0.05 TO 8 FOR V _S =10V 0.05 TO 3.2 FOR V _S =5V	110 FOR V _S =10V 85 FOR V _S =5V	0.05 FOR V_S =10V 0.03 FOR V_S =5V	DUALS: DIP-8, SO-8, LCC-20 QUADS: DIP-14, SO-14, LCC-20	TLC27L7: \$1.59 TLC27L9: \$2.61	
	$ \begin{array}{lll} -0.2 \text{ TO } +9 \text{ FOR V}_{\text{S}} = 10\text{V} \\ -0.2 \text{ TO } +4 \text{ FOR V}_{\text{S}} = 5\text{V} \\ \text{FOR COM (-C) AND} \\ \text{IND (-I) GRADES} \\ 0 \text{ TO } 9 \text{ FOR V}_{\text{S}} = 10\text{V} \\ 0 \text{ TO } 4 \text{ FOR V}_{\text{S}} = 5\text{V} \\ \text{FOR MIL (-M) GRADES} \end{array} $	0.05 TO 8 FOR $V_S = 10V$ 0.05 TO 3.2 FOR $V_S = 5V$	635 FOR V _S =10V 525 FOR V _S =5V	0.62 FOR V_S =10V 0.43 FOR V_S =5V	DUALS: DIP-8, SO-8, LCC-20 QUADS: DIP-14, SO-14, LCC-20	TLC27M2: \$0.77 TLC27M4: \$1.25	
	$ \begin{array}{lll} -0.2 \text{ TO } +9 \text{ FOR V}_{\text{S}} =& 10\text{V} \\ -0.2 \text{ TO } +4 \text{ FOR V}_{\text{S}} =& 5\text{V} \\ \text{FOR COM (-C) AND} \\ \text{IND (-I) GRADES} \\ 0 \text{ TO } 9 \text{ FOR V}_{\text{S}} =& 10\text{V} \\ 0 \text{ TO } 4 \text{ FOR V}_{\text{S}} =& 5\text{V} \\ \text{FOR MIL (-M) GRADES} \\ \end{array} $	0.05 TO 8 FOR $V_S = 10V$ 0.05 TO 3.2 FOR $V_S = 5V$	635 FOR V _S =10V 525 FOR V _S =5V	0.62 FOR V _S =10V 0.43 FOR V _S =5V	DUALS: DIP-8, SO-8, LCC-20 QUADS: DIP-14, SO-14, LCC-20	TLC27M7: \$1.59 TLC27M9: \$2.61	
	-11.5 TO +14 -1.5 TO +4 FOR V _S = ±5V	12.5 TO +13 ±3 FOR V _S =5V	1100 FOR V _S = ±15V 1000 FOR V _S = ±5V	2.9 FOR $V_S = \pm 15V$ 2 FOR $V_S = \pm 5V$	SINGLES: DIP-8, SO-8, LCC-20 DUALS: DIP-8, SO-8, LCC-20 QUADS: DIP-14, SO-14, LCC-20	TL031: \$0.57 TL032: \$0.77 TL034: \$1.42	
	-0.2 TO +9 FOR V _S =10V -0.2 TO +4 FOR V _S =5V	0.025 TO 8.2 FOR V _S =10V 0.025 TO 3.2 FOR V _S =5V	110 FOR V _S =10V 85 FOR V _S =5V	0.047 FOR V _S =10V 0.032 FOR V _S =5V	DUALS: DIP-8, SO-8, LCC-20 QUADS: DIP-14, SO-14, LCC-20	TLC1078: \$2.76 TLC1079: \$4.01	

MAX =MAXIMUM
MIL =MILITARY TEMPERATURE RANGE
SO-xx =SMALL OUTLINE SURFACE-MOUNT PACKAGE (xx DENOTES NUMBER OF LEADS)

SMD-xx =0.3-in.-WIDE SURFACE-MOUNT PACKAGE (xx DENOTES NUMBER OF LEADS)
TYP =TYPICAL





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LEADTIME INDEX

Percentage of respondents

							last.	
•			,	12	Ove		Last month's (weeks)	
	the shelf	5. W. O. TO	7.20	21-30 Weeks	, 30 W	2	The We	ale.
ITEM	Shelf	leeks	veeks	leeks	eeks	leeks	eeks,	King R
TRANSFORMERS		_	U.					
Toroidal	0	17	66	17	0	0	8.4	11.
Pot-Core	8	8	53	23	8	0	10.0	11.
Laminate (power)	0	15	62	23	0	0	8.9	7.
CONNECTORS								
Military panel	33	0	33	17	17	0	9.6	9.
Flat/Cable	18	35	35	12	0	0	5.7	6.
Multi-pin circular	22	0	56	22	0	0	7.8	6.
PC (2-piece)	8	33	33	26	0	0	7.6	5.
RF/Coaxial	11	33	33	23	0	0	7.1	5.
Socket	12	41	35	12	0	0	5.8	4.
Terminal blocks	7	20	53	20	0	0	7.9	5.
Edge card	7	40	40	13	0	0	6.4	5.
D-Subminiature	6	50	31	13	0	0	5.9	4.
Rack & panel	10	30	40	20	0	0	7.1	5.
Power	9	27	45	19	0	0	7.3	5.
PRINTED CIRCUIT BOAF								
Single sided	5	42	42	11	0	0	6.3	5.
Double sided	0	38	54	8	0	0	6.6	6.
Multi-layer	0	17	66	17	0	0	8.4	8.
Prototype	8	75	17	0	0	0	3.6	3.
RESISTORS	-		124		HALL IN			
Carbon film	30	35	35	0	0	0	3.8	3.
Carbon composition	30	26	35	9	0	0	4.9	4.
Metal film	26	30	39	5	0	0	4.7	3.
Metal oxide Wirewound	0	38	54	8	0	0	6.6	3.
Potentiometers	20	20	55 36	5 18	0	0	5.7	4.0
Networks	20	40	35	5	0	0	6.8	5.
FUSES							4.7	
	14	36	50	0	0	0	5.0	3.
SWITCHES Pushbutton	17	28	44	11	0	0	6.0	
Rotary	6	41	41	11	0	0	6.0	5.9
Rocker	6	47	41	6	0	0	5.6	5.
Thumbwheel	10	20	50	20	0	0	7.6	5.4
Snap action	7	27	46	13	7	0	8.2	6.3
Momentary	6	44	44	6	0	0	5.7	5.8
Dual-in-line	9	45	36	10	0	0	5.7	5.2
WIRE AND CABLE								
Coaxial	25	25	37	13	0	0	5.7	4.
Flat ribbon	35	40	20	5	0	0	3.5	3.
Multiconductor	26	32	37	5	0	0	4.6	5.0
Hookup	29	41	30	0	0	0	3.6	2.8
Wirewrap	38	23	31	8	0	0	4.4	2.7
Power cords	16	41	32	11	0	0	5.4	5.
POWER SUPPLIES								
Switcher	8	17	58	17	0	0	7.7	6.
Linear	17	33	33	17	0	0	6.2	5.3
CIRCUIT BREAKERS	11	11	56	22	0	0	8.2	7.
HEAT SINKS	8	33	33	26	0	0	7.6	4.0
BATTERIES		30	50		0	-	7.0	7.0
Lithium coin cells	30	20	30	20	0	0	6.1	3.8
9V alkaline	60	10	30	0	0	0	2.7	1.3
Real-time clock back-up	43	14	43	0	0	0	3.8	4.
RELAYS					J	0	3.0	7.
General purpose	27	13	26	27	7	0	8.4	8.0
PC board	0	38	23	31	8	0	9.8	8.5

					0		mo	
ITEM Dry reed	1	6,	11-20 Weeks 25	21-30 Weeks	Over 30 o		t month's (weeks) 8.9	
The state of the s	2	6.10 Weeks	We	wes	6	Wes	Wera	era
ITEM	6	K	eks .	1	*	To	TO B	600
Dry reed	0	37	25	38	0	0	8.9	9.
Mercury	0	0	25	75	0	0	13.6	8.
Solid state	0	50	0	50	0	0	9.2	9.
DISCRETE SEMICONDUCTO	RS							
Diode	28	20	32	20	0	0	6.2	5.
Zener	22	26	17	35	0	0	7.5	5.
Thyristor	13	25	25	37	0	0	8.4	5.
Small signal transistor	21	21	16	42	0	0	8.4	6.
MOSFET	20	13	40	27	0	0	7.7	7.
Power, bipolar	8	25	42	25	0	0	7.9	6.
INTEGRATED CIRCUITS, D	IGITA	L						
Advanced CMOS	15	15	40	30	0	0	8.2	5.
CMOS	23	14	45	18	0	0	6.8	6.
TTL	35	13	35	17	0	0	5.8	4.
LS	36	23	27	14	0	0	5.0	4.
INTEGRATED CIRCUITS, LI	NEAF	?						
Communication/Circuit	20	0	40	30	10	0	10.3	6.
OP amplifier	14	8	57	21	0	0	8.0	6.
Voltage regulator	19	25	37	19	0	0	6.6	5
MEMORY CIRCUITS								
DRAM 16K	18	18	10	45	9	0	10.6	12
DRAM 64K	9	18	18	45	10	0	11.5	14
DRAM 256K	8	17	25	42	8	0	11.0	14
DRAM 1M-bit	9	10	27	45	9	0	11.7	14.
SRAM 4K × 4	10	10	30	40	10	0	11.4	12.
SRAM 8K × 8	8	0	31	38	15	8	14.6	15
SRAM 2K × 8	11	0	11	78	0	0	12.9	14
ROM/PROM	8	9	50	33	0	0	9.3	11.
EPROM 64K	6	19	37	38	0	0	9.4	10.
EPROM 256K	14	7	43	29	7	0	9.9	10
EPROM 1M-bit	0	0	29	57	14	0	14.7	12
EEPROM 16K	10	0	50	30	10	0	11.1	11
EEPROM 64K	0	8	31	53	8	0	12.9	12
DISPLAYS								
Panel meters	0	13	49	38	0	0	10.1	4.
Fluorescent	0	17	17	49	17	0	13.7	6
CRT 12-inch monochrome	11	23	22	44	0	0	9.2	7.
LED	23	31	31	15	0	0	5.7	6
Liquid crystal	0	23	46	31	0	0	9.1	10.
MICROPROCESSOR ICs								
8-bit	9	19	45	27	0	0	8.3	8.
16-bit	10	20	30	40	0	0	9.1	9
32-bit	0	27	18	45	10	0	11.7	11.
FUNCTION PACKAGES								
Amplifier	22	12	44	22	0	0	7.2	7
Converter, analog to digital	9	19	45	27	0	0	8.3	8
Converter, digital to analog	10	20	40	30	0	0	8.4	8
LINE FILTERS	10	30	10	50	0	0	9.4	6
CAPACITORS				30			01.7	-
Ceramic monolithic	20	35	20	25	0	0	6.5	5.
Ceramic disc	13	25	37	25	0	0	7.5	4.
Film	17	28	22	33	0	0	7.7	5.
Aluminum electrolytic	11	17	39	33	0	0	8.7	5.
Tantalum	18	12	41	29	0	0	8.7	5.
			1000					
INDUCTORS	0	29	35	36	0	0	9.2	7

Source: Electronics Purchasing Magazine's survey of buyers.



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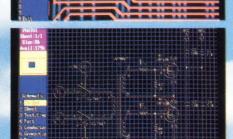
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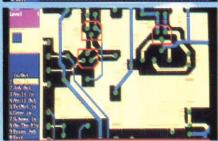
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60-MHz operational amplifier provides 2000V/µsec slew rate

Though it boasts a rapid slew rate, wide bandwidth, and low offset voltage, the AD844 monolithic op amp's best feature may be its price/performance ratio. Commercial versions in an 8-pin plastic miniature DIP cost only \$4.50 in 100-piece quantities. Higher-cost industrial and military versions are also available. While other op amps can meet or exceed an individual AD844 spec, none provide the overall performance at this price level.

The AD844 slews at the dazzling speed of $2000 V/\mu sec$. It also features a number of other impressive specifications. For example, the amplifier's unity-gain bandwidth is 60 MHz and its full-power (20V p-p, $R_L = 500\Omega$) bandwidth is 20 MHz. At 2V p-p, the bandwidth is 40 MHz.

Strictly speaking, the AD844 does not slew-rate limit; instead, it has a constant 10-nsec rise time whether the signal is a 1 or a 20V step. Moreover, because it is a current-feedback op amp, the AD844 does not degrade in bandwidth at higher gains. Although optimized for use in current-to-voltage conversion and as an inverting-mode amplifier, it is also suitable for non-inverting applications.

Settling time is only 100 nsec to 0.1% for a 10V step and is independent of gain. Differential gain error is only 0.1%, and differential phase error is only 0.1° at 3.58 MHz. Powered by a ± 4.5 to $\pm 18V$ supply, the AD844 can drive as much as ± 50 mA into loads as low as 50Ω in parallel with 100 pF, or capacitive loads to 10,000 pF with an external network.

Many of the chip's impressive do specifications result from laser trimming during manufacture. For

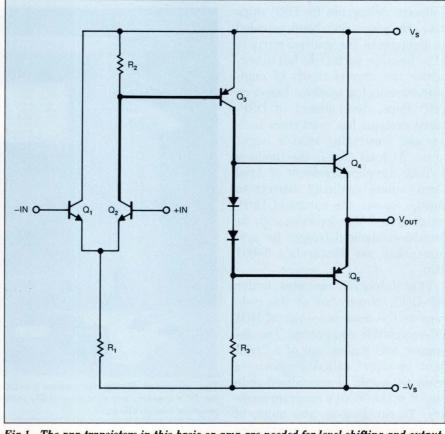


Fig 1—The pnp transistors in this basic op amp are needed for level shifting and output drive. The AD844 op amp features true complementary performance—both the pnp and npn transistors have identical gain-bandwidth products.

example, input offset voltage (V_{os}) is typically 150 μ V, offset-voltage drift is only 2 μ V/°C, and biascurrent drift is a low 8 nA/°C. Quiescent current is 6.5 mA max, and the output is short-circuit protected to 80 mA.

The key contributor to the AD844's ac performance is its CB (complementary bipolar) processing. This process uses p-type epitaxy and a p-well structure with updown isolation to produce npn and pnp bipolar transistors having complementary characteristics. Both the npn and pnp transistors have nearly identical gain-bandwidth products (f₇) of about 550 MHz.

The basic op amp (**Fig 1**) requires pnp transistors for both level shifting and efficient load drive. If, as is typically the case with many op amps, the pnp transistors are much slower (lower f_{τ}) than the npn transistors, the resulting op amp is also slow and exhibits a narrow gain-bandwidth product. An op amp having complementary and identically performing npn/pnp transistors is inherently a better amplifier.

—Dave Pryce

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565.

Circle No 734

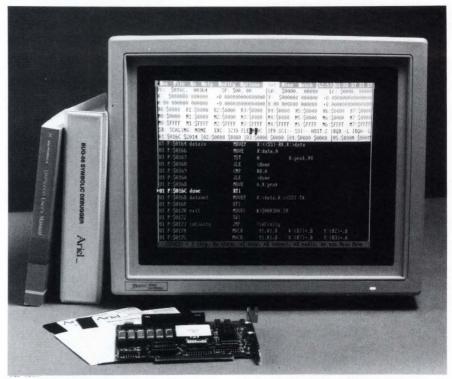
PRODUCT UPDATE

DSP debugger lets you instantly see and hear effects of code changes

Software debuggers for DSP chips have, by and large, been modeled on debuggers for general-purpose μPs. Because such tools fail to recognize the special needs of engineers developing systems based on DSP chips, development of DSPbased systems has been more tedious and frustrating than it ought to be. At least that is the thinking of Tony Agnello, president of Ariel Corp, whose company expects to change forever the nature of DSPbased system development with its Bug-56 symbolic debugger for systems that use Motorola's 56001 chip.

This debugger operates under MS-DOS. Nearly all of the code runs on the main processor of IBM PC-compatible computers. The debugger also makes use of a "resident monitor" called Degmon-a scant 64 words of specialized code placed in the 56001's program memory. To run Bug-56, you must, of course, install a board containing the DSP chip in one of the PC's I/O slots. One such board comes from the debugger's manufacturer. The \$595 PC-56 contains, beside the 56001, a 14-bit ADC and DAC capable of handling analog data at 20k samples/sec. The company plans additional DSP boards with faster, higher-resolution converters.

The software provides a windowed display with pull-down menus that enable you to access many facilities—for example, the full-screen symbolic debugger with program tracing capability, symbolic breakpoints, and symbolic patch assembly. The debugger lets you directly modify control-register bits, and it can update the register display and make changes to register and memory contents while pro-



This windowed display can contain a mixture of text and graphics. Moreover, by use of the PC's speaker, you can, essentially instantaneously, hear as well as see the effects of program modifications.

grams run at full speed. In addition, there is on-line help, a file browser, and a capability called DSPeek, which provides a graphic display of the data in any 56001 memory space with programmable scaling and "zooming." The software can perform an FFT to let you view the data in the frequency domain and can send data to the PC's speaker, enabling you to hear as well as see the effects of program changes.

To avoid having to simultaneously debug programs running on the DSP chip and the PC's μP , Bug-56 lets programs running on the 56001 perform a wide range of MS-DOS functions. Programs running on the DSP chip can access the PC's real-time clock, poll the keyboard, verify the existence of DOS files,

open, read, write, and append those files, and determine the free space on a disk. Such programs can also access custom windows you create to provide users with menu options and information.

Bug-56 for IBM PCs and compatible computers sells for \$395. The manufacturer intends to make it available in the future to run on additional computing systems.

—Dan Strassberg

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Circle No 732



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MODEL	CONFIG- URATION	SPEED (ns)	PACKAGE
CXX5863P	8K x 8	25/30/35	DIP 300 mil
CXX5863M	8K x 8	25/30/35	SOP 450 mil
CXX5863J	8K x 8	25/30/35	SOJ 300 mil
CXX5464AP	16K x 4	25/30/35	DIP 300 mil
CXX5464AJ	16K x 4	25/30/35	SOJ 300 mil
CXX5465P*	16K x 4	25/30/35	DIP 300 mil
CXX5465J*	16K x 4	25/30/35	SOJ 300 mil
CXX5164P	64K x 1	25/30/35	DIP 300 mil
CXX5164J	64K x 1	25/30/35	SOJ 300 mil
CXX5971P	8K x 9	25/30/35	DIP 300 mil
CXX5971J	8K x 9	25/30/35	SOJ 300 mil
CXX58255AP	32K x 8	25/30	DIP 300 mil
CXX58255AJ	32K x 8	25/30	SOJ 300 mil
CXX58258P	32K x 8	35/45	DIP 600 mil
CXX58258SP	32K x 8	35/45	DIP 300 mil
CXX54256P	64K x 4	35/45/55	DIP 300 mil
CXX51256P	256K x 1	35/45/55	DIP 300 mil

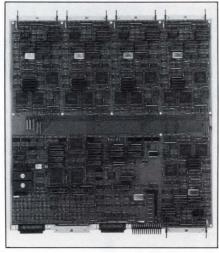
SCSI-2 disk-drive-array controller board stores data across five ESDI drives

Disk-drive arrays offer you a way to improve system data-transfer rates, and now you can buy a disk-drive-array controller board off the shelf. The Rimfire 6600 disk-drive-array controller stores data on four drives and uses a fifth drive to store parity information. The board also offers SCSI-2 (Small Computer System Interface) as an interface to the system and ESDI (Enhanced Small Device Interface) as an interface to the drives. The use of industry-standard interfaces simplifies the system design and integration task.

The Rimfire 6600 and five ESDI drives appear to the system, via the SCSI bus, as a single SCSI drive with a quadruple capacity provided by the individual drives in the array. During write operations, the controller breaks up each byte, word, or long word of data and spreads or "stripes" the data among the four data drives. The controller reconstructs the data during read operations for transmission to the system.

The controller also reads and writes parity data to the fifth drive. The parity drive allows the array to continue to function when any single drive fails. Furthermore, after a single drive failure and replacement with a new drive, the controller can regenerate the data on the replacement drive from data on the four operational drives.

Potentially, the controller provides four times the raw-data-transfer rate offered by a single drive. Typical ESDI drives feature read-channel data rates of 15M bits/sec (almost 2M bytes/sec). The array can generate a raw-data rate four times that number and system transfers at rates as high as 20M



Five ESDI drives and the disk-drive-array controller emulate a large single drive, but they offer raw data rates four times the rate of a single drive and SCSI-2 transfer rates as high as 20M bytes/sec.

bytes/sec. But ultimately, the SCSI implementation on the host may control the true transfer rate.

The interface on the Rimfire 6600 supports the new SCSI-2 specification, including 16- and 32-bit-wide data-transfer options. In the synchronous mode, the controller can transfer data at 20M bytes/sec, using a 32-bit-wide path. The controller retains compatibility with the original 5M byte/sec synchronous, 8-bit SCSI spec, however. Most currently available host adapters support only the original SCSI spec.

The controller includes a 512k-byte cache on board. The cache performs read-ahead operations and allows the interface to operate at maximum speeds of 20M bytes/sec when the data requested by the host is in the cache. Furthermore, read requests from the host have no seek-time delay on cache hits. On reads or writes to the disk, how-

ever, the array subsystem suffers a seek-time latency equal to the seek time associated with a single drive.

Other SCSI-2 controller features include tagged commands. These commands allow the system to perform command queuing; that is, to issue multiple commands to the SCSI controller before the command first issued has been completed. The controller uses tagged commands to optimize operations by combining and sorting commands.

The Rimfire 6600 is offered as a 16×16.5 -in. board suitable for rack mounting. The board costs \$5995 and will be available in August. You can use the controller board with any ESDI drives that offer spindle synchronization.—*Maury Wright*

Ciprico Inc, 2955 Xenium Lane, Plymouth, MN 55441. Phone (612) 559-2034. FAX 612-559-8799. TWX 910-240-0585.

Circle No 731

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MK41H69N	4K x 4	20, 25, 35ns A
MK41H78N	4K x 4	25, 35ns A
MK41H79N	4K x 4	25, 35ns A
MK41H87N/X	64K x 1	35, 45, 55ns A, B
MK48H64N/S	8K x 8	70, 120ns C, D
MK48H65N	8K x 8	35, 45, 55, 70, 120ns A
MK6116N	2K x 8	150, 200, 250ns C
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Full-height 5¹/₄-in. Winchester drives store 760M bytes and seek in 16 msec

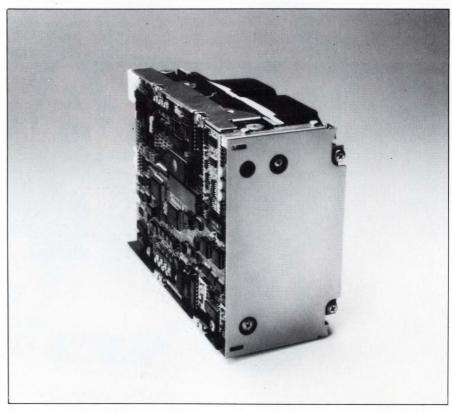
The MK-350 family of 5½-in. Winchester disk drives offer an unformatted storage capacity of 760M bytes. The drives can perform a seek command to data in an average of 16 msec. You can choose a drive with ESDIs (Enhanced Small Device Interface) or SCSIs (Small Computer System Interface). The SCSI drive employs a soft-loaded command set that the company calls "Virtual SCSI."

The MK-358FA ESDI and MK-358FB SCSI drives share the same HDA (head and disk assembly). The HDA includes eight platters; that is, 16 data surfaces. One of the surfaces stores dedicated servo information and the other 15 store data. When designing the drive, the designers also chose to store servo information embedded between each data sector on the drive.

The company believes that the servo scheme, called a hybrid servo, offers performance and reliability. The dedicated servo surface allows the HDA to accurately perform fast seeks. And the embedded servo information allows the drive to make fine tracking adjustments, thus eliminating off-track conditions caused by thermal expansion.

Other key drive features include a track-to-track seek time of 4 msec, a worst-case seek time of 36 msec, and a MTBF of 30,000 hours. The drives have 1632 cylinders, a track density of 1330 tpi, and a recording density of 31,400 bpi. The HDA features a read-channel data rate of 15M bits/sec, and employs sputtered thin-film media and minimonolithic heads.

The MK-358FB drive includes an embedded controller compatible with the SCSI-2 specification. The Virtual SCSI controller includes no



Based on a dedicated and embedded servo-scheme combination, the MK-358 family of disk drives includes ESDI and SCSI models that store 760M butes.

command set in EPROM. Instead, on power-up the controller loads a command set stored on the disk into RAM.

The soft command set offers several advantages compared with more traditional EPROM-resident command sets. For example, you can download firmware updates from a floppy disk in the field. Furthermore, the company has implemented a robust command set for the drive. Because few customers have use for the entire command set, the customer can pick and choose from available commands and create a custom implementation.

The SCSI controller can decode any command in less than 1 msec.

The controller also includes a 64k-byte, 3-track read-ahead cache. Firmware implements zero-latency reads and writes, and the controller transfers data at 1.5M bytes/sec in asynchronous mode and 5M bytes/sec in synchronous mode.

The MK-358FA ESDI costs \$2495; the MK-358FB SCSI sells for \$2645 (1000). You can expect samples of the drives around midyear.—*Maury Wright*

Toshiba America Inc, 9740 Irvine Blvd, Irvine, CA 92718. Phone (714) 380-3000. FAX 714-583-3133. TLX 183812.

Circle No 730

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➤ VALIDATE/Soft-Scope is a complete in-circuit source level debugger that shows variables, data structures and assembly instructions	V,	
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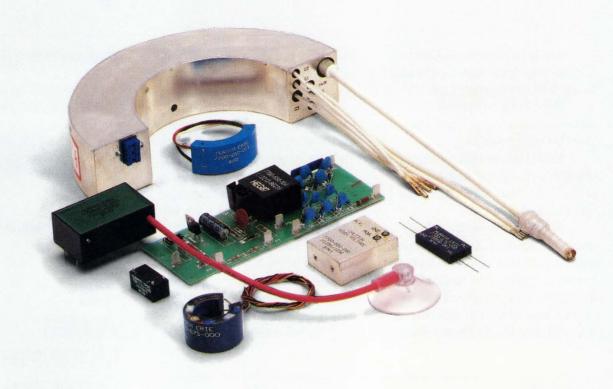




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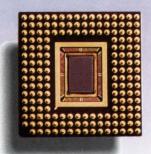
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EDN SPECIAL REPORT

User-programmable GATE ARRAYS



The first generation of programmable logic devices (PLDs) allowed you to vacuum up five or 10 TTL devices into one package. The latest programmable devices, FPGAs, can replace many more TTL devices.

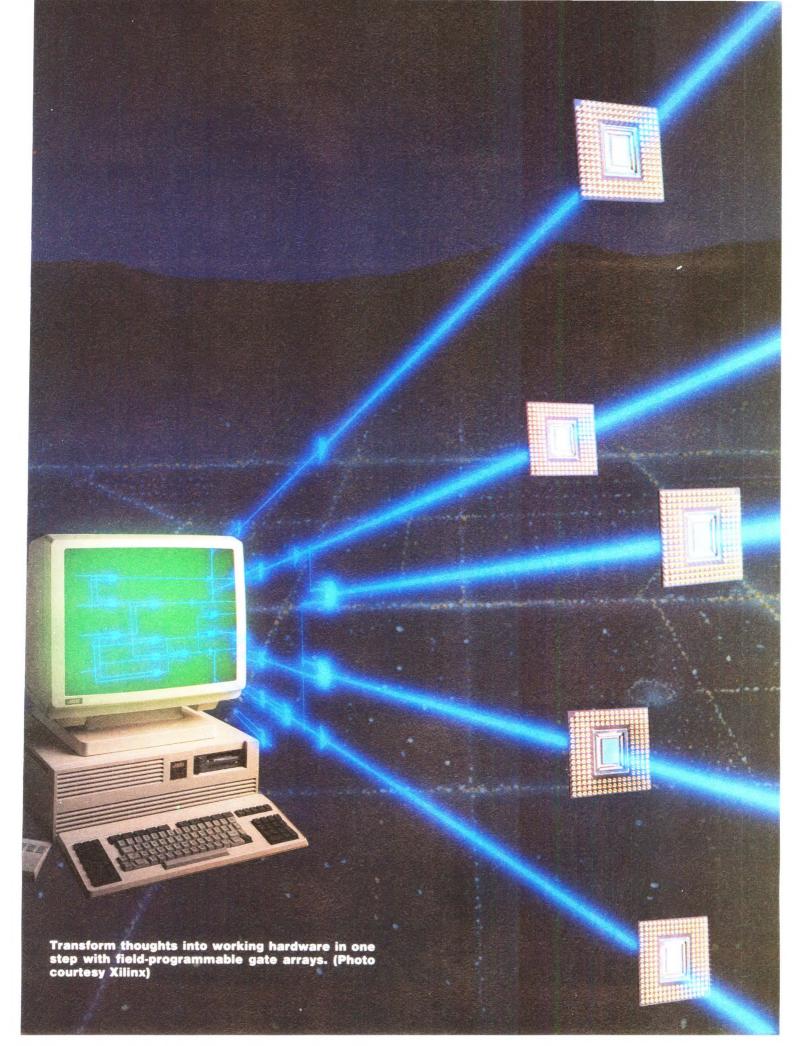
Charles H Small, Associate Editor

S

ome of the latest programmable logic devices (PLDs) are so large that they can replace small mask-programmed gate arrays. Consequently, engineers are calling these new devices "field-programmable gate arrays" (FPGAs), despite the fact that the name ignores a few problems. First, the abbreviation "FPGA" is too similar to the established one for pin-grid arrays (PGA). Second, although the FPGAs share a common application area with factory-programmed gate arrays, on the whole, the FPGAs from different manufacturers bear little resemblance to each other. And, among other things, FPGAs bear no resemblance whatsoever to mask-programmed gate arrays. Fig 1 shows a

portion of a conventional mask-programmed gate array; keep its structure in mind as you examine the architecture of FPGAs in the course of this article.

No matter what you call them, you should have no problem deciding to consider these FPGAs for your next design. A glance at the sparsely populated pc boards in Figs 2a and 2b should provide all the motivation you need. Consider not only that you can pack a lot of logic into these devices but also that you can program these devices right on your lab bench. Programming FPGAs in your lab means that you don't have to pay the large, up-front, nonrecurring engineering (NRE) costs—or suffer the long turn-around times—as-



Although the FPGAs share a common application area with factory-programmed gate arrays, they bear little resemblance to each other.

sociated with custom ASICs such as mask-programmed gate arrays.

You'll actually confront only two barriers to adopting these devices: their high cost per gate compared with mask-programmed gate arrays, and the effort you must make to understand these new devices and master their new design techniques.

If you recall the wide variety of divergent design approaches taken by early automobile and airplane designers, you won't be surprised to find that the new, large FPGAs employ wildly different architectures, processing technologies, and programming methods. This field is in its infancy, and chip designers will surely continue to explore innovative approaches for some time before FPGAs settle down and mature into a few industry-standard types.

Right now, you can get FPGAs from Xilinx, Altera, Actel, and Signetics. (Despite unsubstantiated stories in the rumor-mongering segment of the electronics trade press, Plessey insists it will have no FPGAs until next year.) Each company's products exemplify a fascinating, unique approach to providing you with a blank slate upon which you can inscribe your logic.

Programmable devices intrude

Xilinx was the first company to make a device large enough to start nipping at the heels of mask-programmed gate arrays. Advanced Micro Devices is an alternate source for Xilinx devices; the company has also added AMD-designed versions of Xilinx parts that have "toggle rates" of 100 MHz instead of the 70-MHz toggle rates of Xilinx's original parts.

Beware: Toggle rate is one of those specs, like MIPS or calculated MTBF specs for power supplies, that everyone touts but that mean little or nothing. The toggle rate of an FPGA's logic elements would be a useful spec only if your design simply spins its wheels, clocking the logic at full speed, but not actually processing any inputs or generating any outputs. In systems doing useful work, FPGAs actually run at some fraction of their toggle rate—typically around 60%.

Similarly, you should be aware that the term "gate count" is a holdover from conventional, mask-programmed gate arrays. The gate count refers to the total number of 2-input NAND gates that would be required to realize a logic function. Because a mask-programmed gate array is, in fact, a sea of uncommitted gates, the gate count provides an exact measure of the device's capacity.

FPGAs, on the other hand, are generally not a sea

of uncommitted gates. FPGA manufacturers base their gate counts upon how large a design will fit into both a given FPGA chip and a mask-programmed gate array. In other words, if the FPGA can hold a design that also fits into a 2000-gate mask-programmed gate array, the manufacturer claims that the product is a "2000-gate-equivalent" device. The accuracy of the gate-equivalency measure depends heavily on the nature of the circuits used for comparison and the percentage of utilization of the FPGA.

Xilinx calls its FPGAs "logic-cell arrays" (LCAs). The name is apt because a rectangular, 2-dimensional array of programmable logic blocks—called, for no good reason, *configurable* logic blocks—occupies the bulk of the interior of Xilinx devices (Fig 3). A protective phalanx (hollow square) of I/O cells comes between the programmable logic blocks and the outside world.

Connecting the I/O blocks to the logic blocks and the logic blocks to each other is an elaborate network of programmable interconnection lines. These intercon-

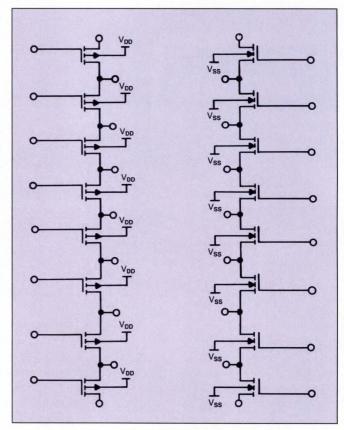


Fig 1—The architecture of a typical mask-programmed gate array bears little resemblance to any field-programmable gate array (FPGA).

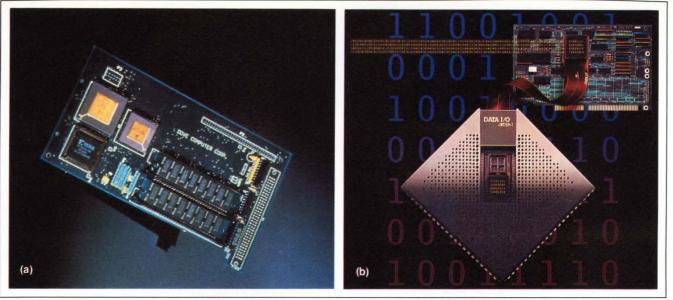


Fig 2—This accelerator board for the Macintosh (a) (from the Dove Computer Co, Wilmington, NC) has a 68030 μ P and companion floating-point processor, some bus drivers, and only a single Xilinx FPGA, which contains all the board's logic. The Data I/O Mesa I in (b) is an in-circuit emulator for Xilinx devices that uses 12 such devices for all its logic functions.

nection lines form a waffle-like pattern in whose interstices the logic blocks reside. At the intersections of the interconnection lines lies a sort of crossbar switch. Although some global long lines bypass these programmable crossbar switches, the bulk of the interconnection lines must go through the crossbar switch. Note that these crossbar switches get programmed only once, when the device is initialized; you don't switch them dynamically as you would a real crossbar switch in a telephone exchange.

Tie lines from the logic blocks and I/O blocks tap into these interconnection lines. You route signals around the device by threading them from one interconnection line to another via the switches.

Xilinx's parts have two types of logic blocks. The original XC2018 and XC2064 have 100 and 64 logic blocks, respectively. These devices' logic blocks have a single flip-flop and enough associated logic elements so that you can program them to execute any Boolean function of four variables. The XC3090 has 320 logic blocks, each of which contains two flip-flops and can execute two 4-input Boolean functions or one 5-input function. For all Xylinx devices, you need not use the flip-flops in the logic blocks; you can bypass the flipflops to achieve combinational functions as well as registered ones. The parts' gate-equivalency figures range from 1200 gate equivalents for the XC2064 to 9000 gate equivalents for the XC3090. For the same range of devices in the lowest cost packages, the prices are \$11.25 to \$135 (1000). AMD offers the 1200-gateequivalent Am2064 for \$21.44 (100), the 1800-gateequivalent Am2018 for \$32.50 (100), and the 2000-gateequivalent Am3020 for \$42 (100).

Timing specs for FPGAs vary widely—some are easy to calculate, some are difficult. Because of the nature of the programmable interconnection lines, the timing specs for Xilinx's devices depend heavily on the layout.

The Max family is Altera's (Intel and Cypress Semiconductor are alternate sources) answer to some of the problems that chip designers encountered when they tried to enlarge the scale of the now-familiar PAL-device architecture. The basic PAL-device architecture suffers from a lack of flexibility and a tendency to underutilize its internal logic elements. The UV-erasable Max family currently consists only of the 500-to 1250-gate-equivalent EPM5032 (which costs \$30 in

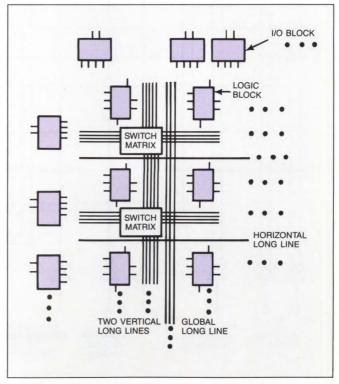


Fig 3—These FPGAs feature programmable logic blocks embedded in a matrix of programmable and fixed interconnection lines. A ring of programmable I/O blocks lines the periphery of the device, which hails from Xilinx.

Only two barriers really exist to adopting FPGAs: their high cost and the effort needed to understand both these new devices and their new design techniques.

sample quantities and \$24 in quantities of 1000) and the 2000- to 5000-gate-equivalent EPM5128 (which sells for \$111 in sample quantities and \$90 in quantities of 1000), but other members are currently gestating. The Max family retains the programmable-AND/fixed-OR structure of conventional PAL devices—with a couple of twists (Fig 4).

First, a Max device's external inputs link to a programmable matrix of interconnection lines that Altera calls the PIA (programmable interconnect array). This interconnection array is, in effect, a crosspoint switch

for linking any input on the chip, whether external or internal, to any output.

Internal inputs to the interconnection array include feedback lines from the chip's macrocells and feedback from programmable I/O lines. The feedback from the chip's macrocells allows you to use a macrocell's I/O pin as an input and simultaneously use its flip-flop as a buried register.

Outputs from the interconnection array go, naturally enough for a PAL-like device, to the AND/OR and XOR minterms that feed the registers in the chip's

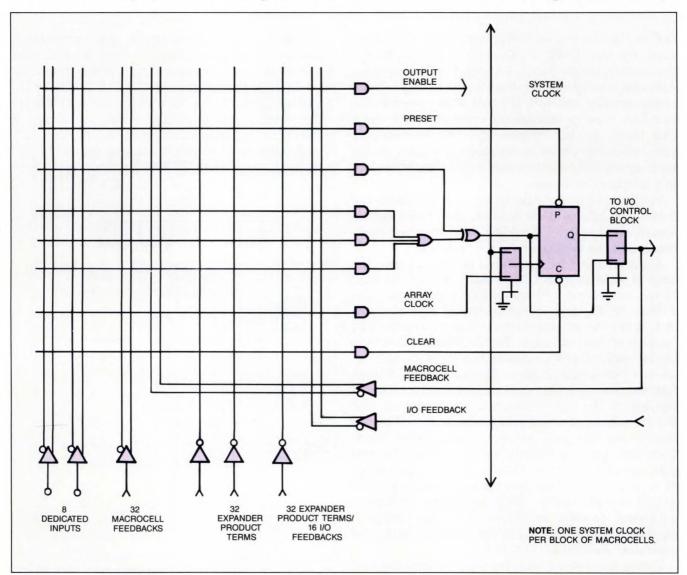


Fig 4—The Max family devices from Altera contain blocks of macrocells linked by an interconnection array. Note that each macrocell has only three dedicated AND gates; for minterms with more than three AND gates, you link in uncommitted AND gates from the expander-product array.

macrocells. Other outputs from the interconnection array handle housekeeping functions for the macrocells, functions such as output enable, preset and clear, and clock.

The chip's macrocells, as is common with advanced CMOS PLDs, have flip-flops that you can program to be one of five types: D, T, J-K, S-R, and D with enable. Note that some advanced PLDs have 8 or 12 programmable register types.

So far, the Max family appears to differ little, in principle, from advanced PLDs such as the 22V10 or the 39V18. However, a close inspection of the diagram of the devices' architecture discloses a surprising fact: Each macrocell's AND/OR minterm has only three AND gates; PAL devices traditionally have eight AND gates or more per minterm.

Altera explains this surprising paucity of AND gates by claiming that the company's research shows that the vast majority of PAL-device designs use three or fewer AND gates per minterm—leaving five or more AND gates unused in PAL devices. However, you will not be left in the lurch if your Max-family design calls for more than three AND gates per minterm. Lurking in the heart of a Max device is a sea of uncommitted AND gates (the EPM5032 has 64 such gates), which gives the Max device a hint of the flavor of a programmable gate array. Altera calls these gates the "expander array" or "expander terms."

These expander-array gates' inputs and outputs communicate with the same interconnection array that links all the other elements of the device. Thus, at the cost of some extra delay, you can selectively add AND gates to any macrocell's AND/OR array. If you don't need some or all of the uncommitted AND gates, you can cross-connect pairs of them to form extra registers.

The underutilization bugaboo departs

Altera hopes that the expander array of uncommitted AND gates will solve the biggest bugaboo of PAL-type devices: underutilization of gates. Designs that require considerable conditioning or qualifying logic to precede registers tend to use a significant portion of a PAL device's AND/OR array. On the other hand, register-intensive logic elements, such as counters, tend to use up PAL devices' registers long before they make a dent in the available AND/OR resources.

When designing the Max devices, Altera strove to make all the paths through the chips the same length. Thus, you can easily calculate a Max chip's timing. The delay through the chip is fixed at one of two values;

which value it is depends on whether you use the expander array or not.

Actel makes no bones about the nature of its devices; the company calls them desktop-configurable gate arrays. (Presumably, the company means you can configure its FPGAs *on* your desktop, not configure them *as* a desktop.)

The architecture of Actel's ACT family (Texas Instruments is an alternate source) resembles that of a medieval castle (**Fig 5**). The company offers the 1200-gate-equivalent ACT1010 for \$62 (in sample quantities) and \$45 (1000), and the 2000-gate-equivalent ACT1020 for \$109 (in sample quantities) and \$80 (1000). A ring of I/O cells lines each chip's outer perimeter. Inside lie rows of logic-block cells separated by horizontal rows of interconnection lines. Each logic block has eight inputs and one output. You can program a logic block to function as multiplexers and D flip-flops as well as a subset of common 2-, 3-, and 4-input logic gates. Other common logic elements require two or more logic blocks.

The logic blocks' input and output lines run vertically, at right angles to the interconnection lines. At each intersection of a logic block's input or output line and an interconnection line is a unique, one-time-programmable "antifuse."

Like PROMs, conventional fuse-programmed PLDs come with all the possible connections made. You program these devices by blowing fuse links and opening up connections you *don't* want. In contrast, Actel's parts come with all connections open and you blow the

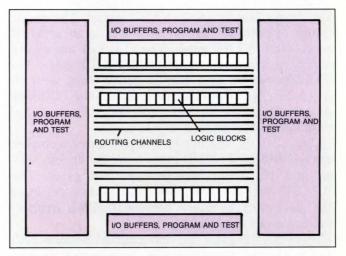


Fig 5—Rows of programmable logic blocks are separated by horizontal routing channels in these FPGAs from Actel. I/O buffers encircle the logic-block array.

FPGA chip designers are sure to continue to explore innovative approaches for some time before FPGAs settle down and mature into a few industry-standard types.

insulation between any two lines you do want to connect.

The distinction between fuses and antifuses is pretty much academic for all users except device-programmer designers. The key spec for antifuses that matters to most users is their small size. An antifuse is 50 times smaller than a RAM cell and 10 times smaller than an EPROM cell—both of which are programming elements in other FPGAs. The small size of Actel's programming element allows the company to put more programming elements on a chip—by an order of magnitude—than their competition does.

The timing specs of a design realized in an Actel device are obviously layout dependent. However, the firm has enough confidence in its layout software's ability to pack the logic together, and in the speed of its interconnection lines, that it has factored in interconnection delays in the specs for its gate delays.

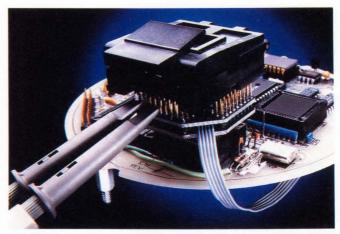
Sea of gates

The Signetics PML devices (programmable macro logic) come in two versions, the PLHS501 and the PLHS502. These fuse-programmed, bipolar devices are based on a variation of the same basic principle of Boolean logic that animates PAL-device PLDs. Conventional PAL devices have a 2-level AND/OR architecture, because once you cast your logic equations in canonical, sum-of-products form, you can realize any logic function with a combination of AND and OR gates. The PML devices embody a variation of that basic axiom and use NAND gates instead (Fig 6).

Further, the PML devices' NAND gates do not come in a fixed, 2-level NAND/NAND array. The major feature of both devices' architectures is an array of uncommitted NAND gates. The PLHS501 has an uncommitted array, or "sea," of 72 NAND gates; the PLHS502 has 64 such NAND gates, along with 16 buried flip-flops. Note that even though the PLHS501 has only 72 gates, its gate-equivalency figure is approximately 1800 gates.

Along with the uncommitted NAND gates, a smaller array of dedicated NAND gates feeds the devices' output pins via either inverters or XOR gates. The PLHS502 costs \$14 (1000). You can expect to see larger PML devices in the future, because the PML architecture can easily be scaled up.

These NAND gates are uncommitted because both their inputs and outputs connect—along with the external inputs—to the same interconnection array. Thus, you can loop any gate's output back into the intercon-



This utility meter takes advantage of the built-in diagnostic feature of Actel's ACT1020 to simplify testing.

nection array and use it as an input to another gate or gates. With this flexibility, you can create many-layered logic functions. Logic designs for PML devices often resemble the equivalent circuits printed in TTL manuals.

PML timing specs are straightforward to compute. You simply calculate a fixed delay for input and output gates plus another fixed delay for every layer of NAND gates that your logic uses.

Will your design fit?

The preceding quick tour of the architectures of the new FPGAs only hints at their complexity. Without doing a complete, detailed design and simulation, you can't be absolutly sure that your design will fit into and run fast enough in a given FPGA.

You can, however, get a rough idea by first counting up the total number of inputs and outputs your design requires and then consulting each company's library of preprogrammed logic functions (macros). Matching your design's logic functions to the functions in the manufacturer's macro library will give you a rough count of the number of logic elements your design will consume, because the manufacturers list the number of such elements that each of their macros uses.

Although the areas of application for all these devices overlap, each device suits some application areas better than others. For example, the Signetics PML has only 72 uncommitted gates—far less logic than the many, more-powerful logic blocks in the Xilinx and Actel devices. Yet each PML gate can accept as many as 32 external and 72 internal inputs; the logic blocks accept only a few inputs each. Thus, the PML can easily han-

dle decoding jobs in 32-bit systems that would exhaust the other devices' resources.

Or take the Altera Max devices. Like their PAL-device forebears, they have dedicated registers for only their outputs. By contrast, the Xilinx and Actel devices have a plentiful supply of registers. But the Max devices have a dense, populous AND/OR array feeding their registers. Therefore, Max devices suit designs, such as state machines, that require considerable conditioning of inputs prior to registering. Registerintensive applications such as counters breeze into Actel and Xilinx parts.

Onboard programming opens up options

The programming technology these devices employ can affect your product-development and productiontesting practices in fairly obvious ways. What's not so obvious is how the programming methods can affect your design itself.

Actel's and Signetics' devices are fuse-programmed,

which means, obviously, you have to use the "blowand-go" method to verify a prototype of your design. Also, fuse-programmed parts present an obvious and well-known challenge to your testing department, which won't be able to check out the parts until they're programmed.

Note that Actel devices have special pins that you can program to sample the state of any node in the chip. Actel devices need these test probes because the chip is so large that many possible failures could occur at internal nodes not visible at the chip's outputs.

Experienced μP users will be able to roll their incircuit-emulator prototyping skills over only to the Xilinx devices. Both Xilinx and Data I/O offer in-circuit emulators for Xilinx devices. (Data I/O's \$9390 Mesa I is a testimonial to Xilinx devices; the unit uses 12 Xilinx devices internally.)

In practice, the Mesa I provides a "shadow" device that responds to inputs just as your target-system device does. The shadow device, however, does not need

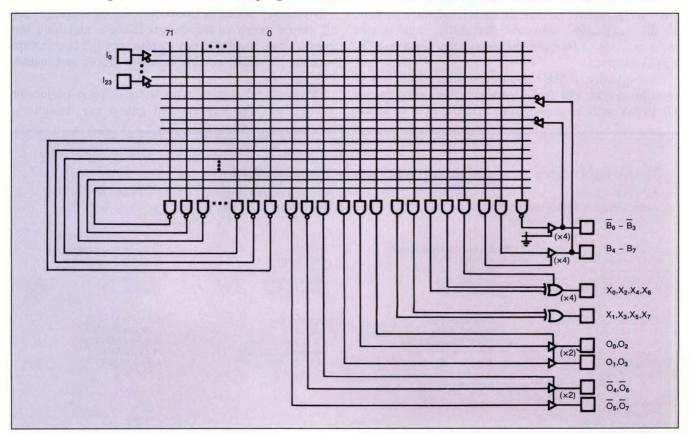


Fig 6—The PML features a sea of uncommitted NAND gates. The inputs to each uncommitted NAND gate are 24 bipolar chip inputs, 72 feedback lines from all of the uncommitted NAND gates' outputs, and eight bipolar output-feedback terms. The wide gates and the feedback array allow you to set up complex, multiple-level logic circuits. The product is available from Signetics.

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The accuracy of the gate-equivalency measure depends heavily on the nature of the circuits used for comparison and the percentage of utilization of the FPGA.

to have the same output structure as the target-system device does, because it has no function in the target system. Therefore, you can program the shadow device's outputs to connect to any node in the device. The Mesa I does not record any of the shadow device's inputs or outputs. To perform that task, you must add your logic analyzer.

Altera's UV-erasable parts, on the other hand, allow you to reuse devices during the development phase of your design. Similarly, Xilinx's RAM-based programming links have to be initialized at least at each power-up. Because these devices are reusable, the factories can program a variety of test patterns into the devices and test them before shipping.

Less obviously, you could employ Xilinx devices' RAM-based programming in a number of novel ways. For example, you could store several configurations in memory and load whichever version suits your customers' applications. Thus, one pc board could suit several applications. Or your design could load different configurations on the fly under software control, as the application demands. Naturally, your design must be able to tolerate the delay that reloading the FPGA incurs.

Conceptually, if the computer system's logic can be reinitialized at will from memory, there's no reason not to use application programs to declare the structure of a computer system's hardware constructs along with its software constructs. If high-level-language compilers were intelligent enough to set up some common software constructs in programmable hardware, realtime and computationally intensive software could run much faster than it does now.

For example, real-time systems rely on intertask communication, coordination, and synchronization mechanisms such as semaphores, mailboxes, queues, schedulers, and timers. Although you could design custom hardware to accomplish these tasks at high speed, most real-time systems build these constructs entirely in software and thereby sacrifice a considerable amount of operating speed on the altar of flexibility.

When programmable logic is available, a suitable compiler could translate an individual program's definitions of counts, timeouts, pattern matches, semaphores, queues, priority levels, and myriad other constructs into custom, hardwired logic specific to that program.

No matter which of these devices you employ, they all permit much easier design changes and field upgrades. You could do your "white wiring" in software without physically cutting pc-board traces and installing jumpers.

Obviously, designing with these chips is no job for a beginner. For experienced gate-array designers,

Manufacturers of field-programmable gate arrays

For more information on field-programmable gate arrays such as those described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Actel Co 955 E Arques Ave Sunnyvale, CA 94086 (408) 739-1010 Circle No 650

Advanced Micro Devices 901 Thompson Pl Box 3453 Sunnyvale, CA (408) 235-7487 Circle No 651

Altera Co 3525 Monroe St Santa Clara, CA 95051 (408) 984-2800 Circle No 652 Cypress Semiconductor 3901 N First St San Jose, CA 95134 (408) 943-2614 Circle No 653

Data I/O Corp FutureNet Div 10525 Willows Rd NE Box 97046 Redmond, WA 98073 (800) 247-5700 ext 461 Circle No 654 Intel Co 3065 Bowers Ave Santa Clara, CA 95051 (408) 967-8080 Circle No 655

Signetics Co Box 3409 811 E Arques Ave Sunnyvale, CA 94088 (408) 739-7000 Circle No 656 Texas Instruments Box 225012 Dallas, TX 75265 (214) 995-2011 Circle No 657

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Successful designers will learn all the ins and outs of FPGAs and design circuits that take into account all the parts' strengths and weaknesses.

switching to these FPGAs should prove to be no problem. For designers experienced with TTL, PLDs, or μ Ps, the transition could be painful.

Some industry observers, however, claim that the transition to FPGAs need not be painful if designers employ a variation of the Carver-Mead method called the DWBH approach (don't worry—be happy, pronounced "dweeb," also used as a verb, as in "to DWBH something"). Using this approach, you simply lay out your design in any fashion that suits your fancy, without regard for the target device's peculiarities.

Many vendors offer schematic-capture packages that allow you to draw up a design that looks just like the TTL designs you are familiar with. When your design looks good, you submit it to a schematic compiler or so-called "logic synthesizer" (actually, such programs don't synthesize any logic at all; they merely extract Boolean equations from the logic inherent in your circuit diagram).

If your design won't fit the target device when you compile the design, you simply select a larger device and recompile. Similarly, if simulation shows your design to be too slow, you just get a faster version of the target device.

Clearly, the more successful designers will probably learn all the ins and outs of FPGAs and design circuits for them that take into account all the devices' strengths and weaknesses.

Painful transitions

Curiously, an experienced TTL designer would probably have less trouble mastering the Xilinx and Actel devices than the Altera or Signetics devices. Designing with the devices that present an array of programmable logic blocks is like designing with a somewhat retarded set of TTL devices.

Actel and Xilinx publish detailed sets of recommendations concerning which logic functions fit their devices' logic blocks best. For example, a single Actel logic block can implement many—but not all—3-input gates directly and only a handful of 4-input gates directly. Xilinx logic blocks, on the other hand, can easily implement any 4-input function, including a majority gate. If experienced TTL designers restrict their design approaches to these recommended ones wherever possible, they will produce optimal designs that will fit their target devices better than a haphazard design will. Instead of just packing the maximum number of functions into a single chip, designers will strive to use the smallest number of logic elements for a given func-

tion, because the fewer logic elements a design uses, the faster the target device will run.

Experienced PLD designers will feel more at home with the Altera and Signetics devices. In fact, the greater flexibility of these devices in comparison with PAL devices should liberate designers from constraints rather than saddle them with new ones.

CAE-like it or not

Unfortunately, all these chips are so large that they virtually require computer-aided design techniques. Designers who prefer manual methods will finally have to give in and start working on an IBM PC or engineering workstation.

The software for FPGAs ranges in price from nothing to tens of thousands of dollars. The cost of the software will come as no shock to gate-array designers who have been using expensive, powerful software on mainframes for years. PLD designers who are used to free software from PLD vendors will be in for some sticker shock when they price software. Signetics' Snap for its PML devices, for example, costs \$500 to \$1000. Xilinx's XACT costs \$3600 to \$12,000, and Actel's ACT1 costs \$20,000 to \$25,000.

The high price of the software stems from two factors. The first is that the FPGA software is much more complex than PAL-device software. PAL devices contain a relatively small amount of logic and have logically simple internal structures. Thus, PAL-device software can consist of no more than a simple Boolean-equation to fuse-map translator. (More advanced PAL-device software packages are available, but they're not absolutely necessary—especially for experienced designers who don't use a wide variety of PAL devices.)

FPGA software, on the other hand, includes a multitude of different input formats: truth-table, circuit-diagram, waveform, logic-equation, and state-machine formats. Additionally, for the chips having arrays of logic cells, vendors offer autorouters and timing simulators. To give you the benefit of other designers' experience, FPGA packages include macros—or predefined, optimized logic functions that you can plug into your design as building blocks.

An unbeatable price/performance ratio

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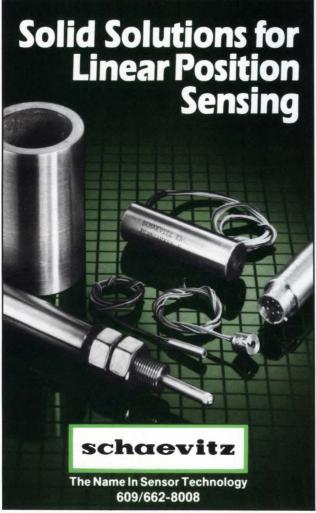
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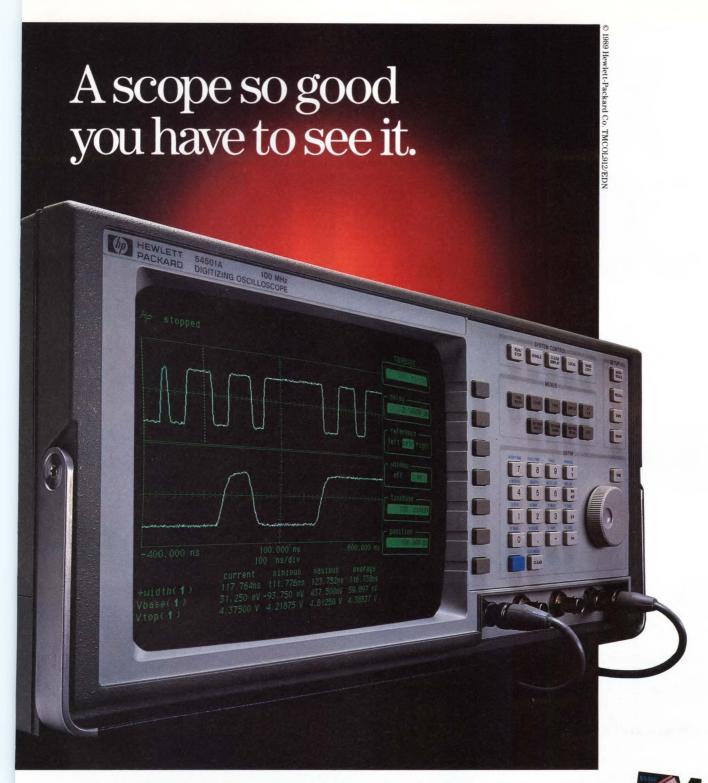
compile designs generated on third-party, schematicentry software packages such as OrCAD/STD or FutureNet, you will have to purchase Signetics' Snap. Snap also provides state-machine entry and macros for common logic functions.

Signetics is not alone in seeing the marketing appeal of using common schematic-capture programs as a front end to logic compilers that suit their particular chips. Xilinx packages Data I/O's FutureNet as a front end to its logic-synthesis, autorouting, and simulation software. Xilinx's back-end software also interfaces with common CAE packages such as Daisy's ACE or DED II, Mentor's Idea, Schema II, OrCAD's SDT, Valid, CASE, PCAD, and ViewLogic.

Similarly, Altera offers Max+Plus software for its Max devices, and Actel has the Action Logic System (ALS) for its programmable gate arrays. The Actel offering also includes an autorouter, which the company claims can route 100% of all paths while using up 95% of a device and a test-software generator.

To understand why this software costs so much, consider that in addition to the much higher software-development costs that FPGA vendors must assume to write such advanced software, recent startups in this field aren't really in the semiconductor business just yet. Right now, these companies are selling more software than hardware and are, rightly speaking, in the software business. If engineers begin to design with these companies' parts and the companies then begin shipping lots of chips, the firms may forsake the software business for the chip business and, as a result, their software prices may come down.

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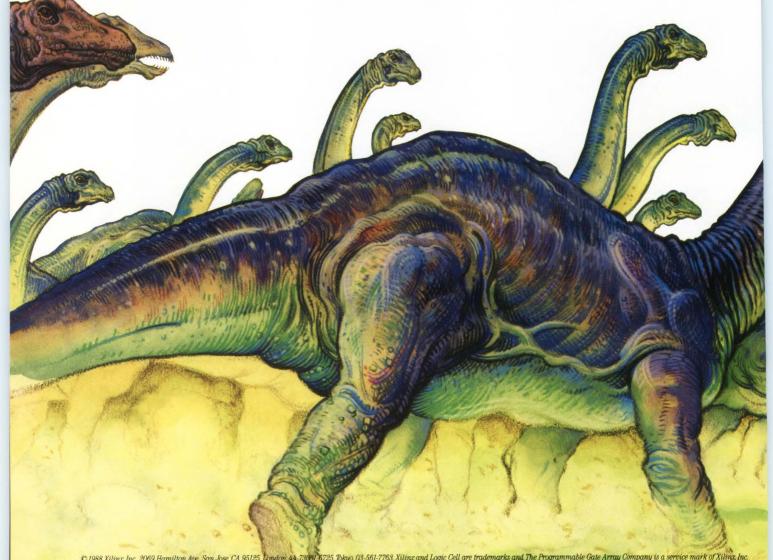
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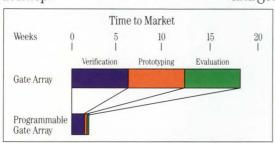


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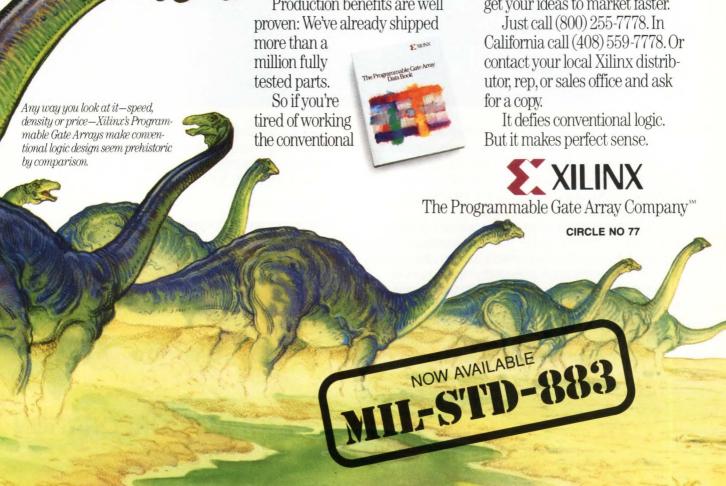
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Design linear circuits that serve digital system needs

Digital circuits require a slew of analog support circuits to provide life support in the real world. Many of these functions are related to memory support and range from power-sense circuits to voltage supplies for programming onboard, nonvolatile memories.

Jim Williams, Linear Technology Corp

The pristine, regimented symmetry of digital circuit boards is occasionally interrupted by irregular huddles of linear components. Designers tolerate these aberrants because they perform a variety of ancillary tasks necessary to keep the digital system running. Most analog designers wouldn't relish lifetime employment working on digital circuit boards, but the need for certain kinds of analog circuits exists. Memory- and power-control circuits are two examples of linear circuits needed in digital systems.

The recently introduced flash memories offer a good example of linear circuits supporting a predominantly digital function. Flash memory, unlike conventional EPROM, lets you erase and reprogram a memory chip electrically. A full-chip erasure takes one second with 100-µsec byte-program times and two seconds for full-

chip programming. (See box, "A primer on flash memory," for a more complete description of flash memory.)

Flash-memory devices require carefully controlled, high-voltage programming power. A typical unit, the Intel 28F010 1M-bit flash memory, specifies V_{PP} pulses of 12 or $12.75\pm0.2V$, depending on the part type. (PP stands for program power.) V_{PP} excursions beyond 14V for 20 nsec or longer will destroy the device. To reliably generate such pulses in a 5V-powered digital system, you must deal with several analog issues. You must derive or supply a high-voltage source and then control its output and the pulses generated from it within the tight tolerances required by the memory device. In addition, you may want to control the high-voltage pulses with a 5V logic command.

Memories require precise programming pulses

A simple way to provide the necessary programming power would be to use an existing high-voltage power-supply line or a switching-regulator output voltage set at the desired V_{PP} level. You could then use a simple, low-resistance FET or bipolar switch to generate the V_{PP} pulses. In theory, this approach will work. In practice, however, transmission-line effects in printed-circuit trace runs may cause memory-destroying overshoots. The $\bf box$, "Preventing memory destruction," details this phenomenon.

In general, you need more sophisticated design techniques to stay within the V_{PP} -pulse tolerance limits. The circuit shown in Fig 1a meets almost all flash-

EDN April 27, 1989

Whichever design world you find yourself in—analog or digital—you should be aware of the linear-circuit needs of different types of digital circuitry.

memory V_{PP} requirements. When the V_{PP} command pulse goes low (**Fig 1b**, trace a), the LT1072 switching regulator drives L_1 , thus producing high voltage at the output. Resistors R_1 and R_2 provide the necessary defeedback; the ac rise and fall times are controlled by the 2-pole compensation of the LT1072. This compensation is set by the values chosen for C_1 , C_2 , and R_3 ; these values have been selected for optimal compensation with respect to this application. The circuit's response should have no overshoot under any conditions including short-circuit recovery (see **Ref 1** for more information on LT1070/LT1072 compensation).

The final output of the circuit is a smoothly rising

 V_{PP} pulse (**Fig 1b**, trace b) that settles to either 12 or 12.75V, depending on the values you choose for R_1 and R_2 . The 5.6V Zener diode permits the output to return to zero volts when the V_{PP} command pulse goes high; you may delete the diode in cases where a 4.5V minimum output is acceptable or desirable. You can eliminate circuit-trimming requirements by using precision resistors for R_1 and R_2 . Alternatively, you can use 1% resistors and a trimmer for R_1 and R_2 .

You can easily modify the circuit of Fig 1a to eliminate the 1N5919 Zener diode and its attendant power dissipation by inserting a pnp transistor in its place as shown in Fig 2a. To further modify the circuit for

A primer on flash memory

Saul Zales, Intel Corp

Flash memories reduce firmwareupdate costs for EPROM-based products. Such products often need software revisions, and EPROMs are costly to update. You often have to dismantle your equipment, either to UV erase and then reprogram the EPROMs or to replace them with new ones. This operation takes a technician at least 15 minutes. Double that time if you wait for UV erasure. In contrast, flash memories allow in-system reprogramming in seconds and are not discarded as EPROMs often are. In the factory, flash EPROMs let you execute multiple tests during a single board-testing step.

To distinguish between EEPROMs and flash EPROMs consider that EEPROMs suit parameter storage, as opposed to code storage. Parameters need to be rewritten individually in real time—that is, while the system is on-line and in normal operation. Parameters also require less memory storage space than code does.

In contrast, flash EPROMs better match embedded-code needs. Even if you only change one line of code, an entirely new microcomputer program results. You must update the software as a complete copy to ensure error-free updating. Flash memories accomplish this process with full-chip erase characteristics in a few seconds of off-line system time.

One flash-EPROM reprogramming method is In-System-Write (ISW). ISW eliminates external programming equipment alto-

gether; it uses an existing data-communication channel, such as a modem. ISW utilizes the embedded, local CPU for the flash-memory device's reprogramming "intelligence," thus taking advantage of the off-line nature of updates. The only new requirement for ISW is a local programming power supply (V_{PP}) of either 12 or 12.75V, depending on device specifications.

The author is an applications engineer at Intel Corp (Santa Clara, CA).

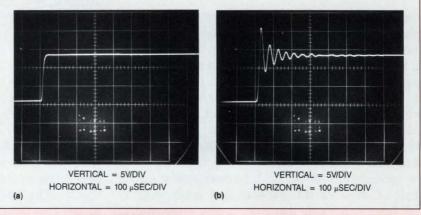


Fig A—An ideal flash EEPROM V_{PP} pulse has a smooth rise time with no overshoot (a). If your pulse-generator design doesn't include circuitry for rise-time control, the pulse can ring at destructive voltages (b) simply due to transmission along a pc trace.

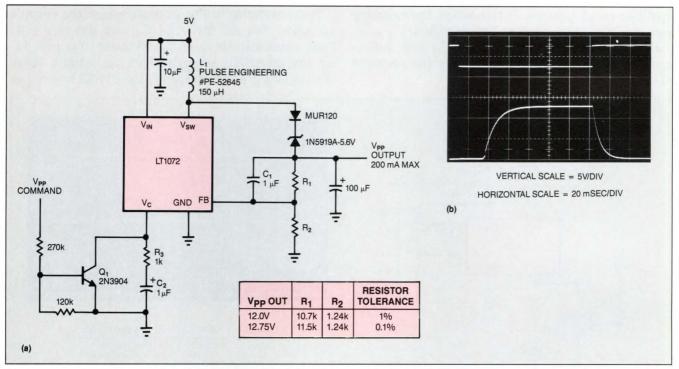


Fig 1—High-voltage pulses with smooth rise characteristics are the basic flash-memory programming requirements that this circuit (a) fulfills. Due to the compensation of the LT1072 switching regulator, the command pulse (b, trace A) produces a pulse with a clean rise-time characteristic (b, trace B).

high power outputs, see the table in Fig 2b.

A key feature of the circuit in Fig 1a and many circuits similar to it is that they will not spuriously overshoot during power-up or power-down, thereby preventing memory destruction. This feature is due to the compensation of the LT1070, which causes a highly overdamped pulse response, and to the fact that the control components of these circuits function even at low supply voltages. In other words, the control circuits will be active long before the memory circuits

settle and will prevent uncontrolled V_{PP} outputs.

The repetition rate of the circuit in Fig 1 is limited because the regulator must fully rise and settle for each V_{PP} command. Depending on how often your memory devices require updating, this limited repetition rate may or may not present a problem. Most requirements are for low repetition rates (from one hertz to the kilohertz range), but there are cases where the pulser is required to serve many memories. The circuit in Fig 3 serves those cases that require higher-

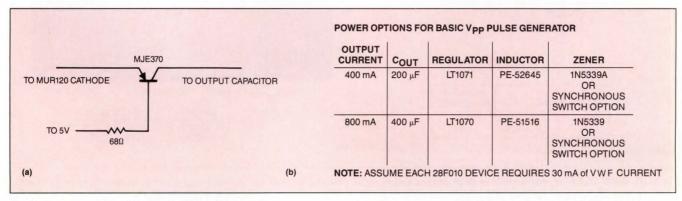


Fig 2—You can replace the Zener diode of Fig 1 with a pnp transistor (a). You can also modify Fig 1 for higher power outputs (b).

Power control and memory management are just two areas where some analog design tricks will come in handy on a digital circuit board.

repetition-rate V_{PP} pulses. In this design, the switching regulator runs continuously. You provide a V_{PP} command pulse to drive an op-amp (IC₁) and buffer-amplifier (IC₂) loop, which generates the required pulses.

The waveforms in Fig 3b demonstrate the circuit's operation. You can drive the V_{PP} lock line to a logic high, which will shut down the regulator, thus preventing any possibility of inadvertent V_{PP} outputs. After the V_{PP} lock goes low (trace A), the LT1072 loop comes

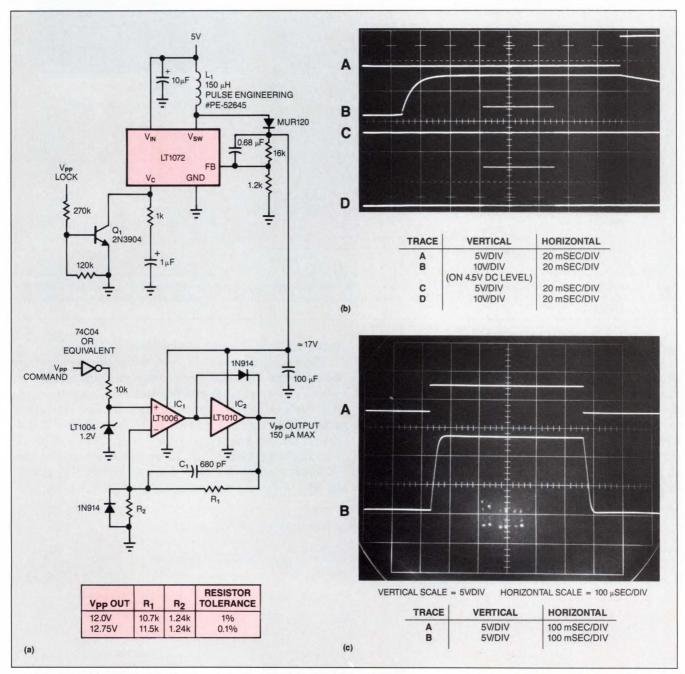


Fig 3—To fulfill higher-repetition-rate voltage-programming requirements, you can run a switching regulator continuously and generate the V_{PP} pulses by using an op amp and a buffer amplifier (a). High-voltage pulses, whose level is dependent on the value you choose for R_1 and R_2 , result from the application of the V_{PP} command pulse (b, trace D); these pulses exhibit clean rise times (c, trace B).

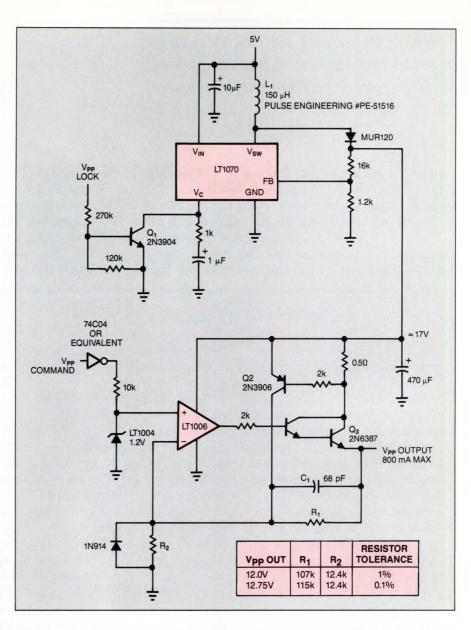


Fig 4—By replacing the buffer-amplifier stage of Fig 3 with a discrete-output stage, you can supply up to 800 mA of output current.

on (trace B), stabilizing at about 17V. Pulsing the V_{PP} command line then causes the 74C04's output (trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V, and the gain loop containing IC₁ and IC₂ produces a pulsed output voltage dependent on the values you choose for R_1 and R_2 (trace D). The 680-pF feedback capacitor, C_1 , controls loop slewing, thereby eliminating overshoots. Fig 3c details the V_{PP} output. Trace A is the 74C04 output; trace B displays the clean V_{PP} -pulse characteristics.

As in Fig 1, the 2-pole compensation of the LT1072 in Fig 3a ensures a clean rise time, and spurious V_{PP} outputs are suppressed during power-up and power-down. The LT1010 buffer amplifier provides short-circuit protection and 150 mA of drive current, which is enough for five 28F010s. The diode path around the LT1010 prevents destructive overshoot when the circuit is recovering from output shorts. The diode at IC_1 's input clips excessive negative voltages arising from C_1 's differentiated response.

To drive more memory devices—supply more output

current—you can modify the circuit in Fig 3a by replacing the LT1010 buffer amplifier with a discrete power stage, as shown in Fig 4. Q_3 furnishes up to 800 mA of output current, enough to drive 26 28F010 memories; Q_2 functions to limit the current to a maximum of approximately 1.2A. The values of the feedback components used in Fig 3a have been scaled by a factor of 10; R_1 and R_2 were increased and C_1 was decreased to maintain the same level of compensation. These changes prevent Q_2 's collector current from causing excessive heating in the grounded resistor, R_2 . This heating could occur during prolonged short-circuit conditions. The ac dynamics of the circuit in Fig 4, including a glitchless short-circuit recovery, are identical to those of the circuit in Fig 3a.

You should note that for both Fig 3a and Fig 4 the LT1070 or LT1072 is running continuously to provide a fixed high voltage. If a suitable high voltage is already available in your system, you can power IC_1 and IC_2 directly from that high-voltage line and delete the regulators from the circuit.

A diode path around the final V_{PP} output stage prevents destructive overshoot when the circuit is recovering from output shorts.

These V_{PP} -generating circuits require waiting a small length of time for the regulator to settle before proceeding with a V_{PP} operation. Note the lag between the V_{PP} command pulse and the rise of the output pulse in Fig 1. In almost all circumstances, this delay is acceptable, but some situations may require verification that the V_{PP} is within a certain tolerance before

the pulsing begins.

When used in conjunction with either V_{PP} pulser, the circuit in Fig 5 gives a handshake output when the V_{PP} has settled. This simple circuit works by comparing the V_{PP} output against the known LT1004 reference voltage. The resistor values given allow for possible variations in V_{PP} voltage due to component tolerance

Preventing memory destruction

The 12 or 12.75V V_{PP} pulses used with flash memories seem uncomfortably close to the devices' 14V breakdown limit. In actuality, the overvoltage precautions required are similar to those for 5V rails. Excursions beyond 14V for durations longer than 20 nsec exceed the chip's absolute maximum rating. Thus, the design of V_{PP}pulse-generating circuitry requires care to avoid seemingly mysterious memory failures. Although the 28F010 flash memory is used here as an example, the considerations are applicable to other devices.

In theory, a simple low-loss transistor switching a low-impedance power supply will generate the required pulses. In practice, this is a hazardous approach. Fig Aa shows an ideal V_{PP} pulse produced by simple transistor switching. The pulse settles to the desired V_{PP} level quickly with no overshoots or aberrations. Fig Ab shows the same pulse measured at the memory pins after a printed-circuit trace run. The pc trace looks like an unterminated transmission line with ill-defined characteristics. Reflections occur, which cause ringing exceeding 20V. This ringing is well beyond specified destructive levels and almost guarantees chip failures. Similar overshooting on the falling edge can cause equally destructive negative voltages to appear at the memory pins.

These effects demonstrate the necessity for rise-time control. The controlled edge times of the closed-loop circuits in the text eliminate this problem. Other features of these circuits make them attractive. Short-circuit protection is obviously desirable to protect the V_{PP}-pulse generator. More subtly, it also protects the memory. In an unprotected V_{PP} pulser, the pass switch may fail in a shorted condition. This failure will expose the memory to destructive overvoltage. You should design short-circuit-protection circuitry so that it does not cause overshoots when operating or recovering from overload.

For example, removing IC₂'s shunt diode from the circuit shown in Fig 3 in the text causes dangerous overshoots on shortcircuit recovery. Fig Ba shows V_{PP} output recovery with the diode removed. With the diode in place (Fig Bb), the recovery is free from overshoot. Similar considerations apply on power-up and power-down. The V_{PP} generator must not produce spurious outputs during power application or removal. You can avoid these unwanted outputs by employing circuit techniques and ICs that operate down to low voltage. Circuits that provide control even when the power supply is not yet at its specified operating level yield predictable and controllable outputs during transient supply conditions.

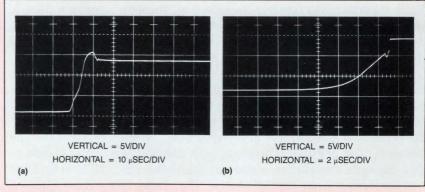


Fig B—Without a shunt diode at the output of a V_{PP} -pulse generator, dangerous memory-destroying overshoots can occur (a). With the diode in place, the recovery is smooth and controlled (b).

stack-up. When you use this circuit, you should set the output of the V_{PP} generator circuit to within 0.4% of nominal value. You can set the output to a precise value by trimming or by using 0.05% resistors in place of the 0.1% values specified.

Although EEPROMs fulfill a different purpose than flash memories, their $V_{\rm PP}$ -pulse requirements have similarities. The Intel 2816 specifies a $V_{\rm PP}$ amplitude of $21\pm1V$ with a maximum allowable voltage of 22.5V. A special EEPROM stipulation is that the $V_{\rm PP}$ -pulse rise time must have an RC time constant very close to 600 $\mu \rm sec$. The circuit in Fig 6 meets these requirements. As in the circuit in Fig 3, an LT1072 switching regulator generates the high supply voltage; an op amp (IC1) and a buffer amplifier (IC2) generate the actual $V_{\rm PP}$ pulse. While the Erase/Write lock line is low (Fig 6b, trace A), the LT1072 is in standby; no high voltage is produced, and there is no circuit activity. Under these conditions, the $V_{\rm PP}$ output line is pulled toward 5V via the 1N914 diode. (Note the 4.5V dc

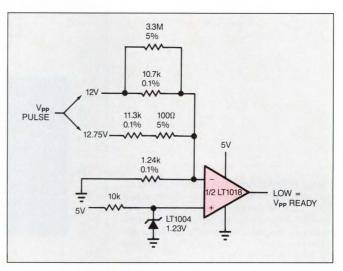


Fig 5—Switching-regulator-based circuits require that you wait a certain length of time for the regulator output to settle before you begin a V_{PP} operation. This simple comparator circuit provides a handshake output when either of these two V_{PP} levels has reached its final value.

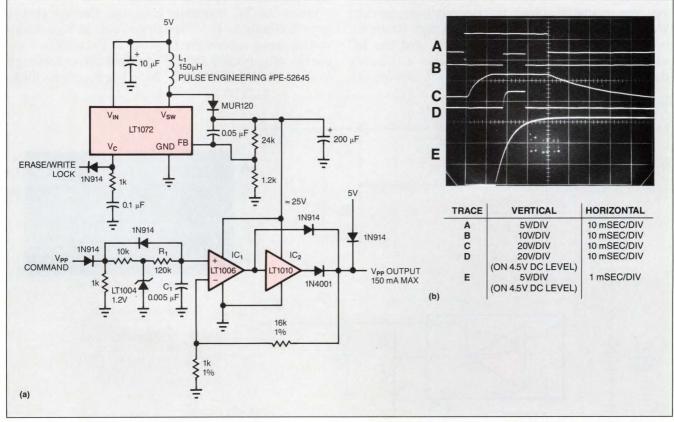


Fig 6—EEPROM high-voltage programming requirements are similar to those of flash memory. EEPROMs require 21V amplitude pulses with RC time constants of 600 μ sec. A simple modification of Fig 3's input (a) provides rise-time control via R_1 and C_1 . By choosing R_1 and C_2 so that their product equals 600 μ sec, the output-pulse conditions are met (b, trace E).

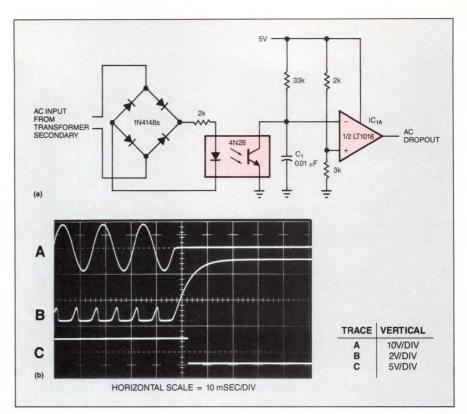


Fig 7—Dropout detection enables you to issue memory-store commands before power fails. This ac detector uses an optoisolator connected across the secondary of a transformer to continually reset C_1 (\boldsymbol{b} , trace B). When power fails, C_1 charges up and triggers the comparator (\boldsymbol{b} , trace C).

level on traces D and E of Fig 6b.)

When the Erase/Write lock line goes high (trace A), the regulator output (trace C) builds smoothly and regulates at 25V. The 2-pole LT1072 compensation allows the regulator output to rise relatively quickly. When the V_{PP} command line is pulsed high (trace B), the LT1004 reference clamps at 1.23V, and the RC network made up of R_3 and C_1 delivers a 600- μ sec edge to IC1's positive input. The feedback-resistor val-

ues chosen produce 21V at the V_{PP} output (trace D). The 21V amplitude is ensured by the LT1004 reference and closed-loop operation. Trace E is a time- and amplitude-expanded version of this pulse.

When the V_{PP} command goes low, the V_{PP} output returns cleanly to 4.5V. The shunt diode at IC₁'s noninverting input speeds the recovery of the 0.005- μ F capacitor. IC₂ provides 150 mA of output current, enough to drive 10 2816 EEPROMs. As in Fig 3, a shunt diode

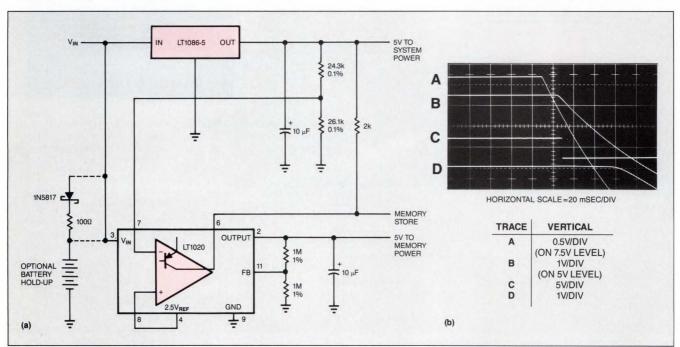


Fig 8—By making use of two 5V dc regulators (a), you can alert the memory section to store data (b, trace C) before the memory power fails (trace D).



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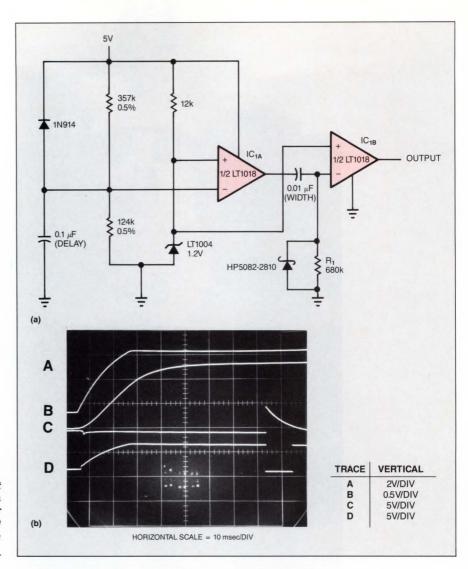


Fig 9—The flexible power-on-reset circuit shown in **a** lets you modify the delay between the power onset and the pulse-onset trigger (**b**, trace C). The circuit also lets you modify the reset pulse-width by changing R_1 and C_1 (**b**, trace D).

around the LT1010 prevents overshoot when the circuit is recovering from output shorts. When the Erase/Write lock line returns low, the regulator's output decays toward zero. As with the other $V_{\rm PP}$ circuits, this design does not produce undesired outputs during power-up or power-down.

Digital systems driven from the ac power line often require dropout detection. You'll want to implement fast ac line dropout detection in order to issue a memory-store command before the dc power falls. The circuit in Fig 7 detects ac dropout by connecting an optoisolator across the power transformer's rectified secondary. Under normal power conditions, the ac line (Fig. 7b, trace A) turns on the LED every 8 msec, or ½ cycle of the line. This repetitive action causes the output transistor to continually discharge the 0.01-µF capacitor (trace B). However, when the ac line drops out, the capacitor charges via the 33-k Ω resistor. IC_{1A} compares the resultant ramp voltage to a 5V supplyderived reference. In this case, the 2-k Ω and 3-k Ω resistors bias IC_{1A} to go low (trace C) within one cycle of ac line dropout.

In many cases, you won't have access to the ac power line. Such cases include PC add-on memory applications and battery-powered systems in which there simply isn't any ac power available. When ac line dropout detection isn't feasible, you'll have to implemement a dc-sensing circuit, such as the one shown in Fig 8a. This circuit uses the different dropout voltages of two regulators. Under normal operating conditions, the LT1086 supplies 5V power to the main system, and the LT1020 drives the memory section.

When the input power falls (Fig 8b, trace A), the LT1086 drops out first (trace B). This voltage change is detected by the LT1020's onboard auxiliary comparator, which then goes low (trace C). This action alerts the memory section to store data. The LT1020 regulator output (trace D) maintains memory power for an additional amount of time due to its low-dropout characteristics. The LT1020's output begins to fall approximately 50 msec after the memory-store command. You can include the optional battery and diode as shown in Fig 8a to extend the holdup time.

In addition to these power-fail circuits, digital systems often require power-up circuitry, such as power-on-reset. When supply power is applied to the circuit in **Fig 9a**, the 5V rail comes up (**Fig 9b**, trace A). The LT1004 clamps at 1.2V, and IC_{1A} 's positive input (trace

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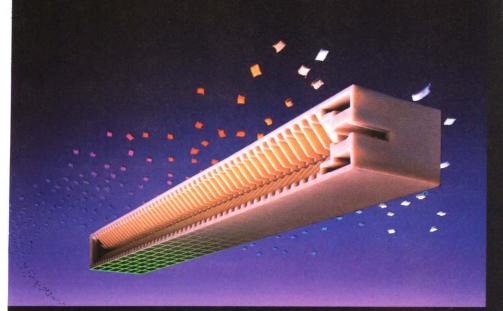
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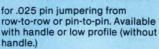
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B) ramps at a time constant determined by the 0.5% resistors and the 0.1- μ F capacitor. When IC_{1A} 's positive input ramps beyond the LT1004 potential, its output goes high, which delivers a differentiated pulse to IC_{1B} 's negative input (trace C). IC_{1B} 's output (trace D) then goes low for a period determined by the differentiator made up of R_1 and C_1 . This pulse is used for system reset.

The 1N914 quickly resets the 0.1-μF delay capacitor, and the Schottky diode clips differentiator-caused negative voltages at IC_{1B}'s input. The ratio of the 0.5% resistors determines the turn-on threshold, in this case 4.8V. The output-pulse delay time—the time at the onset of the pulse in relation to the 5V rail—is controlled by the 0.1-μF capacitor; you can vary the delay time by changing the value of the capacitor. Similarly, the RC combination at IC_{1B} sets the output pulse width and may be similarly varied. As previously discussed, the LT1018's 1.2V minimum supply voltage prevents spurious output during supply power-up.

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



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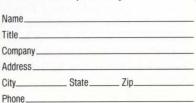




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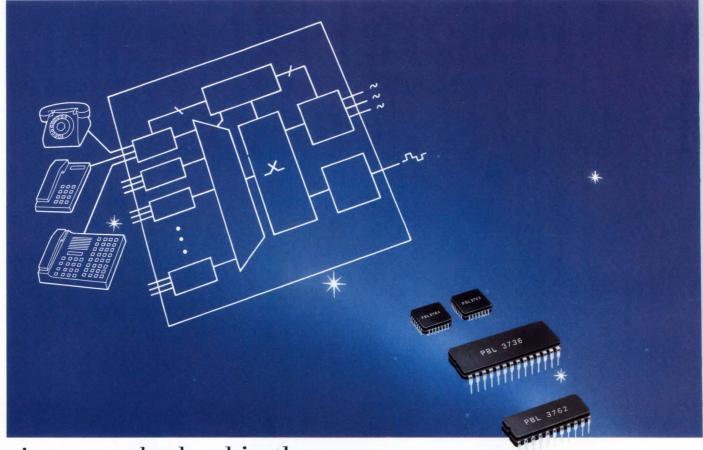
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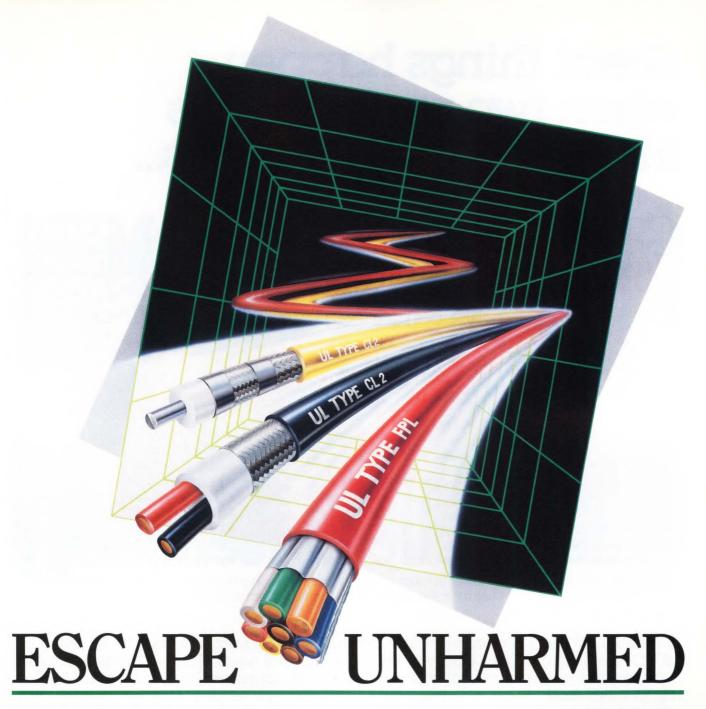
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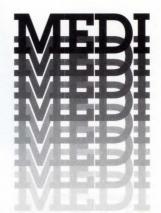
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dyanmic RAMs Part 3

Design a DRAM controller from the top down

To implement a DRAM system, you need a DRAM controller, which acts as a liaison between the CPU and the DRAM. This article, part 3 of a 4-part series, presents the basics of DRAM-controller design. Parts 1 and 2 of this series introduced the fundamentals of DRAMs and the architectural options available to the DRAM-system designer. Part 4 will consider DRAM-board layout.

Robert Adams and Gregory Scavone, Texas Instruments

The heart of any memory system that uses dynamic RAMs (DRAMs) as building blocks is the DRAM controller. The simplest way to design a DRAM controller for your memory system is to perform "top-down" design. To design from the top down, you first consider what tasks the DRAM controller must perform, or, more specifically, what functions the controller must have. You then divide the functions into functional blocks and design or implement each one separately. Finally, you connect the functional blocks and design some circuitry to supervise their interaction.

Essentially, what a DRAM controller does is to coordinate the handshake between the system's CPU (or CPUs) and its DRAMs to facilitate efficient data transfer. The controller is responsible for establishing all of the DRAM's row and column addresses, timing parameters, refresh requirements, and access-mode sequences. A typical DRAM controller consists of a number of functional blocks that are interconnected with

a sequential machine, which performs the supervisory tasks. It is instructive to look at each functional block separately before considering how to interconnect the blocks.

One of the DRAM controller's functions is to accept an N-bit address from a CPU and split it in half to produce a row and a column address for the DRAM. Because DRAMs are configured to accept the row and column addresses on the same pins, the controller requires a block that multiplexes the upper and lower halves of the N-bit input address onto an output address bus. A row- and column-address multiplexer block is shown in Fig 1a.

Some CPUs, such as the Intel 8086 μP , have a multiplexed address/data bus. In order to use these CPUs, you need some external circuitry to latch the address before the CPU can place the data on the bus. On the other hand, many CPUs, such as Motorola's 68000 μP , have separate address and data buses that don't require external latches. One way to handle both these types of CPU is to use transparent external latches.

A transparent latch, such as the one shown in Fig 1b, is a functional controller block whose outputs follow the address inputs when the latch-control signal is low. When the latch-control signal goes high, the latch holds the last address on the input address bus. This configuration can support CPUs with separate address and data buses by simply keeping the latch in its transparent condition. For a CPU with a multiplexed address and data bus, the latch-control signal causes the address to be held while the CPU places the data on the input bus.

Of course, the controller must guarantee that all of

The DRAM controller consists of a number of functional blocks that are interconnected with a sequential machine.

the DRAMs in the memory system are refreshed within the maximum allotted refresh period. The methods of refresh are numerous—RAS-only refresh, burst refresh, RAS-before-CAS refresh, or scrub refresh, to name a few (see part 1 of this series, "Unraveling the intricacies of dynamic RAMs," EDN, March 30, 1989, pg 155). Some refresh methods require more circuitry than others.

The RAS-only and the scrub refresh methods require the largest amount of internal DRAM-controller circuitry. In the RAS-only method, the controller provides a new row address every refresh interval, which is every few microseconds. An N/2-bit counter can easily generate the necessary row-refresh addresses. The outputs from the counter feed the row-and-column multiplexer, which drives the row-refresh address onto the output bus at the refresh interval.

In the scrub refresh method, the controller must generate a row and a column address every refresh interval. You can meet this requirement by extending the counter to N bits. Fig 1c shows the functional blocks that can perform both RAS-only and scrub refresh. When using the scrub refresh method, you shoud use the lower bits of the counter as the row address to ensure that each row is accessed once for each column. Using the lower bits as the row address maintains the refresh interval.

Other refresh methods, such as the RAS-before-CAS method, use an address counter that is internal to the DRAM. Therefore, the controller doesn't require an internal counter, a fact that significantly simplifies the controller's design. In either case, the controller must contain a timer that establishes the start of a refresh cycle.

Address generation and refresh are only part of the controller's functions. The controller must also contain a functional block that interfaces the control signals with the system CPU. To keep the host-interface block modular, you should make sure that the block produces the same output signals, regardless of the variations in the control-signal formats. That way, to accommodate different system CPUs, you only have to alter the interface block.

Systems with multiple CPUs require multiple control-signal interfaces, a fact that further complicates the controller design. With multiple interfaces and one refresh timer, the controller must contain an arbiter, which schedules access request from the CPUs. Fig 2 shows a block diagram of a DRAM controller, including the CPU-interface and arbiter functions.

You'll note that the refresh counter doesn't enter into the arbitration process with the system CPUs. Even though refresh is a valid memory request, the DRAM controller performs the refresh as a top-priority item. Because the controller is responsible for refreshing all of the DRAM cells within the specified refresh period, it treats a refresh as a "super" request that supercedes all other memory requests.

To coordinate the activities within the DRAM controller, the design requires a block that can interconnect the functions. A state machine performs this task efficiently (Fig 3). After executing an initialization sequence, the state machine accepts a request from the arbiter for DRAM access. The state machine controls the multiplexer, via the S_0 and S_1 signals, to place the row address and the column address on the controller's output bus. The state machine also issues a combination of \overline{RAS} , \overline{CAS} , and \overline{WRITE} signals; the particular

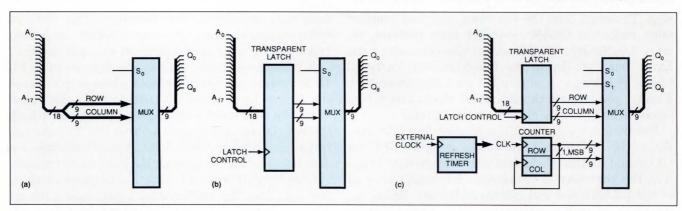


Fig 1—You build a DRAM controller from a number of functional blocks. A multiplexer (a) splits the CPU address into a row and a column address. A transparent latch (b) permits the controller to handle separate and multiplexed address and data lines. A counter/timer (c) generates the refresh addresses at the specified refresh interval.

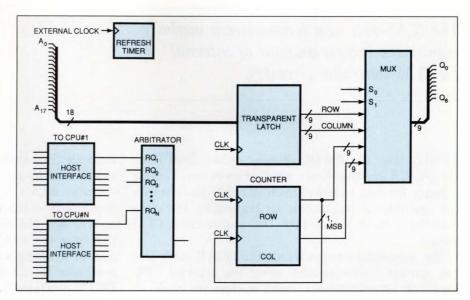


Fig 2—For systems that contain multiple CPUs, the controller requires a host interface for each CPU. The host interface generates and acknowledges the handshake signals. Each interface must connect to an arbitration block, which grants memory access on a priority basis.

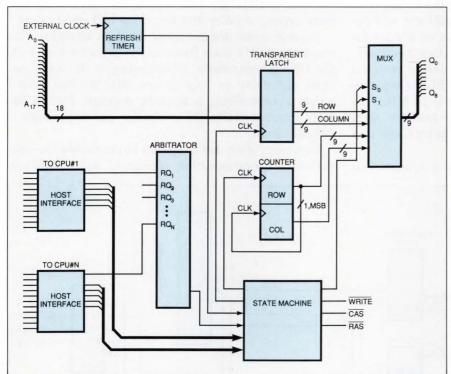


Fig 3—A state machine interconnects all of the DRAM controller's functional blocks, and implements the memory-access modes as well.

combination depends on whether the memory request is for a read, write, or refresh operation.

Finally, the controller should have independent control of several banks of memory. The controller needs separate \overline{RAS} , \overline{CAS} , and \overline{WRITE} lines for each bank in order to achieve this independent control. Fig 4 shows three demultiplexers, which generate four independent DRAM control signals by using the DRAM control signals from the state machine. Two bank-select lines select the individual control signals. The design includes a chip-select line and output-enable signals for the demultiplexers; both these features allow you to use the controller for larger memory systems.

Although the access times of today's DRAMs continue to decrease, DRAMs are often not able to keep up with current high-speed µPs. In such a case, the

 μP must execute wait states while waiting for the DRAM to complete an access cycle or a refresh operation. Wait states are CPU clock cycles during which the μP does nothing. Obviously, a CPU that has fewer wait states will execute a program faster than one that has more. Because the μP does not automatically execute wait states, the DRAM controller must provide an external control signal that indicates when the DRAM is ready.

Within the DRAM controller, the interface block sends a signal to the state machine, through the arbiter, when a CPU desires access to the memory. If the memory is busy, the state machine places the interface block "on hold." Subsequently, the interface block sends a control signal that indicates that the CPU should execute wait states. The 8086 μP uses the

The RAS-only and scrub-refresh methods require the largest amount of internal DRAM-controller circuitry.

 \overline{READY} line; the 680X0 μP uses either \overline{DSACK} or the \overline{DTACK} line to indicate whether an external device is ready for data transfer. Each interface block within the controller is responsible for translating the state machine's Hold signal into the appropriate CPU format.

The sequential circuits within the DRAM controller can operate synchronously, using the external CPU clock, or asynchronously, using a separate clock. A synchronous design is simpler because the timing relationships between the various commands are well defined. In addition, the controller incurs no latency for synchronizing the commands with the clock frequency. Practically, however, a synchronous design restricts the controller to operating at the CPU's clock frequency. If the CPU's clock frequency is 10 MHz, the state machine can't respond any faster than 100 nsec, which can amount to an appreciable percentage of a typical memory-access cycle.

In addition, you virtually can't use a synchronous

controller in a system that has multiple CPUs running at different frequencies. An asynchronous design that operates with a high internal clock frequency overcomes some of the limitations imposed by the synchronous design. You can design an ASIC DRAM controller that operates with a 50-MHz clock frequency, for instance, by using a product such as TI's ASIC DRAM controller ToolKit (see **box**, "ASIC core yields flexible DRAM controller"). In such an ASIC design, the state machine can change states every 20 nsec, using full clock cycles, or every 10 nsec, using half clock cycles.

Asynchronous designs incur inherent latencies. Because the CPU's clock frequency is asynchronous with the DRAM controller's clock frequency, the state machine can delay as long as one DRAM clock period before synchronizing a memory request. With a 50-MHz internal clock, the controller can experience a 20-nsec latency.

Designers often use a pipeline to accelerate the execution of operations that consist of more than one

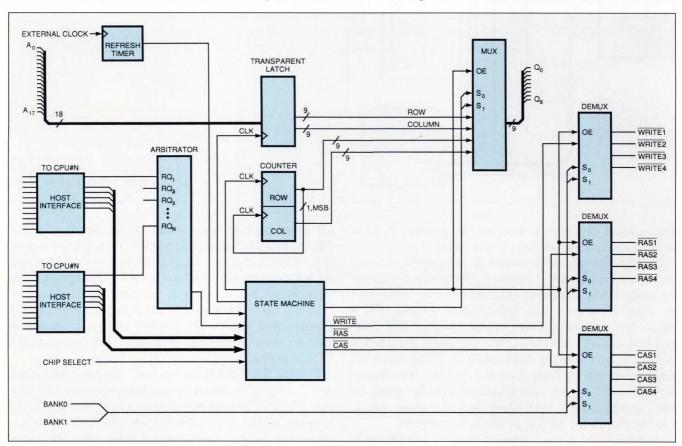


Fig 4—Systems with multiple memory banks require separate \overline{WRITE} , \overline{RAS} , and \overline{CAS} lines for each bank. A series of demultiplexers uses bank-select lines to generate these commands.

ASIC core yields flexible DRAM controller

To build a DRAM controller around an application-specific IC (ASIC) core that can be tailored exactly to a system's needs, you can use TI's ASIC DRAM Controller ToolKit (Fig A). The product consists primarily of predefined functional blocks called SuperMacros. Each SuperMacro comprises 1-µm standard-cell elements, such as gates and buffers. and standard-cell soft macros, such as counters and shift registers. The vendor assembles and compiles these standard cells to form the SuperMacro, a hard macro that the ToolKit user can't alter.

Three types of SuperMacros are included in the kit: host interfaces, an arbiter, and a programmable sequence generator. The ToolKit contains several interface blocks for the major μ Ps, including Intel's 80186, 80286, and 80386 μ Ps, as well as Motorola's 68020 and 68030 μ Ps. The ToolKit also lets you design cus-

TABLE A-DRAM CONTROLLER TOOLKIT MODES

MODE	ARCHITECTURE	RAS- ONLY	CAS- BEFORE- RAS	EDC- SCRUBBING
READ/WRITE	BANK-ORIENTED CAS	YES	YES	YES
	BYTE-ORIENTED CAS	YES	NO	NO
AUTO PAGE	BANK-ORIENTED CAS	YES	YES	YES
	BYTE-ORIENTED CAS	NO	NO	NO
STATIC-COLUMN	BANK-ORIENTED CAS	YES	YES	YES*
	BYTE-ORIENTED CAS	NO	NO	NO

*EDC-SCRUBBING REFRESH MODE CAN BE USED WITH ONLY ONE BANK OF STATIC-COLUMN MEMORY.

tom interfaces by using the company's standard-cell libraries.

The host-interface block generates and acknowledges the handshake signals between the host processor and the DRAM controller. In addition, it generates the enable and direction-control signals for any external bidirectional buffers, if necessary. A single arbitration SuperMacro can accept memory requests from as many as four host interfaces and grant memory access by using a fixed

priority scheme. If there is a single host interface, the arbiter is not required. The programmable sequence generator produces the row and column addresses as well as the WRITE, CAS, and RAS control signals.

Because the sequence generator is programmable, you can design a DRAM controller that can handle a variety of operating modes. By adding a special port to the ASIC, you can design flexibility into the controller. Essentially, you can alter the timing parameters, access modes, and refresh modes during the powerup sequence. An internal delaylocked loop provides a timing resolution as small as 10 nsec when using an external 50-MHz clock. Further, the sequence generator can be programmed externally to handle many of the access modes and refresh methods described in this series. Table A lists some of the modes supported by the tool kit.

In order to design an ASIC DRAM controller, you need an engineering workstation for wiring the SuperMacros together. After this step, you can add whatever customization is necessary to complete the design. Finally, you should simulate the controller design at the workstation before submitting it to the vendor for final approval and fabrication.

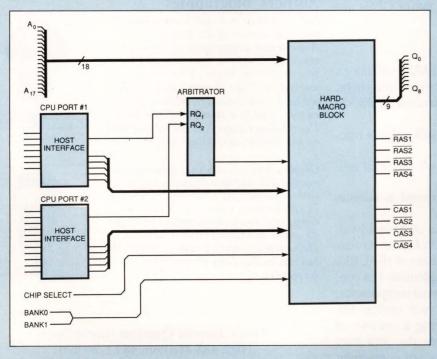


Fig A—A number of interconnected SuperMacros compose the ASIC DRAM Controller ToolKit. The hard-macro block contains the input latch, the refresh timer and counter, the row- and column-address multiplexer, and the state machine, none of which can be physically altered by the user.

EDN April 27, 1989

The DRAM controller can take advantage of pipelining by latching the address and data early in the access cycle.

stage. The stages pass sequentially through the pipeline, a process that makes the execution of certain tasks overlap. The DRAM controller can take advantage of pipelining by latching the address and data early in the access cycle. Thus, the CPU or the memory is available for other operations before the cycle is complete. Using a pipeline in a DRAM-controller design is sometimes called the "latch-and-go" technique.

During a latch-and-go write cycle, the DRAM controller latches the address and data from the CPU as soon as they are available. The controller then sends a command that fools the CPU into believing that the write cycle is over. Subsequently, the CPU can release its I/O bus (or buses) and initiate the next operation while the DRAM controller completes the write cycle. The latch-and-go technique can significantly reduce the number of CPU wait states incurred during write operations to slow memory devices.

During a latch-and-go read cycle, the controller latches the CPU address and the data from the memory as soon as the DRAM's output data is valid. This arrangement is particularly useful in systems with multiple CPUs. Essentially, the technique permits slower CPUs to read the latched data while faster CPUs are accessing the memory.

Three ways to obtain controllers

Now that you're aware of the DRAM controller's functions, you must decide how to implement them. You can choose one of three methods to obtain a DRAM controller:

- Buy an off-the-shelf DRAM controller that's compatible with a specific CPU
- Design a DRAM controller from off-the-shelf controller subassemblies
- Design a DRAM controller around a custom ASIC.

An off-the-shelf component has some obvious advantages. Most CPU vendors offer a DRAM controller that is compatible with the signal formats of the CPUs they manufacture. You can usually implement the controller design by using only a few external components, such as 3-state buffers. However, if your system has special requirements, such as servicing a variety of CPUs that have different signal formats, you may spend more time trying to get a standard component to meet all the system requirements than you would if you designed the controller from scratch.

Using off-the-shelf controller subassemblies gives you a wider choice of controller design. IC vendors sell a variety of LSI devices that perform specific DRAM-controller functions. Some of these subassemblies include refresh timers, address and refresh multiplexers, programmable state machines, and page-mode address comparators. Of course, the disadvantage of this approach to controller design is that you need more components than the off-the-shelf method requires.

The custom ASIC design combines the advantages of a single VLSI component with the advantages of using predesigned controller subassemblies. For example, TI's ASIC DRAM Controller ToolKit lets you build a controller that incorporates a "hard macro" containing the state machine, the refresh counters, input latches, and the output multiplexer. The hard macro is a functional block designed and laid out by the vendor; you can't modify it. Therefore, you can be sure that the critical timing relationships for these modules are correct and will remain unchanged. It's up to you to design in the rest of the controller enhancements for your particular application.

Authors' biographies

Robert Adams is a systems engineer for the CAE branch of the Engineering Automation Department of Texas Instruments' Defense System and Electronics Group (Plano, TX). He has worked for TI for 10 years. Bob obtained a BSEE from Southern Methodist University, and is a member of Tau Beta Pi and Etta Kappa Nu. He lists softball as his chief leisure-time interest.

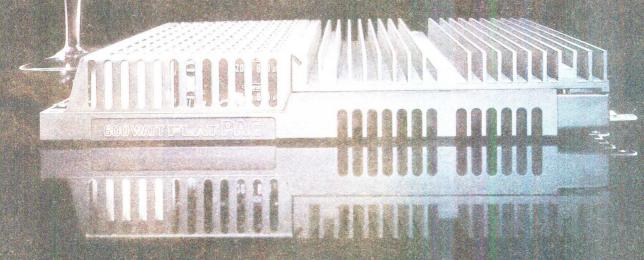


Gregory Scavone is also a systems engineer in TI's Defense Systems and Electronics Group. He's currently occupied in validating a CAE system for EEs. Greg, who has been employed at TI for 10 years, graduated from Southern Methodist University with a BSEE. He belongs to Tau Beta Pi and Etta Kappa Nu.

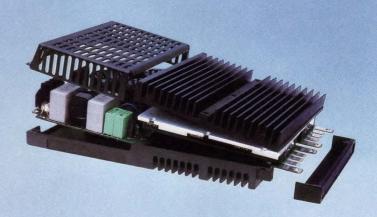


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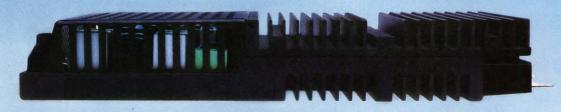
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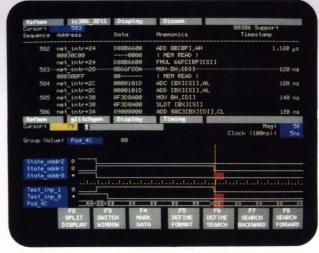
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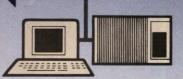
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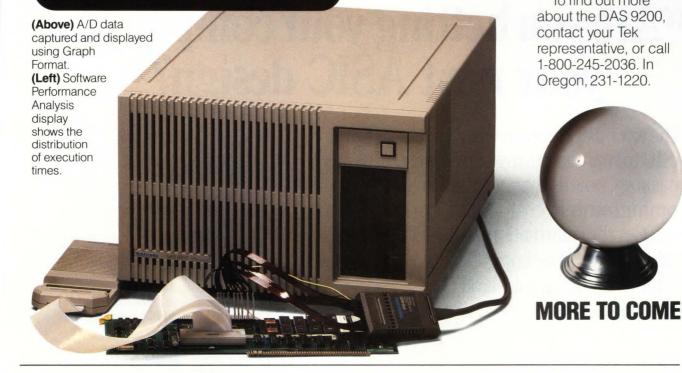
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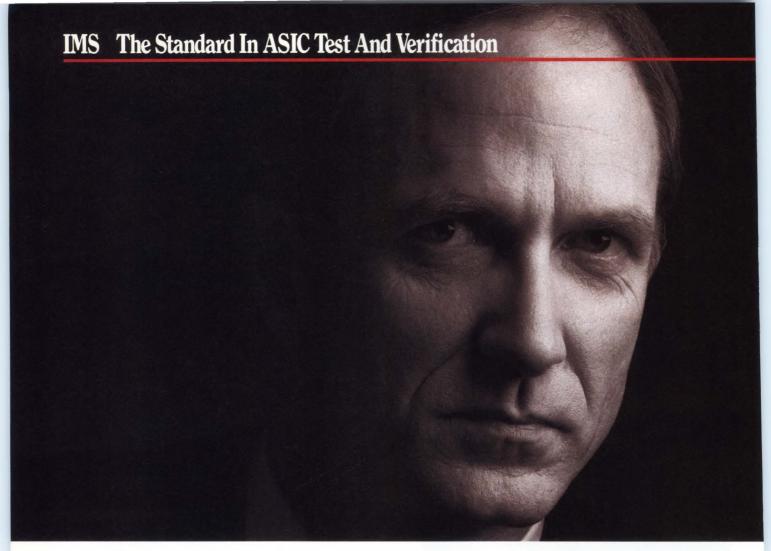
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Hybrid-IC techniques increase power in motor-drive circuits

Thick-film, hybrid-circuit motor drivers not only let you save board space, but also preserve the motor-drive ICs' overtemperature protection and provide a high drive output.

Ed Goodell, Omnirel Corp

Thanks to the availability of "smart-power" motor-drive ICs, you can control motors in a variety of applications. Problems arise, though, when an application requires more drive current than these ICs can provide. By simply adding output-drive transistors and other discrete components to a motor-drive IC's outputs, you can triple the drive current, but you also increase the board size and sacrifice the benefits of overtemperature protection. However, if you use hybrid circuits that combine a motor-drive IC with high current-output devices, you can minimize the space requirement of motor-control circuitry, preserve the IC's inherent thermal-protection capabilities, and obtain the power that your application requires.

A variety of motor-drive ICs that you might employ for servo applications use pulse-width-modulation techniques. Consider, for example, the industry-standard 2935 family of bipolar half-bridge drivers, which are available from Sprague Semiconductor, National Semiconductor, SGS-Thomson, Texas Instruments, and Silicon General. This type of driver (Fig 1) combines a source and sink output stage with diode transient pro-

tection, level shifting, logic stages, and a zener-diode voltage regulator that lets the IC operate from 8 to 35V power supplies. The device accepts TTL-level inputs from a variety of PWM controller ICs.

In addition, the 2935 incorporates an overtemperature shutdown capability and a logic-lockout feature that prevents the source and sink output drivers from turning on simultaneously. If lockout occurs, the output assumes a 3-state (high-impedance) characteristic. In its TO-220-style power package, which has an integral heat-sink tab, the 2935 can provide $\pm 2A$ continuous current and $\pm 3.5A$ peak current to a motor winding. To drive motors that require more current, you must add an external output stage that uses either bipolar power transistors or power MOSFETs.

Avoid simultaneous conduction

To obtain additional current, you may be tempted to add a pair of complementary power MOSFETs to the output of a 2935 motor driver. Fig 2 shows a simple way to drive the p-channel Source driver and the n-channel Sink driver. The circuit is simple, but it presents several problems. First, the configuration gives rise to large crossover currents; that is, there is an interval during the transition from sinking to sourcing or vice versa when both Q_1 and Q_2 are on. During this transition interval, the power MOSFETs form a crowbar across the power-supply terminals, and enormous currents flow through the short circuit.

Another problem arises when the 2935's output assumes its high-impedance state. This condition occurs when both the Source and Sink logic inputs to the IC

You can use a 2950 motor-drive IC in one side of the bridge and a 2935 in the other side to provide a 180° phase differential.

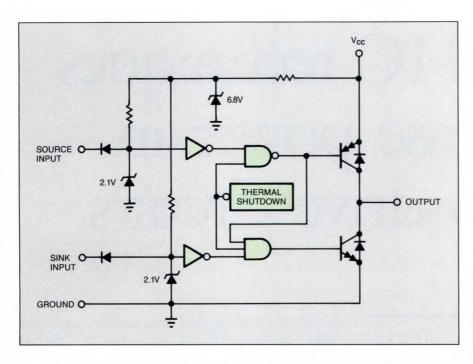


Fig 1—The multisourced 2935 motor-drive IC supplies ±2.5A continuous current from 8 to 35V supplies. It has overtemperature shutdown and a logic-lockout feature that prevents the two output drivers from conducting simultaneously.

are high (a forbidden, but nonetheless possible fault state). During this state, both Q_1 and Q_2 turn on, and, again, constitute a crowbar across the supply terminals. Invariably, at least one power MOSFET burns out.

Your goal, therefore, is to minimize crossover currents during the output transitions and to prevent output conduction when the 2935's output assumes its

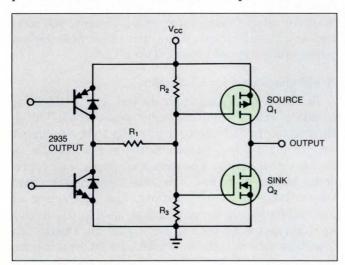


Fig 2—Simplicity is elegant, but it can be dangerous, as this MOSFET-drive configuration shows. If the 2935's output assumes a high-impedance state (as the result, for example, of a forbidden logic state at the Source and Sink inputs), both MOSFETs conduct simultaneously and impose a crowbar across the supply terminals.

high-impedance state. The configuration in Fig 3 satisfies both conditions. In this circuit, the disparate on and off impedances of Q_1 and Q_2 's collector circuits collaborate with the gate-source capacitances of the power MOSFETs Q_3 and Q_4 to eliminate simultaneous conduction.

Consider, for example, the case in which the output stage is sinking current; that is, Q_4 is on and Q_3 is off. In this condition, Q_2 is turned off, and the R_5 - D_2 combination supplies an 18V gate-source turn-on voltage to Q_4 . Q_1 is saturated and therefore holds Q_3 's gate-source voltage well below the MOSFET's turn-on threshold. When the circuit switches from a sinking to a sourcing mode, Q_1 turns off and Q_3 turns on at the same time. When Q_1 turns off, its collector impedance is $2 \text{ k}\Omega$ in series with Q_3 's gate-source capacitance (approximately 1000 pF). The time constant at the gate of Q_3 is therefore about $2 \text{ } \mu\text{sec}$; Q_3 turns on after a delay of less than $2 \text{ } \mu\text{sec}$.

Switching delays prevent crossover

The situation is different, however, for Q_4 . When Q_2 turns on, it presents a low impedance to Q_4 's gate circuit, and the gate capacitance discharges rapidly to turn off Q_4 . Because of the disparate turn-on and turn-off impedances, the turn-on/turn-off time ratio is greater than 100:1. Both MOSFETs, therefore, are turned off for a significant interval during transitions, and no crossover current can flow.

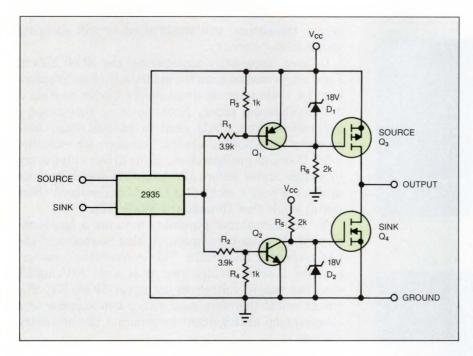


Fig 3—Simultaneous conduction of the two MOSFETs can't occur in this circuit configuration. If the 2935's output assumes its high-impedance state, the voltage divider at the bases of Q_1 and Q_2 turns off both bipolar transistors and, consequently, turns off both MOSFETs.

The oscilloscope photos in Fig 4 show how the gate-circuit time constants ensure break-before-make operation of the output stage. In Fig 4a, the fast rising edge of the p-channel gate waveform in trace A makes the MOSFET turn off quickly. In trace B, the rising waveform's time constant ensures that the n-channel MOSFET doesn't turn on until after the p-channel device is turned off. The same situation applies to the negative-going gate signals; in this case, the p-channel MOSFET doesn't turn on until the n-channel device is firmly turned off. Figs 4b and 4c show the output-current waveforms in relation to the gate signals of the n-channel MOSFETs (c).

The circuit in Fig 3 also solves the problem of faulty logic at the inputs to the 2935 IC. When both the IC's Source and Sink inputs are asserted, the output stage in the 2935 turns off and assumes a high-impedance state. The voltage divider at the bases of Q_1 and Q_2 causes both transistors to turn on, and the saturated transistors hold both power MOSFETs off.

A similar fault condition can arise if the 2935 derives its power from a separate power supply. In Fig 2, if the MOSFETs' power supply turns on before the 2935's supply, both MOSFETs turn on simultaneously and, again, place a crowbar across the supply terminals. In the configuration shown in Fig 3, however, the MOSFETs stay off in this supply-sequencing scenario.

You might assume that Fig 3's circuit configuration

would be equally suitable for connecting bipolar output drivers, rather than MOSFETs, to the motor-drive IC. To do so, however, you must consider the bipolar transistors' high drive requirements. To produce a forced gain of 10, for example, to saturate the transistors, the drive circuitry would have to provide 600 mA of base drive to the output transistors. You can produce such drive current by scaling down the circuit impedances, but you waste a considerable amount of power.

Bipolar Darlington pairs, of course, reduce the base-drive requirement, but it's still appreciable. At a 6A continuous current and a 3V collector-emitter saturation voltage, the minimum current gain for a typical Darlington pair is 100. The required base-drive current, therefore, is 60 mA.

Another problem that attends the use of bipolar power transistors, whether you use a single or a Darlington configuration, is the disparity in current rise and fall times. Because the transistors have long storage times, they turn on faster than they turn off. You're therefore faced with large crossover currents that arise from the simultaneous conduction of the upper and lower power devices.

Bipolar transistors (both single and Darlington) are also susceptible to secondary breakdown. This problem is especially acute for motor-drive circuits because the winding inductance of a motor can induce large voltage spikes (the inductive-kickback effect). To protect the

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Adding a pair of complementary power MOSFETs to the ICs' outputs is a poor high-drive solution.

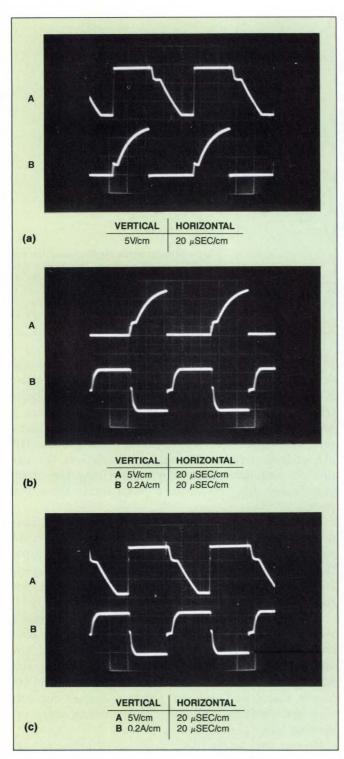


Fig 4—Disparate turn-on and turn-off times eliminate crossover currents. The bipolar drivers' rapid turn-on times ensure that each power MOSFET turns off well before its complementary partner turns on.

output transistors, you would need to add clamping and snubbing circuitry.

In most motor-drive applications, the MOSFETs in Fig 3 are protected from the inductively induced spikes because their intrinsic drain-source diodes provide a built-in clamping action. Note, however, that in some applications, you would need to add external, fast-recovery freewheeling diodes. Consider, for example, a full H-bridge configuration. If the driver outputs try to switch states before the moderate-speed intrinsic diodes recover, a momentary, kickback-induced short circuit would flow through the MOSFETs.

Yet another output possibility is to use a quasicomplementary output configuration; that is, you could use two n-channel MOSFETs. This connection, however, requires a drive voltage that is at least 10V higher than the supply voltage to the upper MOSFET. The circuit would therefore need either two supplies or a charge-pump arrangement to generate the necessary voltage.

Layout considerations

If you choose to use the fail-safe, crossover-free circuit of Fig 3, you must select the proper components for the application and lay out the circuit. Assume your single-ended motor requires 6A continuous, 10A peak current—three times the current you can obtain from an unassisted 2935 motor-drive IC. To satisfy these requirements, you can use an inexpensive power MOSFET such as the n-channel MTP3055E and its MTP12P05 complement from Motorola (and other manufacturers). The TO-220-housed devices provide 50V and 6A continuous output current.

For commercial or industrial applications, these low-cost MOSFETs fill the bill. A quick thermal analysis reveals that the MTP3055E and MTP12P05 can easily provide the 6A continuous current. The n-channel MTP3055E, for example, has 0.15Ω on-resistance ($r_{DS(on)}$) at 25°C and 3.12°C/W junction-to-case thermal resistance (R_{AIC}).

Based on your knowledge of the maximum permissible junction-temperature rise and the power dissipated in $r_{\rm DS(on)}$, you can calculate the maximum allowable current. Keep in mind, however, that a power MOSFET's on-resistance isn't a constant—it increases with temperature. In fact, at $150^{\circ}\mathrm{C}$ (the maximum permissible junction temperature), a typical MOSFET's on-resistance is about 2.2 times the value at $25^{\circ}\mathrm{C}$. The MOSFET's on-resistance thus becomes 0.33Ω at $150^{\circ}\mathrm{C}$.

Assuming you provide sufficient heat removal to

keep the TO-220 case at 70°C, the allowable junction-to-case temperature differential is 80°C. If you divide this temperature rise by the 3.12°C/W thermal resistance, you find that the allowable power dissipation is 25.64W.

Because the $I^2r_{DS(on)}$, or $0.33I^2$, equals the 25.64W, I is about 8.8A. Although the p-channel MTP12P05 has an $r_{DS(on)}$ that is about twice that of the MTP3055E, its junction-to-case thermal resistance is about half that of the n-channel device (because of the larger die employed). The thermal calculation for the MTP12P05 yields a permissible continuous current of about 8.5A.

Hybrid circuits combine benefits

Fig 5a shows a possible pc-board layout of the MOSFET-augmented, half-H-bridge motor driver. The IC and the power MOSFETs in this layout come in TO-220-style plastic packages; the small-signal transis-

tors are housed in plastic TO-92 packages. Using the same layout, you can make a hermetically sealed, military version of the driver. As a result of the cooperative efforts of Omnirel and Sprague Semiconductor, the 2935 IC is also available in a hermetically sealed package, whose outline is similar to that of a TO-220 package.

The power MOSFETs, too, are available in hermetically sealed, TO-220-outline packages: the TO-258 and TO-220H packages. Note, however, that these devices aren't cheap; MOSFETs in the hermetic TO-258 packages cost more than \$40. For about \$4, you can get the same device in the TO-3 package. However, the inexpensive, TO-3-packaged power MOSFETs shown in Fig 5b consume about 65% more pc-board space than the versions in Fig 5a. The hermetically sealed hybrid circuit shown in Fig 5c combines the features

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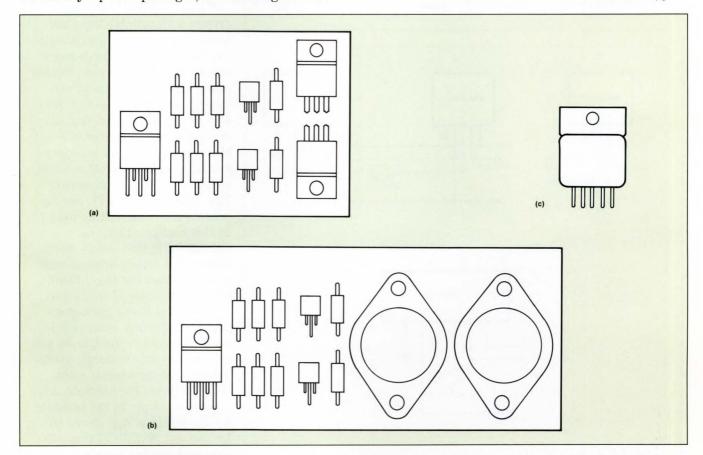


Fig 5—The pc-board version (a) uses plastic or hermetically sealed TO-220-style power devices in the layout of Fig 3's circuit. Another hermetic version (b) uses less-expensive power MOSFETs in the classic TO-3 package. The hermetically sealed hybrid-circuit version (c) offers the same power capabilities as the pc-board versions, and it provides thermal coupling from the power MOSFETs to the overtemperature-protected 2935 motor-drive IC.

Use hybrids to power your motors

Three hybrid-circuit versions of the H-bridge motor drivers are currently available: the OM9320SS, OM9319SC, and OM9321SC. Model OM9320SS is a full-H-bridge motor driver; the OM9319SC and the OM9321SC are half-H-bridge drivers. The OM9319SC corresponds to (and uses) the 2935 motor-drive IC: the OM9321SC uses the invertedphase 2950 IC. Table A is the truth table for the three models. You can see that the forbidden 1,1 input combination (0,1 for the drivers that incorporate the 2950) produces an open condition at the outputs.

Table B gives some of the salient performance characteristics of the hybrid-circuit motor drivers. For all the specifications shown, the input high and low levels are the standard TTL levels of 0.8V max, 2.4V min, respectively. You can see that the on-to-off propagation delay is much shorter than the off-to-on delay, thereby ensuring a break-before-make characteristic in the output stage. The output on voltages are given with the 10A

maximum peak current; for the 6A maximum specified continuous current, the figures are 33V and 2V, respectively.

Fig A shows three ways to use the motor drivers with single-phase dc motors. In Fig Aa, the OM9321SC drives a motor in a half-H-bridge connection. Note that the motor's return lead must connect to a voltage equal to half the supply voltage. As a result, the drive to the motor is $0.5V_{\rm CC}$ p-p.

Figs Ab and Ac show two ways to implement full-H-bridge drivers. These drivers let you control both the direction and the speed of the motor. In these full-H-bridge drivers, the motor receives peak-to-peak drive equal to the full power-supply voltage minus Ir_{DS(on)} of the power MOSFETs.

If you couple the hybrid motor drivers with suitable logic and proper phase timing, you can also use the drivers to drive 3-phase motors. Fig B shows one possible configuration. This circuit uses three UGN-3130 Hall-effect sensors to sense the shaft position of the motor. The motor is a brushless dc type; the sensors essentially replace the older brush switches, which can wear out. The 7400 and 7402 TTL circuits provide the commutating logic. In this configuration, the OM9321SC hybrid-circuit motor drivers can supply drive as high as 35V (minus the Ir_{S(on)} drop), 6A to each phase of the motor.

Additional power packages that are currently being developed will make it possible for you to fabricate hybrid-circuit motor drivers that incorporate even more features. For example, adding one more pin to the package for the full-H-bridge driver will let you use MOSFETs that offer a current-sensing terminal. With the addition of some simple feedback circuitry, this sensing termi-

TABLE A-MOTOR-DRIVER TRUTH TABLE

SOURCE	SINK	OM9319SC	OM9321SC	OM9320SC	
INPUT	INPUT	OUTPUT	OUTPUT	OUTPUT 1	OUTPUT 2
0	0	HIGH	LOW	HIGH	LOW
0	1	HIGH	HIGH Z	HIGH	HIGH Z
1	0	LOW	HIGH	LOW	HIGH
1	1	HIGH Z	HIGH	HIGH Z	HIGH

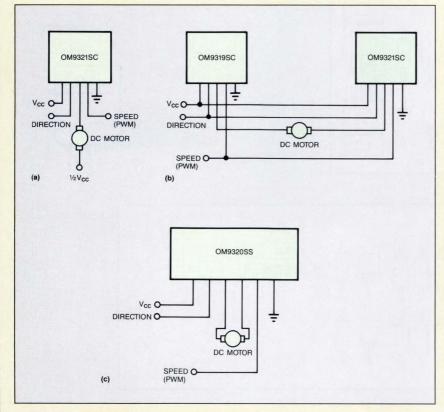


Fig A—The OM9321SC half-H-bridge driver in a provides a voltage swing equal to half the supply voltage. In the full-H-bridge configurations in b and c, the single-phase dc motor receives a voltage swing equal to the full power-supply voltage minus $Ir_{DS(on)}$.

nal allows you to control the current limiting in the driver.

Packages with higher pin counts would also let you power the 2935 and 2950 motor-drive ICs from a separate power supply. With the addition of some level-shifting circuitry, you could run the MOSFETs from high-voltage (100V and higher) power supplies. In additon, by using larger power-device dies, you could produce hybrid-circuit drivers that handle tens of amperes and several hundred volts.

TABLE B-MOTOR-DRIVER SALIENT CHARACTERISTICS

PARAMETER	MINIMUM	MAXIMUM	UNITS
OUTPUT OFF—STATE LEAKAGE CURRENT		50	μА
OUTPUT ON VOLTAGE AT OUTPUT=10A HIGH STATE LOW STATE	30	3.3	VOLTS VOLTS
INPUT CURRENT LOW STATE HIGH STATE		1.5 50	mA μA
PROPAGATION DELAY OUTPUT ON-TO-OFF OUTPUT OFF-TO-ON		750 2	nSEC μSEC
INTRINSIC DIODE FORWARD VOLTAGE AT OUTPUT=6A		2.2	VOLTS
SUPPLY CURRENT HALF H-BRIDGE FULL H-BRIDGE		80 160	mA mA

NOTES:

 $T_A = 25$ °C, $T_{TAB} = 70$ °C, AND $V_{CC} = 35$ V

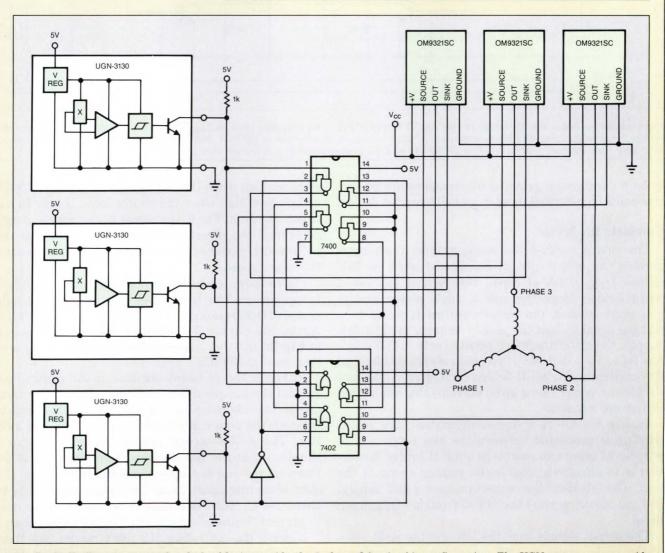


Fig B—Hall-effect sensors and a dash of logic provide the 3-phase drive in this configuration. The UGN-3130 sensors provide shaft-position information; the 7400-series TTL circuits provide the commutating logic. The OM9321SC hybrid-circuit motor drivers provide drive as high as 35V, 6A to each of the three phases of the motor.

If the Source and Sink inputs are asserted, the output stage of the 2935 turns off and assumes a high-impedance state.

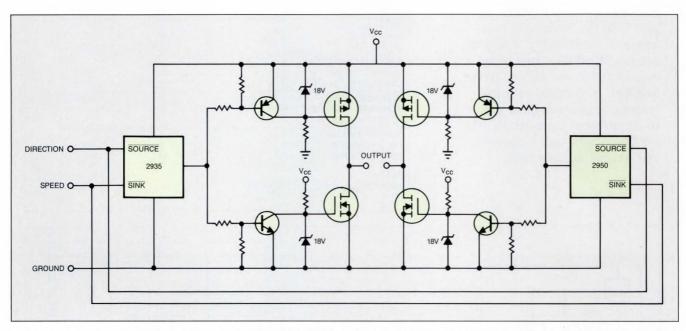


Fig 6—A mirror-image circuit completes the half-H bridge of Fig 3. By providing push-pull operation, this circuit doubles the available voltage swing at the load. The 2950 motor-drive IC is an inverted-phase version of the 2935. Both sides of the bridge feature logic lockout to prevent simultaneous conduction of the MOSFETs and, as a result, offer crossover-current-free switching.

of both packages; it provides overtemperature protection and a high current drive in a small footprint device.

Complete the bridge

The bipolar motor-driver configuration, which incorporates the hybrid circuit, delivers as much as 35V (minus $Ir_{DS(on)}$), 6A of drive. However, if you use a half-H-bridge connection and a single power supply, you must connect the motor's return terminal to a voltage equal to half the supply voltage. With a 35V supply, the motor therefore receives only ± 17.5 V (minus $Ir_{DS(on)}$) p-p of drive. If you use two nearly identical driver circuits in a full-H-bridge configuration, you can double the power (for a given current) that the circuit delivers to a motor.

In Fig 6's full-H-bridge configuration, the motor winding is connected between the two outputs. The purpose of using two circuits in a full-H-bridge connection is to effectively double the voltage swing at the load. The full-H-bridge connection uses a 35V supply, and the motor receives the full 35V (minus $Ir_{DS(on)}$) p-p drive.

The output signals from the left and the right sides of the bridge must be 180° out of phase. The circuit in **Fig 6** accomplishes this phase inversion by using a 2950 motor-drive IC in the right side of the bridge. This IC is identical to the 2935, except that its output

switches high when the Source input is high; the 2935's output goes high when the Source input is low. In the circuit shown in Fig 6, the signal to the Source inputs determine the direction of motor rotation, and the pulse-width-modulated signal to the Sink inputs control the motor speed.

Fig 7a shows a possible pc-board layout of the full-H-bridge driver. This layout uses plastic or hermetically sealed TO-220-packaged ICs and power MOSFETs. Again, you can use TO-3-housed MOSFETs, as shown in Fig 7b, but they use about 85% more pc-board area than the TO-220 ICs.

Although the pc-board versions of the motor-drive circuits are inexpensive to construct, they suffer from one serious shortcoming. No thermal feedback exists between the power MOSFETs and the 2935 and 2950 ICs. These ICs incorporate an overtemperature-shutdown feature that disables them when the chips' temperature reaches approximately 165°C. The ICs start operating again when the temperature drops to about 140°C. This hysteresis is necessary, of course, to prevent "hunting" around the trigger temperature.

Because the controlling ICs don't receive any thermal feedback, they can't protect the power MOSFETs against fault conditions in the load. For example, if a motor becomes overloaded, the excessive current flow could burn out one or both of the MOSFETs. There-

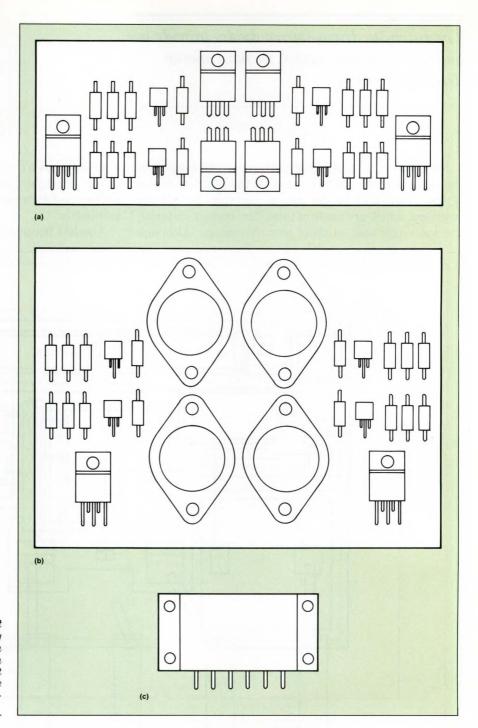


Fig 7—Layouts for the full-H-bridge circuit of Fig 6 use either plastic or hermetically sealed TO-220-style power devices shown in a or TO-3-housed power MOSFETs shown in b. The hermetically sealed, hybrid-circuit version in c uses about 20 and 10% less space than the pc-board versions in a and b, respectively.

fore, in addition to space-saving considerations, the intrinsic thermal coupling of devices is another benefit of developing a hybrid-circuit motor driver. Fig 7c shows this hybrid-circuit implementation of the full-H-bridge driver.

Making the hybrid

To make the hybrid, you must optimize the ICs' thermal intimacy, and, at the same time, provide efficient heat transfer from the circuit elements to the pc board and/or the external heat sink. A beryllia (BeO) substrate, soldered to the metal-package header, fulfills these objectives. This substrate has thermal conductivity properties that are approximately equal to

those of aluminum metal. This substrate serves three purposes: In addition to providing efficient heat transfer among the circuit elements and to the external environment, it provides electrical isolation to the circuit devices, and it offers a platform for printing conductors and thick-film resistors.

The hybrid-circuit layout for the half-H-bridge driver (Fig 8) is quite simple; its component designations are the same as the those in Fig 3. The semiconductors are bonded to the BeO substrate by a high-temperature solder-reflow process. The leads that connect the circuit to the package tabs are 10-mil aluminum wires that are stitch-bonded to the MOSFETs and the conductor pads on the substrate.

The intrinsic drain-source diodes provide a built-in clamping action in most motor-drive applications.

Note the large conductor pattern at the bottom of the substrate; the pattern connects the common drains of the MOSFETs to the output pin (pin 3). All the resistors, which are made of thick-film cermet material, are laser trimmed to their nominal values. Although tolerances aren't critical in these motor-drive circuits ($\pm5\%$ is ample), the laser-trimming process and the cermet resistors can easily produce tolerances of $\pm1\%$ and better.

Another feature that you should note in this hybrid-

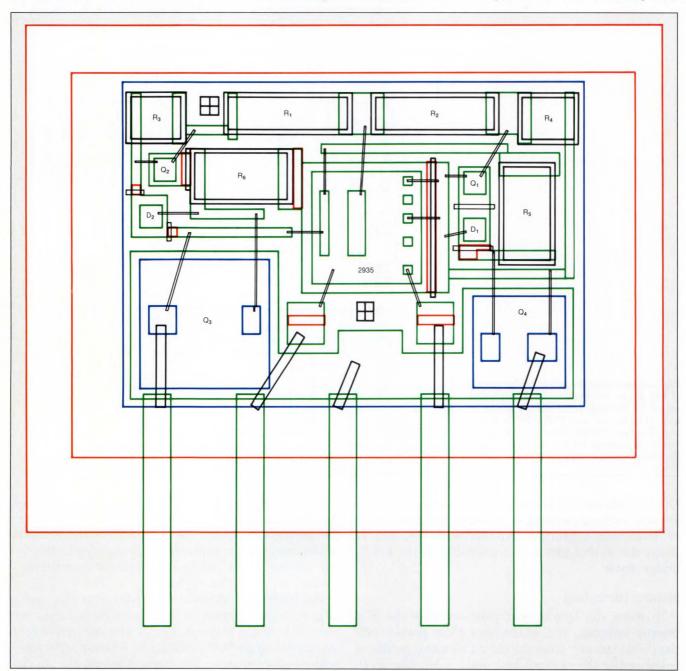


Fig 8—This half-H-bridge driver uses readily available semiconductor chips. High-temperature solder die attach ensures efficient heat transfer from the junctions to the BeO substrate. The 10-mil aluminum wires eliminate high-temperature intermetallic problems that can accompany a gold-to-aluminum interface.

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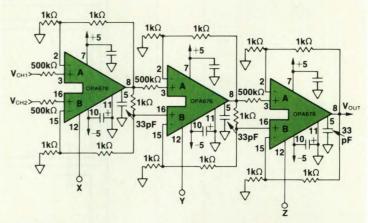
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By thermally coupling devices, you enable the controlling ICs to protect the power MOSFETs against fault conditions in the load.

circuit layout is the proximity of the 2935 motor-drive IC to the two power MOSFETs. Because the IC is situated between the two power devices, it quickly senses any overtemperature condition in either or both of the MOSFETs and shuts down accordingly. The

high thermal conductivity of the BeO substrate plays a major role in this isothermal design.

By making some thermal calculations, you can determine the maximum continuous operating current for the half-H-bridge driver. Again, $R_{\theta JC}$ for the package

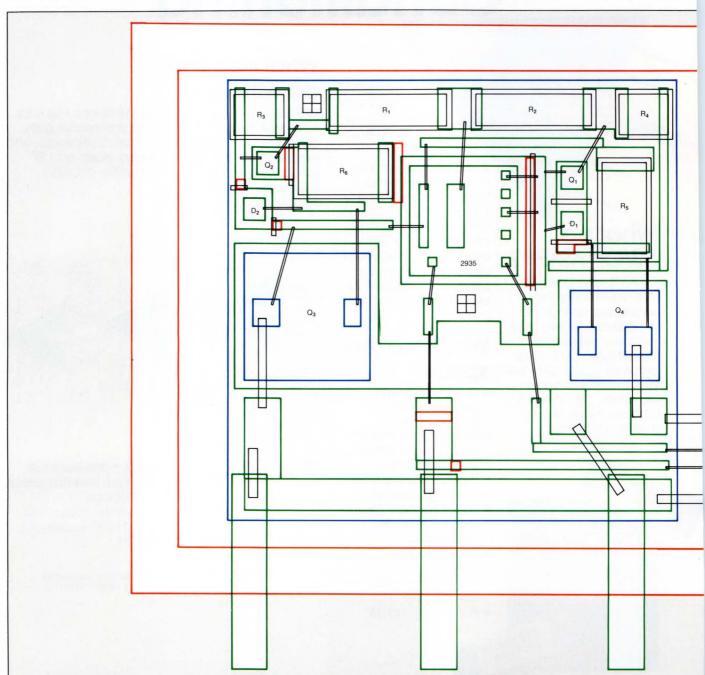
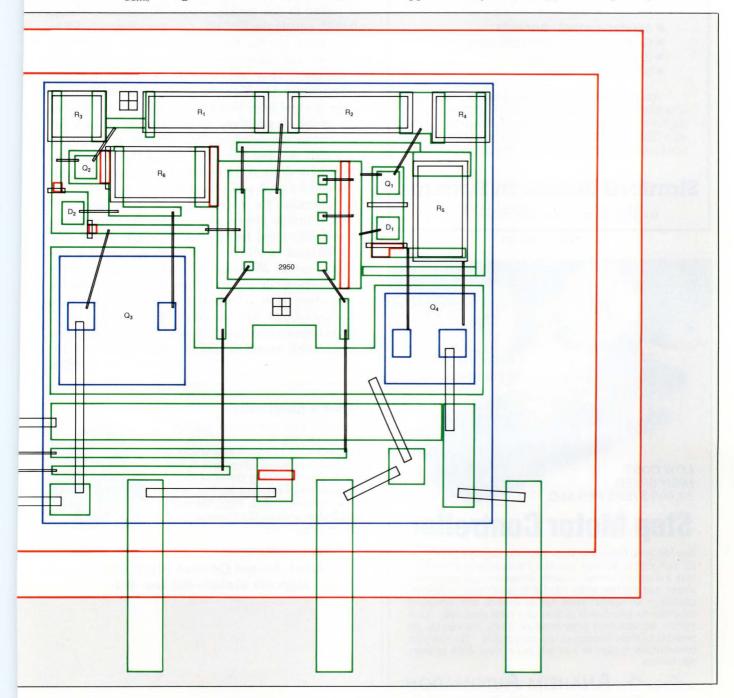


Fig 9—This full-H-bridge layout provides bonding pads for interconnecting the left and the right sides of the bridge. To provide the necessary phase inversion for push-pull operation, the right side of the bridge uses a 2950 motor-drive IC instead of a 2935.

and $r_{\rm DS(on)}$ for the power MOSFETs are the determining factors in your thermal analysis. You need to calculate the values for only one of the MOSFETs because when one is on, the other is off. Because the p-channel MOSFET's $r_{\rm DS(on)}$ is higher than that of the n-channel

device, the p-channel 12P05 produces the worst-case current-limiting situation.

For the 12P05, $r_{DS(on)}$ is 0.3 Ω at 25°C. At the maximum allowable junction temperature of 150°C, $r_{DS(on)}$ is approximately 0.66 Ω . $R_{\theta JC}$ for both packages is 1.5°C/



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W. Assuming the package temperature is held at 70°C, the permissible junction-temperature rise is 80°C. Dividing 80°C by the 1.5°C/W yields the maximum allowable power in the package: 53.33W. Because $I^2R_{\rm eJC}$, or 0.66 I^2 , equals the 52.33W, I is approximately 8.9A.

The layout for the full-H-bridge driver (Fig 9) includes two substrates that are the same except for two features. They use different conductor patterns to interconnect the $V_{\rm CC}$, the Source and Sink inputs, and the ground lines between the left and right sides of the circuit. In addition, the components on each side of the circuit are different. The left side of the circuit uses a 2935 IC, and the right side of the circuit uses a 2950 motor-drive IC to provide the 180° phase reversal needed for push-pull operation.

To determine the maximum continuous current of the full-H-bridge driver, you can use the same values that you calculated for the half-H-bridge driver with one additional condition. You must assume that the p-channel power MOSFET is conducting on one side of the circuit while the n-channel device is conducting on the other side. The power is therefore equal to $I^2(r_{\text{PDS(on)}} + r_{\text{NDS(on)}})$. The two on-resistances at the 150°C junction temperature are 0.66 and 0.33 Ω , respectively. Because 0.99 I^2 equals 53.33W, I is approximately 7.3A.

Author's biography

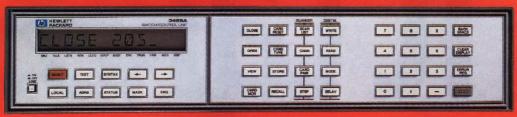
Ed Goodell is the manager of applications engineering at Omnirel Corp (Leominster, MA), which specializes in high-power semiconductors and hybrid circuits. Before joining Omnirel, he worked on magnetic-tape backup systems at Tecmar (Solon, OH). Ed holds a BSEE degree from the University of Massachusetts.



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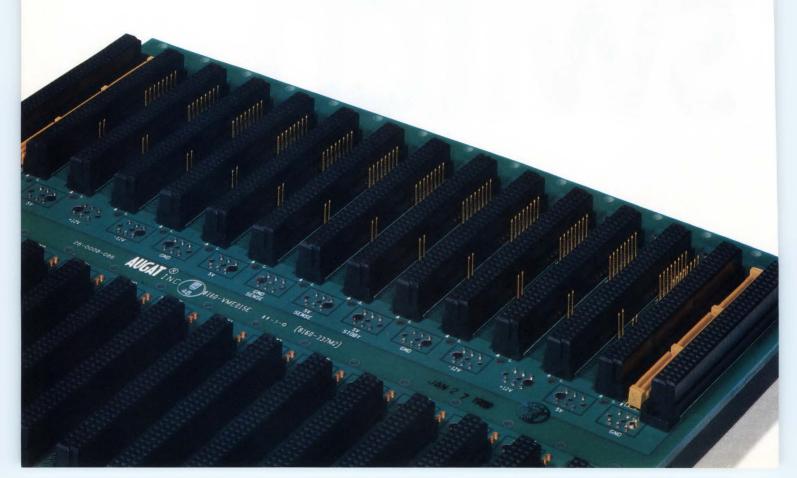
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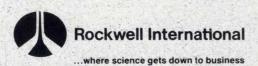
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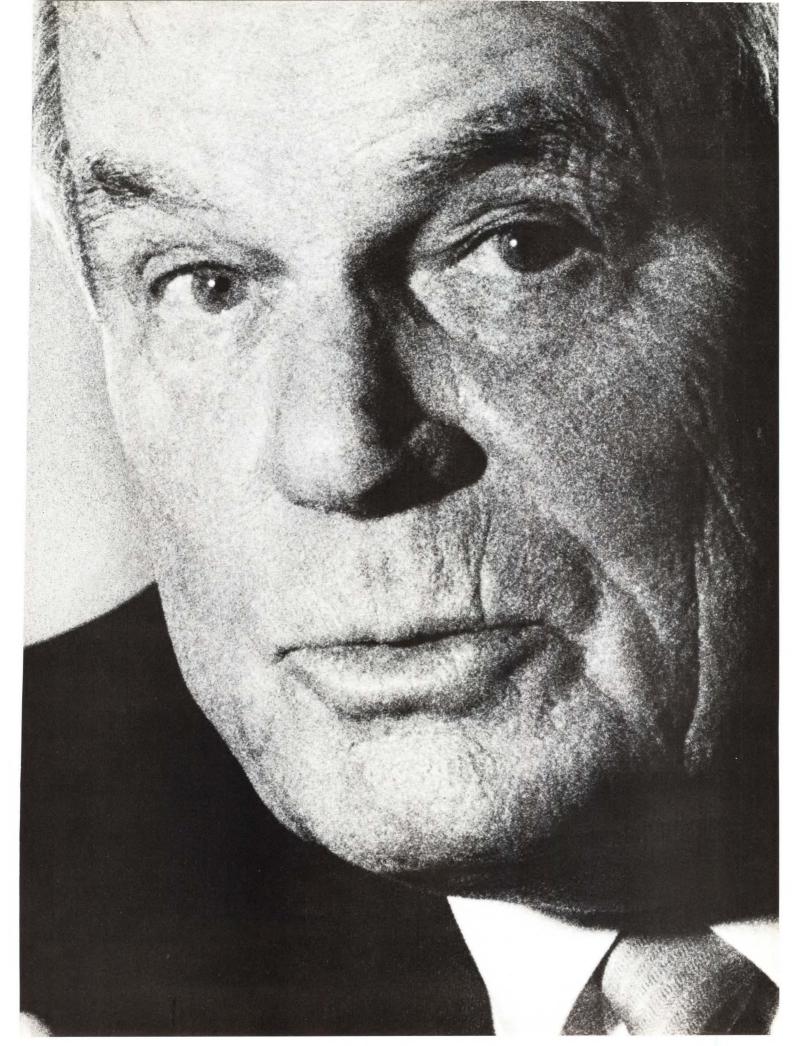


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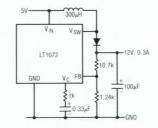
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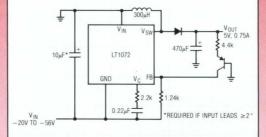
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DESIGN IDEAS

EDITED BY CHARLES H SMALL

Self-biasing reference consumes low power

Walter Jung and George Erdi Linear Technology Corp, Milpitas, CA

The circuit in **Fig 1** is a micropower, buffered reference that works best with loads that source current. It will operate from any supply that is 3V higher than the reference voltage, including 4 to 9V batteries. Typical line regulation is 10 ppm/V. The overall temperature coefficient of the circuit is essentially that of D_1 : 20 ppm/°C (max for the B device grade).

Overall, this reference's quiescent current is 30 μ A—essentially the quiescent current of the dual op amp plus the currents in R₂ and R₃. The reference can source several milliamperes of load current to external loads. For example, the IC_{1A}, 1.227V stage has a typical output impedance of 30 μ V/mA for currents of 10 mA or less.

Normally, you would bias D_1 —a 20- μA , 2-terminal reference diode—with a simple series resistor connected to V^+ . This simple biasing scheme, however, can be sensitive to line-voltage changes and could depart from micropower operation when heavily loaded.

Instead, op amp IC_{1A} 's 30- μA quiescent current provides a "free" bias source for D_1 . Both the input and

the output of the op amp used for IC_{1A} must be able to swing down to the op amp's V^- voltage level. In this case, the op amp's V^- pin will be at 1.225V $\pm\,15$ mV.

The simple RC filter comprising R_1 and C_1 feeds the noninverting input of IC_{1A} , which functions as a low source-impedance buffer. The other half of IC_1 functions as a precision $2\times$ amplifier/buffer. Note that both op-amp sections draw their input currents through R_1 . These currents serve to raise the op amps' inputs a few millivolts above the level of the reference diode. This slight raise and the tiny current drawn by R_2 serve to bias IC_{1A} and IC_{1B} 's inputs up into a slightly more linear operating region than they would experience at the negative rail.

Note that you should use caution when employing this circuit with current-sinking loads, because the sunk current must necessarily flow through the reference diode. While the diode can safely sink up to 20 mA, the saturation characteristics of the op amp will add an error proportional to the sunk current.

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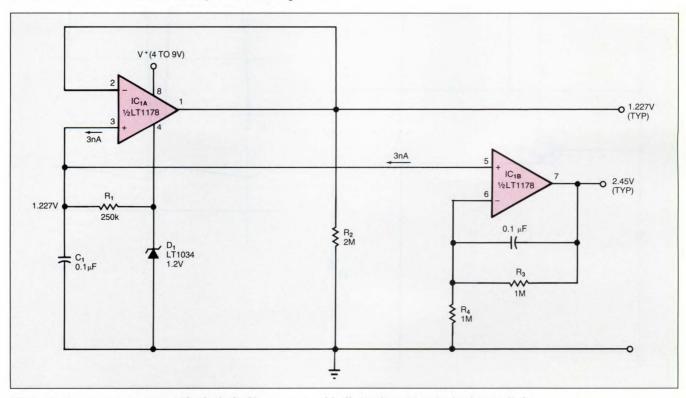


Fig 1—A micropower op amp provides both the bias current and buffering for a 2-terminal reference diode.

Single cell lights LED

Lacz Gyula and Bunsits Józef Hiradástechnika Szövetkezet, Budapest, Hungary

You can light LEDs from a low-voltage source with the 150-kHz shunt switch-mode driver in Fig 1. Without this circuit, for example, a 1.2V battery has insufficient voltage to bias an LED on via a series resistor.

In the circuit, comparator Q_1 turns electronic switch Q_2 on and off. When Q_2 turns on, current flow ramps up in L_1 , and LED D_2 is back-biased. Eventually, the voltage this current flow develops across R_6 turns off

 Q_1 . Q_1 's turning off, in turn, turns off Q_2 . When Q_2 turns off, LED D_2 acts as a freewheel diode for L_1 and lights up.

Diode D_1 compensates for the temperature dependence of Q_1 's base-emitter voltage and reduces the sensitivity of the R_1/R_2 divider to changes in supply voltage. R_4 limits the base current of Q_2 , and R_5 adds hysteresis to the Q_1 comparator.

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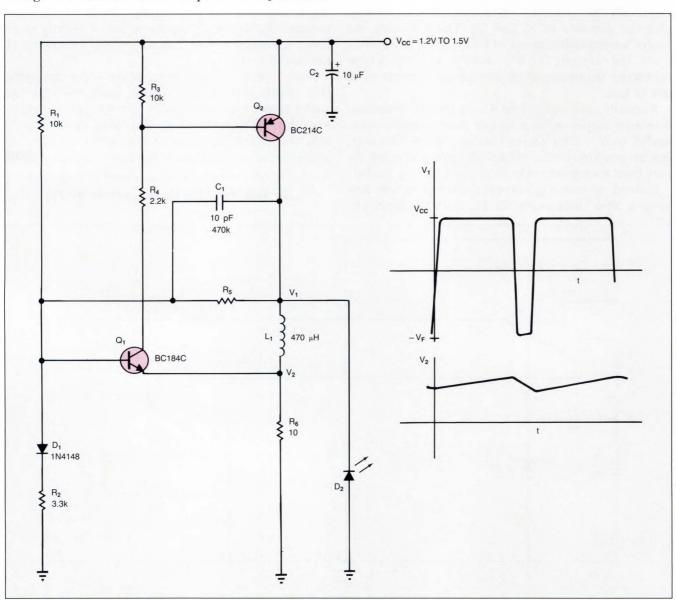


Fig 1—This free-running switch-mode driver can light an LED from a low-voltage source.

Amplifier handles duplex line

Mansour Ahmadian Technical and Engineering University, Tehran, Iran

The circuit in Fig 1 is a bidirectional amplifier that can amplify both signals of a duplex telephone conversation. It uses the principle of negative resistance. Obviously, such an amplifier could easily be unstable; how-

ever, you can adjust R_1 in Fig 1 for maximum amplification and the circuit will remain stable. You might also consider replacing the LM324 op amps with op amps that would distort less, such as the LM1558, LF412, LF353, or LF442.

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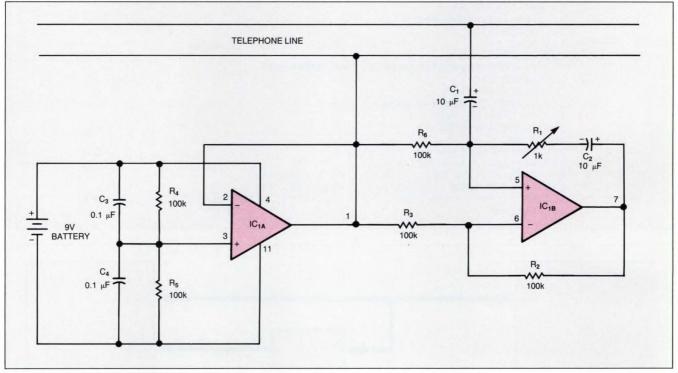


Fig 1—This amplifier uses the negative-resistance principle to amplify full-duplex telephone signals.

Single-chip µP acquires Basic

G Nagendra Rao ISRO Satellite Centre, Bangalore, India

Unfortunately, no CMOS equivalent exists for the very handy 8052-AH single-chip μP with built-in Basic interpreter. This NMOS chip draws 100 mA typ. A low-power CMOS version of the 8052, the 80C32, lacks the on-chip Basic interpreter. You can remedy this situation by simply dumping the contents of an 8052-AH's

onboard ROM into a 27C64 CMOS EPROM for subsequent use by the 80C32.

The combination of the CMOS single-chip μP and EPROM consumes $\frac{1}{100}$ the power of the NMOS chip and cost $\frac{2}{30}$ less. Running the Basic program in Listing 1 on the single-chip μP board in Ref 1 results in a dump, in Intel hex format, of the Basic interpreter through the board's console port. You can store this file on a disk using the Capture command of any com-

DESIGN IDEAS

munication program such as Crosstalk or Mirror. Sub- μP's External Code space from 0000_{HEX} to 1FFF_{HEX} sequently, you can download this file to any EPROM programmer that accepts Intel hex format.

Of course, your target system must have chip-select circuitry that places the EPROM in the single-chip (Fig 1).

To Vote For This Design, Circle No 748

```
LISTING 1—BASIC INTERPRETER DUMP ROUTINE
10 REM To transmit data in Intel HEX format
20 M=0:X=0:Y=0:
30 COUNT=0:SUM=16+X+Y+0
40 PRINT ":10"
50 T=X:GOSUB 210
60 T=Y:GOSUB 210
70 T=0:GOSUB 210
80 FOR I=M TO M+15
90 T=CBY(I):SUM=SUM+T
100 GOSUB 210
110 NEXT I
120 COUNT=1
130 B1=INT(SUM/256):B2=SUM-B1*256:T=256-B2
140 GOSUB 210
150 M=M+16:Y=Y+16
155 IF Y>255 THEN Y=0:X=X+1
170 IF M<2000H THEN 30
180 PRINT":00000001FF"
190 STOP
210 REM subroutine for hex conv
220 Al=INT(T/16):A2=T-16*A1
230 IF A1>9 THEN C1=65+(A1-10) ELSE C1=A1+48
240 IF A2>9 THEN C2=65+(A2-10) ELSE C2=A2+48
250 IF COUNT=1 THEN PRINT CHR(C1), CHR(C2) ELSE PRINT CHR(C1), CHR(C2),
260 RETURN
```

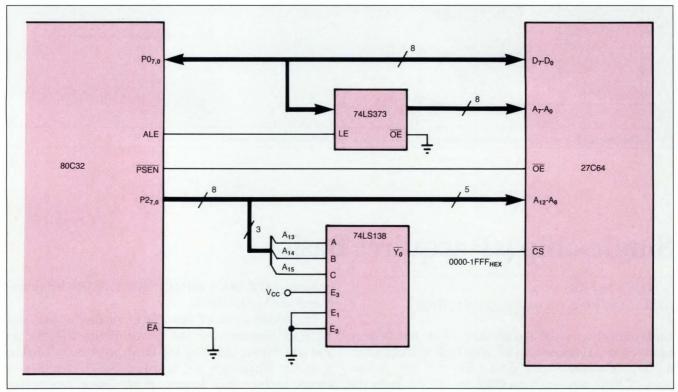


Fig 1—With a simple modification to an 80C32 system's chip-select circuitry, the CMOS single-chip \(\mu \)P can access a Basic interpreter residing in an EPROM and function like a low-power version of the NMOS 8052-AH.



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r ass bario (ivii iz	-)	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)			26	55	95	116	150	190	290	365	460	520	570	660	720

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*Prefix P for pins, B for BNC, N for Type N, S for SMA

example: PLP-10.7

C105 REV. E

Reactive limiter protects transformer

Jim Zannis Renishaw Metrology Ltd, Gloucestershire, UK

The simple reactive voltage divider in Fig 1 (a capacitor in series with the primary of a transformer) performs a dual function: It protects the transformer against excessive currents if its secondary gets shorted, and it prevents damage if anyone inadvertantly connects a 120V transformer to a 240V line.

The reactive current-limiting scheme works best if your load normally draws little current through its mains-connected transformer (Fig 2). You should therefore choose $jX_{\rm C}$ to be less than the effective input impedance of your transformer's normal load. Under fault conditions, $jX_{\rm C}$ drops a proportionally larger voltage than under normal, lightly loaded conditions, which reduces the voltage across the transformer's primary. This reduction of voltage prevents the transformer from saturating and thus overheating.

The capacitor in the limiter dissipates no significant power because its voltage is not in phase with its current. However, the circuit reaction can impress a voltage on the capacitor that is greater than the mains' input voltage. You must choose a capacitor, such as a high-quality film capacitor that can handle both the expected current and the voltage overstress.

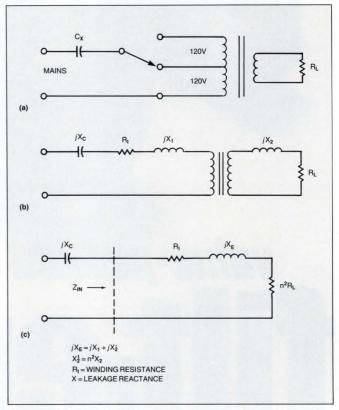


Fig 1—The 120/220V transformer in a has a current-limiting capacitor in its primary circuit; b shows the transformer's equivalent circuit. Reflecting all the circuit elements over to the primary side of the circuit produces the equivalent circuit in c.

To Vote For This Design, Circle No 747

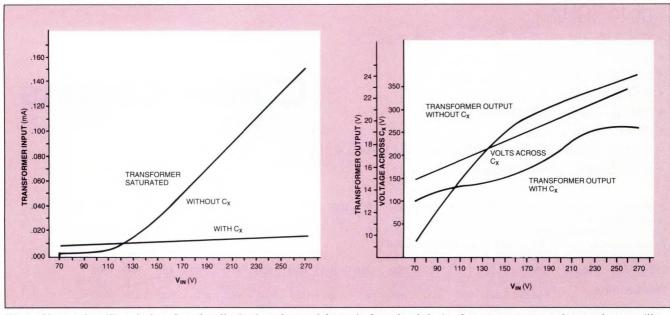


Fig 2—If you select jX_C to be less than the effective impedance of the equivalent circuit in Ic, then your power-supply transformer will not saturate during an overvoltage stress.



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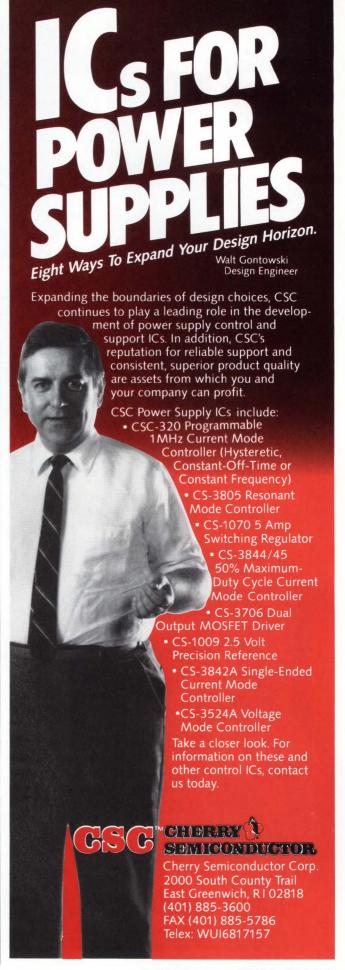
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The winning Design Idea for the January 19, 1989, issue is entitled "Filter settles faster than a Butterworth," submitted by Einar Abell of ADA Instruments (Three Rivers, CA).

Your vote determines this issue's winner. All designs published win \$100 cash. All issue winners receive an additional \$100 and become eligible for the annual \$1500 Grand Prize. Vote now, by circling the appropriate number on the reader inquiry card.



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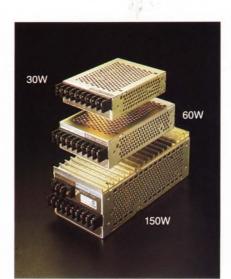
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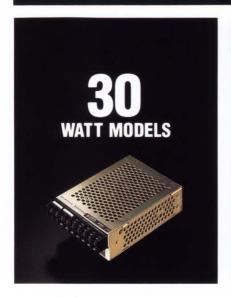


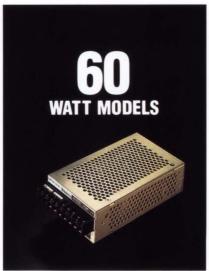
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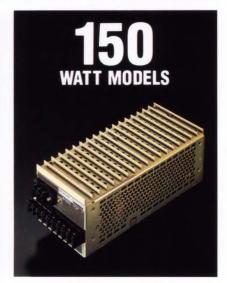
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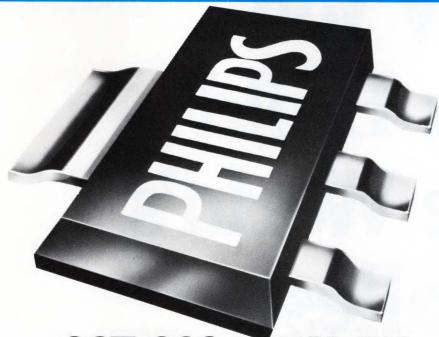




SPECIFICATION	OUTPUT VOLTAGE		OVP SETTING	OUTPUT CURRENT			CURRENT LIMIT	RIPPLE		NOISE (SPIKE)	EFFICIENCY	
Unit	Volts		Volts	Amps		Amps	mV		mV	Percent		
Condition	Factory set, (1)	Adjustment range	Nom. input, 25°C	50°C	50°C 60°C 71°C		25°C nom input, rectangular fixed	nom input max load p-p typ max		d-c to 50MHz	nom input max load typ	
30 WATT MOD	ELS				5	Size: 1.	38" H x 3.74"	W x 5.	12" D	Net we	ight: 0.9 lb.	
ERD 5-6-24 ERD 5-6-48	5	4.0~ 5.5	6.0~ 6.9	6.0	4.2	2.4	6.6~ 7.1	30	50	100		
ERD 12-2.5-24 ERD 12-2.5-48	12	8.4~13.2	13.7~15.7	2.5	1.8	1.0	2.8~ 3.1	50	80	170	77%	
ERD 15-2-24 ERD 15-2-48	15	12.0~16.5	17.0~19.5	2.0	1.4	0.8	2.3~ 2.6	50	80	200		
ERD 24-1.3-24 ERD 24-1.3-48	24	16.8~26.4	27.0~30.5	1.3	0.9	0.5	1.5~ 1.8	50	100	290		
ERD 48-0.6-24 ERD 48-0.6-48	48	32.6~52.8	55.0~63.0	0.6	0.4	0.2	0.7~ 1.0	60	150	530		
60 WATT MODELS Size: 1.69" H x 3.74" W x 6.3" D									Net we	ight: 1.2 lb.		
ERD 5-12-24 ERD 5-12-48	5	4.0~ 5.5	6.0~ 6.9	12.0	8.4	4.8	13.2~13.8	30	50	100	24V input: 79% 48V input: 82%	
ERD 12-5-24 ERD 12-5-48	12	8.4~13.2	13.7~15.7	5.0	3.5	2.0	5.6~ 6.0	50	80	170		
ERD 15-4-24 ERD 15-4-48	15	12.0~16.5	17.0~19.5	4.0	2.8	1.6	4.5~ 4.9	50	80	200		
ERD 24-2.5-24 ERD 24-2.5-48	24	16.8~26.4	27.0~30.5	2.5	1.8	1.0	2.8~ 3.1	50	100	290		
ERD 48-1.2-24 ERD 48-1.2-48	48	32.6~52.8	55.0~63.0	1.2	0.8	0.5	1.4~ 1.7	60	150	530		
150 WATT MOD	ELS				S	ize: 3.	15" H x 3.74"	W x 8.	66" D	Net we	ight: 2.6 lb.	
ERD 5-30-24 ERD 5-30-48	5	4.0~ 5.5	6.0~ 6.9	30.0	21.0	12.0	33.0~35.0	30	50	100	24V input: 79% 48V input: 81%	
ERD 12-12-24 ERD 12-12-48	12	8.4~13.2	13.7~15.7	12.0	8.4	4.8	13.4~14.4	50	80	170		
ERD 15-10-24 ERD 15-10-48	15	12.0~16.5	17.0~19.5	10.0	7.0	4.0	11.2~12.0	50	80	200		
RD 24-6-24 RD 24-6-48	24	16.8~26.4	27.0~30.5	6.0	4.2	2.4	6.8~ 7.3	50	100	290		
ERD 48-2.8-24 ERD 48-2.8-48	48	32.6~52.8	55.0~63.0	2.8	2.0	1.1	3.3~ 3.6	60	150	530		

⁽¹⁾ Nominal input, maximum load, 25°C

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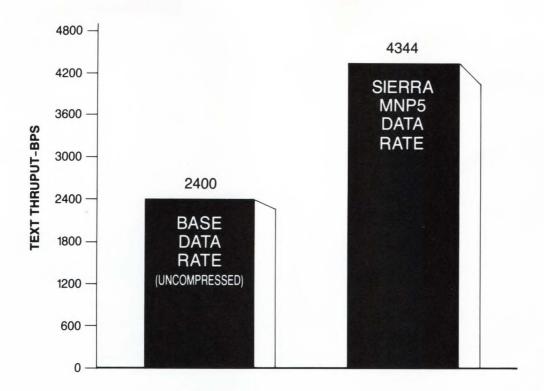




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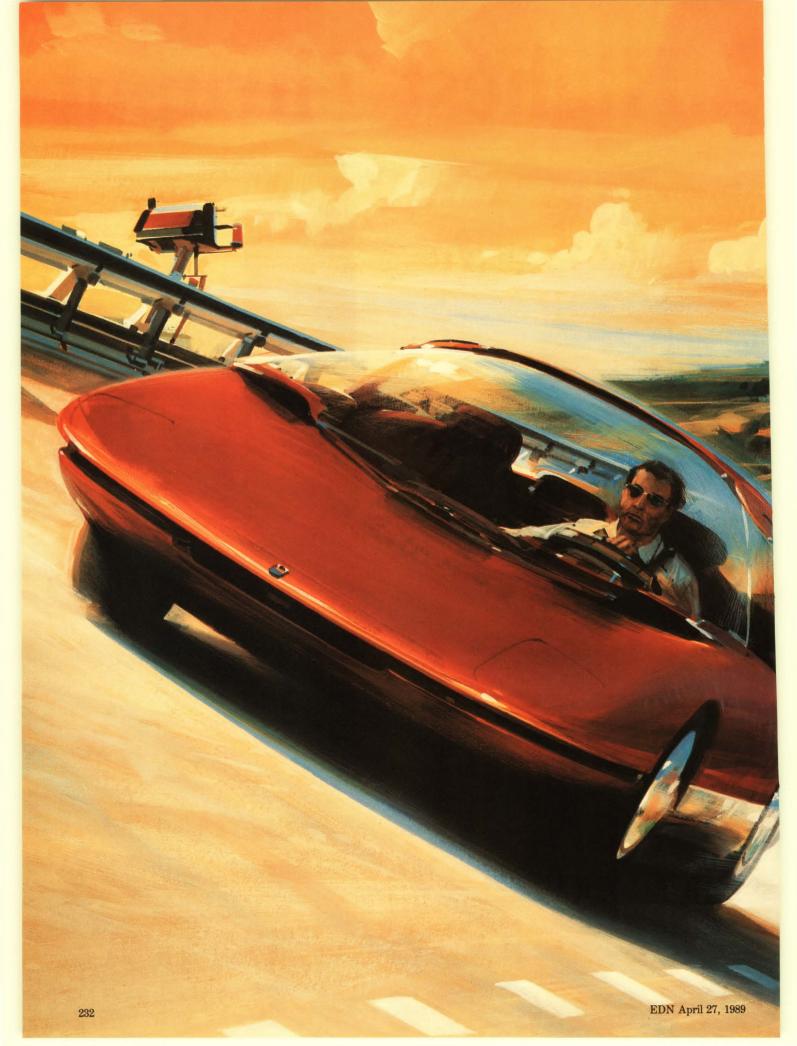
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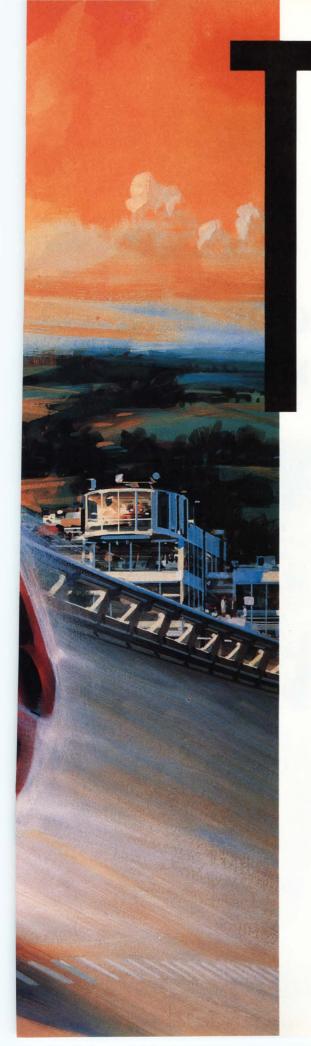
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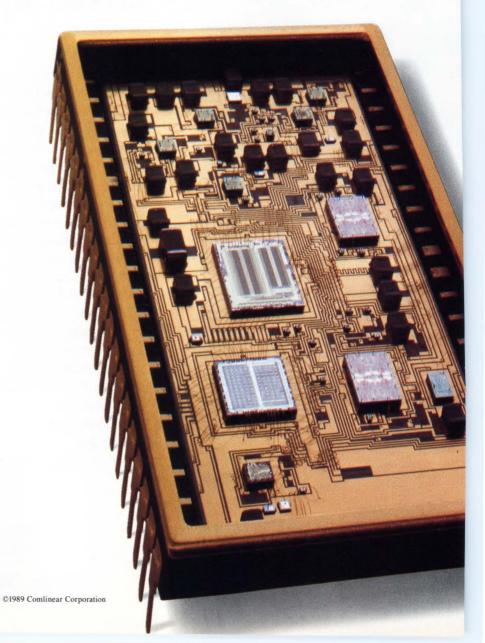
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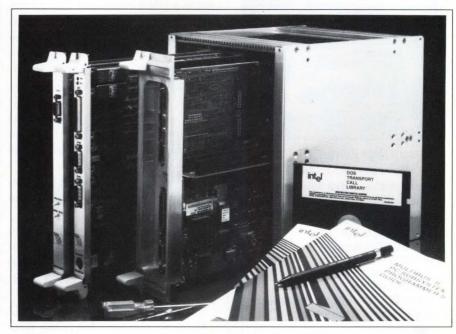
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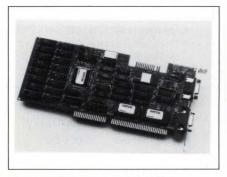


PC/XT and compatible boards. The system includes an Award BIOS and runs with PC-DOS or MS-DOS. CPU board, \$4700; companion board, \$1295; adapter board, \$995; 2-slot backplane, \$195; 4-slot

backplane, \$295.

Intel Corp, Literature Dept, #AP-13, Box 58065, Santa Clara, CA 95052. Phone (800) 548-4725.

Circle No 350



GRAPHICS ADAPTER

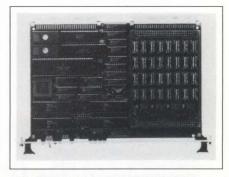
- Provides 1024×768-pixel resolution with 16 colors
- Automatically switches between IBM PC/XT and PC/AT buses

The SuperVGA 16-bit graphics adapter is a VGA card for the IBM PC, PC/XT, PC/AT and compatible computers. The adapter provides 1024×768 -pixel resolution with 16 colors for interlaced and noninterlaced monitors and comes in two models: the 5300, which has 256k

bytes of display RAM, and the 5400, which has 512k bytes of display RAM. (You can upgrade the 5300 to a 5400 by purchasing an extra 256k bytes of RAM.) Both models come with drivers for AutoCAD, Ventura Publisher, Lotus 1-2-3, and Windows. Each board has an autosensing capability to automatically switch between an 8-bit PC/ XT bus and a 16-bit PC/AT bus. The 5400 offers the following resolution and color combinations: 1024×768 pixels with 16 colors, 800×600 pixels with 256 colors, and 640×480 pixels with 256 colors. Both products support digital and analog monitors. 5300, \$499; 5400, \$699.

Genoa Systems Corp, 75 E Trimble Rd, San Jose, CA 95131. Phone (408) 432-9090. FAX 408-434-0997. TLX 172319.

Circle No 351



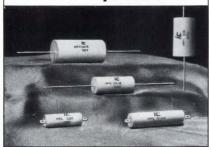
PARALLEL I/O BOARD

- Has 64 configurable parallel I/O lines with handshake facilities
- Includes an onboard 68000 μP and a DMA controller

The SYS68K/IPIO-1 parallel I/O board includes an onboard $68000~\mu P$ and can offload parallel I/O control tasks from VME Bus CPUs. A piggyback board accommodates the board's 64 I/O lines. You can select from a range of piggyback boards that allow you to configure the I/O



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Type MPH and MPL axial lead High Current capacitors feature flame retardant wrapped and filled construction and meet the specifications of MIL Std. C-55514/9. Type MPL is designed with tinned lug terminals for high current (30A) applications. Offering superior environmental performance up to +105°C without voltage derating, Type MPH and Type MPL are excellent replacements for polycarbonate dielectric capacitors. The self-healing design provides excellent transient and surge protection. Non-inductive extended foil metallized windings are electronically welded to lead wire terminations, providing high ripple current and dV/dt ratings for pulse circuits along with rugged mechanical performance. Designed for operation at 20 to 100KHz min. with rated RMS ripple current. They are perfect for modern SMPS designs.



COMPUTERS & PERIPHERALS

lines with relay, optocoupler, or TTL-level interfaces. The board includes a DMA controller that allows you to set up high-speed data transfers between the I/O port and the board's 128k bytes of onboard, zerowait-state, dual-port static RAM. Communication between the host system's CPU and the SYS68K/ IPIO-1's onboard µP is also via this dual-port RAM. The board has an EPROM-resident real-time kernel based on the company's VME-PROM real-time kernel for processing commands that are sent by the host CPU. DM 2995.

Force Computers GmbH, Daimlerstrasse 9, 8012 Ottobrunn/Munich, West Germany. Phone (089) 600910. TLX 524190. FAX 089-6097793.

Circle No 352

Force Computers Inc. 3165 Winchester Blvd, Campbell, CA 95008. Phone (408) 370-6300. FAX 408-374-1146.

Circle No 353

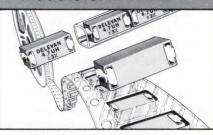
VME A/D BOARD

- Samples at 300 kHz and has 12bit resolution
- Contains a 68010 µP and 64k bytes of dual-port RAM

The DVME-601E, an A/D board in a 6U VME form factor, contains a 12-bit A/D converter that can sample 16 single-ended or 8 doubleended inputs at 300 kHz. The board also contains a 68010 µP that can access one port of a dual-port RAM; the other port services the VME Bus. The board has 64k bytes of EPROM that is expandable to 128k bytes, and its µP can access 64k bytes of local RAM. Other peripherals include an interrupt controller, an RS-232C port, five TTL I/O ports, three timer outputs, and two timer-counter inputs. The board comes with executive and monitor firmware supplied in EPROM. Using the host, you can download user-written code through the dualport RAM or from the RS-232C

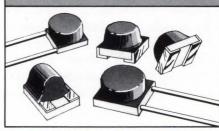
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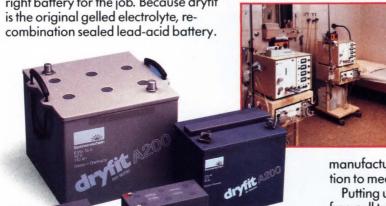
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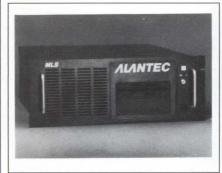
USA: DIGELEC INC., 22736 Vanowen Street Canoga Park, CA 91307 Tel: (800) 367-8750 In CA: Tel: (818) 887-3755 Fax: (818) 887-3693

COMPUTERS & PERIPHERALS

port. Sample software drivers in both C and assembly language are supplied on the floppy disk. \$2195.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX 508-339-6356. TLX 174388.

Circle No 354



LAN SWITCH

- Connects local-area networks using a 160M-bps data rate
- Connects LANs 10 km apart using fiber-optic links

The Multi LAN Switch Ethernet bridge can connect several localarea networks (LANs) at a 160M bps data-transfer rate. A patentpending architecture converts an IBM PC/AT bus into a packetswitching bus to provide the highspeed operation. The unit can connect as many as 16 LANs in one building or it can connect LANs as far apart as 10 km by using fiberoptic cable. A network manager can dynamically forward packets to each LAN segment based on protocol types, source or destination address, packet length, broadcast identifiers, or TCP/IP connection requests. The network administrator can isolate traffic or enforce security, such as in applications where network segments can send but not receive packets from other locations. A 4-port configuration with Ethernet connectors, \$9800; expansion cards, \$2000 each.

Alantec, 101 Hammond Ave, Fremont, CA 94539. Phone (415) 770-1050.

Circle No 355

CIRCLE NO 123

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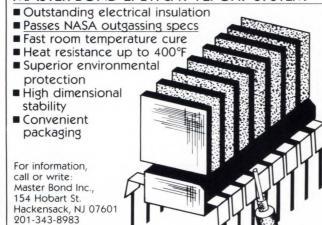


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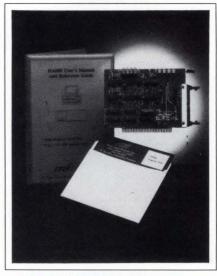
CIRCLE NO 113

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MASTER BOND EP21TCHT-1 EPOXY SYSTEM



COMPUTERS & PERIPHERALS



12-BIT D/A BOARD

- Uses the AD7537 chip; fits IBM PCs, PC/XTs, and PC/ATs
- Provides two channels of analog output

The DA600 12-bit D/A converter for the IBM PC, PC/XT, PC/AT and compatible computers is based on Analog Devices' AD7537 chip, which contains two D/A converters. Having two converters in one IC package ensures close matching between channels. The board provides two 12-bit analog-output channels that you can optionally upgrade to four channels, and it uses an AD712 precision op amp as an output buffer that provides 1.8-usec settling time to .01% of full scale. The host can control both channels in software including a clear function for generating calibration routines or specialized waveforms. Each board has two jumper-selectable full-scale output ranges of 5 or 10V and includes a manual and a disk with programming examples in Basic, Turbo C, Pascal, and Forth. 2channel version, \$179; 4-channel version, \$239.

Real Time Devices Inc, Box 906, State College, PA 16804. Phone (814) 234-8087. TLX 4948141. FAX 814-234-6864.

Circle No 356

Master Bond Inc. Adhesives, Sealants & Coatings

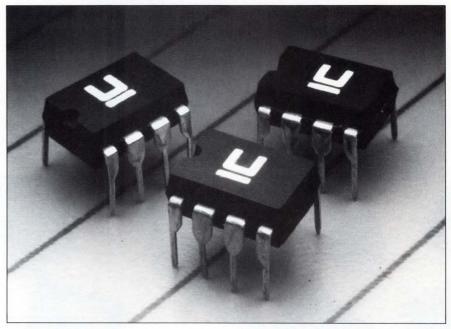


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- Improved industry-standard types
- High-current totem-pole outputs The UC3842A, UC3843A. UC3844A, and UC3845A are improved, pin-compatible versions of the industry-standard 3842/3/4/5 family of current-mode PWMs that are widely used in switched-mode power supplies. The "A" series features a start-up current of <0.5mA, a precise oscillator-discharge current of 8.2 mA, and a 1A peakoutput stage that can sink at least 10 mA at <1.2V during undervoltage lockout (UVLO) for V_{CC} over 5V. The family members differ in their UVLO thresholds and maximum duty-cycle ranges. UC3842A has UVLO thresholds of 16V (on) and 10V (off). The corresponding UVLOs for the UC3843A and UC3845A are 8.5 and 7.9V. The UC3842A and UC3843A can oper-

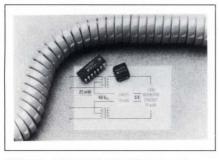


ate to duty cycles approaching 100%; the UC3844A and UC3845A are clamped at a maximum of 50%. The units are available in an 8-pin DIP and 14- or 16-pin SOIC pack-

ages. 8-pin DIP, \$1.32 (1000).

Unitrode Integrated Circuits, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

Circle No 361



ISDN SWITCHMODE IC

- Meets CCITT requirements
- Features high conversion efficiency

The Si9105 high-voltage switch-mode regulator is designed for use in low-power, high-efficiency dc/dc converters. CCITT recommendations for ISDN power supplies call for conversion from 40V down to 5V with 40 to 60% efficiency for the light-load condition. The Si9105 provides typical efficiencies of 64% under light-load conditions, and 88% under full-load conditions. The

CCITT recommends a total power consumption of <25 mW during emergency operation in the power-down state. An ISDN power supply using the Si9105 uses approximately 10 mW, leaving the 15 mW needed for line-activity detection circuitry. 14-pin plastic DIP, \$5.97; 20-pin plastic leaded-chip carrier, \$6.95 (100).

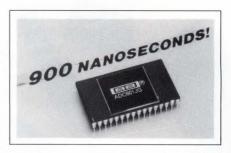
Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 362

12-BIT ADC

- Has 900-nsec conversion rate
- 2-tone IMD is -77 dBc

Specially characterized for dynamic performance, the ADC601 12-bit, successive-approximation A/D converter features a 900-nsec conversion rate. Other dynamic specifications, measured at the Nyquist fre-



quency with the company's SHC804 S/H amplifier, include -68-dBc THD, -77-dBc intermodulation distortion, and a 67-dBc S/N ratio. The ADC601 employs a 2-chip bipolar/CMOS design that permits optimization of both analog and digital performance. Maximum dc specifications include $\pm 0.012\%$ integrallinearity error, $\pm 0.1\%$ offset error, and $\pm 0.2\%$ gain error. 32-pin ceramic DIP, \$79 (1000).

Burr-Brown, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 363

CONTROL PONT

Test and Control Product News from Ziatech Corporation

Spring, 1989

ZIATECH OFFERS WORLD OF IEEE 488 CHOICES



A free, easy-to-use software driver comes with Ziatech's ZT 1444 GPIB interface to PCs.

GPIB hardware supports PCs, PS/2s, STD, MULTIBUS and MULTIMODULE standards

Ziatech's IEEE 488 interfaces are a popular choice of OEMs and end users utilizing GPIB products in their test and measurement designs. The Ziatech interfaces owe their popularity to their cost efficiency, their wide array of software choices and the extensive

technical support capabilities of Ziatech.

GPIB SINCE 1976

Ziatech was the first to bring the IEEE 488 bus concept to microcomputers with its charter

(Continued on page 2)

Software simplifies IEEE 488 control

Ziatech offers a wide array of software drivers and programs to support its IEEE 488 hardware interfaces, including an installable driver called EZ.488 that is offered at no additional charge with Ziatech's interfaces for personal computers.

All of Ziatech's software drivers are available with no recurring license fees for multiple systems, making purchases of Ziatech GPIB interfaces cost-efficient for high volume users.

Ziatech offers two types of installable drivers, both of which allow IEEE 488 interfaces to be configured as controllers or talker/listeners.

(Continued on page 3)

INSIDE

GPIB:

Hard Choices Page 2

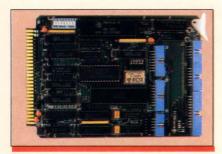
Ziatech's Large Software Menu Page 3

GPIB Control
Gets SmartPage 4



Free software drivers with PC and PS/2 boards -

ZIATECH GPIB BOARDS PROVIDE COST-EFFECTIVE INSTRUMENT CONTROL



ZT 8847 interface for STD systems

(Continued from page 1)

product in 1976, a GPIB interface for MULTIBUS systems. The Ziatech product line now features a number of hardware interfaces for personal computers, the IBM PS/2, STD Bus and MULTIBUS systems, as well as software packages and drivers that simplify system integration.

GPIB FOR THE PC

The most popular GPIB interface in the Ziatech product line is the ZT 1444A. Each interface controls up to 15 GPIB instruments from within an IBM-compatible PC, XT, AT or PS/2 Models 25 and 30. The ZT 1444A offers an optional security device for protecting OEM software. This interface occupies a short slot in a PC, while the ZT 1488A interface requires a full slot because of two additional capabilities, a batterybacked clock/calendar and MULTIMODULE (SBX) expansion. Both GPIB boards come with a free software driver, Ziatech's EZ.488 (see software story, pages 1 and 3).

GPIB FOR PS/2

Ziatech also supports GPIB systems using the IBM PS/2 Models 50, 60, 70 and 80, with the ZT/2 interface. This interface features free software support, an Adaptor Description File for setting system parameters, a "watchdog timer" to help prevent system hang-ups and an optional security device for protecting OEM software.

GPIB FOR STD

As a leading supplier of boardlevel and packaged STD Bus systems, Ziatech offers several options for adding GPIB capability to STD systems. Up to 15 IEEE 488 devices can be interfaced through one STD I/O slot with Ziatech's

ZT 8847 or ZT 8848 GPIB interfaces. Ziatech also offers sinale board computers and integrated systems with GPIB capability. (See story, page 4.)

GPIB FOR MULTIBUS

The ZT 87A IEEE 488 Interface for MULTIBUS systems features data rates of 300 Kbytes per second with on-board DMA utilizing 64 Kbytes of dual-ported RAM.

GPIB MULTIMODULE

Ziatech's zSBX 20 controller brings GPIB control to any system that uses the MULTIMODULE standard, without using an additional I/O slot. (See story, page 4).



ZT/2 interface for IBM PS/2s



ZT 87A interface for MULTIBUS systems

No recurring fee for mulitple use of software drivers -

ZIATECH SOFTWARE INSTRUMENTAL TO GPIB APPLICATION SUCCESS

(Continued from page 1)

EZ.488 - EASY TO USE

EZ.488 is the simplest installable driver to use, with HP 85 compatible syntax and the ability to access IEEE 488 devices from most high-level languages. EZ.488 is the best choice for applications requiring a driver that is accessible from any language. Many OEMs choose EZ.488 for their products because of its flexibility and ease of use.

INSTALL.488 – PC DOS-COMPATIBLE

Like EZ.488, INSTALL.488 uses the resources of PC DOS, but with efficient language interfaces for BASIC, C, Pascal, FORTRAN and Assembly. This driver type is a good choice for system integrators who want to use National Instruments' IEEE 488 interfaces as second sources for Ziatech interfaces. It also allows existing application software written for IBM

and National interfaces to work with Ziatech hardware.

The compatibility of Ziatech's installable drivers with PC DOS-based STD Bus systems (STD DOS) enables system designers to connect STD Bus and PC systems via IEEE 488 interfaces, using identical software in both. It also allows a system designed on a PC or PS/2 to be easily ported over to the more industrial STD Bus.

LINK.488 – FAST DRIVERS LINK TO LANGUAGES

Ziatech offers high-level language linkable software support for both controllers and talker/listeners. This high-performance software, called LINK.488, is designed to provide extremely efficient code for accessing the IEEE 488 bus while maintaining a userfriendly environment. LINK.488, available in versions that support C, BASIC, Pascal and Assembly, is best suited for Original Equipment Manufacturers

(OEMs) whose products provide integral IEEE 488 support. In many cases, once the software is developed, it is placed in EPROM, never to be changed again.

MENU-DRIVEN INSTRUMENT CONTROL

In addition to its software driver support, Ziatech offers software packages from selected companies that enhance the functionality of Ziatech GPIB interfaces.

ASYST, for example, is a completely integrated package allowing full control of a wide assortment of I/O devices with data collection and graphic display capabilities. This package has an interactive, menu-driven user interface which speeds program development and is easy to use. With the ASYST package, highly sophisticated data acquisition programs can be developed, complete with graphical display or plotting capabilities.

ASYSTANT GPIB

ASYSTANT GPIB uses the same user interface as ASYST, but is limited to supporting IEEE 488 I/O. This package allows the user full control of IEEE 488 instruments, combined with full data analysis and graphics display capabilities.

(Continued from page 2)

GPIB LOGIC ANALYZER

Ziatech's ZT 488 is a low cost, handheld logic analyzer that can help eliminate hours of wasted troubleshooting time in building, debugging and servicing IEEE 488 systems.

For more information, circle the response number or return the Control Point postcard.



Ziatech's STD DOS systems run GPIB control software like ASYSTANT GPIB.

Unique GPIB network capability -

ZIATECH INDUSTRIAL COMPUTERS PROVIDE INSTRUMENT CONTROL

Ziatech offers a variety of STD Bus-based industrial computers with GPIB capability for users requiring "smart" GPIB control.

"SLOT-LESS" GPIB

GPIB capability can be added to Ziatech's 80188-based single board STD Bus computers (ZT 8814/15), and 8088-based intelligent control processor (ZT 8830) via the zSBX 20 MULTIMODULE controller. This expansion capability will also be available on Ziatech's soon-tobe-released ZT 8832 I/O control processor. These SBC-IB products allow system designers to expand their IEEE 488 capabilities without using an additional I/O slot.

Ziatech's integrated STD systems, the ZT 300 Industrial Computer and the ZT 1000 Industrial Workstation, can also be easily configured for GPIB-based instrumentation applications.

RACK-MOUNTED COMPUTER

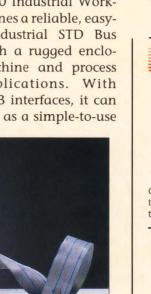
The ZT 300 integrates an STD Bus computer and IBM PC DOS in an enclosure designed for rackmounting. It is available in a diskless configuration for embedded applications, in a PC feature set with video display and keyboard, and as a remote node in an industrial ARCNET network. All of these configurations are available with GPIB capability via an IEEE 488 interface and driver software.

NETWORK EXTENDS GPIB CONTROL

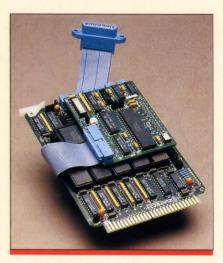
The combination of network and GPIB capability in the ZT 300 results in a powerful instrument controller that extends the geographic limitation of GPIB control. This combination allows other nodes on the network to transparently control GPIB instruments connected to the ZT 300 or ZT 1000, extending the 20-meter GPIB limit to the ARCNET network limit of up to four miles away.

FACTORY FRIENDLY GPIB

The ZT 1000 Industrial Workstation combines a reliable, easyto-operate industrial STD Bus computer with a rugged enclosure for machine and process control applications. With Ziatech's GPIB interfaces, it can be configured as a simple-to-use



Ziatech's integrated STD Bus computers such as the ZT 300 combine ARCNET industrial network cabability with GPIB control.



The SBC-IB, a Ziatech 80188 single board computer with GPIB control via the zSBX 20 MULTIMODULE interface.

instrument controller rugged enough for the factory floor.

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Tokin America Inc.

155 Nicholson Lane, San Jose, California 95134, U.S.A. Phone: 408-432-8020 Fax: 408-434-0375 Chicago Branch 9935 Capitol Drive, Wheeling, Illinois 60090, U.S.A. Phone: 312-215-8802 Fax: 312-215-8804

VOLTAGE REFERENCES

- 10, -10, and $\pm 10V$ outputs
- ± 2.5 to ± 5 -mV accuracy

Supplied in JEDEC-compatible 28-pin LCC packages, the HC2700 Series precision voltage references offer a choice of 10, -10 and ± 10 V models. The devices are available in both industrial (-25 to $+85^{\circ}$ C)

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Hycomp Inc, 165 Cedar Hill St, Marlborough, MA 01752. Phone (508) 485-6300.

Circle No 364

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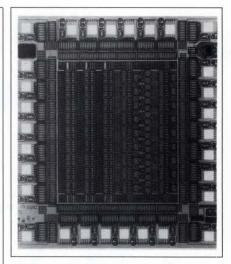
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The MA Series analog/digital semicustom CMOS arrays let IC designers create application-specific circuits that range from 45 gates and 400 MOSFETs to 1150 gates and 2500 MOSFETs. The MA Series consists of eight arrays varying in size from 67×77 to 189×223 mils. Device operation extends from 3 to 14V, and I/Os range from 18 to 84. You can use the devices at internal flip-flop toggle frequencies to 50 MHz and at amplifier bandwidths to 5 MHz. A library of more than 50 digital and 20 analog macrocells is available. Nonrecurring engineering charges vary from \$10,000 to \$50,000, depending on complexity. Delivery, eight to 16 weeks ARO.

Plessey Semiconductors, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900. TLX 4940840.

Circle No 365

POWER SUPPLIES AT YOUR COMMAND.

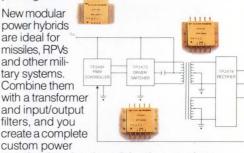


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CIRCLE NO 119

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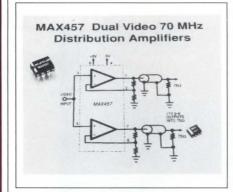


(216) 439-4091

Telex 6502820864 • Fax (216) 439-4093 IOtech, Inc. • 25971 Cannon Road • Cleveland, Ohio 44146

CIRCLE NO 122

INTEGRATED CIRCUITS



VIDEO AMPLIFIER

- Has a 70-MHz bandwidth
- Has dual 75 Ω drive capability Using a silicon-gate CMOS process to achieve high-speed performance,

the MAX457 dual op amp has a unity-gain bandwidth of 70 MHz and can drive two 75Ω outputs. Because of the device's low-input bias current of 100 pA, its low-input capacitance of 4 pF and its high-input impedance of $10^{10}\Omega$, you can tie the two inputs together with minimum loading of the source. Both outputs can simultaneously drive ±1V into a 75Ω-terminated video coaxial cable. The differential phase error is 0.2° typ and differential gain error is 0.5% typ. These values make the device suitable for low-cost video broadcast applications. MAX457 is available in commercial and industrial temperature grades in an 8-pin DIP, an 8-pin SOIC, or an 8-pin ceramic DIP. From \$4.45 (1000).

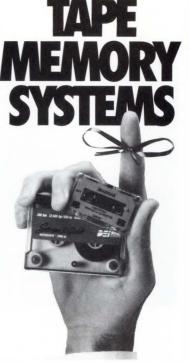
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 366

ENCODER/DECODERS

- Low-power CMOS operation
- Operate from a 5V supply

Fabricated in low-power, highspeed CMOS, the MC145439 and MC142103 encoder/decoder units translate clocked serial data into two streams of return-to-zero digital pulses. The pulses are externally mixed to form a selection of ternary signals for driving transmission



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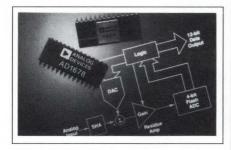
CIRCLE NO 144

INTEGRATED CIRCUITS

lines. Reversing the process translates the two streams of clocked pulses into a single stream of clocked binary data. Encoder/Decoder functions are useful in converting T1 links to clear channels. The devices, which operate from a 5V supply, perform coding and decoding functions independently at clock rates from dc to 9M bits/sec. Both parts perform HDB3 coding/ decoding functions within CCITT G.703 guidelines. The MC145439 comes in a 20-pin DIP, and the MC142103 is available in a 16-pin DIP. Each device, \$7.13 (500).

Motorola Inc, Box 52073, Phoenix, AZ 85072. Phone (512) 928-7364.

Circle No 367



12-BIT ADC

- Features recursive subranging
- Has a 5-usec conversion time

The AD1678 A/D converter uses recursive subranging to deliver a conversion time of 5 µsec for a throughput rate of 200k samples/sec. The AD1678 contains an S/H amplifier. a 12-bit ADC, a reference, a clock, and a processor interface on a single BiCMOS chip. The chip's ac performance includes a 1-MHz typ input bandwidth, a min S/N + D ratio of 72 dB, and a maximum THD and intermodulation distortion of -80dB. The AD1678's S/H amplifier has a 10-M Ω input impedance, thus eliminating the need for external input-signal buffering. A complete digital interface permits a µP or a digital signal processor to read data in either a 12-bit or an 8+4-bit format for 16- or 8-bit buses, respectively. The AD1678, which operates

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CIRCLE NO 147

DID YOU KNOW?

Half of all EDN's articles are staff-written.

EDN

in either a synchronous or an asynchronous mode, accommodates both unipolar or bipolar input signals. The device operates from 5 and \pm 12V supplies. From \$38 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565.

Circle No 368

TELETEXT DECODER

- Provides 2-chip teletext systems
- Includes character sets for thirteen languages

With the addition of a dynamic RAM, the MV1815 single-chip CMOS teletext decoder produces a complete teletext system. By adding more memory, you can produce

A/D Converter

THE STREET

848P8E80-2 1.0-256Hz

Minimum = 2 Sample Rat Roll-off Rate Corner Frequent

Anti – Alias Filter

a teletext system that can store as many as 254 teletext pages. The decoder includes a complete set of level-one teletext functions and also has several level-2 capabilities. In addition, it has an on-chip data slicer, two separate page-acquisition circuits, and RGB color-display logic. Its selectable character sets support thirteen languages, including most European and Scandinavian languages. Around £5 (100,000).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 518000. TLX 449637. FAX 0793-518198.

Circle No 369

Plessey Semiconductors Corp, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900. TLX 4940840. FAX 408-438-5576.

Circle No 370

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BIFET OP AMP

- Has good dc characteristics
- Fast settling time is guaranteed Combining good dc and ac characteristics, the LF401A BiFET op amp is guaranteed to settle to 0.01% of a 10V step in <400 nsec. The standard LF401 carries a spec of 500 nsec. The typical settling time for both parts is 365 nsec. Other ac specs include a minimum gain-bandwidth product of 14 MHz, an input noise voltage of 2.3 µV, a slew rate of 70 V/µsec, and THD of only 0.002%. Maximum dc specs include an input-offset voltage of 200 µV for the LF401A and 500 µV for the LF401; an input bias current of 200 pA at 25°C; and a CMRR of 90 dB. 14-pin DIP, \$9.60 (100).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2274. TLX 346353.

Circle No 371

Searching for a source for Z80180s? Competitively priced... from an American company?

You found it! Zilog from Hall-Mark.



64180Z™ users call Hall-Mark to get both SuperintegrationTM and super values in Zilog controllers.

Instead of reinventing the wheel, improve on it. Add the impact of CMOS and the flexibility of Superintegration of the Z80180 to the proven performance of Z80TM/8080TM and you have a product that's ready to go to market. Fast.

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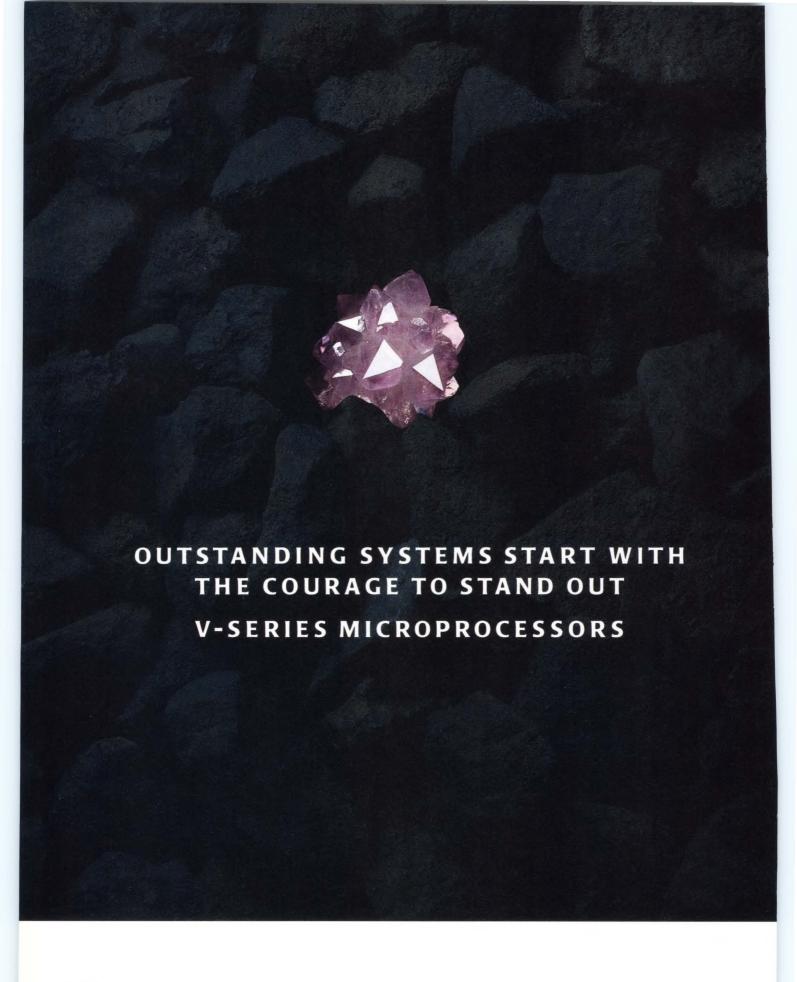
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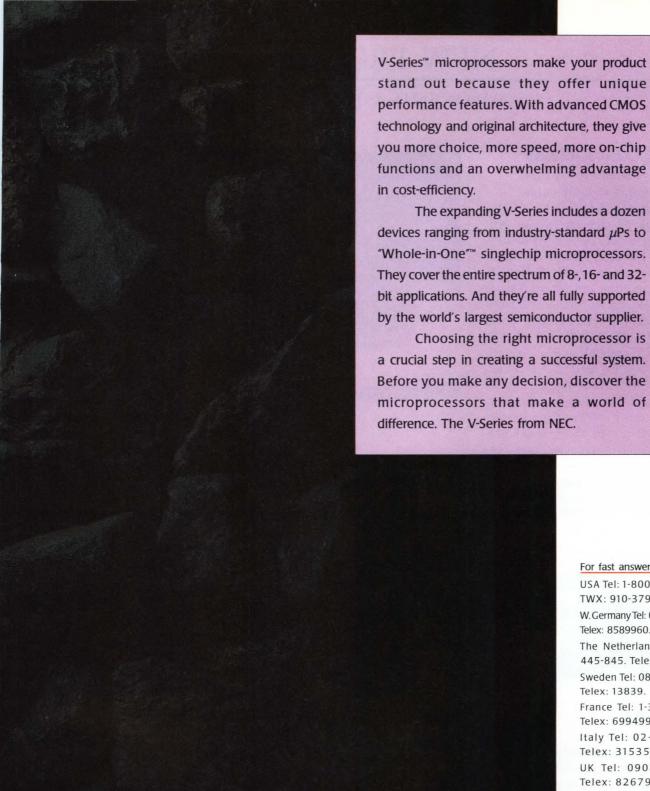
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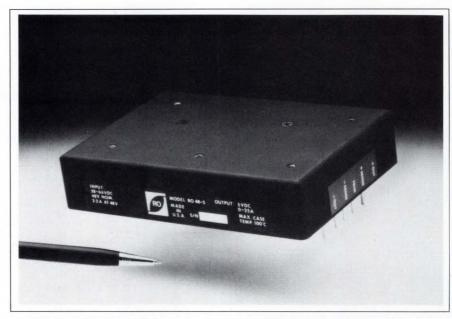
NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

DC/DC CONVERTERS

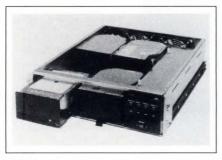
- Require no fan or heat sink
- Feature 125 to 150W output

Units in the RO Series singleoutput dc/dc converters can produce outputs of 125 to 150W at 20°C without the need for a heat sink or a fan. Housed in a $0.98 \times 3.4 \times 4.85$ in. package, the converters feature a 2.5°C/W case to ambient thermal resistance. Converter outputs equal 5V at 25A, 12V at 12A, 15V at 10A, 24V at 6A, and 28V at 5A. The converters feature true N+1 redundancy with current-sharing, paralleling, and hot plug-in capability. Nonshutdown overvoltage protection, logic on/off, short-circuit protection, and overtemperature protection are standard on all units. The converters comply with MIL STD 810D, UL, CSA, and VDE requirements. The converters oper-



ate with inputs of 36 to 66V in the RO 48 Series or 200 to 400V in the RO 300 Series. \$249. Delivery, stock to 60 days ARO.

RO Associates Inc, 246 Caspian Dr, Sunnyvale, CA 94088. Phone (408) 744-1450. FAX 408-744-1521. Circle No 376



CHASSIS

- Holds four drives
- Contains five supplies

The SA-H188 expansion chassis can support four 5½-in. removable Winchester drives. The drives mount on a bracket that's compatible with DEC's drive-mounting shoe. The drive/bracket assembly slides easily in and out of the chassis to provide portability between systems. The chassis contains a front console with write protect and ready switches and LEDs for each drive. The chassis also includes a controller I/O panel to ease the cabling to an ESDI or SCSI disk controller. The

modular power-supply unit contains five 52W modules. Each module powers one of the drives; the fifth module powers the fans and other chassis functions. You can replace any power module without affecting the operation of other drives in the chassis. \$1270.

Sigma Information Systems, 3401 LaPalma Ave, Anaheim, CA 92806. Phone (714) 630-5417. TLX 298607.

Circle No 377

DC/DC CONVERTERS

- Provide 5W from single- or splitvoltage outputs
- Operate over a 2:1 input-voltage range

PT4900 Series 5W dc/dc converters operate over 2:1 input-voltage ranges of 9 to 18V, 18 to 36V, or 36 to 72V. They are available in single-output versions with an output voltage of 5, 12, or 15V, and as dual-output versions with output volt-

ages of ± 12 or ± 15 V. Line regulation is $\pm 0.1\%$ over the full operating input-voltage range, and zero-to full-load output regulation is 0.2% max for single-output versions and $\pm 2\%$ for dual-output versions. An internal Pi filter minimizes conducted RFI. The converters feature an input-to-output isolation voltage of 500V dc, and have output current limiting that allows you to operate them in series or parallel combinations. They have an operating temperature range of -25 to $+71^{\circ}$ C, and an MTBF at 25°C of 120,000 hours. PT4900 converters are housed in $51 \times 51 \times 9.6$ -mm screened cases, £63.

Powertrade GmbH, Lechwiesen Strasse 9, 8910 Landsberg, West Germany. (08191) 46068. FAX 08191-21770.

Circle No 378 Dowty Electronics Corp, Box 250, Brandon, VT 05733. Phone (802) 247-6811.

Circle No 379

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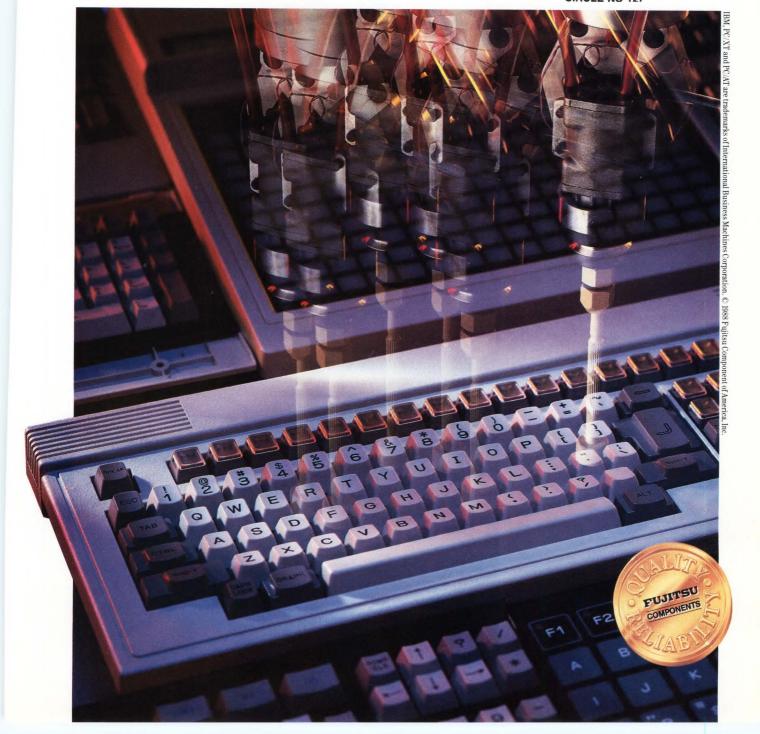
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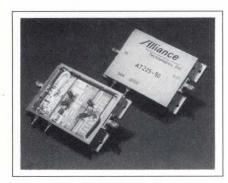
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CIRCLE NO 127



COMPONENTS & POWER SUPPLIES



POWER AMPLIFIER

• Has a 50W output

• Operates from a single supply

The AT225-50 miniature RF power MOSFET amplifier is designed for airborne and military/aerospace applications. Over a bandwidth of 225 to 400 MHz, it provides a 50W output. The amplifier is housed in a hermetically sealed, gold-metallized module, which measures 2.75× 2×0.45 in., excluding mounting flanges. The amplifier requires a 28V power supply and operates over a -55 to +85°C range. The module features feedthrough capacitor gain control and de input pins. The unit is available with SMA or 50Ω pin terminations. \$595 (250). Delivery, stock to 14 weeks ARO.

Alliance Technologies Inc, 16150 NE 85th St, Suite 217, Redmond, WA 98052. Phone (206) 882-4535. FAX 206-882-7517.

Circle No 380

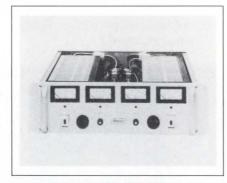
DISPLAY

- Features sidelighting
- Has a 50° viewing cone

Featuring cold cathode fluorescent sidelighting, the FLC640-480 WSUB black and white LCD uses double super-twisted nematic technology. The display's polarizing layers consist of indium tin-oxide coated glass substrates, which produce a high-refractive coefficient of light. The display has a 640×480 dot matrix and features a 50° viewing cone. The display has a 15:1 contrast ratio and features a 15.12-fL brightness. The unit also has a 180msec response time and a viewing area that measures 8.3×6.2 in. The overall panel measurements are 11.7×8 in. \$575 (1000).

Fujitsu Component of America, 3330 Scott Blvd, Santa Clara, CA 95054. Phone (408) 562-1000.

Circle No 381



POWER SUPPLIES

- Offer redundant operation
- Current outputs to 61A

This line of power systems includes 27 models, which provide outputs of 5 to 120V dc at current levels ranging to 61A. Each system consists of a 19-in. rack, containing two modular supplies. The supplies are configured to provide the required output to the load even if one supply should fail. You can remove a defective supply while the host system remains in operation. Each supply contains an overvoltageprotection circuit as well as a voltage-monitoring circuit that operates a relay. The relay contacts are available for use in controlling an external alarm or other circuitry. Built-in alarms are available as an option. \$1095 to \$2795.

Acopian, Box 638, Easton, PA 18044. Phone (800) 523-9478.

Circle No 382

MAP CABLES

- Meet IEEE-802.4 requirements
- Feature EMI shielding

These 75Ω coaxial cables for MAP (manufacturing automated protocol) networks meet IEEE-802.4 reguirements and are CL2X rated.

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R.O. Whitesel & Assoc

(PA) (412) 963-6161

Quality

(NY) (315) 682-8885

Components

(716) 837-5430

SOUTHEAST:

SACS

(FL) (407) 857-3650 (407) 391-1034 (813) 577-6819

Design Marketing & Assoc.

(TX) (214) 480-8151 (504) 542-1115 (512) 263-9151 (713) 550-3318

SACS

(NC) (919) 859-9970

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(TN) (615) 694-9476

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Circuit Sales, Inc. (N.IL) (312) 773-0200 (WI) (414) 784-7773

Comprehensive Technical

(MN) (612) 941-7181 Sales

Hill & Company

(W.MO) (314) 432-1136 (KS) (816) 561-2593

C.H. Horn & Assoc

(IA) (319) 393-8703 John Macke Co. (S.IL)(E.MO) (314) 432-2830

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(MI) (616) 942-5420 (MI) (616) 983-7337

WEST:

Compass Marketing & Sales

(NM) (505) 888-0800 (AZ) (602) 293-1220 (602) 996-0635

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(CA) (415) 367-9000

N.R. Schultz Company

(WA) (206) 454-0300 (OR) (503) 643-1644

Waugaman Associates

(CO) (303) 423-1020 (UT) (801) 261-0802

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(CA) (818) 700-0933

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Renmark Electronics (E.CD) (416) 881-8844



BEST PERFORMANCE IN A SUPPORTING ROLE.

ASC

ASC Presents First Class Film Capacitors And Technical Support, Second To None.

When you buy high technology film capacitors from ASC, you get all the support you need, absolutely free.

It begins with a fully computerized sales and customer service department authorized to provide extremely competitive prices on volumes large and small. It means you get the highest level of technical support from a nationwide team of

engineers prepared to help you with application specific solutions over-the-phone or at your own facility. And, when it comes to custom or "special orders," well, it's just standard procedure with us. All this, plus "just in time"

deliveries that go out on

time.

Since our acquisition of TRW's film capacitor division, ASC has acquired a reputation for service and support, second to none. By combining strong engineering knowhow, and an even stronger commitment to technical

259

support, ASC has emerged as the fastest growing film capacitor manufacturer in the U.S.

In fact, you'll find we offer one of the most complete lines of high quality, cost effective film capacitors in the world, including: polyester, polycarbonate, polypropylene and polystyrene dielectrics, both metalized and non-metallized, plus oil filled capacitors for lighting and motor run applications.

So, when you want an award winning performance in both product and personnel, call ASC. We'll show you why business is better when it's done right, at home. Call us today at **818/710-8555**.



Sales & Marketing, Canoga Park, California Engineering & Manufacturing, Ogallala, Nebraska ASC, 21541 Blythe Street, Canoga Park, CA 91304

The 1223A cable is designed for broadband and carrier-band applications. It features a #18 AWG solid copper-covered steel conductor and a black PVC jacket. The 1224A cable can accommodate either trunk cable or carrier-band transmissions. It has a #14 AWG solid conductor and a PVC jacket. Both cables feature a shield design that provides effective protection against EMI. The double-layer foil shield is bonded to the dielectric core, followed by an aluminum braid and an overall copolymer mylar foil. The outer foil has a shorting fold that provides metal-to-metal contact to maximize shield effectiveness. The cables are available in 1000-ft putups. 1223A, \$220.65; 1224A, \$377.25.

Belden Wire and Cable, Box 1980, Richmond, IN 47375. Phone (800) 235-3364.

Circle No 383



KEYBOARD ENCODER

- Provides IBM PC-compatible or ASCII output codes
- Operates with a range of keyswitch technologies

The Input universal encoder translates as many as 90 individual keyswitch positions into IBM PC, PC/XT, or PC/AT keyboard codes, or ASCII codes. It requires no programming other than the setting of

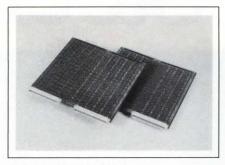
DIP switches to its operating mode. In the PC modes the encoder produces PC-compatible upstroke and downstroke codes at TTL output levels. In the ASCII mode you can select TTL, RS-232C, or RS-423 output levels. Operating at TTL or RS-423 output levels, the encoder only requires one 5V supply. The unit is fully enclosed in an ABS plastic case that you can mount directly behind the company's Input range of sealed keyboards, or within standard Eurocard packaging systems. The encoder works with a variety of commonly used keyboard technologies, including touch-sensitive membrane switch panels. £70.

Keymat Technology Ltd, 14 Bentinck Court, Bentinck Road, West Drayton, Middlesex UB7 7RQ, UK. Phone (0895) 431421. FAX 0895-431132.

Circle No 384

This is how others see LCDs.





SOCKET BOARDS

- Designed for Multibus II applications
- Feature a high-density layout
 These 6U×220-mm wire-wrap
 socket boards are designed for Multibus II applications. They feature
 a high-density layout that supports
 both FAST (Fairchild advanced
 Schottky TTL) and ECL in all sizes
 of DIPs at maximum packing density. The board layout imposes no
 predetermined device location restrictions. Two versions are available—the P/N 031-108-xx, which

has no pin-grid-array (PGA) areas, and the P/N 031-109-xx, which includes PGA areas. The PGA area has a 26×77-pin pin-grid pattern on 0.100-in. centers. The 4-layer boards are constructed of copperclad epoxy laminate FR-4 and are available with a choice of finishes and wrap-pin lengths. Boards with 3-level wrap pins: P/N 031-108, \$595; P/N 031-109, \$617.

Hybricon Corp, 12 Willow Rd, Ayer, MA 01432. Phone (508) 772-5422. TWX 710-347-0654.

Circle No 385

FILTERS

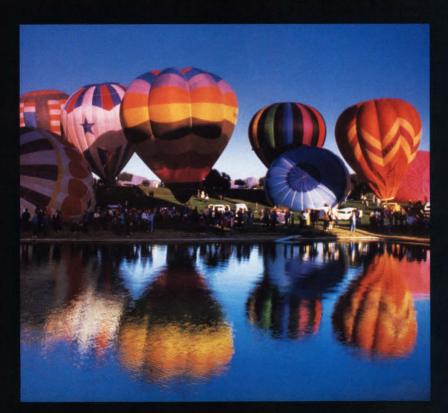
- Housed in surface-mount packages
- Reject high-frequency noise EPA120G RF filters reject noise transfer between the cable and keyboard of personal computers. Each module contains a 4-line common-

mode filter whose inputs and outputs are interchangeable. The filters exhibit an impedance of 425 to 637Ω at 50 MHz and 421 to 631Ω at 70 MHz. At 30 and 100 MHz, the filter's impedance measures 326 to 489Ω and 328 to 540Ω , respectively. Filter characteristics include a 1A/ winding max dc current and a 45°C temperature rise at 25°C ambient. The devices undergo a 500V highpotential test. The units are housed in an 8-pin transfer-molded packwhich measures 0.25×0.78 in. and is compatible with automatic insertion equipment. \$1.04 (1000). Delivery, stock to six weeks ARO.

PCA Electronics Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761. FAX 818-894-5791.

Circle No 386

This is how HITACHI sees LCDs.



Today's LCD world is moving from monochrome to color. Hitachi innovation and world leadership continue with exciting new *color LCD* technology: our brilliant new *TFT Flat Panel Color Display* offers breathtaking clarity, sharpness and vibrant color saturation that must be seen to be believed. Or choose the new *color DSTN LCD* for more cost-sensitive applications.

The future of LCD technology? It's perfectly clear. It's Hitachi.

For more information about exciting new Hitachi color and monochrome LCDs, call or write today.



Hitachi America, Ltd. Electron Tube Division 300 N. Martingale Road, Suite 600 Schaumburg, IL 60173 1-312/517-1144

CIRCLE NO 130

Steel,

NCR

ASICs have become an integral part of today's automotive products.

Improving performance.

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Enhancing driver safety and convenience in ways unimaginable just a few years ago.

In this very demanding industry, on the most unforgiving proving grounds, NCR has earned an enviable reputation for first-pass success, responsive service and high quality.

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To kick the tires on our automotive, commercial and military ASIC libraries, call today: 1-800-334-5454.

NCR Microelectronics, 1700 South Patterson Blvd., Dayton, Ohio 45479.

CIRCLE NO 131

Creating value



Style & Silicon.

Electronic Instrument Cluster Mixed mode system-on-a-chip replaces traditional 2-to-3 chip discrete implementations. Includes a 68HC05 Light Controller Chip Single chip solution includes all the microprocessor core, plus memory, digital, analog and memory functions to analog functions and digital glue logic. control headlights, parking and fog Design Turn: 26 weeks. lights. Provides exit delay timer and allows manual control of exterior lights from driver door. Design Turn: 14 weeks. **Keyless Entry** Chip contains EEPROM supercell that provides direct write capability for flexible security code generation. Ten years data retention and 10,000 read/ write cycles for harsh automotive environment. Can be configured for dual or single supply programming. Design Turn: 14 weeks.

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NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

C CROSS-COMPILER

- Runs on VMS, Unix, or MS-DOS host computers
- Generates code for MC68000family target systems

CrossCode C, an optimizing C cross-compiler, lets you develop software for target systems based on one of the MC68000-family processors. The compiler runs on all members of the VAX family under VMS or Unix and on IBM PCs, PS/ 2s, and compatibles, generating identical object code regardless of the host architecture. It generates ROMable object code for all members of the MC68000 family, including the 68020 and 68030 processors, the 68881 and 68882 numeric coprocessors, and the 68851 memorymanagement unit. You can share source- and object-code files across systems; for example, CrossCode linker running on a VAX can link object files that were generated by the CrossCode compiler running on a PC or PS/2 host. The package includes a Motorolacompatible assembler, a linker, a librarian, and a library of more than



47 C functions. You also get a universal downloader that converts your object code to Motorola S records, Intel Hex records, or a variety of other industry-standard file formats for downloading to a target system or to an EPROM program-

mer. VAX host for the MicroVAX 2000, from \$1595.

Software Development Systems Inc, 4248 Belle Aire Lane, Downers Grove, IL 60515. Phone (312) 971-8170. FAX 312-971-8513.

Circle No 391

80960 TOOLS

- Allow you to develop software for the 80960 controller
- Run on MS-DOS, Sun-3, and VAX hosts

The ASM-960 cross-assembler and iC-960 C cross-compiler allow you to develop software for embedded systems based on the vendor's 80960 microcontroller. Different versions of the cross-assembler and cross-compiler run on IBM PCs and PS/2s under MS-DOS, on Sun-3 workstations under Unix, and on VAX and MicroVAX systems under Unix. Support services include training classes and workshops, onsite and telephone consulting, and hardware maintenance contracts. ASM-960 cross-assembler. \$1950:

iC-960 cross-compiler, \$1550; packaged together, \$3150.

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone local office.

Circle No 392

ROM-RESIDENT OS

- Equivalent to MS-DOS 2.x
- Boots up on a standard IBM PC and runs .EXE and .COM files ROM-DOS is a small, modifiable ROM-resident operating system that is equivalent to MS-DOS 2.0 and higher. It boots up on a standard IBM PC and operates directly from ROM. (It does not have to be downloaded to RAM.) ROM-DOS occupies only 29k bytes of ROM for all functions, and less if some func-

tions are not needed; you can use it with the vendor's standard BIOS or with the vendor's miniBIOS, which occupies only 3k bytes of ROM. The miniBIOS provides support for a hardware timer and serial ports (one of which can serve a remote console). The development kit lets you customize the OS to include only the functions that are needed by the target system; you can link application programs and load them into ROM with the OS and miniBIOS. Development kit, \$495; source-code license, \$5000; firmware, \$6/copy (5000).

Datalight, 17505 68th Ave NE, Suite 304, Bothell, WA 98011. Phone (206) 486-8086.

Circle No 393



Not only does Signetics offer 3 more I/O ports than the 80C51, we also do windows.

At first glance, it's easy to see why our new SC87C451 offers you a rare window of opportunity.

It's called EPROM flexibility.

And it comes in both UV and OTP EPROM versions that cut costs and save time in system development. Especially when you consider that it's fully supported by the Signetics development system.

The 87C451 gives you seven I/O ports for advanced applications. You'll find up to 60 I/O lines—28 more than on the standard 80C51.

Other 87C451 features include a "mailbox" interface for parallel communications, which gives you the ability to use port #6 for handshake data transfers. For added flexibility, the 87C451 also comes in ROM and ROMless versions, as well as in 12- and 16-MHz frequencies, and commercial and extended temperature ranges.

The 87C451 is just one part of our large and growing family of 80C51 derivatives. We also offer a 24-pin 80C51 microcontroller in ROM, UV or OTP EPROM. As well as parts with on-chip A/D that are available now. Each one is fully compatible with the 80C51 instruction set.

We're Signetics. We've got the guts—those essential microcontrollers to improve system performance. For a free '451 Microcontroller Information Packet, call us at (800) 227-1817, ext. 993D.

For surface mount requirements and military product availability, contact your local Signetics sales office. Learn the advantages of window-shopping at Signetics.

One standard. Odefects.

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PLOT-FILE EDITOR

- Lets you view, edit, and print HPGL plot files
- Features include scaling, rotating, and scrolling

PlotView 2.0 is a utility program for viewing, editing, and printing plot files in HPGL format. The program operates under Microsoft Windows so that you can view HPGL plot files while running other applications. You can display a plot, output it to a graphics printer, or paste an image into other documents. New features include cut-

ting and pasting, selection of pen colors and widths, and unrestricted input-file size. The program also features scaling, rotating, and scrolling; zooming in and out; the emulation of five different plotters; and the ability to control laser, inkjet, and other graphics printers. \$79.

Ajida Technologies Inc, 613 Fourth St, Santa Rosa, CA 95404. Phone (707) 545-7777. TWX: 650-363-9045.

Circle No 394

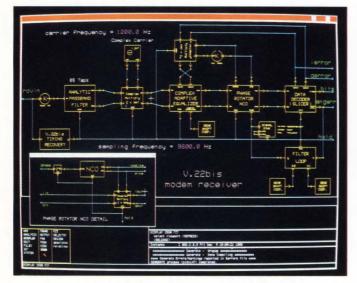
REAL-TIME ADA

- Lets you develop software on Sun or Mizar workstations
- Real-time OS lets you run code on SPARC or 68000 systems

The VADSWorks Ada software package combines the Verdix (Chantilly, VA) Ada Development System (VADS) and Wind River

(Emeryville, CA) Systems' VxWorks real-time operating system. This combined package can run on Sun-3 and Sun-4 workstations or on the vendor's Hybrid Ada Development System. You can use VADS to develop and debug your code; the package includes a window- and mouse-based source-level debugger that lets you debug multiple tasks in separate windows. The VxWorks operating system for realtime, multitasking target systems provides task-state control, intertask communications and synchronization, and performance-analysis features. Networking features allow programs running on a realtime system to communicate with other target systems or with multiple host computers. The VADS-Works development subsystem is based on the Sun-3 Eurocard set, and includes a 20-MHz 68020 processor; 4M bytes of dynamic RAM;

AT LAST, DESIGN DSP



Use our Block Diagram Editor to graphically capture and edit your DSP or communications design algorithm on-screen with hierarchical function blocks.

AND THEN TEST IT



Automatically simulate your block diagram with the Simulation Program Builder, all with just a few clicks of a mouse.

266 EDN April 27, 1989

an MC68881 numeric coprocessor; SCSI, Ethernet, and monochrome video controllers; a 141M-byte hard disk; a 65M-byte streaming tape drive; a 19-in. monochrome monitor; and a keyboard and mouse. VADSWorks, from \$27,500; with complete workstation, from \$58,095.

Mizar, 1419 Dunn Dr, Carrollton, TX 75006. Phone (214) 446-2664. FAX 214-522-5997.

Circle No 395

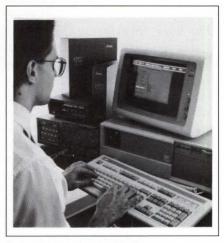
METRIC TOOL

- Measures complexity of dBASE-III and -IV application programs
- Predicts probable number of errors and modification difficulty PC-Metric is a software-measurement package that accepts a dBASE III or dBASE IV application program as input and applies a variety of measurement tech-

niques to the source code. PC-Metric generates reports that estimate the difficulty of understanding and modifying your program, the probable number of programming errors in the source code, and the amount of time required to write the program. The statistics include total and unique operators and operands, length vs predicted length, purity ratio, volume, effort, cyclomatic complexity, and estimated errors. A text report advises you whether each function conforms to recognized standards of excellence. To run PC-Metric, you need an IBM PC or compatible that runs PC-DOS 2.11 or higher. Other versions of PC-Metric are available for C, Cobol, Pascal, Modula-2, Fortran, and Basic. \$199.

SET Laboratories Inc, Box 83627, Portland, OR 97283. Phone (503) 289-4758.

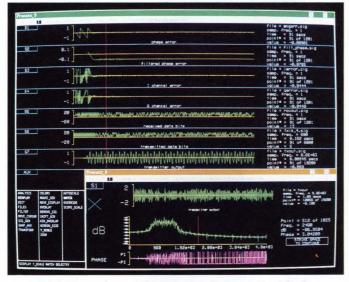
Circle No 396



ANALYSIS PACKAGE

- Includes menu-and commandfile-building tools
- DOS shell lets you perform DOS operations from within the tool
 Asyst version 3.0 is a programmable data-acquisition and -analysis software package that runs on IBM PC and PS/2 computers and compatibles. Several new features make

WITH REAL WORLD DATA



Analyze and modify signals on-screen with the Signal Display Editor. GPIB support allows simulation and analysis with real world data.

WITH ONE TOOL, SPW."

From start to finish, the Signal Processing WorkSystem™from Comdisco Systems is the only comprehensive, integrated software tool that lets you graphically and interactively design, simulate and test digital signal processing systems.

Design complete DSP and communications systems. SPW automates the design cycle and lets you try as many alternatives as you wish – using real world data to test and perfect your design.

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101 California Street, San Francisco, CA 94111

CIRCLE NO 133

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it easy to create customized turnkey systems with simple and effective user interfaces. The Easy Coder feature uses a series of menus to prompt you for parameters and to generate code for a number of common operations such as data acquisition, GPIB control, and data analysis. A new language interface lets you call up routines from within Asyst that you've previously developed in C or Fortran. Menu-building tools let you create menus that can call other menus, run custom macros, perform status checks, or display directories, and the new DOS shell allows you to run application software or perform DOS operations without leaving Asyst. From \$1695.

Asyst Software Technologies Inc, 100 Corporate Woods, Rochester, NY 14623. Phone (716) 272-0070. FAX 716-272-0073.

Circle No 397

CAD SOFTWARE

- Integrates the Ella and Idea VLSI design tools
- Allows high-level circuit description and top-down VLSI design

The Ellalink CAD package lets you transfer design information between the Ella VLSI design system and the Mentor Graphics Idea design-to-fabrication CAD system. By integrating Ella and Idea, the package allows you to perform top-down design of VLSI devices. In the early stages of the design, you can generate schematics using abstract Ella types, allowing you to assess various system architectures. Once you've partitioned the design, Ellalink lets you transfer well-defined circuit blocks to Idea so that you can do detailed design and simulation. Ellalink generates a hierarchical schematic in Mentor Graphics NETED format to translate Ella circuit descriptions into a form that

can be used with Mentor Graphics design tools. The package works with the full Ella language. Behavioral primitives are represented by symbols, and abstract signal types are preserved during the translation. You can set up the translator to use Mentor Graphics library parts rather than Ellalink's normally generated symbols to represent components in the Ella design; this facility allows you to transfer the design to Mentor Graphics lowlevel simulation and layout tools without manual editing. Multiuser license, £8000.

Praxis Systems plc, 20 Manvers St, Bath BA1 1PX, UK. Phone (0225) 444700. TLX 445848. FAX 0225-65205.

Circle No 398

FASTFRAME

Bus-board development in miniature.

Adding to Dage's successful Foundation enclosure family is Fastframe, a completely self-contained miniature bus-based board system. Fastframe offers a full-system capability while its compact design and low cost combine to make it ideal for bench-top prototyping, exhibitions, field service or as a 'one per student' training station.

Compatibility with VME, STE or Multibus II boards provides users with a comprehensive operating environment. Fastframe has its own integral power supply and backplane, and an open-sided construction allows easy access to boards under test or development. External devices are powered via rear-mounted 5 and 12V connectors.

Foundation Fastframe further enhances Dage's wealth of in-depth hardware and software expertise for real-time system builders. For a single source of standard products and full custom facilities make Dage your first choice.

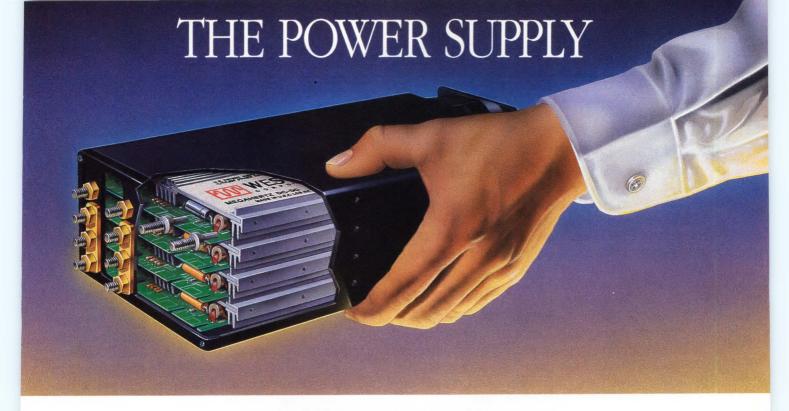


Backplane Systems Technology Division

Dage Precision Industries Incorporated

46701 Fremont Boulevard, Fremont, California 94538, U.S.A. Telephone: (415) 683 3930 Telex: 4990512. Fax: (415) 683 3935





REDEFINED

THE WESTCOR STAKPAKTM. NEW **GENERATION 250 TO 1200 WATT** SINGLE OR MULTIPLE OUTPUT OFF-LINE SWITCHER. 3.2 X 5.5 X 11.4 INCH CASE. FAN-COOLED.

Stack the odds in your favor by designing-in Westcor's 6 watt/cubic inch high power megahertz switcher. Capitalizing on patented and proven megahertz module technology and innovative thermal management techniques, the StakPak provides up to 1200 watts of power at 50°C with 1 to 8 isolated and fully regulated outputs.

For existing designs the StakPak's small size and low profile allow system enhancement without mechanical redesign. Simply replace your open frame switcher with up to 1200 watts of StakPak power or replace your "box switcher" with 2 StakPaks and realize up to twice the power without losing additional space. StakPak power factor correction provides 850 watts of output power from a standard 115 VAC wall outlet. In new designs, more space can be devoted to functionality or the system can be downsized.

The StakPak's 8 module output section can be factory configured in virtually an infinite number of voltage, current and power combinations. Special models providing between 250 to 1200 watts and outputs from 2 to 95 VDC are available.

Other features include outstanding electrical performance; UL, CSA, VDE safety agency approval (in process); variable speed fan option for low ambient noise enviroments and 3 phase or DC input options. Indeed, with unprecedented power density, versatility and new features, the StakPak redefines power packaging. Please contact Westcor for a data sheet, pricing and additional information.



STANDARD 1200 WATT STAKPAK MODELS (110/220 VAC input)

Model	Output Voltage (VDC) and Maximum Current							
	(amperes) per Channel							
	#1	#2	#3	#4	#5			
Single Outpu								
SP1-1801	2@240							
SP1-1802	5@240	Total output power may not exceed						
SP1-1803	12 @ 100			ny model, s				
SP1-1804	15 @ 80							
SP1-1805	24 @ 50		or multiple output. Lower power StakPak models are available.					
SP1-1806	28 @ 42	Please contact the factory.						
SP1-1807	48 @ 25							
Dual Output								
SP2-1801	2@120	5@120						
SP2-1802	5@120	5@120						
SP2-1803	5@120	12@66						
SP2-1804	12@66	12@66						
SP2-1805	15 @ 53	15 @ 53						
Triple Outpu	ıt							
SP3-1801	5@180	12@16	12@16					
SP3-1802	5 @ 150	12@33	12@16					
SP3-1803	5@180	15@13	15@13					
SP3-1804	5 @ 150	15 @ 26	15 @ 13					
Quad Outpu	t							
SP4-1801	5 @ 150	12@16	12@16	5@30				
SP4-1802	5 @ 150	15@13	15@13	5@30				
SP4-1803	5 @ 150	12@16	12@16	24@8				
SP4-1804	5 @ 150	15@13	15 @ 13	24@8				
Five Output								
SP5-1801	5@120	12@16	12@16	5@30	24@8			
SP5-1802	5@120	15@13	15@13	5@30	24@8			
SP5-1802	5@120	15 @ 13	15 @ 13	5 @ 30	-			



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NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

TEST TRANSLATOR

- Adapts programs from Lasar Version 6 to Genrad 2225/35
- Handles go/no-go tests and guided-probe fault diagnosis

Genrad Inc's 2225 and 2235 testers can now run go/no-go and, optionally, guided-probe diagnostic test patterns developed using the vendor's Lasar Version 6 simulator. The Lasar/2225 postprocessor software makes the conversion for you. The translator can incorporate a fault dictionary that allows noninvasive testing—that is, testing without probing any of a board's internal nodes. Many military applications require such an approach. The translator, which runs on DEC V VAX systems under the VMS operating system, includes algorithms for "compacting" test programs to fit the testers' memory. \$22,000; guided-probe diagnostic capability, \$4500; fault dictionary, \$13,500.

Teradyne Inc, 5155 Old Ironsides Dr, Santa Clara, CA 95054. Phone (408) 980-5200.

Circle No 403

WAFER IDENTIFIER

- Reads identifying codes written on wafers with laser
- Provides accuracy greater than 99%

You install the WIS 2000 system's solid-state cameras on units that perform semiconductor wafer-processing operations. With accuracy exceeding 99%, the system reads alphanumeric characters scribed by a laser onto the wafers being processed. The characters uniquely



identify individual wafers for process control. The system includes a 68000-based single-board computer in a chassis, a video monitor, a trackball for operator input, menudriven software, and as many as eight cameras. 8-station system, approximately \$66,000.

Microvision Corp, 12849 Industrial Park Blvd, Minneapolis, MN 55441. Phone (612) 559-2608.

Circle No 404

This pear



is a peach

Our A Series motors, with their pear-shaped gear box, are used in thousands of diverse products. Small wonder. Rated torque up to 150 oz.-in. in a package only 1.63" wide x 2.81" high and a choice of permanent magnet stepping or synchronous operation.

TOUGH, DURABLE GEAR TRAINS

Hurst gear trains are engineered and lubricated for long life at rated loads. They employ hardened steel gears and pinions running on ground, hardened studs. No plastic or fibre parts are used.

SPECS TO FIT YOUR NEEDS

Step angles from 0.025° to 3.6° . Reductions from 300 to 4-1/6. Output speeds @ 200 p/s from 0.83 to 120 rpm. Or, let us know what non-standard specs you require.

DIRECT DRIVE "A" MOTORS, TOO

Both stepping and synchronous direct drive motors are available, many for off-the-shelf delivery from Hurst authorized distributors. Stepping motors provide a choice of 7.5° or 15° step angles. Synchronous motors are available at 300 or 600 rpm.

GET MORE INFORMATION TODAY

For a free, 48-page catalog, call or write Hurst Manufacturing Division, Emerson Electric Co., Box 326, Princeton, IN 47670. 812 385 2564.

Hurst motors make things work...precisely.



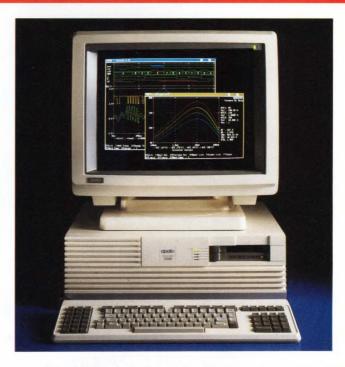
The Standard for Circuit Simulation Now Available on Apollo Workstations

Since its introduction five years ago, MicroSim's PSpice has sold more copies than all other SPICE programs combined. Now PSpice is available for the Apollo Workstation. All these features which have made PSpice so popular are available:

- GaAs MESFET devices, BSIM MOSFET model
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs
- Libraries of over 2,200 common discrete devices

All these PSpice options are available for the Apollo:

- Probe graphics post-processor, for analog and digital waveform display and processing
- Parts parameter extraction program
- Monte Carlo analysis, includes Sensitivity and Worst Cases analyses
- Analog Behavioral Modeling extension, for user-defined linear and non-linear functions
- Digital Simulator extension, for combined analog/digital systems simulation and logiconly simulation, including 690 device TTL/ CMOS libraries



- Digital Files interface, for file-based transfer of digital signals to/from popular logic simulators
- Device Equations source code, for semiconductor devices

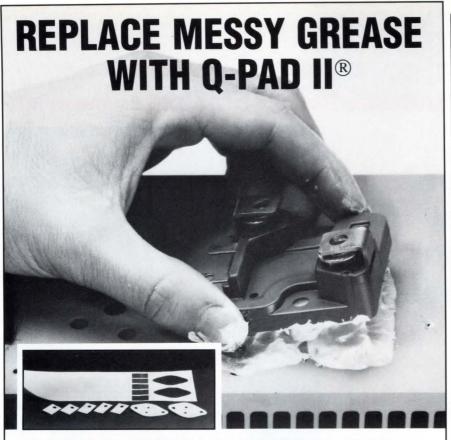
In addition to the Apollo, PSpice is available on these computers:

- PC DOS and OS/2
- Sun 3 and 4 workstations
- VAX/VMS family, including the MicroVAX II
- Macintosh II
- NEC

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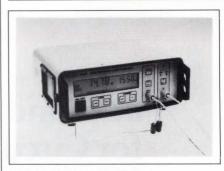
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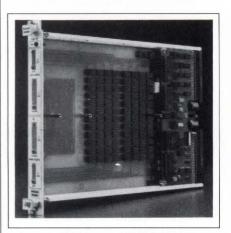
LASER LOSS SET

- Combines power meter and dualwavelength source
- Operates from ac or battery

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INSTRUMENTS

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Circle No 406

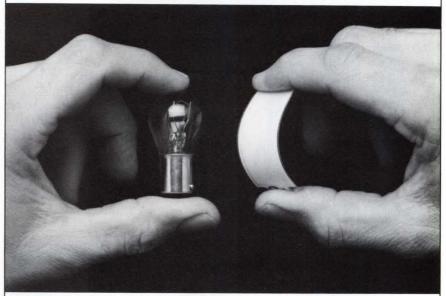


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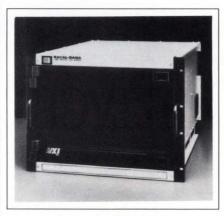


INSTRUMENTS

tured waveforms at the same rate at which it acquired them. The system works with an IBM PC/AT or a compatible computer, VAX/MicroVAX, or a VME-based computer. 40M-sample system, expandable to 160M samples, \$160,000.

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Circle No 407



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- Accommodates C-size modules
- Incorporates 8-output power supplu

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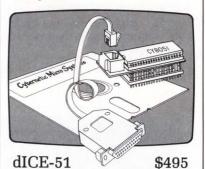
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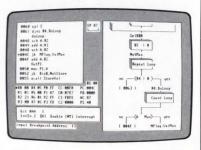
Low Cost 8051 Tools



This Real-Time ICE is the lowest cost and smallest sized full speed 8051 incircuit emulator. Full access to hardware I/O. Includes all debugging features of Sim and dICE below. Fits in shirt pocket.



This reduced-speed in-circuit 8051 debugger provides full access to I/O but will not run real-time. With the same user interface features as Sim8051 below, dICE-51 generates execution profiles during reduced speed execution. (CMOS and MIL also available.)



Sim8051

This software Simulator/debugger allows 'no-circuit', debugging of 8051 code on IBM-PGs. All Cybernetics 8051 debug tools offer multi-window source code displays, symbolic access to data, single key commands, breakpoints, trace, full speed and single step execution, execution profiler, and more.

Other 8051 tools include:

Cross Assembler 8751 Programmer Debugger Demo Disk

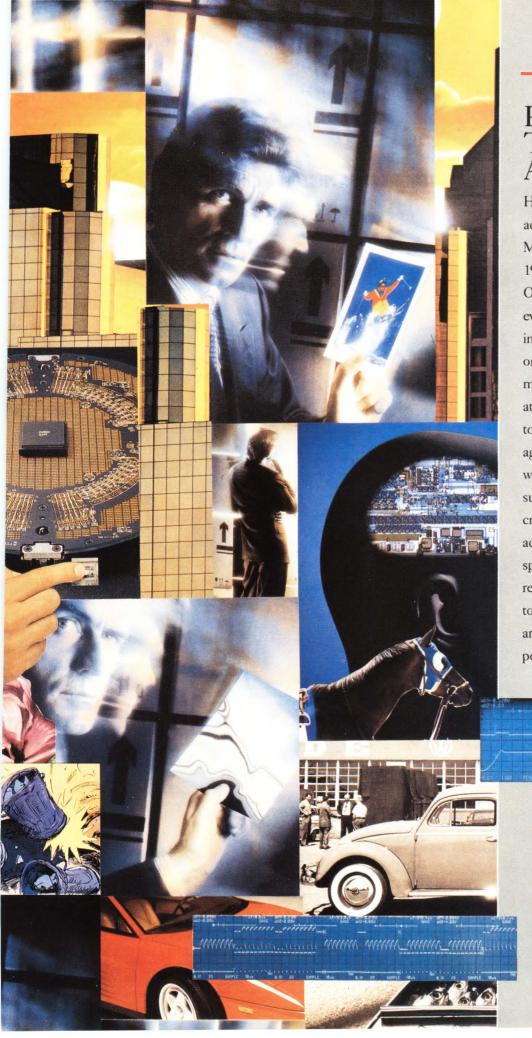
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Presenting The Winning Advertisements

Here are the winning advertisements from EDN Magazine Edition's January 5, 1989 Reader Vote Contest. Our readers analyzed and evaluated the advertisements in the issue to select the ones they judged to be the most informative, helpful and attractive. Congratulations to the advertisers and agencies who combined well-written copy and superior design to create these winning advertisements. And, a special thank you to the readers who took the time to participate. Here then are the outstanding performers.





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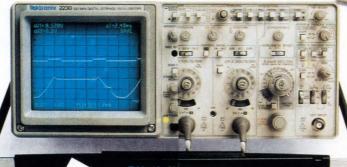
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Record Length	1K/4K Selectable	4K	4K	4K	2K	
Glitch Capture	100 ns	100 ns	100 ns	No	No	
CRT Readout/ Cursors	Yes	Yes	140	No	No	
GPIB/RS-232-C Options	Yes	Yes	Yes	No	RS-232-0 Hardcopy	
Warranty	3-years on labor and parts including CRT					
Price	\$4995	\$3995	\$2995	52395	\$1495	



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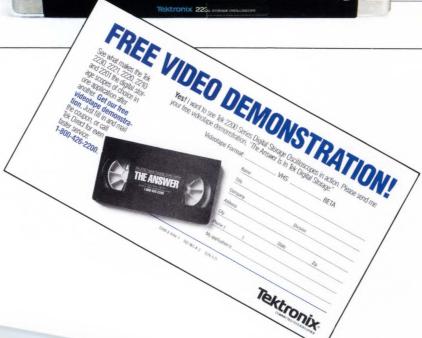
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COMPANY: Altera

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COMPANY: Hitachi America Ltd. AGENCY: Sutter Martin Inc.

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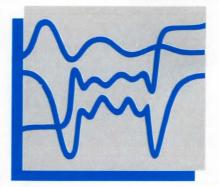


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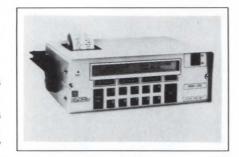
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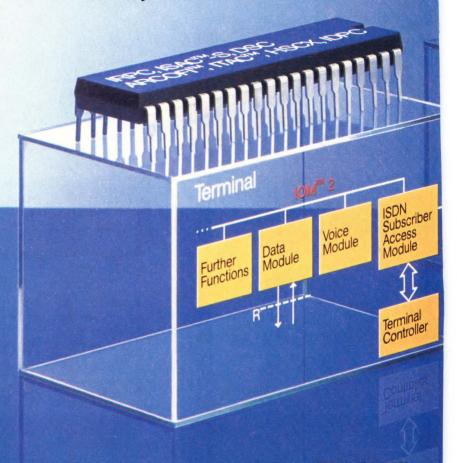
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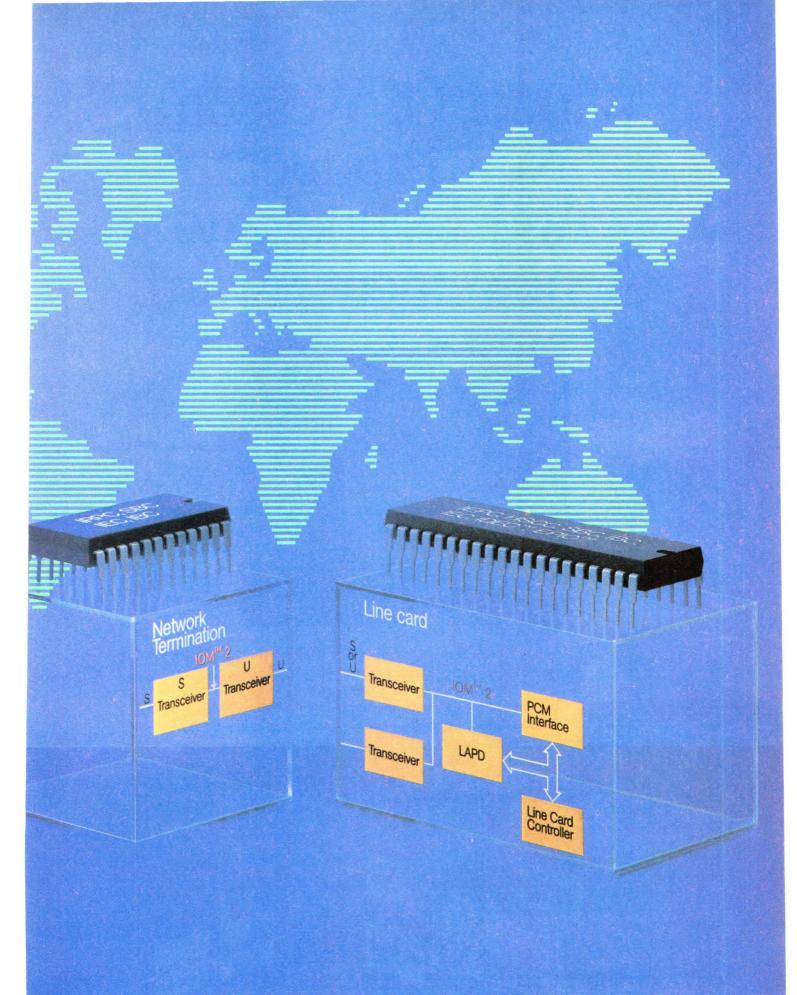
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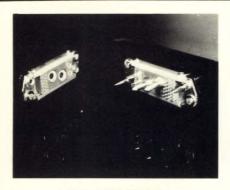
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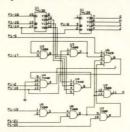
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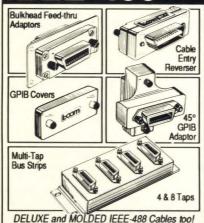
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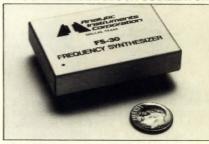
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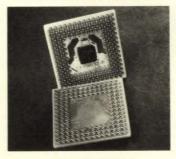
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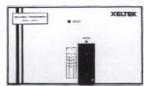
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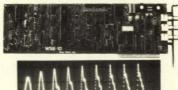
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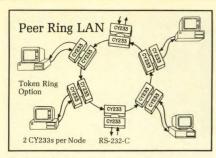
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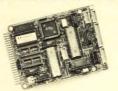


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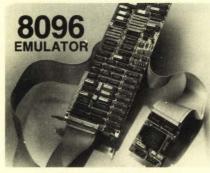
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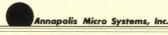
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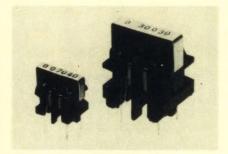


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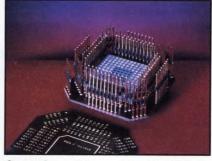


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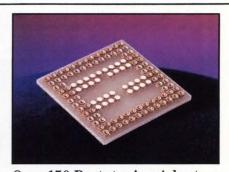


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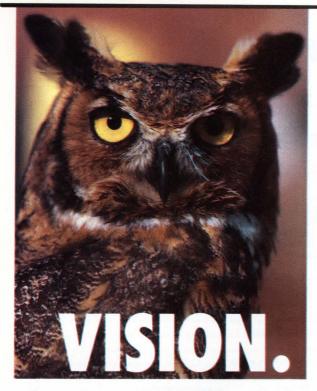
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1989 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News Edition
May 25	May 4	Digital ICs, Computer Peripherals	Closing: May 25
June 8	May 18	Components, Digital ICs	Mailing: June 15
June 22	June 1	Semicustom ICs, Computer Boards	Closing: June 9 Mailing: June 29
July 6	June 15	Product Showcase — Volume I, Power Supplies	Closing: June 22 Mailing: July 13
July 20	June 29	Product Showcase — Volume II, Components	Closing: July 21
Aug. 3 July 13		Integrated Circuits, Computer Boards	Mailing: Aug. 10

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Catalog describes protocol analyzers

The New Wave of Digilog Automatic Protocol Analyzers presents a wide range of protocol analyzers and applications for field service, data-communications operations, and protocol development, including the vendor's recent models for ISDN analysis/emulation. The 20pg catalog has display-screen pictures of protocol decodes, response times, and statistical charts that show how you can use the equipment for a variety of needs. Also included are a variety of turnkey applications for automatic monitoring, testing, and analysis of dataline performance. A specifications list completes the catalog.

Digilog Inc, 1370 Welsh Rd, Montgomeryville, PA 18936.

Circle No 415

Leaflet discusses analyzer-emulation software

The vendor's 4-pg brochure explains its Maestro II multichannel analyzer-emulation software package. The 4-color publication describes the software, listing its functions, features, and hardware prerequisites. The vendor also offers a demonstration disk of the software.

EG&G Ortec, 100 Midland Rd, Oak Ridge, TN 37831.

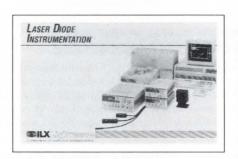
Circle No 416

Package helps you evaluate circuit-design series

This kit for qualified design engineers contains software and a 60-pg illustrated tutorial guide, which describes the Series II Tango-PCB and Tango-Route design-software programs. The guide details features such as pop-up menus, user-definable macros, on-screen prompts, context-sensitive help, and "Hot Spot" and "Speed Palette" aids.

Accel Technologies Inc, 7358 Trade St, San Diego, CA 92121.

Circle No 417



Fold-out focuses on laser-diode instruments

The vendor's 6-pg fold-out brochure features three recently released products for laser-diode instrumentation and highlights its expansion into custom-built laser-diode test systems. The pamphlet provides specifications, illustrations, and prices.

ILX Lightwave Corp, Box 6310, Bozeman, MT 59771.

Circle No 418

Product note tells you how to increase throughput

The company's 16-pg product note explains how to increase functional test throughput using its 3458A multimeter. Topics covered include an overview of parameters (as well as reading rates) that affect throughput; dc and ac measurements; choosing the best mode and specifications for each application; frequency and period-selecting gate time to achieve allocation, intelli-

gence, and computer/multimeter interactions; and benchmarks with properly structured programs to obtain maximum throughput.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 419

Directory of ESD-control products

Three 4-in.-post binders contain the vendor's "yellow pages" of the CPF (Control Products File) Consulting Service for ESD-control products. The reference work is updated quarterly and is organized for comparative analysis of products. It's arranged in seven major categories: chemicals & raw materials; ionizers; meters and instruments; packaging; personal protection; workstation products; and miscellaneous (tools, tapes, etc). More than 2000 pages of data sheets, indexes, directories, and selection tables are included in the document. In US, first-year subscription, \$335; renewal, \$195. In Canada, \$375 and \$225, respectively; elsewhere, \$425 and \$260, respectively.

SAR Associates, 1212 E Dominick St, Rome, NY 13440.

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Listing of code numbers

The 1989 EIA Source Code and Date Code Booklet provides an alphabetical and numerical listing of code numbers that are stamped or marked on electronic products to identify production sources or the vendor assuming product responsibility. The EIA code system also provides for adding numerals to the source-code symbol to identify both the year and week of production. \$5.

Electronic Industries Association, EIA Engineering Dept, 2001 Eye St NW, Washington, DC 20006.

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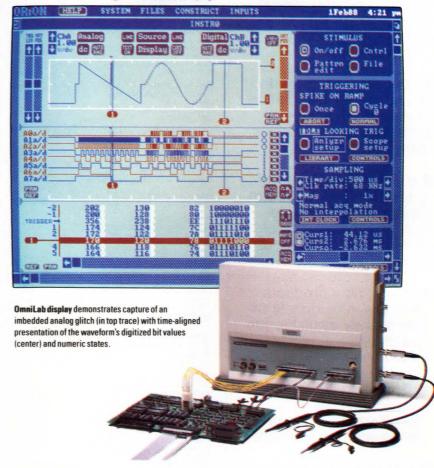
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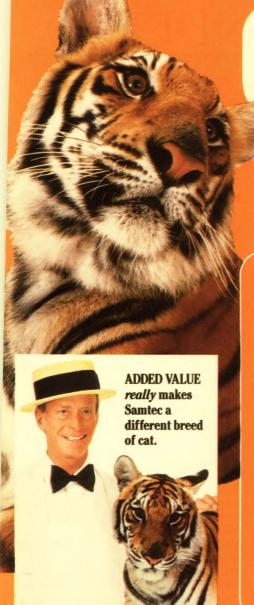
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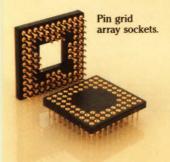
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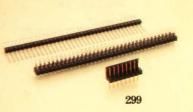
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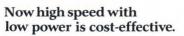
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LOOKING AHEAD

EDITED BY JULIE ANNE SCHOFIELD

World CD market to grow to \$10 billion in 1989

Shipments of compact disks to the United States, Japan, and Europe soared to 390-million units in 1988, up 56% from 250-million units in 1987, according to BIS Mackintosh (Luton, England). The company expects CD shipments to these three areas to grow 38% in 1989 to 540-million units and the overall world demand for CDs to increase to over 650-million units, worth almost \$10 billion at retail.

Japan is now well into the CD age: Over 20% of all homes are equipped with CD players, and the markets are building for in-car and portable CD players. In contrast, less than 15% of homes in Europe and the US have CD players, but the CD-media market values there have exceeded those of vinyl records. In Europe, CD sales already

RECORDED MUSIC FORECAST SUMMARIES (US, JAPAN, AND EUROPE TOTAL ALBUMS)

	1988		1992	
	(MILLIONS)	VALUE (\$M)	(MILLIONS)	VALUE (\$M)
COMPACT DISK	390	6,020	870	10,795
CASSETTES	787	6,740	720	6,360
VINYL	295	2,835	147	1,460
TOTAL ALBUMS	1,472	15,595	1,737	18,615

(SOURCE: BIS MACKINTOSH)

match those of music cassettes, according to the market research company.

Manufacturers are continuing to price CDs to meet market expansion rates and the price tolerances of consumers. Overall, prices are down, mainly due to the introduction of budget-priced CDs, especially in the US. But popular CD releases will still cost 35 to 40%

more than vinyl records and cassettes indefinitely as the older media fade into obsolescence in the 1990s.

RISC µPs to skyrocket to sales of \$600M in 1993

Total revenues for 32-bit reduced-instruction-set computer (RISC) chips will grow from \$34 million in 1988 to \$600 million in 1992, according to a report recently published by The Information Network, a San Francisco-based market research company. This increase corresponds to a compound average growth rate of 77.6%; the company expects the sales of 32-bit complex-instruction-set computer (CISC) chips to increase at a compound average growth rate of 14.1% during the same period.

The report also predicts that RISC consumption will grow from 3.1% of all $32\text{-bit}~\mu\mathrm{Ps}$ in 1988 to

22.6% in 1993. IC manufacturers held the largest share of the market in 1988 with revenues of \$30 million. These companies, such as AMD, Intel, Mips, Motorola, and Sun Microsystems, are expected to increase their market share from 88.2% in 1988 to 95% in 1993.

RISC chips will be used in both workstations and embedded systems, but the chips used in these two application areas will differ because of interrupt-response speed and memory-size constraints. According to the report, unit shipments of embedded RISC processors will grow from 41.2% of the market in 1988 to 76.2% of the market in 1993.

However, The Information Net-

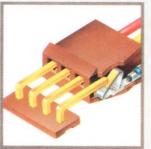
work also reports that many computer companies have been designing their own RISC processors in house. These companies include Apple Computer, Apollo Computer, Ardent, Compaq Computer, Hewlett-Packard, IBM, and Ridge Computer. Proprietary gate-array RISC implementations could undermine the efforts of RISC processor manufacturers.

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