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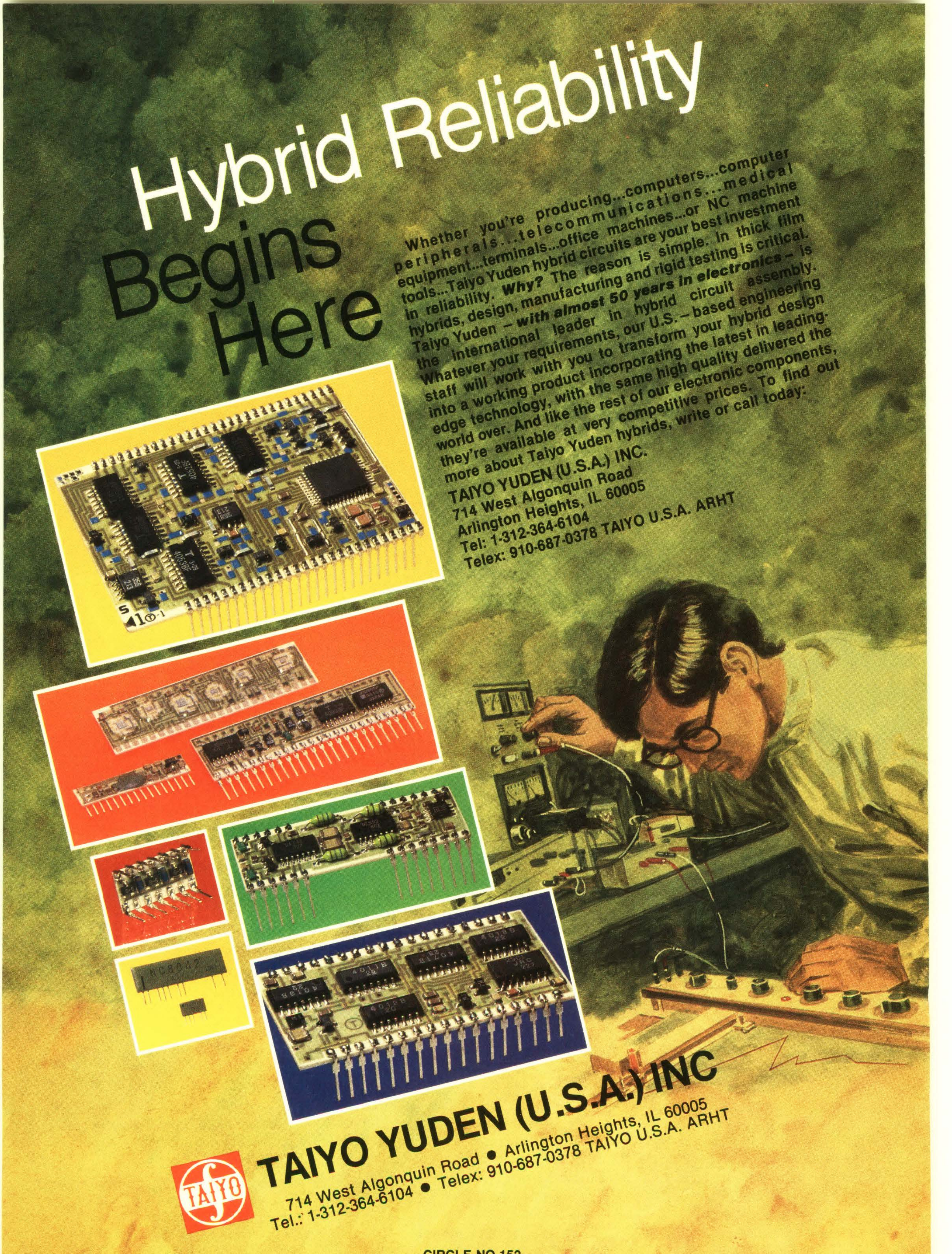
Design Ideas Special Issue VOLUME III

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



CIRCLE NO 152

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February 16, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

(Photography by Mike Blake; art direction by Chinsoo Chung)

Continued on page 5

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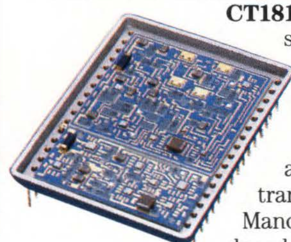

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CIRCLE NO 153

Continued from page 3

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February 16, 1989

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INTRODUCTION

Every batch of Reader Service cards we receive contains many comments about our Design Ideas section. Most often, readers tell us that they've found a particularly useful circuit that helped them solve a tricky design problem. But readers also want to know how they can get a complete set of past circuits and software. Alas, such a compendium doesn't exist. But this Design Ideas Special Issue represents the next best thing—a collection of 33 of the best Design Ideas published in EDN from 1985 through June 1988.

This collection of designs reflects your preferences, not necessarily those of our technical editors. You and your colleagues voted for these winning ideas by circling the Reader Service numbers that appear at the end of each Design Idea we publish. Of the circuit-design tips in this Design Ideas Special Issue, 21 garnered Best-of-Issue honors based on reader preference. The remaining Design Ideas received the second-highest number of reader votes over the 1985 to 1987 time frame.

In planning these Design Ideas Special Issues, EDN hoped to be able to present a good mixture from the standpoint of design disciplines. Happily, our readers' choices made it easy to achieve this goal. This issue contains 16 analog circuit designs and 12 digital designs, and the remaining five ideas highlight programming tips. To achieve some semblance of order, we've divided the ideas into some generic categories and provided an index that lists design and circuit categories. Although the index is a handy place to look for a special circuit, we'll bet that most readers will want to read the ideas one by one, just to see what circuits are available.

As you read these Design Ideas, remember that each one came from a reader who thought someone else might benefit from his or her work. So, if you find this issue helpful, thank your fellow engineers who submitted the ideas we've published over the years. And the next time you have an interesting and useful circuit, consider sharing it with others by submitting it for publication in EDN's regular Design Ideas section.

Besides seeing your name in print and earning $100, you might find your idea has been selected as the issue winner. Each issue winner collects an extra $100. Keep in mind, too, that EDN's editors also choose a grand-prize winner each year. The grand prize includes a check for $1500. Your idea may also be selected to appear in a future Design Ideas Special Issue. You'll find an entry form in the Design Ideas section of most issues of EDN.

If you enjoy this Design Ideas Special Issue and find it useful, we'd like to hear from you. If you have suggestions for improvements and changes, we'd like to hear those, too. Just send us a note or give us a call. We'd also like to thank all the readers who have submitted Design Idea entries over the years.

Enough introduction. Here are more of the ideas you've been clamoring for. Good reading. EDN

Tom Ormond

Tom Ormond
Senior Editor

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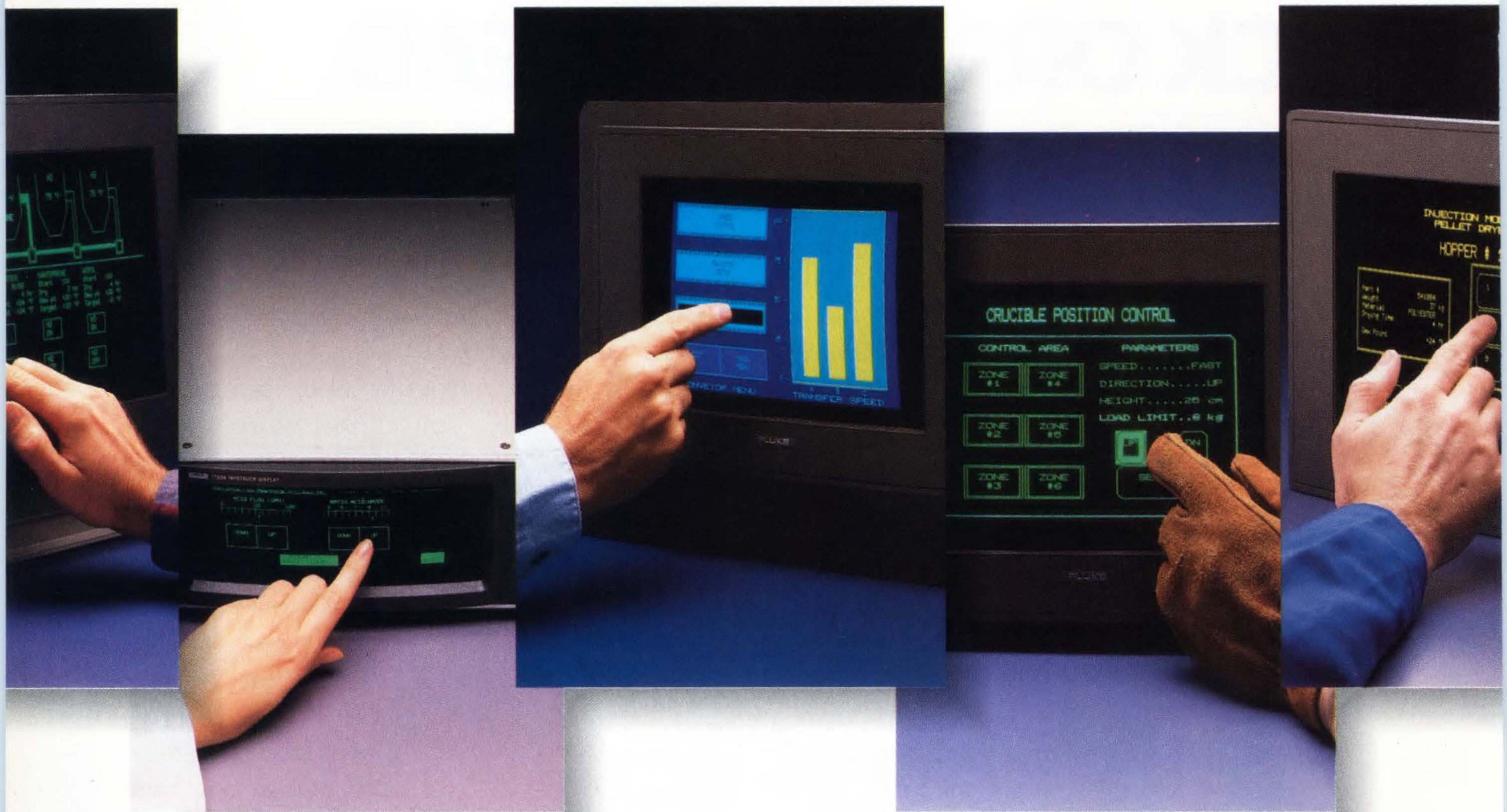

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CIRCLE NO 155

EDITED BY STEVE COGGER

Circuit lets you analyze NiCd batteries

Mike Scaglione
Todd Medical Products, North Canton, OH

Because NiCd batteries maintain a constant output voltage, it is difficult to determine how much of the battery's charge remains. The **Fig 1** circuit provides a way of determining the capacity of a battery by draining it at a preset current to its depleted voltage of 1V/cell. You measure the discharge time of the cells and perform a simple calculation to obtain the battery's capacity.

You set the drain current (I_D) to 0.5C (C=battery capacity in mAhr) by selecting an appropriate value for R_4. Choose R_5 such that $I_D \times R_5 = 1V$. V_{PEF} is set so the comparator turns off the drain current and timer when the battery reaches its depleted voltage, V_B (usually 1V/cell). You calculate V_{REF} as follows:

$$V_{REF} = \frac{R_3[R_2(V_S - 1.3) + R_1V_B]}{R_1R_2 + R_2R_3 + R_1R_3}.$$

With the battery in place, activate the circuit by grounding V_{REF} with the momentary switch. The battery drains at I_D until it reaches V_B, turning off the drain circuit and the timer. Hysteresis keeps the circuit from restarting.

Determine the battery's capacity using the following equation:

$$C_{(mAhr)} = \text{Time of Cycle} \times I_D.$$

The circuit shown tests 4.8V, 180-mAhr batteries. I_D is 100 mA and V_B is 4V. **EDN**

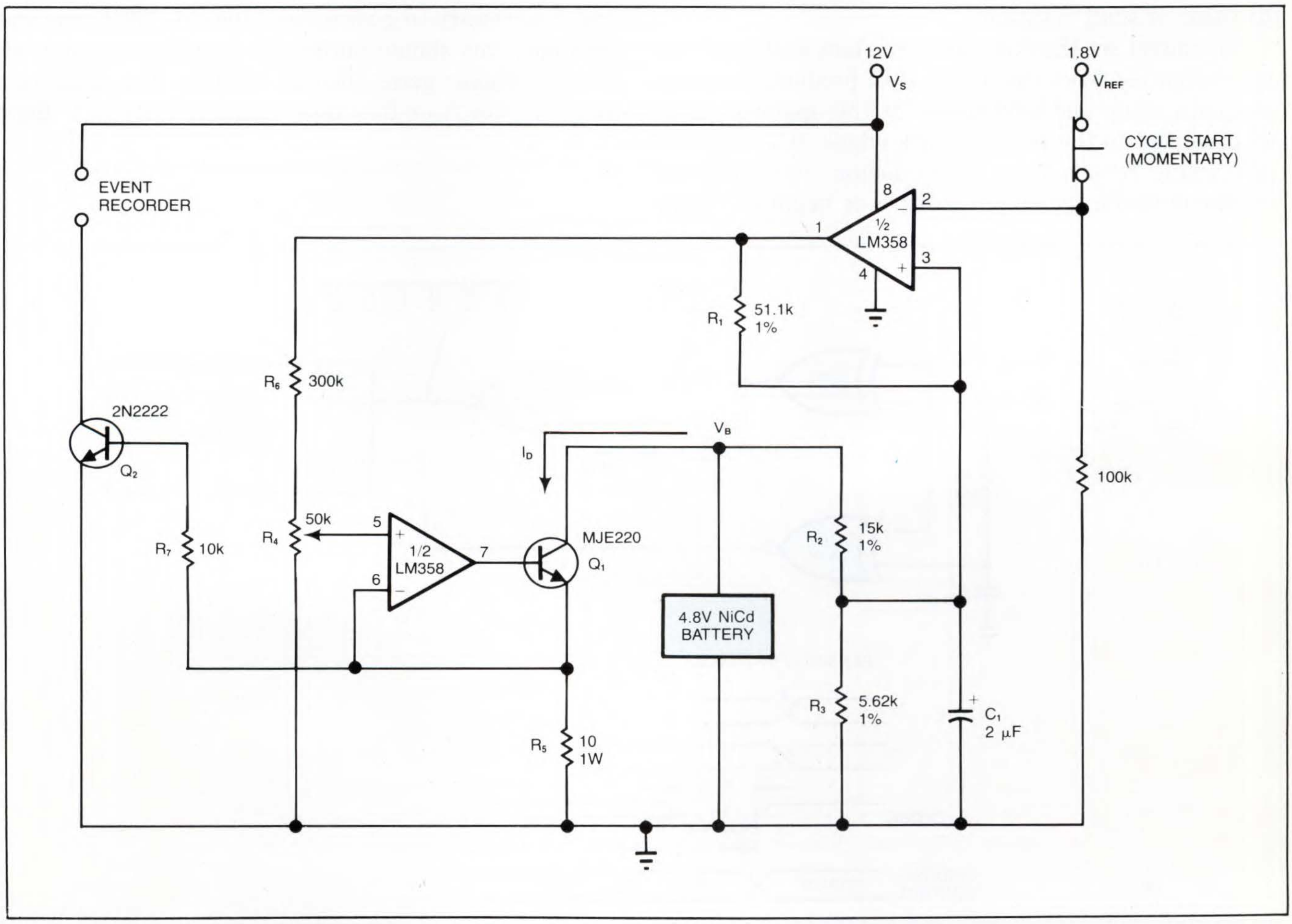

*Fig 1—**This circuit drains NiCd batteries** and controls a timer to test the battery's capacity. When the battery voltage (V_B) reaches 1V/cell, the test stops and the timer turns off.*

Tachometer circuit reduces parts count

William McClelland
Stahl Research, Port Chester, NY

The tachometer circuit of **Fig 1** requires only one IC (besides the counter), yet it achieves the same resolution and eliminates backlash just as the 3-IC circuit of an earlier Design Idea did ("Improved tachometer eliminates backlash," March 31, 1987, pg 210).

A standard shaft encoder's A and B ports generate square waves with the same frequency as the shaft turns. The phase of A will lead or lag that of B by 90°, depending on the direction of rotation. To obtain maximum resolution, the tachometer circuit must count every change of state for the A and B signals. Each such change causes a change of state at IC_{1A}'s output, followed by a 1-µsec negative pulse at the output of IC_{1C}. These clock pulses' positive (trailing) edges cause the counter to count up or down according to the direction of shaft rotation.

You should set the R_1C_1 time constant such that it is approximately twice that of the R_2C_2 product, to ensure adequate setup and hold times for the up/down signal with respect to the positive clock edges. IC_{1C} supports this timing requirement by producing clock pulses of similar duration for either positive or negative transitions from IC_{1A}.

The exclusive-NOR logic of IC_{1B} generates the correct polarity of the up/down signal when necessary—at the positive clock edges—by combining the A value with the B value just prior to a transition of either A or B. C_1 provides memory by storing the B value voltage for about 2 µsec. (To understand this single-gate encoding, note that, because the phase relationship of B and A is + or −90°, adding −90° to B makes the phase difference 0 or −180°, depending on the direction of rotation. Therefore, an exclusive-NOR operation on A and a phase-shifted B produces a logic 1 when the inputs are in phase, or a logic 0 when they are 180° out of phase.)

If necessary, you can invert the up/down signal's polarity by swapping the A and B connections or by using a fourth X-NOR gate as a selectable inverter buffer. To invert the clock signal, substitute identical-pinout, X-OR gates (4070s) for the 4077 X-NOR gates. And if necessary to guarantee standard CMOS rise and fall times, you should buffer the A and B signals with Schmitt-trigger gates such as 74C914s. The maximum frequency for A or B is approximately $(4R_1C_1)^{-1}$. **EDN**

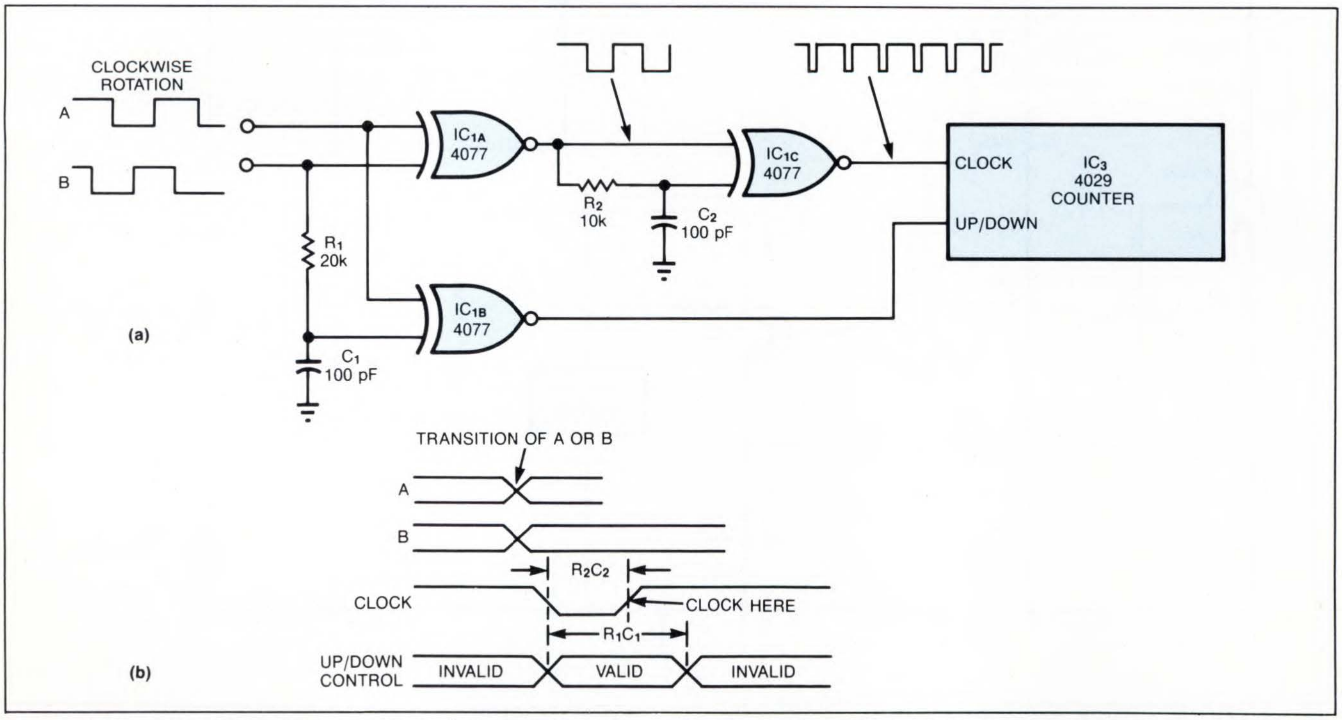

Fig 1—This 1-chip tachometer circuit *drives the counter up or down, according to the speed and direction of shaft rotation (the shaft encoder isn't shown).*

Analog delay line uses digital techniques

T G Barnett and J Millar
The London Hospital Medical College, London, UK

The analog delay line of **Fig 1** uses a digital technique to delay an analog signal for as long as two seconds, reconstructing the signal with 8-bit resolution. The product of the delay time and the bandwidth is a constant: For a 1.024-kHz clock frequency (2-sec delay), the analog bandwidth is 100 Hz; for the maximum 40.96-kHz clock frequency (50-msec delay), the analog bandwidth is 4 kHz. There is no lower limit for the clock frequency.

The clock signal drives a binary counter (IC_2), which then scans the address inputs of a 2048-byte×8-bit RAM (IC_3). The RAM writes the contents of each memory location to the D/A converter (IC_4) and then reads out the results of a just-completed conversion by the 8-bit A/D converter IC_1. The RAM reads out each data sample 2048 cycles after it is read in, so the delay is 2048 times the clock period, or 2048 divided by the clock frequency.

The clock signal also drives two monostable multivibrators in parallel (IC_{5A} and IC_{5B}). IC_{5A} triggers on the clock's rising edge; IC_{5B} triggers on the clock's falling edge. You choose the timing components R and C so that each device produces a pulse of approximately 1 μsec. These pulses have the proper polarity and phase to control the A/D converter, D/A converter, and RAM as shown.

You should scale the analog input for a range of 0 to 2.5V. The 100-pF capacitor sets the A/D converter's internal clock to its maximum rate of 900 kHz; you should monitor the $\overline{\text{BUSY}}$ signal (pin 1) and adjust the capacitor value as required to achieve 900 kHz. Both converters include a 2.5V voltage reference, but to improve accuracy use the A/D converter's reference for both. Power consumption is 120 mA from the 5V supply and 50 μA from the −5V supply. You can greatly reduce current drain from the positive supply by adding logic to control the RAM's chip-enable input (pin 18).

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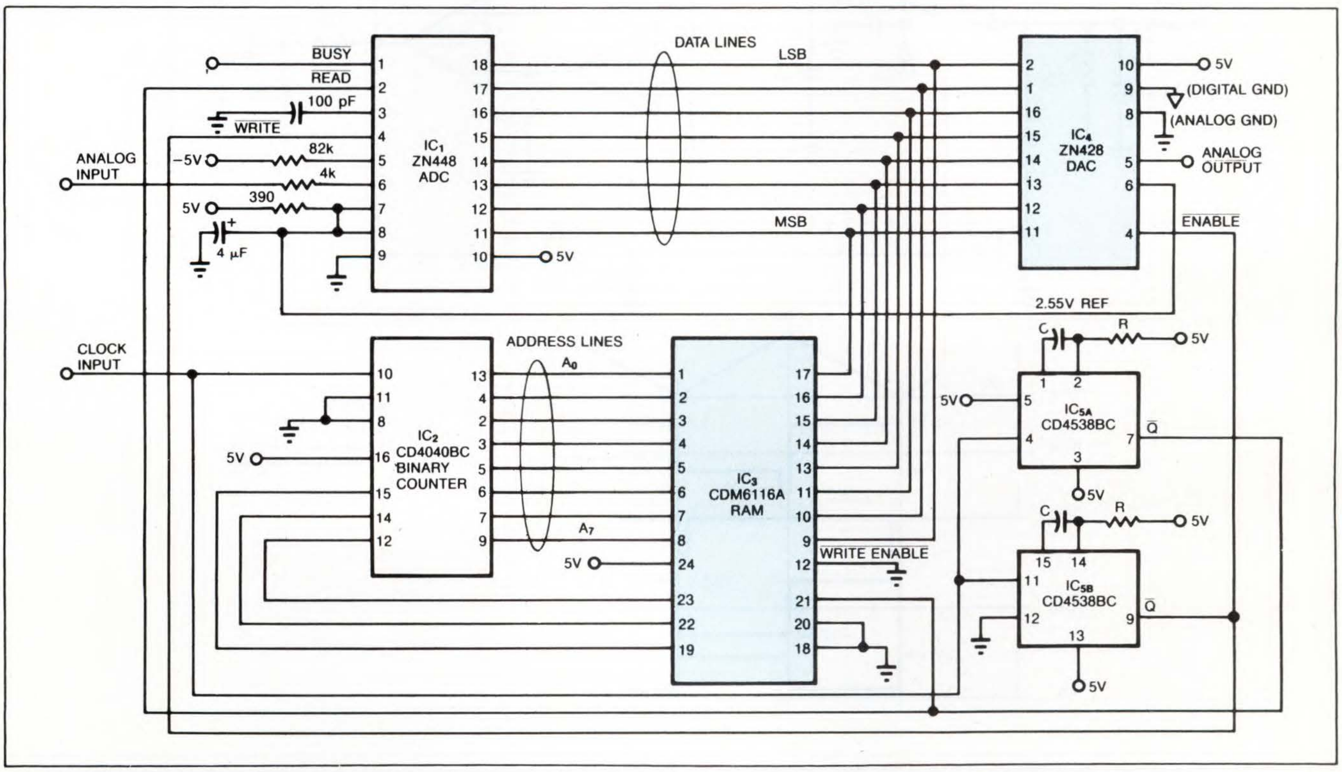

Fig 1—This analog delay line digitizes a signal *once per clock cycle, stores the result in a 2048-word RAM, and converts one sample per clock cycle with a D/A converter. The resulting delay equals 2048 divided by the clock frequency.*

DESIGN IDEAS

EDITED BY TARLTON FLEMING

Circuit converts voltage ratio to frequency

Bobircă Florin Daniel
The Electronic Research Institute,
Bucharest, Rumania

The circuit of **Fig 1** accepts two positive-voltage inputs V_N and V_D and provides a TTL-compatible output pulse train whose repetition rate is proportional to the ratio V_N/V_D. Full-scale output frequency is about 100 Hz, and linearity error is below 0.5%.

The output F_O equals KV_N/V_D, where $K=1/(4R_2C_1)$ and provided $R_1=R_3$. Op amp IC_{1A} alternately integrates $V_N/2$ and $-V_N/2$, producing a sawtooth output that ramps between the V_D level and ground. When transistor Q_1 is on, for example, IC_{1A} integrates $-V_N/2$ until its output equals V_D. At that time, the IC_{1B} comparator switches low, causing IC_{1D}'s bistable output to go low, which turns off Q_1. IC_{1A}'s output then ramps in the negative direction. When the output reaches 0V, the IC_{1C} comparator switches, Q_1 turns on, and the cycle repeats. Transistor Q_2 converts the IC_{1D} output to TTL-compatible output logic levels.

Setting V_D to 1.00V yields a linear V/F converter ($F_O=KV_N$), and setting V_N to 1.00V yields a reciprocal V/F converter ($F_O=K/V_D$). **EDN**

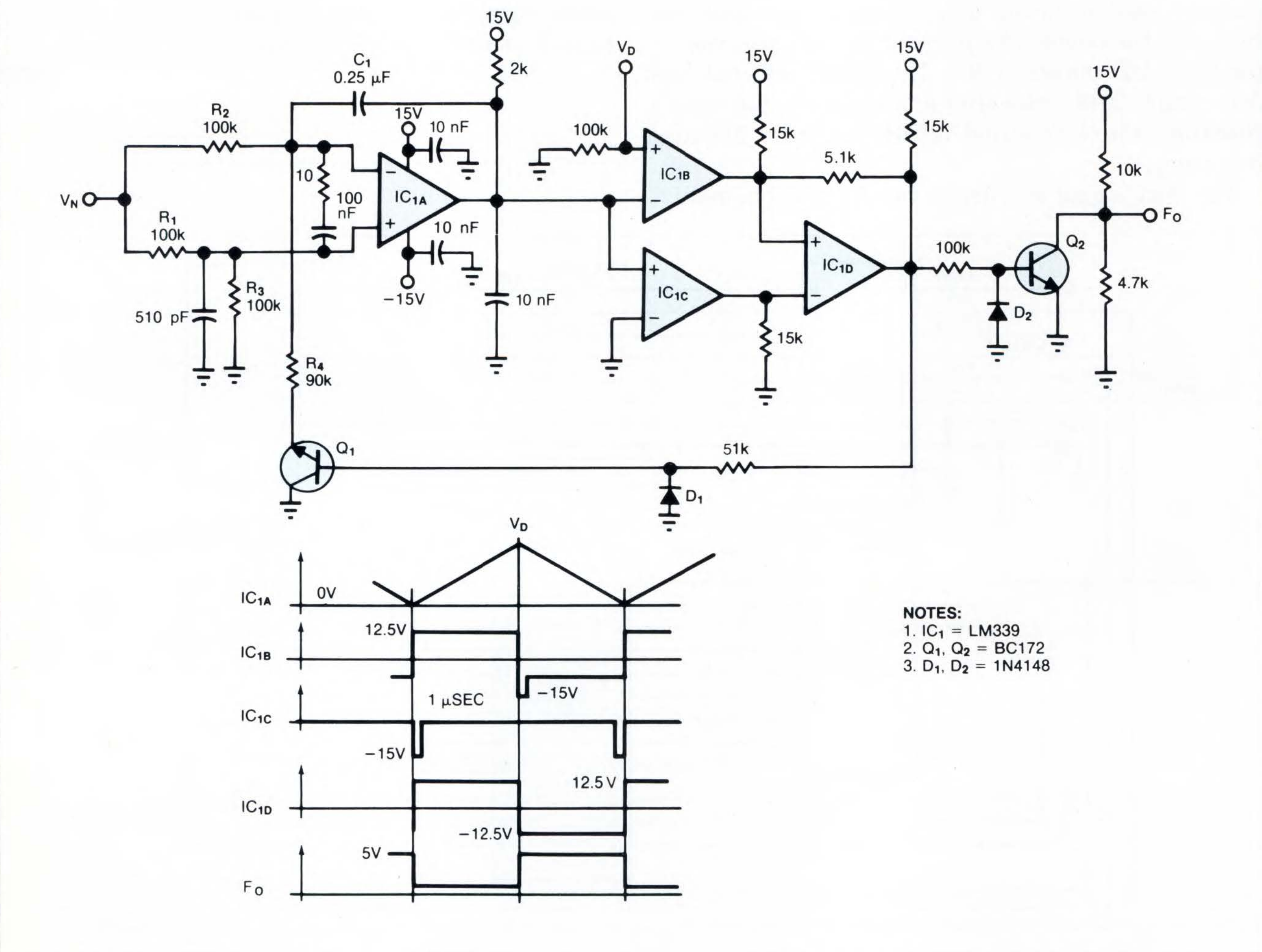

Fig 1—This voltage-ratio/frequency converter produces a TTL-compatible output pulse train that equals KV_N/V_D, where V_N and V_D are the inputs and $K=4R_2C_1$. Linearity error is less than 0.5%.

EDITED BY TARLTON FLEMING

Microphone controls voice-actuated switch

Jonathan Audy
Precision Monolithics Inc, Santa Clara, CA

The **Fig 1** circuit is a speech-actuated switch that enables voice operation of a radio transceiver or similar device. Low-current consumption and 5V operation make the circuit suitable for battery-operated applications. (The original application involved hands-free control of a radio on a hang glider.)

The input stage (IC_{1A}), a bandpass filter with gain, responds to the speech components that are most reliable for actuating the output switch—those at 800 Hz. The main speech components fall in the 200- to 300-Hz range, but centering the bandpass at these frequencies would make the circuit too sensitive to wind noise, breathing, and "banging-door-type" noises. Fortunately, normal speech includes harmonic peaks every 100 Hz or so, to beyond 1 kHz. Centering the filter's bandpass at 800 Hz provides a good compromise between sensitivity and the suppression of false signals.

To ensure the detection of two harmonics, the filter must provide at least 40 dB of gain over a 400-Hz bandwidth. The component values shown for R_1, R_2, C_1, and C_2 give the desired gain and 800-Hz center frequency. (Although not recommended, IC_{1A} can operate without feedback in this application because the op amp's open-loop gain attenuation acts as a lowpass filter.)

The microphone produces 5- to 10-mV signals, which undergo just enough amplification to trip the comparator's (IC_{1B}'s) output high, turning on Q_1. D_1, R_6, R_7, and C_4 make up a peak detector that stores this high state long enough to delay the turnoff of Q_1 for about 0.7 sec—long enough to allow pauses between spoken words. The $R_3/R_4/R_5$ voltage divider sets the comparator's threshold and the filter's dc reference level; adjusting R_4 determines the circuit's sensitivity. C_3 removes noise that might otherwise appear at the high-impedance node that serves as a reference for the gain stage.

The circuit's input connects directly to a microphone jack. For radio applications, connect the circuit output directly to the nongrounded side of the radio's transmit switch (or you can add a 5-kΩ pullup resistor, which allows Q_1 to drive a TTL-logic input). For transceiver applications, you don't need a voice-on/off switch because the circuit's open-collector output allows the transmit switch to operate normally when you remove the voice headset. **EDN**

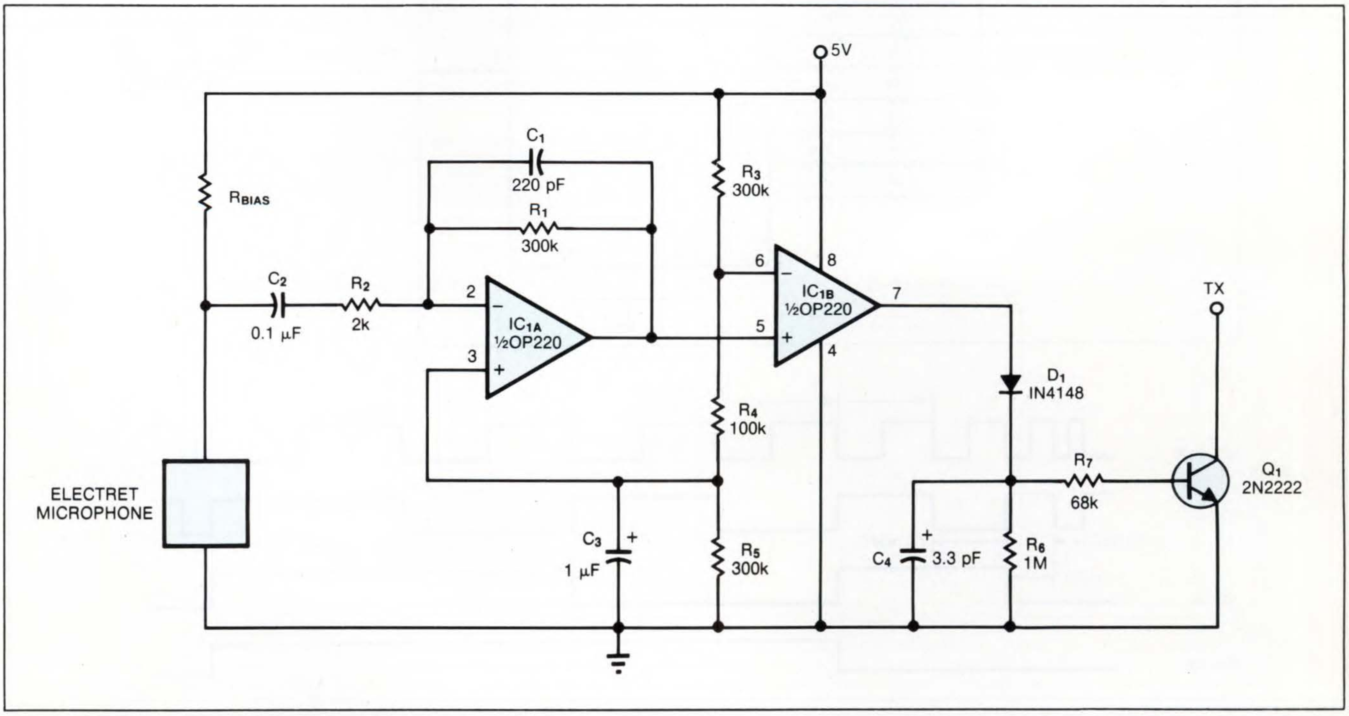

Fig 1—Speaking into this circuit's microphone *drives the TX output low. The output remains low for about 0.7 sec following the last word spoken.*

Counter controls its own clock frequency

Shantha Fernando
Arthur C Clarke Centre, Moratuwa, Sri Lanka

You can implement a finite-state machine by properly decoding the outputs of a binary counter. Driving the counter with a constant-frequency clock signal produces output states of equal duration. **Fig 1**'s circuit, however, produces output states with different time intervals, as most applications require.

The analog multiplexer, IC_3, selects a timing resistor for the timer, IC_1. The timer's output clocks the counter (IC_2) and the counter outputs drive the multiplexer's address inputs. The resistor values shown (R_{T0} through R_{T7}) produce a chirped clock and an ascending sequence of output-state durations, but you can generate arbitrary durations by choosing other resistor values. You can obtain longer durations by increasing the resistor values or by inserting a digital divider between the timer and the counter. **EDN**

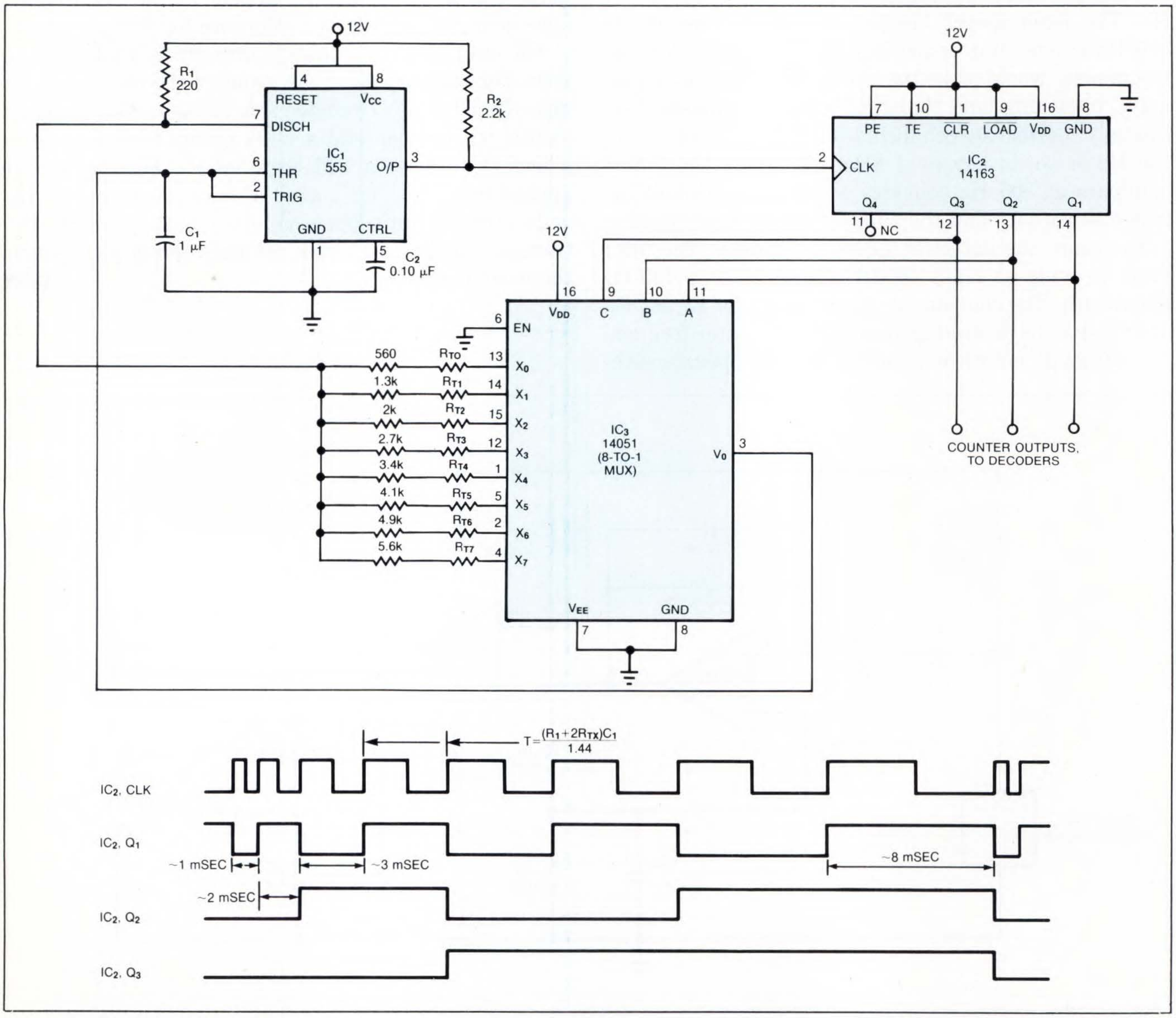

Fig 1—In this loop, the multiplexer *selects a timing resistor for the timer, which clocks the counter, IC_2. The counter's resulting output-state durations depend on the values you select for resistors R_{T0} through R_{T7}.*

Baseline restorer is voltage-programmable

Peter Henry
Precision Monolithics Inc, Santa Clara, CA

The **Fig 1** circuit is a nonlinear, highpass filter that acts as an active baseline restorer **(Fig 2)**. Baseline restoration improves the signal-to-noise ratio for pulse or ac measurements by counteracting the dc errors caused by amplifier drift and electromagnetic pickup. The circuit is particularly useful for signals derived from a high-impedance source such as the human body.

Unlike standard frequency-domain filters, this one acts on the slew rate rather than the frequency of the input signal. At V_{OUT}, the circuit restores the base level of input-signal pulses to an arbitrary level set by V_{REF}. You set the filter's slew-rate cutoff by adjusting $V_{PROGRAM}$, which in turn sets the currents I_1 and I_2. (In applications such as analog adaptive filtering, you can set $V_{PROGRAM}$ using a voltage-output D/A converter, or you can remove $R_{PROGRAM}$ and set the currents using a current-output D/A converter.)

To understand the circuit operation, first note the action of the transistor current mirrors: Collector current in Q_2 (I_1) mirrors the collector current in Q_1, and the transistors Q_5 and Q_6 mirror this current again. Transistors Q_3 and Q_4 each mirror the I_1 current as well, producing the current $I_2=2I_1$. This 2× relationship assures symmetric operation, in which the restoration rates are equal for positive and negative excursions from the baseline.

Assume the capacitor C has charged to the input signal's baseline voltage. If the baseline level of V_{OUT} attempts to rise, the IC_2 output swings low, decreasing the current through D_1. This action causes a flow of current from capacitor C and thus restores equilibrium by lowering the voltage on C. Conversely, a tendency for the baseline to fall causes charge to flow onto the capacitor.

The IC_2 op amp must have a high slew rate to ensure that the restoration circuitry keeps up with the pulses. The rate of restoration depends on the current available (I_1) to charge C. Using $V_{PROGRAM}$, you can set this current to any value between a few nanoamps and a few milliamps. Higher current lets the circuit reject higher slew rates. **EDN**

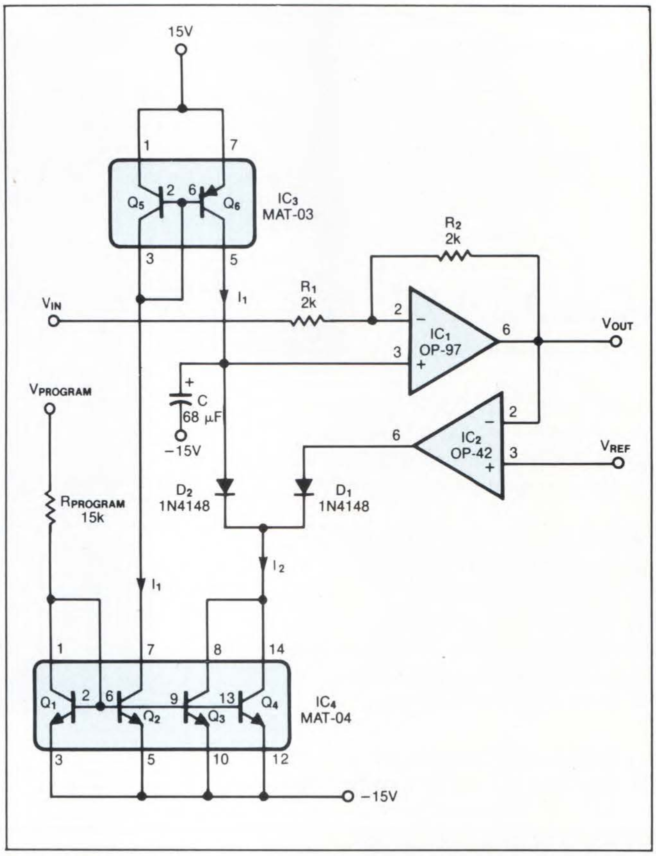

Fig 1—This circuit forces the bases of pulses *in V_{IN} to the arbitrary level V_{REF}, and it rejects pulses on the basis of slew rate according to the voltage $V_{PROGRAM}$.*

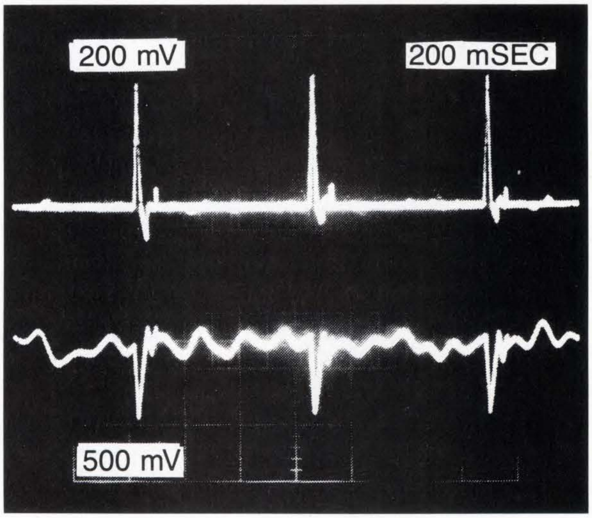

Fig 2—These waveforms show that the Fig 1 *circuit's output (upper trace) inverts V_{IN} (lower trace) while filtering and restoring the signal's baseline voltage level.*

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Electronic thermometer has 10-mV/°F output

Bill Donofrio and Dennis R Bernard
Moore Research Ctr, Grand Island, NY

Using type-K thermocouple wire, you can build an inexpensive electronic thermometer that generates 10 mV/°F (**Fig 1**). Because type-K thermocouples are reasonably linear for the range of 0 to 660°C, you can obtain a moderately accurate temperature measurement for this range by adding a scaling voltage to the cold-junction reference voltage.

The 9V battery powers a bridge circuit in which the temperature sensor, IC_2, and the 2.5V reference, IC_3, provide a signal and reference voltage, respectively. You should place the cold-junction thermocouple close to the temperature sensor. Note that the chromel wires form secondary junctions where they attach to the circuit (nodes A and B). To avoid introducing dc errors, you should maintain these junctions at the same temperature by placing them close together. Bypass capacitors C_6 and C_7 guard against errors due to RF pickup.

Potentiometer R_5 produces a temperature-dependent scaling voltage, and the chopper-stabilized op amp, IC_1, amplifies (with a gain of 1001) the sum of the scaling and thermocouple voltages. As a result, the output V_T equals the sum of the thermocouple cold-junction voltage plus the scaling voltage (0.744 mV), divided by 0.0226. Potentiometer R_6 determines the 0.0226 figure.

To calibrate the circuit, first adjust R_4 for 2.554V across IC_3. Then adjust R_3 so the voltage across IC_2 equals 10 mV times the ambient temperature (in °K). Place the hot-junction thermocouple in a well-stirred mixture of crushed ice and water, and adjust R_5 so that the op-amp output (across R_6) equals 0.744V. To complete the calibration, adjust V_T to 0.32V using R_6. **EDN**

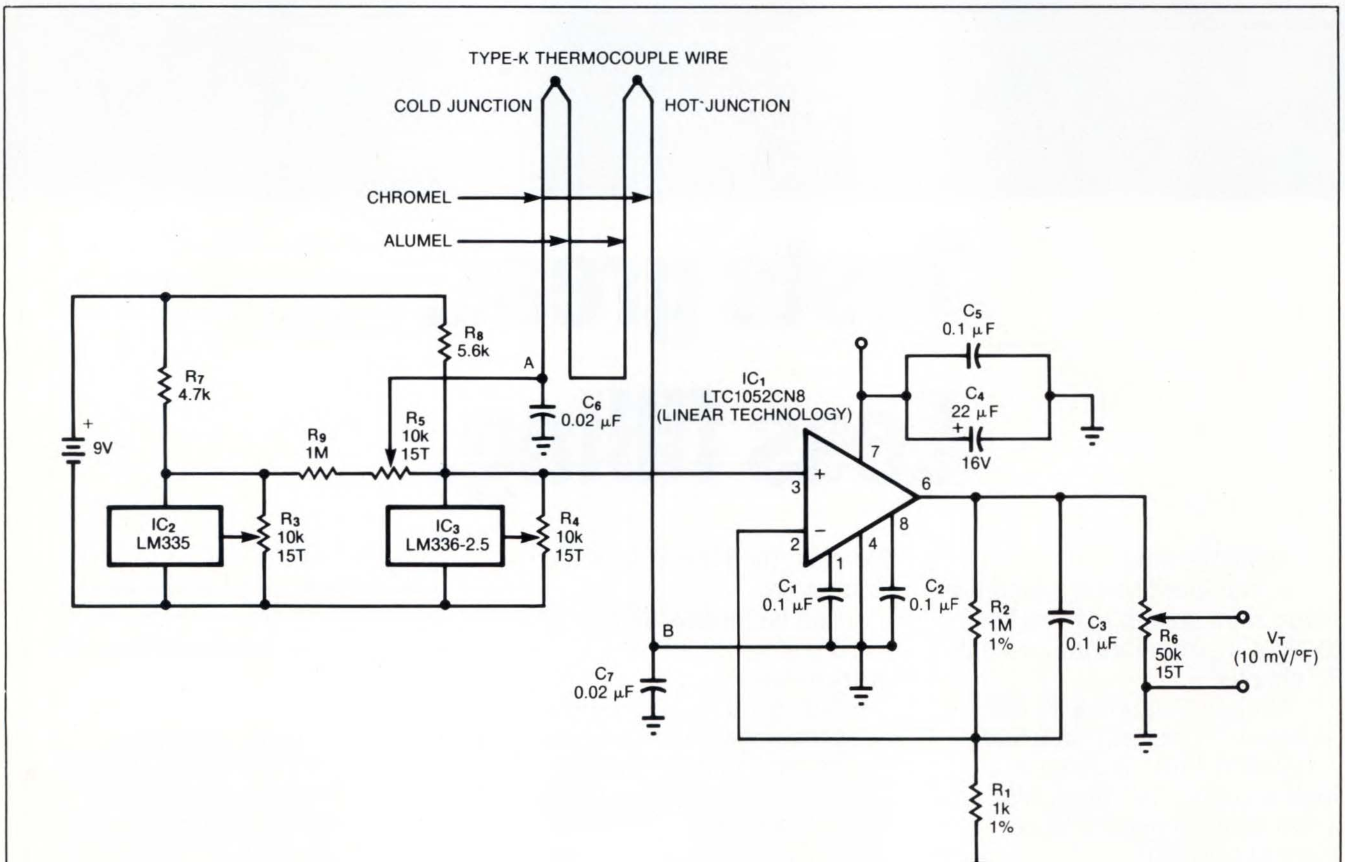

Fig 1—This circuit adds a linearizing voltage *to the thermocouple voltage and produces an output V_T of 10 mV/°F.*

EDITED BY TARLTON FLEMING

Driver circuit boosts 3-state outputs

Einar Abell
ADA Instruments, Burlington, VT

The power booster in **Fig 1** allows an ordinary 3-state gate to drive 50Ω loads to several volts peak-to-peak. Rise and fall times are only a few nanoseconds for a properly terminated coaxial cable. Employing two switched current sources of opposite polarity, the booster converts the gate's unipolar output to a bipolar one. Further, the booster output shuts off when the gate goes to a high-impedance state; this feature is particularly useful when the gate must drive inductive and capacitive loads.

When the 3-state gate output is enabled and in a high state, transistor Q_1 turns on the upper current source (D_1, D_2, R_6, and Q_3); when the 3-state gate output is enabled and in a low state, Q_2 turns on the lower current source (D_3, D_4, R_7, and Q_4). When the 3-state gate is disabled (in a high-impedance state) both sources are off and the booster output discharges to zero through R_8.

Fig 1's circuit is simple because its transistors are biased so that they don't saturate. If the transistors were allowed to saturate, you'd need to add components to the circuit to compensate for the unequal turn-on and turn-off times that would result.

To prevent Q_3 and Q_4 from saturating, you must set R_8 to limit the output within 2V of either supply rail. The output current I_0 equals 0.7 R, where R is the value of R_6 and R_7. To obtain greater output current, you can replace the output transistors with Darlington pairs. If necessary, you can improve I_0's temperature stability by thermally coupling D_2 to Q_3 and D_3 to Q_4 and by replacing D_1 and D_4 with low-voltage zener diodes. R_4 and R_5 bias the input transistors to the midpoint of the 3-state gate output and set the drive current to Q_3 and Q_4. **EDN**

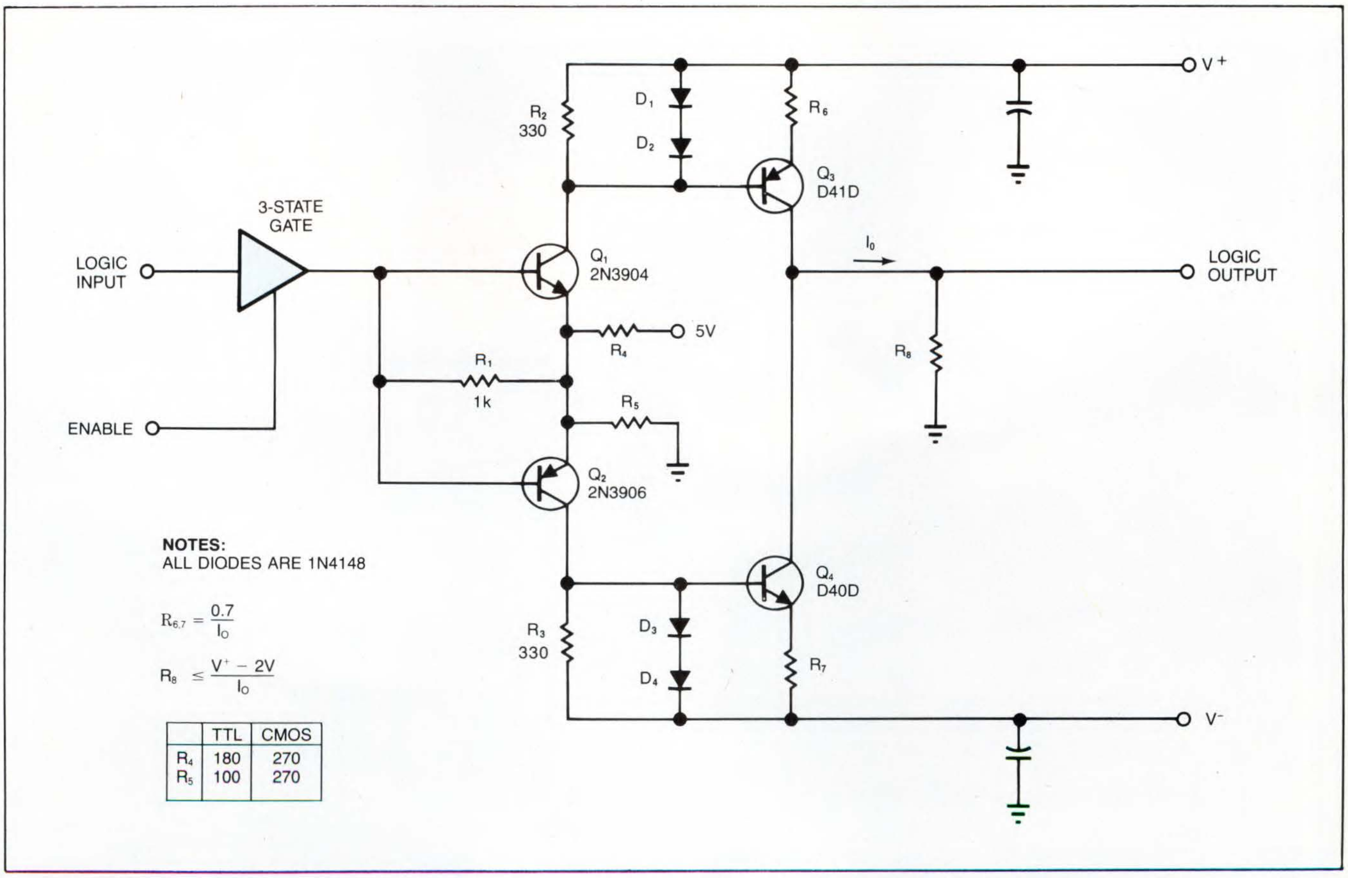

*Fig 1—**With this discrete driver circuit,** any 3-state gate can drive 50Ω loads with ease. Output resistance equals the value of R_8 when the gate is in a high-impedance state.*

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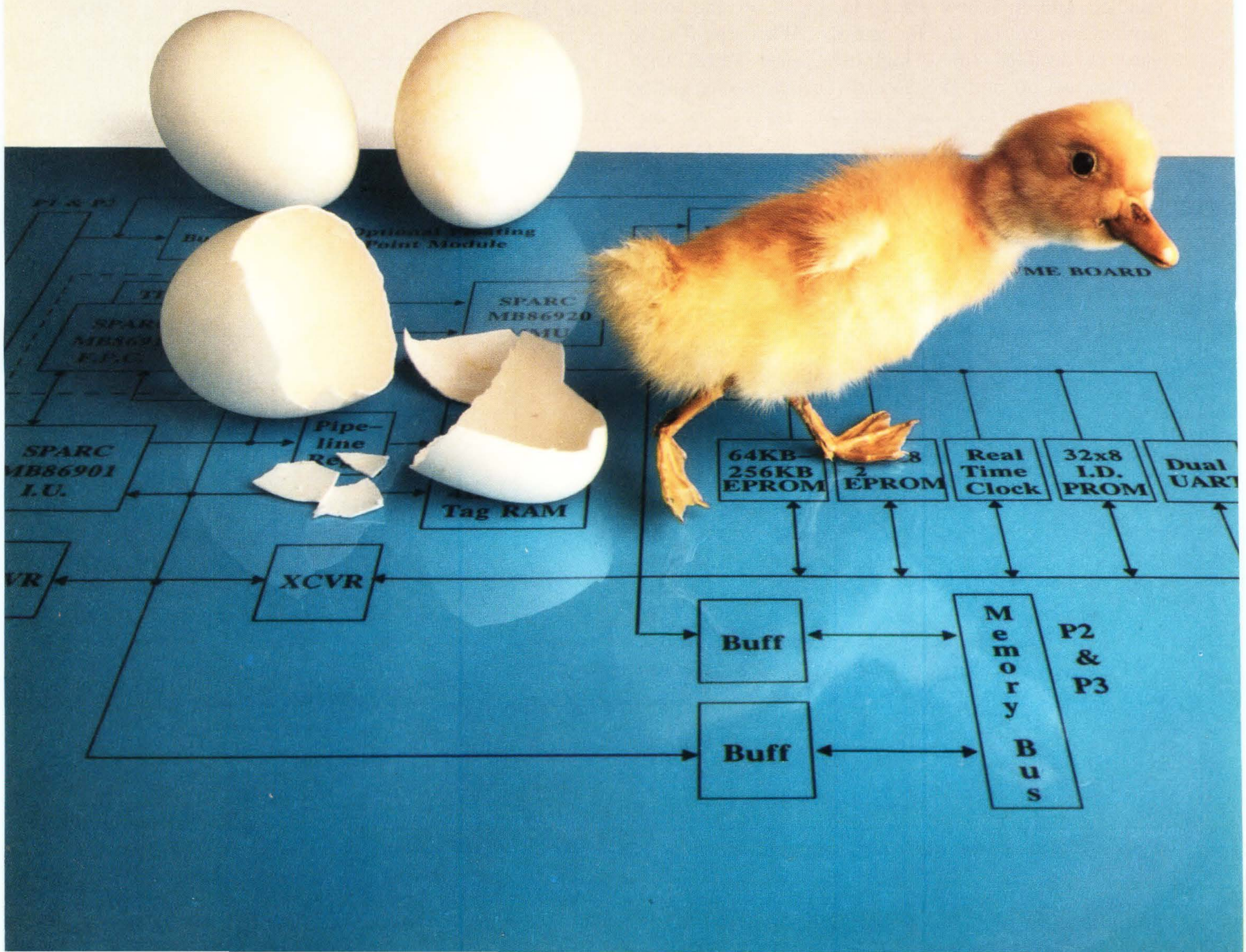

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CIRCLE NO 165

DESIGN IDEAS

EDITED BY TARLTON FLEMING

Simple calculator acts as low-speed counter

J N Lygouras
University of Thrace, Xanthi, Greece

By adding a handful of inexpensive components, you can transform a 4-function calculator into a low-speed counter or tachometer. Note, however, that the calculator must have a constant-calculation feature for this scheme to work.

Fig 1 illustrates the scheme. In **Fig 1a**, a series of 555 timers produces a string of pulses **(Fig 1b)**, which key the calculator. When you press the reset switch, S_1, its negative-going edge triggers the first 555 timer, IC_1, making its output go high for about 23 msec. This high level closes electronic switch S_2. This closure is equivalent to pressing the calculator's zero digit.

In a similar fashion, the circuit sequentially activates the plus and one keys. The negative-going output of the third 555 timer, IC_3, triggers the fourth 555 timer, IC_4. Triggering IC_4 enables electronic switch S_5, which routes the input pulses to the equals key for the duration of IC_4's time period. This sequence is equivalent to your pressing the calculator's keys as shown in **Fig 2**, where N is the number of counted pulses that correspond to the final display on the calculator at the end of IC_4's time period, T_C.

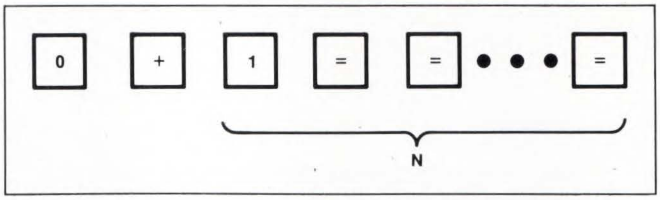

Fig 2—The circuit shown in Fig 1 *mimics the key strokes shown here.*

You can add the optional circuit to convert the counter to a tachometer. The Schmitt trigger shapes pulses from an engine's contact points. You must divide the points' signal by four because the calculator's maximum counting frequency is 20 Hz. For example, a 4-stroke, 4-cylinder engine running at 1000 rpm would generate 33.3 sparks/sec. Of course, if you divide the incoming pulse stream by four, you must increase IC_4's counting period by a factor of four to compensate. **EDN**

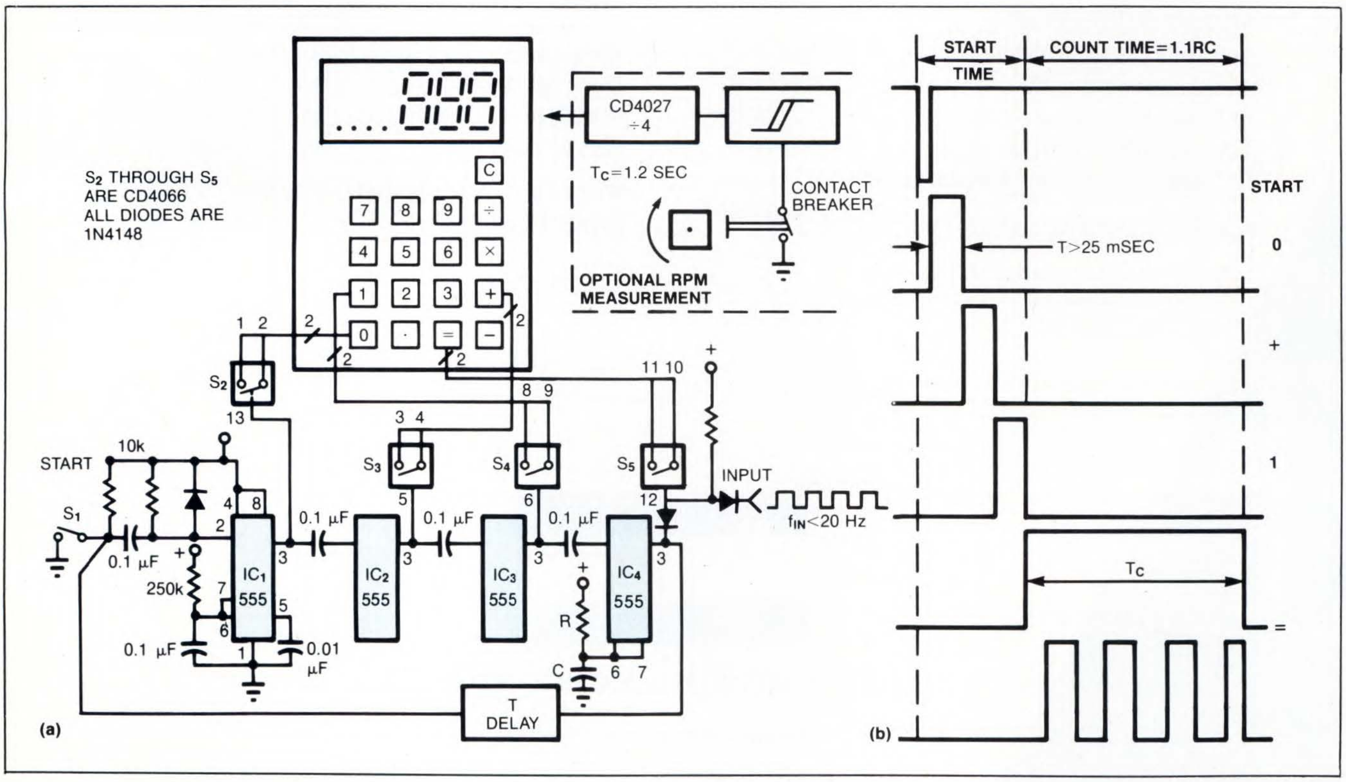

Fig 1—Electronic switches, triggered by 555 timers *and an incoming pulse train, turn a simple 4-function, constant-calculation calculator into a low-speed counter or, optionally, a tachometer.*

EDITED BY TARLTON FLEMING

Tachometer measures low frequencies

Ricardo Jimenez-G
Mexicali Technological Institute, Mexicali, Baja California, Mexico

The **Fig 1** tachometer lets you measure heartbeats, respiratory rates, and other low-frequency events that recur at intervals of 0.33 to 40.96 sec. The circuit senses the period of f_{IN}, computes the equivalent pulses per minute, and updates the LCD accordingly. (Although the decimal readout equals $60f_{IN}$, the circuit doesn't actually produce a frequency of $60f_{IN}$.) The computation involves counting and comparison techniques and takes 0.33 sec.

To understand the circuit's operation, suppose a reset pulse arrives at pin 15 of IC_1, setting Q_1 and Q_2 low. Then, the first f_{IN} pulse drives Q_1 high, which opens the IC_{3A} gate and allows 100-Hz pulses to drive the counter IC_4. The next f_{IN} pulse drives Q_1 low and Q_2 high, which simultaneously freezes IC_4 at a count of N by turning off the 100-Hz pulses. The same f_{IN} pulse opens the gate IC_{8A}, which allows 18-kHz pulses to drive the IC_7 counter.

Each time IC_7 reaches a count equal to that of IC_4, the IC_5-IC_6 comparator produces a pulse that increments the display counter IC_{11} and resets IC_7 via IC_{3D}. Thus, IC_7 counts at a rate of 18 kHz without interruption and resets to zero after every N counts. (N is proportional to the period of f_{IN}.) This process terminates at 6000 counts, when the BCD counters IC_9 (count of 100) and IC_{10} (count of 60) produce a pulse at pin 11 of IC_{8D} that resets IC_1, IC_4, IC_9, and IC_{10}. The reset at pin 15 of IC_1 drives Q_0 (pin 3) high, which in turn resets the display counter and updates the display.

An f_{IN} of 1 Hz, for instance, sets IC_4 to a binary count of N=100. Consequently, IC_7 counts 60 times from 0 to 100 during the 6000-count interval, producing a readout of 60. Similarly, f_{IN}=1.25 Hz produces N=80 and sets the readout to 6000÷80=75 pulses per minute. **EDN**

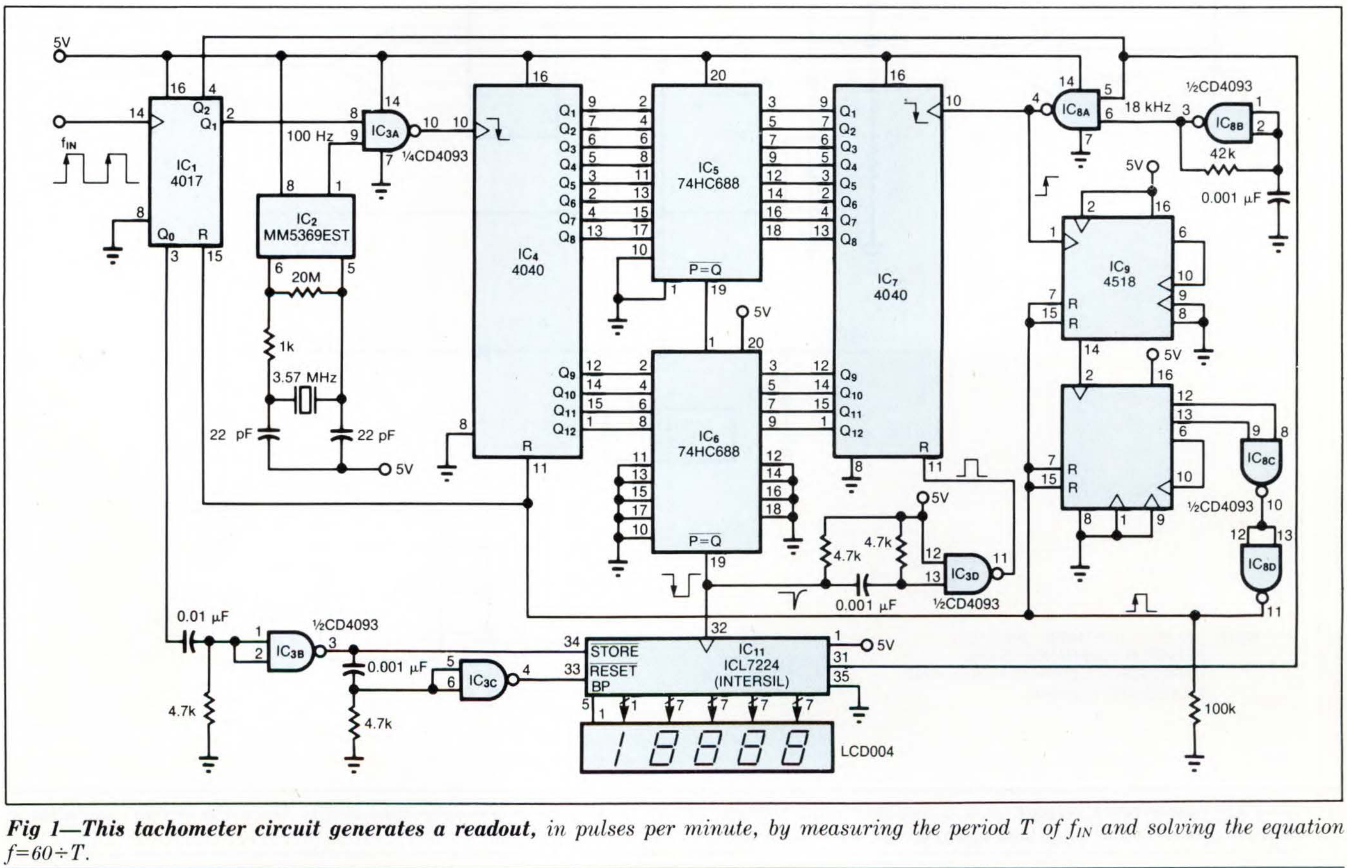

Fig 1—This tachometer circuit generates a readout, in pulses per minute, by measuring the period T of f_{IN} and solving the equation f=60÷T.

EDITED BY KEN MARRIN

Power-reset circuit provides four functions

James Colotti
Eaton Corp, Farmingdale, NY

The power-reset circuit shown in **Fig 1** provides a reset signal under four conditions: during initial power-up; when the supply voltage falls below 4.5V; after a supply-voltage glitch; and after a manual reset. When you first apply power to the circuit, the output ($\overline{PWRST}$) goes low. After 500 msec, the output goes high. If the supply voltage drops below 4.5V, the output goes low and stays low until 500 msec after the supply voltage returns to 5V.

The open-collector outputs of comparators IC_{1A} and IC_{1B} are connected in an OR configuration. When either output is low (this condition is caused by a power-on reset or a low-power condition), that low output holds IC_{1C}'s output low through D_2. IC_{1C}'s low output, in turn, drives both IC_{1D}'s output and $\overline{PWRST}$ low.

When the outputs of both IC_{1A} and IC_{1B} go high—which indicates that the supply voltage has returned to 5V and that no power-on reset is in progress—IC_{3A}'s Q output goes high for 500 msec (IC_{3A} is configured as a one-shot multivibrator). After 500 msec, the Q output goes low, IC_{1C}'s output goes high, and $\overline{PWRST}$ goes high.

S_1 gives you a manual-reset option. Holding S_1 closed maintains $\overline{PWRST}$ in a low state. When you release the switch, you trigger the monostable multivibrator; 500 msec later, $\overline{PWRST}$ goes high. EDN

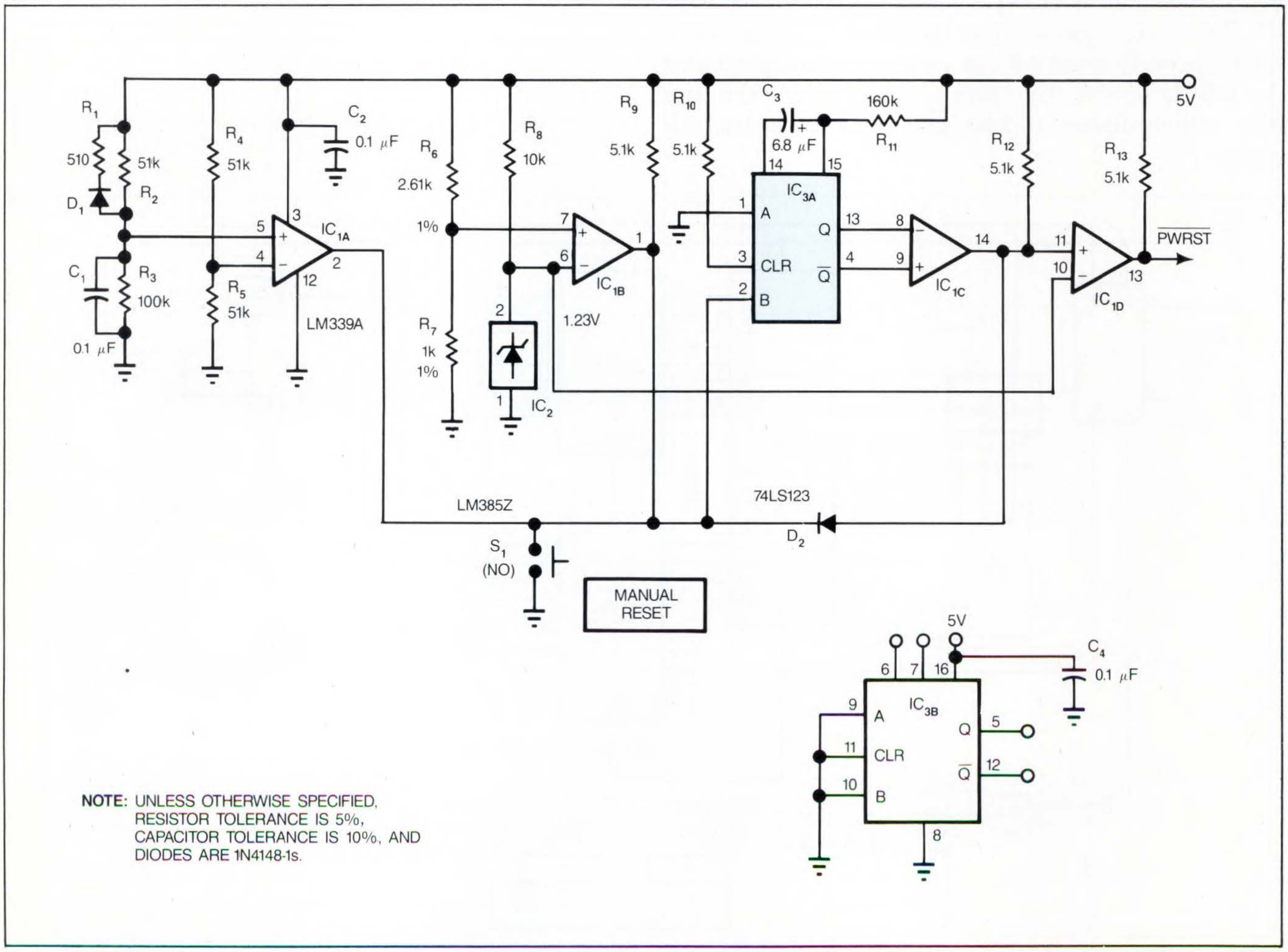

*Fig 1—**This power-reset circuit** uses a one-shot multivibrator (IC_{3A}) to provide a 500-msec time delay. Once the circuit generates a power-reset signal, it will hold that signal for at least 500 msec.*

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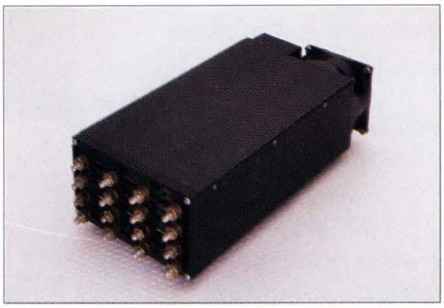

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	#1	#2	#3	#4	#5
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SP1-1802	5 @ 240				
SP1-1803	12 @ 100				
SP1-1804	15 @ 80				
SP1-1805	24 @ 50				
SP1-1806	28 @ 42				
SP1-1807	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8

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CIRCLE NO 168

EDITED BY TARLTON FLEMING

Digital ICs form programmable divider

Steve Lubs
Dept of Defense, Washington, DC

The **Fig 1** circuit divides the input clock frequency by an integer between 2 and N (N=8 in this case). You select the integer by applying a 3-bit word at the divisor-control inputs.

IC_1 and IC_2 form an 8-bit shift register. These cascaded ICs either shift their output data to the right or load input data in parallel: When S1 (pin 10) is high, the chips load the A through D inputs (pins 3 through 6) on a positive transition of the input clock. When S1 is low, each positive clock transition causes the chips to shift their output data (which appears on Q_A through Q_D) to the right. Multiplexer IC_3 selects one of its eight inputs according to the 3-bit divisor-control input, and the multiplexer's output drives the S1 inputs of IC_1 and IC_2.

During operation, the circuit's output goes high for one clock cycle, causing the shift register to load the input word 10000000. Succeeding clock cycles shift the input word's single 1 to the right until it enters the selected IC_3 input. The resulting output pulse loads the shift register with another 10000000, which reinitiates the cycle. Coincident with each parallel-load operation, the circuit consisting of IC_4, IC_5, and IC_6 presents a 1 to the shift register's D_{SR} input, ensuring continued operation in the event that a malfunction clears the shift register.

The circuit can operate at 50 MHz if you use high-speed devices such as ones from Fairchild's Fast Series. You can obtain larger divisors by increasing the number of shift-register stages. Adding another multiplexer, however, lowers the system clock rate. EDN

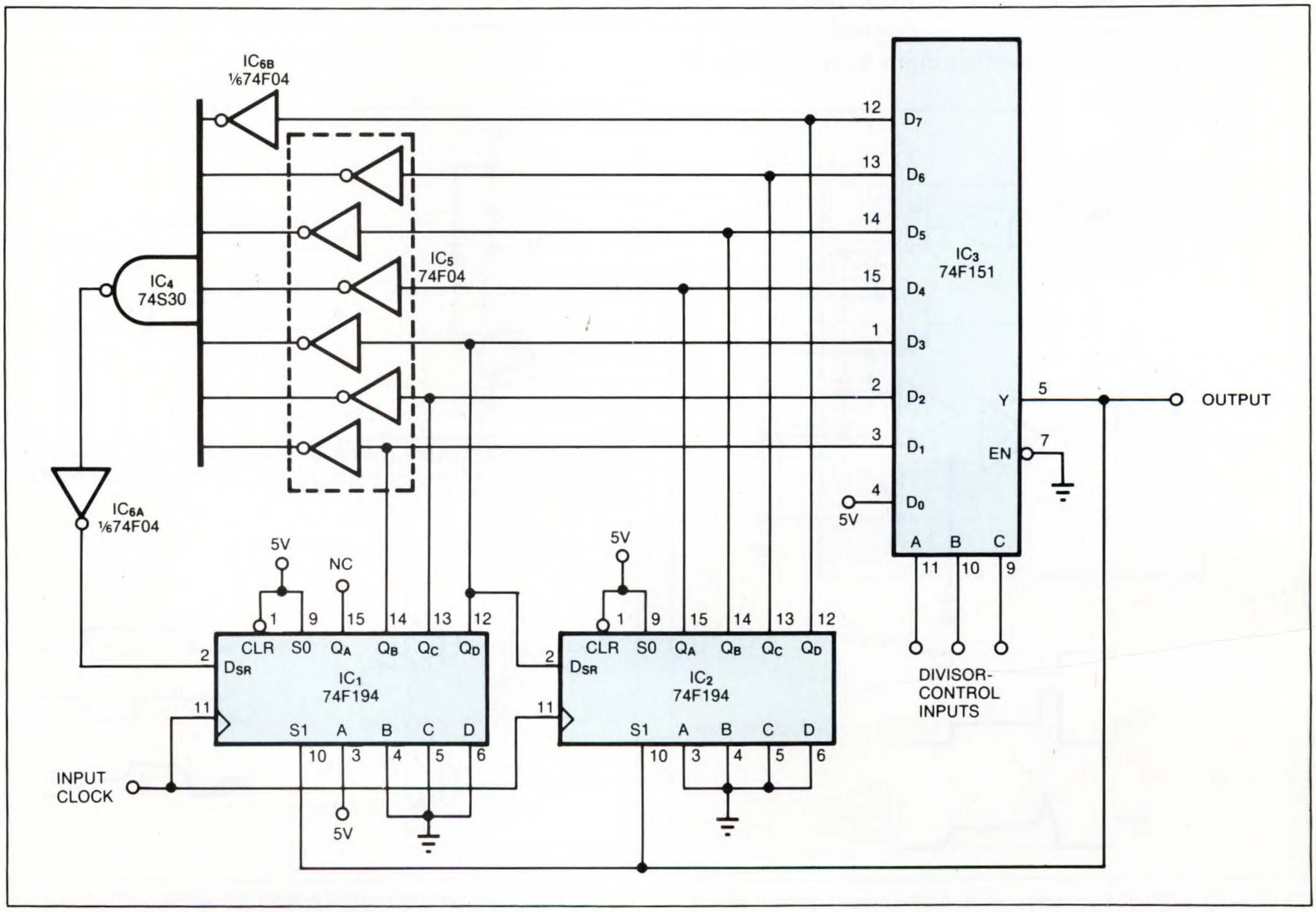

*Fig 1—**Two universal shift registers** (IC_1 and IC_2) and a 1-of-8 data selector (IC_3) form a programmable divider; IC_4, IC_5, and IC_6 provide a backup function for the divider's operation.*

EDITED BY KEN MARRIN

Simple circuit supplies relay hold current

F Raymond Dewey
Sprague Electronic Co, Worcester, MA

The **Fig 1** circuit generates hold current for relays and solenoids by taking advantage of an integrated power driver's (UDN-2975W) internal short-circuit-protection circuitry. This technique provides an efficient alternative to RC timing circuits **(Fig 2)** and a simple alternative to configurations that require multiple discrete power drivers with split supplies and complicated timing sequences **(Fig 3)**.

Fig 1's driver can supply as much as 5A of peak current to a relay or solenoid. A single input activates the relay. When the input goes low, both the source driver (Q_1) and the sink driver (Q_2) turn on. The positive voltage source then supplies current to the load relay. Sensing resistor R_1 monitors relay current. When the voltage across this resistor and, subsequently, the voltage at the inverting input to comparator A_1 exceed the reference voltage at the noninverting input, the comparator sets the latch. You can calculate a value for R_1 using the equation

$$R_{SENSE}=V_{REF}/(10I_{TRIP}),$$

where V_{REF} is the reference voltage and I_{TRIP} is the current value at which the relay trips.

Once the latch is set, Q_1 turns off and the load's current and voltage drop to a value determined by supply B^+. The sink driver remains on as long as the input stays low. You could also use a current-limiting resistor across the source driver to limit load current in the hold state. When the input goes high, the sink driver shuts off and the latch is reset. The circuit is now ready for another operation. EDN

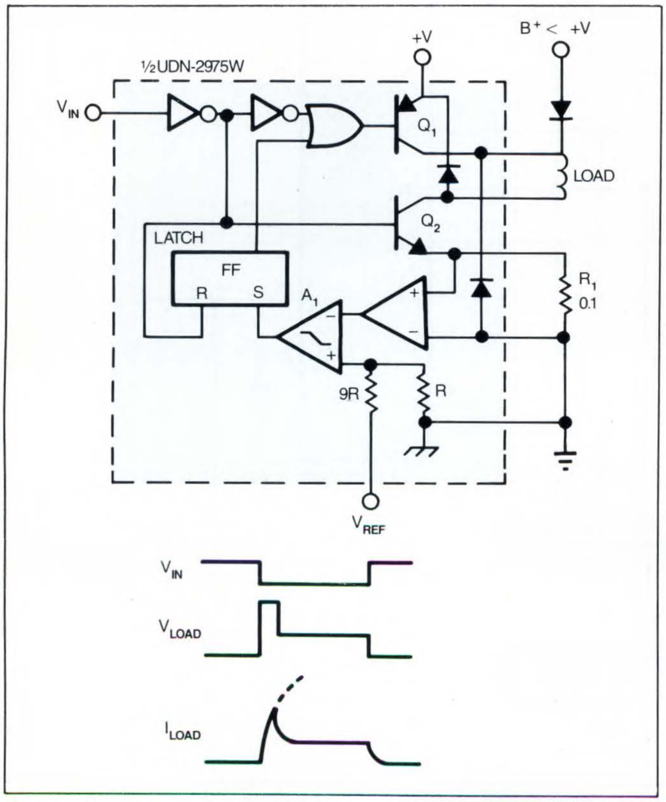

Fig 1—By taking advantage of a high-current power driver's internal short-circuit protection, you can build a simple circuit for supplying hold current to relays and solenoids.

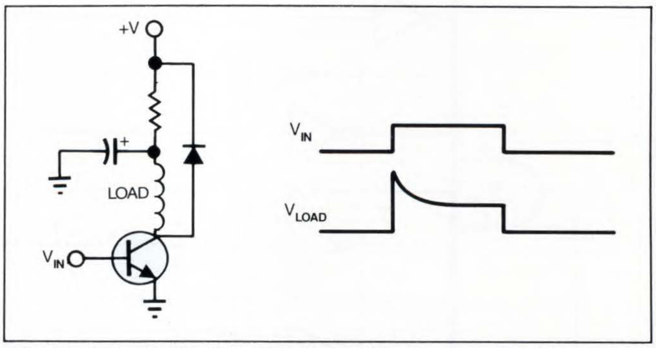

Fig 2—This RC timing circuit provides one means of generating relay and solenoid hold currents, but it's less efficient than the Fig 1 method.

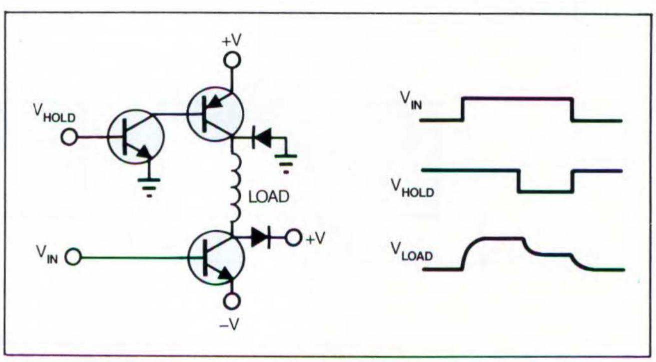

Fig 3—This hold-current control circuit for relays and solenoids is effective, but it requires split supplies and complicated timing sequences.

EDITED BY ROBERT M CLARKE

Algorithm produces base-2 logarithms

Robert D Grappel,
Compdata Services Corp, Wellesley, MA

To most programmers, an algorithm that computes a logarithm is something hidden in the bowels of a compiler or math package. Typically, the computation involves floating-point operations and series expansions. Nevertheless, an algorithm exists that lets you quickly and easily calculate base-2 logarithms, even using μPs.

The algorithm uses the fact that a binary number can be represented as the sum of a series of powers of two in which each power is multiplied by either a zero or one coefficient. Thus, you can represent the number as a series of bits, each zero or one, with each bit's position corresponding to a power of 2. For example, the binary string 0110 represents

$$0\times2^3+1\times2^2+1\times2^1+0\times2^0.$$

(For further theory, see "Exponential and Logarithm by Sequential Squaring," *IEEE Transactions on Computers*, Vol C-33, No 5, May 1984.)

Consider a subroutine example that implements the algorithm. First, note that this example uses a scaled integer representation for the arguments for the logarithm subroutine. The assumed decimal point lies between bits 14 and 15 of a 16-bit value. Assume that the real argument value has been multiplied by 2^{14} (16,384) and is now an integer. The subroutine uses 16- and 32-bit integer operations. Its output is a scaled 16-bit fraction whose assumed decimal point is to the left of bit 16. Hence, the subroutine produces results significant to about 16 places.

Second, the example requires that the argument be between 1.0 and 2.0. This isn't a great hardship, because values outside this range can be scaled to fit, and the return value from the logarithm routine can be adjusted. Scaling base-2 values requires only shifting and adding, which isn't too difficult to accomplish. The scaling code is not shown here.

The code in **Fig 1** shows how you can implement the algorithm in C. Integers are assumed to be represented in 32 bits. The array "L" stores the bits of the 16-bit logarithm.

You can also implement the algorithm on a μP. **Fig 2**'s code shows how simply you can write the subroutine in Motorola 68000 assembly language. Note that with the scaling factor chosen, there's no danger of overflow in the multiplication step. Shifts do all the divisions. The order of bits is reversed to match Motorola's format.

You can calculate logarithms in other bases by multiplying the base-2 logarithms by the appropriate constant, which is simply the base-2 logarithm of the desired base. This multiplication requires 32 bits of precision because the constant scaled will exceed 16 bits. **EDN**

```
#define SCALE 16384     /* 14-bit scaling constant */

int x;          /* the argument, whose base-2 log. is desired */
int i;          /* bit counter index for L */
char L[16];     /* bits of the logarithm base-2 of x */

for (i=0; i < 16; i++)
    {/* loop through 16 bits of L */
    L[i] = 0;        /* initialize bit */
    x *= x;          /* square x */
    x /= SCALE;      /* re-scale its value */
    if (x >= (2 * SCALE))
        {
        L[i] = 1;    /* set bit in logarithm */
        x /= 2;      /* ready for next position */
        }
```

***Fig 1—Calculate base-2 logarithms** to about 16 bits of precision using the algorithm implemented in this C code.*

```
    }
*   Rodister usage:  D0 argument (input) and logarithm base-2 (output)
*                    D1 logarithm temporary
*                    D2 bit index
*                    D3 scale factor
*
LOG0    MOVEM.L D1-D3,-(A7)     SAVE REGISTERS
        MOVEQ #0,D1             INIT. LOG. TEMP.
        MOVEQ #15,D2            INIT. BIT INDEX
        MOVEQ #14,D3            INIT. SCALE FACTOR
*
LOG1    MULU D0,D0              SQUARE ARGUMENT
        LSR.L D3,D0             RE-SCALE ARGUMENT
        CMPI.W #32768,D0        ARG < BASE-2?
        BLO.S LOG2              YES
*
        BSET D2,D1              NO, SET BIT IN LOGARITHM
        LSR.W #1,D0             READY FOR NEXT POSITION
*
LOG2    DBRA D2,LOG1            LOOP THROUGH THE 16 BITS
*
        MOVE.L D1,D0            RETURN LOGARITHM IN D0
        MOVEM.L (A7)+, D1-D3    RESTORE WORKING REGISTERS
        RTS
```

***Fig 2—You can easily** calculate base-2 logarithms on a μP, as this Motorola 68000 assembly-language subroutine shows.*

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CIRCLE NO 169

Program speeds best-fit 1%-resistor calculations

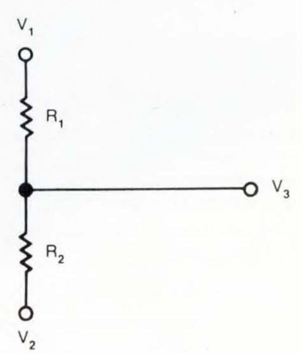
Andrew Dart
Trans-Texas Telegraph Co, Duncanville, TX

The program shown in **Fig 1a** calculates best-fit 1%-resistor values for the voltage divider shown in **Fig 1b,** and it runs 400 times faster than a similar program that appeared as a Design Idea earlier this year (see "Program calculates best-fit 1% resistors," EDN, April 18, pg 286).

The version shown in **Fig 1a** takes advantage of the fact that the 96 standard values for 1% resistors are evenly spaced powers of the 96th root of 10. For each of the 96 values that the program calculates for R_1, it performs only one calculation to find the value of R_2. The program thus eliminates 95 out of 96 of the calculations that the earlier resistor-value-calculation program performed. Note that V_1 can be less than V_2 as long as V_3's value is between V_1 and V_2. **EDN**

```
100 REM New & Improved Version of the
110 REM One Percent Resistor Calculator Program:
120 REM 1% resistor values are based on the 96th root of 10.
130 REM Refer to EIA RS-385
140 DIM RV(99)
150 FOR X=1 TO 96
160  READ RV(X)
170 NEXT X
180 P(0)=1:P(1)=10:P(2)=100:P(3)=1000:P(4)=10000:P(5)=100000
190 CLS:REM Clear the screen
200 INPUT "Enter voltage V1";V1
210 INPUT "Enter voltage V2";V2
220 INPUT "Enter the desired voltage at V3";V3
230 IF V2>V1 THEN F1=1:X=V1:V1=V2:V2=X
240 IF V3>=V1 OR V3<=V2 THEN PRINT "V1 > V3 > V2 please":GOTO 220
250 REM R is the ratio R1:R2
260 R=(V1-V3)/(V3-V2)
270 REM Be sure R is greater than 1
280 IF R<1 THEN F2=1:R=1/R
290 REM Assure 1 < Ratio < 10 by dividing by a power of ten:
300 SF=LEN(STR$(FIX(R)))-2
310 REM SF = Scale Factor
320 R=R/P(SF)
330 REM The inverse of the natural log of the 96th root of ten
340 REM is approximately 41.69227
350 Q=FIX(LOG(R)*41.69227+.5)
360 H=99
370 FOR X=1 TO 96
380  G=0
390  Y=X+Q
400  IF Y>96 THEN Y=Y-96:G=1
410  IF RV(Y)/RV(X) < H THEN H=RV(Y)/RV(X):J=RV(Y):K=RV(X)
420 NEXT X
430 IF G=1 THEN SF=SF+1
440 J=J*P(SF)
450 IF F1=1 THEN Z=J:J=K:K=Z
460 IF F2=1 THEN Z=J:J=K:K=Z
470 PRINT
480 PRINT "With ";V1;"volts at V1"
490 PRINT "and ";V2;"volts at V2"
500 PRINT "if R1 =";J;"ohms"
510 PRINT "and R2 =";K;"ohms"
520 PRINT "then V3 will be ";K*(V1-V2)/(J+K)+V2;" volts"
880 END
890 REM 1% Resistor values:
900 DATA 1.00,1.02,1.05,1.07,1.10,1.13,1.15,1.18,1.21,1.24
910 DATA 1.27,1.30,1.33,1.37,1.40,1.43,1.47,1.50,1.54,1.58
920 DATA 1.62,1.65,1.69,1.74,1.78,1.82,1.87,1.91,1.96,2.00
930 DATA 2.05,2.10,2.15,2.21,2.26,2.32,2.37,2.43,2.49,2.55
940 DATA 2.61,2.67,2.74,2.80,2.87,2.94,3.01,3.09,3.16,3.24
950 DATA 3.32,3.40,3.48,3.57,3.65,3.74,3.83,3.92,4.02,4.12
960 DATA 4.22,4.32,4.42,4.53,4.64,4.75,4.87,4.99,5.11,5.23
970 DATA 5.36,5.49,5.62,5.76,5.90,6.04,6.19,6.34,6.49,6.65
980 DATA 6.81,6.98,7.15,7.32,7.50,7.68,7.87,8.06,8.25,8.45
990 DATA 8.66,8.87,9.09,9.31,9.53,9.76
```

(a)



(b)

Fig 1—This program (a) calculates best-fit 1% resistors *for a divider network* ***(b)*** *and eliminates 95 out of 96 of the calculations performed by a similar program.*

Run Z80 software on an 8085 system

Leo M Almazan
Naval Ocean Systems Center, San Diego, CA

The **Fig 1** circuit shows how to convert an 8085-based µP system to one that runs Z80 software. The scheme involves replacing the 8085 with an NSC800 µP. (The NSC800 is similar to the Z80 internally but has the same bus structure as the 8085). The resulting system is advantageous for those who would rather program for the Z80 than for the 8085.

The main external difference in the Z80 (NSC800) and 8085 µP is the latter's serial-I/O lines SID and SOD; no Z80 instructions can implement these functions. In addition, two discrepancies concern the programmer: The 8085 Trap (nonmaskable-interrupt) input causes a jump to location 24_{HEX1}; the NSC800 equivalent input NMI causes a jump to location 66_{HEX}. Finally, the NSC800 control register for internal interrupts is located at $0BB_{HEX}$, so that address must be free to service a mode-2 interrupt request. EDN

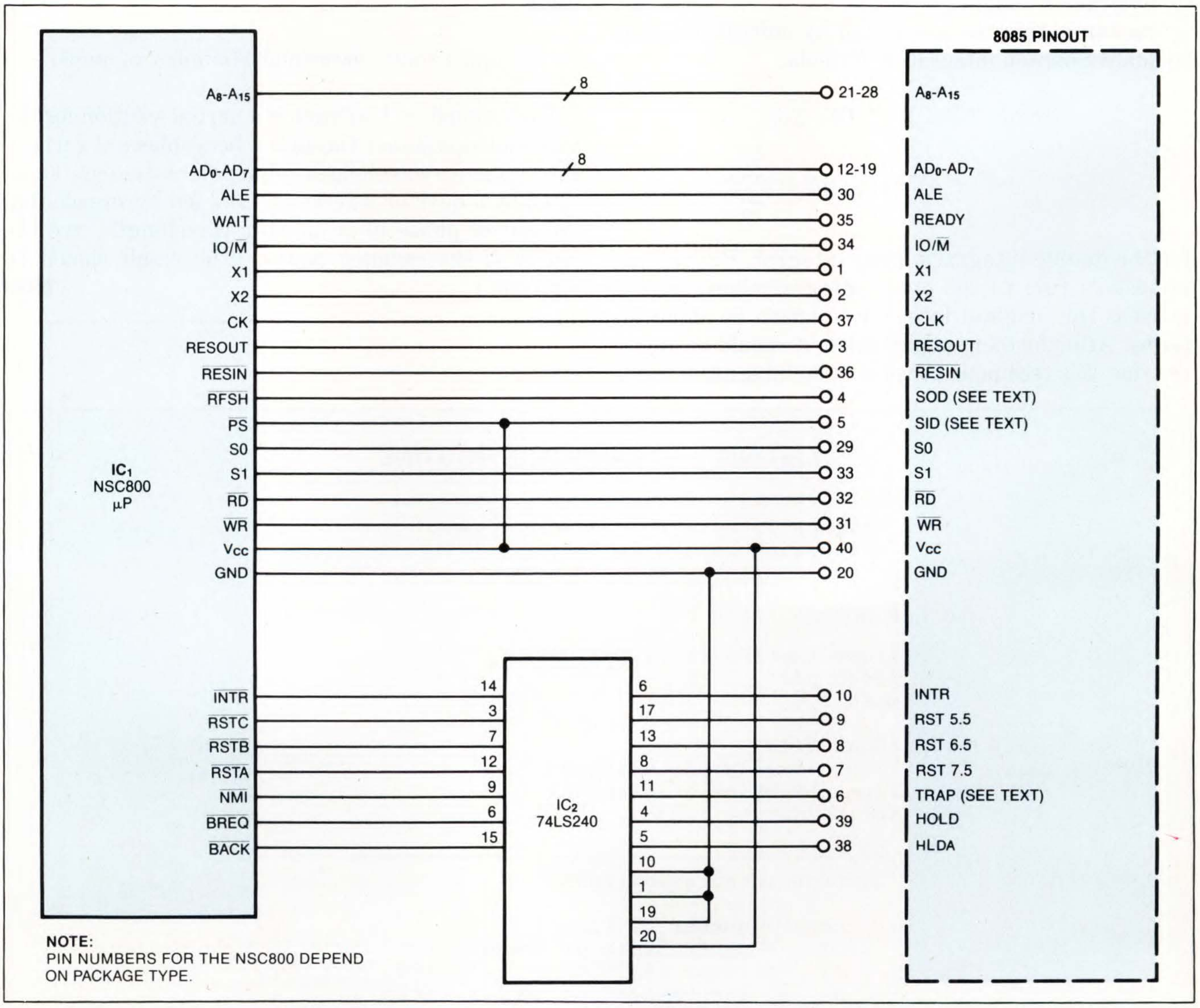


***Fig 1—This circuit lets you substitute** the Z80-like NSC800 for an 8085 µP and thereby obtain a system that can develop and run Z80 software.*

Simpson's rule solves double integrals

A Cameron
Defence Research Centre, Adelaide, SA, Australia

Although one generally uses Simpson's rule to approximate single integrals, you can extend the technique for use in solving double integrals. The C language routine of **Listing 1** contains the required algorithm plus an example, demonstrating that you can apply Simpson's rule to certain complex double integrals that would normally require the application of numerical techniques. In addition, the technique applies equally well to integrals of a higher order.

You can obtain the algorithm by substituting the standard Simpson integration formula,

$$S_X(y_j) = f(x_0, y_j) + f(x_n, y_j) + 4\sum_{i=1}^{\frac{n-2}{2}} f(x_{2i-1}, y_j) + 2\sum_{i=1}^{\frac{n-2}{2}} f(x_{2i}, y_j),$$

for the double integral's inner integral. Reapplying Simpson's rule to the outer integral allows you to express the original integral equation in algebraic terms. After further simplification, it should be apparent that this technique consists of an integration along one axis for each interval on the orthogonal axis, followed by an application of Simpson's rule on the accumulated results along the orthogonal axis.

If $S_X(y_n)$ represents Simpson's rule applied along the x-axis as a function of the position y_n on the y-axis, then

$$\text{SIMPSON} = \frac{h_X * h_Y}{9} (S_X(y_0) + S_X(y_n) + 4 * S_X(y_1) + 2 * S_X(y_2) \ldots \text{etc}),$$

where h_X and h_Y represent the increments between steps:

$$h = (\text{upper limit} - \text{lower limit})/(\text{number of steps}).$$

The example in **Listing 1** is a partial solution for the total radiated power through a hemispherical surface. Two quarter-wavelength monopole antennas, separated by a quarter wavelength and fed by signals that are out of phase by a quarter wavelength, are the source of the radiated power. (The result should be 3.829042.) **EDN**

LISTING 1—C LANGUAGE ROUTINE

```
/*--------------------------------------
 Simpson integration technique for
 evaluating double integrals.
---------------------------------------*/

#include "math.h"

float fxy[100][100],fy[100];
float pi;
main() {

float f();
float llx,lly,ulx,uly,x,y;
float hx,hy,ef,of,simpson;
int nosx,nosy,i,j;

/*---------------------------------------
 Simpson integration constants.

    nos -> number of strips
    ul  -> upper limit of integration
    ll  -> lower limit of integration
    h   -> incremental value per strip
-------------------------------------------*/
```

LISTING 1—C LANGUAGE ROUTINE *(Continued)*

```
    pi=3.1415926;
    nosx=30; nosy=40;
    llx=0.le-8;lly=0.le-8;
    ulx=pi; uly=2.0*pi;
    hx=(ulx-llx)/nosx;
    hy=(uly-lly)/nosy;

    printf (" \n\nDouble integration parameters: \n");
    printf ("  Step size hx and hy:  %f,%f\n",hx,hy);
    printf ("  Number of steps(x,y): %d,%d\n\n",nosx,nosy);

/*
 Calculate all the points within the
 integration region.
*/
    for (j=0; j <= nosy; j++) {
        for (i=0; i <= nosx; i++) {
            x = hx*i+llx;
            y = hy*j+lly;
            fxy[i][j] = f(x,y);
        }
    }

/*
 Now perform a Simpson integration along
 the x axis and accumulate results using
 the y axis variable as an index.
*/
    for (j=0; j <= nosy; j++) {
        of=fxy[1][j];
        ef=0.0;
        for (i=2; i <= nosx-2; i += 2) {
            ef += fxy[i][j];
            of += fxy[i+1][j];
        }
        fy[j]=fxy[0][j]+fxy[nosx][j]+2.0*ef+4.0*of;
    }
/*
 Lastly perform Simpson integration
 along the y axis.
*/
    of=fy[1];
    ef=0.0;
    for (j=2; j <= nosy-2; j += 2) {
        ef += fy[j];
        of += fy[j+1];
    }
    simpson = (hx*hy/9.0)*(fy[0]+fy[nosy]+2.0*ef+4.0*of);

    printf("Result = %f\n\n",simpson);
}

/*
 Enter the function to be integrated here.
*/
float f(x,y) float x,y; {
double xd,yd,zd,zdl;

    xd = x; yd = y;
    zd = pi*cos(xd)/2.0;
    zd = cos(zd);
    zdl = pi*(1.0-sin(xd)*cos(yd))/4.0;
    zdl = cos(zdl);
    zd = zd*zdl;
    zd = pow(zd,2.0)/sin(xd);
    return ( fabs(zd) );
}
```

Bidirectional tachometer offers low error

R L Dave
PDO, Muscat, Sultanate of Oman

The inexpensive circuit of **Fig 1** lets you sense or control shaft rotation. In addition, it provides a tachometer output that tracks bidirectional rotation without error (except the $\pm\frac{1}{2}$-count uncertainty common to digital circuits, that is, $\pi R/P$, where R equals the radius of the encoder disk and P equals pulses/revolution).

Photosensors A and B produce quadrature square

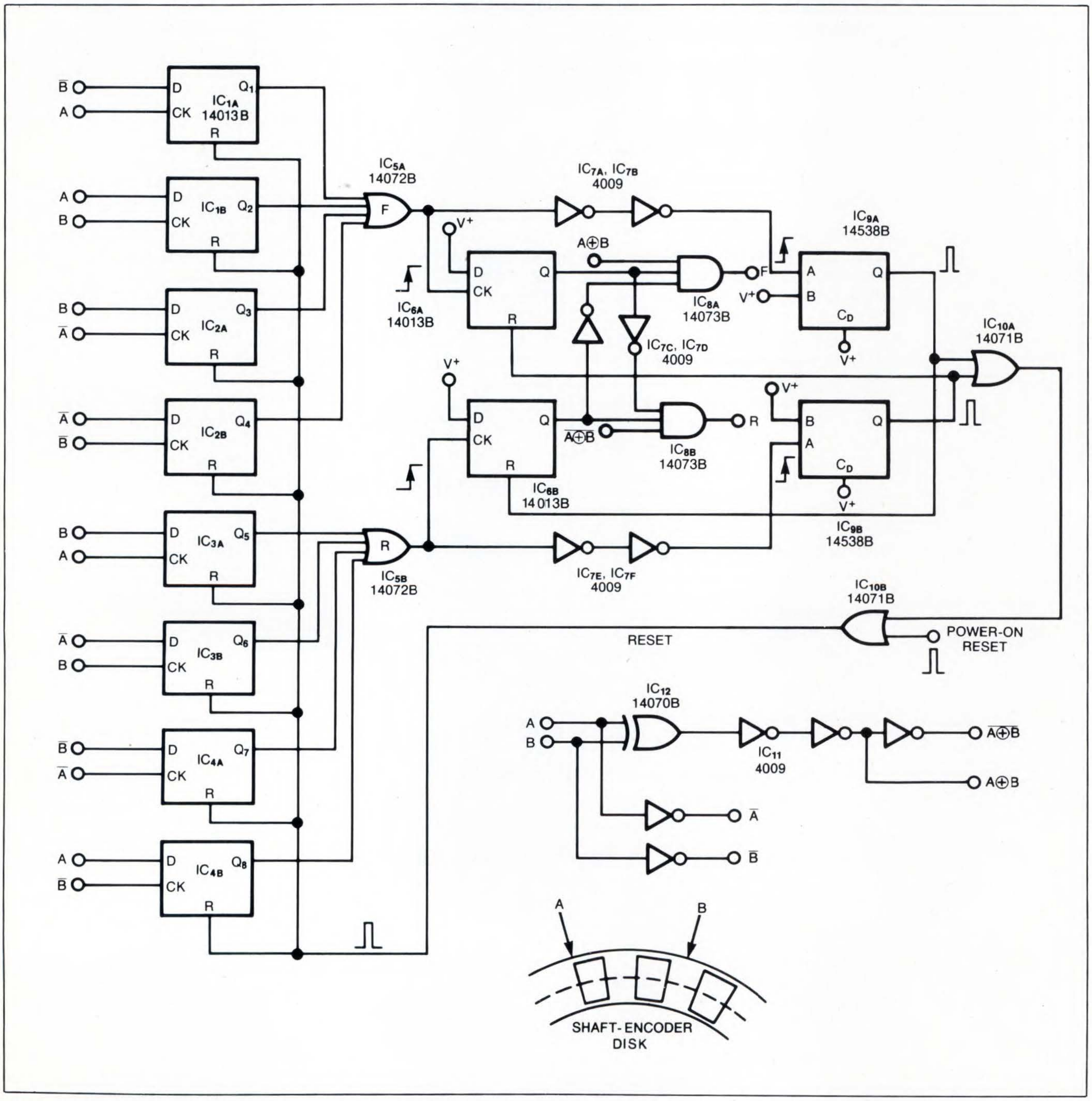


***Fig 1—This circuit converts** the incremental shaft encoder's photosensor outputs A and B to bidirectional tachometer outputs F (forward) and R (reverse).*

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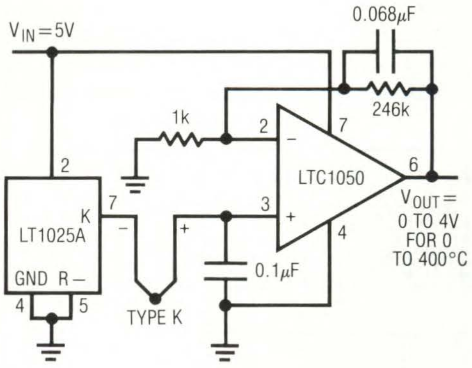

LINEAR TECHNOLOGY

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CIRCLE NO 171

waves **(Fig 2)** as the encoder disk **(Fig 1)** turns. Direction-sense latches IC_1 through IC_4 respond to the eight possible states of A and B, causing the OR gates IC_{5A} and IC_{5B} to identify forward (F) or reverse (R) rotation. The 3-input AND gates IC_{8A} and IC_{8B} provide tachometer pulse-count outputs proportional to the forward or reverse rpm.

IC_9 provides resets to the IC_6 latches. IC_{10} combines these reset pulses to provide a reset to the eight input latches for every change in the state of waveforms A and B, which ensures that the circuit is always ready to detect a change in the direction of rotation. **EDN**

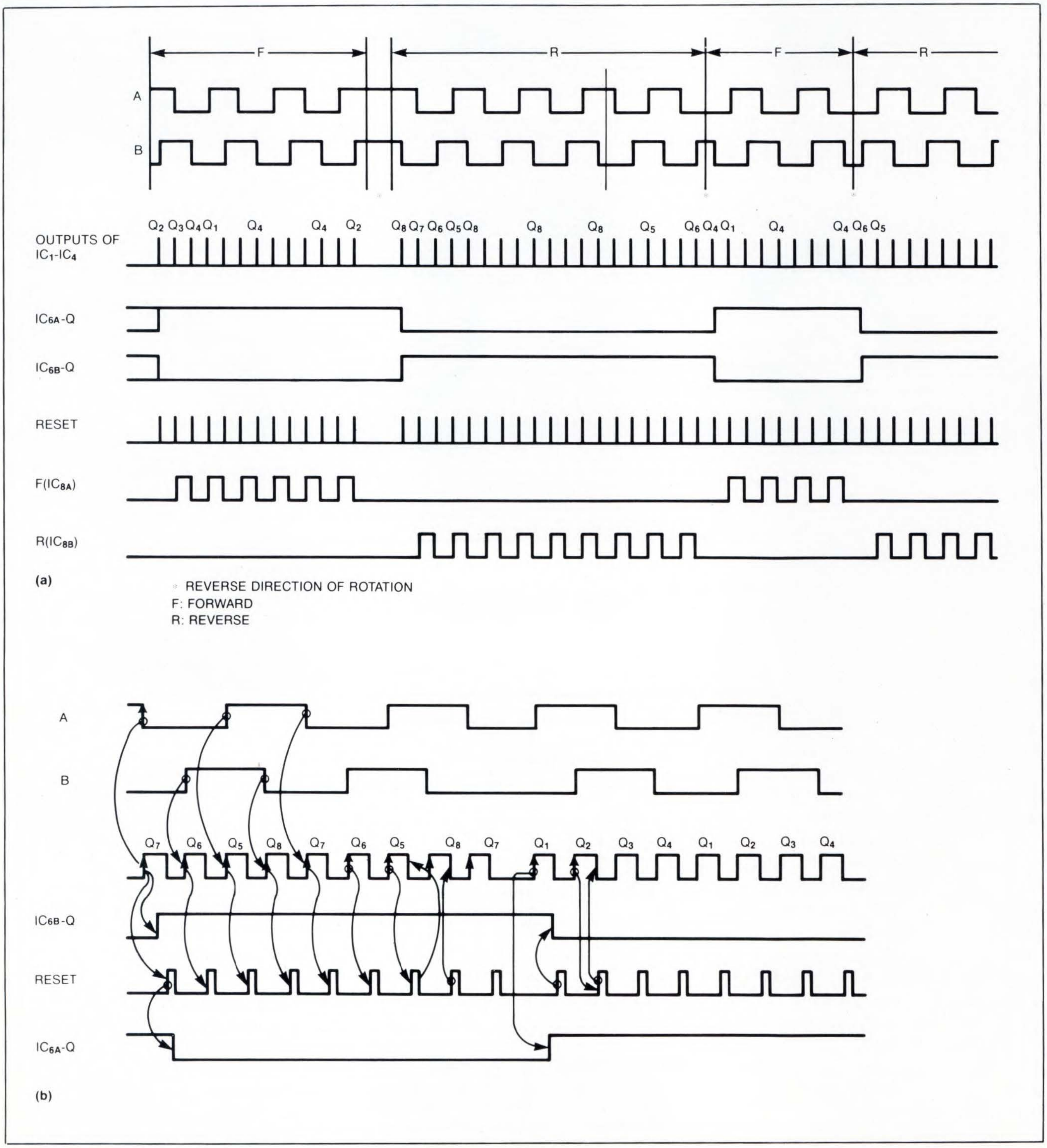

Fig 2—These waveforms (a) illustrate the operation of Fig 1. The expanded traces (b) offer greater clarity.

Circuit deletes power-line cycles

Steve Ross
Kentrox Industries, Portland, OR

The circuit of **Fig 1** is useful in testing the response of equipment to a momentary loss of power. Each time you depress the normally on start switch, the circuit deletes zero to seven full or half cycles from the line voltage applied to the load. You can create various load-voltage waveforms by appropriate settings of the 8-pole DIP switch.

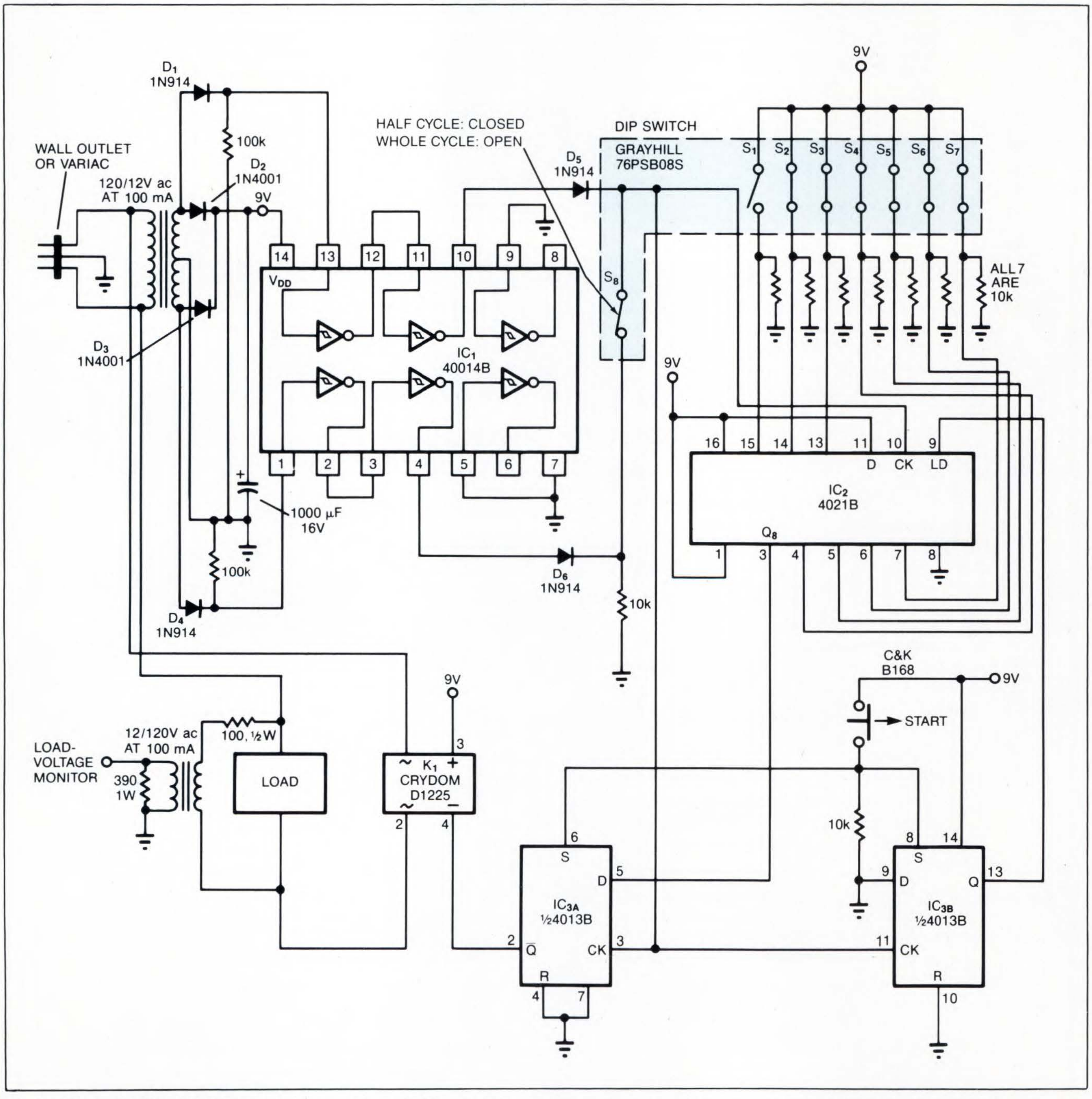

***Fig 1—This circuit deletes a sequence** of whole or half cycles from the line voltage applied to the load according to a 7-cycle pattern that you program using the DIP switch's sections S_1 through S_8.*

The simple full-wave rectifier (diodes D_2 and D_3) supplies about 9V to the logic ICs. Diodes D_1 and D_4 also rectify the stepped-down line voltage and apply alternate half cycles to the Schmitt-trigger inverters in IC_1. The inverters square these half-sinusoidal waveforms, and diodes D_5 and D_6 constitute an OR gate that combines the inverter outputs for use as a clock signal to IC_2 and IC_3.

Section S_8 of the DIP switch determines whether the circuit deletes half or full cycles. The remaining sections (S_1 through S_7) determine the number and serial position of the cycles deleted. Shift register IC_2 converts the information in these sections to a serial bit stream, which controls the solid-state relay K_1 via flip-flop IC_{3A}. (An open switch deletes a full or half cycle by opening the relay, removing line voltage from the load during that period.)

In each scope photo of **Fig 2,** the top traces show the load voltage (which you measure at the monitor terminal,) and the bottom traces show the corresponding control voltage for the solid-state relay K_1 (which you measure at IC_{3A}, pin 2). You trigger the scope on the falling voltage (IC_3, pins 6 and 8), which you create by activating the start button. **EDN**

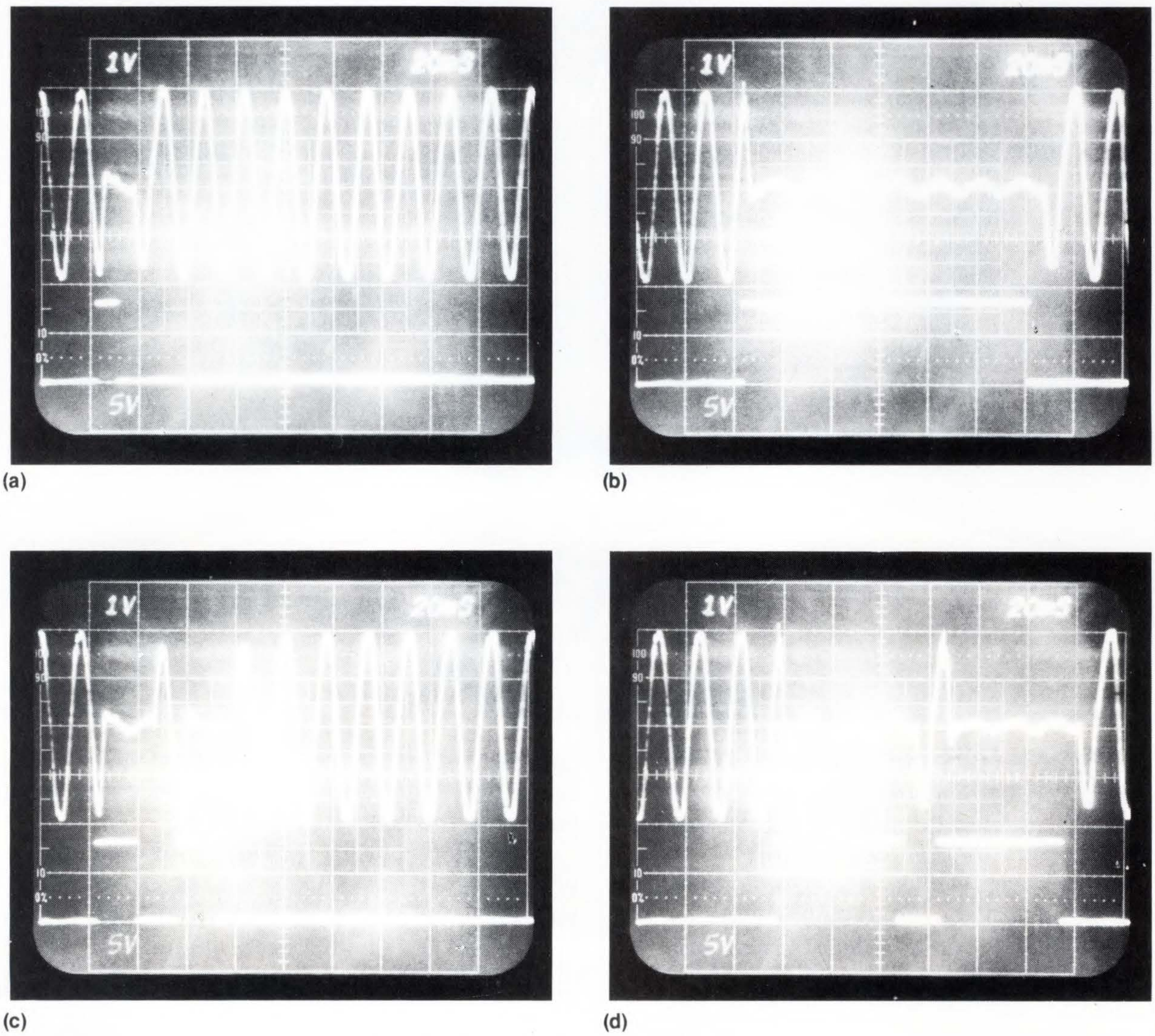

Fig 2—The top traces in these photos show the load-voltage waveforms, *following activation of the start switch, for various settings of the DIP switch: With S_1 open and all others closed, one half cycle is deleted* ***(a);*** *with all switches open, seven full cycles are deleted* ***(b);*** *with either S_1, S_2, S_3, and S_6 open or S_1, S_4, and S_8 open, two alternate full cycles are deleted* ***(c);*** *and with all switches open except S_4, three full cycles on either side of a single full cycle are deleted* ***(d).***

Thermistor bridge senses air flow

Larry G Smeins
Hewlett Packard Co, Loveland, CO

Using the thermistor-bridge circuit shown in **Fig 1**, you can detect system-cooling air losses caused by filter or inlet blockage or fan failure. One thermistor is mounted directly in the air flow; the other is baffled. The exposed thermistor senses the temperature in the cooling system; the baffled thermistor senses the ambient temperature in still air. As long as the thermistors are at different temperatures, the bridge stays unbalanced, and the circuit produces a logical high, indicating that the cooling system is working. If the air flow stops, the exposed thermistor will reach ambient temperature, the bridge will become balanced, and the circuit will indicate ventilation-system failure by producing a logical low.

The bridge circuit's matched thermistors are biased by matched-current sources. Two LM10C operational amplifiers act as constant-current sources, and an LM311 comparator senses the difference between the voltage drops across the thermistors, producing the logical high when the bridge is unbalanced and the logical low when the bridge is balanced. You use a 20-kΩ potentiometer to set the comparator's threshold; this setting determines the minimum air flow that will cause the circuit to produce a logical high. **Fig 2** shows how you can mount and baffle the thermistors. Note the thermistors' long leads; they maximize the devices' thermal isolation.

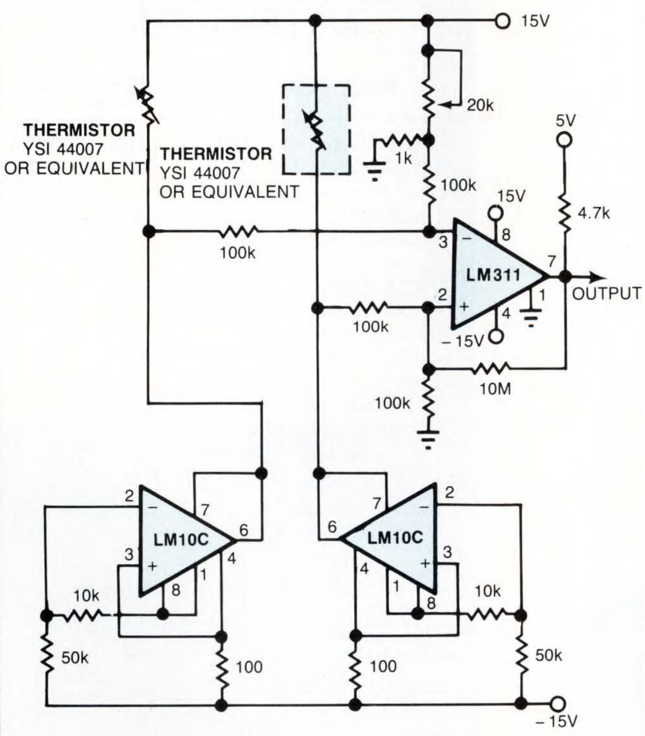

Fig 1—Using this thermistor-bridge circuit, you can detect the loss of system-cooling air caused by filter or inlet blockage or fan failure. As long as the thermistors are at different temperatures, the bridge stays unbalanced, and the circuit produces a logical high, indicating that the cooling system is working.

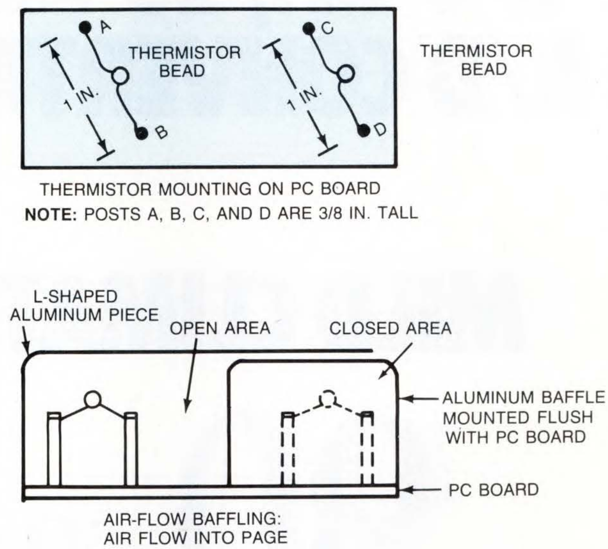

Fig 2—Mount the thermistors on a pc board and baffle one thermistor with an aluminum can mounted tightly to the board. The baffle removes one thermistor from the system-cooling air flow, keeping the thermistor at ambient temperature. The long leads maximize the thermistors' thermal isolation.

By replacing **Fig 1**'s comparator with a differential amplifier, you can build a circuit that measures the system-cooling air flow. Because only one of the thermistors is mounted in moving air, the differential amplifier's output is proportional to the air velocity. Using a given thermistor/bias combination, you can derive a calibration chart for voltage output vs air flow.

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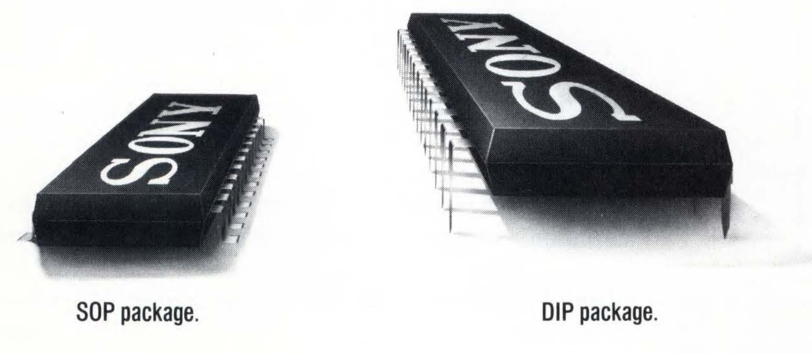

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CIRCLE NO 174

Fortran program calculates op-amp noise

James S Taylor
James S Taylor & Associates, Fairborn, OH

Calculating the input-referred noise of an op-amp circuit isn't difficult, but making this calculation for several different op amps, over different bandwidths and for different circuit configurations, can become a chore. **Listing 1** is a Microsoft Fortran program that simplifies this task. It computes the total input-referred noise for an op-amp circuit (based on the test circuit of **Fig 1**), is flexible enough to handle a range of options, and runs on IBM PCs and compatibles.

The program prompts you for the external resistor values and such op-amp noise parameters as noise-voltage and noise-current densities (**Listing 2**). (For those parameters, use a frequency well above the op amp's noise-corner frequency—1 kHz, for example.)

Listing 2 also includes an example of **Listing 1**'s output for the OP-27A op amp. The program presents the data inputs and the output on your CRT screen for verification before printing. Boltzmann's constant and the absolute temperature are listed in separate data statements, so you can easily modify the program to calculate the resistor's thermal noise at different temperatures. **EDN**

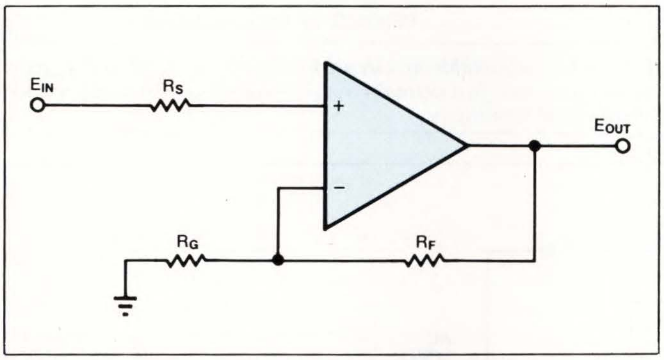

*Fig 1—**The program of Listing 1 calculates** the total circuit noise referred to the input of the op amp for this noninverting-gain configuration.*

References

1. Precision Monolithics Inc, *Application Note AN-15, Minimization of noise in operational amplifier applications*, Santa Clara, CA.
2. National Semiconductor Corp, *Application Note AN-104, Noise specs confusing?* Santa Clara, CA.
3. Signetics Corp, *Application Note AN-104, Explanation of noise*, Sunnyvale, CA.

LISTING 1—CALCULATION OF OP-AMP NOISE

```
D Line# 1        7                                   Microsoft FORTRAN77 V3.31 August 1985
C         NOISE    .FOR
C
C         THE SOURCES OF NOISE IN AN OP-AMP CIRCUIT ARE:
C
C         1.   THERMAL NOISE IN THE SOURCE RESISTANCE SEEN BY THE + INPUT
C         2.   THERMAL NOISE IN THE SOURCE RESISTANCE SEEN BY THE - INPUT
C         3.   NOISE CURRENT THROUGH THE SOURCE RESISTANCE AT THE + INPUT
C         4.   NOISE CURRENT THROUGH THE SOURCE RESISTANCE AT THE - INPUT
C         5.   INTERNAL OP-AMP NOISE WHICH APPEARS AS A VOLTAGE ACROSS THE
C              DIFFERENTIAL INPUT
C
          REAL*4       IWN,  K,    LBW,  NE,  NI,   NIN,  NIP,  NOISE,
        &              N6,   NRSP, NRSN
          LOGICAL      NEW,  AGAIN
          CHARACTER*8 OPAMP
          CHARACTER*1 ANSWER
          DATA         K / 1.38E-23 /, T / 300.0 /, NEW / .TRUE. /
C    OPEN FILES
          OPEN (UNIT = 1, FILE = 'CON')
          OPEN (UNIT = 2, FILE = 'CON')
C    GET INPUT
     1000 WRITE (1, 1) ' ', CHAR(27), '[', '2', 'J'
          IF (NEW) THEN
C    THE OP-AMP ID IS USED FOR LABELLING THE PRINTOUT
            WRITE (1, 2)
            READ (2, 3) OPAMP
```

AC circuit breaker has adjustable threshold

Kurt French
C F Electronics Inc, Commack, NY

Protecting sensitive electronic equipment from ac overcurrent conditions in the 100 to 300% range often proves to be difficult. At 125% of rated current, for example, a so-called "fast-acting" breaker probably won't trip at all **(Fig 1)**, and a fast-acting fuse takes about 10 sec to blow. The fuse will blow in 0.02 sec at 300% of rated current, but damage can occur at that current level. The fast-acting breaker requires nearly 700% of rated current to respond in 0.02 sec.

The adjustable circuit breaker shown in **Fig 2** responds in 0.02 sec under all conditions (provided you select a fast relay for K_1). For moderate overload conditions, then, it's preferable to the fuse or the fast-acting breaker. The toroid transformer (T_1) senses ac load current and produces an ac signal at the wiper

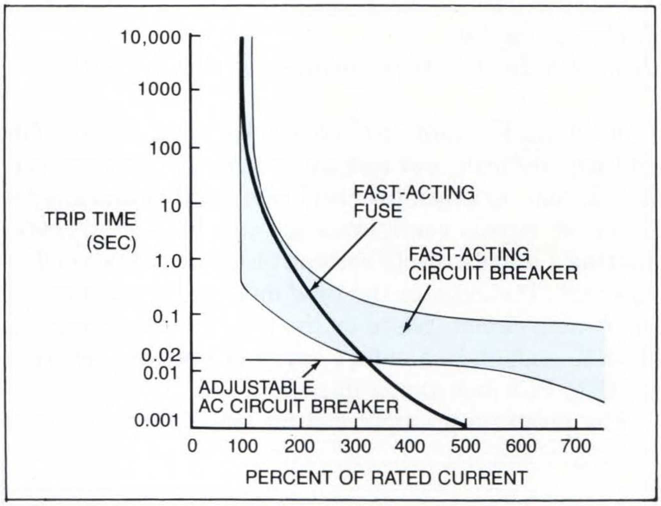

Fig 1—The adjustable ac circuit breaker *shown in* ***Fig 2*** *is faster than a so-called "fast-acting" circuit breaker or a fuse under moderate overload conditions.*

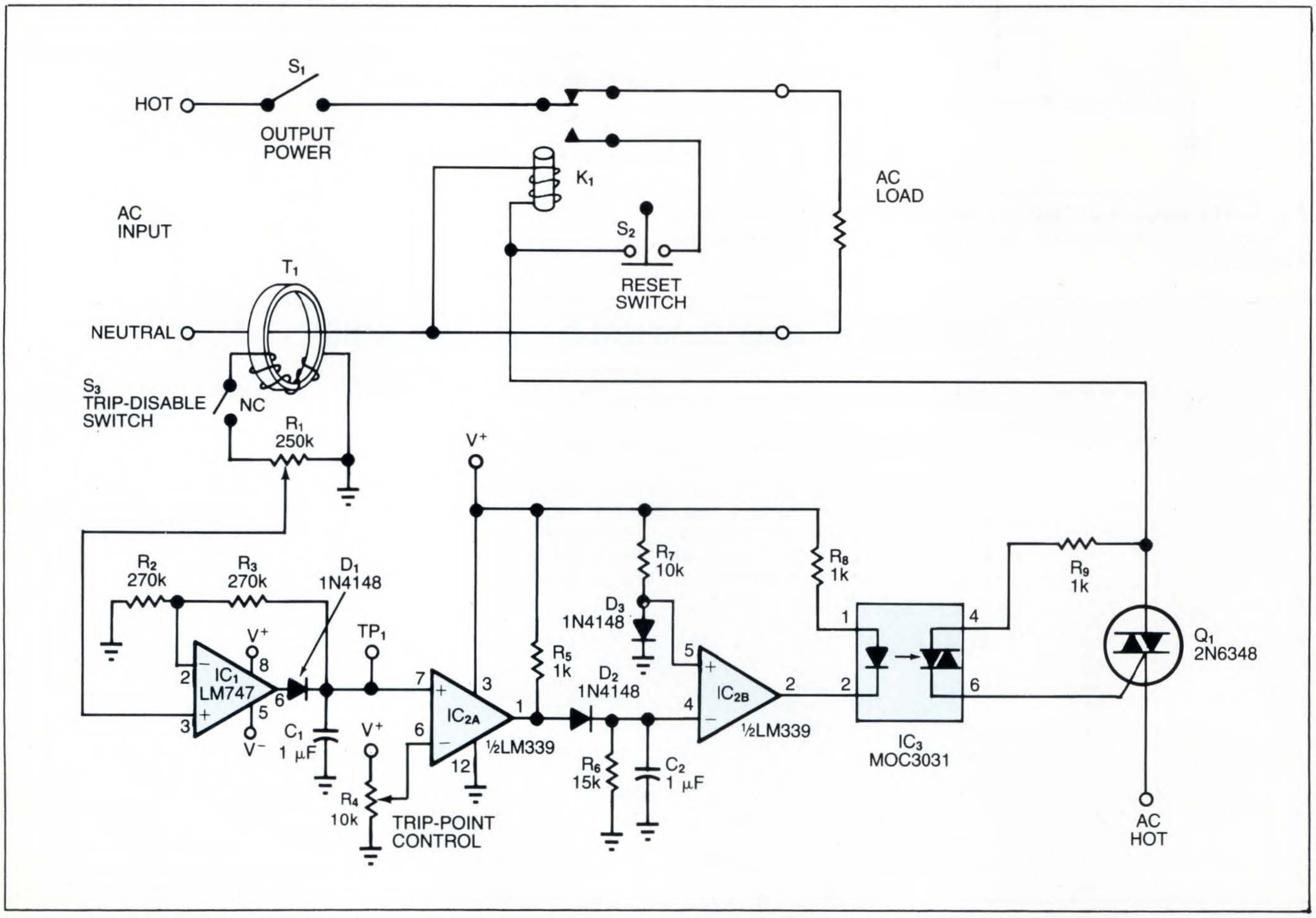

Fig 2—This ac circuit breaker features *an adjustable trip point, high speed, and a fast relay controlled by an optically isolated triac. If you need additional protection for heavy overload conditions, you can connect a fast-acting fuse.*

of R_1 when switch S_3 is closed. Diode D_1 rectifies this signal to produce a positive voltage at the test point (TP_1). Because R_1 allows you to calibrate this voltage, the circuit accommodates a variety of current-sense transformers.

To calibrate the trip threshold, you apply the maximum expected overload and adjust R_1 until the TP_1 voltage is 0.7V below the positive saturation level for IC_1. Then you adjust R_4 for the desired trip point. To reset the circuit breaker after it has tripped, you must open S_1 or S_2. **EDN**

Reconstruct missing sync pulses for VCR

James A Work Jr,
Syntex Corp, Palo Alto, CA

By using **Fig 1**'s circuit, you can reconstruct the equalizing and vertical pulses that are often lost when a VCR (a Panasonic NV-8950, in this case) is in the pause or slow-motion mode. Without these pulses, the VCR's digitizer loses its sync at the top of the frame, causing horizontal distortion and instability (flag waving) at the top of the digitized picture.

The circuit reconstructs the equalizing-pulse and vertical-sync-pulse intervals with compensating pulses. Switch S_1 selects normal-speed sync (circuit bypass) or slow-speed sync (circuit in line). **Fig 2** shows the waveforms at various points in the circuit. The comparator IC_1 picks off (via pin 7) the composite-sync information from the bottom of the composite video signal. One-shot IC_{2A} and type D flip-flop IC_3 form a pulse-

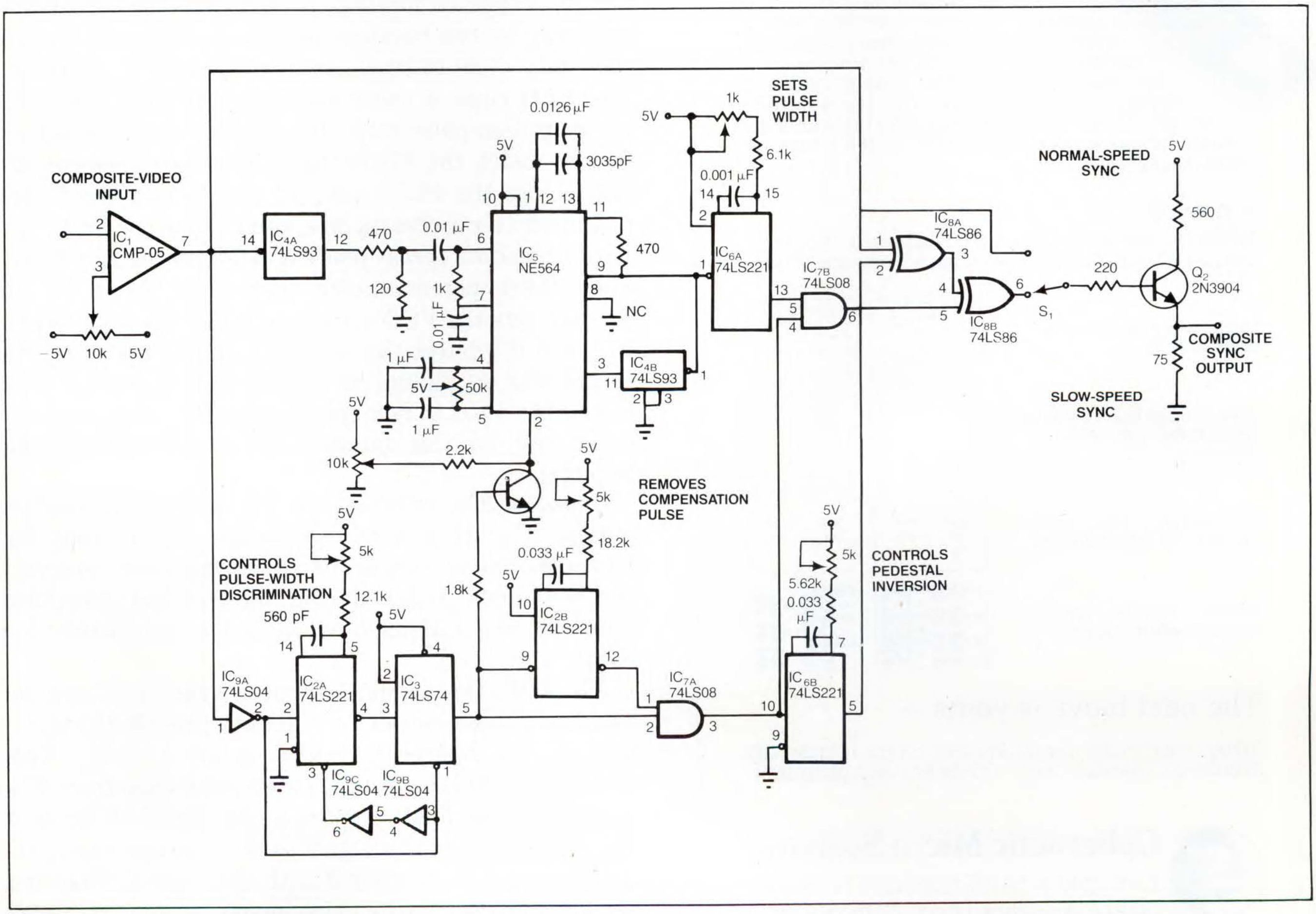

*Fig 1—**Your VCR won't lose sync** in the pause or slow-motion modes when you use this circuit to restore the missing sync pulses.*

DESIGN IDEAS

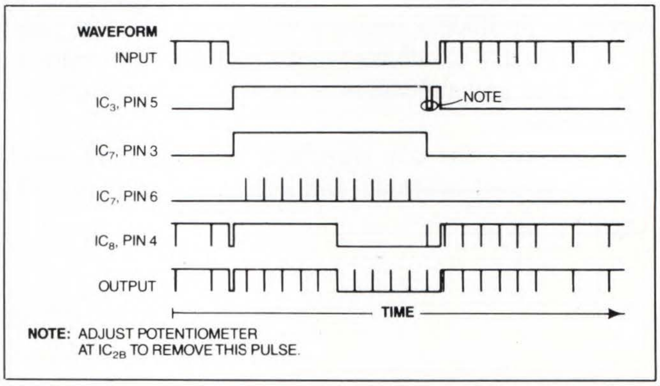

***Fig 2—These waveforms show how Fig 1's circuit** reconstructs the missing sync pulses.*

width detector that ignores pulses longer than 6 μsec. Because the horizontal-sync pulses are 4.77 μsec long, the pulse-width detector (pin 5 of IC_3) changes state only when it sees the recorder's vertical-blanking pedestal. AND-gate IC_{7A} and 1-shot IC_{2B} shut off the pulse-width detector, IC_7's pin-3 output. Another 1-shot, IC_{6B}, defines the first equalizing period before the vertical-sync-pulse interval via its output to pin 2 of XOR-gate IC_{8A}.

Phase-locked loop IC_5 generates the compensation pulses. A type JK flip-flop, IC_{4A}, divides the horizontal-sync rate by two because the PLL's VCO must have a 50% duty cycle to track its input frequency properly. The VCO runs at twice the horizontal-sync rate (the compensation-pulse rate); IC_{4B} divides the feedback by four to match the PLL's input frequency. The capacitors across the PLL's pins 12 and 13 and the 50-kΩ potentiometer across its pins 4 and 5 tune the VCO; the 1-μF capacitors across pins 4 and 5 form the loop filter. The 10-kΩ potentiometer, connected from 5V to ground, sets the VCO's tracking range via pin 2. When IC_{2A} and IC_3 detect the vertical-blanking pedestal, IC_3 switches Q_1 on, pulling pin 2 of the PLL to ground. This causes the VCO to run open loop at the compensation-pulse rate for the duration of the vertical-blanking pedestal.

One-shot IC_{6A} provides the 4.45-μsec compensation pulses; IC_{7B} gates these. Although RS-170 calls for 2.54-μsec pulses during the equalizing-pulse intervals and 4.45-μsec pulses during the vertical-sync-pulse intervals, the 4.45-μsec pulses prove satisfactory for both.

IC_{8A} XORs the original composite-sync signal and the equalizing-pulse output from IC_{6B} to provide the envelope for the desired waveform at pin 4 of IC_8. This envelope is XORed with the gated pulse train from IC_{7B} to produce the final composite-sync signal at pin 6 of IC_{8B}. You can feed this signal to the digitizer's composite-sync input or combine it with the original video and send it to the composite video input. **EDN**

Feedforward amplifier reduces distortion

Michael Ellis
Scientific Atlanta, Norcross, GA

You can employ feedforward techniques to reduce distortion in wideband RF amplifiers; the audio amplifier in **Fig 1** illustrates the feedforward principle, even though feedforward techniques offer no significant advantage in the audio-frequency range. (Both feedforward and feedback techniques reduce distortion in amplifiers, but each approach carries a distinct penalty. Feedback loops are subject to instability, whereas feedforward amplifiers are inherently stable but require an additional error amplifier.)

In **Fig 1**, the main amplifier has a gain of 10, but it introduces some distortion (D) in the amplification process. This component appears at the error amplifier's output (−D), but the signal components cancel at that amplifier's summing junction. In turn, the distortion component cancels in the output voltage divider, leaving the desired output of $-10V_{IN}$.

The feedforward technique allows amplification at RF frequencies without stability problems. In an RF amplifier, a directional coupler replaces the output 10-kΩ/10-kΩ divider. The coupler cancels the distortion while maintaining a 50Ω (or 75Ω) output impedance. CATV amplifiers use feedforward techniques, for example, to transmit 60 TV channels (54 to 450 MHz and higher) for 30 miles. **EDN**

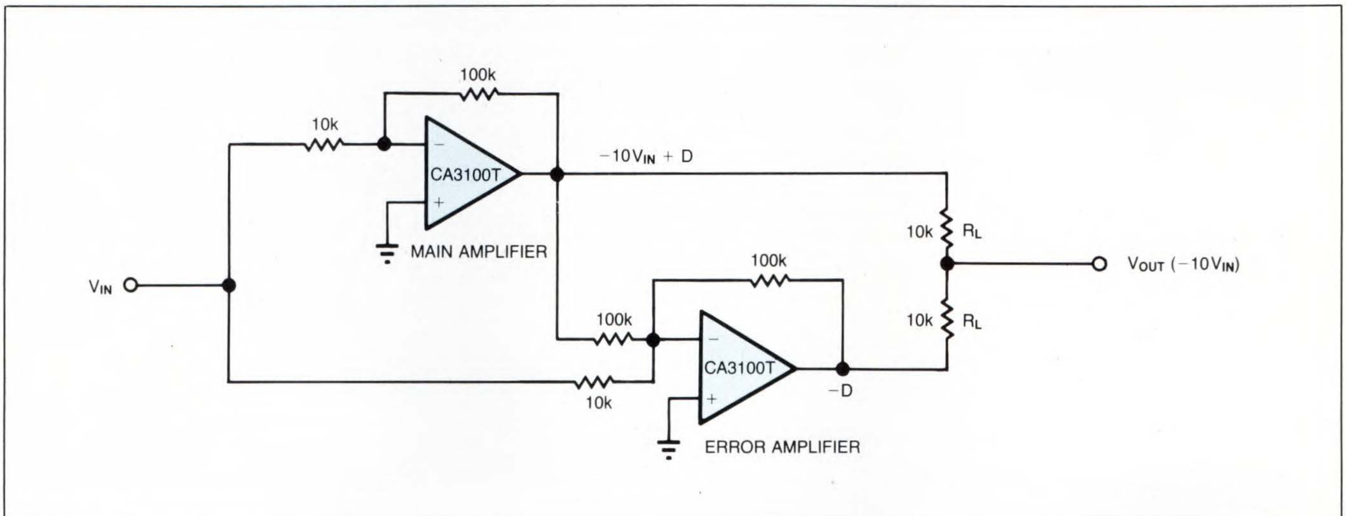

***Fig 1—A feedforward error amplifier** provides cancellation of the main amplifier's distortion products (D) while preserving the desired ($-10V_{IN}$) output.*

Variable-gain amplifier uses matched FETs

Burton S Abrams and Daniel R Frey
Zeger-Abrams Inc, Glenside, PA

A FET can vary the gain of an amplifier by serving as a variable-resistance element, but because the FET's pinch-off voltage varies with temperature and from unit to unit, the control voltage for a particular gain is not fixed. In **Fig 1**, though, a given control voltage $V_{CONTROL}$ produces the same channel resistance in the gain-control FET Q_{1B} for different FET pairs regardless of any variation in their parameters.

The lower circuit (IC_2) is a generalized inverting amplifier whose dc gain varies inversely with the channel resistance of Q_{1B}. The top half of the circuit

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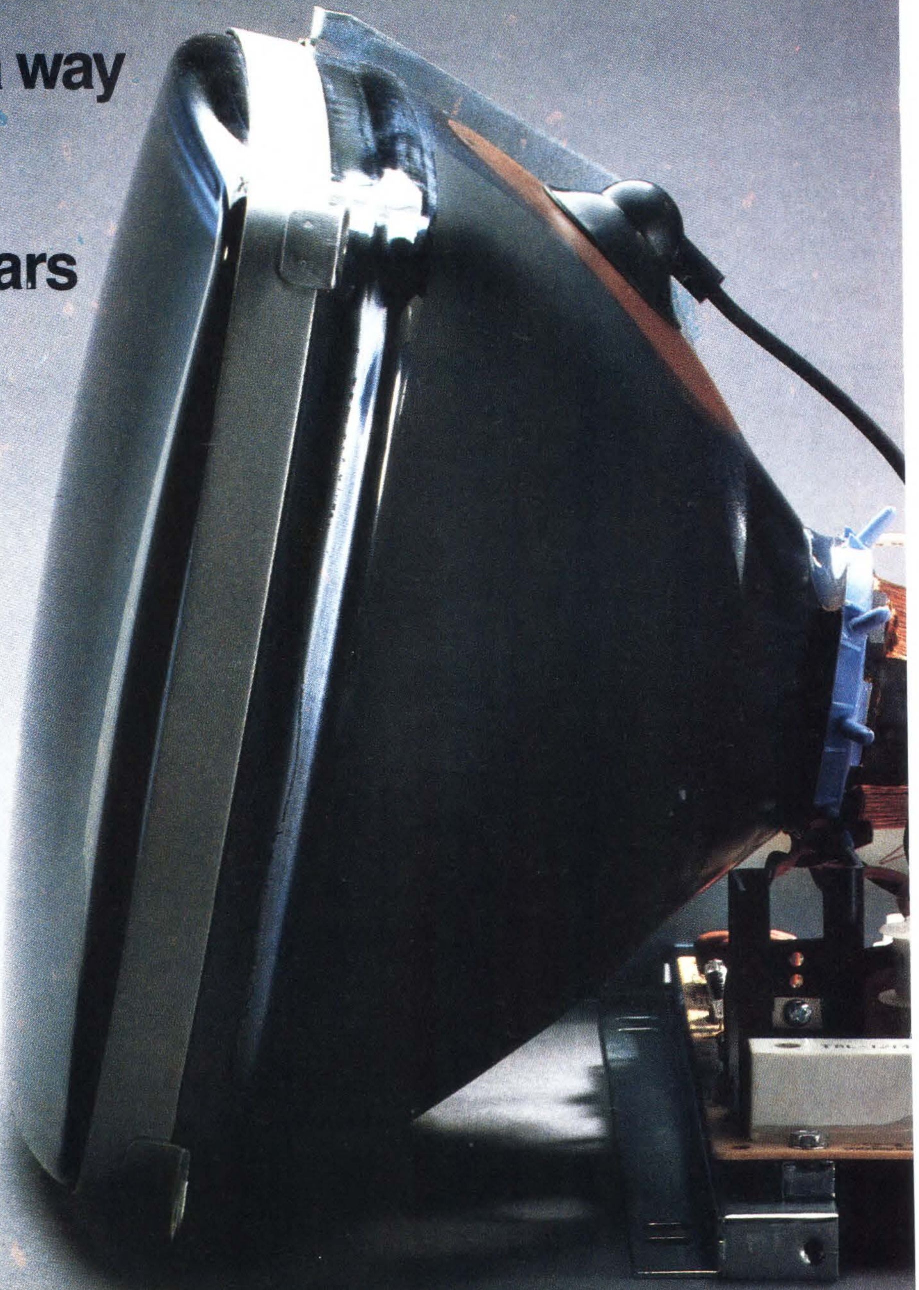

The real challenge is to keep it busy for that long.

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(IC_1) generates a gate-to-source voltage for master FET Q_{1A} that applies to the slave FET Q_{1B} as well.

You apply the negative voltage $V_{CONTROL}$ to set a constant current through R_1 that flows into the source of Q_{1A}. Op amp IC_1 adjusts Q_{1A}'s gate voltage to accommodate this current. Because the small positive voltage V_{BIAS} is fixed, Q_{1A}'s channel resistance must always assume the same value in response to a given value of $V_{CONTROL}$. And because Q_{1B} is a closely matched FET with the same gate-source voltage, it will assume the same channel resistance as Q_{1B}.

V_{BIAS} should be much smaller than the FET's pinch-off voltage so that the FET will not operate in its saturation region. And R_1 must be large enough to avoid demanding a lower resistance than Q_{1A} can provide.

The circuit in **Fig 2** includes additional refinements that compensate for other undesirable characteristics of Q_{1B}. Q_{1B}'s resistance is not only a function of gate-to-source voltage but of drain-to-source voltage as well, which varies with the input signal. The resulting output nonlinearity becomes more pronounced with an increasing signal level. In a familiar approach, the 10-kΩ resistors R_1 and R_2 mitigate this effect by applying about half the signal voltage to Q_{1B}'s gate bias voltage.

R_1 and R_2 also divide in half the gate voltage applied to Q_{1B} by the output of IC_1, so R_3 and R_4 are added to reduce Q_{1A}'s gate voltage by the same amount. Still, signal distortion is noticeable when Q_{1B}'s resistance is high. A diode-resistor network shunts Q_{1B} to compensate for this distortion at the expense of gain-control range. The circuit provides a 20-dB gain-control range for ±1V-max input signals, and it exhibits a maximum 7% output distortion—sufficient for use as an integrator within a phase-locked loop, for example. **EDN**

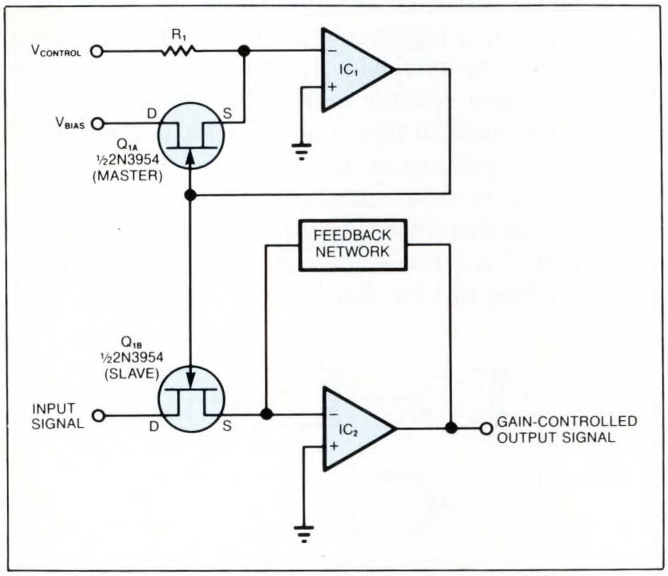


***Fig 1—You use the negative voltage $V_{CONTROL}$** to set this amplifier's gain. The matched dual-FET circuit ensures that a given gain is unaffected by the use of different FET pairs or by the effect of temperature on FET parameters.*

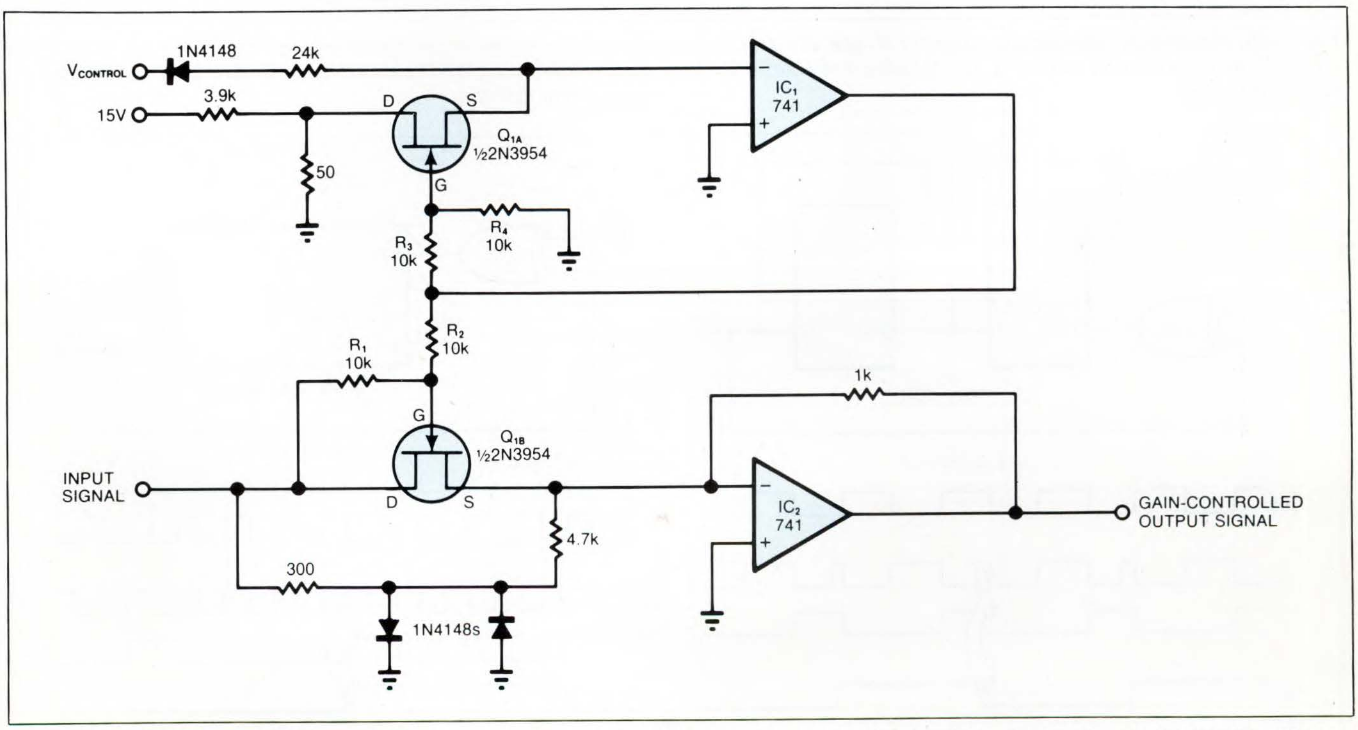


***Fig 2—This circuit is similar to that of Fig 1,** but it includes refinements that compensate for signal distortion caused by high FET resistance and for distortion caused by varying drain-to-source voltage.*

Frequency divider generates 50% duty cycle

Andrzej Partyka
Ademco, Syosset, NY

Fig 1 is the general representation of a digital frequency divider that divides by any odd number (M=2N−1) and always produces an output with a symmetrical duty cycle. (The duty cycle for an ideal waveform is $t_L/(t_L+t_H)=t_L/T$, where L and H refer to the low and high portions of the waveform, and T is the period). The duty cycle of the divide-by-N circuit's output can range from 1/2N to (1−1/2N).

Fig 2a shows the same divider circuit for the case M=3 (and therefore N=2). Because the duration of each half period at V_{OUT} is 1½ CLK periods, one output period equals three input periods. Note that you can simplify some applications by using the Q outputs for the A and B waveforms (in place of $\overline{Q}$).

To divide by a higher odd number such as 9 (N=5), you can use any available divide-by-5 circuit—eg, the 74XX90 decade counter in **Fig 2b.** The output duty cycle of the internal divide-by-5 circuit will not affect the output symmetry of the overall divider.

By adding an AND gate, you can build a programmable circuit that divides by any integer greater than 2 and produces a symmetrical output **(Fig 3).** The delay through a long divider chain, however, limits the maxi-

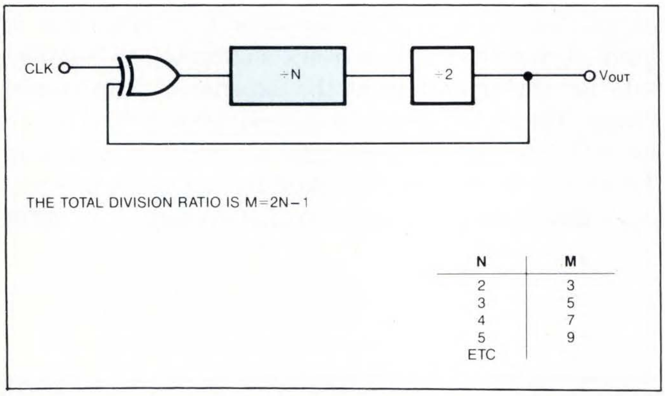


Fig 1—By choosing an appropriate value for N, you can divide *the digital CLK frequency by a desired odd number and obtain a 50% output duty cycle.*

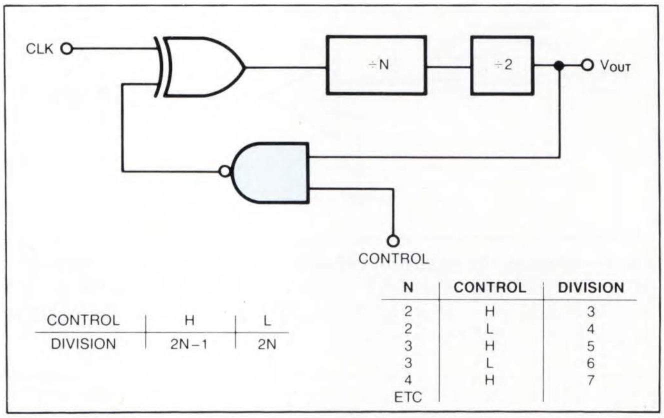


Fig 3—Adding an AND gate *lets you program* ***Fig 1's*** *circuit for even or odd division.*

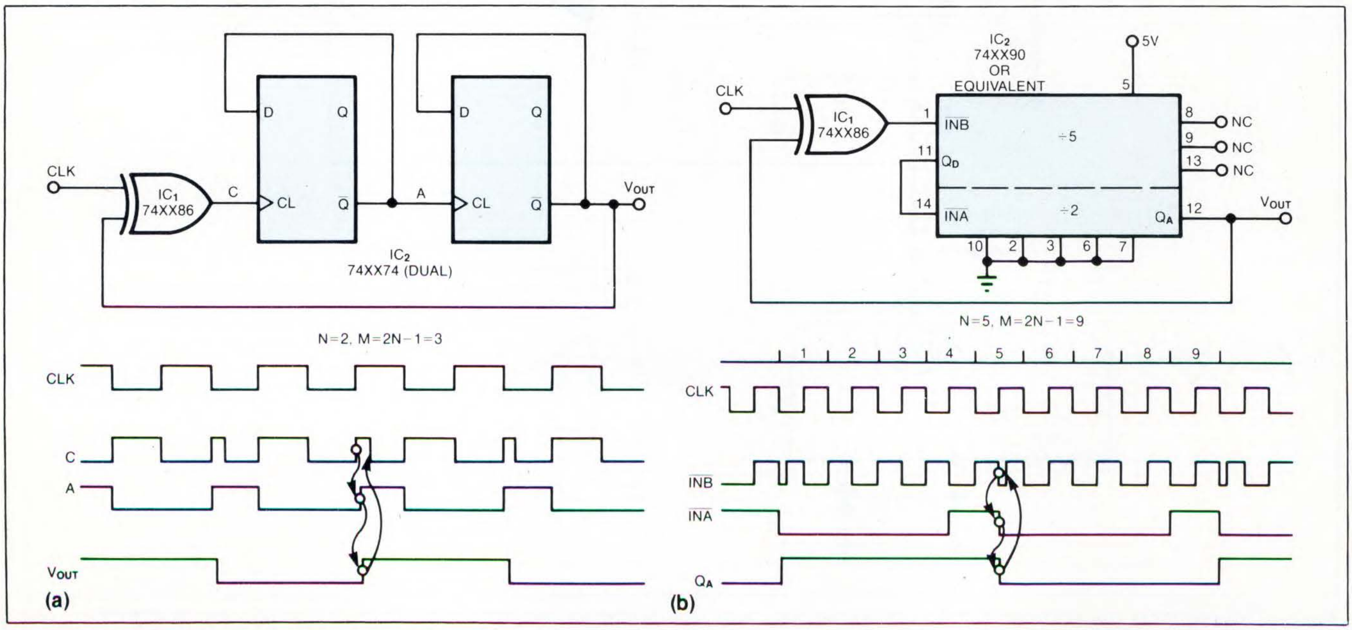


Fig 2—Here, you can see the Fig 1 circuit's *implementation of a divide-by-3 operation* ***(a)*** *and of a divide-by-9 operation* ***(b).***

mum CLK frequency; that is, the sum (t_{SUM}) of the propagation delays in the XOR gate, N-divider circuit, 2-divider circuit, and Control gate must be less than one-half the CLK period ($t_{CLK}/2$).

You can increase the maximum CLK frequency by adding a flip-flop (**Fig 4**). In this configuration, only the lower of two constraints ($t_{FF}<t_{FF}/2$ and $t_{FF}+t_{SUM}<(N-½)t_{CLK}$) limits the CLK frequency. A circuit using LSTTL logic, for example, imposes a 5-MHz limit on **Fig 3** and a 12.5-MHz limit on **Fig 4**. **EDN**

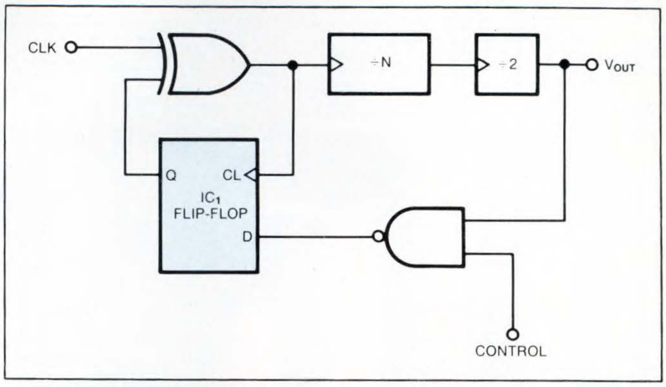


Fig 4—Adding a flip-flop (IC₁) *to the* ***Fig 3*** *circuit enables operation at a higher CLK frequency.*

Improve voltage-controlled current source

Giovanni Stocchino,
FATME, Rome, Italy

Although you can use various methods to design voltage-controlled current sources, the design you use to eliminate one problem can easily lead to other problems. By using op amps and feedback, though, you can build a circuit that furnishes high precision, wide output-current range, high ac/dc output impedance, good temperature stability, low noise, and high input impedance.

As **Fig 1** shows, you can use an emitter follower and various circuit techniques to compensate for the inaccuracies introduced by parameters such as the transistor's base current and wiring resistance (see "Op amps compensate current source," EDN, September 15, 1983, pg 227). This approach, however, introduces the problems of lower input impedance and higher equivalent input-noise-voltage contribution from input resistors R_{IN}. Moreover, the op amp's input-offset current produces a temperature-dependent offset voltage across R_{IN} that increases the total output-current error. Finally, the error introduced by the transistor's temperature-dependent input impedance also reduces

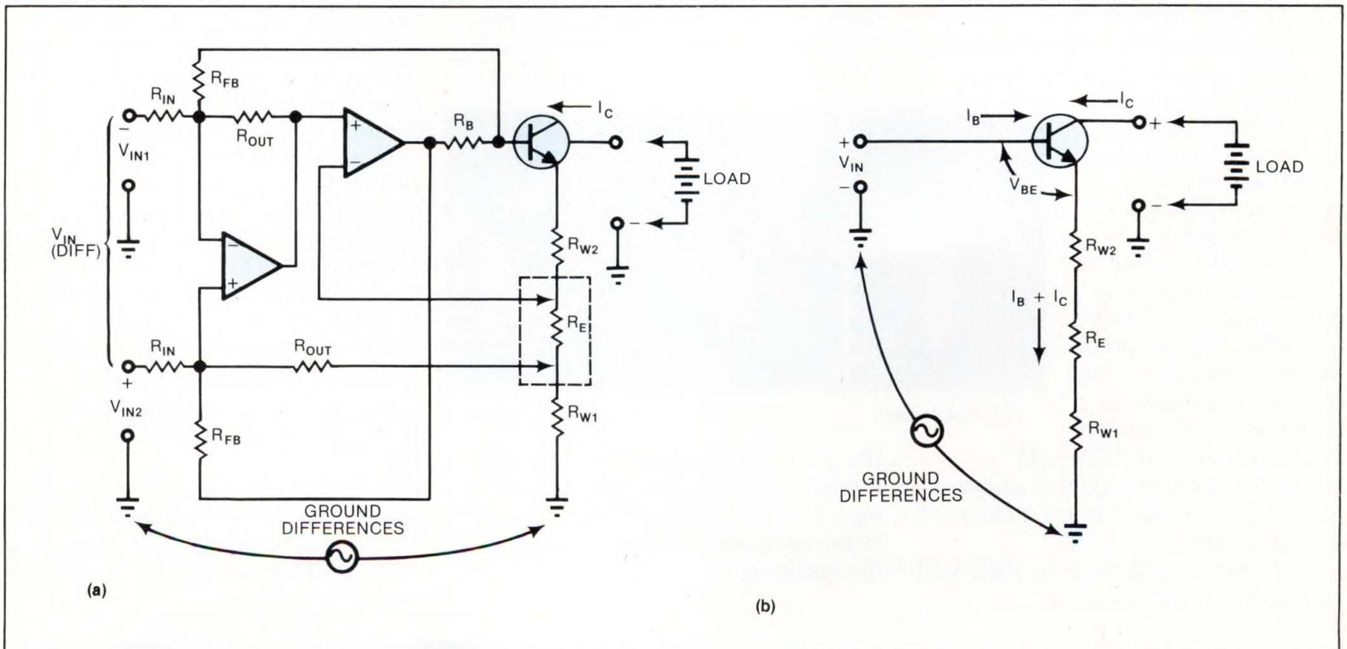
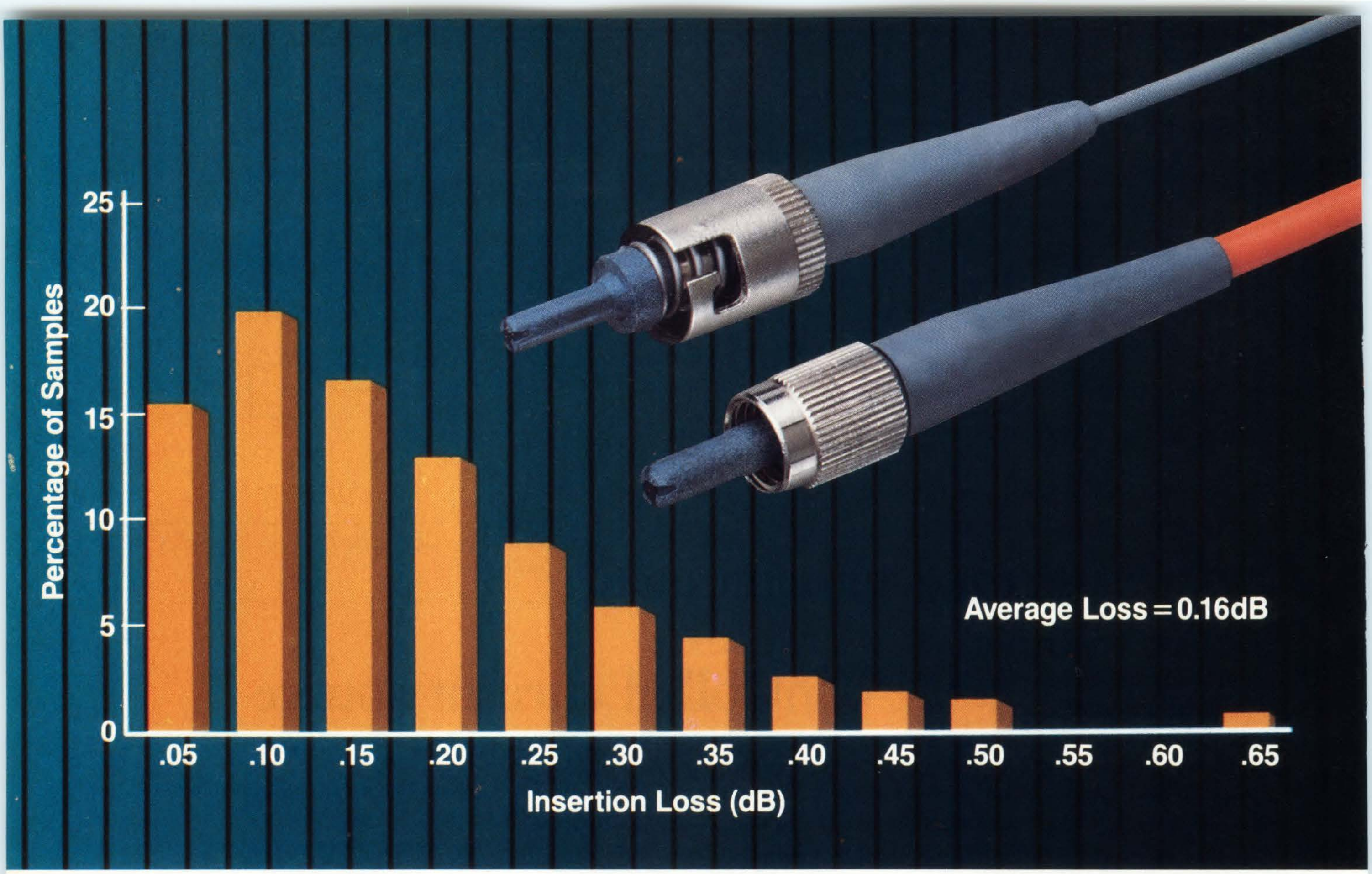


Fig 1—A circuit (a) incorporating several modifications *to a basic emitter-follower current source* ***(b)*** *eliminates errors caused by wiring resistance, common-mode signals, and the transistor's finite base current. However, the modifications introduce offset-current and equivalent input-noise errors and give the circuit a low input impedance.*



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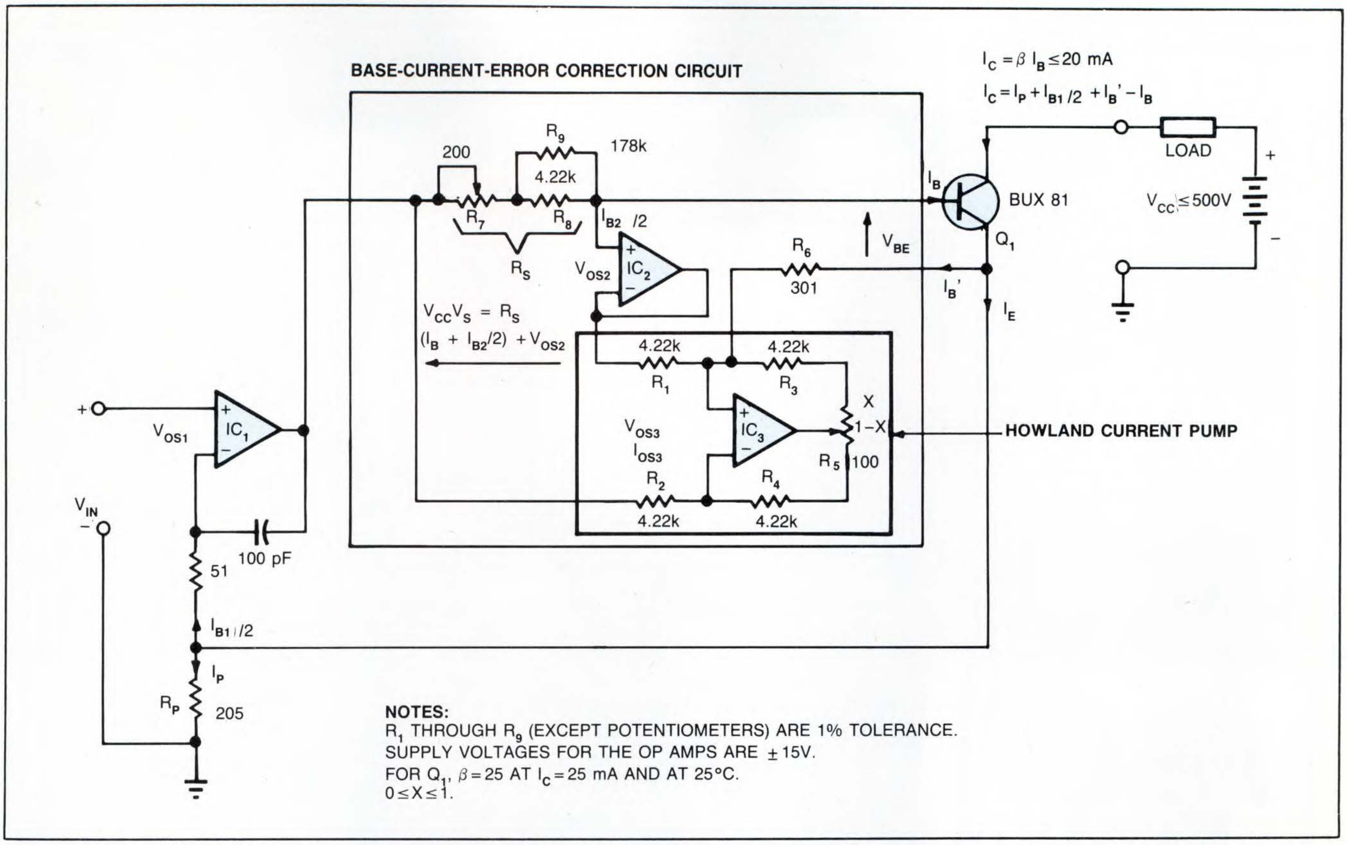

***Fig 2—This improved voltage-controlled current source** almost completely cancels base-current-induced error, has high input and output impedances, and features excellent compliance and a wide output range.*

circuit accuracy. You can reduce this last error contribution by inserting a voltage follower between the transistor's base and feedback resistor R_{FB}.

Fig 2's voltage-controlled-current source uses a technique that almost completely cancels the error caused by the transistor's finite base current. The technique neither affects the circuit's input characteristics nor increases the error contributions from other sources. The circuit consists of the standard op-amp-plus-transistor current source (Q_1 and IC_1) plus the insertion of a base-current error-correction circuit (IC_2 and IC_3). The circuit's output current is given by the expression

$$I_C = \frac{V_{IN}}{R_p}.$$

The circuit corrects the base-current error as follows. Q_1's base current, I_B, causes a voltage drop across R_S. This drop (I_BR_S), through noninverting-buffer IC_2, drives a Howland current pump consisting of IC_3 and resistors R_1 through R_6 (see "Improve circuit performance with a 1-op-amp current pump," EDN, January 20, 1983, pg 85). The Howland current pump's output,

$$I_B \approx I_{B'},$$

is then summed with the transistor's emitter current to cancel the emitter current's base-current component and thus leaves only the collector-current contribution. This process makes the voltage drop across R_P and the feedback to IC_1 independent of base current. Thus, the circuit eliminates the base-current contribution error.

The expression for I_B' is

$$I_B = \frac{R_S}{R_1} I_B + \frac{V}{R_S + XR_5} \left\{ \frac{R_4 + (1-X) R_5}{R_2} - \frac{R_3 + XR_5}{R_1} \right\} \pm \epsilon \pm \gamma I_B, \quad (1)$$

where $$V \approx \frac{R_6 R_5 I_B}{R_1} - V_{BE},$$

$$\epsilon \le \frac{R_S}{R_1} \cdot \frac{I_{B2}}{2} + I_{OS3} + \frac{1}{R_1}(V_{OS2} + V_{OS3}),$$

$$\gamma \le \frac{R_6}{R_1}\left(\frac{1}{A_0} + \frac{1}{CMRR}\right),$$

and

I_B = input bias current,
I_{OS} = input offset current,
V_{OS} = input offset voltage,
A_0 = op amp open-loop gain,
CMRR = common-mode rejection ratio.

Because the circuit incorporates precision op amps, ϵ and γ have very low values; for example, $\epsilon \le 50$ nA and $\gamma \le 10^{-6}$.

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For the circuit to operate properly, you must use low-temperature-coefficient resistors. Also, you have to adjust R_5 and R_7 to meet the following conditions:

$$R_S = R_1 \tag{2}$$

and

$$\frac{R_4 + (1 - X)R_5}{R_2} = \frac{R_3 + XR_5}{R_1}. \tag{3}$$

When these conditions are satisfied, **Eq 1** reduces to

$$I_{B'} = I_B \pm \epsilon \pm \gamma I_B$$

and the circuit's output current is

$$I_C = I_P + \frac{I_{B1}}{2} + I_{B'} - I_B = I_P + \frac{I_{B1}}{2} \pm \epsilon \pm \gamma I_B. \tag{4}$$

Bearing in mind that

$$I_B = \frac{I_C}{\beta},$$

where β is Q_1's current gain, and that

$$I_P = \frac{(V_{IN} \pm V_{OS1})}{R_P},$$

then you can express d, the maximum deviation of the circuit's output current I_C from the ideal value

$$I_P = \frac{V_{IN}}{R_P},$$

using the expression

$$d = I_C - \frac{V_{IN}}{R_P} = \pm \left\{ \frac{\gamma}{\beta}\frac{V_{IN}}{R_P} + \frac{V_{OS1}}{R_P} + \frac{I_{B1}}{2} + \epsilon \right\} \tag{5}$$
$$= \pm 5 \times 10^{-8}\frac{V_{IN}}{R_P} \pm 90 \text{ nA}.$$

Note that this expression holds only when the conditions of **Eqs 2** and **3** are met. The prototype of this circuit has shown an accuracy better that 0.002% of full output (20 mA), with a ±20 mA residual error. **EDN**

IC replaces mechanical-interlock switches

Charles E Murphy
Elcotel Inc, Sarasota, FL

As an alternative to mechanical-interlock switches or membrane switches with latches, **Fig 1**'s circuit debounces, latches, and displays status information for a group of eight pushbutton switches in which only one switch at a time is active. The circuit's only IC is an octal latch.

Closing any one of the switches turns on transistor Q_1 and discharges capacitor C_2. Current through Q_1 then charges C_1, causing a positive transition at IC_1's CLK input (pin 11), which turns on the LED for that switch. The LED remains on until you depress another switch. Because the CLK input is edge-triggered and remains high until you release all the switches, two or more switch closures cannot register at one time unless they occur within approximately one millisecond.

Capacitor C_1 provides a delay that debounces each switch closure. Capacitor C_2 causes Q_1 to turn on briefly at power-up, which produces a pulse at IC_2's CLK input, ensuring all LEDs are off by latching all ones at the Q outputs of IC_1. **EDN**

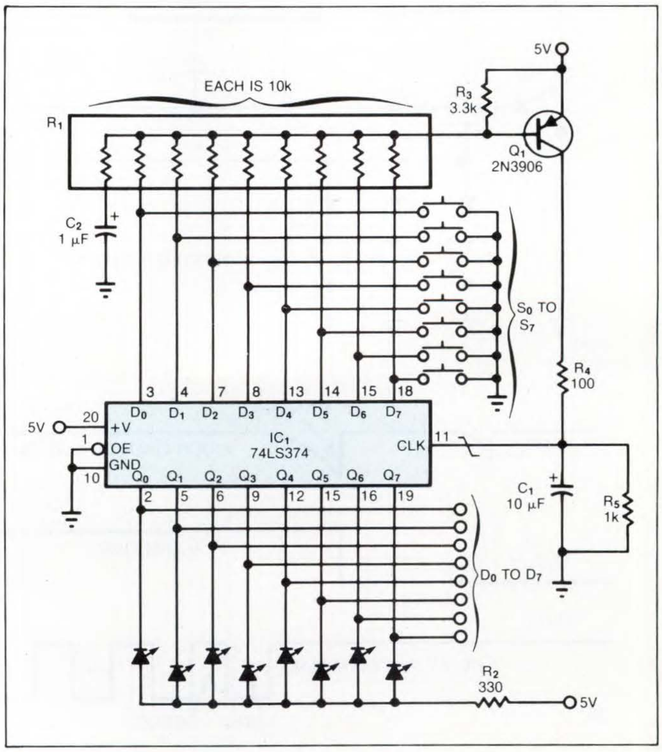

Fig 1—This single-IC circuit debounces a group of eight pushbutton switches, latches the last switch closure, and provides an LED indicator for the currently active circuit.

Burglar-alarm circuit uses one chip

Jacek Bartys
Alpha, Marco Electronics Div, Kraków, Poland

The single-chip burglar-alarm circuit shown in **Fig 1** uses a dual 556 timer, draws 10 mA of standby current, and generates a pulsing alarm signal that conserves battery energy. Once activated, the alarm will remain on, independent of the subsequent state of any of the sensors. The sensors support both deferred and immediate-action modes. You can attach this circuit to your car's internal lighting circuitry using a single wire and a relay.

To arm this circuit, you open your car door and close switch S_A. The switch discharges capacitor C_4 and holds

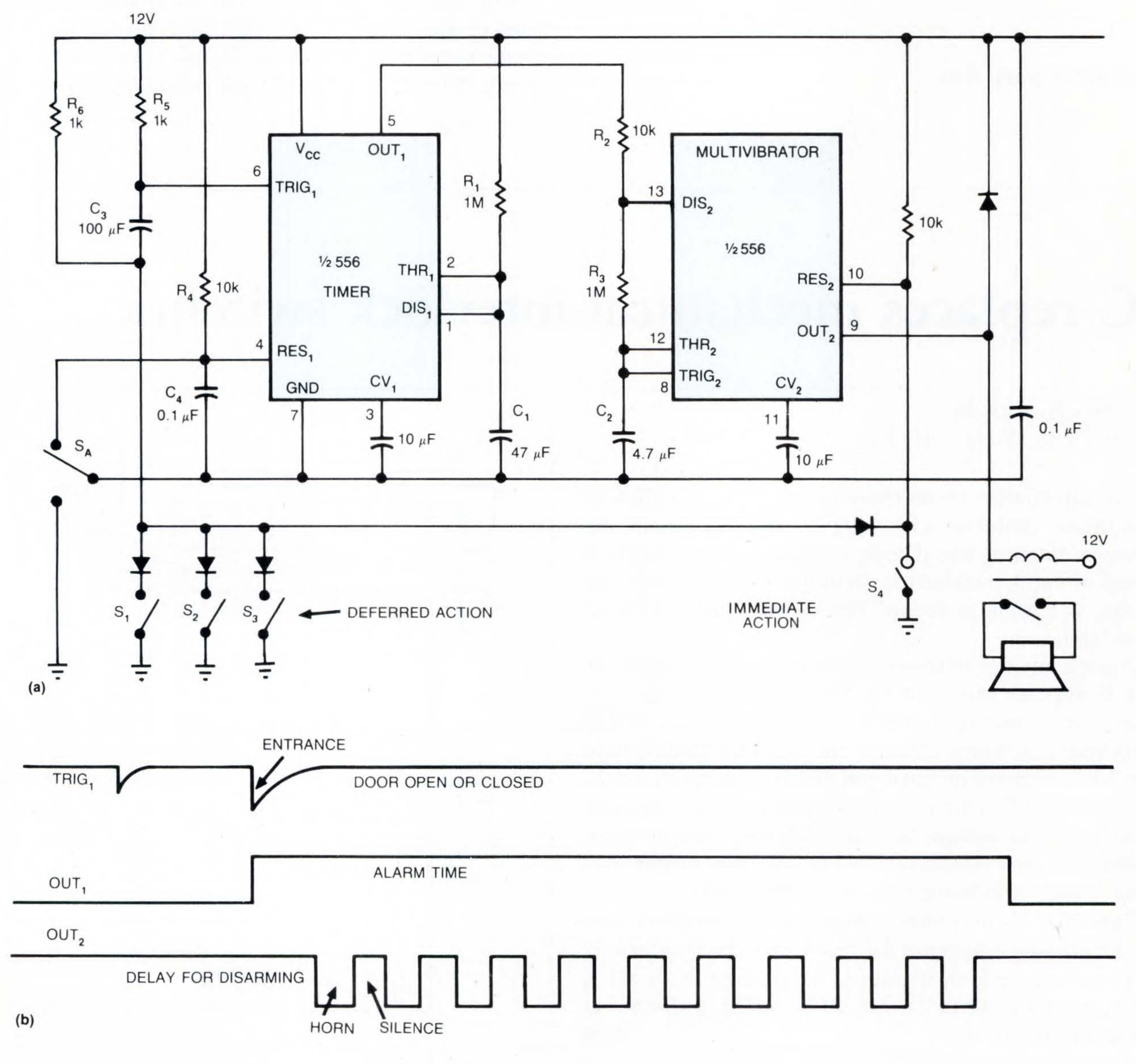

***Fig 1—This burglar-alarm circuit (a)** draws 10 mA of standby current and generates a pulsing alarm signal that conserves battery energy. You can connect this circuit to the lighting circuit inside your car using a single wire and a relay. The timing diagram **(b)** demonstrates that, while the timer's output is high, output 2 will cycle, turning the horn on and off.*

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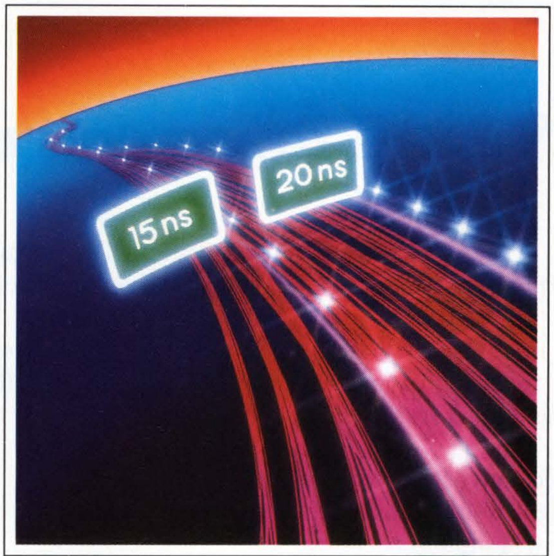

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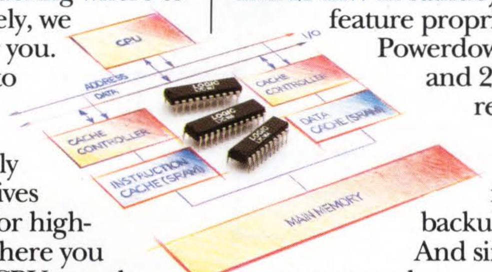

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the timer (one half of the 566 IC) in a reset state to prevent false triggering while you're arming the circuit. When you close your car door, the circuit enters a standby mode.

If the door is then reopened, the sensors apply a negative-going pulse to trigger 1. Output 1 then goes high and stays high, enabling the alarm for $1.1R_1C_1$ sec. Output 1's high state triggers the multivibrator (the other half of the 566), which begins to cycle after a delay equal to $1.1(R_2+R_3)C_2$ sec. As long as the timer's output stays high, the multivibrator will continue to cycle, turning the horn off and on at 3.3-sec intervals.

During the interval between the time that the timer's output goes high and the time that the multivibrator's output goes low, you can disarm this circuit using switch S_A. To prevent false triggering caused by switch contacts (switches 1, 2, and 3) that may bounce when you're closing the door, you should make the R_6C_3 time constant as large as possible. In addition, capacitors C_1 and C_2 should be tantalum types and should exhibit leakage of less than 1 μA at room temperature. **EDN**

Low-power RS-232C driver operates from 5V

Mark Walczak
Microcontrol Pty Ltd, Monterey, Australia

The circuit in **Fig 1** draws only 4 mA from a 5V supply while driving a standard RS-232C receiver. In contrast, a 1488 quad-driver IC draws 10 to 20 mA from each of its two supplies.

The system clock drives a dc/dc converter that produces −3.4V. Frequency can range from 0.5 to 8 MHz, but a range of 0.5 to 1 MHz will minimize power dissipation. The circuit output withstands direct shorts to ground or to either of the supplies (±12V max). In place of the 74HC04 high-speed CMOS driver shown, you may want to substitute miscellaneous spare gates; one noninverting buffer, for example, can replace the two inverting types that receive the UART signal. **EDN**

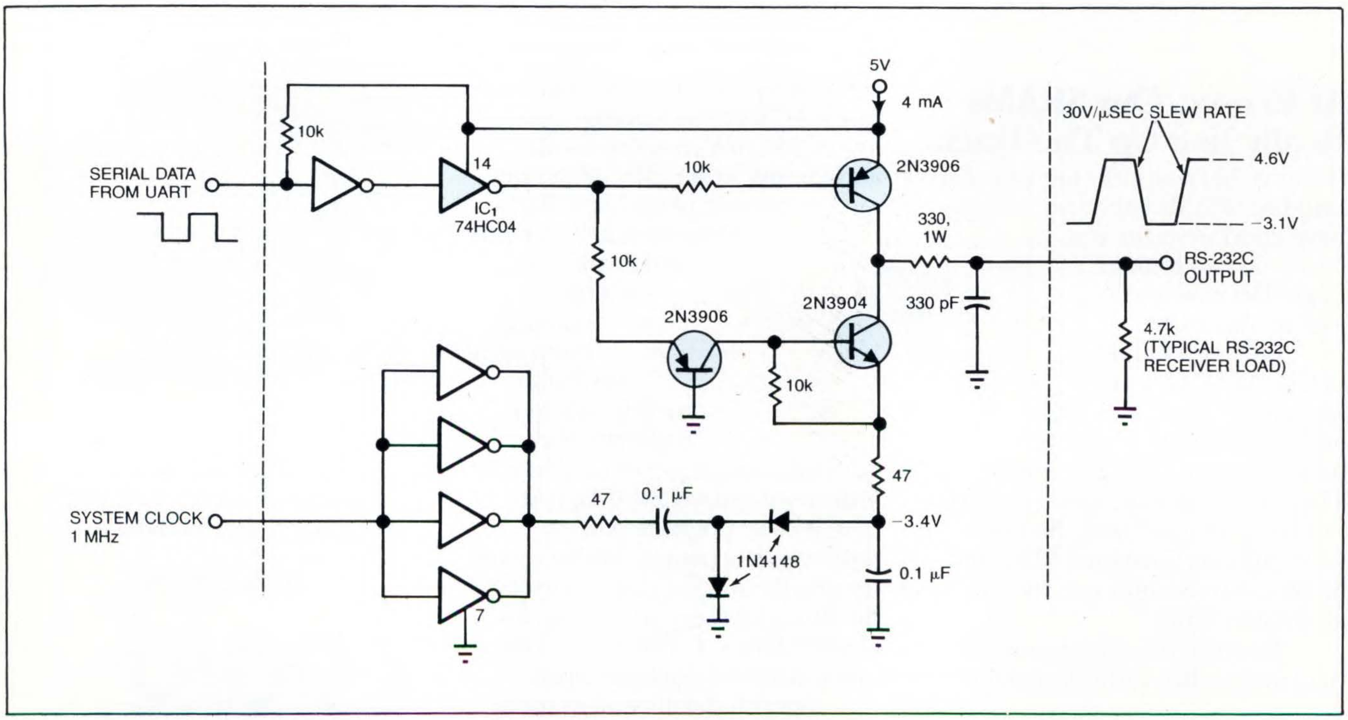

***Fig 1—You can build an RS-232C driver** using a CMOS IC and three transistors. Power consumption is 20 mW.*

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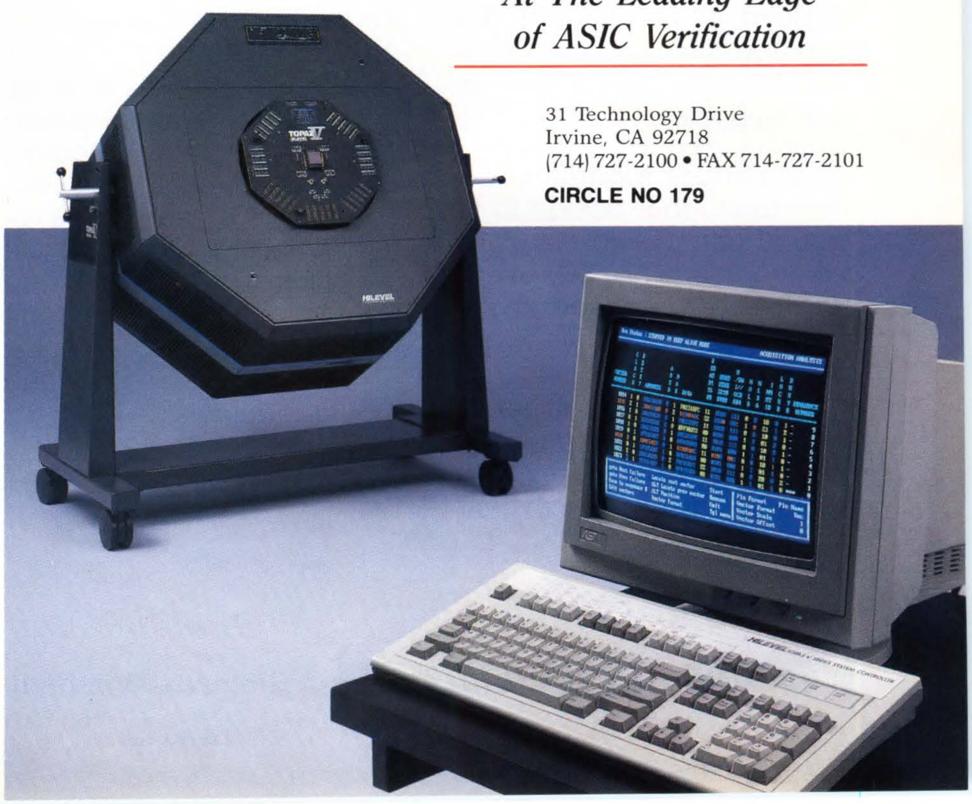

CIRCLE NO 180

Amp provides 100V common-mode range

Mark Stitt
Burr-Brown Corp, Tucson, AZ

The unity-gain amplifier of **Fig 1** can reject common-mode voltages as high as 100V. For an application that does not require galvanic isolation, this circuit is an inexpensive alternative to the conventional isolation-amplifier solution.

IC_1 is a monolithic gain-of-10 difference amplifier. By reversing normal connections to the on-chip resistor network, you place 100-kΩ resistors (instead of the 10-kΩ ones) at the amplifier's input, which attenuates the normal- and common-mode signals by a factor of 10. Then, resistors R_1, R_5, and R_6 form a T network in the feedback path that boosts the normal-mode gain to unity.

Because the addition of R_5 and R_6 degrades common-mode rejection by unbalancing the internal resistor ratios, you should restore the balance by adding about 158Ω (R_7) in series with R_3. A fixed-value R_7 that differs by 2% from the T network's equivalent value degrades CMR by only a few dB, but note that IC_1's CMR is already 20 dB below its specified value (100 dB min) because the amplifier is operating at a gain of 0.1 instead of 10. You can improve the CMR by using a 500Ω potentiometer for R_7, as shown.

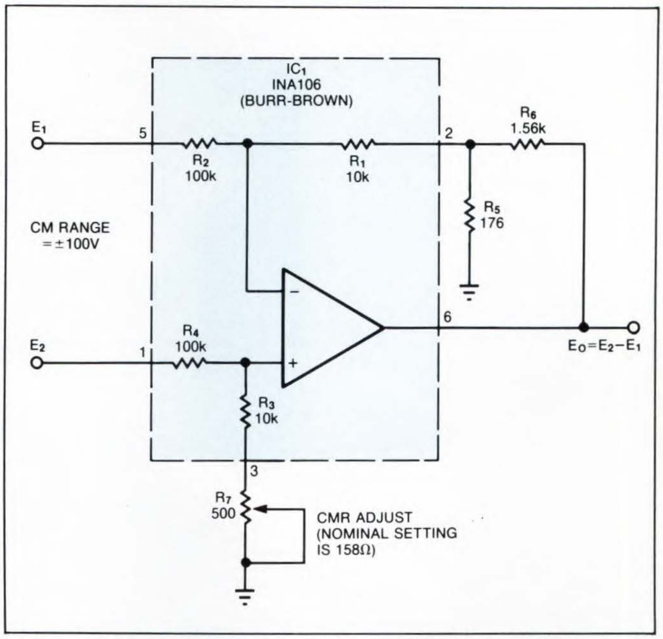

***Fig 1—This amplifier offers unity gain** to E_2-E_1 signals while rejecting common-mode voltages as high as ±100V.*

The differential-gain accuracy is within 2% if you use 1% resistors for R_5 and R_6. Adjusting the R_6/R_5 ratio can improve the gain accuracy, but calibration is difficult because the gain and CMR adjustments interact. You can eliminate this interaction and improve the gain accuracy by using the **Fig 2** circuit.

In **Fig 2**, IC_2 preserves IC_1's CMR by buffering the R_5/R_6 network. Again, IC_1's gain-of-0.1 connection reduces the guaranteed CMR by 20 dB—to 80 dB min. (This CMR estimate is reliable because the IC_1 amplifi-

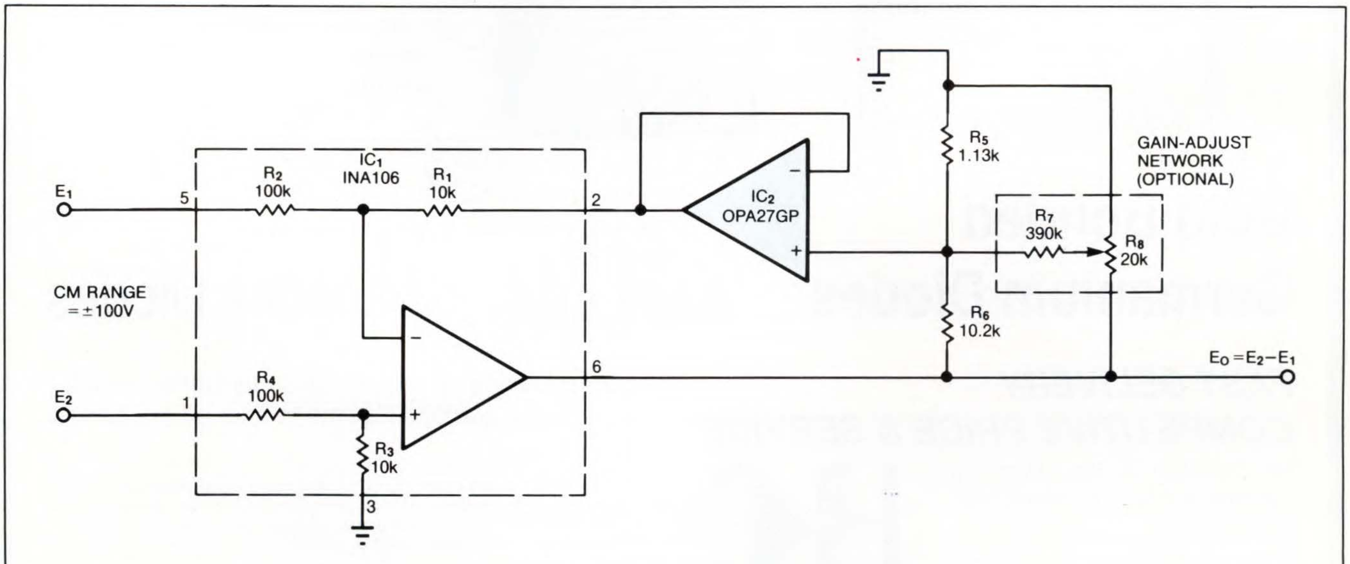

***Fig 2—Adding an op amp to the Fig 1 circuit** eliminates interaction between the gain-adjust potentiometer and the CMR-adjustment pot (not shown).*

er (distinct from its thin-film resistor network) contributes only −120 dB of CMR error. Therefore, the resistor network is responsible for most of the residual CMR error that remains after laser trimming. This trim error affects CMR by about the same amount whether operating with a gain of 10 or a gain of 0.1.)

You can improve this circuit's CMR by adding 10Ω in series with R_1 (pin 2) and adding a 20Ω potentiometer in series with R_3 (pin 3). To adjust CMR, connect the inputs and drive them with a 1-kHz square wave whose amplitude is in the range from ±10V to ±100V. (A sine wave will introduce unwelcome CMR-vs-frequency effects.) Adjust the 20Ω pot for a minimum-amplitude signal at E_O.

As before, $1+R_6/R_5$ sets the gain. The tolerance on this expression plus ±0.01% (contributed by IC_1) determines the overall gain accuracy. You can improve gain accuracy by using higher-precision resistors or by adding the optional gain-adjust network shown (R_7 and R_8). Gain and CMR adjustments don't interact in the **Fig 2** circuit.

One application for the circuit of **Fig 1** or **Fig 2** is in monitoring high-side load current in a regulator or power supply. By connecting the difference amplifier across a 1Ω resistor in series with the supply's output, you can interpret the difference amplifier's output as one ampere of load current per volt for supply voltages in the range from −100V to 100V. **EDN**

Op amp provides a current and voltage source

Scott Wayne
Analog Devices Inc, Norwood, MA

You can obtain a controlled source of voltage ($-V_R$) and current ($V_R/2R$) by using a single op amp and four transistors **(Fig 1)**. The current and voltage outputs track the reference voltage. Moreover, they show little variation with temperature because the circuit compensates for changes in the transistors' beta and base-emitter voltage. For best results, you should use a single-chip array for the transistors and another one for the R-value resistors.

Transistors Q_1 and Q_4 form a current mirror that generates I_O by replicating Q_1's collector current. To calculate V_O, note that the currents through R_1 and R_2 are equal, so the voltage across R_2 is $V_R/2$. Similarly, the voltages across R_3 and R_4 are equal, because currents through these resistors are the same. Further, the voltage across R_4 is $V_R/2$ minus one base-emitter voltage (V_{BE}), so Q_1's base-collector voltage is also $V_R/2-V_{BE}$. Therefore, Q_1's collector-emitter voltage is $V_R/2$, and $V_O=-V_R$.

Without compensation, each transistor's V_{BE} would change about −2.2 mV/°C, making V_O vary with temperature. Q_2 and Q_3 prevent this variation by creating a temperature-dependent current in R_3 that moves the base voltage of Q_1 and Q_4 in a direction opposite to the change in V_{BE}.

You should choose the value of R_3 and R_4 so that the collector current of Q_2 and Q_3 will equal the collector current of Q_1 and Q_4. The matched currents and the circuit's symmetry ensure that all betas and collector currents will remain equal as temperature varies, provided that the transistors are well matched. Capacitor C_1 reduces output noise by limiting the circuit's bandwidth. **EDN**

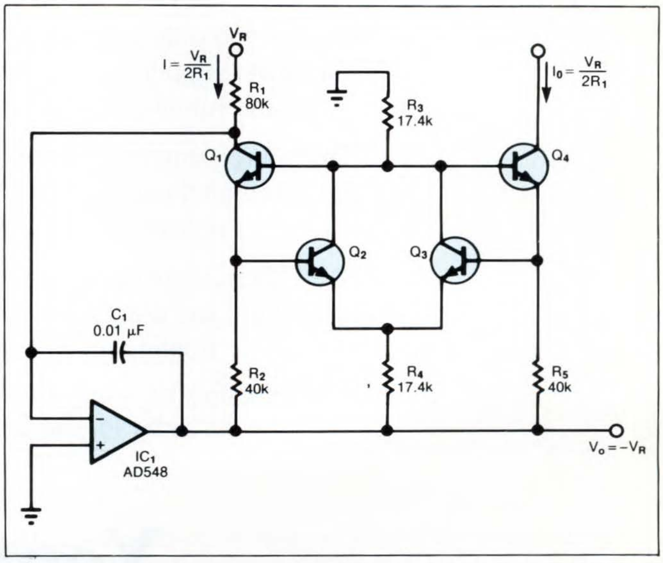

Fig 1—This single-op-amp circuit generates *temperature-stable current- and voltage-source outputs that track the reference voltage (V_R).*

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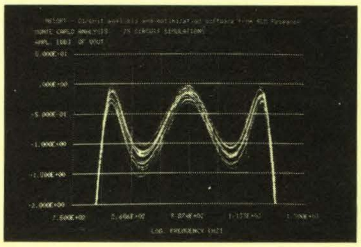

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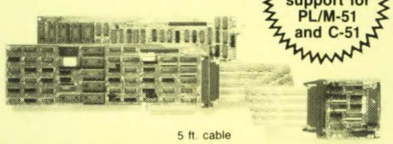

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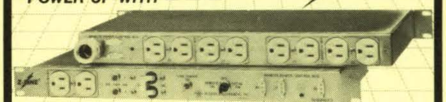

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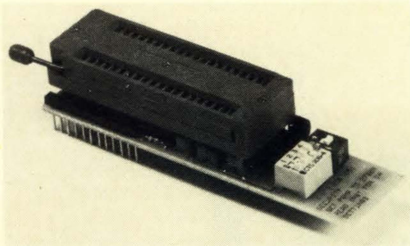

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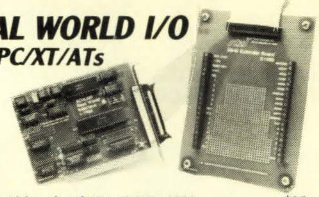

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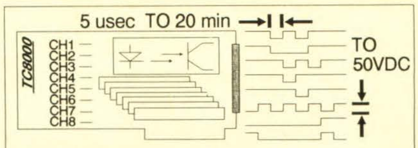

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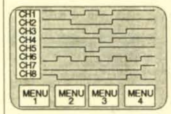

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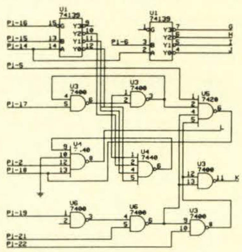

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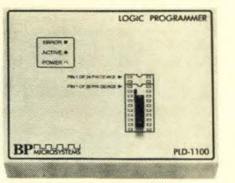

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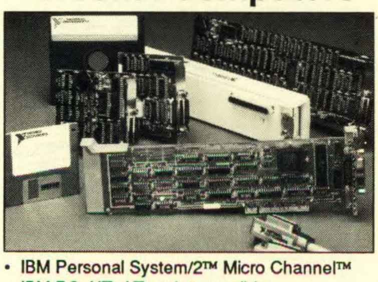

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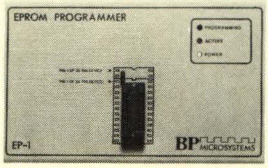

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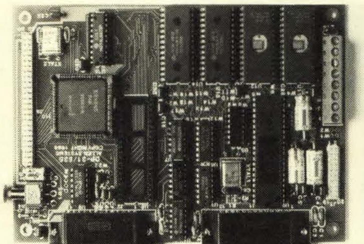

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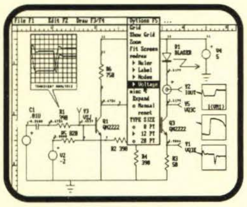

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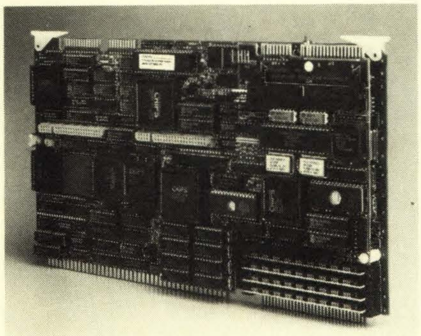

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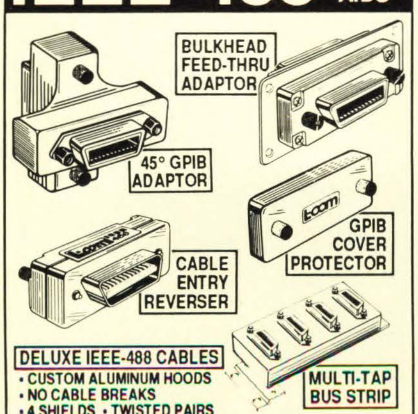

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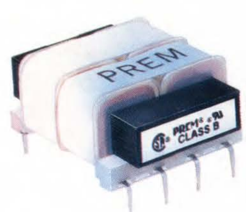

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