® 16 JAN 1989 Troubleshooting analog circuits—Part 1

Glossary of DSO terms

RISC compilers

SCSI development systems

VXI Bus specifications

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



of improvements

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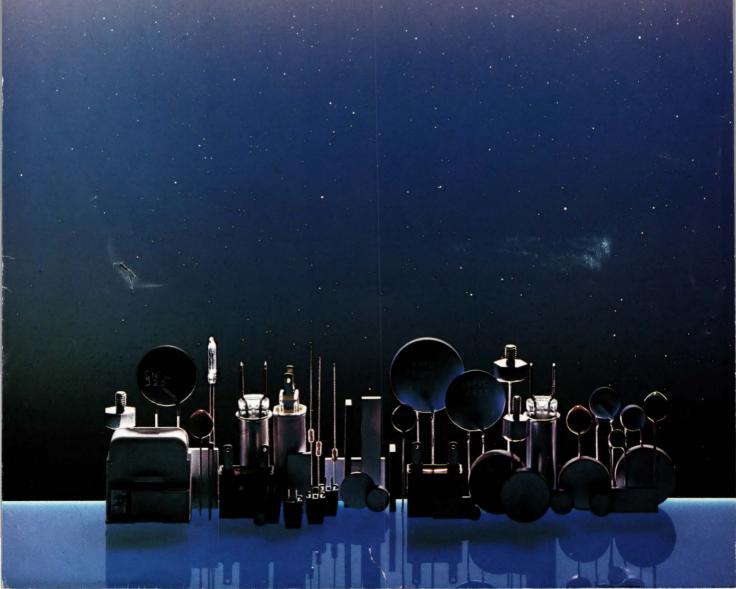
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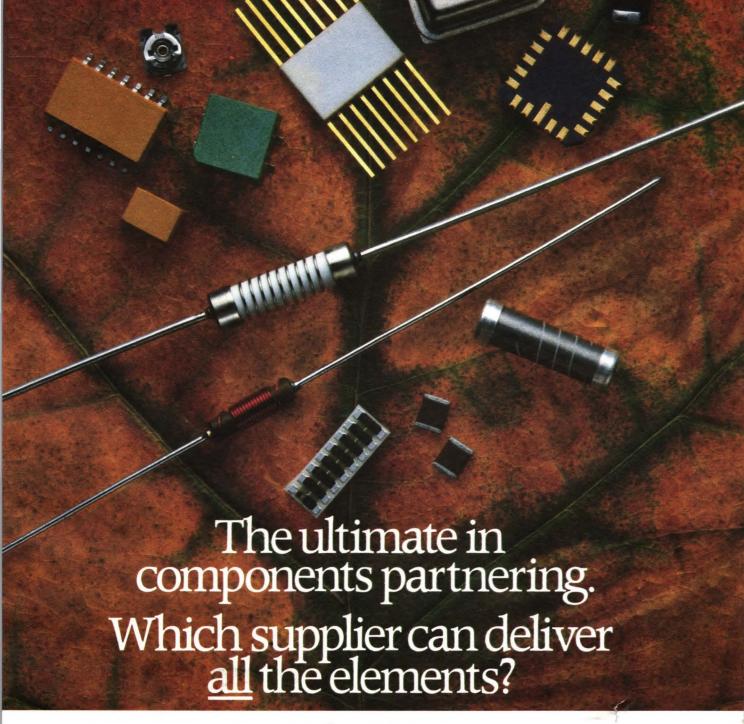
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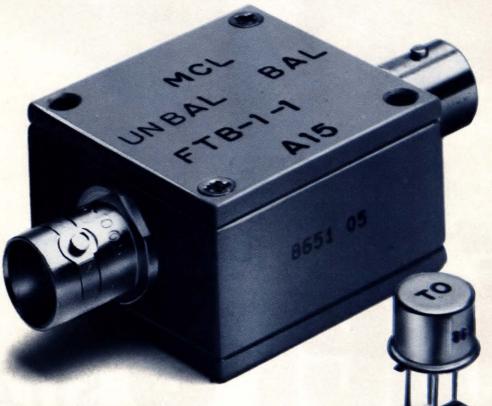
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January 5, 1989

#### ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: Denser geometries, processing innovations, and packaging improvements are resulting in power MOSFETs and IGBTs (insulated-gate bipolar transistors) that have everhigher voltage ratings and current-handling capabilities, as well as volumetric power-handling efficiency. See pg 128. (Photo courtesy International Rectifier)

#### SPECIAL REPORT

#### Power MOSFETs & IGBTs

128

The increasing diversity and steadily improving performance of available power MOSFETs and IGBTs are making them the switching devices of choice in many applications.—*Bill Travis*, Contributing Editor

#### **DESIGN FEATURES**

#### Troubleshooting analog circuits—Part 1 14

In this first installment of a multipart series, one the world's leading analog-circuit designers makes the case that a significant part of effective troubleshooting lies in the way that you think about the problem.—Robert A Pease, National Semiconductor

#### Current-feedback amplifiers benefit high-speed designs

161

Current-feedback amplifiers offer significant advantages over conventional high-speed op amps. Like the conventional devices, however, they exhibit nonideal behavior, so some circuit configurations require special care. Understanding the circuit topology will help you achieve successful designs.—Sergio Franco, San Francisco State University

#### Glossary takes the mystery out of DSO terminology

175

Specification sheets for digital storage oscilloscopes (DSOs) contain many specialized terms, which can be confusing to the uninitiated. This glossary should solve the terminology problem.

—Bruce W Blair and Gene Andrews, Tektronix Inc

#### PSpice review reveals strengths, drawbacks of optional packages

193

PC versions of Spice are available from several vendors, and more often than not they provide facilities not present in the original. One such version is MicroSim's PSpice.—Jonathan B Scott, University of Sydney

Continued on page 7

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The VXI Bus specification will boost instrumentation performance; system-level software specs, however, remain unaddressed (pg 61).

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#### TECHNOLOGY UPDATE

#### VXI Bus specifications: Manufacturers tackle 61 cloudy software issues

The new VXI Bus specifications provide the instrumentation industry with the hardware compatibility that eluded its precursor, the VME Bus. But the proposed guidelines intentionally ignore issues concerning the VXI's sophisticated software options.

—J D Mosley, Regional Editor

#### RISCs force move to compilers

73

Reduced-instruction-set computers (RISCs) promise to speed up computer systems. That's the good news. The bad news is that 70% of EDN's readers do the bulk of their embedded-system programming in assembly language.—Charles H Small, Associate Editor

#### SCSI development systems: Tools allow debugging of software, firmware

Compared to a relatively simple hardware design, implementing the Small Computer Systems Interface (SCSI) in a host computer or a peripheral controller entails a sizable firmware- and softwaredevelopment task. Luckily, several companies offer test and development tools.—Maury Wright, Regional Editor

#### PRODUCT UPDATE

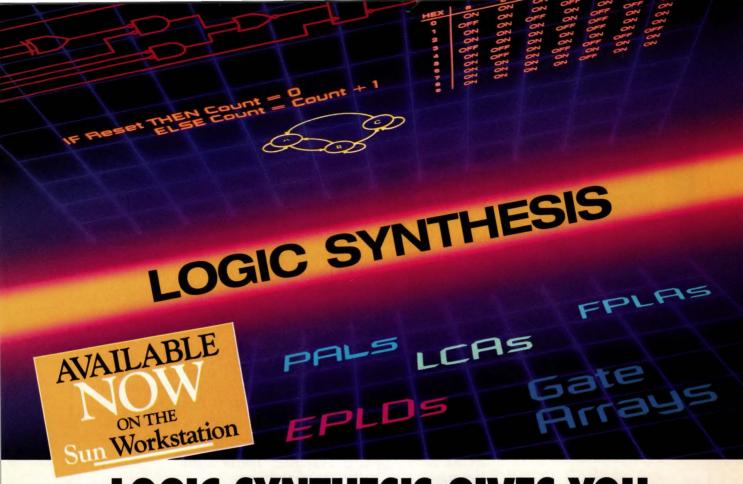
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## LEOK...SO THE TRANBUT R

They're everywhere. Worldwide over a thousand Transputer designs are in today's marketplace or are entering production. Some belong to Fortune 500 companies committed to using Transputers to build their next-generation products.

Although Transputer applications are diverse, the theme for each is the same – combining the power of individual Transputers with the unique architectural benefits of parallelism to achieve results that cannot be obtained as economically any other way.

#### Data Compression Transputers are

being used in the

Generic Checkout

System at the NASA
Kennedy Space
Center.

They are embedded within VME based front-end Data Acquisition Modules to provide data filtering for the system.

These modules pre-process data for a network of Unix based workstations that provide real-time control and monitoring of ground and flight equipment, like that used by the Space Shuttle. Only Transputers offered the degree of parallelism needed for this application.



#### **Medical Imaging**

University College London is using the parallel processing power of Transputers to convert CAT, NMR and laser scans into rotating 3-D images. These facial, skeletal, and soft-tissue images provide accurate computerized measurements to assist doctors with each step of an operation, and are also used by plastic surgeons to 'rehearse' operations for reconstruction.

#### **Data Collection**

British Steel is implementing an intelligent system that is designed to dramatically cut its multimillion dollar annual energy costs. It is built around T800 floating point microprocessors which process information from a highly complex data gathering system. These Transputers operate in parallel, condensing enormous amounts of data into information which helps energy management decide how to respond to a plant's changing demands for different fuels.



#### **Data Transmission**

Kokusai Denshin
Denwa (KDD), the
Japanese international
telecommunications
company, has developed an imageprocessing video
telephone using
Transputers to manipulate and condense
images for transmission
over telephone links.

This image communications system uses 32 Transputers operating in parallel

for ultrafast image processing. It can be connected to PC's to transmit images over telephone lines, function as a video phone, or be programmed to match the specifications of other receiving equipment, such as

facsimile machines and TV monitors.



#### Space

The European Space Agency is using Transputers to build a light-weight, radiation-tolerant, on-board computer for spacecraft. Programs which utilize Transputers in scientific computing and spacecraft control applications are also being developed in the U.S.

Transputers are manufactured on epitaxial silicon and have been shown to withstand aggressive tactical radiation levels.

## PUTER'S TERRIFIC, 17

#### light Simulation

British Aerospace have used ansputers to develop a low-cost ight simulator comprising a flat orld, groundrid, buildings, ees and mountains vith an optional Headp display. Future enhancements vill include the addition of undulating rrain and a single or triple window isplay option.

American companies are also using ransputers to build high-performance ight simulators more cheaply. One U.S. nanufacturer utilizes over one thousand 800 processors per system.

#### -D Rendering

Pixar in the US has developed a ransputer-based rendering system which uickly renders photorealistic images from D models. The system consists of ransputer boards for VME and AT-bus ystems optimized to run 🎩 ophisticated rendering software.



The system holds great promise for such applications as architecture, automobile styling, package design, simulation as well as animation. Pixar's recent computer generated film 'Tin Toy' could not have peen done without using this Fransputer-based accelerator.

#### System Control

As the number of Transputers in a system design are increased, a proportional increase in performance can be achieved.

In West Germany, Parsytec GmbH is using this principle in their Megaframe Superclusters. Superclusters represent a complete series of reconfigurable industrial control boards as used in the automotive industry, which exploit the Transputer's parallel processing capability.



The basic Model 64, built with T800's, has a performance of 640 MIPS and 96 MFLOPS. The Model 256 comprises four Model 64 cabinets connected by cables and provides 2,560 MIPS and 384 MFLOPS.

Parsytec believes there is no limit to the size Superclusters can grow to. Two Model 256s can be combined easily to realize twice the raw performance of one system.



#### Robotics

Transputers are ideally suited for robotics applications because their special on-chip links make communication between control centers naturally easy. They are often used in the central control area for dumb robots, in multi-jointed robots, and in machine vision systems.

At the Houston Space Center, NASA and Lockheed are using Transputers in the development of an intelligent, selfmanoeuvering, voice-controlled robot named EVA Retriever. EVAR is being built to investigate the autonomous retrieval of objects and astronauts that become detached from the Space Station.



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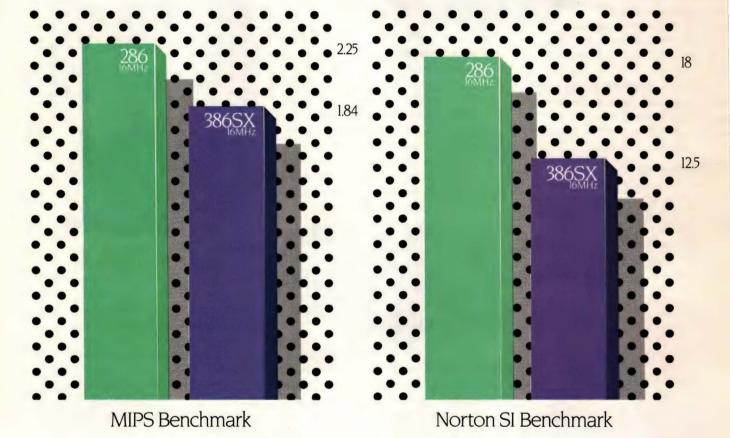
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# The 386SX: Good who want slower,



All benchmarks performed with an Everex Step 286-16 with 0 wait states and a Compaq Deskpro 3865™ with 0 wait states. Both systems running 16-bit DOS and OS/2 software.

Dhrystone 1.1 compiled with Microsoft® C compiler with no optimization. Run under DOS 3.31. Norton SI by Peter Norton Computing, Inc. performance reported relative to an IBM PC-XT.®

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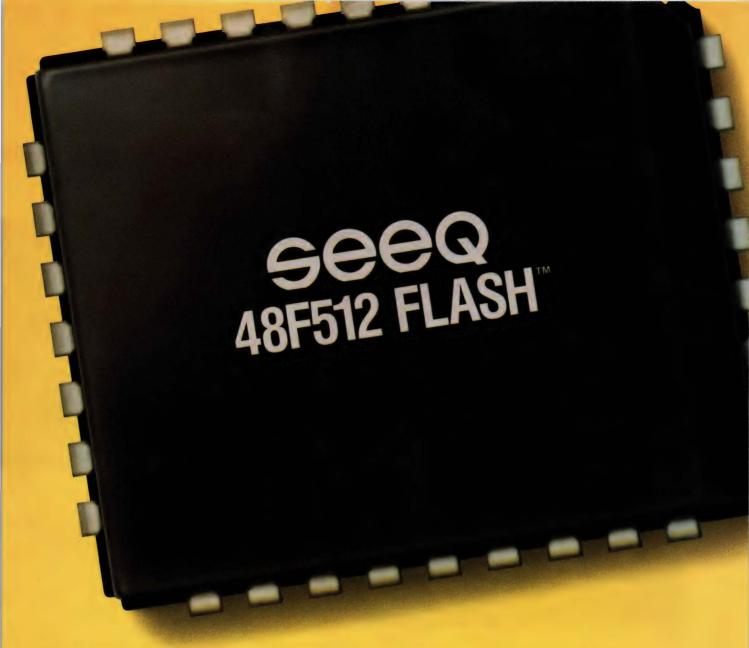
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The electrical erasure of an EEPROM.



ceramic DIPs. The DIP packages are in a 32-pin JEDEC format so you can easily upgrade in density from 512K through 2Mbit with no hardware changes.

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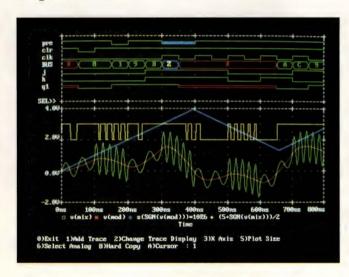
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15

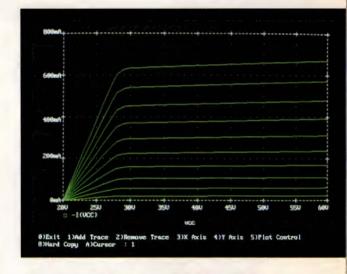
## **PSpice**

Since its introduction five years ago, MicroSim's PSpice has sold more copies than all other Spice programs combined. Now PSpice 4.0 is available with the most significant new capabilities since the creation of PSpice in 1984.



#### Mixed Analog/Digital Simulation

With the Digital Simulation option, PSpice can simulate mixed analog and digital circuits. The option contains a 28-state, event-driven, logic simulation engine to efficiently process digital events. It is easy to use: analog and digital devices are included in the same netlist file, in the usual SPICE syntax, and may be freely interconnected. Probe, the graphics post-processor for PSpice, can display both analog and digital waveforms on the screen at the same time with a common time axis. PSpice includes a library of over 660 digital components.



#### **Analog Behavioral Modeling**

The Analog Behavioral Modeling option allows the user to describe a circuit block by giving the block's transfer function, either by formula or by table. Nonlinear transfer functions make it easy to model unique devices, such as Josephson junctions. Linear transfer functions are also available that describ the device in the frequency domain, either by a Laplace transform or by a frequency response table. Analog Behavioral Modeling helps top down design since a circuit block can be modeled by its transfer function at the beginning of a design and later replaced by the actual circuitry.

#### **Extensive Device Libraries**

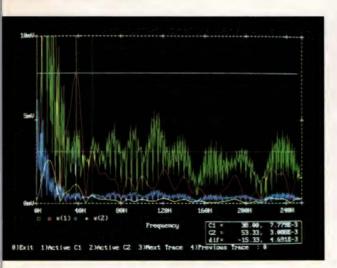
Included with each copy of PSpice 4.0 i an extensive library of over 2,200 analog components. The library files are not encrypted and may be modified by the

#### Extends the Bounds of Circuit Simulation

user. We also offer the Parts parameter extraction program to help you characterize additional devices.

#### **Interactive** Operation

On the PC, PSpice 4.0 allows interactive operation of the simulator. On-line help and pull-down menus assist one in using the simulator. An on-screen text editor which "knows" about the PSpice nput format makes it easy to create or nodify circuits, or use your favorite schematic editor.



#### **Enhancements and Options**

In addition to the devices included in standard Spice, PSpice 4.0 includes these: GaAs MESFET's; BSIM MOS model; non-linear transformers, modeling saturation, hysteresis; and deal switches for use with, for example, power supply and switched capacitor circuit designs. Extra options available: Monte Carlo analysis,

including Sensitivity and Worst Case; Digital Files interface to popular logic simulators; and Device Equations source code for semiconductor devices.

#### Choice of Platforms

PSpice is available on these computers: the PC family, including the PS/2, under both DOS and OS/2; the Macintosh II, the Sun 3 and 4 workstations; and the VAX/VMS family, including the MicroVAX.

#### **Technical Support**

Each copy of PSpice comes with our extensive product support. Our technical staff has over 50 years of experience in CAD/CAE and our software is supported by the engineers who wrote it. With PSpice, expert assistance is only a phone call away.

#### For More Information...

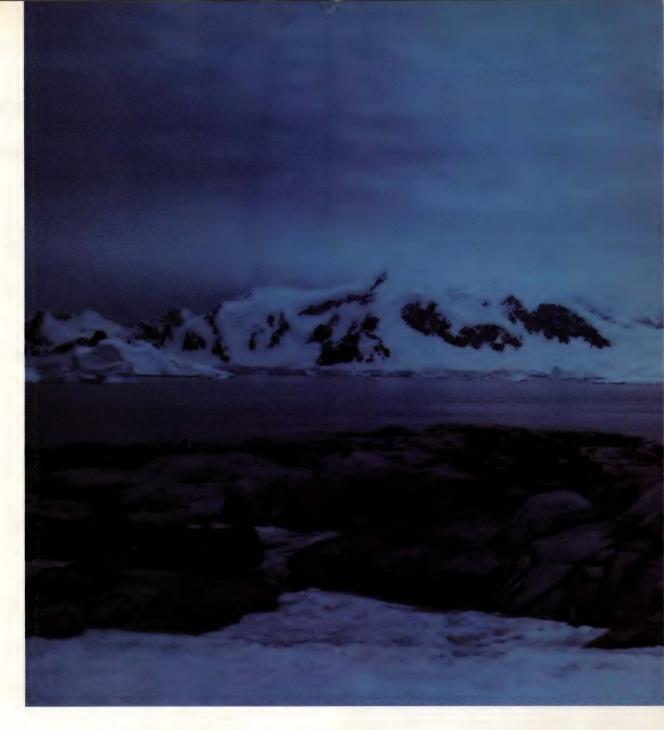
If you want more information about these advanced features and a free PSpice demo diskette, please call us today at (800) 826-8603 or, in California, (714) 770-3022. Find out for yourself why PSpice is the standard for circuit simulation.



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#### NEWS BREAKS

EDITED BY JOANNE CLAY

#### TOKEN-RING CONTROLLER CHIP ACHIEVES 16M-BPS TRANSFER RATES

The \$96 (1000) TMS380C16 Commprocessor from Texas Instruments Inc (Dallas, TX, (800) 232-3200, ext 700) functions in token-ring LANs that operate at data rates to 16M bps. This second-generation device performs the functions of three of the manufacturer's first-generation token-ring parts—the TMS38010 communications processor, the TMS38020/21 protocol handler, and the TMS38030 system interface—as well as the functions of two additional ASIC components: a PC bus-interface unit and a dynamic-RAM memory-expansion unit.

The company also integrated the functions of the two remaining ICs in its first-generation token-ring chip set—the TMS38051 and TMS38052 ring-interface chips—in the \$24 (1000) TMS38053. Thus, the manufacturer has reduced the core chip count for a token-ring interface chip set from seven to two devices and boosted the performance from 4M bps to 16M bps.—Steven H Leibson

#### CASE TOOLS SUPPORT EMBEDDED-µP SOFTWARE DEVELOPMENT

The HP 64000 AxCASE software-development tools support the entire development cycle for embedded-microprocessor system designs. Products provide support for analysis, design, software construction, software integration, hardware/software integration, release, and maintenance of software. Hewlett-Packard (contact local sales office) offers the products for more than 40 µPs, including the 68000 and 8086 families. The cross-development tools run on HP 9000 Series 300 and Series 800 computers under the HP UX operating system. Some specific tools included in the family are Advanced Cross C Compiler Systems, Debug Systems, and Basis Branch Analyzers. Prices for these products vary, depending on the number of users and the host computer. The cross-compilers cost \$2375 to \$6650, the debuggers cost \$2655 to \$3835, and the Basis Branch Analyzers cost \$1840 to \$5330.—Maury Wright

#### CACHE RAM OPERATES AT 20 MHz

If you want to simplify the cache memory design in your 80386-based system, consider using the V63C328 cache RAM from Vitelic (San Jose, CA, (408) 433-6000). The device is internally configurable as one  $8k \times 16$ -bit or two  $4k \times 16$ -bit memories, so you can create a 2-way set-associative cache without additional parts. You can also connect two devices in parallel for 32-bit operation. The device provides a direct interface to an Intel 82385 cache controller operating at 25 MHz; no additional logic is needed. Samples cost \$100; volume production is scheduled for the second quarter of 1989.—Richard A Quinnell

#### CACHE CONTROLLER OPERATES WITH 80286 OR 80386SX

To add cache memory to your 80286 or 80386SX systems, you can use the A28285 controller from Austek Microsystems (Mountain View, CA, (415) 960-1315). The A28285 offers 20- and 25-MHz speeds, a 32k- or 64k-byte cache size, and a 4-way set-associative architecture. It directly controls  $16k \times 4$ - or  $8k \times 8$ -bit static RAMs. Samples will be available during the first quarter of 1989 at a target volume price of less than \$45 (10,000).—Richard A Quinnell

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#### **NEWS BREAKS**

#### IC PRODUCES 5V DC DIRECTLY FROM AC MAINS

The HV-1205 monolithic ac/dc converter from Harris Semiconductor (Melbourne, FL, (407) 724-7800) accepts ac input voltages from 30 to 264V rms with a frequency range of 48 to 440 Hz. It produces 5 to 24V dc with a minimum of 50 mA at 5V dc. Line and load regulation are less than 5%. Manufactured in a high-voltage dielectric-isolation process, the device allows you to build small, 5 to 24V power supplies without transformers, rectifiers, or voltage regulators. It comes in an 8-pin plastic DIP. The 0 to 75°C version costs \$3.57 (100); the -40 to +85°C version is \$4.80 (100).—Richard A Quinnell

#### SCSI-BASED GRAPHICS CONTROLLER SUPPORTS STANDARDS

The ScuzzyGraph II intelligent graphics controller from Aura Systems Inc (Carlsbad, CA, (619) 438-7730) employs a SCSI (Small Computer Systems Interface) host connection. Furthermore, the resident 34010 graphics processor provides support for the GKS-CGI, Tek41XX, DGIS, and X-Windows graphics standards with no host intervention. A 68000  $\mu P$  acts as a traffic cop, and the 34010 controls an onboard frame buffer. The board supports a maximum resolution of  $1664\times1280$  pixels, and eight bits define the color of each pixel. The SCSI port offers transfer rates as high as 5M bytes/sec for incoming pixel data. Once the frame buffer is filled, however, the local processors perform manipulations on the frame buffer based on commands from the host CPU. A ScuzzyGraph II configured for a  $1024\times768\times4$ -pixel resolution costs \$1395 and is available 60 days ARO.—Maury Wright

#### 12-MIPS WORKSTATION IS BASED ON RISC CHIP SET

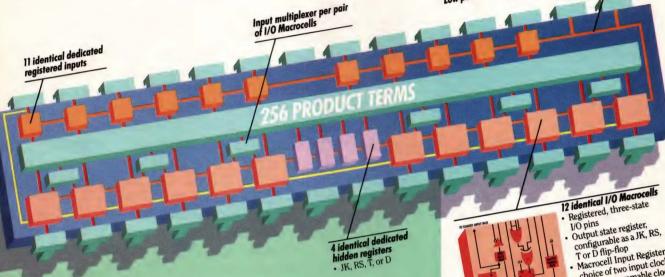
The Advantedge 2000 workstation from Integrated Solutions (San Jose, CA, (408) 943-1902) is based on the R2000 RISC chip set from Mips Computer Systems. The 12-MIPS workstation, targeted at OEMs, system integrators, and value-added resellers (VARs), costs \$12,000 for a basic system with no monitor. A system configured with a 100M-byte hard-disk drive, a 40M-byte cartridge tape drive, a 16-in. color monitor, a keyboard, and a mouse, costs \$20,375. The company will sell the product at various levels of integration, including the board level, and it will offer custom packaging.

Standard features include a 32k-byte cache, a  $1280 \times 1024$ -pixel graphics controller, onboard SCSI and Ethernet controllers, and an 80186-compatible I/O processor. You can choose from Mips Computer Systems' RISC/os or Integrated Solutions' Dual Universe Unix operating systems. The Dual Universe package includes both System V.3 Unix and Berkeley Unix 4.3BSD.—Maury Wright

## Why high performance designers are so excited about the new PLD 7C330 State Machine:

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#### NEWS BREAKS: INTERNATIONAL

#### 68030-BASED VME BUS BOARD SUITS SYSTEM MANAGEMENT

Incorporating a variety of interprocessor communications interfaces, the CC-112 68030-based VME Bus CPU card from Compcontrol by (Eindhoven, The Netherlands, FAX 040-120296; in the US, Los Gatos, CA, (408) 356-3817) is suited to system management in multiprocessor VME Bus systems. In addition to its message-passing capability over the VME Bus, the board can also communicate with other system CPUs via the VMS bus (VME serial bus). Onboard RS-232C and SCSI bus interfaces not only allow you to connect to terminal and mass-storage devices, but also provide low-and high-speed data links, respectively, between the CPU and other computer systems. The board's 20-MHz 68030 µP is accompanied by a 68882 math coprocessor, 4M bytes of 32-bit-wide dual-ported dynamic RAM, 2k bytes of battery-backed 8-bit-wide static RAM, and space for as much as 2M bytes of 16-bit-wide EPROM. The board also includes a watchdog timer, a real-time clock/calendar, and optional VME Bus system controller functions. The board costs \$3000 (100).—Peter Harold

#### IBM PC/AT-COMPATIBLE VME BUS MODULE SUPPORTS OS/2 AND XENIX

Offering full IBM PC/AT compatibility, the PX4010 VME Bus module from Philips's Industrial and Electro-acoustic Systems Div (Eindhoven, The Netherlands, TLX 35000; in the US, Mahwah, NJ, (201) 529-3800) allows VME Bus systems to run operating systems and application programs that are written for the IBM PC/AT. The module's 10-MHz 80286  $\mu$ P and 1.64M bytes of onboard RAM can support the OS/2 and Xenix operating systems in addition to MS-DOS. The module also includes a CGA-, EGA-, and Hercules-compatible graphics adapter, onboard hard-disk and floppy-disk interfaces, a keyboard interface, a real-time clock, a parallel port, and two RS-232C/RS-422 serial I/O ports. VME Bus accesses are transparent to the processor, so that memory and I/O on the VME Bus appear as though they are within a normal IBM PC/AT environment.

The board's P2 connector carries an interface that is compatible to the IBM PC/XT system bus. By coupling it to a suitable backplane, you can expand the system with standard PC-compatible add-in cards. The PX4010 is a 2-board sandwich that occupies two VME Bus slots. It sells for approximately gld 7500.—Peter Harold

#### JAPANESE SEMICONDUCTOR VENDORS PLACE 1, 2, AND 3 FOR 1988

According to Status 1989, a report from Integrated Circuit Engineering (Scottsdale, AZ, (602) 998-9780), NEC, Toshiba, and Hitachi were the top three semiconductor suppliers of 1988. The companies had estimated sales of \$4.65 billion, \$4.545 billion, and \$3.61 billion, respectively. (The three companies ranked in the same order in 1987.) Motorola, Texas Instruments, and Intel Corp placed fourth, fifth, and sixth, followed by Matsushita, Fujitsu, Philips, and Mitsubishi.

—Steven H Leibson

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MODEL	f <sub>L</sub> to f <sub>u</sub>	min	flatness++	dBm	(typ)	mA	(10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
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**SPECIFICATIONS** SCM-1NL (L=with leads) (typical) FREQ. RANGE (MHz) 1-500 LO,RF DC-500

SCM-1L

SCM-2L

SCM-2NL

(NL=no leads)

10-1000

5-500

6.5 dB

8.0 dB

(L-R)(L-I)

45 35

35 30

25 20

\$5.45 (1-9)

\$4.15 (1000 qty)

CONVERSION LOSS (dB) 6.3 dB Midband

Total Range 7.5 dB (L-R)(L-I) ISOLATION (dB) Low-Band 60 45 Mid-Band 45 40

High-Band 40 35 PRICE \$3.30 (1000 qty) \$4.25 (1-9)

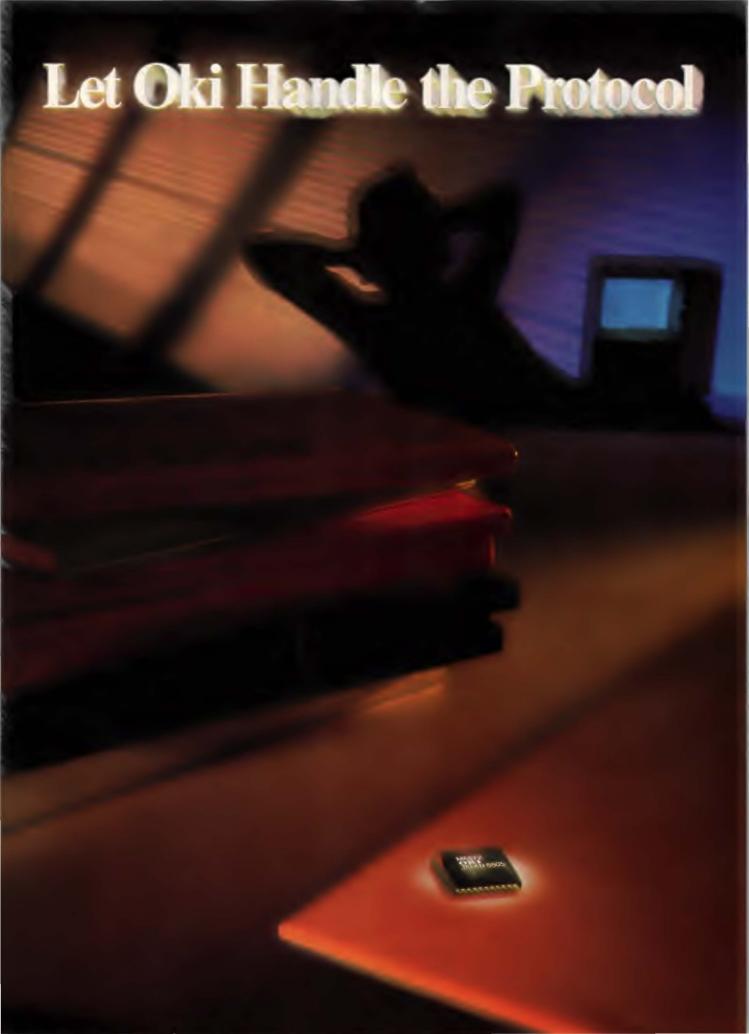
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**CIRCLE NO 46** 

C 115 REV. B



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The new Protocol Serial Communications Controller (PSCC) from Oki Semiconductor is a highly innovative VLSI device which automatically supports LAPB and LAPD HDLC protocols and saves you from having to program and manage them. With a speed of 10 Mb/s, the PSCC also gives you great networking flexibility.

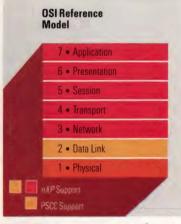
#### **Integrated functions**

The PSCC combines a full-duplex HDLC channel, on-board DMA controller, and 520 bytes of internal RAM. It allows you to send and receive messages directly from memory and frees system intelligence for higher level functions. It automatically supports the update and comparison of state variables for multiframe transmission. In addition, the PSCC supports collision and priority detection.

For even greater integration, the PSCC will be imbedded in Oki's high-performance 16-bit *nXP* microcontroller which will support all seven OSI levels of the ISDN.

#### Great flexibility

Easy interface is provided to standard 16-bit CPUs and to multiplexed buses. The PSCC can be easily customized to support different serial communications protocols. The high speed of the PSCC allows you to create a small inexpensive network, then to expand to a LAN, and later move into ISDN—all supported by Oki.



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The PSCC is only one of the ways Oki can save you time and help you realize competitive advantages. You can also count on Oki for extensive experience, creative solutions, and proven

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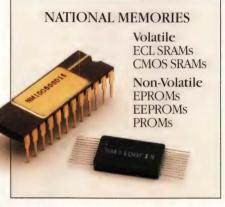
drop the current down to about 120 milliamps.

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It gives you the best ratio of



speed, power and cost per bit.

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#### SIGNALS & NOISE

#### Super Collider will be worth the expense

I disagree with Jon Titus's editorial "Spend a lot, get a little" (EDN, September 1, 1988, pg 51), in which he expresses his opinion that the proposed Superconducting Super Collider (SSC) proton synchrotron is not worth the \$5 billion investment. First of all. Jon seems to feel that since, as he says, "the billions of dollars of tax money needed for SSC must come from other programs' budgets . . . ," the inverse must also be true. Namely, that not building the SSC will suddenly free up these monies for other good purposes such as "refurbishing and rejuvenating college and university laboratories . . . . " That's not the way Washington works, especially with current political and economic realities (such as budget deficits). Like it or not, our politicians will always be inclined to spring for very expensive "glamour" projects (which the SSC admittedly is), but will pinch pennies when money is tight for the more down-to-earth programs that Jon Titus proposes programs that are less visible and lack political clout. To put it simply, if the money isn't spent on the SSC, it will probably be lost for other scientific or technological endeavors.

Jon also overlooks the near-term benefits that would result simply from building as massive a hightech project as the SSC. For instance, the state of the art of superconductivity would, no doubt, be greatly advanced by the mammoth scale of the conductors, the magnets, and the microwave transmitters and waveguides that this huge machine will require. Even my own field of instrumentation and controlsystems engineering could benefit from the development of the exotic sensors and control elements needed for the individual experiments as well as for the SSC itself. Most significantly, the sheer size of this system will demand factorywide automation and integration on a scale that, to my knowledge, has not been attempted. (In my judgment, the control-engineering field is critically weak in large-scale systems integration.) Best of all, these technologies would be readily available, because of the open and international nature of research facilities such as the SSC will be.

Having said all that, I believe nevertheless that the SSC should be judged chiefly by the potential value of the SSC physics—its value to mankind, not just to "a small number of particle physicists." On this point I agree with Jon.

So what is the potential value of the SSC physics? Well, what is the value of Morley and Michelson's experiments, 100 years ago, which showed that the speed of light in all directions is the same? (Those experiments led Albert Einstein, almost 30 years later, to his theories of relativity.) What is the value of Thomson's discovery of the electron or de Broglie's confirmation of the dual (wave/particle) nature of photons? (Those events led Heisenberg, Dirac, Schrödinger, et al, to the revolutionary postulations of the Principle of Uncertainty and the rest of quantum mechanics.)

The SSC could be extremely important to the future of mankind. It provides the same potential for discovery as that enjoyed by the above-mentioned scientists, who are now recognized as pioneers in their fields. The SSC can provide theoretical physicists with the raw material for their speculations on how the universe works, and ultimately, perhaps, form the technological and even the philosophical framework for the next century. What will these discoveries and their resultant technologies and philosophies be? Who can possibly know? How could Albert Michelson and Edward Morley have even guessed, back in 1887, where their disturbing discovery about the

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**CIRCLE NO 30** 

#### SIGNALS & NOISE

speed of light would lead in the 20th century?

Do I exaggerate? I don't think so. Just consider the profound effects of general relativity on our concept of the universe. And what would we electronics engineers be doing if not for modern solid-state physics, which is based largely on quantum mechanics? (We'd all be in different lines of work, that's what.) How different would our lives be without the atomic bomb? Or if scientists in another country or at another time had created it?

Although it's true that the price of the SSC is very high, it's possible that the discoveries made in it could be priceless to future generations, in ways we can't possibly predict.

We will leave our children and their children a tremendous burden of debt, the legacy of our profligate ways. Perhaps the knowledge made possible by the SSC will provide something to show for this debt.

Kenneth C Kmack

Manufacturing Automation Consultant

Lilburn, GA

#### Errata

The Technology Update entitled "Widespread graphics use spawns diversity in data-compression devices" (EDN, September 15, 1988, pg 87) incorrectly quoted the speed of Tekand Labs' continuous-feed scanners as 500 dots × 50 lines/in. Actually, the scanners handle 500 dots × 500 lines/in.

Also please note that the phone number given for Corvallis Micro-Technology Inc in the New Products section of EDN's October 27, 1988, issue (pg 360) is not correct. You can reach the company at (503) 752-5456.

#### WRITE IN

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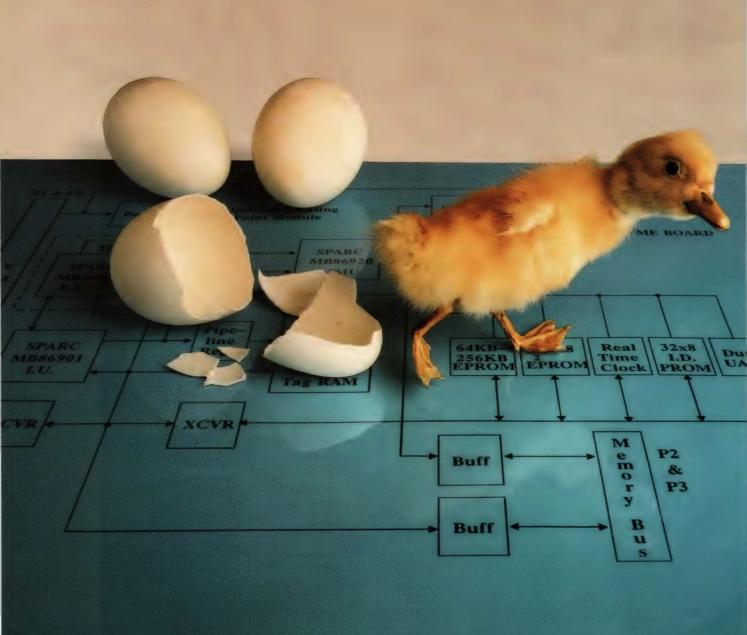


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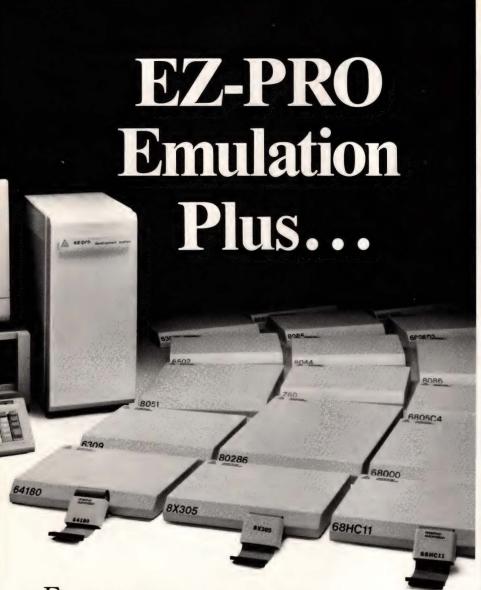
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#### CALENDAR

Real-time System Design: A Hands-on Workshop (short course), Washington, DC. John Valenti, Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (231) 417-8888. January 10 to 13.

SC Global 89, San Francisco, CA. Superconductor Applications Association, 24781 Camino Villa Ave, El Toro, CA 92630. (714) 586-8727. January 11 to 13.

OE LASE '89, Los Angeles, CA. Society of Photo-Optical Instrumentation Engineering (SPIE), Box 10, Bellingham, WA 98227, (206) 676-3290; in Europe: SPIE, Koblenzer Strasse 34, D-5300 Bonn 2, West Germany, 49-228-36-15-46, TWX 172-283-747. January 15 to 20.

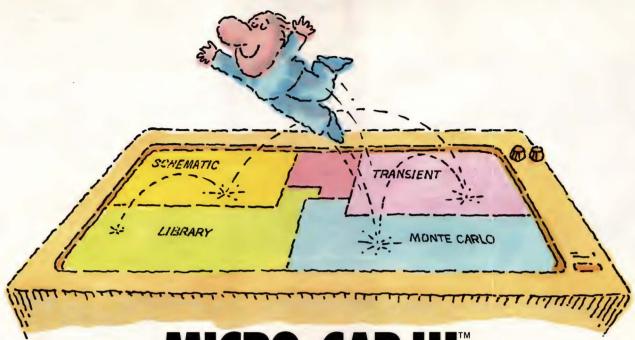
Fifth Annual Computer Graphics New York Show, New York, NY. Exhibition Marketing & Management Co, 8300 Greensboro Dr, Suite 110, McLean, VA 22102. (703) 893-4545. January 17 to 19.

The 1989 Optical Disk Systems Conference: From the Mail Room to the Board Room, Phoenix, AZ. CAP International Inc, 1 Longwater Circle, Norwell, MA 02061. (617) 982-9500. January 23 to 25.

ATE & Instrumentation Conference West, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. January 23 to 26.

Winter 1989 Unix Technical Conference, San Diego, CA. Usenix Conference Office, Box 385, Sunset Beach, CA 90742. (213) 592-1381. January 30 to February 3.

Electromagnetic Interference— Characteristics and Control (seminar), Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N Sixth



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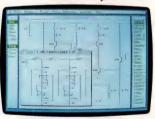
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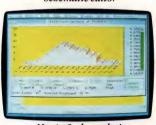
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#### **CIRCLE NO 27**

#### CALENDAR

St, Milwaukee, WI 53203. (414) 227-3120. January 31 to February 2.

Power Electronic Conference '89, Santa Clara, CA. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06854. (203) 852-0500. February 7 to 9.

Software Development '89, San Francisco, CA. Miller Freeman Publications, 500 Howard St, San Francisco, CA 94105. (415) 995-2471. February 14 to 17.

Power Supply Design Seminar, Tampa, Orlando, and Fort Lauderdale, FL; Huntsville, AL. Unitrode Corp, 580 Pleasant St, Watertown, MA 02172. (617) 926-0404. February 21 to 24.

Compcon Spring 89 (34th IEEE Computer Society International Conference), San Francisco, CA. Kenichi Miura, Fujitsu America, 3055 Orchard Dr., San Jose, CA 95134. (408) 432-1300. February 27 to March 3.

Systems Engineering for Integrated Hardware/Software Applications (short course), Los Angeles, CA. John Valenti, Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (231) 417-8888. March 7 to 10.

The Executive Forum on Supercomputing, San Jose, CA. Pat Westly, Westly Enterprises, 3697 S Court, Palo Alto, CA 94306. (415) 494-7115. March 9 to 10.

APEC '89 (IEEE Applied Power **Electronics Conference and Expo**sition), Baltimore, MD. Trey Burns, Data General Corp. 4400 Computer Dr, E213, Westboro, MA 01580. (508) 870-9182. March 13 to 17.

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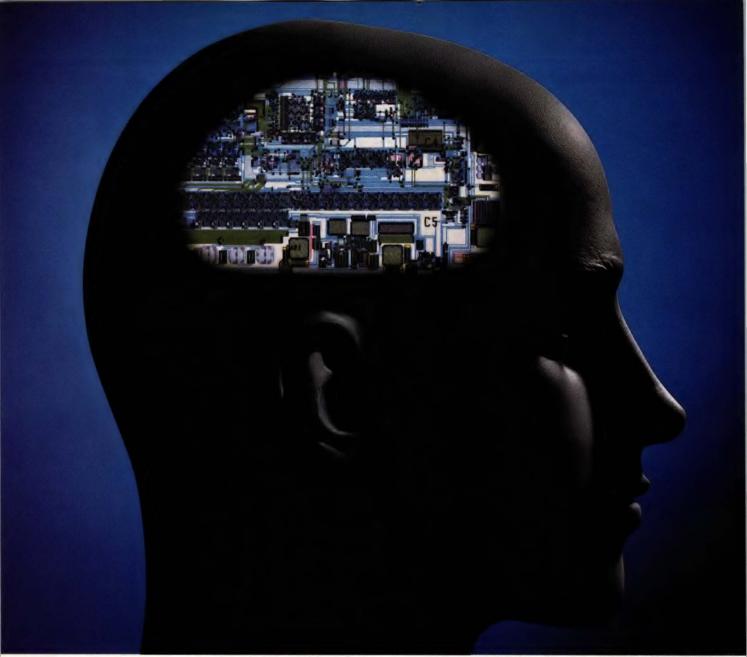
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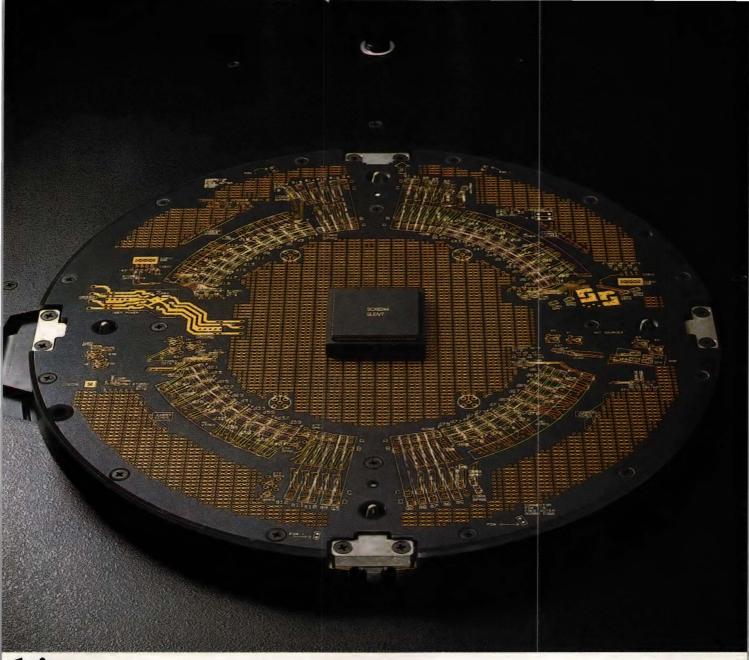
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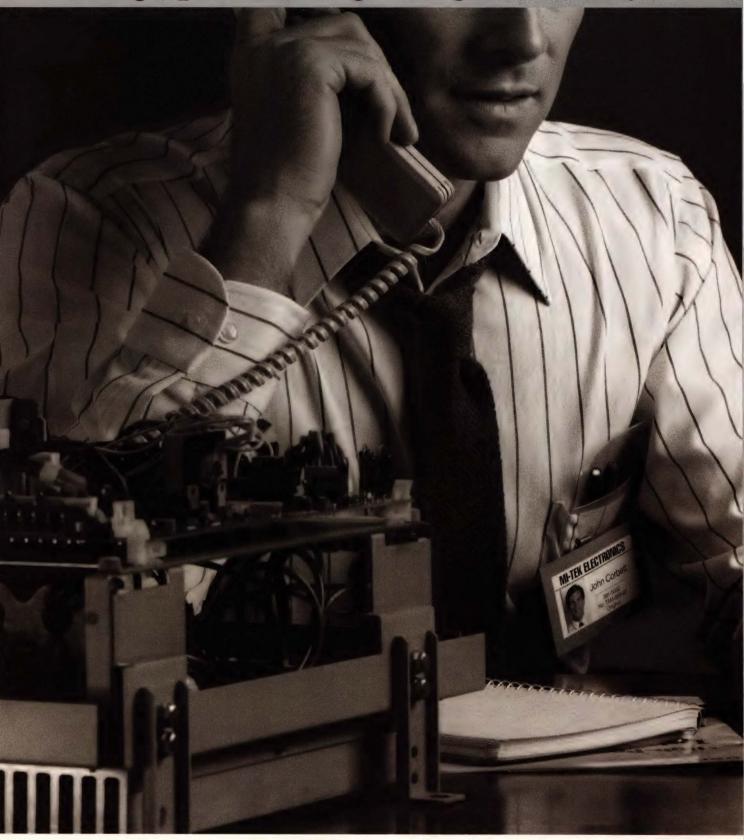
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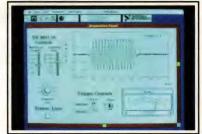
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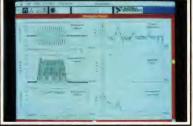
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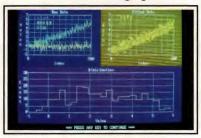
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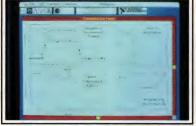
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## **EDITORIAL**

## Honesty pays



Recently, I received a letter from Bill Windsor, a strategic marketing manager at Analog Devices Inc in Norwood, MA. Bill's letter told me that ADI has discontinued the development of its ADSP-3264, a floating-point math chip that was announced about six months ago. Many companies stop product-development projects, but most don't go out of their way to announce it—least of all to members of the press. Usually we discover such announced, but undeveloped products when we see an "Advance Information" data sheet and call a manufacturer for more information.

Bill and the people at Analog Devices get the editors' cheers for being forthright and honest about a product's demise. In the long run, such honesty will win friends and customers for ADI.

Unfortunately, not everyone has such high standards. In fact, many companies want to publish product-application articles that would appear simultaneously with a product's introduction. It's hard to believe that engineers and marketers can develop real applications for products before they exist, but they frequently do. It's easy to draw a flow diagram of a program or a schematic diagram of an imagined circuit and then pass it off as an application. When manufacturers are confronted with the absence of any real chips or devices, we hear excuses such as, "Well, it worked for the earlier version of the chip," and, "But we simulated it."

Applications based on simulations can be misleading because simulations can miss problems and bugs. For example, the November issue of *Microprocessor Report* describes the simulation of Intel's 80960 microcontroller chip. Although three programs ran millions of simulations on the 80960 design, none of them caught one remaining bug. It turned out that all three simulator writers made the same mistake. The danger of running application articles based on simulations alone should be obvious.

Suppose, though, that a company publishes a promotional application article far in advance of a product's existence. Several months after the article appears, the company is acquired by management that decides to end many developments. Now, readers have an application article that describes how to use a product that never existed—although the readers may think that the product's introduction is pending. Whether or not the product ever exists, the promotional-application approach misleads people, and in my opinion it's dishonest, too.

Someone once said that honesty is the best policy. It should be the *only* policy.



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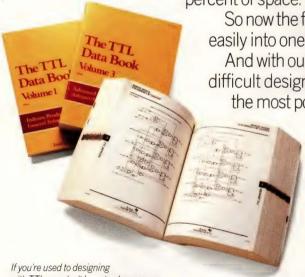
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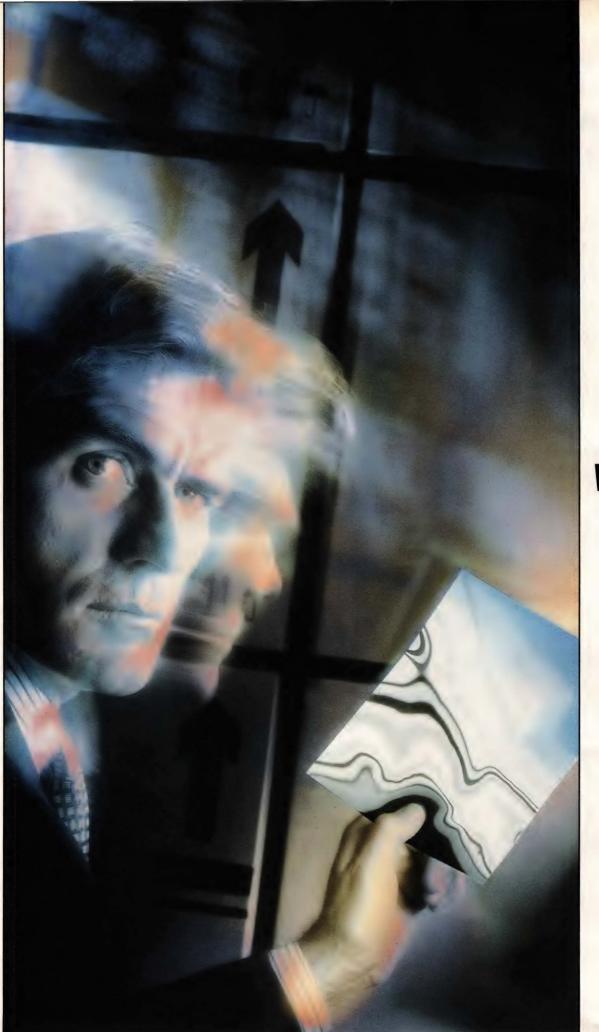
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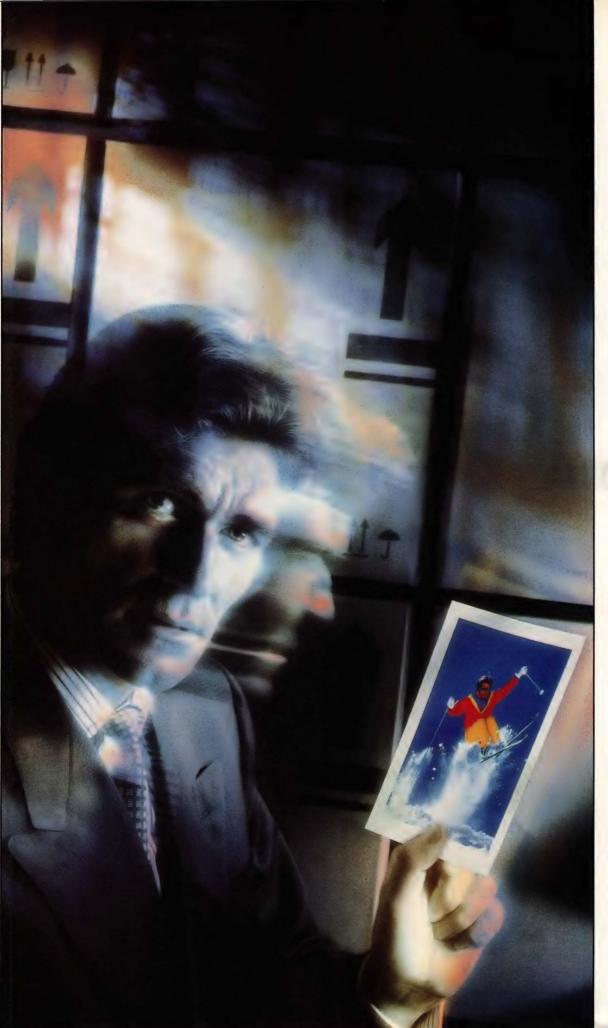


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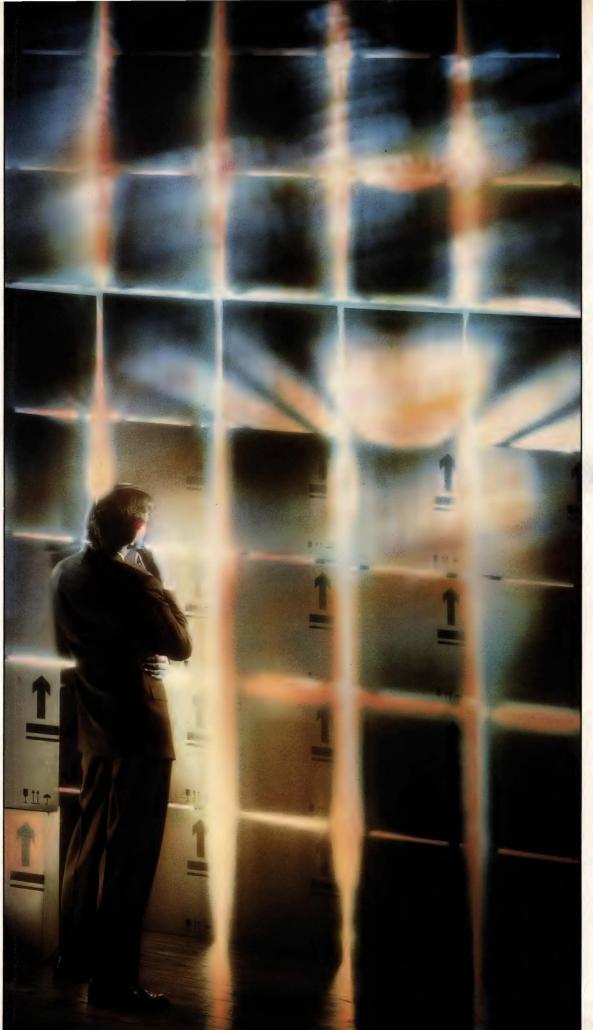
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## TECHNOLOGY UPDATE

#### VXI BUS SPECIFICATIONS

# Manufacturers tackle cloudy software issues



The VXI Bus specifications are shaping up, but they're still soft in the software department.

J D Mosley, Regional Editor

o be sure, the new VXI Bus specifications provide the instrumentation industry with the hardware compatibility that eluded its precursor, the VME Bus. But the proposed guidelines intentionally ignore issues concerning the VXI's sophisticated software options, particularly the sharedmemory protocol for communications between instruments. In trying to maintain a balance between the engineers' need for standardization and the manufacturers' need to distinguish their own products, the members of the consortium have created a situation where some crucial software standards may be established in the marketplace rather than the committee room.

Still under development and revision, VXI—which stands for VME Bus Extensions for Instrumentation—is an expansion of the VME Bus and is

specifically designed to boost instrumentation performance and make more efficient use of board space in a variety of ways. A consortium of companies has developed clear hardware parameters for the VXI Bus instrument-on-a-card architecture. However, the system-level software specifications remain unaddressed, as Tektronix and HP are busy preparing what may become the defacto software standards for this new instrumentation bus.

One reason for this disregard is that the authors of the VXI Bus specifications come from a group of competing instrumentation companies (see box, "For more information...", pg 68). Although the consortium belongs to the IEEE P1155 committee for modular instrumentation and will eventually submit the guidelines to the IEEE for approval, the group is still an informal collection of competitors, and each company's intentions are far from altruistic.

#### Compatibility is crucial

These manufacturers are aware that some level of compatibility among instrumentation devices is necessary to encourage a broad acceptance of the new specifications. Indeed, the lack of such compatibility in the VME Bus domain forced these companies to band together and extend the standard in the first place. But a number of system-level



To provide control panels for those embedded VXI instruments, try using the GPIB-VXI interface from National Instruments, in conjunction with its LabView 2 graphical software interface.



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#### TECHNOLOGY UPDATE

#### VXI Bus specifications

software-integration issues remain unresolved because consortium members simply cannot agree beyond the hardware register levels already defined in the guidelines.

#### A closer look at VXI

At the hardware level, the standard offers higher system throughput and more precise timing and synchronization in comparison to its precursor, the VME Bus. Unlike the way some terminology is used in connection with the VME Bus, "modules" for the VXI Bus refer to the physical cards that fit into the mainframe (or chassis); "devices" refer to the instrument functions themselves. One module may hold several devices. On the other hand, one device may require one or more modules.

You can fit as many as 13 instru-

ment modules into each VXI Bus mainframe, and address as many as 256 instrument devices per system. It's significant that, by developing modules that contain multiple instruments (or by using virtual instrumentation schemes to expand the versatility and functions of each module), you could conceivably house 256 different types of instrument devices in a single mainframe, and each of those devices could have its own logical address. In contrast, a VME Bus mainframe has 20 slots, but the VME specifications make no provision for an extension chassis or for communication among mainframes.

Fig 1 illustrates the specified VXI architecture. The hybrid devices include VME Bus devices that don't comply with the VXI Bus requirements but can nevertheless

communicate with or make use of VXI Bus devices. On the tier below that, the VXI Bus accommodates four types of devices: messagebased, memory, extended, and register-based devices. The messagebased devices are the simplest level of software communications as defined in the specifications and use word-serial protocol. The memorydevice sector is included in the specifications but left undefined. Extended devices are VME devices that have been enhanced to operate on a VXI Bus. The register-based devices can offer either A16-only, or A16/A24 and A16/A32, or all three types of control, to run, for example, A/D or multiplexer functions.

#### Slot 0 handles common resources

The physical VXI Bus system reserves one mainframe slot for a Slot 0 module with a modified P2 connector for central handling of common bus resources, such as backplane clocks, MODID (module-identification) configuration signals, and synchronization signals. The Slot 0 controller can detect all the modules in a VXI Bus system, even if a module is inoperative.

VXI mainframes provide 1.2-in. slot spaces between modules to allow for individual shielding for each device. That specification retains the 16-bit P1 connector and the center row of the P2 connector, as defined by the VME Bus guidelines, but also defines the outer rows of P2 for 32-bit data transfers, adding functions such as clocks, TTL (and sometimes ECL) triggers, a module-identification bus, an analogsum bus, and extra power and ground conductors. Accordingly, you can mix VME and VXI modules within a single system. The VXI's automatic module-identification provisions eliminate any need for manual system configuration.

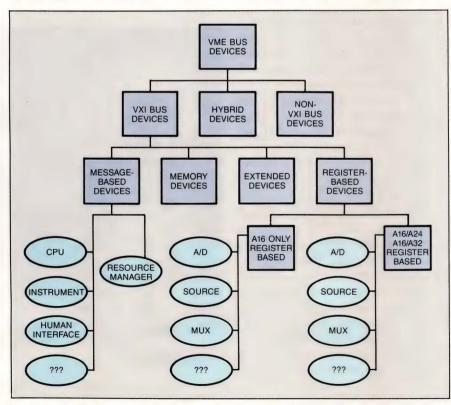


Fig 1—The four major VXI Bus device classifications are based upon the protocol supported by the various types of devices you can use in a VXI Bus system. Hybrid devices are VME Bus devices that don't comply with VXI Bus requirements, but can communicate with or make use of VXI Bus devices.

#### TECHNOLOGY UPDATE

#### VXI Bus specifications

In addition, the VXI specifications describe two new modules, C-and D-size modules, which are both based on the Eurocard format; the new modules are more than twice as long as the A- and B-size versions and thus double the available board space per module. The D-size module also sports a high-performance P3 connector with a 100-MHz clock and ECL triggers.

In the hardware department, the new VXI parameters are fairly thorough and clear. They spell out mechanical, environmental, EMI, cooling, and power considerationsall of which may ultimately reduce the cost of modules because the devices can share hardware resources like power supplies and timing circuitry. Such sharing also frees additional board space so that manufacturers can shrink complex instruments to fit on a single card or expand the number of instruments per module. A defined set of configuration and communication registers maintain low-level hardware compatibility among different manufacturers' instrument modules.

#### Message-passing techniques vary

But it's really the intermodule communications for synchronization and data transfer that makes the VXI Bus a superior instrumentation format. One software module that is defined within the VXI Bus guidelines is the Resource Manager. You can order this program as firmware that can reside either on any VXI module or outside the VXI chassis on a network or in a host computer. The Resource Manager, in combination with the Slot 0 module, preforms several key tasks: It identifies every VXI Bus device in the system and configures any necessary resources. In addition, it manages the self-test and diagnostic sequences and establishes the system's address maps.

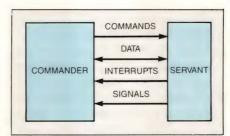


Fig 2—The VXI Bus features a commander/ servant hierarchy in which the commander controls one or more servants, but each servant has only one commander to which it can send interrupts, signals, and data.

The program also initiates normal operation of the system and determines the system's commander/servant hierarchy.

The commander/servant hierarchy is the heart of the VXI Bus system. Each device that controls at least one other device is called a commander. Commanders are also bus masters (they can gain control of the bus when they need it). The commanders can have multiple servant devices to which they send either register- or message-based communications. As a servant under the control of a commander device, a device can have only one commander and can send signals and interrupts to that commander, as illustrated in Fig 2. A commander can also be a servant to another commander.

This hierarchy is based upon a layered set of communication protocols (Fig 3). Every VXI device has a set of configuration registers that are accessible from connector P1. These registers allow the system to identify the device, including its type, model, and manufacturer; its address space; and memory requirements. A device that offers only this configuration-register set is called a register-based device.

#### Devices might exchange data

On the other hand, a messagebased device has communication registers, and it also uses specific communication protocols to exchange data with other devices or modules. The VXI Bus guidelines describe a word-serial protocol as the simplest communications that use the data and response registers to transfer data between commanders and servants in a serial fashion along a 16-or 32-bit data path. All communications between messagebased devices begin with the wordserial protocol, and may progress to a higher performance protocollike a shared-memory protocol—if both devices are capable of following such a protocol.

Shared-memory protocols are either connection or operational protocols. A connection protocol establishes a shared-memory communications path; an operational protocol does that and more—it determines how communications occur through the shared memory. Thus,



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#### TECHNOLOGY UPDATE

#### VXI Bus specifications

whereas word-serial communication is limited to communication between commanders and servants, shared-memory communication can occur between peers at both the commander and the servant levels. In addition, shared memory allows commanders to communicate with servants other than their own.

#### Memory protocols are vague

Unfortunately—and this is quite significant—the specifications don't detail how to use the shared-memory protocols. Although the Resource Manager retains data regarding the system configuration, the guidelines don't define any way for the Resource Manager to control device access to shared memory. The specifications also fail to describe how shared memory is managed or how a device actually obtains the right to use a portion of memory.

Manufacturers could decide individually to provide controls with dual-ported memory or through the operating system, but the consortium established no uniform method. Accordingly, each manufacturer is free to decide how to build multiprocessor VXI Bus systems that can efficiently distribute tasks.

Hewlett-Packard and Tektronix are both working on a standard communications interface to exploit the high-level communications that the VXI Bus makes available. At present, the addressing scheme is a major point of contention.

The VXI Bus specifications provide for an interface between the IEEE-488 bus and the VXI Bus interface and defines protocols for transferring data, clearing the bus, triggering signals, serial polling, local lockout, and SRQ commands. This interface makes communications between a GPIB controller and VXI Bus devices transparent

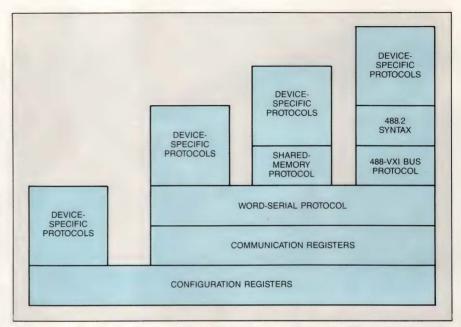


Fig 3—The VXI Bus specifications offer flexibility. Depending upon your system's configuration, you can meet its communication needs within the VXI Bus architecture by selecting the required level of sophistication.

by converting IEEE-488 bus protocols to VXI instrument protocols and by translating GPIB addresses to VXI logical addresses. But the interface doesn't specifically dictate a method for address mapping.

#### Two-tier addressing is one way

HP's recommendation retains close similarity with the current industry-standard GPIB programming environment. The HP solution uses a multiple secondary-addressing scheme that relies upon a primary address for the VXI Bus system and as many as thirty secondary addresses for individual VXI devices. Such a 2-tiered approach adds another level of communications to the system, but retains compatibility with GPIB addressing schemes. It also allows a system developer to maintain his or her investment in GPIB software.

However, this method artificially limits a VXI system to 31 devices; what's more, you can't employ this method in conjunction with any external protocols other than those specified in the IEEE-488 standard. But then, HP did originate the GPIB and maintains an interest in its continued success.

Tektronix rejects HP's multiplesecondary-addressing solution, preferring instead a logical-naming convention called embedded addressing. Using compound-command program headers, the Tektronix solution defines the bus system as a single address and identifies each device as a unique logical unit. This arrangement permits direct communications between an external controller and any of the VXI devices (to the 256-device limit). However, there is a slight decrease in system performance due to the extra overhead. The company claims only a 1% increase in execution time.

Tektronix's approach also requires a software interface called the VXI Bus C Language I/O System. This I/O system manages all VXI-defined communication protocols and relieves you of the task of redefining your device-specific



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#### VXI Bus specifications

application software for use in a VXI Bus environment. The I/O System operates on a C functional level, uses an embedded real-time kernel, and provides a set of I/O routines that allow applications to communicate across the VXI Bus. Low-level drivers let you access word-serial protocols and commands, shared-memory protocols, signals, and interrupts.

Two products, one from Radix Microsystems and the other from National Instruments, illustrate some of the variety that companies are offering in their VXI Bus devices. The EPC-2 from Radix MicroSystems is a 2-slot C-size VXI module that includes an embedded PC and uses embedded addressing. The EPC-2 comes with a 40M-byte SCSI hard-disk drive, a 1.4M-byte floppy-disk drive, a VGA controller, a GPIB controller, and Slot 0 functions. It sells for \$9550 with 1Mbyte of RAM, but you can expand the RAM to 8M bytes.

The EPC-2 also comes with software, including the Configurator, a program that lets you define the location and attributes of both VXI

and VME cards for storage in the EPC-2's database. An on-line Resource Manager lets you dynamically allocate reusable resources. And a message-based system permits an application to communicate with any device in the system—regardless of whether the device is a GPIB instrument or even if it's located in another chassis. The EPC-2 uses several layers of software bridges to permit hierarchical communications and window-based diagnostic functions.

Another company, National Instruments, offers a C-size message-based VXI Bus module called the GPIB-VXI (Fig 1). It's an intelligent device with a 68070 µP, which has its application program in firmware; the module facilitates communications between the GPIB and the VXI. The GPIB-VXI provides Slot 0 functions, controls VXI Bus trigger lines and protocols, lets you download custom code via the IEEE-488 bus, and offers an interface to the company's LabView 2 and LabWindows software packages.

This latter point is of particular

interest, because VXI Bus devices lack traditional control panels, and the graphical interfaces provided by both LabView and LabWindows let you design a control-panel image on your computer monitor. Thus, you can provide system operators with a simple user interface for controlling embedded VXI devices. The module has four dual-ported RAM options, three ROM options, and support for both secondary-address mapping and embedded-address mapping. Pricing starts at \$3000. LabView 2 costs \$1995 and the standard LabWindows package sells for \$495.

#### References

1.VME Bus Extensions for Instrumentation (VXI Bus) System Specification, Rev 1.2, June 21, 1988.

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#### For more information . . .

For more information on the VXI Bus specifications or on the products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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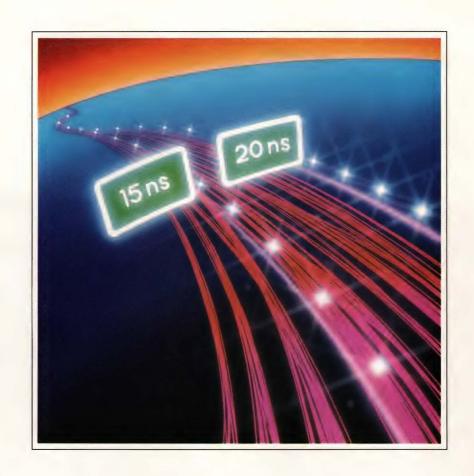
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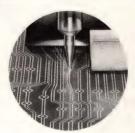
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### RISCs force move to compilers



RISC technology is not without its risks.

Charles H Small, Associate Editor educed-instruction-set computers (RISCs) promise to speed up computer systems. That's the good news. The bad news is that 70% of EDN's readers do the bulk of their embedded-system programming in assembly language. RISC-compiler writers insist that software engineers will be forced to shift to compiled, high-level languages if their companies adopt RISC processors.

Adopting RISCs and consequently shifting software-engineering methodology from assemblers to compilers and other ancillary high-level tools would force these changes in software development: (1) programmers would have to abandon assembly language and instead write in high-level code, (2) programmers would not be able to hand-tune or -assemble programs, and (3) debugging

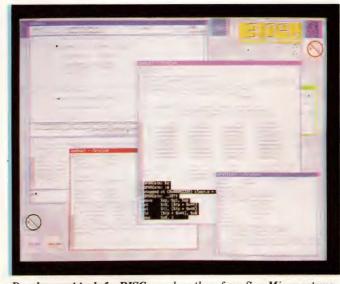
would be more difficult than for complexinstruction-set computers (CISCs). The adoption of RISCs would also mandate that software engineers undertake an extensive compiler-evaluation program and learn to use these new tools.

High-level programdevelopment tools are the rule for native-system development. But EDN readers, much more so than the general run of applications programmers, program embedded systems. The challenges of developing programs for embedded systems differ from those of native-system development.

Embedded systems lack the usual computer I/O devices, such as CRTs, printers, and mass storage. Instead, they have system-specific I/O. Further, embedded systems often must respond to asychronous inputs much faster than many high-level-language programs and operating systems possibly can. Consequently, most embedded-system software engineers have stuck with assembly-language programming.

#### A good compiler is hard to find

RISC-processor makers and major third-party software vendors are readying complete suites of high-level tools for developing RISC code for both native and embedded systems. Their first products support C++ Fortran; Forth;



**Development tools for RISCs,** such as these from Sun Microsystems, link the source code to the program running in the target system.

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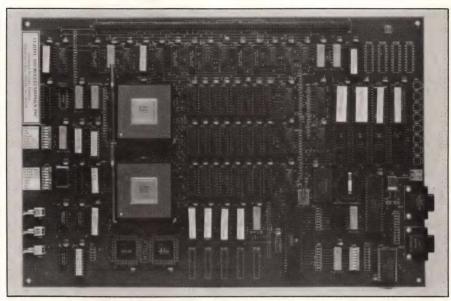
#### RISC compilers

and, given the Department of Defense's insistence upon it, Ada. Products supporting other, more obscure languages, such as Smalltalk, Cw, Prolog, Lisp, Modula 2, and Pascal, are under development.

Along with the compilers, you should look for cross compilers, high-level-language debuggers and ROM debuggers for embedded applications. At present, Sun Microsystems has a ROM debugger for its SPARC RISC. Intermetrics, showing its embedded-system orientation, has RISC compilers that can produce Hewlett Packard-style cross-reference files that hardware-based debugging aids, such as logic analyzers and software-performance analyzers, can use for source-code debugging.

#### Runnable code is no problem

You can take for granted that, except for the usual number of minor bugs that you find in newly minted programs, all RISC compilers generate "runnable" code. But, RISC programs, far more so than CISC programs, benefit from the optional optimization step of compilation. And, you can expect individual RISC optimizing compilers to vary extensively in their ability to improve the performance of programs written in high-level languages. Potential optimization gains are much greater for RISCs than for CISCs. Turning on the op-



This evaluation board, the Fujitsu Microelectronics MB86900 EBOO, contains a 16-MHz SPARC RISC processor.

timizer in your RISC compiler can shrink the size of a program by onehalf and cut its run time by twothirds.

If you do not use an optimizing compiler, the expected performance gains of your RISC over a CISC could prove illusory. For example, experts differ on just how many more instructions a RISC program needs as compared to an equivalent CISC program, but estimates run from 30 to 200% more. Without optimization, your RISC program could be alarmingly overweight and disappointingly slow.

Unfortunately, no easy method exists to judge which compiler is

the best. Software engineers will have to rely on extensive evaluations involving the compilation of many real programs (as opposed to benchmarks) and, possibly, the anecdotal advice of other users to select the best compiler for their application.

#### Magazines off the mark

Embedded-system software engineers will not be able to rely on comparisons in third-party sources, such as computer magazines, because these sources do not reflect their concerns. For example, compilation speed ranks high in compiler evaluations. But, embedded-system

#### What makes a RISC different from a CISC?

RISCs differ significantly from conventional complex-instruction-set computers (CISCs), although future CISCs will probably have many RISC-like features. In general, the features unique to RISCs are

- Simple instruction sets that provide only one way to perform a given operation
- No instructions for manipulating or modifying data in memory
- No internal microcode

- Large internal register sets
- Many triple-address instructions that have two source registers—not memory locations—and a single destination register
- Few addressing modes for reading and storing
- Architectures that are so heavily pipelined that the processors almost always execute the statement after a branch statement, even if the branch is taken.

#### RISC compilers

programmers are much more interested in issues that are seldom mentioned, such as the quality of error messages, support for hardware-based debugging tools, ROM-able-code generators, and the effectiveness of the optimizer.

#### Simple instructions hard to use

On the surface, the assertion that RISC processors will force software engineers to use compilers and that these compilers will produce complex, hard-to-follow program threads, seems paradoxical. After all, RISCs should, by definition, have a simple instruction set. But, a simple instruction set alone does not guarantee simple assembly-level programs.

The purpose of the simple instruction sets is not to make RISCs simple to program, but to permit simple but fast processors that can execute instructions in a single cycle and, hence, need no internal microcode. To achieve their high exe-

cution speeds, RISCs are heavily pipelined. This design philosophy puts severe strain on a RISC's main memory and floating-point unit to keep the RISC's pipeline full of data and instructions without holding up the processor. Because RISC processors outrun RISC memories and peripherals, RISC programs have to be modified extensively to make up for the speed differential.

RISC compiler writers maintain that the sheer volume of optimization needed because of these hardware constraints is too much for mere humans to do manually at the assembler level. They also say that the kind of hand optimization that is possible with CISC code—primarily selecting the best instruction for a particular operation—doesn't work with RISC code because RISCs don't offer a variety of related instructions to do the same job.

Although RISC programs can benefit from all the standard optimization techniques that compiler writers have been using for some time with CISC compilers (see box, "Optimizers fine-tune your program automatically"), RISCs' instruction sets and hardware constraints change the traditional code-generation priorities and procedures.

Some compilers, such as those from Language Processors Inc, perform optimization at several stages during compilation—usually global optimization on the intermediate-level file and one or more passes of local, or "peephole," optimization on the assembly-level file. Software engineers cannot simply submit a hand-written assembly-level file to an optimizer because, at present, no assembly-level optimizers are available.

When writing code for CISCs in high-level languages, software engineers can often effectively handtune their compiler's output. This hand tuning often takes the form of substituting a more efficient

#### Optimizers fine-tune your program automatically

Optimizers methodically scan and improve your program in several ways. An optimizer normally removes all dead code—code that never gets executed. Examples of dead code are subroutines that never get called, WHILE loops that never get executed, calculations that get performed but whose results aren't used or stored, and DO loops that always execute only once. In fact, optimizers have been known to ruin hardware-setup routines that involve repeated writes to the same address; the optimizer mistakenly indentifies these setup routines as redundant writes and eliminates the "extra" ones.

Optimizers rearrange your code in several ways. One way is branch-tail merging, which is the process of pulling common statements out of both branches of an IF-THEN-ELSE construct and putting just one instance of the common statements at the end of the construct. An optimizer can also remove redundant jumps. That is, if you have a jump statement to yet another jump statement, the optimizer jumps directly to the second statement's destination.

Less obviously, if you have nested WHILE statements, an optimizer jumps directly to the outer WHILE when the inner WHILE fails instead of jumping first to the inner WHILE's exit point.

Another way optimizers can rearrange your code is by violating some of the overly restrictive rules of structured programming, such as requiring all routines to have just a single exit point. An optimized CASE statement has an exit point for each clause.

Optimizers also pull invariant operations out of loops, so that the operations are executed only once prior to entry into the loop rather than being executed once for every pass through the loop. Optimizers sometimes partially unroll a loop and concatenate several passes through the loop into a monolithic segment of straight-line code. Such unrolling often makes a good tradeoff between increasing the code space and lowering loop overhead, thereby speeding execution.

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#### RISC compilers

instruction and addressing mode for an instruction or group of instructions chosen by the compiler. This scheme doesn't work for RISCs because of their simple instruction sets—you just don't have a lot of choices.

Therefore, RISC compiler writers assert that their compilers can do a better job of optimizing RISC code automatically than software engineers can do manually. Their assertion is based on the observation that RISC programs benefit, to a much greater degree than do CISC programs, from two optimization techniques that especially suit the hardware constraints of RISCs processors: instruction shuffling ("scheduling") and register optimization.

RISCs run so fast and are so heavily pipelined that they seem to exhibit what amounts to programflow inertia. That is, most RISC processors execute the first instruction following a branch, even if the program flow takes the branch. It's almost as though the RISC is running so fast that it cannot swerve quickly.

For a first cut at unoptimized, "runnable" code, the compiler can simply place a NOP (no operation, or dummy instruction) after every branch. Such a program will run, but could be made more compact and swift if the compiler's optimizer searches for an instruction that can be moved, without harm to the program's operation, from its place in the program's flow as specified by the high-level code and inserted after the branch instruction.

An optimizer can further shuffle instructions to make sure that the

RISC processor does not have to wait for slow external systems, such as main memory or a floatingpoint processor, to respond. For example, the AMD 29000 takes four cycles for a memory store. Therefore, if the optimizer spaces all store instructions at least four cycles apart, the 29000 will never have to wait for the memory system. Note that the 29000 will always work properly no matter how slow its memory is. The pipelines of some RISC processors can get corrupted if load and store instructions create a hazard.

Instruction shuffling is not a new technique, but it has had limited application to CISCs. The technique is especially hard to apply to a CISC if, as is the case for the 68000, the manufacturer doesn't publish instruction timing. Without

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an exact idea of how much time each instruction takes, a compiler writer cannot write an optimizer that can choose the fastest way to accomplish a given function.

Even given exact timing specifications, instruction shuffling is much more complex for CISCs than for RISCs. Optimizers for CISCs generally only work with a small subset of the instruction set; RISC optimizers use the entire instruction set.

#### Registers beg for optimization

The second optimization technique that particularly suits RISCs is register optimization. Because of the heavy penalty memory acceses exact upon a RISC's performance, RISC compiler's optimizers strive to keep all data in registers for as long as possible. The optimizer can

#### For more information . . .

For more information on the RISCs and RISC tools described in this article. contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request

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#### RISC compilers

try to follow a calculation to its ultimate end and only allow the contents of a register to be written out when the calculation is completely finished. The optimizer can also endeavor to follow data being passed between routines and try to pass as many parameters in registers as possible. Because of the large register sets, RISC-compiler writers assert that manual register allocation is not nearly as effective as that done by an optimizer.

As an example of one of the many things that must be taken into consideration when allocating registers for the AMD 29000, an optimizer must try to save base addresses in registers because this RISC, like all RISCs, has no 32-bit immediate instructions. Immediate values can occupy only a portion, or field, of a 32-bit instruction.

Optimization is not a panacea, however. High-level languages and operating systems do impose some constraints on instruction shuffling and register allocation. The compilers must be careful to observe program-module boundaries, exception-handler restrictions, and multitasking partitions.

Also, optimization has a major, deleterious effect on high-levellanguage debuggers: Optimization confuses and stymies them. Because the optimizer muddles the one-to-one correspondence between the high-level code and the corresponding assembler code, high-level language debuggers often have just as much trouble as humans do when trying to follow the execution thread in an optimized RISC program.

Software vendors are meeting

the challenge that optimization presents to high-level-language debuggers by suggesting that you do all your debugging before switching on the optimizer. Software engineers who have to debug real-time code may find this suggestion unacceptable because they need to observe their programs running at full speed.

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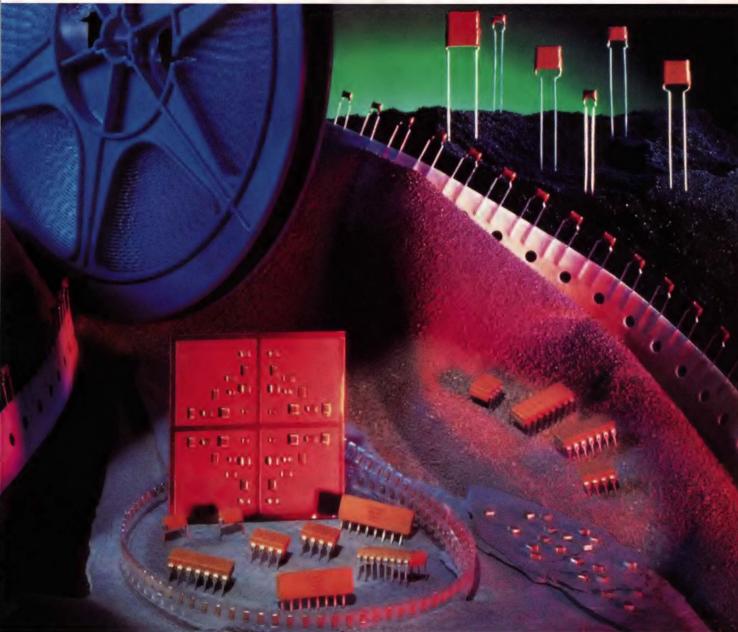
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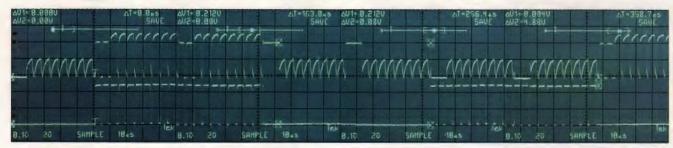
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# Tools allow debugging of software, firmware



Anything more complicated than adding a turnkey SCSI host-adapter board to a personal computer as a diskor tape-drive interface requires firmware or software development.

Maury Wright, Regional Editor

ompared to a relatively simple hardware design, implementing the Small Computer Systems Interface (SCSI) in a host computer or a peripheral controller entails a sizable firmware-and software-development task. Luckily, several companies offer test and development tools that allow you to functionally and comprehensively test firmware and device-driver software for such designs. The tools are capable of performing passive capture and analysis of signal states and bus phases as well as active emulation of the host and the peripheral.

When designing a SCSI interface, you'll find that designing and testing the hardware is simple. Many companies offer intelligent VLSI ICs to implement the SCSI hardware interface. With the exception of a few older first-generation chips, these ICs handle the bus-handshake, -arbitration, and -protocol functions. In fact, the ICs by definition conform to the SCSI bus hardware specification and do not allow violations of the spec.

The VLSI chips suit most design applications, so you don't usually need specialized SCSI hardware-test equipment for debugging. The SCSI ICs interface to µPs in

the same manner as other peripheral chips, and you can test your pc-board design with traditional tools such as scopes and logic analyzers. Furthermore, choosing board-level products such as host adapters can remove the burden of hardware design testing completely.

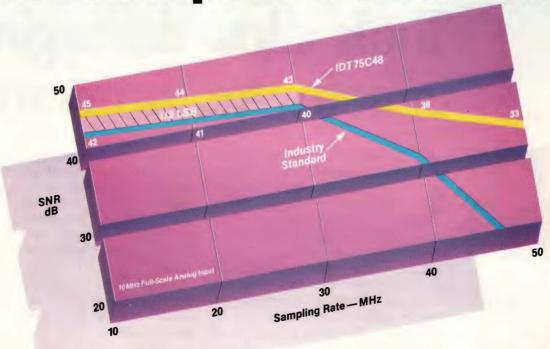
Anything more complicated than adding a turnkey SCSI host-adapter board to a PC as a disk- or tape-drive interface requires development of firmware or software (or both), which means that you have to be able to perform testing and debugging.



Single-stepping through SCSI bus operations is possible with the Rancho Technology SCSI Byte Grabber. This capability allows you to inexpensively debug SCSI firmware.

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In chip-level designs, for example, you have to develop firmware to control the basic operation of the SCSI IC. Peripheral-controller designs typically include a single  $\mu P$  to manage the SCSI interface and provide the control function. The portion of the firmware dedicated to the interface responds to bus activity and controls the flow of data to and from the peripheral.

Host designs include a dedicated  $\mu P$  or, in some cases, the host CPU manages the SCSI IC. The firmware handles SCSI transactions such as instigating or responding to bus activity and completing data transfers.

For both chip- and board-level host implementations, you also have to develop operating-system device drivers.

The SCSI testing and debugging tools available all share one common feature—they connect to the unit under test via the SCSI bus and thus provide true functional testing. Passive tools simply monitor or capture and analyze bus activity. Active tools actually emulate a host or a peripheral device. Some tools have both passive and active capabilities. Ultimately your application—and your budget—will determine which tool you choose.

#### Which tool to use?

If you require minimal datacapture capabilities and don't want to spend too much money, the SCSI Byte Grabber from Rancho Technology may fulfill your needs. The product functions as the physical interface between a host and a peripheral. It passively monitors all SCSI control and data signals except for one-the REQ signal. Because it has control of this signal, the Byte Grabber can control all SCSI bus activity and make the bus operate in a single-step mode. Front-panel LED indicators let you monitor the bus's control signals,



Analysis and emulation software from Pacific Electro Data allows you to stimulate bus activity, capture all SCSI transactions, and analyze the results.

and a 2-digit hexadecimal display lets you see the data lines. Although limited in capabilities, the \$380 device offers a low-cost way of testing a SCSI design.

If you need more data-capture ability but want relatively low-cost testing, consider the Flexstar FS600 SCSI Bus Monitor. The FS600 can passively capture 8k bytes of SCSI bus activity, operates at SCSI bus speeds of 1.5M bytes/sec, and costs \$1800. The bus monitor includes a parallel-printer port so that you can print the captured data. The monitor will output your choice of raw control and data signals and disassembled bus phases with or without the captured data bytes.

#### More analysis is possible

For more extensive analysis needs—and corresponding higher cost—Ancot, Pacific Electro Data, and Peer Protocols all offer SCSI testing tools. Products from all three companies allow you to capture and analyze SCSI bus activity

based on a variety of conditions. All of the tools employ event triggering and time stamping; they don't needlessly capture data into limited-size buffers when the SCSI bus is idle. The products use time stamping to provide information such as time elapsed during a test, time elapsed since last event, and time elapsed between any two events.

Ancot's Model DSC-202 analyzer includes a 68008 local µP and comes in a stand-alone case. You control the Ancot product via a terminal or a personal computer connected via one of two serial ports. The other port can connect directly to a printer.

Pacific Electro Data's PED-4000 Series and Peer Protocols' 2000, 3000, and 5000 Series each use a personal computer as a host for the development system. The products include an IBM personal-computer-compatible add-in board and software.

You have a choice of controlling the Ancot, Pacific Electro Data, and Peer Protocol analyzers via

#### SCSI DEVELOPMENT SYSTEMS

menus or by developing your own control programs. The analyzers can selectively capture activity based on trigger conditions: You can choose to capture all data transmissions or only selected portions. The menu interfaces of all the products allow a fair amount of flexibility in controlling the capture operation. Furthermore, because you have the option of developing your own control programs, you can set the products to selectively capture almost any conceivable event or events.

Peer Protocols' analyzers capture bus activity based on bus-phase changes. Because several signal transitions occur between phase changes, some engineers may construe this capture approach as a potential weakness. Not so, says company president Herbert Silverman. He believes that, provided the hardware is working, you don't need analysis at the individual control-signal level to debug either the software or the firmware. The prod-



Triggered by bus-phase transitions, the Peer Protocols Peer-3000 can analyze bus activity and provide time stamps with 1-usec resolution.

ucts from Peer Protocols all provide 1-µsec resolution time stamps corresponding to phase changes.

The \$995 Peer-2000 occupies a half-slot in a personal computer and adequately tests low-end asynchronous SCSI operation. The board does not include a dedicated capture buffer, and therefore the PC's DMA capability limits the product's abil-

ity to capture data being transferred at fast rates. The Peer-2000 reliably captures data at the 1.25M-byte/sec rate prevalent in many SCSI-peripheral designs.

The \$2995 Peer-3000 and the \$4995 Peer-5000 feature identical analysis capabilities (the higher-priced Peer-5000 includes a µP that improves performance during emu-

#### Don't ignore other tools for SCSI testing

The prolific growth in SCSI usage in the computer industry has spawned a market for various types of specialized test equipment. Tools for debugging SCSI software and firmware designs are by no means the only ones available to aid engineers. Designers can use other test equipment for evaluation and acceptance testing of SCSI peripherals, for factory testing, for evaluating I/O subsystem performance, and for several others.

Numerous companies offer test systems specifically designed to test disk and tape drives, for instance. You'll find test systems capable of testing one drive or capable of simultaneously testing as many as 4000 drives. These types of units satisfy roles such as burn-in and incoming-inspection testing. Companies that offer such products include Adaptec (Milpitas, CA), AVA Instrumentation Inc (Ben Lomand, CA), Brian Instruments Inc (Fullerton, CA), Cambrian Systems Inc (Westlake Village,

CA), Flexstar (Milpitas, CA), I-Tech (Eden Prairie, MN), JCS Technology Inc (Los Gatos, CA), Peer Protocols (Costa Mesa, CA), Santa Cruz Digital (Santa Cruz, CA), and Wilson Laboratories Inc (Orange, CA).

Another company, I/O Xel Inc (Santa Clara, CA), sells disk-drive performance-evaluation tools. The \$1200 SCSI Benchmark, for example, lets you benchmark a disk drive's performance. The company also recently introduced a multiple-drive real-time performance-evaluation tool.

Despite the proliferation of SCSI chips, a few designers may still be forced to build SCSI-compatible interfaces with discrete-logic or semicustom-IC techniques. For these designers, Hewlett-Packard (Palo Alto, CA) offers a SCSI-specific add-on, the Preprocessor Interface Module, for its series of logicanalyzer products.

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lation). The products have 128kbyte RAM buffers and can capture asynchronous bus operations at 4Mbyte/sec rates and synchronous operations at 5M-byte/sec rates. The Model DSC-202 analyzer from Ancot captures bus activity based on signal changes rather than phase changes. For \$5650, you get the basic product capable of captur-

ing 32,000 16-bit events, but no time-stamping capability. The timestamping option costs \$1200 and makes the trace memory 56 bits wide. The analyzer will also capture

State_Analysis_Sample_Printout		11-03-88 22:57:01
RBSAMCIF   DELTA TIME   EXTRN SSETS//F  MM:SS:MILLISEC 43210 TYLNGDOC	C: DATA BUS  RK:P76543210:HEX: PHASE	BUS           ID: NUM  NUM  LINE   CNDTN I T REQS ACKS NUM
00:00:000.0018	00 000000000 000 BUS CLR 00 010000000 080 ARBTRTN 00 010000000 080 SELECT 00 110000001 181 SELECT 00 110000001 181 SELECT 00 110000000 100 COMMAND 11 100000000 100 COMMAND	NORM         10000 0000 0000
	00100000000010001B03 CLK	[NOKH 1 1 [0000100010014]
(a)		
Phase Analysis Sample Printout		11-03-88 22:51:19
	!	1 22 1 22 1
DELTA TIME BUS PHASE	INFORMATION	EXTRN LINE   43210 NUM
100:00:000.0018 BUS FREE 100:00:006.3124  ARBITRATION	100000000 10000000 Device 7 won.	11111 0000    ATN 11111 0001
100:00:000.31241 ARBITRATION	100000000 Device / Won.	the state of the s
100:00:000.3851  COMMAND	100 - Test Unit Ready	11111110003
00:00:000.0296  COMMAND	100 00 00 00 00	11111 0004
100:00:004.70601 STATUS	100 - Good Condition	11111 0005
100:00:000.2608 MESSAGE IN 100:00:000.0253 BUS FREE	100 - Command Complete	
100:00:024.99621 ARBITRATION	110000000 Device 7 won.	ATN   11111   0008
00:00:000.0216  SELECTION	110000001 Initiator 7, Tar	get 0. ATN 11111 0009
100:00:000.3892  COMMAND	25 - Read Capacity	11111 0010
100:00:000.02821 COMMAND	100 00 00 00 00 00 00 00	111111100111
100:00:000.3100  COMMAND 100:00:003.0449  DATA IN	100 100 00 A0 2B 00 00 02 00	11111 0012    11111 0013
100:00:003.04491 DATA IN	100 00 A0 25 00 00 02 00	111111100131
(b)		
(0)		

Sample state- and phase-analysis printouts from the PED-4000 demonstrate the type of analysis SCSI development tools can perform. Transitions in the state of SCSI signals generated the data in the state-analysis printout (a). The phase-analysis report (b) depicts data gathered based on transitions in bus phases.

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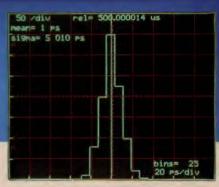
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Analyzer Display or	n X-Y scope
Graphics His	stogram and Strip Chart
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eight external inputs along with the SCSI signals.

The Ancot analyzer offers 50-nsec resolution and can capture asynchronous or synchronous bus operations at speeds of 4.5M bytes/sec. You control the DSC-202 via menus stored in its ROM or with C programs that you can download. EEPROM stores current setup parameters. You can upload, view, or print the analyzed data in a structured Pascal-like format or in either hexadecimal or binary formats.

Pacific Electro Data's PED-4000 Series of analyzers also captures data based on signal state changes. The PED-4001 costs \$3950 and includes the personal-computer addin board and the state-analysis program. The product includes time stamping, provides 100-nsec resolution, includes five external inputs, and has a 2k × 32-bit capture buffer. You can capture asynchronous or synchronous bus activity with the PED-4001, but the resolution limits the capture of data to about 2.5Mbyte/sec transfer rates. The company also offers a \$295 phaseanalysis program, the PED-4002, for the PED-4001.

The PED-4000 Series includes a proprietary procedural programming language that you can use to set up complicated test sequences. The company has also just begun to offer an analyzer product with 50-nsec resolution. The PED-4501 costs \$5950 and includes an  $8k \times 32$ -bit capture buffer. The new product employs a user interface and programming interface similar to the PED-4001.

Although all of these analyzer products offer powerful capabilities, your application may demand a development tool that actively stimulates bus activity along with monitoring it. Adaptec, along with Ancot, Pacific Electro Data, and Peer



An 8k-byte buffer captures SCSI bus activity in the Flexstar bus monitor. The product includes a parallel-printer port, so that you can subsequently print the data.

Protocols, offers a number of development systems that can actively emulate host and peripheral devices.

Adaptec's marketing philosophy, or approach, is different from the other three vendors, however. Adaptec's analyzers are an adjunct to its active-emulation development systems, which Adaptec considers the basic tools for testing and debugging. Ancot's, Pacific Electro Data's, and Peer Protocols' active-emulation products are software options to the previously described analyzers that the three companies sell.

Both initiator and target emulation packages are available. In real-world applications, a host computer is typically an initiator and a peripheral is typically a target. The SCSI spec, however, allows any device to initiate bus activity and any device to respond.

The emulation products from all four companies include a similar set of features. The initiator emulators include a library of test routines typical of host activity or communication with peripherals such as disk and tape drives. You can control the

emulation via menus. You can also use the menus to develop new tests based on routines in the library or on routines you define at the SCSI command level. In fact, the menus allow you to set up tests representative of virtually any SCSI environment.

You can also use programming languages to control the emulation. Adaptec, Ancot, and Peer Protocols offer C; Pacific Electro Data provides a proprietary procedural language. During software testing, you will find that the menus offer the flexibility to quickly change emulation parameters and to create new tests. The programming languages ultimately offer more flexibility, however, and can also be useful to set up standard test sequences for testing or evaluating peripherals.

The target emulation packages operate in the same manner as the initiator emulation products. However, they include libraries that simulate disk or tape drives, and you can use the menu interface to develop emulations of virtually any peripheral. In addition, you can use the programming languages to set

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up emulations.

The initiator and target emulators provide a vehicle to simulate a working product and test your design in the early debugging stages. The emulators also allow you to fully test your finished product. For example, you can have a target emulator generate selective busparity errors and ensure that your host software handles those errors properly. In fact, the ability of the emulators-both initiators and targets-to generate improper conditions is of more importance than the simulation of working products in many testing applications.

Ancot's active-emulation package includes target and initiator and costs \$3100. The product supports asynchronous data transfers of 1.5M bytes/sec. The menus allow you to select from standard test routines stored in EPROM. You can store test routines that you design in EEPROM, too.

Peer Protocols sells its initiator and target emulation packages separately. Each program costs \$500 and will work with any of the company's analyzer boards. The Peer-5000 includes a local μP and doesn't require host intervention to execute an emulation; the product can therefore simulate the operation of fast peripherals with little SCSI command overhead.

To add initiator and target emulation to Pacific Electro Data's PED-4001, you have to pay \$795 for each capability. The PED-4001 can transfer data asynchronously at 1.5M bytes/sec. The company currently doesn't offer an emulation package for the PED-4501, but it expects to introduce one during the first quarter of 1989. The product will include a second add-in board and software.

Adaptec's line of SCSI development tools are the most extensive of any of the manufacturers—in-

```
Function Pick Window——ELEMENT PICK—
readcap (0,0x00000000,0)
readr (0x0000,0x0000)
reset ()
-> seek (0x0000)
sense (0x0000)
testur ()
,End,PqDn,; Enter,Esc,a..z,^Group

Test Sequence Edit ——INSERT MODE—
begin {
reset ()
readcap (0,0x00000000,0)
}
end
```

Tools such as the SCSI Program Generator from Adaptec provide easy program creation and execution by allowing you to pick from a list of more than 300 test functions. The program then places these functions into an executable test program.

cluding analyzer and active-emulation products. You can choose from the \$10,500 SDS-1, \$14,500 SDS-2, or \$18,500 SDS-3 system. All of the products require a host IBM-compatible personal computer; as an option, Adaptec offers the products bundled with Compaq and Wyse computers.

The SDS-1 offers target emulation only and supports asynchronous data transfers. The SDS-2 and SDS-3 include both initiator and target emulation. The former can only handle 1.8M-byte/sec asynchronous data transfers, whereas the latter can transfer data either in asynchronous (1.8M bytes/sec) or synchronous (5M bytes/sec) modes.

The \$4950 SDS-210 analyzer board is an accessory for the SDS-1 or the SDS-2; the SDS-3 accepts the

#### For more information . . .

For more information on the SCSI test and development products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

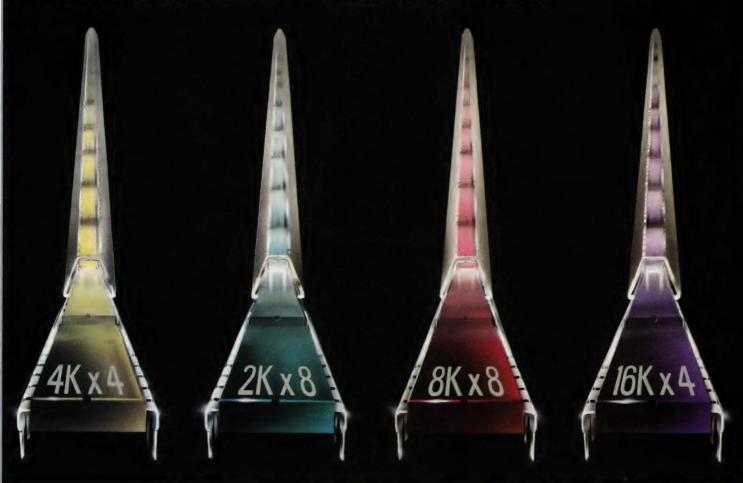
Adaptec Inc 691 S Milpitas Blvd Milpitas, CA 95035 (408) 945-8600 FAX 408-262-1845 TWX 910-338-0060 Circle No 351

Ancot Corp 1755 E Bayshore Rd, Suite 18A Redwood City, CA 94063 (415) 363-0667 FAX 415-363-0735 Circle No 352 Flexstar Corp 606 Valley Way Milpitas, CA 93035 (408) 946-1445 Circle No 353

Pacific Electro Data Inc 14 Hughes, Suite B205 Irvine, CA 92718 (714) 770-3244 Circle No 354 Peer Protocols Inc 3176 Pullman, Suite 101 Costa Mesa, CA 92626 (714) 662-1929 FAX 714-662-1437 Circle No 355

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P4C1981	16K x 4	15ns	NOW
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#### UPDATE

\$4950 SDS-310 analyzer. All of these analyzers can capture 64k bytes of data and include a set of features similar to the products from Ancot, Pacific Electro Data, and Peer Protocols. The SDS-3 system also includes support for SCSI-2 features such as command queueing. Another key feature of the SDS-3 is its menu-driven Program Generator for developing test programs.

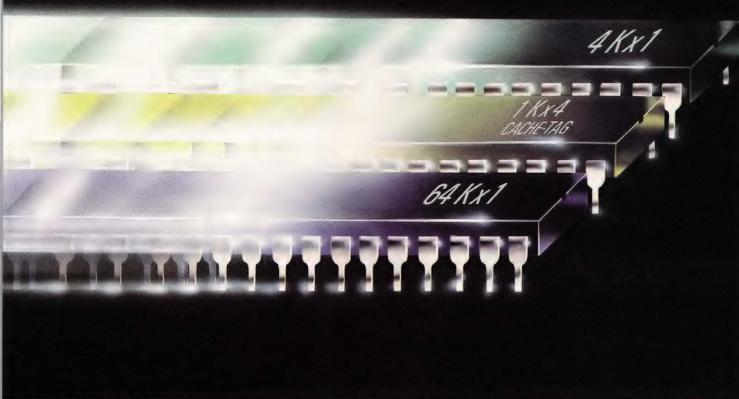
The Adaptec products also all include capability for testing differential SCSI operation, in addition to being able to test the more popular single-ended operation. SCSI specifies a choice of single-ended or differential bus transceivers. Even though the other products don't include this capability, you can buy single-ended-to-differential converters, which typically cost \$200 to \$500, so that you can attain this capability.

Adaptec's prices also include two days of training (in Adaptec's facility) in the use of its SCSI development tools. As more designers address SCSI for the first time, this type of training will certainly ease the learning process. Peer Protocols has also perceived a need for customer training, and the company offers a 2-day training class (for as many as three people) for \$1200.

EDN

Article Interest Quotient (Circle One) High 509 Medium 510 Low 511

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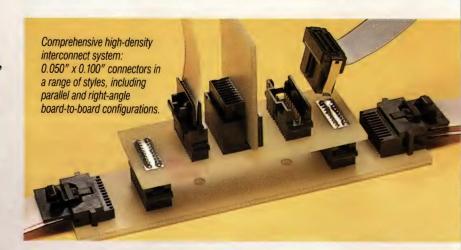
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**Interconnecting ideas** 



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grammable Logic Devices (PLDs) because it com-bines the high performance levels expected by users of today's PLDs with substantially greater equivalent logic densities and previously available. The PLHS50 is a flexible, high-density high-speed can backet" that previously available, a high-nin-

The PLH530/18 a next be, figure density, figure-speed.

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	2000 to 000 to 0	Series Comparison.
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Buffer Size (bytes)	64K	16K
Buffer Management	DisCache®	None
Transfer Rate (MB/sec)		
AT-Bus	4	4
SCSI Sync	4	_
SCSI Async	2	2
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<sup>\*</sup>These are the best individual specifications of competitive drives. (This is not a real product.)

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**CIRCLE NO 81** 

<sup>\*\*</sup>Average seek time with DisCache is 12 ms in typical applications.
(All specifications subject to change.)



### 8-bit microcontroller incorporates a slew of peripheral functions

If your embedded-control applications require speed and a host of functions, consider the H8/532. This 8-bit microcontroller is packed with more than 25 built-in analog and digital peripheral functions. The internal structure and the memory capacity enable the device to support high-level languages.

The device is built around a CPU with a dual ALU structure. The 16-bit-wide internal data path enables the CPU to operate at 10 MHz and to execute most instructions in 200 to 400 nsec. It can multiply two 16-bit values in 2.3 μsec and divide a 32-bit value in 2.6 μsec.

The H8/532 provides plenty of memory space—32k bytes of EPROM for program storage and 1k byte of RAM. It allows you to access external memory either with or in place of the internal memory. You have a choice of five operating modes, which you specify during reset. You can use the internal memory, the internal and the 64k-byte or 1M-byte external memory, or either of the external memory capacities.

A 10-bit A/D converter, an 8-input multiplexer, and four 16-bit registers that buffer the data are also included. The built-in converter has its own sample and hold circuit and offers a 13.8-µsec conversion time. You can use the A/D converter to dwell on a single channel or to automatically scan through as many as four channels. When the data is ready, the A/D converter generates an interrupt to the CPU.

The H8/532 also provides a number of digital data paths, including a serial-communications interface (with a baud-rate generator) and nine I/O ports. The serial interface



This 8-bit microcontroller features a number of onboard peripherals, including an 8-channel A/D converter, several timers, serial and parallel I/O ports, and programmable memory.

handles either synchronous or asynchronous communications at a data rate of 2.5M bits/sec max. The I/O ports include 57 bidirectional lines and eight input-only lines.

The interrupt, wait-state, and data-transfer controllers simplify program control. The interrupt controller handles three external and 19 internal interrupt sources. You can assign each interrupt to one of eight priority levels. The wait-state controller simplifies the use of slow memory and peripherals by letting you delay the CPU's operation under either software or external control. Further, the data-transfer controller frees the CPU from the task of moving data between memory and I/O ports.

A variety of timing functions are available with the H8/532. Three free-running 16-bit timers let you generate output waveforms or measure incoming waveforms. Ad-

ditionally, you can select an 8-bit general-purpose timer, a watchdog timer, and three PWM timers with 0.4% resolution.

The H8/532 is available in windowed-EPROM and one-time-programmable versions, and it comes in either an 84-pin plastic leaded chip carrier or an 80-pin quad flat pack. It costs \$59 (100). Samples are currently available; full production is scheduled for March 1989.

—Richard A Quinnell Hitachi America, Ltd. 2210 O'Toole Ave, San Jose, CA 95131. Phone (408) 435-8300.

Circle No 729

### Digital-signal-processing workstation performs algorithmic verification

The Signal Processing WorkSystem (SPW) does for signal-processing design what schematic capture did for logic design. Starting from software descriptions of primitives, you can interactively capture DSP system algorithms. You can then apply stimuli to your algorithm's inputs and tweak the system to verify and optimize performance.

The menu-driven SPW features a Block Diagram Editor (BDE) that supports hierarchical design. You use the BDE to focus on DSP algorithmic design. Because the editor has revision control and offers transparent location and relocation of design data on a network of workstations, you can partition the design effort among a team of engineers.

The components you use to construct and simulate a DSP system come from the Function Block Library (FBL). The library contains about 100 software-coded function blocks. If you need a function that doesn't exist in the library, you can write source code in C or in Fortran and create a custom block. While the simulation is running, FBL lets you view signals, modify simulation parameters, and observe the results.

The Simulation Program Builder takes the signal-flow block diagram from the BDE and converts it into a program that simulates the signal-flow behavior of an entire DSP system. Your design can incorporate multiloop, nested, and hierarchical feedback paths.

The Signal Display Editor creates, edits, displays, and analyzes signals within your DSP system. The editor's interactive commands let you cut and paste signals, thereby decreasing the the amount of time you devote to signal construction and analysis.

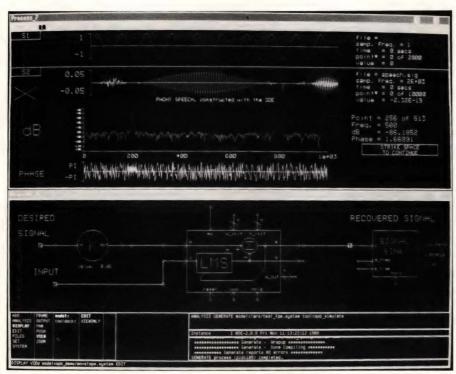
Because the library elements are software-coded functional models, designing and verifying an algorithmic DSP system doesn't guarantee that you can actually build the hardware. However, algorithmic development is a significant portion of DSP design, and the vendor is developing library elements that have hardware equivalents.

The Signal Processing Workstation costs \$25,000 and runs on both DEC VAXstation 3000 and Apollo DN3000/4000 workstations. The SPW will be available on the Sun 3 in the second quarter of 1989.

-Michael C Markowitz

Comdisco Inc, 101 California St, 38th Floor, San Francisco, CA 94111. Phone (415) 421-1800.

Circle No 675



The Block Diagram Editor lets you design a digital-signal-processing workstation such as this LMS adaptive-filter noise canceller (bottom); the Signal Processing WorkSystem's Signal Display Editor (top) displays the signals.

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# Macintosh-based logic analyzer samples at 1 GHz and can expand to 384 channels

Last October, when EDN published a special report on PC-based logic analyzers (October 13, 1988, pg 134), there were no products based on Apple Computer Inc's Macintosh family. Now there is one, and it's a lot more than just another logic analyzer based on a personal computer. The CLAS 4000 configurable logic-analysis system can have as many as 384 channels and can acquire data at 1 GHz on as many as 64 channels. Heretofore, PC-based logic analyzers were limited to 320 channels and could acquire data at a maximum of 500 MHz-except when using equivalent-time sampling, which is valid only with repetitive signals.

The base model of the CLAS 4000 system includes a Macintosh SE, and the higher-performance version includes a Mac II with a 13-in. color monitor. The logic analyzer and the Mac communicate via the computer's SCSI bus, allowing you to configure systems with several logic-analyzer mainframes. When you order one mainframe, the vendor supplies a Mac with 2M bytes of RAM and a 20M-byte hard disk. Systems with multiple mainframes run under Apple's Multi-Finder operating system; they have more RAM and a larger hard disk. Although Multi-Finder is not a true multitasking OS, the intelligence in the analyzer mainframes allows each mainframe in a multiple-mainframe configuration to operate unimpeded.

Using several mainframes is one approach to debugging multiprocessor systems, but with the CLAS 4000 it is not the only method. Each mainframe accommodates from one to four logic-analyzer modules. Currently, there are two varieties of



Incorporating a Macintosh II or Macintosh SE, Gould's CLAS 4000 provides performance and ease-of-use features heretofore unavailable in PC-based logic analyzers.

modules: a 200-MHz unit that accepts 96 inputs when operating at 50 MHz and a 1-GHz unit with two levels of Trace Control and event recognition. The 1-GHz module handles 16 channels. You can use the modules as several independent but closely coupled instruments or, with the help of software, configure them as a single analyzer. Both types of modules time-stamp data to correlate information acquired by different modules.

The 200-MHz module, which the vendor calls the "pyramid" unit, operates in both state- and timinganalysis modes. It also offers a mode that automatically captures data before and after the inputs satisfy the trigger conditions. Additionally, you don't have to move probes to continue viewing the activity on selected signal lines as the module achieves sampling rates beyond 50 MHz by multiplexing channels. Instead, the supplied software lets you specify which channels you want to view, and relays within the analyzer module disconnect the signals that you are willing to forego viewing.

The relay-switching capability also lets you use a single set of

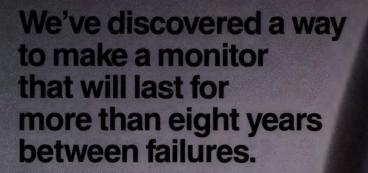
probes with a pair of analyzer modules to simultaneously acquire state and timing information. Moreover, any group of eight or fewer channels can act as the external clock input to one or several analyzer modules.

The system conforms to Macintosh human-interface guidelines. It lets you manipulate graphics symbols to control complex functions such as probe reassignment, triggering, and external clocking. You can simultaneously display as many as 16 windows that contain such information as the system configuration, status, and time-correlated data. Because the software uses color sparingly, systems based on a Macintosh SE, which has a monochrome display, can perform the full range of functions.

Prices for the CLAS 4000 system with a single analyzer mainframe and a computer range from \$19,950 to \$50,270. Delivery is 90 days ARO. The vendor also offers disassemblers and pods for popular µPs.—Dan Strassberg

Gould Inc, 19050 Pruneridge Ave, Cupertino, CA 95014. (800) 538-9320. TWX 910-338-0509.

Circle No 419



The real challenge is to keep it busy for that long.

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# Real-time operating system assists in development of DSP-chip applications

The powerful 32-bit DSP chips that are now available can accomplish tasks that used to require both a DSP chip and a host  $\mu P$ . In the past, the task was partitioned so that the DSP chip handled the math-intensive operations, and the μP did everything else. Although the DSP chips were very fast at math functions, they were awkward to use in general-purpose applications. The new wave of 32-bit DSP chips, however, are beginning to look like very capable generalpurpose 32-bit µPs. The Texas Instruments' TMS320C30, for example, has enough flexibility and power to take on many applications without a host µP, and you can now use these new 32-bit DSP chips for an entire task.

SPOX, a real-time operating system/development environment for the TMS320C30, is available to assist you in the development of these applications. As a real-time operating system, SPOX provides a kernel that contains the executive and

modules for memory management, stream I/O, and DSP math functions

The kernel performs the task handling, scheduling, and message passing; consumes only 2k words of memory; and can switch a task in only 10 µsec. The stream I/O module provides real-time device-independent stream I/O to ease the acquisition of data. The kernel, memory-management module, and stream I/O module can all fit within the internal 4k-word memory on the TMS320C30.

SPOX also includes various math functions and the hooks that allow any C program to use these functions. These math functions also allow you to easily perform most common DSP applications.

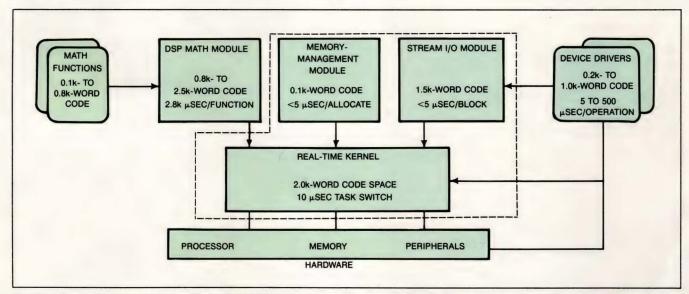
As a development environment, SPOX interacts with a host computer. You can write your algorithms in C, then test them on the host computer. You can use this same code to create the application code for testing on the host com-

puter, using a simulator that also simulates the operation of SPOX to verify timing and memory requirements. Once the code has been proven with the simulator, you can then test it in the target environment.

You can run SPOX in a C environment on an IBM PC or on a Sun workstation to develop and evaluate your application code. The IBM PC version costs \$1000, and the Sun workstation version sells for \$2000. It's also available bundled with the Texas Instruments XDS development system where you can run your application, using native code in real time. The development system is priced at \$16,000 with no additional costs. Later in 1989, SPOX will be available as a linkable library for production use at a negotiable price.—David Shear

Spectron Microsystems Inc, 600 Ward Rd, Suite B-2, Santa Barbara, CA 93111. Phone (805) 967-0503

Circle No 732



The SPOX real-time operating system for the TMS320C30 includes modules for memory management, DSP math, and stream I/O. The development environment included with SPOX permits simulation and time/space analysis from the beginning of the project and allows much of your code to be reusable.



# 16-bit MICROPROCESSOR



# 16-bit Performance Boost for 6502 Designs

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# PRODUCT UPDATE

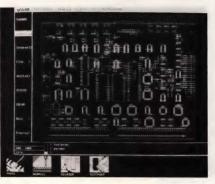
# Analyzer package features test-fixture accessibility

The DFA (design for accessibility) Analyzer is a member of the Testbridge family of design-for-test products, running in the vendor's Allegro pc-board design system. The analyzer allows you to incorporate access for automatic-testequipment (ATE) test fixtures when you place and route components on your board.

Using the DFA Analyzer, you can evaluate the accessibility of signals on boards with fine-line technology, including micro vias and blind/buried vias. You also have the option of examining for accessibility those boards with surface-mount devices on both sides, for either clamshell-type fixtures or for fixtures that probe only one side of the pc board.

The analyzer lets you automatically identify existing via holes and pads that meet test-fixture requirements. If your text fixture uses test-probe nails in a 100-mil grid pattern, the software will limit test points to only those locations where the fixture has probes. In addition, the software inserts test points on the proper grid for those nets on the board that don't have a readily accessible test location. You have the option of introducing test rules that guide the selection and insertion process via an accessibility rules form, or you can use the vendor's default rules.

The numerically controlled (NC) drill-hole marking feature of the DFA Analyzer generates NC drill and route tapes of test-point locations to physically drive the equipment that produces custom test fixtures. Further, the software generates the pc-board documentation that uses the design database, re-



The DFA Analyzer automatically selects existing test points that meet selection criteria. An automatic insertion routine adds additional test points for complete accessibility, and it adds net-name cross-references and target figures for document generation.

duces transcription errors, and provides revision control.

The DFA Analyzer runs on Sun 3 and 4 workstations and DEC VAX-stations. Prices for Allegro start at \$20,000.

#### -Michael C Markowitz

Valid Logic Systems, 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 432-9400.

Circle No 731





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Like Compaq's.

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## And If That Sounds Fast, Wait Till You See Our New 25 MHz 386-Based System.

At 25 MHz, our new System 325 offers you the highest possible performance in a 386.

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But speed isn't the only reason to buy from Dell. Or even the best.



#### THE DELL 25 MHz 386 System 325.

STANDARD FEATURES: \* Intel® 80386 microprocessor running at 25 MHz. \* 1 MB of RAM\* expandable to 16 MB using a dedicated high speed 32-bit memory slot. \* Advanced Intel® 2385 Cache Memory Controller with 32 KB of high speed static RAM cache. \* Page mode interleaved memory architecture. \* VGA systems include a high performance 16-bit video adapter. \* Socket for 25 MHz Intel® 80387 or 25 MHz. WEITEK 3167 math coprocessor. \* 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive. \* Enhanced 101-key keyboard. \* 1 parallel and 2 serial ports. \* 200-watt power supply. \* 8 industry standard expansion slots.

**Lease for as low as \$252/Month. The Dell System 325 is an FCC Class A device, intend- ed for business use only.	System 325	WITH MONITOR & ADAPTER			
	Hard Disk Drives	VGA Mono	VGA Color Plus		
	150 MB-18 ms ESDI 322 MB-18 ms ESDI	\$6,999 \$8,999	\$7,299 \$9,299		

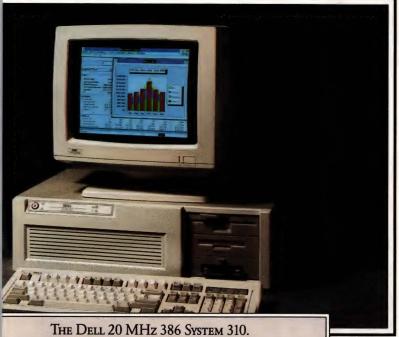
System 325 and 310 Options: • Intel 80387 math coprocessor: 25 MHz for 325; 20 MHz for 310. • 1 MB or 4 MB memory upgrade kit. • 2 MB or 8 MB memory expansion board kit. • Dell Enhanced Microsoft\* MS-DOS \* 3.3. • Dell Enhanced Microsoft MS-DOS 4.0. • Both

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Lease for as low as	System 310	WITH MONITOR & ADAPTER			
48/Month.	Hard Disk Drives	VGA Mono	VGA Color Plus		
	40 MB-28 ms	\$4,099	\$4,399		
	90MB-18ms ESDI	\$4,899	\$5,199		
	150MB-18ms ESDI	\$5,399	\$5,699		
	322 MB-18 ms ESDI	\$7,399	\$7,699		

S-DOS versions with disk cache and other utilities. \* Dell Enhanced MS\* OS/2. \*640 KB is ailable for programs and data. The remaining 384 KB is reserved for use by the system to enhance

ness needs, we will help you select the features that are right

for you. After your system unit is custom built, we burn-in everything to make sure the entire system works perfectly.



# READERS' CHOICE

Of all the new products covered in EDN's August 18, 1988, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our August 18, 1988, issue.

## SOFTWARE PACKAGE

Combining communications and software development, the Unibridge package links Unix host systems to OS-9-based real-time target systems (pg 107).

Microware Systems Corp.

Circle No 601

#### DISK DRIVE

The Model I325 Floptical disk drive is a removable-disk storage system in a  $3\frac{1}{2}$ -in. format that provides 25M bytes of unformatted disk capacity and 20.8M bytes of formatted memory (pg 117).

Insite Peripherals.

Circle No 602

### **INDUCTORS**

Model 8RBC fixed inductors are designed for noise-filtering and trapping applications (pg 240).

Toko America Inc.

Circle No 603

#### 16-BIT AUDIO ADC

The PCM78P 16-bit successive-approximation A/D converter has a typical total-harmonic-distortion-plusnoise (THD+N) spec of -88 dB (-82 dB max) at full scale (pg 258).

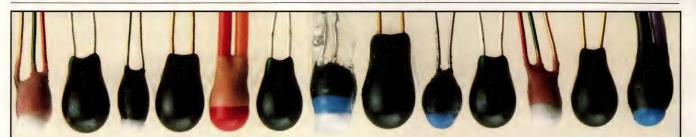
Burr-Brown Corp. Circle No 604

### FFT ANALYZERS

The battery-powered PL21 single-channel and PL22 dual-channel FFT analyzers are suitable for a variety of field and lab test applications in mechanical, structural, acoustic, and electrical engineering (pg 274).

Diagnostic Instruments Ltd.

Circle No 605



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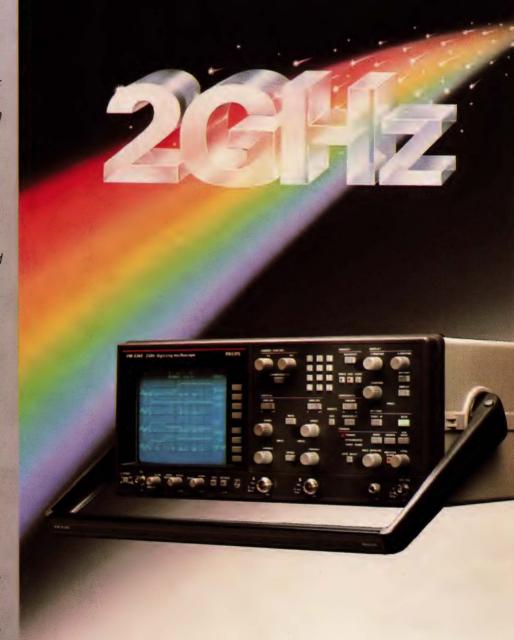
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publication.



From the staff of EDN

EDN January 5, 1989

# LEADTIME INDEX

						Per	centa	ige o	f respondents
							Last month		
							Ta		
c c	A the shell		,	12	Que		OTH		
	1	6.1	1	2 3	3	9	-E	ň .co.	
	65.	40	4	Ze ·	4	4	Wets &	o et	
ITEM	Tell	eks	ex.	,eks	eks	eks	ekside ekside	S.C.	ITEM
TRANSFORMERS			ų.			_	1		Dry reed
Toroidal	7	15	64	14	0	0	7.7	8.2	Mercury
Pot-Core	8	15	46	31	0	0	8.9	11.5	Solid state
Laminate (power)	10	50	25	15	0	0	5.8	8.5	DISCRETE SEMICON
CONNECTORS	10	-					0.0		Diode
Military panel	0	44	33	23	0	0	7.5	9.6	Zener
Flat/Cable	25	45	20	10	0	0	4.4	4.2	Thyristor
Multi-pin circular	14	36	36	14	0	0	6.1	9.7	Small signal transisto
PC (2-piece)	21	43	29	7	0	0	4.6	7.3	MOSFET
RF/Coaxial	18	58	18	6	0	0	4.1	7.4	Power, bipolar
Socket	15	60	20	5	0	0	4.1	3.8	INTEGRATED CIRCU
Terminal blocks	29	47	18	6	0	0	3.7	4.8	Advanced CMOS
Edge card	13	33	47	7	0	0	5.8	5.9	CMOS
D-Subminiature	27	36	27	10	0	0	4.7	4.1	TTL
Rack & panel	15	46	31	8	0	0	5.1	8.1	LS
Power	13	40	27	13	7	0	7.1	6.0	INTEGRATED CIRCU
PRINTED CIRCUIT BOAR	DS								Communication/Circu
Single sided	0	65	35	0	0	0	4.7	5.3	OP amplifier
Double sided	0	59	36	5	0	0	5.4	6.2	Voltage regulator
Multi-layer	0	26	63	6	5	0	8.0	6.8	MEMORY CIRCUITS
Prototype	0	87	9	4	0	0	3.9	3.4	DRAM 16K
RESISTORS									DRAM 64K
Carbon film	24	37	29	10	0	0	4.9	3.4	DRAM 256K
Carbon composition	32	36	32	0	0	0	3.6	3.8	DRAM 1M-bit
Metal film	19	48	33	0	0	0	4.0	4.1	SRAM 4K × 8
Metal oxide	23	39	38	0	0	0	4.2	4.9	SRAM 8K × 8
Wirewound	35	24	35	6	0	0	4.4	5.2	SRAM 2K × 8
Potentiometers	13	50	33	4	0	0	4.7	5.2	ROM/PROM
Networks	21	47	26	6	0	0	4.4	4.3	EPROM 64K
FUSES	56	27	11	6	0	0	2.6	2.2	EPROM 256K
SWITCHES									EPROM 1M-bit
Pushbutton	22	39	30	9	0	0	4.9	4.5	EEPROM 16K
Rotary	6	53	29	12	0	0	5.7	7.8	EEPROM 64K
Rocker	21	32	36	11	0	0	5.5	5.8	DISPLAYS
Thumbwheel	0	56	31	13	0	0	6.1	9.0	Panel meters
Snap action	7	29	57	7	0	0	6.5	7.3	Fluorescent
Momentary	14	43	36	7	0	0	5.2	5.7	CRT 12-inch monoch
Dual-in-line	14	50	29	7	0	0	4.9	6.2	LED
WIRE AND CABLE									Liquid crystal
Coaxial	29	47	19	5	0	0	3.7	4.0	MICROPROCESSOR
Flat ribbon	35	43	22	0	0	0	3.0	3.3	8-bit
Multiconductor	41	27	27	5	0	0	3.7	4.3	16-bit
Hookup	50	31	19	0	0	0	2.4	3.0	32-bit
Wirewrap	38	31	31	0	0	0	3.4	3.7	<b>FUNCTION PACKAG</b>
Power cords	38	29	25	8	0	0	4.1	4.2	Amplifier
POWER SUPPLIES									Converter, analog to
Switcher	8	30	31	31	0	0	8.1	8.6	Converter, digital to a
Linear	7	27	39	27	0	0	8.1	6.1	LINE FILTERS
CIRCUIT BREAKERS	23	38	23	16	0	0	5.4	7.9	CAPACITORS
HEAT SINKS	24	46	24	6	0	0	4.2	4.5	Ceramic monolithic
BATTERIES									Ceramic disc
Lithium coin cells	15	38	38	9	0	0	5.5	7.0	Film
9V alkaline	40	40	20	0	0	0	2.8	3.4	Aluminum electrolytic
Real-time clock back-up	30	40	30	0	0	0	3.6	7.4	Tantalum
RELAYS		,5		-	-	-	0.0		INDUCTORS
General purpose	43	28	19	10	0	0	3.9	6.6	
PC board	30	45	5	20	0	0	4.8	7.3	Course Flacture
	-	10	-	20		0	0		Source: Electror

	Off the shell			Over 30 weeks  11-20 weeks  9 27 0 0			month's liverage		
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ITEM	Jel .	eks	eks	eks	eks !	e Ks	CKS CO	Se Co	
Dry reed	0	64	9	27	0	0	6.8	7.2	
Mercury	14	57	0	15	14	0	7.6	7.5	
Solid state	39	38	6	17	0	0	4.2	7.1	
DISCRETE SEMICONDUCTO	ORS								
Diode	42	23	19	16	0	0	4.6	5.2	
Zener	36	28	16	20	0	0	5.2	5.6	
Thyristor	19	37	19	25	0	0	6.5	8.0	
Small signal transistor	26	42	16	16	0	0	5.0	4.3	
MOSFET	14	43	14	29	0	0	6.9	7.6	
Power, bipolar	33	42	8	17	0	0	4.5	6.1	
INTEGRATED CIRCUITS, D	IGITA	L							
Advanced CMOS	15	35	35	15	0	0	6.1	7.0	
CMOS	33	33	25	9	0	0	4.3	5.4	
TTL	52	22	13	13	0	0	3.7	4.3	
LS	52	24	14	10	0	0	3.3	4.6	
INTEGRATED CIRCUITS, L			-						
Communication/Circuit	29	36	21	14	0	0	4.9	6.8	
OP amplifier	29	29	29	13	0	0	5.2	6.0	
Voltage regulator	40	35	10	15	0	0	4.1	5.8	
MEMORY CIRCUITS									
DRAM 16K	22	44	0	22	12	0	7.7	15.0	
DRAM 64K	11	56	0	22	11	0	7.8	13.1	
DRAM 256K	8	25	17	33	17	0	11.5	15.1	
DRAM 1M-bit	0	20	40	30	0	10	11.5	18.9	
SRAM 4K × 8	0	13	25	62	0	0	11.9	10.6	
SRAM 8K × 8	6	12	12	46	12	12	15.2	14.3	
SRAM 2K × 8	14	15	14	57	0	0	10.4	13.1	
ROM/PROM	8	50	9	33	0	0	7.3	9.1	
EPROM 64K	29	7	35	29	0	0	7.5	7.1	
EPROM 256K	25	9	33	33	0	0	8.0	8.5	
EPROM 1M-bit	0	38	13	49	0	0	9.7	10.9	
EEPROM 16K	10	20	20	50	0	0	9.9	9.7	
EEPROM 64K	18	27	19	36	0	0	7.9	10.9	
DISPLAYS					THE REAL PROPERTY.		PE		
Panel meters	20	27	33	13	7	0	7.2	8.8	
Fluorescent	11	23	33	33	0	0	8.4	10.0	
CRT 12-inch monochrome	8	42	17	33	0	0	7.7	7.3	
LED	37	31	16	16	0	0	4.6	6.8	
Liquid crystal	8	23	38	31	0	0	8.5	7.2	
MICROPROCESSOR ICs	40	0.4	40	40	To see	•			
8-bit	13	31	13	43	0	0	8.6	5.6	
16-bit	0	40	20	40	0	0	8.9	6.6	
32-bit	11	23	22	44	0	0	9.2	10.3	
FUNCTION PACKAGES	00	40	00						
Amplifier	23	16	38	23	0	0	7.0	6.0	
Converter, analog to digital	7	14	43	36	0	0	9.4	6.7	
Converter, digital to analog		17	42	33	0	0	8.9	6.8	
LINE FILTERS	25	13	25	37	0	0	8.1	5.4	
CAPACITORS									
Ceramic monolithic	32	31	23	14	0	0	4.9	5.2	
Ceramic disc	36	19	27	18	0	0	5.5	5.8	
Film	30	30	20	20	0	0	5.5	5.8	
Aluminum electrolytic	28	32	24	16	0	0	5.3	7.3	
Tantalum	31	31	19	19	0	0	5.3	5.5	
INDUCTORS	0	43	44	13	0	0	6.8	9.0	

Source: Electronics Purchasing Magazine's survey of buyers.

# Let's compare automated audio test equipment performance:

	KEY PERFORMANCE SPECS	AUDIO PRECISION SYSTEM ONE	H-P 8903B	S-T 3100/3200	TEK AA5001/SG5010		
	Flatness 20-20kHz, gen/analyzer	0.03/0.03 dB	0.06/0.2 dB <sup>1</sup>	0.1/0.1 dB	0.05/0.1 dB		
	Amplitude accuracy, gen/analyzer	0.1/0.1 dB	0.2/0.2 dB	0.2 dB/no spec	0.2/0.3 dB		
	Generator amplitude range	+30 to -90 dBm	+17 to -68 dBm	+30.6 to -90 dBm	+28 to -72 dBm		
	System THD + N 20-20kHz, 80 k BW	0.0015%	0.01%	0.0018%2	0.0032%		
	Min. amplitude for THD + N function	25 microvolts	50 millivolts	30 millivolts	60 millivolts		
	Residual noise (80 kHz BW)	3.0 μV	15 μV	4.0 μV	3.0 μV		
	Analyzer stereo separation @ 20 kHz	140 dB	function not avail.	100 dB	function not avail.		
	Common mode rejection ratio	70 dB, 50-20kHz	60 dB, 20-1kHz	100 dB @ 60 Hz	50 dB, @ 50/60 Hz		
	Speed, THD function (autorange)	10 sec 16-pt sweep	1.5 sec to 1st rdng	2.5 sec to 1st rdng	2.5 sec to 1st rdng		
	Speed, amplitude function (autorange)	10 sec 30-pt sweep	1.5 sec to 1st rdng	1.3 sec to 1st rdng	2.0 sec to 1st rdng		
		(2 chan simultaneous)	(1 channel)	(per channel)	(1 channel)		
Ī	PRICE (U.S. DOMESTIC)						
	Computer-interfaceable instrument Software package Typical controller	\$6950 included \$600-\$3000 <sup>3</sup>	\$5800 none available \$5750 <sup>4</sup>	\$9985 \$575-\$1220 \$1000-\$3400 <sup>5</sup>	total system \$16490 <sup>6</sup>		

Analyzer flatness not specified separately; analyzer accuracy 0.2 dB 20 Hz-20 kHz <sup>2</sup> Total system THD + N not specified; generator THD plus analyzer distortion specs added together equal 0.0018%

<sup>3</sup> Personal computer. Interface card included in instrument price.

<sup>4</sup> H-P Model 310M IEEE-488 compatible

<sup>5</sup> Personal computer plus IEEE-488 interface card

<sup>6</sup> Total of instruments, software, Tek 4041/4205 IEEE-488 controller

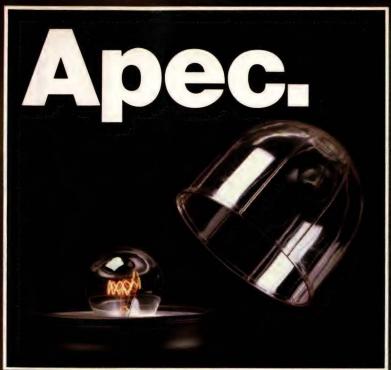
Competitive data compiled from H-P 1988 catalog, S-T data sheet 3000A 1987, Tektronix 1988 catalog

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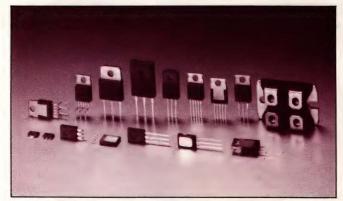
# Power MOSFETs & CIGBTs

Your choice of a switching element in highcurrent applications depends on the required speed and switching efficiency, cost factors, and volumetric considerations. The increasing diversity and steadily improving performance of available power MOSFETs and IGBTs are making them the switching devices of choice in many applications.

Bill Travis, Contributing Editor

he quest for the perfect switch proceeds relentlessly. This switch will have zero on-resistance and infinite off-resistance, and will require no activation power. Further, the switch will commutate instantaneously and will be capable of switching at an infinite repetition rate. Electromechanical switches, of course, provide the closest approximation to the ideal on-and off-resistances. For fast switching speeds and high reprates, though, you're obliged to use a solid-state solution—thyristors, bipolar transistors, MOSFETs, or IGBTs (insulated-gate bipolar transistors). MOSFETs and IGBTs are rapidly supplanting thyristors and bipolar transistors in fast-switching applications.

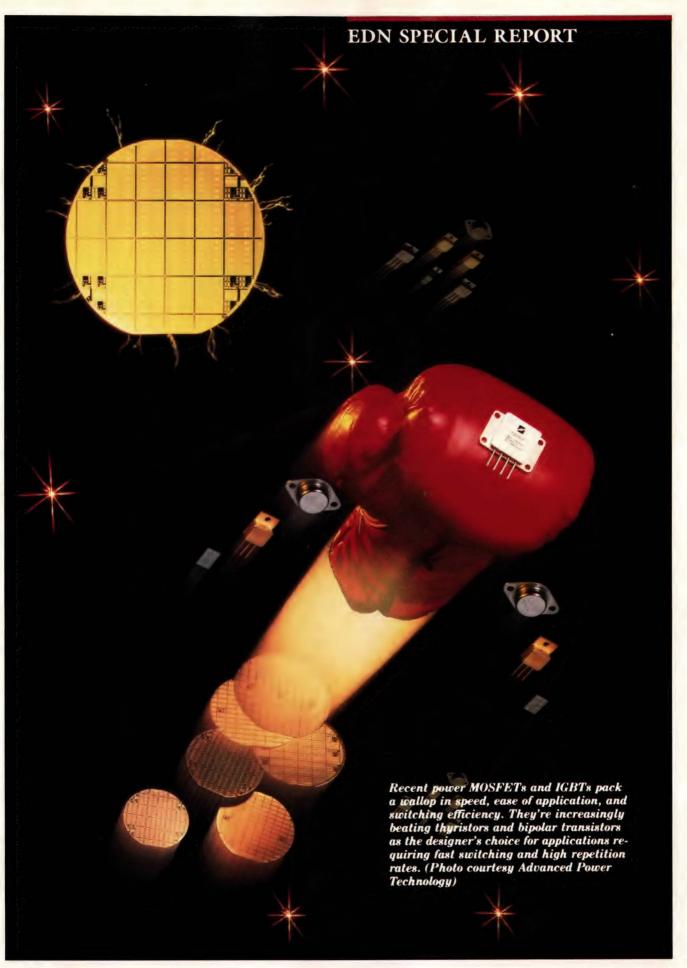
High speed, ease of application, and switching efficiency are three of the factors that endear power MOSFETs and IGBTs to designers. Further, the steadily growing number of MOSFET suppliers is nurturing keen competition, in both price and performance. As a result, the once-significant cost advantage that bipolar transistors have traditionally had over MOSFETs is dwindling. Speaking of cost, you must consider total system cost when you're choosing a switching device. In many cases, the less-complex drive circuitry needed to control a MOSFET (compared



Plastic power packages from Philips-Amperex come in a variety of sizes and styles to suit the application.

with that needed to control a bipolar device) more than offsets the MOSFET's higher purchase price.

Denser geometries, processing innovations, and packaging improvements are resulting in power MOSFETs that have ever-higher voltage ratings and current-handling capabilities, as well as volumetric power-handling efficiency. The same holds true for IGBTs. In addition to making steady improvements in voltage and current ratings, manufacturers are add-



# MOSFETs and IGBTs are rapidly supplanting thyristors and bipolar transistors in fast-switching applications.

ing various features that bear on the devices' survivability, ease of use, and—in some cases—their "smartness" (for example, overtemperature protection). Before considering these peripheral improvements, it's useful to get an overview of the technological trends in raw voltage and current ratings.

## Resistance fighters battle r<sub>DS(on)</sub>

The current-carrying capabilities of a power MOSFET are, naturally, related to the device's onresistance, or  $r_{\rm DS(on)}.$  The conducted current times this resistance represents the on-state power, and this power is the limiting factor for the transistor. You can easily determine the maximum allowable current for a given MOSFET by using the specs for the junction-to-case or junction-to-ambient thermal resistance  $(R_{thJC} \ or \ R_{thJA})$  of the device. You'd use the former spec in systems that have perfect heat sinking; the latter, in systems without any heat sinking.

The criterion for determining a MOSFET's maximum allowable current is the 150°C limit on junction temperature. If the case (and junction) temperature is 25°C at no power, the allowable junction-temperature rise when power is applied is 125°C. Consider the

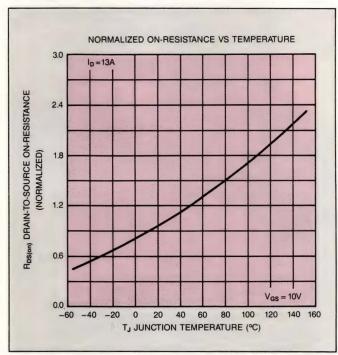


Fig 1—The positive temperature coefficient of  $r_{DS(on)}$  in a power MOSFET makes it necessary to derate operating currents at elevated temperatures. That requirement can be beneficial; it prevents thermal runaway. (Courtesy International Rectifier)



These hermetic packages from Motorola resemble the plastic TO-220 and TO-247. These housings let you replace the old, bulky TO-3 in environments requiring hermeticity.

calculation for the ubiquitous IRF450, a 500V device that was developed by International Rectifier (IR) and is now available from many vendors. Its  $r_{DS(on)}$  is  $0.4\Omega,$  and its  $R_{thJC}$  is  $0.83^{\circ}\text{C/W}.$  This figure produces a maximum-allowable-power spec of 150W. When you use the equation  $P=I^2R$  and work backwards, you apparently obtain a current limit of 19.4A.

Note, however, that the  $0.4\Omega$   $r_{DS(on)}$  is valid at  $25^{\circ}\mathrm{C}$  only. Fig 1 shows the typical variation in  $r_{DS(on)}$ ; at a  $150^{\circ}$  junction temperature, the on-resistance is 2.2 times the  $25^{\circ}\mathrm{C}$  value, or  $0.88\Omega$ . A new calculation yields a  $13\mathrm{A}$  current limit, the value given by the manufacturer. Most data sheets do specify the maximum allowable current; the point of this calculation exercise is to allow you to determine this current in situations in which the heat sinking is less than perfect. The important thing to know is the *case* temperature in any given application.

This said, consider the state of the art in terms of  $r_{\rm DS(on)}$  for available power MOSFETs. Starting with 50V devices, Siliconix and SGS-Thomson both offer TO-220-packaged power MOSFETs that spec 23-m $\Omega$  max on-resistance. The secret to getting the resistance down is to pack as many parallel-connected cells as possible onto a die. For example, the \$1.30 (OEM qty) STVHD90 from SGS has a density of 2.3 million cells/in2. Such packing densities don't come without a price—the input capacitances ( $C_{\rm iss}$ ) for the mentioned types are 3500 and 3000 pF max, respectively. By contrast, 50V devices having  $0.1\Omega$  on-resistance have  $C_{\rm iss}$  specs lower than 1000 pF.

IXYS and Siliconix offer 100V devices that spec the

lowest  $r_{DS(on)}$  figures in the industry. The \$17.50 (50) IXTH75N10 from IXYS has  $20\text{-m}\Omega$  max on-resistance, handles 70A, and comes in a plastic TO-247 (also called TO-3P) package. Its 4200-pF typ  $C_{iss}$  is indicative of the high-density architecture used in the company's process, dubbed MegaMOS. Housed in a hermetic TO-3 package, Siliconix's 25-m $\Omega$ , 75A SMM70N10 costs \$14.40 (100). And remember the VLSI nature of these powerhouses—Siliconix uses a Class-1 wafer-fabrication facility for the devices. To keep prices to a reasonable level, the company fabricates the parts on 6-in. wafers.

For applications requiring somewhat lower current-handling capabilities, Siliconix has recently introduced two companion devices housed in the venerable TO-220 plastic package. The SMP40N10 and SMP30N10 have  $r_{DS(on)}$  specs of 40 and 60 m $\Omega$ , respectively. Again,  $C_{iss}$  inversely tracks the on-resistance—the transistors spec 3000 and 1500 pF typ, respectively, and cost \$9.60 and \$4 (100).

#### 1000V MOSFETs proliferate

Bipolar transistors have always been available with very high voltage ratings, and those ratings don't carry onerous price penalties. Achieving good high-voltage performance in power MOSFETs, however, has been problematical, for several reasons. First, the  $r_{\rm DS(on)}$  of devices of equal silicon area increases exponentially with the voltage rating. To get the on-resistance down, manufacturers would usually pack more parallel cells onto a die. But this denser packing causes problems in high-voltage performance. Propagation delays across

a chip, as well as silicon defects, can lead to unequal voltage stresses and even to localized breakdown.

Manufacturers resort to a variety of techniques to produce 1000V, low- $r_{DS(on)}$  power MOSFETs that offer reasonable yields (and therefore, affordable prices). Advanced Power Technology (APT), for example, deviates from the trend toward smaller and smaller feature sizes in its quest for low on-resistance. Instead, the company uses large dies to get  $r_{DS(on)}$  down. The rationale is twofold. First, the relatively large geometries make the chips more tolerant of defects than are VLSI-based devices, and this tolerance manifests itself in higher yields. Second, the company claims the large chip sizes provide for efficient heat transfer to package headers.

A striking example of APT's large-die power MOSFETs is a 1000V device that uses a  $388 \times 588$ -mil chip. The \$177.65 (1000) APT5010FN specs  $0.5\Omega$  rDS(on), a figure that gives the device a 22.5A usable-current rating. According to Terry Bowman, APT's marketing and sales manager, this high current rating makes it easy to design with this part, because it reduces the number of parallel MOSFETs required in high-power systems.

Housed in a hermetically sealed F-pack (called "Mighty MOS" by APT), the APT5010FN can dissipate 595W at  $25^{\circ}$ C case temperature. The package measures  $1.5 \times 2 \times 0.325$  in. It's impressive for its power-handling capability, but also for the fact that it provides four leads for the MOSFET connections. A source-sense lead allows you to maximize switching speed. Fig 2a shows a traditional 3-lead connection. Here, a voltage

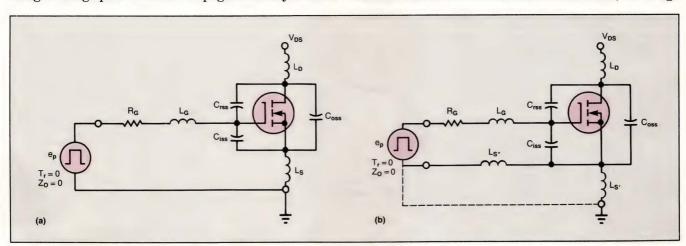


Fig 2—A source-sense terminal speeds the operation of a power MOSFET. When you use a 3-terminal MOSFET (a), the inductance in the source line degrades switching performance. In b, the fourth terminal allows the full potential of the driving source to develop between the gate and the source.

EDN January 5, 1989

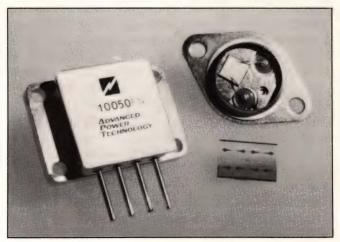
You must consider total system cost when choosing a switching element. Low-cost bipolars often require complicated, costly drive circuits.

L<sub>S</sub>di/dt appears at the source, effectively reducing the gate-drive potential. In Fig 2b, the added source-sense lead provides for an essentially floating gate drive. The resulting full gate-drive potential improves the device's fall time.

Other F-pack units from APT, rated from 400 to 800V, have corresponding  $r_{\rm DS(on)}$  specs ranging from 0.07 to 0.3 $\Omega$ . The maximum  $C_{\rm iss}$  for these large MOSFETs is 6300 pF. A number of less-expensive 1000V devices can still provide impressive  $r_{\rm DS(on)}$  figures, because they use smaller silicon dies. The IXTH12N100 from IXYS Corp, for example, comes in a plastic TO-247 or a hermetic TO-3 package and specs  $1\Omega$  on-resistance. The unit has a  $C_{\rm iss}$  of 4500 pF max and costs \$26.71 (50).

Speaking of large MOSFETs, note that a family of huge-die units (available in die form) from APT is poised to hit the market. These range from the 1000V/43A APT10020DN to the 350 and 400V/120A APT3503DN and APT4003DN. These giants, connected in a full-bridge configuration, allow designers to break the 4-device, 2-kW barrier (in fact, to 10 kW).

Even lower in price than IXYS's IXTH12N100 is the company's  $2\Omega$ , 2800-pF IXTM5N100A, which comes in a plastic TO-247 or a hermetic TO-3 package and costs \$14.06 (50). Note that APT, too, offers smaller-die units in TO-3 packages; the parts spec onresistances from 1 to  $3.5\Omega$ . APT claims its process yields  $C_{iss}$  figures lower than those for other equivalent-rated units in the industry. Its 1 and  $2\Omega$  units, for example, spec 2450 and 1750 pF, respectively, while the IXYS devices with the same ratings spec 4500 and 2800 pF. Note that International Rectifier, the univer-



This relative behemoth of a package from Advanced Power Technology dissipates 595W and can accommodate chips larger than 1 in<sup>2</sup>.

sally acknowledged leader among MOSFET suppliers, introduced 2 to  $11.5\Omega$  1000V MOSFETs last year. Finally, watch for the imminent announcement of a  $0.7\Omega$ , 1000V device from SGS-Thomson.

#### Ruggedness catches on

Some years ago, General Electric (Syracuse, NY) introduced the concept of "ruggedness" specs to the MOSFET world. Ruggedness, for a MOSFET, is the ability to withstand an avalanche current (at the breakdown voltage) caused by the flyback effect that an unclamped inductive load produces. A MOSFET's ruggedness is certainly of interest to designers, because it determines whether or not a given application will need external protective circuitry.

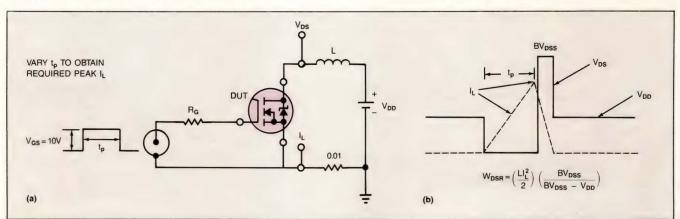


Fig 3—An unclamped inductive load proves a MOSFET's ruggedness. The inductance, L, in a, causes a flyback action (b) when the falling input signal tries to shut the MOSFET off. Avalanche energy is a function of the peak drain-source current, the voltage levels, and the inductor value.

Fig 3a shows the unclamped, inductive switching test circuit that appears in IR's power-MOSFET data sheets. With minor variations, it's the same circuit adopted by most MOSFET manufacturers. The timing diagram in Fig 3b shows what happens when the input pulse falls and tries to turn the device off. The flyback effect of the inductor sustains the MOSFET current at  $I_L$ , and the MOSFET undergoes avalanche at its breakdown voltage,  $BV_{DSS}$ . The equation in Fig 3 gives the avalanche energy in Joules.

Among several manufacturers, ruggedness specs are becoming an integral part of power-MOSFET data sheets. What's needed are standardized test methods and conditions. According to IXYS marketing director Rich Fassler and other authorities, DESC will soon issue such standards. To see an example of how ruggedness specs vary from manufacturer to manufacturer, consider the IRF450 workhorse (a 500V/13A part) and the IRFP040 (a 50V/40A device).

For both devices, International Rectifier specifies the nonrepetitive avalanche energy at 760 mJ and the avalanche current (the value at the time of attempted shutoff) at 14A. The repetitive energy (the duty cycle is <1%) listed in the IR sheet is 18 mJ. Further, that spec sheet gives a curve of avalanche energy vs starting junction temperature. For its identically rated IXTH12N50, IXYS specifies only the nonrepetitive avalanche energy (it's 800 mJ). For its ruggedized IRF450R, RCA specs the energy at 860 mJ and gives the inductor value (9.2 mH) for the test circuit.

In the data sheet for its 50V/40A MTM50N05E, Motorola specifies nonrepetitive energy at 55 mJ with the conditions  $I_L=160A$  and  $V_{DD}=25V$ . Further, the sheet lists the energy in a repetitive test as 100 mJ at a 25°C case temperature ( $I_L=50A$ ), and as 35 mJ at a 100°C case temperature ( $I_L=20A$ ). For its samerated IRFP040, IR specs  $I_L$  at 4.3A and gives no energy figures. These examples illustrate that, at the moment, it's somewhat difficult to compare the ruggedness of devices from different manufacturers. The situation will change with the advent of the DESC standards.

Another object of scrutiny by the military establishment is commutating safe operating area (CSOA). This

## "Die" and other atrocities

How many times have you seen the word "die" used as a plural? "Company X offers a full range of power MOSFET die," people have been heard to say. Well, the plural of the singular word "die" is "dies." To point out this incorrect usage might seem like nitpicking, but I'm convinced that there are those among EDN's readership who object to our industry's systematic massacre of the English language. After all, would you say "I bought three new shirt last week"?

Consider, for example, "verbizing"—the art of creating new verbs from nouns. (Of course, there's no such word as "to verbize;" it's the editorial world's contribution to the massacre.) In the electronics industry, verbizing is rampant: "You can input

the signal to pin 1, you can interface the data to the bus, you can leverage the stock deal—there's an inductive load, let's freewheel-diode the output." Sometimes it's easier to use such nouns as verbs, and difficult to come up with the correct equivalent phrase, but that's no excuse for incorrect grammar.

Finally, note the industry's propensity for obfuscation, the fine art of using jargon either to hide the fact that you don't know what you're talking about, or to make sure the reader or listener will never be able to figure out what you're trying to say. This art—born, nurtured, and perfected in Washington, DC—is catching on like wildfire in high-tech circles. The following example is taken from an interview

that appeared in another publication (we'll leave it unnamed here):

Q: Can you give us an example of how such total integration might be achieved using expert systems?

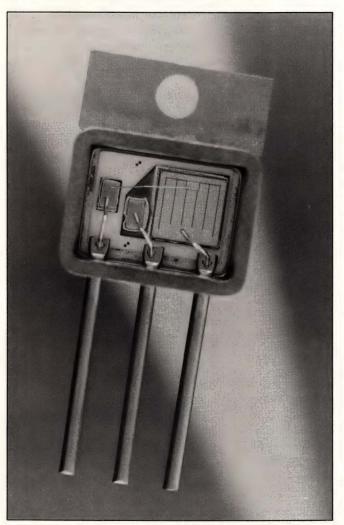
A: Let's look at a hypothetical greenfield situation. To begin with, the integration process will have to be both top-down and bottom-up. In other words, it will involve incremental expansion of the corporate-level knowledge infrastructure at the same time that individual expert systems are being developed and put on-line to provide productivity solutions at the level of the component life-cycle phases.

I rest my case.—BT

Besides improving MOSFETs' and IGBTs' voltage and current ratings, manufacturers are adding survivability, ease of use, and "smartness."

area is bounded by the recovery characteristics (dV/dt) of the intrinsic source-drain diode. Motorola, for example, gives CSOA curves in its MOSFET data sheets. The rectangular areas in the curves impose limits on drain current and drain-to-source voltage with the condition of a specified maximum rate of change of the source current. Motorola's product-marketing manager, Bob Bailey, states that JEDEC specs for dV/dt will appear this year.

One example of the emphasis MOSFET manufacturers are placing on the ruggedness issue is IR's introduction of 400 and 500V devices this year; the product announcements stress avalanche and dV/dt ratings. The \$6.69 (1000) IRFP448, a 500V/11A MOSFET, specs the nonrepetitive and repetitive avalanche en-



This hermetic power package from Omnirel provides isolation and accommodates large power-semiconductor chips.

ergy at 550 and 17 mJ, respectively, and gives peak diode-recovery dV/dt as 3.5V/nsec. The \$23 (1000) IRFP360 is a 400V/25A device; its corresponding ruggedness specs are 980 and 30 mJ and 4V/nsec. Finally, be aware that, for its 30, 40, and 70A MOSFETs, Siliconix specs the repetitive avalanche current at 30, 40, and 70A (continuous).

#### Fast-recovery diodes

Speaking of dV/dt, manufacturers are devoting a lot of development effort to improving the recovery characteristics of the intrinsic source-drain diode. For example, the 1.2-µsec max recovery time for the IRF450's diode places a severe limitation on the attainable repetition rate in inductive-load applications, and often creates the need for external snubbers and clamps. A number of available devices address the diode-recovery issue.

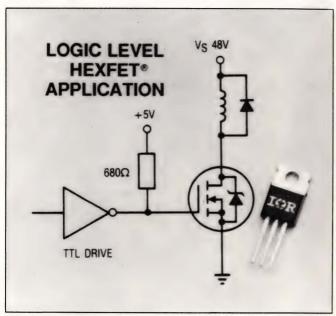
As for Siliconix's 30, 40, and 70A MOSFETs, note that these devices spec respective recovery times of 130, 120, and 125 nsec typ. For its TMOS IV Series ruggedized MOSFETs, Motorola specs low (70 to 300 nsec typ) diode-recovery times. SGS's 50V/52A STVHD90 specs a recovery time of 70 nsec typ.

Siemens started the fast-recovery ball rolling some years ago by introducing its line of FREDFETs (fast-recovery epitaxial-diode FETs). Philips-Amperex has joined the fray by offering the BUK600 Family of FREDFETs. These devices spec ratings to 400V/14A and 1000V/9A.

#### Sensing makes sense

The technique of current mirroring for source-current-sensing purposes, which was introduced a few years ago, involves connecting a small fraction of the cells in a power MOSFET to a separate sense terminal. The current in this terminal is a fixed fraction of the source current feeding the load. This Kelvin-like configuration is useful for monitoring and in closed-loop-feedback applications. It's also valuable if you must squeeze the maximum switching speed from a MOSFET. For example, you can use the sense terminal as described in Fig 2 to eliminate the effects of source-lead inductance in high-speed switching applications.

A couple of examples of such sense-terminal MOSFETs come from IXYS's recent line of Mirror-FETs. Housed in a TO-247 package, the IXTH39N08MB specs 80V/39A and costs \$9.26 (50). Also in a TO-247 package is the IXTH20N60MB, which handles 600V/20A and costs \$18.53 (50). IR, Motorola,



Logic-level MOSFETs from International Rectifier derive drive directly from TTL or CMOS logic.

and Philips-Amperex also offer a wide variety of source-sensing power MOSFETs; they're called HEXSense, SenseFETs, and SensorFETs, respectively.

Another subdivision of the rapidly diversifying power-MOSFET market is a class of devices called logic-level FETs. Before the advent of these units, drive circuitry had to supply gate-source turn-on levels of 10V or more. The logic-level MOSFETs accept drive signals from CMOS or TTL ICs that operate from a 5V supply. Suppliers of these types include IR, GE, IXYS, Philips-Amperex, and Motorola.

Some recent offerings from IR exemplify what's available in logic-level MOSFETs. One family of TO-220-packaged units, for example, has voltage ratings of 60 and 100V, and handles continuous currents from 5.7 to 35A. In keeping with the present spirit of ruggedness, IR specifies avalanche and dV/dt parameters for the devices. The parts' prices range from \$0.34 to \$2.39 (1000).

A recent series of units from Philips-Amperex rounds out the company's 50, 100, and 200V logic-level product line. The new devices increase continuous-current ratings from 8.5 to 40A for 50V units, and 3.5 to 12A for 200V MOSFETs. Motorola's logic-level line spans the range from 60V/15A to 150V/10A. Speaking of these two companies, something's afoot in the way power MOSFETs will be specified in the future. The

Philips-Amperex devices are specified for operation at a 175°C junction temperature vs the classical 150°C. Motorola plans to specify all its <250V MOSFETs the same way. And note that certain of IR's HEXSense devices are also specified at 175°C.

This increase in allowable junction temperature allows you to squeeze about 10% more current out of a MOSFET of a given die size. Motorola's Bob Bailey attributes the spec loosening to improvements in molding compounds; earlier plastics suffered a glass transition and became brittle at approximately 165°C.

The way to make logic-level MOSFETs is to reduce the thickness of the gate oxide. This reduction, of course, makes the gate more susceptible to voltage breakdown. Motorola ensures the breakdown-proof properties of its power MOSFETs by using what the company dubs the "Bullet-Proof" process. To guarantee gate-breakdown integrity, Motorola applies a 200-msec pulse to the gates of all its production units. The amplitude of the pulse is 60V for ≥400V devices, 40V for <400V units, and 20V for logic-level MOSFETs.

Killing two birds with one stone, IXYS both achieves logic-level operation in its LIMOFET line and lowers input-drive requirements by incorporating two chips in a single package. An internal CMOS driver has a totem-pole output section that can switch the Mega-MOS chip at rates as high as 500 kHz. A side benefit of the 2-chip solution is the low input capacitance—about 50 pF vs thousands of picofarads for large, unassisted MOSFETs. Note that although the input of the tandem operates from TTL levels, the driver requires a separate 7 to 15V supply. These are big devices; packaged in large, hermetic packages called Z-Pacs, they span the range from 100V/67A to 1000V/11A. They cost \$118.78 to \$163 (10).

#### Making MOSFETs spaceworthy

Some military and space applications require that their electronic parts be immune to radiation. Although, thanks to the physics of their technology, power MOSFETs are relatively immune to the effects of radiation exposure, they do tend to undergo self-enhancement in the presence of large doses. To counteract this self-turn-on tendency, you need to supply a negative gate-source bias voltage in your application. There are also some parts from GE/RCA and IR that don't have this proclivity for self-enhancement.

Rad-hard MOSFETs from IR, first announced last year in TO-3 packaging, have voltage ratings of 100, 250, and 500V, and respective current ratings of 38,

Dense geometry, new processes, and more efficient packaging have raised the voltage and current capabilities of both power MOSFETs and IGBTs.

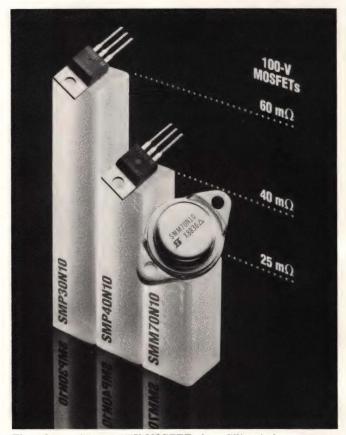
19, and 10A. A series of units housed in TO-254 (hermetic TO-220) packages, which the company announced shortly thereafter, have identical ratings. These MOSFETs are guaranteed to be immune to radiation doses as high as 1M rad (S<sub>i</sub>). Further, they can survive short-term doses as high as 10<sup>12</sup> rad (S<sub>i</sub>)/sec. The TO-3 devices cost \$493.84 to \$609.78 (1000); the TO-254 units sell for \$519.83 to \$576 (10).

Similar rad-hard MOSFETs are available from GE/RCA. Rated to withstand steady doses as high as 1M rad, they're available in 100V (14 and 38A) and 200V (9 and 30A) versions. These TO-3-packaged units, too, display survivability to  $10^{12}$  rad ( $S_i$ )/sec. In addition, their data sheets claim they can survive exposures of  $2 \times 10^{12}$  neutrons.

These rad-hardened MOSFETs could be considered specialty items. To a lesser degree, you could also consider p-channel power MOSFETs to be specialties. Although a healthy market exists for them, it pales in comparison with the market for n-channel devices. It takes so much more silicon to achieve a given rating in a p-channel device, that first, equally rated units cost much more; and second, in a given package, the current limit for a p-channel MOSFET is usually ½ to ¼ of the limit for n-channel devices. As a result, designers often resort to quasicomplementary output structures, and—when the need exists for a high-side switch—they resort to charge-pump techniques to generate the necessary gate drive for an n-channel MOSFET.

Nevertheless, most of the manufacturers cited here do make p-channel MOSFETs to complement their n-channel devices. New-product announcements are few and far between, however. One exception, and a recent one, is Siliconix's family of MOSFETs housed in JEDEC TO-254 (hermetic TO-220) packages. Designated 2N7071 through 2N7080, the series comprises eight n-channel and two p-channel MOSFETs. The n-channel units have ratings of 100V/24A and 100V/30A; 200V/16A and 200V/28A; 400V/9A and 400V/15A; and 500V/7A and 500V/13A. The two p-channel devices have ratings of 100V/17A; and 200V/9.5A (minus signs are omitted for clarity). Prices range from \$48.37 to \$75.60 (100).

Another exception to the paucity of p-channel announcements is a series of low-cost devices from Motorola, appropriate as complements to the company's (and many others') 3055-type n-channel MOSFETs. The MTD/MTP Series is rated at 60V/12A, and costs \$0.60 (1000). The parts are available in a surface-mount



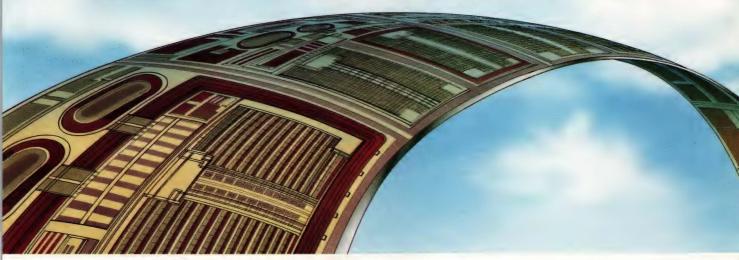
These low-resistance 100V MOSFETs from Siliconix have 25-, 40-, and  $60\text{-}m\Omega$  on-resistance specs.

or insertion-mount miniature plastic package called the D-Pack, or in a TO-220 package.

A final specialty item worthy of note is a series of temperature-protected power MOSFETs from Siemens. These products each contain a power-MOSFET chip and a temperature sensor having a thyristor (SCR) characteristic. When the MOSFET's junction temperature exceeds 150°C, the sensor places a short circuit across the gate and source, thereby shutting the MOSFET off. To reset the device, you bring the gate to 0V, then reapply the gate signal.

The BTS Series of temperature-protected MOSFETs covers the range from 50V at 12, 14, 25, 27, and 58A; and 60V at 24A. The 50V/58A device comes in a TO-218 package; all the others are housed in TO-220 packages. In addition to these n-channel units, a 50V/8A p-channel device in a TO-220 package is available.

Finally, although they're somewhat beyond the scope of this report (because they're ICs, and not discrete devices or assemblies thereof), some "smart" power devices are worthy of mention. The BTS412A



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The migration to a 175°C maximum permissible junction temperature allows you to obtain about 10% more current from a MOSFET.

from Siemens and the MPC1510 from Motorola, for example, are 30V/12A high-side power switches that incorporate such features as short-circuit and overtemperature protection and a charge-pump circuit to provide gate drive for the output stage.

For motor control, medium-frequency (50 kHz or so) switching power supplies, and other applications requiring a low-loss switch, IGBTs (insulated-gate bipo-

lar transistors) are a viable alternative to bipolar transistors and power MOSFETs. Their MOS-like input characteristics and bipolar-like output traits would seem to make them attractive indeed to designers. However, their slow fall times (several microseconds) and their propensity to latch when overcurrent conditions occur have seemingly proved an impediment to their popularity in the marketplace.

## Manufacturers of power MOSFETs and IGBTs

For more information on power MOSFETs and IGBTs of the types discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

ABB Semiconductor 2150 W 6th Ave Broomfield, CO 80020 (303) 469-1883 FAX 303-469-8394 Circle No 357

Advanced Power Technology 405 SW Columbia St Bend, OR 97702 (503) 382-8028 FAX 503-388-0364

Fairchild Semiconductor Corp 313 Fairchild Dr Mountain View, CA 94042 (415) 962-4011 Circle No 359

Circle No 358

Ferranti Electric Inc 87 Modular Ave Commack, NY 11725 (516) 543-0200 Circle No 360

Fujitsu Components 3320 Scott Blvd Santa Clara, CA 95054 (408) 562-1000 Circle No 361

GE/RCA Solid State Route 202 Somerville, NJ 08876 (201) 685-6000 Circle No 362

General Instrument Corp 600 W John St Hicksville, NY 11801 Circle No 363 Gentron Corp 6667 N Sidney Pl Milwaukee, WI 53209 (414) 351-1660 TLX 26881 Circle No 364

Hitachi America Ltd 2210 O'Toole Ave San Jose, CA 95131 (408) 942-1500 Circle No 365

International Rectifier 233 Kansas St El Segundo, CA 90245 (213) 772-2000 Circle No 366

IXYS Corp 2355 Zanker Rd San Jose, CA 95131 (408) 435-1900 FAX 408-435-0670 Circle No 367

Motorola Semiconductor Products 5005 E McDowell Rd Phoenix, AZ 85008 (602) 244-6900 Circle No 368

Omnirel Corp 205 Crawford St Leominster, MA 01453 (508) 534-5776 FAX 508-537-4246 Circle No 369

Philips Components Amperex Div George Washington Hwy Smithfield, RI 02917 (401) 232-0500 Circle No 370 Powerex Inc Hillis St Youngwood, PA 15697 (800) 451-1415 In NY, (315) 457-9334 Circle No 371

Powertec Inc 20550 Nordhoff St Chatsworth, CA 91311 (818) 882-0004 TLX 277483 Circle No 372

Samsung Semiconductor 3725 N First St San Jose, CA 95134 (408) 434-5538 FAX 408-434-5650 Circle No 373

Sanyo Semiconductor Corp 7 Pearl Ct Allendale, NJ 07401 (201) 825-8080 TLX 135138 Circle No 374

SGS-Thomson Microelectronics 1000 E Bell Rd Phoenix, AZ 85022 (602) 867-6100 Circle No 375

Siemens Semiconductor Group 2191 Laurelwood Rd Santa Clara, CA 95054 (408) 980-4500 Circle No 376 Silicon General 11861 Western Ave Garden Grove, CA 92641 (714) 898-8121 FAX 714-893-2570 Circle No 377

Siliconix Inc 2201 Laurelwood Rd Santa Clara, CA 95054 (408) 988-8000 FAX 408-727-5414 Circle No 378

Supertex Inc 1225 Bordeaux Dr Sunnyvale, CA 94086 (408) 744-0100 Circle No 379

Tokin America Inc 2261 Fortune Dr San Jose, CA 95131 (408) 432-8020 FAX 408-434-0375 Circle No 380

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Pin for pin compatible.

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Only a few years ago, manufacturers had a very limited list of options for packaging MOSFETs; now, that situation has changed dramatically.

Well, they're improving, and the improvements are coming from companies outside of the original IGBT three (GE with its IGT, RCA with its COMFET, and Motorola with its GEMFET). The companies that are announcing the improved products are International Rectifier, SGS-Thomson, Philips-Amperex, and IXYS.

IR's recent IRG Series, for example, is a 600V/11 to 30A family that carries on the company's policy of specifying avalanche energy (as high as 100 and 12.5 mJ nonrepetitive and repetitive, respectively) in unclamped inductive-switching situations. Housed in a TO-220 package, the parts dissipate 74W and exhibit 3V max saturation voltage at rated current. The fall time is a respectable 420 nsec typ. The IRGBC20, -30, and -40 spec current ratings (at 25°C) of 11, 18, and 30A, respectively, and cost \$3.60, \$5.10, and \$9.40 (1000). Also watch for IR's imminent announcement of the industry's first 1200V IGBT.

Also extending its IGBT voltage ratings is IXYS, which now offers 1000V units. Housed in TO-247 packages, the parts spec 25°C currents of 20, 40, and 50A. The fall time is 500 nsec typ, 1 µsec max. The 40A IXGH20N100A and 50A IXGH25N100A come in TO-247 packages and cost \$9.98 and \$14.98 (1000). The 20A IXGP10N100A, in a TO-220 package, costs \$4.99 (1000). The company also offers 800 and 900V versions of the devices.

As with its power-MOSFET line, IXYS offers high-density IGBTs, dubbed MegaMOS IGTs. These parts have higher current-handling specs than those of the company's standard line of IGBTs. For example, the 600V IXGH40N60A handles 75A (by comparison, the IXGH30N60A offers 60A). The fall time is 0.8 μsec, and the saturation voltage is 3.2V at rated current. Housed in a TO-247 package, the device costs \$15.84 (10).

Both IR and IXYS claim their IGBTs provide latchfree operation. That claim is substantiated by the data sheets, which guarantee enormous peak-current capabilities for the devices. For instance, IXYS's IXGH40N60A IGBT can withstand 150A at a 150°C junction temperature without latching. And IR's 600V family specs 72A peak-current capability.

Also housed in a TO-220 package, SGS-Thomson's STHI Series has ratings of 500V/7A and 500V/10A. The STHI07N50 and STHI10N50 spec a 2.7V max saturation voltage at rated current, and a 1.5- $\mu$ sec max fall time. Finally, although details are sketchy,

Philips-Amperex has an IGBT family in the offing. The BUK800 family will comprise 500, 800, and 1000V devices, and will be available in various packages.

#### New packages proliferate

Just a couple of years ago, MOSFET makers had a very limited list of options for packaging their high-power devices. The list included the hermetic TO-3 (which has since been renamed "TO-204" for reasons unknown), the plastic TO-218 and TO-247 (also called TO-3P) for high-wattage devices, and the venerable TO-220 for medium-power chips. Unfortunately, the only workable hermetic package was the bulky, difficult-to-mount TO-3.

Now, the situation has changed dramatically. Hermetically sealed equivalents exist for both the TO-247 and the TO-220. The TO-258 replaces the TO-218 (or TO-247), and the TO-257 is a hermetic TO-220. Another hermetic package, the TO-254, lies between the TO-257 and TO-258 in terms of dimensions. In addition to these standard package types, several manufacturers have developed special packages to accommodate their dies. Especially striking is the advent of very large, high-current packages that accept very large dies or multiple chips.

Consider, for example, Advanced Power Technology's Mighty MOS package, also called the F-Pack. This 4-lead, isolated package handles 595W (the nonisolated TO-3 is limited to about 250 or 300W). As a bonus, the F-Pack has an enormous cavity that accommodates chips whose total area exceeds 1 in<sup>2</sup>. Another large hermetic package is IXYS's Z-Pac, which occupies roughly the same area that a TO-3 package does. This 300W housing has five axial leads that egress from opposing edges of the package. Another example of power packaging is SGS-Thomson's IsoTop, which also occupies about as much space as a TO-3 does. It holds as many as four chips and accommodates currents as high as 100A. Philips-Amperex also produces power products in the IsoTop.

A specialist in plastic packaging, Motorola offers its MOSFETs in the small, surface-mountable D-Pack. This package measures about 240×260 mils and accepts chips as large as 112×112 mils. Although it's much smaller than the TO-220, the D-Pack can dissipate nearly 80% as much power. IR also produces a wide range of MOSFETs in the D-Pack. Another plastic package from Motorola is the isolated, metal-backed

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IcePack. This 12-lead package accommodates multiple chips for such applications as H-bridge drivers (for example, the MPM3002 H-bridge power module).

Motorola is also making progress with its hermetic packaging. The MO-78 is a 5-pin hermetic package that resembles the TO-257 and TO-258. And, in a symbiotic relationship with Omnirel, a hybrid-circuit manufacturer and packaging specialist, Motorola is developing a larger version of the D-Pack—a surface-mountable replacement for the TO-220. Further collaboration with Omnirel will help Motorola expand its penetration of the military/high-reliability MOSFET market. This collaboration involves standard TO-257 and TO-258 packages, as well as large, multipin packages for power hybrids.

Finally, note that virtually all the companies mentioned here are producing power modules. These modules combine power-MOSFET chips, rectifiers, and other devices in such configurations as half or full H-bridges. Omnirel takes power-module manufacture one step further by hermetically sealing all its large power packages. Gentron is another company that produces high-power, hermetically sealed modules; it also makes a broad line of large plastic power modules. Yet another manufacturer is ABB Semiconductor (formerly Brown Boveri), which combines IGBTs, for example, in sextuples in a large plastic package for a 3-phase motor drive.

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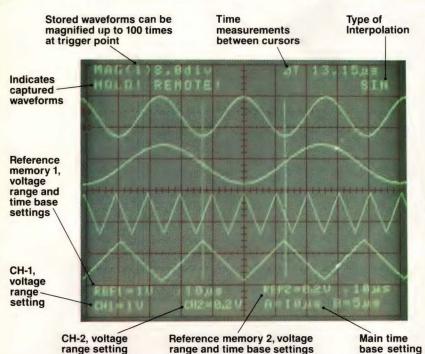
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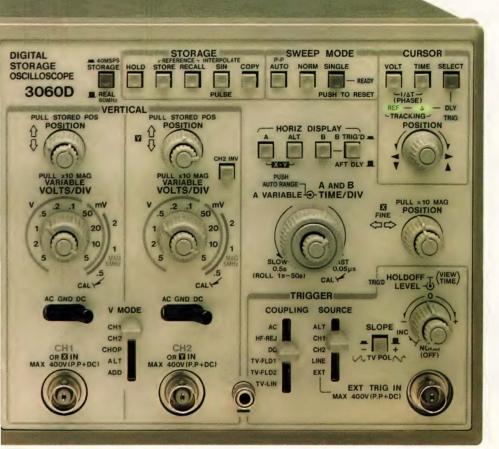
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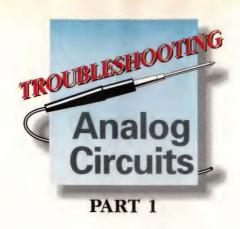
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# Troubleshooting is more effective with the right philosophy

In this first installment of a multipart series, one of the world's leading analog-circuit designers makes the case that a significant part of effective troubleshooting lies in the way that you think about the problem. The next installment will cover the equipment you should buy—and build—to help you diagnose problems, and future installments will illuminate some of the more subtle and elusive characteristics of passive and active components and the pc boards and cables that interconnect them.

#### Robert A Pease, National Semiconductor Corp

If you recall that the most *boring* class in school was a philosophy class, and you think this article will be boring that way, well, WRONG. We are going to talk about the real world and examples of how we can recover from mistakes, goofs, and all the nasty problems the world tries to inflict on us. We are talking about Trouble with a capital T, and how to overcome it.

Here at National Semiconductor, we decided a couple of years ago to write a book about switching power supplies. Within the applications and design groups, nearly all of the engineers volunteered to write chapters, and I volunteered to do a chapter on troubleshooting. At present, the status of the book is unclear. But, the troubleshooting chapter is going strong, and EDN readers are the first to benefit.

Although I am probably not the world's best analog-circuit troubleshooter, I am fairly good; and I just happened to be the guy who sat down and put all these stories in writing. (Ed Note: For a better insight into how Bob happened to tackle this assignment, see box, "Who is Bob Pease, anyway?") Furthermore, the techniques you need to troubleshoot a switching power supply apply, in general, to a lot of other analog circuits and may even be useful for some basic digital hardware. You don't have to build switchers to find this article useful—if you design or build any analog circuits, this article is for you.

Perhaps EDN readers who are more knowledgeable than I am about computers, microprocessors, and software will contact the editors about contributing articles on troubleshooting those types of products. If you don't have enough troubleshooting ideas to produce a full-length article but do have some good tips that you don't see in this series, send them to the Design Ideas editor at EDN. No doubt, EDN will print some of them. (Be sure to include a copy of the design entry blank included in each issue's Design Ideas section.)

Why are we interested in troubleshooting? Because even the best engineers take on projects whose requirements are so difficult and challenging that the

## Troubleshooting should resemble fencing more closely than it resembles wrestling.

circuits don't work as expected—at least not the first time. I don't have data on switching regulators; but I read in an industry study that when disk drives are manufactured, the fraction that fails to function when power is first applied ranges from 20 to 70%. Of course, this fraction may occasionally fall as low as 1% and rise as high as 100%. But, on the average, production

engineers and technicians must be prepared to repair 20, 40, or 60% of these complex units.

Switching-regulated power supplies can also be quite complex. If you manufacture them in batches of 100, you shouldn't be surprised to find some batches with 12 pieces that require troubleshooting and other batches that have 46 such pieces. The troubleshooting

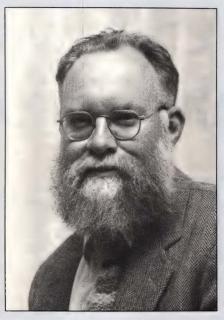
#### Who is Bob Pease, anyway?

For the record, Bob Pease is a senior scientist in industrial linear-IC design at National Semiconductor Corp in Santa Clara CA; he has worked at National since 1976. He is also one of the best-known analog-circuit designers in the world—he's been creating practical, producible analog products for fun (his) and profit (both his and his employers') and writing about analog topics for over a quarter of a century.

As you might expect, though, there's a lot more to Bob Pease than his impressive credentials. Following untrodden paths to discover where they lead is one of Bob's avocations. He's done it on foot, on skis, and on a bicyclesometimes by himself and sometimes with his wife and two sons-mostly along abandoned railroad beds throughout the US. Aside from the peace and quiet and the thrill of the journey itself, the reward for these wanderings is observing vistas of America that few people have seen. The curiosity that motivates Bob's exploration of old railroad routes is reflected in many of his other activities both at and away from work.

For example, another of Bob's hobbies is designing voltage-to-frequency converters (VFCs).

Most people who design VFCs do



it as part of a job. Although Bob sometimes designs VFCs for use in National products, he often does it just for fun and because he finds the activity educational and challenging. A while ago, on such a lark, he put together a VFC that used vacuum tubes. The device proved that the company where he spent the first 14 years of his career, George A Philbrick Researches, (now Teledyne-Philbrick of Dedham, MA) could have gone into the VFC business in 1953-eight years before Pease received his BSEE from MIT. Fifteen years after he designed it, one of Bob's first

solid-state VFCs, the 4701, continues to sell well for Teledyne-Philbrick.

#### Pease pontificates prolifically

Bob also loves to write—he clearly enjoys communicating to others the wisdom he has acquired through his work. He has published 46 magazine articles (not including this series) and holds eight patents. Bob takes great delight in seeing his ideas embodied in the work of others. For example, one of his proudest accomplishments is a seismic preamplifier that he designed for an aerospace company during his coffee break. After many years of service, the amplifier is still at work on the moon, amplifying and telemetering moonquakes.

National has taken advantage of Bob's penchant for providing ideas that others can use. In his role of senior scientist, Bob's responsibilities—besides designing voltage references and regulators, temperature sensors, and VFC ICs—include consulting with coworkers, fielding applications questions that have stumped other engineers, and reviewing colleagues' designs. In a similar vein, Bob is a long-time EDN contributing editor who reviews design-idea submissions in the analog area.—Dan Strassberg



**Peer review is often effective** for wringing problems out of designs. Here, the author gets his comeuppance from colleagues who are not as familiar with his circuit layout as he is.

may, as you well know, be tough with a new product whose bugs haven't been worked out. But, it can be even tougher when the design is old and the parts it now uses aren't quite like the ones you once could buy. Troubleshooting can be tougher still when there is little documentation describing how the product is supposed to work and the designer isn't around anymore. If there's ever a time when troubleshooting isn't needed, it's just a temporary miracle.

#### You might avoid troubleshooting . . . for a while

And, what if you decide that troubleshooting isn't necessary? You may find that your first batch of products has only three or four failures, so you decide that you don't need to worry. The second batch has a 12% failure rate, and all of the rejects have the same symptoms as those of the first batch. The next three batches have failure rates of 23, 49, and 76%, respectively. When you finally take the time to study the problems, you will find that they would have been relatively easy to fix if only you had started a couple of months earlier. That's what Murphy's Law can do to you if you try to slough off your troubleshooting chores—we have all seen it happen.

If you have a bunch of analog circuits that you have to troubleshoot, well, why don't you just look up the troubleshooting procedures in a book? The question is excellent, and the answer is very simple: Almost nothing has been written about the troubleshooting of such circuits. The best write-up I have found is a couple pages in a book by Jiri Dostal (Ref 1). He gives some basic procedures for looking for trouble in a fairly straightforward little circuit: a voltage reference/

regulator. As far as Dostal goes, he does quite well. But, he does not offer much advice, and there is much to explain beyond what he has written. Another book that has several pages about the philosophy of troubleshooting is by John I Smith (Ref 2). Smith explains some of the foibles of wishing you had designed a circuit correctly when you find that it doesn't work "right." What's missing, though, is general information

#### You'll probably use general-purpose test equipment

What equipment can you buy for troubleshooting? I'll cover that subject in considerable detail in the next installment. For now, let me observe that if you have several million dollars worth of circuits to troubleshoot, you should consider buying a \$100,000 tester. Of course, for that price you only get a machine at the low end of the line. And, after you buy the machine, you have to invest a lot of time in fixturing and software before it can help you. Yes, you can buy a \$90 tester that helps locate short circuits on a pc board; but, in the price range between \$90 and \$100,000, there isn't a lot of specialized troubleshooting equipment available. If you want an oscilloscope, you have to buy a general-purpose oscilloscope; if you want a DVM, it will be a general-purpose DVM. Now, it's true that some scopes and some DVMs are more suitable for troubleshooting than others (and I will discuss the differences in the next part of this series), but, to a large extent, you have to depend on your wits.

Your wits: very handy to use—your wits—but, then what? One of my favorite quotes from Jiri Dostal's book says that troubleshooting should resemble fencing more closely than it resembles wrestling. When your troubleshooting efforts seem most like wrestling in the mud with an implacable opponent (or component), then you are probably not using the right approach. Do you have the right tools, and are you using them correctly? I'll discuss that in the next issue. Do you know how a failed component will affect your circuit, and do you know what the most likely failure modes are? I'll deal with components in subsequent installments. Ah, but do you know how to think about Trouble? That is to-day's main lesson.

One of the first things you might do is make a list of all the things that could be causing the problem. This idea can be good—up to a point. I am an aficionado of stories about steam engines, and this story comes from the book, *Master Builders of Steam* (**Ref 3**). A class of new 3-cylinder 4-6-0 (four little wheels in front



The breadboard that launched a million chips, including National's LM 131. Pease's breadboards are legendary.

of the drive wheels, six drive wheels, no little wheels in back) steam engines had just been designed by British designer W A Stanier, and they were "perfect stinkers. They simply would not steam." So the engines' designers made a list of all the things that could go wrong and a list of all the things that could not be at fault; they set the second list aside.

The designers specified changes to be made to each new engine in hopes of solving the problem: "Teething troubles bring modifications, . . . and each engine can carry a different set of modifications." The manufacturing managers "shuddered as these modified drawings seemed to pour in from Derby (site of the design facility—the Drawing Office), continually upsetting progress in the works." (Lots of fun for the manufacturing guys, eh?)

In the end, the problem took a long time to find because it was on the list of "things that couldn't go wrong." Allow me to quote the deliciously horrifying words from the text: "Teething troubles always present these two difficulties: that many of the clues are very subjective and that the 'confidence trick' applies. By the latter I mean when a certain factor is exonerated as trouble-free based on a sound premise, and everyone therefore looks elsewhere for the trouble: whereas in fact, the premise is not sound and the exonerated factor is guilty. In Stanier's case this factor was low superheat. So convinced was he that a low degree of superheat was adequate that the important change to increased superheater area was delayed far longer than necessary. There were some very sound men in the Experimental Section of the Derby Loco Drawing Office at that time, but they were young . . . and their voice was only dimly heard. Some of their quite painstaking superheater test results were disbelieved." But, of course nothing like that ever happened to anybody you know—right?

Another thing you can do is ask advice only of "experts." After all, only an expert knows how to solve a difficult problem—right? Wrong! Sometimes, a major reason you can't find your problem is because you are

too close to it—you are blinded by your familiarity. You may get excellent results by simply consulting one or two of your colleagues who are not as familiar with your design; they may make a good guess at a solution to your problem. Often a technician can make a wise (or lucky) guess as easily as can a savvy engineer. When that happens, be sure to remember who saved your neck. Some people are not just lucky—they may have a real knack for solving tricky problems, for finding clues, and for deducing what is causing the trouble. Friends like these can be more valuable than gold. (For more on clues, see box, "Learn to recognize clues.")

At National Semiconductor, we usually submit a newly designed circuit layout to a review by our peers. I invite everybody to try to win a Beverage of Their Choice by catching a real mistake in my circuit. It's fun because if I give away a few pitchers of brew, I get some of my dumb mistakes corrected—mistakes that I might not have found until a much later, more painful, and more expensive stage. Furthermore, we all get some education. And, you can never predict who will find the little mistakes or the occasional real killer mistake.

#### You can make Murphy's Law work for you

Murphy's Law is quite likely to attack even our best designs: "If anything can go wrong, it will." But, I can make Murphy's Law work for me. For example, according to Murphy's Law, if I drive around with a fire extinguisher, I will make sure that I never have a fire in my car. When you first hear it, the idea sounds dumb. But, if I'm the kind of meticulous person who carries a fire extinguisher, I may also be neat and refuse to do the dumb things that permit fires to start. Similarly, when designing a circuit I leave extra safety margins in areas where I cannot surely predict how the circuit will perform. When I design a breadboard, I might tell the technician, "Leave 20% extra space for this part because I'm not sure that it will work without modifications. And, please leave extra space

around this resistor and this capacitor because I might have to change those values." When I design an IC, I leave little pads of metal at strategic points on the chip's surface, so that I can probe the critical nodes as easily as possible. To facilitate probing when working with 2-layer metal, I bring nodes up from the first metal through vias to the second metal. Sometimes I leave holes in my Vapox passivation to facilitate probing dice.

The subject of testability has often been addressed

for large digital circuits, but the underlying ideas of design for testability are important regardless of the type of circuit you are designing. You can avoid a lot of trouble by thinking about what can go wrong and how to keep it from going wrong before the ensuing problems lunge at you. By planning for every possibility, you can profit from your awareness of Murphy's Law. Now, clearly, you won't think of *every* possibility. (Remember, it was something that *couldn't* go wrong that caused the problems with Stanier's locomotives.)

#### Learn to recognize clues

There are four basic questions that you or I should ask when we are brought in to do troubleshooting on someone else's project:

- Did it ever work right?
- What are the symptoms that tell you it's not working right?
- When did it start working badly or stop working?
- What other symptoms showed up just before, just after, or at the same time as the failure?

As you can plainly see, the clues you get from the answers to these questions might easily solve the problem right away; if not, they may eventually get you out of the woods. So even if a failure occurs on your own project, you should ask these four questions—as explicitly as possible-of yourself or your technician or whoever was working on the project. Similarly, if your roommate called you to ask for a lift because the car had just quit in the middle of a freeway, you would ask whether anything else happened or if the car just died. If you're told that the headlights seemed to be getting dimmer and dimmer, that's a clue.



The telephone is sometimes a good troubleshooting tool; at other times, however, it is just another wretched part of the problem.

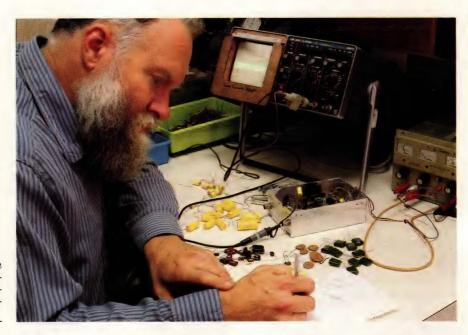
When you ask these four questions, make sure to record the answers in a notebook. As an old test manager I used to work with would tell his technicians, "When you are taking data, if you see something funny, record the amount of funny." A few significant notes can save you hours of work. Clues are where you find them; they should be saved and savored.

Ask not only these questions but also any other questions suggested by the answers. For example, a neophyte product engineer will sometimes come to see me with a batch of ICs that have a terrible yield at some particular test. I'll ask if the parts failed any other tests, and I'll hear that nobody knows because the tester doesn't continue to test a part after it detects a failure. A more experienced engineer would have already retested the devices in the RUN ALL TESTS mode.

Likewise, if you are asking another person for advice, you should have all the facts laid out straight—at least in your headso that you can be clear and not add to the confusion. I've worked with a few people who tell me one thing and a minute later start telling me the opposite. Nothing makes me lose my temper faster! Nobody can help you troubleshoot effectively if you aren't sure whether the circuit is running from +12V or  $\pm 12V$  and you start making contradictory statements.

And, if I ask when the device started working badly, don't tell me, "At 3:25 PM." I'm looking for clues, such as, "About two minutes after I put it in the 125°C oven," or, "Just after I connected the 4- $\Omega$  load." So just as we can all learn a little more about troubleshooting, we can all learn to watch for the clues that are invaluable for fault diagnosis.

It is important to get the paperwork scrupulously correct, or the alligators will surely circle back to vex you again.



A large collection of used components in good condition, such as the group of capacitors shown here, forms one part of an experienced analog troubleshooter's hardware armamentarium.

But, a little forethought can certainly minimize the number of problems you have to deal with.

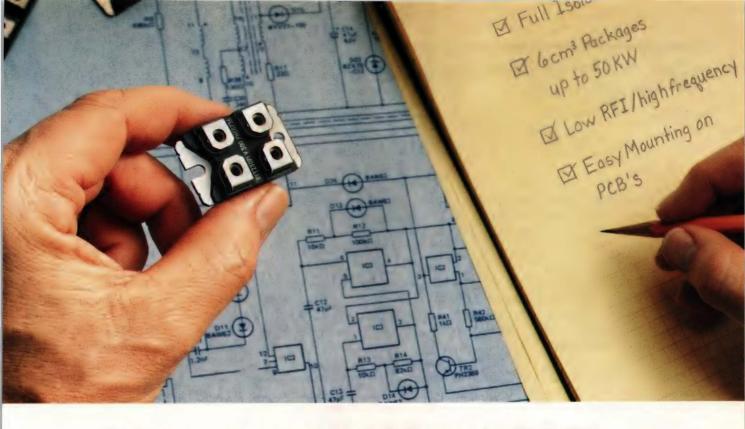
Recently, we had so many nagging little troubles with band-gap reference circuits at National, that I decided (unilaterally) to declare myself, "Czar of Band Gaps." The main rules were that (a) all successful bandgap circuits should be registered with the Czar so that we could keep a log book of successful circuits; (b) all unsuccessful circuits, their reasons for failure, and the fixes for the failures should likewise be logged in with the Czar so that we could avoid repeating old mistakes; and (c) all new circuits should be submitted to the Czar to allow him to spot any old errors. So far, we think we've found over 50% of the possible errors, and we're gaining. In addition, we have added Czars for start-up circuits and for trim circuits, and we are considering other czardoms. It's a bit of a game, but it's also a serious business to use a game to try to prevent expensive errors.

I haven't always been a good troubleshooter, but my "baptism of fire" occurred quite a few years ago. I had designed a group of modular data converters. We had to ship 525 of them, and some foolish person had bought only 535 pc boards. When less than half of the units worked, I found myself in the troubleshooting business because nobody else could imagine how to repair them. I discovered that I needed my best-triggering scope and my best DVM. I burned a lot of midnight oil. I got half-a-dozen copies each of the schematic and the board layout. I scribbled notes on them—

of what the dc voltages ought to be, what the correct ac waveforms looked like, and where I could best probe the key waveforms. I made little lists of, "If this frequency is twice as fast as normal, look for Q47 to be damaged, but if the frequency is 1/10 normal, look for a short on bus B." I learned where to look for solder shorts, hairline opens, cold-soldered joints, and intermittents. I diagnosed the problems and sent each unit back for repair with a neat label of what to change. When they came back, did they work? Some did—and some still had another level or two of problems. That's the Onion Syndrome: You peel off one layer, and you cry; you peel off another layer and cry some more . . . By the time I was done, I had fixed all but four of the units, and I had gotten myself one hell of a good education about troubleshooting.

After I found a spot of trouble, what did I do about it? First of all, I made some notes to make sure that the problem really was fixed when the offending part was changed. Then I sent the units to a good, neat technician who did precise repair work—much better than a slob like me would do. Lastly, I sent memos to the manufacturing and QC departments to make sure that the types of parts that had proven trouble-some were not used again, and I confirmed the changes with ECOs (engineering change orders). It is important to get the paperwork scrupulously correct, or the alligators will surely circle back to vex you again.

I once heard of a similar situation where an insidious problem was causing nasty reliability problems with a



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### Clues are where you find them; they should be saved and savored.

batch of modules. The technician had struggled to find the solution for days. Finally, when the technician went out for lunch, the design engineer went to work on the problem. When the technician came back from lunch, the designer told him, "I found the problem; it's a mismatch between Q17 and R18. Write up the ECO, and when I get back from lunch I'll sign it." Unfortunately, the good rapport between the engineer and the technician broke down: there was some miscommunication. The technician got confused and wrote up the ECO with an incorrect version of what should be changed. When the engineer came back from lunch, he initialled the ECO without really reading it and left for a two-week vacation.

When he came back, the modules had all been "fixed," potted, and shipped, and were starting to fail out in the field. A check of the ECO revealed the mistake—too late. The company went bankrupt. It's a true story and a painful one. Don't get sloppy with your paperwork; don't let it happen to you.

#### Troubleshooting by phone—a tough challenge

These days, I do quite a bit of troubleshooting by telephone. When my phone rings, I never know if a customer will be asking for simple information or submitting a routine application problem, a tough problem, or an insoluble problem. Often I can give advice just off the top of my head because I know how to fix what is wrong. At other times, I have to study a while before I call back. Sometimes, the circuit is so complicated that I tell the customer to mail or transmit the schematic to me. On rare occasions, the situation is so hard to analyze that I tell the customer to put the circuit in a box with the schematic and a list of the symptoms and ship it to me.

Sometimes the problem is just a misapplication. Sometimes parts have been blown out and I have to guess what situation caused the overstress. Here's an example: In June, a manufacturer of dental equipment complained of an unacceptable failure rate on LM317 regulators. After a good deal of discussion, I asked, "Where did these failures occur?" Answer: North Dakota. "When did they start to occur?" Answer: In February. I put two and two together and realized that the climate in a dentist's office in North Dakota in February is about as dry as it can be and is conducive to very high electrostatic potentials. The LM317 is normally safe against electrostatic potentials as high as 3 or 4 kV, but walking across a carpeted floor in North Dakota in February can generate even higher

voltages. To make matters worse, the speed-control rheostat for this dental instrument was right out in the handle. The wiper and one end of the rheostat were wired directly to the LM317's ADJUST pin; the other end of the rheostat was connected to ground by way of a  $1-k\Omega$  resistor located near the IC.

The problem was easily solved by placing the resistor in series with the IC's ADJUST pin and relocating it to the instrument's handle. By moving the resistor and connecting the rheostat wiper to ground, much less current would take the path to the ADJUST pin and the diffused resistors on the chip would not be damaged or zapped by the current surges.

A similar situation occurs when you get a complaint from Boston in June, "Your op amps don't meet spec for bias current." The solution is surprisingly simple: Usually a good scrub with soap and water works better than any other solvent to clean off the residual contaminants that cause leakage under humid conditions.

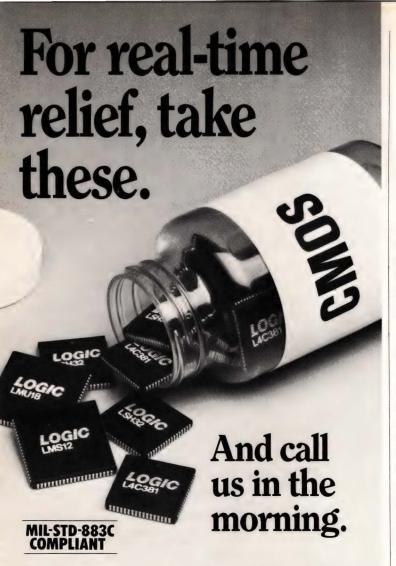
#### When computers replace troubleshooters, look out

Now, let's think—what needs troubleshooting? Circuits? Television receivers? Cars? People? Surely doctors have a lot of troubleshooting to do—they listen to symptoms and try to figure out the solution. What is the natural temptation? Letting a computer do all the work! After all, a computer is quite good at listening to complaints and symptoms, asking wise questions, and proposing a wise diagnosis. Such a computer system is called an expert system—part of the general field of artificial intelligence. But, I am still in favor of genuine intelligence.

I won't argue that the computer isn't a natural for this job; it will probably be cost effective, and it won't be absent minded. But, I am definitely nervous because if computers do all the routine work, soon there will be nobody left to do the thinking when the computer gives up and admits it is stumped. I sure hope we don't let the computers leave the smart troubleshooting people without jobs, whether the object is circuits or people.

My concern is shared by Dr. Nicholas Lembo, the author of a study on how physicians make diagnoses, which was published in the *New England Journal of Medicine*. He recently told the *Los Angeles Times*, "With the advent of all the new technology, physicians aren't all that much interested (in bedside medicine) because they can order a \$300 to \$400 test to tell them something they could have found by listening." An editorial accompanying the study commented sadly:





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no confidence in their own ability to make worthwhile bedside diagnoses." Troubleshooting is still an art, and it is important to encourage those artists. No problems? No problem . . . just wait

"The present trend . . . may soon leave us with a whole new generation of young physicians who have

Now, let's skip ahead and presume we have all the necessary tools and the right receptive attitude. What else do we need? What is the last missing ingredient? That reminds me of the little girl in Sunday School who was asked what you have to do to obtain forgiveness of sin. She shyly replied, "First you have to sin." So, to do troubleshooting, first you have to have some trouble. But, that's usually not a problem; just wait a few hours, and you'll have plenty. Murphy's Law implies that if you are not prepared for trouble, you will get a lot of it. Conversely, if you have done all your homework, you may avoid most of the possible trouble.

I've tried to give you some insights on the philosophy of how to troubleshoot. Don't believe that you can get help on a given problem from only one specific person. In any particular case, you can't predict who might provide the solution. Conversely, when your buddy is in trouble and needs help, give it a try-you could turn out to be a hero. And, even if you don't guess correctly, when you do find out what the solution is, you'll have added another tool to your bag of tricks.

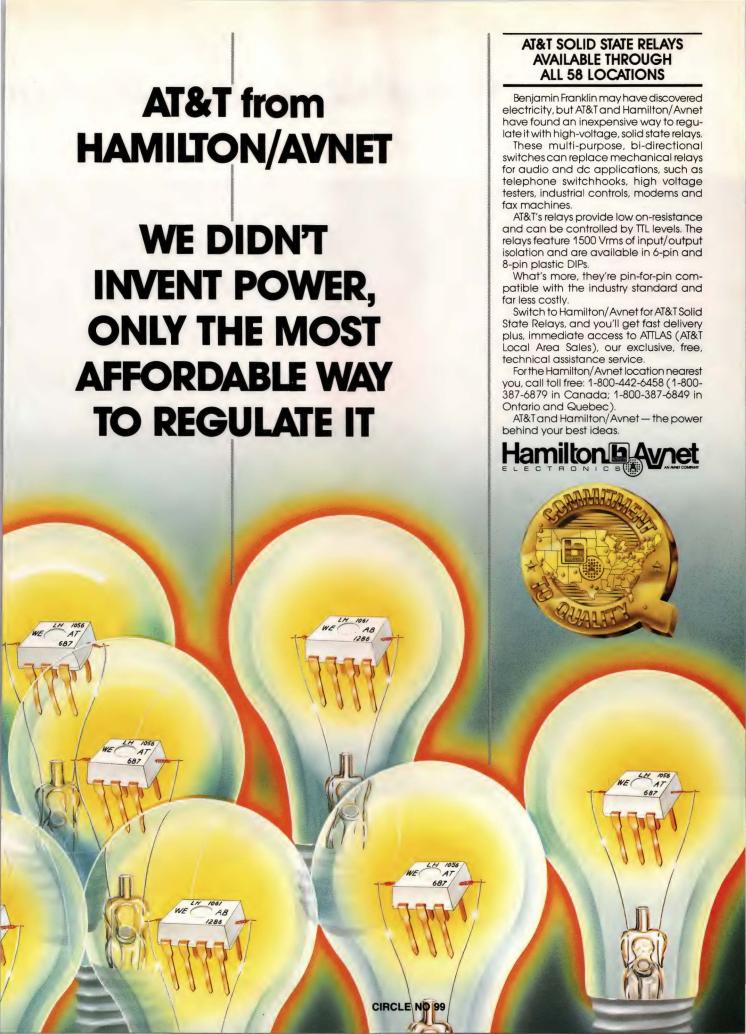
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#### Acknowledgment

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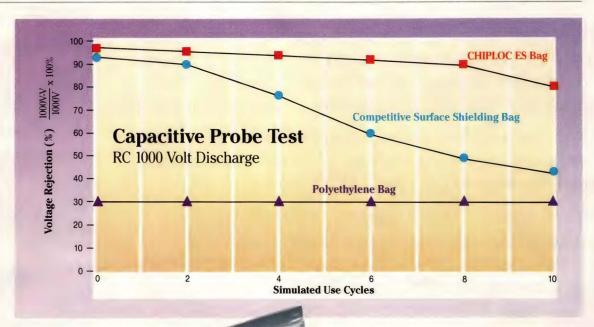
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# Current-feedback amplifiers benefit high-speed designs

Current-feedback amplifiers offer significant advantages over conventional highspeed op amps. Like the conventional devices, however, they exhibit nonideal behavior, so some circuit configurations require special care. Understanding the circuit topology will help you achieve successful designs.

Sergio Franco, San Francisco State University

Amplifiers based on the current-feedback topology are now more widely available than ever. They offer designers of high-speed systems some key advantages over conventional op amps (Ref 1). First, you can independently vary their gain and bandwidth; second, they have a virtually unlimited slew rate. The absence of slew-rate limiting not only allows for faster settling times, but also eliminates slew-rate-related nonlinearities such as intermodulation distortion. Thus, current-feedback amps are attractive for use in high-quality audio-amplifier applications.

These two advantages are the result of the amps' current-mode operation, which has long been recognized as inherently faster than voltage-mode operation. The effects of stray inductance in a circuit are usually less severe than those of stray capacitance (or the

Miller effect), and bipolar transistors can switch currents much more rapidly than voltages. Current amplifiers must still have a voltage output, however, and op-amp designers sidestep some of the problems associated with voltage-mode operation by using gain configurations such as common-collector and cascode configurations, which provide immunity to the Miller effect. Further, thanks to manufacturing processes that ensure symmetrical npn- and pnp-transistor switching characteristics, manufacturers can now create monolithic op amps that achieve high speeds that were previously available only from hybrid devices.

In many ways, current-feedback amps are very similar to their conventional op-amp counterparts (Ref 2). For a standard circuit configuration, you derive the transfer functions for current-feedback amplifiers in the same way that you do for conventional op amps. However, if you're going to use a current-feedback amp in your design, you'll have some other considerations to make. For example, you'll have to decide how to use reactive feedback elements, which cause oscillation when connected directly from output to input. Thus, before designing with current-feedback amps, you need a thorough understanding of the current-feedback architecture.

The easiest way to understand the advantages of the current-feedback topology is to compare it with the architecture of a conventional op amp (**Ref 3**). The conventional op amp consists of a high-input-impedance differential stage followed by additional gain stages, Current-feedback amps don't involve a gain-bandwidth tradeoff, and they have virtually no slew-rate limiting.

the last of which is a low-output-impedance stage. The op amp's transfer characteristic is:

$$V_{OUT} = a(jf)V_{D}, \tag{1}$$

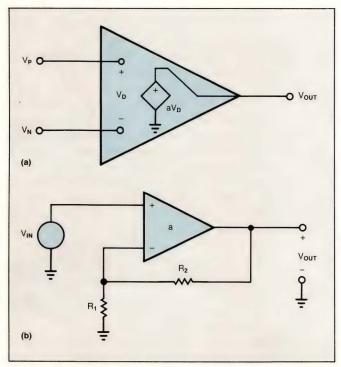
where  $V_{OUT}$  is the output voltage;  $V_D = V_P - V_N$  is the differential input voltage; and a(jf), a complex function of frequency (f), is the open-loop gain (Fig 1a). Connecting an external resistor network as shown in Fig 1b creates a feedback path; the voltage signal derived from the output is applied to the noninverting input. You can solve for  $V_D$  to obtain

$$V_D = V_{IN} - \frac{R_1}{R_1 + R_2} V_{OUT}.$$
 (2)

By substituting Eq 2 for  $V_D$  in Eq 1 and solving for the ratio  $V_{OUT}/V_{IN}$ , you obtain the familiar closed-loop transfer characteristic for a noninverting amplifier:

$$A(jf) = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)}, \quad (3)$$

where  $1 + R_2/R_1$  is the ideal gain value, and



**Fig 1—The circuit model** of a conventional op amp includes a differential input stage and a gain stage (a); resistive feedback configures the op amp as a noninverting amplifier (b).

$$T(jf) = \frac{a(jf)}{1 + R_0/R_1}$$
 (4)

represents the loop gain. The denominator of the loop-gain expression is called the noise gain. In this case, it's equal to  $1+R_2/R_1$ . Note that in this example, the noise gain just happens to be equal to the ideal closed-loop gain. It's important not to confuse the two.

#### Loop gain determines stability

Eq 4 represents the loop gain, because if you break the loop as shown in Fig 2a and inject a test signal  $(V_X)$  with  $V_{IN}$  suppressed, the circuit will first attenuate  $V_X$  to produce  $V_N = V_X/(1 + R_2/R_1)$ , and then amplify  $V_N$  to produce  $V_{OUT} = -aV_N$ . Hence, the gain that a signal experiences when it goes around the loop is  $V_{OUT}/V_X = -a/(1 + R_2/R_1)$ . The negative of this ratio represents the loop gain, T.

The loop gain provides a measure of how close A is

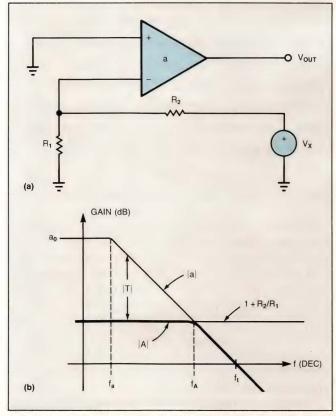


Fig 2—You can find the loop gain by injecting a signal  $V_X$  with  $V_{IN}$  grounded and solving for  $V_{OUT}/V_X$  (a); the loop gain is, graphically, the difference between the open-loop curve and the noise-gain curve.

to the ideal value of  $1+R_2/R_1$ . The larger the value of T, the better. To help the user achieve high loop gains over a wide range of closed-loop gains, op-amp manufacturers strive to make the open-loop gain (a) as large as possible. Consequently,  $V_D$  will assume extremely small values, because  $V_D = V_{OUT}/a$  (see Eq 1). As the value of the open-loop gain approaches infinity,  $V_D$  approaches zero; that is, the value of  $V_N$  approaches that of  $V_P$ . This fact is the basis of the familiar op-amp rule: When it's operated with negative feedback, an op amp will ideally provide whatever output voltage and current are needed to force  $V_N$  to equal  $V_P$ .

#### Op amps require a familiar tradeoff

In practice, op amps can physically realize large open-loop gains only over a limited frequency range. Beyond this range, the gain rolls off with respect to frequency because of the op amps' internal frequency compensation. Most op amps are designed for a constant rolloff of -20 dB/decade, so the open-loop response can be expressed as

$$a(jf) = \frac{a_0}{1 + j(f/f_a)},$$
 (5)

where  $a_0$  represents the dc gain and  $f_a$  is the -3-dB frequency of the open-loop response.

By substituting Eq 5 for a(jf) in Eq 4 and then substituting Eq 4 for T(jf) in Eq 3, and recognizing the fact that  $(1 + R_2/R_1)/a_0 < 1$ , you can obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)},$$
 (6)

where

$$f_{A} = \frac{f_{t}}{1 + R_{2}/R_{1}} \tag{7}$$

represents the closed-loop bandwidth and  $f_t = a_0 f_a$  represents the open-loop unity-gain frequency—that is, the frequency at which  $k = k \cdot 1$  is equal to 1. For instance, the 741 op amp has an  $f_t$  equal to 1 MHz.

Eq 7 reveals the familiar gain-bandwidth tradeoff. As you raise the  $R_2/R_1$  ratio to increase the closed-loop gain, you decrease its bandwidth. Moreover, the loop gain also decreases, leading to a greater closed-loop-gain error.

You can see this tradeoff by plotting the frequency

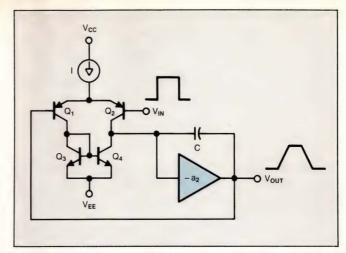


Fig 3—As shown in this simplified slew-rate model, there is limited current to charge and discharge C when the transconductance stage saturates.

response on a graph. From Eq 4,  $\Pi_{dB} = |a|_{dB} - (1 + R_2/R_1)_{dB}$ . Thus, you can think of the loop gain as the difference between the open-loop gain and the noise gain (Fig 2b). The intersection of the two curves is the crossover frequency or -3-dB point, at which T has a magnitude of 1 and a phase shift of  $-90^{\circ}$ .

As you increase the closed-loop gain, the noise-gain curve shifts upward, thus reducing the loop gain. Also, the intersection point will move up the lal curve, thus decreasing the closed-loop bandwidth. Clearly, the circuit with the widest bandwidth and the highest loop gain is also the one with the lowest closed-loop gain. This circuit is the voltage follower, for which  $R_2/R_1\!=\!0$ , so  $A\!=\!1$  and  $f_A\!=\!f_t$ .

#### Slew-rate limiting is also a factor

To fully characterize the dynamic behavior of an op amp, you also need to know its transient response. In many applications, the dynamic parameter of greatest concern is the settling time, a characteristic in which slew-rate limiting plays an important role. If you apply a small voltage step to an op amp connected as a unity-gain voltage-follower, the amp's dynamic behavior will be similar to that of an RC network. The input step,  $\Delta V_{IN}$ , will cause the output to undergo an exponential transition with a magnitude of  $\Delta V_0 = \Delta V_{IN}$  and a time constant of  $\tau = 1/(2\pi f_t)$ . For the 741 op amp,  $\tau = 1/(2\pi \times 10^6) \approx 170$  nsec.

The rate at which the output changes with time is highest at the beginning of the exponential transition, when its value is  $\Delta V_{OUT}/\tau$ . Increasing the step magnitude increases this initial rate of change, until the latter saturates at a value called the slew rate (SR). This fact is due to the limited ability of the internal circuitry to charge and discharge the compensation capacitor as well as capacitive loads.

The input stage of a typical op amp is a transconductance block consisting of differential pair  $Q_1$ - $Q_2$ and current mirror  $Q_3$ - $Q_4$  (Fig 3). The remaining stages, considered together, comprise an integrator block consisting of an inverting amplifier and the comBefore designing with current-feedback op amps, you should thoroughly understand their architecture; some circuits require special attention.

pensation capacitor, C. Slew-rate limiting occurs when the transconductance stage saturates, so all the current available to charge and/or discharge C is the bias current (I) of this stage.

For example, for the 741 op amp, I=20  $\mu A$  and C=30 pF, so SR=I/C=0.67 V/ $\mu sec$ . The step magnitude corresponding to the onset of slew-rate limiting is such that  $\Delta V_{IN}/\tau$ =SR; that is,  $\Delta V_{IN}$ =SR  $\times \tau$ =(0.67 V/ $\mu sec$ )  $\times$  (170 nsec)=116 mV. As long as the step is less than 116 mV, a 741 op amp configured as a voltage follower will respond with an exponential transition governed by  $\tau$ =170 nsec, whereas for a greater input step the output will slew at a constant rate of 0.67 V/ $\mu sec$ .

#### Current-feedback-amp architecture

The architecture of the current-feedback amp differs from the conventional op amp in two respects (Fig 4). First, the current-feedback amp's input stage is a unity-gain voltage buffer connected across the inputs of the op amp. Its function is to force  $V_N$  to follow

V<sub>P</sub> O V<sub>OUT</sub>

V<sub>N</sub> O V<sub>OUT</sub>

V<sub>N</sub> O V<sub>OUT</sub>

V<sub>OUT</sub>

R<sub>1</sub>

R<sub>1</sub>

R<sub>2</sub>

R<sub>2</sub>

R<sub>3</sub>

Fig 4—The circuit model of a current-feedback amp includes a unity-voltage-gain input buffer and a transimpendance block (a). Connected as a noninverting amplifier (b), the current-feedback amp looks identical to its conventional-op-amp counterpart.

 $V_P$ , very much as negative feedback forces  $V_N$  to follow  $V_P$  in a conventional op amp. However, because of the low output impedance of this buffer, current can easily flow in or out of the inverting input. During normal operation, this current is extremely small.

Second, a current-feedback amp has a transimpedance amplifier, which senses the current delivered by the buffer to the external feedback network and produces an output voltage  $V_{\rm OUT}$  such that

$$V_{OUT} = z(jf)I_N, (8)$$

where z(jf) represents the transimpedance gain of the amplifier and  $I_N$  represents the output current of the inverting input.

To fully appreciate the inner workings of the currentfeedback amp, you need to examine the simplified cir-

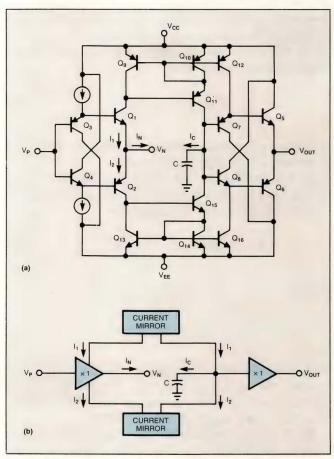


Fig 5—When you look into the actual circuit inside a current-feedback amp, you'll find both push-pull and Darlington transistor configurations at the input (a) (diagram courtesy Comlinear Corp). The block diagram of the circuit (b) shows the current-feedback amp's basic features.

cuit diagram of Fig 5a. The input buffer consists of transistors  $Q_1$  through  $Q_4$ .  $Q_1$  and  $Q_2$  form a low output-impedance push-pull stage.  $Q_3$  and  $Q_4$  provide  $V_{BE}$  compensation for the push-pull pair and have a Darlington function, which raises the input impedance.

Summing the currents at the inverting node yields  $I_1 - I_2 = I_N$ , where  $I_1$  and  $I_2$  are the push-pull transistor currents. Two Wilson current mirrors, consisting of transistors  $Q_9$  through  $Q_{11}$  and  $Q_{13}$  through  $Q_{15}$ , reflect these currents and recombine them at a common node, whose equivalent capacitance to ground is designated "C" in Fig 5.

#### A closer look at the internal circuit

By mirror action, the current through this capacitance is  $I_C = I_1 - I_2$ ; that is,  $I_C = I_N$ . The voltage developed by C in response to this current is then conveyed to the output by a second buffer, which consists of  $Q_5$  through  $Q_8$ . Fig 5b's block diagram summarizes the salient features of the current-feedback amp.

When the amplifier loop is closed, as in Fig 4b, and an external signal attempts to imbalance the two inputs, the input buffer will begin sourcing (or sinking)

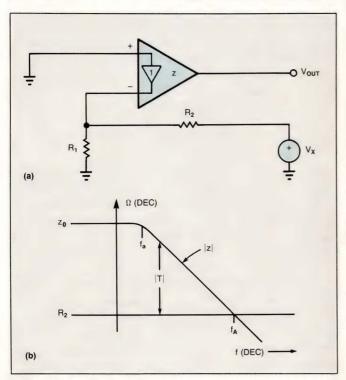


Fig 6—As with conventional op amps, you can use this test circuit (a) to determine the loop gain. The loop gain is represented graphically as the difference between the open loop gain,  $\bowtie$ , and the noisegain curve,  $R_2$  (b).

an imbalance current,  $I_N$ , to the external feedback network. The Wilson mirrors convey this imbalance to C, causing  $V_{\rm OUT}$  to swing in the positive (or negative) direction until the imbalance is neutralized via the negative feedback loop. Thus,  $I_N$  plays the role of error signal in the system.

To obtain the closed-loop transfer characteristic, refer again to Fig 4b. By summing the currents at the inverting node, you obtain

$$I_{N} = \frac{V_{N}}{R_{1}} - \frac{V_{OUT} - V_{N}}{R_{2}}.$$
 (9)

Because the buffer ensures that  $V_N = V_P = V_{IN}$ , you can rewrite Eq 9 as:

$$I_{N} = \frac{V_{IN}}{R_{I} \| R_{2}} - \frac{V_{OUT}}{R_{2}}, \tag{10}$$

which confirms that the feedback signal,  $V_{OUT}/R_2$ , is now in the form of a current. By substituting Eq 10 for  $I_N$  in Eq 8, and solving for the ratio  $V_{OUT}/V_{IN}$ , you obtain

$$A(jf) = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)},$$
 (11)

where A(jf) represents the closed-loop gain of the circuit, and

$$T(jf) = \frac{z(jf)}{R_2}$$
 (12)

represents the loop gain. As for a conventional op amp, this terminology is derived from the fact that if you break the loop as shown in Fig 6a, and inject a test voltage ( $V_X$ ) with  $V_{IN}$  suppressed, the circuit will first convert  $V_X$  to  $I_N = -V_X/R_2$  and then convert  $I_N$  to  $V_{OUT} = zI_N$ , so  $T = z/R_2$ , as expected.

To ensure that the circuit will have substantial loop gain, and, therefore, minimal closed-loop gain error, manufacturers strive to make z as large as possible in relation to the expected values of  $R_2$ . Consequently, because  $I_N = V_{OUT}/z$ , the inverting-input current will be very small, even though this input is a low-impedance node because of the buffer. As a current-feedback amp's open-loop gain (z) approaches infinity, its  $I_N$  approaches 0, so the amplifier will provide whatever output voltage and current are needed to drive  $I_N$  to zero. Thus, the conventional op-amp conditions,

The magnitude of an op amp's loop gain determines the closed-loop-gain error, and its phase determines stability.

 $V_N\!=\!V_P$  and  $I_N\!=\!I_P\!=\!0$ , hold for current-feedback amps as well.

#### No gain-bandwidth tradeoff

The transimpedance gain of a practical currentfeedback amp rolls off with frequency according to

$$z(jf) = \frac{z_0}{1 + j(f/f_a)},$$
 (13)

where  $z_O$  is the dc value of the transimpedance gain and  $f_a$  is the frequency at which rolloff begins. For instance, the data sheets of Comlinear's CLC401 current-feedback amp state that  $z_O{\approx}710~k\Omega$  and  $f_a{\approx}350~kHz.$ 

By substituting Eq 13 for z(jf) in Eq 12, and then substituting Eq 12 for T(jf) in Eq 11, and recognizing the fact that  $R_2/z_0<1$ , you obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)}, \qquad (14)$$

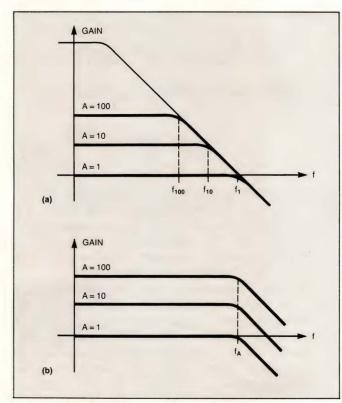


Fig 7—The most significant advantage that current-feedback amps have over conventional op amps can be seen in this simple frequency-response plot. Note the gain-bandwidth tradeoff for conventional op amps in **a** and the absence of such a compromise in **b**.

where

$$f_A = \frac{z_0 f_a}{R_2} \tag{15}$$

represents the closed-loop bandwidth. When  $R_2$  is in the kilohm range,  $f_A$  is typically in the 100-MHz range. The noise-gain curve is now simply  $R_2$ , and  $f_A$  can be represented graphically as the frequency at which the  $R_2$  curve meets the  $\bowtie$  curve (**Fig 6b**).

These closed-loop-gain expressions are formally identical to those for the conventional op amp Eqs 6 and 7. However, the bandwidth now depends only on  $R_2$  rather than on the closed-loop gain  $1 + R_2/R_1$ . Consequently, you can use  $R_2$  to select the bandwidth and  $R_1$  to select the gain. Fig 7 highlights these frequency-response differences between current-feedback amps and conventional op amps.

The other major advantage of current-feedback amps is their inherent absence of slew-rate limiting. This feature is due to the fact that the current available to charge the internal capacitance at the onset of a step is now proportional to the step, regardless of its size. Indeed, applying the step  $\Delta V_{IN}$  induces, according to Eq 10, an initial current imbalance  $I_N = \Delta V_{IN}/(R_1\tau R_2)$ , which the Wilson mirrors then convey to the capacitor. The initial rate of charge is, therefore,

$$\begin{split} &I_{C}/C = I_{N}/C \\ &= \Delta V_{IN}/((R_{1}\tau R_{2})C) \\ &= (\Delta V_{IN}(1+R_{2}/R_{1}))/(R_{2}C) \\ &= \Delta V_{OUT}/(R_{2}C), \end{split}$$

which indicates an exponential output transition in which the time constant,  $\tau$ , is equal to R<sub>2</sub>C. Like the frequency response, then, the transient response is governed by R<sub>2</sub> alone, regardless of the closed-loop gain. When R<sub>2</sub> is in the kilohm range and C is in the picofarad range,  $\tau$  will be in the nanosecond range.

The rise time is defined as the amount of time,  $t_r$ , that it takes for the output to swing from 10% to 90% of the step size. For an exponential transition,  $t_r = \tau \times \ln(0.9/0.1) = 2.2\tau$ . For example, the CLC401 has a  $t_r$  equal to 2.5 nsec for a 2V output step, indicating an effective  $\tau$  of 1.14 nsec. The time it takes for the output to settle to within 0.1% of the final value is  $t_s = \tau \times \ln$  1000, which is approximately  $7\tau$ . For the CLC401, therefore,  $t_s$  is approximately 8 nsec, which is in reasonable agreement with the data-sheet value of 10 nsec.

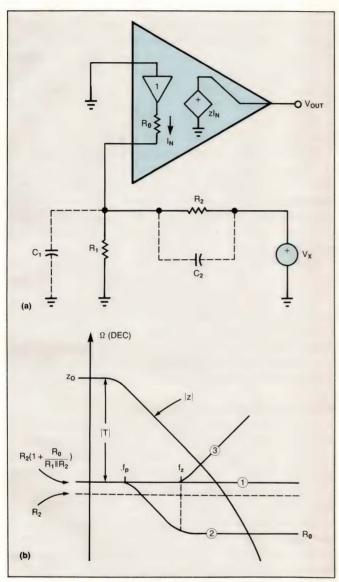


Fig 8—By using the more real-world circuit model in a, you can determine the effects, shown in b, of  $R_O$  (curve 1), feedback capacitance (curve 2), and input capacitance (curve 3).

So far, this analysis indicates that once  $R_2$  has been set, the dynamics of the amplifier are unaffected by the closed-loop-gain setting. In practice, you'll find that a current-feedback amp's bandwidth and rise time do vary somewhat with gain, though not as drastically as do those of conventional op amps. The main cause of this nonideal behavior is the input buffer's nonzero output impedance ( $R_0$ ), which alters the loop gain and, hence, the closed-loop dynamics.

As Fig 8a shows, the circuit first converts  $V_X$  to a current,  $I_{R2} = V_X/(R_2 + R_1 \tau R_0)$ , and then divides  $I_{R2}$ 

to produce  $I_N = -I_{R_2}R_1/(R_1 + R_0)$ . Finally, it converts  $I_N$  to the voltage  $V_{OUT} = V_N$ . Eliminating  $I_{R_2}$  and  $I_N$  and letting T equal  $-V_{OUT}/V_X$  yields  $T = z/Z_2$ , where

$$Z_2 = R_2 \left( 1 + \frac{R_0}{R_1 || R_2} \right). \tag{16}$$

Thus, the effect of  $R_O$  is to increase the noise gain from  $R_2$  to  $R_2(1+R_O/(R_1\tau R_2))$  (Fig 8b, curve 1.) Consequently, both the bandwidth and the rise time will be reduced by a proportional amount.

You can replace  $R_2$  in Eq 15 with  $Z_2$  from Eq 16, and, after simple manipulation, obtain

$$f_{A} = \frac{f_{t}}{1 + \frac{R_{0}}{R_{2}} \left(1 + \frac{R_{2}}{R_{1}}\right)},$$
 (17)

where  $f_t = z_O f_a/R_2$  represents the extrapolated value of  $f_A$  in the limit  $R_O \rightarrow 0$ . Eq 17 indicates that the bandwidth reduction caused by  $R_0$  will be more pronounced at high closed-loop gains. For example, suppose a current-feedback amp has  $R_0 = 50\Omega$ ,  $R_2 = 1.5 \text{ k}\Omega$ , and  $f_t = 100 \text{ MHz}$ , so  $f_A = 10^8/(1 + (50/1500)A_O) = 10^8/(1 + A_O/30)$ , where  $A_O = 1 + R_2/R_1$ . Then, the bandwidths corresponding to  $A_O = 1$ ,  $A_O = 10$ , and  $A_O = 100$  are, respectively, 96.8 MHz, 75.0 MHz, and 23.1 MHz. Note that these values still compare favorably with those of a conventional op amp, whose bandwidth would be reduced, respectively, by 1, 10, and 100.

If you wish, you can predistort the external resistance values to compensate for the bandwidth reduction at high gains. By solving for  $R_2$  in Eq 17, you can obtain the required value of  $R_2$  for a given bandwidth  $(f_A)$  and gain  $(A_O)$ , which is

$$R_2 = \frac{z_0 f_a}{f_A} - R_0 A_0, \tag{18}$$

while the required value of R<sub>1</sub> for gain A<sub>0</sub> is

$$R_1 = \frac{R_2}{A_0 - 1}. (19)$$

For example, suppose you want the above amplifier to retain its 100-MHz bandwidth at a closed-loop gain of 10. When  $R_2 = 1.5~k\Omega$ , this device has a  $z_0 f_a/R_2$  equal to 100 MHz, so it follows that  $z_0 f_a = 10^8 \times 1500 = 1.5 \times 10^{11} \Omega \times Hz$ . Then, Eqs 18 and

In current-feedback amps, you can use one of the feedback resistors to set the gain, and the other to set the closed-loop bandwidth.

19 yield  $R_2 = (1.5 \times 10^{11}/10^8) - (50 \times 10) = 1 \text{ k}\Omega$ , and  $R_1 = 1000/(10-1) = 111\Omega$ , respectively.

#### Current-feedback amps have higher-order poles

In addition to the dominant pole at f<sub>a</sub>, the open-loop response of a practical current-feedback amp also has poles above the crossover frequency. As Fig 8b shows, the effect of these poles is to cause a steeper gain rolloff at higher frequencies, further reducing the closed-loop bandwidth. Moreover, the additional phase shift caused by these poles decreases the phase margin somewhat, thus causing a small amount of peaking in the frequency response and creating some ringing in the transient response.

Like the real current-feedback-amp bandwidth characteristics, the transient response also strays from the ideal. The rise time of a practical current-feedback amp increases somewhat with the step size, primarily because of the transistor's current-gain degradation at high current levels. For instance, the rise time of the CLC401 changes from 2.5 to 5 nsec as the step size changes from 2 to 5V. Despite their second-order limitations, current-feedback amps provide dynamics superior to those of conventional op amps.

#### Consider other feedback configurations

This discussion has focused so far on the noninverting configuration, but you can use current-feedback amps in most other resistive feedback configurations, such as the inverting amplifier, the summing and difference amplifier, current-to-voltage and voltage-to-current converters, and KRC active filters (Ref 3).

You should take special care, however, with circuits in which the feedback network includes reactive elements, whether they're intentional or parasitic. Con-

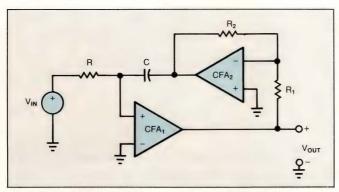


Fig 9—To implement an integrator, you must use circuit configurations that involve indirect feedback, such as this actively compensated current-feedback integrator.

sider first the effect of feedback capacitance ( $C_2$ ) in parallel with  $R_2$  in the basic circuit of **Fig 8a**. By replacing  $R_2$  in **Eq 16** with  $Z = R_2 \tau (1/sC_2)$ , you obtain a noise gain of  $Z_2 = Z(1 + R_0/(R_1 \tau Z))$ . After expanding the equation (and performing some algebraic manipulation), you'll find that the noise-gain curve now has a pole at  $f_p = 1/(2\pi R_2 C_2)$ , and a zero at  $f_z = 1/(2\pi (R_0 \tau R_1 \tau R_2) C_2)$ , as curve 2 of **Fig 8b** shows.

This new pole and zero move the crossover frequency or intersection point into the region where the loop gain, T, will have increased negative phase shift (remember that there are higher-order poles in the open-loop transfer function). It is the phase shift of the loop-gain curve at the crossover frequency that deter mines amplifier stability. If the overall shift reaches  $-180^{\circ}$  at that frequency, then T=-1, and the circuit will oscillate. Even if the phase shift fails to reach  $-180^{\circ}$ , the closed-loop response may still exhibit intolerable peaking and ringing. Hence, when you use current-feedback amps, you must avoid applying direct capacitive feedback between the output and the input. To minimize the effect of stray feedback capacitances, manufacturers often provide  $R_2$  internally.

#### Use unique integrator topologies

To synthesize the integrator function in current-feedback form, you must use configurations that don't have direct capacitance between the output and the inverting input. (The integrator function provides the basis for dual-integrator-loop filters and oscillators as well as for other popular circuits.) One possibility is to use the Deboo integrator (Ref 3), which belongs to the class of KRC filters. It has a drawback, however: If you desire lossless integration, you must make sure the circuit resistances are tightly matched.

The alternative circuit shown in Fig 9 provides indirect feedback and also features active compensation, a highly desirable feature for coping with Q-enhancement problems in dual-integrator-loop filters (Ref 3). By using standard op-amp-analysis techniques, you can see that the unity-gain frequency of this integrator is  $f_0 = (R_2/R_1)/(2\pi RC)$ . The availability of current-feedback amps in dual monolithic packages, such as the OP-260 from Precision Monolithics, makes this circuit cost-effective.

#### Compensate for stray input capacitance

Next, consider the effect of input capacitance  $(C_1)$  in parallel with  $R_1$  in the basic circuit of Fig 8a. By replacing  $R_1$  in Eq 17 with Z, and letting  $Z = R_1 \tau (1/2)$ 



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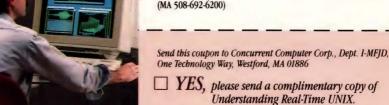
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Beware of the instability problems that direct capacitive feedback and stray input capacitance can cause.

sC<sub>1</sub>), you obtain a noise gain of  $Z_2 = R_2(1 + R0/(Z\tau R_2))$ . After expanding the equation and performing more algebraic manipulation, you find that, as curve 3 of **Fig** 8b shows, the noise-gain curve now has a zero at

$$f_z = 1/(2\pi(R_0\tau R_1\tau R_2)C_1)$$
.

Again, recall that T is equal to  $\bowtie$  in decibels *minus* the noise gain in decibels. Likewise, the phase of T is equal to the phase of Z minus the phase of the noisegain curve. So, the positive phase shift contributed by the new zero in the noise-gain curve looks like negative phase shift to T. If  $C_1$  is sufficiently large, the phase of T at the crossover frequency will again approach  $-180^\circ$ , placing the circuit on the verge of instability. This fact is of particular concern in current-mode-DAC output buffering, where  $C_1$  is the output capacitance of the DAC, typically in the range of a few tens to a few hundreds of picofarads, depending on the DAC type.

As with a conventional op amp, you can stabilize the current-feedback amp by using feedback capacitance (C<sub>2</sub>) to introduce sufficient negative phase shift in the noise-gain curve (positive phase shift to T), thus compensating for the effect of the input capacitance (C<sub>1</sub>).

For a phase margin of 45°, choose the value of  $C_2$  so that the noise-gain pole,  $f_p=1/(2\,R_2C_2)$ , coincides with the crossover frequency,  $f_A$  (Fig 10a). Using linearized Bode-plot reasoning (Ref 3), also known as straight-line approximation, you find that:

$$f_A = (z_O f_a f_z / (R_O + R_1))^1$$

where  $f_z = 1/(2\pi(R_0\tau R_2)C_1)$ . Setting  $f_p = f_A$  yields

$$C_2 = \left[ \frac{R_0}{2\pi R_2 z_0 f_a} C_1 \right]^{\frac{1}{2}}.$$
 (20)

To cope with impractically low values of  $C_2$ , it's convenient to drive  $C_2$  with a voltage divider as in Fig 10b; this action will scale the value of  $C_2$  to a more practical value:

$$C_{c} = \left(1 + \frac{R_{B}}{R_{A}}\right)C_{2}. \tag{21}$$

(Note that this circuit configuration will provide an additional zero in the noise-gain curve that lies to the right of the compensation pole,  $f_A$ , in (Fig 10a).

For this technique to be effective, RB must be much

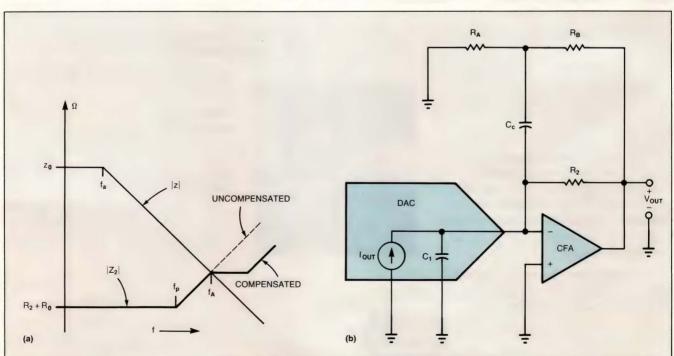


Fig 10—To compensate for input capacitance, you should add a pole at  $f_A$  (a) that will add positive phase shift to the loop gain, thereby stabilizing the circuit. Use the circuit in b to achieve practical compensation-capacitor values.

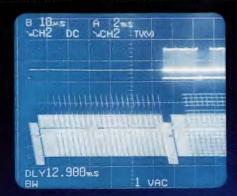
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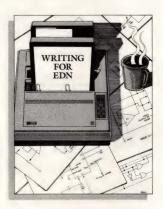
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less than  $R_2$ . For example, suppose that a DAC in which  $C_1$  equals 100 pF feeds the current-feedback amp considered earlier. Eq 20 yields:

 $C_2 = (50 \times 100 \times 10^{-12} \div (2\pi \times 1.5 \times 10^3 \times 1.5 \times 10^{11}))^{\frac{1}{2}}$ = 1.88 pF.

To scale  $C_2$  to a more practical value, you can use  $R_A = 50\Omega$  and  $R_B = 500\Omega$  (Ref 4). Eq 20 then yields  $C_c = (1+500/50) \times 1.88$  pF=21 pF. You may need to fine-tune this estimate to optimize the transient response.

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#### Author's biography

Sergio Franco is a professor of electrical engineering at San Francisco State University, where he teaches microelectronics courses and acts as an industry consultant. He has taught at the university for the past eight years. Previously, he was employed at Zeltron, Zanussi's Electronics Institute (Udine, Italy). Sergio received a BS in physics from the University of Rome (Italy), an MS in physics from Clark University (Worcester, MA), and a PhD in computer science from the University of Illinois at Urbana. He is a member of the IEEE. In his spare time, Sergio enjoys classical music, gardening, and mountain hiking.



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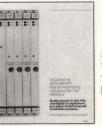
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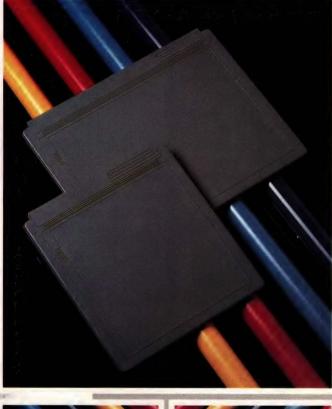
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# Glossary takes the mystery out of DSO terminology

Specification sheets for digital storage oscilloscopes (DSOs) contain many specialized terms, which can be confusing to the uninitiated. This glossary should solve the terminology problem and allow you to take full advantage of the benefits afforded by DSOs.

Bruce W Blair and Gene Andrews, Tektronix Inc

DSO manufacturers have not established a cast-in-concrete set of terms, thus creating confusion. The following definitions are designed to help alleviate this confusion, but in no way do they presume to be the final word on terminology.



**ACCURACY**—Specifies how close a measurement is to an absolute standard. Do not confuse accuracy with *resolution*—they are not interchangeable.

ACQUIRE—The total process of transferring an analog-type signal

into acquisition memory in digital form. Steps in the acquire process vary from DSO to DSO.

ACQUISITION MEMORY—Any memory that stores new waveform data points after they've been converted to digital form.

A/D CONVERTER—A device that transforms a continuous range of input voltage levels into a discrete set of digital codes.

ALIASING—Occurs when the analog-signal frequency content extends above the DSO's *Nyquist frequency*. In the time domain, undersampling leads to aliasing.

ANTIALIASING—Preventing or minimizing aliasing. Antialiasing filters, for example, remove signal components greater than the Nyquist frequency before the sam-

pling process.

APERTURE WIDTH—Sometimes called the effective aperture width, it is a measure of the interval during which the DSO's acquisition sample/hold circuit samples a waveform. The aperture width is a key contributor to a DSO's overall frequency-response specification: the longer the aperture width, the lower the bandwidth.

**APERTURE TIME**—A measure of a DSO's absolute data-sample time. Often, the *aperture width* is erroneously referred to as the aperture time.

**AVERAGED WAVEFORM**—The eventual output of the *averaging* process.

AVERAGING—A means of suppressing noise or signal variation,

averaging techniques estimate the mean of repetitive waveforms. The averaging process depends on the DSO implementation. Some DSOs, for example, acquire new waveform record points at random time points in the waveform record, and averaging occurs point by point as the scopes obtain the new data. On the other hand, a DSO with a scan converter gets a complete waveform record at one time, so each acquire and averaging event occurs at one time for the entire waveform. For sequential sampling, a DSO can collect all the points at one equivalenttime point for a given average before going on to collect the data for the next point. If the waveform is a completely repetitive waveform, the averaging technique doesn't change the resulting output. However, time-varying aspects of the waveform can cause the averaging technique to influence the outcome. Averaging is not employed to filter or reduce the bandwidth of a waveform. But, when the trigger points are not synchronous with respect to the qualified trigger events, smoothing occurs.



**CODING**—The process in A/D conversion that consists of translating an amplitude's n quantizing levels into a digital word. For an 8-bit conversion, typical coding produces integer values between 0 and 255  $(2^8-1)$  for positive binary coding and -128 to 127 for 2's complement coding.

COMPLETELY REPETITIVE WAVEFORM—A repetitive waveform that does not have waveform-to-waveform variations.



**DIGITAL FILTERING**—Any filtering done on data that have been converted to digital form. *Smoothing* and *interpolation* are two examples of digital filtering.

DIGITIZER—The subsystem or instrument that generates digital data to represent the incoming analog signal. Examples include such devices and processes as flash conversion, scan conversion, CCD FISO (charge coupled device, fast in, slow out), and successive approximation.

**DIGITIZING INTERVAL**—The time between A/D conversions that produce new waveform record points.

**DIGITIZING RATE**—The frequency at which A/D conversion for new waveform record points takes place. The digitizing rate is the inverse of the digitizing interval.

**DYNAMIC RANGE**—The useful range of a control or signal input. In amplifiers, the dynamic range is the ratio of the largest signal to the smallest signal. The largest signal is usually limited by some distortion level; the smallest signal by noise level. In A/D converters, the dynamic range is often specified as the number of bits. For example, an 8-bit digitizer has a dynamic range of 256 to 1.



**ENVELOPE MODE**—A DSO mode that produces a *waveform record* representing the accumulated maxima and minima of the signal

at or between each pair of waveform record points. The term "minmax" is sometimes applied to this mode, although min-max is often used to describe single-event envelope acquisition. To accomplish single-event enveloping, a DSO's sample rate must be greater than the waveform point rate or an analog peak-detect circuit must be used prior to sampling. The DSO examines the analog signal or digitized samples for the minimum and maximum values and transforms them into waveform record points for the envelope waveform record. In contrast, multiple-event enveloping can compare successive waveform record points that represent the same waveform time and then use these comparisons to select the new min or max value. The single- and multiple-event operations record signal content that would otherwise be lost from signals that are higher than the Nyquist frequency. These modes let you capture narrow glitches and envelopes of burst frequencies, and they also detect aliasing.

#### EQUIVALENT-TIME SAMPLING

—A type of sampling in which a DSO composes a waveform record using samples obtained from multiple occurrences of a repetitive waveform. Equivalent time sampling is used to obtain waveform point intervals that are much smaller than the smallest real-time sample interval (see sequential sampling and random sampling).



FAST IN, SLOW OUT (FISO)—A data acquisition device, such as a CCD operating as a shift register,

that accepts analog samples at its input and shifts them through to its output. During the input phase of operation, data shift as quickly as possible to obtain high sample rates. When the device is filled with data, the shift rate slows down to match the rate of downstream devices, such as an A/D converter or a memory.

FLASH CONVERTER—An A/D converter that presents a digital word at its output for each clock cycle (Fig 1). Typically, a flash converter contains an input signal comparator for each quantization level, followed by coding logic to produce the output data. An 8-bit flash converter, for example, has 256 quantization levels and 255 comparators, followed by logic to convert the output of the comparators to 8-bit results for each sample taken.

FULL-SCALE VOLTAGE RANGE
—The voltage range that represents all of the DSO's quantizing levels. For example, if the nominal LSB size in a 9-bit digitizer is 1 mV, the full-scale voltage range is 512 mV.



HOLD-OFF INTERVAL—The time the system takes to accept two successive *qualified trigger events*. The holdoff interval helps to stabilize triggering and obtain nonoverlapping waveform data.



**INTERPOLATION**—A method of approximation used to obtain additional data values between *samples* 

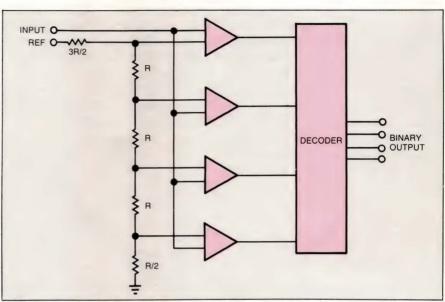


Fig 1—High speed is the key feature of the flash-conversion technique for transforming analog signals to digital outputs. Basically, a flash converter consists of a binary resistive divider and a number of comparators equal to the binary resolution.

or waveform record points. DSOs use various approximation methods; the simplest is linear interpolation. For waveforms that are sampled so that all frequencies are below the Nyquist frequency, an ideal low-pass filter provides ideal interpolation. Sin x/x-type digital filters with a cutoff at the Nyquist frequency approximate the ideal lowpass filter and provide excellent results for band-limited waveforms. For some waveforms, such as a step with no samples on the rise or fall, the sin x/x-type interpolation produces preshoot and overshoot glitches around the step that might not be part of the input signal. This estimate of the input waveform represents the waveform that has no samples on the rise or fall and also satisfies the band-limited assumption of the interpolator. Linear interpolation does not produce the preshoot/overshoot glitches, but it produces significant errors on frequency components near the Nuquist frequency.



JITTER-In oscilloscopes, the term "trigger jitter" typically describes the horizontal spreading of the trace at the trigger point on the displayed waveform. If the trace at the trigger point is sharp but becomes fuzzy away from the trigger point, the jitter indicates frequency variations of the input signal or problems in the DSO's horizontal circuits. A fuzzy trace on a dc signal indicates noise in the vertical circuits. Note that jitter is usually a combination of all the above, including variation or noise in the input signal.



LINEARITY—A measure applied to systems, such as amplifiers and

A/D converters, where the system response over its input-signal range is compared with a straight line. Vertical linearity in an oscilloscope is typically measured by comparing the amplitude of a 2-division square wave at center screen with its amplitude when positioned at the top and bottom of the display. Circuits with poor linearity produce distorted output images of the input signal.



NYQUIST FREQUENCY—Equal to half the DSO's sample rate in real-time sampling or half the effective sampling rate developed during equivalent-time sampling. False data, or aliasing, crops up at frequencies above the Nyquist frequency because the DSO cannot distinguish the signal content from that in signals below the Nyquist frequency.



**POST-TRIGGER**—The section of a waveform record that follows the *trigger point*.

**PRETRIGGER**—The section of a waveform record that precedes the *trigger point*.



#### QUALIFIED TRIGGER EVENT

—A trigger event that a DSO associates with a specific waveform record. A DSO might require many

qualified trigger events to construct a full waveform record, especially in equivalent-time sampling and other methods involving fast repetitive-signal processing.

**QUANTIZING**—A/D conversion that consists of splitting an analog signal into n levels (**Fig 2**).

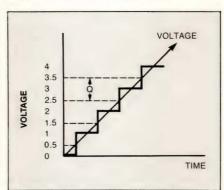


Fig 2—As the analog voltage increases, it crosses the transitions, or decision levels, represented by the dotted lines, which causes the A/D converter to change states.

QUANTIZING ERROR—Equal to  $\pm \frac{1}{2}$  the *quantizing* level for an ideal *quantizing* process. For example, using rounding techniques to convert a real number to an integer produces -0.5000 to +0.4999 error between the real number and its integer representation. Similarly, an ideal A/D converter produces integer values at the output for the

continuous range of signals at the input.



RANDOM SAMPLING-One of the two categories of equivalent time sampling. In random sampling (Fig 3), the DSO determines the time relation between the sample and the trigger event after it takes the sample. The timing of the random sample can be either signal independent or an estimate developed by using previous trigger points to predict the time for taking the present sample. Random sampling can also obtain multiple points for each trigger event. With random sampling, it's possible to obtain pretrigger records without using a delay line.

REAL-TIME SAMPLING—The second main sampling category (Fig 4). In real-time sampling, successive samples or sets of samples become successive waveform record points in the waveform record.

**RECORD LENGTH**—The number of waveform record points in a complete waveform record.

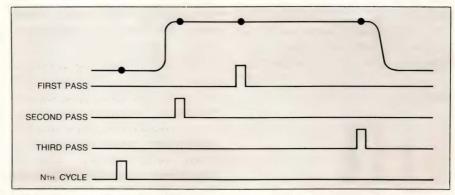


Fig 3—In random sampling, the DSO acquires signals in a random sequence in relation to where they are stored in memory. These sample acquisition points are referenced in time to the trigger point. This equivalent-time sampling technique retains pre- and post-triggering capability and minimizes the effects of normal trigger jitter.

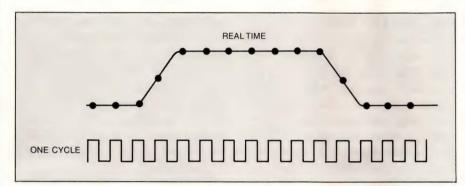


Fig 4—You only need a single pass to reconstruct a waveform with real-time sampling. However, the sample rate must be high enough to acquire sufficient data points to reconstruct the waveform.

RECORD TIME—The waveform time interval required for the waveform record. The record time equals the waveform point interval multiplied by the record length.

REPETITIVE WAVEFORM—A waveform that occurs repeatedly and has little or no variation from one occurrence to the next.

RESOLUTION—In an n-bit A/D converter, the resolution equals one part in 2n; thus, an 8-bit converter has a resolution of one part in 256. Resolution is not a measure of accuracy, but it does limit the achievable measurement accuracy. For example, a DSO might have a 2% accuracy specification for its vertical system. If the DSO employs an 8-bit A/D converter, the resolution is about 0.4%. For 6- and 10-bit A/Dconverters, the resolution is 1.5% and 0.1%, respectively. The resolution directly affects measurementto-measurement repeatability.

ROLL DISPLAY-A DSO waveform presentation that locates each new waveform record point at the right-hand edge of the screen. Previous waveform record points shift to the left as new points are displayed. In roll display, the waveform scrolls through the waveform record in real time. Some DSOs can terminate data acquisition in response to a trigger event. The roll

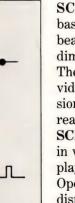


Fig 5—In sequential sampling, the DSO samples one point on the waveform for every acquisition cycle. This sampling occurs sequentially and is repeated until enough points are acquired to fill the memory. If the memory is 1000 points long, it will take 1000 passes to acquire the waveform.

SEQUENTIAL EQUIVALENT TIME

display closely mirrors that of the window view in a strip-chart recorder, with the pen at the righthand edge of the window and the chart moving out of view to the left.



SAMPLE-The acquired and stored signal information resulting from the sampling process. Samples may go through some processing before becoming waveform record points.

SAMPLE/HOLD (S/H)-A circuit that operates in two modes under the control of a strobe signal. During the sample mode, the circuit's input couples through to the output to capture a new sample value. The input disconnects from the output during the hold mode, and the output maintains the amplitude of the previous sample.

SAMPLE INTERVAL—The time between successive samples. The reciprocal of the sample interval is the sample rate.

SAMPLE RATE—The real-time frequency at which a DSO acquires waveform samples.

SCAN CONVERTER—A CRTbased device that uses an electron beam to store a waveform as a 2dimensional pattern on a target. The target is usually a phosphor-or video-format imager. A/D conversion often takes place as part of the reading operation.

SCROLL MODE—A display mode in which a DSO simultaneously displays multiple repetitive waveforms. Operationally, the DSO scrolls the display up or down and replaces the oldest previous waveform with the newest waveform. All waveforms usually have a common trigger position.

FIRST CYCLE |

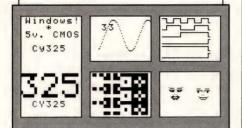
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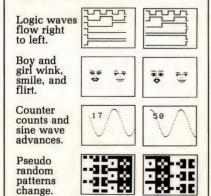
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SEQUENTIAL SAMPLING—One of the two categories of equivalenttime sampling. In sequential sampling (Fig 5), the sample timing signals lock onto the trigger events. The trigger event controls the sample-taking sequence. One waveform point interval increments successive samples forward to gather the points for each new waveform record. Because this method depends on the trigger to initiate sampling, a DSO without a delay line in its vertical data acquisition path cannot use sequential sampling to collect pretrigger data.

SMOOTHING—A method of bandwidth filtering and noise suppression. Typically, a DSO combines a set of waveform record points that represent different instants in time to produce the smoothed waveform. Numerous smoothing algorithms exist. In sequential sampling, the smoothing operation employs a filtering technique that uses the exponential decay of the data of previous points. Another algorithm relies on a square-pulse convolution, where

each data point in the smoothed record represents the average of selected points from the source waveform record. This convolution produces a frequency response that closely mirrors that of a sin x/x filter. It's possible to smooth single-event waveforms; averaging, on the other hand, applies only to repetitive waveforms.

SUCCESSIVE-APPROXIMATION CONVERTER—An A/D converter that generates an n-bit digital word after n+1 clock cycles (Fig 6). Typically, this converter contains a single input signal comparator, a logic register to store the result, decision logic, and a D/A converter that feeds back the register's value to the input comparator. On each clock cycle after the start of a conversion cycle, the converter makes a decision about one bit and continues to work toward the least significant bit. Successive-approximation conversion is much slower than flash conversion but requires much less circuitry.

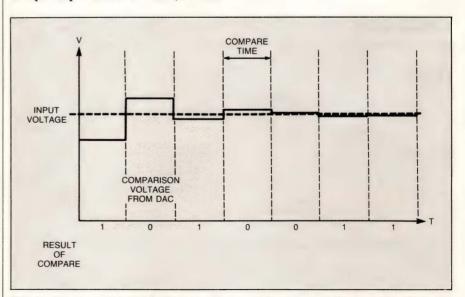


Fig 6—Average speed and high accuracy contribute to the popularity of the successive-approximation converter. Note that the time to convert the analog signal to a digital number is directly proportional to the achieved resolution.

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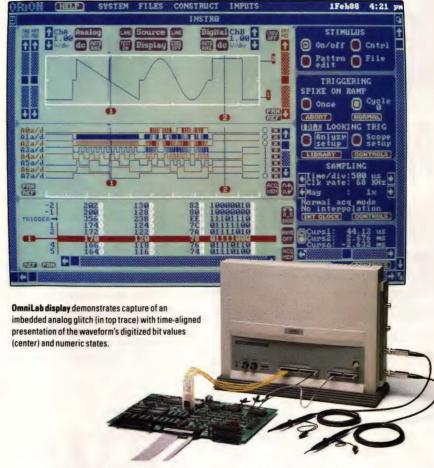
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TRIGGER EVENT—Each signal occurrence that the DSO's trigger circuits detect.

TRIGGER POINT—An identified waveform record point that occurs at the same time as a qualified trigger event. The qualified trigger event might occur between two of the actual waveform record points and generate a time uncertainty equal to half of a waveform point interval. A waveform record doesn't require a trigger point. In a roll display waveform record, for example, no qualified trigger event occurs.

TRIGGER POSITION—The location of the trigger point in time—either within or relative to the waveform record.



#### WAVEFORM POINT INTERVAL

—The time between adjacent points in the complete waveform record.

WAVEFORM POINT RATE— The effective sample rate of data stored in acquisition memory. Reducing the sample rate lets you acquire longer time windows in acquisition memory. You can reduce the sample rate by slowing down the A/D converter or by saving only selected data values. For example, to see a 5-times longer time interval in a record, save only every fifth data point from the A/D converter. WAVEFORM RECORD-A set of waveform record points that includes a full waveform in digital form.

#### WAVEFORM RECORD POINT

—A digital word that represents an analog input voltage at one instant in time.

#### Authors' biographies

Bruce W Blair is an engineering section manager at the Portable Instruments Division of Tektronix Inc (Beaverton, OR). In this position, he manages a

new-product development team. Bruce holds a BA in mathematics and an MSEE degree from the University of Nebraska. He has been awarded five patents and is a registered professional engineer and a member of IEEE. In his spare time, Bruce enjoys golfing, skiing, camping, and flying radio-controlled airplanes.



Gene Andrews is chief engineer and manager of technology development at the Laboratory Instruments Division of Tektronix Inc. In this position, he has

led the development of a number of oscilloscopes. Gene has worked for Tektronix for 26 years and holds 12 patents. He has a BSEE from Oregon State University and an MSEE from Stanford University.



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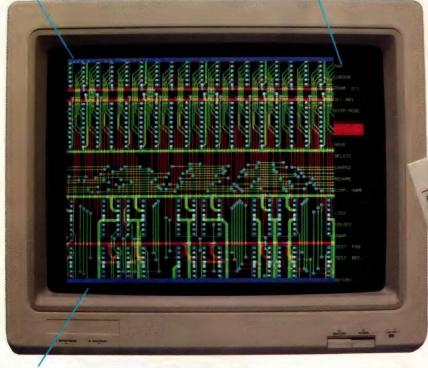
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## PSpice review reveals strengths, drawbacks of optional packages

Ten years ago, Spice was found only on mainframes at universities and large corporations. Today, PC versions of Spice are available from several vendors, and more often than not they provide facilities not present in the original. One such version is MicroSim's PSpice.

#### Jonathan B Scott, University of Sydney

Spice, which stands for simulation program with integrated circuit emphasis, is probably the best known and most widely used analog simulator. What most people don't know is that it is the brainchild of L W Nagel, who wrote the first version of Spice as part of his PhD thesis when he was at the University of California Berkelev in the late 1960s. Spice was the first program that provided a means of telling a computer about the electrical characteristics of electronic components such as resistors, capacitors, inductors, and transistors, and their interconnections in a circuit, and then inducing the computer to predict numerically how the circuit would perform if and when someone actually built it. Such predictions are particularly important in IC design because you can't breadboard an IC and the first prototype is extremely expensive. Further, "testing" a circuit by computer simulation lets you perform "what if?" experiments in ways that would be economically unfeasible with a physical prototype.

Spice was always capable of running on any type of computer. However, if you wanted to simulate a great number of nodes the program needed a great deal of computing power to produce results within a reasonable period of time. Ten years ago, for example, it was found only on mainframes at universities and large corporations, and you had to justify the cost of simulation time by citing the cost of IC fabrication.

Nonetheless, Spice began to be so widely used and valuable that the University of California Berkeley continued to develop and expand its features. Today the most common and trusted version is Release 2, Revision G. Although Version 3 is available, and incorporates models of GaAs devices, as well as new facilities such as the modeling of switches in circuits, it's new and some bugs still exist.

Berkeley Spice has one major disadvantage from today's standpoint: It doesn't offer any graphics capability. It is designed to produce output on a line printer; a .plot command produces graphs that come out sideways from the printer, that use only printable, alphanumeric characters, and that must be either 80 or 132 characters wide.

Basically Spice is public-domain software. The University of California Berkeley charges a nominal fee for translating the program into a customer's format, but it doesn't charge royalties. After all, the university

Spice's performance predictions are especially important when you consider that you can't breadboard an IC and that the first prototype is extremely expensive.

is interested in Spice as a research tool, not as a slick commercial package. It's encouraging to note that software vendors that have produced their own versions of Spice have closely followed the University of California Berkeley's conventions and have maintained a remarkable degree of standardization.

#### What's the motivation?

You may wonder why a commercial house would want to write and try to sell a version of a program that is available to everyone for a nominal copying and shipping charge. The answer is that they hope to corner the market by offering some or all of the following additional features:

- Code that executes faster and more efficiently and thus runs faster on a mainframe or runs in the same amount of time on a less powerful machine.
- Versions for different or more popular machines, such as the IBM PC family or the Apple Macintosh II.
- Related programs that make using Spice easier and more convenient—drivers for graphics devices such as color monitors or plotters are a good example.
- Associated libraries of component models, or programs that help the user develop new models from data sheets.
- More up-to-date handling of newer devices, such as MOSFETs and GaAs JFETs.

The vendors are also working on the problem of numerical convergence during the simulation of complex circuits or of circuits that have feedback mechanisms, and they are trying to eliminate as many bugs as possible.

Because modern microcomputers have the power to run complex analog-circuit simulations within a reasonable amount of time, several vendors offer PC or Macintosh II versions of Spice. MicroSim's (Laguna Hills, CA) PSpice is an up-to-date commercial version of Spice and can run on a variety of machines, including 80286-based personal computers in the IBM PC family, 80386-based machines such as the Compaq and Sun 386i, and Apple's Macintosh II. It offers 44 statements, most of which are Spice2 standard, though some (which allow you to model JFETs, GaAs MESFETs, and other new devices) are unique. PSpice also has four optional packages—Probe, Monte Carlo, Parts, and Device Equations—each of which offers a special capability.

(Ed Note: This review draws on the author's and his

University of Sydney colleagues' experiences with PSpice running on an IBM PC/AT.)

The Probe package allows you to plot output waveforms and graphs on output devices that have graphics capability. The program works with a wide range of PC graphics cards, monitors, plotters, and printers. It does an impressive job running on PCs that have a CGA or EGA card.

The package is also capable of a number of operations that standard Spice can't perform at all. For example, Probe can plot one variable against another in oscilloscope X-Y fashion; it can determine power dissipation as a function of time or ascertain the average value; it can apply a Fourier transform to a plot; it can display several graphs simultaneously; and it can overlay a number of plots. The overlay facility is very useful in conjunction with the Monte Carlo option—in fact, you may well find that Probe is *essential* to make full use of the Monte Carlo option.

#### Overall, it works fine

Overall, Probe works well and is a valuable accessory, especially when you consider the execrable quality of a great deal of commercial software. To use Probe, you merely insert a .PROBE statement in the PSpice input file. When PSpice runs, it creates a special data file that the Probe postprocessor can read and process at a later time. Nevertheless, Probe does exhibit some traits that detract from its appeal.

A minor problem is that Probe always presents a menu of options and forces you to choose a number from the list. It ought also to accept a mnemonic letter or the name of the function you want. If you want to rescale the X axis, for example, you have to enter the appropriate number—you can't enter "X." You can't effectively type ahead: At each menu you have to convert what you want to do into some arbitrary number. This quirk is surprising, because at initialization the program can accept commands in the form of the English words in the menu—in itself a very useful facility. The "numbers only" syndrome becomes even more annoying in light of the second complaint.

Probe is sometimes ridiculously slow—so slow in fact that you must leave it to do its work as a batch job. This seems to be the reason why Probe has the ability to execute commands from a file at initialization. For example, at the University of Sydney, some simple runs generated data files, but it took many minutes for Probe to load these and plot them. It would have been just as quick to print the original PSpice output

on a printer.

A third detracting trait is that Probe can crash without giving any error indication. The crash itself presents no great burden because the program doesn't generate any data and the crash doesn't destroy any. But the lack of any indication as to the cause of the crash can be extremely irritating.

#### The Monte Carlo option handles tolerances

The Monte Carlo option allows you to attach both individual component tolerances and lot tolerances to parameters in the PSpice input file. You can then perform any specified number of repeat runs (limited by time and disk-storage space); for each new run, the Monte Carlo option changes the values of the tagged parameters randomly. Using this method, you can assess the spreads to be expected in production. If you're familiar with the difficulty of calculating how far the various operational properties of a circuit are sensitive to particular component tolerances (particularly in filter design), you'll appreciate that this option can save you a tremendous amount of time and effort.

For example, you could use the Monte Carlo option to find the expected variation in the response of a triple-notch canyon filter, and then use Probe to superimpose the responses of 50 or 100 runs with varied component values. Fig 1 shows the result of such a test. For any design, the Monte Carlo option can save you an enormous amount of time and serious algebra, and if you're designing a circuit specifically for production in volume, this option can give you a great deal of power.

The hard work—and potential for error—in a Spice simulation lies in determining the model parameters of special components. For example, what would you enter for the Early voltage of a 2N3055 transistor? The data sheet doesn't contain any mention of this parameter. You can calculate it, however, if your data sheet gives you the device's output conductance for a known collector current or if there is a graph of  $I_{\rm C}$  vs  $V_{\rm CE}$ , and if you have a good textbook to tell you how to perform the calculations.

To help you determine model parameters, PSpice comes with a library of standard components such as op amps, diodes, MOSFETs, BJTs (bipolar-junction transistors), and so on. Unfortunately, the model-library writers seem to think that only Motorola and Texas Instruments make BJTs, and so this standard library is all but useless in Europe and Australia, where local suppliers carry a large range of devices

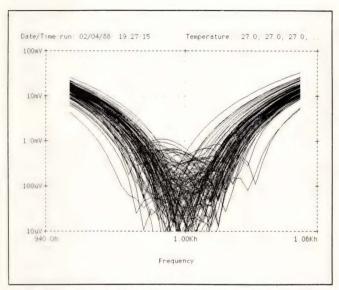


Fig 1—With the aid of the Monte Carlo option, MicroSim's PSpice produced this prediction of response spreads for a triple-notch filter. The plots were superimposed using the Probe option.

that are far more common than those from Motorola and TI.

Luckily, the Parts option can also produce models of diodes, BJTs, and MOSFETs using data that you have extracted from data sheets. As long as you have a good data sheet for the part you are trying to model, you'll meet with reasonable success. However, at a number of places you can cause the program to crash by entering silly data, and this should not be possible. On several occasions we found that the program either gave warning that results were out of sensible bounds or rejected ludicrous data, but at other times it crashed.

#### Specs are at fault

The Parts option's severest limitation—that it must use data from the device specifications—isn't really the fault of the vendor. Most components are terribly underspecified, and the program either does not attempt to estimate the parameters for which the manufacturer does not usually supply data, or else it makes a crude guess at the values from a few simple pieces of data. For instance, using erroneous data you can induce the program to tell you that a 2N3055 has a beta of about 16,000, but as long as you adjust the other parameters to equally ridiculous values, the Parts program will produce a plot that resembles what is known to be correct for hfe.

What you must take into account is that precise

Vendors of PC versions of Spice have closely followed University of California Berkeley's conventions and have maintained a remarkable degree of standardization.

specification is not necessary—as the manual does indeed point out. Nevertheless, the program would be much better if it offered to take the results of measurements made on an actual device, and then to give a better model, instead of saying (as it does): "... suchand-such a parameter is not so important, anyway...."

It would be foolish to expect anyone to be able to use Parts successfully without first knowing the significance of many of the device parameters. In short, the Parts program assumes a lot of knowledge on the part of the user. For many designers, an hour or two in the lab with a curve tracer and some measuring gear, followed by a few minutes with a calculator and a textbook on device models, would give a far better model than Parts and a data book ever would. This criticism is less true for op amps, which are significantly harder to measure and are generally much better specified. Even so, you need to know what you're doing before you can successfully use the Parts program.

The future may hold promise in this regard, however. Spice is becoming so widespread that manufacturers may one day publish the Spice models of their op amps and devices as standard items in their data books.

#### Device Equations option lets you make changes

With the Device Equations option, you get the PSpice program in partially compiled form so that you can make changes to the basic equations of the simulator. This option can be very valuable to a serious research establishment, but it is of no interest to the general user. Consider the model of a MESFET. This model is still a matter for discussion in contemporary publications, and MicroSim periodically updates its model in response to published research from major institutions; such updates are still somewhat behind the state of the art, nonetheless. For example, a local designer closely involved with GaAs MESFET IC design and fabrication evaluated the PSpice's MESFET model and found that the temperature-compensation equations had been transferred directly from the silicon case—which is incorrect. To make the proper correction, the Device Equations option is necessary. Much praise is due to MicroSim for making this option available despite the limited market for it.

The consenus at the University of Sydney is that PSpice is very up-to-date in comparison with other versions; revisions continued to appear even while we were reviewing the program. The shortcomings that came to light affect only the most advanced applications and will not bother the typical user. We found considerably fewer bugs in PSpice than in other PC versions of Spice that we had used, and also fewer bugs than in the Berkeley Spice Version 3 that we received at about the same time.

When you run PSpice on a PC/AT with a 10-MHz CPU, an 8-MHz math coprocessor, a fast hard disk, fast memory, and a full expanded EGA, the program executes significantly slower than it does on a VAX 11/780. Nevertheless, the speed is quite adequate for the types of jobs that a small business is likely to be interested in running. For small jobs, the speed is quite satisfactory even on an IBM PC/XT with 760k-byte floppy-disk drives.

The Probe graphics postprocessor is very good, and more than lives up to its sobriquet of a "software oscilloscope." Initially, we felt that Probe was unnecessary, but the more we used it, the more we found it could do. We recommend its purchase to anyone who's paying for the time of the person using PSpice, and certainly for anyone who's using the Monte Carlo option. We also highly recommend the Monte Carlo option to anyone who is contemplating the manufacture (or publication for others to build) of circuits.

Our first major criticism of PSpice concerns its copy protection. We realize that Spice is a large and relatively costly package, given away virtually free to anyone who has a mainframe; obviously the temptation to copy it is strong. Nevertheless, the copy protection is an unmitigated pain in the neck for several reasons. First, if PSpice has been supplied with "key disk" protection, the key disk must be in the A drive every time you use the program or any of its options. We understand that the vendor will supply a security plug (called a "dongle") instead of key-disk protection, but you have to have a free port for the dongle, and it's still a nuisance, especially on portable and lap computers. Other reviewers have commented that if you have additional dongle-protected application programs, the multiple dongles can interfere with each other. Further, the disk type of copy protection precludes the use of machines that don't have at least one 5\(^1/4\)-in. drive that can handle the 360k-byte format. For a PC/ AT, you would have to add another expensive piece of hardware to your system.

The second criticism is that PSpice and its four packages won't run at all without a math coprocessor. If anything, this constraint is the more serious defect, and little justification exists for it. Coprocessors are

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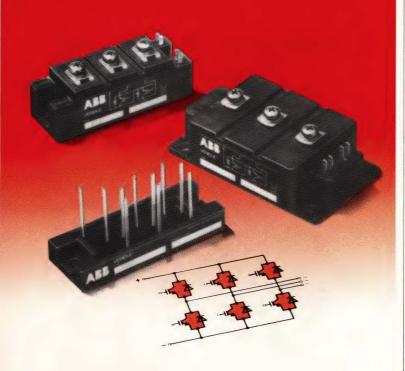




ABB SEMICONDUCTOR 2150 W. 6th AVE. BROOMFIELD, CO 80020 1-303-469-1883 1-800-992-0312 TELEX 299-745 FAX (303) 469-8394 expensive, and some machines (particularly lap ones) simply don't have any provision for a coprocessor. We assume that MicroSim didn't want to be criticized for the slow execution that would result from running PSpice without a coprocessor. However, we contend that they deserve far more criticism for the omission—many potential users outside the US on low budgets would be willing to wait those few more minutes for the results.

Finally, as far as the cost of the package is concerned, it is high if you're only an occasional user but quite reasonable for a large company. PSpice is more expensive than any of the other PC versions of Spice we've heard of—but then it also seems to be better.

One feature of PSpice largely offsets all our criticism: MicroSim offers a demonstrator package and "welcomes" copying. This package allows you to try the full range of functions, except the Device Equations option, but limits you to the simulation of small circuits with no more than 10 transistors. The demonstration package runs from any type of disk and does not need a coprocessor. We were able to test filters of considerable complexity by using half a dozen E cards as op amps. We were also able to test models of transistors and MOSFETS, to design RF front-end amplifiers, and to generally exercise all the facilities of the larger program. We strongly recommend this package to anyone who's thinking of buying PSpice, as well as to anyone who just wants to learn about Spice.

#### Acknowledgment

This review originally appeared, in a much longer format, in the May, 1988, issue of Roger Harrison's Australian Electronics Monthly magazine, Sydney, Australia.

#### Author's biography

Jonathan B Scott teaches fourth-year students of electronics at the School of Electrical Engineering, University of Sydney, Australia. He is also a director of an electronics R&D company specializing in the areas of modeling and circuit design. Jonathan holds BSc, BE, and MEngSc degrees from the University of Sydney. In his spare time he enjoys cooking and entertaining, bicycle riding, and making toys and models.



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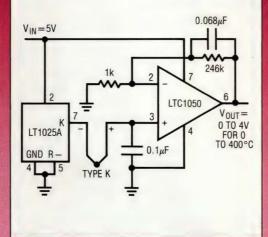
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EDN January 5, 1989

## **DESIGN IDEAS**

EDITED BY CHARLES H SMALL

## Circuit eases writing of modifiable code

Paul D Gracie
The Microdoctors Inc, Palo Alto, CA

The circuit of Fig 1 adds a new type of instruction to a  $\mu P$ 's instruction set and thus makes writing self-modifying code much easier. With this circuit installed, the  $\mu P$  can execute the contents of any of its registers as if the contents were the next instruction in the program. You can process instructions as data or you can select and modify instructions before executing them

To use the circuit, your program first must write the register's value out to the Jam register, IC<sub>3</sub>. The system-memory decoder recognizes the specific address for the memory-mapped Jam register and, along with  $IC_{1A}$ , generates the jam-register write-strobe signal,  $\overline{JWR}$ . This signal performs two functions. It clears flip-flop IC<sub>2A</sub>, which disables the system-memory decoder, and it gates the  $\mu P$ 's  $\overline{RD}$  strobe signal to both the Jam register and flip-flop IC<sub>2B</sub>.

When the next instruction fetch occurs, the  $\overline{RD}$  strobe signal dumps the contents of the Jam register onto the data bus as an instruction that the  $\mu P$  proceeds to process. Note that, because IC<sub>2A</sub> has disabled the system-memory decoder, the  $\mu P$ 's read request

does not fetch an instruction from memory. The  $\overline{RD}$  strobe signal also toggles  $IC_{2B}$ , which sets  $IC_{2A}$ , reenabling the system-memory decoder and presetting  $IC_{2B}$ . The system then returns to normal operation.)

To operate the circuit, you need software in the form

•

MOV B,INST ;LOAD INSTRUCTION IN B REGISTER

MOV M,B NOP NEXT ;MOVE INSTRUCTION TO THE JAM REGISTER

;INSTRUCTION EXECUTES HERE ;NEXT INSTRUCTION IN SEQUENCE

•

In this sample code, the value loaded to the B register gets executed as an instruction. The instruction executes in place of the following NOP (no operation). After the instruction executes, the program proceeds in the normal manner. You should be careful when programming multibyte instructions—the second (and third) bytes of such instructions will be read from main memory at the location following the NOP.

To Vote For This Design, Circle No 746

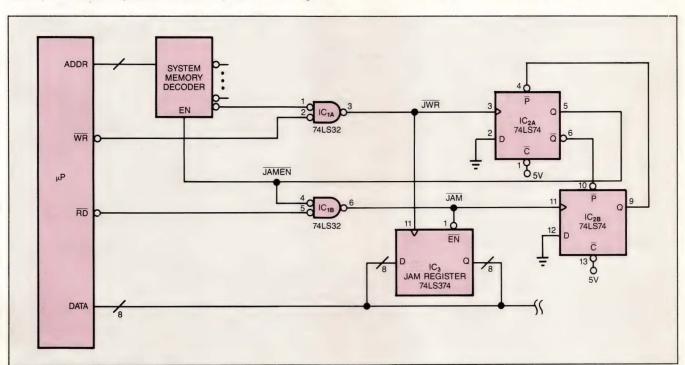


Fig 1—This circuit makes writing self-modifying code much easier. The circuit allows you to write a register's contents to an offboard Jam register, and it then automatically substitutes the Jam register's contents for the next CPU instruction fetch.

## Technique maximizes converter efficiency

Roger C Whipple Hazeltine Corp, Braintree, MA

For a designer wishing to use a Linear Technology LT1072 switching regulator in the buck mode and being forced to deal with high input voltages, achieving the highest efficiency possible poses a problem. If, for example, you need to convert 20V to 5V at a relatively low power level of 1.25W, the quiescent current of the device itself (typically 6 mA) will become an important part of the circuit's power consumption. Because the quiescent current is relatively unaffected by the input voltage, the power that the IC consumes is directly proportional to its applied supply voltage. If your system has an external low-voltage supply available, you could run the IC from it-the LT1052 operates down to 2.6V. If such an auxiliary supply is absent, you can operate the IC from its own output by incorporating a switch-over circuit (Fig 1). Adding this feature boosts the supply's overall efficiency from 77 to 83%.

When you first apply power to the supply, the regulator has no output: R<sub>8</sub> and D<sub>7</sub> hold C<sub>6</sub> discharged and

the gate of MOSFET  $Q_4$  at ground. Because  $Q_4$  is turned off, the rising supply voltage pulls the gate of  $Q_3$  up via  $R_5$ . As the supply voltage rises,  $Q_3$  turns on, applying the full input voltage to the IC and allowing the regulator to begin operation.

Once the regulator starts and the output voltage rises,  $C_6$  begins charging through  $R_8$ . When the voltage on the gate of  $Q_4$  reaches about 2.5V,  $Q_4$  turns on, pulling the gate of  $Q_3$  to ground and shutting it off. This shutoff removes the input voltage from the IC. As  $C_5$  discharges into the IC,  $D_5$  becomes forward-biased and supplies voltage from the output to the IC.

If a power glitch or a momentary short circuit causes the output voltage to drop below the minimum that the LT1072 needs to operate, diode D<sub>7</sub> will rapidly discharge C<sub>6</sub>, allowing the input voltage again to be applied to the IC. When the voltage rises again, normal operation will resume.

To Vote For This Design, Circle No 749

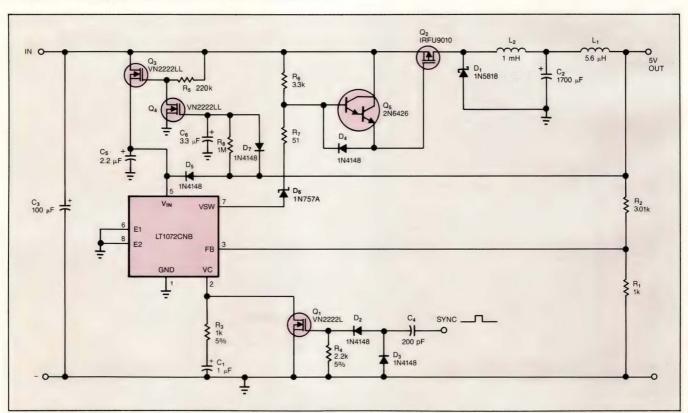


Fig 1—This switchover circuit powers the regulator IC from the supply's output after the supply starts up. Running the IC from the lower-voltage output instead of the intput raises the supply's efficiency from 77 to 83%.





# dc to 2000 MHz amplifier series

#### **SPECIFICATIONS**

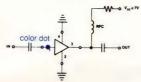
MODEL	FREQ.	GAIN, dB				• MAX.	NF	PRICE	\$
	MHz	100 MHz	1000 MHz	2000 MHz	Min. (note)	PWR. dBm	dB	Ea.	Qty.
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MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8 🗆	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	_	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
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## Digital potentiometers set biquad filters

Nikolay T Tchamov High Institute of Mechanical and Electrical Engineering, Sofia, Bulgaria

Digital potentiometers allow you to digitally configure biquad filters so that they will retain their setups even if you remove power from the circuit. Biquad filters can have a Q of as high as 100, are easy to tune, are stable, and can be cascaded to achieve higher-order filters. The digitally configured filter circuits in Figs 1, 2, and 3 all use Xicor X9503s and suit telephone-band applications.

Fig 1a is a Butterworth lowpass filter with a cutoff frequency of 3000 Hz and a gain of 10 (Ref 1). By

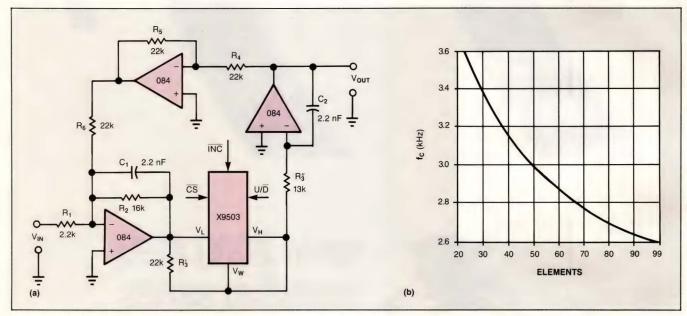


Fig 1—The X9503 digital potentiometer makes it possible to tune the cutoff frequency of a telephone-band lowpass filter.

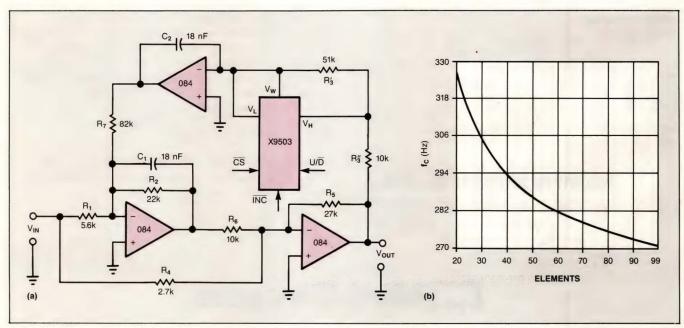
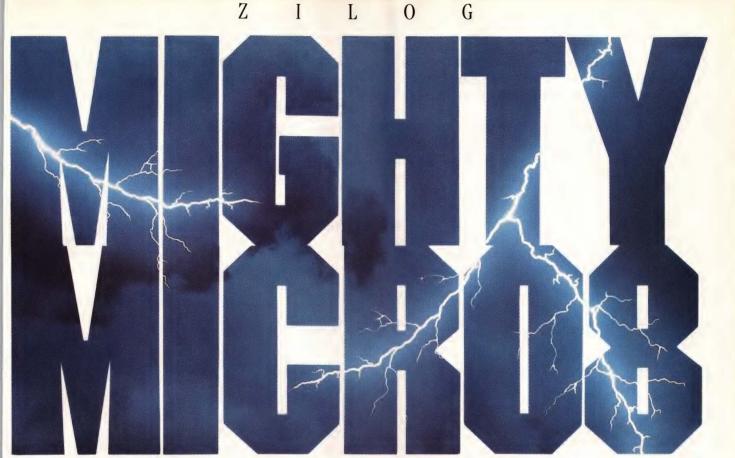


Fig 2—Similar in operation to Fig 1, this highpass filter relies on its digital potentiometer to set the cutoff frequency.



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EDN January 5, 1989 205 **CIRCLE NO 115** 

## **DESIGN IDEAS**

adjusting the digital potentiometer, you can shift the cutoff frequency (fc) by 30% (Fig 1b). Replacing R<sub>1</sub> with a digital potentiometer allows you to control the gain digitally as well.

Fig 2a is a generalized filter circuit based on Ref 2. A Butterworth highpass filter, it has a 300-Hz cutoff frequency and a gain of 10 in its passband. Again, you can shift the filter's tuning by 30% via digital control (Fig 2b). In this case, replace R<sub>4</sub> and R<sub>5</sub> with digital potentiometers to control the filter's gain.

Ref 2 also provided the design equations for the tunable bandpass filter of Fig 3a, which has a gain of 10. You can vary the filter's center frequency over a 6:1 range (Fig 3b) by simultaneously trimming R<sub>5</sub> and

R<sub>6</sub>. In this circuit, substituting digital potentiometers for R<sub>1</sub> and R<sub>2</sub> allows you to control the filter's gain.

#### References

- 1. Tow, J, "A step-by-step active-filter design," IEEE
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- 3. Aurada, M J, "Application of multiplying digital-toanalog converter to digital control of active filter characteristics," IEE Proceedings, Vol 128, part G, No 2, April, 1981.

To Vote For This Design, Circle No 747

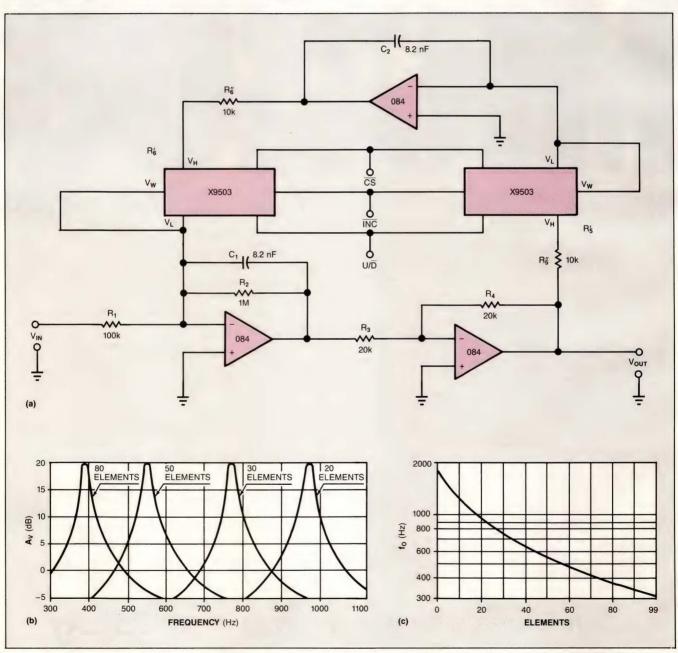


Fig 3—Using a pair of digital potentiometers, you can vary a passband filter's center frequency over a 6:1 range.



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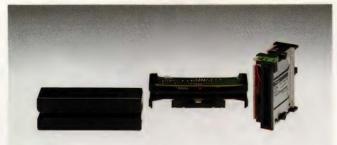
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MCI-111	ISO 3554 Track 2	Magnetic card insertion system	67×65×24	

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## 555 timer triggers on millivolt signal

John J O'Farrell
The Tran-Trol Co, Tallahassee, FL

You can trigger the 555 timer of Fig 1 with a signal as low as 15 mV because the signal appears directly across the threshold comparator's inputs. Be aware, however, that some chips may require a worst-case level of 30 mV; no chip maker specifies a value for the base current into pin 6 of a 555 timer. Even using worst-case inputs, though, the circuit of Fig 1 triggers at much lower levels than any other 555 circuit.

To ensure that the trigger level is independent of the chip's dc bias, the impedance of  $C_2$  should be much lower than the resistance of  $R_B + R_C$ . You must clamp the input signal if it would otherwise drive pin 6's voltage more than 0.3V below  $V_0$  (the input-voltage range should be  $\leq V_{CC} + 0.3V$  to  $\geq V_0 - 0.3V$ ). Also, for the circuit to operate,  $R_1$ 's impedance must be significantly lower than the threshold comparator's gigohm-range input impedance. Unless  $R_1$  is less than 150 k $\Omega$ , no signal path will exist from the input to  $C_2$ . In other words, increasing  $R_1$  does not increase the circuit's sensitivity.

You can use the standard 555-timer equation,  $T=1.1R_TC_T$ , to determine the 555's output-pulse width. You should set the output pulse's width shorter than the input pulse's to allow the chip to timeout and reset itself before the next input pulse arrives. If you

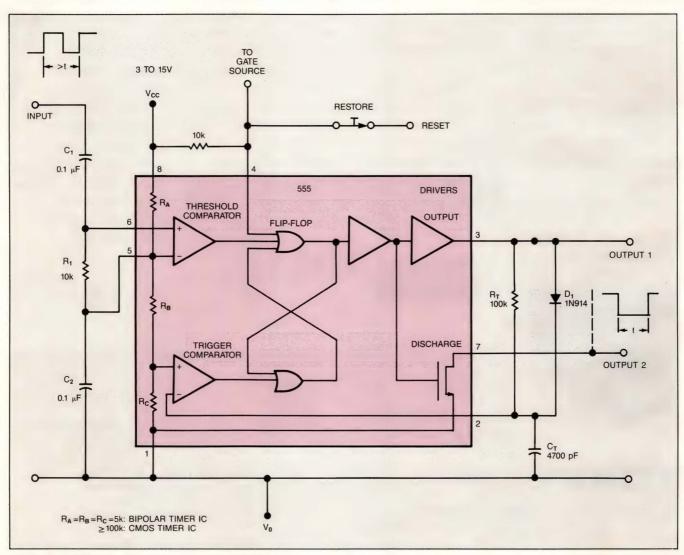


Fig 1—This 555 timer circuit can trigger on signals as low as 15 mV.

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### **DESIGN IDEAS**

don't set it to operate in this manner, the timer will ignore subsequent input pulses until after timeout and reset occurs and may consequently act as a frequency divider.

The values for the external components in Fig 1 work from approximately 400 to 1800 Hz. The time required for  $C_T$  to recharge to above  ${}^{1}\!\!/_{3}V_{CC}$  (the pin 2 trigger comparator's operating point) determines the upper-frequency limit of the timer. The impedance of  $C_1$  and  $C_2$  determines the voltage across  $R_1$  and hence sets the circuit's lower-frequency limit. Pin 3 of the 555 timer produces an inverted, amplified version of the trigger signal.

At startup, pin 6 of the 555 timer is low relative to pin 5.  $C_T$  is discharged and pin 2 is momentarily held low. This condition trips the internal latch, forcing pin 3 high, which starts to rapidly charge  $C_T$  through  $D_1$  until the charge on  $C_T$  reaches a voltage level above  $\sqrt[4]{V_{CC}}$ . This entire sequence can occur only if pin 4 is above the reset level (0.7V).

When a positive-going input signal greater than the threshold comparator's limit appears across  $R_1$ , the threshold comparator switches state, forcing pin 3 low and grounding the high end of  $R_T$ . Capacitor  $C_T$  then discharges through  $R_T$  to  $V_0$  until the voltage at the junction of  $R_T$  and  $C_T$  goes below  $\frac{1}{2}V_{CC}$ .

If the Reset terminal's voltage is above its operating point, pin 3 switches high again, rapidly recharging  $C_T$  to the  $V_{CC}$  level. If the Reset terminal's voltage is below its operating point, the circuit will latch on, with pin 3 low, and it will ignore subsequent input signals until it is restored. Pin 7 is available as an independent open-collector output, which also conducts to  $V_0$  while pin 3 is low.

You can use pin 4 (the Reset pin) to control the timer in several ways:

- Connecting pin 4 to pin 8 will disable the Reset function and allow the timer to respond to each input pulse.
- Connecting pin 4 to a gating voltage source will tell the timer when to respond to input pulses.
- Connecting pin 4 to pin 3 or pin 7 via a restore switch will force the timer to trigger and latch on the first input pulse it senses following a restore instruction, thereby forming a single-pulse detector.

You can also combine a pair of these timer circuits to achieve a voltage-crossover detector having a very narrow window.

To Vote For This Design, Circle No 748

## Dual op amps improve bridge sensitivity

John Waugh Wautec Inc., Santa Barbara, CA

Using a pair of high-performance op amps, you can improve both the sensitivity of a Wheatstone bridge and its ability to handle large, off-balance signals without losing linearity. The conventional configuration of Fig 1a employs a single, differential amplifier; the circuit of Fig 1b uses less-expensive, dual transresistance amplifiers.

The output of the conventional Wheatstone bridge is expressed as

$$e_0 = \frac{kde_{IN}}{(k+1)^2 \left(1 + \frac{kd}{k+1}\right)},$$

where d is the off-balance fractional resistance and k is the bridge ratio (k is always less than unity). The sensitivity factor is  $k/(k+1)^2$ . The  $(1+k\times d/(k+1))$  fac-

tor in the output equation accounts for the bridge's nonlinearity.

When k=1 (the nominally optimal bridge ratio), the linear part of the output expression reduces to  $e_0 = d \times e_{IN}/4$ . The fractional nonlinearity is approximately -d/2, which is, in effect, scale compression at large bridge unbalances, thus limiting the range of the bridge element's deviation from a specified linearity.

The dual transresistance bridge amplifier of Fig 1b has an output signal expressed as

$$e_0 = \frac{kde_{IN}}{k+1}$$

where the k+1 factor is inserted to obtain the same total voltage across the bridge. This circuit's sensitivity is thus k+1 times larger than that of the conventional arrangement, and the nonlinearity factor is absent. For k=1, the dual transresistance configuration's output is  $d\times e_{IN}/2$ , which is twice the sensitivity of the









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### **DESIGN IDEAS**

conventional, differential arrangement.

You can effectively use this doubled sensitivity to good advantage with piezoresistive, strain-gauge-bridge pressure sensors having at least one corner of the bridge open (several manufacturers supply such gauges). Fig 2 shows the basic circuit using an inexpensive Teledyne TSC-914, quad chopper-stabilized op amp. The two additional transresistance amplifiers are a more economical way of obtaining the differential output as compared with the usual instrumentation amplifier that requires three amplifiers to obtain high common-mode rejection.

In this case, the bridge output is expressed as

$$e_0 = \frac{4aPe_{IN}}{1 - a^2P^2}$$

where aP, the pressure-induced fractional-resistance change, is limited to about  $2\times 10^{-2}$  by mechanical strain in the sensor's silicon diaphragm. The maximum bridge nonlinearity is thus  $4\times 10^{-4}$ , which is much lower than the nonlinearity of the conventional differential-amplifier configuration or the sensor's inherent linearity.

You can take advantage of this twofold increase in sensitivity to extend either the low-end pressure sensitivity or the over-range safety margin by making sensors with thicker diaphragms, yet having the same low-end sensitivity.

#### To Vote For This Design, Circle No 750

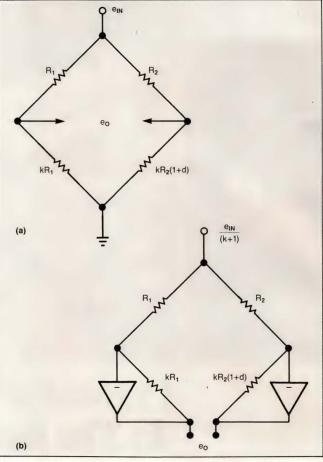


Fig 1—The conventional Wheatstone bridge (a) is not as sensitive and doesn't handle off-balance signals as well as the dual transresistance configuration of b.

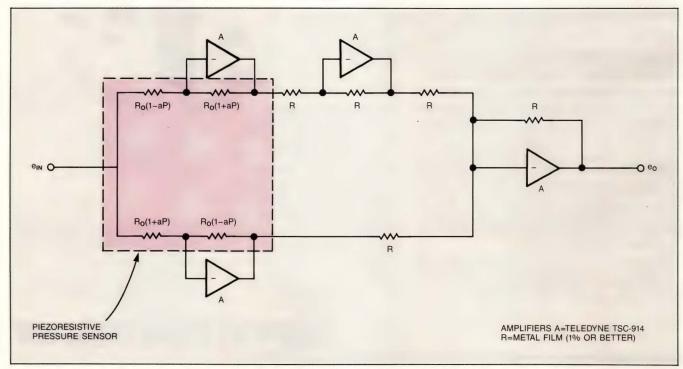


Fig 2—Combining a piezoresistive pressure sensor with a dual transresistance amplifier yields a superior strain gauge.

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### **DESIGN IDEAS**

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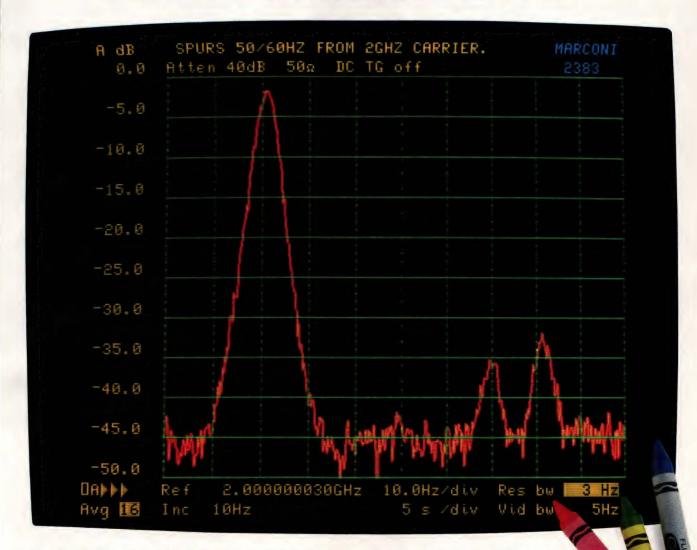
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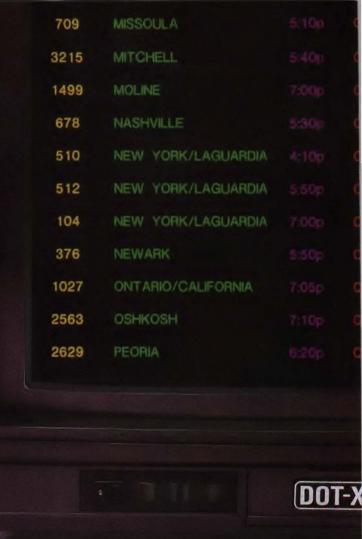
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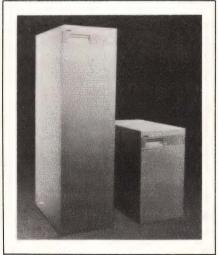
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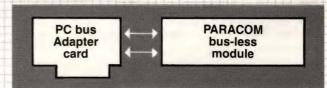
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#### **How it Works:**

Remove the plate on any Paracom bus-less card, plug a MEGAFRAME/PC into it's connector, and insert the assembly into a PC/XT/AT slot.



If your project grows beyond the limitations of the PC, detach the bus-less module, re-install the adapter in a slot by itself, and use the adapter's external connector to link to the bus-less module and additional cards in an external expansion chassis.



BLDG. 9, UNIT 60 245 W. ROOSEVELT RD. WEST CHICAGO, IL 60185 PHONE (312) 293-9500 FAX (312) 231-0345 commodate two drives. Sample units are available now; production quantities will be available in the second quarter of 1989. From \$31,500.

Mitsubishi Electronics America Inc, Computer Peripherals Div, 991 Knox St, Torrance, CA 90502. Phone (213) 515-3993.

Circle No 457



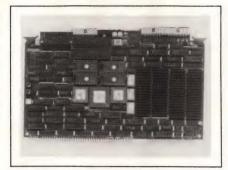
#### UNIX COPROCESSORS

- For the IBM PC/XT, PC/AT, PS/ 2 model 30 or 35 computers
- NS 32532 CPU simultaneously runs MS-DOS and Unix

The models 260PM and 270PM are part of the company's 200 Personal Mainframe family. The series consists of 32-bit Unix coprocessors that reside in IBM PC/XT, PC/AT, PS/2 model 30 or 35 computers as I/O processors and subsystems for workstations and multiuser systems. The models 260PM and 270PM use National Semiconduc-· tor's 32532 µP to provide simultaneous use of the MS-DOS and Unix System V operating systems. The 260PM operates at 25 MHz and achieves 8.5 MIPS of processing speed with 4M to 20M bytes of physical memory in a 4G-byte virtual address space. The 270PM operates at 30 MHz and a similar configuration provides 10 MIPS of performance. The boards utilize the 32381 floating-point processor for single- and double-precision IEEE format calculations. Model 260PM, \$6995; model 270PM, \$7995; floating-point unit, \$895.

Opus Systems, 20863 Stevens Creek Blvd, Bldg 400, Cupertino, CA 95014. Phone (408) 446-2110.

Circle No 458



#### MULTIBUS I SBC

- Features a 68030 μP having 8M to 32M bytes of RAM
- Has two multiprotocol RS-232C ports

The OB68K/MSBC30 single-board computer conforms to the IEEE-796 specification for Multibus I. The board features a 32-bit 68030 µP and 8M to 32M bytes of onboard zero-wait-state RAM with parity. It provides a 32-bit access to the RAM. In addition, a 68564 dual USART creates two multiprotocol RS-232C ports and a 68230 parallel interface/timer implements two 8bit parallel ports. An Omnimodule I/O connector lets you expand the number of serial ports and parallel ports, and add specialized I/O interfaces such as a SCSI or an IEEE-488. You can also add a 68881 or 68882 coprocessor and a 2-channel 68442 DMA controller. The board has a 2-year limited warranty. \$5995.

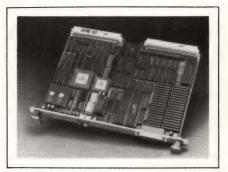
Omnibyte Corp, 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (312) 231-6880. TLX 210070.

Circle No 459

#### VME CPU BOARD

- Features a 25-MHz 68030 μP and 4M bytes of DRAM
- Contains four 28-pin sockets for ROM, EPROM, or EEPROM

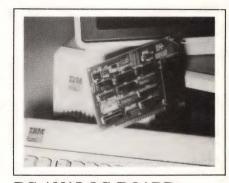
The MVME143 single-board computer for the VME Bus features a  $68030~\mu P$  with three versions: 16.7, 20, and 25~MHz. The board also contains a 68882 floating-point coprocessor operating at the same speed as the CPU. The board has 4M



bytes of dynamic RAM and four 28pin sockets for ROM, EPROM, or EEPROM. Using a Z8530 serial communications controller, the board provides two multiprotocol serial ports; it also has an RS-232C debug port on the front panel, using the MC68901 multifunction peripheral (MFP) chip. The MFP also provides four 8-bit timers. An MC68230 parallel interface/timer IC supplies a 24-bit timer that can generate autovectored interrupt to the CPU on level 4. Mostek's MK48T02 provides a battery-backed real-time clock and 2k bytes of batterybacked static RAM. \$2995.

Motorola Microcomputer Div, Marcom Dept, DW283, 2900 S Diablo Way, Tempe, AZ 85282. Phone (800) 556-1234, ext 230; in CA, (800) 441-2345, ext 230.

Circle No 460



#### PC ANALOG BOARD

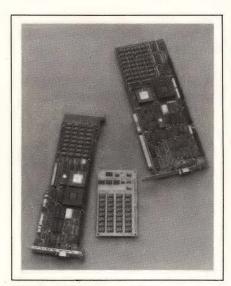
- Features eight single-ended input channels
- Board provides 8-bit resolution for a ±5V input voltage range
   The DAS-4 8-channel analog input board for the IBM PC, PC/XT, PC/ AT, and compatibles features an S/ H circuit and an A/D converter with

8-bit resolution. The input voltage

range is  $\pm 5V$ , and all inputs are protected for overvoltages as high as  $\pm 30$ V. The board has an external interrupt input that is jumper selectable to any of the PC/XT interrupt levels 2 through 7. The external interrupt allows the board to sample data based on the timing of an external event. The board also provides four digital outputs and three digital inputs that are compatible with TTL and CMOS levels. Each output can sink 8 mA of current. The board comes with a utility software package that contains a driver routine in assembly code, example programs, and initialization and setup routines. \$199; STA-U optional screw terminal board, \$115.

Metrabyte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX 508-880-0179. TLX 503989.

Circle No 461



#### GRAPHICS CARDS

- For the IBM Micro Channel and IBM PC/AT buses
- A proprietary 2-chip set provides 1024×768-pixel resolution

The Verticom HX-Series consists of four graphics coprocessor cards. Two of the boards, the HX16/AT and the HX256/AT, are compatible with the IBM PC/AT bus; the HX16/MC and HX256/MC are compatible with the IBM Micro Channel

bus. Both the HX16/AT and HX16/ MC offer 1M byte of memory and can display 16 simultaneous colors with as much as 1024×768-pixel noninterlaced resolution. The HX256/AT and HX256/MC provide 2M bytes of memory and can display 256 simultaneous colors with the same resolution. A proprietary 2-chip set supports the 8514/A Adapter Interface specification, making the boards compatible with an IBM 8514/A display adapter. The boards also support a VGA pass-through mode that permits the use of a VGA controller on the system bus. The HX-Series comes with the following drivers: 8514/A Adapter Interface, AutoCAD Rel 9 and 10, AutoSketch, AutoShade, Microsoft Windows 2, and Verticom Twin Focus. HX16/MC, \$2795; HX256/MC, \$3795; HX16/AT, \$2495; HX256/AT, \$3495.

Western Digital Imaging, 800 E Middlefield Rd, Mountain View, CA 94043. Phone (415) 960-3353.

Circle No 462

#### **DOT-MATRIX PRINTER**

- Prints letter quality at 60 cps and drafts at 180 cps
- Comes with 5 resident and 16 optional fonts

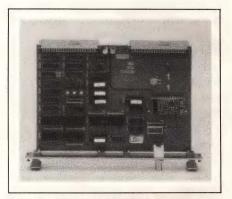
The ExpressWriter311 24-pin dotmatrix printer performs letterquality printing at 60 cps and a high-speed draft mode prints at 180 cps. The printer's five resident fonts are Courier, Prestige Elite, High-Speed Draft, Condensed, and Proportional. The printer has a card slot, which accepts 16 of the company's optional font cards. For software compatibility, the printer emulates three types of printers: Toshiba/Qume, IBM ProPrinter, and the Epson LQ Series. A Windows driver supports programs that run on Microsoft Windows 2.0/2.1 or Windows/386. The printer has a 16k-byte data buffer, and an additional 32k bytes of memory via a RAM card is available. A parallel



interface is standard and an RS-232C port is optional. The printer operates at <56 dB in normal mode and 53 dBA in quiet mode. The unit measures  $12.7 \times 16 \times 4.8$  in. and weighs 11 lbs. \$589.

**Toshiba America Inc,** Information System Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (714) 583-3000.

Circle No 463



#### VME ARCNET BOARD

- 2k-byte buffer holds four 508-byte packets
- Uses SMC's COM 9026 controller chip

The CC-121 VME Bus board provides a link to Arcnet's 2.5M-bps token-passing network. The board is based on SMC's COM 9026 controller chip. It contains a 2k-byte dual-port RAM with a 100-nsec access time for buffering as many as four 508-byte data packets. The board handles 10M-byte/sec databurst transfers on the VME Bus and supports a throughput of 1.5M bps on the Arcnet network, including software overhead. It transfers data packets to and from a star or optionally from a bus topology, us-

## **Euro-Connectors**

## **High Reliability and High Performance**

Level One (500 operations) and Level Two (400 operations)



STOCK AVAILABILITY: Signal Contacts Types B, C and R (Reverse); Power Contacts Type D, 5 ampere rated; Type M with Removable Shielded, Power and High Voltage Contacts; Reverse Ericcson Type and Half-C Type.

CONTACT VARIANTS: 16 to 96 contacts. SIGNAL CONTACTS: formed, copper alloy; female contact "Tulip Style," gold over nickel plated contact surfaces. Contact terminations offered in Printed Board Mount, Straight and 90°, Wrap Post, Press-Fit and Solder Hook. Selectively plated solder or gold terminations. REMOV-ABLE CONTACTS: Type M Connector, machined copper alloy. Power, 10 to 40 amperes, Shielded; 50 ohm, High Voltage, 2800 V (rms). AUXILIARY POWER CONNECTOR: eight, 16 ampere rated contacts, sequentially mated and designed for use with Euro-Connectors. INSULATORS: glass filled polyester, UL 94V-0. POLARIZATION: coding and "Ground before Signal Contact" options available.



### POSITRONIC INDUSTRIES, INC.

423 N. Campbell • Springfield, Mo. 65801
Tel. 417-866-2322 • 800-641-4054 • Telex 436445 • Fax 417-866-4115

**CIRCLE NO 16** 

#### **COMPUTERS & PERIPHERALS**

ing coaxial or fiber-optic cables. The board operates as a VME Bus slave with 8-bit access to the controller chip and board registers. The VME Bus has 8- or 16-bit access to the 2k-byte buffer. The VME Bus interface has a 7-level interrupt requester with a software-programmable interrupt vector. \$825 (100).

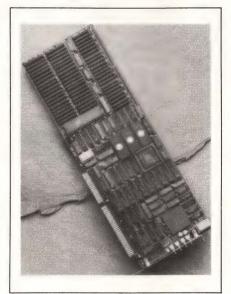
Compcontrol, Stratumsedijk 31, Postbus/Box 193, 5600 AD Einhoven, The Netherlands. Phone 040-124955. TLX 51603.

Circle No 464

#### **GRAPHICS CARD**

- Provides 1280×1024-pixel resolution for the IBM PC/AT
- Uses a TI 34010 processor and supports PGL drivers

The Artist Designer 12 graphics controller card for the IBM PC/AT, Compaq 386, and compatible computers provides 1280×1024-pixel resolution, using TI's 34010 graph-



ics processor chip. The board supports drivers for IBM's PGL (Professional Graphics Language) and for Graphic Software System's DGIS (Direct Graphics Interface Standard) via onboard firmware. The board displays 256 colors from a palette of 16.7 million colors. Its

resolution makes it suitable for solid modeling programs such as Autodesk's Autosolid software. Because the board is compatible with PGL and DGIS, it provides access to AutoCAD, VersaCAD, Lotus 1-2-3, Framework, Symphony, and many other professional-level software programs. The board operates with a horizontal scan rate of 64 kHz and a video bandwidth of 108 MHz. The frame buffer memory has 1.25M bytes of video RAM, and the system memory has 512k bytes of dynamic RAM. \$4495.

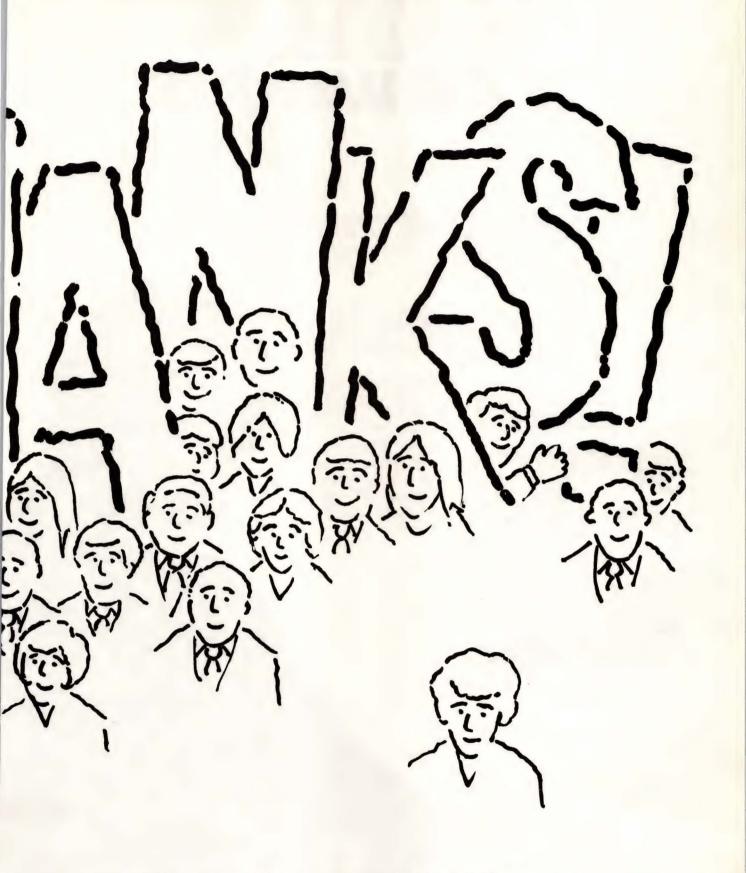
Control Systems, Box 64750, St Paul, MN 55113. Phone (612) 631-7800. TLX 756601.

Circle No 465

To EDN readers, for consistently votin EDN your favorite electronics

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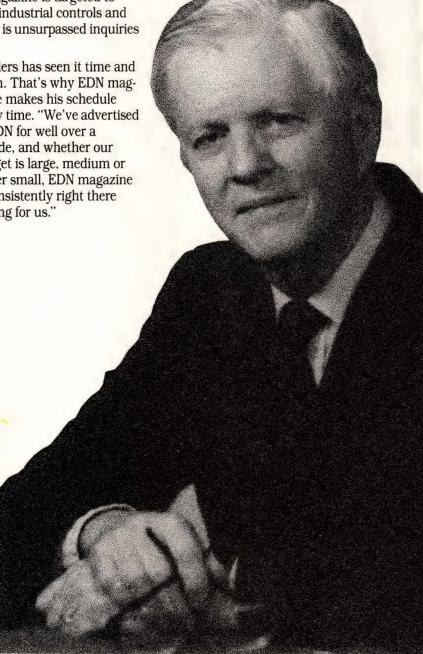
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### **NEW PRODUCTS**

#### **COMPONENTS & POWER SUPPLIES**

#### DC/DC CONVERTERS

- Accept any input between 18 and 72V dc
- Operate at 78% efficiency

Designed for 24 or 48V telecommunication systems, Models 48T5.12UW and 48T5.15UW accept any input between 18 and 72V dc. Both models provide a main output of 5V at 800 mA; secondary outputs are  $\pm 12V$  and  $\pm 15V$  for the 48T5.12UW and 48T5.15UW, respectively. The converters operate at 78% efficiency. A shutdown pin, which you can toggle on and off with an open-collector TTL/CMOS control signal, allows you to turn off the converters when the system requires no power. Key specifications include a 0.5% line regulation, a 3% load regulation, 20-mV p-p typ output noise, and a 500V dc isolation

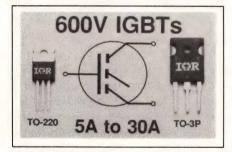


rating. Short-term stability measures 0.1% over 24 hours. The converters operate over a -25 to +80°C range and provide 8 hours min of short-circuit protection. \$50 (OEM qty). Delivery, stock to six

weeks ARO.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. FAX 415-932-6017.

Circle No 440



#### TRANSISTORS

- Offer continuous current ratings from 11 and 30A
- Single-pulse avalanche energy ranges as high as 100 mJ

The IRGBC20, IRGBC30, and IRGBC40 600V IGBTs (insulated-gate bipolar transistors) have a latch-free, repetitive avalanche rating, and at 25°C, they offer continuous current ratings of 11, 18, and 30A, respectively. Like power MOSFETs, the IGBTs are voltage-driven, gate-controlled devices. The IGBTs provide the added advantage of a low forward-voltage drop, which is 3V at a 25°C junction temperature. The devices' single-pulse avalanche energy ranges as

high as 100 mJ, and repetitive avalanche energy is as high as 12.5 mJ. All devices are housed in TO-220 packages. IRGBC20, \$3.60; IRGBC30, \$5.10; IRGBC40, \$9.40 (1000). Delivery, stock to eight weeks ARO.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 772-2000.

Circle No 441

#### **JUMPER**

- Has a 50Ω impedance
- Features 51 signal contacts

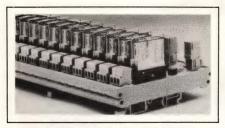
The Invisicon board-to-board jumper has a  $50\Omega$  characteristic impedance and terminations that are virtually invisible to even fast risetime signals. The 4-in.-long jumper has 51 signal contacts spaced on 0.025-in. centers. Hardware at both ends of the circuit provides 0.875 mm of wiping action during assembly. The circuit's cenellated contact pads provide scraping edges that remove dust particles and noncon-



ductive surface contaminants during the wiping action. The connector system combines traces on a circuit board with a controlled-impedance flexible circuit board. An elastomer with high stress retention maintains contact force and accommodates any gap tolerances in the system. The RO2500 material used for the system's flexible circuit has a  $2\frac{1}{2}$  dielectric constant, a 0.0025 dissipation factor, and 0.4% water absorption. \$105 to \$400.

Rogers Corp, Box 700, Chandler, AZ 85244. Phone (602) 963-4584.

Circle No 442



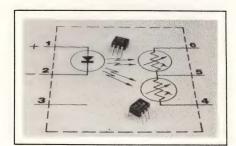
#### RELAY MODULES

- Provide outputs rated at either 10 or 16A
- Snap-mount onto either DIN-1 or DIN-3 rails

Series 20.000 relay interface modules simplify the design and packaging of programmable-controller output circuits. Available with 4, 8, or 16 plug-in relays, the modules snapmount onto DIN-1 and DIN-3 mounting rails. Relay input coils, rated for both ac and dc voltages, operate at 24, 48, 110 to 127, and 220V. Each relay in the module has one spdt output contact rated at either 10 or 16A. Built-in LEDs provide relay status and indicate the ac or dc input voltage. 8-relay module, \$138.32 (5).

Entrelec, 2 Ram Ridge Rd, Spring Valley, NY 10977. Phone (914) 425-7460. FAX 914-425-8108.

Circle No 443



#### **OPTOISOLATORS**

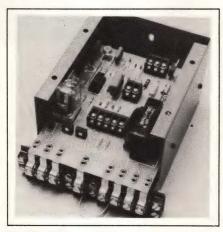
- Feature 2500V isolation
- Provide circuits for linear and logic functions

The CLM50/2 and CLM51/2 optoisolators are housed in a 6-pin DIP. Both incorporate a GaP light-emitting diode and two photoconductive cells, thereby providing separate circuits for both linear and logic functions. Specifications include a 250V peak line-voltage capability, 2500V peak isolation, and a 1 M $\Omega$ 

min off-resistance. Maximum cell on-resistance measures  $2^{1}/2$  k $\Omega$  at 16-mA drive currents for the CLM50/2 and  $4^{1}/2$  k $\Omega$  at 1 mA for the CLM51/2. Input-to-output capacitance for both devices equals 1.5 pF typ. Both isolators are UL recognized. \$1.35 to \$1.60 (1000).

Clairex Electronics, 560 S Third Ave, Mount Vernon, NY 10550. Phone (914) 664-6602.

Circle No 444



#### RELAY

- Operates with either voltage or current inputs
- Has programmable ranges

The Reflex 12M03-00101 is an industrial-grade relay that senses either voltage or current analog input signals. It provides an output contact that serves as a turn-on and turn-off signal or as an input for an alarm. Onboard jumpers allow you to program ac or de pickup or dropout points. Operating ranges of 0.1, 1, 10, 100, and 500V dc or ac are also user-programmable. The standard shunt provided with the relay accommodates a current range of 2 to 25A; an optional 50 mV shunt will extend the current range to thousands of amperes. The relay operates from 120V ac singlephase power lines. Setpoint, differential, and hysteresis adjustments are provided. \$212.

**Reflex Inc**, Box 1515, Providence, RI 02901. Phone (401) 941-4444.

Circle No 445



#### CONNECTORS

- Feature a quick connect/disconnect system
- Available in cable- and pc-boardmount versions

These circular connectors feature a self-latching, quick connect/disconnect system for use in confined places. They are made of polysulfone, which improves electrical insulation, heat resistance, and oil and chemical tolerance: the connectors can be autoclaved and exposed to temperatures from -100 to +150°C. The polysulfane material has a 94V-0 UL flammability rating. The connectors are available with two to nine contact positions and come in cable or pc-boardmount versions. Shell configurations include an in-line plug and a front- or rear-panel-mount receptacle. The units feature four keying possibilities to ensure keying exclusivity and/or color coding. From \$20.93 per mated pair. Delivery, stock to 12 weeks ARO.

**Lemo USA Inc,** Box 11488, Santa Rosa, CA 95406. Phone (707) 578-8811. TLX 340933.

Circle No 446

#### TRANSCEIVERS

- Meet Ethernet and IEEE LAN requirements
- Feature a switch for heartbeat selection

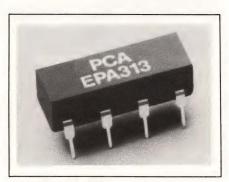
CentreCOM 200 Series baseband single-port transceivers feature an easily accessible on/off switch for heartbeat selection. They are available in a variety of connector configurations that meet the require-

# COMPONENTS & POWER SUPPLIES

ments of Ethernet Version 2.0 and IEEE 802.3 network coaxial cables. The transceivers include a number of diagnostic LED indicators. A 2color LED indicates heartbeat status-amber for heartbeat on, green for heartbeat off. A transmit LED shows when the terminal is transmitting: the LED's frequency of illumination and brightness are proportional to the network's traffic density. A receive LED indicates incoming traffic in the same manner. Another LED indicates the presence of signal quality error and is lit when it detects a collision. The transceivers are available for thickor thin-net coaxial cable applications. From \$245.

Allied Telesis Inc, 2672 Bayshore Parkway, Unit 900, Mountain View, CA 94043. Phone (415) 964-2771.

Circle No 447



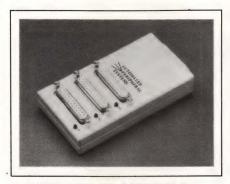
# **DELAY LINES**

- Feature three separate lines in a single package
- Include input and output buffers EPA313 Series delay lines provide three separate TTL-compatible delay lines in a single 14-pin DIP. Each of the delay lines in the 42 standard units have identical delay times ranging from 5 to 250 nsec  $\pm 5\%$  or  $\pm 2$  nsec, whichever is greater. Each delay line includes an input and an output buffer. Fan-out for the output buffer equals 20 TTL loads for the high level and 10 TTL loads for the low level. Output rise time measures 4 nsec max. Operating range spans 0 to 70°C. Custom units with special buffering and de-

lay times are also available. \$2.26 (1000). Delivery, stock to six weeks ARO

PCA Electronic Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761. FAX 818-894-5791.

Circle No 448



# CONNECTOR MODULE

- Allows three computers to share a single printer
- Requires no external power

The ScanCube allows as many as three personal computers to share one printer. The entire device connects directly to the printer's serial port and requires no external power supply. The ScanCube independently scans each of its three computer serial ports, locks onto any port transmitting data, stays with that computer port for a preset time-out, and then resumes scanning. The module accommodates all existing PC applications and requires no special tools. \$149.95.

Automated Peripheral Systems, 3131 E Monroe Ave, Orange, CA 92667. Phone (714) 997-3975.

Circle No 449

### CHASSIS

- Provides power and mounting for as many as three disk drives
- Complies with FCC requirements The SA-H116/2 chassis provides power and mounting for as many as three 5½-in. disk drives. Two drives that show through the front panel allow you to use removablemedia drives such as tapes and optical and floppy disks. A filler panel

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**CIRCLE NO 14** 

# **COMPONENTS & POWER SUPPLIES**

covers the unused slot for applications involving only one drive. The third drive also mounts near the front of the chassis but is concealed behind the front panel. In order to meet FCC requirements, the unit includes shielded connector data cables. The standard chassis connector configuration provides two 50-pin D subminiature connectors for

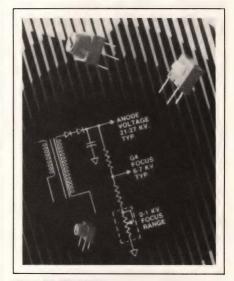


SCSI in and out. Other configurations are available. The H116/2 includes a 200W power supply and two fans. The supply operates from either 115 or 230V ac inputs and includes an unswitched ac outlet. \$586.

Sigma Information Systems, 3401 E LaPalma Ave, Anaheim, CA 92806. Phone (714) 630-6553.

Circle No 450





# TRIMMERS

- Feature a 1-kV voltage rating
- Sealed for operation in rugged environments

Designed for CRT adjustment applications, Model 3386-HV1 trimmers have a 1-kV max voltage rating. They feature an O-ring seal to provide reliable operation under dusty and humid conditions. Standard resistance values are 2.5 and 5 M $\Omega$ . Key specifications include a ±150-ppm/°C temperature coefficient, a 1% max contact resistance variation, and a 200-cycle min lifetime. Adjustability in the voltage divider and rheostat modes equals  $\pm 0.5$  and  $\pm 0.15\%$ , respectively. Standard knobs are available in white or blue; red knobs are optional. \$1.01 (1000). Delivery, stock to eight weeks ARO.

**Bourns Inc,** 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5500. TLX 676423.

Circle No 451

JAE Electronics, Inc.

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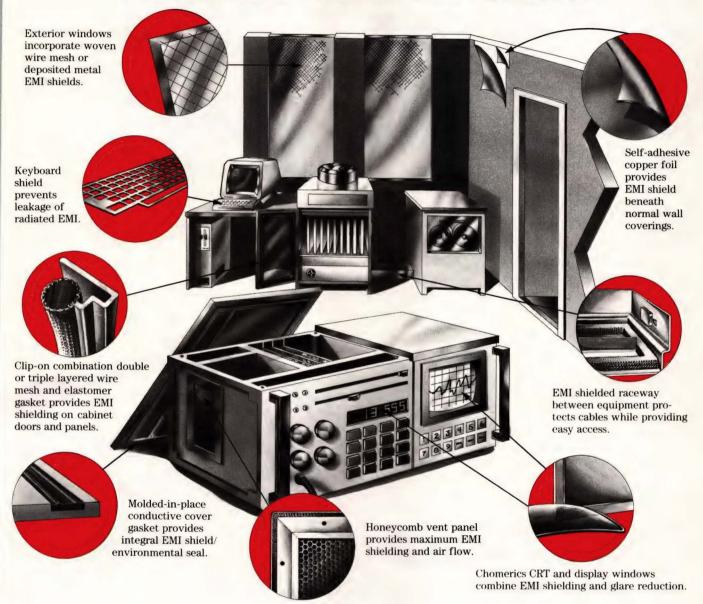
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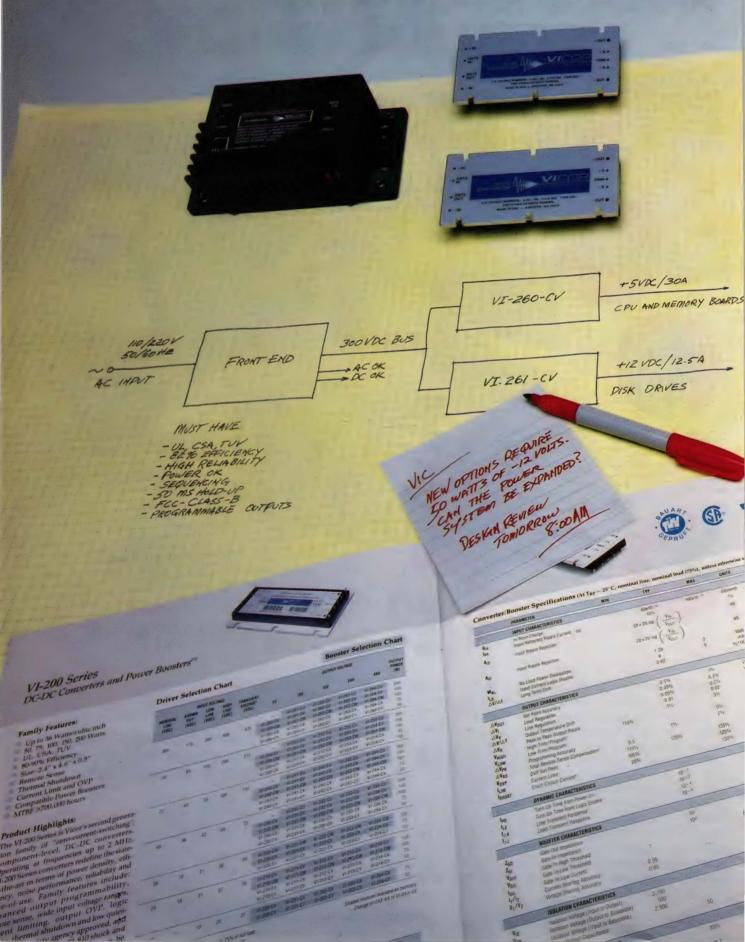
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# LEADER IN EMI SHIELDING INNOVATION, DESIGN, AND TESTING TECHNOLOGY.

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# **New Solutions From VICOR ...**



# **OFF-LINE Modular Power From 50 to 600 Watts!**

From AC line in, to highly regulated DC out, VICOR now offers the total design solution through a complete family of Off-Line Front End and DC/DC modular power components.

The system configuration changes...The power budget changes...What do you do about the power supply? If you are designing with modular power components, configuring the most effective power system is as straight forward as changing the mix of components used. Configurable Power...the most efficient and cost effective means to maintain flexibility and minimize time to market.

# **Off-Line Front Ends**

The Front Ends are available in output power ratings of 250, 500, and 750 Watts and are designed to deliver an unregulated 300 Volt DC bus to Vicor's VI-26X Series of DC/DC converter modules.

### FRONT END SELECTION CHART

	PAC	PACKAGE		OUTPUT POWER	
MODEL	PC MOUNT	CHASSIS MOUNT	250W	500W	750W
VI-FPE6-CUX			-		Jones W.
VI-FKE6-CUX		~	~		
VI-FPE6-CQX	~			~	
VI-FKE6-CQX				-	
VI-FPE6-CMX	-				-
VI-FKE6-CMX		-			-

	OPERATING PARAMETERS (ALL MODELS)										
INPUT VOLTAGE (VAC)											
NOM	LOW	HIGH	TRANSIENT (1 SEC								
110	90	135	150								
220	180	270	300								

Strappable to provide operation from 90 VAC to 270 VAC single phase lines, the Front Ends feature conducted EMI/RFI filtering to VDE/FCC A & B, 50 msec holdup, active inrush limiting and a BUS-OK status output. An opto-isolated AC-OK output is provided for advance warning of DC BUS dropout due to AC line failure.

# DC/DC Converters

The VI-26X Series is Vicor's family of 300 Volt input, "zero-current-switching," component-level, agency approved, DC/DC converters. These converters represent the state-of-the-art in terms of power density, efficiency, noise performance, reliability and ease-of-use. Available in 38 standard combinations of power rating and output voltage, the VI-26X Series modules in combination with the Front Ends, offer unprecedented flexibility in providing off-the-shelf solutions to virtually any off-line power requirements.



### CONVERTER/BOOSTER SELECTION CHART

Shaded modules available as boosters. Change VI-2XX-XX to VI-BXX-XX.

	OU	TPUT VOLTAG		OUTPUT POWER	
5V	12V	15V	24V	48V	(W)
10	VI-261-CU	VI-262-CU	VI-263-CU	VI-264-CU	200
VI-260-CV	VI-261-CV	VI-262-CV	VI-263-CV	VI-264-CV	150
VI-260-CW	VI-261-CW	VI-262-CW	VI-263-CW	VI-264-CW	100
VI-260-CX	VI-261-CX	VI-262-CX	VI-263-CX	VI-264-CX	75
VI-260-CY	VI-261-CY	VI-262-CY	VI-263-CY	VI-264-CY	50

\*Other output voltages from 2 to 100 Volts are available as semi-custom modules. Consult factory or see page 30 of the Vicor Product Catalog.



To Receive A Complete Catalog, Including Information On Vicor Products, Applications And Accessories, Call Vicor Today At (508) 470-2900 23 Frontage Road Andover, MA 01810.



Component Solutions For Your Power System
CIRCLE NO 127

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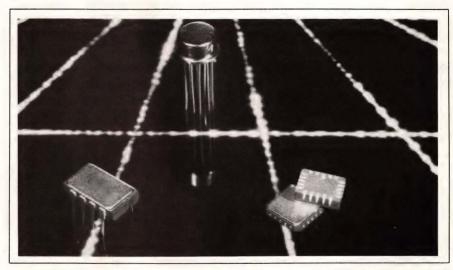
# **NEW PRODUCTS**

# INTEGRATED CIRCUITS

# **BIPOLAR OP AMP**

- Features a 1-GHz unity-gain bandwidth
- Has a 150V/µsec slew rate

Suited to video applications and high-speed data-acquisition systems, the HFA-0002 bipolar op amp offers a gain bandwidth of 1 GHz and a slew rate of 150V/µsec. The op amp also features an offset voltage of 0.7 mV and a high gain of 80V/mV. The HFA-0002 is available in an 8-lead TO-99 metal package, an 8-pin side-brazed ceramic DIP, or an 8-pin plastic DIP. The metal and ceramic packages operate over commercial, industrial, and military temperature ranges. The plastic package is specified for com-

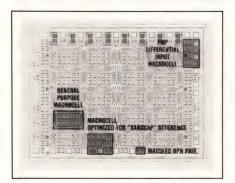


mercial and industrial use. From \$7.05 to \$38.15 (100).

Harris Corp, 1025 W Nasa Blvd,

Melbourne, FL 32919. Phone (407) 724-7800.

Circle No 382



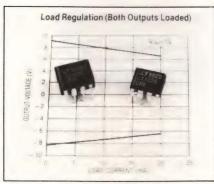
# LINEAR SEMICUSTOM IC

- Contains 20 macrocells
- Includes 8 high-current transistors

The Genesis 5000 linear array contains 20 macrocell tiles organized in a 4×5 matrix. One of these macrocells is configured as a bandgap voltage reference; you can configure the other 19 macrocells as a variety of standard analog functions. The 20,000-mil<sup>2</sup> chip also contains eight 200-mA npn transistors that you can use to implement an octal buffer, a dual H-bridge driver, or a quad push-pull output stage. You can use the low-offset matched npn pairs and the substrate pnp pairs to implement input stages of op amps and comparators. The Genesis 5000 contains 314 active components and 864 passive components. The typical NRE charge is \$7200. In a 16-pin plastic DIP, \$2.30 (50k).

Cherry Semiconductor Corp, 2000 S County Trail, E Greenwich, RI 02818. Phone (401) 885-3600.

Circle No 383



### DC/DC CONVERTER

- Accepts from 4 to 10V input
- Provides ±18V and 20 mA output

The LT1026 converts a single input to a higher-voltage dual output. For example, the chip can convert a single 5V supply to a  $\pm 9V$  output for use with op amps. Similarly, the chip will convert a 9V battery input

to a ±18V output. Because the chip uses bipolar switched-capacitor technology, it does not require an inductor. The LT1026 requires 1- $\mu$ F charge-pump capacitors and delivers a maximum output current of 20 mA. The IC is available in a plastic or ceramic DIP, a TO-5 metal package, or an 8-pin miniDIP. In an 8-pin miniDIP, \$2.10 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900.

Circle No 384

# **CMOS TIMER**

- Offers an 80-μA supply current
- Operates at 500 kHz

The ICM7555 CMOS timer replaces the NE/SE555 bipolar device for most applications. The supply-current requirement is 80 µA typ and the trigger, threshold, and reset currents are 20 pA typ. High-speed operation is guaranteed to 500 kHz, and the device operates over a guaranteed voltage range of 2 to 18V. In addition, the ICM7555 features a normal reset function; there is no need to crowbar the sup-

ply current during output transitions. The 50-mA driver can drive TTL/CMOS logic. The ICM7555 is available in commercial and industrial grades, and in 8-pin DIPs and SO packages. \$0.34 and \$0.46 (100).

Signetics Co, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

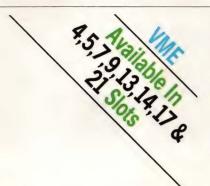
Circle No 385

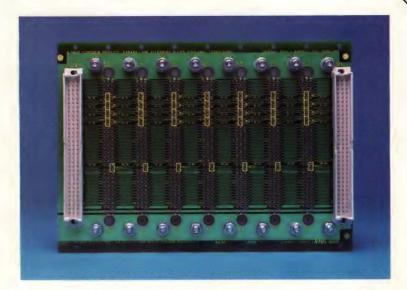
# A/D CONVERTERS

- Offer 12-bit resolution
- Have a 700-kHz throughput rate Featuring a digitally corrected subranging architecture and an internal sample/hold circuit, the ADS-125 and ADS-126 provide 12-bit resolution and a 700-kHz throughput rate. Both devices have a conversion time of 800 nsec max



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- $\square$  Impedence  $-60\Omega$  ( $\pm 2$ )
- $\Box$  Capacitance 77 pF ( $\pm 3$ )
- □ Crosstalk -<200 mV



**DAGE PRECISION INDUSTRIES, Inc.** 

46701 Fremont Blvd. Fremont, CA 94538 (415) 683-3930

**CIRCLE NO 12** 

and an acquisition time of 395 nsec max for sinusoidal inputs. The ADS-125 has pin-programmable input ranges of  $\pm 10V$  and 0 to 10V; the ADS-126 has ranges of  $\pm 2.5 \text{V}$ and 0 to 5V. Other features include TTL- and CMOS-compatible inputs and 3-state outputs. Output coding can be in Two's Complement, Complementary Two's Complement, Straight Binary/Offset Binary, or Complementary Binary/Complementary Offset Binary. Power requirements are  $\pm 15V$  and 5V dc. Packaged in 32-pin DIPs, the devices are available in commercial and military temperature-range versions. From \$250 to \$274 (1-24).

**Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. TLX 174388.

Circle No 386

# MICROCONTROLLERS

- Come in ROM and EPROM versions
- Based on 80C51 architecture

The 83C751 (ROM) and 87C751 (EPROM) are 8-bit microcontrollers based on the Intel 80C51 architecture. The 83C751 and the 87C751 are 40% smaller than the 40-pin Intel device. They contain 2k bytes of ROM and 64k bytes of RAM, as well as 19 I/O lines, an I2C serial port, a 16-bit reloadable counter/ timer, and a fixed-rate timer. In normal operation, the devices consume <55 mW of power at 12 MHz. The 83C751 ROM version is available in either a 24-pin DIP or a 28pin PLCC. The quartz-windowed 87C751 EPROM version comes in

# INTEGRATED CIRCUITS

a 24-pin ceramic DIP; it is also available as a one-time-programmable version in a 24-pin plastic DIP or a 28-pin PLCC. ROM version in plastic package, \$2.65.

**Signetics Corp,** Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

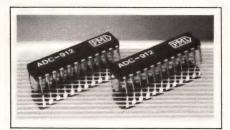
Circle No 387

encoder and decoder functions using a user-programmable Reed Solomon (random error correction) code to correct errors from 1 to 5 bytes. The on-the-fly correction is time independent of the error pattern and the number of errors, thus eliminating the need for additional  $\mu$ Ps and software to perform Reed Solomon encoding and decoding.

FEC applications require an AHA4510 at both ends of the channel; memory applications usually require a single chip. The chip is packaged in a 68-pin PLCC. \$100 (1000).

Advanced Hardware Architectures, Box 9669, Moscow, ID 83843. Phone (208) 883-8000. FAX 208-885-7893.

Circle No 389



# 12-BIT CMOS ADC

- µP compatible
- Features low transition noise

Fabricated in CMOS, the ADC-912 12-bit A/D converter has a lownoise comparator that exhibits <1/6 LSB of transition noise between codes. The ADC-912 has a 90-nsec bus-access time and a 12-usec conversion time when used with an external 1-MHz clock. Further, it is compatible with 8- or 16-bit data buses. An external -5V reference sets the 0 to 10V input range. Power consumption is 95 mW from 5V and -12V supplies. Package options include a 24-pin SOL package, a 24-pin DIP, or a 24-pin ceramic DIP. From \$19.95 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX 408-727-1550.

Circle No 388

### REED-SOLOMON CODEC

- Has a 15-MHz sustained byte rate
- Offers user-programmable byte correction

According to the manufacturer, the AHA4510 is the industry's first single-chip forward-error-correction (FEC) Reed Solomon codec that operates at a sustained byte rate of 15 MHz. The chip implements both



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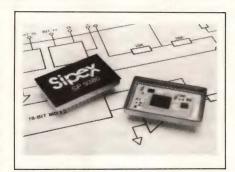
Measurement Systems, Inc.

121 Water Street, Norwalk, CT 06854 U.S.A. (203) 838-5561 CIRCLE NO 11

# D/A CONVERTER

- Features 18-bit resolution
- Offers 1/2 LSB accuracy

The SP9380 18-bit D/A converter uses a stable thin-film resistor process and a digitally decoded switching architecture to provide ½ LSB accuracy for both differential and integral linearity. The SP9380 contains a precision reference, input





# Reliability

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### The Reliable Company

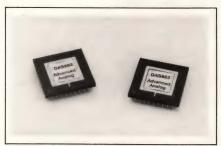
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data latches, and an output amplifier. Voltage-output settling time to 0.00019% is 30 µsec for a 10V step and 50 µsec for a 20V step. Analog output-voltage ranges are pin programmable for 0 to 5V, 0 to 10V,  $\pm 5V$ , and  $\pm 10V$ . Differential nonlinearity stability is 1 ppm/1000 hours at 25°C and 16 ppm/168 hours at 125°C. The SP9380 operates from ±15V supplies and is packaged in a 32-pin hermetic triple-DIP. Four product grades are available. From \$200 to \$475 (100).

Sipex Corp, Hybrid Systems Div, 22 Linnell Circle, Billerica, MA 01821. Phone (508) 667-8700. FAX 508-667-8310.

Circle No 390



# DATA ACQUISITION ICS

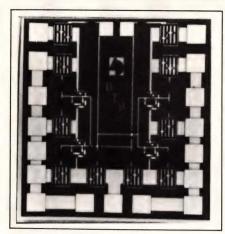
• Have 8- to 12-bit accuracy

• Feature selectable input ranges The DAS862 and DAS863 are complete data-acquisition subsystems that feature 8-bit accuracy at 45 kHz and 12-bit accuracy at 33 kHz. The chips provide selectable input ranges for unipolar or bipolar operation: 0 to 10V,  $\pm 5$ V, and  $\pm 10$ V. The DAS862 and DAS863 contain an input multiplexer, an instrumentation amplifier, a sample/hold amplifier, and an A/D converter with a μP interface and 3-state buffers. The DAS862 input multiplexer has 16 single-ended inputs and the DAS863 has 8 differential inputs. The devices come in 1-in.-square ceramic LCCs or pin-grid-array packages. Military screening is available. From \$89 (500).

Advanced Analog, 2270 Martin Ave. Santa Clara, CA 95050. Phone (408) 988-4930. FAX 408-988-2702.

Circle No 391

# INTEGRATED CIRCUITS



# **MMIC SWITCHES**

- Suited to spdt operation
- Feature 4- and 12-GHz performance

The ASW40010 and ASW12010 are monolithic microwave integrated circuit (MMIC) spdt switches designed for operation from dc to 4 GHz and dc to 12 GHz, respectively. Both switches feature a <2-nsec switching time, a 1.6:1 I/O VSWR, and a 25-dBm third-order intercept. The ASW40010 has an insertion loss of 0.8 dB at 500 MHz and 1.0 dB at 4 GHz; isolation is 65 dB and 45 dB at respective frequencies. The wider-bandwidth ASW12010 has an insertion loss of 2.0 dB from dc to 12 GHz and an isolation of 30 dB. ASW40010, \$21.60; ASW12010, \$53.00 (100).

**Anadigics Inc,** 35 Technology Dr, Warren, NJ 07060. Phone (201) 668-5000. FAX 201-668-5068.

Circle No 392

# OCTAL FLIP-FLOPS

- D-type with reset
- Available in two versions

The CD54/74AC/ACT273 devices incorporate 8 D-type flip-flops in a single package. Data on the D input of each flip-flop is transferred to the Q output on the positive-going edge of a common clock pulse. A low-level signal (logic 0) applied to the master-reset line clears all flip-flops, independent of the input clock. With a 5V supply and a 50-pF load, the minimum propagation de-

# Polaroid's Ultrasonic Ranging System opens the door to new technology.

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# ELECTRONICS CORP.

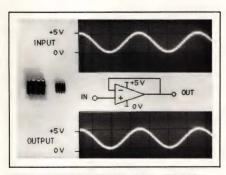
2380 Qume Drive, Suite A San Jose, CA 95131 (408) 434-0877 Fax # (408) 434-0539 Telex 279366

# INTEGRATED CIRCUITS

lay from a clock-pulse input to data output is 3½ nsec over the full military temperature range. The CD54/74AC version is for all-CMOS system designs; the CD54/74ACT version is intended to replace bipolar TTL devices. In a 20-pin plastic DIP, \$1.49 (100).

**GE Solid State**, Box 2900, Somerville, NJ 08876. Phone (201) 685-6562.

INQUIRE DIRECT



# MICROPOWER OP AMP

- Operates from single or dual supplies
- Requires a 40-µA max supply current

The ALD-1706 op amp requires a supply current of 20 µA typ and 40 µA max. The chip operates from either a single supply of 2 to 12V or dual supplies of  $\pm 1$  to  $\pm 6$ V. Because the ALD-1706 is fabricated in silicon-gate CMOS, it has an input bias current of 1 pA typ and 30 pA max, and an input resistance of  $10^{12}\Omega$  typ. When operating from a 21/2V supply, it has a large-signal voltage gain of 100,000 and a settling time of 10 µsec within 0.1%. Other features include a 400-kHz bandwidth and a 0.17V/µsec slew rate. The chip, which is internally compensated for unity-gain stability and does not need a nulling resistor, provides more than 70° of phase margin at the unity-gain frequency. The ALD-1706 is available in four grades with an 8-pin DIP. From \$0.89 (10,000).

Advanced Linear Devices Inc, 1180F Miraloma Way, Sunnyvale, CA 94086. Phone (408) 720-8737.

Circle No 393

# 1989

# EDN

CALENDAR

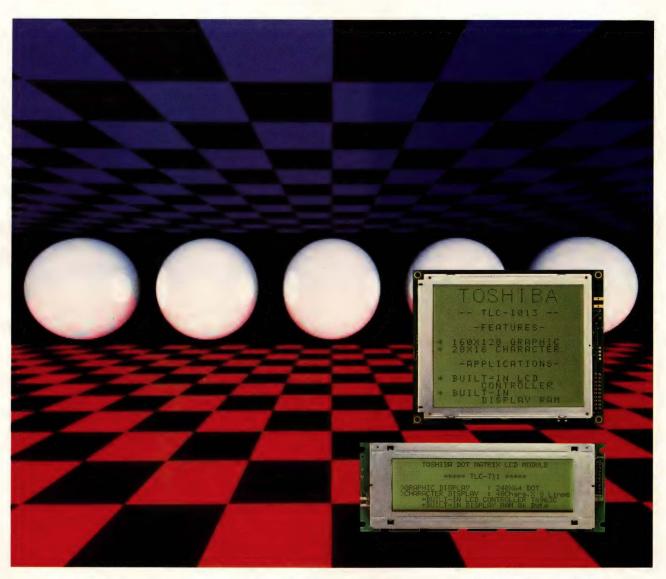
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# JANUARY 1989



MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
2	3	4	5	6	7
9	10	11	12	13	14
MARTIN LUTHER KING, JR. DAY	17	18	19	20	21
23	24	25	26	27	28
30	31				
	9  16  MARTIN LUTHER KING, JR. DAY  23	2 3 9 10 16 17 MARTIN LUTHER KING, JR. DAY 23 24	MONDAY   TUESDAY   WEDNESDAY	MONDAY   TUESDAY   WEDNESDAY   THURSDAY	MONDAY

•3-5 1989 International Conference on Wafer Scale Integration
Fairmont Hotel, San Francisco, CA (Prof. Earl Swartzlander, c/o TRW, R212076,
One Space Park, Redondo Beach, CA 90278, 213/812-0791)

One Space Park, Redondo Deadri, CA 90276, 213/012-0791)

5 OEM Peripheral ICC
Irvine Hilton & Towers, Irvine, CA (Invitational Computer Conferences, 3151
Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

-3-6 22nd Hawaii International Conference on System Sciences Kona Surf Resort, Kailua-Kona, Hawaii (Pamela S. Harrington, University of

Hawaii, 2404 Maile Way, B-101, Honolulu, HI 96822, 808/948-7396)
-16-17 Career Expo

Columbus OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

•18 Basic Integrated Circuit Technology Seminar
Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale,

AZ 85260, 602/998-9780)

-18-19 Exploitable UK Research for Manufacturing Industry
London, United Kingdom (IEE, Savoy Place, London WC2R OBL, United Kingdom)

•18-21 Internepcon Japan Tokyo, Japan (Jean D. Skolnik, Cahners Exposition Group, 1350 E. Touhy Avenue, Des Plaines, IL 60017, 312/299-9311)

•19 OEM Peripheral ICC
Park Hilton Munich, Munich, W. Germany (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

-19 Status 1989

Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•22-26 Energy Sources Technology Conference & Exposition Houston, TX (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•23-26 ATE & Instrumentation Conference West

Disneyland Hotel, Anaheim, CA (Lisa Palange, MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-3976)

-24 OEM Peripheral ICC

Ft. Lauderdale Marriott Hotel/Marina, Ft. Lauderdale, FL (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-

•24-26 1989 Annual Reliability and Maintainability Symposium Atlanta Peach Tree Plaza Hotel, Atlanta, GA (V. R. Monshaw, RCA, Astro-Electronics, P.O. Box 800 MS 55, Princeton, NJ 08540, 609/426-2182)

•25 Basic Integrated Circuit Technology Seminar

SunBurst Resort, Scottsdale, AZ (Patricia Fruscello, ICE, 15022 N. 75th Street,

Scottsdale, AZ 85260, 602/998-9780)

•25-26 1989 San Diego Electronics Show

Del Mar Fairgrounds, Del Mar, CA (Harry Schwartz, President, Epic Enterprises, Show Management, 3838 Camino Del Rio N., Suite 164, San Diego, CA 92198, 619/284-9268)

•26 OEM Peripheral ICC

Il Leonardi Di Vinci, Milano, Italy (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

•26 Status 1989

SunBurst Resort, Scottsdale, AZ (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-29 1989 Power Engineering Society Winter Meeting New York, NY (Julius G. Derse, 130 Country Club Road, Bedminister, NJ 07921 201/725-4388)

•29-Feb. 3 1989 Power Engineering Society Winter Meeting New York Penta Hotel, New York, NY (Julius Derse, 130 Country Club Road,

Bedminister, NJ 07921, 201/725-4388)

•30-31 Career Expo

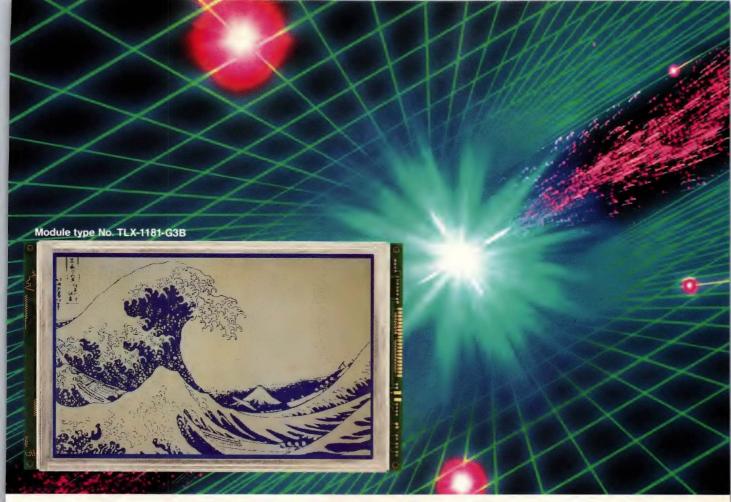
Melbourne/Orlando, FL (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

•30-Feb. 2 1989 Florida Instructional Computing Conference IX Hyatt Orlando Hotel, Kissimmee, FL(Dr. Jan Richardson, ISDT, 1590 Eaton

Way, Annapolis, MD 21401, 301/849-2274)

-31 OEM Peripheral ICC

Hotel Sofitel Paris, Paris, France (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)



# When your eyes need high quality displays, you need the Toshiba ST LCD.

Once again Toshiba has made a breakthrough in display quality. Clear and beautiful displays are achieved with the ST LCD. The LCD for the new age. And for your eyes. Now, by employing a new operating mode, this module provides excellent readability from a viewing angle perpendicular to the LCD panel. This was difficult to achieve with conventional LCDs. The aim was to make our LCD easier on the eyes. We succeeded with the ST LCD. Just another improvement in the man-to-machine interface by Toshiba.

### ST LCD Module Specifications

Model name	Number of dots	Dot pitch (mm)	Outline dimensions (mm)	Recommended controller	Built-in EL module
TLX-1181	640 × 400	$0.35 \times 0.35$	276 × 168 × 12	T7779	TLX-1181-EO
TLX-1181-G3B	640 × 400	$0.35 \times 0.35$	276 × 168 × 12	T7779	*
TLX-561	640 × 200	$0.35 \times 0.49$	275 × 126 × 14	T7779	TLX-562-EO
TLX-1342-G3B	640 × 200	$0.35 \times 0.49$	275 × 126 × 14	T7779	*
TLX-932	640 × 200	$0.375 \times 0.375$	293 × 97.6 × 14	T7779	-
TLX-1241	480 × 128	$0.48 \times 0.48$	277 × 86 × 14	T7779	-
TLX-1301V	240 × 128	$0.70 \times 0.70$	241 × 125.3 × 12	(T6963C)	_
TLX-1013	160 × 128	$0.60 \times 0.60$	129 × 104.5 × 14	(T6963C)	TLX-1013-EO
TLX-711A	240 × 64	$0.53 \times 0.53$	180 × 65 × 12	(T6963C)	TLX-711A-EO
TLX-1021	120 × 64	$0.48 \times 0.60$	85 × 70 × 20	(T6963C)	TLX-1021-EO
TLX-1391	128 × 128	$0.43 \times 0.43$	85 × 100 × 14	(T6963C)	TLX-1391-EO
TLX-341AK	128 × 128	$0.45 \times 0.45$	93.2 × 86.6 × 12	T6963C	-
TLX-761	640 × 64	$0.38 \times 0.42$	320 × 47 × 14	T6963C	_

( ): Built-in controller, \*: B-ST, built-in EL module

In Touch with Tomorrow
TOSHIBA

Toshiba America, Inc., Chicago Office: One Parkway North, Suite 500, Deerfield, IL 60015-2547 Tel: 312-945-1500 Western Area Office: 2021 The Alameda, Suite 220, San Jose, CA 95126 Tel: 408-244-4070 Eastern Area Office: 25 Mall Road, 5th Floor, Burlington, MA 01803 Tel: 617-272-4352

# FERRIJARV 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
			1	2	3	4
5	6	7	8 ASH WEDNESDAY	9	10	11
12 LIN- COLN'S BIRTH- DAY	13	14	15	16	17	18
19	20 WASHINGTON'S BIRTHDAY	21	22	23	24	25
26	27	28				

-1 Basic Integrated Circuit Technology Seminar Hyatt Regency, Dallas, TX (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•2 Computer Reseller ICC Stouffer Waverly Hotel, Atlanta, GA (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

•2 Status 1989

Hyatt Regency, Dallas, TX (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-5-7 Safecon/89

Fairmont Hotel, San Jose, CA (Anne Weber, MultiDynamics, 13762 Newport Avenue #204, Tustin, CA 92680, 714/669-1201)

•6 Computer Graphics ICC

Red Lion Inn, San Jose, CA (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171) -6-8 Communication Networks 1989

Washington Convention Center, Washington, D.C. (Hajar Associates Inc., Suite 1, 45 Walpole Street, Norwood, MA 02062, 617/769-8950)

-6-10 1989 Integrated and Guided Wave Optics (IGWO '89)

Houston Convention Center, Houston, TX (IEEE Headquarters, 345 East 47th

Street, New York, NY 10017)

7 Semiconductor Packaging

Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•7-9 Buscon West

Santa Clara Convention Center, Santa Clara, CA (CMC, 200 Connecticut Avenue, Norwalk, CT 06856, 203/852-0500, x232)

8 Basic Integrated Circuit Technology Seminar
 Hyatt Regency, Dallas, TX (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-8-10 Practical Integrated Circuit Fabrication Seminar

Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•9 Status 1989

Le Meridien, Newport Beach, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-9-12 14th West Coast Computer Fair

Moscone Center, San Francisco, CA (Interface, 300 First Avenue, Needham, MA 02194, 617/449-6600)

12-16 Saudi Elenex Riyadh '89 Riyadh Exhibition Centre, Riyadh, Saudi Arabia (Gerald G. Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450, 201/652-7070)

-13-14 Career Expo

St. Louis, MO (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

-15 Basic Integrated Circuit Technology Seminar
Omni Parker House, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•15 Computer Graphics ICC

Boston Marriott Hotels Newton, Newton, MA (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-

·16 Status 1989

Omni Parker House, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street,

Commit Parker House, Buston, MA (Fathica Pruscello, ICE, 19022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•21 OEM Peripheral ICC

Hyatt Regency Bellevue, Bellevue, WA (Invitational Computer Conference, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

-21-23 CSC 89 - Computer Science Conference
Commonwealth Convention Center, Louisville, KY (Arthur Riehl, Department of Engineering, Mathematics & Computer Science, University of Louisville, Louisville, KY 40292)

•22 Basic Integrated Circuit Technology Seminar
Hotel International, Zurich, Switzerland (Patricia Fruscello, ICE, 15022 N. 75th
Street, Scottsdale, AZ 85260, 602/998-9780)

-22-25 Expo Hospital

El Pres. Chap. Hotel, Mexico City (MIC, P.O. Box 4749, Arlington, VA 22204, 703/685-0600)

-23 Status 1989

Hotel International, Zurich, Switzerland (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-27-28 Career Expo

Cincinnati, OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030) -28-Mar. 2 NetWorld '89

Hynes Convention Center, Boston, MA (Annie T. Zdinak, H. A. Bruno, Inc., 385 Sylvan Avenue, Englewood Cliffs, NJ 07632, 201/569-8542)
-28-Mar. 2 Uniforum

Moscone Center, San Francisco, CA (Patricia Fruscello, ICE, 15022 N. 75th

Street, Scottsdale, AZ 85260, 602/998-9780)

-28-Mar. 3 MEXICO ComExpo
National Auditorium, Mexico City (MIC, P.O. Box 4749, Arlington, VA 22204, 703/685-0600)





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CIRCLE NO 55

# MARCH 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17 ST. PATRICK'S DAY	18
19 PALM SUNDAY	20	21	22	23	24  GOOD FRIDAY	25
26  EASTER SUNDAY	27	28	29	30	31	

•1 Live Videoconferences Via Satellite Network - Self Testing of ICs (Jeff Mathuran, Videoconference Services, The Learning Channel, 1525 Wilson Boulevard, Suite 550, Rosslyn, VA 22209, 800/346-0032)
•1-3 1989 Topical Meeting on Photonic Switching Santa Fe, NM (IEEE/LEOS IEEE Service Center, 455 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855, 201/562-5564)

·2 Computer Reseller ICC

Boston Marriott Cambridge, Cambridge, MA (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-

-6-9 FOSE '89, FOSE Software '89, FOSE Computer Graphics '89 Washington Convention Center, Washington, DC (Linda Carter, National Trade Productions, Inc., 2111 Eisenhower Avenue, Suite 400, Alexandria, VA 22314, 800/638-8510)

•7-9 Nepcon West

Anaheim Convention Center, Anaheim, CA (Jerry Carter, Cahners Exposition Group, 1350 East Touhy Avenue, Des Plaines, IL 60017, 312/299-9311) -7-9 8th International Zurich Symposium and Technical Exhibition

on Electromagnetic Compatibility
Zurich, Switzerland (Prof. Dr. T. Dvorak, ETH Zentrum-IKT, 8092 Zurich,
Switzerland, 411/256-2790, Fax: 411/690-943)

-7-9 SEMICON/Europa

Zuspa Convention Center, Zurich, Switzerland (SEMI, 805 East Middlefield Road, Mountain View, CA 94043, 415/964-5111)

•7-9 Statistical Process Control Workshop

Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-9-10 The Executive Forum on Supercomputing

Fairmont Hotel, San Jose, CA (Pat Westly, Westly Enterprises, 3697 South Court, Palo Alto, CA 94306, 415/494-7115)

10-12 Technology Executives Conference
Denver, CO (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•13-14 1989 International Conference on Microelectronic Test Structures

Caledonian Hotel, Edinburgh, UK (Professor Anthony Walton, Dept. of Electrical Engineering, Kings Building, Edinburgh University, Edinburgh EH9 3JL, Scotland, 031/667 1081 (ext. 3261)

13-15 House World Expo

Jacob K. Javits Convention Center, New York, NY (Interface, 300 First Avenue, Needham, MA 02194, 617/449-6600)

•13-16 Interface '89

Jacob K. Javits Convention Center, New York, NY (Interlace, 300 First Avenue, Needham, MA 02194, 617/449-6600)

Needmann, MA 02194, 617/449-6600)
+13-17 1989 IEEE Applied Power Electronics Conference and Exposition - APEC '89

Baltimore Convention Center, Baltimore, MD (Ann Ryland, Courtesy Associates, 655 15th Street, N.W., Suite 300, Washington, D.C. 20005, 202/347-5900)
-14-15 Failure Analysis/Avoidance of Integrated Circuits Seminar SunBurst Resort, Scottsdale, AZ (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•14-16 Internepcon U.K.

National Exposition Center, Birmingham, England (Jean D. Skolnik, Cahners Exposition Group, 1350 East Touhy Avenue, Des Plaines, IL 60017, 312/299-

•14-16 Semiconductor International U.K.

National Exposition Center, Birmingham, England (Jean D. Skolnik, Cahners Exposition Group, 1350 East Touhy Avenue, Des Plaines, IL 60017, 312/299-

•16 OEM Peripheral ICC

Red Lion Inn, San Jose, CA (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

•20-21 Career Expo

Huntsville, AL (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030) •20-23 1989 IEEE Particle Accelerator Conference

Hyatt Regency Hotel, Chicago, IL (Dr. Francis T. Cole and Donald Young, Fermi National Accelerator Laboratory, P.O. Box 500, MS #347, Batavia, IL 60510, 312/840-3801)

-27-28 Career Expo

Indianapolis, IN (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030) -28 OEM Peripheral ICC

Omni Europa Hotel, Chapel Hill, NC (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

-28-30 Southcon/89

Georgia World Congress Center, Atlanta, GA (Alexes Razevich, Electronic

Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)

\*28-31 Intermag '89
Mayflower Hotel, Washington, DC (Ralph W. Patterson, Hewlett Packard, 1501

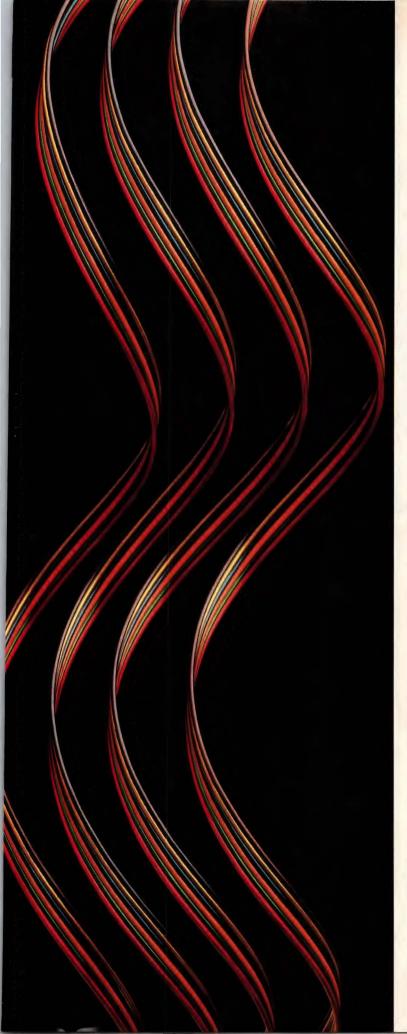
Page Mill Road, Palo Alto, CA 94303, 415/857-1501)

•29-30 1989 IEEE/AESS National Radar Conference
Sheraton Park Central Hotel & Towers, Dallas, TX (Russell Logan, Chairman, Texas Instrument, P.O. Box 801, Mail Station 8045, McKinney, TX 75069,

214/952-3151)

•29-31 WCC - World Congress on Computing
McCormick Place, Chicago, IL (Interface, 300 First Avenue, Needham, MA 02194, 617/449-6600)

•30-Apr. 1 Internepcon/Semiconductor Korea Seoul, Korea ((Jean D. Skolnik, Cahners Exposition Group, 1350 East Touhy Avenue, Des Plaines, IL 60017, 312/299-9311)





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APRIL 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
						1
2	3	4	5	6	7	8 .
9	10	11	12	13	14	15
16	17	18	19	20 PASSOVER	21	22
23 30	24	25	26	27	28	29

•2-4 Solar Energy Conference, International
San Diego, CA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•2-7 International Offshore Mechanics and Artic Engineering Conference

Hague, Netherlands (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•3-7 1989 IEEE International Conference on Control and

**Applications** 

Hyatt Regency Hotel, Jerusalem, Israel (Jurgen Ackermann, DFVLR, Oberpfaffenhofen, 8031 Wessling, West Germany, 40/8513 281)

•6 Live Videoconferences Via Satellite Network - Robotic Devices (Jeff Mathuran, Videoconference Services, The Learning Channel, 1525 Wilson Boulevard, Suite 550, Rosslyn, VA 22209, 800/346-0032)

•7-11 SEMICON/Beijing

Beijing Exhibition Center, Beijing, China (SEMI, 805 East Middlefield Road, Mountain View, CA 94043, 415/964-5111)

-9-12 Southeastcon '89

Swearingen Engineering Center, Univ. of South Carolina, Columbia, SC (Dr. Joseph M. Bienbach, University of South Carolina, Swearingen Engineering Center, Columbia, SC 29208, 803/777-6693)

•10-12 1989 International Workshop on Industrial Applications of Machine Intelligence and Vision

University of Tokyo, Tokyo, Japan (Prof. Mitsuru Ishizuka, Institute of Industrial Science, University of Tokyo, 7-22-1 Roppongi, Minato-ku, Tokyo 106, Japan, 81/3-402-6231)

Detroit, MI (Engineers Expo and Software/Data Processing Career Fair Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030) •10-13 1989 International Reliability Physics Symposium Hyatt Regency Phoenix, Phoenix, AZ (Alfred L. Tamburrino, RADC/RBRP, Griffiss AFB N.Y. 13441, 315/330-2813)

•10-13 Comdex Spring

McCormick Place, Chicago, IL (Interface, 300 First Avenue, Needham, MA 02194, 617/449-6600)

•10-13 Electronic Imaging Conference West

The Pasadena Center, Pasadena, CA (Lisa Palange, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-3976)

•10-13 Semiconductor China

Shanghai/PRC (Jean D. Skolnik, Cahners Exposition Group, 1350 East Touhy Avenue, Des Plaines, IL 60017, 312/299-9311)

•11-12 Training Workshop for Visual Inspection of ICs and Hybrids Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•11-13 Electro/89
Jacob K. Javits Convention Center, New York, NY (Alexes Razevich, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045,

•11-13 MELÉCON '89 - Mediterranean Electrotechnical Conference Forum Picoas, Lisbon, Portugal (Prof. Manuel de Medeiros Sil, CEAUTL, Instituto Superior Tecnico, Avenida Rovisco Pais, 1096 Lisbon, Portugal, +351 1 80 06 37, Telex: 63423 ISTUTL P)

-17-20 NCGA '89

Philadelphia Civic Center, Philadelphia, PA (Sharon Sutton, National Computer Graphics Association, 2722 Merrilee Drive, Suite 200, Fairfax, VA 22031, 703/698-9600)

-18-20 Statistical Process Control Workshop Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•20 Computer Reseller ICC
Hotel International Zurich, Zurich, Switzerland (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

•24 OEM Peripheral ICC

Sheraton Tara Hotel, Nashua, NH (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

•24-25 Career Expo

Chicago, IL (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030) -24-26 American Power Conference

Chicago, IL (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

Palmer House, Chicago, IL (Interface, 300 First Avenue, Needham, MA 02194, 617/449-6600)

-24-27 Infocom '89

Westin Hotel, Ottawa, Canada (Celia Desmond, Telecom Canada, 483 Bay Street, 5th Floor So., Toronto, Ontario, M5G-2E1 Canada, 416/581-2318) 24-27 Spring National Design Engineering Conference & Show Chicago, IL (The American Society of Mechanical Engineers, 345 East 47th

Street, New York, NY 10017, 212/705-7785)

-25-27 CITEX - Computer Industry Trade Exposition
Georgia World Congress Center, Atlanta, GA (Annie T. Zdinak, H. A. Bruno, Inc.,

385 Sylvan Avenue, Englewood Cliffs, NJ 07632, 201/569-8542)
-25-27 IMTC '89 - 1989 IEEE Instrumentation and Measurement Technology Conference

Key Bridge Marriott Hotel, Arlington, VA (Robert Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/475-4571)

•25-27 BEW - British Electronics Week

Olympia, London, England (Evan Steadman Ltd., The Hub, 9 Emson Close, Saffron Walden, Essex, CB10 1HL, 0799 26699, Telex: 81653 a/b INFORM G)
-25-28 Worker in Transition

Chicago, IL (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•26 Computer Reseller ICC

London Hilton on Park Lane, London, England (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

-30-May 4 Conference on Human Factors in Computing Systems Stouffer's Austin Hotel, Austin, TX (Claudia Raun, MCC, 9390 Research Blvd., Kaleido II #328, Austin, TX 78759)



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abbott

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MAY 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29 MEMORIAL DAY	30	31			

•1-4 Offshore Technology Conference
Houston, TX (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

Sheraton & Towers Hotel, Seattle, WA (J. H. Spare, Philadelphia Electric Co., 2301 Market Street, Philadelphia, PA 19101, 215/841-4785)

-2-5 Command, Control, Communications and Management

Information Systems

Bournemouth International Conference Centre, UK (Conference Services Dept., IEE, Savoy Place, London, WC2R 0BL, UK, 01/240 1871, Telex: 261176 IEE LDNG)

 2-5 Design of Experiments Workshop
 Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•3 Live Videoconferences Via Satellite Network - Integrated Product Processing for Engineers: A New Challenge (Jeff Mathuran, Videoconference Services, The Learning Channel, 1525 Wilson

Boulevard, Suite 550, Rosslyn, VA 22209, 800/346-0032)

•8-11 1989 IAS Industrial & Commercial Power Systems
Conference - I&CPS '89

Palmer House, Chicago, IL (Dennis Lamont, Weldy-Lamont Assoc., 1008 E. Northwest Hwy., Mt. Prospect, IL 60056, 312/398-4510)
-8-12 Compeuro '89 - "VLSI and Computer Peripherals"

Hamburg, Federal Republic of Germany (Prof. W. E. Proebster, IBM Laboratory, P.O. Box 80 08 80, D-7000 Stuttgart 80, Federal Republic of Germany, 07031/16 39 29, Telex: 7265 705 IBM D)

9-11 1989 International Symposium on Circuits and Systems

ISCAS '89
Portland Hilton, Portland, OR (Dr. Tran Tong, Tektronix, Inc., P.O. Box 500, M.S. 50-370, Beaverton, OR 97077, 503/627-6109)

-9-11 EDS - Electronic Distribution Show and Conference Las Vegas Hilton Hotel, Las Vegas, NV (Janet Thelen, Market Communication Associates, 230 East Ohio Street, Chicago, IL 60611, 312-648-1140) 9-11 3rd Annual National FinCom

Jacob K. Javits Convention Center, New York, NY (Annie T. Zdinak, H. A. Bruno, Inc., 385 Sylvan Avenue, Englewood Cliffs, NJ 07632, 201/569-8542)

9-12 AUTOMAN - International Advanced Manufacturing Systems

**Exhibition and Conference** National Exhibition Centre, UK (Jean D. Skolnik, Cahners Exposition Group, 1350 East Touhy Avenue, Des Plaines, IL 60017, 312/299-9311)

-9-12 Venezuela ComExpo

Hilton Hotel, Caracas, Venezuela (MIC, P.O. Box 4749, Arlington, VA 22204,

703/685-0600)
•14-19 AEA Wharton/School Business Management Program Philadelphia, PA (Mary Horngren Frost, AEA, 5201 Great America Pkwy., Santa Clara, CA 95054, 408/987-4285)

•15-18 1989 Cement Industry Technical Conference
Fairmont Hotel, Denver, CO (Elroy D. Cook, Southwestern Portland Cement Company, P.O. Box 8789, Lyons, CO 80540, 303/823-6685)

•15-18 1989 Custom Integrated Circuits Conference - CICC '89 Town & Country Hotel, San Diego, CA (Laura A. Hayward, 1100 East Avenue, Rochester, NY 14601, 716/473-7515)

•15-18 Midwest Electronics Exposition
St. Paul Civic Center, St. Paul, MN (Lisa Palange, MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-3976)

•15-19 1989 International Conference on Robotics and Automation The Registry Resort, Scottsdale, AZ (Dr. George A. Bekey, University of Southern California, The Robotic Institute, Los Angeles, CA 90089) 17 Computer Graphics ICC

Frankfurt Sheraton Hotel, Frankfurt, W. Germany (Invitational Computer Conference, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-

•17-20 AEA Executive Marketing Forum
Monterey, CA (Susan Puleo, AEA, 5201 Great America Pkwy., Santa Clara, CA
95054, 408/987-4251)

95054, 408/987-4251)

•22-23 1989 Electronics Components Conference - ECC '89
Westin Hotel, Houston, TX (Peter J. Walsh, Electronic Industries Assoc., 2001
Eye Street, Washington, D.C. 20006, 202/457-4932)

•22-25 SUPERCOMM '89

Anaheim, CA (Telecommunications Industry Association, 150 North Michigan Avenue, Suite 600, Chicago, IL 60601)

-23 Computer Graphics ICC

Hotel Sofitel Paris, Paris, France (Invitational Computer Conference, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-0171)

-23-24 Career Expo

Dayton, OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSi Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

•23-25 1989 IEEE Electromagnetic Compatibility Symposium - EMC 89

Denver, CO (Mr. John W. Adams, 1435 Gillaspie Drive, Boulder, CO 80303, 303/497-3328) •23-25 SEMICON/West

San Mateo Fairgrounds, San Mateo, CA (SEMI, 805 East Middlefield Road,

San Mateo Fairgrounds, San Mateo, CA (SEMI, 805 East Middlefield Hoad, Mountain View, CA 94043, 415/964-5111)

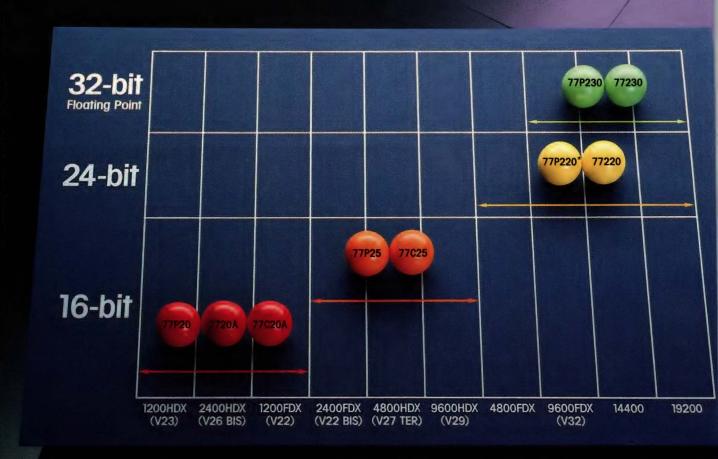
•31-June 2 43rd Annual Frequency Control Symposium

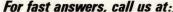
Denver Marriott Hotel, City Center, Denver, CO (Frequency Control Symposium, P.O. Box 826, Belmar, NJ 07719)



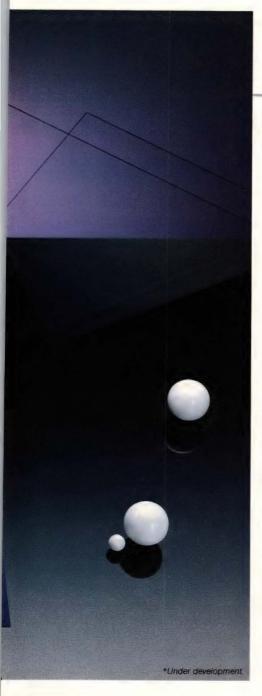
# The 16-bit sensation from

NEC's DSP family covers the entire MODEM spectrum





# the DSP pioneer.



New 16-bit DSP offers twice the speed, more than twice the memory of the 77C20A.

You've made NEC a part of your modem designs for years. Because we've led the industry with a whole series of pioneering devices — the 7720, 7720A, and 77C20A. Now our latest DSP powerhouse surges to the head of the 16-bit line.

The enhanced 77C25 gives you twice the performance of the 77C20A. We mean that literally. You get twice the speed — 122ns. And more than twice the memory capacity — 2K x 24 instruction ROM; 1K x 16 data ROM; 256 x 16 data RAM.

You can replace two 77C20As with one 77C25. There's almost no need to modify peripheral circuits. Power consumption is a mere 0.25W max.

The 77C25 comes in a 28-pin DIP or 44-pin PLCC. It's pin- and software-compatible at the source level with the 77C20A. Development tools are available off the shelf.

NEC also offers a choice of programmable versions:

☐ EPROM in CerDIP with window: 77P25D.

☐ OTP in plastic DIP: 77P25C.

☐ OTP in PLCC: 77P25L.



In addition, we supply socket adaptors (PA-77P25C/PA-77P25L) for programmers.

Whatever your modem design calls for, NEC's DSP family has the answers. From 1,200 to 19,200bps and everywhere in between, the DSP powerhouse has you covered. Call us on it, today.



II INF 1989

MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDA
			1	2	3
5	6	7	8	9	10
12	13	14 FLAG DAY	15	16	17
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•1 Computer Graphics ICC

London Hilton on Park Lane, London, England (Invitational Computer Conferences, 3151 Airway Avenue, Suite 32, Costa Mesa, CA 92626, 714/957-

•1-2 1989 IEEE Pacific Rim Conference on Communications,

Computers and Signal Processing
Empress Hotel, Victoria, B.C. (Dr. W. D. Little, Department of Electrical and Computer Engineering, University of Victoria, P.O. Box 1700 Victoria, B.C., V8W 2Y2, 604/721-7211)

-4-8 International Gas Turbine and Aeroengine Congress and Exposition

Toronto, Canada (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)
•5-8 The 1989 AIIM Show

Moscone Center, San Francisco, CA (Betty Garrett, The Association for Information & Image Management, 1100 Wayne Avenue, Suite 1100, Silver Spring, MD 20910, 301/587-8202)

-6-9 1989 IEEE IAS Pulp & Paper Industry Conference

Hyatt Regency, Dallas, TX (Alex Dean, The Rockbestos Co., 2995 LBJ Frwy., Suite 130, Dallas, TX 75234, 214/484-1077)

-11-14 1989 IEEE International Conference on Communications

Sheraton Boston, Boston, MA (Ed Elowe, Infocorp International, P.O. Box S, Brunswick, ME 04011, 207/833-5403)

•12-13 Career Expo

12-13 Career Expo
 Albuquerque, NM (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)
 12-14 1989 7th IEEE Pulsed Power Conference
 Monterey, CA (Bernard Bernstein, Physics International Co., 2700 Merced

Street, San Leandro, CA 94577, 415/577-7236)

•12-15 Nepcon East '89

Bayside Exposition Center/World Trade Center, Boston, MA (Janet Schafer, Cahners Exposition Group, 1350 E. Touhy Ave., Des Plaines, IL 60017,

-14-16 International Microwave Symposium & Workshops
Hyatt Regency Hotel, Long Beach, CA (C. W. Swift, C. W. Swift and Associates,
15216 Burbank Blvd., Van Nuys, CA 91411, 818/873-4778)

•18-22 Summer Annual Meeting/The American Society of

Mechanical Engineers
Pittsburgh, PA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

-19-22 ATE & Instrumentation Conference East World Trade Center, Boston, MA (Lisa Palange, MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-3976)

-20-22 2nd Annual National CASEcon (Computer Aided Software Engineering Conference & Show)

Jacob K. Javits Convention Center, New York, NY (Annie T. Zdinak, H. A. Bruno,

Jacob K. Javits Convention Center, New York, NY (Annie T. Zdinak, H. A. Bruno, Jacob K. Javits Convention Center, New York, NY (Annie T. Zdinak, H. A. Bruno,

Inc., 385 Sylvan Avenue, Englewood Cliffs, NJ 07632, 201/569-8542)

-21-23 1989 American Control Conference

Pittsburgh Hilton and Towers, Pittsburgh, PA (H. Vincent Poor, University of Illinois at Urbana-Champaign, 1101 West Springfield Ave., Urbana, IL 61801,

-25-28 1989 ACM/IEEE 26th Design Automation Conference Las Vegas Convention Center, Las Vegas, NV (P.O. Pistilli, MP Associates, 7366 Old Mill Trail, Boulder, CO 80301, 303/530-4562)

-26-27 Career Expo

Cleveland, OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030) •26-30 1989 IEEE Antennas and Propagation Society International Symposium and National Radio Science Meeting

Red Lion Inn, San Jose, CA (Ray J. King, Lawrence Livermore Nat'l Lab, L-156, P.O. Box 5504, Livermore, CA 94550, 415/423-2369)

27-30 Design of Experiments Workshop Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-29-July 1 SEMICON/Osaka

Intex Center, Osaka, Japan (SEMI, 805 East Middlefield Road, Mountain View, CA 94043, 415/964-5111)

JIJIY 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDA
						1
2	3	4 INDEPENDENCE DAY	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23 30	24 31	25	26	27	28	29

### •9-12 3rd Joint ASCE/ASME Mechanism Conference

San Diego, CA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

-9-14 AEA/Santa Clara University Management Development Program

Santa Clara, CA (Mary Healy, AEA, 5201 Great America Pkwy., Santa Clara, CA 95054, 408/987-4229)

•9-14 Power Engineering Society Summer Meeting
Long Beach, CA (Ed Solorzano, L.A. Dept. of Water & Power, 111 North Hope Street, Room 1236, Los Angeles, CA 90051, 818/352-7864)

•11-12 Manufacturing Excellence Workshop
Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•11-14 PetroExpo

National Auditorium, Mexico City (MIC, P.O. Box 4749, Arlington, VA 22204, 703/685-0600)

16-21 AEA Manufacturing Strategy Program
 Santa Cruz, CA (Stephany Nickel, AEA, 5201 Great America Pkwy., Santa Clara, CA 95054, 408/987-4293)
 17-18 Career Expo
 Melbourne/Orlando, FL (Engineers Expo and Software/Data Processing Career

Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

•23-27 Pressure Vessels and Piping Conference Honolulu, HI (The American Society of Mechanical Engineers, 345 East 47th

Street, New York, NY 10017, 212/705-7785)

•24-25 Career Expo
Columbus, OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

-25-28 Internepcon/Semiconductor Malaysia Kuala Lumpur/Malaysia (Jean D. Skolnik, Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Avenue, Des Plaines, IL 60018, 312/299-9311)

-30-Aug. 2 Computers in Engineering Conference and Exposition, International

Anaheim, CA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•31-Aug. 4 Siggraph '89
Hynes Auditorium, Boston, MA (Chris Herot, Javelin Software Corp., One Kendall Square, Bldg. 200, Cambridge, MA 02139)

# AUGUST 1989



MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDA
	1	2	3	4	5
7	8	9	10	11	12
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### 6-9 National Heat Transfer Conference and Exhibition

Philadelphia, PA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•6-18 AEA/Stanford Executive Institute
Stanford, CA (Mary Horngren Frost, AEA, 5201 Great America Pkwy., Santa Clara, CA 95054, 408/987-4285)

-8 Basic Integrated Circuit Technology Seminar SunBurst Resort, Scottsdale, AZ (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•9 Mid-Term 1989 Seminar

SunBurst Resort, Scottsdale, AZ (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-15 Basic Integrated Circuit Technology Seminar

Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale,

AZ 85260, 602/998-9780)

•16 Mid-Term 1989 Seminar Hilton, Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•22 Basic Integrated Circuit Technology Seminar
Red Lion Inn, Costa Mesa, CA (Patricia Fruscello, ICE, 15022 N. 75th Street,
Scottsdale, AZ 85260, 602/998-9780)

-22-23 Manufacturing Excellence Workshop

Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-23 Mid-Term 1989 Seminar

Red Lion Inn, Costa Mesa, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•26-28 Buscon East

World Trade Center, Boston, MA (CMC, 200 Connecticut Avenue, Norwalk, CT 06856, 203/852-0500, x232)
 Basic Integrated Circuit Technology Seminar
 Omni Parker House, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, 127 07802, 202020 (2720)

Omni Parker House, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•28-29 Career Expo

Cincinnati, OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

•28-31 Surface Mount '89

San Jose Convention Center, San Jose, CA (Lisa Palange, MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, (617) 232-3976)

•29 Mid-Term 1989 Seminar

Omni Parker House, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

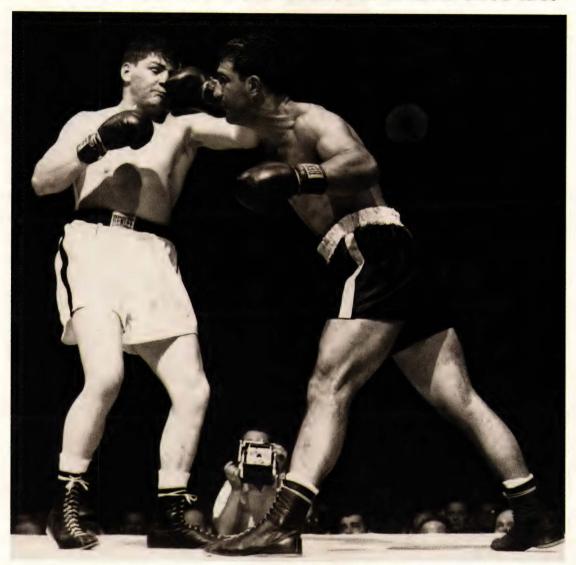
•29-31 International Test Conference

Washington, D.C. (Amy Gold, Advantest America, Inc., Parker Plaza, 400 Kelby Street, Fort Lee, NJ 07024, 201/886-0300)

•30-Sept. 2 Internepcon/Semiconductor Hong Kong

Hong Kong (Jean D. Skolnik, Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Avenue, Des Plaines, IL 60018, 312/299-9311)

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# ZENITH'S STANDARD SWITCHING POWER SUPPLIES—A DEVASTATING 1-2 PUNCH OF SUPERB FEATURES AT A COMPETITIVE PRICE.



It took an industry heavy-weight like Zenith to put it all together. The kinds of options and features you'd have to pay extra for with other manufacturers. Combined with competitive pricing. And even a smaller footprint, so you save on space, too.

It all adds up to a full family of technically superior standard switching power supplies. And a value you'll find hard to match. Because we've outclassed the other contenders in every round:

- CERTIFIED. The Zenith series meets international safety requirements of UL 478; CSA 22.2, No. 154; IEC 380; VDE 0806; VDE 0871/B; FCC PART J, CLASS B.
- FLEXIBLE. All outputs are independently isolated, mag amp regulated, and adjustable. Outputs 2 and 3 can be widely adjusted between 10 and 15V. to meet different equipment demands—at no extra cost!

- TOUGH. Exceeds 100,000 MTBF for durable performance.
- RELIABLE. Comes with 2-year limited warranty, backed by Zenith.

Output & Voltage Current Ratings

Model	Max	Main Output		2nd Output		3rd Output		4th Output		
	Output Power (Watts)	Volts DC (Min/Max)	Amps (Min/Max)	Volts DC (Min/Max)	Amps (Min/Max)	Volts DC (Min/Max)	Amps (Min/Max)	Volts DC (Min/Max)	Amps (Min/Max)	Size (inches)
ZPS-250-N	250	4.75/5.25	3.5/35.0	10.0/15.5	0.4/4.0 PK6	10.0/15.5	0.4/4.0 PK6	4.75/5.25	0.3/3.0	5.0 x 2.5 x 13
ZPS-300-N	300	4.75/5.25	4.5/45.0	10.0/15.5	0.8/8.0 PK12	10.0/15.5	0.8/8.0 PK12	4.75/5.25	0.4/4.0	5.0 x 2.5 x 13
ZPS-400-N	400	4.75/5.25	5.5/55.0	10.0/15.5	1.0/10.0 PK15	10.0/15.5	1.0/10.0 PK15	4.75/5.25	0.6/6.0	6.0 x 2.5 x 13

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# SEPTEMBER 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1	2
3	4  LABOR DAY	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30 ROSH HASH- ANAH

### 5-7 GUADALAJARA ComExpo

Exhibition Center, Guadalajara (MIC, P.O. Box 4749, Arlington, VA 22204, 703/685-0600)

•6-7 The Federal Microcomputer Conference and Exposition Convention Center, Washington, DC (Linda Fitzgibbon, National Trade Productions, Inc., 2111 Eisenhower Avenue, Suite 400, Alexandria, VA 22314, 703/683-8500)

•7-9 Internepcon Osaka

Osaka/Japan (Jean D. Skolnik, Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Avenue, Des Plaines, IL 60018, 312/299-9311)

-11-12 Career Expo

Long Island, NY (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)
-11-13 PCIC '89 - 1989 Petroleum & Chemical Industry Conference
Del Coronado Hotel, San Diego, CA (R. M. Jackson, Union Oil Company of CA, P.O. Box 7600, Los Angeles, CA 90051, 213/997-6417)

•12-14 Midcon '89
O'Hare Exposition Center, Rosemont, IL (Alexes Razevich, Electronic

O Haire Exposition Center, Hosemont, II. (Alexes Hazevich, Electronic Convention Mgmt., 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)

•12-14 NetWorld 89 Dallas (4th Annual)
Infomart, Dallas, TX (Annie T. Zdinak, H. A. Bruno, Inc., 385 Sylvan Avenue, Englewood Cliffs, NJ 07632, 201/569-8542)

-12-14 Semicon/East

Hynes Convention Center, Boston, MA (SEMI, 805 East Middlefield Road, Mountain View, CA 94043, 415/964-5111)

•12-14 Statistical Process Control Workshop

Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ

Sunnyale, On (Fatrica Fluscello, IoE, 1962 11. 7517 518-518, 5250, 602/998-9780)

•16-17 1989 39th Annual Broadcast Symposium

Washington Hotel, Washington, DC (Steve Crowley, A. D. Ring & Associates, 1140 19th Street, N.W., Suite 500, Washington, DC 20036, 202/223-6700)

•17-20 Mechanisms Conference

Montreal, Canada (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

47th Street, New York, NY 10017, 212/05/1703/ 17-20 Vibrations Conference

Montreal, Canada (The American Society of Mechanical Engineers, 345 East
47th Street, New York, NY 10017, 212/705-7785)

-18-20 1989 35th IEEE Holm Conference on Electrical Contacts

Chicago Marriott Downtown, Chicago, IL (Registrar, IEEE Headquarters, 345 East 47th Street, New York, NY 10017, 212/705-7405)

•18-21 OCEANS '89

Seattle Sheraton Hotel & Tower, Washington State Convention & Trade Center, Seattle, WA (Ken W. Mohn, Honeywell Inc., Marine Systems Division, 6500 Harbour Heights Pkwy., Everett, WA 98204, 206/356-3000)

19-21 Assembly Technology Expo

O'Hare Expo Center, Rosemont, IL (PEMCO, 2400 East Devon Avenue, Suite 205, Des Plaines, IL 60018, 312/299-3131)

•19-21 Automated Manufacturing Expo O'Hare Expo Center, Rosemont, IL (PEMCO, 2400 East Devon Avenue, Suite 205. Des Plaines. IL 60018, 312/299-3131)

 19-21 Fall National Design Engineering Conference and Show New York, NY (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

19-22 AEA Executive Forum for Senior HR Professionals Monterey, CA (Diane McIntyre, AEA, 5201, Great America Pkwy., Santa Clara, CA 95054, 408/987-4227)

•20-21 1989 California Electronics Show Pasadena Center, Pasadena, CA (Harry Schwartz, Epic Enterprises, Show Management, 3838 Camino Del Rio North, Suite 164, San Diego, CA 92108, 619/284-9268)

-20-24 ELENEX TURKEY 89

Istanbul Hilton Convention & Exhibition Centre, Istanbul, Turkey (Gerald G. Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450, 201/652-7070)

-25-26 Career Expo

Detroit, MI (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)
•25-28 AUTOTESTCON '89

Adams Mark Hotel, Philadelphia, PA (Fred Liguori, 38 Clubhouse Road, Brown Mills, NJ 08015, 201/323-2842)

-25-28 Buscon East World Trade Center, Boston, MA (CMC, 200 Connecticut Avenue, Norwalk, CT •26 Semiconductor Packaging
Holiday Inn, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

27 Live Videoconferences Via Satellite Network - Neural Networks (Jeff Mathuran, Videoconference Services, The Learning Channel, 1525 Wilson Boulevard, Suite 550, Rosslyn, VA 22209, 800/346-0032)

•27-29 Practical Integrated Circuit Fabrication Seminar

Holiday Inn, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-30-Oct. 4 1989 International Conference on Computer Design Rye Town Hilton, Rye Brook, NY (ICCD 1989, 1730 Massachusetts Ave., NW, Washington, DC 20036, 202/371-0101)

# End the connector compromise...

- 1. CONTACT WIPE ELIMINATES INTERMITTANCE
- 2. 80-700 CONTACTS WITH LOW INSERTION FORCE
- 3. JACK-SCREW ECONOMY AND RELIABILITY





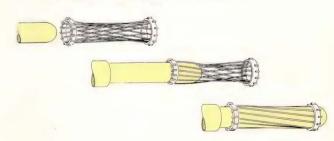
Only Hypertronics ends the compromise in multipin connectors—for heavy-duty power/signal applications—by replacing low wipe Zero Insertion Force (ZIF) contacts and expensive cams with lowforce, high-cycle reliability.

Our N Series housing design accommodates 80 to 700 removable contacts, in a variety of types and terminations. And the wipe action of each Hypertac contact maintains electrical continuity under corrosive conditions and extremes of shock and vibration...ending the intermittance problems of ZIF contacts.

This design provides Low Insertion Force (LIF)—less than 45 pounds for a 700 contact connector—that eliminates the need for cams. A simple jack screw affords a more reliable and economical closure.

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CIRCLE NO 60

# OCTOBER 1989



SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDA
1	2	3	4	5	6	7
8	9 YOM KIPPUR COLUMBUS DAY	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
	29	30	31			
			HALLOWEEN			

-1-4 MEXICON IEEE of Mexico (MIC, P.O. Box 4749, Arlington, VA 22204, 703/685-0600) -1-5 1989 Industry Applications Society Annual Meeting Hotel del Coronado, San Diego, CA (Ronald Jackson, Union Oil Co. of California, P.O. Box 7600, Los Angeles, CA 90051, 213/977-6417)

-1-6 Object Oriented Programming Systems, Languages &

Hyatt New Orleans, New Orleans, LA (George Bosworth, Digitalk, 9841 Airport Blvd., Los Angeles, CA 90045)

+2-5 Electronic Imaging Conference East
Hynes Convention Center, Boston, MA (Lisa Palange, MG Expositions Group,

1050 Commonwealth Avenue, Boston, MA 02215, 617/232-3976)

-3-4 Failure Analysis/Avoidance of Integrated Circuits Seminar Embassy Suites, Scottsdale, AZ (Patricia Fruscello, ICE, 15022 N. 75th Street,

Scottsdale, AZ 85260, 602/998-9780)

-3-5 4th Annual PC Expo in Chicago

McCormick Place North, Chicago, IL (Annie T. Zdinak, H. A. Bruno, Inc., 385

Sylvan Avenue, Englewood Cliffs, NJ 07632, 201/569-8542)

-4-6 1989 IEEE Ultrasonics Symposium Le Grand Hotel, Montreal, Quebec, Canada (Herman van de Vaart, Allied-Signal, Inc., P.O. Box 1021R, Morristown, NJ 07960, 201/455-2482)

University of Missouri-Rolla, Rolla, MO (E. F. Richards, University of Missouri-Rolla, Rolla, MO (5401)

-13-15 RAINBOWfest

New Jersey (Ira D. Barsky, Development Coordinator, Falsoft, Inc., 9509 U.S. Highway 42, Prospect, KY 40059, 502/228-4492)

-15-17 Internal Combustion Engine Technical Conference
Dearborn, MI (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)
•15-18 Industrial Power Conference

Hartford, CT (The American Society of Mechanical Engineers, 345 East 47th

Street, New York, NY 10017, 212/705-7785)

•15-20 AEA Manufacturing Strategy Program

Boston, MA (Stephany Nickel, AEA, 5201 Great America Pkwy., Santa Clara, CA 95054, 408/987-4293)

•16-19 Tribology Conference, Joint ASME/ASLE
Ft. Lauderdale, FL (The American Society of Mechanical Engineers, 345 East
47th Street, New York, NY 10017, 212/705-7785)

•17-19 Northcon/89

Portland Memorial Coliseum, Portland, OR (Alexes Razevich, Electronic Convention Mgmt., 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)

•17-20 Design of Experiments Workshop
Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

17-20 Supercomputing World

Civic Auditorium, San Francisco, CA (Lisa Palange, MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-3976)

-18-19 SEMICON/Southwest

Infomart, Dallas, TX (SEMI, 805 East Middlefield Road, Mountain View, CA 94043, 415/964-5111)

•18-20 International Professional Communication Conference Garden City Hotel, Long Island, NY (Richard Robinson, General Chairman, Grumman Corp., Mail Station C39-05, Bethpage, NY 11714, 516/575-5472) 21-28 Personal Publishing

McCormick Place, Chicago, IL (PEMCO, 2400 East Devon Avenue, Suite 205, Des Plaines, IL 60018, 312/299-3131)

•22-25 1989 IEEE GaAs Integrated Circuits Symposium Sheraton Harbor Island Hotels, San Diego, CA (Kenneth J. Sleger, Naval Research Laboratory, Code 6852, Washington, DC 20394, 202/767-3894)

-22-26 Joint Power Generation Conference

Hyatt Regency Hotel, Dallas, TX (Marisa Scalice, ASME, 345 E. 47th Street, New York, NY 10017, 212/705-7053)

•23-24 Career Expo
Dayton, OH (Engineers Expo and Software/Data Processing Career Fair,
Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

23-28 International Waste Management

Kyoto, Japan (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

·26 Live Videoconferences Via Satellite Network - RISC

(Jeff Mathuran, Videoconference Services, The Learning Channel, 1525 Wilson Boulevard, Suite 550, Rosslyn, VA 22209, 800/346-0032)

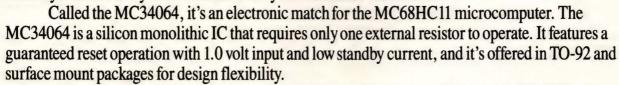
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# NOVEMBER 1989

EDIN
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SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
			1	2	3	4
5	6	7 ELECTION DAY	8	9	10	11  VET- ERANS DAY
12	13	14	15	16	17	18
19	20	21	22	23 THANKSGIVING DAY	24	26
26	27	28	29	30		

Huntsville, AL (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

•7-11 Productronica '89

Munich Trade Fair Centre, Munich, West Germany (Gerald G. Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450, 201/652-7070)

-9-10 Training Workshop for Visual Inspection of ICs and Hybrids Holiday Inn, Boston, MA (Patricia Fruscello, ICE, 15022 N. 75th Street,

Scottsdale, AZ 85260, 602/998-9780)

-9-16 1989 International Test Conference
Sheraton Washington, Washington, DC (Doris Thomas, ITC, P.O. Box 264, Mt. Freedom, NJ 07970, 201/895-5260)

-13-14 Career Expo
Dayton, OH (Engineers Expo and Software/Data Processing Career Fair,
Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

•13-17 Comdex Fall
Las Vegas Convention Center, Las Vegas, NV (Interface, 300 First Avenue, Needham, MA 02194, 617/449-6600)

•14-16 Nepcon Southeast '89

Orange County Convention Center, Orlando, FL (Janet Schafer, Cahners Exposition Group, 1350, E. Touhy Ave., Des Plaines, IL 60018, 312/299-9311) -14-16 Wescon/89

Moscone Convention Center, Brooks Hall and Civic Auditorium, San Francisco, CA (Alexes Razevich, Electronic Conventions Mgmt., 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)

Angeles, CA 90045, 213/7/2-2955)

27-30 1989 Global Telecommunications Conference
Loew's Anatole Hotel, Dallas, TX (Harold Sobel, Rockwell International Corp.,
P.O. Box 10462, Dallas, TX 75207, 214/996-5881)

28-Dec. 1 1989 Conference on Magnetism and Magnetic Materials

Sheraton Boston, Boston, MA (Courtesy Associates, Inc., 655 15th Street NW, Suite 300, Washington, DC 20005, 202/639-5088)

-29 Live Videoconferences Via Satellite Network - Machine Vision

(Jeff Mathuran, Videoconference Services, The Learning Channel, 1525 Wilson Boulevard, Suite 550, Rosslyn, VA 22209, 800/346-0032)

•29-Dec. 1 SEMICON/Korea

Korea Exhibition Center, Seoul, Korea (SEMI, 805 East Middlefield Road,

Mountain View, CA 94043, 415/964-5111)

# DECEMBER 1989

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDA
					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24 31	25 CHRISTMAS	26	27	28	29	30

-3-6 1989 IEEE International Electron Devices Meeting Washington Hilton, Washington, DC (Melissa Widekehr, c/o Courtesy Associates, Inc., 655 15th Street NW, Suite 3000, Washington, DC 20005,

Associates, Inc., 655 15th Street NW, Suite 3000, Washington, DC 20005, 202/347-5900)

4-5 Career Expo
Dayton, OH (Engineers Expo and Software/Data Processing Career Fair, Divisions RSI Group, 2367 Auburn Ave., Cincinnati, OH 45219, 513/721-3030)

10-15 Winter Annual Meeting - The American Society of Mechanical Engineers
San Francisco, CA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

12-13 Manufacturing Excellence Workshop
Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

Sunnyvale, CA (Patricia Fruscello, ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•12-14 Winter National Design Engineering Conference Show Anaheim, CA (The American Society of Mechanical Engineers, 345 East 47th Street, New York, NY 10017, 212/705-7785)

•13-15 1989 289th IEEE Conference on Decision & Control Hyatt Regency-Tampa, Tampa, FL (Prof. Leonard Shaw, Department of Electrical Engineering and Computer Science, Polytechnic University, 333 Jay Street, Brooklyn, NY 11201, 718/260-3802)

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#### **NEW PRODUCTS**

#### TEST & MEASUREMENT INSTRUMENTS

#### DSO SPEED BOOSTER

- Increases effective sample rate to 2G samples/sec
- Doubles display memory to 16k samples

The HP 54114A test set connects to the front of the vendor's 54111D scope; it doubles the scope's effective sampling rate to 2G samples/ sec-a value that the vendor believes is the highest available in general-purpose DSOs that use random equivalent-time sampling. (Scopes shipped before the introduction of the 54114A require you to install an upgrade to use the test set.) The test set works by allowing the scope's two channels to sample a single waveform; it positions each channel's samples midway between the other channel's. In the process. it allows the use of the second chan-



nel's waveform memory to augment that provided for the first channel's data and thus doubles the number of samples of a single waveform that the scope can store. \$1625; \$2625 for older 54111Ds.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No 660



conform to such standards as ESDI and SCSI. \$15,000; upgrade of model TIA 2001 to 2001A, \$1195.

Odetics Inc Kode Div, 1515 S Manchester Ave, Anaheim, CA 92802. Phone (714) 758-0400. TLX 3716642.

Circle No 661

#### INTERVAL ANALYZER

- Performs 800k measurements/sec
- Resolves time intervals to 1 nsec The TIA 2001A performs a series of time-interval measurements, logs how often each interval value has occurred, and displays the results as a histogram. It can also compute such statistical measures as mean and standard deviation. The instrument can make as many as 800k measurements/sec and can resolve interval durations to 1 nsec. Its primary uses are in analysis of serialdata quality, for example, in measuring the bit shift, margin error, and rate performance of disk drives. Its triggering capabilities enable it to handle data at rates to 10M bps and suit it to use with drives that

#### 100M-SAMPLE/SEC DSO

- Achieves analog bandwidth of 350 MHz
- Stores 50k samples in nonvolatile memory

The 9420 2-channel digital-storage oscilloscope makes 100M samples/sec—1/4th the rate of the vendor's recently introduced 9450—so it is less expensive. Nonetheless, both scopes have the same 350-MHz analog bandwidth and 50k-sampledeep, battery-backed waveform memory. The reduced sample rate of the 9420 forces it to revert to equivalent-time sampling (ETS) at some fast sweep speeds where the 9450 can sample in real time; hence, the 9420 cannot capture single-shot



transients as short as those acquired by the 9450. In ETS mode, however, both scopes sample at a maximum effective rate of 10G samples/sec; therefore, their 350-MHz analog bandwidth becomes the limiting factor. Furthermore, at any sweep speed, the 9420 can detect glitches as brief as 2.5 nsec. The analog-scope "feel" of the 9420 is identical to that of the 9450, as are the triggering and automatic pulse parameter measurement modes. \$14,900. Delivery, six to eight weeks ARO.

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 425-2000. TWX 710-577-2832.

Circle No 662

#### TEST & MEASUREMENT INSTRUMENTS



#### DEFECT ANALYZER

- Performs as stand-alone tester for simple pc boards
- Screens complex boards to minimize test time

The Midata 520 manufacturingdefects analyzer screens pc boards for problems such as open circuits, solder-flow and copper-etch defects, incorrectly loaded components, and damaged components. The system addresses as many as 4096 circuit nodes, each of which is actively guarded; it performs componentlevel tests on resistors, capacitors, inductors, diodes, and transistors. It also detects whether ICs have been loaded and determines if IC orientation is correct. The system can log fault information on a highspeed ticket printer or write it to a fault database. A high-speed switching matrix allows the unit to test a board in 1 to 5 sec, rather than the 20 to 30 sec required by other testers. From \$55,000. Delivery, 90 days ARO.

Marconi Instruments Inc, 3 Pearl Ct, Allendale, NJ 07401. Phone (201) 934-9050.

Circle No 663

#### 80386 DISASSEMBLER

- Is on a pc board that plugs into logic analyzer
- Lets you plug μP into personality adapter

The PM 8858/80 is a pc board that plugs into the vendors' PM 3570 logic analyzer. ROMs on the board contain two disassemblers for Intel Corp's 80386 32-bit  $\mu$ P. For easy connection to the 80386's pin-gridarray package, the vendor also of-

fers the PM 8817/41 personality module. You plug the µP into the personality module, plug the personality module into the target system, and also connect the personality module to the logic analyzer. One disassembler displays all 80386 instructions (including virtual protected-mode instructions) on a single line along with the corresponding mnemonics and addresses. You can select 16- or 32-bit operation of the µP in virtual protected mode. The second disassembler displays code bytes. Disassembler board and personality module, \$500 each.

John Fluke Mfg Co Inc, Box C-9090, Everett, WA 98206. Phone (800) 443-5853, ext 77. TLX 185102.

Circle No 664

Philips Test and Measurement, Building HKF, 5600 MD Eindoven, The Netherlands. Phone local sales office.

Circle No 665



#### ASIC VERIFIER

- Holds cost down by sharing resources
- Locates all pin electronics on one board in test head

The LV 500 ASIC-verification system can fit on a benchtop and holds down its purchase price by using a shared-resource architecture. Yet, according to the vendor, it achieves flexibility in generating and dynamically modifying timing sets that was available heretofore only in much larger and more expensive systems intended for high-volume testing. Virtually all of the system's pin-related circuits are on a single pc board in the test head. The sys-

tem can accommodate 64 to 256 channels with 64k words of pattern memory. It operates at speeds to 50 MHz with 500-psec timing resolution and provides 16 clock phases. It permits you to select drive and comparison levels and to separately control the timing, data format, and function of each pin. The software offers you many ways to present acquired data, including schmoo plots. \$55,000 to \$172,000.

**Tektronix Inc,** Box 12132, Portland, OR 97212. Phone (800) 245-2036.

Circle No 666



#### ASIC VERIFIER

- Stores 463k vectors
- Dynamically alters I/O direction, masking, and inhibiting

The Topaz-V<sub>L</sub> ASIC-verification system handles devices with 32 to 256 pins and with propagation delays of 500 psec or more. In a 32-pin configuration, the system can store 463k vectors. You can upgrade the system to the performance level of more expensive members of the product family. This system has a 50-MHz max test rate and a 1-nsec pin-to-pin timing skew, but like its higher performance brethren, it uses resource-per-pin architecture that provides dynamic control of I/O direction, data format, masking, and device-output inhibit functions. The system permits you to vary logic levels and the comparison threshold. \$67,000 to \$220,000.

Hilevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (800) 445-3835; in CA, (800) 541-2742. TLX 655316.

Circle No 667



### THE SIMPSON 560 MENU DRIVEN MULTIMETER.

# SOMETHING NEW ON THE MENU.

From microvolt transducer measurements to high voltage work, Simpson's new *Professional Series* Model 560 Digital Multimeter is designed to quickly give the answers you need—without elaborate signal conditioning.

Diagnostic functions such as MIN/MAX Hold and Peak Hold let you find and display transient amplitudes, while the bar graph continues to monitor the incoming signal. Programmable data logging on any range or function and a built-in 500 KHz frequency



counter, further expand the acquisition capabilities of the Simpson 560.

What's more, it's now possible to speed up routine tests—saving only the measurements of interest—because the 560 offers real-

time comparison to stored test limits. Permanent records of the captured data can be generated by computers or printers connected to the optional interfaces (Centronics, RS-232 or IEEE-488). Displayed menus make it quick and easy to set the measurement parameters. And ultra-fast autoranging inputs instantly calculate the proper scale.

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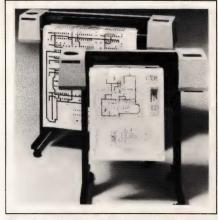
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#### **Intermetrics**

#### INSTRUMENTS



#### DRAFTING PLOTTERS

- Handle drawing sizes to D and E
- Support the HP-GL language

The Draftpro DXL and EXL drafting plotters handle D- and E-size media. Both feature pen acceleration of 2g as well 0.0005-in, resolution and 0.2% accuracy. A pensorting capability reduces plotting time by minimizing the number of pen changes. The units store their pens in an 8-pen carousel; they cap pens not in use to prevent them from drying out. You can use both liquid-ink and fiber-tip pens. The units incorporate an RS-232C interface and, optionally, an IEEE-488 interface. They use HP-GL (Hewlett-Packard Graphics Language); hence, they are compatible with the same software as are the vendor's other pen plotters. Draftpro DXL. \$4995; EXL, \$6495.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 668

#### **IEEE-488 INTERFACE**

- Plugs into MicroVAX 3000's Q Bus
- Performs DMA transfers to 250k bytes/sec

The GPIB-MV3000 kit provides an interface between the Q Bus in Digital Equipment Corp's MicroVAX 3000 series computers and the IEEE-488 bus. The controller board in the kit performs DMA transfers at 250k bytes/sec with a maximum block length of 64k bytes/

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The Model 2040 offers two outputs, each 1 V p-p, in phase opposition to provide both single-ended and differential outputs at a bandwidth of greater than 700 MHz.

The Model 2045 provides one low level output (1 V p-p/50 ohms) at a full 700 MHz bandwidth and another output channel at 5 V p-p/50 ohms, 200 MHz bandwidth and 8 bits resolution over the full dynamic range.

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#### TEST & MEASUREMENT INSTRUMENTS



transfer. The kit includes source code for a multiboard handler compatible with the MicroVAX's VMS operating system. The handler implements more than two dozen functions related to management of the IEEE-488 bus and control of instruments attached to it. The vendor can furnish the software on floppy disk, on tape cartridge, or on 9-track tape. \$2095 to \$2195 depending on software-distribution medium.

National Instruments Corp, 12109 Technology Blvd, Austin TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737.

Circle No 669

#### PATTERN GENERATOR

- Provides 32k×4-bit patterns at 2.5 GHz
- Achieves 150-psec typ rise and fall times

The PG-2500 is a digital pattern generator that produces 32k×4-bit patterns at 2.5 GHz or 16k×8-bit patterns at 1.25 GHz. You can interconnect as many as eight units to obtain wider patterns. In the standard unit, outputs conform to the specs of 100K-series ECL and are series terminated with  $50\Omega$  at the sending end; you must provide a  $50\Omega$  termination at the receiving end of the output cable. As an option, you can obtain outputs that you can program over the range of -2 to +2V, with a 2V p-p max amplitude. You can shift output timing over a range of  $\pm 2$  nsec with 10-psec resolution and 100-psec accuracy. You can load patterns from a host computer via the IEEE-488 bus in several formats. You must

supply an 80286- or 80386-based computer with 640k bytes of RAM, a 10M-byte hard disk, a floppy-disk drive that can read 360k-byte disks, an EGA (enhanced graphics adapter) card, a high-resolution color monitor, and a National Instruments Corp PC 2A IEEE-488 interface card and cable. With fixed output levels, \$60,000; with variable output levels, \$75,000.

Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 408-374-9273.

Circle No 670



#### **IEEE-488 CONTROLLER**

- Sends strings in response to 1-character commands
- Buffers 32k characters

The Micro488A allows you to connect IEEE-488 devices to an RS-232C or RS-422 port that operates as fast as 57.6k bps. The unit can act as a talker or a listener on an IEEE-488 bus as long as 4000 ft that connects as many as 14 devices. To minimize traffic through the relatively slow serial interface. the unit can output stored character strings in response to 1-character commands. You can define as many as 100 of these "macros." The unit, which uses Hewlett-Packard programming syntax, can also buffer 32,000 characters. \$695.

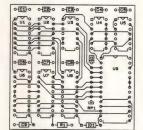
IOTech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. TWX 650-282-0864.

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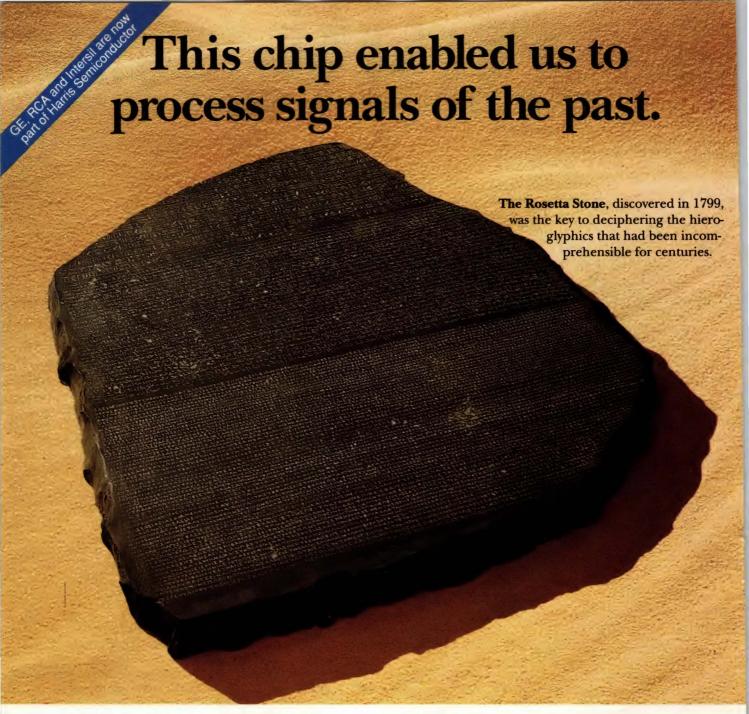
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ISP 9216 16x16 Multiplier: low-power, industry-standard compatible to AM29516 and MPY016.

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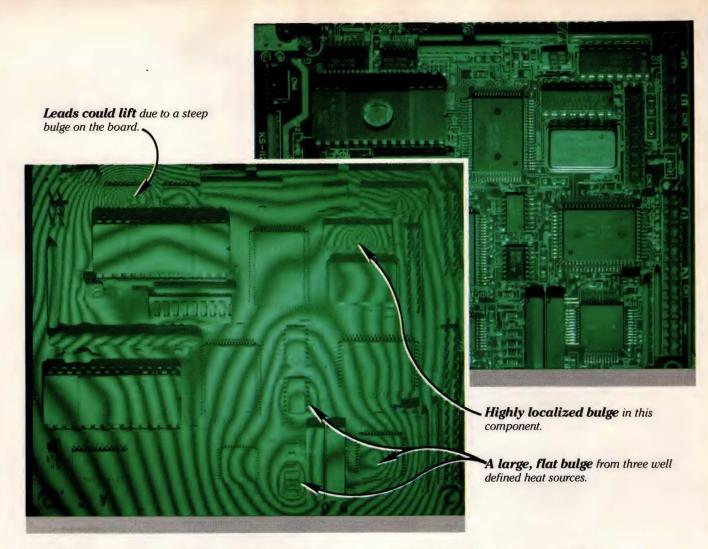
If worries about complexity and cost have deterred you from taking the exciting step into digital signal processing, call us. Together, we'll step into the future.

For more information, call toll-free today, 1-800-4-HARRIS, ext 30.

In Canada: 1-800-344-2444, ext. 30.

In Europe, call: Brussels, (02)246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.





# Thermally induced failures? See them easily with Holographic NDT

#### A powerful solution

In seconds anyone can produce an image of minute deformations and view them as they evolve. Newport's holographic systems provide the power of holographic interferometry, with push button ease.

#### Interpretation is easy

The crisp lines on the PC board form a topographic map of its deformations, with the elevation between successive contour lines being precisely 10 micro inches. Our system allows you to resolve tightly spaced contours even on variable contrast objects like this PC board, so you never miss a detail.

#### Failure identification

Failures are easily understood when you can watch the board or component deform during its power-up cycle. As the board heats up, closely spaced fringes indicate large board or component deformation, which can indicate too much heat, or perhaps excessive stress on the leads of a high reliability component.

#### Easy operation

Operation is simple and easy: the system is completely electronic, and it takes only 10 seconds from exposure to viewing.

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#### **NEW PRODUCTS**

#### CAE & SOFTWARE DEVELOPMENT TOOLS

#### CAD TRANSLATOR

- Converts motion into servo commands
- Permits CAD control of motion systems

The CAD-to-DMC (digital-motion controller) software translates an Autocad or a DXF (Data-Exchange Format) file into servo motion and links IBM PC-based CAD software with a motor controller. You use CAD software to draw the motion that you want to implement, and the translator converts the CAD-DXF file into a set of DMC commands. The commands travel to the controller, which moves the motors along the motion path. You can define motion in the XY plane and use as many as 256 arc and straight line segments to define your path. By specifying continuous motion between segments, you can achieve smooth contouring. Vector speed varies from 2 to 500,000 counts/sec. The software includes the CAD-to-



DMC translator, Autosketch CAD software, and the DMC controller executive. Software, \$1500; controller, \$1495.

Galil Motion Control Inc, 1054 Elwell Court, Palo Alto, CA 94303. Phone (415) 964-6494.

Circle No 420

#### MULTISOURCE ASIC KIT

- Allows vendor-independent ASIC design
- Includes twelve software tools

The Design Kit enables users of IBM PC-based workstations to design an ASIC and compare its performance in alternative gate-array or standard-cell technologies before committing the design to a vendor. Working within the Viewlogic CAE workstation environment, the kit allows you to reimplement a design in an alternate ASIC technology, resimulate, and compare the design's performance and gate utilization. Vendor technology files provide the data that the software tools use to verify a design's performance. The library contains 109 logic and I/O cells. The verification tools generate delay values that match the vendor's mainframe simulation numbers. The Design Kit checks for spikes, setup- and hold-time violations, and release-time and pulse-width errors. To operate the system, you need an IBM PC/AT or compatible with at least 640k bytes of RAM, an IBM CGA or EGA graphics board, and both a serial and a parallel port. The package includes the generic library, twelve software tools, and a choice of two technology files. \$9950. Additional technology files, \$1200.

Custom Silicon Inc, 600 Suffolk St, Lowell, MA 01854. Phone (508) 454-4600. FAX 508-458-4931.

Circle No 421

#### NEURAL SOFTWARE

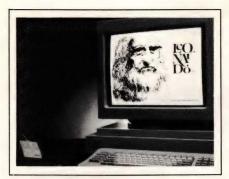
- Tutorial software for neuralcircuit design
- Emulates a small section of the human brain

The Brain Simulator is an MS-DOS program that implements an array of 1200 neurons, using a digital

model of the human brain neuron developed by the Neural Network Laboratory. The CRT represents a network of neurons; when a neuron fires, its CRT location flashes. Using a mouse to indicate a particular neuron, you can display the existing synaptic connections and modify sample networks or define new ones. To establish initial conditions or to emulate the input of a visual image, you can force neurons to fire. The Brain Simulator package includes simple switching, memory, and pattern-recognition-circuitry examples. An accompanying booklet explains the operation of biological neurons and describes how the program emulates biological neurons. \$99.

Abbot, Foster, & Hauserman Co, 44 Montgomery St, Fifth Floor, San Francisco, CA 94104. Phone (800) 562-0025.

Circle No 422



can output directly to PostScript printers. It provides support for SunRaster and encapsulated Post-Script formats; support for IGES is optional. \$1200.

**Qubix Graphic System Inc, 1255** Parkmoor Ave, San Jose, CA 95126. Phone (408) 292-4000. FAX 408-295-7485.

Circle No 423

matics. Lice requires DOS 2.0 or higher with an IBM CGA or equivalent and needs 256k bytes of RAM. It comes with a tutorial manual.

BSoft Software, 444 Colton Rd, Columbus, OH 43207, Phone (614) 491-0832.

Circle No 424

#### GRAPHICS DESIGNER

- Integrates vector and raster graphics with text/table creation
- Runs on Sun-3 workstations

Leonardo software allows you to prepare business forms, presentation materials, and graphics in a variety of formats, using the system's constrained drawing, freehand drawing, and raster editing tools. You can use Leonardo as a standalone tool or as a complement to other software packages. The software comes with the LaserWriter Plus fontload of 35 typefaces and

#### LOGIC SIMULATOR

- Runs on IBM PCs and compa-
- Features tabular logic display of

Lice is a low-cost, menu-driven logic-circuit emulator program. The simulator has three main menu selections: a logic-default editor. which initializes circuits and sets up the tabular output display; a TTLfamily-component dictionary listing; and a logic-circuit entry, which accepts keyboard or diskfile sche-

#### STORAGE SOFTWARE

- Provides data security
- Supports most networks and in-

FileSafe Software 4.5 provides enhanced and full transparent support of all network requirements on Novell, IBM's Token Ring, 3Com, and most other networks. The software provides backup to any drive on the network to a specific station and supports more than 100,000 files per backup. The package fulfills the requirements of the Novell network operating system, includ-

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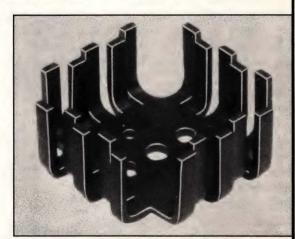
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#### CAE & SOFTWARE DEVELOPMENT TOOLS

ing backing up user rights and trustee lists, the Net\$bind.sys and Net\$bval.sys files, owner ID numbers, file-creation dates, last-access dates, last-modified dates, and all-file attributes. The software provides backup of on-line servers; you don't have to halt the network. File-Safe supports a range of tape drives, including QIC-40, QIC-24, QIC-150, and SCSI-based tape-drive systems. The software utilizes Lotus/Intel/Microsoft expanded-memory specification and virtual disk support. \$99.

Mountain Computer Inc, 240 Hacienda Ave, Campbell, CA 95008. Phone (408) 379-4300. FAX 408-379-4302.

Circle No 425



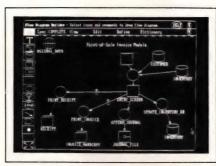
#### GRAPHICS DATABASE

- Includes drawing and picture graphics as a field type
- Allows as many as 200 fields DataSketch is a database system that includes drawing and picture graphics as a field type as well as numeric, character, date, multiline, and sound fields. The built-in art capability allows you to paint solid or cross-hatched figures and create circles, lines, rectangles, dots, text, and arcs. You can rotate, duplicate, move, and zoom sections of a field and then save the data to disk for future recall. DataSketch has an English-like programming language with extensions for graphics fields and variables. For example, you can list all the records that contain circles or add up the lengths of all the lines in a file. You can create and modify drawings interactively

or under program control. Data Sketch can index without converting fields to the same data type. The pc-based database requires a DOS with 512k bytes of RAM and an IBM CGA or EGA, or a Hercules display. \$99.

Tarbell Electronics, 1082 E Artesia Blvd, Suite C, Long Beach, CA 90805. Phone (213) 422-7081.

Circle No 426



#### C-CODE CASE TOOL

- Produces C source code from graphics specification
- Generates code for IBM PC applications

MicroStep is a CASE tool that produces 100% C source code and executable programs directly from graphics specifications. The tool features an interactive graphicsdesign environment, automatic specification analysis, generation of executable code, and production of technical documentation. You can interactively create a system specification using five sets of seamlessly integrated tools to build the data flow diagrams, specify the data structures, layout the screens, format the reports, and describe the applications computations and processing logic. Additionally, you can copy and store elements in the data dictionary for use in other specifications. Currently, MicroStep accepts .DBF and both fixed and delimited ASCII files. It runs on IBM PCs and compatibles running DOS 3.1 through 3.3. \$5000.

SysCorp International, 9420 Research Blvd, Suite 200, Austin, TX 78759. Phone (512) 338-0591.

Circle No 427

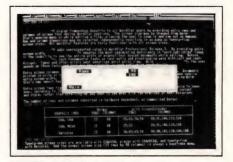
#### PC-BASED PCB CAD

- Offers 1-mil resolution
- Can place and route 16 signal layers

Cadstar 4 is a moderately priced tool in the vendor's trio of pc-board design packages. Cadstar 4 accommodates complex boards with surface-mount devices on both sides of the board and handles multiple power and ground planes. It provides autoplacement routines that let you interactively optimize connections during component movement for higher density and shorter track lengths. The software can handle as many as 1023 components and 3500 connections per design. Cadstar 4 runs on IBM PC/ATs and compatibles as well as on 80386based systems. \$4850.

**Racal-Redac Inc,** Box 365, Westford, MA 01886. Phone (508) 692-4900.

Circle No 428



#### SCREEN MANAGER

- Works with WordStar Professional Releases 4 and 5
- As many as 25 screen sizes available

ScreenExtender is a screen manager for WordStar that provides more than 25 rows and 80 columns of screen text. From WordStar's opening menu or while editing a file, you can change the number of screen rows and columns and zoom in and pan out on demand. Screen-Extender lets you see the entire width of a proportionally spaced document while editing; previously, you had to use horizontal scrolls to see the "hidden" portion of proportionally spaced documents. You can

#### CAE & SOFTWARE DEVELOPMENT TOOLS

increase the viewing area to as many as 58 rows, which is a whole screen. The number of screen sizes that ScreenExtender will support depends on the graphics standard you employ. However, an IBM EGA/VGA has 21 sizes, an IBM CGA/MCGA has 11 sizes, and a Hercules display has 25 screen sizes; all have 25 rows and 80 columns as their default. ScreenExtender features screen colors, normal or reverse video, and hot-key definitions. It also lets you save your option choices so you can begin a session with your defaults. \$59.95.

Stairway Software Inc, 700 Harris St, Suite 204, Charlottesville, VA 22901. Phone (804) 977-7770.

Circle No 429



#### TOUCHSCREEN SYSTEMS

- For the vendor's 1030 and 1050 series Touch Control Screens
- Run on IBM PC/XTs, PC/ATs, or compatibles

ScreenBuilder and IconBuilder software packages simplify programming of display screens for custom applications. ScreenBuilder, a screen development tool, allows you to develop application screens. To position a touchkey or to specify its visual and feedback characteristics, you fill in the blanks on the ScreenBuilder's questionnaire. IconBuilder allows you to create custom characters to display common symbols, circles, and static

graphics on an IBM PC for downloading into one of the Touch Control Screen's programmable 128character sets. Both packages eliminate high-level programming. \$95.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 453-5853.

Circle No 430

Philips Test and Measurement, Building HKF, 5600 MD Eindhoven, The Netherlands. Phone local office.

Circle No 431

#### **EDITOR BUILDER**

- Lets you create drawing editors
- Runs on Apollo, Sun, DEC, HP, and other workstations

The Editor Construction Kit lets you build tailored editors with graphical object-manipulation capability. The kit provides a graphical interface, which allows you to interactively create objects and define their control points. In addition, it gives you control over the interactive appearance of the editor and the ability to extend and constrain editing activities. The Editor Contruction Kit permits you to write less code to set up the editing session and spend more time perfecting the interface. \$4000.

VI Corp, Amherst Research Park, Amherst, MA 01002. Phone (413) 253-3482.

Circle No 432

#### CASE TOOL

- Allows you to structure your own CASE environment
- Interfaces and integrates other tools

Sylva Foundry MS/DOS is an IBM PC-based workbench that contains tools for creating and modifying techniques, interfacing open architecture with other tools, and generating diagrams from external data. Once you create modeling objects, you can store them in technique-specific Icon Drums for use in creating system models. A diagram editor provides a rule-based drawing

capability through an intuitive interface. The Foundry Diagram Generator lets you generate diagrams from external data, and the Foundry Screen Maker lets you create active menus and panel-to-panel relations, and control other screen functions. An optional Starter Kit enables you to modify or blend De-Marco Data Flow, Gane and Sarson Data Flow, Ward-Mellor Control Flow, Entity Relationship, State Transition, Constantine Structure, and three other techniques. \$8500. Starter Kit, \$3000.

Cadware, 869 Whalley Ave, New Haven, CT 06515. Phone (800) 223-9273; in CT, (203) 397-2908.

Circle No 433

#### C DEVELOPMENT KIT

- Facilitates C code generation for parallel and embedded applications
- Supports features specific to the Transputer

The Transputer Toolset provides a complete C and assembly language development environment for the INMOS Transputer family. The toolset works with a single Transputer or in a Transputer network. The toolset offers optimization facilities and close conformance to the emerging ANSI C standard. The Transputer Toolset includes a C compiler, an assembler, a linker, a librarian, and both a single processor and a network loader. The compiler supports in-line assembly language and can generate in-line code for the C functions, which map into the Transputer instruction set. The compiler can generate code for the 64-bit/32-bit ANSI floatingpoint model, or the 32-bit only floating-point model. The toolset is portable across MS-DOS, Apple Mac II, and SYS5/BSD4.3 Unix systems, including Apollo, Sun, and DEC. \$995.

Logical Systems, Box 1702, Corvallis, OR 97339. Phone (503) 753-9051.

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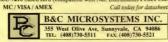
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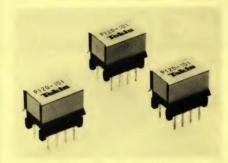
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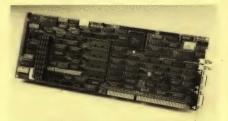


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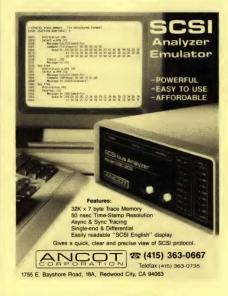
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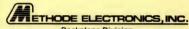
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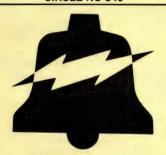
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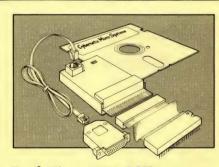
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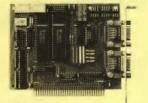
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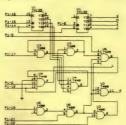
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## Guide helps you select electronic tools

The 32-pg buyer's guide entitled Gain control of your soldering operation! lists electronic tools, test equipment, and supplies used for manufacturing, assembling, and repairing electronic equipment. The publication describes and illustrates test instruments. soldering/ desoldering systems, tool kits, lamps and magnifiers, antistatic products, and precision hand tools. Comparison charts and color-coded specification charts complete the catalog.

**HMC**, Box 526, Canton, MA 02021.

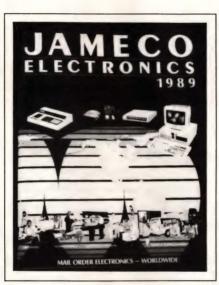
Circle No 650

## Directory of electronic measuring devices

The company's 1988/89 Electronic Measuring Instruments catalog provides a comprehensive listing of 14 instrument categories, including oscilloscopes, logic analyzers, signal generators, modulators, wow and flutter meters, analog and digital voltmeters, and frequency counters/timers. The 213-pg catalog introduces the VP-5516A, a 100-MHz, 4-channel, 10-trace analog oscilloscope featuring a 3-D video display for analyzing complicated waveforms; and the VP-5741A, a DSO featuring a 100-MHz sampling clock and three 10,000-word memories for high-speed transient signals. Divided into product categories that contain general product descriptions, the publication lists specifications and cross references. Diagrams illustrate specific functions.

Panasonic Industrial Co, 50 Meadowlands Parkway, Secaucus, NJ 07094.

Circle No 651



# Broad range of computer kits, peripherals, and ICs

The vendor's 1989 catalog presents a wide variety of electronic products, from computer kits and IBM PC/XT-, PC/AT-, and Apple-compatible peripherals to ICs. It introduces several new products, including AMI 80386, 16- and 20-MHz mother boards and the New Enhanced AT (NEAT) mother board. The 76-pg, 4-color publication also features a 2-pg insert of useful TTL and  $\mu P$  pin-out data.

Jameco Electronics, 1355 Shoreway Rd, Belmont, CA 94002.

Circle No 652

## Direct purchase service for test instruments

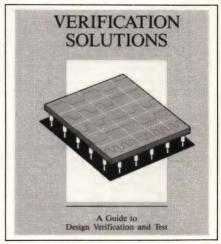
The Tek Direct Catalog for Instruments, Accessories, and Services is a quarterly, 4-color publication. Describing a sampling of test-instrument products, this catalog tells you how to make direct purchases



of the vendor's highest volume products. Products highlighted in the latest edition are the vendor's 200 and 2200 Series portable oscilloscopes, the 1205 logic analyzer, accessories, software, and training aids.

Tektronix Inc, Box 500, Beaverton, OR 97077.

Circle No 653



## Using a prototype hardware verification of ASICs

The 118-pg book, Verification Solutions: A Guide to Design Verification and Test, helps you with IC design and test, as well as prototype hardware verification of ASICs and semiconductor parts. The paperback book explains how prototype verification bridges the steps between computer-aided de-

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UPT311 - UPT315	SFT6800	TO - 5	400	3.0	5.0	25
2N3418 - 2N3421	SPT5333	TO - 5	120	5.0	15	70
2N3996 - 2N3997	2N3996 - 2N3997	TO - 111	80	5.0	40	80
2N6676 - 2N6678	2N6676 - 2N6678	TO - 3	400	15	175	50
2N5038 - 2N5039	SFT5671 - SFT5672	TO - 3	140	30	150	50
UBT430	SFT430	TO - 3	120	15	150	30
U2T301 (Darlington)	SFD5390	TO - 5	80	5.0	15	40
	PNP Bi-Polar Switch					
Unitrode Part Number	SSDI Replacement	Case Style		I <sub>C</sub> AVG. (A)	PD (W)	fT (MH
NONE	SSDI has a full line of I to our NPN transistors		stors th	at are co	mplimenta	ary
	Silicon Controll	ed Recti	fiers			
Unitrode Part Number	SSDI Replacement	Case Style	VDRM	I <sub>T</sub> AVG. (A)	PD (W)	tgt (ns
GA200,A - GA201,A	2N3027 - 2N3032	TO - 18	100V	0.4	0.6	20
2N3027 - 2N3032	2N3027 - 2N3032	TO - 18	100V	0.5	0.6	100
AA100 - AA118	2N3027 - 2N3032	TO - 18	400V	0.5	0.6	100
ID100 - ID106	2N3027 - 2N3032	TO - 18	400V	0.5	1.2	100
2N2323 - 2N2329	SPT2323 - SPT2329	TO-5	500V	1.5	3.5	400
2N5724 - 2N5728	2N5724 - 2N5728	TO-5	400V	1.6	2.5	400
AD100 - AD118	SPT2323 - SPT2329	TO-5	400V	1.6	2.5	1μs
ID200 - ID203	SPT2323 - SPT2329	TO-5	200V	1.6	2.5	1μS
ID300 - ID301	SPT2323 - SPT2329	TO-5	400V	1.6	2.5	1μS
GB200,A - GB201,A	SPT200A - SPT201A	TO - 59	100V	6.0	25	100
GB300,A - GB301,A	SPT300A - SPT301A	TO - 59	100V	6.0	25	100
NONE	STX2381	TO-3	600V	50	75	400
GA300,A - GA301,A	2N3027 - 2N3032	TO - 18	100V	100 Peak	0.6	20
	Ultrafast Centert	ap Recti	fiers			
Unitrode Part Number	SSDI Replacement	Case Style	BVR (V)	I <sub>O</sub> (A)	RθJC (W/°C)	t <sub>rr</sub> (ns
SCHOTTKY						
USD245	SPD245	TO-5	45	4	12	3.0
SD241	SPD241	TO-3	45	30	1.4	3.0
USD320C	SPD320C	TO-3	20	60	1.4	3.0
USD335C	SPD325C	TO-3	35	60	1.4	3.0
USD345C	SPD345C	TO-3	45	60	1.4	3.0
PLANAR	3503430	10-3	45	00	1.4	3.0
UES2601 - UES2603	SHA2604	TO-3	200	30	1.0	35
UES2604 - UES2606	SHA2604 - SHA2607	TO-3	500	30	1.0	35
SES5601C - SES5603C	SHA2604 - SHA2607	TO-3	500	30	1.0	35
	PIN Radiation De					
Unitrode Part Number	SSDI Replacement	Case Style	BVR (V)	I <sub>p</sub> (mA)	CJ (pf)	t <sub>rr</sub> (ns
UM9441	SPD1511-1	TO - 18	90	50	10 - 17	250
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sign and production test. It illustrates each step in the hardware verification process with examples of specific tasks and solutions.

IMS, 9400 SW Gemini Dr, Beaverton, OR 97005.

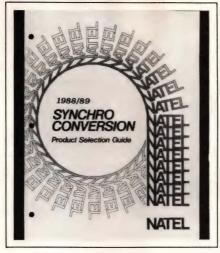
Circle No 654

## Brochure presents troubleshooting system

This 4-color brochure describes the company's Tracker 5100DS computer-controlled troubleshooting system. Noting that the Tracker 5100DS is the most advanced member of the Tracker family, the publication discusses the device's ability to examine a known-good board and then store the signature information in a PC database for recall at a later time.

Huntron Instruments Inc, 15720 Mill Creek Blvd, Mill Creek, WA 98012.

Circle No 655



## Synchro-conversion product selection

The 1988/89 Synchro-Conversion Product Selection Guide focuses on the vendor's line of synchro-conversion components and instruments. The booklet presents synchro/resolver-to-digital and digital-to-synchro/resolver converters, and synchro/resolver instruments such

as the L200 dynamic-angle synchro/ resolver simulator. The publication includes a reader service card for ordering product data sheets or for inquiries.

Natel Engineering Co Inc, 4550 Runway St, Simi Valley, CA 93063.

Circle No 656

# Handbook features data-acquisition interfaces

The vendor's product handbook No 19 surveys the complete line of data-acquisition, industrial-control and monitoring, signal-conditioning, and communications products for IBM PC/XT, PC/AT, PS/2, Apple II, and VME Bus computers. The 260-pg publication also features application notes, selection guides, and price information.

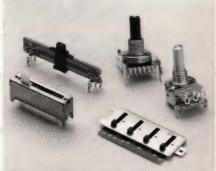
MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780.

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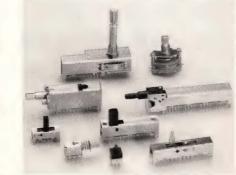
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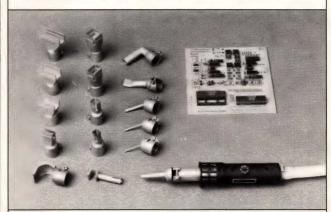


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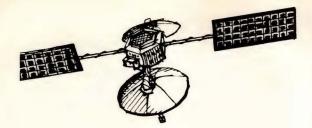
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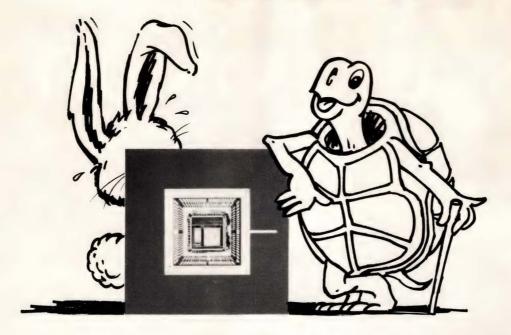
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#### 1989 Editorial Calendar and Planning Guide

Issue Date	Recruitmen Deadline	t <b>EDN</b> Editorial Emphasis	EDN News Edition
Jan. 5	Dec. 15	Power Semiconductors, Computer Peripherals Software	Closing: Dec. 20 Mailing: Jan. 12
Jan. 19	Dec. 29	Computer Boards, Analog ICs	Closing: Jan. 6 Mailing: Jan. 26
Feb. 2	Jan. 12	Semicustom ICs, Computer Boards	Closing: Jan. 20 Mailing: Feb. 9
Feb. 16	Jan. 26	Display, Analog ICs	Closing: Feb. 3 Mailing: Feb. 23
Mar. 2	Feb. 9	Digital ICs, CAE	Closing: Feb. 16 Mailing: Mar. 9
Mar. 16	Feb. 23	CAE, Analog ICs	Closing: Mar. 3 Mailing: Mar. 23
Mar. 30	Mar. 9	Integrated Circuits, Computer Boards	Closing: Mar. 17 Mailing: Apr. 6
Apr. 13	Mar. 23	Test & Measurement, Digital ICs	Closing: Mar. 31 Mailing: Apr. 20
Apr. 27	Apr. 6	Communications Technology Special Issue Communication ICs	Closing: Apr. 13 Mailing: May 4
May 11	Apr. 20	Analog Technology Special Issue Computer Peripherals	Closing: Apr. 28 Mailing: May 18
May 25	May 4	Digital ICs, Computer Peripherals	Closing: May 25
June 8	May 18	Components, Digital ICs	Mailing: June 15
June 22	June 1	Semicustom ICs, Computer Boards	Closing: June 9 Mailing: June 29
July 6	June 15	Product Showcase — Volume I, Power Supplies	Closing: June 22 Mailing: July 13
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Aug. 3	July 13	Integrated Circuits, Computer Boards	Mailing: Aug. 10
Aug. 17	July 27	Military Electronics Special Issue Military Software	Closing: Aug. 4 Mailing: Aug. 24
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Oct. 26	Oct. 5	Test & Measurement Special Issue Computers & Peripherals	Closing: Oct. 27
Nov. 9	Oct. 19	CAE, Integrated Circuits	Mailing: Nov. 16
Nov. 23	Nov. 2	16th Annual μΡ/μC Directory, Integrated Circuits	Closing: Nov. 9 Mailing: Nov. 30
Dec. 7	Nov. 16	Product Showcase — Volume I, Power Supplies	Closing: Nov. 22 Mailing: Dec. 14 N January 5, 1989

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# LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

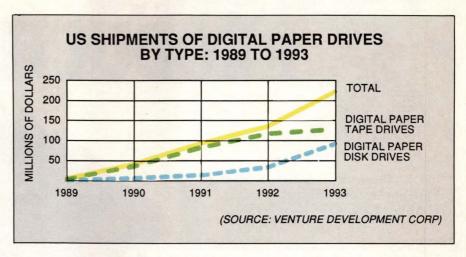
## Digital paper may reshape US mass-storage market

Digital-paper drives have the potential to provide as much as 1000 times the capacity of existing drives at a fraction of the cost. This latest development in optical storage media could revolutionize the US mass-storage market, according to Venture Development Corp (Natick, MA). The technology is currently available in two drive forms-one for driving digital-paper disks and the other for processing digital-paper optical tape. The first drives might be available in the third and fourth quarters of next year.

Digital paper is actually a thin flexible film that is manufactured in large rolls. It can be cut into various sizes and shapes. Using laser beams, the digital-paper drives etch data into an infrared-sensitive dye on the film. Once etched, the media can retain the data for 15 years—and the data is tamper-proof. These characteristics, VDC points out, make it attractive for archival purposes in large data-collection agencies such as governments, insurance companies, research laboratories, and hospitals.

A disk drive that uses 1G-byte disks is now in development and offers an access time of 40 msec, a figure that challenges other types of optical drives and some magnetic drives as well. VDC projects that WORM-drive manufacturers will suffer the most from digital paper's arrival in the marketplace. The digital-paper drives outperform WORM drives and undercut them in price.

A digital-paper optical-tape recorder has also been announced. It can hold 1000G bytes (1 terabyte) on a 12-in. tape reel. This form will be aimed at the mainframe storage market and will offer a \$5/gigabyte media cost. The digital-paper tape can store the equivalent of 5000



magnetic tapes, 1666 CD ROMs, 1000 WORM disks, 3 million floppy disks, or 1 billion sheets of typed text on a single 2900-ft reel.

VDC forecasts that digital-paper drive shipments will increase at an

average annual rate of 270% between the years 1989 and 1993. Sales of the disk drives are expected to reach \$94.5 million in 1993.

#### ISDN IC market to reach \$759M in sales by 1992

The Information Network (San Francisco, CA) projects a 263.3% compound annual growth rate for Integrated Services Digital Network (ISDN) ICs between 1989 and 1992. The ISDN represents an international effort to convert the world telephone network to all-digital operation. It promises to reduce the operating costs of telecommunications and improve telecommunications performance at the same time (see "Integrated Services Digital Network," EDN, Nov 12, 1987, pg 118).

The Information Network analyzed the growing demand for ISDN services in the US, Canada, Europe, and Japan. A total of 97,060 access lines will be installed in 1989. The largest number of the access lines will convert existing PBX lines to ISDN lines. From 1989 to 1992, this sector alone will grow from 33,600 lines in 1989 to 3,834,000 in 1992. A large number of the US installations will come from field trials by the regional Bell operating companies, but independ-

ent companies and nonaffiliated suppliers are also contributing to the market's growth.

On the European front, France, West Germany, Italy, and the UK all have wide-ranging plans to test and install an ISDN network that will be compatible for all of Europe. France began commercial ISDN operations in 1987 with a trial network of 300 small businesses and professional organizations in Britain. West Germany launched a pilot program in 1986 for 800 subscribers; this year, 8 switches will serve 8000 users in that country. That figure is expected to grow to 85,000 by 1990.

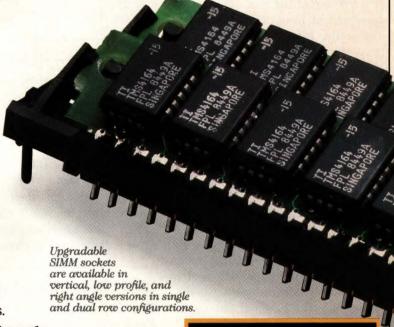
Japan's NNT is in the process of installing a commercial ISDN service between Tokyo and Osaka (it's been conducting field tests since 1983). In Canada, Bell Canada serves federal agencies in Ottawa that intend to use DMS-100 digital switches from Northern Telecom for six ISDN applications, including wide-area networking and digital telephony.

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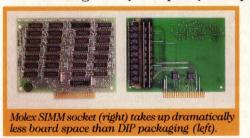
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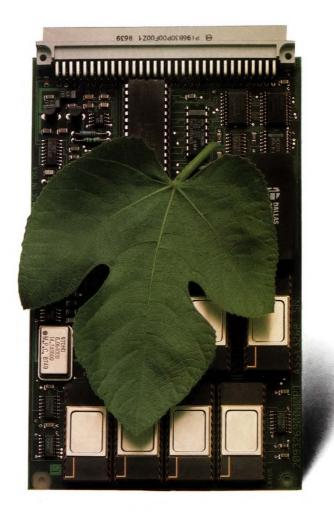
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For the bare facts about technical details and quantity pricing, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/721-8000; Telex 752602 UDS HTV.



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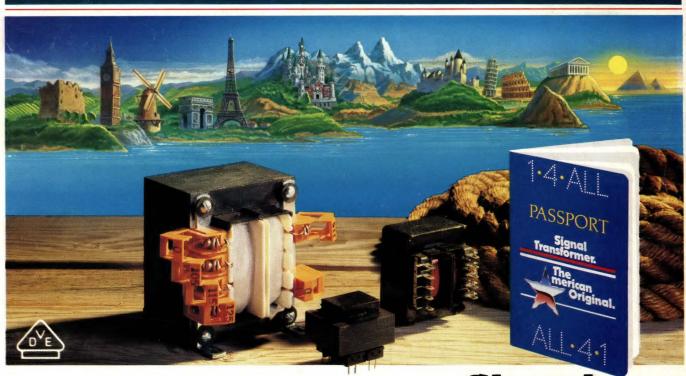
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