A CAHNERS PUBLICATION

OCTOBER 27, 1988

EDN®

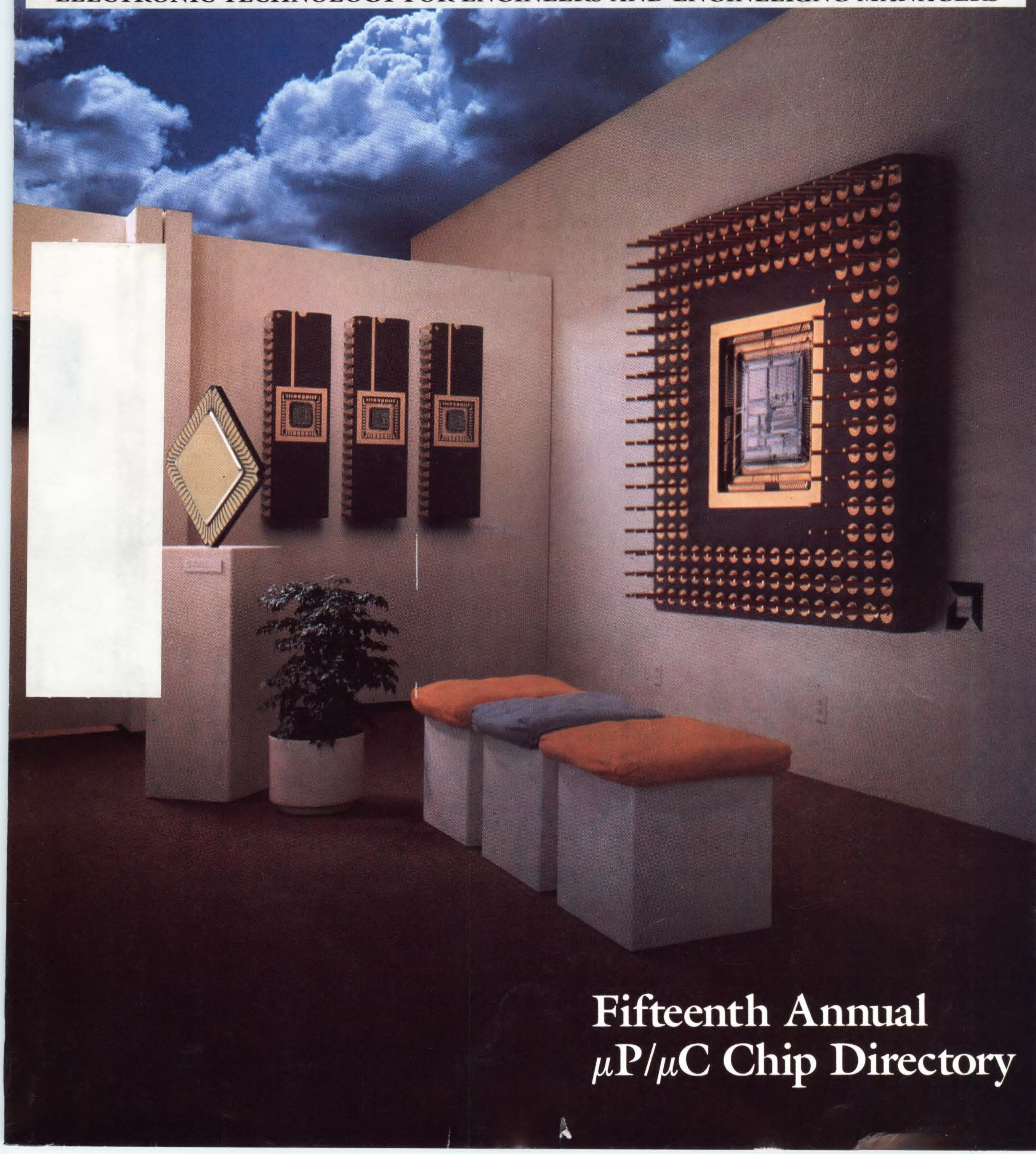
Designer's Guide to dc/dc converters—Part 2

High-capacity 3½-in. floppy-disk drives

EEPROMs

Wescon/88 and Electronica show previews

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Fifteenth Annual μP/μC Chip Directory

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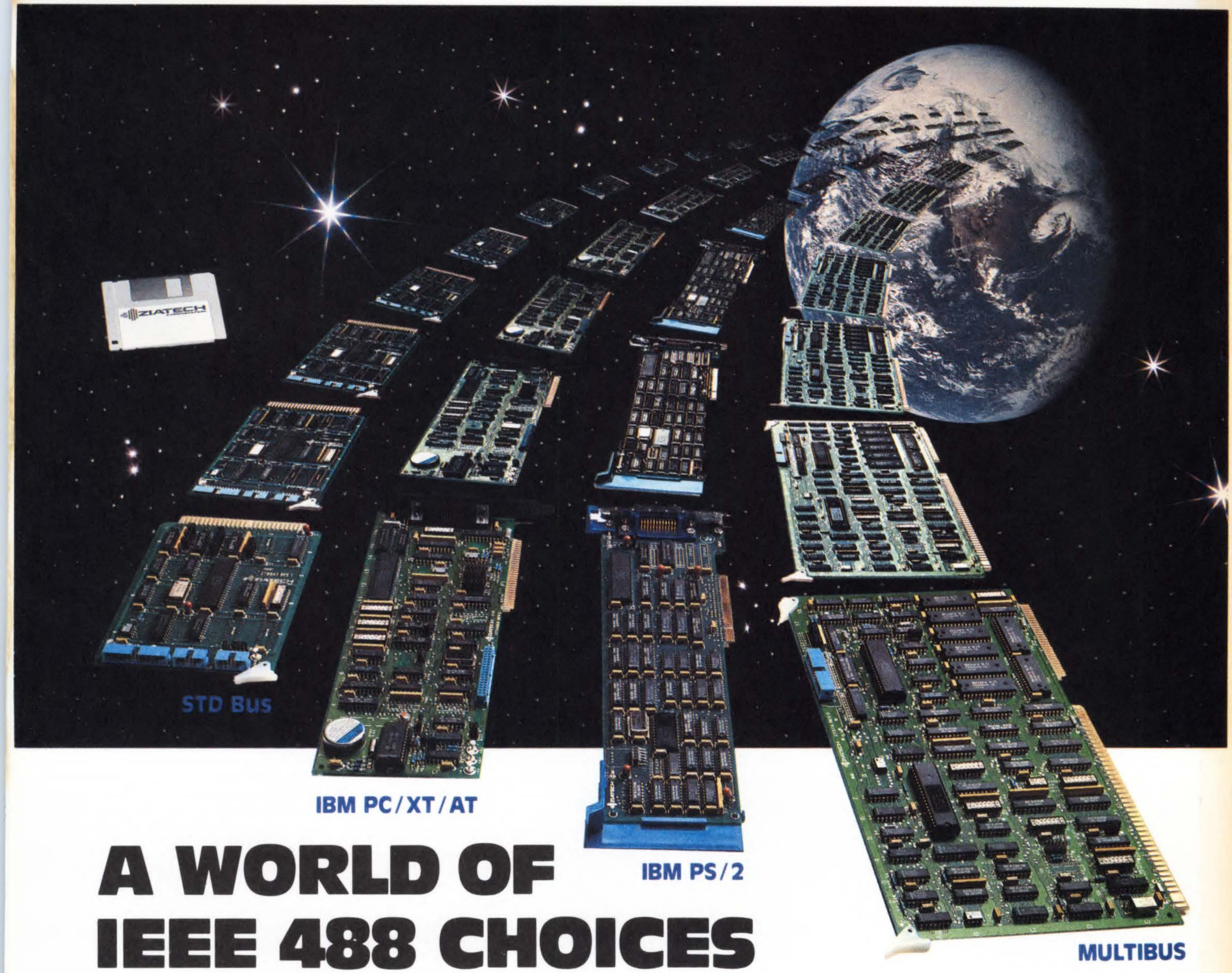

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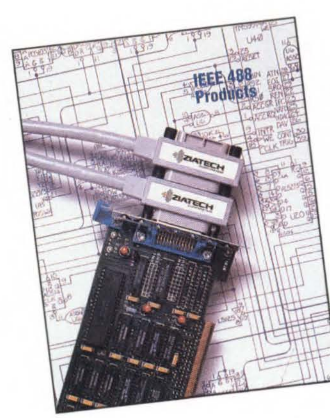

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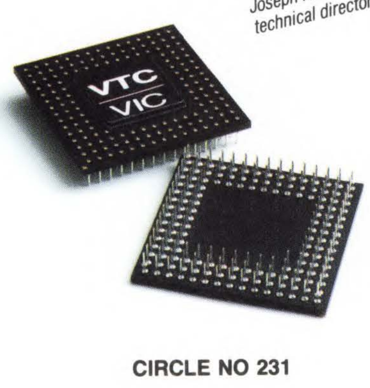
Joseph Ramunni, chairman (left), and Jack Regula, technical director, VME Technology Consortium.



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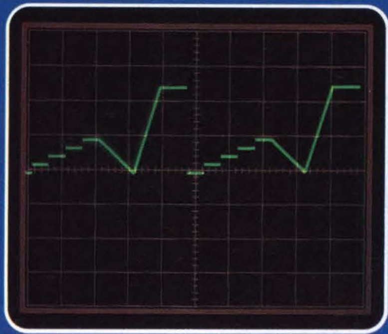
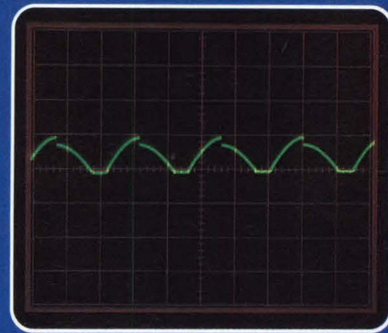
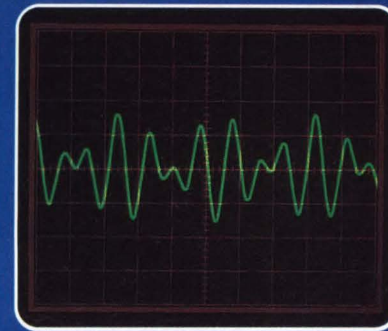


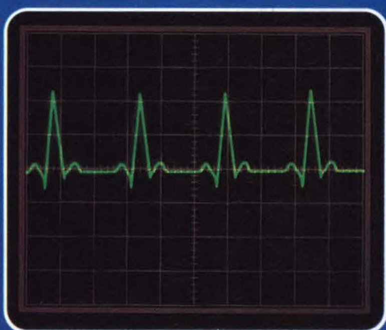
Vibration analysis
with stop and hold.



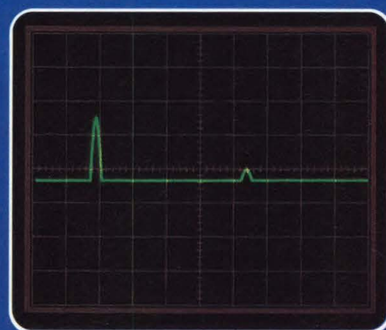
Complex waveforms
for servo drives.



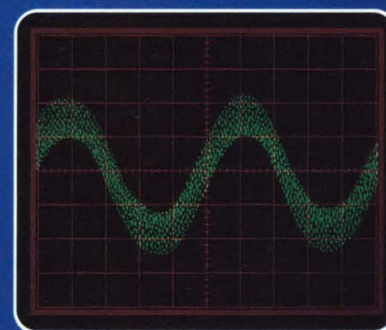
Dual tones for
telephone testing.



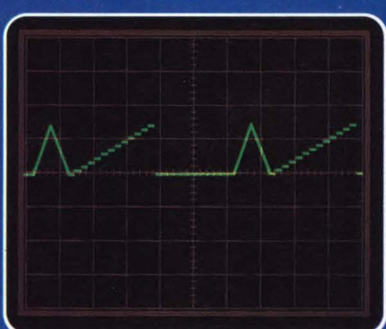
EKG and hemodynamic
waveforms.



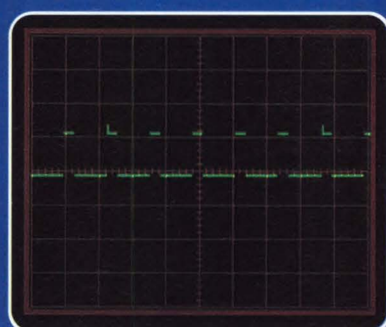
Radar/sonar envelope
simulation.



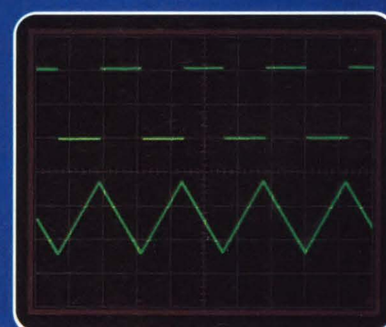
Noise added to
any waveform.



A/D, amplifier development
and calibration.



Digital testing and
troubleshooting.



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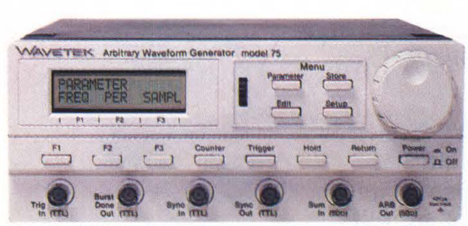

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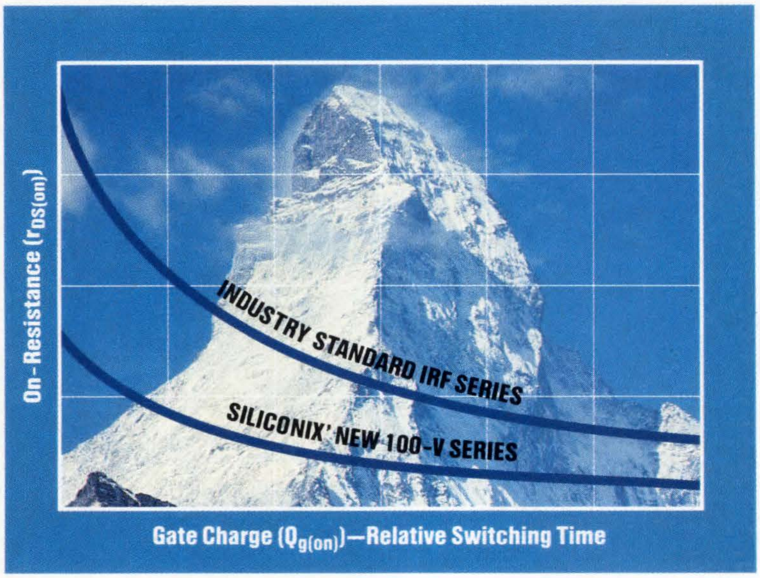

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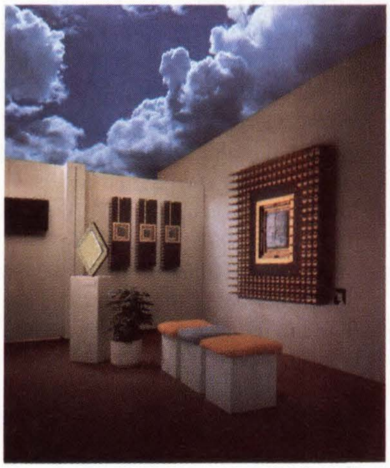

On the cover: Browse through EDN's Fifteenth Annual $\mu P/\mu C$ Chip Directory to find the best device for your needs. This year, the spotlight is on embedded-controller chips. See pg 164. (Photo courtesy Advanced Micro Devices)

SPECIAL REPORT

EDN's 15th Annual $\mu P/\mu C$ Chip Directory — 164

Forget about RISCs, MIPS, and Dhrystones. This year, the real action revolves around new embedded-controller μP chips.—*Jon Titus, Editor*

DESIGN FEATURES

Designer's Guide to dc/dc converters—Part 2 — 285

This article, part 2 of a 4-part series, provides tips on selecting the right instrumentation to evaluate the performance of your low-power 5, 12, and $\pm 12V$ converter designs.—*Jim Williams and Brian Huffman, Linear Technology Corp*

Use npn and pnp devices effectively in semicustom arrays — 297

Although accustomed to using npn and pnp transistors of equivalent performance, many analog-circuit designers have difficulty with the lower performance pnp transistors usually found in semicustom arrays. Yet you can in fact use a combination of npn and pnp devices in a variety of useful circuits.—*Winthrop Gross, Tektronix Inc*

Designer's Guide to PC-based analog pc-board design—Part 2 — 315

Unfortunately for analog engineers, PC-based software for pc-board layout does not easily accommodate the distinct requirements of analog design. This article offers some tips for making the most of the packages available today.—*Kimberley F Quirk, Engineering Services Group*

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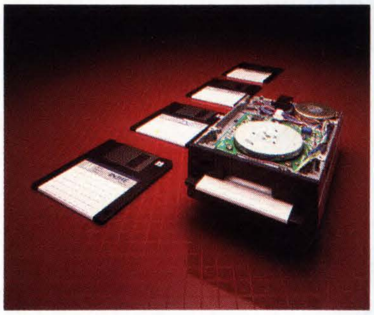

***The performance** of some of the new 3M- to 20M-byte, 3½-in. floppy-disk drives rivals that of some low-cost Winchesters (pg 103.)*

TECHNOLOGY UPDATE

Interactive simulation packages prove faster and more versatile than ever 65

Computer-simulation software has seen both quantitative and qualitative changes in recent years.—*Chris Terry, Associate Editor*

Conventional EEPROMs and flash EEPROMs offer a spectrum of bit densities 89

Applications abound for nonvolatile memory devices capable of occasional reprogramming.—*John A Gallant, Associate Editor*

Recent 3M- to 20M-byte, 3½-in. floppy-disk drives suit mainstream uses 103

Will 3½-in. floppy-disk drives that store 3M to 20M bytes venture forth into mainstream applications or will they be relegated to niche applications?—*Maury Wright, Regional Editor*

Mix business with pleasure at Munich's Electronica 113

Electronica '88 is Europe's largest exhibition for electronics components and assemblies.—*Peter Harold, European Editor*

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Wescon/88 will focus on engineering workstations and automated design tools 133

Wescon/88 will have more than 1300 booths showcasing a wide variety of electronics products.—*Clare Mansfield, Associate Editor*

Europe 1992 poses a challenge for the US electronics industry 139

After 1992, European countries will no longer raise protectionist barricades against products from their neighbors.—*Jack Gee, Contributing Editor*

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US electronics shipments up 16% in first half of 1988 . . . 3½-in. flexible drives to claim 82% of 1992 market.

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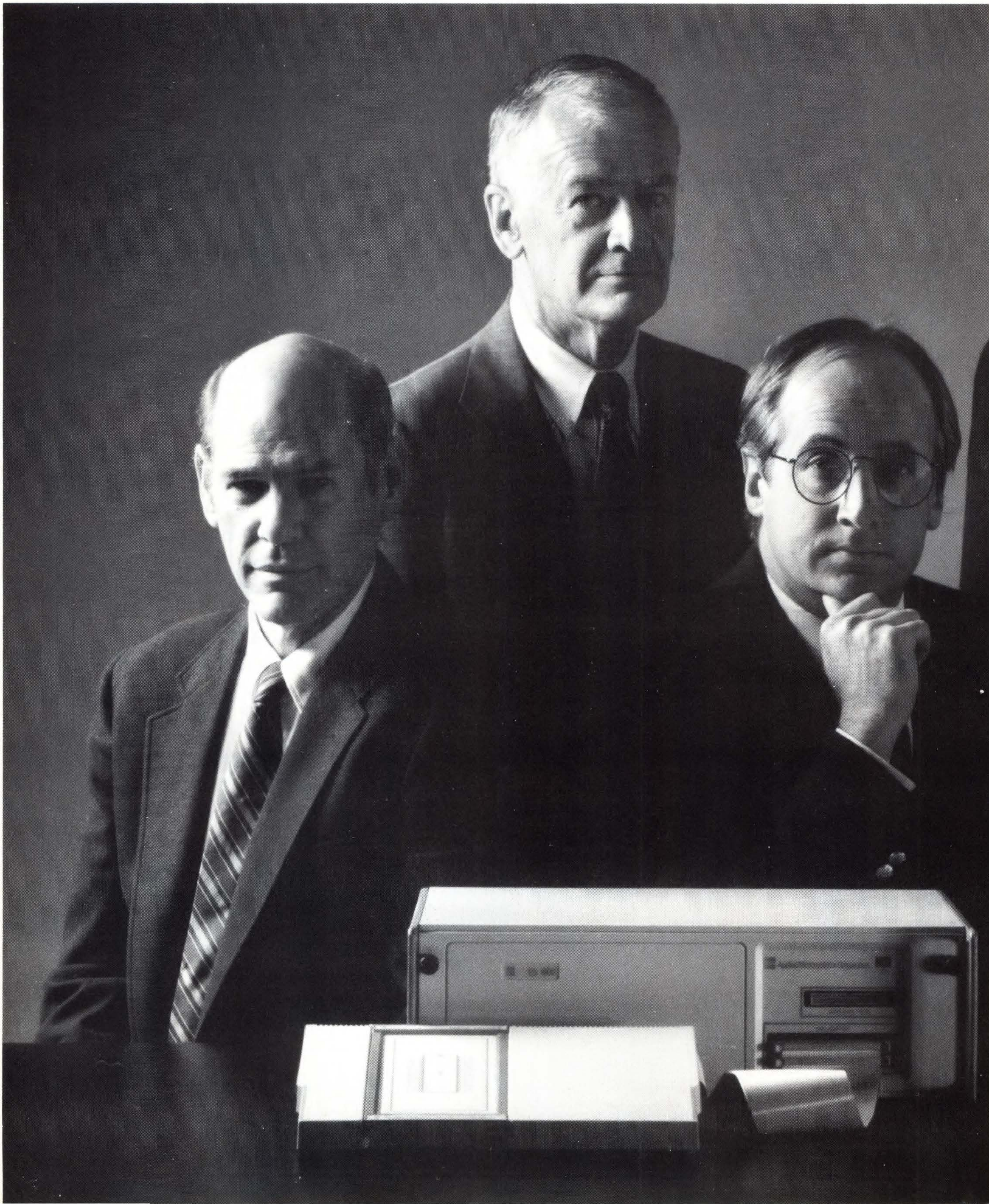

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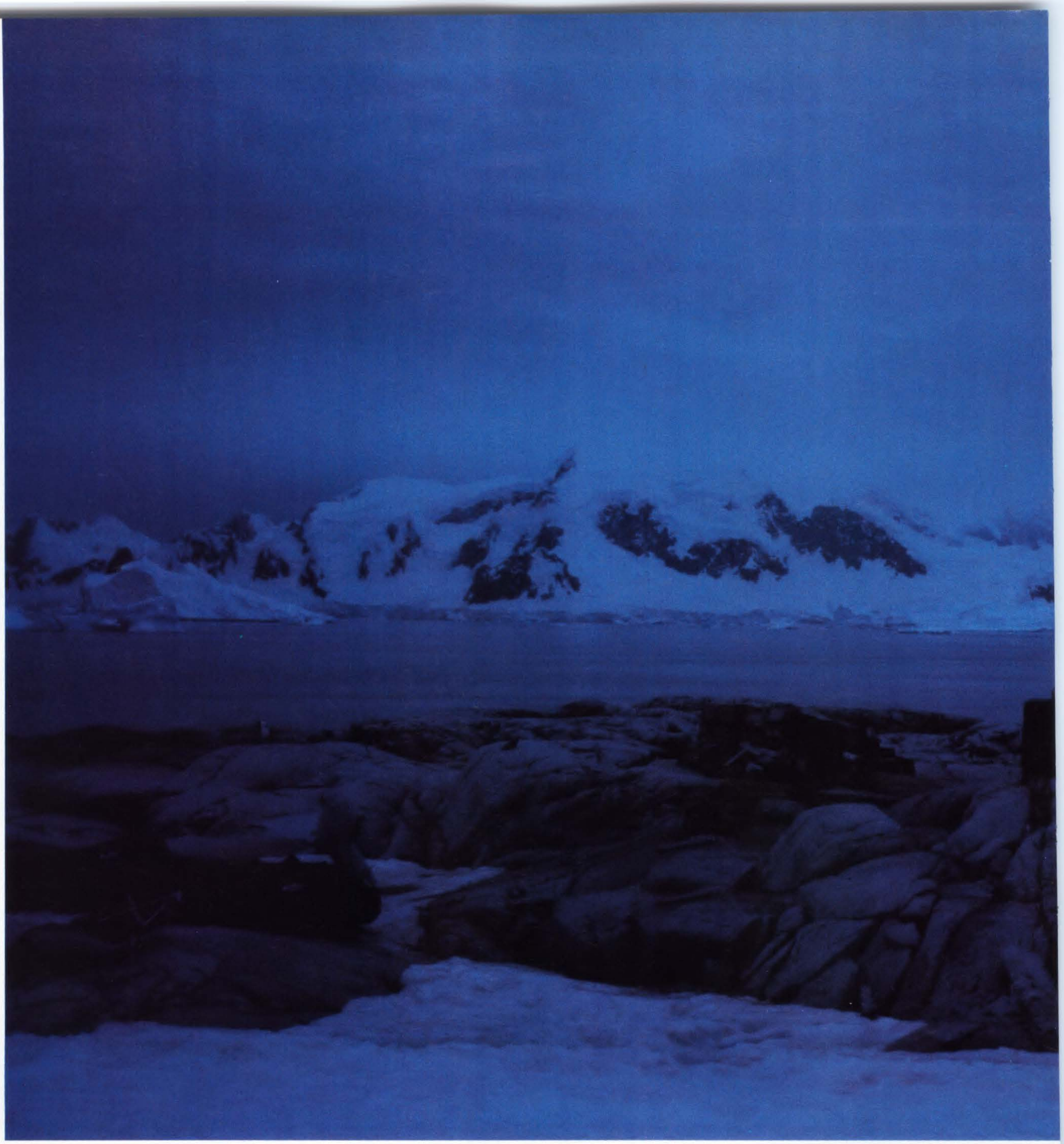

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NEWS BREAKS

EDITED BY JOANNE CLAY

ACCESSORY MODULE BOOSTS SCOPE'S SAMPLE RATE TO 2 GHZ

Comprising a power splitter and a precision delay line packaged in a plug-on module, the $1625 HP 54114A test set from Hewlett-Packard (Palo Alto, CA; phone local office) allows you to team both 1G-sample/sec channels of the company's 54111D digital sampling oscilloscope (DSO) to create one channel with a 2-GHz digitizing rate and a 500-MHz bandwidth. Previously, the company published an application note (#HP 54111D-1) that explains how to obtain this faster sampling rate with the 54111D, an IEEE-488 controller, a 500-psec delay line, and a 50Ω power splitter. However, the company recently changed the DSO's firmware to accommodate the test set, eliminating the need for the IEEE-488 controller. If your 54111D's serial-number prefix is 2840 or higher, your scope will work with the test set. Older DSOs require an HP 54111D-68702 upgrade kit, which costs $2625 and includes the 54114A test set.—Steven H Leibson

BOARD- AND CHIP-LEVEL PRODUCTS FEATURE VGA ENHANCEMENTS

The IBM PS/2 computer with its Micro Channel architecture may or may not become as popular as its forerunners, the PC/XT and PC/AT, but the PS/2's video adapter, the IBM VGA, is already firmly entrenched. Two products offer enhanced versions of the VGA. The first is the CL-GD510A/520A chip set from Cirrus Logic (Milpitas, CA, (408) 945-8300), which features a 32-bit-wide interface to video memory. It costs $40. The company also sells either an 8- or a 16-bit ROM-based basic I/O system (BIOS), as well as a BIOS that can be uploaded to system RAM for maximum performance on the 32-bit internal buses of 80386-based systems. The second product is the Paradise VGA Plus 16 board from Western Digital Imaging (Mountain View, CA, (415) 349-8400). The board uses its Autosense capability to determine whether or not the host system has a 16-bit data bus, and thus whether it should use an 8-or a 16-bit video BIOS. The board costs $499.—Margery Conner

MILITARY FLOATING-POINT PROCESSOR PERFORMS 75M FLOPS

Two on-chip multipliers and three on-chip ALUs allow the 15-MHz UT69532 IQMAC floating-point processor to execute 75M flops. While performing this feat, the $1845 CMOS chip—from United Technologies Microelectronics Center Inc (UTMC, Colorado Springs, CO, (719) 594-8000)—dissipates less than 2W over the full military temperature range (−55 to 125°C). The IQMAC performs 32-bit floating-point operations that conform to IEEE standard 754-1985. The chip performs real-number operations in one clock cycle and complex-number operations in one or two cycles. On-chip, built-in self-test logic, including a signature analyzer, verifies the IQMAC's operation by using 32,000 unique test vectors. UTMC says that it will begin delivering the IQMAC in 248-pin PGA and 304-lead flatpack packages by the second quarter of 1989.—Steven H Leibson

STACKED HEADERS MAXIMIZE AVAILABLE SPACE ON PC BOARDS

If you need to conserve space when designing your next pc board, consider using the condo-style header system developed by 3M (Austin, TX, (512) 834-6792). By stacking two right-angle boxed headers, you can make use of the free space above your pc board. Designed with 0.155-in. solder tails for use with 0.100×0.100-in. pc grids, a 50-position, long-latch stack header costs $12.01 (1000). You can order other configurations that accommodate 20 to 128 leads in either a low-profile 0.63-in. or a 0.675-in. housing suitable for robotic insertion.—J D Mosley

NEWS BREAKS

RUGGEDIZED 2½-IN. WINCHESTER STORES 20M BYTES

Targeting lap- and portable-computer applications, the Prairie 220 hard-disk drive stores 20M bytes in a 2½-in. form factor. The drive, from PrairieTek Corp, (Longmont, CO, (303) 772-4011) consumes an average of 1.5W, weighs 9 oz, and occupies 30% as much space as a standard 3½-in. drive does. You can purchase the drive with an embedded SCSI or IBM PC/AT controller. The drive specs a 28-msec average seek time. To ensure that the drive will operate reliably in rugged environments, the company developed a ramp mechanism to load and unload heads, and to lock the heads into place when power is removed. The drive costs $400 (OEM qty) and is currently available in limited production quantities. The firm plans to offer higher-capacity 2½-in. drives in the first half of 1989.—Maury Wright

LOW-COST LOGIC COMPILER FOCUSES ON GAL DEVICES

The PLAQ logic compiler from Querty (San Diego, CA, (619) 455-0500) is priced at $395 and supports only GAL (Generic Array Logic) devices from Lattice Semiconductor Corp. Because the logic compiler is dedicated to GAL devices, you don't need to set configuration fuses on the GALs—PLAQ derives it from your design. You can enter designs either as equations or as truth tables. The logic compiler also lets you run simulated test vectors through a design before you program the part. First-time GAL users will find helpful tutorial information in the logic compiler's instruction manual.—Doug Conner

ISDN SOFTWARE KIT AIDS IN NETWORK CONNECTIVITY

Compatible with CCITT Q.931 and X.25 recommendations, the AmLink3 software-development kit from AMD (Austin, TX, (512) 462-4360) provides you with OSI layer 3 software, two ISDN terminal coprocessor boards, and two Digital Exchange Controller boards and software. The kit lets you design terminal equipment that provides for voice and data communications through OSI layer 3. It also lets your terminal equipment communicate directly with AT&T's central-office switch. The AmLink3 software kit costs $40,000, including a one-time software-license fee, and comes with documentation and development tools. You can order a layer 2 AmLink LAPD/LAPB kit for $12,000.—J D Mosley

MOTOROLA AND CHERRY SEMICONDUCTOR EXCHANGE TECHNOLOGIES

The Semiconductor Products Sector of Motorola Inc (Phoenix, AZ, (602) 897-3841) and Cherry Semiconductor Corp (East Greenwich, RI, (401) 885-3600) have signed a formal agreement to exchange manufacturing technologies for selected high-volume, bipolar linear ICs. As a result, each company will have the technical capability to act as an alternate source for certain products designed by the other. By providing linear devices with equivalent electrical performance, the agreement will eliminate multiple-sourcing problems for many of the customers of both companies.

According to Steve Hanson, vice president of Motorola's Bipolar Analog IC Div, truly compatible alternate sourcing is particularly important in the market for custom linear automotive ICs, where both Motorola and Cherry have a growing customer base. Cherry Semiconductor president Alfred S Budnick indicated that the agreement provides a level of assurance and stability of supply beyond what would otherwise be possible.—Dave Pryce

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Stay Generations Ahead in Video/RF 12-Bit ADCs

When it comes to the industry's highest performance 12-bit, 10 MSPS converters, TRW LSI can keep you out front. Whatever your data acquisition problem, TRW LSI's THC1200 Series provides the solution.

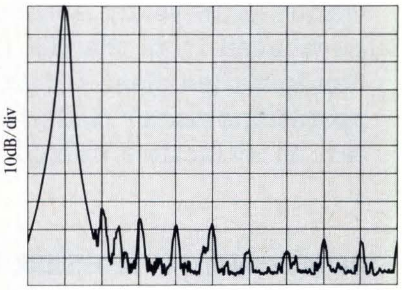
Take the THC1201: It's completely self-contained, including track/hold and all timing circuitry. Signal in, data out, all in a 46-pin hermetic DIP. Standard ±1.0V input range, ±15V and ±5V supplies, TTL interface and synchronous data output make this the easiest part of your system design.

Really cramped for space? Try the THC1202. You get the same leading-edge performance as the THC1201, but in a 40-pin package that's 40% smaller. And, as an extra bonus, you can dump that -15V power supply. And accommodate bipolar or unipolar input signals. That's not all . . .

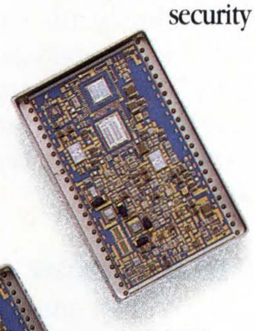
If you have signals down in the mud, our THC1200 is the solution. It offers a full scale input range of ± 167 millivolts. That means you won't need that extra low-noise gain stage. But, the whole world doesn't speak softly, so the THC1200 has a gain switch that gives you a ±2.5V input range. That's a gain shift of 15X, extending the dynamic range by over 23dB.

Need more? Give us a call. We have many other leading-edge conversion products on the drawing board. Or we'll do one just for you.

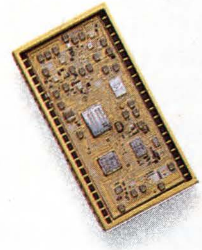
Even if you have already solved your 12-bit acquisition problem, talk to us. Remember, we guarantee full-spec performance. Plus, we can show you how to save time, space, power and money — and obtain multiple-source security without a redesign.



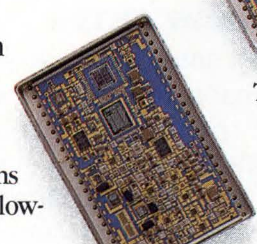
Part Number	Analog Input Range (V)	Package Style	Area (Sq. In.)	Power (W)
THC1202	±1.0	40-Pin DIP	2.3	5
THC1201	±1.0	46-Pin DIP	3.8	5
THC1200	±2.5 and ±0.167	46-Pin DIP	3.8	9



THC1200



THC1202



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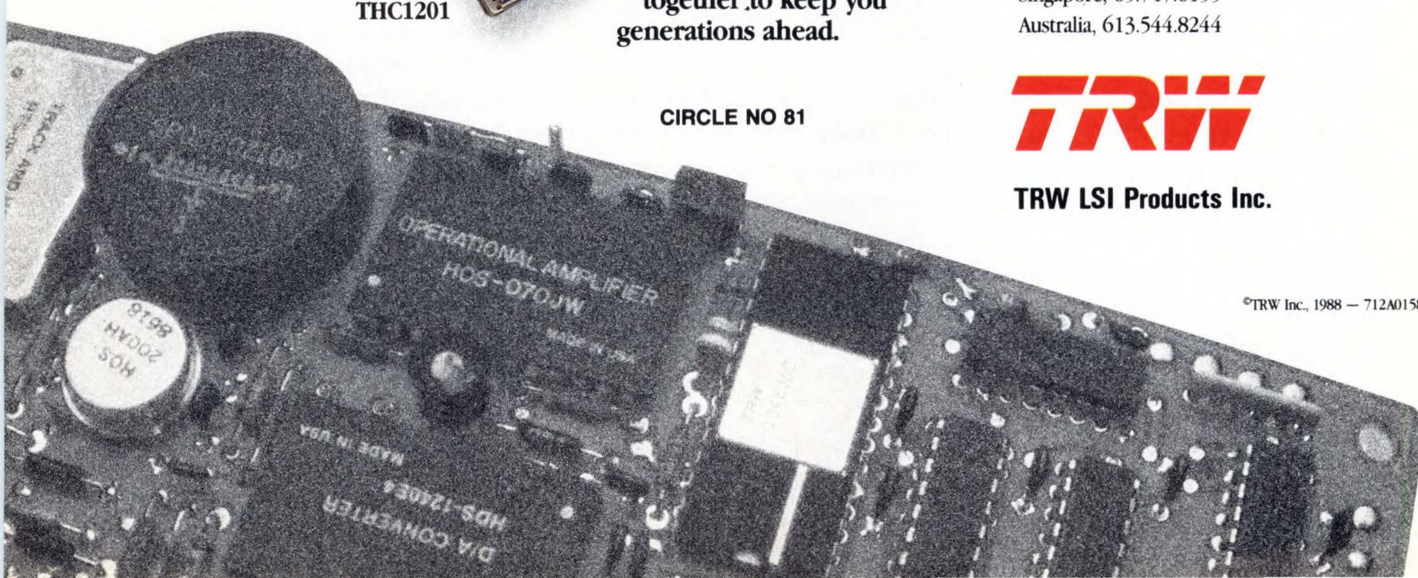

EUROPEAN COMPANY GAINS MIL-STD-1772A APPROVAL

The hybrid division of STC Components Ltd (Great Yarmouth, UK, TLX 818746) claims to be the first company outside North America to have gained US Department of Defense MIL-STD-1772A approval for its production facilities. This approval allows the company to participate in the offset-contract arrangements whereby European manufacturers are authorized to supply components for use in defense systems purchased from the US. In order to meet MIL-STD-1772A requirements, the company has installed class-100,000 clean rooms in which to carry out critical assembly operations under class-100 laminar-flow hoods. Using these facilities, the company can manufacture hybrid circuits that are qualified to MIL-STD-883C requirements.
—Peter Harold

COMPONENT TESTER MEASURES DEVICE PARAMETERS AT 1 MHz

Capable of performing 55 tests/sec with an automatic component handler, the Model 7010 component tester from Wayne Kerr Ltd (Bognor Regis, UK, TLX 86420; in the US: Woburn, MA, (617) 938-8390) is suited for high-speed component testing and binning applications. The tester measures capacitance and inductance along with a range of secondary parameters—such as Q factor, equivalent series resistance, equivalent parallel resistance, and dissipation factor—at frequencies of 1 kHz, 10 kHz, 100 kHz, or 1 MHz. Its basic measurement accuracy is 0.05% at all frequencies, and its maximum measurement resolution is 10 ppm. You can select the drive level, measurement speed, and ranging mode independently for each test frequency, and an internal compensation system automatically compensates for test leads as long as 2m. The component-handler interface allows you to sort components, according to both primary and secondary parameter limits, into as many as 30 component bins. In addition to the component-handler interface, the tester has IEEE-488 and RS-232C interfaces. It costs £5250.—Peter Harold

INTERNATIONAL PARTNERSHIP DEVELOPS ISDN CHIPS

As a result of a partnership to develop ISDN chip sets, National Semiconductor Corp (Santa Clara, CA, (408) 721-5000) and SGS-Thomson Microelectronics (Agrate Brianza, Italy, TLX 330131) have jointly announced the availability of several ISDN devices. The TP3420 (National Semiconductor) or ST5420 (SGS-Thomson) is an S- or T-interface transceiver that operates to CCITT I.430 recommendations. It's suitable for use in TE (terminal equipment), TA (terminal adapter), NT-1 (network termination), or NT-2 equipment or in PABX line cards. The TP3075/6 or ST5075/6 is a pulse-code-modulated (PCM) codec/filter with μ-law or A-law companding algorithms, time-slot assignment logic, and a direct interface to a 4.096-MHz serial PCM data highway. National Semiconductor has also announced the availability of two other products: the TP3401 full-duplex, 144k-bps burst-mode transceiver for twisted-pair subscriber loops, and the HPC16400 dedicated microcontroller, which provides HDLC controller functions for ISDN networks. SGS-Thomson Microelectronics will act as an alternate source for the TP3401. To help you evaluate the devices in S-interface applications, National Semiconductor is selling a $995 evaluation board—the TP3500—that includes software support for its onboard HPC16400 microcontroller.—Peter Harold

The P-CAD Software That Made This Famous Laptop Computer Is Now Made To Fit Your Budget.

When Zenith Data Systems needed to pack power into their laptop computers they turned to P-CAD®'s Master Designer™ printed circuit board software.

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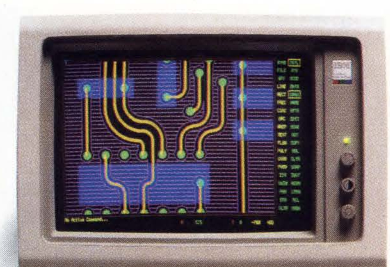

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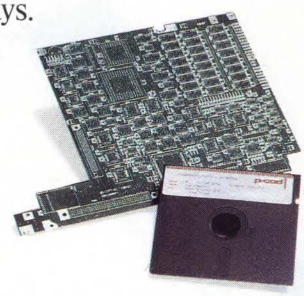

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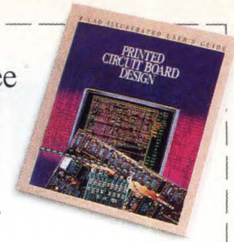

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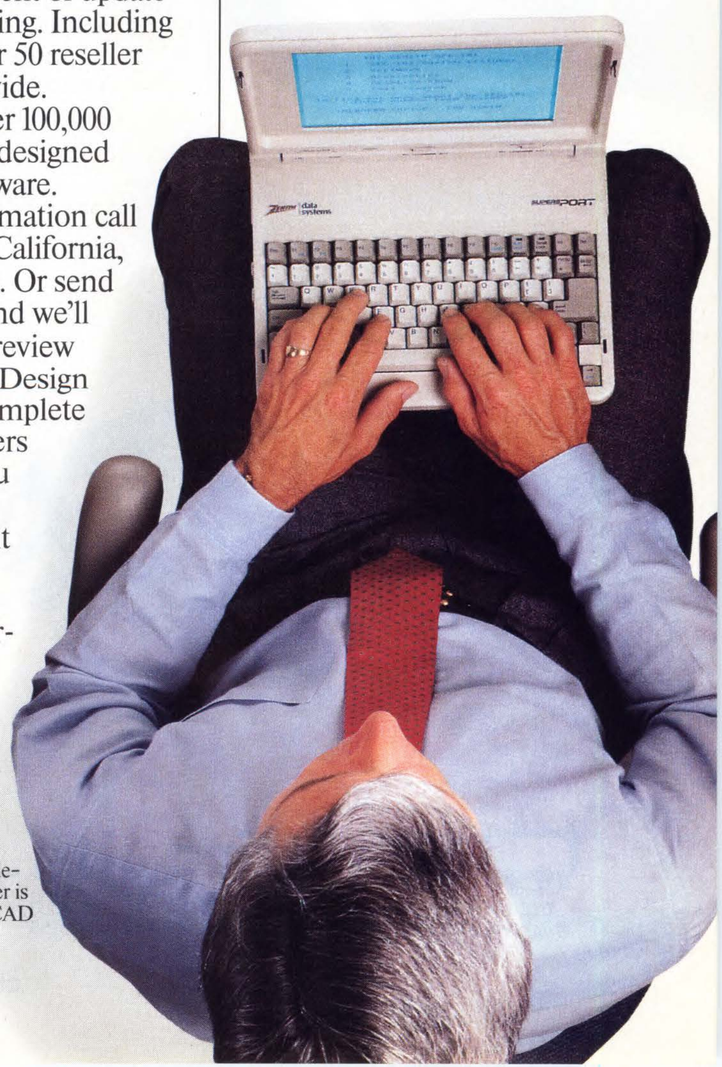

tiny SPDT switches

absorptive... reflective

dc to 4.6GHz from $32.95 (1-24)

Tough enough to pass stringent MIL-STD-883 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	**-5V** on, OV off		**-5V** on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (1-24)	**$32.95**		**$48.95**	
	$72.95		**$88.95**	

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setting higher standards

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CIRCLE NO 83

SURFACE MOUNT MIXERS

2^{49} (1,000 qty)

The opportunity for automated, low-cost assembly is a key benefit of surface-mount technology, but is often wiped out by the high price of surface-mount components. Now, Mini-Circuits offers a new series of mixers to meet the pricing demands of SMT ... only $2.49 in 1,000 quantity ($3.75 ea. in quantity of 10) ... at a cost even lower than most conventionally-packaged mixers.

The SCM-1 spans 1 to 500MHz with only 6.0dB conversion loss, 45dB LO-RF isolation, and 40dB LO-IF isolation. Housed in a rugged, non-hermetic 0.4 by 0.8 by 0.3 in. high (maximum dimensions) plastic/ceramic package. Spacing between connections is 0.2 in. The mixer is offered with leads (SCM-IL) or without leads (SCM-INL) to meet a wide range of pc board mounting configurations.

Each SCM-1 is built to meet severe environmental stresses including mechanical shock/vibration as well as temperature shock. The operating and temperature storage range is −55°C to +100°C. Each SCM-1, designed and built to meet today's demanding reliability requirements, carries Mini-Circuits' exclusive 0.1% AQL guarantee of no rejects on every order shipped (up to 1,000 pieces).

When you think SMT for low-cost production, think of Mini-Circuits' low-cost SCM mixers.

SPECIFICATIONS (typical)	SCM-1L (with leads)	SCM-1NL (no leads)
FREQ. RANGE (MHz)		
LO, RF	1-500	
IF	DC-500	
CONVERSION LOSS (dB)		
Mid-Band (10-250MHz)	6.3	
Total Range (1-500)	7.5	
ISOLATION (dB)	(L-R)	(L-I)
Low-Band (1-10MHz)	60	45
Mid-Band (10-250MHz)	45	40
High-Band (250-500MHz)	40	35
PRICE	$2.49 (1,000 qty) $3.75 (10-49)	

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

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C115 REV. ORIG.

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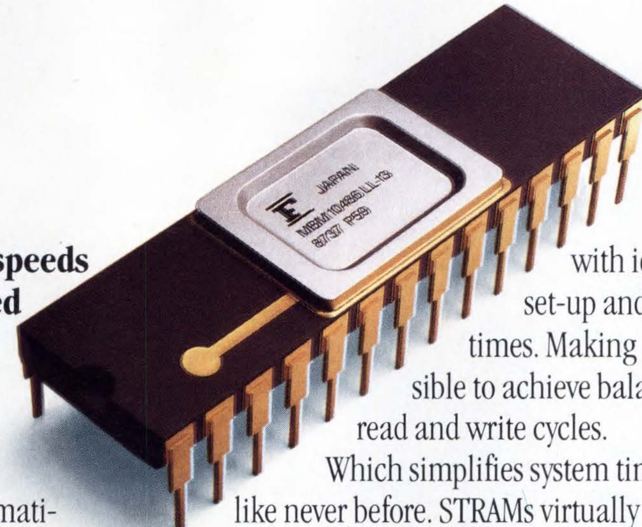

Finally. A series of fast-access, self-timed ECL RAMs (STRAMs). With all the onboard logic you need to dramatically improve your high-performance system cycle times. Not surprisingly, they're from Fujitsu Microelectronics.

Outwardly, our new STRAMs may seem like conventional RAMs. But we've given them a highly unconventional sense of timing. Which takes the worry out of shrinking write windows and faster cycle times.

In fact, these timely devices let you forget all about setting the write pulse. Because the STRAM does it for you. Simply and precisely. Using an onboard write-pulse generator that automatically generates the pulse.

What's more, the STRAM never loses track of the time. Its inputs and outputs are fully synchronous to the clock signal. The self-timed write operation is initiated when the clock signal and the write strobe jointly start the write-pulse generator cycle.

On-chip timing generation not only frees you from the need for external control of the write pulse width. It also provides you with identical set-up and hold times. Making it possible to achieve balanced read and write cycles.

Which simplifies system timing like never before. STRAMs virtually eliminate setup delays caused by signal skew, enabling your system to operate at maximum throughput.

As a result, you can spend far less time checking your pulse and far more time reaping the benefits of improved system performance.

We've even made STRAMs available in both latched and registered versions. In 1K x 4 and 4K x 4 configurations. With cycle times of 9 ns for the 1K x 4 devices and 13 ns for the 4K x 4 devices. All on less real estate than conventional RAMs and their peripheral circuitry.

Best of all, they're from Fujitsu Microelectronics. The partner you can count on. Now and in the future. Providing you with the edge you need to always stay ahead.

To find out more about our new family of self-timed RAMs, call 800/642-7616. We'll show you how easy it is to stop watching the clock.

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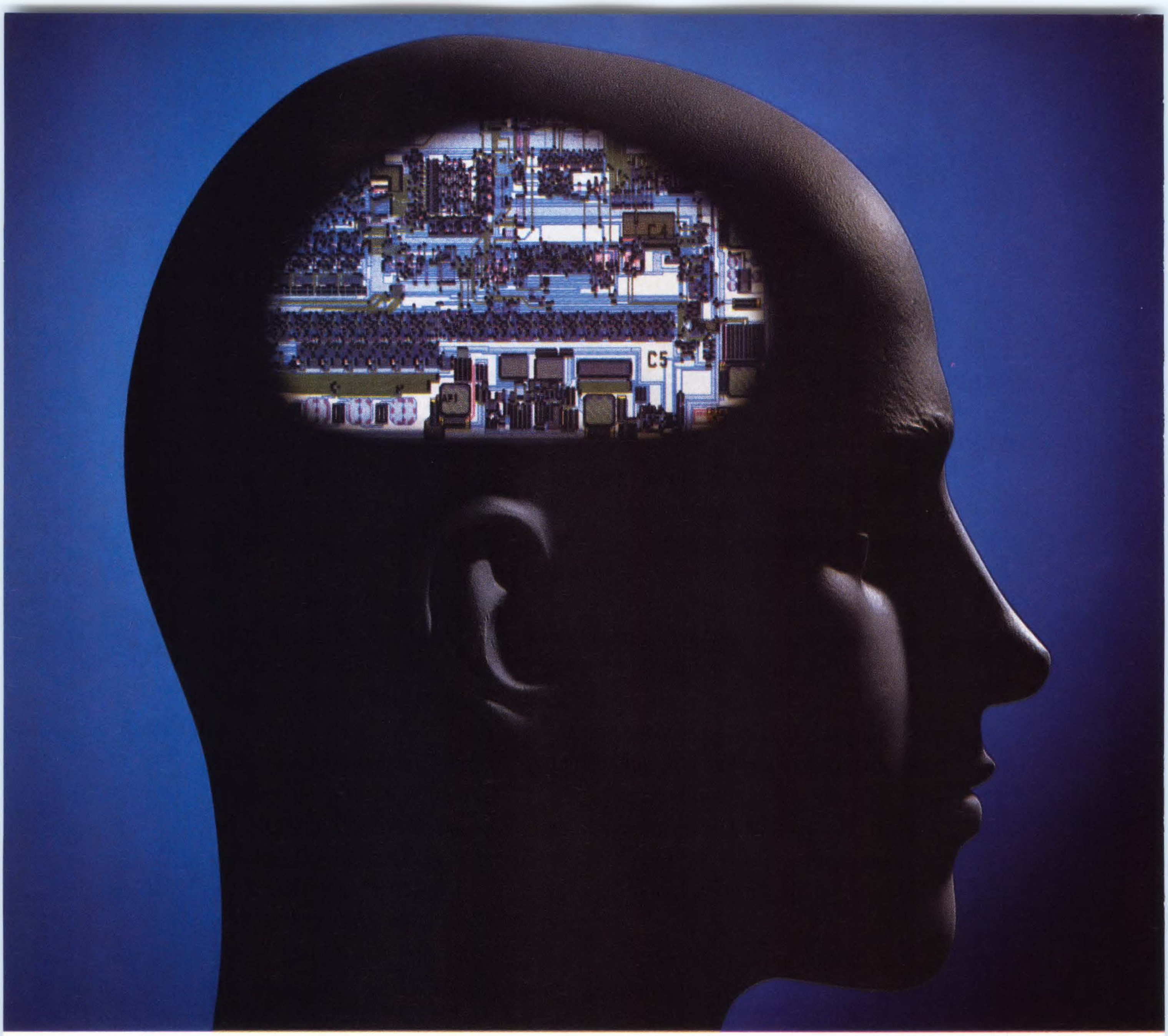

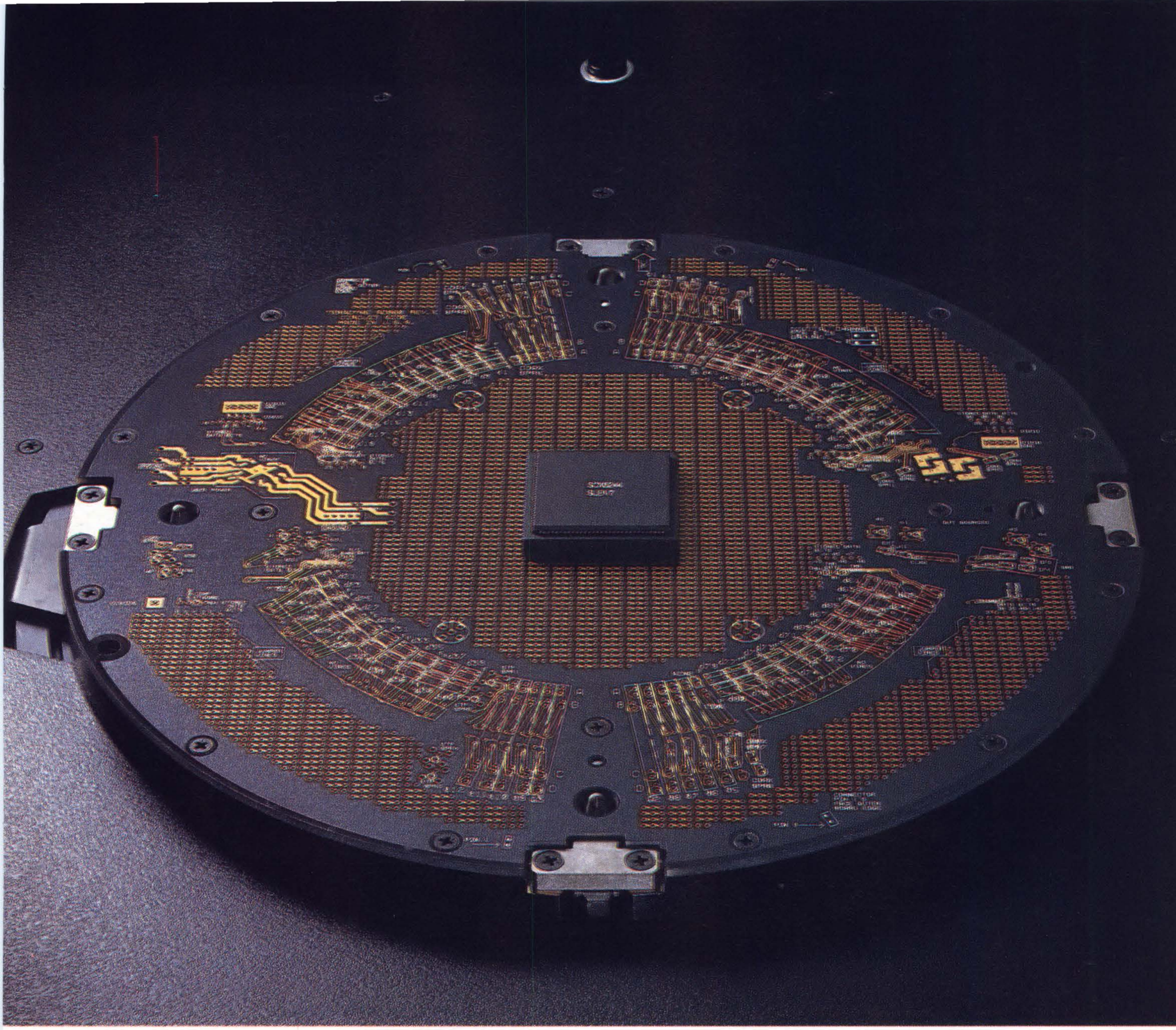

this system can test.

to test per test head, and the A520, which packs all the performance of an A500 into a smaller footprint at a lower capital cost.

Teradyne's new A500 family not only gives you the capability to test the range of today's devices, it's ready to help you test tomorrow's devices, as well.

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SIGNALS & NOISE

It's time to dump the old ±15V standard

Thanks to John Shier and Jerry Thimsen of VTC Inc for their article "New ±5V standard unshackles analog-IC designers" (EDN, June 9, pg 229). I have been doing analog design work since the early 1970s, and I have never run anything on more than 12V, because to do so would either create problems in interfacing with digital ICs or make it difficult to power the whole thing from batteries, if desired. Also, higher voltages, even in dedicated line-powered equipment, didn't buy me anything more than increased power-supply costs. Apparently, most engineers who design around the ±15V standard let someone else figure out the power supply.

In recent years, some IC manufacturers have been willing to abandon the ±15V requirement on some products, particularly those manufactured with CMOS technology. I suppose that in terms of total usage, the Texas Instruments TLC line of op amps and comparators (and a few other items) is the best example. This is a very welcome development. And some products that use slow, high-voltage processing are designed to permit operation on low-voltage supplies—the LM324 and LM339 are probably the best examples.

There is some movement toward the ±5V standard you describe, particularly by manufacturers of D/A converters (who have apparently not yet learned how to make CMOS voltage-output DACs—but that's a sermon I should save for another time) and system engineers who are incorporating ECL in their systems. However, there is also some movement toward single-supply 5V systems with or without an analog ground of 1.25 or 2.5V. Our in-house standard for instruments powered from 9V transistor batteries or 12V battery packs is 6V with a 2.5V analog ground: Host ICs will run on this voltage (BiMOS is a no-

table exception), and we can use either high-speed CMOS or metal-gate CMOS. The biggest limitation of the 6/2.5V standard is that certain microprocessors and other LSI devices are not guaranteed at 6V, and so we're now considering adopting a 5/2.0V standard. Such a standard severely limits our choice of analog components, but bit by bit we are finding components that will work satisfactorily on this supply—including high-speed OTAs.

Again, I'm pleased to see Shier and Thimsen stick their necks out and holler for dumping the old ±15V standard. I hope others will climb aboard that bandwagon.

David E Johnson
Fisher Research Lab/
Los Banos, CA

Vendors should supply Spice models

I would like to compliment one of the advertisers in your July 7, 1988 issue, Linear Technology, for its Design Notes "An LT1013 and LT1014 Op Amp Spice Macromodel."

There is a profusion of analog-circuit simulation software on the market, most based on Berkeley Spice. The software frequently supplies a reasonably complete library of standard devices. Problems arise when a nonstandard part is required. Estimations from manufac-

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CIRCLE NO 88

turers' data sheets are sometimes—not always—accurate.

I was pleased to see a circuit manufacturer, the organization most familiar with its own circuit's performance, supply a Spice model. I encourage other vendors to make such models available also. Indeed, let's move into the electronic era: Why not make these models available through the more popular online databases?

When simulation runs without too many source-code bugs, and when simulation results closely correlate with actual circuit performance, the result is rewarding—not only emotionally, but cost- and time-wise, too. For manufacturers to make Spice models as available as data sheets would be a big step toward hassle-free simulation.

Glenn Fasnacht
Senior Reliability Engineer
Smith Meter Inc
Erie, PA

By any other name

Please note that EDN used the term "TRIMPOT" incorrectly in the New Products section of the August 4, 1988 issue (pg 234). "TRIMPOT" is a registered trademark of Bourns Inc for its line of trimming potentiometers, and it is improper to apply the term to trimmers manufactured by other firms. We apologize for the error.

Address corrections

Readers who tried to reach Virtual Instrument Corp in Connecticut by calling the number listed in the Special Report on Virtual Instruments (EDN, September 1, 1988, pg 126) reportedly reached a Colorado waterbed store instead. Our apologies for the area-code gaffe. Meanwhile, the firm has moved. You can contact the company (no kidding) at:

Virtual Instrument Corp
23 Clarke Circle, Unit #5
Bethel, CT 06801
(203) 748-2000
FAX 203-798-8863 TLX 4930512

Also please note that the µP Support-Chip Directory in EDN's June 9, 1988 issue contained an incorrect address for Toshiba America Inc's Electronic Components Business Sector (pg 143). The correct address is 9775 Toledo Way, Irvine, CA 92718; phone (714) 455-2000. Readers wishing to contact the company's Semicustom Division, which includes ASIC marketing, should use the same address.

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

MAXIM
DESIGN NEWS
Analog Design Insights from Maxim Integrated Products November '88

New μP Supervisory ICs Improve System Designs

Sharply reduce the complexity, component count, and space of standard microprocessor supervisory circuits; improve the accuracy and reliability of reset and battery-switchover circuits; add to that a watchdog timer and write protection. The result: the MAX690 series of microprocessor supervisory ICs, which pack many common housekeeping functions into 16-pin and 8-pin packages. The MAX690 Series is comprised of eight ICs that feature pre-trimmed (50ms, 200ms) or user-adjustable reset timing, enabling them to meet the specs of any μP.

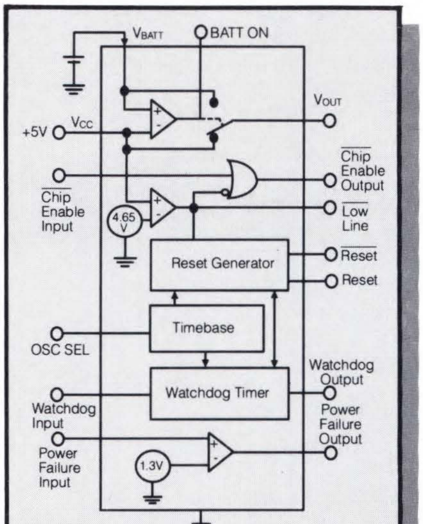


Figure 1.

Micropower For Battery Applications

The MAX690-697 offer precise pre-trimmed 4.65V or 4.4V and user-adjustable 3.0V to 5.5V threshold voltage detectors which issue a reset pulse for any supply voltage problem. The newest member of the family, the MAX697, features a micropower supply current (160μA) providing a single-chip supervisory solution for battery powered systems.

Because the needs of μP systems defined the ICs, they contain several seemingly distinct functions that microprocessors commonly need (Fig. 1). For one, the chips have a precise threshold detector and a timer that generate an accurate reset signal for any power-up, power-down, brownout, or momentary-interrupt condition. For another, power-switchover circuitry offers a battery backup for CMOS RAMs or a real-time clock. On top of that, an uncommitted 1.3V threshold comparator can serve as a power-failure warning indicator or monitor for the backup battery.

To keep the microprocessor from writing incorrect data into a CMOS RAM or EEPROM during power-up, power-down, or brownout, there is chip-enabling circuitry. This circuitry forces a Chip Enable Output high whenever the power supply falls below the threshold detector voltage. Moreover, the chip's watchdog timer monitors software execution, resetting the microprocessor if execution is disrupted for any reason.

Power-On/Low Line Reset

The reset function relies on a reference-voltage technique that is

Part #	Pins	Reset (Volts)	Isupply (mA) Typ	Reset (ms)	Battery Switch	Memory Protect	Lowline In	Lowline Out
MAX690	8	4.65	4	50	Yes	No	No	No
MAX691	16	4.65	4	50*	Yes	Yes	No	Yes
MAX692	8	4.40	4	50	Yes	No	No	No
MAX693	16	4.40	4	50*	Yes	Yes	No	Yes
MAX694	8	4.65	4	200	Yes	No	No	No
MAX695	16	4.65	4	200*	Yes	Yes	No	Yes
MAX696	16	Adj	4	50*	Yes	No	Yes	Yes
MAX697	16	Adj	0.16	50*	No	Yes	Yes	Yes

* default; also adjustable

(Please see uP Supervisory IC's on back)

3 1/2 Digit A/Ds Work With a Single +2.5V to +7V Supply

Converting a negative signal (or one that's around ground) with an integrating A/D used to require both positive and negative supplies – a significant disadvantage for applications working off a single supply such as +5V DPMs, or battery powered +3V DVMs. MAX138 and MAX139, the new CMOS integrating A/Ds from Maxim solve this problem by including, on-chip, a voltage inverter that generates the negative supply voltage internally. These devices convert signals ranging from -2V to +2V, or -200mV to +200mV with a single +2.5V to +7V supply, while maintaining an incredibly low 200 μA of supply current.

Bandgap Reference

Unlike previous integrating A/D converters which use a zener reference, the MAX138/MAX139 use a bandgap reference that provides excellent long term stability and a maximum temperature coefficient of 100ppm/°C. Perhaps the most impor-

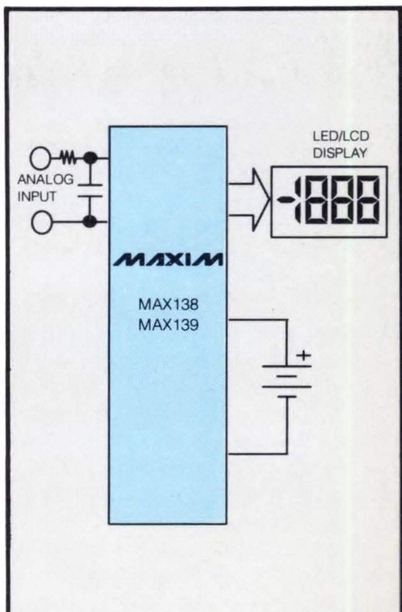


Figure 1.

(Please see 3 1/2 Digit A/Ds on back)

much more reliable than simple RC circuits. RC circuits work well if a change occurs abruptly between completely off and +5V. But if the power is applied slowly or lost, or if a brownout or momentary low occurs, they don't properly reset the system. The reset section in the MAX690 series contains a bandgap reference, a voltage divider that establishes the reset detection threshold, and a retriggerable monostable oscillator.

The voltage detector forces the Reset output low whenever the power supply voltage drops below the reset threshold. The circuit holds Reset low until the supply stays above the voltage detector threshold for the reset timing period, ensuring that the microprocessor receives the minimum reset pulse width specified by the manufacturer. The designer can extend this pulse width by adding a capacitor to the oscillator input or he can shorten it by overdriving the oscillator input. The voltage detector also serves a second purpose: forcing Chip Write Enable Output high whenever the power supply voltage input is too low.

Although the 4.65V threshold (MAX690/1/4/5) is a nominal value, the 4.5V minimum and 4.75V maximum are guaranteed because the thresholds are trimmed at the wafer level. A Low Line output offers an instantaneous view of the voltage detector status. The Reset output , however, goes high only after the input voltage has been at a valid level for the reset period.

Automatic Battery Switchover

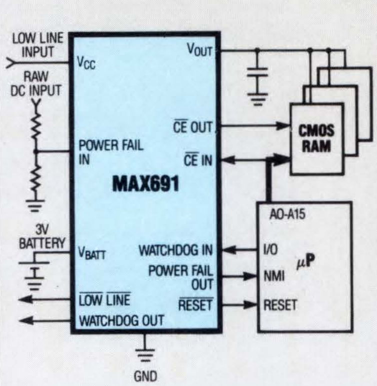
The battery-switchover circuitry, although shown in the block diagram as an SPDT switch, is more complicated than that. In practice, a voltage comparator checks V_{CC} against the battery voltage. As long as the supply is higher than the battery, V_{CC} is connected to the output terminal, V_{out}. This connection is made through a PNP transistor whose base drive modulation circuitry saturates the transistor while minimizing base current.

When V_{CC} falls to within 100mV of the battery voltage, the circuit turns off the base drive, and a 200ohm MOS switch connects the battery to V_{out}. With the MOS switch, the voltage drop is about 2mV at a 10µA current, compared to about 500mV across the diode switch used in a discrete circuit typically found in battery backup circuits.

With V_{CC} present, battery current is a maximum of ±1µA and is typically a 10nA charging current. This level extends battery life while remaining within the allowable charge current of even the smallest lithium batteries.

When V_{CC} falls to about 700mV below the battery voltage, a second comparator shuts down all circuitry not needed in the battery-backup mode. In this low-quiescent-current state, the typical drain on the battery is about 600nA, ensuring a long battery life.

The chip's Battery-On pin, which has a sink current of 25mA, indicates whether V_{CC} or the battery is powering V_{out}. It can be used directly to drive the base of an external PNP transistor if the power bus needs more than 50mA of output current during normal operation. An internal PNP transistor, meanwhile, is guaranteed to have a maximum voltage drop of 500mV at 50mA, a level that will power several CMOS RAMs.



Typical Application

Watchdog Timer

The third major section of the MAX690-697 chips is the watchdog timer, a function often desired but seldom found. This circuit monitors system execution, detecting hardware, and software faults. Because many µP systems can't strobe the watchdog timer, this chip automatically disables the timer if the Watchdog Input, WDI, is left floating. When that input floats, two internal resistors bias it at an invalid logic level detected by internal voltage comparators.

On the job, the microprocessor drives the WDI pin with an I/O line that is periodically strobed. At each strobe, the supervisory chip resets the timer. If the microprocessor fails to strobe WDI for the programmed time-out period, a watchdog fault occurs. Typical reasons for a failure to strobe include hardware problems, a temporary disruption caused by voltage transients, and software errors that put the microprocessor in an endless loop.

If a watchdog fault occurs, the chip sends a reset pulse and the Watchdog Output, WDO, goes low. The output remains low, and the chip periodically pulses the Reset line until WDI is again strobed.

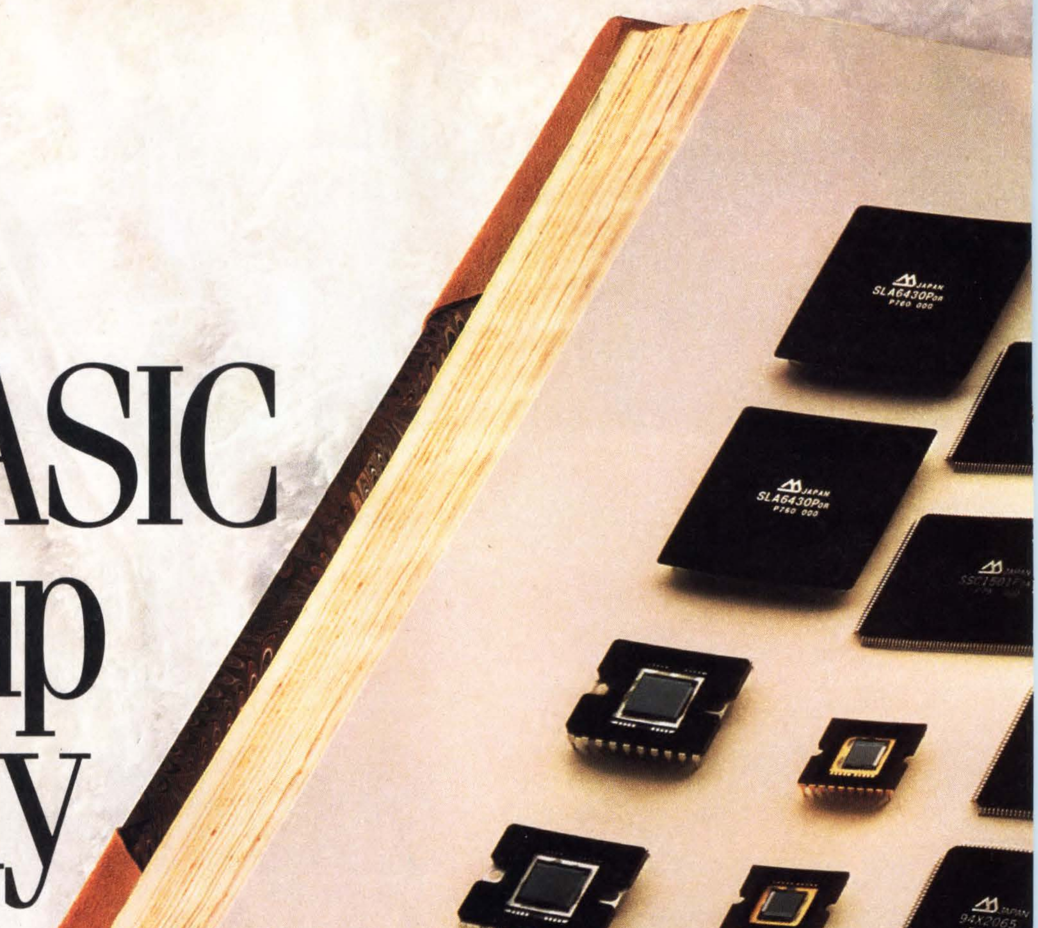
tant benefit of the bandgap reference and the internal voltage inverter is the ability to operate the MAX138/MAX139 with low supply voltages – down to +2.5V. This is a critical requirement for applications using two "AA" alkaline battery cells (or a single lithium cell) where the cell output will decrease with time from the fully charged value of +3V.

Upgrades 7106/36 and 7107/37

The MAX138/MAX139 are similar to Maxim's existing 3 1/2 digit A/D converters, 7106/36 and 7107/37. They use a dual slope integration technique to convert the differential input signal to a digital output (with a full scale of ±1999) that is ready to drive a multiplexed seven-segment LCD (MAX138) or LED (MAX139) display.

The MAX138/MAX139 use a voltage inverter similar to Maxim's 7660 to generate the internal negative supply. Since the voltage inverter requires two non-critical capacitors, the MAX138/MAX139 make use of the oscillator pins (38 to 40) of the 7106/36/07/37 for this purpose. This makes it possible to drop the MAX138/MAX139 into existing 7106/36/07/37 sockets by exchanging the two oscillator capacitors for two charge pump capacitors – a relatively minor change. Since the MAX138/MAX139 use an on-chip oscillator, the oscillator capacitors are no longer needed.

Our ASIC line-up is only half the story.



When it comes to delivery of high-quality, reliable ASICs, S-MOS wrote the book.

We did it in collaboration with our manufacturing affiliate, Seiko Epson. With 18 years of CMOS experience, Seiko Epson is one of the world's most advanced CMOS IC manufacturers.

Through Seiko Epson's high-yield manufacturing technology, we ship millions of ASIC units a month, and with a reject rate of less than .0001%. That's our quality story.

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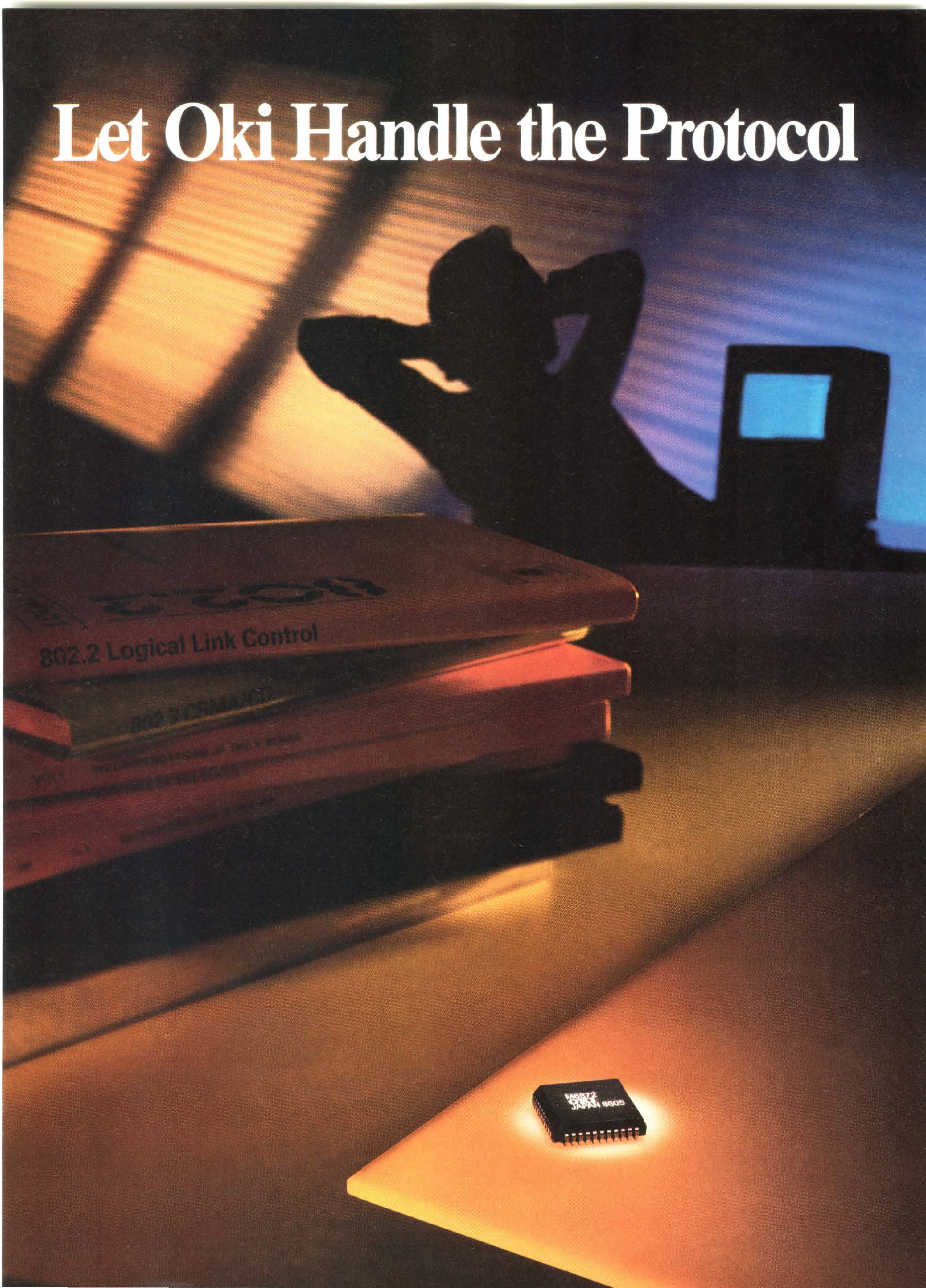
Up to 38,550 available gates ▪ SLA8000 (800 ps)*, 1.2μ drawn, 1.0μ Leff. ▪ SLA7000 (1.0 ns)*, 1.5μ drawn, 1.2μ Leff. ▪ SLA6000 (1.8 ns)*, 2.0μ drawn, 1.5μ Leff. ▪ SLA700B High Drive Output ▪ SLA100L Low Voltage	Complexities to 16K gates** ▪ SSC1000 (1.4 ns)*, 1.8μ drawn, 1.4μ Leff. ▪ Fully migratable from S-MOS gate arrays ▪ RAM and ROM blocks available	*The* Alternative to Full Custom ▪ 1.8μ CMOS process ▪ Can utilize dissimilar cell geometries ▪ 3-button approach to custom design ▪ Currently over 300 fully characterized cells ▪ Fast 14-week implementation time ▪ Timing-driven TANCELL® place-and-route software

TANCELL is a registered trademark of Tangent Systems.
*Typical propagation delay of 2-input NAND gate driving 2 internal loads with 1mm of interconnect.
**Maximum gate utilization depends on amount of interconnect used.

CIRCLE NO 90

S-MOS SYSTEMS

S-MOS SYSTEMS, INC.
2460 North First Street
San Jose, CA 95131-1002


Let Oki Handle the Protocol
802.2 Logical Link Control

Oki's new PSCC provides automatic support for protocols—together with great networking flexibility

The new Protocol Serial Communications Controller (PSCC) from Oki Semiconductor is a highly innovative VLSI device which automatically supports LAPB and LAPD HDLC protocols and saves you from having to program and manage them. With a speed of 10 Mb/s, the PSCC also gives you great networking flexibility.

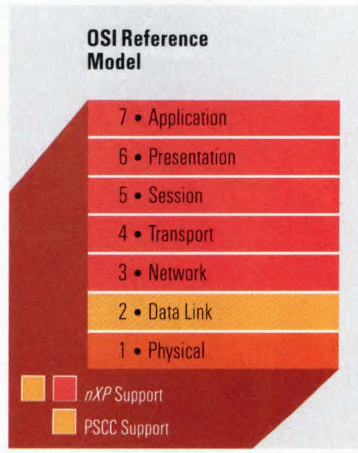
Integrated functions

The PSCC combines a full-duplex HDLC channel, on-board DMA controller, and 520 bytes of internal RAM. It allows you to send and receive messages directly from memory and frees system intelligence for higher level functions. It automatically supports the update and comparison of state variables for multiframe transmission. In addition, the PSCC supports collision and priority detection.

For even greater integration, the PSCC will be imbedded in Oki's high-performance 16-bit *nXP* microcontroller which will support all seven OSI levels of the ISDN.

Great flexibility

Easy interface is provided to standard 16-bit CPUs and to multiplexed buses. The PSCC can be easily customized to support different serial communications protocols. The high speed of the PSCC allows you to create a small inexpensive network, then to expand to a LAN, and later move into ISDN—all supported by Oki.



You can count on Oki

The PSCC is only one of the ways Oki can save you time and help you realize competitive advantages. You can also count on Oki for extensive experience, creative solutions, and proven reliability in every aspect of semiconductor device design and manufacturing. We invite you to put the full resources of Oki Semiconductor to work for you.

Automatic protocol support from Oki.

☐ Please send the complete technical data package on the MSM6872, the first member of Oki's Protocol Serial Communications Controller (PSCC) family.

☐ Please call. We have immediate requirements.

( )
Phone

Name

Title

Company

Attach coupon to business card or letterhead and return to: PSCC Customer Service, Oki Semiconductor, 785 North Mary Avenue, Sunnyvale, CA 94086. Phone: (408) 720-1900.

EDN102788

OKI
SEMICONDUCTOR

CIRCLE NO 92

This chip enabled us to process signals of the past.

The Rosetta Stone, discovered in 1799, was the key to deciphering the hieroglyphics that had been incomprehensible for centuries.

Signal processing, when you come right down to it, is multiplication, addition, subtraction and storage. Doesn't sound very exciting.

But put together a set of building blocks that do those simple operations with almost unimaginable digital speed and precision. Then add A/D converters that bring in information from the world around you. Plus D/A converters that restore the digitally processed signals to a form your senses can understand.

And you've built a signal processing system that will enable you to do things that couldn't be done before, see things that couldn't be seen before and understand things that could never be understood before.

That's exciting. And we can help make it happen.

Complete systems solutions.

Our approach to signal processing is simple.

We've taken our unparalleled experience in data conversion and added to it a set of signal processing chips that perform operations that used to require entire circuit boards.

Here's a sample of what they can do for you:

ISP 9110 12-Bit Microprogram Sequencer: expanded 33 word stack, 50 ns minimum cycle time.

ISP 9119 FIFO RAM Controller: uses standard RAMs to build FIFOs up to 64K deep, 15 MHz operation.

ISP 9128 FIR Filter Controller: implements 16-bit filters to 128 Taps, 128 Tap sampling rate of 100kHz.

ISP 9210 16x16 Multiplier Accumulator: innovative high-speed architecture (65 ns commercial, 75 ns military), low-power operation.

ISP 9216 16x16 Multiplier: low-power, industry-standard compatible to AM29516 and MPY016.

ISP 9520/21 Pipeline Register: high-speed access,

These are the chips you need to process signals of the future.

Our DSP building blocks, combined with our data conversion know-how, will help you design systems that depict reality more clearly than ever before possible.

output selectable from any register.

With devices like these, we can give you a total integrated signal processing solution. Plus the added benefits of single-vendor support and package pricing.

Position yourself for the future.

Signal processing is changing every day.

That's why you need more than a signal processing supplier who has a few good parts.

You need a long-term partner who has a commitment to signal processing, and the resources in every area that signal processing calls upon.

For example, the chips of tomorrow will very likely combine signal processing, data conversion and high-speed logic. When you work with us, you'll get our Intersil expertise in processing and conversion. Plus our RCA Advanced CMOS Logic capabilities. Plus the more than 20 years of GE experience in radar, sonar, medical imaging and other demanding DSP applications.

If worries about complexity and cost have deterred you from taking the exciting step into digital signal processing, call us. Together, we'll step into the future.

For more information, contact your local GE Solid State sales office or distributor. Or call toll-free, 800-443-7364, extension 30.

In Europe, call: Brussels, (02)246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

General Electric Company, U.S.A.

GE/RCA/INTERSIL
SEMICONDUCTORS

CALENDAR

Seminar on DOD-STD-2167A & 2168, Washington, DC. DOD Software Seminars, c/o David Maibor Associates, Box 846, Needham Heights, MA 02194. (617) 449-6554. October 24 to 25.

OEM Peripheral Invitational Computer Conference (ICC), Westlake Village, CA. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 25.

11th Annual Newport Conference on Fiberoptics Markets, Newport, RI. Kessler Marketing Intelligence, America's Cup Ave at 31 Bridge St, Newport, RI 02840. (401) 849-6771. October 25 to 26.

Seminar on DOD-STD-2167A & 2168, Boston, MA. DOD Software Seminars, c/o David Maibor Associates, Box 846, Needham Heights, MA 02194. (617) 449-6554. October 27 to 28.

11th Northeast Computer Faire, Boston, MA. The Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. October 27 to 29.

ICALEO '88 (International Congress on Applications of Lasers and Electro-Optics), Santa Clara, CA. The Laser Applications Congress, 5151 Monroe St, Suite 102W, Toledo, OH 43623. (419) 882-8706. October 30 to November 4.

Seminar on DOD-STD-2167A & 2168, Orlando, FL. DOD Software Seminars, c/o David Maibor Associates, Box 846, Needham Heights, MA 02194. (617) 449-6554. October 31 to November 1.

Unix Expo (Unix Operating System Exposition and Congress, New York, NY. National Expositions, 15 W 39th St, New York, NY 10018. (212) 391-9111. October 31 to November 2.

CALENDAR

CASE for Data Modeling (seminar), New York, NY. Technology Transfer Institute, 741 Tenth St, Santa Monica, CA 90402. (213) 394-8305. November 2 to 4.

Seminar on DOD-STD-2167A & 2168, San Diego, CA. DOD Software Seminars, c/o David Maibor Associates, Box 846, Needham Heights, MA 02194. (617) 449-6554. November 3 to 4.

1988 IEEE GaAs IC Symposium, Thousand Oaks, CA. John Selin, registration chairman, Raytheon Co, Equipment Div, MS E21, 430 Boston Post Rd, Wayland, MA 01778. (617) 440-5532. November 6 to 9.

GOMAC '88 (Government Microcircuits Applications Conference), Las Vegas, NV. Palisades Institute for Research Services, 201 Varick St, Rm 1140, New York, NY 10014. November 8 to 10.

Electronica, Munich, West Germany. Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. November 8 to 12.

IEEE 1988 Nuclear Science Symposium, Orlando, FL. E Barsotti, Fermilab, MS 222, Box 500, Batavia, IL 60510. (312) 840-4061. November 9 to 11.

CASE Benchmarks: A Product Comparison Seminar, Denver, CO. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. November 14 to 16.

Expert Systems: An Intensive Seminar on Choosing Applications and Tools, Chicago, IL. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. November 14 to 16.

CASE and the Real World (seminar), Boston, MA. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. November 15 to 16.

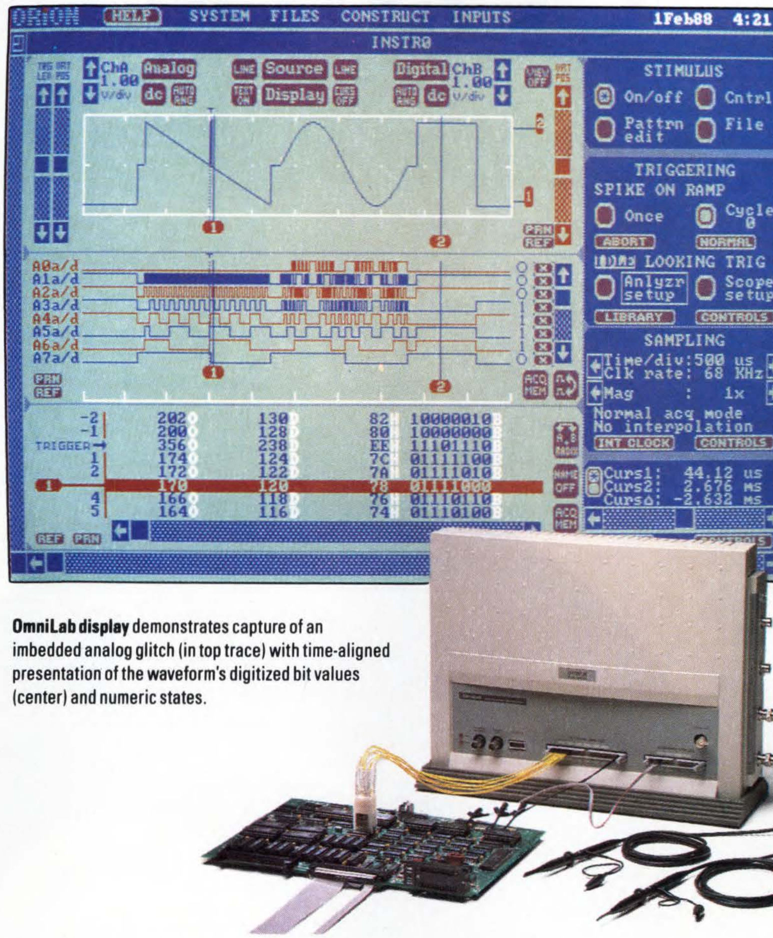
Introducing OmniLab 9240.
Totally Integrated Scope-Analyzer-Stimulus.

■ Combine a 100 MHz digital oscilloscope with a time-aligned, 200 MS/s 48-channel logic analyzer. Next add synchronized analog **and** digital stimulus generators. Then a remarkable new triggering system. What you have is the 9240 — a whole **new class** of instrumentation. Expressly designed to speed challenging analog and digital analysis. And get you from concept to product faster.

■ The 9240 is based on an innovative new instrument architecture that merges high-speed universal hardware and seamlessly-integrated software to create high-performance capabilities not available in separate instruments. Analog and digital traces are always time-correlated in a unique, single screen display. SELECT™ triggering bridges scope and analyzer techniques. And OmniLab's stimulus generators can playback captured or edited signals.

■ At the heart of the 9240 is SELECT triggering, the most straightforward and complete solution **ever** to triggering dilemmas. It's one system, operating with synchronized analog and digital views of your data. By combining conventional oscilloscope and analyzer triggering with powerful RAM truth tables — plus min/max time qualification as needed — SELECT triggering helps you analyze hardware, debug software, and integrate systems more easily.

■ OmniLab™ is a generation ahead of conventional digital scopes that often hide rarely occurring faults because they only show you a few cycles out of millions. With its continuous monitoring, you can use SELECT triggering to quickly catch every occurrence of rare events like metastable states, bus contentions, missing pulses, and buried noise glitches.



OmniLab display demonstrates capture of an imbedded analog glitch (in top trace) with time-aligned presentation of the waveform's digitized bit values (center) and numeric states.

■ The 9240 is like having a complete benchtop of instruments integrated with your PC/AT or compatible. Which you can easily customize for digital development, analog development, or a combination of both.

■ With OmniLab, your productivity will soar. Because you achieve results with fewer instruments. And in fewer steps than ever before. By no means least, the 9240 delivers the best price/performance you'll find anywhere, costing just $8900 fully outfitted. And most importantly, without compromising a single high-performance spec. Not a one.

NO-COMPROMISE 9240 SPECIFICATIONS

DIGITAL OSCILLOSCOPE		LOGIC ANALYZER	
Digitizers:	Two, 8 bit	Inputs:	48, timing and state
Bandwidth:	100 MHz	Asynchronous Clocking:	34 MS/s on 48 inputs; 204 MS/s on 8 inputs
Single-Shot Digitizing:	34 S/s to 204 MS/s		
Repetitive Sampling:	680 MS/s	Repetitive Sampling:	680 MS/s on 48 inputs
Scale Factor:	5 mV/div to 10V/div in 1-2-5 sequence	Synchronous Clocking:	0 to 34 MS/s
		Acquisition Memory:	4K samples (16K, 64K optional)
Record Length:	4K (16K, 64K optional)	Disassembly Options:	Over 150 microprocessors
ANALOG STIMULUS		**DIGITAL STIMULUS**	
Output:	8mV to 8 V peak-to-peak, 8 bit	Outputs:	24, 74F tri-state drivers
Cycle Length:	4 to 4K samples (16K optional)	Cycle Length:	4 to 4K samples (16K optional)
Clocking:	34 S/s to 34 MS/s	Timing:	34S/s to 34MS/s
Functions:	Record, edit and playback	Functions:	Record, edit and playback

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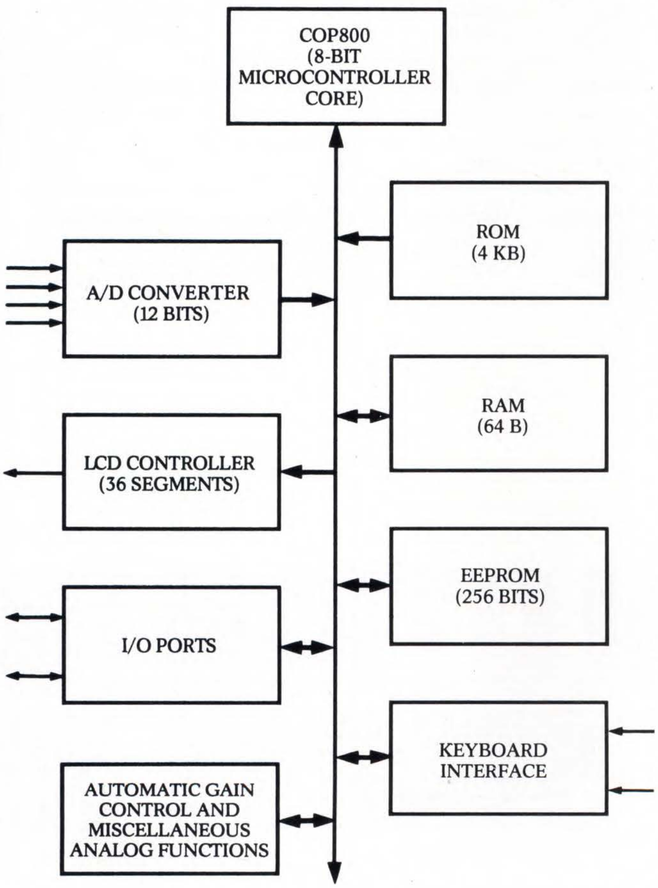
CIRCLE NO 242

E^2/DIGITAL/ANALOG. COMBINATION Y

THE TECHNOLOGY OU CAN BANK ON.

To be perfectly honest, we didn't invent the concept that says high integration equals high profit. But as you can see from the application diagram on this page, we definitely perfected it. With our Triple Technology,™ a process that allows you to combine E^2, digital, and analog functions on the same chip. And, create higher levels of integration than ever before.



Single chip measurement and control system, integrating several EEPROM, analog, and digital functions.

In this case, our customer's last product was a medical instrument the size of a paperback, with 70 different components. By combining a sophisticated 8-bit controller, RAM, ROM, A/D converter, and 256 bytes of EEPROM on the same chip, we helped them shrink the same instrument to the size of a matchbox. And cut the costs just as dramatically.

As a result, they have a product that sets new standards for the industry. And for their shareholders. And by working closely with their designers, we were able to create this one-chip solution with standard cells from our library. In fact, our customer only had to design about 200 gates of logic using our standard digital cells.

Turnaround time from code to first silicon was only 18 weeks. And because of our development tools and mixed-mode simulation (MIXsim™), the first prototypes worked.

Of course, this is only one example. With 250 digital, 50 analog, and over 20 EEPROM cells in our library, we can create literally thousands of combinations. Including Analog/E^2, E^2/Digital, Analog/Digital, and E^2/Analog/Digital. For every application you can imagine. And we can execute them all in high performance CMOS.

So, no matter what you're designing, call or write for our complete library card. And we'll show you a combination you can always bank on. Your ideas and our technology.

Sierra Semiconductor
Triple Technology.™ In CMOS.

2075 North Capitol Avenue, San Jose, California 95132. Telephone (408) 263-9300

CIRCLE NO 94

	AD840	AD841	AD842	AD843	AD844
Gain Bandwidth Min Stable Gain	400MHz 10	40MHz Unity	80MHz 2	35MHz Unity	60 to 430MHz Unity
Settling Time (10V Step)	100ns to 0.01%	110ns to 0.01%	100ns to 0.01%	110ns to 0.01%	100ns to 0.05%
Slew Rate	400V/μs	300V/μs	375V/μs	300V/μs	to 2,000V/μs
Quiescent Current (max)	12mA	12mA	14mA	12mA	6.5mA
Comments	HA2540 Improved Replacement	50mA min Output Current	100mA min Output Current	FET-Input, Replaces FET- Input Hybrids	Current Feedback, $2nV/\sqrt{Hz}$ Noise at 1kHz

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High Speed Op Amp Selection Guide

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AD845	AD846	AD847	AD848	AD849	
16MHz Unity	46 to 600MHz Unity	50MHz Unity	175MHz 5	750MHz 25	Gain Bandwidth Min Stable Gain
350ns to 0.01%	100ns to 0.01%	120ns to 0.1%	100ns to 0.1%	80ns to 0.1%	Settling Time (10V Step)
100V/µs	450V/µs	300V/µs	300V/µs	300V/µs	Slew Rate
12mA	6mA	5.7mA	5.7mA	5.7mA	Quiescent Current (max)
FET-Input, Drives Cap Loads	Current Feedback, 75µV max Offset Voltage	Excellent Flash ADC Buffer	Stable into any Cap Load	Low Noise Pre-Amp	Comments

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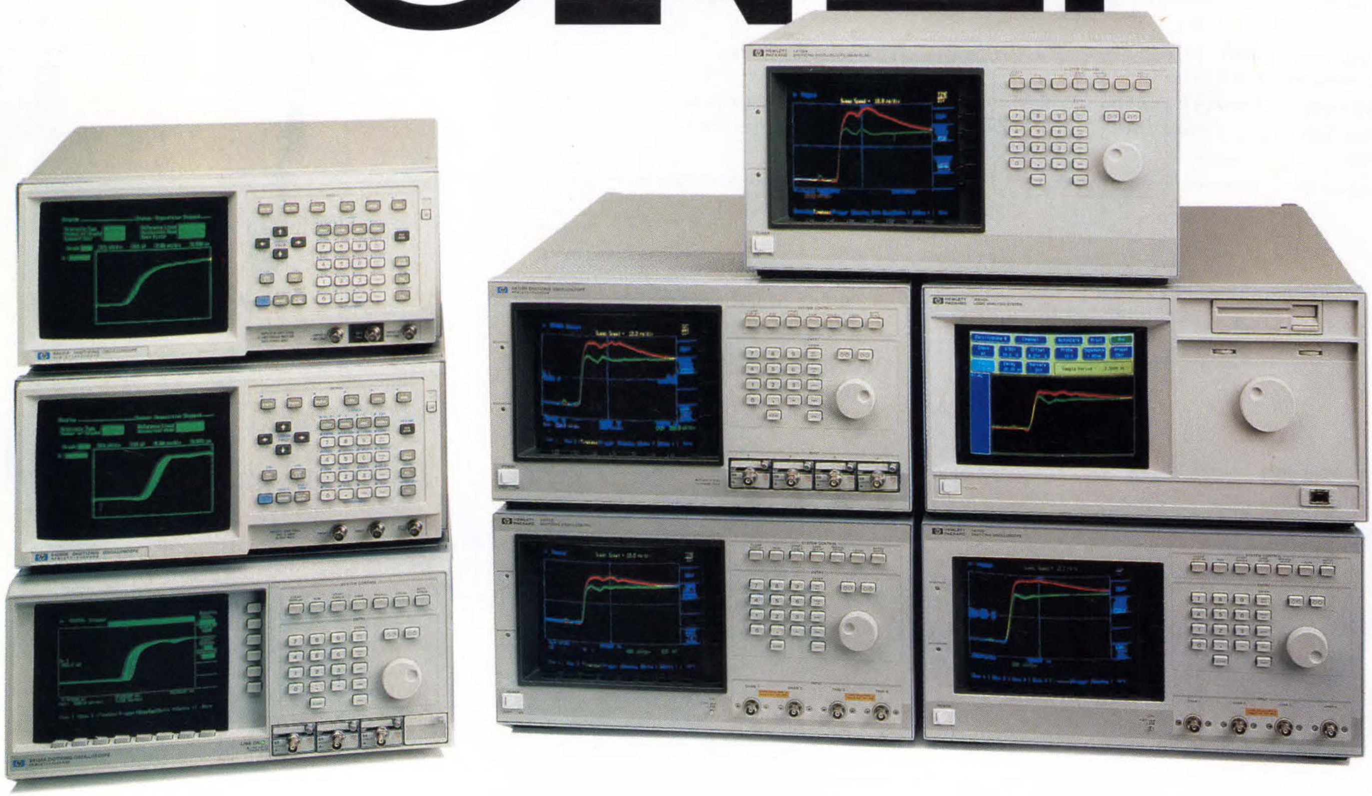

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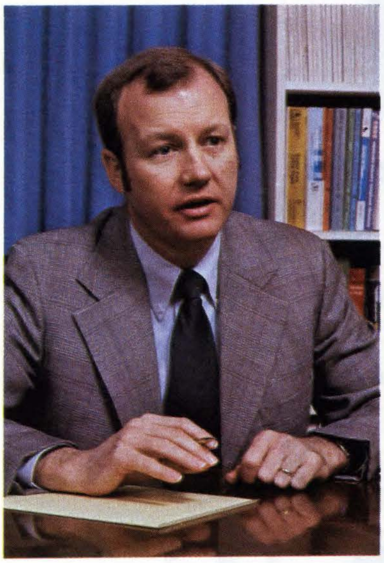
Send alien graduates home



Assuming that a foreigner has sufficient money and ability, it's not difficult for him or her to get a college or university education in the USA. Student visas are fairly easy to obtain, and, as long as a student maintains good grades, he or she can remain in the US on a student visa. After graduating, however, many of those foreigners stay in the US by taking permanent jobs. Once employed, they can ask the Immigration and Naturalization Service to change their status from student to immigrant. According to the National Science Foundation, about 4% of the engineers in our profession are not US citizens.

Many people have proposed that aliens go home after graduation rather than taking jobs that US engineers could fill. Foreign graduates, it is said, often work for less than their US counterparts, thus "busting" or lowering the wages paid for the job. Although that issue deserves a thorough airing, there's another reason that foreign graduates should return home. Simply put, their countries need them. All too often, foreign students come to the US to study a subject that will let them get a job in the US after they graduate. In fact, there may be no market at home for the skills they learn in the US.

Frankly, having foreign students study in the US is a good investment. Getting a quality education and learning how other people work and live benefits us all in the long term. However, foreign students who train in our schools owe their countries a debt. So, they should study a subject that benefits their home economy. Knowing that they would be required to return home for two or three years before emigrating to the US might push many young foreigners to study civil engineering instead of electrical engineering, or food science instead of computer science.

During the summer, my family and I visited a developing country that benefits from abundant year-round sunshine and an almost constant on-shore breeze. Yet most of the hot water is heated by electricity, and all the electricity is generated by burning oil. The country isn't poor—average per capita income is about $9000—but it isn't rich enough to throw away energy so wastefully. I was left wondering why no one had tackled solar- and wind-energy problems. It may be that the smart young people were in the US working as engineers and sending money to the folks at home.

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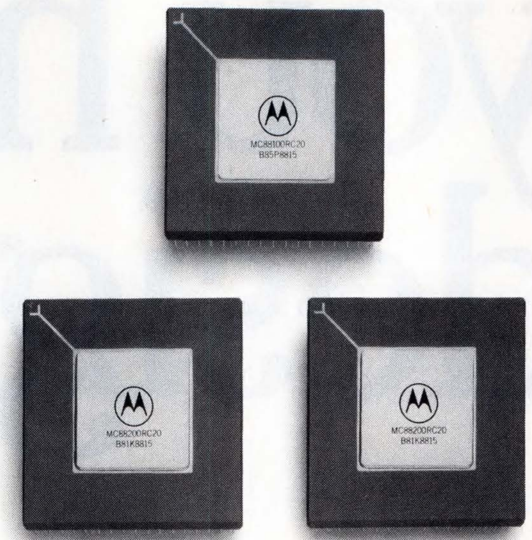

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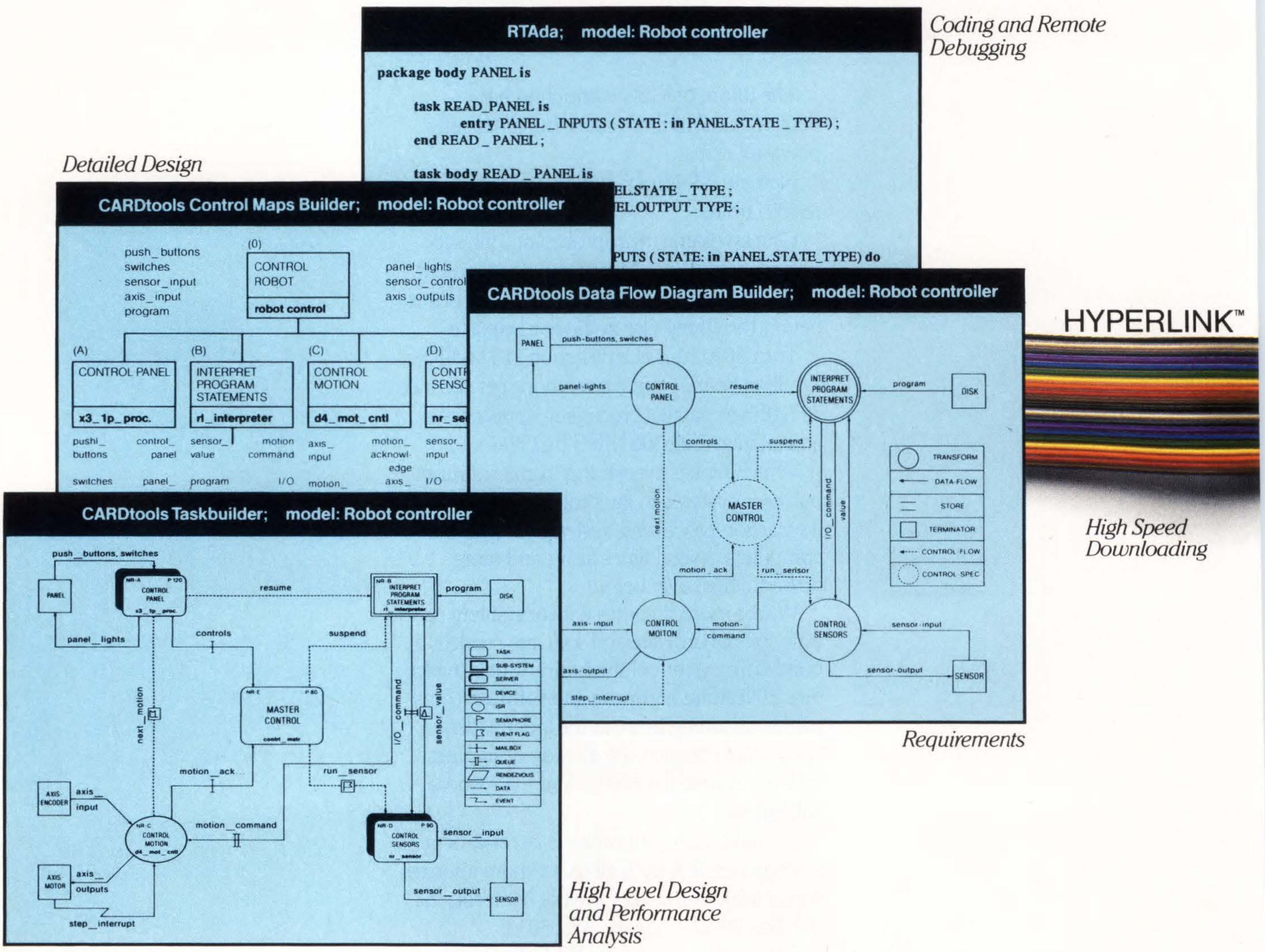

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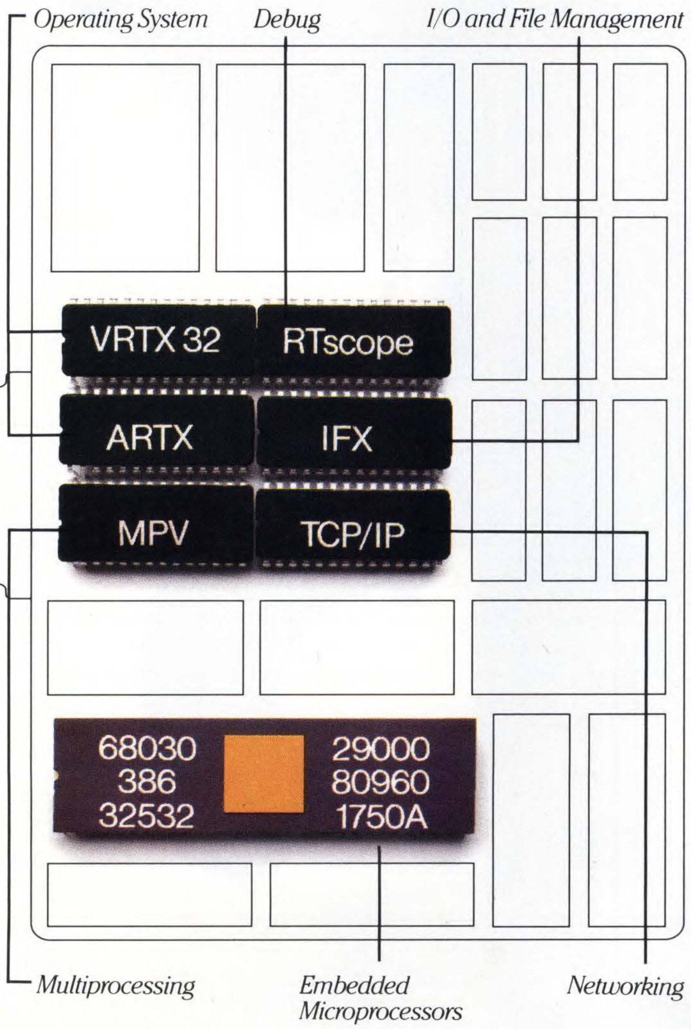

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READY SYSTEMS

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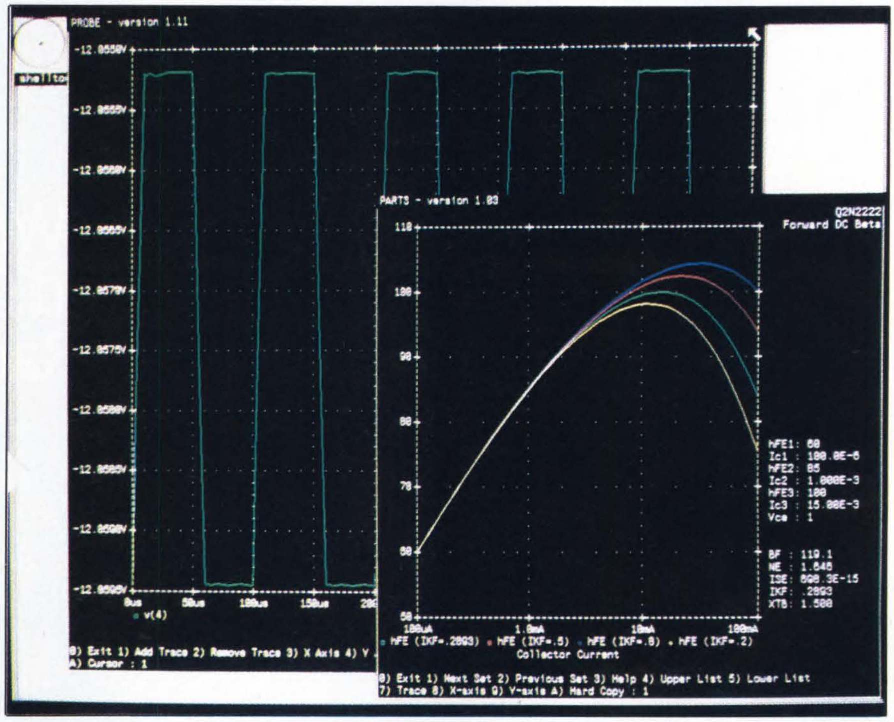
Interactive simulation packages prove faster and more versatile than ever

Chris Terry, *Associate Editor*



Interactive analog simulators, *such as PSpice from Microsim Corp, let you see the results of changes in circuit parameters immediately.*

Computer-simulation software has seen both quantitative and qualitative changes in recent years. The quantitative changes include both faster execution and wider distribution: The relatively low cost and vastly increased computing power of workstations, many of which include floating-point hardware accelerators, have brought fast simulation capabilities out of the mainframe computer room and onto almost every engineer's desktop.

Even more important are the qualitative changes, which came about because of the startling growth and power of graphics capabilities. It is these graphics capabilities, above all, that let simulation aid the engineer in all phases of hardware design and software design and development. You no longer have to submit a simulation as a batch job and wait for numeric results. Current software packages, which combine graphics with incremental compilation techniques, allow you to see right on the screen how a model behaves. You can stop the simulation, change the properties of the model by entering new parameters from the keyboard, and then immediately restart the run or continue it from where you left off.

Simulation can drastically reduce the cost of developing a new system in several ways. If you're developing a custom IC, for example, simulation will help you to eliminate logic errors and timing glitches from your design before you get to the expensive stage of photoplotting, and the even more expensive stage of obtaining prototype parts from the foundry. Likewise, if you are developing an embedded system based on a new or unfamiliar CPU architecture, a simulator that can execute the instruction set of the CPU will allow you to start developing software for the new system before the hardware is complete. It may even reveal potential problems with the hardware and allow the hardware designer to make the necessary modifications at an early stage.

Analog simulators are mature

Simulators for hardware design fall into three main classes: analog, mixed-mode (which simulate digital circuits at the board, gate, or switch level), and multimode (which simulate boards containing both analog and digital circuits). Note that some vendors use the term "mixed-mode" to refer to simulators that handle both digital and analog circuits. Here, "mixed-mode" will be restricted to the definition above.

A notable characteristic of most of the currently available simulators is that they're compatible with other CAE tools from the same vendor, and they may also have the ability to exchange data with tools from other vendors via EDIF or other interchange standards.

Analog simulators were the first to appear; perhaps the best known analog simulator is the Spice program, which was originally developed at the University of California at Berkeley to run on VAX computers. Now MicroSim supplies versions of PSpice that run on a wide variety of machines, including the Macintosh II. Prices range from $950 for the IBM PC version to $11,600 for the large-VAX version. Spice is not particularly easy for a

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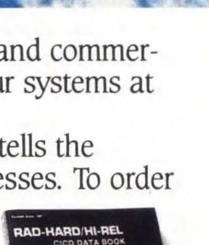

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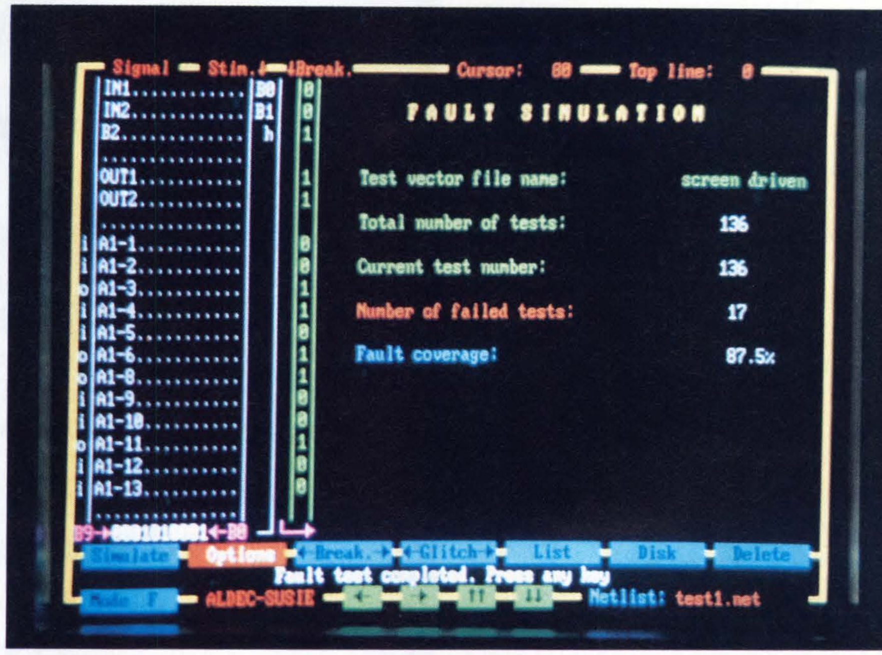
beginner to use, because you have to learn a special language for defining the characteristics of the components contained in your circuit; however, the program is very flexible and can handle dc operation, transfer functions, transient response, distortion analysis, frequency response, and many nonlinear functions. A Monte Carlo option also lets you perform worst-case analysis on complex circuits.

Another widely used analog simulator is the $9000 Touchstone from EEsof. This package will be of particular interest to microwave designers, because the latest version (1.6) includes a large number of microwave/RF element models, as well as a Monte Carlo yield-analysis program that can project the manufacturing yield of microwave/RF circuits. The program emphasizes the optimization of your circuit; the optimizer techniques include quasi-Newton, least p*th*, minimax, and random maximization. Touchstone is part of a family of microwave/RF design tools that includes foundry libraries, network- and filter-synthesis tools, a harmonic-balance simulator, and tools for layout and artwork control.

Somewhat less expensive is the $495 Analog Simulator from Visionics, which runs on IBM PCs and compatibles. Analog Simulator is part of the vendor's EE Designer toolset, and it takes its input from the schematic-capture module. The simulator has two distinct modules: one for nonlinear dc simulation, the other for frequency-domain ac simulation. You can simulate as many as 50 nodes simultaneously. The libraries of modeled components that come with the simulator include inductors, resistors, transistors, op amps, and voltage sources. Note that the program can't stand alone: You need EE Designer 1.7 or EE Designer II 2.03 in order to access the simulator and to specify the nodes to be simulated.

For those who want an inexpensive tool for learning about analog simulation, Tatum Labs offers EC-Ace, which is a subset of the company's ECA-2 analog-circuit simulator. EC-Ace runs on IBM PCs and compatibles and costs $145; it can handle as many as 100 components, and provides sine, pulse, pulse-width-linear, swept-frequency frequency-moulation, and exponential transient signal generators. You can use the program in either batch or interactive mode. The vendor claims it runs at least twice as fast as Spice does.



***Digital simulators** (such as this one from Aldec) may include built-in or optional fault simulators that indicate which pins of an IC fail the tests applied.*

Logic simulators

When ICs embodied only a few transistors (as in the 7400 Series and similar SSI chips), manufacturers were able to use Spice to simulate logic circuits and even complete boards. However, as VLSI and ASIC chips became more complex, simulation at the switch (transistor) level became impractical—simulators such as Spice ran far too slowly when handling thousands (instead of tens) of nodes. It was vital to have some means of simulating the behavior of a design (you can't breadboard an ASIC or PLD) to avoid costly logic errors or unforeseen interactions and timing glitches. Chip foundries developed gate-level simulators to cope with this situation; the first examples operated only in batch mode on a mainframe; their input was a net list extracted from the schematic captured by a CAD program.

On a time-sharing mainframe, it was certainly hours (and sometimes days) before the simulation results came back to the design engineer. CAE vendors, therefore, began developing their own interactive simulators that would run on the same workstations as their schematic-capture and board-layout tools. This integration of schematic-capture, simulation, and board-layout modules as a complete tool set not only allowed each tool to be interactive, but also provided communication between the modules, so that, at any stage, an engineering change would be reflected in all the relevant files. As the logic simulators matured, their scope widened to allow the behavioral ("black-box") simulation of a complete board, the gate-level simulation of individual VLSI chips, or the switch-level simulation of functional blocks within a chip.

Typical of these advanced simulators is the Daisy Logic Simulator (DLS), which shares common component libraries and a common database with other tools from the vendor, such as the Daisy Timing Verifier (DTV), which comes bundled with DLS for $24,000 and runs on Daisy and Sun 386i workstations. At the switch level, DLS lets you examine transistor action and timing in critical portions of your design. At the gate level, you can specify the primitive forms of Boolean functions (AND, OR, NAND, NOR, XOR, XNOR, and NOT). At the functional level, you can specify a complex Boolean expression instead of using lengthy gate-level descriptions; DLS performs logic minimization on your expression and uses the timing characteristics of the most appropriate models in its library for the simulation. At the behavioral level, you can specify a "black box" model in terms of a special behavioral specification language; this mode of operation lets you simulate very complex logic and verify the critical timings.

This microwave/RF simulator *from EEsof Inc runs on IBM PCs and compatibles and handles striplines as well as networks.*

A logic simulator that has some unusual features is the $995 Susie (Standard Universal Simulator for Improved Engineering), which runs on IBM PCs and compatibles. First, it is based on an incremental compiler, so you can load new JEDEC fuse maps for PLDs during the simulation without having to recompile the simulation model. This program provides three simulation modes: a high-resolution, 10-psec mode; an automatic glitch-detection mode; and a mode with unit propagation delays. You can change modes on the fly, and you can resimulate any previous cycle in the new mode. Because the program is designed for board-level simulation, you can simulate multiple PLDs together with microprocessors and glue logic (many PLD-design tools handle only single-chip designs). To speed up processing, the program automatically identifies all timing problems in the complete design and lets you limit subsequent simulations to sections of the design in which timing problems exist. In addition, you can have Susie automatically break your design into several parts for concurrent fault simulation on as many as eight separate PCs. The fault simulator (PAFS) comes as a $1950 option to Susie and processes 256,000 AND/OR gates per second on an IBM PC/AT.

Another low-cost PC-based tool is the $950 GateSim offered by Tanner Research. This program allows you to simulate a design that has about 7000 gates on a PC/XT; if you have a PC/AT, the virtual protected mode allows you to access 16M bytes of memory and simulate a design with as many as 250,000 gates. Because the program is written in assembly language, it's very fast; according to the vendor, a 5000-gate design with a 2000-vector test suite finishes in 10 minutes on a 10-MHz PC/AT.

Traditionally, analog circuits and digital circuits have been handled quite separately for simulation purposes, because of their very different characteristics. At present, however, it's no longer possible to make this rigid distinction. At the board level, for example, a digitally controlled adaptive filter has both digital and analog circuits that interact with each other. The mixture is starting to occur also at the chip level; a surprising number of ASICs and custom chips contain both digital and analog blocks. If you have access to both a digital simulator and an analog simulator, you can run separate simulations for each portion of the system, but that procedure is far from satisfactory, because the actual hardware may exhibit interactions that neither simulator picks up.

According to David Smith, vice president of engineering at Analogy Inc, the optimum solution is to combine the matrix techniques of an analog simulator with an event-driven digital simulator **(Ref 1)**. Because not all of a digital circuit is active at once, the simulator can

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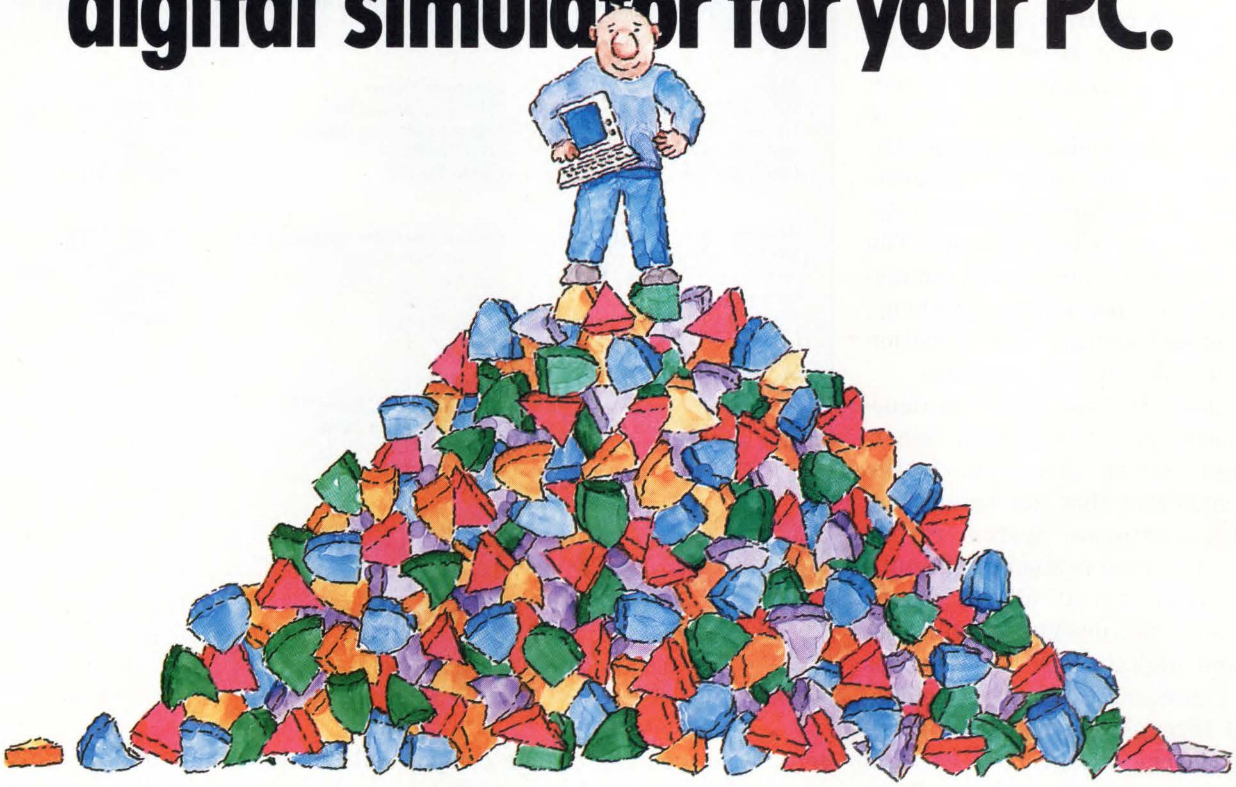

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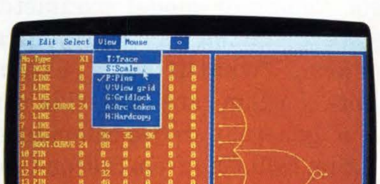

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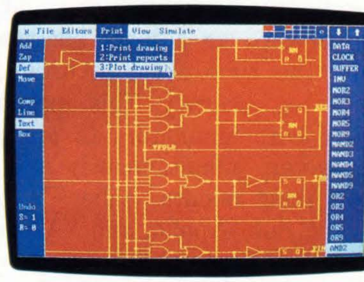

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make use of an event queue, which speeds up the simulation because the simulator does not have to deal with inactive circuit elements. The two simulators should run concurrently, each controlling the other's progress in time. However, combining the two techniques poses a number of problems, not the least of which is the modeling language: Users shouldn't be forced to describe counters in analog terms or to describe op amps in digital terms. The most advanced multimode simulators resolve most of these problems, and several provide fast execution and a consistent user interface.

Analogy Inc and HHB Systems Inc have jointly developed Saber/CADAT, which they claim is the first simulator that can simulate an entire multimode system rather than only small segments of multimode circuitry. It allows you to simulate ASIC designs for both analog and digital elements in modes that represent the lowest (component) through the highest (behavioral) levels. A special algorithm (the Calaveras algorithm) allows Saber to take optimum time steps until a digital event requires analog simulation processing; Saber then re-evaluates its solution and continues forward or adjusts backward along the time scale in order to guarantee accuracy. This approach allows both simulators to analyze the system simultaneously and to share their results. Saber/CADAT runs on Sun, Apollo, and VAX machines and starts at $35,000.

A slightly less expensive multimode simulator ($20,000) is Simucad's PacSim. The latest release (2A.4) provides a conditional-termination feature, which allows the simulation to terminate when a specified event occurs, instead of running for a fixed length of time. You can use this feature to help you analyze the results more quickly. The stop/start feature ensures that you can save circuit states during simulation and restart from any saved state instead of from time zero. Also, you can change component values or model parameters before restarting, so that you can perform "what-if . . ." experiments. PacSim runs on a wide variety of general-purpose computers.

LSim ($49,000) from Silicon Compiler Systems runs on Apollo, Sun, and MicroVAX machines. You can use it as a stand-alone tool or as part of the vendor's Generator Development Toolset. This simulator is based on an extensible set of simulation algorithms, all of which share a common infrastructure; thus, you can combine all the commonly recognized levels of simulation for the blocks that make up your IC design. You can even alternate between simulation levels at specific time points during the simulation. The modeling language is a superset of the C programming language, so users who are familiar with C can quickly learn to exploit all of LSim's features.

One advantage of LSim for analog simulation is a circuit-simulation algorithm that makes voltage, rather than time, the independent variable. Because Spice uses time, the analysis matrix grows as the square of the number of nodes in the circuit. The LSim simulator, on the other hand, only has to re-evaluate nodes that are changing from one voltage to another, so that the simulation time grows at a slower rate than the number of nodes. LSim also provides you with a choice of fault-simulation modes, including a statistical fault-analysis algorithm that greatly reduces the time needed to generate a fault-coverage estimate. EDN

For more information . . .

For more information on the interactive simulators discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Circle No 715

Visionics Corp
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References

1. Smith, David, *Mixed Analog/Digital Simulation*, Analogy Inc, April 1988.

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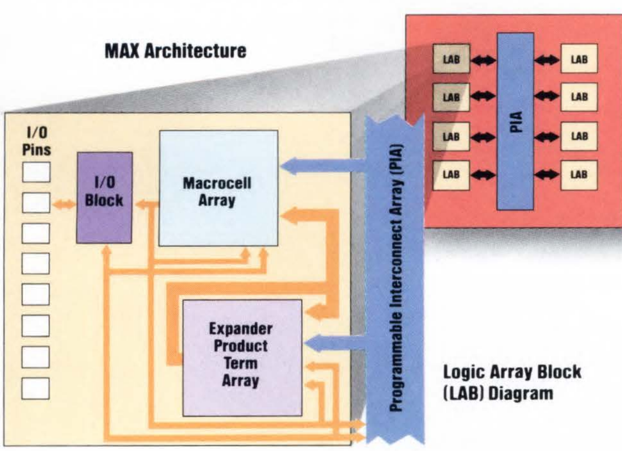


At the highest densities, MAX incorporates a Programmable Interconnect Array that lets you connect all your logic without routing bottlenecks. The result is high array density with small array performance.


Get ready to can the idea
EPLDs can't be dense.
SARDI

Now you can pack the functions of 50 TTL devices on a single MAX family EPLD.

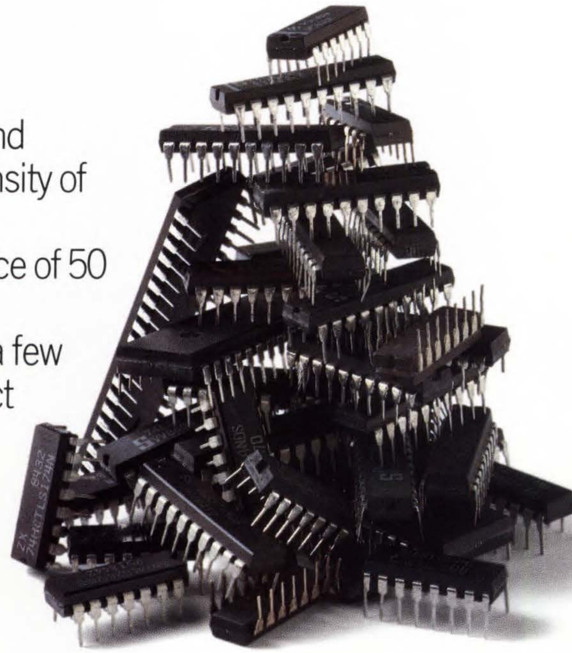
The key to MAX is density and speed combined.

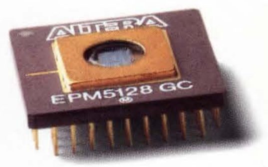
But first, let's do a little cramming on density.

Because of its streamlined logic array blocks, PIA and advanced process, MAX delivers three times the density of the largest conventional EPLDs.

For instance, the MAX EPM5128 can take the place of 50 or more TTL devices. Or 20 plus PALs.®

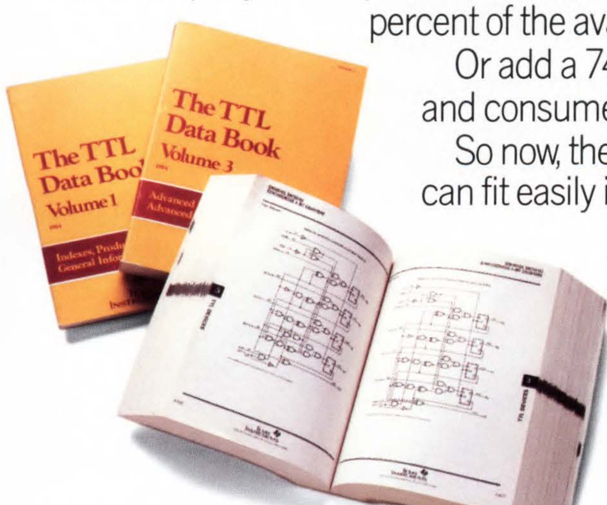
In fact, you can put the entire TTL Data Book on a few MAX EPLDs. Because MAX can accommodate exact functional equivalents of all popular 7400 type MSI and SSI standard-logic parts.





Which means you can still design by The Book, while enjoying all the benefits of user-configurable logic. Plus you get the simplicity of using just a few MAX devices in place of hundreds and hundreds of TTL part numbers.

For example, you can place a 74161 counter in the EPM5128. And take up only three percent of the available space.

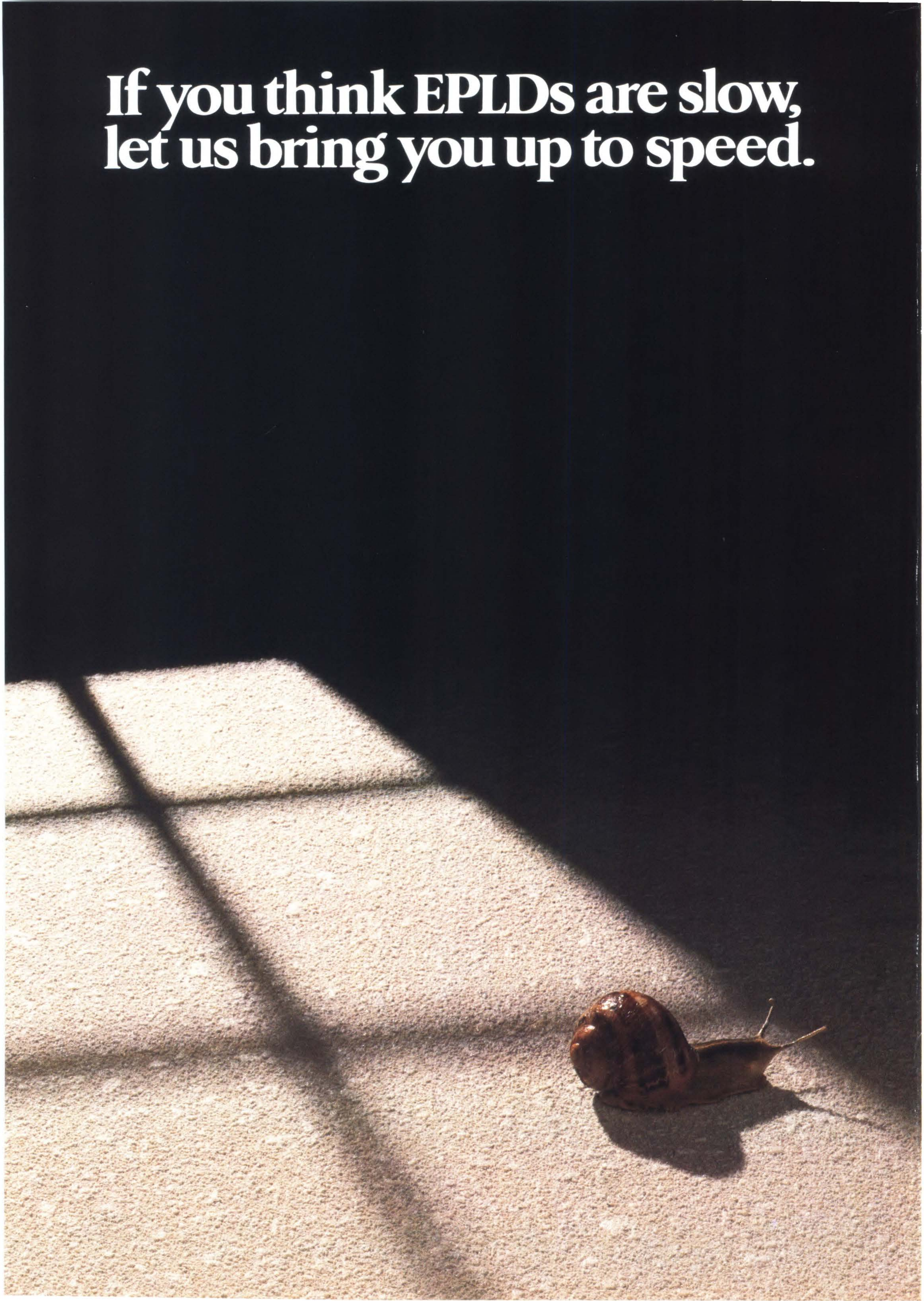


Or add a 74151, 8-to-1 multiplexer to the same MAX device and consume less than one percent of space.

So now, the functions that used to take up an entire board can fit easily into one extremely dense MAX part.

A part that you'll also find to be extremely fast.

If you're used to designing with TTL, you don't have to change your way of thinking. MAX accommodates exact functional equivalents of all popular TTL part numbers.


If you think EPLDs are slow, let us bring you up to speed.

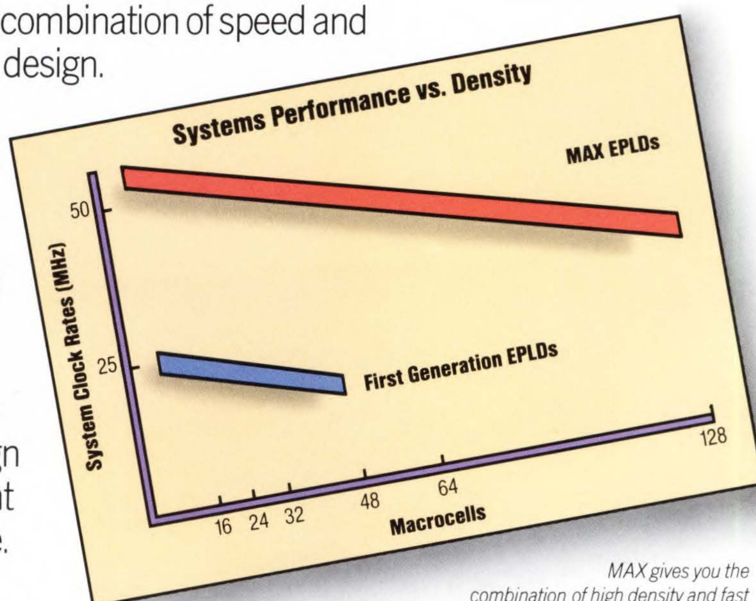
The MAX family runs at system clock rates up to 50MHz. Twice the speed of any other high density EPLD.

Only the MAX family can give you the combination of speed and density you need in your next system design.

And not just raw speed, but predictable speed as well.

Because at higher densities, our Programmable Interconnect Array gives you predictable delays between all corners of the chip.

And that means no more hair-pulling over lost speed. No gate array timing skews. No more multiple design iterations to get the speed you thought you were going to get in the first place. The result is more useable system performance at system clock rates up to 50 MHz.



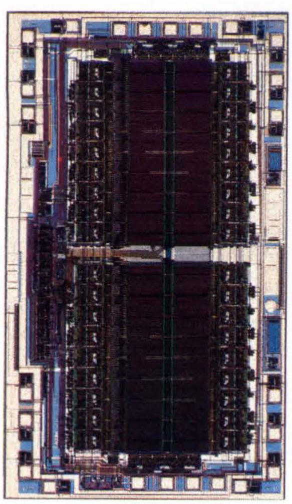
MAX gives you the combination of high density and fast performance you need for your most advanced designs.

Which makes MAX the fastest, high density CMOS EPLD in the world. For example, with our EPM5032, you can design a bus controller that runs at 32MHz while utilizing 32 registers and up to 32 product terms feeding a single register.

And with our EPM5064, you can breeze through a 25 nanosecond address decoder for a cache controller and still achieve a fan-in of 25.

For really big jobs like state-of-the-art DMA controllers, our EPM5128 has an array of expanders and macrocells that can easily soak up all the logic you need.

All of these logic functions can be designed fast, too. In just a matter of hours, in fact. Because MAX is supported by software that's easy and quick to design with.



Fast, high density controller designs can be implemented with the EPM5032, 32- macrocell MAX EPLD.

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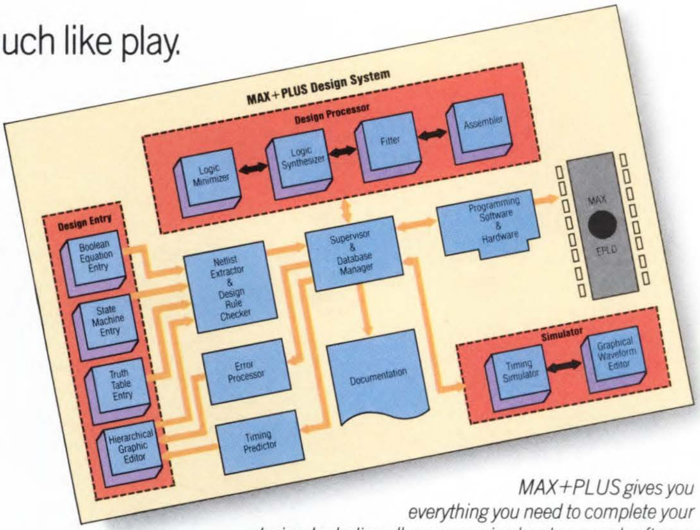
And block any thoughts about EPLDs being difficult to design with.

The new MAX+PLUS™ software makes every step of the design process quick and easy.



MAX+PLUS gives you everything you need to complete your design. Including all programming hardware and software.

Working with MAX EPLDs can be very much like play.

Thanks to MAX+PLUS.

It's software that uses powerful logic synthesis techniques that make design simple and intuitive. And it runs on your IBM PC AT™ or compatible, or IBM PS/2.™

MAX+PLUS gives you a whole set of programs under the control of a supervising database manager module.

Included are a variety of design entry methods, a design processor, a timing simulator and programming software.

A hierarchical graphics design editor lets you build your design from the top-down, starting with an overall device block diagram. Or you can go from the bottom-up, by first simulating small logic functions.

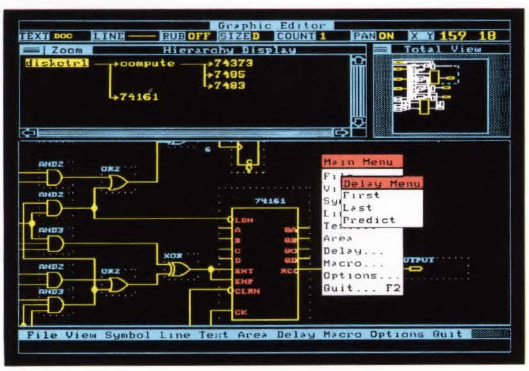
You can select logic symbols from the complete 7400 series library or build your own custom library for your specific needs.

And when you're ready to compile, the software will minimize and automatically place your design in MAX. So you don't have to. And it does it in minutes.

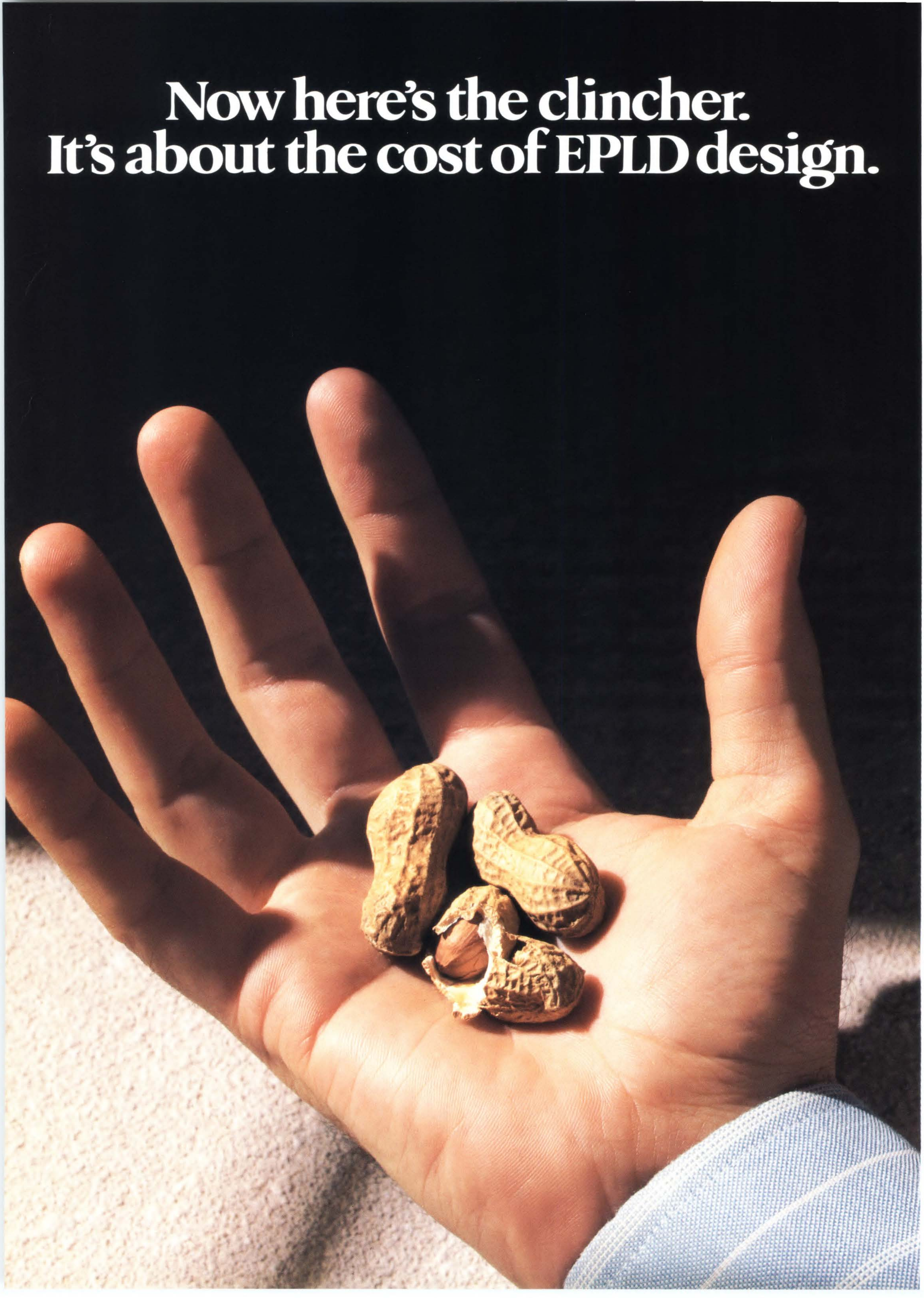
MAX+PLUS even locates your design entry errors automatically, highlighting problem nodes on your schematic. Thus saving you time and trouble.

MAX+PLUS also offers a convenient timing calculator that instantly displays your worst case delay between two points. Plus full timing simulation software to simulate your entire design.

MAX+PLUS software even solves the most important timing problem of all. Because it lets you put your custom design on your board in hours instead of weeks. Speeding you to market right on time, ahead of the competition.



The MAX+PLUS hierarchical graphics editor lets you organize your design from either the top-down or the bottom-up.


Now here's the clincher.
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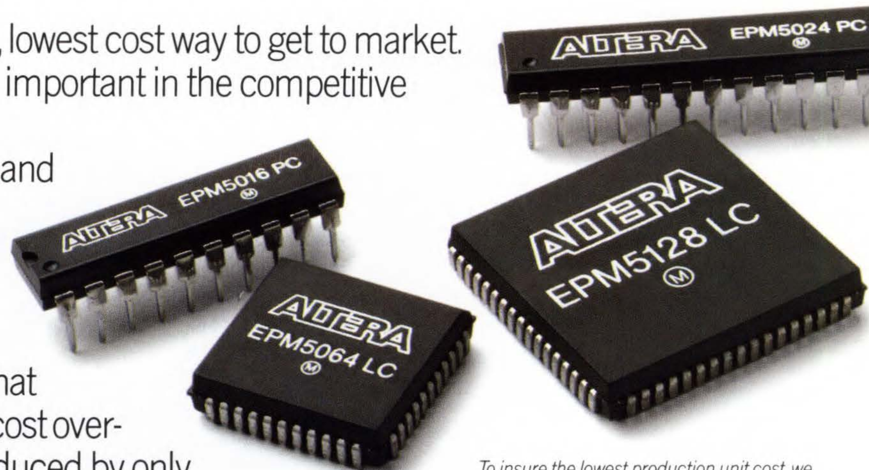
Faster design time, fewer parts on your board means MAX saves you money.

The MAX family is your fastest, lowest cost way to get to market.

Which has never been more important in the competitive electronics marketplace.

In fact, a study by McKinsey and Company shows that getting to market six months ahead of a competitor can triple profits over the life of a product.

And the same study shows that even with a 50% development cost over-run, after tax profit would be reduced by only 3.5 percent.

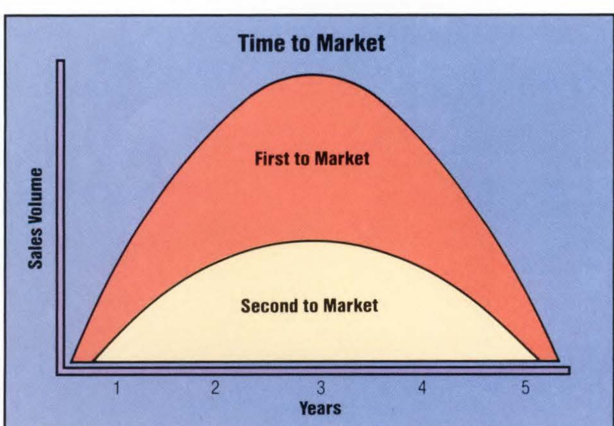


To insure the lowest production unit cost, we also offer OTP plastic devices.

But the beauty of MAX is not only that it offers the shortest time to market of any logic technology, but it's also one of the least expensive ways to go. Compare it to expensive NRE charges and the high risks of time consuming gate arrays. And you'll find there's no comparison at all.

Compared to discrete TTL, CMOS or PALs, MAX not only speeds the design process, but also dramatically reduces your parts count and your board size. That's why MAX can mean all the difference between winning the largest piece of the pie, or getting stuck with what's left of the crust.

With MAX you design for peanuts and end up with a fistful of dollars.



Getting to market six months earlier than the competition could mean a tripling of profit over the life of the product.

If you're ready to take the lead in logic design, here's your window of opportunity.

Density, speed, ease-of-use, development costs – it all points to the MAX EPLD family as the leading choice for any level of logic design.

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While your window of opportunity is wide open.

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MAX Flip Flops		16	24	32	64	128	128
MAX Latches(1)		32	48	64	128	256	256
MAX Inputs(2)		15	19	23	35	35	59
MAX Outputs		8	12	16	28	28	52
Packages		20D	24D	28D	40D	40D	68J
				28J	44J	44J	68G

Key: D—DIP J—J-Lead Chip Carrier G—Pin Grid Array
Notes: (1) When all Expander Product Terms are used to implement latches.
(2) With one output.

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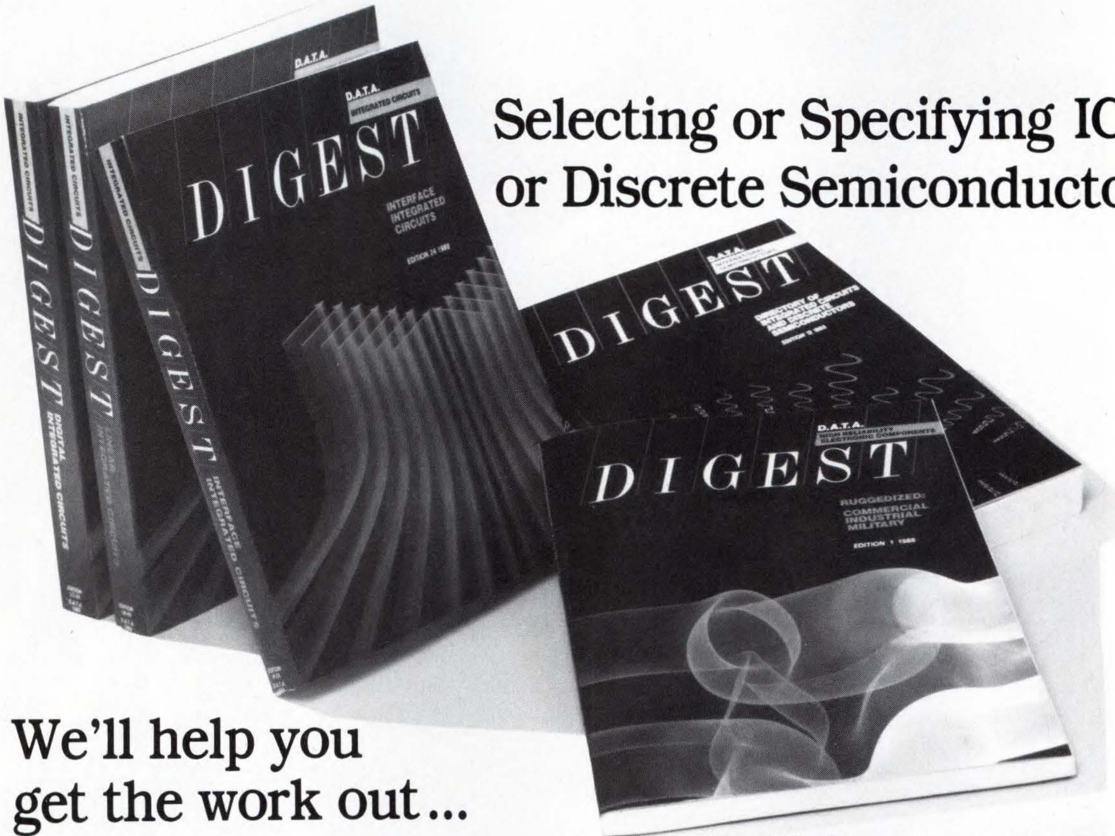

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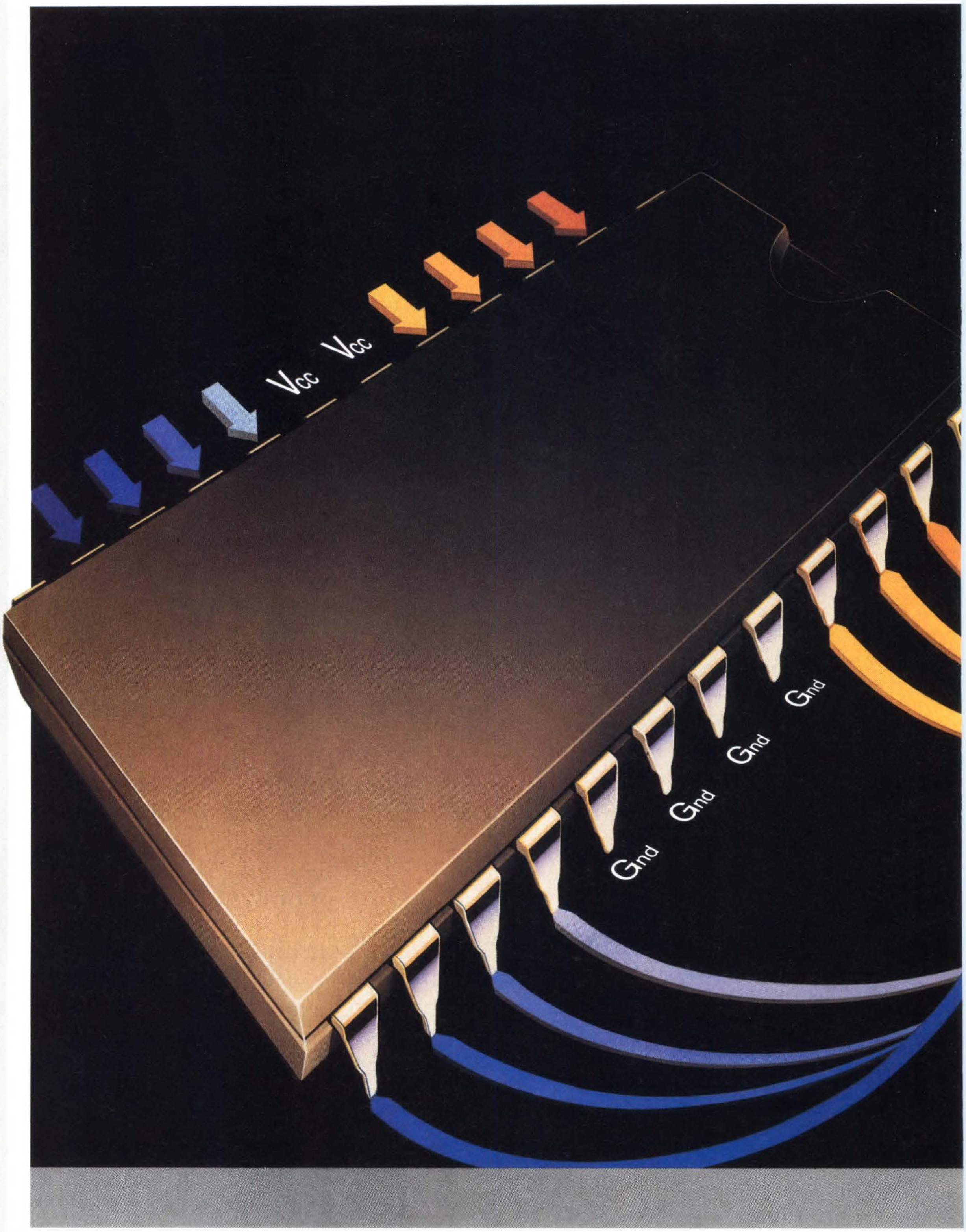
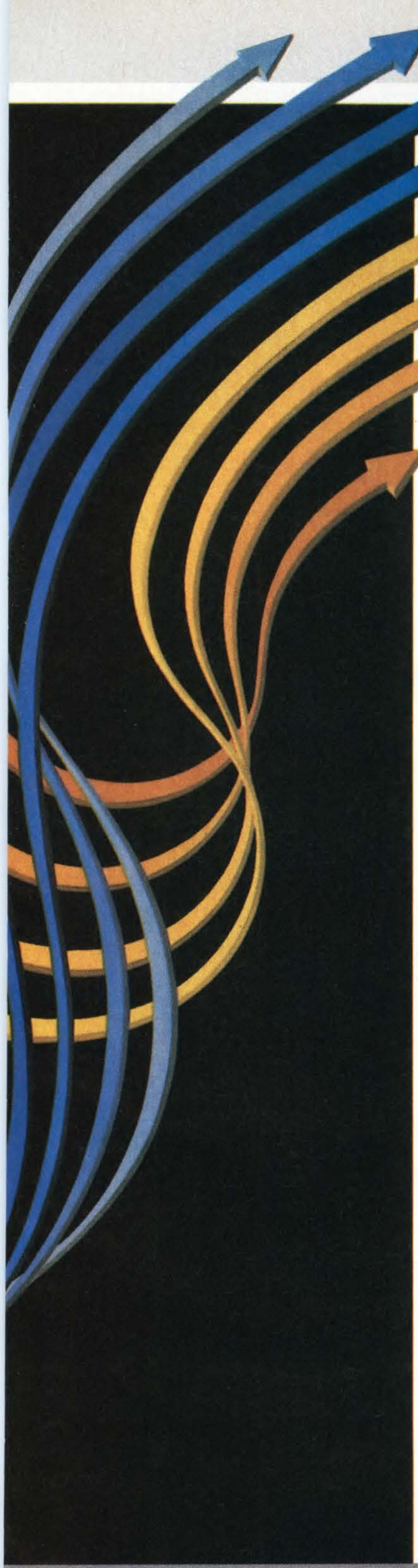


Vcc Vcc
Gnd
Gnd
Gnd
Gnd



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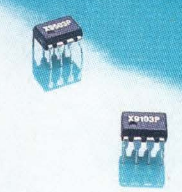

Part No.	Max. Resistance
X9103	10K Ω
X9503	50K Ω
X9104	100K Ω

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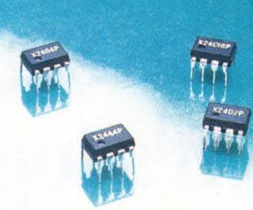
SERIAL I/O

E²PROMS AND NOVRAM



Part No.	Organization
X2402	256 x 8
X2404	512 x 8
X24C04	512 x 8
X24C16	2048 x 8
X2444	16 x 16

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E²PROMs

4K, 16K, 64K, 256K

Part No.	Organization
X2804A	512 x 8
X2816B	2K x 8
X2864A	8K x 8
X2864B	8K x 8
X2864H	8K x 8
X28256	32K x 8
X28C256	32K x 8

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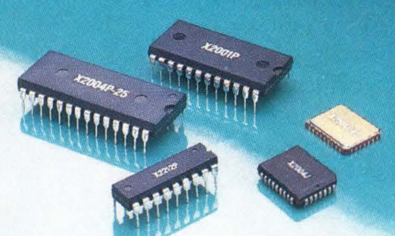
NOVRAMs*



Part No.	Organization
X2201A	1K x 1
X2210	64 x 4
X2212	256 x 4
X2001	128 x 8
X2004	512 x 8

*NOVRAM is Xicor's nonvolatile static RAM device.

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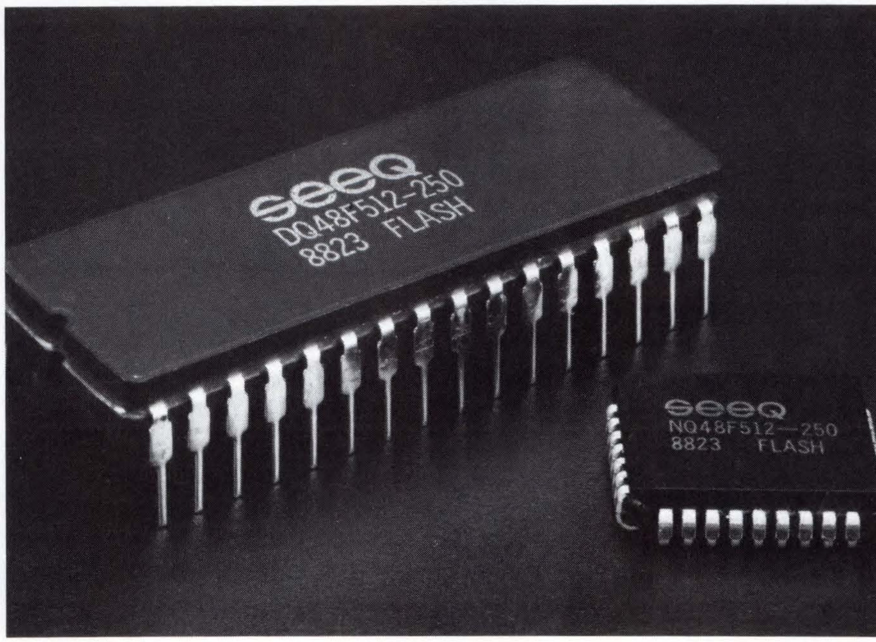
Conventional EEPROMs and flash EEPROMs offer a spectrum of bit densities

John A Gallant, *Associate Editor*



***The flash EEPROM** offers high bit densities and a chip-erase mechanism. Seeq's 48F512 is a 512k-bit device available in 32-pin ceramic and plastic DIPs as well as surface-mount packages.*

Applications abound for nonvolatile memory devices capable of occasional reprogramming. The storage of frequently used numbers in telephone equipment, password entry in security systems, patient-data monitoring in medical equipment, set-up operators in word processors and printers, and mission-configuration parameters in military countermeasure equipment are just a few that come immmediately to mind.

Although UV EPROMs meet the requirements of these applications, you have to remove them from the system before you can reprogram them. Theoretically, you could overcome this limitation by designing-in a large number of DIP switches, but this approach has practical drawbacks—imagine trying to include 2000 DIP switches in your design! EEPROMs offer a feasible alternative.

Nowadays EEPROMs come in two guises (see **box,** "The EEPROM: from the 70s to the 80s"). The flash EEPROM uses hot electrons to charge the floating gate. Manufacturers are still searching for a term to distinguish the flash EEPROM from its forerunner, a device that charges the floating gate through Fowler-Nordheim tunneling. The term most often bandied about is the full-featured EEPROM.

Because tunneling requires much less current for programming, manufacturers include charge pumps on full-featured EEPROM chips to develop the high programming voltage from a standard 5V input. In addition, the requirement of a select gate allows the tunneling device to be programmed on a byte-by-byte basis. These two features are not currently available on flash EEPROMs.

Both NMOS and CMOS full-featured EEPROMs are characterized according to how data is transferred to the chip—either serially or in parallel. Serial EEPROMs are popular in applications that require a small package size and when programming time isn't critical. Parallel EEPROMs permit faster programming yet exact a larger package size. Because full-featured EEPROMs require a select transistor in each memory cell, bit densities are restricted to 256 to 256k bits on one chip.

Many cereals taste the same

Serial EEPROMs operate more or less alike, but they have differing bit densities—256 to 4k bits. Most serial EEPROMs come in 8-pin DIPs. You command one of the pins (ORG) to set the memory organization to be either 8 or 16 bits wide. An external clock tied to the serial clock (SK) pin serially loads an instruction word on the input data pin (DI) into on-chip holding registers. Each instruction consists of a start bit, a 2-bit op-code field, a memory-address field, and an optional 8-or 16-bit data field. Once an instruction is loaded, you externally set the chip-select (CS) line to execute the instruction. Program execution is transparent to the user. Data is serially clocked out of the device on the data-output (DO) pin.

The industry-standard 93C46 is an example of a 1k-bit serial CMOS full-featured EEPROM **(Fig 1).** The device is available from Catalyst, ICT (International CMOS Technology), Sierra, and National Semiconductor. You can externally command the memory array to have

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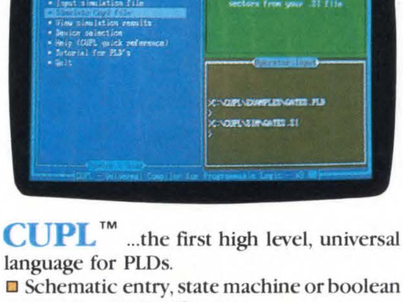

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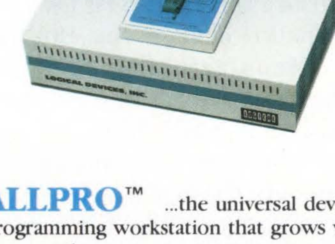

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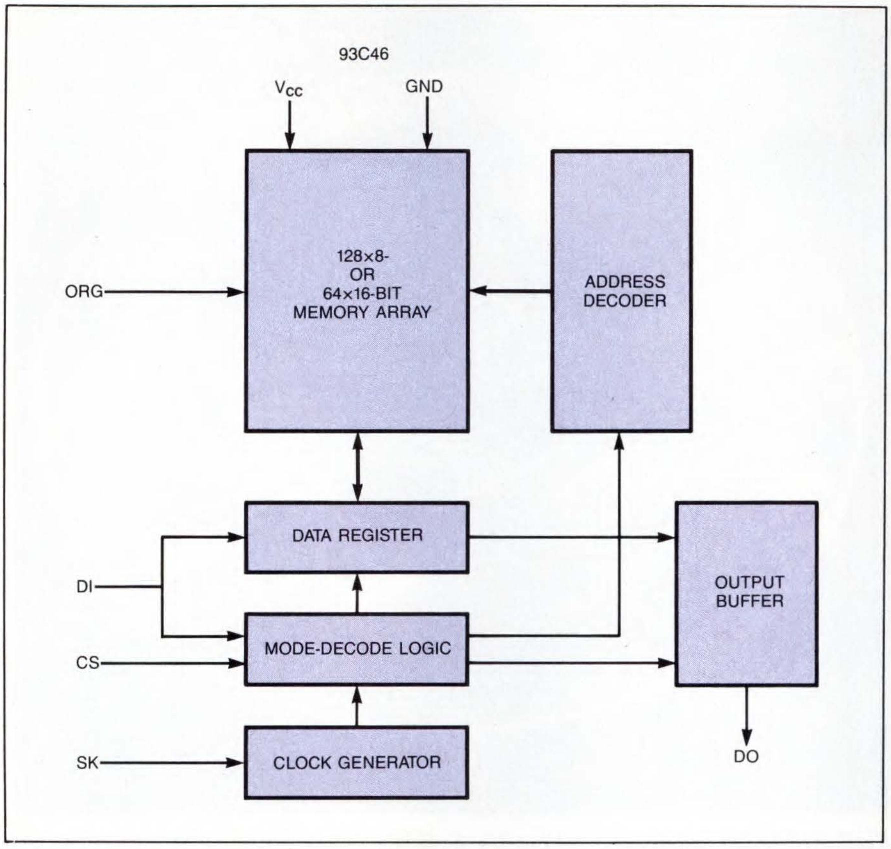


***Fig 1—The 93C46 is representative** of the industry-standard serial EEPROM. This type of device comes in an 8-pin package, yet differs in bit densities.*

either a 64×16-bit or a 128×8-bit organization. The external clock can operate as high as 250 kHz. If the chip decodes either an erase or a write instruction, it generates a 10-msec (max) erase/write pulse to execute the instruction after the CS line is brought low. You can also issue an Erase All or a Write All instruction, which lets you simultaneously alter all locations in memory. Depending on the manufacturer, the device draws 3 to 4 mA while operating and 100 μA in standby mode. The 3-mA Catalyst CAT93C46 comes in either an 8-pin plastic DIP or single-outline surface-mount package and costs $2.60 (100).

To respond to the industry demand for a low-power serial EEPROM capable of operating from battery voltages, ICT recently introduced an extended-voltage version of the 93C46 EEPROM. Labeled the 93C46X, it operates from input voltages over the range of 2.5 to 6.0V. The maximum current drawn during active operation is 1 mA; the standby consumption is 50 μA (or less). The 1k-bit memory is arranged into 64 registers of 16 bits each.

In addition, the company offers the 93C66X EEPROM, which has the same features as the 93C46X except that it has 4k bits of memory arranged as 256 registers of 16 bits each. Both devices are available in 8-pin DIPs or SO surface-mount packages. The 93C46X sells for $2.20, and the 93C66X sells for $5.30 (100).

Endurance is limited

When EEPROMs undergo repeated data alterations, they suffer from endurance limitations. The two predominant technologies used to manufacture EEPROMs today have different failure mechanisms and therefore have different endurance specs. The previously discussed devices depend on a thin dielectric (approximately 100Å) lying between two silicon surfaces to transport the charge. The thin dielectric, called Flotox for floating-gate tunnel oxide, experiences a dielectric breakdown effect after a certain number of erase and write operations. EEPROMs of this type typically have an endurance specification of 10,000-erase/write cycles per register and 10 years of data retention.

Xicor takes a different approach. This manufacturer uses a textured polysilicon to deposit charge on the floating gate **(Fig 2)**. This technique depends on enhanced fields on the surface bumps of the polysilicon material. Charging and discharging the floating gate occurs as a result of Fowler-Nordheim tunneling of the electrons through a thick dielectric layer (greater than 500Å).

Xicor's serial EEPROMs have bit densities varying from 2k to 16k bits. The company specifies a data-retention time of 100 years and a failure rate of 0.015% for EEPROMs requiring 10,000 data changes. Because only the surface of the textured polyoxide experiences the electrical field, Xixor's cell is not as susceptible to dielectric breakdown as the Flotox cell. However, the thicker oxide is more susceptible to electron trapping.

Parallel is always faster

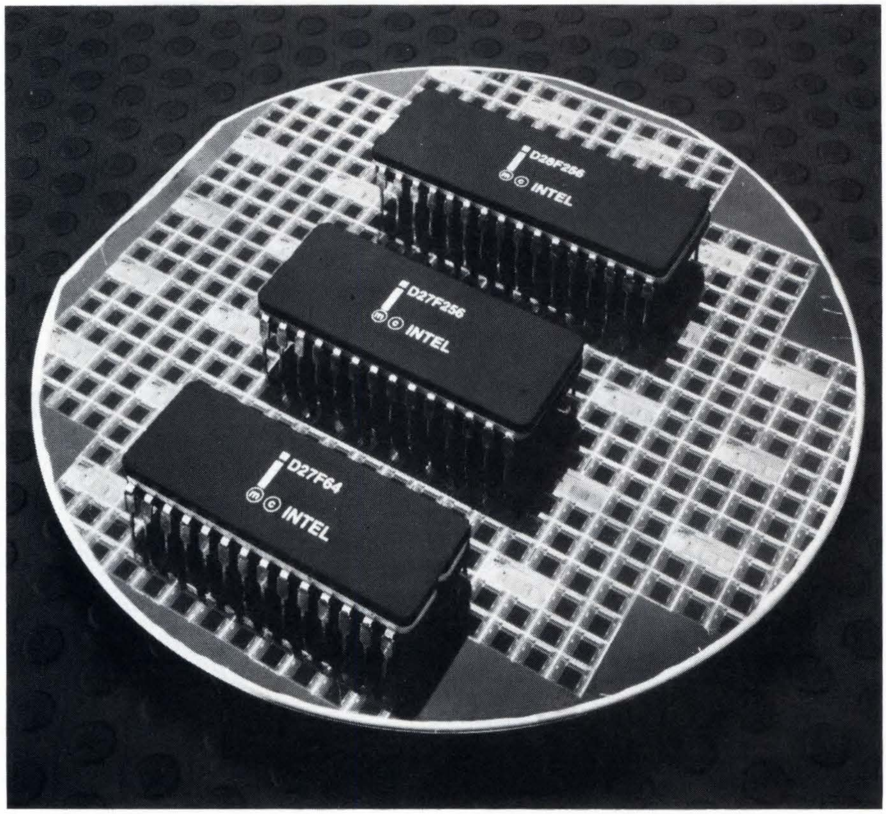
If your application requires fast read and write times, you'll want to consider a parallel EEPROM. With these devices, you access data on a per-byte basis (8-bit parallel). Current bit densities range from 4k to 256k bits. Xicor's parallel EEPROMs, for example, have densities as great as 256k bits. Typical read-access times range from 150 to 450 nsec.

Some high-speed versions are available, however. Seeq offers a series of 16k-bit and 32k-bit high-speed EEPROMs that rival the read-access times of static RAMs. The devices have access times of

35 to 70 nsec. In addition, Xicor offers a 64k-bit EEPROM with a read-access time of 70 nsec.

Manufacturers generally specify the time to write a byte into a location in the EEPROM as less than 5 or 10 msec—depending on the device. Some EEPROMs, however, include on-chip features that effectively reduce the byte-write time.

Seeq, for instance, sells a 64k-bit part and a 256k-bit part that includes a 64-byte page buffer that the user can write to in a page mode. Each of these Timer E^2 chips latches the row and column addresses into itself, and an on-chip timer automatically loads anywhere from 1 to 64 bytes into the buffer. When the timer times out, all the bytes loaded into the buffer are simultaneously written to their addressed locations in the EEPROM. Although it takes 10 msec to write one byte into memory, a 64-byte page has an effective 160-μsec average byte-write time. The 64k-bit part costs $13; the 256k-bit part costs $85 (100).



Flash EEPROMs can directly replace *UV EPROMs. Intel's 27F64 and 27F256 are direct-socket replacements for their 64k- and 256k-bit JEDEC-standard EPROMs.*

AMD's Am2864BE is another example of a 64k-bit parallel EEPROM with on-chip page-mode features. In this case, the page-write mode lets you write 1 to 32 bytes of data in a single write cycle. The page mode consists of a load sequence that sequentially loads the byte address and the byte data into a 32-byte on-chip register. The load sequence is followed by a write sequence that automatically erases any data existing in an addressed cell before it writes it to the addressed locations. The effective average byte-write time is 312 μsec; thus you can fill the 8k-byte space in 2.6 sec. A 250-nsec commercial-temperature version of the Am2864E sells for $9 (100).

The Seeq and the AMD parts have bidirectional I/O data pins, which let you use data polling. Data polling provides a method of determining the exact end of the automatic write cycle so that you read only valid data from the memory. Data polling complements the last byte sent to the page buffer while a write operation is in progress. A user-written software routine reads the data at this buffer location until the chip returns the valid data once again to this location when the write sequence is complete. The software routine ignores the data until it recognizes the byte as valid.

These full-featured EEPROMs'

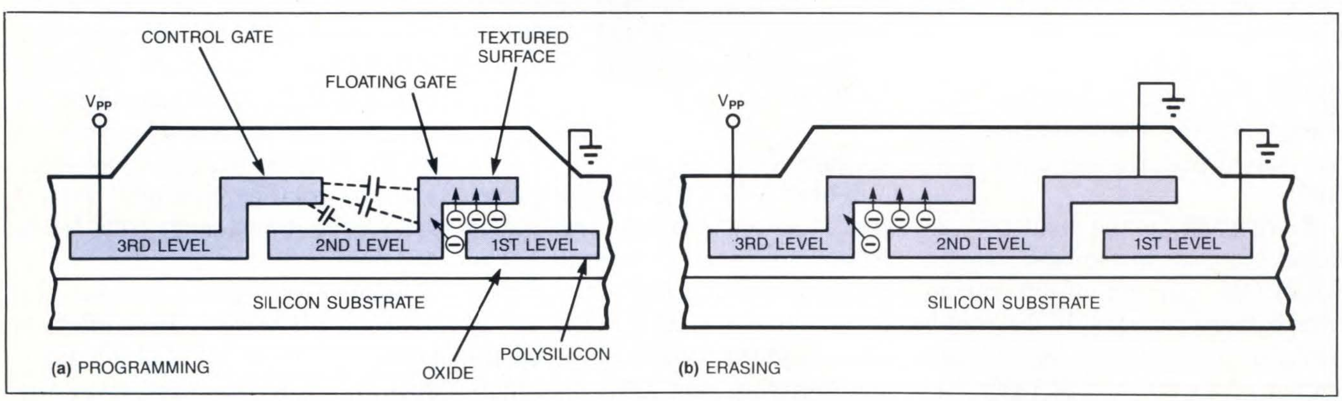


Fig 2—The textured-surface EEPROM cell *uses three polysilicon gates. These Xicor cells make use of a thick tunneling oxide to charge and discharge the floating gate.*

on-chip attributes exact a penalty, however. The select gate in each of the cells allows you to program the device on a byte-by-byte basis, but the extra gates occupy valuable chip real estate. Furthermore, the integrated charge pumps, timers (and, in some cases, write-protect circuitry) increase chip size and component cost.

Flash EEPROMs surmount bit-density limitations, yet they aren't cost prohibitive. Because flash EEPROMs have one polysilicon structure for the control and select gate, the flash cell size can be comparable to that of a standard UV EPROM cell. Therefore, bit densities comparable to UV EPROMs are economically attainable. In addition, flash devices require hot electrons to charge the floating gate similar to UV EPROMs. Because the charging process requires large currents, manfacturers do not include on-chip charge pumps on their devices, which conserves additional chip area.

Built-in reset is the key

The erase mechanism for flash EEPROMs utilizes Fowler-Nordheim tunneling to move electrons from the floating gate to either the source or the drain region. However, because the control gate and the select gate are all one structure, there is no isolation between cells and all cells get erased simultaneously.

Intel builds its flash EEPROMs with its proprietary Etox (EPROM tunnel oxide) process. The Etox process incorporates a tunnel oxide into the company's CHMOS II-E EPROM process to move the charge to the source of the flash cell **(Fig 3a)**.

In essence, the Etox process provides an EPROM with a typical 1-sec electrical erasure time instead of the usual 20 minutes required to erase a UV EPROM. The current Intel product line consists of 64k-

The EEPROM: from the 70s to the 80s

The patriach of electrically alterable nonvolatile memory devices is the UV EPROM. In the mid 1970s, Intel pioneered the development of the UV EPROM by creating an extra floating gate positioned between the conventional gate and the substrate of an MOS transistor **(Fig Aa)**. Intel renamed the conventional gate the control gate.

When a high voltage (aproximately 20V) is applied to the drain and the control gate, the large channel current (1 to 2 mA) is made up of high-energy, or hot, electrons. Some of these hot electrons have enough energy to conduct through the insulating SiO_2 layer and deposit themselves on the floating gate. When the control gate operates from normal logic levels (0 to 5V), the cumulative negative charge on the floating gate (approximately $-8V$) affects the transistor's pinch-off characteristics.

The UV EPROM consists of an array of these types of MOS transistors. When a transistor in the array is selected, the transistor either conducts current or remains cut off, depending on whether its floating gate is negatively charged. You erase the UV EPROM by exposing the transistor array to an ultraviolet light for about 20 minutes. The energy in the ultraviolet light neutralizes the cumulative charge on the floating gates to approximately 0V.

In the early 1980s, memory-device manufacturers began using another method to deposit charge on the floating gate. For some time it had been known that a strong electrical field applied across a thin layer of SIO_2 would induce low-energy, or cold, electrons in the silicon's conduction band to tunnel into the SI_2's conduction band. This effect, known as Fowler-Nordheim tunneling, was useful for depositing charge on a floating gate. Moreover, because the process didn't require high-energy electrons, you could reverse it to electrically remove the

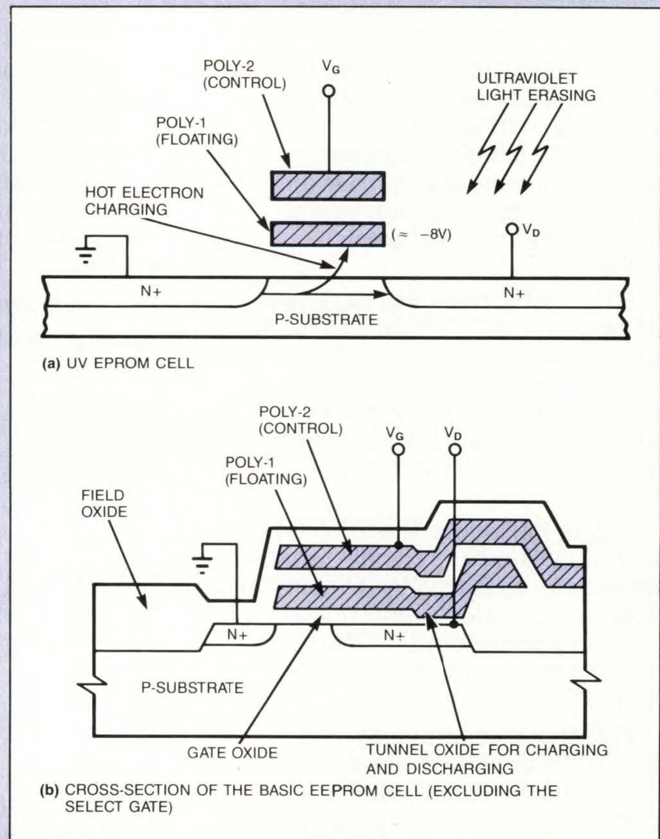


*Fig A—**As you can see,** the differences between the conventional EEPROM cell and the UV EPROM cell are marked.*

and 256k-bit parts that can be programmed in less than 4 sec using an external 12.0 or 12.75V programming voltage. The failure rate of these devices is less than 0.01% for 100 erase and program cycles.

The company also offers an extended-endurance version of the 256k-bit part that boasts a failure rate of less than 0.1% for 10,000 erase and program cycles. A 256k-bit part with a read-access time of 250 nsec and a standard endurance specification sells for $31 (100). An extended-endurance 256k-bit version costs $40.10 (100).

The memory cell in Seeq's product line of flash EEPROMs has a polysilicon control gate modified to create a pseudoselect transistor **(Fig 3b)**. Electrons tunneling through a thin oxide layer to the drain region erase the floating gate. The cell size on the 512k-bit 48F512 is 25 μm^2, which is comparable to a UV EPROM cell size. The memory array consists of 128 sectors of 512 bytes each. Using an external 12V programming voltage, you can individually erase and reprogram each of the sectors, or you can erase the entire memory contents. The maximum erase time is 7.5 sec for either of the erase options. The write time is 1 msec/byte and the typical read-access time is 200 nsec. The part specifies an endurance of 100 erase and program cycles, but is available screened to 1000 cycles. It comes in a 32-pin plastic or ceramic package and costs $33.

Adhering to the pervasive eclectic approach to electronic-device design, designers are beginning to include intelligence on EEPROM chips. Because EEPROMs require a μP for programming, it seems reasonable to include the necessary intelligence on the same IC.

Texas Instrument's TMS370 family of μcontrollers include full-featured EEPROM options for program development and data alteration. These ICs have, along with

charge on the floating gate. This new method made possible the birth of the EEPROM **(Fig Ab)**.

Manufacturers had to overcome a number of difficulties in order to develop an EEPROM cell, however. First they had to develop a thin-film SiO_2 layer 100Å or less as compared with the >500Å SiO_2 layer in the UV EPROM. Like the UV EPROM, an EEPROM requires a high voltage on the control gate. The capacitive coupling between the gates induces a voltage on the floating gate to create the electrical field across the thin SiO_2 layer. Because the tunneling current of an EEPROM is small (on the order of 1 nA), the floating gate is programmed with a lower cumulative charge than its UV EPROM counterpart. Therefore, when the cell operates from standard logic voltages, the channel can draw current in both of the programmed states.

To isolate the cell from the other cells in an EEPROM array, each cell requires a select transistor. When the select transistor turns on, a current-sense amplifier determines the programmed state of the cell.

The requirement of a select transistor is both a blessing and a curse. The select transistor requires extra cell area. Whereas the typical UV EPROM cell area is 25 μm^2, the typical EEPROM cell can be 50 μm^2 or greater. The extra area limits the maximum economically feasible bit densities of EEPROMs to 256k bits.

You can erase and write to the EEPROM on a byte-by-byte basis, however. The cell's select transistor isolates the storage transistor from other cells in the array when programming a particular column. Erasure is no more than a write operation, which charges the floating gate of a selected cell. A write operation consists of grounding the program line for a selected row and raising the appropriate column lines to a high voltage (15 to 20V) to match the desired data pattern. The high-voltage column lines discharge the floating gates of the selected cells.

The flash EEPROM is a recent innovation that overcomes the the high cost and low density of what are now referred to as full-featured EEPROMs. The flash EEPROM combines the programming techniques of UV EPROMs with the erasure techniques of EEPROMs. In much the same manner as the UV EPROM, the flash EEPROM charges the floating gate by injecting hot electrons through a thick SiO_2 layer. A small portion of the floating gate overlaps the drain (or the source) region, which is separated by a thin oxide layer. The charge on the floating gate is removed when the control gate is grounded and the electrons are tunneled through the thin oxide layer as a result of applying a high voltage to the drain (or the source).

Because the floating gate gets charged to a high negative voltage, the control gate can govern the cell operation similar to the UV EPROM cell. This control eliminates the need for a select gate so that the cell size of a flash EEPROM is close to that of a UV EPROM. However, without a select transistor, no isolation exists between cells in the array, and therefore the erasure operation discharges all of the floating gates in the array.

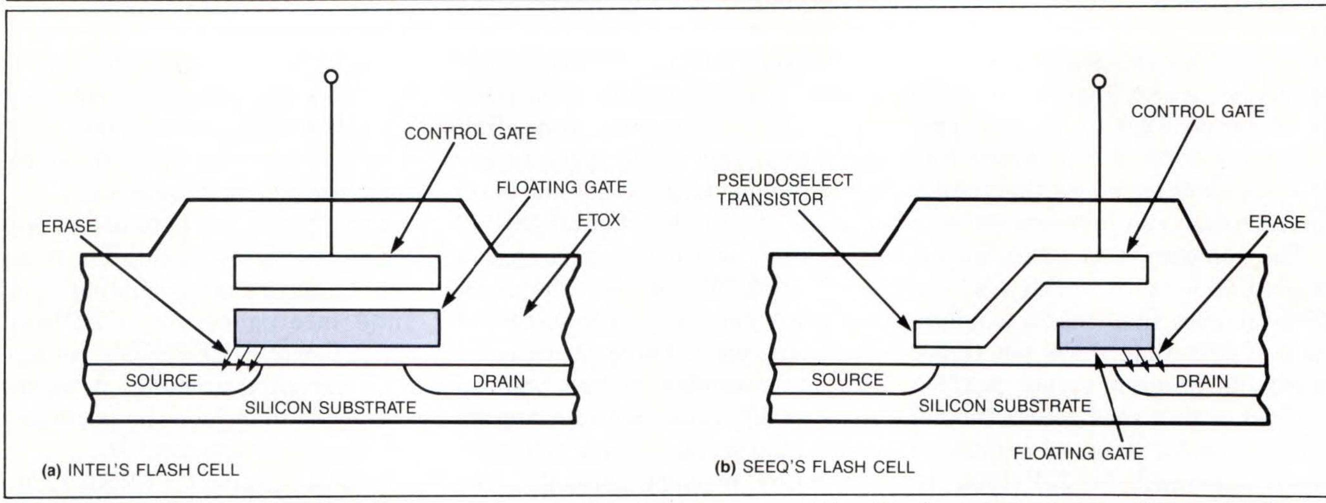


*Fig 3—**Although flash EEPROM cells** differ in structure, they do have commonalities. The floating gate is charged using hot electrons and is discharged via Fowler-Nordheim tunneling.*

an A/D converter and other peripherals, 4k bytes of program memory and either 256 or 512 bytes of data memory in EEPROM. The data memory has a 10,000-cycle endurance spec and a 10-year data-retention specification. The TMS370C010 and the TMS370C310 are available in 28-pin plastic DIPs and cost $3 and $7, depending on quantity.

Sierra Semiconductor recently expanded its CMOS library of standard cells to include a 256-bit EEPROM megacell array. You can combine the EEARRY256 in an ASIC with over 300 digital cells and 50 analog cells. Available in 64×4-, 32×8-, and 16×16-bit configurations, the megacell has an endurance specification of 1-million write and erase cycles. It retains data for 25 years. The nonvolatile memory has a 10-msec write cycle and a 125-nsec read-access time. The company estimates that the inclusion of the megacell adds $1.25 (50,000) to the cost of a mixed analog and digital semicustom chip design.

Catalyst Semiconductor, which makes a line of serial and parallel full-featured EEPROMS, has not only incorporated a μC with a serial EEPROM on an IC but has included security features as well. The CAT35C704 requires the entry of an access code word, which can range from 8 to 64 bits, before you can access the 4k-bit EEPROM data. The IC is designed for the smart card market, which requires a secure nonvolatile, but alterable, storage device. The data in memory can be separated, so that users without security clearance can access one section while only those with a "need to know" can access the other.

The chip has eight connections so it can reside in an 8-pin DIP or a direct-mounting assembly. If you require more intelligence than that provided by its on-chip controller, you can connect the CAT35C704 to an 8051 or COPS family of μCs through serial I/O ports. An 8-pin DIP version costs $16 (100). EDN

For more information . . .

For more information on the EEPROMs described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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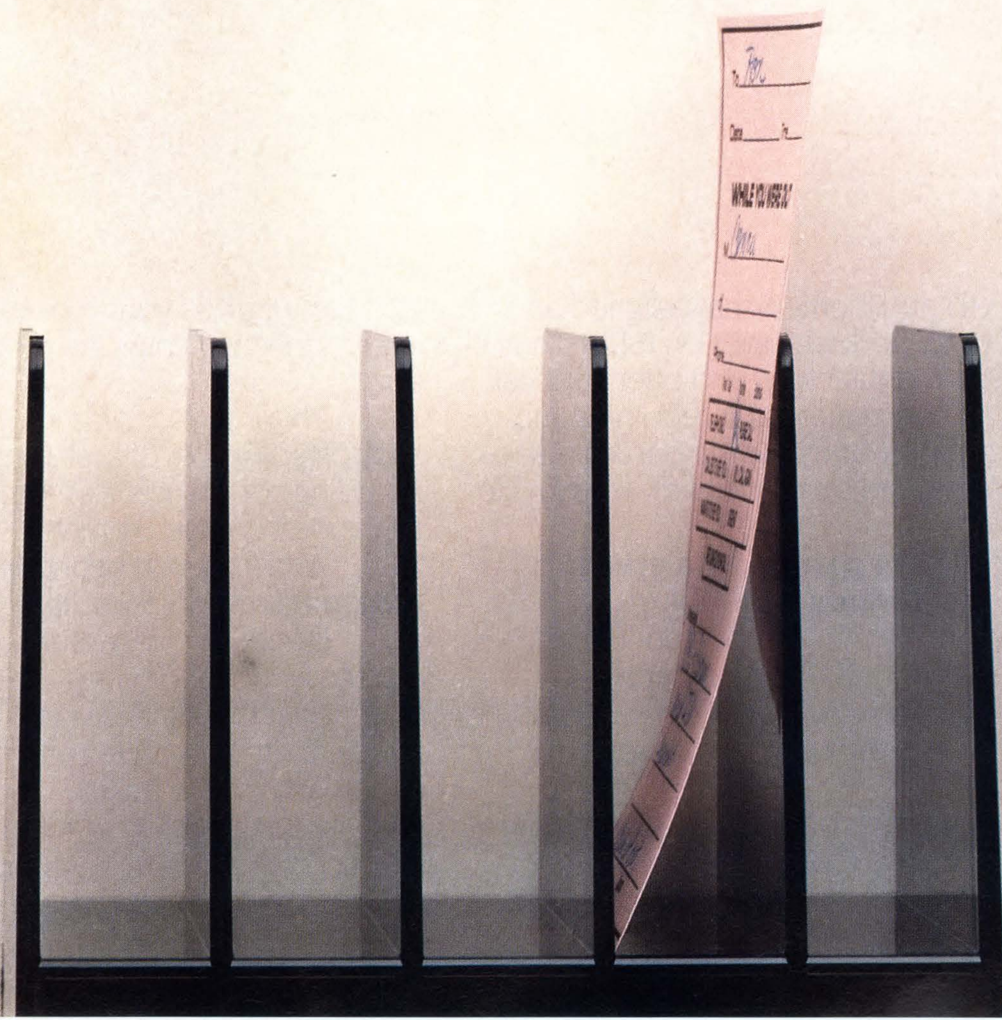

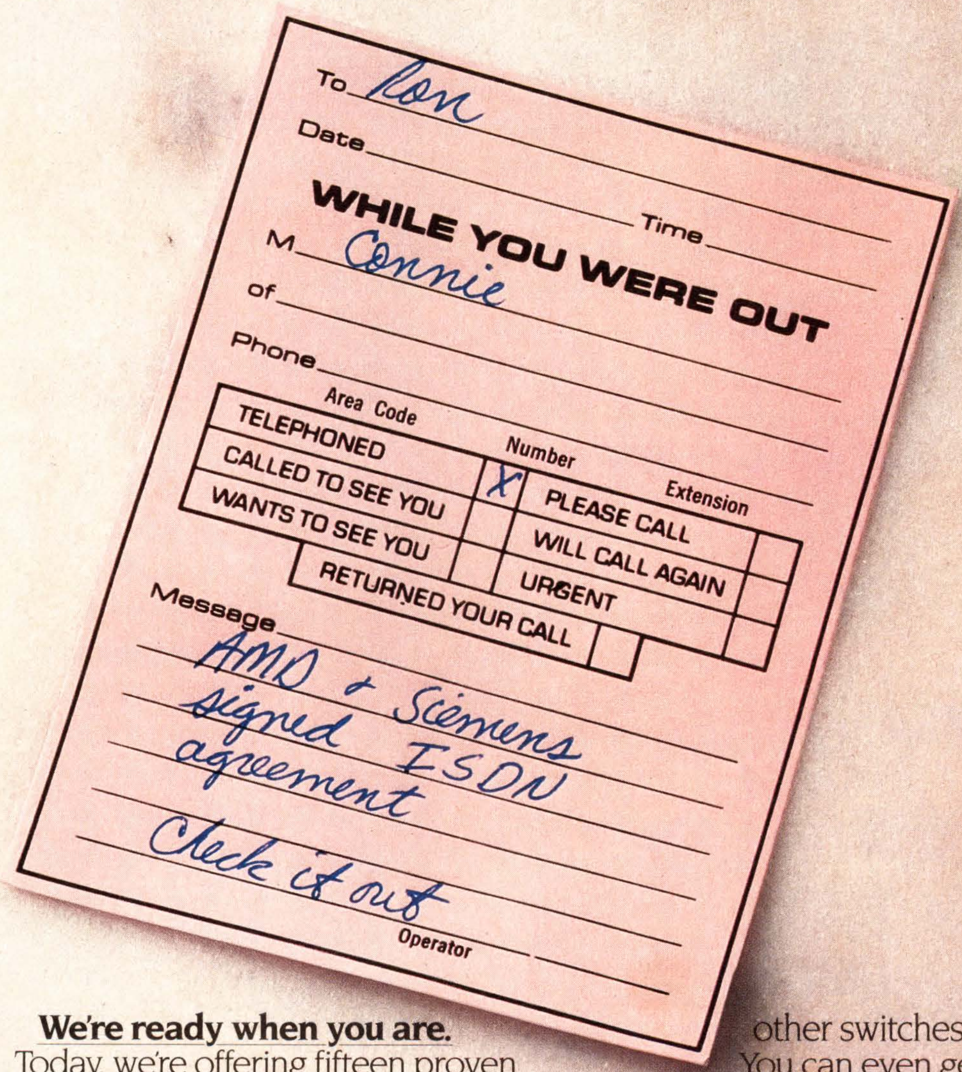

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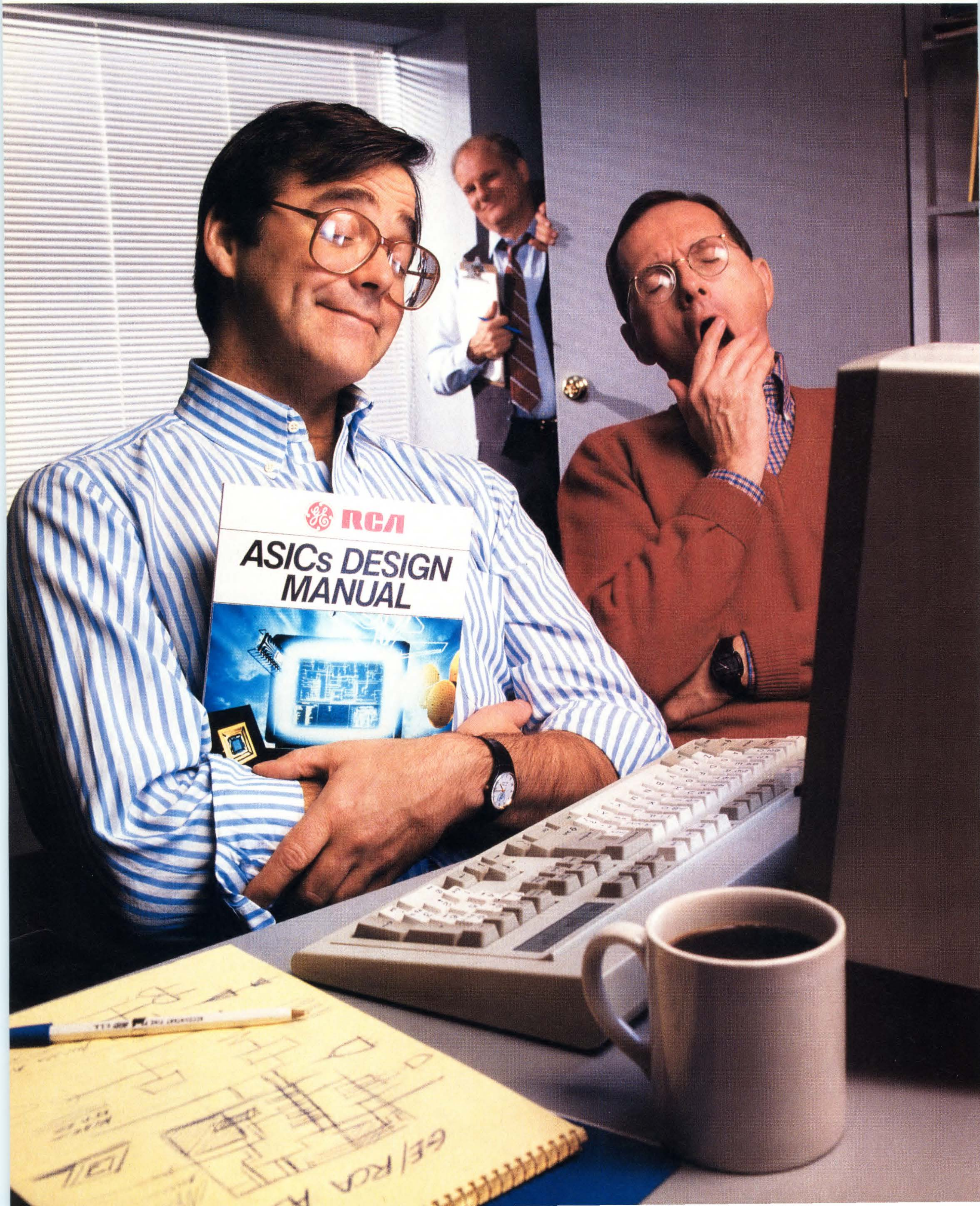

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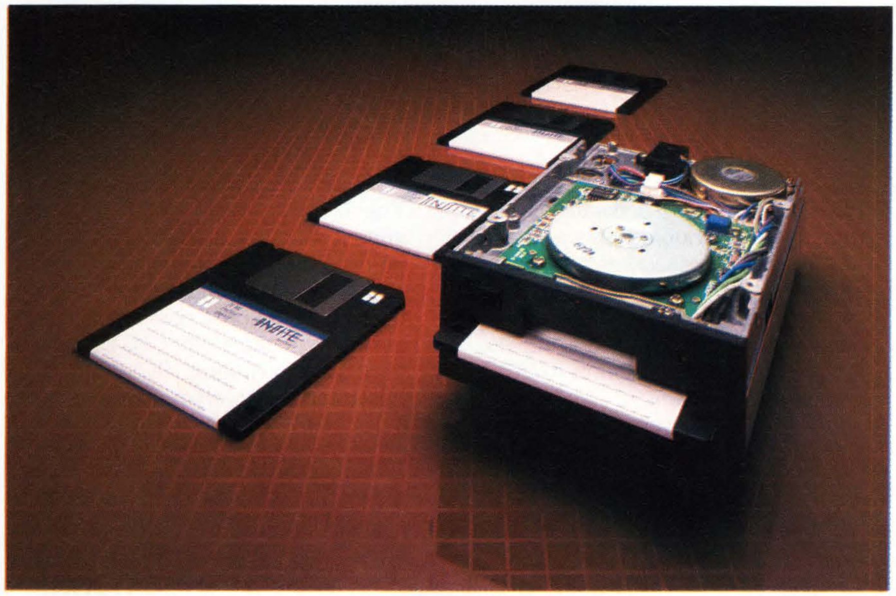
Recent 3M- to 20M-byte, 3½-in. floppy-disk drives suit mainstream uses

Maury Wright, *Regional Editor*



Servo tracks optically inscribed *on standard floppy media allow the Insite Peripherals Floptical drive to store 20.8M bytes at a track density of 1250 tpi.*

Manufacturers of floppy-disk drives are starting to offer 3½-in. models that store 3M to 20M bytes, and the main question is whether this new breed of floppy drives will venture forth into mainstream applications or, like their 5¼-in. high-capacity cousins, be relegated to niche applications. In terms of technology, the new 3½-in. drives are well suited to mainstream uses like general back up, program and data distribution, and primary storage. But logistics may decide the issue: Factors such as media, interfaces, cost, and read/write compatibility with lower-capacity drives may determine how much of an impact these high-capacity drives will have on major application areas.

Virtually every computer system shipped, and many products with embedded computers, include at least one floppy-disk drive. Most often, the lower-capacity floppy drive serves only to boot the computer initially and then to load programs onto the system. The 3M- to 20M-byte 3½-in. drives do a lot more: A 20M-byte drive can be the primary storage, for instance, for a laptop, or even a desktop, computer. What's more, performance of some of the new floppy drives rivals that of some low-cost Winchesters.

Drives provide data security

High-capacity floppy drives also provide an attractive alternative to tape drives for μC backup applications. The drives offer an effective way to store graphics images that can quickly fill even a large Winchester drive. And, the drives can store sensitive data that require vault storage when not in use.

Based strictly on technological grounds, you can integrate floppy drives into various applications, and meet with limited success. For example, users often only back up data from their own system and don't swap data with other systems, so compatibility doesn't become an issue. Nor does it become an issue for manufacturers of captive systems, such as a single-source closed-architecture computer. And some end users, such as those concerned with data security, frequently place less emphasis on media, cost, and compatibility issues.

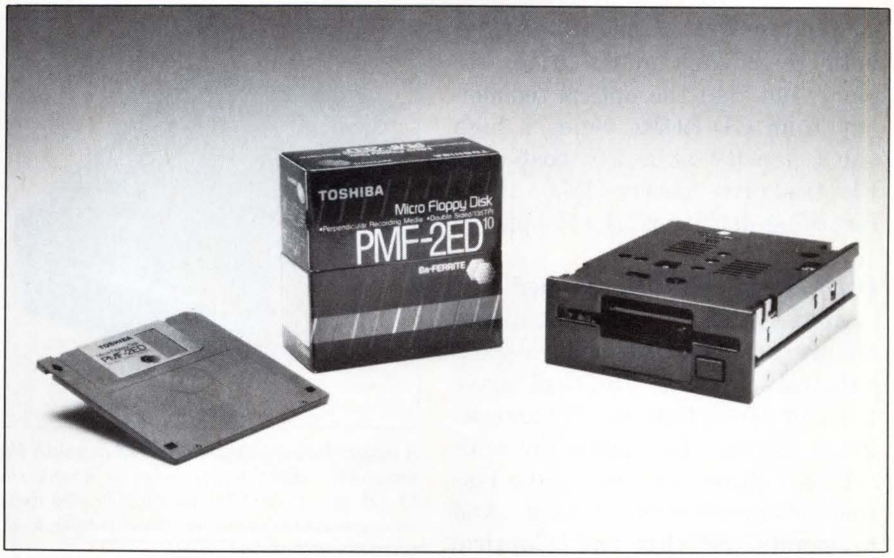
Downward compatibility is key

To achieve mainstream status, however, high-capacity floppy-disk drives can ignore neither cost nor compatibility. A resolution to the compatibility problem for these drives can come about in one of two ways: IBM could impose a standard by adopting a high-capacity 3½-in. floppy-disk drive for some of its products. Or, the drive manufacturers can offer downward compatibility with the standard 720k-byte 3½-in. drive. Insite Peripherals' president James Adkisson believes a drive must offer downward read/write compatibility, plus be low in cost and be accepted as a de facto standard with multiple sources, before it can become the primary floppy drive in an open system, such as an IBM-compatible personal computer.

For users of personal computers, workstations, and even minicomputers, a standard high-capacity 3½-in. floppy drive would offer distinct advantages over other devices. Floppy drives have the advantage of random access compared with tape drives in archival and backup roles. Publishers could distribute software and data on a single floppy disk rather than many low-capacity disks. In addition, the high-capacity drives could provide truly transportable primary stor-

age—you could take your software with you.

Three companies, Toshiba, Insite Peripherals, and Brier Technology, have introduced high-capacity 3½-in. drives, which should all be available in production quantities around the end of the year. The three products are vastly different from one another. Toshiba's $100 (1000) PD-210 drive stores 2.95M bytes formatted (4M bytes unformatted) and uses a perpendicular-recording scheme. The $250 (5000) Model I325 Floptical drive from Insite features an optical-servo-tracking scheme and stores 20.8M bytes formatted (25M bytes unformatted).



***Using perpendicular-recording technology** and a 34,868-bpi recording density, Toshiba produces the PD-210 2.95M-byte floppy-disk drive that maintains read/write compatibility with 720k-byte drives.*

Servo guides head

The BR 3020 drive from Brier Technology costs $350 (5000) and stores 21.4M bytes formatted (25M bytes unformatted). This drive uses a magnetic servo signal buried beneath the magnetic data. Irwin Magnetics plans to second source the Brier drive, although it has not announced production dates.

The available drives have one common feature—each product uses the standard 3½-in. flexible-media cartridge. They don't, however, use the standard magnetic oxide coating—all of the new drives require barium ferrite media. Once considered to be more costly, barrium ferrite is now a thoroughly viable media: it's economical, available, and technologically superior for some applications. Insite's drive can operate with the standard 1.4M-byte 3½-in. oxide media, but the company recommends barium ferrite disks. In fact, drive and media manufacturers agree that even 1.4M-byte 3½-in. drives work better with barium ferrite media than with the high-density oxide media.

The Toshiba PD-210 is the only one of the three drives coming out this year that uses the standard barium ferrite disks. Toshiba has begun producing 3½-in. barium ferrite disks in volume, and other media manufacturers plan to do so soon. The high-capacity oxide disks for 1.4M-byte drives currently retail for about $5, and manufacturers plan to offer barium ferrite disks at a competitive price by year's end.

Disks use barium ferrite

The drives from both Brier and Insite require preformatted media. The buried-magnetic-signal scheme Brier uses must be written on the barium ferrite media with a custom magnetic servo writer. Initially Brier and Irwin will supply the servo-written disks. The companies expect them to retail for $25. Brier also plans to license media manufacturers to produce the disks.

The Insite drive requires a magnetic disk that has optical servo tracks inscribed on it. The company plans to start selling the media for a retail price of $20. It believes it can drop that price to $10 within a year. Insite has licensed Dysan and Verbatim to produce the disk and plans to license other media vendors as well.

Of the three products, Toshiba offers the most inexpensive drive and media, but it also makes the lowest-capacity product. The company uses the exact same mechanics in its 2.95M-byte drive as it does in its 1.4M-byte drives. The PD-210 just has an increased bit density (34,868 bpi); the track density—135 tpi—is the same as the density on its 720k- and 1.4M-byte disks.

By keeping the track density constant, Toshiba claims to have produced a drive that can read and write 720k-byte disks, but skeptics don't believe the perpendicular-recording heads can reliably write the 720k-byte disks, which are based on longitudinal recording. The company has also demonstrated a 16M-byte drive that uses the perpendicular-recording technology, and a servo scheme for higher track density.

Insite also based its drive on standard 3½-in. floppy-disk-drive mechanics. A standard stepper motor performs the basic head movements. The head carriage, however, carries both a magnetic head for reading and writing data and an optical sensor adapted from CD-ROM technology. The optical sensor follows the optically inscribed tracks, which are essentially concentric circles defining magnetic tracks between adjacent circles. A servo motor mounted on the head carriage makes the finer head adjustments based on the optical feedback.

Adkisson believes Insite has

adopted the best of optical and magnetic technology in its drive. He points out that the optical technology from CD-ROMs yields a high track density at a low cost—the Floptical drive features 1250 tpi. Its recording density is 24,145 bpi.

Drive works with flawed media

Adkisson also thinks that manufacturers can produce media less expensively for the Floptical drive than for drives that use a magnetic-servo scheme. He claims the optical-inscription process costs less than magnetic-servo writing. And he points out that the Floptical drive can work with flawed media, whereas magnetic-servo drives require flawless media. The current Floptical drive can't read or write 720k-byte disks; Adkisson does admit that read/write compatibility is one of the company's goals.

Brier's drive can't read or write 720k-byte disks either. But Jack Taylor, Brier vice president of marketing and sales, doesn't believe a 20M-byte drive has to have read or write compatibility to succeed. Taylor claims that the 20M-byte 3½-in. floppy drive belongs to a product class that's different from 720k-byte drives, and that compatibility is unnecessary for these high-capacity products to gain broad acceptance. Taylor claims Brier engineers could add a read-only feature to the BR 3020 for 720k-byte disks in one quarter, but prospective customers have not requested such a feature.

Servo partitions media

The Brier technology revolves around recording a low-frequency servo signal that's located beneath the high-frequency data signal. A cross section of the media would show the magnetic coating on top of a substrate. Brier divides the magnetic coating into upper and lower halves. A servo writer records the servo signal in the lower half of the magnetic coating (adjacent to the substrate). The drive reads and writes a high-frequency data signal in the upper half of the coating.

A magnetic servo signal buried beneath the magnetic data *continuously keeps the 21.4M-byte Brier Technology BT 3020 drive on track and allows the drive to offer a 35-msec average-access time.*

Some 5¼-in. high-capacity floppy drives use a servo signal embedded at the start of each sector. Using its buried-signal technology, however, Brier can make use of the entire data surface of a disk. And the Brier drive can continuously monitor the servo signal. This technology yields a track density of 777 tpi and a recording density of 26,000 bpi. Brier also employs zone-bit recording, which increases the number of sectors per track of the outside tracks in comparison with those of the inside tracks.

The performance offered by the high-capacity 3½-in. drives also varies with the drive technology. For example, Brier's drive uses a closed-loop magnetic servo with a voice-coil actuator similar to Winchester drives and features an average seek time of 35 msecs. The Insite I325 based on a stepper motor performs an average seek in 65 msecs. Toshiba's PD-210 has a 94-msec average seek time.

Physics affects transfer rate

The recording density, encoding scheme, and rotational speed of the drives determine their respective data transfer rates. The Toshiba PD-210 uses modified FM encoding, rotates the disk at 300 rpm, and transfers data at 1M bps (2 times the speed of a 720k-byte drive and 4 times the speed of a 1.4M-byte drive).

Both the Insite and Brier drives use a run-length-limited (RLL) code to encode data, and both offer a rotational speed of 720 rpm. The Insite Floptical drive offers a 1.6M-bps transfer rate. And Brier's BR 3020 transfers data at 2.2M bps.

The electrical interface of each drive also affects performance. Toshiba has simply modified the standard floppy-disk drive interface by adding an additional mode signal on an unused pin. A single signal currently lets you select either a 720k-byte or a 1.4M-byte operating mode. And a new signal lets you select the 2.95M-byte mode. Toshiba offers a disk-control chip set compatible with the industry-standard NEC 765; the set can handle the 2.95M-byte drive. A controller built for the 2.95M-byte drive can also handle 720k-byte and 1.4M-byte drives.

SCSI speeds transfers

Both Brier and Insite include a SCSI (Small Computer Systems Interface) controller embedded on their drives. The Insite I325 can transfer data from its buffer across the SCSI bus at 2M bytes/sec. Brier's BR 3020 offers SCSI transfers at 1.25M bytes/sec. The intelligence built into the SCSI-based drives will at some point let Brier and Insite offer features such as read-ahead caches that effectively increase the drive transfer rate to the SCSI transfer rate.

Interfacing is also an important issue. IBM-compatible personal computers, for example, currently use the standard floppy-disk drive interface like the one on the Toshiba PD-210. Of course, you must have a controller that can handle the 2.95M-byte drive, but once you have that, the PD-210 can work with all IBM-compatible operating systems and hardware environments.

In order for the SCSI-based

For more information . . .

For more information on the floppy-disk drives discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Brier Technology Inc
2363 Bering Dr
San Jose, CA 95131
(408) 435-8463
Circle No 735

Irwin Magnetics
2101 Commonwealth Blvd
Ann Arbor, MI 48105
(313) 996-3300
Circle No 737

Toshiba America Inc
Disk Products Div
9740 Irvine Blvd
Irvine, CA 92718
(714) 583-3150
Circle No 738

Insite Peripherals Inc
2363 Calle del Mundo
Santa Clara, CA 95054
(408) 727-8484
Circle No 736

drives from Brier and Insite to work with IBM-compatible systems, they need some type of driver. IBM products do not now support SCSI-type devices. So Insite and Brier will either have to provide emulation of the interrupt-13 hard-disk controllers prevalent in IBM-compatible personal computers, or provide an installable device driver. As new operating systems like OS/2 emerge that may require different driver software, both companies do plan to offer the appropriate software support.

Although you also need a SCSI host adapter to support the Insite or Brier drives on an IBM-compatible personal computer, Apple includes SCSI as the primary mass-storage interface in its Macintosh. But Apple does not support the industry-standard floppy-disk interface. Your system architecture may also dictate a preference for one of these interfaces.

Capacity will increase

In the next few years, you can expect even higher-capacity floppy-disk drives that offer even faster performance. Toshiba attempted to minimize the hardware/software impact of upgrading to a new floppy by starting at 2.95M bytes. And that company is aggressively trying to make the PD-210 an industry standard. It hopes to license Teac and Matsushita to produce the drives. Toshiba does have plans for higher-capacity drives as well.

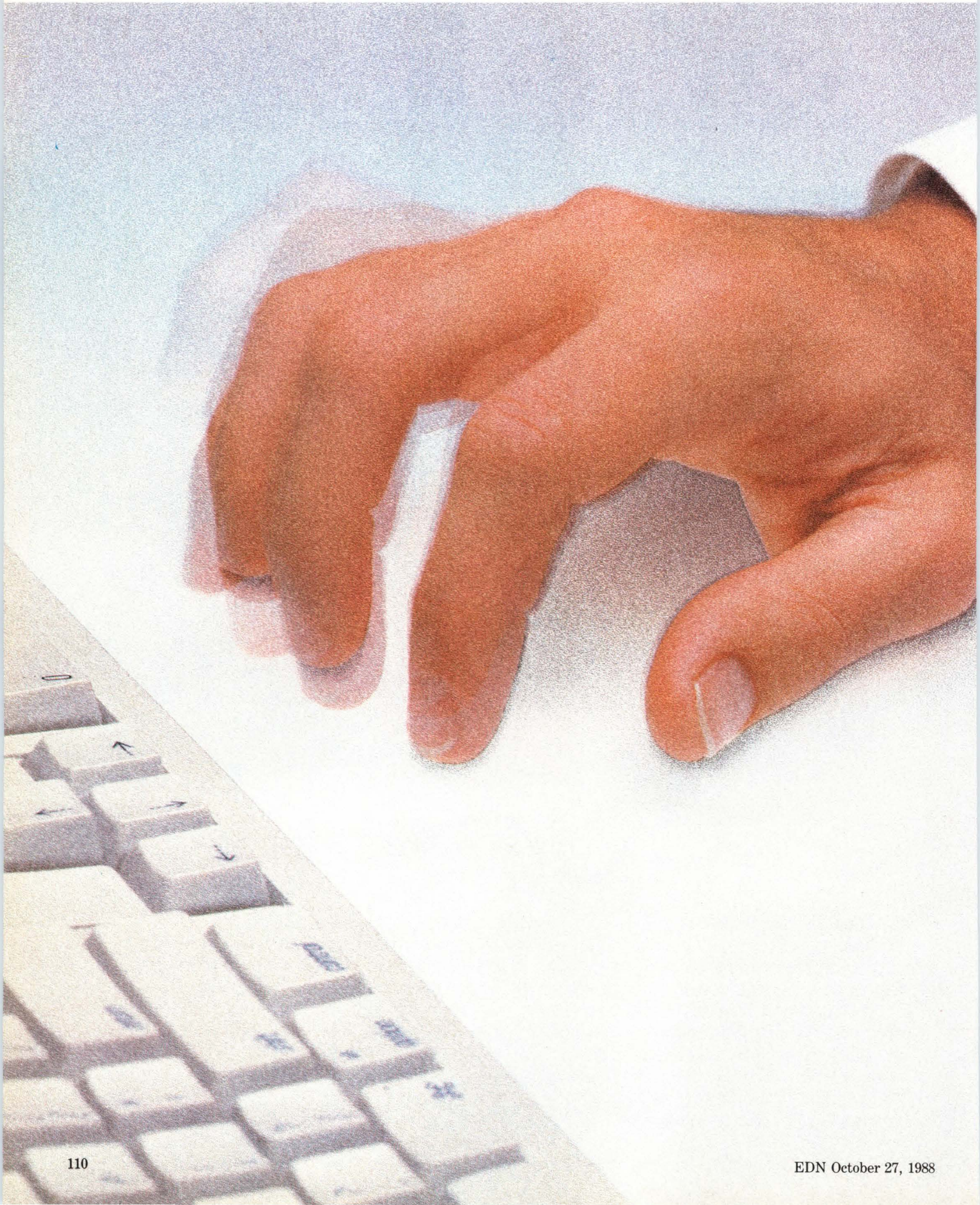
Brier's Taylor and Insite's Adkisson believe that 2.95M bytes is too small an increase to encourage customers to buy the new drives. Although Toshiba has made the biggest increase in recording density of the three, Brier and Insite have both engineered workable ways to boost track density—and you can't design 20M-byte or higher-capacity drives without the schemes for increased track density. According to Adkisson, the Floptical technology will support even higher track densities and will produce a 100M-byte floppy drive within a couple of years. EDN

Reference

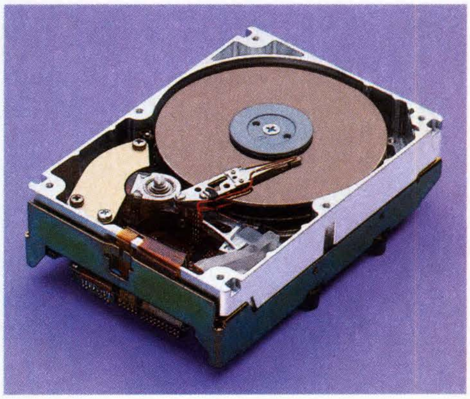
Wright, Maury, "Floppy-disk drives store 3M to 20M bytes in niche applications," *EDN*, July 23, 1987, pg 88.

Article Interest Quotient
(Circle One)
High 518 Medium 519 Low 520

ProDrive. Because



you can't afford to hurry up and wait.



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Transfer Rate (MB/sec)		
AT-Bus	4	4
SCSI Sync	4	—
SCSI Async	2	2
MTBF (hours)	50,000	30,000

*These are the best individual specifications of competitive drives. (This is not a real product.)

**Average seek time with DisCache is 12 ms in typical applications. (All specifications subject to change.)

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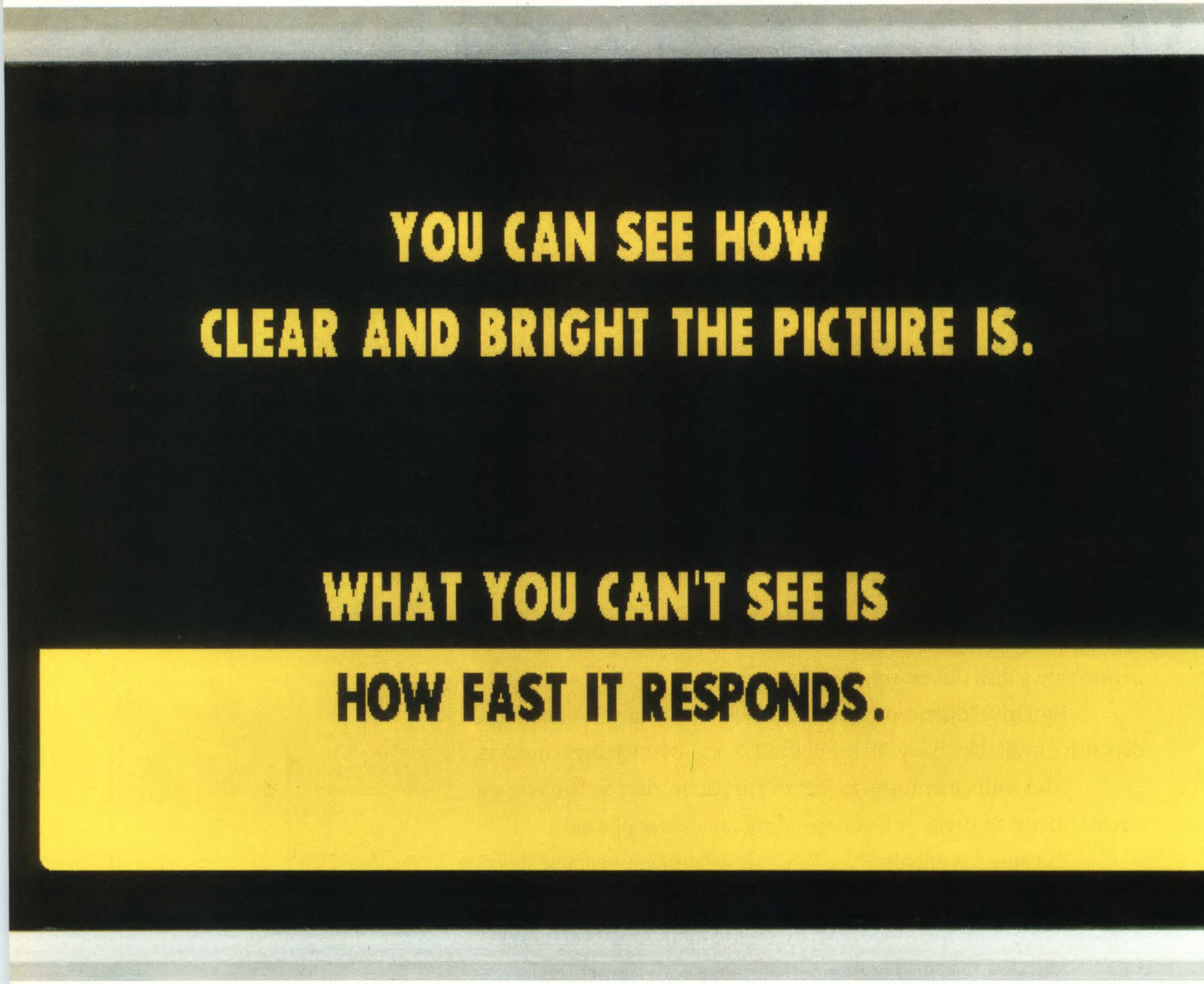
Quantum

Quantum Corporation, 1804 McCarthy Blvd., Milpitas, CA 95035 Western Region (408) 980-8555 Eastern Region (603) 893-2672
Europe (49) 69-666-6167 Authorized Distributors: Arrow (800) 777-ARROW Marshall (800) 522-0084

CIRCLE NO 117



Fast response time, less than 5 ms, gives Finlux Electroluminescent displays video capability. In laptop PCs, the cursor is visible during all rapid movements or data changes.

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FINLUX Display Electronics
Box 46
SF-02201 ESPOO 20, FINLAND
Telephone (+358-0) 420 01
Telecopy (+358-0) 422 143
Telex 125023 ldis sf

In the USA:
FINLUX INC.
20395 Pacifica Drive
Suite 109
Cupertino, CA 95014, USA
Telephone (408) 725-1972
Telecopy (408) 996-7547

CIRCLE NO 118

Mix business with pleasure at Munich's Electronica

Peter Harold, *European Editor*

Electronica '88, which takes place in Munich, West Germany, from November 8 to 12, is Europe's largest exhibition for electronic components and assemblies. It's also one of Europe's most international electronics exhibitions, with exhibitors not only from Europe, but also from the United States and the Pacific Rim. The exhibition occupies 20 halls, each the size of an aircraft hangar; over 2000 companies from more than 30 countries will exhibit their products and services. As a result, it's an ideal opportunity to investigate what's new in the electronic-components market in general, and to see what your competitors are up to. But Electronica is huge, so if you only plan to be at the exhibition for one or two days, plan your visit carefully. If you have more time, you can also enjoy the culture and history of Munich.

For companies from member countries of the European Economic Community (EEC), the Electronica '88 exhibition, and next year's Salon des Composants exhibition (Paris, France), have special significance. These two exhibitions will be those companies' first real opportunity to exploit the single European market, which will come into being between now and 1992. Although the EEC has always fostered close ties between member countries, European markets have remained fragmented. Individual member countries have been able to protect their indigenous industries by imposing hidden trade restrictions—such as import licensing or stringent product-testing requirements—in order to make foreign goods less competitive.

For EEC countries, 1992's single European market promises to change this situation. Under the terms of the Single European Act, set out by the European Parliament, all such trade restrictions between EEC member countries must cease, giving all those countries equal access to each other's markets. As a consequence, companies from countries within the EEC will be able to compete in much larger markets and take advantage of the economies-of-scale that ensue.

From a worldwide perspective, any single EEC country represents only a few percent of the electronic-components market. When combined, however, they make up around one-third of the world market for electronic components—ahead of Japan, and second only to the USA. Although a market of this size will greatly encourage competition within the EEC, it may actually discourage competition from companies based outside the community. Theoretically, these companies might find trade barriers erected around the consolidated European market—barriers that could be much harder to surmount than those currently established by its individual members.

In spite of the far-reaching business implications of the single European market, Electronica's associated conference program devotes itself largely to technical matters. Four separate conferences accompany the exhibition—the 13th International Conference on Microelectronics, the 4th International Macroelectronics Conference, the Sensorik Technical Sessions, and the Symposium on Quality Assurance in the Field of Electronics. Participants may present their conference papers in either English or German, but all the conferences feature simultaneous English-to-German or German-to-English translation facilities.

The International Conference on Microelectronics takes place on the afternoon of Monday, November 7, and the morning and afternoon of Tuesday, November 8. The conference is a mix of contributed papers and lectures from invited speakers. Topics for contributed papers include data-acquisition and signal-processing systems, new packaging concepts, and the role of gallium arsenide devices in future information and communications technology.

The Macroelectronics Conference, which spans November 9 and 10, covers areas of electronics that primarily use discrete components and power-control devices. Contributed papers focus on the solutions to practical problems, and the topics for discussion include switched-mode and uninterruptible power supplies; dynamic motor drives and motor-speed control; interfaces between microelectronic and power devices; and line-supply distortion.

The Sensorik Technical Sessions also take place on November 9 and 10. The first session, on Wednesday afternoon, examines sensors designed for use in mass-produced electronic equipment, and the second session, on Thursday morning, discusses geometric and mechanical techniques for evaluating and testing electronic components.

The Symposium on Quality Assurance, on Friday, November 11, focuses on the legal implications of the zero-defect policies that are currently offered by component manufacturers. The symposium includes

experts from industry and the legal and insurance professions.

If you'll be at Electronica all week, you should have more than enough time to attend one or more of the conference sessions. Conference fees, which include conference documentation, the exhibition catalogue, and entrance charge, are DM 355 for the Microelectronics Conference; DM 420 for the Macroelectronics Conference; DM 250 and DM 230, respectively, for the first and second of the Sensorik Technical Sessions; and DM 340 for the quality-assurance symposium. Half-day tickets for the Microelectronics Conference, which don't include documentation packages or the exhibition catalogue, are available for DM 150. You ought to book in advance, or immediately after you arrive at the exhibition.

Unlike many of Europe's exhibition sites, Munich's Messegelände trade-fair center, where Electronica '88 will be held, is in the heart of the city. So whether you arrive in Munich via rail or air, you can reach the exhibition within 20 minutes. From the Hauptbahnhof, Munich's main railroad station, you can easily walk to the center. Take a right out of the station along Bayerstrasse and then a left into Martin-Greif-Strasse. The Theresienwiese is straight ahead of you. Popularly known as the Wies'n, it's used each year for the city's world-famous Oktoberfest folk and beer-drinking festival. To the right of that is the Messegelände. If you opt for the subway from the main station, take the U-5 subway westbound, get off two stations later, and you'll be at the exhibition.

From the airport you can take a 15-minute taxi ride (unless you arrive in the morning rush-hour when it could take at least 30 minutes), or use the airport shuttle bus, which departs every 20 minutes between 8 and 11 AM and between 3:30 and 7 PM, to take you directly to the exhibition. If you come by car, there's plenty of parking space on the Theresienwiese and on other sites around the exhibition ground.

Because the Electronica exhibition is in the heart of Munich, it's easy to escape the rigors of exhibition walking to take in the pleasures of the city. Getting around is simple. You can use the S-Bahn or U-Bahn subway systems, as well as streetcars and buses. And you don't have to buy separate tickets for each type of transportation—the strip tickets (which you can purchase wherever you see the white and green K symbol) are valid on all three kinds of mass transit. Just cancel the appropriate number of ticket sections for each journey in the machines provided. Or you can use the city's taxis.

Munich is a city that has a great deal to offer within a small area. By strolling through the pedestrianized center of the old city from Karlsplatz through Neuhauser Strasse and Kaufingerstrasse to the open square of the Marienplatz, you'll pass several historic buildings. These include the German Renaissance church of St Michael, which houses the crypt of the Wittelsbacher princes; the magnificent Frauenkirche cathedral, which dates back to 1488; and Munich's City Hall, which features a glockenspiel clock where, at 11 AM daily, carved figurines perform and bells chime. Along this stretch, you can enjoy Munich's street performers, who'll keep going all day if a few deutsche marks appear in their cap at the end of each show.

A left turn after the Marienplatz into Burgstrasse takes you up toward the Residenz. This complex of buildings, dating from the 16th to the 19th century, illustrates European cultural development, mirroring Renaissance, Baroque, Rococo, and Neoclassic styles. On the way, you'll pass through the Alter Hof—the 13th century palace of the Bavarian dukes—where you'll find a largely unchanged medieval courtyard. The Residenz complex houses several museums that contain fine collections of porcelain, Egyptian art, and coins. Theatergoers can also check here on performances of the Bavarian State Opera, the Bavarian State Theater, and the Cuvilliés Theater.

When the light fades, you can retire to one of Munich's many restaurants. Try at least one beerhall, where you can drink Bavarian beer and eat Bavarian food until you're once again fit to tramp the exhibition halls of Electronica '88.

What follows is a selection of products which will be launched or exhibited for the first time at this year's Electronica exhibition.

Article Interest Quotient
(Circle One)
High 500 Medium 501 Low 502

For more information . . .

For more information on the Electronica '88 exhibition and its associated conference program, contact the following organizers directly.

Münchener Messe- und Ausstellungsgesellschaft mbH
Messegelände
Postfach 12 10 09
8000 Munich 12, West Germany
(089) 51070
TLX 5212086

For assistance in obtaining accommodations, contact the following organizations directly.

Fremdenverkehrsamt
Sendlinger Strasse 1
8000 Munich 2, West Germany
TLX 524801

MesseReiseService
Heidemannstrasse 220
8000 Munich 45, West Germany
Phone (089) 32304244
TLX 5213969
FAX (089) 3232594

Token-bus controller IC simplifies MAP network interfaces

In conjunction with the company's SAB82511 token-bus modem, the SAB82510 token-bus controller IC implements a 1M-, 5M-, or 10M-bps carrier-band network interface that conforms to the IEEE 802.4 standard. It's designed to work in equipment that connects into MAP (Manufacturing Automation Protocol) or Proway factory automation networks. You can also interface the token-bus controller with a broadband modem.

The SAB82510 performs OSI-model layer-2 media-access-control functions. It communicates with its host-system processor via shared memory and uses high-level commands that you can link into chained command blocks.

A 10-channel on-chip DMA controller maximizes throughput. This DMA controller supports the command block chain, four prioritized levels of transmit-frame data chain, four prioritized levels of receive-frame data chain, and the IEEE 802.4 immediate-response mechanism.

The controller's host interface is pin-programmable to operate on an 80186 or 68000 µP bus. However, you can interface the device to other µPs as well. The SAB82510 is a CMOS device that operates from a single 5V supply. It comes in a 68-pin plastic leaded chip carrier. Sample quantities, $94.

Siemens AG, Zentralstelle fur Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 620

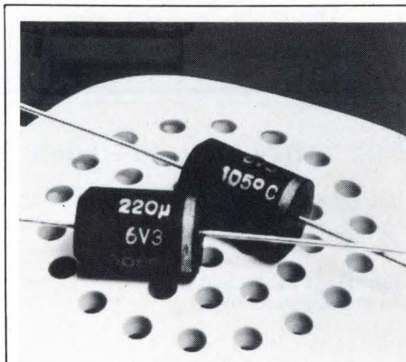
Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500. Hall 23, Stand A04.

Circle No 621

Long-life electrolytic capacitors save pc-board area

Series-138 aluminium wet-electrolytic capacitors are 50% smaller than traditional type-1 electrolytics, and feature an operating life as long as 15 years at 40°C. The series includes capacitors with nominal values in the range of 0.22 to 220 µF, and voltage ratings of between 6.3 and 100V.

A flame-retardant plastic seal, which is molded around the aluminum casing, largely accounts for the devices' long operating life. This seal prevents drying of the electrolyte and protects any adjacent circuitry from short circuits. A high-temperature electrolyte gives the devices an operating temperature range of −55 to +105°C. Their useful lifetime at 105°C is at least 2000 hours.



The capacitors meet reliability tests comparable to those specified in DIN-41257. Their basic specification conforms to the IEC/384-4 long-life capacitor specification, and they are suitable for use in climatic category 55/105/56. Series-138 capacitors are axially leaded, and are packaged in 6.3- or 7.7-mm diameter cases with a length of 12.7 mm. They are supplied on bandoleers, in boxes, or on reels. Under gld 0.50 in large quantities.

Philips, Components Division, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 757189. TLX 51573.

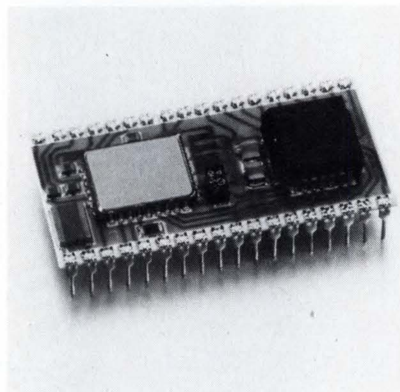
Circle No 622

Mepco/Centralab Inc, 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (305) 881-3200. Hall 24, Stand B02.

Circle No 623

Telephone ICs suit both ends of the subscriber line

Integrating a monolithic subscriber line interface (SLIC) and a codec/filter IC into a single 36-pin hybrid DIP, the PBA3276/1 handles all the battery-feed, supervisory, and voice-transmission functions required in a digital PABX or hybrid key telephone system. The circuitry can operate from a battery voltage as low as −24V.



The device provides a terminating impedance of 600Ω and achieves a longitudinal-to-metallic balance of 70 dB typ (63 dB minimum). Its codec interfaces directly to a pulse-code-modulation highway, and features selectable μ-law or A-law coding schemes, programmable transmit and receive gains, and programmable hybrid balancing. The PBA3276/1 costs $20 (5000).

Suitable for use in telephone handsets, the PBL3726/19 telephone speech-circuit IC features soft clipping to reduce distortion at high speech levels. Automatic gain control reduces the gain of the transmit amplifier by as much as 5 dB when the ac signal on the telephone line increases to 2V peak.

The circuit performs 2- to 4-wire conversion and automatic loop-loss compensation. The PBL3726/19 is supplied in an 18-pin DIP. A surface-mount version should be available by the end of the year. $1.40 (10,000).

Ericsson Components AB, Microelectronics Division, Isafjordsgatan 16, 16481 Kista-Stockholm, Sweden. Phone (08) 7574354. TLX 8125008. FAX 08-7526034.

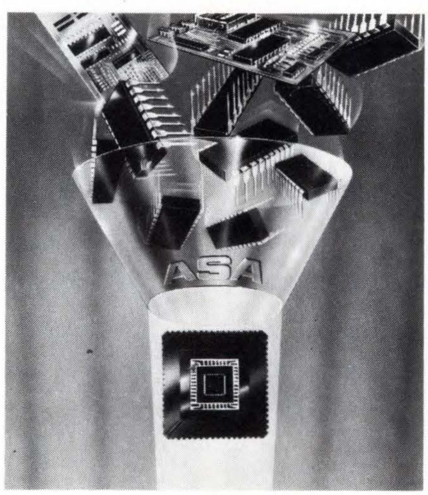
Circle No 626

Ericsson/Rifa Inc, 403 International Pkwy, Richardson, TX 75083. Phone (214) 480-8300. FAX 214-680-1059. Hall 25, Stand D07.

Circle No 627

Foundry-independent silicon compiler simplifies ASIC design

The ASA silicon compiler reduces the complexity of ASIC design to a level at which system designers can undertake the design of custom ICs from start to finish. In addition, it makes IC design independent of any particular semiconductor process or technology. During the design process you can also generate test patterns and evaluate your design for testability.



The compiler's hardware-description language allows you to describe both the function and structure of an IC design in a hierarchical form. As a result, you can adopt a top-down approach to IC design. All the relevant information about transistor-level circuit design is already built into the compiler. From the outset, the ASA compiler generates layout information that the compiler's logic editor and simulator take into account as you use them.

Version-I of the compiler includes a cell library of SSI and MSI logic functions. Version-II will include cells for regular structures such as RAM, ROM, and PLAs. You can create macrocells from this library, or add your own cells to it. The ASA compiler runs on DEC VAX computers under the VMS operating system. Its open-system software structure allows you to interface a variety of existing CAD tools to it. From around gld 360,000 to gld 900,000.

Sagantec BV, Kemenade 12b, Son, 5600 CC Eindhoven, The Netherlands. Phone (04990) 77117. TLX 59163. FAX (04990) 73297. Hall 14, Stand C04.

Circle No 625

ISDN chips provide single-chip solutions for S and U interfaces

Packaged in a 22-pin plastic DIP, the MTC2072 provides a single-chip solution for interfacing equipment to the S interface of an ISDN network. The device uses the AMI line code, and conforms to CCITT recommendations I.430 for the 4-wire S-interface between subscriber terminals and network termination units. The interface connects to a passive network bus, which provides separate receive and transmit loops that operate at 192k bps. You can connect as many as eight terminals to the network bus, which incorporates collision protection to prevent more than one terminal from accessing the bus at any one time.

For U-interface applications, the MTC2071 provides a single-chip solution for interfaces to ISDN networks that use the 4B/3T line code. The device uses an internal DSP adaptive filter to provide echo cancellation and equalization. You can use the device on a telephone line as long as 8.2 km, and you can configure it for use at a number of different locations within an ISDN network. These locations include line termination (LT) equipment, network termination (NT) equipment, PABX and subscriber modules, and up- and downstream repeaters.

The MTC2071 is expected to sell during 1989 for $185, and to fall to less than $50 (1000) during 1990. The MTC2072 should sell for $9.50 during 1989 and $7.50 (1000) during 1990.

Mietec, Westerring 15, 9700 Oudenaarde, Belgium. Phone 55332211. TLX 85739. FAX 55318112. Hall 19, Stand B07.

Circle No 624

Single-chip CMOS tone detector facilitates call-charge metering

The FX611 tone-detector IC detects the call-charge metering pulses transmitted during telephone calls. It is suitable for use in subscriber private metering (SPM) systems in PABX or general pay-phone equipment, and is programmable to operate on either 12- or 16-kHz SPM systems.

In addition to selecting the frequency of the detected tone, you can also select the FX611 to operate in one of two tone-detection modes. In tone-follower mode, the device outputs a logic 0 whenever it detects a tone of the correct frequency. In the SMP-packet mode, the detector's output is activated only when a tone-burst meets specified mark and space timing.

All frequency timing within the device is controlled by an external crystal, and an internal op amp allows you to adjust the gain of the tone input. The FX611 is fabricated in CMOS and draws a maximum supply current of 3.5 mA from a single 5V supply. It is available in either a 16-pin ceramic DIP or a 24-pin plastic, gull-wing or J-lead, surface-mounted chip carrier. Around £3 (1000).

Consumer Microcircuits Ltd, 1 Wheaton Rd, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382. FAX (0376) 518247.

Circle No 628

Mx-Com Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (919) 744-5050. Hall 25, Stand A04.

Circle No 629

IF YOU'RE WASTING TIME LOOKING FOR THE BROADEST LINE OF SMD® PASSIVES,

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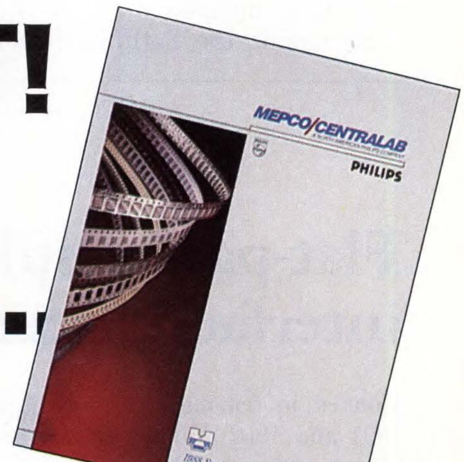

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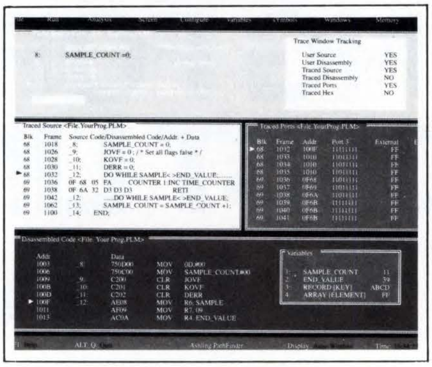
CIRCLE NO 120

Emulator's window environment traces source-code and assembler

Used in conjunction with the company's CT-series of PC-based 8-bit in-circuit emulators, the ViewFinder emulation-control software and PathFinder system-debug software provide you with a window environment in which you can simultaneously trace programs at both the assembler and source-code level.

Using ViewFinder you can select the content, size, and position of the windows that are displayed, allowing you to simultaneously follow logically connected areas of your system. In addition, you can maintain windows that are not displayed as virtual windows, which can continue to be updated.



By adding the PathFinder software package and a suitable compiler you can trace program activity at all software levels. To capture elusive program bugs, PathFinder allows you to perform continuous trace-and-compare operations. PathFinder is currently available for use with a PL/M-51 compiler or a C compiler for the 8051 μC, but versions that run with C compilers for 68HC11, Z80, and 64180 μPs are scheduled for release between now and the first quarter of '89. ViewFinder is supplied free-of-charge with new development systems or as a $275 upgrade for existing users. PathFinder costs from $1250 to $1500.

Ashling Microsystems Ltd, Plassey Technological Park, Limerick, Ireland. Phone 061-334466. TLX 70357. FAX 061-334477. Hall 20, Stand D22.

Circle No 630

Flat-pack display drivers interface directly to CRTs

Housed in flat-pack packages, the 1901 and 1902 display driver modules accept a low-level video input signal and are capable of directly driving the cathode of a high-speed CRT. The 1901 is capable of maintaining a bandwidth of greater than 146 MHz when driving a 50V p-p signal into a 6-pF load. The 1902, which incorporates an additional output stage, can drive 100V p-p output signals into a 20-pF load.

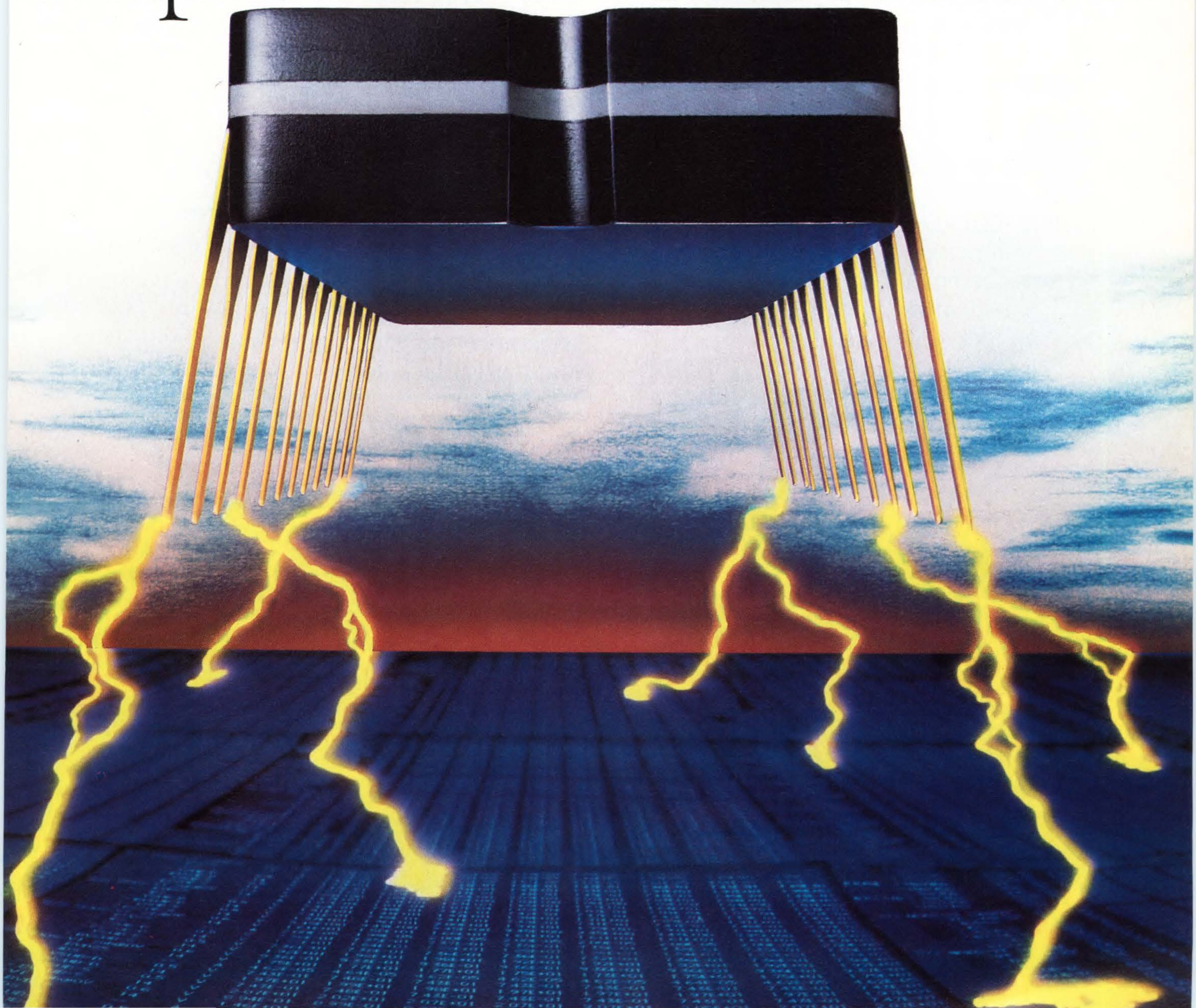
Both devices operate as transconductance amplifiers. They have differential inputs that you can configure for differential or single-ended, positive or negative video operation. These inputs have a common-mode voltage capability of 3V, and will accept an RS-343 or RS-170 video signal.

Analog inputs are also provided that control the gain and output-offset of the amplifier, allowing you to adjust display contrast and brightness, respectively. The modules have a 5.5V reference output. The gain control provides overall gains of between 0 and 80, and the offset control allows you to vary the quiescent output current from several microamperes to 100 mA.

The 1901 is housed in a 24-pin flat-pack with a 1×1-in. footprint. The 1902 is housed in a 30-pin flat-pack with a 1×1.5-in. footprint. They are available in version with commercial or military operating temperature ranges. The 1901 commercial grade, $124; military grade, $229 (100); 1902 commercial grade, $291; military grade, $366 (100).

Teledyne Philbrick, 40 Allied Dr, Dedham, MA 02026. Phone (617) 329-1600. TLX 212711. FAX (617) 326-6313. Hall 25, Stand B06.

Circle No 631



What do you get with Power MOSFETs that have 2.3 million cells per square inch and 0.023Ω R_{DS} (on)?

Specify the 50V/52A STVHD90 and get everything you need for high efficiency power conversion and motor control systems—including the power to win.

The STVHD90's breakthrough performance puts you ahead of the pack with the industry's best ratio of current capability to gate charge packed in a space and cost-saving TO-220 package.

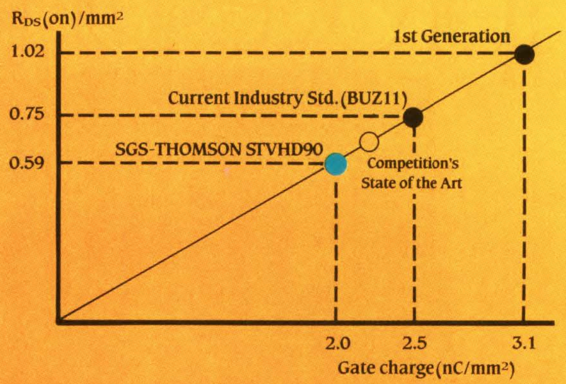
Plus, SGS-THOMSON saves you even more with the ISOWATT220™, a unique package option that's fully isolated to 2000V DC.

No one backs you with a better combination of cell density, on resistance (0.023 ohms max.) and low gate charge (56 nC typical).

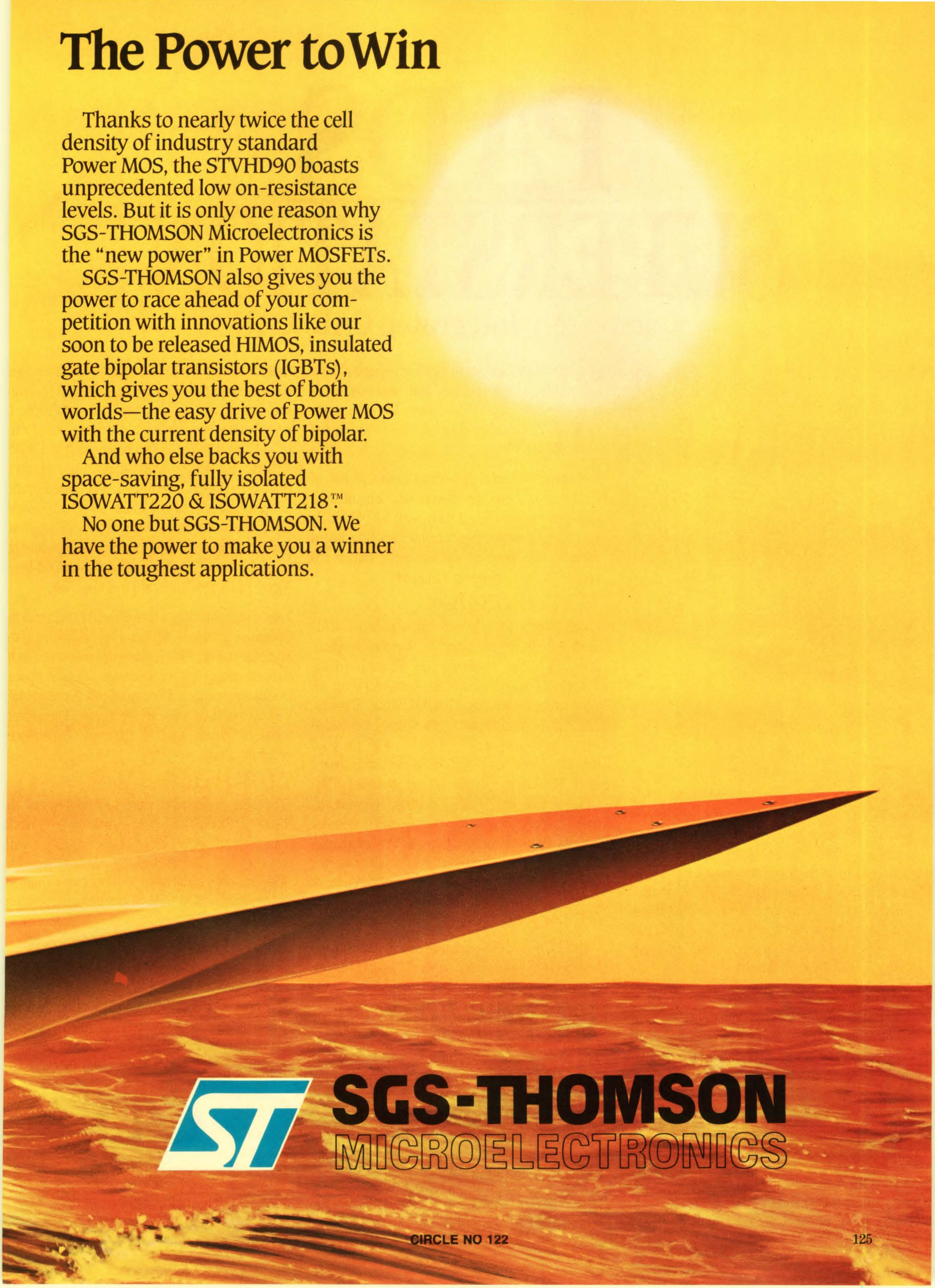
Add up the advantages. Lower gate charge means less energy needed to drive the ultra-fast switching STVHD90. High transconductance means more drain current for a given gate voltage. Lower source drain diode V_{SD} means better free wheeling.

Compare the STVHD90 with the competition's best. SGS-THOMSON gives you the winning edge in virtually all applications, including automotive body controls, DC/DC converters, stepper motors, switching power supplies, synchronous rectifiers and more.

Get the facts and you'll get The Power to Win. For a comprehensive set of data sheets and tech notes, call 602/867-6259 or write: SGS-THOMSON Microelectronics, 1000 E. Bell Road, Phoenix, AZ 85022.



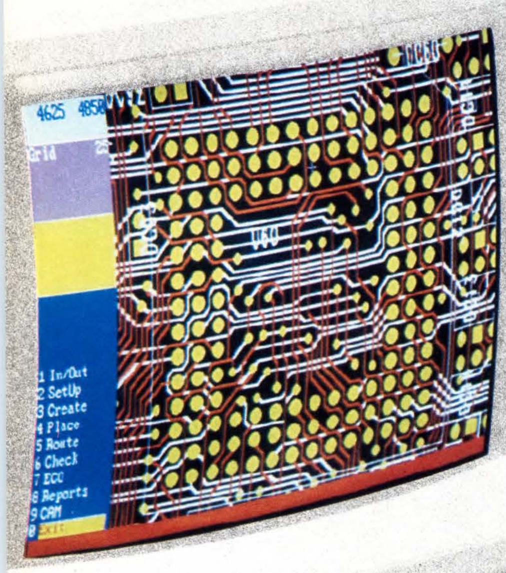
The Very High Density SGS-THOMSON STVHD90 (Blue dot) has a lower "R_{DS} On" resistance and gate charge than industry standard (Black dot).


The Power to Win
Thanks to nearly twice the cell density of industry standard Power MOS, the STVHD90 boasts unprecedented low on-resistance levels. But it is only one reason why SGS-THOMSON Microelectronics is the "new power" in Power MOSFETs.
SGS-THOMSON also gives you the power to race ahead of your competition with innovations like our soon to be released HIMOS, insulated gate bipolar transistors (IGBTs), which gives you the best of both worlds—the easy drive of Power MOS with the current density of bipolar.
And who else backs you with space-saving, fully isolated ISOWATT220 & ISOWATT218™?
No one but SGS-THOMSON. We have the power to make you a winner in the toughest applications.
SGS-THOMSON
MICROELECTRONICS
CIRCLE NO 122

See us at Wescon Booth #'s 3669, 3671, 3768, 3770

PADS SUPERSTATION™

Completely Integrated CAE/CAD



The Integrated PADS-Superstation™ is a new and powerful PC-Based Design Station that allows the Engineer or Circuit Designer to perform the entire design sequence from cradle-to-grave. Every decision required in the design effort, from Logic Capture to Printed Circuit Design, to 100% Connection Routing, to Checking, to generating Manufacturing Aids is made by the responsible engineer and implemented on a single, fully integrated CAE/CAD SUPERSTATION!

LOGIC CAPTURE

The PADS-CAE system maximizes Logic Capture automation, while allowing the engineer to concentrate on the design task. This high degree of automation results from the use of a new type of database: A Design-Oriented-Database. All drawing sheets of the design are simultaneously available - not merely a single sheet, as with most other Logic Capture systems.

Among the many advantages of this new database are Automatic (hands-off) entry of Reference Designation, gate and pin data, on-line real time data checking across all drawing sheets, rapid paging from sheet-to-sheet, and instantly available (no batching) Annotation Lists to both PADS-PCB and other board CAD systems using FUTURE NET™.

The most tedious and error-prone phase of Engineering Documentation, i.e., Engineering Change Order (ECO), is easy with PADS. ECOs generated in either the Schematic, or the Board database are used to automatically (hands-off) update the corresponding database.

BOARD DESIGN

PADS-PCB is today's most popular board CAD System and is the heart of the Superstation. PADS-PCB has revolutionized Printed Circuit Board CAD expectations by demonstrating an alternative to today's $100,000 Work Stations. Thousands of designers, engineers, and Board Design Centers use PADS-PCB - and for good reasons: 1 mil resolution, 30 layers, large board (over 400 14 pin ICs per board), complete SMD support, fine line (1, 2 & 3 tracks between IC pins), both Analog & Digital capability, fast Air Gap & Data checking, Gate & Pin swapping, dynamic rubber banding, rats' nest display, interactive and auto placement, interactive & auto routing, and all required Manufacturing Aids (CAM).

PADS-PCB is tightly coupled, both to and from PADS-CAE, and from other Logic Capture systems using FutureNet™.

100% COMPLETION AUTOROUTING

The most demanding phase of board design is routing the connections; approximately 70% of the board design effort is spent in this time consuming, labor-intensive task. Every Designer and Engineer's dream is to have a 100% completion autorouter, and PADS-Superrouter™ brings this capability to the Superstation™.

Here's how it works: the Designer places the components on the board, selects the "Route" command, and the SUPERROUTER takes ove routing around the clock, hour after hou performing this tedious task to completion, c near completion, while the Designer is involve in other tasks. It's that easy! PADS Superrouter allows the designer to set up routing strategy based upon the requirement of each board. A costed Maze Search algorithm using obstacle hugging on a 10, 20, 25 or 50 m grid, and up to 12 simultaneous layers attempt to achieve 100% completion. A Rip-up-and-Retr Algorithm is used to obtain this objective.

Following routing, an Ease-of-Manufacturin Optimizer prepares the board for maximizing th manufacturing yield. Bends and curves put in b obstacle hugging are removed, closely space tracks are unpacked, corners are made at 45° and all possible Vias are removed. The result equal or exceed that of the most experience board designer.

LOW PRICE

While the performance and functionality of th PADS-SUPERROUTER is equal to any Work station at any price, its price is competitive wit the very low cost PC-based CAD systems. Th price has been structured to allow every enginee in the organization to have his/her own persona SUPERSTATION™.

EVALUATION PACKAGE

So that you can appreciate the impact the PADS Superstation™ will have in your organization, w have created a Superstation Evaluation Package It is available at no cost to qualified engineers and designers. Please call our Sales Departmen at (800) 255-7814; Inside Mass. (508) 486-9521.

CAD Software, Inc.
Suite #6
119 Russell Street
Littleton, MA 01460

FutureNet is a registered trademark of Data I/O Corp.

CIRCLE NO 123

I/O CONTROLLER

The SAB82525 is a functionally enhanced version of the SAB82520 high-level serial communications controller. The controller provides two HDLC channels, each provided with its own clock oscillator, baud-rate generator, digital phase-locked loop, and time-slot alignment circuitry. In addition to OSI-model layer-1 functions, the controller's on-chip link-access-procedure (LAP) controller handles several layer-2 functions, including flag insertion and detection, bit-stuffing, CRC generation and checking, and address field recognition. The controller can handle serial I/O data rates as high as 4M bps. The SAB82525 supports X.25 LAP-B, ISDN LAP-D, and SDLC (normal response mode) protocols.

Communication with a host processor system is via a µP bus that is pin-programmable to operate as either an Intel-style multiplexed bus or as a Motorola-style non-multiplexed bus. To maximize throughput, the controller has an on-chip 64-byte FIFO and a dedicated DMA-channel for the receive and transmit sections of each serial I/O channel. You can also program the controller to interrupt the host processor to initiate data transfers.

The SAB82525 is a CMOS device with a typical active power consumption of 25 mW and a standby power consumption of 4 mW. It is packaged in a 44-pin plastic leaded chip carrier and is expected to sell for around DM 25 (10,000) by 1990.

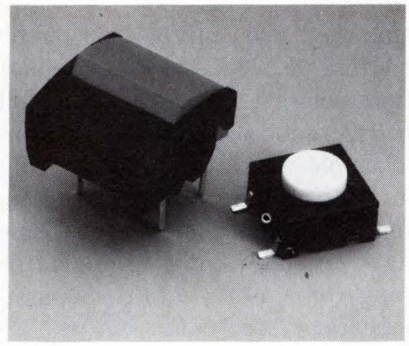
Siemens AG, Zentralstelle fur Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 610

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500. Hall 23, stand A04.

Circle No 611

SMD SWITCHES



These fully sealed miniature keyboard switches are suitable for surface mounting using pick-and-place equipment. They have a 10.1-mm-square footprint and a height of 6.4 mm. You can fit them with a range of standard or customized colored keycaps. The keycaps can incorporate a medium intensity LED indicator or high intensity illumination. The keyswitches have an operating force of 150 grams and provide 1 mm of switch travel with tactile feedback. $0.65.

Mec A/S, Box 26, Industriparken 23, 2750 Ballerup, Denmark. Phone (02) 973366. TLX 9125649. FAX (02) 681514. Hall 16, stand F34.

Circle No 612

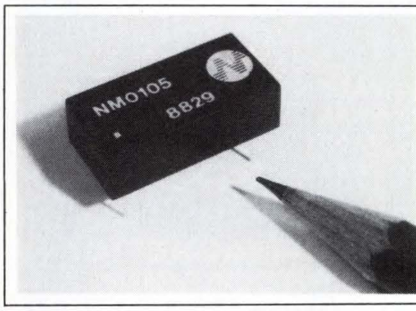
MOSFETS

RF power MOSFETs in the BLF500 range operate at frequencies as high as 500 MHz and include devices with power ratings between 2 and 150W. Compared to bipolar types, these MOS transistors feature lower wideband noise levels, greater tolerance of load mismatch, and freedom from thermal runaway and parasitic oscillation. In addition, you can drive them from a voltage source rather than a current source. In many applications there is no need for an output driver stage, and the ability to modulate the output power by modulating the MOSFET's gate voltage suits the devices for use in AM transmitters.

Devices with power ratings as high as 40W are available in sample quantities now, with production volumes available by the middle of 1989. Samples of the 100W and 150W devices will be available during the first half of 1989, with production volumes during the second half of the year. As a price guide, the 10W BLF543 is expected to cost between gld 50 and gld 60 (100).

Philips, Components Division, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 757189. TLX 51573. Hall 24, stand B02.

Circle No 613

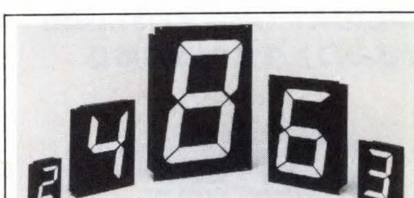


DC/DC CONVERTER

Suited for use in battery-powered hand-held equipment, the NM0105 dc/dc converter generates a 5V output from a 1.2 to 1.5V input. As a result, you can power equipment from one single-cell battery. The converter can deliver an output power as high as 200 mW. The NM0105 is packaged in a 7-pin DIP with overall dimensions of 20.3×10.2×7.1 mm (0.8×0.4×0.28 in.). Around £6 (100).

Newport Components Ltd, Tanners Dr, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (0908) 615232. TLX 825621. FAX (0908) 617545. Hall 1, stand A05.

Circle No 614

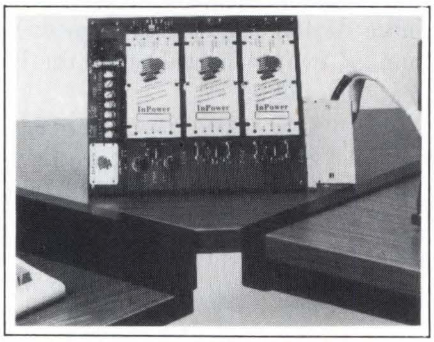


7-SEGMENT DISPLAY

The H-700 range of bi-stable, electromagnetic, 7-segment display modules can display any numeric character and selected letters and symbols. Available with digit heights of 10, 15, 25, 30, 45, or 58 cm, they are suitable for public-address displays and other applications where a high degree of legibility is required. The displays are available with white or yellow digits against a black background and feature aluminum casings. They have an operating temperature range of −40 to +70°C. Separate interface electronic boards are available. From around Fr 350 to Fr 1100 (100), depending on digit height.

Bodet SA, Box 1, 49340 Trémentines, France. Phone 41625528. TLX 722429. FAX 41629564. Hall 16, stand F06.

Circle No 615



EVALUATION BOARD

The IP-2361 and IP-2362 evaluation boards allow you to evaluate different configurations of the company's IP-series dc/dc converter and power booster modules. The boards accept as many as three IP-series modules configured to provide a single-, dual-, or triple-output power supply. Configured as a single-output 5V power supply, the board can deliver a current as high as 90A. Other single-, dual-, or triple-output configurations can deliver a total output power as high as 600W.

To assist accurate parametric testing, the board has oscilloscope jacks that are connected to appropriate points in the circuit. You can access the gating and output-voltage trimming connections for each module. You can also plug in the company's phasor modules, which allow you to introduce a constant phase angle between the switching cycles of each converter to minimize power-supply-generated noise.

The IP-2361 evaluation board accepts converter modules with input voltages of between 100 and 400V, and the IP-2362 board accepts converters that have input voltages of 100V or less. Irish Pounds, 115.

InPower Europe Ltd, Ballysimon Rd, Limerick, Ireland. Phone 061-49677. TLX 70322. FAX 061-42730. Hall 22, stand C16.

Circle No 616

ANALOG/DIGITAL ASIC

The Expert Array from Mietec allows you to subdivide a mixed analog/digital ASIC into sections that are implemented using standard cells and sections that are implemented using mask-programmable arrays of analog components and logic gates. You can define the size and functionality of the standard cell and the array sections, both of which are then integrated onto the same silicon die.

You can use the technique to produce standard-function parts that you can modify for different applications—for example, telephone ICs that you can adapt to different international standards. Or, you can use it to accelerate the prototyping phase of a custom design.

The initial non-recurring engineering (NRE) charges for the Expert Array are similar to those for normal standard-cell designs. However, if you implement circuit changes using only the analog and digital arrays, subsequent design iterations involve only the tooling and production costs you'd expect to pay for a gate-array product.

Mietec, Westerring 15, 9700 Oudenaarde, Belgium. Phone 55332211. TLX 85739. FAX 55318112. Hall 19, stand B07.

Circle No 617


We have solutions to your toughest microcircuit prob
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And many are coming right off our shelves.

For over twenty years, CTI has been providing design and manufacturing solutions for some of the most complex black box requirements in the most demanding markets—military and government, avionics, telemetry, navigation, communications, guidance and control systems, among others.

Our products range from custom hi-rel hybrid microcircuits, to Standard Electronic Modules (SEMs) in high-density configurations, to miniaturized subsystems for military and space applications. We have in-house hybrid and monolithic design, manufacturing, and technology expertise to convert the toughest requirements into high-performance microcircuits.

And we've used our experience to build a host of standard circuits. These pre-engineered "off-the-shelf" packages include MIL-STD-1553 standard data bus products, and MIL-STD-1397 interfaces.

One new standard product is the CT2100, a microprocessor controlled, quad solid state relay, with 1500 volt isolation. The circuit incorporates fully isolated switch status and built-in test functions, and operates from -55 to +125°C in military environments.

So, whether your project is in the early design stage or is approaching production, call on CTI. Solutions to some of your requirements may have to be invented. Others may already be on our shelves. We offer you the advantage of either—or both. Call or write us today.

See us at Wescon, Booth #2292-2294

CTI

Circuit Technology Inc.
160 Smith Street, Farmingdale, New York 11735
Tel: (516) 293-8686 Fax: (516) 293-8622

CIRCLE NO 125

Wescon/88 will focus on engineering workstations and automated design tools

At the annual show, you'll have the chance to attend conferences, evaluate products, and make contacts.

Clare Mansfield, *Associate Editor*

Wescon/88, running from November 15 to 17 at the Anaheim, CA, Convention Center, will have more than 1300 booths showcasing products from components and microelectronics to subassemblies and systems.

In addition to the traditional technical programs, tutorials, and business conferences, the show will incorporate three new aspects: an automated design center, a new-products and technology-achievement competition, and a Micromouse track. For the second year in a row, Wescon will also run computer-generated films in the Electronics Theater.

Motivated by industry prophecies that 90% of the electronic circuits designed by 1990 will be produced using some type of CAD, Wescon's sponsors this year decided to emphasize the concept of the automated design center. Under this umbrella, nearly 180 exhibitors will showcase their engineering workstations, CAD and CAE tools, and related design aids.

In the new-product contest, companies will compete in five categories: engineering workstations and design tools; instrumentation, test equipment, and control systems; production equipment; and components and microelectronics. Vendors will exhibit their new products in a special section of the convention center and will have an opportunity to elaborate on each product's technology and applications during scheduled forums.

Winning companies in each of the five categories will have a $10,000 scholarship awarded to a Southern California educational institution in their name. The IEEE will administer the scholarship; editors from technical publications around the country will judge the competition.

The third new aspect of Wescon will be the inclusion of a Micromouse track. Micromouse competitions have been gaining in popularity since their debut in 1979. In a Micromouse contest, self-contained robotic devices or mice race to be the first to find the center of a maze. Designers of the winning devices receive cash prizes, awards, and the chance to compete in the 1989 international competition.

Wescon/88 also offers plenty of opportunities for you to improve your technical knowledge. Thirty-six technical sessions are scheduled, ranging from ASICs to peripheral devices to neural networks (see **table**). You can attend these sessions at the Anaheim Hilton.

Further, for those engineers looking for detailed information on narrowly focused topics, 11 tutori-

Wescon/88®

als will be held at the Anaheim Marriott Hotel in conjunction with the show. These will include short courses on project and time management, fiber-optic systems design, grounding and shielding, and practical C programming. You must pay a fee for each tutorial.

Four business-oriented conferences will also convene at the Anaheim Marriott during Wescon. Discussions will cover distribution, purchasing, mergers and takeovers, and the importance of public relations in trade shows and promotion. The merger and takeover panel discussion is free; there is a charge for the other conferences.

You can obtain more information on Wescon/88 by calling Electronic Conventions Management at (213) 772-2965. Also look for EDN's extended Wescon coverage in the next issue. EDN

Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

WESCON/88 TECHNICAL-SESSION PROGRAM AT THE ANAHEIM HILTON HOTEL

		CALIFORNIA BALLROOM A	CALIFORNIA BALLROOM B	PACIFIC BALLROOM A	PACIFIC BALLROOM B	PACIFIC BALLROOM C
TUESDAY, NOVEMBER 15	9:00 AM TO 11:00 AM	(1) ADVANCED FLOATING POINT SOLUTIONS FOR 32-BIT MICROPROCESSORS	(2) SYSTEM LEVEL DESIGN SUCCESS WITH ADVANCED CMOS LOGIC	(3) VLSI SOLUTIONS FOR MICROCHANNEL INTERFACING	(4) SUCCESSFUL SYSTEM DESIGN TECHNIQUES USING ASICs	
TUESDAY, NOVEMBER 15	12:00 PM TO 2:00 PM	(5) MEMORY MANAGEMENT SCHEMES FOR TODAY'S COMPLEX COMPUTER ARCHITECTURES	(6) ADVANCED ECL—GENESIS OF A NEW ERA IN PERFORMANCE	(7) HIGH PERFORMANCE SCSI INTERFACE CHIPS	(8) ASIC MODULE COMPILATION/ CUSTOMER SPECIFIC CELLS	(9)* UPDATE ON THE SPACE STATION
TUESDAY, NOVEMBER 15	3:00 PM TO 5:00 PM	(10) SYSTEM DESIGN FLEXIBILITY OFFERED BY FLASH EPROM/EEPROM	(11) EMITTER COUPLED LOGIC (ECL)—SYSTEM SOLUTIONS FOR HIGH PERFORMANCE SYSTEMS	(12) MODEMS IN THE 1990's	(13) DESIGN FOR TESTABILITY; SYSTEM TESTABILITY IN LIGHT OF EMERGING TEST BUS STANDARDS	
WEDNESDAY, NOVEMBER 16	9:00 AM TO 11:00 AM	(14) DESIGN TECHNIQUES FOR INNOVATIVE PLD ARCHITECTURES	(15) MODERN PROGRAMMABLE STATE MACHINES	(16) INTEGRATED CIRCUITS' ELECTROMAGNETIC COMPATIBILITY		
WEDNESDAY, NOVEMBER 16	12:00 PM TO 2:00 PM	(17) PROGRAMMABLE LOGIC TESTABILITY—THE DESIGN IS DONE. . . NOW WILL IT WORK IN PRODUCTION?	(18) HIGH SPEED/HIGHLY INTEGRATED MICROCONTROLLERS AND THEIR APPLICATIONS	(19) SILICON CIRCUITS OFFER CIRCUIT DENSITY IMPROVEMENT	(20) THE USE OF PERSONAL COMPUTERS IN TEST AND MEASUREMENT APPLICATIONS	(21) NEURAL APPLICATIONS
WEDNESDAY, NOVEMBER 16	3:00 PM TO 5:00 PM	(22) SPECIAL-PURPOSE PROGRAMMABLE LOGIC DEVICES AND THEIR APPLICATIONS	(23) RISC SYSTEMS ENTER THE MAINSTREAM	(24) NEW TECHNOLOGY; PROTECTING IT AND PROTECTING YOURSELF	(25) SIGNIFICANT ADVANCES IN DATALOGGING	
THURSDAY, NOVEMBER 17	9:00 AM TO 11:00 AM	(26) MEETING THE NEEDS OF THE EE PROFESSION	(27) AUTOMATION OF SURFACE MOUNT MANUFACTURING	(28) GALLIUM ARSENIDE ICs FROM A USER'S PERSPECTIVE: PART I—STANDARD PRODUCTS	(29) PARALLEL COMPUTING AND MULTIPROCESSORS	
THURSDAY, NOVEMBER 17	12:00 PM TO 2:00 PM	(30) BUSINESS ISSUES FOR THE YOUNG HIGH-TECHNOLOGY COMPANY	(31) SOLVING THE INDUSTRIAL COMMUNICATION PROBLEMS BY IMPLEMENTING MANUFACTURING AUTOMATION PROTOCOL (MAP)	(32) GALLIUM ARSENIDE ICs FROM A USER'S PERSPECTIVE: PART II—ASICs	(33) C DEVELOPMENT ENVIRONMENT FOR SUPPORTING ELECTRONIC APPLICATIONS	
THURSDAY, NOVEMBER 17	3:00 PM TO 5:00 PM	(34) SYNERGISTIC MARKETING	(35) CAE/CAD: LINKING DESIGN TO SUPPORT MANUFACTURING		(36) DEVELOPMENT TOOLS FOR HIGH PERFORMANCE RISC MICROPROCESORS	

*SESSION 9 RUNS FROM 2:00 PM TO 5:00 PM, RATHER THAN 12:00 TO 2:00.

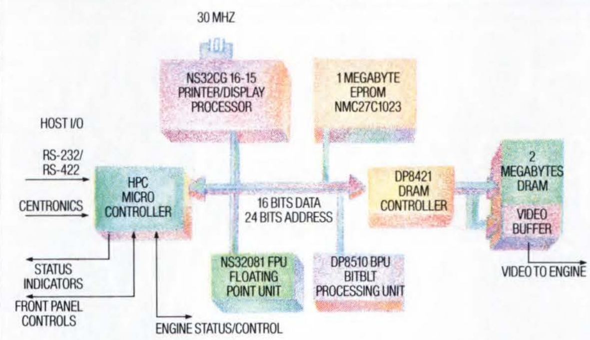
When it comes to page-printer electronics, only National puts it all together.

ALL TOGETHER FOR PRINTERS, SCANNERS, COPIERS, FAX MACHINES AND DESKTOP DISPLAYS

Introducing the NS32CG16 Printer/Display Processor.

The only fully programmable 32-bit, CMOS microprocessor tuned for graphics applications.

And the heart of the most cost-effective systems solution for a full range of imaging designs.



The NS32CG16 is the heart of a high-performance, cost-effective systems solution for applications like this page-printer controller.

ALL TOGETHER: THE CHIP

The NS32CG16 combines the programmability of a high-performance 32-bit microprocessor with the power of a specialized graphics coprocessor. It includes 18 dedicated graphics instructions for:

- bit-aligned block transfers (BitBLT) with 16 logical operations for high-speed character moves and windowing
- line drawing (9 Mbits/sec)
- pattern drawing, replication, and filling (60 Mbits/sec)
- pattern magnification to support Epson and HP LaserJet™ emulations (1X, 2X, 3X, 4X)
- binary data compression/expansion for compact font storage under run-length-limited (RLL) encoding
- supports CCITT Group III and IV protocols for facsimile transmission
- on-chip clock generator
- programmable power-down modes
- on-chip DMA support circuitry.

A true 2-address machine (for direct memory-to-memory graphics operations), the NS32CG16 has a 16-Mbyte linear address space to support large font storages, high-dpi (dots-per-inch) page buffers, and memory-intensive page-description languages (PDLs).

ALL TOGETHER: THE PERIPHERALS

The NS32CG16 is supported by a full range of peripheral devices, available now:

- hardware floating-point coprocessors for high-speed outline-font calculations in PDLs like PostScript™ and PCL™
- DRAM controllers
- single-chip I/O support for RS232 Serial, Centronics Parallel, and AppleTalk® interfaces
- LAN support, including Ethernet, Thin Ethernet, StarLAN, and IBM® 3270/5250 protocols
- interrupt controllers with timers and parallel I/O ports
- National's family of logic: FAST,™ FACT,™ ALS and AS.

ALL TOGETHER: THE TOOLS

The NS32CG16 is also supported by a full range of development tools, available now:

- add-in cards to turn your PC/AT® or compatible into a powerful, multiuser development host
- a full set of language tools, including
  - —assemblers, linkers, debuggers
  - —optimizing compilers for C, Pascal, FORTRAN 77, and Ada®
- MicroCASE (formerly Northwest Instrument Systems) Software Analysis Workstation for performance-tuning your code
- National's In-System Emulator (ISE™) for complete hardware/software integration
- the NS32CG16 Evaluation/Development Board to reduce development time and costs, and bring your design to market faster (*in development*).

ALL TOGETHER: THE PROOF

The NS32CG16 has already been designed-in by a number of major office peripherals manufacturers, such as Canon and Olivetti, and is now being evaluated by over 100 companies around the world.

But find out for yourself what the NS32CG16 can do in *your* design.

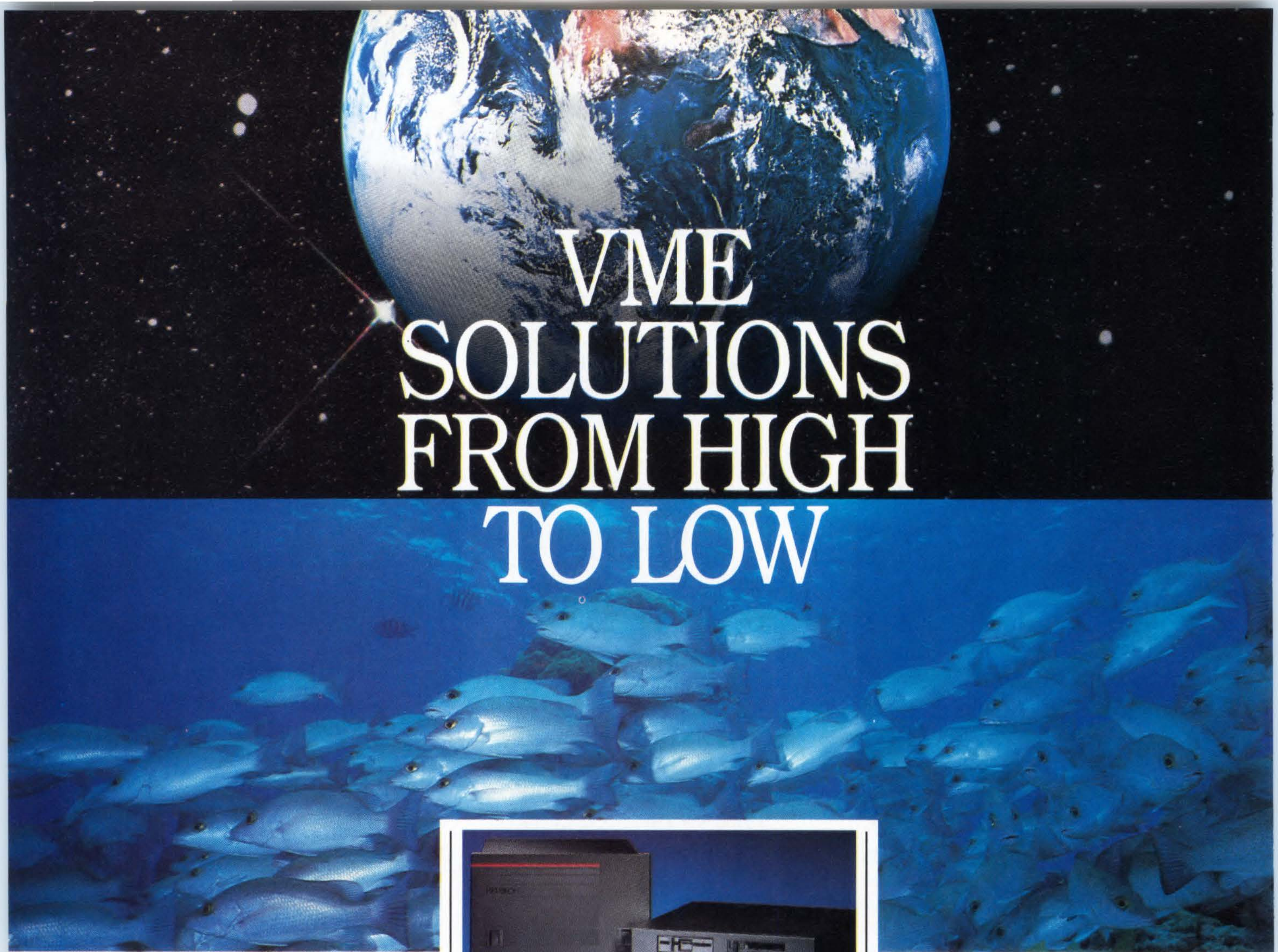
For more information immediately, call us toll-free at **(800) 227-1817, ext. 15.**

We think you'll be pleasantly surprised.

Altogether.

National Semiconductor

CIRCLE NO 128



The Power to Serve. Whatever your application, high or low-end, Heurikon has the VME power to drive it. From UNIX™ to real-time. From satellite communications to oceanographic research. We can solve the problem.

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3201 Latham Dr., Madison, WI 53713
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CIRCLE NO 129

Europe 1992 poses a challenge for the US electronics industry

Jack Gee, *Contributing Editor*

Managers and engineers at US electronics companies will soon be making entries in their diaries for 1989, but it's already time for them to begin focusing on 1992. That year will be a landmark for firms that design, manufacture, and market products destined for customers in Europe.

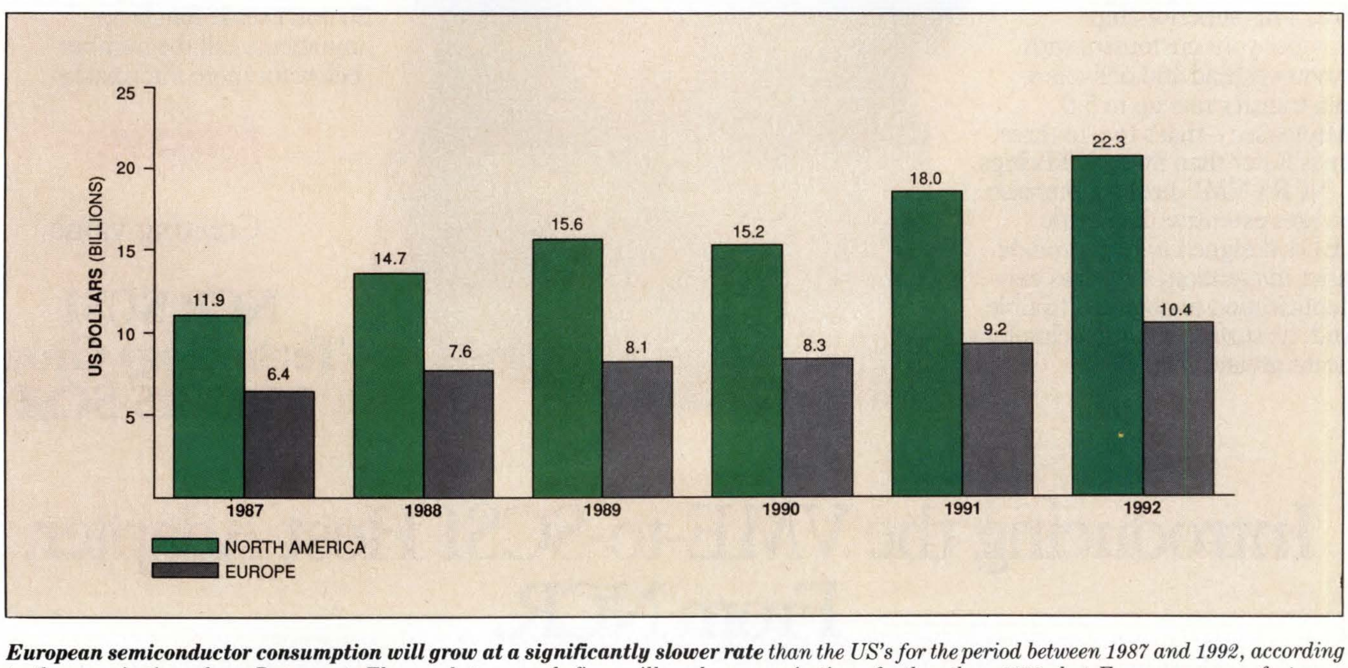
In 1992, the European Community's (EC) hodgepodge of 12 national markets will merge into a single market which, with 320 million consumers, will be as large as that of the US. The objective is to create a single marketplace in which physical, fiscal, and technical barriers to trade will be dismantled. European countries will no longer be able to raise protectionist barricades against products from their neighbors. But it's far from certain that Europe will become more hospitable to foreign competitors.

Robert R Heikes, who has successively headed the European semiconductor operations of Motorola and National Semiconductor, is optimistic. "After 1991, US firms can only do even better than they are already doing in Europe. It is 20 years since they began penetrating each European country with manufacturing, sales, and marketing. Now they are ready to attack Europe globally. The European companies, long confined within their own national frontiers and markets, are not ready for this new challenge."

Heikes and other electronics veterans argue that as bigger and more powerful European companies emerge in electronics and other industries, they will be forced to introduce common manufacturing standards. And, according to that school of thought, the standards will make life easier for US firms, which have so far been deterred by the maze of conflicting standards currently applied by European industry.

"It is amazing that, while the US usually has a common set of standards for each product family, Europe often has a dozen," says Robert Taylor, a consultant at European Research Associates in Brussels, Belgium. "The big question for US industry is whether the EC will become Fortress Europe. Americans and Japanese have grounds to fear that Europe will become more difficult to penetrate. There are already signs that the protective barriers which European countries are about to dismantle between each other will be raised again as an EC barrier against outsiders."

Europe's strategy should be



European semiconductor consumption will grow at a significantly slower rate *than the US's for the period between 1987 and 1992, according to these projections from Dataquest. The market-research firm will make no projections further than 1992, but European manufacturers are hoping to see great gains after that year, when the market becomes unified.*

based on improving its own resources in semiconductors, according to Klaus Luft, chairman of Nixdorf AG, the Paderborn, West Germany, data-processing company. Says Luft, who recently set up an ASIC plant in Neuchatel, Switzerland, to make chips for Nixdorf's computers, "Europe has been making it too easy for US and Japanese chipmakers to open factories, thanks to big cash grants and red-carpet treatment. Europe's needs would be better served by building more plants of our own. That would safeguard us from the recent unhappy experience with chip shortages which the US and Japan artificially created in order to push up prices."

From the American perspective, manufacturing in Europe will be more important than ever. Says Ted Richardson, director of the European Telecommunications Industry Service of Dataquest, a market-research firm based in San Jose, CA, "As 1992 looms closer, American and Japanese telecomm firms will find themselves under increasing pressure to manufacture in Europe. There's a real danger that, if they don't, they will find that, as the internal European barriers come down, the external ones will be raised higher. EC has made telecomm a strategic industry for Europe that it intends to defend."

Norbert Bininda, a telecomm executive for Siemens (Munich, West Germany), argues: "What Europe expects from the US and Japan are more open public-procurement practices. It would be very bad if Europe were alone in adopting free-trade measures." At present, however, less than 10% of procurement by Europe's government agencies is put out to international competition. Telecommunications contracts have traditionally been the preserve of local industry—and are likely to remain so.

US companies that are selling but not yet marketing in Europe are closely studying the implications of 1992's changes. Declares William P Conlin, president of Calcomp, an Anaheim, CA, manufacturer of computer-graphics products: "By that date, we could be close to capacity in our US plants. That could be the time to turn to manufacturing overseas, particularly in Europe. We are already having difficulties shipping product across the Atlantic. A European plant could be the solution to a number of problems."

However, many US electronics firms consider themselves well geared already to cope with the implications of 1992. Dr Gilbert F Amelio, president of Rockwell International Corp's Telecommunications and Semiconductor business, reports that Rockwell has recently opened its first remote chip-design center in Europe, which is linked directly to the firm's R&D center in Newport Beach, CA.

Rockwell is targeting an increase in the European share of its worldwide semiconductor business from 12% at present to 20% by 1990. Amelio says he chose Sophia Antipolis, a science park on the French Riviera, as the site of the design center because of the high concentration of telecomm manufacturers in France. "France is the most advanced country in the world in telecomm," he says. "Look at the work their engineers, designers, and market people have done on smart-card-operated phones, their Minitel videotex network, and other state-of-the-art ventures. It may take some years for the Europeans to introduce common standards in telecomm. Whatever line they take, we at Rockwell intend to be ready."

Chip manufacturers who target the European telecomm market are pinning their hopes on moves toward the deregulation of telecomm services and purchasing structures. Until now, these factors have successfully closed European national markets to outside suppliers of equipment. Only in Britain has the carrier service been opened to competition.

Pierre Suard, chairman of Alcatel NV, the French-dominated consortium that has acquired ITT Corp's telecomm activities, says: "Deregulation in Europe is going to take longer than some people imagine. For Alcatel, which already sells ITT's System 12 and the French-designed E 10 and E 12 central-office switches throughout most of Europe, it won't make a dramatic change, because we have plants that span much of the continent. So it makes little difference to us how swiftly deregulation is introduced. We are a local company in almost every country."

Sematech worries Europe

While US chip makers eye the scene across the Atlantic with optimism, European semiconductor manufacturers look westward with concern. They are carefully tracking the efforts of their American competitors, who, under the umbrella of Sematech, a $1.5. billion research venture by leading US chipmakers, are striving to recapture the industry leadership they lost to Japan.

"In Europe we have no real answer to what the Americans are doing," says Hartwin Breitenbach, director of marketing at Austria Mikro Systems International GmbH of Unterpremstaetten, Austria. "We lack the focal point of Sematech." Pasquale Pistorio, chief executive of SGS-Thomson Microelectronics, takes a more optimistic view: "Sematech could be a real stimulus to the European chip industry."

Although Sematech is directed against Japan, many Europeans fear that by excluding them from the club, the US manufacturers are trying to weaken Europe's lackluster chip industry. As Jim Beveridge, director of the London-based European Semiconductor Div of Dataquest, notes: "Just look at the performance of some of the European chip manufacturers. Then you will understand why Sematech has got them worried."

Europe's chip makers have carved out only a meager 7.7% share of the US marketplace, according to Dataquest. But 43% of all chips sold in Europe come from the US. Excluding IBM, whose European plants produce chips exclusively for the company's own consumption, 24% of European-made chips come from US-owned plants.

What concerns the European chip makers even more is that they're performing in a lifeless marketplace. This stagnation is camouflaged by the sales figures, which grew from \$5.5 billion to \$6.4 billion between 1986 and 1987, an increase of 14.4%. However, that increase reflects last year's weakness of the dollar against European currencies. In European terms, the local market decreased by 1.2%, according to Dataquest.

Executives at European firms such as SGS-Thomson Microelectronics (Agrate Brianza, Italy) and Philips (Eindhoven, the Netherlands), which have chip operations of their own in the US, are disappointed that their American rivals don't want them at Sematech. Cees Koot, Managing Director of the Integrated Circuits Business Unit at Philips International BV, says: "We would much rather have our Signetics offshoot in the US within Sematech. The Americans are wrong in keeping us out. It is important for them to mobilize European expertise. Without healthy interaction between the US and European semiconductor industries, the Japanese are going to run away with the world's chip equipment business. The Americans have to realize that they cannot survive on their own."

Dataquest analyst Beveridge doesn't believe that Sematech is hamstringing Europe's semiconductor industry. "Sematech simply reflects the failure over the years of the US chip firms to get their act together. Europe has its own problems in getting its own manufacturers to cooperate. But we are likely to get over them faster. In fact, we are already well on the way."

European Silicon Structures (ES2) (Sèvres, France) is a company that symbolizes a growing determination not to lag behind the US and Japan. Financed by electronics firms and financial institutions from all over western Europe, ES2 specializes in ASICs. It's now turning out these custom devices at the rate of 200 per year. The firm's chairman, Robb Wilmot, boasts that ES2 is "ahead of all the competition. We have already built the largest custom chip: 1.1 cm a side. We have put the most designs on a wafer: 28. We have also achieved fastest delivery—only two weeks. And we are taking one quarter of the full custom designs on offer in Europe."

Over the past year, Europe's muscle in chip making has also been strengthened by two major mergers. Italy's SGS Microelettronica teamed up with the commercial semiconductor arm of France's Thomson group to create SGS-Thomson Microelectronics. This year, the new company forecasts revenues of at least \$1 billion, compared with \$860 million for the two separate entities in 1987. Says CEO Pistorio: "One of the basic reasons for our type of merger is to acquire technological characteristics or specific technologies that enrich the existing portfolio."

The Sematech partners could soon take notice as Europe's leading semiconductor firms launch the Joint European Semiconductor Silicon (JESSI) project. The founders, Philips of the Netherlands and Siemens of West Germany, have already spent four years in developing 1M- and 4M-bit memory chips. JESSI's task is to match US and Japanese efforts by developing powerful new semiconductors for the 1990s. According to the group's present plans, much of the \$1.8 billion investment for the project will be financed by the West German and Dutch governments.

Pat Brockett, managing director of National Semiconductor Ltd (Swindon, UK), argues that Europe's priority is to make an impact on the US chip market, where, as the Dataquest numbers show, its presence is very poor. "Look how Siemens and Ericsson are forging their way into the US telecommunications marketplace," Brockett says. "This is what the European chip makers should be doing, too."

Gerald B Thomas, President of LSI Logic Ltd (Sidcup, UK), the European wing of the US company, comments: "Europe has the opportunity to match Sematech. Chips are a business where everybody is fighting tooth and nail. But there are big opportunities as we approach the 1992 landmark year, both for US manufacturers in Europe—and for Europeans in the US."

These messages from the competition are likely to fall on deaf ears, however. For the moment, Europe's chip makers regard the protection of their own patch of ground as the priority. Any assault strategy will come later—if at all.

EDN

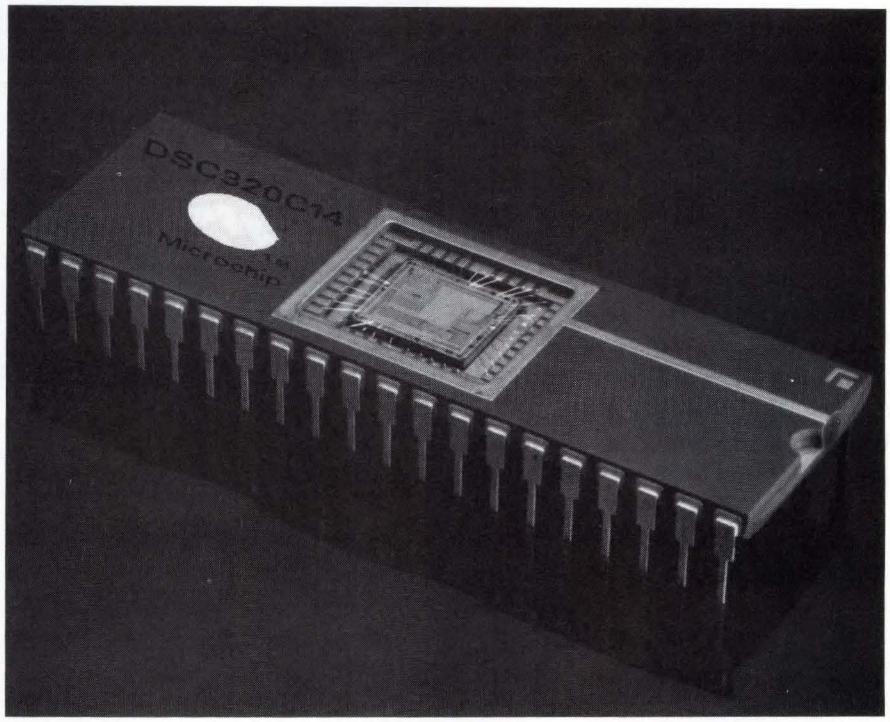
Jack Gee is a contributing editor for Electronic Business magazine. He lives and works in Paris, France.

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517

DSP microcontroller performs multiply-accumulate operations in 160 nsec

The DSC320C14 microcontroller combines ROM, RAM, and digital I/O signals with a DSP320C10 DSP µP core. Target applications for the microcontroller include real-time closed-loop control for computer peripherals, automotive systems, and industrial and military equipment. The chip achieves a performance of 6 MIPS and executes multiply-accumulate operations in a single 160-nsec instruction cycle.

On-chip features include 16 bit-selectable I/O lines, 15 internal/external interrupt inputs, and 1 nonmaskable interrupt signal. The chip also includes four 16-bit general-purpose timers that have 160-nsec resolution. You can set one timer to function as a watchdog timer, you can combine two of the timers to work as a single 40-bit timer, and you can configure the remaining timer as a baud-rate generator.



***ROM, RAM, timers, and digital I/O signals** combine with a DSP320C10 µP core in the DSC320C14 DSP microcontroller. The chip fits into real-time control applications that benefit from single-cycle, multiply-accumulate operations.*

In addition, two of the timers can produce 6 PWM outputs and perform edge detection on four inputs. The outputs produce pulses as small as 160 nsec with frequencies as high as 2.5 MHz. The edge-detection circuitry stores a timer value corresponding to an event and can be programmed to interrupt the µP upon occurrence of events.

A serial port with a Codec mode, which operates at 6.4 MHz synchronously or 400 kHz asynchronously, also resides on the chip. This port can detect and flag parity, overrun, framing, and other errors. You can also configure the serial port to connect to the BitBus. Operating in codec mode, the port provides an analog interface and supports the 1.544-MHz T1 digital-telephone rate.

The microcontroller includes 256 16-bit words of RAM and 4k 16-bit words of ROM. Furthermore, the µP can address 4k words of memory connected externally to the chip. The microcontroller employs a memory bank-switching technique to execute code out of internal or external memory. You can store DSP routines in internal ROM and call them from code residing in external memory. However, the internal ROM can't be read externally, thus providing data security for the chip's ROM-based applications.

Because the microcontroller offers object-code compatibility with the DSP320C10, you can access a large base of existing DSP and control application software. In addition, the company plans to offer an assembler/linker and simulator for the chip. You can also expect an evaluation board, an in-circuit emulation module, and an IBM PC-based development system to be available soon.

The chip will be offered in a 40-pin DIP, a 44-pin PLCC (plastic leaded chip carrier), and a 68-pin PLCC. Only the 68-pin device will allow access to external memory. You can buy an engineering sample of the 40-pin device for $75, and production quantities will be available in the first quarter of 1989. Texas Instruments will act as a second source for the chip.

—Maury Wright

Microchip Technology Inc, 2355 W Chandler Blvd, Chandler, AZ 85224. Phone (602) 345-3287.

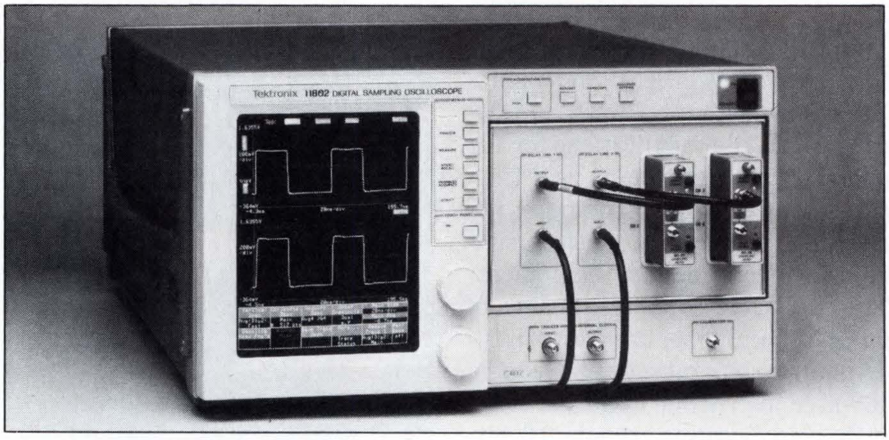
Circle No 732

20-GHz-bandwidth DSO samples at 100G samples/sec and implements differential TDR

Necessity has long been known as the mother of invention, but, among electronic products, there are many inventions that become the mother of necessity: Once users understand what such a product can do, they can see no way to accomplish their jobs without it. Tektronix envisions this kind of role for the 11800 Series digital sampling oscilloscopes.

The 11800 Series scopes aren't the only DSOs that combine a 20-GHz bandwidth with a resolution of at least eight bits or the only ones that, in effect, sample at 100G samples/sec. (Their actual sample rate of 200k samples/sec is faster than that of most sequential equivalent-time-sampling scopes.) They do, however, sport several unique features. One is expandability to 136 channels, with 1-psec timing inaccuracy between any pair. Eight channels can appear on the screen at one time. Another is the ability to make *differential* TDR (time-domain reflectometry) measurements.

By applying pulses and looking for reflections, TDR allows you to measure the electrical length of transmission lines and to locate discontinuities in them. In differential TDR, the scope, when equipped with an appropriate sampling head, applies equal amplitude pulses of opposite polarity to a pair of conductors—for example, the twisted pairs that constitute the balanced lines often used for clock distribution in high-speed computer systems. Heretofore, commercial TDR instruments have been single ended, causing measurements on balanced lines to be inaccurate as well as difficult to make. Tektronix believes that differential TDR is such a great improvement over single-ended TDR that it will become an industry standard.



***A touch-sensitive screen** and rotary controls, whose functions depend on the menu from which you access them, give the 11800 Series scopes an uncluttered panel despite a wealth of firmware-resident features.*

Because the new scope can accommodate so many channels, its vendor envisions it at the heart of automatic test systems—systems, for example, that characterize the dynamic performance of high-pin-count ICs. Most attempts to use scopes in such applications have involved the use of relays to sequentially connect a small number of inputs to different device pins. However, in addition to being slow, this approach is subject to timing errors introduced by signal paths through the relays.

So far, nobody has succeeded in quantifying ease-of-use. Nonetheless, the 11800 Series scopes provide a bevy of features that would accord them a high score for user-friendliness. Unlike the vendor's portable digital scopes, which attempt to provide the "feel" of analog instruments, the 11800 Series scopes supplant many separate front-panel controls with a series of on-screen menus, a touch-sensitive screen, and a pair of rotary controls. The functions of the rotary controls change depending on the menu from which you access them. This approach makes possible an uncluttered panel and yet provides easy access to a surprisingly large firmware-resident feature set.

You can invoke 16 automatic measurement modes—for example, you can measure propagation delay and many pulse parameters—and display six measurements on the screen below the waveforms. The readings update continuously until you stop data acquisition. Tektronix claims that a concerted human-engineering effort has made frequently used menu selections much more easily accessible than the comparable functions of competitive instruments.

The 11801 8-channel mainframe is priced at $23,500; the 11802 4-channel mainframe is priced at $22,000. Expanders, each of which accommodates as many as 32 channels, are priced from $10,000. A 2-channel sampling head is $3500, a TDR sampler $5000, and a 9-GHz-bandwidth passive probe $1250.

—Dan Strassberg

Tektronix Inc, Box 1700, Beaverton, OR 97077. Phone (800) 835-9433, Ext 170.

Circle No 731

PC-based CD-ROM tool speeds component selection

If you need a 5V, 45-nsec, 8k-byte × 8-bit static RAM that is screened to MIL-STD-883C and fabricated in CMOS, you typically start your search in the IC Master catalogue. After finding that seven vendors make SRAMs that meet your specifications, you have to chase down data sheets and application notes before you can evaluate the devices for criteria such as MIL qualification, power consumption, source and sink currents, and a host of other design considerations. Only after spending days, weeks, or months finding the necessary documentation can you start the real engineering task of component selection. Now there is an easier way.

CAPS (Computer Aided Product Selection) is a tool that automates the whole process of integrated-circuit and semiconductor-device selection. To use the system, you need a PC/AT or compatible computer and a laser or dot-matrix printer with graphics capability. The CAPS system is available on an annual subscription basis and comes with two plug-in boards; a 4-disk CD-ROM reader; a high-resolution, 1650 × 1200-pixel, full-page monitor; a mouse; and a set of about 20 CD-ROM disks.

The disks contain a conveniently organized, indexed database of more than 400,000 devices from over 250 vendors. You access the database via a menu-driven user interface that allows you to search for a part on the basis of fabrication technology, function, and dc or ac parameters. You can identify equivalent devices and alternate sources, find mil-spec parts, locate functionally identical components with different reliabilty ratings, ensure that a particular part is still in production, and look up replacements for obsolete components. The CAPS database also includes in-depth reference data covering component upgrades and downgrades, military and DESC (Defense Electronics Supply Center) part numbers, reliability ratings, QPL (qualified parts list) sources, and manufacturers' addresses and phone numbers. If needed, you can print data sheets and applications notes directly from the database.

***CAPS is a PC-based hardware and software package** that utilizes a high-resolution monitor and a 4-disk CD-ROM player to automate the time-consuming process of selecting ICs and semiconductor devices.*

The CAPS system is available on an annual subscription basis from Cahners Technical Information Service for $7,950. Update disks are issued at 90-day intervals and include information on new components as well as revisions to existing information.

—Michael Markowitz

Cahners Technical Information Service Division, 275 Washington St, Newton, MA 02158. Phone (617) 964-3030.

Circle No 730

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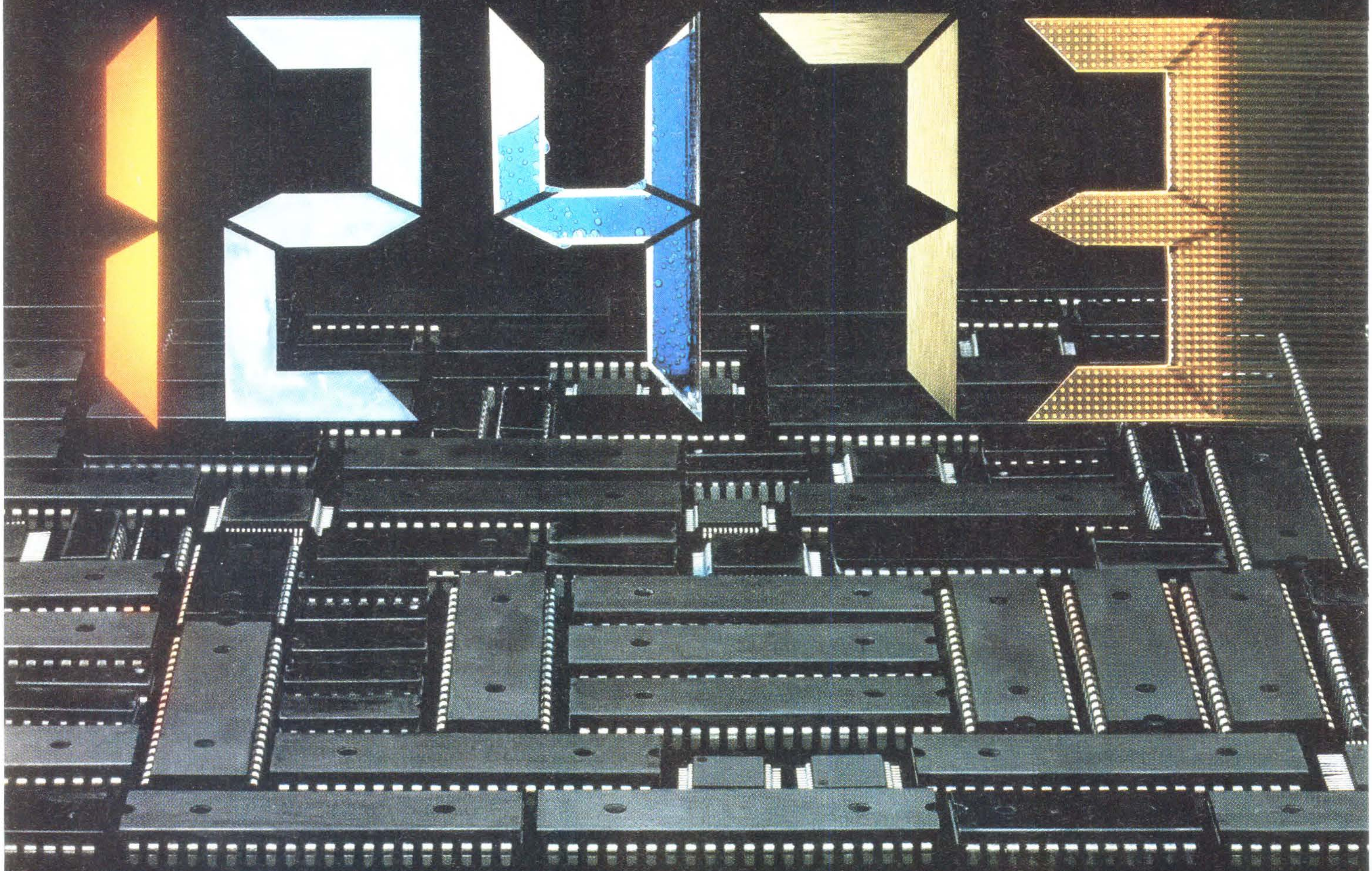
CIRCLE NO 134

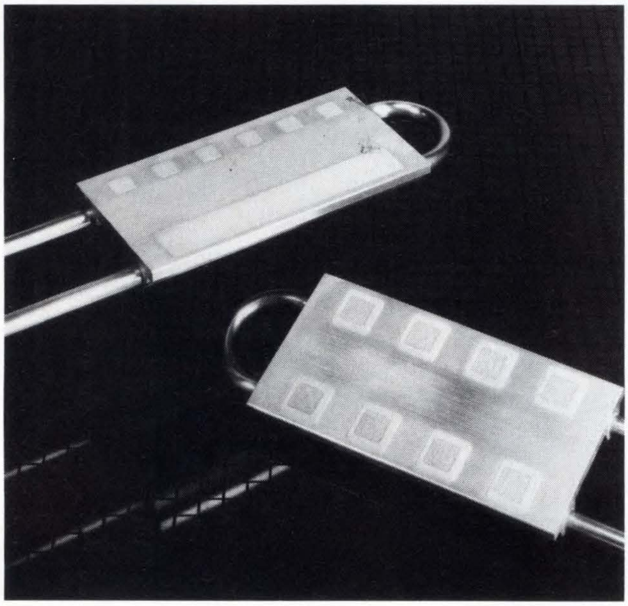
No matter what your element, our display ADCs are in it.



TELEDYNE SEMICONDUCTOR

READERS' CHOICE

Of all the new products covered in EDN's **July 7, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our **July 7, 1988,** issue.



◀ COLD PLATES

These liquid- and air-cooled plates have a ceramic coating with high thermal conductivity as well as good electrical insulation. The manufacturer uses a proprietary process for applying ceramic coatings to a metal base (pg 220).
EG&G Wakefield Engineering.
Circle No 601

UNIX UTILITY

XDOS converts binary-code programs written for the IBM PC to binary images for Unix computers (pg 260).
Hunter Systems.
Circle No 604

ENHANCED MICROPROCESSOR

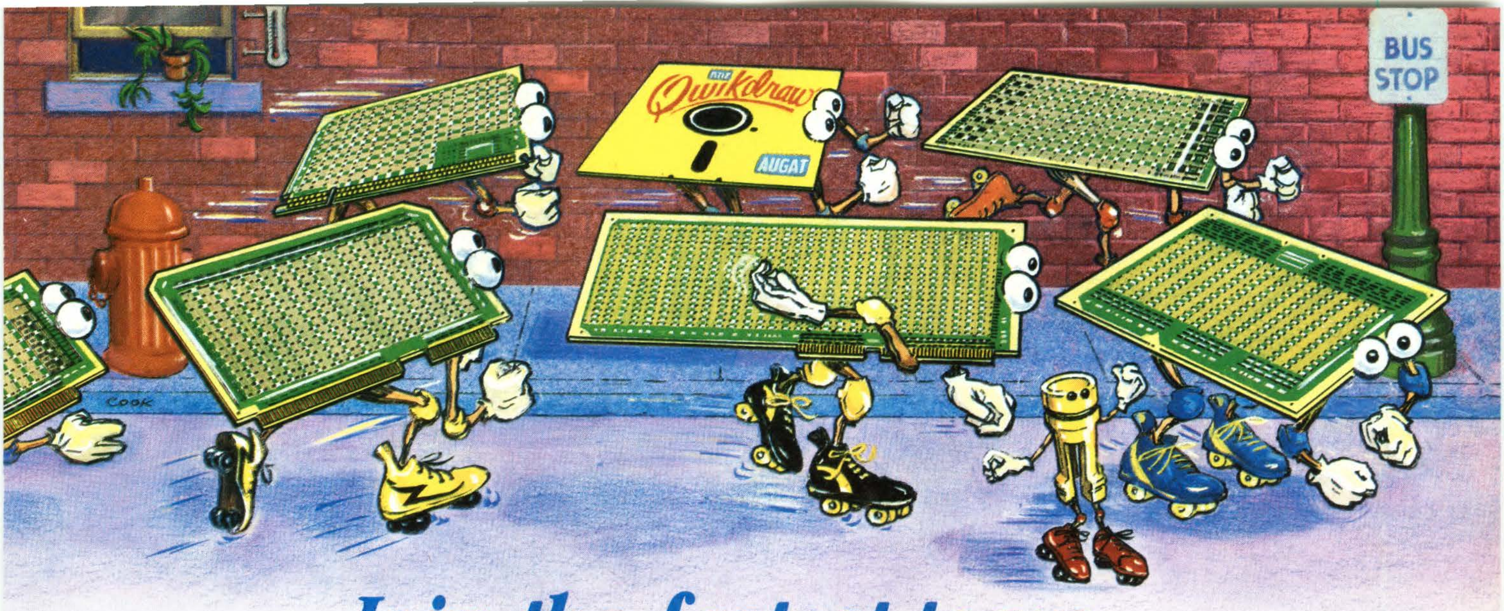
The Z80180 incorporates an on-chip memory-management unit (MMU) that can address as much as 1M byte of memory and support 64k bytes of logical I/O space (pg 100).
Zilog Inc.
Circle No 603

DC/DC CONVERTERS

Models in the NMA line of dc/dc converters accept inputs of 5, 12, 24, or 48V dc. The units provide an output of ±5, ±12, or ±15V with 750 mW of power (pg 198).
International Power Sources Inc.
Circle No 602

▲ AUDIO PREAMP

The TEA 6300 audio preamplifier incorporates a signal source selector; volume, bass, treble, and stereo balance controls; and a quad fader to control the front and rear speaker amplifiers in surround-sound systems (pg 140).
Philips.
Circle No 605
Signetics Corp.
Circle No 606



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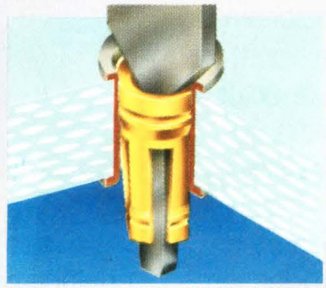

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CIRCLE NO 136

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	34	33	33	0	0	**8.7**	8.3
Pot-Core	0	13	61	13	13	0	**10.5**	8.1
Laminate (power)	0	18	64	18	0	0	**8.4**	9.5
CONNECTORS								
Military panel	0	0	83	17	0	0	**9.2**	12.9
Flat/Cable	10	50	30	10	0	0	**5.4**	6.6
Multi-pin circular	13	13	48	13	13	0	**9.5**	11.3
PC (2-piece)	0	60	20	20	0	0	**6.4**	7.8
RF/Coaxial	0	33	58	9	0	0	**7.0**	6.5
Socket	8	38	38	16	0	0	**6.6**	6.3
Terminal blocks	20	40	33	7	0	0	**4.9**	3.6
Edge card	8	46	38	8	0	0	**5.6**	6.7
D-Subminiature	21	50	21	8	0	0	**4.4**	5.2
Rack & panel	11	33	23	33	0	0	**7.9**	8.4
Power	22	44	12	22	0	0	**5.6**	6.3
PRINTED CIRCUIT BOARDS								
Single sided	0	60	40	0	0	0	**4.9**	5.3
Double sided	0	50	50	0	0	0	**5.4**	5.9
Multi-layer	0	20	80	0	0	0	**6.9**	8.5
Prototype	0	94	6	0	0	0	**3.3**	3.2
RESISTORS								
Carbon film	29	35	24	12	0	0	**4.8**	4.2
Carbon composition	35	24	29	12	0	0	**4.9**	5.4
Metal film	33	27	33	7	0	0	**4.5**	4.6
Metal oxide	33	22	33	12	0	0	**5.1**	5.0
Wirewound	25	13	49	13	0	0	**6.3**	6.4
Potentiometers	22	17	44	17	0	0	**6.6**	6.5
Networks	14	50	21	15	0	0	**5.5**	6.2
FUSES	25	44	31	0	0	0	**3.8**	3.6
SWITCHES								
Pushbutton	7	53	33	7	0	0	**5.3**	5.8
Rotary	15	38	31	16	0	0	**6.1**	7.5
Rocker	0	58	33	9	0	0	**5.7**	5.9
Thumbwheel	10	50	20	10	10	0	**7.1**	8.6
Snap action	0	43	43	14	0	0	**6.9**	6.2
Momentary	11	56	22	11	0	0	**5.1**	6.1
Dual-in-line	0	56	33	11	0	0	**6.0**	6.1
WIRE AND CABLE								
Coaxial	0	58	42	0	0	0	**5.1**	3.7
Flat ribbon	13	67	20	0	0	0	**3.6**	3.5
Multiconductor	13	53	27	7	0	0	**4.8**	3.4
Hookup	29	47	24	0	0	0	**3.3**	2.4
Wirewrap	36	36	28	0	0	0	**3.3**	4.1
Power cords	18	29	41	12	0	0	**6.0**	4.7
POWER SUPPLIES								
Switcher	0	40	40	20	0	0	**7.4**	10.4
Linear	0	44	44	12	0	0	**6.6**	7.8
CIRCUIT BREAKERS	9	45	18	18	10	0	**8.1**	7.1
HEAT SINKS	33	25	25	17	0	0	**5.3**	5.8
BATTERIES								
Lithium coin cells	18	36	36	10	0	0	**5.5**	5.1
9V alkaline	27	37	36	0	0	0	**3.9**	3.6
Real-time clock back-up	0	33	67	0	0	0	**6.3**	7.6
RELAYS								
General purpose	13	47	20	20	0	0	**6.1**	6.2
PC board	0	44	25	31	0	0	**8.1**	8.6

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
Dry reed	0	22	56	22	0	0	**8.5**	7.2
Mercury	0	17	33	50	0	0	**10.8**	7.6
Solid state	9	10	36	45	0	0	**10.1**	8.7
DISCRETE SEMICONDUCTORS								
Diode	26	32	26	16	0	0	**5.5**	6.1
Zener	25	37	19	19	0	0	**5.5**	5.4
Thyristor	14	36	29	21	0	0	**6.6**	6.8
Small signal transistor	33	33	7	27	0	0	**5.7**	7.7
MOSFET	25	17	25	33	0	0	**7.6**	8.7
Power, bipolar	30	20	20	30	0	0	**6.8**	7.4
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	21	7	43	29	0	0	**8.1**	9.0
CMOS	11	32	46	11	0	0	**6.3**	7.5
TTL	35	18	41	6	0	0	**4.7**	6.7
LS	29	24	41	6	0	0	**4.9**	7.1
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	44	23	33	0	0	**8.2**	7.5
OP amplifier	8	15	46	31	0	0	**8.9**	6.2
Voltage regulator	19	31	25	25	0	0	**6.8**	5.7
MEMORY CIRCUITS								
DRAM 16K	0	20	0	80	0	0	**12.9**	13.3
DRAM 64K	0	13	0	87	0	0	**13.8**	12.1
DRAM 256K	0	8	0	54	23	15	**19.1**	15.2
DRAM 1M-bit	0	12	11	22	44	11	**19.2**	17.9
SRAM 4K × 4	0	17	17	33	33	0	**15.3**	16.7
SRAM 8K × 8	0	9	15	38	23	15	**17.8**	18.6
SRAM 2K × 8	0	13	0	74	13	0	**15.1**	16.1
ROM/PROM	0	14	0	86	0	0	**13.7**	12.5
EPROM 64K	8	25	17	50	0	0	**9.8**	13.3
EPROM 256K	0	15	15	62	8	0	**13.2**	15.3
EPROM 1M-bit	14	15	0	57	14	0	**12.8**	18.5
EEPROM 16K	0	17	17	66	0	0	**12.0**	15.8
EEPROM 64K	0	15	14	71	0	0	**12.5**	16.9
DISPLAYS								
Panel meters	0	20	50	20	0	10	**10.8**	8.9
Fluorescent	0	13	38	49	0	0	**11.0**	11.1
Incandescent	0	25	25	50	0	0	**10.4**	5.3
LED	14	43	22	21	0	0	**6.3**	5.9
Liquid crystal	10	10	40	40	0	0	**9.6**	8.1
MICROPROCESSOR ICs								
8-bit	0	50	20	30	0	0	**7.7**	8.2
16-bit	13	37	13	37	0	0	**7.8**	9.4
32-bit	0	22	33	33	12	0	**11.4**	13.3
FUNCTION PACKAGES								
Amplifier	0	25	37	38	0	0	**9.5**	7.1
Converter, analog to digital	0	18	55	27	0	0	**9.1**	8.6
Converter, digital to analog	0	25	37	38	0	0	**9.5**	8.6
LINE FILTERS	8	54	15	23	0	0	**6.3**	6.6
CAPACITORS								
Ceramic monolithic	24	29	29	18	0	0	**5.9**	7.3
Ceramic disc	18	29	29	24	0	0	**6.9**	7.0
Film	27	27	13	33	0	0	**6.9**	6.5
Aluminum electrolytic	19	25	19	37	0	0	**8.0**	8.4
Tantalum	17	22	27	28	6	0	**8.6**	7.8
INDUCTORS	8	30	31	31	0	0	**8.1**	9.3

Source: Electronics Purchasing Magazine's survey of buyers.

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PLESSEY KEY PROCESS TECHNOLOGY

BIPOLAR

DESCRIPTION	Ft	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14μm	1
High voltage	400MHz	20μm	1
High speed linear	4.5GHz	4μm	2
High speed digital	6GHz	3μm	2
Ultra-high speed	14GHz	0.6μm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4μm	3-10V
JG Double SiGate NMOS	10MHz	6μm	9-18V
VB High speed CMOS	40MHz	2μm	3-5V
VJ Very fast CMOS	50MHz	1.5μm	3-5V
VQ Ultra fast CMOS	75MHz	1.2μm	3-5V
MH/MA SiGate CMOS	30MHz	4μm	3-15V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5μm				
CDI FAB I	3.75μm	11.5μm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5μm	8μm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5μm	8μm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5μm	6μm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2μm	4.5μm	200ps	0.2pJ	0.14pJ

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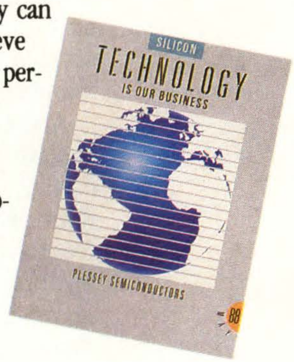

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Scotts Valley, CA 95066
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Plessey Semiconductors Ltd.
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PLESSEY
Number 1 for **ASICs**

EDN's 15th Annual μP/μC Chip Directory

Jon Titus, *Editor*

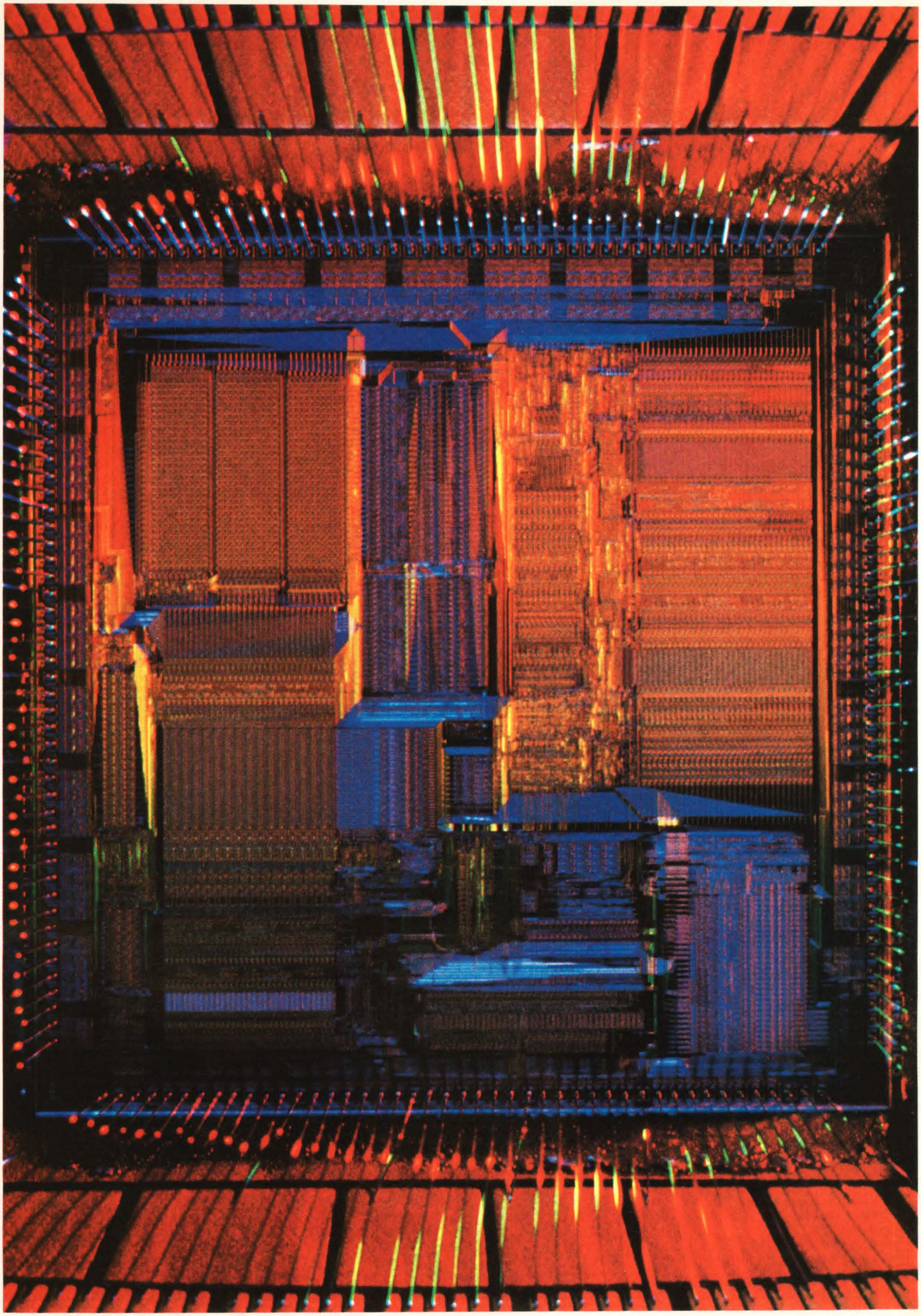
Forget about RISCs, MIPS, and Dhrystones. This year, the real action revolves around new embedded-controller μP chips.

This year, new μP chips aimed at embedded-control applications deserve the limelight—even though high-performance RISC (reduced instruction-set computer) chips have garnered most of the headlines. Actually, today's new embedded controllers and RISC CPU chips aren't that far apart. Three of the new high-end embedded-control μPs take advantage of at least some form of RISC architecture. Today, embedded controllers encompass a wide range of applications that go far beyond obvious uses in toys, appliances, and vending machines. Recently introduced 16-and 32-bit μP chips are letting designers insert unprecedented computer power in new graphics, data-communication, and data-processing applications.

Historically, devices such as the 8048 and 8051 have dominated the embedded-control market—a market aimed mainly at event-driven control applications. Those applications required chips that could respond to external stimuli and produce appropriate drive or control signals. But about two or three years ago, the embedded-controller market started shifting into other areas, and designers started demanding more performa ance from μP chips.

According to Alan Steinberg at Intel, the embedded-control market now includes four broad areas: event processing, numeric processing, digital signal processing, and data processing. Thus, today's market shows a shift away from event-driven controllers—although thousands of these applications still exist—toward more complex data-manipulation tasks. That shift may be one reason why today's μP manufacturers have been pushing more gen-

With recent 32-bit μP chips, *designers are putting unprecedented computer power into new graphics, data-communication, and data-processing applications. (Photo courtesy Motorola)*



eral-purpose and reprogrammable μP designs into the embedded-controller market. Examples of new high-end embedded-controller chips include Intel's 80960, Harris's RTX2000, and AMD's 2 29000.

Certainly, the embedded-controller market continues to consume millions of low-end, 4-bit μC chips, and that important market will exist for many years. In terms of units shipped, however, this year the 8-bit devices may surpass their 4-bit cousins. Keep in mind it has taken *17 years* for this development to come

Manufacturers of μP/μC chips

For more information on μP/μC chips such as those included in this directory, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. Information about recent mergers and acquisitions appears in parentheses.

Advanced Micro Devices
901 Thomson Pl
Sunnyvale, CA 94086
(408) 732-2400
Circle No 650

Analog Devices Inc
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1 Technology Way
Norwood, MA 02062
(617) 329-4700
FAX (617) 326-8703
Circle No 651

AT&T Technologies Inc
Dept LT
555 Union Blvd
Allentown, PA 18103
(800) 372-2447
TLX 82772977
Circle No 652

Bipolar Integrated Technology
Box 4750
Beaverton, OR 97076
(503) 629-5490
FAX (503) 690-1498
TLX 263097
Circle No 653

California Micro Devices
2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
FAX (602) 921-6298
Circle No 654

Calmos Semiconductor
20 Edgewater St
Kanata, Ontario, Canada K2L 1V8
(613) 836-1014
FAX (613) 831-1742
Circle No 655

Cypress Semiconductor
3901 N First St
San Jose, CA 95134
(408) 943-2852
FAX (408) 943-2741
Circle No 656

Fujitsu Microelectronics Inc
3330 Scott Blvd
Santa Clara, CA 95054
(408) 727-1700
FAX (408) 922-9128
Circle No 657

GE-Intersil
(Acquired by Harris)
2450 Walsh Ave
Santa Clara, CA 95051
(408) 996-5000
Circle No 658

GE Solid State
(Formerly RCA, recently acquired by Harris)
Rte 202
Somerville, NJ 08876
(201) 685-6000
FAX (201) 685-6487
TWX 710-480-9333
Circle No 659

Gould Semiconductor (AMI)
2300 Buckskin Rd
Pocatello, ID 83201
(208) 233-4690
Circle No 660

Harris
Semiconductor Products Div
Box 883
Melbourne, FL 32902
(407) 724-7418
FAX (407) 729-5691
TWX 510-959-6259
Circle No 661

Hitachi America Ltd
2210 O'Toole Ave
San Jose, CA 95131
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Circle No 662

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Semiconductor &
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Marunouchi 1-Chome
Chiyoda-ku, Tokyo 100, Japan
(03) 212-1111
Circle No 663

Inmos Corp
Box 16000
Colorado Springs, CO 80935
(719) 630-4000
Circle No 664

Inmos Ltd
1000 Aztec W
Almondsbury
Bristol BS12 4SQ, UK
(0454) 616616
Circle No 665

Integrated Device Technology
3236 Scott Blvd
Santa Clara, CA 95051
(408) 727-6116
Circle No 666

Intel Corp
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Santa Clara, CA 95051
(408) 987-8080
Circle No 667

Intel Corp
Embedded Controller Operation
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Chandler, AZ 85226
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Circle No 668

Intergraph Corp
Advanced Processor Div
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FAX (415) 856-9224
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Austin, TX 78721
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Austin, TX 78735
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2900 Semiconductor Dr
Santa Clara, CA 95051
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NCR Corp
2001 Danfield Ct
Fort Collins, CO 80525
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Circle No 677

about. But because of the need for more complex devices and for advanced data-processing architectures, it shouldn't take the 16-bit μP chips quite as long to overcome their 8-bit relatives in embedded-control applications. Dataquest, a San Jose, CA, market-research company, reports that the 16-bit high-performance microcontroller market is the fastest growing portion of the entire microcomputer market.

Although 16-bit μP chips have been available for some time, the popularity of 16-bit embedded control-

NCR Microelectronics Div
1635 Aeroplaza Dr
Colorado Springs, CO 80916
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Circle No 678

NEC Electronics Inc
(US Headquarters)
401 Ellis St
Mountain View, CA 94039
(415) 960-6000
Circle No 679

NEC Electronics USA Inc
Microcomputer Div
1 Natick Executive Park
Natick, MA 01760
(508) 655-8833
FAX (508) 872-8692
Circle No 680

NV Philips
Eindhoven, The Netherlands
31-40-79-3333
Circle No 681

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TWX 310-499-9283
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Semiconductor Products Div
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Newport Beach, CA 92658
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Circle No 684

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1849 Fortune Dr
San Jose, CA 95131
(408) 432-9550
Circle No 685

SGS-Thomson
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20041 Agrate Brianza, Italy
(3939) 6555590
Circle No 686

SGS-Thomson Microelectronics
1000 E Bell Rd
Phoenix, AZ 85002
(602) 867-6259
Circle No 687

SGS-Thomson Microelectronics
(Formerly Mostek)
1310 Electronic Dr
Carrollton, TX 75006
(214) 466-6000
FAX (214) 466-8130
TLX 730643
Circle No 688

SGS-Thomson Semiconducteurs
BP 2
13790 Rousset, France
(42) 23-96-01
Circle No 689

Sharp Corp
Integrated Circuits Group
2613-1, Ichinomoto-Cho, Tenri-shi
Nara 632, Japan
Circle No 690

Sharp Microelectronics Corp
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10 Sharp Plaza
Mahwah, NJ 07430
(201) 529-8757
Circle No 691

Siemens AG
Components Group
Balanstrasse 73
Postfach 80 17 09
8000 Munich 80
West Germany
Circle No 692

Siemens Components Inc
Semiconductor Group
2191 Laurelwood Rd
Santa Clara, CA 95054
(408) 980-4500
Circle No 693

Sierra Semiconductor
2075 N Capitol Ave
San Jose, CA 95132
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FAX (516) 273-3123
TLX 7401051
Circle No 696

Texas Instruments Inc
MOS Microcomputers
Box 1443
Houston, TX 77001
(713) 274-2000
FAX (713) 274-2445
Circle No 697

Texas Instruments Inc
13536 N Central Expressway
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9775 Toledo Way
Irvine, CA 92718
(714) 455-2000
Circle No 699

Vitesse Electronics Corp
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Camarillo, CA 93010
(805) 388-3700
Circle No 700

VLSI Technology Inc
1109 McKay Dr
San Jose, CA 95131
(408) 434-3000
Circle No 701

WaferScale Integration Inc
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Fremont, CA 94538
(415) 656-5400
Circle No 702

Weitek Corp
1060 E Arques Ave
Sunnyvale, CA 94086
(408) 738-8400
Circle No 703

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
(602) 962-4545
Circle No 704

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
(408) 370-8000
Circle No 705

lers was enhanced by Intel's introduction of its 80188 and 80186 μP chips. Those chips became available after the introduction of the 8088 and 8086—the μP chips that quickly became popular with personal-computer designers. However, the 80188 and the 80186—both upgrades of the basic 8088/8086 architecture—were almost forgotten by the PC crowd during its rush to e embrace the 80286 and then the 80386.

Originally, Intel aimed the 80186 primarily at the reprogrammable (general-purpose) computer market; the embedded-controller market was of secondary importance. However, the embedded-controller market quickly embraced the 80186, designing the chip into office-automation and telecommunications products. To date, Intel claims almost 3000 design wins for the NMOS (80186) and CMOS (80C186) versions of the IC.

Engineers design I/O systems

These days, most engineers aren't designing central-processing units (CPUs), new personal computers, or workstations. Instead they're designing the I/O subsystems that surround these computers. That's where the embedded-controller chips are being used. The 80186 chip has gained great acceptance because software development is relatively painless. Programmers can write, debug, and test their programs on an IBM PC or compatible computer by using readily available hardware and software tools that support 8088- and 8086-development projects. Typically, embedded-control applications for the 80186 require between 20,000 and 60,000 lines of program code—which is well within the range that a PC can handle.

Ever since designers got used to having extra features on a μP chip, they've been demanding even more functions and higher-speed operations. It shouldn't be a surprise, therefore, that although most of us associate the 80386 μP chip with high-performance PCs and workstations, almost half of the design wins for the chip fall into the embedded-control area. Keep in mind, though, that the *number of chips* consumed by embedded-controller applications is small when compared with the number of 386 chips that go into PCs.

Most μP manufacturers aren't complacent about the embedded-controller market. Intel, for example, is aggressively pursuing new architectures aimed at new applications. For example, the company's 16-bit 8096 chip has been adopted within the automobile industry for engine, drive-train, and chassis control. Intel's 32-bit 80960, introduced in April, is finding use in laser printers, document scanners, and graphics products. Typically, those applications require intensive data-processing operations, so Intel also offers the 80960 chip in a version that supplies a full IEEE-P754 floating-point math unit. Programs for the 960 μP chip often run as long as 500,000 lines of program code. You'll find the 80960 chip in this year's directory.

Intel has company

Intel hasn't been alone in aiming new products at the embedded-controller market. Harris and AMD have been touting new μP chips, too. Harris's new 16-bit RTX2000 chip takes advantage of a RISC-like architecture that lets it execute most instructions in one 100-nsec cycle. Again, responding to users' needs to process more data in their applications, the RTX2000 supplies a 16×16-bit multiplier.

Although the RTX2000 incorporates some RISC-like features and supplies two external buses, don't be misled. The chip doesn't implement the Harvard-type architecture, in which data and instructions each have their own bus. The RTX2000's main bus, or memory bus, addresses a 1M-byte range of external memory locations that store instructions and data. The chip's second bus—the ASIC bus—addresses only eight word-width locations that act like an extension of the CPU's internal registers. Thus, the ASIC bus provides a high-speed communication channel between the CPU and other CPUs in a multiprocessor system. You could also use the ASIC bus to communicate with special-purpose coprocessor chips.

The RTX2000's software operations may be even more important than its hardware features. Like other μP chips, the RTX2000 has its own native assembly language, but there the similarity ends. Instead of cryptic assembly-language commands, the RTX2000's commands look like Forth-language statements. In fact, Forth programs compile directly into RTX2000 operations: Each Forth statement compiles into an RTX2000 instruction.

29000 takes high and low end

AMD took a different approach, aiming its 29000 μP chip at embedded-controller applications as well as general-purpose computer systems. AMD believes the chip's architecture is advanced and flexible enough to let the μP fill both needs. According to Mike Wodopian, the 29000 program manager at AMD, the embedded-control market is more attractive now because of the high volume of chips that it requires. The 29000 is attractive to customers because it employs a

Hey, what's your problem?

- [ ] Measurements take too long
- [ ] Questionable accuracy
- [ ] Poor frequency resolution
- [ ] Complicated test set-up
- [ ] Unreasonable boss
- [ ] Can't sleep at night
- [ ] _ _ _ _ _ _ _ _ _ _ _ _ _ _

RISC architecture and because it operates with inexpensive memory ICs, says Wodopian.

It will take longer to penetrate the small-computer market, although Wodopian thinks that time isn't far away. He believes that the differences among the high-end PCs—such as the Compaq 386, the Macintosh II, and the Sun workstation—are getting harder to discern. As the computer spectrum becomes more continuous between PCs and high-end workstations, the emotional arguments about Unix, MS-DOS, and OS-2 will decrease, and many applications for new processors will arise.

Microprocessor manufacturers must all remember that engineers are becoming reluctant to put several different processor types or architectures in one product. Instead, engineers want a complete family of devices that offers a continuous spectrum of price-vs-performance choices. The µP chips are no longer the "point product"—that is, they're no longer the device you choose first and then design everything else around.

Software remains the key

No matter what µP chip you choose for an embedded-control application, software development may make more demands than hardware design. Therefore, software-development tools and environments are often as important as a chip's architecture, and designers are pressing chip manufacturers for more support. For example, many customers could use software simulators that go beyond the capabilities of today's offerings. Users also clamor for more efficient operating systems and compilers. In fact, software may prove to be the bottleneck in embedded-control applications. EDN

Note

Some of the earlier microcontroller chips are not strictly general-purpose µP chips, but they have been in the directory for some time, so we include them for historical interest.

Also, AT&T asked us to remove the listing for the WE32 µP chip from this year's directory. Apparently, the company no longer seeks markets for the µP chip, although it expects to continue supplying peripheral and I/O chips. We have included the chip because of engineers' continuing interest in it. We recommend that you check with AT&T before considering the WE32 for use in a new application.

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

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BUILDING-BLOCK FAMILIES	264	2900 BIT SLICE
	267	29300/400, 29C300
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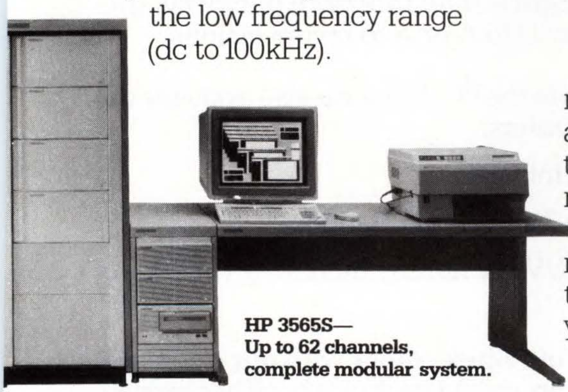

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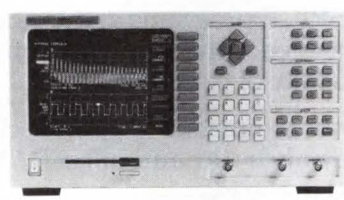

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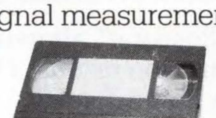

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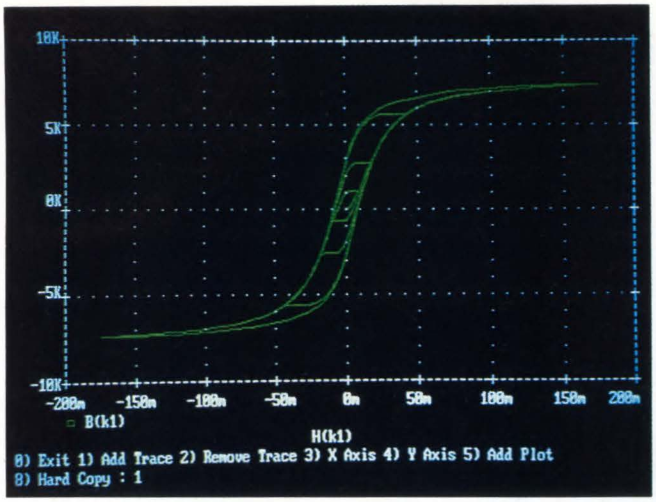
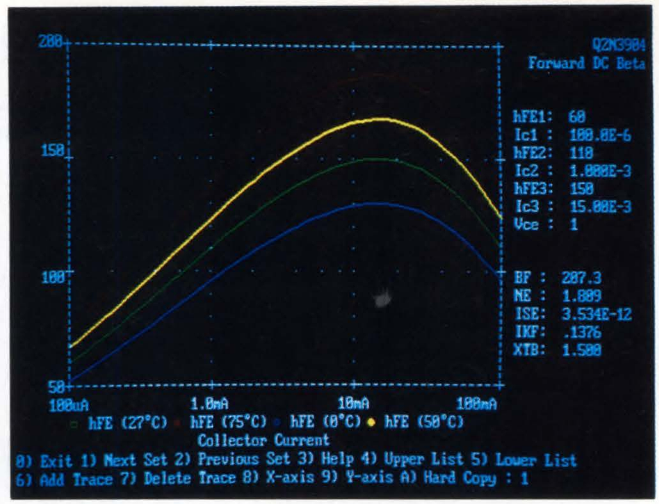


Waveform display from Probe



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PSpice

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All these features which have made PSpice so popular are available:

- Standard parts libraries for diodes, bipolar transistors, small-signal JFET's power MOSFET's opamps, voltage comparators, and transformer cores.
- GaAs MESFET devices, BSIM MOS model.
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

All these PSpice options are available under OS/2:

- Monte Carlo analysis to calculate the effect of parameter tolerances on circuit performance.
- The Probe "software oscilloscope", allowing interactive viewing of simulation results. The left photograph above is a Probe display.
- The Parts parameter extraction program, allowing you to extract a device's model parameters from data sheet information. The right photograph above is a Parts display.
- The Digital Files interface, allowing you to transfer data from your logic simulator to (or from) PSpice. The interface performs the necessary D to A or A to D conversions.

In addition to the PC, PSpice is also available on these computers:

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MicroSim Corporation

20 Fairbanks, Irvine, CA 92718 USA
(714) 770-3022 (800) 826-8603 Telex 265154 SPICE UR

COP400

4-BIT NMOS AND CMOS

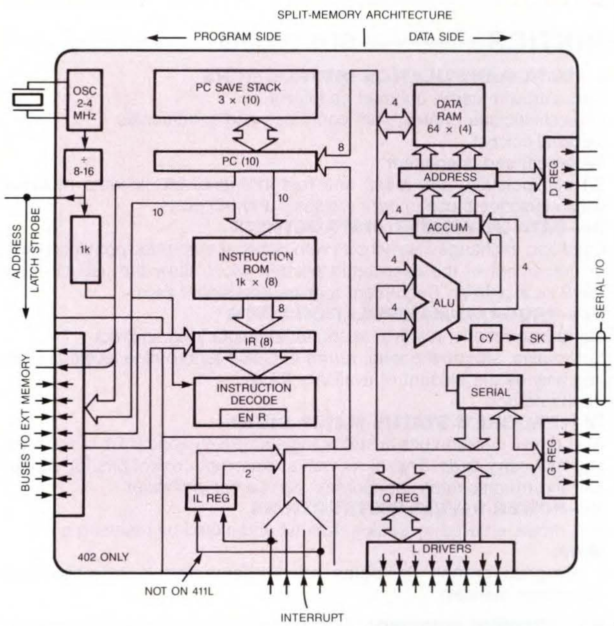
AVAILABILITY: Now.
COST: Under $0.50 for NMOS 413L and under $1 for CMOS 413C in very high volume (1M/yr).
SECOND SOURCE: Thomson.
CORE: Core μP concept has been used all along for this single-chip family, though on an internal basis.

Description: NMOS and CMOS minimum-cost single-chip family. COP chips are microcontrollers intended to make low-cost, intelligent products feasible, and contain the complete μC system—μP, memory and I/O—necessary to implement dedicated control functions. Typical application would be as lone chip in a low-cost toy for mass consumer market, where it would provide the intelligence to interface to a human. An OEM customer might order COP chips at the rate of one million annually, paying just $0.50 apiece.

National Semiconductor Corp
2900 Semiconductor Dr, MS 16-174
Santa Clara, CA 95051
Phone (408) 721-5000

Status: Dataquest figures show COP continues to hold 2nd place in the mostly Asian-dominated 4-bit μC market. COP had 14½% of 4-bit market vs NEC's 1st-place 75XX, which had 16%. Total COPS unit shipments were 37½M units; 31M were from prime source National. Note that National's COP800 (next directory entry) is similar to COP400 in name only; it has a different architecture and instruction set.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. ROMless 402 and 404 are available for development and low-volume production, as well as piggyback CPUs that carry standard EPROMs.
2. Some COP400 models and peripherals are configured with National Microbus serial I/O for easy exchange of data with low pin count.
3. CMOS chips have optional multi-input wake-up feature, improved timer, including interrupt-on-overflow; designed for increased ESD and latch-up margin.
4. 24- and 28-pin surface-mount packaging available for space-sensitive applications such as consumer goods.

I—DATA-MANIPULATION INSTRUCTIONS
Binary arithmetic (add and subtract) with BCD handled by add immediate of correction. Only logical is exclusive-OR. Can test individual bits in RAM
II—DATA-MOVEMENT INSTRUCTIONS
Direct and indirect movements between data RAM and accumulator. Like some other 4-bit, 1-chip μCs, makes use of clever built-in exclusive-OR in instruction to flip back and forth between nibbles of data strings
Combination instructions permit indexing forward and backward through data RAM
Move 8-bit pattern from instruction ROM to Q output register, also 8-bit table look-up on input
Can set up operating modes on serial I/O with software, turning it into counter if desired
I/O instructions to individually serve unique I/O ports
III—PROGRAM-MANIPULATION INSTR
Jump and jump indirect
Jump and return from subroutine (three levels of return stack; two for 410L)
Skip-type conditional test instructions
Vectored hardware interrupt
IV—PROGRAM-STATUS-MANIP INSTR
Set and carry bit, and interrupt enable (there's a special means for saving carry status upon interrupts)
V—POWER-SAVING INSTRUCTIONS
Halt instruction disconnects internal circuitry from clock, which lowers power consumption to few μA. Because chip is static CMOS, all registers retain data, and upon Reset, will restart from where left off.

Specification summary: Single-chip μC with split-memory architecture; 8-bit-wide instruction side (1k for 420 part) and 4-bit-wide data side (64 for 420 part). Considerable on-chip I/O despite small package size (28 pins for 420) including clocked serial/event-counter port. Family includes 30 devices with different memory and I/O options and fabricated in several device technologies, including basic metal-gate NMOS and CMOS. Power for CMOS will vary from 3 mA at 14-μsec cycle to 120 μA at 64-μsec cycle (using 32-kHz watch crystal) and 2.4V supply. "Asleep" drain will be 6 μA max. Extended-temperature-range devices available, as well as extended-voltage-range devices.

COP400 FAMILY (CMOS MEMBERS)

PART NUMBER	MEMORY ROM (BYTES)	RAM (DIGITS)	I/O PINS	INTERRUPT	STACK	TIMER BASE COUNTER	SIZE (PINS)	OTHER
COP413C	0.5k	32	16	NO	2 LEVEL	NO	20	
COP413CH	0.5k	32	16	NO	2 LEVEL	NO	20	
COP410C	0.5k	32	19	NO	2 LEVEL	NO	24	
COP411C	0.5k	32	16	NO	2 LEVEL	NO	20	
COP424C	1.0k	64	23	1 SOURCE	3 LEVEL	YES	28	PMP
COP425C	1.0k	64	20	NO	3 LEVEL	YES	24	PMP
COP426C	1.0k	64	16	NO	3 LEVEL	YES	20	PMP
COP444C	2.0k	128	23	1 SOURCE	3 LEVEL	YES	28	PMP
COP445C	2.0k	128	20	NO	3 LEVEL	YES	24	PMP

NOTE: PMP IS POST-METAL PROGRAMMING.

COP400 FAMILY (NMOS MEMBERS)

PART NUMBER	MEMORY ROM (BYTES)	RAM (DIGITS)	I/O PINS	INTERRUPT	STACK	TIMER BASE COUNTER	SIZE (PINS)	OTHER
COP410L	0.5k	32	19	NO	2 LEVEL	NO	24	
COP411L	0.5k	32	16	NO	2 LEVEL	NO	20	
COP413L	0.5k	32	16	NO	2 LEVEL	NO	20	PMP
COP414L	0.5k	32	16	NO	2 LEVEL	NO	20	PMP
COP420	1.0k	64	23	1 SOURCE	3 LEVEL	YES	28	MICROBUS
COP421	1.0k	64	20	NO	3 LEVEL	YES	24	
COP422	1.0k	64	16	NO	3 LEVEL	YES	20	
COP420L	1.0k	64	23	1 SOURCE	3 LEVEL	YES	28	PMP
COP421L	1.0k	64	20	NO	3 LEVEL	YES	24	PMP
COP422L	1.0k	64	16	NO	3 LEVEL	YES	20	PMP
COP440	2.0k	160	36	4 SOURCES	4 LEVEL	YES	40	MICROBUS
COP441	2.0k	160	23	4 SOURCES	4 LEVEL	YES	28	MICROBUS
COP442	2.0k	160	19	2 SOURCES	4 LEVEL	YES	24	
COP444L	2.0k	160	23	1 SOURCE	3 LEVEL	YES	28	
COP445L	2.0k	160	20	NO	3 LEVEL	YES	24	

NOTE: PMP IS POST-METAL PROGRAMMING.

HARDWARE — SUPPORT — SOFTWARE

Mole (microcomputer on-line emulator) consists of two hardware components and software for a host computer. The two hardware components are a general-purpose Brain board common to all National microcontroller μCs and a personality board specific to the particular National μC being supported (which plugs into the Brain board). COP is supported by one of the personality boards.
The general-purpose Brain board works in conjunction with a terminal or host computer such as the IBM PC. With the personality board plugged in, it provides platform for both hardware and software development. **Application hot line:** (408) 721-5582.

Mole software is intended for user's host computer and is written for MS-DOS and CP/M. Includes COP cross-assemblers.

COP800

8-BIT CMOS

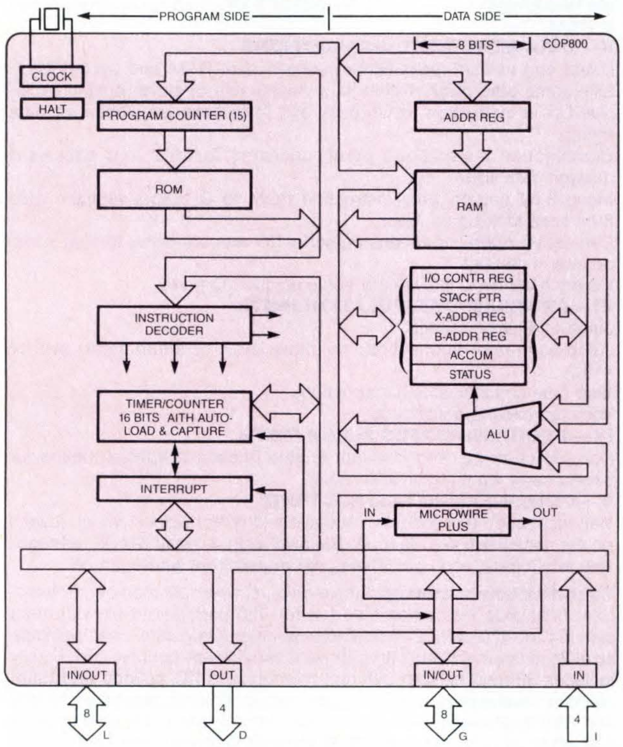
AVAILABILITY: Now.
COST: $2 to $5 for standard parts, 10k qty.
SECOND SOURCE: Sierra Semiconductor.
CORE: Sierra is using COP800 core for custom designs for portable medical monitors and home security, etc. Successful silicon has been achieved, Sierra says. Expect the standard cells to appear in National's ASIC library, too.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

Description: 8-bit CMOS 1-chip family in which a purposely simple core µP is surrounded by varying amounts of memory, peripheral functions, and I/O. Some 20 parts exist or are in the works and many more are forecast for future. Initial core has provision for addressing 32k-byte program memory and 256-byte data memory, but that can be expanded in future. The program and data memory are treated separately so, like the 4-bit COP400, the COP800 has a Harvard architecture. Otherwise it seems more similar to Von Neumann common-memory machines such as Motorola's 6805 or National's 16-bit 1-chip device, the HPC.

Status: Having gained one of the leadership positions in the 4-bit microcontroller field with its COP400, and having gotten 16-bit microcontrollers off to a start with its HPC 16040, National has introduced this 8-bit controller to fill gap in between. The architecture of the core µP seems quite simple—a bit like the Motorola 6508. National explains that it purposely kept the core simple and straightforward to leave room for lots of memory, peripheral functions, and I/O. National considers the family as its entry into ASICs.

HARDWARE — CHARACTERISTICS — SOFTWARE



COP800 FAMILY

PART NUMBER	MEMORY ROM (BYTES)	MEMORY RAM (DIGITS)	I/O PINS	INTERRUPT	STACK	TIMER BASE COUNTER	SIZE (PINS)	OTHER
COP820C	1.0k	64	24	3 SOURCES	IN RAM	1	28	
COP821C	1.0k	64	20	3 SOURCES	IN RAM	1	24	
COP822C	1.0k	64	16	3 SOURCES	IN RAM	1	20	
COP8720C	1.0k*	64	24	3 SOURCES	IN RAM	1	28	EEPROM IN ROM
COP8721C	1.0k*	64	20	3 SOURCES	IN RAM	1	24	EEPROM IN ROM
COP8722C	1.0k*	64	16	3 SOURCES	IN RAM	1	20	EEPROM IN ROM
COP840C	2.0k	128	24	3 SOURCES	IN RAM	1	28	
COP841C	2.0k	128	20	3 SOURCES	IN RAM	1	24	
COP888CF	4.0k	128	33/37	10 SOURCES	IN RAM	2	40/44	2 PWM TIMERS & A/D CONVERTERS
COP888CG	4.0k	192	33/39	14 SOURCES	IN RAM	3	40/44	3 PWM TIMERS & UART
COP888CK	4.0k	128	33/39	10 SOURCES	IN RAM	2	40/44	2 PWM TIMERS, A/D CONVERTERS, & UART

*EEPROM

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, subtract and carry
Logicals include rotates, shift compares and conditionals
Decimal correct
Increment and decrement
Bit manipulation: set, reset, and test individual bits in data memory, which includes those in data registers and I/O ports
II—DATA-MOVEMENT INSTRUCTIONS
Load and exchange instructions with optional automatic post increment or decrement of the associated pointer. Most allow the use of either the B or X pointer. Decrement register and skip if zero
III—PROGRAM-MANIPULATION INSTR
Jump instructions: relative, absolute, absolute long, indirect
Subroutine, subroutine long, return and skip (subroutine levels are limited only by the amount of available RAM)
Push and pop
IV—PROGRAM-STATUS-MANIP INSTR
ALU-driven decision bits in status register (PSW) appear limited to carry and half-carry flags. These, as well as interrupt control bits for various on- and off-chip interrupt sources, can be set and reset
V—POWER-SAVING INSTRUCTIONS
Halt mode, entered by setting data bit and exited by resetting bit
Note:
1. Program-branch decisions are implemented in skip-the-next-instruction manner.

Specification summary: 8-bit Harvard (split-memory) architecture µC in CMOS. 15-bit program counter (PC) can address 32-byte program memory, which can include data and data tables. Initial on-chip memory selections will be 1k, 2k, and 4k bytes. 8-bit data-address register can address 256-byte data. All data, control, and I/O registers are mapped into data-side memory space. Two bidirectional 8-bit and two unidirectional 4-bit I/O ports max. Each I/O pin has software-selectable options to adapt the chip to specific applications. Part may be operated in ROMless mode to provide for emulation and for applications requiring external program memory, in which case external memory is accessed serially via the two 4-bit ports. On-chip peripheral functions include software-selectable use assignment of as many as 39 I/O pins, 3-wire serial I/O, 16-bit timer/counter with capture register and auto reload, and a multisource (8) interrupt. Each part has an EEPROM equivalent planned for full "form-fit" function emulation. Maximum speed is 1-µsec instruction cycle (most instructions take one cycle), and because part is static CMOS, it will run down to dc and won't lose data in memory. Clock for 1-µsec cycle is 20 MHz (10 MHz for COP888). Fabricated in double-metal 2-µm (1½ µm on way) silicon-gate CMOS. Operates over 2.5 to 6V range and draws 9 mA running full speed at 1-µsec cycles, but less than 1 µA when halted. Enclosed in 20-, 24-, 28-, and 40-pin DIPs and surface-mount packages. MIL-spec versions are planned.

Notes:
1. Diagram shows basic COP800 family architecture. Over 10 basic parts planned for the family. Each has an emulator part created by replacing standard masked-ROM with EEPROM.
2. The basic core, including CPU and some peripherals, is only 66 mils per side (4330 mils sq area), thus only taking up ⅒th of reasonable-sized chip (200 mils per side or 40k sq mils area) and leaving adequate room for not only basic memory and I/O but also for UARTs, A/D converters, additional timers, LCD display drivers, and custom features for specific applications. Sierra says cost of ASIC design can be as low as $40k up front (16 weeks' time), meaning it can be cost competitive for 100k quantities.

HARDWARE — SUPPORT — SOFTWARE

Supported on National Mole (microcomputer on-line emulator), which consists of Brain mother board and COP800 personality board. Mole can be used in conjunction with IBM PC as host.

Cross-assembler for IBM PC and other computers.

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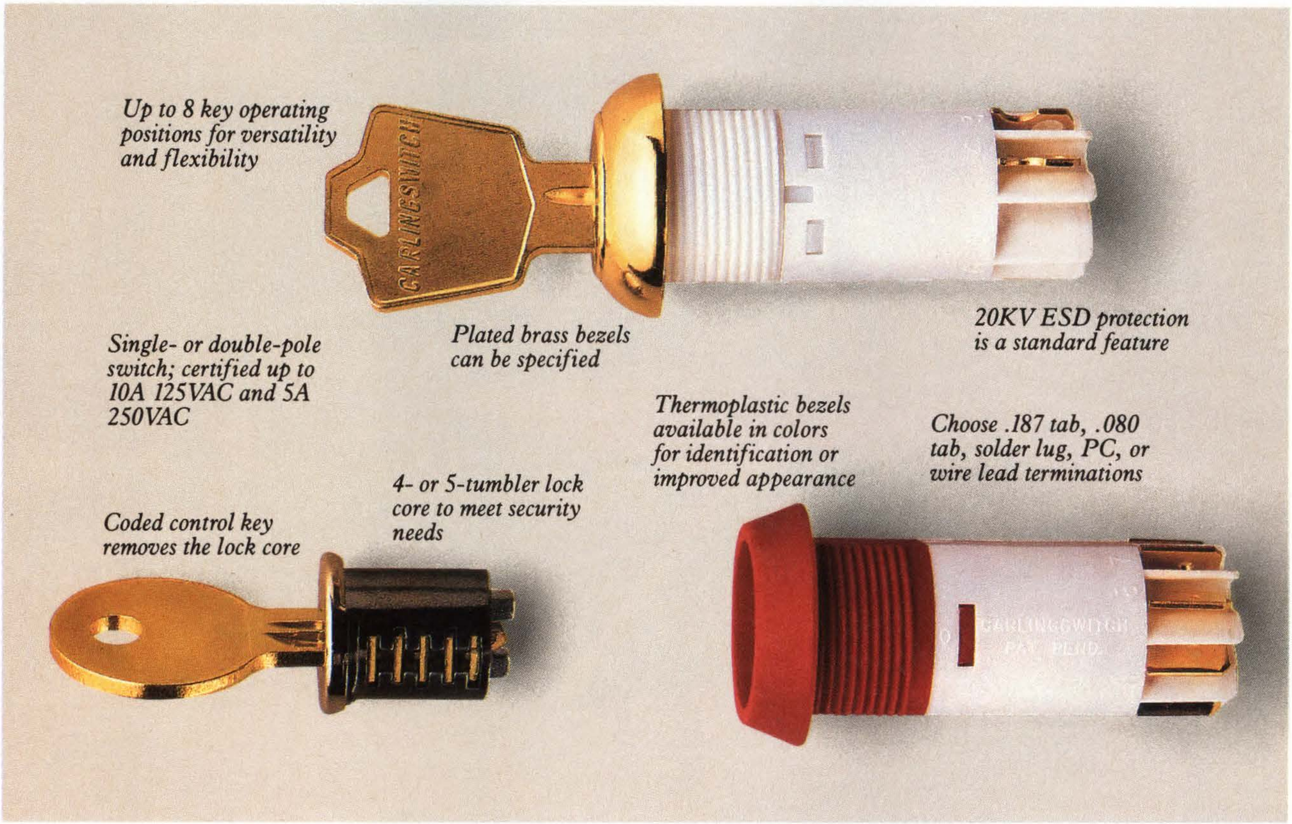

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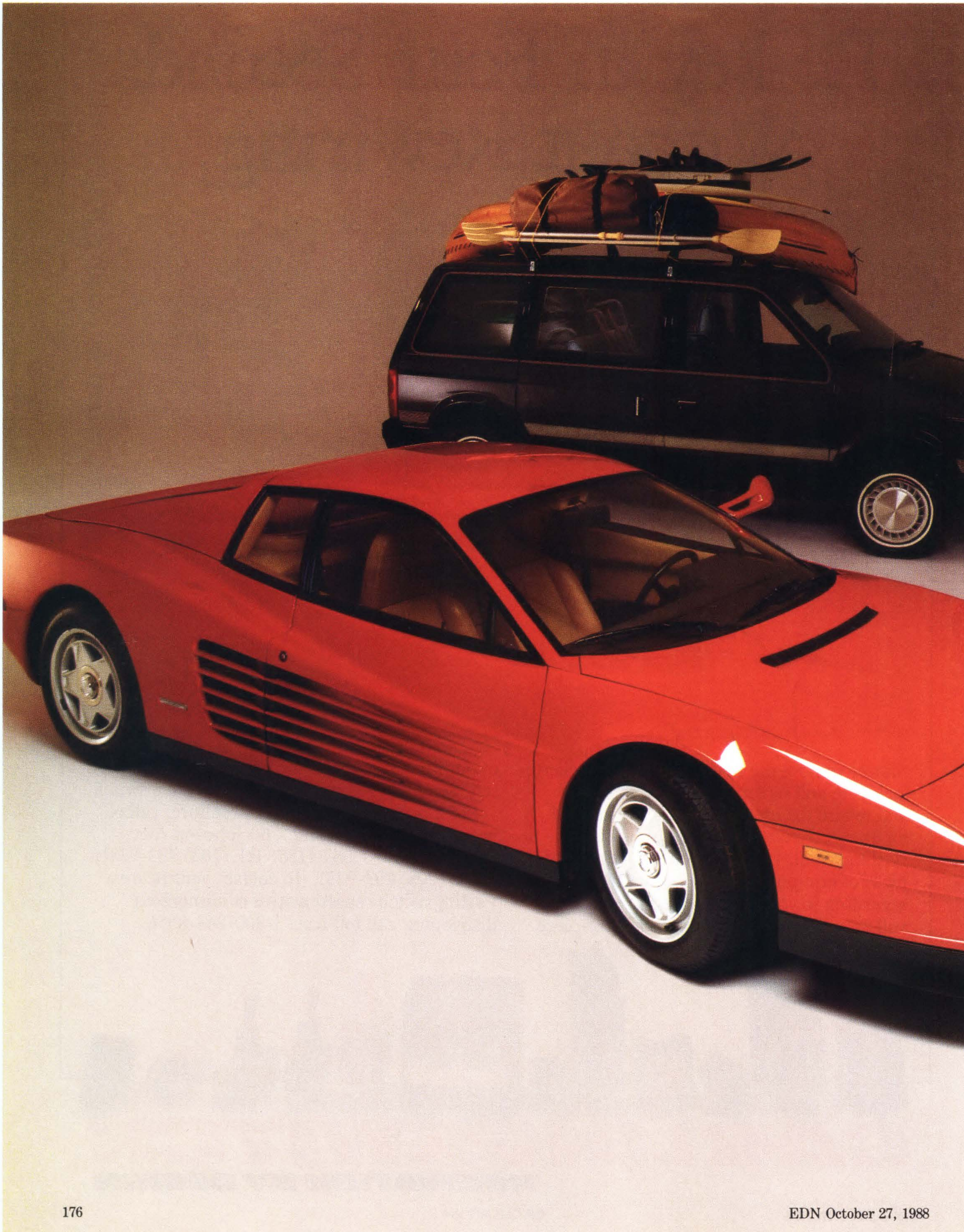
CIRCLE NO 144

National Semiconductor



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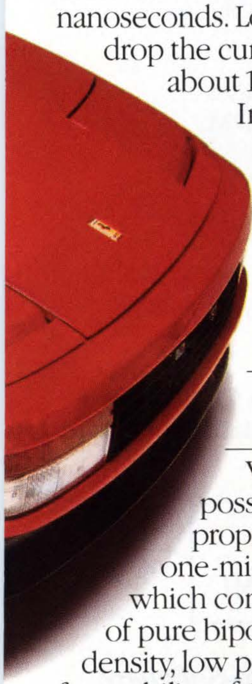
OUR NEW 256-KBIT BiCMOS ECL SRAM GIVES YOU BOTH HIGH SPEED AND HIGH DENSITY

Finally, you can go all out for system performance without being forced to use low-density SRAMs. This new device has an access time of only 15 nanoseconds. Yet it has the storage capacity of four 64-kbit ECL chips in one-fourth the space.

Its modest power consumption makes air cooling not only possible but practical. It draws a maximum of 200 milliamps at 15 nanoseconds. Longer cycle times drop the current down to about 120 milliamps.



In worst-case testing, power dissipation stays below a single watt. In typical applications, it's only 600 to 700 milliwatts.

BiCMOS III IS THE KEY

What makes it all possible is National's proprietary BiCMOS III one-micron process, which combines the speed of pure bipolar with the high density, low power, and manufacturability of CMOS.

It gives you the best ratio of speed, power and cost per bit.

NATIONAL MEMORIES

Volatile
ECL SRAMs
CMOS SRAMs

Non-Volatile
EPROMs
EEPROMs
PROMs

And we designed reliability into the process from the beginning. In fact, one-third of the development team had reliability as their sole responsibility.

The pay-off is a life test failure rate less than 50 FIT with more than 400,000 device hours. And a soft error rate less than 100 FIT. What's more, latch-up immunity is more than 200 mA. And ESD protection is greater than 2,000 volts.

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For more information on our new 256-kbit SRAM—or any other memory product—ask for a copy of our new memories brochure. Call us toll-free at (800) 252-4488, ext. 735.

National Semiconductor

CIRCLE NO 145

PIC1600 FAMILY

8-BIT CMOS

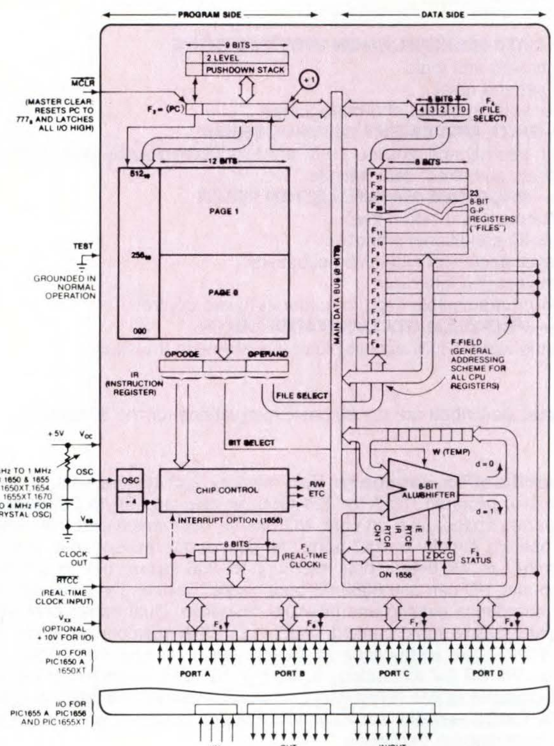
AVAILABILITY: Now.
COST: Projected at less than $2 to $5 in 25k qty, depending on speed and temperature specs and size of EPROM.
SECOND SOURCE: None.

Microchip Technology Inc
2355 W Chandler Blvd
Chandler, AZ 85224
Phone (602) 345-3287

Description: Family of small 1-chip static CMOS µCs that will use EPROM technology for both low- and high-volume production. Supplier says efficient 12-bit instruction word allows use of small EPROMs. Compact architecture also allows small die (100×105 mils for smallest part).

Status: It had begun to look like the 14-year-old PIC µP was nearing the end of its life—demand for existing NMOS parts had dropped to 2% of 8-bit µC market (4.6M units), according to Dataquest. But now the supplier—the successor to General Instrument—is bringing out its updated silicon-gate CMOS versions, and has added the twist of offering EPROMs for both low-volume production (in windowed packages) and high-volume production (windowless plastic packages). Supplier hopes to use its existing ability of mass-producing stand-alone EPROMs to offer users fast turnaround and prices competitive with masked-ROMs, even at high volumes.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram applies to original NMOS 1655A. See table for new CMOS parts.
2. 12-bit-wide instruction word allows all instructions to be single word, which produces compact code; supplier claims benchmarks show almost double the code efficiency of 8-bit instruction word.
3. All current devices are silicon-gate CMOS with 8-bit real-time clock counter, watchdog timer, and 2-level PC-save stack for subroutine nesting. No interrupts.
4. Security EPROM fuse for user's code protection.

PART	EPROM (BITS)	RAM (BITS)	I/O PINS	PACKAGE PINS
16C52	256×12	32×8	12	18
16C54	512×12	32×8	12	18
16C53	256×12	32×8	20	28
16C55	512×12	32×8	20	28

I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract
Logicals
Rotate right and left, decimal adjust
Swap halves
Bit set and clear

II—DATA-MOVEMENT INSTRUCTIONS
All RAM (general- and special-purpose registers) accessible by direct or indirect addressing
Page addressing
Move file

III—PROGRAM-MANIPULATION INSTR
Skip if zero (for comparisons and bit tests)
Move literal to W
Call subroutine
Go to routine

IV—PROGRAM-STATUS-MANIP INSTR
Can bit test on status-register carry, decimal carry, and zero

V—POWER-SAVING AND CONTROL INSTRUCTIONS
Sleep stops oscillator. CLRWDT clears watchdog timer. Tris instructs 3-state ports. Option loads option register.

Specification summary: Split-memory Harvard architecture with 12-bit-wide program EPROM and 8-bit-wide data registers (RAM). See table for EPROM and RAM sizes. Not expandable in memory because intended for self-contained, stand-alone applications. Instructions executed from dc to 200 nsec (20-MHz clock). Devices are fabricated in silicon-gate CMOS. Power consumption ranges from less than 1 µA with clock stopped to 30 mA at 20 MHz. In 18- and 28-pin DIPs and surface mount.

HARDWARE — SUPPORT — SOFTWARE

Supplier will resell a new PC-based development system that Audix (Bohemia, NY, (516) 737-5600) is readying for both the PIC and the TI 320 DSP that Microchip second sources. This development system will have user-friendly features such as extensive use of Microsoft Windows. Its price has been targeted at $3500 to $5000. It is scheduled for introduction later in '88.

Software will be bundled with the new Audix hardware development system. (Actually because the instruction set has not changed—just 6 added instructions—considerable software has existed for some time, including many application programs, such as for motor control.)

8048 FAMILY

8-BIT NMOS AND CMOS

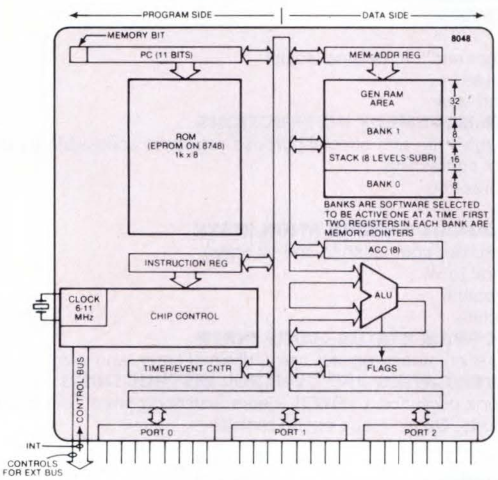
AVAILABILITY: Now.
COST: Masked-ROM parts less than $2 in high volume (100k qty). EPROM parts cost $18 in 100 qty. CMOS parts cost as low as $3 in 100k qty. Windowless-PROM parts cost $8 in 5k qty.
SECOND SOURCE: Toshiba, NEC, Signetics/Philips, National, Oki, Siemens, Fujitsu, GE-Intersil, UMC (Taiwan), with volume being spread out among suppliers.
CORE: Zymos has been using 80C49 as core for semicustom for a number of years. Others are following as 8048/49 combines widespread popularity with reasonably small core size.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Description: Broad family of 1-chip controller-type μCs, including version that can function as slave (8041). Basic models don't have serial communication ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

Status: Intel is still bullish about its 8048, saying total family shipments were reported to be 70 million in '87. However, we note that Intel chose the 8051 over the 8048 as the kick-off core for ASIC, and Intel says it has no definite plans to ever use the 8048 as an ASIC core.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram is for basic 8048. Table indicates some of other basic parts, most of which exist in both NMOS and CMOS.
2. CMOS parts are designated 80C48, 80C49, 80C50, etc.
3. There are many other variations on basic 8048 among the many suppliers. For example, Intel's 8041/42 chips are software compatible but can be configured as slaves to host μPs for interface applications. The National NS 405/455 uses the 8048 core as basis of a terminal controller. Siemens has telecomm-oriented 80C382/482. A number of semicustom houses use the 8048 as a core processor in their libraries.

PART NO	MEMORY (BYTES)			PACKAGE PINS	
	ROM	EPROM	RAM	PARALLEL I/O	TOTAL
8035	0	0	64	3×8	40
8048	1k	0	64	3×8	40
8748	0	1k	64	3×8	40
8039	0	0	128	3×8	40*
8049	2k	0	128	3×8	40*
8749	0	2k	128	3×8	40*
8040	0	0	128	3×8	40
8050	4k	0	256	3×8	40

*ALSO AVAILABLE IN 44-LEAD PLCC PACKAGE.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
Bit set and reset
Two working banks of 8-bit registers
II—DATA-MOVEMENT INSTRUCTIONS
Both internal and external RAM are fully accessible by instruction set.
Indirect and direct data fetches
III—PROGRAM-MANIPULATION INSTR
Decrement and skip if zero
Over 20 conditional branches
8-level stack with expansion capability
Two vectored interrupts
Two programmable flag bits under software control
IV—PROGRAM-STATUS-MANIP INSTR
Status word is fully accessible and is stored in the stack

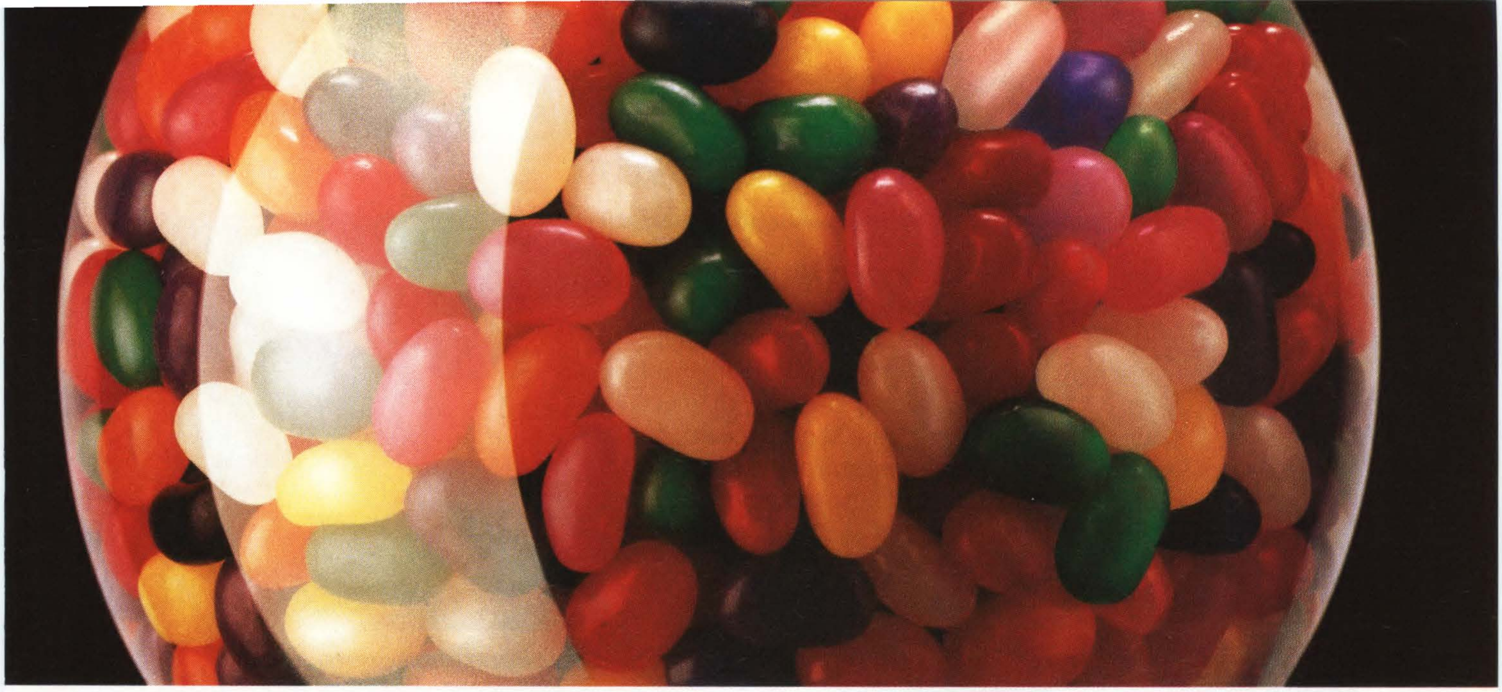
Note: Described are the 90 basic instructions for the 8048/8748.

Specification summary: Split-memory architecture with 1k to 4k bytes of program ROM (or EPROM) on chip and 64 to 256 bytes in separate space, also on chip. I/O has its own space and instructions to operate directly on I/O ports. All spaces are expandable: program memory to 4k bytes, data memory to 256 bytes, I/O to unlimited amounts. I/O can use 8080/85 peripherals. Devices have 8-level stack for subroutine nesting and interrupt response. Dual banks of working registers allow rapid context switching. Family members execute their 1- and 2-cycle instructions at 1-cycle times ranging from 1.36 to 15 μsec. NMOS 5V technology in 40-pin DIP and 44-pad chip carriers; UV-erasable ROMs (EPROMs) and windowless PROM parts are available. CMOS versions available with idle and power-down features and optional flatpack packages.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Intel now plays down 8048 support, saying that there are now numerous third-party OEM suppliers of PC-hosted emulators for the 8048 family.
From NEC: Ekakit 84C-1 stand-alone emulator (less than $2000).

From Intel: ASM-48 package with linker to run on Intel microcomputer development systems running ISIS operating system ($1500 for 8-copy license).
From others: Because of the broad-based popularity of this family, dozens of independent sources of development and application software exist, including support on universal development systems from Tektronix, Applied Microsystems, etc.
Program library: Insite Library contains variety of application programs.



If this is how you see LEDs, the ad is over.

The popular myth goes something like this: "An LED, is an LED, is an LED." Or: "If you've seen one, you've seen them all." And of course: "LEDs? They're commodity products."

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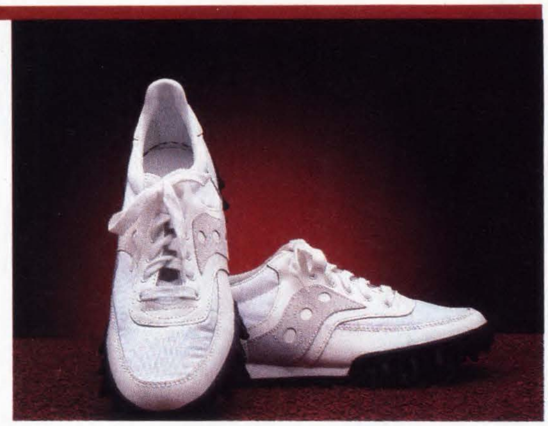
CIRCLE NO 147 See us at Wescon, Anaheim, CA Nov. 15-17



8051/8052 FAMILY

8-BIT NMOS AND CMOS

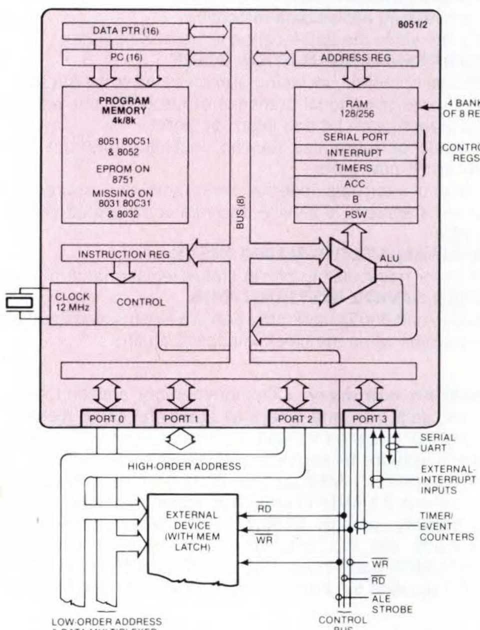
AVAILABILITY: Now for 8051, 80C51, 8031, 80C31, 8751, 87C51, 8032, and 8052, as well as special versions from second sources (see notes). Many other versions such as 80C451 and 83C451 available from Intel.
COST: $4.50 in 100k qty for 8051; $32 in 1k qty for 8751; $6.50 in 100 qty for 80C51; $5.35 in 100k qty for 8052; $44 for 87C51; $70 for EEPROM UPI-452 slave version, 1k qty.)
SECOND SOURCE: Siemens, Signetics/Philips, AMD, Fujitsu, Oki, and Harris-Matra (France) licensed.
CORE: Intel's ASIC Components Group is using the 8051 as its starting μP core. RCA and Fujitsu also using it as an ASIC core.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Description: Expandable single-chip "controller," an enhanced version of the same supplier's widely used 8048 family. Architecturally, it features the more "regular" nonpaged form of addressing for easier programming, more interrupts with extra RAM register banks to service them, increased stack depth, and new instructions such as multiply, divide, and compare. In peripheral support, it adds a full-duplex hardware UART and enlarged timer/counter capability.

Status: Generally thought of as the leader among the newer, more powerful 8-bit 1-chip μCs. It faces stiff competition from both high-end 8-bit μCs, such as Mitsubishi's 50740 version of the 6500/1, Motorola's 68HC11, NEC's 7811, Hitachi's 647180, and National's COP800, as well as from the new 16-bit μCs, such as Intel's own 8096 and National's 16040.

HARDWARE — CHARACTERISTICS — SOFTWARE



Specification summary: Expandable 1-chip μC. Split-memory architecture has 4k- to 8k-byte ROM on chip and 128 to 256 bytes of RAM on chip. Memories each expandable externally to 128k bytes. Four 8-bit ports on chip, but only one of these remains a port when all off-chip expansions and on-chip special functions are used. Special functions included on chip are full-duplex hardware UART (to 500k baud), two or three 16-bit timer/counters, and interrupt system to service these internal functions along with two external interrupts with 3-to 7-μsec latency. Instructions are a superset of the 8048s, with paged addressing eliminated. At 12-MHz clock, most instructions take 1 μsec; multiply or divide requires 4 μsec. Supplier's high-density HMOS silicon-gate n-channel technology used to achieve small die size and good speed. Packaged in 40-pin DIP and 44-pad chip carriers. 8051 is also available in CMOS (80C51) with 12- or 16-MHz performance and idle/power-down modes.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, multiply, and divide
Bit manipulation, including complex tests on bits (and branching on results)
II—DATA-MOVEMENT INSTRUCTIONS
Register addressing for the eight working registers in the four register banks
Direct, immediate, and indirect data addressing for more general data accessing
Table look-up in ROM via data pointer
III—PROGRAM-MANIPULATION INSTR
Depth of subroutining limited only by available space in 128-or 256-byte on-chip RAM
Conditional jumps on status-register flags
Conditional jumps on comparisons
Vectored interrupts to service two external interrupts, timers, and UART
IV—PROGRAM-STATUS-MANIP INSTR
CPU's program-status word fully accessible via software. Status bits in timer and UART also software accessible

Notes:
1. The 14 members of the 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip ROM. The 8051 and 80C51 incorporate 4k bytes of masked ROM. The 8751 and 87C51 have 4k bytes of EPROM. The 83C51FA has 8k bytes of masked ROM and a programmable counter array (PCA). The 87C51FA has 8k bytes of EPROM and a PCA. The 8031, 80C31, and 80C51FA have no on-chip ROM. (Hence, because it must use ports to access external memory, only port 1 is available for I/O.) The 8052 has 8k bytes of masked ROM. The 8032 has no on-chip ROM. The 8052 and 8032 have 256 bytes of on-chip RAM.
2. The 8051's so-called Boolean-processor capabilities refer to the way instructions can single out bits in RAM, accumulators, I/O registers, etc, and perform complex bit tests and comparisons, then execute relative jumps based on results.
3. The slave version of the 80C51, the UPI-452, is counterpart of UPI-42 (8041/42) for 8048 family. It is intended for software-customizable interfaces.
4. Intel has one model of 8052 preprogrammed with a full Basic interpreter.
5. Siemens has developed proprietary enhancements called 80515/535. They feature 16k ROM, with additional I/O ports, 15-μsec 8-bit A/D with eight input channels, 12 interrupts with four programmable priority levels. They are 12-MHz (1-μsec cycle) NMOS, packaged in TAB (Micropack).

HARDWARE — SUPPORT — SOFTWARE

From Intel: ICE-5100/252 in-circuit emulator ($5495) supports the entire MCS-51 family including 8051, 8052, and 80C52. Comes with macroassembler and editor. The emulator is hosted on an IBM PC AT/XT running DOS 3.1 or later, as well as Intellec Series III/IV development systems. ICE-51 in-circuit emulator ($4995) hosted on Series III/IV Intellec supports 8051 at 12 MHz.
SDK-51 System Design Kit ($950) is a single-board computer for low-cost development of 8051 applications.
From Siemens: Meta-ICE-80515 in-circuit emulator for 80515, hosted on IBM PC.

From Intel: ASM-51 and PL/M-51, both containing a relocation and linkage utility, are available for the IBM PC and Intel microcomputer development systems.
From others: A number of third-party software suppliers have developed C compilers for 8051 that have special features suited to microcontroller applications. Among these are Micro Computer Control (Hopewell, NJ) for $1495 and Archemides Software (San Francisco, CA) for $851. Both are hosted on IBM PC.

6804/6805

8-BIT NMOS AND CMOS

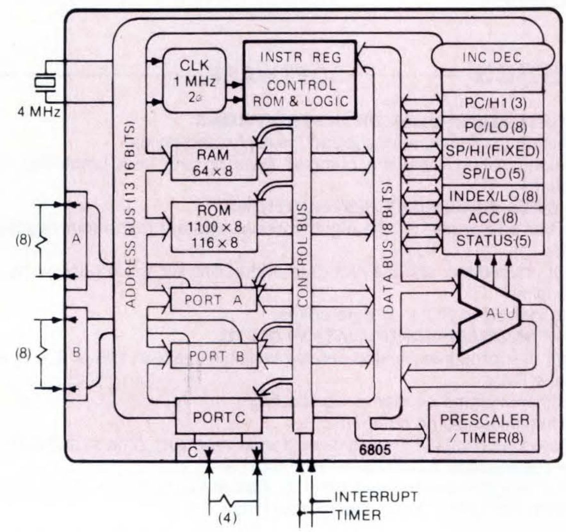
AVAILABILITY: Now for most models.
COST: $0.49 to $40. The $0.49 is 1M qty of 6804J1 (500k minimum order). CMOS parts remain more expensive than NMOS.
SECOND SOURCE: Hitachi, RCA, and Thomson; RCA for CMOS parts only.
CORE: Motorola and NCR have joint ASIC pact that will use CMOS 6805 as core along with NCR's similar 6502 μP core. (SGS has S6 core, which has somewhat similar architecture to 6804.)

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

Description: Family of 1-chip μCs based loosely on 6800 architecture, but in some ways more like 6502 (especially 6805). Family offers various amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 2 MHz. Some parts contain on chip an A/D converter, EEPROM, serial I/O, and software security. The 6804s are meant for lowest-end applications. They use some serial data paths internally to reduce chip sizes.

Status: Supplier's steady commitment to this family over past 10 years has apparently paid off. It trails only the 8048/49 family (which has 20% of 8-bit-μC market) and the 50740 (which has 16%). RCA is concentrating its efforts on the CMOS side of family and is bringing out its own enhancements. Motorola continues to expand the 6805 family; it plans to add at least five 6805-derivative parts in 1988.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. Diagram is for nonexpandable Model P2 in 28-pin package.
2. Comparison of 6805 with 6800: Stack pointer has only five working bits, so stack is only 32 bytes deep. Only one accumulator. Index register only 8 bits wide, so it can only span 256 memory locations. Program counter only 11 bits (adequate for P2's 2k-byte RAM+ROM memory space). Only one external interrupt.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Program is initiated by special pin.
4. RCA has emulator versions (68EM05/C4,D2) for prototyping and low-volume production. These are ROMless devices with all ROM access buses brought out for direct interfacing to industry-standard EPROMs. Come in 40-pin piggyback (for 2764).

I—DATA-MANIPULATION INSTRUCTIONS
All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test (bit tests can be made quite generally on all I/O and memory bits). 68HC05 has 8×8 multiply
II—DATA-MOVEMENT INSTRUCTIONS
Relative addressing allows data relocation
True indexing within the 256-location limits of 8-bit index
III—PROGRAM-MANIPULATION INSTR
18 conditional branches, including branch of interrupt line test
Mostly the same conditional branches of the 6800, but with more emphasis on branch upon bit and interrupt tests
Only 15 levels of subroutine nesting, including interrupt returns; 31 levels on certain new parts
Four sources of interrupts: external, timer, software, and reset. 68HC05 has vectored interrupts to service its serial communication and peripheral interfaces
IV—PROGRAM-STATUS-MANIP INSTR
Instructions for manipulating bits in status register (and in timer)
V—POWER-SAVING INSTRUCTIONS
CMOS 6804s and 6805s have Stop and Wait instructions and will safely reset themselves when the clock is applied again

Specification summary: Common-memory architecture, in which instructions, data, I/O, and timers all share the same memory space. This allows I/O to be bit rotated, bit manipulated, etc. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most -05 versions. New 68HC05s have a 2.1-MHz internal bus speed. Included are parts with program security, on-chip EEROM, A/D converter, serial peripheral interface (SPI), and PLL frequency synthesizer. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs (also chip carriers, etc). NMOS requires 5V supply, while CMOS will operate over 3 to 6V.

FAMILY		SPEED BUS (MHz)	INSTR	ON-CHIP ROM	MEM RAM	I/O PINS	TIMER	INTER-RUPTS	POWER CONSUMPTION (mW)	PINS
6804	MIN	0	42	0.5k	32	16	—	3	0.01	20
	MAX	2	42	2k	128	20	YES	4	~400	28
68HC04 P4			42	3744	156	20 +2	YES	1	NA	28
6805	MIN	0	51	1k	64	16	—	3	0.01	28
	MAX	2	59	4k	176	32	YES	5	~700	40
68HC05	MIN	0	62	2k	96	32	YES	2	0.25	40
	MAX	2.1	62	7.7k	176	32	YES	2	0.25	40

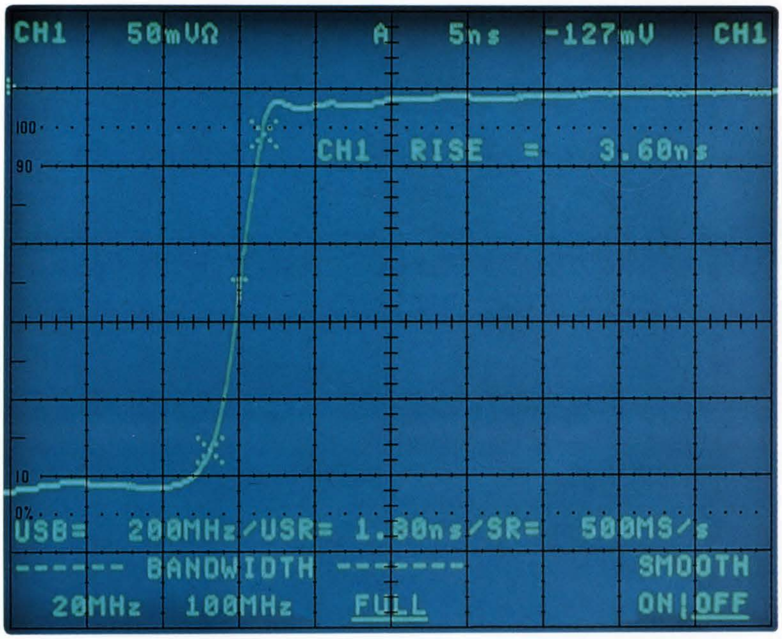
NOTES:
1. CMOS VERSIONS CAN BE STOPPED (CLOCK = DC). IN THIS CONDITION POWER DROPS TO 10 μW.
2. SOME 6805 DEVICES CAN BE EXPANDED EXTERNALLY TO 8k MEMORY. RCA 6805E3 BRINGS OUT 16 LINES FOR 64k ADDRESS SPACE.
3. SPECIAL FUNCTIONS SUCH AS SERIAL COMMUNICATION PORTS & A/D CONVERTERS ARE AVAILABLE AMONG FAMILY MEMBERS.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: HDS-200 hardware/software development station; operates stand-alone or interfaced to virtually any host with an RS-232C line (including Motorola's Exor-trademarked stations). The less-costly 68705EVM (HMOS) or 1468705EVM (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.
From RCA: Single-board evaluation kit that will interface to IBM PC via RS-232C.
From others: A number of third-party companies provide hardware emulators for the 6805 family: Sophia Systems (Santa Clara, CA), American Automation (Tustin, CA), etc. Most of these interface to IBM PCs.

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733.
From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has cross-assemblers for 6805 and 6804 that run on IBM PC, etc.

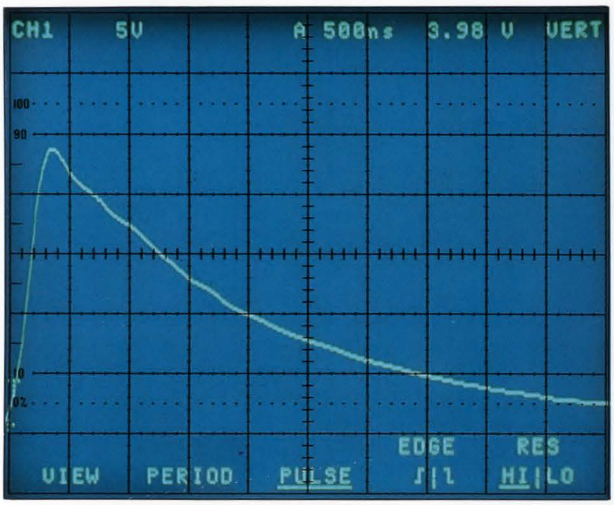
NEW 500 MEGASAMPLES/SEC 300 MHz DIGITAL PORTABLE



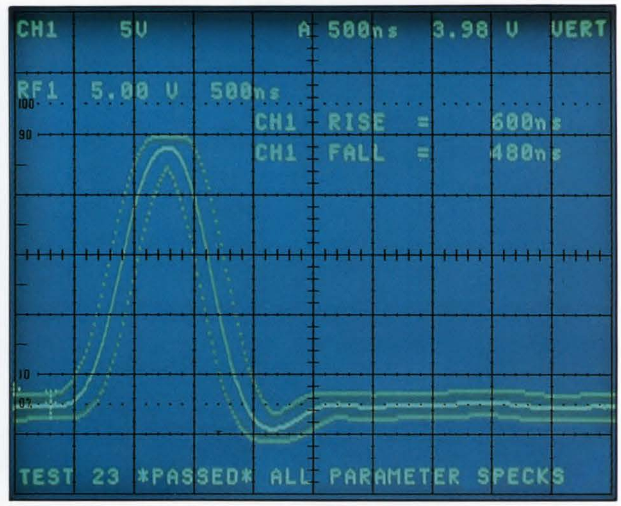
TEK PUSHES THE LIMIT...

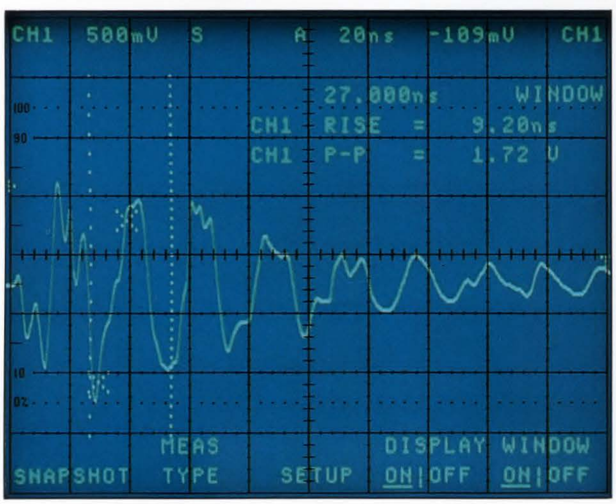
AT THE PUSH OF A BUTTON.

AUTO SETUP

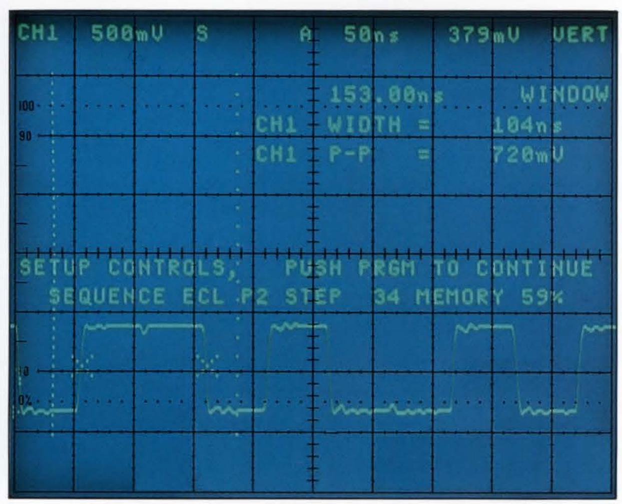


AUTO PASS/FAIL





AUTO MEASURE



AUTO SEQUENCE

ONLY FROM TEK.

The new Tek 2440 Digital Oscilloscope is the only portable offering a 500 MS/s sampling rate—on *two* channels simultaneously.

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You can digitize, store and process single-shot phenomena to 200 MHz and repetitive signals to 300 MHz. At the touch of a button.

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On the design bench, the 2400 DSOs are effective standalone test systems. Full GPIB programmability, pass/fail testing and time-saving measurement sequencer make them equally powerful system components. With off-the-shelf software you can fully automate measurements and extend waveform analysis.

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PXA-894

6801/6301/68HC11 — 8-BIT NMOS AND CMOS

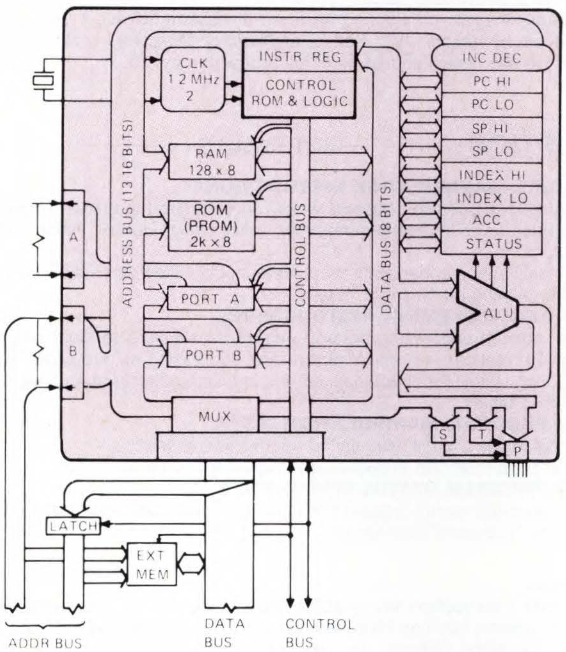
AVAILABILITY: Now.
COST: In 1k qty, from less than $3 to $40.
SECOND SOURCE: Hitachi, Thomson. Hitachi is prime source for the 63XX CMOS versions.

Description: 6801 is large, expandable 1-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8×8 multiplication, and a multifunction 16-bit timer. 6301 is slightly enhanced CMOS, and 68HC11 is further enhanced in static CMOS. 68HC11 has a second 16-bit-wide register, an 8-function timer, a 2-function pulse accumulator, an enhanced UART (SCI), a high-speed (1-MHz) serial shifter (SPI), an 8-channel, 8-bit A/D converter, and an EEPROM.

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

Status: This has been a well-received family. Motorola is now following migration of customers to more powerful 1-chip devices and is concentrating on the new 68HC11 enhancement of the 6801, such as increased on-chip EEPROM. During late 1988, Motorola will offer the 68HC11E9 with 12k bytes of ROM and 512 bytes of EEPROM and the 68HC811E2 with no on-chip ROM, but with 2k bytes of EEPROM.

HARDWARE — CHARACTERISTICS — SOFTWARE



PART	DESCRIPTION	MEMORY ON CHIP ROM	MEMORY ON CHIP RAM	EXT	INTERNAL BUS SPEED	I/O PAR	I/O SER	TIMER EVENT CTR	EXT INTS	PINS
6801	EXPANDABLE 1-CHIP μC	2k	128	64k	0.5M–2.0M	29	3	3×16	2	40
68701	EPROM VERSION OF 6801	2k	128	64k	0.5M–2.0M	29	3	3×16	2	40
6803	ROMLESS 6801	—	128	64k	0.5M–2.0M	13	3	3×16	2	40
6301	CMOS	4k	128	64k	0–2.1M	28	3	1×16	2	40
6303	CMOS	—	128	64k	0–2.1M	17	3	1×16	2	40
68HC11	CMOS WITH UART, SPI, SERIAL, 8-BIT A/D	8k (ALSO 512 EEPROM)	256	64k	0–2.1M	28 32	6	4×16	2	48 (DIP) 52 (QUAD)

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
Instructions to take advantage of two accumulators, including 8×8 multiply. 68HC11 has additional 16-bit operations, integer and fractional divides, and bit manipulation
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions
Can list-process efficiently with the index register (two on 68HC11) and can add accumulator to index register, within a 64k-byte range
Relative addressing allows data relocation
Has 16-bit load and store
III—PROGRAM-MANIPULATION INSTR
Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM
Eight levels of prioritized, vectored interrupts (21 on 68HC11)
IV—PROGRAM-STATUS-MANIP INSTR
Instructions for storing status register or transferring to or from accumulator. 68HC11 has additional active bits related to "stop" mode
V—POWER-SAVING INSTRUCTIONS
6301 has sleep instruction. 68HC11 has Stop and Wait instructions similar to 146805 but with disabling provision via a bit in status register

Hardware Notes:
1. Diagram is for 6801. See table for others.
2. Hitachi has developed some slightly enhanced CMOS versions, the 63XX Series, that Motorola has second sourced. Zero turn-around time (ZTAT) versions, such as the 63701VOP, have EPROM program memories in inexpensive windowless packages for 1-time programming in moderate-volume production (to 10k).
3. Motorola 68HC11 is very much enhanced 6801. New 68HC11A8 has 512 bytes EEPROM. 68HC811A2 has 2k bytes EEPROM.

Notes:
1. 6801 has all 6800 μP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set, with 88 additional op codes.

Specification summary: Expandable single-chip μC with common-memory architecture, in which all instructions, data, I/O, control, and data registers share the same memory space. This allows I/O, etc, to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and, beyond that, 91 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 2.1 MHz for 68HC11. The 6801 is fabricated in NMOS, the 6301 is fabricated in CMOS, and the Motorola 68HC11 is fabricated in static CMOS (to allow dormant, micropower "asleep" state). 6801 in 40-pin DIP, 6301 in 64-pin DIP and flat pack, and 68HC11 in 48-pin DIP and 52-pin quad.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: For 6801 family, M68701EVM is evaluation module that has port for terminal and port for any RS-232C host and will program 68701 EPROM parts. For 68HC11, the similar M68HC11EVM. Also M68HC11EVB boards ($168.11) for evaluating EEPROM versions. For both 6801 and 68HC11, HDS-300 software-development station operates stand-alone or interfaced to most any host with RS-232C.
From others: Third-party hardware development systems. For example CT68HC11 ($5000 to $6000) from Ashling Microsystems Ltd (Limerick, Ireland).

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733. C compiler to run on Unix System V for 68HC11. For least expensive approach, you can use 6801 parts with LILbug monitor in on-chip ROM (MC6801L1).
From others: Cross macroassemblers and linking loaders, some relocatable, to run on popular minis and personal computers. For example, C compiler from Archimedes (San Francisco, CA) to run on IBM PC ($995) and DEC VAX ($3995 to $5995).

6500/1, 65C124, 50740, 37700

8-BIT (AND 16-BIT) NMOS AND CMOS

AVAILABILITY: Now for all NMOS and most 8-bit CMOS parts. Late 1988 for Mitsubishi 37700 16-bit internal part.
COST: Prices range from $2 to $20 according to complexity of part and volume, whether in NMOS or CMOS. Volume leader Mitsubishi says its prices range from $3 to $25.
SECOND SOURCE: NCR (licensed) and California Micro Devices for Rockwell NMOS parts. WDC says it has licensed a number of suppliers worldwide for its CMOS designs. Seiko and Epson second source Mitsubishi chips.
CORE: Standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, etc. Widely used because of compact 6502 die size.

Rockwell International
Semiconductor Products Div
4311 Jamboree Rd
Newport Beach, CA 92658
Phone (714) 833-4600

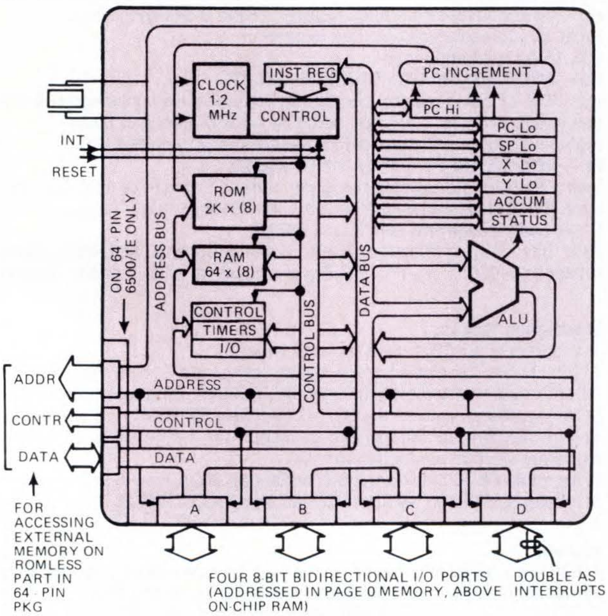
Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545

Mitsubishi Electronics America Inc
1050 Arques Ave
Sunnyvale, CA 94086
Phone (408) 730-5900

Description: There are three different sources for 1-chip versions of 6502 μP: the original 6500/1 NMOS family from Rockwell, the new 65C124 and -134 CMOS family from WDC, and the very successful 50740 CMOS family from Mitsubishi. Most parts are 100% software compatible with 6502, though in some cases enhanced instructions such as bit manipulation have been added. Because of small die size of 6502 core, many of these parts take a standard-cell ASIC approach. Vendors claim these 1-chip sets have a speed advantage over competing 1-chip devices, because of 6502's 2-cycle bus and pipelining.

Status: Mitsubishi's 50740 Series has become a top volume leader among 8-bit μCs, according to Dataquest, along with the 8048/49, 6805/6801, and 8051 μC families. Mitsubishi's explanation for rapid volume growth is that the 50740 is used in Japanese consumer products (Mitsubishi says you will find standard or custom 50740s if you open products by Hitachi, JVC, Sanyo, or Minolta). Mitsubishi is readying a pilot fab line, which should be in full production by '89.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram favors initial Rockwell 6500/1 version. There are dozens of versions from various sources, most of which are more complex.
2. Mitsubishi 740 Series parts are all CMOS and have as much as 16k bytes of ROM and 512 bytes of RAM. Some models have special functions such as UARTs, 8-bit A/D converters, LCD drivers, or high-voltage (−35V) outputs. Some have 54 pins of I/O.
3. Mitsubishi's new M37700 version will also be CMOS and 8 bits externally but will be 16 bits internally (much like the 68C816 version of the 6502 μP). On chip it will have 16k bytes of ROM, 512 bytes of RAM, eight 16-bit timers, two UARTs, one watchdog timer, and an 8-channel 8-bit ADC. It will be expandable to 16M bytes off chip. Initial package will be 80-pin quad flat pack for Japanese consumer market, but later it will be available in 84-pin PLCC for US market.
4. WDC says its first part, 65C124, has been joined by 65C134—a 6502 core μP—which includes a LAN connection.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM or I/O ports)
Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset
II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset limited to eight bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables
III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses
Nonmaskable and/or maskable interrupt, depending on model
IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits

Notes:
1. 6500/1 instruction set is 100% identical to that of previous 650X family devices such as 6502, with exception of bit-manipulation instructions for some devices. (No new instructions added to handle new on-chip features like timers and I/O because they are all handled as if in external memory space.)
2. Mitsubishi chips have some added instructions.

Specification summary: 1-chip nonexpandable and expandable versions of 650X family. Have 2k- to 16k-byte ROM, 64- to 512-byte RAM, as many as 52 I/O lines, and one or more 16-bit programmable interval timers, as well as two or more programmable interrupts (plus the 650X's NMI interrupt). Family options (Rockwell) include RS-232C port and bus expansion. Operates from 5V, 500 mW, and has separate 5V supply to keep 64 static bytes of RAM alive (50 mW required). Wide variety of package types and sizes from various suppliers ranging to 80-pin flat pack and 84-pin PLCC from Mitsubishi. Full MIL-spec temperature range devices from WDC.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: Emulator part, the 64-pin 6500/1E ($75), can be used in R6500/1 personality card ($995), which plugs into LCE System ($1250). Backpack part will be ROMless 40-pin 6500/1EA ($75), into which industry-standard EPROMs can be plugged.
From Mitsubishi: Debugging machine PC4000E ($1000) with ICE cards for each device model ($750 to $1100).
From WDC: Toolbox Design System in-circuit emulator (ICE) for W65C124 runs on an Apple IIGS host and can communicate with an IBM PC via a serial port ($4995).

From Rockwell: Because the 6500/1 emulator runs on LCE system and Aim-65 (now from Dynatem, Irvine, CA), existing 6502 program-development software can be used. A debug monitor is available for all 6500/1 and 6500/11 devices, and the macroassembler supports new (enhancement) instructions. Cross software.
From Mitsubishi: Cross software for MS-DOS. (Has plans for a C compiler and Forth interpreter.)
From WDC: Many software packages available from third parties for the W65C02/W65C816 μPs.

Z8, SUPER8

8-BIT NMOS AND CMOS

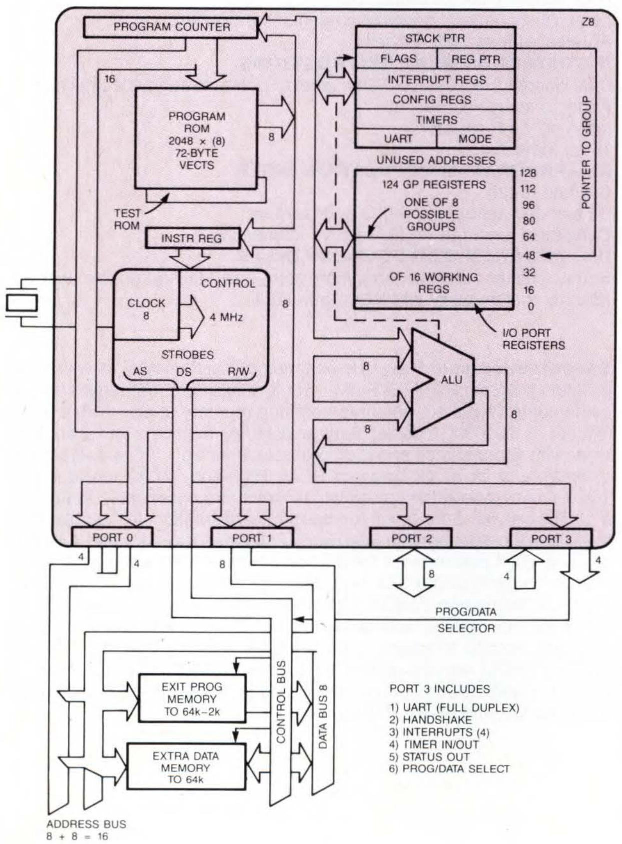
AVAILABILITY: Now for 2k-byte, 4k-byte, and ROMless parts at 8 to 12 MHz and Super8. Sharp and Zilog have CMOS now. SGS has 4k EPROM and 8k ROM and should have S9 core in late '88.
COST: Less than $3.50 for Z8 in volume. $6.50 for Super8 in volume. (28-pin version for $1.)
SECOND SOURCE: SGS-Thomson (licensed); Sharp for both NMOS and CMOS; Catalyst for EPROM version; VLSI Technology for CMOS.
CORE: From Zilog & VLSI Technology. (SGS-Thomson's S9 core is based on Super8 architecture.)

Description: Z8 is a "maxi" single-chip μC that is a composite of many machines. It has powerful features that can't necessarily be used simultaneously, a common problem with single-chip units—particularly the expandable ones. Not really compatible with supplier's Z80 or Z8000 because architecture is so different; closest to Z8000. However, slave Z8 versions interface to Z80 and Z8000 buses. New "Super8" version has more of everything: more data and program memory, more on-chip peripherals, more instructions.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

Status: Last year, supplier predicted Z8 would reach 7-million-unit level in '87, because of increasing demand for $1 28-pin Z8, which is directed at consumer applications. Dataquest showed a volume of 3.4 million for '86. Zilog points out that Z8 volume is still growing, and that Z8 has had several hundred design wins (many in Far East), and some of these are now going into production. Meanwhile, second-source SGS has turned its CMOS efforts to its S9, a proprietary enhancement of the Super8, which SGS will use for an ASIC building block.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, subtract with carry
Multiply and divide added to Super8 version
Logicals: AND, compare, complement, OR, and exclusive OR
Rotates and swaps
Bit manipulation: test under mask, test complement under mask, and logical tests of bits
II—DATA-MOVEMENT INSTRUCTIONS
Address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative
Block transfer: load constant autoincrement, load external autoincrement
Load: clear, load, load constant, load external, pop and push
III—PROGRAM-MANIPULATION INSTR
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, jump relative conditional, return
IV—PROGRAM-STATUS-MANIP INSTR
Set, reset, and complement of carry flag
Note: Ability to set, reset, and test any bit or combinations of as many as eight bits allows any byte to function as a user flag register.

Specification summary: Unique architecture with three memory spaces: program memory (0, 2k, 4k, or 8k bytes in internal masked ROM; rest to 64k bytes can be external), data memory (to 64k bytes external), and CPU register file (256-byte space that includes 124 truly general-purpose working register/accumulators). Executes 129 instructions at 0.6 to 3.0 μsec at 8-MHz internal clock (16-MHz oscillator). Has built-in duplex UART (96k bps) and two 8-bit timers, each with 6-bit prescaler. Housed in 40-pin DIP, with 28-pin economy versions planned. New enhanced Super8 has 352 bytes of on-chip data and control registers (256 of which are general purpose). Initially it will be a ROMless part, but as much as 16k bytes of on-chip program ROM are expected. New multiply and divide instructions. On-chip peripheral functions include DMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has fast (600-nsec) interrupt response, with 37 interrupt sources. Comes in 48- and 44-pin packages.

Notes:
1. Diagram applies to basic 2k-byte version. Many other versions exist.
2. The 124 working registers (272 on Super8) are truly general purpose. Any one can be used as accumulator or indexer.
3. The register pointer singles out a "workspace" of 16 working registers for fast access. Eight such workspaces are possible in the 124-register space (16 in Super8) and provide mechanism for fast context switching upon interrupt.
4. The data- and program-manipulation instructions use the working registers in the CPU. The instructions that apply to the external data RAM are essentially just loads and stores. (There is a similarity to RISC philosophy.)
5. SGS has not announced any CMOS Z8s. Instead it has introduced an S9 ASIC core in 1.5-μm CMOS. SGS says it will reach 12 MHz (24-MHz external clock) and be priced at $4 to $10 in volume.

HARDWARE — SUPPORT — SOFTWARE

Development packages are available from JK Engineering (Singapore, 65-744-8414). In the US, IAM (Sacramento, CA) distributes JK Engineering's products. Development packages in various configurations are also available from Zilog Inc (Campbell, CA) and Inner Access (Belmont, CA). Emulation packages are available from Orion Instruments (Redwood City, CA); Microtek (Beaverton, OR); Creative Technology (Atlanta, GA); and Sophia Systems (Santa Clara, CA). This list isn't exhaustive.

Software development tools are available from Allen Ashley (Pasadena, CA); Avocet (Rockport, ME); Relational Memory Systems (San Jose, CA); and Western Wares (Norwood, CO). You can purchase compiler software from Micro Computer Compilers (Hopewell, NJ); 2500 AD (Buena Vista, CA); and Inner Access (Belmont, CA). This list isn't exhaustive.

7000 FAMILY

8-BIT CMOS

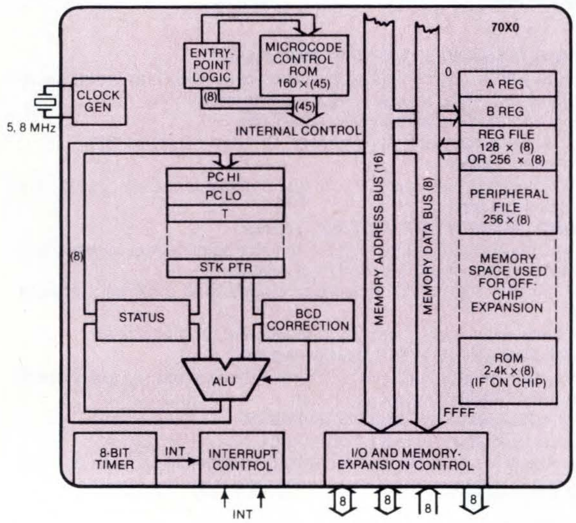
AVAILABILITY: Now.
COST: TI pricing: $1.60 to $3.50 for standard CMOS masked-ROM versions in 100k quantities.
SECOND SOURCE: Microchip Technology and Seeq for NMOS versions only. Note that each supplier is taking a different direction, so direct second sourcing is limited.

Texas Instruments Inc
13536 N Central Expressway
Dallas, TX 75265
Phone (214) 995-6611

Description: Software-compatible family of NMOS and CMOS 8-bit, expandable 1-chip μCs. Architecture laid out on chip so that new product variations in memory size, I/O, etc, are easier to accomplish. A full-duplex UART, enhanced timers, and interrupts are incorporated in high-end family members (70C42). Instructions typically perform combined load, operation, and store functions, thereby increasing overall system performance and code efficiency.

Status: Primary supplier TI has apparently switched its emphasis to new CMOS models with expanded features. New low-end devices (70CT20/40) continue to offer an alternative for designers who are using 4-bit μPs, but who seek a low-cost 8-bit alternative.

HARDWARE — CHARACTERISTICS — SOFTWARE



Note:
Supplier says it uses a "strip-chip" architecture to keep registers and control elements in isolated, self-contained modules in silicon, and then it uses single layer of metal to interconnect chip. This is, of course, similar to the cell-library, semicustom approach and useful for the same reason. Changes can be made easily, which helps TI bring out new models or give large customers special variants.

MODEL	ROM (BYTES)	RAM (BYTES)	CLOCK (MHz)	I/O	INTERRUPT LEVELS	POWER REQUIRED V	POWER REQUIRED mW
70C00	0	128	5	32	4	2.5–6.0	30
70C20	2k	128	5	32	4	2.5–6.0	30
70CT20	2k	128	5	20	4	4.5–5.5	30
70C40	4k	128	5	32	4	2.5–6.0	30
70CT40	4k	128	5	20	4	4.5–5.5	30
70C02	0	256	6	32	6	2.5–6.0	30
70C42	4k	256	6	32	6	2.5–6.0	30

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8×8 multiply, BCD
Logicals, increment, decrement (single and double)
Rotates right and left. Bit test
II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator
Apply to many instructions
Indexing via B register
16-bit moves
III—PROGRAM-MANIPULATION INSTR
Call and return
Bit test and jump on both I/O and memory
Conditonal jumps using PC-relative addressing
IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, and interrupt enable. Instructions to change carry and interrupt enable

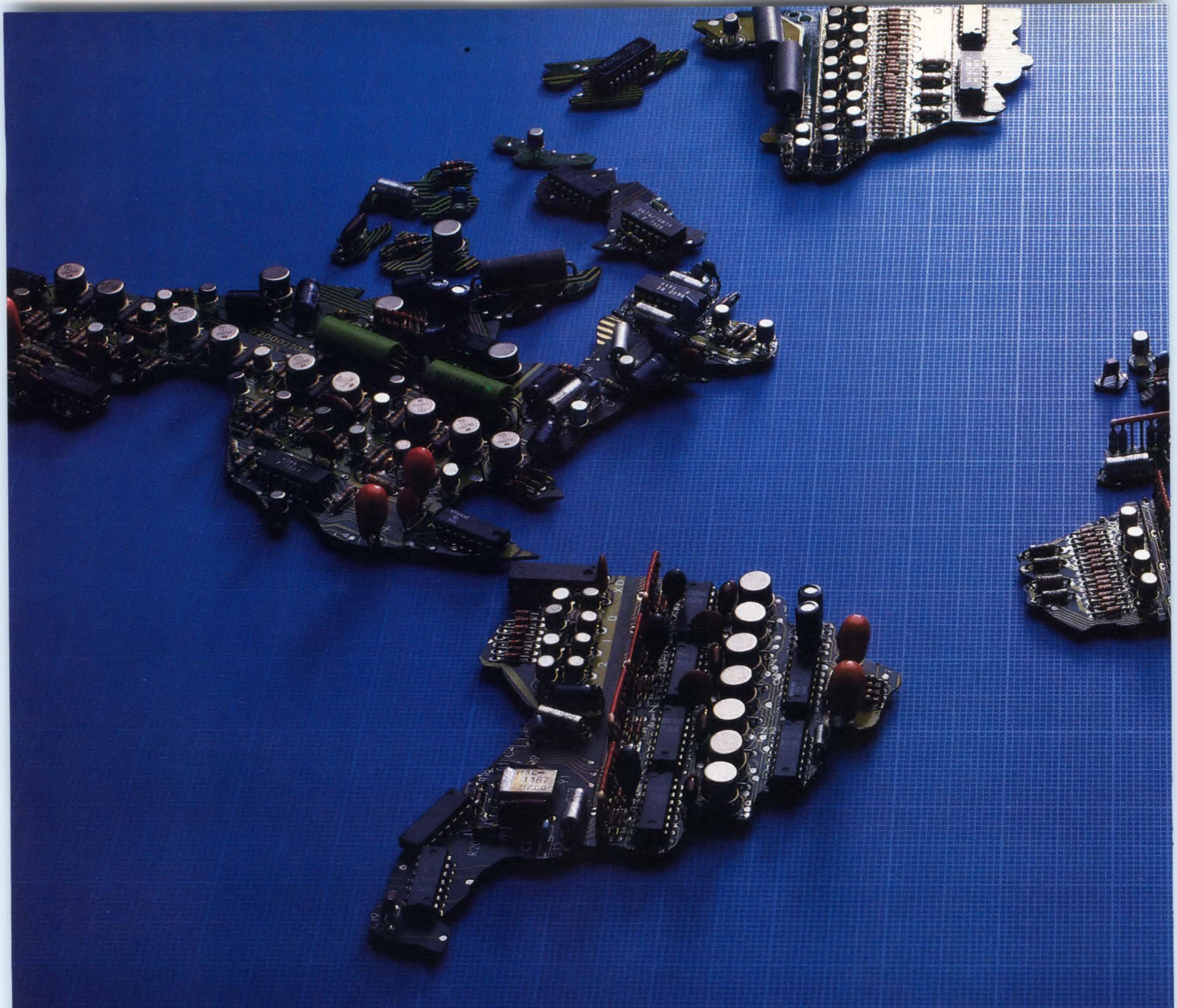
Specification summary: Unified-memory architecture in which application program ROM (EPROM), working registers, I/O registers, and some control registers all share common memory space of 64k bytes (except TI 70CTXX models). Low-end family members have an 8-bit timer with capture latch and 5-bit prescale; interrupt; 128 and 256 bytes of RAM; and 2k or 4k bytes of ROM. High-end 70C42 includes two 16-bit timers (one with capture latch), which are cascadable to 26 bits; a UART with an 8-bit timer for baud-rate generation (or usable as a third timer); programmable interrupts; 256 bytes of RAM; and 4k bytes of ROM. High-performance model operates to 6 MHz with basic microinstruction cycle taking 333 nsec. Most instructions take 5 to 9 cycles. Minimum instruction time is 1.25 μsec, which includes load, logic or arithmetic operations, and store. I/O to 32 pins with some models, including special functions such as UARTs and ADCs. NMOS and NMOS-EPROM devices require 5V supplies; CMOS operates over 2.5 to 6V V_{CC} and includes power-down modes. Available in 28-and 40-pin DIPs and 28- and 44-pin PLCCs.

HARDWARE — SUPPORT — SOFTWARE

From TI: XDS development system ($5900). It provides in-circuit emulation, target-system debug (with breakpoints and logic-state trace), and RS-232C link to host computer or terminal. EVM evaluation board ($795) provides in-circuit emulation, programs SE77C42 and EPROMs, and has serial interface to standard terminals. Piggyback devices accept 27C64 and 27C128 EPROMs. SE70CP160 CMOS piggyback device supports prototyping for 70C20, 70CT20, 70CT40, and 70C40 μCs. SE70CP162 CMOS piggybacking device and SE77C42 support prototyping for 70C42.

From TI: Cross-assembler and linker to run on MS-DOS-based PC that may serve as host for XDS. DEC VAX VMS assembler/linker support is also available.
From Cybernetic Micro Systems (San Gregorio, CA): Assembler, simulator, and debugger to run on IBM PC.
From Allen Ashley (Pasadena, CA): Cross-assemblers and emulators to run on IBM PC.
Literature: TI 7000 family data manual with applications.

GENERAL DYNAMICS LAND SYSTEMS



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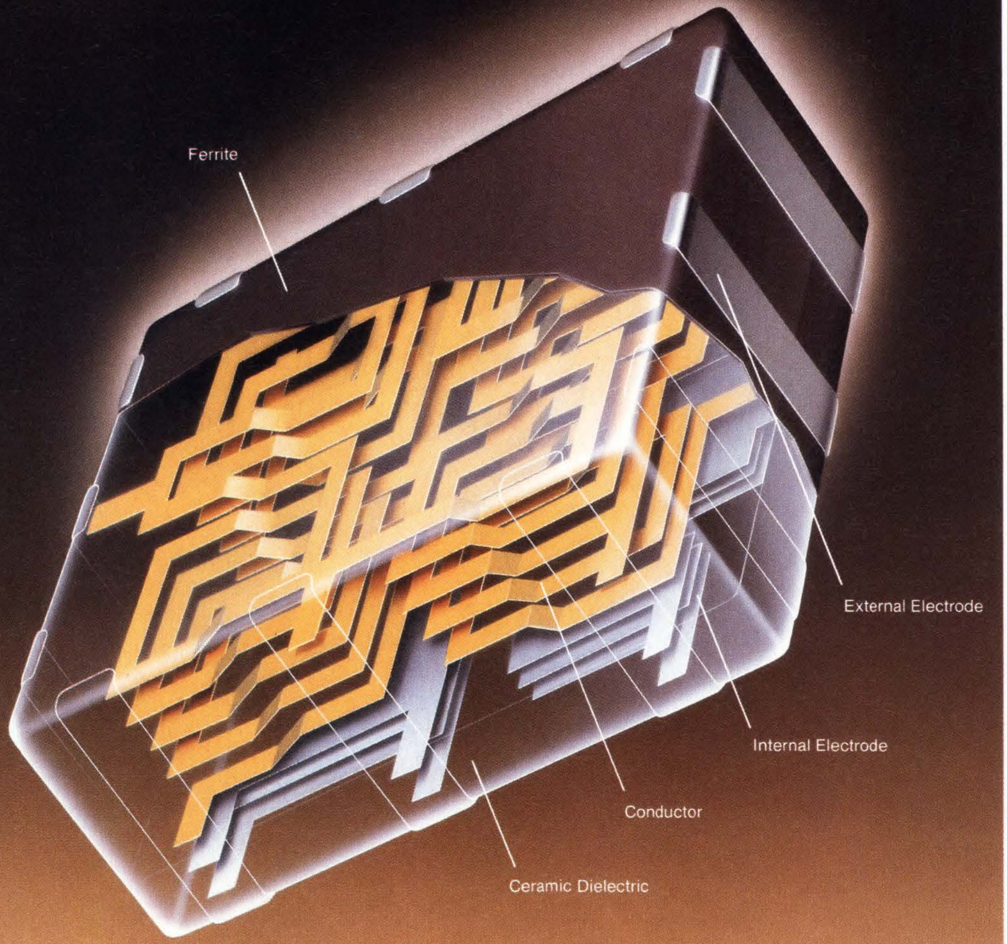

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Simplifying High Density Placement TDK Surface Mount Devices

Multilayer Ceramic Chip Capacitor
C1608 (CC0603) C: 0.5~22,000pF
C2012 (CC0805) C: 0.5~100,000pF
C3216 (CC1206) C: 0.5~220,000pF
C3225 (CC1210) C: 750~470,000pF
C4532 (CC1812) C: 2,400pF~1μF
C5650 (CC2220) C: 5,100pF~1.5μF

Multilayer Ceramic Chip Capacitor Network
MCN7575 TC: COH, 1~100pF SL, 10~1,000pF TC: −1,000, +350ppm/°C (12 capacitors) Class II, 100~470,000pF (12 capacitors)

Multilayer Ceramic Chip Capacitor (High Frequency, Low Loss)
FC1414 C: 0.5~3,300pF
FC2828 C: 0.5~22,000pF
FR1414 C: 0.5~3,300pF
FR2828 C: 0.5~22,000pF

Multilayer Chip Inductor
MLF2012 L: 0.047~33μH
MLF3216 L: 0.047~33μH
MLF3225 L: 39~220μH

Multilayer Chip LC Trap
MXT4532
MXT5050
F range: 700kHz~10MHz Tolerance: ±3%

Multilayer Chip IFT
MIA4532 F: 455kHz
MIF4532 F: 10.7MHz

Multilayer Chip Transformer
MTT4532 L: 10~200μH

Multilayer Chip LC Filter
MXF4532H HPF (TV)
MXF4532B BPF (FM radio)
MXF5050H HPF (VCR)
MXF5050B BPF (VCR)
MXF5050L LPF (VCR)
MXF5050D Delay Line (VCR)

Micro Chip Inductor (Wound Micro Chip Inductor)
ACL3225S
ACL3225R
L: 0.01~1,000μH

Leadless Inductor (Wound Chip Inductor)
NL322522 L: 0.01~220μH
NL453232 L: 1.0~1,000μH
NL565050 L: 1,200~10,000μH
NLF453232 L: 1.0~1,000μH (Shielded Inductor)

Power-Line Leadless Inductor (Wound Chip Inductor)
NLC322522 L: 1.0 (850)~330μH (60mA)
NLC453232 L: 1.0 (1,050)~220μH (120mA)
NLC565050 L: 1.0 (1,800)~1,000μH (85mA)

Leadless LC Trap (Wound Chip LC Trap)
NLT4532 F: 630kHz~13MHz Tolerance: ±2% Attenuation: 20dB min.

Leadless EMI Filter (Wound Chip EMI Filter)
NLL4532 C: 33pF~100,000pF L: 1μH~220μH

Ferrite Chip EMI Suppressor
CB201209 Zo: 7, 10, 11Ω
CB321611 Zo: 19, 26, 31Ω
CB322513 Zo: 31, 52, 60Ω
CB453215 Zo: 70, 120, 125Ω

NTC Chip Thermistor
NTC CS3216 R typical: 1.0~150kΩ at 25°C Temp. Range: −25 to +85°C

SM Pulse Transformer
CPT6 x 6 L: 10~100μH Winding ratio $N_1:N_2$; 1:1
CPT10 x 10 L: 100~1,000μH Winding ratio $N_1:N_2:N_3$; 1:1:1

SM Transformer/Inductor
EE5 **EE12** **ER9.5** **ER11/5** **ER14.5/6** **T2**

SM Step-up Inductor (Unimorph Piezoelectric Buzzer)
OL3.3 x 1.6
OL3.3 x 2.1

CIRCLE NO 152

8085AH/80C85 — 8-BIT NMOS AND CMOS

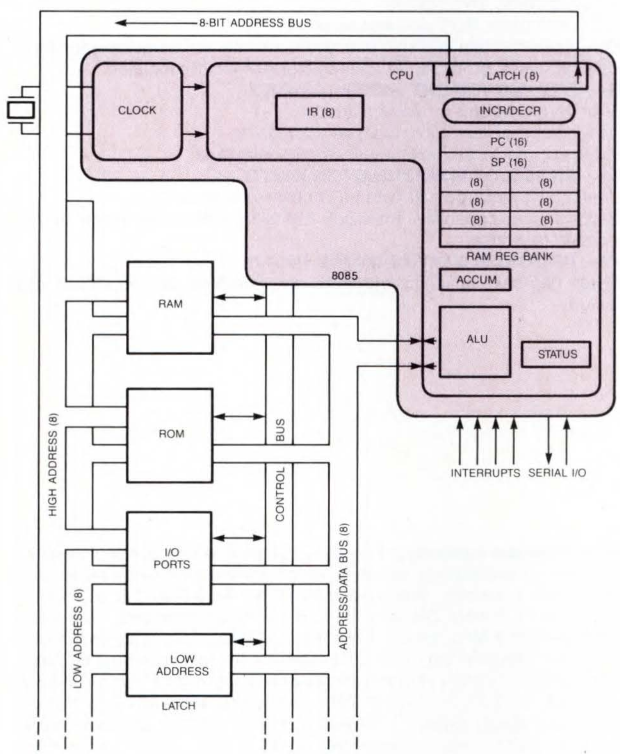
AVAILABILITY: Now for both in NMOS 8085 and for CMOS 80C85 versions.
COST: Prices for these older multisourced parts have dropped to $1 and below, with prices as low as $0.65 for volume purchases. CMOS parts, especially faster ones, are more expensive. Radiation-hardened CMOS parts are very expensive ($300 to $800).
SECOND SOURCE: 8085: NEC and Toshiba (and Intel) had most of market between them in '86, but Mitsubishi, Siemens, and AMD also shipped parts. 80C85: Oki active with Harris and Calmos supplying nuclear-radiation-hardened CMOS to military and aerospace customers.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Description: Based on the older 8080 µP, this family has proven a good general-purpose, midrange µP, though not the most efficient one for small programs. 8085 executes 8080 instructions, but with simpler hardware. Z80 (see elsewhere in this directory) is an enhanced 8080 but has different package pinouts and bus operation. New 8086 (see elsewhere in this directory) is vaguely software compatible, but 8-bit-bus 8088 version of 8086 can interface to 8080 and 8085 peripherals.

Status: The venerable 8080—the µP that gave legitimacy to the µP revolution—is obsolete. It had less than 0.28% of the 8-bit-µP market in '86, according to Dataquest. The 8085 is also starting to fall off, according to Dataquest figures. Still, it was in second place behind the Z80.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
BCD arithmetic
Double-precision operations (instructions string two data bytes together as 16-bit word)
II—DATA-MOVEMENT INSTRUCTIONS
Uses three pairs of so-called GP registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can perform multiple indexing with these, but takes additional steps compared with classical index-register concept. 8085 has two additional instructions—RIM and SIM—that interface with new serial-I/O pins (as well as interrupt system)
III—PROGRAM-MANIPULATION INSTR
Uses stack pointer (SP) to create LIFO stacks in external RAM for unlimited subroutine nesting
All GP registers can be incremented and decremented
Multiple-interrupt capability
Bus controls allow addition of DMA
IV—PROGRAM-STATUS-MANIP INSTR
Software access to status register

How 8085 differs from 8080:
8085 has on-chip clock, needs only a 5V supply, and has relaxed memory-access time. But because it multiplexes lower eight bits of address on data bus, it's not pin compatible with 8080. New pins gained by multiplexing implement address-latch strobe, four additional interrupts, and two serial-I/O lines. For small "few-chip" µP systems, a designer can use 8155/56 and 8355/8755 combo chips with built-in address latches.

Specification summary: Common instruction and data architecture (64k bytes) with optionally separate I/O space (256 addresses). Three 16-bit pointer registers allow efficient addressing of 64k-byte main-memory space. 78 basic instructions with 2-µsec typ register-to-accumulator addition execute time. 8085A has on-chip clock and needs only 5V. High-speed (5 MHz) and CMOS versions of the 8085A are available.

HARDWARE — SUPPORT — SOFTWARE

Most of the vendors of third-party µP development systems have included 8080/8085 development components as a routine part of their catalog. Typically, they use IBM PCs as host.

Most of the many companies that supply 8080/8085 development systems also supply the software. Also, many software houses have 8080/8085 software in every conceivable category.

Z80 — 8-BIT NMOS AND CMOS

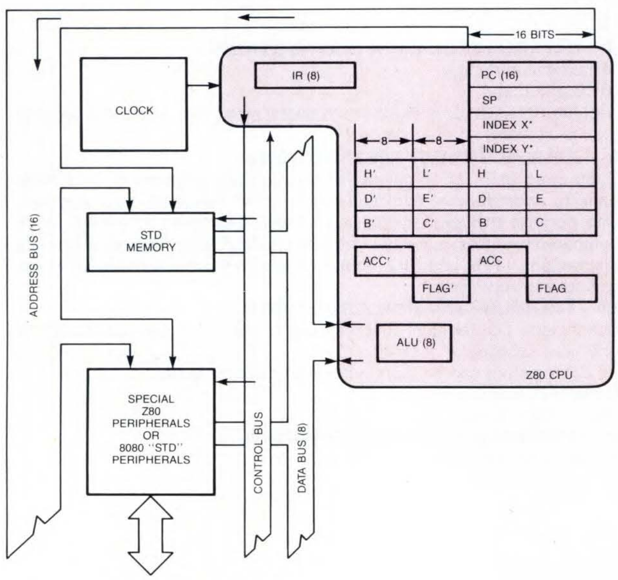
AVAILABILITY: Now for 6- and 8-MHz NMOS and CMOS versions.
COST: Because of the many aggressive second sources for this most-widely-used part, NMOS prices have dropped to $1 (6 MHz) and less (4 MHz); CMOS volume prices have dropped to $1.70 (6 MHz) and $1.30 (4 MHz), both in high volume.
SECOND SOURCE: Sharp, SGS, NEC, Toshiba, and Thomson-Mostek. Toshiba, Sharp, and SGS as well as Zilog have CMOS versions. Additional sources mentioned by Zilog are Gold Star, VLSI Technology, and Rohm.
CORE: Both Zilog and Hitachi are considering the Z80 μP as an ASIC core in their enhanced versions, the 64180 and the Z280.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

Description: Superset of widely used 8080/85; adds hardware and software features. Not pin-for-pin compatible with 8080 or 8085, but can use 8080 software and peripherals—though to do so would not take full advantage of Z80, and its peripherals and might require additional logic for interfacing.

Status: By far the most successful 8-bit μP. The Z80 is still being used in new designs but may be superseded by the new enhanced versions. Of these, the Hitachi 64180 seems to be the most popular, but the Zilog Z280 represents the greatest Z80 enhancement. Whatever happens, one thing is certain: The Z80's momentum will probably last for the rest of this century, especially in ASIC core form.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Support chips include peripheral interface (PIO), timer (CTC), serial communications (SIO), and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. Several enhancements of Z80 exist or are imminent. All are in CMOS. The first is the Hitachi 64180, to which many Z80 designers are converting. The second is the supplier's Z280, which boosts the Z80 into minicomputer performance. In addition, the NEC 78XX single-chip device is similar. Most are covered elsewhere in this directory.

I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logicals
16-bit arithmetic BCD add and subtract
Nine types of rotate and shift directly on any register or memory location
Can set, reset, or test bit in any register or memory location
II—DATA-MOVEMENT INSTRUCTIONS
8- or 16-bit register or memory loads
Two index registers allow indexed addressing
Extensive memory-block move/search commands
III—PROGRAM-MANIPULATION INSTR
Uses 16-bit stack pointer with LIFO stack with RAM
Relative-jump capability. Interrupt capability with three types of selectable response
IV—PROGRAM-STATUS-MANIP INSTR
Seven flag bits, including arithmetic and overflow, can be stored and tested

Specification summary: Upwardly compatible with 8080A software, but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 0.5 to 1.8 μsec (1.5 μsec avg) for 8-MHz Z80 and 1.0 to 5.5 μsec (2 μsec avg) for 4-MHz Z80A. 6- and 8-MHz versions are also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires single-phase clock and one 5V supply at 60 mA for Z80; 90 mA for Z80A. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. MIL-temperature parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 μA when in power-down (clock-stopped) mode. Housed in 40-pin DIP. CMOS versions available also in flat pack and PLCC.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: "Z-Scan" emulator boxes that can be used alone or with host computers. Z-Scan-80 that will provide emulation for the Z80H ($6695).
From SGS: UX-8/22 development system based on CP/M and two 8-in. floppy disks. Package for full-speed in-circuit emulation.
From others: Some of the many third parties that supply Z80 hardware support are Applied Micro, Boston Systems, Emulogic, Hewlett-Packard, Huntsville Microsystems, Nicolet, Orion, Sophia Systems, Tektronix, and Zax. Contact Zilog for addresses.

From Zilog: Software for the various development systems. Macroassembler with relocatable assembler, linking loader, file-maintenance programs, and resident Basic, Cobol, C, Fortran, and PLZ (Zilog-created language that comes in "lower" level that mixes assembly-and system-language statements with a "higher" C language). Z80 has cross-software package (assembler, etc) that runs on DEC VAX or Zilog S8000 under Unix.
From SGS: Software package for UX-8/22, including debugger, disassembler, and tracer.
From others: A lot of software of all sorts, including the popular CP/M operating system (Digital Research) and the MS/X operating system (from Microsoft), which is popular in Japan. Contact Zilog for names and addresses of several dozen others.

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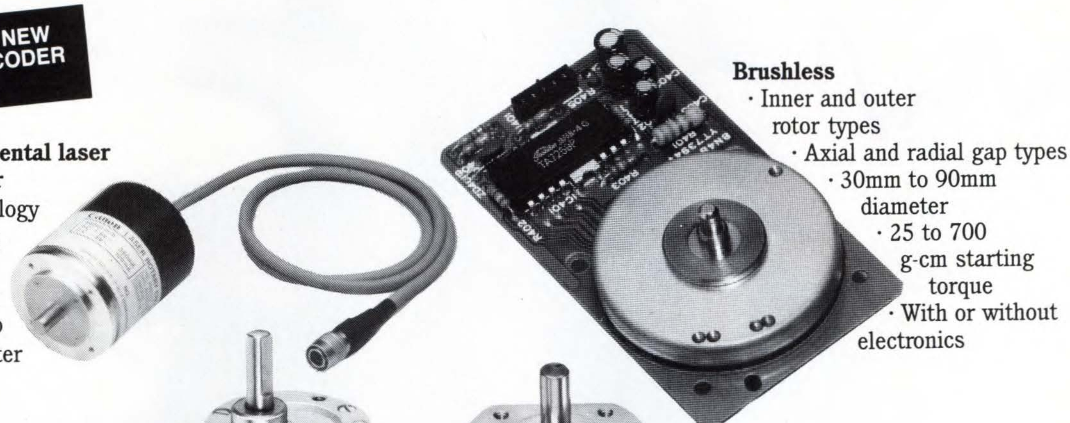

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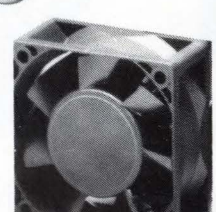

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HD 64180, Z180 — 8-BIT CMOS

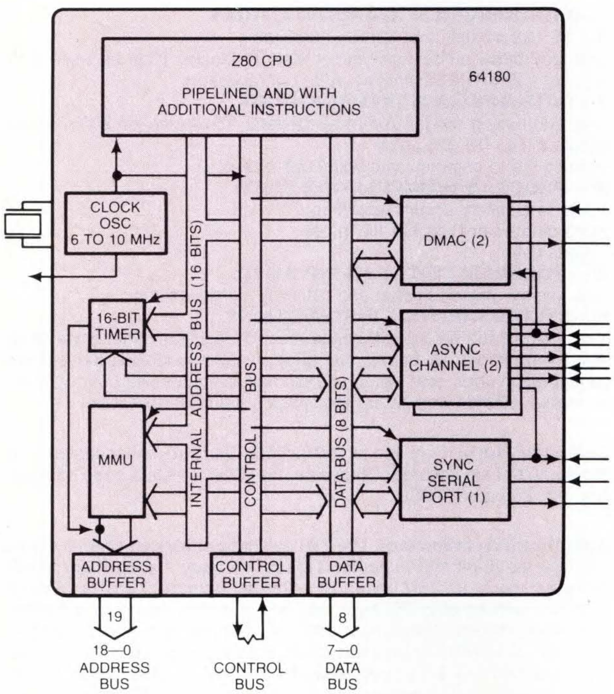
AVAILABILITY: Now for 6-, 8-, and 10-MHz parts.
COST: For 10-MHz parts, $20 (100) and $18 (1000).
SECOND SOURCE: Zilog.
CORE: Hitachi considers basic 64180 a standard cell for building high-integration µPs and µCs.

Hitachi America Ltd
Semiconductor and IC Div
2210 O'Toole Ave
San Jose, CA 95131
Phone (408) 435-8300

Description: Enhancement of Z80 with various peripheral functions such as memory management (to reach larger, 1M-byte, memory space), 2 DMA channels, 2 serial ports, timers, etc, added on CMOS CPU chip. R-suffix versions will have "total" compatibility with Z80-family peripheral chips. Hitachi 647180 with on-chip EPROM represents first 1-chip Z80 µC.

Status: Another CMOS enhancement of the widely used Z80. This one has on-chip MMU, multiple DMA channels, and UART like the Zilog Z280, but it's not as ambitious. It doesn't have sophisticated big-computer features such as separate privileged "system" control registers nor does it have a cache. Moreover, the 64180's MMU is not for virtual and protected memory; it translates between the Z80 64k address space and the 1M-byte space reached externally by the 64180. It has received a boost from all the Z80 users and third-party supporters of the venerable Z80. Hitachi predicts a buildup to 10 million units by '89.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. Diagram is for basic 64180 core. Hitachi plans to expand upon this core.
2. The 647180 is 1-chip version of 64180 in which 16k bytes of EPROM and 512 bytes of RAM have been added along with another 16-bit timer, 6-channel analog comparator, and 54 I/O pins. It comes in windowless plastic 84-pin PLCC and 80-pin flat pack. Because of EPROM, Hitachi bills this style µC as a Zero Turn Around Time (ZTAT) part, saying it is cost effective up to 5k volume.

I—DATA-MANIPULATION INSTRUCTIONS
Unsigned $8\times 8=16$ multiply
Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator
II—DATA-MOVEMENT INSTRUCTIONS
Immediately addressed locations
Block output to I/O. (Must set up MMU bank registers to translate between 64k of Z80 and 512k external)
V—POWER-SAVING INSTRUCTIONS
Sleep command disconnects processor from clock. (Interrupt or reset will reconnect)

Software Notes:
1. Only new instructions beyond Z80 instructions listed.
2. The MMU adds base registers to Z80 16-bit addresses to produce the 19-bit addresses needed externally.
3. Trap interrupt can be used both for catching undefined op codes and for allowing users to extend instruction set.

Specification summary: Object-code compatible with Z80 (and 8080, 8085). Pipelined CPU. On-chip MMU generates 19 bits (512k to 1M bytes) external physical address space. 2-channel DMAC (direct-memory-access controller), 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (R-suffixed versions are matched to Z80-family peripherals). CMOS 50 mW at 4 MHz with lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

ASE Adaptive System Emulator ($7000) plus H6805M01S, a 256k-byte memory board for use with IBM PC, HP6400, or DEC VAX as host. Real-time operation up to 8 MHz and real-time tracer buffer for 2048 machine cycles. All hardware lines are captured, and the trace is automatically disassembled.
American Automation AA 572-64180 real-time in-circuit emulator for use with company's E2-PRO development host.
Hewlett-Packard and Tektronix offer support on their development systems and logic analyzers.
Contact suppliers for the many other third parties.

Microtec Research (Santa Clara, CA) is supplying macroassembler, utilities, Pascal, and C compilers (to run on IBM PC and DEC VAX hosts). Also, Avocet (Rockport, ME) and Allen Ashley (Pasedena, CA) have announced IBM PC-based assemblers. Hitachi provides help so that the additional 64180 instructions can be treated as macros on a Z80 macroassembler. Boston Systems Office (Waltham, MA) has VAX-hosted assembler ($3900). Software compatible with CP/M (Digital Research) and MSX (Microsoft) operating systems (latter being result of project for Japanese market).
American Automation has cross-software to go with development hardware (assembler, C compiler, and debugger).
Archimedes (San Francisco, CA) has C compiler ($995 for IBM PC; $3995 for MicroVAX; and $5995 for VAX).

Z280

8/16-BIT CMOS

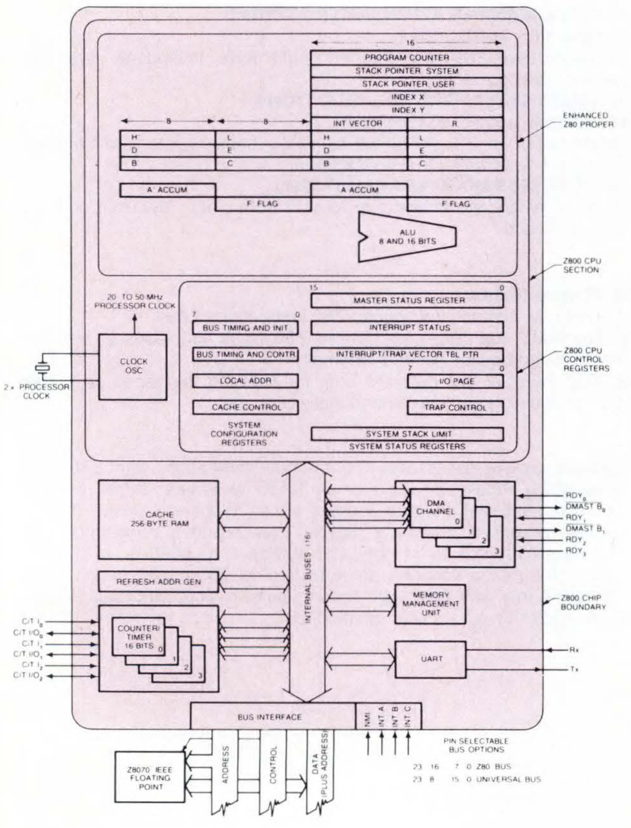
AVAILABILITY: Now.
COST: About $15 in large volumes.
SECOND SOURCE: None announced, but supplier says it has strong interest from major European and Far East semiconductor houses.
CORE: Zilog is incorporating elements of Z280 in its megacell library so it can rapidly put together new combinations. However, it does not plan to offer ASIC tools to customers.

Description: Enhanced Z80 μP, upgraded to the point that it has most of the features of larger 16/32-bit machines. It has "privileged" system-control hardware and associated software for multiuser, multitasking operating systems. It has memory management for virtual memory and incorporates cache to achieve high throughput with moderate-speed external memories.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

Status: The Z280 became available in late '87. Basically, the Z280 lets designers upgrade Z80-based personal computers into multiuser systems that have large virtual memories and, claims Zilog, high performance. Zilog says it is finding a great deal of interest, especially in Europe and Japan, where Z80-based personal computers have persisted. Compared with other Z80 enhancements, such as the Hitachi 64180 (which Zilog second sources), the Z280 offers a greater performance edge. Zilog is also pushing the Z280 as upgrade for the many dedicated systems using Z80s as embedded controllers.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. Zilog says the integration not only lowers system cost but provides a speed advantage: When all subsystems are on chip, the system speed automatically increases.

I—DATA-MANIPULATION INSTRUCTIONS
16×16=32 multiply and 32/16=16 divide
Extended block mode manipulates data in blocks. (Can be used with supplier's Z8070 IEEE floating point coprocessor)
II—DATA-MOVEMENT INSTRUCTIONS
New addressing modes for more general 16-bit use of Z80's 16-bit registers (HL, DE, BC pairs)
Instructions to communicate with coprocessors
III—PROGRAM-MANIPULATION INSTR
Jump on auxiliary accumulator/flag
Jump on auxiliary register file in use
System call
IV—PROGRAM-STATUS-MANIP INSTR
New master status register; see category V instructions
V—SYSTEM CONTROL INSTRUCTIONS
New instructions for added system-control registers. These are privileged instructions to permit operating system to define the system configuration upon start-up, to use the new system stack pointer, master status register, and set up the cache's mode of operation

Software Note: Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).

Specification summary: The Z80 upwardly enhanced toward a general-register 16-bit minicomputer. On-chip memory management to address as much as 16M bytes of external memory. CPU is 3-stage pipelined with on-chip 256-byte program and data cache to automatically keep recently used instruction on chip for fast—to 2 MIPS—execution at 10-MHz internal bus clock. Planned mask shrink from initial 2-μm geometry to 1.5 μm is expected to allow 25-MHz clock. Future mask improvements are expected to allow speeds to 50 MHz. The I/O is pin programmable to match either 8-bit Z80 bus or 16-bit "universal" bus. Also included on chip are four 16-bit timer/counters, four DMA channel controllers, dynamic memory refresh control, and a serial UART port. The Z280 will be fabricated in static CMOS and housed in 68-pin PCC package; other options planned for future as requested by customers.

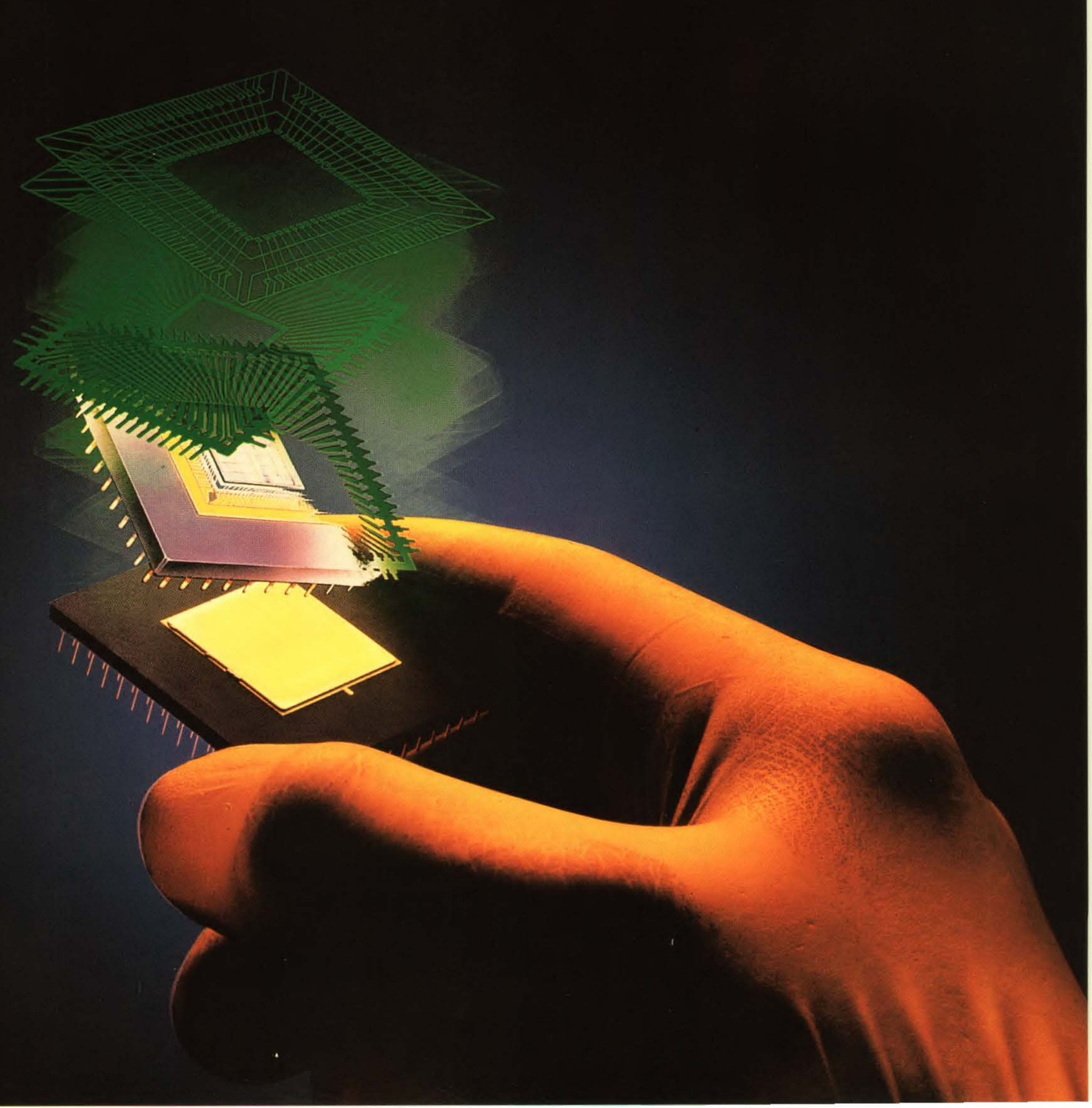
HARDWARE — SUPPORT — SOFTWARE

From Zilog: ICE chip (1st qtr '89) and evaluation board.
From others: Softaid (Columbia, MD) has a low-cost real-time development system, and CDS (Statesville, NC) offers evaluation boards for several popular buses. Also logic analyzers are sold by Hewlett-Packard and Tektronix.

From Zilog: You can obtain a debug monitor program and a cross-assembler with Zilog's evaluation board. Zilog plans no other software support.
From others: 2500 AD is shipping a cross-assembler and is reported to be working on a C compiler. CDS offers both a cross-assembler and a C complier.

TEXAS INSTRUMENTS REPORTS ON GRAPHICS

IN THE ERA OF MegaChip TECHNOLOGIES



Graphics in the Era of MegaChip Technologies:

Why do industry leaders graphics processors from

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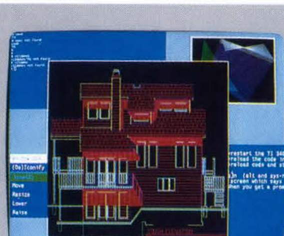

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Stretching across the bottom of these pages is but a fraction of the hundreds of systems based on TI's industry-standard TMS340 graphics family. At the left is a Sun-3 utilizing TI's leadership '74ACT8800 building-block processor family. Which only goes to prove designers choose TI graphics products for everything from workstations to PCs, from laser printers to arcade games.

They get design options that allow them to differentiate their products and to better tailor price and performance to their markets.

They also move to market faster with less risk. TI graphics products are proven, available, fully supported—the standard by which others are measured.

Let a few of the designers tell you about their choices:

"The TMS34010 was the only graphics processor that could meet the performance requirements of our laser plotter controller."

—*Al Sabel, Advanced Products Manager, Xerox Corporation*

The Xerox 8836 had to produce D- and E-sized drawings with a resolution of 400 dots per inch at a constant speed of one inch per second. The 34010 delivered: Six million instructions per second with a "draw" rate of up to 50 million pixels per second.

"The programmability and architecture of the TMS34010 provide the performance and flexibility we need for color- and graphics-intensive printer products."

—*Dr. Donald Parker, Exec. V.P. Products & Technology, QMS, Inc.*

Because the 34010 is programmable, QMS was able to build a printer that their customers could program to accept scanned color input and to provide high-speed color output as well as hard copy with multiple printer support.

"TI's ACT8800 technology allows our TAAC-1 application accelerator to significantly boost the computing power of a Sun workstation for imaging and graphics applications."

—*Nick England, Director Application Accelerator Group, Sun Microsystems, Graphics Products Division*

"The 8800's power lets us combine the functionality of an image processor, an interactive graphics device, and an array processor in a single product and still offer user programmability."

There's more in store from the ACT8800 family. The recently disclosed 8847 floating-point processor combines two 64-bit functions on a single chip: A floating-point multiplier and a floating-point arithmetic logic unit. Its number-crunching capability: 33 MFLOPS.

"In designing graphics systems, you can't forget about tomorrow. And TI hasn't."

—*Carl Calabria, Director of Engineering, Truevision® Inc.*

"The 34010 enables our True Vista® video graphics boards to bring workstation performance to IBM® compatibles and Mac IIs. It is the only graphics chip that will allow us to migrate our applications software to even higher-performance second-generation TMS340-based systems." *See road map on next page.*

The TMS340 second-generation processor is three to 20 times faster than the 34010. It is user configurable, software and plug-in compatible.

Two other products designed in parallel with the new TMS340 processor are the One-Megabit Video RAM and the industry-first floating-point graphics processor, with on-board, high-level graphics instructions.

The One-Megabit VRAM enhances the performance of the 34010. And when used in tandem with the second-generation processor, performance is improved up to 50 times over other processor/VRAM combinations.

The floating-point graphics processor executes up to 40 MFLOPS and interfaces directly with the address and data buses of the second-generation TMS340, allowing it to perform computation-intensive functions more than 10 times faster than current PCs.

For details on TI's software and third-party support, turn the page.

RasterOps

Renaissance GRX

Truevision

Vermont Microsystems

Vectrix

6800/6802 AND 6809/6309 — 8-BIT NMOS AND CMOS

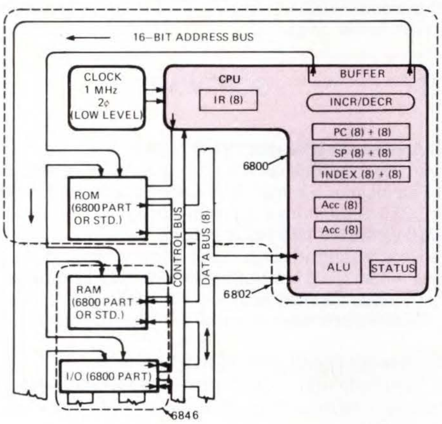
AVAILABILITY: Now.
COST: As with other mature µPs, costs have dropped (to a few dollars per µP), except when a part is at end of its life, in which case prices might rise again.
SECOND SOURCE: Hitachi, Fujitsu, and Thomson Semiconducteurs.

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

Description: The 8-bit 6800 CPU was the original part in the family named after it. That family has been broadened to include not only the 2-chip 6802/6846 and 6809 covered here but also the 1-chip 6801, the low-end 1-chip devices, and the 6804 and the 6805. Note, though, that new CPU members of family aren't precisely compatible with the original 6800, especially at the low and high ends. Even the 6809 here is only software compatible with the original 6800 at source-code level.

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest µP families of all. Among its progeny must be included the 6809 covered here and the following Motorola µPs and µCs, which are described elsewhere in this directory: the 6804, 6805, 6801, and 68HC11. The 6800 itself is now past its prime and is not recommended for new designs; we retain it in the directory for reference. But the newer 6802 and 6809 continue to be shipped in volume. For new designs, Motorola steers designers either upwards to 16- and 32-bit 68000 family (68008 has 8-bit bus) or downwards to the 68HC11.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram shows 6800 and 6802. The 6809 has another 16-bit index and a second "user" stack pointer, which make the 6809 more powerful than the 6800; these additional resources give the 6809 many more instructions. On simple benchmarks, the 6809 is 270% faster than the equivalent-speed 6800, programs in 42% fewer instructions, and uses 33% less code.
2. Basic 6809 version has on-chip clock. A minimum system results with the following parts: 6809, 6810, and 6846. 6809E version has off-chip clock. An early valid-memory-address (VMA) signal on 6809E allows 3-MHz bus operation with a 2-MHz memory. External clock permits multiprocessing.
3. The memory-management unit (6829) allows the 6809 to run 32 concurrent protected tasks (per management unit) in 2M-byte address space.
4. Hitachi CMOS version (6309) has 2-, 2.5-, and 3-MHz bus timing, and the Sync and CWAI instructions allow a low-power sleep mode.

PART	DESCRIPTION	CLOCK SPEED (MHz)	ROM ×(8)	RAM ×(8)	AVAIL	COST (100 QTY)
6800	CPU NEEDS 2 φ CLOCK	1-2	—	—	NOW	$4-$5
6802	CPU, CLOCK & RAM	1-2 (4 MHz EXT)	—	128	NOW	$4-$5
6809	CPU	2	—	—	NOW	$5-$6
6309	CPU CMOS	3	—	—	NOW	$9.50

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic
Instructions to take advantage of two accumulators
6809 has unsigned 8×8 multiply with 16-bit product
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions
6809 can use four index registers for merging three source blocks into one destination block
Can autoincrement and autodecrement by one or two directly and indirectly. (Page zero can be software relocated during program execution, effectively increasing its size)
Indexing uses the "true indexing" relationship between base and offset (0, 5, 8, 16 bits) rather than the 6800 relationship
Can utilize the user stack for Polish-notation operations or interpretive languages
III—PROGRAM-MANIPULATION INSTR
Has PDP-11-type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM
Does not have vectored interrupt, but can achieve function with software (or with 6828 priority interrupt controller)
6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs
IV—PROGRAM-STATUS-MANIP INSTR
6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register, or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction
V—POWER-SAVING INSTRUCTIONS
6309 has SYNC and CWAI to put CMOS CPU in sleep mode. Sync instruction stops µP until it gets go-ahead signal from interrupt line

Specification summary for 6800: Common-memory architecture with 16-bit (64k-byte) memory space for instructions, data, and I/O; all data 8 bits wide. Instruction set patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 µsec. NMOS circuitry requires one 5V supply, 500 mW; housed in 40-pin DIP. Versions with −55 to +125°C range also available.
Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upwardly compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing increases throughput. Instruction set has 59 mnemonics and seven addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-inherent operations executing in 1 µsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page-zero register is retained but can be software relocated anywhere in memory via programmable register. The chip requires one 5V supply. Two versions, each in 40-pin DIP.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: Emulators range from low-cost (hundreds of dollars) boards to HDS-300 system (about $5000) plus personality modules ($5000).
Support systems and OEM boards available from Motorola Semiconductor Div, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-6900 or (602) 438-3500.
From others: Tektronix and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola "Micromodule" 8-bit boards.

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733. The basic assemblers and other tools are for IBM PC.
Two versions of Basic are available for the 6809: Basic-M and Basic09. The latter is designed to be fast and to permit structured programming.
A Pascal compiler diskette is available.

650X, 65C0X

8-BIT NMOS AND CMOS

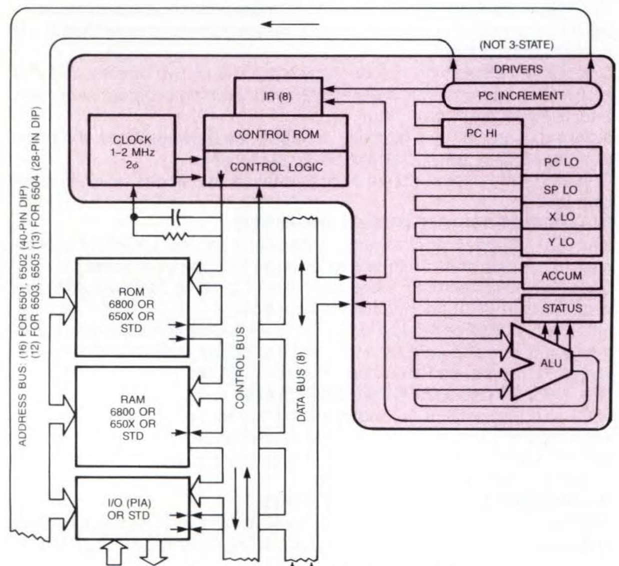
AVAILABILITY: Now.
COST: The prices for both NMOS and CMOS were said to have dropped to less than $1. However, "legitimate" US price said to be $2 to $3 for NMOS and twice that for CMOS.
SECOND SOURCE: Rockwell, California Micro Devices, NCR, and WDC (Western Design Center). WDC created some of the CMOS designs, which it has licensed (UMC in Taiwan, ITT-Intermetall in West Germany, etc), which is one explanation why second sources have proliferated.
CORE: WDC claims to have developed the semicustom 6502 core as NCR and others now use it. Many suppliers now specify it as part of their cell libraries.

Description: Original design team's goal was to achieve as much PDP-11-style addressing capability as would fit in an economical chip. Because of the μP's short 8-bit index registers, it is optimally suited only to applications requiring access of smaller blocks of memory (although it benchmarks ahead of most other 8-bit μPs with respect to its speed of execution of high-level languages such as Basic and Pascal). New CMOS parts also have small economical die that gets still smaller with today's finer geometries. See 6500/1 for 1-chip versions and 65SC816/802 for 16-bit-internal version.

Originator Commodore (Westchester, PA) no longer sells chips to the merchant market. Contact second sources.

Status: The falling share of market for this μP appears to indicate that it has reached the end of its lifecycle. However, the architecture lives on in the form of 1-chip versions (see 6500/1 and especially the 50740) and ASIC versions. Some of these have very large unit volumes, so the 6502 architecture may remain, by volume, the leading 8-bit architecture in the world. WDC is shipping 8-MHz parts and claims to be developing even faster chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes on CMOS versions:
1. CMOS 65CXX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are new 4-phase clock that gives decreased memory access time and a memory-lock (ML) output and bus-enable (BE) input that simplify multiprocessor designs.
3. Among the software enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
4. Decimal mode is automatically set Off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
5. A BRK followed by interrupt is executed.
6. See instruction set for comments on new instructions.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM or I/O ports). CMOS parts have bit manipulation
II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset limited to 8 bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables. CMOS parts have indexed absolute indirect and zero-page indirect
III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model. CMOS parts have branches on bit test
Stack pointer for implementing 256-byte LIFO in external RAM
IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits. (6502 and 6512 have external input to one status bit, useful for handshaking with peripherals)
V—POWER-SAVING INSTRUCTIONS
WAIT and STOP on 65C02 respectively stop processor and disconnect clock to lower power consumption

Specification summary: Common-memory architecture with instructions, data, and I/O in same 64k-byte space; 57 instructions (68 for CMOS). Many instructions provide choice of 13 PDP-11-type addressing modes (15 for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mV supply. Some CMOS parts can run at 8-MHz clock (125 nsec/cycle). CMOS parts require 4 mA/MHz for operation and 10 μW for standby.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: LCE low-cost emulator ($1250) that will optionally interface to IBM PC host.
From Western Design Center: Toolbox Design System in-circuit emulator (ICE) runs with an Apple IIGS host and can communicate with an IBM PC via a serial link ($4995).
From California Micro Devices: GEM-I in-circuit emulator package ($3750) capable of interfacing with a variety of host computers including ISIS development system and Apple. Functions as a stand-alone assembler and disassembler using a nonintelligent terminal. Evaluation board for 65SC150 ($499) that functions as in-circuit system when coupled with GEM-I.
From NCR: Hardware emulator interfaces to Apple IIe through RS-232C. Allows complete in-circuit software debug.
From Dynatem (Irvine, CA): AIM-65 single-board computer and RM industrial modules.

From Rockwell: Cross software for Intel ISIS-II and personal development system ($250). Support (in firmware) for assembly ($35), monitor ($65), Basic ($65), PL/65 ($85), Forth ($65), Pascal-"instant" ($100), math package ($35), and disk operating system ($50).
From California Micro Devices: 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).
From NCR: Monitor for use in conjunction with emulator. Supports breakpoint, change memory and registers, software trace and real-time execution, etc.
From others: Because the 6500 has been so widely used, there are innumerable sources of software at different language levels; for example, Byte Works (Albuquerque, NM); S-C Software (Dallas, TX); Roger-Wagner Publishing (El Cajon, CA); and 2500 AD (Aurora, CO).

65C816/65C802

8/16-BIT CMOS

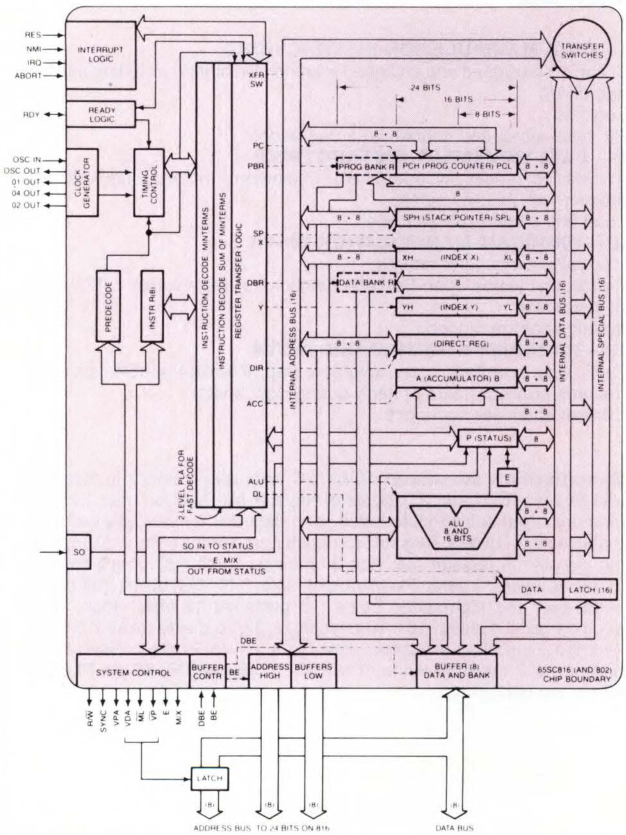
AVAILABILITY: Now for 2-, 4-, 6-, and 8-MHz parts.
COST: In 100 qty, plastic, $20 for 816 and 802.
SECOND SOURCE: VLSI and California Micro Devices said to be main sources, but WDC says it has licensed others in US and abroad. (Mitsubishi says it will be doing a version of its 50740 6502-based 1-chip device that will also have a 16-bit internal architecture.)
CORE: All suppliers are considering this as μP megacell in their libraries, but WDC has most commitment to its ASIC use.

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545

Description: CMOS 8/16-bit μPs featuring software compatibility with 8-bit 6502 (both original NMOS 6502 and enhanced CMOS 65C02). The 802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The 816 has a different pinout but expands the addressing range of the 6502 from 64k to 16M bytes. Additional hardware enhancements on the 816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

Status: Apple's use of the 65C816 in the IIGS upgrade of the widely used Apple computer provides a firm basis for hardware and software availability. Software support is growing as third-party houses that have supported the 6502-based Apple computers convert software to take advantage of the expanded memory and other capabilities of the 65C816. One indication of breadth of software support is Byte Works claim that it has delivered several hundred of its software-development tools.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. Compare diagram with previous 6502/65SC02 (elsewhere in directory) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits and the 16-bit registers widened to 24 bits.
2. The new control-bus outputs on the 816 facilitate multiprocessing, caching, and virtual memory.
3. The new control-bus inputs on the 816 allow you to abort instructions for virtual memory and to control bus access.
4. Apple is said to have had to resort to special semicustom chips to allow the Apple IIGS to operate efficiently and at full system-level speed.

I—DATA-MANIPULATION INSTRUCTIONS
The 6502/65C02 instructions with 16-bit versions of add, subtract, BCD, and logicals. No multiply, but future 65C832 version will have provisions for floating point on chip
II—DATA-MOVEMENT INSTRUCTIONS
6502/65C02 instructions, but with choice of 8- or 16-bit indexing and 8- or 16-bit data widths
On 816, addressing can span 16M bytes with aid of paging through new register extensions. New block-move (forward or backward) instructions. Increased stack-pointer addressing modes, including stack relative, indirect, and indexed
III—PROGRAM-MANIPULATION INSTR
Wait for interrupt, stop clock (restart via interrupt). (Abort instruction on 816 via pin input acts like interrupt and directs program to perform memory repair and retry)
IV—PROGRAM-STATUS-MANIP INSTR
Additional bits in status register allow software selection of 8- or 16-bit modes for indexing and data. Also, new E bit associated with status register (but not handled as part of it) provides software choice of emulation or native mode

Software Notes:
1. Upon reset, 802 and 816 are in 6502 emulation mode. To go to native (enhanced) mode, the E bit must be reset to 0 via an exchange with previously reset carry bit in status register.
2. Full-sized 16-bit registers reported to facilitate high-level-language compiler writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Tendency of new native (enhanced) mode coding to become trickier than 6502, because of tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

Specification summary: Enhanced 6502 with 16-bit internal data option and 24-bit addressing option, software selectable. Data I/O off chip remains 8 bits, however. The 802 version is hardware compatible with 6502 (or 65SC02) and can be plug-in replacement. It will reset into 6502 emulation mode but can be software switched into varying degrees of 16-bit operation. The 816 version is almost identical internally to 802, but it has different pinouts because it brings the additional bits for 24-bit address space out of the multiplexed 8-bit data bus, and it has special control lines to facilitate virtual memory, coprocessors, and data and program caching. Performance is mostly identical to 6502 of same clock speed, except that extended addressing and data modes take additional cycles. Clock to 8 MHz. Fabricated in 2.4-μm and 1.5-μm CMOS and specs 5-mA/MHz power consumption with 1 μA standby.

HARDWARE — SUPPORT — SOFTWARE

From Western Design Center: The Toolbox Design System in-circuit emulator (ICE) runs with an Apple IIGS host and can communicate with an IBM PC over a serial link ($4995).
From California Micro Devices: Prototyping board for 816.
From Microtek Lab Inc (Gardena, CA): In-circuit emulation.
From Dynatem (Irvine, CA): RME-1600 board with 65C816.
From Apple (Cupertino, CA): The Apple IIGS personal computer ($700 to $1300) for use as development platform because it uses 65C816.

From Byte Works (Albuquerque, NM): The ORCA/M cross-assembly and utility package. C and Pascal compilers are also available.
From Apple (Cupertino, CA): Assember and debugger ($100) and C compiler.
From others: Supporting products are also available from S-C Software (Dallas, TX); Roger-Wagner Publishing (El Cajon, CA); and 2500 AD (Aurora, CO).

8096 FAMILY

16-BIT NMOS AND CMOS

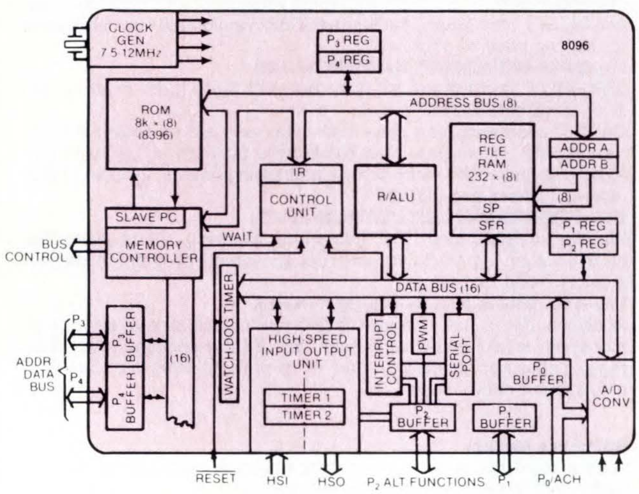
AVAILABILITY: NMOS 8096 family is in production. The 8098 chip offers an 8-bit external bus. The EPROM version is also available. The higher-performance CMOS version 80C196 is now in production.
COST: Less than $8 in 10k qty.
SECOND SOURCE: Signetics/Philips.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Description: Highly integrated 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes 8k bytes of ROM and 232 bytes of register-file RAM. I/O capabilities include an 8-channel, 10-bit ADC, full-duplex UART, 8-level priority interrupt, pulse-width-modulated output, high-speed pulsed I/O, four 16-bit software timers, five 8-bit I/O ports, and a watchdog timer.

Status: This earliest of the 16-bit microcontrollers continues to have a large share of 16-bit market. However, because that market is still young, it's too early to tell whether this will be another case of Intel dominance. The only other 16-bit μC shown with any volume was the Thomson-Mostek 68200, but following the Thomson-SGS merger it has dropped out of the picture. Meanwhile, the National 16040 and NEC 783XX (78312), which are newer designs, are being aggressively marketed and could pose threats. Actually, with the advent of the ASIC approach, the definition of this market is blurring; for now, any μP that is in core form in an ASIC library could have memory added and become a "μC," even Intel's own 80188/80186s.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. The initial NMOS 8096 family consists of parts that come with or without A/D converters (and S/H circuits) and onboard ROM, and with either 48 I/O lines (68-pin package) or 32 I/O lines (48-pin package). They have option of either 8- or 16-bit system bus. The 8098 offers an external 8-bit bus. The 8k-byte EPROM version has onboard programming capability and read/write selectivity.
2. New CMOS version 80C196 has 2× NMOS performance.
3. Four high-speed trigger inputs record times at which external events occur. Storage in 8-deep FIFO.
4. Six high-speed pulse outputs can trigger external events at preset times. Commands are stored in 8-deep content-addressable memory. Output section can concurrently run as many as four software timers simultaneously.
5. 16-bit watchdog timer allows recovery from hardware or software error.

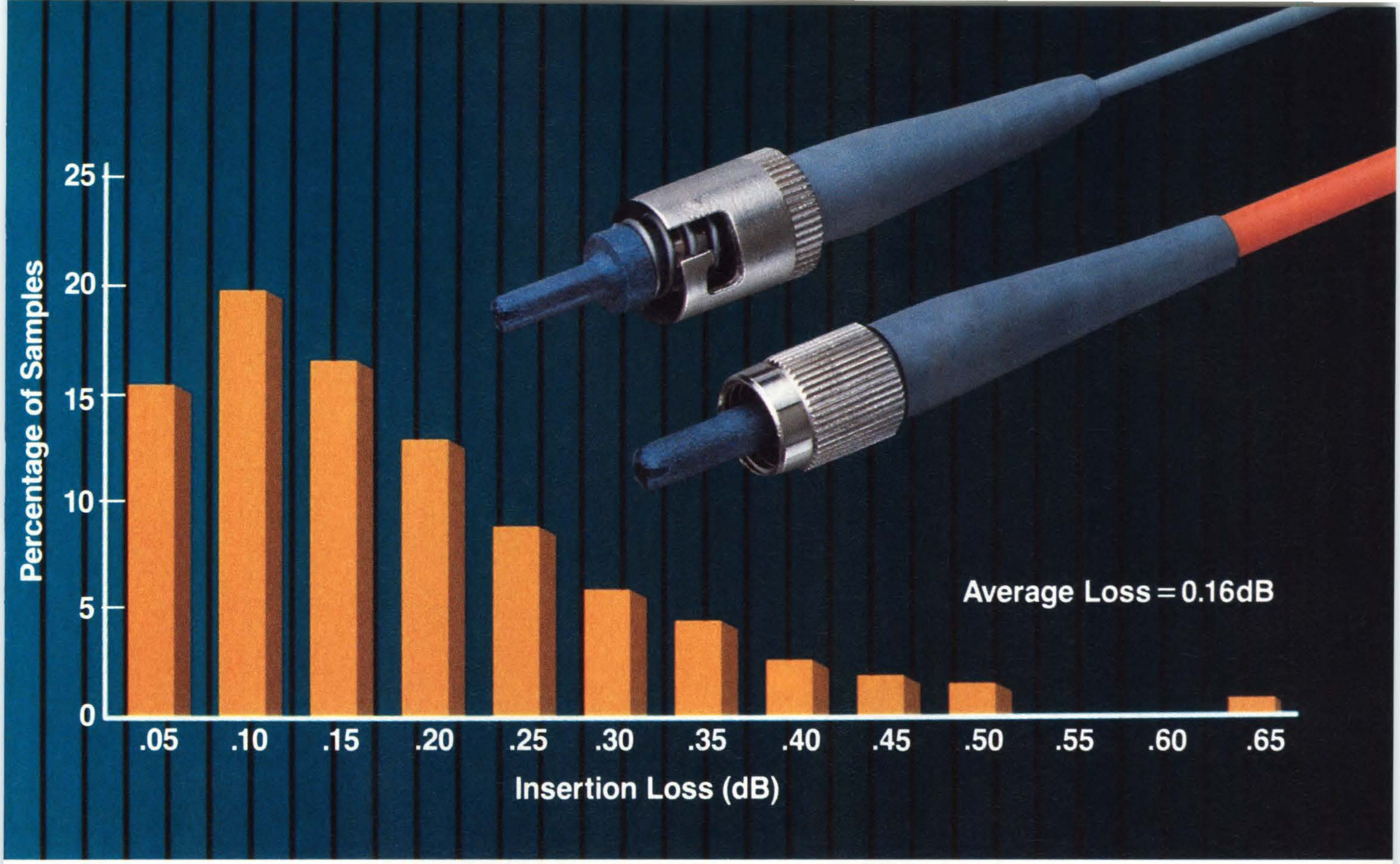
I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide
Logicals
Bit, byte, word, and double-word operations
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include Direct, Immediate, Indirect, Indexed, and Indirect with Autoincrement
Load and store, push and pop
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction
Iteration control of loops
IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, sticky bit (records previous value of carry during right shifts)
Can set and clear some bits

Specification summary: 16-bit μC with split-memory architecture and 8k-byte ROM and 232 bytes of register-file RAM on chip. External memory expandable to 64k bytes, with data bus dynamically programmable as 8 or 16 bits. Register-to register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter, four 16-bit software timers, PWM output, five 8-bit I/O ports, full-duplex serial port and high-speed pulse I/O ports. At 12-MHz clock, 16-bit addition takes 1 μsec, 16×16 multiply or 32/16 divide takes 6.5 μsec. Average instruction-execution time equals 1 to 2 μsec. New CMOS parts have 2× performance of NMOS. In 48-pin DIP, 68-pin PLCC or 68-pin pin-grid array.

HARDWARE — SUPPORT — SOFTWARE

From Intel: Low-cost development kit ($2695) includes iSBE-96 emulator board and ASM-96 macroassembler and runs on IBM PC host as well as Intellec Series III and IV. Real-time emulation to 12 MHz. VLSICE-96 advanced emulator provides real-time emulation up to 12 MHz and is hosted on IBM PC as well as Intellec Series III and IV. Intel also offers support hardware for the 80C196 chip.
Programming support for EPROM versions supplied through Intel's line of universal PROM programmers as well as third-party programmers from companies such as Data I/O.

From Intel: Macroassembler (ASM-96), PL/M-96 and C-96 compilers. PL/M and C supply hardware-control features such as interrupts. Each software package includes relocation/linkage utility (RL-96), library management utility (LIB-96), object-to-hex conversion utility (OH-96), and FPAL-96, a 32-bit floating-point utility. Software packages run on an IBM PC and compatible computers. $750 for a single-user license.
From Archimedes (San Francisco, CA): ANSI C-8096 compiler with additional features like control of interrupt. Hosted on IBM PC ($995), MicroVAX ($3995), and VAX ($5995).
From Cybernetic Micro Systems (San Gregorio, CA): Graphic programming and simulation aids that run on IBM PC ($295 and $995).



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Both the SMA and ST types are highly suitable for manual or automated polishing and are adaptable on all styles of optical fiber cables. The SMA type is compatible with the 905 connector design, while the ST type features a spring-loaded bayonet lock.

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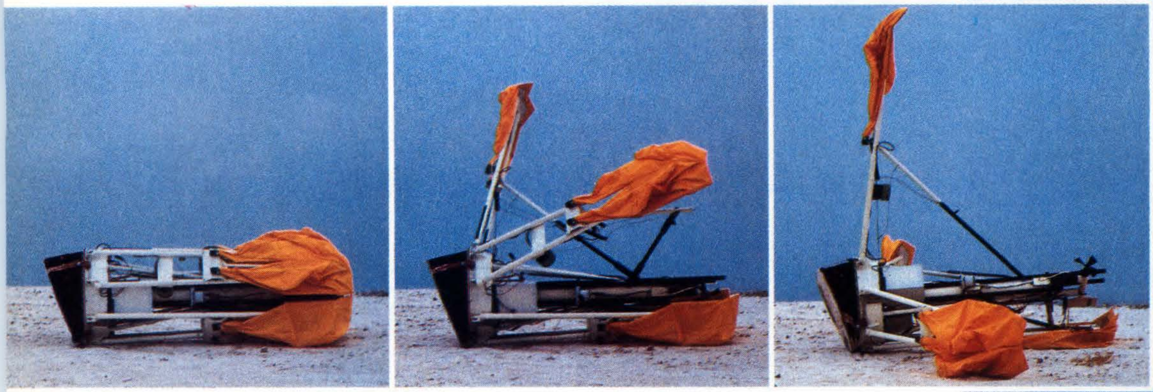

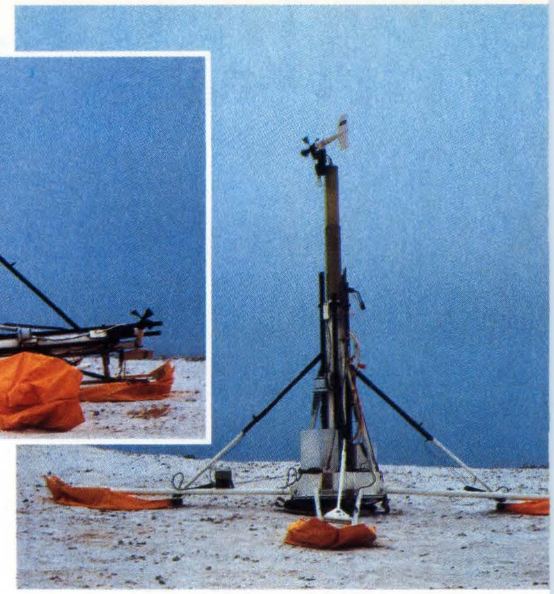

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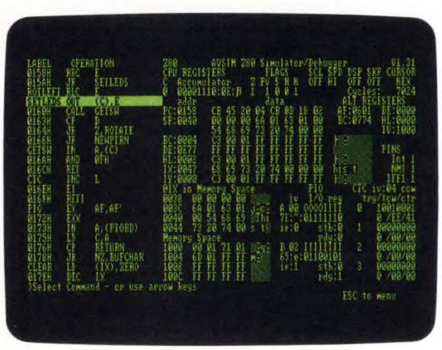
This "Self-Erecting Weather Station," sponsored by the National Science Foundation and designed and developed by Polar Research Lab, was made possible by Avocet and AVSIM™, Avocet's unparalleled simulator/debugger.



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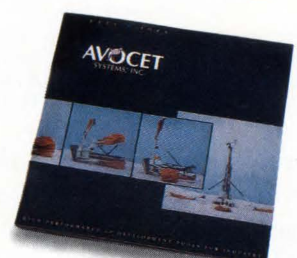

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CIRCLE NO 156

HPC 16000

16-BIT CMOS

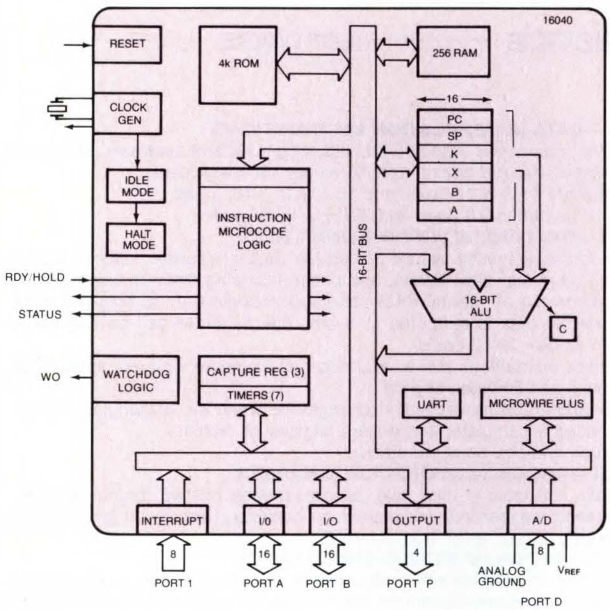
AVAILABILITY: Now for 17- and 30-MHz parts.
COST: Less than $10 in volume.
SECOND SOURCE: None.
CORE: Standard cell is in supplier's ASIC library.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

Description: 16-bit CMOS microcontroller family with basic version having 8k bytes of onboard ROM, 256 bytes of RAM, extensive I/O, and onboard peripherals. Original 16040 had 16.8-MHz clock with 240-nsec register instruction execution. Due to shrinking, new 16083 samples achieve 30-MHz clock rates, with shortest instructions just 134 nsec, over −55 to +125°C. Supplier says HPC stands for "high-performance microcontroller."

Status: Supplier says HPC 16040 and 16083 are first members of what is to be a family of industrial controllers. Supplier's benchmarks (August '86 with HPC at 17 MHz) indicate that HPCs outperform other similar 8- and 16-bit controllers such as Intel 8051 and 8096, Motorola 68HC11, and TI 7000 on both throughput and ROM-program efficiency. NEC 78XX and 78XXX and Zilog Super Z8 weren't mentioned. This family is from the same group at National that has produced National's most successful µP/µC, the 4-bit COPS.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Family is designed around common µP core for instruction-set consistency, with various models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are ADCs, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPROMs. Also planned are HDLC, CRT, DMA, SCSI, and Ethernet controllers.
2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (ADCs, display drivers, EEPROM), COPS 4-bit µCs, 8050 8-bit µCs, and other HPCs for multiprocessing.
3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity such as infinite loops.
4. Halt and idle modes provide additional power savings by stopping clock or disconnecting it.
5. Emulator parts are available for the 16000 family.
6. µPI (Universal Peripheral Interface) port for connecting to µPs such as National's 32000 family.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results
Logical AND, OR, XOR, and compares
Bit manipulation of all registers and through all 64k address space
II—DATA-MOVEMENT INSTRUCTIONS
10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip
Instructions include load, store, push, pop, and exchange
III—PROGRAM-MANIPULATION INSTR
Calls, jumps, returns, and conditional jumps implementing high-level-type constructs
IV—PROGRAM-STATUS-MANIP INSTR
There is a carry bit and several status registers. These may be manipulated as all bits in register space, and in 64k address space may be set, reset, and tested

Specification summary: 16-bit CMOS µC and µP with memory-mapped architecture and 8k-byte ROM and 256-byte RAM on chip. External memory expandable to 64k bytes. 16-bit-wide architecture includes data bus, ALU, and registers. Has eight programmable 16-bit timers, eight vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, four input capture registers, 52 general-purpose I/O lines. Performance of 16083 at 16.8-MHz clock is 240 nsec for register operations and 7 µsec for 16×16 multiply and 32/16 divide. Performance of 16083 at 30 MHz is 134 nsec. Supplier says its "microCMOS" process will provide 47-mA power consumption. Idle instruction will reduce this to 1 mA, and halt instruction will drop it to 200 µA. Supply range is 4 to 5.5V. Available in industrial (−40 to +85°C) and extended (−55 to +125°C) temperature ranges (MIL-STD-883 now). In 68-pin PCC, LCC, and 68-pin PGA, and 84-pin TapePak.

PART NUMBER	MEMORY ROM (BYTES)	MEMORY RAM (DIGITS)	I/O PINS	INTERRUPT	STACK	TIMER BASE COUNTER	SIZE (PINS)	OTHER
HPC16003	ROM-LESS	256	52	8 SOURCES	IN RAM	8	68	4 INPUT CAPTURE REGISTERS
HPC16083	8.0k	256	52	8 SOURCES	IN RAM	8	68	4 INPUT CAPTURE REGISTERS
HPC16164*	16k	512	52	8 SOURCES	IN RAM	8	68	4 INPUT CAPTURE REGISTERS & 8-CHANNEL A/D
HPC16400	N/A	256	52	8 SOURCES	IN RAM	4	68	2-CHANNEL HDLC & 4-CHANNEL DMA
HPC16900	N/A	256	52				68	PORT EXPANSION AND RECREATION LOGIC
HPC16104	NONE	512	52	8 SOURCES	IN RAM	8	68	4 INPUT CAPTURE REGISTERS & A/D
HPC16064	16k	512	52	8 SOURCES	IN RAM	8	68	4 INPUT CAPTURE REGISTERS
HPC16004	NONE	512	52	8 SOURCES	IN RAM	8	68	4 INPUT CAPTURE REGISTERS

*AVAILABLE 1Q '89

HARDWARE — SUPPORT — SOFTWARE

A designer's kit is available for under $500. Supplier's Mole (microcomputer on-line emulator) is a low-cost ($4590) development system for the HPC family. Mole consists of brain board and HPC personality board and optional software. The brain board is common to all National µCs. The personality boards tailor the system to emulate particular µCs. Moles can be used in conjunction with various hosts like IBM PC/XT/ATs or VAXs (Unix/VMS).

Cross-assembler and C compiler to run on IBM PC. VAX (Unix/VMS) support is available, as is a symbolic debugger. Floating-point math and general math packages are currently available.
Dial-A-Helper is a 24-hr on-line computer bulletin board serviced by National. It provides latest information on all National µC chips (including development systems) and also specific application support. Phone (408) 739-1162.

783XX

16/8-BIT CMOS

AVAILABILITY: Now for ROMless, masked ROM, and EPROM versions of 78312 (See also Note 3).
COST: 10k qty, $12.50; expected to go under $10.
SECOND SOURCE: None.
CORE: As with many of the 1-chip sets, supplier has been using cell-library concepts in house all along.

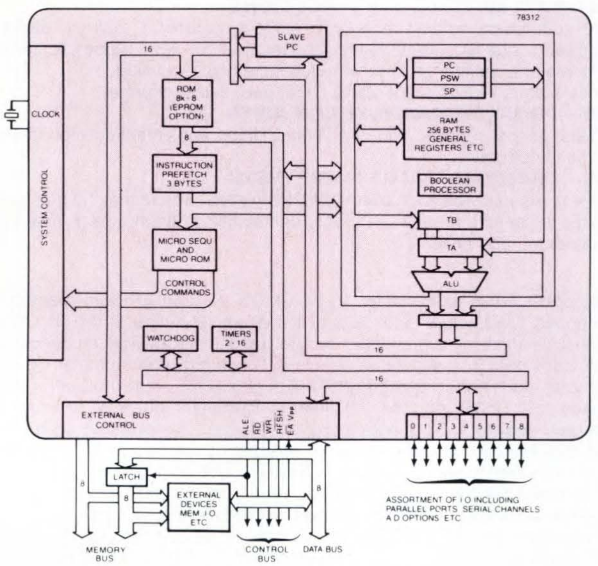
NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics USA Inc
1 Natick Executive Park
Natick, MA 01760
Phone (508) 655-8833

Description: Intended for high-end controller-type applications, 783XX combines a fairly fast, powerful, 16-bit ALU with many peripheral functions on single chip. Although there's some architectural resemblance to supplier's existing 7811 (see Note 3) and new V Series (especially V25), this is said to be an original design with its own unique instruction set.

Status: Supplier says 78312 is the first in a new family that is expected to bridge the gap between 8-bit 1-chip controllers and 16-bit minicomputer-like chips. Emphasis is on economic high-speed processing of real-time events. Competes with Intel 8096, National 16040, etc. Supplier says future chips in family will have same core architecture, but peripherals on chip will be aimed at specific applications (ie, the "ASIC" approach). One application is auto engine control. Another is an intelligent typewriter (said to have 1M-byte address space).

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. On-chip RAM contains eight banks of general-purpose registers and also eight "macroservice channels" that can perform DMA in response to interrupts.
2. Eight peripheral blocks at bottom of diagram are for the following functions: two 4-bit real-time output ports, external interrupts, serial communication, two 16-bit up/down counters, two 16-bit capture registers, two PWM outputs, an 8-bit 4-channel ADC, two 16-bit timers, and six 8-bit ports.
3. The 783XX's "parent" family, the 78XX, is still going very strong. The 7811 (4k-byte ROM) is the most popular member of that family and is now available in CMOS (78C11). Also in CMOS is 16k-byte-ROM 78C14. Prices range from $5 to $8 in 25k qty.

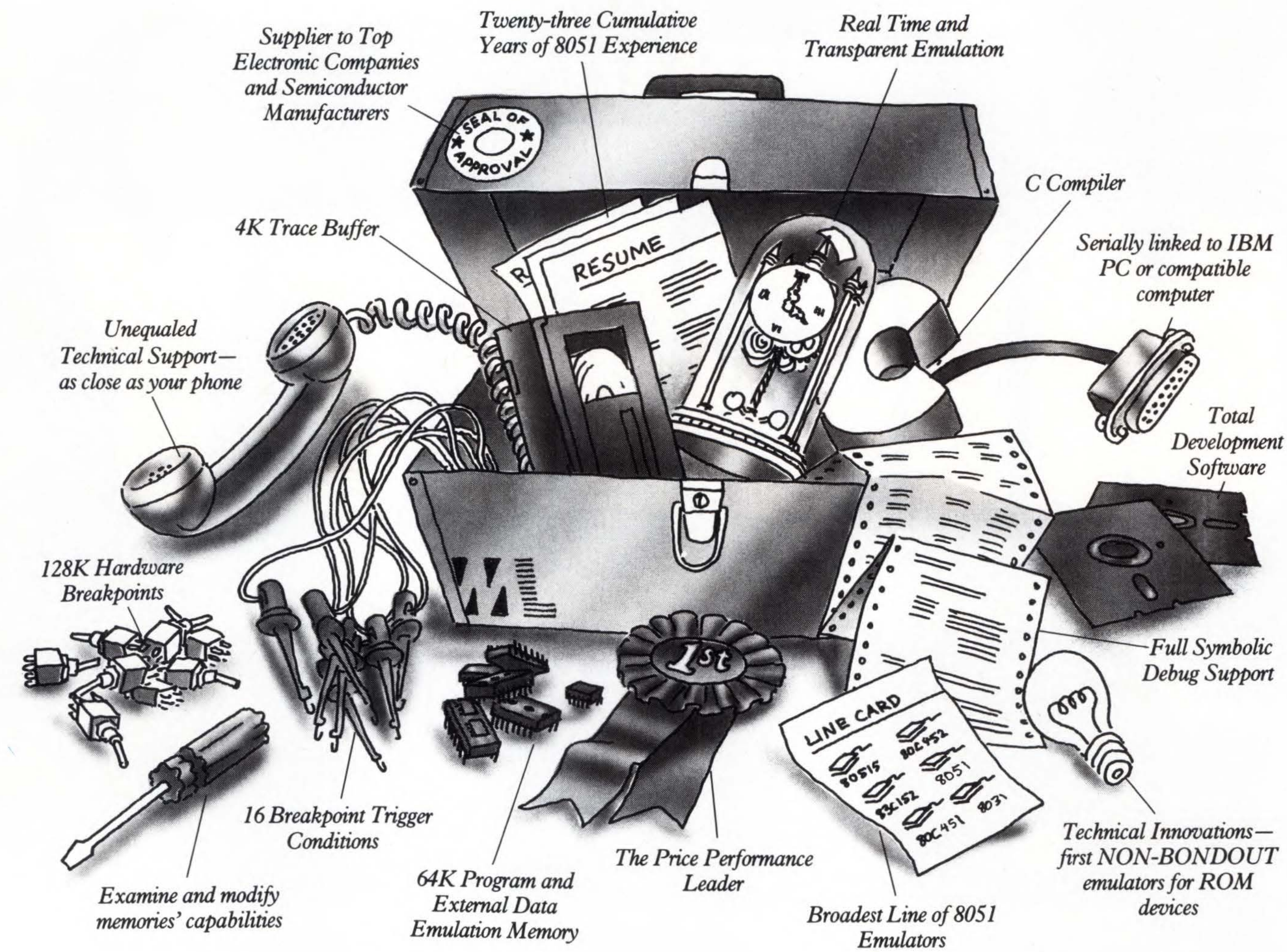
I—DATA-MANIPULATION INSTRUCTIONS
Most operations 8 and 16 bit, including adds and subtracts, shifts and rotates, decimal adjust, and increment and decrement
Multiply 8×8 in 3.0 μsec and 16×16 in 3.167 μsec
Divide 16/8 in 3.0 μsec and 32/16 in 8.333 μsec
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include immediate, register-register, indirect (including base and base-index), and direct (including direct-indexed). Direct addressing of internal RAM can accommodate 8 or 16 bits. (Although external data is restricted to 8 bits, internal RAM can be addressed on an 8-or 16-bit basis)
Block instructions move, exchange, or compare with accumulator as much as 256 bytes of data
8- and 16-bit moves and exchanges between the accumulator or extended accumulator and general register or memory
Push and pop on or off stack
III—PROGRAM-MANIPULATION INSTR
Call, call table (1-byte call), branch, branch relative, branch register, branch register indirect, branch on condition, branch on bit, software break, return, return from interrupt
IV—PROGRAM-STATUS-MANIP INSTR
Enable and disable interrupts, break with context switch, select register bank, increment/decrement stack pointer. Software control of standby modes, watchdog timer, and on-chip peripherals

Specification summary: A new high-performance, single-chip architecture that features eight switchable register banks to handle demands of real-time control. This CMOS processor uses IEEE standard mnemonics. The 12-MHz (max frequency) oscillator is divided by 2 to create a 167-nsec system clock. Min instruction time is 500 nsec. A 3-byte instruction prefetch queue further speeds processing. Chip can access 64k bytes of memory, including 8k bytes of on-chip ROM, 256 bytes of on-chip RAM, and a 256-byte special-function register area that communicates with on- and off-chip peripherals. On-chip peripherals include a 4-channel 8-bit A/D converter, a full-duplex UART, and an extensive timer/counter system. There are two 16-bit up/down counters, two 16-bit timers, two PWM outputs, a 16-bit timebase counter, and a free-running counter with two 16-bit capture registers. The 48 I/O lines include two 4-bit, real-time output ports. There are four external interrupt lines and 11 internal interrupt sources. Eight macroservice channels can perform DMA in response to various interrupt sources. The CMOS device is housed in 64-pin flat pack, shrink DIP, and PLCC.

HARDWARE — SUPPORT — SOFTWARE

From NEC: Supported on the NEC MD-086 CP/M-86-based development system. An emulation board, the IE-78310-R, hooks up to IBM PC and other popular computers. Evaluation package consisting of board with monitor, relocatable assembler, and software examples ($150).
From Orion (Redwood City, CA): Emulator.

From NEC: Software to run on MD-086 and other CP/M-based systems, includes relocatable assembler. Now also runs on IBM PC under MS-DOS.
From third parties: C compiler from Lattice. Forth interpreter under development.



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V SERIES

16- AND 32-BIT CMOS

AVAILABILITY: Now. (V70: sample quantities.)
COST: In 100 qty, \$6 for V20, \$8 for V30, \$17 for V40, \$13 for V50, and \$375 for V60 (16 MHz). The V70 costs \$500 (50).
SECOND SOURCE: None.

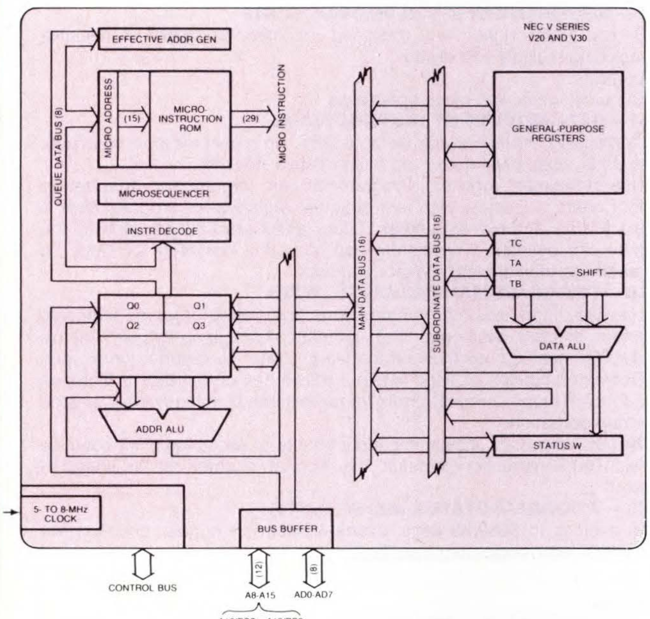
NEC Electronics Inc
(Corporate Headquarters)
401 Ellis St
Mountain View, CA 94039
Phone (415) 960-6000

NEC Electronics USA Inc
1 Natick Executive Park
Natick, MA 01760
Phone (508) 655-8833

Description: Parts with numbers to 50 are enhanced versions of Intel 8086 family. They obtain increased performance via such enhancements as dual internal 16-bit data buses, dedicated hardware for address generation, loop counters for block transfers, 16/32-bit temporary register/shifters for fast multiplication and division, and a prefetch register. Some parts can even do 8-bit 8080 instructions in an emulation mode. The 32-bit V60 and V70 share internal architectures but offer different external bus widths. The V60 and V70 support multitasking operations.

Status: The first members of this family represent a strategy used by several major Japanese suppliers of basing a µP family on an established instruction set, in this case the popular 8086, and then enhancing the core software and adding features to hardware to produce parts that outflank original parts. Unfortunately for NEC, Intel has sued, claiming that NEC copied Intel 8086-family microcode in violation of US copyright law. This has slowed acceptance of these parts. The lawsuit has yet to be settled.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram show V20 and V30, which have enhanced 8088/8086 architectures.
2. New V60 and V70 are 32-bit microprocessors. Three of them can run same code redundantly with majority-vote scheme for systems that demand fault tolerance.

Specification summary: 16-bit CPU with dual-bus internal architecture and dedicated addressing hardware can reach 1M-byte memory locations. Multiplication and division take 6 to 8 µsec at 5-MHz clock rate. Data-block transfer rate to 625k bytes/sec at 5-MHz clock rate. Devices dissipate 500 mW max at 5 MHz, 50 mW in standby, and operate over −40 to +85°C. Housed in 40-pin DIP, which is pin-for-pin compatible with 8088 (V20) and 8086 (V30). The V25, V40, and V50 chips are available in 68-pin PGA, 68-pin PLCC, and 80-pin mini flatpack. The V60 and V70 offer a different 32-bit architecture, one with a more general-register orientation. The V60 at 16 MHz performs 3 MIPS max, 1½ MIPS sustained; 20-MHz V70 performs 5½ MIPS max, 2½ sustained. See table for synopsis of family features.

I—DATA-MANIPULATION INSTRUCTIONS
Added instructions for multiply, shift, and rotate registers by immediate value; add, subtract, and compare packed decimal strings. Also included are a large number of variations on bit manipulation, like insert or extract bit; rotate left or right on one BCD digit; test, invert, clear, or set specified bit

II—DATA-MOVEMENT INSTRUCTIONS
Various memory-addressing modes are derived from four segment registers, pointers, and index registers. In addition to MOV instructions for transferring data between CPU registers and memory, there are instructions for moving a string of data between memory and I/O port

III—PROGRAM-MANIPULATION INSTR
In addition to call, jump, and return instructions, stack operations such as push immediate data or 8 general registers onto stack, pop 8 general registers from stack; allocate/free an area for a stack frame on a procedure; and enter/exit. Also includes an instruction to check array index against designated boundary and an instruction for floating-point-processor call procedure

IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8086-type status and control flags, an extra mode flag for indication of 8080 emulation mode or a native mode

Notes:
1. V20 and V30 instruction sets are supersets of 8088/8086 sets and can execute MS-DOS-type programs.
2. 101 instructions, some of which are designed to support high-level languages like Pascal.
3. 16-MHz V60 is available in a PGA. 16- and 20-MHz versions of the V70 will be available in PGAs also.

PART NUMBERS (CORRESPOND-ING INTEL 8086 FAMILY PART)		µP SPEED (MHz)	EXTERNAL ADDR BUS	EXTERNAL DATA BUS	ON-CHIP MEMORY ROM	ON-CHIP MEMORY RAM	ON-CHIP PERIPHERALS	PACK-AGE PINS
V20	70108 (8088)	5	20 (1M)	8	0	0	NONE	40 DIP
V25	70320 (80188)	5	20 (1M)	8	0	256	2-CHAN DMA INTER CONT 2×UART 2×16 C/T	80 FLAT 84 LCC
	70322				16k			
V30	70116 (8086)	5	20 (1M)	16	0	0	NONE	40 DIP
V40	70208 (80188)	8	20 (1M)	8	0	0	4-CHAN DMA INTER CONT 3×16 C/T UART CLOCK GEN	68 PGA 68 80 FLAT
V50	70216 (80186)	8	20 (1M)	16	0	0		
V60	70616 (NONE)	16	24 (16M)	16	0	0	FLOAT PT MMU, CACHE	PGA
V70	70632 (NONE)	16	32 (4G)	32	0	0	FLOAT PT MMU, CACHE	PGA

HARDWARE — SUPPORT — SOFTWARE

From NEC: The V60-based MV-9000 board plugs into an IBM PC. The board runs Unix System V and in particular, NEC's V60/V70 software-development tools. NEC also supplies a V60-based Multibus board.
Third-party hardware available from Zax and Sophia Systems.

From NEC: C compiler, assembler, link editor, etc, based on Unix tools (available for VAX Unix 4.3 or for MV-9000 board). Unix System V and V60 ITRON operating system.
Third-party software from Intermetrics (Cambridge, MA) and Digital Research (Monterey, CA).

8086/8088, 80186/80188 — 8/16-BIT NMOS AND CMOS

AVAILABILITY: Now for both NMOS and CMOS 8086/88. Now for 8- and 10-MHz 80186. Now for 6-, 8-, and 10-MHz 80188. Now for 10-, 12.5-, and 16-MHz 80C186.
COST: At 100 qty, under $5 for 8086/88; under $10 for 80186/188 in PLCC. $18 for 80C186 in 1k qty.
SECOND SOURCE: For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, OKI. For 80186/8188: AMD, Fujitsu, Siemens.
CORE: Intel's ASIC group says it will be incorporating 80C186 in its cell library.

Description: Supplier's objective when 8086 was introduced back in '78 was to offer a machine that matched performance of latest mid-range minis but retained some upward compatibility with widely used 8080/85. 8088 is intended as highest performance 8-bit μP. Floating-point math coprocessor (8087) available to enhance performance. 80186 and 80188 are intended as higher-integration counterparts of 8086 and 8088. They incorporate some of the often-used support-chip functions on CPU chip, somewhat in anticipation of ASIC standard-cell trend (and in fact Intel plans to add 8086 family members to its ASIC cell library to give customers a chance to design their own higher-integration combinations).

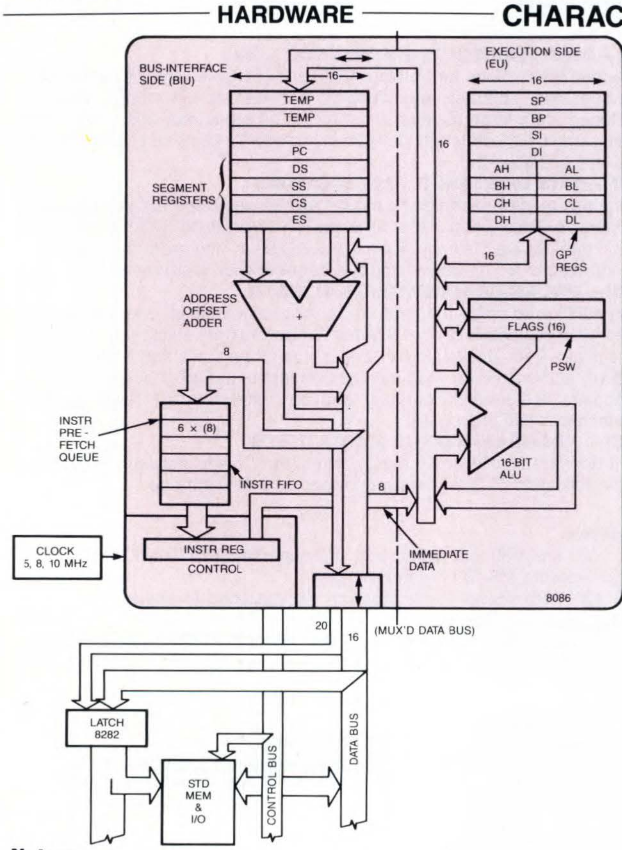
Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Status: Next to the 8080/Z80 family group, the 8086 family has been the most successful μP family. The most visible application for the family has been in the IBM PC and its many clones. The 80186/88 high-integration versions covered here were intended for PC applications, but the 80188/86 never caught on with PC makers. Now that new designs for the PC market have switched to the 80286 and 80386, Intel is directing the 80186/88 at embedded applications, and is claiming success—2000 design wins for 80186 and 600 design wins for new 80C186.

CHARACTERISTICS

HARDWARE



Notes:
1. Diagram is for initial family member, 8086.
2. 8088 is downgraded version of 8086. It has only 8-bit-wide external data output bus (only 8 lower bits of address bus are multiplexed for data). Some pin functions have been changed. Prefetch queue is only 4 bytes (to prevent overuse of bus). Instruction execution is slower as all 16-bit fetches and writes take 4 extra cycles.
3. 80186/88 integrate support functions on chip to reduce system costs. Functions added are clock generation, 2-channel DMA, interrupt controller, 3 16-bit timers, memory- and peripheral-chip-select logic, and wait-state generator. 80188 is 8-bit external data-bus version of 80186; it has shortened prefetch queue, and instructions take longer.
4. Math coprocessors implementing IEEE-754 floating-point standard are part of family.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide
Logicals
Bit, byte, word, and block operations

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base plus index, and base relative indexed
Use of segment registers: Programmer can, through software, set up four areas in memory with four segment registers—a program area, a stack area, and two data areas. These areas need not be full 64k, and they can overlap. Programmer can alter the four area locations by modifying the segment-register contents

III—PROGRAM-MANIPULATION INSTR
Has call, jump, and return instructions both inside program segments and to different segments. Intrasegment call and jump use self-relative displacement for position-independent code. Conditional jump upon Boolean functions of flags within ±128 bytes of instruction. Iteration control of loops, a repeat prefix for rapid iteration in hardware-repeated string operations
Note: Jumps can occupy varying amounts of execution time, because with BIU's instruction prefetch, the program counter can be ahead of itself

IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8080/85 flags: overflow, interrupt enable, direction (for strings), and single-step trap flags

Notes:
1. Enhanced CPU in 80186/188 includes new instructions: Pusha, Popa handle all registers at once; Immediate mode for Push and Imul; Ins and Outs for strings; Bound for address ranging; Enter and Leave for stack-frame saving and restoration.
2. Further enhancements in 80C186 include power saving with programmed clock division, and DRAM-control circuit.

Specification summary for 8086/88: 16-bit CPU that can reach 1M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 μsec with 5-MHz clock (0.37 μsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry; requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch 8 pins from minimum to maximum external system mode. Harris CMOS 8086 dissipates only 10 mA/MHz when running, and clock can be stopped for 500 μA standby.

Specification summary for 80186/188: Highly integrated μPs that combine functions of most common iAPX 86 system components onto one chip. Have same memory reach as 8086/88 but with improved execution times on some instructions. HMOS II ion-implanted, depletion-load, silicon-gate circuitry requires 5V at 300 mA (90 mA and less for CMOS). Housed in 68-pin JEDEC Type A ceramic leadless chip carrier and a ceramic pin-grid array. Plastic leaded chip carrier also.

SUPPORT

HARDWARE

From Intel: I²ICE in-circuit emulator ($7995) supports 8086/8088 and 80186/80188 to 10 MHz. Emulators are hosted on IBM PC and Intellec Series III/IV development systems. ICE186/188 in-circuit emulator supports 16-MHz operation.
From others: Because of popularity, family is widely supported by third-party universal development systems.

SOFTWARE

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. Pscop-86 provides source-level debug with full source-code display. Hosts include PC-DOS, VAX/VMS, and Intel development systems. Prices start at $750 (for DOS versions).
From others: Because of wide base of 8086/8088-based systems, and in particular the IBM PC, there exists a lot of third-party software of all sorts, enough to fill whole catalogs. Check with Intel and various trade journals.

80286

16-BIT NMOS

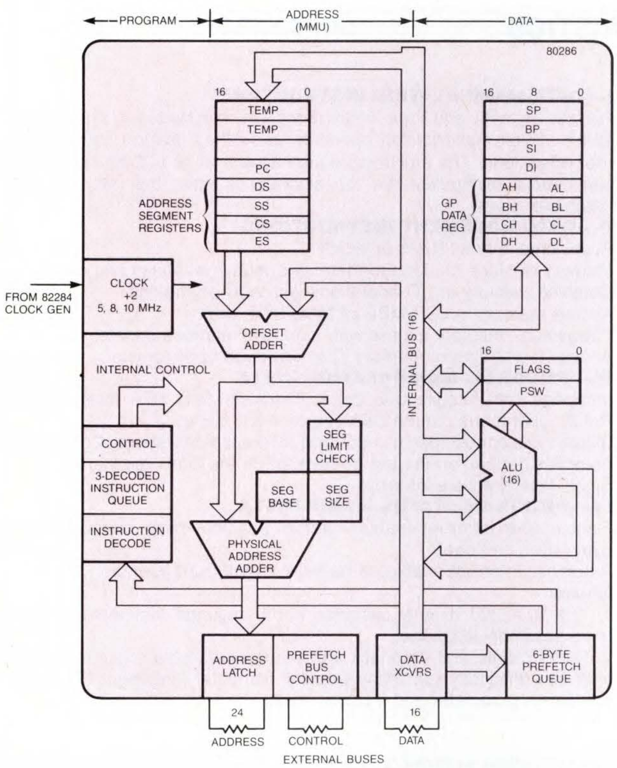
AVAILABILITY: In production with 8, 10, 12.5 and 16 MHz (AMD for 16 MHz). CMOS 80C286 12.5 MHz in production and 20 MHz sampling.
COST: In 100 qty: $37 for 8 MHz, $59 for 10 MHz, $95 for 12.5 MHz, and $150 for 16 MHz in LCCs (PGAs more). For 80C286: $125 for 10 MHz and to $170 for 16 MHz, also in 100 qty.
SECOND SOURCE: AMD, Siemens, and Fujitsu. Harris for CMOS 80C286.

Description: An evolutionary extension of the 8086 with special capabilities for multitasking systems. Has on-chip memory-management and protection functions that support intertask isolation, program and data security, and 4 levels of privilege within a task. Memory management supports as much as 1G bytes of virtual-address space per task, mapped into a 16M-byte physical memory. Device is upward compatible with 8086/88 software.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Status: Currently, the 80286 has the highest volume in the 8086 family. The total volume of 80286 chips was 4 million units for 1987. The 286's popularity has been based on the PC/AT, and the 286 will also share in the expected growth of the IBM PS/2 market. Its big sister, the 80386, will take over some of the 286's applications, but that will take time. Certainly the second sources will wish to give the 286 as long and thriving a life as they can, as so far Intel has shown no inclination to ever let them second source the 80386. Therefore it's logical to expect more enhanced 286s, such as the 16-MHz version from AMD and the CMOS version from Harris.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Support chips for 80286: 82C284 clock, 82288 bus controller, 80287 floating-point numeric processor ($290 for 10 MHz, 100 qty), and 82258 advanced DMA coprocessor.
2. A new trend is for third-party VLSI houses to do high-integration chip sets to consolidate the devices being used around popular platforms, which for the 80286 would be the IBM PC/AT. Chip sets for the PC/AT are being offered by Chips and Technologies (San Jose, CA), Zymos (Sunnyvale, CA), VLSI Technology (Phoenix, AZ), and Hudson & Supinger (Santa Clara, CA); and also by Intel.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide
Logical operations on bytes, words, and blocks
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base plus index, base relative indexed, and register indirect
Programmers can manipulate 16,383 segments in memory by means of memory-base descriptor tables and 4 segment registers. These segments can be between 1k and 64k bytes in length
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks
Intrasegment calls and jumps use self-relative displacement for position-independent code
Intersegment calls and jumps use the memory-based descriptor tables to provide position-independence of code
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction
Iteration control of loops
String instructions, including repeat, for rapid iteration
IV—PROGRAM-STATUS-MANIP INSTR
8085 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible

Notes:
1. Has high-level-language support instructions.
2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.
3. Trusted instructions can only be executed at highest protection levels.

Specification summary: 16-bit CPU with 1G-byte virtual-address space per user, mapped onto 16M-byte physical-address space. Bus cycles execute in 250 nsec at 8-MHz clock (200 nsec at 10 MHz), requiring 0.25 μsec for register-to-register moves at 8-MHz clock, with 8M-byte/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry in a large chip (335×339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has two operating modes: Real-address mode emulates 8086; protected virtual-address mode native to 286. Housed in a 68-pin JEDEC Type A leadless chip carrier, PLCC, and PGA.

HARDWARE — SUPPORT — SOFTWARE

From Intel: ICE in-circuit emulator ($9995) supports 80286 at 8 and 10 MHz. It is hosted on IBM PC/AT/XT and Intellec Series III/IV development systems. ICE286 ($12,495) supports 80286 at 12.5 MHz. iPAT Performance Analysis Tool, consisting of a hardware base unit, an interface to ICE, and host software for the PC/AT/XT, as well as Intellec Series III/IV. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 80286.
From others: Number of third parties support 286 on their universal development systems; for example, American Microsystems Corp (Beaverton, OR).

From Intel: Macroassembler (ASM 286) that includes systems builder, binder, mapper, and librarian. Compilers for C, Pascal, PL/M, Fortran, and Ada. For applications running in virtual 8086 mode, any of Intel's 8086 software tools can be used. Hosts include PC-DOS, VAX/VMS, and Intel development systems. Prices are $750 for DOS. Real-time operating systems (Intel's iRMX 286) available.
From others: Other operating systems and compilers being developed by third-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Coherent 286 (Mark Williams), Concurrent DOS (Digital Research), Unix System V (Digital Research), and of course OS/2 by Microsoft (Redmond, WA).

RTX2000

16-BIT CMOS

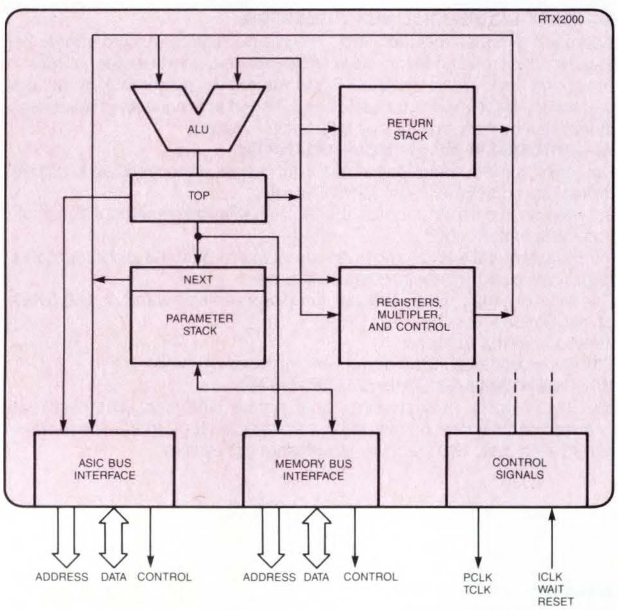
AVAILABILITY: Engineering samples of the RTX2000GI-8E (8 MHz) and the RTX2000GI-10E (10 MHz) are available now in 85-pin PGA packages. Harris expects to have production quantities on the market late in '88.
COST: In single-piece quantities: 8-MHz RTX-2000 costs $190, the 10-MHz version costs $250.
SECOND SOURCE: Zoran Corp (Santa Clara, CA).
CORE: Available in the Harris Advanced Standard Cell and Compiler library.

Harris Semiconductor
Box 883
Melbourne, FL 32902
Phone (407) 724-7418

Description: The RTX2000 is a high-performance 16-bit μP with on-chip timers, interrupt controller, multiplier, and two 256-word stacks. The manufacturer claims that the chip offers a sustained performance above 10 MIPS, because each instruction requires only a single clock cycle for execution. The chip's architecture lets designers add hardware accelerators and I/O devices that extend the chip's basic structure. The CMOS RTX2000 operates between dc and the maximum clock rate. Power consumption is typically 5 mA/MHz.

Status: Although Harris places its RTX2000 in a RISC microcontroller category, the chip fits into the general-purpose μP category, too. The company expects most of the chip's applications will fall into the real-time embedded-control realm. Because the chip directly executes Forth-language commmands, Harris expects that designers will find it relatively easy to do real-time software development. Harris designed the RTX2000 using its advanced standard-cell and compiler library. Thus, designers can incorporate the device into ASIC chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram shows basic RTX2000 architecture.
2. The ASIC-bus interface lets designers extend the chip's basic architecture with peripheral and I/O devices.

I—DATA-MANIPULATION INSTRUCTIONS
Full set of math and logic instructions which includes a single-cycle 16-bit×16-bit multiplication operation as well as division and square-root operations. The architecture also allows 16-and 32-bit shifts. You can directly manipulate the top element of either the return or the parameter stack
II—DATA-MOVEMENT INSTRUCTIONS
Access memory as bytes or words
Memory-to-stack or stack-to-memory operations require two cycles
Combine memory or I/O operations with ALU operations
Access memory in LSB-MSB or MSB-LSB order
"Streamed" memory access with automatic address update
Access to 1M byte of memory space through page register
III—PROGRAM-MANIPULATION INSTR
Intrapage calls require one cycle, interpage calls take three cycles.
Return operations require either zero or one cycle
Single cycle conditional or unconditional branch operations. Conditional branches depend on the top-of-stack or on the index registers
Single-level software interrupt
IV—PROGRAM-STATUS-MANIP INSTR
Flags include interrupt enable; interrupt pending; carry; complex carry; byte order; and boot
Automatic interrupt enable on return-from-interrupt operation
Notes:
1. The RTX2000 directly executes Forth-language statements—there is no assembly language.
2. Harris claims that the stack architecture is flexible enough that the chip can efficiently run many popular computer languages. The chip contains a parameter and a return stack.

Specification summary: 16-bit CPU with 1M-byte address space. Bus cycles execute in 100 nsec with a 10-MHz clock. All instructions execute in 1 or 2 cycles, and the memory bus is active during every cycle. Additional I/O bus for high-speed transfer operations simultaneous with memory-access and processing operations. The architecture includes two 256-byte stacks, both of which may be active when memory- and I/O-transfer operations take place. Harris claims a peak data-transfer rate of 80M bytes/sec. On-chip peripheral devices include 3 counter/timer units and a 16-bit multiplier. The 170,000 mil^2 chip comes housed in an 85-pin PGA, or an 84-pin PLCC package.

HARDWARE — SUPPORT — SOFTWARE

From Harris: A Real-Time Express Development System (10-MHz, TRXDS-10; $2995) runs from within an IBM PC or compatible. Harris also offers 8- and 10-MHz development boards (from $1495) for those who want to write their own development software.
From others: Silicon Composers (Palo Alto, CA) supplies a development board for IBM PC, PC/AT, and compatible computers. The MicroProcessor Engineering (Southampton, UK; US agency is AMICS Enterprises, Rochester, NY) Power Board is a stand-alone unit that furnishes a variety of I/O ports and 500k bytes of RAM.

From Harris: Available software includes a target/host monitor; a PC-based Forth development system; an RTX Forth cross-compiler; a disassembler; and a DOS file utility program. A Forth kernel and a multitasking operating system are in development.
From others: Laboratory Microsystems (Marina del Rey, CA), Forth Inc (Manhattan Beach, CA), and others have software packages for the RTX2000 μP. MicroProcessor Engineering's Power Forth for its development board is an extended Forth-83 development environment.

80386 FAMILY — 32-BIT CMOS

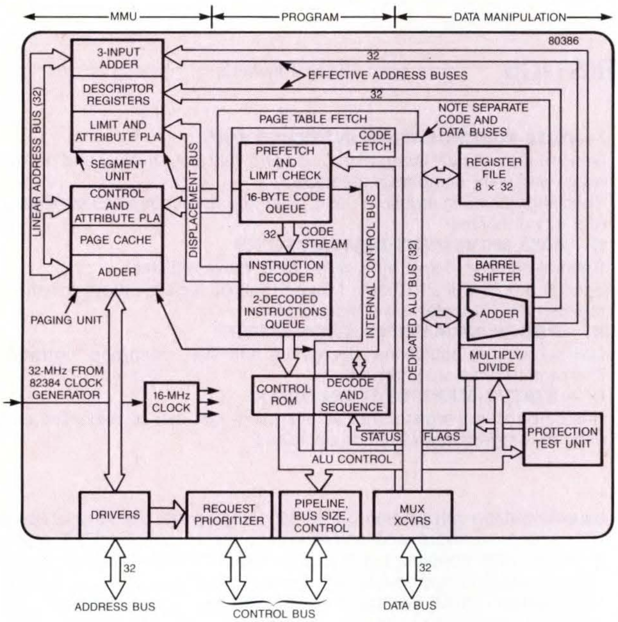
AVAILABILITY: 16, 20, and 25 MHz in production (at 4 locations). 80386SX in production, 80376 samples available now.
COST: In 100 qty, $299 for 16-MHz 80386, $484 for 20-MHz 80386. 80386SX in production; $219 (100). New 80376, $72 (1000).
SECOND SOURCE: None announced or planned in immediate future.

Description: The 32-bit member of the 8086 family, suitable for both mutiprocessing and multitasking. Contains a full 32-bit, largely uncharacterized register set (some competitors debate this) and an on-chip MMU containing selectable segmentation and paging support with a 32-entry TLB. Has slower emulation mode in which it is 100% binary compatible with the 8086 and 80286, allowing 8086 and 80286 and 80386 applications to run concurrently.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

Status: All things point to the 80386 remaining the dominant 32-bit µP, certainly for the next 5 years and probably until the year 2000. The 386 is not necessarily the best µP, but it's the sole µP carrying the IBM PC momentum into the 32-bit world. Not satisfied that it "owns" the MS-DOS and OS/2 world, Intel is now aggressively after the Unix world and now has samples of the 80376—a version of the 386 aimed at the embedded-controller world. Intel recently introduced the 80386SX, another version of the 386 that supplies a 16-bit data bus and a 24-bit address bus. The new chip is aimed the installed base of 8086 and 80286 chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. No on-chip cache, but 20-MHz 82385 cache controller ($125 for 20 MHz at 10k qty) for implementing 32k-byte external cache. Has posted-write and bus-watch features.
2. MMU on chip said to allow for memory management with no penalty in bus bandwidth (if off chip, supplier says, an extra cycle would be needed). Allows choices of segmentation or paging singly or in combination for multiuser protection and for virtual memory.
3. The 80386 has its own math coprocessor, the 80387 ($441 for 16 MHz, $583 for 20 MHz, 100 qty).
4. Along with the 80387 and 82385, the 80386 can use the 82380 32-bit peripheral combination chip that incorporates DMA and interrupt support and interval timers, etc.
5. The 80376 is compatible with the 386 programming model, but cannot run 8086 or real-mode programs. The chip has a 16-bit external bus.

I—DATA-MANIPULATION INSTRUCTIONS
Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter)
Conversion between bytes, words, and double words
Arithmetic, including 16-bit and 32-bit operands and 32-bit signed and unsigned multiply and divide
(80387 math coprocessor has full IEEE-754 instructions, including all transcendentals)
II—DATA-MOVEMENT INSTRUCTIONS
String moves and gang push and gang pop of all registers
Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers)
III—PROGRAM-MANIPULATION INSTR
Repeat instructions based on flags
Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4G-byte memory space
IV—PROGRAM-STATUS-MANIP INSTR
Flag instructions mostly same as on 8086 (contains 4 debug registers, allowing breakpoints on data or code accesses, even when in ROM)
V—HLL AND OS INSTRUCTIONS
Instructions for checking array bounds
Segment assignment instructions
Load and store descriptor tables for protection (processor context switch via 1 instruction)

Notes:
1. Only those instructions beyond basic 8086 instructions described.
2. 80386 said to be object-code compatible with previous members of 8086 family and can run their operating systems. There is a "virtual 8086" mode in which 8086 (and 8088) code can be run within the protected 386 environment.

Specification summary: A more or less standard, "classical" 32-bit minicomputer architecture that has a basic register set similar to the previous 16-bit members of 8086 family so that it can directly run their machine code. It has added features that make it more general and suited to larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. Performance can be 9k Dhrystones when operating at 16 MHz and with sufficiently fast (45-nsec) memory. Fabricated in 1.5-µm CMOS (supplier calls it CHMOS-III), it's expected to consume no more than 400 mA at 32-MHz external clock (16 MHz internal). Packaged in 132-lead ceramic PGA.

HARDWARE — SUPPORT — SOFTWARE

ICE-386 in-circuit emulator for 80386 hosted on Intel 286/310 running Xenix 286, allowing full 16-MHz operation in continuous or single-step mode. Can store more than 2000 frames of program-execution history. Has high-level-language symbolics. Can analyze time taken by code. Supports 80287 and 80387 coprocessors.
iSBC 386/20 single-board computer for Multibus I and iSBC 386/100 single-board computer for Multibus II. Besides the usual features expected of supplier's single-board computers, these incorporate 64k-byte caches to permit 16-MHz execution of 386. Starter kits are $9490, $7995, and $3860 in 100 qty.

From Intel: ASM-386 macroassembler ($600) and PMON-386 ($3500), DOS-hosted software debugger (DMON-386 ($2500) is unhosted version). Also iC-386 and PL/M-386 high-level languages, RLL-386 set of relocation linkage and library utilities ($600).
From others: Rapidly growing third-party support, of which most important are MS-DOS and OS/2 from Microsoft (Bellevue, WA). (There are variations in DOS such as Concurrent DOS by Digital Research (Monterey, CA).) Next is Unix V from AT&T (Morristown, NJ) and Zenix from Microsoft. Also real-time executives from Ready Systems (Palo Alto, CA), JMI Software (Spring House, PA), and others. In addition there are dual combinations of operating systems such as Unix-DOS from Phoenix (Norwood, MA), Locus (Santa Monica, CA), and Interactive Systems (Santa Monica, CA); CTOS-DOS from Convergent Technolgies (San Jose, CA); and DOS-DOS from Intelligent Graphics (Santa Clara, CA).
Note: Some software depends on 386 mode.

340X0 GRAPHICS μP FAMILY

32-BIT GRAPHICS

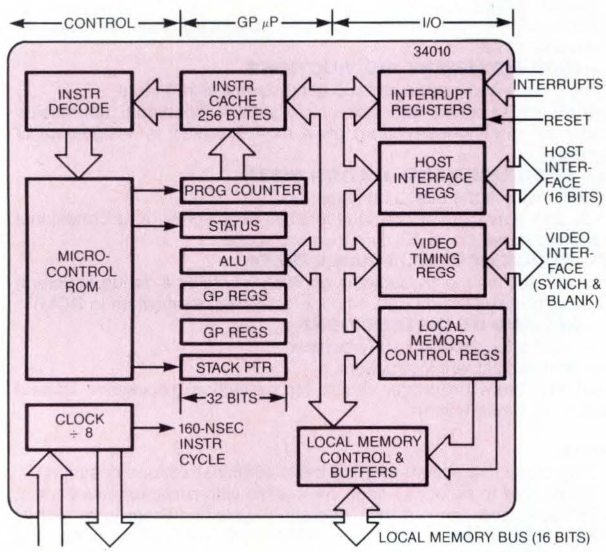
AVAILABILITY: Now.
COST: $50, qty 10k.
SECOND SOURCE: Under active consideration.

Texas Instruments Inc
MOS Microcomputers
Box 1443
Houston, TX 77001
Phone (713) 274-2000

Description: 32-bit CMOS μP optimized for graphics-display systems, but with true general-purpose Von Neumann architecture so it can be used for other applications that need the same bit manipulations as are required of pixel manipulations of CRT-type raster graphics. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular μP instructions, it has specialized instructions for pixel manipulation. 1G-byte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits).

Status: This μP is included in directory despite its obviously specialized slant toward CRT graphics because it has a general-purpose Von Neumann architecture and instruction set, and some of its attributes can be equally applied to other, nongraphics applications. In particular, its ability to do rapid bit manipulation of a large local address field. From the number of IBM PC-based board-level products announced that incorporate this part, it can be concluded that it is a success. One nongraphic area being explored by users is for industrial control where bit manipulation and low cost relative to other 32-bit μPs is found attractive, according to TI (even for consumer-oriented uses such as arcade games). In some cases, designers in nongraphic areas are making clever use of some special graphic features.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Added graphics features are embodied in the second 16×(32) register file and among 28 16-bit I/O control registers. They allow programmable pixel and pixel-array processing for both monochrome and color systems of variable pixel sizes. Hardware incorporates 2-operand raster operations with Boolean and arithmetic operations, x-y addressing, window clipping, window "pick" operations, 1-to-n bits/pixel transforms, transparency, and plane masking.
2. TI's 2nd-generation version (34020) will have a full 32-bit (nonmultiplexed) bus for greater bandwidth.

I—DATA-MANIPULATION INSTRUCTIONS
General-purpose μP instructions: add and subtract, multiply and divide, rotate and shift, compare and logicals
Special graphics instructions: add, subtract, and comparisons relating to x-y coordinates
II—DATA-MOVEMENT INSTRUCTIONS
General-purpose: Move byte, move field, move register
Special graphics instructions: Move x half of register, move y half of register, pixel transfer, pixel block transfer
III—PROGRAM-MANIPULATION INSTR
Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt
IV—STATUS-MANIPULATION INSTR
Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions

Specification summary: 32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16×(32) registers files, hardware stack pointer, and 256-byte instruction cache. One of the 16-word register files contains stack pointer and 15 general-purpose registers (the equivalent of the GP registers found in regular nonspecialized μPs). Addressing modes of these registers are tuned to support high-level languages. Other register file is dedicated to CRT control as described in hardware note. Has 32-bit-wide address-data bus to support a gigabyte of off-chip "local" memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A microcoded local memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host μP. Fabricated in 5V CMOS and packaged in 68-pin PLCC. TI expects to sample its 34020 chip in early 1989. The new chip is compatible with the 34010, but provides a 512-byte cache and supports 1M-bit VRAM chips.

HARDWARE — SUPPORT — SOFTWARE

From TI: TMS34010 software development board ($1495), which plugs into IBM PC or compatible. Used for evaluation, familiarization, and software development, and comes with user interface and debugger software. TMS34010 XDS/22 emulator box ($14,995) operates as a stand-alone unit with nonintelligent terminal or with IBM PC or compatible as host.
From others: Board-level and other hardware support now available from numerous sources. See TI's *TMS 34010 3rd-Party Guide* (call (800) 232-3200, ext 701, and ask for literature No SPVB066A).

From TI: TMS34010 assembler package ($500) for IBM PC and compatibles using MS-DOS 2.11 or higher and for VAX ($1000) using VMS, Unix Berkeley 4.2, or Unix System V. Includes macroassembler/linker, source/object code archiver, and ROM utility. MS-DOS version also has a 34010 simulator.
A C compiler supporting full Kernighan & Ritchie C with extensions for in-line assembly code and enumerated data types. $1000 for PC and $3000 for VAX.
A graphics/math function library ($5000 for source code) provides graphics primitives, transcendental functions using double-precision floating point, matrix operations for 3-D transformations, text generation, etc. TI also offers a font library that contains 19 font styles and over 100 font sizes ($3000).
From others: Software now available from numerous third-party sources such as JMI (Spring House, PA), which has done a real-time executive. See the TI *TMS 34010 3rd-Party Guide* mentioned under Hardware Support.

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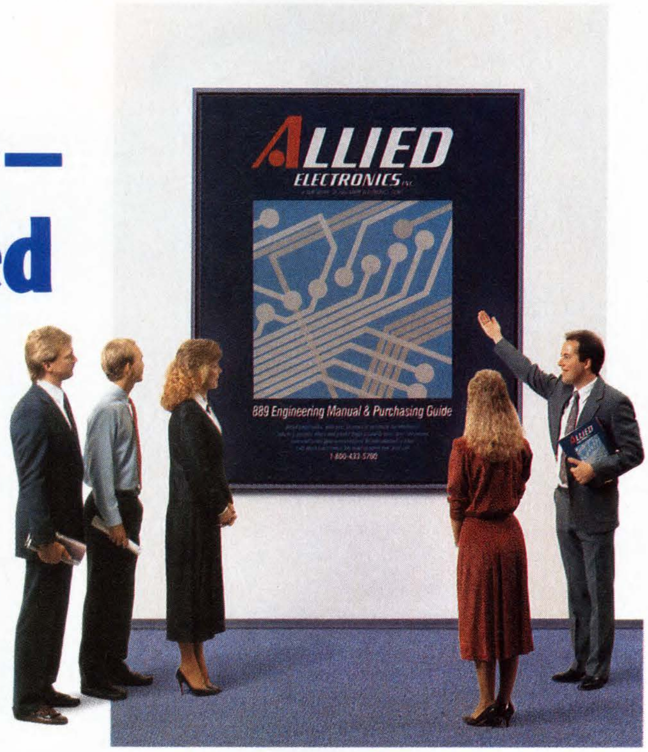

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CIRCLE NO 162

8051 Emulator Has Innovative Breakpoint Features

Nohau Corporation's 8051 emulator, the EMUL51-PC, uses a 64K bit RAM to generate breakpoints. Each of the 65,536 possible combinations of the 16 address lines corresponds to one bit in the breakpoint RAM. The "break bit" coming out of the RAM is then qualified with RD (read), WR (write), FB (first byte of instruction) and an optional user-chosen external signal.

The concept of calculating and writing relevant patterns into the breakpoint RAM results in a number of sophisticated breakpoint features. Individual addresses, ranges of addresses and "wild-carded" addresses are among the most obvious useful setups.

Using line numbers and the corresponding values from symbol lists generated by C-compilers and PL/M compilers, breakpoints can be set on the first assembly instruction in each source line. The result is a "high-level" single step function.

Everyone who has debugged 8051 code has probably wished for the ability to break on a change of value in internal data RAM and special function registers. This feature is made possible by scanning the entire code memory for instruction patterns which would write to a specified byte or bit if they were executed. Memory changes caused by indirect writes and stack manipulations cannot be detected this way in real time, but a pseudo-real-time feature of the EMUL51-PC makes even this kind of breakpoint possible.

Every software engineer's nightmare is to have a program that crashes in a random way, especially if the crash happens only once a day, or once a week. Bugs like these may be virtually impossible to find, and they can cause severe problems for end users. A crash often results in the loss of program control, with instructions being executed outside the legal program area, in data tables, or even on second and third bytes of legal instructions.

The emulator can be set up to break when the program goes out of control. This setup is accomplished by first setting the entire breakpoint RAM so that every address would generate a breakpoint, then defining the starting and ending points of all blocks of legal instructions and finally by removing breakpoints on every valid FB (first byte of instruction).‡ Execution will then break as soon as the program goes outside of legal program blocks. By looking back in the EMUL51-PC's 16K trace buffer (described in a separate article), the engineer has a very good chance of seeing the cause of the problem.

Nohau Corp., 51 E. Campbell Ave., Campbell, CA 95008 (408) 866-1820

‡Pat. Pend. by Logical Services.

VL 86C0X0 ARM

32-BIT CMOS

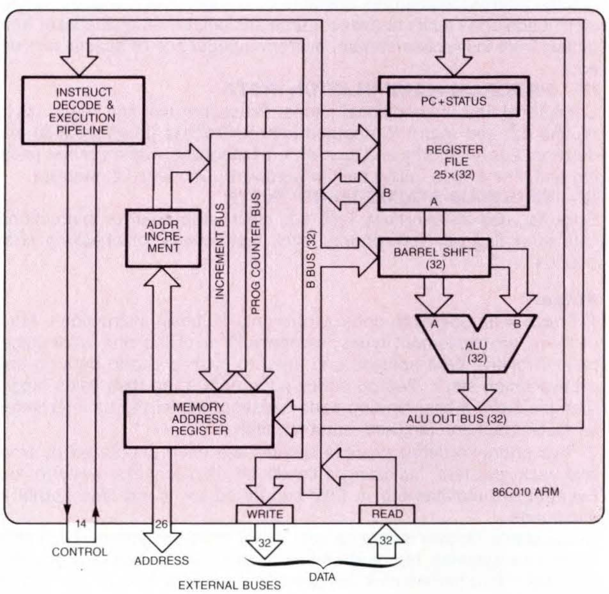
AVAILABILITY: Now for production volumes of 86C010.
COST: $99 for samples. $20 for 86C010 in volume.
SECOND SOURCE: None.
CORE: Part of VLSI's cell library. (Was designed by customer Acorn Computers using VLSI's semicustom tools.)

VLSI Technology Inc
1109 McKay Dr
San Jose, CA 95131
Phone (408) 434-3000

Description: ARM stands for Acorn-RISC machine (RISC stands for reduced-instruction-set computer). According to RISC-architecture philosophy, by leaving out seldom-used instructions, a designer can make chip smaller and faster. Then, when complex instructions are needed, they can be generated by compiler, which in turn is supposed to be more efficient and easier to write because of simpler instructions. It is one of first μPs designed by customer using supplier's ASIC tools. It took 2 systems engineers and 4 circuit designers at Acorn 18 months to design initial 86C010 chip, but announcing subsequent upgrades such as the 86C020 (tentative number) are that much easier and quicker, because the μP is now part of the VLSI ASIC library and the Acorn designers are familiar with the design tools.

Status: VLSI is the foundry for Acorn Computers Ltd's (Cambridge, UK) ARM μP, and Acorn has permitted VLSI to market the ARM μP to the general OEM market. VLSI says its strategy will be to keep the ARM priced well below other 32-bit μPs (as indicated by the $20 volume price compared to $200 or more for other 32-bit chips). The low price will be possible because the ARM's bare-bones architecture keeps the chip size small (230 mil sq compared to as much as 400 mil sq for some other 32-bit devices). VLSI says Acorn demand is sufficient to get the ARM μP up the learning curve. VLSI plans to use the ARM core as basis for ASIC variations and has found interest from US OEMs in two areas: embedded controllers for graphics and printers, and artificial intelligence (according to VLSI, the ARM runs A/I programs like Lisp surprisingly fast).

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. In addition to 86C010 μP, VLSI has associated set of chips for memory (86C110), video (86C310), and I/O (86V410). For floating-point math, VLSI suggests using one of the commercially available coprocessors such as AT&T's WE32206.
2. Note the 25 registers. This is less than on some RISC machines, but they do overlap as is common in RISC to speed interrupt service (overlapping gives automatic saving of data). This means programmer only sees 16 registers at most, and of these, only 15 are general purpose.
3. Some provisions for memory management, including cache and virtual memory through abort signal, mode control bits.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, logicals and comparisons. Bit clear. Shifts (barrel shifter with ALU)
II—DATA-MOVEMENT INSTRUCTIONS
Most data movements are by register-to-register instructions with option for multiple-register addressing. Only load and store operations to memory (typical of RISC)
III—PROGRAM-MANIPULATION INSTR
Skip-type decision instructions (though old-fashioned, this simple approach can give fastest response in some cases). Branch instruction has option where combined PC and status register are copied in R14 data register for quick, simple return
IV—PROGRAM-STATUS-MANIP INSTR
Usual status bits are combined with PC and mode-control bits in a 32-bit-long register. This allows all three elements to be saved in one fell swoop

Notes:
1. Only 44 instructions, in keeping with RISC concept.
2. Simple RISC instructions are said to ease the task of writing efficient high-level-language compilers.
3. User and supervisory modes with supervisory mode being entered by software interrupt.

Specification summary: 32-bit CMOS Von Neumann (common memory) μP with RISC-style architecture. Has simple ALU with associated barrel shifter and set of 32 registers on CPU μP chip, 16 of which are accessible to programmer. Has some features expected in a large-memory-space machine: instructions and controls to handle virtual memory and caching. 32-bit external data bus and 26-bit external address bus allows linear addressing for external 64M-byte external memory space (can be addressed on 8-bit-byte or 32-bit-word basis). Only simple load and store instructions for external memory. 10- to 12-MHz, 2-phase clock gives 4- to 5-MIPS sustained performance with 10 to 12 MIPS max. Interrupt latency is 2.75-μsec max. No provisions for separate I/O addressing so I/O must be memory mapped. Fabricated in 2-μm CMOS with chip 230 mils on side. 0 to 70°C temperature range. Packaged in 88-pin JEDEC Type-B leadless ceramic chip carrier and plastic leadless chip carrier.

HARDWARE — SUPPORT — SOFTWARE

VLSI says that much of the hardware support comes from Acorn. There is a PC-form-factor board ($2500) for software development. (Note: It can be expected that VLSI will bias its support toward the ASIC approach, in which the ARM μP will be considered a core around which the customer will be encouraged to apply "application-specific" I/O, memory, etc; thus, VLSI's ASIC design tools might be considered part of the hardware support.)

VLSI indicates that most of the software support comes from Acorn. There is an assembler for the ARM's instruction set, a Basic interpreter, and compilers for popular high-level languages (C and Fortran-77). There are also compilers for artificial-intelligence languages (Cambridge Lisp and Prolog). Typical pricing for software is $500 each.

IMS T212, T414, T800 TRANSPUTER

16/32-BIT CMOS

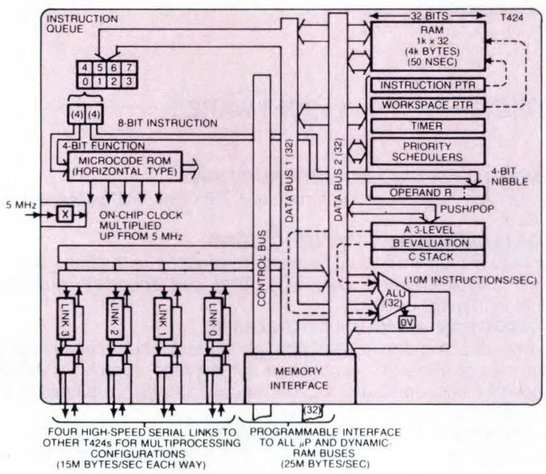
AVAILABILITY: T801, T425, and T222 available late '88 or early '89. All other chips available now.
COST: In 100 quantities; T212, $119; T414, $254; T800, $487.50.
SECOND SOURCE: None.

Description: RISC-like machine, though it uses microcode and has multiple-cycle instructions. Most interesting feature is incorporation of interprocessor communication links to simplify construction of multiple-Transputer systems. As many as 100 Transputers have been linked in parallel, and supplier claims that the performance increase has been linear. To make such multiple-μP systems feasible from standpoint of cost and board space, supplier has incorporated dynamic-RAM controller and timers, as well as communication links, on chips. Software support for multiprocessing is in form of multitasking real-time kernel in instruction set and supplier's Occam language.

Inmos Corp
Box 16000
Colorado Springs, CO 80935
Phone (719) 630-4000

Status: Volume buildup has been slow—Inmos reports 50k units for '87. One possible explanation is that most of the applications have been for multiprocesssor configurations (typically 4 to 10 Transputers), so designers have been engrossed by the challenge of developing practical parallelism. Supplier expects some of its 75 or so "design wins" will move into volume production '88 and '89.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram is for T424. T414 same except has only 2k-byte RAM. T212 is 16-bit version. T800 is 32 bits with 4k-byte RAM and IEEE-754 floating-point unit.
2. Unlike most other 32-bit machines, there's no group of general-purpose registers. Instead, substantial on-chip RAM plays an equivalent role.
3. ALU fed from 3 accumulators forming a small 3-deep stack, allowing compact implied addressing.
4. The four serial links allow arrays of Transputers in multiprocessing with no bus saturation, which is why speed increase when more μPs are added is said to be linear.

I—DATA-MANIPULATION INSTRUCTIONS
Integer arithmetic, including multiply and divide. Logicals, shifts, and comparisons. T800 has on-chip IEEE FP add and subtract, multiply and divide, and square root, both 32 and 64 bits
II—DATA-MOVEMENT INSTRUCTIONS
Memory-bandwidth block moves, 2-dimensional block moves for graphics BitBlt. Load/store of local variables done relative to workspace pointer. Indexed load/stores available from address in A register. Immediate loads done 4 bits at a time. Large immediate values loadable from tables, from instruction stream, or from a sequence of special instructions
III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional jumps. Procedure call and return. Subroutine call and return. Computed jumps. Process (task) creation and deletion. 2-level priority and time-sliced scheduling with message passing and time events, using built-in hardware. One level of interrupt
IV—PROGRAM-STATUS-MANIP INSTR
Error flag detects overflow. Test, set, clear, stop-on-error instructions. One error flag per task priority level. Instructions for checking array bounds

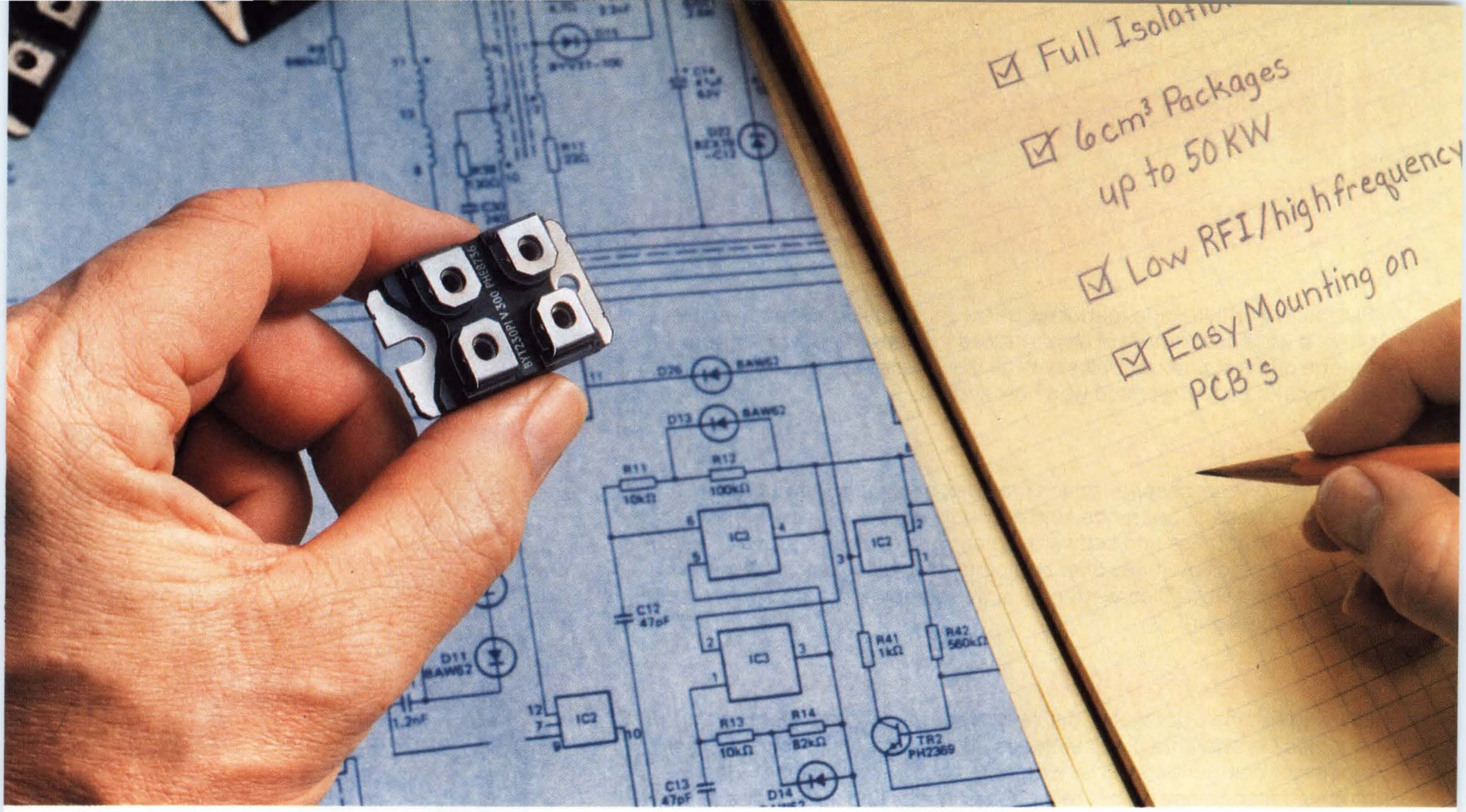
Notes:
1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack. Two op codes support building data fields bigger than the basic 4 bits. One op code causes data field to be interpreted as stack operation (eg, add, subtract, etc).
2. Two priority-ordered process queues are each supported by front and back registers, indicating a linked list of processes ready to run. Event-based multitasking is fully supported by a real-time kernel in microcode.
3. Supplier's Occam language said to facilitate programming multiple Transputer systems, but programmer must still study how best to partition task. Third parties have announced extensions to C to accomplish same ends.

Specification summary: Family of 16- and 32-bit μPs oriented toward multiprocessing. Unique in that they have the hardware and software links that allow them to be hooked to each other for parallel processing. The newest family member, the T800, has 4k-byte on-chip RAM, which occupies the bottom 4k bytes of a full 4G-byte address space. Four, full-duplex, 20M-bps serial links driven by on-chip, 8-channel DMA provide basic multiprocessor communication links as well as I/O. T800 has on-chip dynamic-RAM controller and a pair of timers. One 5-MHz external clock is multiplied by on-chip PLL to generate 20-MHz chip clocks, giving 50-nsec instruction cycle. Submicrosecond interrupt latency, procedure call, and task switch. Most instructions take 1 or 2 cycles. Integer multiply takes 38 cycles, and divide takes 39 cycles (under 2 μsec). Single-precision floating-point add takes 7 cycles (350 nsec), FP multiply takes 11 to 18 cycles (550 to 900 nsec), and FP divide takes 16 to 28 cycles (800 to 1400 nsec).

HARDWARE — SUPPORT — SOFTWARE

T800, T414, and T212 are available as discrete components as well as on board-level products, including boards for IBM PC, VME, Multibus, Macintosh, Sun, and MicroVax systems. Modules are also available, ranging from a T800 with 8M bytes to a T212 with 64k bytes, and include graphics facilities. Multiple modules can be mounted on a mother board, and the interconnections can be varied under program control using a IMSC004 switchbar chip on the mother board. Mother boards are available from Inmos and from third-party suppliers. Buses supported include those used in the computers listed above in this section.

From Inmos: C, Pascal, and Fortran compilers for all family members. Development tools allow multilanguage programming. For distributed systems and parallel computing, Inmos also offers Occam, a concurrent language with explicit facilities for Transputer interrupt handling, multitasking, and message passing. Compilers are available either as integrated suite—the Transputer Development System—with editor, compiler, syntax checker, and multiprocessor linker/loader, or as separate components for use with customer's own editors, etc.
From others: Inmos says there is a growing body of software tools from third parties, including C, Pascal, Fortran, Ada, Lisp, Prolog, Modula2, profilers, and debuggers.



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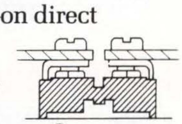

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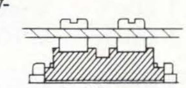

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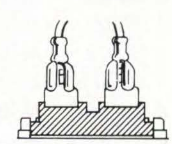

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DOT MATRIX MODULES

Utilizing Futaba's dot matrix displays, a completely intelligent line of "dot modules" is available. Each includes all drive, power supply and microprocessor components surface mounted onto a single board. Surface mounted technology results in higher reliability and allows for a smaller overall package and lower cost. All dot modules require only a 5V DC power source and can accept parallel or 8 possible serial baud rates.

GRAPHIC DISPLAYS/MODULES

Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1013A	GP1013A02	64X34	200	3.35X2.95X0.7
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1018A	GP1018A01	400X240	40	7.10X6.30X1.61
GP1004C	GP1004C03	640X400	30	9.65X7.3X1.85
GP1019A	GP1019A03	640X400	35	7.10X6.70X2.56

*Different Versions Available

DOT MATRIX/CHARACTER DISPLAY MODULES

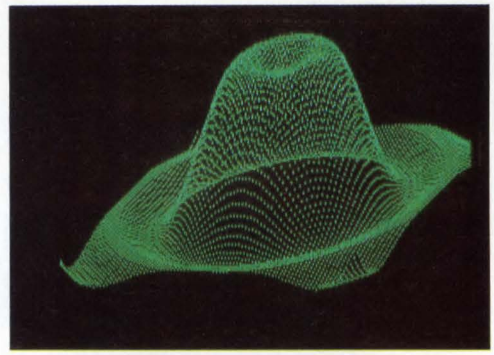
Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
16LD03G	M16LD03B	16X1	5X7	0.433	8.90X1.95X.98
16SY03Z	M16SY03B	16X1	14 SEGMENT ALPHANUMERIC	0.200	4.92X1.32X.83
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90

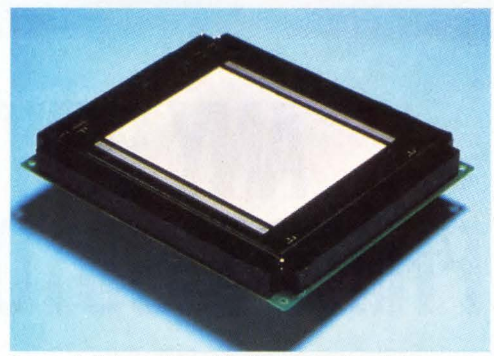
MANY OTHER DISPLAYS **NEW MODULES AVAILABLE SOON**

FUTABA
Corporation of America
Electronic Components Division

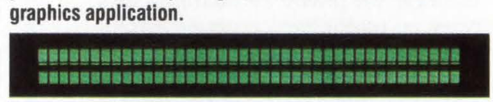
711 E. State Parkway
Schaumburg, IL 60173

Telephone: (312) 884-1444
FAX: (312) 884-1635

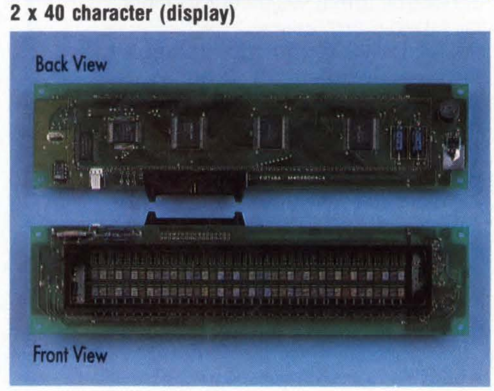




Compact, flat panel graphic displays and modules present clean, sharp images, whether for text or full graphics application.



2 x 40 character (display)



2 x 40 character (module)

Pattern flexibility and pleasing appearance are offered by Futaba in dot displays and modules.

Futaba also offers a complete catalog of alphanumeric, segmented displays.

Futaba supports its products with design engineering and system integration assistance. Call or write today.

Z8000/Z80000

16/32-BIT NMOS AND CMOS

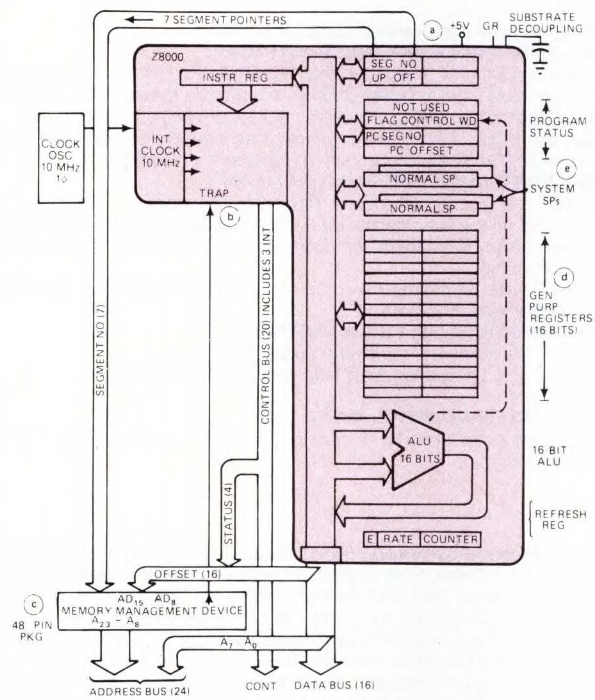
AVAILABILITY: Now for NMOS Z8000 at 4, 6, 10, and 12 MHz. Now for NMOS Z80000 at 8 and 10 MHz. CMOS versions for Z8000 in '89 and for Z80000 in '90.
COST: $13.80 for Z8000 in 10k qty.
SECOND SOURCE: AMD (licensed), SGS (Italy and Arizona), and Sharp for Z8000. NEC for Z80000, by mask exchange.
CORE: Zilog is incorporating both Z8000 and Z80000 as cores in its "in-house" ASIC library, planning to use Zbus for their systems on silicon. Says that 160×160-mil Z8000 core is small enough to leave room for other functions on practical 400×400-mil ASIC chip.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

Description: One of first μPs to have architectural features of a modern minicomputer. Original 16-bit Z8000 comes in 40-pin package for addressing 64k-byte memory or in 48-pin package for addressing 8M-byte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit μP, offering best CPU speed, interrupt handling, and character-string search. New 32-bit version, Z80000, is superminicomputer-like enhancement that remains object-code compatible with the Z8000. Has cache for data and instructions and an MMU.

Status: The Z8000 has, according to Zilog, found most acceptance in real-time control applications, particularly military. Supplier says it has been shipping samples of the much-delayed Z80000 for 6 months and some customers have found it will run at over 16 MHz in their systems. Zilog will be pushing the Z80320 "32-bits-for-32-bucks" derivative of the Z80000. Supplier has again slipped on its schedule for CMOS versions, and now says it will be '89 for Z8000 and '90 for Z80000.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
Supplier has companion peripherals suitable for both processors:
For Z8000, a range of DMA, FIFO, data ciphering (NBS), communications and counter/timer parts.
For Z80000, two 32-bit parts: a Z32104 CMOS DMA controller, 32-bit address and data buses with 8-bit peripheral bus; and a Z32106 CMOS floating-point coprocessor that implements IEEE P754 format.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed)
Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n)
Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulator
The Z32106 floating-point processor will do IEEE-754 operations
II—DATA-MOVEMENT INSTRUCTIONS
Eight addressing modes using general-purpose registers as indexers and stack pointers
Comprehensive set of block-transfer and string-manipulation macroequivalents, including many dedicated to I/O space
III—PROGRAM-MANIPULATION INSTR
Call and call relative (±4096 bytes)
System call using special system stack pointer
Jump conditionals
IV—PROGRAM-STATUS-MANIP INSTR
Set and reset flags, complement flags. Set-multiple-interrupt modes
Tests for the micro in and micro out lines for multiple-microprocessor configurations
V—SYSTEM-CONTROL INSTRUCTIONS
The 80000 has privileged instruction for exclusive use by an operating system

Specification summary: Common-memory architecture with optional separate I/O space and separate "systems" stack. Z8000 is 16-bit μP that has directly addressable memory space of 8M bytes (8001, 8003) using segment pointers, expandable to 48M bytes using the six available memory spaces and an MMU. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 μsec through 1 or 2 μsec to 7 μsec for 16-bit multiply, all at 10-MHz system clock (4 and 6 MHz also available). Eight large-computer-style addressing modes. NMOS, requiring one 5V supply (plus substrate-decoupling capacitor) in either 40-or 48-pin package. Z80000 is a 32-bit upward-compatible version of Z8000 and can run same software. 6-stage pipelining of instruction fetch/execute cycle and 256-byte on-chip associative cache for instructions and data for improved performance (and use of 100- to 120-nsec memories). Also on-chip MMU for virtual memory with address bus a full 32 bits for 4G-byte memory space. At 25-MHz, clock has 12.5-MHz (80-nsec) instruction cycles that give 12.5-MIPS burst rate (when doing loops out of cache) and 5 MIPS continuously (4 MIPS with MMU virtual-memory translation). 16×16 multiply in 1.2 μsec and 32×32 in 1.9 μsec. 2-μm NMOS dissipating 3 to 4W with 1½-μm CMOS promised for '88 (Z8000) and '89 (Z80000). Initial samples have been packaged in ceramic PGAs but lower-cost Z80320 will have muxed address and data buses and be in 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Z-Scan 8000 in-circuit emulator ($5500). 500-pg Z8000 technical manual.
From others: Applied Micro, Boston Systems, Hewlett-Packard, Kontron, Orion, Single Board Sol, Sweet Micro System, and Tektronix. Contact supplier for addresses.

From Zilog: Real-time application software (PC-based). C and PLZ/SYS compilers.
From others: Real-time executive from Ready Systems (Palo Alto, CA), VRTX/8002 ($5775), which is suited to embedded applications, and an Ada compiler ($795) from Meridian Software Systems (Laguna Hills, CA). Contact supplier for names and addresses of others.

68000 FAMILY

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

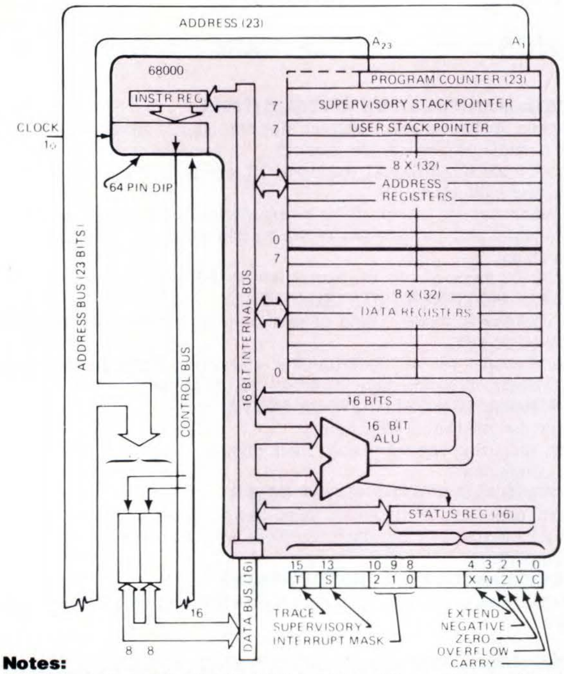
AVAILABILITY: Now for production quantities of all models to 25-MHz 68020. Samples of 68030.
COST: In 100 qty, from $10 for low-end 68008 and 68000 to $135 for 12.5-MHz 68020 and $530 for 25-MHz 68020. 68881 math coprocessor is $107 for 12.5 MHz and $347 for 25 MHz. Production pricing for 68030 not available.
SECOND SOURCE: Rockwell, Hitachi, Mostek, Signetics/Philips, and Thompson SGS, all licensed with mask interchange for 16-bit parts. Thompson was to be second source for 32-bit 68020, but Motorola says it plans to keep 68020 and 68030 to itself for time being.

Motorola Integrated Circuits Div
3501 Ed Bluestein Blvd
Austin, TX 78721
Phone (512) 928-6000

Description: Family based on a modern minicomputer architecture using a basic group of 16 fairly general, 32-bit registers. Family members have various addresses and data-bus widths and different ALU widths. The bottom of the line, the 68008, has a narrow 8-bit data bus. The middle member, the 68000, has a mid-sized 16-bit data bus and ALU and 24-bit addressing. Current top of the line, the 68030, is full 32 bits throughout with instruction and data caches and MMU on board.

Status: Part of the success of the 68000 family is due to the success of the Apple Macintosh II, and much of the rest is due to 68020's popularity among Unix-based workstations. The new 68030, which is now available, is similar to the 68020 but with an extra cache for data (in addition to the 68020 instruction cache) and with the 68851 MMU on board. There is considerable speculation about the competition the 68030 will receive from the new RISC μPs, including Motorola's own 88000 RISC chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram favors the basic 68000, which although it has 32-bit-wide registers, has 16-bit-wide ALU and data buses and only 23-bit-wide address bus. It comes in 64-pin DIP and 68-pin grid array.
2. Bottom-of-the-line 68008 has only 8-bit data bus and 20- or 22-bit address bus. It comes in 48-pin DIP.
3. Upper-range 68010 and 68012 are similar to 68000 but support virtual memory. 68010 has 24-bit address bus and comes in a 64-pin DIP or 68-pin grid array. 68012 has full 32 bits of address and comes in 84-pin grid array.
4. Top-of-the-line 68020 and 68030 are full 32 bits throughout, including ALU and address and data paths. Both have instruction caches and the 68030 also has a data cache and an MMU.
5. Two important support chips, not shown, are the 68881 floating-point coprocessor and the 68851 MMU. Both are in CMOS.
6. The 68070 by Philips/Signetics includes various support functions on chip.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply and divide (signed and unsigned)
Logicals and rotates and shifts
Can handle bits, BCD nibbles, bytes, short (16 bits), and long (32 bits) words
(Floating-point coprocessors 68881/2 available)
II—DATA-MOVEMENT INSTRUCTIONS
Five basic address modes are register direct, register indirect, immediate, absolute, and program-counter relative. To these modes can be added postincrementing, predecrementing, offsetting, and indexing
Can use eight 32-bit address registers as indexers or stack pointers. The eight 32-bit data registers can also serve as indexers
III—PROGRAM-MANIPULATION INSTR
Branch and jump to subroutine. Branch conditionally
Link and unlink instructions invoking one address register as frame pointer (used to establish temporary local environments in structured programming)
Seven levels of priority interrupts, including nonmaskable, with 256 possible interrupt vectors
IV—PROGRAM-STATUS-MANIP INSTR
16-bit status register is software accessible
Sophisticated trap operations help user debug programs
Trace mode
V—SYSTEM-CONTROL INSTR
Privileged instructions for operating systems and multiprocessor communication

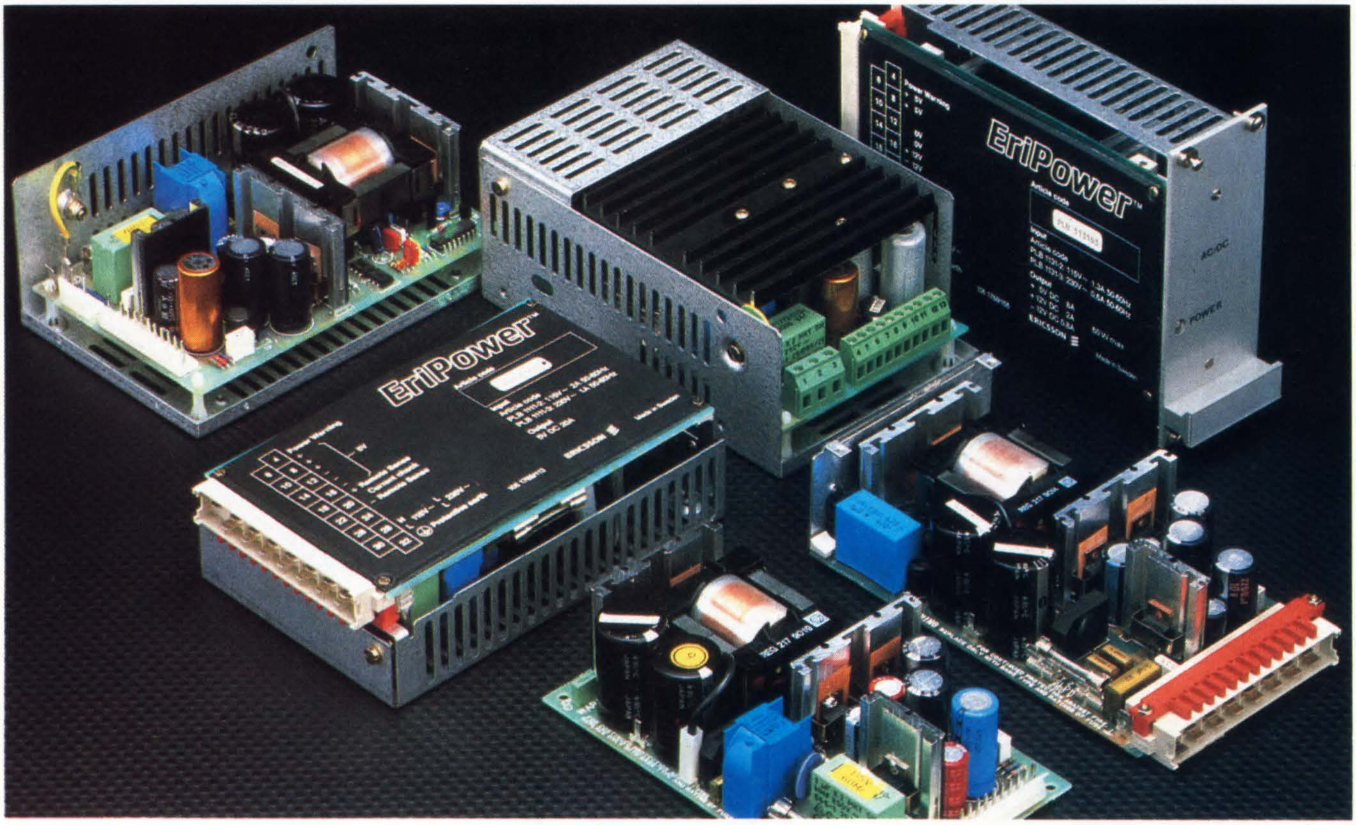
Specification summary: 68020: full 32-bit CPU version of the 68000 family that's object-code compatible with all members. Has 16 32-bit general-purpose data and address registers, 32-bit ALU with barrel shifter, and 32-bit data bus. Also has full 32-bit address bus that can reach 4G bytes of direct linear external memory. Supports instruction-continuation-type virtual memory. Has 256-byte instruction cache on chip and 3-stage pipelining. At 25-MHz maximum clock, executes 5 MIPS. For tight inner loops with so few instructions that they can be contained in cache, and when data can be contained in registers, will operate at burst modes to 12 MIPS. With 68881, it can run at 1.25M Whetstones. Has 18 addressing modes and instructions to support structured high-level languages and sophisticated operating systems. Fabricated in 1.5-μm CMOS with 1.5W power dissipation and packaged in 114-pin grid array. 68030 is similar to 68020 but also has data cache and incorporates 68851 MMU. It will run at 20 to 30 MHz and have 2× 68020 performance at systems level. It is fabricated in 1.2-μm CMOS (with planned shrinkage to 1.1 μm). Packaged in 128-pin grid array.

HARDWARE — SUPPORT — SOFTWARE

HDS-300 hardware/software development station ($15k to $20k) provides real-time emulation of 68000 family μPs with bus-state-analyzer support and source-level debugging. MEX68KECB educational computer board is based on 68000. VM04 is a 68020-based 32-bit Versamodule interconnected within a target system using the 32-bit, asynchronous, Versabus interconnect standard. VME130 is a 68020-based, 32-bit VME bus module using Eurocard mechanical format.
From third parties: Family is widely supported by makers of universal μP development systems such as Applied Microsystems (Redmond, WA). Also, the VME Bus system architecture is used in a broad range of applications with more than 150 independent suppliers of compatible products.

VersaDOS real-time operating system, system V/68 operating system, CP/M-68K operating system, concurrent DOS-68K operating system, and VRTX real-time operating system ($6775 from Hunter Systems). Unix support from Motorola includes direct ports of Unix V, AT&T. X assembler for Exormacs and VME/10, X-C compiler VME/10 and Exormacs for VAX/780 are available.
From third parties: Supplier has catalog listing the considerable outside support for family. New type of support is software to allow 68000 to run MS-DOS (8086) programs: by emulation from Phoenix (Norwood, MA) and by Insignia (London, UK, but with offices in San Francisco); and by binary translation from Hunter Systems (Palo Alto, CA). The latter's package, XDOS ($600), uses a binary compilation approach to generate disks that will run at competitive speeds on 68000 μPs.

These six power supplies are all the same



They're all reliable, with an MTBF of over 300,000 hours. They're all very compact and between 78% and 85% efficient. And, they all meet internationally recognized standards including VDE, IEC, UL, CSA, BS and FCC with respect to safety and RFI.

The differences you see are purely in mechanical construction. The options mean there's a PLB series AC/DC power supply to suit almost every application, whether you need rack or chassis mounting.

These new 60 to 100 Watt SMPS use highly developed flyback technology to minimize component count and maximize efficiency. As a result, they're up to 50% smaller than comparable power supplies.

You can choose from single, dual or triple output versions and all units are user selectable 115/230 VAC. The output voltages, in combinations of ±5, ±12, ±15, 24 or 48 VDC, can be adjusted by ±5% with a potentiometer on the PCB. Standard features include comprehensive protection circuitry, together with a power warning signal.

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In short, the PLB is smaller, more efficient, more reliable and more flexible than other power supplies in its class. But then, you would never expect anything less from Ericsson, would you?

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Ericsson Components AB
Power Products, S-164 81 Stockholm, Sweden
Tel: +46 8 757 4011
Telex: 10948 POWERI S
Fax: +46 8 757 4884

ERICSSON

CIRCLE NO 168

SERIES 32000

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

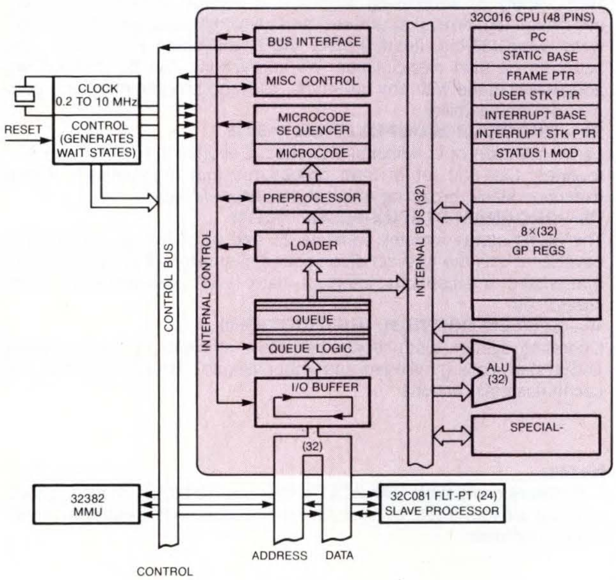
AVAILABILITY: Now for all older NMOS and some CMOS replacements for NMOS parts. The new CMOS 32532 is available now.
COST: In 100 qty, from $1 to $975 (see table).
SECOND SOURCE: None.

Description: A 32-bit µP family in which various models bring out different-sized address and data buses. The fully 32-bit core processor has acquired reputation even among competitors for being "elegant" in its symmetry: that is, its instructions and addressing apply regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It also has reputation for needing less memory space for programs. These software virtues should apply to all family members as strict code compatibiltiy across line. Family is intended to match the needs of operating systems like Unix and to have big-computer features expected of 32-bit systems, such as demand-paged virtual memory, protection of operating system from users, and protection of one user from another user.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

Status: National says that because all its 32XXX family members are full 32-bit internally, those members with 8-and 32-bit external data buses should also be included, which would bring the total up to 700,000 units or roughly on par with what Motorola and Intel are claiming for their 68020 and 80386. What seems critical now is how well the new 32532 is received. It appears to be the ultimate CISC machine (for now), and if it can run at the promised 30 MHz and deliver the promised 10-MIPS sustained performance, it should be attractive for multiprocessor Unix systems (whether in reprogrammable or embedded applications).

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. Floating-point chip (NS32580) is example of slave-type processors that National is using to extend CPU. These processors will be integrated on CPU when VLSI technology permits; they are transparent to programmer and recognize op codes not used by CPU.
2. Advanced features include demand-paged virtual memory, position-independent ROM code and multiprocessing. Latest 32532 has instruction and data caching sufficiently sophisticated to handle multiple-processor situations. Supplier claims relaxed memory-access specifications, even at 30 MHz.

I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals and bit manipulation throughout memory space and CPU registers
II—DATA-MOVEMENT INSTRUCTIONS
Intelligent string operations and bit-field handling allow efficient movements
III—PROGRAM-MANIPULATION INSTR
Stack- and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in slave processors and MMU as well as in CPU, with both privileged and user access

Specification summary: 32-bit "maxi-mini"-type pipelined architecture implemented in multichip NMOS VLSI. Uniform addressing of up to 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, and 32 bits, etc) and all register and memory locations. Performance of family ranges from ¾ MIPS to 10 MIPS (sustained). The top-of-line Model 32532, when running at maximum 30-MHz clock, has a peak performance of 15 MIPS and a Dhrystone benchmark of 16.3k. It has 4-stage overlapping execution pipeline that includes instruction prefetch and branch prediction. It has parallel address and data units, each with own buses and 32-bit ALU. Separate caches for instruction and data: the instruction cache is 1k bytes (direct mapped); the data cache is 1k bytes, 2-way set associative. On-chip demand-paged virtual MMU with 64-entry associative translation look-aside buffer. Fabricated in 1.5-µm double-metal CMOS. Packages range from 48-pin DIP for 320008 to 175-pin pin-grid array for 532. LCC and PLCC packages available for some models.

PART NO	DESCRIPTION	BUS WIDTH INTERNAL	BUS WIDTH EXTERNAL ADDR	BUS WIDTH EXTERNAL DATA	TECHNOLOGY	AVAILABILITY	COST (MHz) (100 QTY)
32008	CPU	32	24	8	CMOS	NOW	$15 (10)
32C016	CPU	32	24	16	CMOS	NOW	$49 (10)
32C032	CPU	32	24	32	CMOS	NOW	$59 (10)
32332	CPU	32	32	32	CMOS	NOW	$110 (15)
32532	CPU	32	32	32	CMOS	NOW	$750 (20) $975 (30)
32382	MMU	—	32	32	NMOS	NOW	$120 (15)
32081	FPU	64	—	16	CMOS	NOW	$69 (15)
32381	FPU	64	—	32	CMOS	NOW	$399 (20) $599 (30)
32580	FPU	64	—	32	CMOS	NOW	$249 (20) $325 (30)

HARDWARE — SUPPORT — SOFTWARE

From National: SYS32/20 that converts IBM PC XT/AT into a Series 32000 development tool (from $3500). Splice in-system emulation covers family µPs up to 32332 with support for 32532 on way. Development/evaluation boards based on 32016, 32032 and 32332 are also available from National and from other suppliers (contact National for list) with prices from $532 to $9900.
From others: PC plug-in board with 32016 or 32032 and memory ($2000 to $3000) that allows running Unix from Opus Systems (Cupertino, CA). PC-based logic-analysis workstation by Northwest Instrument Systems (Beaverton, OR).

From National: Series 32000 Software Catalog is guide to available software from third-party vendors. It lists compilers for C, Pascal, Fortran, Cobol, Modula-2, Ada, etc. Supplier says its GNX (Genix Native and Cross) languages and tools, and its optimizing compilers can increase performance and code density as much as 2×. Operating systems include supplier's Genix V.3.1 derived from AT&T System V, release 3.1.
From others: Software-analysis workstation from Northwest Instrument Systems (Beaverton, OR). Software coprocessor from Phoenix Technologies (Norwood, MA) that allows family to run MS-DOS 8086 programs. VRTX real-time multitasking operating system from Ready Systems (Palo Alto, CA); and MTOS-UX from Industrial Programming Inc (Jericho, NY).

WE32 FAMILY — 32-BIT CMOS

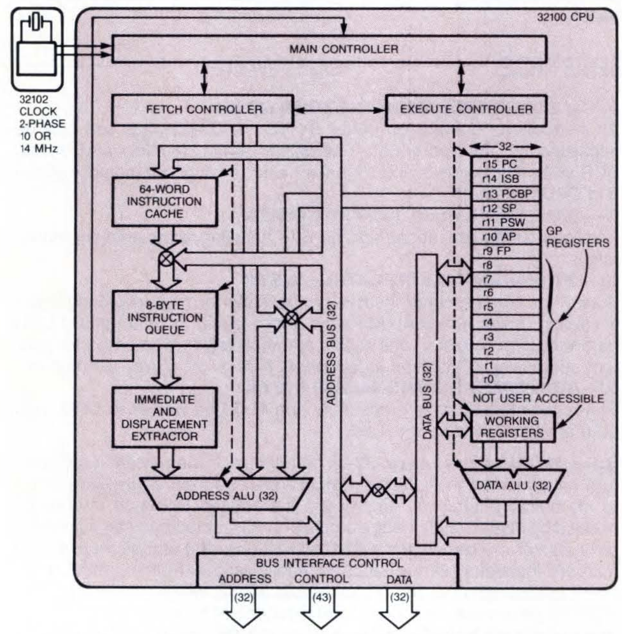
AVAILABILITY: Now for both WE32100 and WE32200 (see table for speeds).
COST: $110 for 10-MHz 32100 CPU, 1k qty (see table for others).
SECOND SOURCE: Zilog for 32100.

Description: CMOS chip sets for building top-of-the-line, minicomputer-like computing systems. Provided with depth of Unix operating system support, so suited to multiuser/multitasking applications.

AT&T Technologies Inc
Dept LT
555 Union Blvd
Allentown, PA 18103
Phone (800) 372-2447

Status: These chip sets have an advantage: AT&T is developing its newest versions of Unix on them. But so far there has been no indication that they have any marked acceptance for Unix applications compared with any of the many other 32-bit μPs. Meanwhile, AT&T's internal use of the chips for its 3B computers (in the "tens of thousands") plus other uses where the chips are embedded in AT&T telecomm equipment and in commercial applications have given the family the start down the production learning curve that is so important for all large 32-bit chips.

HARDWARE — CHARACTERISTICS — SOFTWARE



PART NUMBER	TYPE	DESCRIPTION	SPEED (MHz)	PACKAGE PINS	AVAIL-ABILITY	COST (1k QTY)
WE32100	CPU	32-BIT MICROPROCESSOR	10 14 18	125	NOW NOW NOW	$110
WE32101	MMU	MEMORY-MANAGEMENT UNIT	10 14 18	125	NOW NOW NOW	$105
WE32102	CLOCK	2-PHASE CLOCK	10 14 18	16	NOW NOW	$27
WE32103	DRAMC	DYNAMIC-RAM CONTROLLER	10 14 18	125	NOW NOW NOW	$50
WE32104	DMAC	DIRECT-MEMORY-ACCESS CONTROLLER	10 14 18	133	NOW NOW NOW	$100
WE32106	MAU	MATH-ACCELERATION UNIT	10 14 18	125	NOW NOW NOW	$110
WE32200	CPU	32-BIT MICROPROCESSOR	20 24 28	133	NOW NOW NOW	$250
WE32201	MMU	MEMORY-MANAGEMENT UNIT	20 24 28	133	NOW NOW NOW	$275
WE32204	DMAC	DIRECT-MEMORY-ACCESS CONTROLLER	20 24 28	133	1Q'88	NA
WE32206	MAU	MATH-ACCELERATION UNIT	20 24 28	125	NOW NOW NOW	$225

I—DATA-MANIPULATION INSTRUCTIONS
Fairly complete arithmetic, logical, and bit-manipulation instructions (including 2- and 3-operand instructions)
II—DATA-MOVEMENT INSTRUCTIONS
Wide variety of addressing modes that support high-level language constructs (eg, arrays, structures) and allow manipulation of byte, half-word, word (32-bit), floating-point, BCD, and string data types. Also supports bit field manipulation. All instructions can be used in any addressing mode with any data type, allowing programming and compiler design flexibility
III—PROGRAM-MANIPULATION INSTR
Large selection of conditional branches. Conditional returns from subroutines. Call and return from procedures that automatically update execution stack, providing efficient procedure linkage
IV—PROGRAM-STATUS-MANIP INSTR
The 32-bit status register contains 26 bits of status information that covers not only the ALU condition codes of smaller μPs but information that relates to exceptions, interrupt mask level, execution level, cache control, etc
V—SYSTEM-CONTROL INSTRUCTIONS
Operating system instructions that allow efficient process switching and system calls (privileged and nonprivileged). Breakpoint, trap, and cache flush instructions

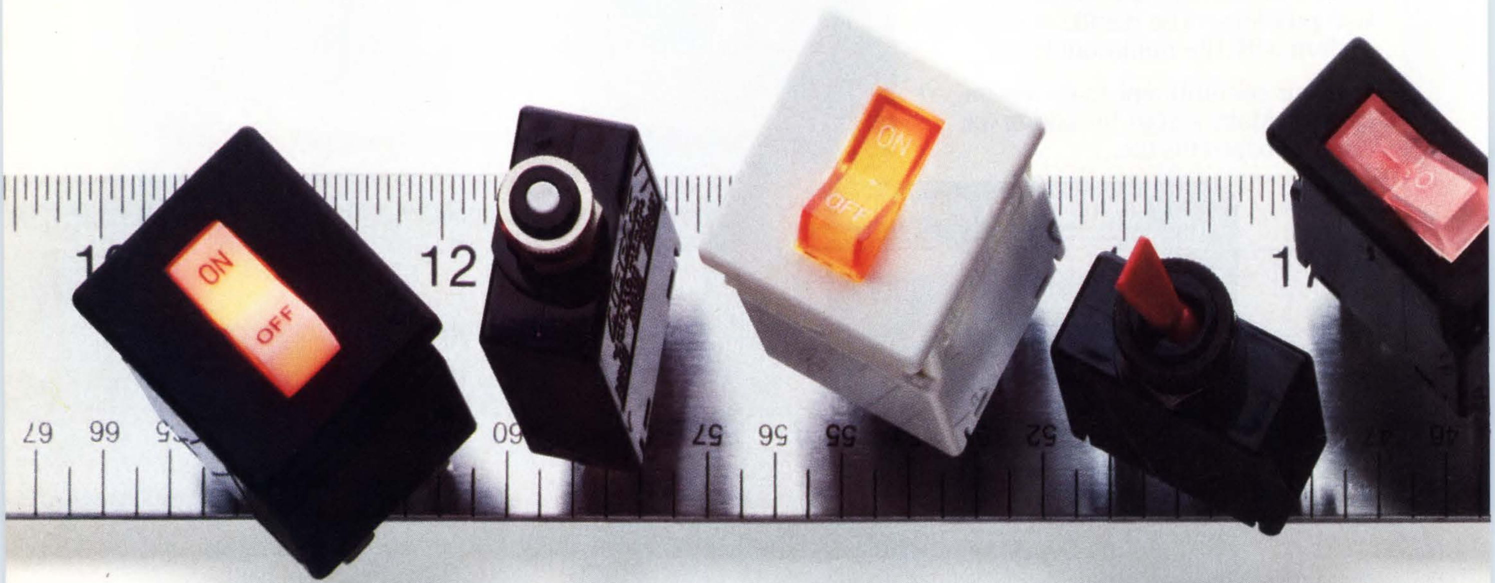
Notes:
1. Software compatible with AT&T's previous 32-bit μP, the WE 32000.
2. There are four levels of execution privilege: kernel, executive, supervisory, and user.

Specification summary: Upwardly compatible chip sets (see table) intended for large-memory, minicomputer-like 32-bit systems. The 32100 CPU features separate addressing and data execution sections each with 32-bit-wide bus. A 64-word instruction cache followed by an 8-byte instruction queue control a 3-deep pipelined execution unit. Performance can be maintained at 3 to 4 MIPS. The 32100 CPU is augmented by four VLSI support chips (see table): The 32101 MMU provides support for 4G bytes of virtual memory and incorporates both demand-paged and demand-segmented approaches. The 32103 DRAMC addresses 16M bytes of dynamic RAM, supporting the newest 1M-bit devices and incorporates refresh control, etc. The 32104 DMAC handles 32-bit address generation for rapid memory-to-memory data transfers (14.5M bytes/sec) and has additional 8-bit-wide bus for efficient transfers to slower peripherals. The 32106 MAU coprocessor executes IEEE floating-point math, allowing the 32100 system to achieve 1.4M Whetstones/sec. Chip set is fabricated in 1.5-μm twin-tub CMOS (32100 CPU consumes 0.8W) and are in ceramic grid array packages (see table).
The 32200 enhanced chip set delivers up to 8 MIPS when operating in the 20- to 30-MHz range. CPU has 32 registers and 256-byte instruction cache. MMU has 4k-byte data cache plus bus watcher. MAU provides up to 3.9M Whetstones.

HARDWARE — SUPPORT — SOFTWARE

WE321DS development system that includes WE321AP analysis pod ($22,500 for 10-MHz) in-circuit emulation of 32100 and 32101. 14 MHz also available. WE321/22 device monitors provide signal observation of high-speed systems.
WE321EB evaluation board ($5500 at 10 MHz, $6500 at 14 MHz) with 32101 MMU and 32106 math accelerator.
WE321SB single-board computer with VME Bus that is compatible with AT&T 3B computers, giving users access to one of the largest off-the-shelf collections of Unix software.

WE321SG software-generation programs run on host Unix systems. Includes C compiler, assembler, linking editor, and optimizer. Prices range from $750 to $1250. Also compilers for Fortran, Cobol, Lisp, Basic, and Ada. Over 1000 end-user programs, including Informix, Crystal Writer, and Multiplan have been developed for the chip set, according to AT&T.
AT&T provides a range of Unix licensing arrangements from $60 for binary sublicense for a 1- or 2-user situation to $72,000 for an initial license for source code (substantial discounts for educational institutions).



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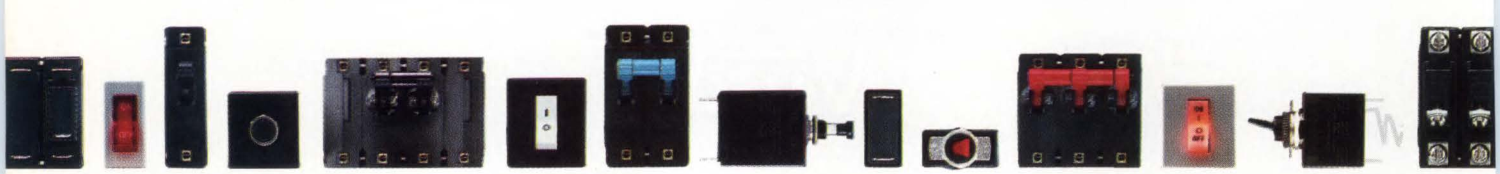

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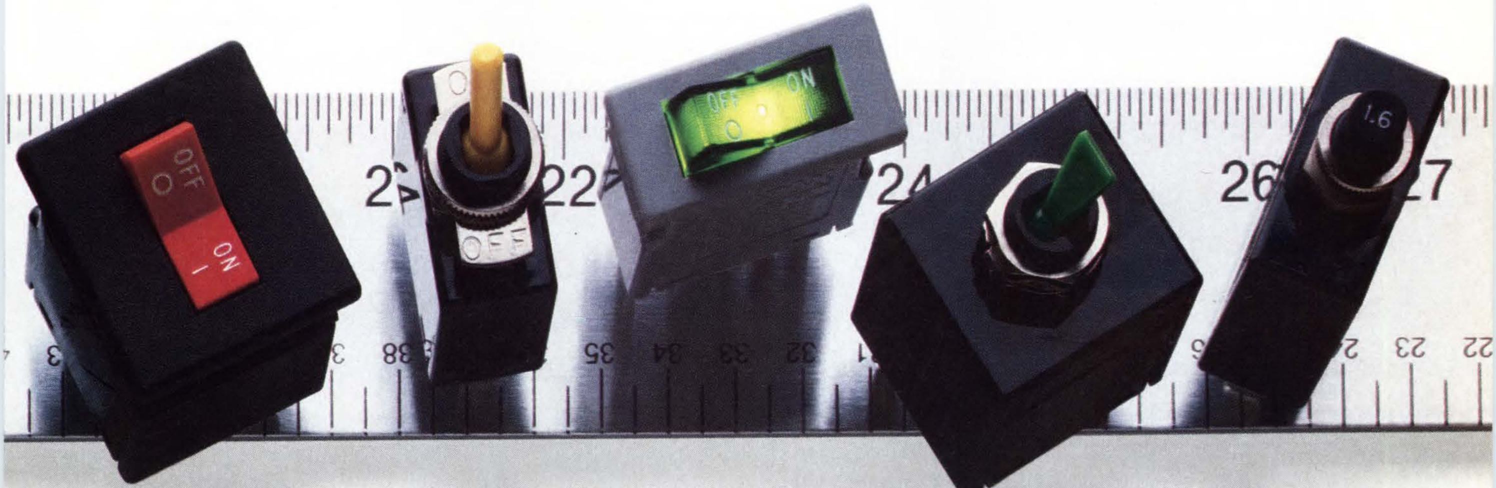

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CIRCLE NO 171

CLIPPER

32-BIT CMOS

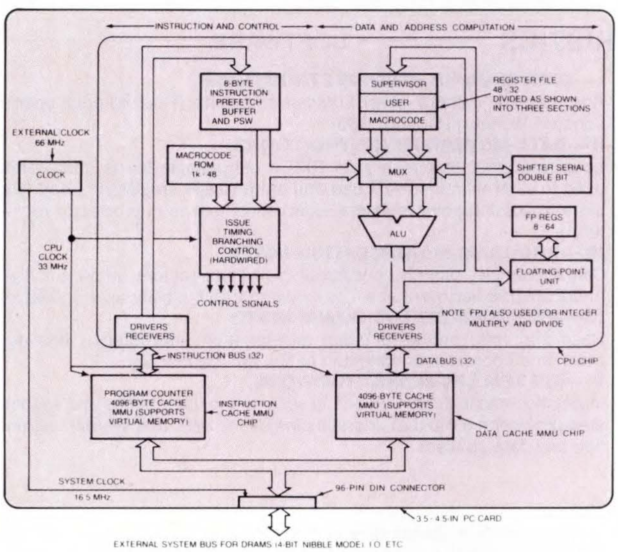
AVAILABILITY: Now for C100. Samples of C300 available now, production in late '88.
COST: For C100 module (33 MHz) with clock, $715 (1000); 30 MHz C100 chip set $549 (1000); and C300 module (50 MHz) $1215 (1000).
SECOND SOURCE: None announced.

Intergraph Corp
Advanced Processor Div
2400 Geng Rd
Palo Alto, CA 94303
Phone (415) 494-8800

Description: CMOS RISC-based µP has a dual-bus Harvard architecture. Three-chip set includes a CPU that incorporates a floating-point math unit (FPU) and two cache/MMU chips: one for instructions and one for data. Because the dual caches are large (for µPs), the Clipper is said to achieve 90% hit rates and sustain a 5 to 17 MIPS performance with peak performance reaching 50 MIPS.

Status: The Clipper C100 has been in production since early 1987, with 18,000 units shipped through July 1988. The manufacturer claims monthly shipments exceed 1000 units. The C100 is now available as a 3-chip set in PGA packages, and the C300 µP is now available in sample quantities. The Advanced Processor Div, part of Intergraph Corp (Huntsville, AL), enters its second year of operation, and Intergraph says it wholeheartedly backs Clipper's efforts in the merchant OEM market.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware Notes:
1. Clipper consists of three CMOS chips. The original chip set, C100, with its 33-MHz clock, is shown in diagram. The forthcoming C300 is a plug-in upgrade that runs at 50-MHz clock.
2. The CPU chip has RISC-like ALU plus a CISC-like macrocode ROM and floating-point unit. The other two chips are identical pin-programmable cache/MMU chips, so one can be used for instruction caching and the other for data caching. The instruction cache carries the CPU's PC (instruction program counter). The 4096-byte capacity of each cache (large for µPs) plus the sophisticated caching control (2-way set associative) gives the Clipper a high hit ratio (over 90%), a key factor for sustained execution speed.
3. Each cache supports virtual memory via the on-chip MMU. The caches (especially the data cache) operate on a physical memory basis, so less flushing is needed. The C100 requires 135-nsec memory devices, and the C300 requires 90-nsec memory devices.
4. Sophisticated pipelining is used on CPU, but with provision for bypassing so that an instruction can obtain the result of a preceding instruction without delay.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, and divide (32-bit integer and 32- and 64-bit IEEE floating point done in floating-point unit), floating-point converts, negate, compare, logicals, including AND, OR, EXCL OR, and NOT
32- and 64-bit shifts and rotates, including floating point
II—DATA-MOVEMENT INSTRUCTIONS
Architecture favors register-to-register operations and avoids operations on memory other than register-to-memory movements. There are nine addressing modes, including absolute, relative (with and without displacements), relative indexed, and PC indexed. Despite streamlined instruction set, architecture provides efficient string moves, because execution control is switched over to macrocode ROM
III-PROGRAM-MANIPULATION INSTR
Macrocode ROM is used for context switching save and restore instructions that support entry and exit from interrupt and trap routines. Push, Pop, supervisor, and user stacks (any register can be used as pointer)
IV—PROGRAM-STATUS-MANIP INSTR
Two status words, a user-program status word and a privileged system status word (which can only be written in supervisory mode)
V—SPECIAL INSTRUCTIONS
Supervisory mode commands. Hardware supports 18 hardware traps and 128 supervisory calls. Software semiphores are supported for multitasking

Software Notes:
1. Clipper's 168 instructions are a balance between 1-cyle RISC and multicycle CISC commands. The RISC takes care of the simpler, most frequently used instructions. The CISC macrocode takes care of complex instructions such as floating/integer conversion, character-string manipulation, save and restore registers, and trap/interrupt entry and return sequences.
2. C100 and C300 instructions are compatible.

Specification summary: Modified RISC-type architecture in which the basic frugal RISC instruction set is supplemented with boost from microcode ROM. The bus-bandwidth bottleneck is solved by having separate buses for instruction and data and putting a cache/MMU chip on each bus. Putting the caches on separate chips allows them to be large enough to generate hit rates over 90%. Partitioning also allows IEEE 64-bit floating point to be incorporated on CPU chip so there is no off-chip delay (as when going to an external coprocessor). There is no need for CPU to have a separate multiply divide hardware because these operations can be done in the floating-point unit. Performance is 6 to 7 MIPS average for C100 and more than 13 MIPS for C300. For user convenience, the chips are sold mounted with clock on a 3.5×4.5-in. multilayer pc card with 96-pin DIN connector. C100 chips are available separately, too.

HARDWARE — SUPPORT — SOFTWARE

The Clipper Module card integrates the three Clipper chips into a functioning CPU. It provides the clock and PC wiring and a 96-pin DIN connector. User must provide the bus buffers externally.
Intergraph supplies development systems that provide a 33-MHz Clipper CPU, 8M bytes of RAM, 156M bytes of hard-disk storage, and an Ethernet interface. Software includes Clix, based on Unix System V; a C compiler, a loader/debugger; and utilities.

Clipper cross-support package that runs on VAX ($8000) and MicroVAX-II ($6000). Consists of three elements: standard Unix System V development tools; optimized C, Fortran, and Pascal compilers, Basic interpreter, assembler, linker, and debugger; and a complete software simulator. There is also Clipper's Clix, a Unix V 3.0 operating system. Third parties are preparing software that will allow Clipper to run MS-DOS 8086 programs via software emulation from Insignia (UK) and via binary code conversion from Hunter Systems (Palo Alto, CA).

SPARC RISC

32-BIT CMOS

AVAILABILITY: From Fujitsu: now for prototype quantities of MB86901, production quantities by 9/88. From Cypress: 7C601 is available now. From BIT: early '89 for bipolar ECL BIT SPARC chip. From LSI Logic: late '88.
COST: For Fujitsu: $325 (5000). For Cypress: $634 (100). Prices for LSI Logic and BIT parts not yet determined.
SECOND SOURCE: Fujitsu, Cypress, LSI Logic, and BIT SPARC µPs will be different and probably not hardware compatible. But they must all run SPARC software as defined by Sun Microsystems Inc (Mountain View, CA).
CORE: Fujitsu has made a start in this direction with a gate array. LSI Logic will also offer RISC elements in its ASIC library.

Description: Goal is to set a high-performance RISC-type software standard while allowing maximum hardware flexibility so that multiple vendors can vie for present and future maximum performance. Sun Microsystems defined SPARC at instruction-set and programmer's model level and then entered into entirely separate joint agreements with silicon vendors with the intent of reaching 100-MIPS performance by 1990. Meanwhile, Sun provides development hardware and software support via its workstations.

Fujitsu Microelectronics Inc
3330 Scott Blvd
Santa Clara, CA 95054
Phone (408) 727-1700

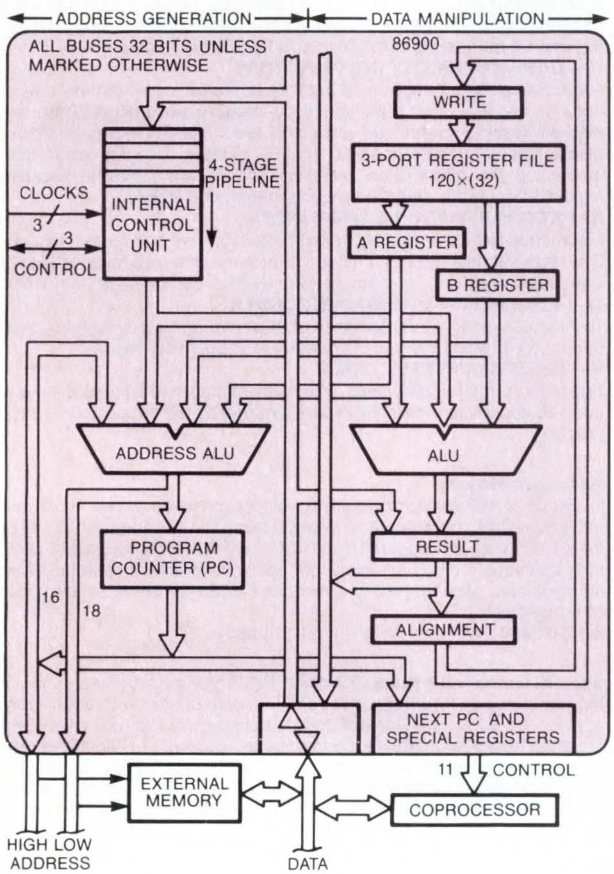
Cypress Semiconductor
3901 N First St
San Jose, CA 95134
Phone (408) 943-2852

Bipolar Integrated Technology (BIT)
Box 4750
Beaverton, OR 97076
Phone (503) 629-5490

LSI Logic Corp
1551 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 433-8000

Status: Here is another instance where an OEM has developed a µP for its own strategic needs and then let semiconductor vendors openly market the resulting device. A twist in this case is that the OEM, Sun Microsystems (Mountain View, CA), is also a leading workstation vendor and is able to back up the µP with all-important development support. The motivation of all concerned is to demonstrate and promise such dramatic performance/price progress that there's sufficient OEM and third-party following to make SPARC a "winner" in the current high-MIPS sweepstakes. As with some other RISCs, SPARC lacks full multiply (only multiply step) and thus may need help of coprocessor.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Diagram is for Fujitsu 86901. Fujitsu also supplies gate-array companion chip 86910 that provides interface to Weitek 1164/65 floating-point chip set.
2. Cypress will implement its SPARC in full-custom CMOS using Cypress's 0.8-µm 2-layer metal process. The chip set will include integer, floating point, and cache "solutions."
3. BIT will implement its SPARC in bipolar ECL, and will provide companion FPU chips.
4. SPARC stands for scalable processor architecture.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step). Logicals and shifts. (Floating-point operations via Weitek 1164 and 1165)
II—DATA-MOVEMENT INSTRUCTIONS
Load and store to memory (in RISCs only simple loads and stores used to external memory). Load and store to CPU registers. Load and store to floating-point registers. Load and Store to coprocessor registers
III—PROGRAM-MANIPULATION INSTR
Call subroutine, branch conditional, save and restore, jump and link (there are 128 hardware and 128 software traps, mostly user definable)
IV—PROGRAM-STATUS-MANIP INSTR
Read and write processor state register (note that integer, floating-point, and coprocessor condition codes are mentioned)
V—SYSTEM LEVEL INSTRUCTIONS
Instruction-cache flush. Can set up system and user modes and associated protection (note that address pins define user and system instruction and data spaces)

Notes:
1. There are four stages (five in BIT µP) of pipelining, and it is up to optimizing compiler to prevent pipeline breaks by inserting a delay instruction before branch instructions.
2. Overlapped CPU register file windows are said to allow faster contact switching than if usual stack were used.

Specification summary: 32-bit µP family that is standardized at software level but open at hardware level for whatever implementation gives a competitive performance/price ratio. Architecturally it follows the RISC philosophy of minimum instructions (Fujitsu shows about 107), most of which execute in single cycles (1.3 to 1.7 clocks per instruction). It has a fairly large number of on-chip registers (120) to hold data being processesd for rapid access, which also permits the fixed-length instructions to carry the two source and one destination addresses needed for single-cycle operations (register file has 3-port structure). The on-chip registers are partitioned into seven 24-register groups that are overlapped at edges so that parameters can be easily passed between them. There are also eight global registers. Can address 4G bytes of direct address space and 256 pages of 4G-byte indirect space. Addressing supports various user-defined cache configurations. Fujitsu 86901 has separate coprocessor port that couples tightly to Weitek 1164/65 FP chips. Performance ranges from 10 MIPS sustained for Fujitsu 86900 at 16.67 MHz, to 20 MIPS expected of Cypress chip set, to projections of 50 to 100 MIPS by 1990. Both semicustom (gate arrays) and full-custom design approaches are being used. Strategy is to aggressively upgrade performance by frequent redesign in newer technologies as they emerge. (LSI Logic is extending its RISC commitment by also manufacturing the MIPS Computer Systems Inc (Sunnyvale, CA) 32-bit RISC µP and its family of support chips.)

HARDWARE — SUPPORT — SOFTWARE

Silicon vendors refer customers to Sun workstations, indicating that even the older models that use Motorola 68000-family µPs are adequate as Sun maintains software compatibility (obviously the newer models, from Sun-4 onward, which use SPARC, would be ideal).
Evaluation boards from Cypress and Fujitsu. Mizar (Carrollton, TX) expects to offer VME Bus boards for the 86901 in late '88.

Vendors say they'll pass along Sun's optimizing compilers for C, Pascal, and Fortran as well as Sun's Unix operating system. Wind River Systems (Emeryville, CA) will provide a real-time operating system. A SPARC monitor is available from Bradley Forthware (Sunnyvale, CA).

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HEWLETT PACKARD

29000 RISC

32-BIT CMOS

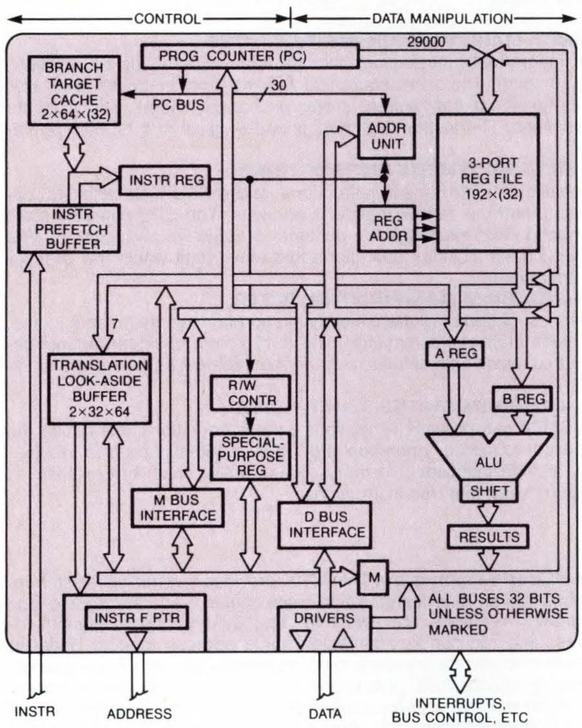
AVAILABILITY: Now for 29000 CPU and 29027 arithmetic accelerator.
COST: In 100-piece lots, $174 for the 29000 (16 MHz) and $422 for the 29027 (16 MHz). Parts are also available in 20-and 25-MHz grades.
SECOND SOURCE: Under negotiation.

Advanced Micro Devices (AMD)
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

Description: State-of-the-art implementation of RISC µP concepts with expected stress on obtaining as close to single-cycle operation as possible (even with branching) and a special emphasis on keeping user's system costs down by bus timing, etc, which allows lower-cost external memories. Note that though first two digits of this µP's designation—"29"—are the same as supplier's previous building-block families (see elsewhere in directory), this 29000 family is the opposite architecturally. The other building-block families are intended for user-defined (microcoded) complex instruction sets, whereas this µP has a regular, fixed and purposely simple instruction set; moreover, it is decoded by logic. Companion compilers are an essential part of family.

Status: AMD has long been conscious of performance tradeoffs in high-end architectures because of its involvement in bit-slice µPs (2900 family), and this first venture into a fixed-instruction-set µP is most interesting. This µP is RISC (reduced-instruction-set computer) based, and is quite the opposite of the microcoded CISC (complex-instruction-set computer) architectures of the bit-slice µPs. It's too early to tell how this µP will fare in the marketplace, but AMD says it is aiming squarely at the embedded-processor market with the 29000. AMD believes competition for the 29000 will come not from existing RISC µPs such as the Clipper and SPARC, but from Motorola's 88000 and RISC products from Intel.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Burst-mode addressing allows use of lower-cost video RAMs to replace more-expensive, high-speed, static CMOS RAMs, with only moderate loss in performance (14 MIPS sustained vs 17 MIPS).
2. There is a coprocessor interface to companion 29027 floating-point chip. The 29027 uses combinatorial logic, so operations take only five 29000 cycles.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step), divide (step)
Logicals, compare, convert floating point (floating point is not currently implemented in hardware but companion floating-point chip 29027 is available)
II—DATA-MOVEMENT INSTRUCTIONS
Register-to-register moves
Load and store to external memory and I/O
III—PROGRAM-MANIPULATION INSTR
Jump, call subroutine, and returns
Branches (with decisions based on Boolean data in general-purpose registers rather than ALU condition codes)
IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition
V—SYSTEM-LEVEL INSTRUCTIONS
Some of the 23 special-purpose registers are for system control, and these are protected and can be set up via software (some also are affected by execution)

Notes:
1. Total of 115 instructions, not all of which are yet implemented in hardware, and only cause traps.
2. Multiply and divide on the 29000 only does one step. The full multiply and divide instruction causes a trap operation at which a compiler can insert a software routine.

Specification summary: 32-bit CPU fashioned after RISC concepts, designed to perform most frequently used, simple instructions in one cycle. Offered with companion compilers intended to take advantage of architectural simplicity and produce code optimized for performance. Also offered with companion floating-point chip, 29027, which in more CISC fashion makes up for crudeness of math instructions (only partial multiplication and division instructions). Features that ensure uninterrupted flow in 29000's 4-stage execution pipeline are single-cycle branching with branch delays and a 512-byte branch-target cache. Main 192-register file has a 3-port configuration so that instruction fields can specify sources for both operands and the destination for the result. 128 of the registers are addressed by a stack pointer that (in conjunction with the compiler) provides a type of "caching" that speeds procedure calling. External memory space is reached by 4G-byte virtual addressing with demand paging. An on-chip 64-entry MMU performs address translation in a single cycle and is flexible so users can choose memory strategy. 25-MHz operating frequency (40-nsec clock period) gives 25-MIPS peak and 17-MIPS sustained performance. Fabricated in 1.2-µm (effective) CMOS with 1.5W power dissipation. Housed in 169-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

The ADAPT29K development and prototyping tool lets you develop hardware and software on a 29000-based system. Debugging and chip-test aids are available in 29000 hardware, some of which are equivalent to having an in-circuit emulator. Can halt and single-step through pipeline. Can jam instructions into instruction register, execute them, and then return to regular code.

AMD supplies a simulator, debugger, resident debugger, and a cross-development package. AMD has contracted with a "leading" compiler source for optimizing compilers for C, Fortran, Pascal, and Ada. Note that there is an intentional symbiotic relationship between 29000 architecture and compilers. For example, compilers have access to internal 29000 operations, such as pipelining, and thus can insert useful instructions at branch delays. They can also weed out redundancies in loops.

88000

32-BIT CMOS

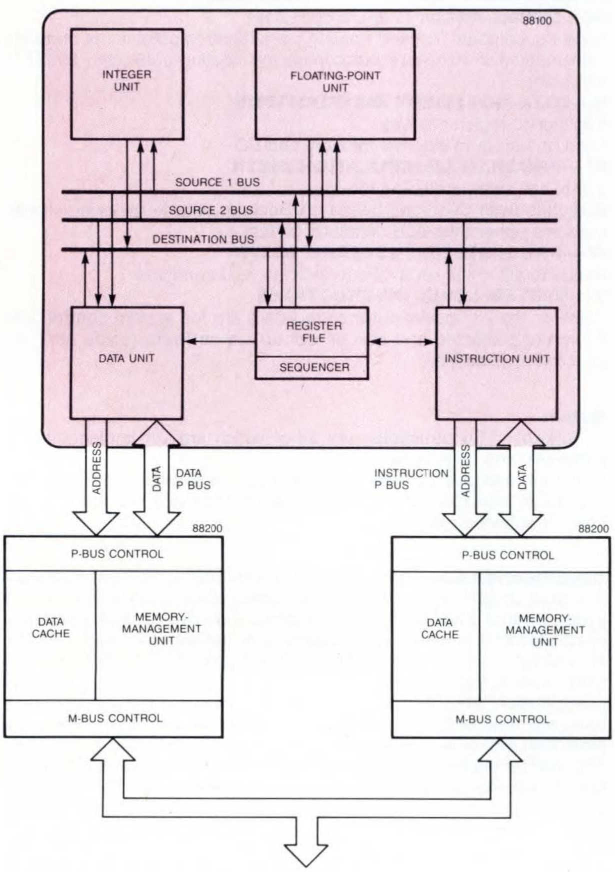
AVAILABILITY: Both the 88100 CPU and the 88200 cache/memory-management unit (CMMU) should be available in late '88. Limited numbers of samples have been available for selected customers during the past months. Motorola and Data General (Westborough, MA) have an agreement to produce the 88000-family chips in ECL.
COST: In 100 to 499 quantities, the 88100 costs $495; the 88200 costs $795.
SECOND SOURCE: None announced.
CORE: Motorola's architecture can incorporate as many as six special-function units (SFUs) into the 88100 chip. Customers can place coprocessors and other circuits in the SFUs.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (800) 441-2477

Description: The 88000 family is Motorola's entry into the reduced-instruction-set computer (RISC) arena. Originally dubbed the 78000, the 88000 family encompasses the 88100—the CPU—and the 88200—the memory-management unit. The 88100 chip supplies full 32-bit registers, data paths, and addresses. Most instructions take only one cycle, or are put in a concurrent execution pipeline in one cycle. The chip also performs standard IEEE-P754 floating-point math operations in one cycle. The corresponding 88200 cache/memory-management unit (CMMU) supports a demand-paged virtual-memory environment. The chip controls two 4G-byte logical address spaces—one for the user and one for the supervisor. The chip's architecture supports multiprocessor operations.

Status: Although it was known for some time that Motorola was undertaking a RISC μP project, the resulting 88000 μP family was finally announced in April '88. Motorola not only unveiled its two chips, but also produced a list of more than 25 companies that have adopted the 88000 μP family or that are developing software for it. Further bolstering the position of the nascent 88000, an independent group of manufacturers has already founded the 88open Consortium Ltd (Stratham, NH) to support and promote the μP family. More than simply a promotional trade group, the consortium aims to develop standards for the 88000 family.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Architecture shown is for the 88100. The CMMUs are shown in block-diagram form.
2. The P bus supplies the interface between the 88100 and either local memory or an 88200 CMMU. The synchronous P bus operates at the same clock rate as the 88100. Peak data rate is 80M bytes/sec.
3. The 88100 includes 32 general-purpose registers.

I—DATA-MANIPULATION INSTRUCTIONS
The integer-math instructions include add, subtract, divide, multiply, and compare. There are equivalent floating-point instructions as well as integer-float conversion, store, exchange, round, and truncate instructions. The instructions also provide logical and bit-field operations

II—DATA-MOVEMENT INSTRUCTIONS
The basic data-movement instructions let the CPU load registers, addresses, and the control register's contents. The CPU can also store information and exchange the contents of registers and memory. The instruction set includes operations that move data within the floating-point math unit

III—PROGRAM-MANIPULATION INSTR
These instructions include conditional and unconditional branch, jump, and subroutine-call commands. The 88100 also provides trap instructions that check bit locations, memory boundaries, and interrupt conditions

IV—PROGRAM-STATUS-MANIP INSTR
The 88100 can process exceptions—those conditions that cause the processor to stop its operation and locate a potential problem. Exceptions include interrupts, memory-access faults, math errors such as divide by zero, and trap instructions

Specification summary: The 88100 provides register-to-register operations for all data-manipulation instructions. Separate source and destination registers are available. The CPU supports register-to-register and register-plus-immediate-value address modes. Because address calculations are quick, memory-access operations are speedy, in keeping with the RISC philosophy. The CPU employs delayed branching, which reduces pipeline delays due to a change in program flow. The 88200 incorporates 16k bytes of cache memory as well as cache-control logic, memory-management logic, and bus-control circuits. Multiple CMMUs can operate in parallel. Both the 88100 and 88200 come packaged in 180-pin PGA packages. The chips operate over the standard 0 to 70°C temperature range.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: The company has announced its Platform-88 ($39,500) for system developers. The computer should be available for shipment now.
From others: Various 88000 hardware is available from Beacon Technologies (Valparaiso, FL); Golden Triangle Computers Inc (San Diego, CA); Integrated Micro Products Ltd (Durham, UK); Tadpole Technology (Cambridge, UK and Dublin, CA); and Tektronix Inc (Beaverton, OR).

From Motorola: The Platform-88 computer will run Motorola's Unix System V.3 as well as other languages and development tools such as an assembler, a code scheduler, and optimizing C and Fortran compliers.
From others: Support for the 88000 is available from Absoft Corp (Auburn Hills, MI); Diab Systems Inc (Foster City, CA); Green Hills Software, Inc (Glendale, CA); Informix Software Inc (Menlo Park, CA); Insignia Solutions Inc (Sunnyvale, CA); Software Components Group (Santa Clara, CA); and many others.

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John R. Belden
Marketing Manager
Glassman High Voltage, Inc.

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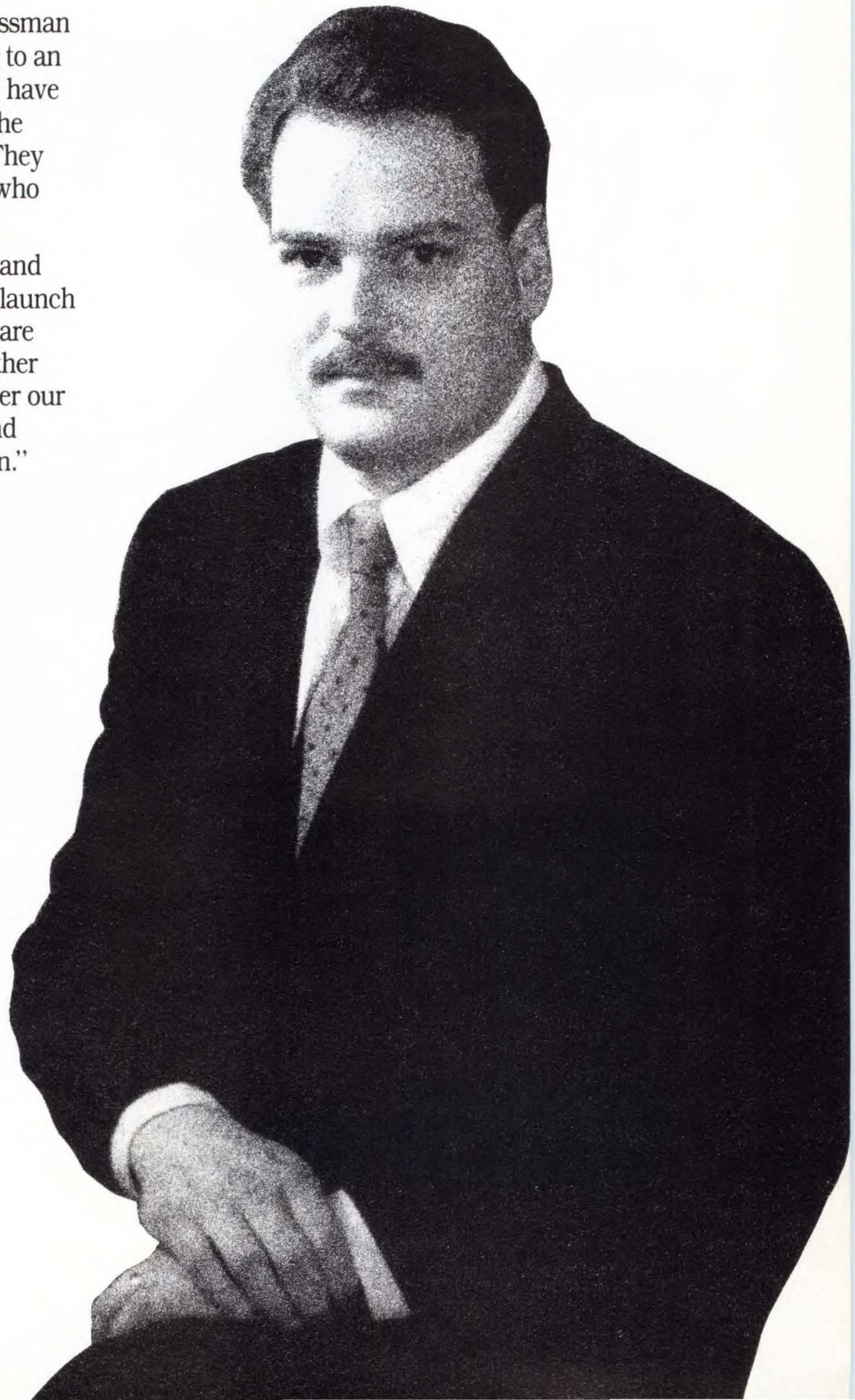

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CIRCLE NO 176

80960 — 32-BIT CMOS

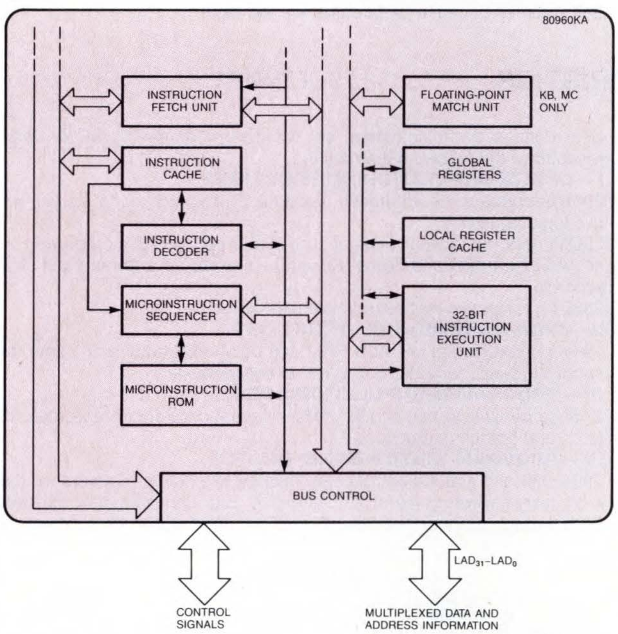
AVAILABILITY: Now for 80960KB; later in '88 for MC and KA versions.
COST: $333 for 80960KB-16; $390 for 80960KB-20; $174 for 80960KA-16; $213 for 80960KA-20 (all in 100s).
SECOND SOURCE: None.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Description: The 80960 is Intel's 32-bit family of μP chips that has been designed specifically for embedded-control applications. There are three upward-compatible versions of the RISC-based architecture. The family includes the basic 80960KA core version, the 80960KB which includes an on-chip floating-point math unit, and the 80960MC. The latter is a military version of the chip, which supplies multiprocessing and Ada-tasking support. The '960 family furnishes a large set of registers, a register cache, an instruction cache, and an interrupt controller, among other features.

Status: Unlike many new μPs, the 80960 was available at the time of its announcement in April '88. Currently, both 16- and 20-MHz versions are available. The MC version is available in sample quantities, and the chip is undergoing MIL-STD-883B qualifications now. Samples of the KA chip that run at higher clock speeds are expected by the end of '88. Intel will probably announce new '960-family chips in '89 and '90.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Unlike other RISC processors, the '960 provides only one data bus for instructions and data. The bus multiplexes address and data information.
2. The basic '960 chip includes 16 32-bit global registers and 16 32-bit local registers. The stack requires one global and three local registers for housekeeping operations.
3. The floating-point math unit (80960KB) operates from four 80-bit registers.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic: add, subtract, multiply, divide, remainder, modulo, shift
Bit and bit-field instructions, including complex tests on bits
Full set of single-cycle Boolean operations
Decimal move, add, and subtract with carry
The KB/MC versions include full IEEE-P754 floating-point math operations
II—DATA-MOVEMENT INSTRUCTIONS
Loan-and-store between memory, movement between registers. Eight addressing modes, including direct, immediate, and register indirect
III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional compare and branch instructions. Call and supervisor-call instructions. One return instruction. Optional branch-and-link. MC version includes multitasking, memory-management, interprocessor-communication, and multiprocessing instructions
IV—PROGRAM-STATUS-MANIP INSTR
Modify arithmetic controls. Flush registers. Built-in trace and debug support

Specification summary: Register set includes 32-bit global and local registers. The chip provides caching for four sets of local registers. Direct mapped, 512-byte instruction cache is automatically filled by intelligent bus-control logic. Register scoreboarding allows bus operations and instruction executions to proceed in parallel. The built-in interrupt controller handles as many as 256 vectors within 32 priority levels. Interrupts arise from four external signal lines or from an external 8259A controller chip. Memory is located in a 4G-byte linear address space, and data transfers take place at a burst rate that reaches over 50M bytes/sec. The floating-point math unit supports standard IEEE-P754 math operations.

HARDWARE — SUPPORT — SOFTWARE

From Intel: EVA960 PC/AT-based unit ($6000) available now for developing and testing programs. ICE-960 in-circuit emulator hosted on an IBM PC/AT will be available in late '88 as will an 80960KB-based prototyping board.

From Intel: C compiler with ANSI extensions, assembler, and utilities are available now for an IBM PC/AT or compatible computer. Software for other host computers is expected late in '88. An Ada compiler is expected in '89. A real-time kernel will also be available in '89.
From others: Ada-to-C translator from ICC (Irvine, CA); VRTX real-time executive from Ready Systems (Palo Alto, CA); and hardware modeling program from Mentor Graphics (Beaverton, OR), among others.

2900, 29C00, 29G00 BIT SLICE

4-BIT×N, 16-BIT, 32-BIT; BIPOLAR, CMOS, AND GaAs

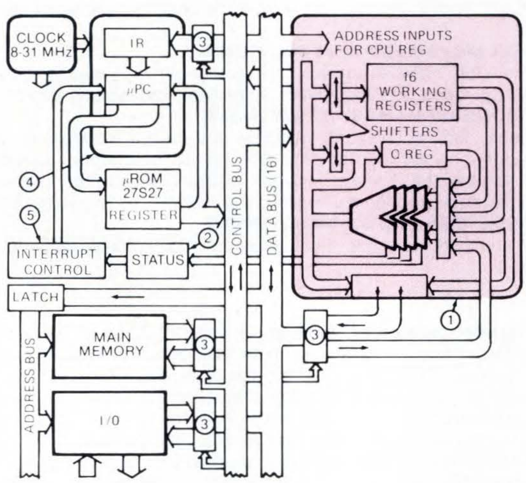
AVAILABILITY: Now for older, original bipolar parts and many new CMOS variations on 2900 theme. Varies for latest highest speed and widest data word versions.
COST: $6 for 2901A/B/C in 100 qty; $20 for 2903A in 100 qty. See table for others. Prices for CMOS similar.
SECOND SOURCE: None for original bipolar 2900. For new CMOS versions: IDT, Cypress, Wafer Scale Integration, Logic Devices, and others. For GaAs versions: Vitesse (29G01) and possibly McDonnell Douglas.
CORE: Most of the sources for CMOS 2900 also have either the family parts in their cell library or intend to have them. In addition, there are companies, such as VLSI Technology, that may not have standard 2900 parts, but still have them in their cell libraries.

Description: Ever-growing and changing family of mostly TTL bus-compatible, "bit-slice" building blocks. By now almost all possible semiconductor technologies are being used: bipolar (both TTL and ECL internally), CMOS, and even GaAs. Intended for microprogrammable systems in which they emulate existing computers or for use in specialized digital controllers. Latest twist is to use them as macrocells in semicustom libraries.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

Status: This bit-slice family has been around a long time. Each time its life seems over, it is reborn. Now it's getting new life from CMOS versions from many different sources. These versions have almost the same speed as the original bipolar—some suppliers claim equal or better speed—and only a fraction of the power consumption. The architectural motivation usually is to attain higher levels of parallelism with wide microcoinstructions, in which many fields control different hardware blocks. In many instances the CMOS versions are part of macrocell libraries, so that they can be assembled (ideally by a customer engineer at his workstation) into single-chip or few-chip semicustom VLSI solutions. The 2900 family is never likely to see especially high unit volumes because parts costs are too high.

HARDWARE — CHARACTERISTICS — SOFTWARE



Specification summary: TTL bus-compatible building blocks for creating moderately high-performance computers and controllers. Slices were originally 4 bits wide but now can be as much as 32 bits wide. Parts include sufficient features for emulating most computer architectures. User defines end product's macroinstruction set by microprogramming ROM. RALUs (2901, 2903, and 29203) respond to 8 and 16 basic instructions (2903 and 29203 include multiply and divide and floating-point normalization) within one clock cycle of 50 to 125 nsec (2901C performs 16-bit add in 83 nsec). Original family parts fabricated entirely from Schottky TTL. Now fine-geometry (near 1 μm) CMOS can produce equivalent speeds at lower power consumption. With CMOS, there's a trend to consolidate multiple 2900 functions on chip and to go to new space-saving packages.

User defines macroinstruction set by microprogramming ROM. Parts respond to the following instructions:
I—DATA-MANIPULATION INSTRUCTIONS
2901 performs three arithmetic functions on two operands, as well as five logic functions
2903A performs seven arithmetic functions and nine logic operations, as well as multiply and divide. Simultaneous add (or subtract) and shift possible
29203 has floating-point-normalize instruction
II—DATA-MOVEMENT INSTRUCTIONS
16 working registers in RALU RAM can be addressed two at a time for supplying two operands to the ALU simultaneously
III—PROGRAM-MANIPULATION INSTR
Defined by user in microcode. 2930 program-control unit executes 32 fetch and branch instructions
IV—PROGRAM-STATUS-MANIP INSTR
2904 shift and status-control chip provides two status registers for the 4-bit carry, overflow, zero, and negative. Bits can be set or cleared. Shift through carry or overflow. Borrows can be stored for subtract

BASIC 2900 PARTS

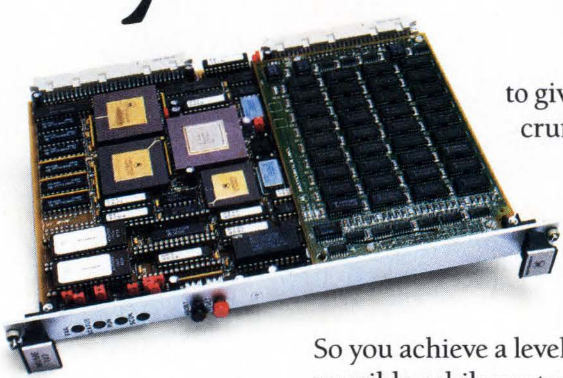
PART	# ON DIAGRAM	DESCRIPTION	COST (100 QTY)
2901/B/C	1	ALU	$6
29C01			$6
29C101			$35
2902A			$1.80
2903/A			$20
29203		ALU (BCD)	$20
2904	2		$16
29705/A		2-PORT RAM	$10
2909/A	4	MICROPROGRAM CONTROL UNITS	$5
2910/A			$13
29C10A			$13
2911/A			$4
29803A			$4
29811A			$3
2930		PROGRAM CONTROL UNITS (RELATIVE ADDRESSING)	$20
2932			$18
2913		INTERRUPT	$5
2914	5		$10
2905	3	TRANSCEIVERS	$5
2906			$7
2907			$4
2915A			$5
2916A			$4
2917A			$4

HARDWARE — SUPPORT — SOFTWARE

From third parties: Step Engineering (Sunnyvale, CA) offers new lower-cost PC XT/AT-based Microstep microcode development station ($3695). It consists of plug-in card for PC containing 25-nsec RAMs to simulate a 128×4k-bit microcode ROM plus debug/control software. It would be used in conjunction with Step's Metastep Microprogram language ($3000, or $6195 bundled with Microstep). Step's full-fledged Step-40 is expensive, but it has 10-nsec, 512×64k-bit microcode ROM. Hardware tools also available from HiLevel Technology (Tustin, CA) and others.
For ASIC: Silicon compilers for members of 2900 family (2901, 2910, 2913, and 2940) are in VLSI Technology's compiler library.

From third parties: Step Engineering (Sunnyvale, CA) offers Metastep, a generalized software language for developing microcode ($3000). It runs on CPM/68K, MS/DOS, VAX/Unix, and VAX/VMS. It is claimed to have the flexibility and structure to greatly ease the tedious and error-prone software side of microcode system development. Software tools also available from HiLevel Technology (Tustin, CA) and others.
Literature: *Bit Slice Microprocessor Design*, by John Mick and Jim Brick, McGraw-Hill, NY, NY, 1980.

"Their new 030 board isn't really a single-board computer. It's a single-board system."



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29300, 29C300

32-BIT BIPOLAR AND CMOS

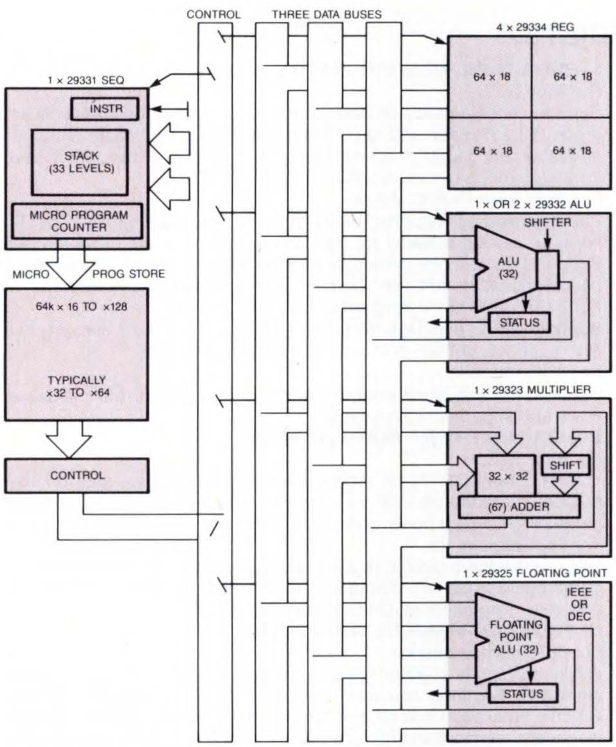
AVAILABILITY: 29300 and C300 available now in several speed grades. 29400 ECL discontinued in favor of advanced CMOS.
COST: A set of 29300 chips costs under $350.
SECOND SOURCE: None directly but, especially for CMOS parts, TI and Weitek offer 32-bit building blocks.

Description: 32-bit bipolar and CMOS building-block chip set that follows concepts established by 2900 bit-slice family, but with two major differences. First, family members all have a fixed, 32-bit data width. Second, the architecture and resulting microinstruction set are optimized for easy compiler writing. State-of-the-art performance has been achieved, as indicated by 70-nsec microinstruction cycle times, and a 32×32-bit multiplier (50 nsec).

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

Status: Supplier now has two very different architectures targeted at high-performance 32-bit applications: The 29000 and the 29300 μPs. The 29000 is RISC, rather than CISC like the 29300. RISC chips use combinatorial logic to get instructions down to single-cycle execution. The 29C300 also executes instructions in a single cycle, but implementing complex instruction sets on the C300 requires a 70-nsec clock cycle. The 29000 RISC family can operate faster. AMD appears to be involved in both extremes of the CISC-vs-RISC controversy.

HARDWARE — CHARACTERISTICS — SOFTWARE



PART NUMBER	DESCRIPTION	PERFORMANCE	AVAIL-ABILITY	COST (100 QTY)
TTL				
29331	16-BIT SEQUENCER	75 nSEC	NOW	$88
29332	16-BIT ALU	75 nSEC	NOW	$220
29334	84x18 REG FILE	24 nSEC	NOW	$80
29337	BOUNDS CHECKER	20 nSEC	NOW	$22
CMOS				
29C323	32-BIT MULTIPLIER	100 nSEC	NOW	$119
29C323-2	32-BIT MULTIPLIER	50 nSEC	NOW	$238
29C331	16-BIT SEQUENCER	90 nSEC	NOW	$72
29C331-2	16-BIT SEQUENCER	70 nSEC	NOW	$99
29C332	32-BIT ALU	80 nSEC	NOW	$175
29C334	64x18 REG FILE	30 nSEC	NOW	$54
29C334-2	64x18 REG FILE	20 nSEC	NOW	$86
29325/12	32-BIT SINGLE PRECISION	120 nSEC	NOW	$99
29325A	32-BIT SINGLE PRECISION	70 nSEC	NOW	$269
29C325/12	32-BIT SINGLE PRECISION	120 nSEC	1988	$99
29C327	64-BIT DOUBLE PRECISION	125 nSEC	1988	$329

NOTE:
'325 AND '327 PERFORMANCE SPEC REFERS TO CLOCKED MULTIPLY TIME.

Notes:
1. Many different architectures possible because of flexibility of parts.
2. Possibility of sharing dual-ported registers between two ALUs so that address calculation and data manipulation occur simultaneously within cycle. (Each ALU would have its operands and result read and written into a common multiported register file.)
3. Deep pipelining avoided so there can be fast response to decisions.

I—DATA-MANIPULATION INSTRUCTIONS
For 29332 ALU: includes 64-bit n-bit shift-up/down funnel shifter that can be combined with logic functions. Multiply and divide (one bit at a time). Priority encoding to support floating-point operations and graphics
For 29325 floating point: efficient execution of Newton-Raphson division and Horner's method of polynomial evaluation. Both IEEE and DEC formats (addition, subtraction, multiplication) with conversion between two modes
For 29323 32×32-bit multiplier: single- or double-precision multiply in one or four cycles, respectively
II—DATA-MOVEMENT INSTRUCTIONS
For 29334 64×18-bit register file (cascaded for full word width and desired length and used in conjunction with ALU): individual write for byte, 16-bit half word, or 32-bit full word
III—PROGRAM-MANIPULATION INSTR
For 29331 microprogram sequencer: instructions designed to support high-level-language constructs
The 33-level stack supports interrupts, loops, subroutine nesting, and multitasking at microlevel
Microtrapping for reuse of prior microinstruction
No support for relative addressing, because designers wanted to avoid performance penalty of adder, but decisions and interrupts handled on chip for fastest response
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in ALU, floating point, etc

Notes:
1. Designers say they endeavored to keep instructions orthogonal and symmetrical to ease task of compiler writing and facilitate structured microprogramming.
2. Self-checking implemented by parity bits in register file and by parity in off-chip data paths and ability to parallel units and compare results.

Specification summary: Building blocks for 32-bit-wide microprogrammable computer systems. Core set includes five parts (see table) that can stand alone or be used in mixed systems. Architecture supports features needed on advanced minicomputers, like parity checking and master/slave functional comparisons. Also suited for direct, very fast execution of high-level languages via compiled microcode. Triple data-bus architecture, with unidirectional buses for minimum speed loss caused by bus turnaround. Architecture sufficiently open to allow inclusion of performance accelerators, and family includes floating-point unit and 1-cycle fixed-point multiplier. TTL packages incorporate three low-profile horizontal fins to handle 4 to 7W heat dissipation. CMOS versions will dissipate in the 1W range and will not require heat sinks or cooling airflow.

HARDWARE — SUPPORT — SOFTWARE

From third parties: Step Engineering (Sunnyvale, CA) offers new lower-cost PC XT/AT-based Microstep microcode development station ($3695). It consists of plug-in card for PC containing 25-nsec RAMs to simulate a 128×4k-bit microcode ROM plus debug/control software. It would be used in conjunction with Step's Metastep Microprogram language ($3000, or $6195 bundled with Microstep). Hardware tools also available from HiLevel Technology (Tustin, CA) and others.

From third parties: Step Engineering (Sunnyvale, CA) offers Metastep, a generalized software language for developing microcode ($3000). It runs on CPM/68K, MS/DOS, VAX/Unix, and VAX/VMS. It is claimed to have the flexibility and structure to greatly ease the tedious and error-prone software side of microcode system development. Software tools also available from HiLevel Technology (Tustin, CA) and others.

74AS8XX/74AS88XX

8- AND 32-BIT BIPOLAR AND CMOS

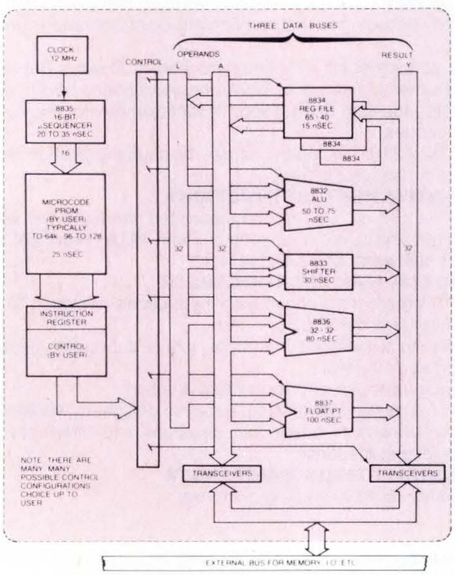
AVAILABILITY: Now for 8XX parts and first 88XX parts, but some have slipped behind promised schedule.
COST: See table for prices.
SECOND SOURCE: No direct sources, but AMD 29300/400 and Analog Devices Word Slice are similar.

Description: 8- and 32-bit custom CPU building-block chip sets done in high-performance bipolar and CMOS processes. Cycle times of 50 to 75 nsec worst case said to be accomplished at relatively low power-dissipation levels even for bipolar members, so no heat sinking is required. Family architecture facilitates byte operation, allowing for flexibility in data-word manipulation and resulting in system throughput in the 10-MIPS range.

Texas Instruments Inc
13536 N Central Expressway
Dallas, TX 75265
Phone (214) 995-6611

Status: Supplier expects to compete with similar AMD bipolar 29300/400 chip set for applications in high-end workstations, graphic systems, and superminis. Supplier's chips may also receive competition from new μPs such as Clipper, SPARC, and 29000. These CMOS devices have MIPS rates similar to those of the supplier's chips, though the RISC chips don't allow designers the architectural flexibility to achieve higher levels of parallelism. With respect to bipolar-vs-CMOS controversy, TI engineers tell us they have found it expeditious to convert some bipolar parts to CMOS (even after bipolar samples were put out) because CMOS has been better at meeting desired specs.

HARDWARE — CHARACTERISTICS — SOFTWARE



PART NO	DESCRIPTION	PERFORMANCE (mSEC)	NO OF PINS	AVAIL-ABILITY	COST (100 QTY)
74AS888	8-BIT REGISTER ALU	46	68	NOW	$35
74AS890	14-BIT MICRO-CONTROLLER	42	68	NOW	$40
74AS897	16/32-BIT BARREL SHIFTER	50	68	NOW	$40
74AS870	DUAL 16-WORD x4-BIT REGISTER	22	24	NOW	$6.58
74AC8832	32-BIT REGISTER ALU	50–75	208	NOW (SAMPLES)	NA
74AC8835	16-BIT MICRO-SEQUENCER	20–35	156	NOW (SAMPLES)	NA
74AS8834	65Wx40-BIT REGISTER FILE	15	156	NOW (SAMPLES)	NA
74AS8833	BARREL/FUNNEL SHIFTER	30	156	NOW (SAMPLES)	NA
74AC8831	32/64-BIT BARREL SHIFTER	25	86	NOW	$40
74ACT8836	32x32-BIT MULTIPLIER	80	NA	NOW (SAMPLES)	NA
74ACT8837	FLOATING-POINT PROCESSOR	100	NA	NOW (SAMPLES)	NA

Notes:
1. Family architecture facilitates the high degree of system parallelism possible with "wide" microcoding, allowing designer to operate devices simultaneously for greater throughput.
2. ALU and microsequencer support master/slave operation for tandem processing.
3. All members are 2-μm bipolar except for 8836 and 8837, which will start out in 1-μm CMOS. The bipolars will achieve low (4W) power dissipation because of special Schottky transistor logic that operates at 2V internal supply.

I—DATA-MANIPULATION INSTRUCTIONS
For 8800 ALU:
Supports double-precision data format for all instructions. Multiply and divide, 13 arithmetic and logic functions. Eight conditional shifts, normalization (all double and single length). Byte-oriented architecture allows structuring of data word in 8, 16, 24, or 32 bits.
For 8833 funnel/barrel shifter:
Priority encoding supports floating-point and graphics applications. 64-bit input can be masked for data manipulation on 32 extracted bits. Supports single-clock-cycle byte rotation. Circular arithmetic and logical operations on 32-bit fields. On-chip parity generation/checking.
For 8837 16/32-bit floating point:
Supports IEEE and DEC formats with conversion between the two. Also supports double- and single-precision operations.
For 8836 multiplier:
Supports 16- and 32-bit signed and unsigned multiplies. Indicates overflows and supports sign extends.
II-DATA-MOVEMENT INSTRUCTIONS
For 8832 RALU:
Three-operand 64×36-bit register file on chip supports byte-oriented operands for variable data word widths. 36-bit width = 32 bits data + 4 parity bits. On-chip parity generation/checking.
For 8834 register file:
64×40-bit edge-triggered register file cascadable with 74AS3232 ALU. Three-operand file with output mux for flexibility in data-word manipulation. Also byte oriented. On-chip parity checking.
III-PROGRAM-MANIPULATION INSTR
For 8835 microsequencer:
Facilitates high-level-language constructs; deep 65×20 stack supports interrupts. Two loop counters support nested loop program routines. On-chip breakpoint comparator for automatic branch routines. On-chip diagnostic registers and 890 upward compatibility for easy microcoding. Executes simultaneous interrupt and trap operations. Select next branch instruction from one of nine locations via output mux. All instructions can be made conditional via externally applied condition-code pin and/or value in internal register.

Note: Instructions described are for 88XX family devices. 8XX instructions are a subset, and the two sets are completely compatible.

Specification summary: Building blocks for microcoded custom CPU architectures. The 8XX family has four parts, and the 88XX family will have seven (see table). As 74AS prefix indicates, the devices meet the specifications of the AS version of the well-known 74 logic family line. Two of the devices with 74ACT prefixes use TI EPIC CMOS process but have TTL-compatible outputs. The architecture is designed to support high-performance minicomputer workstation and graphic machines by incorporating features like parity generation/checking, master/slave operation for tandem processing, and 3-bus architecture (see diagram). Worst-case cycle times of 50 to 75 nsec can be accomplished with relatively low power dissipation (4W), which eliminates need for device heat sinks. On-chip diagnostic registers on the sequencer and barrel/funnel shifter ease microcode development. Large pin-count devices (see table) are packaged in pin-grid arrays and plastic leaded chip carriers.

HARDWARE — SUPPORT — SOFTWARE

Supplier recommends same approach for development systems as that used with other microcoded building-block chip sets such as the 2900. Third-party support available from Hewlett-Packard, HiLevel Technology (Tustin, CA), and Step Engineering (Sunnyvale, CA). High-speed microcode ROM emulators from above companies cost $13,000 to $30,000. Supplier's evaluation module (EVM) board incorporates a full Basic interpreter and monitor program that can be accessed through an RS-232C port using a nonintelligent terminal or terminal emulator (personal computer with appropriate software).

Meta- and cross-assemblers will be provided by third-party vendors such as HiLevel Technology ($1400), as well as an OEM version from the supplier. Existing assemblers in place for the 74AS8XX are compatible with the 74AS88XX family.

CIRCLE NO 183

WORD-SLICE GP NUMERIC PROCESSOR

AVAILABILITY: Now for most parts; see table.
COST: $27 to $300; see table.
SECOND SOURCE: No direct source, except for industry-standard multipliers. Similar functions are available from AMD, Cypress Semiconductor (San Jose, CA), Integrated Device Technology (Santa Clara, CA), Wafer Scale Integration (Fremont, CA), Weitek (Sunnyvale, CA), and many others.

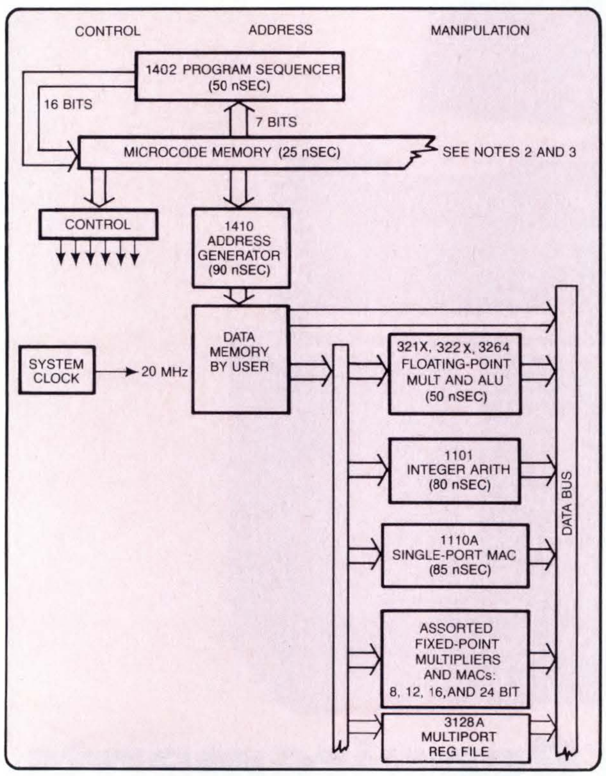
Description: Follows trend established with 2900 bit-slice family of providing building blocks that system designers can use in microprogrammed systems. This family has been found suitable for general numeric or number-crunching applications, such as accelerators. Supplier's goal was to provide microprogram sequencers and address generators that could be used with supplier's floating- and fixed-point multipliers to design complete systems.

16-BIT CMOS µP BUILDING BLOCKS

Analog Devices Inc
Digital Signal Processing Div
Box 9106
Norwood, MA 02062
Phone (617) 329-4700

Status: Most parts are available now. The 3264 floating-point unit should be available in late '88 ($689), and the 1402 sequencer should be ready in early '89 ($68). The 3128 register file is available now ($145).

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes:
1. Architecture shown is only one of many possibilities.
2. Microcode memory can be 64k deep. It can be as wide as designer needs for simultaneous control of one or more data pipes (typically approximately 100 bits).
3. Microcode memory can be RAM for downloading of algorithms from host.

I—DATA-MANIPULATION INSTRUCTIONS
For ADSP-1101 16-bit integer arithmetic unit:
Add and subtract, multiply, multiply and accumulate (MAC)
Conditional multiply and accumulate
Dual 40-bit accumulator control and internal feedback
Logicals and shifts
Block floating-point shifters and control
For ADSP-321X/2X floating-point multipliers and ALUs:
Multiply single-precision floating point, double-precision floating point, and 32-bit fixed point
Complete arithmetic and logical ALU operations
Complete format-conversion operations

II—DATA-MOVEMENT INSTRUCTIONS
For ADSP-1410 16-bit address generator:
Preupdate and postupdate mode conditional looping (zero overhead)
Add or subtract increments or offsets to pointers
Register transfers
Logicals and shifts
Bit-reverse output (for FFT)

III & IV—PROGRAM-MANIPULATION AND -STATUS INSTR
For ADSP-1401, 16-bit program sequencers:
Jump and branch-absolute, relative and indirect
Push, pop data, counters and pointers to subroutine stacks
Modify subroutine stack and register stack pointers
Interrupt masking and control
Writable control store (for downloading)

Specification summary: Microprogrammable chips set for numerical processing, permitting increased throughput by user-developed parallelism. Consists of various multipliers and multiplier accumulators (see table) and microcode program sequencers and address generators (see table). It can be driven by a 10-MHz clock, and within resulting 100-nsec cycle can perform complete instructions (obtain data from memory and process it). Most recent versions support 50-nsec cycle. Sequencer helps host computer download code into a RAM microprogram store (for accelerator applications). Fabricated in CMOS.

PART	DESCRIPTION	AVAIL-ABILITY	COST (100 QTY)
3201	MULT, SINGLE PRECISION, FP	NOW	$97
3202	ALU, SINGLE PRECISION, FP	NOW	$97
3210	MULT, FP	NOW	$300
3211	MULT, FP	NOW	$300
3212	MULT, FP (IEEE)	NOW	$297
3213	MULT, FP (DEC)	NOW	$297
3220	ALU, FP	NOW	$300
3221	ALU, FP	NOW	$300
3222	ALU, FP (IEEE)	NOW	$297
3223	ALU, FP (DEC)	NOW	$297
1401	SEQUENCER, PROGRAM	NOW	$57
1410	GENERATOR, ADDRESS	NOW	$37
1110A	MULT/ACCUM, 16-BIT, 1 PORT	NOW	$37
1101	ALU, 16-BIT, INTEGER	NOW	$108
1080A	MULT, 8-BIT, 2'S COMPL	NOW	$27
1081A	MULT, 8-BIT, UNSIGNED	NOW	$27
1012A	MULT, 12-BIT	NOW	$42
1016A	MULT, 16-BIT	NOW	$45
1024A	MULT, 24-BIT	NOW	$81
1008A	MULT/ACCUM, 8-BIT	NOW	$41
1009A	MULT/ACCUM, 12-BIT	NOW	$53
1010A	MULT/ACCUM, 16-BIT	NOW	$56

HARDWARE — SUPPORT — SOFTWARE

Supplier recommends same approach to development systems as that used with bit-slice microcoded components (ie, the AMD 2900 family). Suitable ROM-simulation systems are available from Step Engineering (Sunnyvale, CA) and HiLevel Technology (Tustin, CA). Similar aids are offered by Tektronix and Hewlett-Packard.

Mnemonics with microcode fields are available from the supplier for use with a meta-assembler. These programs can be used by a designer to create a design-dependent assembly-level language. Step Engineering, HiLevel Technology, and Microtek Research meta-assemblers support parts via definition files for Wordslice mnemonics. Most of the parts are included in Logic Automation (Beaverton, OR) simulation libraries.

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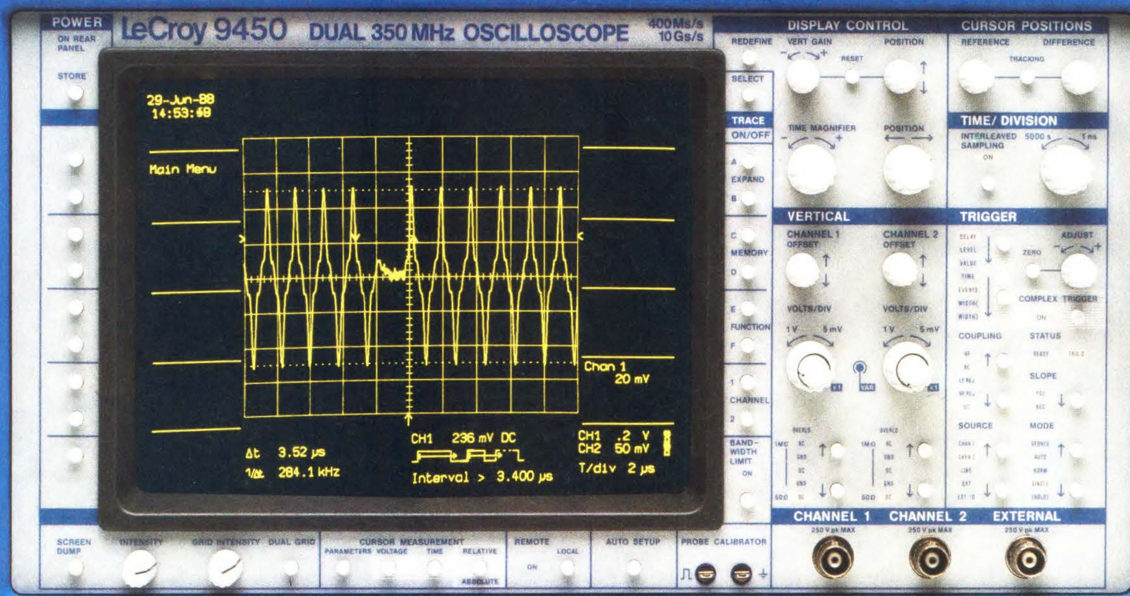

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* Automatic Waveform Parameters

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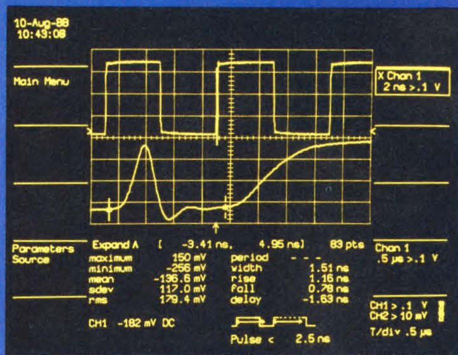

FASTGLITCH trigger mode is used to trigger on a glitch 1.51 nsec wide which occurs before the leading edge of a 500 kHz clock signal (top trace, see trigger arrow at the bottom of the graticule). Fast sampling rates, automatic pulse parameters and horizontal expansion by 250 times (lower trace) all combine to reveal the signal details.

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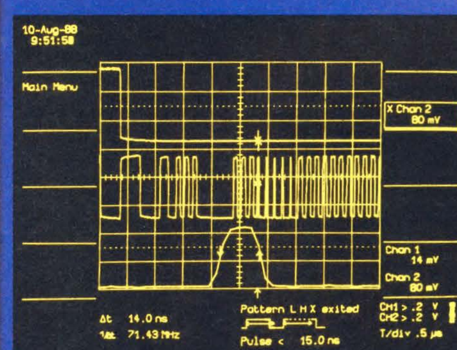

Logic conditions can be individually set for each of the 9450's inputs. PATTERN trigger mode is used to trigger only when the logic condition CH1 Low (top trace) and CH2 High (middle) is exited. The pattern must also be present for less than 15 nsec (lower trace). The trigger position is shown by the arrow at the bottom of the graticule.

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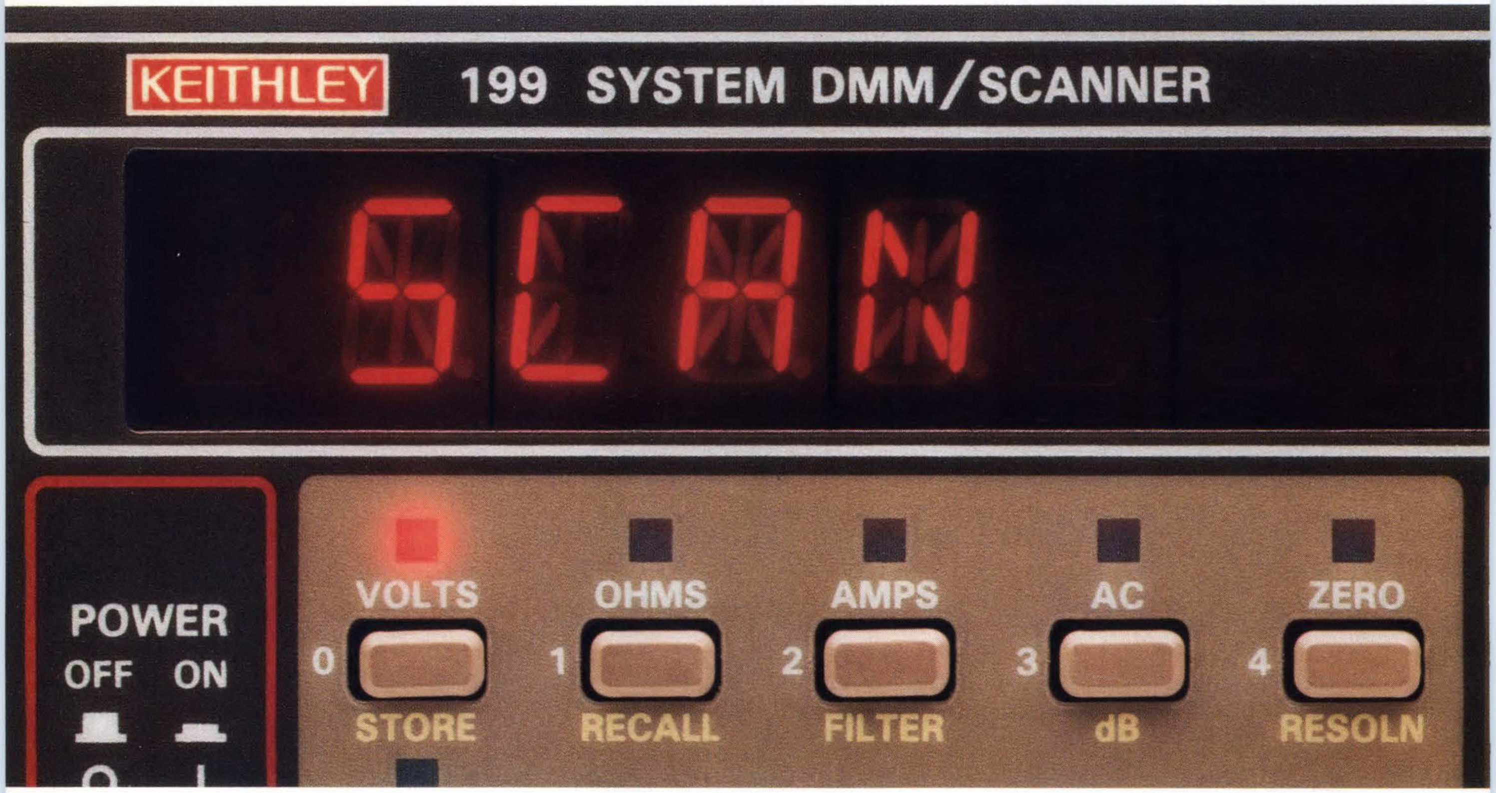

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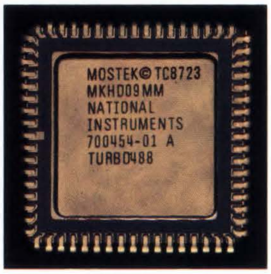
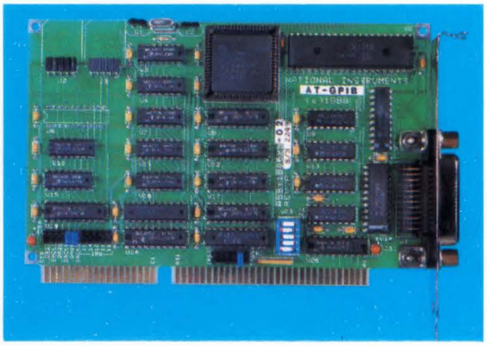
National Instruments has been working with the IEEE-488 bus (GPIB) for more than 12 years. Our hardware products are designed to meet *all* your needs. Choose any popular computer and we have an IEEE-488 solution. Each product line also offers you the choice of a low-cost solution for less demanding applications or a high-performance solution for applications that demand the best. We back our products with comprehensive customer support. No one gives you more choices, better performance, or better support than National Instruments.



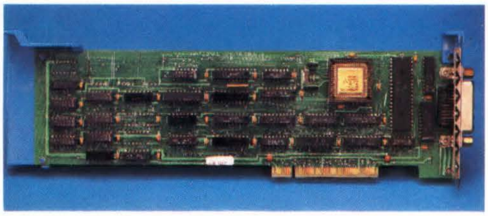
Turbo488™ ASIC Technology

At the heart of our highest performance interface boards is the National Instruments Turbo488 Application Specific Integrated Circuit (ASIC). Turbo488 integrates 26 chips into one, resulting in a lower cost implementation with significantly improved performance. Special last-byte handling significantly reduces the software overhead of an application program.



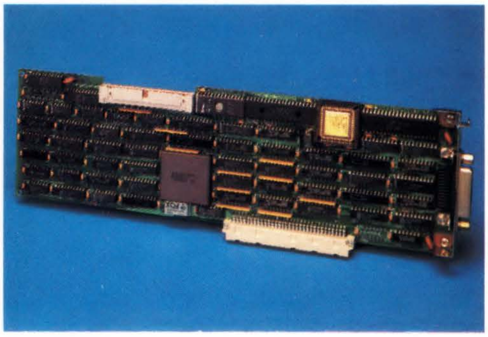
AT-GPIB—PC/AT Interface

- ★ Turbo488 ASIC
- ★ 1M bytes/sec DMA rates
- ★ GPIB monitor port for board and bus level diagnostics
- ★ Byte-to-word packing/unpacking to increase throughput
- ★ 11 interrupt levels
- ★ Three 16-bit DMA channels
- ★ Shared interrupt and DMA capability
- ★ LabWindows and NI-488 Software support



MC-GPIB—Personal System/2 Micro Channel Interface

- ★ Turbo488 ASIC
- ★ 1M bytes/sec DMA rates
- ★ Programmable Option Set circuitry for selecting I/O address, interrupt level, and DMA channel
- ★ Byte-to-word packing/unpacking to increase throughput
- ★ LabWindows and NI-488 Software support



NB-DMA-8-G—Macintosh II NuBus Interface

- ★ Turbo488 ASIC
- ★ 1M bytes/sec DMA rates
- ★ 8 channels of high-performance 32-bit DMA
  - — Buffer chaining
  - — Accesses full NuBus 4 gigabyte address space
- ★ DMA and timing support for National Instruments data acquisition cards via RTSI bus
- ★ 8 independent 16-bit counter/timer channels
- ★ LabVIEW and NI-488 Software support

NB-GPIB—Macintosh II NuBus Interface

GPIB-SE—Macintosh SE Interface

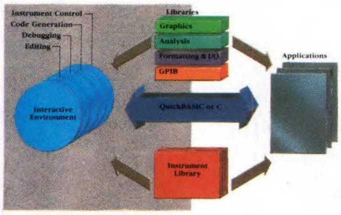
NB-GPIB

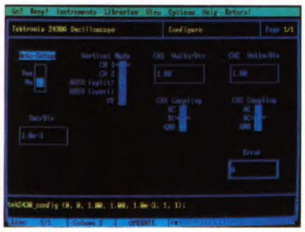
- ★ Turbo488 ASIC
- ★ 400K bytes/sec programmed I/O rates
- ★ GPIB monitor port
- ★ DMA operations over RTSI bus with NB-DMA-8-G
- ★ Byte-to-word packing/unpacking to increase throughput
- ★ LabVIEW and NI-488 Software support

GPIB-SE

- ★ Turbo488 ASIC
- ★ 1M bytes/sec rates with optional DMA controller
- ★ Optional numeric coprocessor
- ★ LabVIEW and NI-488 Software support

SECOND GENERATION





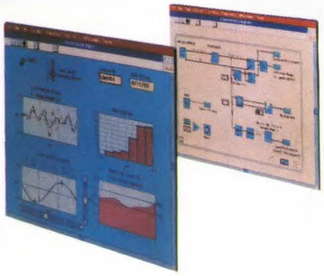
LabWindows®

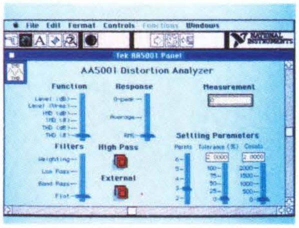
LabWindows is a software system for the IBM PC, PS/2, and compatibles designed to provide rapid development, prototyping, and operation of test and measurement applications by fortifying and enhancing C and QuickBASIC. These languages are fortified by an interactive development environment and enhanced by supportive libraries. Instrument control applications can be quickly developed using LabWindows interactive editing and debugging features, automatic code generation mechanisms, instrument library, GPIB library, graphics library, analysis library, and formatting and I/O library.

Lotus Measure®

Lotus Measure is a set of data acquisition drivers for Lotus 1-2-3 or Symphony that can collect data and store it directly into a 1-2-3 or Symphony spreadsheet. Lotus Measure fortifies the 1-2-3 or Symphony macro command language by adding an advanced set of macro commands to perform IEEE-488, RS-232, and analog-to-digital operations. All functions available in the worksheet can be easily accessed for immediate reduction, analysis, and presentation of the data.

THIRD GENERATION





LabVIEW®

LabVIEW is an easy-to-use, powerful graphical programming language for the Macintosh family of computers. LabVIEW (Laboratory Virtual Instrument Engineering Workbench) has a complete integrated programming environment for applications involving instrument control, data acquisition, data analysis, data formatting, data presentation and data management. LabVIEW also has an extensive Instrument Library. The basis of LabVIEW is the representation of a software module as a Virtual Instrument. A Virtual Instrument is a real instrument made with software. LabVIEW users construct programs using block diagrams—a natural design notation of scientists and engineers. These block diagrams are the actual executable programs, that can be operated by way of user-defined graphical front panels that look and act like instruments.

Additional Application Software

National Instruments IEEE-488 interface boards are widely recognized for their quality and performance and are supported by many application software packages:

- ASYST
- GURU
- TestWindows
- ASYSTANT
- EZ-TEK
- LaserPaint
- TBASIC
- EZ-TEST
- SPD
- XScan
- WaveTest
- ChromaScan
- LABTECH NOTEBOOK
- Parameter Manager

Instrument Libraries

There exist over 4000 IEEE-488 compatible instruments manufactured by more than 300 vendors worldwide. Each of these instruments has its own, unique set of commands that make it function programmatically. The real ease of programming instruments comes from having a library of pre-packaged software modules that operate instruments, by way of intuitive, graphical panel interfaces. An instrument library makes operating an instrument from the computer as easy as operating it from its front panel. National Instruments is dedicated to increasing the instrument libraries of both LabWindows and LabVIEW by adding the instruments frequently requested.

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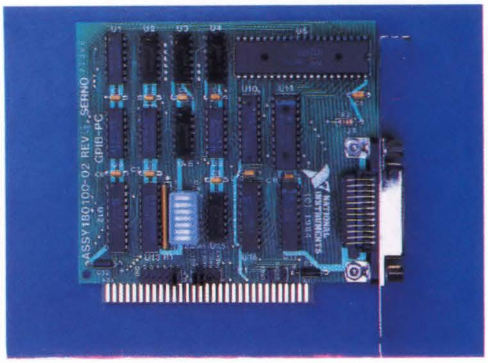
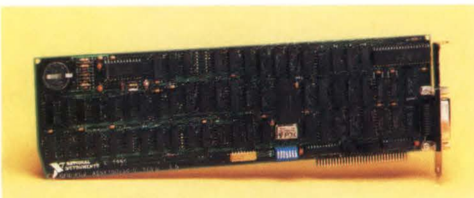


GPIB-PCII/IIA—IBM PC Interface

- ★ Half-size card
- ★ DMA rates over 300K bytes/sec
- ★ Standardized by IBM
- ★ AEGIS handler for Apollo 3000 and 4000 workstations
- ★ 6 interrupt lines
- ★ 3 DMA channels
- ★ LabWindows and NI-488 Software support



GPIB-PCIII—IBM PC/XT/RT PC Interface

- ★ Onboard high-speed FIFO buffer
- ★ 1M bytes/sec DMA rates
- ★ GPIB monitor port
- ★ Optional AIX handler
- ★ Interrupt circuitry for detecting SRQ and clock alarm
- ★ LabWindows and NI-488 Software support

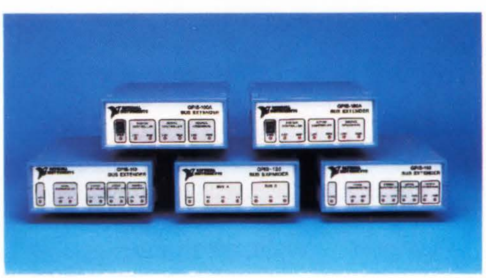
MicroGPIB Products—Converters, Controllers, and Data Buffer

MicroGPIB Products

- ★ **GPIB-232CV** bidirectional transparent data converter between IEEE-488 and RS-232
- ★ **GPIB-422CV** bidirectional transparent data converter between IEEE-488 and RS-422
- ★ **GPIB-PRL** transparent parallel data converter
- ★ **GPIB-232CT** full-function IEEE-488 controller from RS-232 port
- ★ **GPIB-422CT** full-function IEEE-488 controller from RS-422 port compatible with Macintosh serial port
- ★ **GPIB-SCSI** full-function IEEE-488 controller from SCSI port
- ★ **GPIB-BUF** IEEE-488 data buffer with 900K bytes/sec transfer rates and 1M bytes of RAM

GPIB-MAC

- ★ Macintosh serial port interface
- ★ External configuration switches
- ★ 2K to 32K byte data buffer
- ★ Baud rates from 300 to 57.6K bits per second
- ★ LabVIEW Software system support



GPIB 100 Series—Bus Extenders/Expander

- ★ **GPIB-100A** High performance parallel bus extender
  - — Supports 28 devices at 300 m
  - — 222K bytes/sec transfer rates
- ★ **GPIB-110** Serial bus extender
  - — Fiber optic or coaxial cabling
  - — 144K bytes/sec transfer rates
- ★ **GPIB-120** Bus Expander
  - — Optically isolates 2 GPIB buses
  - — Extends GPIB by interfacing up to 14 more devices
  - — Doubles the GPIB 20 m cable limit
  - — Transparent to user software

GPIB-410—Bus Analyzer/Monitor

- ★ For use in debugging any GPIB application
- ★ Stores GPIB status in memory for later review
- ★ Simulated LEDs reflect the current condition of the GPIB
- ★ Emulate source or acceptor
- ★ Requires IBM PC as host

GPIB11 Series—Q-BUS/UNIBUS Interfaces

GPIB11V-2
- ★ Dual height card for Q-BUS
- ★ Supports MicroVAX series of computers
- ★ 250K bytes/sec DMA rates

GPIB11V-1
- ★ Dual height card for Q-BUS
- ★ 50K bytes/sec programmed I/O rates

GPIB11-2
- ★ Hex height card for UNIBUS
- ★ 500K bytes/sec DMA rates

GPIB11-1
- ★ Quad height card for UNIBUS
- ★ 60K bytes/sec programmed I/O rates

GPIB11 Series Software Support—RT, RSX, MicroVMS, VAXELN, UNIX, and RSX11M+ handlers in source code; NI DEC-Style Software

GPIB-1014 Series—VMEbus Interfaces

Complete Support for Sun Computers

GPIB-1014
- ★ 500K bytes/sec DMA rates
- ★ Full 24-bit addressing

GPIB-1014P
- ★ Single or double height front panels
- ★ 80K bytes/sec programmed I/O rates

GPIB-1014DP
- ★ Dual GPIB-1014P interface; one expansion slot

GPIB-S3/4
- ★ Kit for Sun-3 and Sun-4 workstations
- ★ Includes interface board, adapter bracket, internal cable, and software

GPIB-1014 Series Software Support—UNIX, real-time and multitasking handlers, NI-488 Software

GPIB-796 Series—MULTIBUS/SBX Interfaces

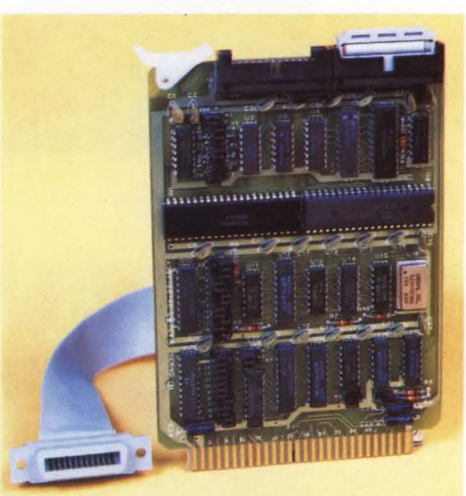
Complete Support for Apollo Computers

GPIB-796
- ★ 24-bit MULTIBUS addressing
- ★ 500K bytes/sec DMA rates
- ★ AEGIS handler for Apollo 3000 and 4000 workstations

GPIB-796P
- ★ 3 optional iSBX connectors
- ★ 50K bytes/sec programmed I/O rates

GPIB-SBX
- ★ Intel iSBX bus interface
- ★ Turns GPIB-796P into multiport interface
- ★ 250K bytes/sec DMA rates

GPIB-796 Series Software Support—UNIX, AEGIS, real-time, and multitasking handlers, NI-488 Software



GPIB-961P—STD Bus Interface

- ★ STD-Z80, -8085, -8088 compatible
- ★ 500K bytes/sec DMA rates
- ★ RS-232, counters, timers, digital I/O lines
- ★ NI-488 Software support

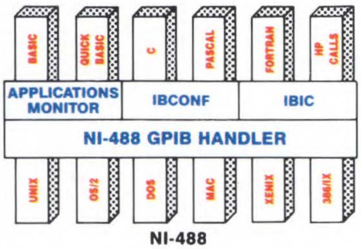
GPIB-3B2—AT&T 3B2 Interface

- ★ Onboard 80186 processor with 128K bytes of memory
- ★ 790K bytes/sec DMA rates
- ★ UNIX software
- ★ NI-488 Software support

THREE GENERATIONS OF SOFTWARE TECHNOLOGY

Three generations of innovative, high-performance software technology have been developed to simplify your programming task. The first generation includes flexible products that handle the fundamental I/O and data acquisition requirements. The second generation is an extension of the first generation that includes products that fortify and enhance an existing programming environment in order to minimize development time and meet the data acquisition, data analysis, and data presentation requirements. The third generation combines the features of the first two generations with an integrated programming environment and language designed for instrument control applications.

FIRST GENERATION



NI-488 Software

The NI-488 software established a standard for PC-based instrument control drivers by introducing the first loadable IEEE-488 device driver for MS-DOS based personal computers. The NI-488 software now covers a number of different computer platforms such as IBM PC and PS/2, Macintosh, Sun, and Pro-Log STD-DOS. Major companies such as IBM, Tektronix, Philips, LeCroy, Howtek, Sharp, Perkin Elmer, Instron, Bruel & Kjaer, Hitachi Nakaworks, and Advantest all use the NI-488 software to produce innovative, high-quality products. This large backing has established NI-488 as the *de facto* **industry standard**.

Flexible

- Use any instrument, even one not 100% compatible with the IEEE-488 specification
- Use a language that meets the demands of your specific application (BASIC, C, Pascal, FORTRAN, Assembler)
- Use a computer architecture that will handle all your computing needs
- Use a multitasking operating system: versions for OS/2, UNIX, 386/ix, and XENIX

High-speed

- Designed to be a high-speed device driver
- Subroutine-based structure as opposed to a slower character I/O implementation
- Direct Memory Access (DMA) transfers are used without special programming instructions

Easy-to-use

- Subroutines and functions can be called from familiar programming languages
- Only a small number of high-level functions are needed for most applications
- To initialize the bus and configure a multimeter only two simple commands are needed:

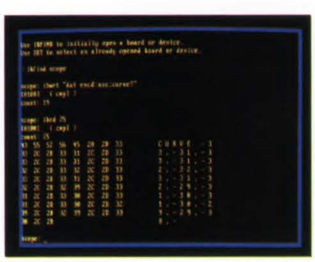
```
CALL IBFIND("DMM", DMM%)
CALL IBWRT(DMM%,"F1ROTO")
```

Reliable

- Over twelve years experience developing GPIB device handlers
- Built-in error checking
- Exhaustive testing prior to release
- Quick response to user needs and suggestions

Utilities:

IBIC—With the IEEE-488 Bus Interactive Control (IBIC) utility you can control and communicate with instruments from the keyboard. The IBIC utility is a simple way to learn the NI-488 handler functions and the device-specific commands of the instrument or to troubleshoot the system.



Applications Monitor— A utility that performs automatic error detection and identification. For ease in debugging, a Session Summary of all the GPIB commands made during a session is generated.

IBCONF—A utility program that configures the NI-488 handler for GPIB addresses, timeout settings, termination methods, and device-specific characteristics.

HP-Style Calls—For users familiar with the calls supported by a Hewlett-Packard controller, the NI-488 software has an option for HP-Style function calls.

DESIGNER'S GUIDE

dc/dc converters
Part 2

Proper instrumentation eases low-power dc/dc-converter design

This article, part 2 of a 4-part series, provides tips on selecting the right instrumentation to evaluate the performance of your low-power 5, 12, and ±12V converter designs. Part 1 emphasized the design of low-noise 5 to ±15V converters; parts 3 and 4, respectively, will show how to design dc/dc converters for power conservation and how to replace inductors with switched-cap techniques in dc/dc converter designs.

Jim Williams and Brian Huffman,
Linear Technology Corp

Flexibility is the key parameter in selecting instrumentation for dc/dc-converter design. Although wide bandwidths, high resolution, and computational sophistication are valuable features, they're really unimportant in designing converters. Typically, converter design requires the simultaneous observation of a number of relatively slow circuit events. The instruments used in converter design must have such features as fully floating inputs, high sensitivity, differential dc nulling or slide-back plug-in capability, high-impedance probes, and versatile triggering/multitrace capability.

Consider probe impedance, for example. Standard 1× and 10× scope probes are fine for many measurements, but the ground strap can be a problem in some cases. Because wideband switching noise is present in dc/dc converters, you must use the shortest possible ground return when making low-level measurements.

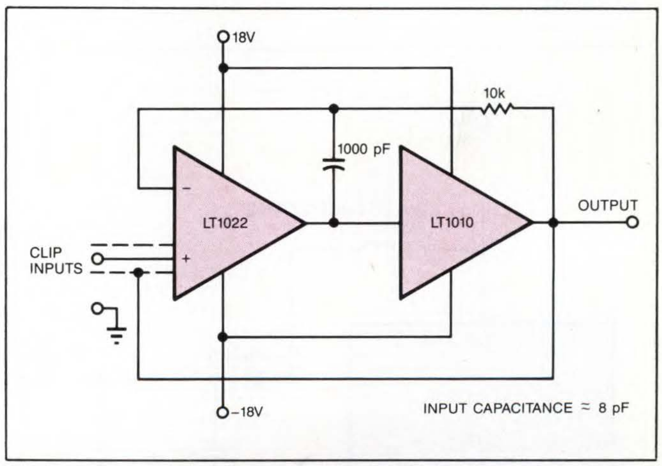


***Fig 1—You can solve a lot of loading problems** by using this simple probe, which employs an LT1022 high-speed FET op amp to drive an LT1010 buffer. The LT1010's output serves as a cable and probe drive source, and it also biases the circuit's input shield.*

It's important, therefore, to use a probe that can accommodate a variety of tip-grounding accessories.

You'll rarely require wideband, FET-type probes, but a moderate-speed, high-impedance buffer probe is quite useful. In many converter circuits (especially micropower designs), you'll have to monitor high-impedance nodes. Usually, the 10-MΩ loading of standard 10× probes will suffice, but when you use these standard probes, you have to trade away sensitivity. On the other hand, the sensitivity of 1× probes is adequate for most measurements, but these probes can create loading problems.

You'll rarely require wideband FET-type probes, but a moderate-speed, high-impedance buffer probe is useful.

The simple circuit in **Fig 1** solves probe-loading problems. The design's LT1022 high-speed FET op amp drives an LT1010 buffer. The LT1010's output serves as a cable and probe drive source and also biases the circuit's input shield. This biasing bootstraps the input capacitance and reduces its effect. The bandwidth as well as the ac and dc errors of this circuit are low enough for almost all converter work. If you build the circuit, along with its own power supply, into a small enclosure, you can use it as an input to an oscilloscope, with good results.

An isolated probe allows you to make fully floating measurements even in the presence of high common-mode voltages. Such a capability is very useful when you have to look across floating points in a circuit rather than make the usual ground-referenced measurements. This probe can be very valuable for directly observing an ungrounded transistor's saturation characteristics or for monitoring waveforms across a floating shunt.

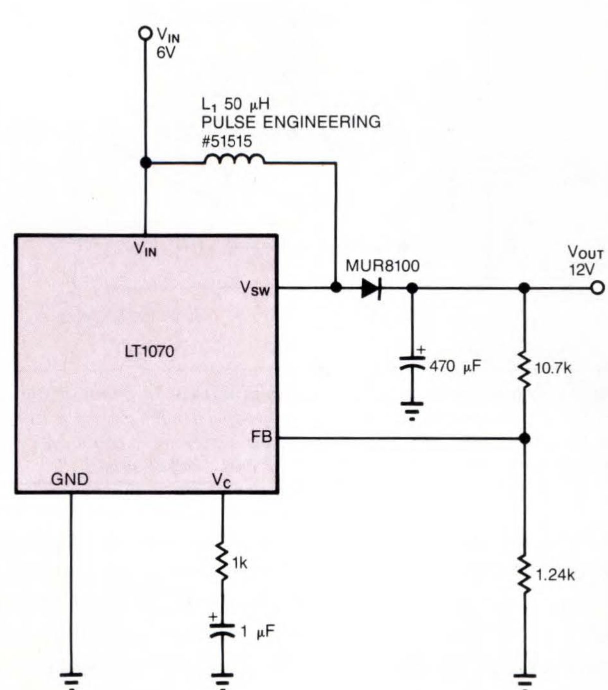


Fig 2—In this typical flyback-type converter, *the LT1070's internal 40-kHz clock produces a flyback event every 25 µsec. Each time the LT1070's V_{SW} pin internally switches to ground, it produces an inductive flyback voltage that converts the 6V battery input to a 12V output.*

Current probes are also an indispensable tool for converter design. In many cases, current waveforms contain more valuable information than do voltage waveforms. Clip-on current probes are convenient. Hall-effect-based versions respond as low as dc and feature 50-MHz bandwidth capability. Transformer-type current probes are faster, but they have rolloff below several hundred hertz. Both types have saturation limitations. If you exceed these limitations, you'll get some confusing displays on the CRT.

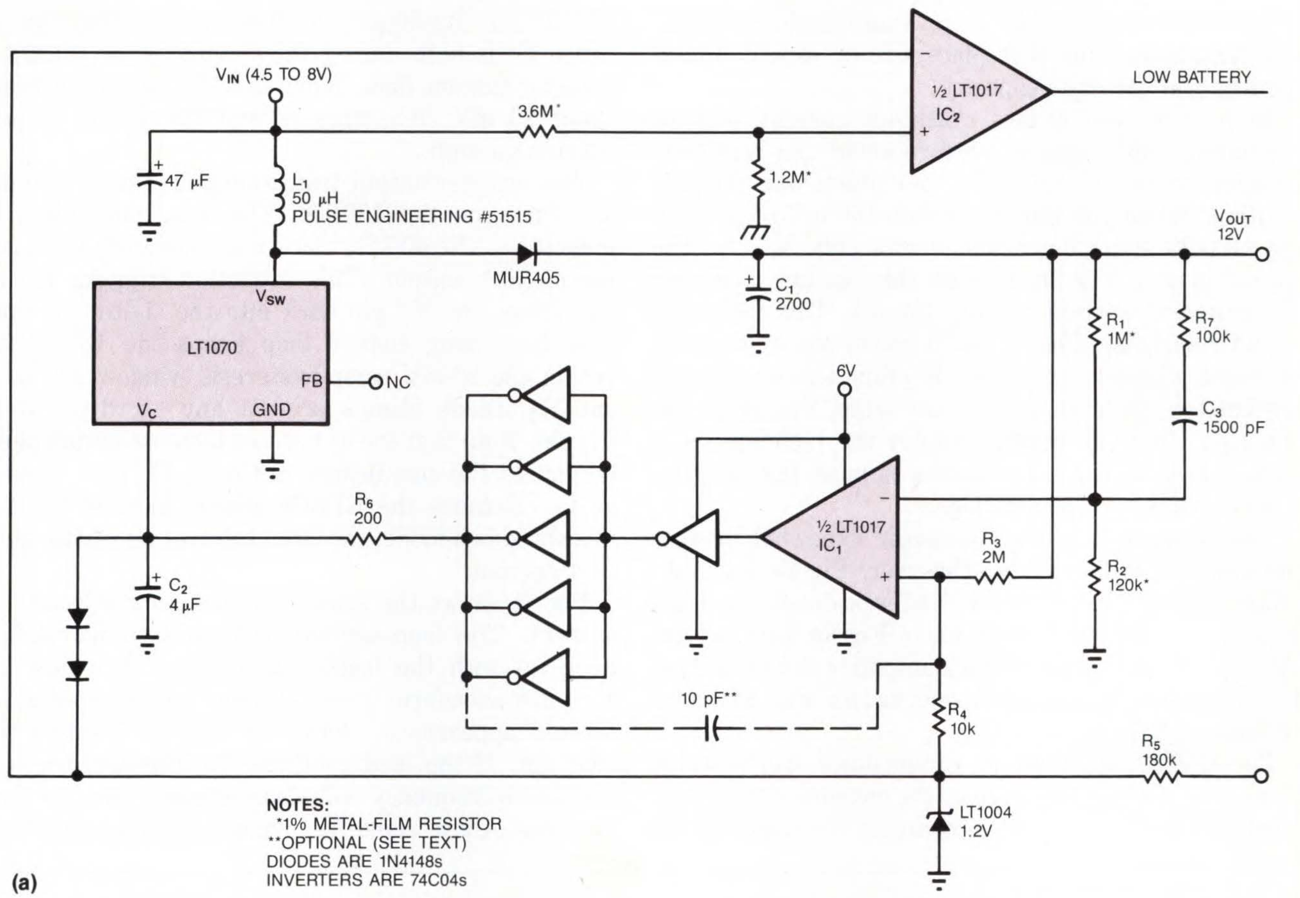
Consider using a nonelectronic voltmeter

Almost any digital voltmeter will suffice for converter work. The meter should have current-measurement capability and provisions for battery operation. The instrument's capability to operate from battery power allows you to make floating measurements and eliminates possible ground-loop errors. In addition, a nonelectronic voltmeter (or volt-ohmmeter) is a worthwhile addition to the converter-design bench. Converter noise occasionally disturbs electronic voltmeters and produces erratic readings. A nonelectronic voltmeter contains no active circuitry, so it's less susceptible to noise-related problems.

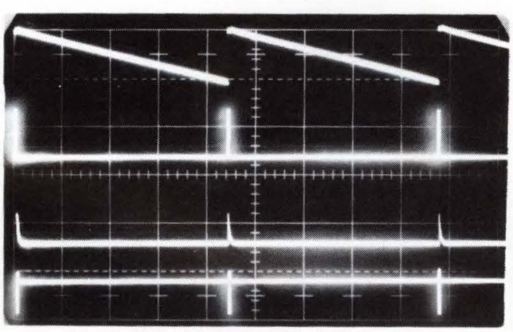
Addressing the needs of portable applications

The power supply's current requirements can vary widely in many battery-powered applications. Although normal operation might require currents in the ampere range, supply-current drain might drop into the microampere range for systems that are in standby or sleep mode. A typical lap-top computer may draw 1 to 2A while running and require only a few hundred microamps for memory backup when not running. Theoretically, any dc/dc converter designed for loop stability under no-load conditions will work in this computer application. From the practical standpoint, however, a converter with a relatively large quiescent-current requirement may drain the battery excessively during intervals of low output current.

Fig 2 shows a typical flyback-type converter. Each time the LT1070's V_{SW} pin internally switches to ground, it produces an inductive flyback voltage that converts the 6V battery input to a 12V output. The LT1070's internal 40-kHz clock produces a flyback event every 25 µsec. The LT1070's internal error amplifier controls the energy in this event by forcing the feedback pin, FB, to a 1.23V reference level. The RC damper network on the error amplifier's high-impedance output (V_C pin) provides compensation to stabilize

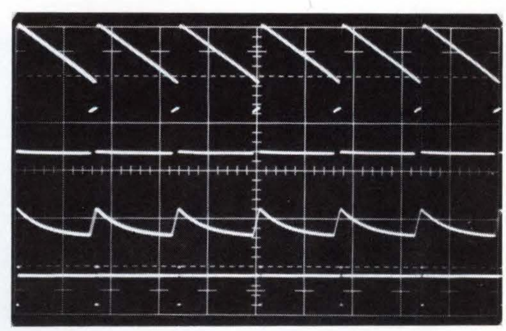


(a)



TRACE	VERTICAL	HORIZONTAL
A	0.02V/DIV (AC COUPLED)	1 SEC/DIV
B	5V/DIV	1 SEC/DIV
C	2V/DIV	1 SEC/DIV
D	10V/DIV	1 SEC/DIV

(b)



TRACE	VERTICAL	HORIZONTAL
A	0.02V/DIV	20 mSEC/DIV
B	5V/DIV	20 mSEC/DIV
C	2V/DIV	20 mSEC/DIV
D	10V/DIV	20 mSEC/DIV

(c)

***Fig 3—You can reduce quiescent current to only 150 μA** by pulling the V_C down to within 150 mV of ground **(a)**. Under no-load conditions **(b)**, the 12V output (trace A) ramps down over a number of seconds. During this period, the outputs of the paralleled 74C04 inverters and comparator IC_1 (trace B) are low, pulling the V_C pin low (trace C) and putting the LT1070 into its 50-μA shutdown mode. For a 3-mA load current **(c)**, the loop-oscillation frequency increases to keep up with the load's sink-current demands.*

An isolated probe lets you make fully floating measurements even in the presence of high common-mode voltages.

the loop. This circuit works well, but it draws 9 mA of quiescent current. The 9 mA value might be excessive for applications that place size or weight limitations on the battery's capacity.

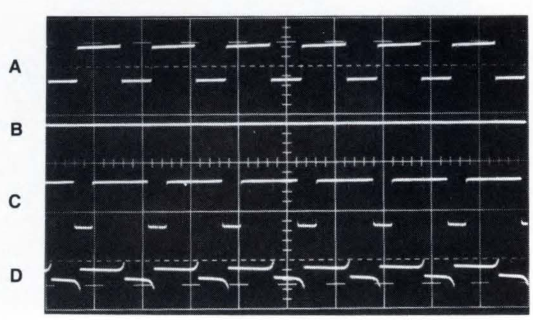
So how do you reduce quiescent current without degrading high-current performance? An auxiliary function of the LT1070's V_C pin offers one possible solution. When you pull V_C within 150 mV of ground, the LT1070 shuts down and draws only 50 μA. The special loop in **Fig 3a** exploits this feature, reducing the quiescent current to only 150 μA. This technique is particularly significant, and it has broad implications for battery-powered systems. IC_2 functions as a simple low-battery detector, pulling low when V_{IN} drops below 4.8V. You can readily employ the technique in a wide variety of dc/dc converters to meet the needs of a great number of applications.

The signal flow in **Fig 3**'s circuit somewhat mirrors the flow in **Fig 2**'s circuit. However, **Fig 3a** has additional circuitry between the feedback divider and the V_C pin. In addition, the circuit in **Fig 3a** does not use the LT1070's internal feedback amplifier and reference. **Fig 3b** shows operating waveforms for **Fig 3a** under no-load conditions.

The 12V output (trace A) ramps down over a period of seconds. During this period, the outputs of the paralleled 74C04 inverters and comparator IC_1 (trace B) are low, pulling the V_C pin low (trace C) and putting the LT1070 into its 50-μA shutdown mode. The V_{SW} pin (trace D) is high during this sequence, so there's no inductor current flow. When the 12V output decreases about 20 mV, IC_1 triggers and the 74C04 inverter outputs go high.

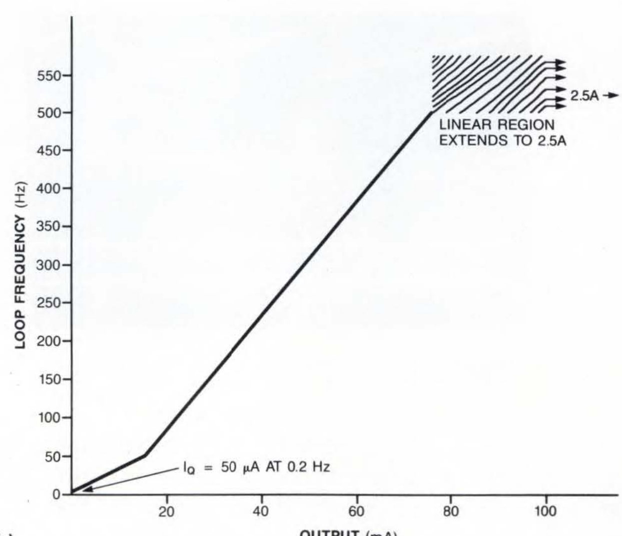
This inverter output transition pulls the V_C pin high and turns on the LT1070. The V_{SW} pin pulses the inductor at the 40-kHz clock rate, abruptly increasing the circuit's output. This transition triggers IC_1 low and forces the V_C pin back into the shutdown mode. This bang-bang control loop keeps the 12V output within the 20-mV ramp-hysteresis window set by R_3 and R_4. Diode clamps prevent any overdrive at the V_C pin. Note that the 4- to 5-sec loop-oscillation period minimizes the significance of the R_6-C_2 time constant at V_C. Because the LT1070 spends most of the time in a shutdown mode, the circuit draws very little quiescent current.

Fig 3c shows the same waveforms for a 3-mA load current. The loop-oscillation frequency increases to keep up with the load's sink-current demands. The V_C pin's waveform (trace C) now begins to take on a filtered appearance, thanks to R_6-C_2's 10-msec time constant. If the load continues to increase, the loop-oscillation frequency will also increase. The Ris fixed, however. Above some frequency, therefore, the R_6-C_2



TRACE	VERTICAL	HORIZONTAL
A	0.02V/DIV	20 μSEC/DIV
B	5V/DIV	20 μSEC/DIV
C	2V/DIV	20 μSEC/DIV
D	10V/DIV	20 μSEC/DIV

(a)



(b)

Fig 4—When you look at the waveforms for a 1A load, *you see that the V_C pin is at dc and the repetition rate now equals the LT1070's 40-kHz clock frequency* ***(a)****. As the loading increases* ***(b)****, the loop oscillates at a higher frequency because of C_1's decreased decay time.*

network must average loop oscillations to dc.

When you look at the waveforms for a 1A load **(Fig 4a),** you see that the V_C pin is at dc and the repetition rate now equals the LT1070's 40-kHz clock frequency. **Fig 4b** plots what's happening. As the output current rises, the loop-oscillation frequency also increases until it reaches approximately 500 Hz. At 500 Hz, the R_6-C_2 time constant filters the V_C pin to dc, and the LT1070 goes into normal operation. When the V_C pin is at dc, it's convenient to think of **Fig 3a**'s IC_1 and the inverters as a linear error amplifier with a closed-loop gain set by the R_1-R_2 feedback divider. Actually, IC_1 is still duty-cycle modulating, but it's doing so at a rate far above R_6-C_2's break frequency. The R_6-C_2 roll-off plus the R_7-C_3 network dominate the phase-error contribution from C_1 (which was selected for low loop frequency at low output currents). The loop is stable, and it responds linearly for all loads greater than 80 mA. In this high-current region, the LT1070 is actually fooled into behaving as it does in **Fig 2**'s circuit.

Simplifications give insight into loop's stability

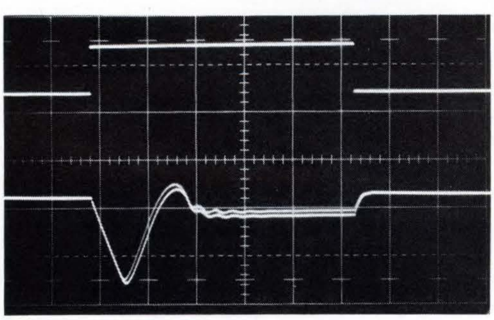
Performing a formal stability analysis for this circuit is quite complex, but some simplifications can provide insight into the loop's operation. When the load current is 100 µA, C_1 and the load resistance form a decay time constant that exceeds 300 sec. This value is larger by several orders of magnitude than the R_7-C_3 and R_6-C_2 time constants or the LT1070's 40-kHz commutation rate. As a result, C_1 dominates the loop.

Wideband amplifier IC_1 sees phase-shifted feedback that develops very-low-frequency oscillations similar to those that occur in **Fig 3b.** Some layouts may require substantial trace area for IC_1's inputs. In such cases, the optional 10-pF capacitor shown in **Fig 2a** ensures clean transitions at IC_1's output. Although C_1 has a long *decay* time constant, it has a short *charge* time constant because the circuit has a low source impedance. These disparate time constants account for the ramp-like nature of the oscillations.

You can reduce the C_1 load's time constant by increasing the loading. As the loading increases **(Fig 4b),** the loop oscillates at a higher frequency because of C_1's decreased decay time. When the load impedance becomes low enough, C_1's decay time constant ceases to dominate the loop and passes control to the R_6-C_2 combination. Once R_6 and C_2 take over as the dominant time constant, the loop begins to behave as a linear system does.

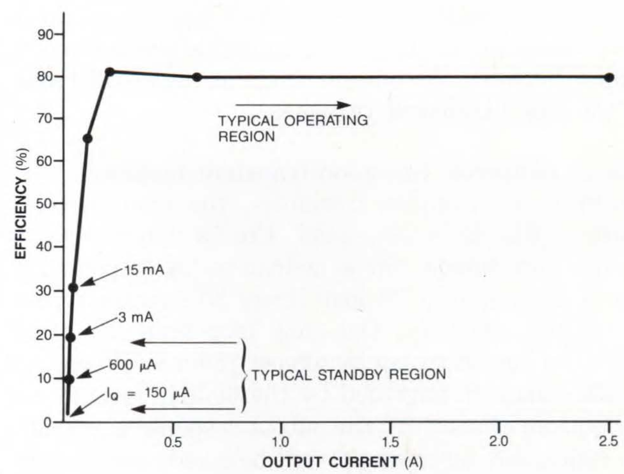
In the region above 75 mA, the LT1070 runs continuously at its 40-kHz clock rate. Now the R_7-C_3 time constant becomes significant, and it acts as a simple feedback lead to smooth the output response.

Selecting values for R_7 and C_3 involves a fundamental tradeoff. When the converter is running in its linear



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	5 mSEC/DIV
B	0.1V/DIV (AC COUPLED)	5 mSEC/DIV

(a)



(b)

Fig 5—Despite the complex dynamics inherent in Fig 3, *the transient response for a no-load-to-1A step* ***(a)*** *is quite good. When you look at the converter's efficiency performance* ***(b),*** *you'll note that the converter's high-power efficiency matches that of standard converters, and its low-power efficiency is somewhat better than that available from standard converters.*

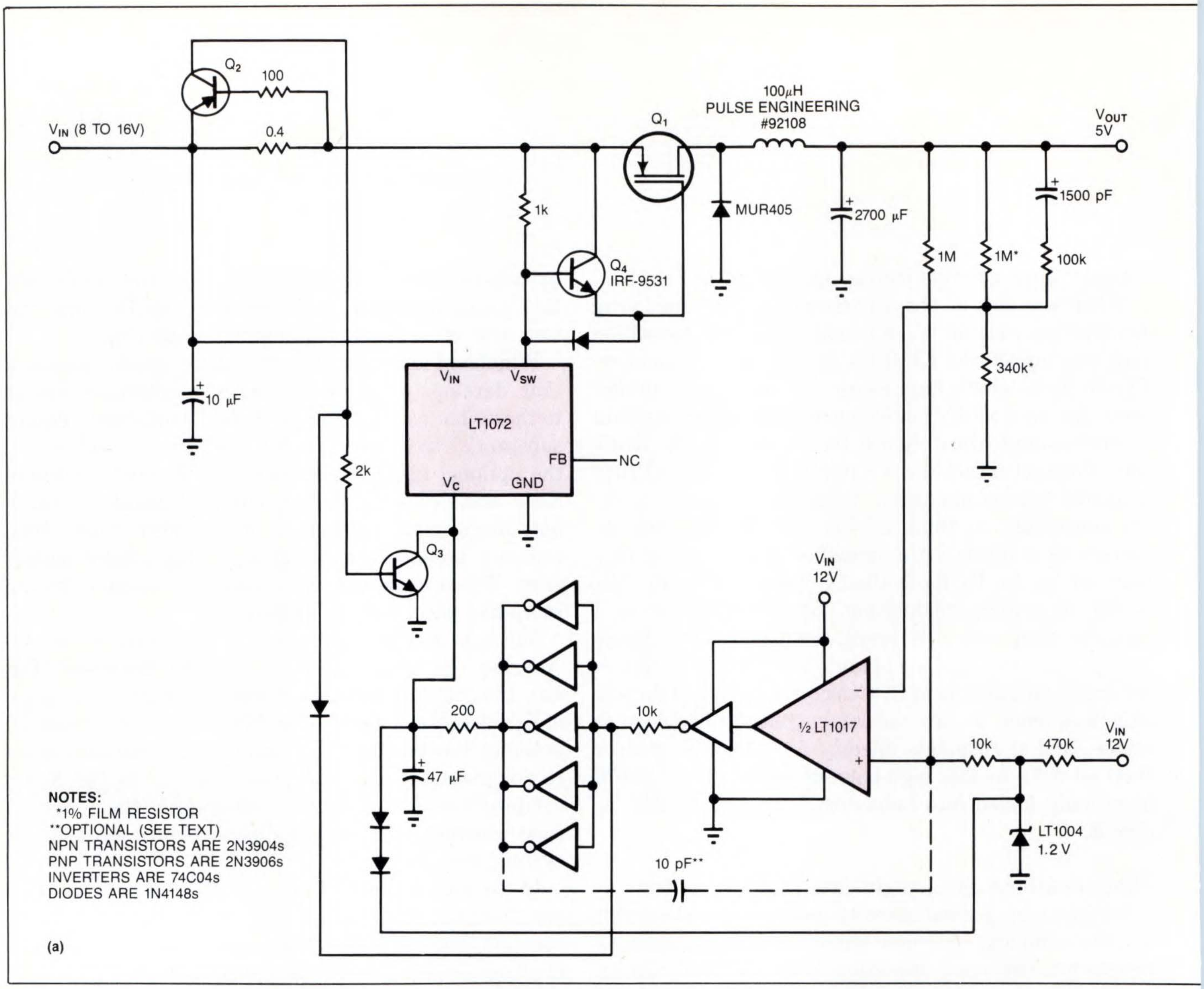


Fig 6—Using the special loop technique to introduce conditional instability *works just as well in step-down converters* ***(a)****. In transformer-coupled converters* ***(b)****, you can use the loop technique to develop multiple outputs.*

region, R_7 and C_3 must dominate the designed-in dc hysteresis generated by R_3-R_4. As a result, you must select values for R_7 and C_3 that provide the best compromise between the output ripple at high load levels and the loop's transient response.

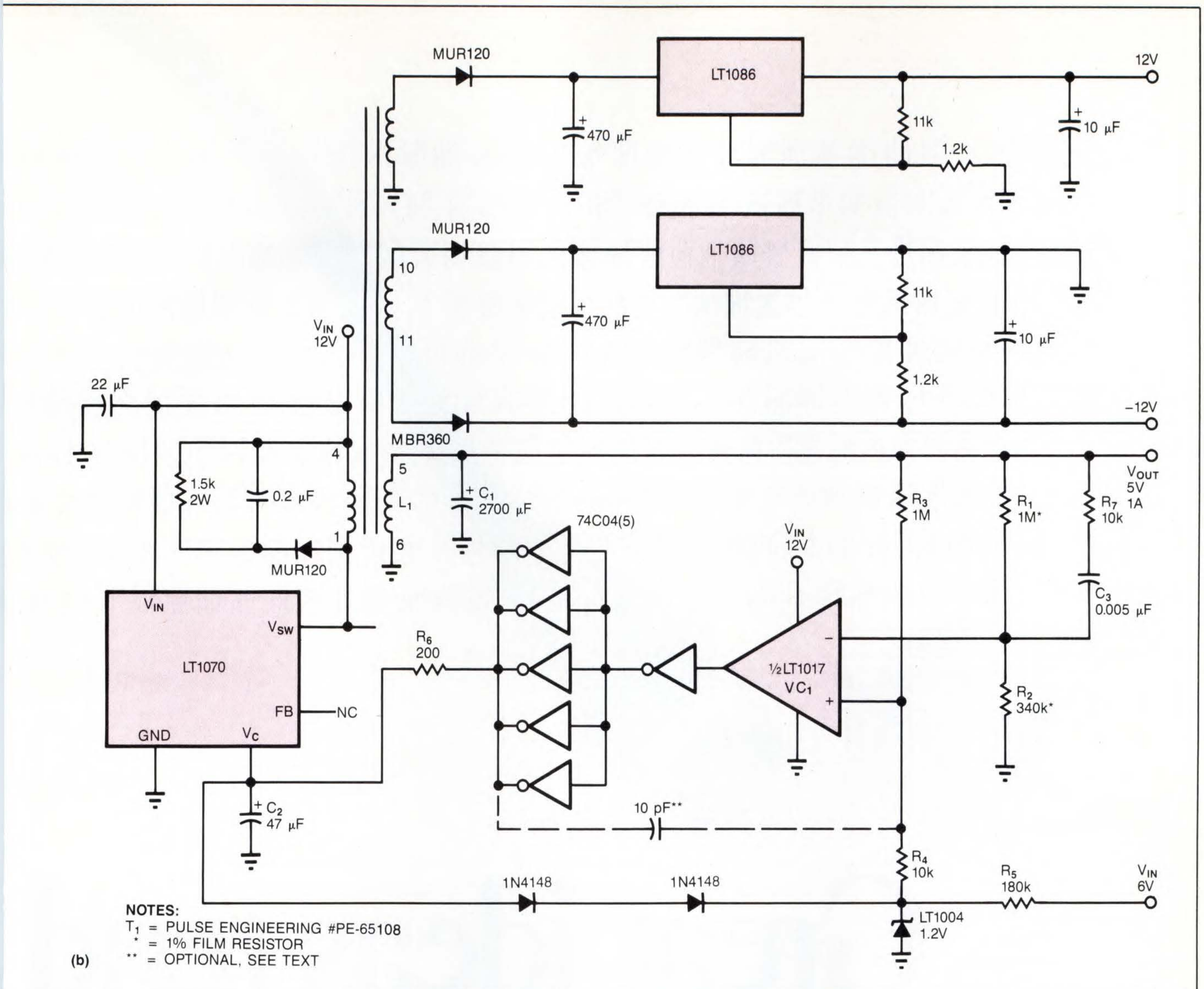
Flyback converter has good transient response

Despite the complex dynamics, the transient response of **Fig 3a** is very good. **Fig 5a** illustrates the circuit's performance for a no-load-to-1A step. When trace A goes high, a 1A load (trace B) appears across the output. Initially, the slow loop-response time causes the output to sag by almost 150 mV. When the LT1070 comes on (signaled by the 40-kHz fuzz at the very bottom of trace B), the output response is reasonably quick and surprisingly well behaved, considering the circuit dynamics. The multitime-constant decay (or rattling) shows up as trace B approaches steady state between the fourth and fifth vertical divisions.

Fig 5b plots efficiency versus output current for **Fig 3a**'s circuit. The circuit's high-power efficiency matches that of standard converters. Its low-power efficiency is somewhat better than that available with standard converters. Its standby efficiency is rather low, but that fact is not particularly bothersome, because the power loss approaches battery self-discharge levels.

The special loop in **Fig 3a** provides a controlled, conditional instability, rather than the usually more desirable and often elusive unconditional stability. This deliberately introduced characteristic lowers the converter's quiescent current by a factor of 60 without sacrificing high-power performance. This special loop technique is not restricted to boost-type converters—it will readily work in other designs.

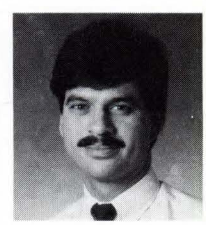
The step-down (buck-mode) configuration in **Fig 6a,** for example, uses the same basic loop and most of the same components. The LT1072 (a low-power version of the LT1070) drives Q_1 (a p-channel MOSFET) to convert a 12V input to a 5V output. Q_2 and Q_3 provide current limiting, and Q_4 supplies turn-off drive for Q_1. **Fig 6a**'s hysteresis biasing (the 1-MΩ resistor at the comparator's noninverting input) differs slightly from



that of **Fig 2a** because of the lower output voltage. In other respects, the loop and its performance are identical to those of **Fig 2a.** **Fig 6b** shows how you can use this loop concept in a transformer-coupled converter. Note that the floating secondaries allow the circuit to generate a ±12V output. EDN

Authors' biographies

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



Brian Huffman is an applications engineer at Linear Technology Corp. A member of the IEEE, he holds a BSET degree from Indiana State University and an MSEE from Santa Clara University. In his spare time, Brian enjoys plays, concerts, and the beach, and he likes to travel.

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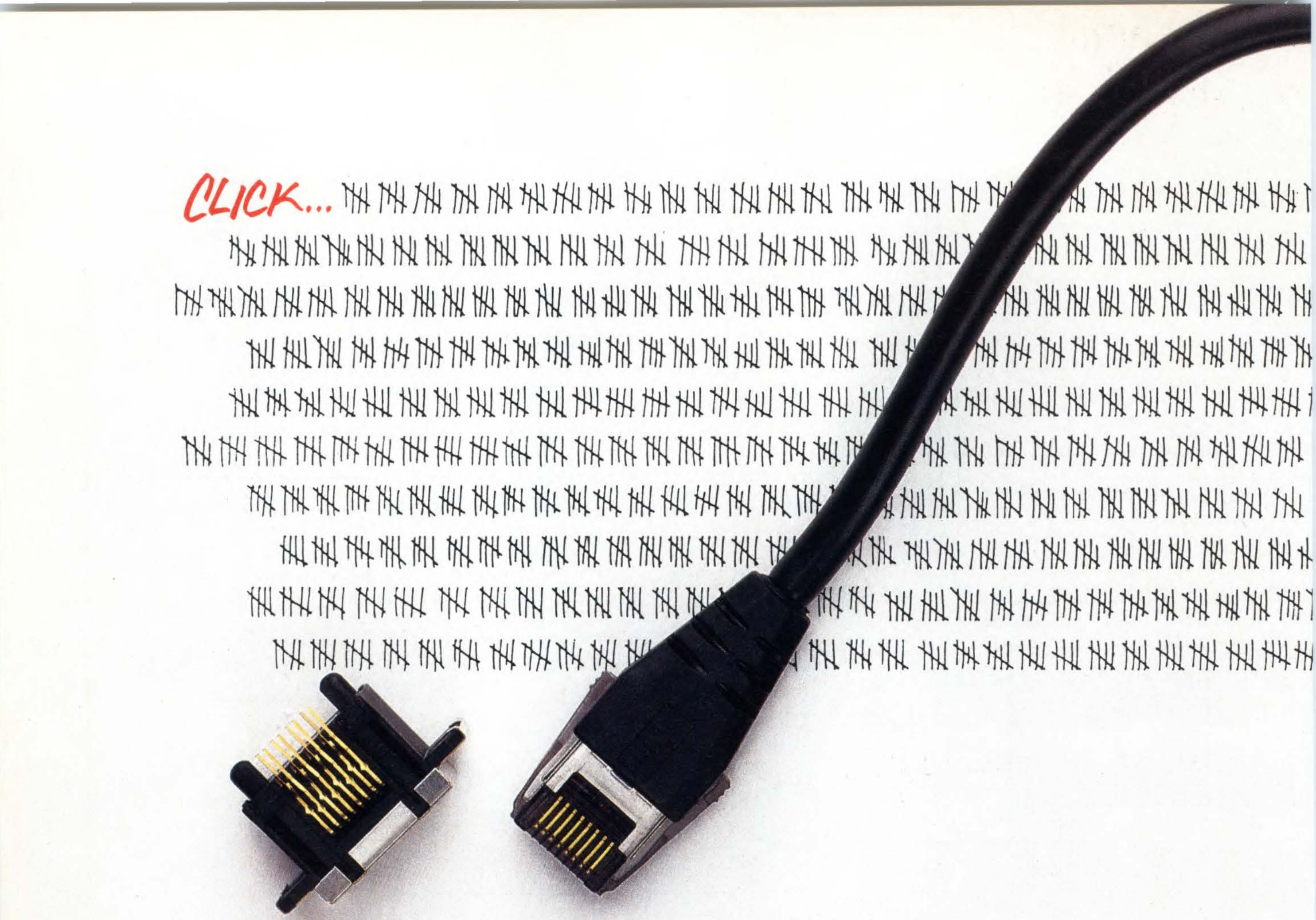

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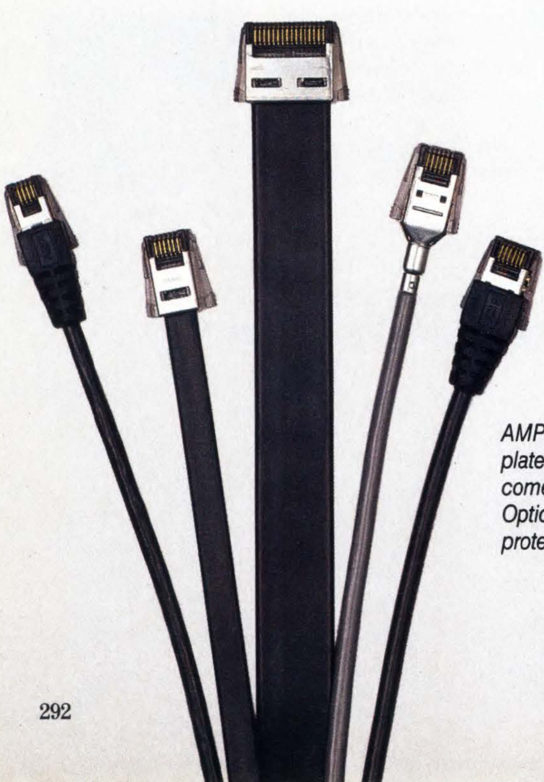

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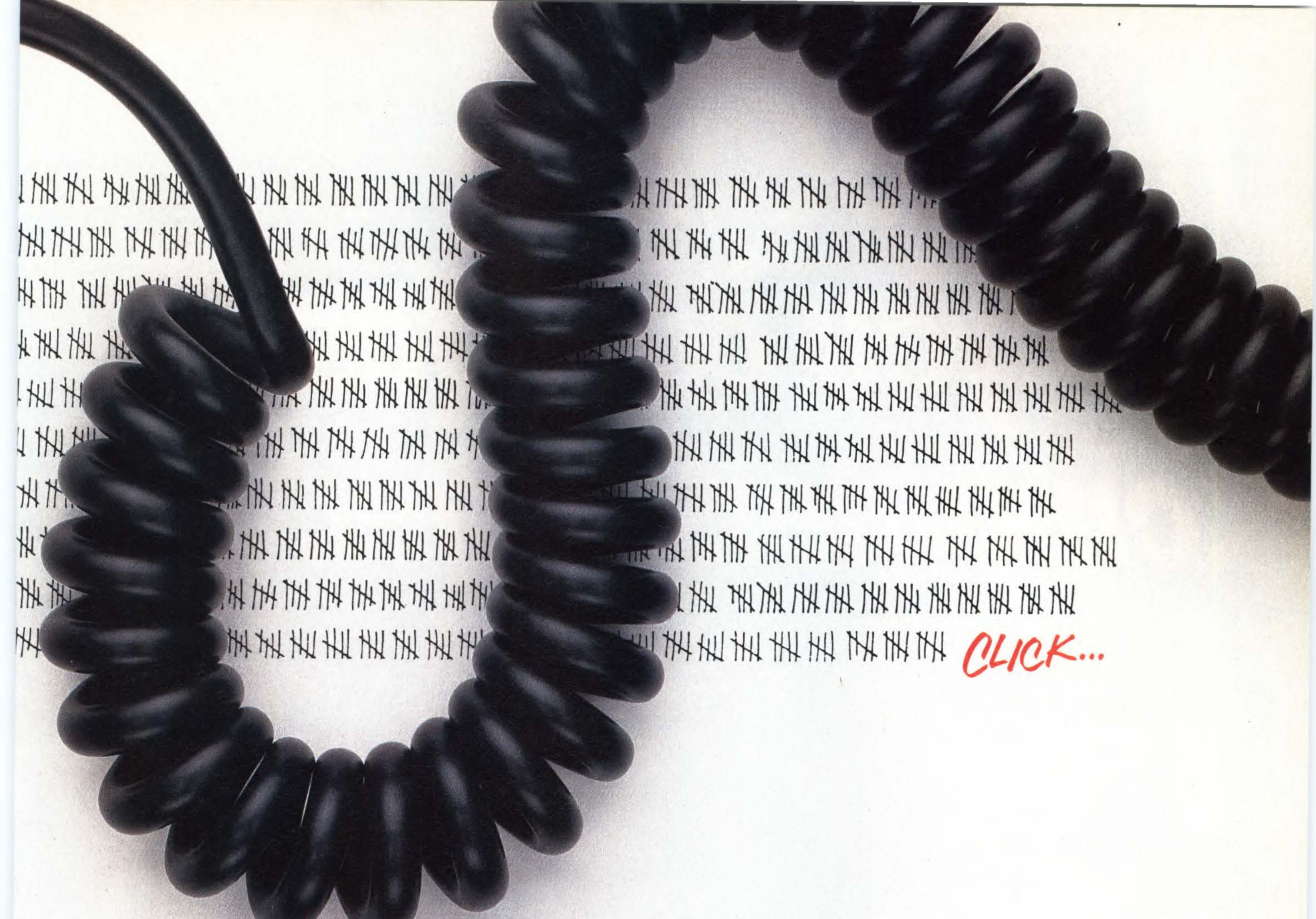

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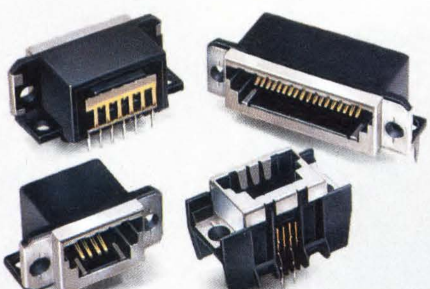

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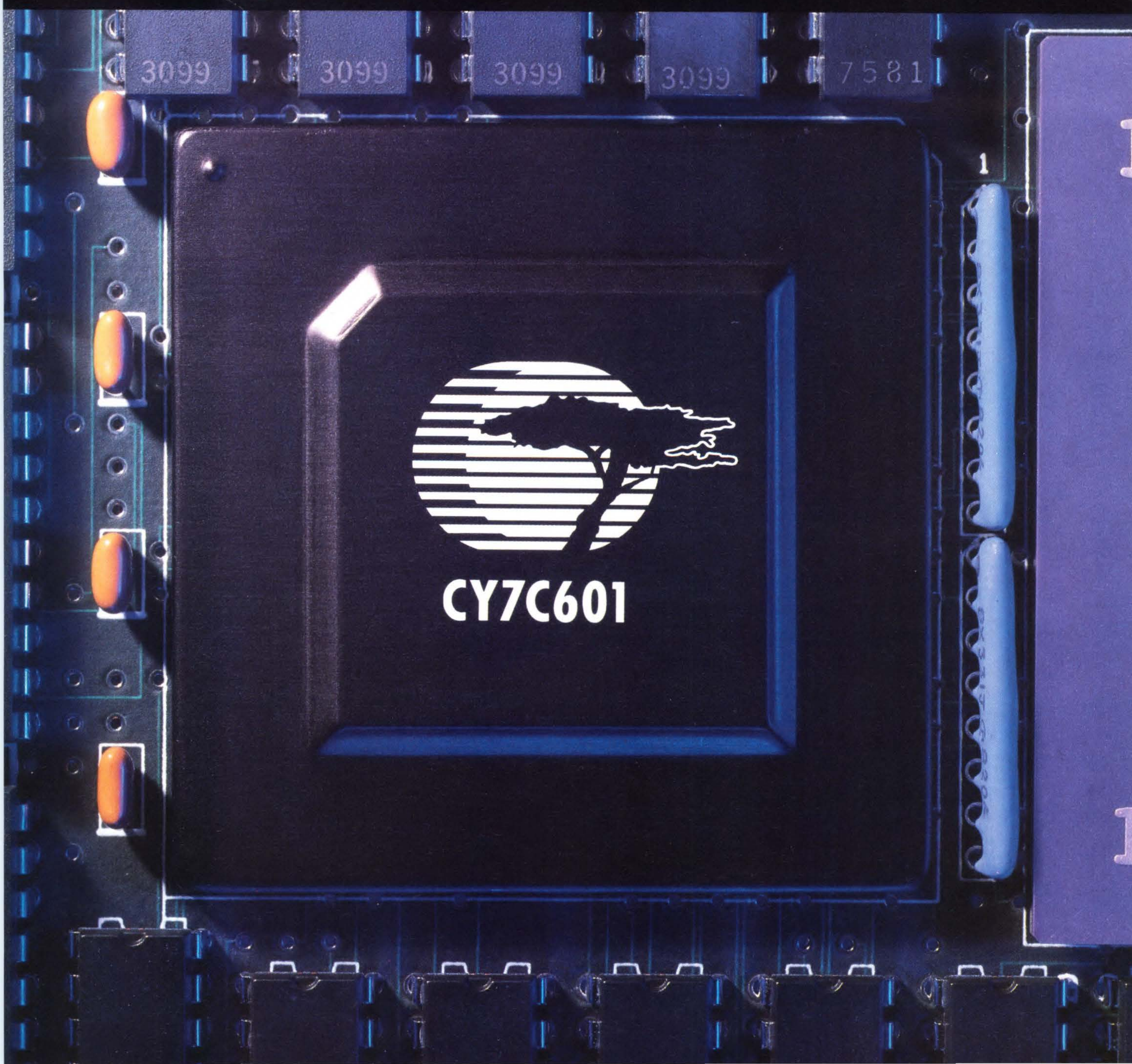

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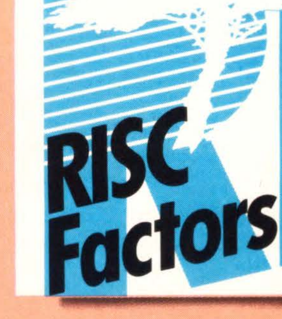

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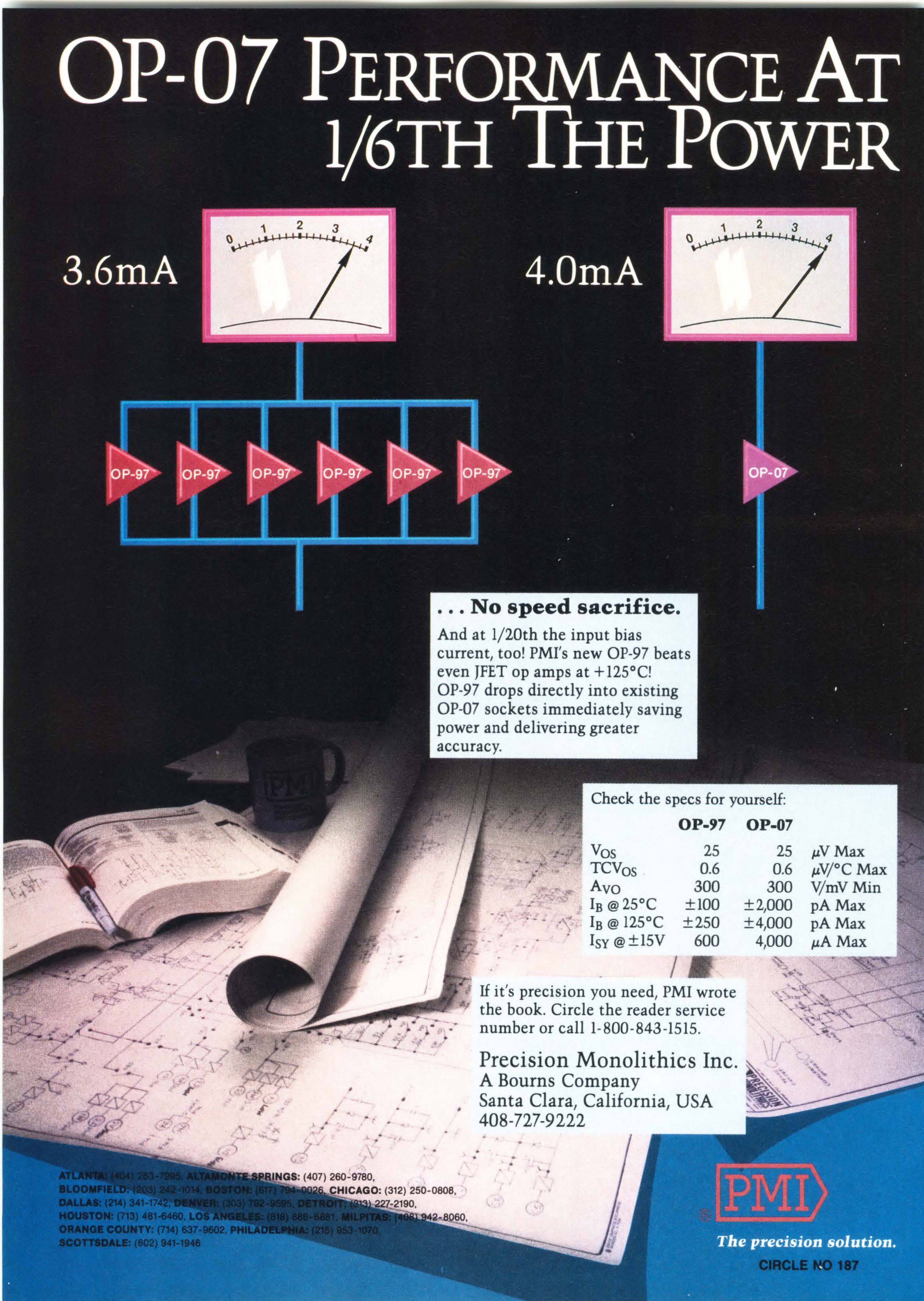
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CIRCLE NO 187

Use npn and pnp devices effectively in semicustom arrays

Although accustomed to using npn and pnp transistors of equivalent performance, many analog-circuit designers have difficulty with the lower performance pnp transistors usually found in semicustom arrays. Yet you can in fact use a combination of npn and pnp devices in a variety of useful circuits.

Winthrop Gross, *Tektronix, Inc*

Although practically all semicustom analog arrays contain both npn and pnp transistors, pnp devices perform poorly in comparison with their npn counterparts. *Lateral* pnp transistors commonly found in analog arrays exhibit low beta (current-transfer ratio) and a low transition frequency (f_T). *Substrate* pnp transistors in analog arrays perform somewhat better than the lateral ones do, but because of their basic construction, you can only use substrate vertical pnp transistors as emitter followers. In spite of these limitations, however, you can often find innovative ways to use these pnp devices. In other cases, you can construct adequate—and sometimes superior—substitutes for pnp transistors by using additional npn types.

Such extravagance is unthinkable in discrete circuits where every component costs money. With a semicustom array, however, the incremental cost of adding extra devices is negligible, which makes the pnp transistors in analog arrays like Tektronix's QuickChip 2 and QuickChip 6 more useful than they at first appear. In fact, you can use these pnp devices (as well as npn types) as dc level shifters, current sources, compound devices, and output drivers, but in order to do so, you need to be familiar with the basic characteristics of these transistors.

Lateral pnp devices have two p-type implants

Lateral pnp transistors are formed by placing two p-type implant regions adjacent to, but not touching, each other. Because the epitaxial layer is an n-type, the p-type implants are separated laterally by an n-type region. This construction forms a pnp transistor in which the current flow runs parallel to the surface of the die. A combination of geometry, feature size, and doping profiles determine the characteristic of any given transistor. Unfortunately, the implants used for the lateral pnp are actually spare parts left over from the npn devices, and the feature sizes are large. Unless the process engineers add mask and implant steps (at considerable expense), they have no latitude with which to optimize the pnp transistors' performance levels. Consequently, the IC designer has to take what he can get.

The SH3 process used to fabricate the QuickChip 2 and QuickChip 4 has a heavily doped epitaxial layer to maximize the speed of the npn devices. As a result, however, the emitter of the lateral pnp can't efficiently inject minority carriers into its base. Thus the transis-

In contrast to discrete designs, the use of additional devices to improve performance does not usually mean more cost for semicustom arrays.

tors have an extremely low pnp beta—SH3 lateral pnp transistors have typical peak betas of 7. What's more, the beta drops rapidly as the current increases; at 1 mA, for example, the beta can drop to as low as 1. As you might expect, these transistors are also relatively slow. The transition frequency, f_T, is only about 20 MHz—more than two orders of magnitude lower than the 6.5-GHz performance of the npn types.

Substrate pnp transistors are so named because they use the p-type substrate material as the collector. Instead of two adjacent p-type implants, as in the lateral device, the substrate transistors use a single p-type implant for the emitter. Again, the n-type epitaxial region forms the base, but the current flow is vertical. Because the epitaxial region on the SH3 process is only 3 μm, substrate pnp transistors are somewhat faster (100 MHz f_T) and have higher beta (75) than do their lateral equivalents. The problem with the vertical type of pnp transistor is that its collector is connected to the substrate, which is common to all devices on the IC and which must be biased to the most negative voltage in the circuit. Consequently, all substrate pnp transistors share a common collector and are only useful as emitter followers.

Low-performance pnp devices have some pluses

Clearly then, SH3 pnp transistors have limited use in high-performance signal paths, but they do have some advantages. For example, both the lateral and substrate transistors have reasonably high breakdown voltages. Breakdown voltages are all >10V for such parameters as BV_{CBO}, LV_{CEO}, and BV_{EBO}. The lateral pnp devices' Early voltage is high, and its collector-base capacitance is low; together those voltage and capacitance values result in a high output impedance. The V_{be} matching ($\sigma(\Delta V_{BE})$~0.5 mV) is also excellent for both devices.

Level shifting can be a problem

An obvious problem with all-npn signal paths is level shifting. As the signal progresses through cascaded npn amplifier stages, the dc level inevitably rises. To compensate, you can use one of several techniques that negatively shift dc levels and yet maintain dc coupling and wide bandwidth.

The simplest level shifter is an emitter follower. Emitter followers are especially useful in SH3 chips because the npn devices retain their high f_T at low collector-base voltages. A common-emitter amplifier (Q_1) driving an emitter-follower (**Fig 1**) can operate at $V_{CE}=1.6V$, and the combination exhibits no change in the dc level. The f_T of the common-emitter device is greater than 6 GHz. The major disadvantage of the emitter-follower level shifter (other than its small voltage change) is temperature drift, which is typically −1.8 mV/°C.

Diode strings are useful

You can of course use diode strings for level shifting. You can form signal diodes from npn transistors by shorting the base to the collector. The disadvantages of diode level shifting are the large temperature coeffi-

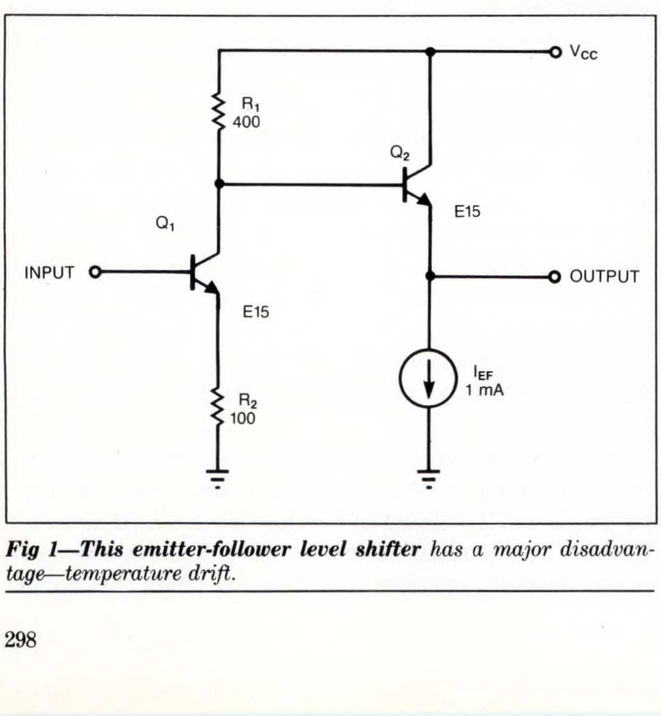

***Fig 1—This emitter-follower level shifter** has a major disadvantage—temperature drift.*

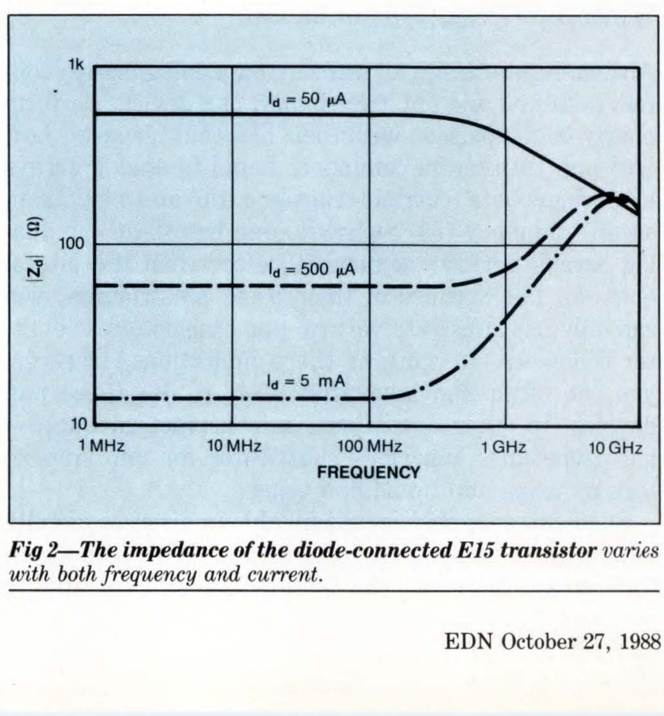

***Fig 2—The impedance of the diode-connected E15 transistor** varies with both frequency and current.*

cient of voltage (-1.8 mV/°C per diode) and the diode impedance, which can affect the speed of the circuit. The impedance (Z_d) is:

$$Z_d \approx \frac{KT}{qI_d} + r_e + \frac{r_{bb'}}{\beta} \times \frac{s\beta\tau_t + 1}{s\tau_t + 1},$$

where r_e and r_{bb} are the transistor's emitter and base resistances, respectively; s is jω; τ_t is the base transit time; β is the forward-current gain; and I_d is the diode current. Examination of this equation shows that the diode impedance is inductive in the region defined by:

$$1/\beta\tau_t < \omega < 1/\tau_t.$$

Fig 2 plots Z_d versus frequency for a diode-connected E15 transistor from a QuickChip 2 IC at several current levels.

For noninteger multiples of V_{BE}, or when devices are scarce, the V_{BE} multiplier circuit of **Fig 3** is useful. The voltage drop obtained with this circuit (ignoring β) is:

$$V_d = \frac{R_1 + R_2}{R_2}(V_{BE}).$$

Because of the soft knee in its voltage-current characteristic, this circuit requires a minimum value of current I_{bias} to work properly:

$$I_{bias} > V_{BE}/R_2.$$

The circuit must satisfy this minimum bias current over temperature extremes and process variances. Note that the worst-case situation occurs at low temperatures, when V_{BE} is maximum, and when R_2 is minimum. The dc impedance, Z_d, of the V_{BE} multiplier is:

$$Z_d \approx [\beta(R_1 + R_2) + gmR_1R_2] \times \frac{r_e + \frac{1}{gm}}{\beta\left(R_2 + \frac{1}{gm}\right)}.$$

The V_{BE} multiplier is similar to a string of diodes in operation: The voltage temperature coefficient is about -1.8 mV/°C per V_{BE} of V_d, and the impedance has an inductive component. **Fig 4** plots Z_d versus frequency for the V_{BE} multiplier in **Fig 3**. You can lower the high-frequency impedance of the V_{BE} multiplier by adding capacitance from the collector to the base of the transistor. **Fig 5** shows the effect of this added capacitance.

Zener diodes also shift levels

Another simple level-shifting device is a zener diode. You can make zener diodes on single-layer-metal QuickChip 2s by shorting the collector to the emitter and using the emitter-base breakdown voltage of the transistor. The emitter-base breakdown voltage is 5.7 ± 0.3V at 50 μA/μm of emitter length. The TC of this breakdown voltage is approximately 1 mV/°C.

The advantages of zener level shifting are simplicity and high speed. The zener-connected npn has low dy-

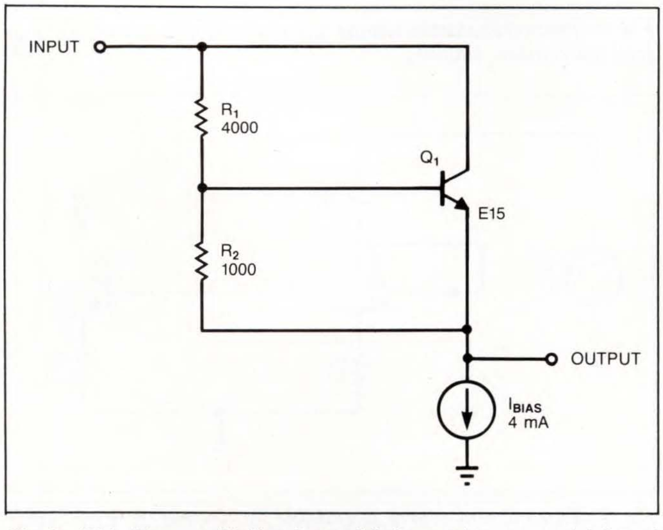

Fig 3—This V_{BE} multiplier is useful *for noninteger multiples of V_{BE} or when available devices are scarce.*

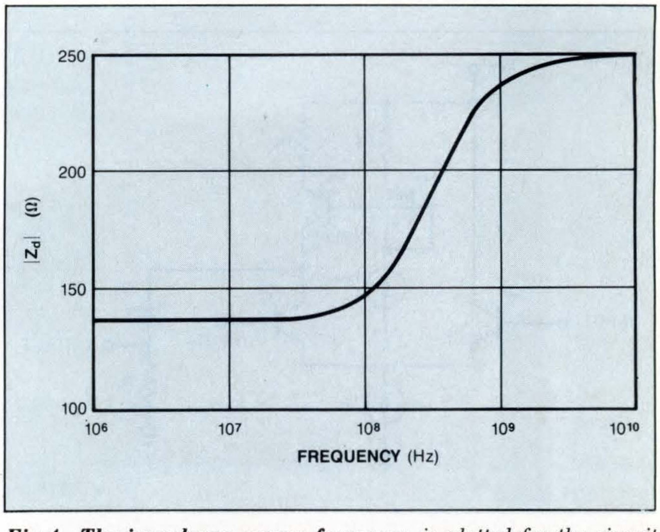

Fig 4—The impedance versus frequency *is plotted for the circuit in **Fig 3**.*

The lateral and substrate pnp transistors on analog arrays exhibit low betas and low transition frequencies.

namic impedance because there is considerable capacitance shunting the junction and little resistance in series with it. The QuickChip 2 library includes a model of an E15 device used as a zener diode, which accurately models dynamic impedance and temperature effects.

The disadvantages of zener-diode level shifting are that level shifts are only possible in increments of 5.7V, and that zener diodes are inherently noisy. (The QuickChip 2 library includes an equivalent zener-diode model, although you should consider the results obtained only approximate.) SH3 zener diodes typically have an equivalent noise resistance of 66 kΩ. A good way to avoid zener noise problems is to level shift from a high-impedance source. **Fig 6** illustrates this technique. The lateral pnp transistors found on SH3 chips are useful for this type of circuit because they have low output capacitance.

Fig 7 shows yet another level-shifting technique that has the low noise and flexibility of a V_{BE} multiplier and good temperature stability. Capacitor C_1 optimizes the frequency response through the level shifter as in the V_{BE} multiplier. For temperature stability, the voltage across resistor R_D should obey the relation:

$$V_{R_D} = V_d - V_{B_E}.$$

The V_{BE} term makes this relation temperature-dependent. And I_{RD} should have the correct temperature- and resistor-dependence. That is:

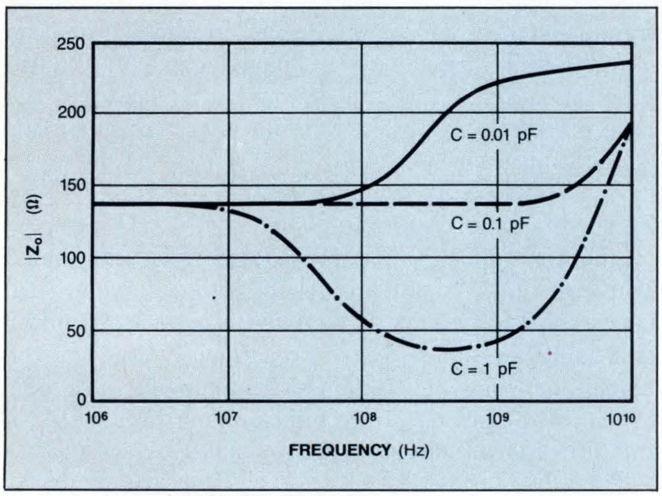

***Fig 5—The impedance of the V_{BE} multiplier** in **Fig 3** is affected by the circuit's total collector-base capacitance.*

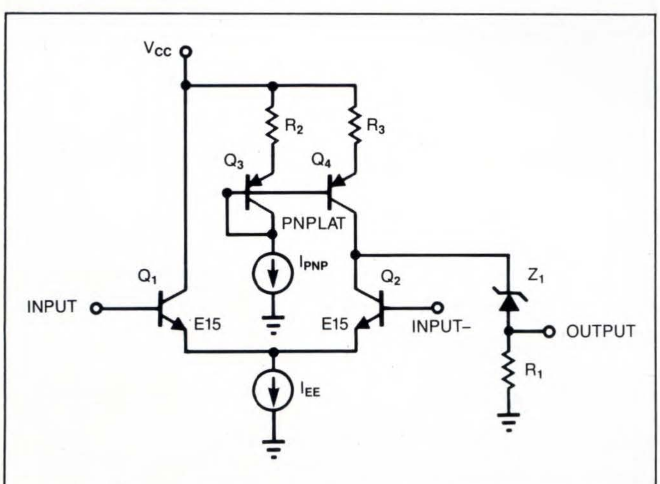

***Fig 6—A zener-diode level shifter** is driven from a high impedance source.*

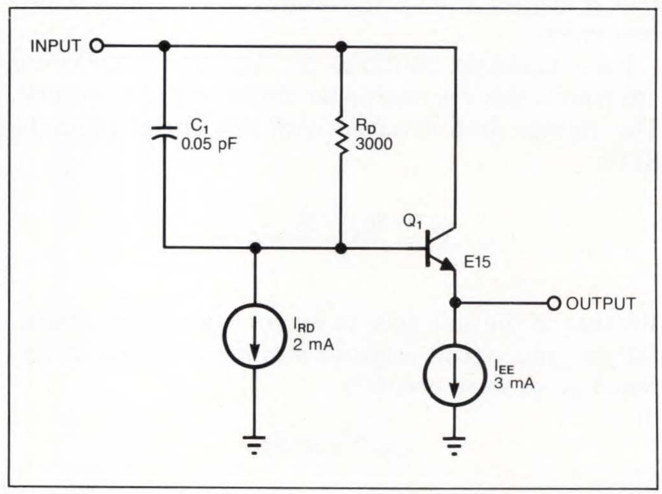

***Fig 7—This level-shifter circuit** has low dynamic impedance and good temperature stability.*

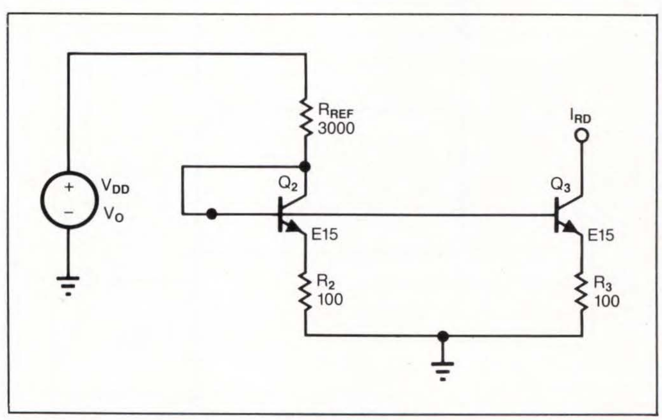

***Fig 8—This current source is suitable** for driving the level shifter in **Fig 7**. You can use multiple current sources to drive additional level shifters.*

$$I_{R_D} = (V_d - V_{BE})/R_D,$$

You can easily establish these temperature dependencies with the simplest of current mirrors (see **Fig 8**). The design of the voltage source V_{dd} should provide a constant voltage equal to V_d across the reference string (R_{REF} and Q_1). You should make R_{REF} from the same implant or thin film as R_D in **Fig 7**. If you use a 1:n mirror, then $R_{REF} = nR_D$.

Although QuickChip 2 lateral pnp transistors are useful as current sources, you must take their low β into consideration. For example, the simple current mirror in **Fig 9** has a large error due to the pnp's low β. In that circuit, the output current is:

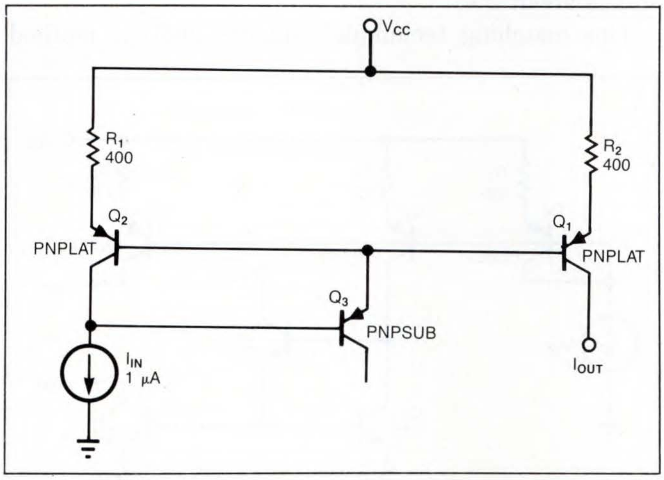

Fig 9—Because of the low beta of the lateral pnp devices, *this simple pnp current mirror has an output-current error of about 4%.*

$$I_{OUT} = \frac{I_{IN}}{1 + \dfrac{1/\beta_{Q_1} + 1/\beta_{Q_2}}{\beta_{Q_3} + 1}}.$$

At best, the SH3 lateral pnp devices in such a mirror produces an error of about 4%. If the base current from the lateral pnp is less than about 1 mA, then Q_3 is a good place to use a substrate pnp, which has a much higher β than the lateral transistors.

Several techniques can improve the performance of pnp current sources. For example, the Darlington connection turns out to be a bargain at low β because the term β_D is usually ignored in the expression for Darlington current gain:

$$\beta_D = \beta^2 + 2\beta.$$

Even at a device β of 1, the current gain of the Darlington connection is 3.

You also have the option of using a more sophisticated control amplifier in place of the substrate pnp Q_3 (**Fig 10**). This circuit is particularly useful for controlling relatively high-current pnp sources (greater than 1 mA of the total base current). The npn differential pair can sink more pnp base current than a substrate pnp can. An additional advantage is that pnp

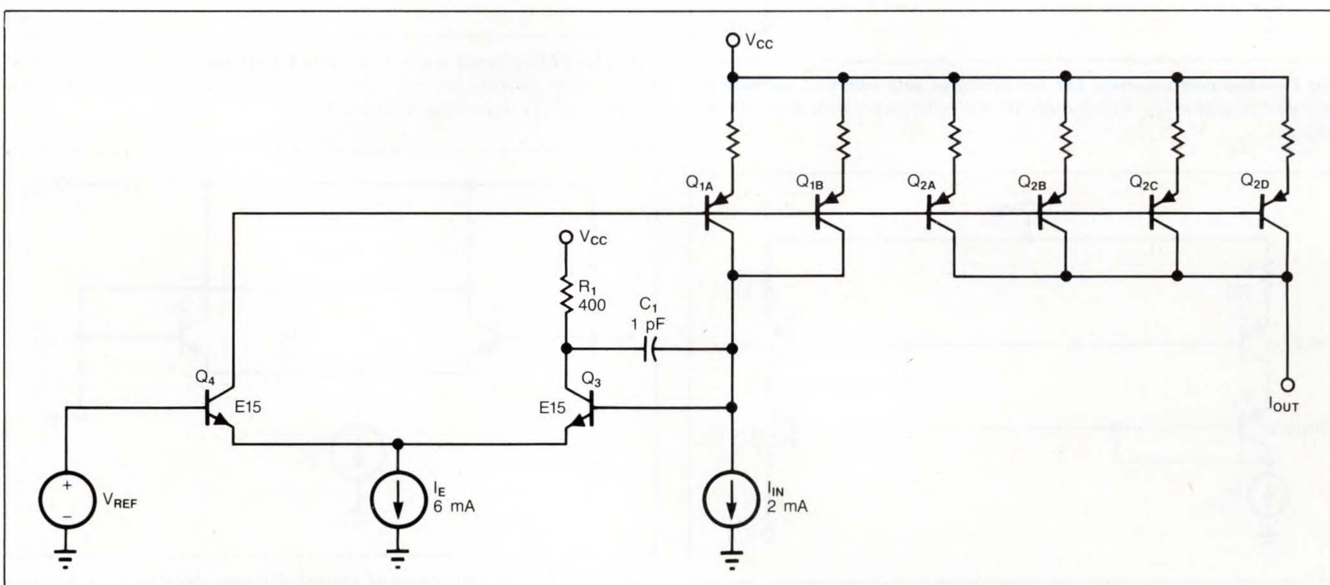

Fig 10—This pnp current source uses *an npn control amplifier. This circuit is useful for controlling relatively high-current pnp sources.*

Although they have low beta, lateral pnp transistors are okay in designs of a current mirror that have only a moderate error.

base current does not have to return to substrate potential, so you may be able to save power. Capacitor C_1 provides stability; a single QuickChip 2 capacitor section should be adequate. To minimize VA effects in the pnp devices, you should make V_{REF} equal to the nominal voltage at the current-source output.

Fig 11 illustrates another way to improve the accuracy of pnp current mirrors. The helper transistor, Q_3, adds its collector current to the mirror output. This mirror has essentially perfect accuracy at two values of beta: infinite and 1. You also should not overlook the Wilson current source **(Fig 12)**, which has high output impedance and slightly improved accuracy at low beta. The output current for the Wilson current mirror is:

$$I_{OUT} = \frac{I_{IN}}{\dfrac{\beta+1}{\beta+2} + \dfrac{1}{\beta}}$$

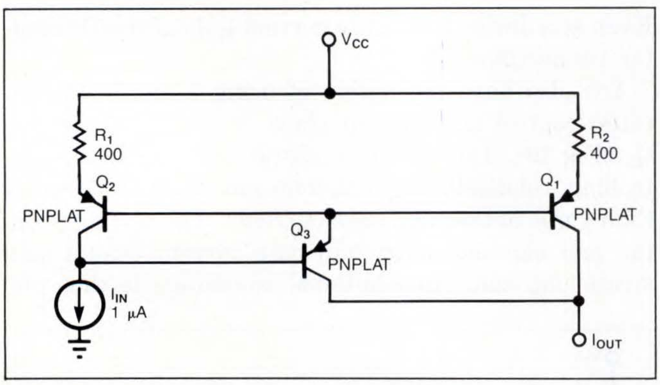

Fig 11—You can improve the accuracy of pnp current mirrors *by adding transistor Q_3, which adds its collector current to the mirror's output.*

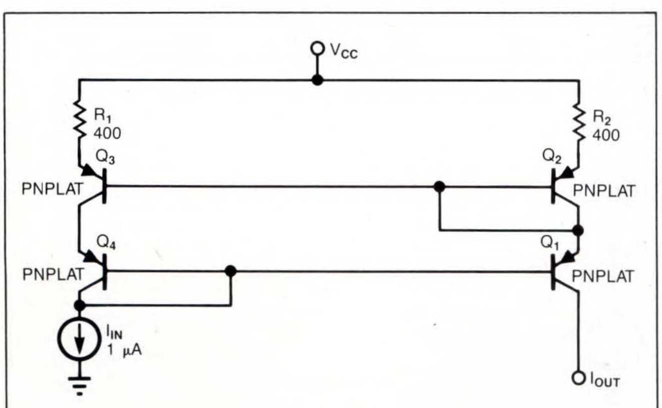

Fig 12-This Wilson current mirror *has a high output impedance and slightly improved accuracy at low beta.*

A common IC design problem is how to match a pullup (pnp) current to a pulldown (npn) current. One solution is to create a pair of matched pnp sources and to use one of the devices in the pair as the reference current for an npn mirror, as shown in **Fig 13.** Although it's difficult to accurately determine the absolute value of the pnp current sources because of their low beta, the two sources, Q_2 and Q_3, match by more than 98%. You can obtain even better matching by using Darlington-connected pnp devices. Because npn mirrors generally match by better than 99.9%, the total mismatch between the pnp source and the npn sink is about 2%.

This matching technique suggests another method

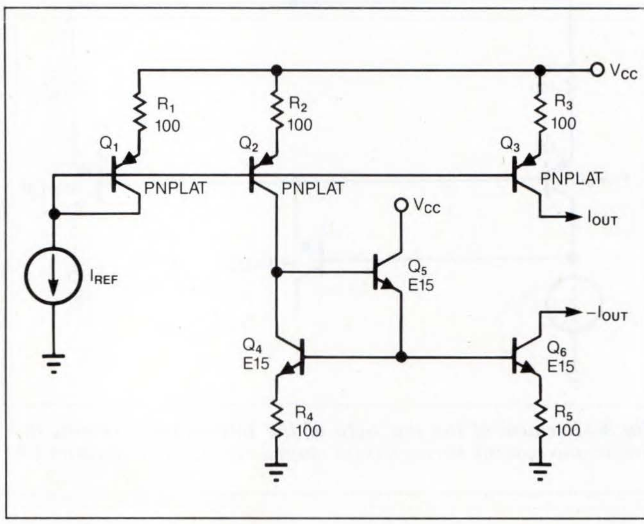

Fig 13—This circuit uses a matched pnp source *as the reference for an npn current mirror. The total mismatch between the pnp source and the npn sink is about 2%.*

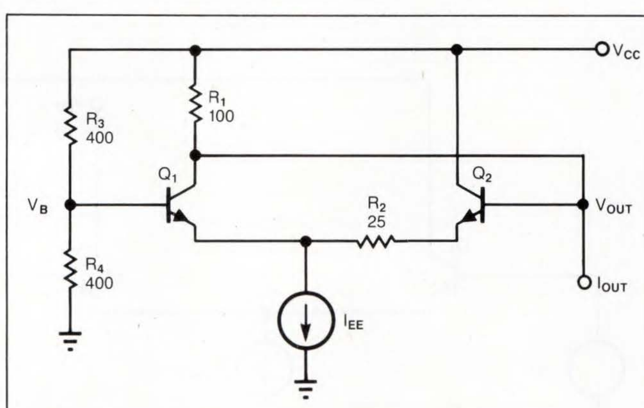

Fig 14—This all-npn current source for pnp devices *uses positive feedback to increase the impedance of R_1. A disadvantage of this circuit is its small voltage compliance, which is approximately I_ER_2.*

of providing accurate, absolute mirroring of a reference current: You can create a matched pair of pnp sources and use one source to model the other (**Fig 10**). More sophisticated npn control amplifiers than the one shown in that figure increase the accuracy of this mirror to the limit dictated by the pnp alpha mismatch. This mismatch is typically less than 1% with a current of 100 μA per pnp.

The all-npn "pnp" current source

The circuit in **Fig 14** uses positive feedback to increase the impedance of long-tail resistor, R_1. Ignoring the value of r_e for both transistors, the total I_{EEE} plus I_{OUT} current is:

$$(V_{CC}-V_{OUT})/R_1+(V_{OUT}-V_B)/R_2=I_{EE}+I_{OUT}.$$

If you set $R_2=R_1$, then:

$$I_{OUT}=(V_{CC}-V_B-I_{EE}\times R_1)/R_1,$$

which is a constant.

The differential pair, Q_1 and Q_2, has a voltage gain of 1 (R_2 must be slightly less than R_1 to account for the finite G_m of Q_1 and Q_2). A disadvantage of this circuit is the small voltage compliance (approximately I_ER_2). A tradeoff does occur between output current and compliance: As I_{EE} increases, I_{OUT} decreases and compliance increases. Because of the high f_T of SH3 npn transistors, the apparent increase in the impedance of R_1 continues through high frequencies. **Fig 15**

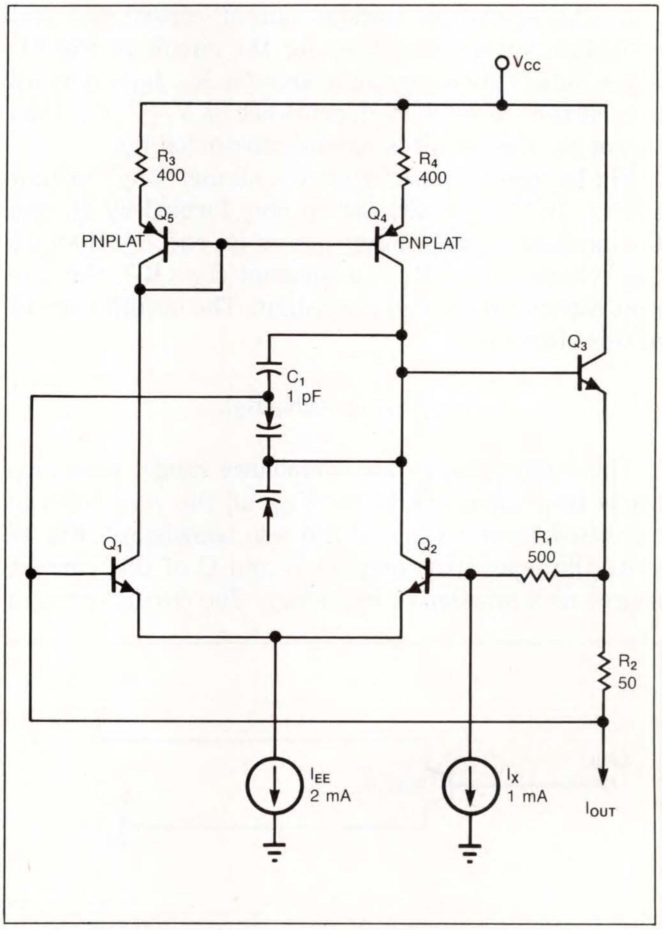

***Fig 16—This almost-all-npn current source** has a wide compliance range: from about 2V below V_{CC} down to the breakdown voltage of the npn devices.*

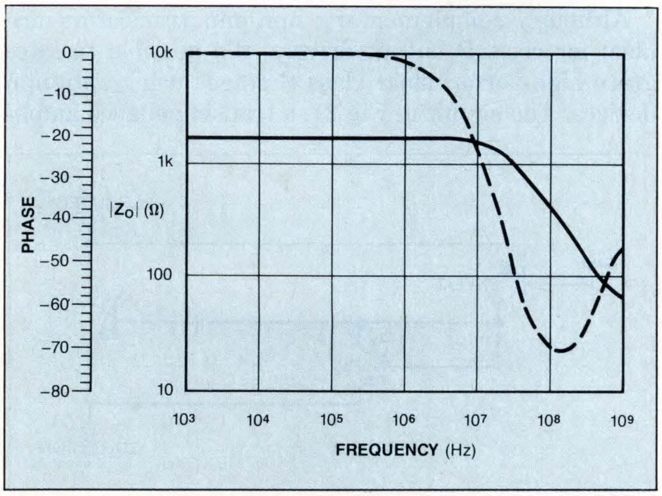

***Fig 15—Plotted here is the output impedance versus the frequency** for the circuit in **Fig 14**. The magnitude of the circuit's impedance continues through high frequencies.*

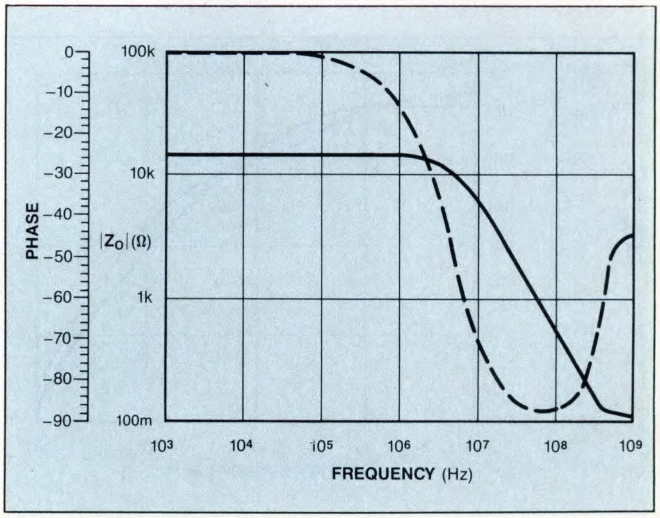

***Fig 17—This plot shows the output** impedance versus the frequency for the circuit in **Fig 16**.*

The higher beta in substrate pnp transistors makes them useful in current mirrors where the base current from the lateral device is low.

plots the equivalent parallel output capacitance and resistance versus frequency for the circuit in **Fig 14.** If you substitute a current source for R_4, I_{OUT} mirrors that current through its dependence on $V_{CC}-V_B$. Furthermore, the circuit is an anti-mirror for I_{EE}.

Fig 16 shows a superior almost-all-npn "pnp" current source. In this circuit, the op amp formed by Q_1 and Q_5 maintains equal voltage across R_1 and R_2. Because the voltage across R_1 is a constant ($I_X \times R_1$), the current through R_2 is also a constant. The output current of this circuit is:

$$I_{OUT} = I_X \times (R_1/R_2).$$

This circuit has a wide compliance range, which extends from about 2V below V_{CC} all the way down to the breakdown voltage of the npn transistors. **Fig 17** plots the equivalent parallel R and C of this current source as a function of frequency. The circuit recovers rapidly from a transient load change, aided by the feed-forward capacitor, C_1. The only disadvantage of this circuit is that the noise from current source I_x is multiplied by the ratio R_1/R_2.

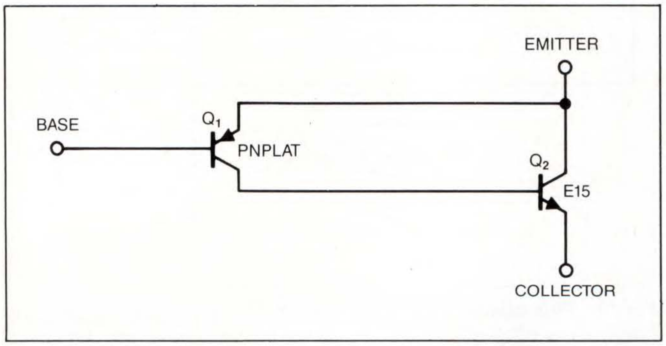

Fig 18—This compound pnp device *combines an npn transistor and a lateral pnp transistor to form a high-beta pnp equivalent.*

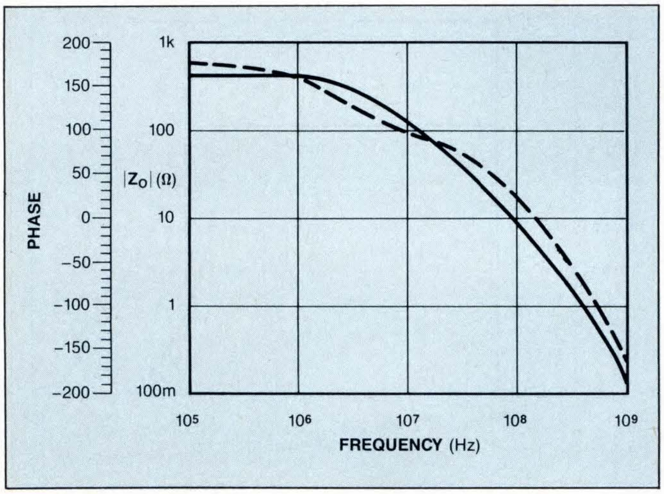

Fig 19—The compound pnp device has *an excess phase of 160°. Its equivalent delay of 1.2 nsec is undesirable in feedback circuits.*

Compound pnp devices are tricky

The compound pnp circuit (**Fig 18**) enjoys some notoriety. It combines an npn transistor and a lateral pnp transistor to make a high β pnp equivalent. The current gain, β_{eff}, is:

$$\beta_{eff} = (\beta_{NPN}+1)\beta_{PNP}.$$

Furthermore, the circuit's f_T of about 400 MHz is impressive. All this high performance may seem too good to be true, and in fact it is. For one thing, the plot of **Fig 19** shows that the excess phase of the compound pnp device is a whopping 160°—equivalent to about 1.2 nsec of delay—which is disastrous in feedback circuits. The compound pnp circuit of **Fig 18** is also intrinsically unstable under certain conditions. For example, in a common-collector (emitter-follower) operation, the loop formed by the lateral pnp transistor feeding back from the collector of the npn transistor to its base is unstable.

Although it exhibits lower beta, the compound pnp device in **Fig 20** is much better behaved. The diode, Q_3, limits the current gain of the npn section to 4. The low gain pushes the pole (contributed by the npn transistor) far enough out so that the loop is stable. The f_T of this compound pnp device is about 100 MHz; the excess phase shift is a tolerable 35°.

Although complementary npn-pnp transistors are ideal for class B output drivers, it's possible to integrate high-performance class B stages using only npn devices. The circuit in **Fig 21**, a transimpedance ampli-

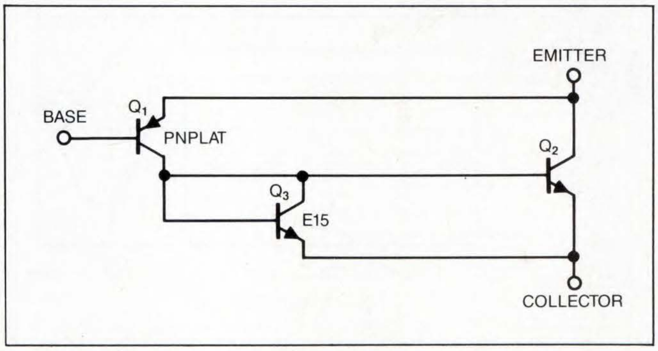

Fig 20—The presence of diode Q_3 improves *the operation of this compound pnp device. The f_T of this compound pnp is about 100 MHz, and its phase shift is a tolerable 35°.*

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CIRCLE NO 188

Because using extra npn devices on analog arrays is essentially cost-free, you can use them by themselves or with pnp devices.

fier with a gain of 12 kΩ, illustrates the basic approach. The circuit's input has a nominal dc level of $1V_{BE}$ above ground and should be driven from a current source. The low-impedance output can swing from approximately $2V_{BE}$ above ground to $1V_{BE}$ below V_{CC}. Q_1 takes care of negative going outputs; Q_2 is an emitter follower that handles the positive excursions. Q_2 derives its base drive from R_1. What makes the circuit work is D_1, which switches off Q_2 on negative excursions. Thus, the circuit acts like a class B output with the standing current determined by R_1.

Integrated node limits stray capacitance

Note that the positive slew rate of this amplifier is a function of R_1 and the effective capacitance at the base of Q_2. Because this node is integrated, the stray capacitance is low. Consequently, this output circuit is capable of fast voltage slewing. The capacitance of Q_2 is sometimes reduced further with a degenerated Darlington pair (f_T doubler) that is substituted for Q_2 when driving low-impedance loads.

Fig 22 shows a practical implementation of this circuit on an SH3 chip with overall shunt feedback and with the common base Q_3 added to cascode-connected Q_1 and with Q_4 and Q_5 added in order to speed up Q_2. Additional devices are added to the collectors of Q_4 and Q_2 to prevent LV_{CEO} breakdown. Q_9 and Q_{11} provide current limiting to control the slew rate and protect against output shorts. D_2 and D_3 minimize the voltage swing at the base of Q_4 in the transitional region between pullup and pulldown.

The quiescent power dissipation of the circuit in **Fig 22** is only 50 mW. The input's dc level is now $2V_{BE}$ above ground, and the output can swing from about $1V_{BE}$ above Q_3's base supply of 5V to about $3V_{BE}$ below the 20V V_{CC} supply. Moreover, you could easily translate the circuit to operate between 10V supplies with a level shifter, such as that in **Fig 7**, driving the input. On an SH3 chip, the **Fig 22** circuit is capable of about 12V of output swing (limited by BV_{CBO} of Q_3); on an SH-HV chip, 60V of output swing is possible.

Performance isn't always everything

Although high-performance pnp transistors are an important weapon in the discrete-circuit designer's arsenal, the advantage of having high-quality pnp devices is usually a minimum number of transistors for a particular function and not higher performance. With integrated-circuit design, the number of devices required to implement a function is not nearly as important as

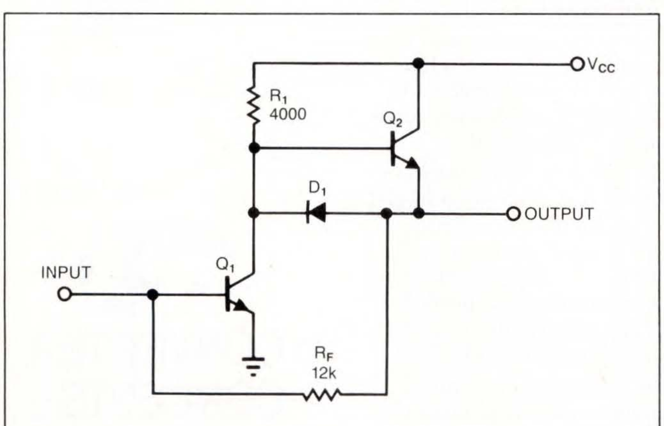

Fig 21—Although complementary npn-pnp transistors *are often used for class B output drivers, this basic circuit uses only high-performance npn devices.*

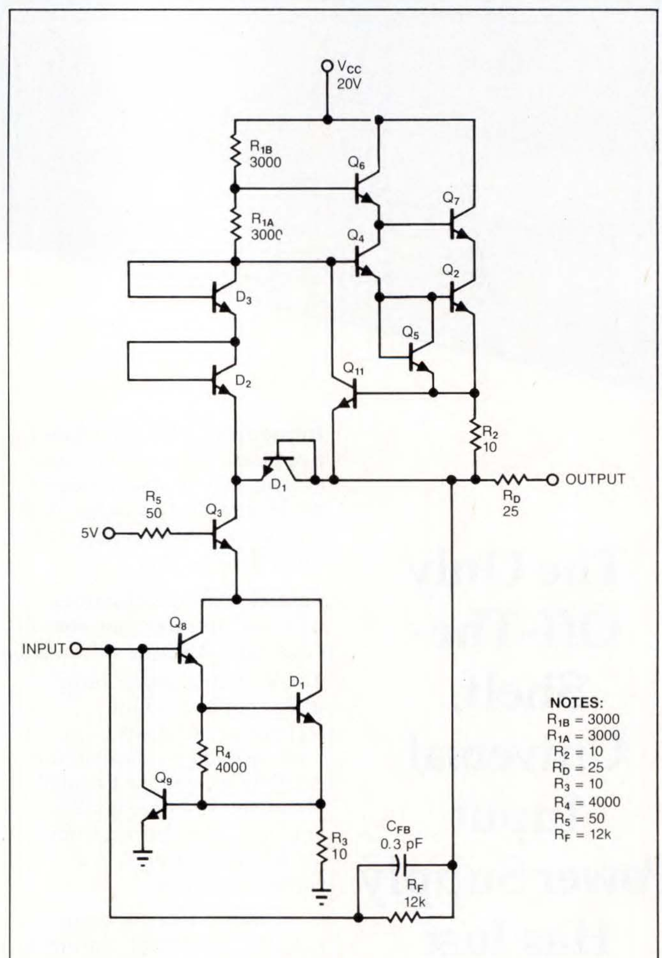

Fig 22—This practical implementation of a class B driver *uses several additional devices to achieve high performance.*

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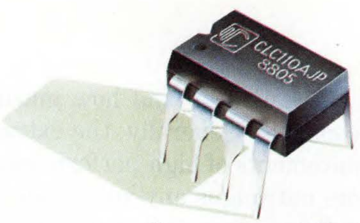

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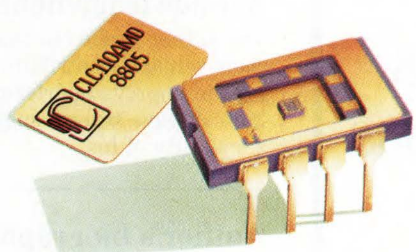

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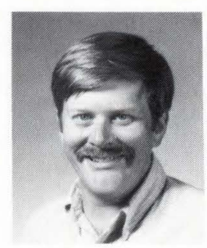
the cost of the silicon and how much area the added devices consume. Generally, the extra cost and greater area requirements of high-performance, integrated pnp transistors outweighs any advantage in device count.

In some cases, pnp transistors can offer higher performance—for example, an output driver that swings to within a few hundred millivolts of its positive and negative rails—but such cases are rare. Although you would normally design discrete circuits with npn and pnp transistors of equal performance, this option is usually not available with semicustom circuits. Nevertheless you can, in many cases, duplicate discrete-circuit performance by using primarily npn transistors—with some help from lateral and substrate pnp types. EDN

Acknowledgements

The author wishes to thank Pat Quinn and Mike Metcalf for their valuable contributions. Pat Quinn suggested the circuit for the improved-performance, all-npn current source. Mike Metcalf gave several suggestions for all-npn class B drivers, a specialty of his.

Author's biography



Winthrop "Wink" Gross is an engineering manager with Tektronix Integrated Circuits. He manages a design group for custom and semicustom products. Wink, who has a BA from Harvard and an MSEE from MIT, has been with Tektronix for 19 years and has 2 patents to his credit. His hobbies include classical piano and bird watching.

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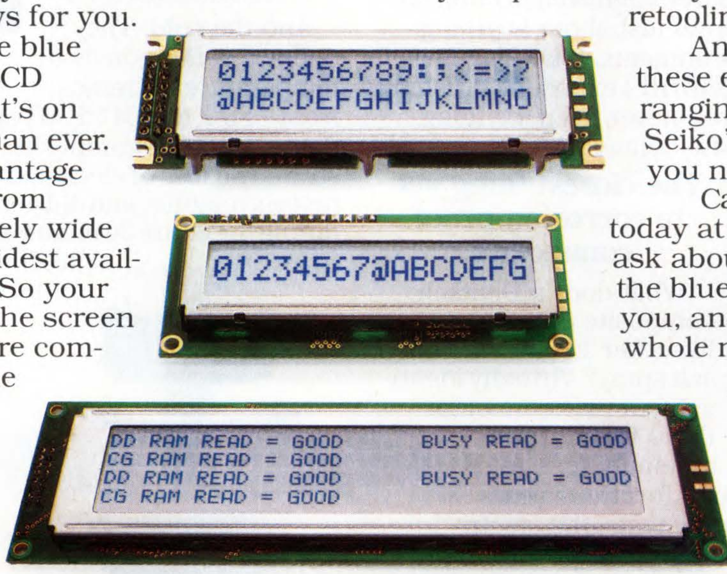

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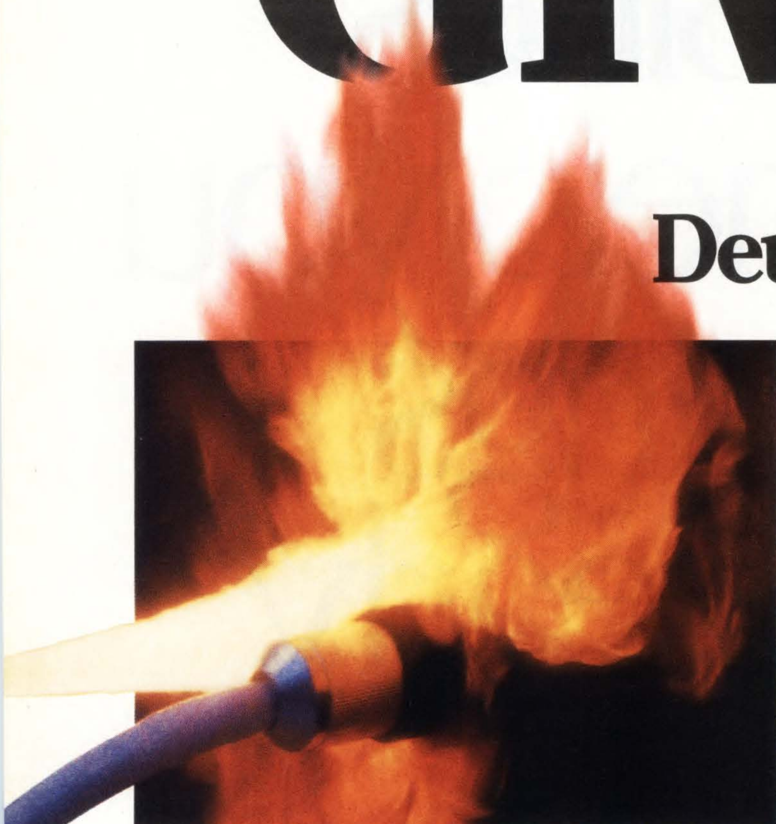

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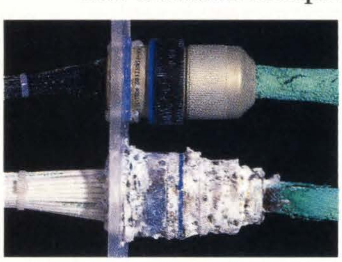

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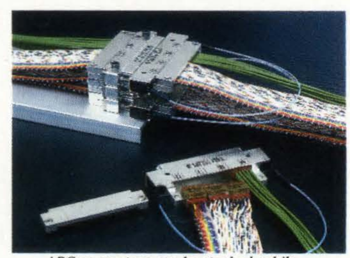

ABC connectors can be stacked, while accessibility is maintained to each plug shell for easy removal of the module.

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Composite connectors weigh substantially less than comparable aluminum connectors.

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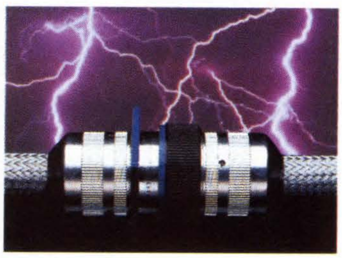

DG123 and ABC composite connectors offer outstanding EMI/RFI protection.

Outstanding EMI/RFI protection.

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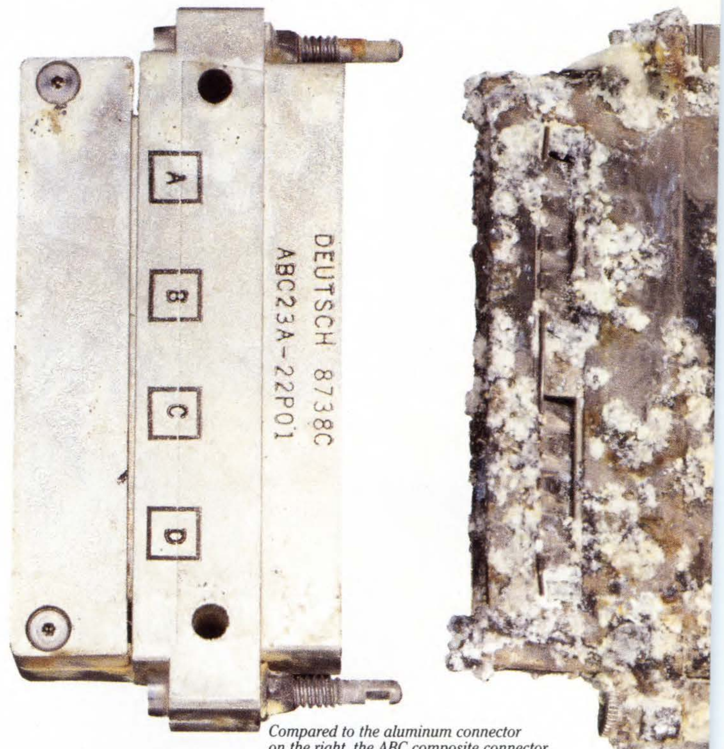
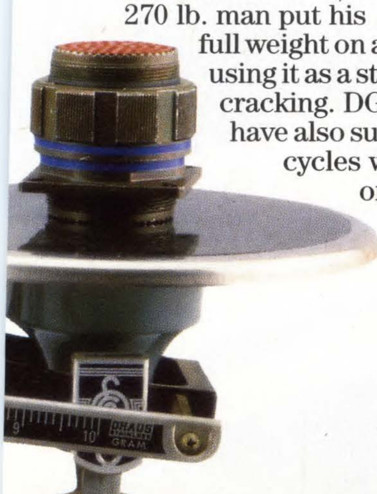
In many instances, composite connectors will give, rather than break under stress.



Compared to the aluminum connector on the right, the ABC composite connector on the left is virtually unaffected after 1000 hours of salt spray testing.



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DESIGNER'S GUIDE

PC-based analog pc-board design Part 2

Analog-board-layout tips overcome limitations of CAD software

Unfortunately for analog engineers, PC-based software for pc-board layout does not easily accommodate the distinct requirements of analog design. Part 1 of this series examined CAD packages in terms of their applicability to analog pc-board design. Part 2 offers some tips for making the most of the packages available today.

Kimberley F Quirk, *Engineering Services Group*

Analog pc-board designers who want to use inexpensive, PC-based CAD software soon find out that most packages are intended for engineers designing relatively simple digital boards. Designers of sensitive or high-frequency circuits need special capabilities. They need to be able to add extra grounding or guarding signals and to define parts and custom traces to 1-mil resolution. More importantly, they need to create planes, put multiple planes on one layer, and incorporate signals into ground planes—all of which are tasks that PC-based CAD software generally doesn't perform too well.

Using two inexpensive software packages as examples, this article will demonstrate what you can expect from your PC-based pc-board software and how you can overcome its limitations. The two packages are PADS-PCB from CAD Software (Littleton, MA) and RGraph/Criterion II from Aptos Systems (Scotts Valley, CA). Aptos Systems is specifically trying to sell RGraph to the analog market, and some of the software's features reflect that goal. CAD Software, on the other hand, takes into account some analog issues but is not actively catering to the needs of analog designers.

In late 1986 (when I was choosing a software package), the most significant difference between the two programs was the price. RGraph was about $10,000 and PADS was about $1000. The RGraph system included, as standard items, higher-resolution graphics as well as schematic entry, photoplotter outputs, and other features that were only options with PADS-PCB. The PADS-PCB program was strictly a layout package, with no router, no Gerber output, and no schematic-capture capabilities. Aptos Systems has since split up its system into parts, and CAD Software has added all the options, so the two systems are very competitive in price.

Basically (and being overly simplistic), PADS-PCB is a very capable program that people who aren't very knowledgeable about pc-board design can use. To achieve simplicity, the program makes assumptions, some of which limit its analog capabilities. PADS-PCB does not allow for freehand drawing, especially in the area of pads and silkscreen shapes. You cannot copy

"Dummy" signals may be a good way to trick the software into allowing you to add extra guard signals.

groups of symbols easily, and you are restricted to 90° increments of rotation.

On the positive side, however, the program does contain features that you'd expect to find only in larger CAD systems. You can apply some of these features to analog designs, but most of them were intended for the digital domain. For instance, PADS-PCB has many valuable reporting features and placement aids, a good user interface, and interactive routing and checking features. It handles ground planes well and allows for interesting combinations of split ground planes. You won't find it easy to put traces on ground planes, but it can be done.

RGraph/Criterion II permits freehand drawing, customizable pads, and rotation in 0.1° increments. You can very easily copy areas or individual parts over and over again. Everything you can do to a part on one layer, you can do to a group of parts on one or many layers. This kind of flexibility requires a more complex program, however, and RGraph/Criterion II may not be as easy to learn or to use on an occasional basis as is PADS-PCB. It is also more difficult to maintain continuity and perform error checking. In addition, RGraph/Criterion II has fewer "digital" reporting features and automatic functions than does PADS-PCB. You'll have more trouble setting up ground planes with RGraph, but you'll find it easier to put traces on them.

If you have noise-sensitive signals in your design, you may need to individually shield the traces. By surrounding a trace with extra ground (or guard) copper, you can help to isolate two nearby signal lines and prevent crosstalk between them. Filling in blank spaces with extra copper ensures even better grounding or isolation. **Fig 1** shows an example of shielded traces and added ground copper.

Some programs make no distinction between drawing copper (any shape, any place on the board) and laying down traces. If this is the case with your software, you can probably add quite a bit of extra copper as traces before you run into memory limitations. A traditional digital design package allows thousands of connections, but you don't need nearly as many on an analog board.

Other programs have two separate routines, one for adding copper and one for laying down traces. Such programs are more likely to run into memory-based restrictions regarding the amount of copper you can put down because digital software assumes you don't need much extra copper.

In placing extra copper for grounding and isolation purposes, don't forget to consider the impact on design-rule checking. Many systems don't require or permit you to name this extra copper, which means that they won't do an accurate job of checking. Hopefully, your system will still be able to check the rest of the board, but there's a chance that the checking feature will be useless for some designs.

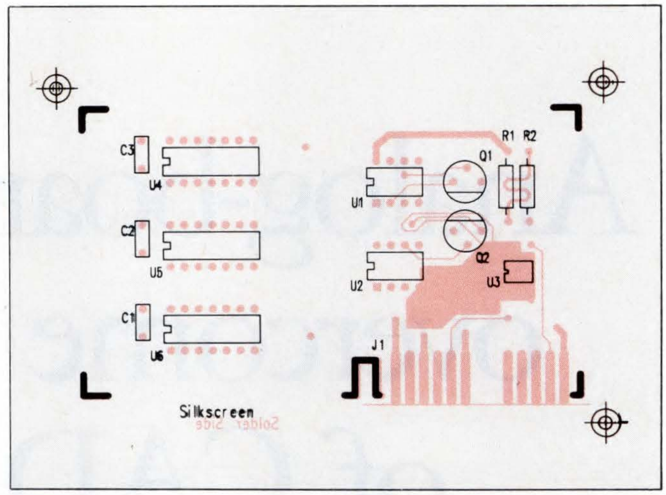

***Fig 1—Most pc-board CAD packages** allow the user to add copper and guard signals. Notice the shielded trace on the right side.*

If your software doesn't allow you to add enough copper to adequately guard the necessary signals, another alternative is to add dummy signals (ultimately tied to ground) to the rat's nest. Some software programs allow the addition of extra ground traces to the rat's nest, which you can later route between noisy signals. Be aware that some software may limit the number of connections you can make from point A (one ground connection) to point B (another ground connection). PADS-PCB, for instance, will only let you make one direct connection from A to B, though you can make indirect connections from A to B to C to A.

Some software programs may force you to route these multiple traces as independent signals shorted together, but because they are all tied to ground, you shouldn't have to be concerned. Moreover, this method has an important advantage. Once the traces are part of the rat's nest, the design-rule checker will automatically check them for spacing violations just like all the other traces.

If you need to fill in the blank spaces with copper and it turns out that your software's memory limitation restricts the amount of copper you can use, you do have another alternative. You could redefine the entire layer as a ground plane with embedded signals. This type of design achieves the best grounding, but it is generally more difficult to implement.

Most analog pc-board software has (or should have) some way of generating a plane. The difference between programs is the ease of generating it. A "basic" plane (power or ground) is an inner layer that does not have any signal traces. It is a layer of copper with relief pads (unconnected pads) around most of the holes and with solderable thermal pads for those points that need to connect to the plane.

RGraph/Criterion II is fairly typical in its method of creating a plane. It requires that you know in advance where the connections to the plane will be and that you call for a thermal pad in the initial part definition. It may also require multiple definitions for each part in the library.

PADS-PCB, on the other hand, automatically puts thermal pads on the plane layer in the appropriate places by referring to the rat's nest signal name. For example, if your ground signal is called "GND" in the rat's nest, PADS-PCB will automatically insert a thermal pad instead of the pad defined with the original part on the appropriate plane layer. Because this placement is automatic, you have no say in the appearance of the thermal pad and you cannot view the actual plane on your monitor. The software makes many other assumptions, which simplify the layout process, but which can often be too restrictive for analog users.

If you need a ground plane with signals . . .

Imagine that you want to design an analog board with the component side made up of only a ground plane except where signal traces must be run **(Fig 2d).**

Ideally, you would set up the computer so that the top side would be the ground plane and the bottom side would be a regular trace layer. You would route

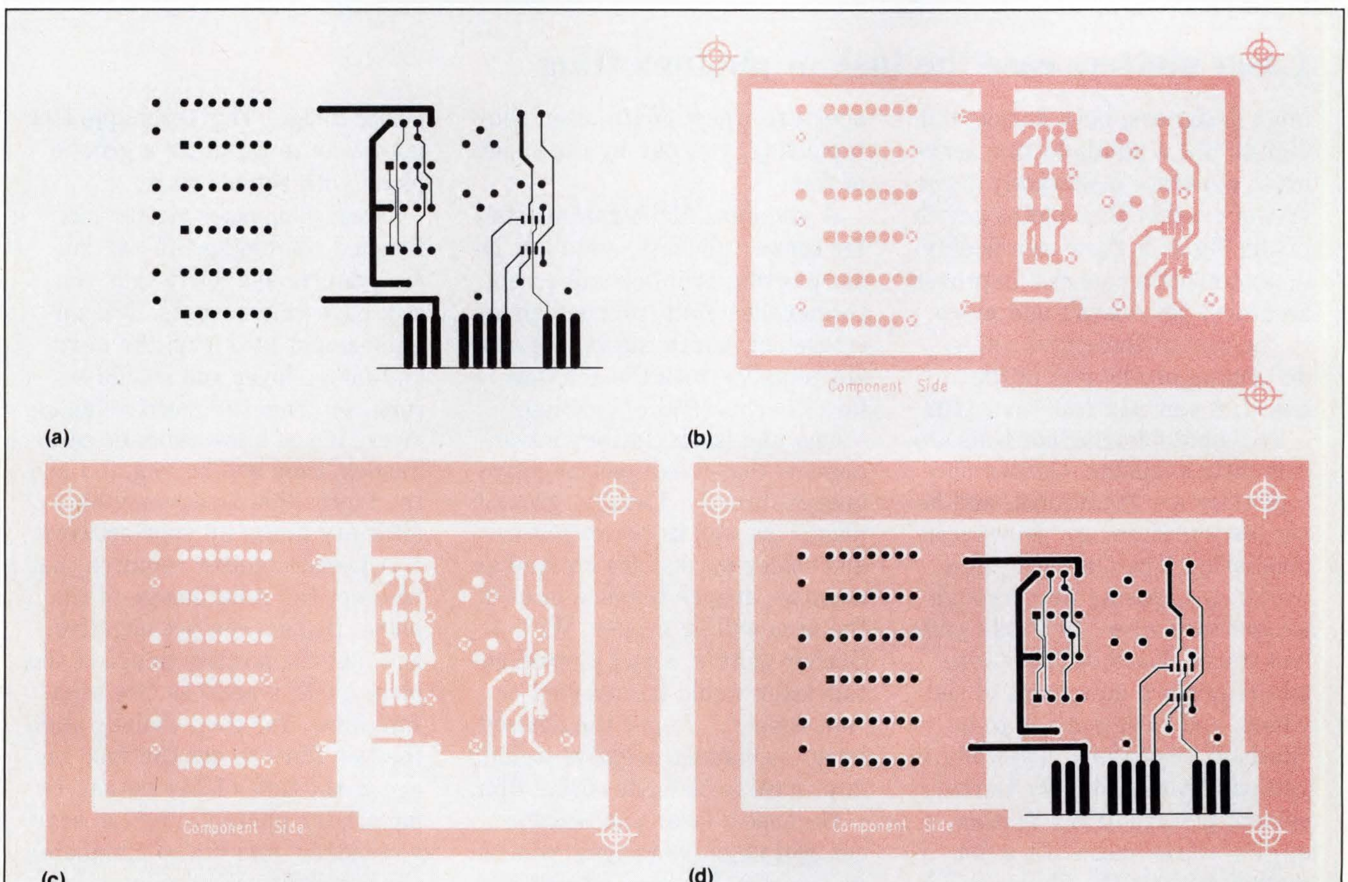

***Fig 2—Being able to incorporate traces** on a ground plane is important for many analog applications. First, you need to route the traces on the trace layer **(a)**. Then copy this pattern and widen the traces and pads **(b)** and invert the image **(c)**. Finally, combine the two patterns to make the composite image **(d)**.*

If your design calls for a board with noise-sensitive signals, you may need to individually shield the traces.

traces on the bottom side as usual. When you route the traces on the top side, the software would automatically generate the necessary relief around the traces to isolate them from the plane.

Unfortunately, you won't find any ideal software. To actually design such a board, you may have to create your own relief layer and trace layer as two separate items. (Again, you would route the bottom traces as usual.)

In the real world . . .

Begin the process by routing traces of the desired width on the trace layer **(Fig 2a)**. Then copy all the traces and pads from that layer to the relief layer and make them wider **(Fig 2b)**. Make a negative image of this relief layer **(Fig 2c)** and combine it with the trace layer to get the desired result **(Fig 2d)**. Depending on your resources, you may be able to use a laser photoplotter to superimpose the two images on one piece of film (see **box,** "Laser plotters ease the task of photoplotting").

The RGraph/Criterion II program handles this process simply because it allows you to copy all traces from one layer to another and widen them. As was discussed earlier, though, you must treat the thermal pads individually when creating parts. As long as you are organized from the start of the project, you can define parts to include the correct thermal and relief pads on the relief layer and the desired pad sizes on the trace layer (see **box,** "Careful design preplanning enhances productivity"). You will then find it relatively easy to generate the desired ground-plane signals.

The procedure that the PADS-PCB program uses is slightly more cumbersome. As with RGraph/ Criterion II, you must choose pad sizes when creating parts, but PADS-PCB doesn't permit you to copy

Laser plotters ease the task of photoplotting

Most designers, both analog and digital, use a photoplotting service to generate moderately dense artwork rather than plotting with ink on Mylar in their own facility. A photoplotting service improves accuracy, yet doesn't add much to the cost of the entire job—depending on the size of the board, it can cost less than $100.

Two photoplotting methods are currently available. Gerber photoplotters are traditional, and laser photoplotters are growing in popularity. The Gerber system works by exposing film through an aperture wheel to create pads and traces. Each different-size pad requires a movement of the wheel, and each pad has to be "flashed" separately. Typically, you pay by the hour for Gerber-system photoplotting. A laser system works more like a dot-matrix printer; the file is read in and printed from top to bottom without the need for a physical aperture wheel. With laser photoplotting, you pay by the sheet of film.

A standard file format exists for Gerber plotters, and most laser-plotting facilities will accept Gerber files. You still need an aperture list (which the vendor usually supplies with the software) for either method of plotting.

One of a laser plotter's advantages is that it can plot negative images directly. Usually, ground planes (as well as power planes and solder masks) are created as negative images because most of the area will be copper. With a Gerber plotter, a pad plotted on this layer would be inverted or "not copper." To get the desired image, a contact negative would later have to be made of that film.

Because a laser photoplotter can plot negative images, you can go one step further and plot the positive image directly on top of the negative image to form a composite image. This technique is a good way to generate a ground plane with signals on it.

When your laser plotter has finished combining the two layers, you should verify that you still have your targets. The targets should be left on the negative-image layer and should be removed from the positive-image layer. If you leave them on both images, they will be negated and the fabrication house may have difficulty lining up your artwork.

A Gerber plotter requires that you plot the relief image of the plane, make a contact negative, and plot the positive image of the plane (with traces) as two separate films. You then visually align the two films to get the final image at the time of fabrication. Using a laser photoplotter can save you money, and it also eliminates the possibility of misaligned images.

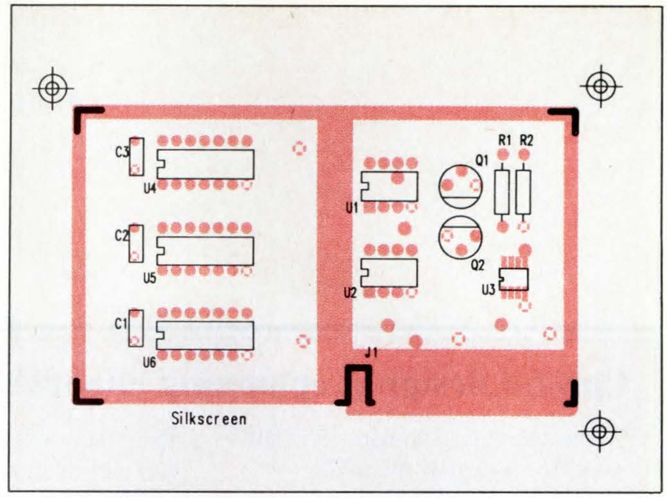

Fig 3—Split planes can be useful for accommodating both ground and power signals when you need to mix analog and digital grounds or when you need to isolate large areas.

traces onto another layer (though you can uniformly increase trace widths). One way you can get the same traces with different widths is to save the job under two names and change the trace widths on one of the files. With this technique, of course, you have to take care not to confuse your original and modified files and artwork. The positive images will be generated from the original file and the negative image will be the product of the newly created file with increased widths.

You have one other option

For situations where there aren't many traces on the composite plane (that is, the ground plane with signals), one other method is also suitable. After routing the few signal traces that there are on the trace layer, you can create relief traces by adding copper to the relief layer directly over the signal traces. The relief traces should be 30 to 50 mils wider than the signal traces, and they must line up perfectly. Because of the independent creation of the layers, you'll probably find it difficult to line them up. If the layers aren't properly aligned, or if changes are made on one layer and forgotten on the other, you will end up with traces shorted to ground. This is another reason to take great care in tracking files and changes.

If your software package does not support any of these methodologies, you still can use it to create the two layers: Save the job under two file names, as above, and change each trace width and pad size by hand in one of the files. This process is very tedious and, because of the time and work required, you should only attempt it as a last resort.

Split planes may be crucial, too

For those applications where it is desirable to have a digital and an analog ground plane, or more than one analog ground plane, you may need a split ground plane. On a 4-layer board, for instance, you can use the two outer layers to run all the traces, one inner layer for the power ground, and the other inner layer for both the digital and the analog grounds. Until you actually buy a software program and experiment with it, you'll find it next to impossible to determine if you can use split ground planes and, if so, what sort of contortions you might have to go through to implement them. **Fig 3** shows a representative split plane with thermal connections on each plane.

The PADS-PCB program allows you to assign as many as 10 different signal names to any one plane layer. Every pad that connects to one of these signals gets a thermal pad on the plane layer. You must be careful because of the likelihood of accidentally connecting both the V_{CC} and ground signals to the same plane. If you need to connect the digital ground and the analog ground to planes on the same layer, however, using a program such as PADS-PCB is a fairly direct method. Other software offering automatic generation of planes may allow only one signal to be connected to the plane at a time, which would prevent you from using multiple signal names to create a split plane.

With PADS-PCB, you can use relief copper to define the outline and separation of the ground layer—remember that this layer will be a negative image. Assign names such as AGND (analog ground) and DGND (digital) to the proper plane layer to ensure that thermal pads are automatically generated. Don't forget that a DGND pin that lies over the analog ground area will introduce a thermal pad into the analog ground area. Any pins that you connect to AGND that are physically located over the digital ground plane will result in an incorrect connection to that plane.

Ideally, the program would have a clean way of creating and utilizing split or multiple ground planes, including the ability to perform error checking on these planes. In reality, expect to spend time carefully hand checking these areas.

If you're using a program such as RGraph/Criterion II, you can define any part, regardless of its signal connection, as having a thermal pad on a particular layer. Because the software doesn't perform any checking to see if you've connected more than one signal name to a ground area, you'll need to carefully check the layers by hand. As with PADS-PCB, you must draw or create copper on the ground layer to separate the two ground planes.

In certain situations, it may be impossible to split the plane: if the software generates planes automatically; if the software allows only one signal name per plane layer; or if you're not permitted access to the

Careful design preplanning enhances productivity

When you begin to use CAD software to design your analog pc boards, you'll discover that your first few boards will take much, much longer than your most conservative "guesstimate." Completing the following steps before beginning your layout should help you to become better organized and to use your time more efficiently:

1. Create a table relating part types to decal or footprints, as well as to pad sizes on each layer and to hole sizes.

2. Make sure you understand board information such as dimensions, "keep-out areas," number of layers, and grounding schemes.

3. Define all parts. With many packages, this may be a 2-step (or more) process. First, define the graphic representation of a part, and second, document the text that relates part types to decals and defines packaging information.

4. Double-check that your net list is suitable for direct input into the layout/routing software. If your schematic package and pc-board design software are from different vendors, it may not be. You may need to fiddle with the net list to make it compatible.

5. Unless it's a very small board, use paper, pencil, and scissors to do a first-pass layout. It really helps to see the flow of the entire board. Even on a moderate-size board, reference designators will be too small to read when viewing the whole image.

By adequately planning from the beginning, you'll be able to accurately determine whether you can design the circuit in two or four layers. Although most software makes reasonable provisions for adding layers, you'll want to avoid this if at all possible. You may need to plan different pad sizes for each layer at the time you are creating the library. It is an annoying task to redefine the pads for each part in the middle of a job to accommodate a new layering structure.

Establish a notebook of pertinent data for each job you start. You'll find it extremely useful when designing similar boards later.

The following is a list of data you'll find helpful to have on hand:

- Brief description (or sometimes a drawing) of the layering structure; you'll find this especially important when dealing with multiple planes. Your characterization should also describe positive, negative, and composite images.
- A table of layer numbers and descriptions. Most software is set up in user-definable layers. Decide and record which layers you'll be using for component-side and solder-side traces, power and ground planes, and solder-mask, fab/drill, and silkscreen information.
- A table of part types, associated decals, and pad information for all parts used on this board. If you develop your own list of desired pad sizes, drill-hole sizes, and naming conventions, you'll find it much easier to check or change the parts as needed.
- Other, software-specific, information. For instance, some programs allow you to use macros, which may be specific to a board, or let you save a board outline separately from the rest of the job for easy retrieval later.

Backing up data

A good habit is to save your data in such a way that it is easy to reference. One method is to use a table that includes the date, file name, and a description every time you save the job. Keep this information in the same book as the above job data.

It is important to save different stages of your work under different file names. Not only does it prevent you from overwriting a file with bad data, but it allows you access to important stages of your work later on. You should be able to go back to a certain point in your design and start again if necessary. You might find this data useful if you want to make major modifications at a later date, or if the same board and power/ground scheme proves feasible for a future project.

Finally, don't forget to save your data on a floppy disk at *least* a few times during the job.

pad information to define your own thermal pads. In most other cases, you should be able to devise a method of splitting the plane, no matter what software package you're using.

You can extend the idea of split or multiple planes even further and, in specific designs, you may be forced to. For example, consider a pc board that splits up a plane layer and requires signals on the same layer. As long as you can define an area of relief from the ground plane, and route traces in that area, you won't have much to worry about. First set up your computer with two layers (trace layer and relief layer). On the relief layer, define a copper area large enough to contain all the routed traces of the trace layer. When you make the negative image of the relief layer, the copper will become the relief area and therefore you won't have to create individual relief traces. Combine these two layers to make the composite image. You'll have to do manual checking to ensure that the signal traces are far enough away from the ground plane area.

As you experiment further with analog pc-board design, you'll discover other possible combinations of signals and grounds. Don't forget, however, that many PC-based CAD packages weren't designed to allow these permutations of signals. Therefore, when you do devise an unusual layout technique, make sure you allow plenty of time for careful checking before the photoplotting or final artwork generation begins. **EDN**

Reference

1. Quirk, Kimberley F, "Part 1—Designer's guide to PC-based analog pc-board design," *EDN*, October 13, 1988, pg 195.

Author's biography

Kimberley F Quirk is founder and president of Engineering Services Group in Westford, MA, a company that specializes in analog and RF pc-board design. Kim holds an AB from Dartmouth College and a BSEE and an MSEE from Thayer School of Engineering at Dartmouth College. In her spare time, she enjoys tennis, racquetball, and music (both electronic and acoustic).

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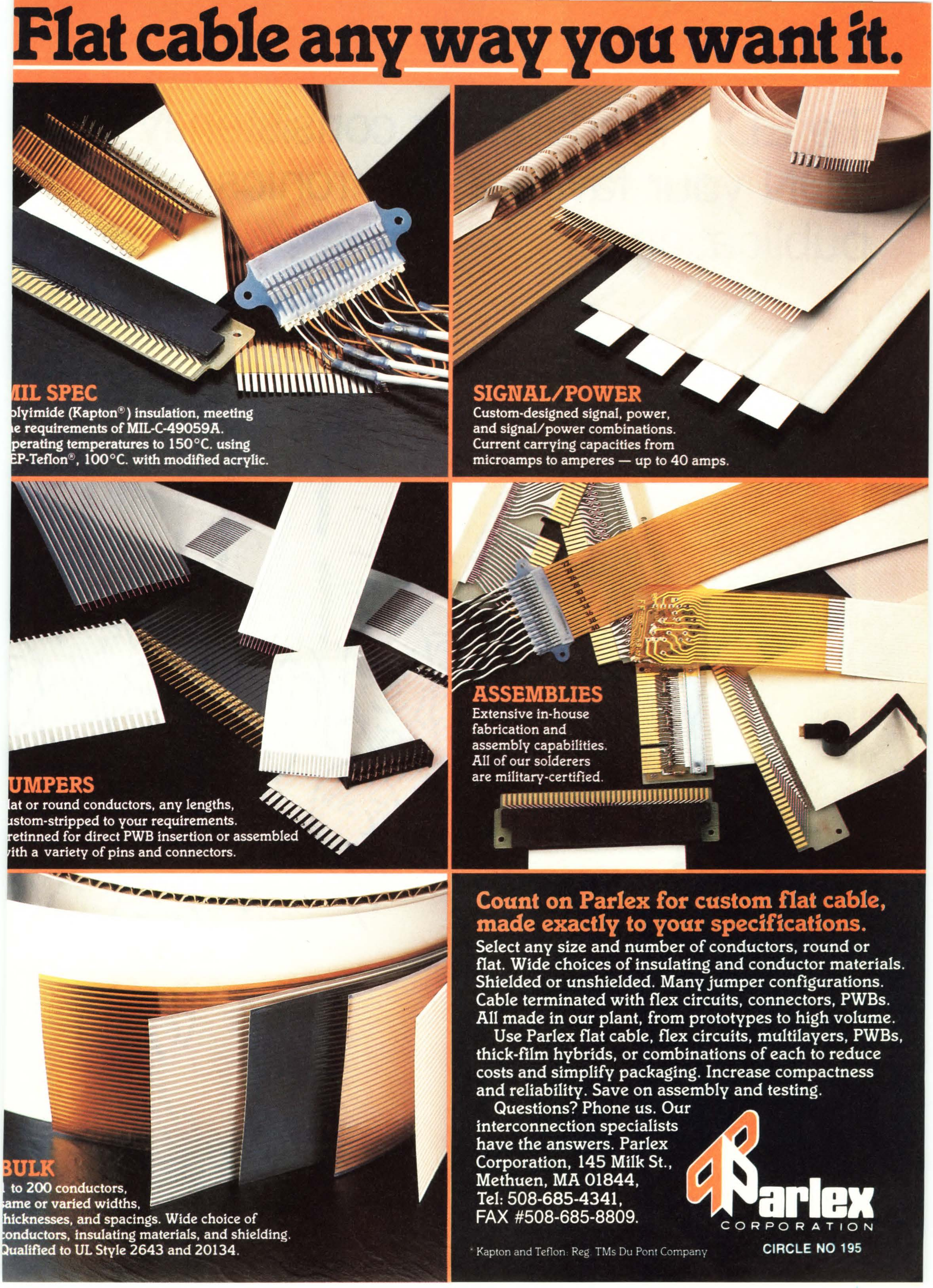
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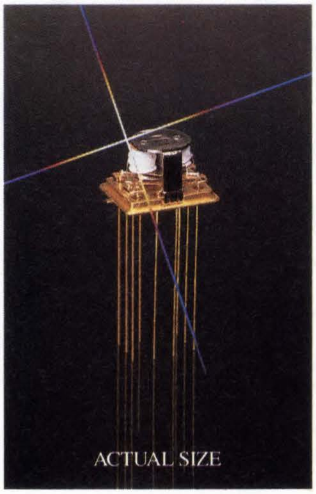

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EDITED BY CHARLES H SMALL

Pseudorandom sequencer simulates flicker

Andrew K Dart
Andy's Bureau of Standards, Duncanville, TX

The pseudorandom sequencer in **Fig 1** drives a solid-state relay. If you power a low-wattage lamp from the relay, the lamp will appear to flicker like a candle's flame in the wind; using higher-wattage lamps allows you to simulate the blaze of a fireplace or campfire. You can enhance the effect by using three or more such circuits to power an array of lamps.

The circuit comprises an oscillator, IC_1, and a 15-stage, psuedorandom sequencer, $IC_{2\text{-}4}$. The sequencer produces a serial bit stream that repeats only every 32,767 bits. Feedback from the sequencer's stages 14 and 15 go through IC_{4D} and back to the serial input of IC_2. Note the RC network feeding IC_{4C}; the network feeds a positive pulse into the sequencer to ensure that it won't get stuck with all zeros at power-up. The leftover XOR gates $IC_{4A,B}$, further scramble the pattern. The serial stream from IC_{4B} drives a solid-state relay that features zero-voltage switching and can handle loads as high as 1A at 12 to 280V ac. EDN

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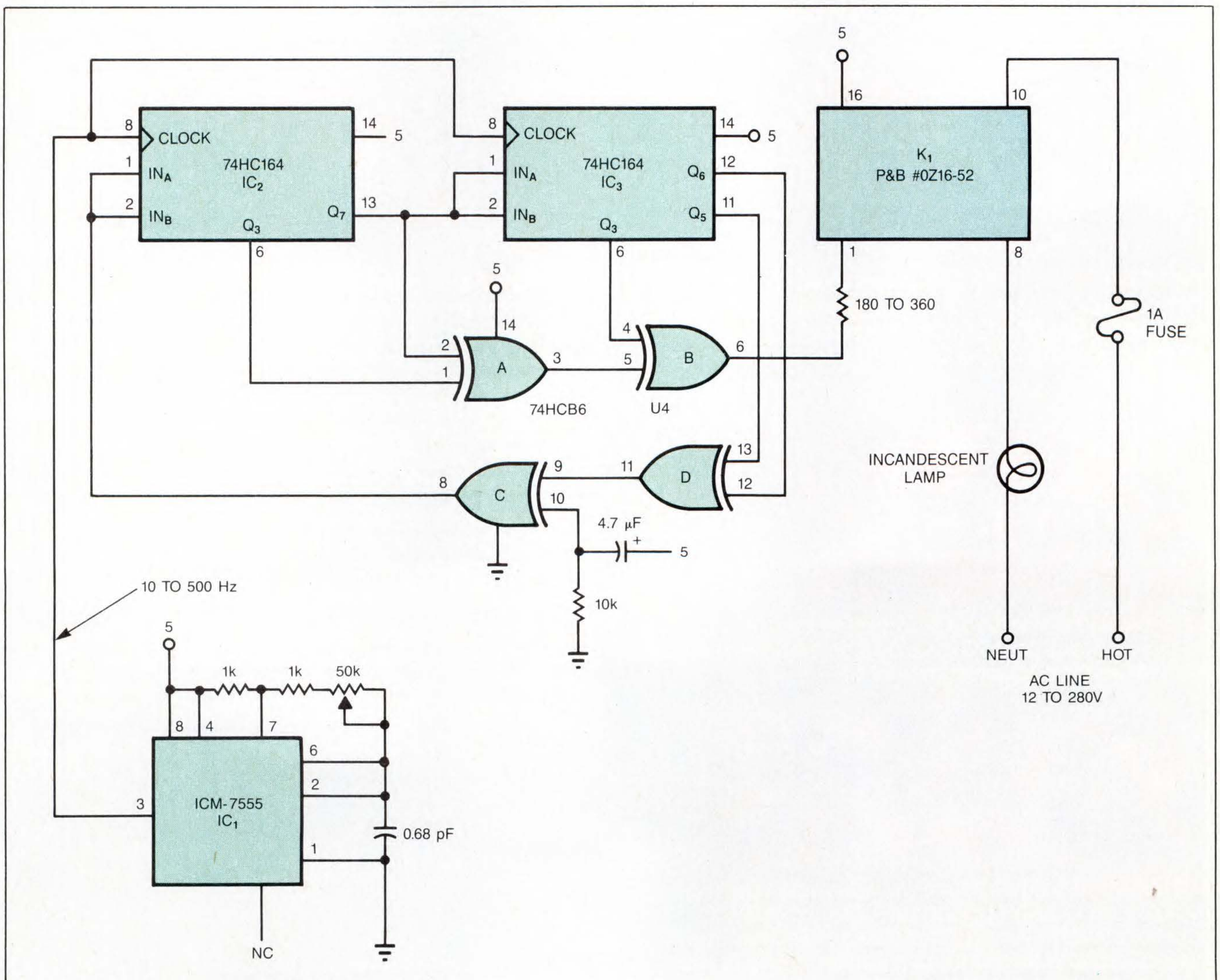

***Fig 1—This pseudorandom sequencer can produce** a realistic flickering in incandescent lamps that is similar to the flickering of a flame in the breeze.*

Regulator manages battery depletion

Robert Dobkin
Linear Technology Corp, Milpitas, CA

Powering electronics from batteries poses special problems for power-supply designers. The circuit in **Fig 1** automatically shuts down when the supply's output voltage begins to fall out of regulation range and automatically restarts when the battery recharges, without the annoying chatter or intermittent operation that some battery regulators can exhibit. Its quiescent current is ~60 μA, and it can deliver 125 mA. The reference voltage at Pin 4 is 2.5V, and it can source or sink as much as 1 mA; you can use this pin as a source of power for keep-alive circuitry.

This circuit provides better performance than circuits whose shutdown circuits merely sense the battery's voltage. Because such circuits sense the battery's—and not the supply's—output voltage, they can shut down prematurely while the battery still has some energy left. In addition, such circuits fail to take into account the ability of a battery's voltage to recover partially after its load is removed. This effect can cause a battery-monitoring shutdown circuit to erroneously switch the power supply back on.

The circuit in **Fig 1** takes advantage of the LT1020's dropout detector to shut itself down. The dropout detector has no output until the IC's series-pass output transistor actually starts to saturate. The circuit also uses the IC's built-in comparator to turn on the output only when the regulator's input voltage is 2.5V higher than its output.

Resistors R_5 and R_6 set the output voltage. The values shown in **Fig 1** are for a 5V nominal output. Capacitor C_2 provides frequency compensation for the output. R_1 and R_2 sense the input voltage for the inverting input of the comparator. During start-up and normal operation, the npn output of the comparator saturates, and no current flows from the pnp output at Pin 5. Positive feedback through R_3 latches the comparator. As the input voltage sags under load, the regulator IC's output transistor eventually saturates, and current flows from the dropout detector, Pin 13, into the noninverting input of the comparator.

This current forces the npn section of the comparator off and the pnp section on. The current from Pin 5 flows into Pin 11 and turns off the output of the regulator. Because no current flows through the npn portion of the comparator, the reference voltage applied to Pin 7 increases, and the comparator stays latched. These results keep the circuit's output off until the input rises 2.5V above the required output. EDN

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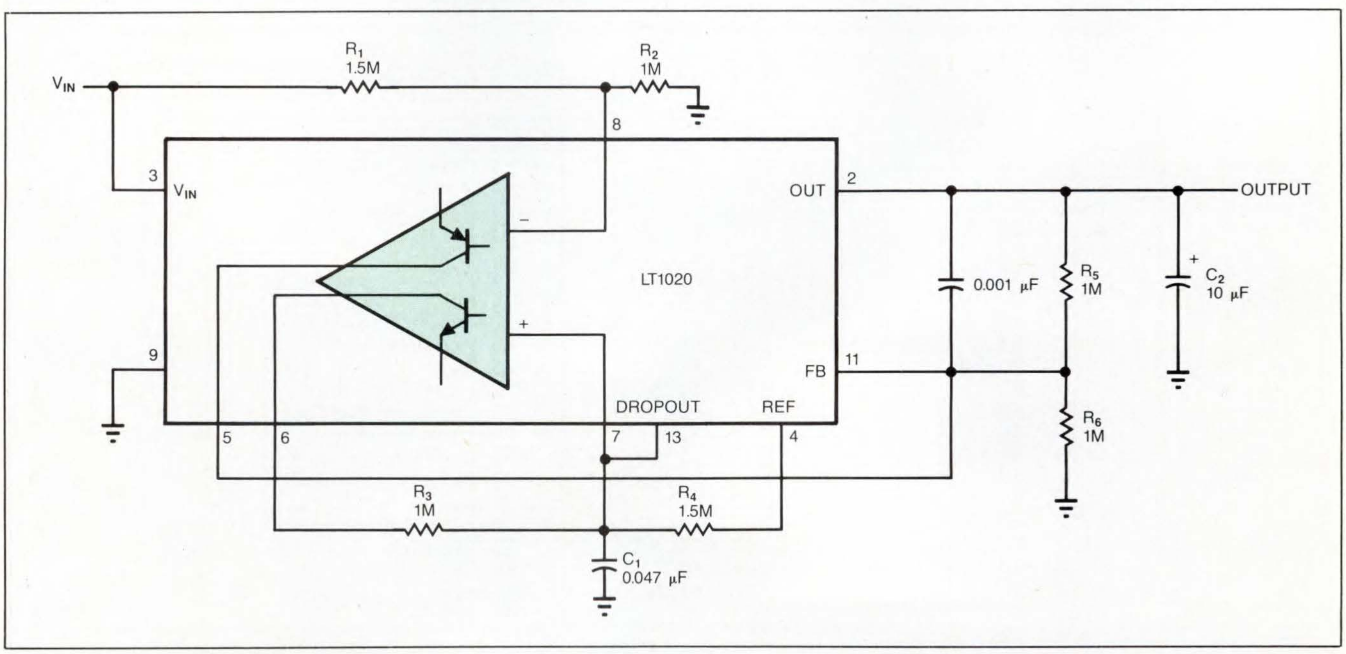

***Fig 1—This battery-powered regulator circuit** shuts itself down when the battery is depleted and doesn't resume supplying power until the battery is recharged.*

Routine extends multiply instruction

Donald E Powers
Cardinal Microsystems, Marion, MA

Unlike many single-chip μPs, the 8051 family has a multiplication instruction, MUL AB (multiply accumulator, A, by register B with the high byte of the result in B and the lower byte in A). Even when you must multiply numbers larger than 8 bits, using this instruction saves a great deal of time over the traditional add-and-shift method. The routine in **Listing 1** accomplishes 16×16-bit multiplication.

Two registers, R4 and R5, hold the upper and lower byte of the multiplicand; two other registers, R6 and R7, hold the multiplier. The results return in R4 through R7 with R4 holding the highest byte.

You may specify any register bank you wish. Because the routine needs only six stack locations for temporary storage of partial products, the routine changes only the contents of the accumulator, A, and register B. You can save A and B on the stack in order to retrieve their values later if necessary. Because the routine makes no checks for zero or partial zero results, its code is kept to a minimum and the routine's run-time is constant.

LISTING 1—16-BIT MULTIPLY ROUTINE

```
                          ORG   OFOOH
OFOO  EE         MUL16:   MOV   A,R6      ;Do highest partial
OF01  8C FO               MOV   B,R4      ;product first.
OF03  A4                  MUL   AB
OF04  CO FO               PUSH  B         ;R6*R4 Hi
OF06  CO EO               PUSH  ACC       ;R6*R4 Lo
OF08  EE                  MOV   A,R6
OF09  8D FO               MOV   B,R5
OFOB  A4                  MUL   AB
OFOC  CO FO               PUSH  B         ;R6*R5 Hi
OFOE  CO EO               PUSH  ACC       ;R6*R5 Lo
OF10  EF                  MOV   A,R7
OF11  8C FO               MOV   B,R4
OF13  A4                  MUL   AB
OF14  CO FO               PUSH  B         ;R7*R4 Hi
OF16  CO EO               PUSH  ACC       ;R7*R4 Lo
OF18  EF                  MOV   A,R7
OF19  8D FO               MOV   B,R5
OF1B  A4                  MUL   AB
OF1C  FF                  MOV   R7,A      ;R7*R5 Lo -> R7 Product
OF1D  E3                  CLR   C
OF1E  DO EO               POP   ACC       ;R7*R4 Lo +
OF20  25 FO               ADD   A,B       ;R7*R5 Hi
OF22  FE                  MOV   R6,A      ;-> R6 Partial Product
OF23  DO EO               POP   ACC       ;R7*R4 Hi
OF25  34 00               ADDC  A,#0      ;+ any previous carry
OF27  FD                  MOV   R5,A      ;-> R5 Partial product
OF28  E4                  CLR   A
OF29  34 00               ADDC  A,#0      ;-> R4 Partial product
OF2B  DO EO               POP   ACC       ;R6*R5 Lo
OF2D  2E                  ADD   A,R6      ;+R6 Partial Product
OF2E  FE                  MOV   R6,A      ;-> R6 Product
OF2F  DO EO               POP   ACC       ;R6*R5 Hi
OF31  3D                  ADDC  A,R5      ;+R5 Partial Product
OF32  FD                  MOV   R5,A      ;-> R5 Partial Product
OF33  EC                  MOV   A,R4      ;R4 Partial product
OF34  34 00               ADDC  A,#00     ;+ any previous carry
OF36  FC                  MOV   R4,A      ;-> R4 Partial Product
OF37  DO EO               POP   ACC       ;R6*R4 Lo
OF39  2D                  ADD   A,R5      ;+R5 Partial product
OF3A  FD                  MOV   R5,A      ;-> R5 Product
OF3B  DO EO               POP   ACC       ;R6*R4 Hi
OF3D  3C                  ADDC  A,R4      ;+ R4 Partial product + C
OF3E  FC                  MOV   R4,A      ;-> R4 Product
OF3F  22                  RET
```

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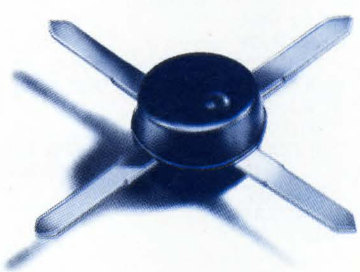

dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8 □	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
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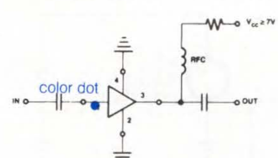

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*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

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C113-Rev. D

The routine uses this algorithm:

		R4	R5
	*	R6	R7
		R7*R5 Hi	R7*R5 Lo
	R7*R4 Hi	R7*R4 Lo	
	R6*R5 Hi	R6*R5 Lo	
R6*R4 Hi	R6*R4 Lo		
R4	R5	R6	R7

Note that the routine does MUL AB in reverse order with the most significant bytes first. This order puts the partial products on the stack in a way that eases adding partial products later. EDN

To Vote For This Design, Circle No 750

Spice2 routine simulates switch

Henry Valker
Sundstrand Aviation, Rockford, IL

You can simulate the simple switch of **Fig 1** using Spice2's "poly" nonlinear, dependent source. Possible applications for this simulated switch include stress testing (causing shorts at various points in the circuit and determining their effects), and discharging a capacitor. **Fig 2** shows the switch's Spice2 equivalent circuit, and **Listing 1** shows the actual Spice2 model. Two voltages control the nonlinear dependent source, E, in the switch's equivalent circuit; hence the term for such a dependent source is "poly."

A pulse-voltage source, V_P, controls the opening and closing of the switch; a second control voltage, $V_{2,3}$, which develops across R_2, is a compensating factor that allows the combination of the dependent source E and R_2 to act like a switch. The equation that defines the dependent source is

$$E = p0 + p1{*}V(2,3) + p2{*}V(4) + p3{*}V(2,3)^{**2} + p4{*}V(2,3){*}V(4).$$

where p0 through p4 are the gain constants that Spice2 requires you to select. Setting p0 = 1, p1 = −1, p2 = 0, p3 = 0, and p4 = 1 reduces this equation to:

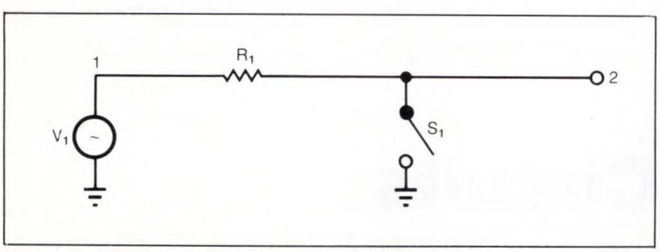

Fig 1—You can simulate this switch circuit with a Spice2 model.

LISTING 1—SWITCH SIMULATOR

```
SWITCH
V1 1 0 SIN 0V 10V 90KHz
R1 1 2 100K
R2 2 3 100K
E 3 0 POLY(2) 2 3 4 0 0 -1 0 0 1
VP 4 0 PULSE 0V 1000KV 12US 20NS 20NS 12US 30US
RP 4 0 1K
.WIDTH OUT=80
.OPTIONS LIMPTS=4000 LVLTIM=2 ITL5=0 ITL4=100 ITL3=25
+         METHOD=GEAR MAXORD=4 NOMOD
.TRAN .1US 100US 0US .1US
.PRINT TRAN V(2)
.END
```

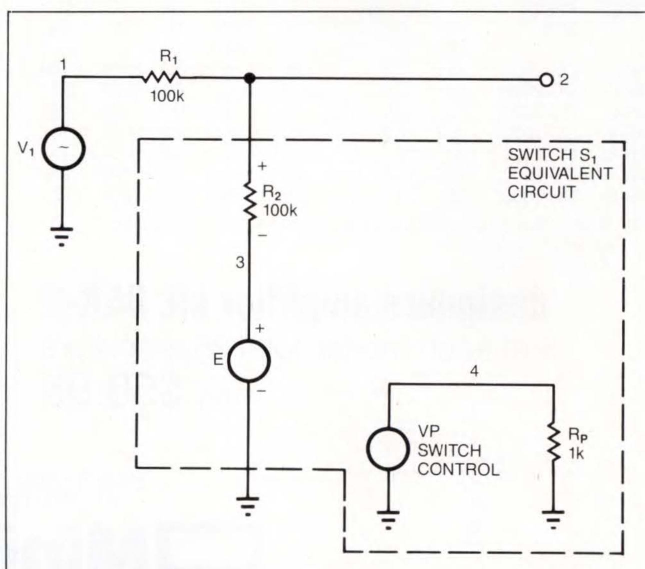

Fig 2—This Spice2 model is the equivalent circuit for the simple switch in Fig 1.

DESIGN NOTES

Number 16 in a series from Linear Technology Corporation October, 1988

Switched-Capacitor Low Pass Filters for Anti-Aliasing Applications

Richard Markell
Nello Sevastopoulos

INTRODUCTION

Many signal processing applications require a front end low pass filter to bandwidth limit the signal of interest. This filter is often crucial to the system designer since it determines the number of bits which the system can resolve by its noise and dynamic range. Until now, the designer rejected the use of switched-capacitor filters as being too noisy, having too much distortion, or because they were not usable at a high enough frequency. The LTC1064-1 8th order Cauer filter can compete directly with the discrete operational amplifier design. Not only that, but the cost and performance advantages are tremendous.

The LTC1064-1 is a complete 8th order, clock tunable Cauer (also known as elliptic) low pass switched-capacitor filter *with internal thin film resistors.* The passband ripple is ±0.1dB and the stopband attenuation at 1.5 times the cutoff frequency is 72dB. The device is available in a 14-pin DIP or 16-pin surface mount package.

The LTC1064-1 boasts internal thin film resistors factory adjusted to optimize the Cauer 8th order response. The LTC1064-1 attains wideband noise (2kHz–102kHz) of $150\mu V_{RMS}$ and a total harmonic distortion of 0.03% for $V_{IN} = 3V_{RMS}$. No external components are required for cutoff frequencies up to 20kHz. For cutoff frequencies over 20kHz two small value capacitors are required to maintain passband flatness.

By way of comparison, older switched-capacitor filters had noise in the millivolts, THD in the percents, and maximum corner frequencies limited to <20kHz.

This note compares the performance of the LTC1064-1 8th order Cauer filter with internal thin film resistors to that of the equivalent filter built with operational amplifiers. The LTC1064-1 quad switched-capacitor filter competes favorably with op amp RC designs in most parameters of interest to the designer and wins easily when printed circuit board space is considered. *Since it is tunable,* the LTC1064-1 can replace not just one, but many op amp RC designs, if multi-frequency filtering is required. The specification comparisons become even more favorable to the LTC1064-1 as the frequencies become higher.

COMPARING THE LTC1064-1 WITH RC ACTIVE FILTERS UTILIZING OPERATIONAL AMPLIFIERS

Performance

The Cauer filter has target design specifications as follows: a cutoff frequency of 40kHz, ±0.05dB passband ripple and a −72dB attenuation at 1.5 times the cutoff frequency. This filter is realized with stopband notches and it is considered a quite complex and selective filter realization. Figure 1 details the frequency response of this design.

An 8th order active RC was designed using a fully inverting state variable topology. This topology is considered "state-of-the-art" for active filters since all non-inverting inputs of the op amps are grounded. The discrete active RC version of the Cauer filter is quite complex requiring 16 op amps, 31 resistors and 8 capacitors. The op amps used for this comparison were TL084 quad FET input amplifiers. The circuit topology was optimized to yield the maximum useful input voltage swing.

Test Results

Figure 1 shows the frequency response of the LTC1064-1 connected as shown in Figure 3. The shape of the frequency response of the active RC state variable filter was very similar and its differences cannot

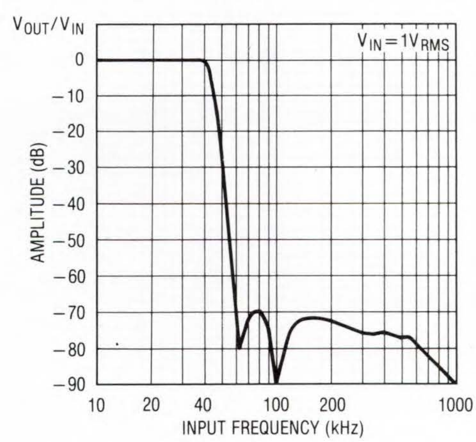

Figure 1. LTC1064-1 Frequency Response

be easily shown here. Figure 2, curve (a), details the TL084 state variable filter response near the 40kHz cutoff frequency. Laboratory "tweaking" of resistor values could not produce any better response than shown here. This is a passband ripple of approximately

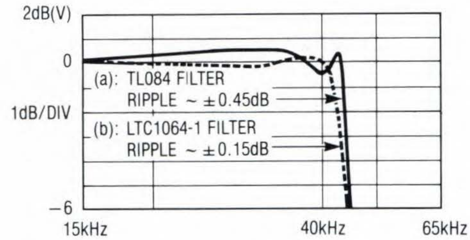

Figure 2. Passband Ripple

±0.45dB. For comparison, the LTC1064-1 passband ripple is ±0.15dB as shown in Figure 2, curve (b). This is for a clock to center frequency ratio of 100:1, or a 4MHz clock. The measured filter amplitude response at 1.5 times the cutoff frequency for the TL084 active RC filter was about −65dB while that of the LTC1064-1 was −68dB. The noise for the TL084 state variable implementation was $111\mu V_{RMS}$ while that for the LTC1064-1 was $145\mu V_{RMS}$. Second harmonic distortion measurements were also made on both filters and they are included on the summary chart, Table 1.

Table 1 compares the LTC1064-1, the switched capacitor implementation of the 8th order Cauer low pass filter, to the active RC. Both circuits operate with dual ±7.5V supplies or a single 15V supply.

System Considerations

Not only does the LTC1064-1 compare favorably on individual specifications, but it wins easily when system considerations are evaluated. Suppose four sharp cutoff frequencies are needed. The closest active RC solution is a 7th order single cutoff frequency Cauer filter. Four of these non-tunable devices (each a 2″ x 3″ hybrid) would be required for the four cutoff frequencies. This would be 24 square inches of PC board space. The discrete approach using operational amplifiers requires even more space. Since the LTC1064-1 is tunable, four frequencies can be selected merely by tuning the clock to the LTC1064-1. A complete LTC1064-1 system with tunable clock is estimated to occupy only 4 square inches of board space. This is a whopping savings of 6 times in board area. The LTC1064-1 wins easily in this category.

SUMMARY

In summary it can be seen from Table 1 that the LTC1064-1 is the equal of the active RC filter. In the pure specification battle there is no clear winner, but when the amazing difference in hardware complexity, the full clock tunability and the simple method of application of the LTC1064-1 device are all considered it is the sure winner.

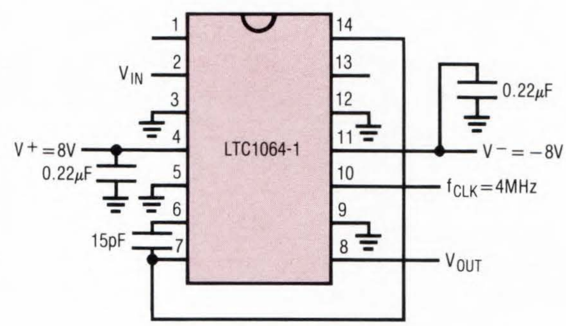

Figure 3. The LTC1064-1, Monolithic 8th Order Cauer Low Pass Filter Operating with a 4MHz Clock and Providing a 40kHz Cutoff Frequency

Table 1. 8th Order Cauer (Elliptic) LPF with a 40kHz Ripple Bandwidth

	# EXT OP AMPS	# EXT R's, 1%	# EXT CAPS, 5%	TUNABLE	WIDEBAND NOISE, RMS[4]	DISTORTION $V_{IN} = 1V_{RMS}, 3V_{RMS}$ (dB)	V_{OS} OUT (mV)[3]	I_{SUPPLY} (mA)	ATTENUATION AT 60kHz	MEASURED PASSBAND RIPPLE	TRIMMING[2]
RC Active TL084	16	31	8	No	111μV	−87, −87	55	33	65dB	±0.45dB	Yes
LTC1064-1	None[1]	None	1	Yes	145μV	−70, −70	30	18	68dB	±0.15dB	None

Note 1: An output inverting buffer (LT118) was used for driving cables during measurements.

Note 2: To obtain the ±0.45dB ripple for the TL084, 3 resistors were trimmed.

Note 3: The output offset voltage numbers are as measured by DVM with the input of the filter grounded.

Note 4: Measurement BW (2kHz-102kHz).

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IM/GP 988 165K

$$E = -V(2,3) + V(2,3)*V(4).$$

Now you can see how V_P controls the action of the switch. When $V_P=0$, $E=-V_{2,3}$, which is equal and opposite to the voltage across R_2. Thus, the two voltages cancel each other out, and node 2 is effectively a virtual ground. In this state, the model simulates a closed switch.

When V_P switches to some large voltage, the voltage

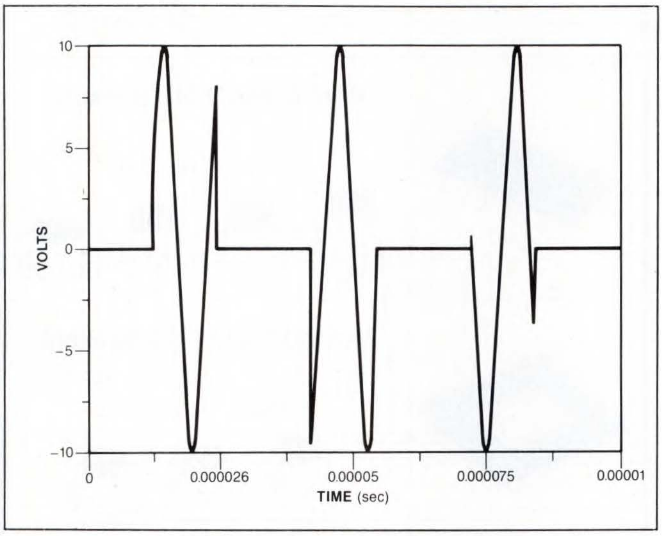

Fig 3—Using the intervals specified for V_P in Listing 1 to gate a sine wave on and off produces this waveform.

at E opposes that of V_1 and decreases current flow. Forcing V_P to be very large causes the loop current flowing through R_1 and R_2 and the voltage sources to be very small. This state simulates an open switch.

Although the 1000-kV term in V_P's definition in **Listing 1** might at first appear to be overpowering, the model never actually sees such high voltages because E depends on both V_P and the voltage across R_2. The voltage at node 2 is exactly that of node 1 in the open-switch state. **Fig 3** shows the waveforms that result.

EDN

To Vote For This Design, Circle No 748

RS-232C transmitters power LEDs

John Marszalek
Denro Labs, Gaithersburg, MD

You can use a pair of Maxim's 5V-powered MAX231 RS-232C transmitters as drivers to obtain a 2-color LED. The transmitters require only a single-ended 5V input to generate ±10V internally. Their outputs are short-circuit-proof and can supply as much as 10 mA—enough to drive most LEDs. Depending on which LED you select, their current-limiting feature may also eliminate the need for external series resistors. Using the simple circuits in **Fig 1a** and **1c**, you can implement a variety of functions.

EDN

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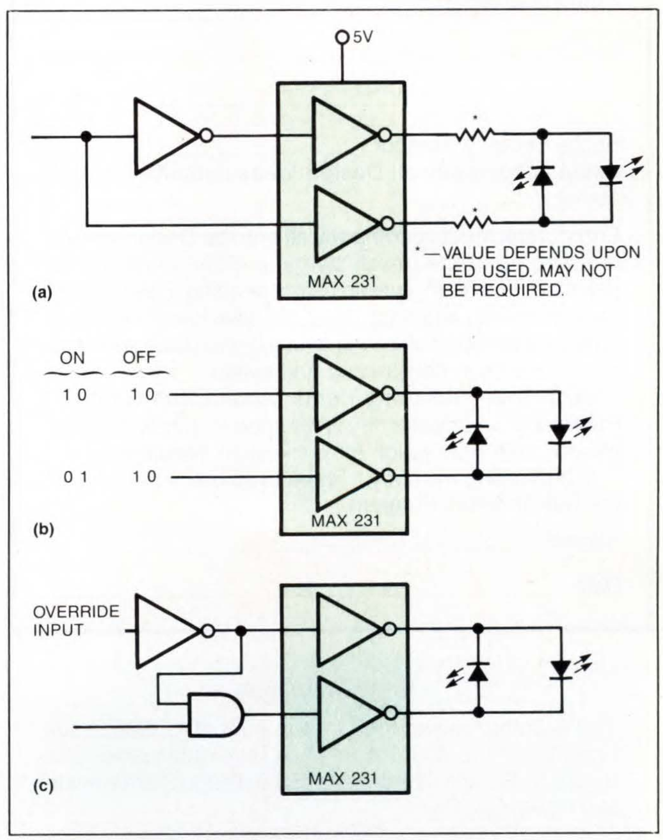

*Fig 1—**The simplest circuit, (a), lights one LED** or the other. The circuit in **b** allows you to light one, the other, or neither, while **c** provides an override function.*

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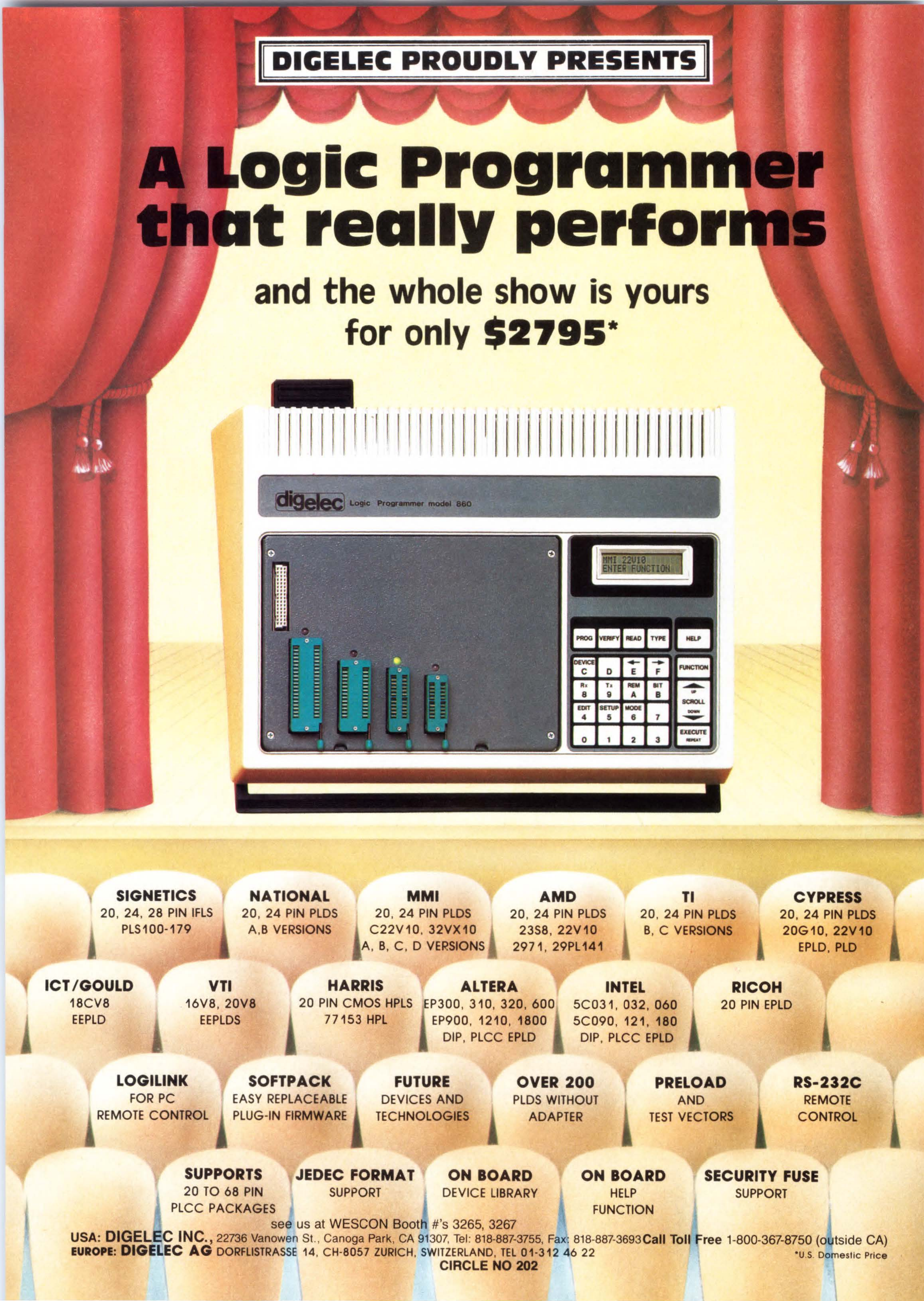

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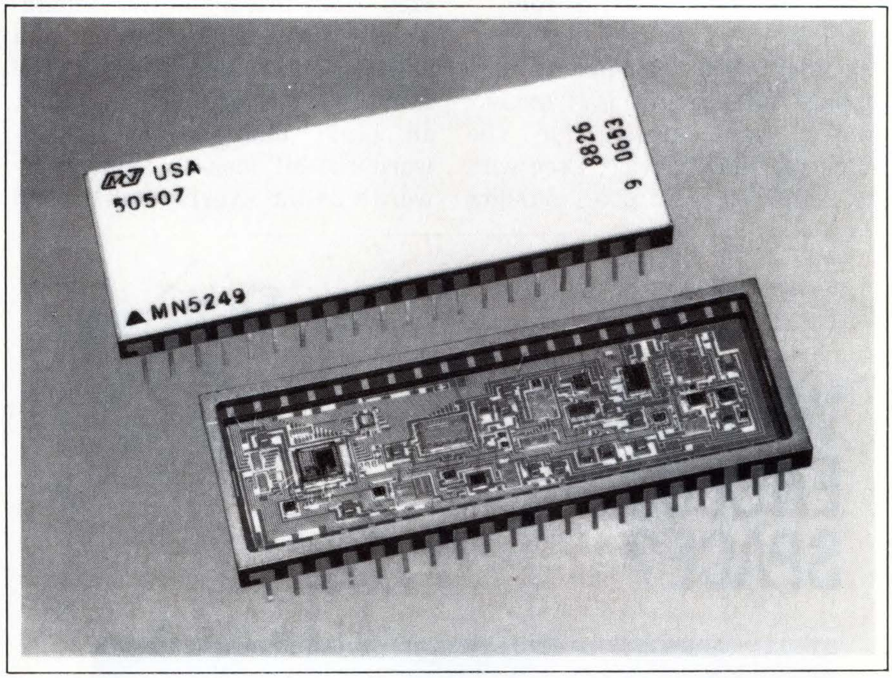
CIRCLE NO 202

INTEGRATED CIRCUITS

A/D CONVERTER

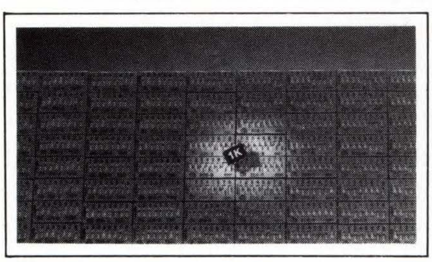
- *12-bit resolution*
- *400-nsec conversion time*



Intended for high-speed commercial, industrial, and military digitizing applications, the MN5249 A/D converter features 12-bit resolution with no missing codes. The device has a maximum conversion time of 400 nsec, which ensures a minimum conversion rate of 2.5 MHz. The integral linearity is ±0.024% FSR, and the analog input range is ±2.5V. A 3-state output buffer facilitates µP interfacing. When used with the company's MN376 track-and-hold amplifier, the MN5249 forms a pair that is capable of digitizing full-scale 5V signals with bandwidths to 1 MHz. The MN5249 comes in a 40-pin, double-wide, hermetically sealed DIP and consumes 2.5W of power. Commercial devices, $297; MIL-screened devices, $401.50 (100). Delivery, 12 to 16 weeks ARO.

Micro Networks, 324 Clark St, Worcester, MA 01606. Phone (508) 852-5400.

Circle No 351



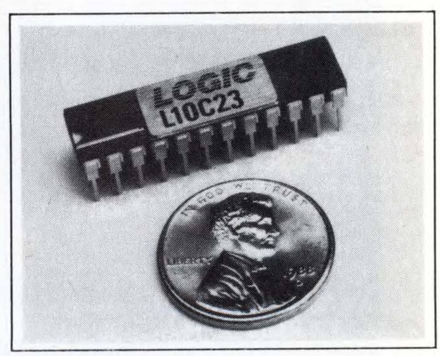
EEPROM

- *Contains 1024 bits of read/write memory*
- *Has typical access time of 250 nsec*

Designed for applications requiring as many as 10,000 erase/write cycles per register, the XL93C46 holds 1024 reprogrammable bits of information. The EEPROM, which has a typical access time of 250 nsec, is organized into 64 registers of 16 bits each. You can serially read or write information to each register by means of a 4- or 8-bit controller or a standard µP. The XL93C46 features a low-power standby mode that reduces power consumption by more than 80% compared with an NMOS device. The standby current for the XL93C46 is 100 µA; the typical operating current is 3 mA. In an 8-pin DIP, $1.70; in an 8-pin SOIC, $3.26 (100).

Exel Microelectronics Inc, Box 49007, San Jose, CA 95161. Phone (408) 432-0500. TWX 910-338-2116.

Circle No 352



DIGITAL CORRELATOR

- *Provides 64-bit comparison*
- *Searches 50-MHz data streams*

Designed for applications such as image-recognition systems, the L10C23 64-bit correlator chip searches for a 64-bit pattern in a 50-MHz data stream in 20 nsec. The device compares the 64-bit data stream value with the 64-bit value being sought and generates a 7-bit correlation score to indicate the degree of match. A 64-bit mask register can disable individual bits. For even faster operation, you can preload a 7-bit threshold value in the chip, and a compare-flag output pin will indicate if the 7-bit score exceeds the threshold value. You can cascade any number of L10C23s to search data streams for longer patterns such as 128 and 192 bits. The typical power consumption is 5V at 25 mA. The L10C23 is available in three speed ranges and comes in either a 24-pin ceramic leadless-chip carrier or a plastic DIP. $25 to $34.60 (1000).

Logic Devices Inc, 628 E Evelyn Ave, Sunnyvale, CA 94086. Phone (408) 720-8630.

Circle No 353

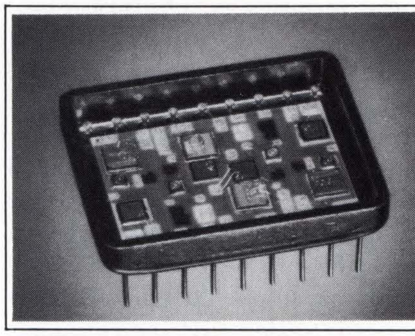
COLOR PALETTE

- *Supports 1280×1024-pixel displays*
- *Can display as many as 259 colors*

The Am81C458 color-palette chip supports full-page displays and is a plug-in replacement for the Brooktree Bt458 device. Used with the Am95C60 quad pixel dataflow manager (QPDM) and video dynamic RAMs, the Am81C458 supports graphics displays to 1280×1024 pixels and can simultaneously display 259 colors out of a palette of 16.8 million colors. The Am81C458 includes an input buffer, an input multiplexer, a 256-word×24-bit look-up table, a 4-word×24-bit overlay table, and three 8-bit RS-343A-compatible D/A converters. The device features pixel rates to 125 MHz and has a typical power dissipation of 1W. The Am81C458 comes in either an 84-pin PGA or an 84-pin plastic leaded-chip carrier. In the PLCC, 80-MHz version, $105; 110-MHz version, $112; 125-MHz version, $119 (100).

Advanced Micro Devices, Box 3453 Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 354



H-BRIDGE DRIVER

- *Has a 7A drive capability*
- *Features a 100V breakdown rating*

Available in either a hermetic DIP or a hermetic flatpack, the PH26450 is an H-bridge motor driver that features a drive capability of 7A and a minimum 100V breakdown-voltage rating for all output elements. The hybrid needs only 10 mA of input drive current to provide 4A of output load current. The PH26450 includes four Darlington transistors and four fast-recovery (30 nsec) epitaxial rectifiers, which eliminate current spikes during turn-on. The PH26450 interfaces directly to logic control circuits without need of additional buffers. The independent power-output stages let you drive unipolar or bipolar stepper motors, as well as other dc motors and solenoids. $62 to $99 (100), depending on the temperature range and screening option.

Micro Networks, 324 Clark St, Worcester, MA 01606. Phone (508) 852-5400.

Circle No 355

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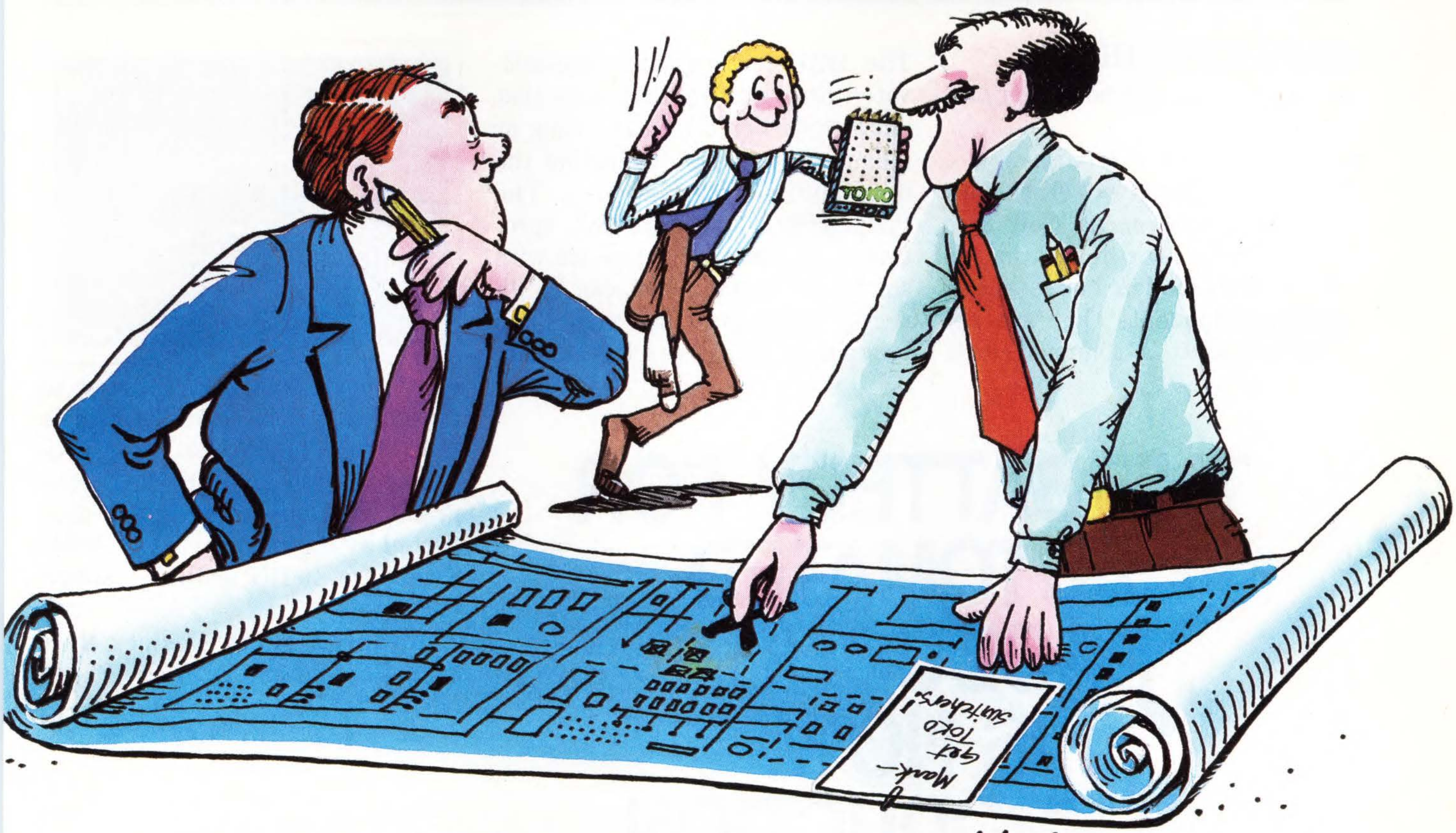

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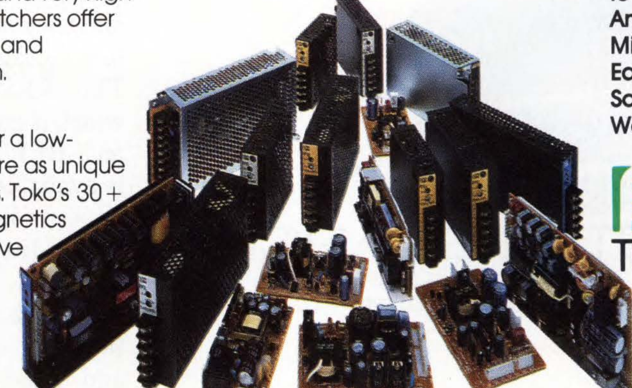
EM	170-264	10W	3	6
		15W		
PU & PS	85-132/	10W	1	192
	110-175/	15W		
	170-264	30W		
		50W		
PE&PT	85-132/	15W	3 (PT)	60
	170-264	30W	1 (PE)	
		50W		
MW	85-264*	15W	3	7
		30W		
		50W		

*Automatic (no jumpers required)



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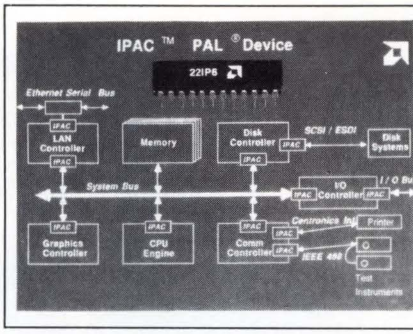
CIRCLE NO 203

INTERFACE CHIP

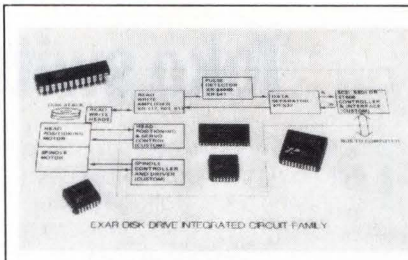
- *Provides asynchronous communication*
- *Features six 48-mA outputs*

The PAL22IP6 IPAC (Interface Protocol Asynchronous Cell) is a programmable logic device that allows communication between two system components that are not synchronized to a common clock. The IPAC features six edge-activated programmable flip-flops that store signals on their own rising or falling edges, thus eliminating the need for a separate clock. The PAL22IP6 is a 24-pin PAL (programmable array logic) device with six 48-mA outputs that can be directly connected to most bus backplanes. The device has 16 dedicated inputs and a PAL array to implement two-level AND-OR logic functions. The PAL22IP6 is programmable on standard PAL programmers, and its design is supported by the company's PALASM-2 software. In DIP or PLCC, $13.95 (100).



Advanced Micro Devices, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 356



DISK-DRIVE ICs

- *Features Read/Write amplifiers*
- *Has a pulse detector circuit*

Designed for medium-capacity Winchester disk-drives, the XR-501 and XR-511 Read/Write amplifiers provide an interface for eight disk-drive heads and their controller circuitry. The ICs have a programmable write-current source and a low-noise ($0.8\ nV\sqrt{Hz}$) read amplifier, and they are fully protected against low-voltage power supply faults. The XR-8464B pulse detector, which is compatible with both MFM and RLL clock-encoding schemes, is available with pulse-pairing accuracies of better than 0.5 nsec at 2.5 MHz. Internally, the XR-8464B uses ECL logic to minimize current transients; the output is fully Schottky/TTL compatible. The XR-501 and XR-511 come in PLCC and

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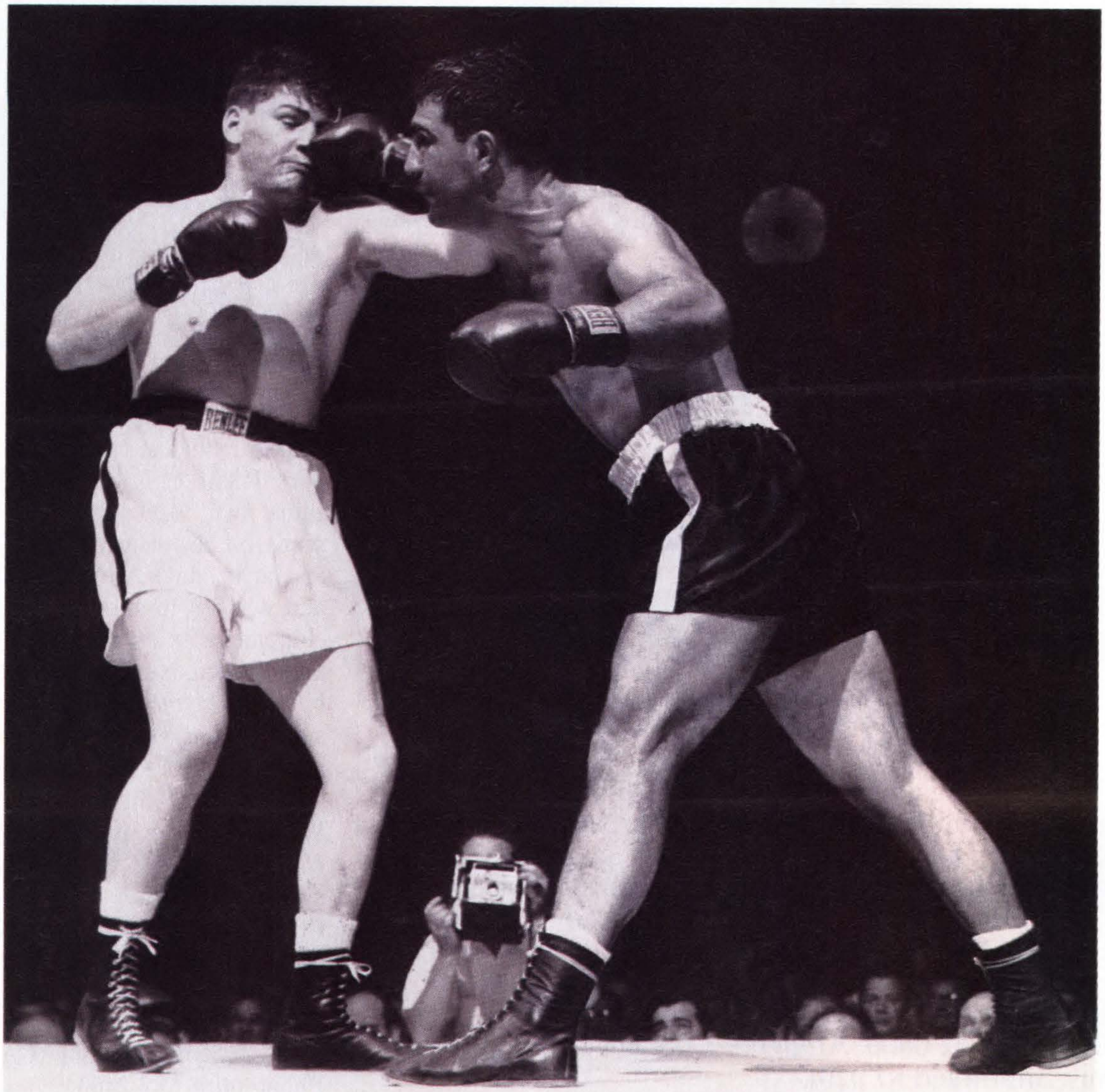

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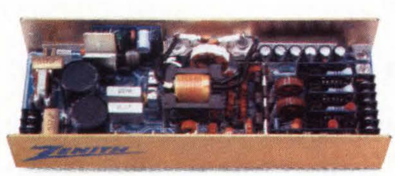

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ZPS-250-N	250	4.75/5.25	3.5/35.0	10.0/15.5	0.4/4.0 PK6	10.0/15.5	0.4/4.0 PK6	4.75/5.25	0.3/3.0	5.0 x 2.5 x 13
ZPS-300-N	300	4.75/5.25	4.5/45.0	10.0/15.5	0.8/8.0 PK12	10.0/15.5	0.8/8.0 PK12	4.75/5.25	0.4/4.0	5.0 x 2.5 x 13
ZPS-400-N	400	4.75/5.25	5.5/55.0	10.0/15.5	1.0/10.0 PK15	10.0/15.5	1.0/10.0 PK15	4.75/5.25	0.6/6.0	6.0 x 2.5 x 13

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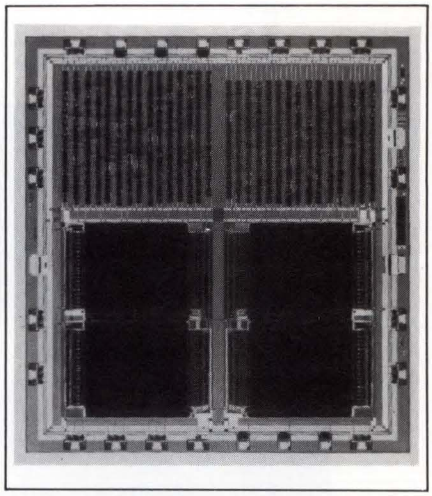
Exar Corp, Box 49007, San Jose, CA 95161. Phone (408) 434-6400. TWX 910-339-9233. FAX 408-943-8245.

Circle No 357

BIDIRECTIONAL FIFO

- *Contains two 512×9-bit FIFOs*
- *Includes multiplexing logic*

The 67C4701 bidirectional FIFO facilitates the exchange of data bidirectionally between devices with different data transfer rates. The device provides an asynchronous full-duplex connection between two CPUs working in a multiprocessing mode, or between a CPU and a peripheral device. Based on a dual-port RAM cell, the 67C4701 contains two 512×9-bit FIFOs (the ninth bit is reserved as a framing, or parity, bit), which can be read and written to simultaneously. The chip includes all necessary control and multiplexing logic circuits. A byte-detect mode allows a comparison between the value of bytes being read and an 8-bit value preprogrammed into the internal register. When the specified value is read from the FIFO, the device generates an interrupt to tell the host that a byte detect has occurred. The 67C4701 is packaged in a 28-pin DIP. $42.50 (100).



Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 358

BUS INTERFACE

- *Is a remote terminal interface for 1553B bus systems*
- *Decouples a CPU from 1553B bus transactions*

The MCT83000 is a MIL-STD-1553B remote-terminal interface that allows 1553B bus transactions and a host CPU's 1553B bus I/O operations to take place asynchronously without significant timing constraints. On the processor side of the interface, the host CPU has continuous access to a 2k×16-bit dual-port RAM, which contains validated received 1553B bus mes-

C&C Computers and Communications

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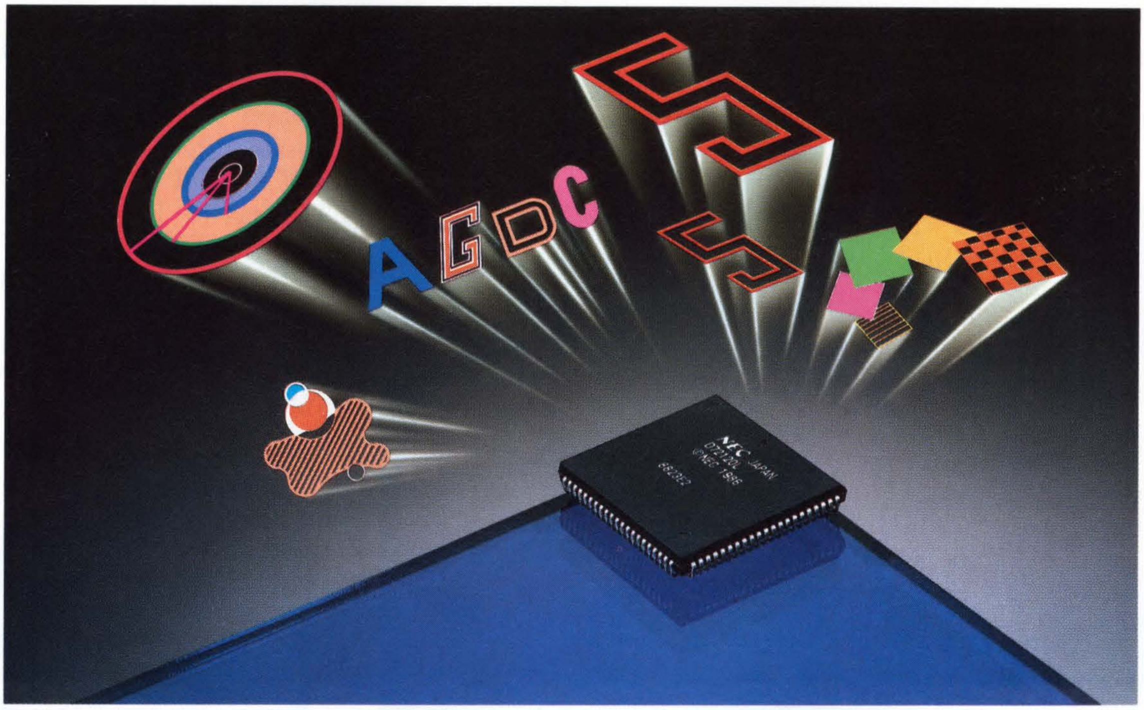

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The AGDC has all the graphics capabilities you need – including draw, paint and copy – hardwired into one chip. In overall speed and versatility, the AGDC outperforms every other "programmed" chip on the market. Higher performance flows from four on-chip processors that function independently for optimum efficiency. The AGDC supports a 32M-byte memory and offers an impressive array of features, including:

- ☐ 4K x 4K bit map x 65,536 colors.
- ☐ 27 drawing functions with a wide variety of drawing modes.
- ☐ Line drawing speed: 2 million pixels/sec.
- ☐ Powerful filling functions with tiling patterns for both arbitrary and fixed areas including triangles, trapezoids, circles and ellipses.
- ☐ Bit BLT including arbitrary-angle slant, rotation, enlarge, shrink and inter-plane transfer.
- ☐ Bit BLT speed: 32M bits/sec.
- ☐ Supports dual-port memories.

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NEC

CIRCLE NO 205

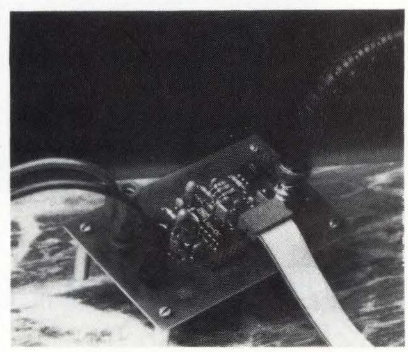
sages or 1553B messages that are ready for transmission. Similarly, the 1553B remote terminal controller chip, which is integrated into the device, has continuous access to a separate 2k × 16-bit dual-port RAM containing complete 1553B bus messages ready for transmission and received 1553B bus messages. Integral control logic performs burst-mode transfers of complete 1553B bus messages between the two dual-port RAMs at appropriate times during 1553B bus operation, freeing the host CPU of the delays that can occur with other remote terminal interface devices. The MCT83000 is also available with 4k × 16-bit dual-port RAMs to provide separate data buffers for broadcast commands in accordance with MIL-STD-1553B notice 2. The hybrid device also contains low-power 1553B bus transceivers. The MCT83000 is available in a 2.375-in. square, 90-pin quad in-line package or flat-pack. Around $1200 (100).

Marconi Electronic Devices Ltd, Microsystems Div, Hargreaves Rd, Groundwell Industrial Estate, Swindon, Wiltshire SN2 5BE, UK. Phone (0793) 727005. TLX 444460. FAX 079-372-3348.

Circle No 359

Marconi Electronic Devices Inc, Microsystems Div, 45 David's Dr, Hauppauge, NY 11788. Phone (516) 231-7710. TLX 275801. FAX 516-231-7923.

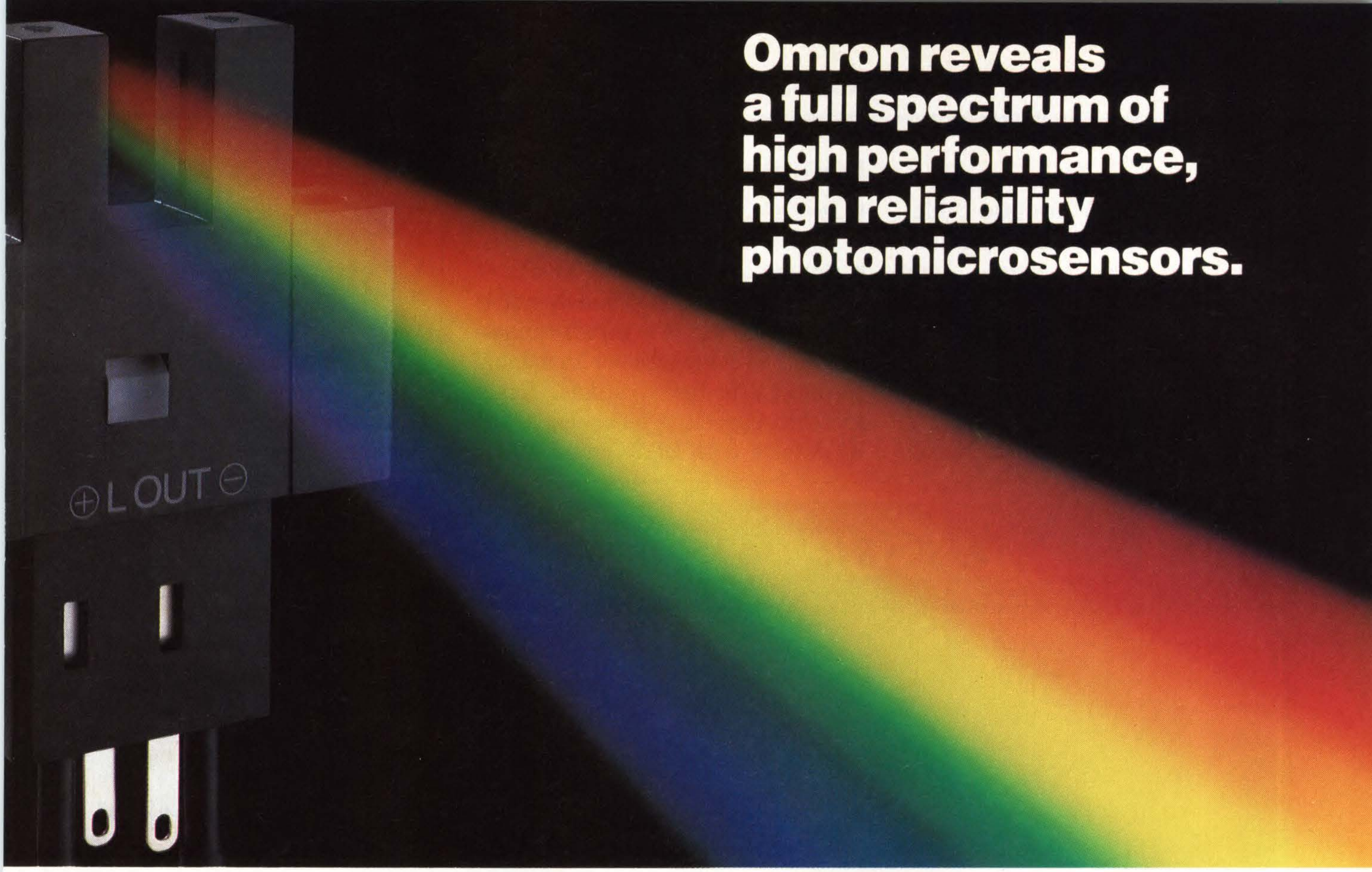
Circle No 360



DATA RECEIVER

- *Works with line lengths to 6000 feet*
- *Accepts RZ and NRZ data formats*

The LIU-01 is a high-speed serial data receiver capable of operation on line lengths of 0 to over 6000 feet. The IC accepts both RZ and NRZ data formats and is suitable for ISDN and high-speed LAN applications. The LIU-01 internally separates the data and transmitted clock of the incoming signal and presents both as TTL/CMOS outputs for direct interface to μP-based systems. The IC provides automatic compensation for variable transmission line lengths at data rates to 4M bps. Communication equipment using the LIU-01 can interface directly with T1, T148, and T1C



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CIRCLE NO 206

twisted-pair telephone lines and with coaxial or fiber-optic cables. The IC is available in 16-pin DIP, CERDIP, and SO packages. From $12.00 (100).

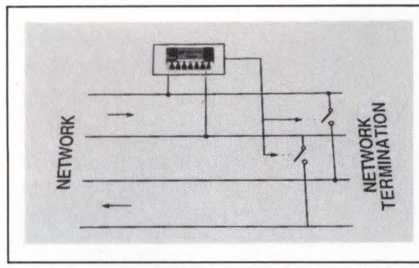
Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-7384. TLX 713719541. FAX 408-727-1550.

Circle No 361

LOOPBACK DETECTOR

- *Detects 2713- and 2813-Hz signals*
- *Conforms to Bell PUB 43004*

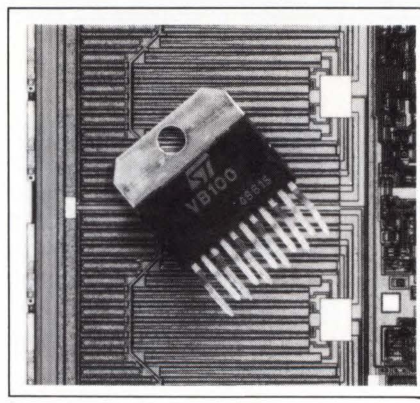
The XR-T2713 loopback detector is designed for use in 4-wire terminating units in conjunction with manual or automatic test systems. Using switched-capacitor technology, the IC detects both 2713- and 2813-Hz



signals and performs the loopback in accordance with Bell PUB 43004. The XR-T2713 features a low operating current of 3.5 mA at 12V, pin-selectable detection bands accurate to ±15 Hz, a detection level to −34 dB, and complementary TTL-compatible outputs. The device comes in a 16-pin DIP. $5.02 (1000).

Exar Corp, Box 49007, San Jose, CA 95161. TWX 910-339-9233. FAX 408-943-8245. Phone (408) 434-6400.

Circle No 362



SMART POWER IC

- *Drives loads as high as 2 kVA*
- *Incorporates a pulse-width modulation controller*

The VB100 smart power driver contains a pulse width modulation controller and a Darlington power output stage that can handle voltages as high as 450V and currents as high as 5A. In applications such as the direct drive of dc motors from rectified line supplies, the VB100 can control loads as high as 2 kVA using only four external components. The device has on-chip thermal protection circuitry and is packaged in an 11-lead Multiwatt power package. $5 (100).

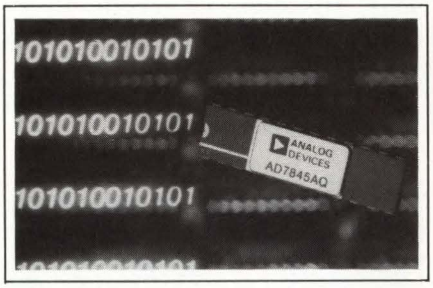
SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate

Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 363

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 364



MULTIPLYING DAC

- *12-bit, 4-quadrant type*
- *Includes on-chip output amplifier*

The AD7845 12-bit multiplying D/A converter features 4-quadrant operation, an on-chip amplifier, and interfaces for popular 16-bit μPs. External connections let you configure the AD7845 for either unipolar or bipolar operation, as a programmable-gain amplifier, or as a programmable current source. The DAC is monotonic over the full operating temperature range, and has a maximum of ±1 LSB differential nonlinearity. The on-chip amplifier and feedback resistor perform current-to-voltage conversion with relative accuracy to within ±1 LSB. The internally compensated output amplifier delivers a ±10V swing into a 2-kΩ load and settles to 0.01% FSR in <5 μsec. The full-power bandwidth is 250 kHz, and the unity-gain small-signal bandwidth is 600 kHz with a 7V/μsec slew rate. Package options include a 24-pin plastic or ceramic DIP. Three temperature ranges are available. From $7.40 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 935-5565. TWX 710-394-6577.

Circle No 365

FLASH A/D CONVERTERS

- *Include an input amplifier and voltage reference*
- *Sample at frequencies as high as 15 MHz*

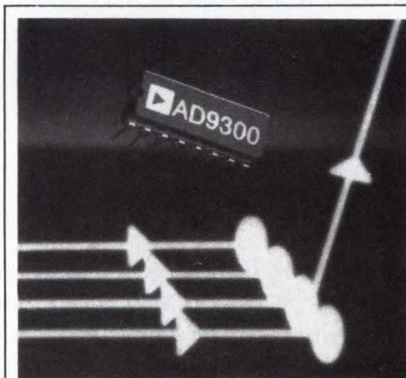
Incorporating an input amplifier, voltage reference, and an 8-bit A/D converter, SO1080-series flash A/D converters contain all the circuitry required to convert high-speed analog signals into 8-bit data. They are capable of maintaining their 0.5 LSB integral or differential nonlinearity specification at sampling rates as high as 10 MHz. You can operate them at higher sample rates if you're prepared to accept reduced performance. The SO1080 has an input dynamic range of 0 to 5V and incorporates power supply regulators that allow you to power its analog circuitry from an 8 to 20V positive supply and a 3 to 17V negative supply. The SO1081 has an input dynamic range of 0 to 3V and requires regulated ±5V supplies for its analog circuitry. The SO1082 and SO1083 incorporate input and feedback resistors around the input amplifier that allow you to select positive input dynamic ranges of 0 to 0.75, 1, 1.5 or 3V, or negative input dynamic ranges of 0 to −1, −1.5, or −3V. You can also configure these versions to accept bipolar inputs. Both the SO1082 and SO1083 feature buffered reference-voltage outputs of +3V for the SO1082 and −1.5V for the SO1083. All the converters are housed in 24-pin DIPs and dissipate less than 1W of power. SO1080 and SO1081, around $200; SO1082 and SO1083, around $220 (100).

Sorep SA, Z I Bellevue, Box 5, 35220 Chateaubourg, France. Phone 99623955. TLX 740573. FAX 99003247.

Circle No 366

Sorep Technology Corp, Box 4364, Houston, TX 77210. Phone (713) 923-5200. TLX 166081. FAX 713-923-4182.

Circle No 367



FOUR-CHANNEL MUX

- *Full-power bandwidth of 34 MHz*
- *Small-signal bandwidth of 350 MHz*

The AD9300 video multiplexer provides 4-to-1 channel switching for video signal routing, medical imaging, and ECM applications. The monolithic IC has a typical full-power bandwidth of 34 MHz (30 MHz min) and a small-signal bandwidth of 350 MHz. The gain of the AD9300 is flat within ±0.1 dB to 8 MHz. The circuit lets you randomly switch any of the four inputs to the output at rates exceeding 20 MHz with a two-bit channel-select code. You can combine multiple AD9300s in either parallel or cascade arrangements to form larger switching matrices. When not enabled, the mux output has a high-impedance state; when enabled, the mux acts as a buffer with high input and low output impedances. Other features include 75 dB of crosstalk rejection at 10 MHz and 0.05° differ-

Text continued on pg 354

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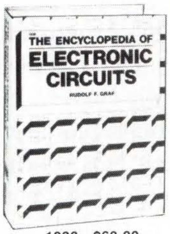

1938 $60.00
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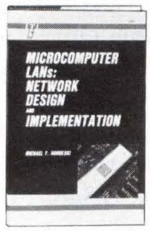
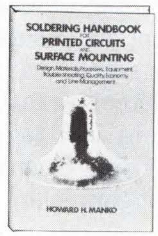
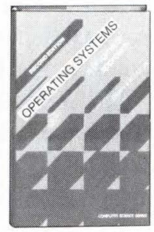


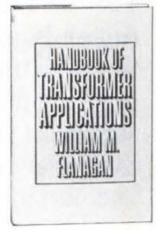
2888 $28.95



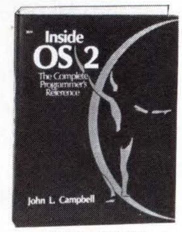
9825 $49.95



9808 $34.95



9788 $49.50



3019 $39.95
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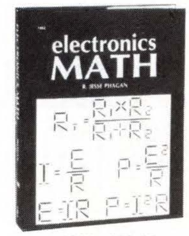
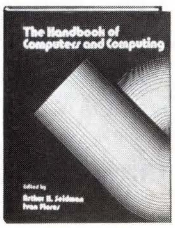
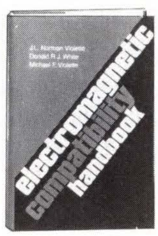


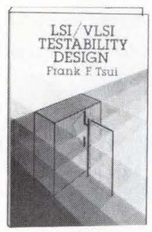
1962 $22.95



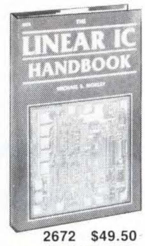
9785 $79.95



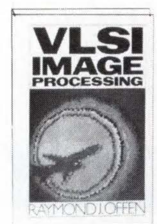
9781 $68.95



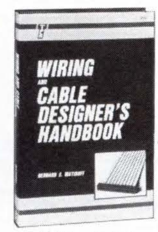
9799 $49.95



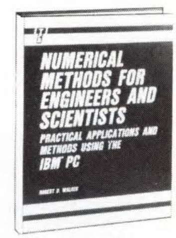
2672 $49.50
Counts as 2



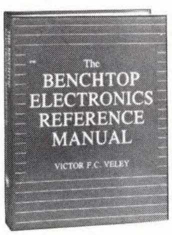
9832 $36.95



2720 $32.50



2697 $19.95



2785 $39.95
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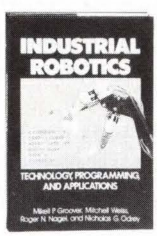
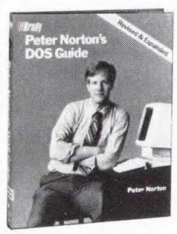
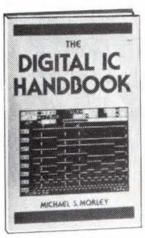


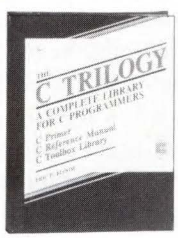
9794 $35.95



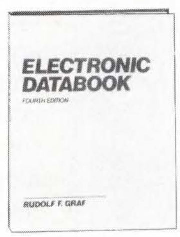
9083 $29.95



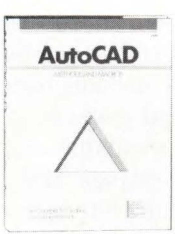
3002 $49.50
Counts as 2



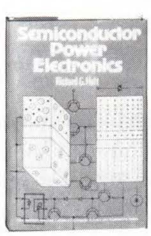
2890 $32.95



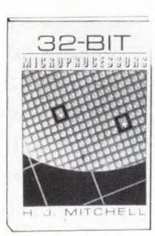
2958 $34.95



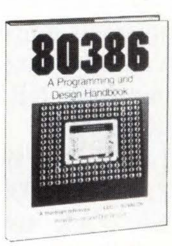
2989 $29.95



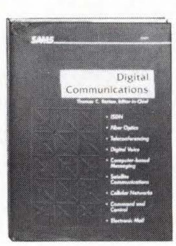
9820 $46.95



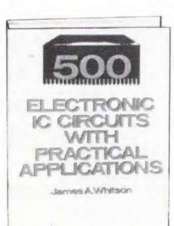
9829 $45.00



2937 $29.95



9773 $44.95



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CIRCLE NO 207

ential phase error. The AD9300 operates from ±10V to ±15V supplies. The IC is available in a 16-pin ceramic DIP and a 20-pin LCCC. From $8.00 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TLX 924491. TWX 710-394-6577.

Circle No 369

FAULT INTERRUPTER

- *Detects electrical ground faults*
- *Provides interface to an SCR*

The LM1851 Ground Fault Interrupter is a direct replacement for the industry-type bearing the same part number. The device detects hazardous grounding conditions in consumer and industrial wiring. The output of the LM1851 triggers an external SCR, which opens a circuit breaker to prevent a harmful or lethal shock. The device complies with UL943 timing standards to ensure immunity to false triggering caused by line noise. The LM1851 features adjustable fault-current integration time and adjustable fault-current threshold. You can configure the LM1851 to detect both normal faults (hot wire to ground) and grounded neutral faults. The device is available in 8-pin DIP and 8-pin small-outline packages. $1.19 (100).

Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94043. Phone (415) 968-9211.

Circle No 370

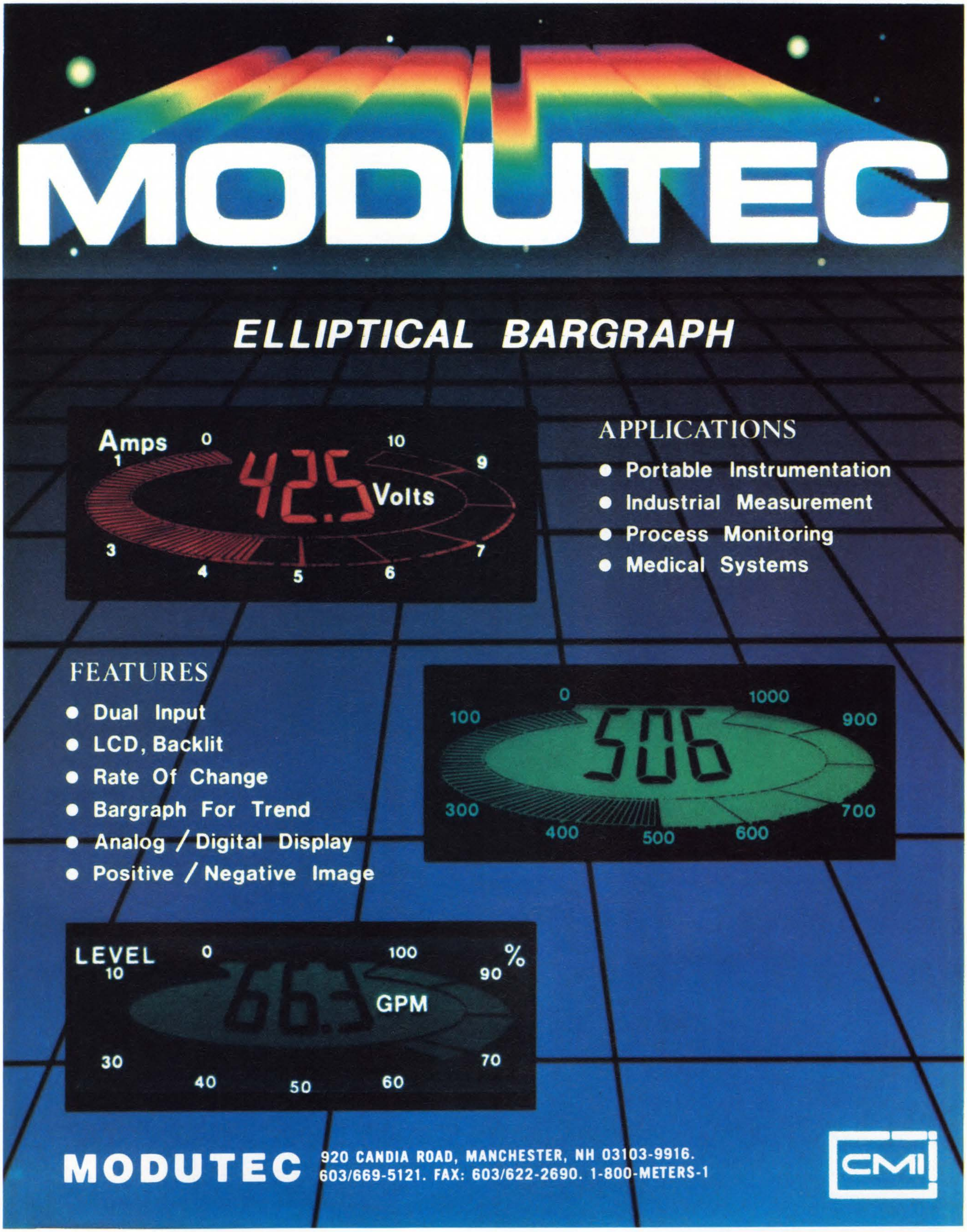
ANALOG ARRAY

- *Provides dielectric isolation*
- *Has complementary npn/pnp transistors*

The SP1104 is a high-density analog array that provides such features as dielectric isolation and vertical, complementary npn and pnp transistors. The array also uses thin-film nichrome resistors and dual-layer aluminum metalization. Each transistor in the SP1104 is fully isolated, allowing the designer to use conventional discrete design techniques. The complementary transistors provide similar performance. The npn transistors have a beta of 200 and an f_T of 1 GHz; the pnp transistors have a beta of 100 and an f_T of 600 MHz. Performance features of the SP1104 include bandwidths to 30 MHz and gains to 120 dB. The device is available with either 20V or 35V ratings and is supported with a complete set of SPICE model parameters. Also available is the SP1104 Macro Cell library, which includes op amps, voltage references, transimpedance amplifiers, and comparators. NRE charges start at about $20,000.

Sipex Corp, Data Linear Div, 491 Fairview Way, Milpitas, CA 95035. Phone (408) 945-9080. FAX 408-964-6191.

Circle No 371



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COMPONENT OF AMERICA, INC.
CIRCLE NO 209

COMPUTERS & PERIPHERALS

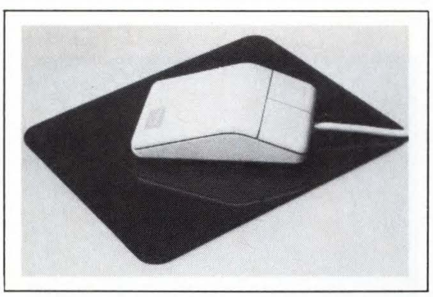
PORTABLE COMPUTER

- *Comes with either a 16-MHz 80286 or a 20-MHz 80386 CPU*
- *Has an electroluminescent flat-panel display*

The portable add-in computer (PAC) is IBM PC/AT-compatible and comes in two versions. The 16-MHz 80286 CPU version weighs just under 20 lbs, and the 20-MHz 80386 CPU version weighs slightly over 20 lbs. The 80386 version has a RAM cache and delivers a performance figure of 4.5 MIPS. The units come with a yellow or orange electroluminescent flat-panel display. The display measures 80 characters × 25 lines and has a 640 × 400-pixel resolution. A gas plasma display is optional. The system also comes with 1M byte of main memory (expandable to 8M bytes), a 1.2M-byte 5¼-in. floppy-disk drive, a 20M-byte hard-disk drive, and an 86-key keyboard. The 16-MHz 80286 version, from $4270; the 20-MHz 80386, 4.5-MIPS version, $7470.

Dolch American Instruments Inc, 2029 O'Toole Ave, San Jose, CA 95131. Phone (800) 538-7506; in CA, (408) 435-1881. FAX 408-435-8260. TWX 910-338-2023.

Circle No 375



MOUSE

- *Has a variable resolution from 20 to 2000 counts/in.*
- *Optical sensors provide an MTBF of greater than 20 years*

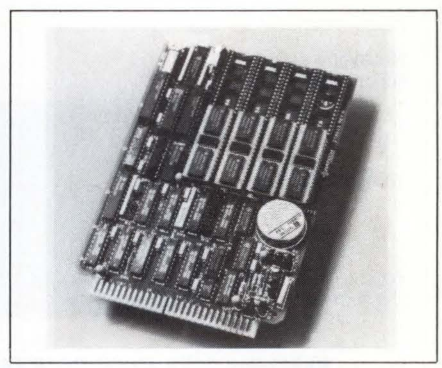
Designed for high-end applications, the PC Mouse II input device has a built-in accelerator that lets the user determine how fast the mouse moves the screen cursor. The unit achieves variable resolutions from 20 to 2000 counts/in. with nine different speed settings. In addition, the mouse boasts a counted-error accuracy of <1% of the total counts. Incorporating a 2-button design and a 9-ft cable, it comes with software for automatic installation, a mouse driver, and pop-up menus. It's designed to operate using the Microsoft Corp mouse protocol. It uses optical technology to sense position on a 5¾ × 7-in. mouse pad. Because the sensors are optical, the MTBF is greater than 20 years, and the unit comes with a lifetime warranty. $149.

MSC Technologies Inc, 47505 Seabridge Dr, Fremont, CA 94538. Phone (415) 656-1117. FAX 415-770-1924.

Circle No 376

MEMORY BOARD

- *Uses the Expanded Memory Specification for the STD Bus*
- *Provides as much as 2M bytes of PROM or RAM*



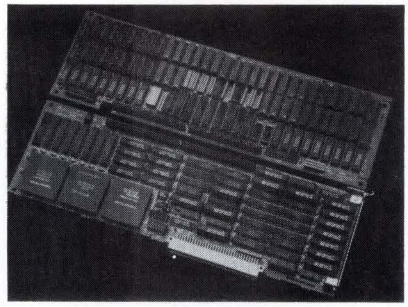
The ZT 8825 memory board for the STD Bus uses the Expanded Memory Specification (EMS) developed by Lotus, Intel, and Microsoft (LIM) to overcome the 640k-byte limitation in STD DOS applications. The board can have as much as 2M bytes of PROM or RAM or battery-backed RAM. For non-STD DOS applications, you can use the board as a standard 1M-byte memory board. The board is compatible with the company's family of STD Bus CPU boards based on the 8088, V20, and V50 μPs. It is also compatible with boards that meet the STD-8088 specification. It contains eight 32-pin JEDEC sockets that accept either 28- or 32-pin EPROMs, EEPROMs, and static RAMs. $395.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. TLX 4992316.

Circle No 377

COPROCESSOR

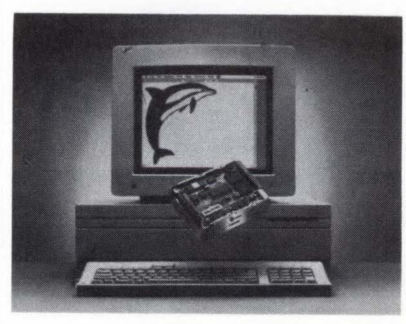
- *Achieves 20M flops for the Macintosh II*
- *Has an optimizing compiler*



The MC3200NU floating-point coprocessor board for the Macintosh II computer achieves 20M flops and 10 MIPS performance ratings. It comes with 2M, 4M, 6M, or 8M bytes of memory that is 2-way interleaved on a 40M-byte/sec onboard bus. The single-slot board is based on Weitek's XL-8032 RISC processor chip set, which includes the WTL-3132 32-bit floating-point unit. The board can be used as both a master and a slave on the Nubus, and it supports block and nonblock mode transfers for 8-, 16-, and 32-bit data. As a master, it can transfer data independent of the host anywhere in the 4G-byte address space of the Nubus. The board runs on the same operating system as the host so the host CPU can handle operating-system calls, multitasking operations, and graphics while the board is performing the number crunching. 2M-byte system hardware, $10,000; Fortran and C development software, $8500.

Mercury Computer Systems Inc, 600 Suffolk St, Lowell, MA 01854. Phone (508) 458-3100. FAX 508-458-9580.

Circle No 378



DISK DRIVE

- *Its 3½-in. form factor fits in the Macintosh II*
- *Formatted capacity of 80M bytes*

The AM80-IIi 3½-in. hard-disk drive fits in the position usually set aside for a second floppy-disk drive in the Macintosh II computer. The drive has a formatted capacity of 80M bytes which, when combined with the hard-disk drive in the standard Macintosh II computer, expands the available storage space to 120M bytes. The drive features an average access time of 19 msec and an MTBF of 50,000 hours. It

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CIRCLE NO 210

measures 1.625×4.0×5.75-in. and weighs 2 lbs. The drive comes with the necessary mounting hardware for installation, utility software, and a 1-year warranty. $1995.

Dolphin Systems Technology, 603-B E Alton Ave, Santa Ana, CA 92705. Phone (714) 546-6938. FAX 714-546-1435.

Circle No 379

HANDHELD COMPUTER

- *Runs IBM PC and HP-41C compatible software*
- *Has an 8-line×21-character display*

Featuring an 8-line×21-character LCD, the MC-II handheld computer contains a 5-MHz 80C88 μP and an operating system similar to DOS; these characteristics allow many applications written for the IBM PC computer to run with little or no modification. In addition, the unit can run programs written in MBase, MC-Basic, C, and programs written for the HP-41C calculator. It has two RS-232C ports, and it has a Kermit file-transfer program for transferring data to a PC or a mainframe computer. It also accepts data from a bar-code laser scanner or a smart wand. The unit comes with 128k bytes of RAM, which is expandable to 512k bytes. A built-in text editor supports EPROM application modules. The unit measures 8.25×3.75×1.75 in. and weighs 1.4 lbs. With 41M software for running HP-41CX programs, $750.

Corvallis MicroTechnology Inc, 895 NW Grant Ave, Corvallis, OR 97330. Phone (503) 752-5466.

Circle No 380

GRAPHICS ADD-IN

- *Is compatible with IBM CGA, EGA, VGA, and PGA graphics*
- *Has as much as 4M bytes of on-card video memory*

The TT786 add-in graphics card for IBM PCs and compatible computers provides both digital and analog outputs, allowing you to drive standard monitors at resolutions as high as 800×560 pixels. In analog mode the card allows you to simultaneously display as many as 256 colors from a palette of 262,144 colors. It's compatible with IBM CGA and EGA digital graphics adapters, and with the IBM VGA and PGA analog

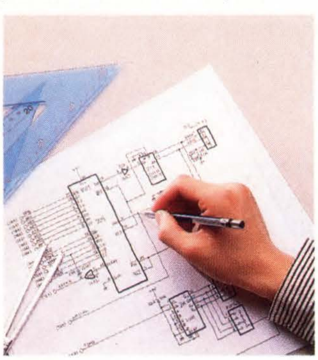
50th Anniversary

Eliminate the noise from your design.

A MUST FOR IC BOARD DESIGN

The problem of constructing IC boards free from electromagnetic interference is one you can easily solve with Tokin EMC Filters.

But if you wait until you've started designing the board, it's already too late; it's something you need to consider *before* you begin. The Tokin EMC Chip Filters above are a good example. By including them in the IC design from the start, the designer can create an IC board that enables the end user to enjoy the full, unrestricted potential of the board's performance. That's why more and more companies are using Tokin EMC components in a mushrooming range of electronic products throughout the world every day.



AN ANSWER FOR YOUR EVERY DIGITAL NEED

Digital electronics are changing the shape of the world we live in, in more ways than one. And to deal with EMI, the normal- and common-mode noise that attacks data communications terminals and digital equipment, Tokin has come to the rescue with an incomparable lineup of EMC data line filters that deliver clear, accurate data transmission. From easy-to-mount EMC Chip Filters for normal- and common-mode noise absorption, to DIP Noise Filters for high impedance over a wide frequency range.

Specifications (DIP Noise Filters)

Model	Circuit	Rated Current per Line (mA)
D-03C/ D-03C1	8 circuits; Common-mode	100
D-05N1	8 circuits; Normal-mode	100
D-07C1	8 circuits; Common-mode	300
D-08C2	4 circuits; Common-mode	2,300
D-08C2A	4 circuits; Common-mode	500
D-16C	4 circuits; Common-mode	100
D-20C	8 circuits; Common-mode	500
D-40C	3 circuits; Common-mode	300
D-42C	5 circuits; Common-mode	300
D-45C	8 circuits; Common-mode	300
D-47C	10 circuits; Common-mode	300
D-55C	5 circuits; Common-mode	300
D-58C	8 circuits; Common-mode	300

Specifications (EMC Chip Filters)

Model	Circuit	Frequency Range (MHz)	Impedance (Ω)	Rated Current (mA)
M608	1 circuit; Common-mode	5 ~ 200	≧300 (at 100MHz)	100
M614	1 circuit; Common-mode	5 ~ 100	≧700 (at 50MHz)	100
M620	1 circuit; Common-mode	5 ~ 50	≧1,000 (at 30MHz)	100
M720N	20 circuits; Normal-mode	50 ~ 300	≧50 (at 200MHz)	50

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TOKIN

Tokin Corporation
Hazama Bldg., 5-8, Kita-Aoyama 2-chome, Minato-ku, Tokyo 107, Japan Phone: 03-402-6166 Fax: 03-497-9756 Telex: 02422695 TOKIN J

Tokin America Inc.
155 Nicholson Lane, San Jose, California 95134, U.S.A. Phone: 408-432-8020 Fax: 408-434-0375
Chicago Branch: 9935 Capitol Drive, Wheeling, Illinois 60090, U.S.A. Phone: 312-215-8802 Fax: 312-215-8804

München Liaison Office
Elisabethstraße 21, 8000 München 40, Bundesrepublik Deutschland Phone: (089) 271 75 22 Fax: (089) 271 75 67 Telex: 5 24 537 tokin d

You can reach our agents by phone: London 01-837 2701; Paris 1-45 34 75 35; Milan (0331) 678.058; Munich (089) 5164-0; Seoul (02) 777-5767; Taipei (02) 7311425; Hong Kong 3-315769; Singapore 747-8668 graphics systems. The card is available with 512k, 1M, 2M, or 4M bytes of video memory. The 4M-byte version allows you to store and manipulate images containing as many as 8000×4000 1-bit pixels, or 2000×2000 8-bit pixels. An Intel 20-MHz 82786 graphics processor provides features that include a drawing speed of 35 nsec/pixel and hardware windowing capabilities. The company can provide a library of graphics routines for the card. £395 to £1400.

Tektite Ltd, Box 5, Felixstowe, Suffolk IP11 7LW, UK. Phone (0394) 672117. TLX 987458.

Circle No 381

FAX TRANSCEIVER

- *Provides voice announcements for incoming messages*
- *Optional storage of 120 pages for message relaying*

The NeFAX desktop facsimile and phone transceiver has four types of voice announcements. It allows users to record a message for incoming calls; it automatically reports the transmission of a document; it informs the sender of a successful data transmission; and it confirms the transmission status to a remote location. A high-speed transmission mode sends documents at speeds as high as 9 sec/page. A relay feature allows the unit to forward pages to as many as 20 other units. A 1M-or 2M-byte memory option lets the unit store 120 pages for forwarding at a preprogrammed hour. The device has 200×400-line/in. resolution and can record 16 levels of gray scale for photograph reproduction. It has speed dialing for as many as 200 numbers including 30 1-touch numbers. The unit measures $19 \times 15.7 \times 6.6$ in. with a telephone handset and weighs 31 lbs. $3495.

NEC America Inc, Facsimile Div, 8 Old Sod Farm Rd, Melville, NY 11747. Phone (800) 782-7329; in NY, (516) 753-7406.

Circle No 382

CONTROLLER

- *Provides eight serial I/O channels for Multibus II systems*
- *Runs an onboard 80386 μP*

The M-CC386/008 communications board for Multibus II systems controls eight synchronous/asynchronous serial I/O channels. Its onboard 16-MHz 80386 μP, 1M or 4M bytes of onboard RAM, 82380 DMA

controller, and optional 80387 math coprocesssor make it suitable for use in high-performance systems running standard operating systems such as Unix. The board also has sufficient functionality for use as a stand-alone system. The on-board RAM is dual-ported to the 80386 and the Multibus II iPSB. Each serial I/O channel supports RS-232C or RS-422 protocols, and operates at baud rates between 50 and 19.2k baud in asynchronous mode, or at a bit rate as high as 1.5M bps in synchronous mode. All baud and bit rates are software programmable, and all the serial channels provide full modem control. The board supports bit- and byte-synchronous modes for a variety of protocols including HDLC, SDLC, X.25, and IBM BiSync. Other features include four 32-pin JEDEC EPROM sockets, and an iSBX expansion interface. The iPSB interface supports the Multibus II message passing, built-in self-test, and interconnect space functions. $5495 to $6450.

Concurrent Technologies Ltd, Fairfax House, Causton Rd, Colchester, Essex CO1 1RJ, UK. Phone (0206) 42996. TLX 94012560. FAX (0206) 67333.

Circle No 383

Concurrent Technologies Inc, 25401 Cabot Rd, Suite 206, Laguna Hills, CA 92653. Phone (714) 768-3332. FAX 714-951-8902.

Circle No 384

MONITOR

- *Displays 1 page of a letter-size document at 80 dots/in.*
- *Provides an 8×10.7-in. viewing area for the Macintosh SE*

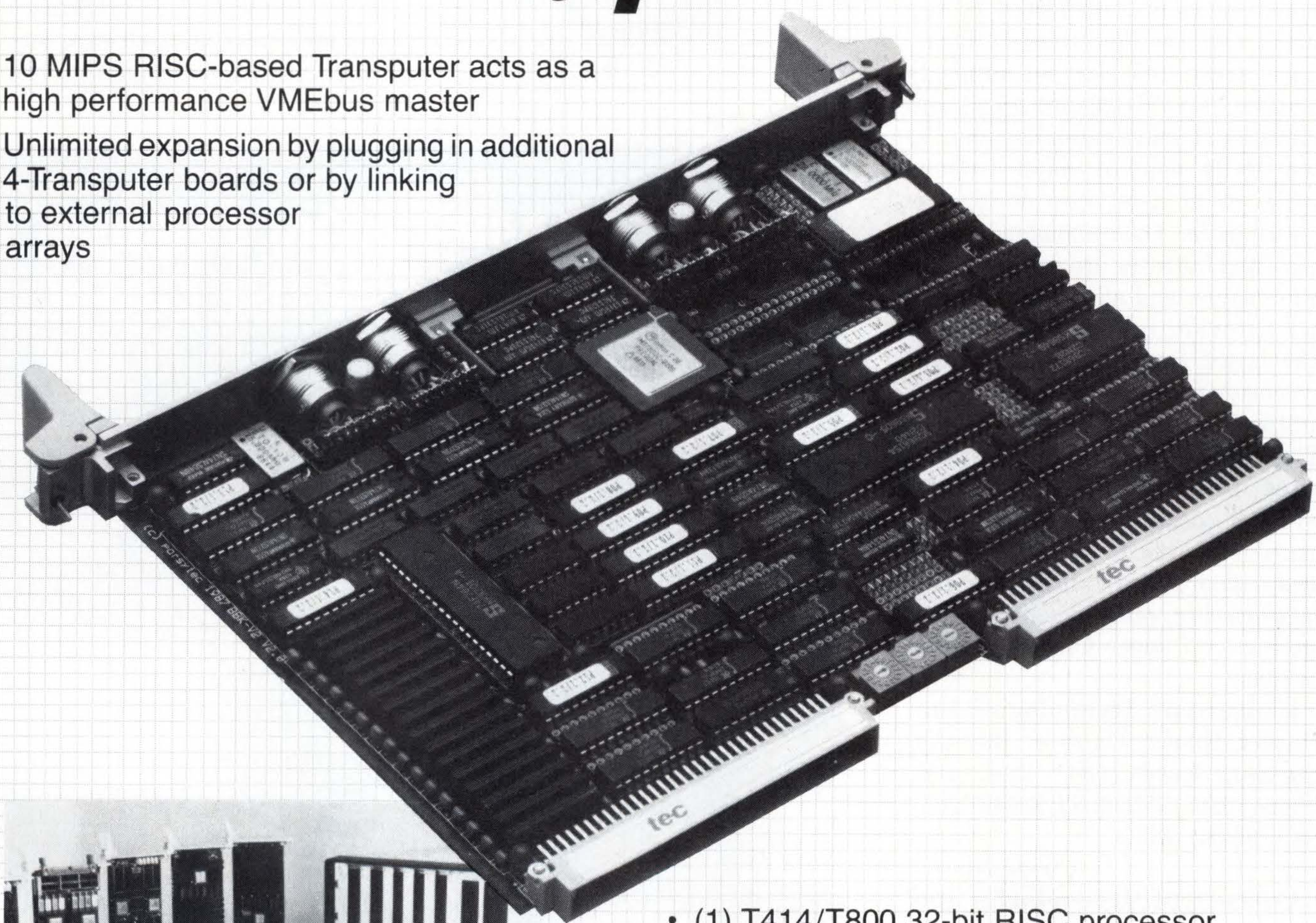
Providing an 8×10.7-in. viewing area for word-processing and single-page publication applications, the PageView is a 15-in. display monitor for the Macintosh SE computer. It has two display resolutions: An actual-size resolution displays 576×768 pixels, using 72 dots/in., and a letter-size resolution displays 640×870 pixels, using 80 dots/in. The letter-size model displays a single-page document on the screen. Other features include a noninterlaced screen refresh rate as fast as 97 Hz, a full tilt-and-swivel base, and contrast and brightness control switches. The software lets the user switch between the two

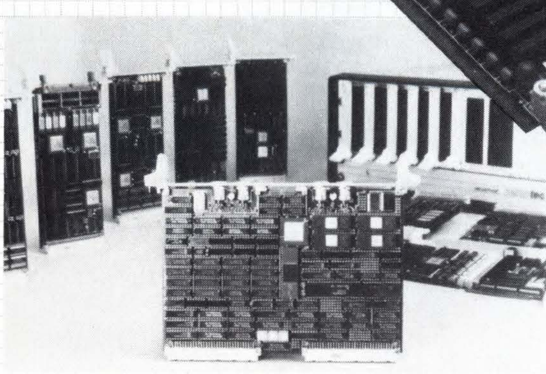
High Speed Bridge Brings Transputer Parallel Processing Power to VMEbus.

BBK-V2 by paracom

10 MIPS RISC-based Transputer acts as a high performance VMEbus master

Unlimited expansion by plugging in additional 4-Transputer boards or by linking to external processor arrays





- (1) T414/T800 32-bit RISC processor
- 2M-Bytes of dual ported RAM
- Full VMEbus master/slave capability (Rev. C, D8, D16, D32, A24, A32)
- (4) 20M-Bit/sec. communications channels
- Supports ultrafast Transputer block move with D8/D16/D32

The BBK-V2 board is complemented by a family of over 25 transputer-based boards and three separate levels of systems. They include interfaces to the IBM PC/XT/AT, IBM PS/2, Macintosh II (NUBUS), VME, Q-BUS, SCSI, Graphics Video Input, Parallel I/O, etc. An extensive software environment includes compilers for "C", FORTRAN, PASCAL, OCCAM, PARALLEL "C", PARALLEL PROLOG, and the "HELIOS" (Unix-like) distributed operating system with X-windows support.

Inexpensive starter kit packages for PC, PS/2 and Mac-II are now available.

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WEST CHICAGO, IL 60185

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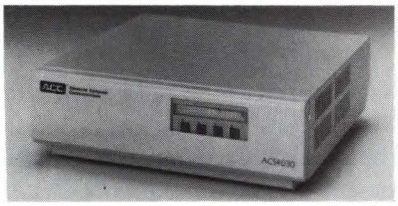
FAX (312) 231-0345

CIRCLE NO 164

resolution modes, select several cursor sizes, set a time delay before activation of a screen save feature, and select one of two system-font sizes. $999.

Sigma Designs Inc, 46501 Landing Parkway, Fremont, CA 94538. Phone (415) 770-0100. FAX 415-770-0110.

Circle No 385



ETHERNET BRIDGE

- *Links three or more LANs using the Spanning Tree Protocol*
- *A protocol-precedence feature prioritizes protocol types*

The ACS 4030 remote Ethernet bridge can connect three or more remote LANs to create a single network with transparent connections between all devices. The bridge implements the IEEE-802.1 specification better known as the Spanning Tree Protocol (STP). STP overcomes problems that occur when three or more linked networks create a situation where data packets travel in different directions and arrive out of order or continue to loop if a device is too busy to accept packets. The bridge also features protocol precedence, which prioritizes packet order according to protocol type. Protocol precedence also allows high priority for packets with time-sensitive local protocols such as DECnet Local Area Transport (LAT) and transmits them ahead of other packets in the queue. Base unit, $4975; STP implementation for either X.25 or point-to-point applications, $500.

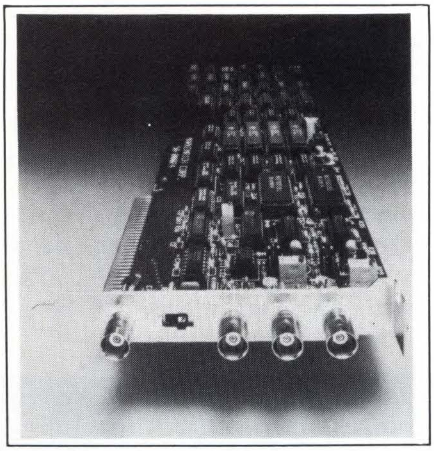
Advanced Computer Communications, 720 Santa Barbara St, Santa Barbara, CA 93101. Phone (805) 963-9431. TWX 910-334-4907.

Circle No 386

WAVEFORM BOARD

- *Acquires and arbitrarily generates waveforms*
- *Samples two channels simultaneously at 20-MHz rates*

The WAAG II waveform acquisition board and an arbitrary waveform generator on a single IBM PC card can simultaneously sample two input channels at rates as high as 20 MHz. Each channel has a standard 16k-byte data-buffer memory, which is optionally expandable to 64k bytes. The input video bandwidth is 40 MHz and minimizes phase distortion. The arbitrary waveform generator can synthesize either one-shot or continuous waveforms for two output channels. The synthesized waveform can be as



long as 32k bytes with an option that extends it to 64k bytes. Jumper straps allow the card to sample one channel at 40 MHz with 32k bytes of memory (or an optional 128k bytes), select X1 or X10 gain, and perform master/slave triggering for parallel channels. $1395.

Markenrich Corp, 1812 Flower Ave, Duarte, CA 91010. Phone (818) 359-9190.

Circle No 387

GRAPHICS BOARD

- *Uses TMS34010 graphics processor for VME Bus*
- *Provides 1280×1024-pixel resolution*

Based on TI's TMS34010 graphics-processor chip, the VG-1281 graphics board for the VME Bus has three gate arrays that allow the board to achieve drawing speeds of 100,000 vectors/sec and BitBlt transfers at 100M bps; the gate arrays also perform real-time zooming and smooth panning. The board provides a resolution of 1280×1024 pixels from a video RAM frame buffer, and it can display 256 colors from a palette of 16.7M colors. It has 1M byte of RAM to store firmware, display lists, fonts, and patterns. A graphics library called Lib Shell has over 185 commands and resides in onboard ROM. The command consists of primitives for drawing lines, circles, outlines, fills, and text along with 2D and 3D transforms. The board operates from a 5V supply and draws 3A typ. $4295.

Matrox Electronic Systems Ltd, 1055 St Regis Blvd, Dorval, Quebec, Canada H9P 2T4. Phone (514) 685-2630. TLX 05822798. FAX 514-685-2853.

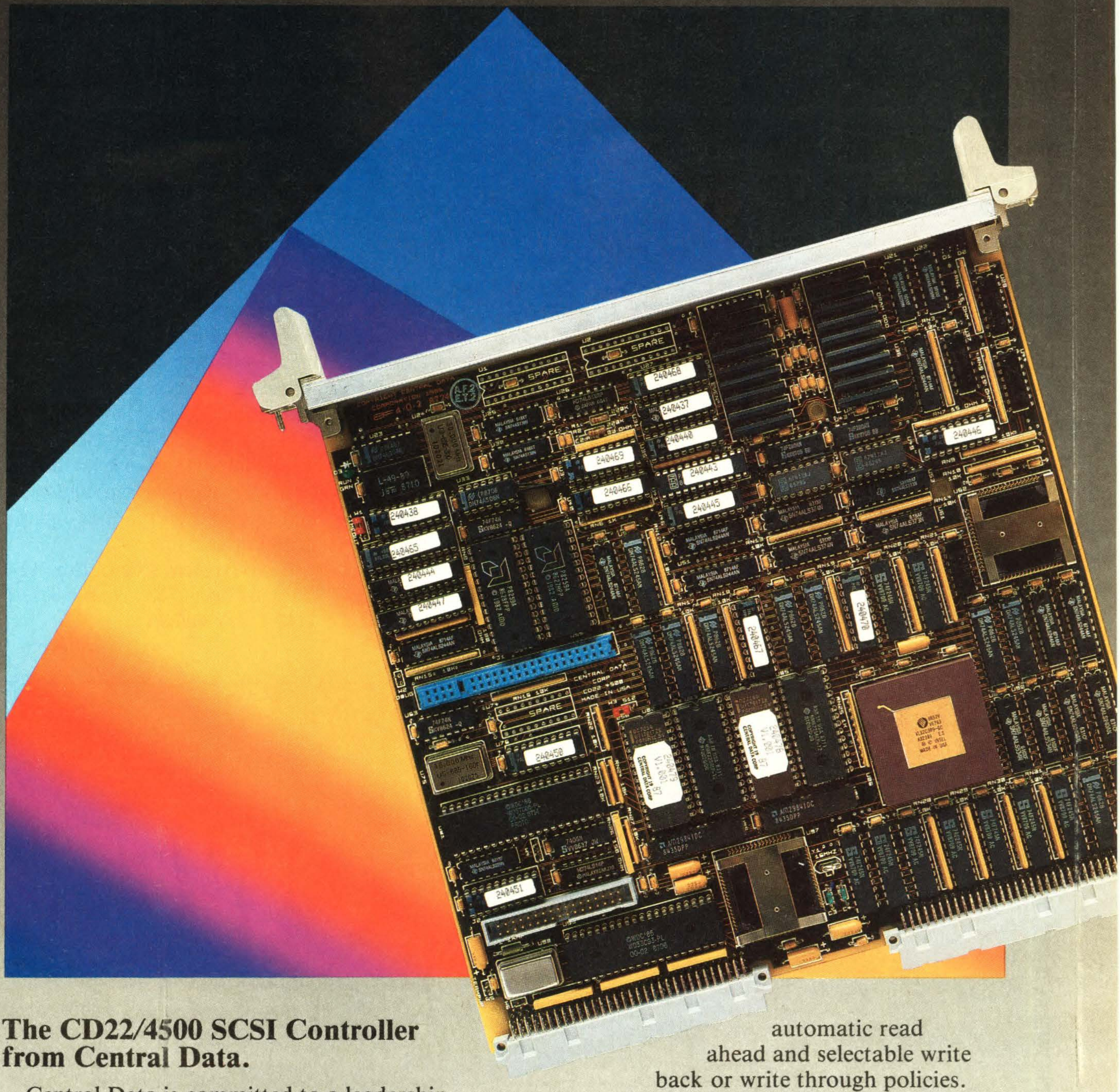
Circle No 388

GRAPHICS CONTROLLER

- *Provides 1280×1024 pixels for the IBM PC/AT*
- *Designed around TI's 3410 graphics processor*

The Artist Designer 12 graphics controller card for the IBM PC/AT, Compaq 386, and compatible computers is designed around TI's 34010 graphics processor to deliver 1280×1024-pixel resolution. It provides 256 colors from a palette of 16.7 million. The board supports drivers for IBM's professional graphics language (PGL), and the

Disk-Caching SCSI for Multibus* II.



The CD22/4500 SCSI Controller from Central Data.

Central Data is committed to a leadership role in the Multibus II market. With special emphasis on SCSI support.

The CD22/4500 provides the ultimate Multibus II SCSI solution. It's fast, transferring data at the limits of the SCSI bus. And versatile, providing either direct SCSI commands or Intel compatible PCI commands.

On-board disk-caching firmware makes it even faster. Up to 2 megabytes of parity protected RAM and 80186 CPU speeds of up to 12.5MHz mean cache hits are frequent and fast.

For extra efficiency, tune your systems using the four provided disk-sorting algorithms, automatic read ahead and selectable write back or write through policies.

Design excellence, unparalleled account service, easy access to design engineers, even customizing for some applications. You'll find them in this and every Central Data product.

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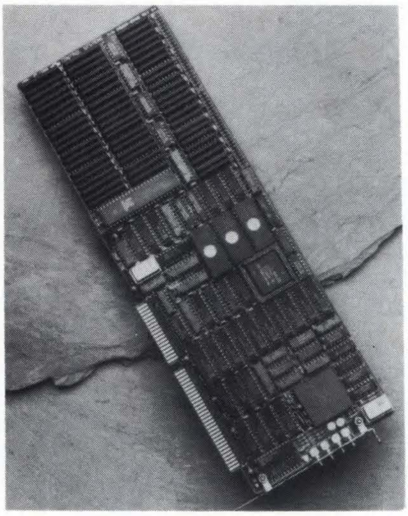
(In Illinois 217-359-8010)
FAX 217-359-6904

*Multibus is a trademark of Intel Corporation.

CIRCLE NO 213

direct graphics interface standard (DGIS) from Graphic Software Systems via onboard firmware. The graphics μP controls and executes all graphics functions, relieving the host from executing drawing algorithms and emulating graphics standards. The unit provides a horizontal scan rate of 64 kHz and a video bandwidth of 108 MHz. The frame buffer memory consists of 1.25M bytes of onboard video RAM. Board and software drivers, $4495.



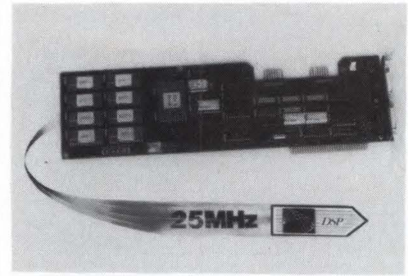
Control Systems, 2675 Patton Rd, St Paul, MN 55113. Phone (612) 631-7800. TLX 756601.

Circle No 389

DSP BOARD

- *Uses 25-MHz version of AT&T's WE DSP32 chip*
- *High-speed version performs a 1024 complex FFT in 5.7 msec*

The ZPB32-HS high-speed version of the company's ZPB32 DSP board utilizes a 25-MHz version of AT&T's WE DSP32 chip. It also contains 64k bytes of RAM with a 45-nsec access time and two sets of buffered serial I/O ports for passing data between multiple μPs or I/O cards. The serial ports can transfer data at 3M bps to internal devices and at 12M bps to external devices. The



software includes a utilities program that downloads DSP32 asssembler code and lets the user edit registers and memory, a C utilities library, and a disassembler program. Some performance benchmarks include calculation of a 1024 complex FFT in 5.7 msec, an FIR (finite impulse response) filter design with 160 nsec/tap, and a 32-bit multiply and accumulate operation in 160 nsec. $1495.

Burr-Brown Corp, Box 11400, Tucson, AZ 85743. Phone (602) 746-1111. TLX 666491.

Circle No 390

COLOR PRINTER

- *Uses thermal wax printing with 300 dot/in. resolution*
- *Prints 2D and 3D drawings using range of 7 to 4096 colors*

The 469RGB color screen printer uses thermal wax printing to achieve 300 dot/in. resolution. A 3-pass printing method produces color copies in 43 sec from display systems such as IBM's 5080, DEC's GPX, HP's 9000 series workstations as well as the company's 4111, 4115, and 4120 graphics terminals. A video adapter offloads the data on the screen in <4 sec. The printer can reproduce 2D and 3D drawings with a range of 7 to 4096 colors. The entire system consists of the company's 4693 Series Print Engine, which has a 2M-byte frame buffer (expandable to 8M bytes); a fiber-optic cable connection between the printer and the display, which can extend the distance between the two units to 100 ft; and a print controller with a 32-character LCD display for controlling the printer. 2M-byte frame buffer, $7700.

Tektronix IDG Marketing, Box 1000, MS 63-447, Wilsonville, OR 97070. Phone (800) 225-5434; in OR, (503) 235-7202.

Circle No 391

ACQUISITION UNIT

- *Has a 12-bit ADC for the IBM PS/2 and PC/AT*
- *Can sample at 1 MHz and perform DMA transfers to the host*

Suitable for IBM's PS/2 models 50, 60, and 80, an IBM PC/AT, or compatible computers, the System 12000 stand-alone data-acquisition unit contains an 8-channel, 12-bit ADC; a 2-channel, 12-bit DAC; and 24 digital I/O ports. The system can sample at 1 MHz and has a 256k-word × 16-bit memory for data storage. You can transfer data to the

host memory through DMA control independent of the host CPU. Other hardware features include pre- and post-triggering, overvoltage protection, programmable gains, and an 8255 digital I/O controller. Software features include assembly-language drivers that are callable from Basic, QuickBasic, Turbo Pascal, Fortran, and C programs. $2995.

Qua Tech Inc, 478 E Exchange St, Akron, OH 44304. Phone (216) 434-3154. TWX 510-101-2726. FAX 216-434-1409.

Circle No 392

Plug-in power for VME!

Here's a fully featured 400-watt, triple-output power system that's configured for *direct connection* to the motherboard in your VME bus system. It's a standard MOSFET switcher that includes all the features you've come to expect from NCR Power Systems.

Switching frequency is 80 kHz, and the unit has protection against overvoltage, overcurrent, and input surges. It meets the stringent safety and EMI requirements established by UL, CSA and TUV (VDE). Packaging complies with the Eurocard standards defined in DIN-41494 and IEC-297 for plug-in attachment to the motherboard. Precise (±0.4%) line and load regulation and 75% efficiency make the unit ideal for data communications and processing applications.

Standard units can be modified by NCR for precise conformance to customer requirements.

For detailed specifications and price quotation, contact NCR Power Systems, 3200 Lake Emma Road, Lake Mary, FL 32746-3393; Telephone 800/327-7612 or in Florida, call 407/323-9250.

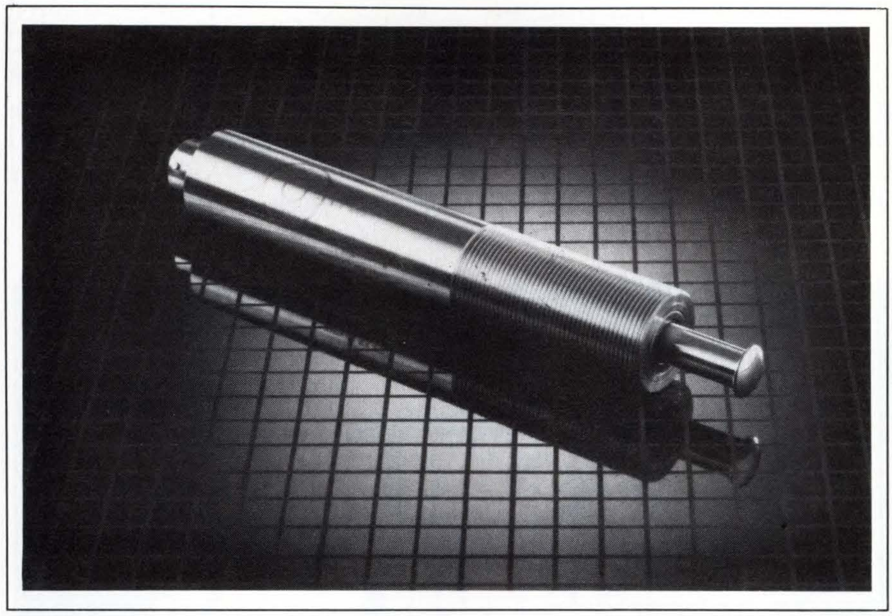
NCR

CIRCLE NO 214

COMPONENTS & POWER SUPPLIES

GAUGE HEADS

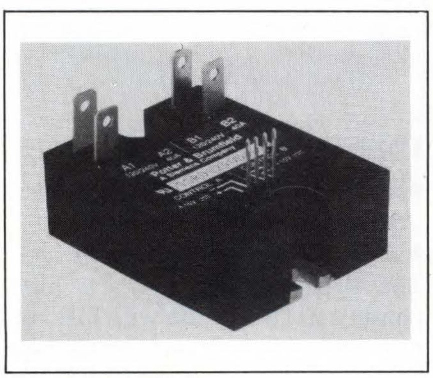
- *Operate efficiently against external pressures of 1000 psi*
- *Protected against dirt, water, and corrosive vapors*



RBB Series gauge heads are built to withstand the abuse of heavy side loads. They operate efficiently against external pressures ranging to 1000 psi. The sensors are protected against dirt, water, and corrosive steam and vapor. The stainless steel construction features a double-shield design that resists external magnetic influences. Probes are hardened to a Rockwell 60 rating and are hard chrome plated and polished for smooth operation. The gauge heads utilize ball bearings to extend life and reduce friction. Probe life is estimated at 8×10^6 cycles with 26-lb side loads. Linearity and repeatability are $\pm25\%$ and 0.000025-in., respectively. The gauge heads are available in ac and dc versions in linear ranges of ±0.25 and ±1 in. From \$616 and \$807 for ac and dc units, respectively.

Schaevitz Engineering, Route 130 & Union Ave, Pennsauken, NJ 08110. Phone (609) 662-8000. FAX 609-662-6281.

Circle No 395



RELAYS

- *Offer two relays in a single standard package*
- *Feature outputs rated for either 40 or 25A each*

SSRD Series solid-state relays provide two totally independent relays in a common hockey-puck package. Versions are available where each of the spst-NO relays have outputs rated for either 40 or 25A. The units use inverse parallel SCRs as output devices and include internal dv/dt snubber networks across the output switches. These 4-to-15V dc input devices are available in both zero-voltage and random-voltage turn-on versions. The relays are UL recognized and CSA certified and feature optical coupling, which provides 2500V rms input-to-output isolation. \$30 (100) for a 25A, zero-voltage turn-on version. Delivery, stock to 10 weeks ARO.

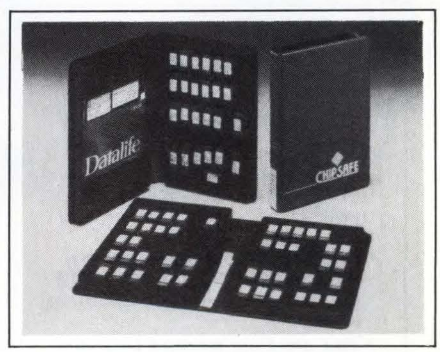
Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2194.

Circle No 396

STORAGE SYSTEM

- *Provides safe keeping for ICs*
- *Snap-closure design prevents accidental opening*

A handsomely bound 7×11-in. album, the ChipSafe is a booksize storage system for the safe keeping of ICs. The ribbed structure and interlock design of the thermoformed inner compartments ensure crushproof and dust-tight storage. The snap-fastening closure design pre-



vents damage due to accidental opening. The album can store any size IC in any orientation. Components are protected from electrostatic discharge damage and held firmly in place by the gripping strength of a conductive, noncorrosive foam, which is abrasion and solvent resistant. Each album comes with a supply of color-coded binder labels and self-adhesive IC labels. \$16.95.

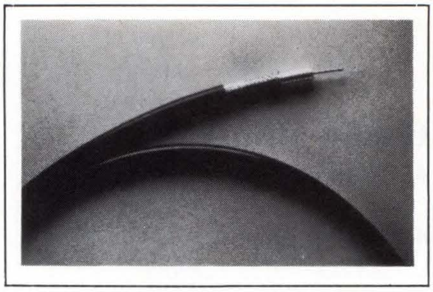
iToi Enterprises, Box 59, Newton Highlands, MA 02161. Phone (617) 332-1010.

Circle No 397

NETWORK CABLES

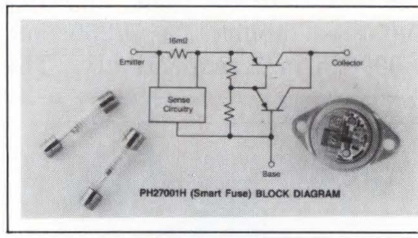
- *Designed for manufacturing-automated-protocol networks*
- *Available with copper-covered-steel center conductors*

The 1223A and 1224A 75Ω coaxial cables are designed for manufacturing-automated-protocol (MAP) networks. Both meet IEEE MAP requirements and are CL2X rated. Designed for drop applications from the cable trunk to individual workstations, the 1223A cable features an 18 AWG solid copper-covered steel conductor and a black PVC jacket. The 1224A accommodates either trunk-cable or drop-cable applications and features a 14 AWG conductor. Both cables employ a sheild, which consists of a double-layer foil bonded to the dielectric core followed by an aluminum-braid shield and then an overall copolymer mylar foil. The outer foil has a shorting fold, which provides metal-to-metal contact for maximum shield effectiveness. Both cables are available in 1000-ft put-ups. \$220.65 and \$377.25 for the 1223A and 1224A, respectively.



Belden Wire and Cable, Box 1980, Richmond, IN 47375. Phone (800) 235-3364.

Circle No 398



PNP DARLINGTON

- *Features internal short-circuit protection*
- *Has a 312W dissipation rating*

The PH27001H is a smart, high-power pnp Darlington with fast current-foldback overload protection. To protect against short-circuit conditions, the unit monitors the current through an internal 16-mΩ sense resistor. Upon detecting an overload condition, the sense circuitry diverts the input base current to shut off and protect the Darlington. Other features include a 312W power dissipation rating, a 1.8V max $V_{CE(SAT)}$, an 80V min collector-to-emitter breakdown, a 1500 min dc current gain, a −55 to +125°C operating range, and a 1.2-μsec turn-on time. The unit is housed in a TO-3 hermetically sealed package with a 0.4°C/W ther-

NEW MICROLITHIUM™ BATTERY SERIES JOINS THE DURACELL® XL™ POWER FAMILY!

Today Duracell is your best source for all your lithium battery needs.

First with high-power consumer-replaceable lithium batteries, Duracell now introduces the MicroLithium Battery Series for long-life, low-drain applications. These new lithium/manganese dioxide cells have the same quality and dependability as our popular High Power Series, but have been optimized for micropower equipment. UL recognized, they're available in a wide-range of coin and cylindrical sizes, with or without pin terminations.

DL123A – First 3-volt, high-power consumer-replaceable lithium batteries.

Our sales engineers listen to your engineers.

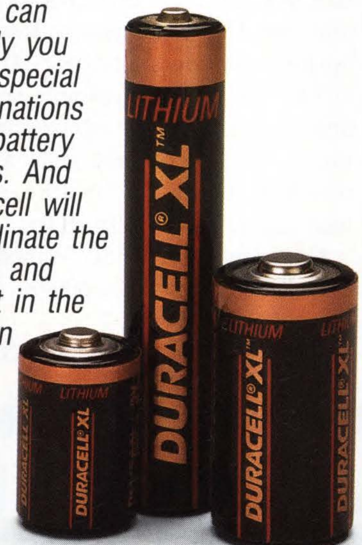
World-wide, you can count on our field sales engineers for

Assorted cell sizes and PCB pin types. Shown are DL2450; DL2032 with chip-straddle pins; DL1/3N.

expert applications assistance, battery samples, and test information, when you need it. From form-fit evaluation to component sourcing, we can help match the optimum lithium cell to your requirements.

Custom assemblies... standard solutions.

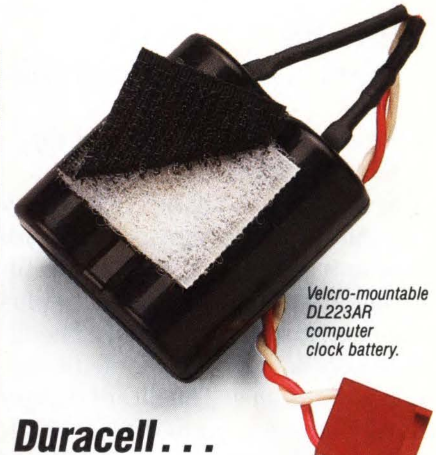
Our national network of Authorized Value-Added Assemblers can supply you with special terminations and battery packs. And Duracell will coordinate the effort and assist in the design work too!



Popular-size cylindrical configurations: DL1/2AAL; DL2NSE; and DL2/3AL.

SPECIAL 10% INTRODUCTORY DISCOUNT!

We want you to try the new DURACELL XL MicroLithium Series of batteries. That's why we're offering a special discount on all new customer orders placed and shipped before June 30, 1989.*



Velcro-mountable DL223AR computer clock battery.

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The Duracell Team is just a phone call away to help you in fulfilling your battery requirements, from technical information to competitive pricing and quick deliveries. With Duracell, satisfying your lithium battery needs is easier than ever!

Call us today at one of the toll-free numbers listed below and lock in your 10% introductory discount.

*Discount applies to cells with and without PCB pins purchased directly from Duracell: DL2450; DL2430; DL2032; DL2025; DL2016; DLAAL; DL2/3AL; DL1/2AAL.

DL2/3AL with single pins (polarized pins available).

DURACELL INC.
OEM Sales and Marketing Group
Berkshire Industrial Park
Bethel, CT 06801

FOR INFORMATION AND TO GET YOUR 10% DISCOUNT CALL:

East	1-800-423-5962	(In Connecticut, 203-264-3935)
Central	1-800-525-8457	(In Illinois, 312-954-2714)
West	1-800-331-3923	(In California, 800-225-1962)

CIRCLE NO 215

mal impedance. Units are available screened to MIL-STD-883. $89 (100).

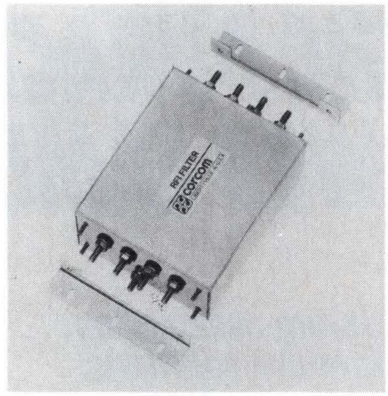
Micro Networks, 324 Clark St, Worcester, MA 01606. Phone (508) 852-5400.

Circle No 399

FILTERS

- *Usable in either 3- or 4-wire systems*
- *Feature both common- and differential-mode suppression*

The A Series 3-phase RFI power-line filters are designed for 4-wire wye applications. They provide filtering in each of the three lines plus the neutral and ground line. The filters also handle 3-phase delta system applications. The filters feature both common- and differential-mode suppression from 50 kHz to 30 MHz. They are effective for both balanced and unbalanced 3-phase loads and incorporate a shielded



construction. The units are manufactured to IEC 380 specifications and are UL recognized. Mounting options include mounting studs at either the line or load side, removable L brackets for surface mounting at the line or load side, and removable endbells for line and/or load sides. $67 to $99 (100).

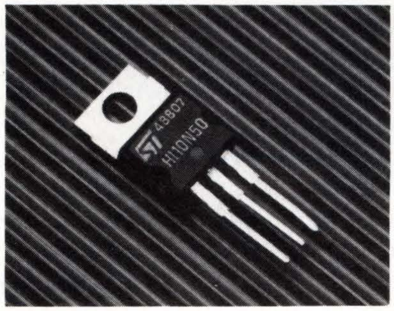
Corcom Inc, 1600 Winchester Rd, Libertyville, IL 60048. Phone (312) 680-7400.

Circle No 400

POWER TRANSISTOR

- *Combines the advantages of MOS and bipolar transistors*
- *Has an output rating of 500V at 10A*

Featuring a maximum drain-source voltage of 500V and a maximum continuous drain current rating of 10A, the STHI10N50 insulated-gate bipolar transistor is suited for use in dc motor drives, solenoid drivers, relay drivers, and similar applications. Because the device has a high input impedance—its maximum gate-current specification is 100 nA—you can drive it in a similar way to a power MOSFET. However, the device's output characteristics are similar to those of a bipolar junction transistor. Its large reverse-bias safe operating area suits the transistor to applications such as switch-mode control of dc motors that are powered directly from a 220V ac line supply. In such applications, you can switch the de-



vice at frequencies as high as 10 kHz. Other features of the device include 100W maximum power dissipation, the ability to operate at a junction temperature as high as 150°C, and typical rise and fall times of 0.7 and 1.1 μsec, respectively. The STHI10N50 is available in a TO-220 or a fully isolated ISOWATT-220 package. $2.16 (100).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 401

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 402

POWER SUPPLY

- *Delivers 1000W from as many as five outputs*
- *Meet UL, CSA, and VDE requirements*

These power supplies provide as many as five outputs and deliver 1000W at 50°C. The main channel delivers 825W at 165A; the four auxiliary channels output as much as 350W combined. Auxiliary channels 1 and 2 deliver 20A max, and auxiliary outputs 3 and 4 deliver 10 and 3A, respectively. The supplies operate from inputs of 90 to 132 or 180 to 264V ac. Line and load regulation are 0.2%, and the minimum hold-up time is 30 msec. Standard features include overload and overvoltage protection, thermal and reverse-voltage protection, remote sensing, and ±10% output voltage adjustment. Standard interface signals include power-fail detection, current sharing, dc okay, overvoltage protection activated, remote inhibit, and remote margining. The units meet UL, CSA, and VDE requirements. $806 to $961 (50). Delivery, eight to ten weeks ARO.

Jeta Power Systems Inc, 2675 Junipero Ave, Signal Hill, CA 90806. Phone (818) 363-9655.

Circle No 403

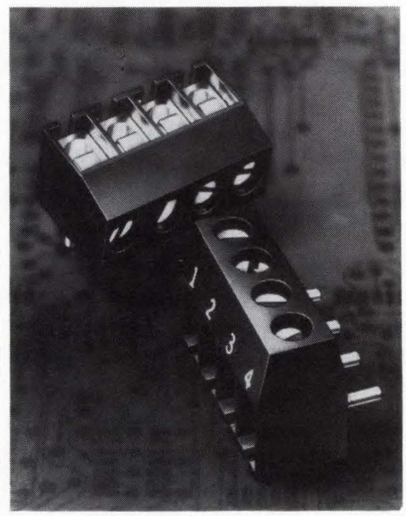
PROXIMITY SWITCH

- *Features a 15-mm sensing distance*
- *Available in 2- and 3-wire versions*

KIE Series capacitive proximity switches sense metallic and nonmetallic objects at distances ranging to 15 mm. The units are housed in a threaded tubular package, which features an integral terminal chamber and can be mounted in either straight-on or right-angle configurations. The switches are available in a 2-wire ac/dc version and a 3-wire dc version with either positive or negative switching models. All models can be programmed in the field for either normally open or normally closed operation. The outputs of all dc versions include short-circuit and overload protection. $87 and $103 for 3-and 2-wire versions, respectively.

Efector Inc, 805 Springdale Dr, Whiteland Business Park, Exton, PA 19341. Phone (800) 441-8246; in PA, (215) 524-2000.

Circle No 404



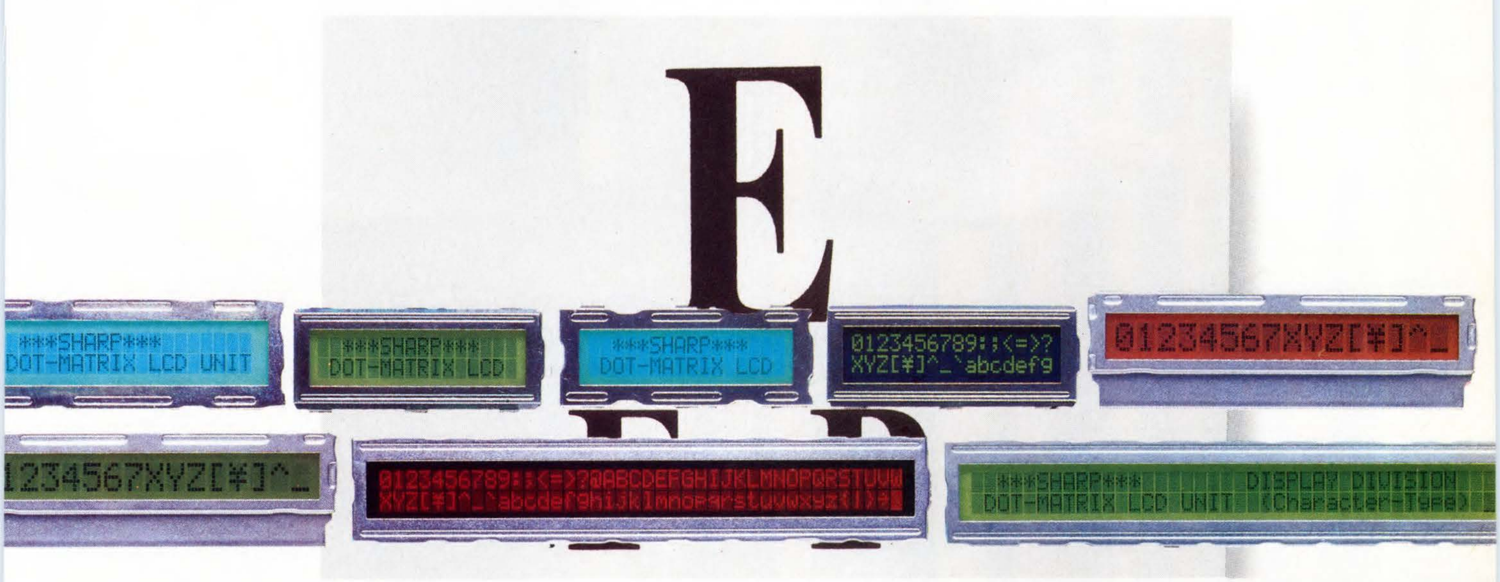
TERMINAL STRIPS

- *Provide easy access for wiring on crowded pc boards*
- *Feature a 94V-0 UL rating*

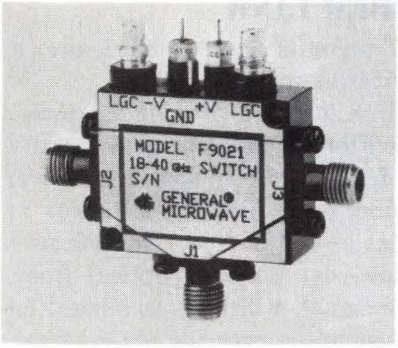
Featuring a 90° entry, Eurostyle terminal strips save space and provide easy, safe access for wiring on crowded pc boards. The 0.197-in. contact spacing provides five terminations in less than an inch. The strips have touch-proof terminals and wire-ready captive screws that won't fall out and cause shorts. The terminals have UL ratings of 15A and 300V max. Other features include wire entries that accept wires as large as 14 AWG, a closed side that acts as a wire stop, and thermoplastic insulator material that has a UL flame-retardant rating of 94V-0 and a UL temperature index of 130°C. $0.17 (500).

Vernitron Corp, Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. TWX 710-364-1843. FAX 603-524-1627.

Circle No 405



CIRCLE NO 216



PIN DIODE SWITCHES

- *Cover frequencies to 40 GHz*
- *Feature a 20-nsec max switching time*

F90 spst and spdt PIN-diode switches cover an 18- to 40-GHz frequency range. The spst switches are available with or without integrated TTL drivers in three different isolation grades. Models F9012, F9013, and F9014 have isolations of 30, 50, and 70 dB min, respectively. Insertion loss ranges from 2 to 3.5 dB max, and VSWR in the on position is 2.2 max. The spdt switches are available with integral TTL drivers in two versions: the F9021 with 30-dB min isolation and the F9023 with 60-dB min isolation. Insertion loss for these two switches ranges from 2.7 to 4.5 dB. For all five switches, rise and fall times are 10 nsec max, and the total switching time is less than 20 nsec. From $850 for spst units; from $1500 for spdt devices.

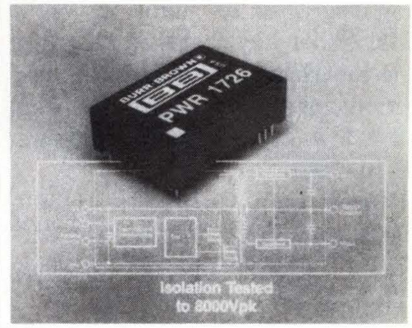
General Microwave Corp, 5500 New Horizons Blvd, Amityville, NY 11701. Phone (516) 226-8900.

Circle No 406

DC/DC CONVERTER

- *Features high isolation and low barrier capacitance*
- *Has a maximum leakage current of 2 μA*

The PWR1726 1.5W dc/dc converter is designed for applications where high isolation and low barrier



capacitance are critical for system integrity. The single-channel, dual 15V-output unregulated device features a minimum isolation voltage of 3500V dc (units are tested at 800V pk for 60 sec at 60 Hz) and a typical barrier capacitance of 7 pF. The maximum leakage current is 2 μA. The converter operates over a 7 to 18V dc input range. You can synchronize the converter to eliminate unwanted beat-frequency noise generated by multiple units in the same system. By interconnecting device sync pins, you can

CIRCLE NO 36

gang together as many as eight units. Other key features include a logic-controlled remote on/off connection; input and output filtering; and a low-profile, 0.4-in. package. $22.10 (100).

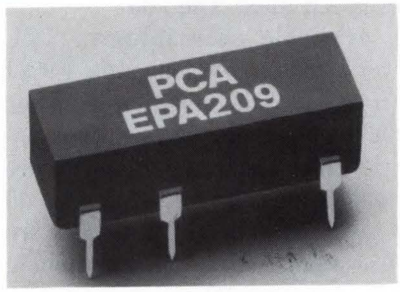
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 407

OSCILLATORS

- *Have outputs that range to 100 MHz*
- *Feature a ±5% tolerance*

The members of the EPA209 family of oscillators are housed in 14-pin DIPs and generate fixed-frequency square wave outputs. The 18 units in the line provide fixed frequencies of 2, 3, 4, and 5 MHz; then every 5 MHz from 10 to 50 MHz; and every 10 MHz from 60 to 100 MHz. Standard features include a 50% duty cycle, ±5% tolerance, complementary Schottky TTL outputs, a 4-nsec rise time, and an Enable line for synchronization service. The units' low-level output can drive 10 TTL loads, and the high-level output can drive 20 TTL loads. Maximum supply current measures 75 mA, and the operating range spans 0 to 70°C. $1.70 (1000) for a 5-MHz unit. Delivery, stock to six weeks ARO.



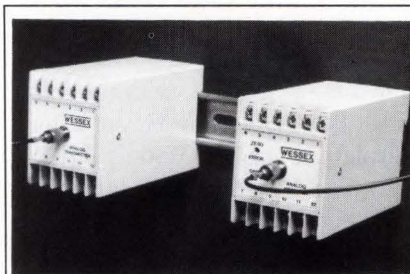
PCA Electronics Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761.

Circle No 408

FIBER LINK

- *Transmits analog signals over a fiber-optic cable*
- *Monitors link for signal failure*

The Fibre-Link-2 transfers 0 to 10V or 4- to 20-mA analog signals over a fiber-optic link for distances as great as 150 meters. The link uses a low-cost polymer optical fiber. The signal, which is modulated for transmission over the optical fiber, is continuously monitored for transmission failures. If a failure occurs, the receiver activates an alarm relay and reduces its output to 0V. The receiver also has a zero-error



adjustment. Both the transmitter and receiver modules are mounted in DIN-standard, rail-mounting packages with screw terminals. £200 for a transmitter/receiver pair.

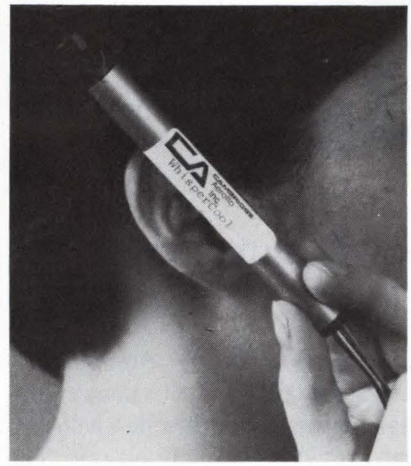
Wessex Machine Controls Ltd, The Gallery, Brookside, Sandhurst, Camberley, Surrey GU17 8AP, UK. Phone (0344) 761613. TLX 858893.

Circle No 409

SPEED CONTROLS

- *Feature a closed-loop controller*
- *Respond in under 3 seconds*

The Whispercool controller regulates fans and blowers to eliminate the excessive noise generated when these systems are running at full speed or cycling excessively. The controller senses the actual demand on the cooling systems and compensates for temperature, altitude, humidity, and air-flow reversal. The Whispercool features a closed-loop controller, which can be set to specific parameters, and an air flow switch that responds to any change, beyond a failure, in under 3 seconds. The unit operates on a supply voltage of 11.4 to 26V dc and consumes only 0.8W. From $21.



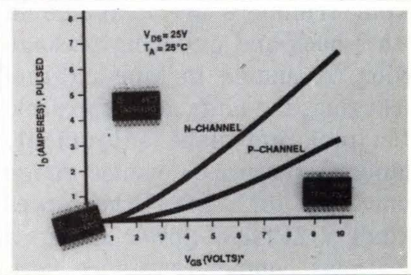
Cambridge Aeroflo Inc, 900 Mount Laurel Circle, Shirley, MA 01464. Phone (508) 425-2346.

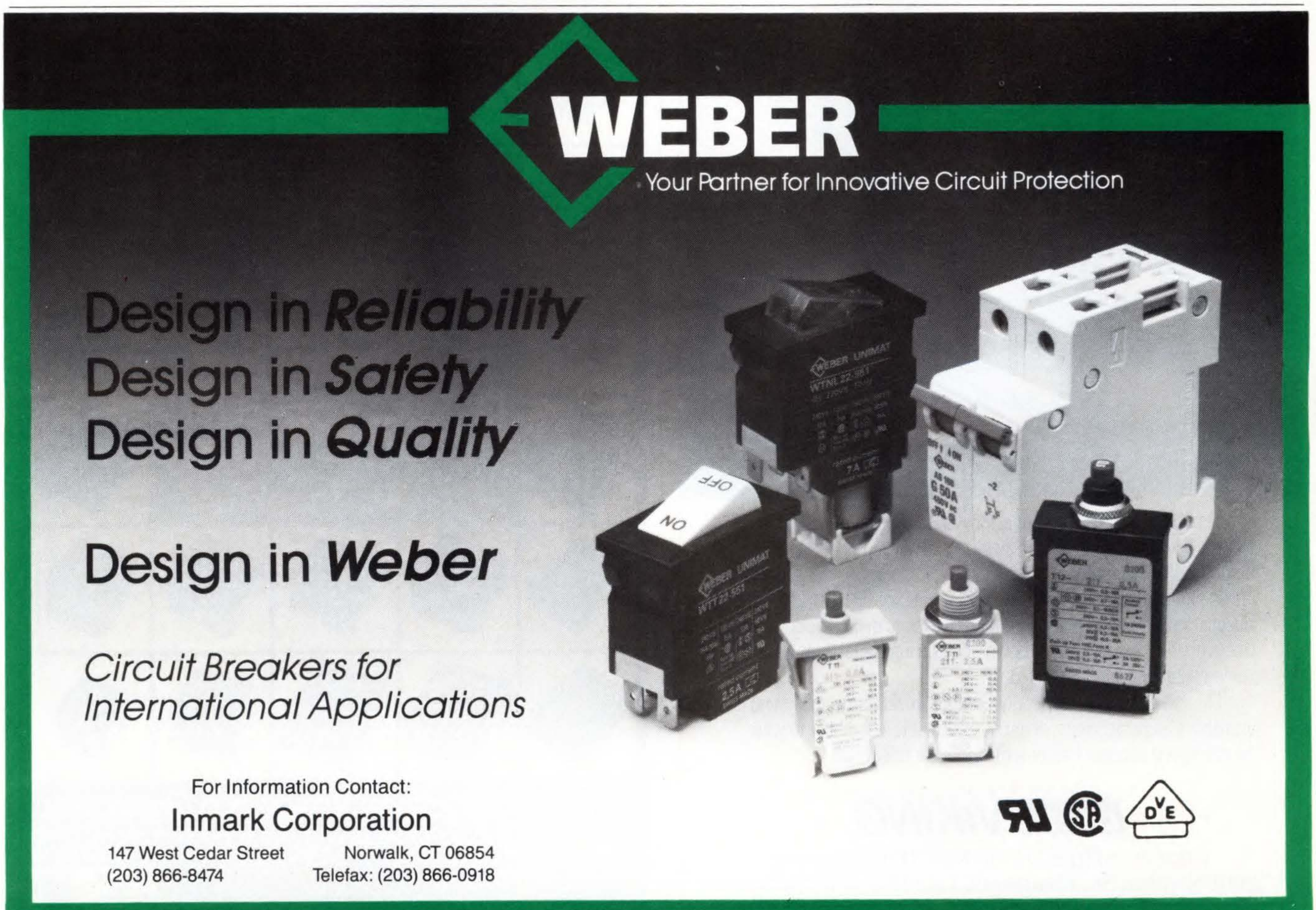
Circle No 410

MOSFET ARRAYS

- *Offer four completely independent MOSFETs*
- *Offered in P-, N-, and complementary N-/P-channel versions*

Available in 20-pin surface-mount plastic packages, these arrays feature four independent MOSFETs. The N-channel (TN0604WG) and the P-channel (TP0604WG) devices have a BV_{DSS} of 40V and an RDS_{on} of 0.75Ω each and 2Ω each, respectively. The 2 N-channel and the 2 P-channel devices in the TC0604WG have identical respective specifications. The N-channel and P-channel MOSFETs have





CIRCLE NO 39

threshold voltages of 1.6 and 2.4V, respectively, with guaranteed RDS_{on} performance at gate drives of 5 and 10V, respectively. $3.89 to $5.08 (100). Delivery, four to six weeks ARO.

Supertex Inc, Box 3607, Sunnyvale, CA 94088. Phone (408) 744-0100. TLX 6839143. FAX 408-734-5247.

Circle No 411

TRIMMERS

- *Designed for surface mounting*
- *Operate from −55 to +125°C*

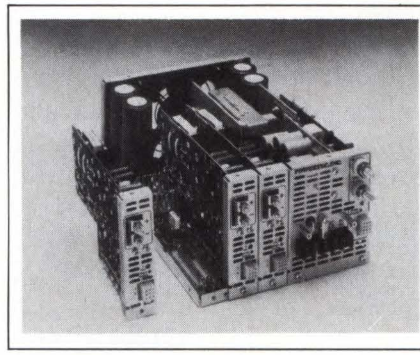
Model 23 4-mm, sealed, surface-mount trimmers are available in both J-hook and gull-wing package styles. Available in tape-and-reel packaging, the units are compatible with pick-and-place equipment. Standard resistance values range from 100Ω to 1 MΩ. Other specs include a 250-mW power rating, a 0.2% max contact resistance variation, and a −55 to +125°C operating range. $0.97 (1000).

Beckman Industrial Corp, 4141 Palm St, Fullerton, CA 92635. Phone (714) 447-2510.

Circle No 412

POWER SUPPLIES

- *Have power ratings that range to 1000W*
- *Feature four-output capability*



Series 6A, 6B, and 6C power supplies feature a mainframe enclosure that provides the main output. The mainframe accommodates and powers as many as three auxiliary modules with 2 to 48V outputs; the overall power ratings are 600W for the 6A series, 800W for the 6B series, and 1000W for the 6C series. Main output values range from 2 to 24V; a 5V main output supplies currents of 90 to 150A. You can connect outputs with identical voltages in parallel, regardless of current ratings. When so configured, outputs automatically current-share in proportion to their current ratings. Standard features include overvoltage protection, remote sense, automatic thermal shutdown, soft start, an EMI filter, and reverse-voltage protection. From $939 to $1079 for models with four outputs. Delivery, stock to eight weeks ARO.

Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. TLX 277483. FAX 818-998-4225.

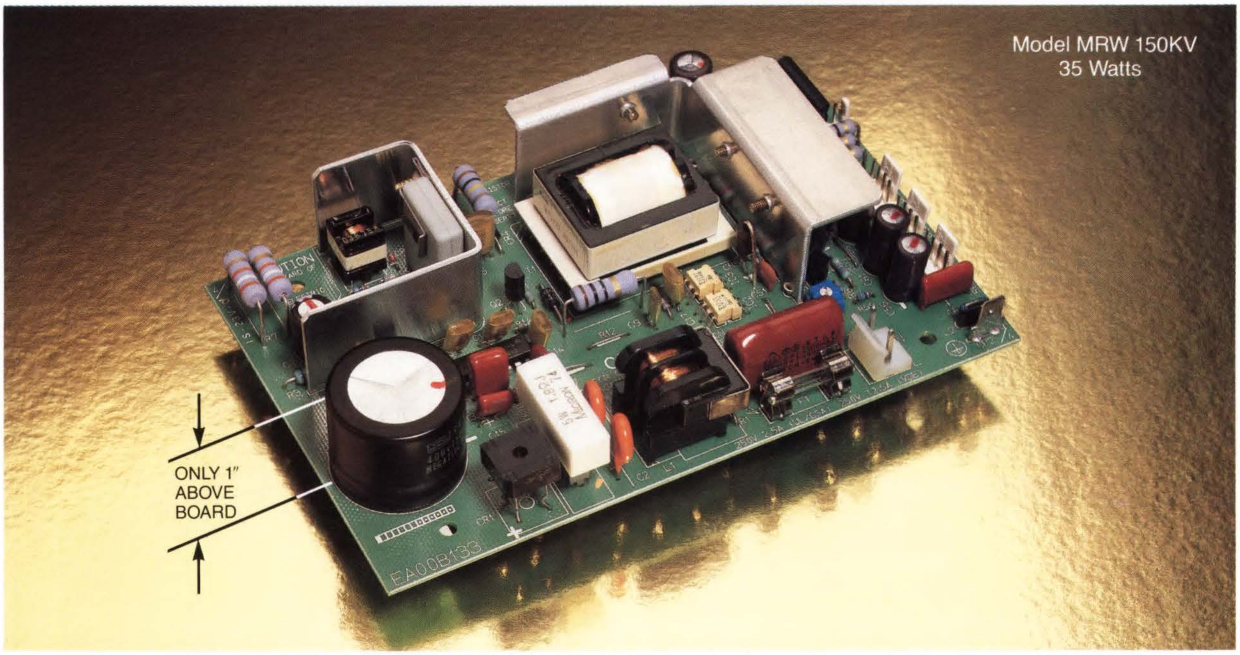
Circle No 413

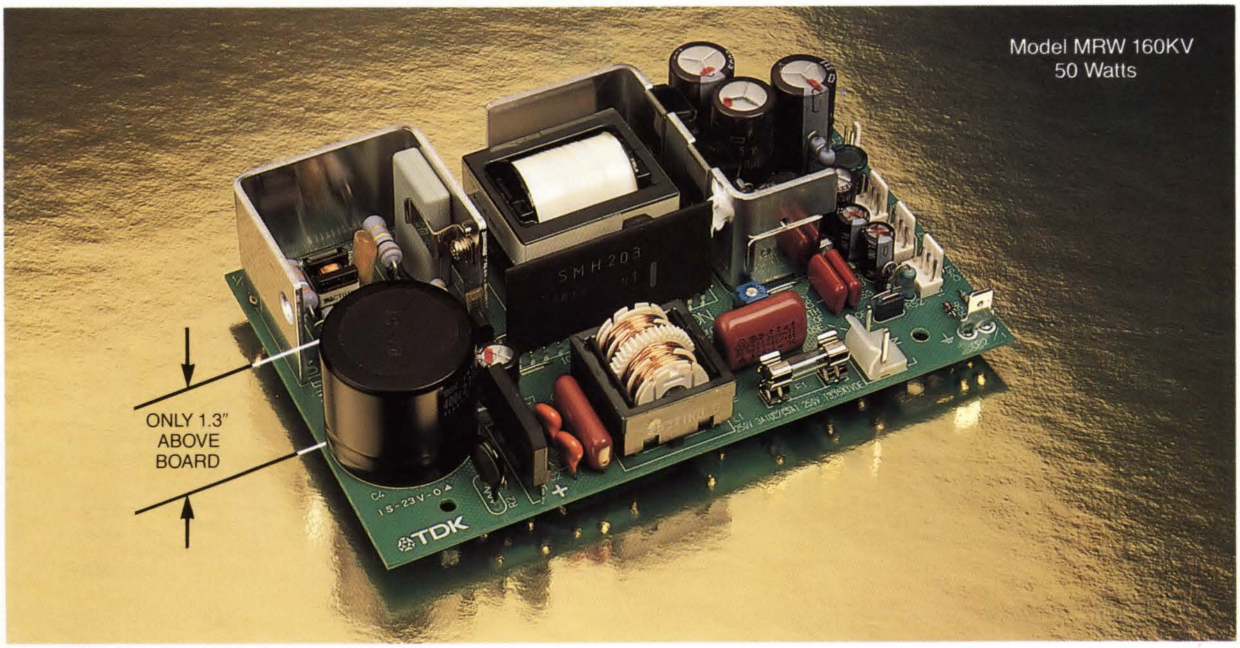
146-1630

KEPCO
THE POWER SUPPLIER™

KEPCO/TDK TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES

SERIES MRW/35 AND 50 WATTS





- **Current trade-off:** Current may be increased from one of the outputs at the expense of the others, within the limits defined by Figure 1.
- **Adjustable voltage:** Internal trimmer accessible through the case allows manual adjustment of the voltage setting.
- **Overvoltage protection for principal output** shuts down all outputs if output voltage is forced beyond the set limit.
- **Holding time:** Output is sustained by internally stored energy for 30 milliseconds typically, 20 milliseconds minimum.
- **Built-in EMI filter** attenuates conducted noise below the requirements of FCC 20780 for Class B computing devices.
- **Safety:** All models recognized by UL, certified by CSA, and approved by TÜV Rheinland to meet VDE 0806/IEC 380.

MRW INPUT CHARACTERISTICS

SPECIFICATION	MRW 150KV	MRW 160KV	CONDITION
Voltage range	95 to 264V a-c; 135 to 370V d-c		
Brownout voltage	85V a-c; 120V d-c		Maximum load
Current	1.0A	1.3A	Typ load, 115V a-c
	0.5A	0.9A	Typ load, 230V a-c
Fuse value	2.5A	3A	
Initial, turn-on surge, first 1/2-cycle.	50A max		115V a-c, rated load 25°C cold start
Frequency	50/60Hz nominal; range 47-440Hz(1)		Single Phase
EMI	Meets the conducted noise standard of FCC 20780, Class B and VDE 0871, Class B		
Leakage current	0.5mA		115V a-c (UL method) 25°C
	0.75mA		230V a-c (VDE method) 25°C
Startup time	400msec (typ)	500msec (max)	Std.(2)
Holdup time	20ms		Std.(2)
Circuit type	Flyback		
Switching frequency	~100KHz	80KHz typ	Operating

(1) At 440Hz the leakage current exceeds the UL/VDE safety specification limit.
(2) Std conditions = nominal input, nominal load, 25°C

MRW OUTPUT CHARACTERISTICS

SPECIFICATION	MRW 150KV			MRW 160KV			CONDITION
	OUTPUT #1	OUTPUT #2	OUTPUT #3	OUTPUT #1	OUTPUT #2	OUTPUT #3	
Source effect	1% max	1% max	1% max	2% max	2% max	1% max	95-132V a-c or 190-264V a-c
Load effect	3% max	5% max	1% max	4% max	2% max	1% max	Minimum load to rated load
Temperature effect	2% max	2% max	1% max	2% max	2% max	1% max	Nominal input, rated load, 0-50°C
Combined effect (source, load, & temperature)	+4%-2% max	+4%-6% max	±6% max	±4% max	±5% max	±6% max	Initial setting 5.00V ±20 mV
Time effect (drift)	0.5% max						0.5-8.5 hr; nom input, rated load, 25°C
Cross effect Output #1	—	4.0% max	0.5% max	—	4.0% max	1.0% max	Load change from minimum to typical, nominal input 25°C
Output #2	1.5% max	—	0.5% max	1.5% max	—	1.0% max	
Output #3	0.5% max	0.5% max	—	0.5% max	0.5% max	—	
Recovery characteristics: Excursion	<4.0%						Step load change from 50% to 100% of rated load. Nominal input, 25°C
Recovery (within ±1%)	<2msec						

KEPCO
THE POWER SUPPLIER™

KEPCO, INC. • 131-38 SANFORD AVENUE • FLUSHING, NY 11352 USA • (718) 461-7000 • TWX #710-582-2631 • FAX: (718) 767-1102

TEAR ON DOTTED LINE TO REMOVE AND SAVE.

MRW MODEL TABLE

SPECIFICATION	OUTPUT VOLTAGE		OVP SETTING	OUTPUT CURRENT	CURRENT LIMIT	OUTPUT POWER				RIPPLE SOURCE	RIPPLE SWITCHING	NOISE (SPIKE)	EFFICIENCY
Units	Volts		Volts	Amps		Watts				mV		mV	Percent
Condition	Factory set[1]	Adjustment range	Nominal Input, 25°C	50°C (See Fig. 1)	Nominal input	40°C	50°C	60°C	71°C	Nominal input, typ load p-p max		d-c to 20MHz p-p max	Nom input, rated load typ
MRW 150KV (35 WATTS)													
Output #1	+ 5	4.75-5.25	5.8-6.9[2]	1.0-2.2 (typ) (4.0 max)	Total maximum output power no more than 38.5 Watts	35.0	35.0	24.5	14.0	30	50	150	70%
Output #2	+ 12	—	—	0.6-1.8 (typ) (2.5 max)						30	50	290	
Output #3	− 12	—	—	0-0.1 (typ) 0.3 (max)						10	20	290	
MRW 160KV (50 WATTS)													
Output #1	+ 5	4.75-5.25	5.8-6.9[2]	1.0-5.0 (typ) (6.0 max)	Total maximum output power no more than 60 Watts	50	50	35	20	30	50	150	72%
Output #2	+ 12	—	—	0.6-2.0 (typ) (2.5 max)						30	50	290	
Output #3	− 12	—	—	0-0.1 (typ) (0.5 max)						10	20	290	

(1) Nominal input, maximum load, 25°C (2) All outputs are shut down when OVP is activated

KEPCO/TDK TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES

SERIES MRW

These are the first models of a new series of switchers which employ advanced input and output capacitors and magnetics to achieve a very slim profile. In Model MRW 150KV (35 Watts) the overall thickness is 30mm and component length is only 1″ (25.4mm) above the PC card. Both models are built on the same card footprint (100 x 160mm), and with the same plug pattern as our popular MRM 144KV, to allow users for whom low profile and/or a wide input range will be significant, to easily upgrade.

FEATURES:

- **115/230V a-c operation without user intervention:** Special flyback circuit accepts any input voltage from 95V to 264V a-c.
- **Power-OK logic (TTL compatible) signal** may be used as *power fail* signal. Logic "1" is given when +5 output is above 4.5V.

MRW GENERAL SPECIFICATIONS

SPECIFICATION		RATING/DESCRIPTION	CONDITION
Temperature		0-71°C (see model table)	Operating
		−40 to 85°C	Storage
Humidity		95% RH	Non-condensing; operating & storage
Shock		20g, 3 axes (11msec ±5msec pulse duration)	Non-operating 3 shocks each axis
Vibration		5-10Hz: 10mm amplitude	Non-operating 1 hour each axis
		10-55Hz: 2g, 3 axes	
Isolation	Output to case	500V d-c, 100MΩ	25°C, 65% RH
Withstand voltage	Input to output	3.75KV a-c for 1 minute	25°C, 65% RH Y capacitor removed
	Input to case	2KV a-c for 1 minute	25°C, 65% RH
Safety		UL 478 recognized, CSA C22.2 certified. VDE 0806/IEC 380 approved by TÜV Rheinland	
Type of construction		PC card	
Enclosure		Optional metal	
Cooling		Convection	

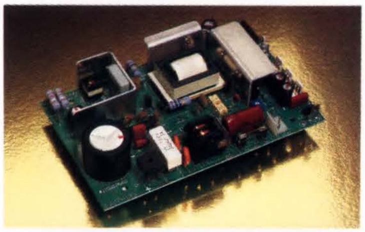
UL RECOGNIZED CSA CERTIFIED TÜV APPROVED

This KEPCO product is backed by a firm 1-YEAR WARRANTY

Data subject to change without notice.

KEPCO/TDK TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES

SERIES MRW



DIMENSIONS

MRW 150KV:
inches — 1.12 x 3.93 x 6.3
mm — 28.5 x 100 x 160

MRW 160KV:
inches — 1.5 x 3.93 x 6.3
mm — 38 x 100 x 160

NET WEIGHT

MRW 150KV: 12.35 oz, 350 gm
MRW 160KV: 17.65 oz, 500 gm

OPTIONAL STEEL ENCLOSURES:
For MRW 150KV: CA 19
For MRW 160KV: CA 20

INPUT-OUTPUT CABLE KITS:
For MRW 150KV — 219-0184
For MRW 160KV — 219-0184

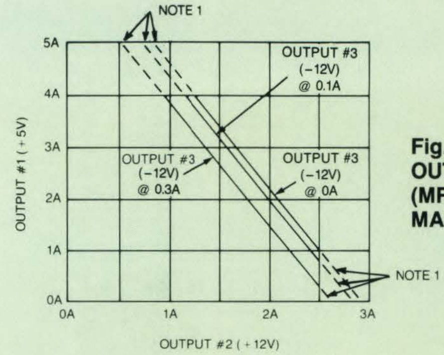
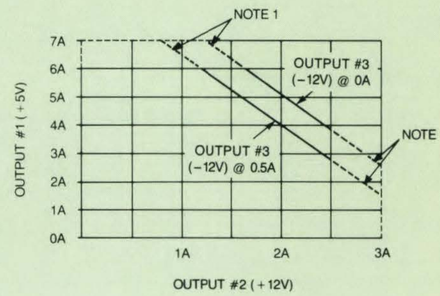


Fig. 1
OUTPUT RATINGS
(MRW 150KV)
MAX POWER: 38.5W

FIG. 1
OUTPUT RATINGS
(MRW 160KV)
MAX POWER: 60W



NOTE 1:
Forced air 20 CMF
at 1 atmosphere.

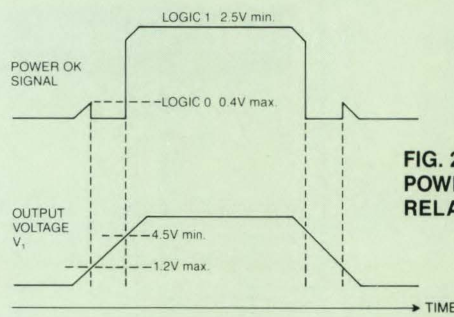
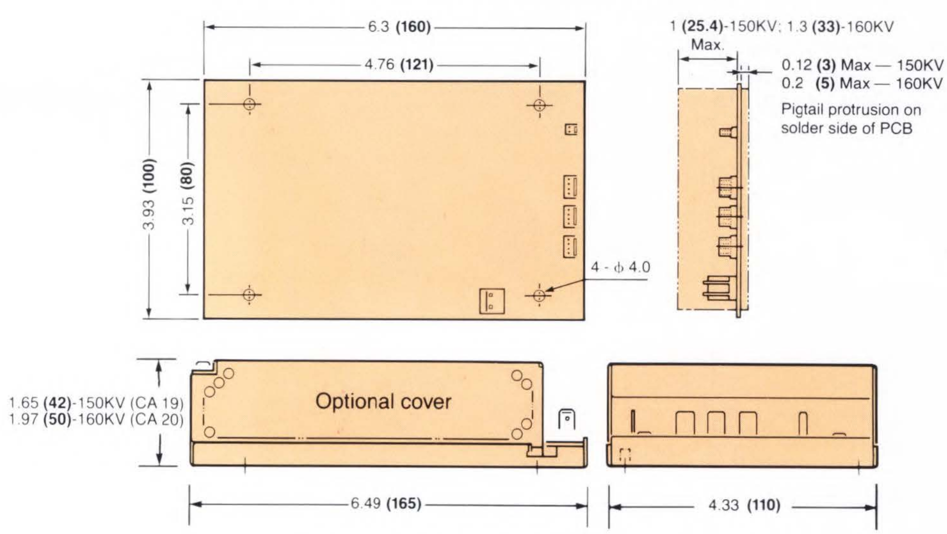


FIG. 2
POWER OK SIGNAL
RELATED TO OUTPUT

KEPCO® THE POWER SUPPLIER™

OUTLINE DIMENSIONAL DRAWINGS

Dimensions in light face type are in inches, **dimensions in bold face type are in millimeters.**



Mounting: 0.16″ (4.0 mm) diameter holes — (4) bottom.

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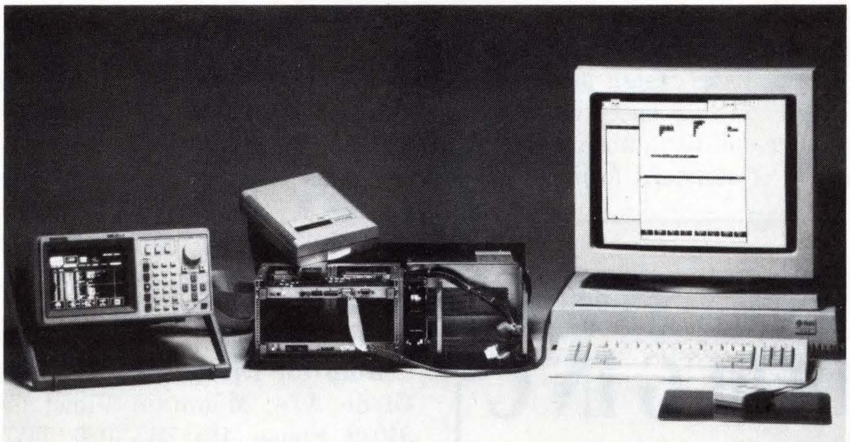


C DEBUGGING SYSTEM

- *Works with a logic analyzer to provide hardware breakpoints*
- *Lets you develop C software for any 68000 μP*

TekDB combines a source-level C debugger and a debug monitor in one EEPROM that you can plug into any prototype that is based on a μP of the 68000 family, including the 68030. The package lets you download your program into the target system, control the program's execution, and debug the program at the C source-code level. If you combine the debug package with the vendor's 1241 logic analyzer, you can set hardware breakpoints and the package can then perform real-time tracing. You can adapt the package to almost any prototype that contains an RS-232C serial port. The package is intended for use with the vendor's CLANDS II ANSI C development system, which has been enhanced to generate code for the 68030 μP and includes a code-coverage analyzer that reports execution statistics for the program under test. It also reports on code that never gets executed. TekDB debug package, $2500 to $7000, depending on host configuration; CLANDS II, $3850 to $11,000; 1241 Logic Analyzer, $10,950.

Tektronix Inc, Logic Analyzer Div, Box 12132, Portland, OR 97212. Phone (800) 245-2036.

Circle No 415

GRAPHICS TOOL

- *Lets you write programs for a graphics processor*
- *Implements the features of the ANSI C standard*

The DP8500 C compiler lets you write high-level code for the vendor's DP8500 raster-graphics processor. The compiler implements all the features of the proposed ANSI standard; however, a command-line switch allows you to compile programs that are written in traditional K&R C. This feature allows you to use existing C programs with the DP8500 graphics processor. The output of the compiler is macro-assembler source code; you'll need the vendor's raster-graphics assembler package to convert the compiler output to executable code. The compiler runs on MS-DOS and Unix systems. MS-DOS version, $1000; Unix version, $5000; raster-graphics assembler package, $700.

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-4425. TLX 346353. TXW 910-339-9240.

Circle No 416

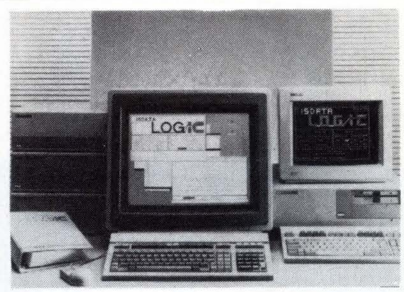
DATA-ACQ SOFTWARE

- *Allows a Macintosh to emulate an oscilloscope*
- *Lets you create many virtual laboratory instruments*

MacInstruments is a software package that works with the vendor's McADIOS II data-acquisition hardware and allows a Macintosh II or SE computer to emulate oscilloscopes, chart recorders, scrolling-strip recorders, and scan-line recorders.

GW Instruments Inc, 35 Medford St, Somerville, MA 02143. Phone (617) 625-4096. TLX 940103. FAX 617-625-1322.

Circle No 417



ASIC DESIGN TOOL

- *Allows manufacturer independent PLD design*
- *Provides facilities to transfer PLD designs to gate arrays*

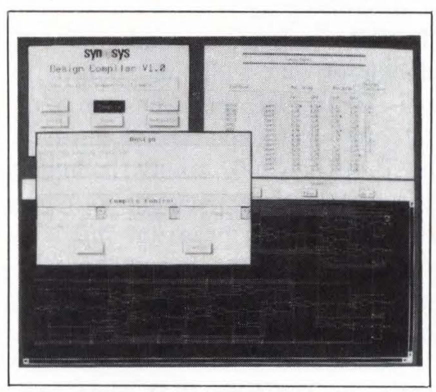
The LOG/iC CAE package allows you to transfer a PLD design from one manufacturer's device to another, or to convert it for implementation as a gate array. The package's PLD compiler allows you to specify a PLD design without requiring detailed manufacturer-specific device information. A schematic capture facility also allows you to use circuit diagrams generated by the OrCAD CAE package as input to the PLD compiler. In conjunction with the package's PLD database, the compiler then allows you to select suitable devices with which to implement your design and generates the required PLD data. The library includes technical data for more than 1000 PLDs from 36 PLD vendors. After specifying a design, the package's functional verifier allows you to simulate the logic to determine parametric information such as propagation delays. You can also use the functional verifier to generate test vectors using a high-level language or sections of the verifier's trace buffer. If you wish to integrate one or more PLD designs into a gate array, you can use the LOG/iC Gates software. This software allows you to optimize the logic design and, in conjunction with a postprocessor, to generate net-list information in a variety of standard formats. LOG/iC runs on DEC VAX and MicroVAX computers; Apollo and HP-9000 workstations; and on the IBM PC/XT, PC/AT, and PS/2 or compatible computers. IBM PC versions: PLD compiler, DM 4885; PLD database, DM 980; logic verifier, DM 1980; gate-array package, DM 5480; postprocessors, DM 870.

Isdata GmbH, Haid-und-Neu-Strasse 7, 7500 Karlsruhe 1, West Germany. Phone (0721) 693092. TLX (17) 721170. FAX (0721) 174263.

Circle No 418

Kontron Electronics Inc, 630 Clyde Ave, Mountain View, CA 94039. Phone (415) 965-7020. TWX 910-378-5207. FAX (415) 965-3505.

Circle No 419



LOGIC SYNTHESIS

- *Converts HDL specification into a simulatable net list*
- *Optimizes circuits for speed and area*

The HDL Compiler, which is written in C and runs under Unix, synthesizes gate-level net lists from Hardware Description Language (HDL) design specifications. A companion tool, called the Design Compiler, optimizes net lists for speed and area; it allows you to evaluate performance/area tradeoffs so that you can optimize the circuit for your particular application. Comprehensive documentation includes the Verilog Synthesis Policy, which describes how to define Verilog HDL descriptions that are suitable for

translation and optimization. The HDL Compiler and the Design Compiler can also operate on Register Transfer Level (RTL) design descriptions; the software can analyze and evaluate setup and hold times of storage elements. You can examine such constraints as minimum delay, minimum rise delay, clock skew, loading, temperature, voltage, and process, and compensate for their effects. You can maintain your hierarchical design, and you have the flexibility to limit the scope of the optimization. The tools run on Sun 3/4/386i and Apollo DN3000/4000 workstations. Prices start at $35,000 for the HDL Compiler and $17,500 for the Design Compiler. The Verilog Synthesis Policy is included in the documentation for the HDL Compiler.

Synopsis Inc, 1500 Salado Ave, Mountain View, CA 94043. Phone (415) 962-5000.

Circle No 420

TMS320 ASSEMBLER

- *Provides macro facilities*
- *Generates absolute-address code*

The ASM-320 is a macroassembler that runs on an IBM PC or compatible and generates code for TI's TMS32020 and TMS320C25 digital signal processors. The instruction mnemonics conform to those used by TI, but the pseudo-operations and assembler directives differ. The assembler generates hex files that are suitable for uploading to the vendor's DSP-16 data-acquisition or DSP-C25 signal-processing boards by means of a utility that is included in the package. The package also includes utilities that convert these files to TI-compatible tagged format for downloading to a target system or to binary files that many EPROM programmers can accept. The assembler generates absolute addresses, so you don't need a linker. Command-line switches let you direct the assembly listing and/or the symbol cross-reference table to the screen, to a file, or to a printer. Other switches let you suppress code generation or the listing of source code, so that assembly will proceed faster and the listing file will contain only error messages. $49.95.

Ariel Corp, 110 Greene St, New York, NY 10012. Phone (212) 925-4155. TLX 4997279. FAX 212-966-3981.

Circle No 421

DATA-STREAMING TOOL

- *Can transfer data between disk and any I/O device*
- *Achieves transfer rates of 190k bytes/sec or more*

DATASTREAM is a software package that runs under DOS 3.0 or higher, on IBM PCs and compatibles, and on the PS/2 Model 30. It works in conjunction with language interface software for Turbo

Pascal, C, and the vendor's implementation of Basic, as well as with the vendor's high-performance DMA board. Using DMA techniques, the program transfers data in either direction between the hard-disk drive and any other I/O device. On an 8-MHz PC/AT you can achieve transfer rates as high as 190k bytes/sec; higher transfer rates are possible when the storage device is a RAM-disk. Typical applications are event analysis and environmental monitoring; you can also use the software for high-speed retrieval of data from the disk in waveform-generation and -analysis and simulation applications. Separate versions are avilable for Basic, C, and Turbo Pascal. $295.

Intelligent I/O, 1141 W Grant Rd, Suite 131, Tucson, AZ 85705. Phone (602) 629-9872. TLX 888225. TWX 910-997-0735. FAX 602-623-8965.

Circle No 422

CASE TOOL FOR MAC

- *Lets you create structured-design charts*
- *Checks the consistency of your data structures and diagrams*

The MacDesigner version 2.0 CASE tool lets you capture and communicate software design and organization with the aid of structure charts, tree diagrams, module descriptions, and a data dictionary. The program automatically checks the consistency of your data structures and diagrams, and generates a verification report. Six types of windows and a complete set of text- and graphics-editing features allow you to create structured-design charts, the data dictionary, and text documents. Other Macintosh application programs can use the graphics and text created with MacDesigner. To run the program, you need a Macintosh, MacPlus, Mac SE, or Mac II computer that has at least 1M byte of RAM. The demonstration software has all the features of the full product except that the document-save function is disabled. $795; demo version with complete manual, $79.

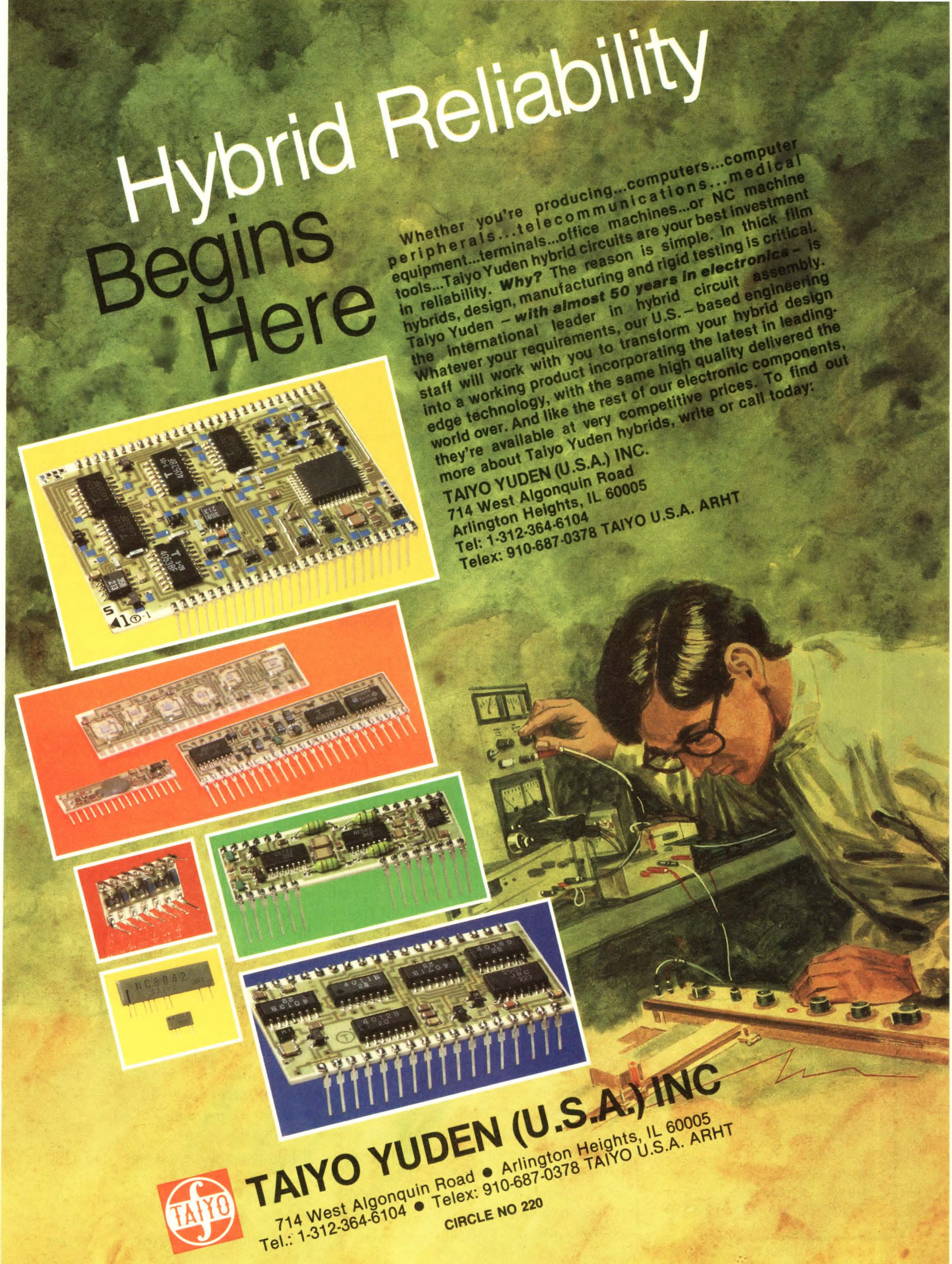
Excel Software, Box 1414, Marshalltown, IA 50158. Phone (515) 752-5359.

Circle No 423

INTRINSIC LIBRARY

- *Contains eight intrinsic functions written in C*
- *New algorithms provide faster execution and better accuracy*

The vendor's library of eight basic intrinsic functions provides C language sin, cos, tan, arctan, exp, log, sqrt, and pow(xY) functions. The routines use a newly developed table-look-up procedure; according to the vendor, the double-precision accuracy is more than 99% over a range of several hundred thousand test cases. Because the procedures


Hybrid Reliability
Begins
Here
Whether you're producing...computers...computer peripherals...telecommunications...medical equipment...terminals...office machines...or NC machine tools...Taiyo Yuden hybrid circuits are your best investment in reliability. Why? The reason is simple. In thick film hybrids, design, manufacturing and rigid testing is critical. Taiyo Yuden – with almost 50 years in electronics – is the international leader in hybrid circuit assembly. Whatever your requirements, our U.S. – based engineering staff will work with you to transform your hybrid design into a working product incorporating the latest in leading-edge technology, with the same high quality delivered the world over. And like the rest of our electronic components, they're available at very competitive prices. To find out more about Taiyo Yuden hybrids, write or call today:
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TAIYO
TAIYO YUDEN (U.S.A.) INC
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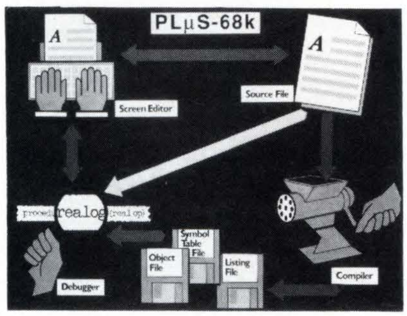
CIRCLE NO 220

greatly reduce the number of operations needed to calculate a result, the routines execute much faster than other currently used algorithms. The functions are based on the IEEE floating-point standard and are portable to all machines that implement this standard. $20,000.

Quantitative Technology Corp, 8700 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 626-3081.

Circle No 424



PROGRAMMING AID

- *Runs under the OS-9 operating system*
- *Lets you create OS-9 device drivers and descriptors*

The PLμS (Programming Language for micro systems), a complete programming package for users of the OS-9/68K operating system, is modeled on Pascal, but includes many of the useful features of C. Variable types include signed and unsigned integers, 32-bit fixed- and floating-point numbers, and in the 68020/68881 version, 84-bit floating-point numbers. The language provides low-level facilities such as direct access to registers and an easy interface to assembly-language programs and operating-system calls. The package includes a screen editor, a compiler, and a source-level debugger. Unlike other high-level languages, the package lets you create OS-9 device drivers and descriptors. PLμS-68K produces code for the 68000, 68008, 68010, and 68020 processors; PLμS-020 adds the capability of creating code for a 68020 with a 68881 math coprocessor. PLμS-68K, £299; PLμS-020, £399.

Windrush Micro Systems Ltd, Worstead Laboratories, N Walsham, Norfolk NR28 9SA, UK. Phone (0692) 404086. TLX 975548.

Circle No 425

C CROSS-COMPILER

- *Lets you develop C programs for 68000 systems on PCs or VAXs*
- *Includes an interactive, source-level cross-debugger*

The Whitesmiths Version 3.31 C cross-compiler package includes the CXDB/S68K cross-debugger. The package runs either on IBM PCs and compatibles or on VAX/VMS machines, and allows you to develop software for an embedded target system that is based on a processor of the 68000 family. The compiler includes source code of a subset of the vendor's ANSI-standard run-time library. The debugger provides nonintrusive simulation of the target code at the C source and symbolic assembly-language levels; it permits expression handling, user-defined functions, breakpoints, and stack searching. Using the package allows you to display both the C code and the assembly language, to monitor and display selected variables, and to control the execution of the program. PC version, $2500; VAX version, $10,000.

Whitesmiths Ltd, 59 Power Rd, Westford, MA 01886. Phone (800) 225-1030; in MA, (508) 692-7800. TLX 750246. FAX 508-692-3561.

Circle No 426

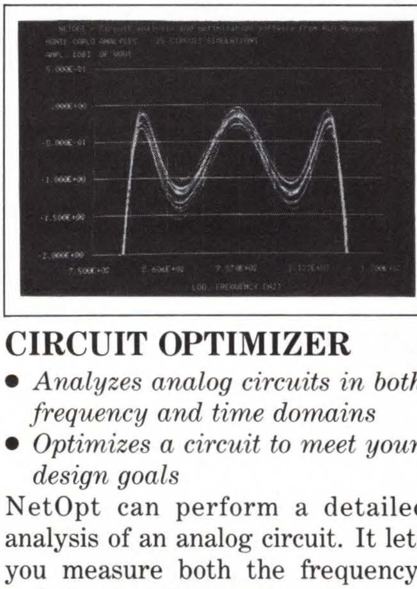
MODULA-2 COMPILER

- *Generates code for 8-, 16-, and 32-bit target systems*
- *Runs on a variety of host computers*

Running on workstations, and IBM PCs and compatibles, the Introl Modula-2 cross-development package lets you develop software for a variety of embedded target systems that are based on processors in the Motorola 6301, 6801, 6809, or 68000 families or in the National 32000 family. The package consists of an optimizing Modula-2 compiler that implements all the features of the language described in the third (corrected) edition of Niklaus Wirth's *Programming in Modula-2*; an optimizing, relocating macro cross-assembler; a library of run-time support functions that includes real-time, multitasking extensions; and a variety of utility programs. Versions are available for a wide variety of host computers, including IBM PCs and compatibles, Macintosh PCs, and Vax, Apollo, Sun, Hewlett-Packard, and Gould workstations. Depending on the host configuration, $2000 to $8000.

Introl Corp, 647 W Virginia St, Milwaukee, WI 53204. Phone (414) 276-2937. FAX 414-276-7026.

Circle No 427



CIRCUIT OPTIMIZER

- *Analyzes analog circuits in both frequency and time domains*
- *Optimizes a circuit to meet your design goals*

NetOpt can perform a detailed analysis of an analog circuit. It lets you measure both the frequency- and the time-domain responses and display them with the aid of the high-resolution graphics feature. The program can also perform a Monte Carlo analysis and will predict the manufacturing yield of the design from the component tolerances that you supply. The optimization feature allows you to specify design goals for output magnitude, phase shift, or group delay, then the program adjusts component values until the circuit most closely meets those goals. You can specify Minimax, least-squares fit, or constrained optimization as goals, as well as the tolerance or standard deviation of the circuit's amplitude response. You can also adjust a circuit to compensate for component-related parasitics or generate a circuit with a nonstandard frequency response. IBM PC version, $1995; VAX/Unix version, $3995.

RLM Research, Box 3630, Boulder, CO 80307. Phone (303) 499-7566. TWX 710-111-1401.

Circle No 428

SIMULATOR FOR 386

- *Runs in real mode on 80386-based machines*
- *Can make use of math coprocessors*

The IS_Spice/386 simulator package runs in protected mode on 80386-based machines. The program uses recent extensions to DOS that allow full access to all DOS functions from the protected mode, and it can make full use of all available memory. According to the vendor, these features, together with the ability to use either an Intel 80387 or a Weitek 1167 or 3167 math coprocessor, allow IS_Spice to achieve an execution speed that can be as much as four times faster than other versions of Spice. To run the program, you need an 80386-based computer that has 3M bytes of 32-bit memory, a hard disk, and DOS 2.0 or higher. $386.

Intusoft, Box 6607, San Pedro, CA 90734. Phone (213) 833-0710.

Circle No 429

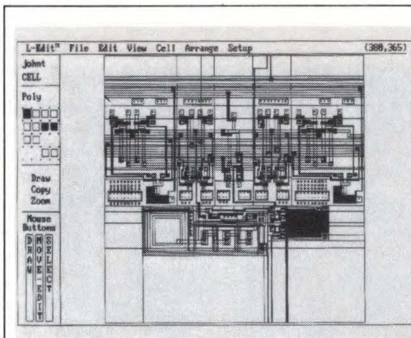
VHDL SIMULATOR

- *Provides tools that simulate both hardware and software*
- *Has a programmable command language*

Endot_VHDL is a tool that uses VHDL (VHSIC Hardware Description Language) to capture the structure of electronic systems, subsystems, and devices in a technology-independent format and to simulate their behavior. The interactive simulator allows the evaluation of expressions and can perform graphical and statisical analysis. The package incorporates all of the features of the vendor's N.2 system-design tools and includes a translator that converts the N.2 hardware-description code into VHDL. It can be integrated with the vendor's line of simulation-accelerator hardware via stimulus-translation and results-comparison tools. From $40,000 for a workstation configuration.

Zycad Corp, 3900 Northwoods Dr, Suite 200, St Paul, MN 55112. Phone (612) 490-2500.

Circle No 430



ASIC DESIGN TOOL

- *Provides color-graphics editing for ASIC design on a PC*
- *Output can be used by a wafer fab to produce $100 prototypes*

L-Edit is a color-graphics editor that you can use to design and layout ASICs, hybrid microcircuits, and pc boards. The MOSIS MOS Implementation System at the vendor's wafer-fab plant can accept the editor's output and generate four packaged prototype parts at a cost of $100 each. The wafer fab can handle 2.3×3.4-mm wafers and uses 3-μm CMOS technology. The editor is menu-driven and provides mouse-following cursors that let you use any of 64 colors (including pastels) and an 8×8-pixel matrix for stipple, crosshatch, and outline patterns. Redraw, pan, and zoom operations are fast because the algorithms don't need to process objects that are not currently on-screen. To save further time, the program structures data files as lists instead of arrays and stores them in binary, rather than ASCII format. According to the vendor, the execution speed of the editor on a 10-MHz PC/AT clone is four-times faster than that of an equivalent program running on a Sun 4/260 equipped with an accelerator. $495.

Tanner Research Inc, 128 W Del Mar Blvd, Pasadena, CA 91105. Phone (818) 795-1696.

Circle No 431

MATH-MODEL LIBRARY

- *Provides software for 16 common computational tasks*
- *Works with MathCAD engineer's problem-solving program*

The Advanced Math Applications Pack consists of mathematical models that solve specific computational problems in conjunction with MathCAD version 2.0. The package provides software and documentation for tasks that include first- and second-order differential equations, real and complex eigenvalues and eigenvectors, convolutions, polynomial least-squares fit, digital filtering, conformal mapping, diffusion, Laplace equations, and static equilibrium. You can customize any of the models. MathCAD lets you use an IBM PC or compatible as a scratchpad to enter and solve equations; the graphics features allow the program to display your equations in standard mathematical symbols. MathCAD, $395; Advanced Math Applications Pack $40.

MathSoft, 1 Kendall Sq, Cambridge, MA 02139. Phone (617) 577-1017. FAX 617-577-8829.

Circle No 432

"EDN'S MAGAZINE AND NEWS EDITIONS ADDRESS THE WORLDWIDE LINEAR IC MARKET WE'RE AFTER."

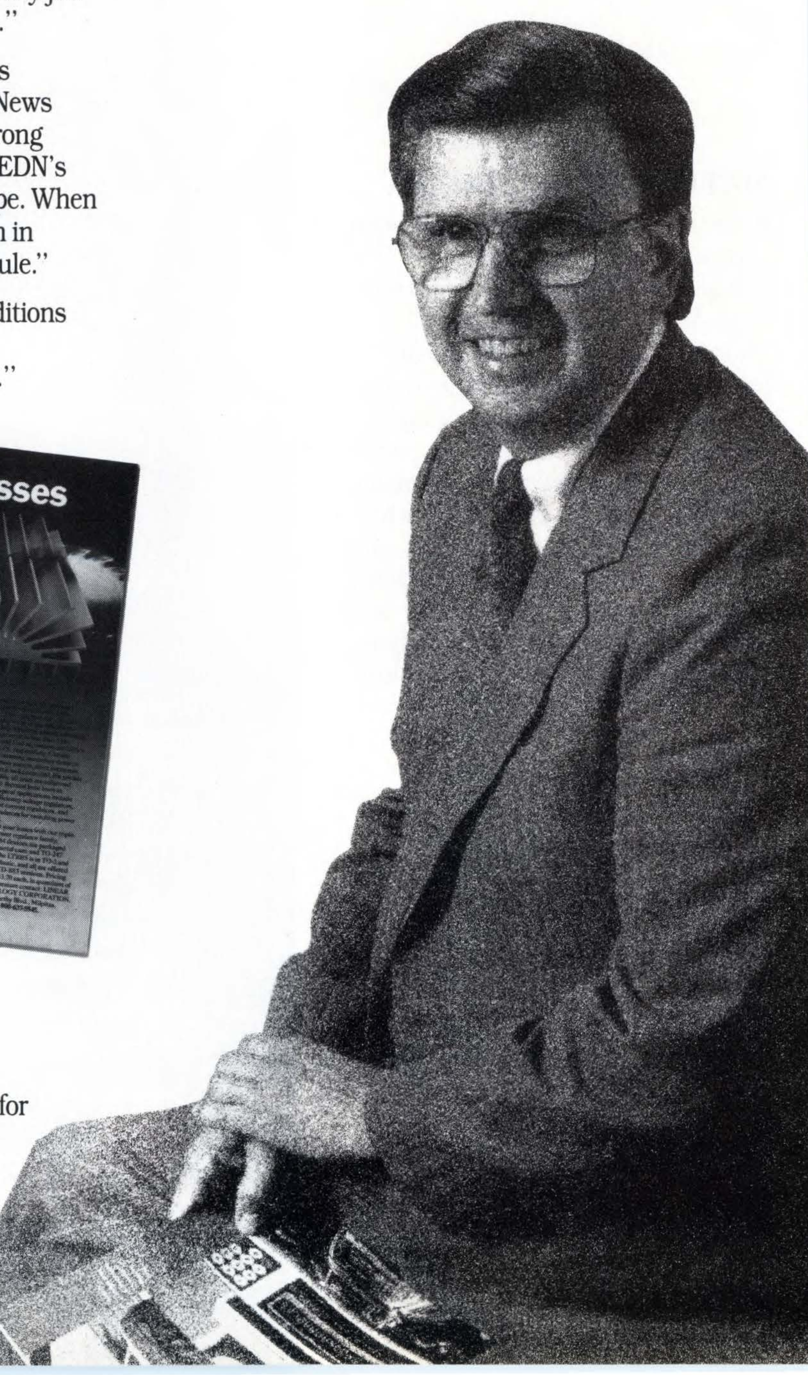
Bill Ehrsam
Vice President of Marketing
Linear Technology Corporation

"When I buy EDN's Magazine and News Editions, I'm buying a powerful worldwide circulation and the most prestigious editorial environments available. That's a combination that gets results," says Bill Ehrsam, Vice President of Marketing for Linear Technology Corporation.

Ehrsam knows industry sales for high-performance linear ICs are split between the United States, Western Europe, and the Pacific Rim. Says Ehrsam, "It's my job to choose media that mirrors the world markets."

For complete global coverage, Ehrsam places his advertising in EDN Magazine Edition and EDN News Edition. "Linear Technology Corporation is a strong supporter of EDN Magazine Edition. We rely on EDN's targeted coverage of the U.S. and Western Europe. When EDN News Edition added Pacific Rim circulation in December 1987, we added it to our media schedule."

For Bill Ehrsam, "EDN's Magazine and News Editions form the cornerstone for Linear Technology Corporation's media plan now and in the future."



Advertising in EDN Magazine and News Editions works for Linear Technology Corporation. It can work for you.

EDN

Where Advertising Works

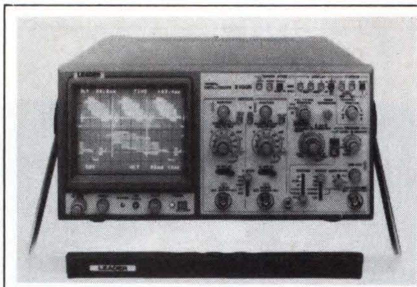
PROGRAMMER

- *Supports all types of PROMs and PLDs with 16 to 40 pins*
- *With SMD station, supports LCCs and PLCCs to 68 pins*

The System 3000 uses pin drivers—identical, configurable driver/detector circuits—for all device pins. As a result, its manufacturer claims that it can handle all currently available programmable devices (over 1600 types in DIPs with 16 to 40 pins) as well as any likely to appear well into the 1990s. With an SMD adapter, it can also handle devices in LCCs and PLCCs with 20 to 68 leads. The base configuration contains 2M bits of program RAM; you can expand it to 64M bits. A credit-card-size IC memory card contains the library of supported devices and programming algorithms; to update the library, you slip in a new memory card. With its own CRT display and keyboard, the programmer can stand alone; but its two RS-232C ports, IEEE-488 port, and handler interface facilitate connecting it to other equipment. $9495; additional RAM, $500/2M bits; SMD adapter, $2900.

Stag Microsystems Inc, 1600 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 988-1118.

Circle No 435



100-MHz SCOPE

- *Displays many setup parameters on screen*
- *Uses cursors to measure voltage, time, and frequency*

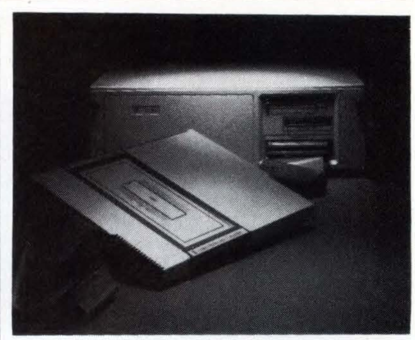
The 2100R is a 100-MHz bandwidth, 3-channel oscilloscope. It displays such setup parameters as scale factor, input coupling, vertical mode, main and delayed sweep times, and trigger-control settings in alphanumeric form on its CRT. In addition, by manipulating cursors on the display, you can obtain on-screen numeric readouts of voltage, voltage ratios, time, time ratios, frequency, and phase. The scope has many triggering and sync modes, and it offers an automatic timebase mode that displays several cycles of an input waveform. Maximum sensitivity is 0.5 mV/div. A rear-panel channel-1 output facilitates connection of additional instruments, such as a frequency counter. $2195.

Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788. Phone (516) 231-6900. TWX 510-227-9669.

Circle No 436

68000 EMULATOR

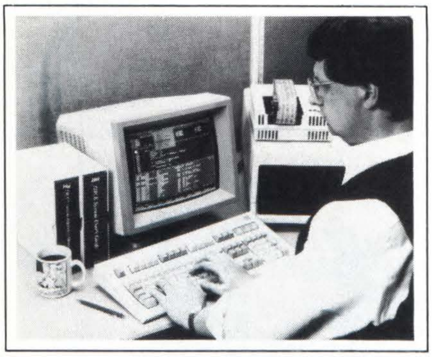
- *Emulates 68000 at 16.7 MHz with zero wait states*
- *Works with VAX, Sun, Apollo, and IBM PC hosts*



The ES 1800 16.7-MHz probe module allows the vendor's ES 1800 in-circuit emulator (ICE) to emulate the 68000 μP with zero wait states. The ICE works with VAX, Sun, Apollo, and IBM PC, PC/XT, PC/AT, and compatible hosts. It allows program control by breaking on any combination of address, data, status, pass-counter, and logic-state fields. An optional SCSI interface transfers data to and from the host at much higher rates than the standard RS-232C interface. A C language source-level debugger works with all of the above-named hosts except those made by Apollo. ES 1800 16.7-MHz probe module, $4095; ES 1800 ICE, from $11,000.

Applied Microsystems Corp, Box 9702, Redmond, WA 98073. Phone (800) 426-3925; in WA (206) 882-2000. TLX 185195.

Circle No 437



EMULATOR INTERFACE

- *Provides windowed displays and pull-down menus*
- *Works with the vendor's in-circuit emulator*

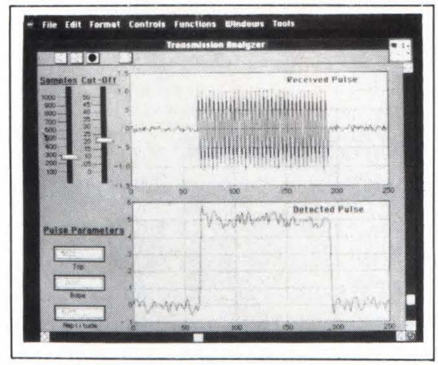
ICEview graphical-interface software works with the vendor's I²ICE in-circuit emulator that supports real-time testing and debugging of the 8086, 8088, 80186, 80188, and 80286 μPs at speeds to 10 MHz. The graphical interface, which works with monochrome displays as well as color displays that support the CGA and EGA standards, provides pull-down menus that simplify access to application information and emulator functions. With the interface, you can open and maintain windows for display of application source code, execution-trace data, and register contents. You can view data by stepping through programs, or you can observe data as it changes at breakpoints. $495, until December 1988.

Intel Corp, Box 58065, Santa Clara, CA 95051. Phone (800) 548-4725.

Circle No 438

INSTRUMENT SOFTWARE

- *Runs on Macintosh II, SE, and Plus computers*
- *Allows instrument control through virtual front panels*



Version 2.0 of Labview is a graphical programming system that runs on Macintosh II, Plus, and SE computers. In addition to facilitating data analysis, the software's on-screen virtual front panels let you control instruments interfaced to the serial ports of slotless computers via IEEE-488 buses generated by external controllers. If you use a Macintosh II, the software supports color displays and lets you control instruments resident on cards that plug into the Nubus. Unlike what occurred with earlier versions, data acquisition and processing continue while you work with on-screen pull-down menus and dialog boxes. Furthermore, a graphi-

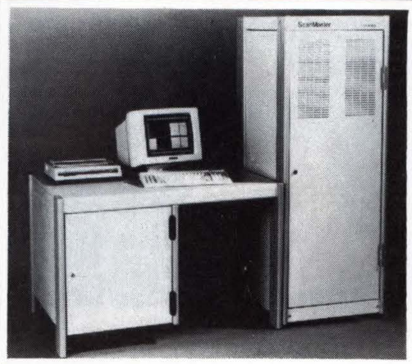
cal-language compiler speeds performance of computation-intensive functions by a factor of as much as 60. $1995.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737. FAX 512-250-0382.

Circle No 439

ASIC VERIFIER

- *Achieves high fault coverage on scan-path-designed ICs*
- *Expands to 1792 pins in 128-pin increments*



The Scanmaster DV-6005 is an unusual design-verification system for ASICs. It tests devices that conform to scan-path design rules. The vendor claims that, regardless of a device's gate count, the tester can identify all stuck gates and can thus provide complete fault coverage on the most complex devices. In addition to functional verification, the system measures dc parameters. To test the dynamic (ac) properties of an IC, the system uses a "scan-ring" technique—it interconnects the scan circuits' inputs and outputs to form a free-running oscillator whose oscillation frequency is a measure of the device's speed. The system is based on an IBM PC/AT-compatible computer. It is modular in increments of 128 pins and can accommodate 1792 pins. Each module can contain four scan generators. The maximum scan memory has 256M bytes. From $125,000. Delivery, 60 days ARO.

Gillytron Inc, 2150 Bering Dr, San Jose, CA 95131. Phone (408) 435-3043. FAX 408-435-5089.

Circle No 440

RECORDER

- *Provides digital or chart recorder output*
- *Accepts plug-in front-end measurement instruments*

The Model 520 data-acquisition and recording system accepts a range of plug-in front-end instruments and produces digital or pen-recorder trace outputs. The front-end instruments, which digitize input signals at 30 readings/sec, include a 15-bit dc measurement module, a 15-bit DVM module, a 13-bit DMM module, a thermocouple linearization module, and a 100Ω PRT (platinum resistance thermometer) module. The recorder can preprocess measured data and output it in digital form over optional IEEE-488 or RS-232C interfaces. In addition, you can plot the data on the unit's integral 10-in., 2- to 8-pen chart recorder. The chart recorder has 0.1% nonlinearity, a ±0.2-dB frequency response of 1.5 Hz, and a 10 to 90% full-scale-deflection step response of

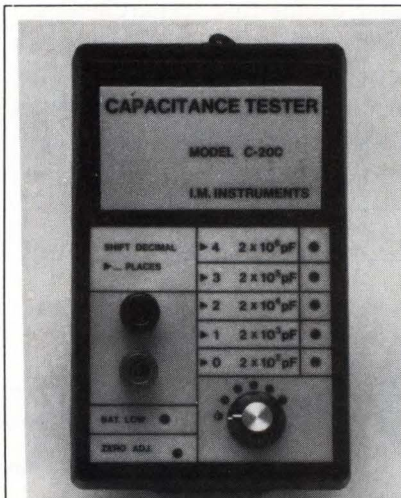
200 msec. It features trace annotation, trace overlap, retrace, and external synchronization facilities. The Model 520 is portable and operates from 110 or 220V ac line supplies or from a 10 to 32V dc supply. Options include an alarm module that detects and flags out-of-limit input signals. From £3500.

Kontron Elektronik, *Oskar-von-Miller-Strasse 1, 8057 Eching, West Germany. Phone (08165) 707103. TLX 526719. FAX (08165) 707113.*

Circle No 455

Kontron Electronics Inc, *630 Clyde Ave, Mountain View, CA 94039. Phone (415) 965-7020. TWX 910-378-5207. FAX 415-965-3505.*

Circle No 441



C AND L METERS

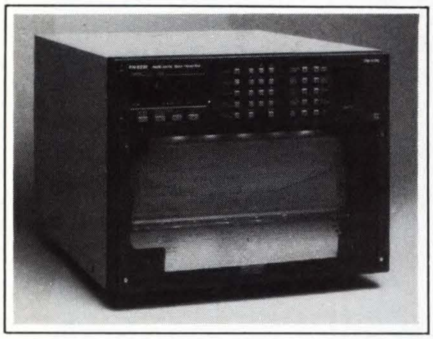
- *Add measurement functions to DVMs*
- *Measure nanohenries and femtofarads*

The C-200 and L-200 are $3\frac{1}{2} \times 5\frac{3}{4}$-in., 9V-battery-powered units that respectively add capacitance- and inductance-measuring capabilities to digital voltmeters. When used with a $5\frac{1}{2}$-digit meter, the C-200 can measure capacitances as small as 1 femtofarad and as large as 2 μf. With the same DVM, the L-200 can measure inductance from 1 nH to 2H. The ac signals the units apply to the component under test repeat at 200 kHz. The C-200 applies

2V max, and the L-200 forces 5 mA max into the component. C-200, $149; L-200, $199.

I.M. Instruments, 776 Colborne St E, Brantford, Ontario, Canada N3S 3S1. Phone (519) 756-3770. FAX 519-759-1547

Circle No 442



MULTIPOINT RECORDER

- *Records 30 simultaneous inputs in 3 sec*
- *Can resolve 1 μV over 10-in. chart*

The PM 8238 multipoint data recorder records as many as 30 simultaneous inputs in 3 sec. At its maximum sensitivity, it can resolve signal changes as small as 1 μV anywhere on its 10-in.-wide chart. Zero suppression lets you put the signal range of interest on the chart, and the wide range of transport speeds lets you display data so that you can interpret it. The recorder accepts 2-, 3-, and 4-wire transducer outputs. Plug-in memory modules store range, span, linearization, and chart-speed settings and allow you to quickly recall instrument setup conditions. Thermal printing eliminates problems associated with ink-writing systems. $5500; industrial version with full-size front door, $5950.

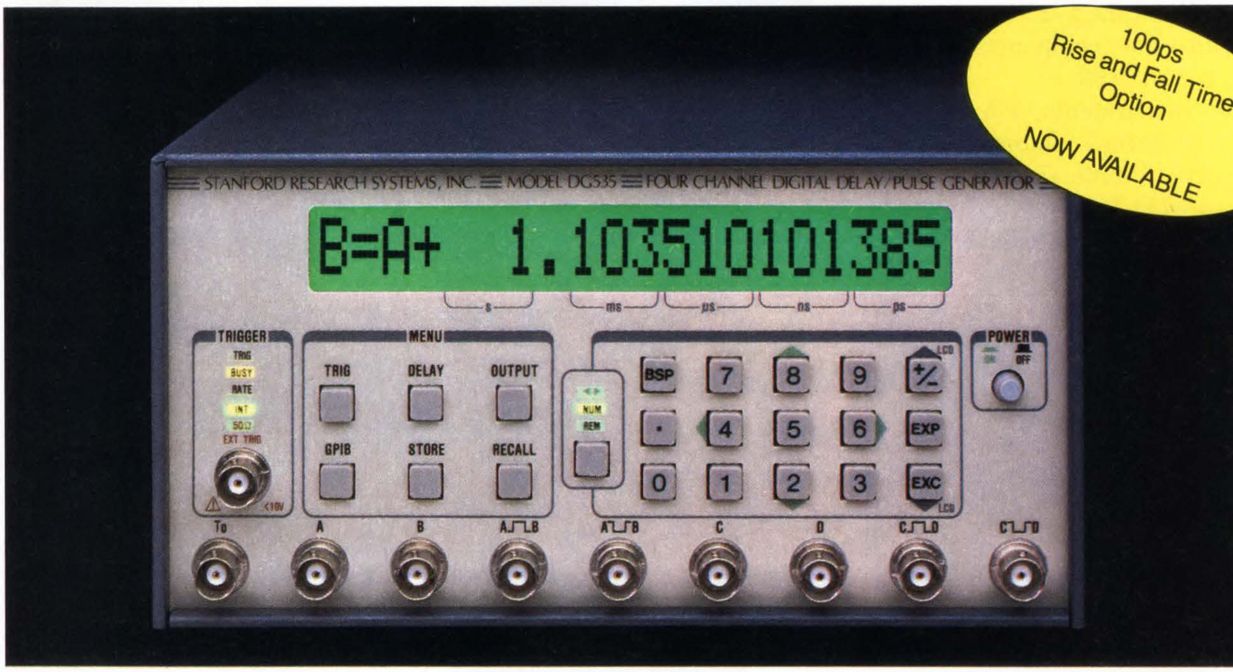
John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853 Ext 77; in WA, (206) 347-6100. TLX 185102.

Circle No 443

Philips Test and Measurement, Bldg HKF, 5600 MD Eindhoven, The Netherlands. Phone local office.

Circle No 444

New Precision Pulse Generator



Four Channels, 5 ps Resolution, and GPIB Interface...Price: $2995

TIMING IS EVERYTHING

Your critical timing problems are over. No more worries about drift, jitter, or control. The DG535 Precision Pulse Generator has four delay channels (two pulse outputs), each with a 1000 second range and 5 ps resolution. The four independent delays specify two variable-width pulse outputs. With only 50 ps jitter and accuracy down to 1 ppm (option 03), the instrument can handle the most demanding applications. The internal trigger may be programmed from 0.001 Hz to 1.000 MHz, or operated in single-shot or burst modes. Output levels are continuously adjustable or may be set to TTL, NIM, or ECL levels. High impedance or 50 Ohm loads can be driven with a slew rate of 1 V/ns. Optional rear panel outputs generate pulses to 35 volts.

EASY TO USE

The delay and output levels for each channel may be entered numerically or modified by cursor keys on the backlit LCD display. Delays may be linked together so that as one moves, the other follows. Up to nine instrument settings may be stored in nonvolatile RAM for later recall, and, of course, all of the instrument's functions may be controlled via the GPIB interface.

A GENERATION AHEAD

The DG535's precision, accuracy, range, and versatility make it the solution to all your timing needs, at a price that will meet your budget. Call us today for more information.

FEATURES AND PERFORMANCE

- **Four Delay Outputs**
- **Two Variable-Width Outputs**
- **Times from 0 to 1000 sec.**
- **5 ps Resolution**
- **50 ps rms Jitter**
- **1 ppm Accuracy (Option 03)**
- **Internal or External Timebase**
- **Internal, External, Single-Shot, or Burst Mode Triggers**
- **Frequency Synthesized Rate Generator**
- **Variable, TTL, NIM, and ECL Outputs**
- **Optional ± 35 Volt Outputs**
- **GPIB Computer Interface**

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0 8105/5011, TLX 523862

JAPAN
Tokyo Instruments
Koizumi Building
6-10-13-403 Nishikasai
Edogawa-ku, Tokyo 134
03 (686) 4711, TLX J326463

Seki and Company
1-2-6, Nihonbashi Ningyocho
Chuo-ku, Tokyo 103
03 (669) 4121, TLX J24419

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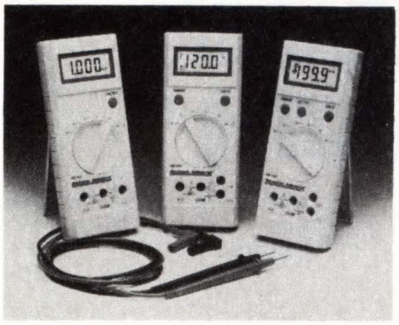
02302/3410, TLX 825633

Stanford Research Systems, Inc.

1290 D Reamwood Avenue, Sunnyvale, CA 94089, TLX 706891 SRS UD, FAX 4087449049, TEL (408) 744-9040

CIRCLE NO 232

See us at Wescon Booth #4217 and 4219



INDUSTRIAL DMMs

- *Survive 10-ft drop onto concrete*
- *Indicate measured value, using audible tone*

The HD151, HD152, and HD153 3½-digit autoranging DMMs survive a 10-ft drop onto a concrete surface. The meters, each of which is about the size of two cigarette packages placed end to end, carry a five-year warranty against the entry of contaminants. The instruments differ primarily in basic accuracy (for dc-voltage measurements—0.7, 0.5, and 0.25% plus one count for the HD151, HD152, and HD153, respectively). The meters include "sky hooks" that, according to the vendor, enable you to hang them "virtually anywhere." On the HD153, a V/F converter drives a small loudspeaker that produces a tone whose pitch is proportional to the measured value. This audible indication of the measured value permits use of the meters in situations where the LCD display is hidden. HD151, $149; HD152, $169; HD153, $199.

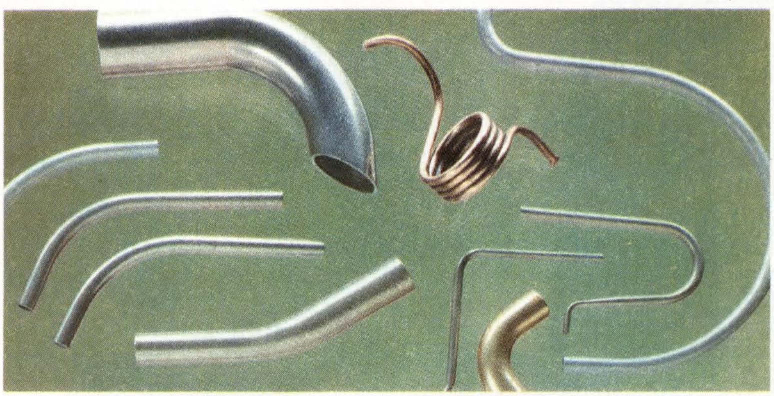
Beckman Industrial Corp, 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3200. TLX 249031.

Circle No 445

ELECTRONIC LOAD

- *Is programmable for 0 to 10A load currents*
- *Employs internal batteries to avoid common mode problems*

Suitable for power supply testing, the Powerload-50 electronic load has a continuous maximum load rating of 50W. It accepts dc input volt-



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John Poturny, President
Poturny & Associates
Northridge, CA

Fred Silver, Director of Marketing
Rantec
Chatsworth, CA

Advertising results. Agencies want them. Clients need them.

"When I was on the client side, I demanded sales results from my advertising dollars," says John Poturny, President of Poturny & Associates. "Today I'm on the agency side, and I expect the same for my clients — advertising that generates sales."

Advertising results. A publication must provide them.

"After running ads in EDN News Edition, our phones ring and proposal activity soars immediately for our military power supplies," says Fred Silver, Director of Marketing at Rantec, a division of Emerson Electric.

Advertising results. For Poturny & Associates and Rantec, EDN News Edition gets them.

"We traced prototype orders worth $2 million in sales to a lead generated by our ad in EDN News Edition," said Silver.

Both Silver and Poturny agree about the power of EDN News Edition, "it gets results."

EDN News Edition works for marketing communication partners, Poturny & Associates and Rantec. It can work for you.

EDN

Where Advertising Works

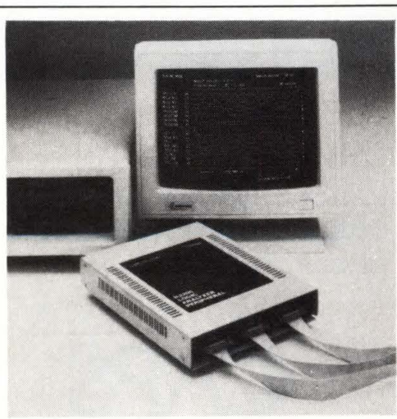
ages between 3 and 75V and allows you to program the load current to any value between 0 and 10A. An external programming input lets you control the load current with a 0 to 10V analog input signal. Built-in panel meters monitor the load current and voltage, and a 0 to 1V analog output allows you to monitor the load current using external equipment. The unit has built-in rechargeable batteries so that you can operate it as a stand-alone unit to avoid problems caused by common-mode currents. The Powerload-50 has an operating temperature range of 0 to 40°C and is protected against overtemperature conditions by a thermostat. It measures 132×135×220-mm (5.2×5.3×8.7-in.). Around $465.

Powerbox AB, Box 148, 15400 Gnesta, Sweden. Phone (0158) 11920. TLX 11502. FAX (0158) 11811.

Circle No 446

Powerbox Inc, 1503 Spruce St, Boulder, CO 80302. Phone (303) 444-1461. FAX 303-444-3135.

Circle No 447



LOGIC ANALYZER

- *Clocks 8 channels at 100 MHz or 24 channels at 25 MHz*
- *Uses IBM PC for control and data storage*

The R3200 logic-analyzer peripheral for IBM PCs and compatible computers provides 8 channels at 100 MHz, 16 channels at 50 MHz, and 24 channels at 25 MHz. The instrument consists of a board that

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CIRCLE NO 233

plugs into the PC bus as well as an externally mounted unit. The analyzer performs both timing and state analysis. Its memory depth is 8k words/channel. You can store logic patterns on disk and retrieve them, and you can "zoom in" on segments of stored patterns. $1995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No 448

PC-BASED TESTER

- *Measures dc volts and ohms*
- *Provides two programmable voltage outputs*

The SYS-127 is a dc and digital test system based on a PC that you provide. It includes a 4½-digit autoranging volt/ohmmeter, a pair of independently programmable voltage sources whose output varies over the ±10.5-volt range with 20-μV resolution, 21-bit parallel digital I/O, and three 8-bit parallel control ports for interfacing to logic or relays. You can use the system to test components, modules, and circuit boards. To make data displays and print-outs easier to interpret, you can make the values assumed by either source output or the 21-bit digital port appear as the X coordinate of an X-Y display; measured values appear along the Y axis. The supporting software's "learn" mode enables the creation of test sequences without programming. $2750.

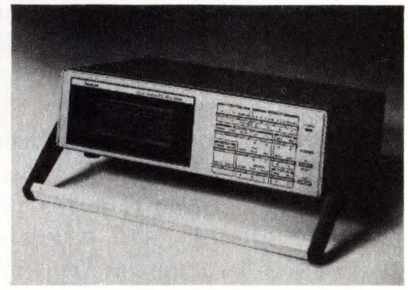
Audio Precision, Box 2209, Beaverton, OR 97075. Phone (800) 231-7350; in OR, (503) 627-0832. TLX 283957.

Circle No 449

LOGIC ANALYZER

- *Uses LCD; weighs 7 lb; operates from ac or battery*
- *Samples 16 channels at 10 MHz*

The PLA-3300 is a 16-channel logic analyzer with a liquid-crystal display. It weighs 7 lb and operates from ac or internal batteries. The unit can sample data at 10 MHz, and it has 256 bits/channel of acqui-



sition and reference memory. The contents of these memories remain intact when power is off; an automatic power-shutdown feature extends battery life. The analyzer performs state, timing, and signature analysis. It also captures 15-nsec-wide glitches and triggers when it detects a glitch. The unit includes an IEEE-488 interface. $2495.

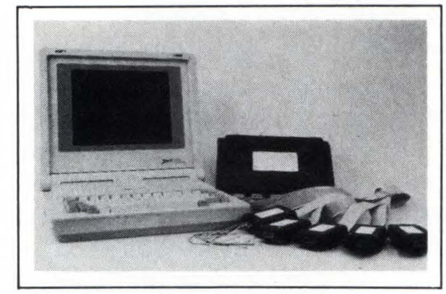
Primeline, Box 670, San Fernando, CA 91341. Phone (800) 525-5554; in CA, (818) 365-0101. TLX 4943094. FAX 818-365-7839.

Circle No 450

LOGIC ANALYZER

- *Performs 32-channel state and 8-channel timing analysis*
- *Uses IBM PC for data storage and control*

The PCLA-32 logic analyzer performs 32-channel state analysis and 8-channel timing analysis in con-



junction with an IBM PC or a compatible computer. For timing analysis, you can set the sampling period from 10 nsec to 1 msec and store 8118 samples/channel. The unit can detect glitches whose duration are at least 6 nsec. For state analysis, the minimum clock period is 40 nsec and the storage depth is 2047 samples/channel. State-machine triggering with 15 states utilizes eight comparators whose outputs you can logically combine; occurrence counters for each state can count to 2064. Disassemblers for popular μPs allow on-line debugging. You can define the symbols that appear in trace listings. The trace function will operate once or will repeat until the trace buffer contents become equal to (or not equal to) the contents of a reference memory. $2000.

Nobel Systems, Box 13083, La Jolla, CA 92038. Phone (619) 452-3208. FAX 619-457-0579.

Circle No 451

PC-BASED INSTRUMENTS

- *Make PC into 4½-digit DMM and function generator*
- *Accept English-language commands*

The PCIP-DMM 5-function, 4½-digit multimeter has isolated inputs and 0.03% basic error. The PCIP-SST 1-Hz to 5-MHz sine/square/triangular-wave generator provides limited operation to 10 MHz. Both are on cards that plug into the IBM PC bus. You program both instruments using English-language commands. For example, the command

"WE'VE GAINED MAXIMUM EXPOSURE WITH THE PRODUCT MART SECTIONS OF **EDN MAGAZINE** AND **EDN NEWS!**"

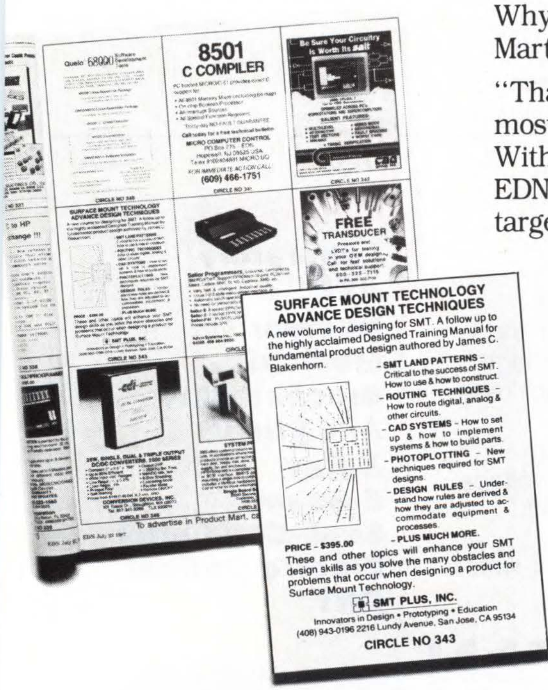
Cosette Trautman-Scheiber
Marketing Manager
SMT Plus, Inc.
San Jose, CA

Cosette Trautman-Scheiber is the marketing manager for SMT Plus, Inc., a two-year-old company that provides surface-mount designing, assembling, and education services.

Cosette has watched SMT Plus triple its sales in the last year. "We have a small advertising budget, and as a growing company, visibility is important. We need to reach the right audience, at the right time, for the right price."

Where does Cosette place her advertising?

"In the Product Mart sections of EDN magazine and EDN NEWS."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"Set offset −4.5" adds a dc offset of −4.5V to the waveform produced by the function generator. Running the CONFIG.SYS file establishes the instrument's command syntax. You can then control the instrument from a program written in any language by "opening" the device and sending it an ASCII string of the proper syntax. PCIP-DMM, $699; PCIP-SST function generator, $999.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989.

Circle No 452

POWER ANALYZER

- *Measures delivered and absorbed power*
- *Displays magnitude of harmonics to the 13th*

The PM1000 is a µP-based power analyzer designed in accordance with IEC348 Class 1. It measures power delivered by a source and power absorbed by a load and provides displays of many ac waveform properties, including the content of harmonics from 0 (dc) to the 13th. The unit also measures apparent power (VA), power factor, rms voltage and current, voltage and current crest factor, frequency, and peak inrush current. From $2175.

Powerline Inc, 10 Cochituate St, Natick, MA 01760. Phone (508) 655-7987. TWX 510-100-3630. FAX 508-655-7984.

Circle No 453

WAVEFORM DIGITIZER

- *Samples two channels to 20M samples/sec*
- *Stores 64k or 128k samples/channel*

The R2088 waveform digitizer samples two channels simultaneously at speeds to 20M samples/sec. Each

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Rapid Systems, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017. FAX 206-548-0322.

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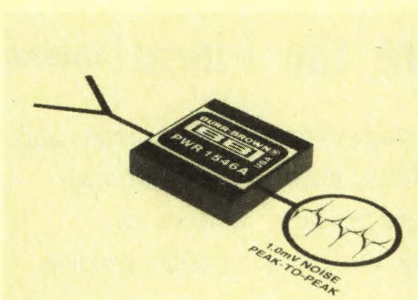
EDN PRODUCT MART

This advertising is for new and current products.

Please circle Reader Service number for additional information from manufacturers.



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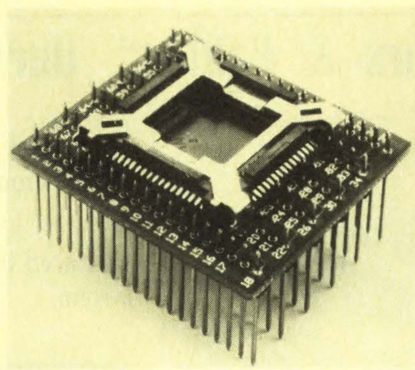

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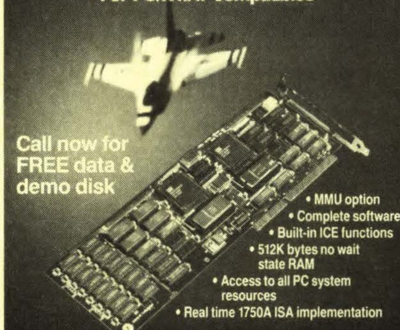

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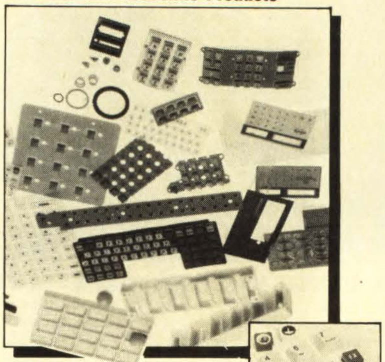

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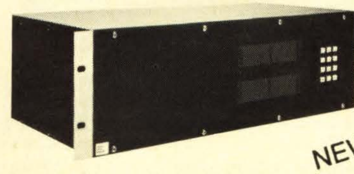

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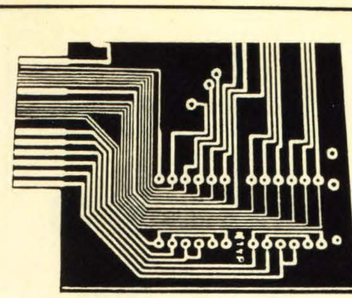

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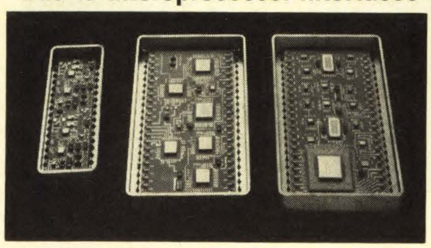

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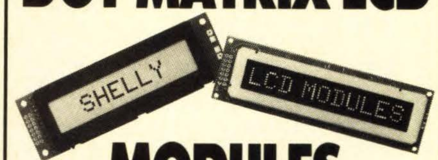

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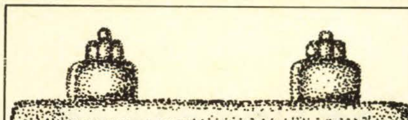

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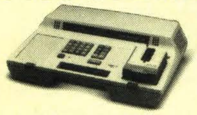

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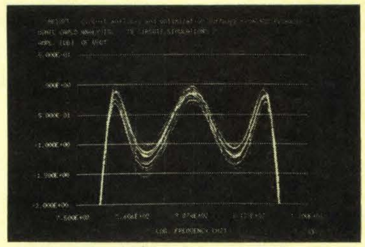

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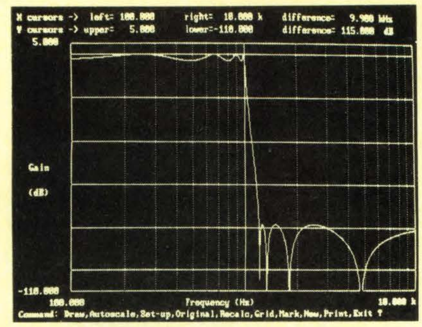

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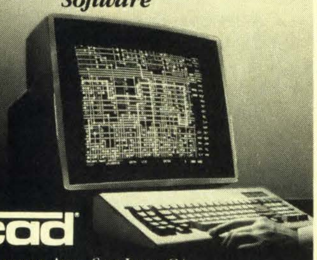

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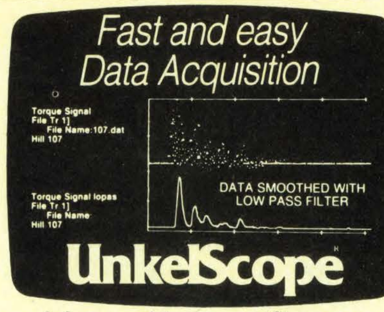

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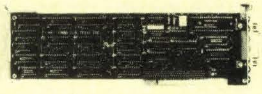

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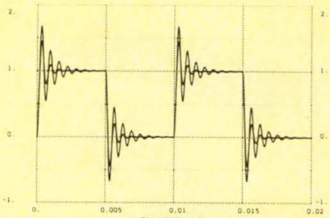

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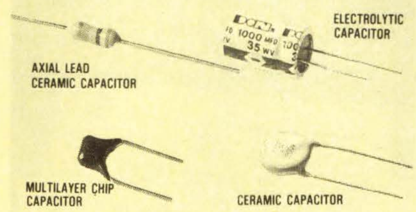

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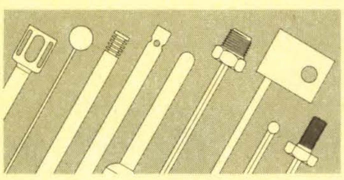

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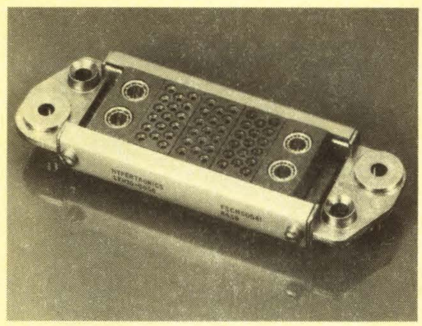

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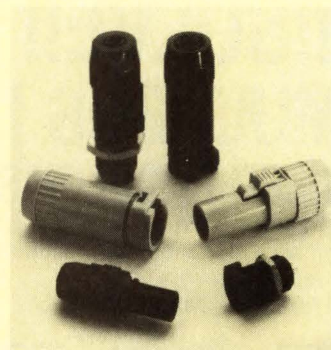

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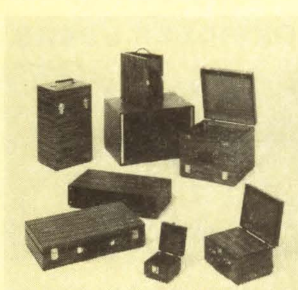

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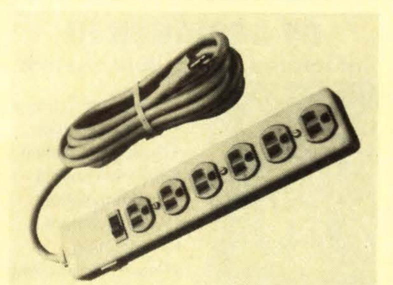

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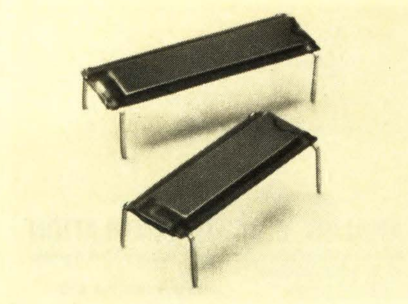

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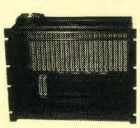

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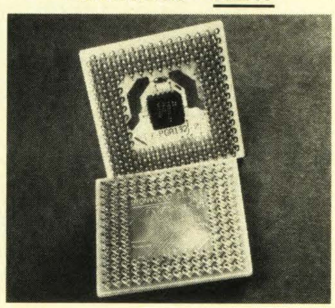

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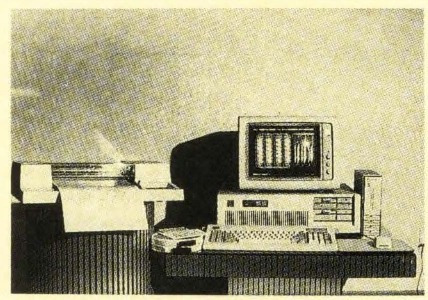

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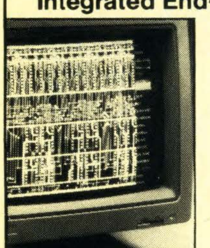

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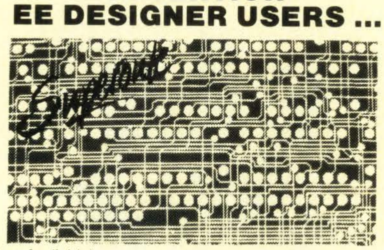

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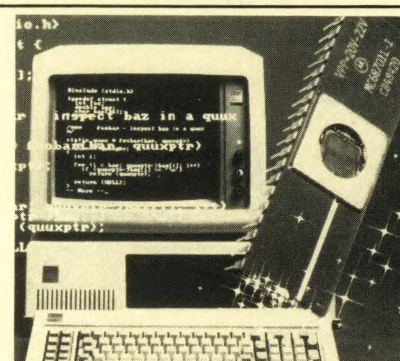

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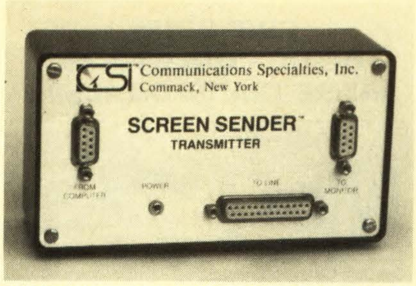

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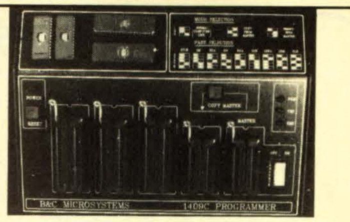

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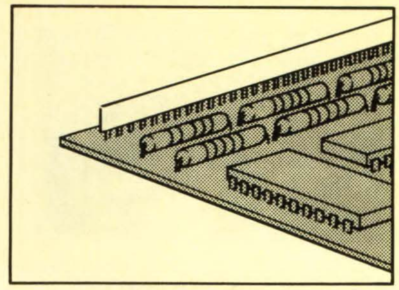

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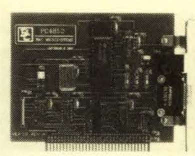

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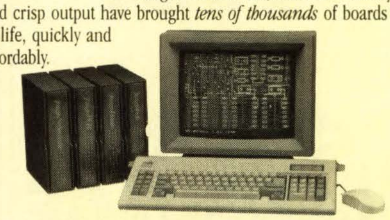

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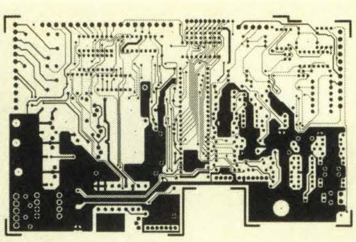

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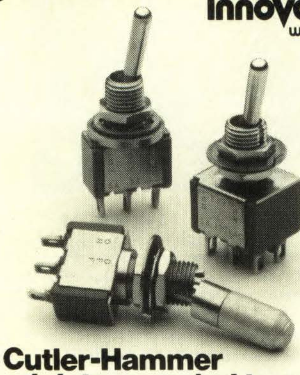

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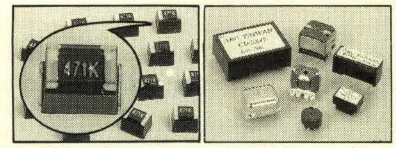

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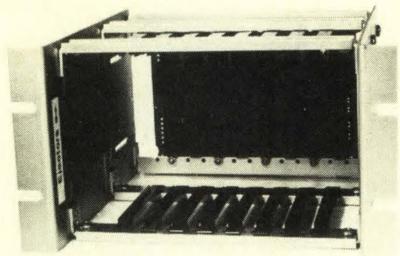

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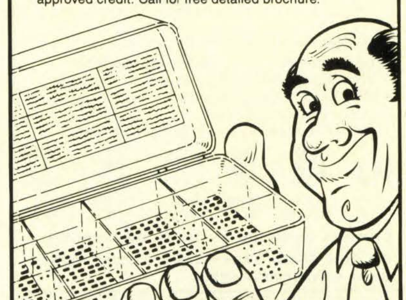

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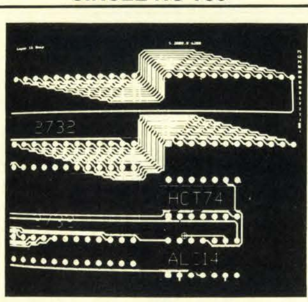

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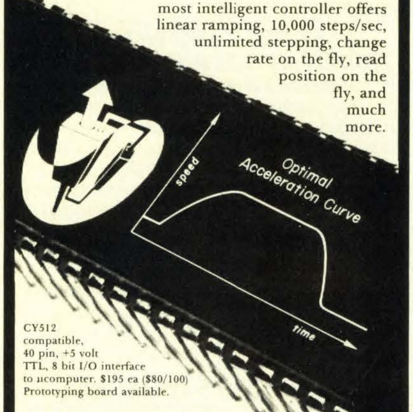

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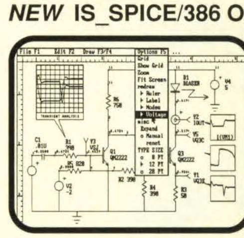

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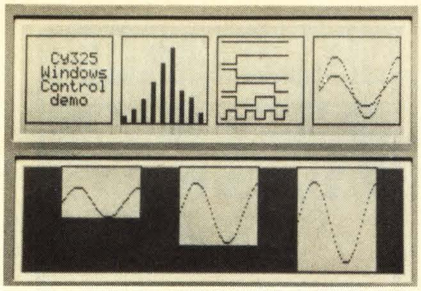

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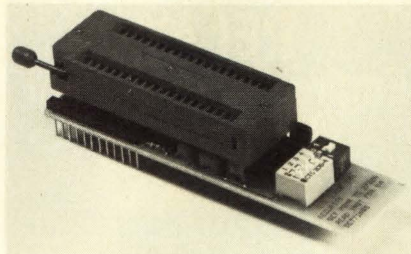

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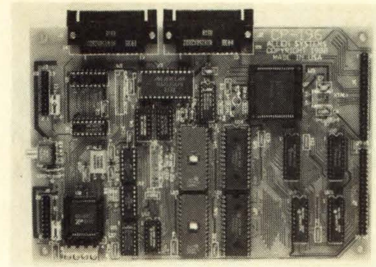

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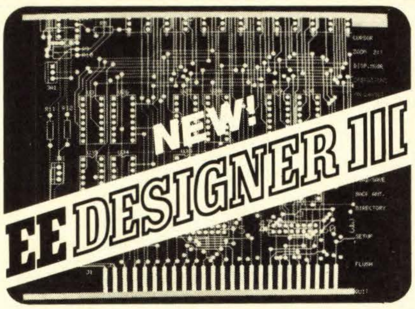

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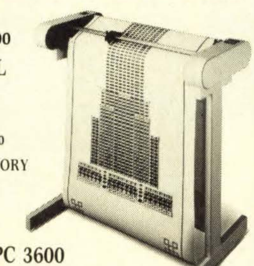

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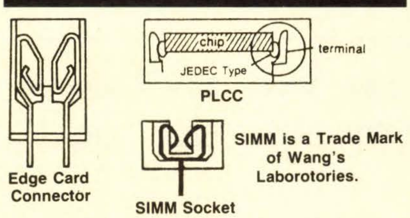

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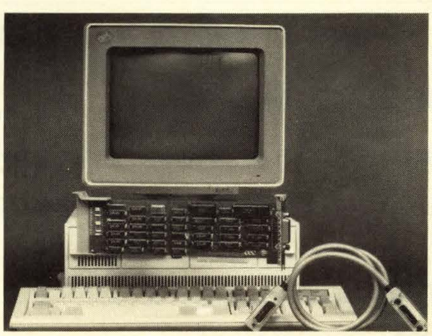

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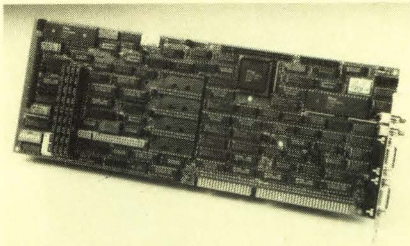

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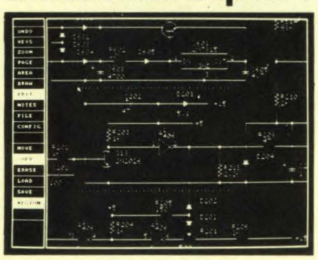

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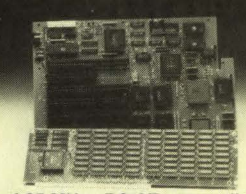

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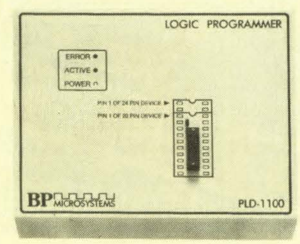

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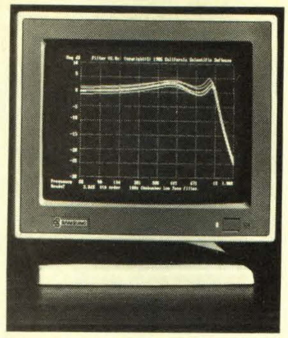

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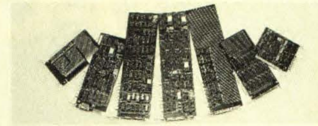

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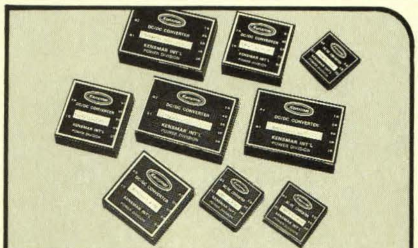

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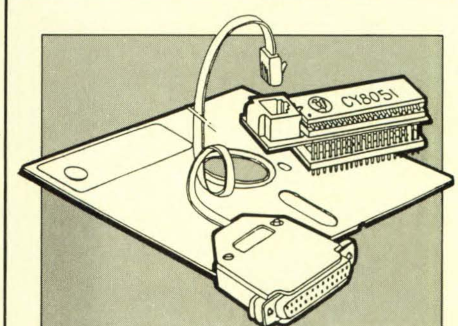

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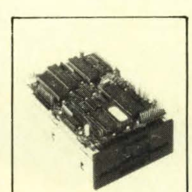

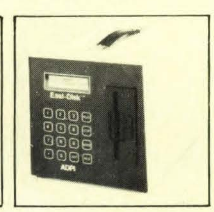

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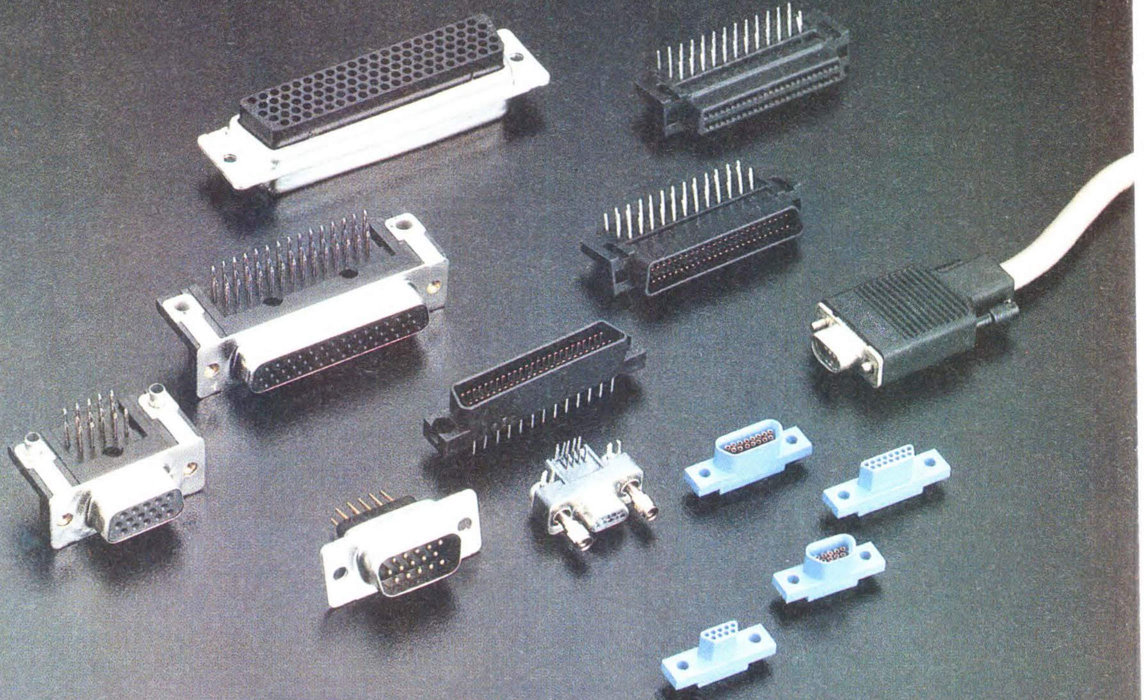

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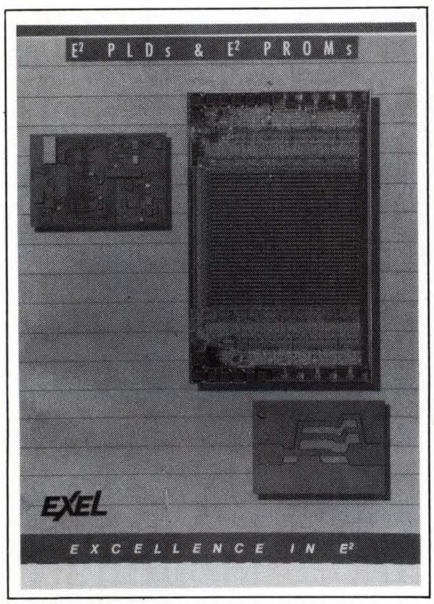


Databook features EEPLD, EEPROM devices

The company's 326-pg E2 Databook presents an extensive line of electrically reprogrammable PLD and memory devices. Besides overviews of E2 technology, the publication provides specifications, article reprints, design examples, and manufacturing procedures for MIL-STD-883C devices. The volume's four main sections deal with general information, PLD products, memory products, and packaging information. Specific application notes are also included.

Exel Microelectronics Inc, Box 49007, San Jose, CA 95161.

Circle No 460

Brochure deals with frequency synthesizers

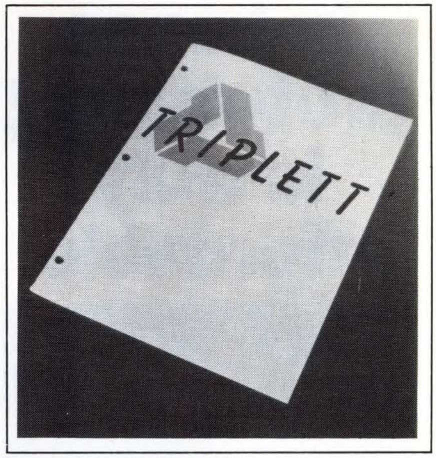
The vendor's 14-pg technical brochure discusses 1-μsec switching frequency synthesizers, detailing the Model FS-2000's technology, switching speed, and phase noise. Application information includes radar and simulators. In addition to complete mechanical and electrical specifications, the booklet contains standard and custom OEM configuration guides and IEEE-488 programming examples.

Comstron Corp, 10 Hub Dr, Melville, NY 11747.

Circle No 461

Catalog features panel meters and bar graphs

Presenting an overview of the vendor's digital panel meters and bar graphs, this catalog includes recently added products as well. The 32-pg manual highlights the "A+" Series digital panel meters, which are compared in a reference chart. This section also describes ac and



dc voltage and current meters, meter relays, process monitors, a counter, BCD monitors, and thermocouple meters. The second section focuses on the full line of LCD bar graphs, standard LCD meter relays, LCD "Vu" meters, ac meters, and programmable LED meters.

Triplett Corp, 1 Triplett Dr, Bluffton, OH 45817.

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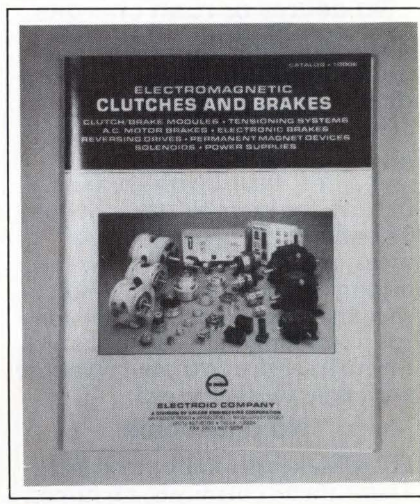


Directory of control devices

The company's 160-pg catalog discusses its electromagnetic rotary-motion control devices, including clutches, brakes, tensioning systems, clutch couplings, power supplies, and related products for industrial, aerospace, and military applications. The book provides complete technical details, applications, specifications, and features for each product. In addition to sections on the aforementioned products, the book includes sections on failsafe brakes, solenoids, and timers.

Electroid Co, 45 Fadem Rd, Springfield, NJ 07081.

Circle No 463

Catalog covers strip-chart recorders

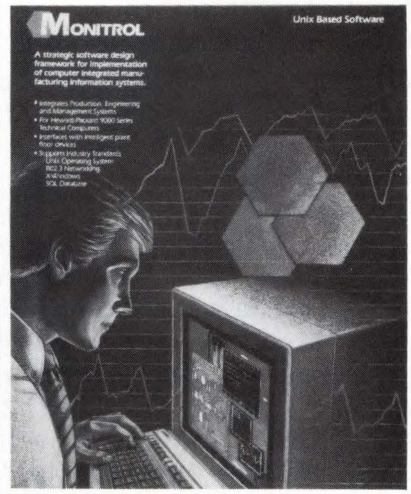
The company's 52-pg catalog of strip-chart recorders describes galvanometric, event, and servo recorders and highlights the Digilog Series temperature/humidity recorders with LCD readouts. The publication categorizes more than 350 combinations for recording parameters such as ac and dc signals, temperature, RH, pressure, wind velocity, and process control variables. It also lists many accessories and options, as well as a selection of chart paper.

Rustrak Instruments, Route 2 and Middle Rd, East Greenwich, RI 02818.

Circle No 464

Brochure focuses on Unix-based software

The vendor's 16-pg brochure discusses Monitrol, a Unix-based software-design framework for the implementation of a computer-integrated manufacturing information system. The publication explains how the system incorporates industry standards, such as 802.3 net-



working, x-windows, and an SQL database, for protection against obsolescence. It also describes the system's real-time database, which features process graphics, alarm logging, report and data entry screens, statistical control charting, historical data storage, and security management.

Hilco Technologies, 3015 S Brentwood, St Louis, MO 63144.

Circle No 465

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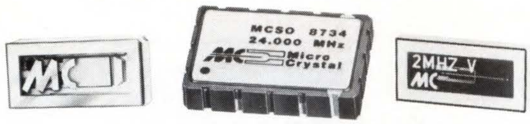

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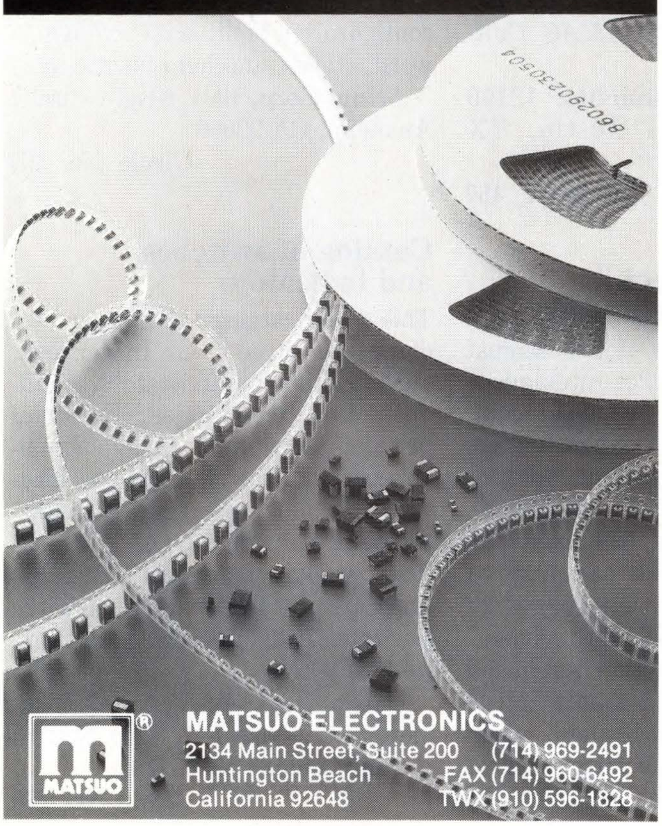

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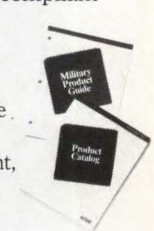

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- 16-bit cascadable ALU, with 26ns. flow-through add time.
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- Implements add, subtract, accumulate, two's complement, pass and logic operations.

16-bit multiplier LMU18

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32-bit barrel shifter/normalizer LSH32

- 32-input, parallel shifter with 32ns. prop. delay.
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- Separate external shift distance inputs for block floating-point applications.

12-bit multiplier-summer (AxB)+C LMS12

- 12x12 multiplier, plus 26-bit adder in one package.
- Cascadable to form 25MHz video filter with broadside coefficient load.

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CIRCLE NO 236

in. The document describes the Qualifiber coherent fiber-optic sensor that transmits the target image to a linear-array CCD chip.

Dolan-Jenner Industries Inc, Box 1020, Woburn, MA 01801.

Circle No 466

App notes address specialized applications

This series of application notes explains the uses of the vendor's LabView instrumentation and analysis software system. The documents cover subjects ranging from data-flow programming and arrays to block-diagramming techniques and using specific instrument drivers. The six notes currently available are titled *Dataflow Programming with LabView,* 320117-01; *An Introduction to Arrays with LabView,* 320122-01; *Using Arrays with LabView,* 320118-01; *Methods of Block Diagramming with LabView: Two Ways to Convert a Fortran Program to a G Program,* 320119-01; *Shift Registers in LabView,* 320121-01; and *LabView Instrument Drivers with the KineticSystems 3988 CAMAC Controller,* 320124-01.

National Instruments, 12109 Technology Blvd, Austin, TX 78727.

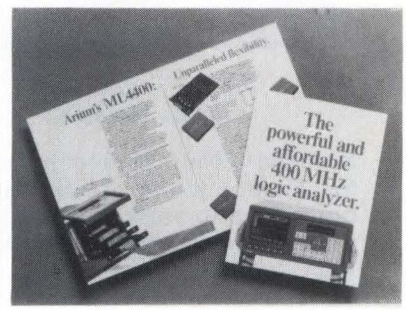
Circle No 467

Letter keeps track of artificial intelligence

The feature article of the August 1988 issue of Artificial Intelligence Letter is entitled "Unilever combines videodisc with expert system to produce maintenance advisor with high resolution;" it reports on how one company has used the enormous database capacity of video disks to present pages of manuals, still photos, and "movies." The Viewpoints section published the second part of a 2-part article by Dr Bruce E Flinchbaugh, which discusses the field of image understanding. Finally, the AI Briefs section provides a calendar of artificial intelligence conferences and events in August.

Texas Instruments, Data Systems Group, Box 2909, M/S 2222, Austin, TX 78769.

Circle No 468



Booklet presents logic analyzer

A 4-color brochure covers the ML4400 400-MHz logic analyzer. It mentions the analyzer's user-selectable input cards for simultaneous analysis of as many as four individual 8-, 16-, and 32-bit µPs. Screen photos in the publication show timing, state-disassembly, trigger-sequence, 400-MHz timing, configuration, split-screen, trigger-word, status, and help functions.

Arium Corp, 1931 Wright Circle, Anaheim, CA 92806.

Circle No 469

Catalog of switches and indicators

This 47-pg catalog takes stock of a complete line of indicators, switches, switch/indicators, readouts, and accessories. Its brief product descriptions include actual-size outline drawings and specifications for mounting configurations, temperature ranges, voltage readings, product materials, lamp options, panel thicknesses, and switch contacts. It also describes customized switches.

Eaton Corp, Aerospace & Commercial Controls Div, 4201 N 27th St, Milwaukee, WI 53216.

Circle No 470

LITERATURE

Report on use of Envex in vacuum applications

Application Report #12 elucidates the high-vacuum, high-temperature performance of bearings and structural insulation blocks made of Envex polyimide. The first application it describes is the development of a bearing for the ion-beam monitor of a heavy ion accelerator. In the second application, it discusses the development of electrical insulation blocks for a collector ring surrounding the wafer platform of thin-film ion-etching equipment. Photographs illustrate the text of the report.

Rogers Corp, 1 Technology Dr, Rogers, CT 06263.

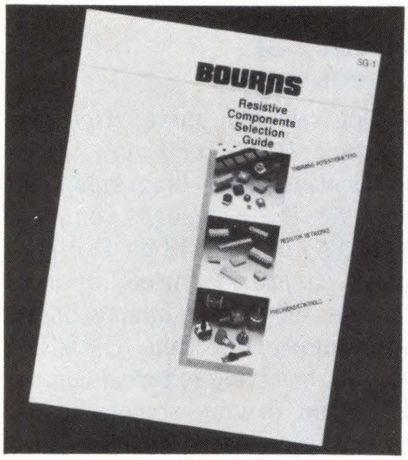
Circle No 471

Software and technical information for board design

The Easy program provides technical information and software that makes designing and implementing Multibus II boards easier. The package has five parts: the Multibus II transport-protocol specification and an accompanying guide that defines a set of services based on the message-passing coprocessor; the Multibus II interconnect specification, which details the use of the address spaces used in board identification and configuration; the Multibus II initialization and diagnostics specification; an application note, *Designing a Multibus II Central Services Module;* and the Multibus II interconnect design guide, which includes a software template to implement the vendor's version of interconnect address space.

Intel Corp, Literature Dept GR1-50, Multibus II Easy Program W476, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle No 472



Publication simplifies component selection

The manufacturer's compact 16-pg catalog provides an easy-to-use selection guide for users of resistive components. It lists the latest specifications and applications for trimming and precision potentiometers, panel controls, resistor networks, and chip resistors. The booklet is arranged according to component types, and it provides schematics where appropriate. It also includes information about digital contacting encoders and stepped attenuators, which are recent additions to the manufacturer's line of products.

Bourns, 200 Columbia Ave, Riverside, CA 92507.

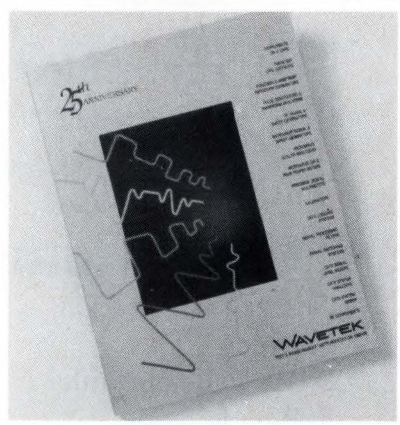
Circle No 473

Communications equipment for IBM PC/AT and PS-2

Divided into sections according to product category, the company's Fall/Winter 1988 catalog presents data-acquisition and industrial-control products, communications boards, waveform-synthesizer boards, IEEE-488 boards, and power-control boards for the IBM PC/AT and PS-2. Each product section contains the product's features, description, a product diagram, specifications, and information pertinent to the type of product being discussed. General information and a list of international distributors complete the publication.

Qua Tech Inc, 478 E Exchange St, Akron, OH 44304.

Circle No 474

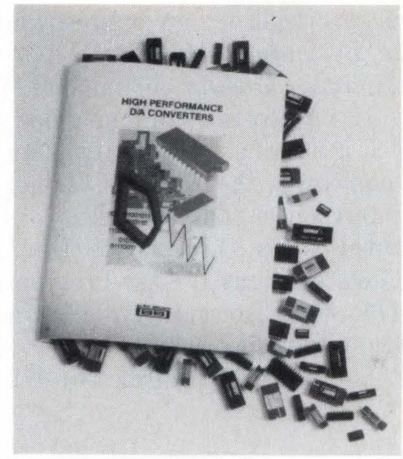


Test and measurement instruments cataloged

The 1988-1989 Test & Measurement Instrumentation catalog provides descriptions, technical specifications, illustrations, prices, and ordering information for the vendor's line of signal sources, measurement equipment, and related special equipment and components. Some of the equipment listed includes instruments on a card, WaveTest IEEE-488 software, pulse generators, and microwave scalar analyzers. The publication previews the 25 most recent products and features several introductory sections. It also includes 16 selection guides, product and model number indexes, and descriptions of customer support services.

Wavetek Corp, Box 85434, San Diego, CA 92138.

Circle No 475

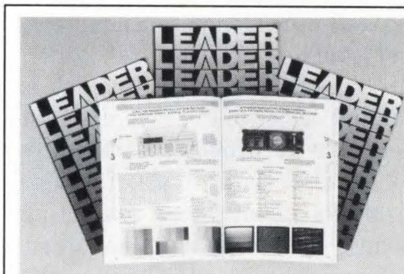


Selection of D/A converters

An 8-pg selection guide, *High Performance D/A Converters,* gives specifications, pin diagrams, and prices for the company's complete line of 12-, 16-, and 18-bit D/A converters. It provides useful application tips on wiring management, power-supply selection, EMI/RFI isolation, selecting external components, and driving remote loads. The DAC glossary summarizes such terms as integral linearity error, monotonicity, and unipolar zero-error.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734.

Circle No 476

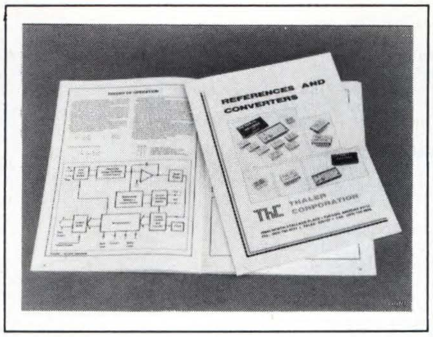


Test and measurement instruments classified

This 4-color catalog describes the vendor's test and measurement instruments. Designed to answer many of the customer's questions, the 96-pg book has photos and specifications for more than 100 products, including 15 new instruments. It also contains a glossary of oscilloscope terms and application notes on such subjects as digital and analog oscilloscopes, video products, programmable RGB video generators, and frequency counters.

Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788.

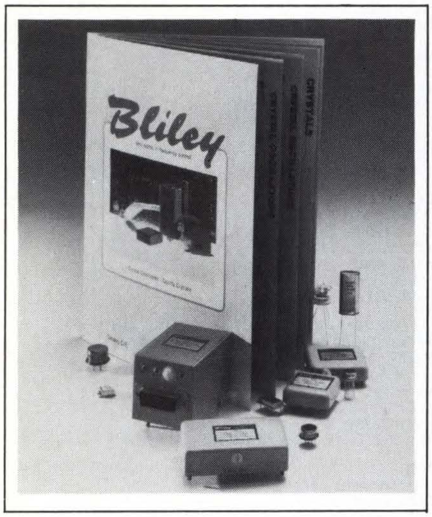
Circle No 477



specifications and performance curves. Selection guides, application notes, price information, and an explanation of quality-assurance processing complete the publication.

Thaler Corp, 10940 N Stallard Pl, Tucson, AZ 85737.

Circle No 479



Crystal oscillators and quartz crystals listed

The vendor's catalog presents its high-reliability crystal oscillators and quartz crystals. The 12-pg booklet notes performance specifications for more than 50 units. The variety in the crystal oscillator section includes oven oscillators and a digitally compensated crystal oscillator, as well as voltage-controlled, temperature-compensated voltage-controlled, and clock oscillators. The quartz-crystal section contains surface-mount designs and SC-cut units among general-purpose, MIL-Spec, vacuum-sealed, and ultra high-stability components.

Bliley Electric Co, Box 3428, Erie, PA 16508.

Circle No 478

Listing of ADCs and "references"

The vendor's 64-pg catalog covers its line of voltage references, sine-wave references, and A/D converters. Data sheets provide electrical

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275 Washington St
Newton, MA 02158
(617) 964-3030

BUSINESS/CORPORATE STAFF

Peter D Coley
VP/Publisher
Newton, MA 02158
(617) 964-3030; Telex 940573
Ora Dunbar, Assistant/Sales Coordinator

Deborah Virtue
Business Director
Newton, MA 02158
(617) 964-3030

Mark J Holdreith
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
Heather McElkenny, Assistant

NEW ENGLAND
John Bartlett, Regional Manager
Chris Platt, Regional Manager
199 Wells Ave
Newton, MA 02159
(617) 964-3730

STAMFORD 06904
George Isbell, Regional Manager
8 Stamford Forum, Box 10277
(203) 328-2580

NEW YORK, NY 10011
Daniel J Rowland, Regional Manager
249 West 17th St
New York, NY 10011
(212) 463-6419

PHILADELPHIA AREA
Steve Farkas, Regional Manager
487 Devon Park Dr, Suite 206
Wayne, PA 19087
(215) 293-1212

CHICAGO AREA
Clayton Ryder, Regional Manager
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3031 Tisch Way, Suite 100
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LOS ANGELES 90064
Charles J Stillman, Jr
Regional Manager
12233 W Olympic Blvd
(213) 826-5818

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Jim McErlean, Regional Manager
18818 Teller Ave, Suite 170
Irvine, CA
(714) 851-9422

PORTLAND, OREGON 97221
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UNITED KINGDOM/BENELUX
Jan Dawson, Regional Manager
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SCANDINAVIA
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Telex: 914911; FAX: 01-628 5984

FRANCE/ITALY/SPAIN
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WEST GERMANY/SWITZERLAND/AUSTRIA
Wolfgang Richter
Sudring 53
7240 Horb/Neckar
West Germany
49-7451-7828; Telex: 765450

EASTERN BLOC
Uwe Kretzschmar
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London EC2A 4JU UK
01-628 7030
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FAR EAST
Ed Schrader, General Manager
18818 Teller Ave, Suite 170
Irvine, CA 92715
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PRODUCT MART
Joanne Dorian, Manager
249 West 17th St
New York, NY 10011
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CAREER OPPORTUNITIES/CAREER NEWS
Roberta Renard, National Sales Manager
(201) 228-8602

Janet O Penn, Eastern Sales Manager
(201) 228-8610
103 Eisenhower Parkway
Roseland, NJ 07068

Mary Beth West, Western Sales Manager
18818 Teller Ave., Suite 170
Irvine, CA 92715
(213) 826-5815

Staci Comstock, Sales Assistant
(201) 228-8608
FAX: 201-228-4622

Wendy A Casella, *Advertising/Contracts Coordinator*
Nan E Coulter, *Advertising/Contracts Coordinator*
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William Platt, Sr, Vice President, Reed Publishing USA

Cahners Magazine Division
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A challenge to designers: Create usable products

The Psychology of Everyday Things, by Donald A Norman. 257 pgs; $19.95. ISBN 0-465-06709-3. Basic Books Inc, NY, NY, 1988.

Steven H Leibson,
Regional Editor

Electrical engineers rarely receive training in the art of designing products that people can use. As a result, consumers buy VCRs they can't program and business telephone systems that tie communications in knots. In his book *The Psychology of Everyday Things*, Donald A Norman tries to correct that educational omission. He lays the blame for hard-to-use products squarely on bad design. Even though the circuitry inside a product may perform perfectly, if the product can't be used by its consumer, the design is flawed.

Norman should know. He's director of the Institute for Cognitive Science at the University of California at San Diego, where he's also a professor. He holds a degree in electrical engineering from MIT, and he spent a half year at MCC, the Microelectronics and Computer Technology Corp (Austin, TX).

In the first few chapters of the book, Norman explores the ways that people interact with objects. He covers such topics as short- and long-term memory and mapping, which is the way we build conceptual models of the relationships between controls and the results they produce, however accurate or inaccurate those models may be. As a designer, writes Norman, you must accommodate human foibles.

The final chapters of the book challenge you to create usable, intuitive designs—or, as Norman puts it, "user-centered designs." Throughout the book, Norman sprinkles excellent, often humorous, examples of products that illustrate his thesis. Some, such as office telephones and VCRs, relate directly to the electrical engineer's trade. Others, such as a simple door or a water faucet, give valuable examples of good and bad design in everyday objects. These examples make the book a practical guide to good design and not just an esoteric discussion of the war between humans and machines.

In seven short chapters, Donald A Norman provides a sound basis for good product design from a user's perspective. The book takes very little time to read, but you'll need years to assimilate and implement the ideas he presents. However, if you accept and use these ideas, you may very well gain that intangible edge that allows some engineers to design great products while the rest merely perpetuate mediocrity. EDN

CAREER OPPORTUNITIES

1988 Editorial Calendar and Planning Guide

EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Oct. 27	Oct. 6	CAE, Computers & Peripherals, Integrated Circuits, Wescon '88 Show Preview	
Nov. 10	Oct. 20	Programmable Logic Devices, Integrated Circuits, Test & Measurements, Wescon '88 Show Issue	Closing: Oct. 27 Mailing: Nov. 17
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	

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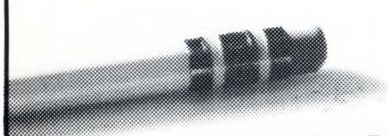

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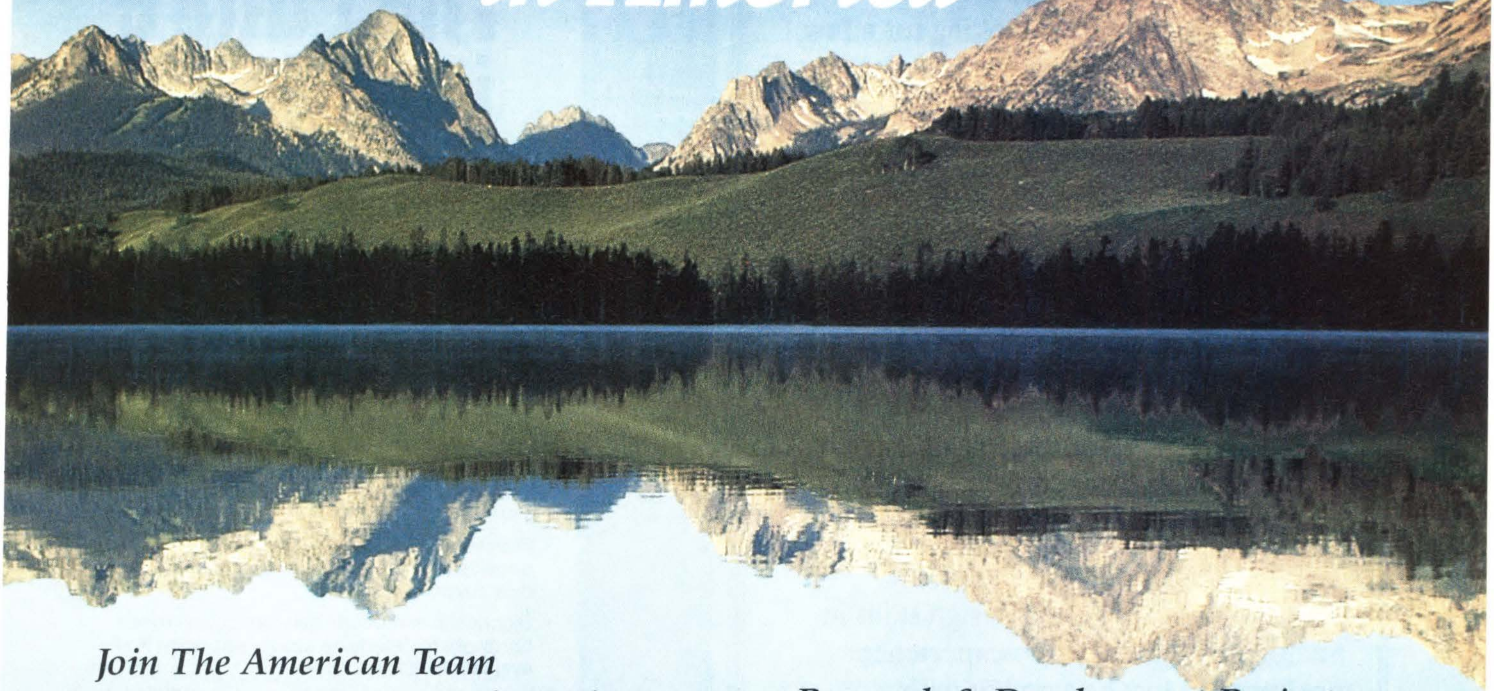

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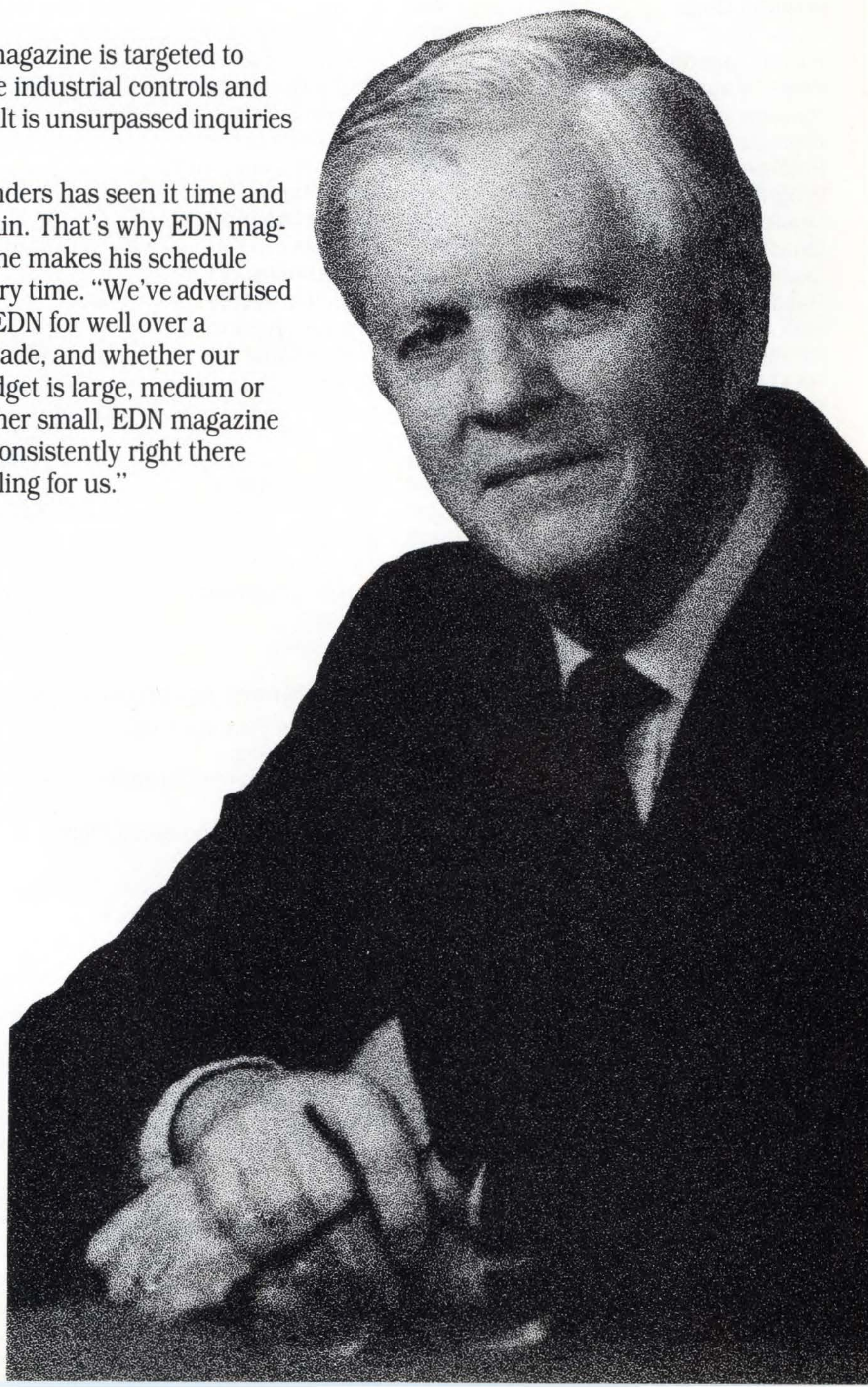

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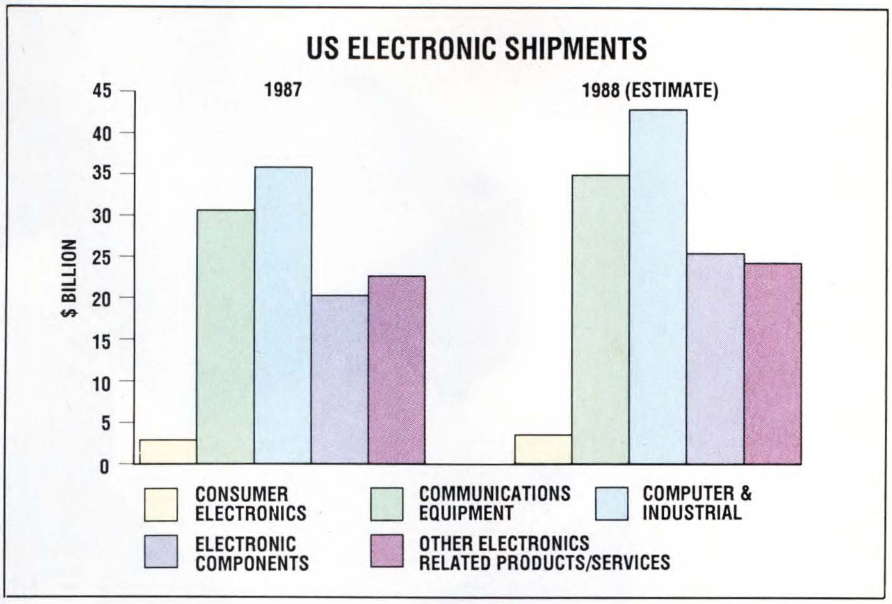
LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

US electronics shipments up 16% in first half of 1988



Total US electronic shipments reached $125 billion for the first half of this year, up 16% from the $107 billion figure for the same period in 1987, according to the Electronics Industries Association (Washington, DC). The association said that a number of factors contributed to this healthy growth rate, including increased exports of electronic products and the general performance of the US economy as a whole.

When analyzed according to industry-group category, both the electronic-component sector and the computer and industrial electronics sector had growth rates of more than 20%. Electronic-component shipments for the first half of the year totaled $24.2 billion, up from a 1987 figure of $20.1 billion. Computers and industrial electronics registered $41.3 billion; the 1987 number was $34.3 billion.

Sales of consumer electronics amounted to approximately $3.2 billion for the first half of 1988; the first six months of 1987 brought sales of $2.7 billion in this sector. The communications equipment sector increased its sales by 11% in the first half of this year. This sector accounted for $33.2 billion in sales compared to a 1987 6-month figure of $29.9 billion.

Other electronic products and services make up the fifth and last sector in EIA's analysis. This area turned in sales for the first half of 1988 that totaled $23.1 billion, up 10.5% from the $20.9 billion reported for the same period last year.

3½-in. flexible drives to claim 82% of 1992 market

ESTIMATED UNIT DEMAND FOR FLEXIBLE-DISK DRIVES (PERCENT OF WORLD MARKET)

	1987	1988	1989	1990	1991	1992
3½-IN.	38%	44%	58%	68%	76%	82%
5¼-IN.	62%	56%	42%	32%	24%	18%

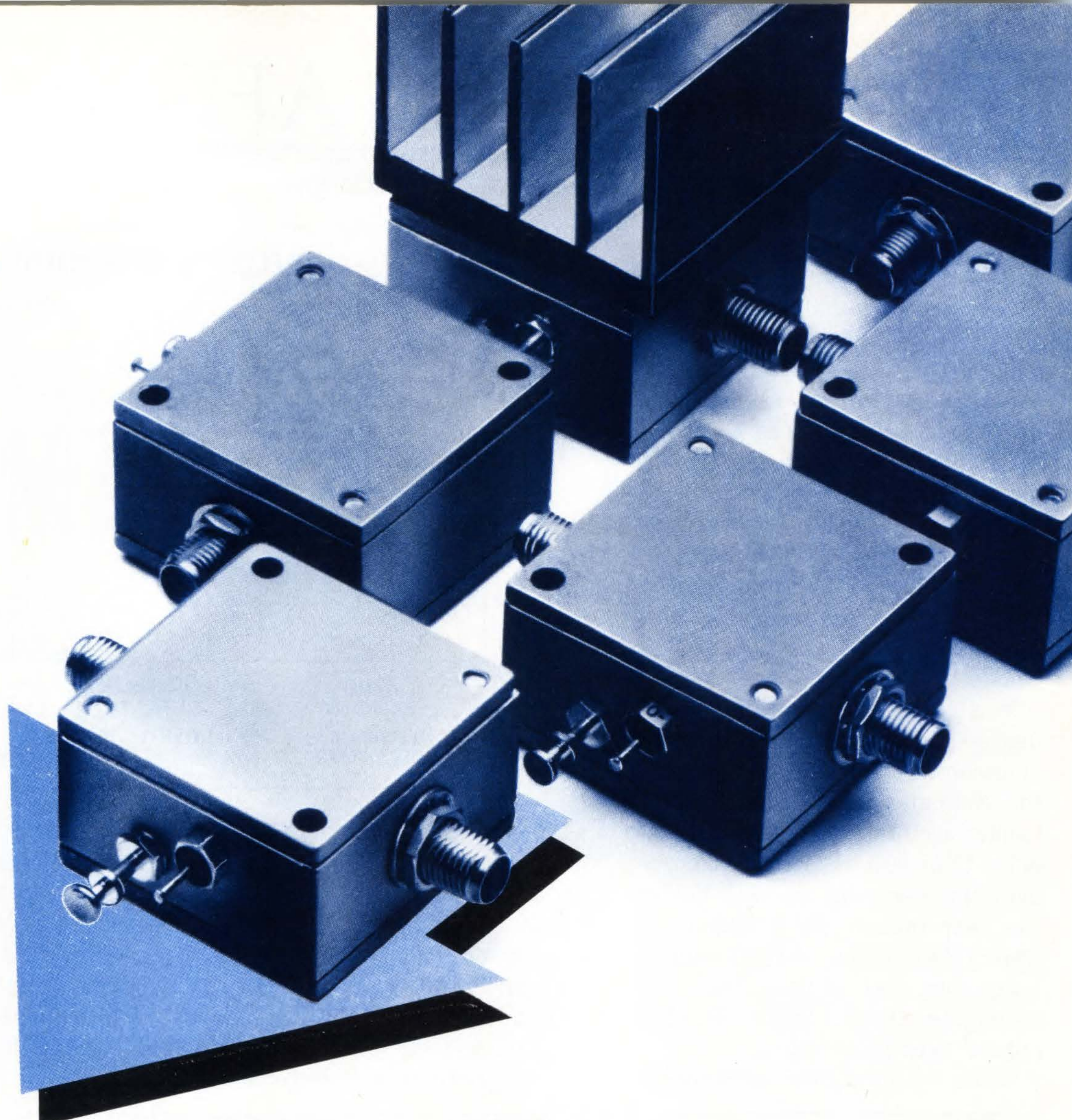
NOTE:
SHIPMENTS OF 8-IN. FLEXIBLE-DISK DRIVES ARE CONSIDERED TO BE NEGLIGIBLE.

(SOURCE: DATAQUEST INC)

Inspired by IBM's endorsement of the 3½-in. format, the market for 3½-in. flexible-disk drives is booming, and the boom will continue, according to Dataquest Inc (San Jose, CA). In 1987, 3½-in. flexible-disk drives accounted for just 38% of the market; 5¼-in. drives claimed the 62% majority. (Dataquest considered shipments of 8-in. drives to be negligible for the purposes of this study). The crossover point in worldwide market share should occur in 1989 when 3½-in. drives will gain 58% of the market; by 1992, those drives will have a full 82% of the market. By April of this year, 23 computer companies were offering 63 models containing 3½-in. flexible-disk drives.

Dataquest predicts that the ratio of computer shipments to flexible-disk-drive shipments will decline to somewhere between 1:1.4 to 1:1 (worst case) within the next five years. For worldwide computer shipments of 18 million units this year, the market research firm estimates shipments of 25 million flexible-disk drives. In 1992, for 28 million computer units, the worst case would be 28 million flexible-disk drives—the best case would register 39 million drives shipped. Although the drop in the ratio seems to reflect a negative trend, the upward movement in the computer market will probably more than offset that trend.

Prices should drop significantly in the next few years. This year, the average factory selling price for 3½-in. flexible drives is $56 (5¼-in. drives cost about the same). By 1990, a 3½-in. flexible-disk drive purchased from the factory should cost about $49. The price should drop another $5 by 1992 to $44.



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MODEL	FREQUENCY MHz	GAIN, dB (min.)	MAX. POWER OUTPUT dBm(typ)	NF dB(typ)	PRICE $ Ea.	Qty.
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ZFL-500LN	0.1-500	24	+5	2.9	79.95	1-24
ZFL-750	0.2-750	18	+9	6.0	74.95	1-24
ZFL-1000	0.1-1000	17	+9	6.0	79.95	1-24
ZFL-1000G*	10-1000	17	+3	12.0	199.00	1-9
ZFL-1000H	10-1000	28	+20	5.0	219.00	1-9
ZFL-500HLN	10-500	19	+16	3.8	99.95	1-24
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95	1-24
ZFL-1000VH	10-1000	20	+25	4.5	229.00	1-9
ZFL-2000	10-2000	20	+17**	7.0	219.00	1-9

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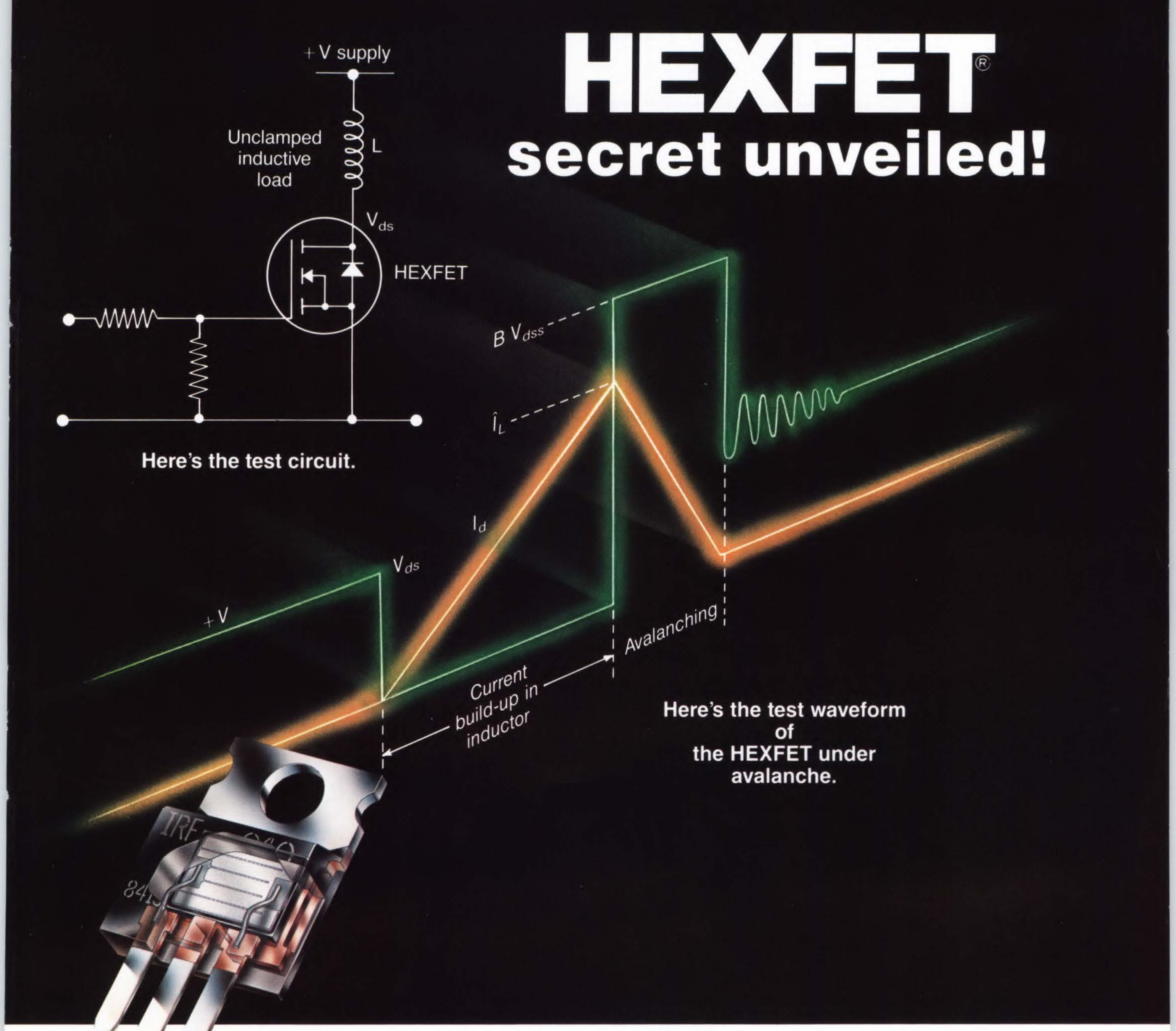

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