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SEPTEMBER 29, 1988

EDN®

Industrial electronics product showcase

Use Spice techniques to analyze feedback circuits

Color-palette chips

Laser diodes

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

EDN's DSP benchmarks can augment your chip-evaluation process

rship that works.

In today's highly competitive marketplace, it takes more than technology and tools to meet your ASIC needs. It takes a long-term partner you can count on. One who's ready to help you turn your hot idea into an even hotter new product.

At Fujitsu Microelectronics, we believe that the only way we can achieve our goals is to help you achieve yours. So we've committed our technical, financial and human resources to providing you with the ASIC technology, tools and trust you need to meet your objectives. From design support through volume production of your advanced VLSI ICs. The heart of your new products.

When you shake hands with Fujitsu, you get more than just a business deal. You get the industry's most experienced volume producer of ASIC devices as a working partner.

We become an extension of your ASIC design team, providing you with a nationwide network of field application and technical resource engineers, ready to offer local technical support on both products and tools.

You also get ASIC sales and marketing support to help you smooth out all the administrative wrinkles.

Plus coast-to-coast technical resource centers, fully equipped with easy-to-use design tools. And local training and twenty-four hour design facilities, so you can work whenever inspiration strikes.

All supporting the most advanced process and manufacturing technologies in the industry, including CMOS, ECL, BiCMOS and LSTTL.

All of which is structured for the fast design input-to-prototype turnaround, design security and timely delivery of volume production you need to get to market faster.

It all adds up to a partnership that works. Which, after all, is everything an ASIC partner should be.

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Everything an ASIC partner should be.

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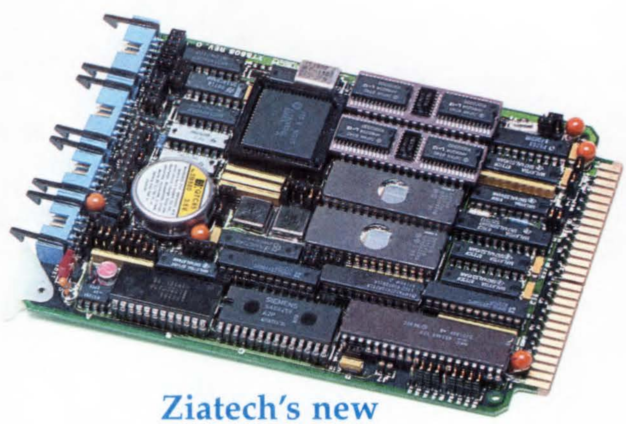
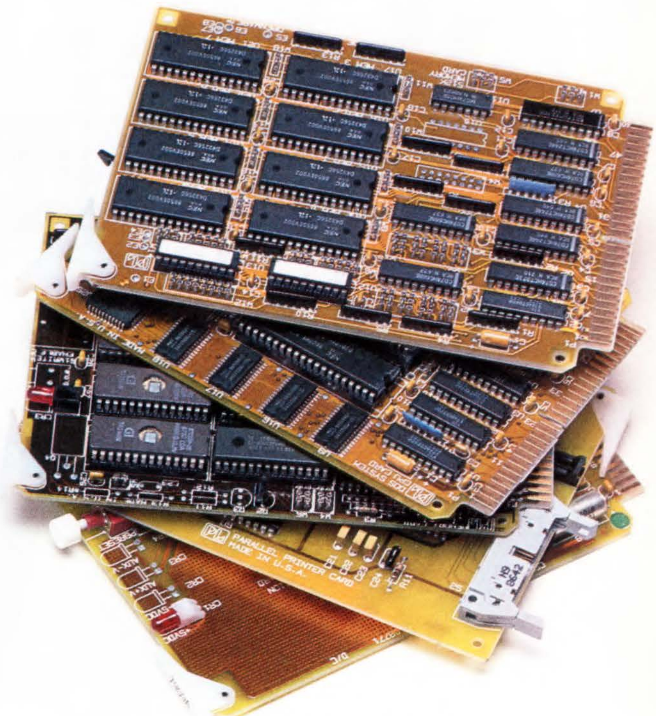
You need a partne

When it comes to ASICs, you need more than technology that works.

Less is More.



Ziatech's new
STD Bus ZT 8809
Single Board System
for OEM applications.



Another manufacturer's
"function-per-board"
STD Bus card set
with equivalent capability.

- **PERFORMANCE** (NEC V20 at 8 MHz clock speed)
- **ON-BOARD MEMORY** (520K)
- **IBM PC HARDWARE COMPATIBILITY**
- **ON-BOARD I/O** (2 serial: COM1, COM2; 1 Centronics: LPT1)
- **DEVELOPMENT CAPABILITY** (industry acclaimed Virtual System Console)
- **OPERATING SYSTEM OPTIONS** (STD DOS, VRTX, Multi-DOS, and more)
- **COMPACTNESS** (one board implementation)
- **RELIABILITY** (fewer connectors, components, boards)
- **VALUE** (Ziatech's single board system is $630 **less** than the 5-board set pictured above*)

To learn **more** about how **less** (Ziatech's new single board system) is **more** (when compared to the 5–board set pictured above), call Ziatech at **805-541-0488**. We'll send you a detailed comparison and all the technical data you'll need.

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ITT Telex 4992316
Fax (805) 541-5088
Telephone (805) 541-0488

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* Prices are according to manufacturers' literature as of 1/88.

MEMBER STDMG STD MANUFACTURER'S GROUP

WHY VTC? ASK THE VME CONSORTIUM.

"For a bunch of companies that don't always agree on everything, we sure were unanimous on VTC."

The VME Consortium needed an economical, yet highly functional VME bus interface chip, to minimize design time . . . and to help raise the VME standard to higher levels.

"We looked at the leading suppliers," said Joe Ramunni, consortium chairman (and president of Mizar), "and VTC came out on top. Their CMOS standard-cell ASIC approach gave us the high drive capability we needed, optimized for bus interfacing. And, it proved much more cost-effective, with higher performance, than gate array technology."

The VME Consortium is made up of such firms as Plessey Microsystems, Omnibyte Corporation, Mizar Inc., Ironics Inc., Heurikon Corporation, Matrix Corporation, and Clearpoint Inc., among others. What did they look for in a supplier?

"We needed a credible business partner," said Ramunni, "with a proven track record, who could provide a turnkey package . . . both design and fab. A supplier that could produce in quantity, and provide technical support to the market at large.

"We also needed a firm with an international marketing structure, because we expect this chip to be the de facto standard worldwide.

"But, we needed *people* we could work with, too. VTC had the right 'comfort factor'."

Jack Regula, consortium technical director (and VP-R&D, Ironics) added: "Our requirements for high speed, high gate-count, low power consumption, and VME bus drive capability were all met well with VTC's 1-micron CMOS standard cell library. And we were extremely impressed with VTC's facilities, its people, and its customer list."

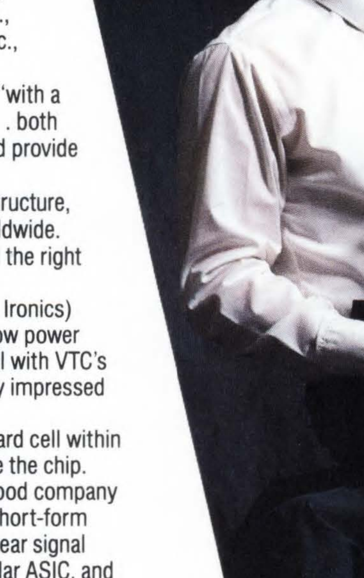
In the future, the VME bus chip (VIC) will become a standard cell within VTC's CMOS library, to allow customers to further customize the chip.

Shouldn't you be getting to know VTC, too? You'll be in good company when you do. Call or write us today, and we'll send you our short-form product catalog, which describes our product offerings in linear signal processing, high-speed CMOS logic, mass storage ICs, bipolar ASIC, and CMOS ASIC.

VTC Incorporated, 2401 East 86th Street, Bloomington, MN 55420. (In Minnesota, 612/851-5200.) Telex 857113.

CALL 1-800-VTC-VLSI

Joseph Ramunni, chairman (left), and Jack Regula, technical director, VME Technology Consortium.



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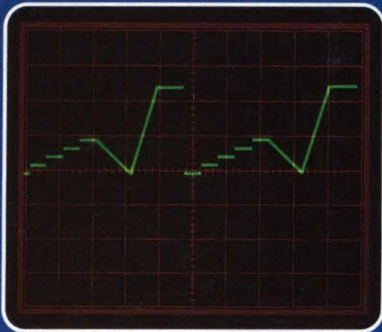
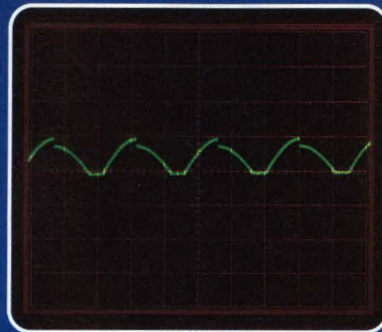
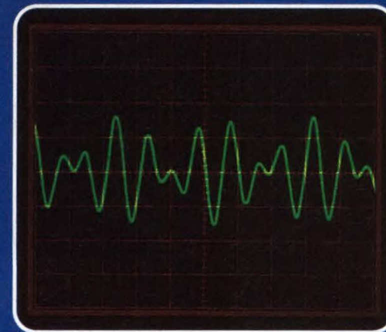


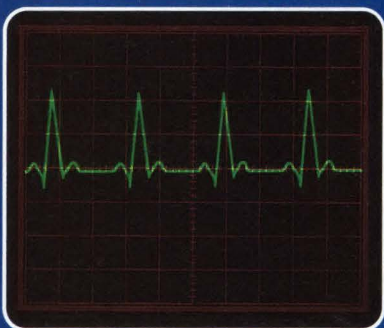
Vibration analysis with stop and hold.



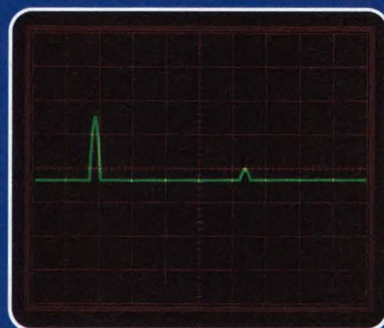
Complex waveforms for servo drives.



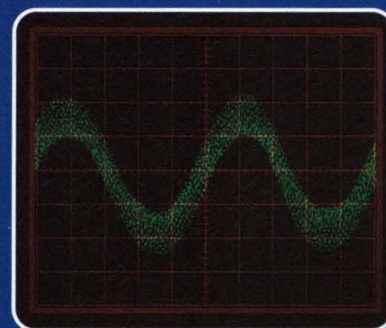
Dual tones for telephone testing.



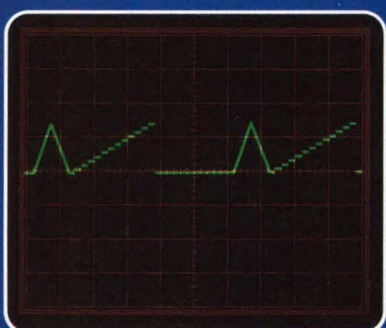
EKG and hemodynamic waveforms.



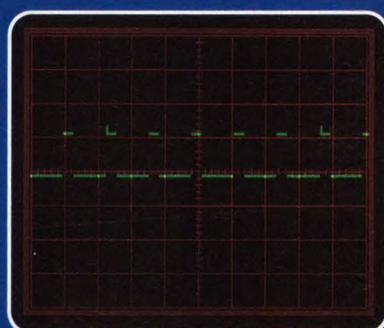
Radar/sonar envelope simulation.



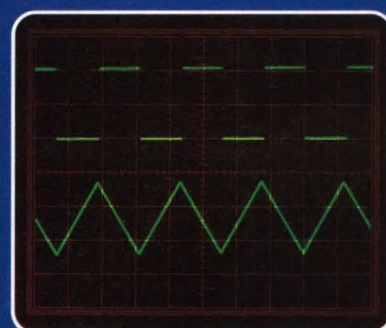
Noise added to any waveform.



A/D, amplifier development and calibration.



Digital testing and troubleshooting.



Standard waves at the push of a button.

We've been making waves for 25 years. Now it's your turn.

A quarter-century ago, Wavetek brought you the first waveforms produced by a solid-state function generator. Now our Model 75 Arbitrary Waveform/Function Generator puts you in control.

Model 75 lets you generate waveforms without entering x/y coordinates. Thumbtack and rubberband modes allow easy development and editing of any waveform. There are also nine standard functions which you can use at the push of a button.

Waveforms are stored in nonvolatile memory, with more than 4,000 vertical points and 8,000 horizontal points of resolution. They can be played back at any rate, up to 500ns per point.

By linking two or more Model 75's together, you can superimpose waveforms to introduce phase displacement or other special effects. And at the low price of $2295, you might want to buy several.

For literature or to arrange an amazing demonstration, call or write Wavetek San Diego, Inc., P.O. Box 85265, San Diego, CA 92138. Phone (619) 279-2200; TWX (910) 335-2007.

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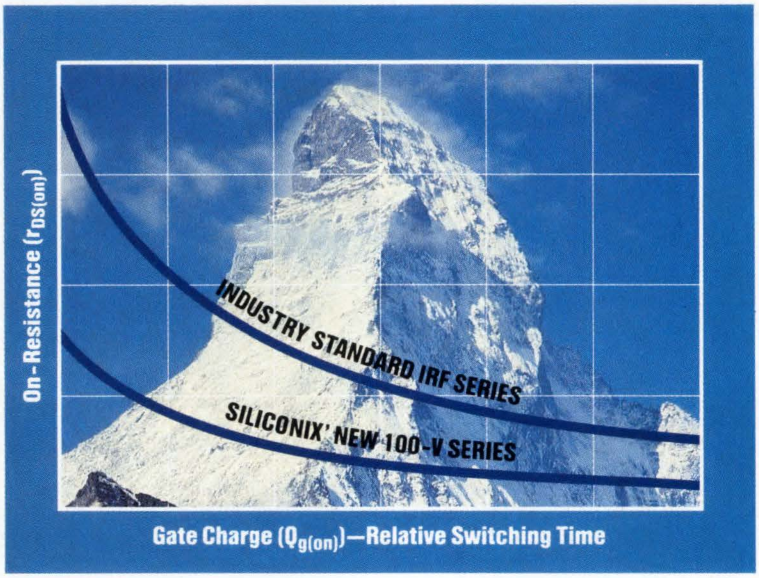
Record highs and lows for DC/DC converters.



Swiss National Tourist Office

New 100 V MOSPOWER switching transistors deliver the highest current rating and lowest $r_{DS(on)}$ for cooler power supplies.

The Siliconix forecast for power supply design is one of record high current ratings and switching speeds combined with record low $r_{DS(on)}$.

Our new family of rugged 100 V MOSPOWER devices lowers operating temperature, shrinks package size, reduces part count and increases system functionality. Now you can use smaller heatsinks and eliminate external components such as snubbers and voltage clamps. The result—a more power efficient DC/DC converter and a more reliable, cost-effective power supply design.

PART NUMBER	PACKAGE	$r_{DS(on)}$	I_D	I_{AR}
SMM70N10	TO-3	25mΩ	70A	70A
SMP40N10	TO-220	40mΩ	40A	40A
SMP30N10	TO-220	60mΩ	30A	30A

These 100 V MOSPOWER devices are ideally suited to switching transistor applications in DC/DC converters for power supplies and military products. In addition, they are excellent for solid state relay applications in automotive products and switching transistors in battery powered vehicles.

All of these Siliconix MOSPOWER devices are produced in our Class I wafer fab and they are 100% UIS (Avalanche) tested. Get record breaking performance. Dial our toll-free hot line now! **Call 1 (800) 554-5565, Ext. 941** for your free 100 V MOSPOWER Design Kit. It includes your sample and data sheets.

Siliconix
incorporated

2201 Laurelwood Road, Santa Clara, CA 95054

Volume 33, Number 20

EDN Magazine Edition

September 29, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: How a DSP IC performs in a benchmark is only one consideration in your selection process; other factors can sometimes be just as important. See pg 126. (Photo courtesy AT&T; photography by Michel Tcherevkoff)

Continued on page 7

EDN®(ISSN 0012-7515) is published 40 times a year (biweekly with 1 additional issue a month, except for July which has 3 additional issues) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Electronics/Computer Group Vice President; Jerry D Neth, Vice President/Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President/Production and Manufacturing. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. POSTMASTER: Send address corrections to EDN® at the Denver address. Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer; Robert L Krakoff, Executive Vice President; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $100/year; Canada/Mexico, $115/year; Europe air mail, $135/year; all other nations, $135/year for surface mail and $210/year for air mail. Except for special issues where price changes are indicated, single copies of regular issues are available for $6, $8, and $10 (USA, Canada/Mexico, and foreign). Please address all subscription mail to Eric Schmierer, 44 Cook Street, Denver, CO 80206-5800.

Today's laser diodes serve in fiber-to-home systems, cable TV, local-area networks, bar-code scanners, and optical disks (pg 57).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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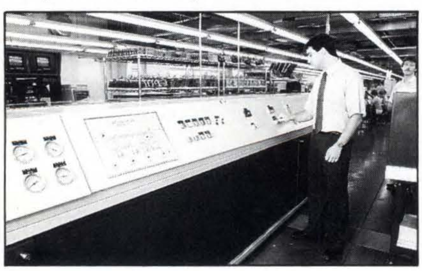

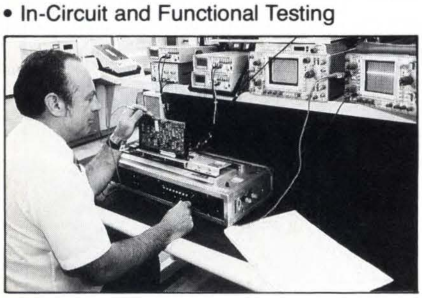

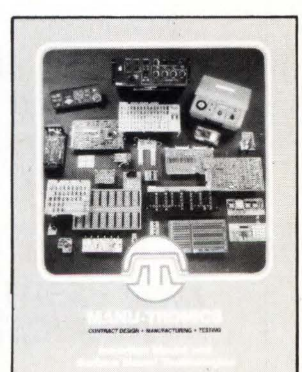

Continued from page 7


You've just assembled the "perfect" EDA system. Now it's boxing you in.
SIMULATION
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IC LAYOUT
ELECTRONIC PACKAGING

How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

It's also fast enough to finally let today's new microprocessors run at the speeds for which they were designed—breathtaking.

Raising your standard.

How fast would you like your standard logic?

How about faster than any TTL logic around? Even FAST™ or AS? You've got it with the 7.5ns PAL device.

And the fact that you can configure it yourself means you can get exactly what you want.

If you want to redesign something, you change the PAL device. Not the board.

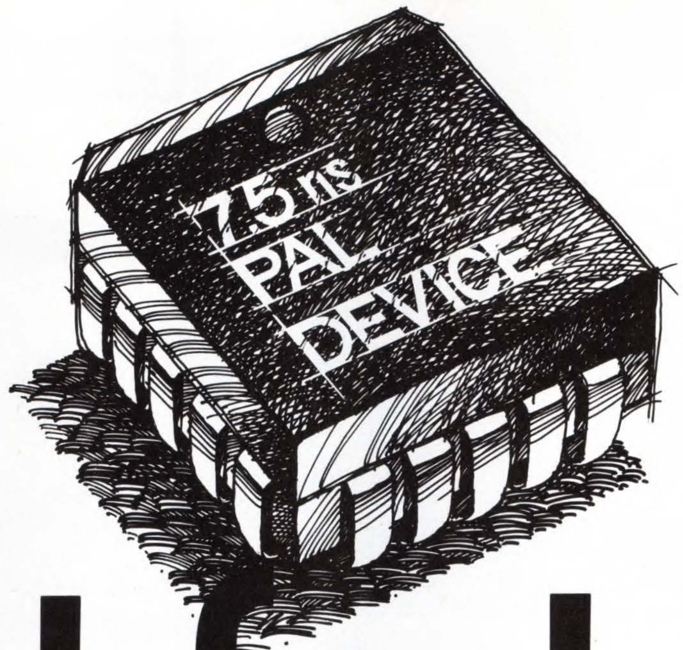
Not only is this the fastest way to get high speed logic, it's also the most practical. One 7.5ns PAL device replaces two to six standard TTL devices.

Which cuts down on board size.

And cuts down chances for a device failure.

7.5ns PAL Device vs. FAST & AS

SSI/MSI		FAST	AS	7.5ns PAL Device
Combinatorial				
74138	tPD	8.0	10.0	7.5
Decoder				
74151	tPD	11.0	15.0	7.5
Mux				
Register/Latch				
74374	tCO	10.0	9.0	6.5
Octal Register				
74373	tPD	8.0	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
Eight bit Ctr	tCO	10.0	11.0	6.5



st get faster.

What to give the microprocessor that has everything.

We suggest the first PAL device that can keep up with it.

The 7.5ns PAL device runs at 74 Mhz. It can deliver the speed the new high performance microprocessors need.

Processors like the 29K, the 386 and the 68030.

This PAL device delivers 25% more speed than any other PAL device.

We even have the fastest 22V10.

Our 15ns 22V10 runs at 50Mhz. That's 10ns faster than anyone else on the market. And it lets you run at twice the rate of the new 25Mhz microprocessors.

We've been shipping 20 pin 10ns PAL devices for eighteen months. And now you can get the new 24 pin 10ns PAL device as well.

There's plenty of service and support to get and keep your project moving. And all our fast PAL devices are available in volume when you need them. Now, for example.

For all the facts about our fast PAL devices, drop us a line. Or call us at (800) 222-9323.

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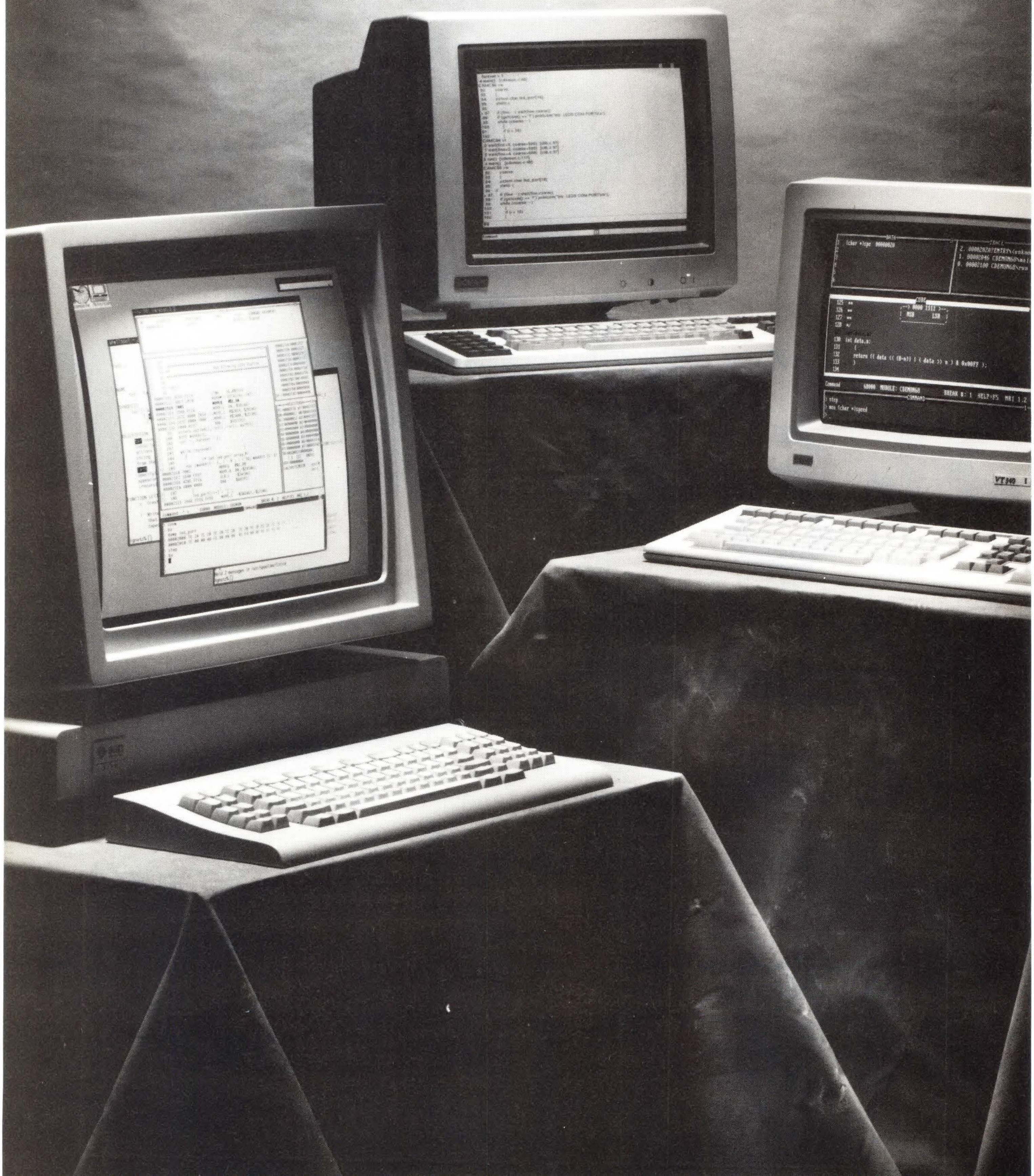
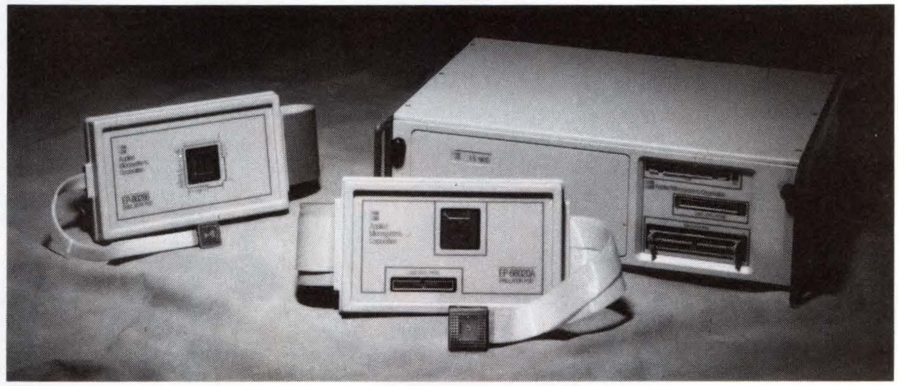


The highest performance development tools.



Our ES 1800 Series of emulators provide the most powerful transparent emulation system available anywhere.

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VAX MicroVAX Apollo Sun PC PC XT PC AT PC Compatibles	VMS ULTRIX UNIX® MS-DOS	**Intel:** 8048 family, 8051 family 8080, 8085, 8086/8, 80186/188 and 80286 **Motorola:** 68HC11, 6800/2/8, 6809/9E, 68000/08/10 and 68020 **Zilog:** Z80, Z80H, MK 3880/4 and Z8001/2 **NSC:** NSC 800 **Hitachi:** 64180	**C** **Pascal** **FORTRAN** **PL/M** **Assembler** **Jovial** **ADA (VERDIX)**	Compilers Assemblers Linkers Locators	**ES 1800** (16 & 32-bit) **EC 7000** (8-bit microcontrollers) **EM Series and** **EL 800** (8-bit microprocessors)	**VALIDATE** and other software products for source and symbolic debugging

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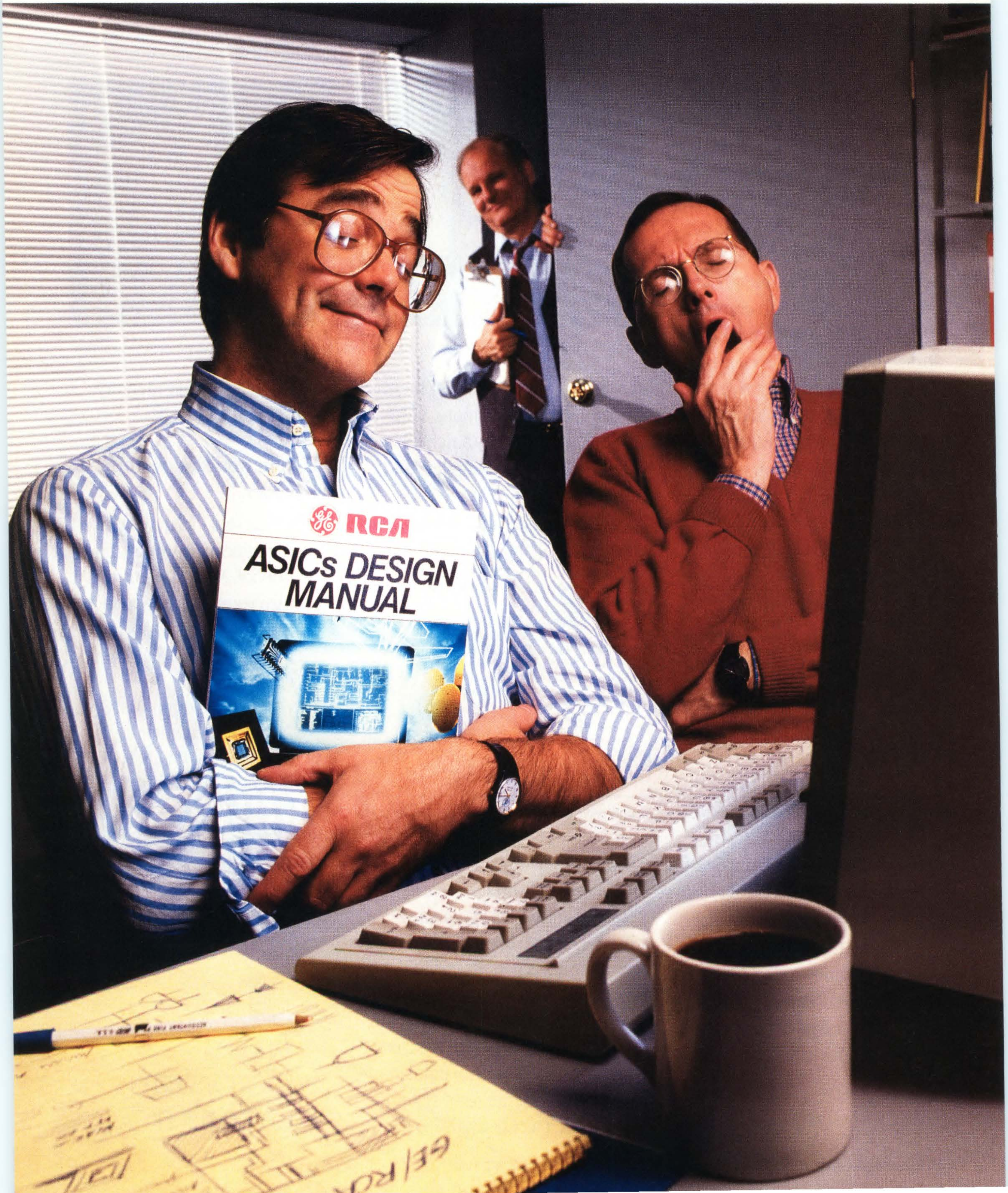
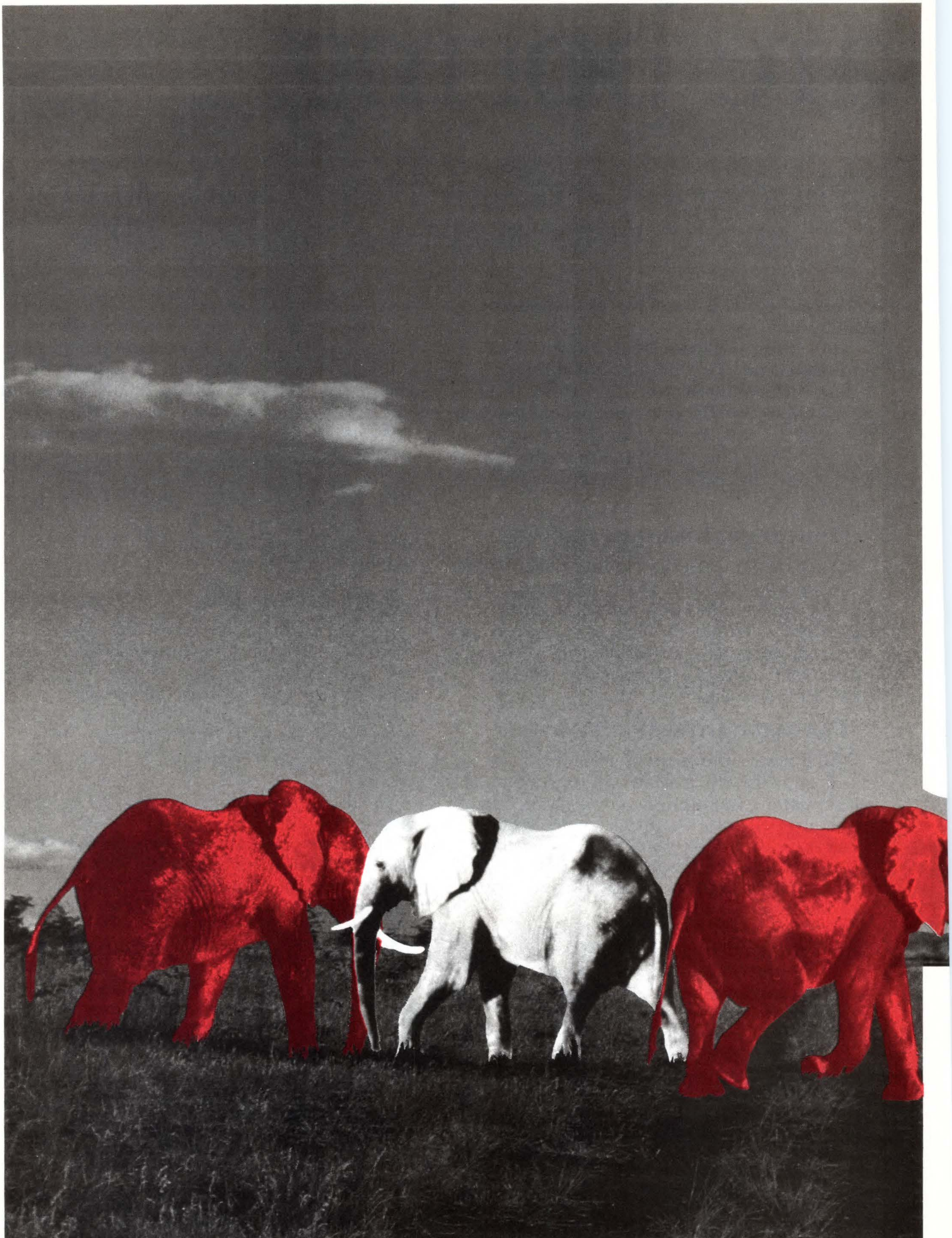
Our ASICs



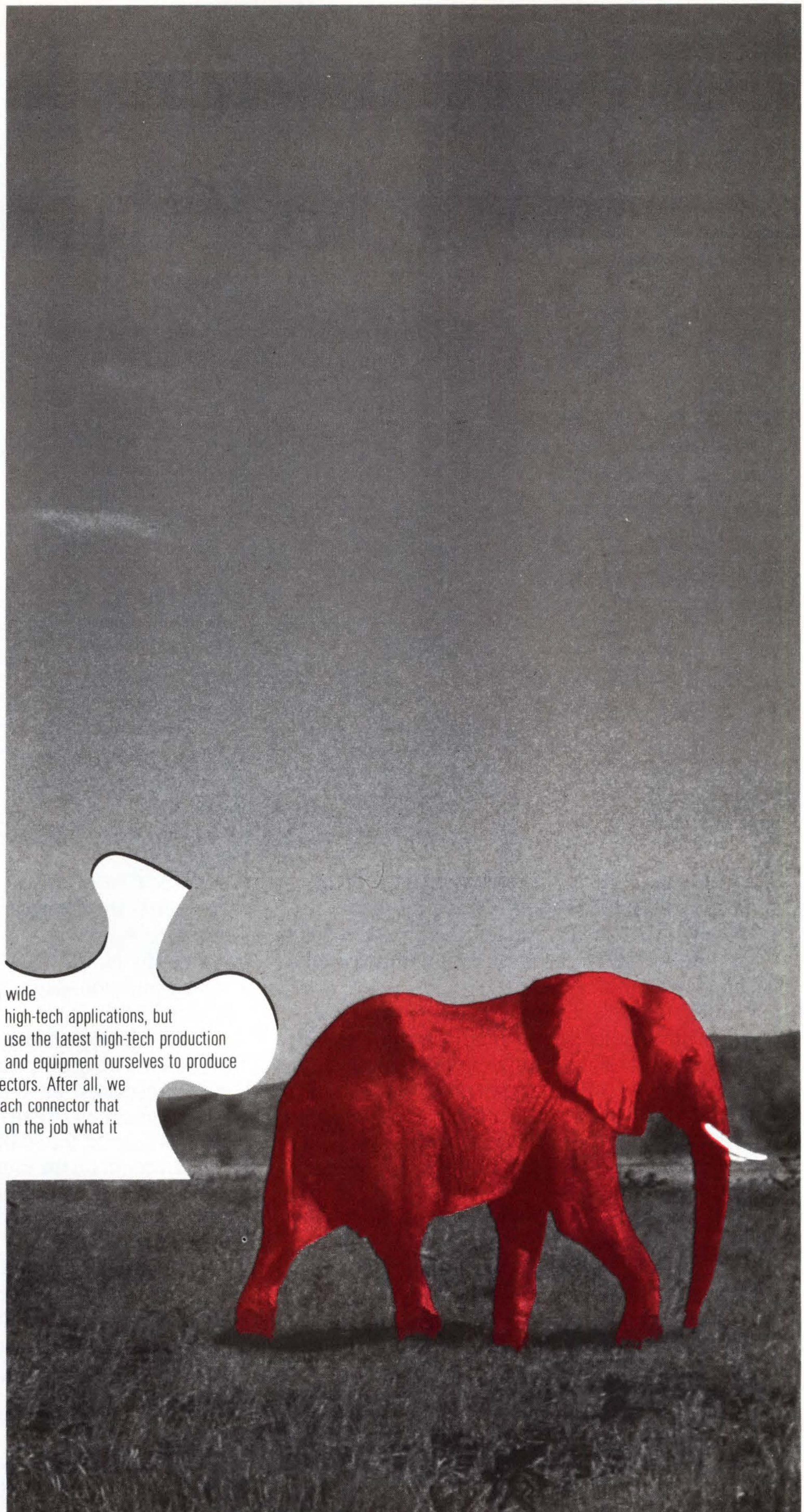


A SINGLE WHITE ELEPHANT CAN PRODUCE AN OPERATIONAL DISASTER.

Elephants may not be the smartes but hundreds or even thousands of them can link up to cover immense distances as a perfectly coordinated entity. They can do it with an efficiency that's often lacking in modern industry. Because, in nature and in industry, a single white elephant can produce an operational disaster.

That's why we at HARTING produce a complete line of connectors for virtually all applications found in the electronics industry. Electronic controls and instrumentation, telecommunications, robotized production technology and industrial automation are typical areas involving state-of-the-art technology where users of high-tech electronics equipment and systems can't afford white elephants. Especially when it comes to connectors.

HARTING's HAN® Industrial Connectors, IDC Connectors, D-Sub Connectors and PCB Connectors are all designed and engineered to cover a wide range of high-tech applications, but we also use the latest high-tech production methods and equipment ourselves to produce our connectors. After all, we make sure that each connector that leaves our plant delivers on the job what it promises on the drawing board.



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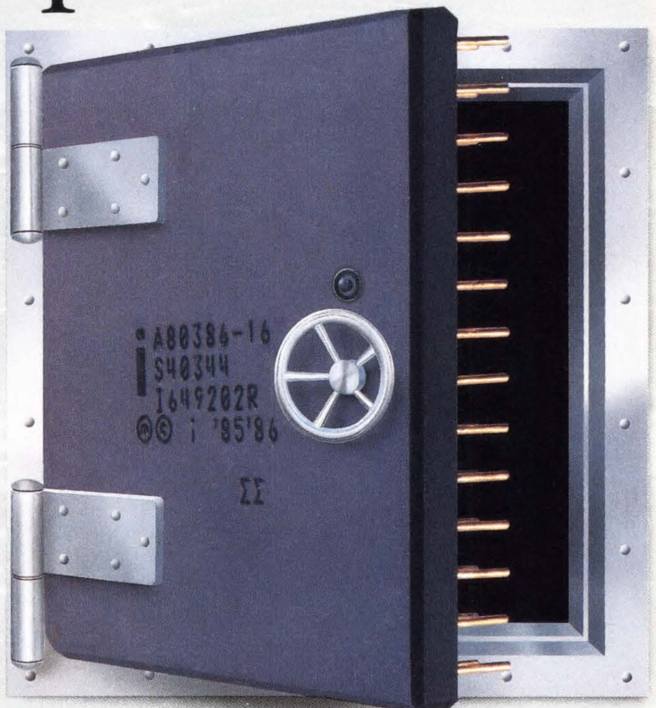
CIRCLE NO 137

How to crack 386 protected mode.



Unlock selectors and descriptor tables. Break open task state segments (TSS) and call gates. Microtek's In-Circuit-Emulator (MICE) cracks 80386 protected mode with real-time, non-intrusive emulation to 20 MHz.

MICE unravels all the intricacies of the 80386, so you harness its full potential. Internal registers, including GDT and IDT base values are all directly accessible. And MICE also provides decoded access to all selector and descriptor bits, like privilege level, segment type and page accessed bits.

Use MICE as a stand-alone device, or integrate it into your development environment. MICE easily interfaces with the IBM® PC/XT/AT, VAX,® Apollo® and Sun® computers.

And the 80386 emulation system is just one of our many embedded software development tools.

Our Software Analysis Workstation (SAW) delivers hardware-based, real-time software analysis in a source code environment. For source code development, our Microtec® Research products provide you with C and Pascal cross-compilers, cross-assemblers and debuggers for many popular microprocessors.

And MicroCASE™ backs all of its products with solid applications support, both at the local and factory level.

Microtek enjoys a long track record of being first to market with quality support for many major microprocessors. We were the first alternative for 80386 emulation. We're first to provide non-proprietary support for 80386 protected mode.* And you can count on the same support in the future.

For more information and product literature on our full line of MICE, call us at (408) 253-5933.

Crack 80386 protected mode, and open the door to exciting design possibilities—with the best 80386 emulation system now available. From MicroCASE.

MicroCASE

Formerly Northwest Instrument Systems, Inc.

P.O. Box 1309 • Beaverton, OR 97075

*Without the use of a proprietary "bond-out" chip.

IBM is a registered trademark of International Business Machines. VAX is a trademark of Digital Equipment Corporation. Apollo is a trademark of Apollo Computer, Inc. Sun is a trademark of Sun Micro Systems.

Processors supported by Microtek: 80386, 80286, 80186, 80188, 8086, 8088, 68020, 68010, 68008, 68000, 6809, 6809E, 6502, Z80, NSC800, 8085, 8032, 8051, 8031, 8344, 8048, 8049, 8050, Z8, SUPER 8, 68HC11, 64180, 80515.

Circle No. 128 for demonstration

Circle No. 129 for literature

NEWS BREAKS

EDITED BY JOANNE CLAY

TWO-BOARD SET PUTS THE IBM PC ON THE STD BUS

The XT-7 card set from Octagon Systems Corp (Westminster, CO, (303) 426-8540) brings IBM PC compatibility to the STD Bus by means of a \$795 XT-7 CPU card and a \$495 XT-7 support card. The CPU card features an NEC V20 μP running at 7.15 MHz, two serial ports, a parallel printer port, 128k bytes of static RAM (SRAM) with room for an additional 128k bytes, a standard PC keyboard interface, a real-time clock, and a battery that maintains the state of the RAM and clock while the system is turned off. The CPU card also incorporates a ROM containing a standard BIOS (basic I/O system) and the latest version of the company's STD Basic language, which is specifically tailored for process-control applications. You can build a system with just the XT-7 CPU card, or you can replicate the function of an entire IBM PC by plugging in the support card, which adds a floppy-disk controller, an IBM CGA-compatible (Color Graphics Adapter) video controller, 128k bytes of battery-backed SRAM, and room for an additional 256k bytes of SRAM.—Steven H Leibson

CONTROLLER LETS YOU ZOOM INTO CAD DRAWINGS IN 2 SEC ON PS/2

Tapping the power of a T414 Transputer and custom graphics chips, the Nth Engine/2 display controller from Nth Graphics (Austin, TX, (800) 624-7552 or (512) 832-1944) lets you use your PS/2 computer to perform 2-sec zooms into large CAD-size drawings. This \$4295 16-color graphics board drives one or two 1024×768-pixel monitors—and the company can also reconfigure the board to work with lower-resolution monitors. The Nth Engine/2 maintains a compressed copy of your CAD drawing's vector-display list in its 1M-byte, onboard display-list RAM. A pop-up window shows you the entire drawing and highlights the area you've zoomed into. You can use the Nth Engine/2 under software control as a remote viewing station for your plotter, or you can use it to preview the plotter's output. Memory options let you increase the display-list RAM to 2M bytes on board, or to 4.5M bytes with a daughter board.—J D Mosley

GRAPHICS TERMINAL OFFERS THREE DIFFERENT COAX CONNECTIONS

The Tektronix (Portland, OR, (800) 225-5434) Model 4211 Graphics Netstation can interface to host computers via RS-232C serial ports, a TCP/IP-based Ethernet LAN, or an IBM 3270 coax connection. Furthermore, the terminal includes a dedicated graphics processor that features a redraw rate of 40,000 transformed and clipped 2-D vectors/sec. You can specify the graphics terminal with a 15- or a 19-in. color monitor. You can use the Graphics Netstation with more than 100,000 software applications developed for 4111 and 4200 Series terminals. The basic configuration of the 4211 costs \$6495 and includes three RS-232C ports, a parallel port, a keyboard, and 0.75M bytes of RAM. A 19-in. monitor costs an additional \$1500. The company plans to begin volume shipments of the product in November.—Maury Wright

SIMULATOR ADDS μP MODELS AND AUTOMATIC TIMING ANALYSIS

You can now simulate μPs with the Susie personal-computer-based simulator from Aldec (Newbury Park, CA, (805) 499-6867). The firm offers models for μPs from Intel, Motorola, and other companies, and it expects to support RISC processors in the first quarter of 1989. The μP models range in cost from \$1495 to \$1995 per processor family. The company has also added an automatic timing-analysis capability to the simulator. You load a net list and test vectors, and the simulator tests every pin on every chip for conflicts and timing violations with an accuracy spec of 10 psec. The newest release of the product also allows you to partition a simulated circuit, so you can simulate only a discovered problem area. The simulator's incremental-compiler design makes partitioning possible: It lets you test a small portion of a design, thus saving you the time required to simulate the entire design. The new release of Susie, with timing analysis, costs $2000.—Maury Wright

VENDOR OPENS ARCHITECTURE OF MODULAR INSTRUMENTS

In the hope of making the architecture of its modular microwave instrumentation system a de facto industry standard, Hewlett-Packard (Rohnert Park, CA, (707) 794-1212) has announced that it is placing the interface and mechanical specifications of the heretofore proprietary 70000 Series in the public domain. The company will provide design guides at cost and will not require vendors who develop modules that work in the system to pay a license fee. In addition, HP will sell kits of mechanical parts to permit the construction of 70000 Series modules and will allow the manufacturer of the custom ICs that interface the modules to the system's MSIB (modular-system interface bus) to sell the chips to anyone interested in buying them.

Hewlett-Packard is a founding member of the consortium that created the VXI (VME extensions for instrumentation) Bus, another open, modular-instrumentation standard. The company believes that despite VXI's wide applicability, the bus does not lend itself to the optimal implementation of microwave instruments. The 70000 Series can work with VXI-based instrumentation. It has been on the market since 1984 and has been thoroughly debugged. Therefore, HP sees the 70000 format as an ideal complement to the VXI bus for extending modular instrumentation to higher frequencies.—Dan Strassberg

VIDEO LINE DRIVERS SPEC 10-BIT RESOLUTION

Meeting the standard established by the RP-125 requirement of the Society of Motion Picture and Television Engineers (SMPTE), the VS620 and VS621 10-bit video line-drivers from VTC Inc (Bloomington, MN, (612) 851-5200) eliminate the skew, matching, and jitter problems previously inherent in similar small-scale ICs. The output-to-output skew for these chips is typically 1 nsec. The VS620 has differential ECL inputs; the VS621 uses single-ended TTL inputs. The chips transmit digitized video signals among different video-system units, via 10 parallel differential ECL signals, at a 27-MHz clock rate. Both chips sell for $26.20 (1000).—J D Mosley

DSOs OFFER 20-GHz BANDWIDTH, PERFORM DIFFERENTIAL TDR

The 11800 Series digital sampling oscilloscopes from Tektronix Inc (Beaverton, OR, (800) 935-9433) perform differential time-domain reflectometry (TDR). For measurements on balanced lines—for example, the twisted-pair cables often used for clock distribution in high-performance computer systems—the differential technique is both faster and more accurate than the more-familiar single-ended method. The scopes, whose pricing starts at $28,000 with a 2-channel sampling head and a pair of passive probes, offer a 20-GHz analog bandwidth. By using sequential equivalent-time sampling, they capture data at an effective 100G-sample/sec rate. They expand to 136 channels, and you can display eight of the channels at a time.—Dan Strassberg

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NEWS BREAKS: INTERNATIONAL

TOKEN-BUS CONTROLLER HANDLES MAP NETWORK PROTOCOL

In conjunction with the company's SAB82511 token-bus modem, the SAB82510 token-bus-controller IC from Siemens AG (Munich, West Germany, TLX 5210025; in the US, Santa Clara, CA, (408) 980-4500) implements a 1M-, 5M-, or 10M-bps carrier-band network station that conforms to the IEEE-802.4 standard. The IC is therefore suitable for use in MAP or Proway factory-automation networks. You can use it at a data rate of 20M bps on a fiber-optic cable. The controller implements the MAC (media access control) functions of layer 2 of the OSI model. To maximize throughput, it has an on-chip DMA controller to transfer received data, or data that is ready for transmission, to and from shared memory in the host system. Controlled by a set of high-level commands, the SAB82510 supports both command- and data-block chaining. The controller also has a real-time clock function that allows you to synchronize token-bus stations to real time, and a host interface that operates in the 80186 or 68000 µP bus mode (the modes are pin-selectable). The SAB82510 is a CMOS device packaged in a 68-pin PLCC. Sample quantities sell for $94.—Peter Harold

COMMUNICATION ICs SUIT ISDN S AND U INTERFACES

The MTC2072 and MTC2071 from Mietec (Oudenaarde, Belgium, TLX 85739) are single-chip implementations for interfacing equipment to the ISDN's S and U interfaces, respectively. The MTC2072 S-interface IC uses the AMI line code and conforms to CCITT recommendations for the 4-wire interface between subscriber terminals and network termination units. It provides separate receive and transmit loops that operate at 192k bps. Housed in a 22-pin plastic package, the device is expected to sell for around $9.50 (1000) in 1989 and drop to around $7.50 (1000) in 1990.

The MTC2071 provides a U interface for ISDN networks that use the 4B/3T line code. It uses adaptive filtering, implemented with DSP techniques, to provide echo cancellation and equalization. You can use the device on a telephone line as long as 8.2 km, and you can configure it for use at a number of different locations within an ISDN. The price for the MTC2071 in a 28-pin plastic package will be around $185 (1000) in 1989 and will fall to less than $50 (1000) during 1990.—Peter Harold

SPARC WORKSTATION BANDWAGON GAINS NEW MEMBER

Solbourne Computer Inc (Longmont, CO, (303) 772-3400) became the latest company to join the SPARC RISC (reduced-instruction-set computer) club when it announced a licensing agreement with Sun Microsystems Inc (Mountain View, CA, (415) 960-6543) for SPARC technology. Solbourne (formerly Solutions Are Everything Inc) was founded by Douglas B MacGregor, a principal designer of the Motorola 68020 µP. The company plans to offer low-cost, multiprocessor workstations based on a single-chip implementation of the SPARC µP that incorporates the CPU, a memory-management unit, data and instruction caches, and a bus controller. The 750,000-transistor, single-chip SPARC µPs and the workstations will be manufactured by Matsushita Electric Industrial Co Ltd (Osaka, Japan, Phone 06 909-1121), which owns 52% of Solbourne.—Steven H Leibson

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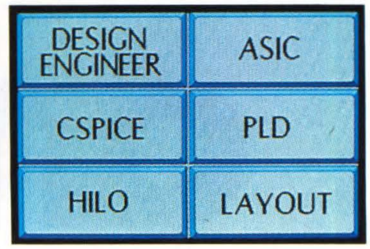

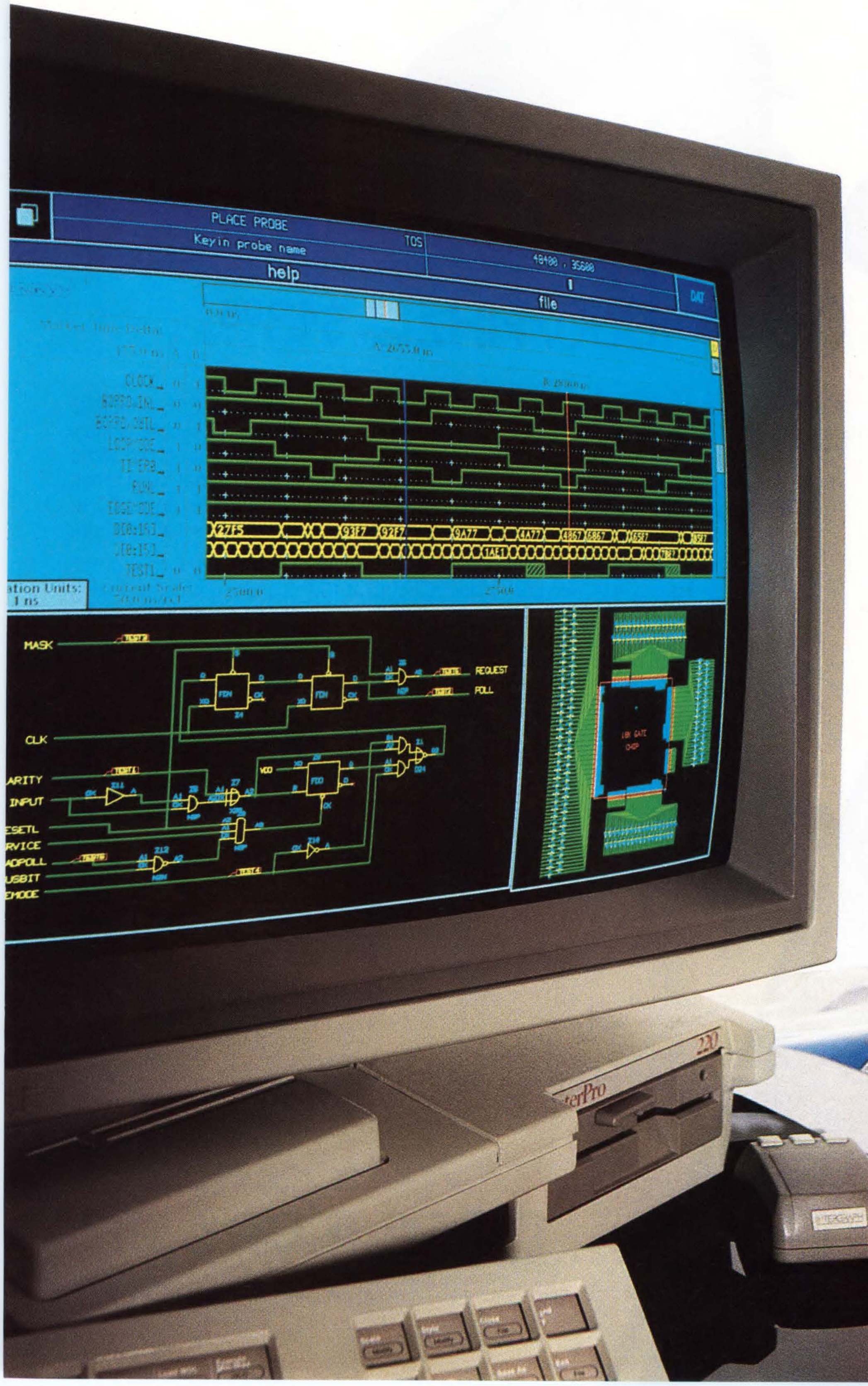

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††Midband $10f_L$ to $f_{u/2}$, ± 0.5dB †1dB Gain Compression ◊Case Height 0.3 In.
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ISOLATION (dB)	(L-R)	(L-I)
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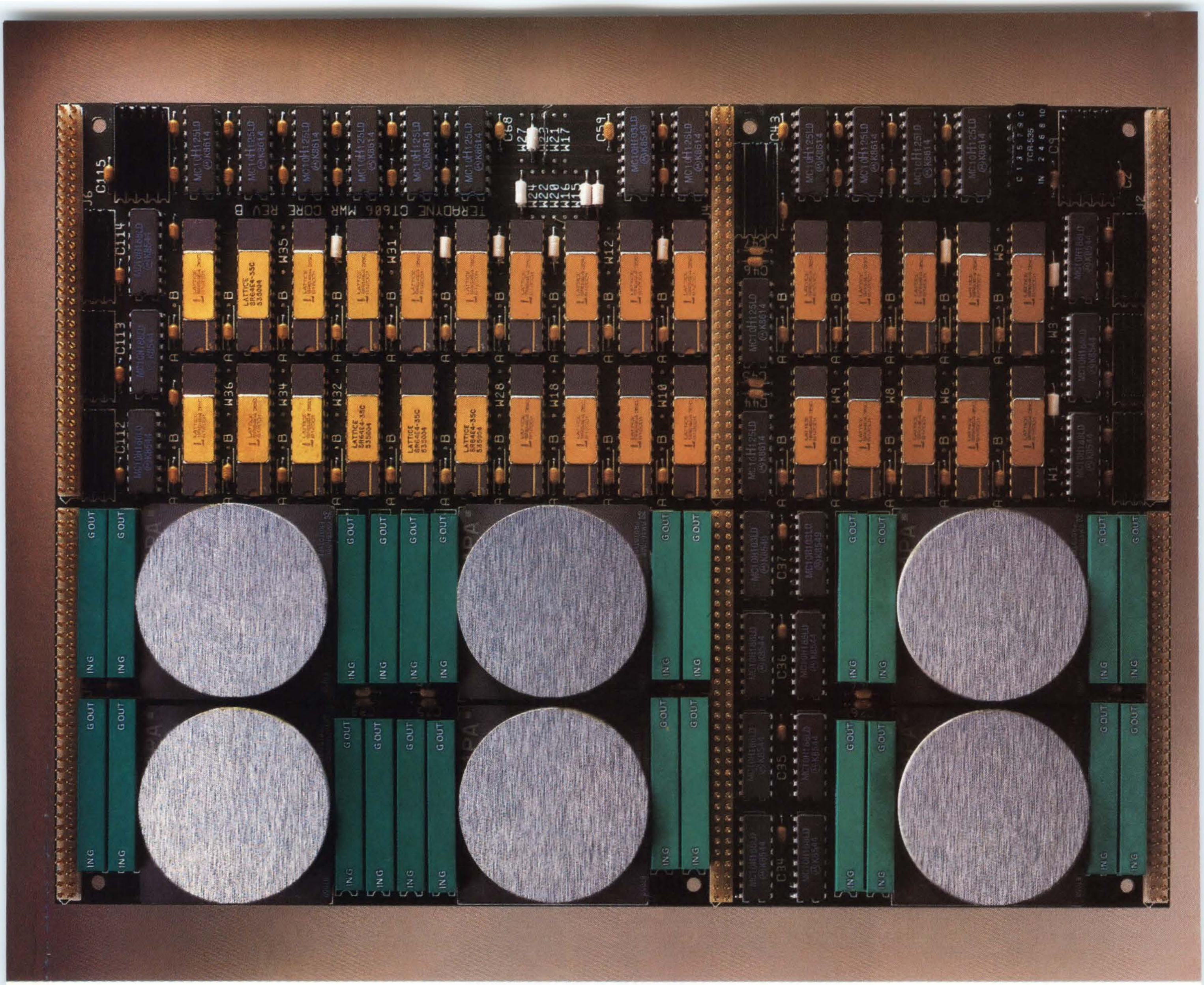

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SIGNALS & NOISE

The Bard takes a bow

Thanks very much for "Differential equations and Shakespeare: Melding engineering studies and liberal arts" in the Professional Issues section of the May 26, 1988, issue of EDN (pg 279). The availability of a good liberal education, alongside an effective engineering education, is certainly the wave of the future for those engineering students who desire it.

As engineers, we hold considerable de facto power in shaping the world through the products we design and produce. But because of our own head-in-the-sand attitudes, we are largely excluded from the decision processes that affect the society in which we live. We can no longer afford to hold such de facto power in technical, business, and entrepreneurial areas, but lack the perspective, techniques, and humanness to wield it properly.

I am very much in favor of a better liberal education for engineers. But a formal, conventional liberal-arts curriculum is not the only way to gain such education, especially now that we've left school and we hold responsible positions. Curiosity and interest in the world outside of science and engineering is the basis for a home-grown liberal education for many of us long past our college years.

We can read, obtain reading lists of related books, and follow our own "reading trails" of such books and periodicals. We can discuss our interests with friends and colleagues, and new friendships, perhaps outside of science and engineering circles, can develop. Mentor relationships with people knowledgeable in fields of interest to us can arise when we probe into certain subjects. We can enroll in selected university or industrial courses and seminars designed to augment the poor humanities backgrounds of scientists and engineers. We can take continuing-education courses and community "free school" courses. Travel for pleasure or business can turn into an educational and personal-reflection process.

The possibilities are endless for accomplishing a liberal education outside the formal university structure. Such structures generally haven't proved suitable for the needs and schedules of working engineers, anyway.

The subject of broadening an engineer's horizons often brings a negative knee-jerk reaction when aired either in discussion or in print. This is too bad, and it's indicative of a potentially destructive and dangerous mentality within the profession. Such broadening is not for everyone, and no one is asking that it be forced on an individual.

But for those of us who are interested in both technology and the world at large, let's make it possible to be involved in both, during our degree educations and in the careers that follow.

Richard Simonelli
Ziji Technical Services
Boulder, CO

Engineering schools can aid in education reform

The Professional Issues pages by Deborah Asbrand in EDN's May 26, 1988, issue (pg 279) discuss the very serious problem of engineers' education in "humanistic," "liberal-arts," or "nontechnical" subjects. As an older engineer, I should like to add some comments and suggestions.

First, the problem is real. Few of us can doubt that engineers will be better in their jobs and better citizens if they know how to write effectively and speak clearly. To do so, they require not only writing and speaking skills, but a full measure of "cultural literacy" (Hirsch, E D, *Cultural Literacy: What Every American Needs to Know*, Houghton Mifflin Co, 1987).

Deborah Asbrand writes that "Technical talent is as important as ever, but it's no longer enough." Of course, it never was. Engineers may be less accomplished than members of some other professions, but the level in most of today's American society is dismally low, and perhaps is still declining (Bloom, A, *The Closing of the American Mind*, Simon and Schuster, 1987; Ravitch, D, and C E Finn, C E, *What Do Our 17-year-olds Know?* Harper and Row, 1987).

Second, consider the solutions. To the extent that we are talking about a national problem, the solutions are beyond the scope of engineering schools. These schools can probably contribute to, and will certainly benefit from, a general improvement in young people's education, but for now they must look at what is specific to engineers. This country is fortunate in that it has a large number of schools with widely differing approaches. Deborah's examples seem to suggest that many of our best engineering schools see an increase in required nontechnical courses as the main road to giving engineers a broader background. In this letter I shall suggest an entirely different approach, which I believe has some merit. I hope a few good schools will try it.

Despite Deborah's remarks about the time available for liberal-arts studies, it should be obvious that a school year has only a finite amount of time. What time is used for subject A is necessarily unavailable for subject B. This fact would not be not changed by lengthening the school year from eight to 10 or 11 months, useful as that might be.

What I propose is to raise entry requirements to include a thorough preparation in all the basic skills as well as math and humanities. Then engineering schools would concentrate on math and physics as general background, and specific engineering theory and applications courses would be the mainstream, with increasing specialization offered for advanced-degree students. Students with an interest in marketing or administration should be encouraged to supplement their engineering degrees with MBAs, not dilute their engineering studies. Any humanities courses offered or required should have direct relevance to an engineering career, and should be offered for credit only if they form a coherent entity. At most, 10 to 12% of graduation credit should be allowed for these courses, and the requirement should not exceed 5 to 6%. Philosophy with application to science might be one such required course. Such a course might also benefit students who are not in engineering.

As requirements for entry, I

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would include basic skills such as reading and writing at a high level and a solid mastery of calculating devices from the slide rule and log tables to simple computer tasks—maybe on personal computers running Basic. Next, students should be required to have elementary math at least up through trigonometry, some number theory, and some calculus.

In the humanities, the entering student should have a thorough knowledge and understanding of American and world history, civics, economics, geography, literature, mythology, and art, and preferably should learn to read, write and speak at least one foreign language. In all of these areas, accomplishment in the subject—not just exposure to it—should count. The engineering school might offer remedial, noncredit courses for students who fall short in one or a few of the entry requirements. The school might also offer a full-year preparation course, maybe for college credit, but not to be counted as part of the engineering graduation requirements. Entering students should prove their knowledge by passing a test, whether they have come directly from high school or from the special preparation course.

I believe that a curriculum set up along these lines could attract many students by offering superior engineering preparation without cultural deprivation. I realize that few high schools today offer preparation at the level this program would require, but that deficiency should not be the engineering school's main concern, and the demanding entry requirements would give some high schools the incentive to improve. That, in itself, is highly desirable.

P S—I also have a piece of advice for EDN and for Deborah Asbrand: It is almost axiomatic that you should write with a clear picture of your audience in mind, but the style Deborah uses is not appealing to engineers, even if another audience might enjoy it. Whatever failings engineers as a group may have, they can think about abstractions; they do not need to have a subject regurgitated by "real" people—such as Bob Wilson, Dale Ogle, Terry McCarty, etc, even if those people are indeed real and not composites or fictions. In fact, the "human interest" style is generally annoying to many of us, and I only read the piece referred to because of my great interest in the subject.

Jorgen P Vinding
Vashon, WA

(Ed Note: The people Deborah quoted in the article are real. EDN does not represent fiction as fact. Further, the Professional Issues section is one of the best-read sections of the magazine. The comments we receive from readers on the Information Retrieval Service cards are a further indication that many of Mr Vinding's colleagues don't share his opinions on human-interest-style writing. As always, we invite readers to send their comments on the subject to the Signals & Noise Editor, EDN, 275 Washington St, Newton, MA 02158.)

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

MAXIM DESIGN NEWS

Analog Design Insights from Maxim Integrated Products August '88

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- Low voltage application circuits
- New RS232 products – Single +5V supply – Already an industry standard – Even more features have been added
- New Opto-Isolated RS-232 transmitter/receivers solve industrial interface problems

Power Supply Circuits

- DC-DC converter IC that works from a single cell battery
- Linear and switching regulators that run on microwatts
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(Please see location and date schedule on back page)

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Attention: Seminar Coordinator

Maxim's 1988 Analog Design Seminar Schedule

Maxim's 1988 Analog Design Seminar is being held in major cities across the United States. Choose a location near you and either mail the attached reply card to Maxim, contact us at (408) 737-7600, or make a reservation today with your Maxim representative.

#44	AL, Huntsville	Nov. 18
#48	AZ, Phoenix	Nov. 30
#50	AZ, Tempe	Dec. 1
#52	AZ, Tuscon	Dec. 2
#62	CA, Los Angeles	Dec. 14
#11	CA, Oakland	Sept. 28
#63	CA, Orange County	Dec. 15
#1	CA, Sacramento	Sept. 13
#57	CA, San Diego	Dec. 8
#60	CA, San Fernando Valley	Dec. 13
#13	CA, San Jose	Sept. 29
#58	CA, Santa Barbara	Dec. 9
#54	CO, Colorado Springs	Dec. 7
#53	CO, Denver	Dec. 6
#8	CT, Waterbury	Sept. 23
#49	FL, Clearwater	Dec. 1
#46	FL, Ft. Lauderdale	Nov. 29
#51	FL, Ft. Walton Beach	Dec. 2
#47	FL, Orlando	Nov. 30
#38	GA, Atlanta	Nov. 15
#36	IA, Cedar Rapids	Nov. 10
#16	IL, Chicago	Oct. 6
#17	IL, Chicago (Hallmark)	Oct. 7
#21	IN, Fort Wayne	Oct. 14
#20	IN, Indianapolis	Oct. 13
#6	MA, Burlington	Sept. 21
#7	MA, Framingham	Sept. 22
#27	MD, Baltimore	Oct. 26
#28	MD, Calverton	Oct. 27
#18	MI, Detroit	Oct. 11
#19	MI, Grand Rapids	Oct. 12
#22	MN, Minneapolis	Oct. 18
#9	Montreal, Quebec	Sept. 26
#35	MO, Kansas City	Nov. 9
#34	MO, St. Louis	Nov. 8
#37	NC, Raleigh	Nov. 11
#5	NH, Nashua	Sept. 20
#25	NJ, Saddlebrook	Oct. 21
#23	NJ, Westchester	Oct. 19
#24	NY, Long Island	Oct. 20
#61	NY, Rochester	Dec. 14
#59	NY, Syracuse	Dec. 13
#33	OH, Cleveland	Nov. 4
#32	OH, Columbus	Nov. 3
#31	OH, Dayton	Nov. 2
#45	OK, Tulsa	Nov. 18
#2	OR, Portland	Sept. 14
#10	Ottawa, Ontario	Sept. 27
#26	PA, Fort Washington	Oct. 25
#30	PA, Pittsburg	Nov. 1
#55	SC, Columbia	Dec. 7
#40	TN, Knoxville	Nov. 16
#42	TN, Nashville	Nov. 17
#12	Toronto, Ontario	Sept. 28
#43	TX, Austin	Nov. 17
#41	TX, Dallas	Nov. 16
#39	TX, Houston	Nov. 15
#56	UT, Salt Lake City	Dec. 8
#4	Vancouver, B.C.	Sept. 16
#29	VA, Tysons Corner	Oct. 28
#3	WA, Seattle	Sept. 15
#15	WI, Madison	Oct. 5
#14	WI, Milwaukee	Oct. 4

Maxim's 1988 Analog Design Seminar Reservation

Select the seminar location nearest to you, noting the seminar number when reserving your seat:

Seminar No.:____________ Location:____________________ Date:__________

Name:____________________ Job Title:____________________

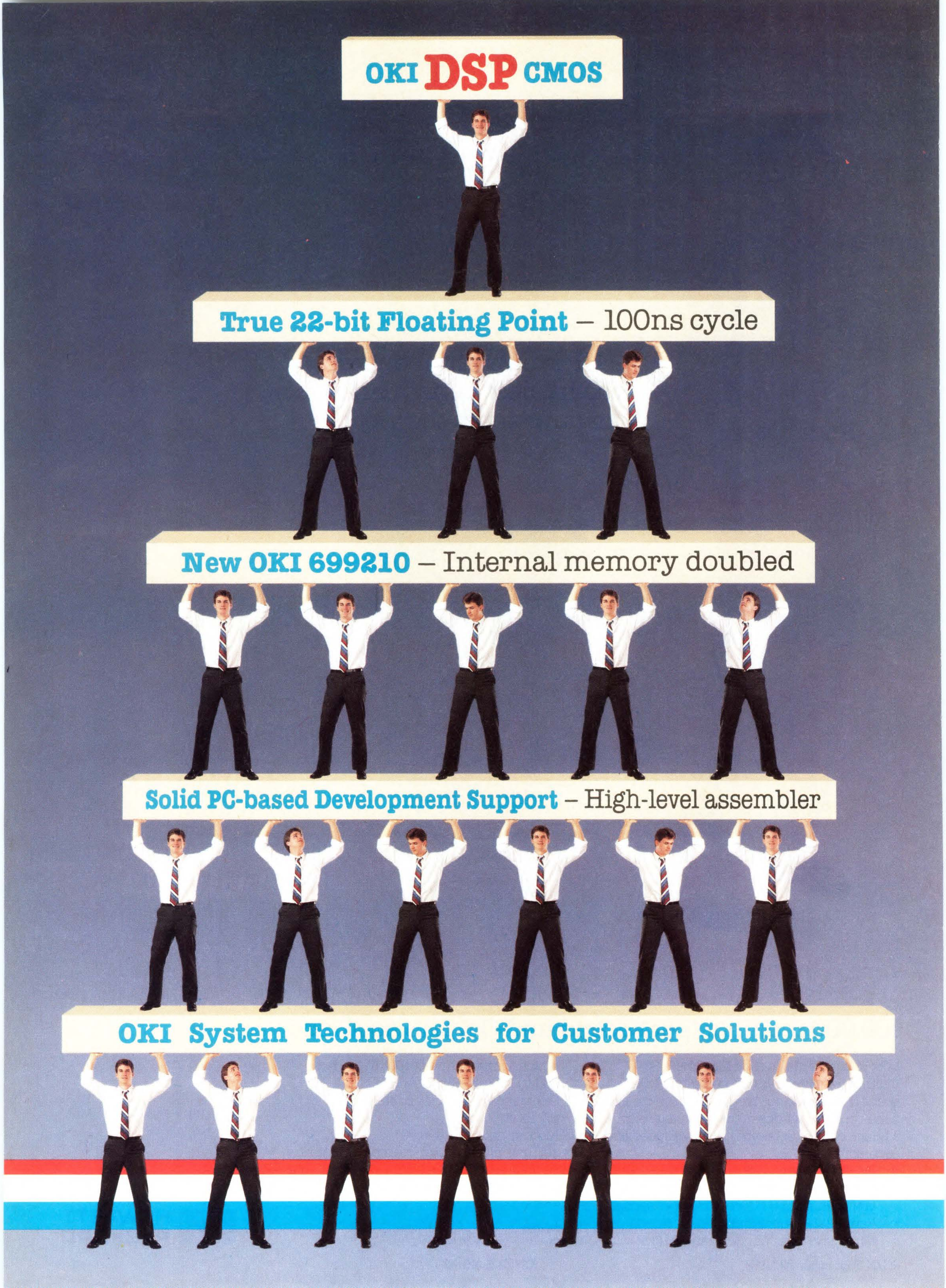
Company:____________________ Dept./Div.:____________________

Address:____

City:____________________ State:____________ Zip Code:__________

Please give a telephone number where you can be contacted, so Maxim's representative can inform you of hotel and starting time (most seminars start at 8:30 a.m.): (   ) ________________. Refreshments will be served.

❒ Sorry, I won't be able to attend. Please send me a set of the Seminar literature.



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True 22-bit Floating Point – 100ns cycle
New OKI 699210 – Internal memory doubled
Solid PC-based Development Support – High-level assembler
OKI System Technologies for Customer Solutions

CALENDAR

1988 National Communications Forum (NCF88), Chicago, IL. NCF88, 303 E Wacker Dr, Suite 379, Chicago, IL 60601. (312) 938-3500. October 3 to 5.

Computer Graphics Invitational Computer Conference (ICC), Irvine, CA. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 4.

International Electronic Manufacturing Technology (IEMT) Symposium, Lake Buena Vista, FL. Bill Moody, 2529 Eaton Rd, Wilmington, DE 19810. (302) 478-4143. October 10 to 12.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Indianapolis, IN. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. October 11 to 14.

Computer-Aided Software Engineering Symposium (CASES), Chicago, IL. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. October 12 to 14.

Modern Electronic Packaging (seminar), Boston, MA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. October 12 to 14.

Worst-Case Circuit Analysis (seminar), San Francisco, CA. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. October 17 to 19.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. October 18 to 21.

Computer Graphics Invitational Computer Conference (ICC), Dal-

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And that's just the start. Coming down the home stretch are more Siemens entries...1.5/1.2 micron CMOS standard cells and 1.2/1.0 micron CMOS sea of gates arrays. Use our sea of gates CMOS family for quick turn logic and memory on one chip or design your high-performance, cell-based ASICs utilizing the common ADVANCELL™ ASIC library and guarantee yourself compatible second sources.

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Siemens...
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 CG/2000-460 WLM 795

CIRCLE NO 99

CALENDAR

las, TX. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 20.

OEM Peripheral Invitational Computer Conference (ICC), Bloomington, MN. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 20.

CASE Benchmarks: A Product Comparison Seminar, Boston, MA. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. October 24 to 26.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. October 24 to 27.

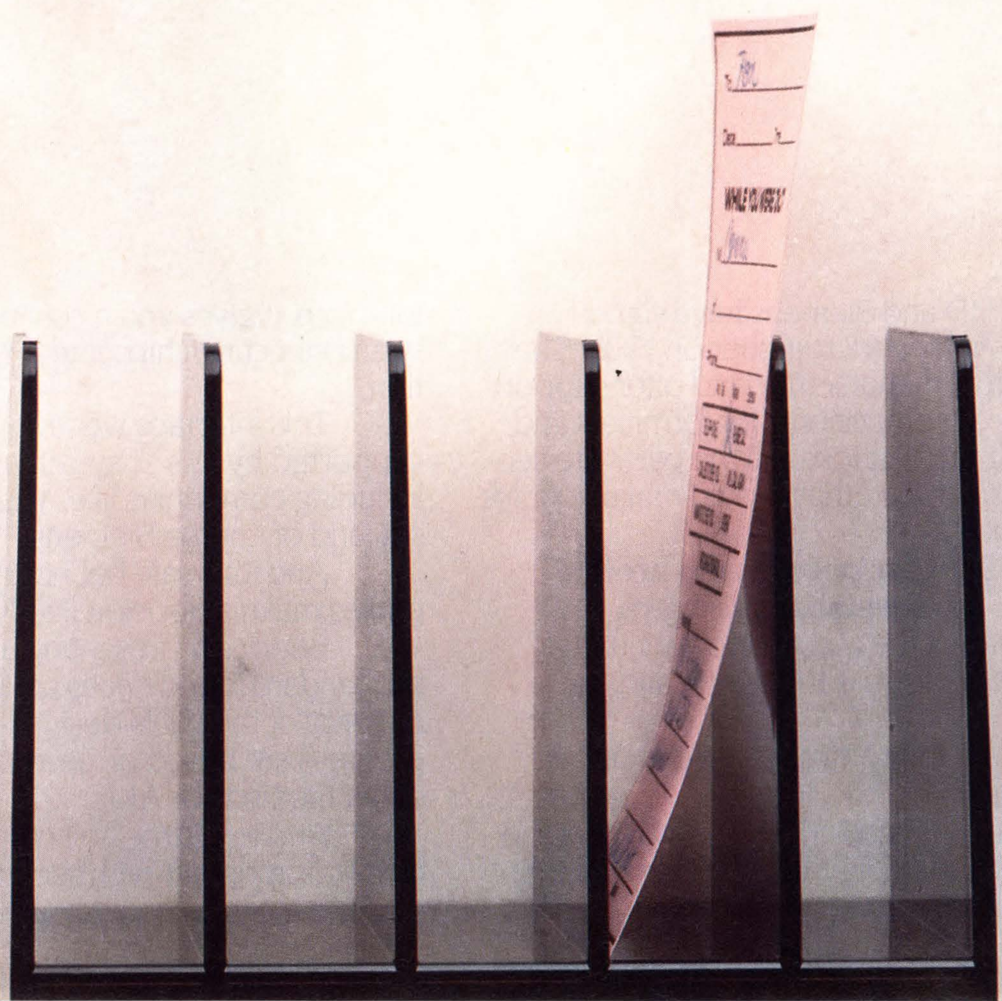
OEM Peripheral Invitational Computer Conference (ICC), Westlake Village, CA. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 25.

11th Annual Newport Conference on Fiberoptics Markets, Newport, RI. Kessler Marketing Intelligence, America's Cup Ave at 31 Bridge St, Newport, RI 02840. (401) 849-6771. October 25 to 26.

Unix Hands-on Workshop (short course), Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. October 25 to 28.

ICALEO '88 (International Congress on Applications of Lasers and Electro-Optics), Santa Clara, CA. The Laser Applications Congress, 5151 Monroe St, Suite 102W, Toledo, OH 43623. (419) 882-8706. October 30 to November 4.

Finally, a really important phone message.



AMD and Siemens have signed an agreement to work together on ISDN. They'll co-develop, manufacture, and offer support for a line of components for terminals and switching applications. All the parts are second sourced. And that should make your life a lot easier.

ISDN for people who aren't professional gamblers.

One of the most important things about any system is the right standard, agreed?

And any company can develop a standard.

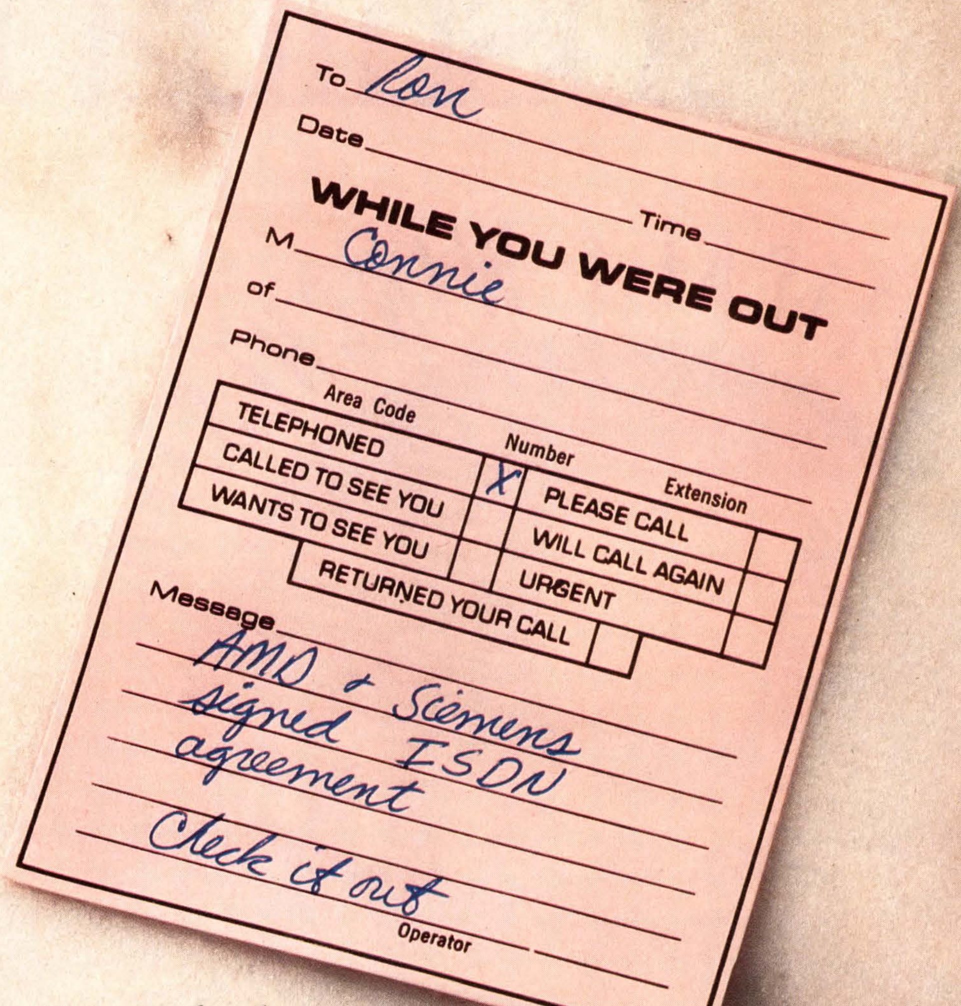
But Siemens and AMD will meet the IOM™-2 standard. IOM-2 is Siemens' implementation of the General Communications Interface. It gives you a cost effective way of interconnecting chips into any ISDN application.

This interface was jointly defined and supported by lots of system manufacturers including companies like Alcatel, Italtel, Plessey, and of course, Siemens.

And it's a safe bet none of these companies make a decision lightly.

Besides representing a widely accepted standard, our devices are proven. The majority of the ISDN designs in the field or in progress are based on components from either Siemens or AMD.

And this is the first complete line of ISDN components with second sourcing. So you'll never have to worry about finding parts.



We're ready when you are.

Today, we're offering fifteen proven ISDN devices for terminal and switching designs. With more to come soon.

And this family of devices is modular. Future advances will fit right into your systems without redesigns.

Reach out and touch some development tools.

We have a complete range of jointly supported hardware and software development tools, too. For example, we've got AmLink3,™ ISDN development software. AmLink3 is a full implementation of Q.931 and X.25. And it's operating system independent.

AmLink3 has passed AT&T compliancy testing. And we have versions to support other switches in the works.

You can even get the source code for AmLink3.

Our human resources are abundant, too. We have an army of experienced Field Application Engineers worldwide.

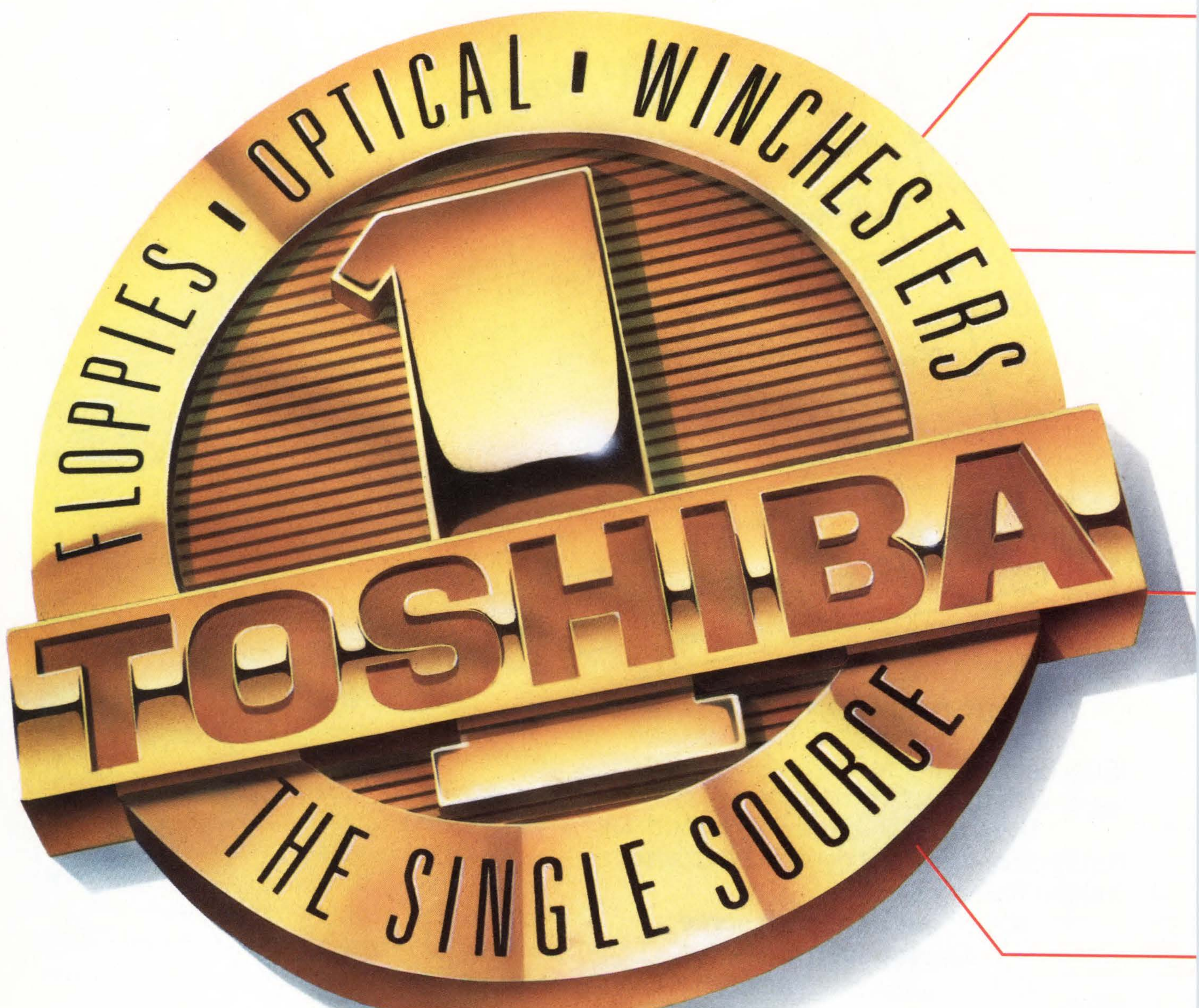
With all that Siemens and AMD have to offer, this might be one phone message you should answer. Here's a number where we can be reached. 800-222-9323. And if you can't call, write.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

CIRCLE NO 95

When You Wa
Toshiba Is



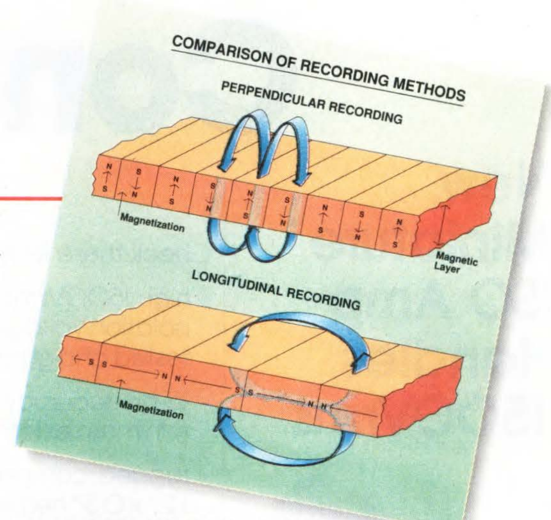
nt Innovation, The One.

CHIP TECHNOLOGY.

Toshiba quality is built right into every disk drive we manufacture. All the way down to the VLSI chips we make ourselves and our advanced Surface Mount Technology. So you get quality and performance that are consistently great.

OPTICAL TECHNOLOGY.

We delivered the world's first optical drive back in 1981. Our current line includes the fastest half-high 5.25″ CD-ROM and the capacity leaders in 5.25″ and 12″ WORM.

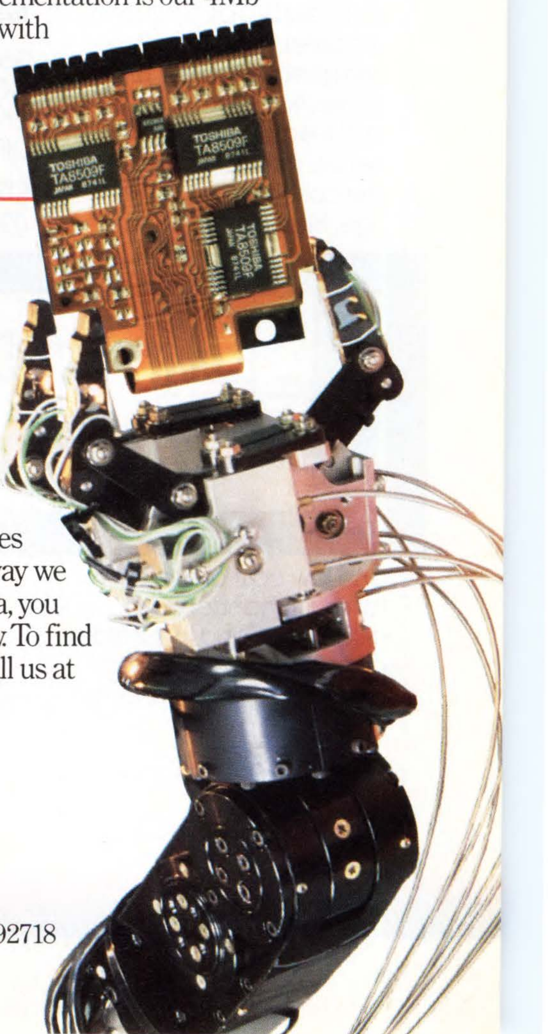


PERPENDICULAR RECORDING.

Toshiba holds key patents in the area of perpendicular recording. The first product implementation is our 4Mb floppy drive, with lots more to come.

SERVO TECHNOLOGY.

The Hybrid-Servo on our MK-250 Winchester drive uses dual servo technology to provide 380Mb on 25% fewer disks. This pioneering effort lays a solid foundation for the gigabyte-plus 5.25″ Winchesters to come.



ROBOTICS.

Even the robots we use to build our drives are built by Toshiba. It's just one more way we make sure that, when you select Toshiba, you get disk drives of consistent high quality. To find out how Toshiba can give you a hand, call us at 1-800-456-DISK.

In Touch with Tomorrow

TOSHIBA

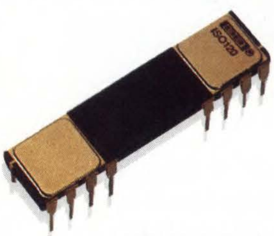
TOSHIBA AMERICA, INC.

Disk Products Division, 9740 Irvine Blvd., Irvine, CA 92718

CIRCLE NO 96

The Analog Isolation Revolution Continues...

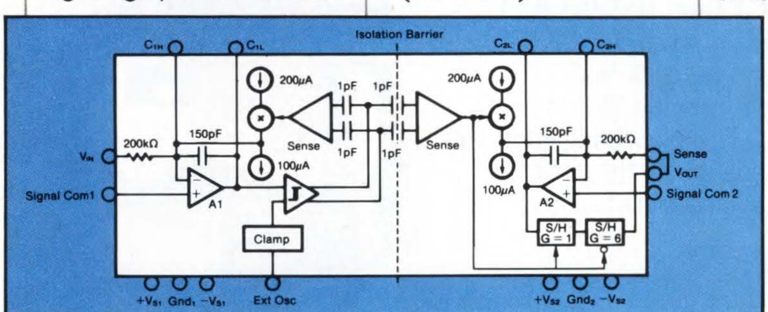
New, Miniature ISO Amp Handles 1500Vrms



Our new ISO120 isolation amplifier gives circuit designers more circuit protection, accuracy, and reliability than ever before possible at such low cost. Its small package, high performance, and low cost are ideal for multichannel data acquisition and industrial control systems and test equipment applications.

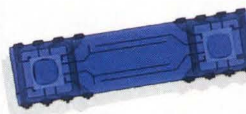
Check these features:

- high 1500Vrms rated isolation voltage, 100% tested and guaranteed
- 12-bit accuracy with minimum external parts
- rugged, compact 1.2″ x 0.3″ hermetic DIP package
- wide ±4.5V to ±18V supply range
- synchronizable to eliminate "beat frequency" noise
- 3500Vrms model, ISO121, available in a 2″ x 0.6″ hermetic DIP
- $17.00 in 100s (ISO120G)*



*U.S. price only

Patented Barrier Technology Is The Key



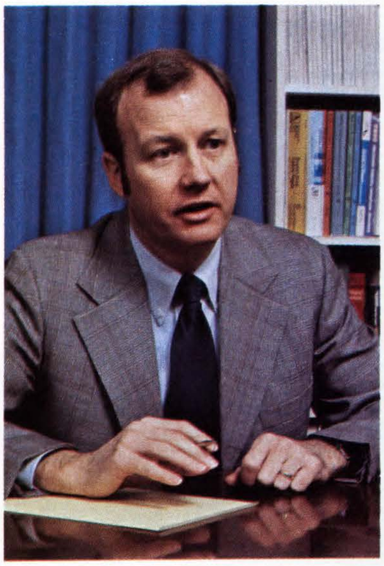
The superior isolation performance of the new amps is achieved using Burr-Brown's revolutionary ceramic capacitive barrier technology, similar to winning designs for the popular ISO102/106 series. The input and output sections of ISO120/121 are galvanically isolated by matched 1pF tungsten capacitors embedded in the ceramic barrier material. This creates a very rugged, completely hermetic isolation barrier able to withstand extreme mechanical, thermal, and electrical stresses with no damage.

We Have All The "Isolutions"™ You Need!

We offer more signal and power isolation solutions than any other company, all backed by 30+ years of analog design and manufacturing experience. Ask your Burr-Brown technical rep for details, or call Applications Engineering, 602/746-1111. Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734.

BURR-BROWN®

It's time for Congressional change



Over the past few decades, Congress has become a haven for people who advocate narrow interests rather than for statesmen who hold a broader vision. Although the issue is easily overshadowed by the Presidential election this year, it's important to remember that we'll also be electing a new set of congressmen and congresswomen this year, along with quite a few senators. Here are several ideas that might get Congress back on track and make it once again responsive to the *people* who elect it:

1. Establish limited terms of office: 12 years for a senator and eight years for a representative. It's unlikely that our Founding Fathers ever envisioned the class of "professional" politicians we have today. New people bring with them fresh ideas, and both are in short supply today.

2. Finance congressional elections by individual contributions alone. No more political-action committee (PAC) money could be given to candidates. If you have a Social Security number, are a US citizen, and are registered to vote, then you can contribute a maximum of $100 to candidates you can vote for.

3. Limit outgoing mailing during election years. During 1986—the last congressional-election year—Congress mailed 12,000 items for every incoming letter. Most representatives flood their constituents with newsletters and reports during election years. Today's PAC money and mailing advantages almost guarantee that we'll see a re-election rate of close to 100% in the House this year. (It was 98% in 1986.)

4. Make Congress live up to the laws and regulations it applies to others. It's now exempt from the Civil Rights Act and the Ethics in Government Act, for example. So Congress can tell you that discrimination is illegal while discriminating against anyone it chooses to. If the citizens should live by the law, so should their representatives.

5. Put a lid on the number of staff employees each representative and senator has. Congress employs about 31,000 people, many of whom are related to other officials. Most of our representatives could get by with smaller staffs if they weren't catering to lobbyists and special-interest groups. Four or five staff people would do it.

6. Limit the length of any bill being considered. Some people suggest a limit of 25 pages, which would be the length of the Constitution if it were typed double spaced. It might be wise to limit a bill to one idea and to disallow any riders or attachments. The recent 1000-page trade bill was an abomination. It was too long to be read—much less understood—by anyone, and it contained many special provisions that would benefit only pressure groups and lobbyists.

Some of the points above may seem a bit radical, but even if you disagree with them, they're worth thinking about and asking your candidates about. If you've been paying attention to Congress's antics this year, you'll have questions of your own, too. Go ahead and ask them. There's no better time to get a representative's attention than during an election year. You've got about four weeks left.

Jon Titus

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2), 1977, 1976, 1975
American Society of
Business Press Editors Award
1988, 1983, 1981

This chip enabled us to process signals of the past.

The Rosetta Stone, discovered in 1799, was the key to deciphering the hieroglyphics that had been incomprehensible for centuries.

Signal processing, when you come right down to it, is multiplication, addition, subtraction and storage. Doesn't sound very exciting.

But put together a set of building blocks that do those simple operations with almost unimaginable digital speed and precision. Then add A/D converters that bring in information from the world around you. Plus D/A converters that restore the digitally processed signals to a form your senses can understand.

And you've built a signal processing system that will enable you to do things that couldn't be done before, see things that couldn't be seen before and understand things that could never be understood before.

That's exciting. And we can help make it happen.

Complete systems solutions.

Our approach to signal processing is simple.

We've taken our unparalleled experience in data conversion and added to it a set of signal processing chips that perform operations that used to require entire circuit boards.

Here's a sample of what they can do for you:

ISP 9110 12-Bit Microprogram Sequencer: expanded 33 word stack, 50 ns minimum cycle time.

ISP 9119 FIFO RAM Controller: uses standard RAMs to build FIFOs up to 64K deep, 15 MHz operation.

ISP 9128 FIR Filter Controller: implements 16-bit filters to 128 Taps, 128 Tap sampling rate of 100kHz.

ISP 9210 16x16 Multiplier Accumulator: innovative high-speed architecture (65 ns commercial, 75 ns military), low-power operation.

ISP 9216 16x16 Multiplier: low-power, industry-standard compatible to AM29516 and MPY016.

ISP 9520/21 Pipeline Register: high-speed access,

output selectable from any register.

With devices like these, we can give you a total integrated signal processing solution. Plus the added benefits of single-vendor support and package pricing.

Position yourself for the future.

Signal processing is changing every day.

That's why you need more than a signal processing supplier who has a few good parts.

You need a long-term partner who has a commitment to signal processing, and the resources in every area that signal processing calls upon.

For example, the chips of tomorrow will very likely combine signal processing, data conversion and high-speed logic. When you work with us, you'll get our Intersil expertise in processing and conversion. Plus our RCA Advanced CMOS Logic capabilities. Plus the more than 20 years of GE experience in radar, sonar, medical imaging and other demanding DSP applications.

If worries about complexity and cost have deterred you from taking the exciting step into digital signal processing, call us. Together, we'll step into the future.

For more information, contact your local GE Solid State sales office or distributor. Or call toll-free, 800-443-7364, extension 30.

In Europe, call: Brussels, (02)246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

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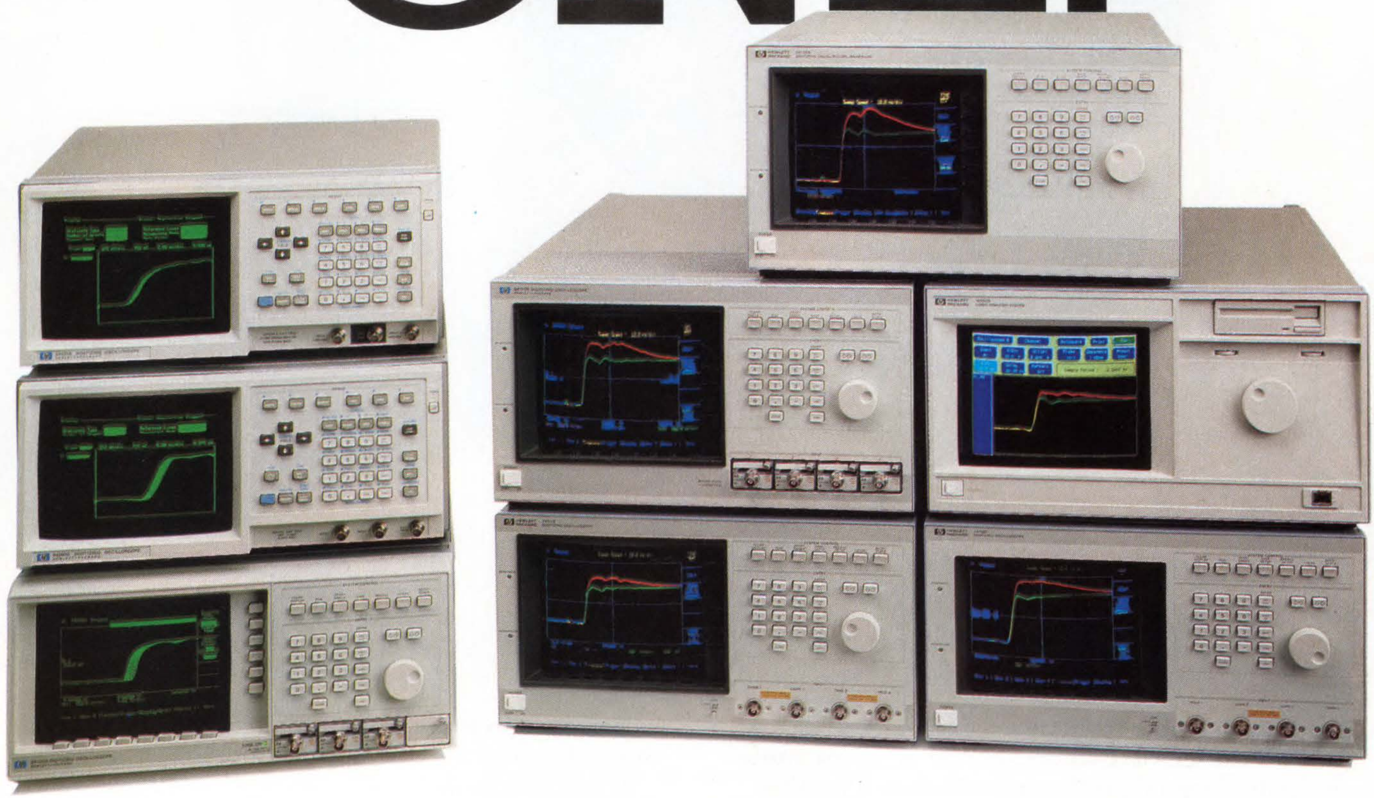

The best new feature in an HP digitizing oscilloscope is a FREE printer!

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- HP 54110D – 1 GHz bandwidth plus color
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- HP 54200A/D – Affordable 200 Megasamples/second
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- HP 16500A Oscilloscope – 8 channels 400 Megasamples/second each

From now until February 28, 1989, when you order a digitizing oscilloscope*, you'll get FREE hardcopy. Because HP will *give* you a printer!

And not just any printer, but a high-performing HP PaintJet® or ThinkJet® printer that quickly and easily creates hardcopy results of on-screen data with just the push of a button. Say goodbye to mounting a camera on

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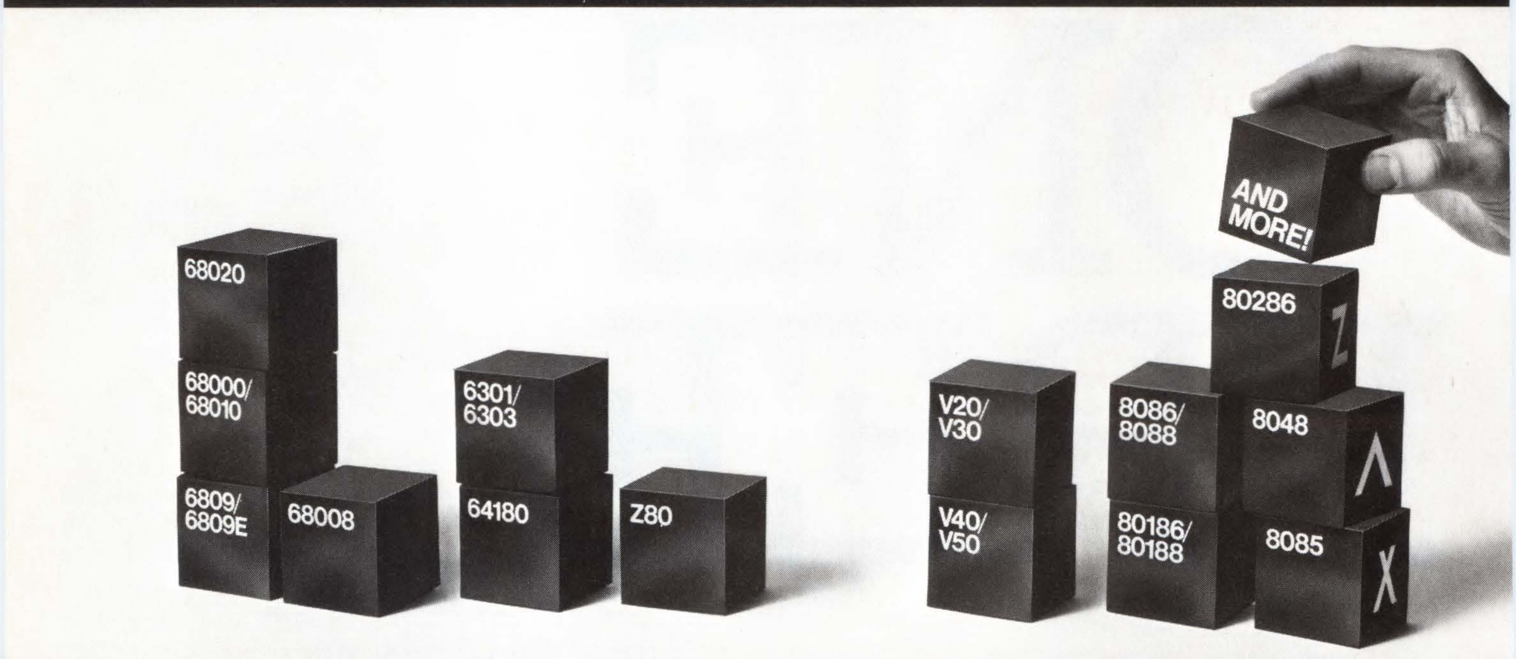
the scope face, developing film and scratching measurement results into the picture. The printer does it all, quickly and easily reproducing the measurements taken by the digitizing oscilloscope. Order an HP scope with a monochrome CRT and get a FREE HP ThinkJet printer — a $495 value. Order an HP scope with a color CRT, and get a FREE HP PaintJet printer — a $1395 value.

Call HP today:
1-800-752-0900, ext. 215W.

Now is definitely the time to team up with an HP scope. For more information about HP's broad family of digitizing oscilloscopes, call today. Our FREE printer offer ends on February 28, 1989. It's an offer so good, even the phone calls are FREE!

HEWLETT PACKARD

Microprocessor Support Made Simple



Now, ZAX simplifies microprocessor design, integration and testing with their advanced line of ERX- and ICD-series emulators. You simply tell us the processor that drives your design and we tailor a development system especially for your environment, including full software support.

Our ERX-series emulators provide over *80 debugging commands, with 256,000 hardware breakpoints, real-time performance analysis, high-level language debug and trace analysis* of program execution while you emulate in real-time. And they interface directly to your personal computer (AT-class) to provide you with a complete host development station and emulation manager. This consolidated approach utilizes industry-standard equipment and eliminates the use of a proprietary dedicated chassis.

ZAX established the benchmark for standalone emulation tools when they introduced their versatile line of ICD-series emulators. Completely flexible, ICD-series emulators can be interfaced to *either a simple terminal or host computer* (from pc to mainframe) depending on your requirements. This makes them ideal for both *in-house development* and *on-site testing.*

Simplify support for your microprocessor development projects with the help of ZAX! Call today to arrange a product demonstration or write for complete details about our product line. Call us TOLL FREE at 800-421-0982 (in California phone 800-233-9817) or write to ZAX CORPORATION, 2572 White Road, Irvine, CA 92714.

In Europe, call United Kingdom: 0628 476 741, West Germany: 02162-3798-0, France: (03) 956-8142, Italy: (02) 688-2141.

ZAX

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CIRCLE NO 45

Laser diodes prove useful in medium-haul, low-bandwidth applications

Tom Ormond, *Senior Editor*

Aimed at the optical disk marketplace, *the blue-light laser from Matsushita lases in the 390- to 420-nm wavelength range. Compared to the 780-nm lasers currently used with optical disks, the devices quadruple disk memory capacity.*

To many systems designers, laser diodes are viable optical sources only for long-haul applications involving bandwidths close to the gigahertz range. Laser diodes are still the only feasible source for such optical links, but they can also be effectively used as optical sources in a variety of medium-haul, low-bandwidth, cost-conscious applications. These applications include such areas as fiber-to-home systems, cable TV, local-area networks (LANs), bar-code scanners, and optical disks.

Each of these areas places different demands on a laser. In some cases, the operating requirements are not demanding and almost any laser will suffice. In others, the laser must meet stringent system requirements. Although some manufacturers have gone after all these application areas, others have concentrated their product offerings on one application.

Bringing fiber to the home

Future telecommunication systems will most likely send a variety of information—telephone, computer data, and cable television—from a central office downstream to the home. Because the upstream signals (those from the home to the central office) will carry less information than the downstream signals, the bandwidth capacity of short-wavelength lasers will be more than adequate.

To break into this application area, however, a manufacturer must offer a laser that is both inexpensive ($50 max) and highly reliable (lifetime of millions of hours). The laser must have a wide operating range, because it will be operating in an outdoor environment, and an output that is easily focused into a single-mode fiber. On the other hand, the output-power and speed requirements will be quite lax and well within the reach of almost any laser.

Aimed at fiber-to-home applications, Mitsubishi'S FU-01LSD-N laser meets these requirements. The device is available in versions that lase at 780 and 870 nm. At 25°C, those versions have lifetimes of 14 and 20 million hours, respectively. The lasers are housed in hermetically sealed packages that feature connectors compatible with single-mode fibers—the standard in long-wavelength systems.

The modules contain an AlGaAs laser diode and a photodiode that serves as an optical-output monitor. They have a low 30-mA typ threshold current and an output of 2.5 mW max from the connector port into a 10-μm core fiber. Rise and fall times are 0.5 nsec, and the operating range spans −20 to +50°C. The units are designed to operate in conjunction with the FU-03PD-N, a short-wavelength silicon PIN photodiode. Pricing is $342 (10) per pair for the 780-nm device and $472 per pair for the 870-nm unit.

Cable TV requires FM

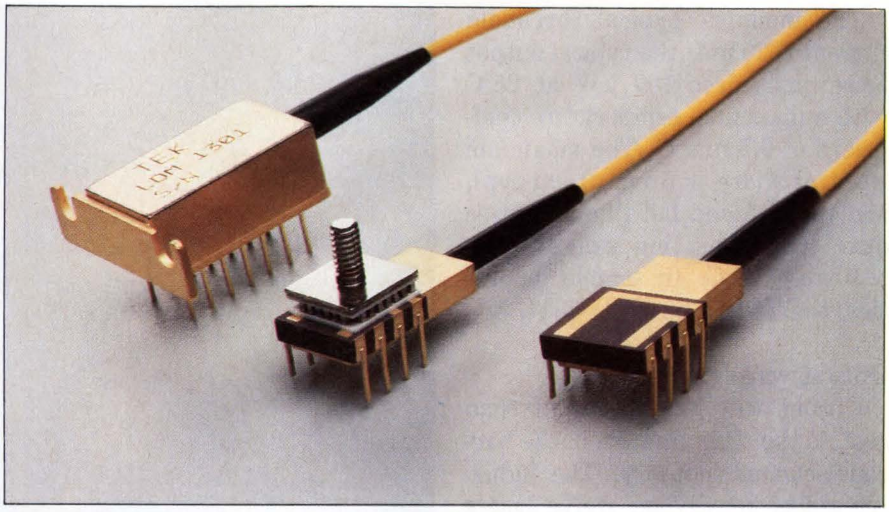
Current approaches to cable TV focus on both AM and FM. FM makes few technical demands, and almost any long-wavelength laser can handle it. But TV sets don't work with FM signals—they accept AM signals. To use FM approaches, you need a converter at each TV set to transform the FM transmissions to AM signals. This solution is thus not viable—the only option is to work directly with AM signals.

Working with AM signals places stringent requirements on the laser, and cable-TV requirements mandate the use of a long-wavelength laser that has an output power in the milliwatt range. The LDM 1301 laser module from Tektronix fits the bill.

Available in 14-pin DIPs, the LDM 1301 modules contain a buried heterostructure-type laser, a photo-

diode to monitor back-facet emission, a thermoelectric cooler (TEC), and a calibrated thermistor that allows designers to precisely control TEC operation. The typical lasing wavelength is 1300 nm; the typical threshold current measures 25 mA. The modules feature a minimum output power of 1 mW (2 mW max) and an output spectral width of 3 nm typ. The operating range is −40 to +70°C.

LDM 1301 modules costs $1395 and normally come with a single-mode fiber pigtail; connectors are available as an option. All devices go through a 250-hour, 70°C ambient burn-in test at a 100-mA forward current level.



Suitable for both analog and digital applications, *the LDM 1300 and 1301 laser modules from Tektronix lase at 1300 nm. Housed in the packages are the laser diode, a thermoelectric cooler, a monitor diode, and a thermister.*

Costs are critical with LANs

Laser costs must go down dramatically to make any penetration into LAN applications. However, because LANs are generally used indoors, operating temperature requirements are much less demanding than those for fiber-to-home applications. LANs will probably use multimode fiber rather than single-mode fiber, and this difference should help lower laser costs.

BT&D's LSC2300 laser diodes are well suited to the LAN operating environment. Available in both DIP and butterfly housings, the units contain a photodiode that monitors the laser output and a thermistor that monitors laser temperature. But, because the unit lacks a thermoelectric cooler, overall power dissipation is low.

The LSC2300 lases at outputs of 1280 to 1320 nm and operates over a −20 to +65°C range. Its costs $390 (1000). The typical threshold current is 20 mA, and the typical output spectral width measures 3 nm. The output power is 200 μW (−7 dBm), and modulation capability ranges to 1G bps. Maximum rise and fall times are 0.5 nsec, and the lifetime is 455,000 hours at 25°C. The 14-pin DIP housing incorporates a heat-sink mounting flange.

Toshiba also offers laser diodes that are well suited for LAN applications. The TOLD 321/323 compact modules (5.6-mm diameter base) incorporate a Fabry-Perot laser diode with a photodiode that monitors laser emissions. They lase at a nominal 1310-nm wavelength, feature a single-mode fiber pigtail, and are available in package styles that feature a flange to facilitate heat-sink attachment.

Laser technology meets microelectronics on a chip

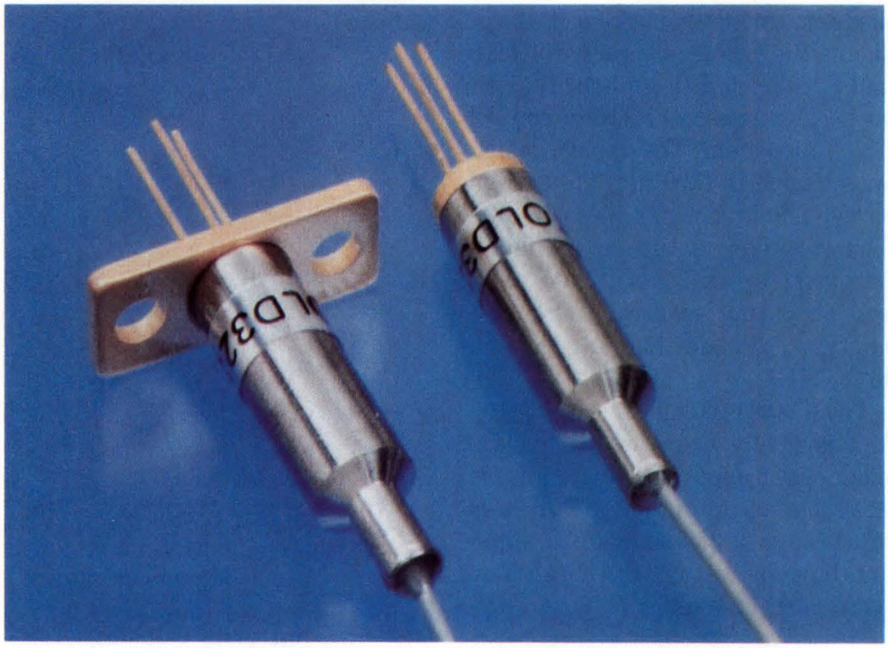
A monolithic optoelectronic transmitter capable of operating at speeds exceeding 2G bps has been processed by scientists at BNR, the research and development subsidiary of Northern Telecom. The single microchip merges laser technology with microelectronics and features two light-reflecting mirrors produced entirely by semiconductor processing.

The laser diode is the key component in the experimental transmitter. It is controlled by an array of on-chip transistors that receive external electronic digital signals. Combining two dissimilar physical structures—transistors and laser diodes—on a single chip was a major challenge for the development team and required the use of advanced fabrication techniques.

The chip's MESFETs are fabricated in GaAs. The laser diodes, made of multiple layers of GaAs and GaAlAs, are made using a technique known as molecular-beam epitaxy, or MBE. MBE can control the layer growth to within 0.5 nm—comparable to the distance between atoms in the semiconductor material. For example, this technique allows the building in layers of the light-emitting section of the laser to a thickness of only 20 atoms.

Air-bridge technology, a technique adapted specifically for this chip, couples the transistors and diodes together using special metal interconnects that measure only 2 μm wide. The air bridges, supported above the GaAs chip by posts, minimize drag on signal-carrying electrons and allow them to move faster than they would through conductors deposited directly on the chip's surface.

The modules' typical threshold current is 20 mA; the typical output power measures 100 μW at 25°C with a maximum temperature coefficient of 0.5 nm/°C. The maximum spectral width is 6 nm (3 nm typ), and the rise and fall time is 1 nsec max. The operating range spans −10 to +65°C. In sample quantities, the TOLD 321 costs $841.



Well-suited for LAN applications, *the TOLD 321/323 compact modules (5.6-mm diameter base) from Toshiba incorporate a Fabry-Perot laser diode with a photodiode that monitors laser emissions and feature a single-mode fiber pigtail. They lase at a nominal 1310-nm wavelength and are available in package styles that feature a flange for making heat-sink attachment easier.*

Output wavelength is key

Output wavelength, rather than cost, is the main concern in the bar-code-scanner industry. The industry relies heavily on HeNe lasers that generate red light. All the inks specified for the bar-code labels are highly sensitive to this wavelength (approximately 670 nm). Changing the label's makeup would be fairly simple, but there's an old saying—"If it ain't broke, don't fix it." To have any impact in bar-code-scanner applications, a laser diode must lase at the HeNe wavelength.

The output wavelength of a laser diode is also the main concern in optical-disk applications. Storage capacity is a direct function of spot size, which, in turn, is a direct function of the laser's operating wavelength. The lower the operating wavelength, the smaller the spot size and the larger the disk's storage capacity.

Laser diodes currently used in optical-disk applications have output wavelengths of 780 or 820 nm. For a 780-nm wavelength, the spot

For more information . . .

For more information on the laser diodes described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

AT&T Microelectronics
555 Union Blvd
Allentown, PA 18103
(800) 372-2447
Circle No 700

BNR
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Research Triangle Park, NC 27709
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BT&D Technologies
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Wilmington, DE 19803
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Circle No 702

Matsushita Electric Corp of America
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Circle No 703

Mitsubishi Electronics America Inc
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Sunnyvale, CA 94086
(408) 730-5900
TLX 172296
Circle No 704

Tektronix Inc
Hybrid Components Operation
Beaverton, OR 97077
(503) 627-4220
Circle No 705

Toshiba America Inc
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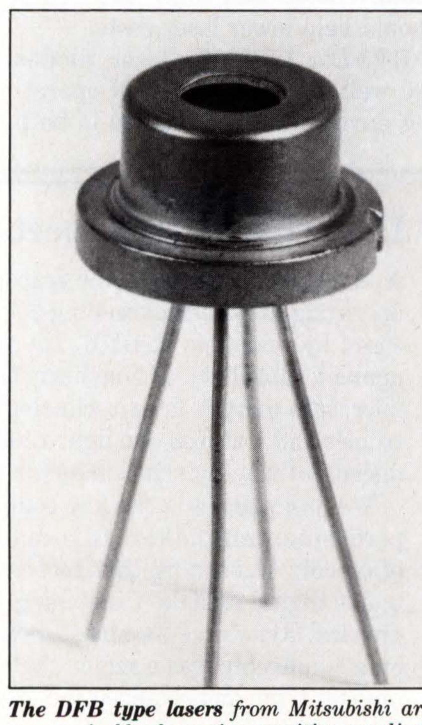
Deerfield, IL 60015
(312) 945-1500
FAX 312-945-1044
Circle No 706



The DFB type lasers *from Mitsubishi are very suitable for noise-sensitive applications, including multichannel cable-TV distribution.*

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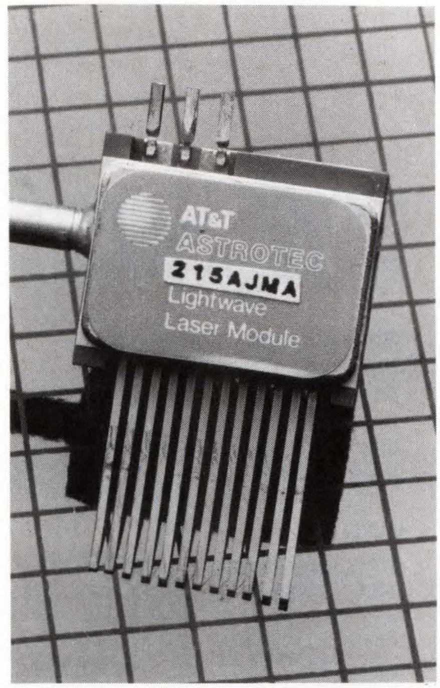
size measures 12 cm in diameter. Matsushita has introduced a blue-laser module that combines an optical-waveguide-type second-harmonic-generation (SHG) element with a laser-diode chip. This module has a 390- to 420-nm output wavelength. At 420-nm wavelengths, the optical spot size equals 6 cm—by cutting the spot size by 50%, the Matsushita device quadruples memory storage capacity.

The module actually uses an infrared-type (840-nm output) laser. The SHG element emits light at half the laser's wavelength to produce the final 420-nm module output. Conventional bulk SHG elements have a conversion efficiency (the ratio of optical harmonic wave to fundamental wave) of approximately 0.01%. Matsushita's manufacturing process yields SHG elements with a conversion efficiency of 1% to 2%. Sample modules will be available for approximately $11,000.

Another product designed for telecommunications is the AT&T 215-Type laser module. The modules are internally cooled InGaAsP single-mode injection lasers designed for 1.3-μm wavelength applications. They offer data-rate capabilities of 417M to 1700M bps with typical launched power ranging to 4 dBm (2.5 mW).

The modules are housed in a 12-pin, hermetic ceramic SIP equipped with a type 5D, 8-μ core single-mode fiber pigtail that's terminated with an AT&T 2016A biconic connector. A separate input for high-bit-rate modulation signals is specially designed to have a nominal 25Ω impedance.

An integral TEC provides stable thermal characteristics. Working in combination with external control circuitry, the TEC can maintain laser temperature at 25°C, offsetting case temperatures reaching as high as 65°C or as low as −40°C. Laser temperature is monitored internally for feedback and control purposes. The 215-Type lasers are designed to be used with a heat sink attached to the base of the module.



Designed for 1.3-μm wavelength telecommunications applications, *the AT&T 215 Type laser modules offer data-rate capabilities from 417M to 1700M bps with typical launched power ranging to 4 dBm (2.5 mW). They are housed in a 12-pin, hermetic ceramic SIP with a separate input for high-bit-rate modulation signals.*

An internal InGaAsP PIN photodiode, mounted directly behind the laser diode, functions as a power monitor. The photodiode monitors emissions from the rear facet of the laser; combined with external circuitry, the diode maintains a constant level of laser output power into the fiber pigtail. All devices go through a 100% burn-in test. Laser prices start at $1300 (OEM qty).

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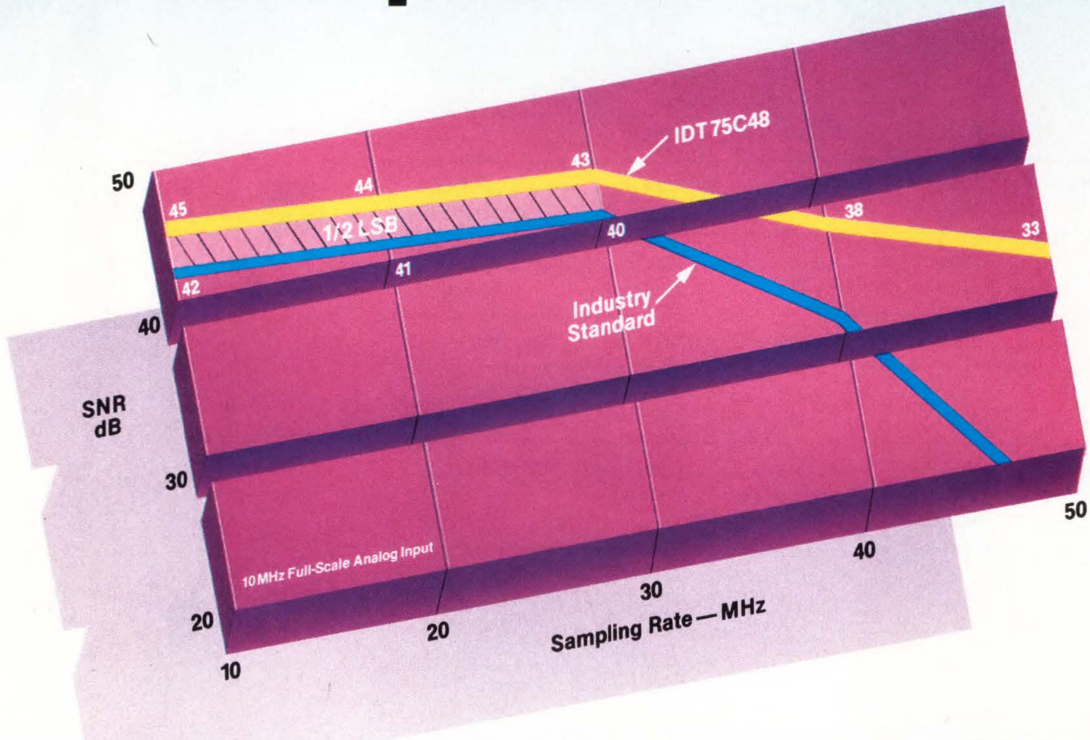

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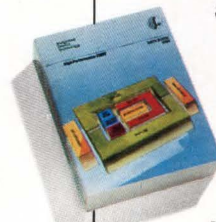

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Color-palette chips bundle extra features with RAM look-up table and DACs

Margery S Conner,
Regional Editor

Today's color palettes feature faster D/A converters (DACs), larger look-up tables, and a handful of special features such as overlay registers and selectable DAC resolution. These enhancements can help your graphics-display design satisfy the end user's ever-growing appetite for higher resolution and more colors.

Color-palette basics

A color palette basically comprises a RAM look-up table and one or three DACs **(Fig 1)**. Although color palettes with 4-bit DACs are available, they have largely been superseded by 6- and 8-bit DACs in current designs. The palette takes the contents of each pixel from the frame buffer and converts the digital representation of the pixel's color into an analog signal that drives the display **(Fig 2)**.

The maximum speed at which the palette can take pixels from the frame buffer and convert them to an analog video signal is the clock rate. You can calculate the palette clock rate for your display by multiplying the total number of pixels on the screen (the x resolution times the y resolution) by the 60-Hz refresh rate, and then adding about 30% for the horizontal and vertical refresh time **(Fig 3)**.

A pixel's color is determined by the bits stored at the pixel's address in the frame buffer. The pixel's contents don't drive the DACs directly—they are pointers to colors in the RAM look-up table. The width of the look-up table in a triple-DAC palette is three times the DAC's resolution; the first third of the look-up table entry controls the red DAC, the second third controls the blue DAC, and the third third controls the green DAC. The number of bits in register controls the total palette size.

For example, the IBM PS/2 VGA uses an Inmos IMS-G171, a triple 6-bit DAC color palette, which results in an 18-bit wide look-up table, allowing a total palette size of 262,144 colors. In its 640×480 mode, the VGA has 4 bits/pixel, which limits the display to 16 colors that can be displayed at once. In

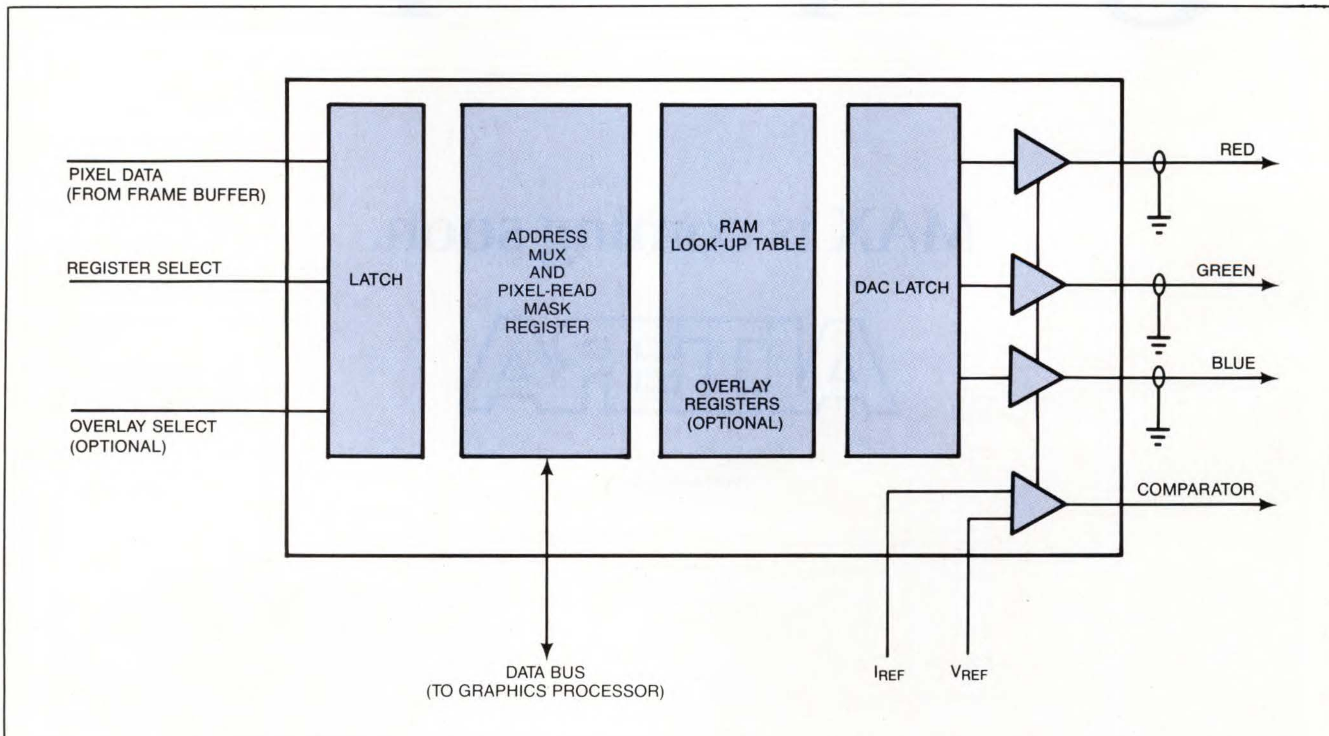

*Fig 1—**A color palette basically comprises a RAM look-up table** and one or three high-speed video DACs. The graphics processor reads colors in the palette and writes new colors to it over the data bus. Palettes may also incorporate overlay registers to create overlay planes of graphical entities such as icons and cursors.*

the VGA's 320×480 mode, the color resolution is 8 bits deep, so 256 colors of the 256,000 available can be displayed simultaneously.

Eight bits per pixel gives a markedly better picture than four bits per pixel, but your eye can still see a difference. It's not until you have 24 bits per pixel that you achieve true color. However, you can cause more than 256 colors to display on the screen at once by changing the colors associated with each address in the look-up table. You can change the colors as often as once every scan line. This technique is called "pseudocolor."

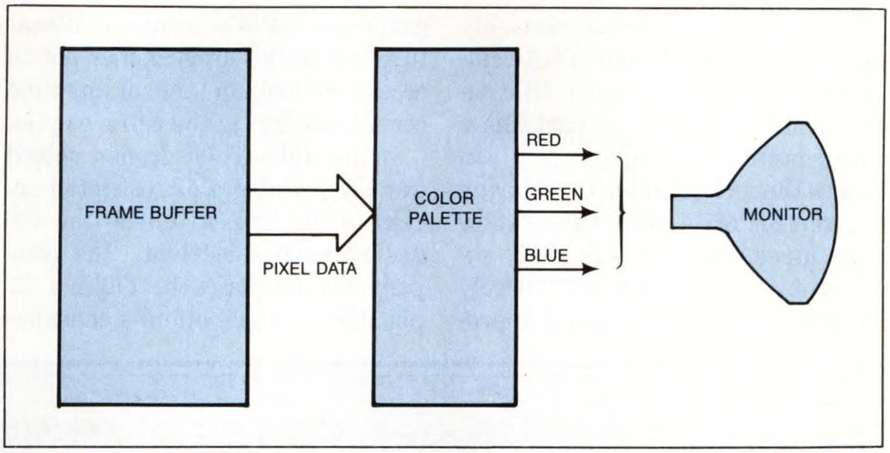

Fig 2—In a simple graphics display, *the bit pattern stored in a pixel address in the frame buffer (the video portion of the graphic processor's memory) serves as a pointer to the color palette's look-up table. High-speed video DACs on the palette convert the digital data to analog signals, which drive the monitor.*

Changing the look-up-table colors, although it's not complex, is a multistep process. You must first specify the starting pixel address while the palette is in write mode ($RS0+RS1=\overline{WR}=0$). The palette stores this address in the pixel-address register. Then you set $RS0=1$ and write the three separate data words of the red, blue, and green color-definition data. The palette collects these three 6-bit values together in the color-value register and concatenates them into an 18-bit word. The palette transfers this value to the address specified in the pixel-address register. After the transfer, the pixel-address register autoincrements, changing consecutive pixel addresses without the graphics processor's specifying each address.

The third option is the fastest method of the three: You can use the pixel mask to change selected bits of the pixel-address value applied to the pixel-address inputs (P_{0-7}), thereby changing the color of a particular pixel without changing either the frame buffer or the look-up table. A one in a bit position leaves the corresponding bit in the pixel address unchanged, while a zero sets that bit to zero.

In sum, there are three ways to change the color of a pixel: You can change the pixel's value in the frame buffer, change the contents of the look-up table, or mask the pixel address.

If you want your graphics-display design to be compatible with IBM's relatively low-resolution (640×480 pixels) VGA standard, you should be aware of the tradeoffs of using standard and nonstandard palettes. If you're designing a relatively high-resolution display, say, greater than 1k×1k pixels, you'll probably be most interested in a palette with such enhancements as extra speed and overlays.

If your graphics-display design absolutely must be VGA compatible, you can choose one of two color palettes: the Inmos IMS-G171/176/178 (the 171 is the color palette in IBM's PS/2) or the Brooktree Bt471/478 (or the ADV471/478 from Brooktree's licensed alternate source, Analog Devices.) **Table 1** lists these and other color palettes.

The Inmos part has many imitators, but no company is licensed to clone it, so none of the imitations are guaranteed to be exactly the same as the original. National, Triad, and VLSI Design Associates make pin-compatible parts aimed at the lucrative VGA-clone market.

In addition to its triple 6-bit DACs, the IMS-G171 has a 256×18-bit RAM look-up table, and it oper-

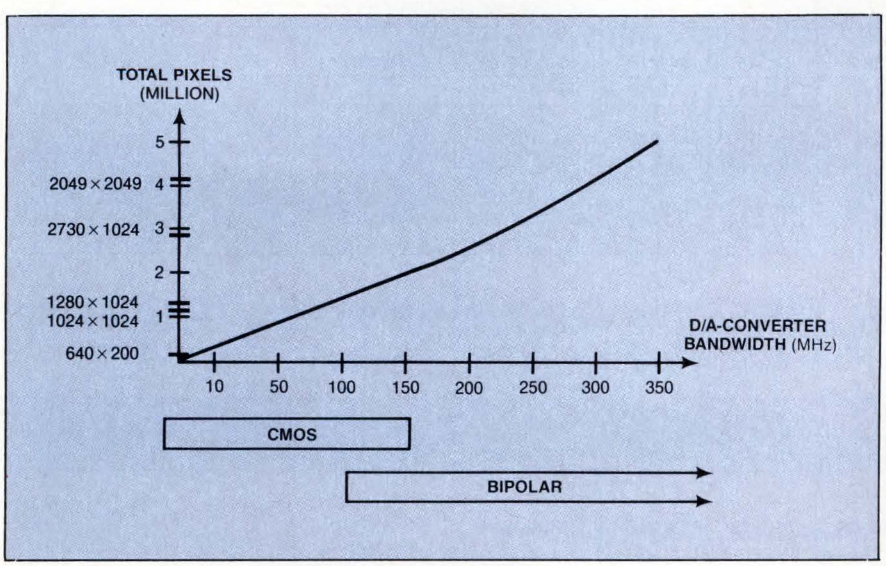

Fig 3—Plotted above is the color-palette DAC bandwidth *required for common display resolutions. The bandwidth calculations shown assume that the refresh rate is 60 Hz and that the horizontal and vertical retrace take 30% of each frame time.*

ates at 50 MHz. Don't slavishly choose the 171 for your VGA-compatible design just because IBM selected it, however. The part has a major problem: It requires that you access the look-up table only during the retrace cycle—otherwise, snow may appear on the CRT. IBM's solution to this problem was merely to pass it on to the application programmer—IBM's technical literature warns the programmer not to access the look-up table at any time other than during the retrace cycle.

In its IMS-G176, Inmos solved the 171's problem of restricted access to the look-up table—the 176 has no such constraint. The company also produces the 176 in a 32-pin PLCC, which offers a considerable space savings over the 171's 28-pin DIP package.

Dean Hayes, the engineering manager at Video-7 (Fremont, CA) who was responsible for the design of his company's VGA board, walked a fine line. On one hand, Hayes was required to make the board 100% hardware compatible with IBM's standard, a requirement

TABLE1—6- AND 8-BIT COLOR PALETTES

MANUFACTURER/ PART NO	DAC ORGANIZATION	SPEED (MHz)	RAM SIZE	OVERLAY SIZE	PACKAGE	PRICE*	COMMENTS
ADVANCED MICRO DEVICES							
Am81C458	TRIPLE 8-BIT	80, 110, 125	256×24	4×24	84-PIN PGA	$105, $112, $119	
ANALOG DEVICES							
ADV471	TRIPLE 6-BIT	35, 50, 80	256×18	15×18	44-PIN PLCC	$29, $36, $57	THE AD471/478 IS A LICENSED ALTERNATE SOURCE OF THE Bt471/478
ADV478	TRIPLE 8-BIT	35, 50, 80	256×24	15×24	44-PIN PLCC	$41, $51, $89	
BROOKTREE CORP							
Bt453	TRIPLE 8-BIT	40, 66	256×24	3×24	40-PIN DIP OR 44-PIN PLCC	$47, $62	
Bt457	SINGLE 8-BIT	80, 110, 125	256×8	4×8	84-PIN PLCC OR PGA	$64, $79, $93	
Bt458	TRIPLE 8-BIT	80, 110, 125	256×24	4×24	84-PIN CERAMIC PGA	$140, $170, $190	
Bt459	TRIPLE 8-BIT	80, 110, 135	256×24	16×24	132-PIN PGA	$134, $158, $191, $232	
Bt461	SINGLE 8-BIT	80, 110, 135, 170	1024×8	256×8	132-PIN PGA	$134, $158, $191, $232	
Bt471	TRIPLE 6-BIT	35, 50, 66, 80,	256×18	15×12	44-PIN PLCC	$19, $22, $27, $57	
BT473	TRIPLE 6- OR 8-BIT	35, 50, 66, 80	256×24	15×8	68-PIN PLCC	$54, $60, $72, $178	DEDICATED RAM LOOK-UP TABLE FOR EACH DAC
Bt478	TRIPLE 6- OR 8-BIT	35, 50, 66, 80	256×24	15×24	44-PIN PLCC	$27, $30, $36, $89	SELECTABLE DAC RESOLUTION
Bt492	SINGLE 8-BIT	360	256×8	16×8	68-PIN CERAMIC PGA	$307	
HONEYWELL INC							
HDAM51100	SINGLE 8-BIT	125	512×8	NONE	46-PIN PGA	$103.43	
HDAM51200	SINGLE 8-BIT	165	512×8	NONE	46-PIN PGA	$131	
INMOS CORP							
IMSG171	TRIPLE 6-BIT	50	256×18	NONE	28-PIN DIP	$10 (100,000)	
IMSG176	TRIPLE 6-BIT	65	256×18	NONE	28-PIN DIP OR 32-PIN PLCC	$10 (100,000)	
IMSG178	TRIPLE 6- OR 8-BIT	65	256×24	NONE	28-PIN DIP OR 32-PIN PLCC	$14 (100,000)	
NATIONAL SEMICONDUCTOR INC							
DAC 0630	TRIPLE 6-BIT	30	256×18	NONE	28-PIN DIP OR 32-PIN PLCC	$9 (1000)	
DAC 0631	TRIPLE 6-BIT	50	256×18	NONE	28-PIN DIP OR 32-PIN PLCC	$9 (1000)	
TRIAD SEMICONDUCTORS INC							
TR9C1710	TRIPLE 6-BIT	35, 50, 66	256×18	NONE	28-PIN DIP	$24, $28, $40	
VLSI DESIGN ASSOC INC							
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CIRCLE NO 50

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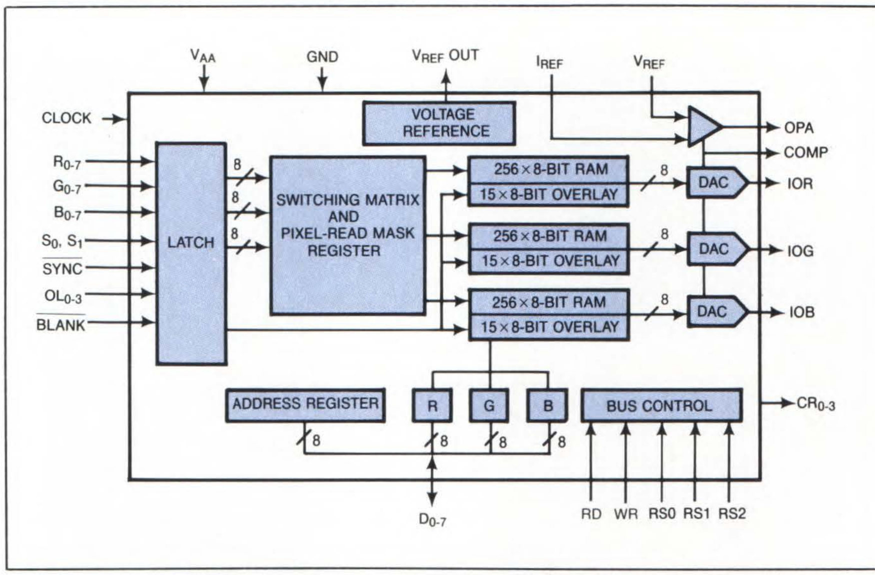
that would seem to mandate the use of the 171. On the other hand, he didn't want snow on the display's CRT. He was reluctant to select the Brooktree Bt471/478 or the Analog Devices ADV471/478, however, because, although they're functionally compatible with the Inmos parts, the 471 and 478, with their advanced capabilities, require different pinouts.

Hayes chose to design the board with the 176. Because Inmos manufactured both the 176 and 171, he could be sure that Video-7's board would be compatible with IBM's VGA. The Brooktree parts could offer enhanced capability, but compatibility with IBM's VGA was Video-7's primary concern. Says Hayes: "Even if the IBM VGA had bugs [other than the snow], I wanted to have the exact same bugs."

The size of the parts also affected Hayes's decision. Both Analog Devices' and Brooktree's parts are larger than the Inmos part. The Bt471/478's package, a 44-pin PLCC, was a drawback on an already crowded board—it requires almost 1/2 in². By contrast, the IMS-G171/176 fits into either a 28-pin DIP or a 32-pin PLCC; the 32-pin package requires only about 1/4 in².



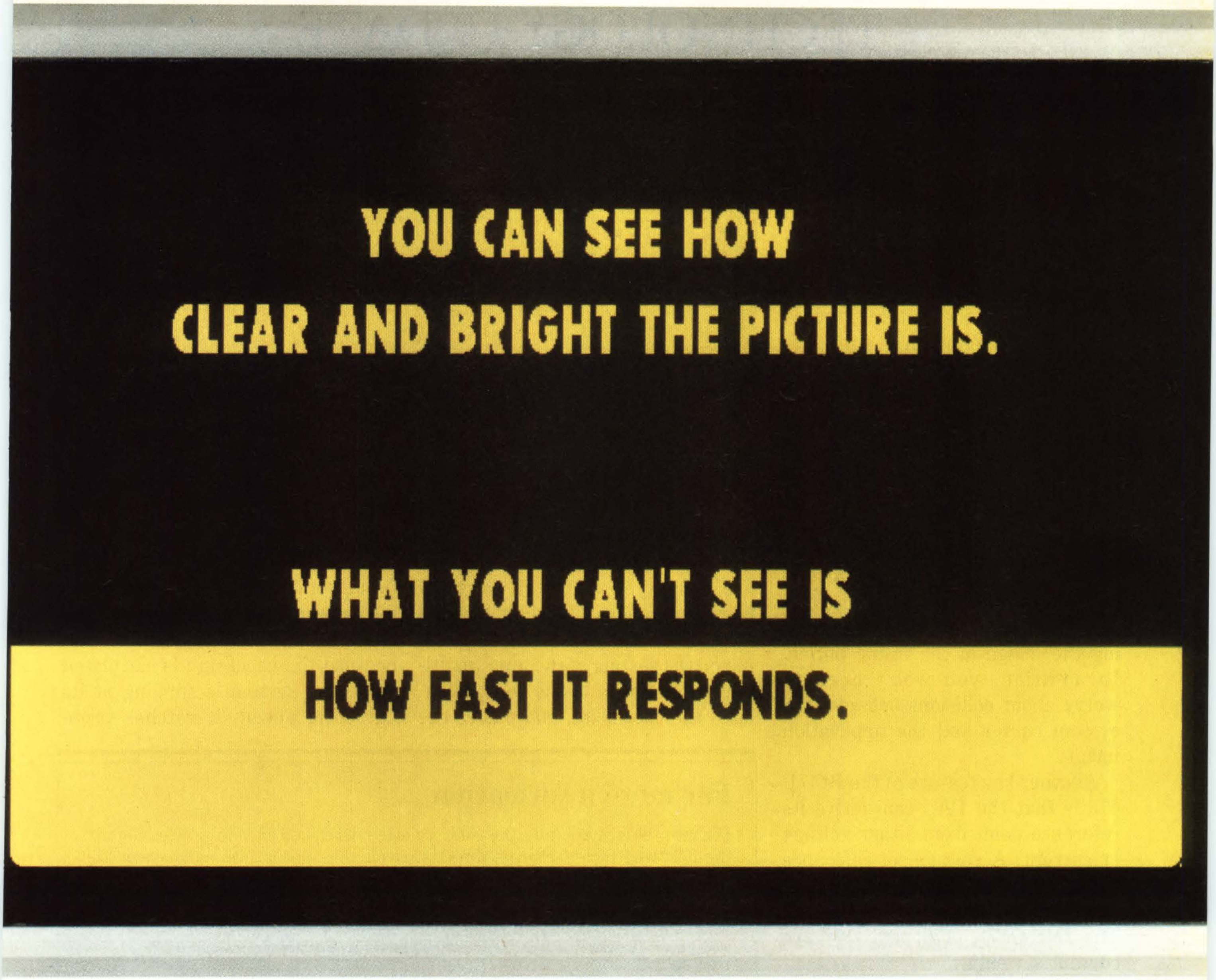
Each DAC in this color palette *has its own 256 × 8-bit RAM look-up table. The palette (the Bt473) can accommodate three 8-bit-wide pixel inputs, and it supports 24-bit true-color graphics.*

The 6-bit ADV471 and the 8-bit ADV478 *from Analog Devices feature internal RAM, which permits a 256-color palette. They also have separate RAM, which allows an overlay of as many as 15 colors.*

Because it incorporates the 171, IBM's VGA is limited to 6 bits of color per pixel. The Bt471/478 was the first palette to offer software-selectable 6- or 8-bit resolution. Inmos picked up this feature and incorporated it in the IMS-G178 palette. The part, which maintains compatibility with the 171 and 176, will sell for about 35 to 40% more than the IMS-G176.

If it's vital that your design exactly duplicate IBM's standard, you may be better off going with the IMS-G176 or one of its clones. However, if you want to offer a board that features VGA compatibility, yet goes considerably beyond the VGA in performance, you should consider using the palettes from Brooktree and Analog Devices. It's easy to forget that many end users of graphic displays are not constrained to use EGA/VGA standard parts.

The look-up table in the Bt471/478 has separate registers for generating overlays. The Brooktree parts have overlay-selection lines, driven by the system processor's address lines, that specify whether



Fast response time, less than 5 ms, gives Finlux Electroluminescent displays video capability. In laptop PCs, the cursor is visible during all rapid movements or data changes.

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The display above is shown as large as life. Just 18 mm thin and weighing less than 500 grammes, this Finlux EL shows as much text as an 11" CRT: 25 lines of 80 characters, or full graphics. Finlux EL displays are available in a range of 320 x 256 to 640 x 400 pixels.

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Telex 125023 ldis sf

In the USA:
FINLUX INC.
20395 Pacifica Drive
Suite 109
Cupertino, CA 95014, USA
Telephone (408) 725-1972
Telecopy (408) 996-7547

CIRCLE NO 51

the color information for a pixel will come from the palette or the overlay register. (It's these extra pins, which address the overlay registers, that add to the pin count on the Bt471/478 and increase the chip size over that of the Inmos part.)

Overlays allow the system software to control the system graphics elements independently from the application-software graphics. System software displays basic, relatively unchanging graphic elements such as cursors, screen frames, and system messages; application software manipulates a variety of changing graphical information.

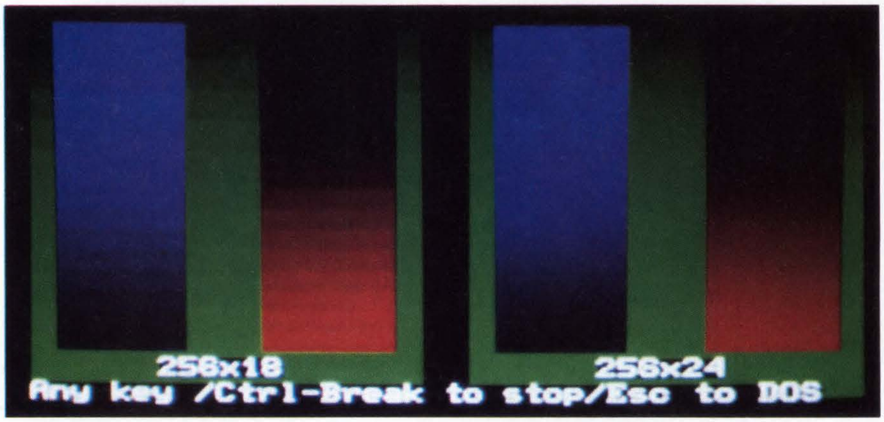
By overlaying one or more separate graphics planes that display system information, you can avoid the time-consuming job of modifying the image in the frame buffer. In addition, you won't need to worry about collisions between the system cursor and the application image.

Another key feature of the Bt471/478 is that the DAC can derive its reference point from either voltage or current. A voltage-set reference requires fewer parts and is more stable than a current-set reference. The IMS-G171, -176, and -178 are current-set only.

To design displays with resolutions greater than that of the VGA, you'll need to use a palette with a clock speed well in excess of 100 MHz. The Bt459 has a maximum speed of 135 MHz, which puts it near the top of the speed range for triple DAC palettes.

Testability is a key consideration for any design, but testing color palettes can be doubly painful because of their combination of digital and analog circuitry. Brooktree eases this test chore for designers who use the 459 by including two types of on-chip diagnostics. The chip can perform the diagnostics on itself as well as help isolate problems in the surrounding board circuitry.

The part helps diagnose digital problems by running a checksum on a frame of data. (A frame of data is the contents of the pixels that are displayed between vertical blanking signals.) The chip catches every fourth or fifth pixel (depending on the setting of the input multiplexer) just prior to the DAC, calculates the checksum, and makes the results available at the system-processor data port. By varying the bit pattern in the frame buffer, you can isolate bad memory chips. And because the checksum is calculated while the system is running at its operating speed, it catches prob-



This photo shows the difference *between 6-bit and 8-bit RAMDAC resolution. A RAMDAC with 6-bit resolution over 25% of the brightness range (from 1/4 to 1/2 bright) produced the left side of the photo. On the right is the smooth shading produced by an 8-bit RAMDAC over the same range. (Photo courtesy Brooktree Corp)*

For more information . . .

For more information on the color palettes described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Advanced Micro Devices Inc
901 Thompson Pl
Sunnyvale, CA 94088
(408) 732-2400
Circle No 708

Analog Devices
One Technology Way
Norwood, MA 02062
(617) 329-4700
TWX 710-394-6577
Circle No 709

Brooktree Corp
9950 Barnes Canyon Rd
San Diego, CA 92121
(619) 452-7580
FAX 619-452-1249
Circle No 710

Fujitsu Microelectronics Inc
3545 North First St, Bldg 1
San Jose, CA 95134
(408) 922-9380
FAX 408-432-9044
Circle No 711

GE/Intersil
2450 Walsh Ave
Santa Clara, CA 95051
(408) 996-5059
Circle No 712

Honeywell Inc
Signal Processing Technologies
1150 E Cheyenne Mountain Blvd
Colorado Springs, CO 80906
(303) 577-1000
FAX 303-577-3716
Circle No 713

Inmos Corp
Box 16000
Colorado Springs, CO 80935
(303) 630-4000
TWX 910-920-4904
Circle No 714

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95052
(408) 721-7000
TWX 910-339-9240
Circle No 715

Triad Semiconductors Inc
5575 Tech Center Dr
Suite 120
Colorado Springs, CO 80919
(719) 528-8574
FAX 719-528-8875
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VLSI Design Associates
910 Campisi Way
Campbell, CA 95008
(408) 371-7400
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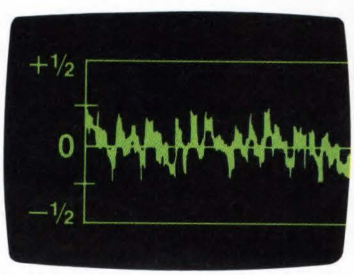

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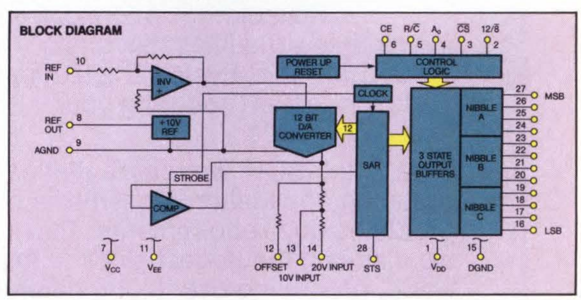

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lems that may only be apparent at that speed.

So that you can check the analog portion of the device and its surrounding circuitry, the part has on-chip comparators that allow you to compare the output of a DAC with either of the other two DACs or with the DAC reference voltage. By comparing the DAC outputs, the chip checks for gross functionality and makes sure that signals are propagating through the chip.

By comparing full-scale DAC outputs to the DAC reference voltage, you can tell if the monitor is properly connected to the system. Analog graphics systems are terminated with two 75Ω resistors in parallel—one at the output of the DAC and one at the monitor's input. If the monitor is not connected, the voltage is twice as high at the DAC as it would be if the monitor were correctly terminated. Note that 80% of the problems in graphics systems are related to the monitor—either the monitor is bad, or, what's even more likely, a cable or a plug is defective. You can use this same method for checking the monitor by manually comparing the DAC output to the reference voltage.

For displays that require faster palette clock rates than the 459 provides, you'll need to switch to a single-DAC palette, such as the HDAM 51200 from Honeywell, which has a top speed of 165 MHz, or the Brooktree Bt492, which has a maximum speed of 360 MHz. If your display must run faster than 360 MHz, you won't be able to use a color palette at all; instead, you'll need to build your video-interface portion from discrete components. Discrete video DACs fabricated in bipolar technology can reach speeds in excess of 360 MHz. EDN

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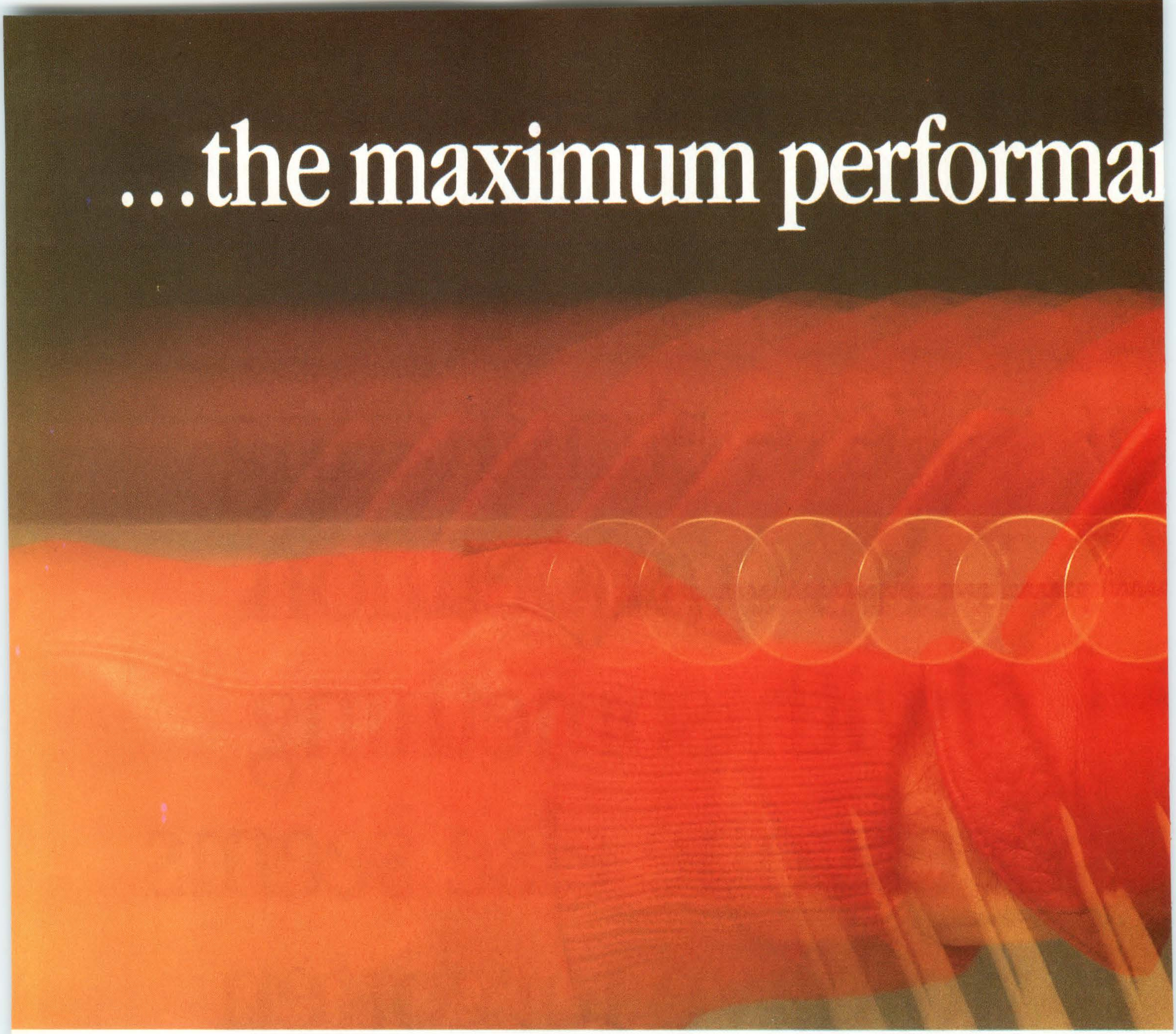

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PLESSEY KEY PROCESS TECHNOLOGY

BIPOLAR

DESCRIPTION	F_t	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14µm	1
High voltage	400MHz	20µm	1
High speed linear	4.5GHz	4µm	2
High speed digital	6GHz	3µm	2
Ultra-high speed	14GHz	0.6µm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4µm	3-10V
JG Double SiGate NMOS	10MHz	6µm	9-18V
VB High speed CMOS	40MHz	2µm	3-5V
VJ Very fast CMOS	50MHz	1.5µm	3-5V
VQ Ultra fast CMOS	75MHz	1.2µm	3-5V
MH/MA SiGate CMOS	30MHz	4µm	3-15V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5µm				
CDI FAB I	3.75µm	11.5µm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5µm	8µm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5µm	8µm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5µm	6µm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2µm	4.5µm	200ps	0.2pJ	0.14pJ

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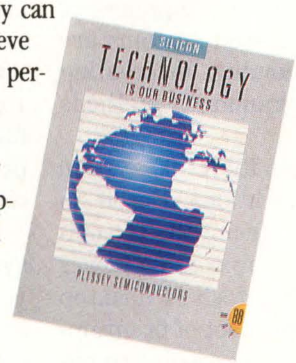

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Number 1 for ASICs

CIRCLE NO 53

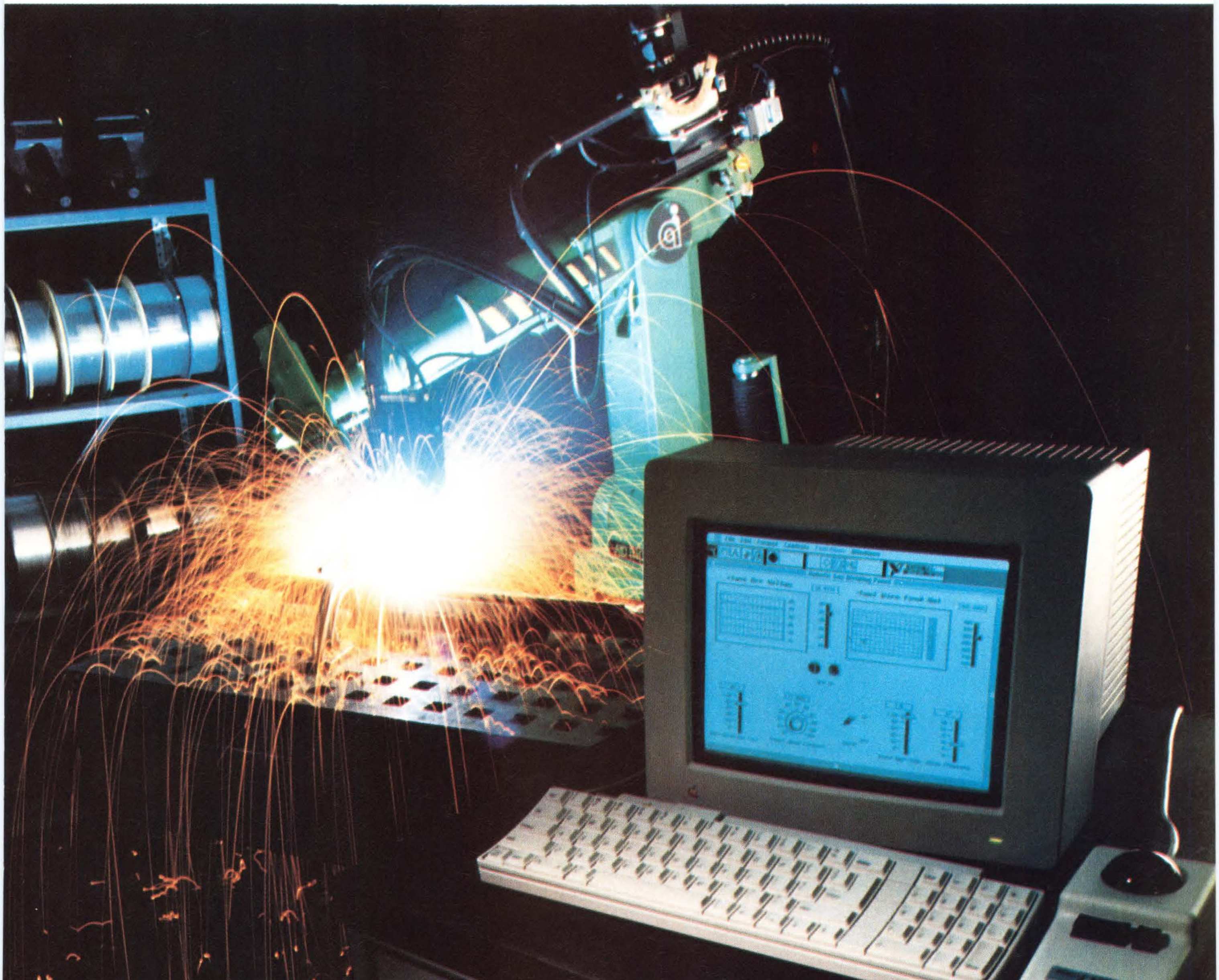
PC-based test systems and equipment dominate industrial applications

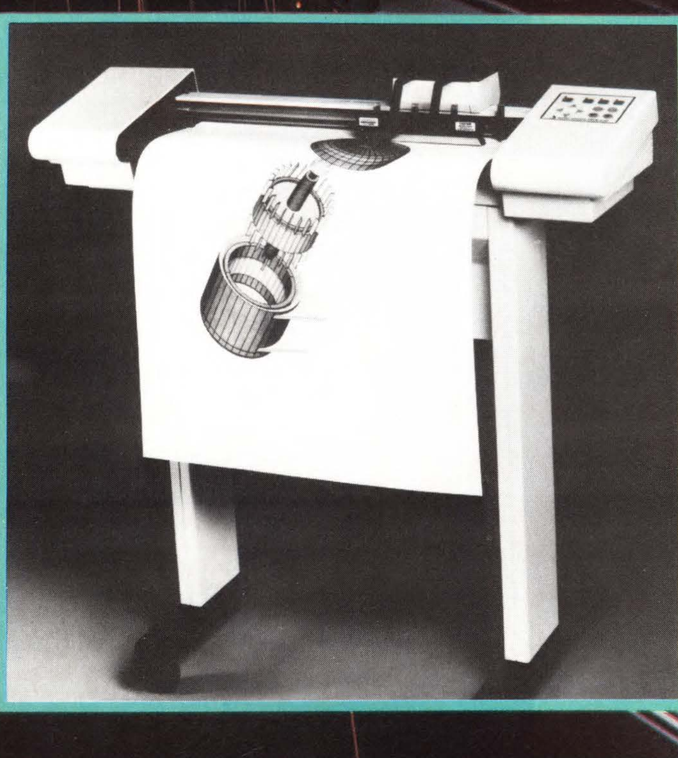
The industrial personal computer is becoming an important tool in factory automation, but several factors have slowed the PC's penetration into the manufacturing environment. Although the PC has gained ground in specific applications, many of its industrial implementations are too proprietary for general use. Some implementations don't have enough power at an affordable price, and others are unnecessarily intimidating to the average factory worker. However, suppliers of PC-based test equipment and automated systems are taking steps to remedy these shortcomings by creating graphics-based software and programming methods that ease the worker's task.

For example, Automatix Inc offers its AI-90 system for use in a variety of factory applications. Based on an industrial version of the Apple Macintosh II computer, the AI-90 combines significant processing power with the recognized ease of the Macintosh II desktop interface. Instead of learning a complex set of programming commands, the operator has only to point to on-screen icons via a mouse, trackball, or touch-screen interface. Such capabilities greatly minimize training time and expense by providing a user-friendly interface that is easy to learn. Moreover, the AI-90 is versatile. You can use it as a cell controller, as an intelligent shop-floor terminal, as a test-stand controller, or as a general-purpose PC suitable for an industrial environment.

Apart from the control field, CADKey Inc and Browne & Sharpe Manufacturing Co have combined their respective strengths in CAD software and coordinate measuring equipment to provide a PC-based system that generates an accurate blueprint of an object—without the original specifications on hand. The CADD-Inspector not only provides this *reverse-engineering* function, but it's also usable in the normal inspection process to compare a manufactured part with its CAD-compatible design.

And, this showcase doesn't confine itself to high-level systems only. In this roundup of industrial products, you'll find numerous examples of other equipment and components. Included are such products as transducers, switches, oscilloscopes, printers, semiconductor modules, power supplies, data recorders, and video monitors, to name just a few. You may very well find just what you've been looking for.

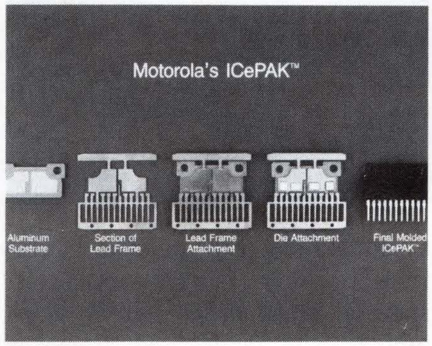





EG&G RETICON

H-bridge power module features current sensing and package isolation

Fabricated in the company's TMOS technology, the MPM3002 is an H-bridge power module with current-sensing capability. The module features a space-saving isolated package that eliminates the need for isolating hardware and reduces assembly costs. Designed for applications in servo motor drives, stepper-motor controls, and switching power supplies, the MPM3002 is rated at 100V, 8A. It has a power rating of 62.5W at a case temperature of 25°C, and an isolation voltage rating of 2000V rms.



The H-bridge consists of p-channel power MOSFETs in the upper legs of the bridge. It simplifies the drive circuit and n-channel SenseFETs in the lower legs of the bridge, allowing cycle-by-cycle current sensing that is essentially lossless. The n-channel and p-channel pairs of the MPM3002 are die-bonded to separate copper lead frames. An insulating material isolates the lead frames from the aluminum case.

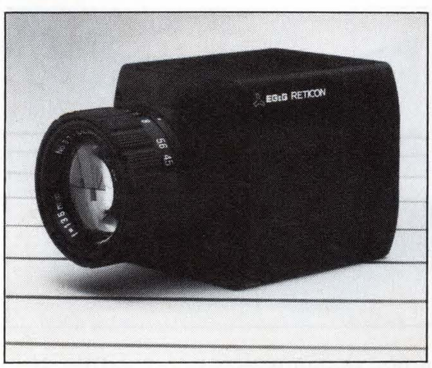
Additional electrical characteristics include a drain-to-source on-resistance of 0.15Ω max at 4A, an input capacitance of 900 pF max, and p-channel rise and fall times of 130 and 60 nsec, respectively. The MPM3002 costs $9.57 (100). Sample quantities are available from stock; production quantities have 6-week lead times.

Motorola Inc, Technical Information Center, Box 52073, Phoenix, AZ 85072. Phone (602) 244-4911.

Circle No 663

Industrial line-scan camera features video data rates to 10 MHz

Designed to operate in harsh industrial environments while delivering laboratory precision, the LC1901 line-scan camera is housed in a lightweight, but rugged, aluminum enclosure. The camera's internal construction utilizes shock-absorbing interconnection materials and features hybrid circuits that are laminated onto aluminum mounting plates for efficient heat transfer. The camera can withstand shocks of 100g peak and random vibration in excess of 20g rms.



The LC1901 senses light input from a scene and converts it into an analog video signal, the amplitude of which is a linear function of the scene's incident illumination. An electronic shutter and antiblooming structures within the sensor ensure performance over a wide range of lighting conditions. The camera is available with 256, 512, 1024, or 2048 photo-element arrays to satisfy the most stringent spatial resolution and speed requirements.

Three externally generated, differential-input signals control the camera operation. The frequency of the master clock determines the video data rate; the period of the line-transfer input defines the line-scan rate; and the line-reset signal, in conjunction with the line-transfer input, controls the integration period. This arrangement allows video data rates as high as 10 MHz, line rates exceeding 35,000 scans per second, and provides electronic exposure control.

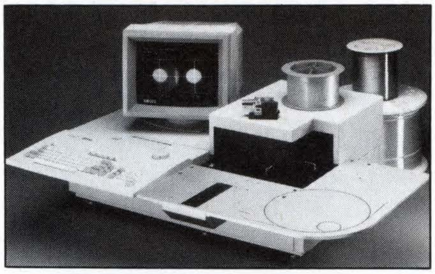
Additional specifications for the LC1901 include a 2000:1 dynamic range, a video level of 1.1V into a 100Ω line, and a 48-dB signal-to-noise ratio. The camera operates from supplies of 12V at 295 mA, −12V at 70 mA, and 5V at 350 mA. The LC1901 costs $1385.

EG&G Reticon, 345 Potrero Ave, Sunnyvale, CA 94086. Phone (408) 738-4266.

Circle No 661

Automated production tester characterizes optical fiber and cable

Designed for the high-volume production environment, the Model 2210 automated optical-fiber analysis system provides manufacturers of optical fiber and cable with a high-speed, high-repeatability system for characterizing both multimode and single-mode fibers.



The 2210 performs multimode spectral attenuation measurements from 800 to 1600 nm with an automated serpentine mandrel in accordance with CCITT- and EIA-recommended methods. An optical far-field scanner helps you make numerical aperture measurements and determine the appropriate mandrel setting.

The tester measures three single-mode optical-fiber characteristics that manufacturers monitor in statistical quality assurance programs: spectral attenuation, cutoff wavelength, and mode-field diameter (performed with an optional variable aperture unit). The 2210 incorporates a fiber preparation system that reduces cleaving and alignment time per fiber to less than 30 sec, and complete measurement time to less than 2 minutes.

The 2210 system is PC/XT compatible and is equipped for data communications via an RS-232C or an optional IEEE-488 interface. The test data is logged on MS-DOS floppy disks for later off-line database evaluation. The system can also communicate with mainframes or other PCs via either RS-232C or IEEE-488 interfaces. A complete Model 2210 system costs $65,000. The price of the optional variable aperture unit is $15,800 and the far-field scanner sells for $17,000. Delivery, six weeks ARO.

Photon Kinetics Inc, 9350 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 644-1960. TLX 4992356.

Circle No 664

Recorder features 30 channels for long-term data acquisition

Designed for long-term data acquisition and recording lasting weeks or months, the PM-8238 multipoint data recorder can record as many as 30 simultaneous inputs in 3 sec. The instrument displays the data from each of the individually programmable channels in either graphic or tabular numeric form.

The recorder's full-scale resolution of 1000 dots provides a μV measuring resolution over the full 10-in. plotting width, allowing precision measurement of all values. A zero-suppression feature, together with selectable chart-transport speeds, ensures proper scaling of input values and optimum use of the recording area.

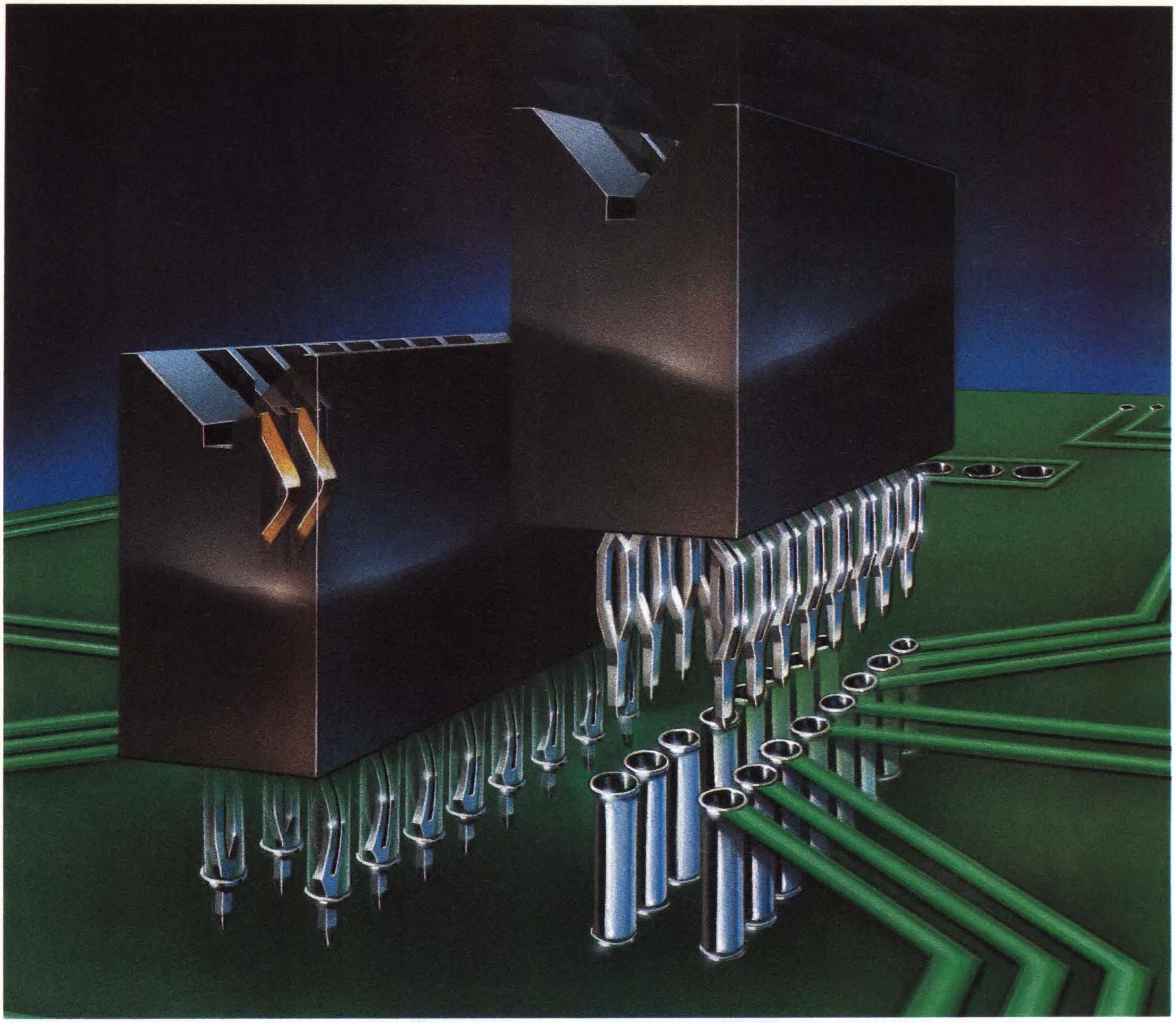
The programmable input channels let the operator choose any desired combination of 2-, 3- and 4-wire measurements of millivolts, volts, or temperature. The operator can choose range, span, and linearization settings to match the inputs from thermocouples or other transducers. Once entered, configuration, scaling, and chart speeds are stored in interchangeable, plug-in memory modules for quick recall.

The PM-8238 uses function keys (with LED indicators) and a numeric panel to select functions and preset values. Interactive programming simplifies the operation, and error signals provide operator guidance. You can also enter parameters remotely through a personal computer via RS-232C or IEEE-488 interfaces.

The instrument uses a low-maintenance thermal printing system that lets you avoid the use of ink reservoirs, ribbons, or pens. A special industrial version of the recorder, the KS-8238, features a full-sized front door to protect the instrument in harsh environments. The PM-8238 costs $5500, and the KS-8238 sells for $5950.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853. TWX 910-445-2943.

Circle No 660



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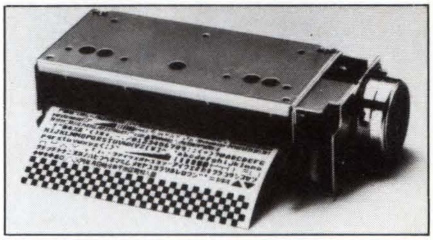
CIRCLE NO 55

Thermal printer mechanisms feature high speed and high resolution



The FTP-421MCL001 and FTP-441MCL001 are 40- and 80-column thermal printer mechanisms, respectively. Both offer print speeds of 250 dot-lines/in. at a resolution of 160 dots/in. for both graphics and character generation. These printers quickly generate the complex data associated with such applications as medical readouts, scientific analysis and measurement, and data communications.

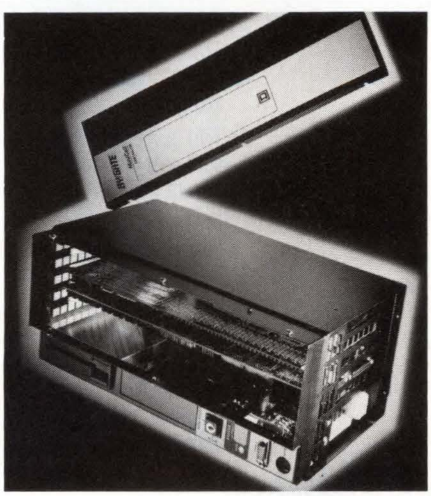
The FTP-421 and FTP-441 achieve their high-speed operation by means of integrated driver circuits in the thermal printhead. In addition to the high printing speed, both mechanisms feature front and rear paper-loading capabilities for printing on different types of media. Rear paper insertion minimizes bending of the media and accommodates thick paper, or labels, for barcoding or coupon-generating applications. This dual-purpose insertion feature also facilitates mounting of the printer mechanism in different devices. Depending on the application, the mechanism can eject paper from either the top or the back of the mechanism.

A step motor friction-feeds paper across the platen for contact with the thermal printhead. A minimum of moving parts ensures a printer service life of 30 million pulses. The FTP-421 costs $198, and the FTP-441 sells for $258.

Fujitsu Components Inc, 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 562-1000. TWX 910-338-0190.

Circle No 667

Cell-controller hardware platform is built for the factory floor



The Sy/Gate MiniCell controller is a compact hardware platform designed for industrial applications. Measuring 14×6.25×6.5 in. and weighing 12.5 lbs, the controller takes up one-fifth the space and weighs one-quarter of comparable products, according to the manufacturer.

The controller boots up on the MS-DOS operating system, *but runs above* the DOS system on its own multitasking operating system. This arrangement lets the user select from the many software packages that run on the MS-DOS system, yet has the advantage of a proprietary operating system designed specifically for the plant floor.

The Sy/Gate unit has an Intel 8088 processor at each of its four serial ports and features 1.5M bytes of RAM, compared to the 640k bytes inherent in MS-DOS. The MiniCell controller communicates with the Sy/Gate MicroCell controller, with ASCII-based devices, and with a variety of programmable controllers, including Allen-Bradley, GE, Gould, Reliance, Struthers-Dunn, and Westinghouse. Unlike similar products, the MiniCell controller operates without a fan at ambient temperatures from 0 to 60°C. A double-digit display presents fault indications, thus allowing you use the controller without a monitor.

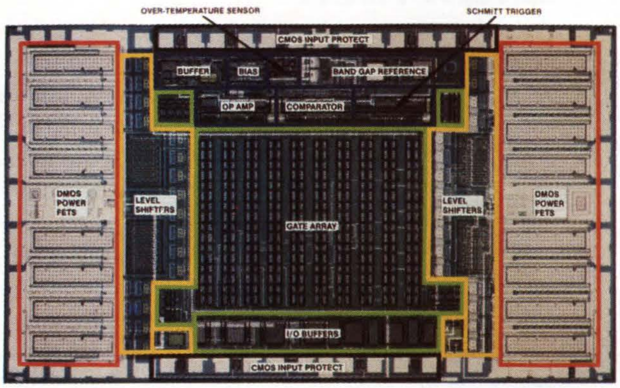
IBM PC/AT-compatible cards plug into the hardware platform. The memory allocation is 1M byte of RAM for application programs and 512k bytes of battery-backed RAM disk for executuve programs, such as DOS batch files. Programs are stored and retrieved using the 512k-byte RAM disk or, optionally, 3½-in. floppy-disk drives or a 20M-byte hard-disk drive.

Including hardware and software, the Sy/Gate MiniCell controller costs $14,995. The company offers a 2-day training seminar and a 4-day application workshop.

Square D, Automation Products Div, 4041 N Richards St, Milwaukee, WI 53212. Phone (414) 332-2000.

Circle No 662

SEMI-CUSTOM SMART 100V I C's IN 45 DAYS.



The MPD8020 uses Mixed CMOS/DMOS/Bipolar Technology to provide the user true monolithic smart power management.

Only 45 days after you give us the layout of your breadboard, built from our Kits #1 and #2, we'll give you perfectly tailored smart 100V ICs. What's more, you'll get them for a fraction of the cost of custom circuits.

Design Power ICs Faster.

Micrel's new MPD8020 CMOS/DMOS Semi-custom High Voltage Array combines CMOS analog circuits, TTL/CMOS compatible high speed CMOS logic, and high voltage DMOS power drive circuits on one monolithic IC.

A Great Library of Parts on Every Array.

16 fully floating 100V, 200 mA N-channel DMOS FETs. • 3 op amp/comparator/Schmitt trigger programmable macro cells and numerous array op amps. • 1 unity gain analog output buffer. • 1 band-gap reference. • 1 overtemperature sensor. • 16 high voltage CMOS level shifters • 200 CMOS gates in an uncommitted array. • 12 TTL/CMOS I/O buffers. • 16 medium current sink pre-drivers. • 4 internal high and low voltage power supplies. • Zeners, resistors, capacitors and more.

Two Development Kits.

For breadboarding your semi-custom MPD8020, Micrel offers two development kits to demonstrate the operation of key SSI and MSI circuits. Each is housed in a 40 pin DIP. Kit #1 ($20) provides 11 commonly used analog circuits. Kit #2 ($15) carries 8 digital circuits to check speed and digital timing characteristics.

After the customer has used the development kits to determine the interconnect pattern, Micrel turns each IC into a proprietary smart 100V ASIC for about one-sixth the cost of a custom IC. As your needs grow, we can quickly turn your semi-custom chip into a full custom chip for even greater savings.

The MPD8020 can be packaged in a 44 PIN JEDEC PLCC with an integral heat sink, 16 to 48 PIN DIPs, or single in-line power package. Packaged units available to MIL STD 883C. Dice are also available for hybrid manufacturers.

A single +5 Volt to +15 Volt supply powers the logic and analog circuitry. High voltage portions operate at +20 to +100 volts. The chip can also derive the +15 volt supply from a 24V, 48V, or 100V high voltage supply. An internal voltage pump can be used to drive the high side gates of the power N-channel DMOS FETs at 15 volts above the +100 volt supply for rail-to-rail high voltage switching.

Wide Range of Applications.

Use the MPD8020 in switching regulators, motor control, relay and solenoid drivers, smart switch with bus decode, smart lamp drivers, automotive switching, printer solenoid drivers, and high voltage display drivers.

Build Safety and Reliability Into Your Product.

You specify which safety features you want built-in such as overtemperature, overcurrent, short circuit, and overvoltage protection. The circuit can then take immediate action whenever any of these faults are detected and send a status signal back on your microprocessor data base. You can design safety in at the outset.

For more information, fill out the coupon below or contact Marvin Vander Kooi, Micrel, Inc., 1235 Midas Way, Sunnyvale, CA 94086.
Phone (408) 245-2500. FAX (408) 245-4175.

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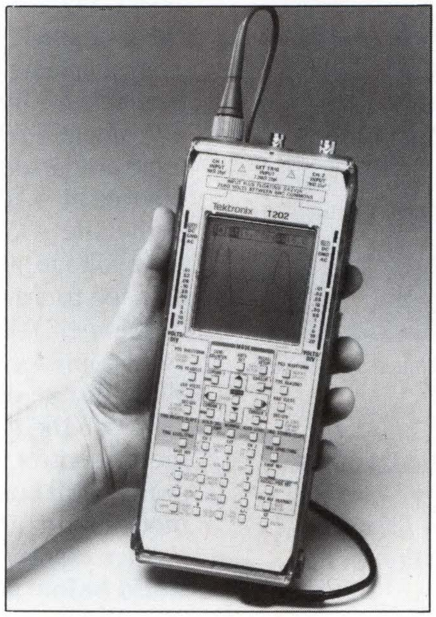
CIRCLE NO 111

Industrial Product Showcase

Handheld oscilloscopes feature digital storage and 5-MHz bandwidth

Weighing less than 7 lbs with carrying case, batteries, and accessories, the T200 and T201 oscilloscopes utilize flat-panel LCD technology and digital capabilities to achieve their 10×4.5×2-in. size.

The 2-channel scopes offer a dual timebase, a 5-MHz bandwidth for repetitive signals, a 2-MHz bandwidth for single-shot signals, and a 20M sample/sec sampling rate with 50-nsec resolution. Users may choose from two different interfaces. The T202 offers a standard scope interface with its front-panel controls divided into traditional functional sections. For users who prefer left-to-right logical manipulations, the T201 offers a calculator-like interface.



Other features include the ability to preset time and trigger functions via simple programming sequences, a nonvolatile memory that can store nine front-panel settings or nine separate waveforms for later recall, and signal-processing capability for differential and ratio measurements.

The T201 and T202 cost $1995 each and include a battery pack, two probes, a carrying case, a manual, and an audio cassette training kit.

Tektronix, Portable Test Instruments Div, Box 1700, Beaverton, OR 97077. Phone (800) 426-2200.

Circle No 670

Industrial computer system provides graphics-based interface

Based on the Macintosh II computer, the AI-90 system combines processing power with an easy-to-use graphics interface. Instead of learning complex programming commands, the factory worker has the choice of using an icon-based mouse-driven, trackball, or touch-screen interface. This type of interface minimizes the time and expense of training, and simplifies day-to-day operation.

You can use the AI-90 system for a variety of factory applications: as a cell controller; as an intelligent shop-floor terminal; as a test-stand controller; as an industrial PC; as a data analyzer; and as a lab instrument controller. The AI-90 runs all Macintosh II software and has optional support for MS-DOS and Unix programs. In addition, the system supports a variety of standard application programs including statistical process control (SPC), motion control, and artificial intelligence languages.

The computer features a 68020 32-bit μP operating at 16 MHz and a 68881 math coprocessor. The system, which provides 1M byte of RAM as standard memory, is onboard expandable to 8M bytes. Additional memory expansion via the NuBus slots provides a maximum 2G bytes of address space. An optional 68851 memory management unit is available.

Standard peripherals include a 3½-in., 800k-byte floppy-disk drive, a color monitor with a 16-million color palette or a monochrome monitor with 256 gray shades, having a resolution of 640×480 pixels. The basic AI-90 measures 21×17.5×8.5 in. and weighs 45 lbs without options. $8500.

Automatix Inc, 1000 Tech Park Dr, Billerica, MA 01821. Phone (508) 667-7900. TLX 951518.

Circle No 665

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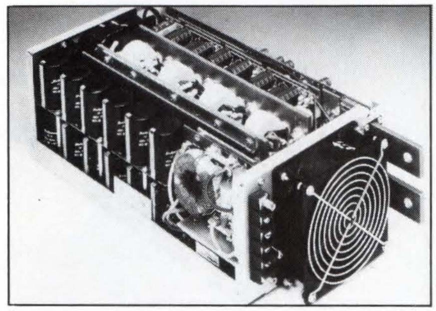
CIRCLE NO 112

Innovative design provides 3 kW of power in a 5 × 8 × 15-in. package



By using a combination of hybrid and monolithic ICs, low-loss miniature capacitors, and 100-kHz power MOSFETs, the 9R-Series switching power supplies deliver 3 kW of power in a 5×8×15-in. package. According to the manufacturer, the 9R SuperSwitcher is the industry's first 3-kW supply with a 5×8×X-in. frame—the previous industry standard being 1.5 kW in a 5×8×11-in.-frame size.

The 9R5-600-381 model provides a 5V, 600A dc output at 50°C. Other models in the series provide outputs of 2, 12, 15, 24, 36, and 48V. The ac input is 165 to 265V (220V typ); either 36A max single-phase, or 21A max 3-phase at 47 to 63 Hz. The series can also function as a dc/dc converter with a 200 to 375V dc input at 19A max. The input power to the supply is via 8-32 screw terminals.

Standard features include an active soft-start, an N+1 current-sharing capability, remote sensing, automatic thermal shutdown, and a ball-bearing dc fan. I/O capabilities include high or low logic inhibit, input power fail, output good, remote adjust, current share, and margin low/high. The supplies meet UL, CSA, IEC, and VDE specifications; approvals are pending.

The 9R-Series current-mode supplies use four time-staggered power inverters that reduce ripple current, minimizing the stress on input and output capacitors. The four separate inverters also enhance overall reliability—if one inverter should fail, the remaining inverters will provide about 80% of the maximum output current. The 9R5-600-381 supply costs $1890 (under 25).

Powertec, 20550 Nordhoff St, Chatsworth, CA. Phone (818) 882-0004. TLX 277483.

Circle No 668

Test system handles circuit boards containing mixed analog/digital functions

The Model 8000 combinational board test system features several capabilities not available in other systems, according to the manufacturer. The 8000's open architecture reduces overall testing costs by allowing users to design and place their own hot-bed test circuitry directly onto 8000 system boards and control it from the board test program—in synchronization with analog or digital test subsystems.

The system contains 2048 nonmultiplexed test points that provide the full range of in-circuit and functional testing. A custom driver/receiver interface provides the shortest possible distance from the board under test to the test-head electronics, resulting in fast, clean signals. The 8000's integral fixture ground plane provides controlled path impedance, and its unipolar fixture design eliminates the capacitance changes caused by wire movements that are inherent in hinged-fixture designs.

For digital tests, the 8000 offers a programmable slew rate from 50 to 300V/μsec, useful in testing CMOS, AS, TTL, ECL and Fast devices. An integrated 32-channel logic analyzer captures the actual digital responses, either during test verification or production test. Also, an integrated graphics waveform editor reduces the time required to create and debug digital test programs.

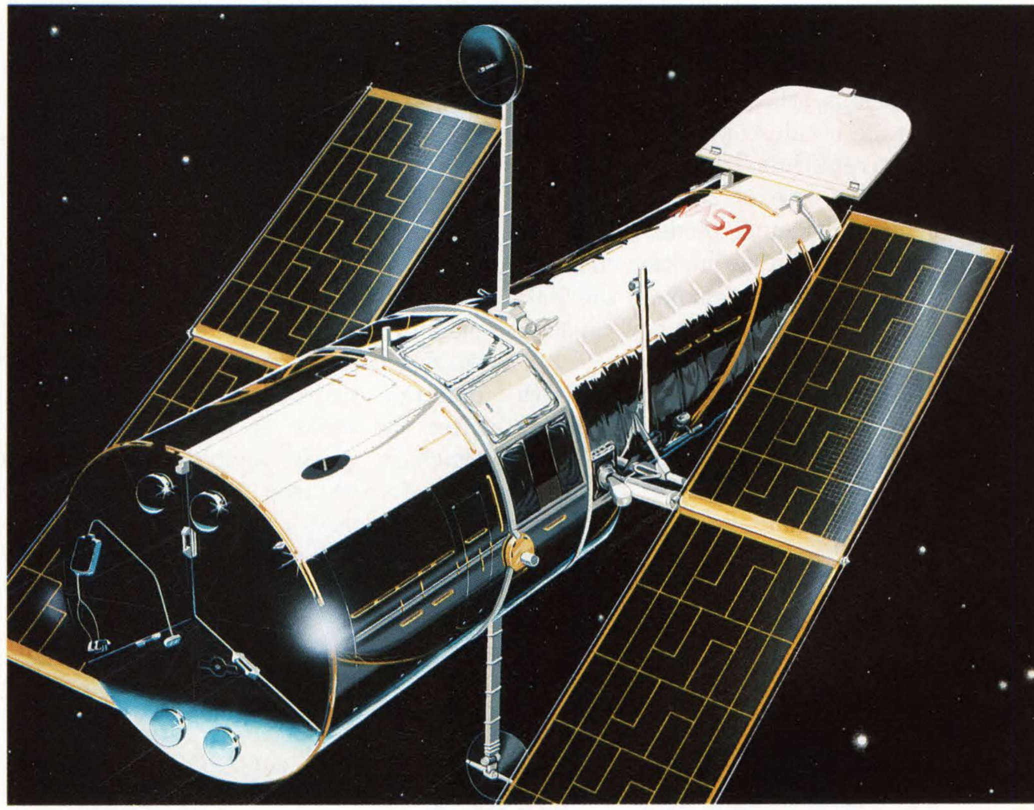
The 8000's modular analog system is fully synchronized to the digital subsystem for mixed signal testing. The system achieves maximum test coverage and flexibility by providing simultaneous analog/digital stimulus and measurement, 6-wire in-circuit measurement, 100V stimulus, and a programmable short-circuit threshold.

The 8000 ranges in price from $275,000 to $550,000, depending on node count and options.

Zehntel Inc, 2625 Shadelands Dr, Walnut Creek, CA 94598. Phone (415) 932-6900. TWX 910-385-6300.

Circle No 666

Before they travel at 17,500 MPH, they travel in Hardigg containers.



Some of the most sensitive components in satellites and telescopes are shipped and stored in reusable containers we custom-design. So before they travel the vacuum of space, they travel the earth in Hardigg.

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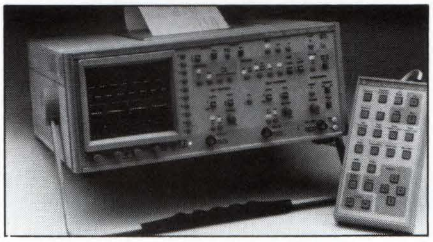
CIRCLE NO 113

Digital storage scope makes low-frequency measurements to 20 MHz

Targeted for transducer measurements and other low-frequency applications, the DSO-1602 digital-storage oscilloscope combines a 20-MHz real-time bandwidth with a sampling rate of 20M samples/sec in single-channel mode. With 10k words of 8-bit acquisition memory available on each channel, the 1602 has both a large memory capacity and a 0.01% resolution.

The oscilloscope features both pre- and post-trigger viewing, a trigger window, and high-frequency trigger rejection. A trigger-count function lets the scope count as many as 16,383 events before triggering to extract the pulse of interest from a long burst. You can



use the pre-and post-triggering capability to acquire all the data occurring before an event, or to show data that occurs as long as 1000 sec after the event. A wide range of timebase speeds enables the capture of events from 50-nsec to 2000-sec duration.

The scope incorporates automatic cursor-based measurement facilities, with on-screen alpha numerics providing a direct readout of the measured values. The addition of a waveform-processor keypad transforms the scope into an analysis tool that can measure rms voltage, rise and fall times, pulse width, frequency, p-p voltage, and the area under the trace.

The 1602 is fully programmable and features IEEE-488 and dual RS-232C interfaces. The 1602 measures 17×14.5×6 in. and weighs 18 lbs. The price of the 1602 is $3990. Delivery, 60 days ARO.

Gould Inc, Test and Measurement Group, 3631 Perkins Ave, Cleveland, OH 44114. Phone (800) 538-9320.

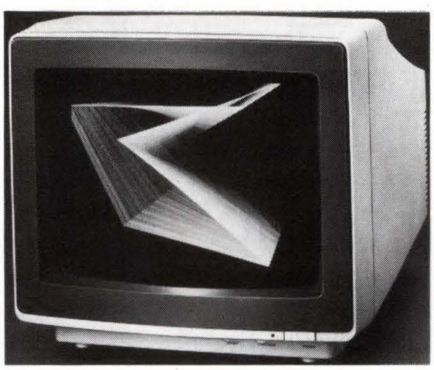
Circle No 674

19-in. color monitors target CAD/CAM applications

Designed to reproduce the large images required by CAD/CAM and other business graphics applications, the ECM 1910, 1911, and 1912 are 19-in. color monitors with variable scan capabilities. The series also provides options of either short- or long-persistence phosphors, and of clear or tinted glass.

The ECM 1910 monitor has a short-persistence phosphor with a tinted antiglare CRT that provides a bright, high-contrast display for use in high ambient-light conditions. The ECM 1911 also has a high-contrast display, but is flicker-free due to its long-persistence phosphor. The ECM 1912 has a clear CRT with a long-persistence phosphor for use in bright environments.

All of the monitors feature automatic adjustment for horizontal and vertical frequency. The horizontal



adjustment lets the monitor interface to a PC using a variety of add-on color cards and software. The monitor automatically adjusts to any color card with a horizontal frequency between 15 and 34 kHz. Color cards in this frequency range include the IBM CGA, EGA, VGA, and PGA. The vertical frequency automatically adjusts between 50 and 85 Hz, a feature that automatically centers the screen's display when the user switches to a different color card.

The ECM monitors have a resolution of 1024×800 (interlaced) and 1024×512 (noninterlaced). A 1900 series monitor becomes a standalone CAD/CAM system when connected to a PC running popular software packages such as AutoCAD and VersaCAD. The RGB monitor accepts both RGB/RS-170 and IBM TTLI inputs via connectors on the rear panel; it accepts switch-selectable TTL/analog inputs via a 9-pin DIN connector. The ECM 1901 retails for $2795; the ECM 1911 and 1912 both sell for $2895.

Electrohome Ltd, 809 Wellington St N, Kitchener, Ontario, Canada N2G 4J6. Phone (519) 744-7111.

Circle No 669

In a Navy test, a Tomahawk cruise missile exploded into a concrete building. When the dust settled, little remained but gravel and fragments of casing.

And the Abbott model C28D0.8 you see here.

Its aluminum baseplate and an adjustment cap were ripped off in the blast. But reconnected on a workbench, the unit still provided a steady .8 amp of DC current — just as it was designed to.

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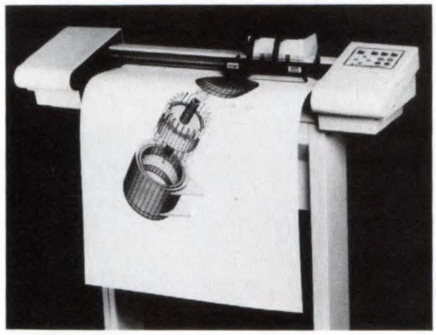
CIRCLE NO 114

Industrial Product Showcase

High-performance drafting plotters feature axial pen speeds to 32 ips

The DMP-60 series single-pen plotters offer adjustable media-size capabilities and handle a variety of English and metric media formats. The plotters also accept numerous add-on performance options such as a multipen accessory, an optical scanner, and an expanded buffer board.

The DMP-61 has an axial pen speed to 32 ips and an axial acceleration as high as 4g. It can produce drawings on 16 media sizes from 8.5×11 in. (A size) to 24×36 in. (D size). The large-format DMP-62 handles 23 media sizes from 8.5×11 in. to 36×48 in. (E size). The DMP-62 has an axial pen speed of 24 ips and an axial acceleration to 2g.



Each model features a mechanical resolution of 0.0005 in. and a same-pen repeatability of ±0.002 in.

Both plotters provide onboard 68000 μP-based intelligence that features capabilities such as multiple fonts, filled fonts, closed-area fill with 15 fill patterns, 10 character sets, and a curve-generating algorithm that ensures high line quality and smooth curves. The plotters can draw on paper, vellum, and polyester film using fiber-tip pens, disposable technical pens, refillable liquid-ink pens, and roller-ball pens.

The DMP-61 costs $4695, and the price of the DMP-62 is $6495. The MP-60 multipen changer costs $750, and a 1M-byte buffer-board option sells for $995.

Houston Instrument, 8500 Cameron Rd, Austin, TX 78753. Phone (800) 444-3425; in TX, (512) 835-0900.

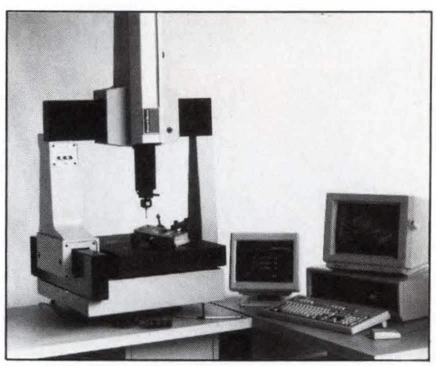
Circle No 671

PC-based measurement system generates reverse-engineered blueprints

The CADDInspector solves the problem of obtaining an accurate blueprint of an object when you don't have the original design, using a process called reverse engineering. The CADDInspector also lets you compare a manufactured part with its CAD-compatible design, following the normal inspection process.

The CADDInspector is the integral link between CADDKey-3, a leading 3-D PC-CADD software package and MicroVal, a highly successful coordinate measuring machine (CMM). The CADDInspector allows direct digitization of both 2-D and 3-D points, lines, arcs, circles, and splines. When digitizing 2-D entities, the user can also set the depth of the digitized entity.

The CADDInspector also performs probe-offset calculations, which allows true part-geometry



creation. For simplicity, 2-D geometry goes on level 2 and is assigned the color red; 3-D geometry goes on level 3 and is assigned the color olive-green; and offset geometry (corrected for probe offsets) goes on level 1 and is assigned the color green. The CADDInspector program is written largely in CADL (CADKey advanced design language) and macros, allowing for rapid customization.

Key specifications of the CADDInspector are a linear accuracy of 0.006 mm, repeatability of 0.004 mm, and resolution of 0.002 mm. The measuring ranges are X, 356 mm; Y, 406 mm; and Z, 305 mm. The work capacity is X, 457 mm; Y, 610 mm; and Z, 381 mm. The price for a CADDInspector workstation, including CADKey-3, CADDInspector, and MicroVal CMM, is $19,245.

CADKey Inc, 27 Hartford Tpk, Vernon, CT 06066. Phone (203) 647-0220. TWX 510-600-7223.

Circle No 672

Browne & Sharpe Manufacturing Co, Precision Park, North Kingstown, RI 02852. Phone (800) 551-6245; in MA, (800) 262-5226. TLX 6814067.

Circle No 673

The discreet alternative to discrete protection.

Introducing Siemens BTS 412A...the world's first fully-protected Smart SIPMOS® device.

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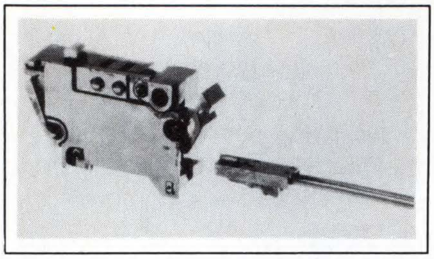
CIRCLE NO 116



SNAP-ACTION SWITCH

The DN Terminator snap-action switch offers potential savings as high as $0.50/switch in installed cost. Its external design permits three methods of installation: traditional screw mount, horizontal snap-in mount, and vertical snap-in mount. The switch also features a plug-in connection that mates with standard 0.025-in. square pin connectors on 0.1-in. centers.

The precision switch has the same internal design as the company's D4 Series: a long-life stainless-steel spring mechanism, arc-resistant internal barriers, and a flame-retardent UL-94V0 case and cover. Currently available in an spst normally open version, the switch has electrical ratings of 0.1A at 125V ac with gold crosspoint contacts, and 3A at 125V ac with silver contacts. At its rated load, the switch has a life cycle of 1 million operations with gold contacts and 500,000 operations with silver contacts. The switch meets UL and CSA standards. $0.95 (OEM qty).

Cherry Electrical Products, 3600 Sunset Ave, Waukegan, IL 60087. Phone (312) 360-3500.

Circle No 610

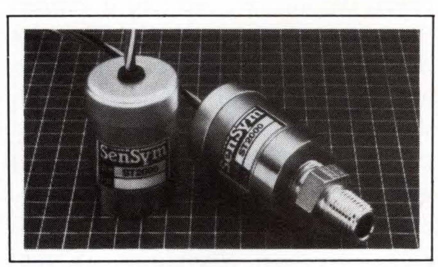
HALL-EFFECT SENSORS

The UGN-5275, UGN-5276, and UGN-5277 are latching Hall-effect sensor/driver ICs for electronic commutation of brushless dc motors. The devices sense the alternating polarity magnetic-flux levels generated by rotating multipole ring magnets in brushless dc motors. They can also drive inductive loads such as relays and solenoids. Packaged in a low-profile SIP with dimensions of 0.2×0.13×0.06 in., the ICs can sink as much as 300 mA from complementary, open-collector outputs.

Included in the monolithic chip are a Hall-effect sensor, a voltage regulator, a closed-loop op amp, a Schmitt trigger, a driver stage, and a complementary power-output stage. The voltage regulator allows operation from supply voltages of 4.5 to 14V. The dual outputs switch from complementary on/off to complementary off/on in accordance with the polarity of the sensed magnetic field. The three devices vary only in their switching points. The UGN-5275 switches at or below 250G (gauss), the UGN-5276 switches at 350G, and the UGN-5277 switches at 150G. The devices are specified for operation over the −20 to +85°C temperature range. UGN-5275, $0.87; UGN-5276, $0.82; UGN-5277, $1.42 (1000).

Sprague Electric Co, Semiconductor Group, 70 Pembroke Rd, Concord, NH 03301. Phone (603) 224-1961.

Circle No 611



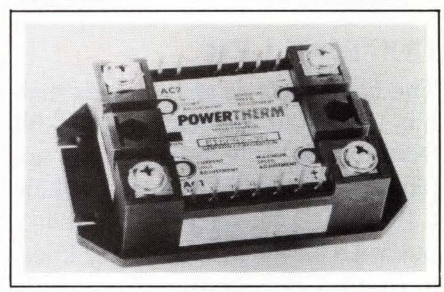
TRANSDUCERS

Designed for measuring hostile media in harsh environments, the ST2000 Series transducers are housed in a stainless-steel case. The series includes four models that measure pressure from 0 to 15 psig through 0 to 300 psig. Each model features a temperature-compensated 2-wire output from 4 to 20 mA. Accuracy is within ±0.5% and all ST2000 Series devices have internal voltage regulation that permits operation over a dc supply-voltage range of 12 to 40V.

The series uses a combination diaphragm/oil-fill isolation technique that minimizes the amount of oil for optimal performance over the specified temperature range of −40 to +125°C. Other specifications include a zero-pressure offset of 4 mA (±100 μA), a full-scale span of 16 mA (±200 μA), a full-scale output of 20 mA typ, and nonlinearity and hysteresis of ±0.5% of full scale. $95 (under 25).

SenSym, 1255 Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-1500. TLX 176376.

Circle No 612



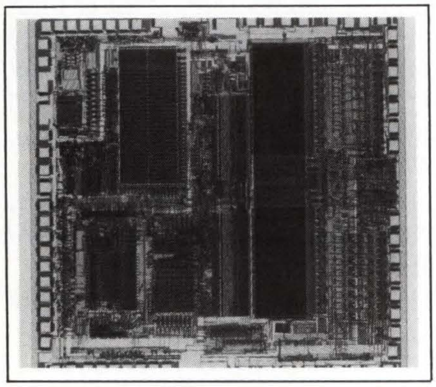
MOTOR SPEED CONTROL

Containing nearly all the components needed for a complete dc motor control system, the EISC72/92 Series power modules can handle motors with ratings from 0.125 to 5 hp. The output current ratings of the modules range from 25 to 50A avg at a 180° conduction angle. The maximum single-cycle surge-current ratings are 300 to 1000A.

Each module, which contains about 300 equivalent discrete devices, needs only an external potentiometer, an on/off switch, and fuses to provide a complete speed control system for dc motors. The EISC modules incorporate a full-wave dc power source for the motor's field, and have a full-wave dc, SCR-controllable power source for the motor's armature. Four trimming potentiometers in the module permit adjustments for IR compensation, current limit, minimum speed, and maximum speed. A red LED indicates when power is available at the module's firing circuit. $150 to $250, depending on the module.

Gentron Corp, 6667 N Sidney Place, Milwaukee, WI 53209. Phone (414) 351-1660. TLX 26881.

Circle No 613



CONTROLLER

The Model 8098 is an 8-bit external-bus version of the company's 16-bit 8096 for real-time 8-bit control applications. On-chip features include a 10-bit A/D converter, a PWM output with a S/H circuit, 32 I/O lines, a 16-bit CPU, a 16×16 multiply unit, a 32/16 divide unit, 8k bytes of program memory, and 232 bytes of general-purpose registers. The multiply and divide functions have speeds of 6.25 µsec.

Additional features of the 8098 include a 16-bit watchdog timer, four 16-bit software timers, and two 16-bit counter/timers. Having the same 16-bit CPU and onboard peripherals as its 8096 counterpart, the 8098 provides a low-cost alternative for achieving 16-bit performance in existing real-time event and motor-control systems, according to the company. $4.75 (large orders).

Intel Corp, Literature Dept W-407, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (800) 548-4725.

Circle No 614

MASS FLOW METER

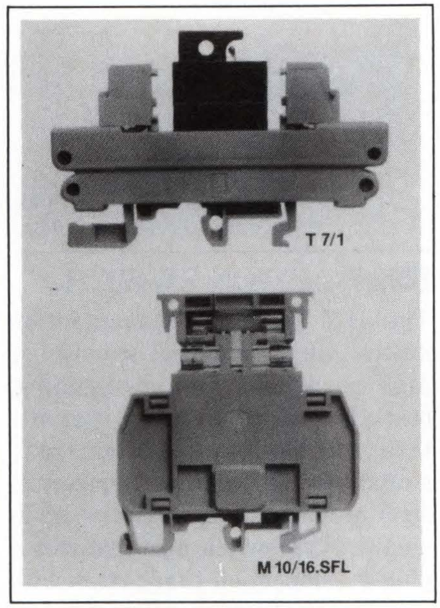
Designed for fast-response gas flow measurements, the 1100 MFM (mass flow meter) features a micromachined silicon flow-rate sensor. The sensor responds to flow-rate changes as low as 0.02 standard cm^3/minute of nitrogen in <500 µsec.

Sensor output data is fed to the MFM's µP-controlled signal-processing electronics, which produces a linear 0 to 5V dc output signal in <5 msec. According to the company, both the long- and short-term stability of the 1100 MFM exceed the characteristics of all conventional mass flow meters by several orders of magnitude. Its repeatability is ±0.2%, and accuracy is ±1.0% of full scale.

The sensor is passivated with silcon oxynitride, making it impervious to chemical attack. The gas flow chamber and all external seals are made of 316L stainless steel, which eliminates interactions between the MFM and the measured gas. Other features of the 1100 include an auto-zero function, an RS-232C interface, selectable alarms, EMI/RFI shielding, and onboard diagnostics. $1100. Delivery, stock to 60 days.

Innovus, 1756 Junction Ave, San Jose, CA 95112. Phone (408) 436-7790. FAX 408-436-8185.

Circle No 615



FUSE BLOCKS

Additions to the company's line of DIN rail-mounted fuse terminal blocks include the 10A and 16A Models. Type M-10/16.SF is a UL-recognized 600V unit that holds standard 0.25×1.25-in. fuses rated from 0.25 to 16A. When ordered with an optional neon or LED blown-fuse indicator, the designation is M-10/16.SFL. Type T-7/1, a 1-point terminal block, is rated at 0.18 to 10A and features an auxiliary contact. Type T-7/8 contains eight fuses and eight separate auxiliary circuits; you can use it for fusing 8-point programmable logic-controller I/O units.

The M-10/16.SF(L) is rated for 18 to 8 AWG wire size and needs only 16-mm spacing on the DIN rail. The T-7/1 and T7/8 require 13- and 89-mm spacing, respectively. M-10/16SF, $8.30; M-10/16SFL, $8.50; T-7/1, $14.25; T-7/8, $98.50.

Entrelec, 2 Ram Ridge Rd, Spring Valley, NY 10977. Phone (800) 431-2308. TLX 996619.

Circle No 616

THICKNESS TESTER

Combining beta-backscatter and magnetic-induction principles in a single unit, the Beta-Min 1800 is a computerized plating/coating thickness measurement system. The

tester measures the thickness of nickel (even through final layers of gold and rhodium), tin-lead, gold, and copper.

The Beta-Min 1800 provides a precise evaluation of all critical coatings, including nickel-plated tabs, and ensures correct plating thicknesses during the manufacture and inspection of pc boards. The µP-based device features a 24-character alphanumeric display. Thickness results are displayed in microinches, mils, micrometers, percent composition, or counts per minute. The unit simultaneously accepts two beta probes and a nickel probe, with software-controlled probe selection.

Other features include nonvolatile memory, 20 data-retention locations, plating-bath density correction, base-material correction, an RS-232C port, and a parallel-printer interface. The unit weighs 12 lbs and measures 15×6×13 in. The power input is 15W at 115/230V, 60 Hz. $5000.

CMI International, 2301 Arthur Ave, Elk Grove Village, IL 60007. Phone (312) 439-4404. TLX 282052.

Circle No 617

12V SEALED BATTERY

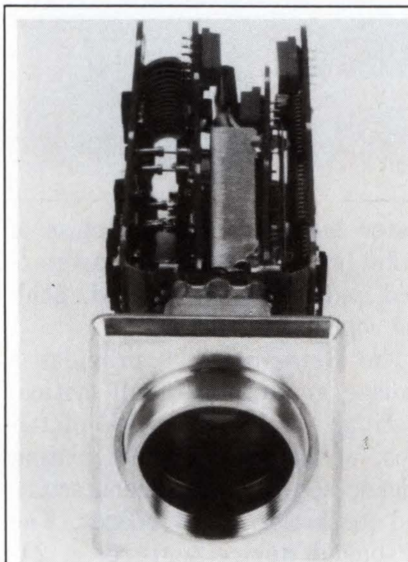
The PS-1242 rechargeable 12V sealed lead-acid battery has a capacity of 4 ampere-hours. The 3.54×2.75×4.01-in. unit packs 1.23 watt-hours of energy/in^3. The battery is designed for such applications as portable power, security equipment, emergency lighting, and electronic memory protection. The maintenance-free battery is usable in any position and suitable for both standby and deep-cycle applications. The PS-1242 can deliver 40A of high-rate discharge current. The battery weighs 3.74 lbs, has a life expectancy of more than 5 years, and can be recharged 200 to 500 times, depending on the average depth of discharge. $16 (500).

PowerSonic Corp, Box 5242,

CIRCLE NO 11

Redwood City, CA 94063. Phone (415) 364-5001. TLX 348400.

Circle No 619



IMAGING MODULE

Based on the company's solid-state image sensor (SSIS), the 56470 Series modular subassembly requires only a chassis and lens to form a complete black-and-white video camera for use in machine vision and surveillance. The module consists of the SSIS and all necessary drive, video-processing, and power-supply circuits. Two basic versions are available: a 525-line version that meets EIA standards, and a 625-line version that meets CCIR standards. Each version is available in three different sensor-quality grades.

The SSIS used in the module has an image area of 6×4.5 mm and works at ambient light levels as low as 0.5 lux. The unit has a bandwidth of 5.8 MHz and an S/N ratio of 46 dB. An integral master clock derives the field-, frame- and line-synchronization pulses, or you can synchronize the unit with an external reference from a computer or another camera. The composite-video output signal is 1V p-p. An iris-control output is available to drive lenses with an automatic iris. The unit's C-mount mechanical interface accepts standard 0.5-in. (or larger) lenses. DM 600 to DM 1300, depending on quantity, grade, and importing country.

Philips International BV, Box 218, 5600 MD, Eindhoven, The Netherlands. Phone +31 40 724173.

Circle No 618

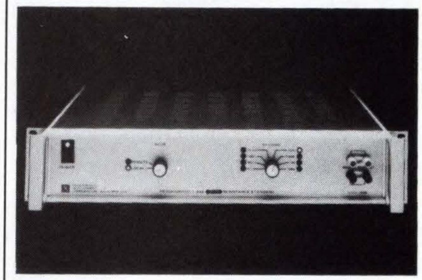
LIMIT CONTROLLER

The Model 2040 limit controller provides a limit shut-off control for temperature-sensitive equipment or process control systems. For overtemperature shut-down and other applications requiring limit control action, the unit can act independently of any other controls. The controller's input works over a current range of 4 to 20 mA and handles a variety of thermocouples including J, K, R, S, T, E, B, and Platinum RTD types. The output of the 2040 controls a 5A, 240V ac noninductive Limit relay that has both NC (normally closed) and NO (normally open) contacts.

A bright-blue, high-visibility vacuum-fluorescent display prompts the user with fixed sequences of displays to ensure the controller's calibration and operation. An independent analog-backup circuit monitors the measurement and provides redundancy to trip the Limit relay should the temperature exceed the primary setpoint. Other features include a self-diagnostics capability, a digital watchdog, and keypad security. Standard unit, $225; FM-approved unit, $235.

LFE Corp, Instruments Div, 55 Green St, Clinton, MA 01510. Phone (508) 835-1074. TWX 710-347-1734.

Circle No 620



CALIBRATOR

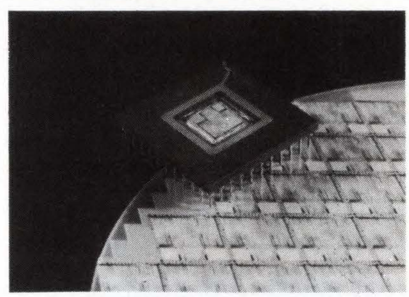
The Model 620A resistance calibrator features eight cardinal resistance points and is IEEE-488 programmable. Without the need to switch leads, the 620A simplifies resistance measurements in laboratory, engineering, and production-

Industrial Product Showcase

line applications. Designed for use with both smart and dumb DVMs and DMMs, the calibrator provides resistance values of 1, 10, 100, 1k, 10k, 100k, 1M, and 10 MΩ. The worst-case accuracy is 0.002 to 0.0125%, depending on the resistance value. The 620A accommodates 2- or 4-wire connections and has a parallel computer interface. $1530.

Electronic Development Corp, 11 Hamlin St, Boston, MA 02127. Phone (617) 268-9696. TLX 951596.

Circle No 621



MICROCONTROLLER

The RTX-2000 10-MIPS, high-performance 16-bit microcontroller has on-chip timers, an interrupt controller, and a multiplier. The chip features an ASIC Bus, which provides off-chip architecture extension, using hardware acceleration logic and application-specific I/O devices. Using a stack-oriented, multiple-bus architecture, the RTX-2000 lets you implement such real-time applications as DSP, image processing, robotics, graphics, and simulation.

The RTX-2000 provides direct execution of Forth, eliminating the need for assembly-language programming. Other features include a single-cycle 16-bit multiply unit, a single-cycle subroutine call/return unit, 3-cycle interrupt latency, and two on-chip 256-word stacks. The controller also has 1M byte of address space, and word/byte memory access. Fabricated in low-power CMOS, the RTX-2000 runs at 5 mA/MHz typ. In an 84-pin PGA package, $190 (1000); evaluation board, $1500.

Harris Corp, Semiconductor Sector, Box 883, Melbourne, FL 32901. Phone (305) 724-7800.

Circle No 622

MOTION CONTROL ICs

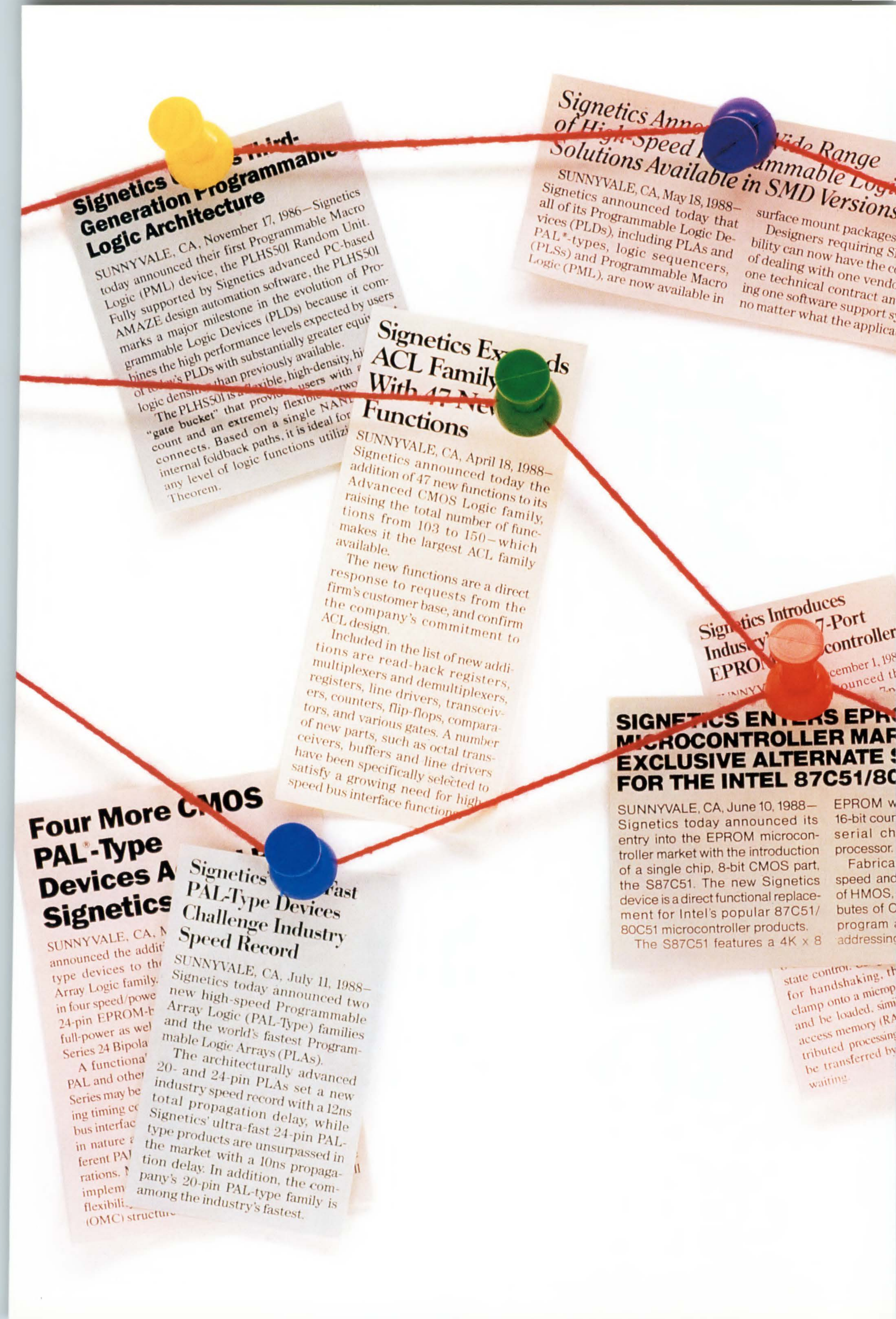
Intended for use with a variety of dc and brushless-dc servo motors, the LM628 motion-controller IC uses incremental shaft-encoder feedback to control the position, velocity, and acceleration and deceleration rates of servo mechanisms. The IC takes pulses from an incremental encoder and commands from an 8-bit parallel bus connected to a host μP. Based on the commands and programmable filter parameters, the LM628 writes to a DAC to control the power to a motor.

The LM628's output port can drive either an 8- or a 12-bit DAC. A second device, the LM629, outputs a PWM pulse stream that can drive an H-switch for dc motors or a commutator like the LM621 to control a brushless dc motor. The LM628 and LM629 differ only in the way they interface to the system's power stage. Other features include 32-bit internal computation abilities, a 750-kHz encoder capture rate, a sampling frequency of 3 kHz, and a clock frequency of 6 MHz. Both devices come in 28-pin DIPs and cost $30 (100).

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-4494. TLX 346353.

Circle No 626

Now, what about the other 95% of your design?



Generation Programmable
Logic Architecture
SUNNYVALE, CA, November 17, 1986—Signetics
today announced their first Programmable Macro
Logic (PML) device, the PLHS501 Random Unit.
Fully supported by Signetics advanced PC-based
AMAZE design automation software, the PLHS501
marks a major milestone in the evolution of Pro-
grammable Logic Devices (PLDs) because it com-
bines the high performance levels expected by users
The PLHS501 is
"gate bucket" that provi
count and an extremely flexib
connects. Based on a single NAN
internal foldback paths, it is ideal for
any level of logic functions utiliz
Theorem.
Solutions Available in SMD Versions
SUNNYVALE, CA, May 18, 1988—
Signetics announced today that
all of its Programmable Logic De-
vices (PLDs), including PLAs and
PAL®-types, logic sequencers,
(PLSs) and Programmable Macro
Logic (PML), are now available in
surface mount packages.
Designers requiring
bility can now have the
of dealing with one vend
one technical contract an
ing one software support
no matter what the applica
Signetics Ex ds
ACL Famil
Functions
SUNNYVALE, CA, April 18, 1988—
Signetics announced today the
addition of 47 new functions to its
Advanced CMOS Logic family,
raising the total number of func-
tions from 103 to 150—which
makes it the largest ACL family
available.
The new functions are a direct
response to requests from the
firm's customer base, and confirm
the company's commitment to
ACL design.
Included in the list of new addi-
tions are read-back registers,
multiplexers and demultiplexers,
registers, line drivers, transceiv-
ers, counters, flip-flops, compara-
tors, and various gates. A number
of new parts, such as octal trans-
ceivers, buffers and line drivers
have been specifically selected to
satisfy a growing need for high
speed bus interface function
tics Introduces
-Port
controller
EPRO
SIGNE CS EN S EP
CROCONTROLLER MA
EXCLUSIVE ALTERNATE
FOR THE INTEL 87C51/8
SUNNYVALE, CA, June 10, 1988—
Signetics today announced its
entry into the EPROM microcon-
troller market with the introduction
of a single chip, 8-bit CMOS part,
the S87C51. The new Signetics
device is a direct functional replace-
ment for Intel's popular 87C51/
80C51 microcontroller products.
The S87C51 features a 4K x 8
EPROM w
16-bit cour
serial ch
processor.
Fabrica
speed and
of HMOS,
butes of C
program
addressin
Four More CMOS
PAL®-Type
Devices A
Signetics
SUNNYVALE, CA,
announced the addi
type devices to th
Array Logic family.
in four speed/powe
24-pin EPROM-
full-power as wel
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PAL and other
Series may be
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Signetics
PAL-Type Devices
Challenge Industry
Speed Record
SUNNYVALE, CA, July 11, 1988—
Signetics today announced two
new high-speed Programmable
Array Logic (PAL-Type) families
and the world's fastest Program-
mable Logic Arrays (PLAs).
The architecturally advanced
20- and 24-pin PLAs set a new
industry speed record with a 12ns
total propagation delay, while
Signetics' ultra-fast 24-pin PAL-
type products are unsurpassed in
the market with a 10ns propaga-
tion delay. In addition, the com-
pany's 20-pin PAL-type family is
among the industry's fastest.

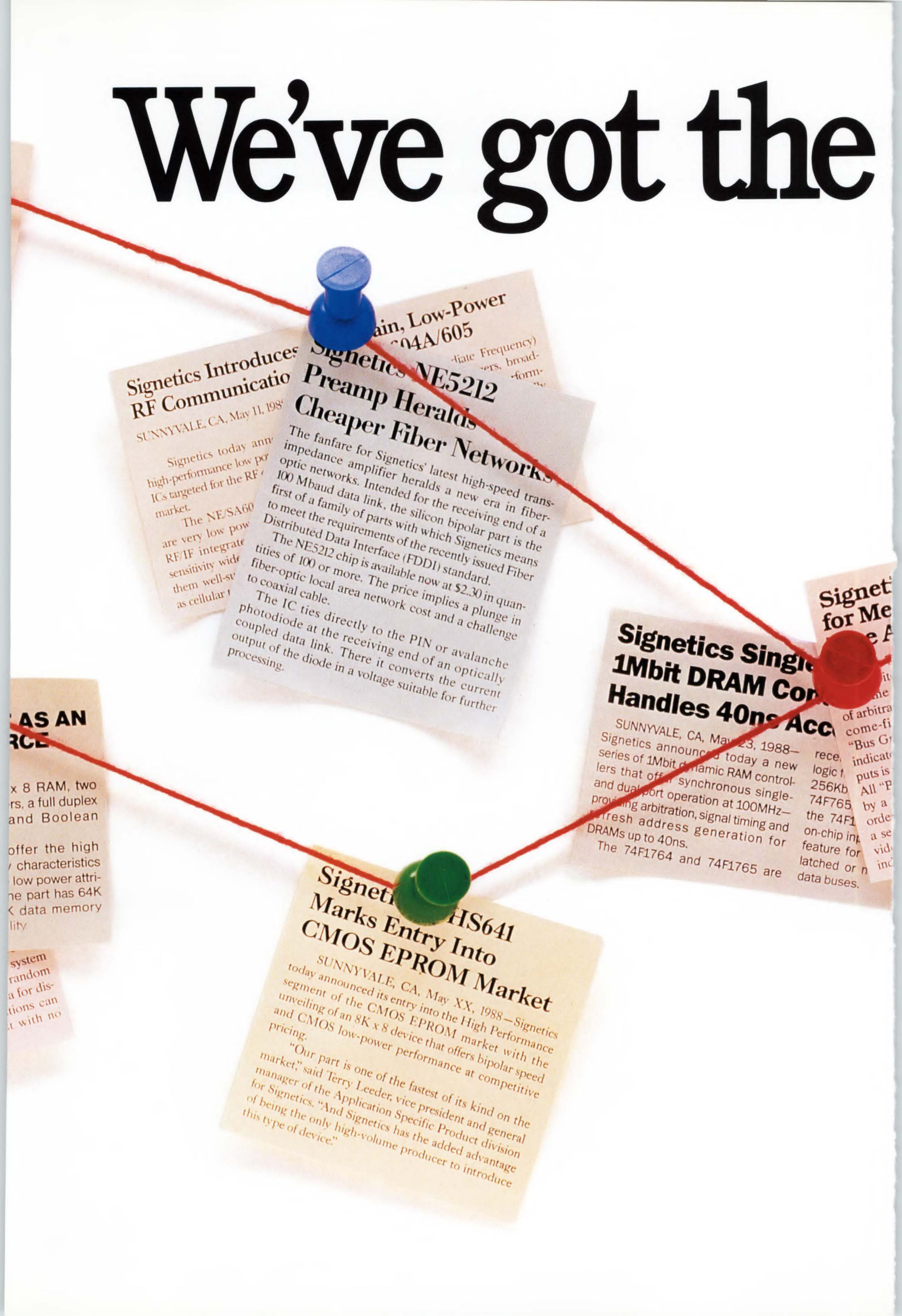
It takes more than a microprocessor to improve product performance.

That's where Signetics comes in.

Your dependable, worldwide supplier of quality ICs.

Processed with leading-edge technology and supported with customer-oriented service.

Everything essential to the total performance of your design.



We've got the
Signetics Introduces
RF Communicatio
SUNNYVALE, CA, May 11, 198
Signetics today ann
high-performance low po
ICs targeted for the RF
market.
The NE/SA60
are very low pow
RF/IF integrate
sensitivity wide
them well-su
as cellular
ain, Low-Power
604A/605
Signetics NE5212
Preamp Heralds
Cheaper Fiber Networks
The fanfare for Signetics' latest high-speed transimpedance amplifier heralds a new era in fiber-optic networks. Intended for the receiving end of a 100 Mbaud data link, the silicon bipolar part is the first of a family of parts with which Signetics means to meet the requirements of the recently issued Fiber Distributed Data Interface (FDDI) standard.
The NE5212 chip is available now at $2.30 in quantities of 100 or more. The price implies a plunge in fiber-optic local area network cost and a challenge to coaxial cable.
The IC ties directly to the PIN or avalanche photodiode at the receiving end of an optically coupled data link. There it converts the current output of the diode in a voltage suitable for further processing.
Signetics Single
1Mbit DRAM Con
Handles 40ns Acc
SUNNYVALE, CA, May 23, 1988—
Signetics announced today a new series of 1Mbit dynamic RAM controllers that offer synchronous single- and dual-port operation at 100MHz—providing arbitration, signal timing and refresh address generation for DRAMs up to 40ns.
The 74F1764 and 74F1765 are
Signet
for Me
AS AN
x 8 RAM, two
rs, a full duplex
and Boolean
offer the high
characteristics
low power attri-
e part has 64K
data memory
system
random
a for dis-
tions can
with no
Signetics HS641
Marks Entry Into
CMOS EPROM Market
SUNNYVALE, CA, May XX, 1988—Signetics today announced its entry into the High Performance segment of the CMOS EPROM market with the unveiling of an 8K x 8 device that offers bipolar speed and CMOS low-power performance at competitive pricing.
"Our part is one of the fastest of its kind on the market," said Terry Leeder, vice president and general manager of the Application Specific Product division for Signetics. "And Signetics has the added advantage of being the only high-volume producer to introduce this type of device."


We've got the essentials that improve total design performance.
The guts, without which there is no glory.
For you—or us.
One standard. 0 defects.
Signetics
a division of North American Philips Corporation
PHILIPS
PHILIPS
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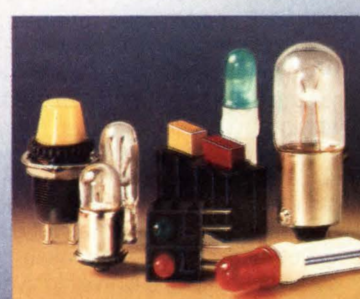
®PAL is a registered trademark of
Monolithic Memories Inc., a wholly-owned subsidiary of
Advanced Micro Devices, Inc.

VCH 9, other miniature lamp suppliers 0.

	VCH	Other Suppliers
Technical Support	In a few hours	In a few weeks
On-going reliability life testing	Yes	No
Chomaticity Tests, X or U' & Y or V' Coordinates	Yes	No
Failure Analysis Reports	Yes	No
Lamp performance data to M.S./A.N.S.I. standards	Yes	No
In-house Chromaticity and M.S.C.P. measurements	Yes	No
Environmental Test Data	Yes	No
Application and specifications development assistance	Yes	No
Just-In-Time delivery program	Yes	No

It's this simple: If your company produces world-class products, you should have world-class components. Can your present miniature lamp supplier provide all you get with VCH? Check the score. It's just no contest.



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Buffalo Grove, IL · 312-459-3400

We're out to be the beacon of miniature lamps.

The VME Volksclosure. $995. Ready to Run.

Finally. The economies of mass production catch up with VME and Multibus II enclosures.

Introducing the Volksclosure, Electronic Solutions' economy model enclosure with turbo performance. All you do is add cards and peripherals for a complete, attractive desktop computer.

With the Volksclosure (also known as our Model One) everything comes standard: six VME or Multibus II slots, space for three half-height 5¼″ disk drives, and a high-performance six-layer backplane all in a highly tooled enclosure with our handsome front panel that hides those ugly connectors and cables.

You do get a choice between two multiple-output power supplies: 190 Watts with 19A at +5V or 270 Watts with 30A at +5V. You can also choose a J2 backplane for VME extended addressing or iLBX II for a Multibus II system.

Most important, while the Volksclosure costs less, you don't get less. It fully reflects Electronic Solutions' commitment to quality and performance. For example, it meets UL and CSA safety standards and FCC Class A EMI/RFI specs to the letter.

THREE YEAR 3 LIMITED WARRANTY

The New Volksclosure. How to get a lot more mileage from your packaging budget. Call right now for complete details.

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Want the latest data in a hurry? Nothing is faster than Electronic Solutions' new "FAX the FACTS" program. If you have a FAX machine, just call our "800" number, give us your FAX number and type of FAX machine, and the information you need from us. We'll FAX it to you immediately.

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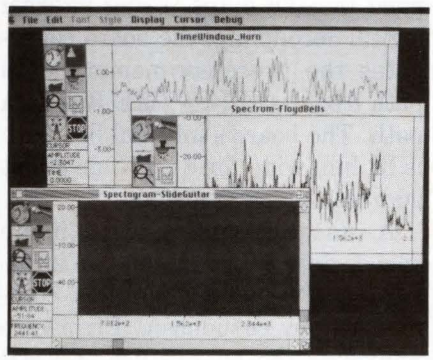
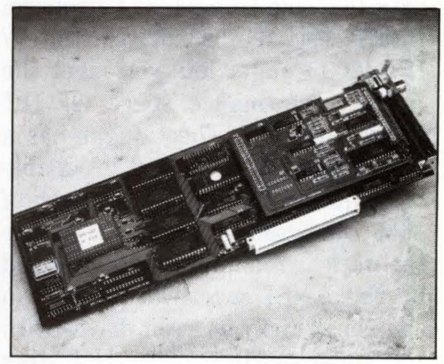
CIRCLE NO 57

DSP board and menu-driven software tools perform signal analysis on a Macintosh II





The signal-analysis software and DSP board *included in the MacDSP package converts a Macintosh II into a real-time interactive DSP workstation.*

The MacDSP add-in card and software tools for the Macintosh II provide users with an interactive menu-driven signal-analysis system. You can specify the DSP card in 8M-, 12.5M-, or 25M- flops speed grades. When used with a data-acquisition daughter card, the DSP board can acquire data at a 125-KHz rate, process the data, and display the data in real time.

The MacDSP employs the AT&T DSP32 floating-point digital-signal processor. The processor can perform multiply-accumulate operations in a single instruction cycle, thereby offering far superior computational power than the Macintosh 68020 native μP. You can employ the card in computationally-intensive applications, such as signal processing, image processing, and graphics.

Equally important, the DSP board comes with a menu-driven application-layer software package. You control the software via the Macintosh mouse and standard icon-based user interfaces. DSP chips are readily available, but you must develop code for a specific application to take full advantage of the chips' speed. However, the MacDSP software does include a complete application package for signal analysis.

For example, the software can perform modulation; FFTs; spectral averaging; Hilbert transforms; Hamming, Blackman and Kaiser windows; and Butterworth, Chebyshev, FIR and elliptic IIR filters. Furthermore, all of the signal-processing functions are performed and can be displayed in real time. The DSP board makes the real-time video-display rates possible by acting as a rasterizing coprocessor to the Macintosh CPU. You can display data in a variety of formats, such as magnitude, phase, color spectogram, and waterfall; and you can manipulate the screen image with functions such as log scaling, zoom, and maximum amplitude hold.

You can apply the signal-processing functions to incoming data from the data-acquisition daughter card, to data stored in main memory (800k samples/sec max), and to data stored on disk (70k samples/sec max). Using the mouse and pull-down menus, you can configure analog/digital inputs/outputs and control parameters such as sample rate and buffer size. Frequently-used setups can be saved as documents.

The software package supports multiple windows, therefore, you can simultaneously display and compare the results of different DSP operations. And, you can change the type of function being applied to data on the fly. You can also modify parameters such as cutoff frequency on the fly.

Finally, you can easily develop other applications for the board. The onboard firmware allows access to all processor registers from high-level Macintosh driver functions. You can also call a library of DSP functions from a high-level language. The company plans to add functions for filter design, linear predictive coding, and adaptive equalization. You can also develop custom code for the board with AT&T's (Allentown, PA) DSP32 C compiler.

The 8M- and 12M-flops versions of the board are available now and cost $2249 and $2745, respectively. The price includes the DSP board with 64k bytes of memory and the menu-driven software. The 25M-flops board should be available by the end of the year for $3241. In addition, the 125-KHz, 16-bit A/D and D/A card costs $486.

—Maury Wright

Spectral Innovations Inc, 292 Gibraltar Dr, Suite A-4, Sunnyvale, CA 94089. Phone (408) 734-1314.

Circle No 721

IPI controller for VME systems provides 36M-byte/sec data transfer

If your VME design calls for faster data I/O from Intelligent Peripheral Interface (IPI) disk drives, the V/IPI 4260 Cougar lets you meet the ANSI performance specs for IPI Level 2 (IPI-2). The Cougar has a bus-packet interface that is capable of transferring data in excess of 36M bytes/sec—that's 90% of the theoretical maximum rate defined by the ANSI spec. One board can control as many as eight drives with 1:1 interleaving. The IPI disk drives currently provide transfer rates reaching 3M bytes/sec, and the next generation of IPI-2 drives are expected to offer transfer rates as high as 6M bytes/sec.

Based on a 16-MHz 68020, the $4995 Cougar comes with a 256k-byte data buffer that you can expand to 512k bytes. Using internal logical decoupling, the board segregates the processor/memory data path from its IPI-to-VME Bus data path. The board's internal bus path is 32 bits wide for 8-, 16-, or 32-bit addressing and transfers.

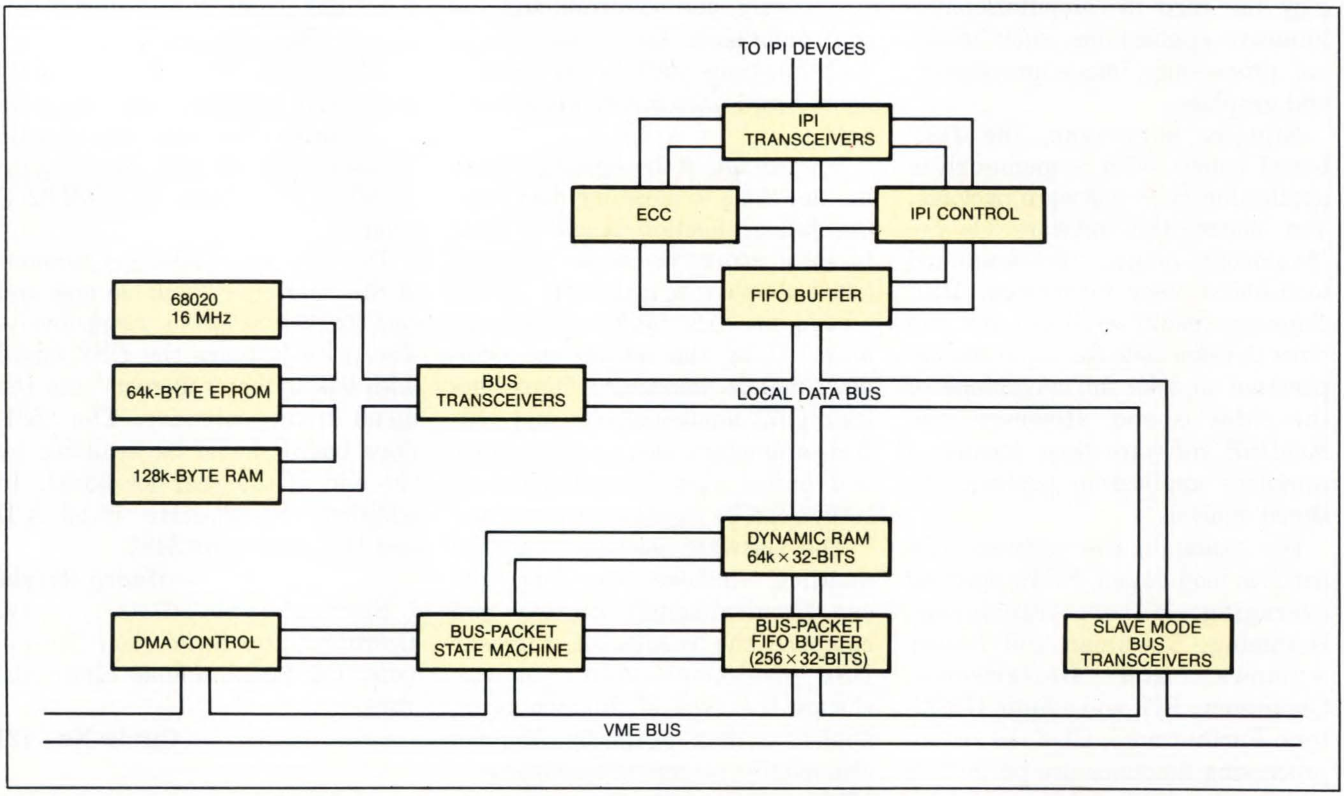
A data-streaming IPI mode speeds data transfers, and an interlocked IPI mode simplifies commands and responses. Firmware minimizes the board's use of VME Bus bandwidth. The board also accommodates VME Bus Sequential Mode transfers, and hardware switches let you select from four bus priority levels.

A proprietary software interface creates individual work queues for each of the IPI devices controlled by this board. Even drives with different data rates can co-exist under the Cougar's control. This capability reduces host-system overhead and boosts operating efficiency.

A Unix-optimized caching algorithm provides zero-latency reads and writes. You can use software-programmable interrupt levels, vectoring, address modifiers, and DMA burst rates to boost your system's performance. Error-correction code and error-recovery tools ensure data integrity and seamless recovery from IPI device faults.

—***J D Mosley***

Interphase Corp, 2925 Merrell Rd, Dallas, TX 75229. Phone (214) 350-9000. **Circle No 722**



Controlling as many as eight IPI-2 disk drives at data rates reaching 10M bytes/sec, *the V/IPI 4260 Cougar from Interphase Corp also sports intelligent features such as error correction and programmable address modifiers.*

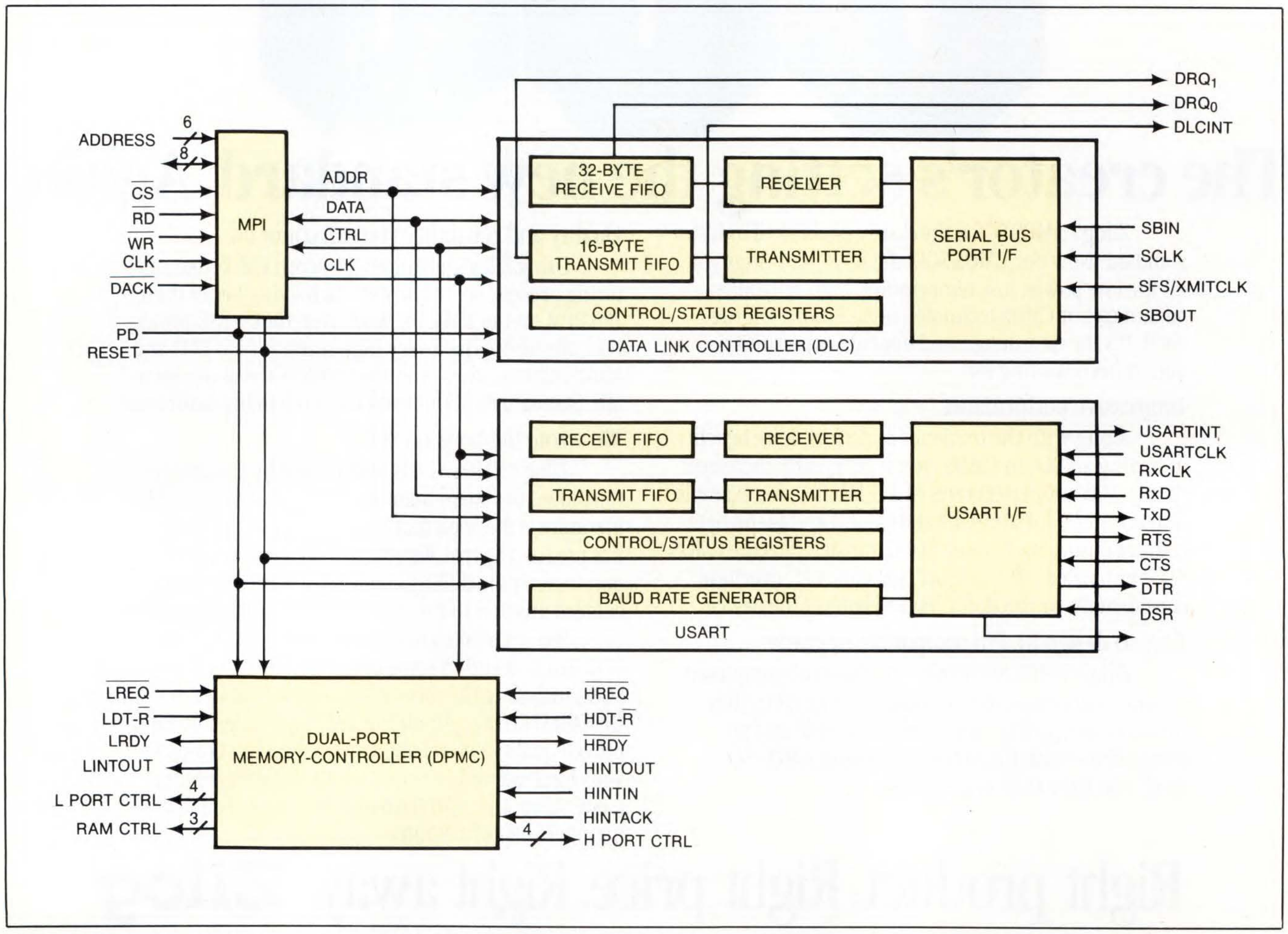
Packet communications controller IC includes USART and memory controller

Combining a data-link controller (DLC), a universal synchronous/asynchronous receiver/transmitter (USART), and a dual-port memory controller (DPMC) in a single IC, the Am79C401 Integrated Data Protocol Controller (IDPC) provides a platform for intelligent ISDN, X.25, SNA, and LAN communication processing. You can use the IDPC in any network that operates at speeds below 2.048 MHz and uses a packet protocol other than Bisync.

The IDPC reduces the host CPU's overhead by providing bit-oriented communication processing for multiple protocols, direct register addressing, and a serial interface that accommodates as many as 31 8-bit channels. The chip operates with zero wait-states when used with a 12.5-MHz 80188 μP. A power-down mode reduces the chip's idle power consumption but maintains program data.

The DLC provides the IC's packet network interface, and the USART gives the chip its terminal interface capability. The DPMC lets you build an inexpensive shared memory interface to your host system. Designed in conjunction with AT&T, the IDPC suits such applications as terminal-to-mainframe communications, instrumentation and industrial control networks, point-of-sale terminal networks, and ISDN terminal adapters.

The chip supports HDLC, SDLC, LAPB, LAPD, and DMI communication protocols at a maximum data



Suitable for use in ISDN, SNA, X.25, and local-area networks, *the Am79C401 Integrated Data Protocol Controller (IDPC) includes a data link controller, a dual-port memory controller, a μP interface, and a universal synchronous/asynchronous receiver/transmitter.*

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The 10Hz to 500MHz range of the HP 4195A make it ideal for audio, baseband, HF, VHF, and IF applications. A unique feature is four-channel spectrum measurement capability that accommodates four independent inputs. The unit features an internal flexible disk drive, color CRT, User Math, User Defined Functions, User Programs for customization—and it's softkey menu driven, making it extremely friendly. As usual, HP delivers value.

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CIRCLE NO 59

transfer rate of 2.048M bps. Certain HDLC Layer-2 functions are supported in the chip's hardware to reduce software requirements: short- and long-packet checking; received-packet length counting; Flag and Abort or Flag and Mark Idle generation and checking; bit-residue handling; and zero-bit inserting and deleting. A 32-byte receive FIFO buffer and a 16-byte transmit FIFO buffer have programmable thresholds and DMA handshake capability. The size of these buffers improves throughput and reduces real-time constraints on software.

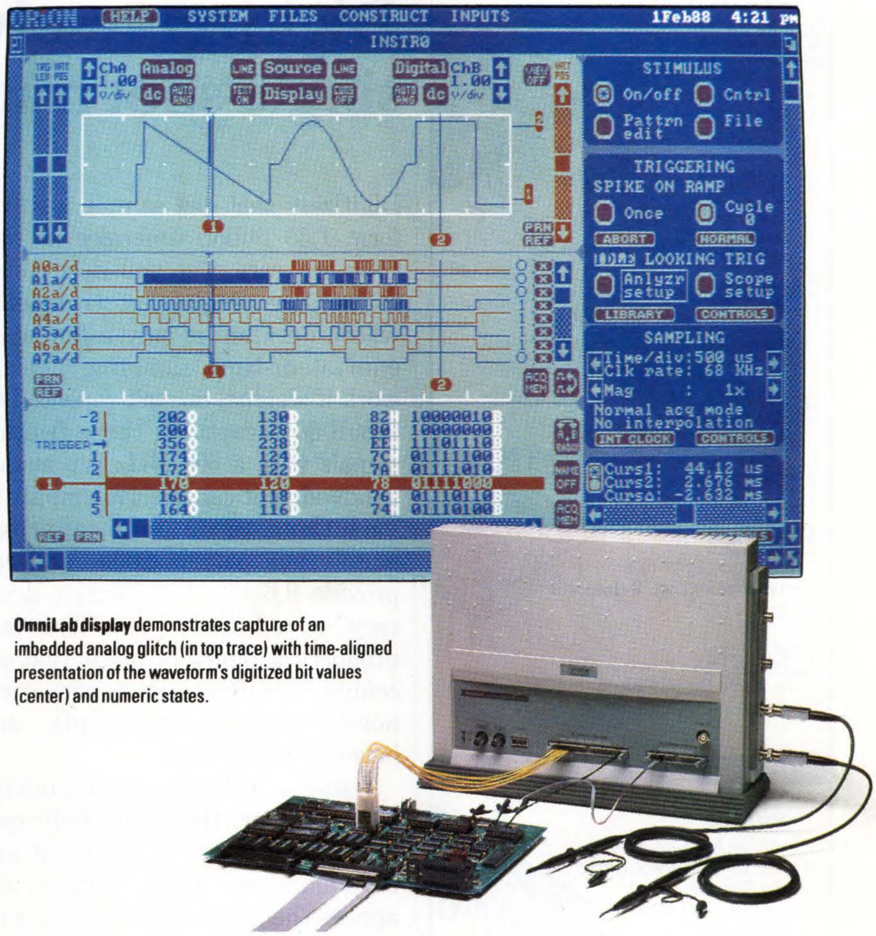
The IDPC includes multiple address recognition in the form of four programmable 8- or 16-bit addresses, a hard-wired broadcast address, and first- or second- byte address selection. You can access an optional command/response bit detection feature, as well as local- and remote-loopback diagnostic modes. The chip's serial interface lets it operate either in a non-multiplexed or a 31-time-slot multiplexed mode. A status-stacking mechanism improves interrupt latency and lets the chip receive as many as four sequential packets.

Software for the Am79C401 includes the $18 (100) Am79LLD401 Low-Level Driver, which provides a common interface to higher layers of software. You can buy the IDPC as a 68-pin PLCC or LCC device for $20.52 (100). The ITC Board, a plug-in PC-compatible evaluation board, sells for $1750.—***J D Mosley***

Advanced Micro Devices, Box 3453, Sunnyvale, CA 94088. Phone (800) 538-8450. TLX 346306. TWX 910-339-9280.

Circle No 723

Introducing OmniLab 9240.
Totally Integrated Scope-Analyzer-Stimulus.



OmniLab display demonstrates capture of an imbedded analog glitch (in top trace) with time-aligned presentation of the waveform's digitized bit values (center) and numeric states.

■ Combine a 100 MHz digital oscilloscope with a time-aligned, 200 MS/s 48-channel logic analyzer. Next add synchronized analog **and** digital stimulus generators. Then a remarkable new triggering system. What you have is the 9240 — a whole **new class** of instrumentation. Expressly designed to speed challenging analog and digital analysis. And get you from concept to product faster.

■ The 9240 is based on an innovative new instrument architecture that merges high-speed universal hardware and seamlessly-integrated software to create high-performance capabilities not available in separate instruments. Analog and digital traces are always time-correlated in a unique, single screen display. SELECT™ triggering bridges scope and analyzer techniques. And OmniLab's stimulus generators can playback captured or edited signals.

■ At the heart of the 9240 is SELECT triggering, the most straightforward and complete solution **ever** to triggering dilemmas. It's one system, operating with synchronized analog and digital views of your data. By combining conventional oscilloscope and analyzer triggering with powerful RAM truth tables — plus min/max time qualification as needed — SELECT triggering helps you analyze hardware, debug software, and integrate systems more easily.

■ OmniLab™ is a generation ahead of conventional digital scopes that often hide rarely occurring faults because they only show you a few cycles out of millions. With its continuous monitoring, you can use SELECT triggering to quickly catch every occurrence of rare events like metastable states, bus contentions, missing pulses, and buried noise glitches.

■ The 9240 is like having a complete benchtop of instruments integrated with your PC/AT or compatible. Which you can easily customize for digital development, analog development, or a combination of both.

■ With OmniLab, your productivity will soar. Because you achieve results with fewer instruments. And in fewer steps than ever before. By no means least, the 9240 delivers the best price/performance you'll find anywhere, costing just $8900 fully outfitted. And most importantly, without compromising a single high-performance spec. Not a one.

NO-COMPROMISE 9240 SPECIFICATIONS

DIGITAL OSCILLOSCOPE	
Digitizers:	Two, 8 bit
Bandwidth:	100 MHz
Single-Shot Digitizing:	34 S/s to 204 MS/s
Repetitive Sampling:	680 MS/s
Scale Factor:	5 mV/div to 10V/div in 1-2-5 sequence
Record Length:	4K (16K, 64K optional)

LOGIC ANALYZER	
Inputs:	48, timing and state
Asynchronous Clocking:	34 MS/s on 48 inputs; 204 MS/s on 8 inputs
Repetitive Sampling:	680 MS/s on 48 inputs
Synchronous Clocking:	0 to 34 MS/s
Acquisition Memory:	4K samples (16K, 64K optional)
Disassembly Options:	Over 150 microprocessors

ANALOG STIMULUS	
Output:	8mV to 8 V peak-to-peak, 8 bit
Cycle Length:	4 to 4K samples (16K optional)
Clocking:	34 S/s to 34 MS/s
Functions:	Record, edit and playback

DIGITAL STIMULUS	
Outputs:	24, 74F tri-state drivers
Cycle Length:	4 to 4K samples (16K optional)
Timing:	34S/s to 34MS/s
Functions:	Record, edit and playback

■ For more information, call **toll free 800/245-8500.** In CA: 415/361-8883. Or write for complete literature.

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Computer Integrated Instrumentation

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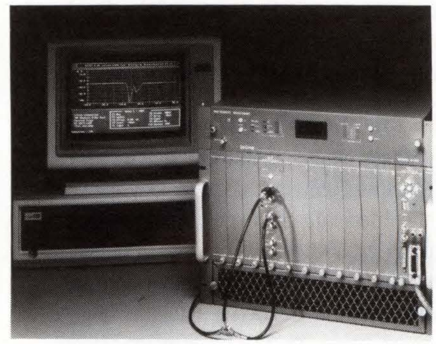
CIRCLE NO 60

Digitizer resolves 500-MHz, single-shot transients to 11 bits

Digitizers that can sample a waveform 1.35 billion times/sec *in real time* are rare, yet you need them to capture single-shot transients whose duration is only a few nsec; equivalent-time sampling doesn't work if a signal doesn't repeat. The 6880B/6010 captures these fleeting signals with a 500-MHz typ analog bandwidth; it can resolve amplitude variations to 11 bits—approximately one part in 2000—and can provide 9.6 bits of "effective accuracy" in a "sine-fit" test. This test produces a figure of merit that accounts for differential nonlinearity, noise, aperture uncertainty, and harmonic distortion.

Using a charge-coupled-device (CCD) buffer, the 6880B/6010 captures "snapshots" of the input signal's amplitude every 750 psec and applies them at a slightly lower rate to a flash A/D converter. The unit can store 10,000 digitized samples in its waveform memory. According to the vendor, the entire digitizing process appears to occur in real time.

When you capture repetitive waveforms with the 6880B/6010, you get a bonus: Through signal averaging performed by a 68020 µP combined with a 68881 arithmetic coprocessor, the resolution improves to 14 bits—but the unit can average a maximum of only 330 waveforms/sec. Besides averaging waveforms, the unit's processors correct for all CCD-induced errors and systematic "noise"; they also control autocalibration to maintain the digitizer's accuracy. You don't have to have a computer to operate the digitizer; you can control operation manually from the front panel.



Coupled to a personal computer, *this waveform digitizer becomes a digital oscilloscope with a 500-MHz bandwidth for single-shot transients and 14-bit resolution for repetitive waveforms.*

To facilitate computer control, however, the unit includes IEEE-488 and RS-232C interfaces.

To form single- or multichannel digitizing systems, as many as six 6880B waveform digitizers team with a 6010 controller and fit in an 8013 benchtop instrument chassis, or in a 1434A or an 8025 rack-mount "mainframe." The vendor also provides prepackaged configurations that include one or two digitizers, a controller, a benchtop chassis, an IEEE-488 cable, and PC-based oscilloscope software. A single-channel benchtop system of this type costs $20,450; a 2-channel version sells for $33,350. The price of the 6880B alone is $14,500.

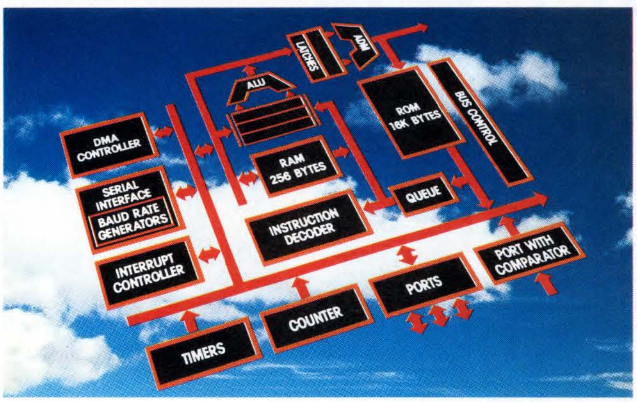
—Dan Strassberg

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 425-2000. TWX 710-577-2832.

Circle No 720

Simplify your life with single source supply.

THE MOST POWERFUL 16-BIT SINGLE-CHIP MICROCOMPUTER.



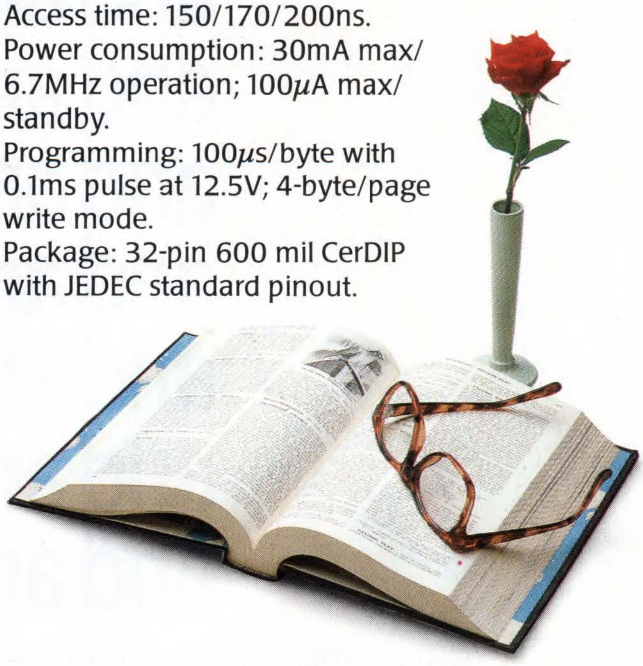
Offering higher integration, higher speed and enhanced functionality, the V25 meets more of your design needs. Which is why so many innovative designers are choosing the V25 for their 16-bit micro-based systems.

- □ High integration: programmable interrupt controller; 2-channel serial I/O port; three 16-bit timers; time-base counter and more.
- □ High speed: 16/32-bit temporary register/shifter; 16-bit loop counter and prefetch pointer.
- □ Enhanced interrupt handling: 8 programmable priority levels, hardware context switching for 8 register banks; 8-channel macro service controller.
- □ Two stand-by modes: halt and stop.

THE FIRST 2M-BIT CMOS EPROM.

NEC has just launched UV EPROMs into the 2M-bit era. The new μPD27C2001D gives you 2M-bit capacity in a 256K x 8 organization. High integration is complemented by high speed. With access times as fast as 150ns, our 2M-bit devices eliminate wait states for your CPU. Programming is also fast at 100μs per byte. The 4-byte page write mode multiplies programming speed.

- □ Organization: 256K x 8.
- □ Access time: 150/170/200ns.
- □ Power consumption: 30mA max/ 6.7MHz operation; 100μA max/ standby.
- □ Programming: 100μs/byte with 0.1ms pulse at 12.5V; 4-byte/page write mode.
- □ Package: 32-pin 600 mil CerDIP with JEDEC standard pinout.



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C&C Computers and Communications

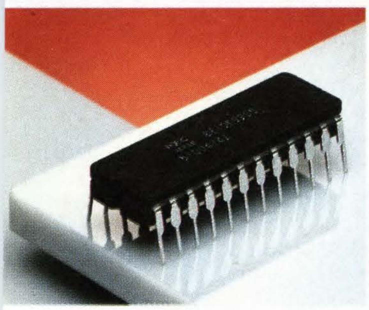
When you're buying semiconductors, multiple vendors can cause major mixups. To simplify everything, build a committed single-source relationship with one supplier: NEC.

We're the world's largest semiconductor manufacturer. We offer the industry's broadest lineup. The technology and quality of our components have made us an international leader in computers, communications and home electronics.

How do you get volume, variety, on-time delivery and applications support across the full spectrum of your semiconductor needs? It's simple. Build a single source relationship with NEC.

THE FASTEST 4K-BIT ECL RAM.

Read and write speeds are the critical parameters for ECL RAM performance. NEC has cut access time to 5ns and write cycle time to 7ns with our new ultra-fast 4K-bit ECL RAMs. How did we boost performance that high?



By using super-shallow junction transistors, trench isolation technology and Schottky diode clamp-type memory cells. Both ECL 10K (μPB10474A) and 100K (μPB100474A) interface devices are available.

- □ Organization: 1K x 4.
- □ Access time: 5/7ns.
- □ Power consumption: 1.2W.
- □ Package: 10K – 24-pin ceramic DIP; 100K – 24-pin ceramic DIP/QFP.
- □ Broad line of other ECL RAMs available: from 1K to 16K-bits; supplied in a diversity of organizations and speeds.

FAST AS A FLASH: 1M-BIT DUAL-PORT GRAPHICS BUFFER.

NEC's new megabit dual-port buffer chip is designed for super fast graphics processing. A unique "Flash Write" function clears the screen in a flash. The 256K x 4 RAM port allows bit write and fast page mode for high-speed bit operations. The 512 x 4 serial port operates at clock speeds up to 33MHz to handle high resolution graphics. To add value to your image processing system, design-in our μPD42274.

- □ Speed: RAS access – 100/120ns; CAS access – 25/30ns; serial read cycle – 30/40ns.
- □ Power consumption: stand-by–3mA; random read/write (serial port active) – 100/90mA.
- □ Package: 28-pin 400 mil ZIP and SOJ.*

**Under development.*

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Taiwan Tel:02-522-4192. Telex:22372.
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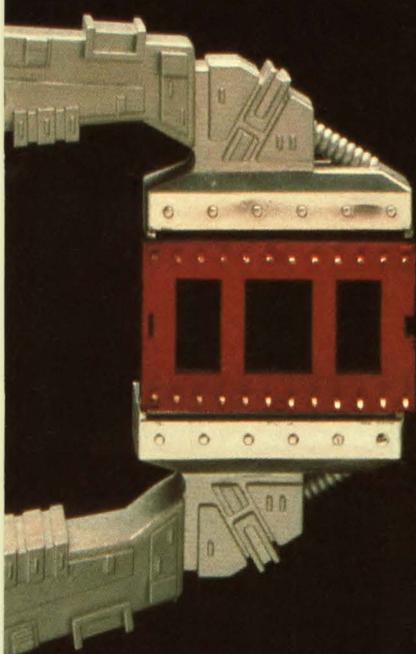
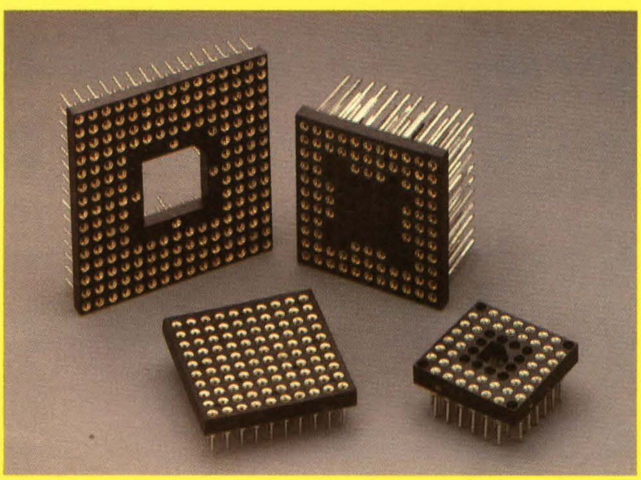
Australia Tel:03-267-6355. Telex:38343.

NEC



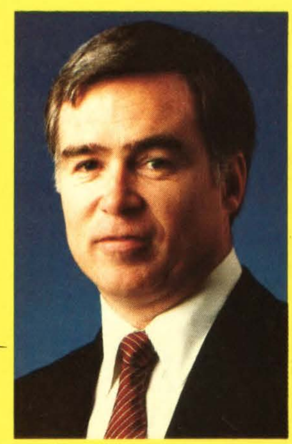
The RN "Partners in Quality Team" delivered precision sockets that made automatic assembly possible!



Application Specific PGA Sockets
Robinson Nugent offers a wide variety of Pin Grid Array Sockets for your ASIC's. They feature: High temp bodies for wave soldering • Disposable pin carriers for zero profile contacts • Sizes, 8x8 up to 21x21 with unlimited configurations • Extraction tools available • Molded standoffs for socket body. Write today for complete new PGA catalog.

"The RN 'P/Q TEAM' concept brings all of our design, engineering and production skills to bear on *your* unique socket/connector problems. We work closely with your people to create solutions that are delivered on-time and defect-free. *You have my personal guarantee on it.*"

R. A. Lindenmuth
President/CEO



Write or call today for the comprehensive new brochure: *"The RN P/Q Team in Action".* You'll learn how smart companies are putting the brains, resources and experience of RN engineers to work to solve tough interconnection problems with speed and efficiency.

The RN "P/Q TEAM"...your Partners in Quality

CIRCLE NO 62

INGENUITY

Amoco's three new microlasers are making the competition see green.

Three new, green-light microlasers are being introduced by Amoco Laser. The 1-3/4" diameter by 4" long laser heads produce green light in the 1 mW to 15 mW range.

Major applications for these lasers include reprographics, color separation, and spectroscopic instrumentation.

The standard green microlasers, the ALC 532 Series, are designed for use in applications such as pointing and display where excellent beam quality is essential, but low noise and high stability are not required. The ALC 532HS Series, with 1% RMS noise and +/-5% long-term stability, is designed for use in film scanning, color separation, and laser-based instrumentation for spectroscopic and scientific applications.

And the ALC 532SF Series, with single-frequency output, a fraction of a percent RMS noise, and exceptional long-term stability, will find use in interferometry, holography, and a variety of specialized research and development applications.

For more information, write us. We have prepared material, including a video tape, that more thoroughly examines the technology and uses of Amoco's entire family of microlaser products. Just write Amoco Laser Company, 1251 Frontenac Road, Naperville, IL 60540. Or phone our marketing group at (312) 961-8400.

AMOCO

Amoco Laser Company

CIRCLE NO 63

146-1629

NEW! KEPCO 100 WATT BENCH TYPE LINEAR POWER SUPPLIES

WITH UNIQUE "PREVIEW" FEATURE

SERIES MSK

KEPCO® THE POWER SUPPLIER™

Model MSK 10-10M

KEPCO, INC. • 131-38 SANFORD AVENUE • FLUSHING, NY 11352 USA • (718) 461-7000 • TWX #710-582-2631 • FAX: (718) 767-1102

MSK STATIC SPECIFICATIONS

INFLUENCE QUANTITY		VOLTAGE MODE *	CURRENT MODE *
Source: 105-125/210-250V a-c		0.01%	0.01%
Load: No load – full load		0.01%	0.05%
Time: 8-hour drift		0.01%	0.02%
Temperature: Per °C		0.01%	0.02%
Ripple and noise	rms	0.5mV	0.02%
	p-p	3.0mV	0.1%

* Note: Percentage values are referenced to the maximum rated voltage or current of the unit.

MSK GENERAL SPECIFICATIONS

SPECIFICATION	RATING/DESCRIPTION	CONDITION
INPUT		
Voltage	105-125/210-250V a-c	User selectable (rear switch)
Current	2.8A rms max	Maximum load, 115V a-c
Frequency range	47-63 Hz	
OUTPUT		
d-c output	Transistor	Series pass
Type of stabilizer	Automatic crossover	Voltage/current
Voltage adjustment range	0-100% of rating	0 to +45°C
Current adjustment range	0-100% of rating	0 to +45°C
Error sense	0.5V per load wire	Voltage allowance(1)
Voltage recovery	50 μsec typ, 100 μsec max	Step load change between 10% and 100% I_O max
Isolation voltage	500V d-c or peak	Output to ground
Leakage current	<5 microamperes	rms at 115V a-c
Output to ground	<50 microamperes	p-p at 115V a-c
OVP	Crowbar SCR	Transient 10msec or more
CONTROL		
Voltage	10-turn precision rheostat	
Current	10-turn precision rheostat	
MECHANICAL		
Input connections	IEC detachable line cord	
Output connections	Front panel binding posts	Output, sense & ground(2)
Meters	Two 3½ LCD digital displays	Accuracy ½ least significant bit
Cooling	1800 rpm low noise blower	
Dimensions (H × W × D)	5¾(3) × 8⅛ × 13⁵⁄₃₂ 146 × 206 × 334	inches mm
Finish: Fed Std 595	Light gray, color 26440	Front panel, 2 tone
Weight (packed for shipment)	19 Lb. (8.6 Kg)	MSK 10-10M, 20-5M, 40-2.5M
	22 Lb. (10 Kg)	MSK 125-1M

This KEPCO product is backed by a firm 5-YEAR WARRANTY

(1) An additional volt is provided in the output beyond the rating for this purpose.
(2) Ground terminal permits grounding of either plus or minus output terminal.
(3) Including feet.

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NEW! KEPCO 100 WATT BENCH TYPE LINEAR POWER SUPPLIES WITH UNIQUE "PREVIEW" FEATURE • SERIES MSK

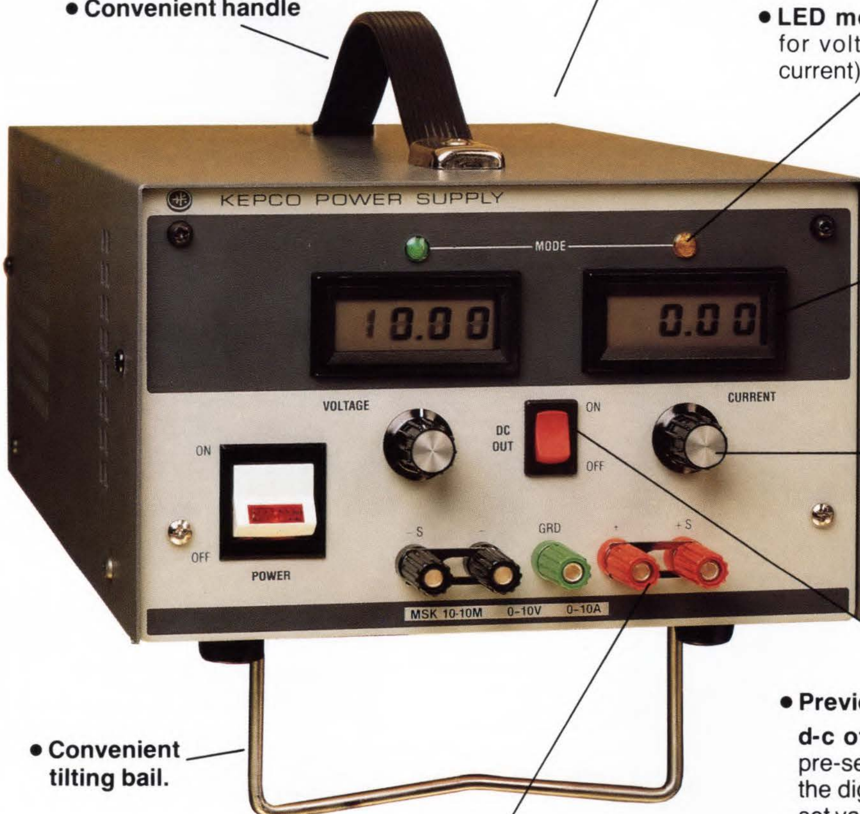
These new Kepco power supplies give you a selection of four models, offering 100 watts of stable benchtop power. They use a fully dissipative, high gain linear (series pass) stabilizer circuit, for low noise output, good stability, and accurate resettability.

- **Compact desk-top package.**
- **Competitively priced.**
- **5-year warranty.**

MSK MODEL TABLE

MODEL	d-c OUTPUT RANGE		POWER
	Volts	Amps	Watts
MSK 10-10M	0-10	0-10	0-100
MSK 20-5M	0-20	0-5	0-100
MSK 40-2.5M	0-40	0-2.5	0-100
MSK 125-1M	0-125	0-1	0-125

- **Built-in quiet, low-speed fan** ensures good cooling in the crowded environment of your laboratory. Fan is rated for 10 year life.
- **Convenient handle**
- **LED mode indicators** (green for voltage mode, amber for current).



- **Two 3½ digit LCD numeric displays.**
- **Front panel 10-turn precision controls for voltage and current, with automatic crossover between modes.**
- **Convenient tilting bail.**
- **Preview Switch (d-c on-off)**

  d-c off selection allows you to pre-set voltage and current with the digital meters displaying the set values. No voltage is applied to the output terminals and no load current needs to be drawn to set the current control.

  d-c on selection applies the set voltage to the output terminals. The appropriate mode indicator illuminates and the meters indicate *actual* voltage and current.
- **Convenient heavy duty front panel binding posts** that accept wires or mating "banana" plugs, allow easy connection to your breadboards and prototypes.

TEAR ON DOTTED LINE TO REMOVE AND SAVE.

Data subject to change without notice.

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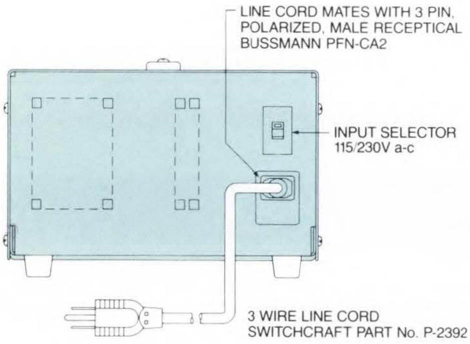
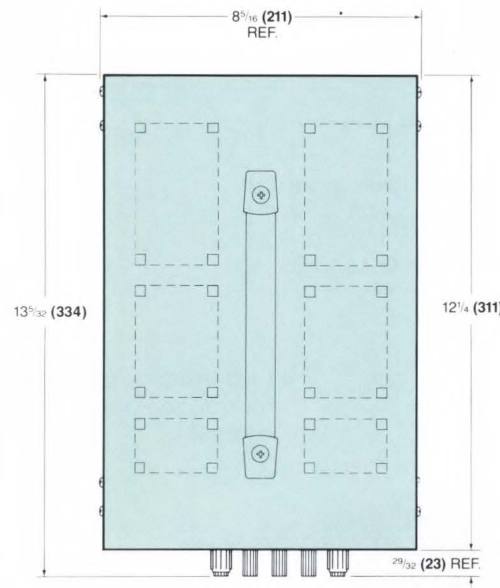
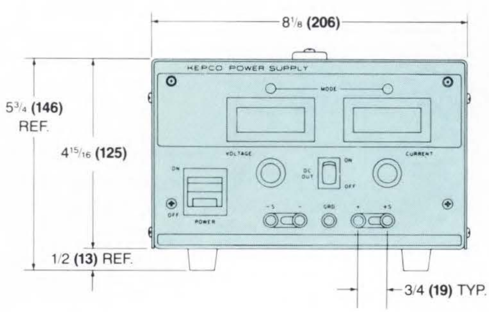
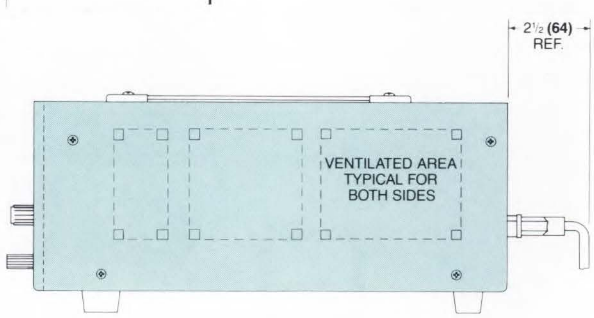
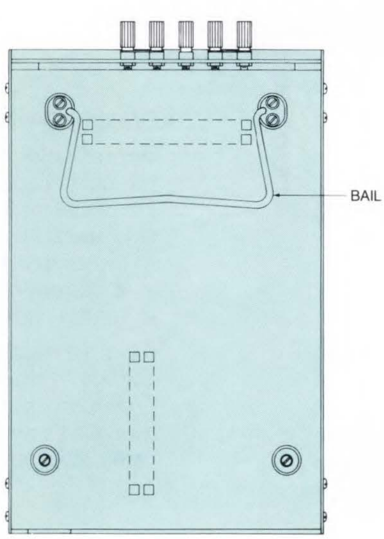
SERIES MSK











OUTLINE DIMENSIONAL DRAWINGS

Dimensions in light face type are in inches, **dimensions in bold face type are in millimeters.**

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CIRCLE NO 68

SPD-88-001

SPECIAL REPORT

EDN's DSP Benchmarks

David Shear, *Regional Editor*

Until now, DSP users have had to muddle through the selection process to find the right DSP chips for their designs, primarily because no comprehensive benchmark study has existed to guide them. To fill this need, EDN canvassed manufacturers and users, and then standardized some common benchmarks, and compiled and analyzed the resulting data on 18 general-purpose DSP ICs and 12 benchmarks. But in order to use these benchmarks, you've got to understand the overall evaluation process. And understanding that process is a bit like fathoming a Chinese puzzle. Neither one is an easy task.

Solving the evaluation puzzle takes time

Benchmarks are often misused and abused. They're cited out of context. Or they're considered in isolation from other design requirements. How a DSP performs in a benchmark, however, is just one piece in the evaluation puzzle. Other considerations are sometimes even more important. You need to figure out how speed relates to the other pieces of the puzzle, that is, how other design requirements, like cost, development tools, application aid, and ease of programming, interrelate (see **box,** "Evaluating DSPs: A worksheet"). What's more, you need to sort out just how the benchmark code affects the results. All in all, you'll probably find the evaluation puzzle is a fairly intricate problem, which you must view thoroughly and carefully from many different angles to resolve it intelligently.

EDN has done benchmarks before. Our 1981 benchmark survey caused something of a stir. Reader response was heavy and positive. In response to some manufacturers' criticisms, we published a follow-up article that re-presented the results and proposed the "Three Not-so-golden Rules of Benchmarking":

- Rule 1—All's fair in love, war, and benchmarks.
- Rule 2—Good code is the fastest possible code.
- Rule 3—Conditions, cautions, relevant discussion, and even actual code never make it to the bottom line when results are summarized.

And these rules still ring true today.

The third rule is especially important. We uncovered a tremendous amount of information during the process of gathering these benchmarks. Such a wealth of information makes contriving the conclusion you want mere child's play. But you can't reduce a benchmark to just one number. (Remember this third rule if you come across any condensed interpretations of our work.)

Why look at benchmarks at all?

When you're trying to decide which DSP to use in your design, raw speed is nevertheless a good place to start, and benchmarks are an excellent index to that speed. However it's also important to know the conditions under which the benchmark was run. Thus for each benchmark, you must be familiar with the exact specifications and the code in order to understand what the bottom line really means.

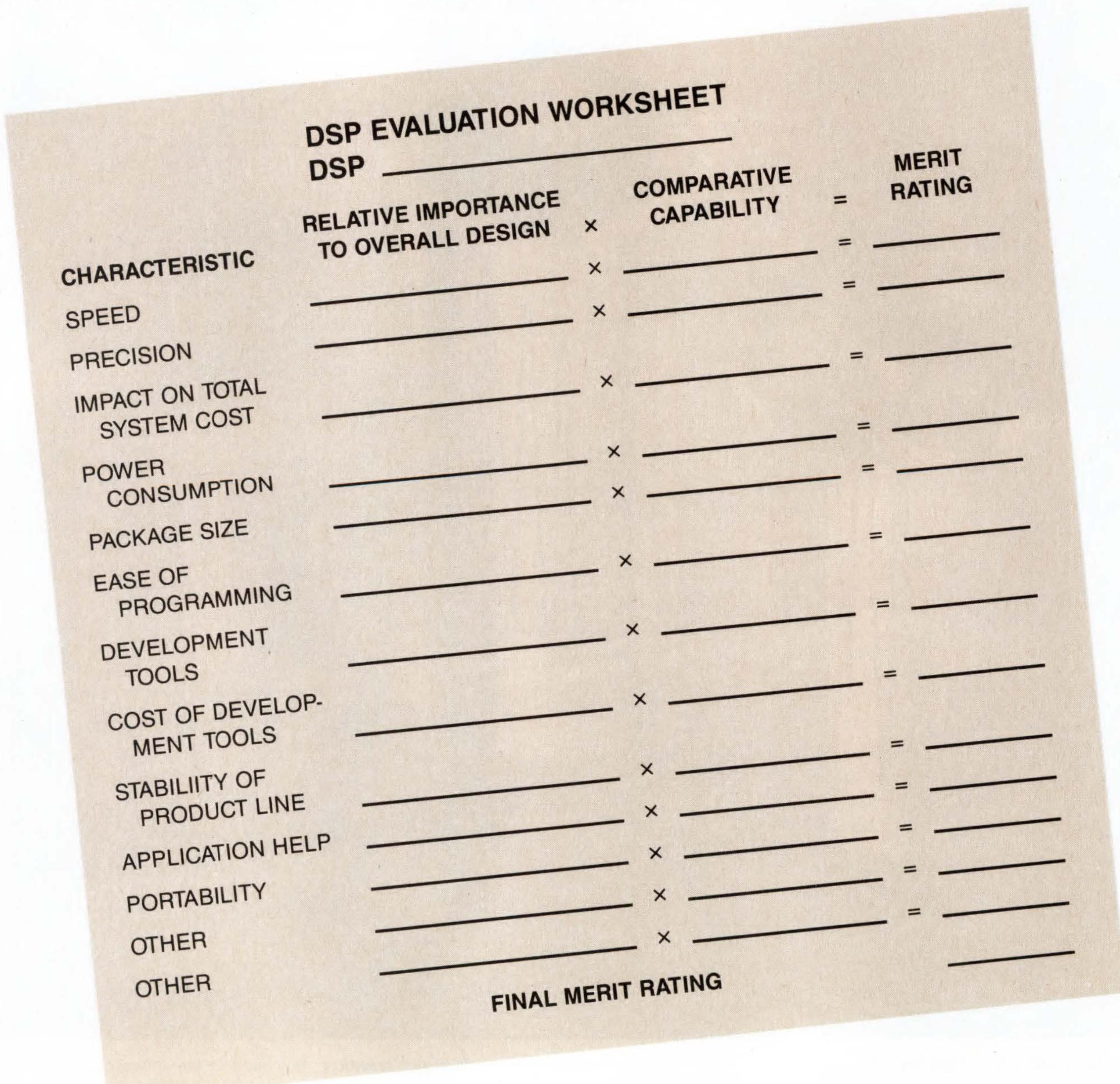
Starting last January, we asked DSP users about the types of applications they were designing. We also invited the major manufacturers of DSPs to submit their own descriptions of benchmarks sets. Initially, Finally, a comprehensive benchmark survey for DSP ICs. EDN solicited the help of some experts in the DSP field and then analyzed the results of 12 benchmarks on 18 general-purpose DSPs. We found that benchmarks, when used correctly, can tell you a lot more about an IC than just raw speed.

Although EDN's benchmarks often place some DSP chips above others in levels of performance, *you need to know how the results were reached and what the benchmarks mean in the context of other design requirements, when you're piecing together the evaluation puzzle. (Photo courtesy Texas Instruments)*

> You can learn a lot from the process of evaluating a DSP's speed. But it is also important to know the conditions of the measurement.

Evaluating DSPs: A worksheet

A worksheet below can help you evaluate the various aspects of a DSP you should consider when trying to decide which one to use in your design. To use this form, first determine the relative importance of each DSP characteristic based on your application (number 1 to 10, where 10 is the best). Then evaluate the capability of each DSP to perform that task in rough comparison with other DSPs on the same rating scale of 1 to 10. Multiply these two numbers together for each characterisitc and then add the last column to find the merit rating for that DSP. Use this final figure as a basis for comparing the DSPs.



DSP EVALUATION WORKSHEET

DSP ____________

CHARACTERISTIC	RELATIVE IMPORTANCE TO OVERALL DESIGN	×	COMPARATIVE CAPABILITY	=	MERIT RATING
SPEED	______	×	______	=	______
PRECISION	______	×	______	=	______
IMPACT ON TOTAL SYSTEM COST	______	×	______	=	______
POWER CONSUMPTION	______	×	______	=	______
PACKAGE SIZE	______	×	______	=	______
EASE OF PROGRAMMING	______	×	______	=	______
DEVELOPMENT TOOLS	______	×	______	=	______
COST OF DEVELOP-MENT TOOLS	______	×	______	=	______
STABILIITY OF PRODUCT LINE	______	×	______	=	______
APPLICATION HELP	______	×	______	=	______
PORTABILITY	______	×	______	=	______
OTHER	______	×	______	=	______
OTHER	______	×	______	=	______
			FINAL MERIT RATING		______

we selected 15 benchmarks for their resemblance to various typical applications. We then distributed the final specifications to all of our DSP manufacturers, and we asked them to respond within two months.

The final set of benchmarks include six filters: 20, 64-, and 67-tap FIR filters, along with three different 8-pole IIR filters. All of the filters programs acquire data from an analog-to-digital converter and send the results to a digital-to-analog converter. The IIR filters are based on two separate difference equations. The canonic type of IIR filter (also known as Direct Form II) is based on the standard difference equation. This type of filter normally requires five multiplications. It's possible, though, to divide all of the coefficients in each section by the coefficient b_{i0} of that section. This operation eliminates one of the multiplications—because it isn't necessary to multiply by 1— thus making the 4-multiplication canonic IIR filter possible. The transpose type of IIR filter (also called Direct Form I) is a variation on the standard difference equation.

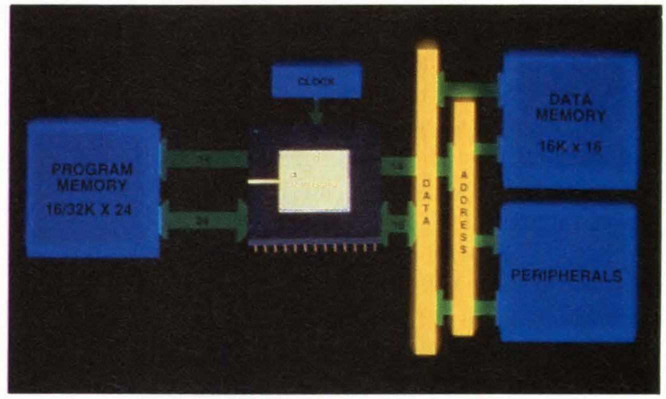
Not all of the filter benchmarks apply to every DSP chip. The 4-multiplication canonic IIR filter, for example, reduces the number of multiplications the DSP must perform but it creates more complex scaling problems. It's extremely difficult to use this algorithm on a 16-bit fixed-point machine, because you run out of resolution. Higher fixed-point resolution, such as the 24-bit Motorola DSP56000/1, can more easily exploit this algorithm. And floating-point DSPs have plenty of resolution, so the 4-multiplication canonic IIR filter is the algorithm of choice for those machines.

The three math benchmarks include a simple dot product and two matrix multiplications: a 2×2 times a 2×2, which results in a 2×2, and a 3×3 times a 3×1, which results in a 3×1.

The FFT: Useful but abused

The FFT is possibly the second most abused benchmark (the lowly MIP has the dubious distinction of first place). Over the years, marketers have corrupted the meaning of "the FFT" by arbitrarily touting FFT benchmark results for the DSP-of-the-month without specifying which FFT, or exactly what code, they are talking about. There are as many different FFTs as there are engineers using them, and every application has its optimized FFT version. Indeed, some experts spend considerable time shaving just one more instruction off an FFT.

At any rate, no set of DSP benchmarks is complete without at least one FFT. Originally, we specified six



The most common architecture for DSPs, *the Harvard architecture, has separate program and data memory and buses. The ADSP-2100A from Analog Devices brings these memories off of the chip and keeps them separate. Many other DSPs have separate memories on the chip but have to use a common memory when using external memory.*

of those algorithms. Later, we deleted three of them (64-, 256-, and 1024-point real-input complex FFTs) from this survey because of wide variations in the algorithms used and because of differing interpretations of the specification. Motorola and TI, for example, both used an optimized FFT that accepts real input and provides complex data (**Ref** 3). Other companies used a straight complex FFT (they inserted a 0 for the imaginary data as the real data was acquired). This discrepancy made a true comparison impossible. The code and results for these three benchmarks are, however, available on disk along with all of the other benchmarks and the results (see **box,** "To order you own DSP disks . . . ").

We intentionally made the FFT specifications vague because excessively restrictive ones might favor one DSP over some others. Certain architectures are, after all, better suited to optimize certain algorithms. But even this strategy didn't please everybody. TI's application experts thought the specifications were too vague; they prefer distributing complete Fortran programs, on which programmers would then base their DSP code. In contrast, the application experts at Motorola thought the specifications were too restrictive. They recommend that future benchmark specifications should just define the type of input and the type of output desired (in this case, a 16-bit ADC and complex data, respectively).

The benchmarks in this survey aren't intended to test the limits of the DSPs' capabilities but to reflect typical application needs. TI thought that the final specifications for the benchmarks were too simple.

> We selected 15 benchmarks for their resemblance to typical applications.

They submitted a 256-tap filter and a 15×15 matrix multiplication. But applications for these kinds of algorithms are rare. Furthermore, it's hard to interpret the results of a very complex benchmark for different applications. For those who may have a use for such complex applications, however, the code for these programs is in the disk set.

Most of the EDN benchmarks fit within the internal memory of the DSPs. Depending on the processor architecture, using external memory can slow speed. For the most part, DSPs get their high speed by using parallel data paths. If you use external memory but the parallel data paths remain on chip, the processor must wait for the completion of the serial access, much the same way a standard μP uses sequential memory accesses. Development tools often use external memory to operate. If this is the case, you may not be able to run the DSP at full speed during the development stage.

We decided to present the comparative-benchmark results in bar charts (they start on pg 136). Bar charts allow for easy and broad comparison: Differences of 5 to 10% aren't very obvious, but small differences are really not important. On the other hand, differences of 50 to 100%, which do matter, are readily apparent.

To order your own DSP disks . . .

For those who want to thoroughly understand the results of this study and for those who would like to review the optimized code used, you can order a copy of the DSP disk set by making out a $45 check or money order payable to "EDN DSP Disk Set"(CA residents add 6% sales tax for a total of $47.70). Send your check or money order to

EDN DSP Disk Set
Box 41412
San Jose, CA 95160.

The set consists of 9 IBM PC double-sided double-density 5¼-in. disks (360k bytes). Please be sure to include your return address. Allow six to eight weeks for delivery. This offer expires April 1, 1989.

Any given length of execution time requires some memory, so we put both values in the result charts for easy comparison.

EDN specifically defined the execution time and memory for the participating manufacturers as follows: "The execution time is the time it takes to execute the given benchmark. This does not include the time it takes to initialize the system or create lookup tables. It does include the time to initialize those items (registers, pointers, etc) that are required each time the routine is run.

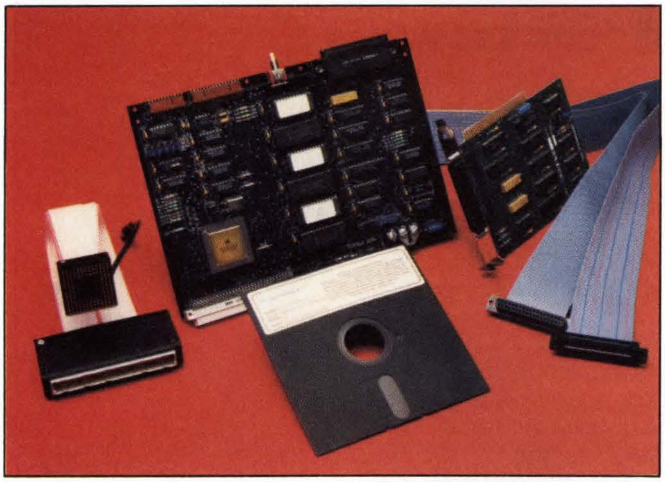
"The total memory required is the total number of words that the program requires. This includes executable code, initialization code, filter coefficients, delay data, twiddle factors, but-reversal look-up tables, and any other item that consumes some of the available memory resources of the DSP."

Hints from the experts can help

We've included the verbatim benchmark outline just below each of the 12 bar charts that compare the 18 products. The actual code that the companies used to determine the results is available on disk (see **box,** "To order your own DSP disks . . . "). This set of nine disks contains more than 2M bytes of optimized DSP code for filters, matrix math, and FFTs. Having available the programming techniques that the optimization experts use can be helpful during the development of programs for your specific applications. Some of the DSP manufacturers have also made the code that they submitted for this survey available on their bulletin boards. Complete and exact results, some with six digits of significance, are available on the disk set.

We divided the DSPs into three groups: fixed-point, floating-point, and future devices. The last group includes any DSPs not yet committed to silicon on July 1, 1988 (the deadline for the submission of the results). Consequently, some of these so-called future DSPs are now available. For instance, a few weeks after our deadline, SGS-Thomson started offering working silicon for the ST18930/31 and ST18940/41, which are in our group of future devices. So refer to the date of working silicon in the DSP profiles that begin on pg 142, and contact the manufacturers for availability updates.

The DSP profiles provide some background on the 18 devices covered in this survey. For more detailed information, see EDN's DSP Chip Directory **(Ref 4)** or contact the manufacturer directly. The prices provided in the profile are for low quantities (singles and



There is more to the evaluation of a DSP than performance. *The availability of software and hardware tools, like these from Motorola, are also very important. Make sure you consider all the pertinent design requirements when selecting your next DSP.*

100s). Larger-quantity prices can differ substantially: For example, the TMS320C30 costs $1300 in single quantities. By 1990, this part will cost $100 in quantities of 10,000.

A bar chart of relative speed accompanies each DSP IC profile. For each benchmark, we determined the slowest execution time, and then we compared each of the other DSPs with this slowest rate on a percentage basis. Therefore, the slowest execution time for any of the benchmarks represents 100%, and all other DSPs have lower numbers, reflecting their faster rates. For the most part, the DSPs with the slowest execution times are first-generation devices. These speed profiles thus offer some historical perspective and show how much newer devices have improved upon the older ones. Not all DSPs have results for each benchmark. Some manufacturers chose not to submit all benchmarks; others we had to disallow.

Each profile also contains the word size, format, and accumulator size for the DSP. The word size ranges from 16 to 32 bits; the format is fixed or floating point; and the accumulator size ranges from 22 to 96 bits.

The multiply-accumulate (MAC) time of a DSP as presented in the profiles is the time it takes the DSP to perform a MAC when the pipeline is full, not the MAC time from beginning to end. Most algorithms are developed to take advantage of pipelined MACs.

The results of the benchmarks don't reflect the precision of any of the DSPs. A fast 16-bit fixed-point device doesn't have the precision of a 24-bit fixed-point device. A 16-bit fixed-point number has a dynamic range of 96 dB while the 24-bit fixed-point number has a 144-dB dynamic range. The 32-bit floating-point devices have the highest precision with more than 1500 dB of dynamic range.

The size of the accumulator can also influence precision. Many algorithms use a multiply/accumulate series, where the results of the multiplications are added to what is already in the accumulator. The larger the accumulator is, the more times you can add results without encountering scaling problems. For example, the ADSP-2100A from Analog Devices is a 16-bit device with a 40-bit accumulator. This architecture allows two hundred fifty-five 32-bit results from the multiplier to be added to the accumulator without the possibility of an overflow.

Tests bypass ease-of-programming issue

Like precision, ease of programming is an issue these benchmarks don't address directly. The DSPs' highly parallel architectures and the complex addressing modes make high-speed operations possible, but they also make programming more difficult. When many memories are operating in parallel, it's impossible to include all the addresses in a single-word instruction. Consequently, you must use address registers to point to the desired memory locations.

A quick look at the code for three of the DSPs reveals a complex and foreign syntax for those of us familiar only with programming μPs **(Listing 1).** The complexity of the code stems partly from the parallelism of the devices, partly from capability of the DSPs to postmodify (that is, to modify the address registers after the execution of the instruction). By postmodifying, the processors point to the appropriate memory locations for the next instructions.

Filters are MAC-intensive

Filters rely on MAC operations heavily, so the benchmark results of the filters mirror the MAC times **(Fig 1).** DSPs are optimized for filtering algorithms. For each tap of an FIR filter, the processor must fetch an instruction, fetch the appropriate delay data, fetch the appropriate coefficient data, multiply the data, add the result to the accumulator, and shift the data in the delay data line—all in a single cycle. This sequence of operations in a single cycle is possible only when the pipeline is full.

The results in the comparative benchmark charts specify not the sample rate but the sample period (that is, the execution time of the filter program). To deter-

EDN's benchmarks don't address either precision or ease of programming directly.

LISTING 1—THREE DSP CODE SEGMENTS

a—DSP16

```
loop:    *r0=pdx0                /* Input data into RAM loc "ibuf."      */

                        /* Perform convolution  */

         /* 3 stage DAU pipeline is executed as follows: */
         /*                          y and x fetch   */
         /*                 multiply                 */
         /*      accumulate                          */
         /* Multiply and/or accumulate statements are    */
         /* permitted in an instruction with x,y fetches,*/
         /* but multiply and/or accumulation operations  */
         /* will be performed on data loaded in the      */
         /* previous instruction (user-visible pipeline).*/

                 a0=p               y=*r1++    x=*pt++ /* Fetch x(63) & h(63)*/
         do 62   {
                 a0=a0-p   p=x*y    y=*r1++    x=*pt++
                 }
                 a0=a0-p   p=x*y    y=*r0      x=*pt++i /* Re-init coef ptr  */
                 a0=a0-p   p=x*y    *r1++=y
                 a0=a0-p
                 pdx1=a0
endl:    goto    loop
```

b—DSP56001

```
         movep   y:input,x:(r0)            ;input sample in memory
         clr     a       x:(r0)+,x0        y:(r4)+,y0

         rep     #n-1
         mac     x0,y0,a x:(r0)+,x0        y:(r4)+,y0
         macr    x0,y0,a (r0)-

         movep   a,y:output                ;output filtered sample
```

c—TMS320C30

```
FIR      LDF     @PORT_IN,R2               ; input new data
;                                          ; initialize R0:
         MPYF3   *AR0++(1),*AR1++(1)%,R0   ; h(N-1) * x(n-(N-1)) -> R0
         STF     R2,*-AR1(2)%
         LDF     0.0,R2                    ; initialize R2.
;
; filter ( 1 <= i < N)
;
         RPTS    RC                        ; setup the repeat single.
         MPYF3   *AR0++(1),*AR1++(1)%,R0   ; h(N-1-i) * x(n-(N-1-i)) -> R0
||       ADDF3   R0,R2,R2                  ; multiply and add operation
;
         ADDF    R0,R2,R0                  ; add last product
         STF     R0,@PORT_OUT              ; output result
```

mine the maximum sample rate that each device can achieve, take the inverse of the execution time. Some manufacturers used in-line code (instead of looping) for those devices that do not have low overhead looping. The memory these filters consume is relatively small, so the sacrifice in longer program size for in-line code is not really significant.

Programmers tried to reduce memory use

The programmers used various methods to minimize the memory required while using in-line code to keep the speed high. The code for the DSP320C10 from Microchip Technology uses an immediate-multiply instruction. This instruction limits one of the operands to 13 bits. Those coefficients that need the full 16-bit word are loaded into RAM during initialization. Those that only need the lower 13 bits of the 16-bit word use the immediate-multiply instruction and do not consume available RAM. In fact, they don't take any extra memory at all, because these coefficients are embedded in the multiply instruction. The only difference in this approach from other filter implementations is the amount of memory consumed. On the 64-tap FIR filter, the DSP320C10 uses only eight 16-bit coefficients out of the required total of 64. If all 64 coefficients required 16-bits, the total memory needed would jump from 178 to 234 words.

Some DSP chips needed help

Not all of the DSP chips were capable of performing all of the benchmarks without the assistance of some external logic (in addition to external memory, addresses, decoders, and buffers). The TMS320C10 and the DSP320C10 both require external address counters to accomplish the larger FFTs; they both set those address counters via I/O. Then, each time external memory is used, the counter automatically increments its address to prepare for the next operation. This is a valid approach since these devices have limited internal data memory and can't access any external data memory directly. The cost of a couple of address counters is minimal, but don't forget their presence when considering these devices for use in calculating large FFTs. For all of the FFTs, the μPD77C25 needs the help of an external DMA controller to move data into and out of the DSP.

Three processors performed significantly better on the FFTs then they did on the other benchmarks, and these three also have faster relative speeds for the FFTs. Both SGS-Thomson and Motorola admitted that they have tuned their architectures to perform FFTs quickly. SGS-Thomson's ST18940/41 has a complex MAC instruction that executes in two cycles. It also has on-chip bit-reversal and three on-chip data memories. The Motorola DSP56000/1 and DSP96001/2 also have three separate memories and hardware bit-reversal. They also have special instructions (ADDR, ADDL, SUBR, and SUBL) written specifically for FFTs.

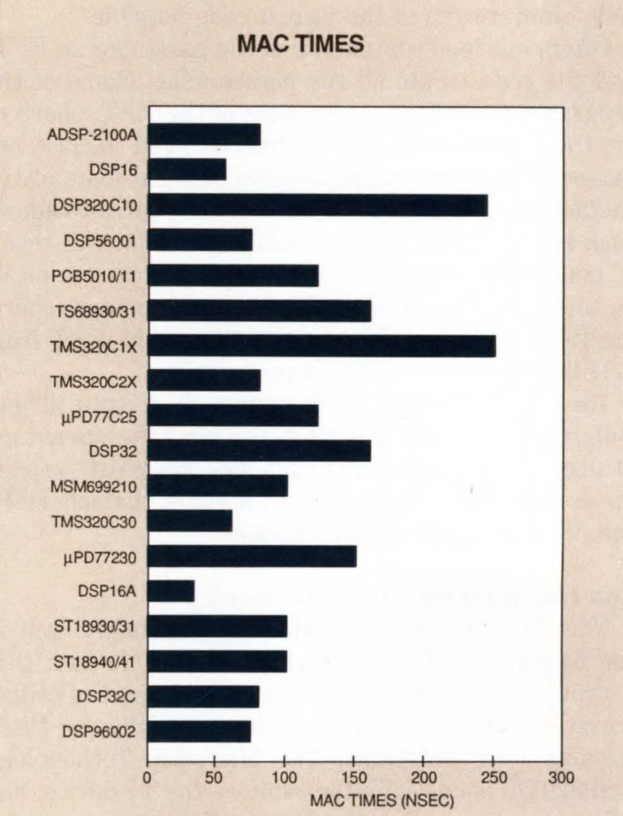


*Fig 1—**The multiply-accumulate (MAC) times** for the DSPs match the execution times for the filters. Filters, after all, are largely a series of MACs.*

Software can improve the results

The programmers who wrote the code for these benchmark tests naturally tried to shrink execution time whenever possible, particularly in the FFT applications. Some used straight-line code. The TMS320C2X, for example, uses 23,636 words of memory for the 1024-point FFT benchmark. Although this memory size is somewhat impractical, straight-line

> The benchmarks are not intended to overtax the capabilities of the DSPs. Rather, they are designed to reflect your everyday needs.

code often results in the fastest code possible.

Often, one loop contains all of the passes for an FFT, and the code treats all the passes alike. Some of the programmers split up the passes of the FFT, shortening the execution time of the first two and the last two passes. This short cut is possible because some of the coefficients are known to be 0 or 1. You can remove such trivial MACs because you know what the result of multiplying anything by 1 or 0 is before you do it. In the case of the DSP96002, the programmers shortened the execution time of the 1024-point FFT from 2.31 to 1.55 msec—a 33% improvement.

We didn't consider such coding short cuts illegal. But remember that not all DSPs can take advantage of all of the programming techniques that exist to speed up an algorithm. So you can't assume that all DSPs can achieve similar speed increases.

You can program purely for speed

The TI TMS320C1X performed amazingly well in the 64-point FFT—it performed so well, in fact, that it provides the perfect example of the impact of coding variations on benchmark results, especially for DSPs running FFT programs. The Microchip Techonology DSP320310 is basically the same as the TI device, and it has the same cycle time; but a different programmer at a different company programmed it. As a result, the performances of the two chips differ quite a bit: The TMS320C1X executes the 64-point FFT in 0.46 msec; the DSP320C10 takes 1.58 msec. Thus, the TI program is more than three times faster than the one from Microchip Technology. On the other hand, a quick check of the total memory required reveals that the TI program needs 3816 words, more than 16 times as many as the Microchip version, which needs only 233.

TI uses all of the tricks in the book to increase the speed of the 64-point FFT benchmark: straight-line code, four different types of butterflies to take advantage of trivial MACs, a lookup table for bit-reversal, and more. The resultant code is very fast, but it might not be useful in many real-world applications. This limitation does not mean that you should dismiss the results at first glance, but you should consider how well the programming techniques fit your application, and not embrace it on the basis of its speed alone.

With more than 20 general-purpose DSPs to choose from, you have, in some ways, a more difficult task than ever when you need to evaluate some DSPs for a new design. In the past, word size and format affected the speed of the device and therefore limited your choices, but the days of having to sacrifice performance if you choose to use a floating-point DSP are over. You still have to sacrifice the cost of the system because the fast floating-point devices are still rather expensive. Of course, the prices for all DSPs should go down in the next few years, so price per se will become less of an issue.

In any event, you should weigh these benchmarks and profiles carefully, evaluating them in the light of your needs, and comparing the DSPs to each other on various aspects of their performances. Speed isn't everything. If you are predominately using the DSP for filter applications, the speed at which a DSP can execute an FFT is probably irrelevant. Those of you looking for simple answers may well be disappointed. We don't have any, for in trying to find the optimum DSP IC, the bottom line just doesn't tell the whole story. In fact, it leaves a lot of important pieces out. In the end, there really are no winners in our DSP survey—only, we hope, a DSP evaluation process made more enlightened by our efforts. EDN

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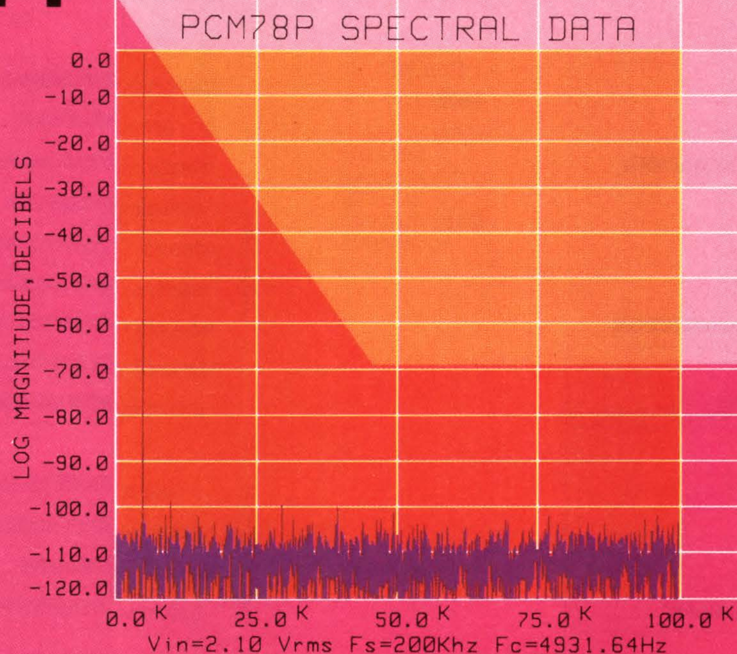

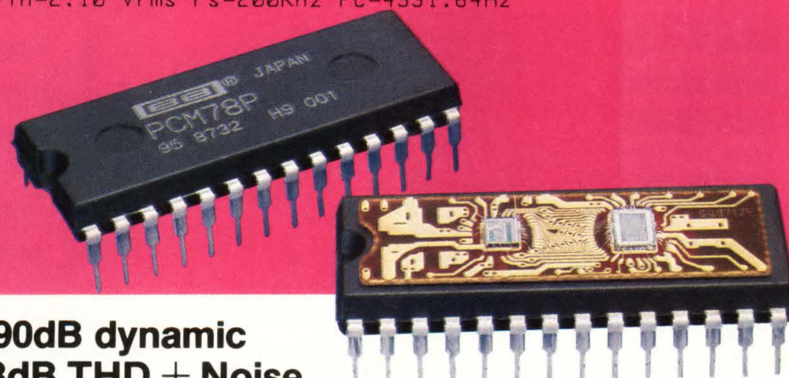

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PCM78P is almost a "drop-in" part; no external trimpots or reference needed, easy interfacing via the serial port and on-board latch. And its fast 4μs conversion time allows oversampling, reducing the complexity of antialiasing filters.

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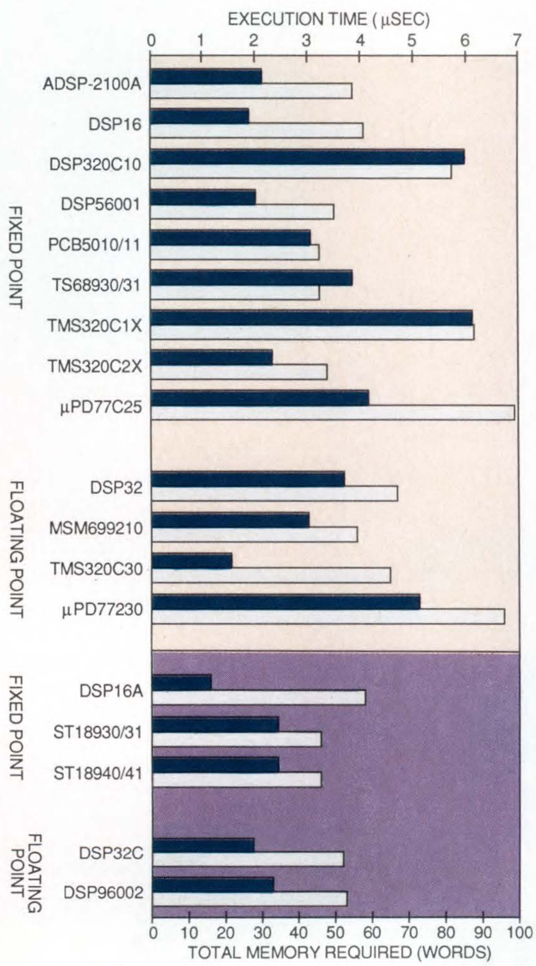
Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734

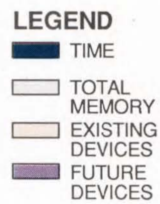
BURR-BROWN®

*U.S. unit prices, in 1000s.

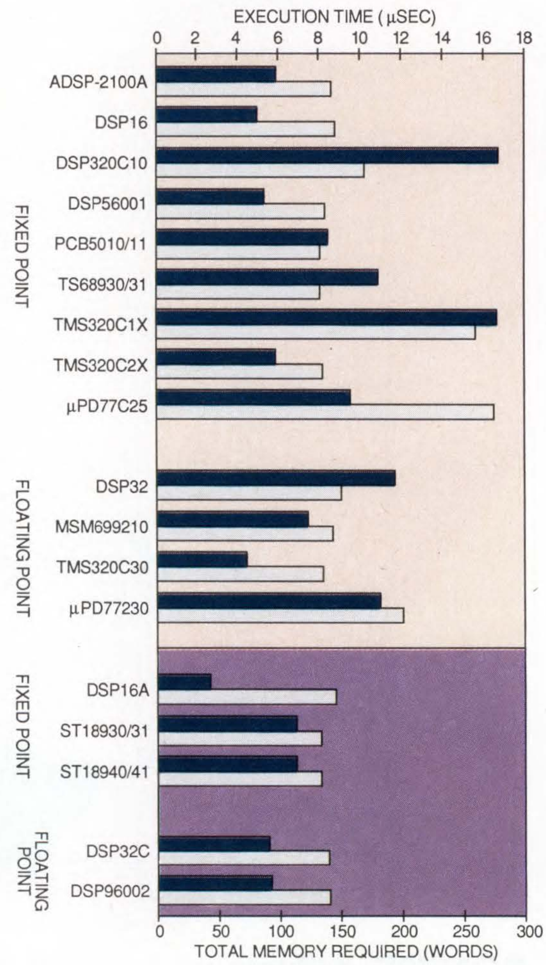
CIRCLE NO 69

BENCHMARK 1
20-TAP FIR FILTER





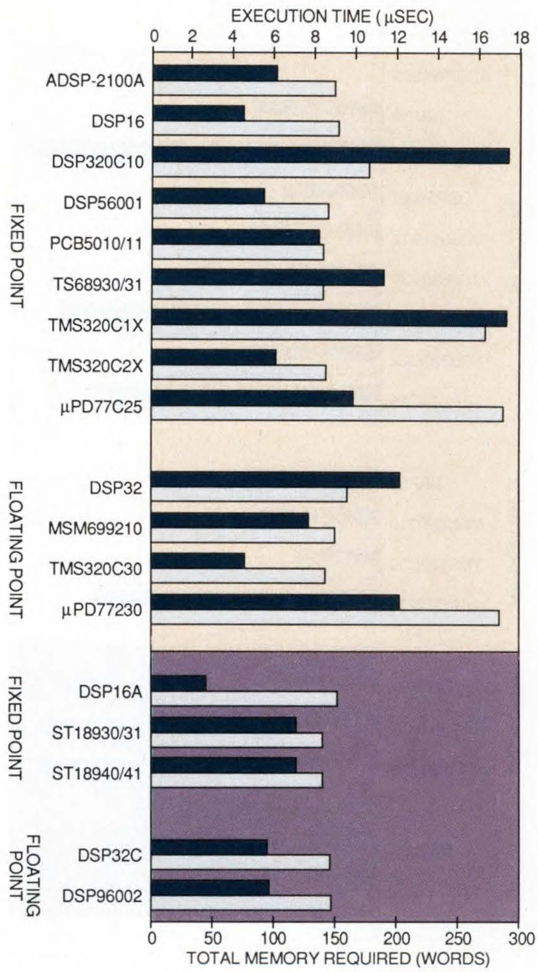
BENCHMARK 2
64-TAP FIR FILTER

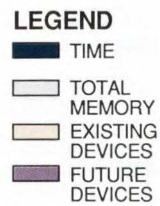


This benchmark is a Finite Impulse Response (FIR) filter routine that takes data from an external parallel port, filters the sample, and then sends the result to a different external parallel port. This is a 20-tap filter. The data will enter the DSP via an external parallel port and leave via a different external parallel port. An external parallel port is defined as a parallel port that is not located on the DSP chip. Assume that the external data converters are 16 bits and are able to convert faster than your DSP can complete the filter. No polling of the ADC is necessary; it will have the next sample when you need it. The filter characteristics are not important.

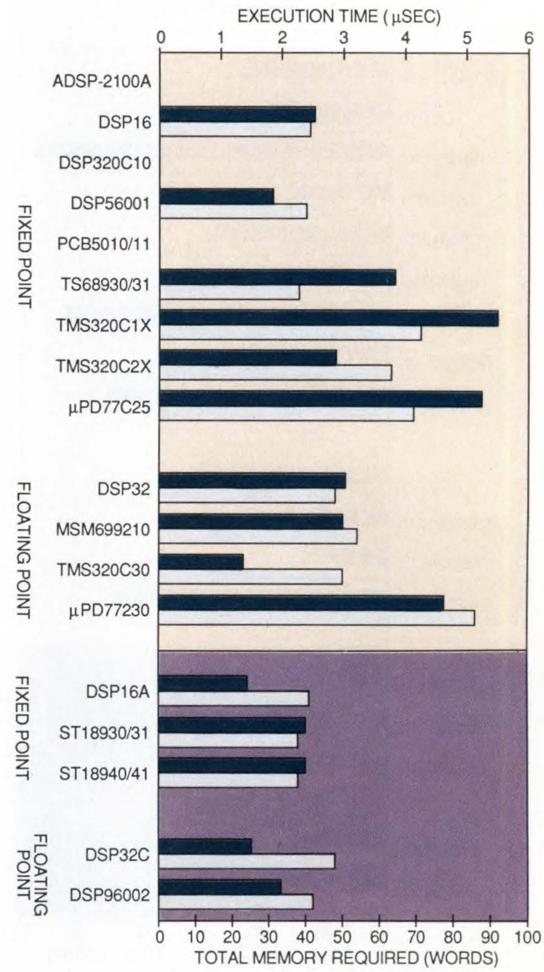
This benchmark is a Finite Impulse Response (FIR) filter routine that takes data from an external parallel port, filters the sample, and then sends the result to a different external parallel port. This is a 64-tap filter. The data will enter the DSP via an external parallel port and leave via a different external parallel port. An external parallel port is defined as a parallel port that is not located on the DSP chip. Assume that the external data converters are 16 bits and are able to convert faster than your DSP can complete the filter. No polling of the ADC is necessary; it will have the next sample when you need it. The filter characteristics are not important.

BENCHMARK 3
67-TAP FIR FILTER





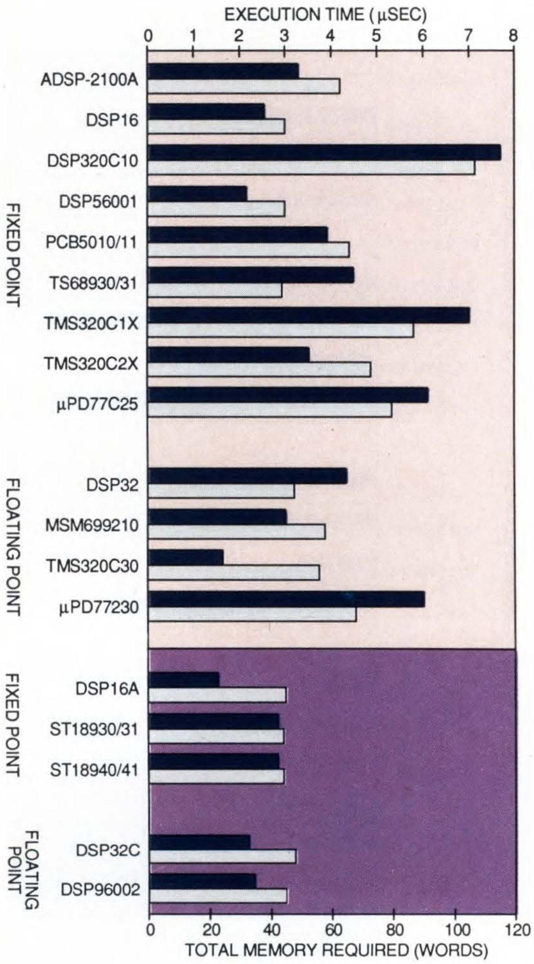
BENCHMARK 4
8-POLE CANONIC IIR FILTER (4X) (DIRECT FORM II)

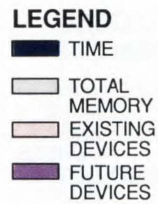


This benchmark is a Finite Impulse Response (FIR) filter routine that takes data from an external parallel port, filters the sample, and then sends the result to a different external parallel port. This is a 67-tap filter. The data will enter the DSP via an external parallel port and leave via a different external parallel port. An external parallel port is defined as a parallel port that is not located on the DSP chip. Assume that the external data converters are 16 bits and are able to convert faster than your DSP can complete the filter. No polling of the ADC is necessary; it will have the next sample when you need it. The filter characteristics are not important.

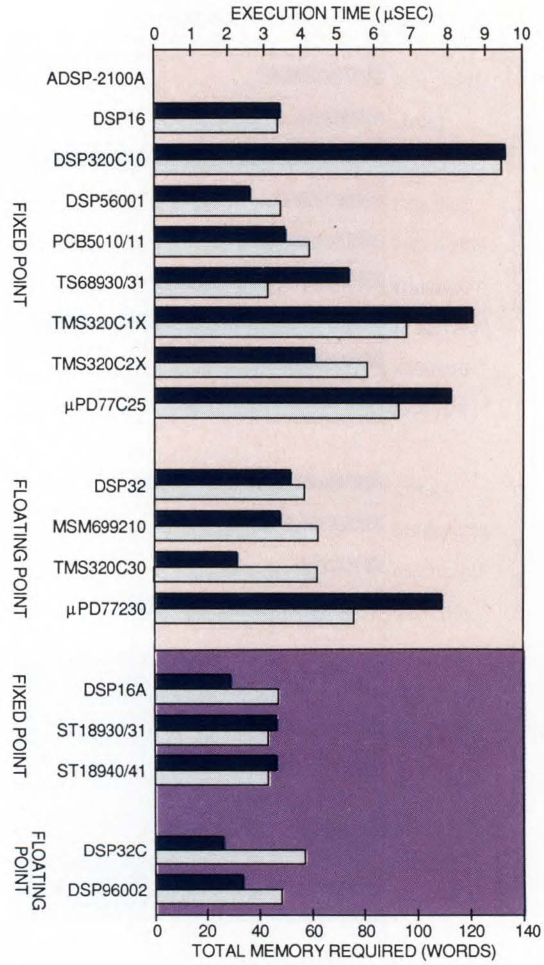
This benchmark is an Infinite Impulse Response (IIR) filter routine that takes data from an external parallel port, filters the sample, and then sends the result to a different external parallel port. This is an 8-pole filter made by cascading 2-pole canonic biquad sections using the 4-multiply technique. The data will enter the DSP via an external parallel port and leave via a different external parallel port. An external parallel port is defined as a parallel port that is not located on the DSP chip. Assume that the external data converters are 16 bits and are able to convert faster than your DSP can complete the filter. No polling of the ADC is necessary; it will have the next sample when you need it. The filter characteristics are not important.

BENCHMARK 5
8-POLE CANONIC IIR FILTER (5X)
(DIRECT FORM II)





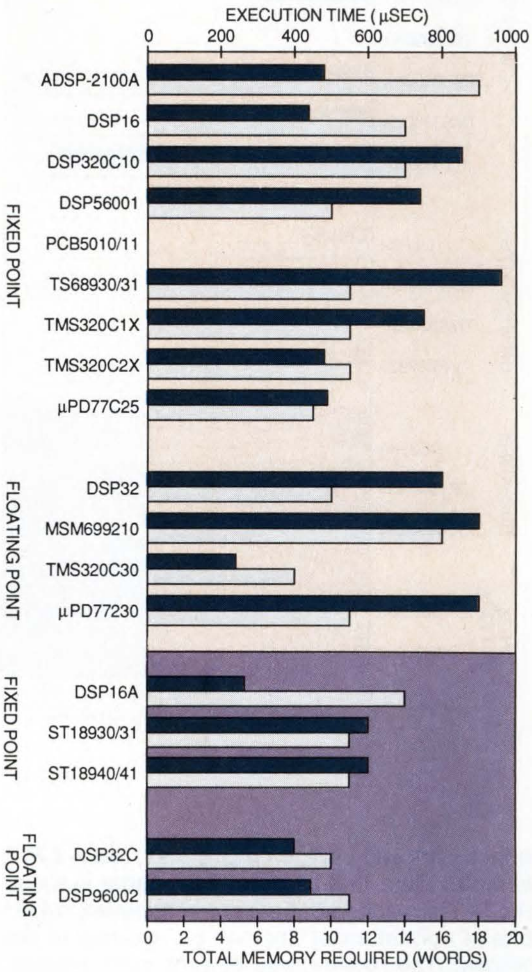
BENCHMARK 6
8-POLE TRANSPOSE IIR FILTER
(DIRECT FORM I)

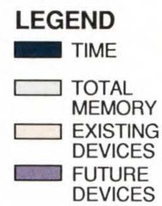


This benchmark is an Infinite Impulse Response (IIR) filter routine that takes data from an external parallel port, filters the sample, and then sends the result to a different external parallel port. This is an 8-pole filter made by cascading 2-pole canonic biquad sections using the 5-multiply technique. The data will enter the DSP via an external parallel port and leave via a different external parallel port. An external parallel port is defined as a parallel port that is not located on the DSP chip. Assume that the external data converters are 16 bits and are able to convert faster than your DSP can complete the filter. No polling of the ADC is necessary; it will have the next sample when you need it. The filter characteristics are not important.

This benchmark is an Infinite Impulse Response (IIR) filter routine that takes data from an external parallel port, filters the sample, and then sends the result to a different external parallel port. This is an 8-pole filter made by cascading 2-pole transpose biquad sections. The data will enter the DSP via an external parallel port and leave via a different external parallel port. An external parallel port is defined as a parallel port that is not located on the DSP chip. Assume that the external data converters are 16-bits and are able to convert faster than your DSP can complete the filter. No polling of the ADC is necessary; it will have the next sample when you need it. The filter characteristics are not important.

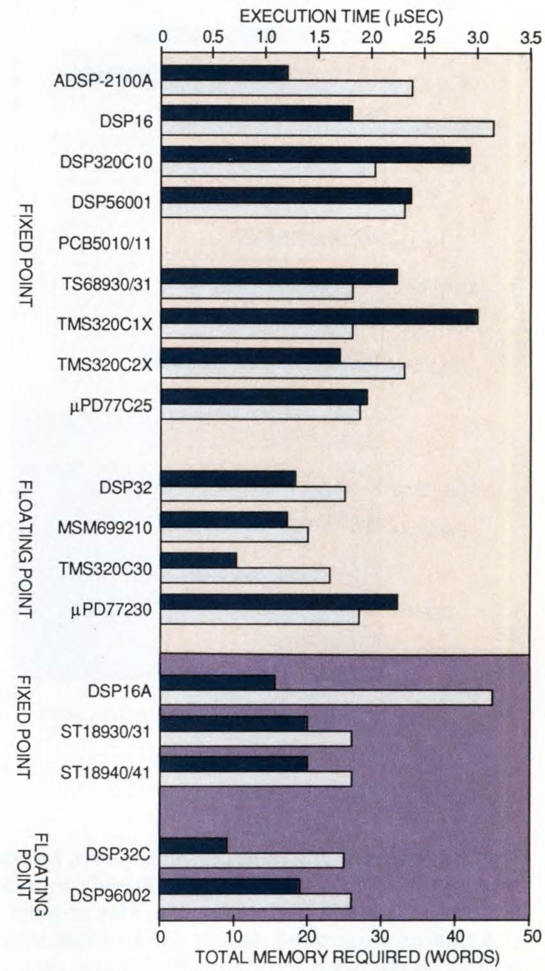
BENCHMARK 7
DOT PRODUCT





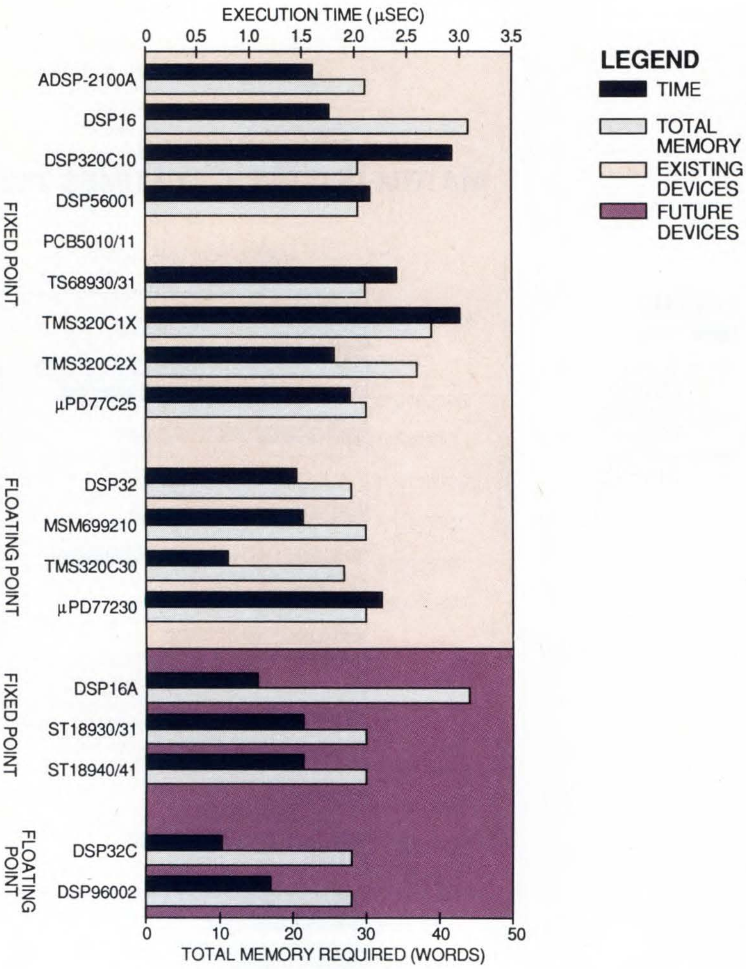
This benchmark will perform a dot product of two vectors and give a scaler result. Each vector will be represented by two points in 2-D (x,y). The original vectors will already be in memory and the result will go to memory. The vectors can be destroyed during the calculation.

BENCHMARK 8
MATRIX MULTIPLY, 2X2 TIMES 2X2

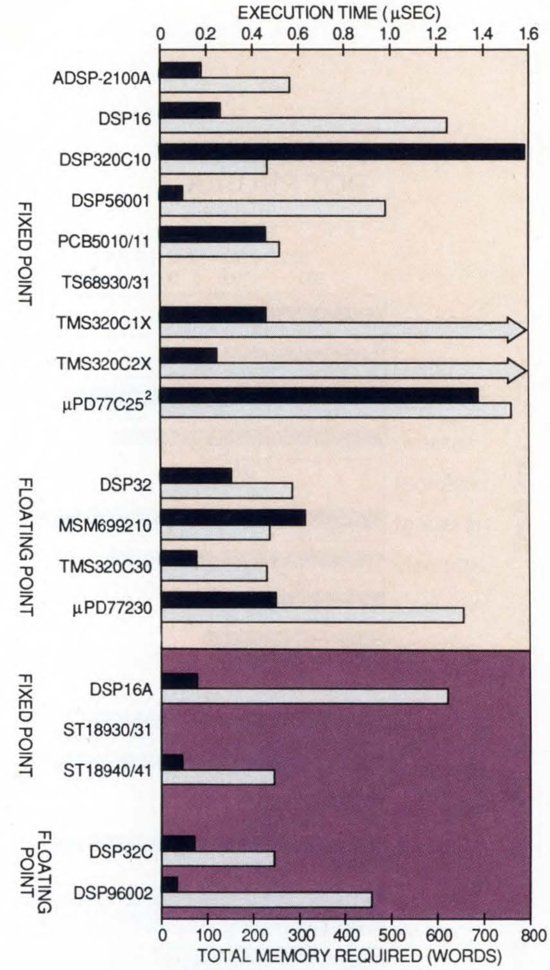


This benchmark will multiply one matrix by another. Assume that both matrices are already in memory and the result will go to memory. The original matrices can be destroyed during the multiplication. The routine performs a matrix multiplication on a 2×2 matrix multiplied by a 2×2 matrix.

BENCHMARK 9
MATRIX MULTIPLY, 3X3 TIMES 3X1



BENCHMARK 10
COMPLEX 64-POINT FFT (RADIX-2)



This benchmark will multiply one matrix by another. Assume that both matrices are already in memory and the result will go to memory. The original matrices can be destroyed during the multiplication. The routine performs a matrix multiplication on a 3 × 3 matrix multiplied by a 3 × 1 matrix.

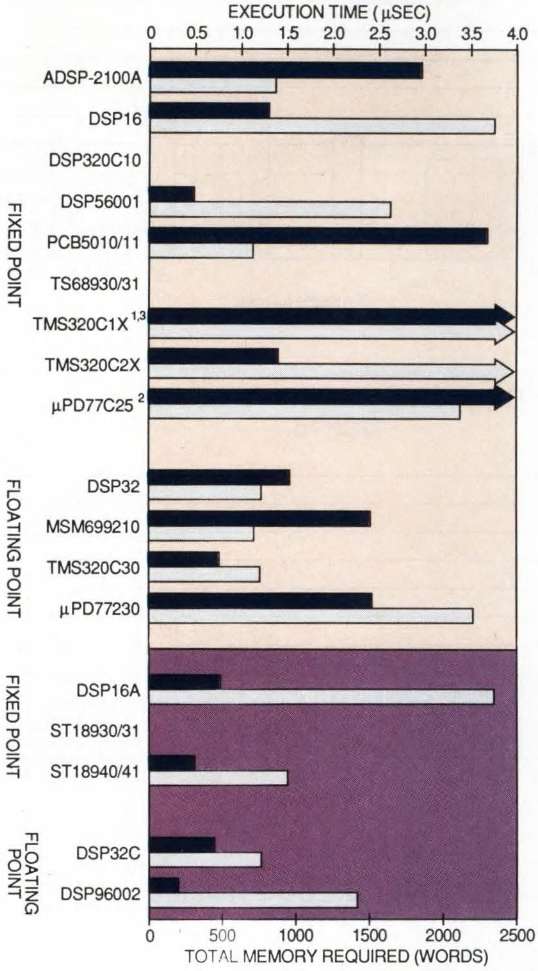
This benchmark will perform a complex, radix-2 FFT with complex data that is already available in memory. The FFT's results will be a set of complex values with bits in normal order (include bit reversal in the benchmark). The routine may destroy your original data during the processing tasks. The size of this FFT is 64-point. Precalculation of coefficients and lookup tables are allowed but their size must be included in the memory size. For example, if you use a lookup-table algorithm for bit-reversal, the number of words occupied by the lookup table must be included in the memory size you report.

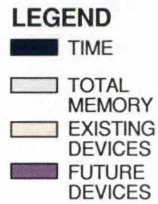
1. These DSPs need external address counters in order to access the external memory required to perform this benchmark.

2. This DSP needs an external DMA controller in order to access the external memory required to perform this benchmark.

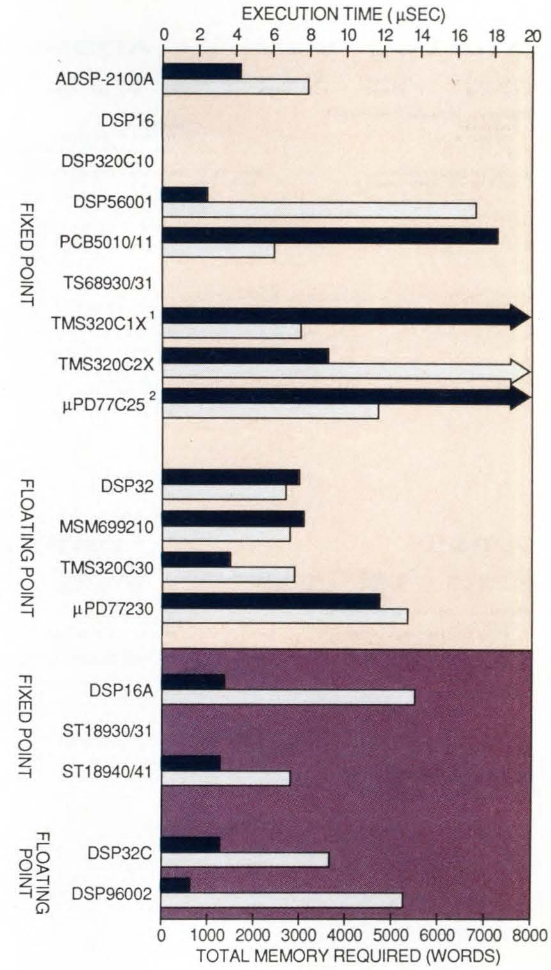
3. The TMS320C15-25 was used for this benchmark.

BENCHMARK 11
COMPLEX 256-POINT FFT
(RADIX-2)





BENCHMARK 12
COMPLEX 1024-POINT FFT
(RADIX-2)



This benchmark will perform a complex, radix-2 FFT with complex data that is already available in memory. The FFT's results will be a set of complex values with bits in normal order (include bit reversal in the benchmark). The routine may destroy your original data during the processing tasks. The size of this FFT is 256-point. Precalculation of coefficients and lookup tables are allowed but their size must be included in the memory size. For example, if you use a lookup-table algorithm for bit-reversal, the number of words occupied by the lookup table must be included in the memory size you report.

This benchmark will perform a complex, radix-2 FFT with complex data that is already available in memory. The FFT's results will be a set of complex values with bits in normal order (include bit reversal in the benchmark). The routine may destroy your original data during the processing tasks. The size of this FFT is 1024 points. Precalculation of coefficients and lookup tables are allowed but their size must be included in the memory size. For example, if you use a lookup-table algorithm for bit-reversal, the number of words occupied by the lookup table must be included in the memory size you report.

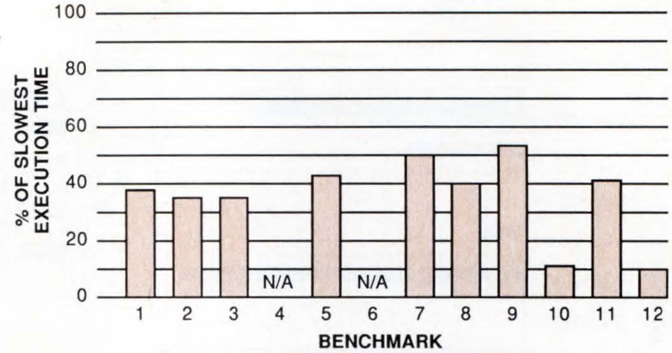
Analog Dev ADSP-2100A

Word Size: 16 bits | Format: Fixed | Accumulator Size: 40 bits | Cycle Time: 80, 100 nsec | MAC Time: 80, 100 nsec

Memory: internal/external
Program: 0/16k X 24
Data: 0/16k X 16 and 16k X 16/24 in program space

Cost (single/100s): $411/$164 (80 nsec)
Date of first working silicon: Nov, 1987

RELATIVE SPEED PROFILE ADSP-2100A



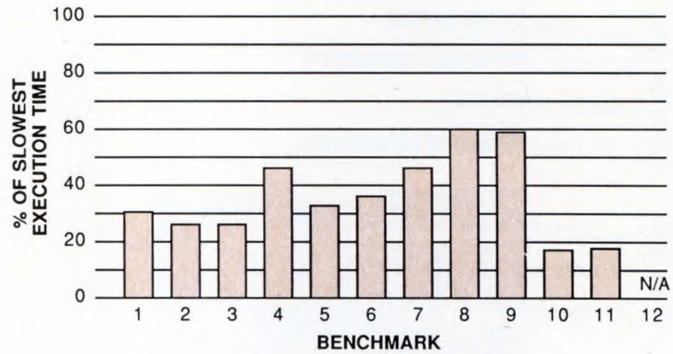
AT&T DSP16-55

Word Size: 16 bits | Format: Fixed | Accumulator Size: 36 bits | Cycle Time: 55, 75 nsec | MAC Time: 55, 75 nsec

Memory: internal/external
Program: 2k X 16 ROM/64k X 16
Data: 512 X 16 RAM/64k X 16

Cost (single/100s): $84/$68 (55 nsec)
Date of first working silicon: Oct, 1986

RELATIVE SPEED PROFILE DSP16



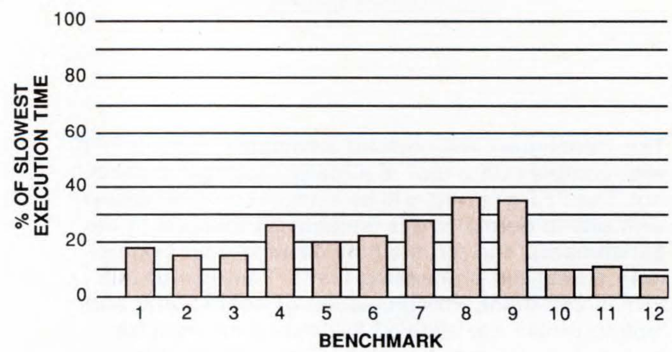
AT&T DSP16A-33

Word Size: 16 bits | Format: Fixed | Accumulator Size: 36 bits | Cycle Time: 33, 55, 75 nsec | MAC Time: 33, 55, 75 nsec

Memory: internal/external
Program: 4k X 16 ROM/64k X 16
Data: 2k X 16 RAM/64k X 16

Cost (single/100s): NA
Date of first working silicon: Estimated Oct, 1988

RELATIVE SPEED PROFILE DSP16A



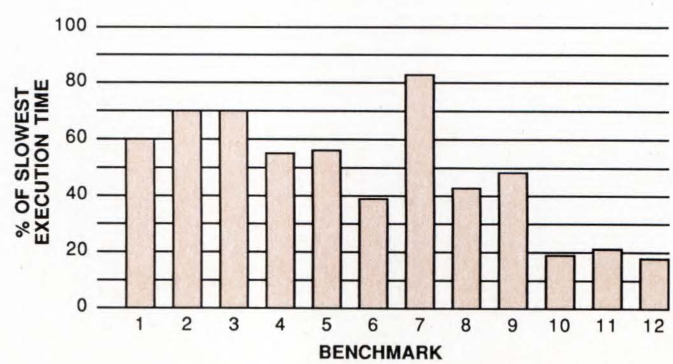
AT&T DSP32-160

Word Size: 32 bits | Format: Floating | Accumulator Size: 40 bits | Cycle Time: 160, 250 nsec | MAC Time: 160, 250 nsec

Memory: internal/external
(Memory is contiguous, can be program or data)
512 X 32 ROM, 1k X 32 RAM/14k X 32

Cost (single/100s): $190/$170 (160 nsec)
Date of first working silicon: Dec, 1984

RELATIVE SPEED PROFILE DSP32



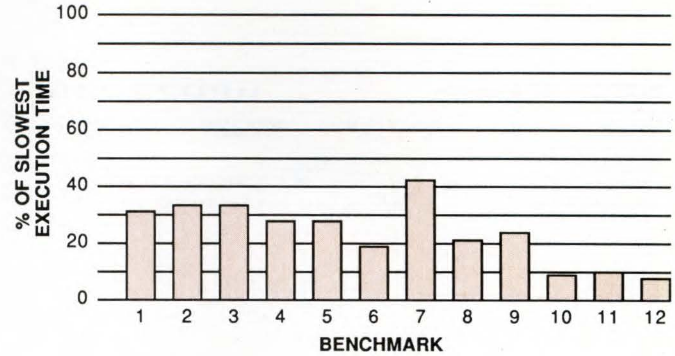
AT&T DSP32C-80

Word Size: 32 bits
Format: Floating
Accumulator Size: 40 bits
Cycle Time: 80, 100 nsec
MAC Time: 80, 100 nsec

Memory: internal/external
(Memory is contiguous, can be program or data)
(512 + 512 + 512) X 32 RAM/4M X 32
or (512 + 512) X 32 RAM, 2k X 32 ROM/4M X 32

Cost (single/100s): NA
Date of first working silicon: Estimated Sept, 1988

RELATIVE SPEED PROFILE
DSP32C



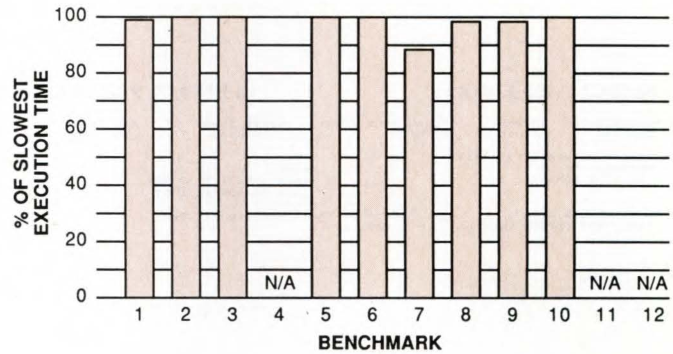
Microchip Tech DSP320C10

Word Size: 16 bits
Format: Fixed
Accumulator Size: 32 bits
Cycle Time: 122, 160, 200 nsec
MAC Time: 244, 320, 400 nsec

Memory: internal/external
Program: 1.5k X 16 ROM/4k X 16
Data: 144 X 16 RAM/0

Cost (single/100s): $48.10/$41.80 (122 nsec)
Date of first working silicon: Sep, 1985

RELATIVE SPEED PROFILE
DSP320C10



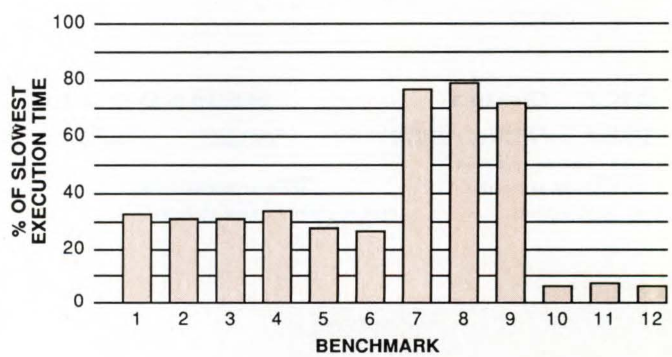
Motorola DSP56001

Word Size: 24 bits
Format: Fixed
Accumulator Size: 56 bits
Cycle Time: 74, 98 nsec
MAC Time: 74, 98 nsec

Memory: internal/external
Program:
3.75k X 24 ROM/64k X 24
or 512 X 24 RAM/64k X 24
Data:
(256 + 256) X 24 RAM,
(256 + 256) X 24 ROM/(64k + 64k) X 24

Cost (single/100s): $75/$75 (74 nsec)
Date of first working silicon: Nov, 1987

RELATIVE SPEED PROFILE
DSP56000/1



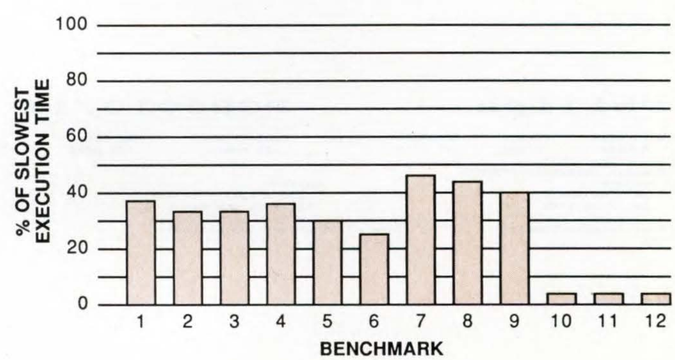
Motorola DSP96002

Word Size: 32 bits
Format: Floating
Accumulator Size: 96 bits
Cycle Time: 74 nsec
MAC Time: 74 nsec

Memory: internal/external
Program:
512 X 32 RAM/4G X 32
Data:
(512 + 512) X 32 RAM,
(512 + 512) X 32 ROM/(4G + 4G) X 32

Cost (single/100s): NA
Date of first working silicon: Estimated 1st quarter 1989

RELATIVE SPEED PROFILE
DSP96001/2



RELATIVE SPEED PROFILE
μPD77C25

NEC Elec — uPD77C25

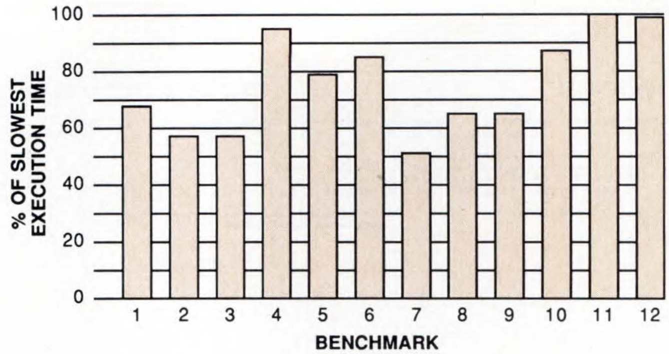
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
16 bits	Fixed	Dual 16 bits	122 nsec	122 nsec

Memory: internal/external
Program:
2k X 24 ROM/0

Data:
1k X 16 ROM, 256 X 16 RAM/0

Cost (single/100s):
$65/$57 (EPROM version)

Date of first working silicon:
Sep, 1987



RELATIVE SPEED PROFILE
μPD77230

NEC Elec — uPD77230

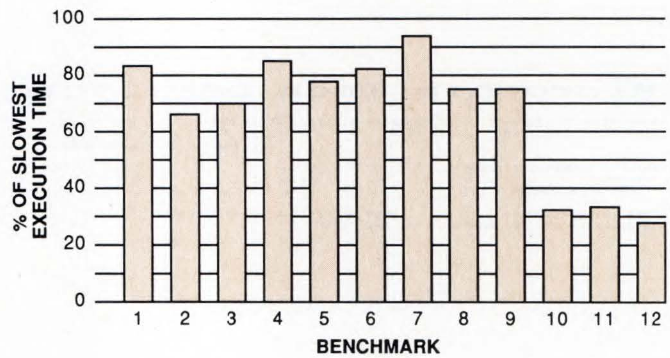
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
32 bits	Floating	55 bits	150 nsec	150 nsec

Memory: internal/external
Program:
2k X 32 ROM/8k X 32

Data:
(512 + 512) X 32 RAM,
1k X 32 ROM/8k X 32

Cost (single/100s):
$400/$350 (EPROM version)

Date of first working silicon:
May, 1986



RELATIVE SPEED PROFILE
MSM699210

OKI Semi — MSM699210

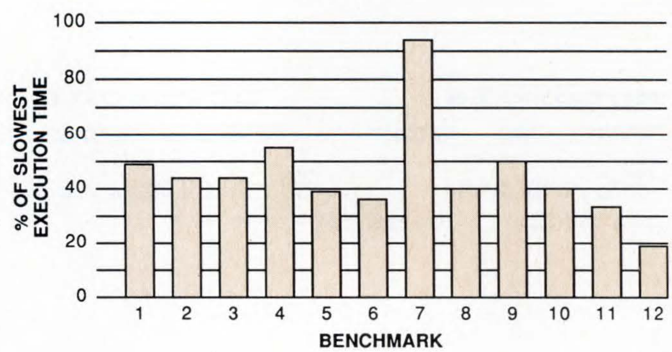
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
22 bits	Floating	22 bits	100 nsec	100 nsec

Memory: internal/external
Program:
2k X 32 ROM/64k X 32

Data:
512 X 22 RAM/64k X 22

Cost (single/100s):
$150/$85

Date of first working silicon:
June 1988



RELATIVE SPEED PROFILE
PCB5010/11

Philips — PCB5010/11

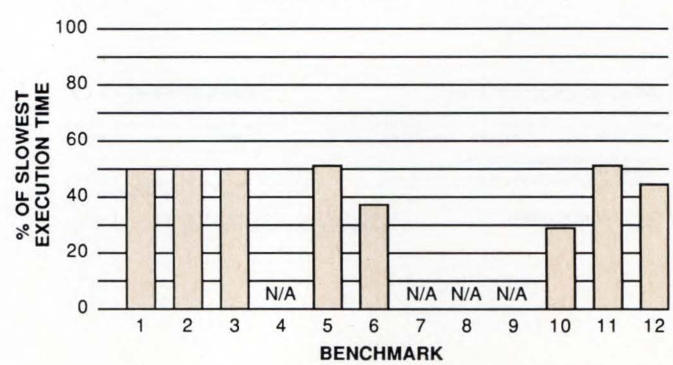
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
16 bits	Fixed	40 bits	122 nsec	122 nsec

Memory: internal/external
Program:
1k X 40 ROM/0
or 0/64k X 40

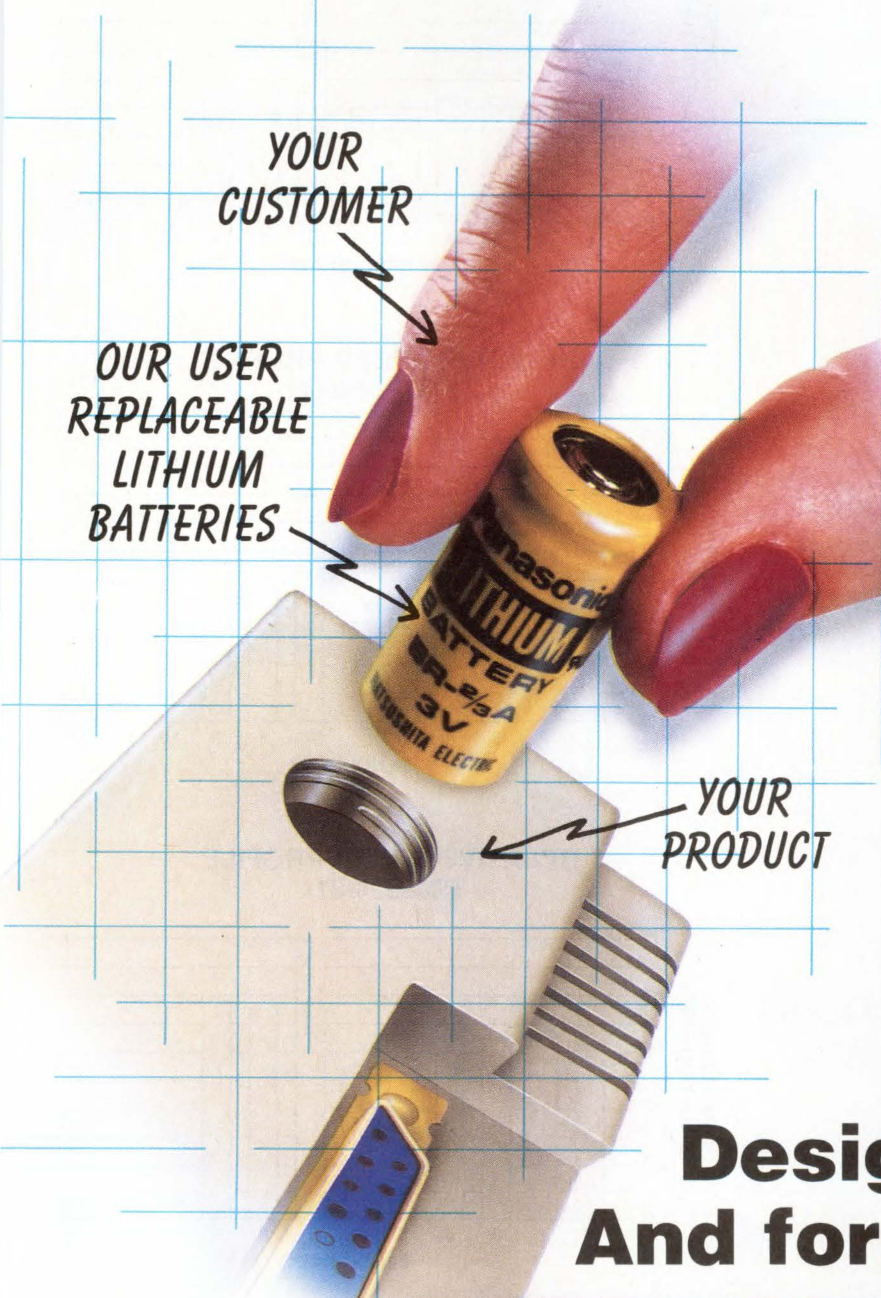
Data:
(128 + 128) X 16 RAM,
512 X 16 ROM/64k X 16

Cost (single/100s):
NA

Date of first working silicon:
1987



Introducing the friendly lithium battery.



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Design it in. And forget it.

Panasonic
Industrial Company

CIRCLE NO 70

SGS-Thomson ST18930/31

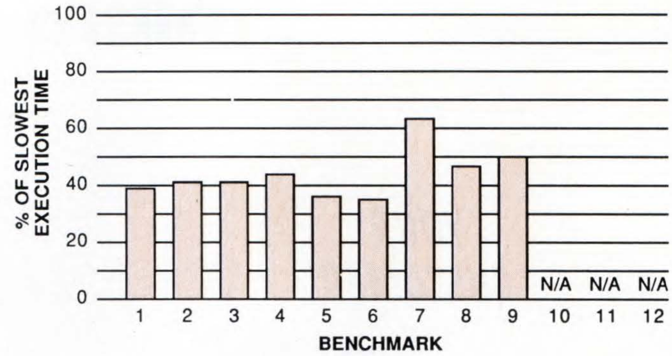
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
16 bits	Fixed	32 bits	100 nsec	100 nsec

Memory: internal/external
Program:
3k X 32 ROM/0
or 0/64k X 32

Data:
(128 + 192) X 16 RAM,
512 X 16 ROM/4k X 16

Cost (single/100s):
$125/$95

Date of first working silicon:
July 1988



RELATIVE SPEED PROFILE
ST18930/31

SGS-Thomson ST18940/41

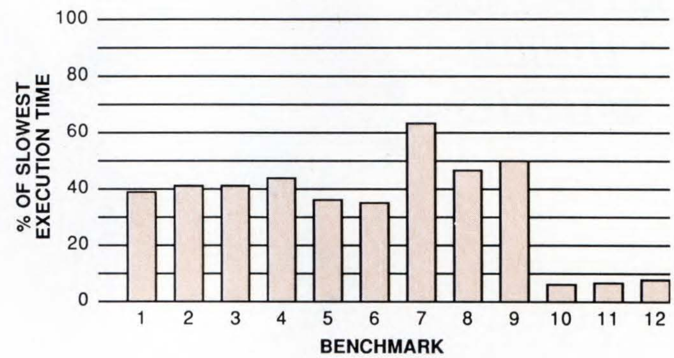
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
16 bits	Fixed	32 bits	100 nsec	100 nsec

Memory: internal/external
Program:
2k X 32 ROM/0
or 0/64k X 32

Data:
(256 + 256) X 16 RAM,
512 X 16 ROM/64k X 16

Cost (single/100s):
$125/95

Date of first working silicon:
July 1988



RELATIVE SPEED PROFILE
ST18940/41

SGS-Thomson TS68930/31

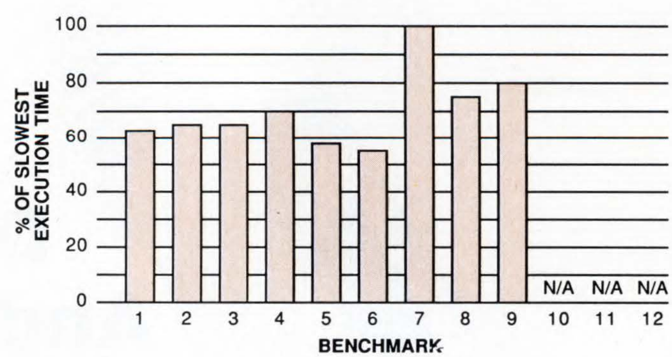
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
16 bits	Fixed	32 bits	160 nsec	160 nsec

Memory: internal/external
Program:
1.2k X 32 ROM/0
or 0/64k X 32

Data:
(128 + 128) X 16 RAM,
512 X 16 ROM/4k X 16

Cost (single/100s):
$125/$95

Date of first working silicon:
April 1986



RELATIVE SPEED PROFILE
TS68930/31

Texas Inst TMS320C1X

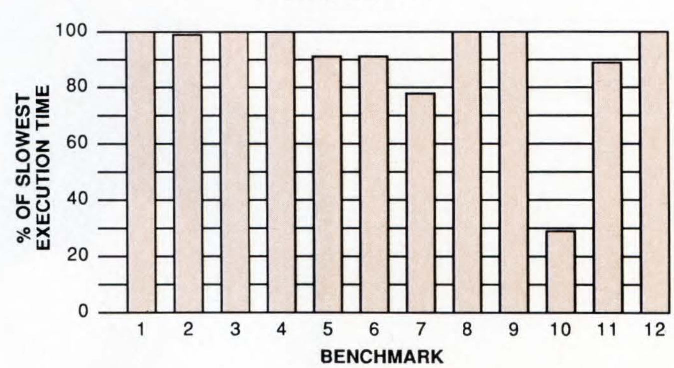
Word Size:	Format:	Accumulator Size:	Cycle Time:	MAC Time:
16 bits	Fixed	32 bits	125, 160, 200, 280 nsec	250, 320, 400, 560 nsec

Memory: internal/external
Program:
1.5k X 16 ROM/4k X 16
or 4k X 16 ROM/0
or 0/4k X 16

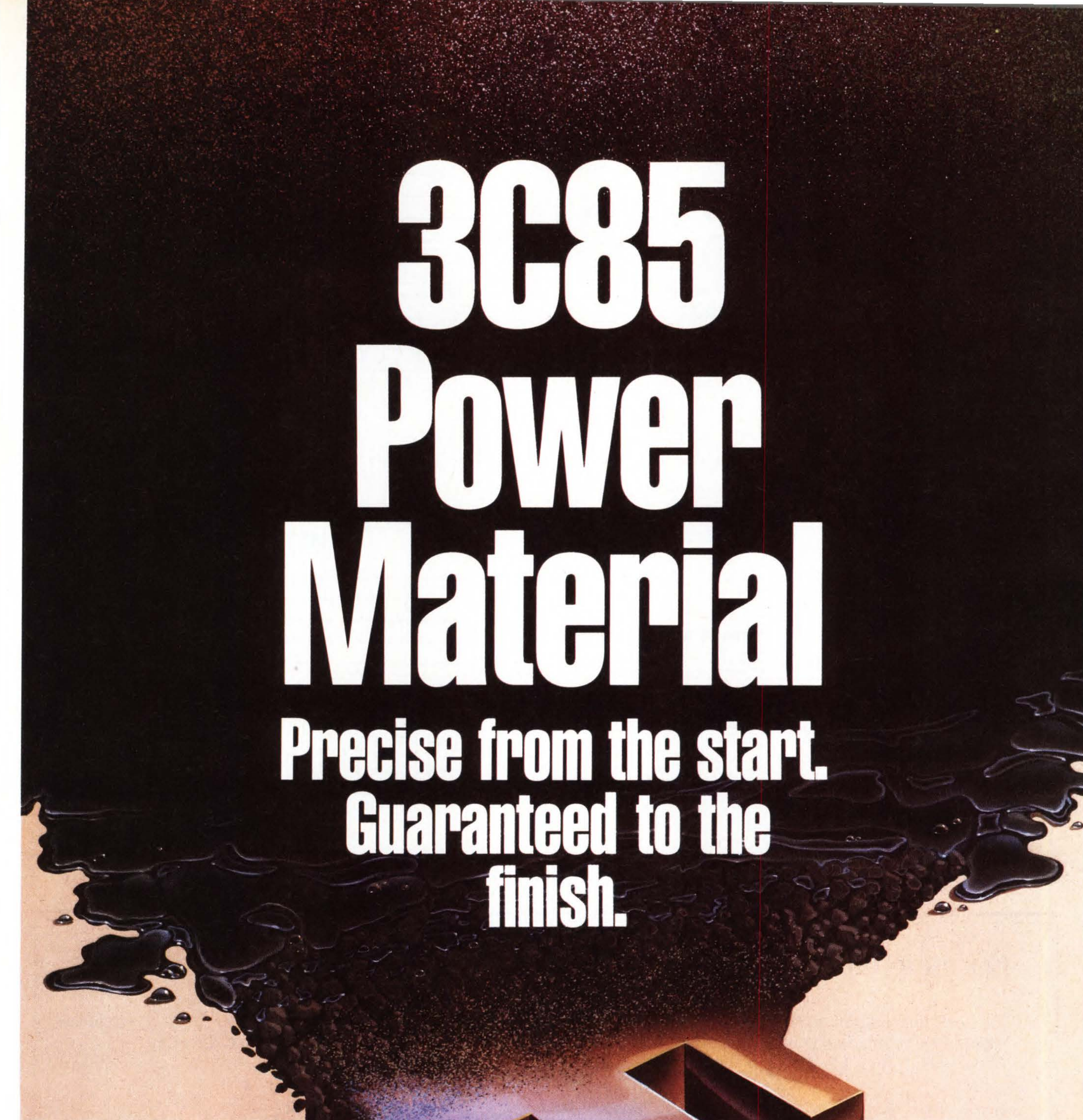
Data:
144 X 16 RAM/0
or 256 X 16 RAM/0

Cost (single/100s):
$50/30 (125 nsec)

Date of first working silicon:
1982, 1984 for CMOS versions



RELATIVE SPEED PROFILE
TMS320C1X



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CIRCLE NO 71

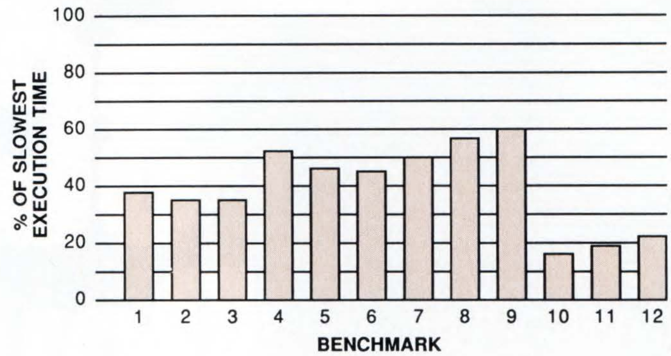
Texas Inst TMS320C2X

Word Size: 16 bits | Format: Fixed | Accumulator Size: 32 bits | Cycle Time: 80, 100, 200 nsec | MAC Time: 80, 100, 200 nsec

Memory: internal/external
Program: 4k X 16 ROM/64k X 16
Data: 544 X 16 RAM/64k X 16

Cost (single/100s): $120/75 (80 nsec)
Date of first working silicon: 1984, 1986 for CMOS versions

RELATIVE SPEED PROFILE
TMS320C2X



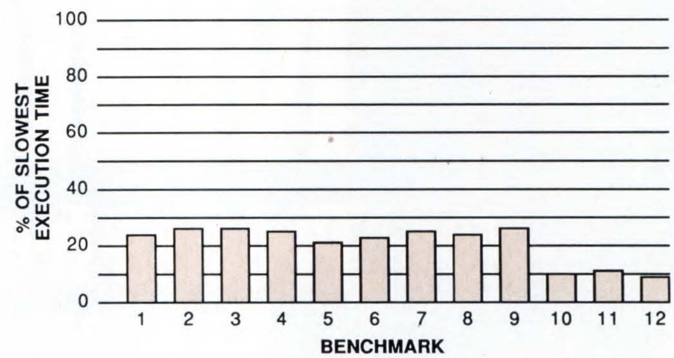
Texas Inst TMS320C30

Word Size: 32 bits | Format: Floating | Accumulator Size: 40 bits | Cycle Time: 60 nsec | MAC Time: 60 nsec

Memory: internal/external
(Memory is contiguous, can be program or data)
2k X 32 RAM, 4k X 32 ROM/16M X 32

Cost (single/100s): $1300/$1000
Date of first working silicon: June 1988

RELATIVE SPEED PROFILE
TMS320C3X



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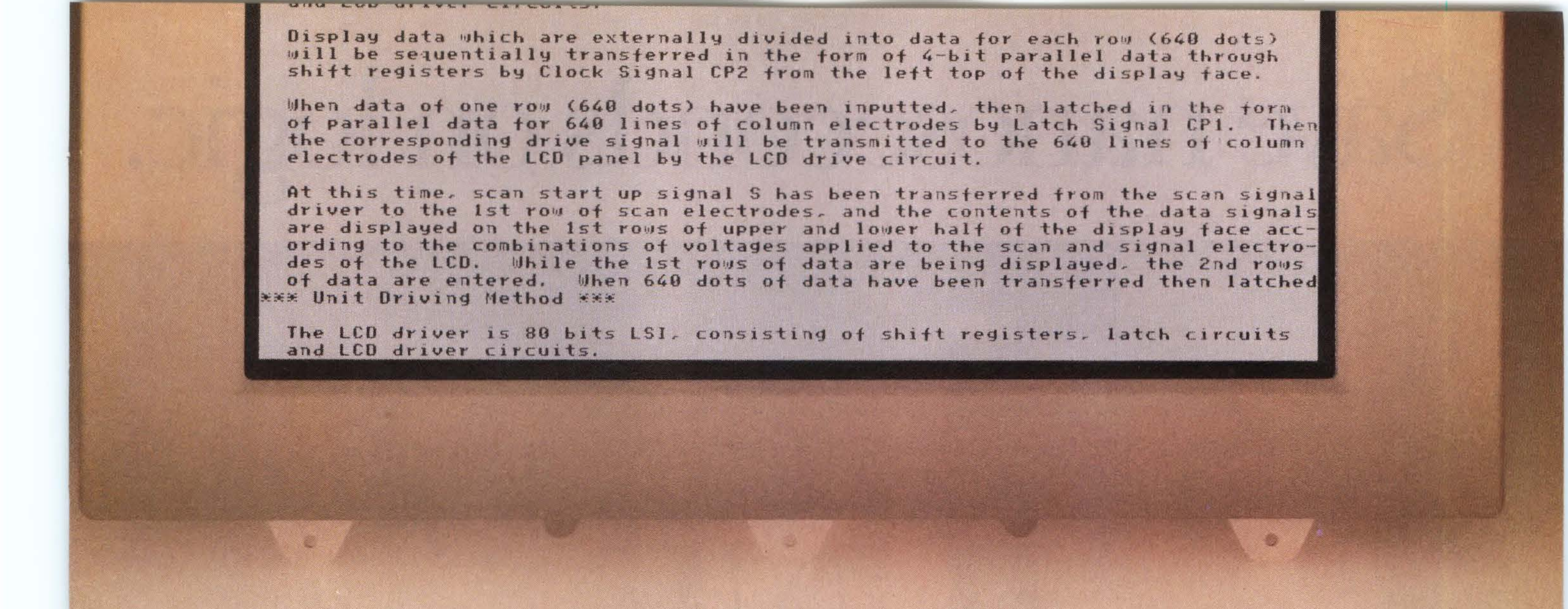

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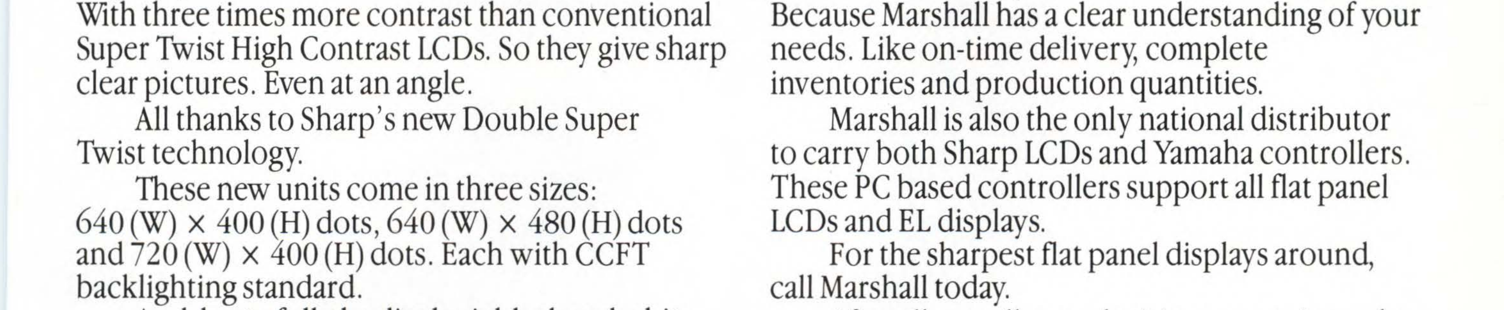

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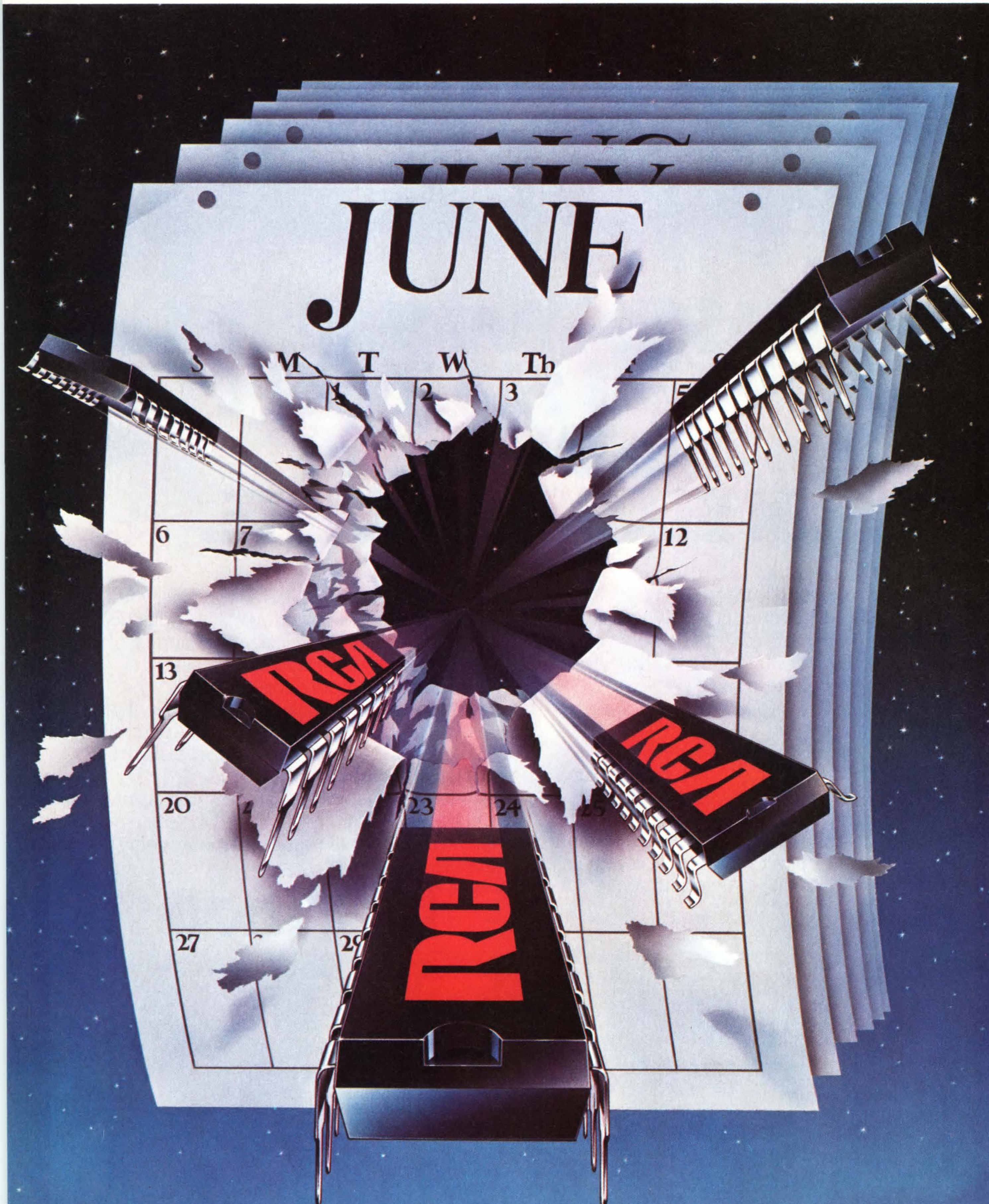

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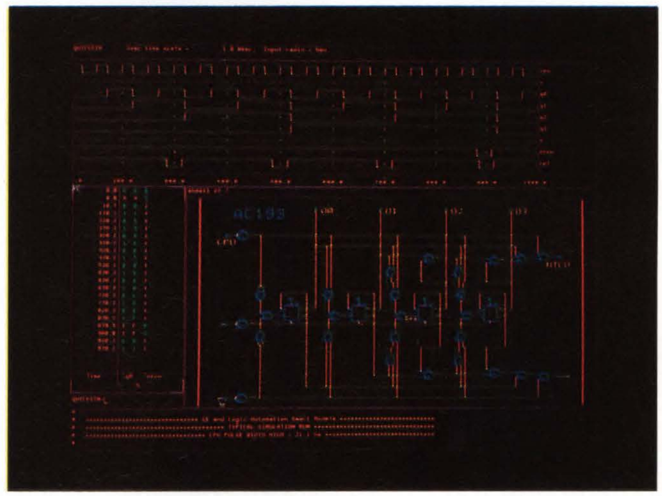

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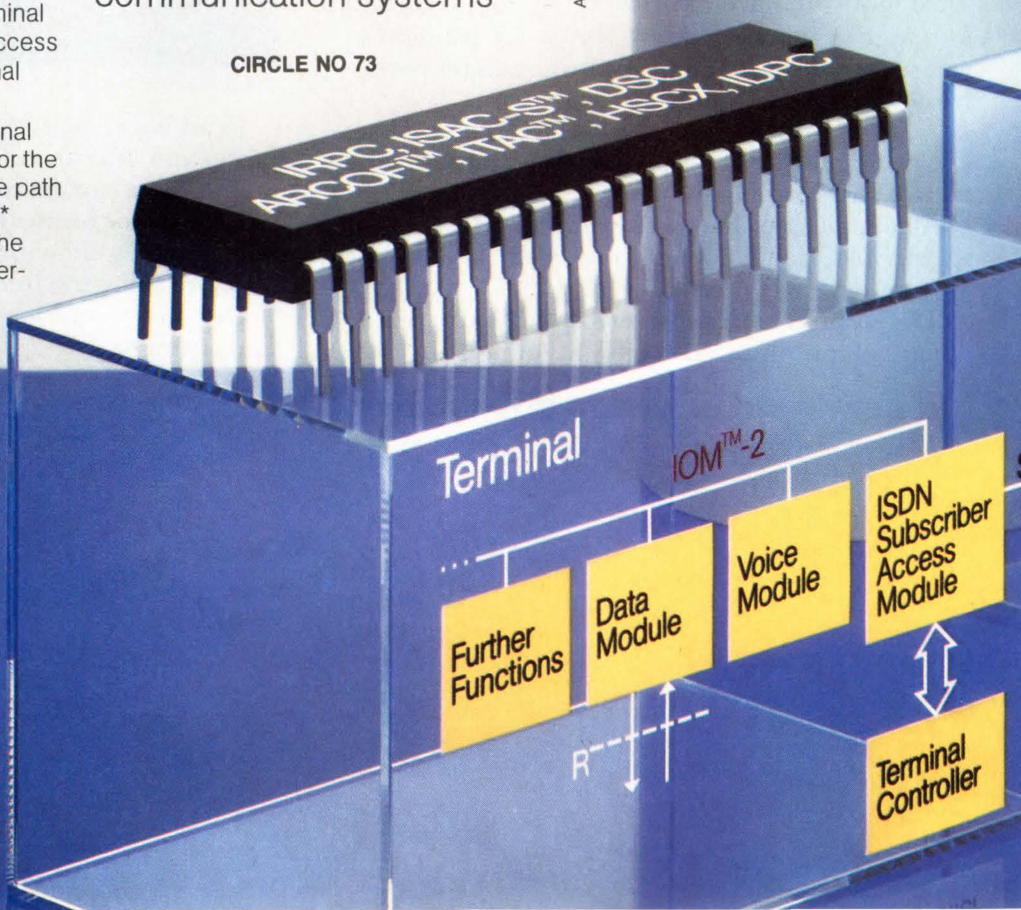

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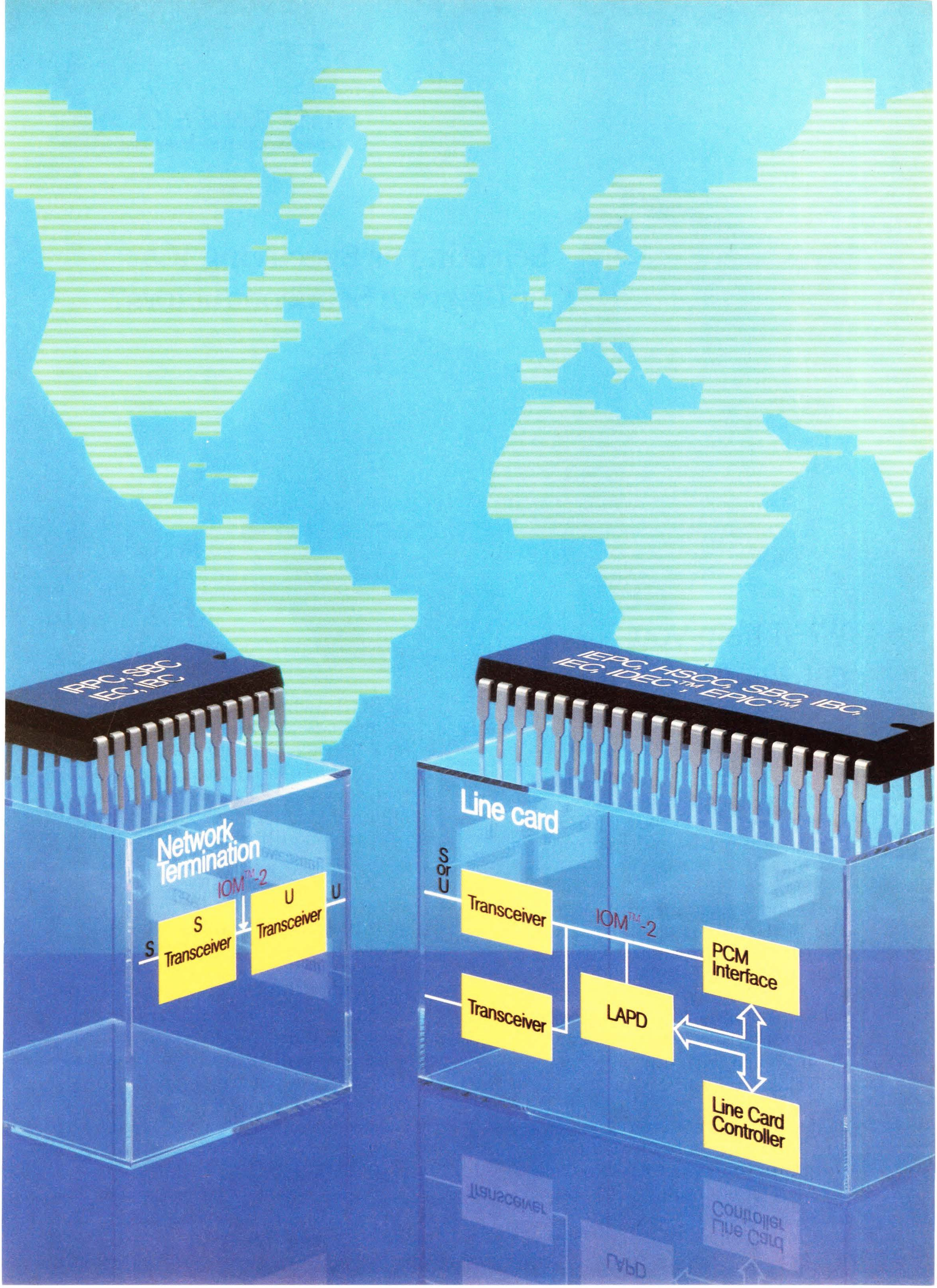
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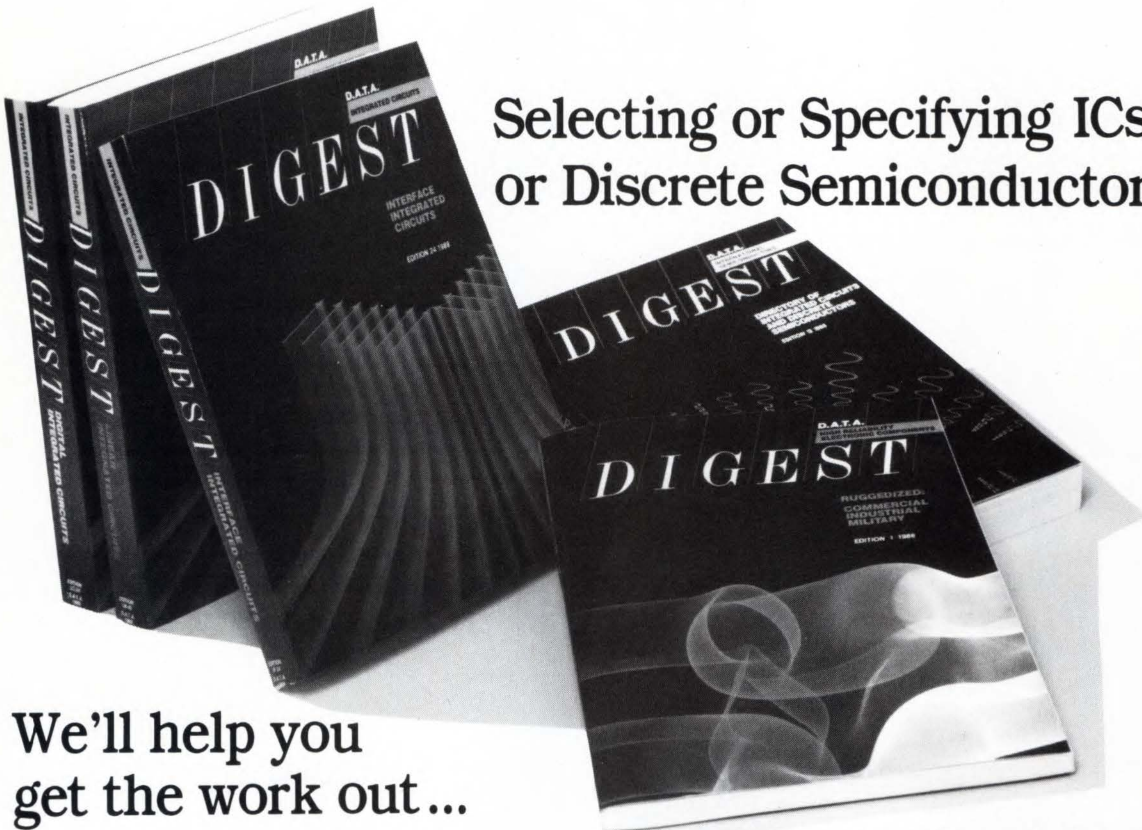

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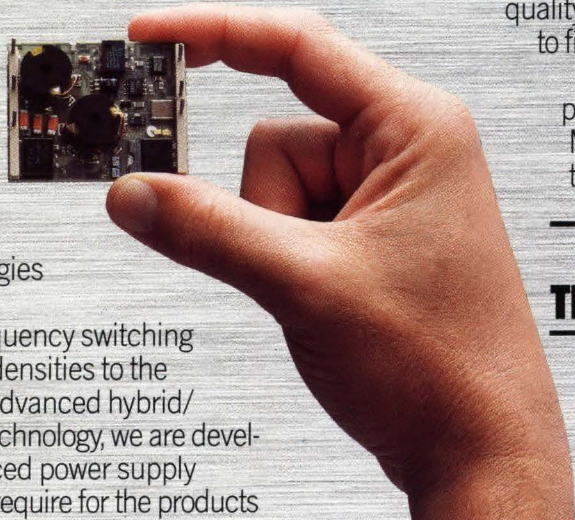

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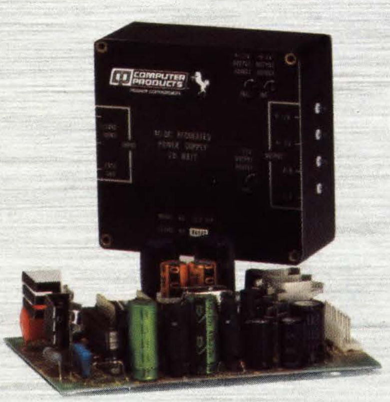

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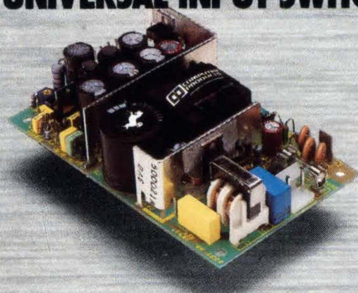

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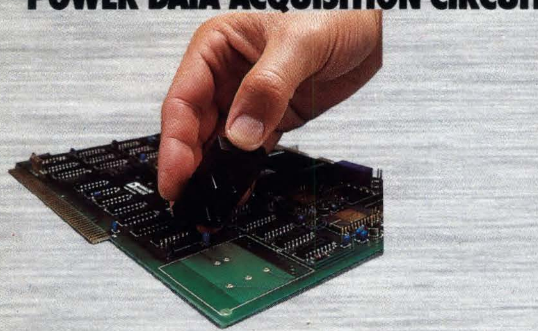

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Sliding FFT computes frequency spectra in real time

Digital-signal-processing (DSP) systems must often perform real-time spectral analysis of a nonterminating data sequence. A simple method for calculating frequency spectra—the sliding FFT—requires less computing power than the conventional FFT approach.

Tom Springer, *Pinson Associates Inc*

Many digital-signal-processing applications, such as certain types of adaptive filters, require you to perform real-time spectral analysis of a nonterminating data sequence **(Ref 1)**. The usual approach to such problems calls for computing power of a very high order, as exemplified by the latest VLSI DSP chips, which can calculate fast Fourier transforms (FFTs) at blinding speed, using standard algorithms. However, for a wide range of practical problems, a simple method for calculating frequency spectra—the sliding FFT algorithm—has a number of advantages over the conventional FFT algorithms. For instance, it can calculate spectra at a rate more closely approaching the sampling frequency than conventional algorithms can do.

You can best understand the computational difficulties that real-time spectral analysis entails if you consider the operation of a Fourier analyzer or dynamic signal analyzer. You can use such an instrument—for example, Hewlett-Packard's Model 3562A Dual Channel Dynamic Signal Analyzer **(Ref 2)**—to view and record signals as they appear in the complex frequency domain. However, there is a fundamental difference, which is not always understood, between a Fourier analyzer and a spectrum analyzer.

The spectrum analyzer displays the output of what is effectively a swept filter; it therefore presents an *average* spectral distribution over a sampling interval. Consequently, you can only use the spectrum analyzer for continuous frequency measurements. The Fourier analyzer, on the other hand, updates the spectrum at approximately the sample rate, and therefore presents the *instantaneous* spectral characteristics of the input signal. You can therefore use it to perform transient analysis; unlike the spectrum analyzer, it provides phase as well as magnitude information.

FFT computation time delays the response

Ideally, the Fourier analyzer would compute the discrete Fourier transform as quickly as the signal is sampled. In practice, however, the computational limitations of the processor make it impossible to realize this ideal, so real instruments specify both an input-signal bandwidth and a real-time bandwidth. The input-signal bandwidth is limited by the sampling rate of the instrument and represents the highest frequency that the instrument can detect without aliasing; this frequency is called the Nyquist frequency. The real-time bandwidth defines the fastest transient event that the instrument can record, and it's directly related to the length of time required to calculate the discrete

You can derive the FFT for any segment of a nonterminating data sequence directly from the FFT computed for the previous segment, with fewer computations.

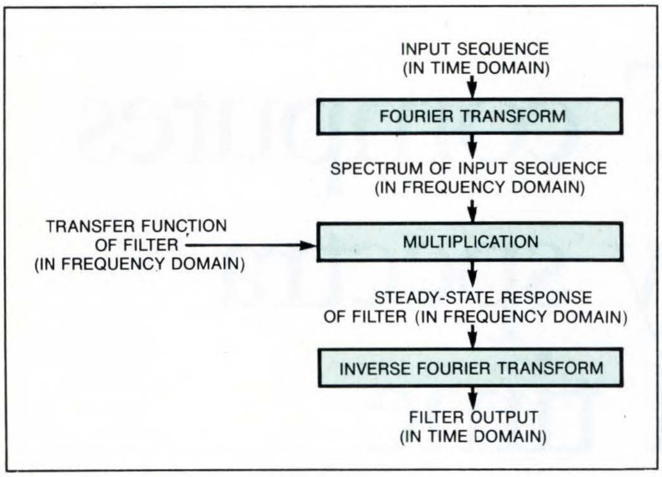

***Fig 1—You can describe the steady-state behavior** of a linear system in the frequency domain by computing the product of the system transfer function and the complex frequency spectrum of the input signal.*

Fourier transform. Because of this computational delay, the real-time bandwidth is typically narrower than the input-signal bandwidth by approximately an order of magnitude.

Any system that must detect transient phenomena in the frequency domain must meet the same performance requirements that a Fourier analyzer must meet in order to generate quasi-instantaneous frequency spectra. The transformation of discrete data from the time domain to the frequency domain is almost always accomplished by means of the FFT; thus, the ability of a system to track dynamic changes in the spectral content of a signal often depends primarily on the speed with which the system can execute the FFT algorithm.

Feedback loops may not tolerate delays

This speed limitation can be an important consideration in digital-filter design. You'd commonly define such filters in terms of frequency-domain parameters and implement them with frequency-domain techniques. Filter design usually begins when you specify a desired frequency response, so frequency-domain methods provide a very direct approach to filter design. Furthermore, it's very simple to describe the steady-state behavior of a linear system in the frequency domain by computing the product of the system transfer function and the complex frequency spectrum of its input **(Fig 1).** Because the FFT efficiently carries out the necessary time/frequency domain transformations, frequency-domain signal processing is computationally attractive for filter applications.

You may find, however, that in some real-time applications such as control systems, using the conventional FFT algorithm renders the filter unsuitable. The reason is that an N-point FFT operates on blocks of N points at a time; thus, it doesn't generate spectra instantaneously for each incoming sample; it generates spectra only at regular intervals. The resulting propagation delay in the computed response of the filter might not be tolerable within a feedback loop. The example below shows the effects of the delay for a 64-point FFT.

Consider a system at steady state that experiences a perturbation (a spike at $t=64$). **Fig 2a** shows the data sequence. Because the FFT is a block operation, it must accumulate 64 new samples before it reevaluates the spectrum; in other words, at $t=63$ it transforms $\{x(0),\ldots,x(63)\}$, at $t=127$ it transforms $\{x(64),\ldots,x(127)\}$, and so on. **Fig 2b** shows a 64-point block of samples beginning at $t=0$ (which doesn't include the spike), and **Fig 2c** shows the frequency spectrum of the block. **Fig 2d** shows the block of samples beginning one sample period later at $t=1$ (now containing the spike), and **Fig 2e** shows its corresponding spectrum. Note the spectral components that the spike introduces—the actual spectrum of the signal has changed at $t=64$, but the system can't detect the change until the next transform. After the spike has occurred, the system must collect 63 more samples before it can revise the spectrum that it calculated at $t=63$. Thus, computing the FFT introduces a delay into the system's response.

In many applications, you can't afford to ignore the dynamic behavior of signals in the frequency domain; however, the FFT updates the frequency spectrum only at the rate f_s/N (where f_s is the sample rate). In Fourier-analyzer terminology, the "real-time bandwidth" is limited to 1/N of the "input-signal bandwidth." This situation would be improved if the system could generate spectra at the sample rate.

Sliding FFT algorithm reduces delays

You might at first think that in order to update the frequency spectrum on a real-time basis, the system would have to recalculate the FFT for each new sample of the input sequence. Intuitively, you'd conclude that this procedure is wasteful, because only one point in the sequence changes for each recomputation of the FFT. Under certain conditions, however, you can apply a faster method of calculating frequency spectra in real time.

It turns out that you can derive an FFT for a segment of the N-point data sequence, beginning at time k+1, directly from the FFT computed for the prior segment that began at time k; this procedure saves a considerable amount of computation time. As suggested by its name, the sliding FFT "slides" over the data sequence, N points at a time **(Fig 3)**. The important constraints are that the input data must be presented in a nonterminating sequence, and that the input-signal bandwidth must be no greater than the real-time bandwidth.

To understand how the algorithm works, let the FFT of the k^{th} sampling interval be $X^k_{(m)}$; that is

$$\text{FFT of } \{x(k),\ldots,x(k+N-1)\} = X^k_{(m)}.$$

Then,

$$X^{k+1}_{(m)} = e^{j(2\pi m)/N}(X^k_{(m)} + x_{k+N} - x_k).$$

This equation states that the FFT of the $k+1^{th}$ sampling interval is equal to the phase-shifted sum of the previous FFT and the difference between the newest sample and the oldest—that is, between the sample entering the leading edge of the window and the sample leaving the trailing edge. For the mathematical details of this relationship, see **box,** "Derivation of the sliding FFT."

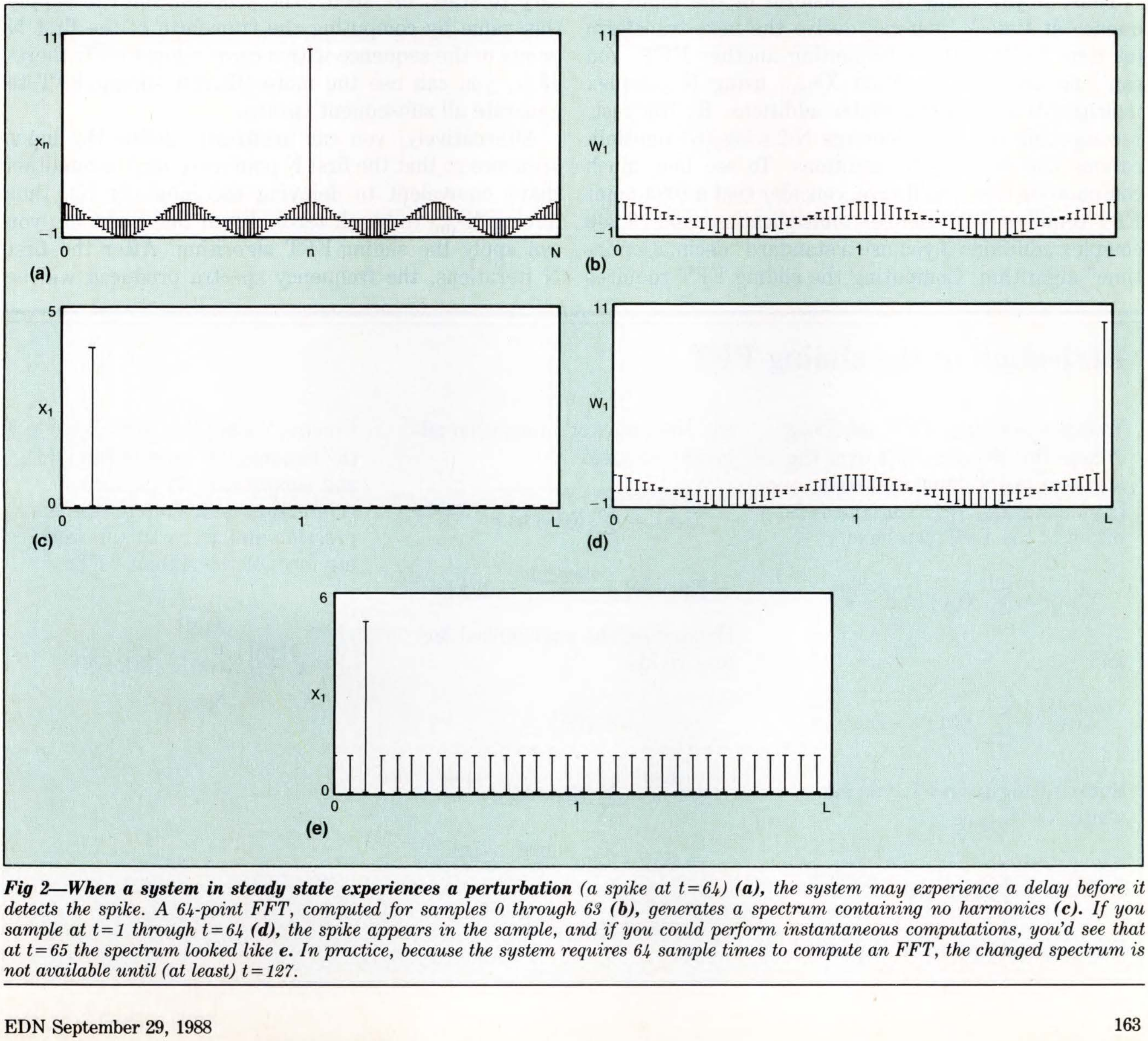

Fig 2—When a system in steady state experiences a perturbation *(a spike at t=64)* ***(a),*** *the system may experience a delay before it detects the spike. A 64-point FFT, computed for samples 0 through 63* ***(b),*** *generates a spectrum containing no harmonics* ***(c).*** *If you sample at t=1 through t=64* ***(d),*** *the spike appears in the sample, and if you could perform instantaneous computations, you'd see that at t=65 the spectrum looked like* ***e.*** *In practice, because the system requires 64 sample times to compute an FFT, the changed spectrum is not available until (at least) t=127.*

An additional advantage of the sliding FFT is that it doesn't require bit reversal, as most FFT algorithms do.

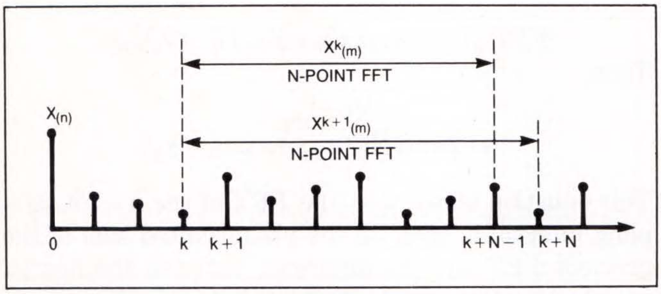

***Fig 3—You can reduce the propagation delay** by computing the first spectrum with the ordinary FFT algorithm, but thereafter deriving each new spectrum from the previous one with the aid of a simpler algorithm. In effect, you slide the window over the data, one point at a time.*

Thus, if you know the transform of the input sequence at time k, you can derive the next transform (at time k+1) without computing another FFT. You can calculate $X^{k+1}{}_{(m)}$ from $X^k{}_{(m)}$, using N complex multiplications and N complex additions. By contrast, recomputing the FFT requires $N/2 \times \log_2(N)$ multiplications and $N \times \log_2(N)$ additions. To see how much computation time you'll save, consider that a 1024-point FFT requires 5120 complex multiplications and 10,240 complex additions if you use a standard "decimation-in-time" algorithm. Computing the sliding FFT requires only 1024 complex multiplications and 1025 complex additions, including $x_{(k+N)} - x_{(k)}$. The amount of time you save will be system dependent, and it will increase with the size of the FFT.

An additional advantage of the sliding FFT is that it doesn't require bit reversal, as most FFT algorithms do. Further, the sliding FFT doesn't require that the data sequence be of a particular length, as fixed-radix FFTs do. Sliding FFTs make it easier to format the input data, therefore.

The sliding FFT is defined *recursively*. That is, at each point in time the algorithm demands that you know the spectrum that existed at the previous point in time. Obviously, an initial value—$X^0{}_{(m)}$—is necessary to start, or "seed," the process. You can supply this value by computing the transform of the first N points of the sequence with a conventional FFT; thereafter, you can use the more-efficient sliding FFT to generate all subsequent spectra.

Alternatively, you can arbitrarily define the input sequence so that the first N points are zero (a condition that's equivalent to delaying the input by N), thus forcing $X^0{}_{(m)}$ to be all zeros. From that point on, you can apply the sliding-FFT algorithm. After the first N iterations, the frequency spectra produced will be

Derivation of the sliding FFT

To derive a sliding FFT, let $X^k{}_{(m)}$ denote the N-point FFT over the segment of the input sequence $\{x_{(k)},\ldots,x_{(k+N-1)}\}$. From the definition of the FFT you have

$$X^{k}_{(m)} = \sum_{n=0}^{N-1} X(n+k)\, e^{-j\frac{2\pi mn}{N}}$$

and

$$X^{k+1}_{(m)} = \sum_{n=0}^{N-1} X(n+k+1)\, e^{-j\frac{2\pi mn}{N}}.$$

Substituting p=n+1, you can write $X^{k+1}{}_{(m)}$ as

$$X^{k+1}_{(m)} = \sum_{p=1}^{N} X(p+k)\, e^{-j\frac{2\pi m(p-1)}{N}}.$$

The summation can be expanded, and the index of summation adjusted, to yield

$$X^{k+1}_{(m)} = \sum_{p=0}^{N-1} X(p+k)\, e^{-j\frac{2\pi m(p-1)}{N}} + X(k+N)\, e^{-j\frac{2\pi m(N-1)}{N}} - X(k)\, e^{j\frac{2\pi m}{N}}.$$

Expanding the exponential factors yields

$$X^{k+1}_{(m)} = e^{j\frac{2\pi m}{N}} \cdot \sum_{p=0}^{N-1} X(p+k)\, e^{-j\frac{2\pi mp}{N}} + X(k+N)\, e^{-j\frac{2\pi mN}{N}} \cdot e^{j\frac{2\pi m}{N}} - X(k)\, e^{j\frac{2\pi m}{N}}.$$

Finally, noting the periodicity of the exponential term ($e^{j2\pi m}=1$), and substituting $X^k{}_{(m)}$ for the summation, you simplify the expression and arrive at the working form of the sliding FFT:

$$X^{k+1}_{(m)} = e^{j\frac{2\pi m}{N}} \left[X^{k}_{(m)} + X(k+N) - X(k) \right].$$

LISTING 1

```
'-----------------------------------------------------------------------
'
'                 SLIDING FFT ROUTINE   4-28-88
'         This routine compares the length of time required to compute
'    an N-PT. FFT using a conventional decimation-in-time algorithm vs.
'    the "Sliding FFT" technique discussed in the accompanying article.
'
'         Since the Sliding FFT is a recursive algorithm the Transform
'    resulting from the first algorithm is used as an input.  In other
'   words, the frequency spectrum at time k is provided and the Sliding
'   FFT is used to calculate the spectrum at the next point in time (see
'   FIG. 1).
'
'         The program prints a record of the calculation time required;
'   this is a rough indication of the speed with which a non-terminating
'   data sequence could be sampled and its frequency spectrum updated.
'
'-----------------------------------------------------------------------
DEFINT A-N: CLS
PRINT "Enter the exponent of 2 which determines the length of the FFT"
INPUT M
N=2©M                              'length of FFT=N
DIM XR(N), XI(N)                   'input/output arrays (real & imag.)
DIM ER(N), EI(N)                   'exponential phase shift table
FOR I=1 TO N                       'create random input array
XR(I)=RND
XI(I)=RND
NEXT I
XROLD=XR(1): XIOLD=XI(1)           'save old sample
XRNEW=RND: XINEW=RND               'save new sample
PI=3.14159
'---------  BEGINNING OF CONVENTIONAL FFT ------------------------------
TIME$="00:00:00"
NV2=N/2
NM1=N-1
J=1
FOR I=1 TO NM1                     'do bit-reversal of input data
IF I>=J THEN GOTO 520
TR=XR(J)
TI=XI(J)
XR(J)=XR(I)
XI(J)=XI(I)
XR(I)=TR
XI(I)=TI
520  K=NV2
530  IF K>=J THEN GOTO 570
J=J-K
K=K/2
GOTO 530
570  J=J+K
NEXT I
FOR L=1 TO M                       'begin decimation-in-time alg'thm
LE=2©L
LE1=LE/2
UR=1!
```

Listing continued on pg 166

The sliding FFT is attractive in comparison with conventional algorithms when you need to update the spectrum at rates approaching the sampling frequency.

LISTING 1 *(Continued)*

```
UI=0!
WR=COS(PI/LE1)
WI=-SIN(PI/LE1)
FOR J=1 TO LE1
FOR I=J TO N STEP LE
IP=I+LE1
TR=XR(IP)*UR-XI(IP)*UI
TI=XR(IP)*UI+XI(IP)*UR
XR(IP)=XR(I)-TR
XI(IP)=XI(I)-TI
XR(I)=XR(I)+TR
XI(I)=XI(I)+TI
NEXT I
TR=UR*WR-UI*WI
TI=UR*WI+UI*WR
UR=TR
UI=TI
NEXT J
NEXT L
'--------- END OF CONVENTIONAL FFT ------------------------------------
M1$=MID$(TIME$,4,2): S1$=MID$(TIME$,7,2)
'
'   Since the exponential phase shift table is a constant factor, and
'   not re-computed each time the algorithm is used, it is not included
'   in the performance comparison.
'
FOR I=1 TO N
ER(I)=COS(2*PI*(I-1)/N)             'Real part of phase term
EI(I)=SIN(2*PI*(I-1)/N)             'Imaginary part of phase term
NEXT I
'---------  BEGINNING OF SLIDING FFT ----------------------------------
TIME$="00:00:00"
DR=XRNEW-XROLD: DI=XINEW-XIOLD      'diff. term = (newest term)-(oldest)
FOR I=1 TO N
TR=XR(I)+DR: TI=XI(I)+DI   'add above term to terms in previous spectrum
XR(I)=ER(I)*TR-EI(I)*TI    'multiply previous spectrum by phase shift
XI(I)=ER(I)*TI+EI(I)*TR    'term-by-term
NEXT I
'--------- END OF SLIDING FFT -----------------------------------------
M2$=MID$(TIME$,4,2): S2$=MID$(TIME$,7,2)
CLS: PRINT TAB(10);"TIME REQUIRED FOR ";N;"-POINT FFT": PRINT
PRINT TAB(10);"CONVENTIONAL";TAB(40);"SLIDING"
PRINT TAB(10);M1$;" MIN.  ";S1$;" SEC.";TAB(40);M2$;" MIN.  ";S2$;" SEC."
END
```

valid. Remember, however, that it takes longer to calculate N sliding FFTs than it does to calculate an N-point FFT by the conventional method. You'll find the results of a quick benchmark comparison between the conventional-FFT and sliding-FFT algorithms in **Tables 1** and **2.**

The Turbo-Basic source listing for the benchmark program appears in **Listing 1.** The program measures performance by using Basic's TIME$ system call to time random data sequences of varying length. The program calculates the conventional FFT first and uses the result to seed the sliding FFT, as described above. Obviously, the execution speed of the Basic interpreter running on an IBM PC/XT or PC/AT is far below the speed that any practical DSP application would require; however, this crude example clearly shows the

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A conventional 64-point FFT won't detect a spike at t=1 until t=127, when the system has collected all remaining data points and computed the new spectrum.

advantage of the sliding FFT. Also note that, as expected, the margin of improvement is greater for longer data sequences.

Although you can use the sliding FFT to enhance real-time spectral analysis, you must observe its inherent constraints. First, the input data must be part of some nonterminating sequence. The benefit of the sliding FFT algorithm is that performing recursive calculation of the spectra of an unending sequence is inherently more efficient than applying the general methods for calculating the discrete Fourier transform to each N-point window as though it were unrelated to the previous one. However, if $X^{k+1}_{(m)}$ and $X^{k}_{(m)}$ actually *are* unrelated, the algorithm is of no use.

Second, if the system must sample the data at a faster rate than the rate at which it can compute the sliding FFT (input-signal bandwidth exceeds real-time bandwidth), you can't use the algorithm. The reason is that the recursive calculation of the transform presumes that the samples are consecutive, so the time required for calculation effectively limits the sampling rate. If the input sequence contains frequency components that are higher than the sampling rate, aliasing will occur in the resultant spectra.

Don't assume that the sliding FFT's computational efficiency applies to all circumstances. In fact, only when you need to compute spectra at a rate that's close to the sampling frequency does the sliding FFT become attractive in comparison with the ordinary FFT. The system must repeat the calculations in the sliding algorithm for each sample; after N samples, you have N^2 multiplications. With a conventional FFT, the same N samples could be transformed at a cost of only N/2($\log_2$(N)) multiplications. The big difference is that you have to wait until the entire block of N samples has been acquired before the ordinary FFT can yield the spectrum.

TABLE 1—BENCHMARK RESULTS FOR AN IBM PC/XT

FFT LENGTH (POINTS)	CONVENTIONAL	SLIDING
128	9 SEC	1 SEC
256	21 SEC	3 SEC
512	46 SEC	6 SEC
1024	1 MINUTE, 40 SEC	12 SEC
2048	3 MINUTES, 38 SEC	24 SEC
4096	7 MINUTES, 50 SEC	49 SEC
8192	16 MINUTES, 50 SEC	1 MINUTE, 37 SEC

TABLE 2—BENCHMARK RESULTS FOR AN 8-MHz IBM PC/AT

FFT LENGTH (POINTS)	CONVENTIONAL	SLIDING
128	<1 SEC	<1 SEC
256	<1 SEC	<1 SEC
512	1 SEC	<1 SEC
1024	3 SEC	<1 SEC
2048	6 SEC	<1 SEC
4096	14 SEC	1 SEC
8192	31 SEC	3 SEC

If that much delay would reduce the system's tran-

Update rate governs sliding FFT's efficiency

To find out whether the sliding FFT is computationally efficient for your application, you have to find the sampling rate at which the sliding FFT requires fewer complex multiplications than the conventional FFT does. In the conventional algorithm, each computation of an N-point frequency spectrum requires N/2($\log_2$(N)) multiplications, whereas the sliding FFT requires only N^2 multiplications.

The computational requirements of the conventional FFT will equal those of the sliding FFT when the spectrum-update rate—f_r (number of updates per sampling period)—is such that

$$f_r \cdot \frac{N}{2} \log_2 (N) = N^2,$$

where $0<f_r\leq N$. Then, for

$$f_r \geq \frac{2N}{\log_2 (N)} = \frac{N}{\log_2 (\sqrt{N})},$$

the sliding FFT will require fewer complex multiplications. Relative to the sample rate $f_s=N$, the sliding FFT is computationally more efficient when:

$$\frac{f_r}{f_s} \geq \frac{1}{\log_2 (\sqrt{N})}.$$

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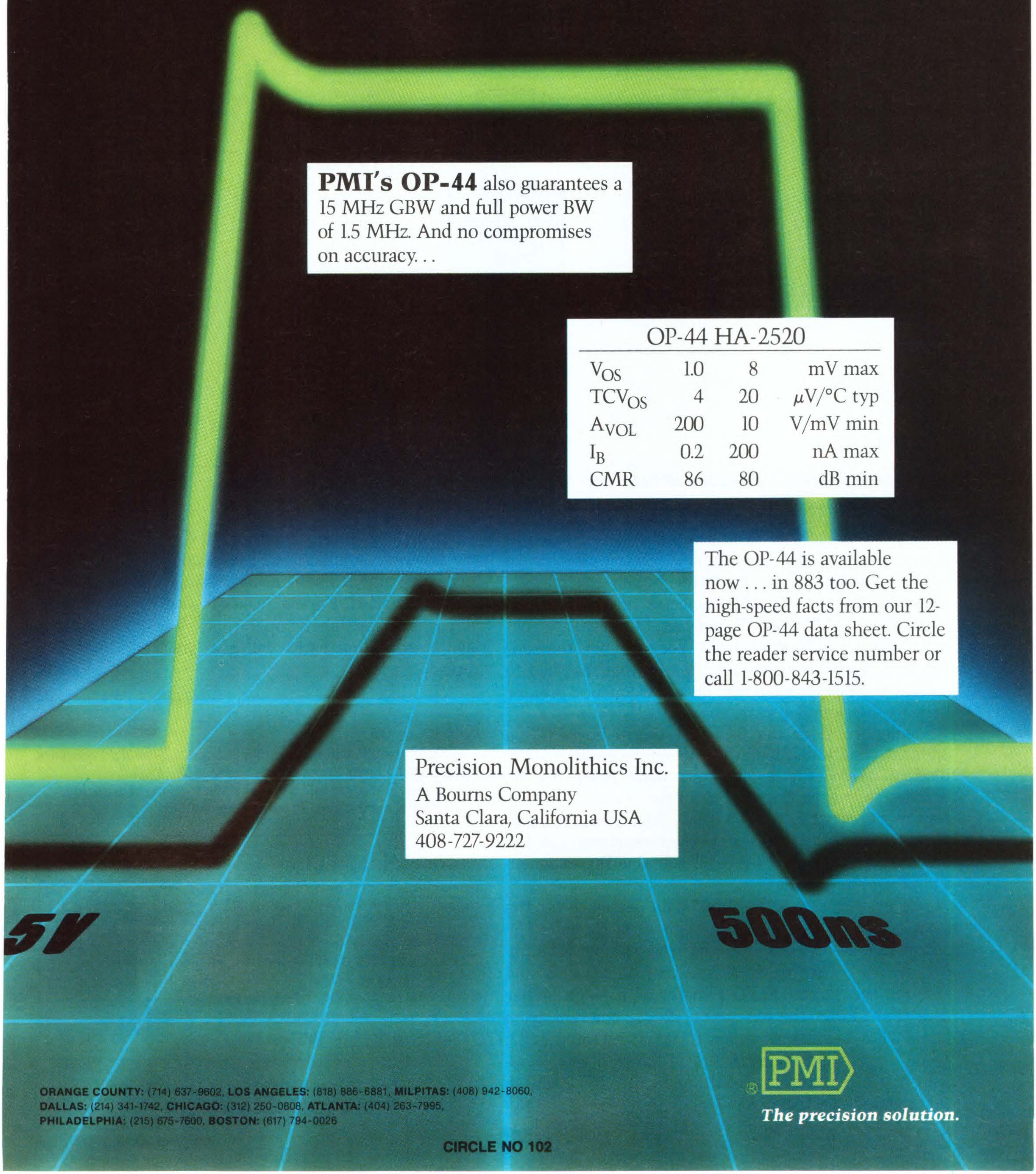

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Provided that you observe a few simple constraints, you can use the sliding FFT to enhance real-time spectral analysis.

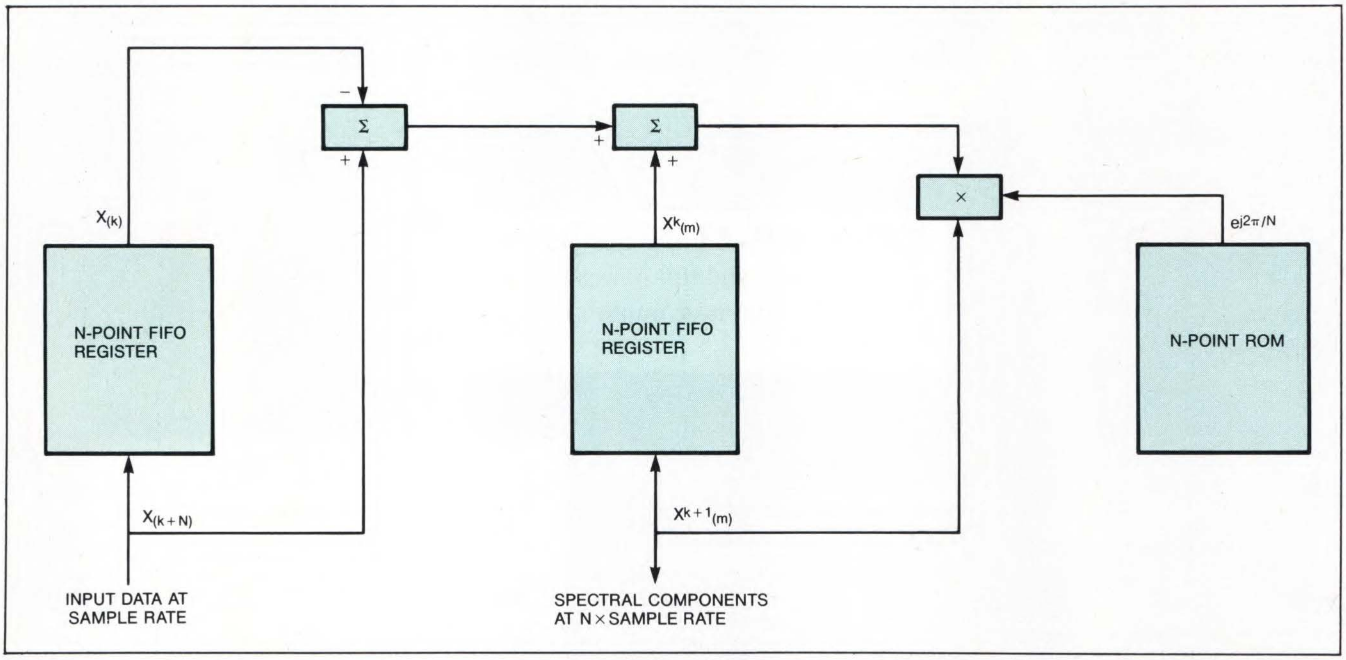

Fig 4—You can implement the sliding FFT algorithm in hardware *with the aid of two FIFO registers and a ROM that holds the system transfer function.*

sient performance to an unacceptable level, you can choose either to compute the FFT more often or to use the sliding FFT. The latter becomes a bargain whenever the rate at which spectra must be recomputed exceeds $f_s/\log_2 \times \sqrt{N}$ (see **box,** "Update rate governs sliding FFT's efficiency"). For example, the sliding FFT would be preferable in a system that had to update a 256-point spectrum at any frequency greater than 1/4 the sampling rate.

Finally, consider the fact that the sliding FFT is eminently suitable for hardware implementation. The block diagram **(Fig 4)** depicts a basic design for an N-point sliding FFT unit. One of the two FIFO registers represents the window that slides over the input data, and the other represents the recursively-updated frequency spectrum. The ROM contains the exponential phase-shift terms.

The system clocks the input data sequence (at the sample rate f_s) into the FIFO register at the left. The oldest sample (x_k) is subtracted from the newest sample (x_{k+N}). The previous spectral data is clocked through the second FIFO register at a much higher rate ($N \times f_s$). As the mth point, $X^k_{(m)}$, emerges from the FIFO register's output, it is summed with $x_{k+N} - x_k$ and multiplied by the mth entry in the phase-shift ROM, $e^{j(2\pi m)/N}$, resulting in the mth point in the updated spectrum, $X^{k+1}_{(m)}$.

From the block diagram in **Fig 4,** you can see that the inherent simplicity of the sliding-FFT algorithm lends the algorithm to a very straightforward hardware realization. Further, you can easily include parallel paths for arithmetic operations. Well-designed parallel computation paths will give you very high data rates. EDN

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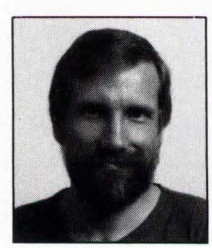
2. "Signal Analyzers," *Test and Measurement Catalog,* Hewlett-Packard Corp, Palo Alto, CA, 1988.

Author's biography

Tom Springer is a design engineer at Pinson Associates Inc (Austin, TX). He holds a BSEE from Michigan State University and is currently a doctoral candidate in electrical engineering at the University of Texas. Tom is a member of Eta Kappa Nu, Tau Beta Pi, and the IEEE. In his spare time he enjoys playing the guitar.



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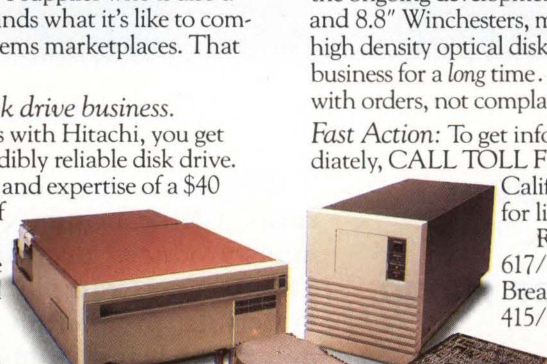

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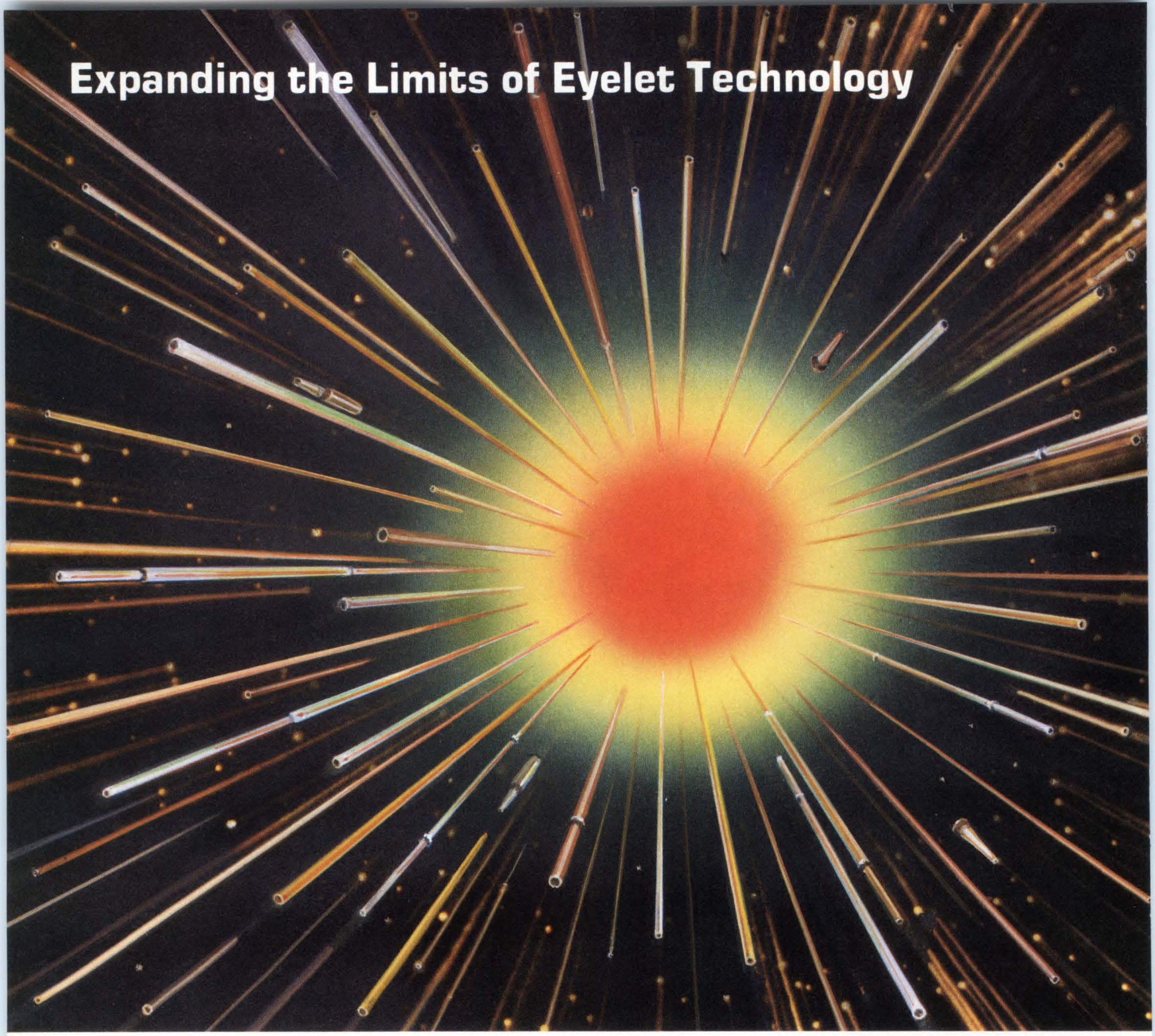

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Spice techniques facilitate analysis of feedback circuits

New, easy-to-apply methods for using Spice allow you to obtain accurate gain and phase information for closed-loop analog circuits that use negative feedback. The new techniques eliminate the loading errors caused by the blocking inductor and the coupling capacitor traditionally used to block and inject signals in Spice simulations.

Steven C Hageman, *Calex Manufacturing Co Inc*

Spice, the venerable analog circuit simulator devised by the University of California Berkeley **(Ref 1)**, is useful for the analysis and measurement of the feedback properties of analog circuits. Traditional Spice-based methods use large-value inductors and capacitors to open the feedback circuit for ac analysis while still allowing Spice to find the proper dc operating point. In simple or close-to-ideal circuits, these methods work fine, but in the analysis of less-than-ideal circuits, errors arise because of improper loading caused by the loop-injection capacitors and inductors. Although complex methods are available to handle these problems **(Ref 2)**, the methods presented here do not disturb the loop impedances at all, and thus eliminate the need for "circuit mirroring" or, alternatively, the acceptance of errors that accrue from improper loading.

These methods also allow Spice to find the dc operating point. The techniques are especially useful with the latest PC-based Spice implementations that have graphical postprocessing that performs waveform mathematics (vector addition, subtraction, multiplication, and division). These methods will work with any Spice implementation that provides "hand analysis" of output files; the techniques are applicable to non-Spice simulators as well. The examples that follow use MicroSim's PSpice syntax **(Ref 3)**.

Transfer-function analysis

Fig 1 gives the simplest example of waveform mathematics applied to feedback-loop circuits. This configuration is a common test circuit for determining the transfer function of an operational-amplifier inverter circuit. You can, of course, extend this analysis concept to any circuit configuration that has input-output nodes and a summing point at virtual ground. You run the analysis by setting V_{IN} to an ac magnitude of 1V. Frequency is the variable, and the desired output is node 3. In PSpice, the graphical-output command (see **box**, "PSpice's Probe postprocessor syntax") for the results at node 3 would be

DB(VM(3))	Transfer Function
VP(3)	Transfer-Function Phase.

This command syntax produces a display of the transfer function and phase response of the circuit (at node 3) as a function of frequency.

All driving-voltage and -current sources use a unity

In the analysis of nonideal circuits, loop-injection capacitors and inductors introduce errors. New simulation methods do not disturb loop impedances in any way.

input value (that is, 1V ac or 1A ac) to make the outputs scale conveniently. Because Spice linearizes the circuit around the dc operating point for the ac analysis, the ac value has no effect on the resulting analysis accuracy.

The node 3 result does not mark the end of the usefulness of the analysis run because PSpice will save the results of every node during the analysis (you can also instruct other Spice versions to save other nodes). You can use this saved information to simultaneously determine both the op amp's open-loop gain and the loop gain (see **box,** "Understanding loop-gain nomenclature") by looking at nodes 2 and 3. The open-loop gain is the $\log_{10}$ ratio of the voltages at node 3 and node 2, and the loop gain is the logarithm of the voltage at node 2. In PSpice, the commands are

DB(VM(3)/VM(2))	Open-Loop Gain
VP(3)-VP(2)	Open-Loop Phase
−DB(VM(2))	Loop Gain
VP(2)	Loop Phase.

Because these additional analyses are dependent on the feedback network, they are really only approximations that hold true when $f<<f_c$ (the 0-dB frequency of the open-loop gain) and when the open-loop gain>>the loop gain. Therefore, use them with caution.

Even this simple example shows the wealth of feedback-loop performance data available when you apply waveform mathematics to Spice.

The classical Spice-based method of determining the

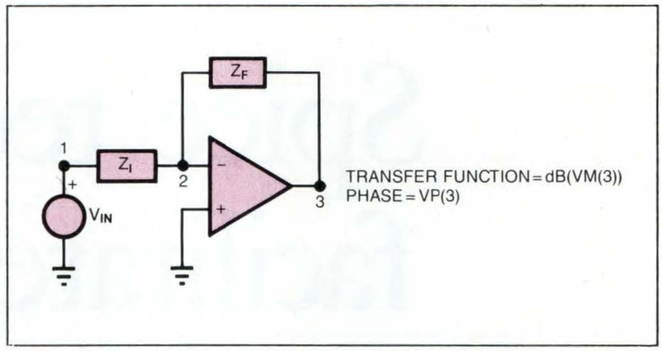

Fig 1—A common test circuit to determine an amplifier's transfer function, *this configuration uses an ideal operational amplifier in the inverting mode. Spice determines both gain and phase vs frequency.*

PSpice's Probe postprocessor syntax

PSpice has a rich set of commands for its Probe graphics postprocessor. For ac analysis, the output variables allowed are V for node voltage and I for current either into a device terminal or through an independent voltage source (usually zero valued, to act as an ammeter). You can augment these variables by using suffixes:

(none)	Magnitude
M	Magnitude
DB	Magnitude in decibels
P	Phase
G	Group Delay
R	Real Part
I	Imaginary Part.

Some usage examples are:

VM(2)	Magnitude of voltage at node 2
VDB(1)	dB magnitude of voltage at node 1
VP(3)	Phase of voltage at node 3
IR(VIN)	Real part of current through V_{IN}.

In addition to displaying just the basic quantities, Probe allows full waveform mathematics, including +, −, /, and * of quantities. Hence the command VM(1)/VM(2) would display the ratio of the voltage magnitudes at nodes 1 and 2, and VP(1)-VP(2) would display the phase difference between nodes 1 and 2.

PSpice also allows the direct measurement of current through the following devices:

R	Resistor
C	Capacitor
I	Independent Current Source
L	Inductor
T	Transmission Line
V	Independent Voltage Source.

Usage examples are

VDB(R1)	dB magnitude of voltage across R_1
IM(C10)	Magnitude of current through C_{10}
IP(L2)	Phase of current through L_2
IR(VIN)	Real part of current through V_{IN}.

loop gain of a feedback circuit is shown in **Fig 2a.** The large inductor and capacitor allow Spice to find the dc operating point for the analysis at the same time as they open the feedback loop for the ac analysis. V_{IN} is injected directly into the feedback path. The loop gain, determined from the analysis of node 2, is accurate only if the impedance looking into node 2 is much lower than the impedance looking into node 3 ($Z_2 << Z_3$).

The drawback to this classical method is that the inductor-capacitor combination disturbs the impedance balance in the loop. If the loop gain is in any way

Understanding loop-gain nomenclature

All feedback circuits have several common performance parameters that completely describe the operation of the feedback loop. The most common of these parameters are the open-loop gain, noise gain, loop gain, and transfer function.

Loop-gain and phase information are used in the determination of gain- and phase-margin information. These parameters give indications of the circuit's closed-loop stability. What is less understood is the relationship that loop gain has with noise gain and open-loop gain.

The open-loop gain is the gain the system would have if no feedback were applied. Manufacturers of op amps display it in the form of open-loop-gain curves. The noise gain is the gain the feedback system would exhibit in response to a corrupting noise source. For the inverter in **Fig A,** the noise gain is $1+R_F/R_I$ (or 20.8 dB). Another, and sometimes easier, way to analyze the noise gain is to insert the noise source into the positive input of the op amp, and then determine the V_{OUT}/V_{NOISE} transfer function.

The loop gain is the difference between the open-loop gain and the noise gain, hence it is the noise gain—and not the transfer-function gain—that determines the system bandwidth. The op-amp circuit of **Fig A** is an example of a 1-pole, inverting gain-of-10 amplifier. The accompanying graph shows the relationship of the various gains to each other.

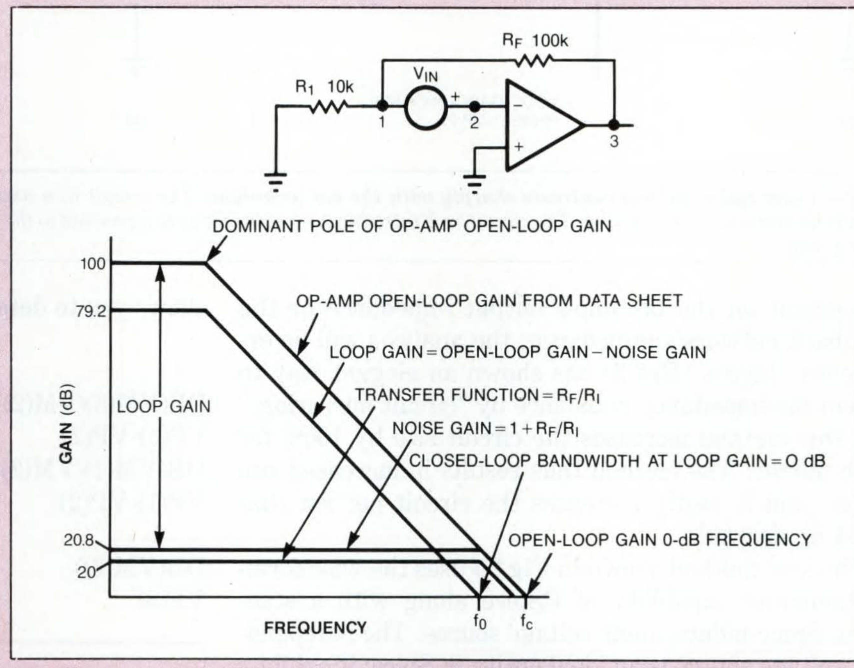

Fig A—In analyzing the performance of an inverting amplifier (a), *the important parameters are its open-loop gain (without feedback), its closed-loop gain (with feedback), and its noise gain. The graph* ***(b)*** *shows the parameters' interrelationship.*

The transfer function relates to the amplification of the amplifier vs frequency, but it is not the sole determining factor in the overall bandwidth of the circuit. The noise gain determines the bandwidth, as can be shown by placing a 1000Ω resistor from node 1 to ground. The transfer-function gain remains at 10 (20 dB), but the bandwidth is now about a decade lower because the noise gain is now 40.9 dB (noise gain $=1+R_F/(R_I \parallel 1000)$).

Any amplifier voltage noise is multiplied by the noise gain, and the input offset voltage is multiplied by the dc value of the noise gain. Therefore, if the op amp in question has a 1-mV offset voltage (referred to input), the offset seen at the output will be 11 mV (dc noise gain $=1+R_F/R_I=11$).

Spice's waveform-mathematics capabilities make it possible to determine the gain and phase of any circuit with input-output nodes and a summing junction.

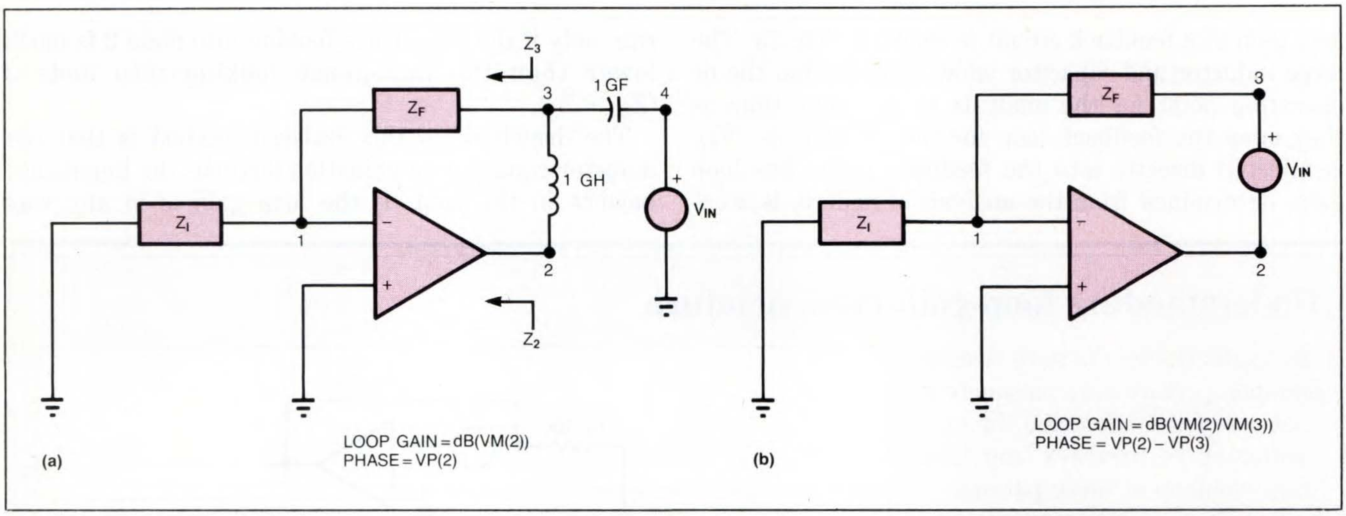

Fig 2—A new Spice method contrasts sharply with the old technique. *The circuit in **a** uses extremely high-value reactive components to provide ac blocking and coupling. The circuit in **b** introduces no extraneous components to the model and does not disturb circuit impedances in any way.*

dependent on the op amp's output impedance or the feedback network's impedance, the analysis will be erroneous. Jaycox **(Ref 2)** has shown an elegant way to lessen the impedance imbalance by "circuit mirroring," but this method increases the circuit size by 100% for each mirror. The method thus results in increased run times, and it vastly increases the circuit net list that must be derived.

The new method shown in **Fig 2b** uses the waveform-mathematics capability of PSpice along with a standard, Spice-independent voltage source. The independent voltage source is an ideal entity in Spice; it exhibits zero series impedance and infinite parallel impedance. It is truly unrealizable in actual circuit design, but you can put it to good use with Spice simulations. In **Fig 2b,** the voltage source itself breaks the feedback loop and does not change the impedance levels of the circuit at all. This scheme preserves the integrity of the feedback loop while allowing a simple loop-gain analysis. The loop gain in **Fig 2b** is determined by

DB(VM(2)/VM(3))	Loop Gain
VP(2)-VP(3)	Loop Phase.

Using the transfer-function analysis described earlier, you can also find the open-loop gain (with the same restrictions).

Fig 3 illustrates a method called "big-gun analysis." This technique allows you to determine almost all loop parameters from a single run. The ideal Spice voltage source, inserted in the loop between nodes 1 and 2, allows you to determine the following loop parameters:

DB(VM(3)/VM(2))	Open-Loop Gain
VP(3)-VP(2)	Open-Loop Phase
DB(VM(1)/VM(2))	Loop Gain
VP(1)-VP(2)	Loop Phase
DB(VM(3))	Noise Gain
VP(3)	Noise Phase.

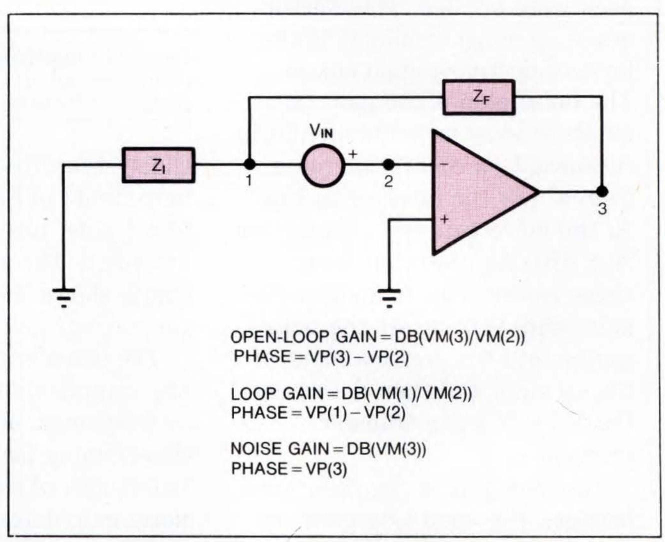

Fig 3—"Big-gun analysis" determines almost all loop parameters *from a single Spice simulation run. These parameters include open-loop gain, loop gain, noise gain, and phase. The secret to the method is the insertion of an ideal voltage source between nodes 1 and 2.*

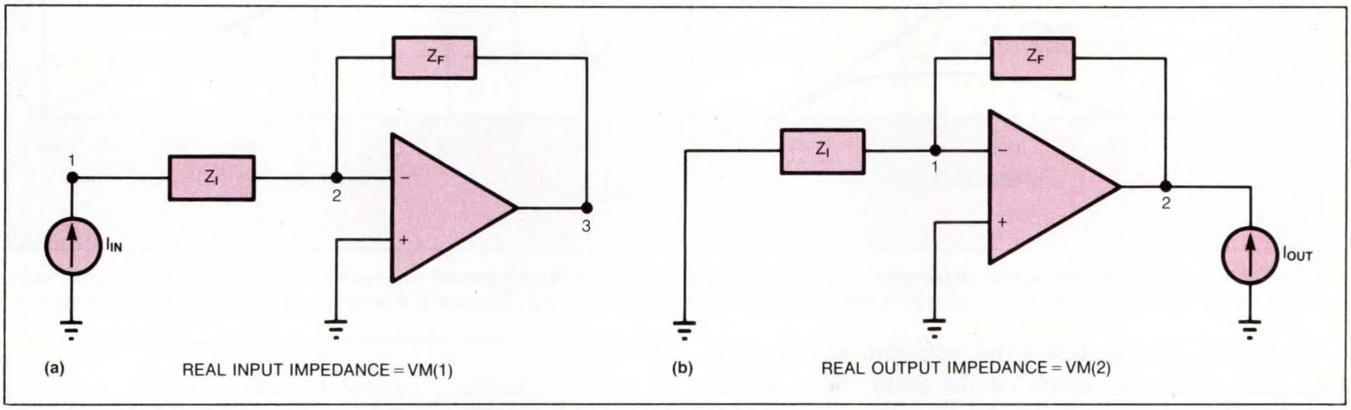

Fig 4—An ideal current source aids in determining input and output impedances. *The 1A ac source allows Spice to read the input impedance **(a)** by simply reading the voltage at node 1; when applied to the amplifier's output **(b)**, the source produces a voltage reading that equals the output impedance of the circuit.*

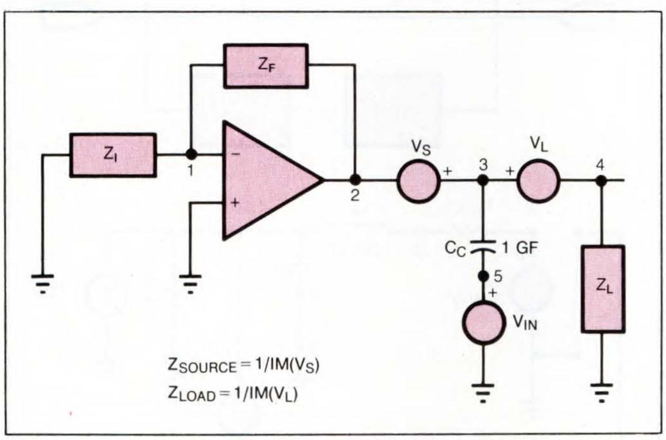

Fig 5—You can measure source and load impedances simultaneously. *V_S and V_L are zero-valued voltage sources. The reciprocal of the measured current in these sources is the real part of the impedance in ohms when V_{IN} = 1V ac. The large blocking capacitor, C_C, provides near-ideal coupling to the source V_{IN}.*

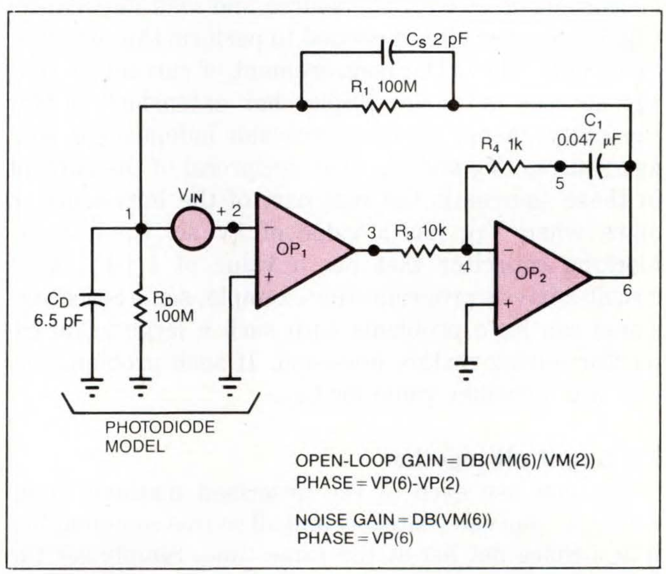

Fig 6—This low-noise photodiode amplifier circuit *uses a compound-amplifier block that limits the noise gain of the circuit but does not reduce the I/V bandwidth. V_{IN} is the independent ac source used for the Spice feedback analysis. The accompanying Spice run of **Listing 1** uses the "big-gun" analysis technique.*

You can determine all of these important loop parameters in a single PSpice run without incurring any penalty on run time, thanks to the fact that PSpice stores the results of each node in the analysis. Using a circuit setup like the one in **Fig 3,** you can determine important loop parameters like gain and phase margins, as well as information on how the circuit will respond to amplifier noise.

Z_{IN} and Z_{OUT} analyses

Other useful information about generalized feedback circuits includes input- and output-impedance values. You can determine these parameters by using a Spice-model independent 1A current source connected to the input or output nodes of the feedback circuit, as shown in **Fig 4.**

You determine the input impedance by placing a 1A independent ac current source on the input to the feedback circuit. The impedance is

VM(1) Real Part of Input Impedance (Ω).

In similar fashion, you can determine the output impedance of a feedback circuit by placing a 1A independent ac current source on the output of the circuit. The impedance is

VM(3) Real Part of Output Impedance (Ω).

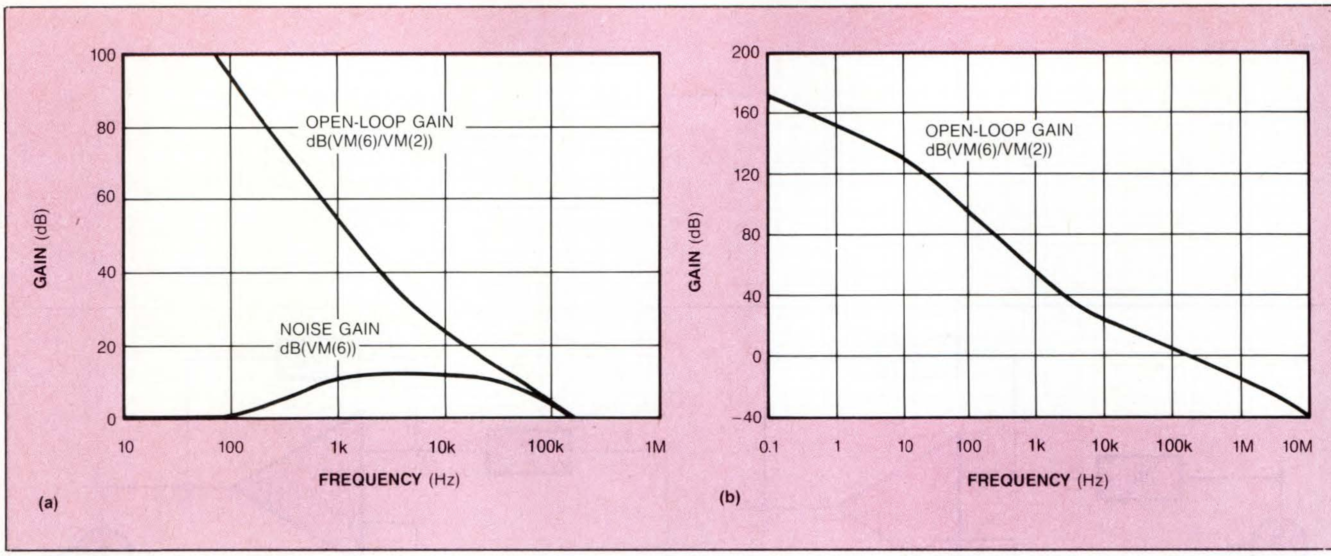

***Fig 7—Spice-derived open-loop gain, noise gain, and phase characteristics of Fig 6's circuit** are visible in these plots. The various poles and zeros of the open-loop gain and the noise gain are evident from the breakpoints in **a**. The plot in **b** gives the phase response of the amplifier.*

Of course, you can derive the loop gain and the open-loop gain of the feedback circuit from these runs as well (again with accuracy restrictions).

Epler **(Ref 4)** has shown a way to extend the output-impedance measurement to allow the simultaneous measurement of both the source and load impedance. **Fig 5** shows the circuit needed to perform this analysis. Spice only allows the measurement of current in voltage sources (although PSpice has extensions to this capability), hence the two zero-value independent voltage sources, V_S and V_L. The reciprocal of the current in these sources is the real part of the impedance in ohms when V_{IN} has a value of 1V ac. C_C is a dc-blocking capacitor that has a value of 1 GF. Some circuit-analysis programs (for example, some Spice versions) can have problems with such a large-value capacitor during matrix inversion. If such problems occur, use a smaller value for C_C.

Putting it all together

You can use each of the described methods separately, or you can write any and all source combinations into a Spice net list at the same time. Simply set the desired source on with an "ac 1" statement or off with an "ac 0" statement for the particular analysis you wish to run. For example, you can use the big-gun analysis with the transfer-function analysis. By setting the desired sources either on or off, you can obtain the proper Spice run. This flexibility exists because an independent source in Spice, when turned off, displays ideal passive characteristics and will not disturb the circuit's impedance levels.

Some practical examples are useful to illustrate the workings of these Spice methods. For instance, you can design a low-noise photodiode amplifier **(Ref 5)** by using a compound-amplifier block that will limit the noise gain of the resulting circuit but that won't reduce the I/V bandwidth. As shown in **Fig 6,** this circuit consists of a model of an HP5082-4204 photodiode at the input of a 2-op-amp amplifier, in which V_{IN} serves

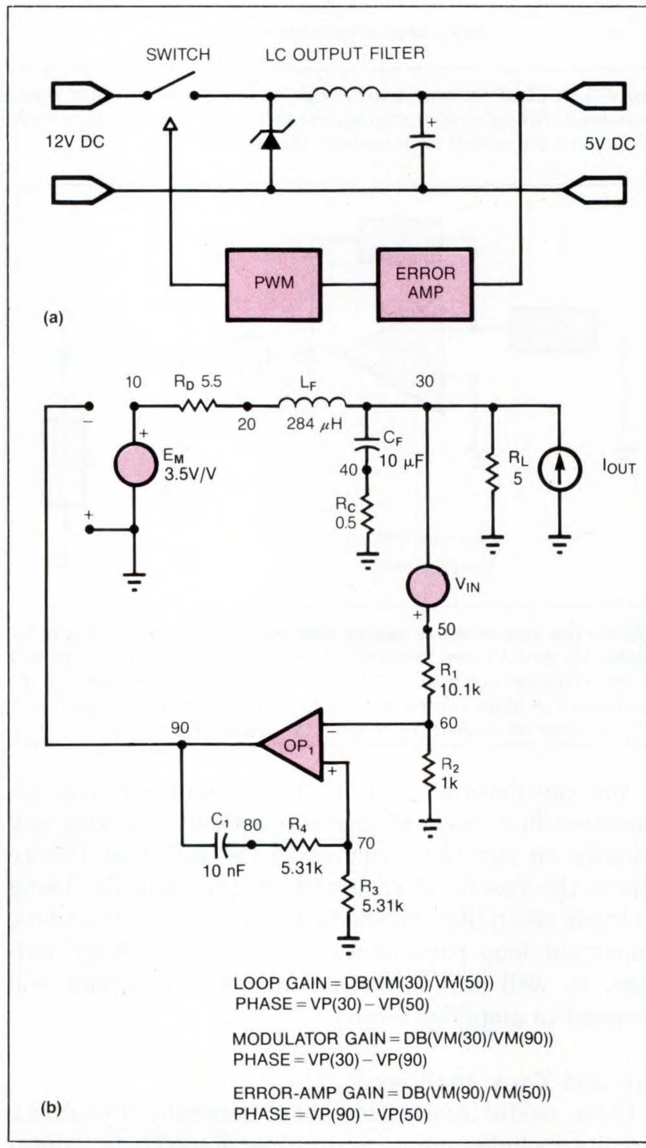

***Fig 8—Spice finds application in power-supply designs, too.** The simulation of this buck-type regulator **(a)** provides gain and phase for the loop, the modulator, and the error amplifier, as well as the regulator's output impedance. The equivalent circuit **(b)** correctly models all small-signal loop dynamics of the regulator.*

Because Spice linearizes a circuit around the chosen dc operating point, this quiescent point has no effect on the ac analysis.

LISTING 1—PHOTODIODE AMPLIFIER

```
 ANALYSIS DIRECTIVES
AC DEC 10   0.1   10E6                         ; AC ANALYSIS 0.1Hz TO 10MHz
PROBE                                          ; FOR PSPICE'S GRAPHICS POST PROCESSOR

* INPUT DRIVING SOURCES
VIN   2   1   AC 1                             ; INPUT DRIVING SOURCE

* CIRCUIT DESCRIPTION
R1    1   6   100MEG
CS    1   6   2P
R3    3   4   10K
R4    5   6   1K
C1    4   5   0.047U

* PHOTODIODE MODEL
RD    1   0   1E11                             ; HP 5082-4204 PHOTODIODE MODEL
CD    1   0   6.5P

* OPAMPS
XOP1  0  2   3  OPA111
XOP2  0  4   6  OPA404

*=============================================================================================

* SMALL SIGNAL OPA111 MACROMODEL SUBCIRCUIT
SUBCKT OPA111 1 2 3
*
*
*                 +- OUTPUT
*               +--- INVERTING INPUT
*             +----- NON INVERTING INPUT

RIN    1    2    1G                            ; INPUT IMPEDANCE

* GAIN STAGE AND 1ST POLE
GM 0, 10   1, 2   1                            ; GAIN = 100K, POLE AT 15Hz
RG    10  0    100000
CP1   10  0    106N

* OUTPUT BUFFER AND STATIC ZOUT
EOUT 20, 0    10, 0    1                       ; OUTPUT IMPEDANCE = 100 OHMS
ROUT 20    3     100
ENDS

*=============================================================================================

* SMALL SIGNAL OPA404 MACROMODEL SUBCIRCUIT
SUBCKT OPA404 1 2 3
*
*
*                 +- OUTPUT
*               +--- INVERTING INPUT
*             +----- NON INVERTING INPUT

RIN    1    2    1G                            ; INPUT IMPEDANCE

* GAIN STAGE AND 1ST POLE
GM 0, 10   1, 2   1                            ; GAIN = 100K, POLE AT 70Hz
RG    10  0    100000
CP1   10  0    22N

* OUTPUT BUFFER AND STATIC ZOUT
EOUT 20, 0    10, 0    1                       ; OUTPUT IMPEDANCE = 100 OHMS
ROUT 20    3     100
ENDS

* END OF EXAMPLE 1 NETLIST
END
```

Methods to lessen the impedance imbalance introduced by adding large capacitors and inductors to a circuit model result in larger circuits and longer run times.

as the independent ac source used for the feedback analysis.

The simulation goal is to analyze the open-loop gain for the compound amplifier and determine the noise gain of the circuit. The resulting PSpice input net list is shown in **Listing 1.** The big-gun method was the technique of choice for the analysis run because the noise gain and open-loop gain can be found with the same nodal data. The Spice net list is also shown in **Listing 1.**

Figs 7a and **7b** show the output of the analysis run. As predicted **(Ref 5),** the noise gain shows a zero at $1/(2\pi R_1 1 C_D)$ or 245 Hz, a pole at $1/(2\pi R_1 C_S)$ or 795 Hz, and a midband gain of $1 + C_D/C_S$ or 12.5 dB. You can clearly see the zero in the open-loop gain plot at $1/(2\pi R_4 C_1)$ or 3.4 kHz.

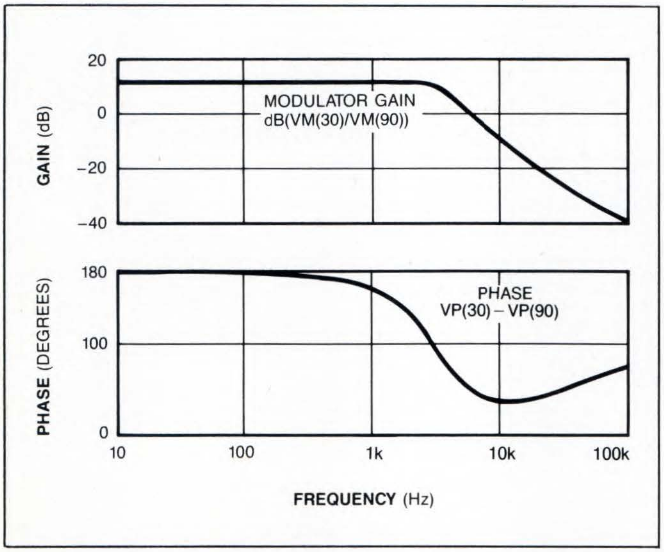

Fig 9—Spice-generated modulator gain and phase plots for Fig 8's circuit *clearly show the resonant frequency of the modulator's LC filter, as well as the zero caused by the capacitor's effective series resistance.*

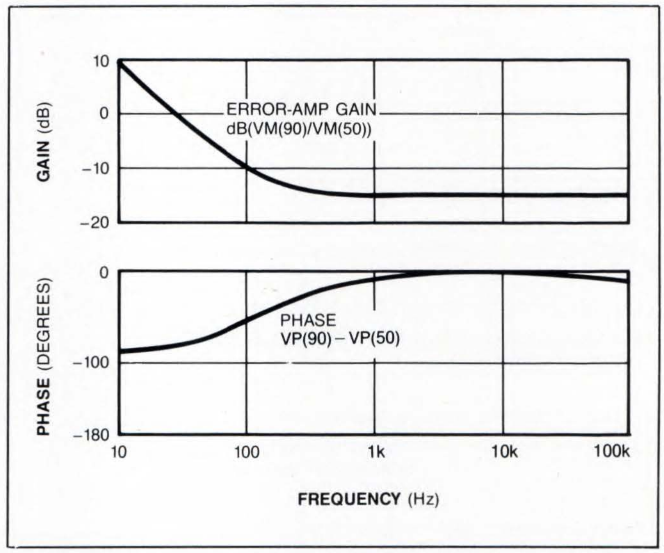

Fig 10—Spice provides gain and phase information for the error amplifier *in **Fig** 8's circuit. Clearly visible in these plots is the zero produced by the error amplifier. The error-amplifier gain is simply the log ratio of the gains at nodes 90 and 50.*

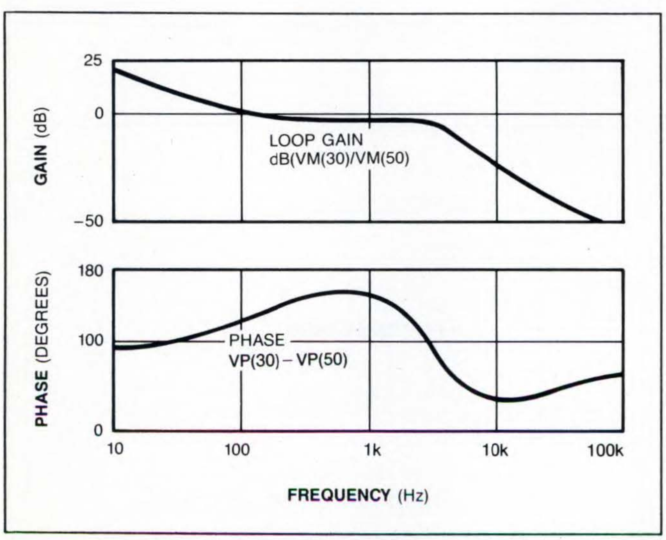

Fig 11—Loop gain and phase for Fig 8's buck-type regulator *are visible in these Spice-derived plots. The loop gain is the result of adding the modulator gain and the error-amplifier gain. The approximately 60° phase margin is evident at the point where the gain plot crosses the 0-dB threshold.*

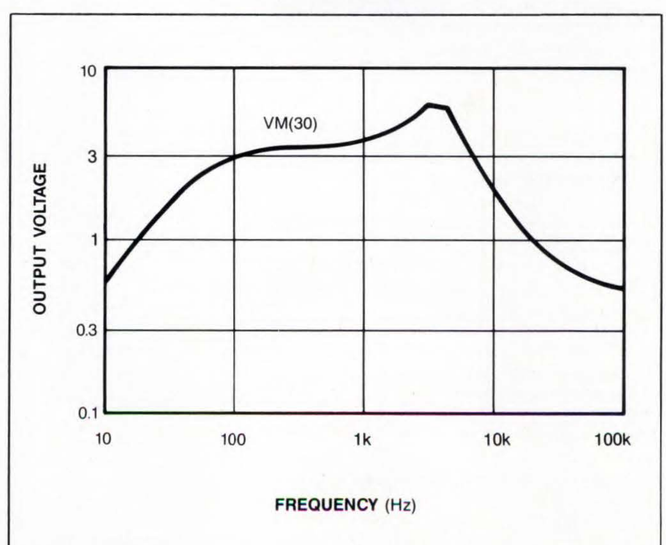

Fig 12—Volts equate to ohms in this output-impedance plot *for the buck-type regulator in **Fig 8.** The plot clearly shows the low impedances at low frequencies, as well as the impedance peak at the resonant frequency of the LC filter in the modulator.*

For a second practical example, assume you need to analyze a buck-type switching regulator (**Fig 8a**) for loop gain and phase, modulator gain and phase, error-amplifier gain and phase, and output impedance. A small-signal equivalent circuit and its net list are shown in **Fig 8b** and **Listing 2,** respectively. The equivalent circuit correctly models all small-signal loop dynamics of the converter. This analysis uses the previously described loop-gain and output-impedance methods.

Figs 9 through **12** show the resulting output plots. All the output plots with the exception of the one for the output impedance are generated from one PSpice run. The output data clearly show the resonant frequency of the modulator's LC filter, as well as the zero caused by the capacitor's ESR. Also visible are the zero produced by the error amplifier, and the loop gain and the phase margin (the loop gain is the result of adding the modulator gain and the error-amplifier gain). The output-impedance plot of **Fig 12** clearly shows the low value at low frequency and the peak at the LC filter's resonant frequency.

Listing 2 shows how the independent V_{IN} and I_{OUT} source are used in the same net list. To measure loop

LISTING 2—BUCK-TYPE SWITCHING REGULATOR

```
* ANALYSIS DIRECTIVES
 AC DEC 10   10   100000                        ; AC ANALYSIS 10Hz TO 100KHz
 PROBE                                          ; FOR PSPICE'S GRAPHICS POST PROCESSOR

* INPUT DRIVING SOURCES
VIN   50   30   AC 1                            ; SET TO 1 FOR LOOP GAIN ANALYSIS
IL    0    30   AC 0                            ; SET TO 1 FOR OUTPUT IMPEDANCE ANALYSIS

* FEEDBACK CIRCUIT DESCRIPTION
R1        50    60    10.1K
R2        60    0     1.0K
R3        70    0     5.31K
R4        70    80    5.31K
C1        90    80    0.1U
XOP1 60 70 90 ONEPOLE

* POWER STAGE MODEL
EM    10, 0    0, 90    3.5
RD    10   20    5.5

* OUTPUT FILTER
LF   20   30      284UH
CF   30   40      10U
RC   40   0       0.5

* SMALL SIGNAL SINGLE POLE OP AMP MACROMODEL SUBCIRCUIT
 SUBCKT ONEPOLE 1 2 3
*
*                     | | |
*                     | | +- OUTPUT
*                     | +--- INVERTING INPUT
*                     +----- NON INVERTING INPUT

RIN     1     2     1G                          ; INPUT IMPEDANCE

* GAIN STAGE AND 1ST POLE
GM 0, 10   1, 2    1                            ; GAIN = 50K, POLE AT 20Hz
RG     10   0      50000
CP1    10   0      0.159U

* OUTPUT BUFFER AND STATIC ZOUT
EOUT 20, 0     10, 0     1                      ; OUTPUT IMPEDANCE = 100 OHMS
ROUT 20     3      100
.ENDS

* END OF EXAMPLE 2 NETLIST
 END
```

gain, set V_{IN} to ac 1 and I_{OUT} to ac 0. To run the output-impedance analysis, set the sources in the opposite way.

It's worthy to note that you could have determined the modulator and error-amplifier gain and phase plots from the output-impedance analysis run. This alternative exists because the current source, I_{OUT}, impresses a voltage on node 30, and this voltage propagates throughout the loop, thus making it possible to measure the gains around the loop. EDN

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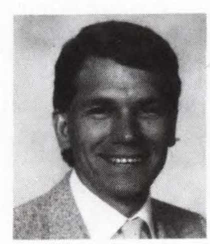
2. Jaycox, Jeffrey M, "CAE tools break barriers of feedback measurement," *Electronic Design*, May 28, 1987, pg 117.
3. "PSpice User's Guide," MicroSim Corp, 23175 La Cadena Dr, Laguna Hills, CA 92635. (Note: MicroSim offers a $10 demo version that will run all the examples shown here and will simulate circuits containing as many as 10 transistors.)
4. Eppler, Bert, "Spice Tricks," *IEEE Circuits and Devices*, July 1987, pg 41.
5. Graeme, Jerald, "FET op amps convert photodiode outputs to usable signals," *EDN*, October 29, 1987, pg 205.

Author's biography



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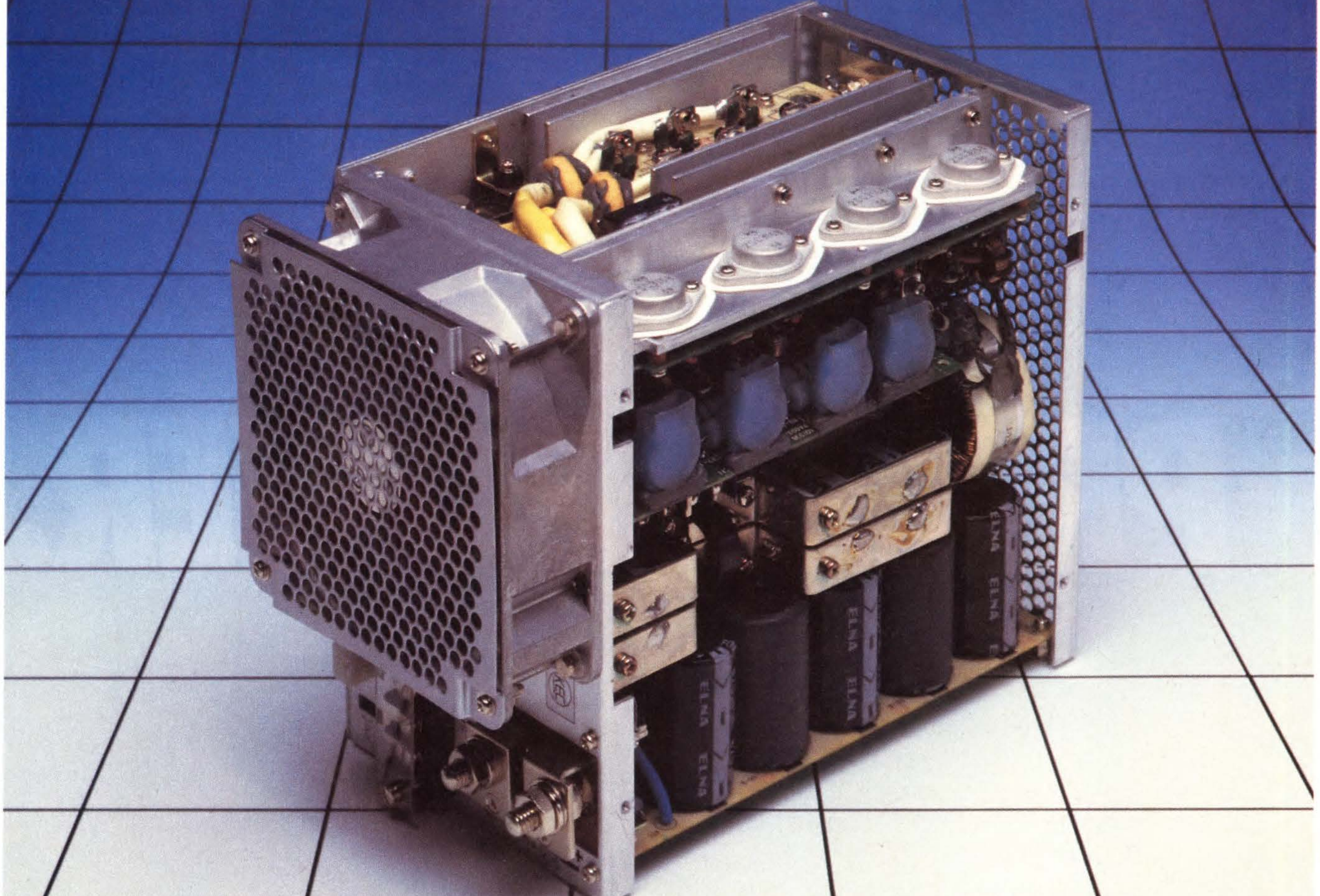

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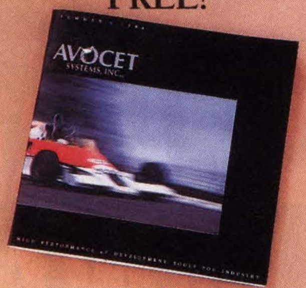

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CIRCLE NO 109

Logic-analyzer interface assists in 68030 program debugging

Real-time program developers can use all the tools they can get. Once you learn how to build a trace-interface circuit for a logic analyzer, you can gain external access to the MC68030's debugging feature and filter out unimportant bus cycles as well.

Don Atkins, *Motorola Inc*

Aids for debugging a program during the development stage are undeniably indispensable. Debugging a real-time program is particularly vexing because you can't stop the program while you evaluate the execution of events. In real-time robotic, automotive, and industrial applications, the target system has to keep operating to determine if the control program in question is functioning properly.

To facilitate program development, Motorola's family of MC68000 μPs include an internal facility that allows you to trace instructions while you debug a program. The MC68030 μP provides additional output pins that give you external access to the internal facility during real-time operation. By decoding the μP's extra outputs and control signals, you can monitor real-time program operation on a logic analyzer.

External tracing lets you examine key parameters while the μP is executing a program. For example, you can detect an instruction boundary, which indicates the end of an instruction cycle during program execution; you can detect if the execution unit is discarding prefetched operations in the pipeline, and you can detect whether read and write accesses are hitting the on-chip cache memories.

To maximize the potential of external tracing, you must fulfill two requirements. First, the external-tracing circuitry must be synchronized to the μP's bus activity. Second, the circuitry must generate a sampling signal that qualifies conditions and eliminates extraneous clock cycles that you don't want or need to analyze.

Tracing takes advantage of μP features

Before you can build a trace-interface circuit, you must understand how the μP performs some of its basic operations. The MC68030 has two modes for transferring data. In the synchronous mode, it has to wait until the device it wants to communicate with sends the $\overline{\text{STERM}}$ (Synchronous Termination) signal, indicating to the μP that the device is ready for data transfer. In the asynchronous mode, the 68030 has to wait till the device responds with the $\overline{\text{DSACK1}}$ or $\overline{\text{DSACK0}}$ signal (or both). To trace data into and out of the μP, both modes must generate a sampling signal when valid data is on the bus.

During program execution, the 68030 prefetches instructions and operands to keep three stages of its

By decoding the µP's control signals and extra outputs, you can monitor the real-time operation of a program on a logic analyzer.

instruction pipeline full. The pipeline allows the execution unit to perform concurrent operations of as many as three words of a single instruction or as many as three consecutive instructions. Instructions predominantly execute sequentially; however, it is possible that the execution unit won't operate on some prefetched data. For example, when a program encounters a change-in-flow instruction, such as a branch, jump, subroutine-call or return statement, the µP must flush the pipeline and refill it with the instructions designated by the change-in-flow statement. These statements cause the µP to assert the $\overline{\text{REFILL}}$ signal, signifying that the instruction pipeline is reloading.

TABLE 1—EFFECTS OF $\overline{\text{STATUS}}$ SIGNAL ASSERTION

IF $\overline{\text{STATUS}}$ IS ASSERTED FOR	THEN
1 CLOCK PERIOD	SEQUENCER IS AT AN INSTRUCTION BOUNDARY AND WILL BEGIN EXECUTION OF NEXT INSTRUCTION
2 CLOCK PERIODS	SEQUENCER IS AT AN INSTRUCTION BOUNDARY BUT WILL NOT BEGIN THE NEXT INSTRUCTION IMMEDIATELY BECAUSE OF EITHER A PENDING TRACE EXCEPTION OR A PENDING INTERRUPT EXCEPTION
3 CLOCK PERIODS	AN MMU ADDRESS-TRANSLATION-CACHE MISS HAS OCCURRED; PROCESSOR WILL BEGIN TABLE SEARCH OR EXCEPTION PROCESSING WILL BEGIN FOR THE FOLLOWING: RESET, BUS ERROR, ADDRESS ERROR, SPURIOUS INTERRUPT, AUTOVECTORED INTERRUPT, OR F-LINE INSTRUCTION (NO COPROCESSOR RESPONDED)
4 OR MORE CLOCK PERIODS	PROCESSOR IS HALTED

The $\overline{\text{STATUS}}$ signal lets you externally trace the progress of the execution unit and certain exceptions as they occur. The external trace circuit ascertains existing conditions by counting the number of clock cycles when a $\overline{\text{STATUS}}$ signal occurs **(Table 1)**.

Cache tracing is hit or miss

Typically, external circuitry is incapable of tracing access operations to a location in the internal cache memory of a µP. However, the MC68030 provides an external address reference to locations in its on-chip cache memory. Because the 68030 implements a write-through policy, you can build a circuit that traces all write operations. If a cache hit occurs on a write cycle, the µP will update both the external device and the location in the on-chip data cache referenced by the lower byte of the address word. If a cache miss occurs

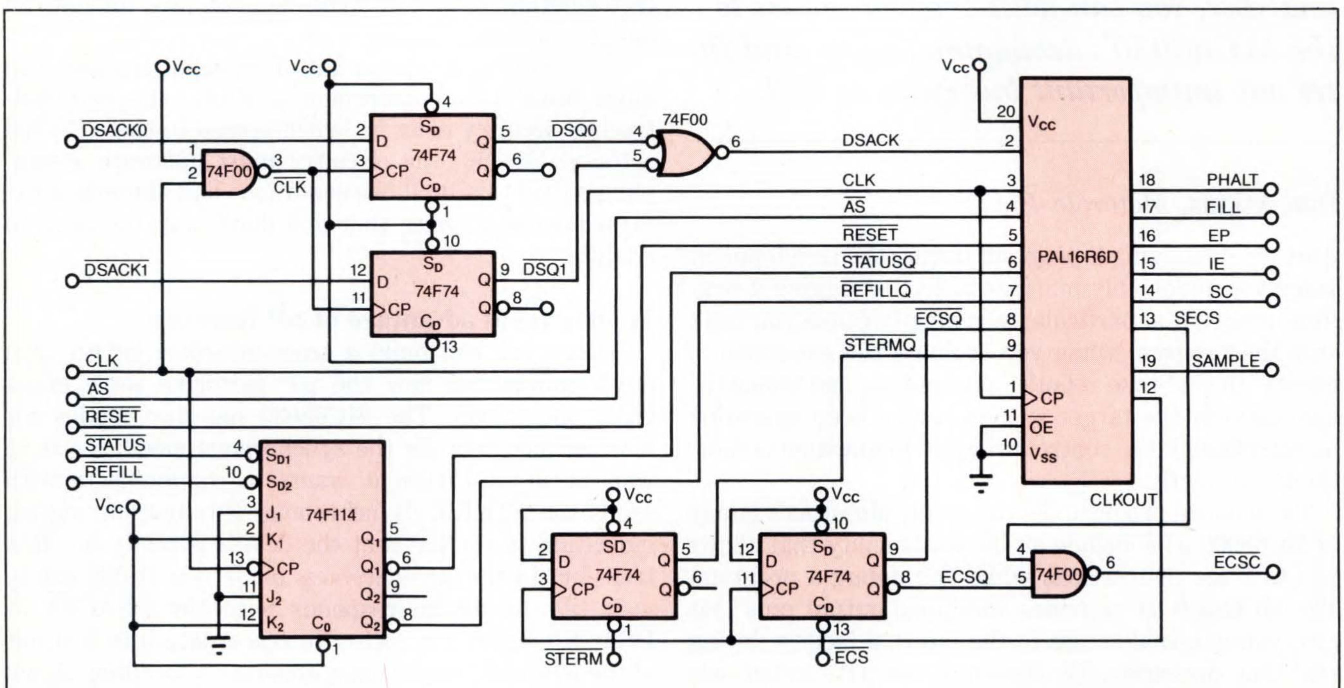


__Fig 1—Developing the qualifying signals__ to externally trace program execution within a 68030 µP and display it on a logic analyzer requires an interface circuit. Fortunately, you can build such a circuit with only a few ICs.

```
THIS DEVICE GENERATES A SAMPLING SIGNAL FOR TRACING
PROCESSOR ACTIVITY ON AN INSTRUCTION LEVEL BASIS FOR THE
MC68030. IN THE PIN DEFINITIONS AND EQUATIONS LISTED
BELOW THE FOLLOWING SYMBOLS ARE USED:

SYMBOL   DEFINITION
  !      LOGICAL NOT
  #      LOGICAL OR
  &      LOGICAL AND
IN ADDITION, THE '.D' EXTENSION ON SIGNAL NAMES REFERS TO
THE 'D' INPUT OF THE INTERNAL PAL FLIP-FLOP.

/** INPUTS *
PIN 1   = CLK      ;  SAME AS PIN 3 CLK
PIN 2   = DSACK    ;  DATA STROBE ACKNOWLEDGE
PIN 3   = CLK      ;  MPU CLOCK SIGNAL
PIN 4   = !AS      ;  ADDRESS STROBE
PIN 5   = !RESET   ;  SYSTEM RESET SIGNAL
PIN 6   = !STATUSQ ;  LATCHED STATUS SIGNAL
PIN 7   = !REFILLQ ;  LATCHED REFILL SIGNAL
PIN 8   = !ECSQ    ;  LATCHED ECS SIGNAL
PIN 9   = !STERMQ  ;  LATCHED STERM SIGNAL

/** OUTPUTS **/
PIN 19  = SAMPLE   ;  SAMPLE SIGNAL
PIN 18  = PHALT    ;  PROCESSOR HALTED
PIN 17  = FILL     ;  REFILL RECEIVED
PIN 16  = EP       ;  EXCEPTION PENDING
PIN 15  = IE       ;  INSTRUCTION EXECUTED
PIN 14  = SC       ;  STATUS COMPLETE
PIN 13  = SECS     ;  SAMPLED ECS SIGNAL
PIN 12  = CLKOUT   ;  DELAYED CLK SIGNAL
(a)
```

```
/** INTERMEDIATE EQUATIONS *              STATE = PHALT SC EP IE
   S0 = !PHALT & !SC & !EP & !IE;          0    =  0    0  0  0
   S1 = !PHALT & !SC & !EP &  IE;          1    =  0    0  0  1
   S2 = !PHALT & !SC &  EP &  IE;          2    =  0    0  1  1
   S3 = !PHALT & !SC &  EP & !IE;          3    =  0    0  1  0
   S4 =  PHALT &  SC &  EP &  IE;          4    =  1    1  1  1
   S5 = !PHALT &  SC & !EP &  IE;          5    =  0    1  0  1
   S6 = !PHALT &  SC &  EP &  IE;          6    =  0    1  1  1
   S7 = !PHALT &  SC &  EP & !IE;          7    =  0    1  1  0

/** LOGIC EQUATIONS **/
!SAMPLE =  !SC & !AS & !SECS #
           !SC & !DSACK & !STERMQ & !SECS #
           !SC & AS & !DSACK & !STERMQ & SECS;

!PHALT.D = !STATUSQ # !EP # IE # RESET;

!SC.D =    RESET #
           S0 # S1 &  STATUSQ #
           S2 &  STATUSQ #
           S4 & !STATUSQ #
           SC & !PHALT;

!EP.D =    RESET #
           S0 # S1 & !STATUSQ #
           S4 & !STATUSQ #
           SC & !PHALT;

!IE.D =    RESET #
           S0 & !STATUSQ #
           S2 &  STATUSQ #
           S3 & !STATUSQ #
           SC & !STATUS;

!SECS.D =  !ECSQ;

!CLKOUT =  !CLK;

!FILL.D =  !REFILLQ & SAMPLE #
           !FILL & !REFILLQ #
           RESET;

(b)
```

*Fig 2—The PAL16R6D logic device uses these defined input and output signals for its internal logic functions (**a**). You can use the accompanying logic equations (**b**) to program the PAL for the trace-interface circuit.*

on a write cycle, only the external device will be updated and no data will be entered into the data cache memory. If a hit occurs on a read cycle, the lower byte of the address word will provide an address reference to the location in the on-chip cache memory.

When the MC68030 wishes to transfer data to an external location, it places that particular address on the address bus and drives the $\overline{\text{ECS}}$ (External Cycle Start) signal low on the rising edge of the clock signal. If a hit occurs in one of the two internal cache memories or in the cache holding register, the μP will abort the external-transfer cycle. During the transfer operation, the least significant byte on the address bus serves as the reference for where the hit occurred in the on-chip cache memory.

If no hit occurs, the μP will assert the $\overline{\text{AS}}$ (Address Strobe) signal to validate the address before the next rising edge of the clock signal. The on-chip MMU (memory management unit) translates its virtual address to an external physical address. The MMU does not use the least significant byte (A_0 through A_7) in the translation process.

Fig 1 shows the hardware required to decode the signals from the 68030 so that you can debug a real-time program on a logic analyzer. All of the nine input signals, $\overline{\text{DSACK0}}$, $\overline{\text{DSACK1}}$, CLK, $\overline{\text{AS}}$, $\overline{\text{RESET}}$, $\overline{\text{STATUS}}$, $\overline{\text{REFILL}}$, $\overline{\text{STERM}}$, and $\overline{\text{ECS}}$, attach to the 68030 μP in the system under development. The interface generates six output signals, PHALT, FILL, EP, IE, SAMPLE, and $\overline{\text{ECSC}}$, to aid in capturing and analyzing real-time data. (A seventh output signal, SC, or Status Complete, is only used to generate state diagrams.) The logic analyzer connects to these signals to qualify information on the address and data bus. The system's CLK signal externally clocks the logic analyzer for synchronization. The logic analyzer captures the data on the falling edge of the CLK signal when the SAMPLE signal is high.

A PLD does most of the tracing

It is the programmable logic device (in this case the PAL16R6D) that generates the qualifying signals for logic analysis. **Fig 2a** defines the signals available on the pins of the PAL, and **Fig 2b** lists the PAL logic equations. **Fig 3** is a state-machine diagram for the PAL.

Any one of the following five conditions will cause the interface hardware to assert the SAMPLE signal.

1. The beginning of an external bus cycle, indicated by the assertion of the $\overline{\text{ECS}}$ command.

The trace-interface circuit generates a sampling signal to qualify the events and eliminate extraneous clock cycles.

2. A hit in the internal cache or cache holding register, indicated by the assertion of the $\overline{ESC}$ signal and without the $\overline{AS}$ command being asserted before the next clock cycle.

3. The encountering of an instruction boundary by the μP's microsequencer.

4. The processing of an exception by the μP.

5. The occurrence of a double bus-fault, which automatically halts the μP.

The $\overline{PHALT}$ signal indicates a double fault on the system bus and signifies that the μP requires a reset signal to continue operation. The interface asserts the $\overline{PHALT}$ signal when the μP sets the $\overline{STATUS}$ signal for more than three cycles. The $\overline{PHALT}$ signal generates a SAMPLE signal.

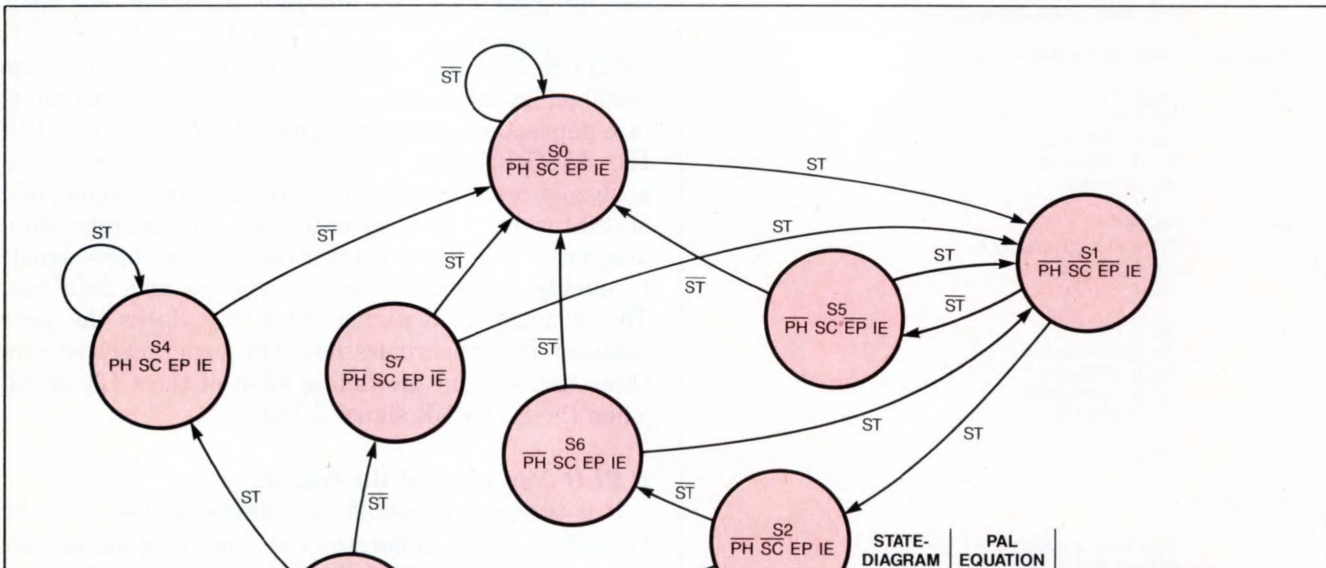
The FILL signal indicates a break in the sequential execution of the program instructions. Actually, the FILL signal is a latched $\overline{REFILL}$ signal from the μP. It remains latched until the assertion of the next SAMPLE signal. The assertion of the FILL signal does not generate a SAMPLE signal.

The EP (Exception Pending) signal indicates that the MC68030 is beginning exception processing for either a reset, bus error, address error, spurious interrupt, autovectored interrupt, F-line instruction, MMU address translation cache miss, or external trace. The EP signal asserts itself if the STATUS signal negates after two or three clock cycles. The assertion of EP generates a SAMPLE signal.

The IE (Instruction Executed) signal indicates the completion of an instruction by the μP's execution unit. The μP asserts the $\overline{STATUS}$ signal for one clock period every time the execution unit finishes executing an instruction. The trace-interface circuitry detects this condition and issues the IE signal. The assertion of the IE signal also generates a SAMPLE signal.

The trace-interface circuit uses the SECS (Sampled ECS) signal generated by the PAL and the latched $\overline{ECS}$ (ECSQ) signal to derive the $\overline{ECSC}$ (External Cycle Start Condition) signal. The $\overline{ECSC}$ command, in conjunction with the $\overline{AS}$ signal, determines if the address bus and data bus are valid for the current SAMPLE signal. **Table 2** lists which bits are valid for the possible combinations of conditions for the $\overline{AS}$ and $\overline{ECSC}$ signals. The assertion of the $\overline{ECSC}$ signal does not generate a SAMPLE signal.

Although logic analysis is possible without a trace-interface circuit, it is difficult because you have to weed



STATE-DIAGRAM SYMBOL	PAL EQUATION SYMBOL	DEFINITION
PH	PHALT	PROCESSOR HALTED
SC	SC	STATUS COMPLETE
EP	EP	EXCEPTION PENDING
IE	IE	INSTRUCTION EXECUTED
ST	STATUSQ	LATCHED STATUS SIGNAL

***Fig 3—This state-machine diagram** elucidates the logic equations of **Fig 2b**. The state of the latched STATUS signal (ST) determines which state transition occurs on each rising clock edge.*

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If a hit occurs on a read cycle, the lower byte of the address word will provide an address reference to the location in the on-chip cache memory.

TABLE 2—EFFECTS OF $\overline{AS}$ and $\overline{ECSC}$ SIGNAL ASSERTION

$\overline{AS}$	$\overline{ECSC}$	EFFECT
0	0	BOTH ADDRESS AND DATA BUS ARE VALID
0	1	BOTH ADDRESS AND DATA BUS ARE VALID
1	0	ADDRESS BITS (A_7-A_0) ARE VALID ADDRESS BITS (A_{31}-A_8) ARE INVALID DATA BUS IS INVALID
1	1	BOTH ADDRESS AND DATA BUS ARE INVALID

through so much data. The trace-interface circuit filters out the "noninteresting" clock cycles so that the logic analyzer displays only the cycles important for debugging. **Listing 1,** a logic-state listing, uses the trace-interface circuit to generate a display for a logic analyzer. In this example, 25 samples display a function that copies a source string to a destination string until the function encounters either a null character or a hexadecimal 0. Without a trace-interface circuit, 99 samples show up when the logic analyzer takes a sample on every falling edge of the system clock. Because the extra 74 cycles occur when there is no external bus activity or when no instruction-execution information is provided by the $\overline{STATUS}$ and $\overline{REFILL}$ signals, they are not relevant to program debugging. **EDN**

Author's biography

Don Atkins is an applications design engineer for Motorola's high-end-µP semiconductor-products sector (Austin, TX). His duties includes application support for the M68000 and M88000 µPs. He received a BSEE degree in 1982 from the University of Illinois. In his spare time, Don enjoys boating and waterskiing with his wife and two children.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

LISTING 1—TRACE-INTERFACE-CIRCUIT LOGIC-STATE PROGRAM

Index	Address	Data	$\overline{AS}$	PHALT	FILL	EP	IE	$\overline{ECSC}$	Comments
									Burst Read Prefetch
0	80000030	206F0004	0	0	0	0	0	1	move.l $4(sp),a0
1	80000030	226F0008	0	0	0	0	0	1	move.l $8(sp),a1
2	80000030	10D966FC	0	0	0	0	0	1	move.b (a1)+,(a0)+ bne.b $-4
3	80000030	206F0004	0	0	0	0	0	1	move.l $4(sp),a0
4	800020F8	FFFFFFFF	1	0	0	0	1	1	Instruction Executed
5	800020F8	80001100	0	0	0	0	0	1	Memory Write
6	800020F8	FFFFFFFF	1	0	0	0	1	1	Instruction Executed
7	80001100	30313233	0	0	0	0	0	1	Burst Operand Read
8	80001100	34353600	0	0	0	0	0	1	Burst Operand Read
9	80001100	00000000	0	0	0	0	0	1	Burst Operand Read
10	80001100	00000000	0	0	0	0	1	1	Instruction Executed
11	00003200	00000000	0	0	0	0	0	1	Byte Read
12	00003201	00000000	0	0	0	0	0	1	Byte Read
13	00003202	00000000	0	0	0	0	0	1	Byte Read
14	00003203	00FFFFFF	0	0	0	0	0	1	Byte Read
15	80001100	00000000	0	0	0	0	1	1	Instruction Executed
16	80001100	FFFFFFFF	1	0	0	0	1	1	Instruction Executed
17	80000040	FFFFFFFF	1	0	0	0	1	1	Instruction Executed
18	80000040	20084E75	0	0	0	0	0	1	move.l a0,d0
19	80000040	FFFFFFFF	0	0	0	0	0	1	rts
20	80000040	FFFFFFFF	0	0	0	0	0	1	------
21	80000040	FFFFFFFF	0	0	0	0	0	1	------
22	80000044	FFFFFFFF	1	0	0	0	1	1	Instruction Executed
23	80000044	FFFFFFFF	1	0	0	0	1	1	Instruction Executed
24	80000044	FFFFFFFF	1	0	0	0	1	1	Instruction Executed

DESIGN NOTES

Number 15 in a series from Linear Technology Corporation September, 1988

Noise Calculations in Op Amp Circuits

Alan Rich

Noise calculations in op amp circuits are one of the most confused calculations that an analog engineer must perform.

One cannot just look at noise specifications; the total op amp circuit including resistors and operating frequency range must be included in calculations for circuit noise. A "low" noise amplifier in one circuit will become a "high" noise amplifier in another circuit.

As a part of this Design Note, an IBM-PC or compatible computer program, NOISE, has been written to perform the noise calculations. This program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate circuit noise using noise specs for any op amp. At the end of this Design Note there are detailed operating instructions for the computer program NOISE.

To calculate noise for an op amp circuit, one must consider the op amp voltage and current noise density and 1/f corner frequency, the frequency range of interest, and the resistor noise.

The most comprehensive specification for voltage or current noise is the noise density frequency response curve as shown in Figure 1.

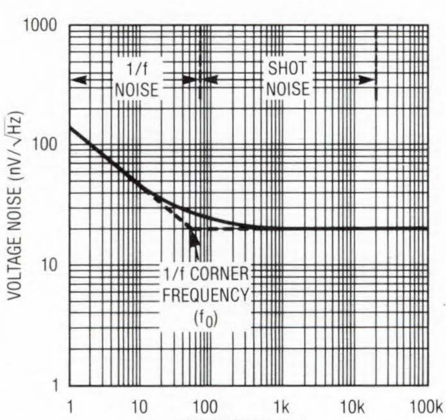

Figure 1.

There are two distinct regions to consider:

1. The high frequency part of the curve shows the shot noise and is independent of frequency.
2. The low frequency part of the curve is the 1/f noise as shown by a rapidly increasing noise density. In low frequency applications, the 1/f noise limits the minimum level of noise. The point on the curve where the asymptotes of the shot noise and 1/f noise intersect is the 1/f corner frequency.

To calculate the total RMS noise of an op amp over a bandwidth:

$$N = NO \times \sqrt{FC \times LN\,(FH/FL) + (FH - FL)} \qquad \text{(Equation 1)}$$

Where N is the RMS current or voltage noise measured from a lower frequency FL to an upper frequency FH and NO is the current or voltage shot noise density with a 1/f corner frequency FC.

Consider an audio preamplifier using an LT1037 as a simple inverting circuit (Figure 2) and the corresponding noise model (Figure 3).

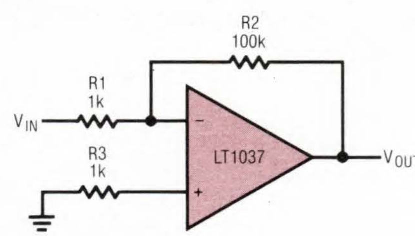

Figure 2.

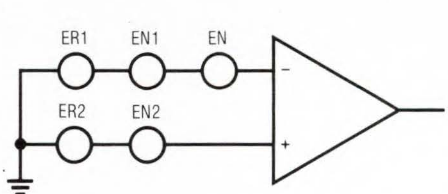

Figure 3. Noise Model

EN is the voltage noise of the op amp, EN1 is the voltage noise developed by the current noise in resistors R1 and R2, EN2 is the voltage noise developed by the current noise in resistor R3, ER1 is the voltage noise of R1 and R2, and ER2 is the voltage noise of R3.

Since we are using an LT1037 over the audio frequency range, $NO = 2.5nV/\sqrt{Hz}$, $FC = 2.0Hz$, $FH = 20kHz$, $FL = 20Hz$. Plugging into Equation 1:

$$EN = 2.5 \times \sqrt{2 \times LN\,(20kHz/20Hz) + (20kHz - 20Hz)}$$
$$EN = 354nV, RMS$$

To calculate EN1, first the current noise must be calculated using Equation 1 and a current noise density of $0.57pA/\sqrt{Hz}$ and 1/f corner frequency of 120Hz.

$$IN = 0.57 \times \sqrt{120 \times LN\,(20kHz/20Hz) + (20kHz - 20Hz)}$$
$$IN = 82pA, RMS$$

IN will flow into the parallel combination of R1 and R2.

$$EN1 = 82pA \times 1k \,||\, 100k = 82nV, RMS$$

Similarly, EN2 results from IN flowing in R3.

$$EN2 = 82pA \times 1k = 82nV, RMS$$

The voltage noise of the resistors must be calculated next. In general, resistor noise is given by:

$$ER = \sqrt{4 \times K \times T \times R \times (FH - FL)}$$

Where K is Boltzman's Constant, 1.39×10^{-23}, T is temperature (K), R is the resistor value, FH is the upper frequency, and FL is the lower frequency of interest.

At 25°C, this equation reduces to:

$$ER = \sqrt{R \times (FH - FL)} \times 1.28 \times 10^{-10}$$

To calculate ER1 we must consider R1 in parallel with R2,

$$ER1 = \sqrt{(1k \,||\, 100k) \times (20kHz - 20Hz)} \times 1.28 \times 10^{-10}$$
$$ER1 = 570nV, RMS$$

Similarly, to calculate ER2,

$$ER2 = \sqrt{1k \times (20kHz - 20Hz)} \times 1.28 \times 10^{-10}$$
$$ER2 = 570nV, RMS$$

To calculate the total noise of the audio preamplifier using an LT1037, the RMS sum of the individual terms must be calculated.

$$TOTAL\ NOISE = \sqrt{EN^2 + EN1^2 + EN2^2 + ER1^2 + ER2^2}$$
$$TOTAL\ NOISE = \sqrt{353^2 + 80^2 + 80^2 + 570^2 + 570^2} = 880nV, RMS$$

To calculate p-p noise, multiply the RMS noise times 6; the total peak-to-peak noise is $5.3\mu V$ for this preamplifier.

It is important to realize this noise is referred to the input of the circuit; to obtain the output noise level, the input noise must be multiplied by the noise gain which can be different from the circuit gain:

$$OUTPUT\ NOISE = TOTAL\ NOISE \times NOISE\ GAIN$$
$$OUTPUT\ NOISE = 880nV \times 101 = 89\mu V, RMS \text{ or } 534\mu V, \text{peak-to-peak}$$

It should be noted that design techniques to optimize DC performance will frequently result in higher noise. For example, to minimize DC errors, a balance resistor is often placed in the + Input of an op amp to compensate for an error voltage created by bias current flowing in gain setting resistors connected to the – Input. This resistor will increase the output noise since op amp noise current must flow through the resistor, and thus create a voltage noise generator. For minimum noise levels, the resistor in the + Input should be 0Ω. As a side note, for precision op amps (LT1001, LT1007, OP07) that employ bias current cancellation techniques, this resistor should be 0Ω to minimize DC errors since the bias current equals the offset current.

Instructions for Operating NOISE

NOISE is a general purpose computer program to calculate noise in op amp circuits. It will run on any IBM-PC compatible computer with a direct call from DOS.

Noise specifications and data for Linear Technology op amps (LT10XX) are contained in the program's data file. All noise specifications are based on typical specifications at 25°C.

To operate NOISE:

1. Boot the system with DOS and wait for DOS prompt "A>".
2. Insert the NOISE.EXE program disk into the A disk drive.
3. Type "NOISE" and <return>.

Operation in NOISE is menu driven throughout the program with default values on all parameters initially.

Best Op Amp for Lowest Noise vs Source Resistance

SOURCE R (R_{eq})	BEST OP AMP @ LOW FREQ. (10Hz)	BEST OP AMP @ WIDEBAND (1kHz)
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400Ω to 1k	LT1007/37	LT1028
1k to 4k	LT1007/37	LT1028, LT1007/37
4k to 15k	LT1001	LT1007/37
15k to 30k	LT1001	LT1001, LT1007/37
30k to 70k	LT1001, LT1012	LT1001
70k to 150k	LT1012	LT1001, LT1012 LT1055/56/22, LT1057/58
150k to 600k	LT1012, LT1006/13/14	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
600k to 2M	LT1012 LT1055/56/22, LT1057/58	LT1012, LT1006/13/14 LT1055/56/22, LT1057/58
2M to 10M	LT1055/56/22, LT1057/58	LT1012 LT1055/56/22, LT1057/58
>10M	LT1055/56/22, LT1057/58	LT1055/56/22, LT1057/58

For literature on low noise op amps, or a 5 1/4" "NOISE" disk, call **800-637-5545**. For applications help, call (408) 432-1900, Ext. 361.

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IM/GP 988 165K

EDITED BY CHARLES H SMALL

Program sets up multiplexer as logic chip

Jozef Kalisz
WAT, Warsaw, Poland

Although you can use a multiplexer having *n* address inputs and 2^n data inputs to realize any arbitrary logic function of n+1 variables, pencil-and-paper methods for assigning input-data signals to the multiplexer's address inputs are tediously iterative and error-prone. The short Turbo Pascal program in **Listing 1** automatically generates all possible assignments. From among them, you can select the optimal assignment. **Listing 1** handles three variables, and you can easily extend it to handle four or five.

Finding optimal assignments involves first developing a total of n+1 address assignments. These address assignments involve all possible combinations of the four signals you can route to each address input of the multiplexer—0, 1, x_i, or x_i (where x_i is one of the input variables)—that result in the desired logical output from the multiplexer. As a rule, you need an inverter for each input-data variable to obtain its complement. In some cases, however, you can eliminate inverters

LISTING 1

```
program Mux4;
  { Generates connections of an 8-input multiplexer to realize
    any arbitrary switching function of four variables  }
uses Crt;
var      t, v  :  set of 0..15;
            u  :  string[2];
      m, n, l  :  integer;
begin
  ClrScr;  GotoXY(3, 8);
  t := [];
  Writeln('Enter elements of the set Σ : ');
  Writeln;
  repeat
    Readln(u);
    Val(u, m, n);
    if n = 0 then t := t + [m];
  until n > 0;
  ClrScr; TextColor(Black); TextBackground(White);
  Write('Elements of the set Σ :  ');
  for m:= 0 to 15 do
    if m in t then Write(m, '  ');
  Writeln; Writeln; TextColor(White); TextBackground(Black);
  for l := 1 to 4 do
  begin
    case l of
      1:  Write('          Design #1: A0-x0, A1-x1, A2-x2');
      2:  Write('          Design #2: A0-x3, A1-x0, A2-x1');
      3:  Write('          Design #3: A0-x2, A1-x3, A2-x0');
      4:  Write('          Design #4: A0-x1, A1-x2, A2-x3');
    end;    Writeln;
    for m := 0 to 7 do
    begin
      if (m in t) and (m + 8 in t) then
      Write('d', m, ' = 1  ') else
      if m in t then Write('d', m, ' = INV(x', 4 - l, ')  ')
    end;  Writeln;
    for m := 8 to 15 do
      if (m in t) and not(m - 8 in t) then
      Write('d', m - 8, ' = x', 4 - l, '  ');
    Writeln;
    Writeln('All remaining data inputs should be set to 0');
    Writeln;
    v := [];
    for n := 0 to 15 do
      if n in t then
        if n < 8 then v := v + [n shl 1]
        else v := v + [(n shl 1) - 15];
    t := v
  end
end.
```

LISTING 2

```
Elements of the set Σ :  0  2  5  7  10

        Design #1: A0-x0, A1-x1, A2-x2
d0 = INV(x3)  d2 = 1  d5 = INV(x3)  d7 = INV(x3)

All remaining data inputs should be set to 0

        Design #2: A0-x3, A1-x0, A2-x1
d0 = INV(x2)  d4 = INV(x2)  d5 = INV(x2)
d2 = x2  d6 = x2
All remaining data inputs should be set to 0

        Design #3: A0-x2, A1-x3, A2-x0
d0 = 1  d5 = 1
d2 = x1
All remaining data inputs should be set to 0

        Design #4: A0-x1, A1-x2, A2-x3
d0 = INV(x0)  d1 = INV(x0)  d5 = INV(x0)
d2 = x0  d3 = x0
All remaining data inputs should be set to 0


Press any key to return to Turbo Pascal
```

by assigning the input data to the multiplexer's address inputs judiciously. An optimal assignment, therefore, uses the fewest inverters.

To use the program in the **Listing,** first specify your logic function in canonical minterm format and then translate the minterms into decimal numbers. For example, the Boolean function

$$f = x_3\bar{x}_2\bar{x}_1x_0 + x_3\bar{x}_2x_1 + x_2\bar{x}_1x_0 + x_2\bar{x}_1x_0.$$

In canonical form is

$$f = x_3\bar{x}_2\bar{x}_1x_0 + x_3\bar{x}_2x_1\bar{x}_0 + x_3\bar{x}_2x_1x_0 + \bar{x}_3x_2\bar{x}_1x_0 + x_3x_2\bar{x}_1x_0.$$

You can represent these minterms as a set of binary numbers—B = (1001, 1010, 1011, 0101, 1101)—or as a set of decimal equivalents—Σ = (9, 10, 11, 5, 13).

Enter the set of decimal numbers corresponding to your function's minterms when the program prompts you for it. The program will then print out all possible input assignments for the multiplexer's address pins that result in valid outputs. You then simply select the assignment that uses the fewest inverters. **Listing 2** shows the results for the set Σ = (0, 2, 5, 7, 10). Note that assignment 3 uses no inverters. **EDN**

To Vote For This Design, Circle No 746

Turbo circuit ensures glitch-free switch

Wayne Jeong
Eaton Corp, Ion Beam Systems Div, Austin, TX

The simple circuit in **Fig 1** generates a dual-speed clock for personal computers. The circuit synchronizes your asynchronous switch inputs with the master clock to provide glitch-free transitions from one clock speed to the other. The dual-speed clock allows some programs to run at the higher clock speed in order to execute more quickly. Other programs—for example, programs that use loops for timing,— can still run at the lower speed as necessary. The circuit will work with any master-clock frequency that meets the flip-flops' minimum-pulse-width specs.

Two D flip-flops (IC_1 and IC_2) and an XOR gate (IC_3) form a binary divider that develops the 6- and 12-MHz clocks. When the NT signal is low, the reset pin forces the 6-MHz output low. On the other hand,

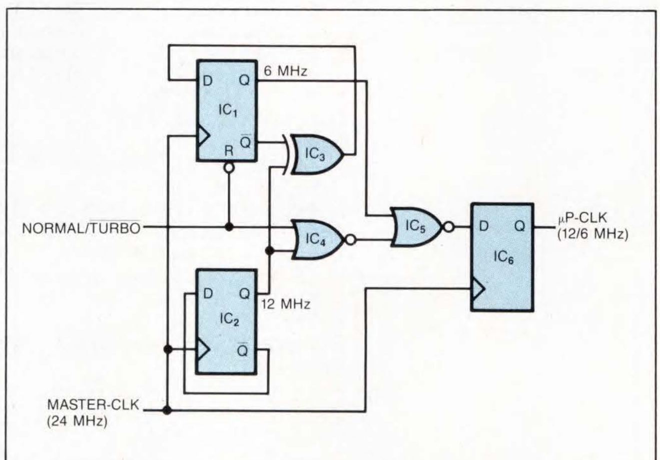

Fig 1—This binary divider generates *a dual-speed clock for personal computers and synchronizes your asynchronous switch inputs with the master clock to provide glitch-free transitions from one speed to the other.*

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when the NT signal is high, IC_3 blocks the 12-MHz output. Therefore, only one of the two clock signals passes through IC_3 and gets clocked into IC_6. Because the MASTER-CLK signal clocks IC_6, asynchronous switching of the NT signal can't generate an output pulse shorter than 41 μsec (1/24 MHz). Also, the synchronization eliminates glitches. EDN

To Vote For This Design, Circle No 749

Simple calculation finds probabilities

Charles Capps
Delco, Goleta, CA

You don't need a computer to solve problems involving the reliability of complex systems. Using a simple, 4-function calculator, you can solve two classes of problems: First, given the reliability of individual subsystems, you can determine the overall reliability of a system; and second, you can determine the number of subsystems you need to achieve a certain level of reliability.

The difficulty of obtaining an exact solution for these problems increases nonlinearly as the number of parts in a circuit, or circuits in a system, increases. But following a simple algorithm yields a good approximation.

First, assuming you can get reliability figures for each component on a pc board, or subsystem in a system, arrange the probabilities in a horizontal, 1-dimensional vector array, A(N), where N is the number of components or subsystems.

Next, construct a 2-dimensional array, $B(2^N-1, N)$. Load this array with binary numbers beginning with 0 and ascending in sequence to 2^N-1. Then, for each row of B, perform the following transformation. If $b_{i,j}$ is a 0, replace the 0 with $1-a_j$; if $b_{i,j}$ is a 1, replace it with a_j. Then multiply all the numbers of each row together and place the results in a vertical vector C(N). Adding up the elements of C(N) that correspond to the rows of B that have the same total numbers of ones (or zeros) yields all the possible combinations of probability of success or failure.

For example, suppose an airplane carries three navigational computers. Two have a probability of 0.65 of successfully guiding the airplane from one airport to the next; the third has a probability of 0.75. What is the probability that the airplane will arrive at its destination and what are the probabilities that only one computer, or perhaps two computers, will fail?

$$P_1=0.65=a_1,\ P_2=0.65=a_2,\ P_3=0.75=a_3,\ N=3.$$

$$\therefore A(N)=[0.65,\ 0.65,\ 0.75].$$

$$B(2^N-1, N)=\begin{bmatrix}0&0&0\\0&0&1\\0&1&0\\0&1&1\\1&0&0\\1&0&1\\1&1&0\\1&1&1\end{bmatrix}=\begin{bmatrix}0.35&0.35&0.25\\0.35&0.35&0.75\\0.35&0.65&0.25\\0.35&0.65&0.75\\0.65&0.35&0.25\\0.65&0.35&0.75\\0.65&0.65&0.25\\0.65&0.65&0.75\end{bmatrix}$$

$$C(N)\cong\begin{bmatrix}0.031\\0.092\\0.057\\0.171\\0.057\\0.171\\0.106\\0.317\end{bmatrix}$$

Fig 1—In this example of the composite-reliability algorithm, *you first place the reliability of each of three subsystems into the horizontal vector, A. Next, you transform the 2-dimensional, binary-loaded vector, B, row-by-row according to the entries in A. Then you multiply all the entires of each row of B together to form the vertical vector, C. Summing related rows of C yields approximations of the probabilities associated with all possible combinations of success and failure.*

Fig 1 shows the steps in the algorithm. From the vertical vector, C(N), you can see that the probability that all computers might fail is 0.031. Adding rows 4, 5, and 6 of C(N) (rows correspnding to the rows of B having only one 0) yields a probability of 0.448 that just one computer will fail. Similar sums indicate that a probability of 0.206 that two computers will fail and 0.317 that no computer will fail. EDN

To Vote For This Design, Circle No 748

One-shots tame tone decoder

V Lakshminarayanan
Centre for Development of Telematics, Bangalore, India

Adding a pair of one-shots to the output of a 567 tone decoder renders it less sensitive to out-of-band signals and noise. Without the one-shots, the 567 is prone to spurious output chatter. Other protection schemes, such as feeding back outputs or using an input filter, do not work as well as the one-shots.

In **Fig 1**'s circuit, the output of the 567 is high in the absence of a tone and becomes low when it detects a tone. The tone decoder triggers a one-shot via an AND gate. The one-shot's period is set to slightly less than the duration of a tone burst. When the output of the tone decoder goes low, it triggers the second one-shot. The second one-shot's period is set to slightly less than the interval between tone bursts. The flip-flop enables and disables the inputs to one-shots such that spurious outputs from the tone decoder do not affect the output. EDN

To Vote For This Design, Circle No 750

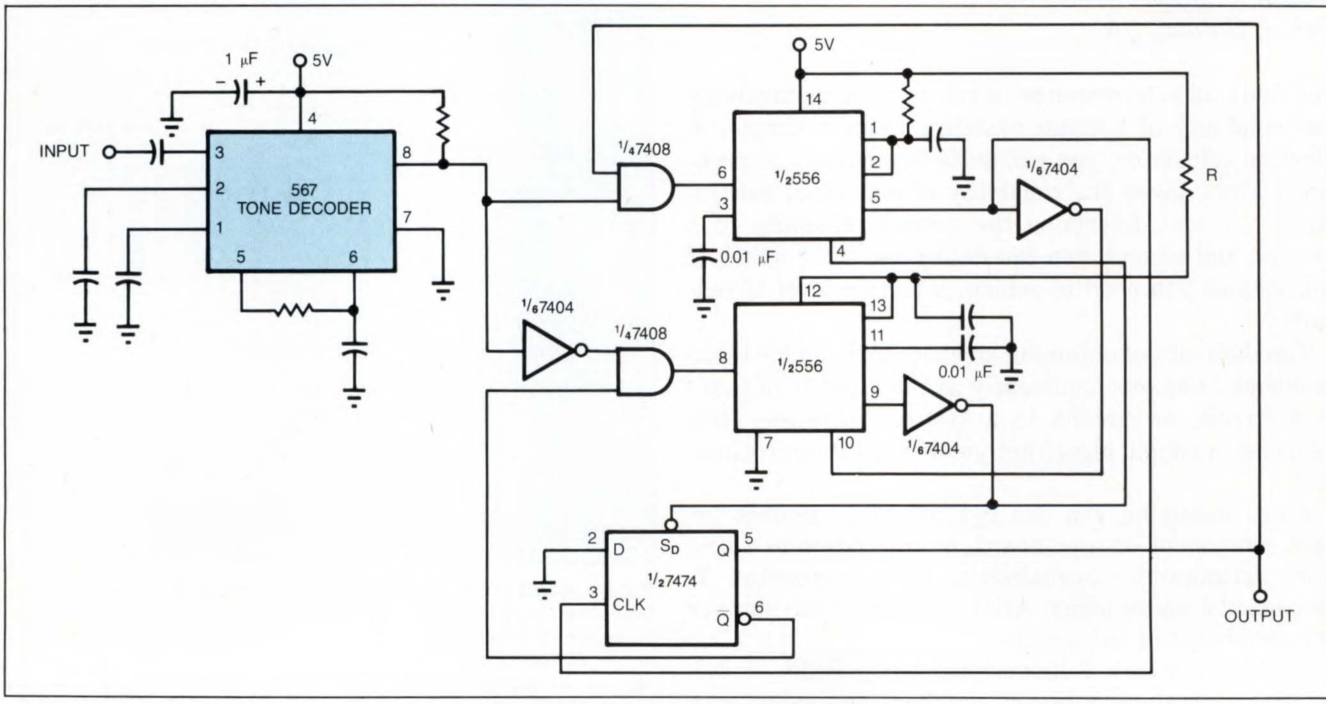

Fig 1—A pair of one-shots and an arbitration flip-flop *filter spurious transitions from the output of the 567 tone decoder.*

Software timer adapts to clock speed

Gerald L Kmetz
National Semiconductor Corp, Santa Clara, CA

You can use the C-language functions in **Listing 1** to build a software timer for IBM PC applications. The timer offers 1-msec resolution, and it automatically calibrates itself despite variations in both clock speed of different PCs (or PC clones) and the different execution speeds of run-time versions of these functions as compiled by different compilers.

Functions calibrate() and getcount() adapt the timer to different clock frequencies and execution speeds. You should call calibrate() before initializing any program that uses the timer function call. This calibration function determines the value of the global variable Control, which provides the key to accurate timing.

Function calibrate() first seeds Control with a value that's appropriate for 4.77-MHz computers, and then adjusts this value by measuring the elapsed real-time counter (RTC) value. Function getcount() returns the RTC's value before and after calling function timer(). The RTC updates about 18.2 times per second. Therefore, the calibration routine uses a 1099-msec calibration interval which works out to 20 counts of the RTC.

When you compile and run the calibration routine, it will report the RTC count and the calculated value for the variable Control. You should then edit this value for Control into your source files for future use. The counter is accurate to about 5% (one count in 20).

To use the timer in your application programs, set the global variable Time to the desired delay in milliseconds and then call the function timer(). The delay range is 1 through 655,536 msec. EDN

To Vote For This Design, Circle No 747

LISTING 1

```
/* test.c: self-calibrating software timer */

#include <math.h>

unsigned int Time, Control;

/* the following function main() is not part of the timer; it's */
/* a program to test and optionally fine-tune the timer */
#define TEST
void main(void)
{
     extern void calibrate();
     calibrate;
}

/* calibrate timer for different clock speeds and compilers */
/* calibrate should be called when initializing the program */
void calibrate(void)
{
     extern void timer();
     long start, stop, diff, getcount();

     do {
          Time = 1099;            /* value to delay 1099 msec */
          Control = 142;          /* initial seed value */
          start = getcount();     /* read RTC count at start */
          timer();                /* trial delay of 1099 msec */
          stop = getcount();      /* read RTC count at finish */
          diff = stop - start;    /* get elapsed RTC count */
     } while (diff < 0);          /* avoid spanning 12am problem */
     Control = (int)((20.0 * (float)Control / (float)diff) + 0.5);
#ifdef TEST
     printf("elapsed count = %ld\tControl = %d\n", diff, Control);
#endif
}

/* get count from RTC counter */
long getcount(void)
{
     unsigned lowerword, upperword;

     int segment = 0x0040;
     unsigned offset = 0x006c;

     lowerword = peek(segment, offset);
     upperword = peek(segment, offset + 2);
     return(((long)upperword << 16) | lowerword);
}
/* delay one millisecond and return */
void delay1ms(void)
{
     int i;

     for (i = Control; i; i--)
          continue;
}

/* delay (Time) milliseconds and return */
void timer(void)
{
     long i;

     for (i = Time; i; i--)
          delay1ms();
}
```


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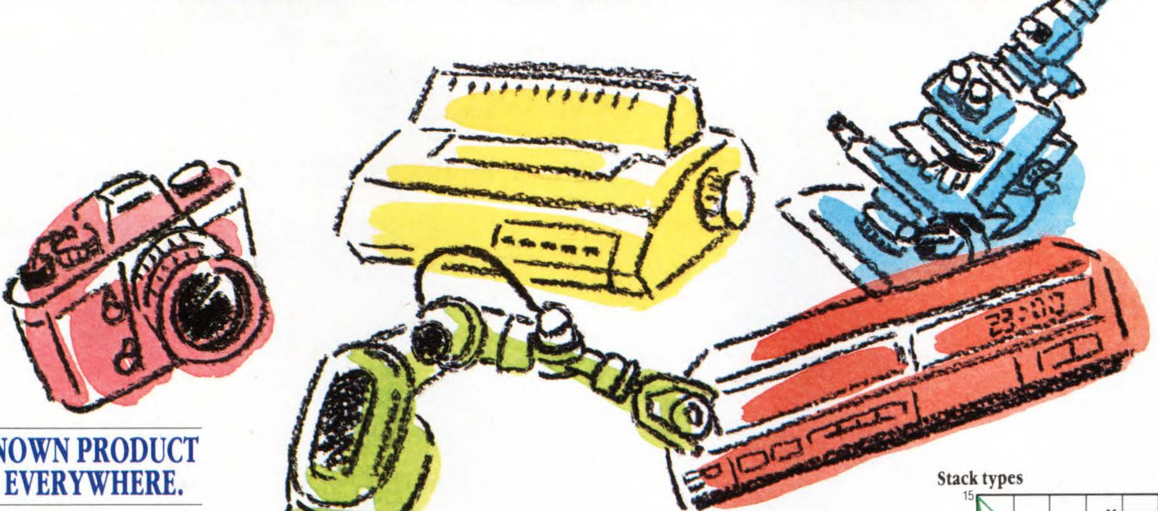

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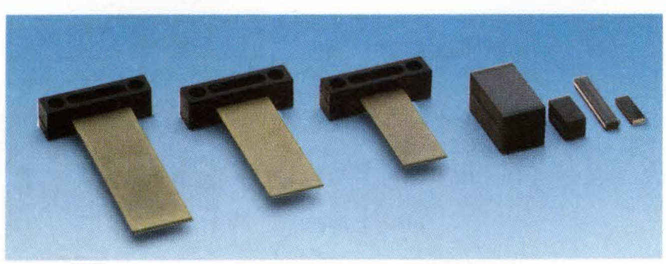

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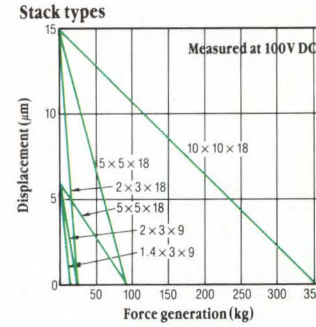

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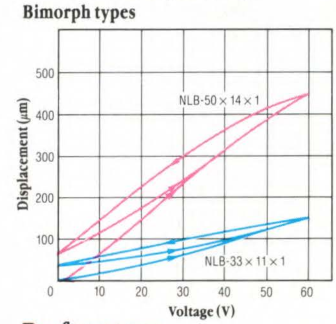

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NLA-2×3×9	6.5	21.0
NLA-2×3×18	15.0	21.0
NLA-5×5×9	6.5	87.0
NLA-5×5×18	15.0	87.0
NLA-10×10×18	15.0	350.0
Bimorph types	(μm/60V) ±20%	(g/60V) ±20%
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NLB-40×12×1	300	30
NLB-50×14×1	450	48

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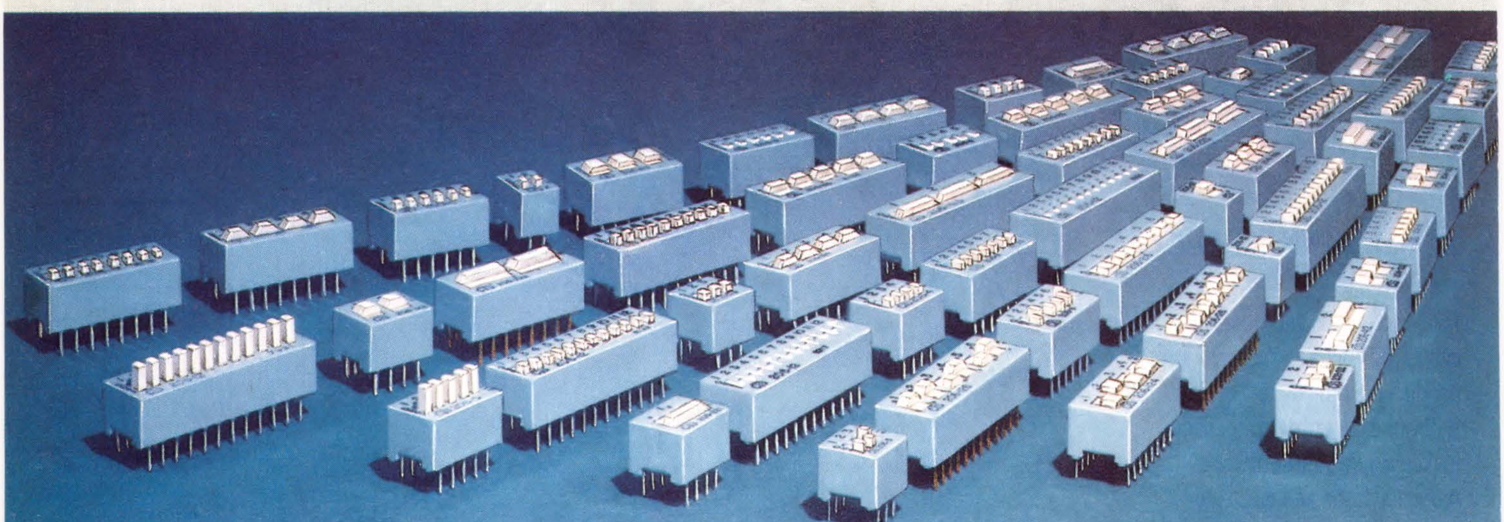

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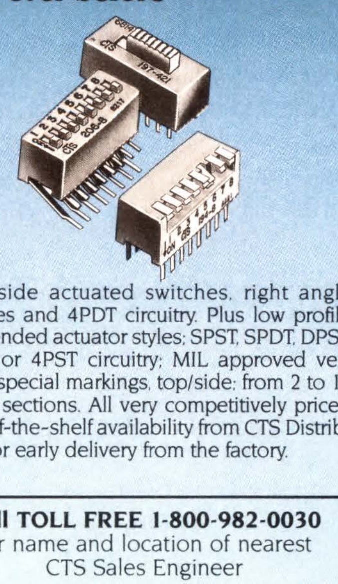

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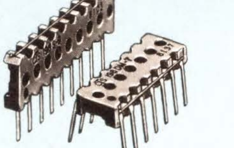

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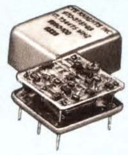

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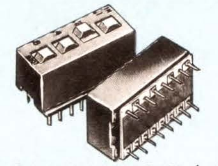

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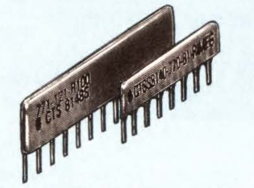

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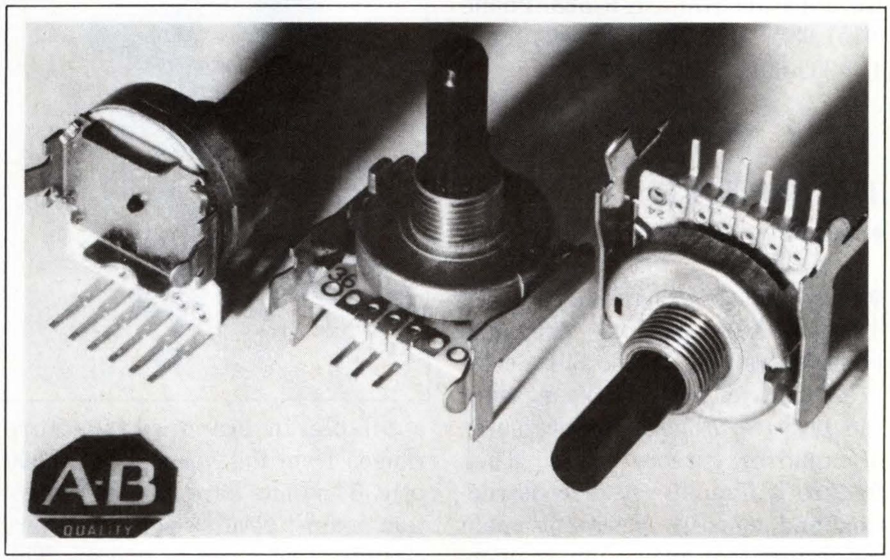
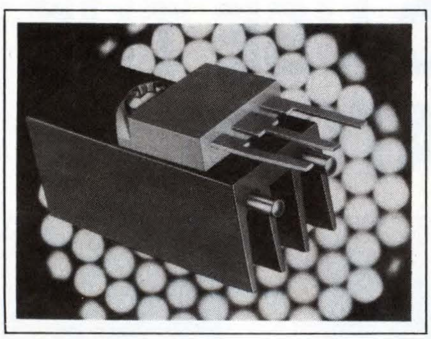
- *Lifetime of 50,000 cycles min*



Type EV and EH encoders are available with 2-, 4-, and 5-bit digital outputs that are directly compatible with μPs. All feature continuous rotation with 36 detents/revolution. The 2-bit devices provide enough output for the μP to count the number of steps and determine the direction of rotation. The 4- and 5-bit versions provide a more complete set of information to the μP; each position has a unique code, and the setting is not dependent on the storage of information in local memory. This absolute-reference design means settings simply correspond to front panel markings, which eliminates the need for a support display. The operating range for each of the three models spans 0 to 85°C. Minimum rotational life specs at 100,000 cycles for the 2-bit models and 50,000 cycles for the 4- and 5-bit models. $1.39 to $1.51 (1000). Delivery, stock to eight weeks ARO.

Allen-Bradley, 1414 Allen-Bradley Dr, El Paso, TX 79936. Phone (800) 592-4888; in TX, (800) 292-4888.

Circle No 395



HEAT SINKS

- *Compatible with wave-soldering systems*
- *Accommodate a variety of package styles*

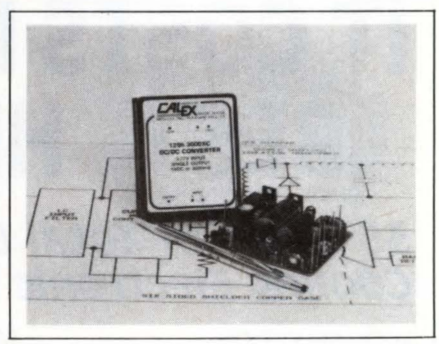
Series 5817-19 heavy-duty extruded heat sinks can accommodate TO-218, TO-247, and TO-3P semiconductor packages. Designed to provide maximum thermal performance in minimum pc-board space, the vertically mounted units have four fins and measure 0.64-in. square. They are available in heights of 1, 1.5, and 2 in., and feature tinned wave-solderable mounting pins to eliminate stress on semiconductor leads. The 2-in. model 5819B has a thermal resistance of approximately 13°C/W under natural convection and 2.8°C/W at 500-ft/min air velocity. The aluminum alloy heat sinks have a standard black anodize finish, but other finishes are available. $0.49 (1000) for the 1-in. high model. Delivery, stock to six weeks ARO.

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400.

Circle No 396

DC/DC CONVERTER

- *Accepts 9 to 27V dc inputs*
- *Can achieve efficiencies over 80%*



Featuring a 70-kHz MOSFET-based switching design, the 12S5.3000XC dc/dc converter accepts any input from 9 to 27V dc and outputs 5V at 3A. Pulse-by-pulse current monitoring provides 8 hours min of short-circuit protection. The converters achieve 80% min efficiency at loads as low as 20% of full load. Key specs include 0.2% line and load regulation, 30-mV p-p output noise, 0.3%/1000-hour long-term stability, 500V dc isolation, and a −25 to +80°C operating range. An internal thermal-limit circuit shuts down the unit when the case temperature exceeds the specified high-temperature limit. A logic-shutdown pin allows you to conserve system energy by toggling the converter on and off. The pin is toggled with an open-collector TTL/CMOS control protocol. Filter circuits provide conducted-noise protection for the input and output, and a 6-sided shielded case provides RFI protection. $120.

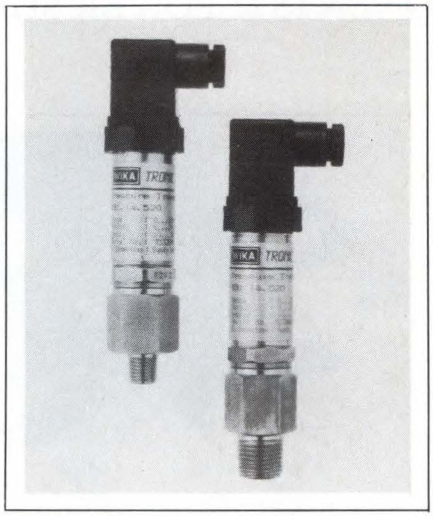
Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 269888. FAX 415-932-6017.

Circle No 397

TRANSDUCER

- *Measure positive or negative pressures*
- *Accommodate corrosive fluids*

Tronic 881 Series pressure transducers and Tronic 891 Series pressure transmitters can measure the positive or negative pressures of liquid or gaseous media. They feature a stainless-steel construction and moisture-resistant cable connectors that allow them to operate in corrosive environments. Sensor, compensator, and amplifier circuits are shock-mounted in a sealed stainless-steel body filled with a silicon compound. Both series are



available in standard pressure ranges from full vacuum to 10,000 psig. The units have built-in protection against reverse polarity, short circuits, and voltage spikes. The transducers operate from supply voltages of 20 to 32 or 15 to 32V dc. They output 0 to 100 mV in a four-wire system. The transmitters have the same capabilities as the transducers but provide a 4- to 20-mA output in a two-wire system and 0 to 5 and 0 to 10V dc at 0 to 20 mA in a four-wire system. The transmitters' supply requirement is 10 to 30V dc. $250 to $500.

WIKA Instruments Corp, Hauppague, NY 11788. Phone (516) 435-0606.

Circle No 398

SENSOR

- *Available in either light- or dark-operate versions*
- *Three models available*

ME photoelectric sensors are available in three models: ME-300 (10-ft through-beam), ME-200Z (7-ft through-beam), and ME-D30 (1-ft diffused reflective). Standard sensor features include a detachable power cord and a 3-turn, racheted adjustment mechanism for fine sensitivity control. Slitter-filters are available for small object detection.

The sensors are available in either light- or dark-operate versions. The ME-200Z has the capability of semi-transparent-object detection in a through-beam mode. From $40.

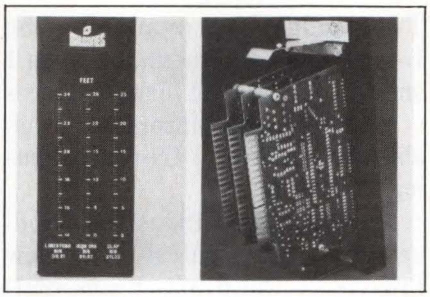
Aromat Corp, Industrial Products Div, 629 Central Ave, New Providence, NJ 07974. Phone (201) 464-3550.

Circle No 399

BAR-GRAPH DISPLAY

- *Single unit handles one, two, or three inputs*
- *Single-supply operation*

Measuring 7.25×2.75 in., Model BP303 can accept one, two, or three inputs. Meter inputs meet standard analog sensitivity requirements per ANSI C39.1—4 to 20 mA, 1 to 5V dc, 0 to 5A ac, and others. The unit operates from a 5V at 2A power supply. Options include digital display, on/off setpoint control, green or amber LEDs, and custom logo/



artwork. From $500 to $690. Delivery, eight to ten weeks ARO.

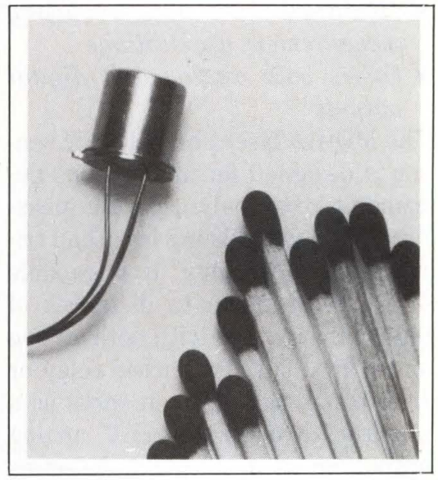
Dixson Inc, Box 1449, Grand Junction, CO 81502. Phone (303) 242-8863. TWX 910-929-6991.

Circle No 400

THERMOSTATS

- *Withstand wave soldering and board-cleaning operations*
- *100-mΩ contact resistance*

Designed for use on pc boards, SD Series thermostats can withstand wave-soldering and all board-cleaning operations. The alloy crosspoint switch contacts, designed to switch logic-level circuits, are operated by a snap-action bimetallic disc. The devices' lifetimes spec at 10,000 cycles at 1A or 100,000 cycles at 100 mA. Versions are available that open or close on temperature rise. Both groups operate to a ±5°C tolerance in 5° increments over the range of 40 to 120°C. Dielectric strength equals 500V ac at 60 Hz for 1 second. Contact resistance



measures 100 mΩ max, and the operating range specs at −50 to +150°C. The devices require no power for operation. $5 (500).

Warren G-V, 1 Apollo Dr, Whippany, NJ 07981. Phone (201) 386-1200.

Circle No 401

LASER SENSOR

- *Designed for high-accuracy measurement applications*
- *Offers both analog and digital outputs*

The MQ-LA laser photoelectric sensor is designed for applications demanding extremely accurate measurements. By utilizing laser and triple-beam technology, it is capable of resolving down to distances of 0.001 in. Provided with both analog and digital outputs (either relay or transistor), the unit can serve as a monitor through its ±5V analog output or as a set-point detector. Two models are available—the LA40 for measurements between 1 and 2 in. and the LA75 for distances of 2 to 4 in. The sensors are available for panel or DIN-rail mounting. $975 (50).

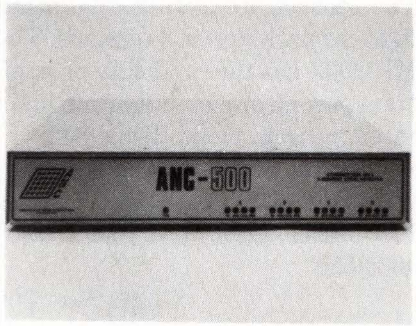
Aromat Corp, Industrial Products Div, 629 Central Ave, New Providence, NJ 07974. Phone (201) 464-3550.

Circle No 402

REPEATER

- *Conforms to IEEE 802.3 specs*
- *Provides 500m transmission distance*

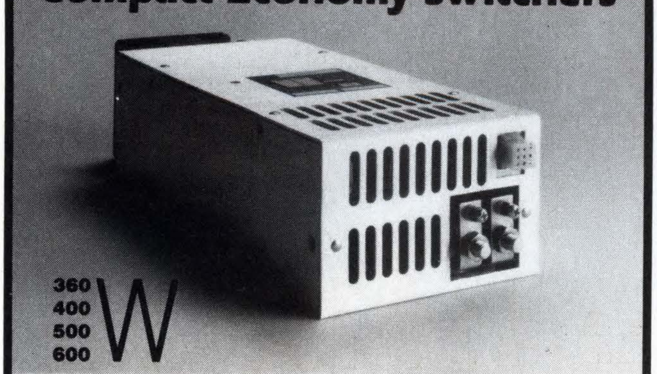
The ANC-500 4-segment Ethernet repeater can extend the transmission distance of a network cable segment more than 500 meters. It conforms to Ethernet/IEEE 802.3 repeater specifications and the 10M-bps Ethernet CSMA/CD operating requirements. The repeater

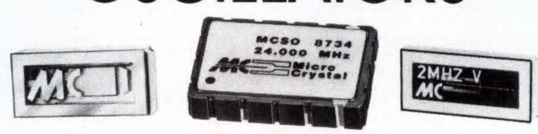


can retime and amplify packets from either Ethernet segment and transmit them to other segments. It can also regenerate the preamble bits. The unit uses four transceivers and four cables to interconnect the four Ethernet segments. Maximum allowable segment-to-segment separation distance is 100m. $1450.

American Network Connections Inc, 179 E Tasman Dr, San Jose, CA 95134. Phone (408) 922-1600. TLX 798562. FAX 408-922-1617.

Circle No 403





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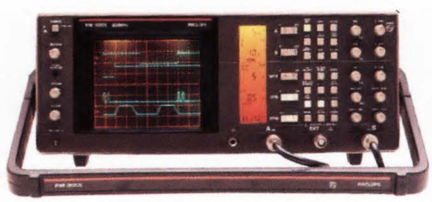
PM 3050 60 MHz, dual channel, single timebase oscilloscope



PM 3055 60 MHz, dual channel, third-channel triggerview, delayed timebase oscilloscope

PM 3065 100 MHz, dual channel, third-channel triggerview, delayed timebase oscilloscope

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PM 3256 75 MHz, compact field oscilloscope

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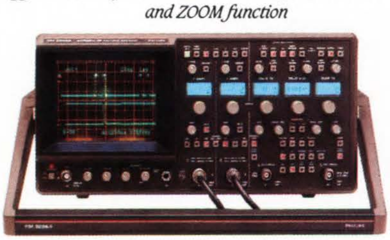

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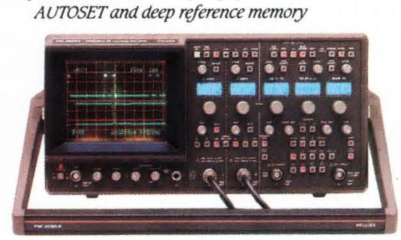
PM 3320A Single event digital storage oscilloscope with 250 MS/s sampling (catches 3 ns glitches), 200 MHz bandwidth and 10 bit vertical resolution



PM 3286A 200 MHz oscilloscope with AUTOSET, subnanosecond risetime, plus infra-red remote control and IEEE

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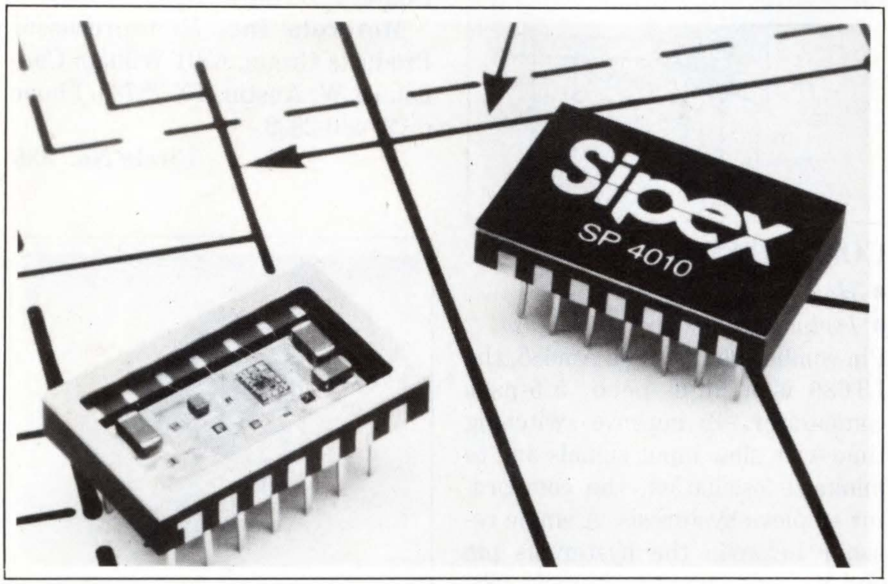


BUFFER AMPLIFIER

- *Offers 16-bit accuracy*
- *Features a 60-MHz bandwidth*

According to the company, the SP4010 is the first wide-bandwidth, fast-settling, FET-input buffer amplifier to achieve 16-bit accuracy. Combining a unity-gain signal follower with a transconductance feedback architecture, the SP4010 features a slew rate of 1000 V/µsec, a bandwidth of 60 MHz, and a settling time of 150 nsec to 0.005% for a 10V step. Other specifications include an input offset voltage of 1 mV (typ), an input bias current of 100 pA, and harmonic distortion of −100 dB at 10 kHz and −80 dB at 1 MHz. The SP4010's output of ±50 mA at ±5V is suitable for driving coaxial lines. Packaged in a 14-pin ceramic DIP, the SP4010 operates from ±15V supplies and dissipates 360 mW of power. Commercial version, $44.50; military version, $82.50 (100).

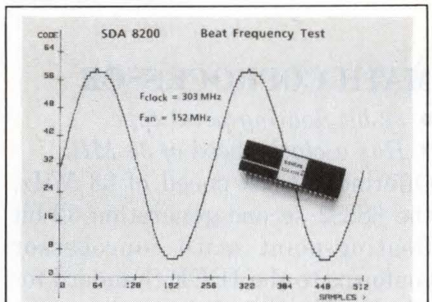
Sipex Corp, Hybrid Systems Div, 22 Linnel Circle, Billerica, MA 01821. Phone (508) 667-8700. FAX 617-667-8310.

Circle No 380

FLASH A/D CONVERTER

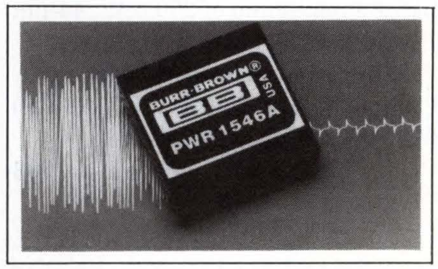
- *Features 300-MHz response*
- *Offers 5-bit resolution at 150 MHz*

The 6-bit, 300-MHz SDA-8200 can digitize a 150-MHz analog-input signal with an effective resolution of 5 bits. You can clock the converter by means of a single-ground symmetrical sine-wave, thus avoiding the performance loss of an ECL clock. Because the analog input range is also ground symmetrical and the 12-pF input capacitance is nearly independent from the input voltage, simple 50Ω interconnections are possible without an external preamplifier. Data capture is simplified by a demultiplexer that delivers two 150-MHz ECL data streams at the output. This feature slows down the output signal through two parallel 6+1-bit output data streams at half the sampling rate. The SDA-6200 comes in a 40-pin ceramic DIP. $170 (100).



Siemens Semiconductor Group, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4534.

Circle No 381



DC/DC CONVERTER

- *Has a 5W-rated output power*
- *Features a maximum output noise of 1 mV p-p*

The PWR1546A dc/dc converter features an output noise of less than 1 mV p-p (0.6 mV typ) over a dc to 10-MHz bandwidth. The unit, which has as a 5W output capability, transforms a 5V input to a ±15V output for powering sensitive analog circuits, such as data converters and high-gain amplifiers. The hybrid IC uses linear regulators to fully regulate each output, and its input-output isolation can withstand 750V dc continuously. The converter's MTTF (calculated per MIL-HDBK-217 Rev E) is over 890,000 hours. $42.00 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 382

CMOS µP

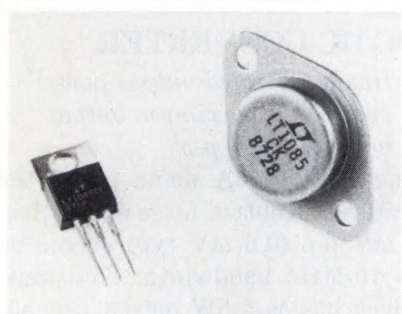
- *Performs at a 10-MHz rate*
- *Has on-chip clock-oscillator circuit*

The Z84C01 8-bit CMOS µP incorporates a Z80 CPU and an on-chip clock generator/controller operating at 10 MHz. It accepts either crystal- or TTL-level source inputs.

The Z84C01's features include the full 158 Z80 instruction set, three processing modes, and an on-chip dynamic RAM refresh controller. The μP consumes 35 mA of current in the operating mode and 0.5 μA in the standby mode. Two mode-select pins allow you to accommodate all application and timing requirements. The device operates from a single 5V supply and dissipates a maximum of 250 mW. 44-pin PLCC, $4.50 (100).

Zilog Inc, 210 Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. TWX 910-338-7621.

Circle No 383



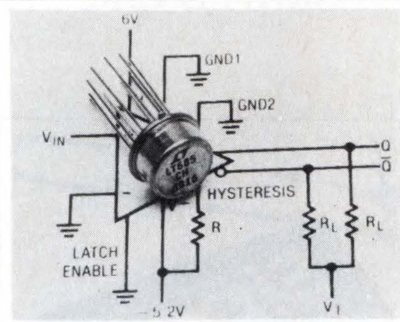
3A REGULATOR

- *Has a dropout of 1.5V max*
- *Operates at a 1V input-output differential*

The LT1085 is a 3A positive adjustable regulator. It can operate at an input-to-output differential as low as 1V, and has a maximum dropout of only 1.5V at maximum current. On-chip trimming adjusts the reference voltage to 1%. The device is pin-compatible with other 3-terminal regulators such as the LM150 and LM350, but has about 50% lower dropout at maximum current, according to the vendor. The IC requires the use of a 10-μF capacitor to achieve its performance. The quiescent current of the device flows into the load, which helps improve its efficiency. $3.70 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. FAX (408) 434-0507.

Circle No 384



COMPARATOR

- *Has 5.5-nsec speed*
- *Includes a hysteresis function*

Pin-combatible with the Am685, the LT685 is a high-speed, 5.5-nsec comparator. To improve switching time with slow input signals and to minimize oscillation, the comparator employs hysteresis. A single resistor between the hysteresis pin and V− adds input hysteresis voltage as the circuit draws more current. The differential inputs and complementary outputs of the LT685 are fully compatible with ECL logic levels. A latch function lets you use the comparator in an S/H mode. The device's output current can drive 50Ω lines. The input-offset voltage is ±2 mV. Packaging includes a 10-pin TO-5 metal can, a 16-pin plastic DIP, and a 16-pin ceramic DIP. Commercial versions in a plastic DIP, $4.50 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545.

Circle No 385

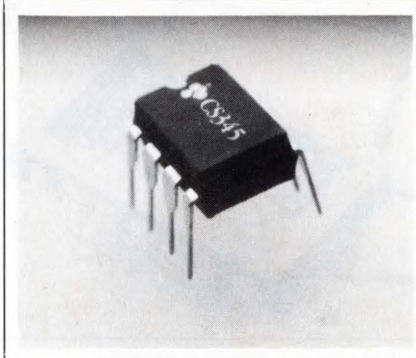
MATH COPROCESSOR

- *32-bit floating-point type*
- *Has a clock speed of 33 MHz*

Offering a clock speed of 33 MHz, the 68882 second-generation 32-bit floating-point math coprocessor conforms to the IEEE Standard for Binary Floating Point Arithmetic. Apollo Computer (Chelmsford, MA) is the first company to announce a 68030-based workstation incorporating the 33-MHz coprocessor. The device is software compatible as well as pin compatible with its predecessor, the 68881. According to the vendor, the 68882 is the first single-chip processor to break the 2-million Whetstone barrier. $708. Delivery, 60 days ARO.

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 440-2839.

Circle No 386



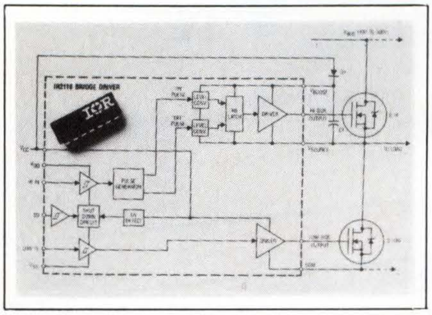
IGNITION PREDRIVER

- *Features a 200-mA output drive current*
- *Has a saturation voltage of less than 0.5V*

Designed primarily for automotive applications, the CS-345 drives and controls an external power transistor or FET to start and regulate inductive load currents. An input control voltage between 0.9 and 3.5V triggers the chip's output driver into saturation, with a maximum drop of 0.5V. An external resistor sets the CS-345's output drive current (200 mA max). A sense input monitors the load current and sets the regulation to a user-selectable level. Once the IC begins regulating the load current, the status pin switches from a logic-1 to a logic-0. When the control input switches to a logic-0, the output transistor goes into cutoff and shuts off the drive current to the load. The CS-345 is packaged in an 8-pin DIP. $0.94 (1000).

Cherry Semiconductor Corp, 2000 South County Trail, E Greenwich, RI 02818. Phone (401) 885-3600. TLX 6817157. FAX 401-885-5786.

Circle No 387



DUAL DRIVER

- *Provides a floating high-side output*
- *Features LSTTL compatibility*

The IR2110 monolithic power IC drives the gates of a pair of n-channel power MOSFETs. It provides the interface between a logic-level control circuit and a high-voltage, high-current, half-bridge converter. The IC can drive insulated gate bipolar transistors, as well as power MOSFETs. The dual-channel driver features a floating high-side output, with a source voltage to 500V above ground and a ground-referenced low side output. Separate pin-outs let you employ a lower voltage bias for the logic function. The IC can operate at frequencies greater than 1 MHz; its output rise time is less than 20 nsec with a 500 pF load. In a 14-pin DIP, $7 (1000).

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 772-2000.

Circle No 388

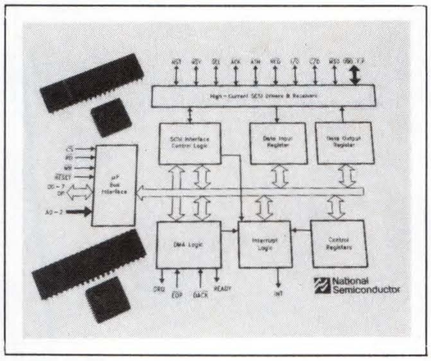
GPS-BAND AMPLIFIER

- *Features noise spec of 4.5 dB*
- *Operates from 1.227 to 1.575 GHz*

You can employ the Model 6011 hybrid amplifier in global positioning systems (GPS) or down-converter applications. The unit follows and powers an antenna amplifier; a low-pass network is used to bias the preceding amplifier. The device features a noise spec of 4.5 dB (max) over the frequency range of 1.227 to 1.575 GHz and 15 dB of gain. The spdt RF-pin switch provides more than 40 dB of isolation. The unit operates over a temperature range of −55° to 125°C. It requires 12V, 45-mA max and 5V, 35-mA max supplies. The amplifier is housed in a 22-pin, 1×1.25×0.150-in hermetically sealed flatpack. $750 (100).

White Technology Inc, 4246 E. Wood St, Phoenix, AZ 85040. Phone (602) 437-1520. TWX 910-951-4203.

Circle No 389



CMOS SCSI CHIPS

- *Feature 30-nsec read-across time*
- *Provide DMA rate of 4M bytes/sec*

The DP8490 and DP5380 CMOS devices comply with the SCSI standard and are pin compatible with the NMOS NCR5380 device. They feature a 30-nsec read-across time and provide a DMA rate of 4M bytes/sec. The DP8490 also features a phase-mismatch interrupt that detects a mismatch in the information-transfer phase, decreasing dead time on the SCSI bus. The DP5380 features input protection that allows the device to power down without collapsing an operating SCSI bus. Both models are offered in 40-pin DIPs and 44-pin PLCCs. The 44-pin PLCC version of the DP8490 provides an extra pin for µP data-bus parity. DP8490, $8; DP5380, $7 (in small quantities).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-4960. TLX 346353.

Circle No 390

Order KEMET T491 Surface-Mounted Tantalum Capacitors with precision-molded design and unique terminations for higher production efficiency, simpler soldering and greater yields. Laser marked; easy orientation. On 7 and 13-inch taped reels in capacitances from 0.10 to 68.0 μF; 6 to 50 VDC.

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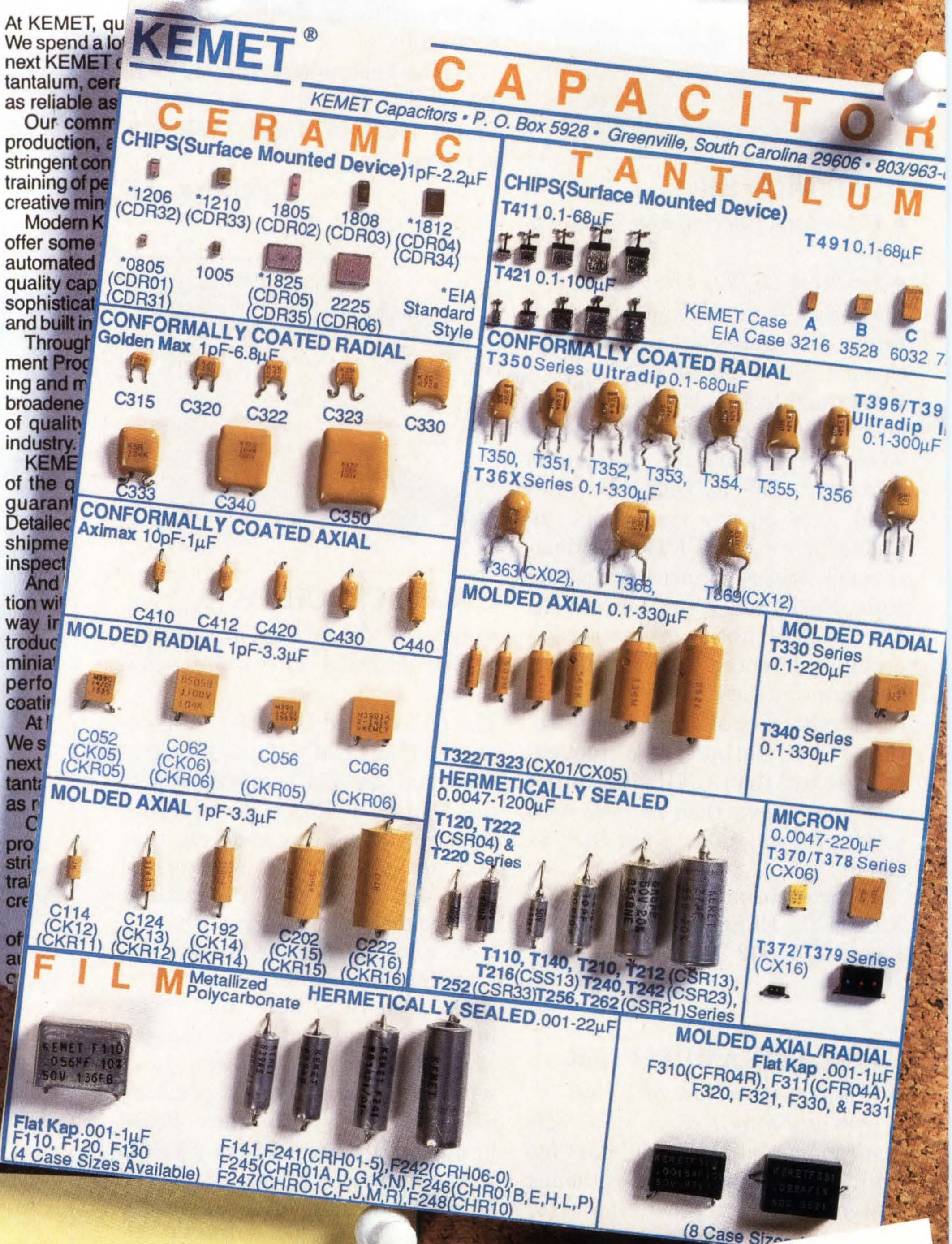


George —
why not KEMET,
instead of all the
different suppliers
we've got now?!!
— Ron

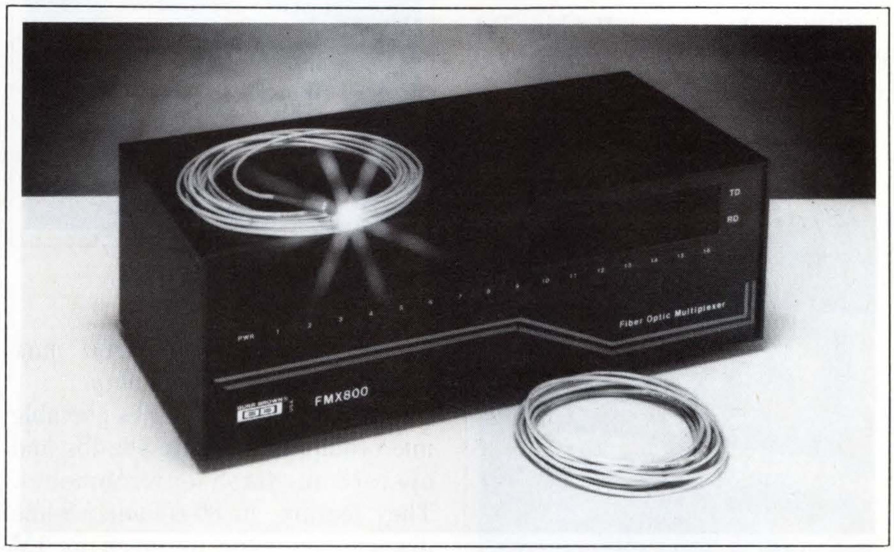
CIRCLE NO 110

Sales Offices and Distributors Worldwide
In U.S.A.: (803) 963-6348; Telex 57-0496.
In Europe: 22-396500; Telex 412-901 KESA CH.
In Asia: 852-3-770-5633; Telex 780-44093 KEMET HX.

KEMET® Electronics Corporation
P.O. Box 5928 • Greenville, SC 29606 • 803/963-6300

MULTIPLEXER

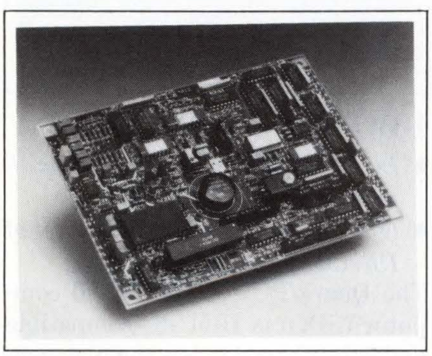
- *Expandable to 64 channels for fiber-optic communications*
- *Each channel can operate full duplex at 19.2k baud*



The FMX800 is a multiplexer and demultiplexer for fiber-optic communications. A stand-alone metal enclosure that's either rack mounted or rests on a table, the unit contains a power supply and a mother board, which accepts plug-in cards. The plug-in cards consist of a fiber-optic module that can transmit and receive signals on a pair of optical cables at a 3M baud rate, as many as 16 19.2k baud RS-232C or fiber-optic channel cards, and an expansion card. The expansion card lets you connect as many as three chassis, thus allowing 64 channels to transmit at full duplex at data rates of 19.2k baud. The unit continually transmits the control signals Request to Send (RTS), Clear to Send (CTS), Data Set Ready (DSR), and Data Terminal Ready (DTR) for each channel. When the unit receives a data byte, it attaches this byte to the control byte. From $800 for two channels to $5700 for each end of a 64-channel system. Delivery, four to eight weeks ARO.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 351



A/D CONVERTER

- *10-bit resolution and 30-MHz sampling rate*
- *150-MHz input bandwidth*

The 4194 10-bit A/D converter operates at sampling rates from dc to 30 MHz and features a data-conversion time of 105 nsec. A single-shot mode lets you trigger on transient events such that data is available as often as 33 nsec delayed by 105 nsec from the input signal. The unit features a 150-MHz input bandwidth, a total harmonic distortion of −56 dB at 4 MHz, a 400V/μsec slew rate, a <10-psec aperture uncertainty, and ECL-compatible outputs. The user can adjust the analog input impedance, which is nominally set to 100Ω at the factory, between 50 and 200Ω. You can mount the 5×7-in. board on a system mother board. The unit contains a track-and-hold circuit, timing circuitry, and latched-offset binary outputs. $2492 (100).

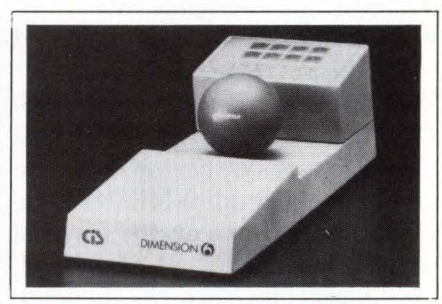
Teledyne Philbrick, 40 Allied Dr, Dedham, MA 02026. Phone (617) 329-1600. FAX 617-326-6313. TLX 212711.

Circle No 352

CONTROL BALL

- *Provides natural manipulation of screen objects*
- *Has three translational, three rotational degrees of freedom*

The Dimension 6 is a control ball that lets the user naturally manipulate screen objects on a 3-D graphics system. The unit uses an optical sensor that measures force and

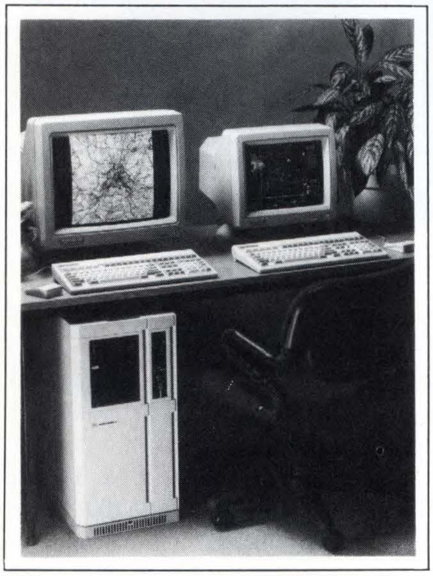


torque. It allows the user to control three translational and three rotational degrees of freedom, using one hand. The unit sends the 8-bit data for each degree of freedom to the graphics system via an RS-232C interface with variable baud rates. In addition, the unit contains a keypad with 11 buttons to select different operational modes. Three of the buttons, labeled Tra, Rot, and Dom, let you control translational or rotational motion only or select the data for the most dominant degree of freedom detected by the sensor. The eight remaining buttons are user selectable for specific functions. The unit is powered from

220 V ac at 50 Hz or 110 V ac at 60 Hz. It weighs 1.5 kg and costs $3300.

CIS Graphics Inc, 2 Robbins Rd, Westford, MA 01886. Phone (508) 692-9599.

Circle No 353



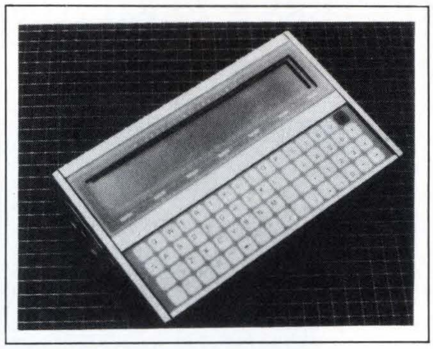
GRAPHICS SUBSYSTEM

- *Uses 32-bit microprocessor*
- *Provides six custom-designed VLSI gate arrays*

The Formula 1 Series Model CGS-4700 provides either an entire graphics subsystem or a single graphics engine for VME Bus systems. The graphics engine features six custom-designed VLSI gate arrays; needs one VME slot; and employs a Motorola 68020 32-bit microprocessor as well as a 256k-byte EPROM. The graphics engine lets you perform tasks such as pan, scale, and rotate at the local level. It generates graphics in 256 colors with a resolution of 1280 × 1024 pixels. The graphics engine provides eight pixel planes—four on the main board and four on a daughter board. In addition, it has I/O drivers to support Unix System V and provides VT100 emulation. A single unit, $4995; $2997(150).

CalComp, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (714) 821-2142.

Circle No 354



MICROCOMPUTERS

- *Weigh 3½ lbs*
- *Feature 1M byte of RAM max and an 80-column display*

The Microscribe 700 Series portable microcomputers weigh 3½ lbs and operate in harsh environments. They feature an 80-column × 8-line display and offer as much as 1M byte of RAM. The microcomputers' EPROM capacity ranges to 274k bytes. A supertwist LCD display increases visibility and readability and provides a 480 × 64-pixel full graphics mode. Backlighting is standard. The keyboard features a separate numeric keypad. The microcomputers measure 10.9 × 6.4 × 1.5 in. and operate over 32 to 122°F. If you don't use the backlight, the rechargeable NiCd batteries provide a 10-hour operating life. From $2875. Delivery, eight weeks ARO.

Amlan Inc, 97 Thornwood Rd, Stamford, CT 06903. Phone (203) 322-1913. TLX 643647.

Circle No 355

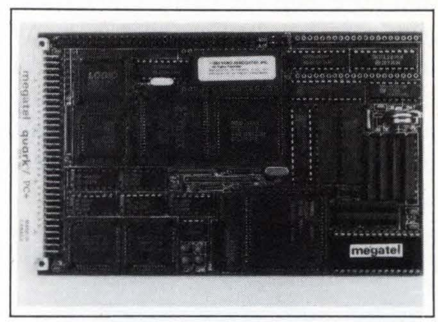
BERNOULLI DRIVE

- *20M-byte cartridges for the Macintosh II computer*
- *File-transfer software for IBM PC-compatible programs*

The Bernoulli Box II consists of a stand-alone Bernoulli drive for Macintosh II computers. The device comes in both a single and dual 5¼-in. half-height drive configuration with removable 20M-byte cartridges. The drive has error checking and recovery that automatically corrects bad sectors and keeps an error log of media problems without user intervention. An integrated SCSI port meets the requirements for devices on an Apple-defined SCSI channel. A file-transfer software package lets you insert a cartridge in the drive that has been formatted by an IBM PC or a compatible computer. The software translates the data on the cartridge so the data appears as Macintosh standard files and file folders. The user can change the information on the cartridge and return it to an IBM system in standard PC format. Dual drive, $2550; single drive, $1650; file-transfer software, $149.

Iomega Corp, 1821 W 4000 South, Roy, Utah 84067. Phone (801) 778-3000.

Circle No 356



1-BOARD COMPUTER

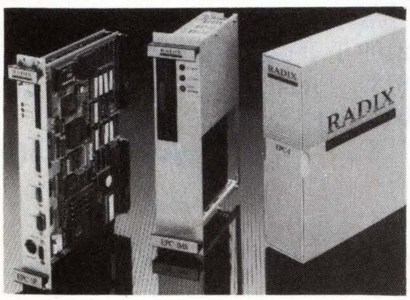
- *Is an IBM PC computer with video and disk controller*
- *Options include 768k bytes of DRAM and a SCSI adapter*

The Quark/PC + single-board computer (SBC) is IBM PC-compatible and has onboard video and disk controllers. The 4 × 6-in. pc board uses a 96-pin Eurocard connector for I/O and either a 64-pin header or a 62-pin male edge connector for connections to the PC bus. The base unit features an 8-MHz NEC V-40 CPU, eight levels of interrupt, 256k bytes of dynamic RAM, 16k-byte BIOS in ROM, an additional 112k bytes of ROM space, three 16-bit timers, three DMA channels, a socket for an 8087 coprocessor, an IBM keyboard port, and an 8-bit parallel I/O port. Options include a Yamaha PCDC 6366 video controller, two additional serial ports, an NCR

5380 SCSI controller for hard-disk control, expandable memory to 768k bytes, a real-time clock with battery backup, and a Western Digital 37C65 floppy-disk controller. The board requires 5V for power; and, since all ICs are CMOS devices, it typically draws 3W of power. Base unit, $325.

Megatel Computer Corp, 174 Turbine Dr, Weston, Ontario, Canada M9L 2S2. Phone (416) 745-7214. FAX 416-745-8792.

Circle No 357



80386 SYSTEM

- *Consists of two modules that run IBM PC/AT software*
- *Has 4M bytes of dual-ported RAM*

The EPC-1 is a 2-module system that creates an IBM PC/AT computer on the VME Bus. It contains a 16- or 20-MHz 80386 µP and as much as 4M bytes of dual-ported RAM. The modules can run the large base of PC/AT-compatible software on a VME Bus mainframe. The processor module contains an EGA graphics controller (with support for 640×480-pixel Super EGA resolution), floppy- and SCSI hard-disk-drive controllers, two RS-232C ports, a parallel printer port, and a PC/AT-compatible keyboard port. The disk module contains a 1.4M-byte, 3½-in. floppy-disk drive and a ruggedized 40M-byte hard disk. Both modules comply with the IEEE-1014-87 VME Bus specification. The system also contains gate array ICs, which implement the functions for the VXI Bus, including geographical addressing. The system includes a software package, which provides device drivers for transporting IBM PC/AT applications to the VME Bus. The system combined with DOS 3.3, Windows 2.0 or 386, a keyboard, and documentation, $7950.

Radix MicroSystems Inc, 19545 NW Von Neumann Dr, Beaverton, OR 97006. Phone (503) 690-1229.

Circle No 358

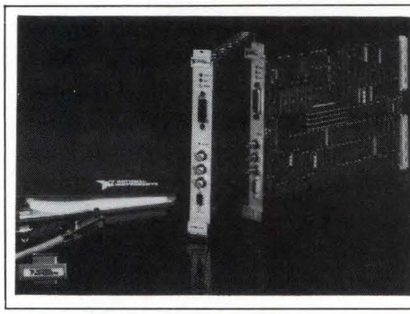
80386-BASED PCs

- *Take both 5¼- and 3½-in. disk drives*
- *Feature adjustable speeds to 16 MHz*

The PC916 80386-based PCs offer 32-bit IBM PC/AT compatibility. They accept either 5¼- or 3½-in. disk drives. The PCs feature speeds to 16 MHz. This feature lets you adjust the speed for specific compatibility modes. The PCs can address 268M bytes of physical memory and 4G bytes of virtual memory. A 2M-byte companion memory board and an EGA card are standard. You can expand the memory by installing additional memory boards and connecting them to the 32-bit extender bus. The PCs can accommodate five half-height or two full-height drives, each allowing for 230M bytes max. You can switch the 220W power supply from 115 to 230V ac. The PCs feature three types of keyboards: standard, with 10 function keys; workstation, with 12 function keys; and advanced, with 30 function keys. Standard model with 30M-byte fixed drive, $6353; with a 70M-byte fixed drive, $7553.

NCR Corp, 1700 S Paterson Blvd, Dayton, OH 45479. Phone (513) 445-4236.

Circle No 359



VXI BUS BOARD

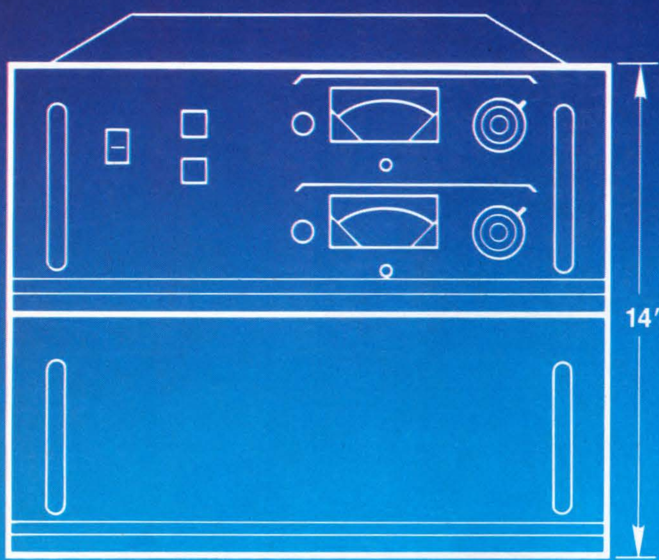
- *Links instruments-on-a-card to the IEEE-488 bus*
- *Can be used as the top-level commander in slot 0*

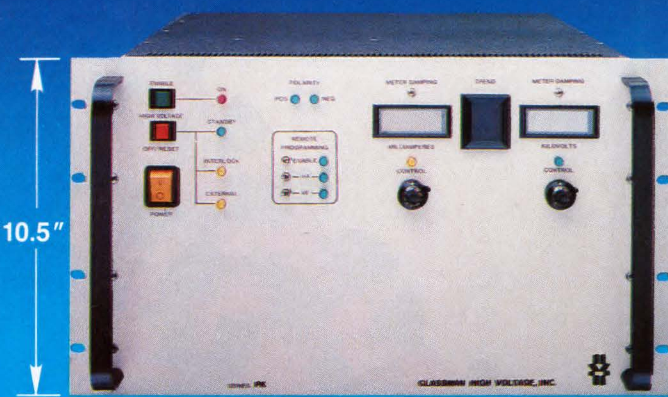
The GPIB-VXI is an interface board that links the IEEE-488 bus to instruments-on-a-card resident on a VXI Bus. The board can function as a top-level commander in slot 0 of a C-size VXI Bus system or as a servant. It contains a 68070 μP that has a 16- or 32-bit CPU, a memory-management unit, a 2-channel DMA controller, an I^2C serial bus interface, a UART serial interface, a 16-bit timer/counter, and an interrupt controller. It has 512k to 4M bytes of memory, which is dual-ported to the VXI Bus. The firmware, which is resident in EPROM, is based on the pSOS real-time operating system. The IEEE-488 interface circuitry on the board consists of a 7210 talker/listener/controller and a Turbo488 custom ASIC. The custom ASIC provides a FIFO buffer between the IEEE-488 interface and a private local bus. A 512k-byte RAM version with the operating firmware in ROM, $3000.

National Instruments Corp, 12109 Technology Blvd, Austin, TX 78727. Phone (512) 250-9119. TLX 756737. FAX 512-250-0382.

Circle No 360

Glassman HV supplies like to be compared!





All Glassman HV supplies are better by design, offering a combination of performance, size, and weight that beats the competition hands-down. Consider the new PK Series. . .

Nearest Competitor	PK Series
3 KW, 14" high 0.63 W/in.^{3} 21.4 W/lb. 140 lbs.	4 KW, 10.5" high 1.2 W/in.^{3} 61.5 W/lb. 70 lbs.

But numbers are not the whole story. For example, only the PK Series shows you at a glance its complete status. Indicators signal power on, HV on, standby, safety interlock, external trip, polarity, remote/local control, regulating mode (voltage or current), output voltage and current. . .even a bargraph trend indicator for pulsed load applications is standard.

Glassman's pulse width modulated circuitry delivers regulation better than 0.01%, low ripple, fast transient response, and full load efficiency greater than 85% . . . all with lower parts count for greater reliability. And Glassman's unique air insulation offers field-proven serviceability while it contributes to reduced weight.

Call or write for full information. Compare the PK Series to any others. . .we're confident you will decide that Glassman is the true innovator in high voltage power supply technology.

Glassman High Voltage, Inc.

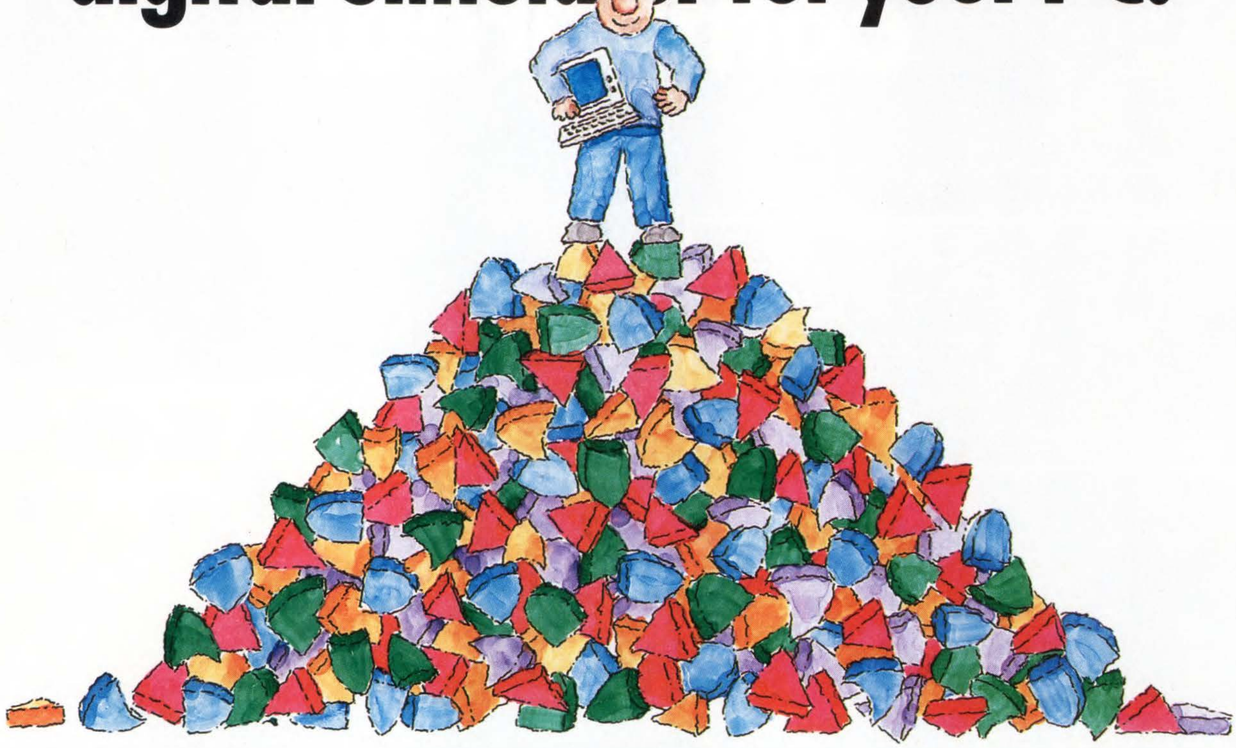
Route 22 (East)
Salem Industrial Park, PO Box 551
Whitehouse Station, NJ 08889
Telephone (201) 534-9007
TWX 710-480-2839
FAX: (201) 534-5672

GLASSMAN HIGH VOLTAGE INC.

CIRCLE NO 117

MICRO-LOGIC II.™

The CAE tool with a 10,000-gate digital simulator for your PC.



Spectrum Software's MICRO-LOGIC II® puts you on top of the most complex logic design problems. With a powerful total capacity of 10,000 gates, MICRO-LOGIC II helps engineers tackle tough design and simulation problems right at their PCs.

MICRO-LOGIC II, which is based on our original MICRO-LOGIC software, is a field-proven, second-generation program. It has a high-speed event-driven simulator which is significantly faster than the earlier version.

Timing Simulator

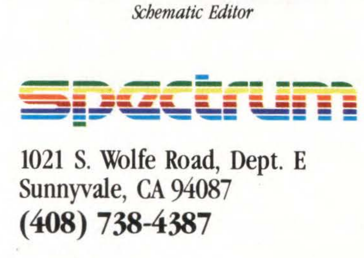
The program provides you with a top-notch interactive drawing and analysis environment. You can create logic diagrams of up to 64 pages with ease. The software features a sophisticated schematic editor with pan and zoom capabilities.

Shape Editor

A 200-type library of standard parts is at your fingertips. And for a new high in flexibility, a built-in shape editor lets you create unique or custom shapes.

MICRO-LOGIC II is available for the IBM® PC. It is CGA, EGA, and Hercules® compatible and costs only $895 complete. An evaluation version is available for $100. Call or write today for our free brochure and demo disk. We'd like to put you in touch with a top digital solution.

- Total capacity of 10,000 gates
- Integrated schematic editor
- Fast assembly language routines
- Standard parts library of 200 types
- Event-driven timing simulator
- Built-in shape editor
- Multiple delay models
- Printer and plotter hard copy



Schematic Editor

spectrum

1021 S. Wolfe Road, Dept. E
Sunnyvale, CA 94087
(408) 738-4387

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CIRCLE NO 109

DIAGNOSTIC TOOL

- *Finds many kinds of bugs that a C compiler can miss*
- *Adapted for use on minicomputers and mainframes*

Generic Lint is a diagnostic tool that analyses software systems written in C and finds bugs, glitches, and inconsistencies that a compiler, working on one module at a time, can miss. The program is a generalized version of the vendor's PC-Lint, which runs on MS-DOS systems. The generalized version is supplied in a "shrouded source" format that is easy to compile, and it is intended for use on VAX machines running VMS or Unix, IBM mainframes running VM/CMS, and 68020-based machines running Versados or OS-9. Generic Lint will find inconsistent declarations, argument/parameter mismatches, uninitialized variables, variables assigned but not used, printf-scanf inconsistencies, and many other potential problems. It provides four kinds of error messages: fatal, syntactic, warning, and informational. You can selectively inhibit any error messages, alter their format, change the size of scalars, and perform other kinds of customization. Prices start at $798 and depend on the machine licensed and the number of users.

Gimpel Software, 3207 Hogarth Lane, Collegeville, PA 19426. Phone (215) 584-4261.

Circle No 411

ANALOG ANALYZER

- *Performs analysis of open- and closed-loop response*
- *Converts time-domain to frequency-domain response*

FANSIM (FFT, Frequency ANalysis, and SIMulation) provides comprehensive simulation capability in the frequency domain. Inputs may be real, measured responses or time-domain functions obtained from the vendor's TUTSIM program or generated internally by the program. FFT techniques convert time-domain responses to spectral functions. The program will find the transfer functions of real or simulated systems and will find poles and zeros. It will accept input or produce output in the form of polynomial functions, poles/zeros, graphical curves, spectral arrays, or pole-residues. The program is menu-driven and provides more than 40 functions for the manipulation of spectra. To run the program, you need an IBM PC or compatible that has at least 330k bytes of RAM (512k bytes recommended); a CGA, EGA, or Hercules graphics card; and a math coprocessor. $395; demo disk, $39.95.

Tutsim Products, 200 California Ave, Suite 212, Palo Alto, CA 94306. Phone (415) 325-4800.

Circle No 412

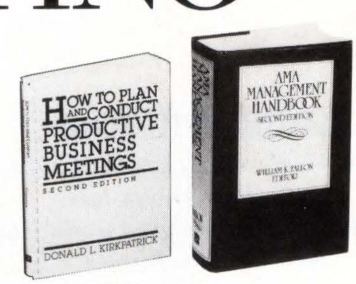
PCB WORKSTATION

- *Allows you to generate panel data for PCB manufacture*
- *Comes with a library of venting patterns*

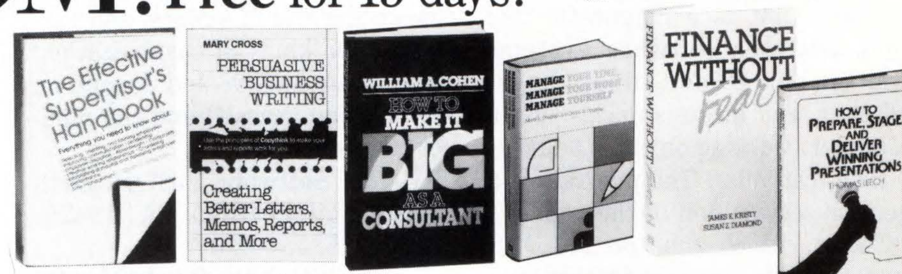
The SeriCAM is a PC-based workstation that runs software developed by Infinite Graphics; the hardware is from Hewlett-Packard and Mitsubishi. The workstation consists of two monitors, a keyboard, a mouse, a disk drive, and an optional graphics tablet. The software lets you use CAD-generated pc-board design data to produce board-manufacturing information for output to laser or vector plotters. You can adjust feature sizes, step-and-repeat the circuit design to produce multiple originals, and merge the circuit with venting patterns that are stored in a panel database. Once you have set the design parameters, the system design-rule-checking function identifies rule violations and lets you correct them and store the corrected design. The program can direct output to magnetic tape or to a local-area network for use by any currently available photoplotter. The software is menu-driven, and all commands are in English. $55,000 (including all hardware).

E I Dupont de Nemours & Co Inc, Imaging Systems Dept, Eagle Run Site, Wilmington, DE 19898. Phone (302) 733-9611.

Circle No 413



HOW TO PLAN AND CONDUCT PRODUCTIVE BUSINESS MEETINGS
SECOND EDITION
DONALD L. KIRKPATRICK
AMA MANAGEMENT HANDBOOK
SECOND EDITION



The Effective Supervisor's Handbook
MARY CROSS
PERSUASIVE BUSINESS WRITING
Creating Better Letters, Memos, Reports, and More
WILLIAM A. COHEN
HOW TO MAKE IT BIG AS A CONSULTANT
MANAGE MANAGE MANAGE
FINANCE WITHOUT Fear
HOW TO PREPARE, STAGE, AND DELIVER WINNING PRESENTATIONS

TIMING ANALYZER

- *Performs timing-margin analysis to allow "what-if" changes*
- *Updates worksheets when you edit library components*

Timing Margins Analyzer (TMA) provides efficient methods of entering min/max data for all necessary parameters of your design. The program handles timing margins in manageable chunks, with a separate worksheet for each timing case, so that you can perform "what-if" analyses and obtain immediate results. The program creates a linked database, and automatically updates all relevent worksheets whenever you edit or change library data. Also, you can build or edit libraries directly from a worksheet. TMA handles both on-chip (IC) and printed-circuit board (PCB) designs. When in the IC mode, the program accounts for on-chip tracking. When in the PCB mode, the program checks and accounts for clock and data paths that share the same package. A graphics window allows you to define waveforms quickly, and adjusts the waveforms to show the true min/max delays that correspond to the computed margins. You can define as many as 54 timing states and view as many as nine waveforms simultaneously. The program also detects potential transmission-line problems; it will alert you to these problems and recommend values of terminating resistors or warn you if your driver is not capable of driving the terminated line. To run the program you need an IBM PC or compatible that has at least 320k bytes of memory and a CGA, EGA, or Hercules graphics adapter. A demo disk provides all functions of the production version except file-save, printing, and entry of I/O loads and values. $295; demo disk, $15.

Design/Analysis Consultants Inc, 2805 W Busch Blvd, Suite 202, Tampa, FL 33618. Phone (813) 933-0672.

Circle No 414

CASE TOOL

- *Allows you to use multiple analysis and design methods*
- *You can buy only those modules that meet your needs*

POSE (Picture-Oriented Software Engineering) is a CASE tool that consists of nine modules that run independently on machines in the IBM PC and PS/2 families and compatibles. The data-driven tool kit comprises the data-model-diagrammer, data-model-normalizer, logical-database-designer, and database-aid modules; the process-driven tool kit comprises the decomposition-diagrammer, dataflow-diagrammer, structure-chart-diagrammer, and action-chart-diagrammer modules. The ninth module, a screen- and report-prototyping module, will be available in the fall of 1988. All modules address the planning, analysis, and design phases of software development. $295 per module, or $885 for each 4-module tool kit.

Computer Systems Advisors Inc, 50 Tice Blvd, Woodcliff Lake, NJ 07675. Phone (201) 391-6500.

Circle No 415

IEEE-488 SOFTWARE

- *Lets you control instruments via an IEEE interface board*
- *Can operate with IBM PS/2s and compatibles*

ROUTE 488 version 1.03 is a memory-resident BIOS-level device driver that runs under MS-DOS. It allows you to transfer data between an IBM PC or compatible and data-acquisition or instrumentation hardware connected to an IEEE-488 bus. Enhancements to the new version extend this capability to IBM PS/2s and other 80286- or 80386-based machines. Because the software operates at the BIOS level and allocates its own buffers for DMA transfers, data transfers take place at rates as much as four times faster than transfers through a DOS device handler, which handles only one character at a time. You can

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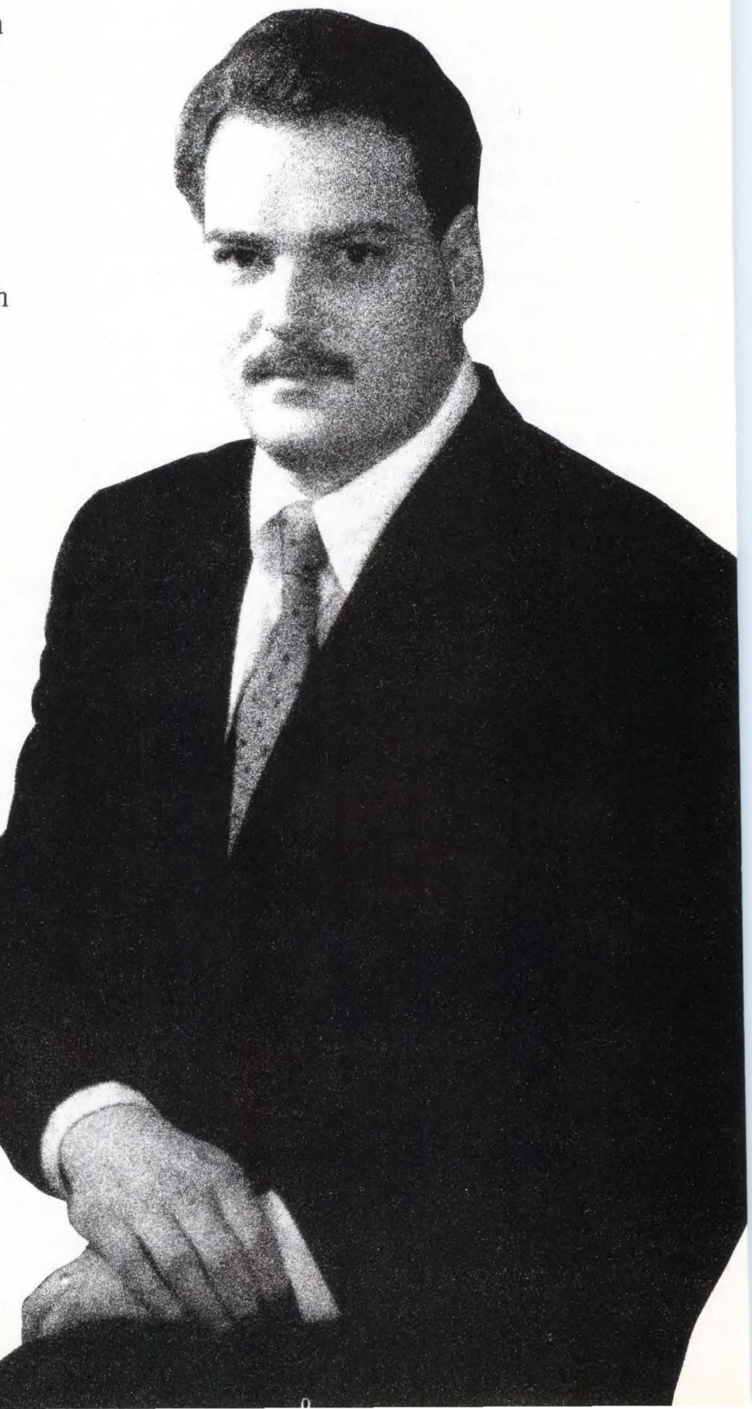
John R. Belden
Marketing Manager
Glassman High Voltage, Inc.

Glassman High Voltage designs and manufactures high-voltage DC power supplies with a difference. The most striking difference is that they're insulated with air, and contain no oil or potting compound.

Marketing Manager John R. Belden has watched Glassman grow from a small shop with a lot of innovative ideas to an industry leader. And EDN magazine and EDN NEWS have helped along the way. "The two publications get us the brand recognition and prestige we need," he says. "They go right to the engineers and engineering managers who make the buying decisions."

John Belden believes in the power of EDN magazine and EDN NEWS. So much so that he's relying on them to launch a series of new product lines. "EDN and EDN NEWS are sure to get them off the ground," says Belden. "No other pair of publications can provide the influence to deliver our message to as many markets, both geographically and demographically, in a cost-effective and timely fashion."



EDN magazine and EDN NEWS work for Glassman High Voltage. They can work for you.

EDN

Where Advertising Works

access the transfer routines from programs written in any of 18 languages that run under MS-DOS and support software interrupts—the latest additions to the list are Turbo Pascal 4.0 and QuickBASIC 4.0. You can transfer data between the IEEE-488 bus and the main memory, disk, or any other peripheral attached to the host computer. $125; upgrades from previous versions, $30.

Scientific Solutions Inc, 6225 Cochran Rd, Solon, OH 44139. Phone (216) 349-4030. TLX 466692. FAX 216-349-0851.

Circle No 416

DBMS WITH DEBUGGER

- *Allows interactive debugging of SQL-based applications*
- *Runs on IBM PC and PS/2 computers and compatibles*

The Informix-4GL Rapid Development System and Interactive Debugger is now available for systems that run the MS-DOS operating system. You write your database application in 4GL code; the development system compiles this code to pseudo-code for execution by a p-code interpreter that is included in the package. The debugger allows you to debug your 4GL code interactively. Your application can use as many as 16M bytes of extended memory. SQL-based applications created with the package will be portable to a number of larger machines that can run Informix. $1495.

Informix Software Inc, 4100 Bohannon Dr, Menlo Park, CA 94025. Phone (415) 322-4100. TLX 361834. FAX 415-322-4571.

Circle No 417

MS-DOS TOOLSET

- *Includes 10 language-independent utilities*
- *Facilitates the updating of multi-file software systems*

The Compiler Companion package consists of 10 utilities that can enhance the productivity of software engineers who use MS-DOS systems. All of the utilities except CXREF are language-independent, and you can use them with Basic, Fortran, Pascal, Assembler, or any other programming language. CXREF generates a cross-reference listing of C source files to help locate variables and function calls. Extract and Build help you to build batch files containing commands that operate on multiple files. The other utilities locate files, compare files, update the time/date stamps of multiple files, and search for and replace strings in multiple files. $100.

Lattice Inc, 2500 S Highland Ave, Lombard, IL 60148. Phone (312) 916-1600. TLX 532253. FAX 312-916-1190.

Circle No 418

CASE FOR OS/2

- *Provides structured-analysis and -design capabilities*
- *Runs on IBM PS/2 machines under the OS/2 operating system*

Teamwork-OS/2 bundles three of the vendor's CASE tools (previously available for workstations and IBM PCs) in a package that runs on IBM PS/2 Models 50Z, 60, 70, and 80 under the OS/2 operating system. Teamwork/SA lets you analyze and capture system requirements with the aid of structured-analysis dataflow diagrams, Teamwork/RT provides the notation needed for showing the relationships between asynchronous events in a real-time system, and Teamwork/IM provides the notation for information modeling. To run these tools, the PS/2 machine must have at least 4M bytes of main memory, 15M bytes of available disk space, a VGA or VGA-emulating monitor, a mouse, and the OS/2 standard edition version 1.0 or later. $4995.

Cadre Technologies Inc, 222 Richmond St, Providence, RI 02903. Phone (401) 351-2273.

Circle No 419

ANALOG F-O LINK

- *Stands voltages determined by optical cable to 40 kV*
- *Reproduces signals with 150-kHz bandwidth*

With appropriate high-voltage probes and fiber-optic cable, the ADTS-210 can pass analog signals across an isolation barrier that withstands common-mode voltages as high as 40 kV and 400 kV on special order. It works with glass-fiber cables as long as 2000m. Using V/F conversion techniques, the system achieves a signal bandwidth of dc to 150 kHz. An "expanded" mode increases bandwidth to 600 kHz and lets you measure the amplitude of pulses that would otherwise be too narrow for the system to handle. Nonlinearity is <0.5%; after autocalibration, gain error is <1% and offset is <5 mV. ADTS-210, $2950; cables to 2000m, $250 + $2.50/m; ADTS-200, including 12m plastic-fiber cable, $2900. Delivery, four to eight weeks ARO.

VG Controls Inc, 34 Jenkins Rd, Hewitt, NJ 07421. Phone (201) 853-4600.

Circle No 365

CALIBRATOR

- *Verifies its own calibration, using three devices*
- *Maintains 5 ppm dc-voltage uncertainty for 90 days*

The 5700A multifunction calibrator addresses a significant problem of calibrator ownership—calibrating the calibrator. The instrument produces direct and alternating voltages and currents, and acts as a resistance standard to 100 MΩ, yet it requires just two standard resistors and a 10V dc reference for its own calibration. As a direct voltage standard, absolute uncertainty is 5 ppm for 90 days at temperatures within 5°C of the calibration temperature. The unit produces voltages to 1100V and currents to 2.2A (20A with external amplifier). The frequency range is dc to 1.2 MHz at 22V; a wideband option extends this range to 30 MHz. $19,950.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853.

Circle No 366

Philips Test and Measurement, Building HKF, 5600 MD Eindoven, The Netherlands. Phone local office.

Circle No 367

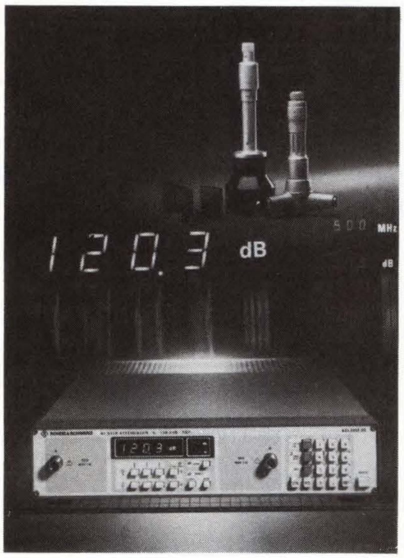
ASIC VERIFIER

- *Runs 560,000 200-pin vectors in <5 sec*
- *Clocks at 220 MHz and tests at 110 MHz*

The Topaz V ASIC-verification system features tester-per-pin architecture that allows separate definition of nine test parameters for each pin. These parameters include data format, comparison threshold, and timing. Currently, the vendor supplies the system in configurations to 320 pins and is developing a 554-pin upgrade. A very high-speed interface connects a 16M-byte (optionally, 64M-byte) RAM array to the pin electronics. This RAM can store as many as 112M vectors divided by the number of pins. The system can thus burst out 560,000 200-bit-wide vectors in <5 sec. The vendor claims that competitive systems require a minimum of several minutes to perform equivalent operations. The clock speed is 220 MHz max, the test rate is 110 MHz max, and the timing skew is ±500 psec max across all channels. $1000 to $1600/pin. Delivery, 90 days ARO.

Hilevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (800) 445-3835; in CA, (800) 541-2742. TLX 655316.

Circle No 368



RF ATTENUATOR

- *Operates from dc to 2.7 GHz*
- *Allows frequency-dependent error correction*

The Model-RSP RF step attenuator allows you to introduce precision losses of between 0 and 139.9 dB into a 50Ω signal line. It has a resolution of 0.1 dB and is suitable for operation at frequencies from dc to 2.7 GHz. To improve accuracy, the attenuator uses frequency-dependent error correction techniques. Using the instrument's integral IEEE-488 bus interface, you can interrogate the instrument to determine its attenuation error at a particular frequency so that you can calculate an appropriate compensation factor. The attenuator has a step switching time of ≤20 msec and a lifetime of greater than 10 million switching operations. Nonvolatile memory in the instrument allows you to store as many as 40 complete front-panel setups that you can then select via front-panel pushbuttons. The instrument is also fully programmable via its IEEE-488 interface. Around DM 18,000.

Rohde & Schwarz GmbH, Mühldorfstrasse 15, 8000 Munich 80, West Germany. Phone (089) 41290. TLX 523703.

Circle No 369

Rohde & Schwarz Inc, 4425 Nicole Dr, Lanham, MD 20706. Phone (301) 459-8800. TLX 510-223-0414.

Circle No 370

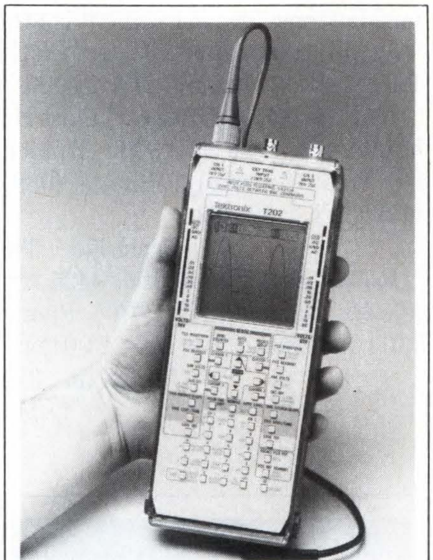
PC-BASED SCOPE

- *Digitizes two channels at 20M samples/sec*
- *Stores 128k words/channel*

The R2000M digital scope works in conjunction with an IBM PC or compatible computer. It operates as a 2-channel digital-storage oscilloscope with separate 8-bit A/D converters for each channel. The unit acquires data at rates from 1 sample/sec to 20M samples/sec, and it stores 128k bytes/channel. This combination allows the instrument to capture 6.4 msec of data on each channel at its maximum speed. The accompanying software can automatically save captured data on the computer's hard disk. You can switch the input impedance to 50Ω or 1 MΩ; and, using software, you can select sensitivities from 10 mV/div to 50V/div. Trigger modes include internal, external, digital, analog, pre, and post. The vendor also offers real-time FFT software and an IEEE-488 interface. $3995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No 371



HANDHELD SCOPES

- *Weigh less than 2 lbs including batteries*
- *Provide two channels with a 5-MHz bandwidth*

The T201 and T202 are handheld, 2-channel oscilloscopes. They measure 10×4½×2 in. and weigh less than 2 lbs each with batteries, probe, and carrying case. The units provide a 5-MHz bandwidth for repetitive signals and 2 MHz for single-shot transients. They sample at 20M samples/sec. The T202 offers a traditional oscilloscope interface with front-panel controls divided by function. The T201 controls operate more like calculator keys. The units' liquid-crystal displays present numeric as well as waveform data, enabling you to use the instruments as voltmeters and counters. The scopes store complete control setups and recall them. $1995.

Tektronix, Box 1700, Beaverton, OR 97077. Phone (800) 426-2200.

Circle No 372

WAVEFORM ANALYZER

- *Operates as 2-channel scope with 60-MHz bandwidth*
- *Indicates voltage, frequency, and time on LCD*

The SC61 waveform analyzer is a 2-channel oscilloscope with a bandwidth (−3 dB) of 60 MHz. It incorporates a 6-digit LCD that displays dc voltage from 2 to 2000V full-scale with 3½-digit resolution, p-p voltage from 8 to 2000V full-scale with 3⅘-digit (8000 count) resolution, and frequency from 1 Hz to 100 MHz with 6-digit resolution on most ranges. You can set the scope's vertical sensitivity from 5 mV/div to 200V/div (200 V/div requires a 10X probe). You can set sweep speed from 0.1 μsec/div to 0.1 sec/div. The counter's accuracy is 10 ppm ±1 digit from 15 to 35°C. The timebase aging rate is 10 ppm/year. $3295.

Sencore, 3200 Sencore Dr, Sioux Falls, SD 57017. Phone (605) 339-0100. TWX 910-660-0300.

Circle No 373

CAPACITANCE DMM

- *Features a 10 MΩ impedance*
- *Provides overload protection for five ranges*

The J380960 DMM lets you troubleshoot capacitance problems over five ranges. The DMM provides a 3½-digit LCD and consumes a 9V battery over a 150- to 200-hour operating life. Its dc voltage range includes 200 mV, 2, 20, 200, and 1000V. The DMM provides an accuracy of ±0.5% and ±0.8% at 200 mV and 750V, respectively. It features a 10 MΩ impedance and provides an overload protection, for dc and ac, of ±1100 and 800V, respectively. The unit measures 7.125×3.375×1.375 in. and weighs 11.5 oz including the battery. The unit comes with a pair of test leads and a 9V battery. The vendor offers in-circuit test leads as optional equipment. $89.

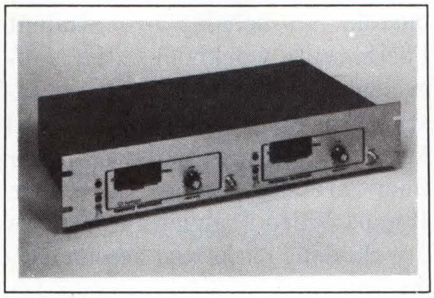
Extech Instruments Corp, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440.

Circle No 374

DUAL SYNTHESIZER

- *Includes two independent 5½-digit sections*
- *Covers 0.1 Hz to 16 MHz*

The DS-102 is a rack-mountable unit containing a pair of independent frequency synthesizers that cover 0.1 Hz to 16 MHz with 5½-digit resolution. The frequency reference is stable to within ±10 ppm from 0 to 50°C. The unit has TTL-compatible outputs capable of driving 50Ω loads. $1485. Delivery, 45 to 60 days ARO.



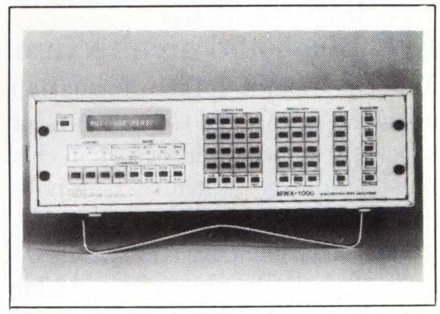
Syntest Corp, 40 Locke Dr, Marlboro, MA 01752. Phone (508) 481-7827. FAX 617-481-5769.

Circle No 375

ESDI DRIVE TESTER

- *Lets you test 760M-byte Winchester drives*
- *Writes and reads media-defect maps*

The MWX-1000E lets you test 760M-byte max Winchester drives. Accommodating all types of ESDI drives, this model can handle 5- and 10-MHz drives with data-strobe and



track-offset functions. The analyzer lets you perform read, write, seek, and other tests. In addition, you can read, write, update, protect, and locate media-defect maps. An optional proprietary card allows you to read data-window margins. The vendor offers multiport capabilities, additional analog test tools, and remote control, using a proprietary hardware/software system. $9983.

Wilson Laboratories Inc, 2237 N Batavia St, Orange, CA 92665. Phone (714) 998-1980. TLX 181598.

Circle No 376

Brochure sums up STE Bus board architecture

You can find helpful information about STE Bus (IEEE 1000) 8-bit processor-board architecture in this illustrated 6-pg brochure. The publication contains charts and diagrams that compare the performance of the STE Bus with a 16-bit bus. It also includes information about the STE Bus's ability to handle multiple masters. Further, the booklet describes the processing of interrupts, and how the device allows priority to be determined without the use of daisy chaining or device-dependent timing constaints.

STEMUG-US, Box 7529, Newark, DE 19714.

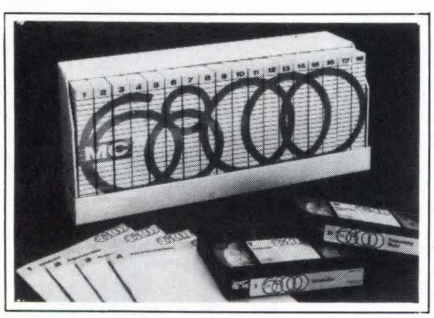
Circle No 420

Guide for designers of embedded systems

The *Guide to Embedded Languages* addresses the tradeoffs involved in embedding a language. This reference for engineers examines the characteristics of ROMable languages, interpreter/compiler tradeoffs, interactive development, and multitasking from within the language. It also contains a discussion of a real case study.

Softaid Inc, 8930 Route 108, Columbia, MD 21045.

Circle No 421



Video series teaches use of MC68000 μP

The MC68000 Video Training Series (MTTV2) for the MC68000 microprocessor is organized into 18 modules with one videotape per module. It includes five Student Packs with workbooks and self-evaluation material. An optional Instructor Pack and an optional MC68000 Educational Computer Board are also available. Complete 18-tape Video Training Series with five Student Packs and accompanying material, \$9000; optional Instructor Pack, \$175; Educational Computer Board, \$495.

Motorola Inc, Training & Technical Operations, 1140 S Priest Dr, Tempe, AZ 85281.

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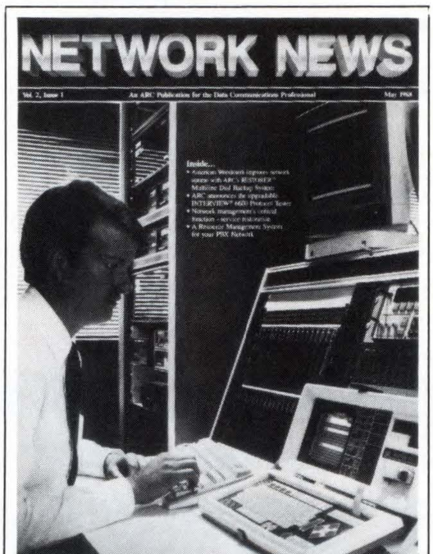

Newsletter for datacomm/telecomm users

This quarterly newsletter, *Network News*, informs data-communications users about the latest time- and money-saving restoration and analysis techniques being used in networks around the globe. Focusing on the vendor's most recent product developments, the third edition features the Interview 6600 protocol tester, a line of network restoration systems, the Artacs PBX management system, and the training courses offered by the company.

Atlantic Research Corp, Teleproducts Div, Marketing Communications, 7401 Boston Blvd, Springfield, VA 22153.

Circle No 422

Pamphlet features precision op amps

The vendor's 8-pg Precision Operational Amplifier Selection Guide presents more than 50 device types. It summarizes performance specifications, packaging information, and MIL-STD-883B availability of the op amps.

Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043.

Circle No 423

Pocket-size guide for fiber-loss measurements

The vendor's 20-pg PG-160 Pocket Guide, *Fiber Loss Measurements with the Intelco 160A*, describes the two most commonly used fiber-cable-loss measurement methods—the stored cross-reference method and the calibrated output power method. The guide also contains step-by-step procedures and figures to illustrate the test setups.

Intelco Corp, 8 Craig Rd, Acton, MA 01720.

Circle No 424

UTX/32 version of Unix explored

The company's brochure describes how UTX/32 provides the standard benefits of Unix, including protection of users' software investments, a wide range of applications software, transparent communications between heterogeneous computer systems, and compatibility with numerous hardware architectures. The publication also explains how the UTX/32 incorporates the advantages of the company's experience in designing real-time computer systems.

Gould Inc, Computer Systems Div, Box 409148, Fort Lauderdale, FL 33340.

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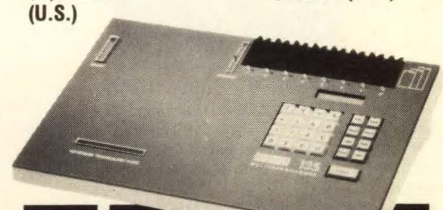

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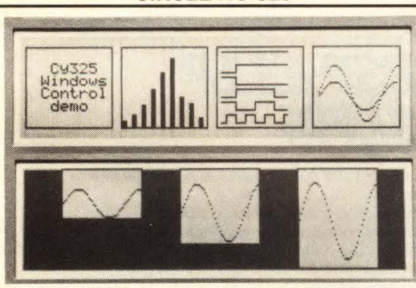

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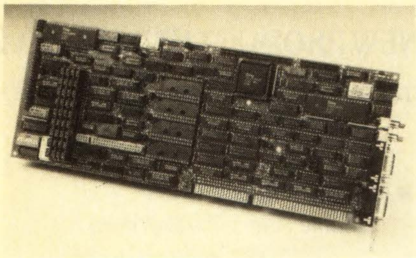

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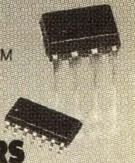

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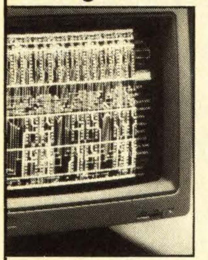

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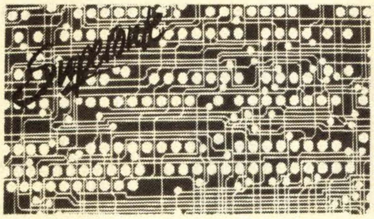

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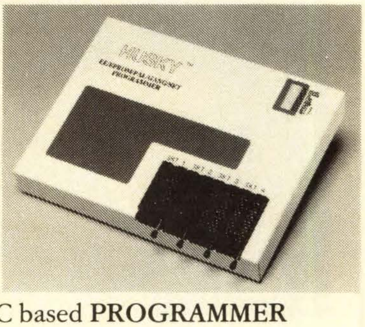

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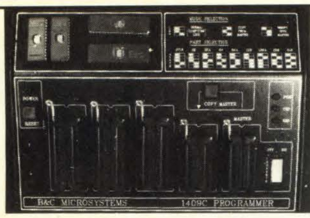

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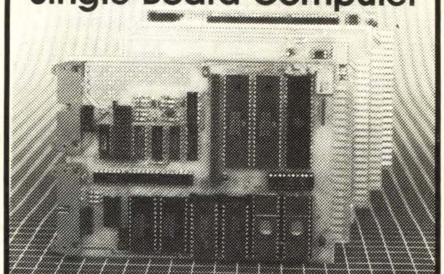

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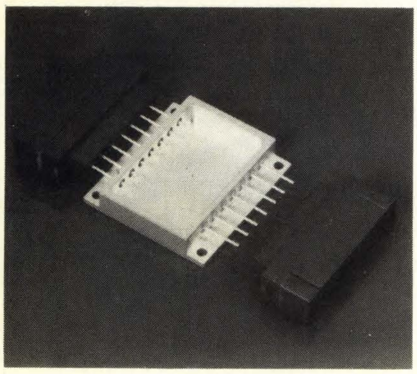

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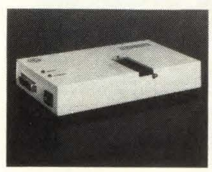

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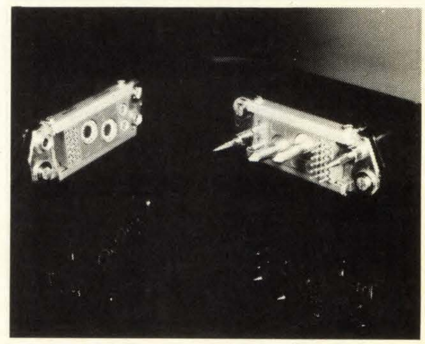

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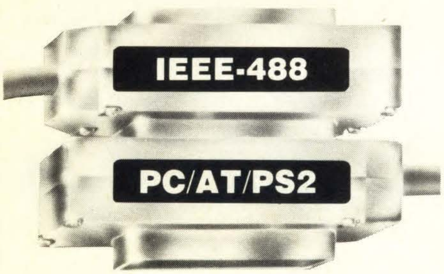

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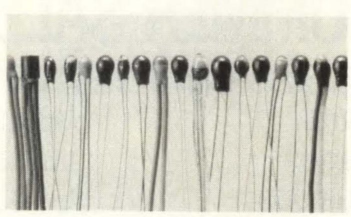

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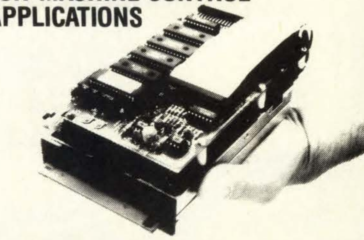

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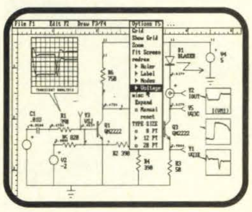

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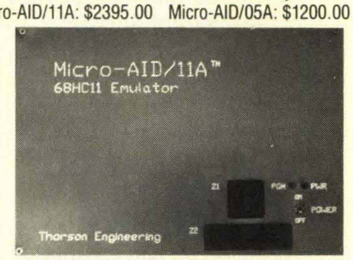

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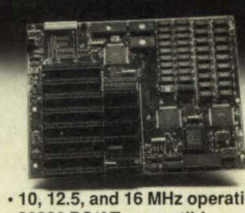

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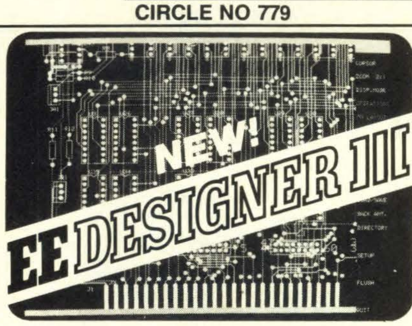

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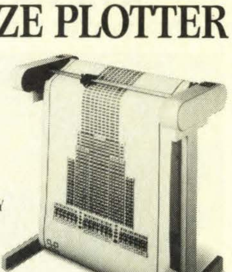

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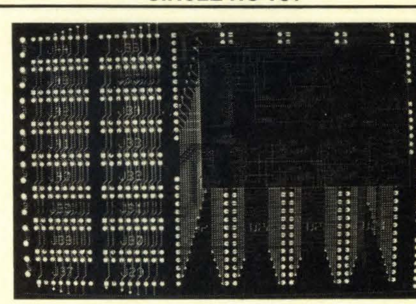

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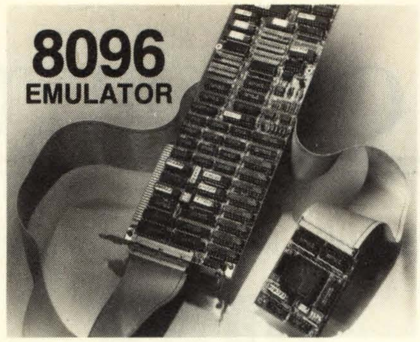

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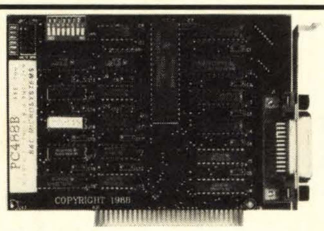

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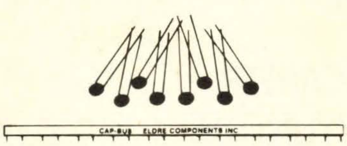

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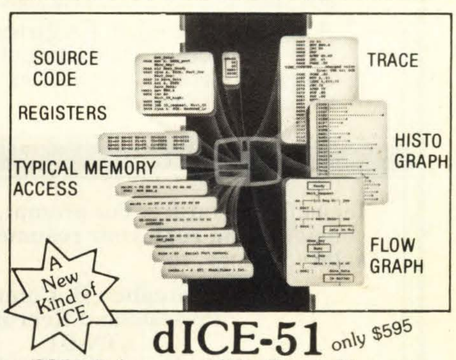

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Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Oct. 27	Oct. 6	CAE, Computers & Peripherals, Integrated Circuits, Wescon '88 Show Preview	
Nov. 10	Oct. 20	Programmable Logic Devices, Integrated Circuits, Test & Measurements, Wescon '88 Show Issue	Closing: Oct. 27 Mailing: Nov. 17
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
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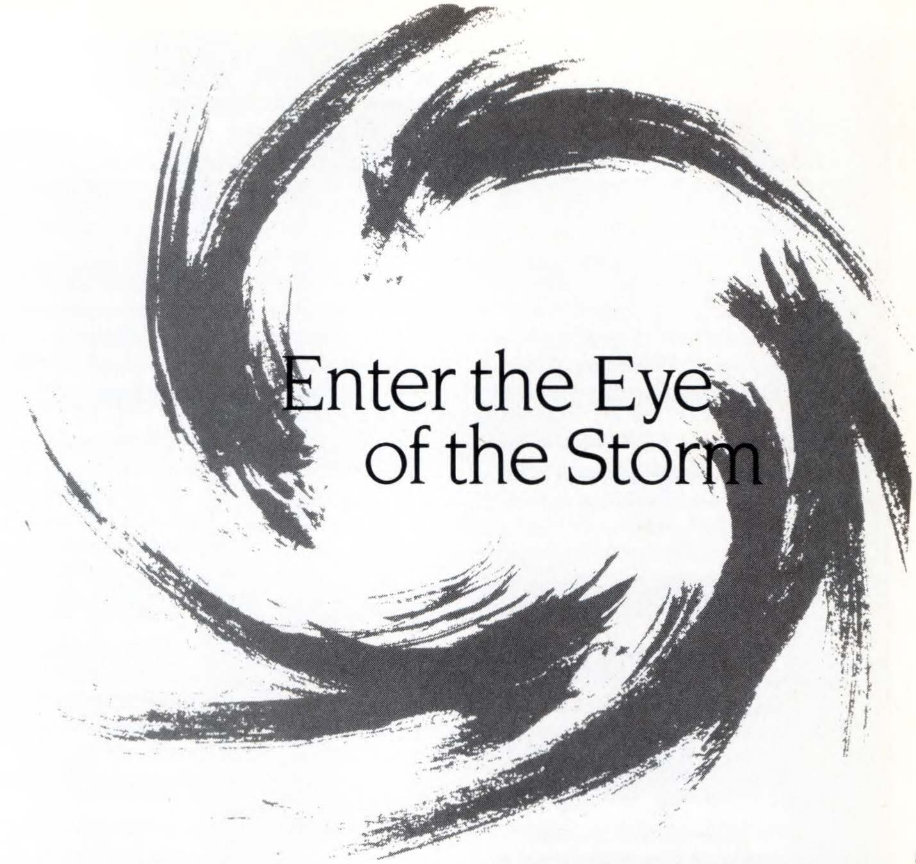

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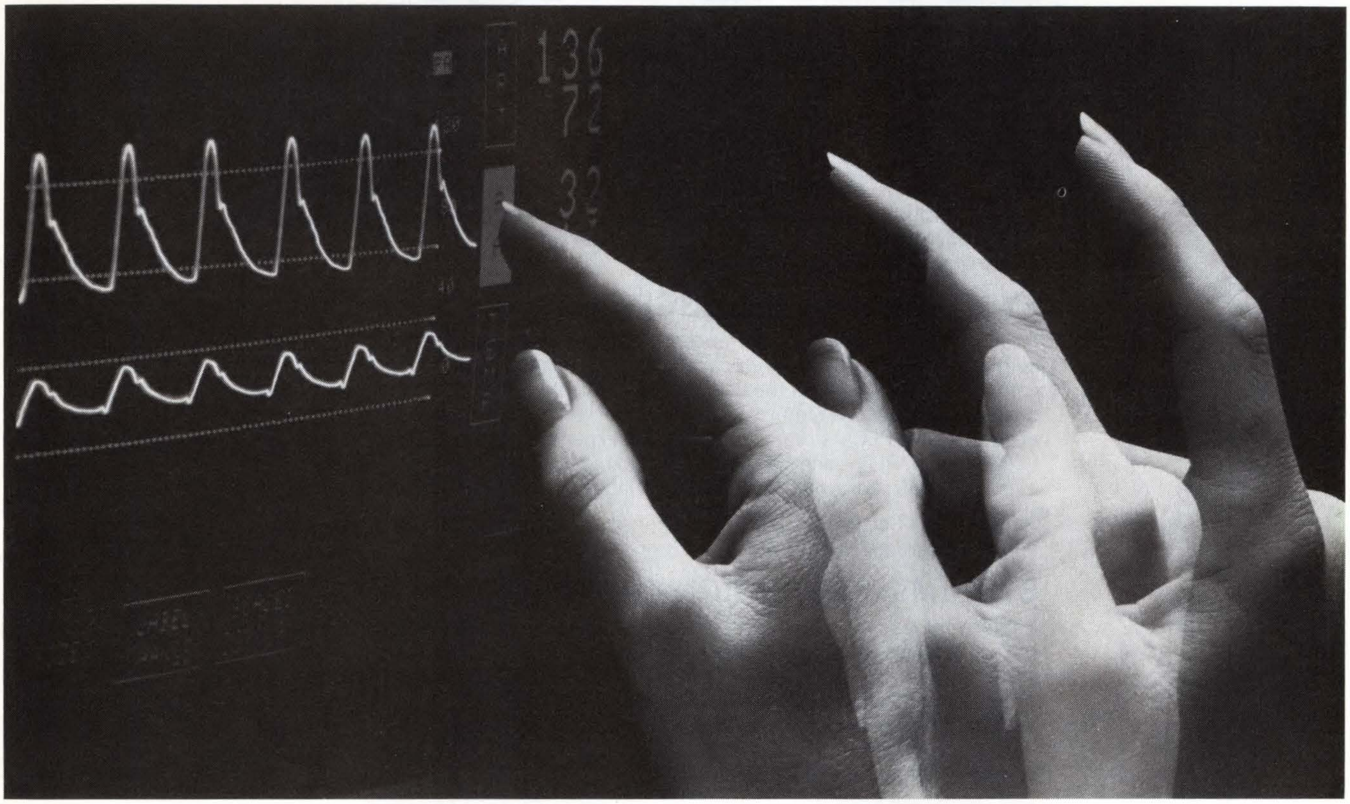

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EDITED BY CYNTHIA B RETTIG

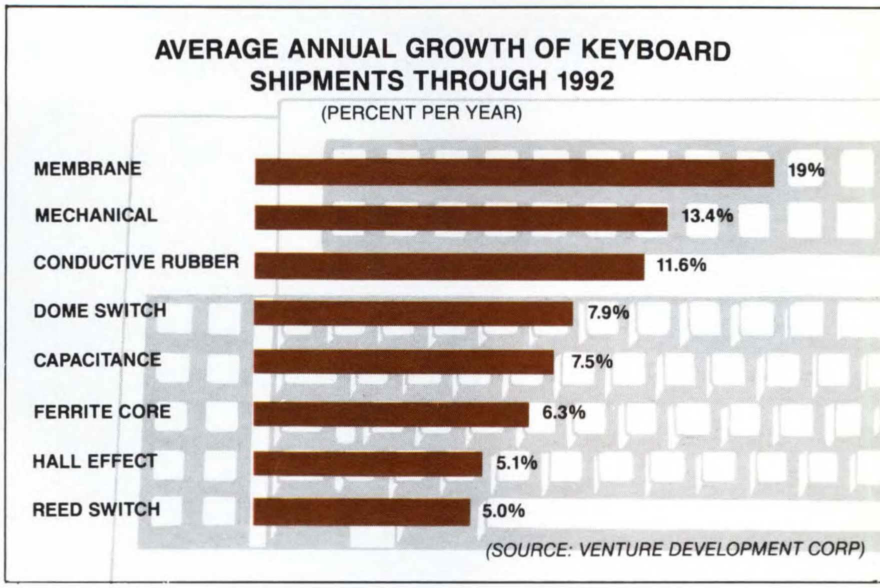
Keyboard market will see solid growth through 1992

The market for keyboards, including full-travel, short-travel/micromotion, and flat-panel devices, should reach $1.6 billion by 1992, up from an estimated total of $990 million for this year, according to Venture Development Corp (Natick, MA). However, the demand for full-travel keyboards is not expected to keep up with the markets for other kinds of keyboards.

The principal markets for full-travel keyboards will remain data processing and office automation, where speed is most prized. Average annual growth in the consumption of keyboards by data processors, for example, will continue to be about 15%. A driving factor behind this growth rate will be a higher demand for personal computers.

For durability and reliability, keyboard buyers are favoring membrane, mechanical, and conductive-rubber keyboards, which are relatively inexpensive. Instrumentation and industrial-control areas will continue to create the primary demands for short-travel/micromotion and flat-panel keyboards, which generally fare well in harsh environments. The market for these two types of devices is expected to grow at an annual rate of 17%, producing revenues of $311 million this year. Membrane keyboards should grow at an annual rate of 19%.

VDC characterizes the current market for short-travel and flat-panel keyboards as a custom market, where technology, flexibility, communication, service, turnaround time, and delivery are all key factors. Manufacturers are now steadily and successfully developing new products in these areas on a regular basis. Short-travel and flat-panel devices are also replacing traditional keyboards in equipment, controls, instruments, and appliances that require only low-speed and low-usage data entry.



Some trends are also discernable for full-travel keyboards. Manufacturers have focused their efforts on low-profile, stand-alone, fully enclosed keyboards. The DIN standard now rules in the market for ergonomically designed keyboards. The detachable or stand-alone keyboard with its own case and cable has also become an industry norm. OEMs continue to take advantage of the cost savings that result from reduced shipping, handling, and packaging charges associated with full-travel keyboards enclosed with cases and cables. Fully encoded keyboards are also becoming quite popular in full-travel devices.

Signal-analyzer revenues will top $5B in 1993

During the next six years, the signal-analyzer market is expected to be the strongest segment of the test and measurement market, reaching a worldwide sales figure of over $5 billion by 1993, according to the Market Intelligence Research Co of Mountain View, CA. The need for faster and more reliable equipment, along with the basic growing need for signal analysis, will fuel the market. Improvements in the computer and semiconductor industries will also help. The use of signal analyzers is expected to broaden, invading the production floor, the telecommunications industry, and the military to a larger extent than ever.

MIRC divides the market into seven segments: oscilloscopes, spectrum analyzers, logic analyzers, network analyzers, waveform analyzers, protocol analyzers, and communications-impairment analyzers. The company expects protocol analyzers, digital oscilloscopes, and lower-priced logic analyzers to enjoy particularly strong growth during the forecast period. The revenues, for example, for analog and digital oscilloscopes should reach about $1.9 billion in 1993.

The US will continue to dominate the market, although MIRC predicts a slump during 1989 and 1990. Asian markets, however, will grow at the fastest rate during the forecast period. Hewlett-Packard and Tektronix will continue to lead in the market.

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	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	150	190	290	365	460	520	570	660	720

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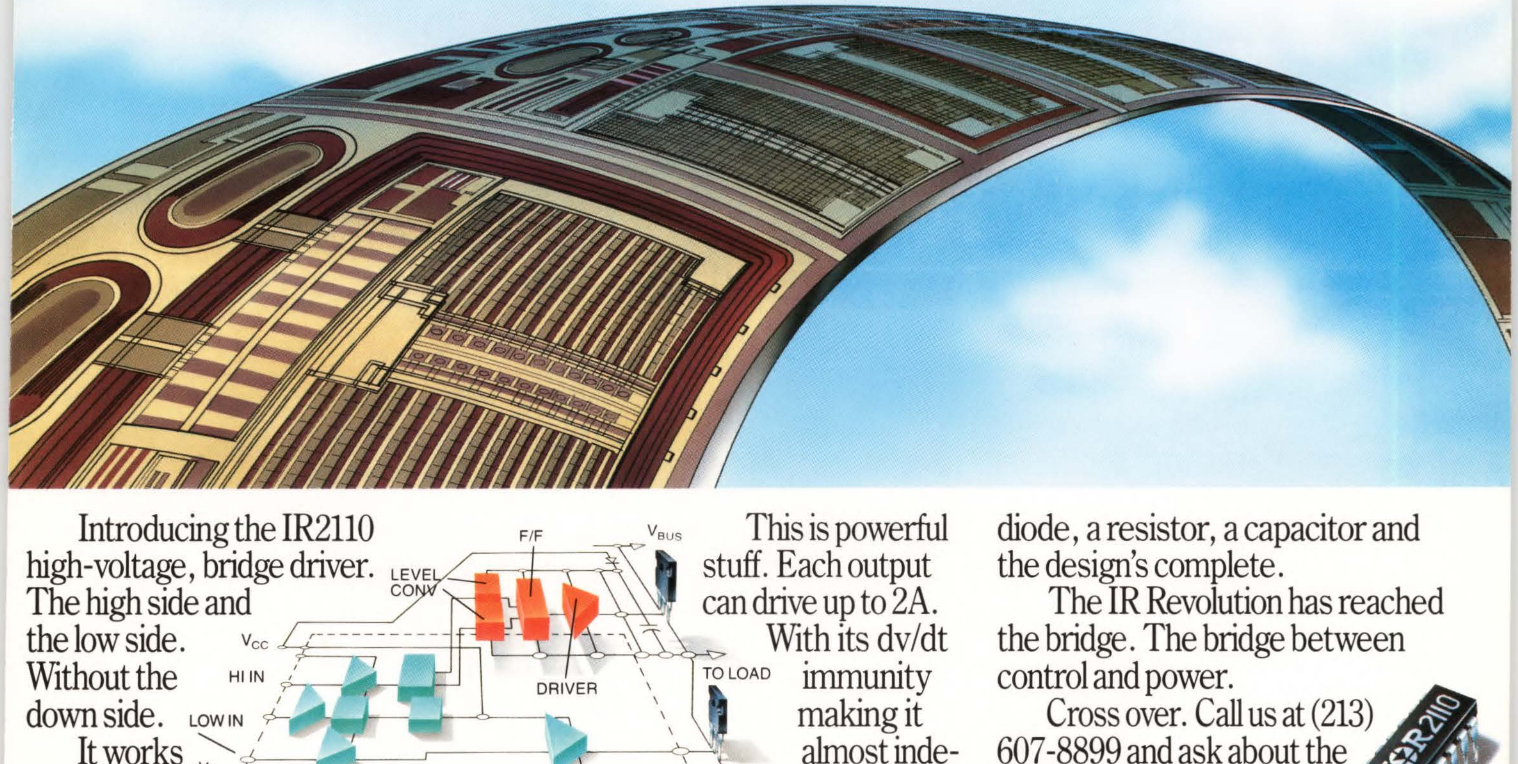

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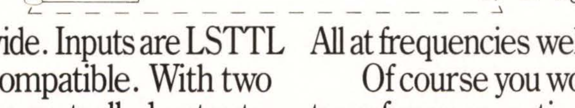

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