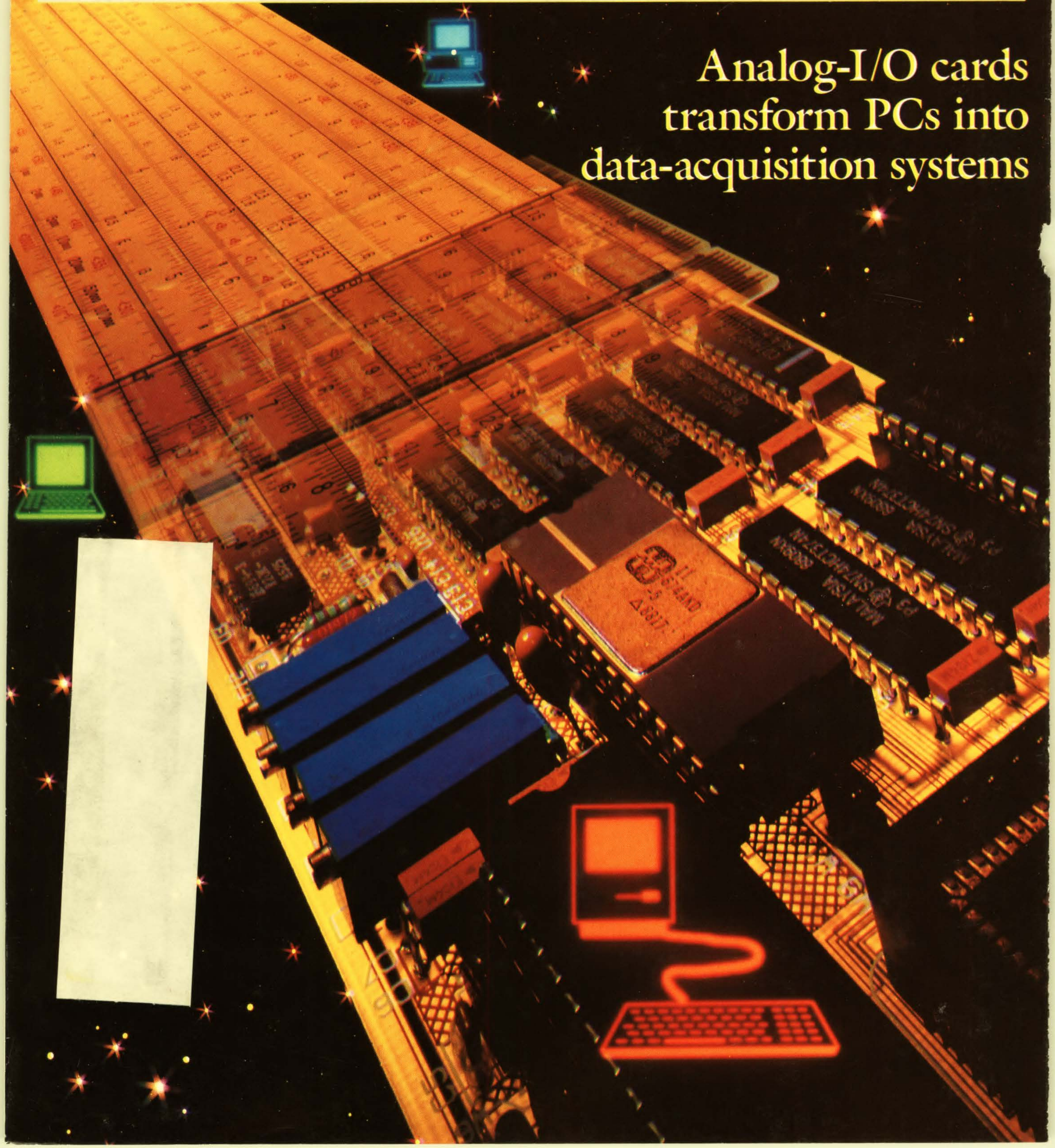
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS
A CAHNERS PUBLICATION

EDN®

MAGAZINE EDITION
SEPTEMBER 15, 1988

Analog-I/O cards transform PCs into data-acquisition systems



Devices' 29K.
platform.

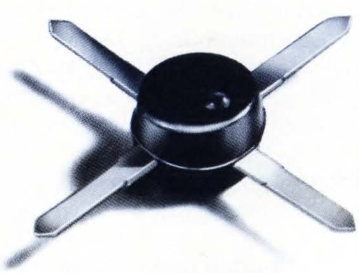
Advanced Micro
The next

42,000 dhrystones with a single 32-bit RISC chip. Sustained. Seventeen MIPS. Real world MIPS. 25Mhz clock speed. Fifty MIPS by 1991. Blazing fast even with low-cost memory. 5x the system throughput of the 68030. 2x the 80960 at half

the system cost. In CMOS. On the shelf. Now.

from

99¢



dc to 2000 MHz amplifier series

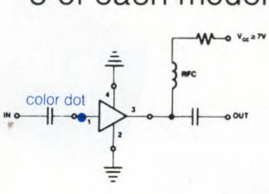
SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers
only $59.95



Unbelievable, until now...tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 100 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047, .068, .1μf

† Minimum Order 50 per Value

finding new ways...
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

CIRCLE NO 106

C113-Rev. D

tiny SPDT switches

absorptive... reflective

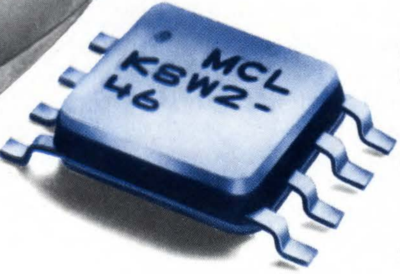
dc to 4.6 GHz from $32.95 (1-24)

Tough enough to pass stringent MIL-STD-883 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

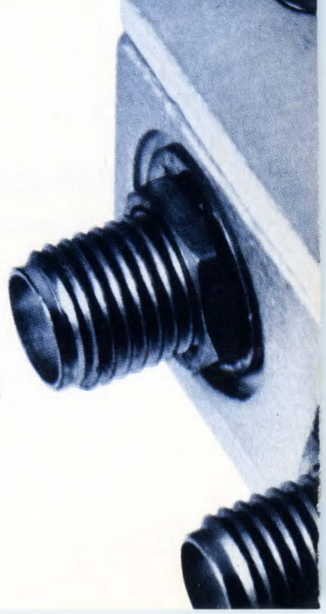
Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.



SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	**-5V** on, OV off		**-5V** on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (1-24)	**$32.95**		**$48.95**	
	$72.95		**$88.95**	



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setting higher standards

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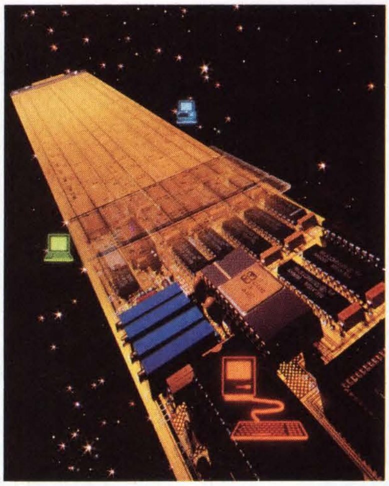
EDN

Magazine Edition

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:** The list of suppliers of analog-I/O cards for personal computers is expanding in response to the acceptance of PCs in the engineering workplace. See pg 150. (Photo courtesy Data Translation Inc)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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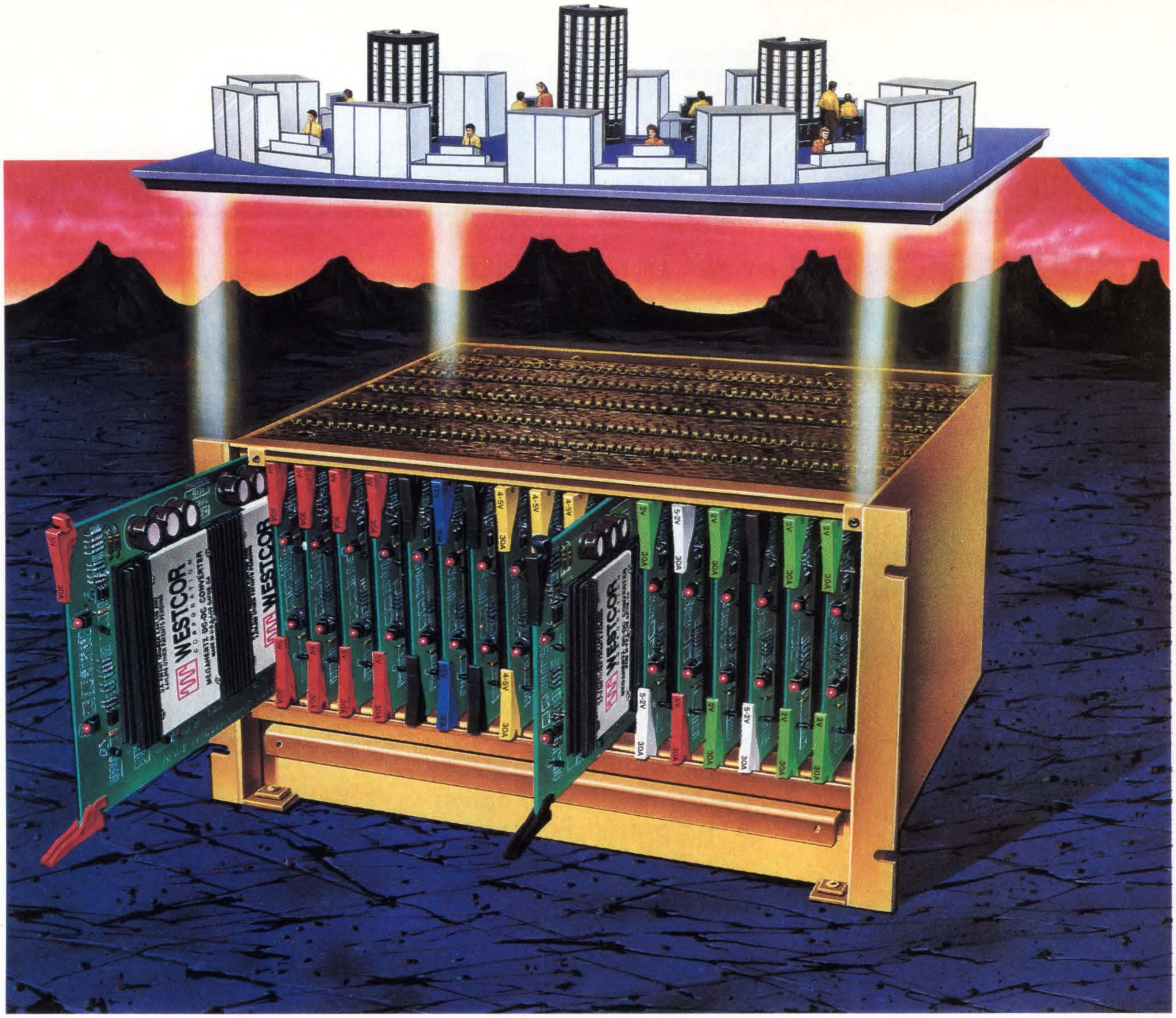

A NEW WORLD OF HIGH POWER FLEXIBILITY

Westcor's PowerCage™ and PowerCards™ comprise a modular power supply system of galactic power (7200 watts max.), flexibility (36 outputs max.) and efficiency (80% typ.). More like an expandable computer mainframe in design and concept than a standard high power supply, the PowerCage offers space-age alternatives to users of outdated 5x8x11 inch box switchers.

Measuring 19x10.5x11.25 inches deep the PowerCage fits into a standard NEMA rack and powers 18 slots for single or dual output PowerCards or dummy cards. PowerCage backplanes provide connections for easy configuration by the user.

Low profile (.8″) PowerCards supply single outputs from 2 to 75 VDC at up to 400 watts (outputs from 2 to 5 VDC limited to 60 amperes). Dual output cards source two isolated outputs each at half of the above ratings. Single output cards can be paralleled with current sharing to provide kilowatts via simple backplane configuration.

The nucleus of each PowerCage system is Westcor's patented 1 MHz, high power density, high reliability converter. Consider these benefits and features: 208 VAC 3 phase input; remote/local sense on all outputs; TTL power good signal and status LED's; designed to meet UL, CSA and VDE safety requirements; TTL inhibit; over-temperature, over-current, over-voltage protection; "hot" card insertion; full power at 50°C.

Future options include: DC input; IEEE-488 programmability; fault tolerant operation and battery backup. To discover a new world of high power flexibility, please contact us.

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CIRCLE NO 108

Continued from page 5

***Brushless dc motors** have always boasted many advantages; one disadvantage, though, has always been cost. Today, the cost differential between brushless and brush-type dc motors has decreased (pg 69).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request

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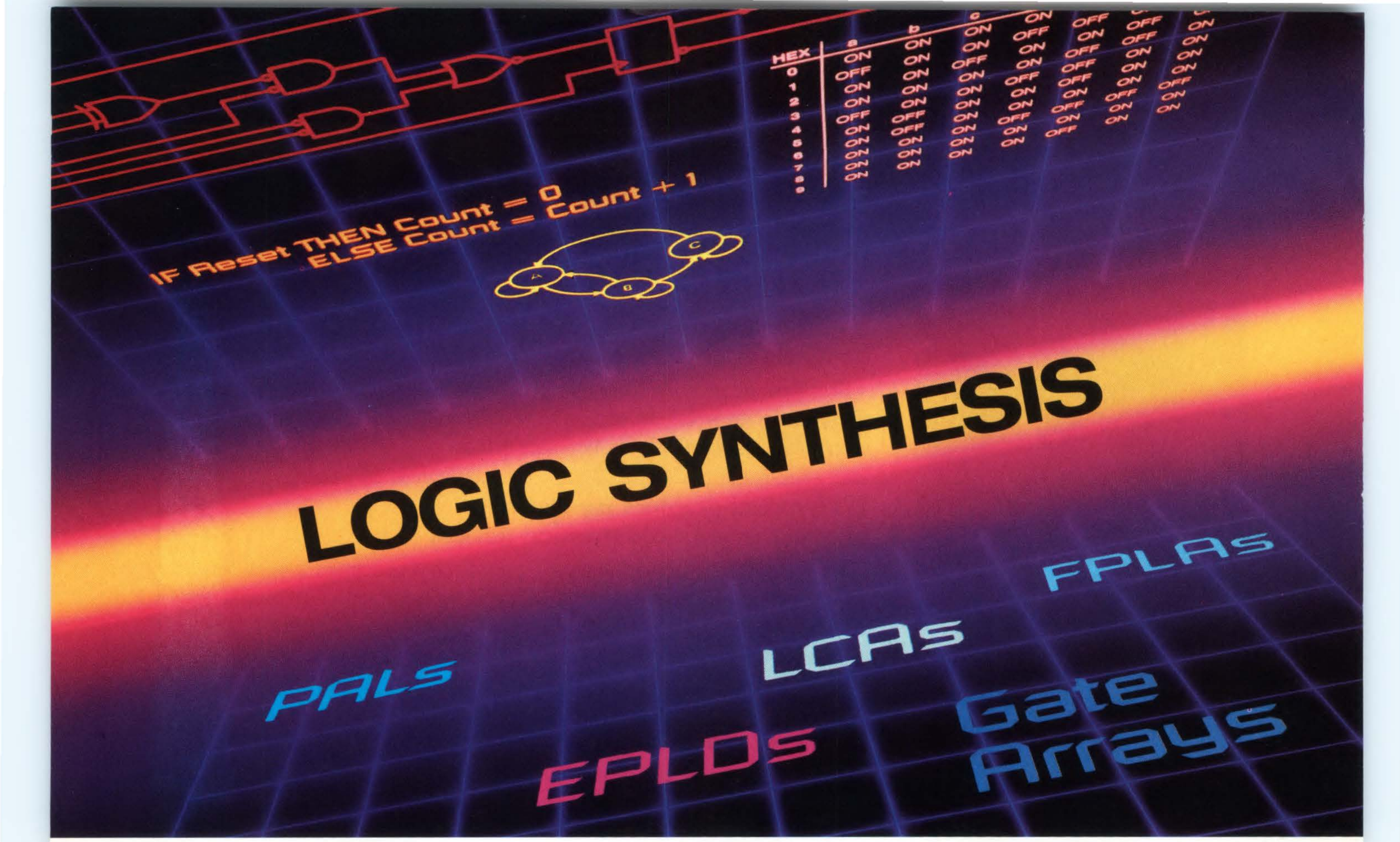

LOGIC SYNTHESIS GIVES YOU MORE DESIGN CHOICES.

FutureDesigner™ gives you more choices than any other design entry software—choices in how you enter your design, in target technologies, and in design output. And only FutureDesigner uses logic synthesis to automatically turn your input choices into your output choices, optimizing and streamlining your design for the technology you select.

CHOOSE THE DESIGN ENTRY METHOD. Only FutureDesigner lets you describe your design in the easiest, fastest, most natural way. You can enter some functions structurally, using DASH schematics. Others can be described behaviorally with any combination of truth tables, state diagrams, or high-level logic equations. Interactive verification and design rule checking help you catch errors up front, as you design.

CHOOSE THE TARGET TECHNOLOGY. FutureDesigner is technology independent. After you've described your design, you can choose any mix of TTLs, PLDs, LCAs, gate arrays, or other ASIC devices for implementation. It's also easy to migrate designs from one technology to another—for example, from TTL to PLD, PLD to LCA, or PLD to gate array.

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CIRCLE NO 109

Continued from page 7

EDITORIAL

To understand the words and phrases that marketers use, you need a translation guide.

NEW PRODUCTS

LOOKING AHEAD

Logic-design automation is ready for takeoff.

DEPARTMENTS

SIGNALLING A NEW ERA

THE IMS A100 CASCADEABLE SIGNAL PROCESSOR

Using pulse compression to improve range resolution, a modern radar system compares signals transmitted to and reflected from a target.

A typical system may use a pattern 512 samples long, collected at a data rate of 2.5 MHz.

This requires more than a billion multiplications a second!

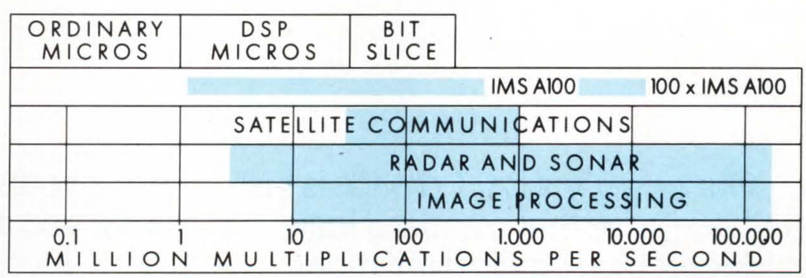
Yet the INMOS A100 Cascadeable Signal Processor enables a pulse compressor with this capability to fit a circuit board half the size of a typical PC card and dissipates less than 30 Watts.

A combination of performance, low power dissipation and reduced board area that means significant reductions in systems costs. Equally impressive results are found in applications such as beamforming, filtering and image processing.

Whatever DSP area you are in the INMOS IMS A100 processor is the only serious contender.

The following features show why the IMS A100 signals a whole new era in DSP. If you would like more information, clip the coupon today.

- Full 16 bit, 32 stage, transversal filter
- 36 bit internal precision
- Block floating point support
- Complex number support
- Easy to control from most ordinary and DSP microprocessors
- Data throughput to 10 MHz
- Power dissipation 1.5 Watts
- Fully static CMOS implementation
- 84 pin Ceramic PGA and Cerquad Packages
- MIL-STD-883C processing available



IN DSP.

inmos

INMOS, P.O. Box 1600, Colorado Springs, Colorado 80935. Tel. (719) 630-4000.

Orange County – 714-957-6018
Baltimore – 301-995-6952
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Santa Clara – 408-727-7771
Atlanta – 404-242-7444
Dallas – 214-490-9522
Minneapolis – 612-932-7121
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Please send me information on the INMOS DSP family. My main area of interest is

Sonar ☐ Comms ☐ Radar ☐ Imaging ☐ Other (please specify) ____

EDN091588

Name ____ Title ____

Company ____ Address ____

____ Zip ____ Tel ____

CIRCLE NO 110

How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

It's also fast enough to finally let today's new microprocessors run at the speeds for which they were designed—breathtaking.

Raising your standard.

How fast would you like your standard logic?

How about faster than any TTL logic around? Even FAST™ or AS? You've got it with the 7.5ns PAL device.

And the fact that you can configure it yourself means you can get exactly what you want.

If you want to redesign something, you change the PAL device. Not the board.

7.5ns PAL Device vs. FAST & AS

SSI/MSI		FAST	AS	7.5ns PAL Device
Combinatorial				
74138	tPD	8.0	10.0	7.5
Decoder				
74151	tPD	11.0	15.0	7.5
Mux				
Register/Latch				
74374	tCO	10.0	9.0	6.5
Octal Register				
74373	tPD	8.0	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
Eight bit Ctr	tCO	10.0	11.0	6.5

Not only is this the fastest way to get high speed logic, it's also the most practical. One 7.5ns PAL device replaces two to six standard TTL devices.

Which cuts down on board size.

And cuts down chances for a device failure.

st get faster.

What to give the microprocessor that has everything.

We suggest the first PAL device that can keep up with it.

The 7.5ns PAL device runs at 74 Mhz. It can deliver the speed the new high performance microprocessors need.

Processors like the 29K, the 386 and the 68030.

This PAL device delivers 25% more speed than any other PAL device.

We even have the fastest 22V10.

Our 15ns 22V10 runs at 50Mhz. That's 10ns faster than anyone else on the market. And it lets you run at twice the rate of the new 25Mhz microprocessors.

We've been shipping 20 pin 10ns PAL devices for eighteen months. And now you can get the new 24 pin 10ns PAL device as well.

There's plenty of service and support to get and keep your project moving. And all our fast PAL devices are available in volume when you need them. Now, for example.

For all the facts about our fast PAL devices, drop us a line. Or call us at (800) 222-9323.

Because you can never be too fast.

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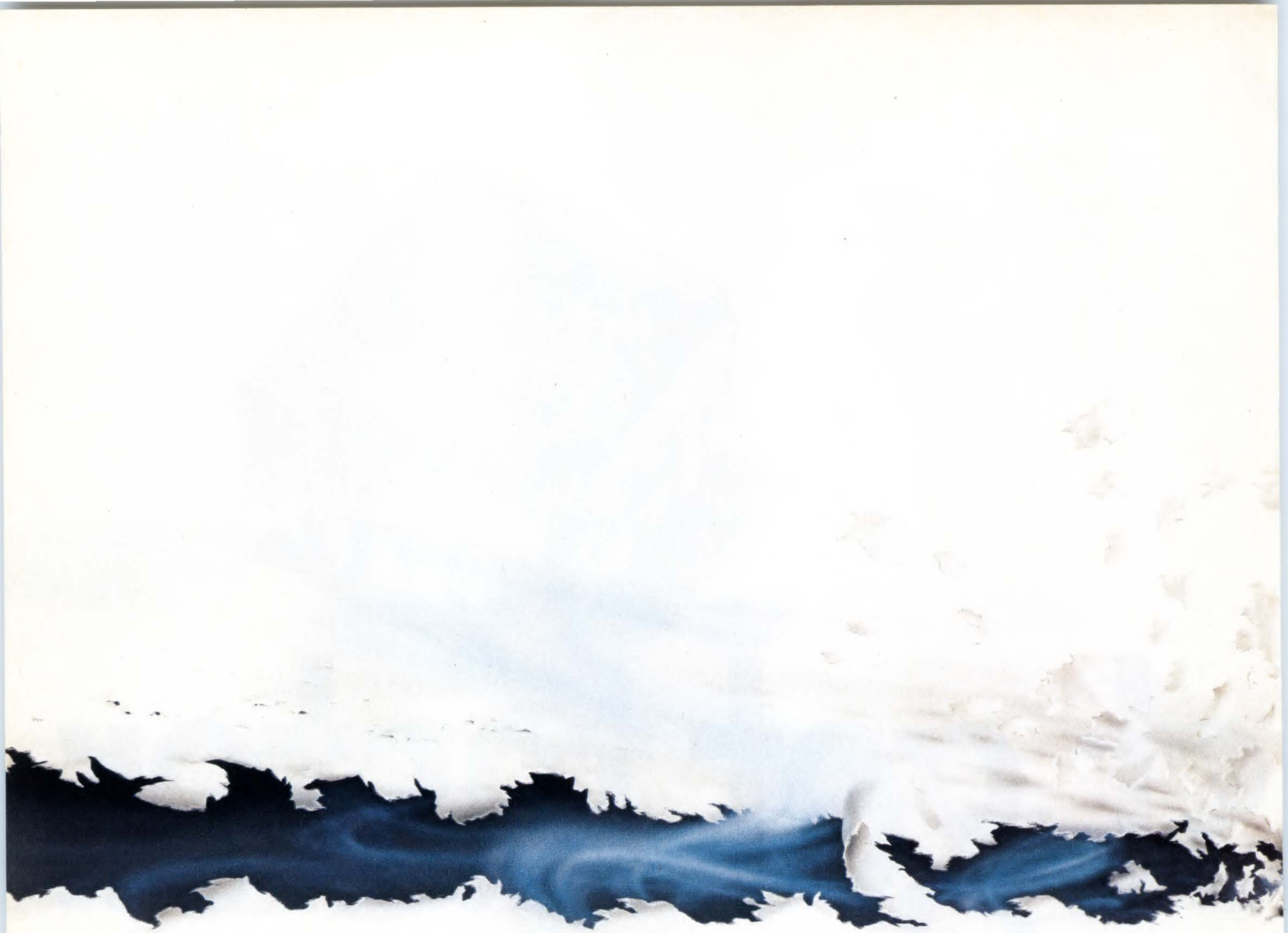


Only HP can put real teeth into faster

Test development and execution speed. We know they're your top priorities. HP BASIC,* combined with our range of controllers and instrumentation, is the answer. Even if you're running on MS™DOS or the UNIX™ operating system. And of course, it's all backed by HP's measurement expertise, and the product reliability you've come to count on from an industry leader.

HP BASIC: Optimized for instrument control.

It's no secret that a critical element of automated instrument control is fast development time. That's where HP BASIC really shines. With power, versatility and ease of use. We invite you to find a better instrument control language.

A few examples:

- Fast program development with interactive editing, syntax checking and the ability to search and replace strings, or move blocks of code easily.
- Optimized for I/O with advanced constructs to simplify otherwise complex tasks. Interrupts, high speed data transfers, automatic data formatting and branching on events can all be handled easily. Since HP BASIC was designed for instrument control, these capabilities are integral, not tacked on as an afterthought.
- Structured programming lets you make your program modular with independent subprograms which can be re-used in other applications. Constructs like CASE statements, IF-THEN-ELSE, WHILE, REPEAT-UNTIL and LOOP are useful for rapid program development and invaluable for program maintenance.
- Powerful computation lets you take advantage of a full range of matrix manipulations such as multiplication, inversion and scalar operations. HP's complex number implementation allows for powerful arithmetic operations.
- Graphic capabilities are simple to program, yet powerful. One program statement can draw axes or grids, a second will plot your data, a third will label your plot and a fourth will provide a permanent copy.

HP Controllers: The right horsepower for the job.

Hewlett-Packard provides a wide range of instrument controllers and operating systems to meet your performance needs, allowing you to choose the most cost effective controller for your job.

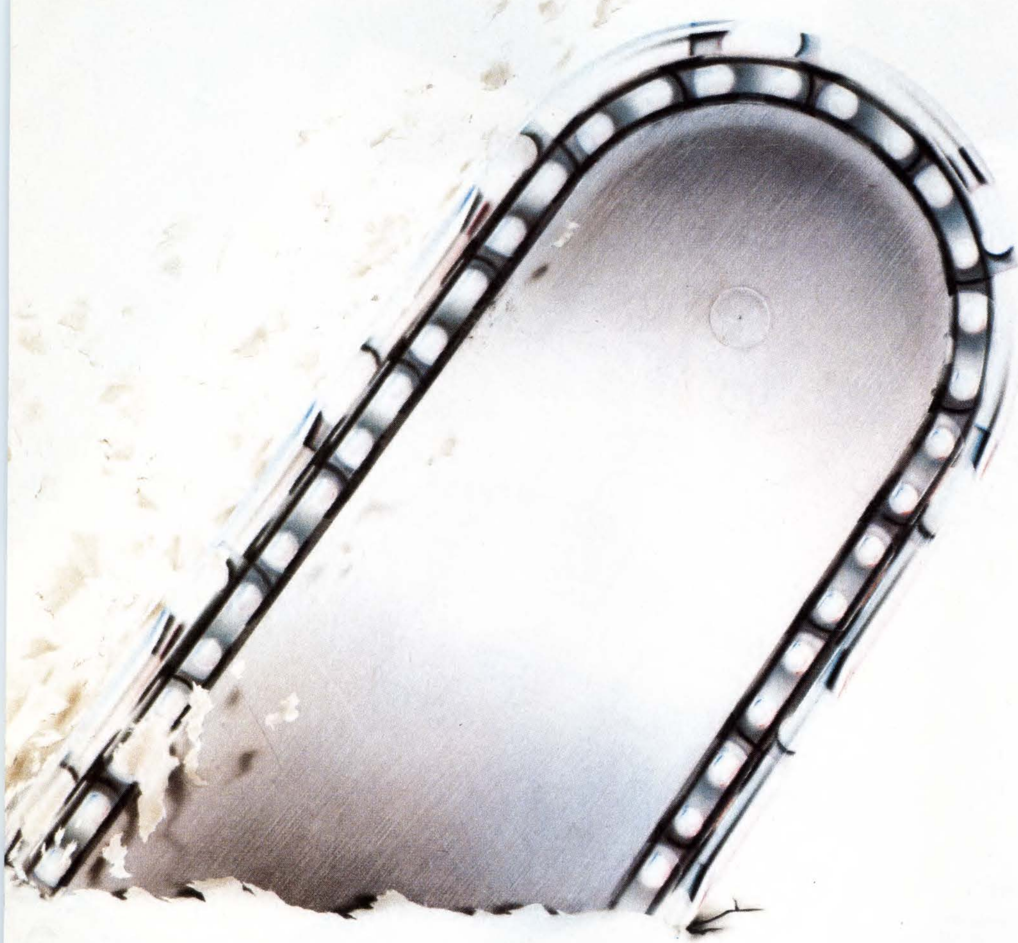
Just look:

- Personal computers; the HP BASIC Language Processor allows you to use HP BASIC on the world's most prevalent operating system, MS DOS. It's available for the HP VECTRA or the IBM PC-AT.

*Sometimes called Rocky Mountain BASIC or BASIC 5.0.

we never stop asking

"What if...



test development.

■ Dedicated controllers up to 4 MIPS. HP's Series 300 controllers provide a dedicated, high performance system for maximum I/O throughput.

■ HP-UX workstations. HP BASIC will also be available for use in the Series 300 HP-UX environment. Our implementation combines the ease-of-use and performance of HP BASIC with the full networking, multitasking and windowing capabilities of the UNIX operating system.

No matter the controller demand, HP makes it in the optimum package.

Trim more time: Deal with the pros.

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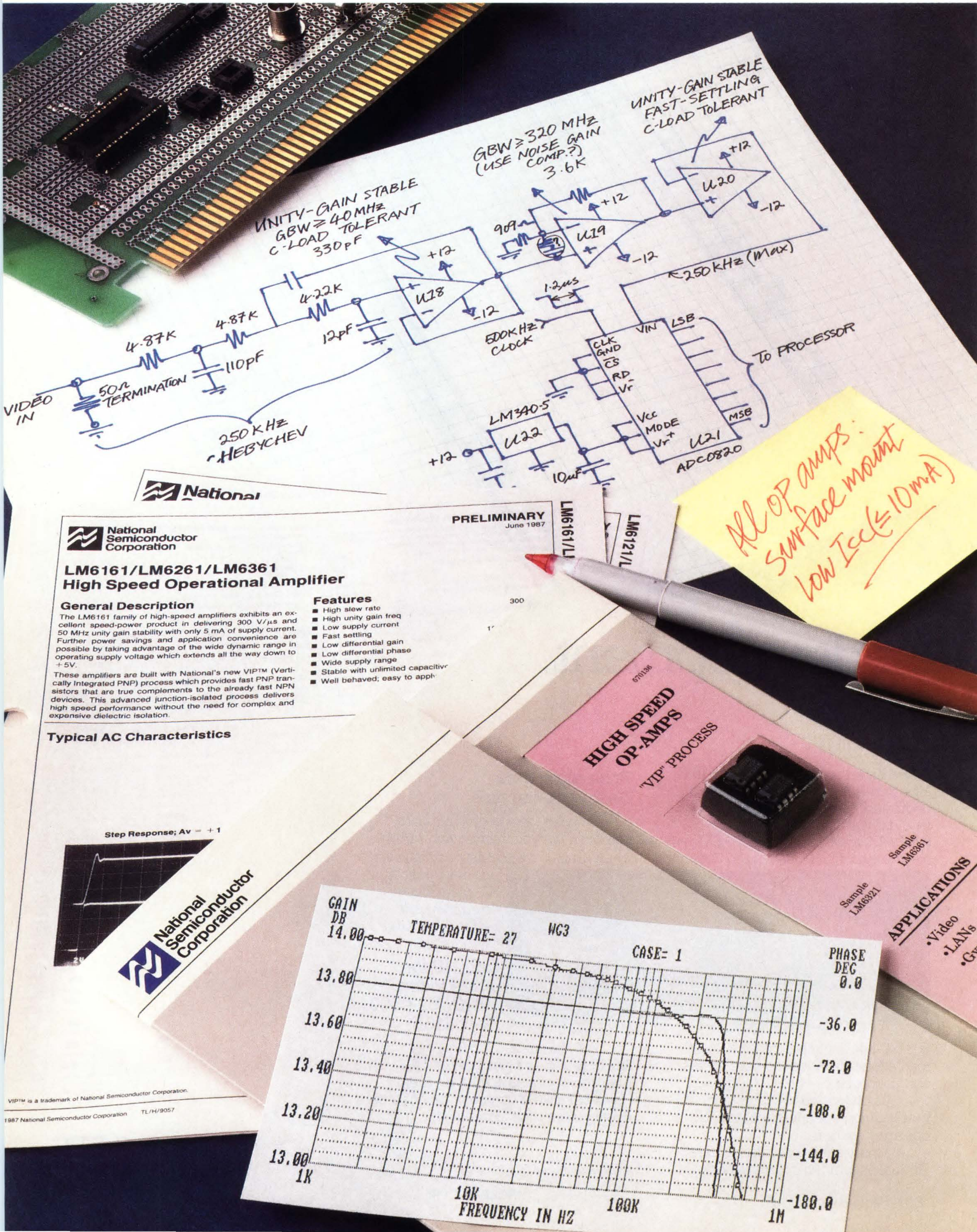

Everything you need to design-in high-speed op amps. For the price of a stamp.

OUR NEW VIP™ OP AMPS MAKE DESIGNING EASIER

Built with National's exclusive vertically integrated PNP (VIP) process, these new amplifiers couldn't be easier to design with — even for the novice.

You can use them to develop new designs never before practical. Or to enhance old designs for very little cost — in dollars, power, or real estate.

And we'll send you everything you need to get started — including a free sample. So you can see for yourself just how easy it is.

HIGHER SPEEDS, LESS POWER

These new op amps feature slew rates of 300 V/μs and gain-bandwidth products up to 750 MHz.

And they do so without complex, expensive, and power-hungry dielectric isolation techniques.

VIP op amps require no more power than traditional op amps. You can even use the same type of circuit-building techniques — with very little supply bypassing.

Because of their unique low power dissipation, you can easily fit them into predominantly digital systems without special analog power supplies.

Our exclusive VIP process and device layout give them excellent stability. They'll drive a 330 pF capacitive load — or any other size — with no oscillation.

The LM6361 is unity gain stable, the LM6364 stable for gains above 5, and the LM6365 for gains above 25. We also offer two VIP buffers.

LOWER COST

Not only are VIP op amps easier to design with than comparable devices but they cost less than a fourth as much. They are not made with expensive processes. Nor are they packaged in expensive packages.

Instead of TO-3s, they are packaged in ordinary 8-pin mini-DIP or surface-mount packaging.

They're ideal for video output stages, data communication systems, graphics systems, local area networks, and sample-and-hold circuits.

MORE CHOICES

In addition to VIP, National offers no less than four other major op amp processes — bipolar, BI-FET,® CMOS, and hybrid. And each category contains many variations and subprocesses, so that you can choose the optimum building blocks for your application.

SEND FOR YOUR FREE SAMPLE KIT TODAY

All you have to do to get your free VIP sample kit is to return the coupon below. Or — if you don't have the price of a stamp — simply give us a call, toll-free, at (800) 252-4488, ext. 732.

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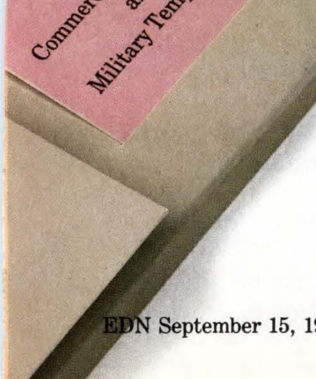

Please send me my free VIP sample kit with comprehensive data.

Name ________ Title ________
Company ________ Phone ________
Address ________
City ________ State ________ Zip ________

ADTL03 FK12000 EDN

EDN091588

Mail to National Semiconductor Corporation, Inquiry Processing Center, P.O. Box 6458, Torrance, CA 90504-9953.

This chip enabled us to process signals of the past.

The Rosetta Stone, discovered in 1799, was the key to deciphering the hieroglyphics that had been incomprehensible for centuries.

Signal processing, when you come right down to it, is multiplication, addition, subtraction and storage. Doesn't sound very exciting.

But put together a set of building blocks that do those simple operations with almost unimaginable digital speed and precision. Then add A/D converters that bring in information from the world around you. Plus D/A converters that restore the digitally processed signals to a form your senses can understand.

And you've built a signal processing system that will enable you to do things that couldn't be done before, see things that couldn't be seen before and understand things that could never be understood before.

That's exciting. And we can help make it happen.

Complete systems solutions.

Our approach to signal processing is simple.

We've taken our unparalleled experience in data conversion and added to it a set of signal processing chips that perform operations that used to require entire circuit boards.

Here's a sample of what they can do for you:

ISP 9110 12-Bit Microprogram Sequencer: expanded 33 word stack, 50 ns minimum cycle time.

ISP 9119 FIFO RAM Controller: uses standard RAMs to build FIFOs up to 64K deep, 15 MHz operation.

ISP 9128 FIR Filter Controller: implements 16-bit filters to 128 Taps, 128 Tap sampling rate of 100kHz.

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ISP 9216 16x16 Multiplier: low-power, industry-standard compatible to AM29516 and MPY016.

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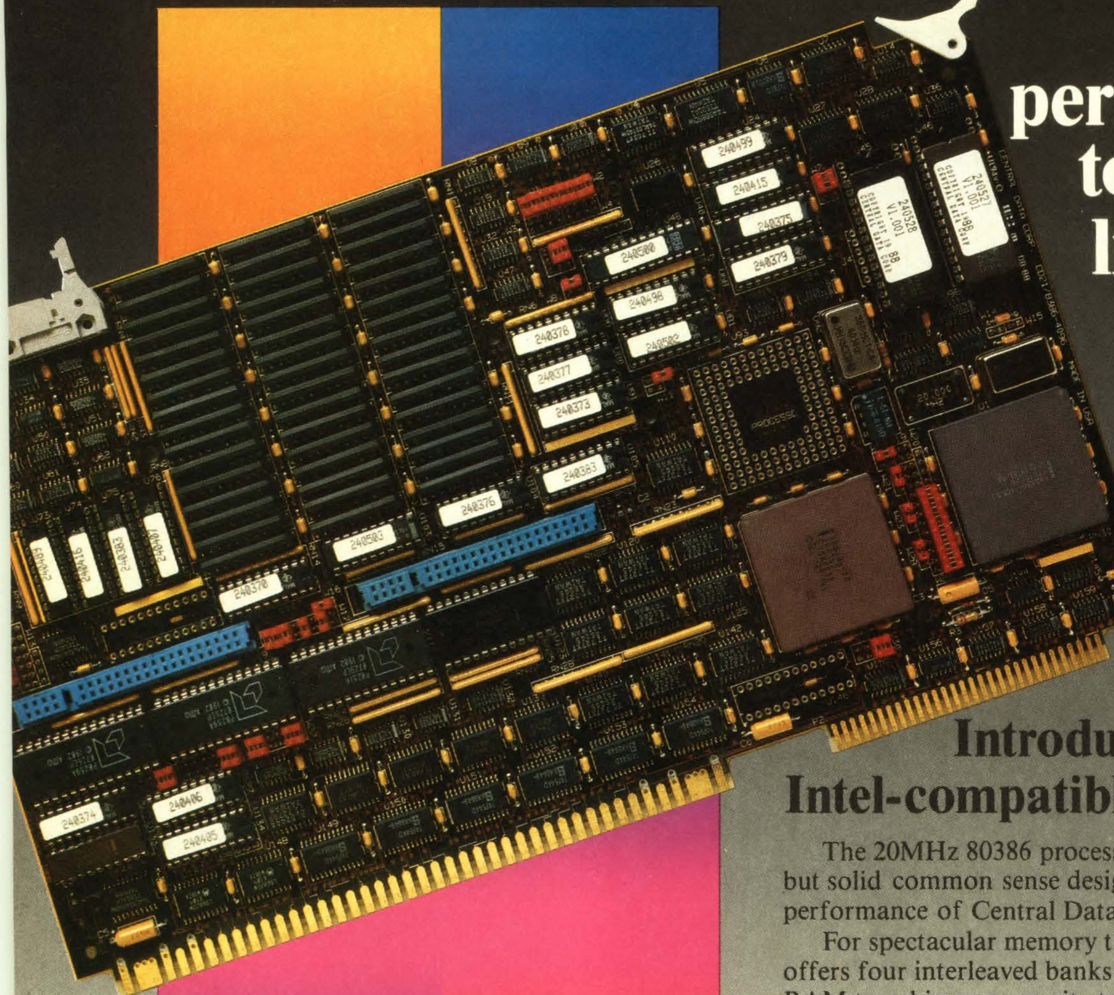

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CIRCLE NO 115

NEWS BREAKS

EDITED BY JOANNE CLAY

GATE-ARRAY MACROCELLS SUPPORT SERIAL-SCAN TEST TECHNIQUES

Macrocell libraries for a pair of CMOS gate arrays from Honeywell Inc's Solid State Electronics Div (Colorado Springs, CO, (719) 540-3539) allow you to build a variety of serial-scan test features into your ASIC design. Macrocells for the company's radiation-hardened, 15,000-gate HCT15000 support serial-scan test techniques and implement a bus controller for the VHSIC (very high-speed IC) Phase 2 serial T&M (test and measurement) bus. In addition to supporting serial-scan testing and the VHSIC T&M bus, the macrocell library for the company's 20,000-gate HC20000 also provides I/O boundary cells that support the JTAG (Joint Test Action Group) boundary-scan scheme.

The company developed both gate arrays for military and aerospace applications. Adders implemented with either product compute a 16-bit result in 7 nsec and a 32-bit result in 11 nsec. NRE charges for the HCT15000 and HC20000 range from $50,000 to $70,000 and $50,000 to $90,000, respectively. Parts cost $350 to $550 (1000) for HCT15000-based designs and $400 to $600 (1000) for HC20000-based designs, depending on the amount of ac testing needed and the required screening level.—Steven H Leibson

DIGITIZER RESOLVES 500-MHz, SINGLE-SHOT TRANSIENTS TO 11 BITS

LeCroy Corp (Chestnut Ridge, NY, (914) 425-2000) has announced a waveform digitizer that provides 11-bit resolution and a 500-MHz bandwidth when capturing single-shot transients. It samples at a maximum rate of 1.35G samples/sec, and, when digitizing repetitive signals, provides 14-bit resolution. LeCroy claims that the single-shot resolution exceeds by a factor of more than two the single-shot resolution of the best 1-GHz-sampling digitizer available until now. The 6880B digitizer and 6010 controller are modules that plug into several of the vendor's instrumentation mainframes. They make it simple to configure multichannel waveform-acquisition systems. The C2100, a single-channel system for benchtop use, includes PC-based oscilloscope-emulation software and sells for $20,450.—Dan Strassberg

MACINTOSH II ADD-IN CARD AND SOFTWARE PERFORM DSP

Spectral Innovations (Sunnyvale, CA, (408) 734-1314) has developed an add-in card and a set of software tools that convert the Macintosh II to an interactive DSP workstation. The MacDSP package includes a board based on the AT&T DSP32 μP and menu-driven DSP software that can perform FFTs, FIR and IIR filtering, spectral averaging, and many other signal-processing functions. You control the software package via the standard mouse-driven Macintosh user interface. You can apply the signal-processing capabilities to real-time incoming data, data stored in memory, or data stored on disk. To perform analysis of real incoming data, you must add a $486 data-acquisition card to the MacDSP. The 16-bit card operates at 125 kHz. Currently, the company offers the MacDSP in speed grades of 8M and 12.5M flops; the products cost $2249 and $2745, respectively. Around year's end you can expect a 25M-flops version.—Maury Wright

FLOPPY-DISK-CONTROLLER IC REPLACES A BOARD FULL OF CHIPS

The DP8473 floppy-disk-controller chip incorporates an analog data separator, write-precompensation and PLL circuitry, 40-mA disk-interface drivers, and 12-mA bus-interface buffers that allow the device to link as many as four floppy-disk drives to an IBM PC, PC/AT, or PS/2 bus with the addition of just an address decoder, a crystal, and a handful of passive components. The $16 (1000) IC from National Semiconductor Corp (Santa Clara, CA; contact Carl Ching at (408) 721-4960) accommodates disk-drive data rates of 250k to 1M bps and disk drives with as many as 4000 tracks/surface. The device retains software compatibility with the NEC µPD765A floppy-disk controller, which is generally incorporated in IBM-PC-compatible designs.—Steven H Leibson

COLOR-PALETTE CHIP ADDS CURSOR GENERATION AND INTEGER ZOOM

The Bt459 triple 8-bit RAMDAC from Brooktree Corp (San Diego, CA, (619) 452-7580) integrates additional features such as cursor generation, but maintains compatibility with the industry-standard Bt458 IC. The palette chip features 135-MHz pipelined operation. You can also specify the chip in 80- and 110-MHz speed ranges. A 2-plane dedicated palette allows the chip's integrated cursor facility to generate a 3-color cursor. The chip can perform a 1× to 16× integer zoom. In addition, the IC features on-chip diagnostics that include a checksum test to verify the operation of the color-palette RAM and the frame-buffer RAM, and on-chip comparators to test the DAC outputs. In 100-piece quantities, the chip costs $251 (135 MHz), $230 (110 MHz), and $200 (80 MHz).—Maury Wright

GRAPHICS PROCESSOR SHEDS COST, GAINS KERNEL AND C COMPILER

At the same time that it dropped the price of its DP8500 raster graphics processor by 26% to $70 (10,000), National Semiconductor Corp (Santa Clara, CA; contact John Blair at (408) 721-4425) released a graphics software kernel and C compiler for the chip. In addition, the company chopped the prices of other devices in its 16-device, advanced-graphics chip set (AGCS)—it cut the price of the DP8511 BitBlt processing unit by 50% to $3.50 (80,000)—which dropped the price of AGCS silicon for an 8-plane color-graphics controller to $98 (10,000).

The kernel implements a real-time, multitasking interface and provides support for implementing high-level graphics standards such as the Graphical Kernel System (GKS) and the Computer Graphics Interface (CGI). The kernel functions include queue management for intertask communication, vector drawing, bit-mapped and stroked font generation, polygon fill, and CGI BitBlt. Source code for the kernel costs $8500. The C compiler accepts source programs written in either the ANSI-compatible or Kernighan & Ritchie dialects, and it emits assembler source code. To produce runnable code, therefore, you'll need the company's macroassembler, which is included in its $700 software-development kit. The C compiler costs $1000 for MS-DOS-based systems and $5000 for selected Unix environments.—Steven H Leibson

CORRELATOR CHIP OPERATES AT 50 MHz

You can search for a 64-bit pattern in a serial data stream as fast as 50 MHz by using the L10C23 correlator chip from Logic Devices (Sunnyvale, CA, (408) 720-8630). This device allows you to independently clock data, reference pattern, and mask registers, and it provides you with a 7-bit count of the matches. An on-chip comparator tells you when a match threshold is reached. You can cascade these devices to any word length you need. The chip uses 125 mW; the 50-MHz version costs $34.60 (1000).—Richard A Quinnell

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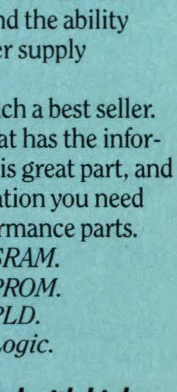

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CPU CARD ADDS LOW-COST I/O CHANNEL TO VME BUS SYSTEMS

By adding a daughter-board STE Bus interface to IO Inc's 68020-based V68/32 CPU card, Arcom Control Systems Ltd (Cambridge, UK, TLX 94016424) can provide you with an intelligent, low-cost I/O subsystem for VME Bus computers. In comparison with using VME Bus I/O cards, Arcom estimates, using the STE Bus as an I/O subsystem can cut I/O cost by as much as 50%. Alternatively, you can use the CPU and daughter-board combination (which Arcom sells as the VSC020 for £1380) to add 32-bit processing power to STE Bus systems. The CPU card's 68020 μP can access the 1M byte of STE Bus memory space, and 4k bytes of STE Bus I/O space, via the STE Bus interface on its P2 connector. An STE Bus arbiter on the daughter board lets you install additional bus masters on the STE Bus, and a 16k-byte dual-port window in the CPU card's onboard RAM allows mailbox-type communication between these STE Bus masters and the 68020 μP. The CPU card includes as much as 4M bytes of onboard RAM, two serial I/O channels, a 16-bit counter/timer, and a full 32-bit VME Bus interface. The board runs the OS-9/68k operating system, for which Arcom can provide software drivers for its range of STE Bus I/O cards.—Peter Harold

PORTABLE DIGITAL STORAGE OSCILLOSCOPE COSTS UNDER £1800

The Model 400 2-channel digital storage oscilloscope from Gould Electronics' Instrument Systems Div (Ilford, UK, TLX 263785) has a sample rate of 100M samples/sec for single-shot waveforms and uses random time sampling to achieve an equivalent sampling rate of 500M samples/sec for repetitive waveforms. The inputs are digitized to 8-bit resolution. Selling for £1795, the oscilloscope features pre- and posttrigger trace capture, trigger delays of as much as 5000 sec, on-screen trace-measurement cursors, nonvolatile storage for multiple traces, and an auto-set facility that you can use to select appropriate timebase and amplitude resolutions. The instrument weighs 5.5 kg and operates from 45- to 400-Hz ac line supplies or from a 12 to 30V dc supply. An RS-423 interface allows you to send trace information to a digital plotter or computer. For unattended operation, you can program the oscilloscope to send out only traces that are of significant interest. The Model 400 will be available in the US during the first quarter of 1989.—Peter Harold

16k × 4-BIT STATIC RAMS INCORPORATE ADDRESS AND DATA LATCHES

The TR9C1640 and TR9C1643 are 16k × 4-bit static RAMs from Triad Semiconductors (Eygelshoven, The Netherlands, (31) 45-467878; in the US: Colorado Springs, CO, (719) 528-8574) whose on-chip address and data latches permit you to implement a pipelined memory subsystem without additional circuitry. The address latches free up a system's address bus early in any transfer cycle, and the transparent data latches extend the data-valid duration of a memory-read cycle. Thus, the RAMs can retrieve new data while a processor is still reading the data placed in the latches by the previous cycle. The chips differ only by the output-enable input on the 24-pin TR9C1643. The TR9C1640 comes in a 22-pin DIP. The company offers both RAMs in 25-, 35-, and 45-nsec versions for $9.75, $12.75, and $15.75 (1000), respectively.—Steven H Leibson

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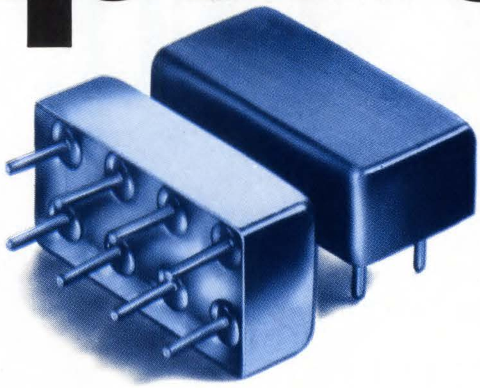

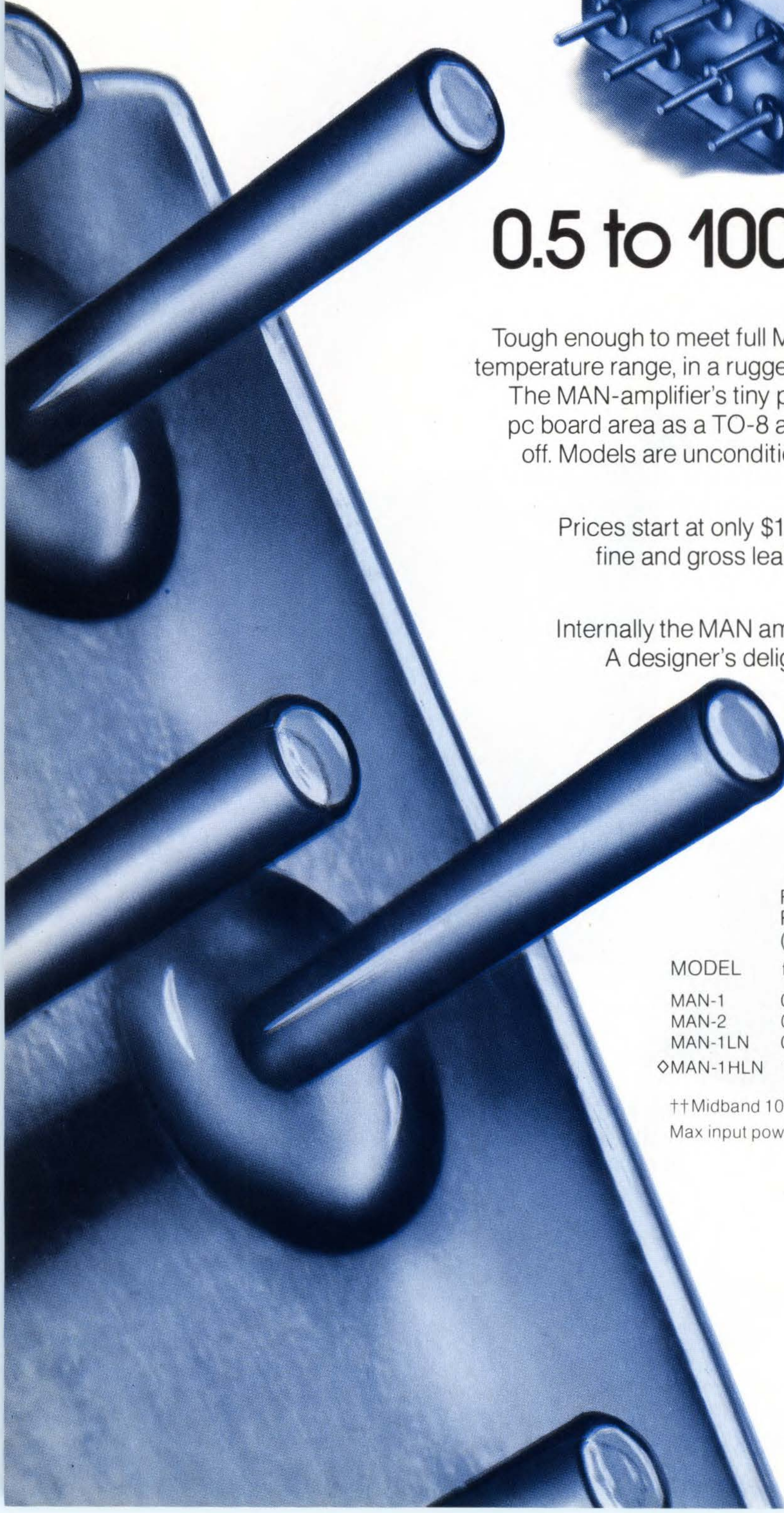

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CIRCLE NO 117

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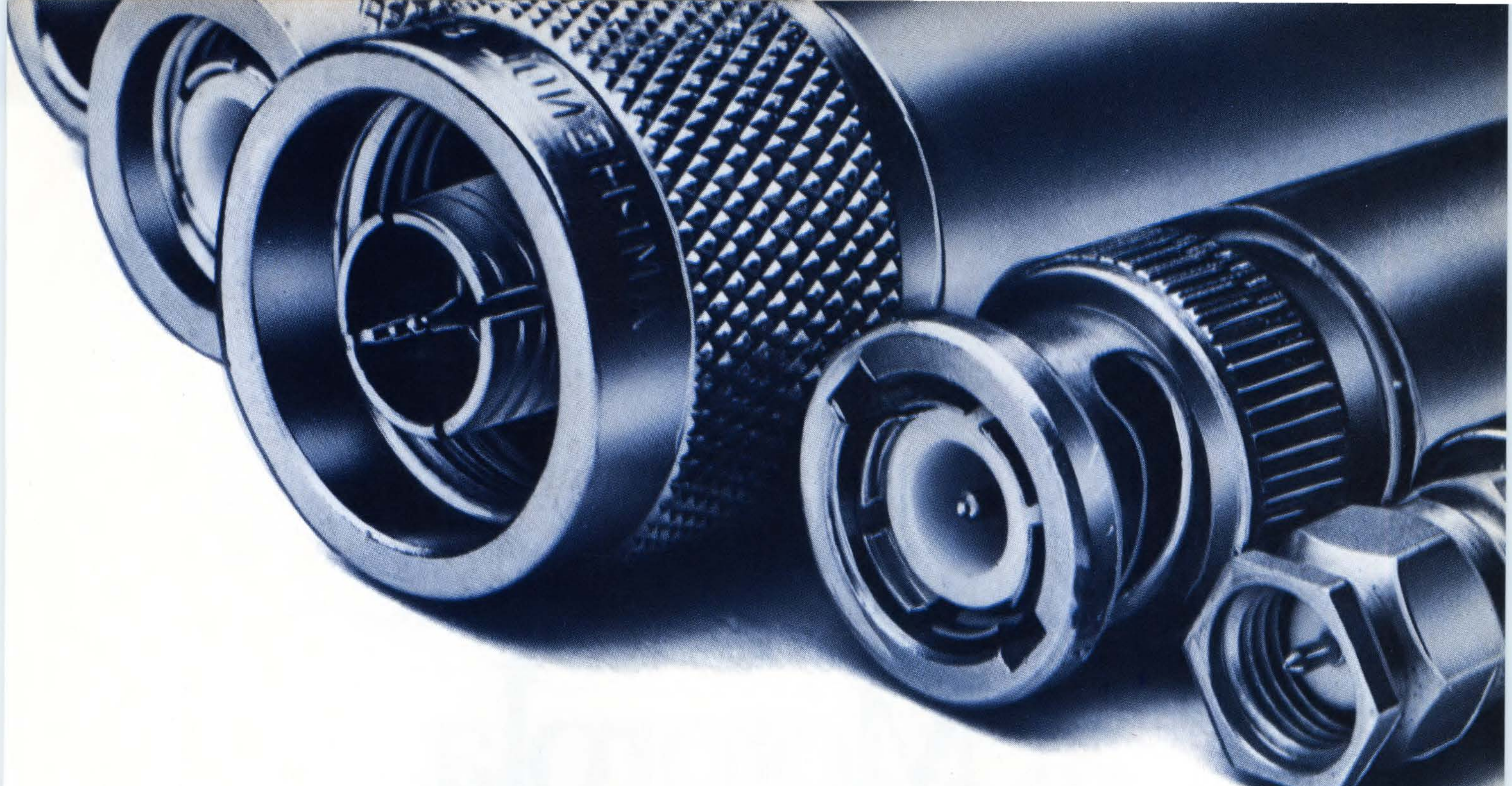

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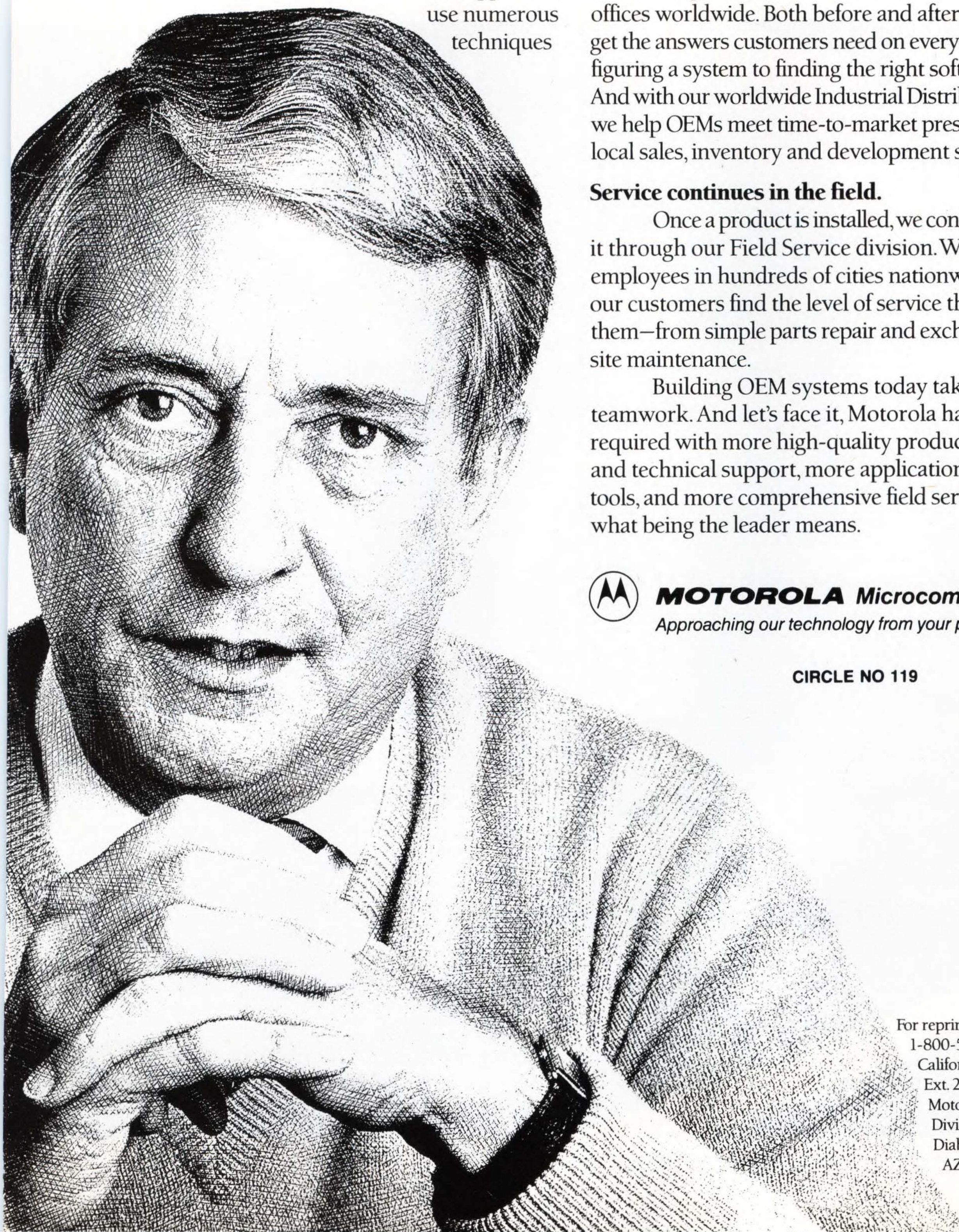

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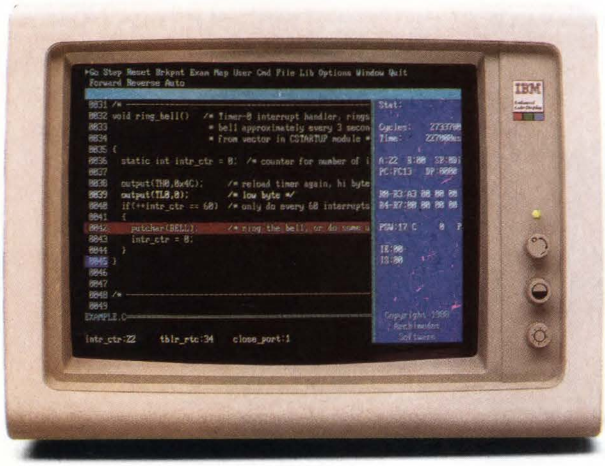

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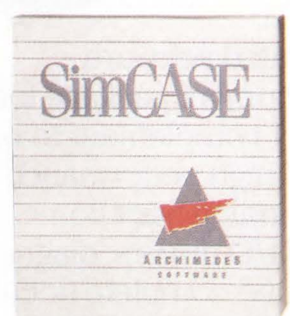

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CIRCLE NO 122

Designers shouldn't ignore *any* device parameters

I am in perfect agreement with Robert Pease's response (Signals & Noise, EDN, May 26, 1988, pg 36) to Keats Pullen's comments on lost technology (Signals & Noise, EDN, March 17, 1988, pg 34). Specifically, any attempt to categorize all types of devices (tubes, FETs, and bipolar transistors) as having transconductance gains (g_m) that are direct functions of qI/kT is misleading. As far as I know, only bipolar devices fulfill the relationship, and they do so over many decades of operating emitter current.

IC designs using bipolar transistors need to take into account several low-frequency parameters, such as current gain, output impedance (controlled by the Early effect), operating currents, and intrinsic bulk impedances in base, emitter, and collector regions. G_m is one parameter that is *not* usually specified because it's generally so close to theoretical ($g_m = qI_e/kT$) that it can be taken for granted. Only at very low or very high currents does g_m deviate significantly from this ideal value.

You can design low-distortion bipolar amplifiers either by employing large amounts of feedback or by using g_m linearization techniques with less overall feedback. The inherent exponential current/voltage characteristics of bipolar devices have in fact also been used to advantage in linearized current amplifiers, AGC circuits, logamps, and various multipliers, mixers, etc. The accuracy and inherent functionality of these types of circuits rely on the fact that the bipolar-transistor g_m is nearly ideally proportional to I_e (that is, it's nonlinear). When you analyze the transconductance gain of an ideal bipolar differential amplifier, you can easily see that the g_m falls to approximately one half its peak value when driven with a differential signal of $\pm 2kT/q$ ($\sim \pm 52$ mV). An ideal linear amplifier could be categorized as one in which the transconductance gain is constant over as wide a signal range as possible (say, several volts). One such method has been devised as a result of extensive simulation verification with the Analog Workbench simulation tool. It takes the form of a complementary quad configuration that can be implemented with any complementary process (the patent is pending).

In sum, let linear designers unite in their determination to use *all* relevant device parameters in finding better ways to design linear circuits. Ignoring any parameter, be it beta or g_m, is like putting one's head in the sand and hoping the problem will go away.

Derek Bray
Director of Design Services
Analog Design Tools Inc
Sunnyvale, CA

Treat design parameters in order of importance

I was pleased to find Bob Pease's letter in response to my letter in EDN's March 17 issue, and I must comment on some of his statements. It appears he does not fully understand what the situation really is for the engineer attempting to design with discrete devices. I first had to solve that problem with tubes, and then with various kinds of relatively linear active devices.

The issue boils down to these facts:

- Phase stability requires controlled voltage gain.
- Voltage gain depends on g_m, not beta.
- The value of g_m is a function of output current with all of our currently available active devices, but can require adjustment for transconduc-

Text continued on pg 47

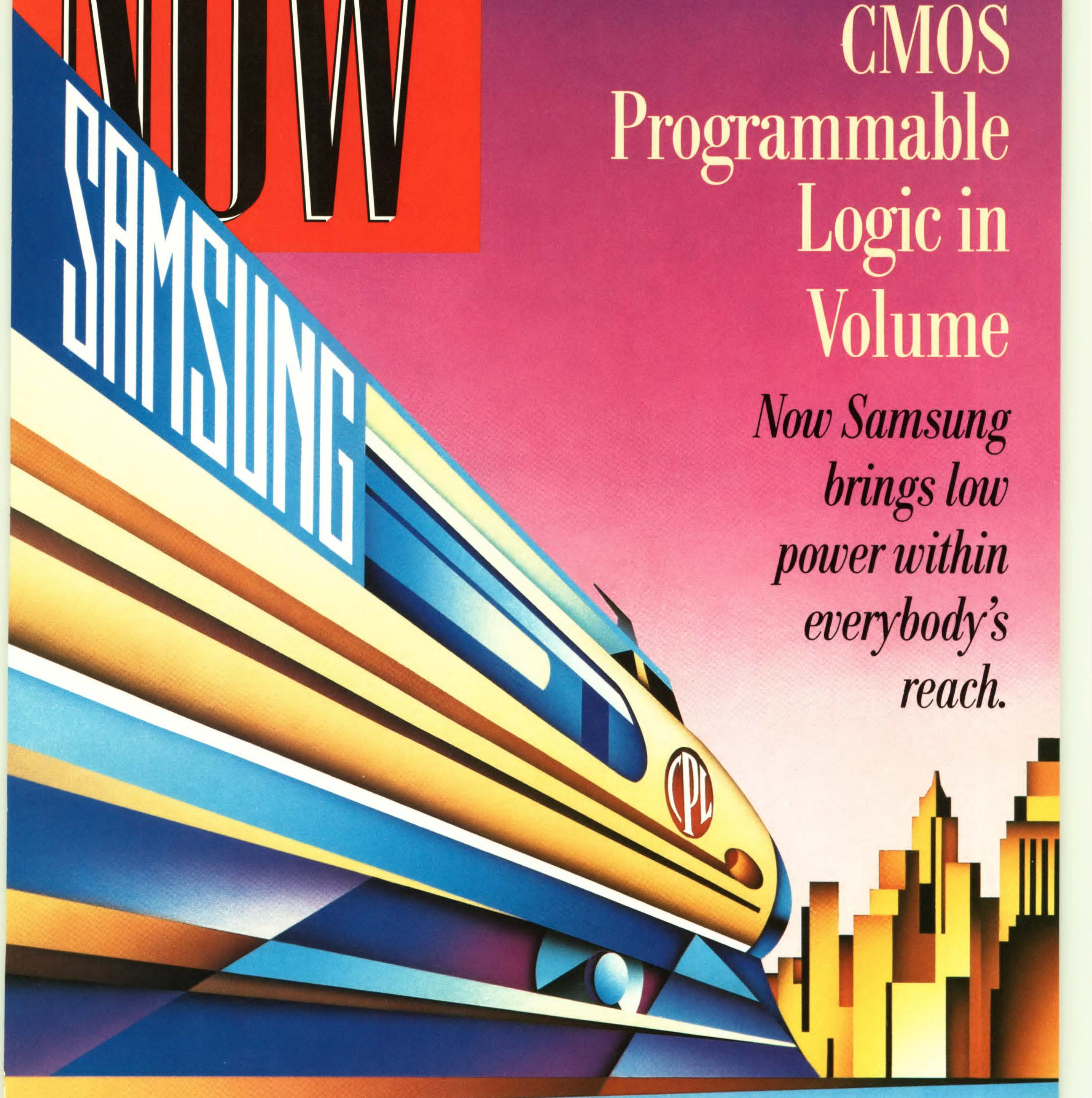
SAMSUNG

NOW

Number I

CMOS Programmable Logic in Volume

Now Samsung brings low power within everybody's reach.



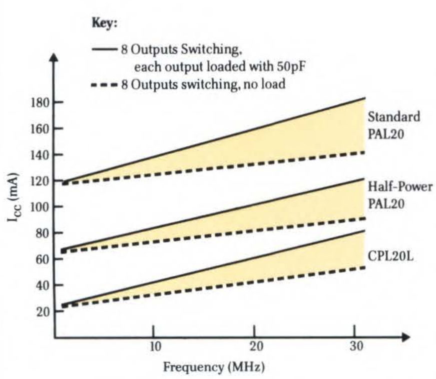
We Introduce an Exceptionally Reliable New EEPROM in CMOS
Blazing Speed from a DRAM Controller □ 400 MOSFETs Superb in Ruggedness.

CMOS PROGRAMMABLE LOGIC

INTRODUCING CPL™

Samsung Moves

Harnessing our manufacturing strength, we become the first to produce this demanding technology in volume.



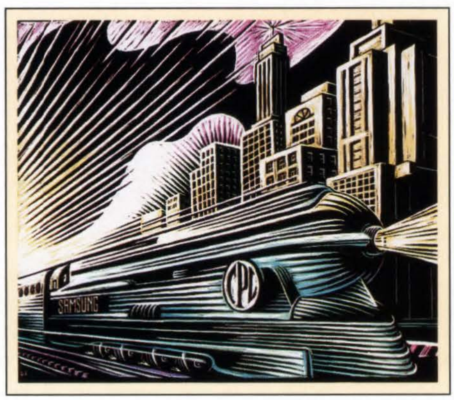
CPL reduces power dissipation up to 70% compared to bipolar PALs.

Since the beginning, Samsung Semiconductor has been known for its manufacturing expertise.

Samsung's commitment to CMOS technology is also long-standing.

Today, our new CPL (CMOS Programmable Logic) product line draws on both of those strengths.

It is a product line at the cutting edge of technology, and we are uniquely positioned to manufacture it–and manufacture it in volume.



What the introduction of CPL means is that, for the first time, there is a viable low-power alternative to bipolar PALs.®

It's viable both because we are offering CPL in volume. And because we're making it affordable–comparable in cost to bipolar parts.

In short, we're taking CMOS Programmable Logic, once and for all, out of its high-priced niche. To make low power a reality. And make compact systems more feasible than ever.

What will CPL do for you as a designer?

It will let you cut your power consumption 70% by directly replacing the bipolar PALs in your existing design. With no new development tools. And with no redesign.

In new designs, you'll have a head start on reducing power consumption.

And there's another critical advantage. Unlike bipolar PALs, Samsung's UV-erasable CPL devices are reprogrammable. Which means that we're in a position to ship 100% tested parts. We subject every CPL device, in fact, to programming, AC, and functional testing.

CPL–low in power, 100% tested, and produced in volume by a manufacturing giant–is here to stay. Request a databook and samples today, and get started with this winning technology now. NOW

Samsung: A leader in CMOS

Samsung Semiconductor is among the world's leaders in manufacturing products that use leading-edge CMOS processes. Our 6-inch wafer-fabrication lines are some of the most advanced in existence. Our technology has evolved from 2.5 micron to 0.8 micron in just four years. And we have invested more than $600 million in new-product development. Throughout our growth, we have continued to manufacture products that meet the very highest quality standards.

The CPL Parts

CPL 20	CPL 24
CPL16L8	CPL20L10
CPL16R4	CPL20L8
CPL16R6	CPL20R4
CPL16R8	CPL20R6
	CPL20R8

Speed options: 25 nsecs, 35 nsecs.
Power options (Icc max.) 45 mA, 70 mA

TURN *to coupon on back page to request free CPL samples and data book.*

To The Forefront.

You can develop a CPL design with existing tools. Or you can use our Starter Kit and start prototyping immediately.

Developing new, low-power designs with Samsung CPL is easy. And to make it that much easier, we're offering a low-priced CPL Starter Kit.

The Starter Kit includes a software package developed by Personal CAD Systems and based on CUPL,™ the most powerful high-level language for designing programmable logic. And it also includes samples of Samsung CPL20 and CPL24 devices, which are supported by the Starter Kit.

Since CPL devices are reprogrammable, this means the Starter Kit includes everything you'll need to prototype and debug your design.

And you'll be doing that in short order. The CUPL software runs on any IBM PC/XT/AT or compatible system, and it lets you choose from a variety of options for entering your design–including truth tables; state diagrams and ASM flow charts (for describing sequential designs); and high-level equations.

CUPL power tools provide logic minimization, available in three algorithms for improved optimization; DeMorganization (helpful when negating complex expressions); and simulation, to help you verify your design.

Comprehensive documentation includes a logic "template" file for design ease; a fuse map and expanded product-term information; a chip diagram illustrating pin assignments; and a symbol table of all variables. In addition to the CUPL software, Samsung's CPL Starter Kit includes:

- CPL20 and CPL24 samples.
- A CPL data book.
- A manual for the CUPL software.
- A Programmable Logic User Guide (PLUG) diskette, which lets you browse interactively through the workings of programmable logic.
- "My First PAL Design," a booklet that leads you step by step through programmable logic design.

At just $220, Samsung's CPL Starter Kit is a bargain. Request ordering information today and get started designing–in low power. NOW

TURN
to coupon on back page to request information on the CPL Starter Kit.

KS74AHCT Parts

Gates and Inverters

00	08	20	51
01	09	21	58
02	10	22	86
03	11	27	132
04	12	30	133
05	14	32	266

Buffers and Line Drivers

125	241	367	467
126	244	368	468*
210	365	465*	540
240	366	466	541

Flip-Flops

73	173	534	823
74	174	564	824*
76	175	574	825*
78	273	670	826*
107	374	794	
109	377	821*	
112	399	822*	

Latches

75*	533	841*	845
77*	563	842*	846
259	573	843*	
373	793	844*	

Transceivers/ Registered Transceivers

242*	643	651	664
243*	645	652	665*
245	646	658*	
640	648	659*	

Counters

160	168	192	590*
161	169	193	591*
162	190	390*	592
163	191	393	593*

Decoders/Encoders

42	139	154	238
138	148	155	239

Multivibrators

121* 123* 423*

Logic Level Converters

4049 4050*

Multiplexers

151	158	257	353
153	251	258	
157	253	352	

Shift Registers

164	194	299	596*
165	195	595	597
166			

Arithmetic Circuits

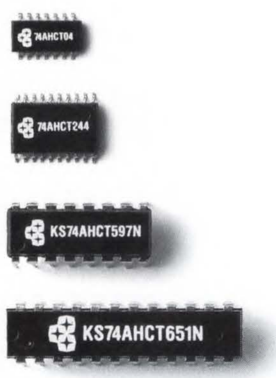
181	518	522	684*
182*	519	679	686*
183	520*	680	688
280	521	682	689*

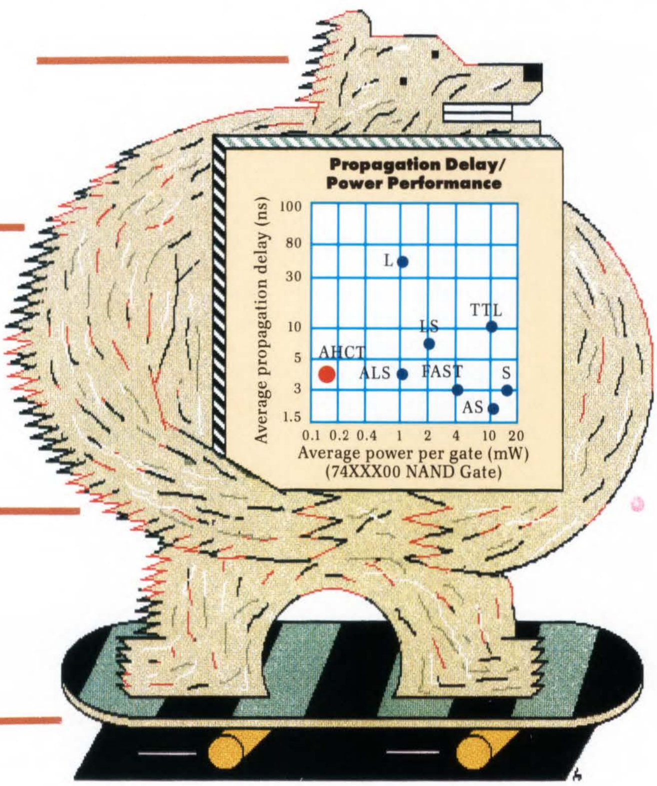
All parts are available in plastic DIP. For SOIC availability, contact the factory.
**Available by end of 1988.*

ADVANCED CMOS LOGIC FAMILY

125 Parts *that are* Exceptionally Fast *and* Very Available.

The entire Samsung AHCT CMOS advanced logic family is in stock, available, ready, and waiting to be shipped—right now. All fast, all very very cool.





When you look at both speed and power, you see that Samsung's AHCT family is, simply, unsurpassed.

And unlike other advanced logic families, these are parts that are available today, from stock.

All 157* of the AHCT CMOS logic family parts are direct plug-in replacements for ALS and FAST™–parts that provide the most comprehensive selection of standard logic functions available. Which means that no matter which ALS or FAST part you're using, you can replace it with an AHCT CMOS part–and cut your power–right away.

The entire family has a successful three-year production history behind it. And the parts are competitively priced –in fact you'll pay no more than you would for ALS.

We have free samples available for you today. Or, as an additional way to learn just how good these parts are, use the coupon at the back of this insert to request information on our AHCT tool box. It keeps 100 of the most popular advanced CMOS logic device types at your fingertips, whenever you need them. NOW

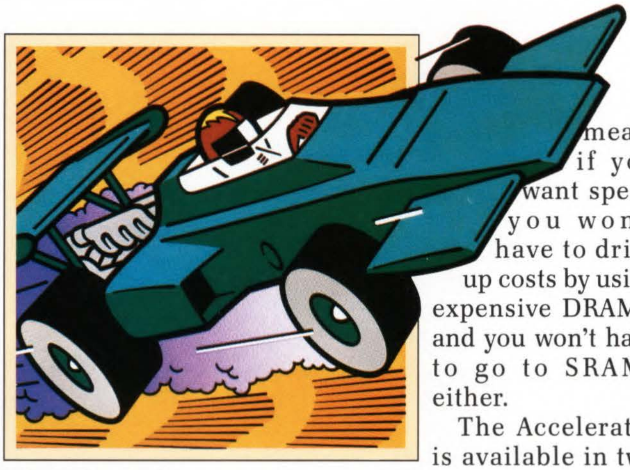
TURN
to coupon on back page to request free AHCT family samples, data book, and toolbox information.

**Of the 157 parts in the family, 125 are available from stock today; the remaining 32 will be available by the end of 1988.*

DRAM CONTROLLER

Our new 1- and 4-meg DRAM Controller is also a system accelerator. It can give you

80ns *Performance* *from* 120ns *DRAMs.*



Our new 1- and 4-meg DRAM Controller does so much for system speed that we've named it *The Accelerator.*

If you're a designer attracted to speed, you're going to want to design it in.

The KS84C21/22 DRAM Controller supports interleaving, and it supports the fastest access modes of the newest DRAMs.

It radically reduces parts count and engineering effort compared to PAL-based designs and interfaces to all major microprocessors.

But above all, it effectively increases the speed of your memory array–giving you performance exceeding 80ns from 120ns DRAMs.* Which means if you want speed, you won't have to drive up costs by using expensive DRAMs, and you won't have to go to SRAMs either.

The Accelerator is available in two versions. One has an externally programmable register, for prototyping and moderate-volume applications. The other version is the first and only mask-programmed DRAM controller ever developed anywhere, and it eliminates still more logic parts.

To make it easier to get started with The Accelerator, we've made up a sample kit.

Request yours today and start designing-in speed! NOW

Samsung's DRAM Controller.

Part	RAMs Supported	Package
KS84C21-25CL	256K, 1 MB	68-pin PLCC
KS84C22-25CL	256K, 1 MB, 4 MB	84-pin PLCC

*System dependent.

TURN
to coupon on back page to request free DRAM controller sample kit and specifications.

Samsung: Building on our leadership in DRAMs
As one of the world's leading producers of DRAMs, Samsung Semiconductor has been able to compete in one of the most demanding technologies of all. And we will continue to do so as our 4- and even 16-megabit products emerge. We're making additional use of this manufacturing know-how to deliver an extremely broad range of semiconductor products that are remarkable for their high performance, their cost-effectiveness, and their reliability.

EEPROMS

Our CMOS 64K EEPROM Is an Entirely New Breed.

Feature by feature it's as good or better. But besides using less power, it also consumes less money.

When you stack it up against the leading competitors, our new CMOS 64K EEPROM is, in a word, better.

It uses less power (100 μA vs. 150 μA standby current, 30 mA vs. 50 mA active current). It's exceptionally fast.

And it's available at much lower cost.

The part is available in volume right now.

In reliability, it's superb–far more reliable than requirements call for. In 1000 hours of testing in the key areas of endurance, WHTS, HOPL, and WHOPL–with industry-standard testing procedures–there were *zero* failures experienced.

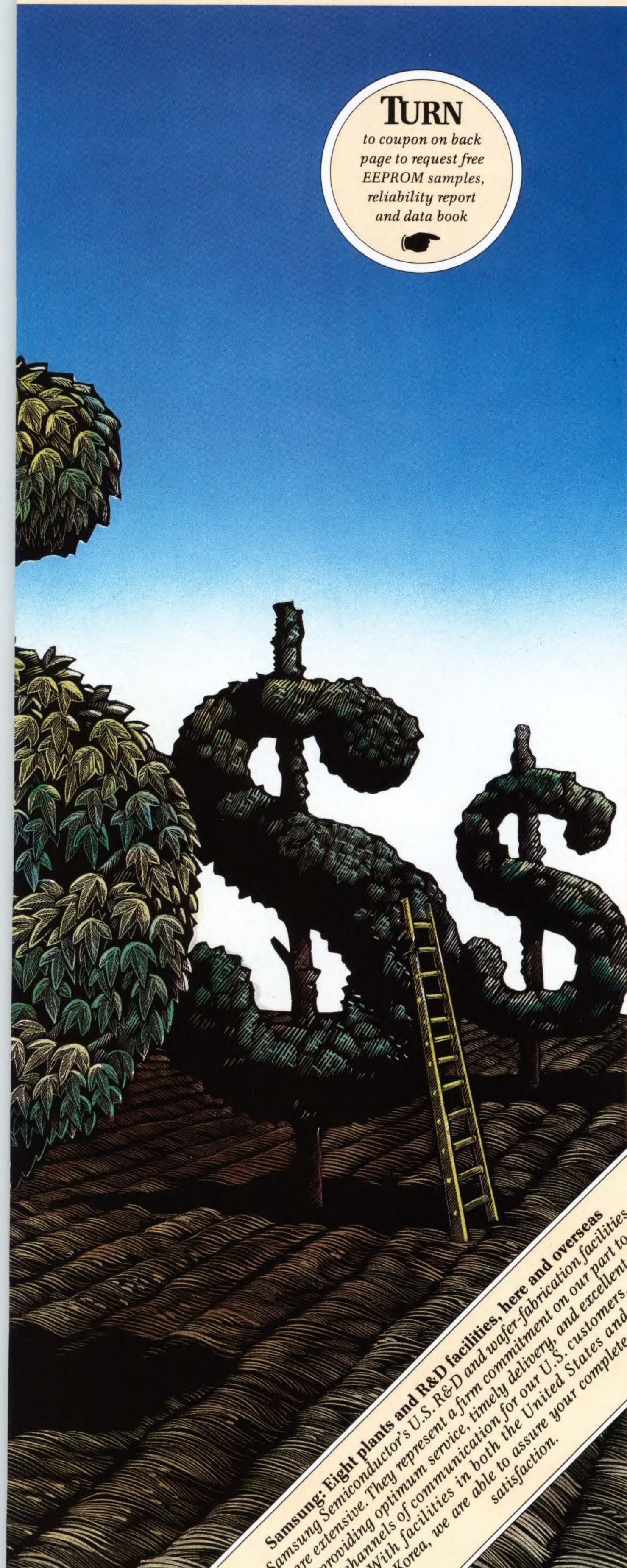
We think what all this means is that our new CMOS 64K EEPROM is simply the most sensible choice on the market.

But don't take our word for it. Request our reliability report, data sheet, and samples today. Then compare it for yourself. NOW

Product Specification	Samsung 28C64 8K x 8 CMOS EEPROM	Leading Competitor's 64K CMOS EEPROM
ISB (standby current)	100 μA	150 μA
ICC (active current)	30 mA	50 mA
TAA (address access time)	200 ns	200 ns
TRC (read cycle time)	200 ns	200 ns
TWC (write cycle time)	2-5 ms/byte	2-5 ms/byte
VCC	5V ± 10%	5V ± 10%
Page mode	Yes	Yes
Endurance (write cycle)	10,000	10,000
Data retention	10 years	10 years
Packaging	DIP, PLCC	DIP, PLCC

The KM28C64/65 at a glance.

8K x 8 CMOS EEPROM ■ 28-pin JEDEC byte-wide memory pinout (DIP, PLCC) ■ Single 5V ± 10% Vcc supply ■ Performance: 200/250ns ■ Current: standby (max) 100μA; active (max) 30mA ■ 32 byte page write: 5ms ■ 4-cell bridge for enhanced reliability ■ Write completion indicator: Data polling, Rdy/busy (for KM28C65) ■ Endurance 10,000 cycles ■ Data retention 10 years



TURN
to coupon on back page to request free EEPROM samples, reliability report and data book

Samsung: Eight plants and R&D facilities, here and overseas
Samsung Semiconductor's U.S. R&D and wafer-fabrication facilities are extensive. They represent a firm commitment on our part to providing optimum service, timely delivery, and excellent channels of communication for our U.S. customers. With facilities in both the United States and Korea, we are able to assure your complete satisfaction.

The Most Reliable Battery-Backed SRAMs Aren't SRAMs at All.

They're EEPROMs from Samsung.

Since EEPROMs don't require batteries to retain data during power loss, they are, of course, inherently more reliable than devices that do–such as SRAMs.

Because of the relative costs, however, it wouldn't occur to most designers to use an EEPROM where conventional thinking calls for an SRAM–even *with* the improvement in reliability that there'd be.

But those relative costs are changing.

Today, SRAMs cost more than they once did. And Samsung's EEPROMs, in fact, now compare favorably in price.

Which means that if you want reliability, there's every reason to start using these EEPROMs–and making your next battery-backed SRAMs, Samsung EEPROMs.

There are, of course, additional applications at which we excel. Our entire EEPROM family–including our new 64K CMOS part–is also superbly suited to rugged applications such as communications, instrumentation, robotics, and industrial control.

All Samsung EEPROMs are guaranteed to provide endurance in excess of 10,000 write cycles and data retention of 10 years. And they meet or surpass all other industry standards for performance, reliability, and quality.

Most important of all, our EEPROMs are available in large quantities *from stock*–so you avoid escalating lead times as well as high prices.

EEPROM performance, reliability, and availability–all at low cost. To start taking advantage of them, request samples, a data sheet, and a reliability report today. NOW

Samsung CMOS and NMOS EEPROMs.

Part Type	Organization	Speed	Features	Technology	Pinout	Availability
KM28C64P	8K x 8	200,250	Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time	CMOS	28 pin	From Stock
KM28C65P	8K x 8	200,250	Data Polling, 32-byte Page Mode, Low Power, 5ms (max) write time	CMOS	28 pin	From Stock
KM2816AP	2K x 8	250,300,350	10ms (max) write time	NMOS	24 pin	From Stock
KM2817AP	2K x 8	250,300,350	Ready/Busy, 10ms (max) write time	NMOS	28 pin	From Stock

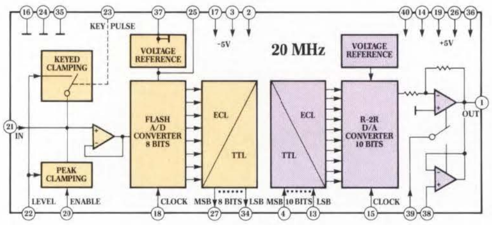
In linear, what Samsung gives you can be stated easily.

MORE.

A DATA CONVERTER THAT DOES MORE.

Samsung's new KSV3110 data converter is a technological feat that we're rather proud of.

On a single chip, it offers independent 8-bit flash A/D and 10-bit D/A functions. And with an operating range of DC to 20MHz, it's faster than any other part available that does both. Also unique, it gives you an auxiliary circuit, which can be used to do impedance matching within the chip.



What's good about having all this on one chip, of course, is that it saves you real estate and money–and also cuts power drain. And, at the same time, boosts system reliability.

In short, the KSV3110 doesn't just do more. It does *way* more.

TURN
to coupon on back page to request linear data books and specifications.

Samsung's 3110 Series Combination A/D-D/A Converters.

Part Type	Resolution		Linearity		Conversion Speed	Industry Part
	A/D	D/A	A/D	D/A		
KSV3110N-10	8 bits	10 bits	±1/2 LSB	±1/2 LSB	20 MSPS	
KSV3110N-9	8 bits	10 bits	±1/2 LSB	±1 LSB	20 MSPS	
KSV3110N-8	8 bits	10 bits	±1/2 LSB	±2 LSB	20 MSPS	
KSV3110N-7	8 bits	10 bits	±1/2 LSB	±4 LSB	20 MSPS	
KSV3100AN-8	8 bits	10 bits	±1/2 LSB	±2 LSB	20 MSPS	UVC3101
KSV3100AN-7	8 bits	10 bits	±1/2 LSB	±4 LSB	20 MSPS	UVC3101

VOLUME LEADERSHIP IN CONVENTIONAL A/D AND D/A...

As a company that does remarkable things in the manufacturing arena, Samsung is in a superb position to produce high-quality conventional data converters cost effectively and in volume.

And that's just what we do.

Which means that if you use data converters in large quantities, you simply won't find anyone it makes better sense to do business with.

Samsung: Some of the world's most advanced fabrication lines
Among our fabrication lines, a particular showpiece is our new Class 1 6" wafer facility in Kiheung, Korea, dedicated to DRAM technology and set to open in October of this year. It utilizes advanced stepper technology and is among the largest in the world.

The Samsung A/D and D/A Lines.

Part Type	Resolution A/D	Resolution D/A	Linearity A/D	Linearity D/A	Conversion Speed	Industry Part
KSV3208N	8 bits		±1/2 LSB		20 MSPS	
KAD0820ACN	8 bits		±1/2 LSB		1.5 μsec	ADC0820BCN
KAD0820AIN	8 bits		±1/2 LSB		1.5 μsec	ADC0820BCJ
KAD0820BCN	8 bits		±1 LSB		1.5 μsec	ADC0820CCN
KAD0820BIN	8 bits		±1 LSB		1.5 μsec	ADC0820CCJ
KAD0808IN	8 bits		±1/2 LSB		100 μsec	ADC0808CCN
KAD0809IN	8 bits		±1 LSB		100 μsec	ADC0809CCN
KDA0800CN		8 bits		±1/2 LSB	*100 nsec	DAC0800LCN
KDA0801CN		8 bits		±1 LSB	*100 nsec	DAC0801LCN
KDA0802CN		8 bits		±1/4 LSB	*100 nsec	DAC0802LCN
KDA0806CN		8 bits		±2 LSB	*150 nsec	DAC0806LCN
KDA0807CN		8 bits		±1 LSB	*150 nsec	DAC0807LCN
KDA0808CN		8 bits		±1/2 LSB	*150 nsec	DAC0808LCN
KS7126CN	3-1/2 digit		±1/2 LSB		333 msec	TSC7126
KS25C02	CMOS 8-bit successive approx. register					DM2502
KS25C03	CMOS 8-bit successive approx. register					DM2503
KS25C04	CMOS 12-bit successive approx. register					DM2504

**Settling Time*

And In Op Amps, Regulators, Comparators, Timers, And More.

Across the entire spectrum of high-volume linear devices, in fact, Samsung–being a manufacturing leader–offers a combination of reliability and competitiveness in price that has given these devices tremendous acceptance in the marketplace.

It's a market we're strongly committed to, and we have more than 250 industry-standard ICs available for immediate delivery now.

If by chance you *aren't* buying linear devices from Samsung, it will make sense for you to look into us.

Solutions Tailored To Specific High-Volume Needs. For Those Who Simply Need More.

A particular specialty that Samsung offers in linear is in the area of specific, rather simple solutions tailored to certain very high-volume applications.

We have developed devices for use in such high-volume areas as telephones, car stereo, and household appliances–among many others.

If you have a need for a high-volume, tailored linear device on this order, we may have the device you need–and if we don't, we'd like to talk about making it for you.

Our line of simple speech synthesis chips–designed for use primarily in electronic toys and answering machines–is one particular example of the kind of low-cost solution we can offer.

To learn about others, please contact us.

Our Speech Synthesizers.

Part	Function	Application
KS5901A	Voice synthesizer (external ROM)	Sound information answering machines
KS5902XX	Voice synthesizer (internal ROM)	Toys; simple sound generation
KS5911	Voice recording and reproducing (talking back type)	Talk-back answering machines
KS5912XX	Natural sound generation	Toys; natural sound effect

Major Linear ICs

Regulators

3T Positive

KA78TXXCF	3 Amp
KA78TXXCT	3 Amp
LM317T	1.5 Amp
MC78XXCT	1 Amp
MC78MXXCT	0.5 Amp
MC78LXXACZ	0.1 Amp
LM723CN	0.1 Amp

3T Negative

KA337T	1.5 Amp
MC79XXCT	1 Amp
MC79MXXCT	0.5 Amp
MC79LXXACZ	0.1 Amp

Switching

KA78S40CN KA3524N

REF Voltage

KA431CZ (TL431CLP) KA336Z-2.5,5
KA431N (TL431CP) KA385Z-1.2

Comparators

KA319N (LM319N) LM2903N
KA361N (LM361N) LM311N*
KA710CN (LM710N) LM3302N
KS374N (TLC374N) LM339N/AN*
LM2901N LM393N/AN*

Op Amplifiers

KA301N/AN (LM301N)* LM348N*
KA733CN (LM733CN) LM358N/AN*
KA9256 (POWER AMP) LM741CN*
KF351N (LF351N) MC1458N*
LM2902N MC3303N
LM2904N MC3403N*
LM324N/AN* MC4558N*

Telecommunication ICs

KA2410N	Tone Ringer
KA2411N	Tone Ringer
KA2418N	Tone Ringer/bridge diode
KA2412FN	Speech Network
KA2413N	DTMF
KS5808N	DTMF (MK5089)
KS5805AN	Pulse (MK50992)
KS5805BN	Pulse (MK50993)
KS55820N	DTMF/Pulse
KT3040J	CODEC Filter
KT5116J	CODEC
LM567N*	Tone Decoder
LM567LN	Tone Decoder (Low Power)
KS5812N	Quad UART

Timers

KS555N (CMOS)* NE555CN*
KS555HN (CMOS)* NE556CN*
KS556N (CMOS)* NE558CN

RS-232 Interfaces

MC1488N* MC1489/AN*

Audio ICs

LM386N	0.5 Watt Power Amp
KA2201N	1.2 Watt Power Amp
KA2206	2.3 Watt Dual Power Amp
KA22062	4.6 Watt Dual Power Amp
KA2210	5.8 Watt Dual Power Amp
KA22101	23 Watt Power Amp
KA2243	AM/FM IF & DET
KA22441	FM IF & DET
KA22495	FM Front End
KA2263	FM MPX

45 other audio ICs available

Video ICs

KA2914A	Color TV VIF/SIF
KA2153	NTSC Chroma & Deflection
KA6101	Video R.G.B. Interface
KA6102	Video R.G.B. Interface

40 other video ICs available

Others

KA2580AN	(UDN2580AN)
KA2588AN	(UDN2588AN)
KA2651N	(UCN5815AN)
KA2615	LED/Lamp Driver
KA2616	LED/Lamp Driver
KA2284	5 Dot LED Meter Driver
KA2286	5 Dot LED Meter Driver
KA2288	7 Dot LED Meter Driver
KA2181	Infrared Amp
KA8301	Motor Driver IC
KS5803AN	Infrared Transmitter
MC3361N	FM IF Amp

**Also available in surface mount package (SOIC)*

TRANSISTORS

We Launch a New 1500 volt Power Transistor

With over 500 transistors, Samsung is among the world's largest producers. Our 1500-volt parts break ground even for us.

As a producer of transistors, Samsung sits squarely among the very largest in the world.

There is virtually no transistor need we can't fill–with a high-quality part, and at an advantageous price.

Our entire line of more than 500 transistors, in fact, is in full production and available from stock.

You can order anything from our list *now,* and get immediate delivery.

At present, we are introducing state-of-the-art, 1500-volt power transistors–transistors so difficult to produce that only one other company makes them.

We also provide 100 types of SOT-23s, ideal for both hybrid and surface-mount applications, plus TIP Series, MJE Series, and TO-92 transistors.

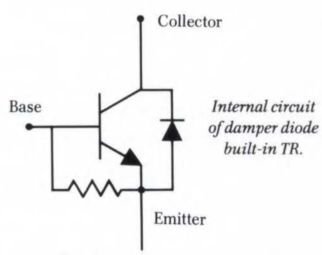
Many are listed here, but for a complete list of Samsung transistors, please turn to the back of this issue and request it.

NOW

Samsung: One of the world's largest corporations

As a unit of one of the world's largest corporations, Samsung Semiconductor is here to stay. Last year, the Samsung Group enjoyed revenues of $24 billion–which would put us in 15th place on the list of the Forbes 500. We have the resources to make things happen technologically, and we have the strength to be a partner in whom you may have absolute confidence.

The new 1500-volt transistors at a glance.



Designed for high-voltage switching systems and industrial motor controls, the eight new Samsung 1500-volt power transistors utilize the TO-3PF fully isolated plastic package.

TURN *to coupon on back page to request complete list of Samsung transistors and data book.*

Transistors From Samsung

1500-Volt Power TR

2.5 amps	5 amps	6 amps
KSD5010*	KSD5012*	KSD5013*
KSD5014	KSD5016	KSD5017

3.5 amps
KSD5011*
KSD5015

**Damper diode built-in transistor*

SOT-23

BCX70G	MMBT4403	MMBTA43
BCX71G	MMBT5087	MMBTA55
MMBR5179	MMBT5088	MMBTA56
MMBT2222A	MMBT5089	MMBTA63
MMBT2484	MMBT5401	MMBTA64
MMBT2907A	MMBT5550	MMBTA70
MMBT3904	MMBT6428	MMBTA92
MMBT3906	MMBTA05	MMBTA93
MMBT4123	MMBTA06	MMBTH10
MMBT4124	MMBTA13	MMBTH17
MMBT4125	MMBTA14	MMBTH24
MMBT4126	MMBTA20	
MMBT4401	MMBTA42	

66 other types also available.

TIP SERIES

TIP29 Family	TIP106	TIP140F
TIP30 Family	TIP107	TIP140T
TIP31 Family	TIP110	TIP141F
TIP32 Family	TIP111	TIP141T
TIP41 Family	TIP112	TIP142F
TIP42 Family	TIP115	TIP142T
TIP47	TIP116	TIP145F
TIP48	TIP117	TIP145T
TIP59	TIP120	TIP146F
TIP50	TIP121	TIP146T
TIP100	TIP122	TIP147F
TIP101	TIP125	TIP147T
TIP102	TIP126	
TIP105	TIP127	

MJE SERIES

MJE170	MJE210	MJE800
MJE171	MJE340	MJE801
MJE172	MJE350	MJE802
MJE180	MJE700	MJE803
MJE181	MJE701	MJE2955T
MJE182	MJE702	MJE3055T
MJE200	MJE703	

TO-92

2N3904	2N5210	MPSA42
2N3906	2N5400	MPSA43
2N4123	2N5401	MPSA55
2N4124	2N5550	MPSA56
2N4125	2N5551	MPSA70
2N4126	2N6427	MPSA92
2N4400	2N6428	MPSA93
2N4401	2N6515	MPSH10
2N4402	2N6517	MPSH17
2N4403	2N6520	MPSH20
2N5086	MPSA05	MPSH24
2N5087	MPSA06	PN2222A
2N5088	MPSA14	PN2907A
2N5089	MPSA20	

200 other types also available.

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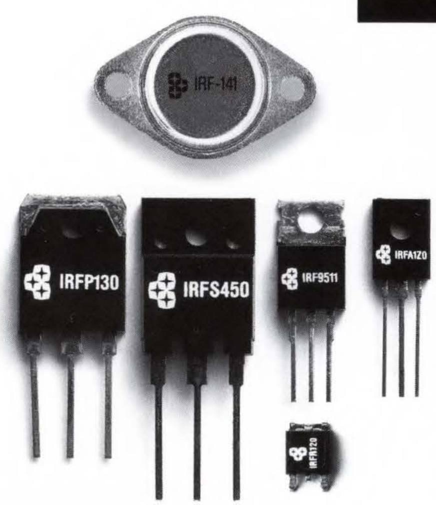

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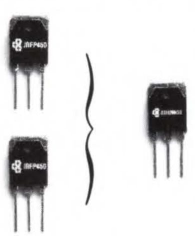

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IRFS130	IRFS450
IRFS140	SSS4N70
IRFS150	SSS6N70
IRFS230	SSS10N70
IRFS240	SSS4N60
IRFS250	SSS6N60
IRFS330	SSS8N60
IRFS340	SSS15N60
IRFS350	SSS20N50
IRFS430	SSS25N40
IRFS440	

TO-3P Package N-Channel Types

IRFP120	IRFP422
IRFP121	IRFP423
IRFP122	IRFP430
IRFP123	IRFP431
IRFP130	IRFP432
IRFP131	IRFP433
IRFP132	IRFP440
IRFP133	IRFP441
IRFP140	IRFP442
IRFP141	IRFP443
IRFP142	IRFP450
IRFP143	IRFP451
IRFP150	IRFP452
IRFP151	IRFP453
IRFP152	SSH3N70
IRFP153	SSH4N70
IRFP220	SSH6N70
IRFP221	SSH10N70
IRFP222	SSH4N60
IRFP223	SSH6N60
IRFP230	SSH8N60
IRFP231	SSH15N60
IRFP232	SSH4N55
IRFP233	SSH6N55
IRFP240	SSH8N55
IRFP241	SSH15N55
IRFP242	SSH4N50
IRFP243	SSH20N50
IRFP250	SSH4N45
IRFP251	SSH20N45
IRFP252	SSH5N40
IRFP253	SSH25N40
IRFP320	SSH5N35
IRFP321	SSH25N35
IRFP322	SSH7N20
IRFP323	SSH8N20
IRFP330	SSH7N18
IRFP331	SSH8N18
IRFP332	SSH7N15
IRFP333	SSH8N15
IRFP340	SSH7N12
IRFP341	SSH8N12
IRFP342	SSH12N10
IRFP343	SSH10N10
IRFP350	SSH12N08
IRFP351	SSH10N08
IRFP352	SSH12N06
IRFP353	SSH10N06
IRFP420	SSH12N05
IRFP421	SSH10N05

TO-3P Package P-Channel Types

IRFP9120	IRFP9220
IRFP9121	IRFP9221
IRFP9122	IRFP9222
IRFP9123	IRFP9223
IRFP9130	IRFP9230
IRFP9131	IRFP9231
IRFP9132	IRFP9232
IRFP9133	IRFP9233
IRFP9140	IRFP9240
IRFP9141	IRFP9241
IRFP9142	IRFP9242
IRFP9143	IRFP9243

TO-3 Package N-Channel Types

IRF120	IRF242
IRF121	IRF243
IRF122	IRF250
IRF123	IRF251
IRF130	IRF252
IRF131	IRF253
IRF132	IRF320
IRF133	IRF321
IRF140	IRF322
IRF141	IRF323
IRF142	IRF330
IRF143	IRF331
IRF150	IRF332
IRF151	IRF333
IRF152	IRF340
IRF153	IRF341
IRF220	IRF342
IRF221	IRF343
IRF222	IRF350
IRF223	IRF351
IRF230	IRF352
IRF231	IRF353
IRF232	IRF420
IRF233	IRF421
IRF240	IRF422
IRF241	IRF423
IRF430	SSM4N50
IRF431	SSM20N50
IRF432	SSM4N45
IRF433	SSM20N45
IRF440	SSM5N40
IRF441	SSM25N40
IRF442	SSM5N35
IRF443	SSM25N35
IRF450	SSM7N20
IRF451	SSM8N20
IRF452	SSM7N18
IRF453	SSM8N18
SSM3N70	SSM7N15
SSM4N70	SSM8N15
SSM6N70	SSM7N12
SSM10N70	SSM8N12
SSM4N60	SSM12N10
SSM6N60	SSM10N10
SSM8N60	SSM12N08
SSM15N60	SSM10N08
SSM4N55	SSM12N06
SSM6N55	SSM10N06
SSM8N55	SSM12N05
SSM15N55	SSM10N05

TO-3 Package P-Channel Types

IRF9120	IRF9220
IRF9121	IRF9221
IRF9122	IRF9222
IRF9123	IRF9223
IRF9130	IRF9230
IRF9131	IRF9231
IRF9132	IRF9232
IRF9133	IRF9233
IRF9140	IRF9240
IRF9141	IRF9241
IRF9142	IRF9242
IRF9143	IRF9243

TO-220 Package N-Channel Types

IRF510	IRF741
IRF511	IRF742
IRF512	IRF743
IRF513	IRF820
IRF520	IRF821
IRF521	IRF822
IRF522	IRF823
IRF523	IRF830
IRF530	IRF831
IRF531	IRF832
IRF532	IRF833
IRF533	IRF840
IRF540	IRF841
IRF541	IRF842
IRF542	IRF843
IRF543	SSP3N70
IRF610	SSP4N70
IRF611	SSP4N60
IRF612	SSP6N70
IRF613	SSP6N60
IRF620	SSP6N55
IRF621	SSP4N60
IRF622	SSP4N55
IRF623	SSP4N50
IRF630	SSP4N45
IRF631	SSP5N40
IRF632	SSP5N35
IRF633	SSP7N20
IRF640	SSP8N20
IRF641	SSP7N18
IRF642	SSP8N18
IRF643	SSP7N15
IRF710	SSP8N15
IRF711	SSP7N12
IRF712	SSP8N12
IRF713	SSP12N10
IRF720	SSP10N10
IRF721	SSP12N08
IRF722	SSP10N08
IRF723	SSP12N06
IRF730	SSP40N06
IRF731	SSP10N06
IRF732	SSP12N05
IRF733	SSP10N05
IRF740	

TO-220 Package P-Channel Types

IRF9510	IRF9610
IRF9511	IRF9611
IRF9512	IRF9612
IRF9513	IRF9613
IRF9520	IRF9620
IRF9521	IRF9621
IRF9522	IRF9622
IRF9523	IRF9623
IRF9530	IRF9630
IRF9531	IRF9631
IRF9532	IRF9632
IRF9533	IRF9633
IRF9540	IRF9640
IRF9541	IRF9641
IRF9542	IRF9642
IRF9543	IRF9643

TO-126 Package N-Channel Types

IRFA1Z0	IRFA1Z3

DRAMS

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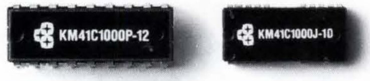

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KM41C1002	1M x 1	Static Column mode	100,120	DIP,ZIP,SOJ	3Q '88*
KM44C256	256K x 4	Fast Page mode	100,120	DIP,ZIP,SOJ	3Q '88
KM44C258	256K x 4	Static Column mode	100,120	DIP,ZIP,SOJ	3Q '89
KM41256	256K x 1	Page mode	120,150	DIP,ZIP,PLCC	Now
KM41257	256 x 1	Nibble mode	120,150	DIP,ZIP,PLCC	Now
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DRAM controller	☐ Sample kit	☐ Specifications	
64K CMOS EEPROM	☐ Samples	☐ Reliability report	________
EEPROMs	☐ Samples	☐ Data book	________
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Transistors	☐ Data book	☐ Complete list of Samsung transistors	
MOSFETs	☐ Samples	☐ Ruggedness application note	________
DRAMs	☐ Data sheets	☐ Reliability report	

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tance efficiency with FETs and tubes.

- The transconductance efficiency can be determined in terms of the input voltage change required to cause a 2:1 change in output current. The resulting kappa value is 0.018/dv, where dv is the change.
- The required supply voltage is just enough to lead to a device collector-to-emitter voltage of 1 to 2V at maximum device current. Any higher current can lead to excessive dissipation.

The critical design parameters need to be treated on the basis of their *order of importance* in control of circuit behavior. Voltage gain in conjunction with operating-frequency range and requirements on minimum phase determine the maximum transconductance. Linearity determines the return feedback (cathode, emitter, source) resistance and forces the readjustment of undegenerated g_m to provide the required linearity.

After these adjustments have been made, special limitations on parameters such as beta can be considered. You need to make an evaluation, in order of importance, of all the parameters for the active devices you use, and you must make certain that the important data is available in accordance with these needs. Experienced designers can short-circuit many of these decisions, but how many of our young circuit designers know all the answers that engineers like Bob Pease have learned so well by experience?

Device makers *should* provide the information that will enable an engineer with some skill to move directly to a successful solution to a problem. I have yet to see the needed data on even *one* National data sheet on any discrete device. (I hope I have missed one!) The data sheets don't even say that the device transconductance for a bipolar device is roughly $39 \cdot I_O$ (for an ideal, low-injection, negligible r_b'

and r_e' device).

I have yet to see a statement on transconductance efficiency for a FET; what you find is a statement that the transconductance is in a certain range when the output current is in some range at some bias condition. What can you do with that on an exponential-type device? Only kappa modifies the exponential relation by reducing the effective value of q/kT with all these devices.

I appreciate Bob's response, and I hope he will help me upgrade data sheets so that one doesn't need all his years of experience to get a good design the first time. I don't have Spice available (as many don't), and I never have had it. And my designs based on the techniques I have developed almost always work the first time. I regret to say that Spice won't make allowances for the internal degenerative-type resistances whose values are not known.

The key to the issue, as far as I am concerned, is accomplishing a goal with the highest possible MTBF. Are we going to let the rest of the world push us all the way out of business because they use these principles and we don't?

Keats A Pullen Jr
Kingsville, MD

Gap between theory and practice is widening

With reference to Keats Pullen's letter in the March 17 issue of EDN (pg 34): I wholeheartedly agree, and I have had similar experiences. There is a serious gap between the IEEE's articles that are not useful to the average engineer and EDN's articles, which must be so specific that they even include part numbers. Furthermore, I believe the gap is widening because of the fast pace of development. EDN can (and used to!) fill this gap. I keep a notebook full of *old* EDN articles and tutorials, which I refer to and (more often) loan to less experienced engineers. The only recent entries are from more general (nonelectrical) publications such as *Measurements & Control*. The latter seem to be the best bet for working engineers, even if they are oversimplified and contain errors.

Really, isn't it the job of the engineer to fill in the gap between the textbook theory and the manufacturer's application sheets? I think EDN should be more slanted toward *how* to find answers than actually trying to provide them; the manufacturers gladly do the latter if they can.

Art Delagrange
Acoustic Signal Processing Branch
Naval Surface Warfare Center
Silver Spring, MD

(Ed Note: EDN's staff-written articles provide the raw material that helps you find answers. Contributed articles cover the how-to-design topics. We strive for a balanced mixture of both article types.)

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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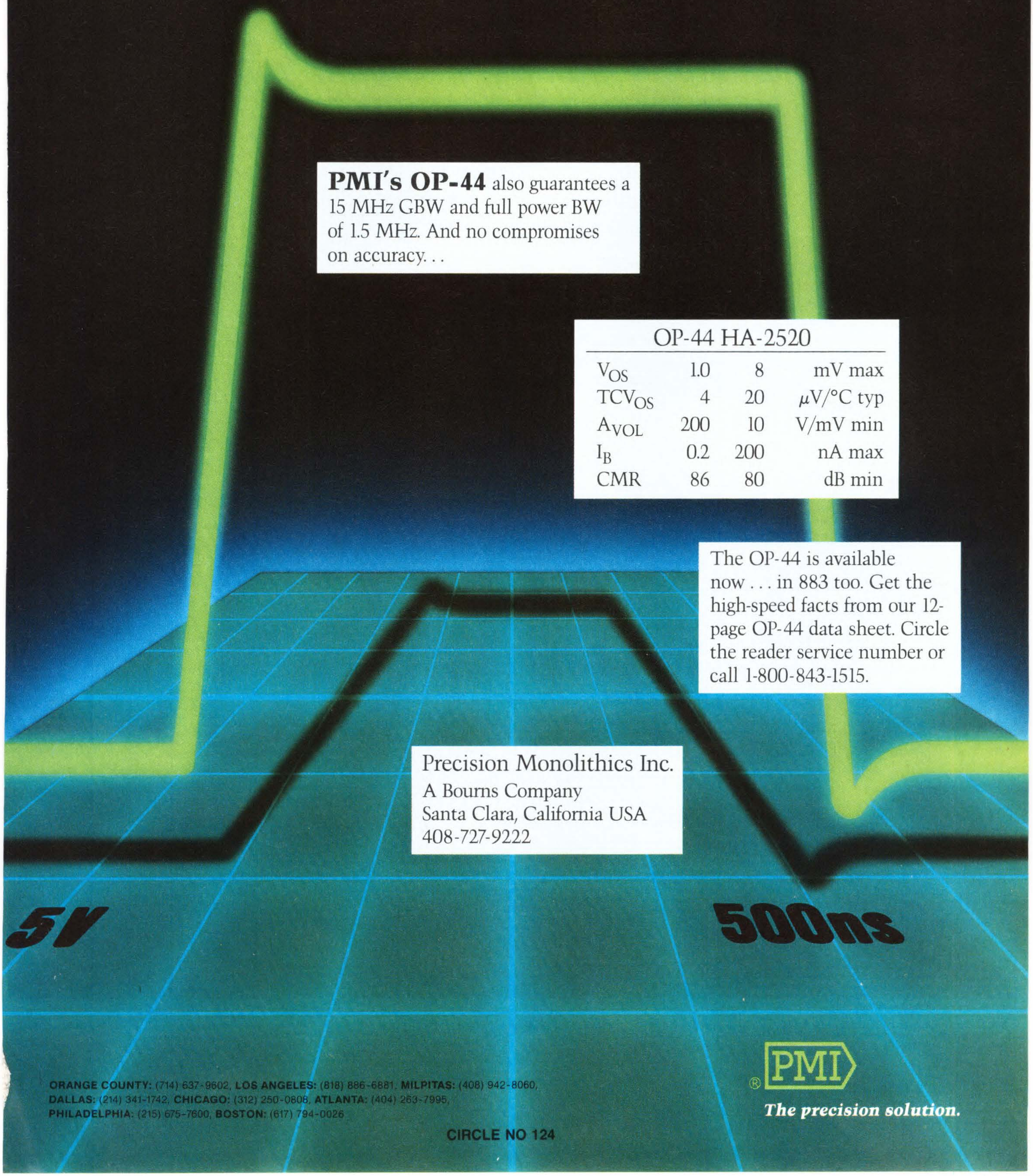

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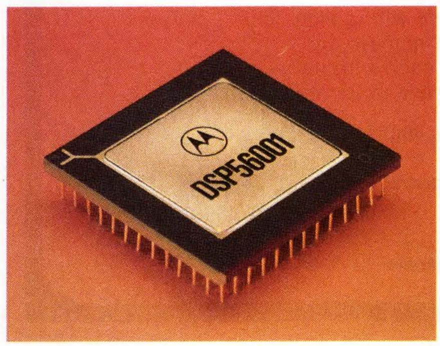

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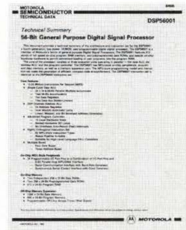

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Unix Hands-on Workshop (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 20 to 23.

34th IEEE Holm Conference on Electrical Contacts, San Francisco, CA. IEEE Holm Conference Registrar, 345 E 47th St, New York, NY 10017. (212) 705-7405. September 26 to 29.

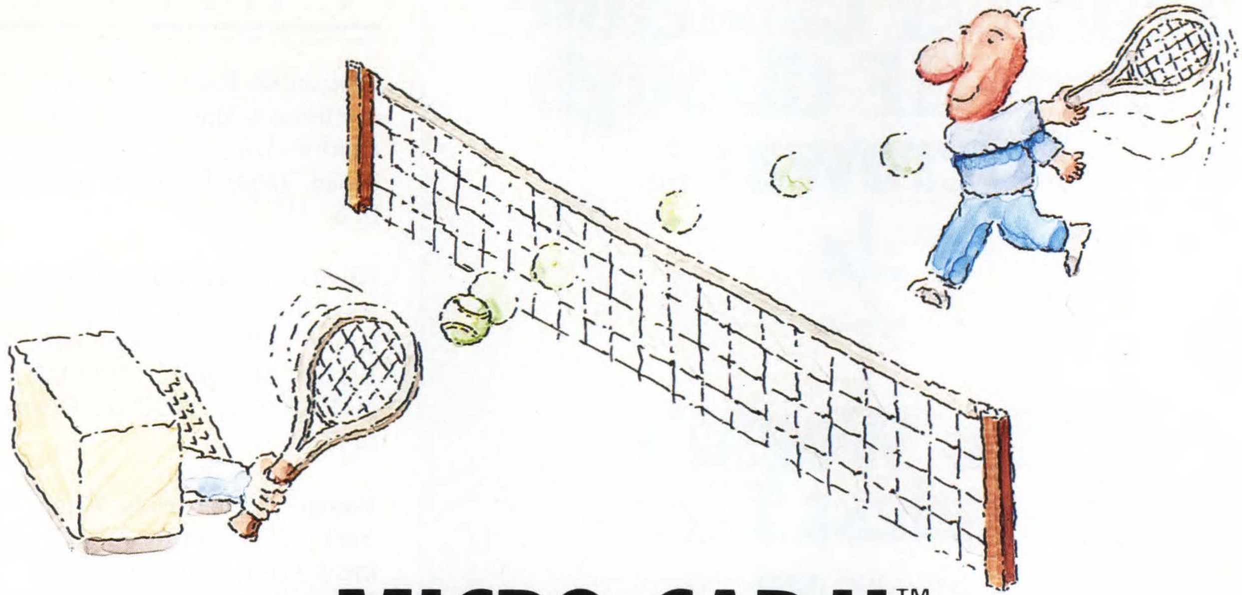
Troubleshooting Microprocessor-Based Equipment and Digital Devices, Chicago, IL. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. September 27 to 30.

Unix Hands-on Workshop (short course), San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 27 to 30.

Connector and Interconnection Technology Symposium, Dallas, TX. Electronic Connector Study Group, 104 Wilmot Rd, Suite 201, Deerfield, IL 60015. (312) 940-8800. October 3 to 5.

IEEE International Conference on Computer Design: VLSI in Computers and Processors, Port Chester, NY. Gail Clanton, IEEE, 1730 Massachusetts Ave NW, Washington, DC 20036. (202) 371-1013. October 3 to 5.

Autotestcon, Minneapolis, MN. Steve Palmer, Unisys, 3333 Pilot Knob Rd, Eagan, MN 55121. (612) 456-2349. October 4 to 6.



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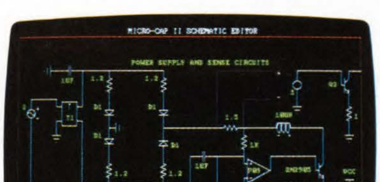

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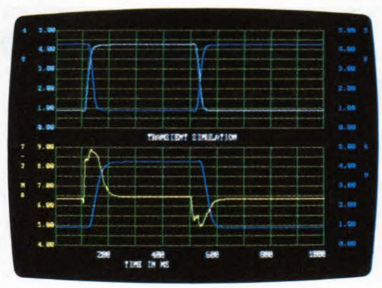

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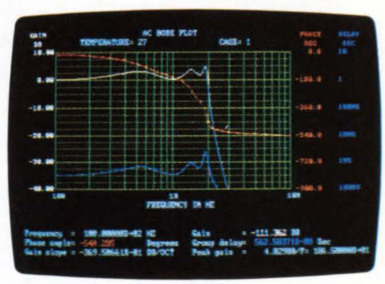

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Electronic Imaging Conference East, Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 4 to 6.

Power Electronics East, New York, NY. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. October 4 to 6.

Frontiers '88: The 2nd Symposium on the Frontiers of Massively Parallel Computers, Fairfax, VA. Frontiers Symposium, Box 334, Greenbelt, MD 20770. October 10 to 12.

International Electronic Manufacturing Technology (IEMT) Symposium, Lake Buena Vista, FL. Bill Moody, 2529 Eaton Rd, Wilmington, DE 19810. (302) 478-4143. October 10 to 12.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Indianapolis, IN. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. October 11 to 14.

Modern Electronic Packaging (seminar), Boston, MA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. October 12 to 14.

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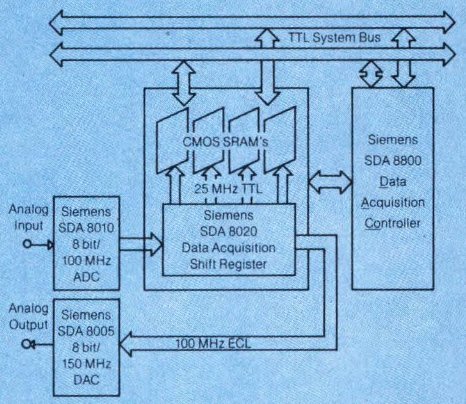

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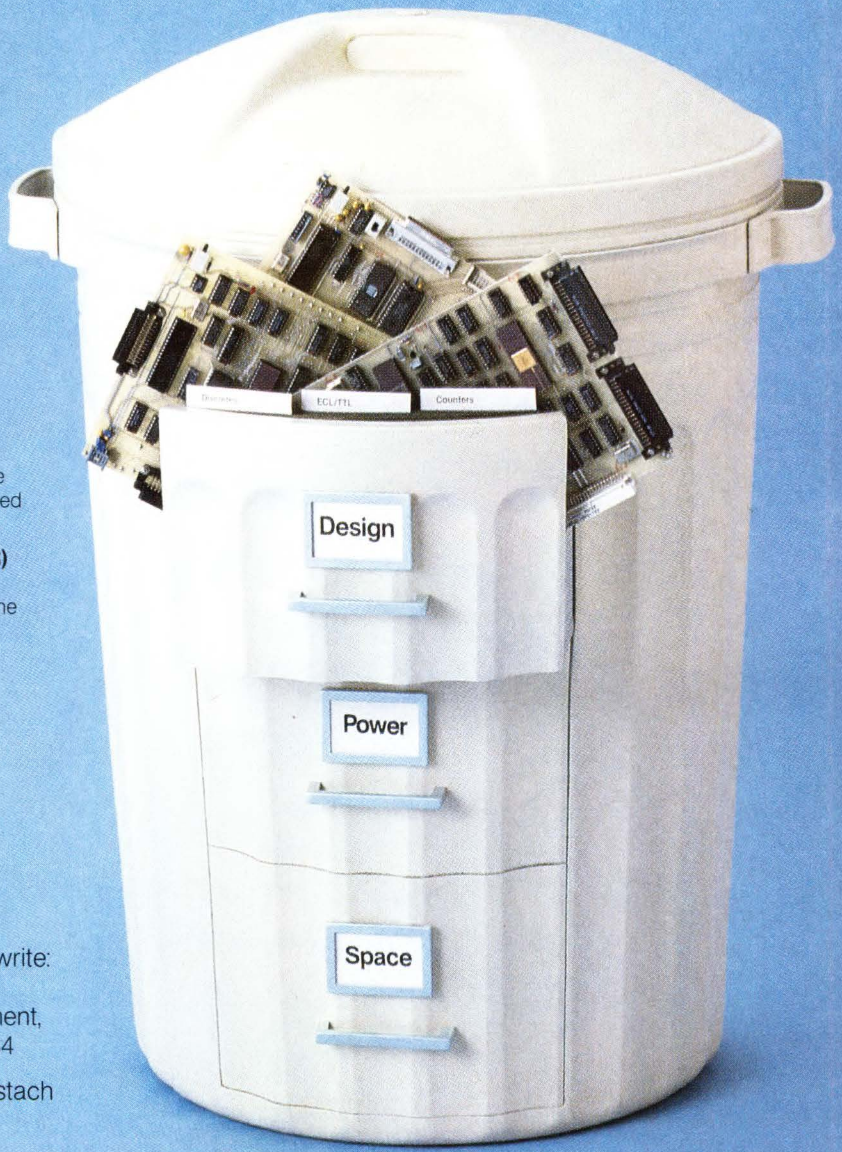

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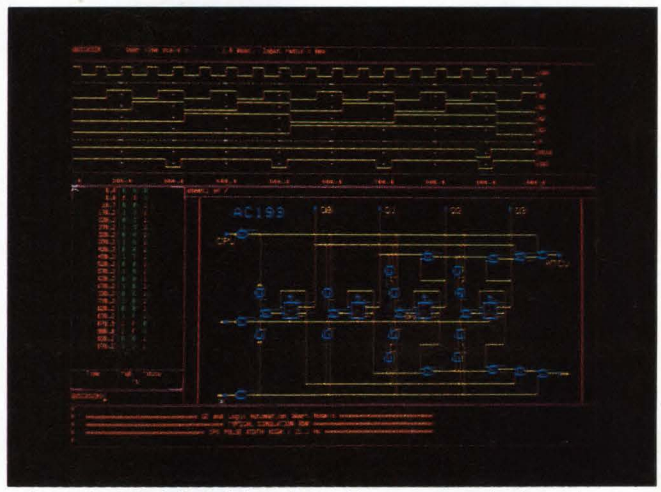

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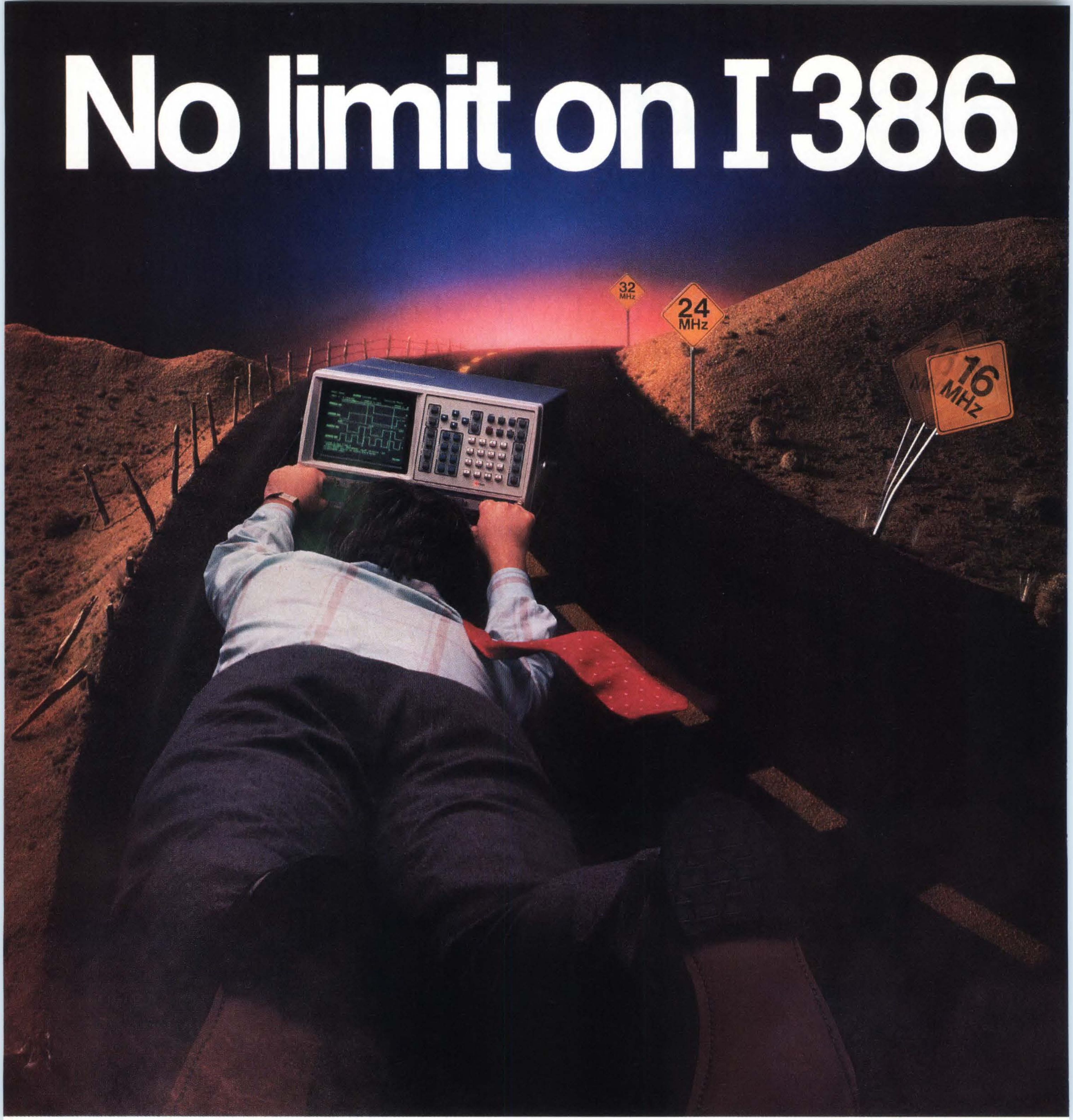

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CIRCLE 29 FOR LITERATURE

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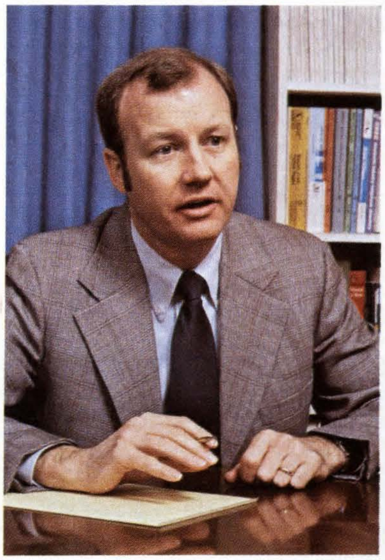
Marketers talk funny



As you talk with electronics-marketing people, you begin to realize that they have a language all their own. Here's a sample of the words and phrases they use along with my translations:

Time frame. Translation: A period or time. Often redundant, as in *the January or February time frame.* Time frames often stretch to match product introductions, and adding the *time frame* preface lets you be imprecise. For example, a January-February *time frame* can stretch into July. A close relative is *window* or *market window*, which usually refers to an even more nebulous period.

Quantum jump. Translation: A big leap, usually upward or forward, as in *a quantum jump in performance.* In truth, however, a quantum jump is an extremely small change in energy, and it can take place up or down. A marketing quantum is undefined, so most marketers mean *a decade leap*, although once in a while we read or hear of *logarithmic* and *exponential leaps.* (How about *a 10-dB increase in performance?*)

Footprint. Translation: Area, or (infrequently), pattern. *Footprint* is a favorite word of computer and workstation suppliers whose products have small *footprints.* What they mean is that the products don't take up much space. (How about *a −3-dB leap in footprint?*). An alternative usage invokes *footprints* to mean standard ASIC-device patterns. Soon someone will be offering a 2-million-gate array dubbed "Bigfoot."

Macro. Translation: Anything big. For example, *the QBX-5 is a macro of our Model 3.* The traditional software-engineering meaning of macro is now archaic. *Macro* also shows up as a verb, as in *to macro*, which is to make something bigger. Teenagers will soon be saying "That's macro" instead of "That's awesome."

Database. Translation: A large collection of data, not necessarily organized. Often simply a synonym for information or data. Thus, *a performance database* is information about a product's performance. People no longer collect information, they *build databases.*

Media. Translation: Just about anything—be it a wire, a floppy disk, a magazine, or an envelope—that holds or transfers information. Often used loosely and with disregard to the singular, *medium.* Both *media* and *medium* are sensitive to context—for example, *crosstalk on the media* could mean electrical crosstalk or an irate discussion between a PR agent and a reporter.

At this point in time. Translation: Now.

Negative time. Translation: a time in the past; before now. Data-acquisition-equipment manufacturers tout an instrument's ability to capture data in *negative time*, an operation we used to call *pretrigger record.* Soon the future will be *positive time* and we can rewrite a certain movie title as "Back to the Positive Time."

Platform. Translation: No, not a structure made of wood, steel, concrete, or other construction materials—a computer. Although many electronics companies say that their products *run on specific platforms*, in fact only politicians and commuters run on platforms, and the politicians run slowly.

Engine. Translation: A mechanism of some sort, usually associated with graphic displays or printers. I've always thought of an engine as a mechanism powered by an expanding gas; that is, a steam engine or a jet engine. However, the computer-publicity people may soon describe *engines* that *run on platforms*—probably next to the politicians.

I haven't exhausted my list, but that's all I can fit in this issue. I'm still wondering where the marketers picked up these expressions. Maybe they were hanging around the engineering department too long.

Jon Titus
Editor

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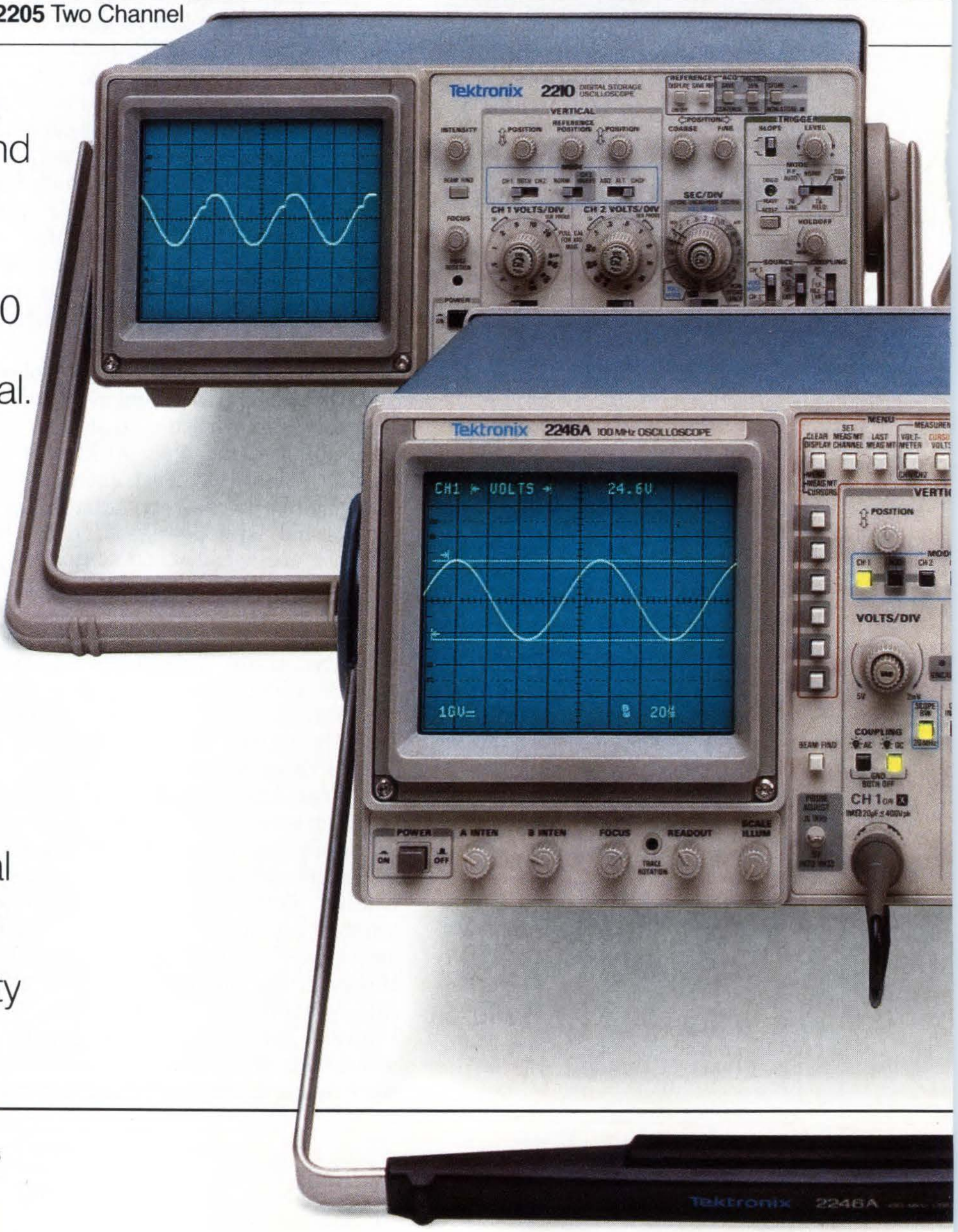

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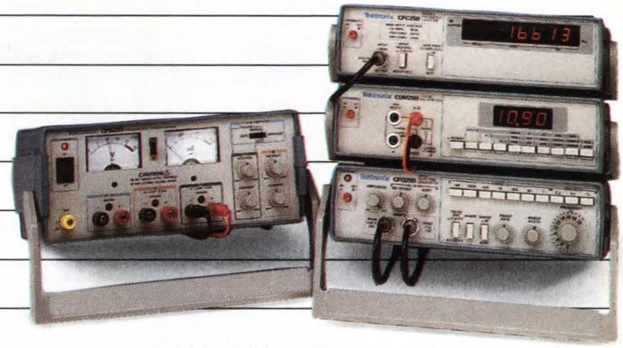

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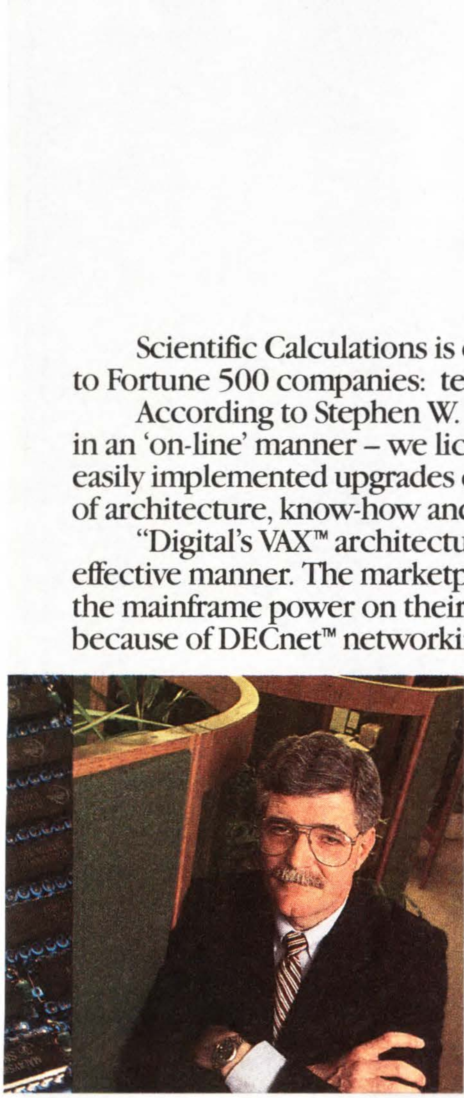

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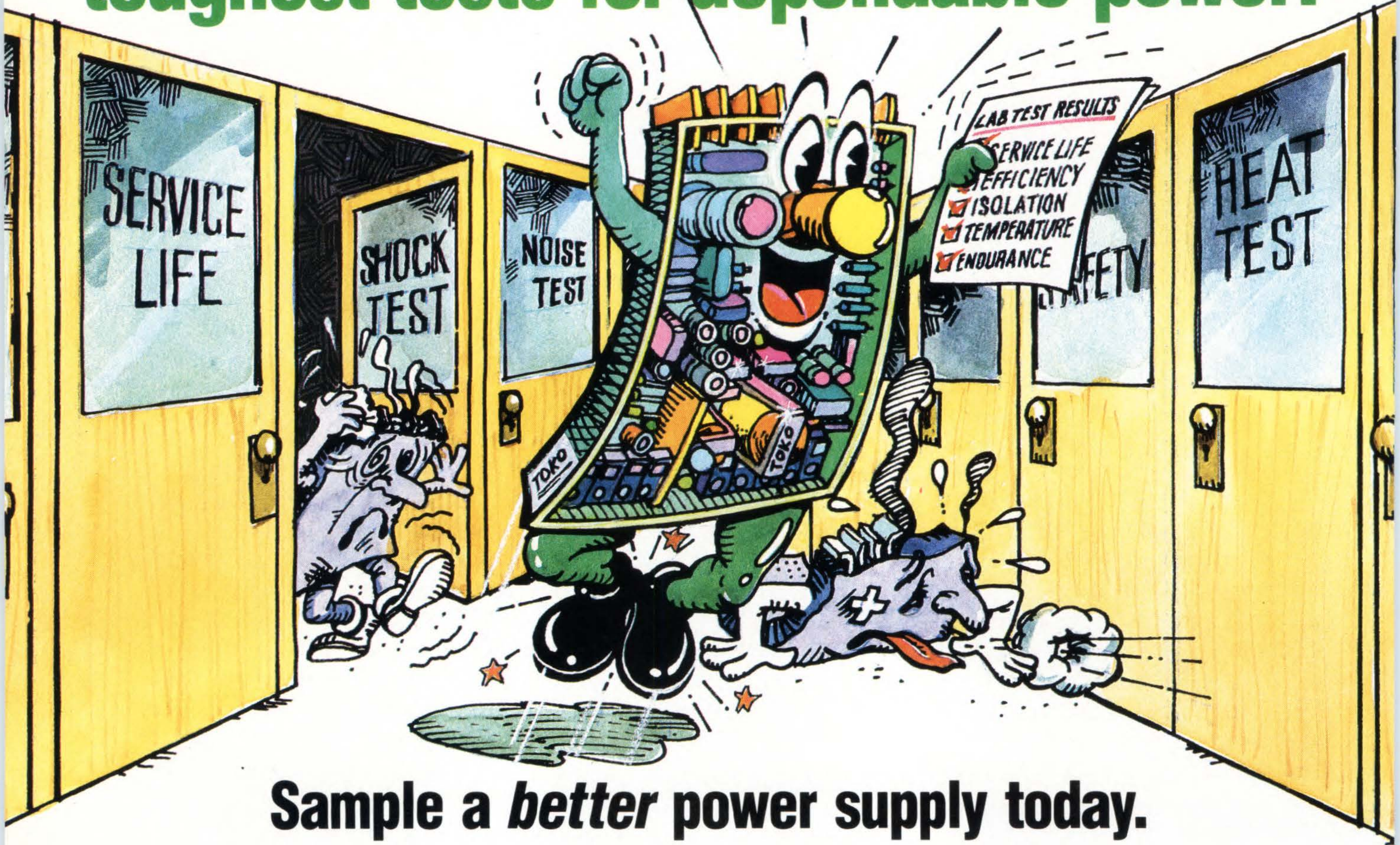

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ET	85-132	10/15W	3	2.6"	4.5"	1.3"
EM	170-264	10/15W	3	2.6"	4.5"	1.3"
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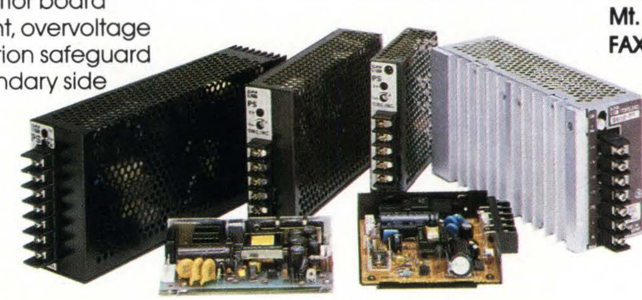

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CIRCLE NO 130

As brushless dc motors decrease in cost, designers find them much more practicable

John Gallant, *Associate Editor*

Brushless dc motors, long ignored by system designers except for applications with stringent or special requirements, are now expanding their niche. The motors have always boasted many advantages: minimal EMI problems, superior heat dissipation, no arcing side effects, and high rotational speeds. The deciding factor, from the viewpoint of the system designer, has always been the attendant high cost.

Until the mid-1970s, system designers had only two choices when selecting an electromagnetic motor for a particular application: a brush-type dc motor or an ac wound-rotor induction motor. A brush-type dc motor is practical for applications that require a relationship between linear motor speed and torque. **Fig 1a** shows typical speed-vs-torque curves for a dc motor. Contrast these curves with the speed-vs-torque relationship for a polyphase ac induction motor **(Fig 1b)**. As you can see by the curve, the ac motor is only useful when operating within 90 to 100% of its synchronous speed; the synchronous speed depends on the excitation frequency.

Brush types of dc motors aren't ideal, though. Eventually motor designers devised a brush*less* type of dc motor. Initially, the extra cost of the circuitry required for a brushless dc motor confined it to special applications. Today, however, the cost differential between brushless and brush-type dc motors has decreased to the extent that brushless dc motors are becoming much more feasible for an increasing number of applications.

DC motors come in two guises

A brush-type dc motor consists of a stator made from a permanent magnet that creates a magnetic field. A rotor with wound coils rotates within the stator. The wound coils connect to the rotor's commutator, which consists of segments of conductive material interspersed with an insulation material. Brushes that press against the commutator carry dc current to the coils. As the motor rotates, the current in the coils alternates to control the speed of the motor.

The brush-type method of commutation proves to be a limitation in certain applications. The wear and tear on the brush and commutator surfaces, for example, affects the reliability of the motor and its lifespan. This type of commutating also causes EMI problems and produces electrical arcing, which can cause problems in particular environments. In addition, it limits the maximum no-load rotational speed of the motor to less than 10,000 rpm.

A brushless dc motor, in contrast, consists of a stator made from wound coils. It is these coils that create the magnetic field. The field rotates when the phase of the current in the coils changes in a prescribed manner, and the rotor consists of a multiple-pole permanent magnet that continually aligns itself with the rotating field. The electri-

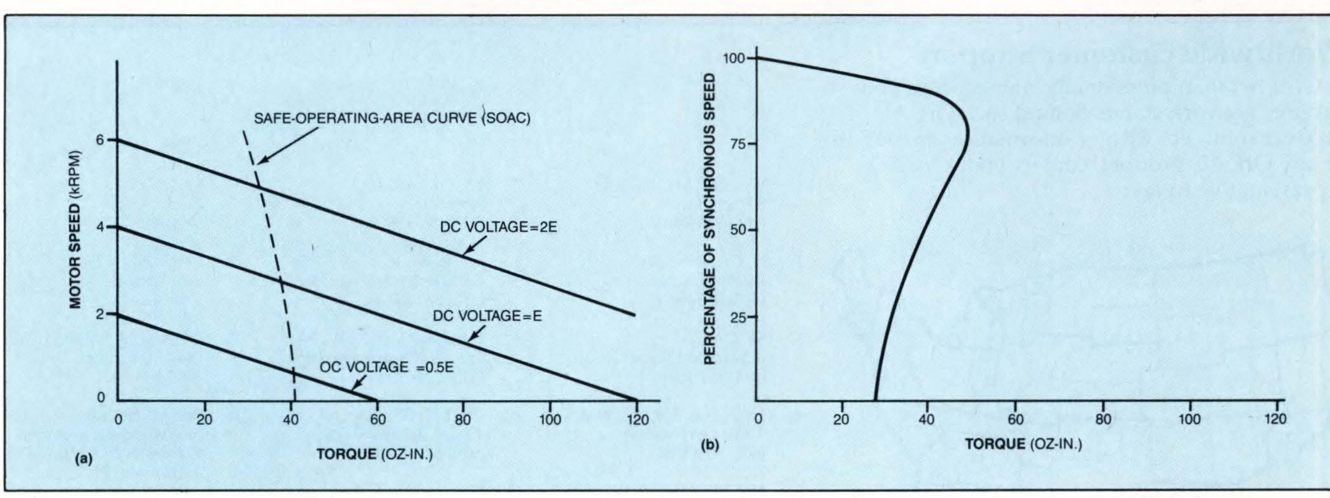

***Fig 1—Speed-vs-torque curves** for various input dc voltages usually describe a dc motor's operating characteristics **(a)**. The area to the left of the SOAC indicates an area of continuous operation based on the thermal properties of the motor. AC motors are usually specified as a percentage of synchronous speed vs torque **(b)**. These types of motors are useful only in the upper region of the curve.*

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CIRCLE NO 131

cal commutatation of the current through the stator windings means that a brushless dc motor doesn't emit as much EMI as a brush type does. And, there are no brushes to wear out or produce arcing.

This method of commutation results in motors with very high rotational speeds. In fact, Inland Motor has built custom brushless dc motors that run at no-load speeds of 80,000 rpm.

The brushless dc motor also dissipates heat more quickly than its brush-type counterpart. Because the current-carrying wires are inside the stator instead of the rotor, they are closer to the surface of the motor. As a consequence, the brushless motor has a lower thermal resistance. Brushless dc motors with a given continuous-torque rating can be smaller in size than their brush-type dc counterparts because the wire can have a smaller diameter.

The cost of the electronics necessary to drive a brushless dc motor still makes them a more-expensive alternative to the brush-type dc motor. Whereas a brush type of dc motor requires only a single dc amplifier, a 3-phase brushless dc motor (for example) requires three amplifiers and three sensor signals to commutate them.

Consider Baldor's general-purpose brushless dc motors, for instance. The ½- to 2-hp motors run at 1800 rpm and have their drive and control electronics, along with a 3-phase rectifier requiring a 230V ac 3-phase input, all in the same housing. A ½-hp model and a 2-hp version cost $1500 and $1850, respectively. The electronics package by itself sells for $1150.

Cost may be worth it

The cost differential may not actually be prohibitive. Baldor's marketing manager Darryl J Van Son estimates that, for an equivalent application, the added cost of a brushless dc motor compared to a brush-type is only 15 to 20% higher. Indeed, in many applications this increased premium is actually cost efficient. Brush maintenance and down time is eliminated, for instance. Two brushless dc motors on each of the two Voyager space probes have performed flawlessly for over 10 years in the unmaintainable void of outer space.

Also, because no arcing occurs during the commutation period, vacuum and explosive atmospheres do not need protection from it. In applications such as medical equipment and computer environments, which can't tolerate EMI pollution, the omission of brushes reduces the cost of meeting emission requirements.

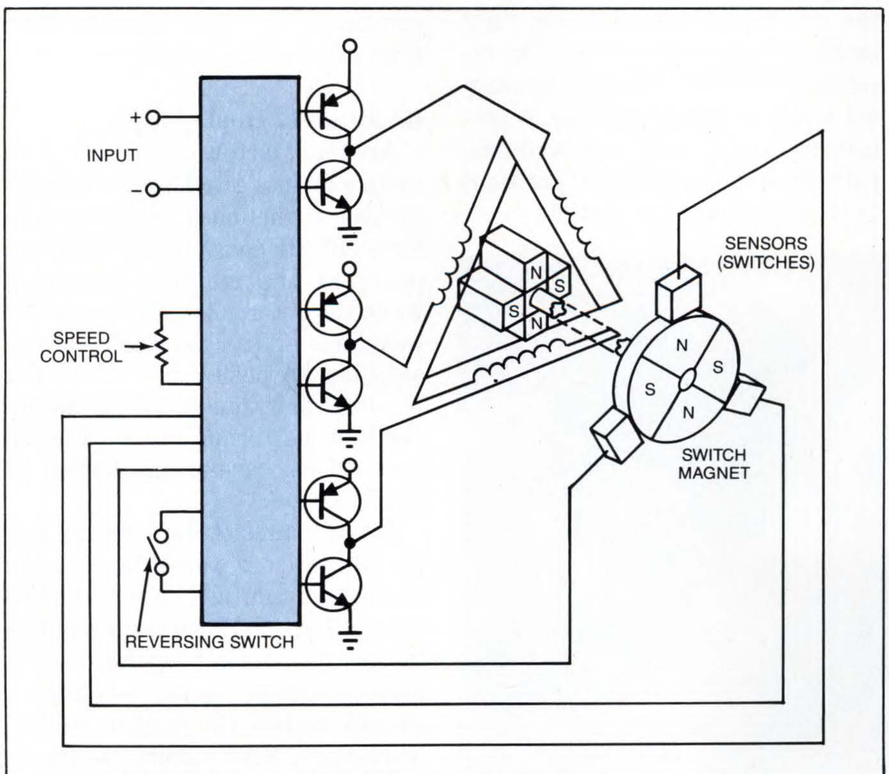

Fig 2—The principle of operation *of most brushless dc motors consists of 3-phase stator windings that surround a multiple-pole permanent-magnet rotor. The shaft of the rotor connects to the three sensors, which detect the rotor's position and electrically commutate the current through the windings. (courtesy Eastern Air Devices)*

Three-phase type is standard

Although 4-phase brushless dc motors do exist, 3-phase types predominate **(Fig 2)**, primarily because of the availability of economical 3-phase circuitry. Eastern Air Devices' brushless dc motors, for example, have 3-phase windings and either 2-pole or 4-pole permanent-magnet rotors. The rotors can be either ferrite or rare-earth magnets, depending on an application's cost constraints and requirements.

The rotor shaft connects to three radially positioned Hall-effect or optical-sensor switches. The sensors detect the angular position of the magnetic poles of the rotor relative to the 3-phase windings. The signals from the sensors provide either velocity feedback or phase-locked-loop signals to control the speed of the motor.

Eastern Air Devices' standard offerings range from the DB10D-30, with a full-load current of 0.26A, a no-load speed of 11,500 rpm, and a peak starting torque of 0.5 oz-in., to the DB39D-32, with a specified full-load current of 10.0A, a no-load speed of 5300 rpm, and a peak starting torque of 200 oz-in. The motors also have a specified torque constant, K_T, which can range from 3 to 25 oz-in./A. They run from 24V dc supplies and offer electronic braking and reversibility.

Prices for a standard model vary tremendously: A motor without electronic drive circuits and with inexpensive ferrite magnets costs $50, whereas a motor with electronic drive circuitry and rare-earth magnets sells for $300.

If you opt for a motor without electronic drive circuitry, you'll need to estimate how much power will be necessary to drive the motor. According to Jeffrey Arnold, an applications engineer for Inland Motor, the motor constant, K_M, of a brushless dc motor provides a good rule of thumb for determining how much power the motor will need.

The motor constant is related to the torque constant according to the equation: $K_M = KR$ represents the resistance of the winding. By knowing the motor constant and your torque specification, you can determine the motor's power requirements by solving the following equation: power in watts = torque^2/K_M^2.

Although all motors strive to maintain constant torque over time, variations in torque materialize as a motor rotates. One variation, known as cogging torque, is due to the change in reluctance of the permanent magnets' field path as the brushless dc motor rotates. Motor manufacturers specify cogging torque as a fixed torque that is superimposed on the applied torque.

The cogging effect is most noticeable when the applied torque is low. In fact, you can manually rotate the rotor of a brushless dc motor (with no power applied) and feel detent positions where the rotor tends to resist rotation.

Brushless dc motor manufacturers have devised a number of techniques to reduce cogging torque to a negligible quantity. Baldor, for example, minimizes cogging torque by skewing the field of the permanent magnet. Baldor's Van Son explains the skewed-magnetic-field concept this way. Suppose you're holding a coffee cup, and the top of the cup represents the north pole of the magnet and the bottom characterizes the south pole. Now, imagine you could twist the top to the left and the bottom to the right (without spilling the coffee). The resultant field path through the magnet would be spiral in shape. A permanent magnet with a skewed field path finds less-preferred positions as it rotates past the stator.

These general-purpose 3-phase brushless dc motors, *which come with 1/2- to 2-hp ratings, are available from Baldor Corp.*

Other vendors attempt to make the reluctance path through the stator more linear. Pittman, a manufacturer of standard 4- and 3-phase dc brushless motors with rotational speeds reaching 25,000 rpm, uses a toothless laminated structure in which a skewed winding reduces perturbations in the magnetic circuit.

NMB Inc uses an inverted structure where the permanent magnet rotates around a fixed polyphase inner stator. The NMB motors' stators use a series of concentric coils encapsulated on a Mylar sheet and wrapped around a soft ferrite cylinder (known as sheet coil technology). The stator current rotates through sets of offset coils to maintain a nearly constant reluctance path and thereby minimize cogging.

NMB's brushless dc motors are intended exclusively for spindle-motor drives in Winchester and optical disk-drive assemblies. The LM-3H-01 and the LM-3H-04, for example, are designed for 3½-in. spindle motors; they range in price from $16 to $22 (100,000).

Be aware of ripple torque

Another factor contributing to variations in a brushless dc motor's torque is the back electromotive force (BEMF) waveform, which appears at the winding terminals when the rotor rotates. The BEMF waveform affects the ability of the amplifier to push current into the winding, and thus it affects the instantaneous torque value. The effect of this waveform is known as ripple torque.

Motor manufacturers specify ripple torque as a percentage of the applied torque, and it is therefore most noticeable for a large applied torque. For smooth operation, the motor-current drive waveform should match the motor BEMF waveshape. Most motors use trapezoidal drive waveforms to control motor speed. Sinusoidal waveforms exhibit less ripple torque, however. Inland Motor specializes in custom-

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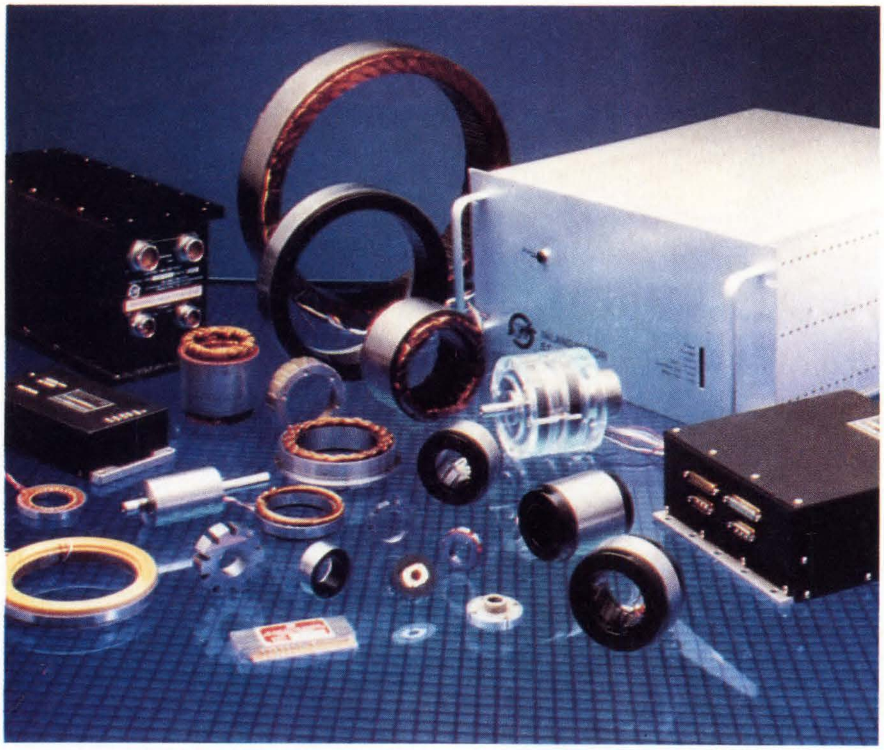

***You can meet the requirements** of your particular application by choosing from Inland Motor Co's custom core-motor structures.*

built brushless dc motors with sinusoidal BEMF drive waveforms. Cost estimates vary, depending on application requirements, but a typical estimate is $2/W.

AC brushless = dc brushless

When a dc brushless motor employs sinusoidal phase currents and a large number of poles on the rotor (10 or more), it is often referred to as an ac brushless motor. This type of motor is especially suitable for high-torque applications and their requisite slow-speed servomechanism operations.

Contraves Goerz Corp, for instance, builds its so-called ac brushless motors with as many as 64 rare-earth magnetic poles bonded to a thin rotor ring (ring motor). Rare-earth magnets, such as samarium cobalt or neodymium iron boron, have higher coercivity than ferrite magnets and are smaller and lighter for a given torque-to-inertia ratio.

The large number of poles on ac brushless motors reduces cogging torque at very low speeds. However, because commutation must be performed for each pole, the control electronics is complicated. An ac brushless motor requires a μP to perform the commutation operation and to process velocity and position feedback information.

All of the previously discussed motors come in their own enclosed housing. A number of manufacturers do offer frameless brushless dc motors, however. These motors consist of the wound stator and a permanent-magnet rotor that can be attached directly to a shaft of a rotating device. The unhoused motors make it possible to eliminate gears, belts, and other couplings.

BEI Motion Systems Co offers six off-the-shelf frameless motor designs. At the low end is the 4-pole DXP09-04E, which has a peak starting-torque rating of 2.1 oz-in., a motor constant of 18.4 oz-in./$\sqrt{\text{watts}}$, and a maximum recommended speed rating of 20,000 rpm. At the high end is the 8-pole DIP37-19A, with a peak starting-torque rating of 600 oz-in., a motor constant of 18.4/$\sqrt{\text{watts}}$, and a maximum recommended speed rating of 6000 rpm. Options include bore size, winding configuration, length, and a printed-circuit board with Hall-effect transducers. The DXP09-04E costs $69, and the DIP37-19A costs $259. EDN

Article Interest Quotient
(Circle One)
High 512 Medium 513 Low 514

For more information . . .

For more information on the brushless dc motors described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Eastern Air Devices Inc
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Inland Motor
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50	BUZ11FI	20.0	BUZ11	30.0
60	MTP3055AFI	10.0	MTP3055A	12.0
60	IRFP151FI	26.0	IRFP151	40.0
60	MTH40N06FI	26.0	MTH40N06	40.0
100	IRF520FI	7.0	IRF520	9.2
100	IRF530FI	9.0	IRF530	14.0
100	IRF540FI	15.0	IRF540	28.0
100	TSD4M150V*	100.0		
200	IRF620FI	4.0	IRF620	5.0
200	TSD4M250V**	80.0		
400	IRF730FI	3.5	IRF730	5.5
400	IRF740FI	5.5	IRF740	10.0
400	TSD4M350V**	40.0		
450	TSD4M451V**	35.0		
500	IRF830FI	3.0	IRF830	4.5
500	IRF840FI	4.5	IRF840	8.0
500	IRFP450FI	9.0	IRFP450	14.0
500	TSD4M450V**	35.0		
600	MTP3N60FI*	2.5	MTP3N60*	3.0
600	MTH6N60FI*	3.5		
600			MTP6N60*	6.0
800	***		STHV82	5.5
1000	TSD5MG40V*	13.0		
1000	***		STHV102	4.2

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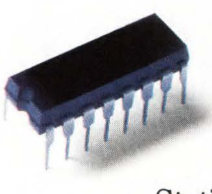

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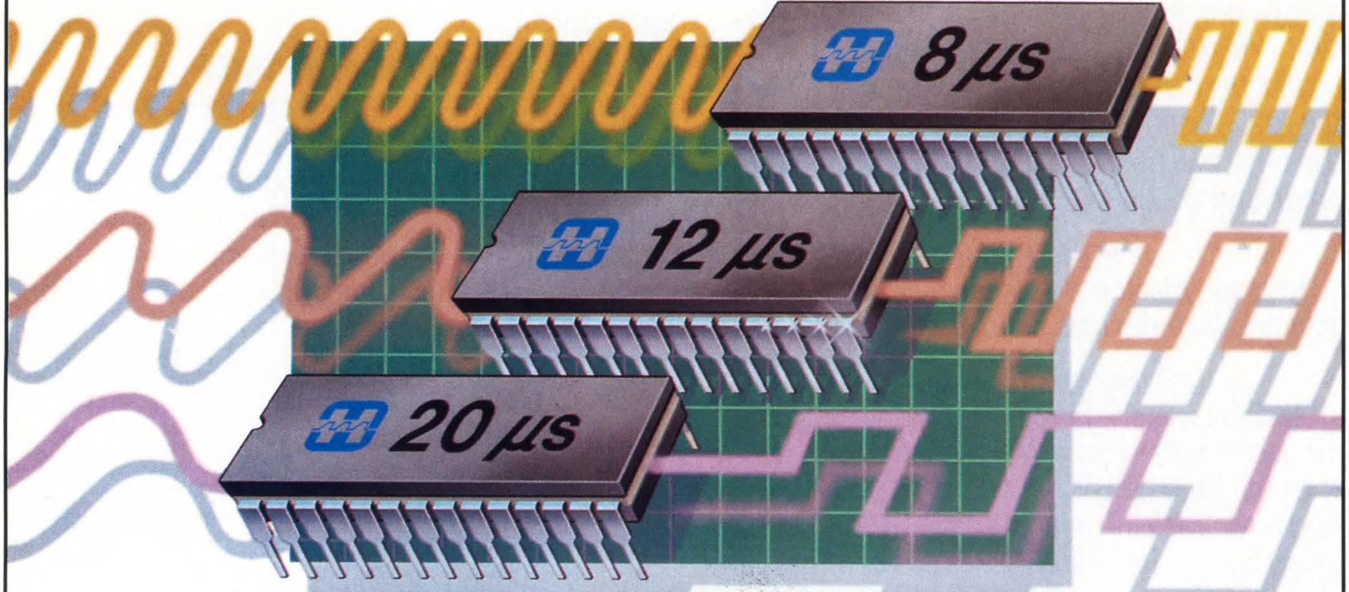

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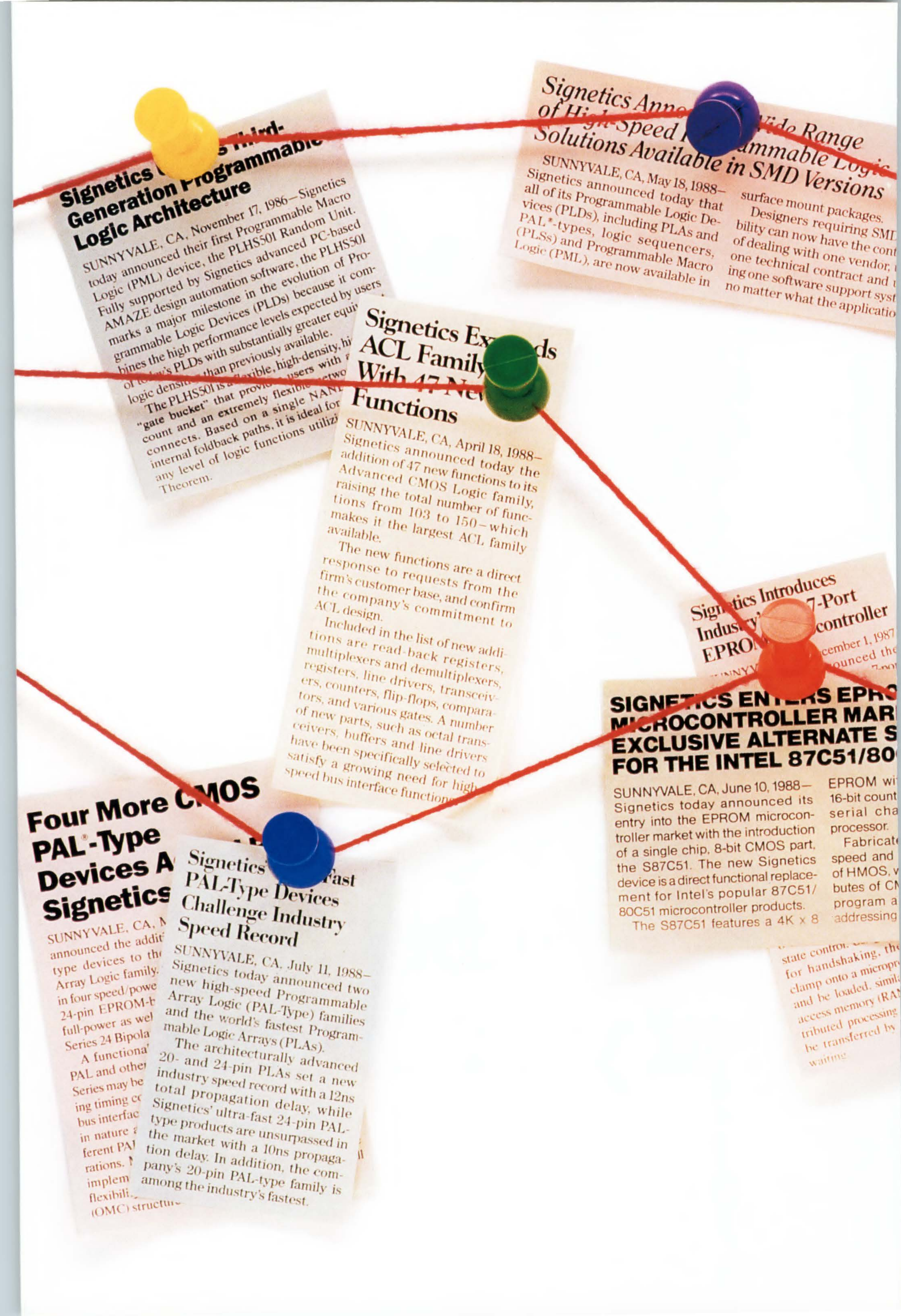
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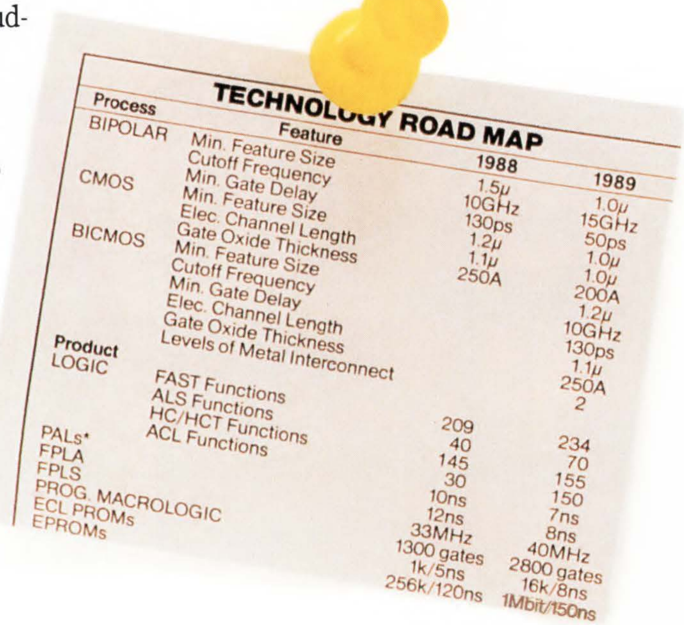
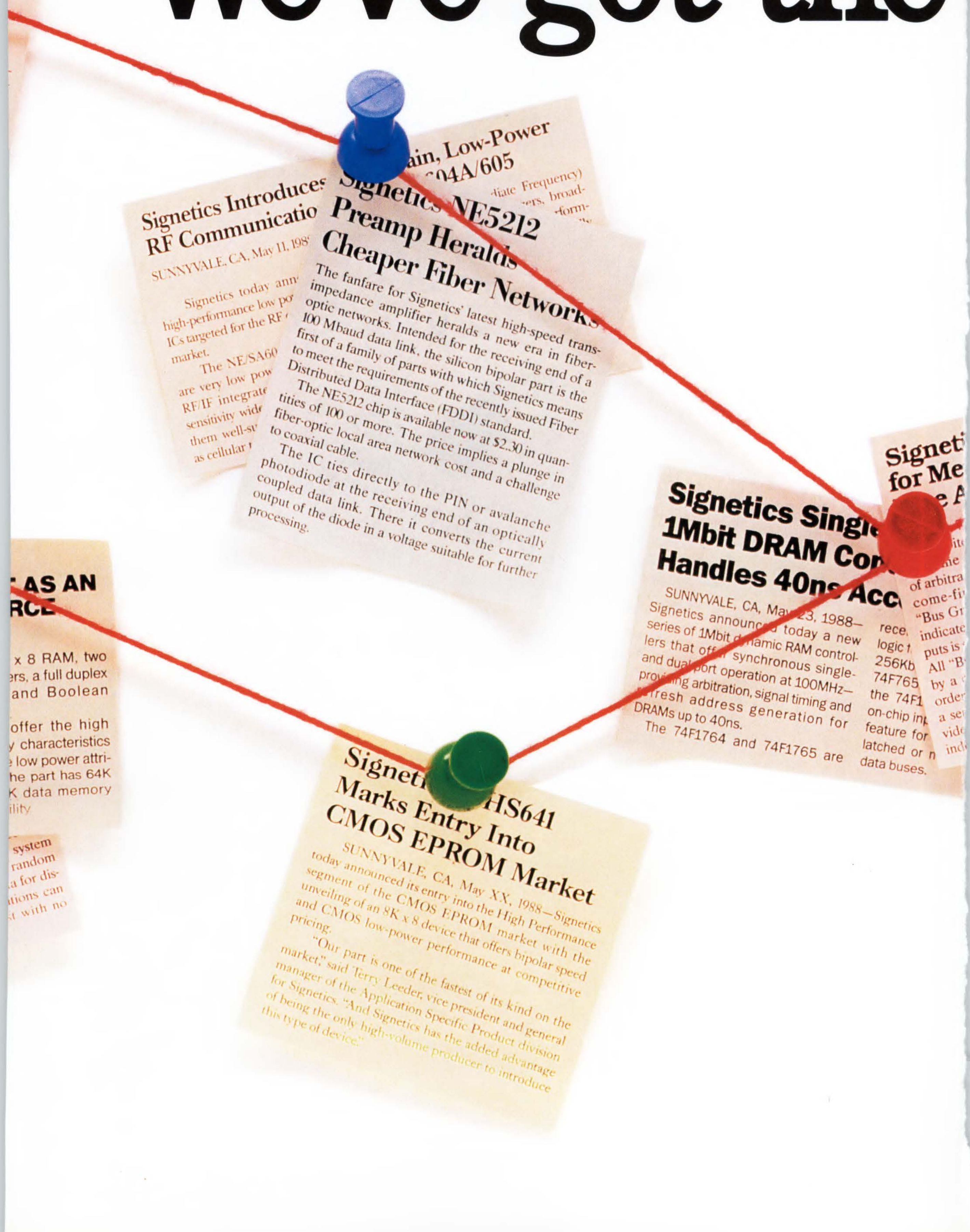

TECHNOLOGY ROAD MAP

Process	Feature	1988	1989
BIPOLAR	Min. Feature Size	1.5µ	1.0µ
	Cutoff Frequency	10GHz	15GHz
	Min. Gate Delay	130ps	50ps
CMOS	Min. Feature Size	1.2µ	1.0µ
	Elec. Channel Length	1.1µ	1.0µ
	Gate Oxide Thickness	250A	200A
BICMOS	Min. Feature Size		1.2µ
	Cutoff Frequency		10GHz
	Min. Gate Delay		130ps
	Elec. Channel Length		1.1µ
	Gate Oxide Thickness		250A
	Levels of Metal Interconnect		2
Product			
LOGIC	FAST Functions	209	234
	ALS Functions	40	70
	HC/HCT Functions	145	155
	ACL Functions	30	150
PALs*		10ns	7ns
FPLA		12ns	8ns
FPLS		33MHz	40MHz
PROG. MACROLOGIC		1300 gates	2800 gates
ECL PROMs		1k/5ns	16k/8ns
EPROMs		256k/120ns	1Mbit/150ns

We've got the



Signetics NE5212 Preamp Heralds Cheaper Fiber Networks
The fanfare for Signetics' latest high-speed transimpedance amplifier heralds a new era in fiber-optic networks. Intended for the receiving end of a 100 Mbaud data link, the silicon bipolar part is the first of a family of parts with which Signetics means to meet the requirements of the recently issued Fiber Distributed Data Interface (FDDI) standard.
The NE5212 chip is available now at $2.30 in quantities of 100 or more. The price implies a plunge in fiber-optic local area network cost and a challenge to coaxial cable.
The IC ties directly to the PIN or avalanche photodiode at the receiving end of an optically coupled data link. There it converts the current output of the diode in a voltage suitable for further processing.
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SUNNYVALE, CA, Ma 23, 1988—Signetics announc today a new series of 1Mbit amic RAM controllers that off synchronous single- and dua port operation at 100MHz— ng arbitration, signal timing and resh address generation for DRAMs up to 40ns.
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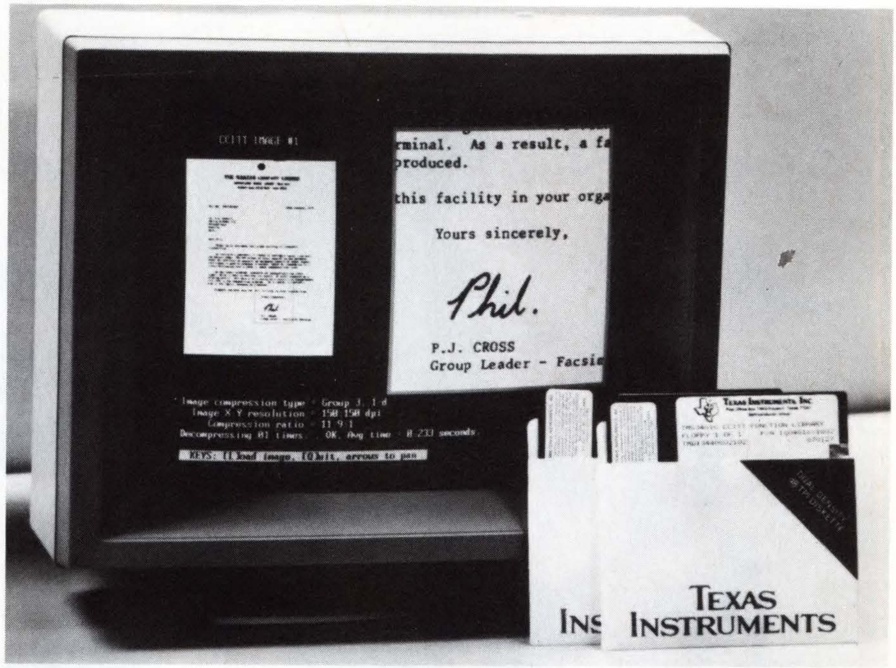
CMOS EPROM Market
SUNNYVALE, CA, May XX, 1988—Signetics today announced its entry into the High Performance segment of the CMOS EPROM market with the unveiling of an 8K x 8 device that offers bipolar speed and CMOS low-power performance at competitive pricing.
"Our part is one of the fastest of its kind on the market," said Terry Leeder, vice president and general manager of the Application Specific Product division for Signetics. "And Signetics has the added advantage of being the only high-volume producer to introduce this type of device."

Widespread graphics use spawns diversity in data-compression devices

J D Mosley, *Regional Editor*

The increasingly pervasive use of graphics has generated a need for the efficient transmission and storage of graphic images—two tasks for which data-compression techniques are well suited. Today's options are varied and include hardware, board, and software products. Facsimile transmission or fax, for example, has long been of interest to the Japanese, who can use neither the American Standard Code for Information Interchange (ASCII) nor the Extended Binary Coded Decimal Interchange Code (EBCDIC) to transmit the characters of their language. And now the ever-increasing demands for high-speed communication via local-area networks, the rising use of document scanners, and the need for efficient mass storage of graphics on magnetic and optical disks have together fired the interest of American engineers in data compression.



Data-compression techniques based in software provide the maximum flexibility *to meet new design requirements or future changes in technical standards. The CCITT Function Library from Texas Instruments lets you transform a TMS34010 Graphics System Processor into an efficient data-compression processor.*

A single $8\frac{1}{2} \times 11$-in. page scanned at a resolution of 300×300 pixels/in. requires more than 1M byte of storage and takes 15 minutes to transmit via a 9600-baud modem. To reduce the expense of bit-mapped storage and communication, CCITT established international standards for compressing monochrome data for digital facsimile transmission.

The two most popular compression algorithms presented by the CCITT are the 1-D Modified Huffman (MH) and the 2-D Modified Relative-Element Address-Designate (Modified READ or MR) codes. MH encoding translates run lengths of identical pixels into binary codes, whereas MR encoding compares adjacent scanned lines for color changes.

The MH algorithm removes redundant information in a single scanned line by assigning a run-length code to each 64-pixel length of data. The code indicates the number of consecutive black or white pixels encountered along the scan line. Although MH encoding offers faster processing speeds, its compression ratios fall short of those obtained using 2-D encoding.

MR 2-D encoding compares a scanned line of pixels to the line of pixels immediately above it and encodes the scanned pixels in a way that takes advantage of the similarities between the two lines. The scanned line then becomes the reference for the next line to be scanned. The MR algorithm is more complex than MH—it compares the scan line to the line immediately above (the reference line) and assigns a code that identifies relative changes in pixel colors between the two lines.

The MR 2-D encoding results in greater data compression than the MH algorithm can achieve. MR ratios of pixels to code bits range from 7:1 to 50:1; MH ratios typically run between 5:1 and 15:1. However, 2-D encoding requires temporary storage of the reference line data, and demands more complex logic circuits and memory configurations than MH schemes. Also, MR encoding errors are propagated throughout the entire document, whereas an MH error remains isolated.

These two CCITT algorithms also share some limitations: They specifically address monochrome data—compression standards for gray-scale and color images do not

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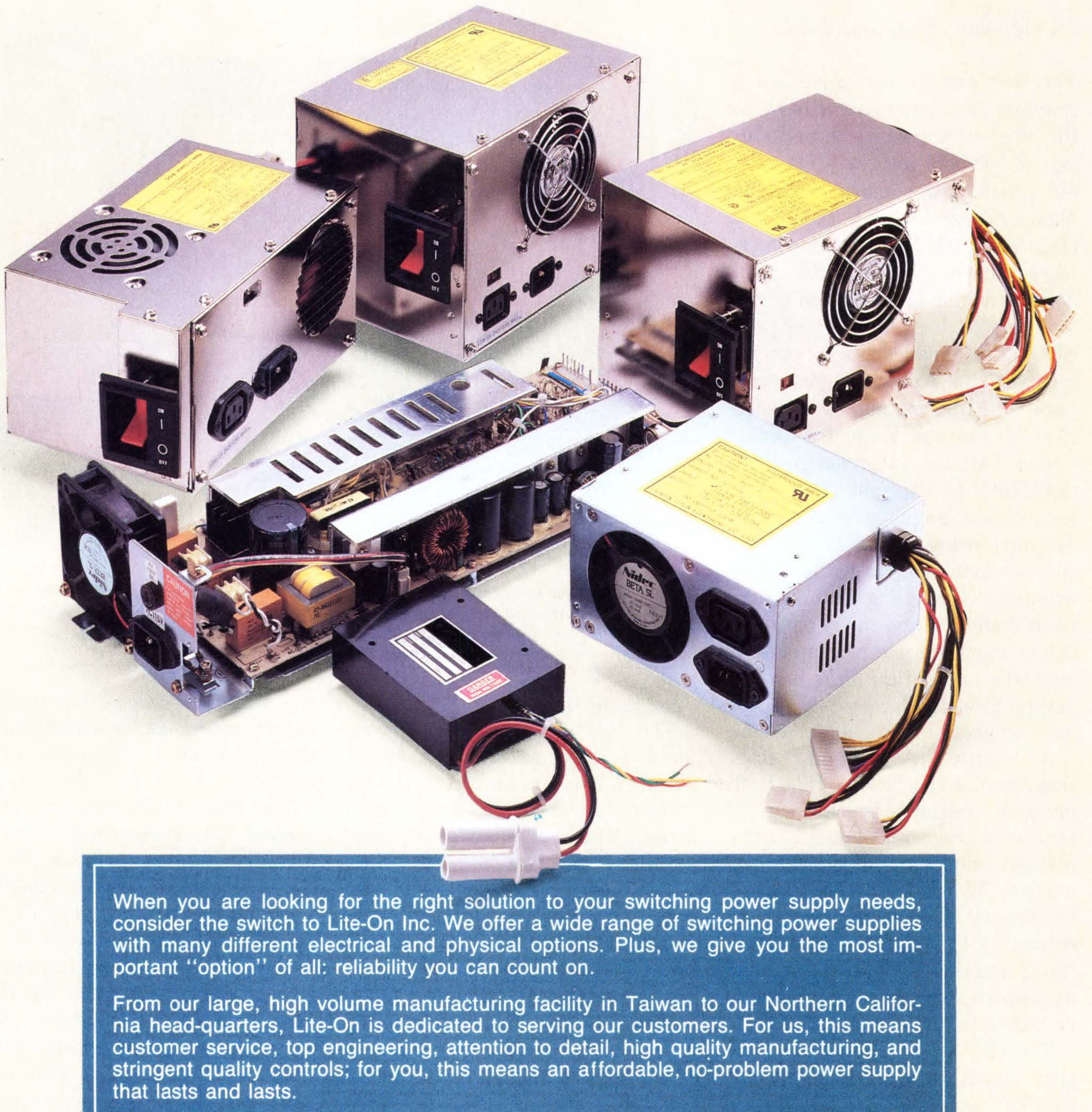

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yet exist. Although you can present RGB color images as three distinct layers of gray-scale data, the randomness of gray-scale image patterns presents a special problem. The more random the patterns, the harder it is to compress an image; in fact, it's impossible to compress purely random data.

Some fax manufacturers have developed proprietary schemes for compression and decompression of nonmonochrome graphics, but using these schemes requires that the sending and receiving fax machines come from the same manufacturer and use the same algorithms.

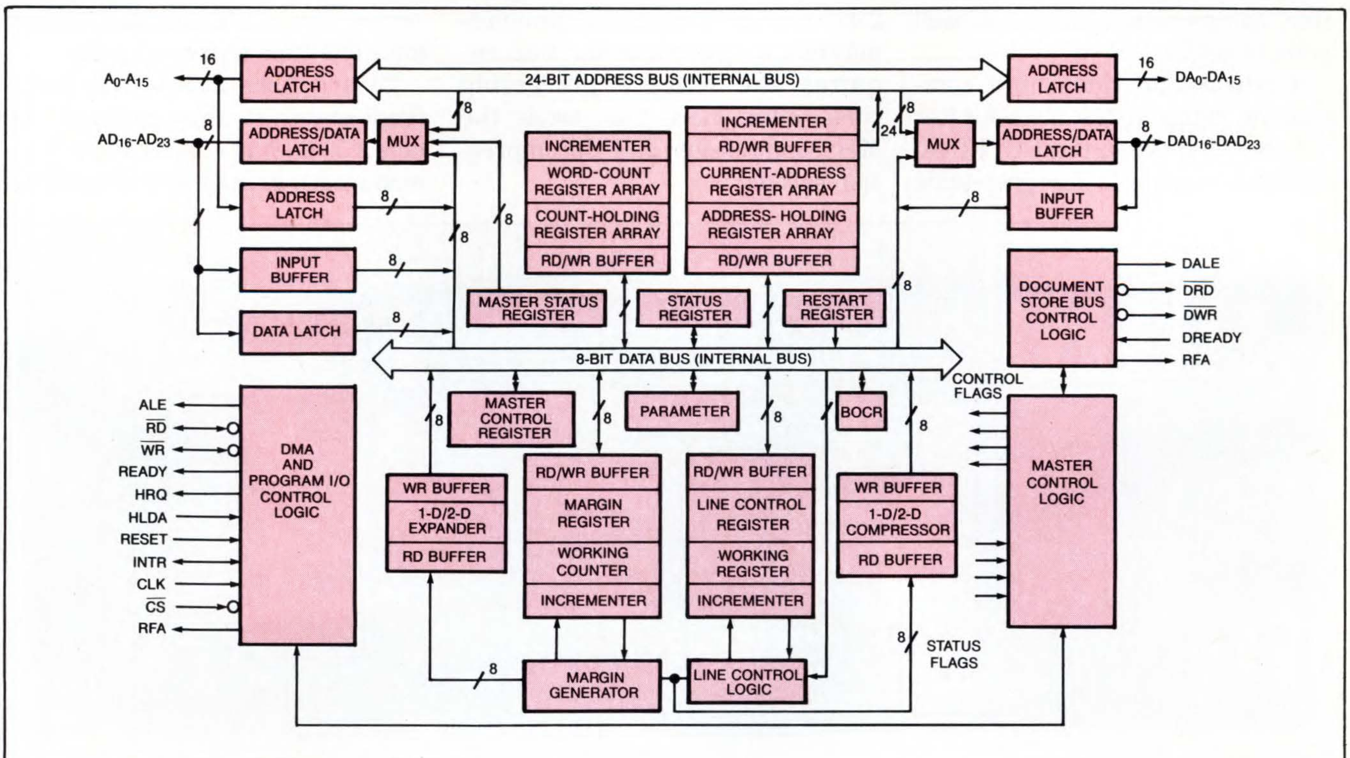
The Imageterminal from Image Data Corp uses one such proprietary scheme. This VT-100-compatible terminal compresses both text and gray-scale data by as much as a 10:1 ratio and transmits the compressed data over standard phone lines at 9600 bps. The terminal offers a 592×440-pixel resolution with 256 shades of gray in its high-fidelity mode and thus can combine sharp-edged text and gray-scale graphics in a single image.

A full-frame mode provides 128 shades of gray with a 296×220-pixel resolution; a document mode limits you to 16 gray levels at 592×440-pixel resolution. In addition, a fast-capture mode can grab about 50% of the image data. Telephone transmission of these compressed images typically takes from 10 to 40 sec, which translates into about 256k bytes of uncompressed image data sent every 7 sec. Prices for the Imageterminal range from $2495 to $3995.

Hitachi has addressed the problem of processing gray-scale data with the HD63084 image preprocessor chip. This 64-pin IC corrects shade distortions at high speeds, makes the picture elements 0.125 to 8 times denser than the original, and automatically assesses line thickness. It uses a dithering algorithm that intersperses black and white pixels to simulate shades of gray at rates as fast as 5 MHz. You can also select a mode that provides 16 levels of digitized gray coding. The chip also includes a shading data memory, a sensor interface, a sensor S/H, and a peak-value detector. It can process images as wide as 5280 picture elements. The chip interfaces with 8-bit computer-system buses and includes a built-in printer interface.

The Document Image Pre-Processor is a companion chip for the HD63085 Document Image Compression Expansion Processor. Compatible with the CCITT MH, MR, and Modified Modified Read (MMR) standards, the HD63085 can process a typical ISO A4-size document in approximately 0.85 sec. The chip accommodates paper in programmable widths that can include 65,535 picture elements. It also offers programmable registers for design flexibility. The HD63084 sells for $26.40 (10,000); the HD63085 costs $96.70 (10,000).

Negative compression poses a significant problem. If a scanned



Offering data-compression ratios ranging from 5:1 to 50:1, *Advanced Micro Devices' AM7971 Compression Expansion Processor integrates Group 3 and 4 CCITT compression functions on a single 68-pin chip. Its full-duplex mode lets you perform simultaneous compression and expansion operations.*

image has many black and white transitions, the size of the compressed image generated by MH and MR algorithms may actually exceed the size of the original image. This typically occurs when an image contains single-colored run lengths of five or fewer pixels. Such short run lengths result in increased pattern randomness.

Because the code for a short run of pixels could actually contain more bits than the number of pixels in the run, it is more efficient to simply store the ones and zeros that represent the actual pixels. Accordingly, your system must check the size of every compressed image and provide a method for deleting any negatively compressed image segments and storing the original segments instead.

Chips, boards, or software

Out of the range of boards, hardware, and software, you should be able to find a data-compression product that fits your specific application. Each type of product, however, has its disadvantages as well as its benefits.

Hardware provides high compression ratios at the fastest rates of speed. But when the CCITT establishes standards for gray-scale and color data compression, it may be difficult to upgrade data-compression ICs. Board-level solutions offer slightly greater flexibility for protocol modifications; on the other hand, they do tie you to a specific bus and require significantly more space. Software is by far the most flexible solution, but it offers the slowest compression speeds.

Software provides an option

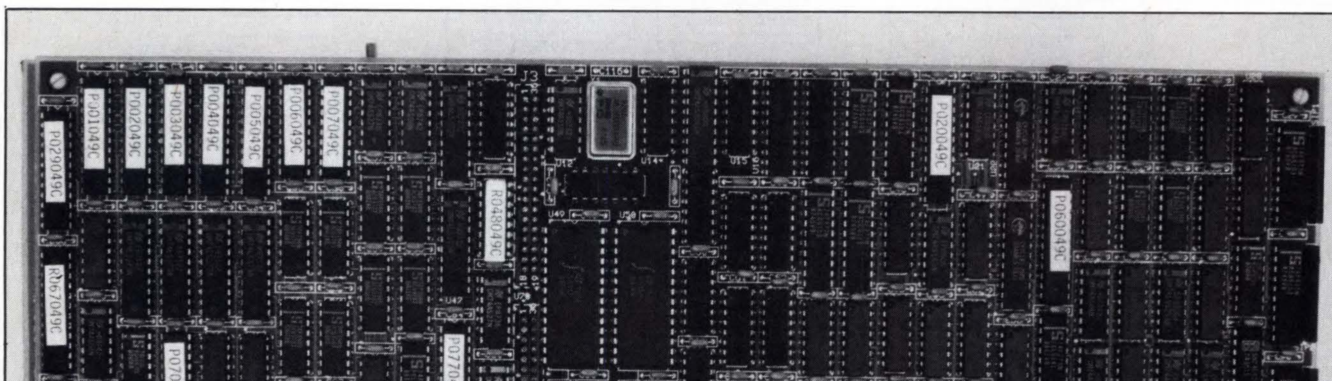
Texas Instruments (TI) offers a CCITT data-compression library as a complement to its 32-bit CMOS TMS34010 graphics processor. This software allows you to use the 34010 in applications that apply CCITT Group 3 and 4 standards. To use it, you need a PC-DOS or MS-DOS computer, TI's assembly-language tools package, and the 34010 C compiler.

The TI library lets a 34010 perform MH, MR, and MMR encoding. The Group 3 MR algorithm uses MH encoding for the initial scanned line in an image, whereas Group 4 MMR encodes the entire image in 2-D. Group 4 encoding provides maximum compression, but requires the longest processing time—often more than triple the MH compression and decompression speeds.

In comparison with dedicated data-compression ICs, the 34010 and its data-compression software do offer certain advantages. For instance, the 34010 is a fully programmable processor with a built-in graphics instruction set that includes Pixel Block Transfer (PixBlT) operations. Furthermore, it supports preclipping for windowing, plane masking, transparencies, and binary-to-color expansion operations.

The 34010 also includes a host interface, a 256-byte instruction cache, two register files, video RAM, and a CRT controller. These features make your circuit easily adaptable with software, should you encounter changes in specifications, standards, or applications. Furthermore, the 34010 is a bit-addressable μP, making it a particularly good IC for data compression because its on-chip barrel shifter eliminates software-based data shifting. The 34010 comes in 40-, 50-, and 60-MHz versions; prices start at $30 (100,000). TI licenses the CCITT Function Library for a one-time charge of $3000.

Tekand Labs makes continuous-feed scanners that process 500 dots × 50 lines per in. for large documents such as maps and blueprints.



For decompressing data at rates to 20M bps, *Brooktree's Bt70101 Image Decompression Processor comes packaged as an expansion board for the IBM PC/AT bus. The board offers nearly real-time data retrieval.*

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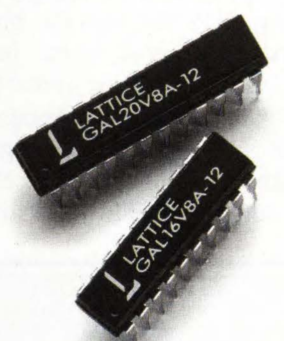

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It relies heavily on data compression to reduce images to a manageable size for storage and transmission. Tekand uses relative quad trees and 2-D compression techniques. Relative quad trees—also referred to as pointerless quadruple trees—require precompression preparation of the image by dividing the image into blocks of small pixel arrays called tiles. Each tree is a software algorithm that keeps a set of tiles in order. Typically, tiles are 512×512-pixel arrays.

Tekand's raster-image compression algorithms begin with the assumption that the entire image is white; the scanner compresses only black elements. Then it examines the first tile. If that tile is white, the system examines the next tile. When a tile is not completely white, the scanner sections it into four smaller tiles, which the system then checks for completely white arrays. This technique results in compression ratios ranging from 20:1 to 100:1.

Custom units with DEC DRV-1 interfaces run from $20,000 to $100,000 and offer impressive performance. An individual system can compress or decompress a typical 500M-pixel image in approximately 8 secs. The company also offers a 3-board PC/AT system with an encoder, scaler, and decoder; this system can convert one complete image in approximately 17 msec.

In dedication is strength

VLSI chips that are dedicated to CCITT data compression offer the best performance for most applications. Advanced Micro Device's Am7971 Compression Expansion Processor includes bit-boundary image processing and a full-duplex mode for simultaneous independent compression and expansion operations. Featuring a dual-bus architecture and on-chip DMA, the Am7971 can process documents as wide as 3.4 ft at 400 pixels/in.

The Am7971 can address as much as 16M bytes of memory on both the system bus and the document bus. Separate and independently programmable compression and expansion processors enhance speed. The chip also provides 46 programmable registers for address pointers, parameters, and status information. On-chip error detection checks for negative compression, illegal codes, incorrect line lengths, and transmission errors. Non-CCITT options include vertical image-resolution conversion and granularity control.

Three versions are available: a 8-MHz LCC version of the Am7971 for $80, a 5-MHz PLCC model for $55, or a 3-MHz PLCC version for $23 (100). If you want to add text compression and expansion to an IBM PC or compatible, the company will sell you an evaluation board for $1150.

Save time and space

One set of products that saves you time as well as space is Hewlett-Packard's family of 1/2-in. reel-to-reel streaming-tape drives—the first such drives to incorporate electronic data compression. By compressing backup-data to anywhere between a half and one-fifth of its original size, the system reduces the need for time-consuming reel changes and the resulting drive downtime needed for tape loading, rewinding, and handling. Furthermore, because the unit compresses the data before sending it to the unit's 512k-byte buffer, the data buffer becomes effectively larger, and the data-transfer rates increase to 1.6M bps.

HP uses a proprietary data-compression algorithm called Option

For more information . . .

For more information on the data-compression products described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Hewlett-Packard
700 71st Ave
Greeley, CO 80634
(303) 350-4209
Circle No 727

Hitachi Ltd
2210 O'Toole Ave
San Jose, CA 95131
(408) 435-8300
Circle No 728

Image Data Corp
11550 Interstate 10W
Suite 200
San Antonio, TX 78230
(512) 641-8340
Circle No 729

Tekand Labs Inc
9119 S Gessner
Suite 101
Houston, TX 77074
(713) 981-4680
Circle No 730

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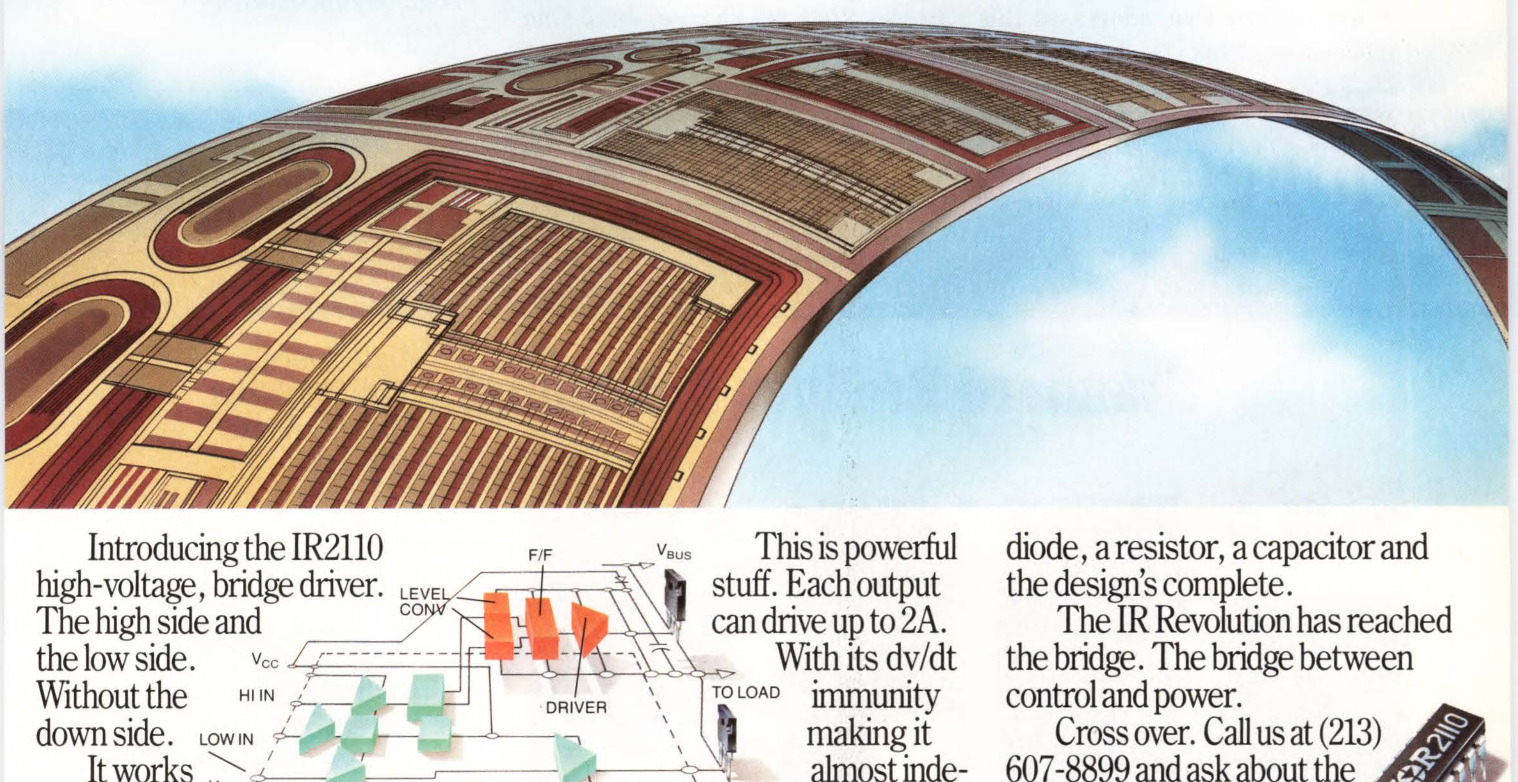

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400 that is implemented in VLSI hardware. Option 400 recognizes every repeated data pattern, regardless of complexity, and replaces it with special codes. The entire compression process occurs in the tape drive and is transparent to the host. Read/write operations take place at the rate of 125 ips for data densities of 1600 and 6250 cpi. The HP 7980XC tape drive sells for $32,200.

Decompression finds a niche

Data decompression may actually represent a bigger market than that provided by data compression. Applications like high-speed data retrieval from optical-disk archives create a need for real-time data decompression to allow researchers to flip through pages of electronic documents as quickly as they could flip through a book.

One product that addresses this processing task is Brooktree's Bt70101 Image Decompression Processor. Packaged as an expansion board for the IBM PC/AT bus, the Bt70101 decompresses data at a 20M-bps decompression rate. The unit conforms to CCITT recommendations T.4 and T.6 for Group 3 and Group 4 facsimile image decoding, and is thus suitable for use in high-speed fax servers as well as image-database retrieval systems. An evaluation kit containing a Bt70101 decompressor board, a user's guide, and software providing demonstrations, diagnostics, and samples of compressed image files, costs $1995.

Jeff Teza, Director of Brooktree's Subsystems Group, estimates that the demand for decompression is ten times that for data compression. For example, a large LAN may have only one scan server but several other stations that allow users to view (but not change) data. One scan server suffices for all document compression and storage, but every viewing station on the LAN must have decompression capability so that all users can have access to data. In response to the suggestion that such a "look but don't touch" environment is undesirable, Mr. Teza noted that LAN users, like library users, frequently need just to refer to data, not to change it. EDN

References

1. Fuchs, Peter M, "Compressing data conserves memory in bit-mapped displays," *EDN*, October 30, 1986, pg 173.

2. Storer, James A, *Data Compression and Methods Theory*, Computer Science Press, Rockville, MD, 1988.

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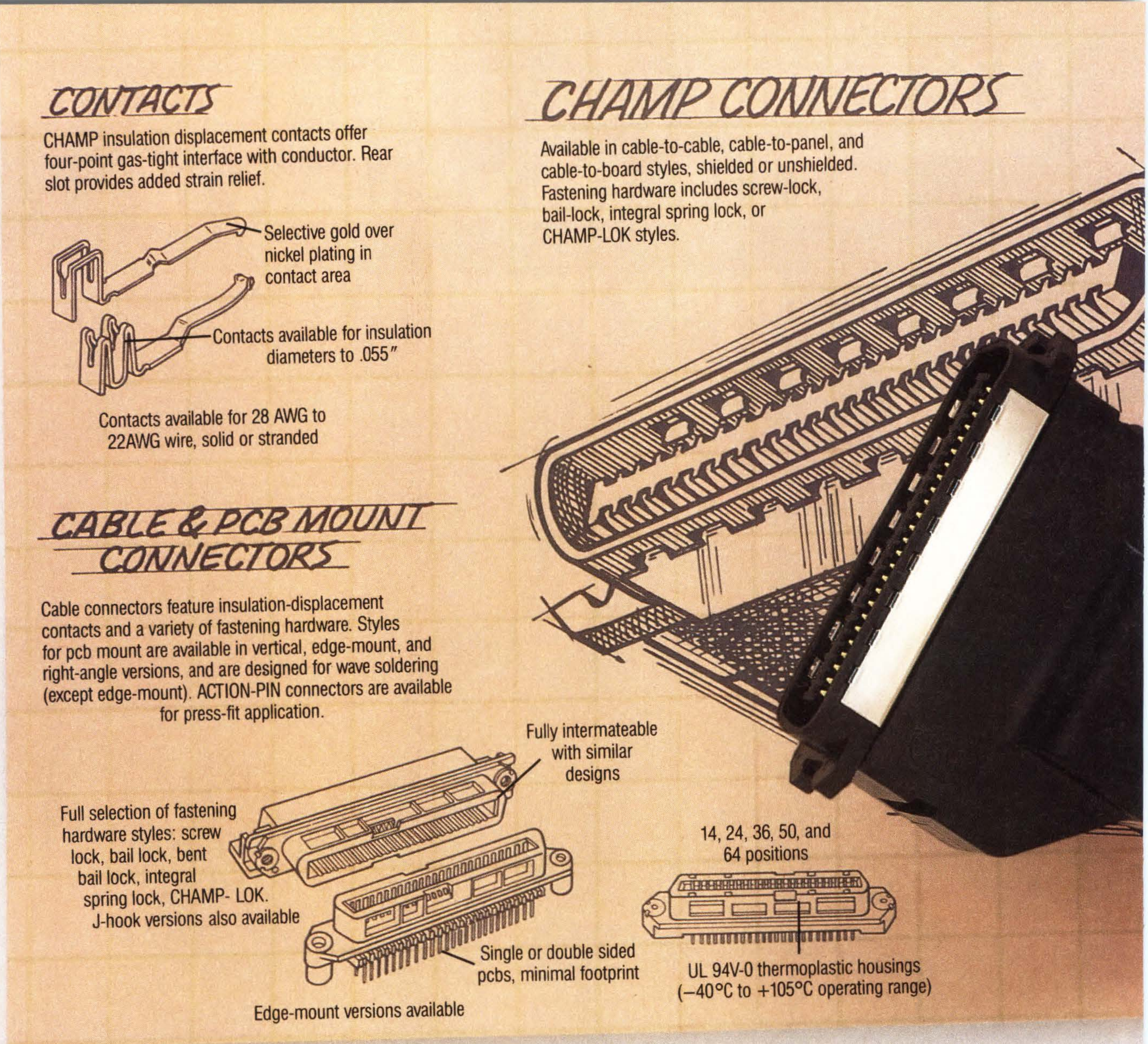

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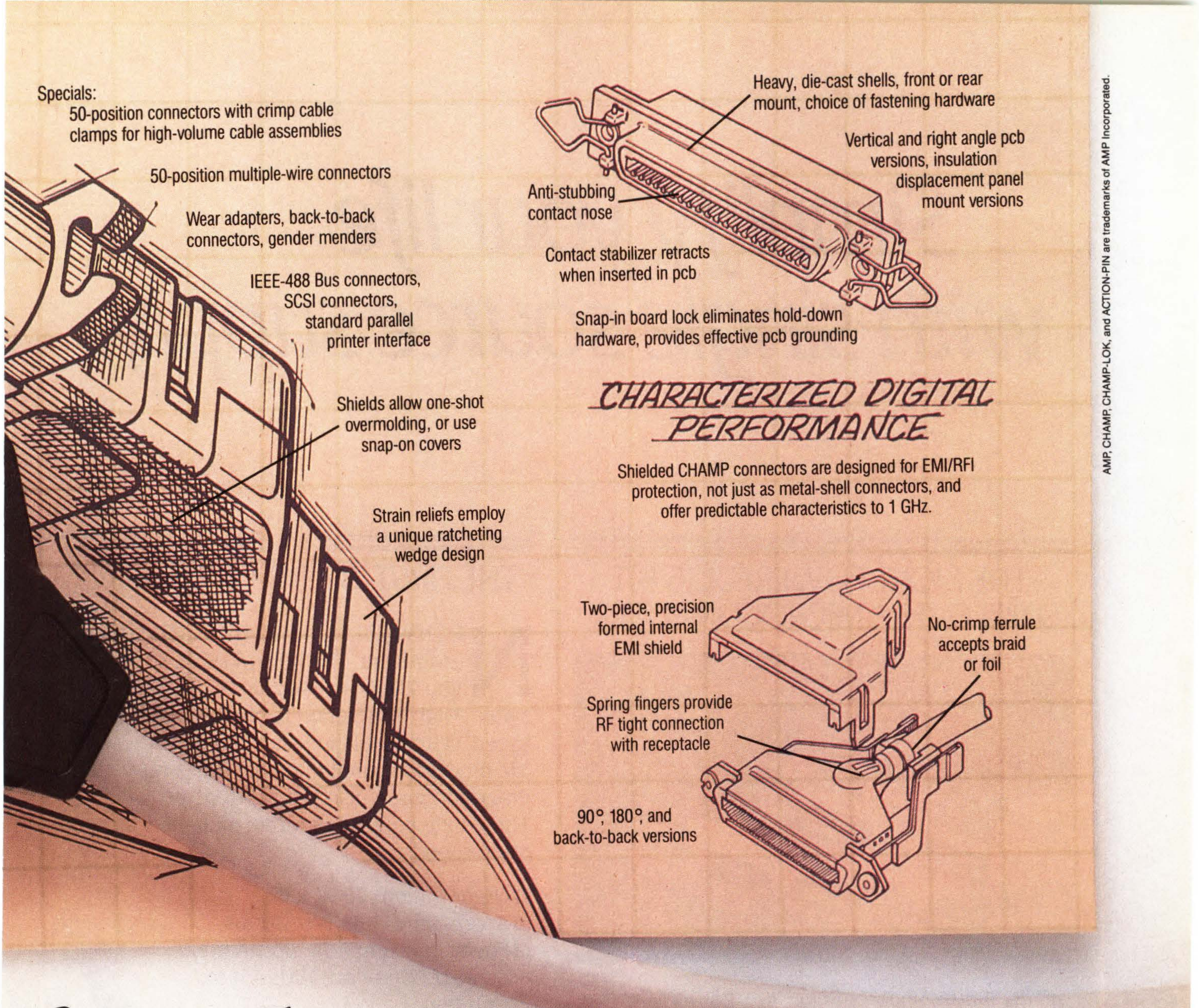

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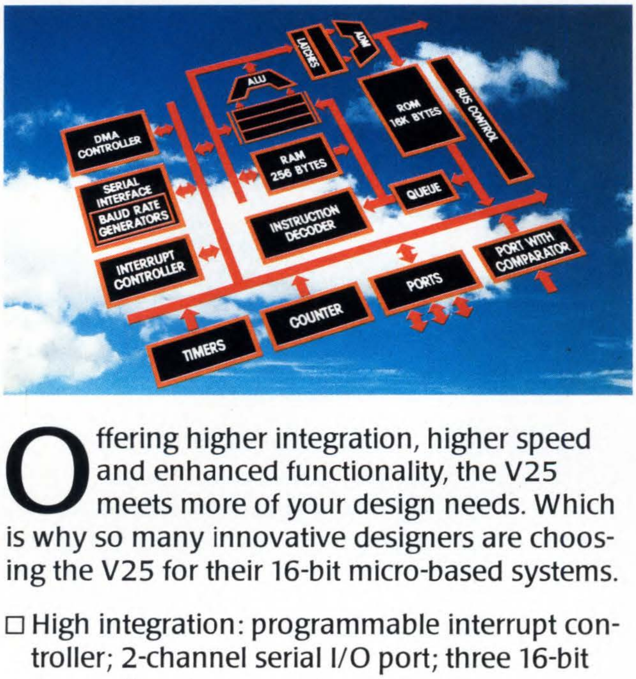

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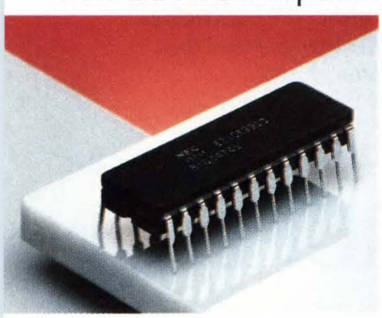

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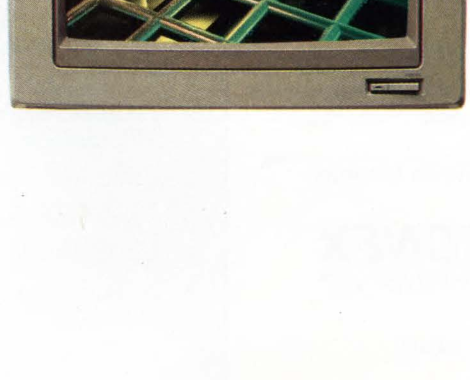

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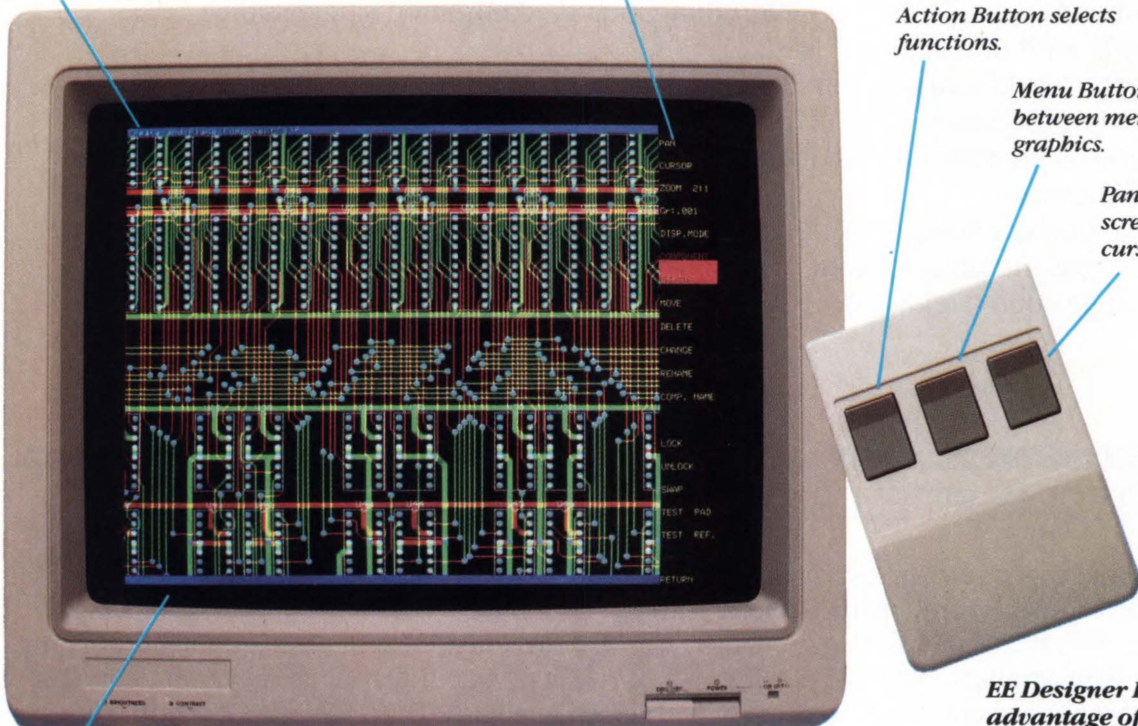

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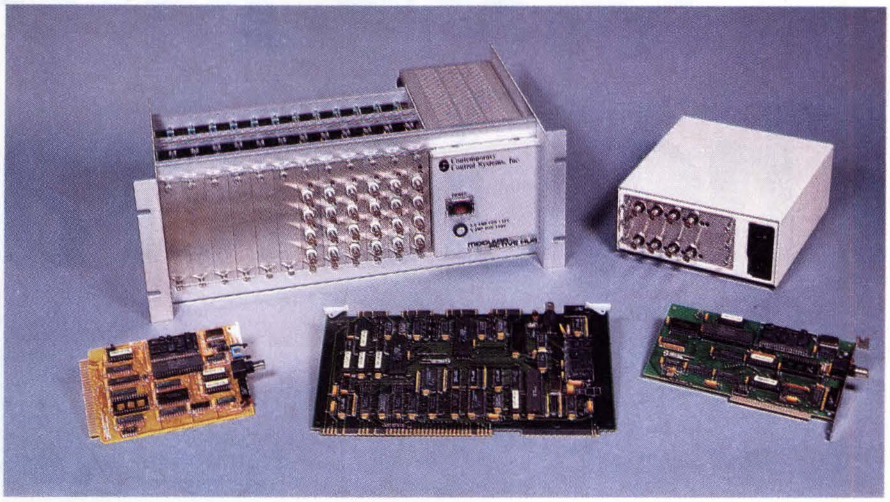
CIRCLE NO 141

The deterministic character of Arcnet proves ideal for the factory floor

Doug Conner, *Regional Editor*

Today, with approximately 1,000,000 Arcnet nodes in service, Arcnet is a significant networking standard, yet compared with Ethernet it remains relatively unknown. You can expect to hear more and more about Arcnet networks, however, as people increasingly realize what benefits Arcnet has to offer. These benefits are especially evident in factory-floor applications.



***Arcnet-interface cards support** a wide variety of buses. These Contemporary Control Systems' cards support Multibus I, the PC bus, and the STD bus, respectively. The other two products are modular active hubs.*

CSMA/CD vs token passing

The primary difference between Ethernet and Arcnet is that Ethernet uses a CSMA/CD (carrier-sense multiple-access/collision-detection) networking protocol, and Arcnet uses a token-passing protocol. These two different protocols force requirements on the networking systems that make them very different.

Ethernet allows any node to instantly begin sending a message to another node as long as there is no other traffic on the network. Even when there's light network traffic, an Ethernet node can still quickly gain access to the network and send messages to another node. Ethernet's 10M-bps data-transfer rate allows long messages to be transmitted rapidly, provided that the computer interfaces can also maintain the 10M-bps rate.

Problems with a CSMA/CD protocol arise when network traffic increases to the point where collisions become common and network throughput is drastically degraded due to network contention problems. When such a situation occurs, the data transferred per unit time can actually drop substantially.

Arcnet's token-passing protocol is essentially a polling-access communication method. A token passes sequentially to each node; the node with the token can send a packet of data to another node, and it must then pass the token on. When there is light traffic on the network, the token travels to each node on the network (255 is the maximum number of nodes that an Arcnet network can support), even if only one node has a message to send.

Although Arcnet's token-passing protocol takes time away from message transmissions, an Arcnet network doesn't suffer from collisions. Alleviating the chance of collisions keeps data transmissions from becoming bogged down when network traffic gets heavy. Moreover, because an Arcnet network doesn't have to detect collisions, its hardware is simpler than Ethernet.

As network traffic increases, Arcnet's token-passing overhead becomes a smaller percentage of network traffic. An Arcnet network with heavy traffic spends less than 2% of its time token passing. Despite Arcnet's data-transfer rate of 2.5M bps, the rate of successfully transmitted data can exceed that of Ethernet when network traffic is heavy.

Arcnet shows a linear increase in the amount of time required to send a message from one node to another until network traffic reaches the point where every node is sending the maximum 508-byte packet each time it receives the token. The amount of time that Ethernet requires to send a message becomes nonlinear at the point when collisions begin to consume significant amounts of time.

Worst-case response is vital

Factory-floor-automation applications are often more concerned with the worst-case response time than with the data-transmission rate. Because Arcnet allows you to calculate the worst-case response time of the network, you can monitor and control critical machines and processes within guaranteed times.

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SG1529	SG3529
Current Mode	
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SG1842	SG3842
SG1843	SG3843
SG1844	SG3844
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Message communications with Ethernet are always statistical; you don't have any way of knowing the absolute maximum time required to send a message.

The deterministic character of Arcnet is not the only difference between the two networks. Ethernet is incompatible with fiber-optic transmission media, yet fiber-optic media is common in Arcnet-network connections as far as 4000 ft apart. Fiber-optic communications offers the ultimate in immunity from electronic noise that may be present on the factory floor. Fiber-optic media is also safe to use in explosive environments.

Low cost is another plus

Arcnet is also typically a lower-cost alternative than Ethernet. Cabling costs can amount to half the cost of a network, and this is especially true in factory-floor applications where cabling runs can be long. Arcnet networks normally use RG62/U coaxial cable, which costs around $0.30 per ft—about a third the cost of standard Ethernet cabling. Although Arcnet can also use twisted-pair cabling, twisted-pair's susceptibility to noise usually prevents its use in factory-floor environments. (Don't forget, when considering Arcnet or any other network, to add the cost of cable *installation* to your estimate of overall cost.)

The lower price of an Arcnet network is also a reflection of the simplicity of its hardware. **Table 1** lists some representative Arcnet-interface products and prices.

Arcnet networks are easy to bring on line, and you can even add or remove nodes while the network is operating. The basic requirement for operation is that every node must have a unique address of 1 to 255. The network automatically uses address 0 for broadcasting messages to all nodes. As long as you have all the nodes set to their unique addresses, the network will automatically configure itself upon powering up. An Arcnet network configures itself within a maximum of 61 msec.

Connecting a new node to a port or powering up a node interrupts the network and precipitates a reconfiguration. If you remove a node or if a node does not respond within a certain time limit, the network will also reconfigure itself; failure of a single node typically brings down just that node, not the entire network.

Factory-floor network communications are often dominated by short messages—process-monitoring data, for instance, which consists of several bytes and is sent at short, regular intervals. Arcnet

TABLE 1—REPRESENTATIVE ARCNET-INTERFACE VENDORS AND PRODUCTS

VENDOR/PRODUCT	BUS INTERFACE	ACTIVE-HUB PORTS	DIAGNOSTIC LEDs	PRICE	COMMENTS
ACTINET SYSTEMS ACTINET II	MACINTOSH II (NUBUS)		✓	$695	NO HARDWARE SWITCHES
COMENDEC V-ARC03 3U	VME 3U			$870	
Q-ARC-01	Q		✓	$1925	SUPPORTS 16-, 18-, AND 22-BIT BUSES INTELLIGENT SLAVE OPERATION
CONTEMPORARY CONTROL SYSTEMS 771-501		4	✓	$275	STD BUS-BASED ACTIVE HUB
M871	MULTIBUS I		✓	$995	INCLUDES 4 SERIAL PORTS
DATAPOINT 7061	RS-232C		✓	$295	DATA RATES TO 38.4k BPS
EARTH COMPUTER TECHNOLOGIES EARTHNET-QUAD	IBM PC	4	✓	$295	COMBINED ACTIVE HUB AND BUS INTERFACE
NOVELL RX-NET	IBM PC			$350	INCLUDES 20 FT OF CABLE
PERFORMANCE TECHNOLOGY POWER RIM II	IBM PC/AT		✓	$795	
PURE DATA PDIμC508	MICRO CHANNEL		✓	$795	NO HARDWARE SWITCHES
STANDARD MICROSYSTEMS PC110	IBM PC			$295	
THOMAS CONRAD TC 6045	IBM PC/AT		✓	$495	20-MHz OPERATION
ZIATECH ZT 8890	STD		✓	$495	

handles these messages efficiently thanks to its variable-length packets that contain 1 to 508 bytes of data. Arcnet can also quickly transfer larger messages, such as downloading programs over the network to reprogram machines. (Ethernet does have a larger packet size than Arcnet, though.)

Datapoint originally developed Arcnet in 1977 as a proprietary network, and even though an IEEE standard hasn't yet formalized it, Arcnet has become a de facto standard. Datapoint also developed the Arcnet control chip set at the same time that it developed the network. Currently, Standard Microsystems Corp and NCR Microelectronics (Fort Collins, CO, (303) 226-9500) are producers of the controller chips. The fact that all Arcnet-interface vendors use two functionally equivalent chip sets has provided excellent compatibility. Today's Arcnet boards operate with boards that were built 11 years ago.

A number of vendors provide Arcnet interfaces for a numerous variety of buses. **Table 2** shows some of the vendors and the buses that they support. You can mix bus interfaces and hubs from multiple vendors on an Arcnet network without any problem.

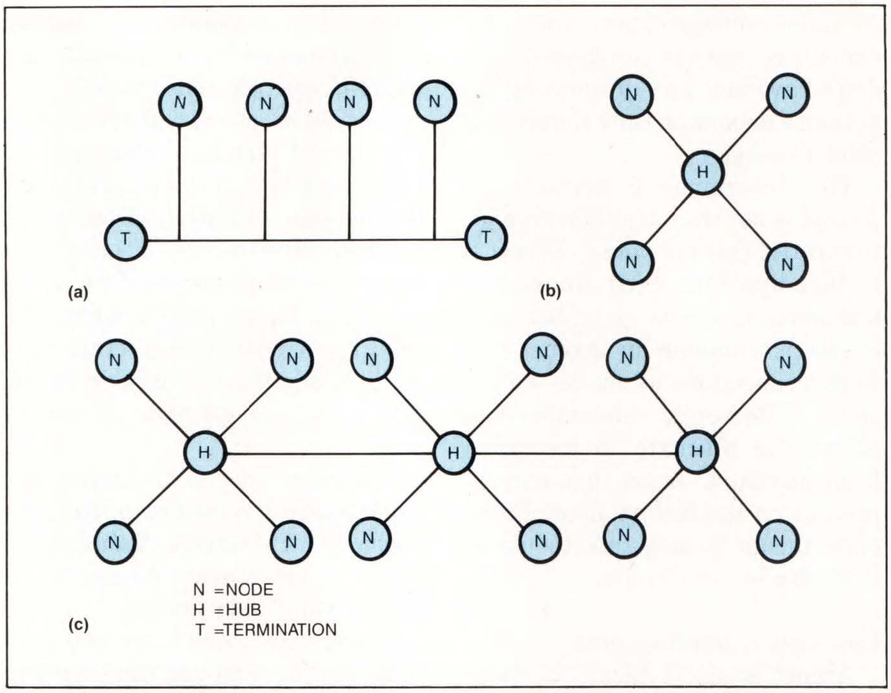

*Fig 1—**You have a choice** of three typical Arcnet network topologies: bus or multidrop **(a)**, star **(b)**, and distributed star **(c)**. Combinations of the three are also possible.*

When setting up an Arcnet network, you can use either a bus or a star network topology or combinations of the two (**Fig 1**). The typical way to expand a star network is to add extra multiple-port active hubs to form distributed stars. The active hub provides bidirectional signal regeneration between ports. You can string multiple hubs together, provided that the separation between any two nodes does not exceed about four miles. The 31-μsec maximum allowable propagation time between nodes imposes the 4-mile requirement.

Using the standard RG62/U coaxial cable in a distributed-star configuration allows cabling runs of 2000 ft between hub-hub or hub-node connections. In a distributed-star network topology, a cable failure will bring down only the attached node in that particular hub-node connection. A hub-hub connection failure will cause the system to reconfigure itself into two separate networks.

You can often troubleshoot problems on a star or a distributed-star network by unplugging nodes one at a time until the problem disappears. Unused active-hub ports

TABLE 2—REPRESENTATIVE VENDOR SUPPORT OF STANDARD BUSES

VENDOR	APPLE MACINTOSH	APPLE MACINTOSH II (NUBUS)	MICROCHANNEL BUS (IBM PS/2)	MULTIBUS I	PC BUS, 8-BIT DATA BUS	PC/AT BUS, 16-BIT DATA BUS	Q BUS	UNIBUS	VME BUS	STD BUS	RS-232C
ACTINET	✓	✓				✓					
COMENDEC			✓				✓	✓	✓		
CONTEMPORARY CONTROL SYSTEMS				✓	✓					✓	
DATAPOINT			✓			✓					✓
EARTH COMPUTER TECHNOLOGIES			✓		✓						
NOVELL					✓						
PERFORMANCE TECHNOLOGY						✓					
PURE DATA			✓		✓						
STANDARD MICROSYSTEMS			✓		✓	✓			✓		
THOMAS CONRAD			✓		✓	✓					
ZIATECH					✓					✓	

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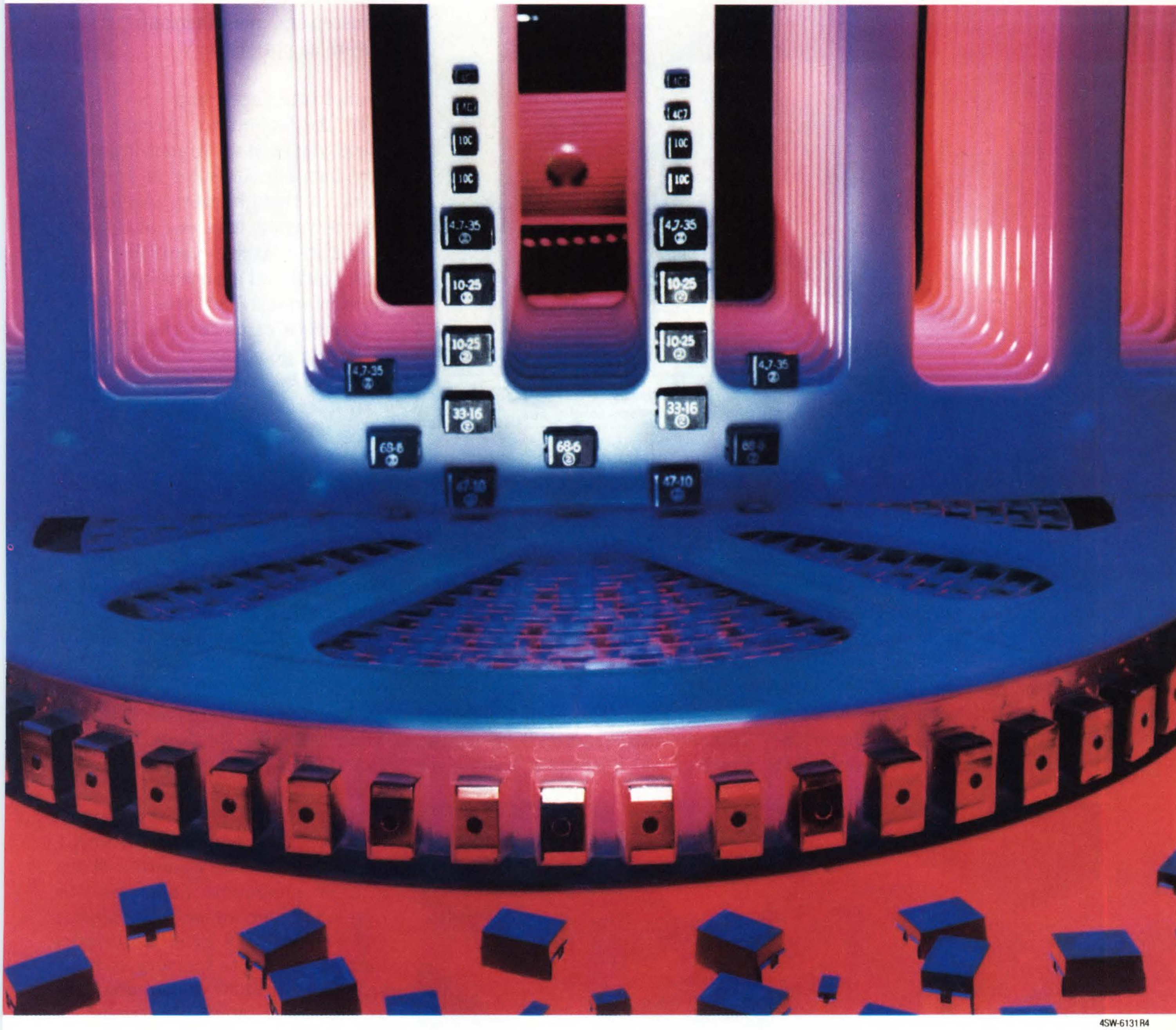

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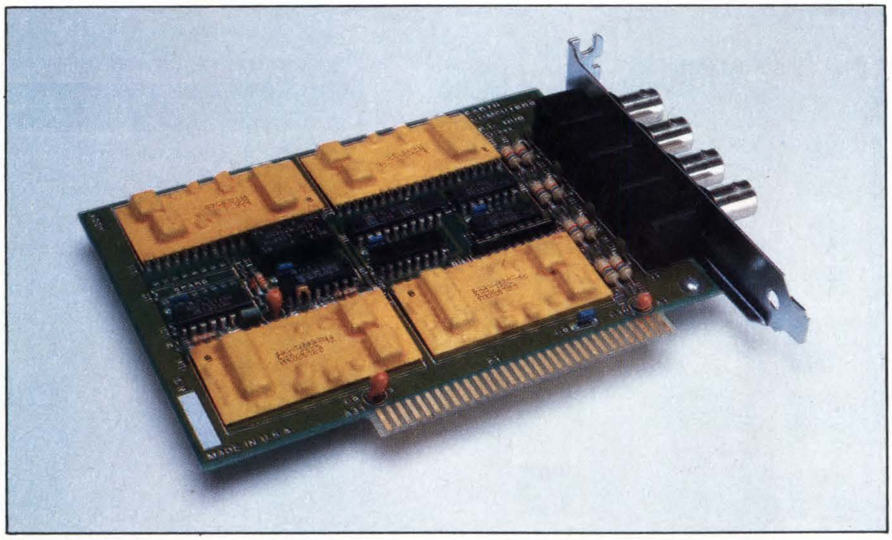


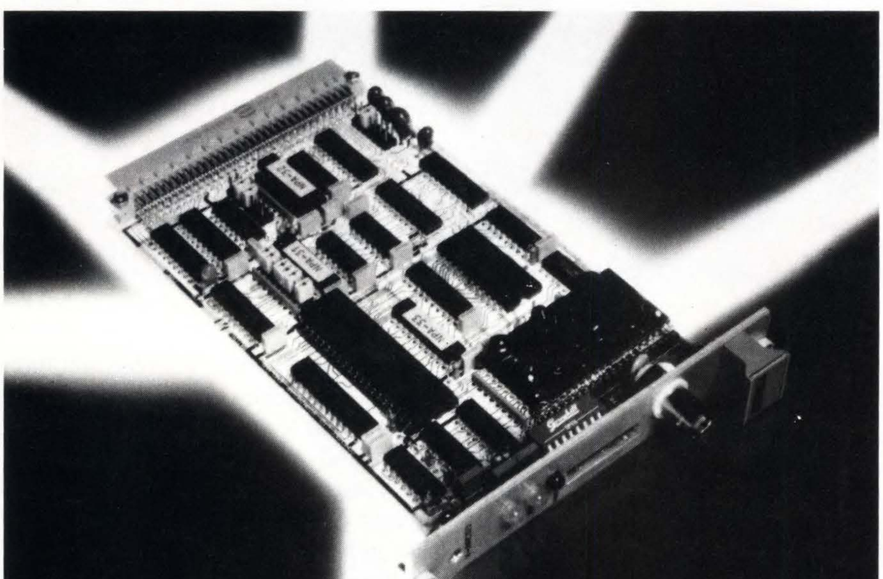
***With this 4-port active hub** from Earth Computer Technologies, you can assemble star and distributed-star network topologies. The hub draws its power from the PC bus.*

need not be terminated.

Bus or multidrop topologies, popular for networking in offices, are useful but add a few more restrictions. The maximum bus length must not exceed 1000 ft for two nodes. As you increase the number of nodes on a bus to the maximum 19, you must reduce the bus length to 200 ft. Also, in a bus configuration, any cable or node problems on the bus will bring down the entire bus. In addition, you'll find that troubleshooting is more difficult with a bus topology.

Transceivers: high or low

Low-impedance transceiver modules are standard for star or distributed-star networks using RG62/U coaxial cable. If you want to use a bus or multidrop network topology, you'll need high-impedance transceivers. If you'll be using fiber-optic communications, you'll of course need to use fiber-optic transceiver modules. Most Arcnet-interface vendors offer high-impedance transceivers and fiber-optic transceivers as options.



***A compact 3U VME bus Arcnet-interface card** available from Comendec has diagnostic LEDs to aid in troubleshooting. You can view and set the node address through the mounting bracket.*

Arcnet interfaces vary

To implement an Arcnet network, you need an Arcnet-interface card for each computer on the network. Although every Arcnet-interface vendor uses one of the two compatible Arcnet controller chip sets, you'll find a surprising variety of interface-card features.

Interface cards for the IBM PC bus are a good case in point. Both 8- and 16-bit data-bus (IBM PC/AT bus) interfaces are available. Both types of cards support the same data rate over Arcnet, but the 16-bit bus can load and unload the Arcnet interface's data-packet buffer more quickly. The 16-bit bus reduces the likelihood of the buffer being full and unable to receive data from another node, which would delay the transfer. When transmitting, the 16-bit bus minimizes the possibility of the data-packet buffer not having a complete packet loaded when the node receives the token and thereby missing a chance to send data.

Different PC bus-based Arcnet interfaces require different amounts of memory-address space in their computers. Some use 64k bytes of memory-address space, and some use 16k bytes. Interfaces that use 64k-byte memory-address space do not allow you to use both an EGA (enhanced graphics adapter) and the LIM EMS (Lotus-Intel-Microsoft extended-memory scheme) at the same time. Cards using 16k bytes of memory space do accommodate both EGA and LIM EMS simultaneously.

PC bus-based interface cards also support varying clock rates. On some high-clock-rate personal computers, you need to make sure that the interface board is compatible with your system's speed. Some Arcnet interfaces for PC bus systems support clock rates of 20 MHz.

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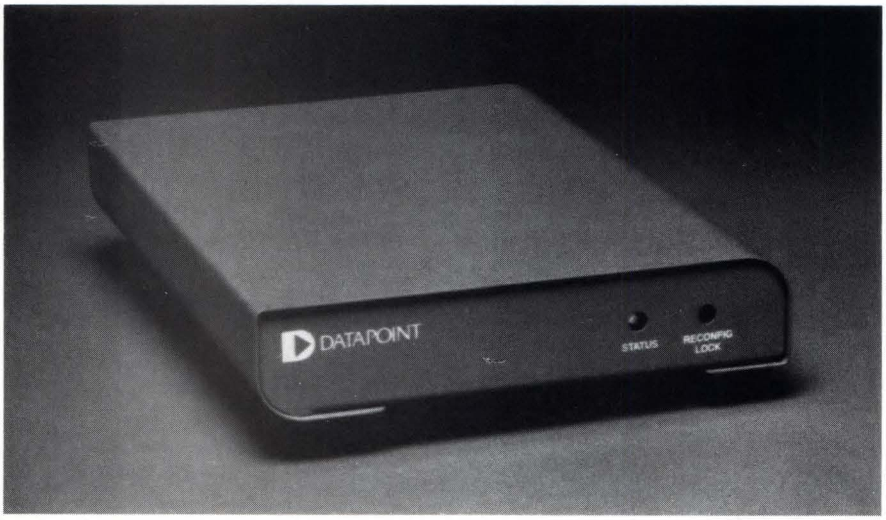
Regardless of whether you're interested in an interface card for the PC bus or one of the many other existing buses, you should find out by what means the node address is specified. Typically, Arcnet cards come with DIP switches that allow you to set the address. Preferably, you want to be able to view and set the address through an access hole in the card's mounting bracket so you don't have to remove the computer's cover. Some cards don't have any hardware switches; in this type of interface card, the node address is set by the software when the system is booted up.



Point-of-use adapters, *such as this one from Datapoint, allow an Arcnet network to interface directly to RS-232C and parallel printer ports.*

These STD bus Arcnet-interface cards and hubs *from Ziatech allow you to network STD bus computers.*

The cards' packet buffers are also another consideration of which you should be aware. Most Arcnet-interface cards have a 2k-byte packet buffer, which allows storage of four 508-byte packets. Some cards have even larger packet buffers, which may increase performance in cases where the host computer does not respond quickly to network activity.

Most Arcnet-interface cards are available with diagnostic LEDs that can simplify the troubleshooting of network problems. These LEDs typically tell you when the Arcnet cable has continuity and when there is activity on the network or in the packet buffer.

Active hubs may be required

In addition to the requisite interface card, if you want your Arcnet network to be configured in a star topology you'll also need one or more active hubs. These generally fall into two categories, bus based and stand alone.

Bus-based active hubs use a slot and receive power from your computer system. The bus-based active hub does not, however, communicate over the computer's data bus, nor does it provide an Arcnet interface to the host computer. An exception is the Earthnet-Quad from Earth Computer Technologies; it does provide a bus interface and a 4-port active hub (**Table 1**).

Stand-alone active hubs are, as the name implies, housed in their own enclosure. Some vendors offer modular active hubs—both stand alone and bus based—that are expandable as your needs grow.

There is one important consideration to keep in mind when you select an active hub. The power to the hub must be on whenever you want to

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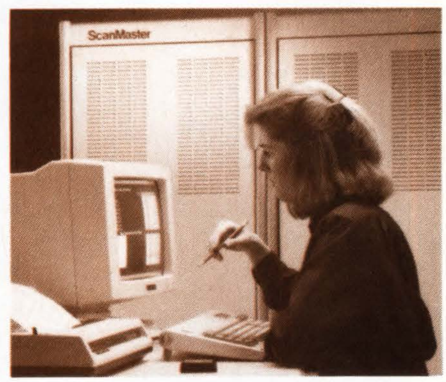

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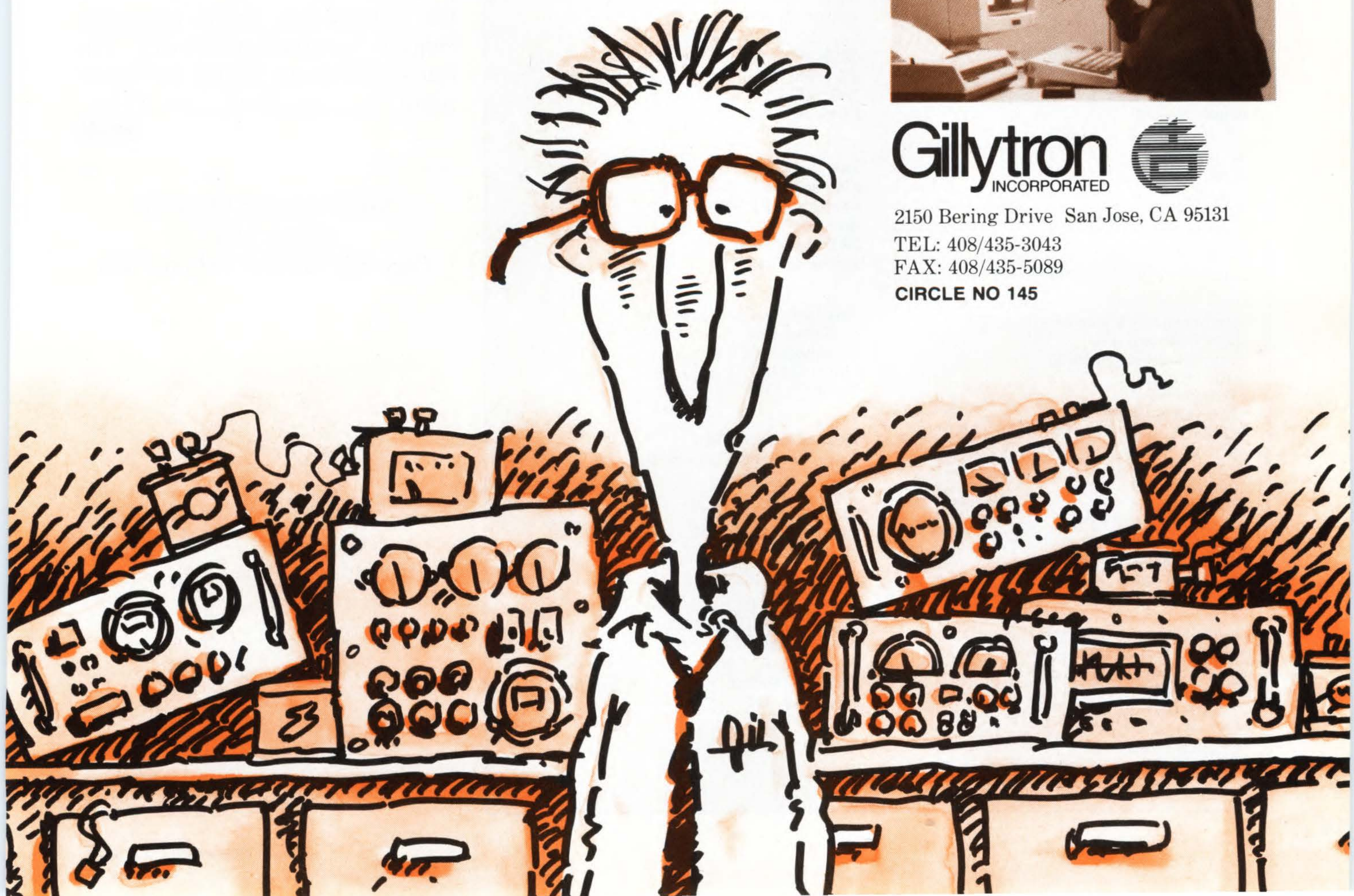

communicate with nodes connected to that particular hub. You wouldn't want an active hub in a computer that someone might power down when they weren't using it.

If you want to add more nodes to a network, you can use passive hubs instead of active hubs, provided that the distances involved are not more than 100 to 200 ft. Passive hubs split the signal and use series resistors to maintain the 93Ω loading, and the signal attenuation reduces transmission distances and impairs system immunity to noise. In addition, unlike an active hub, all unused ports on a passive hub must be terminated. It's probably best to avoid passive hubs when you desire a highly reliable system.

Arcnet's future

Committees within the Arcnet Trade Association (Arlington Heights, IL, (312) 369-2355) are working on some future enhancements to Arcnet. In an effort to keep Arcnet competitive in the future, a committee is working on a backward-compatible hardware upgrade that will increase data rates to 20M bps. The committee is also looking into increasing the maximum packet size to 2k or 4k bytes, as well as increasing the maximum number of nodes on a network to 1000 or 2000. At present, if you need more than 255 network nodes, you must link multiple networks with software bridges.

Factory situations that may eventually require MAP (manufacturing automation protocol) will still be able to consider Arcnet as a subnetwork within the overall MAP environment. You can install an economical Arcnet network now and then link it to MAP when the need arises.

In addition to these developments, advances in electronics have progressed to the point where NCR has reduced the Arcnet controller chip set to a standard-cell core. You can expect to see Arcnet interfaces using these cores in the near future.

EDN

For more information . . .

For more information on the Arcnet products described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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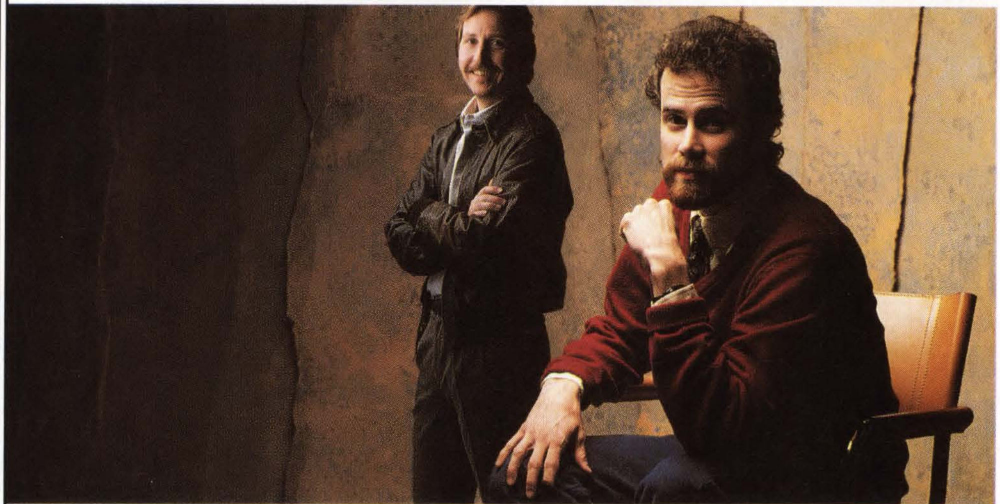

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PG 12806

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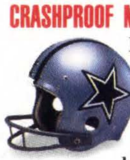
CRASHPROOF MEMORY PROTECTION



Dallas Semiconductor's unique circuitry safeguards the contents of all memory and registers during power fluctuations. Processing is automatically suspended when voltage drops out of operating range and resumes where it left off when power is restored, insuring that data is never lost while waiting for power. Even if it's 10 years later.

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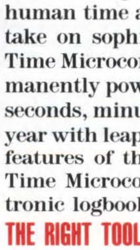
Time-stamping and dating events with human time allows our microcontrollers to take on sophisticated tasks. The DS5000T Time Microcontroller features a built-in, permanently powered clock/calendar that counts seconds, minutes, hours, days, day of week, date, month and year with leap year compensation. In addition to all the basic features of the DS5000 Soft Microcontroller, the DS5000T Time Microcontroller schedules events and keeps an electronic logbook of all activities.

THE RIGHT TOOLS FOR DEVELOPMENT



The DS5000 Soft Microcontroller and DS5000T Time Microcontroller are instruction set and pin compatible with the industry standard 8051 microcontroller. Existing software runs with no modification. The large memory facilitates the use of high-level language compilers for development of application software. The DS5000TK Evaluation Kit allows immediate evaluation of the DS5000 series in an existing application. In-system serial downloading of software to the microcontroller is supported with an IBM personal computer or compatible. Dallas Semiconductor also offers the DS5000DK Development Kit to provide symbolic real-time emulation for the DS5000 series with an IBM PC.

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Quality Completes Our Innovation

Buscon/88 East will stress emerging trends in computer-bus technology

Joan Morrow,
Assistant Managing Editor

For those of you who seek information on just about any aspect of computer-bus technology, Buscon/88 East is the show to attend. The conference, which will be held in the Jacob K Javits Convention Center in New York City on October 3 to the 6, will tempt you with more than 30 user-oriented seminars and sessions in four separate tracks. You have the option of remaining in one track or selecting just the right mix of sessions and seminars that suits your particular expertise or interest. Furthermore, over 200 hardware and software exhibitors will display their wares during the 4-day show.

Track 1, entitled "Board-Level Design," will feature six sessions and two half-day seminars—one on 32-bit buses and their applications and the other on the NuBus. If you're new to the field, you can get the basics in the session entitled "Introduction to Buses." It will go over the terminology and elementary concepts used in bus- and board-level design. If you're more experienced, you might want to take in other sessions in the track: 32-bit design using Multibus I, new issues in Multibus II and the VME bus, understanding the VXI bus, and recent developments in IEEE 896.

Two more half-day seminars will lead off the "System-Level Design" Track 2. "Backplane Bus Design" will provide a theoretical and practical foundation for designers and users of such systems. "Introduction to Intelligent Peripheral Buses" will cover SCSI, ESDI, IPI, and SMD buses and their applications. Sessions scheduled in track 2 include considerations in system packaging, methods for interfacing

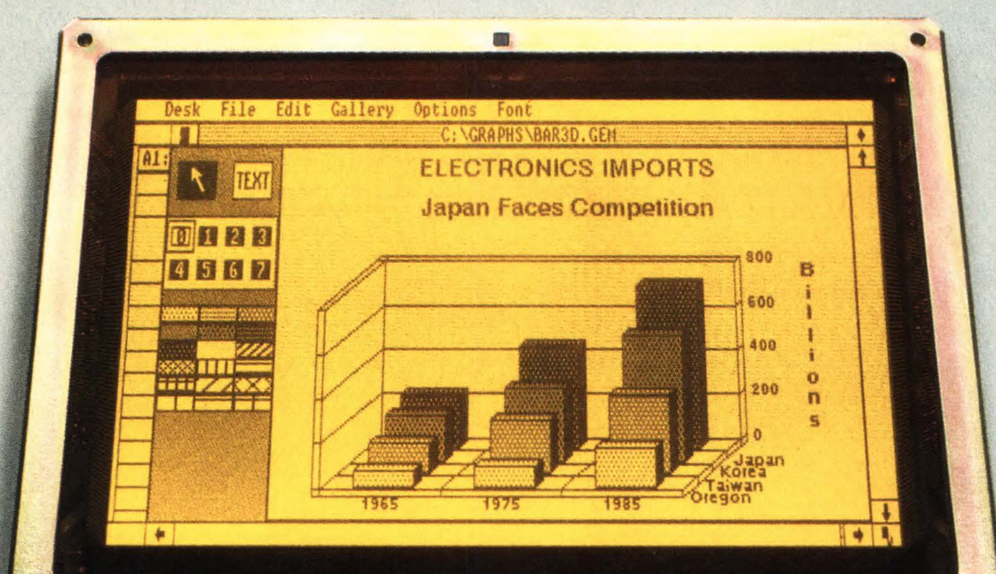
BUSCON/88 EAST PROGRAM SCHEDULE

		TRACK 1 BOARD-LEVEL DESIGN	TRACK 2 SYSTEM-LEVEL DESIGN	TRACK 3 APPLICATION DEVELOPMENT	TRACK 4 ELECTIVE
MONDAY, OCTOBER 3	8 AM-5 PM	SEMINAR 10 SELECTION AND TRAINING OF BOARD-LEVEL MANUFACTURERS' REPRESENTATIVES			
MONDAY, OCTOBER 3	8:00 AM-12:00 PM	SEMINAR 11 32-BIT BUSES AND APPLICATIONS	SEMINAR 12 BACKPLANE BUS DESIGN	SEMINAR 13 REAL-TIME SYSTEMS	
MONDAY, OCTOBER 3	1:00 PM-5:00 PM	SEMINAR 21 NuBUS WORKSHOP	SEMINAR 22 INTELLIGENT PERIPHERAL BUSES	SEMINAR 23 COMMUNICATIONS TECHNOLOGY	SEMINAR 24 ASIC TUTORIAL
TUESDAY OCTOBER 4	9:00 AM-11:00 AM	SESSION 101 INTRODUCTION TO BUSES	SESSION 102 CONSIDERATIONS IN SYSTEM PACKAGING	SESSION 103 REAL-TIME SOFTWARE: PART 1	SESSION 104 QUO VADIS? (FREE)
TUESDAY OCTOBER 4	2:00 PM-4:00 PM	SESSION 201 32-BIT DESIGNS WITH MULTIBUS 1	SESSION 202 CRATE-TO-CRATE COMMUNICATIONS	SESSION 203 REAL-TIME SOFTWARE: PART 2	SESSION 204 EMERGING TRANSPUTER TECHNOLOGY
WEDNESDAY, OCTOBER 5	9:00 AM-11:00 AM	SESSION 301 VXI INSTRUMENTATION BUS	SESSION 302 HIGH-PERFORMANCE ARCHITECTURES	SESSION 303 DESIGNING FOR THE MILITARY	SESSION 304 ADA TUTORIAL
WEDNESDAY, OCTOBER 5	2:00 PM-4:00 PM	SESSION 401 NEW ISSUES IN VMEBUS	SESSION 402 DEVELOPMENT TOOLS FOR RISC	SESSION 403 REAL-TIME GRAPHICS	SESSION 404 DESIGNING FOR SURFACE MOUNT
THURSDAY, OCTOBER 6	9:00 AM-4:00 PM	SESSION 501 NEW ISSUES IN MULTIBUS II	SESSION 502 STEPWISE DEBUGGING	SESSION 503 PARALLEL PROCESSING TECHNOLOGY	SESSION 504 UNDERSTANDING BENCHMARKS
THURSDAY, OCTOBER 6	2:00 PM-4:00 PM	SESSION 601 NEW DEVELOPMENTS IN IEEE 896	SESSION 602 IMPLEMENTING BITBUS	SESSION 603 INDUSTRIAL NETWORKS	SESSION 604 DESIGNING FOR TESTABILITY

GENERAL SESSIONS— WEDNESDAYS, OCTOBER 5
11:00 AM-NOON — SESSION 1000 — EDITOR'S FORUM
6:00-8:00 PM — SESSION 2000 — RISC SYMPOSIUM

Display technology is often the last thing you specify.

And the first thing your customer sees.



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CIRCLE NO 148

between chassis, hardware considerations in high-performance architectures, stepwise bebugging, development and run-time tools for RISC, and implementing BitBus.

Applications and trends

If you're interested in application development, take advantage of the material that will be presented in track 3. The "Introduction to Real-Time Systems" seminar will include information on programming, multitasking, task attributes, and operating systems. The second track 3 seminar will discuss two communications technologies, FDDI and ISDN, and the accompanying benefits, features, architectural requirements, and application areas. Speakers in this track will present a wide variety of topics—from real-time software and designing for the military to real-time graphics and parallel-processing technologies.

Track 4 is entitled "Electives," and it begins with a half-day ASIC tutorial seminar that will cover three main areas: ASIC economics, digital ASIC applications, and analog ASIC applications. One session, "Quo Vadis? The Future of the Bus/Board Industry" is free to all Buscon attendees. This forum will include a summary of a Cahners Publishing bus/board study; a panel of industry experts will address such issues as the need for higher-performance architectures, opportunities for innovation, and bus/board application areas. Other sessions in track 4 will detail Ada, Transputer technology, benchmarking, designing for testability, and designing for surface mount.

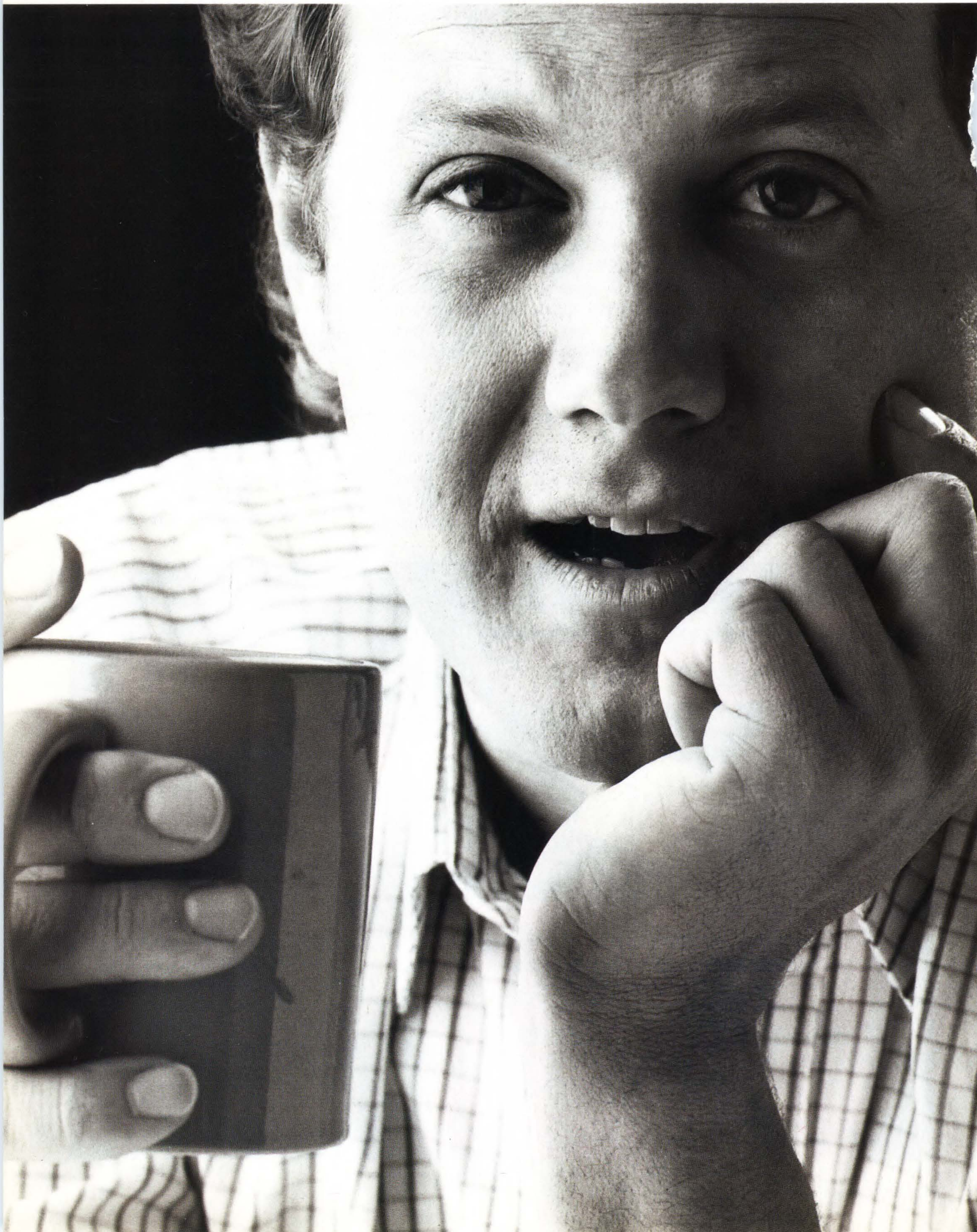
You can take advantage of two other free sessions at Buscon. At "The Editor's Forum," you can meet editors from industry publications who will lend their expertise and answer your questions about developments in buses and boards. And if you're interested in the RISC vs CISC controversy, don't miss the "International Board-Level Symposium." Representatives from industry and the press will get together for a debate of the issues.

Attending Buscon doesn't mean *all* work; this show gives you the opportunity to talk to and relax with your peers and colleagues. On Tuesday, October 4, the Buscon exhibitors will host a reception for all exhibit hall and conference attendees. On Wednesday, you can attend the "all-aboard" reception and mingle with vendors, attendees, and editors over wine and cheese.

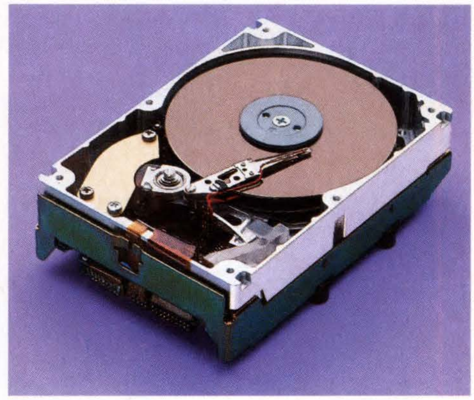
For more information on Buscon/88 East, you can contact CMC, 200 Connecticut Ave, Norwalk, CT 06856. Phone (203) 852-0500. **EDN**

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517

"I shop the specs



because it's my job. But I buy the product because it's my career."



WHAT YOU SHOULD KNOW ABOUT THE NEW PRODRIVE SERIES™ OF 3½-INCH HARD DISK DRIVES FROM QUANTUM.

The numbers are the easy part. Either a product has them or it doesn't.

But you can't build a system out of specs.

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Our new ProDrive Series of 3½-inch hard disk drives offers you the broadest range of capacities in the broadest range of interfaces in the industry. 42 and 84 megabytes formatted with embedded SCSI and AT-Bus interface, right now. And later this year, up to 168 megabytes, in SCSI, ESDI and AT-Bus. Ten new drives in all.

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CIRCLE NO 149


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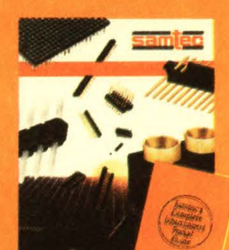

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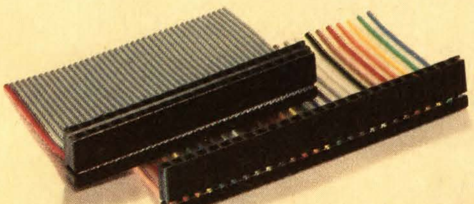
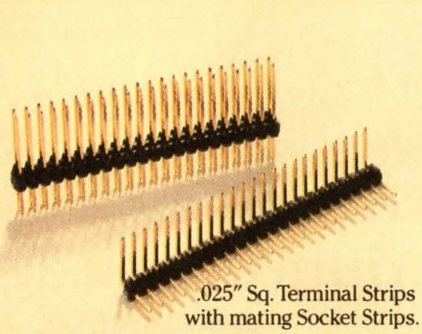
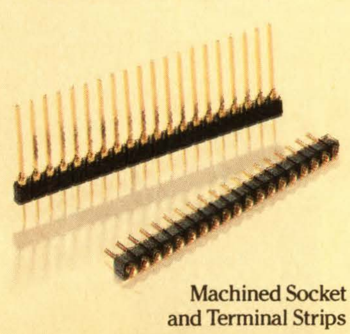


IDC Cable Strips with mating Terminal Strips.



.025" Sq. Terminal Strips with mating Socket Strips.



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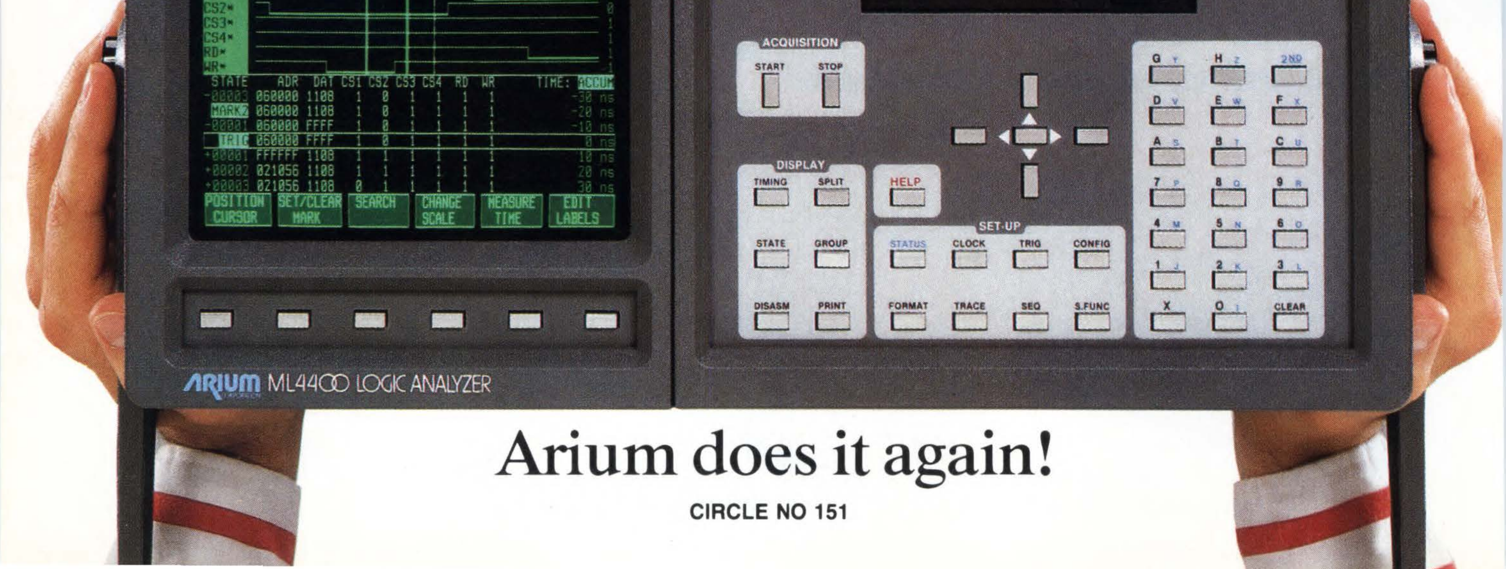


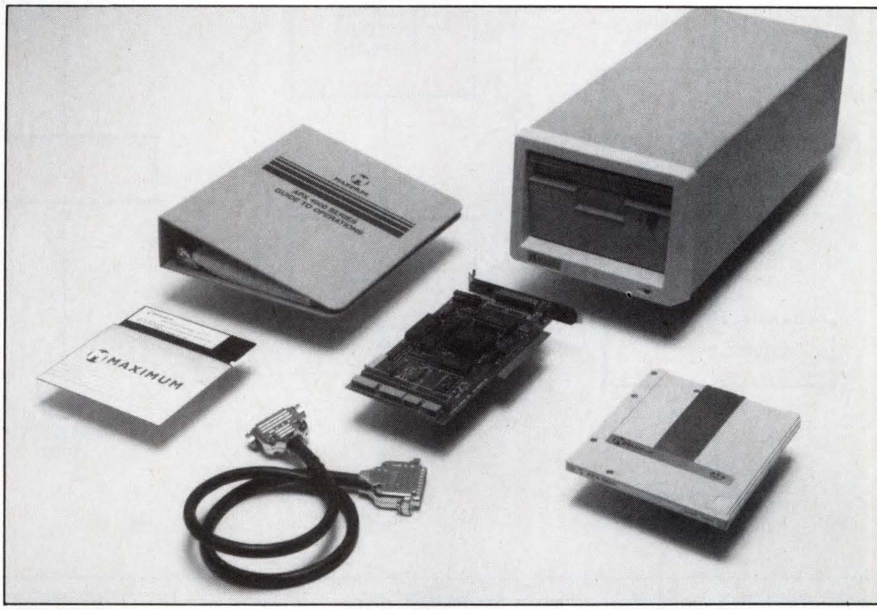
Arium does it again!

CIRCLE NO 151

5 1/4-in., 488M-byte, optical WORM drive challenges high-performance hard disks

The full-height, 5¼-in., APX-4000 optical WORM (write-once, read-many) disk drive stores 244M bytes on each side of a 2-sided disk providing a total storage capacity of 488M bytes. The product can also read and write optical disk cartridges in a half-density format that is compatible with the company's older APX-3000 disk drive. Along with the drive, the company has created a universal file-management software package that allows an operating system to read optical disk files created by other operating systems.

Initially, the company is offering two storage subsystems, based on the APX-4000 drive, for the IBM PC bus: the $4250 APX-4100 subsystem, which mounts inside a PC, and the $4450 APX-4200 subsystem, which includes a case and power supply so that the WORM drive can operate external to the PC. The subsystems accept single-sided APX-3300 and double-sided APX-3600 disk cartridges costing $125 and $175, respectively. Both subsystems include the drive itself, a controller board that adapts the drive's modified ESDI port to the IBM PC bus, cables, Maxsys file-system software that seamlessly integrates the WORM drive's capabilities into MS DOS, and utility programs for file version control and deleted-file recovery.



***This optical WORM disk subsystem** for the IBM PC bus accepts 1- and 2-sided removable cartridges that hold 244M bytes of data/side.*

In a key strategic decision, the company went beyond the traditional route of offering hard-disk emulation software for this optical WORM drive. Instead, it provides a complete hierarchical file manager that attains a much higher level of storage efficiency than mere hard-disk emulation. As shown in **Fig 1a**, hard-disk emulation software typically intercepts data transfers to and from the optical disk at the device-driver level, making the WORM disk appear to support erasable files.

Most operating systems assume that disk drives contain erasable media; thus, the software that allows optical WORM drives to emulate hard disks can produce suboptimal performance results. Operating systems frequently move large chunks of data around on the disk when updating and rewriting files, assuming that the liberated sectors can be reused. However, such a scheme quickly wastes available storage space on a write-once disk, resulting in poor storage efficiency. Through experimentation, the company discovered that some hard-disk emulation software strips a WORM disk of 50% (or more) of its rated capacity. Overhead information consumes the remaining disk capacity.

In contrast, the Maxsys file system for the APX-4000 drive intercepts file I/O operations at the operating-system call level, bypassing the operating system entirely (see **Fig 1b**). The Maxsys hierarchical file manager understands that files stored on a write-once disk are indelible, and it moves a minimal amount of data around on the disk in response to file I/O requests while retaining the ability of write-once media to recover previous versions of a file. As a result, the company claims its Maxsys software attains storage efficiencies of 94% with its WORM drive.

This file-system software also helps the drive subsystem attain high transfer rates. In data-transfer tests using large files, the company found that the APX-4000 subsystems for the IBM PC provided

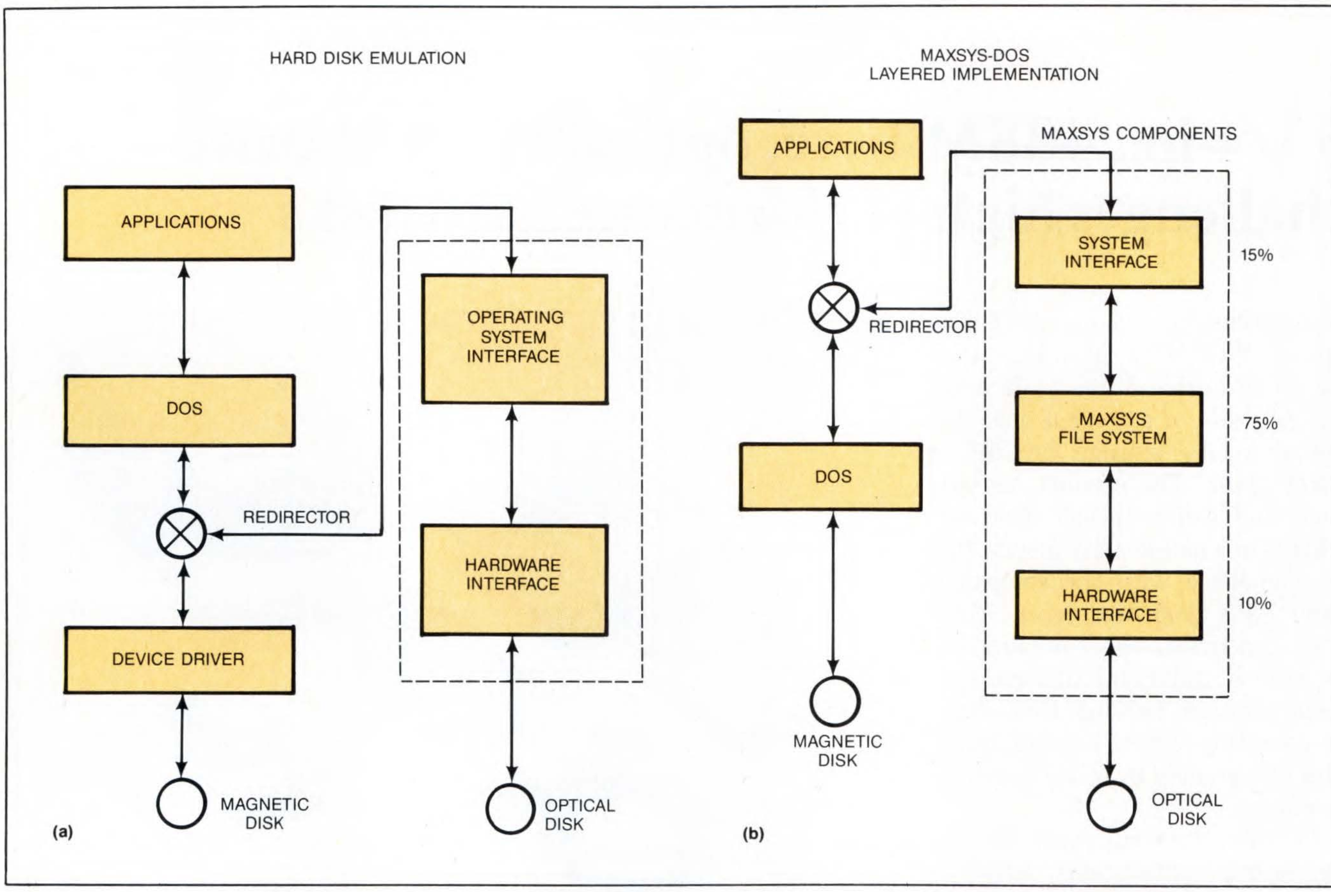


***Fig 1—Hard-disk emulation software for WORM drives** intercepts file I/O at the driver level **(a)**. In contrast, the Maxsys file-system software achieves much better storage efficiencies by intercepting data transfers at the operating-system call level **(b)**.*

transfer rates comparable to hard disks that have an average access-time rating of 28 msec. Thus the optical drive has an "effective access-time" spec of 28 msec. The APX-4000's performance does not degrade as the disk fills.

The modular nature of the file-system software eases the task of adapting the Maxsys software to various operating systems. The Maxsys file-system software consists of three components: the file system itself, hardware-interface code that links the file system software to the disk drive, and system-interface code that links the file system to the operating system. To move this software from one operating system to another, you need only rewrite the system interface, representing about 15% of the code, and then recompile the entire software package for the new target system. You may also need to rewrite the hardware-interface software for new hardware configurations.

To aid in the task of rewriting the system-interface code, the company has created a high-level, C-language specification for the interface between the file-system software and the system-interface software. The company supplies this specification, called OASIS (optical advanced software interface standard), to companies wishing to integrate the APX-4000 into other operating-system environments. Any operating system can read files created by any other operating system that employs the Maxsys software because the software creates the same file structures for every computer.

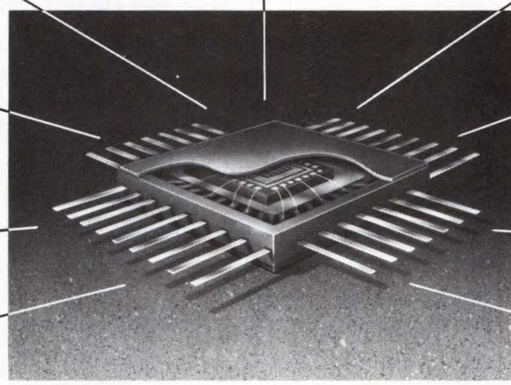
The company plans to offer a SCSI-based optical-disk subsystem for Unix-based workstations from Sun Microsystems. This subsystem, which will be available by the end of the year, will cost about the same as the IBM PC subsystems. The company is using its OASIS interface specification to link its WORM drive with Sun's Unix operating system, so its optical disk cartridge can serve as a medium for data interchange between the Unix and MS DOS systems.

—Steven H Leibson

Maximum Storage Inc, 5025 Centennial Blvd, Colorado Springs, CO 80919. Phone (719) 531-6888.

Circle No 735

SONY'S ECL LOGIC HAS THE GUTS TO CHALLENGE GaAs PERFORMANCE.



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CXB1102Q	Quad 2-in EXOR/NOR	490 ps	1.5 GHz	680 mW	24 FLAT
CXB1103Q	Quint Line Receiver	410 ps	1.5 GHz	650 mW	24 FLAT
CXB1104Q	Dual D Flip Flop	620 ps	3.2 GHz	520 mW	24 FLAT
CXB1105Q	Triple Fan-out Buffer	590 ps	1.5 GHz	720 mW	24 FLAT
CXB1106Q	4-Stage Ripple Counter		3.4 GHz	720 mW	24 FLAT
CXB1107Q	Decision Circuit		3.2 GHz	430 mW	24 FLAT
CXB1108Q	Laser Driver		2.0 GHz	740 mW	16 FLAT
CXB1109Q	Quad D-FF with Master Reset	620 ps	3.4 GHz	790 mW	24 FLAT
CXB1110Q	16 to 1 Multiplexer	610 ps	1.5 GHz	680 mW	24 FLAT
CXB1111Q	Look Ahead Carry Block	580 ps	1.5 GHz	610 mW	24 FLAT
CXB1112Q	Phase Frequency Detector	720 ps	0.8 GHz	500 mW	24 FLAT
CXB1113Q	4 to 1 Multiplexer		2.0 GHz	950 mW	24 FLAT
CXB1114Q	1 to 4 Demultiplexer		2.5 GHz	1100 mW	24 FLAT
CXB1130Q	9, 8, 4-bit Multiplexer		1.6 GHz	730 mW	32 FLAT
CXB1131Q	9, 8, 4-bit Demultiplexer		1.6 GHz	1000 mW	32 FLAT
CXB1132Q	9, 8, 4-bit Universal Shift Register		1.3 GHz	910 mW	32 FLAT
CXB1133Q	22, 15, 7-Stage Scrambler		1.6 GHz	600 mW	24 FLAT
CXB1134Q	22, 15, 7-Stage Descrambler		1.6 GHz	610 mW	24 FLAT
CXB1135Q	8-16 bit Comparator		1.3 GHz	630 mW	32 FLAT
CXB1136Q	8-bit Universal Counter		1.2 GHz	730 mW	32 FLAT
CXB1137Q	8-bit Shift Matrix	1250 ps		700 mW	24 FLAT
CXB1138Q	4-bit Arithmetic Logic Unit	1460 ps		680 mW	24 FLAT

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CIRCLE NO 153

PRODUCT UPDATE

NuBus interface chipset reduces development time

If you design add-in boards for Apple's Macintosh II computer, you should consider the SN74ACT2440 (ACT) and SN74BCT2420 (BCT), a 2-chip NuBus interface set. The ACT is a 32-bit NuBus interface controller, and the BCT is a 16-bit NuBus transceiver. Using one ACT and two BCTs, you can implement a 32-bit master/slave interface that conforms to the IEEE P1196 specification. You no longer have to develop extensive NuBus design expertise to implement the NuBus protocol in your design.

The ACT is a TTL-compatible device that handles NuBus signaling protocol. Fabricated in 1-μm EPIC (enhanced performance implanted CMOS), this 68-pin IC works in master, slave, and master/slave applications. You can functionally organize the chip's input and output signals into five groups: NuBus status outputs; master/slave inputs; data/address interface control; byte decode; and NuBus card slot signals. The chip actually has more status and control lines than the IEEE P1196 requires, allowing you to design more sophisticated applications.

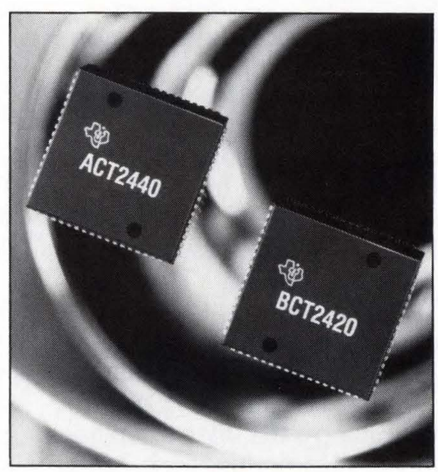
The NuBus status outputs provide buffered NuBus signals. You can use the master/slave inputs to control the master and slave state machines. The master state machine initiates bus locking and unlocking, performs arbitration, and provides status bits for cycle control. The slave state machine monitors the NuBus status and notifies the local board when the NuBus addresses it. The data/address interface control provides buffering signals for multiplexing and demultiplexing the data/address lines. The byte decode differentiates among the various types of NuBus cycles.

The BCT 68-pin BiCMOS device contains an on-chip comparator for slot identification. Providing multiplexed or latched address and data transfers, each BCT offers three 16-bit I/O ports and saves address and data information during each NuBus write cycle. The BCT also contains bus transceiver circuits, D-type flip-flops, latches, and control circuitry.

The interface solution offered by this chipset replaces as many as 45 discrete logic devices and provides you with as much as 66% more pc-board real estate that you can use to increase functionality or to add onboard memory. The ACT sells for $24, and the BCT costs $13.33 (1000).—***J D Mosley***

Texas Instruments, Semiconductor Group (SC 850), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 739



Reducing the component count to three chips for your NuBus interface applications, *Texas Instrument's SN74ACT2440 and SN74BCT2420 controller and transceiver ICs can save both board space and development time.*

THIS T1 TRANSCEIVER IS SMALLER, DESIGNED SMARTER, AND OUTPERFORMS THE COMPETITION.

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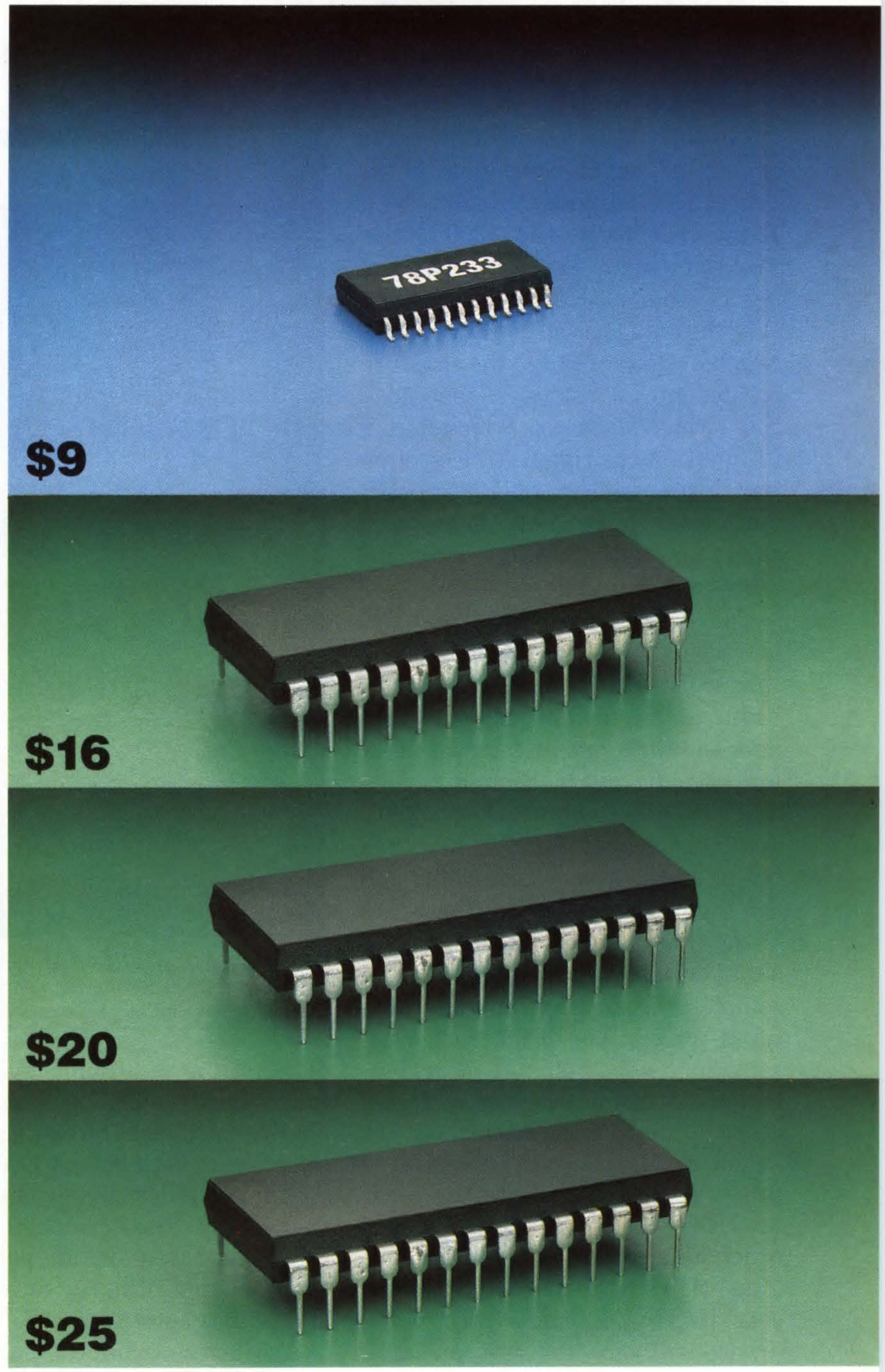
For a copy of our comprehensive T1/CEPT data sheets, and a listing of the company's complete line of telephony products, contact: **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680



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CIRCLE 32 FOR PRODUCT INFORMATION

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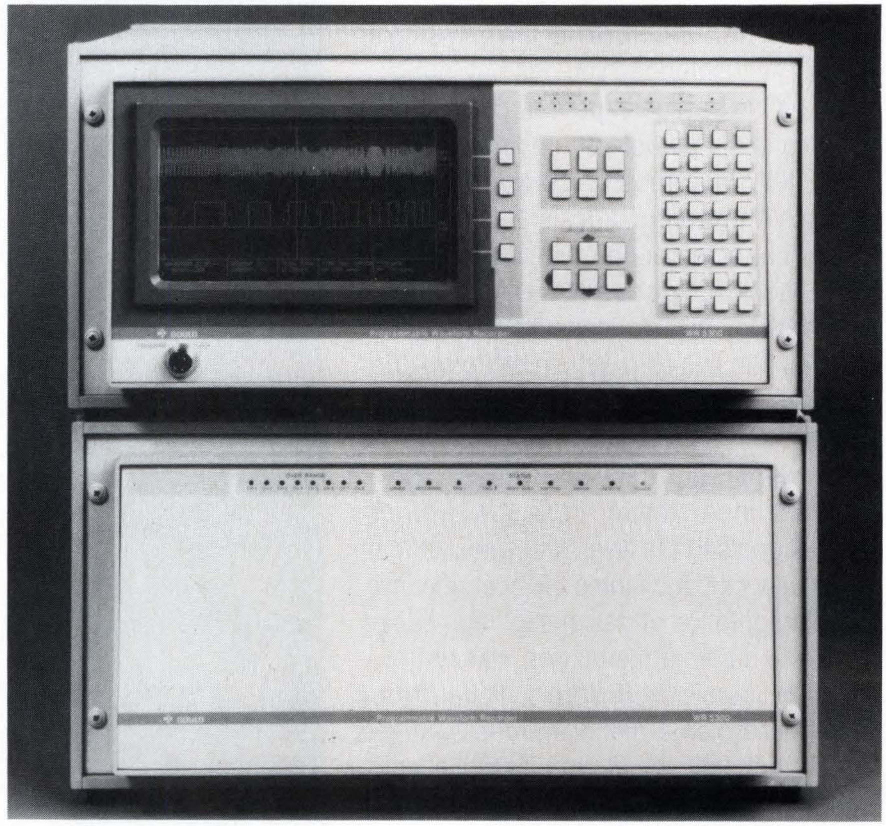
Programmable waveform recorder scans 16 channels at 1M samples/sec/channel

Allowing you to monitor eight analog and eight event data channels at 1M samples/sec/channel with 12-bit resolution, the 5300 series Programmable Waveform Recording System also lets you capture only the data that meet your specifications. You specify the capture parameters via a software tool called the Event Manager, which has a 21-input, dual-trigger tree system that uses logical AND and OR functions to discriminate among more than one-half million transient events.

The 68000-based 5300 has two independent clock functions: a real-time clock that you can program to begin an acquisition at a specific data and time, and an interval timer for periodic event sampling. The unit's 10-MHz master clock allows you to program the unit's dual time bases in 100-nsec increments. You can toggle the speed characteristics of the time bases and specify acquisition delay over time or number of samples. Such programming features prevent the 5300 from oversampling, while helping you achieve longer recording sessions and gain efficient memory utilization.



***Available with or without an Intelligent Front Panel,** Gould's Model 5300 programmable waveform recorder contains two dime bases, 18 independent signal inputs, an IEEE-488 group trigger, and two independent trigger trees.*

You can use a host computer to program the 5300 via its RS-232C or IEEE-488 port. Or you may order an optional Intelligent Front Panel (IFP) with an electroluminescent display that comes with menu-driven software for system setup and waveform display. The IFP attaches to the front of any 5300 chassis and has a dedicated bus for controlling as many as eight 5300 units.

Multi-unit synchronization provides true master/slave control without time skew, because all the units share a single system clock. You can also run a multi-unit system in multi-master mode with each unit sharing common time bases but maintaining independent Event Managers. An IEEE-488 group trigger function lets the 5300 begin acquiring data based on an automated software algorithm or an event as simple as a keystroke.

Another software tool, called the Memory Manager, lets you optimize the 5300's memory utilization. You can define the channel depth of its memory from 256 to more than 2 million samples per acquisition in increments of 256 samples.

Other options include a D/A converter for hardcopy output to standard oscillographic recorders. You can also select from three 12-bit A/D converters. A software package called ACQ5300 simplifies system set-up and data acquisition via interactive, pop-up panels. However, you can also edit all the text, prompts, help messages, and colors; or you can develop and run macros for automatic configuration or for querying a system operator. ACQ5300 runs on IBM PC/AT-compatible computers and sells for $1200. Pricing for the 5300 begins at $15,000. ***—J D Mosley***

Gould Inc, Test and Measurement Div, 3631 Perkins Avenue, Cleveland, OH 44114. Phone (216) 361-3315.

Circle No 736

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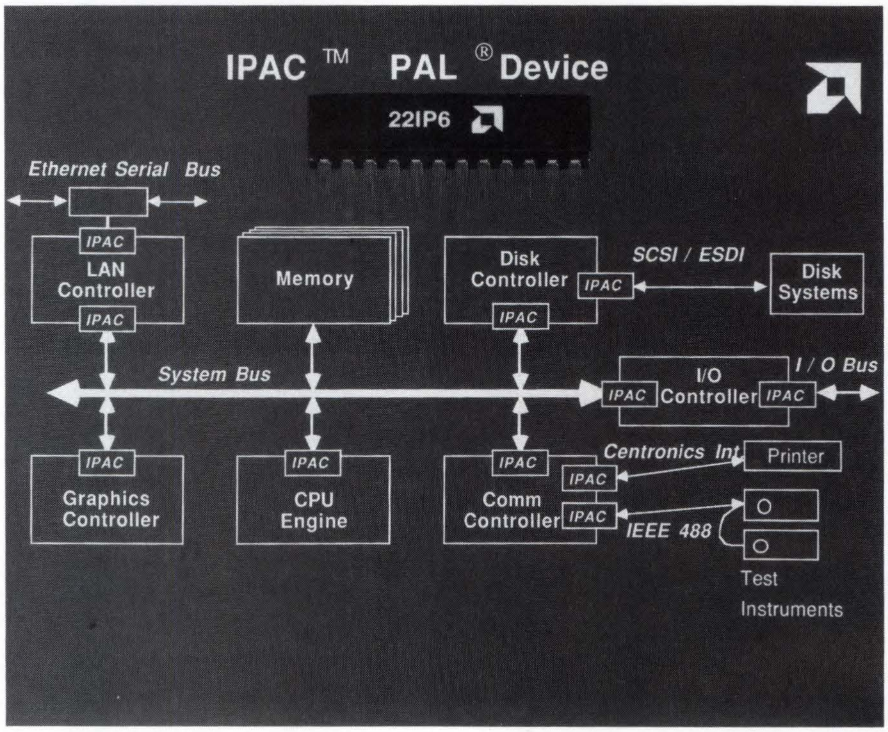
Programmable logic device simplifies design of asynchronous interfaces

The PAL22IP6 interface protocol asynchronous cell (IPAC) is a programmable logic device optimized for asynchronous interface applications. Each of the device's six macrocells offers nine logic product terms and an unusual type of storage element—a clockless flip-flop.

The IPAC features three dual-toggle (2-T) and three set-reset (S-R) flip-flops. Both types respond to the edges of their input signals. An active edge on either input of the 2-T flip-flop causes the output to toggle. Only the edges on the set or reset inputs of the S-R flip-flop specify the output; the input level is ignored. Both types of flip-flops also have independent, level-sensitive, asynchronous preset and clear inputs.



*The **PAL22IP6 interface protocol asynchronous cell (IPAC)** offers 14 inputs, six outputs, and asynchronous storage elements. Each output can drive 48 mA and has an independently programmable output-enable function.*

The designers of the IPAC paid close attention to the problem of metastability in asynchronous designs. By eliminating the requirement for a separate clock at the registers, they removed the data setup and hold constraints usually needed to avoid entering metastable states. The design of the circuit's response to simultaneous inputs also reduces the possibililty of metastability.

If the active edges are more than 5 nsec apart, the 2-T flip-flop will respond properly to both inputs; if the active edges are closer together, it will ignore both inputs. (The output may glitch if the 5-nsec minimum spacing is violated, but there is no possibility of metastability.) The minimum time between set and reset edges for proper operation of the S-R flip-flop is 27 nsec; the output is unaltered if the time is less than 6 nsec. Only if the edges occur within 6 to 27 nsec of each other is the S-R flip-flop output unpredictable. The asynchronous preset and clear inputs override the other inputs on each flip-flop, and the preset input dominates the clear input when both are present.

Offering flexibility in the use of macrocells, the IPAC allows you to select either registered or combinatorial output for each macrocell and to disable each output independently. Each output supplies 48 mA of drive current. You can select from the six outputs, 14 inputs, and their 20 complements to form 2-level AND-OR product terms for any S, R, or T input; to form an OR term for any preset or clear signal; and to form an AND term for output control. And you can specify either polarity for the input edges of each flip-flop. The device is programmable on standard PLD programmers.

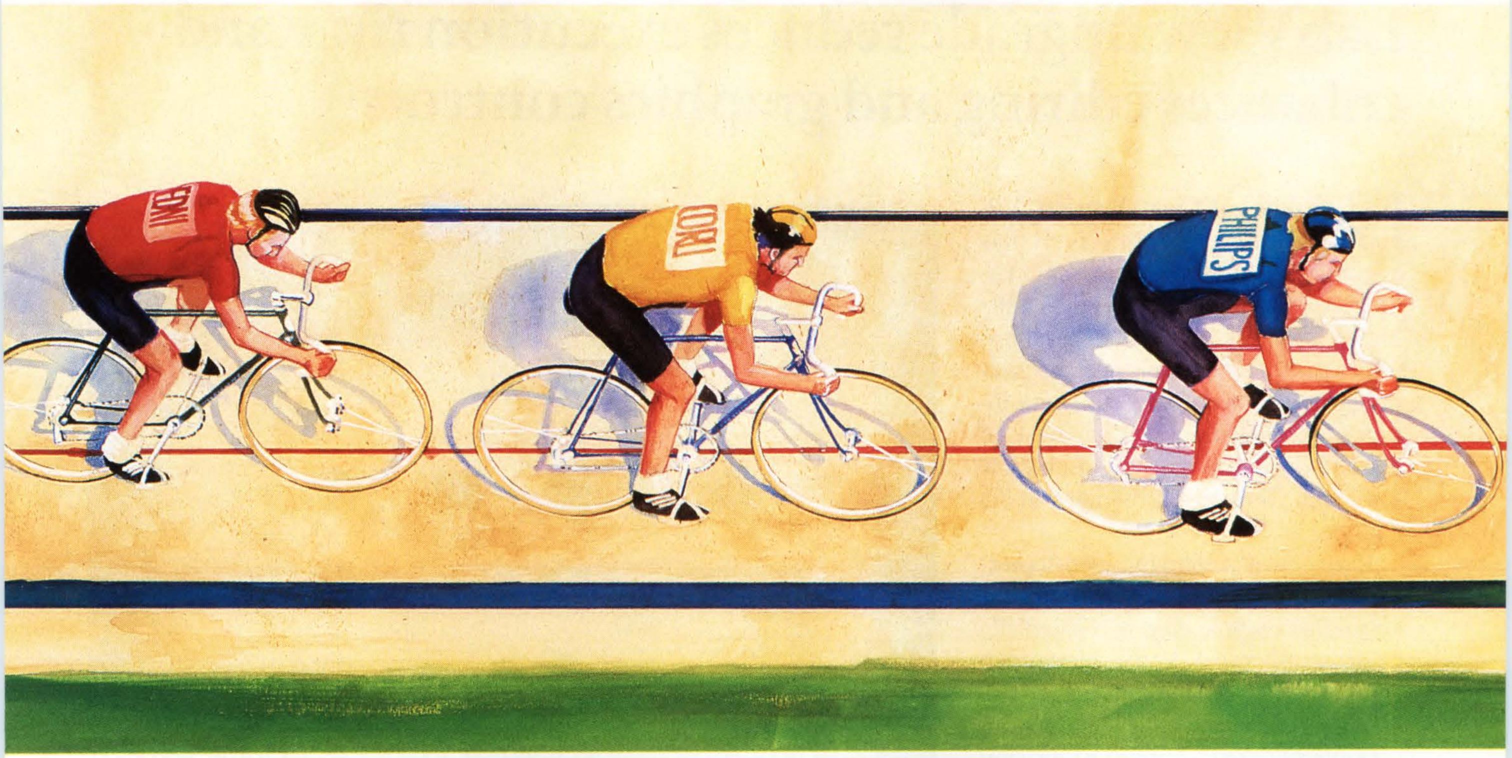
The package style of the IPAC features center V_{CC} and ground pins to reduce ground bounce. The part comes in plastic or ceramic DIPs at prices of $13.95 and $14.65 (100), respectively.

—Richard A Quinnell

Advanced Micro Devices, Box 3453, Sunnyvale, CA 94086. Phone (408) 732-2400.

Circle No 738

PHILIPS IR LED'S SPEED AND ENDURANCE



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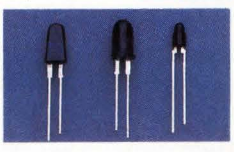

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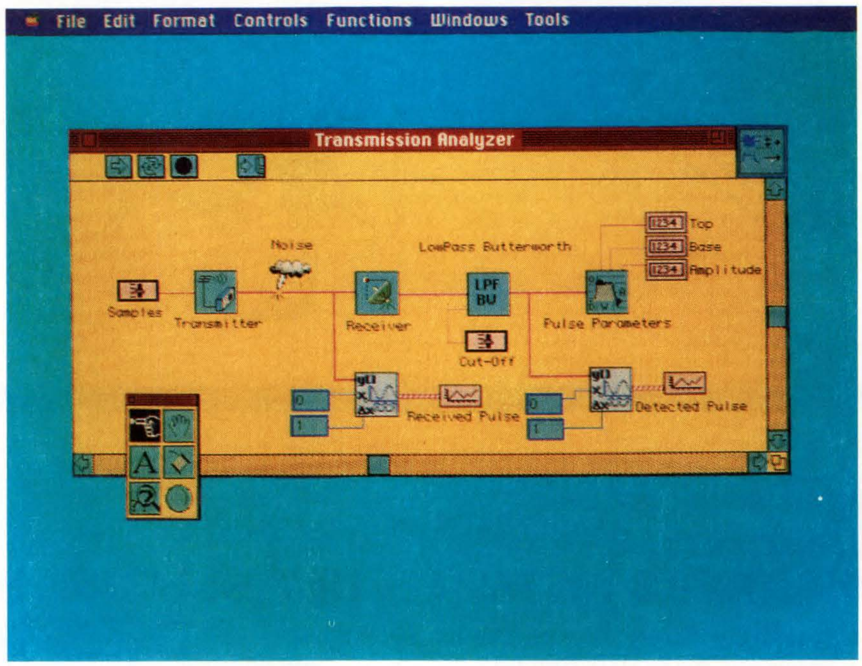
LabView upgrade reduces execution time and enhances editing and graphics controls

If you like LabView Version 1.2, you'll love the 2.0 upgrade. It has a compiler that significantly reduces execution time, provides editing capabilities like rubberbanding, offers graphics controls such as panning and zooming, and supports integer data elements. But, best of all, the company will give LabView 2.0 to all Version 1.2 owners at no charge.

LabView is a colorful, icon-based, graphical programming system that simplifies engineering and scientific programming on Apple Macintosh computers by permitting you to design software-generated "virtual instruments." But, instead of writing lines of code, you produce these instruments by drawing block diagrams that represent test and measurement functions. You then control these instruments via pictorial renditions of the types of switches, dials, and levers you might actually find on 3-D versions of such equipment.

In Version 1.2, the graphical programming language is interpreted as it runs. In Version 2.0, a graphical language compiler generates machine code from the block diagrams that compose your virtual instrument. So I/O intensive applications can realize as much as a 300% speed advantage over your 1.2 rendition, and computation-intensive applications developed under the new software can run as much as 60 times faster. And, LabView 2.0 can run all the applications you've developed under Version 1.2

To reduce memory requirements and to further increase execution speed, LabView 2.0 adds multiple integer and floating-point data formats to the old version's extended precision floating-point data type. For embedded LabView applications, the manufacturer provides a run-time system for "operate-only" end-user functions. The program's object-oriented open-architecture and dynamic linking mechanism lets you write C code and link it to LabView without recompiling the LabView code.



Providing an extensive graphics interface and compiled execution speed, *LabView Version 2.0 simplifies your design efforts when prototyping virtual instruments.*

The rubberbanding feature lets wires remain attached to and move with an icon as you relocate it within a block diagram. You can select multiple objects for group manipulations, or cut and paste icons, front panels, and block diagrams from one part of a virtual instrument to another area in the same device or to a different instrument.

If you don't have LabView 1.2, you can buy the Version 2.0 for $1995. The company also plans to distribute libraries of LabView instrument drivers via its MacNet electronic bulletin board and on 14 3½-in. floppy disks. The disks cost $50 each, and access charges for MacNet vary from $4 to $8 per hour. ***—J D Mosley***

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (512) 250-9119. TLX 756737.

Circle No 737

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Organized as 64 words by-4 and by-5 bits wide, these RAM-based devices deliver performance unmatched in the industry—at 10, 15, 25, 40 and 50 MHz.

Even so, they consume no more power than CMOS FIFOs, while offering high output drive that's TTL compatible. And they can be cascaded to expand in word width and depth. Plus they're available in both commercial and military temperature ranges, in industry-standard pin-outs.

This new generation of FIFOs will soon include 64 by 9 and larger density 512, 1K and 2K by 9 devices. Joining Saratoga's existing lines of high-performance TTL and ECL static RAMs—also among the fastest now available. And all made possible by our proprietary BiCMOS technology—SABIC™—which combines the best of both the bipolar and CMOS worlds.

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Clock Frequency	50 MHz (40 MHz military)
Data Access Time	15 nsec
Data Set-up and Hold Time	3 nsec
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Output Drive	16 mA

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The Technology Leader in BiCMOS

CIRCLE NO 158

Introducing The First 50-MHz FIFOs. In BiCMOS.

ASIC-verification system produces 200-MHz patterns and uses Unix-like OS with XWindows

The HP 82000 boasts hardware and software that its developers are confident will set it apart from the competition. ASIC-verification-system vendors target their products primarily at engineers who develop custom digital ICs and those who produce the devices in limited quantities. Therefore, ASIC verifiers don't need to test devices as rapidly as do automatic test systems intended for high-volume production.

Many users, however, will no longer accept systems that test devices only functionally—that is, systems verifying that the prototypes actually perform the same functions as the parts simulated during development. Most users now demand systems that, after testing a few prototypes, provide high confidence of acceptable production yields. Such systems must have static and dynamic parametric-test capability. And because test development is such a large factor in the life-cycle cost of producing parts in low volume, users are demanding tools to speed test development.

If the preceding requirements aren't enough, the increasing complexity of ASICs, evidenced by ascending pin counts, and their increasing speed make the job of ASIC-verifier designers still more challenging. The engineers at Hewlett-Packard's Boeblingen, Germany instrument division set out to meet these challenges. The resulting system uses a 68030-based HP 9000 Series 360 computer with 8M to 32M bytes of main RAM, a hard disk of at least 120M-byte capacity, and a cartridge-tape backup unit. It runs under HP-UX (the vendor's real-time extension of the Unix operating system) and the XWindows graphics-environment manager.

The desktop configuration of HP's 82000 ASIC verifier can accommodate 80 channels. Larger systems, with as many as 384 channels, place the test electronics in a free-standing enclosure, which includes the DUT interface.

To simplify program development and debugging, the large-screen, high-resolution monitor displays multiple windows, similar to those available on larger and more costly automatic test systems. With this monitor, you use a mouse to make selections from menus, to control editing, and to set the size and shape of screen windows.

You can expand the test hardware to drive and sense 384 channels. The true tester-per-pin architecture eliminates fixture wiring for devices in many dual-in-line and pin-grid packages and allows you to reconfigure channels individually. For example, if you want to "borrow" pattern memory from one channel to provide deeper memory on another, you need affect only two channels—the one contributing its memory and the one receiving it. HP spokesmen point out that the advent of tester-per-pin architecture has prompted companies whose testers share resources among channels (an older, less expensive, and less flexible design approach) to coin yet another term in automatic test's arcane, inscrutible lexicon: "per-pin" architecture. HP claims that when vendors use the term "per-pin" to mean the opposite of "tester-per-pin" they confuse

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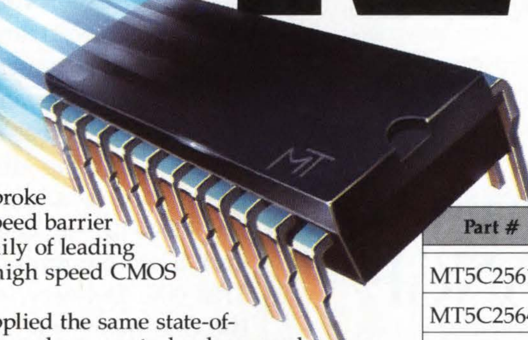

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MT5C2565	64K X 4 $\overline{OE}$	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C6404	16K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 S. I/O	**15ns**	PDIP, CDIP, SOJ
MT5C6408	8K X 8	**15ns**	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C1604	4K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 S. I/O	**15ns**	PDIP, CDIP, SOJ
MT5C1608	2K X 8	**15ns**	PDIP, CDIP, SOJ

*Slower speeds also available.

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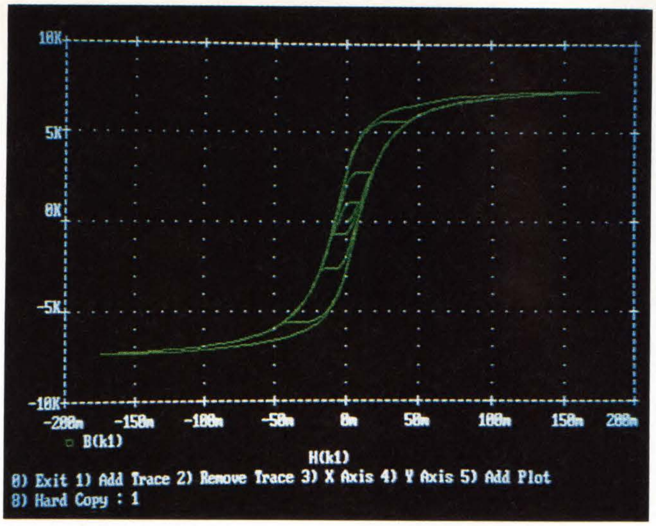
MICRON TECHNOLOGY, INC., 2805 E. COLUMBIA ROAD, BOISE, IDAHO 83706 208-386-3900 prospective buyers—perhaps quite intentionally.

Each of the tester's channels can drive and sense at 200 MHz, a rate that's extremely fast even for a more expensive system. The total edge-placement error is 250 psec. To run at this speed, you do not have to sacrifice channel capacity. In addition, without sacrificing channels, you can burst out 128k-word-deep patterns to the DUT (device under test). The system can output patterns in the following formats: return to 1, return to zero, return to complement, and delayed nonreturn to zero. You can select between edge and window comparison; to accommodate devices fabricated using most semiconductor-manufacturing processes, you can vary the threshold levels from −4 to +8V.

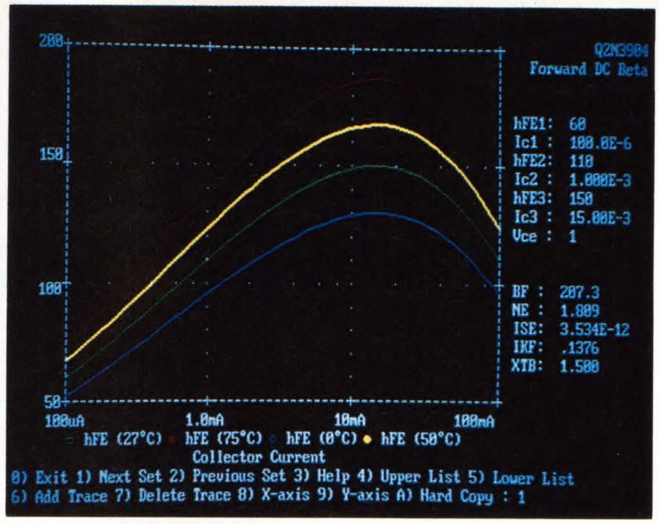
To cut test-development time, the system software provides an automatic test generator and linkage to CAE programs. It provides many choices of test-result displays, including timing diagrams, error maps, state lists, and schmoo plots. HP 82000 pricing begins at $65,000, and a 64-channel system costs $193,000. Delivery is scheduled for the first quarter of 1989.

—Dan Strassberg

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.



Waveform display from Probe



Characterizing a Transistor with Parts

PSpice

The Standard for Analog Circuit Simulation Now Available for OS/2

Since its introduction over four years ago, MicroSim's PSpice has sold more copies than all other commercial SPICE programs combined. Now PSpice is available for the OS/2 operating system on the PC family of computers:

- Larger circuits can be simulated. Maximum circuit size is limited only by the amount of RAM which is installed in the PC.
- The multitasking ability of OS/2 allows running PSpice as a background task, freeing the PC for other uses.

All these features which have made PSpice so popular are available:

- Standard parts libraries for diodes, bipolar transistors, small-signal JFET's power MOSFET's opamps, voltage comparators, and transformer cores.
- GaAs MESFET devices, BSIM MOS model.
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

All these PSpice options are available under OS/2:

- Monte Carlo analysis to calculate the effect of parameter tolerances on circuit performance.
- The Probe "software oscilloscope", allowing interactive viewing of simulation results. The left photograph above is a Probe display.
- The Parts parameter extraction program, allowing you to extract a device's model parameters from data sheet information. The right photograph above is a Parts display.
- The Digital Files interface, allowing you to transfer data from your logic simulator to (or from) PSpice. The interface performs the necessary D to A or A to D conversions.

In addition to the PC, PSpice is also available on these computers:

- The Macintosh II.
- The Sun 3 and 4 workstations.
- The VAX/VMS family, including the Micro VAX II.

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CIRCLE NO 160

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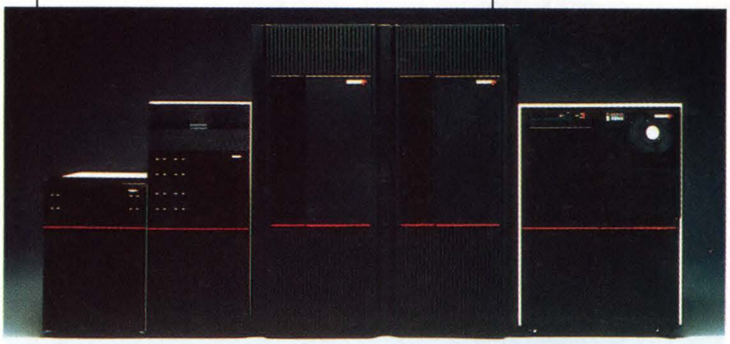

The Tandem NonStop VLX™ system.

later, is Tandem still completely sold on Teradyne's High Density Plus? "We made the right choice with Teradyne. And we look forward to working with Teradyne to meet future interconnection requirements."

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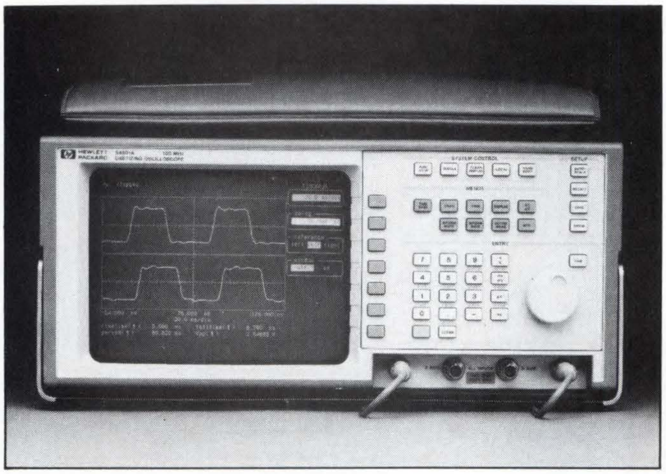
READERS' CHOICE

Of all the new products covered in EDN's **June 9, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our **June 9, 1988,** issue, or use EDN's Express Request service.

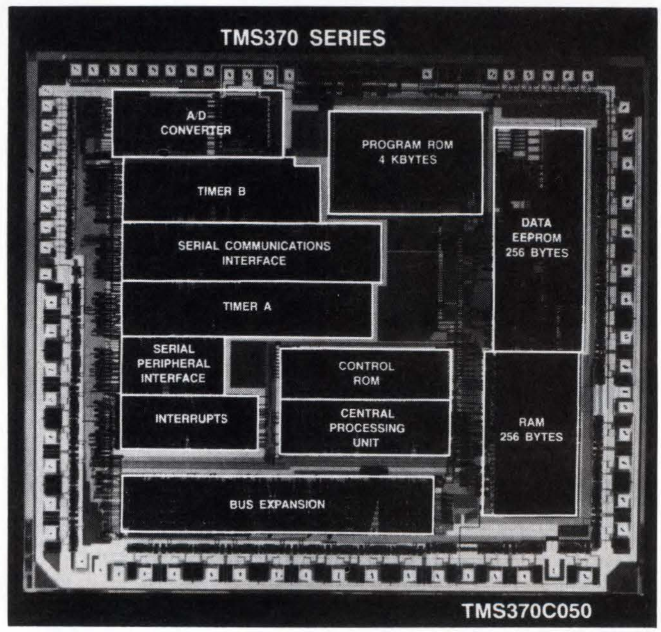


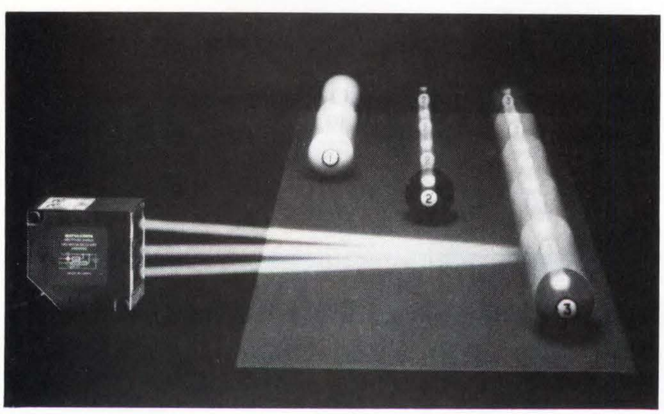
◀ DIGITAL STORAGE SCOPE

The HP 54501A 4-channel, 100-MHz DSO brings you digital-storage-oscilloscope features at a price ($3465) substantially closer to that of an analog scope (pg 94).
Hewlett-Packard Co.
Circle No 601

μC FAMILY ▶

The TMS370 family of 8-bit μCs offers you the convenience of configuring a semicustom μC from a list of available modules (pg 96).
Texas Instruments Inc.
Circle No 605



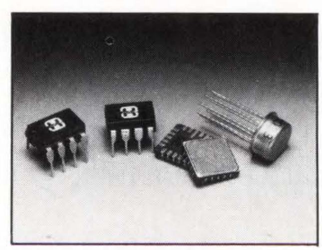


▲ SENSORS

MQ triple-beam photoelectric sensors have a sensing capability ranging from 1 in. to 2 ft, and they feature operating speeds of 200 operations/sec max (pg 284).
Aromat Corp.
Circle No 603

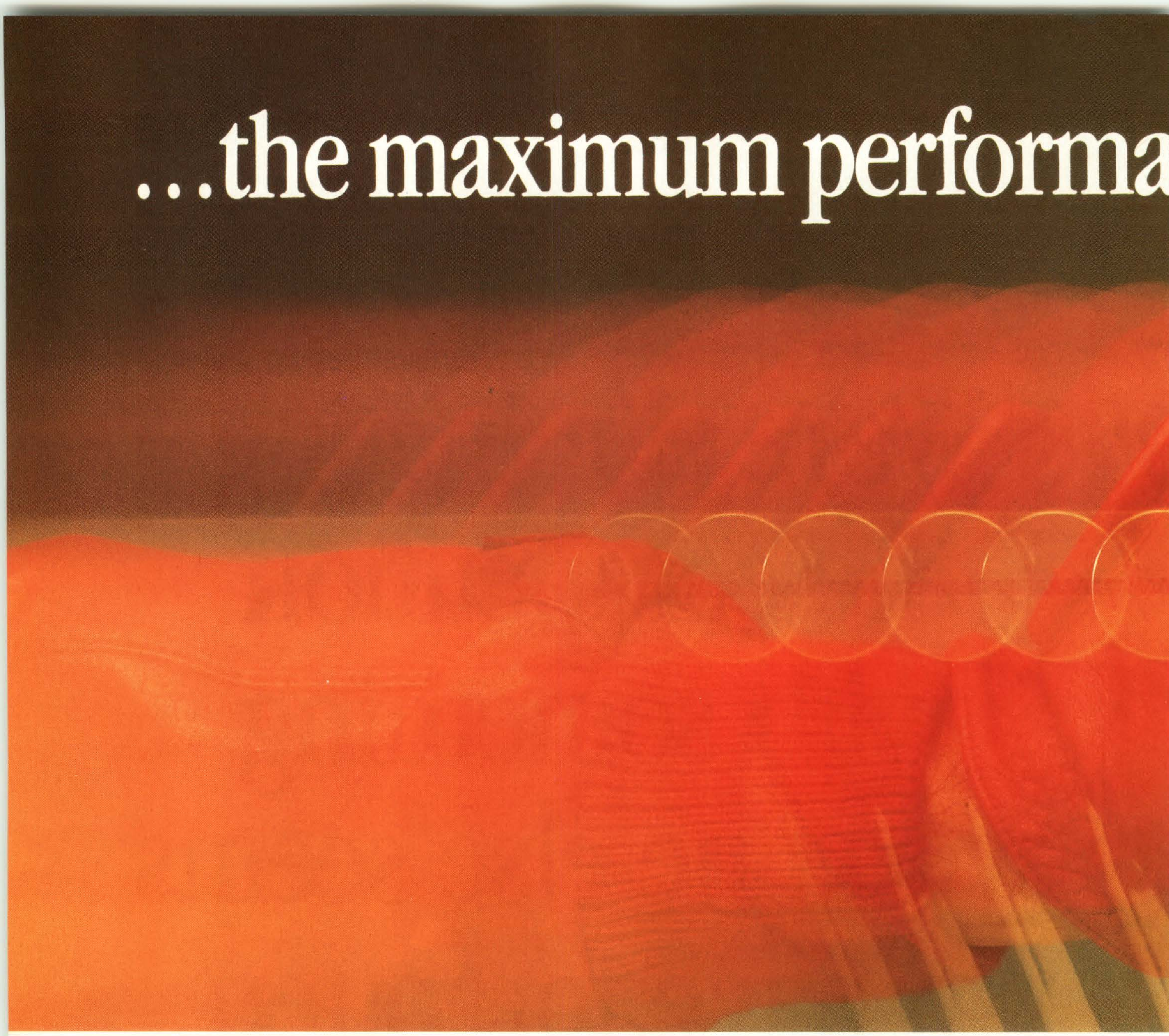
FILTER DESIGN TOOL

PMSS Active Filter Design Tools 2.0 is a low-cost, filter-analysis and -design program that covers the most commonly used filter designs (pg 326).
Power Mountain Software Systems.
Circle No 602



▲ VIDEO OP AMP

The HA-2544 general-purpose op amp is optimized for video and other high-speed signals. The device features a unity-gain bandwidth of 45 MHz and a slew rate of 150V/μsec (pg 269).
Harris Corp.
Circle No 604



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PLESSEY KEY PROCESS TECHNOLOGY

BIPOLAR

DESCRIPTION	Ft	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14μm	1
High voltage	200MHz	20μm	1
High speed linear	4.5GHz	4μm	2
High speed digital	6GHz	3μm	2
Ultra-high speed	14GHz	0.6μm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4μm	3-10V
JG Double SiGate NMOS	10MHz	6μm	9-18V
VB High speed CMOS	40MHz	2μm	3-5V
VJ Very fast CMOS	50MHz	1.5μm	3-5V
VQ Ultra fast CMOS	75MHz	1.2μ	3-5V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5μm				
CDI FAB I	3.75μm	11.5μm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5μm	8μm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5μm	8μm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5μm	6μm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2μm	4.5μm	200ps	0.2pJ	0.14pJ

frequency synthesis, data conversion, telecommunications, data communications and consumer products.

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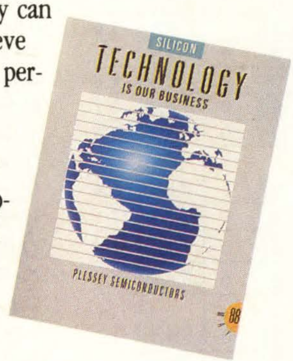

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PLESSEY

Number 1 for ASICs

CIRCLE NO 163

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	33	40	27	0	0	**8.3**	**10.6**
Pot-Core	0	29	50	21	0	0	**8.1**	**10.9**
Laminate (power)	0	26	32	32	5	0	**9.5**	**9.3**
CONNECTORS								
Military panel	0	10	30	50	10	0	**12.9**	**16.0**
Flat/Cable	6	55	22	11	6	0	**6.6**	**5.1**
Multi-pin circular	6	6	41	41	6	0	**11.3**	**9.6**
PC (2-piece)	7	33	33	27	0	0	**7.8**	**8.4**
RF/Coaxial	17	28	38	17	0	0	**6.5**	**8.8**
Socket	19	31	31	19	0	0	**6.3**	**6.4**
Terminal blocks	19	62	15	4	0	0	**3.6**	**4.9**
Edge card	5	38	43	14	0	0	**6.7**	**6.9**
D-Subminiature	23	31	38	8	0	0	**5.2**	**7.2**
Rack & panel	10	20	40	30	0	0	**8.4**	**8.3**
Power	18	18	55	9	0	0	**6.3**	**8.3**
PRINTED CIRCUIT BOARDS								
Single sided	0	53	47	0	0	0	**5.3**	**5.0**
Double sided	0	45	52	3	0	0	**5.9**	**6.2**
Multi-layer	0	22	56	22	0	0	**8.5**	**9.7**
Prototype	4	88	8	0	0	0	**3.2**	**3.5**
RESISTORS								
Carbon film	27	42	24	7	0	0	**4.2**	**6.0**
Carbon composition	27	33	23	27	0	0	**5.4**	**6.9**
Metal film	28	38	24	10	0	0	**4.6**	**6.7**
Metal oxide	31	31	23	15	0	0	**5.0**	**6.8**
Wirewound	7	39	46	4	4	0	**6.4**	**7.7**
Potentiometers	14	38	31	14	3	0	**6.5**	**7.2**
Networks	17	41	25	13	4	0	**6.2**	**6.8**
FUSES	36	36	23	5	0	0	**3.6**	**3.4**
SWITCHES								
Pushbutton	0	57	33	10	0	0	**5.8**	**5.7**
Rotary	5	33	47	10	5	0	**7.5**	**6.6**
Rocker	0	50	44	6	0	0	**5.9**	**6.7**
Thumbwheel	0	30	41	29	0	0	**8.6**	**7.1**
Snap action	0	57	29	14	0	0	**6.2**	**6.7**
Momentary	0	50	42	8	0	0	**6.1**	**5.5**
Dual-in-line	0	50	42	8	0	0	**6.1**	**6.6**
WIRE AND CABLE								
Coaxial	25	46	29	0	0	0	**3.7**	**2.7**
Flat ribbon	25	50	25	0	0	0	**3.5**	**3.0**
Multiconductor	20	60	20	0	0	0	**3.4**	**3.7**
Hookup	44	40	16	0	0	0	**2.4**	**2.8**
Wirewrap	25	37	38	0	0	0	**4.1**	**3.7**
Power cords	17	57	13	13	0	0	**4.7**	**4.5**
POWER SUPPLIES								
Switcher	0	27	40	20	13	0	**10.4**	**8.4**
Linear	7	35	29	29	0	0	**7.8**	**7.2**
CIRCUIT BREAKERS	13	27	40	20	0	0	**7.1**	**7.8**
HEAT SINKS	6	50	33	11	0	0	**5.8**	**5.7**
BATTERIES								
Lithium coin cells	8	58	25	9	0	0	**5.1**	**6.4**
9V alkaline	24	58	12	6	0	0	**3.6**	**4.6**
Real-time clock back-up	0	57	29	0	14	0	**7.6**	**7.2**
RELAYS								
General purpose	27	27	23	23	0	0	**6.2**	**5.7**
PC board	5	33	33	24	5	0	**8.6**	**6.6**
Dry reed	0	41	42	17	0	0	**7.2**	**8.5**
Mercury	0	33	50	17	0	0	**7.6**	**10.6**
Solid state	0	39	33	22	6	0	**8.7**	**7.9**
DISCRETE SEMICONDUCTORS								
Diode	29	29	24	12	6	0	**6.1**	**8.0**
Zener	31	34	13	22	0	0	**5.4**	**8.3**
Thyristor	16	37	21	26	0	0	**6.8**	**8.0**
Small signal transistor	23	27	18	27	5	0	**7.7**	**8.4**
MOSFET	0	44	17	39	0	0	**8.7**	**8.1**
Power, bipolar	5	42	27	26	0	0	**7.4**	**8.0**
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	0	28	39	33	0	0	**9.0**	**9.9**
CMOS	7	27	46	20	0	0	**7.5**	**8.5**
TTL	21	17	45	17	0	0	**6.7**	**8.3**
LS	16	16	52	16	0	0	**7.1**	**6.1**
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	7	29	43	21	0	0	**7.5**	**8.4**
OP amplifier	20	25	40	15	0	0	**6.2**	**6.7**
Voltage regulator	15	37	37	11	0	0	**5.7**	**6.8**
MEMORY CIRCUITS								
DRAM 16K	6	24	12	34	18	6	**13.3**	**18.3**
DRAM 64K	6	29	12	35	12	6	**12.1**	**15.8**
DRAM 256K	0	17	17	38	22	6	**15.2**	**20.0**
DRAM 1M-bit	0	15	0	46	31	8	**17.9**	**20.5**
SRAM 4K × 4	0	14	13	40	20	13	**16.7**	**17.1**
SRAM 8K × 8	0	12	12	34	18	24	**18.6**	**19.6**
SRAM 2K × 8	0	7	33	27	20	13	**16.1**	**18.3**
ROM/PROM	0	21	21	50	0	8	**12.5**	**13.4**
EPROM 64K	0	14	33	38	5	10	**13.3**	**13.6**
EPROM 256K	0	16	5	63	5	11	**15.3**	**14.3**
EPROM 1M-bit	0	9	0	64	0	27	**18.5**	**15.1**
EEPROM 16K	0	9	18	55	0	18	**15.8**	**12.2**
EEPROM 64K	0	8	15	54	0	23	**16.9**	**12.6**
DISPLAYS								
Panel meters	7	14	50	29	0	0	**8.9**	**7.9**
Fluorescent	10	10	20	60	0	0	**11.1**	**11.0**
Incandescent	25	50	0	25	0	0	**5.3**	**7.7**
LED	16	43	22	19	0	0	**5.9**	**6.1**
Liquid crystal	7	27	39	27	0	0	**8.1**	**9.9**
MICROPROCESSOR ICs								
8-bit	0	33	27	33	0	0	**8.2**	**9.8**
16-bit	0	33	25	42	0	0	**9.4**	**10.0**
32-bit	0	10	36	36	18	0	**13.3**	**9.8**
FUNCTION PACKAGES								
Amplifier	13	27	40	20	0	0	**7.1**	**8.3**
Converter, analog to digital	7	8	64	21	0	0	**8.6**	**8.5**
Converter, digital to analog	8	8	61	23	0	0	**8.6**	**9.0**
LINE FILTERS	17	25	41	17	0	0	**6.6**	**8.4**
CAPACITORS								
Ceramic monolithic	13	35	23	29	0	0	**7.3**	**6.1**
Ceramic disc	17	36	17	30	0	0	**7.0**	**6.3**
Film	21	31	28	17	3	0	**6.5**	**6.2**
Aluminum electrolytic	6	35	29	26	4	0	**8.4**	**8.3**
Tantalum	10	28	34	28	0	0	**7.8**	**7.1**
INDUCTORS	0	25	40	35	0	0	**9.3**	**5.8**

Source: Electronics Purchasing Magazine's survey of buyers.

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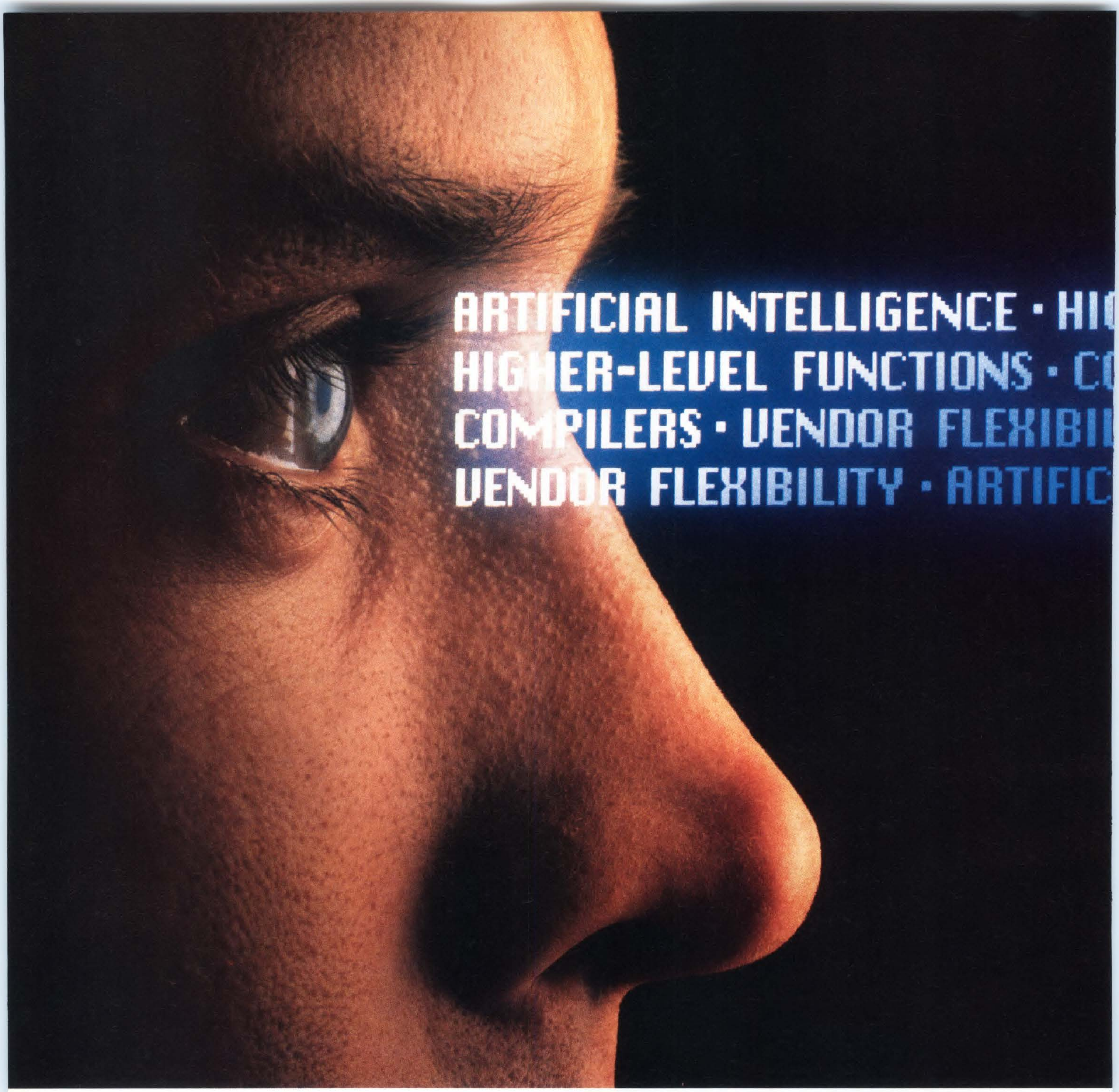

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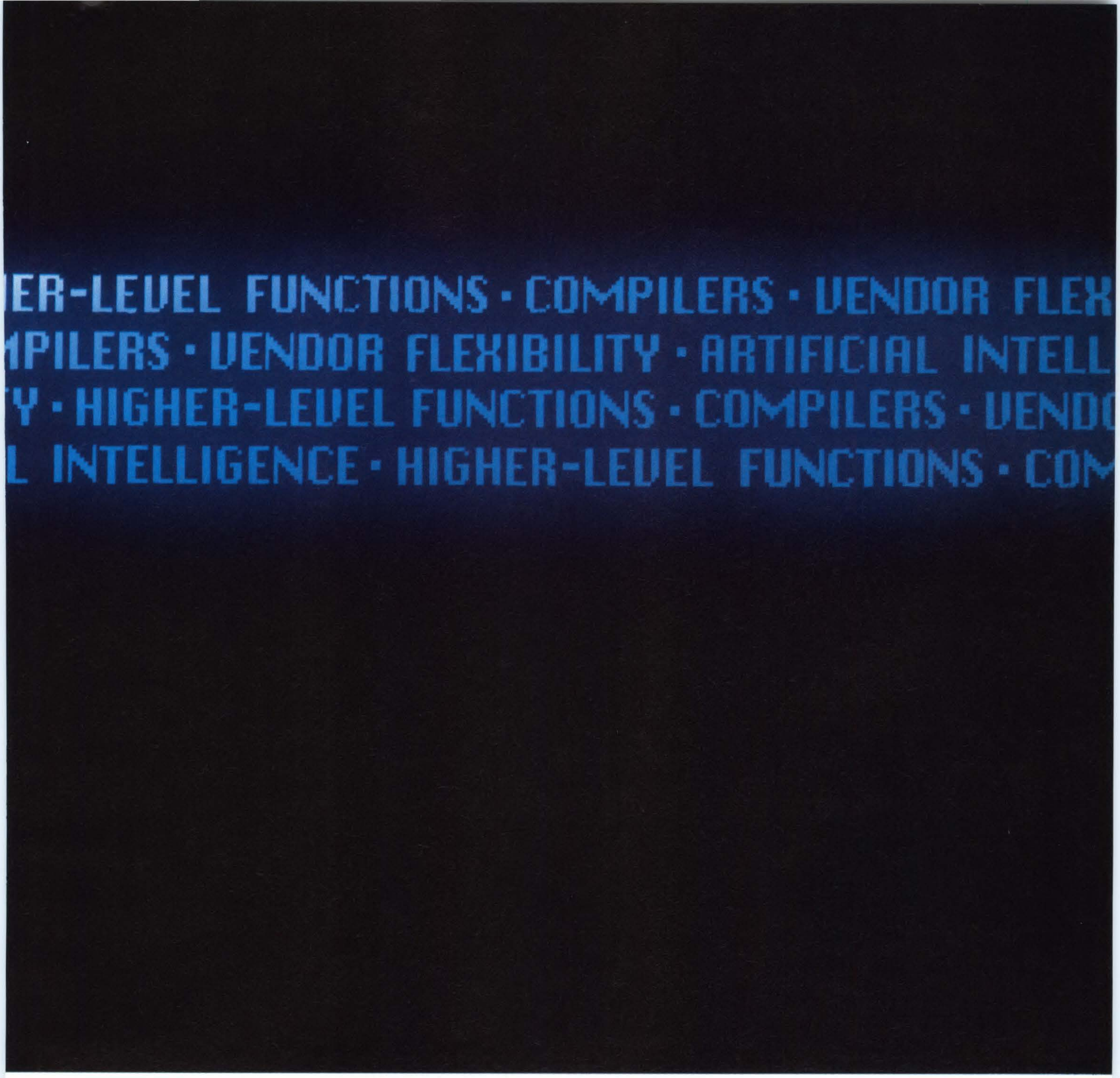

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CIRCLE NO 164

PC-resident analog-I/O cards

Various affordable personal computers make it easy to implement accurate and inexpensive A/D and D/A conversions. The ever-expanding choice of analog-I/O plug-in boards provides compatibility with the IBM-standard PC/XT, PC/AT, and PS/2 Microchannel buses, as well as with the Macintosh II Nubus.

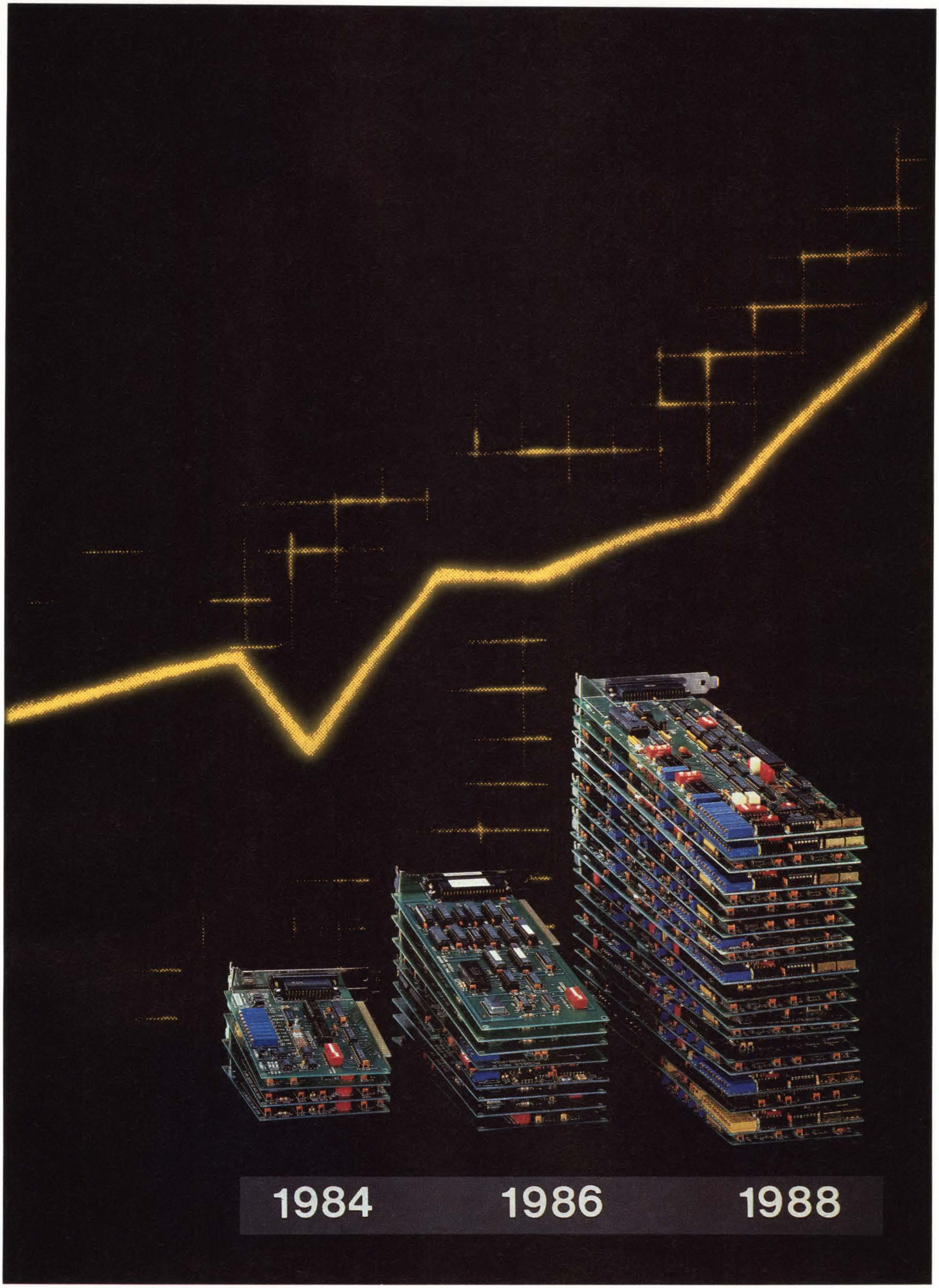
Bill Travis, *Contributing Editor*

If anything underscores the acceptance of personal computers in the engineering workplace, it's the burgeoning list of suppliers of analog-I/O boards for these inexpensive machines. You could count them on one hand only four or five years ago; now these suppliers number more than 35, and the list is growing daily. What's more, the solitary choice of a serious personal computer for analog-I/O purposes—the PC/XT or PC/AT and the clones thereof—has expanded to include the IBM PS/2 Series with its Microchannel Bus and the Macintosh with its Nubus standard.

Manufacturers of analog-I/O cards for personal computers are responding to engineers' acceptance of personal computers in various ways. First, the latest generation of boards intended for the PC/XT and PC/AT buses uses the latest, fastest available A/D converters as well as several architectural innovations to squeeze the maximum sampling speed possible out of this venerable bus. Next, a growing number of board suppliers are devoting all-out efforts to hop on the Microchannel Bus of the PS/2 line. Finally, several manufacturers, recognizing the increasing popularity of the multislot Macintosh II Series, have developed boards that exploit the advantages of the Nubus standard.

When a new standard comes along—for example, the Microchannel Bus and Apple's Nubus—it's a natural tendency to start planning the funeral of the existing standard. According to some experts in the analog-I/O-card industry, however, the death knell of the PC/XT and PC/AT buses is premature. Dick Pleau, product marketing manager at Data Translation Inc (Marlboro, MA) asserts that the PC/XT and PC/AT buses will remain dominant for at least three years, and will still be strong contenders for at least five years. The PS/2 is not without problems, according to Pleau. For example, the unavailability of the OS/2 operating system constrains the Microchannel computers to operate with the older MS-DOS standard. Further, the PS/2 Series likes to use vast amounts of RAM (4M bytes), an expensive commodity these days.

As concerns the Macintosh II with its Nubus standard, Bob Judd, marketing vice president at MetraByte Corp (Taunton, MA), projects that the Macintosh II's market share among engineers will remain minor in comparison with that of the IBM types, and will settle at about 15 to 20% of the total personal-computer market. However, this percentage is still a healthy chunk of a large and growing market, and MetraByte and others are developing products accordingly to fill the Macintosh II niche. This said, it's useful



A steadily increasing inventory *of analog I/O cards is available for your IBM PC family, PS/2, Macintosh II, and compatible computers. (Photo courtesy MetraByte Corp)*

An ever-expanding choice of analog-I/O plug-in boards operates with the PC/XT, PC/AT, PS/2 Microchannel, and Nubus buses.

to examine some recent analog-I/O offerings that exploit the classic PC/XT and PC/AT architectures.

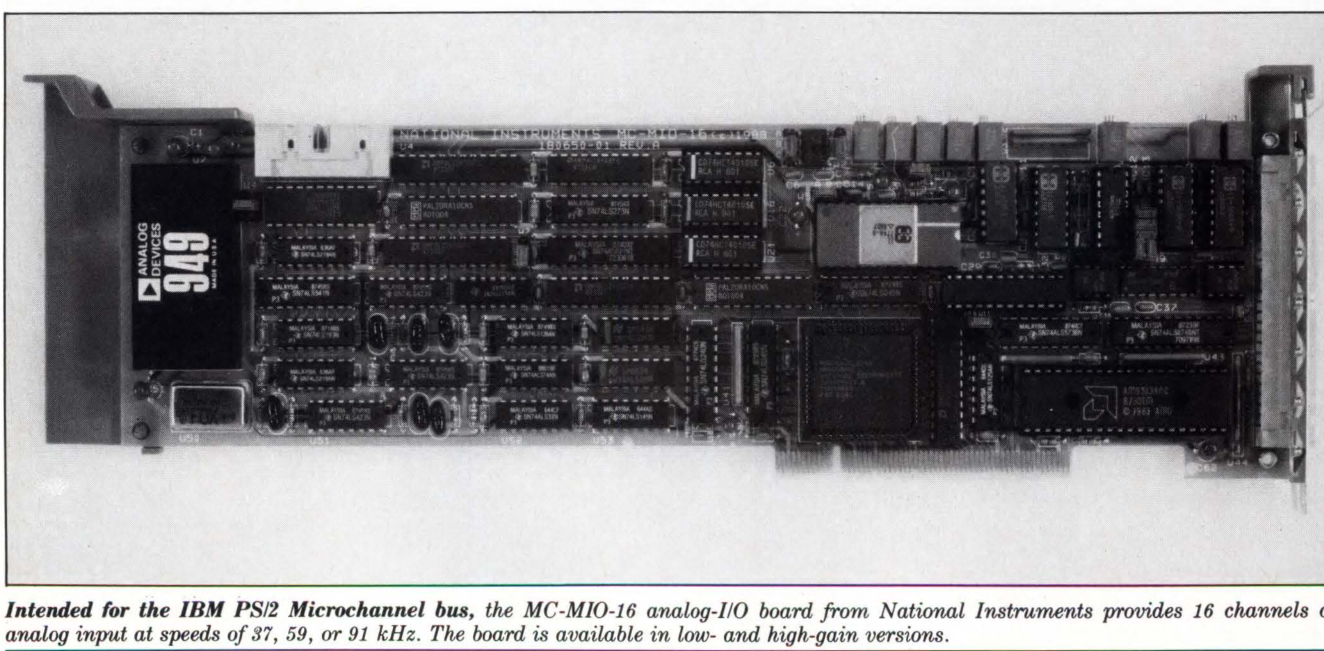
In support of its conviction that the PC/AT bus will enjoy long-term viability, Data Translation has expanded its line of DT2821 Series cards, which operate only with the PC/AT bus. New additions to the family offer enhanced speed, gain, and resolution. For example, the 12-bit, $2995 DT2821-G boosts the speed of the $1995 DT2821-F from 150 to 250 kHz. Both models have 16 single-ended or eight differential (you specify upon purchasing) analog-input channels and two 12-bit, deglitched analog outputs. Both use a dual-DMA architecture that allows full-speed transfer to RAM, and both feature a RAM channel/gain list that allows the user to arbitrarily select gains and channel sequencing.

Another addition to the DT2821 Series accommodates low-level input signals. The 12-bit, 40-kHz DT2825 ($1445) boosts the software-selectable gains of the previous models from 1, 2, 4, and 8 to 1, 10, 100, and 500. The unit can thus process signals as small as ±2 mV full-scale. Designed for such high-resolution applications as audio processing, the 100-kHz DT2823 ($2795) is the only high-speed analog-I/O board on the market that offers analog inputs (four, differential) and outputs (two, deglitched) that spec true 16-bit resolution and linearity. The $2495 DT2827 is identical to the DT2823, but has two 12-bit analog outputs.

Because of the PC/AT bus's bandwidth limitations, the 250-kHz throughput of the DT2821 Series is approximately the upper limit for normal DMA operation. MetraByte gets around this upper limit in its 12-bit, 1-MHz DAS-50 analog-input board by providing onboard data storage of 256k, 512k, or 1M words. Respectively priced at $1999, $2149, and $2449, these PC/XT- and PC/AT-compatible units use 16 consecutive locations in I/O-address space that you can set to start at any base I/O address. The DAS-50, therefore, does not consume any memory-address space and needs no onboard BIOS initialization. You can install the DAS-50 without paying any heed to the I/O addresses used by other peripherals.

Representing an order-of-magnitude leap in speed over its $1495 DAS-20 sibling, the DAS-50 has four single-ended analog inputs (the DAS-20, by contrast, has 16 single-ended or eight differential inputs) and has no analog outputs (the DAS-20 has two 12-bit D/A-converter outputs). Utility software that comes with the DAS-50 provides a pop-up menu that allows users to select the attributes for conversions: number of samples, internal or external clock, sample rate, channels to scan, input range, and trigger and trace modes.

Trigger modes are internal or external (a digital command or an analog-voltage level on an unused channel). An onboard 8-bit D/A converter coupled with a comparator allows users to set the analog trigger levels. The trace modes are "trace-after-trigger," which collects a given number of samples; "trace-before-



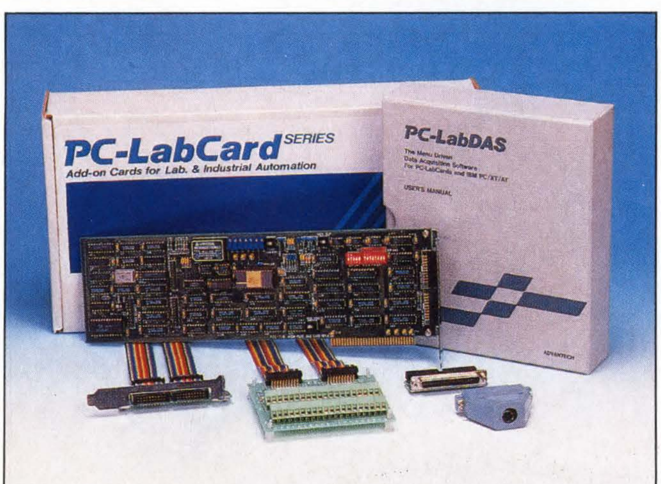
Intended for the IBM PS/2 Microchannel bus, *the MC-MIO-16 analog-I/O board from National Instruments provides 16 channels of analog input at speeds of 37, 59, or 91 kHz. The board is available in low- and high-gain versions.*

trigger," which collects samples until a trigger is received; and "trace-about-trigger," which collects samples until a trigger is received, then continues collecting for a given number of samples thereafter.

Hardware bypasses the PC/AT bus

One way to get around the PC/AT-bus-imposed limit of 250 kHz for data transfers is simply not to use the bus. That's the approach Data Translation adopted for its series of boards that use the DT-Connect hardware bus. These boards have a flat-cable connector along the top. Data ports in this connector provide three independent 16-bit data paths for simultaneous A/D outputs, D/A inputs, and digital-I/O data. In one useful configuration of this hardware-connection system, the company's analog-I/O boards can connect directly to the $6995 DT7020 floating-point array processor.

The analog-I/O boards in the DT-Connect Series comprise the 12-bit DT2841, DT2841-F, and DT2841-G, which spec throughput rates of 40, 150, and 250 kHz, respectively. These boards offer 16 single-ended or eight differential input channels. Model DT2841-L has four differential input channels and a 750-kHz throughput rate. The 16-bit, 100-kHz DT2847 has four differential input channels. Finally, Model DT2848 features a simultaneous sample-and-hold function (with ±5-nsec aperture uncertainty) for its four single-ended input channels. Each of these boards has two independent, 12-bit D/A-converter outputs. Prices range from $1450 to $2995, depending on the version you select.



Low-cost, high-speed 12-bit analog I/O *is available on the PCL-718 board manufactured by American Advantech. The 100-kHz card offers 16 single-ended or eight differential input channels and two analog-output channels.*

A hardware-connect system is not the only way to increase data-collection speed, as you've already seen with MetraByte's DAS-50. Data Translation's 12-bit, $3495 DT2822-L uses an onboard FIFO at its front end to collect 1024 samples while the host CPU (for the PC/AT bus only) takes care of its interrupt, DMA, and disk-control housekeeping chores. The board then transfers data through a pair of buffers in continuous DMA mode. Using this scheme, the DT2822-L can collect data at 750 kHz.

>100-kHz boards abound

Only about three years ago, the throughput of available data-acquisition boards was limited to about 50 kHz. Since then, a number of factors have cooperated

High-end workstations offer advantages in analog-I/O processing. *Intended for Apollo's DN3000 and DN4000 workstations, the hardware and software products produced by SignifiCAT take advantage of the computers' extensive windowing, multitasking, and networking capabilities.*

Architectural innovations such as DMA techniques and onboard acquired-data memory squeeze the maximum sampling speed possible out of the PC/XT and PC/AT buses.

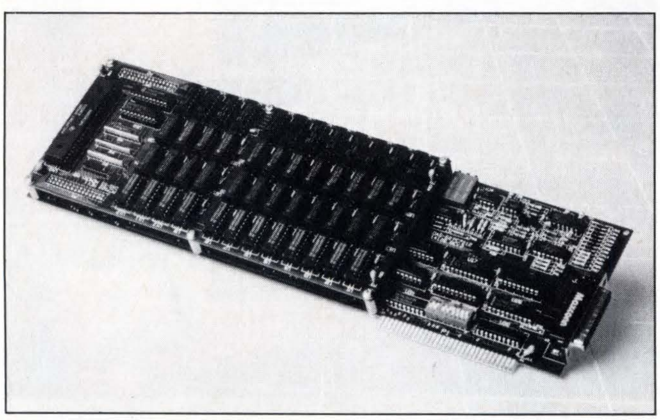
to make boards that acquire at ≥100-kHz rates readily available. One of these factors is the availability of fast, compact 12-bit A/D converters; another is the board makers' adoption of DMA-handling schemes and data-buffering techniques. One A/D converter that's been a boon to producers of analog-I/O boards is the 774 family, which is produced by several monolithic- and hybrid-IC manufacturers. This ADC converts in 8.5 μsec. Given that 10 μsec is the period of a 100-kHz throughput, the 8.5-μsec conversion time leaves an ample 1.5-μsec interval for sample-and-hold settling time and other overhead. Several other 12-bit monolithic and hybrid A/D converters spec conversion times from 5 to 0.5 μsec.

One example of recently introduced ≥100-kHz boards is the $2396 RTI-860 from Analog Devices Inc (Norwood, MA). This 12-bit unit has 16 single-ended analog-input channels. The PC/AT-only board is a dual-resolution device—you can collect either 8 bits of data at 330 kHz max or 12 bits at 250 kHz max. Four simultaneous sample-and-hold channels (with 0.5-nsec typ channel-to-channel aperture uncertainty) allow you to "freeze" the input signals from four channels simultaneously, in applications in which channel-to-channel time relationships are important. The throughput for the simultaneous sample-and-hold function is 62.5 kHz for 8-bit conversions and 50 kHz for 12 bits.

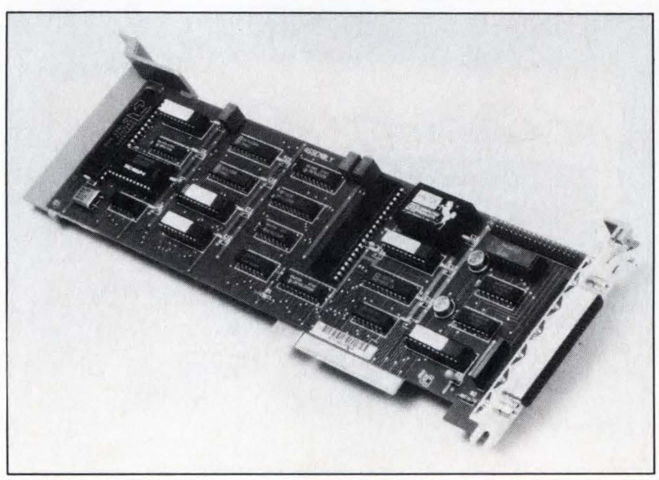
Other features of the RTI-860 include software-programmable random-channel scan, 256k words (of 12 bits) of onboard memory, board-to-system DMA transfer, and a variety of triggering modes. As with MetraByte's DAS-50, you can configure the board to trigger from a digital signal or from a selected analog-input channel. An onboard D/A converter provides the reference for the software-settable analog-input trigger level.

Multiplexing, a sample-and-hold function, and A/D conversion are the main functions of the analog-I/O boards described here. Another important link in the acquisition chain is conditioning the signals fed to the analog-I/O boards. All the board makers offer screw-terminal panels that link the analog signals to the boards, and some offer signal-conditioning blocks (amplifying and filtering, for example). Analog Devices' 5B Series of modular signal conditioners includes gain blocks, thermocouple conditioners, and 4- to 20-mA current-loop circuits. In addition, an analog-output module provides a 4- to 20-mA output for industrial applications. Data Translation also markets Analog Devices' 5B Series as the DT500 Series.

A high-speed modular approach by Burr-Brown's spinoff Intelligent I/O (Tucson, AZ) uses a mother board that accepts a variety of modules: analog-input, analog-output, digital-I/O, simultaneous sample-and-hold, and counter-timer cards, for example. The $695 IQ-141C-3A mother board has 32 points of digital I/O and accepts as many as three modules that communicate with each other via an I^3 bus. A DMA technique allows the mother board to transfer data to and from system memory at rates as high as 360 kHz. As an example of the acquisition rates this modular approach can attain, the $895 IQ-123M-1 provides eight channels



***An order-of-magnitude leap in speed** is the hallmark of MetraByte's DAS-50 analog-input board. The 1-MHz board is 10 times faster than its older sibling, the DAS-20. The board has four 12-bit analog inputs, and it comes with easy-to-use, pop-up software.*



***Choose the resolution that suits your needs—12, 14, or 16 bits,** from the MC-DAS 1612/1614/1616 Series of Microchannel-compatible analog-I/O boards from Scientific Solutions. The 16-channel cards offer programmable gain at the inputs and one 12-bit analog output.*

of 12-bit acquisition at rates as high as 180 kHz.

Another high-speed analog-I/O board has an onboard 80186 microprocessor that imparts intelligence to the data-acquisition process. Model DAP 1200 from Microstar Laboratories Inc (Redmond, WA) is available in 50- and 150-kHz versions that offer either 128k or 512k words of onboard RAM. Their prices range from \$995 to \$1995. The 12-bit PC/XT-PC/AT board provides 16 channels of analog input and two channels of analog output. The onboard software utilities include averaging, peak extraction, sensor linearization, and FFT routines, to name a few. The company's \$200 Advanced Development Toolkit provides software tools for creating custom commands for the card.

Not new, but still significant for its capabilities and price, is a 12-bit analog-input board from Micro Way (Kingston, MA). The \$995 A2D-160 is a 2-channel card that uses DMA techniques to transfer data to and from system memory. The board accommodates the Intel/Lotus Expanded Memory Standard (EMS). Its throughput rate is 166 kHz in single-channel mode, 65 kHz in 2-channel mode. Note that, in 2-channel mode, the A2D-160 provides a simultaneous sample-and-hold function for the two analog signals.

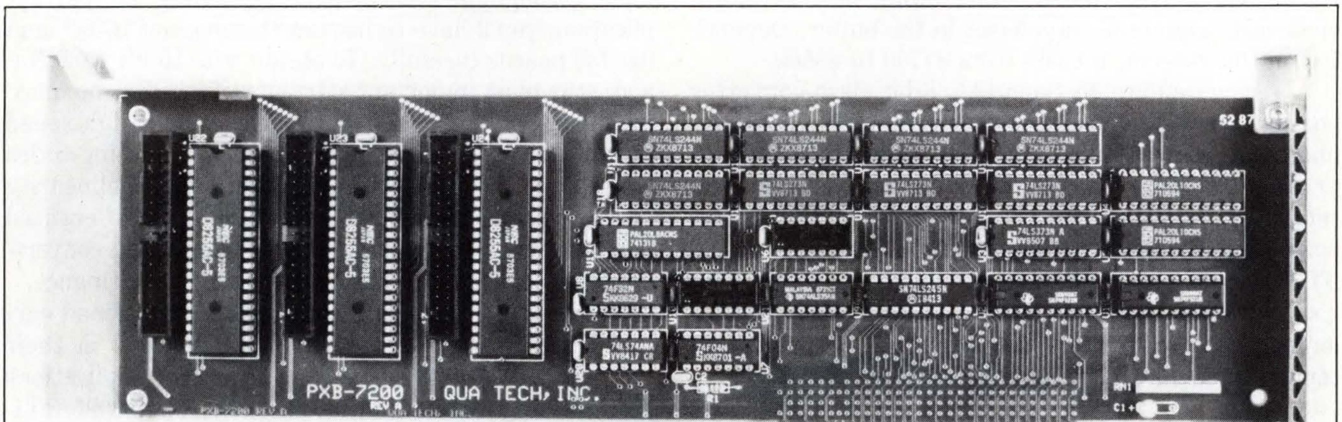
A unique feature of the A2D-160 is its onboard pseudorandom white-noise generator—by using this utility, you can measure the impulse response of a system without having to apply an actual impulse to the system. Further, the board accommodates one or two \$225 AFM-50 programmable lowpass filters (one per channel). This 4-pole antialiasing filter is programmable for Q, pole frequencies, and gain. Its cutoff frequencies range from 500 Hz to 30 kHz.

A final example of ≥100-kHz, 12-bit analog-I/O boards is notable for its price. The \$895 PCL-718 Option 001 board from American Advantech Corp (San Jose, CA) has 16 single-ended or eight differential inputs, and two analog outputs. The PC/XT-PC/AT board uses DMA techniques to provide 100-kHz throughput.

Lower resolution, higher speed

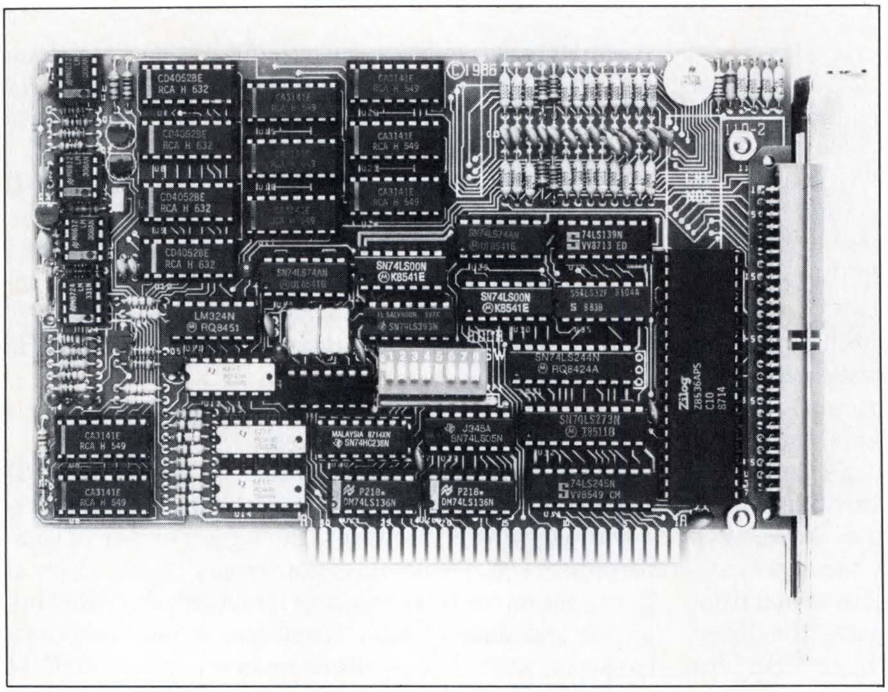
To obtain extremely high speeds (>10 MHz) in A/D conversion, the technique of choice is flash, or simultaneous, conversion. However, the large number of comparators required for flash conversion (2^n-1, where n is resolution in bits) restricts practical embodiments of this technique to 8-bit resolution. A few companies have put such flash converters in the front ends of their PC/XT- and PC/AT-compatible analog-I/O boards.

One example is Markenrich Corp (Duarte, CA). Its WAAG II data-acquisition and arbitrary-waveform-generator board provides simultaneous data acquisition for two channels at 20-MHz throughput for each channel. The \$1395 board provides a 16k-byte (to 64k-byte, optional) memory for each input channel. Its 40-MHz front-end bandwidth eliminates any acquisition and



Using onboard memory to provide high speed, *the Microchannel-compatible System 12000 boards from Qua Tech acquires data at 1 MHz. The memory accommodates 256k words of acquired-data storage; a DMA scheme allows the board to operate independently of the host computer.*

The Macintosh II and its Nubus slots are gaining daily in popularity for performing engineering chores.



***An integrating A/D converter at its front end** gives 16-bit resolution to the Mini-16 analog-input board from Strawberry Tree. The card offers eight programmable-gain differential input channels. You can alternatively configure the board in autranging mode.*

phasing errors. An arbitrary-waveform generator allows you to create waveforms interactively or via a disk file. The waveforms can contain as many as 32k points (or, optionally, 64k points).

Another 8-bit specialist is Sonotek (Springfield, VA). The firm's 25-MHz STR*825 is an analog-input board for the PC/XT and PC/AT buses that comes in 1- or 2-channel versions and contains data buffers that store 16k to 64k words; you can store either one waveform or several sequential waveforms in the buffer. Depending on the version, it costs from $1750 to $3500.

A recent update to Sonotek's 8-bit flash-converter boards, the $2100 STR*832, has a 32-MHz base sampling rate (it can sample 32-MHz transients). An upgrade in the near future will equip the board to take samples at an equivalent rate of 256 MHz. The fastest analog-input board in the industry is Sonotek's $3850 STR*1000. It's a true 100-MHz transient recorder that has 50-MHz analog-input bandwidth, 400-MHz equivalent-time sampling, and programmable gain and attenuation of the analog signal.

16-bit resolution—how much linearity?

Many applications call for resolution finer than the one part in 4096 offered by 12-bit A/D conversion. Such applications include audio processing and signals in medical monitoring equipment. With their theoretical resolution of one part in 65,536, 16-bit converters satisfy the majority of these requirements. Analog-I/O-board suppliers use two types of converters in their high-resolution boards: successive-approximation-register (SAR) converters and integrating converters.

SAR devices are fast converters; they allow you to design analog-input boards that spec throughput rates of 10 kHz or higher. The integrating units take several milliseconds to convert; they therefore restrict analog-input throughput accordingly. Depending on your application, you'll have to inspect the specs of 16-bit analog-I/O boards carefully. To obtain true 16-bit performance (the most important attribute of which is no missing codes out of the 65,536 possible) from a high-speed (SAR) configuration, look for either a no-missing-codes guarantee, a ±0.0015% max differential-nonlinearity spec, or a spec that ensures ±1-LSB max differential nonlinearity. Note that the slower integrating converters inherently ensure no-missing-codes performance.

The 16-bit high-speed (SAR) boards (described earlier) from Data Translation are unequivocal in their guarantee of true 16-bit performance. For applications that can accommodate 14-bit linearity, The $2095 RTI-850 analog-input board from Analog Devices is a 50-kHz, 16-bit-resolution unit that has many of the features of the RTI-860, described in the section on ≥100-kHz boards. The PC/AT-only unit has eight differential analog-input channels, 256k words of onboard memory, and a software-programmable random channel scan.

Manufacturers of PC-resident analog-I/O cards

For more information on analog-I/O plug-in boards for personal computers, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

ADAC Corp
70 Tower Office Park
Woburn, MA 01801
(617) 935-6668
Circle No 650

American Advantech Corp
1460 Tully Rd, Suite 602
San Jose, CA 95122
(408) 293-6786
Circle No 651

Analog Devices Inc
Two Technology Way
Norwood, MA 02062
(617) 329-4700
Circle No 652

Ariel Corp
110 Greene St, Suite 404
New York, NY 10012
(212) 925-4155
Circle No 653

Burr-Brown Inc
Box 11400
Tucson, AZ 85734
(602) 746-1111
Circle No 654

Canetics Inc
Box 70549
Pasadena, CA 91107
(818) 584-0438
Circle No 655

CGRS Microtech
Box 102
Langhorne, PA 19047
(215) 757-0284
Circle No 656

Contec USA Inc
3000 Scott Blvd, Suite 211
Santa Clara, CA 95054
(408) 727-1497
Circle No 657

DAISI Electronics Inc
Box K
Newtown Square, PA 19073
(215) 353-2203
Circle No 658

Dalanco Spry
2900 Connecticut Ave NW
Washington, DC 20008
(202) 232-7999
Circle No 659

Data Translation Inc**
100 Locke Dr
Marlboro, MA 01752
(508) 481-3700
Circle No 660

El Toro Systems
22865 Lake Forest Dr
El Toro, CA 92630
(714) 770-1474
Circle No 661

Galiso Inc
4920 LaPalma Ave
Anaheim, CA 92807
(714) 779-8008
Circle No 662

General Research Corp
7655 Old Springhouse Rd
McLean, VA 22102
(703) 893-5900
Circle No 663

GW Instruments Inc*
264 Monsignor O'Brien Hwy
Cambridge, MA 02141
(617) 625-4096
Circle No 664

Hi Pointe Instruments Inc
5050 Oakland Ave
St Louis, MO 63110
(314) 534-7960
Circle No 665

Industrial Computer Designs
31264 LaBaya Dr
Westlake Village, CA 91362
(818) 889-3179
Circle No 666

Integrated Systems Products
6028 Fremont Circle
Camarillo, CA 93010
(805) 987-5125
Circle No 667

Intelligent I/O
1141 W Grant Rd No 131
Tucson, AZ 85705
(602) 629-9872
Circle No 668

Interactive Microware Inc
Box 139
State College, PA 16804
(814) 238-8294
Circle No 669

John Bell Engineering
400 Oxford Way
Belmont, CA 94002
(415) 592-8411
Circle No 670

Lawson Labs
5700 Raibe Rd
Columbia Falls, MT 59912
(406) 387-5355
Circle No 671

Markenrich Corp
14946A Shoemaker Ave
Santa Fe Springs, CA 90670
(213) 921-0250
Circle No 672

Mesa Electronics
1329D 61st St
Emeryville, CA 94608
(415) 547-0837
Circle No 673

MetraByte Corp**
440 Myles Standish Blvd
Taunton, MA 02780
(617) 880-3000
Circle No 674

Microstar Laboratories
2863 152nd Ave NE
Redmond, WA 98052
(206) 881-4286
Circle No 675

MicroWay
Box 79
Kingston, MA 02364
(617) 746-7341
Circle No 676

National Instruments Corp**
12109 Technology Blvd
Austin, TX 78727
(512) 250-9119
Circle No 677

Qua Tech Inc
478 E Exchange St
Akron, OH 44304
(216) 434-3154
Circle No 678

RC Electronics
5386D Hollister Ave
Santa Barbara, CA 93111
(805) 964-6708
Circle No 679

Real Time Devices
Box 906
State College, PA 16804
(814) 234-8087
Circle No 680

Robotrol
16100 Caputo Dr
Morgan Hill, CA 95037
(408) 778-0400
Circle No 681

Scientific Solutions Inc**
6225 Cochran Rd
Solon, OH 44139
(216) 349-4030
Circle No 682

Sealevel Systems Inc
Box 1808
Easley, SC 29641
(803) 855-1581
Circle No 683

SignifiCAT Associates Inc
21 Main St
Hudson, MA 01749
(508) 562-7363
Circle No 684

Sonotek
Box 1812
Springfield, VA 22151
(703) 440-0222
Circle No 685

Starbuck Data Co
9 Smith St
Wellesley, MA 02181
(617) 237-7695
Circle No 686

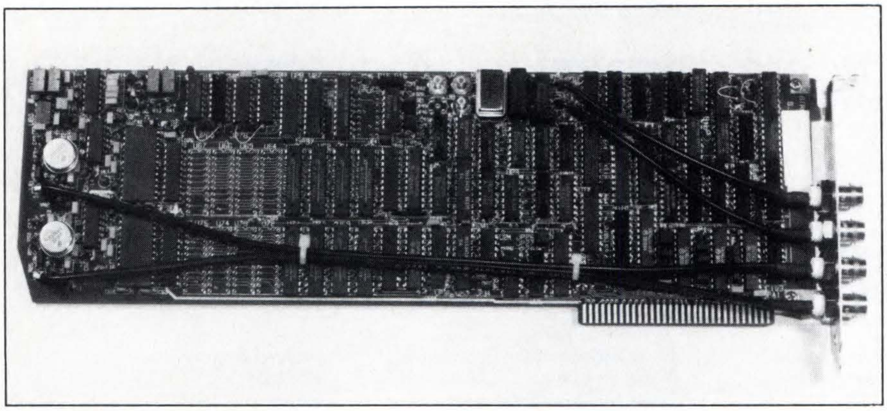
Strawberry Tree Computers**
160 S Wolfe Rd
Sunnyvale, CA 94086
(408) 736-3083
Circle No 687

Vacumed
2261 Palma Dr
Ventura, CA 93003
(805) 644-7461
Circle No 688

*** Vendors of Macintosh II boards**
**** Vendors of PC/XT, PC/AT, Microchannel, and Macintosh II boards**

A piggyback approach adopted by Hi Pointe Instruments Inc (St Louis, MO) uses the $900 HPI-31 I/O processor, a PC/XT-and PC/AT-compatible mother board that accommodates A/D and D/A modules. The 16-bit, $900 HPI-7600 A/D module has 16 single-ended or eight differential analog-input channels. Its differential-nonlinearity spec of ±0.005% max guarantees no missing codes to a resolution of 14 bits. The throughput rate is 50 kHz. A companion 16-bit D/A-converter module, the $450 HPI-7200, guarantees monotonicity (over

Flash A/D converters in the front end of an analog-input board provide transient-waveform sampling rates as high as 100 MHz, with a resolution of 8 bits.



Coaxial-cable RF techniques are necessary for 25-MHz sampling. *The 25-MHz STR*825 8-bit analog-input board from Sonotek offers 16k to 64k words of acquired-data memory for each of two channels; you can store either one waveform or several sequential waveforms in the memory.*

temperature) to 14 bits of resolution.

A final example of an SAR-type 16-bit analog-input board is the $495 Model 134 from Lawson Labs Inc (Columbia Falls, MT). This PC/XT- and PC/AT-compatible unit guarantees no missing codes to 16 bits, has four differential analog-input channels, and specs 12-kHz throughput. Lawson takes an entirely different approach in its $265 Model 140 15-bit analog-input board. This card is a 4-differential-input integrating unit that performs 7.5 conversions/sec.

Another recent integrating-type, high-resolution analog-input board is available from Strawberry Tree Computers (Sunnyvale, CA). The $995 Mini-16 has eight differential analog-input channels and 12 digital-I/O lines. It features six software-selectable full-scale ranges from 50 mV to 10V; you can alternatively use it in autoranging mode. The Mini-16 performs 2500 conversions/sec.

Specialty analog-I/O cards

The boards described so far are basic analog-I/O cards that incorporate various bells and whistles to improve their ease of use, communications with the host processor and memory, and performance parameters. A few specialty boards on the market go further in providing useful engineering tools. Two systems from Ariel Corp (New York, NY) and Dalanco Spry (Washington, DC), for example, incorporate Texas Instruments' TMS320C25 and Motorola's DSP56001 DSP chips to add signal-processing power to the data-acquisition function.

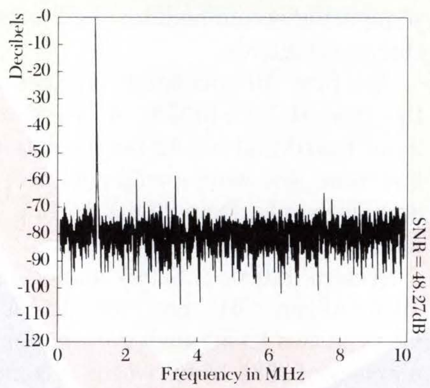
Model DSP-C25 from Ariel uses the TI chip to provide 10-MIPS signal-processing speed. It accommodates as much as 256k bytes of zero-wait-state RAM and works with TI's low-cost ASM-320 DSP assembler. Model PC-56 uses the Motorola chip to provide 10.25-MIPS signal-processing speed. This board accommodates as much as 192k bytes of zero-wait-state RAM, as well as Motorola's assembler and simulator for the DSP56001. Both boards have sockets for TI's TLC32040 analog-interface IC, a device that provides 14-bit (10-bit linear) analog input and output at sampling rates to 19.2 kHz. Both boards cost $595.

Another specialized DSP board that incorporates analog input and output is the PC/XT- and PC/AT-compatible Model 25 board from Dalanco Spry. This unit also incorporates TI's 10-MIPS TMS320C25 and carries 8k bytes of zero-wait-state RAM. The built-in A/D converter and D/A converter provide 110-kHz conversion rate. In a typical performance benchmark, the Model 25 can perform a 1024-point complex FFT in 30 msec.

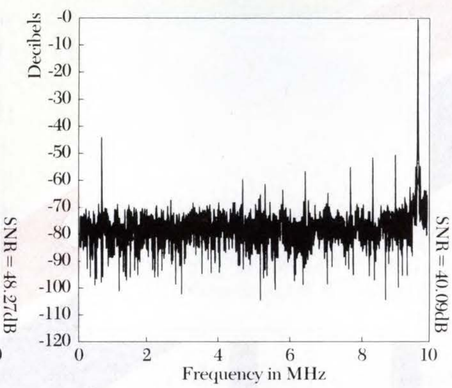
One class of specialty boards turns your PC/XT, PC/AT, or clone into an instrument. The $2495 IS-16 board from RC Electronics Inc (Santa Barbara, CA), for example, configures your computer as a 16-channel, 12-bit, 1-MHz digital oscilloscope. It works with the CGA or EGA, and takes samples consisting of 64 to 64M points. Its double-buffer memory arrangement transfers data into PC/AT RAM at 250 kHz, or onto a hard disk at 70 kHz (hard-disk-transfer software is optional). The board contains a coprocessor for signal processing; specialized DSP software is available from RC. Also available is the $1395 RC-216 16-bit arbitrary-waveform generator, as well as several other specialized peripherals.

A final example of a specialized analog-I/O card is the $3208 ADALAB-PC interface board from Interactive Microware Inc (State College, PA). This card incorporates a 12-bit, 30-Hz integrating A/D converter (a 20-kHz, SAR-type converter is optional) and a 12-bit D/A converter. The system comes with software and hardware that facilitates interfacing with any instruments that have recorder outputs, and with any de-

THE THRILL OF DESIGNING A/D SUPPORT CIRCUITRY ENDS IN A FLASH.



FFT of HS1068 Flash Converter,
Fin = 1.123MHz, Fsample = 20MHz



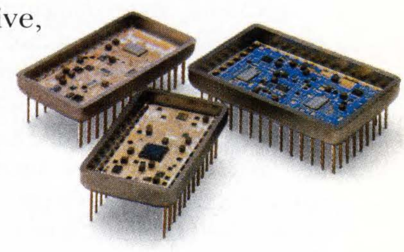
FFT of HS1068 Flash Converter,
Fin = 9.678MHz, Fsample = 20MHz

The thrill of designing voltage references, input buffers, timing, and adjustment circuitry is gone. We do it for you. And in hybrid packages smaller than you'd expect for flash converters alone.

Consider these three "pop-in" converters. Our 8-bit HS1068 flash A/D samples at 20MHz minimum, has no spurious or missing codes, aperture jitter of only 60ps, and true 1/2 LSB 8-bit 47dB signal-to-noise ratio. Our 8-bit SP1070 samples at 25MHz minimum and requires only 1W of power. And our dual-flash SP1072 provides the performance of two SP1070s while saving you considerable real estate.

Naturally, we test each device to ensure maintenance of SNR as input frequencies climb. They'll be distortion-free in your hypersensitive DSP applications.

And, we are the only company you can rely on to deliver full MIL-STD-1772 and MIL-STD-883C, self-contained, hybrid flash converters off the shelf. For data sheets, or a copy of our 382-page 1988 catalog, write SIPEX Corporation, Six Fortune Drive, Billerica, MA 01821, or call 1-800-272-1772. In Massachusetts call (617) 663-7811.

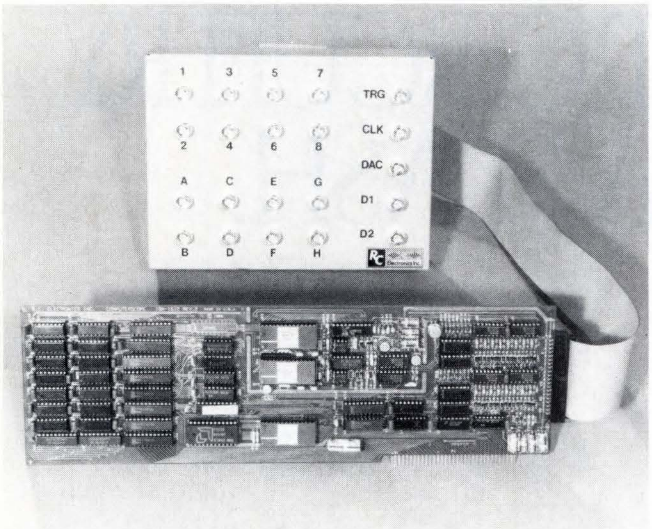


Sipex Corporation Hybrid Systems Division

SIGNAL PROCESSING EXCELLENCE

CIRCLE NO 166

Inspect the specs of 16-bit analog-I/O boards carefully—several boards offer 16-bit resolution, but only 14-bit linearity.



***This virtual oscilloscope on a card**—the IS-16 data-acquisition board from RC Electronics—provides a complete front-end sampling capability. The unit turns your PC/XT or PC/AT into a 16-channel, 12-bit, 1-MHz sampling oscilloscope. It takes samples that contain 64 to 64M points.*

vices that are controlled by a voltage. In short, the system is useful for plotting, control, analysis, and measurement functions.

Migrating to Microchannel

Big Blue's new PS/2 line of personal computers has its proponents and its opponents. The proponents' view is that the Microchannel Bus of Models 50, 60, and 80 and the yet-to-be-released OS/2 operating system will give the personal-computer world dazzling new multitasking, multiuser, multi-everything capabilities. The opponents' view is that IBM should have left well enough alone, and a cynical faction posits that the only reason for the Microchannel's development was to exclude competition from the market.

Whatever the rationale behind—and the merits of—the Microchannel line of PCs, the fact is that they're here now, and they're growing in popularity. This popularity will certainly grow even more once the clone makers (for example, Tandy and Dell) swing into large-scale production. (Clone makers must pay IBM royalties for the use of the Microchannel architecture—something they didn't have to do with the open-architecture PC/XT and PC/AT.) Several manufacturers of analog-I/O boards, having seen the writing on the wall, have developed products for the Microchannel line of PCs.

Two new products signal Data Translation's entry into the Microchannel market. The $995 DT2901 is a 12-bit analog-I/O board that has 16 single-ended or eight differential inputs. It has software-selectable gains of 1, 2, 4, 8, or 16. The $995 DT2905 is similar, but is intended for low-level-signal applications; its software-selectable gains are 1, 100, 500, and 1000. In addition, a jumper on the DT2905 provides gain doubling to allow gains of 2, 20, and 200. Note that the DT2905 has an input configuration of eight differential channels. Both boards have 50-kHz throughput and two 12-bit D/A outputs. RAM-based channel and gain sequencing accommodates high-speed sampling for any channel sequence.

The first Microchannel product from MetraByte is the $650 μCDAS-8PGA, an 8-differential-input analog-input board that has 12-bit resolution. The 5-kHz board has nine software-programmable input ranges: in unipolar mode, from 20 mV to 10V full-scale; in bipolar mode, from ± 10 mV to ± 10V.

System 12000, a $2995 analog-I/O board from Qua Tech (Akron, OH), has eight 12-bit analog-input channels and two 12-bit analog-output channels. Its onboard memory of 256k 16-bit words accommodates a sampling rate of 1 MHz. A DMA scheme allows the System 12000 board to operate independently of the host computer. The board features pre- and post-triggering, programmable gains, and 8255-controlled digital I/O. Available for the PC/AT bus now, the board will come in a Microchannel version in November.

The MC-MIO-16 Microchannel-compatible board from National Instruments (Austin, TX) provides 12-bit analog inputs and outputs. The board has 16 single-ended or eight differential inputs and two analog outputs. A jumper selects unipolar or bipolar input ranges; a software-programmable amplifier provides gains of 1, 2, 4, or 8 for high-level signals (Model MC-MIO-16H) or 1, 10, 100, or 500 for low-level signals (Model MC-MIO-16L). Three speed versions of the board provide worst-case throughputs of 37, 59, and 91 kHz. Prices range from $1195 to $1495.

The final example of Microchannel-compatible analog-I/O boards is the MC-DAS 1612/1614/1616 Series from Scientific Solutions Inc (Solon, OH). These boards are 12-, 14-, and 16-bit units, respectively. They have 16 single-ended or eight differential inputs and one 12-bit D/A output. A software-programmable input amplifier provides gains of 1, 2, 100, or 500. In order of increasing resolution, the throughput rates of the three versions are 80, 40, and 40 kHz. For all three versions, an unequivocal full-temperature spec of

"Their new 030 board isn't really a single-board computer.

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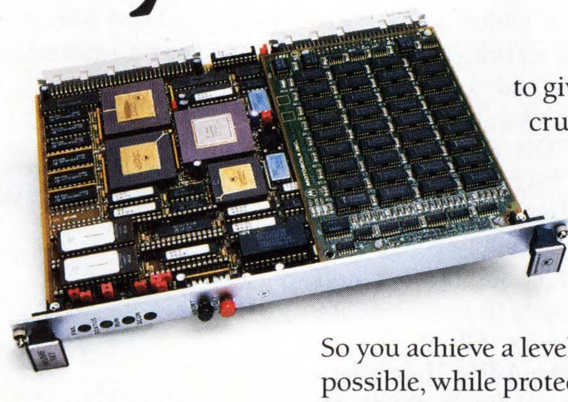

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Attacking the Mac

The Macintosh II's open architecture, crisp graphics, and friendly interface are endearing the machine to a growing number of engineers. The six beckoning Nubus expansion slots have spurred several manufacturers of analog-I/O boards to develop products in a hurry. (For a discussion of the available analog-I/O products for the Macintosh II, see "Vendors offer a range of data-acquisition and -control boards for the Macintosh II," EDN, March 3, 1988, pg 57.)

Data Translation has added several new Macintosh II products to its line. A higher-speed version of the initial DT2221-F—the $2995 DT2221-G—brings the throughput from 150 to 250 kHz. An even higher-speed version, the $3495 DT2221-L, boasts 750-kHz throughput. In addition, the company has added a low-cost, 50-kHz family to its portfolio. The DT2211 is a 12-bit analog-I/O board that has 16 single-ended or eight differential inputs and two D/A outputs. The high-level (0.625 to 5V full-scale) DT2211-PGH costs $795; the low-level (10 mV to 5V full-scale) PGL costs $895.

Also new is a product from GW Instruments (Cambridge, MA). The MacAdios II Jr (no family connection with the IBM PC Jr—shudder) fills out the low end of the MacAdios line—it has no sockets to accommodate extra A/D converters, D/A converters, filters, or analog-input multiplexers. The $800 MacAdios II Jr offers 16 single-ended or eight differential input channels, eight digital-I/O lines, and three counter/timer channels, and it acquires data at 20 kHz.

Another low-level (20 mV to 10V full-scale) unit from Data Translation is the 12-bit DT2225, which has 40-kHz throughput and costs $1695. The DT2228 is a 12-bit unit that has a simultaneous sample-and-hold function on its four single-ended inputs; it specs 100-kHz throughput and costs $2495. Finally, the company has added 16 bits to its Macintosh II capabilities. The $2495 DT2227 has four differential, 16-bit inputs and two 12-bit D/A outputs. Its throughput rate is 100 kHz.

Finally, note that data acquisition for engineering workstations has not gone neglected. A specialist in this field, SignifiCAT Inc (Hudson, MA), offers analog-I/O hardware and software especially tailored for Apollo's DN3000 and DN4000 workstations. Dr E G Merrill, president of SignifiCAT, has strong convictions about the advantages of doing analog-signal acquisition and processing on full-powered workstations.

In Dr Merrill's opinion, Apollo leads the pack in networking, operating system, PC compatibility (the AT bus), graphics, software-development support, dynamic windowing, and third-party support. As he puts it, "Microsoft Windows on a PC is to workstation graphics as your grandma's homemade wine is to Lafite Rothschild."

The $2995 RTS-100 data-acquisition card from SignifiCAT carries an 80186 processor, 32k bytes of command ROM, and 128k bytes of RAM. The 250-kHz board has eight single-ended inputs. The company offers a comprehensive software package for developing data-acquisition and -analysis applications on Apollo DN3000 and DN4000 workstations. The $12,000 package includes extensive graphics support for programming in high-level languages. Another software package, the $800/node ILS Interface, allows the RTS-100 to acquire and format data files for analysis by Signal Technology's Interactive Laboratory System (ILS). EDN

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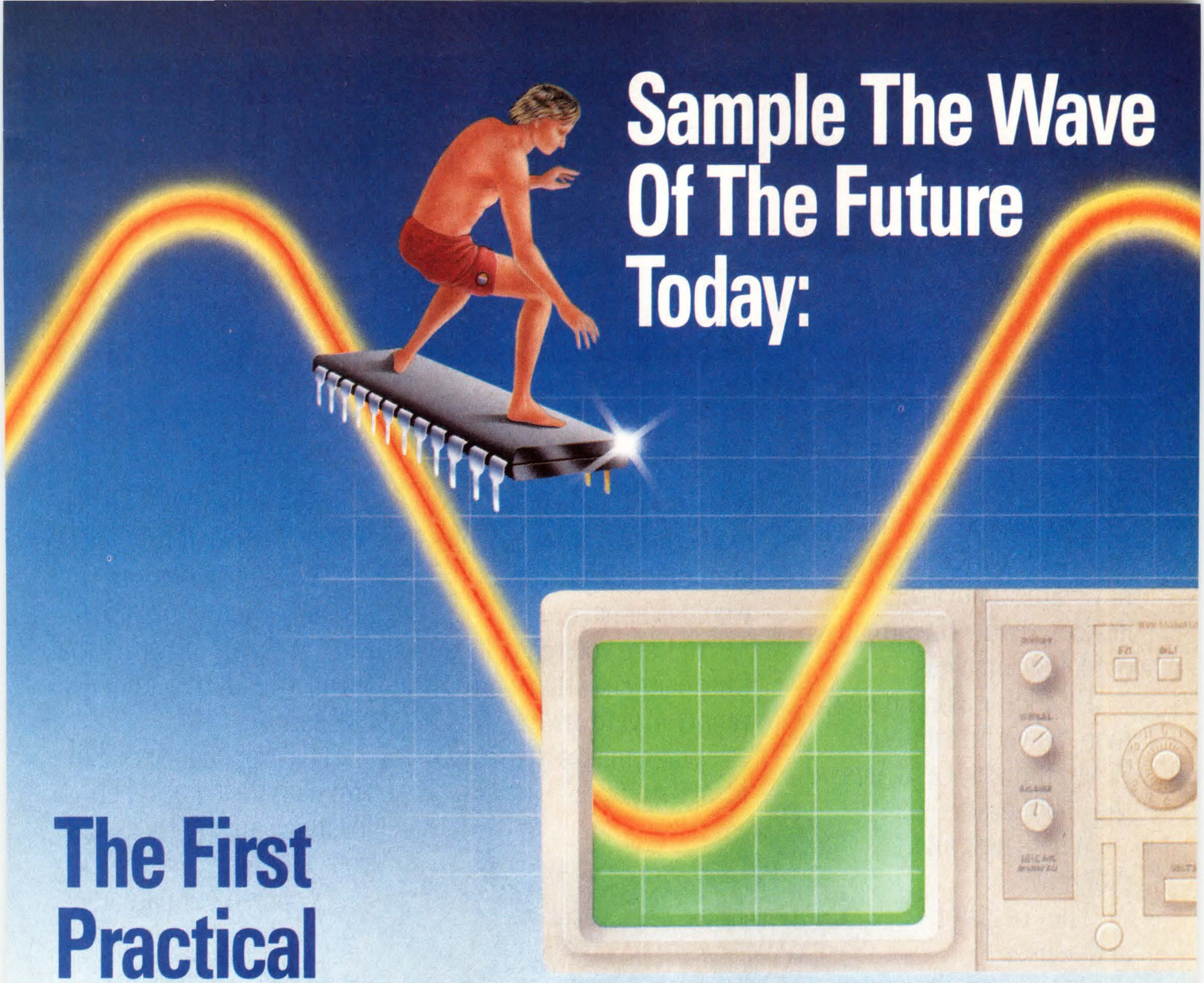

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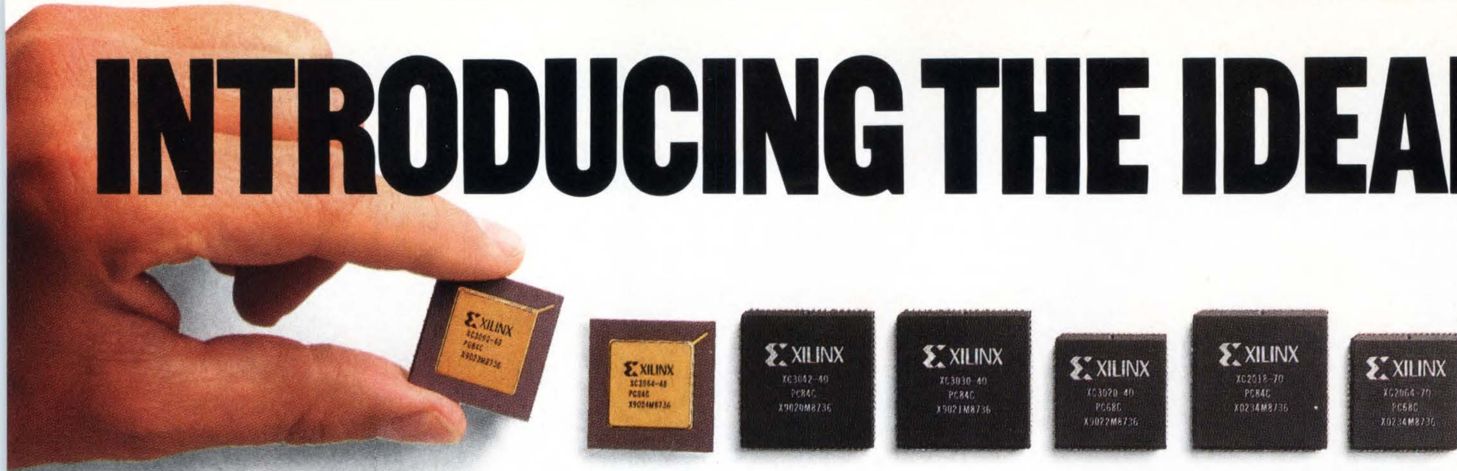

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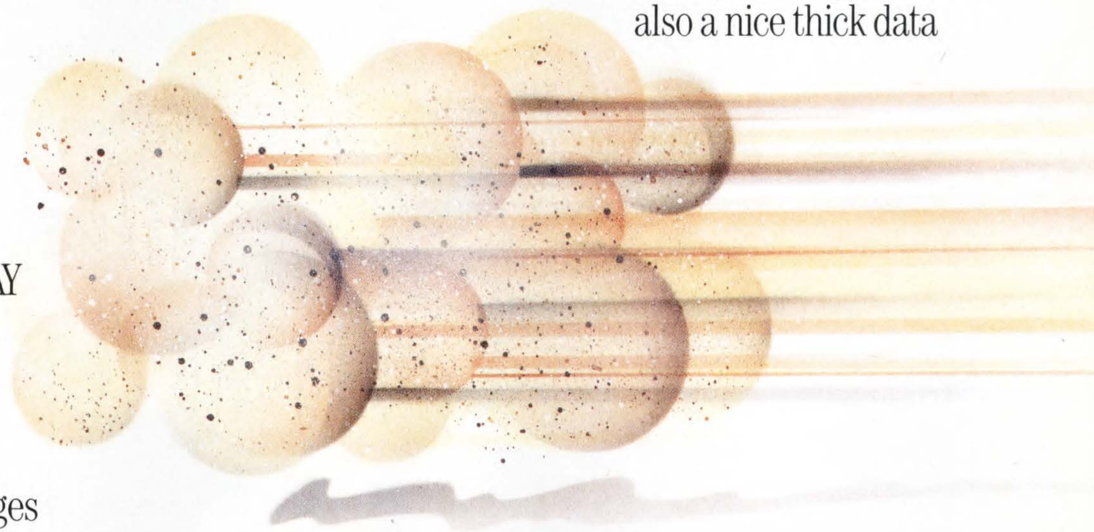

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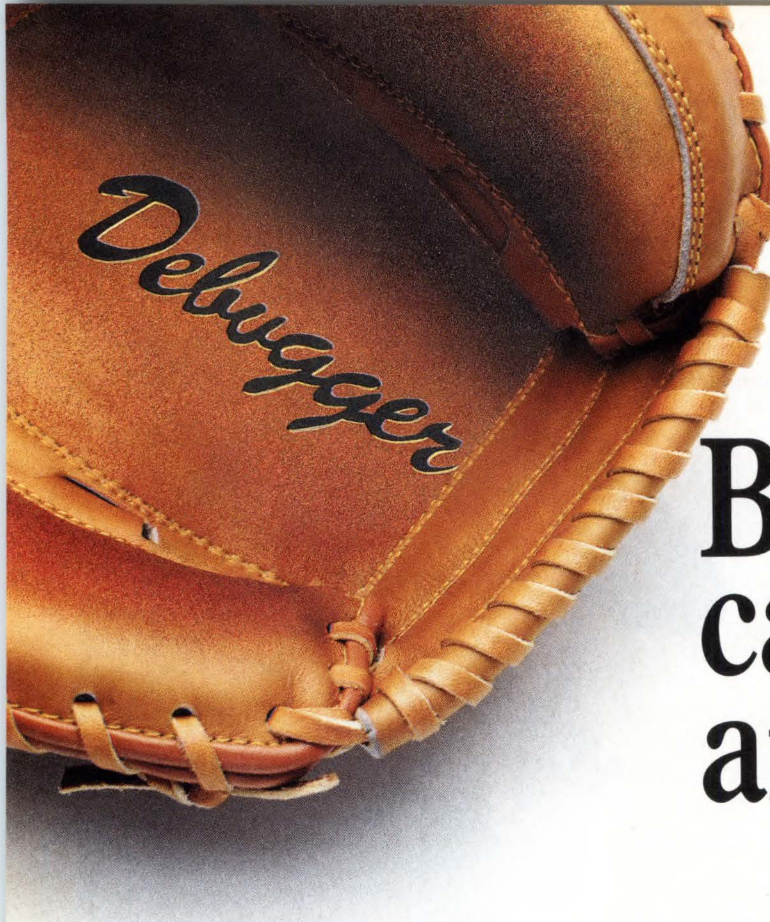

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ZIATECH CORPORATION

CONTROL POINT

Test and Control Product News from Ziatech Corporation — **Fall, 1988**

Time-saving development tools –

STD DOS II OPERATING SYSTEM BRINGS MORE PC FEATURES TO STD

The ZT 300 is an integrated STD Bus computer featuring Ziatech's new version of STD DOS. The new STD DOS II allows Ziatech computers to run PC software programs like 86-Ladder and MICRO-VIEW.

FOCUS ON SOFTWARE

STD DOS II, a new generation of Ziatech's implementation of IBM PC DOS, brings even more capability to Ziatech STD Bus systems.

Originally introduced by Ziatech in 1985, STD DOS enables STD Bus computers to run PC DOS-compatible software programs. It gives these rugged industrial computers access to the familar file system and peripherals of the PC. STD DOS, with unique Ziatech features such as an on-line, battery-backed configuration file and Virtual System Console, significantly speeds the development of test and control applications.

VIRTUAL SYSTEM CONSOLE

Virtual System Console (VSC) is an industry acclaimed development tool unique to Ziatech's STD DOS. With VSC, an IBM-compatible PC and an STD Bus system are transparently connected through host software and serial ports. VSC makes it possible to control the operation of both the STD DOS system and the PC from one user console. The console's screen and keyboard appear to be connected directly to both systems. At the touch of a hot key, the programmer can toggle back and forth between the two systems, developing software on the PC and debugging and testing it on the STD system.

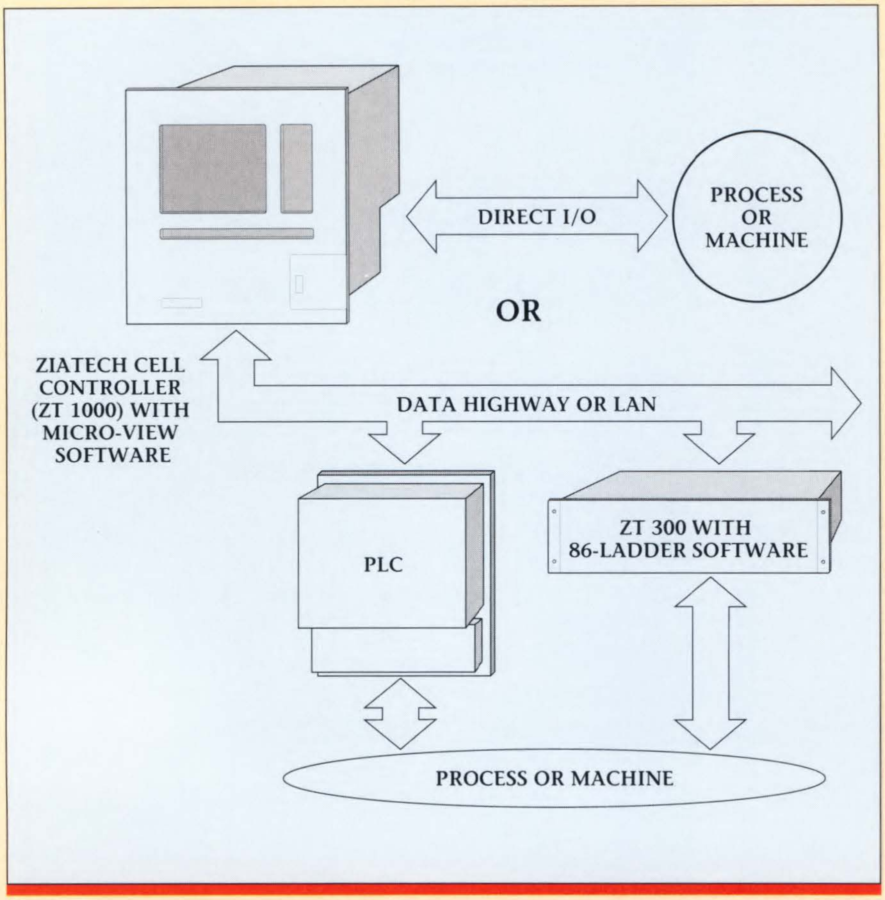
(Continued on page 4)

INSIDE

ZIATECH CORPORATION

86-LADDERS, MICRO-VIEW –

NEW SOFTWARE PUTS ZIATECH STD COMPUTERS IN CONTROL



Ziatech's packaged STD Bus systems operating process control software and ladder logic software for industrial control applications.

Two new software packages for industrial equipment control and process monitoring are now available for use with Ziatech's STD Bus computers.

LADDER LOGIC PROGRAMMING

The 86-LADDER software program from Engineering Tools/Wizdom Systems (Naperville, IL) allows a Ziatech STD Bus industrial computer to function as an Allen Bradley-compatible programmable logic controller (PLC). It offers a superset of Allen-Bradley ladder language, but unlike PLCs, it supports different I/O boards and subsystems from many manufacturers.

The use of 86-LADDER on Ziatech computers extends the performance and flexibility of PLCs while significantly lowering system costs by allowing the use of industry standard off-the-shelf components.

An STD Bus computer with 86-LADDER software is a very cost effective companion to a MICRO-VIEW-equipped cell controller, which is described below.

PROCESS MONITORING AND REPORTING

MICRO-VIEW, a product of Indelec (Brookline, MA) is a multitasking, color graphics-based package. The software is designed to monitor and report on factory automation processes that are being controlled by PLCs or Ziatech industrial computers.

Ziatech's IBM PC-compatible packaged systems (ZT 1000 Industrial Workstation and ZT 300 Industrial Computer) are fully supported by the menu-driven, user-friendly MICRO-VIEW software.

A MICRO-VIEW-equipped "supervisory station" or cell controller features consolidated archiving, trending, alarming, report generation and graphics at one control point. It also has the capability to run monitoring and control programs in a non-viewed "background" while a PC DOS program is being run in the foreground.

PC AND INDUSTRIAL COMPUTER-COMPATIBLE

MICRO-VIEW can be run on a personal computer as well as Ziatech's packaged STD Bus systems. A cell controller equipped with MICRO-VIEW can be connected to individual controllers via serial data highways and Ziatech's Z-NET Local Industrial Network. Future plans include plug-in STD Bus-based PLC emulation computers for use in cell controllers with MICRO-VIEW.

For more information on these software programs and Ziatech computers, check the MICRO-VIEW/86-LADDER box on the return card.

Supports Ziatech GPIB/PC interfaces –

ASYSTANT GPIB SOFTWARE PROVIDES INSTRUMENT CONTROL AND ANALYSIS

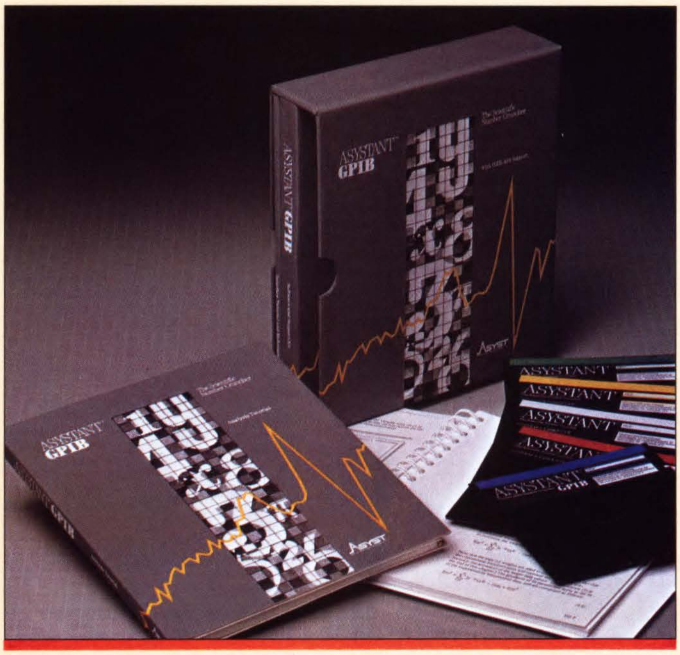
ASYSTANT GPIB, an IEEE 488 software program for scientifc instrument control and analysis, is now available directly from Ziatech.

Ziatech IEEE 488 hardware interfaces for IBM-compatible personal computers and the IBM Personal System/2 are currently supported by ASYSTANT GPIB, and will also be supported by ASYST. Both software packages are products of Asyst Software Technologies, Inc. (Rochester, New York).

GPIB INSTRUMENT CONTROL

The program is designed for scientists and engineers who need to control GPIB instrument clusters, and analyze and graphically present data in one easy-to-use integrated environment. No programming experience is necessary to use the ASYSTANT GPIB.

MENU-DRIVEN, COLOR GRAPHICS



The ASYSTANT GPIB software package, now available with Ziatech IEEE 488 interfaces, combines programmability and an easy-to-use menu-driven interface.

The menu-driven GPIB software allows GPIB device definition, interactive execution of bus commands, device-dependent commands and serial polling, and display and analysis of data. An Interactive Mode verifies instrument operation and data results, while the GPIB Program Mode is used for building automated routines.

IEEE 488 INTERFACE PRODUCTS

Ziatech offers a complete line of IEEE 488 interfaces and software drivers for personal computers, the IBM PS/2, STD Bus systems and MULTIBUS systems.

For more information, check the ASYSTANT GPIB/ IEEE 488 products, on the return card.

New Brochure Details STD DOS Features

In conjuction with the release of STD DOS II (see related stories, this issue), a new 1988/1989 edition of the STD DOS Technical Brochure is now available from Ziatech.

PRODUCT LITERATURE

The new brochure provides a comprehensive description of STD DOS and all of its options. System architecture, performance, software development, target system configurations, and other features are detailed.

For a free copy of the STD DOS Technical Brochure, check the STD DOS box on the return card.

CONTROL POINT

Published bimonthly by Ziatech Corporation 3433 Roberto Court San Luis Obispo, California 93401 For information on any product or service mentioned in Control Point, please call (805) 541-0488 and ask for Customer Service.

ZIATECH CORPORATION

How tough is your tractor?

STD DOS SYSTEM TESTS VEHICLES FOR DEERE

A Ziatech STD DOS computer in this data acquisition system helps Deere & Company test a variety of vehicles ranging from lawn mowers to earth moving equipment.

Deere & Company is well known for its large line of field vehicles, including lawn mowers, golf carts, tractors, logging skidders, tree choppers and earth moving equipment. When new vehicle designs are in the protoype stage, they are tested extensively, using a monitoring system based on Ziatech's STD Bus industrial computers.

CUSTOMER PROFILES

COMPACT DATA ACQUISITION SYSTEM

The company-designed data acquisition systems feature Ziatech's STD DOS (See story, this issue).

The portable units collect a variety of ride, function and fatigue data from operating prototype vehicles. Data is normally collected in RAM memory and copied to a removeable hard or floppy disk drive when the environmental conditions make it possible.

USES RELIABLE, LOW COST STD BUS

The reliability and small size of the STD Bus format combined with the the functionality of STD DOS, make it an excellent choice for applications requiring a low cost, rugged data acquisition or control system. The STD Bus also offers over 1000 different I/O boards for a variety of test and control applications.

A typical Deere & Company test system includes a Ziatech 8088-based single board computer, a MegaRAM board, along with an analog-to-digital card, a disk drive, and two user-designed cards.

New DOS Supports Dual STD Video

(Continued from page 1)

DATA COMPRESSION

Data compression for disk and VSC data communications has been added to STD DOS, increasing system throughput and storage capacity.

IMPROVED DISK SUPPORT

STD DOS II provides support for Ziatech's new integrated floppy and 30 Mbyte hard disk drives, which combine the drive and controller on a single STD Bus board. The new release also supports up two local 30 Mbyte hard disks for the first time.

NETWORK SUPPORT

Ziatech's Z-NET Local Industrial Network, which features ARCNET STD, PC and PS/2 interfaces, and ViaNet network software, is fully supported by STD DOS II.

MULTI-VIDEO SUPPORT

STD DOS II supports two ZT 8844 Video/Keyboard Controllers, making it possible to equip an STD DOS system with two independent video displays.

STD DOS TRAINING

Ziatech also now offers a regularly scheduled three-day training course, designed to teach programmers the important aspects and implementations of STD DOS. The next session will take place October 26-28 in San Luis Obispo, CA.

For more information, check the STD DOS II box on the return card.

ZIATECH CORPORATION

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Multibus II computer-board directory

System architecture, operating systems, software-development support, and product lifetime all play a part in choosing a backplane bus for a computer system. If you choose the Multibus II, you can find computer boards for all the main functional areas—central processing, mass storage, communications, graphics, and industrial I/O—to ease your make-versus-buy decisions.

Peter Harold, *European Editor*

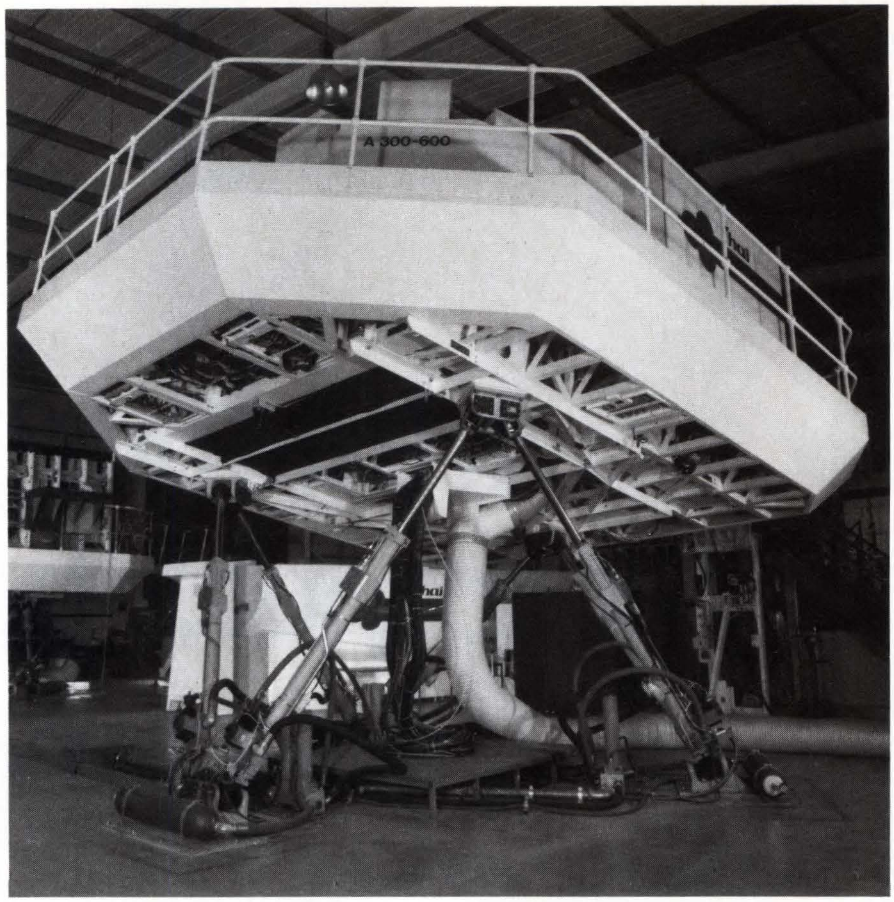
On the following pages we present EDN's Multibus II computer-board directory—an up-to-date compendium of Multibus II board-level products that are currently on the market or close to release. The directory is divided into nine sections—CPU, memory, peripheral controller, communication controller, graphics, analog I/O, digital I/O, special function, and central services module (CSM) boards—and it provides sufficient information on each board's functions for you to decide which boards might suit your application.

Multibus II boards generally provide more functions than do boards for the VME Bus, the Multibus II's main competitor. Multibus II boards have more functions not only because they're approximately a third bigger than VME Bus boards (Multibus II uses an extended double-Eurocard board, whereas the VME Bus uses a standard double Eurocard), but also because most Multibus II boards have onboard intelligence in order to take full advantage of such features as message passing. In addition, because most Multibus II boards are recent designs, they benefit from the high-integration processor, memory, and peripheral devices currently supplied by semiconductor manufacturers.

But if you're wondering why you should consider using the Multibus II instead of the VME Bus or some other IEEE-approved or de facto standard bus, take a look at the following case studies. The three companies profiled below each chose the Multibus II for their systems; two of the companies have already implemented successful designs, and the third has committed itself to a long-term investment in Multibus II systems.

Multibus II flies high

Singer Link-Miles Ltd (Lancing, UK) manufactures advanced training systems, including flight simulators for commercial and military aircraft. The simulators replicate the cockpit areas of particular aircraft, simulating all of the planes' control and instrumentation systems. Both the feel of the controls and the response of the cockpit instrumentation are matched to those of the real aircraft, and computer-generated graphic images simulate forward-vision runway approaches. In addition, the entire cockpit assembly is mounted on a



Employing about forty 80286-based CPU cards, *Singer Link-Miles' flight simulator for the A300 Airbus contains one of the largest Multibus II computer systems yet constructed.*

hydraulically controlled platform to simulate the pitch, roll, and yaw that a pilot would experience when actually flying.

During the 70s, Singer Link-Miles, like all other flight-simulator manufacturers, controlled its simulators with a 32-bit minicomputer or a small cluster of minicomputers that accessed shared memory. However, according to David Parkinson, technical-development manager of Singer Link-Miles' flight-simulation division, the increasing complexity of aircraft-control and -instrumentation systems and the increased fidelity required from simulators soon created an I/O-operations bottleneck in these systems.

To maintain the real-time response essential for high-fidelity simulation, all the simulator's main functional modules—for example, its flight-control and engine-management systems—must perform I/O operations, process data, and exchange information regarding their current status at least 30 times per second. In addition, many control systems must respond locally to the pilot's actions at a much higher rate.

In 1980, the company began to develop a new range of simulators that were based on microprocessor technology, with distributed processing and a high degree of functional partitioning. Rather than sharing a single CPU resource among multiple tasks, the new simulators had a dedicated computer for each major simulation function—for example, they had separate computers for flight, engine management, and so on. In addition, the company designed the simulator as a modular system to make it easier to manufacture and maintain.

After looking at the bus standards available at the time and deciding none were suitable, Singer Link-Miles developed its own backplane bus and board set. This proprietary bus included a 32-bit multiplexed address/data bus with multimaster bus-arbitration capabilities and a 16-bit local bus for memory and I/O extension. The bus also included special memory areas that were accessible via the 32-bit backplane bus, which you could use to interrogate the board to determine its type. In addition, the company developed a high-speed parallel global bus for intercrate communication.

The computer boards were based on Intel μPs, largely because suitable software tools and floating-point coprocessors were available for these μPs in the early 80s. The boards had onboard microcontrollers to perform self-test and system-confidence checks. Interprocessor communication took place via dual-port memory on the individual CPU cards. The computer boards were housed on extended double Eurocards with DIN-41612 connectors. With some pride, Parkinson points out that Singer Link-Miles' proprietary bus already had many of the features that subsequently appeared in the Multibus II specification.

In 1984, Singer Link-Miles adopted the Multibus II for new simulator designs, not only because it matched so well with the company's proprietary bus, but also because it enabled the firm to buy some of the boards it required for the system instead of having to manufacture all the components itself. Currently, the company is able to buy suitable CPU, memory, peripheral-controller, and communications-controller cards, although it still must design most of its specialized I/O cards.

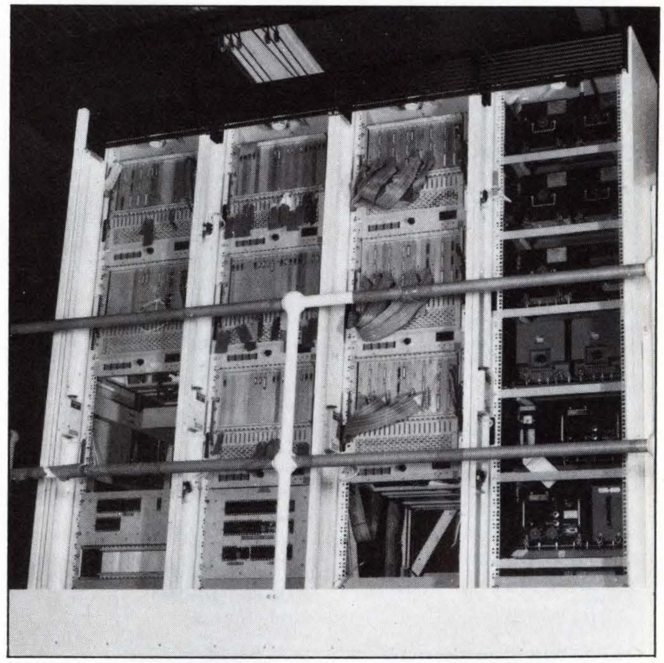
The latest Boeing-747 simulator from Singer Link-Miles illustrates how complex the company's Multibus II systems are becoming. The Boeing-747 simulator contains approximately thirty-five 80386-based CPU boards and 200 I/O cards. Most of the I/O cards are intelligent subsystems in their own right, with message-passing coprocessor (MPC) interfaces to the Multibus II iPSB and onboard μPs.

The systems rely heavily on the Multibus II's interconnect space (the memory space on the iPSB allocated for board identification and configuration) and built-in self-test (BIST) functions. For example, the systems use the interconnect space extensively for system-configuration management and control. A service engineer can change a board (and often can even replace it with one from a different manufacturer) without having to alter jumper links or DIP-switch settings; when the system is initialized, it automatically polls all the boards to determine their type, manufacturer, and revision status. BIST functions run continuously during system operation, alerting the flight instructor to any system malfunctions and pinpointing the malfunctions on a particular area of a particular board.

The company could have based its simulators on a VME Bus computer system, Parkinson says. In fact, the company's US division has used VME Bus computers in designing reduced-functionality training simulators. However, Parkinson notes, if the company had used the VME Bus, it would have had to graft on functions comparable to Multibus II's BIST and interconnect space, which would have increased the overall development time.

Similar technical reasons caused McDonnell Douglas (St Louis, MO) to choose Multibus II computers to control its combat-aircraft simulators, according to systems engineer Mike Chapin. Product lifetime was another important factor in the choice, he adds. The simulators must be able to support the aircraft until well into the 1990s and beyond, and, he says, the company just doesn't believe that the VME Bus will be around 15 years from now. Buses historically have lasted only 10 to 15 years, and the VME Bus was already five years old when McDonnell Douglas started the project.

Although Singer Link-Miles's system requires the broadcast of global data among all its simulation functions 30 times per second, the system doesn't use the Multibus II's message-passing function for this purpose. The reason, Parkinson says, is that the library



Link-Miles' A300 Airbus simulator *illustrates the requirement for a high-speed parallel bus for intercrate communication. To do the job, the company had to develop a proprietary bus.*

of Fortran software modules from which much of the simulator software is built doesn't support message passing, and at present the cost of modifying all these modules to support message passing is too high. As a result, the system performs interprocessor communication via shared dual-port memory, as do the company's older simulators.

One of the few criticisms of the Multibus II that Parkinson cites is the initial lack of suitable operating systems that could support message passing. However, such operating systems are beginning to emerge on the market, and a new product, the ISO-TP4 Transporter, jointly developed by Digital Research Inc (Monterey, CA) and American Manufacturing Systems Inc (Maitland, FL) in cooperation with Intel, may make it easier for you to integrate message passing in the operating system of your choice. Working in conjunction with an Intel MPC, the ISO-TP4 Transporter applies the principles of the Open Systems Interconnection (OSI) 7-layer communication model to the Multibus II architecture. The iPSB bus represents layer 1 (the physical layer) of the OSI model, the MPC handles the layer 2 (data link) and layer 3 (network) functions, and the ISO-TP4 Transporter provides layer 4 (transport) functions.

By transmitting bus messages via the ISO-TP4

Text continued on pg 174

For more information . . .

For more information on the Multibus II computer boards described in this directory, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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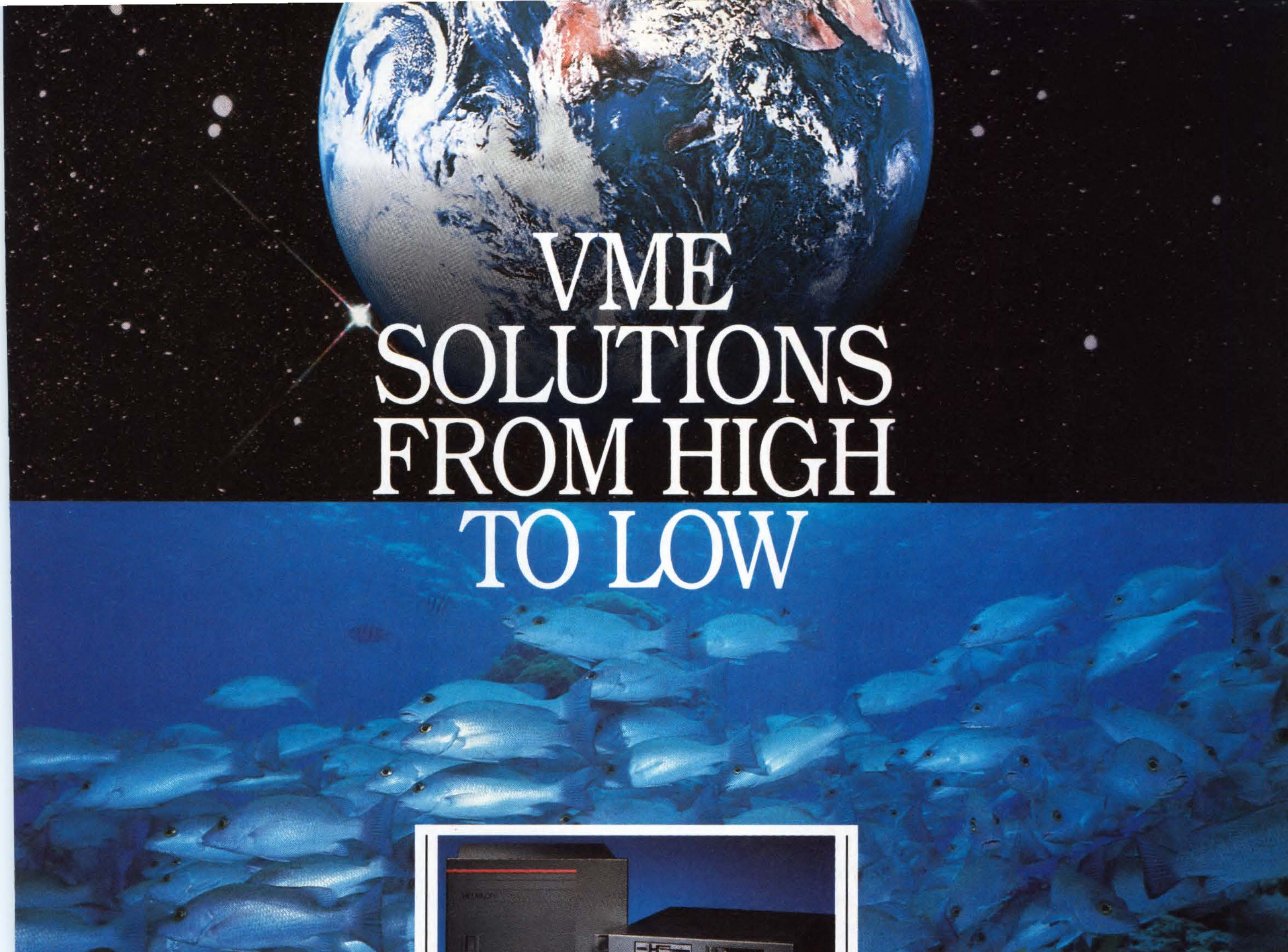


CIRCLE NO 184

Transporter, processes running on particular bus agents (processors) need specify little more than a destination address for the message and the message's data content. The transporter drives the MPC by using Intel's transport-protocol primitives to arbitrate for iPSB access and transmit the message. The result is that the Multibus II backplane appears to Multibus II agents as a local-area network, in which each agent is equivalent to a network node.

In the second stage of the development of its ISO-TP4 Transporter, Digital Research plans to introduce a version that adds application transparency to the current version's media transparency. (Application transparency means that the agents don't have to know the physical addresses to which they must send messages; media transparency indicates that the application programs don't need specific knowledge of the mechanism by which one agent passes messages to another.) The upgraded version will enable bus agents to access devices by using a logical name, without requiring specific information about the device's address in the Multibus II's message-passing space.

Although Digital Research offers the ISO-TP4 Transporter primarily for use with its FlexOS real-time multitasking operating system—a FlexOS Multibus II driver pack, including the FlexOS operating system, a set of target-system drivers, and the ISO-TP4 Transporter (in loadable and linkable form) costs $1000—the company also supplies the transporter as fully documented C-language source code so that you can integrate it in other operating systems.

Multibus II facilitates factory automation

AEG's Automation Systems Div (Frankfurt, West Germany) chose the Multibus II for different reasons (**Ref 1**). When the company decided on an architecture for factory-automation systems, its primary desire was to adopt an open-system architecture. Such an architecture, the company believes, is the only type that allows you to modify a system's functionality by adding or exchanging components from different manufacturers without having to change existing system components. Also, because an open system can readily accept new components, it's easier to upgrade in the future to achieve state-of-the-art performance.

AEG's proposed system calls for distributed processing, in which tasks are executed by the processor most suited to the task. As a result, the system required a bus over which to perform context switching between processors. The company proposes that dedicated processors be used only for certain tasks—that is, for tasks with stringent real-time requirements, for the provision of Unix user interfaces, for control of I/O operations, for control of mass-storage peripherals, and for autonomous protocol handling on communications media such as MAP, Proway-C, or Ethernet. Standard interfaces among these processors allow each processor to run the operating system that best suits it to its allocated task.

In choosing a preferred 32-bit μP for the company's factory-automation systems, AEG considered both the Motorola 68020 and the Intel 80386. However, the company considers operating-system support to be far more significant than the pros and cons of a particular 32-bit μP. As a result, it chose the 80386 because, for real-time applications, it preferred Intel's iRMX-386 operating system to Motorola's VersaDOS. (AEG also has a cooperation agreement with Intel which it believes will allow it to influence the further development of iRMX-386). The company then selected Unix as the preferred operating system for task areas that are not time-critical.

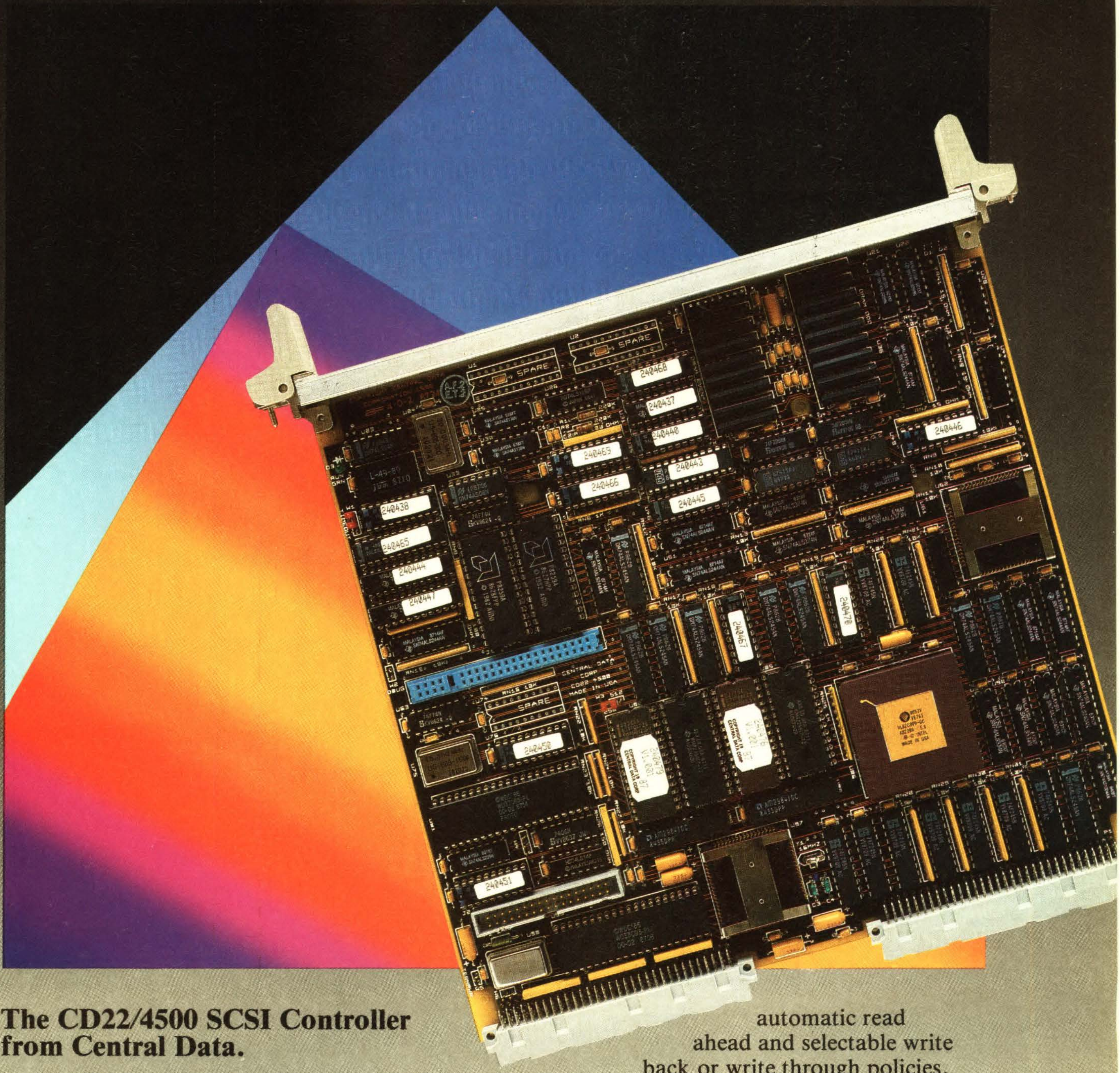
Having chosen Intel processors and operating systems, the company naturally chose the Multibus II as the backplane bus standard because of its greater compatibility with these products. The Multibus II's greater bus bandwidth (40M bytes/sec) and message-passing capability were additional factors in the company's adopting the Multibus II instead of the VME Bus. EDN

Reference

1. Klett, Rolf, *Process computer with distributed intelligence and open system architecture,* AEG, Frankfurt, West Germany, February 1988.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

Disk-Caching SCSI for Multibus* II.



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*Multibus is a trademark of Intel Corporation.

CIRCLE NO 185

TABLE 1—MULTIBUS II CPU BOARDS

MANUFACTURER	MODEL	MICROPROCESSOR TYPE	MICROPROCESSOR CLOCK FREQUENCY (MHz)	DMA CONTROLLER TYPE	DMA CONTROLLER NUMBER OF CHANNELS	MATH CO-PROCESSOR	MMU	ONBOARD MEMORY: LOCAL RAM[1] (BYTES) MAXIMUM	LOCAL RAM[1] SUPPLIED	DUAL-PORT RAM[1] (BYTES) MAXIMUM	DUAL-PORT RAM[1] SUPPLIED
CENTRALP AUTOMATISMES	FAB-086	80186	—	—	—	—	—	—	256k		
	FAB-286	80286	—	—	—	80287	—	—	2M DYNAMIC RAM 64k STATIC RAM		
CONCURRENT TECHNOLOGIES	CP-186-010	80186	10		2			32k		128k	16k
	CP-386-016	80386	16	82380	8	80387		16M		1M	128k
ECKELMANN	EM-CPU01	80386	16			80387		256k	256k	256k	256k
GEOMELEC/RENAULT AUTOMATION	RAUT-286	80286	10	82258	4	80287		320k	—		
	RAUT-386-28	80386	16	82258	4	80387		320k	—		
HEURIKON	HK68-M220	68020	12.5, 16.7, 20	CUSTOM	4	68881, 68882	68851	4M	—		
INTEL	iSBC-186-100	80186	8	82258	4	8087		512k 384k 256k	512k 384k 256k	0 128k 256k	0 128k 256k
	iSBC-286-100A	80286	8	82258	4	80287		128k	16k		
	iSBC-386-116, -120	80386	-116: 16 -120: 20	82258	4	80387		16M (2-SLOT)	1M, 4M (1-SLOT) 2M, 8M, 16M (2-SLOT)	16M (2-SLOT)	1M, 4M (1-SLOT) 2M, 8M, 16M (2-SLOT)
MICROBAR SYSTEMS	MT-68020A	68020	16.67	68451	4	68881	68881			4M	1M
MICRO INDUSTRIES	MIBII-186-101	80186	8	82258	6	8087				1M	1M
	MIBII-186-102	80186	8	82258A	6	8087				1M	1M
	MIBII-186-110A	80186	8	82258	4			512k	512k		
	MIBII-186-110B	80C186	10, 12.5, 16					128k			
	MIBII-386-100, -101, -102	80386	20	82258A	4	80387, WTL1167		2M	2M	2M	2M
	MIBII-386-110, -113	80386	-110: 16 -113: 20	82380	8			128k	128k		
	MIBII-386-111, -112, -114, -115	80386	-111: 16 -112: 16 -114: 20 -115: 20	82380	8			-111: 128k -112: 512k -114: 128k -115: 512k	-111: 128k -112: 512k -114: 128k -115: 512k		
	MIBII-386-120	80386	16	2 8237s	7	80387	82C302	2M	2M		
SIEMENS	OSM-B17	80186	8	82258	6	8087		—	1M	—	1M
	OSM-B35	80386	16	2 8237s	7	80387	82C302	2M	2M		
	OSM-B37	80386	20	82258	4	80387, WTL1167		2M	2M	2M	2M
TADPOLE TECHNOLOGY	TP-33M	68030	16 TO 33	CUSTOM	3	68881, 68882		16M	4M		
	TP-880M	88100	20 TO 33	CUSTOM	4		2 88200s	16M	4M		

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

NOTES:
1. INCLUDES PIGGYBACK MEMORY THAT ALLOWS THE BOARD TO FIT IN A SINGLE SLOT UNLESS OTHERWISE STATED.
2. ALL BOARDS SURVEYED SUPPORT MESSAGE-PASSING INTERCONNECT SPACE, BUILT-IN SELF-TEST, AND THE INTEL TRANSPORT PROTOCOL EXCEPT RAUT-286 AND RAUT-386-28—NO BIST SUPPORT; RAUT-286, RAUT-386-28, AND EM-CPU01—NO INTEL TRANSPORT PROTOCOL SUPPORT (ALTHOUGH IT COULD BE ADDED WITH SUITABLE SOFTWARE ROUTINES).
3. OME STANDS FOR ONBOARD MODULE EXPANSION.

TABLE 2—MULTIBUS II MEMORY BOARDS

MANUFACTURER	MODEL	MEMORY TYPE	MEMORY CAPACITY (BYTES) MAXIMUM	MEMORY CAPACITY SUPPLIED	MEMORY PORTS iPSB	MEMORY PORTS iLBX-II	DATA-TRANSFER WIDTHS SUPPORTED[1] 8-BIT	16-BIT	24-BIT	32-BIT	BUS CYCLES REQUIRED TO ACCESS MEMORY: NUMBER OF CYCLES / MAX CLOCK FREQUENCY (MHz)
BUBBL-TEC	MIH-Y	BUBBLE	2M	512k, 1M, 2M	•		•	•	—	•	4 AT 10
CENTRALP AUTOMATISMES	FAB-104	DYNAMIC RAM	4M	4M		•	•	•	—	•	READ: 3 AT 10 WRITE: 2 AT 10
INTEL	iSBC-MEM-310, -312, -320, -340	DYNAMIC RAM	-310: 1M -312: 512k -320: 2M -340: 4M	-310: 1M -312: 512k -320: 2M -340: 4M	•	•	•	•	•	•	6 AT 8 ZERO-WAIT-STATE ON iLBX-II
MICRO INDUSTRIES	MIBII-130	28-PIN JEDEC ROM OR RAM	1M BYTES IN 16 SITES		•	•	•	•	•	•	MEMORY DEPENDENT
MICRO MEMORY	MM-2100D	DYNAMIC RAM	16M	4M, 8M, 12M, 16M	•	•	•	•	•	•	ZERO-WAIT-STATE ON iLBX-II
MONOLITHIC SYSTEMS	MSC-5910	DYNAMIC RAM	8M	1M, 2M, 4M, 8M	•	•	•	•	•	•	ZERO-WAIT-STATE ON iLBX-II
SIEMENS	OSM-B130	28-PIN JEDEC ROM OR RAM	1M BYTES IN 16 SITES		•	•	•	•	•	•	MEMORY DEPENDENT

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

NOTES: 1. NO BOARDS SURVEYED SUPPORT BURST-MODE DATA TRANSFERS.

INSTALLABLE EPROM (BYTES)	BACKPLANE/EXPANSION INTERFACES: MULTIBUS II				I/O INTERFACES			OPERATING SYSTEMS SUPPORTED	PRICE	COMMENTS
	iPSB	iLBX-II	iSBX	OTHER BUSES	SERIAL I/O PORTS	PARALLEL I/O LINES	OTHER INTERFACES			
256k	•		1		—	—	BITBUS, LAC, OR ETHERNET OPTIONS	iRMX-1, iRMX-2	$4000	REAL-TIME CLOCK AND STATIC RAM WITH BATTERY BACKUP; ONBOARD CSM FUNCTIONS.
8 32-PIN SOCKETS	•		1		4	—		iRMX-1, iRMX-2	$5000	STATIC RAM WITH BATTERY BACK-UP; ONBOARD CSM FUNCTIONS.
256k	•		1		4	48		RMX	$2400	PARALLEL I/O CONFIGURABLE AS CENTRONICS PORT.
1M	•			cCBX	2			UNIX, RMK, RMX	$4900	cCBX LOCAL MEMORY EXTENSION BUS.
256k	•		1	AT	2			RMX, DOS	DM 6500 TO DM 8500	COMPATIBLE WITH THE IBM PC/AT.
512k	•			G96	1			iRMX-286	Fr 14,000	
512k	•			G96	1			iRMX-286	Fr 14,000	
256k	•	•	1		2		SCSI	UNIX V.3, VRTS-32, OS-9, VxWORKS	$3995 TO $8385	REAL-TIME CLOCK AND 128k-BYTE STATIC RAM WITH BATTERY BACKUP.
512k	•		1		2	24		iRMX-86	~$1900	PARALLEL I/O CONFIGURABLE AS A SCSI OR CENTRONICS INTERFACE.
128k	•	•	2		2	24		iRMX-86, iRMX-II	~$2400	PARALLEL I/O CONFIGURABLE AS A SCSI OR CENTRONICS INTERFACE.
512k	•		1		1			UNIX V.3, iRMX-86, iRMX-II.3, iRMK	-116: ~$4800 TO ~20,600 -120: ~$6000 TO ~$21,800	64k-BYTE ZERO-WAIT-STATE CACHE.
256k	•		1		2		SCSI	UNIX, VRTX	$3390 TO $6450	BUILT-IN MONITOR FIRMWARE.
512k	•			OME[3]	3		SCSI, CENTRONICS	RMX, RMOS-2	$2000	
512k	•			OME[3]	5		SCSI, CENTRONICS	RMX, RMOS-2	$2500	
256k	•		2		1			RMX, RMOS-2	$2000	PROTOTYPING AREA.
128k	•				1			RMX, RMOS-2	$1800	PROTYPING AREA; P2 CONNECTOR I/O.
256k	•			OME[3]	1		SCSI	UNIX, RMK, RMOS-286	-100: $5500 -101: $6000 -102: $7000	-101: SAME AS -100 PLUS 64k-BYTE CACHE. -102: SAME AS -100 PLUS 256k-BYTE CACHE.
64k	•				1			RMK	-110: $4000 -113: $5000	PROTOTYPING AREA.
64k	•			OME[3]	1			RMK	-111: $4500 -112: $5500 -114: $5500 -115: $6500	PROTOTYPING AREA; ONBOARD MODULE EXPANSION (OME) INTERFACE.
128k	•			AT	2		CENTRONICS, KEYBOARD	MS-DOS	$6000	REAL-TIME CLOCK; BIOS COMPATIBLE WITH IBM PC/AT.
512k	•			OME[3]	3		SCSI, CENTRONICS	RMOS-2	DM 4950	
128k	•			AT	1		CENTRONICS, KEYBOARD	UNIX, MS-DOS	DM 8776	IBM PC/AT COMPATIBLE.
256k	•			OME[3]	1		SCSI	UNIX, RMOS-2, RMOS-286	DM 9970	AVAILABLE WITH A 64k-BYTE OR 256k-BYTE ONBOARD CACHE.
2M	•	•	1		6	8	SCSI, ETHERNET	TPIX V.3.1, VRTX-32	~£3275 (10)	
1M	•	•	1		4	2	SCSI, ETHERNET	TPIX V.3.1	~£5700 TO ~£5900 (10)	ADDITIONAL 68000 I/O PROCESSOR.

ERROR DETECTION/ CORRECTION	CACHE MECHANISM	MULTIBUS II FUNCTIONS			MEMORY CONFIGURATION VIA iPSB INTERCONNECT SPACE	PRICE	COMMENTS
		MESSAGE PASSING	INTER-CONNECT SPACE	BUILT-IN SELF TEST			
ECC		•	•	•	•	$1485 TO $3427	NONVOLATILE STORAGE FOR HARSH ENVIRONMENTS.
PARITY			•			$5700	REAL-TIME VIDEO-ACQUISITION/GRAPHICS REFRESH MODE.
PARITY	ASSOCIATIVE TAG CACHE	•	•	•	•	~$1500 TO ~$3700	
PARITY			•	•	•	$2500	POWER-FAIL PROTECTION.
PARITY	32k-BYTE ASSOCIATIVE CACHE	•	•	•	•	~$2400 TO ~$7000	
ECC	32k-BYTE ASSOCIATIVE CACHE		•	•	•	$2195 TO $5495	ERROR-SCRUBBING AND ERROR-LOGGING FACILITIES.
PARITY			•	•	•	DM 2500	POWER-FAIL PROTECTION

TABLE 3—MULTIBUS II PERIPHERAL-CONTROLLER BOARDS

MANUFACTURER	MODEL	DESCRIPTION	DRIVES SUPPORTED: TYPE	DRIVES SUPPORTED: NUMBER	INTERFACE STANDARDS SUPPORTED	MAXIMUM DATA-TRANSFER RATE TO OR FROM PERIPHERAL DEVICES (BYTES/SEC)	MAXIMUM DATA-TRANSFER RATE TO OR FROM MULTIBUS II (BYTES/SEC)	ERROR PROTECTION/ CORRECTION
AMERICAN MANUFACTURING SYSTEMS	910-003-02	SCSI MEDIA CONTROLLER	SCSI	7 PERIPHERAL ADAPTERS	SCSI	1M (ASYNC)	40M	PARITY
CENTRAL DATA	CD22-4500	SCSI CONTROLLER	SCSI	7 PERIPHERAL ADAPTERS	SCSI	1.5M (ASYNC) 4M (SYNC)	40M	PARITY
CIPRICO	RIMFIRE-2200	SMD-E CACHING DISK CONTROLLER	SMD-E	4	SMD	3M	32M	PARITY
	RIMFIRE-2500	SCSI BUS HOST ADAPTER AND FLOPPY-DISK CONTROLLER	SCSI FLOPPY DISK	7 PERIPHERAL ADAPTERS 4	SCSI —	4M	32M	PARITY
	TAPEMASTER-2000	PERTEC-COMPATIBLE 1/2-IN. TAPE-DRIVE CONTROLLER	START/STOP OR STREAMER	8	PERTEC	1.5M	32M	
INTEL	iSBC-186-224A	WINCHESTER-DISK, FLOPPY-DISK, TAPE-STREAMER CONTROLLER	WINCHESTER FLOPPY TAPE STREAMER	4 4 4	ST506/412 SA450/460 QIC-02	625k 31.25k 86.7k	4M	ECC/CRC
STELLARCIM	SCIM-ESB-X	INDUSTRIALIZED DATA STORAGE	WINCHESTER OR BUBBLE CARTRIDGE	2	SCSI	(SCSI) 1.5M (BUBBLE) 19.7k	THROUGH MPC AT BUS RATE	PARITY
	SCIM-WFB, -WFB1	WINCHESTER-DISK, FLOPPY-DISK CONTROLLER	WINCHESTER FLOPPY	3 2	ESDI, ST506 SA450/460	(ESDI) 1.8M	THROUGH MPC AT BUS RATE	CRC-CCITT, SINGLE/ DOUBLE BRS
TADPOLE TECHNOLOGY	TPDSCM	DUAL SCSI BUS CONTROLLER	SCSI	14 PERIPHERAL ADAPTERS	SCSI	4M	40M	PARITY

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

TABLE 4—MULTIBUS II COMMUNICATION-CONTROLLER BOARDS

MANUFACTURER	MODEL	DESCRIPTION	ASYNCHRONOUS CHANNELS: TYPE	ASYNCHRONOUS CHANNELS: NUMBER	ASYNCHRONOUS CHANNELS: MAXIMUM BIT RATE (Bps)	ASYNCHRONOUS CHANNELS: PROTOCOL	SYNCHRONOUS/ASYNCHRONOUS CHANNELS: TYPE	SYNCHRONOUS/ASYNCHRONOUS CHANNELS: NUMBER	SYNCHRONOUS/ASYNCHRONOUS CHANNELS: MAXIMUM BIT RATE (Bps)	SYNCHRONOUS/ASYNCHRONOUS CHANNELS: PROTOCOL	SYNCHRONOUS: TYPE	SYNCHRONOUS: NUMBER
CENTRAL DATA	CD-22-3800	SERIAL I/O CONTROLLER					RS-232C RS-232C/422	6 2	76.8k (ASYNC)	ASYNC, X.25		
CONCURRENT TECHNOLOGIES	CC-186-016	TERMINAL CONTROLLER	RS-232C	14	19.2k	ASYNC	RS-232C/422	2	130k	HDLC, SDLC, BISYNC		
	CC-386-008	SERIAL I/O CONTROLLER					RS-232C/422	8	1.5M	HDLC, SDLC, BISYNC		
INTEL	iSBC-186-410	SERIAL I/O CONTROLLER	RS-232C	4	19.2k	ASYNC	RS-232C/422A	2	1M (SYNC)	HDLC, SDLC		
	iSBC-186-530	ETHERNET CONTROLLER									ETHER-NET	1
MICRO INDUSTRIES	MIBII-186-151	SERIAL I/O CONTROLLER					RS-232C/422	6	1.5M			
	MIBII-186-152B	SERIAL I/O CONTROLLER	RS-232C	1	19.2k		RS-232C/422	8	1.5M			
	MIBII-186-153B	MIL-STD-1553B BUS CONTROLLER									MIL-STD-1553B	1
	MIBII-186-157A	SERIAL I/O CONTROLLER	RS-232C	17	19.2k							
	MIBII-186-158	ETHERNET CONTROLLER	RS-232C	1	19.2k						ETHER-NET	1
	MIBII-186-158B	MULTIBUS II INTERCRATE COMMUNICATION CONTROLLER									CUSTOM	—
	MIBII-186-160	CSM/SERIAL I/O CONTROLLER	RS-232C	8	—	ASYNC	RS232C/422	2	—	—		
SIEMENS	OSM-B222	SERIAL I/O CONTROLLER					RS-232C, V.24, V.11	6	—	HDLC, SDLC		
	OSM-B223	ETHERNET CONTROLLER									ETHER-NET	1
SYSTECH	HPS-6850	HOST ADAPTER FOR CLUSTER CONTROLLERS	SEE COM-MENT	SEE COM-MENT	38.4k	UNIX SYSTEM V TTY LINE DISCIPLINE						

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

ONBOARD µP	ONBOARD RAM: LOCAL	ONBOARD RAM: DUAL-PORT	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	MULTIBUS II FUNCTIONS SUPPORTED: INTERCONNECT SPACE	MULTIBUS II FUNCTIONS SUPPORTED: BUILT-IN SELF TEST	MULTIBUS II FUNCTIONS SUPPORTED: INTEL TRANSPORT PROTOCOL	CONFIGURATION VIA INTERCONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE	PRICE	COMMENTS
80386	1M		•	•	•		•	FLEX-OS	$4180	RUNS FLEX-OS LOCALLY; EXECUTES 32-BIT DMA TRANSFERS.
80186	512k, 2M		•	•	•	•		UNIX, RMX	$2345 TO $4510	HAS SUFFICIENT ONBOARD MEMORY FOR DISK CACHING OPERATIONS; ONE SBX CONNECTOR.
80186	512k		•	•	•	•	•	UNIX SYSTEM V, iRMX-286	$3695	EMPLOYS LOOK-AHEAD CACHING AND COMMAND QUEUING/OPTIMIZATION.
80186	256k		•	•	•	•	•	UNIX SYSTEM V, iRMX-286	$2695	EMPLOYS PASS-THROUGH COMMANDS AND COMMAND QUEUING.
80186	512k		•	•	•	•	•	UNIX SYSTEM V, iRMX-286	$2695	SUPPORTS PE-, NRZI-, AND GCR-FORMATTED TAPE DRIVES.
80186	128k		•	•	•	•	•	UNIX V.3, iRMX-II	~$2500	PERFORMS MULTPLE-TRACK CACHING.
80186	512k		•	•	•	•	•		$3579 TO $6654	HAS ONBOARD WINCHESTER DISK AND/OR BUBBLE CARTRIDGE.
80186	128k		•	•	•	•	•		-WFB: $2500 -WFB1: $3000	-WFB1 HAS ONBOARD 89M-BYTE HARD-DISK DRIVE.
68020	1M		•	•	•	•	•	UNIX	£2575	DRIVES TWO SCSI BUSES; EXECUTES 32-BIT DMA TRANSFERS.

CHANNELS: MAXIMUM BIT RATE (Bps)	CHANNELS: PROTOCOL	ONBOARD µP	ONBOARD RAM: LOCAL	ONBOARD RAM: DUAL-PORT	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	MULTIBUS II FUNCTIONS SUPPORTED: INTERCONNECT SPACE	MULTIBUS II FUNCTIONS SUPPORTED: BUILT-IN SELF TEST	MULTIBUS II FUNCTIONS SUPPORTED: INTEL TRANSPORT PROTOCOL	CONFIGURATION VIA INTERCONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE	PRICE	COMMENTS
		80186	512k		•	•	•	•			$3085	ALL CHANNELS OPERATE IN FULL-DUPLEX MODE AT 9.6k BAUD.
		80186	512k	512k	•	•	•	•	•	UNIX, RMX	$2952	FULL MODEM CONTROL ON EACH CHANNEL; CCI SOFTWARE SUPPORT.
		80386	1M, 4M	1M, 4M	•	•	•	•	•	UNIX, RMX	$5495 TO $6450	FULL MODEM CONTROL; 32-BIT DMA CAPABILITY; CCI SOFTWARE SUPPORT.
		80186	512k		•	•	•	•	•	UNIX, iRMX-II	~$2600	TWO SBX CONNECTORS; DIAGNOSTIC EXECUTIVE; DMA CONTROLLER.
10M	IEEE-802.3	80186	512k		•	•	•	•	•	UNIX, iRMX-II, iRMX-I	~$2400	ONE SERIAL I/O PORT; DIAGNOSTIC EXECUTIVE; OPEN-NET INTEROPERATION WITH DOS, VMS, AND XENIX.
		80186	512k		•	•	•	•	•	UNIX, RMX-286	$2600	ONBOARD DMA CONTROLLER; TWO SBX CONNECTORS.
		80C186		128k	•	•	•	•	•	UNIX	$3000	256-BYTE INSTALLABLE EPROM.
1M	MIL-STD-1553B	80C186	64k		•	•	•	•	•		$11,000	ONE DUAL-REDUNDANT 1553B BUS; BUS ANALYZER CAPABILITY; LOOP-BACK SELF-TEST CAPABILITY.
		80186	512k		•	•	•	•	•		$3000	TWO SBX CONNECTORS; ONE SERIAL PORT FOR DIAGNOSTICS/CONTROL.
10M	IEEE-802.3	80186		512k	•	•	•	•	•		$2500	
40M BYTES/SEC	CUSTOM	80C186	—	—	•	•	•	•	•		$3000	SUPPORTS HIGH-SPEED DATA TRANSFERS BETWEEN AS MANY AS 16 MULTIBUS II SYSTEMS.
		80C186	—	—	•	•	•	•	•	UNIX	$3000	ALL CSM FUNCTIONS ONBOARD; REAL-TIME CLOCK; CENTRONICS INTERFACE.
		80186	512k		•	•	•	•	•	RMOS-2	DM 5950	
10M	IEEE-802.3	80186	512k		•	•	•	•	•	RMOS-2	DM 5450	
		68020	1M		•	•	•	•	•	UNIX SYSTEM V	$3345	OPERATES WITH CLUSTER CONTROLLERS TO PROVIDE 8 TO 256 SERIAL I/O CHANNELS.

TABLE 5—MULTIBUS II GRAPHICS BOARDS

MANUFACTURER	MODEL	MAXIMUM SCREEN RESOLUTION: PIXELS,	MODE,[1]	REFRESH RATE (Hz)	BITS PER PIXEL	NUMBER OF SIMUL-TANEOUSLY DISPLAY-ABLE COLORS	NUMBER OF COLORS IN PALETTE	GRAPHICS PROCESSOR	VIDEO RAM (BYTES)	VIDEO-RAM BUS PORTS: iPSB	iLBX-II	ON-BOARD µP	ONBOARD RAM (BYTES): LOCAL	DUAL-PORT
CENTRALP AUTOMATISMES	FAB-210	1024×768,	N,	50	8	256	16M	2 82786s	4M	VIA MPC	•	80286	128k	
CODIS COMPUTER	2100	1024×768,	N,	58	7	128	256k	HD63484	4M		VIA CRTC	80286 AND 80287	1M	
MATROX ELECTRONIC SYSTEMS	MMG-640	640×480, 640×480,	N, I,	60 30	8	256	16M	HITACHI ACRTC	0.31M	•		NS32016	128k	
	MMG-1281	1280×1024,	N,	60	8	256	16M	TMS34010 AND FOUR CUSTOM GATE ARRAYS	2M, 4M	•			1M, 2M	1M
MICRO INDUSTRIES	MIBII-186-170	640×480,	N,	60	4	16	4096	82720	512k	VIA 82720		80186	—	—
OMNICOMP GRAPHICS	OMNI-2000-GDS	1280×1024, 1280×1024,	N, I,	60 30	8	256	16M	CUSTOM	2.93M	•		80386 AND 80387	4M MAX	
	OMNI-2400-GDS	1280×1024, 1280×1024,	N, I,	60 30	24	16M	16M	CUSTOM	8.32M	•		80386 AND 80387	16M MAX	
RASTER GRAPHICS	RG-500	1024×768,	N,	60	8	256	4096	TMS34010	1M	VIA 30410			256k, 1M	
STELLARCIM	SCIM-DGB	640×512,	N,	60	4	16	4096	2 82716s	2×512k	VIA 82716		80186	128k	
	SCIM-DGB-A, -B, -C	1024×1024,	N, I,	60	8	256	4096	2 82786s	-A: 2×1M -B: 2×2M -C: 2×4M	•		80286	128k	

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION

NOTES: 1. I = INTERLACED, N = NONINTERLACED.

TABLE 6—MULTIBUS II ANALOG I/O BOARDS

MANUFACTURER	MODEL	ANALOG INPUT CHANNELS: NUMBER: SINGLE ENDED	DIFFER-ENTIAL	A/D RESOL-UTION	INPUT RANGES	PROGRAM-MABLE GAIN AMPLIFIER[2]	SAMPLING RATE: SINGLE CHANNEL	SWITCHED CHANNELS	ANALOG OUTPUT CHANNELS: NUMBER	D/A RESOL-UTION	OUTPUT RANGES	SETTLING TIME
CENTRALP AUTOMATISMES	FAB-513	16		12	±10.24V		50 kHz	—				
	FAB-514	16	16	12	±10 mV TO ±10V	SPGA	10 Hz	10 Hz				
	FAB-515	8		12	±10V		—	50 kHz				
	FAB-530								16	12	±10.24V	40 µSEC (TYP)
CONCURRENT TECHNOLOGIES	AI-CBX-080	80	40	12	±10V, 10V, −10V	SPGA	80 kHz	40 kHz				
	AI-186-080	80	40	12	±10V, 10V, −10V	SPGA	80 kHz	40 kHz				
	IO-186-070	16	8	12	10V, −10V		100 kHz	50 kHz	6	12	10V, −10V	1.5 µSEC
	AO-CBX-016, -032								-016: 16 -032: 32	12	10V	1.5 µSEC
	AO-186-032								32	12	10V	1.5 µSEC
DATA TRANSLATION	DT-2401	32	16	12	1.25V, 2.5V, 5V, 10V, ±1.25V, ±2.5V, ±5V, ±10V	SPGA	40 kHz	40 kHz	2	12	5V, 10V, ±5V, ±10V	20 µSEC/20V 3 µSEC/100 mV
	DT-2402-F	16	8	16	1.25V, 2.5V, 5V, 10V, ±1.25V, ±2.5, ±5V, ±10V	SPGA	125 kHz	125 kHz	2	12	5V, 10V, ±5V, ±10V	20 µSEC/20V 3 µSEC/100 mV
	DT-2405	32	16	12	0.02V, 0.1V, 1V, 10V, ±0.02V, ±0.1V, ±1V, ±10V	SPGA	40 kHz	40 kHz	2	12	5V, 10V, ±5V, ±10V	20 µSEC/20V 3 µSEC/100 mV
	DT2407		4	16	±10V		100 kHz	100 kHz	2	12	5V, 10V, ±5V, ±10V	20 µSEC/20V 3 µSEC/100 mV
	DT2408	4		12	10V, ±10V		100 kHz	100 kHz	2	12	5V, 10V ±5V, ±10V	20 µSEC/20V 3 µSEC/100 mV
	DT-2805-5716A		8	16	0.02V, 0.1V, 1V, 10V, ±0.02V, ±0.1V, ±1V, ±10V	SPGA	25 kHz	25 kHz	2	12	5V, 10V, ±5V, ±10V	20 µSEC/20V 3 µSEC/100 mV

VIDEO OUTPUTS	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	INTER-CONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL	CONFIG-URATION VIA INTER-CONNECT SPACE	GRAPHICS LANGUAGES SUPPORTED	PRICE	COMMENTS
DIGITAL, RS-170	•	•	•	•	•	CGI	$8000	
RS-170	•	•		•	•	CGI	DM 15,000	COUPLES TO A CPU BOARD VIA THE iLBX-II BUS TO PROVIDE A GRAPHICS SUBSYSTEM WITH INTERFACES FOR DIGITIZER, MOUSE, AND KEYBOARD.
—	•	•			•	PGC	$2495	
ANALOG RGB	•	•	•	•	•	LIB-SHELL INTERFACE	$4995	DRAWS 60,000 2-D AND 30,000 3-D VECTORS/SEC. BITBLT OPERATIONS AT 12.5M 8-BIT PIXELS/SEC.
RS-343 RGB	•	•	•	•	•	—	$3000	DOUBLE-BUFFERED 640 x 480 x 4-BIT PIXELS, QUAD BUFFERED 512 x 512 x 4-BIT PIXELS. SERIAL-PORT AND FOUR 28-PIN JEDEC MEMORY SITES.
RS-343 RGB	•	•				OKS (SUPERSET OF ANSI GKS)	$7860 TO $17,300	DOUBLE-BUFFERED 1280 x 1024 x 8-BIT PIXELS AND TWO OVERLAY PLANES. OKS FIRMWARE. IMAGING AND 3-D WIREFRAME MICROCODE.
RS-343 RGB	•	•		•		NATIVE COMMANDS, OKS (SUPERSET OF ANSI GKS)	$9900 TO $25,380	DOUBLE-BUFFERED 1280 x 1024 x 24-BIT PIXELS AND FOUR OVERLAY PLANES; CONFIGURABLE FOR 3-CHANNEL, 8-BIT-PIXEL OPERATION; IMAGING AND 3-D WIREFRAME MICROCODE; HARDWARE PAN, ZOOM, VECTOR GENERATION, AND IMAGE FILTERING; 10M PIXEL/SEC VECTOR DRAWING.
TTL, RS-343 RGB	•	•	•	•	•	CUSTOM	~$2000 TO ~$4000	SERIAL I/O PORT FOR DEBUGGING.
ANALOG OR DIGITAL RGB	•	•	•	•	•	CUSTOM	$3000	CONTROLS TWO INDEPENDENT MONITORS WITH 512k BYTES OF VIDEO RAM PER MONITOR; CAN SUPPORT NALPS, GKS, AND VDI GRAPHICS LANGUAGES.
ANALOG OR DIGITAL RGB	•	•	•	•	•	CUSTOM	-A: $3500 -B: $4000 -C: $4500	CONTROLS TWO INDEPENDENT MONITORS WITH EITHER 1M, 2M, OR 4M BYTES OF VIDEO RAM PER MONITOR; CAN SUPPORT NALPS, GKS, AND VDI GRAPHICS LANGUAGES.

ISOLATION BETWEEN ANALOG I/O AND MULTIBUS II GROUND	ONBOARD µP	ONBOARD RAM BYTES): LOCAL	DUAL-PORT	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	INTER-CONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL	CONFIG-URATION VIA INTER-CONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE[1]	PRICE	COMMENTS
500V					•			•	iRMX-1, iRMX-2	$4100	
500V					•			•	iRMX-1, iRMX-2	$2300	500V CHANNEL-TO-CHANNEL ISOLATION VIA RELAYS.
	8032	32k		•	•	•	•	•	iRMX-1, iRMX-2	$3300	INTERNAL/EXTERNAL TRIGGERS; iLBX-II INTERFACE.
500V					•			•	iRMX-1, iRMX-2	$3100	OUTPUT TEST CAPABILITY.
	8031	64k			•	•		•		$2300	INTERFACES VIA THE cCBX EXPANSION BUS.
	80186	256k	256k	•	•	•	•	•		$3200	cCBX INTERFACE AND TWO SERIAL I/O PORTS.
	80186	256k	256k	•	•	•	•	•		$2950	48 DIGITAL I/O LINES AND TWO SERIAL PORTS.
	8031	64k			•	•		•		-016: $1950 -030: $2300	INTERFACES VIA THE cCBX EXPANSION BUS.
	80186	256k	256k	•	•	•	•	•		$3200	cCBX INTERFACE AND TWO SERIAL I/O PORTS.
					•					$1695	32 DIGITAL IO LINES AND A PACER CLOCK.
					•					$2045	32 DIGITAL I/O LINES AND A PACER CLOCK.
					•					$1795	32 DIGITAL I/O LINES AND A PACER CLOCK.
					•					$2865	32 DIGITAL I/O LINES AND A PACER CLOCK.
					•					$2195	32 DIGITAL I/O LINES AND A PACER CLOCK; SIMULTANEOUS SAMPLE/HOLD ON ALL INPUT CHANNELS.
					•					$2960	32 DIGITAL I/O LINES AND A PACER CLOCK.

TABLE 6—MULTIBUS II ANALOG I/O BOARDS *(Continued)*

MANUFACTURER	MODEL	ANALOG INPUT CHANNELS: NUMBER: SINGLE ENDED	DIFFERENTIAL	A/D RESOLUTION	INPUT RANGES	PROGRAMMABLE GAIN AMPLIFIER[2]	SAMPLING RATE: SINGLE CHANNEL	SWITCHED CHANNELS	ANALOG OUTPUT CHANNELS: NUMBER	D/A RESOLUTION	OUTPUT RANGES	SETTLING TIME
ECKELMANN	EM-ADA-01	16	8	12	±10V, 0 TO 20 mA, 4 TO 20 mA	SPGA	17.5 kHz	6.7 kHz	8	12	±10V, 0 TO 20 mA, 4 TO 20 mA	20 μSEC
EFISYSTEME	CESA-2-01	32	16	12	10 mV TO 10V, 5V, 10V, ±2.5V, ±5V	SPGA	100 kHz	80 kHz				
	CESA-2-02-0	64	32	12	10 mV TO 10V	SPGA	100 kHz	80 kHz				
	CESA-2-02-2, -4	64	32	12	10 mV TO 10V	SPGA	100 kHz	80 kHz	-2: 2 -4: 4	12	5V, 10V, ±2.5V, ±5V, ±10V	5 μSEC
MICRO INDUSTRIES	MIBII-186-140	32	16	12	5V, ±5V	LPGA	20 kHz	20 kHz				
	MIBII-186-140B	64	32	12	5V, ±5V	LPGA	50 kHz	50 kHz				
	MIBII-186-141B	64	32	14	5V, ±5V	LPGA	50 kHz	—				
	MIBII-186-142B	64	32	16	5V, ±5V	LPGA	50 kHz	50 kHz				
	MIBII-186-145								16	12	5V, ±5V, 4 TO 20 mA	—
	MIBII-186-145B								16	12	5V, ±5V	—

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

NOTES: 1. BOARDS WITH AN ONBOARD μP GENERALLY EXECUTE A HIGH-LEVEL COMMAND SET.
2. LPGA = LINK/RESISTOR-PROGRAMMABLE GAIN AMPLIFIER, SPGA = SOFTWARE-PROGRAMMABLE GAIN AMPLIFIER.

TABLE 7—MULTIBUS II DIGITAL I/O BOARDS

MANUFACTURER	MODEL	LINES: INPUTS	OUTPUTS	INPUT/OUTPUTS	HANDSHAKE	INPUT-VOLTAGE RANGE	OUTPUT-VOLTAGE RANGE	OUTPUT CURRENT: SINK	SOURCE	ISOLATION BETWEEN DIGITAL I/O AND MULTIBUS II GROUND: VOLTAGE	TYPE	ONBOARD μP
CENTRALP AUTOMATISMES	FAB-401	32				0 TO 24V				2.5V AC	OPTOCOUPLER	
	FAB-420		32				0 TO 220V	0.5A	0.5A	2.5V AC	RELAY AND OPTOCOUPLER	
CONCURRENT TECHNOLOGIES	IO-CBX-120	10	15	95	10	TTL	TTL	24 mA	15 mA			8031
	IO-188-120	10	15	95	10	TTL	TTL	24 mA	15 mA			80188
ECKELMANN	EM-IO-01	24	16			24V DC	24V DC		500 mA	500V	OPTOCOUPLER	
EFISYSTEME	CESD-2-01, -02			-01: 128 -02: 64		TTL	TTL	24 mA	2.6 mA			80186
MICRO INDUSTRIES	MIBII-186-111, -112			-111: 96 -112: 48		TTL	30V	40 mA	—			80186
	MIBII-186-115B	32	32			TTL	—	100 mA	100 mA	250V	RELAY	80C186

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

NOTE: 1. BOARDS WITH AN ONBOARD μP GENERALLY EXECUTE A HIGH-LEVEL COMMAND SET.

TABLE 8—MULTIBUS II SPECIAL-FUNCTION BOARDS

MANUFACTURER	MODEL	DESCRIPTION	ONBOARD μP	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	INTERCONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL
ANALOG DEVICES	RTI-980	DIGITAL SIGNAL PROCESSING BOARD WITH PRIVATE BUS EXTENSION	80188 AND ADSP2100	•	•		•
	RTI-984	512×512-PIXEL FRAME GRABBER WITH 256 GREY-SCALE LEVELS			•		
BICC-VERO	34-61333L	PROTOTYPING MODULE WITH MULTIBUS II INTERFACE		•	•	•	

ISOLATION BETWEEN ANALOG I/O AND MULTIBUS II GROUND	ONBOARD μP	ONBOARD RAM (BYTES)		MULTIBUS II FUNCTIONS SUPPORTED				CONFIGURATION VIA INTERCONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE[1]	PRICE	COMMENTS
		LOCAL	DUAL-PORT	MESSAGE PASSING	INTERCONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL				
500V					•			•	RMX-86	DM 2880 TO DM 3450	ACCEPTS EXTERNAL SIGNAL-CONDITIONING AND INPUT-ISOLATION MODULES.
	80186	128k		•	•	•		•		~Fr 28,000	OPTIONAL CSM FUNCTIONS; ACCEPTS EXTERNAL SIGNAL-CONDITIONING AND INPUT-ISOLATION MODULES.
	80186	128k		•	•	•		•		~Fr 30,000	OPTIONAL CSM FUNCTIONS; ACCEPTS EXTERNAL SIGNAL-CONDITIONING AND INPUT-ISOLATION.
	80186	128k		•	•	•		•		-2: ~Fr 32,000 -4: ~Fr 35,000	OPTIONAL CSM FUNCTIONS; ACCEPTS EXTERNAL SIGNAL-CONDITIONING AND I/O-ISOLATION MODULES.
	80186	512k		•	•	•	•	•	UNIX, RMX	$3000	TWO SBX CONNECTORS.
	80C186	SEE COMMENT		•	•	•	•	•	UNIX, RMX	$3000	TWO 28-PIN JEDEC EPROM/STATIC-RAM SITES.
	80C186	SEE COMMENT		•	•	•	•	•	UNIX, RMX	$3500	DMA CAPABILITY AND TWO SBX CONNECTORS; TWO 28-PIN JEDEC EPROM/STATIC-RAM SITES.
	80C186	SEE COMMENT		•	•	•	•	•	UNIX, RMX	$4000	TWO 28-PIN JEDEC EPROM/STATIC-RAM SITES.
	80186	512k		•	•	•	•	•	UNIX, RMX	$3000	DMA CAPABILITY AND TWO SBX CONNECTORS.
	80C186	SEE COMMENT		•	•	•	•	•	UNIX, RMX	$3000	I/O ACCESS VIA P2 CONNECTOR; TWO 28-PIN JEDEC EPROM/STATIC-RAM SITES.

ONBOARD RAM (BYTES)		MULTIBUS II FUNCTIONS SUPPORTED				CONFIGURATION VIA INTERCONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE[1]	PRICE	COMMENTS
LOCAL	DUAL-PORT	MESSAGE PASSING	INTERCONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL				
		•	•			•	iRMX-1, iRMX-2	$1200	PROGRAMMABLE INPUT FILTERING; EIGHT INPUTS CAN GENERATE INTERRUPTS; INPUT SELF TEST AVAILABLE.
			•			•	iRMX-1, iRMX-2	$1500	AUTOCONTROL OF RELAY COIL OPERATION.
64k MAX			•	•		•		$1325	INTERFACES VIA cCBX BUS.
	8k (64k MAX)	•	•	•	•	•		$2450	cCBX EXPANSION BUS AND TWO RS-232C I/O PORTS.
			•			•	RMX-86	DM 2640 TO DM 3140	EXTERNAL DRIVERS, LEVEL SHIFTERS, AND FILTERING.
—		•	•	•		•		-01: ~Fr 17,000 -02: ~Fr 19,000	OPTIONAL CSM FUNCTIONS; CDI-32 COMPANION BOARD ACCOMMODATES ISOLATION AND SIGNAL-CONDITIONING MODULES FOR ALL I/O LINES.
512k SEE COMMENT		•	•	•	•	•	UNIX, RMX	$2500	DMA CAPABILITY; TWO SBX CONNECTORS, ONE SERIAL I/O PORT, AND FOUR 28-PIN JEDEC MEMORY SITES; MIBII-186-112 HAS A PROGRAMMABLE TIMER.
SEE COMMENT		•	•	•	•	•	UNIX, RMX	$2500	LOOP-BACK SELF TEST; I/O ACCESS VIA P2 CONNECTOR; TWO 28-PIN JEDEC EPROM/STATIC-RAM SITES.

CONFIGURATION VIA INTERCONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE	PRICE	COMMENTS
	iRMXII.3 (DEVELOPMENT TOOLS RUNNING UNDER iRMX286 AND PC/DOS)	$5995	ZERO-WAIT-STATE ACCESS TO 16k×16-BIT DATA MEMORY, 16k×24-BIT PROGRAM MEMORY, AND TWO BANKS OF 16k×16-BIT PROGRAM/DATA MEMORY; CAPABLE OF 8 MIPS; PROGRAMMABLE ADDRESS GENERATOR AND PROGRAM SEQUENCER ON PRIVATE BUS.
•	iRMXII.3	$3995	DUAL CAMERA INPUT AND RS-170 VIDEO OUTPUT; PHASE LOCK TO VIDEO SOURCE OR CAMERA PIXEL CLOCK; 10-MHz SAMPLING AT 50- OR 60-Hz FRAME RATE; PROGRAMMABLE WINDOW DIGITIZATION; 512×512×1-BIT OVERLAY PLANE. EIGHT LOOK-UP TABLES.
•	PC/DOS	£953.25	HAS MULTIBUS II iPSB INTERFACE, 8751 MICROCONTROLLER TO SUPPORT INTERCONNECT SPACE AND BIST FUNCTIONS, AND A SOCKET FOR A VL82C389 MPC; USER-DEFINED MICROCONTROLLER I/O PORTS; FOUR VOLTAGE PLANES AND SMD DECOUPLING CAPACITORS.

TABLE 8—MULTIBUS II SPECIAL-FUNCTION BOARDS *(Continued)*

MANUFACTURER	MODEL	DESCRIPTION	ONBOARD µP	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	INTERCONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL
CENTRAL DATA	CD-22-6400	SBX MOTHER BOARD	80186	•	•	•	•
	CD-22-6410	PROTOTYPING BOARD	80186	•	•	•	•
CENTRALP AUTOMATISMES	FAB-540	2-AXIS DC SERVOMOTOR CONTROLLER	8032	•	•	•	•
	FAB-610	VIDEO DATA-ACQUISITION BOARD			•		
	MPI	iPSB I/O REPLIER MODULE		•	•		
CREONICS	MB2-E00, EGO, -EOC, -EGC	2-AXIS DIGITAL SERVOMOTOR CONTROLLER	80186		•		
ECKELMANN	EM-ARI01	2-AXIS POSITION TRANSDUCER AND DAC			•		
FURRER-GLOOR	MB2-LNK-1	BUS COUPLER BETWEEN iPSB AND EUROLOG (ECB) BUS	Z80 OR Z280	•	•	•	
GET ENGINEERING	10054501	NTDS (MIL-STD-1397) INTERFACE ADAPTER	80186	•	•	•	•
MICRO INDUSTRIES	MIBII-32020, -32025	2-CHANNEL DIGITAL SIGNAL PROCESSING BOARD	-32020: 4 TMS32020s -32025: 4 TMS32025s	•	•	•	•
PLANNING RESEARCH	PSBA-100	PARALLEL SYSTEM BUS ANALYZER	80186	•	•	•	•
SIEMENS	OSM-B507-A1, -A3	BUS COUPLER BETWEEN iPSB AND AMS OR SMP BUSES					
STELLARCIM	MATE-1000	MULTIBUS II BUS ANALYZER	80186	•	•	•	•
SYSTECH	HPS-6850	HOST ADAPTER FOR TERMINAL-CONTROLLERS CLUSTER	68020	•	•	•	•
TRANS-MAGNETICS	5402C-1	2-SPEED SYNCHRO/RESOLVER INPUT	—	—	—	—	—
	5402C-6	2-CHANNEL SYNCHRO/RESOLVER OUTPUT AND SINGLE SYNCHRO/RESOLVER INPUT	—	—	—	—	—
	5402C-8	2-CHANNEL SYNCHRO/RESOLVER INPUT	—	—	—	—	—
	5402C-9	3-CHANNEL 60-Hz SYNCHRO INPUT	—	—	—	—	—
	5402C-12	2-CHANNEL, 2-SPEED SYNCHRO/ RESOLVER INPUT	—	—	—	—	—
	54020C-14	3-CHANNEL SYNCHRO/RSOLVER OUTPUT	—	—	—	—	—
	5402C-16	2-SPEED SYNCHRO/RESOLVER OUTPUT	—	—	—	—	—
	5402C-17	3-CHANNEL SYNCHRO/RESOLVER INPUT	—	—	—	—	—
	5402C-19-1	5-VA SYNCHRO OUTPUT WITH WRAPAROUND SELF TEST	—	—	—	—	—
	5402C-22	3-CHANNEL RESOLVER INPUT WITH TURN COUNTERS	—	—	—	—	—
	5402C-23	2-CHANNEL SYNCHRO/RESOLVER INPUT AND SINGLE-CHANNEL SYNCHRO/ RESOLVER OUTPUT	—	—	—	—	—
	5402C-25	QUAD D/A OUTPUT	—	—	—	—	—
	5402C-26	2-CHANNEL SYNCHRO/RESOLVER INPUT WITH 1.2-VA REFERENCE	—	—	—	—	—
	5402C-11REF	5-VA REFERENCE SUPPLY	—	—	—	—	—

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

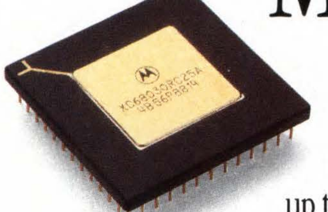
CONFIGURATION VIA INTERCONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE	PRICE	COMMENTS
		$2455 TO $2730	SUPPORTS AS MANY AS FOUR 8-BIT OR 16-BIT SBX MODULES; INCLUDES MPC, 512k BYTES OF ZERO-WAIT-STATE DYNAMIC RAM AND A CENTRONICS PRINTER PORT; FIRMWARE SUPPORT FOR A REAL-TIME OPERATING SYSTEM; OPTIONAL 82258 DMA CONTROLLER.
USER DEFINED		$2505 TO $2780	INCLUDES MPC AND 512k BYTES OF ZERO-WAIT-STATE DYNAMIC RAM; OPTIONAL 82258 DMA CONTROLLER; FIRMWARE SUPPORT FOR A REAL-TIME OPERATING SYSTEM.
•	iRMX-1, iRMX-2	$3100	CONTROLS SPEED AND POSITION OF TWO DC SERVOMOTORS VIA INCREMENTAL ENCODERS; ONBOARD LOGICAL I/O CAN DETECT FAULTS AND CONTROL MOTOR TORQUE OR POWER.
•	iRMX-1, iRMX-2	$5300	OPERATES AS PRIMARY OR SECONDARY MASTER ON THE iLBX II BUS; DIGITIZES VIDEO SIGNALS DIRECTLY TO iLBX-II BUS MEMORY; PLUG-IN MODULES ADAPT INPUT TO A VARIETY OF CAMERA TYPES; PROGRAMMABLE WHITE LEVEL FOR EACH PIXEL IN A LINE.
•		$230	THIS PIGGYBACK BOARD PROVIDES A STANDARD INTERFACE BETWEEN THE iPSB AND SIMPLE I/O BOARDS; PROVIDES MULTIPLEXED ADDRESS/DATA BUS TO THE I/O BOARD; IS CONFIGURABLE VIA ONBOARD REGISTERS.
•		-E00: $2245 -EG0: $2390 -EOC: $2670 -EGC: $2815	-E00: PROVIDES POSITION, VELOCITY, ACCELERATION AND DECELERATION CONTROL; OPTOISOLATED I/O FOR DIFFERENTIAL ENCODERS, ±10V DRIVE SIGNALS AND LIMIT SWITCHES; SELF-TUNING GAIN ADJUSTMENT -EGO: = -E00 PLUS ELECTRONIC GEARING TO SLAVE DRIVES TO A MASTER ENCODER. -EOC: = -E00 PLUS ELECTRONIC CAM-PROFILE FOLLOWING CAPABILITY. -EGC: = -E00 PLUS ELECTRONIC GEARING TO SLAVE DRIVES TO A MASTER ENCODER AND ELECTRONIC CAM-PROFILE FOLLOWING CAPABILITY.
•	RMX-86	DM 2880	HAS TWO 32-BIT UP/DOWN COUNTERS, TWO 16-BIT D/A CONVERTERS WITH ±10V OUTPUT RANGE, AND TWO POSITION INDICATORS.
•		SFr 3000	ALLOWS YOU TO USE THE EUROLOG (ECB) BUS AS A LOW-COST I/O CHANNEL FOR MULTIBUS II SYSTEMS; BUS-TO-BUS COMMUNICATION VIA 256k BYTES OF DUAL-PORT RAM.
•	RMX-86	$4385	PROVIDES A FULL-DUPLEX 32-BIT INTERFACE BETWEEN AN NTDS COMPUTER OR PERIPHERAL CHANNEL AND A MULTIBUS II SYSTEM; CONFIGURABLE TO EMULATE NTDS DEVICES; OPERATES IN A FAST OR SLOW NTDS ENVIRONMENT.
•		-32020: $7500 -32025: $8000	HAS TWO 16-BIT 50-kHz D/A CONVERTERS, AND 4k BYTES OF RAM THAT IS MAPPABLE TO THE MULTIBUS II MEMORY SPACE; LOOP-BACK SELF-TEST CAPABILITY; I/O ACCESS VIA P2 CONNECTOR; ONBOARD DSP FIRMWARE.
		$4995 TO $9995	SELECTIVE CAPTURE OF iPSB CYCLES, 16 TRIGGER LEVELS, 32k×56-BIT CAPTURE MEMORY; HAS MPC AND TWO SERIAL I/O CHANNELS.
		-A1: DM 500 -A3: DM 6195	PIGGYBACKS ONTO A CPU CARD VIA AN ONBOARD MODULE EXPANSION (OME) INTERFACE; -A3 VERSION PROVIDES 8M BYTES OF DYNAMIC RAM.
•		<$1500 AVAILABLE OCT 88	100-MHz SAMPLE RATE; 16 INPUT CHANNELS; 8k-BIT/CHANNEL TRACE MEMORY: INTERNAL/EXTERNAL CLOCKS; 2-LEVEL TRIGGERING; SCSI PORT TO CONTROL COMPUTER.
•	UNIX SYSTEM V	$3345	ALLOWS CONFIGURATION OF A DISTRIBUTED TERMINAL MULTIPLEXER SUBSYSTEM CAPABLE OF SUPPORTING 8 TO 256 USERS.
—	—	$1750	16-BIT OUTPUT. 20 ARC-SECOND ACCURACY; SELF TEST; VELOCITY OUTPUT; STANDARD GEAR RATIOS FROM 9:1 TO 64:1; TRANSFORMER ISOLATED.
—	—	FROM $1900	10-, 12-, 14-, OR 16-BIT TO 1 ARC-MINUTE ACCURACY; 380 TO 2500 Hz; TRANSFORMER ISOLATED.
—	—	FROM $1600	10-, 12-, 14- OR 16-BIT TRACKING COVERTERS; 380 TO 2500 Hz; TO 45 ARC-SECOND ACCURACY; TRANSFORMER ISOLATED.
—	—	FROM $1900	10-, 12- OR 14-BIT; 47 TO 440 Hz; TRANSFORMER ISOLATED.
—	—	$2550	TRACKING CONVERTERS WITH 16-BIT OUTPUT; 20 ARC-SECOND ACCURACY; SELF TEST; VELOCITY OUTPUT; STANDARD GEAR RATIOS FROM 9:1 TO 64:1; TRANSFORMER ISOLATED.
—	—	FROM $1900	10-, 12- OR 14-BIT. TO 4 ARC-MINUTE ACCURACY; 380 TO 2500 Hz; TRANSFORMER ISOLATED.
—	—	FROM $1900	STANDARD GEAR-SPEED MULTIPLIERS FROM 8:1 TO 64:1; 10-, 12-, 14- OR 16-BIT COARSE INPUT; COARSE ACCURACY TO 1 ARC-MINUTE; TRANSFORMER ISOLATED.
—	—	FROM $1900	10-, 12-, 14- OR 16-BIT TRACKING CONVERTERS; 380 TO 2500 Hz; TO 45 ARC-SECOND ACCURACY; TRANSFORMER ISOLATED.
—	—	$2100	12- OR 14-BIT SYNCHRO OUTPUT CAN DRIVE THREE TORQUE RECEIVERS IN PARALLEL; ONBOARD 12-BIT WRAPAROUND SELF TEST.
—	—	$2600	THREE 10-, 12- OR 14-BIT TRACKING CONVERTERS, AND THREE ASSOCIATED 12-BIT TURN COUNTERS WITH PRESET CAPABILITY.
—	—	FROM $2000	10-, 12-, 14- OR 16-BIT; TO 1 ARC-MINUTE ACCURACY; 380 TO 2500 Hz; TRANSFORMER ISOLATED.
—	—	$3400	FOUR 12-BIT D/A CONVERTERS, WITH 2's-COMPLEMENT CODING; 25-μSEC CONVERSION; 15-mA OUTPUTS.
—	—	FROM $2100	TWO 10-, 12-, 14- OR 16-BIT TRACKING CONVERTERS WITH 1.2-VA REFERENCE SUPPLY; TRANSFORMER ISOLATED.
—	—	$550	5-VA OUTPUT AT 6V, 11V, 26V, OR 115V RMS AND AT 400 Hz, 1 kHz, 2.4 kHz, OR 2.6 kHz; OTHER OUTPUT VOLTAGES AND FREQUENCIES BY SPECIAL ORDER.

TABLE 9—MULTIBUS II CENTRAL SERVICES MODULES

MANUFACTURER	MODEL	MULTIBUS II FUNCTIONS SUPPORTED: MESSAGE PASSING	INTER-CONNECT SPACE	BUILT-IN SELF TEST	INTEL TRANSPORT PROTOCOL	CONFIG-URATION VIA INTER-CONNECT SPACE	OPERATING SYSTEMS FOR WHICH DRIVERS ARE AVAILABLE	PRICE	COMMENTS
GEOMELEC/ RENAULT AUTOMATION	RA-CSM		•		•			~FR 3000	
INTEL	iSBC-CSM-001	•	•	•		•	iRMX, iRMK	$995	INTERFACE FOR A MULTIBUS I CHASSIS.
MICROBAR SYSTEMS	MT-3200	•						$495	
	MT-3201	•						$495	MOUNTS ON REAR OF BACKPLANE.
	MT-3202C		•	•		•	UNIX, VRTX, RMX	$595	MOUNTS ON REAR OF BACKPLANE; INCLUDES REAL-TIME CLOCK.
MICRO INDUSTRIES	MIBII-186-160	•	•	•	•	•	UNIX	$3000	80C186 μP, REAL-TIME CLOCK, CENTRONICS PORT, EIGHT ASYNCHRONOUS AND TWO SYNCHRONOUS/ASYNCHRONOUS SERIAL I/O PORTS, AND TWO 28-PIN JEDEC MEMORY SITES.
	MIBII-200	•	•	•	•	•		$1500	
SIEMENS	OSM-B500-A1		•	•		•	RMOS	DM 2500	INCLUDES REAL-TIME CLOCK, RESET, AND TIME-OUT DETECTION.
STELLARCIM	MCSM, MCSMA							MCSM: $400 MCSMA: $450	MOUNTS ON REAR OF BACK-PLANE; ADJUSTABLE LOW-VOLTAGE SENSING OF 5V SUPPLY; FACTORY SETTABLE ID ASSIGNMENT TABLE; OUT-PUT CONNECTIONS FOR LEDs; JUMPER-CONFIGURED COLD/WARM START AND TIMEOUT ENABLE/DISABLE. MCSMA: = MCSM PLUS ADJUSTABLE AC POWER FAIL/LOW VOLTAGE MONITOR.
	MCSMT, MCSMAT							$500 $550	MCSMT: = MCSM PLUS REAL-TIME CLOCK. MCSMAT: = MCSMA PLUS REAL-TIME CLOCK.

— = PARAMETERS UNSPECIFIED OR UNCLEAR AT TIME OF PUBLICATION.

MicroCASE supports the 68030 with 25 MHz emulation.



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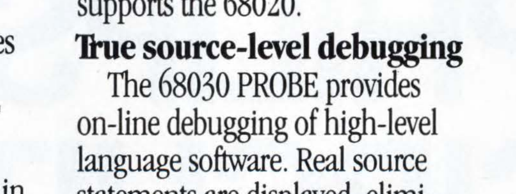

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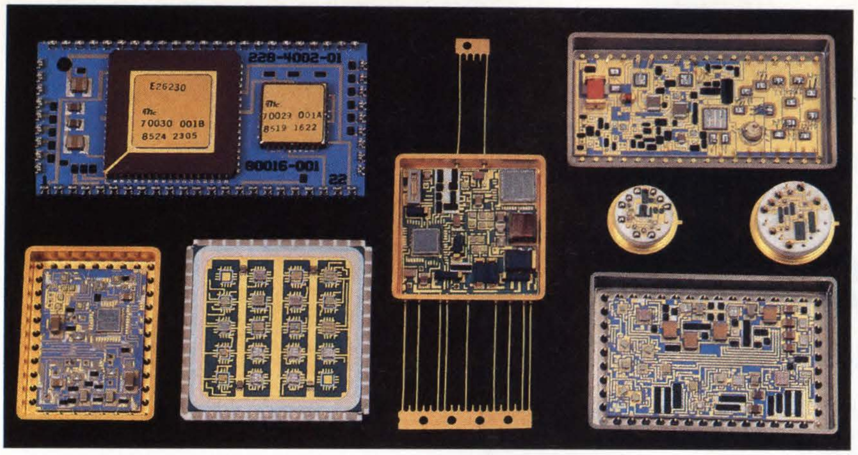

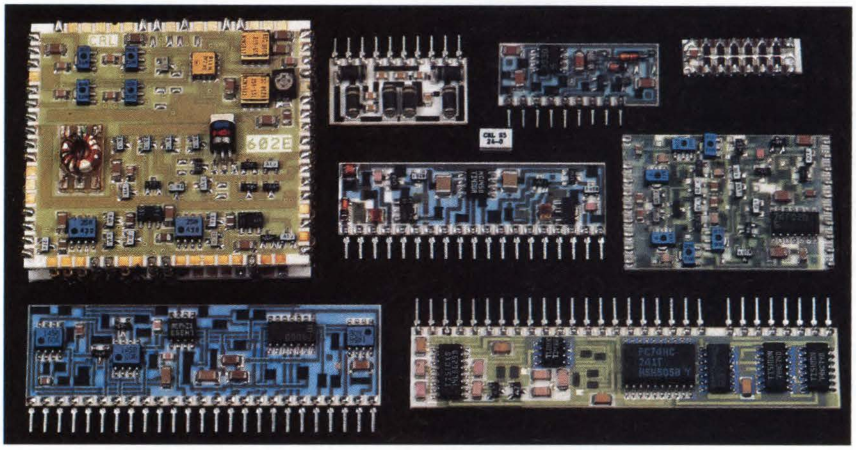

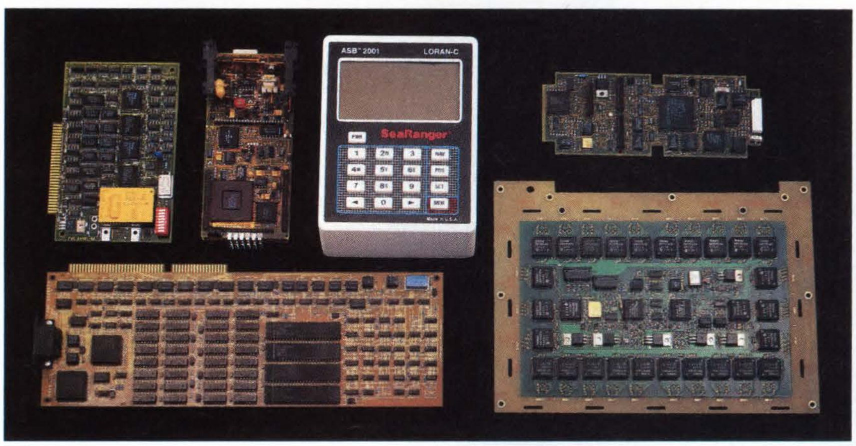

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- SBX CONNECTOR
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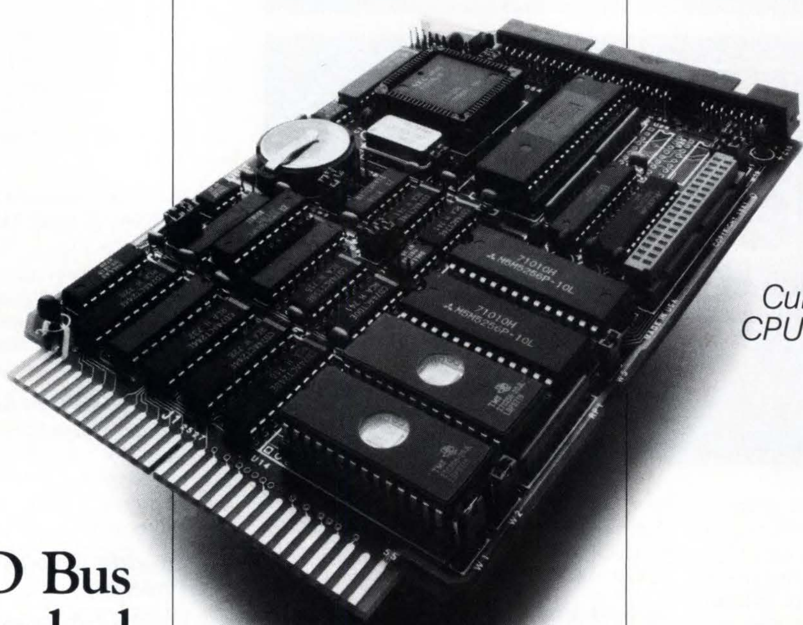

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Use power FETs to design ac-line power choppers

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Tom Visel, *VLSI Technology Inc*

FET power controllers for use with the ac mains are capable of producing either variable dc voltages or ac power of variable voltage or frequency. To design power controllers (or choppers) that function correctly, you must examine several key factors, some of which are interrelated. For example, you must consider FET-device selection, the choice of a gate driver for driving high capacitance, magnetics design and selection, input and output filtering, device paralleling, and the method of control modulation and isolation.

You can use power FETs to design the power circuitry of a 29-kHz switching controller that is capable of handling 10A from the 110V ac mains. Because the frequency niche for power FETs used in switching circuits is usually well above 100 kHz, you could argue that a controller working at only 29 kHz might be better served by bipolar transistors. After all, designers routinely use bipolar transistors at switching frequencies of 80 kHz and higher. The duty cycle, however, changes the ground rules. Most power switching circuits have duty cycles in the 40 to 60% range. The switching-controller design presented here allows duty cycles to range from 0 to 100%. If the duty cycle is controlled by a 7-bit divider, for example, the inductor circuit could have significant frequency content in the 3.5-MHz range.

It's worth noting that the rather odd switching frequency of 29 kHz was chosen not for its intrinsic value to the design, but because we had a large stock of 29-kHz oscillator modules on hand. You can adjust the circuit values to accommodate other frequencies that are reasonably close (within ±10%) to 29 kHz.

Analyzing the power chopper

Most power-controller designs work on the basis of a chopper, a circuit configuration that "chops" an analog signal or dc supply into small units of time. The chopper acts as a single-throw or double-throw switch to turn the signal (or power supply) on and off for short intervals **(Fig 1)**. By varying the on-to-off ratio and integrating the output, you can vary the dc level at the output.

A power chopper is a variation of a basic chopper circuit that's used to obtain dc output voltages that

The value of a power chopper is that it lets you vary the output voltage without incurring losses caused by resistive elements.

are a fixed or varying fraction of the supply voltage. A chopper is valuable because it lets you vary the output voltage, yet lose little power to circuit resistance. The switches (transistors) used in a chopper circuit are either fully closed or fully open. **Fig 2** shows the typical waveforms of a power chopper. You can use a chopper to obtain a dc voltage that is smoothly variable from 0 to 110V, or to create an ac voltage that varies from 0 to 110V rms at 60 or 400 Hz. Although the chopper's power circuit may not be much different in these two applications, the control circuitry that modulates the on/off ratio is significantly different.

For a dc-output chopper, the load should ideally see a pure dc level; any variations caused by voltage or current spikes are undesirable. You can either filter out any variations caused by the chopping action or use the variations to transfer energy from the power source to the load. You can use a switching capacitor or switching inductor for the latter purpose. Low-power choppers frequently use a capacitor for energy transfer. Because circuits that include capacitors encounter losses, high-power choppers must use inductors to transfer power-supply energy to the load. Inductors can transfer 100 to 200V at 10 to 20A and are less expensive than any equivalent capacitor configuration.

You should view the inductor in a power chopper as an energy storage and transfer device, not as a filter. If the inductor were merely a filter, you could remove it and the circuit would still function, albeit with noise. Actually, most chopper and power-supply designs use several inductors—one in the switching circuit for energy storage, and one in the power-input and -output circuits for filtering—and their design is quite different. The voltage swings in the energy-storage inductor can easily range to the full supply voltage and beyond. The filter inductors only see voltage swings whose magnitude is that of the residual ripple voltage, and

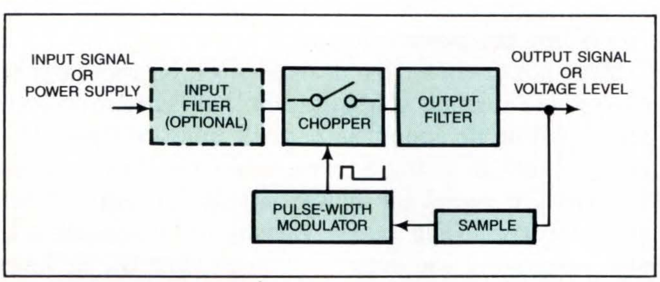

***Fig 1—The basic chopper circuit** includes a switching element whose on-off ratio is controlled by the action of a pulse-width modulator.*

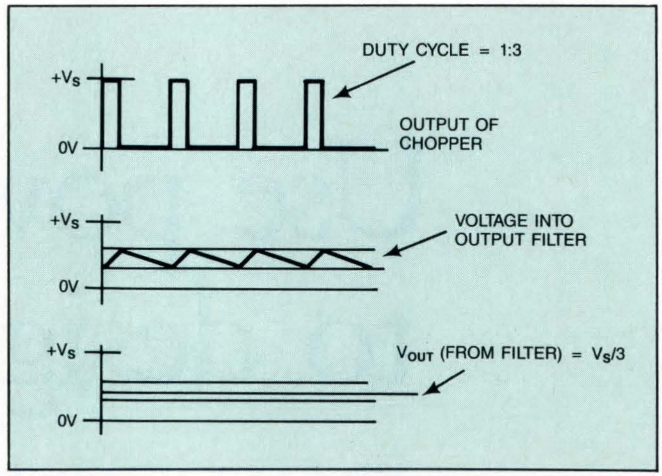

***Fig 2—By varying the duty cycle of a pulse-width modulator,** you can regulate a chopper circuit's output voltage. These waveforms are typical chopper waveforms for a 1:3 duty cycle.*

their inductance may be only a tenth of the storage inductance.

Establish the design parameters

When designing a power converter, you must first establish the converter's operating characteristics. For the power circuitry of the 29-kHz switching controller, these characteristics are:

- Output-voltage range: 0 to 110V dc.
- Output-current range: 0 to 8A (average), 10A (peak). Assume there will be a resistive load, but a no-load condition is possible. The load current requirements are proportional to the output voltage.
- Output ripple: 0.5V (peak) at maximum output voltage.
- The control method must provide an output voltage that is proportional (within a 20% linearity error) to the width of the controlling pulse in open-loop mode.
- The circuit must operate at full current at any output voltage.
- The efficiency should be 85% min.

You should also be able to connect several of the circuits in parallel, and the circuit should be capable of providing 110V rms, 60-Hz ac power output from the dc supply with few changes to the power circuitry.

These requirements, which are some of the worst possible combinations, are moderately difficult to fulfill. As a rule, you can expect any change of load current to have a significant effect on the output voltage. Moreover, because of the requirement for 110V ac out-

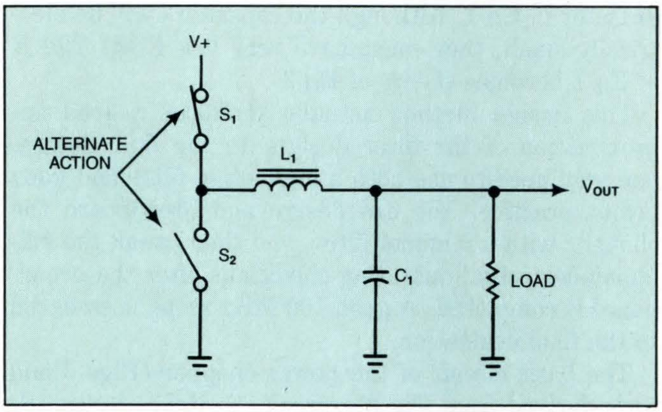

Fig 3—The output voltage of this 2-switch power-chopper circuit *can vary only between the supply limits and ground, and the circuit doesn't require snubbers.*

put power, a bipolar output is necessary, and the circuit might require a significant change to the gate-drive logic to generate the proper waveforms.

Choose the circuit configuration

Once you've decided on the design requirements, you need to choose the circuit configuration. You can choose a single-ended positive or negative converter or a 2-switch power chopper. The single-ended positive or negative converter is an excellent choice for fixed-output-voltage applications or applications in which only a small adjustment range is acceptable. Many of the 29-kHz switching controller's requirements, however, dictate that a single-ended converter is not a good choice for that application. For example, in single-ended converters, the output voltage is heavily dependent upon the load current, and it needs analog feedback to achieve stability. In other words, it can't handle wide output load variations.

In both the positive and the negative single-ended converter, the single active device charges the inductor, which then discharges into the load via a diode. The diode, which has both forward-drop and I^2R losses, must be capable of carrying the full load current. The diode must also have a fast reverse-recovery time, on the order of 50 to 100 nsec, to fully catch the inductive flyback voltage when the switch opens. Because diodes are not perfect, you must sometimes connect an RC snubber across the switch or the inductor to catch the initial edge of the flyback voltage. For the 29-kHz switching converter's design requirements, a typical snubber could dissipate as much as 15W of power—an additional reason to use a different circuit configuration than the single-ended type.

The 2-switch power chopper (**Fig 3**) is the configuration of choice. Its advantages include:

- Inherent stability—the output voltage is roughly proportional to the input pulse width.
- High efficiency—the circuit doesn't need high-speed catch diodes or snubbers.
- The circuit is forgiving of variations in the energy-storage inductor.
- Bipolar output voltages are possible.
- You can add feedback to the circuit for op-amp-like operation.

The 2-switch chopper does have some disadvantages, though: It requires a heat sink for the second transistor, an additional power device, and more-complex drive logic.

Preliminary design considerations

The preliminary design of the 2-chip power chopper includes only the essential design sequence. The design assumes that the chopper will operate directly from the ac mains, and its output is a voltage that varies in the positive direction relative to ground. You can, however, wire the same circuit for a negative output relative to ground.

Fig 4's circuits rectify the ac mains to produce a nominal 150V dc output. **Fig 4a**'s circuit operates from

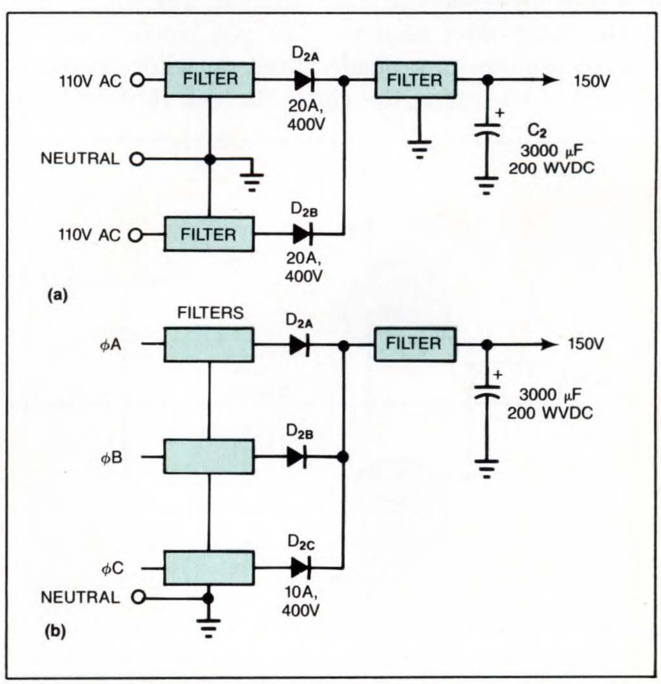

Fig 4—You can configure the power-input stage *for use with single-phase 220V ac lines* ***(a)*** *or 3-phase 208V ac lines* ***(b)***.

The 2-switch power chopper offers several advantages, including inherent stability and the elimination of high-speed catch diodes.

a 220V single-phase ac supply; **Fig 4b**'s circuit operates from a 3-phase 208V ac line. Both circuits feature full-wave rectification. The circuits' output can be either a relatively pure dc level, or simply rectified ac, depending upon the size of the filter capacitor (C_2). If rectified ac is acceptable, C_2 must be just large enough for noise-suppression purposes. At the power levels in question, capacitor current becomes a significant issue. The capacitor's reactance (at 120 Hz) and its equivalent series resistance (ESR) determine the amount of this current, which can be as much as 10A. If 20V p-p ac ripple is permissible, for example, C_2 must dissipate 50W or more.

At these power levels, it's best to make the ac input filters an inductor-based design. The circuit should not permit the switching currents to get back to the ac mains. You can choose from a number of commercially available filters, or you can do a piecemeal design. You can use a traditional LC resonance approach to this design or, alternatively, you can use these equations:

$$E = L(di/dt),\ L = E(dt/di) \quad (1)$$

$$I = C(dv/dt),\ C = I(dt/dv) \quad (2)$$

In this way, the back-reflected input ripple (permitted by C_2) drops across the filter inductor. The supply side of the filter then requires that you connect one or more capacitors to ground. These capacitors must be capable of absorbing the ripple-current variation, the *di* factor in **Eq 1**. Although the capacitors will be electrically small, they must have very low ESR. The *E* of **Eq 1** becomes the *dv* of **Eq 2**.

This design method actually produces a good approximation of the filter design. In the final design, you may need to use both a multistage filter and good layout practice. You can design and breadboard the chopper with a minimal filter, and then tweak the values under actual operating conditions after the breadboard is completed. A good 100-MHz scope is essential to the final evaluation.

The basic circuit of the power chopper (**Figs 5** and **6**) is derived from **Fig 3**'s circuit. Switches S_1 and S_2 in **Fig 3** are replaced in **Figs 5** and **6** by power FETs chosen from International Rectifier's (El Segundo, CA) Hexfet Series.

Fig 5 shows two variations of the basic circuit. **Fig 5a**'s circuit uses complementary n- and p-channel power FETs. Because of its simpler gate drive, this type of circuit would normally be preferred for this application. However, the best voltage and current ratings are found in n-channel devices. The die area of an equivalent p-channel device is normally several times that of the n-channel unit. The gate-source capacitance is also generally higher for a p-channel device. Moreover, in the higher voltage ratings, a p-channel version capable of handling high currents is often not available. For these reasons, **Fig 5b**'s circuit is a better choice.

In **Fig 5b**, inductor L_1 is the energy-storage induc-

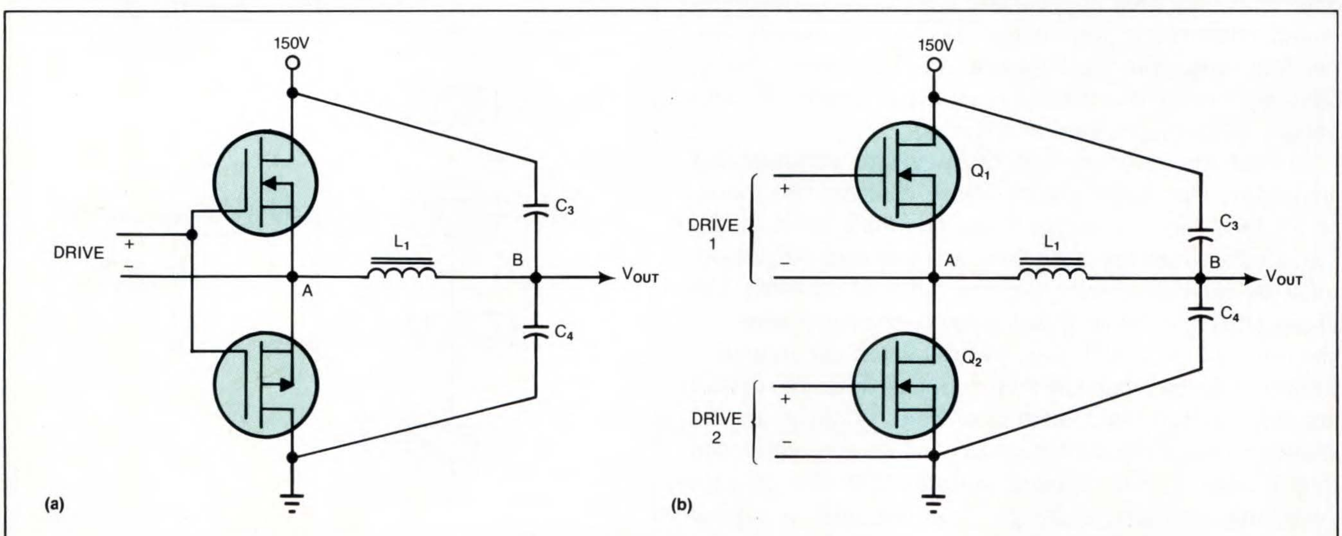

***Fig 5—The output stage of a power chopper** can be a complementary n- and p-channel circuit **(a)** or a straight n-channel circuit **(b)**. Because of simpler gate-drive considerations, the complementary circuit is normally the preferred version.*

tor. In a mechanical analogy, the inductor would be a spring, and capacitors C_3 and C_4 would act as shock absorbers. As Q_1 and Q_2 drive point A up and down, V_{OUT} at point B will stabilize at some average voltage. The actual voltage is approximately equal to the supply voltage times the duty cycle of the waveform at the gate of Q_1.

The gate-source capacitance (C_{gss} or C_{iss}) of a power FET can easily reach 3000 to 5000 pF, the result of multiple paralleled FET sites within the device. Although they don't have stored charge per se, as bipolar transistors do, the FETs' gate-source capacitance presents an equivalent problem. This large capacitance must be charged and discharged past the switching point of the composite transistor before the device can turn fully on. To achieve the requisite fast rise times in the power FETs, the driver must supply several amperes of gate current during the leading or trailing edges of the drive waveform.

The gates of Q_1 and Q_2 are driven by complementary 15V signals. The timing of these signals ensures that only one of the power FETs is on at a time. In the final circuit, the leading or trailing edges of the gate-drive signals are altered to prevent C_{gss} capacitance from causing simultaneous device conduction. Besides being complementary, the drive signals must also be floating with respect to each other. In **Fig 5b**, the drive for Q_2 is referenced to ground, and the drive for Q_1 is referenced to point A.

To provide the high current needed to charge the 3000-pF gates of the power FETs, you'll need about 12 to 15V of drive voltage. Drivers with passive (resistor) pullups are too slow to consider. The options are:

- A totem-pole, high-current bipolar pair
- Paralleled CMOS gate outputs
- A complementary power-FET pair
- A CMOS memory driver, such as National's DS0026
- A power-FET driver, such as one in Teledyne's TSC429 family.

Selecting a driver requires you to make tradeoffs in cost, speed, and current rating. Considerable information on gate drivers is available from several driver manufacturers. Siliconix (Santa Clara, CA), for example, has an excellent applications reference that reviews the subject in detail, and International Rectifier's Hexfet data book provides a thorough analysis of practical circuits.

The power-switching circuit of **Fig 6**, which is designed for a maximum current of 10A, illustrates the action in the energy-storage circuit. During the charging portion of the switching cycle, inductor L_1 is charged through the upper power FET (Q_1). The current flow through L_1 charges C_4 and, in effect, discharges C_3.

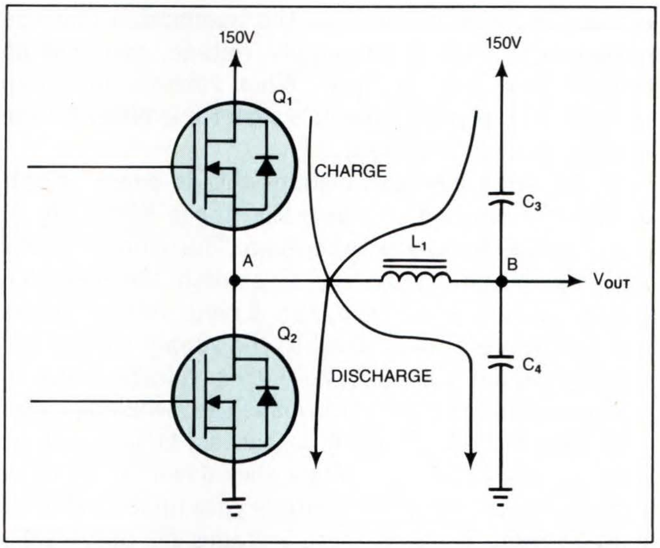

Fig 6—A single inductor and two capacitors make up the energy-storage circuit. *During the charging portion of the cycle, L_1 charges through Q_1 and C_4. During the discharge portion, Q_2 turns on and charges L_1 in the reverse direction through C_3.*

During the discharge portion of the cycle, the lower power FET (Q_2) turns on. Rather than simply discharging, L_1 actually charges in the reverse direction. The circuit doesn't permit the magnetic field to collapse of its own accord, but forces the field to reverse itself. Even so, the turn-on time of Q_2 is referred to as the "discharge cycle." The L(di/dt) equation dictates the reverse-case discharge current. Capacitor C_4 partially discharges in the process, and C_4 charges.

Because dc current flows from the power supply through L_1 to the load, the current through Q_1 is greater than the current through Q_2. The average currents through Q_1 and Q_2 are balanced only when the load is not drawing current. You should also note that there's a reverse-connected diode between the drain and source of each power FET. These diodes are intrinsic to the Hexfet design, and their reverse-recovery times are always longer than the power FET's switching speed. Although they're important for the protection of the power FET in many circuits, in the 29-kHz switching-controller circuit, these diodes never turn on.

Fig 7 shows a plot of the ideal voltage and current waveforms for the inductor as it's connected in **Fig 6's**

Some drawbacks of the 2-switch power chopper are the added expense of a second power device and the need for complex drive logic.

circuit. The plot is based on the assumption that the output is at 50% of the supply voltage, and that no current flows into the load. When current flows into the load, the plotted current waveform is offset by the amount of that dc current.

The storage inductor sustains the dc power output during the interval in which the upper FET **(Fig 6)** is not conducting power to the load. The inductor works with the output capacitors to smooth the delivered power. At any given time, the driving voltage across the inductor is always equal to the supply voltage minus the output voltage. The output voltage is essentially constant over the duration of the switching cycle.

In **Figs 6** and **7**, it's evident that, as the load voltage goes up, the charging voltage goes down for a longer period, and the discharge voltage goes up for a shorter period. **Table 1** charts these voltages for duty cycles (d) of 25, 50, and 75%, and gives you a better understanding of the change in voltage across the inductor. The design parameters specify a 150V power-supply voltage; its actual value will be closer to 165V. Assume that the load current is 10A at the 100% duty-cycle point, and that the current is scaled linearly with the duty cycle. The latter assumption is not absolutely correct, but it's close enough for the present purpose. Point A is the left side of inductor L_1, and point B is the right side.

Keeping **Fig 7** in mind, and assuming the PWM clock is 29 kHz (a full period of 34.5 μsec), you can make a preliminary calculation of inductance L_1. The available charging voltage is 75V, and the the circuit reaches its

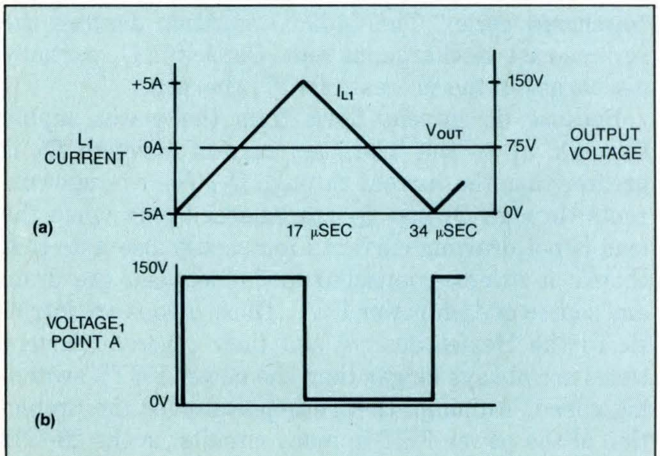

***Fig 7—These waveforms are the ideal voltage and current waveforms** for the inductor in **Fig 6**'s circuit. The waveforms assume that the output is at 50% of the supply voltage, and that no current flows in the load.*

TABLE 1—VOLTAGES AT VARIOUS DUTY-CYCLE POINTS

d	A (V)	B (V)	E_{L1} (V)	I_O (A)
10%	150	15	135	1.0
25%	150	37	113	2.5
50%	150	75	75	5.0
75%	150	113	37	7.5
90%	150	135	15	9.0

20A peak current in half the period, or 17.2 μsec. With these values, the inductance is:

$$L = E(dt/di) = 75(17.2/20) = 64.5\ \mu H.$$

Table 2 shows the values for L_1's voltage and current as a function of time. The transient current in inductor L_1 is $di = E(dt/L)$.

The original maximum-current point in the duty cycle is indeed at the 50% mark, and the total current load on L_1 (and on Q_1) is about 25A peak. These currents will probably not represent major stress to the inductor, but will exceed the 20A target drain-current peak for Q_1. The equation $di = E(dt/L)$ suggests that to reduce the peak current, you must increase the inductance. **Table 3** gives the results of reworking **Table 2** with an inductance value of 85 μH. The results show that the 85-μH value is marginally acceptable. Later, when you scale the duty cycle to set the maximum output voltage to 110V, you'll gain an additional 3 to 4A margin for the Q_1 drain current, however. (Magnetic-materials manufacturers, such as Amperex-Ferroxcube (Saugerties, NY) and Magnetics (Butler, PA), can help the non-magnetics-minded engineer to design the inductors needed for energy storage.)

The inductor in the power chopper carries an average current of 10A or less, but a peak current of 20A. The upper transistor (Q_1), which transfers current from the power supply to the load, must handle all of that current. The lower transistor (Q_2) carries only the transient current, so it may be of smaller design. For convenience, however, we've used identical FETs for both devices in the power-chopper design **(Fig 6)**.

In **Fig 6**'s circuit, it's possible that a transient could exceed the 20A limit. At start-up, under 100% duty-cycle conditions, the output voltage is zero, but point A on L_1 is effectively connected to the positive supply rail. When you use an incandescent-lamp load, the lamp's cold resistance could cause damaging currents

TABLE 2—L_1's VOLTAGE AND CURRENT AS A FUNCTION OF TIME

d	CHARGE (MAX) (μSEC)	E_{L1} (V)	TRANSIENT I_{L1} (A)	TOTAL I_{L1} (A)
10%	3.4	135.0	7.1	8.1
25%	8.5	113.5	14.7	17.2
50%	17.0	75.0	19.8	24.8
75%	25.5	37.5	14.8	22.1
90%	30.6	15.0	7.1	16.1

to flow. For this reason, the PWM controller should have a soft-start function that ramps up the duty cycle as the resistance of the load increases. If this function is not available, you must derate the FET to handle the full surge current of the start-up load. In any case, once you choose the inductance value, for a constant output voltage the current will always ramp up at the constant value set by the equation: $E = L(di/dt)$, regardless of the present pulse width. This action results from the constant voltage differential across the inductor through each phase of the charge-discharge cycle.

The power FET you select must be able to handle 10A (average) and 20A (peak) during inductive charging. The power supply for the circuit in **Fig 6** is a single-ended, 150V dc supply, but you can expect the supply to go as high as 165V during line-voltage variations. Given the rather tolerant nature of the 2-switch chopper, a 200V part will probably suffice.

The design requirements for the power chopper specified an optional 110V ac output. In this case, the output would have to swing positive *and* negative some 165V during the course of the 60-Hz input. In this configuration, the lower ground rail of the circuit would be connected to −150V dc, which indicates the need for a 400V part. (Note that a single-ended switch design is not as tolerant of supply variations. The higher-voltage part is mandatory for even a unipolar output.) The part that fills these requirements best is the IRF352 Hexfet, which has an R_{ds} of 0.4Ω at 25°C. By itself, this resistance dissipates 40W at 10A. Some important specs for the IRF352 are:

- Pulsed drain current (I_d): 20A
- Saturated on-resistance (R_{ds}): 0.4Ω
- Max drain-source voltage (V_{ds}): 400V
- Gate-source capacitance (C_{gss}): 3000 to 4000 pF
- Max junction temperature (T_J): 150°C
- Junction-to-case thermal resistance ($R_{thJ\text{-}C}$): 0.83°C/W
- Case-to-heat-sink thermal resistance, greased (R_{cs}): 0.20°C/W
- Junction-to-ambient thermal resistance ($R_{thJ\text{-}A}$): 30°C/W

The junction-to-ambient thermal resistance suggests that at these power levels, and without a heat sink, the case temperature would be 1200°C. Obviously, the upper transistor will require a heat sink to dissipate 40 to 50W continuously at full power. The lower transistor, which carries only the transient discharge current, dissipates much less power.

Configuring the gate-drive circuit

Power FETs such as the IRF352 have large gate-source capacitances that require high charging currents to overcome the FET's switching point. Moreover, it's essential that the gate-drive circuit make rapid switching transitions, especially when operating near the minimum and maximum duty cycles.

The gate drivers are TSC429 Series parts from Teledyne Semiconductor. The TSC429 can drive the gate with a peak current to 6A, charging the gate-source capacitance in tens of nanoseconds. The part behaves as a complementary pair of power-FET devices. The 429 can swing almost to the supply rail in either direction, and it provides a clean 12V waveform to the IRF352's gate. The input to the 429 is a CMOS-type load, which permits you to insert RC time delays to adjust the chopper to a no-overlap condition. **Fig 8** shows the TSC429 connected to the power FETs. Note that the driver is powered by an isolated power supply. Power for the upper transistor (Q_1) floats between ground and 150V.

In most high-voltage applications, you must isolate the FET gates from the logic signals that drive them. You must also supply complementary signals to the gate driver. That is, Q_1 must be driven On while Q_2 is driven Off, with no overlap in the drive signals.

TABLE 3—L_1's VOLTAGE AND CURRENT AS A FUNCTION OF TIME AT INDUCTANCE OF 85 μH

d	CHARGE (MAX) (μSEC)	E_{L1} (V)	TRANSIENT I_{L1} (A)	TOTAL I_{L1} (A)
10%	3.4	135.0	5.4	6.4
25%	8.5	113.5	11.1	13.6
50%	17.0	75.0	15.0	20.0
75%	25.5	37.5	11.2	18.7
90%	30.6	15.0	5.4	14.4

N-channel FETs usually have the best voltage and current ratings, so they're commonly used in high-power applications, particularly at high voltages.

Furthermore, any significant lag in the rise or fall time of these signals will seriously degrade the operation of the chopper. For a drive circuit, you could choose a transformer drive, capacitive coupling, zener-offset coupling, or an optoisolator. For the 29-kHz power-switching circuit, an optoisolator with a fast data rate (in this case, a 6N137) is ideal. The transformer drive is not a good choice because of its duty-cycle constraints; the capacitive-coupling option is a poor choice because of massive voltage swings, and the zener-offset coupling isn't a good idea because of anticipated variations in the ac power mains. Note that the 6N137 requires a 5V supply, which is derived from the gate driver's power source **(Fig 8)**.

A common buffered CMOS-level signal drives the isolator's input diodes, producing the complementary logic levels. When you tie the diodes in series, the PWM drive signal can alternately sink current from the top device or source current to the bottom device. An appropriate current-limiting resistor is tied to the closest logic-level supply rail.

Choosing the pulse-width modulator

The application also determines your choice of a pulse-width-modulator (PWM) circuit. They range in sophistication from simple unijunction transistors, to digital-logic modulators, to analog modified-cosine ramps. The 74LS592, for example, is a particularly versatile 8-bit counter that makes an excellent PWM. You invert the output from the 592's ripple-carry-output (RCO) pin and feed it back to the CCKEN pin; the timer will stop when the parallel-input pins reach an 8-bit count. **Fig 9** shows the suggested circuit.

The 74LS592 contains a separately clocked latch

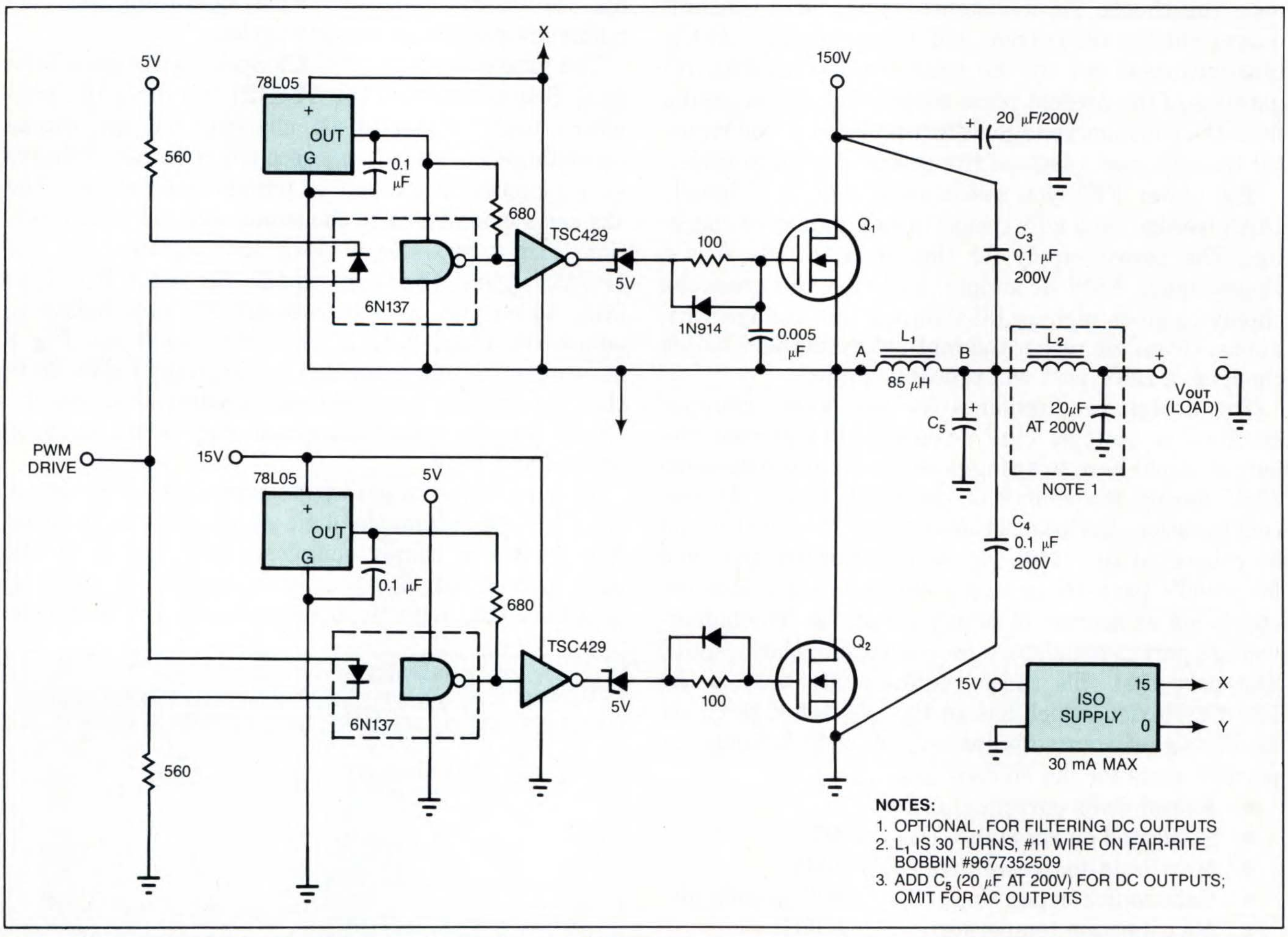

Fig 8—The completed circuit for the power chopper *includes TSC429 drivers, which provide a fast-rising waveform, rapidly charging the gates of the power FETs.*

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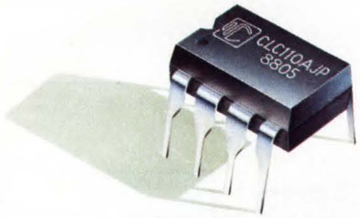

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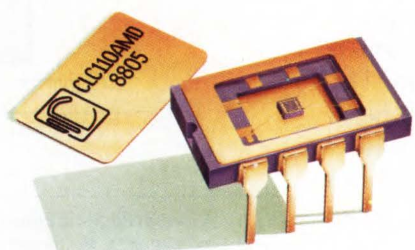

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To drive a power FET at high speeds, you need a fast-rising, high-current pulse, which can rapidly charge the FET's gate capacitance.

buffer and counter; the buffer preloads the counter. When you feed the CLOAD pin with a 29-kHz sync signal, the resulting PWM waveform has a 29-kHz period. A clock running at 256×29 kHz feeds the counter's CCK pin. The uninverted RCO output can feed an HCT-type buffer (such as a 74HCT86) to provide drive signals for the gate-drive optoisolator circuit.

Testing the power chopper

Once you've completed the circuit, you should perform all testing of the chopper with an isolated power supply and a Variac-type autotransformer. The Variac permits low-risk testing of the chopper at low amounts of dissipation. By using the Variac's ac current meter, you can readily determine whether both transistors are conducting or whether magnetic saturation is present—and you can do it all with low input voltages.

Simultaneous conduction shows up in the form of high idling current when the load is disconnected. This current stays relatively constant as you vary the ac input voltage over a wide range. It's reasonable to expect the circuit to draw as much as 50 to 100 mA from the mains during idling, but much larger values indicate a problem.

A sudden increase in idling current above the normal value for a given PWM duty cycle, either with or without the load connected, indicates that the inductor is saturated. You can perform this test safely at low ac source voltages. Sudden changes in the voltage waveform across the inductor for relatively small changes in either the PWM's pulse width or the mains' voltage are another indication that the inductor is saturated. You can easily observe these effects on an oscilloscope.

Once you've confirmed that the circuit operates as intended at low power levels, you'll need a heavy-duty (10A) supply. For safety reasons, you should use a good isolation transformer. To test the 29-kHz power-switching circuit described here, we used two surplus transformers to produce 230V (center-tapped) at the full Variac setting. Each transformer contained three 40V/8A windings, which we wired in series. The transformers sustained 10A of output current for several minutes without significant heating. After this initial procedure, we tested the chopper at the full 10A output level without the Variac or the isolation transformers.

In the absence of a dedicated high-wattage load, you can use incandescent lamps connected in parallel. Using 100W bulbs, you vary the load in approximately 1A increments. To validate the thermal design, you can use an ordinary household laundry iron—it will provide a load of about 10A. It's advisable to turn the iron on high to prevent its thermostatic contacts from arcing.

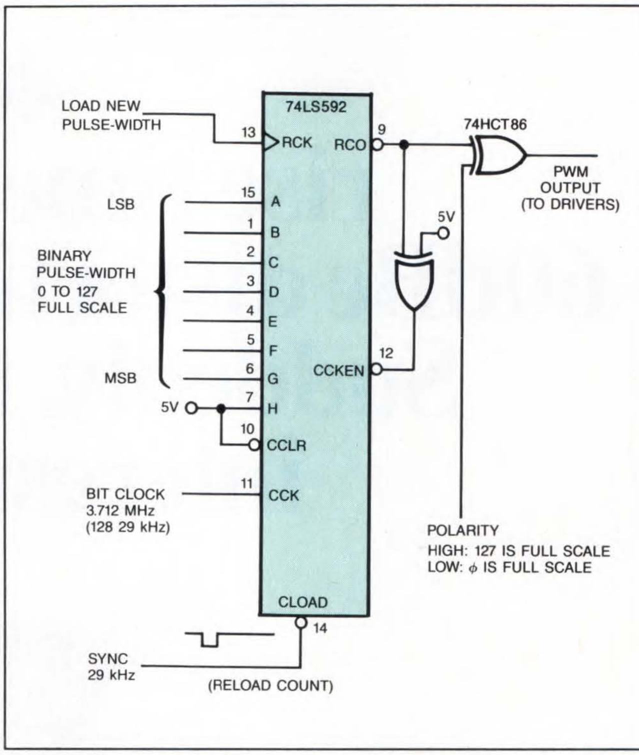
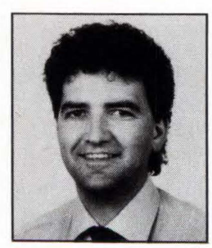


***Fig 9—A versatile 8-bit counter chip,** the 74LS592, acts as a pulse-width modulator in the power-chopper circuit.*

Author's biography



Tom Visel is a senior applications engineer at VLSI Technology Inc (Tempe, AZ), where he provides design support for the 86C010 RISC µP and its C compiler, assembler, and linker. Tom has been with the company for about a year. He was previously employed at Nikos Corp and at Sperry Flight Systems. He graduated from the Signal Corps mainframe school, and he has a BSCE from the University of Illinois. He's also a Governor's appointee to his state's Private Enterprise Review Board. Tom is active in politics, enjoys playing musical instruments and writing songs, and likes to sail.

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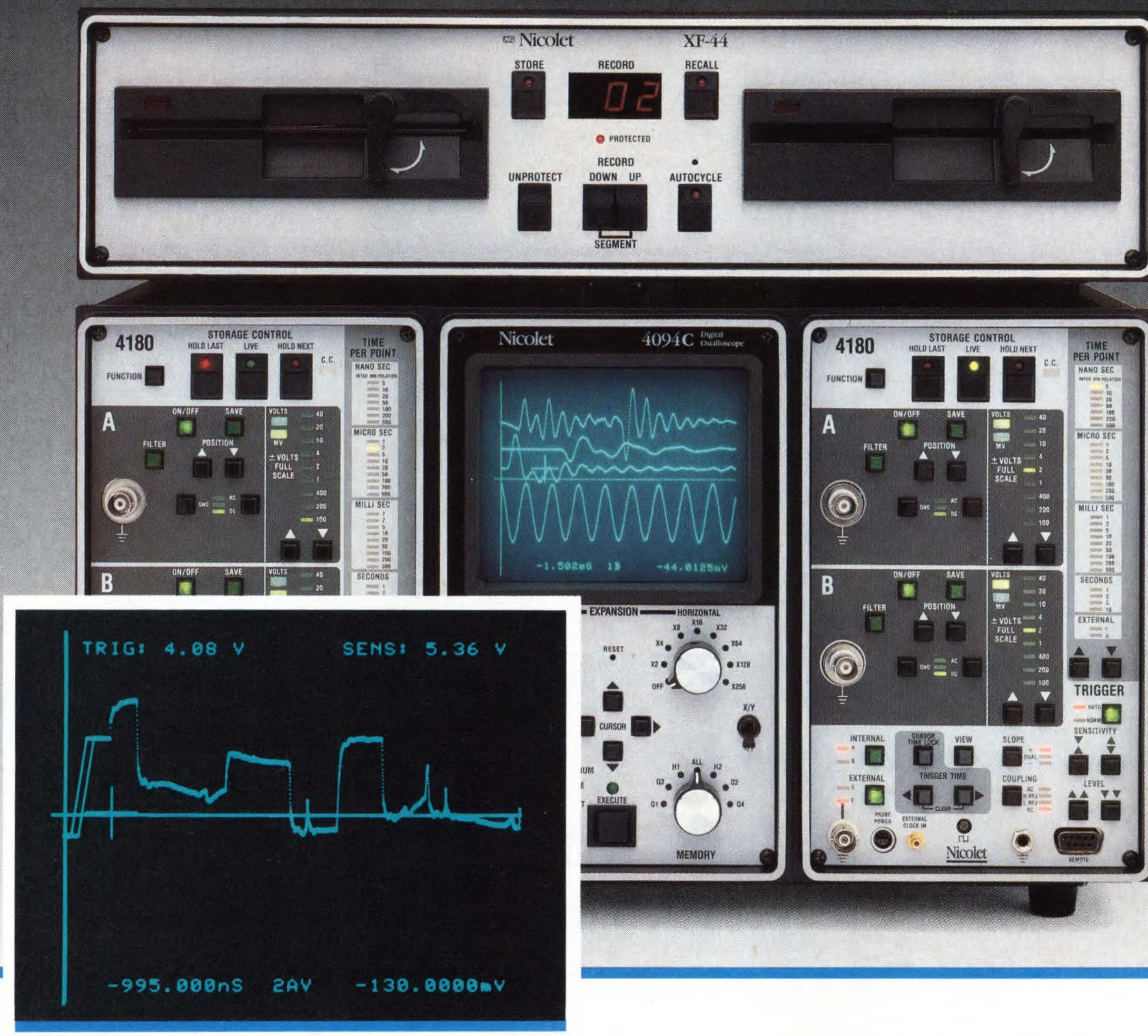

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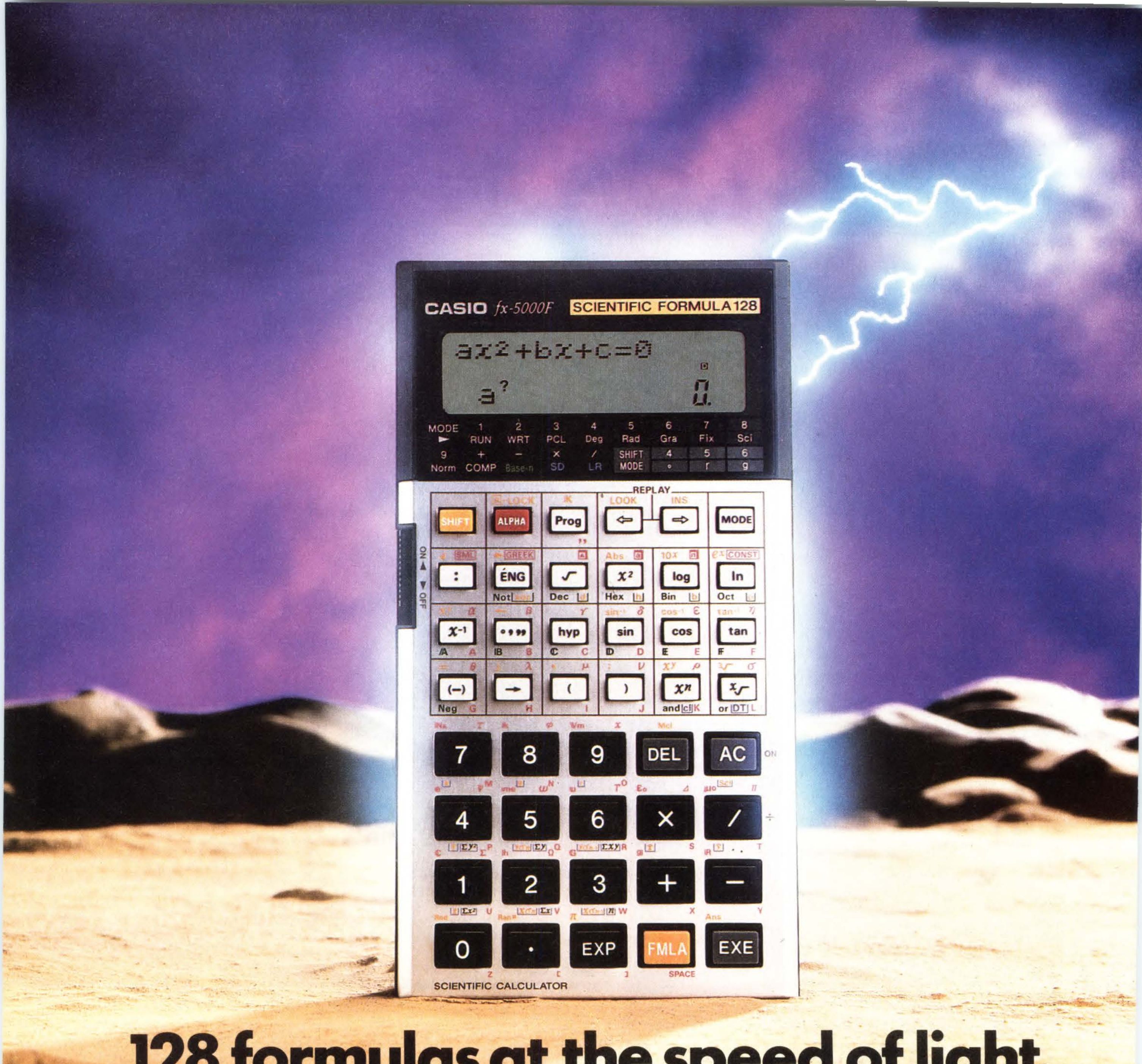

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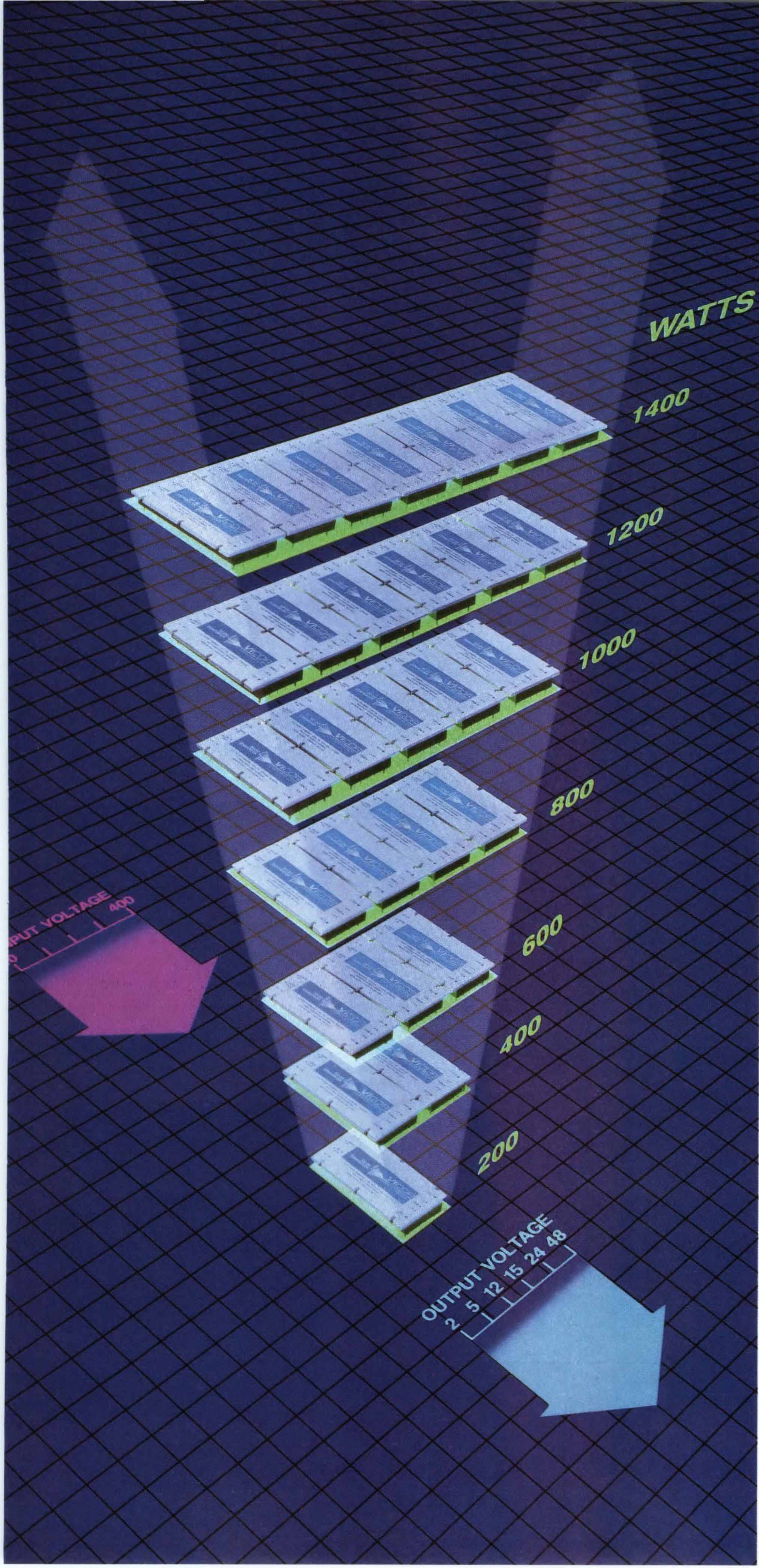

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Time-domain analysis of aliasing helps to alleviate DSO errors

By thinking in terms of the sampling rate rather than the Nyquist frequency, you'll get a better intuitive feel for how a digital storage oscilloscope may be altering your data. Undersampling results in aliasing, a long-feared problem but one that's not difficult to overcome using certain, simple techniques.

Jack Collins and David White, *Tektronix*

If you're using a spectrum analyzer, it makes sense to evaluate aliasing in the frequency domain. For a digital storage oscilloscope (DSO), however, you're usually better off to think of aliasing as the result of taking too few samples of a waveform. Aliasing can cause information not present in the original signal to appear on the display of a DSO. Bolstered with a clear perception of aliasing, you can avoid problems and take better advantage of your scope's capabilities.

Aliasing in DSOs is analogous to the problems produced by the bandwidth limitations in analog scopes. If the bandwidth of an analog scope is 50 MHz, for example, and you try to look at a 50-MHz square wave, you're likely to see a waveform on the scope's screen that is more nearly a sine wave than a square wave. The scope's bandwidth roll-off at high frequencies filters out the square wave's high-frequency components, and you're left with mostly the main 50-MHz sine-wave component. When using an oscilloscope, you learn to be aware of the instrument's bandwidth, and DSOs are no exception. In DSOs, though, you have to concern youself with bandwidth *and* aliasing.

Aliasing stems from too-slow digitizing

Aliasing can appear in any system in which signals are digitized. The classical description of aliasing deals with the frequency domain. Typically, your digitizing rate must be at least twice as high as the maximum frequency you are trying to digitize. If you digitize more slowly than this rate—the Nyquist sampling rate—you'll get aliasing. Remember, if a frequency component exists in the incoming signal, and the component's amplitude equals or exceeds half the size of the least significant bit (LSB) of your scope's A/D converter, the scope will try to digitize it. So, just because a frequency component is beyond *your* range of interest, don't assume that it won't affect the scope display.

Fig 1 illustrates the frequency-domain approach to aliasing. The signal being sampled is a 7-MHz sine wave, and the sampling frequency is 10 MHz. Because the Nyquist sampling rate for a 7-MHz signal is 14 MHz, this sampling rate does not meet the Nyquist criterion, and an alias signal results. The alias is "folded down" into a lower frequency. Specifically, the alias's

Just because a frequency component is beyond your range of interest, don't assume that it won't affect the scope display.

frequency is the difference between the original signal's frequency and the sampling rate—in this case, 3 MHz.

The mechanism that folds the original signal down into a lower frequency becomes obvious when you look at the sampling process in the time domain. **Fig 2** shows the 7-MHz sine wave being sampled at the 10-MHz sampling rate. Connecting the sampled points reveals the lower frequency alias. If you were trying to capture a 7-MHz sine wave with a DSO that had only a 10-MHz sampling rate, you would see the 3-MHz alias on the screen.

From **Fig 2,** it's clear that aliasing results from sampling too slowly—undersampling. You can imagine the sampling rate increasing until you have sampled the sine wave sufficiently to fully reconstruct the original signal. This sufficient sampling rate is two samples per period, the Nyquist rate.

Determining what constitutes a sufficient sampling rate is trivial for a sine wave, but it becomes more difficult when the signals are more complex. Consider, for example, that you might want to know how fast you must sample a square wave to avoid aliasing. If you sample a 7-MHz square wave at 14 MHz, you get a 7-MHz sine wave—along with a variety of aliases.

First, think of how fast to sample a square wave in terms of the frequency domain, where every waveform can be broken down into its component sine-wave frequencies. To represent the square wave, you need to sample at a high enough rate to capture enough of the component sine waves to "reconstitute" the square wave. Every component that is not sampled at its Nyquist rate will be aliased. In the previous example, if the 7-MHz square wave were to be sampled at 100M samples/sec, signal components above the seventh harmonic would be aliased.

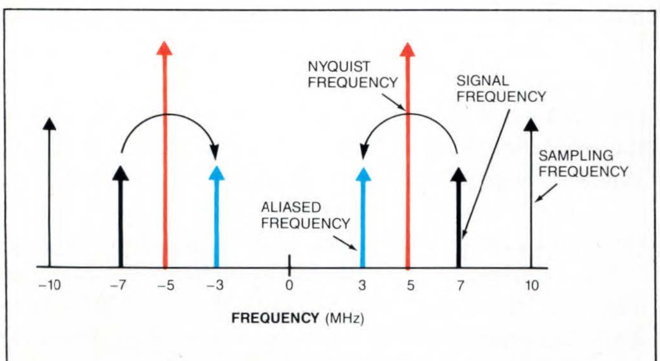

Fig 1—Traditionally, aliasing is described *in the frequency domain, where an aliased frequency folds down to a lower frequency. The alias's frequency is the difference between the original signal's frequency and the sampling rate.*

The time domain offers a simpler way to look at the problem. For the square wave, consider the timing resolution you need on the square wave's edges. If you need to know an edge's timing within ±10 psec, you must sample at least every 10 psec. Considering resolution will help you avoid situations in which the resolution is so low as to indicate the presence of aliasing.

DSOs meet aliasing in the time domain

When you apply these aliasing concepts, it's crucial to remember that you can't assume you're safe from aliasing simply because the *maximum* sample rate of the DSO you're using is high enough. You must exercise caution because the sweep speed you use determines the sampling rate you get. In most DSOs, the number of sampled data points displayed across the screen is constant—regardless of the sweep duration—and therefore only at the highest sweep speeds will a DSO apply its highest sampling rate. As you reduce the sweep speed to view a more extended segment of a waveform, the DSO samples less often. Thus, even the fastest DSO can produce aliasing on relatively low-frequency signals.

Fortunately, there are alternatives to lower sweep speeds. If your DSO has sufficient memory, you can, for example, capture a large portion of a waveform at a high sample rate and have the DSO display the entire waveform record across the screen. This use of long record lengths gives you an overview of the waveform without resorting to lower sweep speeds. You can also expand the display (zoom in) to see a greater amount of detail on a portion of a long record. Scopes with the ability to store long records at high sample rates aren't inexpensive, however.

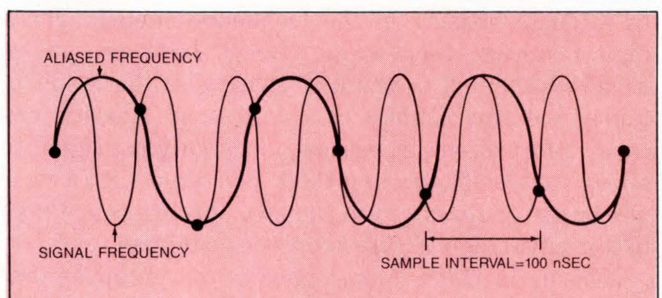

Fig 2—Viewing aliasing in the time domain *helps to reveal how aliasing affects DSOs. This time-domain representation depicts the same situation as that shown in **Fig 1**'s frequency-domain illustration.*

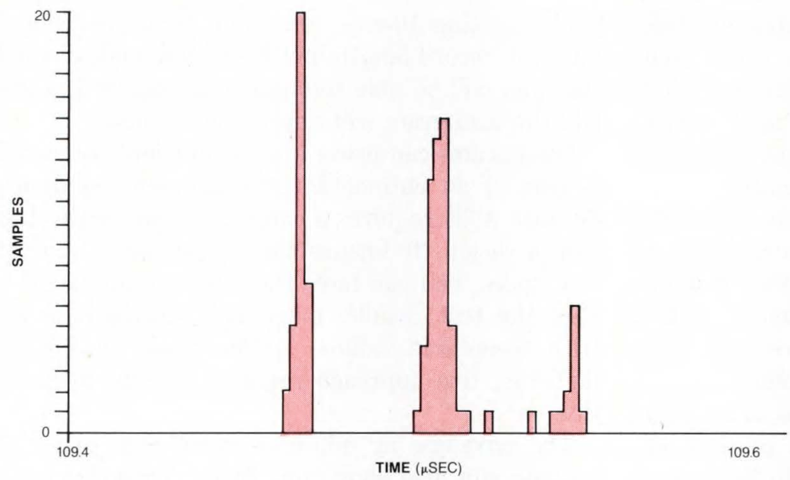

***Fig 3—A histogram screen dump shows** the variations in a measurement over many passes: The wider the histogram, the greater the measurement variation. Although noise in the circuit under test and in the DSO itself makes it impossible to obtain precisely the same measurement every time, a histogram that is wider than expected may indicate aliasing.*

Another consideration in relying on a high sampling rate to avoid aliasing is the difficulty of achieving the extremely high sampling rates necessary. To obtain a sample every 10 psec, for instance, you must sample at 100 GHz, a sampling rate that is not even available on any of today's DSOs.

A cost-effective method of achieving 10-psec resolution on a DSO does exist, however. Equivalent-time sampling is a key capability of many DSOs. It allows a DSO to collect samples over many repetitions of a waveform, until the scope obtains a true representation of even very high-frequency signals. The equivalent-time-sampling technique effectively extends the Nyquist frequency (half the sampling rate, which is the highest frequency you can acquire without aliasing) to a much higher level than is possible using real-time sampling.

Aliasing can spoil any measurement

Aliasing has varying consequences on the basic measurements you make when you use an oscilloscope. Before delving further into methods for avoiding aliasing, you'll find it useful to consider how aliasing can affect the quality of your measurements and data and how to detect an alias.

Amplitude measurements, for instance, are suspect in the presence of aliasing. If you don't happen to obtain samples on the waveform's peak, you cannot make accurate peak-to-peak measurements.

When it comes to timing measurements, aliasing ruins the measurement's validity. When thought of in terms of undersampling and low resolution, aliasing makes the location of a waveform's edge uncertain. And if you cannot be certain of where an edge really is, you cannot make accurate measurements from one edge to another. You might set your DSO to measure a time interval from the 50% point on one edge to the 50% point on another, but if there are no sampled points at the 50% point, your measurement will vary by as much as a sample interval.

Interpolation between the sampled points can reduce this error. However, be aware that this method brings its own risks. For example, undersampling the signal's rising edge causes you to rely on linear interpolation to connect the samples you do have. The edge might be linear at some points, but you can't depend upon it. And if the edge has highly nonlinear features that you do not capture, you cannot tell the correct location of the edge's 10% and 90% levels; thus you cannot even tell where to interpolate to or from. Clearly, you cannot make an accurate rise-time measurement under these circumstances.

Histograms uncover the alias

There are several basic methods to detect aliasing. One of the best—but the least used—is the histogram. The graph of **Fig 3** shows the distribution of several measurement values. Its height represents the number of occurrences of a specific measurement value, and its width represents relative precision.

Imagine, for instance, that you want your DSO to measure a propagation delay many times, log the data to a personal computer or a controller, and display a histogram of the results. If the measurement is consis-

It's crucial to remember that you can't assume you're safe from aliasing simply because the maximum sample rate of the DSO you're using is high enough.

tent, the histogram's curve should be relatively narrow. Noise can widen the curve, but a wider than expected curve hints that the measurement is producing widely varying results, and aliasing might exist. The actual width you can tolerate depends, again, on the resolution that your measurement requires.

Fig 4 illustrates the timing errors that can occur with a random digitizer when linear interpolation is used to measure an undersampled signal. **Fig 4d** shows a histogram of the pulse-width measurement with a 1-sample interval variation in the measurement. This unexpected variation indicates undersampling.

If you attempt to see 10-nsec variations in an ECL propagation-delay measurement over an interval of, say, 100 μsec, you can use a histogram to find out if you're getting 10-nsec precision. Over this long time interval, record-length limitations will make it unlikely that you will be able to obtain the required precision, and the histogram will quickly show this.

Histograms can prove especially useful when a DSO is part of an automatic-test-equipment configuration because ATE requires a careful balance of throughput and precision. To ensure that a test meets your precision specs, you can have the DSO automatically compare the test result's mean and standard deviations with acceptable values. Unlike other alias-detection methods, this approach requires no human intervention.

The envelope or min-max mode that many DSOs provide can also show you when aliasing is present. Even at low sweep speeds, these modes capture minimum and maximum amplitude values at the DSO's highest sampling rate. Thus, if a signal's peak-to-peak value in the normal mode differs significantly from the value in the envelope mode, aliasing is likely.

Another way to detect aliasing is to observe how your DSO is triggering. If you see a rolling or otherwise unstable waveform on the screen that looks as

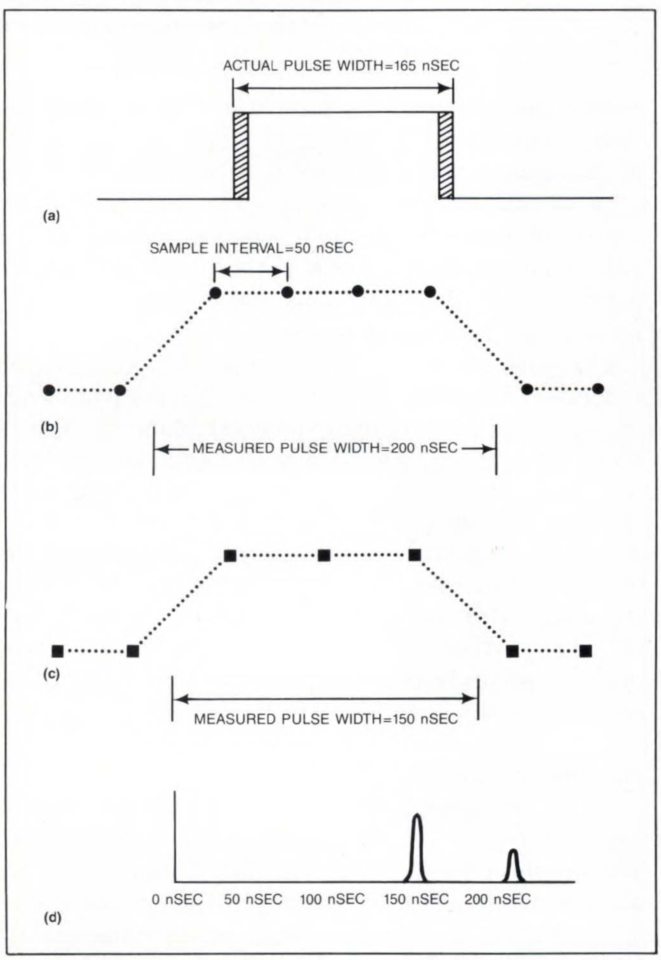

Fig 4—The effects of undersampling *on a pulse-width measurement are evident in the way the condition distorts a square pulse* ***(a)****. The two variants produced by undersampling (****b*** *and* ***c****) are shown here with linear interpolation between sampled points. A histogram of these two measurements shows the measurement variation* ***(d)****.*

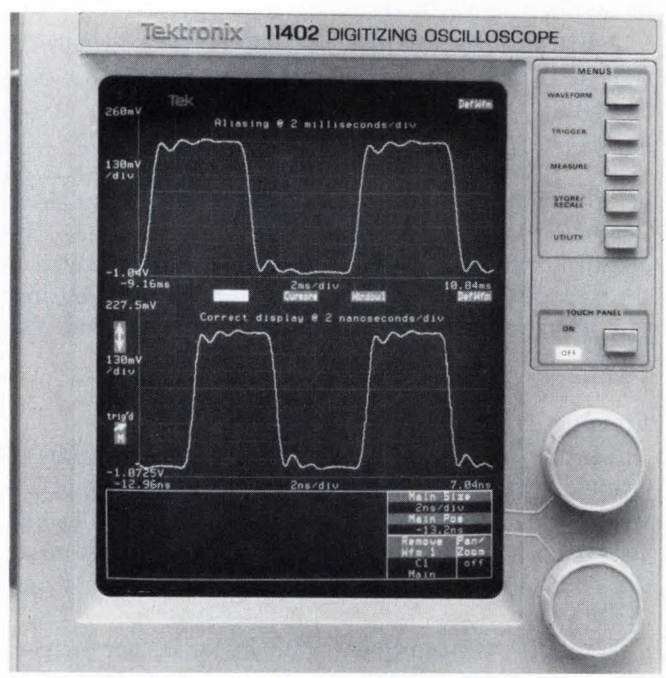

Fig 5—The most fundamental method *of spotting an alias waveform is to do a reality check. If you expect a high-frequency waveform (lower trace—sweep speed is 2 nsec/div) and see a much lower-frequency signal (upper trace—sweep speed is 2 msec/div), you'd better use some of the methods presented in the text to check for aliasing.*

though the scope is not triggered, yet the triggering indicator shows that the scope is triggered, aliasing is probably occurring. The DSO's triggering detector looks for a trigger within a specific time interval (60 nsec for Tektronix scopes). If the DSO triggers before this interval elapses, the triggering indicator is turned on. As is the case with an analog scope, if you're viewing a complex digital signal, you must make sure the trigger hold off is properly adjusted to achieve a stable display.

The last method of detecting aliasing is a basic requirement when making any measurement: Do a reality check. Ask yourself whether the waveform makes sense. Always be aware, for instance, that if you see a lower frequency than expected you might be looking at an alias that "folded down" from a higher frequency **(Fig 5)**.

Equivalent time sampling boosts the sampling rate

Once you've identified (or anticipated the occurrence of) aliasing, of course you need to know how to eliminate it. Fundamentally, you must increase the sampling rate you are using. Sampling faster might mean just using a higher sweep speed—or it might mean buying a faster DSO. Some DSOs with fairly low sampling rates are teamed up with analog scopes in the same instrument, allowing you to take advantage of the analog "infinite" sampling rate and the digital waveform-processing features (see **box,** "DSOs automate your measurements").

Another way to obtain a higher sampling rate, as mentioned earlier, is to employ equivalent-time sampling. You have a choice of two such methods: random (asynchronous) and synchronous (often referred to as sequential). Although only extremely high-speed DSOs use the synchronous method today, it is the easiest approach to understand. As **Fig 6** shows, a DSO using synchronous equivalent-time sampling takes one or more samples on one pass, and then on the next pass it takes one or more additional samples shifted slightly from those taken during the first pass. This process continues on subsequent passes until the DSO acquires the entire waveform.

Originally, the synchronous method was the only form of equivalent-time sampling, and it has the advantage of collecting samples that are relatively close to

DSOs automate your measurements

You may wonder why, in view of the aliasing problems described in the accompanying article, you should use a digital storage oscilloscope in the first place. DSOs do have many advantages over analog oscilloscopes, however, and the enormous growth in DSO usage indicates that many engineers have found such instruments useful. But if you haven't dealt with DSOs before, an overview of their advantages will prove helpful.

The greatest advantage is based on the instrument's ability to capture data and process it afterwards. A DSO's digital nature makes it possible for internal processors to manipulate the data in many ways. For this reason, you'll oftentimes find DSOs in automatic test equipment, especially in IEEE-488-based systems. Instead of requiring a human operator to compare a test waveform against a correct waveform, for example, the DSO's processor can automatically compare them within any given tolerance.

No visual judgments

The DSO can also automatically measure values such as rise time, peak-to-peak amplitude, and propagation delay. And some DSOs can calculate quantities such as power and rms voltage. In making these measurements, DSOs can actually achieve greater accuracy than is possible with an analog scope. They can achieve such accuracy because they measure the values directly after the analog-to-digital conversion process, and they don't require you to make visual judgments. Today's DSOs also employ digital timebases for greater accuracy than is generally available from analog timebases.

Finally, one of the handiest DSO features is the ability to "look back in time" before the trigger event. This ability to see the pretrigger portion of a waveform relies on the DSO's characteristic of storing digitized waveform samples in memory as it acquires them. When acquisition stops, the memory can contain as much pretrigger data as you wish, depending on how much memory the DSO has, of course.

Equivalent-time sampling allows a DSO to collect samples over many repetitions of a waveform, until it obtains a true representation of a very high-frequency signal.

each other. The voltage difference from one sample to the next is thus minimal. This condition is important for high-frequency DSOs because their A/D samplers perform best when the signal amplitude varies little between samples. In addition, because it is easier to create an incremental delay in the subpicosecond region than it is to measure that same delay, synchronous sampling has an advantage when the required sampling interval is less than a few picoseconds.

The disadvantage of synchronous equivalent-time sampling is that it does not permit the DSO to collect pretrigger data that would allow you to "look back in time" before the event you trigger on (although a delay line gives you a very limited look at pretrigger data). The pretrigger limitation results from the need to delay the sample timing on each pass from a fixed point. Thus, the DSO cannot begin to collect data until the fixed point—the trigger—is set.

Random equivalent-time sampling, in contrast, does allow a DSO to collect pretrigger data because it uses no iterative timing process. In **Fig 7**, on each waveform pass the DSO takes samples at fixed intervals that are positioned randomly (asynchronously) with respect to the trigger. The DSO precisely measures the time interval between the sample instant and the trigger event. The DSO then places the sample data in its correct memory location. Just as with the synchronous, or sequential, method, the random approach builds up a true representation of the waveform.

Regardless of the form it takes, equivalent-time sampling extends the effective sampling rate well beyond the A/D-conversion rate, to the reciprocal of the waveform-record interval (the distance between samples in the final waveform record). This result is identical to what you would get if you considered the distance between samples in real-time sampling. To determine the waveform-record interval in random equivalent-time sampling, divide the sweep's time duration by the total number of samples.

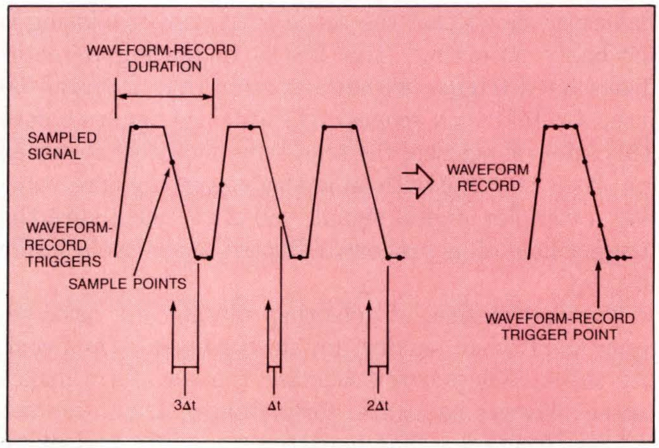

*Fig 7—**In random equivalent-time sampling,** a DSO takes samples at fixed intervals on multiple passes of a waveform, but the samples are asynchronous with respect to the trigger. Using random sampling, you can collect pretrigger data.*

It might seem that there is no limit to the resolution you could obtain using equivalent-time sampling. To increase resolution, you would simply increase the number of passes over which you collect samples. In reality, noise begins to affect the accuracy with which a DSO can assemble samples in time relative to one another. Thus, in equivalent time, a DSO's bandwidth does not depend on its sample rate; the bandwidth depends on the bandwidth of the DSO's front-end amplifier and track-and-hold sampler. Although, for example, the Tektronix 11402 DSO has a 20M-sample/sec sampling rate, by using equivalent-time sampling it provides a 10-psec minimum waveform-record interval—representing an effective sampling rate of 100 GHz. The 11402's bandwidth is 1 GHz, allowing you

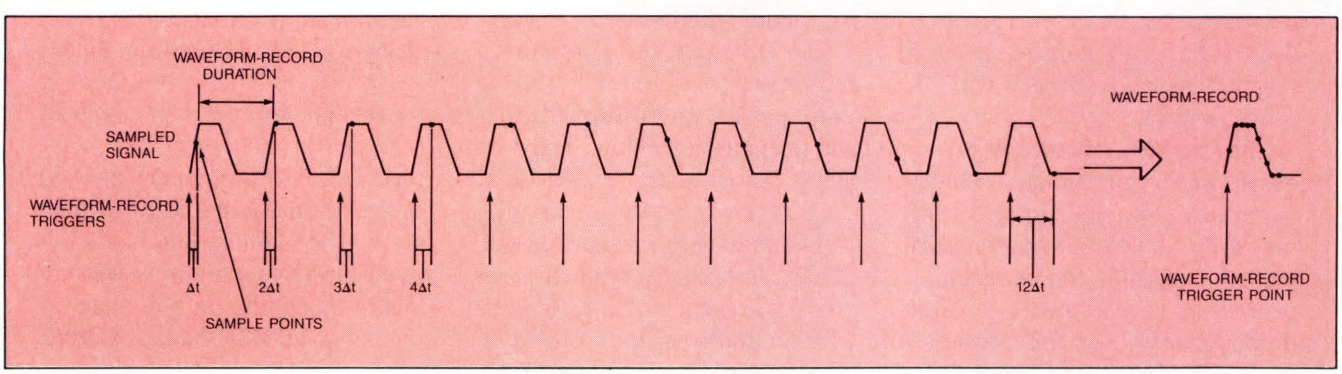

*Fig 6—**In synchronous, or sequential, equivalent-time sampling,** a DSO takes samples on multiple passes of a waveform, sampling a little further from the trigger on each pass.*

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Sampling faster might mean just using a higher sweep speed—or it might mean buying a faster DSO.

to look at very fast repetitive signals, and the 10-psec resolution gives even better resolution for timing measurements.

Autoset provides a clear view

Another way to avoid aliasing is to use your DSO's autoset capability. Most DSOs provide autoset, autosetup, or autoscale features that determine the input signal's peak-to-peak amplitude and its period or frequency. Autoset then sets the DSO's attenuators, triggers, and timebase to reproduce two or three waveform periods in a stable, unaliased display. Even if this display does not show the details you want, it gives you a good overview of the waveform and a starting point for finding the details you do want. Autoset is not infallible, unfortunately. It has a difficult time with very complex waveforms and aperiodic events, and it cannot handle transients because several waveform

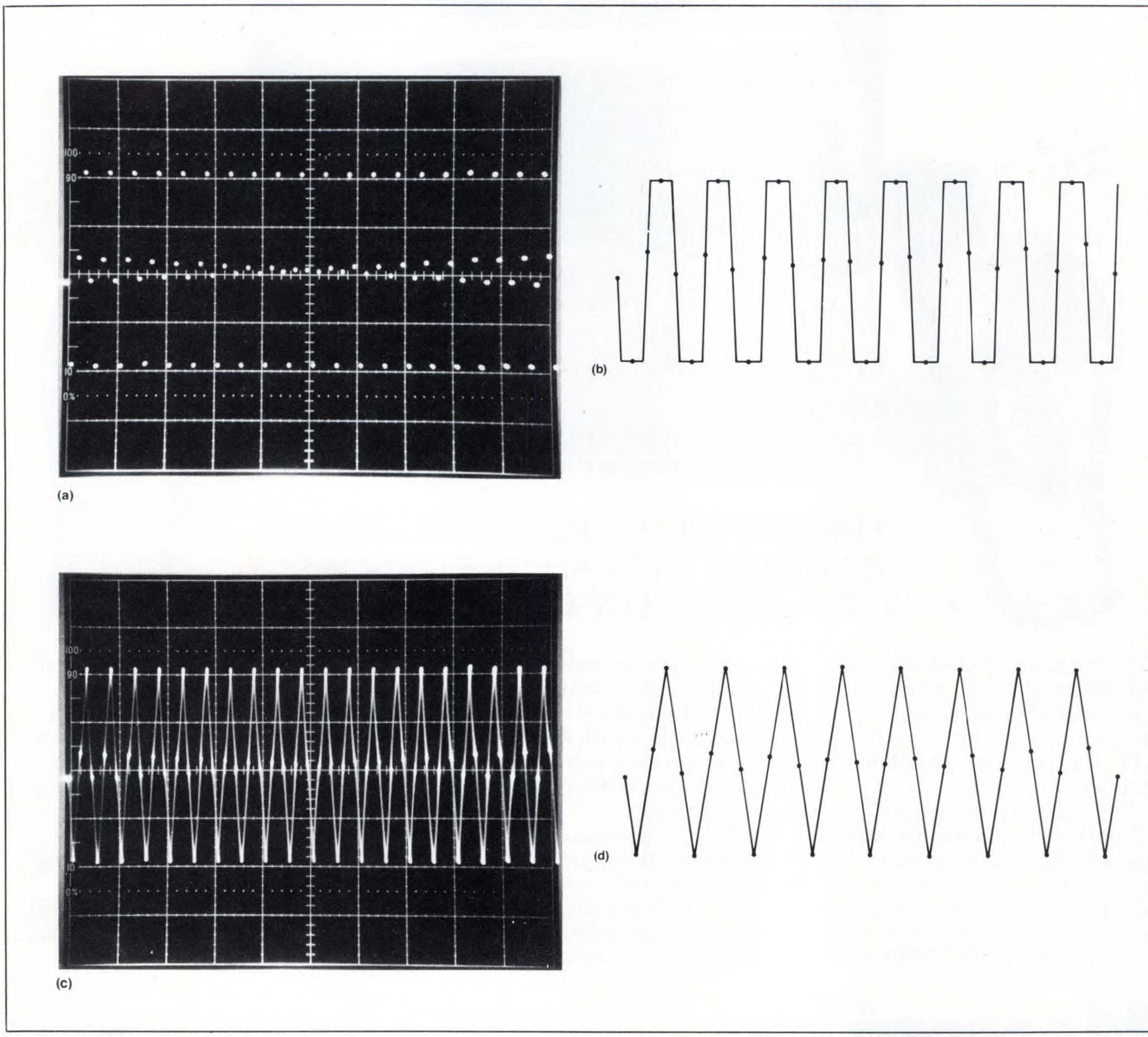


Fig 8—Visual aliasing results *from the human tendency to connect nearby dots visually—for example, when you interpret a high-frequency trapezoidal wave* ***(a)*** *as a group of horizontal (or nearly horizontal) lines* ***(b).*** *In such situations, interpolation between dots,* ***c*** *and* ***d,*** *proves especially useful.*

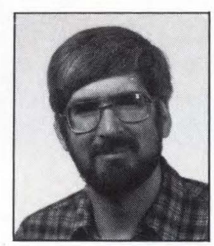
repetitions are required to find a waveform's salient features.

One final method for dealing with aliasing is to use display vectors—connections between the dots on a DSO's screen. This method helps correct an effect sometimes known as visual aliasing, in which the human eye associates dots with their nearest neighbors (**Fig 8**). Visual aliasing often occurs when you look at many periods of a fast-rise-time square wave; there will be many dots at a low level and many dots at a higher level and little way for the eye to discern the underlying high-frequency waveform.

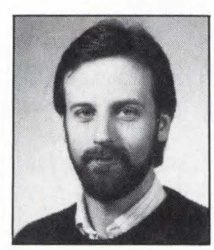
Connecting the dots with linear vectors gives your eye a chance to see the true waveform, even if the linear representation isn't completely accurate. Some DSOs also furnish sinx/x interpolation, which draws connections between points by considering waveform variations over a range of points. This approach takes into account more of the waveform's nonlinear nature. Linear interpolation, on the other hand, draws a straight-line vector from one point to the next.

Using alias-detection and -correction techniques such as these can help prevent incorrect measurements, but none of these methods is any substitute for remaining vigilant at all times. The reality check is the ultimate defense against aliasing. **EDN**

Authors' biographies



Jack Collins is a principal engineer at Tektronix's Laboratory Instruments Div in Beaverton, OR. He holds BSEE and MSEE degrees from the University of Washington and has worked for Tektronix for 14 years. Recently, he served as project leader for the digitizer section of the 11401 scope. His spare-time activities include backpacking, skiing, and windsurfing.



David White is engineering program manager at Tektronix's Laboratory Instruments Div; he has worked there for 10 years and currently manages a design team. David has attended the University of Portland, Portland State University, and Portland Community College. His favorite leisure activities are playing music, weekending on the Oregon coast, and going scuba diving.

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83C158	32	256	3	Extra modes
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CIRCLE NO 209

Circuit testability is critical for product success

Short time-to-market, increased performance in less space, and lower costs are the watchwords in today's rapidly evolving design environment. To meet these challenges, designers and those who supply them with the tools to do their jobs must ensure that their circuits can be tested quickly, efficiently, and economically.

Jon Turino, *Logical Solutions Technology Inc*

"In the past, it took a design engineer a long time to develop an untestable circuit design; now that designers have CAE, they can do it much more quickly." This saying pretty much reflects how test engineers feel about the impact of CAE on today's design environment. But the advent of CAE tools has also moved the design engineer closer to the test problem—at least in the areas of design verification, logic simulation, and fault simulation.

Many designers today still do not concern themselves with manufacturing and service-test times and costs. Smart design engineers, however, are beginning to realize that including testability in their designs saves them time and money during the actual circuit design cycle. They also realize that designs incorporating basic testability features make their lives easier and help ensure that the products they design are successful in an increasingly competitive world marketplace.

This reasoning sounds like a valid rationale for testability. But before you can design for testability, you have to know what testability is.

So what is testability?

You can define testability a number of ways, but two definitions stand out and make the most sense to engineers. First, there's the business definition of testability—a concerted corporate effort to minimize costs and maximize efficiency throughout the total business cycle, from product concept through design, manufacture, and service. Teamwork and trade-offs, in other words. Secondly, you have the qualitative definition. By this definition, testability is measured by how easy it is to write and execute a comprehensive performance-test program—one that easily detects and isolates faults on defective units. However you define it, testability attributes boil down to three basics—partitioning, control, and visibility.

To understand the importance of testability, especially in the face of increasing circuit complexity, it is important to understand the functional test process for circuits. To evaluate circuits, test engineers typically apply stimulus vectors to circuit inputs and monitor response vectors at circuit outputs to ensure that they can detect and isolate all faults that could prevent

To understand the importance of testability, you must first understand how circuits are tested.

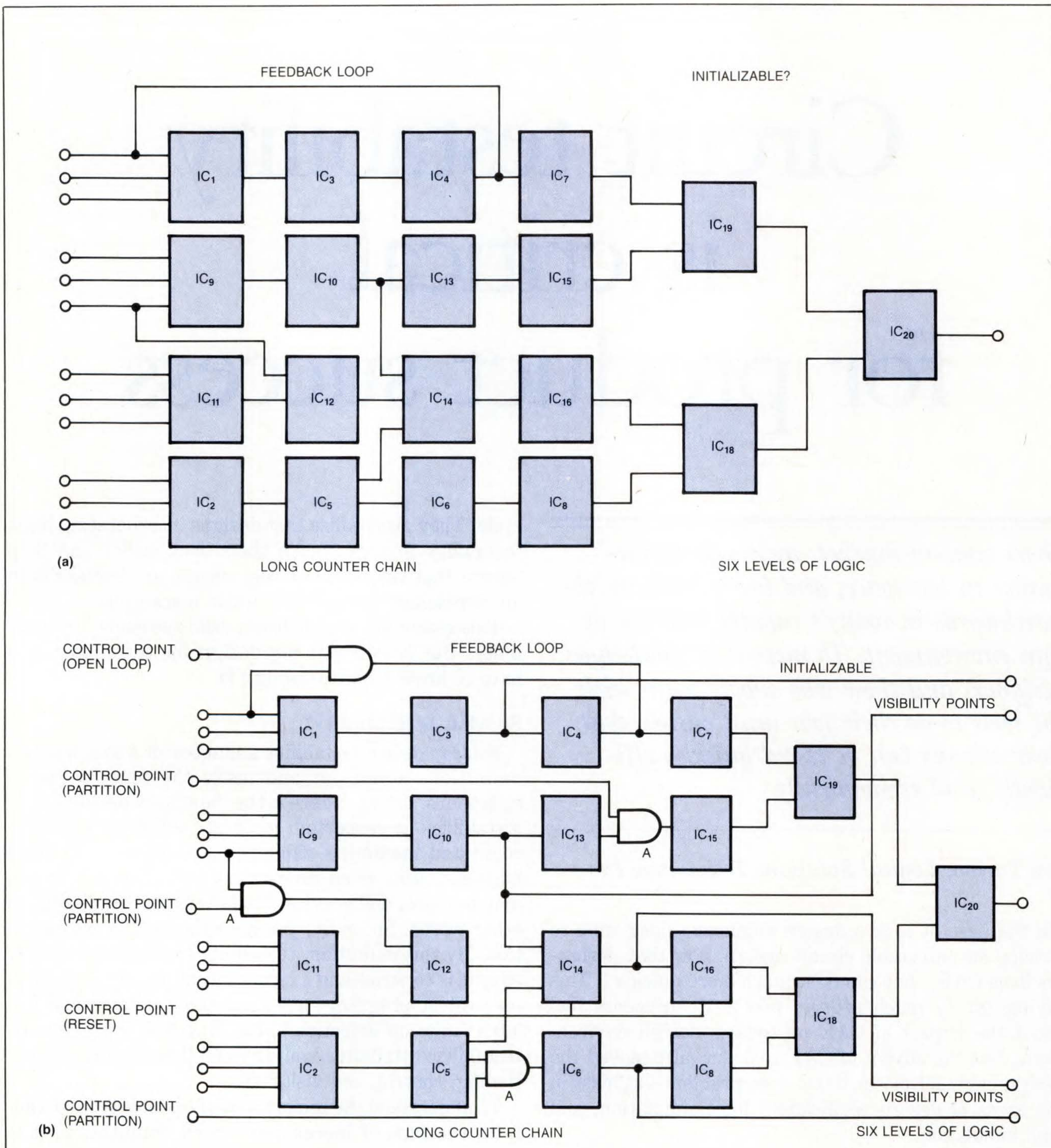

Fig 1—Complex circuit designs without testability features (a) *can be extremely hard to verify, simulate, and test or troubleshoot. Add a few gates, some extra control inputs and visibility outputs,* ***(b)*** *and you partition the circuit into smaller functional blocks. These additions make it easier to activate and propagate faults in the circuit.*

proper circuit operation. They apply these stimulus vectors to activate faults. When the resulting logic activity from potentially faulty nodes propagates to circuit output pins, or test points, test engineers can readily detect all activated faults. With simple circuits, this task is relatively trivial.

But consider the case of a possible fault at the output of IC_3 in **Fig 1a.** It may not be difficult to activate the fault, that is, develop the appropriate stimulus vectors to determine whether or not IC_3's output is latched at zero or one, because the only path to IC_3 is through IC_1. As long as IC_4 sends no signals back through the feedback loop that conflict with the stimulus signals at IC_1's inputs, there are no problems.

However, propagating IC_3's response to the stimulus patterns to the circuit output is another story altogether. There's only one way to ensure that IC_3's response to the stimulus vectors propagates to IC_{20}'s output—you must activate all other IC's in the circuit. Since a complex circuit like **Fig 1a** could well involve μPs, large ROMs and RAMs, peripheral chips, and very powerful ASICs, the design verification and testing tasks are indeed formidable. Here's where testability basics come to the rescue.

Partitioning makes things a lot easier

Partitioning, or breaking a circuit into smaller functional blocks or clusters, significantly improves circuit testability. Smaller functional blocks are easier to understand and, therefore, simplify the task of writing design verification and test vectors. Simply stated, smaller blocks are easier to simulate and easier to test and troubleshoot. To achieve the necessary control, it's important to directly access critical internal circuit nodes to an automatic-test-equipment (ATE) or built-in-test (BIT) interface. Such access makes it easier to partition and directly initialize circuits, which reduces the time, effort, and cost aspects of the design-verification and test activities. Visibility is the key ingredient here. High visibility speeds up the simulation process, increases fault coverage, and increases troubleshooting and debugging speed and accuracy.

Adding four gates, five control points, and four visibility points **(Fig 1b)** provides the desired partitioning, control, and visibility. In two cases, the extra gates are in series with the functional circuitry, and they could impact circuit performance and reliability. The remaining testability circuitry parallels the functional circuitry and thus has no impact on circuit performance and minimal impact on circuit reliability.

But these minor additions have a great impact on testability. First, the reset input will immediately initialize the circuit in **Fig 1b**—there's no need to go through any long initialization sequences to establish known logic levels at all internal nodes. Secondly, long counter chains are broken up reducing the number of logic levels needed to sequentially stimulate the circuit, as well as the number of test patterns (and, therefore, simulation events) necessary to exercise the circuit. The feedback loop has also been broken to eliminate any contention between ICs on the board and the circuits' primary input pins. Finally, several internal nodes have been brought out to test, or visibility, points to reduce the fault propagation task. The task of verifying circuit performance and detecting faults is now orders of magnitude faster, easier, and less expensive then it was for the circuit in **Fig 1a**—all achieved with minimum impact on circuit design time and costs, minimum impact on circuit performance and reliability, and minimum extra-parts cost and real-estate penalties.

A look at some testability alternatives

Once you embrace the concept of testability as a critical product-design requirement, you must then figure out how to implement it. Basically, there are four alternative implementation techniques—serial-only techniques, ad-hoc techniques, probe-ability approaches, and a structured testability-bus approach that might incorporate a combination of both the serial-only and ad-hoc techniques.

Serial-only, or scan, design techniques were originally developed for LSI/VLSI devices and serve extremely well in those applications. The serial-only technique has one main advantage—it requires the absolute minimum number of extra device package pins to implement. Fully structured scan techniques also lend themselves to automated design-synthesis and automated test-pattern generation. This compatibility significantly reduces the need for designers to learn testability techniques and how to generate design-verification and production-test stimulus vectors. Techniques such as LSSD (level sensitive scan design), Scan Path, and Scan/Set are readily available from many ASIC vendors, and you should certainly use them whenever you're designing a new chip. Each will make the chip more testable.

Boundary Scan is another serial-only technique that's gaining world-wide popularity. In addition to improving chip testability, Boundary Scan also makes testing interconnections and detecting manufacturing defects

Basically, there are four testability implementation techniques—serial-only techniques, ad-hoc techniques, probe-ability techniques, and testability-bus techniques.

on loaded pc boards more economical. The JTAG (Joint Test Action Group, whose members include major European and U.S. semiconductor users) and the TBSC (the IEEE P1149 Testability Bus Standardization Committee) have launched a concerted effort to persuade all major merchant semiconductor manufacturers to include at least the minimum JTAG port circuitry in all new standard device designs.

The groups' goal is to make all devices scannable to minimize, or eliminate, the need to use bed-of-nails fixtures for testing at the board level. Ongoing discussions between JTAG, TBSC, and the various developers of VHSIC chips have led to the creation of a powerful P1149.1 subset interface that supports Boundary Scan as well as on-chip and on-board functional testing needs.

However, a fully structured serial-only technique may not be the solution for everyone. With fully structured serial-only techniques, all devices in a given board design must be scannable and have compatible communication protocols **(Fig 2a).** In light of device availability and circuit performance requirements, it is not easy to meet these requirements—it may be several years before all devices include scan capability and can accommodate the extra I/O delays inherent in the Boundary Scan technique. In addition, implementing a powerful on-chip serial-only testability technique can increase silicon overhead by 10 to 22% and require long test sequences that might provide only ambiguous fault isolation **(Fig 2b).**

Ad-hoc testability implementation techniques also have their advantages and disadvantages. On the plus side, ad-hoc techniques accommodate many different design requirements, and they lack structure. But this lack of structure also creates problems. An ad-hoc implementation often requires many discrete I/O connections, so success depends on how well test engineers can use their technical and communications skills to convince designers that they actually require all these discrete test points.

An additional way to provide manufacturing-defects-level testability at the board level is to make sure that the probes of a bed-of-nails test fixture contact every node on the board. Having access to every node eliminates the need for functional testability in some cases but does little or nothing to provide functional, or performance, testing of increasingly high-speed boards or the systems they go into. However, as more and more designers introduce SMT into products, providing for probe-ability is likely to take more space on boards **(Fig 3)** than implementing the actual functional testability that reduces design verification/debug time and board/system-level functional, performance, and built-in testing.

The above discussion indicates that you must make a compromise. Overhead for testability (circuitry, I/O pins, and spacing) is an issue, as are circuit performance, reliability, power consumption, component availability, and design flexibility. To simplify the situation, the IEEE is developing a standard testability bus

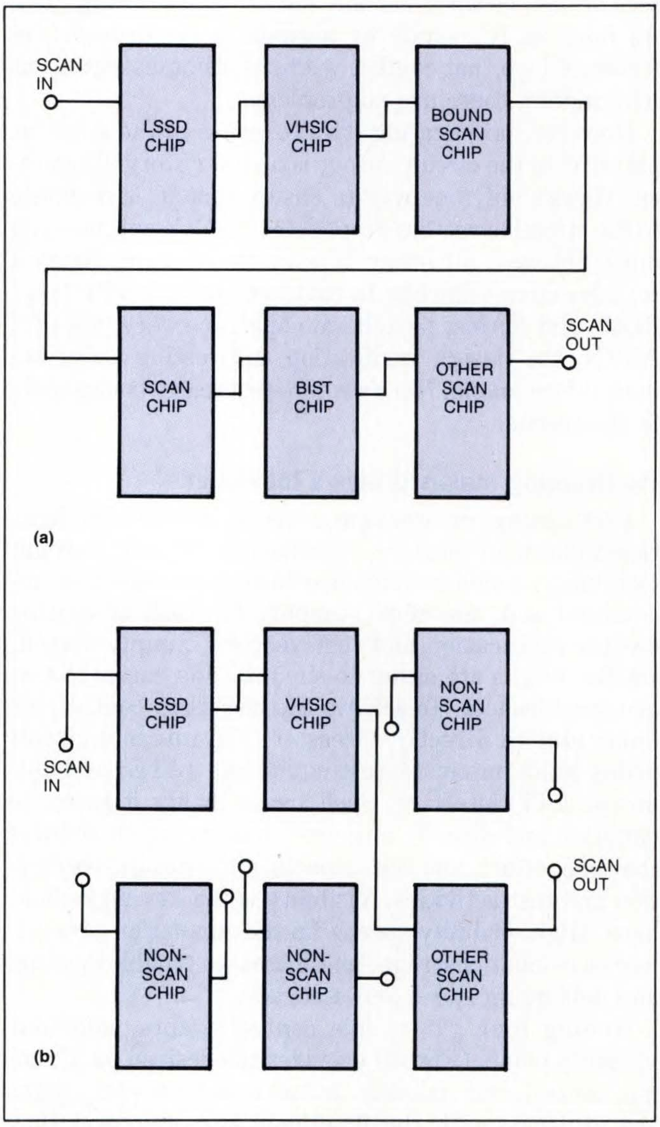

Fig 2—Serial-only testability schemes work well *at the device level because they require very few dedicated pins for the testability interface* ***(a).*** *Given the number of nonscannable chips present in today's designs* ***(b),*** *dependance on a serial-only approach can lead to incomplete fault coverage.*

TABLE 1—PROPOSED STANDARD TESTABILITY BUS LINE DEFINITIONS

P1149 TESTABILITY BUS				
P1149 SERIAL DIGITAL SUBSETS		P1149 REAL TIME DIGITAL & ANALOG SUBSETS		
P1149.1 MSDS	P1149.2 ESDS	P1149.3 RTDS	P1149.4 RTAS	LINE #
—	RESET*	RESET*	—	1
—	ENABLE*	ENABLE*	ENABLE*	2
—	SDOLOAD*	—	—	3
STDI	STDI	—	—	4
STMS	STMS	—	—	5
SCLK	SCLK	—	—	6
STDO	STDO	—	—	7
(INT*)	(INT*)	(INT*)	(INT*)	8
—	(ACK*)	(ACK*)	(ACK*)	9
—	(RCLK)	—	—	10
—	—	(INALE*)	(INALE*)	11
—	—	(OUTALE*)	(OUTALE*)	12
—	—	RTDINEN*	—	13
—	—	RTDIN	—	14
—	—	(D/ASEL*)	(D/ASEL*)	15
—	—	—	ASINEN*	16
—	—	—	ASIN	17
—	—	RTOUTEN*	RTOUTEN*	18
—	—	RTDOUT	—	19
—	—	—	ASOUT	20
—	—	TPAO-n	TPAO-n	21-2n

(Fig 4). The proposed standard testability bus (currently designated as IEEE P1149) is designed to handle almost any combination of serial, ad-hoc, and combination digital/analog testability requirements and still provide designers with as much flexibility as possible in component selection, circuit overhead, I/O line overhead, and circuit design.

The currently defined lines of the proposed standard testability bus are detailed in **Table 1.** There are four subsets to the bus. One subset (P1149.1) handles Boundary Scan and its extensions to on-chip ports for self test and built-in test. The next subset (P1149.2) takes into account such existing serially structured testability techniques as LSSD, Scan Path, Scan/Set, and incomplete scan path. The third subset (P1149.3) offers the capability for real-time digital input and output to and from unit under test (UUT) circuit nodes, on an addressable basis, from external ATE or internal or external BIT or BITE resources. This subset will handle combinations of structured and unstructured (ad-hoc) testability techniques and the various protocols that they require. The fourth (P1149.4) subset provides for real time input and output of analog signals without on-chip or on-board D/A or A/D converters.

The testability bus allows a designer to decide on an application-specific basis what the circuit overhead will be to make a design testable versus how many I/O lines of the testability bus will be required. Obviously, the more bus lines implemented, the simpler the testability circuitry required to implement them. Conversely, fewer implemented bus lines will increase the amount of

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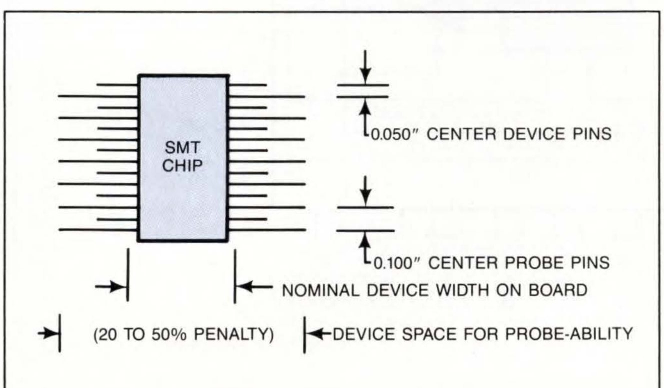

***Fig 3—You can help implement in-circuit testing** of SMT-type designs by spreading out traces and adding test points that ease access for a bed-of-nails test fixture. Unfortunately, this scheme will require lots of extra board space and provide little or no help when it comes to system-level functional testing.*

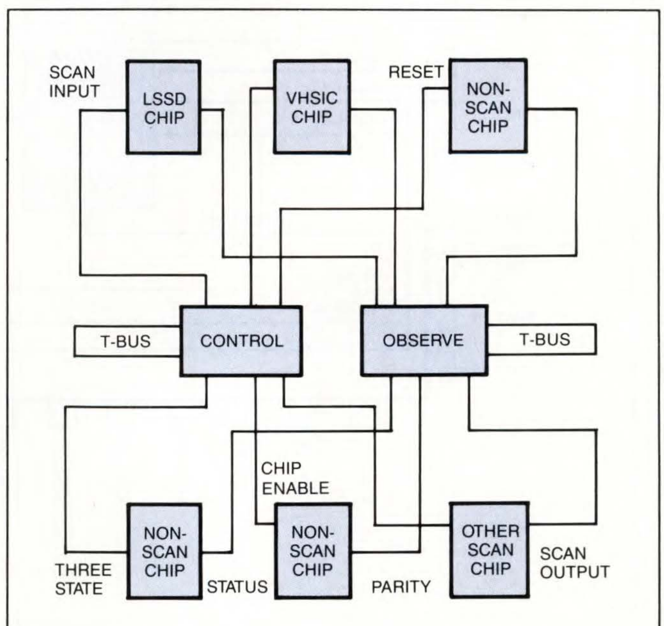

***Fig 4—To handle virtually any combination of scannable and nonscannable devices,** you can add some control and visibility circuits to implement a testability bus.*

Dual function circuits simplify matters

Testability is not always synonymous with extra parts on a board. In some cases, you can replace a standard logic component (such as a shift register, addressable latch, multiplexer, or decoder) with a testable version of the same circuit. This exchange provides a testability port without impacting the circuit's design or performance. In addition, the impact on parts cost, parts count, and board space is minimal.

Control and visibility circuits (**Figs A** and **B**) available from Logical Solutions provide just such features. If the circuit needs the shift register for board functionality, you can use the real-time addressable-control or observation ports for the testability interface. If performance specs require the latch, multiplexer, or decoder functions, you can use the serial input and output lines for testability.

So while testable functional components may have a few more pins than their typically untestable standard counterparts, they do not require dedicated board space (**Fig C**). Designers and test engineers can thus have the best of both worlds with minimal impact on circuit design parameters, circuit reliability, board space, size, weight, and power consumption—testability at almost no extra cost.

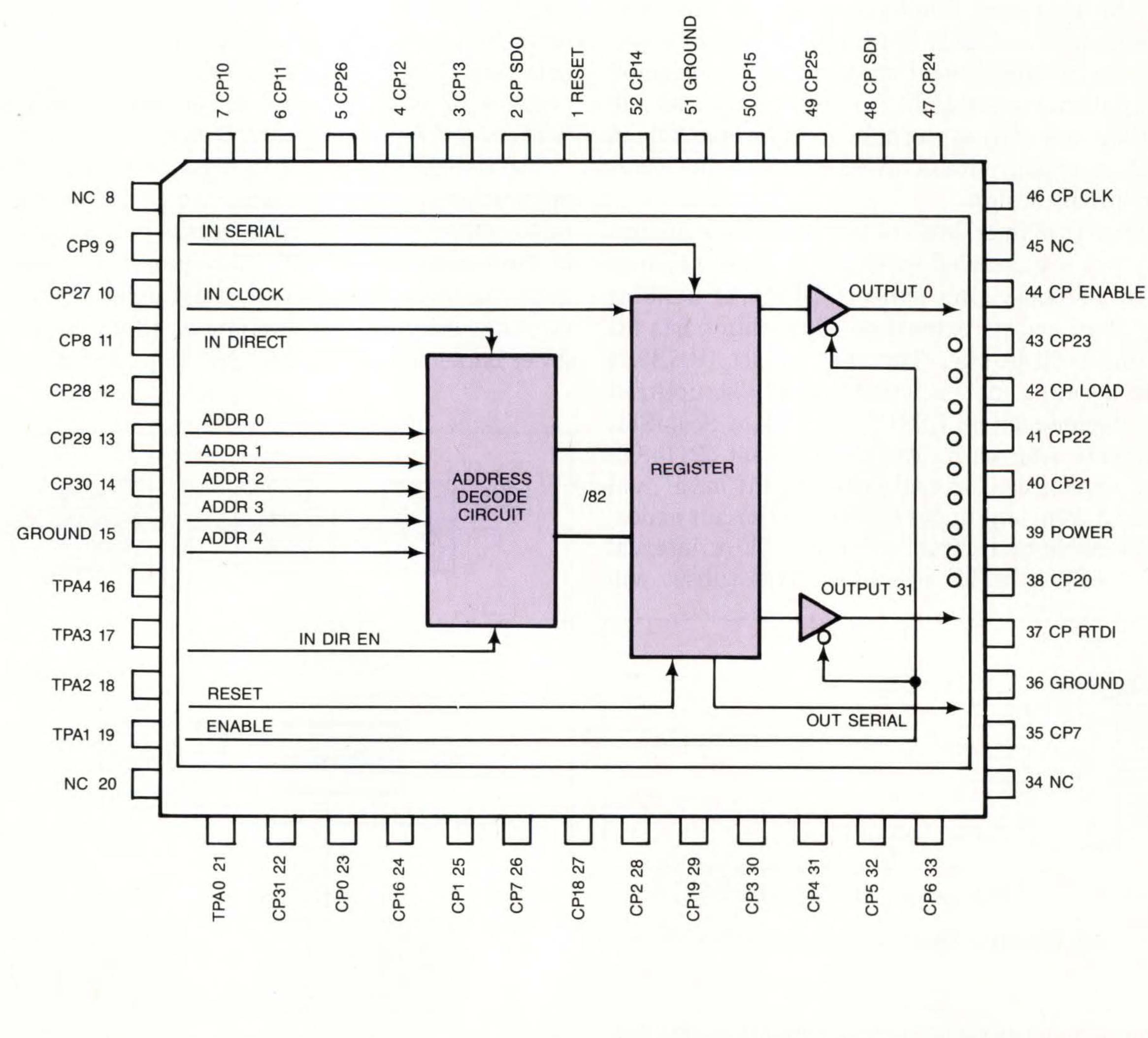

Fig A—Providing both functional performance and a testability interface, *this control circuit has both a shift register and a 1-to-32 demultiplexer that converts it to an addressable latch.*

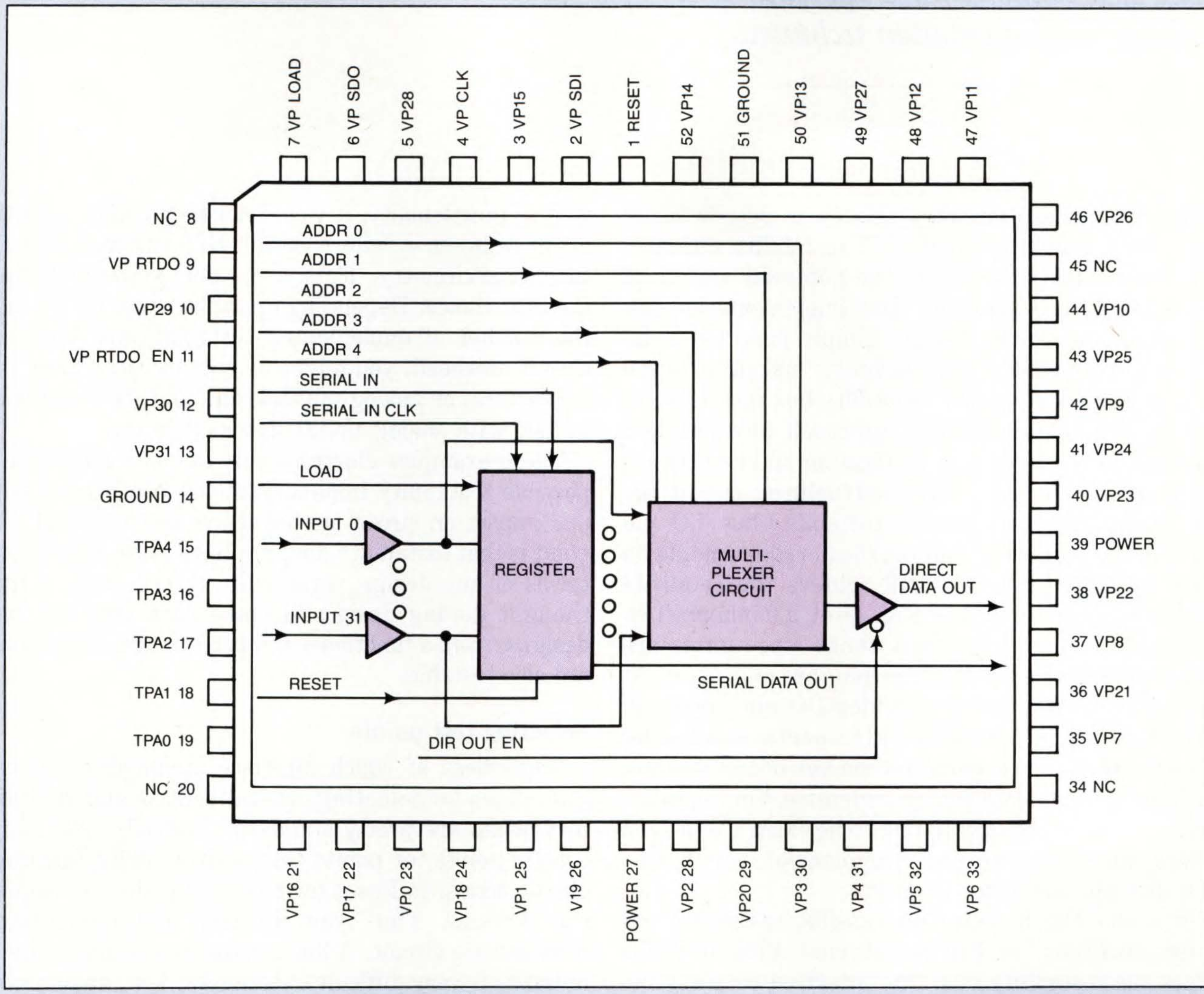

Fig B—This visibility circuit *also has two built-in functions—a shift register and a 1-of-32 multiplexer. One section provides the necessary circuit performance, and the other provides simultaneous on-line monitoring of critical circuit nodes.*

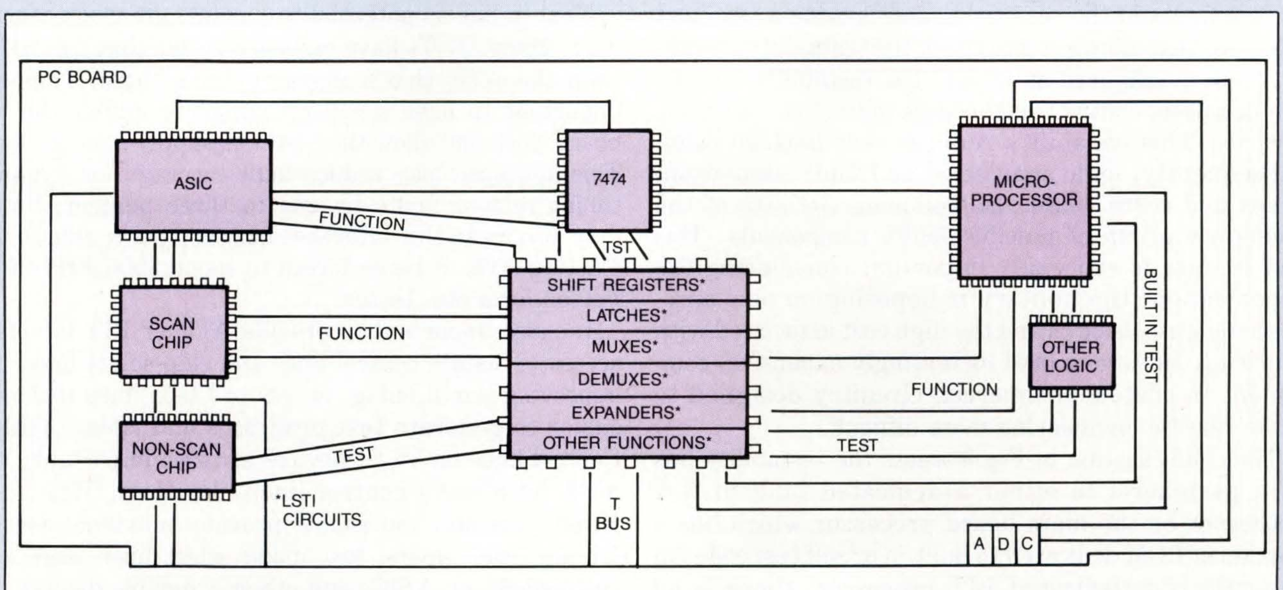

Fig C—Testability does not always take dedicated added components. *You can replace untestable single-function components with testable functional circuits to provide for good testability implementation with virtually no real-estate or parts-cost penalties.*

Flexibility holds the key to the potential success of a testability-bus approach as a testability implementation technique.

on-chip or on-board circuitry needed to decode serial signal commands into actual UUT testability actions.

Flexibility holds the key to the potential success of the testability-bus approach. Bus implementation has little impact on circuit design. Simply partition a design, add some control and visibility, and provide the test access via a standard testability-bus interface. In essence, the testability-bus approach lets you add structure (as far as design verification and testing are concerned) to an inherently unstructured circuit design. Designers can trade-off testability-bus I/O pin requirements against circuit overhead requirements on a case by case basis and still achieve the required testability parameters. At device level, a minimum-I/O-pin approach makes the best sense since gates are cheap on the device and package pins are expensive. At board and system level, a wider-I/O-pin approach makes the best sense since extra parts, conflicting device testability protocols, and the mix of testable and untestable components can be expensive. On the other hand, it is relatively easy to find some extra I/O pins on a board edge connector or to implement a dedicated testability-bus connector or socket.

Fig 5 and **Fig 6** show two possible testability-bus implementations. In **Fig 5,** external ATE or BITE utilizes the testability bus. The interface circuitry between the testability bus and the test resource can accommodate scannable and nonscannable devices, diagnose faults in the scan path, and provide a two-port interface that allows you to check the testability circuitry itself. Configured as shown, the testability circuits can partition, control, and observe individual scannable devices. This capability reduces test pattern (and, subsequently, logic simulation and fault simulation) times and costs while also reducing the size of the ambiguity group of possible faulty components. This last feature is especially important considering the specifications the military is imposing on new aerospace/defense designs and the high cost associated with replacing the wrong (and increasingly expensive) component in custom commercial circuitry designed to make reverse engineering more difficult.

The configuration in **Fig 6** treats the testability bus as a peripheral to either a dedicated built-in test processor or the main board processor which has a portion of ROM dedicated to built-in or self test code. In the case of a dedicated BIT processor, there is no impact on system performance and there are two ports into the functional circuitry—the normal port and the testability port. By using the main processor for BIT as well as functionality, it would not be possible to distinguish between a failure of the BIT circuitry and the functional circuitry. Thus, a two port system is always the best choice. Depending upon the trade-off between the number of implemented testability-bus lines and circuit overhead, you might be able to use A/D or D/A converters, or analog multiplexers and FET switches, to deal with analog circuit signals directly.

These examples illustrate only two of a multitude of possible testability implementations which have minimal impact on circuit performance and overhead. The point is that testability does not have to be expensive in terms of any design parameter. It just takes a little thought during design to make sure that the best designs, from a functional and performance standpoint, are also testable.

Selecting test points

Regardless of which interface techniques you use, guidelines for selecting critical-control and visibility test points are pretty standard. Typically, you assign control points, or points that actively drive functional circuit nodes, to Reset (or equivalent) lines of sequential devices. Thus you directly and immediately initialize the circuit. A logic circuit that's impossible to initialize is very difficult to simulate, test, and troubleshoot, so initialization signals get high priority when it comes to test points.

Next in line as potential test points are clock-control lines. Many UUTs have on-board clocks that run faster than the ATE that's characterizing them. Thus it's important to have a control signal to inhibit the on-board clock and allow the tester to supply its own clock. This approach may reduce fault coverage for dynamic timing-related faults by one to three percent, but it may also mean the difference between being able to use existing ATE or being forced to spend $500,000 to $1.5 million for a new tester.

It's also important to provide ATE or BIT interface access to 3-state control lines and chip-select lines. By improving partitioning, access to these lines makes it easier to generate test programs and isolate faults. Control lines on VLSI devices are also important. You must be able to control lines like Hold, Wait, and Ready. Finally, you should provide individual control for any scan inputs, test mode select lines, and scan chain clocks on ASICs and other scannable devices.

Important visibility points also include scan out lines of scannable devices and fan-in and fan-out points in the UUT circuitry. A fan-in point is a node where many

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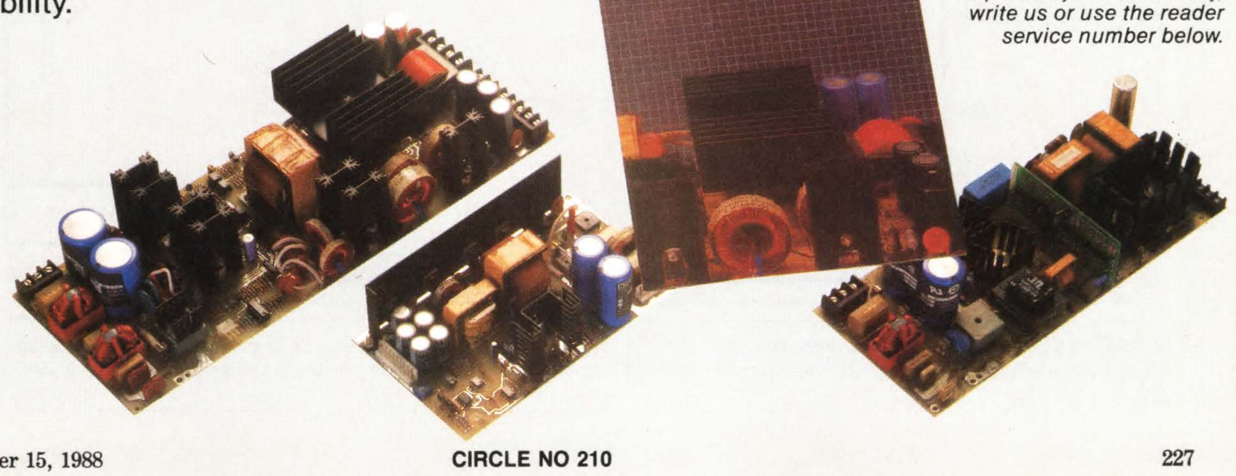

It takes just a little thought during design to make sure that the best designs, from a functional and performance standpoint, are also testable.

signals converge into a signal node; a fan-out point is a node where a particularly significant signal drives several diverging logic paths. There's one particularly good rule of thumb for selecting permanently accessible visibility points: if you're going to connect an instrument or logic analyzer to a point in the circuitry to help debug a prototype, make that point a permanent test point.

Finally, choose test points that partition the design into logic blocks using the cut-it-in-half approach. In other words, put the first test point in the logical mid-point of the circuitry to partition it into two seg-

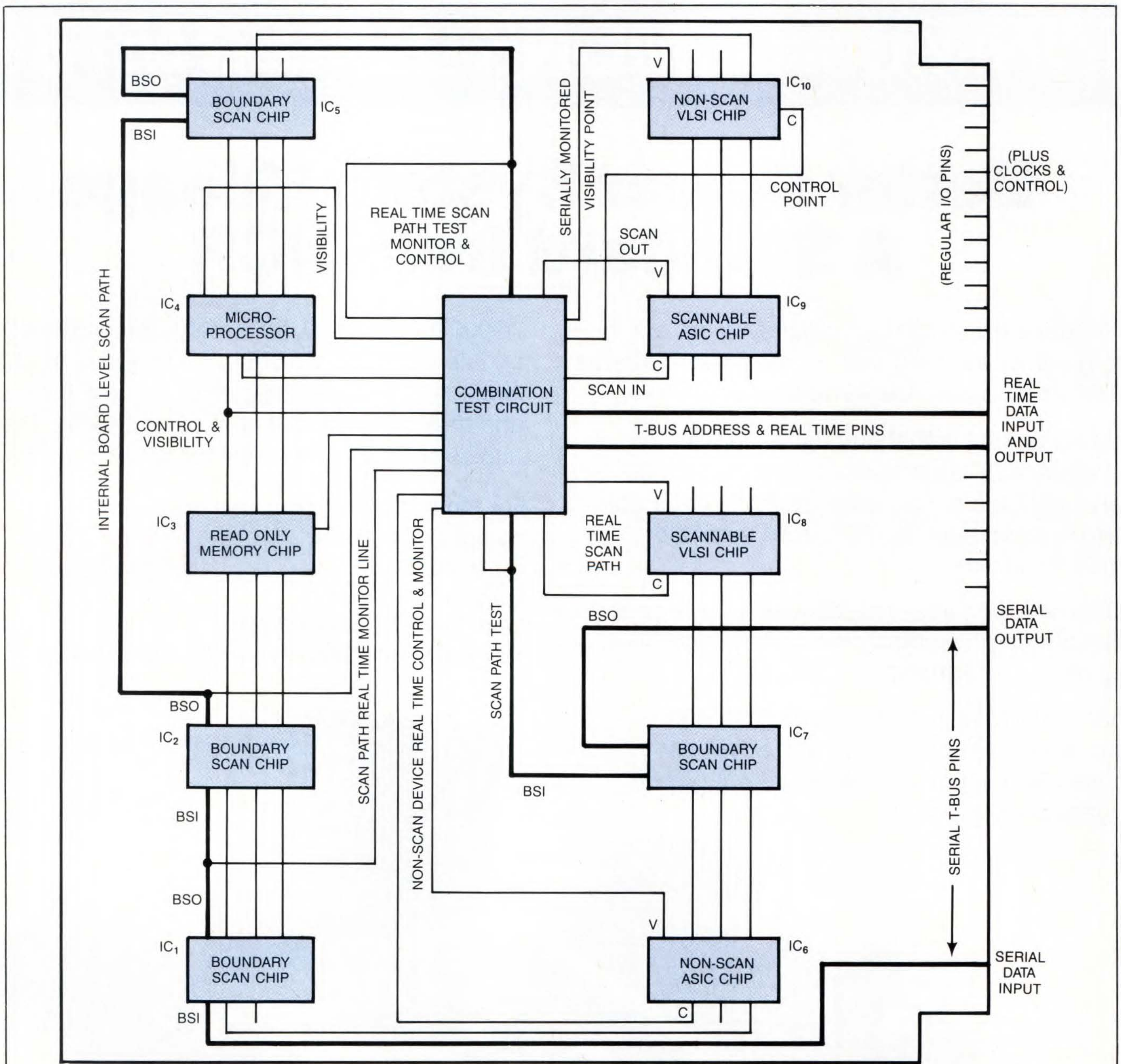

Fig 5—To make a complex circuit more testable, *you can add control and visibility circuits or replace typically untestable standard logic with equivalent-function circuits that also provide a testability-bus interface. In this particular case, the interface is designed for external ATE.*

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Testability, like anything else, is not free; but it does pay large dividends.

ments. Next, split each of the first two partitions by placing visibility points in their logical middles. Continue the cut-it-in-half process until you either use all available test points or achieve adequate fault-isolation resolution. Make sure to route critical VLSI device output lines—status lines, address and data latch lines, strobe lines, and sync output lines—to the test interface.

Testability is no longer just a designer's way of appeasing test engineers. Given the increasing complexity of today's circuit designs, testability is an absolute design attribute—it will save design engineering time and money and also reduce test and service costs. ASIC's typically feature a number of extra gates, and there are circuits available today that provide

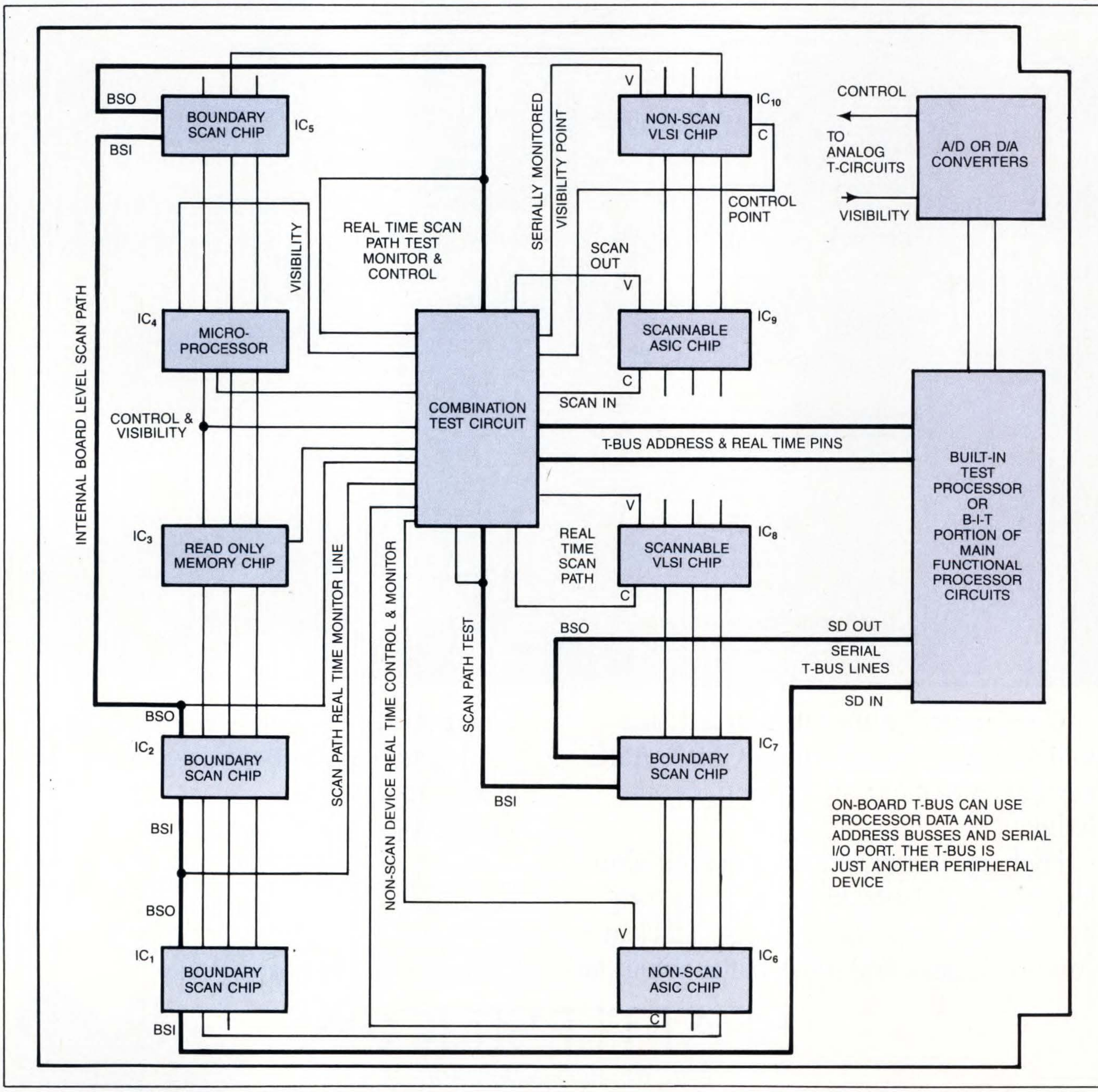

Fig 6—To provide a complete self-test capability *for both analog and digital circuitry, you could add a dedicated built-in test processor to the board. You could accomplish the same thing by using a portion of the main μP's capabilities and some dedicated on-board ROM space.*

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Partitioning, or breaking a circuit into smaller functional blocks or clusters, significantly improves circuit testability.

TABLE 2—TESTABILITY COST CONSIDERATIONS

MAJOR COST CATEGORY	WITHOUT TESTABILITY	WITH TESTABILITY
ITEM DESIGN COST (PER QTY)	$100.00	$105.00
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ATE AMORTIZED OVER 5,000 BOARDS, OTHER ITEMS OVER 200 EA.
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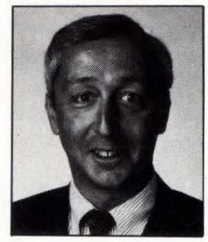
board-level testability ports. With this array of solutions available, the overhead required to implement adequate basic inherent testability need only take up one to three percent of overall board space. This loss of board space is a small price to pay when you consider that without such an investment, it may be impossible to verify a design or to economically test it in a production environment.

Like anything else, testability is not free. But it does pay large dividends **(Table 2)**. You simply must consider and implement testability features in new designs just as carefully as regular circuit performance features. It's also extremely important to remember that the testability design process and the functional circuit design process are inextricably linked and must be done in parallel. Taking an after-the-fact approach to testability almost always results in a less than optimum solution for both design and test.

Products of the 1990s will need increasingly smarter design strategies. Designing testability in early will get those products to market sooner without seriously impacting product design. Testability will make it possible to isolate unambiguous faults with far fewer test patterns and much shorter test times. Higher fault coverage figures will produce a higher quality product —a product where there is less chance that a significant number of customers will find latent faults out in the field. Built-in test features will make new designs more attractive to new customers and result in lower costs for the product's manufacturer. In short, designing for testability is a win-win strategy for design engineers, test engineers, and customers. **EDN**

Author's biography



Jon Turino is founder and president of Logical Solutions Technology, Inc (Campbell, CA). He has given seminars and consulted on testability world-wide for the past ten years. Prior to founding the company in 1978, Jon worked for Fluke, Xerox, and Tektronix. He is a founder and past president of the American Society of Test Engineers, a Fellow in the Institute for Quality Assurance, and Co-Chair of the IEEE P1149 Testability Bus Standardization Committee. Jon is a frequent speaker at major domestic and international technical conferences and the author of three books and numerous papers and articles dealing with test and testability topics.

Article Interest Quotient (Circle One)
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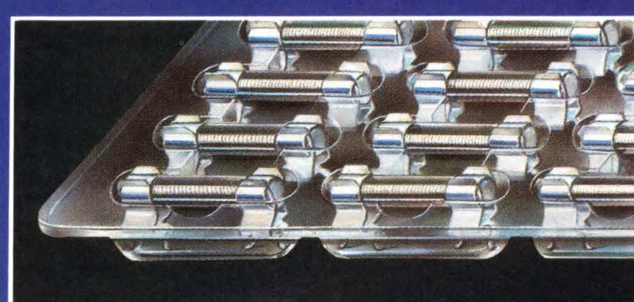

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CIRCLE NO 217

EDITED BY CHARLES H SMALL

Stimulater provides constant current

J Millar and T G Barnett
The London Hospital Medical College, London, England

Most circuits that provide an electrical stimulus for research subjects are constant-voltage designs; the circuit in **Fig 1** is a constant-current design. Stimulater circuits must be isolated for two reasons: to ensure safety and to minimize interference. Isolated stimulaters are essentially 2-terminal devices; output current can flow only between the two output terminals and can at no time flow through any other path, such as the power ground.

The circuit's bandwidth ranges from 50 Hz to 5 kHz when a ±1V sinusoidal input drives the circuit. Output loads can range from a short circuit to 100 kΩ and have as much as 0.033-μF of parallel capacitance. The transformer and associated circuitry conveniently connect to the main circuit via a cable. Note: This circuit is not approved for use on human beings.

Operational amplifiers, IC_1 and IC_2, buffer and set the gain of the circuit, respectively. You adjust trimmer R_1 so that R_2, a 10-turn pot, yields output currents ranging from 0 to 1 mA/V_{IN}. IC_3 is a power op amp. Its output drives the primary of a transformer that has a current gain of 0.1—or a voltage gain of 10. Operating from a ±15V supply, the transformer therefore has a voltage compliance of ±150V.

The circuit senses not only the current supplied to the transformer but also the current in the transformer's secondary. IC_7, a fully isolated, medical-grade amplifier, provides the isolated feedback signal (the op amp has its own built-in isolation transformer). Trimmer R_3 sets the feedback gain precisely (27 kΩ nominal). EDN

To Vote For This Design Idea, Circle No 747

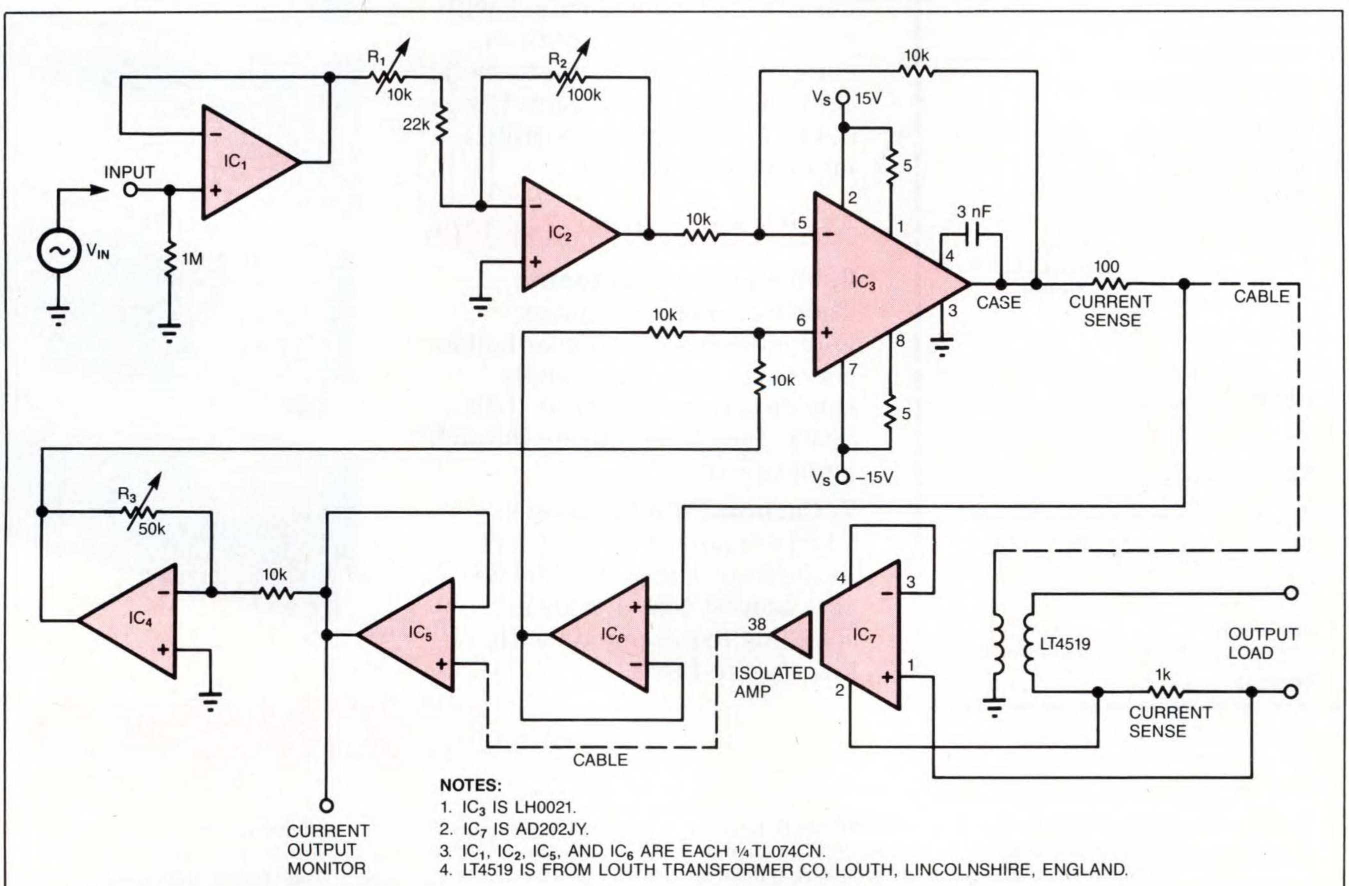

*Fig 1—**Although most isolated biomedical stimulaters** provide a constant-voltage stimulus, this circuit generates a constant-current stimulus.*

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Diagrams convert optical units

Dan G Sporea
Central Institute of Physics, Magurele, Romania

If you work with electro optics, you may find yourself puzzled by the many unfamiliar units of measurement for illuminance and luminance. The simple diagrams in **Figs 1** and **2** can help you convert such units. **Fig 1** is for illuminance units, and **Fig 2** is for luminance units. Using the diagrams is easy: Simply find the arrow going from the unit you want to convert to the unit you want to convert to. The arrow bears the appropriate conversion factor. **EDN**

To Vote For This Design Idea, Circle No 749

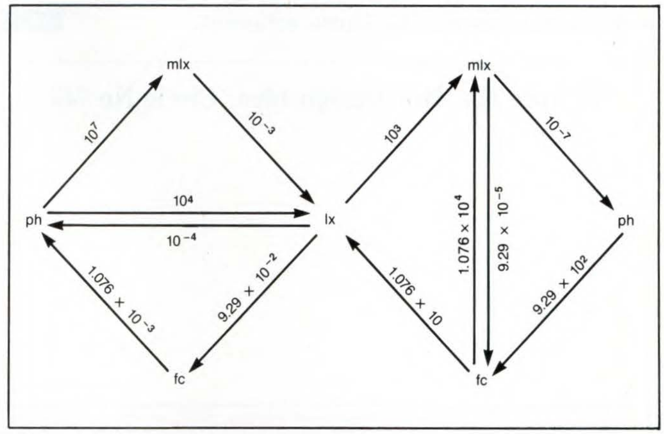


***Fig 1—This diagram supplies** conversion factors for various illuminance units.*

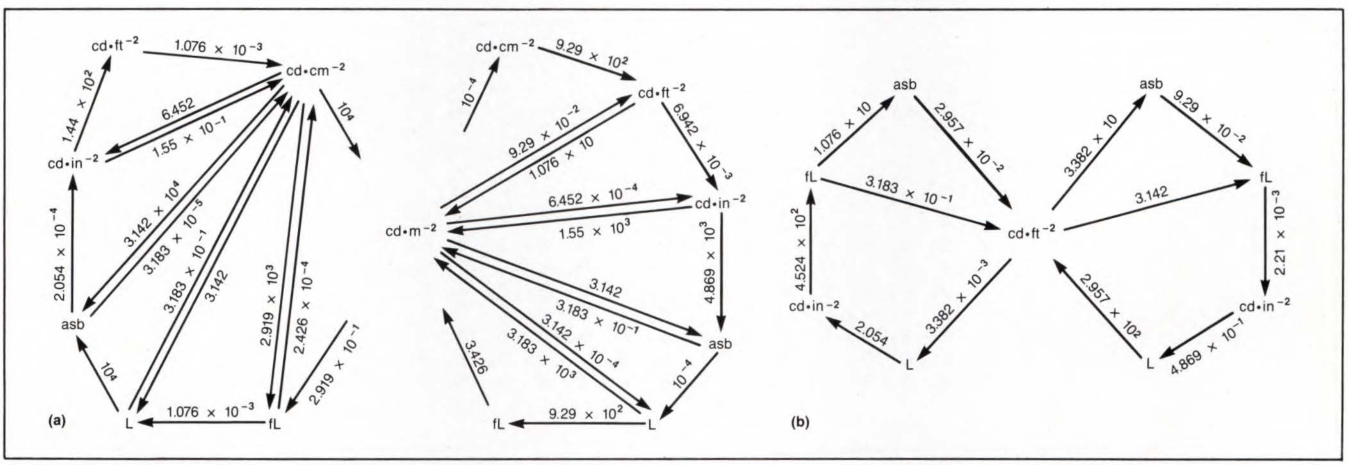


***Fig 2—You can use** this diagram to convert luminance units.*

Fast algorithm determines priority

Dhananjay Bal Sathe
Kanazia Digital Systems, Bombay, India

Starting with an 8-bit mask that represents priority levels, you can find the number of the task that corresponds to the highest, asserted priority bit in just one or two programming steps. This method is significantly faster than the one presented in "Algorithm determines high priority task" (S Murugesan, *EDN*, April 14, 1988, pg 233). But you must be willing to trade some memory space in order to gain the speed advantage.

Listing 1 shows a 256-byte table and the pseudocode you can use to access the table. The table embodies a very simple principle: Whenever you access the table using the priority-bit mask as an index, the table returns the task number corresponding to the highest-order bit set in the mask. Notice, for example, that task 6 occupies all address locations corresponding to $001xxx_2$.

Listing 2 shows a useful variation on **Listing 1**'s scheme. You can cut the table's size in half by first testing for the highest-priority task before accessing the table. **Table 1** details the program-execution and space tradeoffs for the three schemes. EDN

To Vote For This Design Idea, Circle No 748

TABLE 1—SPACE-TIME TRADEOFFS

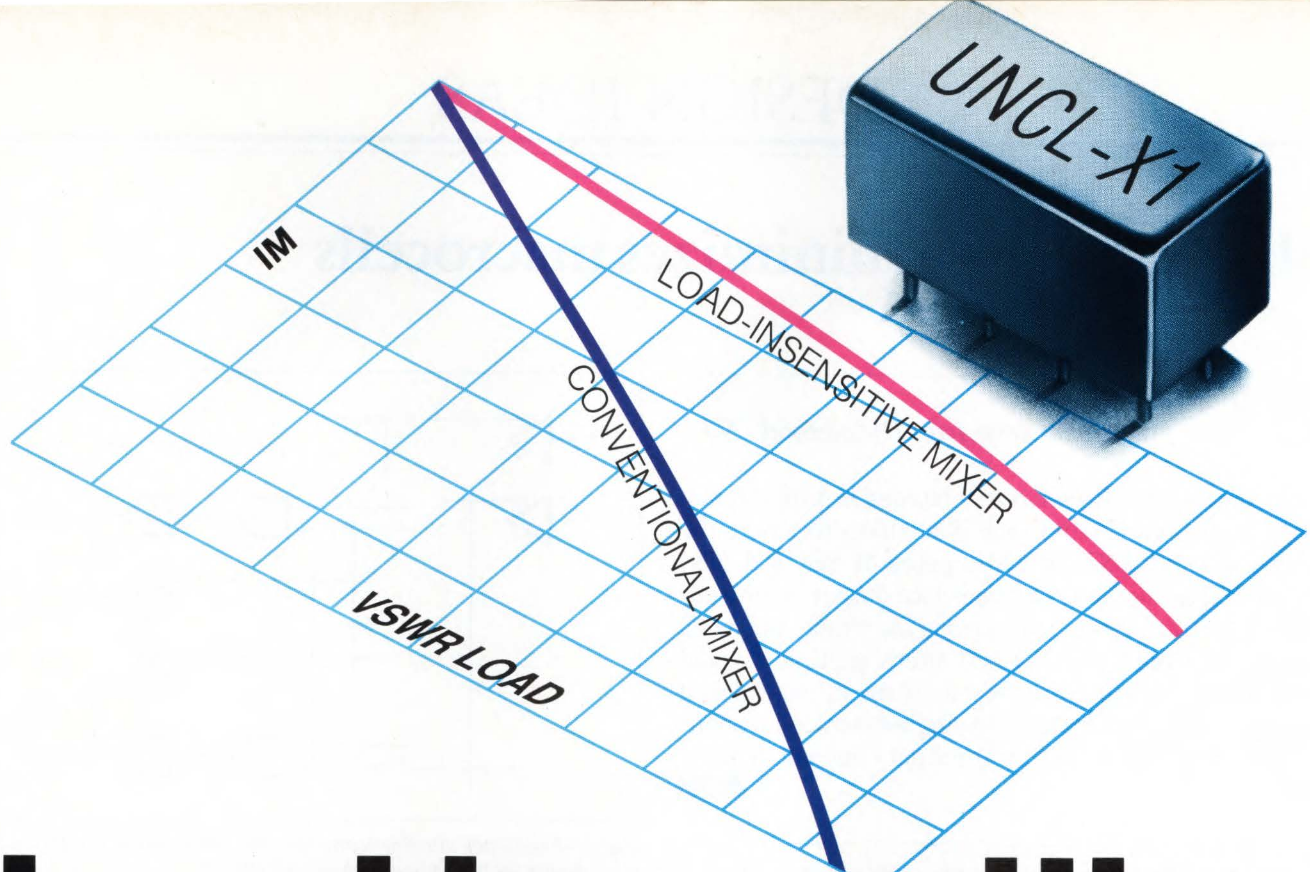
FEATURE COMPARED	ALGORITHM IN EDN DI APRIL 14, 1988	LISTING 2	LISTING 1
TOTAL DATA SPACE	0	128	256
ALGORITHM			
NUMBER OF STEPS	17	3	1
NUMBER OF STEPS EXECUTED	5	2	1
ASSEMBLY LANGUAGE PROGRAM			
NUMBER OF INSTRUCTIONS	28	9	5
NUMBER OF BYTES	70	17	8
NUMBER OF INSTRUCTIONS EXECUTED	10	7	5
SUMMARY			
SPACE (PROGRAM+DATA)	70	144	264
TIME (INSTRUCTIONS EXECUTED)	10	7	5

LISTING 1

```
+--------------------------------------------------------------+
|byte pritab[256]=                                             |
|        {                                                     |
|        0, 1, 2, 2, 3, 3, 3, 3, 4, 4, 4, 4, 4, 4, 4, 4,       |
|        5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5,       |
|        6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6,       |
|        6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,       |
|        };                                                    |
|...                                                           |
|Read priority byte P.                                         |
|Tp= pritab[P];                                                |
|...                                                           |
+--------------------------------------------------------------+
```

LISTING 2

```
+--------------------------------------------------------------+
|byte pritab[128]=                                             |
|        {                                                     |
|        0, 1, 2, 2, 3, 3, 3, 3, 4, 4, 4, 4, 4, 4, 4, 4,       |
|        5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5,       |
|        6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6,       |
|        6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7,       |
|        };                                                    |
|...                                                           |
|Read priority byte P.                                         |
|if P < 128                                                    |
|then                                                          |
|        Tp= pritab[P];                                        |
|else                                                          |
|        Tp= 8;                                                |
|...                                                           |
+--------------------------------------------------------------+
```



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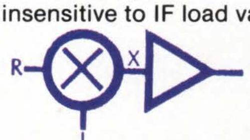

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IF	10–500		10–500	
CONVERSION GAIN, db, Typ.				
Mid-band (10–250 MHz)	1.0		2.5	
Total range (1–500 MHz)	0.5		2.0	
ISOLATION, db, Typ.	L–R	L–I	L–R	L–I
Low-band (1–10 MHz)	60	50	60	50
Mid-band (10–250 MHz)	30	30	35	25
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CIRCLE NO 220

C 121 REV. ORIG.

SR latch design minimizes macrocells

Peter Haas
Electronics For Machinery Inc, Ridgewood, NJ

When designing SR (set-reset) latches in programmable-logic devices (PLDs), you don't have to mimic the cross-coupled NAND or NOR gates of SSI and MSI designs. That method consumes two output macrocells **(Fig 1).** In some cases, you can use the single-macrocell schemes in **Figs 2** and **3. Fig 3** offers multiple set and reset inputs, which are handy features in multiplexed systems. The catch is that the single-macrocell designs can give you either a Q or $\overline{Q}$ output, but not both at once. EDN

To Vote For This Design Idea, Circle No 746

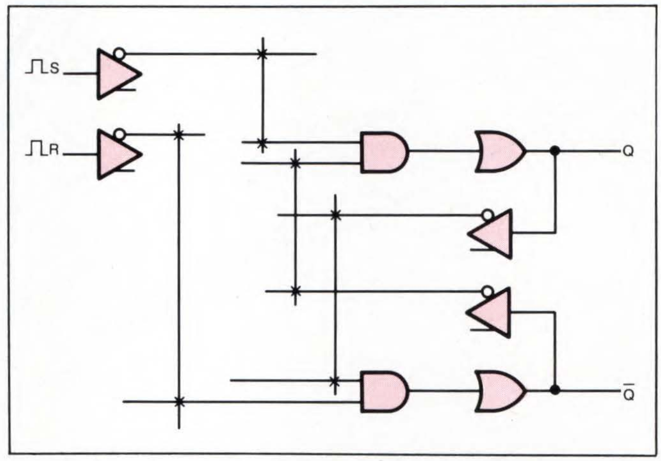

*Fig 1—**Following standard practice for SR latches** results in a PLD design that consumes two macrocells.*

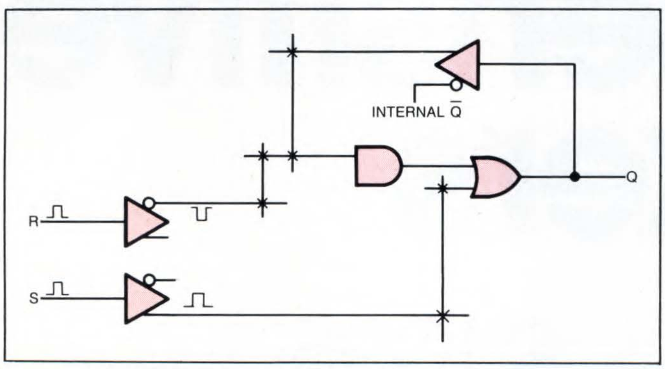

*Fig 2—**If you need only** a Q or $\overline{Q}$ output, you can design a SR latch that consumes only one macrocell.*

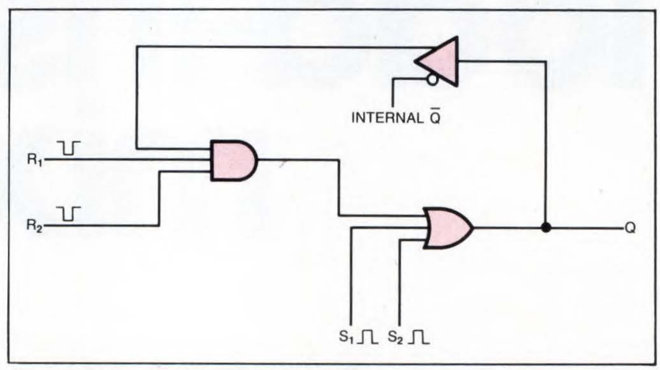

*Fig 3—**This single-macrocell** SR latch provides multiple set and reset inputs.*

Algorithm finds bit's value in decimal

S Murugesan
NASA Ames Research Center, Moffett Field, CA

You don't always have to first convert a decimal number to a binary one in order to find the value of a specified bit. Instead, you can use an algorithm to perform the calculation quickly and directly. The algorithm states that the *m*th binary bit (b_m) of the binary number that corresponds to a given decimal number D is 1 if the integer part of of the quotient of $D/2^m$ is odd; otherwise the binary bit is 0. That is:

$$b_m = \text{remainder of } (D/2^m)/2 = MOD_2(D/2^m),$$

where b_0 corresponds to the least significant bit (LSB). For example, b_3 of 31285_{10} is zero because the quotient of $31285/2^3$ is 3910 and MOD_2 of 3910 is zero. This algorithm suits applications where you must extract the value of a few bits from a large decimal number. EDN

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CIRCLE NO 221

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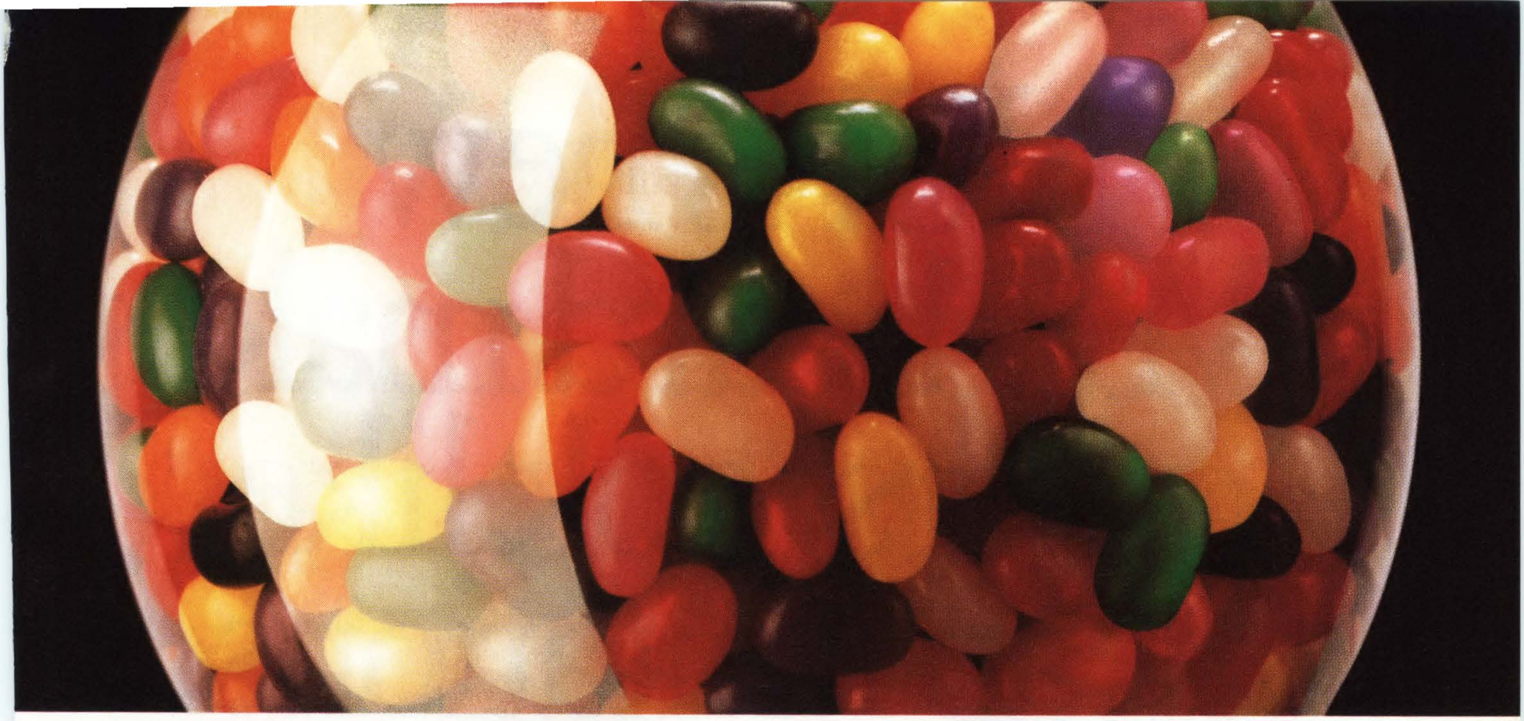

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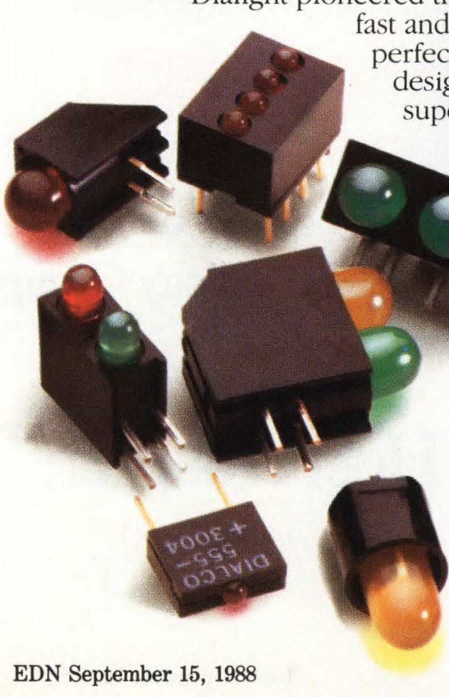
All meticulously engineered with the understanding that the failure of a "jelly bean product" can cost thousands in end-user downtime, and who-knows-what in customer loyalty.

The same understanding might bring you to call 201-223-9400, or write Dialight Company, 1913 Atlantic Ave., Manasquan, NJ 08736, and ask for our catalog or a product sample. At the very least, it's brought you to the real end of our ad.



DIALIGHT COMPANY A Division of North American Philips

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Engineering is the only commodity we sell.

CIRCLE NO 222

NCR's new VME(TM) board makes others look like cheap imitations.

Until now, VME(TM) host adapters have done fairly good impressions of high performance VME boards. But they pale in comparison to NCR's new VME-to-SCSI host adapter.

First of all, NCR's board boasts the NCR 53C90 SCSI protocol chip – the highest performance SCSI chip available. This superior chip provides your customers with lower overhead and delivers a data transfer rate up to 5.0 MBytes/sec – that's two to three times faster than most SCSI chips.

NCR's VME host adapter also features extensive diagnostic LED's designed to help provide easier integration, as well as easy identification of potential trouble. And, its surface-mount technology means greater reliability.

But perhaps the most important feature of this VME-to-SCSI host adapter is the NCR name. Because it means you're getting factory support from the company who initiated SCSI. And a product made by the undisputed leader in designing and manufacturing proven SCSI products.

NCR's VME-to-SCSI host adapter is available now from the NCR SCSI Technology Group.

So don't settle for cheap imitations, call the number below for more information.

NCR

Creating value

NCR SCSI
Technology Group
1-800-325-SCSI

Introducing the VME-to-SCSI Host Adapter. From NCR.

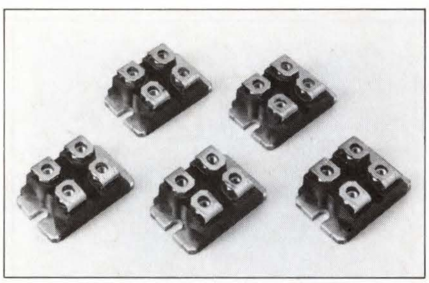
VME is a trademark of Motorola.

CIRCLE NO 201

ISOTOP Packages Tailored for High Power Transistors

Besides offering a range of standard ISOTOP-encapsulated PowerMOS and IGBT devices, Philips now offers ISOTOP packages tailored to user requirements. For large orders, PowerMOS, bipolar transistors, diodes and other semiconductor devices can be combined in a single ISOTOP package.

The four-terminal package, which occupies less than 6 cubic cm, can take 50 V devices passing 110 A with drain-source on-resistance of 10 mΩ, up to devices of 1000 V, 0.5 Ω passing 15 A. More rugged and electrically reliable than externally isolated packages with the same power ratings, the package has a single outline for a wide range of power devices and is internally isolated to 2.5 kV RMS for one minute.



ISOTOP Powerpack tailored for user requirements

The package can be mounted on a printed circuit board. It has very low internal lead inductance and capacitance, and good thermal resistance between junction and mounting base. The package has screw terminals.

CIRCLE NO 1

Rugged Logic-Level MOSFETs Accept 5 V Drive Voltages

A range of logic-level MOSFETs from Philips Components has guaranteed gate-source breakdown voltages of 15 V, rather than the industry standard 10 V. The BUK500 range includes devices that also withstand drain-source voltage spikes of up to 400 V, making them the most rugged logic-level MOSFETs available. The transistors can replace mechanical relays, with drain-source on-resistances down to 40 mΩ, allowing them to pass currents up to 40 A (A 30 mΩ device is currently being developed). They are driven into full saturation by a 5 V gate source, making them ideal for automotive and industrial applications.

The family consists of 14 transistors with maximum drain-source voltages of 50 V, 100 V and 200 V. Depending on crystal size and package, current ratings vary between 12 A and 40 A for the 50 V devices, between 8 A and 25 A for the 100 V devices, and between 5.3 A and 12 A for the 200 V devices. Switching times are comparable to those of standard MOSFETs.

Excellent reliability with very high MTBF allow a maximum operating temperature of 175 °C, rather the normal 150 °C, particularly important for automotive applications.

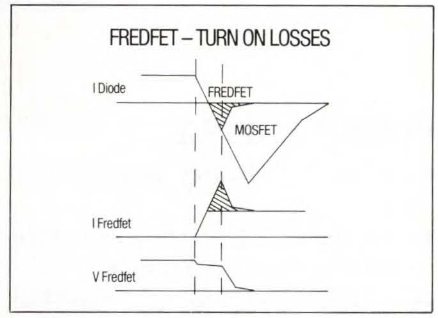
The transistors come in three packages with different power ratings: the TO186, dissipating up to 30 W; the SOT82, dissipating up to 75 W; and the TO220, dissipating up to 125 W. Samples are available.
A 150 W, 30 mΩ device is in development.

CIRCLE NO 2

FREDFETs Reduce Commutation Losses in Bridge Applications

Aimed at half- and full-bridge applications, these 13 FREDFETs combine commutation losses between five and ten times lower than standard MOSFETs with excellent dV/dt behavior. Each member of Philips Components' BUK600 family has an integral Fast-Reverse Epitaxial Diode that offers significant advantages at frequencies greater than 50 kHz in circuits for motor control, inverters and uninterruptible power supplies.

By doping the epitaxial layer of a standard MOSFET, a FREDFET transforms the inherently slow parasitic reverse-biased diode between a MOSFET's source and drain to a fast one. This reduces the device's stored charge, and hence the reverse recovery time by a factor



Turn-on losses: MOSFETS vs. FREDFET

of five or more in practical circuits to as low as 125 ns for a 500 V, 11 A device at 25 °C junction temperature. The doping also keeps leakage currents and drain-source on-resistance down to those of other PowerMOS devices.

The BUK600 family has maximum drain-source voltages between 400 V and 1000 V, while drain-source on-resistances as low as 0.4 Ω lead to high drain currents of a maximum of 14 A for the 400 V transistor and nearly 9 A for the 1000 V devices. Larger crystal sizes will be introduced in early 1989.

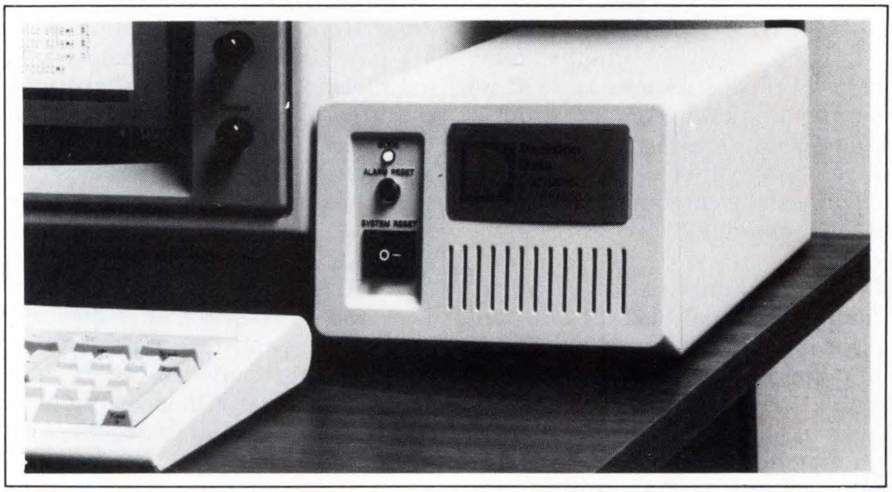
The BUK600 devices come in TO220, SOT93 and SOT199 packages. Samples of the 400 V, 500 V and 600 V devices are available now. Samples of the 800 V and 1000 V devices will be available early next year.

CIRCLE NO 3

COMPONENTS & POWER SUPPLIES

POWER SUPPLY

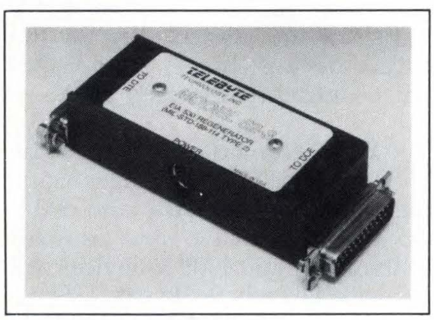
- *Features a 1/2-cycle max transfer time*
- *Input protection includes a fuse and transient suppressor*



The DDCC5920 uninterruptible power system provides 20 minutes of 200W standby backup power for small computer systems. Features include visible and audible power-fail/inverter-on indicators and visible ac-power-restored and normal ac-line-operation indicators. Normal-mode input-output is 102 to 127V ac, and maximum transfer time is 1/2 cycle. A 20A fuse in the primary of the inverter circuit provides output protection; a 3A line fuse combines with a MOV overvoltage transient suppressor to protect the input. The unit weighs 29.1 lbs and measures 5.1×7.7×13.5 in. $295.

Decision Data Computer Corp, 400 Horsham Rd, Horsham, PA 19044. Phone (215) 956-5736.

Circle No 351



REGENERATOR

- *Handles the complete EIA-530 interface*
- *Provides signal amplification in both directions*

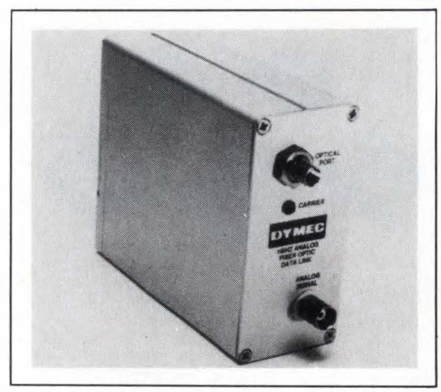
The model 62-3 bidirectional signal regenerator performs the function of a line driver/booster for the complete EIA-530 interface. It handles all thirteen 530 signals—the 10 Category I differential signals and the three Category II single-ended signals. The 62-3 provides signal amplification and regeneration in both directions to increase link transmission distances. The standard length is a function of frequency and varies from 350 ft at 1 MHz to 4000 ft at 100 kHz. Differential inputs terminate in the characteristic impedance of a twisted pair. The units' metal enclosure features two DB-25 connectors (a male and a female) and a mini-DIN connector for power (5V at 0.5A). An optional power supply (Model 62-4PS) is available for $32. $138.

Telebyte Technology Inc, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; in NY, (516) 423-3232.

Circle No 352

OPTICAL LINK

- *Offers variable output levels*
- *Includes an LED that indicates proper operation*

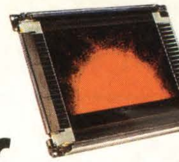


These 1-MHz analog fiber-optic link transmitters and receivers are housed in 3.5×1.75×4.37-in. aluminum cases. The units have front panel BNC- and ST-type connectors for analog signal and optical cables, respectively. An LED indicator signals when the link is functioning properly. The transmitters accommodate either single-ended (Model 6711) or differential (Model 6713) inputs. Both the transmitters and the receiver (Model 6712) come with a rear-panel-mounted, 3-position slide switch that sets the full-scale output voltage range at ±1, ±5, or ±10V. Offset and gain-adjustment controls and a power connector are also mounted on the rear panel. Captive penn-nuts on the bottom of the case allow you to mount the packages to a bulkhead. An optional mounting flange is available for applications where rear access is impossible. 6711 and 6712, $385; 6713, $397. Delivery, stock to six weeks ARO.

Dymec Inc, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1151; in MA, (617) 729-7870. TWX 710-348-6596.

Circle No 353

ONCE YOU'VE SEEN FUJITSU'S AC PLASMA DISPLAY, YOU'LL TAKE A DIM VIEW OF ANYTHING ELSE.



The only way our bright new 8050 display looks anything like the others is through a pair of sunglasses.

That's because the 8050 is without a doubt the brightest, most readable display in its class.

It's the first 10-inch, AC-memory, flat panel display to deliver 640 x 400 resolution with an extraordinary 44 foot-lamberts of brightness. Along with a contrast ratio of greater than 20:1. All in a package just over one inch thick.

In fact, the only thing more impressive than these numbers is looking at the display yourself. Then you'll really appreciate its exclusive solid black background. And the brightness and flicker-free clarity of text and graphics.

And what's truly amazing is that you'll get this remarkable performance under some of the worst possible conditions. Like bright sunlight. And viewing angles up to 120 degrees.

So if your application calls for the clearest images with maximum contrast, call us today at **1-800-556-1234, Ext. 238.** Inside California call, **1-800-441-2345, Ext. 238.** Or write Fujitsu Component of America, Inc., 3330 Scott Boulevard, Santa Clara, CA 95054-3197.

We'll brighten your day.

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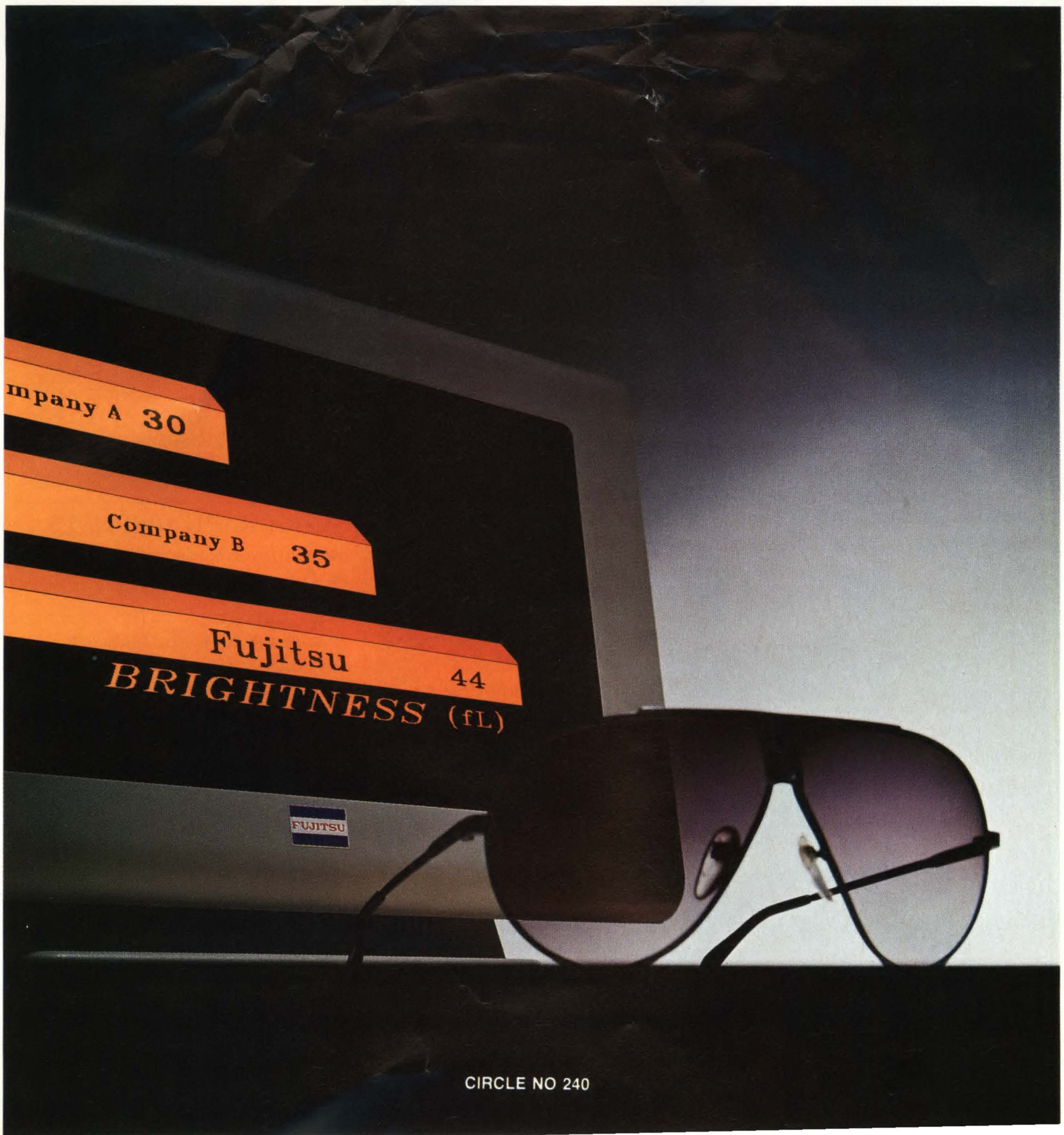
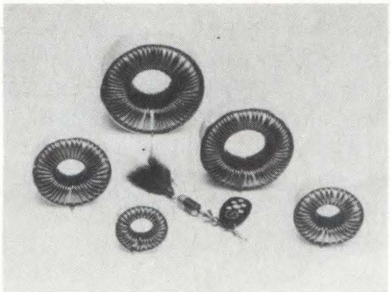


CIRCLE NO 240



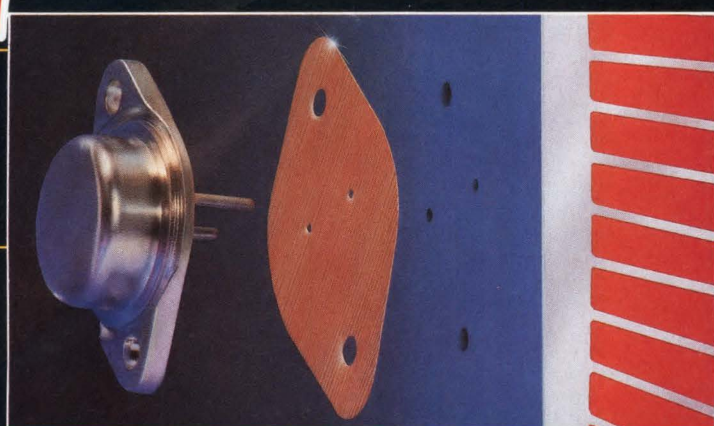
TOROIDS

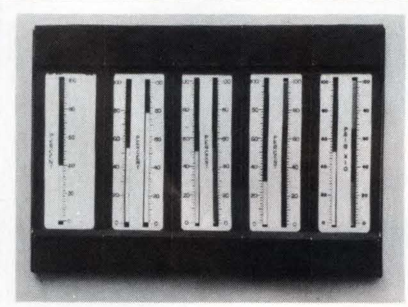
- *Employ core material with a controlled-saturation feature*
- *Produce a closed magnetic field to reduce EMI*

The variable inductance toroids in the Series RL1386 use a special core material (effective to 1 MHz) that has a controlled-saturation feature. Inductance values change as coil current changes, but specific inductance values are repeatable at specific current levels. The toroid design produces a closed magnetic field, which tends to reduce EMI. Models in the line span a standard inductance range of 1.1 to 5600 μH with current ratings ranging from 1.2 to 22A. The five core diameters available range from 1.1 to 2.6 in. The toroids will mount in either the vertical or horizontal position and are also available in a 4-pin mounting boat. Custom and military-grade devices are also available. From $0.90 (10,000). Delivery, stock to six weeks.

Renco Electronics Inc, 60 Jefryn Blvd E, Deer Park, NY 11729. Phone (516) 586-5566. FAX 516-586-5562.

Circle No 354





BAR-GRAPH DISPLAYS

- *Feature 202 elements*
- *Offer ±1% accuracy*

The Lumigraph 9270S electronic bar-graph indicator features a gas-discharge display-panel scale that consists of 202 closely spaced elements. It is available in two systems: as single or dual indicators, which accept and display one or two independent inputs, and as single indicators with two alarm/control setpoints. The units display measured variables as neon-orange bars and indicate alarm set points in red. Unit features include ±0.5% resolution and ±1% accuracy. The units are self-contained and require only power (120V ac) and signal inputs for operation. The two internal plug-in pc boards are designed for

NOW RADSTONE TECHNOLOGY

MIL-STD-VME

From the company that truly knows both military and VME

It took a company that knows both VME and military specifications to design and build the first fully militarized VMEbus boards. . . Plessey Microsystems. Only Plessey offers the totally VME-compatible PMV 68 family of modules for military environments. Processor boards. RAM, EPROM and EEPROM boards. Bubble memory. Even a board for interfacing the VME bus with the 1553B bus. Plus custom Mil VME capabilities.

Full Mil Compliance

Each Plessey military VME board features MIL-STD-883C level B components to meet MIL-E-5400 (airborne), MIL-E-16400 (naval), MIL-E-4158 (ground mobile) and MIL-STD-810 (environmental) specifications. Other features include a bonded aluminum thermal management layer, custom devices and extensive BITE facilities.

Complete ATR Systems Packaging

PMV 68 boards can be furnished separately or assembled into rugged, custom-configured ATR boxes.

Plessey also offers a full range of commercial VME boards, software and development systems for immediate system development.

From the One and Only Source for True Mil-Spec VME

Just call or write for all the details from the one company that truly understands both VME and military applications — Plessey Microsystems. The ultimate supplier for Mil Spec VME.

PLESSEY

CIRCLE NO 227

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Pearl River, NY 10965
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TWX: (710) 541-1512

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Irvine, CA 92718
Tel: (714) 472-2586

Suite 600
2000 E. Lamar Blvd.
Arlington, TX 76006
Tel: (817) 261-9988

FRANCE
BP 74.7-9 rue Denis Papin
78914 Trappes Cedex
Tel: (1) 30.51.49.52
Telex: 696441

GERMANY
D-6090 Rüsselsheim
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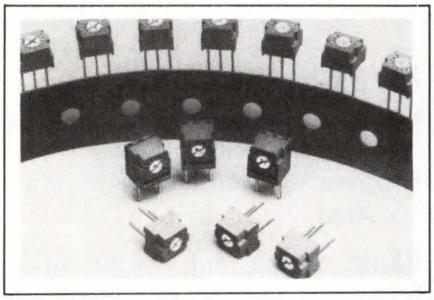
International Instruments, Box 185, North Branford, CT 06471. Phone (203) 481-5721. FAX 203-481-8937.

Circle No 355



TRIMMERS

- *Compatible with pick-and-place equipment*
- *Operate over a −55 to +125°C range*

The model 25 0.25-in. square single-turn cermet trimmer features six pin styles and is available in both side- and top-adjustment configurations. It has a shaft with a cross-slot design to facilitate adjustment and is compatible with pick-and-place equipment. Standard resistance values range from 10Ω to 2 MΩ. The power rating specs at 500 mW, and maximum contact resistance variation equals 1%. The operating range spans −55 to +125°C. Packaging options include tape-and-reel, ammo pack, and magazine. $0.60 (1000).

Beckman Industrial Corp, 4141 Palm St, Fullerton, CA 92635. Phone (714) 447-2510.

Circle No 356

TRANSCEIVER

- *Couples a drop cable to Ethernet/IEEE-802.3 LANs*
- *Has integral LEDs to indicate transceiver status*

The Model 725 Ethernet/IEEE-802.3 transceiver provides an interface between Ethernet trunk or thin-wire coaxial cable and the drop cable to an Ethernet station. It is suitable for connection to Belden 9880 yellow Ethernet trunk cable or Belden 9907 thin-wire coaxial cable, and it has a 15-way D-connector for connection of the drop cable. The transceiver is available with three types of Ethernet tap—an AMP nonintrusive bee-sting tap, an N-type T-piece tap, or a BNC-type T-piece tap. A connector clamp and side locks on the 15-way drop-cable connector prevent accidental disconnection of the drop cable. LEDs on the transceiver provide a continuous indication of the transceiver's power, receive data, transmit data, collision, and SQE test status. You can configure the SQE test function for use with Ethernet or IEEE-802.3 installations. The unit fits inside standard 4×2-in. cable trunking, and it's dust- and splash-proof. It is manufactured and tested to British Standard BS5750 part 2 and has an MTBF of more than 200,000 hours. £239.

Wadsworth Electronics Ltd, Central Ave, East Molesey, Surrey KT8 0QB, UK. Phone 01-941-4716. TLX 892335.

Circle No 357

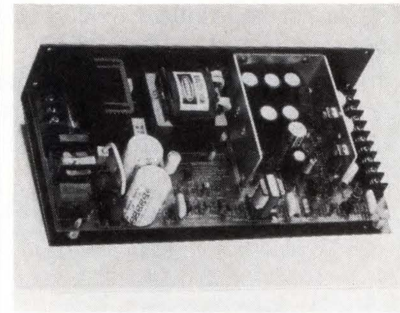
POWER SUPPLIES

- *Provide outputs ranging to 5 kV*
- *Continuously display output current and voltage*

The PS310, PS325, and PS350 are 25W power supplies that provide 1.25-, 2.5-, and 5-kV output capabilities, respectively. Voltage regulation is 0.001% for ±10% line voltage changes, and ripple is less than 0.002% of full scale. Two 4-digit displays provide a continuous readout of current and voltage; a third display indicates which parameter is being entered. The supplies feature arc and short-circuit protection and user-selectable hard and soft current limits. You can adjust the resolution as low as 1V. Connectors accommodate both remote voltage setting/ramping and current and voltage monitoring. The supplies store and recall as many as 10 instrument settings. An optional IEEE-488 bus port allows you to program input settings as well as read output and instrument status. $995.

Stanford Research Systems Inc, 1290D Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-9040. TLX 706891. FAX 408-744-9049.

Circle No 358



POWER SUPPLIES

- *Specifically designed for CRT and disk-drive applications*
- *Offers 65% efficiency at 125W output*

PX125 Series multioutput, open-frame switching power supplies deliver 130W of continuous power. With a highly filtered 12V/1.5A output, they are specifically designed for CRT and disk-drive applications. The units will provide as many as four outputs in various combinations of ±5, ±12, 15, and 24V. The minimum efficiency at 125W output levels is 65%. The operating range spans 0 to 50°C, and line regulation is ±0.5% max at full load. Standard supply features include overvoltage, short-circuit, input surge, and power-fail protection. The units are designed in accordance with UL, CSA, VDE, and IEC specifications, and they meet FCC Class B requirements. $146. Delivery, stock to 10 weeks ARO.

Powerline Inc, 10 Cochituate St, Natick, MA 01760. Phone (617) 655-7987. TWX 510-100-3630. FAX 617-655-7984.

Circle No 359

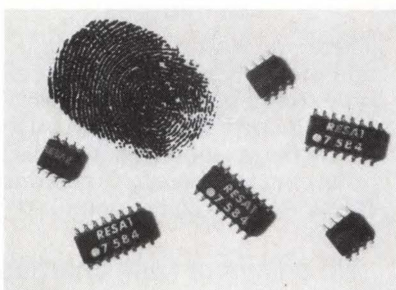
NOISE SOURCES

- *10-MHz to 18-GHz coverage*
- *Come complete with calibration points and charts*

NC 3300 wideband coaxial-type noise sources cover a 10-MHz to 18-GHz frequency range. They have excess noise ratios of 6±0.5 dB. All seven models in the line are available in full- or segmented-band versions. Noise output variation with temperature specs at 0.01 dB/°C, and the operating range is −55 to +85°C. Noise output rise and fall times equal 1 µsec max, and on/off VSWR measures 1.2:1 max. SMA connectors are standard, but any combination of SMA, N, TNC, and BNC is available. Housings can be supplied with threaded mounting holes. Calibration points and charts are provided with each source. From $350.

Noise Com Inc, E 64 Midland Ave, Paramus, NJ 07652. Phone (201) 261-8797. TWX 910-380-8198.

Circle No 360



RESISTOR NETWORKS

- *Are available in surface-mount packages*
- *Feature a TCR of ±10 ppm/°C*

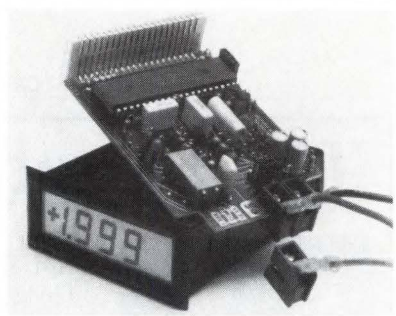
The RMKM Series of small-outline surface-mounting resistor networks feature an absolute temperature coefficient of resistance (TCR) of ±10 ppm/°C over a 0 to 70°C temperature range. The TCR is ±15 ppm/°C between −55 and 0°C and 70 and 125°C. TCR tracking between individual resistors in the same package is a maximum of 5 ppm/°C over the entire −55 to +125°C operating range. Nominal resistance values range from 1 to 200 kΩ with absolute tolerances of ±0.1 to ±1% and relative tolerances of 0.5 to 0.05%. The networks' voltage coefficient of resistance is less than 0.1 ppm/V, and the noise index is typically −45 dB. The RMKM Series includes 8-, 14-, and 16-lead devices. Included are devices that contain four, seven, or eight individual resistors, and devices that contain either two or four center-tapped resistor pairs and one separate resistor. Custom circuit configurations are also available. The 8-lead package has a power rating of 250 mW to 70°C, and the 14- and 16-lead packages have a power rating of 500 mW to 70°C. They can withstand wave or vapor-phase soldering. Guide prices for 8-, 14-, and 16-lead resistor networks are $0.87, $1.35, and $1.35 (1000) respectively.

Sfernice, 199 Blvd de la Madeleine, 06021 Nice Cedex, France. Phone 93446262. TLX 470261.

Circle No 361

Ohmtek, 2160 Liberty Dr, Niagara Falls, NY 14304. Phone (716) 283-4025. TWX 710-524-1653.

Circle No 362



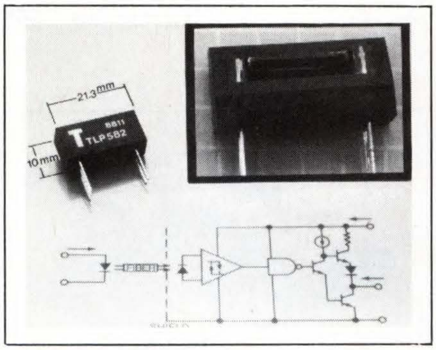
PANEL METERS

- *Available with either LED or LCD digital readout*
- *Offers 20-mV full-scale resolution*

The SM-35XMV and SM-35MV 3½-digit digital panel meters feature LCD- and LED-type readouts, respectively. Both are designed for low-voltage inputs and provide three header-programmable input ranges of 20, 200, and 2000 mV full scale. Internal potentiometers that provide zero-offset capability and continuous fine and course full-scale adjustment allow users to scale the meters to almost any engineering unit of readout. The 20- and 200-mV ranges allow the meters to be scaled for direct reading of all standard 50- and 75-mV current shunts. The units are available with either screw-terminal- or pc-board-type connector inputs. SM-35XMV, $79; SM-35MV, $69.

Texmate Inc, Box 2000, Solana Beach, CA 92075. Phone (619) 481-7177. TWX 910-322-1738.

Circle No 363



PHOTOCOUPLER

- *Includes an optical fiber to increase noise immunity*
- *Features a 3-state output*

The TLP582 photocouplers' design features a 0.5-in.-long optical fiber between the emitter and the detector which, in essence, increases the separation distance between the two. This construction, combined with an internal shield, provides a guaranteed common-mode rejection of 100,000V/μsec. The coupler features a 3-state output and a Schmitt-trigger circuit that operates at 5M bps. The package size measures 21.3×6.5×10 mm. $3 (10,000).

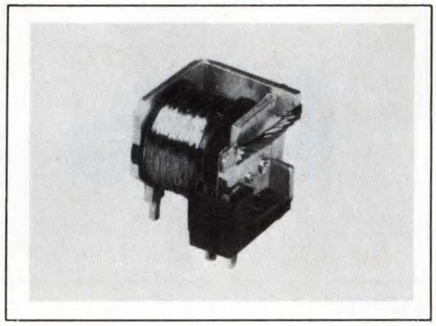
Toshiba America Inc, Semiconductor Products Div, 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000.

Circle No 364

PC-BOARD RELAYS

- *Lifetime exceeds 100,000 operations*
- *Available in spst or spdt contact configurations*

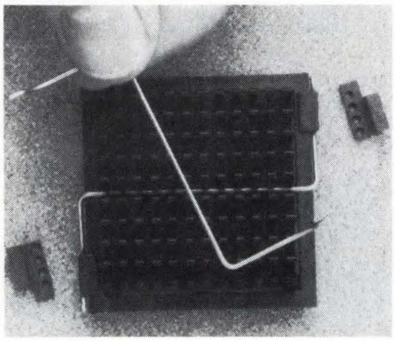
VKP Series pc-board-mountable relays switch 40A. Silver contacts are standard in either spst-NO or spdt contact arrangements. The open-



frame electromechanical relays switch 50 to 500W dc loads and 1000-VA ac loads. Their expected life exceeds 100,000 operations at 40A resistive. The relays are available with coil voltages of 6, 12, and 24V dc; and the nominal coil power dissipation is 1.6W. Initial coil-to-contact breakdown voltage measures 500V dc. The relays occupy less than 0.5 in.^{3} of board space. $1.08 (10,000). Delivery, stock to 10 weeks ARO.

Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2147.

Circle No 365



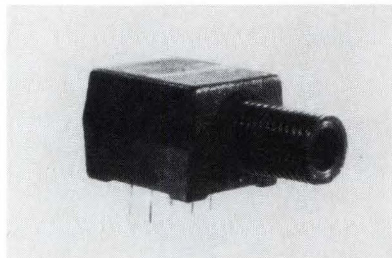
HEAT-SINK MOUNTS

- *Eliminate problems associated with adhesive bonding*
- *Feature easy assembly*

The E-Z Mount assembly provides a mechanical means of attaching a heat sink to a pin-grid array (PGA). Thus, it eliminates the mess and the thermal expansion problems associated with adhesive bonding. The E-Z Mount consists of a spring clip and either a plastic frame or shoes for the PGA. You start the assembly procedure by inserting the PGA into the frame. The spring fits into the heat sink and over the ridges of the frame, securely attaching the heat sink to the PGA. The shoes are useful when board space is tight. The two shoes slip under the four outer pins of the PGA and the spring snaps onto the shoes rather than the frame. You then wave solder the entire assembly to the board. Mounts are available for 11×11-, 14×14-, 15×15-, and 21×21-pin PGA packages. You can use this assembly for extruded-pin or radial-machined heat sinks. $0.40 (1000) for a 15×15-pin mount.

Thermalloy Inc, Box 810839, Dallas, TX 75381. Phone (214) 243-4321. TLX 203965. FAX 214-241-4656.

Circle No 366



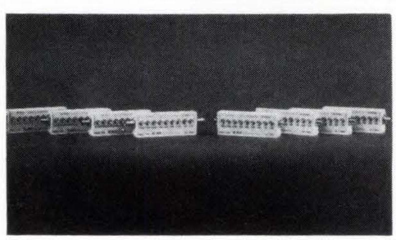
OPTICAL MODULES

- *Transmitter outputs range as high as −16 dBm*
- *Operate at 850 nm*

These fiber-optic transmitter and receiver modules operate at 850 nm and are housed in 8-pin DIPs. HFE4400 Series LED-type transmitters offer outputs ranging from −25 to −16 dBm. HFD3400 Series receivers include a 5M-bps direct-coupled model (HFD3403), a 10M-bps differential-input model (3402), and a 35-MHz analog model (3401). Responsivity specs at 4 mV/μW for the 3401. Sensitivity is 0.6 μW (−32 dBm) and 2.8 μW (−25.5 dBm) for the 3402 and 3403, respectively. Both digital units provide an inverted TTL-type output. All modules feature an optical port that accommodates standard 905- or 906-type SMA connectors. $22.69 to $45.38 per pair (1000).

Micro Switch, Optoelectronics Div, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-5731.

Circle No 367



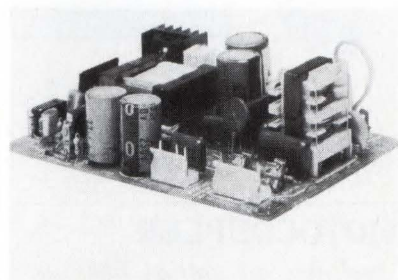
STEP ATTENUATOR

- *Has a 3W power rating*
- *Operates to 3 GHz*

The Model 839 step attenuator features a 3W power rating. It has a 0- to 101-dB attenuation range with a 1-dB step resolution and operates over a dc to 3-GHz frequency range. Impedance specs at 50Ω, and insertion loss ranges from 0.2 to 0.7 dB from dc to 2 GHz. Over the same frequency range, VSWR figures range from 1.1:1 to 1.4:1. $249.

Kay Elemetrics Corp, 12 Maple Ave, Pine Brook, NJ 07058. Phone (201) 227-2000. TWX 710-734-4347. FAX 201-227-7760.

Circle No 368



POWER SUPPLY

- *Designed to power plasma displays*
- *Meets safety and RFI regulations*

PD Series open-frame switching power supplies feature a 75% efficiency and two jumper-selectable input ranges: 100 to 120 and 200 to 240V ac. The two outputs are well-suited for most commercially available plasma displays: 200V dc at 10 to 150 mA and 5V dc at 60 mA. The 200V output has 0.7% line regulation, 2.5% load regulation, and 0.8% temperature drift. Respective figures for the 5V output are 0.2%, 1%, and 1.4%. Ripple and noise for both outputs specs at 1% max, and operating range (without forced cooling) spans 0 to 50°C. The supplies conform to UL/CSA/TUV safety requirements and are designed to meet FCC and VDE Class B RFI rules. The supplies are housed on a board measuring 3.75×5.125 in. $96 (OEM qty).

Panasonic Industrial Co, 2 Panasonic Way, Secaucus, NJ 07094. Phone (201) 348-7000.

Circle No 369

43K+ Dhrystones. 17+ MIPS. 7+ MFlops. 4Mb DRAM. 1 SCSI. One VME Board.

The TP880V from Tadpole

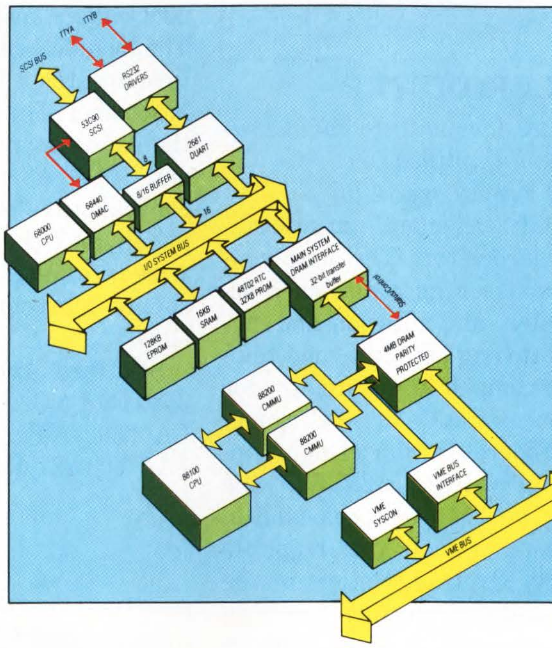
•The Philosophy•

The TP880V is a high performance Single Board Computer for VME based systems. Designed round the Motorola 88000 RISC architecture, the TP880V offers 17MIP, 6MFlop performance at 20MHz and provides a very high level of integration of processing and I/O features on a single card. Tadpole's 88K C Compiler was specially developed to take full advantage of the 88000 RISC architecture.

•The Specification•

- MC88100 RISC processor (20-33MHz)
- 16Kb MC88200 cache/MMU instruction cache
- 16Kb MC88200 cache/MMU data cache
- 4-16Mb Nibble mode parity-protected DRAM
- I/O Subsystem MC68000/ 68440CPU/DMA
- 53C90 high performance sync/asynchronous SCSI
- 2 RS232 Ports • 128Kb-1Mb EPROM
- Extensive diagnostics capabilities
- Full VME Interface Rev C.1 IEEE 1014
- DTB Master-DTB Slave Syscon interrupter/handler
- 64Kb SRAM battery-backed RTC
- TP-CDS/88K advanced C development environment
- T-Mon 88K Monitor with extensive SCSI support
- TP-IX*

•The Design•



• The Evidence•

Tadpole Technology

the driving force in 32-bit design

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Tel: 0223 461000
Fax: 0223 460727

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2157 O'Toole Avenue
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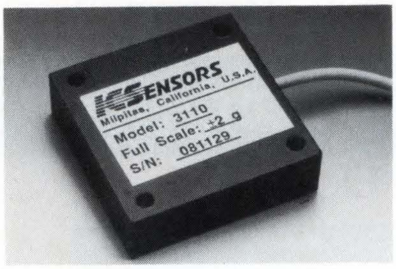
California, 95131, USA
Tel: 0101-408-435-8223
Fax: 0101-408-435-8482

T A D P O L E

*UNIX is a trademark of A T & T *TP-IX V.3.1 is derived from UNIX V.3.1*



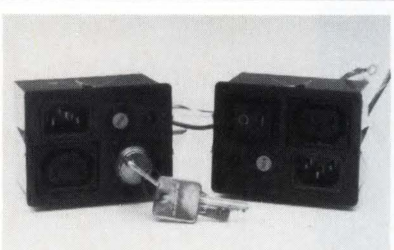
ACCELEROMETER

- *Includes temperature compensation and amplification*
- *Single supply operation*

Model 3110 is a general-purpose silicon accelerometer. The unit consists of a silicon micromachined accelerometer, amplification and signal-conditioning circuitry, and temperature-compensation circuitry for operation over a 0- to 50°C range. The unit operates from a single supply and provides a ±2V full-scale output. The 3110 features built-in damping to provide a dc response capability. Overrange stops in the silicon microstructure provide shock protection. Standard units offer a ±1- to ±100g measurement capability. From $268. Delivery, stock to six weeks ARO.

IC Sensors, 1701 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1800.

Circle No 370



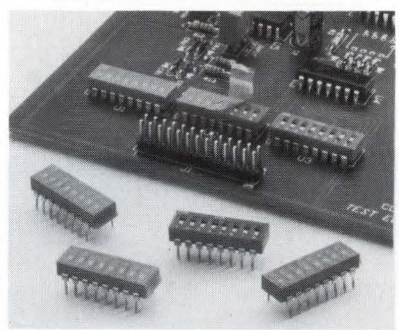
EMI FILTERS

- *Snap-in mounting feature for positive panel bonding*
- *Include IEC accessories*

Rated for 6A/250V ac or 15A/115V ac, EMI input power module filters function in both normal- and controlled-access applications. You can order models with a rocker switch for normal-access applications or a keylock on/off switch that limits unauthorized access to the input power. The modules have a number of International Electro Technical Commission accessories—a power input receptacle, a fuse, an auxiliary outlet, and an indicator lamp. The modules' snap-in mounting feature ensures a positive bond to the host panel. The filter modules meet the safety standards of UL, CSA, and TUV. All module controls are conveniently located on the front panel, and the modules are prewired to facilitate filter/power-supply interconnections. $24 to $64 (1000).

Stanford Applied Engineering, 3520 De La Cruz Blvd, Santa Clara, CA 95054. Phone (408) 988-0700. FAX 408-727-6438.

Circle No 371



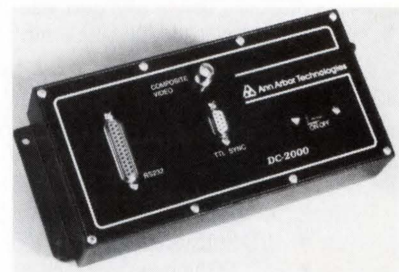
DIP SWITCH

- *Compatible with automatic insertion equipment*
- *Housings have a 94V-0 UL rating*

The LD08 spst, 8-position DIP switch is compatible with automatic insertion equipment and is tape-sealed to withstand wave soldering and cleaning processes. Its contacts are rated for 100 mA at 5V dc or 25 mA at 25V dc. The switches will carry 100 mA max and have a 2000-cycle lifetime. Maximum initial contact resistance is 50 mΩ. Insulation resistance and dielectric strength spec at $10^9\Omega$ and 500V rms, respectively. The glass-filled polyester housings and the glass-filled nylon actuators have a 94V-0 UL rating. The contacts are precious metal over copper alloy, and the terminals are solder clad over copper alloy. $1.25 (1000).

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400.

Circle No 372



CONTROLLER

- *Conforms to ANSI standards*
- *Designed for factory and commercial applications*

The DC2000 video controller converts RS-232C serial data to RS-170 (composite video) and TTL Sync (IBM MDA-compatible) for display on commercially available monitors. Designed for factory and commercial applications, the unit conforms to ANSI standards (X3.4, X3.41, and X3.64) and is compatible with DEC VT-52, VT-100, and VT-220 terminals. The unit provides remote display of computer-generated data in an 80-character×24-line format. It displays characters with a full range of visual attributes including bold, blinking, underlining, reverse video, double wide, double high, and double size. The controller easily rack-mounts for custom installations. $495.

Ann Arbor Technologies, Box 3083, Ann Arbor, MI 48106. Phone (313) 429-3102. FAX 313-662-3707.

Circle No 373

68030 UNIX® or VRTX® Multibus II Single Board Computer

The TP33M from Tadpole

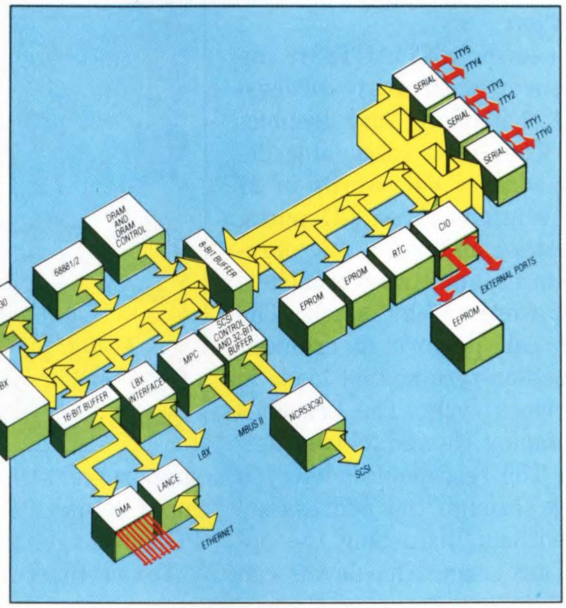
• The Philosophy •

The TP33M is designed to bring together on a fully configured single board computer the outstanding performance of two leading edge technologies: INTEL Multibus II and the 16-33 MHz MC 68030 CISC processor.

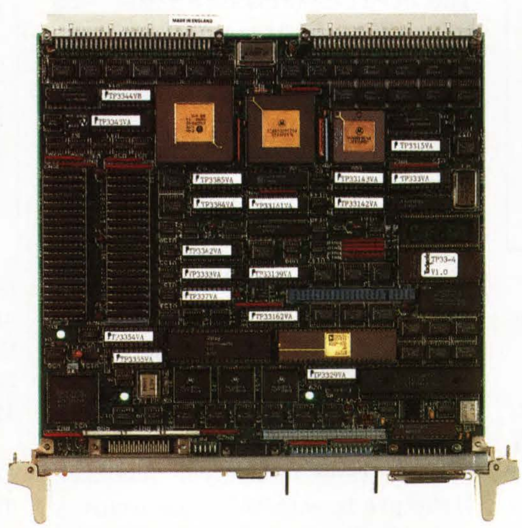
• The Specification •

- MC68030 processor 16-33MHz
- 4-16Mb Nibble mode DRAM
- Custom 32-bit DMA controller
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface
- AMD Lance IEEE 802.3 Ethernet with DMA
- 6 x RS232 ports
- Multibus II/iSBX/iLBX II interfaces
- Battery backed-up real time clock
- 2Kb SRAM • 256Kb EPROM
- TP-IX V.3.1* • VRTX
- VRTX - TP-IX* communications software
- Intel transport layer protocol drivers

• The Design •



• The Evidence •



Tadpole Technology

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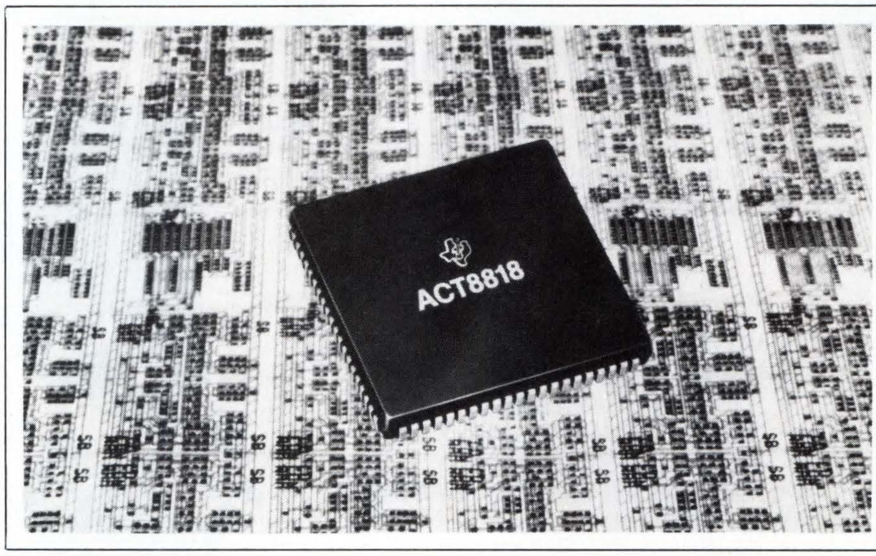
UNIX is a trademark of A T & T Multibus II, iSBX, iPSB and iLBX are trademarks of the Intel Corporation Ethernet is a trademark of the Xerox Corporation
*VRTX is a trademark of Ready Systems *TP-IX V.3.1 is derived from UNIX V.3.1*

INTEGRATED CIRCUITS

MICROSEQUENCER

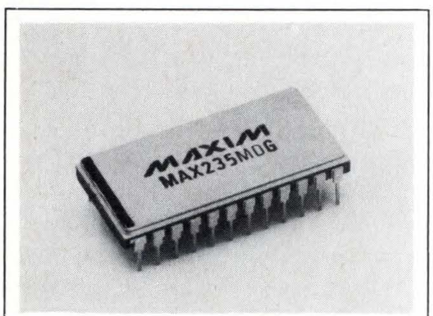
- *Provides 16-bit accuracy*
- *Features 27-nsec next-address generation*

You can use the SN74ACT8818 microsequencer with array processors, I/O controllers, and graphics engines. The 16-bit cascadable device can address 64k words in 27 nsec. It contains three I/O ports, two register/counters, a microprogram counter, multiway branches, and a 65-word × 16-bit stack. The counters can perform decrement and branch-on-zero nested loops in a single clock cycle. The branches let you employ 16- and 32-way networking. The read pointer lets you backtrack through the address sequence without disturbing the operational program. The device can support real-time vectored interrupts. 84-pin PLCC, $48.80; 84-pin PGA package, $67.10 (1000).



Texas Instruments Inc, Semiconductor Group (SC-847), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 375



MILITARY RS-232C IC

- *Provides five drivers and receivers*
- *Requires no external capacitors*

The MAX235M military RS-232C circuit operates from a single 5V supply and provides a low-power shutdown feature. It's available in a 24-pin side-brazed package and needs no external capacitors. Its charge-pump voltage converter generates the ±10V required for RS-232C compatibility. The five receiver outputs are CMOS and TTL compatible, and you can put them in a high-impedance mode via an enable pin. The low-power shutdown mode reduces power consumption from 5 mA to 10 μA. The on-chip capacitors optimize board space. The device operates over the −55 to +125°C military temperature range. $44 (100). Delivery, four to six weeks ARO.

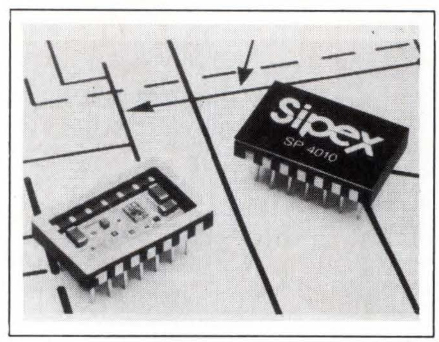
Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 376

BUFFER AMPLIFIER

- *Provides 16-bit accuracy*
- *Has a 60-MHz bandwidth*

The SP4010 buffer amplifier couples a unity-gain voltage signal follower with a transconductance feedback structure to achieve 16-bit accuracy and a 60-MHz amplifier bandwidth. The amplifier also features a slew rate of 1000V/μsec and a settling time of 150 nsec to 0.005% for a 10V step. Its offset voltage is 1 mV typ and 2 mV max. The specified harmonic distortion of −100 dB at 10 kHz and −80 dB at 1 MHz enables the amplifier to buffer high-speed, high-resolution A/D converters. Packaged in a 14-pin ceramic DIP, the SP4010 operates from a ±15V supply and consumes 360 mW. Commercial units (0 to 70°C), $44.50; MIL-STD-883C (−55 to 125°C), $82.50 (100).



Sipex Corp, Hybrid Systems Div, 22 Linnell Circle, Billerica, MA 01821. Phone (508) 667-8700.

Circle No 377

COLUMN DRIVER

- *Features 24 channels*
- *Programmable shift register*

Designed for both commercial and military thin-film electroluminescent (TFEL) flat-panel displays, the HV08 column driver provides 24 channels. The chip uses transistors

68030 - VME
The Real *Single* Board Computer

The TP32V from Tadpole

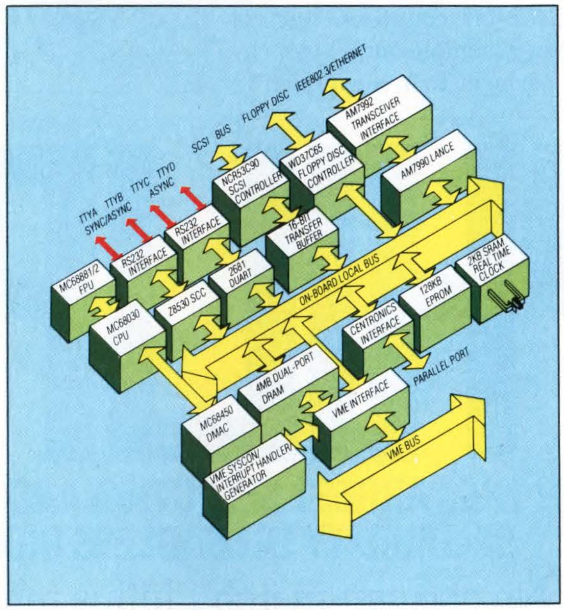
•The Philosophy•

Designed for optimum system performance from a single full IEE 1014 VME board, the TP32V needs no other cards, piggy-backs or mezzanines to deliver the full potential of the 16-33 MHz MC68030. To maximise overall throughput, all the on-board I/O facilities were designed to take advantage of hardware transfer buffers, DMA facilities and advanced DRAM arbitration techniques between competing resources.

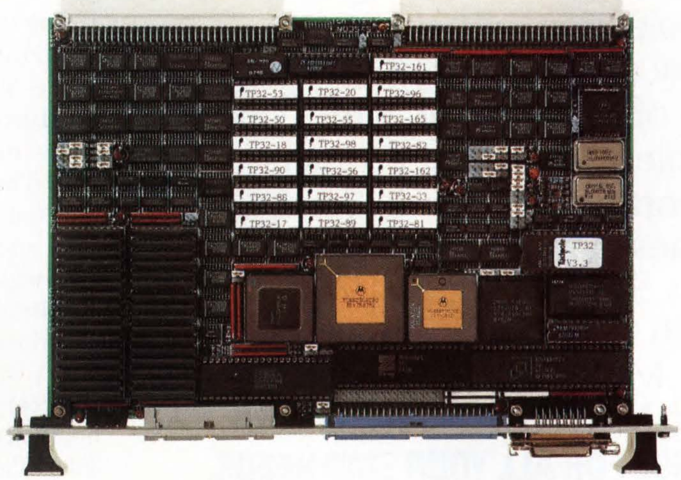
•The Specification•

- MC68030 16-33MHz
- MC68450 4-channel DMA controller
- 4Mb multi-ported nibble-mode DRAM
- AMD Lance IEEE 802.3 Ethernet with DMA
- Z8530 SCC giving two DMA-driven RS232 sync/asynchronous ports and two further RS232 asynchrous ports
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface • Floppy disk controller
- Full VME Rev C.1 IEEE 1014 interface
- 64-512Kb EPROM • Battery-backed RTC/SRAM
- Full debug monitor • Optional MC68881/2 FPU
- TP-IX/68K version of UNIX V.3.1* • NFS, RFS, TCP/IP

•The Design•



• The Evidence•



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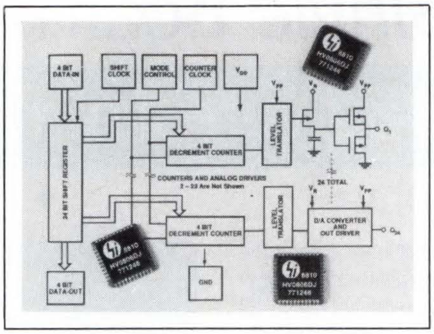
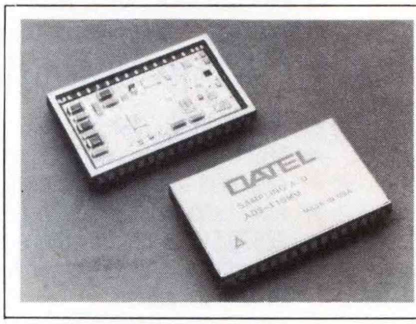
T A D P O L E

with a low threshold voltage to reduce streaking and provide more accurate grey-shade selection. A control pin lets you program the shift-register direction either clockwise or counterclockwise. The driver provides four 24-bit shift registers, 24 8-bit counters, and 24 high-voltage sample and hold circuits to perform D/A conversion to one of 16 voltage levels corresponding to 16 shades of grey. The HV08 comes in 44-pin ceramic or plastic J-lead packages. MIL-STD-883 devices are available. 44-pin plastic, $9.96 (1000).



Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94088. Phone (408) 744-0100. TLX 6839143.

Circle No 378



HYBRID ADCs

- *Perform 10-bit A/D conversion*
- *Support single- or multichannel applications*

Combining a 10-bit sampling ADC with a tracking S/H amplifier, the ADS-115 and ADS-116 support single- or multichannel applications. Hermetically sealed, both units perform over the 0 to 70°C commercial and −55 to +125°C military temperature ranges. The ADS-115 accepts unipolar signals from 0 to 10V. The ADS-116 provides a bipolar input range of −10 to +10V at full scale. The full-power input bandwidth is 60 kHz (10V p-p) with a typical harmonic distortion of −60 dB. Both units operate from ±5 or ±15V supplies. $365.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. TLX 951340.

Circle No 379

LCD CONTROLLER

- *Can handle 16×40-character LCDs*
- *Features 256 built-in windows*

The CY325 is a 5V CMOS device that provides control for LCDs with as many as 16×40 characters and

The MC88000 RISC Multibus II Single Board Computer

The TP880M from Tadpole

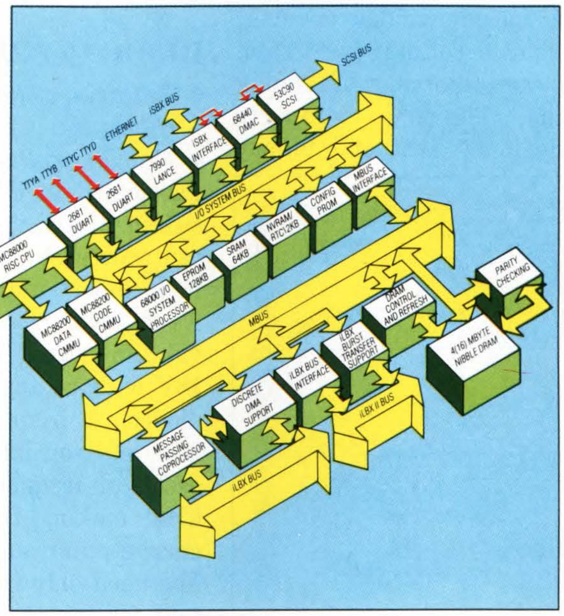
•The Philosophy•

The TP880M design brings together the outstanding performance of the Motorola MC88000 RISC processor set, the power of the full MultibusII/iLBX II interfaces, an MC68000/68440 I/O subsystem with SCSI and Ethernet, and the specially designed Tadpole 88000 RISC optimising C Compiler. The result is an outstanding product that offers users the very best of current SBC technology.

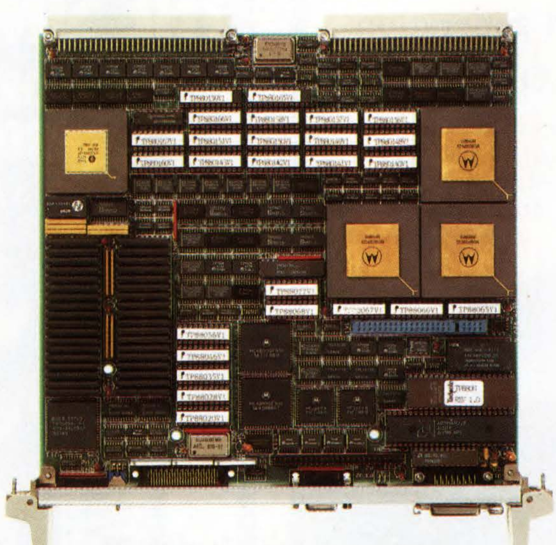
•The Specification•

- MC88100 RISC processor (20-33MHz)
- 16Kb MC88200 cache/MMU instruction cache
- 16Kb MC88200 cache/MMU data cache
- 4-16Mb Nibble mode parity-protected DRAM
- iPSB interface implemented using the Intel Message Passing Coprocessor (MPC)
- iLBX interface and iSBX connector
- I/O Subsystem MC68000/68440 CPU/DMA provides SCSI 4 RS232 ports • Up to 128Kb EPROM
- 64Kb SRAM and optional ETHERNET networking
- TP-IX V.3.1*
- TP-CDS/88K advanced C development environment
- T-Mon 88K Monitor with extensive SCSI support

•The Design•



•The Evidence•



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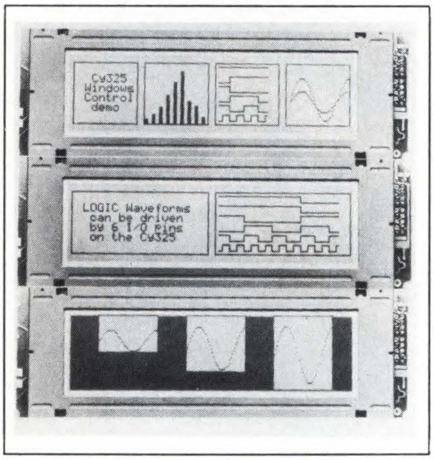
T A D P O L E

128×240 pixels. The chip allows either parallel 8-bit or RS-232C serial interface to any standard computer. The CY325 has a built-in character font, and its 256 built-in windows support text, plotting, bar graphs, and waveforms. Function-oriented commands include window opening, erasing, and scrolling; bar-graph drawing; and plotting of analog waveforms. The chip supports ASCII decimal, hex, and binary



data. 40-pin DIP, $20 (1000).

Cybernetic Micro Systems, Box 3000, San Gregorio, CA 94074. Phone (415) 726-3000. TWX 910-350-5842.

Circle No 380

DC/DC CONVERTER

- *Features switched-capacitor architecture*
- *Provides voltages to 18V*

Fabricated in CMOS, the TSC962 switched-capacitor dc/dc converter can source 80 mA of current. The IC includes an on-chip zener diode. As an inverter, the device can provide an output voltage from 3 to 18V without any need for external diodes. A frequency-doubling feature lets you increase the internal oscillator frequency from 12 to 24 kHz, making the use of smaller charge-pump capacitors possible. You need only two external capacitors for inverter applications. For parallel converter applications, you can use an external clock to synchronize the internal oscillators. The TSC962 is available in 8-pin plastic DIPs, 8-pin ceramic DIPs, or 8-pin wide-body, small-outline packages. From $2.71 (100).

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (415) 968-9241. TWX 910-379-6494.

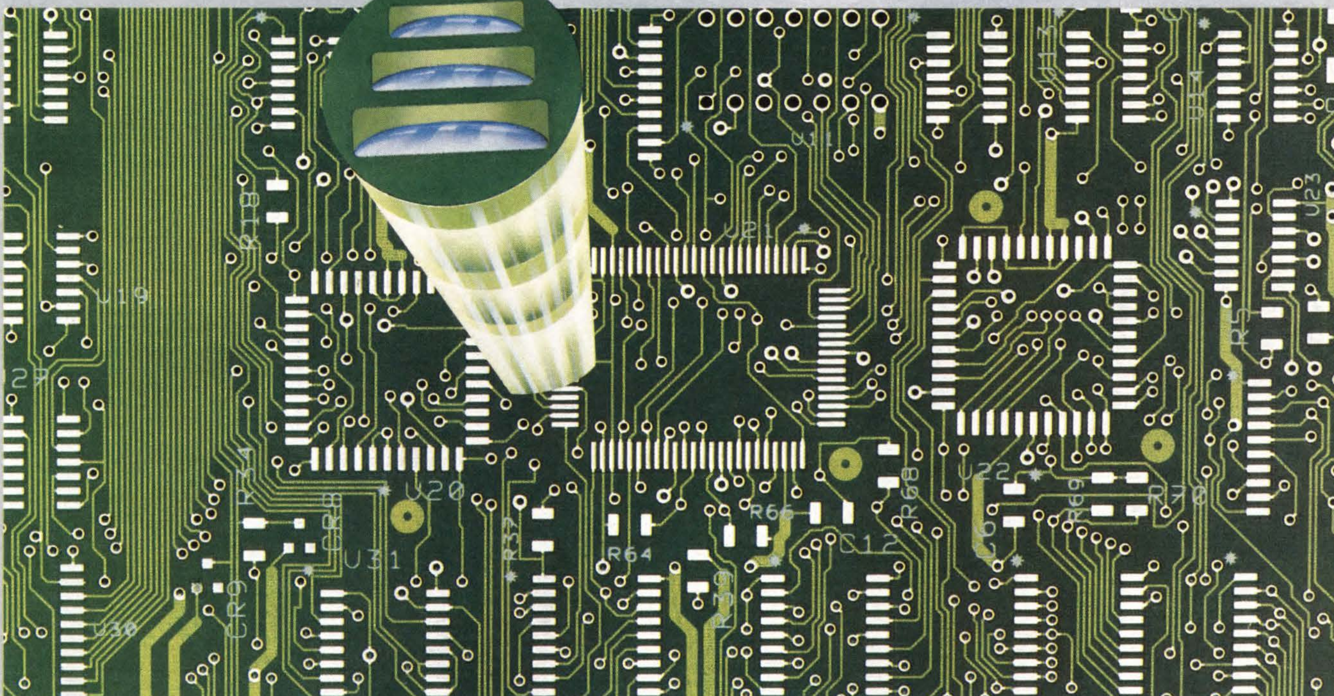
Circle No 381

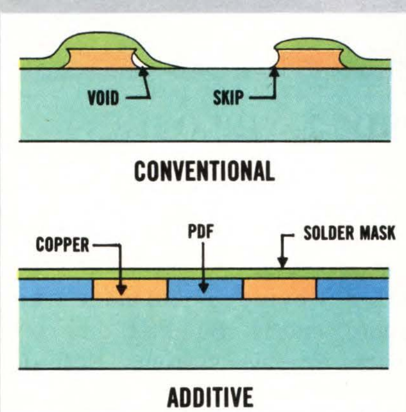
SHIFT REGISTERS

- *Operate in four synchronous or asynchronous modes*
- *Combine 3-state output with a buffered input for each I/O line*

The CD54/74AC/ACT299 and CD54/74AC/ACT323 8-input shift registers provide parallel I/O terminals. Both versions meet JEDEC standards for advanced CMOS logic devices. The registers provide high-speed switching; the maximum

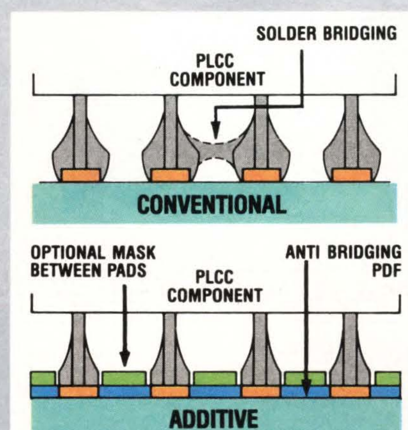
HIGH FIRST PASS SMT ASSEMBLY YIELD STARTS AT THE SURFACE.



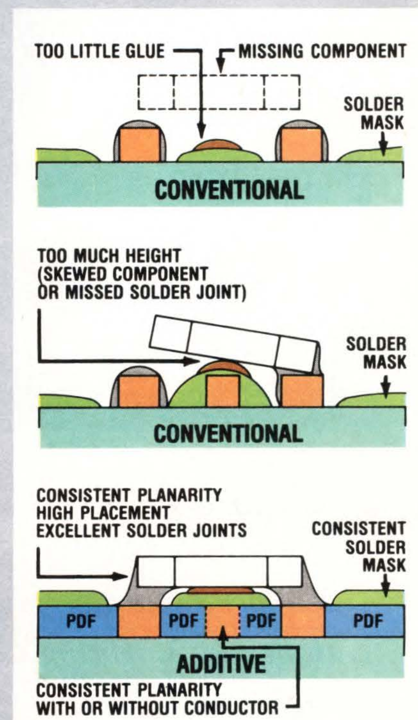


Better solder masking
The PDF dielectric used to define lines and spaces (down to 0.003 inches) totally encapsulates conductor and pad sidewalls. This near-flush surface allows uniform and precisely registered permanent *Solder Mask Over Bare Copper* without skips, smear, bleed, or adhesion loss. The solder mask applied is custom selected to match with the precise placement-soldering-cleaning system used on your assembly line.

Eliminates soldering problems
Choice of either anti-tarnish protected bare copper or computer controlled hot air leveled solder provides the maximum process window for optimum solderability in your soldering system. Bottomside flow soldering is virtually flawless because of the natural solder resistance of the perfectly registered permanent dielectric between every pad. Troublesome solder paste application is made easy because of the flush surface presented by the PWB. Reflow soldering of high pitch PLCC's (tested down to 0.020″ pitch) without solder bridging or touch-up becomes practical when you specify our unique Micro-socket™ solder mask option.

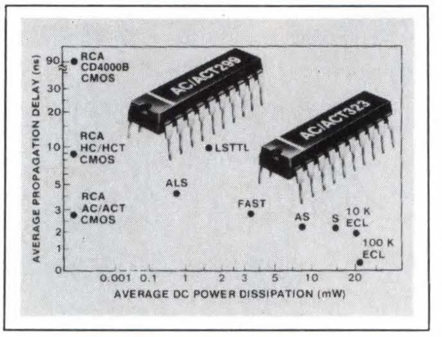


Trouble-free component placement
The uniform, near-flush surface of Additive Surface Mount Circuits provides the ideal planarity for component placement of all common surface mount devices. Whether you're glueing down simple chip passives and SOT's or paste and reflow mounting "super-high" pin count PLCC's and Quads, the problems of uneven glue application, skewing, glue smear, paste skips or bleed can be eliminated. This feature alone can provide the highest "first-pass" pick-and-place yield opportunity in the business.



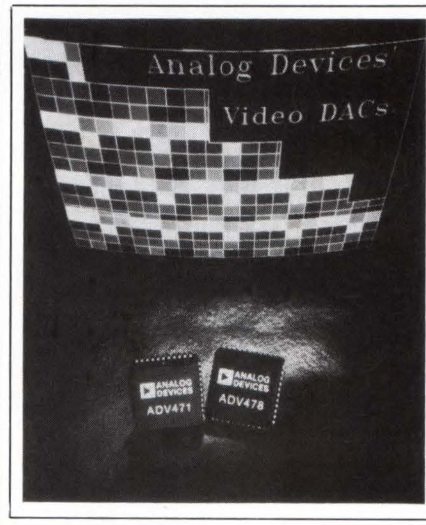
ADDITIVE PRODUCTS DIVISION
KOLLMORGEN CORPORATION
P.O. Box 700, Aquebogue, NY 11931

propagation delay from input clock pulse to output data is 12.9 nsec. In addition, the devices offer four synchronous or asynchronous modes that are selected by two input lines. The ACT299 is reset asynchronously; the ACT323 is reset synchronously. You can cascade both registers to receive data in multiples of 8 bits. The CD54/74AC types operate from a 1.5 to 5.5V supply; the CD54/74ACT types operate from a 4.5 to 5.5V supply. The devices come in die form, a 20-lead plastic DIP, or a 20-lead surface-mount plastic package. $3.71 (100).



GE Solid State, Route 202, Somerville, NJ 08876. Phone (201) 685-6562.

INQUIRE DIRECT



TRIPLE VIDEO DACs

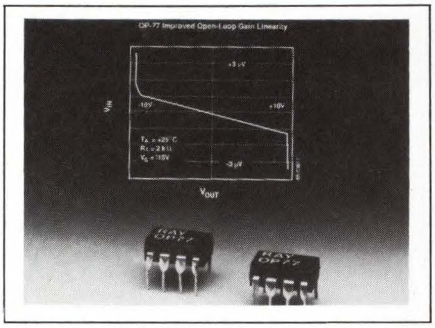
- *Work with VGA graphics standard*
- *Outputs are RS-343A compatible*

The ADV471 and ADV478 video DACs provide performance upgrades for the IBM PS/2 and compatible graphics systems. Both devices are compatible with the PS/2's VGA graphics standard. The ADV478 provides a 256×24-bit color-palette lookup RAM table driving triple 8-bit video DACs; its palette sports 16.7M colors. The ADV471 has a 256×18-bit, 256-color-palette lookup table with triple 6-bit DACs. For compatibility, you can configure the 8-bit device to look like the 6-bit part. The devices have 15 color-overlay registers that let you display overlaid cursors, grids, and menus independently of the main color palette. These RAM/DACs are functionally identical to the Bt478 and Bt471 video DACs. Video outputs are RS-343A compatible and can directly drive a doubly terminated 75Ω load;

these outputs are also RS-170 compatible for singly terminated loads. Clock rates of 35, 50, and 80 MHz are available. ADV471, from $29 to $57; ADV478, $41 to $89 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TLX 924491.

Circle No 383



PRECISION OP AMP

- *5000V/mV minimum gain*
- *Features 25-mV max V_{os}*

The OP-77 operational amplifier is a direct replacement for OP-07, 108, 725, and 741 sockets, and is an improved second-source for the industry-standard OP-77. The op amp's open-loop gain of more than 10 million, maintained over a ± 10V output range, eliminates system nonlinearities. Consuming 35 mW, the amplifier provides a 25-mV max V_{os}. CMRR is 120 dB (min), and PSRR is 110 dB (min). The vendor offers LCC, SOIC, TO-99, and plastic and ceramic DIP packages. Processing for MIL-STD-883B is also available. $1.25 (100).

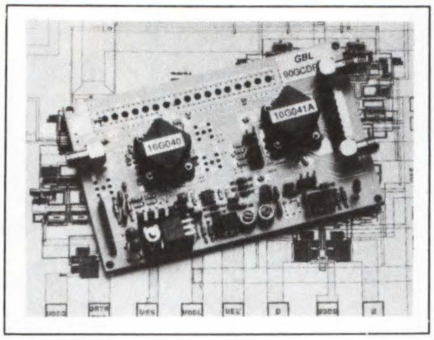
Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043. Phone (415) 968-9211. TWX 910-379-6484.

Circle No 384

FIBER-OPTIC IC

- *Provides clock and data recovery*
- *For high-speed NRZ formats*

The 16G040 clock and data recovery IC allows fiber-optic communications designers to implement a



phase-locked loop (PLL) for clock extraction from high-speed NRZ-format data streams. The 16G040 phase-locks an on-chip VCO or external clock source directly to an incoming digital data stream while simultaneously retiming and regenerating the data stream. The 16G040's center frequency is broadly adjustable and tracks the data

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We Put the STD Bus on a Card.

Octagon's 9500 System Card is a great solution to today's industrial needs, because everything you need is on one board. The 9500, an IBM PC™ and our PC SmartLINK™ are all you need to program and get your application running. It's convenient, it's easy.

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- The 9500 can replace 3 to 7 cards in a typical application. That means no mixing and matching hardware.

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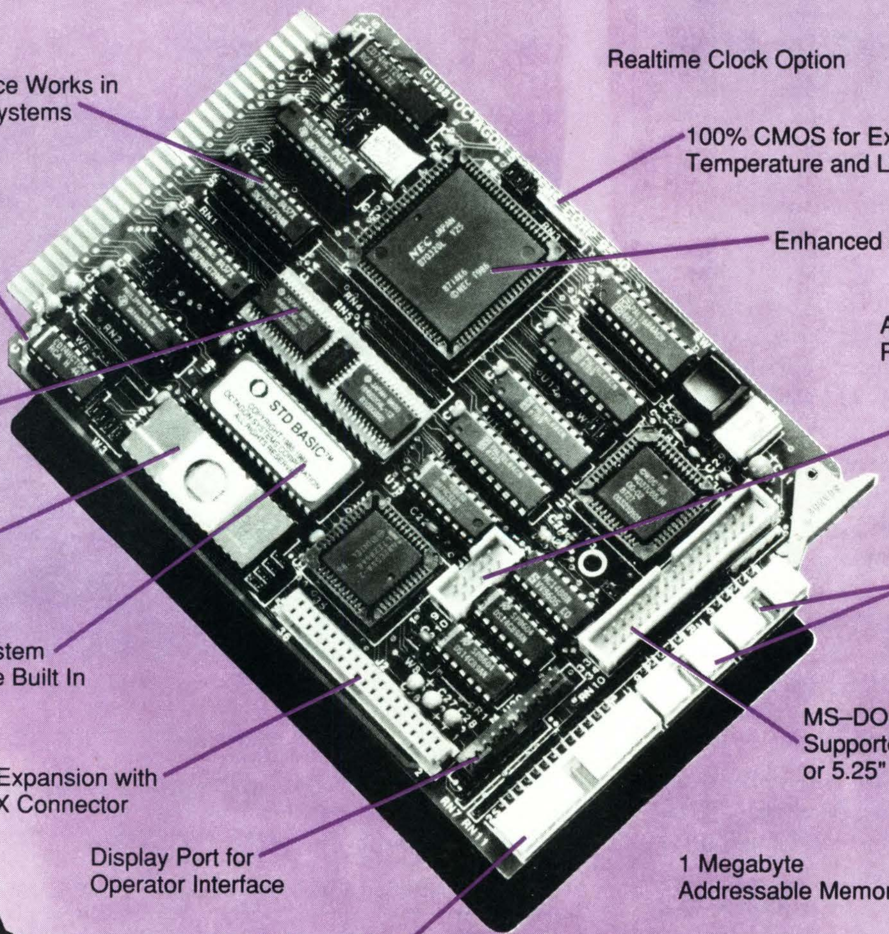

MEMBER STDMG STD MANUFACTURER'S GROUP

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OCTAGON SYSTEMS CORPORATION
6510 W. 91st Ave.
Westminster, CO 80030
303–426–8540
FAX: 303–426–8126

CIRCLE NO 228

rate automatically. A demonstration board (90GCDR-DX), which includes a 16G040 and a 10G041A time-division demultiplexer, is tunable from about 100 to 1000M bits/sec. The 16G040, $75 (1000); the 90GCDR-DX, $1125 each.

GigaBit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320. Phone (805) 499-0610. TLX 6711358.

Circle No 385

RANDOM LOGIC IC

- *Complies with MIL-STD-883*
- *Combines field programability with gate-array complexity*

Designed for military applications, the PLHS501 random logic IC complies with MIL-STD-883. The device provides a high pin count and a flexible network of interconnects. The NAND/NAND structure maximizes interconnect flexibility. Using DeMorgan's theorem, you can implement any level of logic function. You don't have to exit and reenter the device to construct additional logic levels. The device has 24 dedicated inputs and 72 NAND gates with internal foldback paths. An additional 44 NAND gates drive 16 dedicated outputs and 8 bidirectional I/Os. The maximum propagation delay from input to output for a single logic level is 35 nsec. In a 64-pin ceramic DIP, $94.50 (100).

Signetics Corp, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 386

POWER DRIVER

- *Drives 60V loads*
- *Has a logic-level control input and diagnostic output*

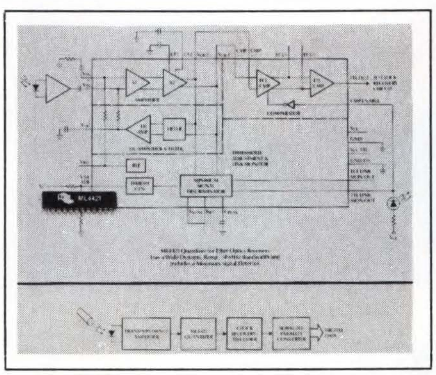
Configured as a high-side driver, the VM200's 40-mΩ on-resistance and 60V output withstand capability suit it for driving loads such as dc motors, lamps, and solenoids. The device has a logic-level control input, and an open-collector diagnostic output that is activated by overload, over-temperature, and open-circuit load conditions. The open-circuit condition is flagged when the current in the device's output stage falls below 0.4A. Internal circuitry prevents false diagnostic outputs under noisy load conditions. The device has internal circuitry for inductive load voltage clamping, surge current limiting, and thermal shutdown. It is packaged in a Pentawatt power package. Around $6.60 (1000).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 387

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 388



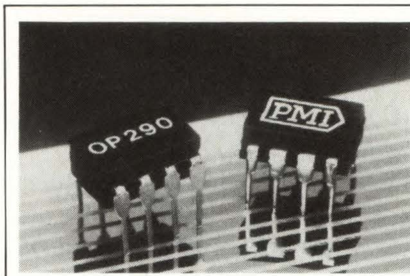
DATA QUANTIZER

- *Converts analog signals to digital pulses*
- *Provides output data at TTL or ECL levels*

The ML4421 is a data quantizer that converts analog signals in fiber-optic receivers to digital pulses. The unit is compatible with Hewlett-Packard's HFBR-24X6 fiber-optic receiver and preamplifier. A dual-stage wideband amplifier, which features an adjustable bandwidth, drives a fast ECL comparator. The output data of the device is available at either ECL or TTL levels. The chip is capable of data rates to 100M baud utilizing the full 50-MHz max bandwidth. The quantizer has a 100-μV noise spec and a dynamic range of 55 dB. The unit comes in either a 24-pin DIP or a 24-pin plastic leaded chip carrier. $6.50 (1000).

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

Circle No 390



DUAL OP AMP

- *Draws <20 μA per amplifier*
- *Operates from single or dual supplies*

The OP-290 dual op amp draws <20 μA for each amplifier, but can drive more than 5 mA/amplifier into a load. It operates from a single supply of 1.6 to 36V, or from a dual supply of ±0.8 to ±18V. In single-supply applications, the OP-290 allows zero-in, zero-out capability. The offset voltage is <200 μV, and the offset voltage drift is only 2 μV/°C over the military temperature range. The chip has a CMRR of 90 dB and a PSRR of 5.6 μV/V max. 8-pin plastic DIP, $2.50; ceramic DIP, $3.40; military-grade ceramic DIP, $9.50 (100).

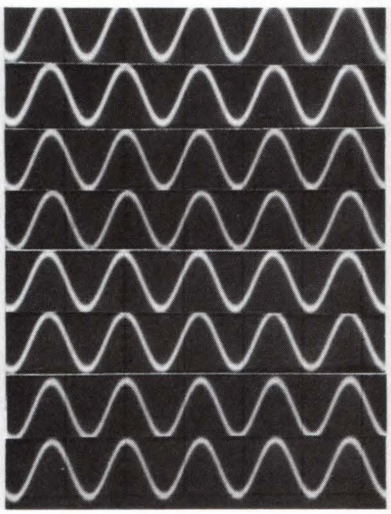
Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TLX 713719541.

Circle No 391

QUAD CMOS OP AMP

- *Operates from single or dual supplies*
- *Features a maximum supply current of 1 mA*

Fabricated in CMOS, the ALD-4701 quad op amp features a maximum supply current of 1 mA for all four amplifiers. It operates from a single supply of 2 to 12V, or from a dual supply of ±1 to ±6V. Each amplifier operates with rail-to-rail input and output signal voltages. The symmetrical push-pull output stage can drive loads of 50 pF and 10 kΩ. Other features include an input bias current of 30 pA max, a bandwidth of 700 kHz, and a slew rate of 0.7 V/μsec. Channel separation is 120 dB, and PSRR and CMRR are both 65 dB min. The large-signal voltage gain is typically 100V/mV. Plastic DIP, $3.63; military ceramic DIP, $6.73; small-outline IC package, $3.99 (100).



Advanced Linear Devices, 1030 W Maude Ave, Sunnyvale, CA 94086. Phone (408) 720-8737. TWX 510-100-6588.

Circle No 392

HALL-EFFECT IC

- *Provides a linear output proportional to flux density*
- *Has an on-chip temperature sensor*

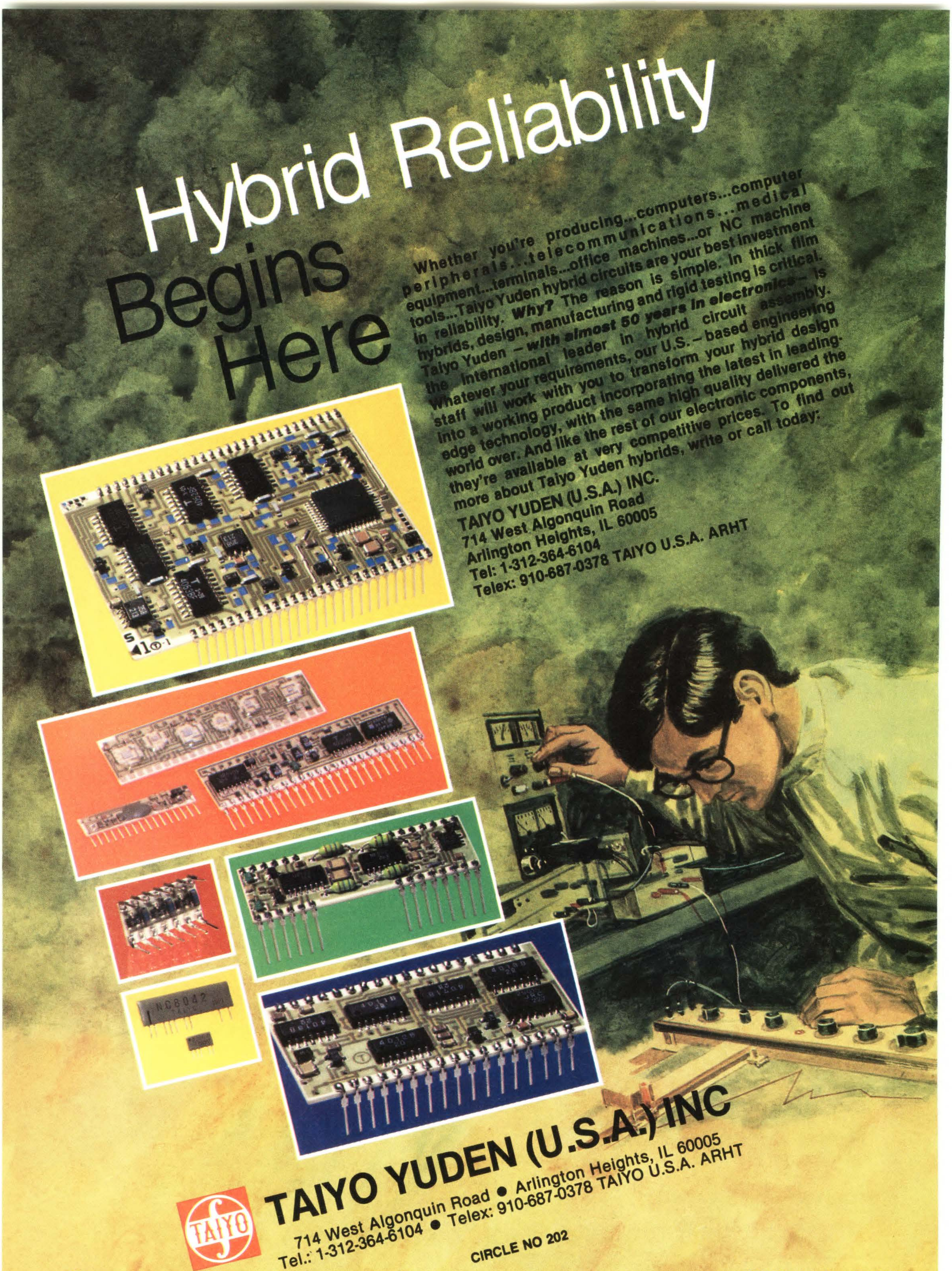
The TLE4910K Hall-effect IC produces an output voltage that is proportional to the flux density of its surrounding magnetic field, allowing you to convert mechanical motion directly into an analog electrical signal. External resistors allow you to adjust the zero-point of the device's linear output characteristic and the device's sensitivity. By adjusting the zero-point you can use the device to detect flux reversal of the magnetic field. The device can withstand ambient temperatures of −40 to +135°C, and includes a temperature sensor that you can use to temperature compensate measurement circuitry. The TLE4910K has an operating supply voltage range of 4.75 to 18V. Around $2.30 (1000).

Siemens AG, Zentralstelle fur Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 393

Siemens Components Inc, 2191 Laurelwood Road, Santa Clara, CA 95054. Phone (408) 980-4500.

Circle No 394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CIRCLE NO 202

Who's got the button?

Nobody, but nobody, offers or delivers more rechargeable button cells and batteries than Varta.

The first in NiCd batteries.

This year, 1988, Varta celebrates its 100th year in manufacturing batteries of all types. In the '50's we led the world in commercialization of NiCd batteries.

100 years 1888 1988 VARTA

We invented the mass-plate cell construction which excels over sintered nickel-cadmium cells.

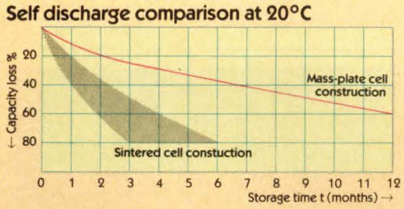
Unique performance advantages.

In stand-by at ambient temperatures, our mass-plate button cells retain 60% capacity after 12 months versus about three months for sintered NiCd cells, because they have much lower internal losses. Similarly, they require much lower recharging rates, as low as 1mA (C/100) versus 4-7mA for competition, so charging power and circuitry will be minimized.

More compact designs.

Varta mass-plate button cells and batteries usually take much less space — or let you put up to 40% more capacity in the same space.

Self discharge comparison at 20°C



Better shelf life.

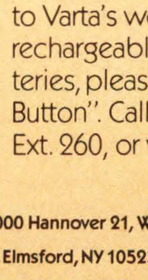
Cells can be stored in any state of charge for over five years without significant loss of performance.

Cost benefits, too.

With all their advantages, Varta mass-plate button cells and batteries usually cost less than comparable sintered-type cells.

Many sizes and types.

Capacities range from 4 mAh to 1000 mAh. Many flat or stacked batteries can be assembled. Extra high temperature ratings and UL listings are available in key sizes. For rechargeable applications above 1000 mAh, Varta also offers a complete line of NiCd cells and batteries.

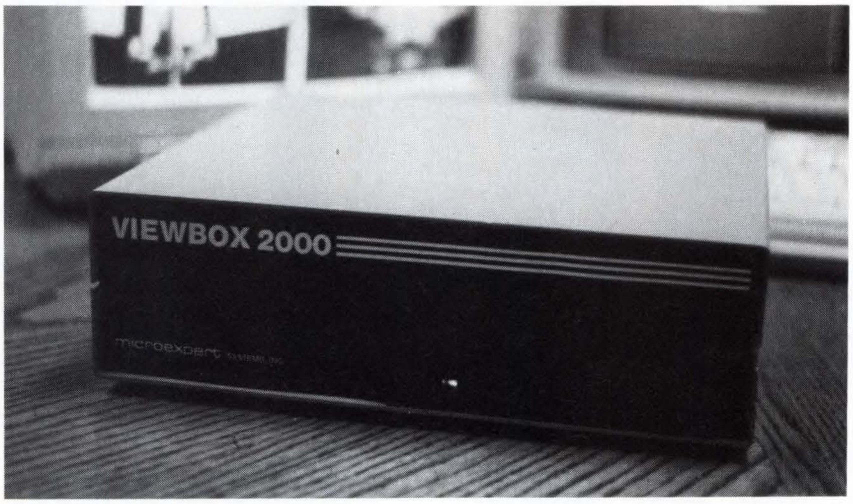


For an introduction to Varta's world-leading line of rechargeable button cells and batteries, please ask for "Who's Got The Button". Call 1-800-431-2504, Ext. 260, or write below.

VARTA

VARTA Batterie AG, Am Leineufer 51, D-3000 Hannover 21, West Germany, Tel. (49) 0511/79031
VARTA Batteries, Inc., 300 Executive Blvd., Elmsford, NY 10523, USA, Tel. 1-800-431-2504, Ext. 260
VARTA Batteries Pte Ltd., 1646 Bedok North P.O. Box 55, Singapore 9146, Tel. (65) 241-2633

CIRCLE NO 203



VIDEO STORAGE

- *Can capture 2460 monochrome images*
- *Records and accesses images in 200 msec (max)*

The View Box 2000 is a system for storing video signals from a TV camera, a computer, or a video source. It can capture 2460 still monochrome images with a resolution of 240×400 pixels under computer control. It connects to a host via an RS-232C port. The computer commands the unit to store, erase, or display a selected video picture. The software, which runs under MS-DOS, stores the picture files in the unit and associated descriptors in the computer's disk file. An 11×12×3.75-in. box contains an erasable Winchester disk drive, the digital and video control circuits, and a power supply. Inputs include a camera connector, a BNC connector, and a loop-through connector. Outputs include a monitor connector, a BNC connector, an RS-170 connector, and a loop-through connector. The system can record and randomly access images in 200 msec max. $2995.

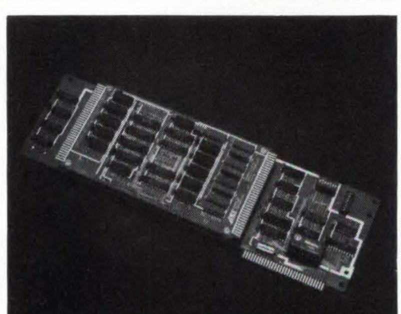
Microexpert Systems Inc, 24007 Ventura Blvd, Suite 210, Calabasas, CA 91302. Phone (818) 712-9934.

Circle No 400

NTDS CARD

- *Emulates AN/UYK-7, -20, -43, -44, and AN/AYK-14 computers*
- *The IBM PC card implements NTDS MIL-STD-1397 protocols*

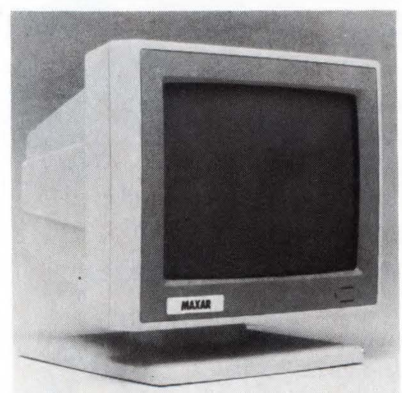
The Micronaut NTDS interface card for the IBM PC computer emulates costly Navy Tactical Data System (NTDS) computers. It is meant to replace tactical peripherals with a commercial alternative, record and analyze data from military devices, develop software for NTDS computers, and simulate consoles and displays. The card can emulate the



AN/UYK-7, -20, -43, -44, and AN/AYK-14 tactical computers. The card lets the PC communicate with military computers and peripherals that implement the NTDS MIL-STD-1397 data transfer protocols. The card performs all I/O functions, including input data, output data, external function, external interrupt, forced function, and forced interrupt. The software can be configured for 8-, 16-, 24-, or 32-bit word lengths. The card and driver software, $1995.

American Systems Corp, 14200 Park Meadow Dr, Chantilly, VA. Phone (800) 336-4564; in VA, (703) 968-5080.

Circle No 401



COLOR MONITOR

- *Compatible with MDA, HGC, CGA, EGA, PGC, VGA modes*
- *Has 15- to 35-kHz horizontal autosynchronization*

The Maxar Maxiscan 14-in. color monitor is compatible with MDA, HGC, CGA, EGA, PGC, MCGA, and VGA graphics standards. It runs with the IBM PC, PC/XT, PC/AT, and PS/2; Apple's Macintosh II; AT&T's 6300; and Olivetti's M24 and M28 computers. The monitor provides autosynchronous operation for horizontal frequencies from 15 to 35 kHz and vertical frequencies from 50 to 100 kHz. It provides a maximum resolution of 820×620 pixels, and the text is

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BusinessWeek

... "Their chip is the most flexible we've seen"
Microprocessor Report

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CIRCLE NO 70

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Call toll-free, 800-443-7364 ext. 23

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Three Dual Flip-Flops	Two Synch 4-Bit Binary Up-Down Counters	One Octal Transparent Latch 3-State
Two 3- to 8- Line Decoder Demultiplexers*	Two Octal Buffer Line Driver 3-State*	One Octal D-Type Flip-Flop 3-State*
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*Standard Military Drawings available

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available in green, amber, cyan, and white-on-blue. It has an infinite color palette in analog mode and 8, 16, or 64 colors in TTL digital mode. The video bandwidth is 35 MHz. $679.

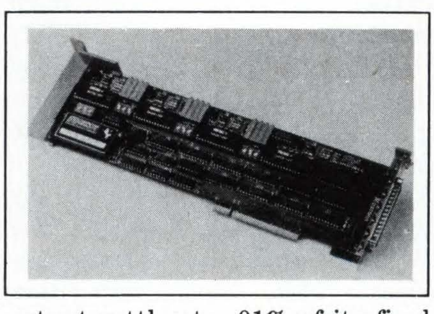
Hyosung Computer, 710 Lakeway, Suite 285, Sunnyvale, CA 94086. Phone (408) 733-0810. FAX 408-733-2638. TWX 510-101-2707.

Circle No 402

ANALOG OUTPUT

- *Has four 12-bit D/A channels*
- *Provides 24 parallel digital I/O lines*

The μCDDA04 is an analog-output board for the IBM PS/2 computer, Models 50, 60, and 80. It provides four independent 12-bit D/A channels based on four Burr-Brown DAC-811KP converters. Each output is configurable for voltage ranges of 0 to 10V, ±5V, ±10V, and as a 4- to 20-mA current loop. The



output settles to .01% of its final value in 4 μsec max for a step input. In addition, the board provides 24 parallel I/O lines via an 8255 programmable peripheral-interface IC. The parallel I/O lines are arranged as two 8-bit ports and two 4-bit ports. The only adjustment devices are trim pots for zero- and full-span calibration and switches for range selection. The PS/2 setup and installation program sets the base address. $699.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989.

Circle No 403

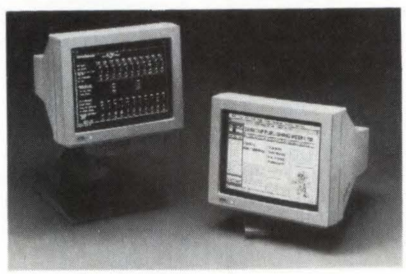
BITBUS INTERFACE

- *Brings industrial control to DEC's VAX computers*
- *Lets multiple processes control multiple slaves*

The BBMaster is an industrial-control network interface for DEC's MicroVAX and IVAX computer families. The system consists of a Q bus board and software that permit multiple VMS processes running on a host to control multiple slaves on a BitBus network. Each network has a master node and as many as 28 distributed slaves. Repeater taps can be added to expand the network to 250 slaves. An Intel 8044 microcontroller located on the dual-height board controls the remote slaves. The hardware can handle multistream DMA data transfers and four levels of interrupts on the Q bus. The software consists of three layers. The first layer is firmware resident on the board for network control and VMS message handling. The second layer is a VMS device driver, which lets multiple processes have concurrent access to the network. The third layer is a library of high-level-language subroutines. $1995.

Lantek, 2131 University Ave, Berkeley, CA 94704. Phone (415) 549-0454.

Circle No 404



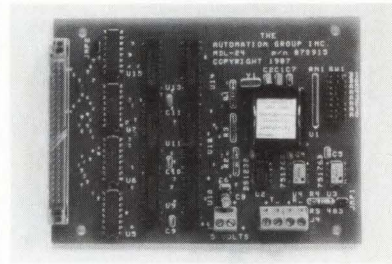
MONITORS

- *Are compatible with IBM PS/2 and PC computers*
- *Display 640×480 pixels on non-glare screens*

The WY-550 and WY-650 monitors come with a video-graphics-array (VGA) adapter that makes them compatible with IBM PC, PC/XT, PC/AT, and PS/2 systems. They display 640×480 pixels on non-glare, high-contrast screens. The monitors scan horizontally with a 31.5-kHz frequency and vertically with a 50- to 70-Hz frequency. The WY-550 monochrome monitor provides a 14-in. display with either paper-white or amber phosphor. The WY-650 12-in. color monitor can display up to 256 colors simultaneously. This model also lets you switch to a monochrome mode for better character resolution. The VGA adapter offers zoom magnification as a custom feature for CAD applications. The adapter's other custom features include full-screen panning, split-screen windowing, and a soft font capability. WY-550, $249; WY-650, $629.

Wyse Technology, 3571 N First St, San Jose, CA 95134. Phone (408) 433-1000. TLX 3719730.

Circle No 405



I/O BOARD

- *Has 24 digital inputs or outputs and one RS-422 port*
- *Can control 8-, 16-, and 24-position solid-state relays*

The MDL-24 digital I/O board has 24 programmable digital lines that can be arranged as inputs or outputs. The board can be used to control 8-, 16-, and 24-position solid-state relays as a 24-channel, 16-bit counter, or simply as a digital controller. A 50-pin connector allows direct interfacing with relay racks from Gordos-Arkansas, Opto 22, and Grayhill. Each digital input has a programmable debounce filter and a 16-bit counter. The digital inputs can monitor and count frequencies from 0 to 1 kHz. Each digital output can be latched, pulsed, or set to oscillate. Each of the open collector digital outputs can sink 500 mA. Communication is through an RS-422 port at 1200, 2400, 4800, or 9600 baud. The board can be located as far as 5000 ft from a computer. $199 (each); $139 (100).

The Automation Group Inc, 848-R Nandino Blvd, Lexington, KY 40511. Phone (606) 254-6916. FAX 606-253-1762.

Circle No 406

TAPE BACKUP

- *Has a 2G-byte capacity in a 5¼-in. form factor*
- *Can transfer data at 1.9M-bps sustained*

The Jobe tape backup system provides 2G bytes of formatted data storage in a 5¼-in. form-factor-compatible package. The system utilizes helical-scan video recording and error correction circuitry to

STANDARD GRIGSBY SWITCHES

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Standard Grigsby, Inc. rises high above the rest with its offering of one of the widest ranges of 1/2″ switch components in the industry. These 1/2″ products are wave solderable, washable, available sealed or unsealed and in commercial or military finishes.

Standard Grigsby, Inc.'s 1/2″ switch products are offered not only in various PC board configurations but also differing indexing angles. Also offered are anti-static keylocks with various levels of security. In addition are concentric shaft switches with numerous versions available.

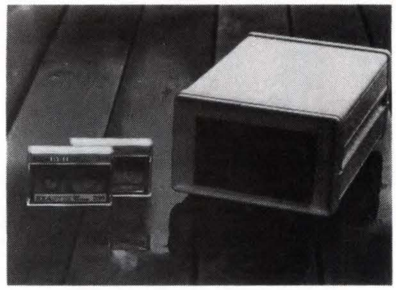
Standard Grigsby, Inc.'s Application Engineering department is available to solve your switching problems.

STANDARD GRIGSBY

920 Rathbone Avenue
Aurora, IL 60507-9990 USA
312/844-4300
TWX 910-232-3138 • FAX 312-844-4286

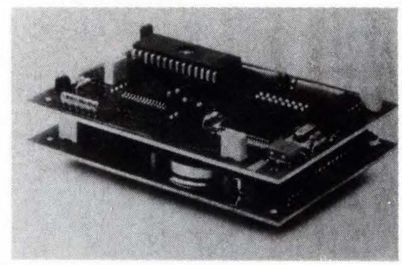
CIRCLE NO 229

correct for a burst of errors as long as 264 bytes. Since the drive can transfer data at a sustained rate of 1.9M bps, it fills a 300M-byte disk file in 20 minutes. A 256-byte buffer can handle burst transfers at 12M bps. The drive comes in a stand-alone box with a power supply and cables. It also comes with software drivers for Unix V.3 systems; SUN-4 version 3.4 systems; and IBM PC, XT, or AT systems. The PC software runs under Novell's LAN. $5990.



Jobe Computers, 8921 Murray Ave, Gilroy, CA 95020. Phone (408) 847-0446. FAX 408-847-1086.

Circle No 407



DATA LOGGER

- *Is suitable for portable or remote logging equipment*
- *Has 128k bytes of nonvolatile memory*

Piggybacked onto the company's TDS9090 control computer board, the TDS9095 multifunction card provides you with a 100×72×30-mm (3.9×2.8×1.2-in.) data-logging module suitable for use in portable or remote-location monitoring equipment. The module has 128k bytes of RAM and a real-time clock that are kept active by a lithium battery. Other features include a 10-channel, 10-bit A/D converter; a keyboard encoder; and a package of software support routines. You can program the module to power itself up at predetermined intervals, log data, and then automatically power itself down. Activated for a period of 1 sec every 10 minutes, the module will run for over a year from a 9V PP3 alkaline battery. The module's processor is programmed using the Forth programming language, and it interfaces to alphanumeric or dot-matrix LCDs. £289.90 (10).

Triangle Digital Services Ltd, 100a Wood St, Walthamstow, London E17 3HX, UK. Phone 01-520-0442. TLX 262284 (quote ref MO775).

Circle No 408

THE ONLY THING MISSING FROM THIS 680-PAGE LEADED RESISTOR/CAPACITOR DATA BOOK IS *YOU.*

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2001 W. Blue Heron Blvd., P.O. Box 10330, Riviera Beach, FL 33404

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New 680-page 1988-89 Leaded Resistor/Capacitor Data Book contains valuable performance and specifying data on the complete, broad line of Mepco/Centralab leaded passive components:

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CIRCLE NO 230

IN VANCOUVER, WASHINGTON, WE'VE JUST ISSUED PERMITS TO BREAK SPEED LIMITS.

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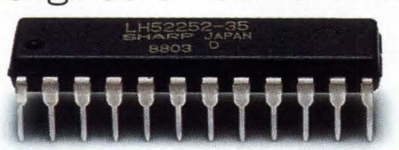

Sharp's new LH52252 64k x 4 SRAM

That's exactly what we've done at our new Sharp Microelectronics Technology Center in Vancouver, Washington. There we've provided our outstanding staff with the most advanced CAD systems available. And we've backed them with a world-class 1.2 micron production facility in Japan, along with a national network of salespeople and distributors.

The purpose of all this? To aggressively carve a niche for ourselves by creating a select line of high-speed chips. Like the new **Sharp LH52252, our 64k x 4 SRAM that operates at 35 ns cycle time and consumes just 100 microamps in standby mode.** It's the first of many high performance products you can expect from our new design center. And it's available right now at Marshall, Milgray, Western Microtechnology, Space Electronics, and Added Value.

If you have specific questions, we invite you to call Sharp at (201) 529-8757. Especially if moving at 35 ns or faster sounds appealing. Because if you like breaking speed limits, Sharp has just the ticket.

SHARP'S NEW HIGH-SPEED CMOS SRAMs			
DEVICE#	ORGANIZATION	ACCESS TIME	AVAILABILITY
LH52252	64k x 4	35 ns/45 ns/55 ns	Immediate
LH52259	32k x 9	35 ns/45 ns/55 ns	3Q 1988
LH52251	256k x 1	35 ns/45 ns/55 ns	3Q 1988
LH52256	32k x 8	70 ns/90 ns/120 ns	Immediate
LH5261	64k x 1	25 ns/35 ns	1Q 1989
LH5262	16k x 4	25 ns/35 ns	4Q 1988

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CIRCLE NO 231

IEEE CONTROLLER

- *Controls test instruments independent of a host*
- *Has 32k bytes of memory for data or program storage*

The Macro488 stand-alone controller for instruments on an IEEE 488 bus contains 32k bytes of nonvolatile memory for storing data or programs. You can load a series of instruction sets, or macros, into its memory from any computer having an RS-232C or RS-422 port. It can store as many as 100 different macros in the nonvolatile memory, and it can control 14 separate instruments on the IEEE-488 bus. The unit has a built-in real-time clock, which lets you collect data at a precise time or at regular intervals. It can automatically assign a time-tag for collected data, thus eliminating the need for constant supervision. Since the unit doesn't occupy computer resources during tests, a computer can be performing other tasks and can retrieve the data at some later time. $995.

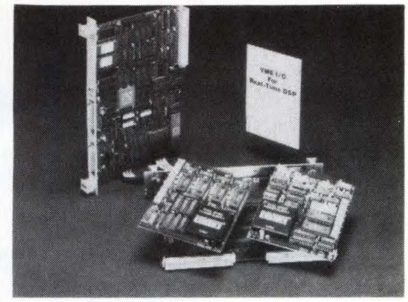
IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. TWX 650-282-0864.

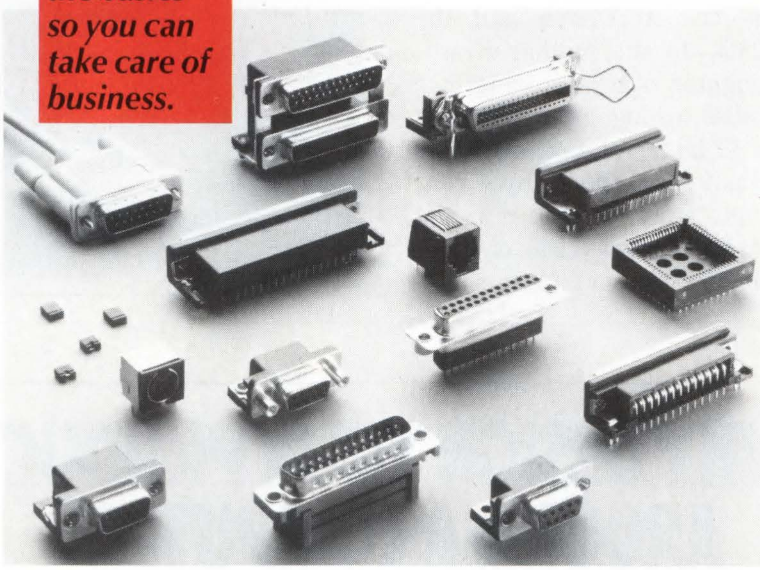
Circle No 409

MOTHER BOARD

- *Features two high-speed parallel ports*
- *Provides single-channel, 100-kHz throughput*

The MPV121 mother board, when combined with the company's SPV120 board, lets you do DSP applications in real time. This VME Bus board features two high-speed I/O parallel ports under DMA control. You can connect two daughter boards—the ACX122A and the ACX123B—to the mother board. The daughter boards provide four differential analog input channels with a 12-bit resolution—100-kHz throughput per channel. Input voltage ranges from 0 to 10, ±5, and ±10V with gain selections of 1, 10, and 100. The boards feature simul-

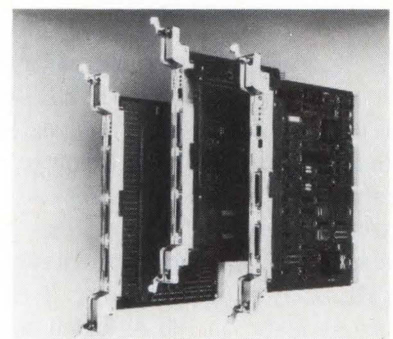




taneous sampling, as well as a programmable sampling rate. In addition, they provide automatic or CPU gain-controlled analog inputs. Single-wide MPV121, $2985; double-wide MPV121/SP120 combination, $5680.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 410



CONTROLLERS

- *Control four drives*
- *3M-byte/sec data-transfer rate*

The QD34 and QD24 disk controllers and the QT14 tape controller come with MicroVAX 3500/3600-compatible handles. The disk-drive controllers emulate the Mass Storage Control Protocol (MSCP) to provide a software-transparent interface to the host computer. All three employ proprietary VLSI logic to optimize performance. The QD34 features a 3M-byte/sec data-transfer rate. The QD34 and QD24 control four 5¼-in. disk drives using SMD and ESDI standards, respectively. The QT14 tape controller interfaces a Pertec streaming or start/stop tape drive to the host computer. The QT14 accepts NRZI, PE, and GCR tape formats and features 1M-byte/sec data-transfer rates and a 64k-byte data buffer. QD34, $2495; QD24, $1795; QT14, $1395.

Emulex Corp, Box 6725, Costa Mesa, CA 92626. Phone (800) 368-5393; in CA, (714) 662-5600.

Circle No 411

TEST & MEASUREMENT INSTRUMENTS

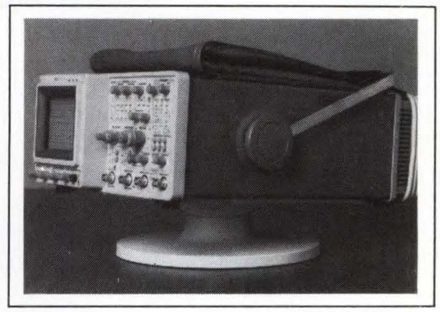
DIGITAL L-C-R METER

- *Identifies inductors, capacitors, and resistors*
- *Tests at three frequencies with 0.1% max error*

The 4210S digital L-C-R meter automatically identifies whether a component is an inductor (L), a capacitor (C), or a resistor (R). It then measures the component's value and the values of its secondary parameters (for example, a capacitor's dielectric losses and series inductance and resistance). The unit can measure at three frequencies—120 Hz and 1 and 10 kHz—with a basic accuracy of 99.9%. A 5-digit LED display indicates the results. The meter can sort components into ten bins by absolute value or percentage deviation from a specified value. Using a single keystroke, you can command the unit to correct for lead resistance and open-circuit impedance. Both test-setup and calibration data remain in nonvolatile RAM, even when you remove power. IEEE-488 and component-handler interfaces facilitate using the instrument in automatic test setups. $3390.

Wayne Kerr Inc, 600 W Cummings Pk, Woburn, MA 01801. Phone (617) 938-8390. TLX 6817257.

Circle No 425

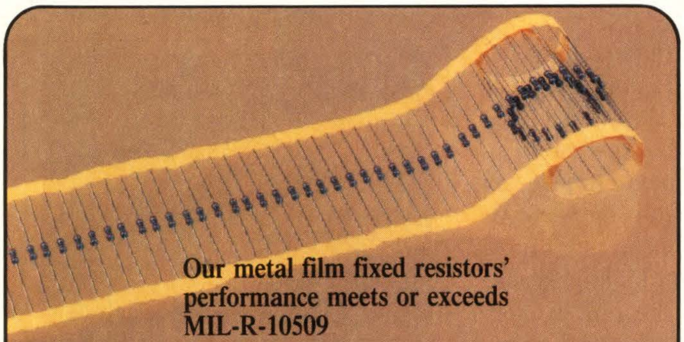


SCOPE ACCESSORIES

- *Include tilting, swiveling scope base*
- *Allow roll-about access to rack-mount instruments*

The K501 is a tilting, swiveling, bench-mounting pedestal for laboratory oscilloscopes. The K217S is a roll-about cart that accommodates equipment designed for mounting in standard 19-in.-wide RETMA racks. The cart features lockable

When quality counts, count on Allen-Bradley



Our metal film fixed resistors' performance meets or exceeds MIL-R-10509

Nichrome resistance element provides stable performance. TCR is less than 100 ppm/°C over the full range of values . . . $10\,\Omega$ to $1\,M\Omega$. Standard tape and reel or bulk packaging. Experience Allen-Bradley quality at a very reasonable price. Call 800-592-4888 or 800-292-4888 in Texas.

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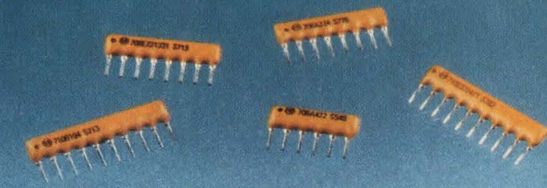
CIRCLE NO 5



Conformal coated cermet resistor networks. . .6, 8, 9, 10 pins

Our C-SIP networks provide world class performance at competitive prices. Space saving low profile, stable thick film elements, 4 through 14 pins available in addition to above standards. High quality, low cost. Call 800-592-4888 or 800-292-4888 in Texas.

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Surface mount SARAs and chip resistors

SARAs . . . resistor networks with solder bumped terminations for surface mount applications. Compatible with automatic placement equipment. Cost effective solution for space-saving custom circuitry. User trimmable.

Chip Resistors . . . 1206 and 0805 sizes. Laser trimmed thick film resistance element. Tight TCR. 5% and 1% tolerance in high volume. Utilizes Statistical Process Control in manufacturing for built-in quality. Call 800-592-4888 or 800-292-4888 in Texas.

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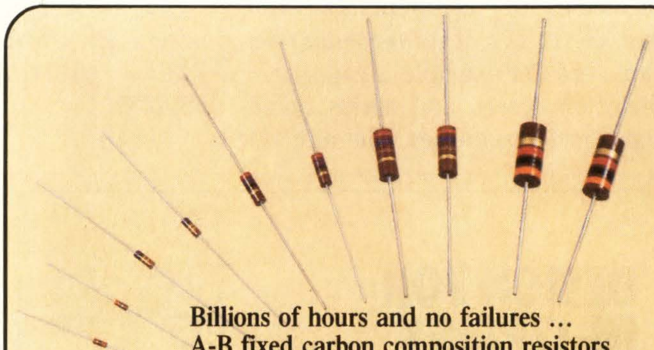
CIRCLE NO 7



Billions of hours and no failures ... A-B fixed carbon composition resistors

We deliver on time. Meet or exceed all applicable military specifications including MIL-R-39008 and qualified to reliability level S. ⅛ Watt through 4 Watt @ 70°C. Call 800-592-4888 or 800-292-4888 in Texas.

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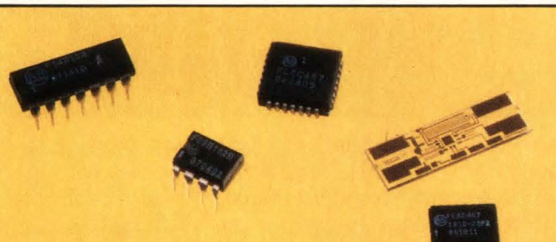
CIRCLE NO 8



Thin film precision resistor networks

Consist of integrated films of chromium cobalt vacuum deposited on specially selected glass or alumina substrates resulting in networks having precision tolerance and stability. Molded and ceramic DIP, ceramic SIP, surface mount, alumina and glass chip, and hybrid network substrates. Standard designs and custom circuits and packages. Meets MIL-R-83401 characteristic. Call 800-592-4888 or 800-292-4888 in Texas.

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A ROCKWELL INTERNATIONAL COMPANY
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Broad line of wire wound resistors – power, precision, aluminum-housed and low ohm

Choose Type WW to meet your power requirements (½W-14W) in a small package. Choose Type W8 for your precision requirements. Our Type WA will meet your high power (5W-50W) needs, and our Type WL provides the very low ohmic values you require. All of our wirewounds are competitively priced and backed by Allen-Bradley quality. Call 800-592-4888 or 800-292-4999 in Texas.

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CIRCLE NO 10

wheels and three trays, two of which tilt. The K318 is a general-purpose utility cart that can accommodate, for example, a personal computer. The vendor also offers a power strip and a second tray as options on its K212 portable instrument cart. K501, $75 (until Oct 31 1988; $95 thereafter); K217S, $625; K318, $375. K212 with power strip and second tray, $445.

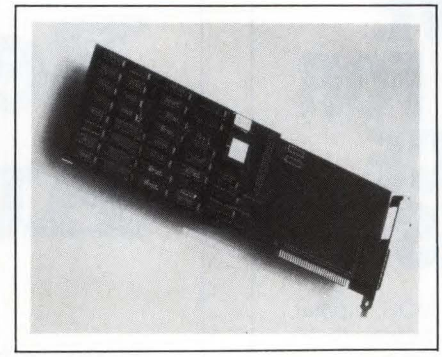
Tektronix Inc, Box 3500, Vancouver, WA 98668. Phone (800) 835-9433, ext 170.

Circle No 426

DSP DEVELOPER

- *Mother board provides a 16k-word memory*
- *Offers dual-channel 16-bit A/D-D/A system*

The Chimera system is a DSP developer for TI's TMS320C25. You can use this hardware/software package on an IBM PC, PC/AT, or



compatible. The system's mother board provides a 16k-word memory for programming and data storage. It lets you design a daughter board for your application. Other options include a dual-channel, 16-bit A/D-D/A system with a 200k sample/sec max rate; a dual 128k-byte buffer configuration; and a wire-wrap board. The vendor's software provides a debugger, a patch processor, an install program, a user-interface program, and an injector program for signal files. Mother boards: with a 128k-byte memory and development software, $2995; with a 32k-byte memory and development software, $2195; with 8k bytes of memory, $1995; daughter boards: with A/D-D/A system, $795; dual 64k-byte buffer, $795; wire-wrap board, $295 (OEM qty).

Atlanta Signal Processors Inc, 770 Spring St, Atlanta, GA 30308. Phone (404) 892-7265.

Circle No 427

18-GHZ MIXER

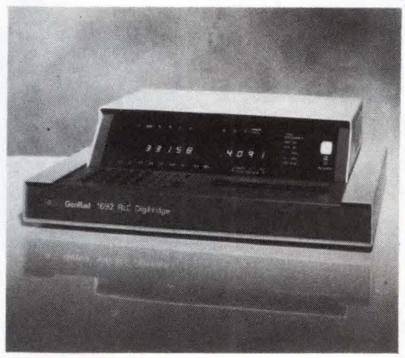
- *Features a group-delay distortion of 2 nsec*
- *Provides video detection of pulse and cw signals*

When combined with the HP 5371A frequency and time-interval analyzer, the HP 5364A microwave mixer/detector performs microwave modulation-domain analysis. Adding a local oscillator to this combination, you can measure spread-spectrum signals, such as agile carriers

and chirped pulses, at frequencies of 18 GHz. The HP 5364A's IF channel provides a 500-MHz bandwidth with a 2-nsec group-delay distortion. A separate video channel lets you trigger the HP 5371A. You can also use the video channel for measuring rise and fall times and pulse widths. HP 5364A, $13,000; HP5371A, $21,500.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 428



DIGITAL BRIDGES

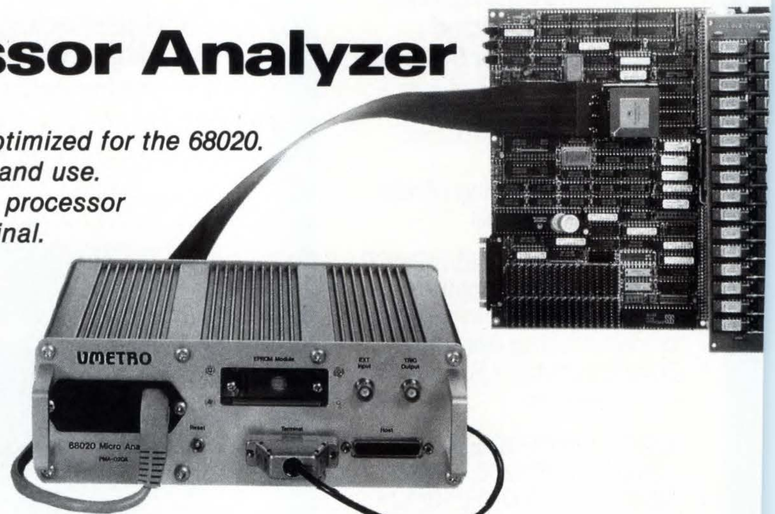
- *Measure passive-component parameters*
- *Test at frequencies from 12 Hz to 200 kHz*

The models 1659, 1692, and 1693 RLC (resistance, inductance, capacitance) testers automatically determine the type of component under test and automatically select the optimal measurement range. The 1659, which is designed for use in laboratories as well as in production and incoming inspection, measures R, L, and C with 0.1% error. It measures D (dissipation factor) and Q (quality factor) with 0.0005% error. Fixturing for radial- and axial-lead components is built in. An interface to the IEEE-488 bus and to component handlers is optional. The 1692 provides accuracy approximately twice that of the 1659. It allows you to select among five test frequencies from 100 Hz to 100 kHz and three test speeds, the fastest of

Real time Logic State and Performance analysis for the 68020 microprocessor

PMA-020

The Personal 68020 Microprocessor Analyzer



- *Logic State Analyzer with increased functionality optimized for the 68020. Preconfigured for the 68020 for ease of installation and use.*
- *Extremely compact, selfcontained unit with its own processor and firmware, operated from a standard ASCII terminal.*
- *Two serial ports and a transparent mode eliminates need for a separate terminal.*
- *Ideal for development of low level software, operating systems, data communication etc.*
- *Several PMAs linked together provides time correlated analysis between CPUs in multiprocessors.*
- *Provides remote diagnostics of 68020 systems via modem.*

Logic State analysis

- 2 K Trace of 88 processor signals plus one user defined input.
- Trace data presented in a decoded, human readable form, including coprocessor and MMU commands.
- Disassembler for 68020 program code.
- Powerful triggers and store qualifiers, Trig Output signal.
- Powerful search in trace memory.

```
                    68020 PROGRAM TRACE. STORED ALL CYCLES

 LINE !  ADDRESS   DATA              IPL MODE INSTRUCTION
------!-----------------------------------------------------------------
   32 !  FF0003D8  0C8000000001       1  SP   CMPI.L #$1,D0
   33 !  FF0003DE  66000008           1  SP   BNE.W $FF0003E8
   34 !  FF0003E2  ........           1  SP   --- Cache hit ---
   35 !  FF0003E8  ........           1  SP   --- Cache hit ---
   35 !  FF0003EA  60000006           1  SP   BRA.W $FF0003F2
   36 !  FF0003EE  60000002           1  SP   BRA.W $FF0003F2
   37 !  FF0003F2  4CEE2000FFFC       1  SP   MOVEM.L -$4(A6),A5
   39 !  FF0003F8  4E5E               1  SP   UNLK A6
   39 !  FF0003FA  4E75               4  SP   RTS
   42 !  FF0003FC  4E56FFF4           4  SP   LINK A6,#-$C
   47 !  FF00041C  4A80               4  SP   TST.L D0
   47 !  FF00041E  66000006           4  SP   BNE.W $FF000426
   48 !                               4  CPU  IACK on level  4 (Vector 108)
   49 !  FF000426  1E14               4  SP   MOVE.B (A4),D7
   50 !  FF000414  00034EB9           4  SP   ORI.B #$B9,D3
   51 !  FF000418  FF00               4  SP   DC.W

Scroll:‹,›,+,-  Group:1,2  Jump:J  Mode (with/WITHOUT data):M  Print:^P  Quit:Q
Add start mark:A  Remove start mark:R
```

Performance analysis

- Address distribution of eigth user defined ranges.
- Cache Hit Rate Indication, total and distributed over eigth address ranges.
- Interrupt levels distribution.

```
************  V M E T R O  68020  MICRO ANALYZER     ACTIVITY MODE  ***********

Trig position    : START OF TRACE
Store qualifier  : NONE
                                              Total # of samples :  20480
                                              Activity  mode     :  CACHE

INSIDE  ADDRESS WINDOW (00000000,FFFFFFFF)           DATA D31-D00 : XXXXXXXX

Total Cache Hit Rate:  66% ********************************  .   .   .   .

0: 00000000-1FFFFFFF   12% ******   .   .   .   .   .   .   .   .   .
1: 20000000-3FFFFFFF    0%      .   .   .   .   .   .   .   .   .   .
2: 40000000-5FFFFFFF    0%      .   .   .   .   .   .   .   .   .   .
3: 60000000-7FFFFFFF   15% *******  .   .   .   .   .   .   .   .   .
4: 80000000-9FFFFFFF    0%      .   .   .   .   .   .   .   .   .   .
5: A0000000-BFFFFFFF   25% ************ .   .   .   .   .   .   .   .
6: C0000000-DFFFFFFF   14% *******  .   .   .   .   .   .   .   .   .
7: E0000000-FFFFFFFF    0%      .   .   .   .   .   .   .   .   .   .

PMA: ‹Command Line›
```

For more information, please contact:

VMETRO INC.
2500 Wilcrest, Suite 530
Houston, Texas 77042
Telephone (713) 266-6430
Telefax (713) 266-6919

CIRCLE NO 233

VMETRO

Personal Test Instruments

VMETRO A/S
Sognsveien 75
N-0855 Oslo 8, Norway
Tel.: (47-2) 39 46 90
Fax.: (47-2) 18 39 38

which is 8 measurements/sec. The 1692 can average the results of multiple readings. The 1693 can make as many as 50 measurements/sec. It lets you program the test frequency over a range of 12 Hz to 200 kHz. Its accuracy for RLC measurements is five times that of the 1659. $1950 to $5900.

GenRad Inc, 300 Baker Ave, Concord, MA 01742. Phone (617) 369-4400.

Circle No 429

100M-SAMPLE/SEC DSO

- *Samples high-speed transient signals*
- *Provides 30k-word memory*

Providing 100M samples/sec, the VP-5741A programmable digital storage oscilloscope can handle high-speed transient signals in waveform-analysis projects. It offers a 30k-word memory that you can expand to 200k words. A 10-program capability allows for 100-step programs. The programs let you control the sequence of panel operations, calculate waveform parameters, and enable the unit to take automatic measurements. The vendor also offers models with a 45-program maximum capability. The oscilloscope comes with a 7-in. CRT display that provides a digital readout and an autoposition function. $9900. Delivery, stock to six weeks ARO.

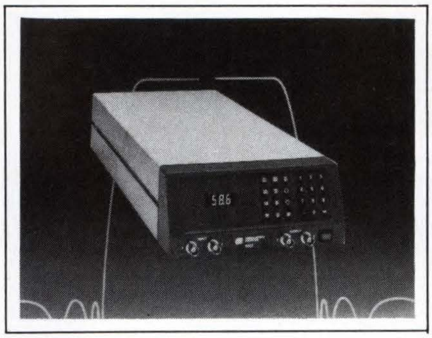
Panasonic Industrial Co, 2 Panasonic Way, Secaucus, NJ 07094. Phone (201) 348-7000.

Circle No 430

PROGRAMMABLE FILTER

- *Covers 0.1 Hz to 102.4 kHz with $3^1/_2$-digit resolution*
- *Stores 6-parameter setups on two channels for five years*

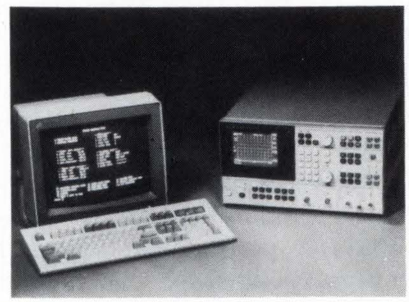
The 9002 programmable filter is a $3^1/_2$-in.-high, half-rack-width unit that covers the 0.1-Hz to 102.4 kHz range. You can program it via an IEEE-488 port or from the front panel. Its battery-backed RAM al-



lows 5-year storage of eight complete 6-parameter setups on each of the two channels. You specify the unit to contain two filters with any combination of the following characteristics: 8-pole Butterworth lowpass or highpass, 8-pole/6-zero elliptic lowpass or highpass, 8-pole Bessel lowpass, or 8-pole/6-zero constant-delay lowpass. The last-named characteristic rolls off more steeply than the Bessel's, yet maintains a flatter passband response and provides 80 dB of stopband attenuation. $2495. Delivery, six to nine weeks ARO.

Frequency Devices Inc, 25 Locust St, Haverhill, MA 01830. Phone (508) 374-0761. TWX 710-347-0314.

Circle No 431



STABILITY ANALYZER

- *Generates frequency-response plots of circuits*
- *System software lets you optimize design*

Incorporating HP's 3562A dynamic signal analyzer, the Model 350 uses a menu-driven operation that lets you generate frequency-response plots of circuits. The test data it acquires lets you optimize your design. The system software allows you to evaluate, combine, model, and verify data. The system works on an IBM PC, PC/XT, PC/AT, PS/2, or compatible. The software supports EGA, VGA, and HP's plotter and printer standards. $5995.

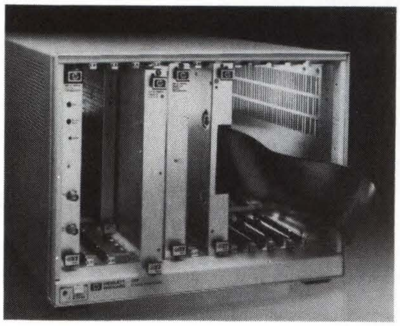
Venable Industries Inc, 3555 Lomita Blvd, Torrance, CA 90505. Phone (213) 539-2522. TLX 752421.

Circle No 432

VXI BUS HARDWARE

- *Includes cage for C-size cards*
- *Interfaces VME Bus to vendor's controllers*

The HP E1400 series includes five hardware products intended for use by developers of card-level instruments based on the VXI Bus (VME



Bus extensions for instrumentation). The HP 98646A is a VME Bus interface for controllers in the vendor's 9000 Series 300 family. The HP E1400A is a powered, 13-slot cage for C-size VXI Bus cards. It mounts in a 12¼-in. space in a standard 19-in. rack. Fan cooling maintains a specified airflow in populated card slots without using filler plates or baffles in empty slots. The HP E1404A is a translator module for slot 0 of a VXI Bus backplane. The HP E1490A is a C-size breadboard module for register-based VXI Bus instruments. The HP E1408A is a carrier for A-or B-size VXI Bus modules inserted in a C-size backplane, and the HP E1409A is a stainless-steel chassis shield for reducing electrostatic coupling between card-level instruments. HP E1400A, \$6600. HP E1404A, \$850. HP E1490A, \$500. HP E1408A, \$170. HP E1409A, \$150. HP 98646A, \$1295.

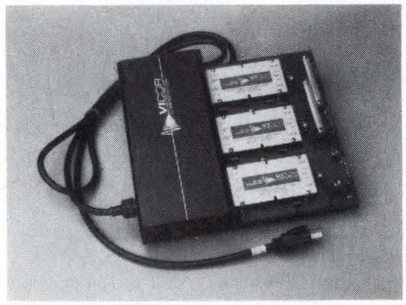
Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local sales office.

Circle No 433

SUPPLY EVALUATOR

- *Has an onboard 750W ac front end*
- *Features input-surge protection and removable line cord*

Designed specifically for the vendor's modules, the VI-MEB-AC lets you evaluate converters in off-line applications. Its 750W ac front-end features include an input-surge protection capability, a removable line cord, a power indicator, and a 110/220V ac selection range. You can plug as many as three converters in the 10.5×12-in. assembly. The evaluator allows you to test single-, dual-, and triple-output applications. The unit comes with module sockets, heavy-duty output lugs, and output measurement jacks. It lets you access gate, trim, and sense connections on each converter. Individually fused module inputs and onboard sockets let you add the vendor's phased-array controllers to the assembly. $695.



Vicor Corp, 23 Frontage Rd, Andover, MA 01810. Phone (508) 470-2900. TWX 910-380-5144.

Circle No 434

DESKTOP CALCULATOR

- *Contains digital clock*
- *Has 12-digit LCD with 10-mm numerals*

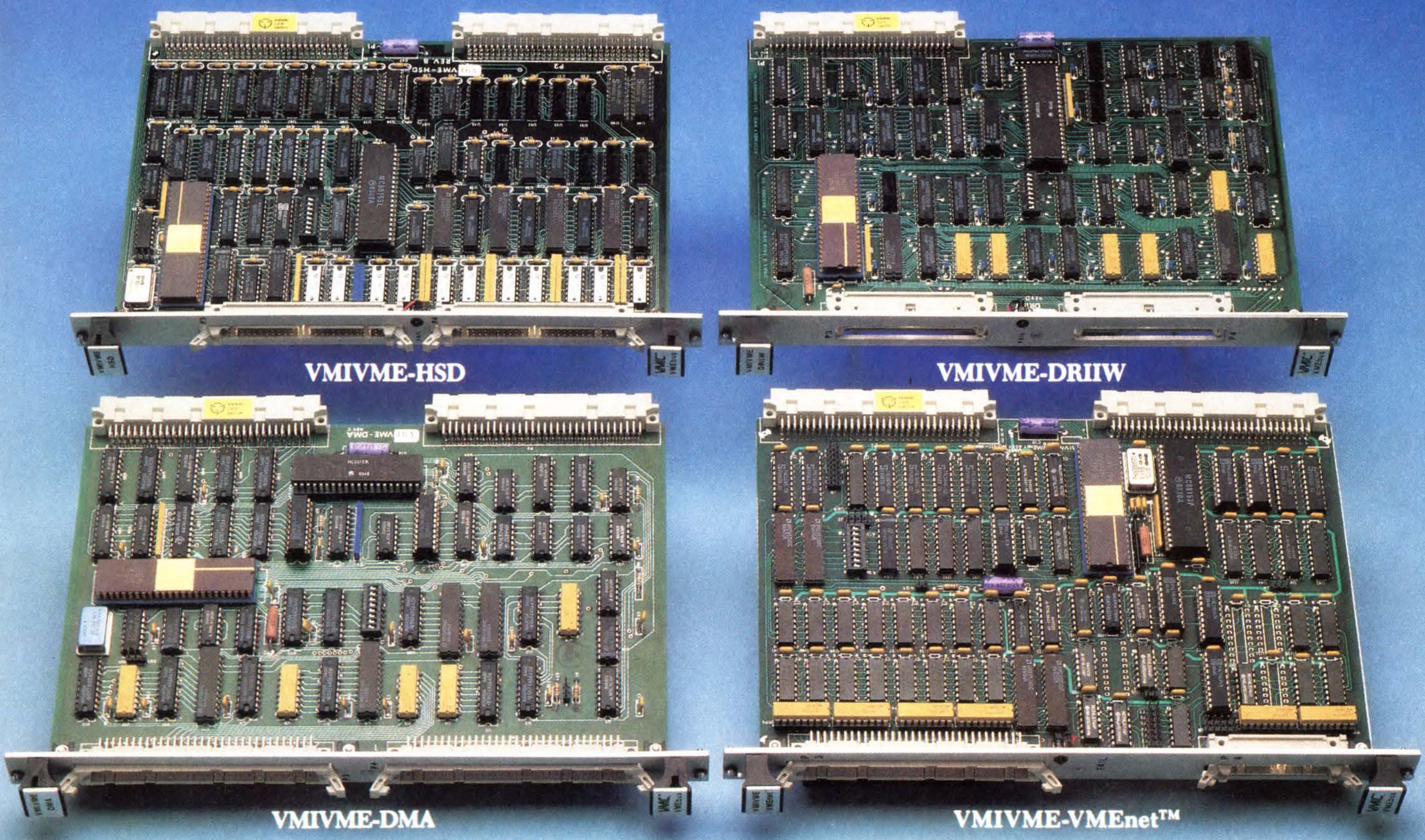
The TI-5021 12-digit desktop calculator includes a digital clock and uses a AA battery. Its keys are larger than those on handheld and credit-card-size calculators. The unit measures 5.7×7.5×1.2 in. and weighs 11 oz. The calculator's features include 4-key memory; a percent key; a margin-up/margin-down key for computing prices; a right-shift key; a plus/minus key; and a numerator-denominator-exchange key. $35, including battery.

Texas Instruments, Box 53, Lubbock, TX 79408. Phone (806) 747-1882.

Circle No 435

CIRCLE NO 89

VME
to DEC, GOULD/SEL...



VMIC manufactures a wide range of parallel DMA interfaces that allow VMEbus connection to a wide range of Host computers.

VMIVME-HSD is a VMEbus HSD compatible interface to GOULD/SEL Concept series HSD products. This 32 bit programmable DMA interface supports GOULD Command Chaining and Data Chaining, and may operate as a HSD Master, or HSD slave; and supports transfer rates up to 3.2 Mbytes/sec.

VMIVME-DRIIW is a VMEbus DRII-W compatible interface to DEC, PRIME, DATA GENERAL, CONCURRENT, SUN Microsystems, Elxsi, Alliant and others. This 16 bit programmable DMA interface supports transfer rates up to 2.25 Mbytes/sec, and is programmable for either master or slave operation; and may be used back to back to form a VME to VME link. The VMIC DR11-W may be used to connect any DR11-W compatible peripheral device such as high speed laser printers, workstations, high resolution graphic terminals or network nodes to the VMEbus. DR11-W links are common with SUN Microsystems.

VMIVME-DMA is a general purpose DMA interface to the VMEbus, and supports 8, 16, and 32 bit transfers, at transfer rates up to 5.0 Mbytes/sec. The board may be used in a back to back configuration to provide a high speed 32 bit DMA link between two VMEbus systems.

VMIVME-VMEnet™ is a high speed parallel multidrop DMA controller. Up to 17 totally independent VMEbus systems may be linked together. This board supports 8, 16, and 32 bit transfers at rates up to 4.76 Mbytes/sec. The board incorporates RS-485 differential line drivers and receivers that support high noise immunity and links up to 2000 feet.

FOR MORE INFORMATION CALL:

VME Microsystems International Corp.
12090 South Memorial Parkway
Huntsville, Alabama 35803
(205) 880-0444
Toll Free 1-800-322-3616/ext. 1007

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CIRCLE NO 204

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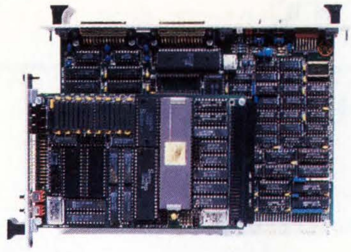
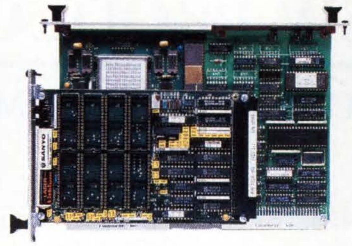
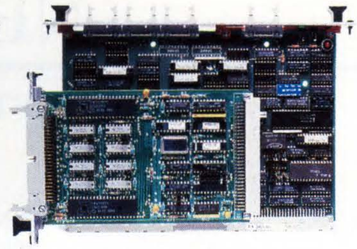


Processor Modules

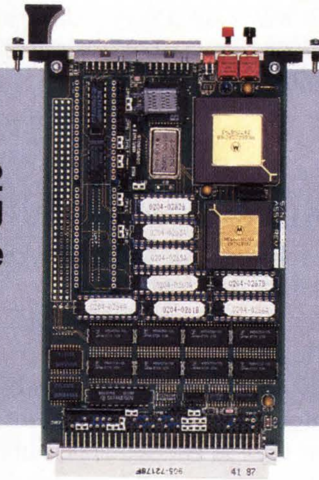


Memory Modules

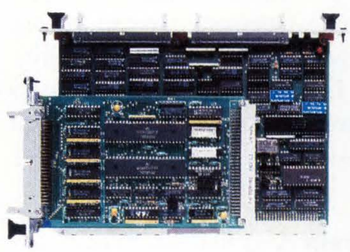


Peripheral Modules

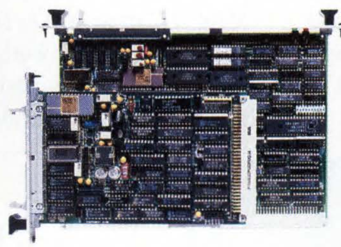
NEW! XVME-602
Low-Cost 3U
68020 CPU Module



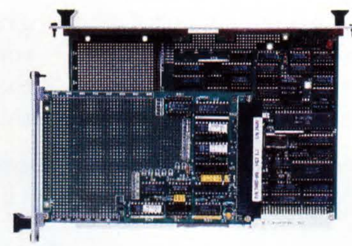
- 16 MHz 68020 CPU
- 68881 math coprocessor site
- 256Kbytes of dual-ported SRAM
- Firmware debug monitor
- User expansion connector



Digital I/O Modules



Analog I/O Modules



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CIRCLE NO 205

VME Products			Software Support
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*Trademarks are acknowledged to: Microware Systems Corp. (OS-9); Eyring Research Institute, Inc. (PDOS); Motorola, Inc. (VERSAdos); V/68K Motorola, Inc. (UNIX); Software Components Corp. (PSOS); SUN Microsystems, Inc. (SUN Workstations); Industrial Programming, Inc. (MTOS).

CAE & SOFTWARE DEVELOPMENT TOOLS

WINDOWING TOOL

- *Complies with Version 11 of the X-Window standard*
- *Runs on Symmetry computers under DYNIX 3.0*

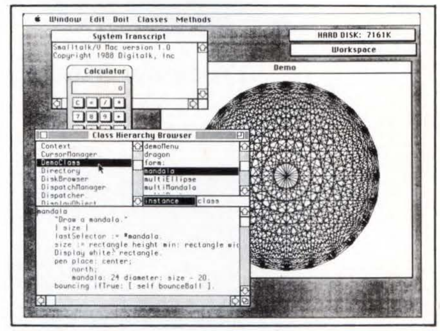
S-Windows is a windowing-management toolset that is fully compliant with version 11 of the X-Windows standard and runs on the vendor's Symmetry series of multiprocessor, multiuser computers under Dynix 3.0 (the vendor's version of Unix). The package includes the standard subroutine library (xlib) and the X toolkit, which provides such functions as menu call-up and scrolling. S-Windows takes full advantage of the parallel architecture of the computers. The package supports all of the standard MIT applications, including a terminal emulator, a window manager, and a bit-map editor. $2495, Symmetry S27 version; $2995, Symmetry S81 version.

Sequent Computer Systems Inc, 15450 SW Koll Pkwy, Beaverton, OR 97006. Phone (800) 854-0428; in OR, (503) 526-4032.

Circle No 415

SMALLTALK FOR MAC

- *Contains all the features of Smalltalk/V-286*
- *Runs on Mac II, Mac SE, and Mac Plus*



Smalltalk/V MAC is an object-oriented software-development language that is particularly suited to the development of AI-related programs. MAC user-interface conventions are closely followed, so that any application developed in this language looks like a standard MAC application program. Smalltalk/V MAC can coexist with any other software resident in the MAC and can also work under MultiFinder; it has complete access to the Mac toolbox. The Smalltalk/V MAC package provides multitasking facilities so that, for example, you can perform program development as a foreground task while tranferring files over communications lines as a background task. You can develop

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very large data structures that are limited only by the amount of available memory. The debugging feature can show all currently executing "methods," highlighting the currently executing source-code statement. This feature allows you to inspect and change all objects, correct source-code errors, and single-step through the application program under test. The documentation includes tutorials, a reference manual for the Smalltalk/V language and development system, and an encyclopedia of classes. You'll need at least 1M bytes of RAM to run this package, and it can use all available memory for your programs. $199.95.

Digitalk Inc, 9841 Airport Blvd, Los Angeles, CA 90045. Phone (800) 922-8255; in CA, (213) 645-1082.

Circle No 416

COMM APPLICATION

- *Lets you store and share Mac files with a VAX*
- *Provides data compression with a 7-bit file protocol*

The VMacS communications application version 2.0 provides a Macintosh connection to VAX. Using the software, you can store and share files with a VAX. You can also use the software with most protocols and emulators. It provides a 7-bit protocol, as well as an 8-bit Xmodem protocol. Using a data-compression algorithm, the software speeds data-transfer rates. It can translate an international character set and control characters in other systems. This feature lets you convert spreadsheets, databases, and word-processing files into text files. The software supports MacWrite 4.5 and Microsoft Word 3.0 file conversions. Upgrade, $25; single-user license, $399; multiuser license, $999.

White Pine Software, Box 1108, Amherst, NH 03031. Phone (603) 886-9050.

Circle No 417

LANGUAGE TRANSLATOR

- *Lets you translate from Pascal to C or vice versa*
- *Can be modified to translate from and to other languages*

QPARSER+ can automatically construct the syntax trees that are needed in order to translate from one programming language to another and provides a technique for the resolution of grammatical conflicts. The program uses an advanced pragma language to generate code within the skeletons for both C and Pascal; however, you can modify the language and customize the skeletons to generate code for other languages. For exam-

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• **a-c to d-c:** Heavy-duty, industrial grade, 50W to 1500W; OEM modules, 3W to 240W; very low profile, very compact modules, 15W to 50W.

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CIRCLE NO 236

ELIMINATING TRANSIENT DAMAGE WITH PAPER!

2.0 kV*

Metallized plastic film capacitors

4.5 kV*

Rifa metallized paper capacitors

In the power supplies or household appliances that you manufacture, RFI capacitors have two primary purposes. (1) eliminating the harmful effects of radio frequency interference, RFI. (2) protecting your equipment against transients from the mains.

In most applications, an RFI cap has to take a lot of punishment.

To define the various kinds of disturbances and irregularities in the voltage wave, UNIPEDE recently carried out an interesting survey. On two separate occasions, measurements were taken in most European countries.

The results may come as a surprise to you.

On average, the transients occur more than ten times a day, and their pulse steepness is acute, approximately 200–2,000 V/µs. Of all categories, 80 percent of the transients have a duration of 1 to 10µs, and an amplitude of up to 1,200 V.

However, transients up to 6,000 V were recorded during thunderstorms.

This is the most realistic picture so far presented of what RFI caps are exposed to, or what they are expected to withstand during the life of your product.

In many cases, the cap you choose is the determining factor for length of life.

Now, there are two primary types of RFI capacitors. (1) metallized plastic film caps. (2) metallized paper caps. Out of five major makes tested at the Rifa labs, the poorest performing samples start breaking down at 2.0 kV.

At the level where even the toughest ones give in, Rifa caps still maintain a safe margin, not starting until 4.5 kV.

QUALITY IN OUR BOOK

In our book, QUALITY means meeting your customer's performance requirements, and he certainly doesn't expect your product to break down or cause interference to radio frequencies, does he?

Rifa capacitors are made to meet the needs of practical applications, not just to come up to a standard.

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CIRCLE NO 237

ple, you can use QPARSER+ to create translator programs for Pascal or dBASE III to C, Basic to Pascal, Bit Map to PostScript, and many other combinations. You can also create programs to convert files from the format of one word processor to the format of a different word processor, or from one CAD format to another. The program runs on IBM PCs and compatibles that have at least 256k bytes of RAM and two disk drives and operate under PC-DOS 2.0 or higher. Another version runs on VAX/VMS machines. PC version, $300 till 12/31/88, then $475; VAX version, $2000.

QCAD Systems Inc, 1164 Hyde Ave, San Jose, CA 95129. Phone (408) 995-5272.

Circle No 418

LEVEL-SENSING SYSTEM

- *Collects product levels for fast-moving containers*
- *Runs on IBM PCs and compatibles*

The model SW-2005 data collection program collects container levels from the vendor's LS-100 level-sensing hardware and saves them in a disk file that you can subsequently analyze with Lotus 1-2-3. The LS-100 determines the level of product in a moving container by echo-sensing methods. To run the software, you'll need an IBM PC or compatible that has at least 512k bytes of RAM, two floppy-disk drives (a hard disk is recommended), the vendor's model IF-100 communications adapter board, the vendor's SW-100 basic communications logic module, and DOS version 3.0 or higher. You can collect the level readings only or the level readings plus the component echoes. $850.

Hyde Park Electronics Inc, 4547 Gateway Circle, Dayton, OH 45440. Phone (513) 435-2121. TWX 910-380-6049. FAX 513-435-6375.

Circle No 419

CADD SOFTWARE

- *Provides preprogrammed drafting standards*
- *Lets you move elements incrementally*

The Anvil-1000MD version 1.3 computer-aided design and drafting (CADD) software runs on the IBM PC/AT and compatibles. The software provides 2½-D elements. A nest function lets you insert elements incrementally; the software also lets you use implicit points, such as the center of a circle or a line bisect. An updated data-entry check allows you to enter numerics and algebraic notation. The software conforms to the ANSI 1973 and 1982, as well as five other drafting standards. The software supports the VGA, PGA, and EGA standards. $2995.

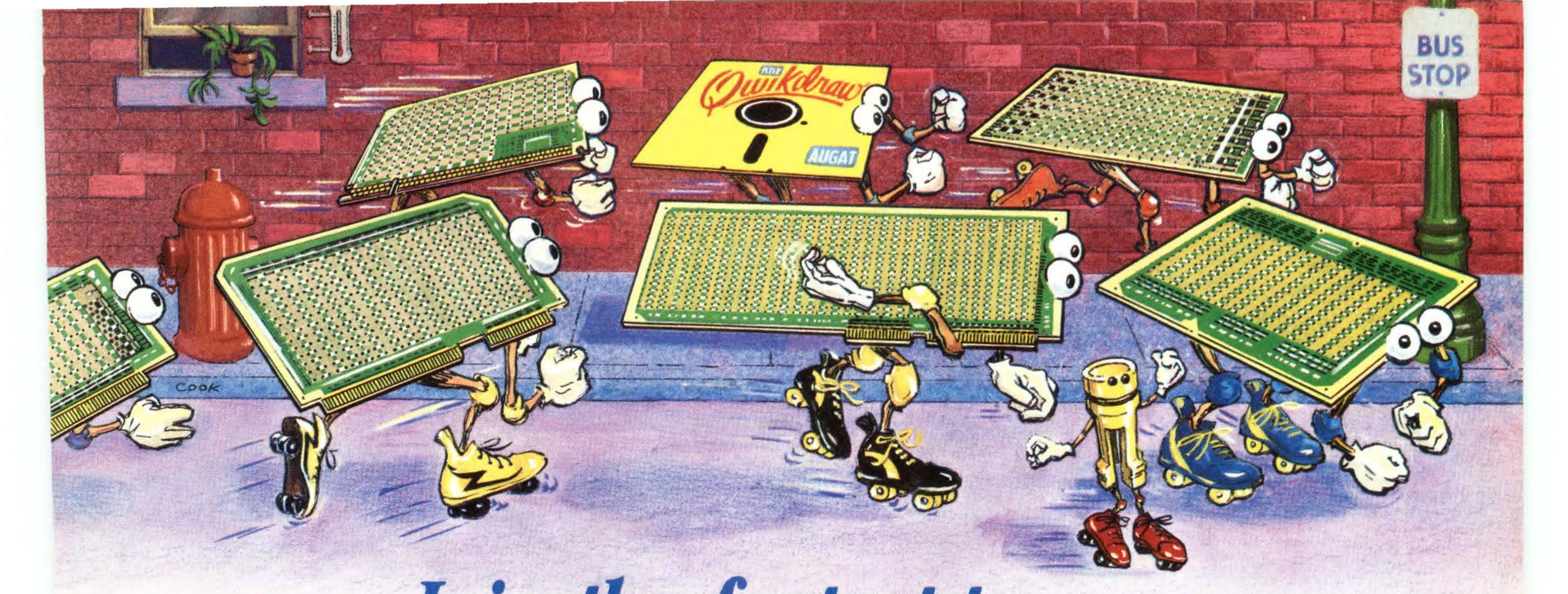
Manufacturing and Consulting Services Inc, 9500 Toledo Way, Irvine, CA 92718. Phone (800) 556-1234, ext 116; in CA, (800) 441-2345, ext 116.

Circle No 420

HELP UTILITY

- *Lets you add on-line help to existing programs*
- *Runs on any IBM PC or compatible*

Helpmate is an easy way to add context-sensitive, on-line help to any existing program that runs on an IBM PC, PC/XT, PC/AT or compatible machine. Installation consists of preparing (with an editor or word processor) an index file that contains keyword definitions and either short help messages or references to a longer help file that you created with the editor and stored on disk. You must also define the Help key that calls up the help utility. When you press the Help key, the memory-resident help program looks for the word at, or closest to, the cursor position. The program then looks up this word in the index file that you prepared and displays the help message or a complete screen of help



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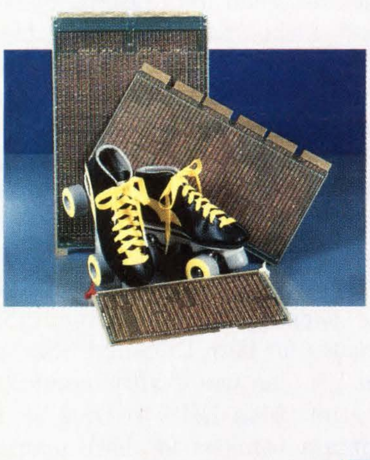

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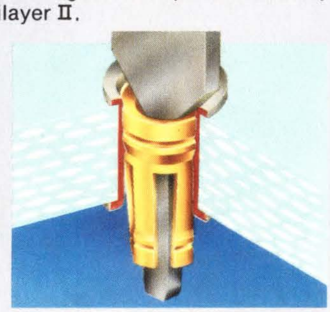
How lean? Tooling charges for Unilayer II are typically 90% less than multilayer. And, since the discrete wires are laminated to pre-built board modules, there's no artwork to be generated. That means minimum up-front charges and rapid-fire delivery with Unilayer II.



Plug In Your Components!

Stuffing your board is a breeze. All Unilayer II boards are provided with zero-profile Holtite contacts, so you can plug your IC's directly into the board, without soldering and without creating a higher profile. Just plug in your components for smooth skating.

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CIRCLE NO 208

text relating to the word at the cursor position. A help screen may itself call up other help files. To run the program, you need a PC or compatible that has at least 128k bytes of RAM. $15.

Pulse Research, Box 696, Shelburne, VT 05482. Phone (802) 985-2928.

Circle No 421

SIMULATOR

- *Simulates transmission lines in pc-board designs*
- *Uses the design's database to analyze signal quality*

The Transmission Line Calculator electromagnetically simulates transmission lines in pc-board, hybrid, and system-level designs. The software works on IBM PCs with math coprocessors, as well as Sun and Apollo workstations. Because the software uses the design's database to check signal quality, you don't have to generate test vectors or input patterns. When combined with the vendor's Motive analysis tool, the software provides worst-case analysis. It lets you check for path delays and clock skew in digitally synchronous designs. From $3550.

Quad Design Technology, 321 N Aviador Blvd, Suite 111, Camarillo, CA 93010. Phone (805) 987-6221.

Circle No 422

GRAPHICS LIBRARY

- *Includes more than 600 C graphics functions*
- *Provides both C and Fortran programmer interfaces*

GFX-4000 is a high-performance set of graphics tools that are based on the proposed PHIGS (Programmer's Hierarchical Interactive Graphics System) standard. PHIGS was designed for large time-sharing systems; GFX-4000 contains extensions and enhancements that improve the performance, capabilities, and usability of the tools on workstations. The toolset is written in C for the sake of portability, contains more than 600 C graphics functions, and provides interfaces to both C and Fortran programs. It runs on VAX machines under the VMS operating system and is tightly integrated with DEC's VWS window-management system; future releases will also support the DEC Windows manager, which is based on X-Windows. A version for Sun workstations will be available late in 1988. Prices start at $3500 for a single VAX CPU license (run-time version, $1250).

Precision Visuals, 6260 Lookout Rd, Boulder, CO 80301. Phone (303) 530-9000. TLX 296428.

Circle No 423

VERSION CONTROL

- *Automates program regeneration after module modification*
- *Operates with both OS/2 and DOS*

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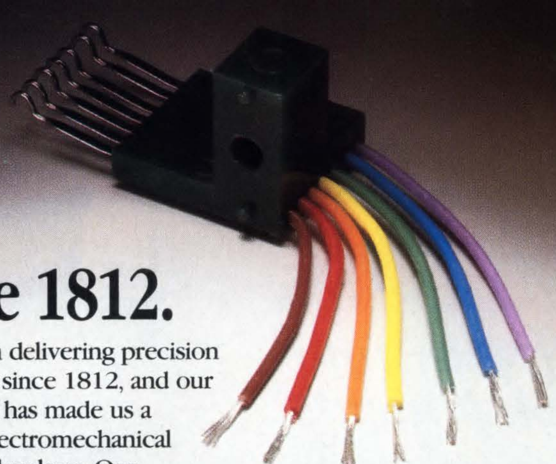

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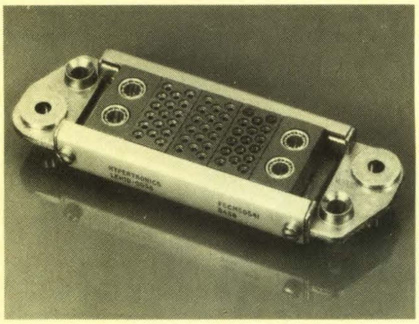

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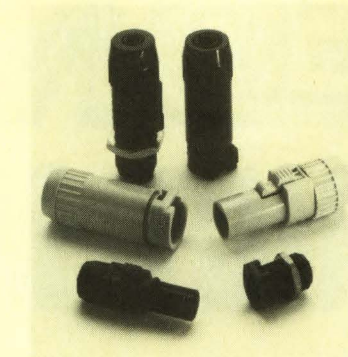

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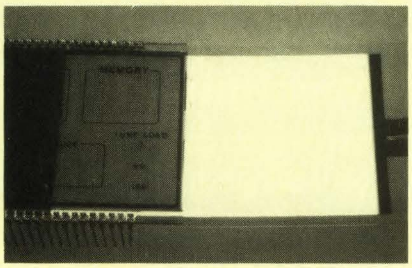

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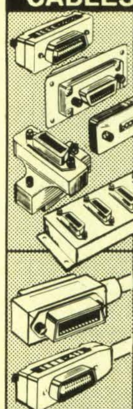

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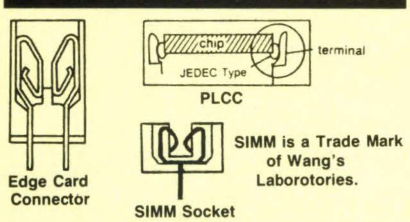

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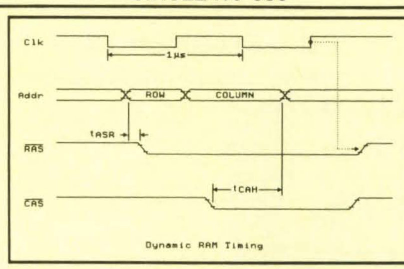

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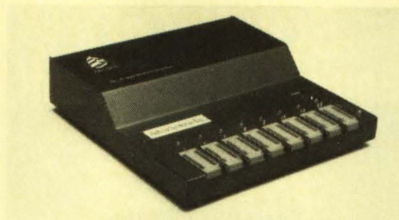

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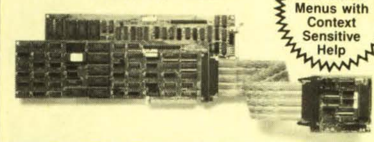

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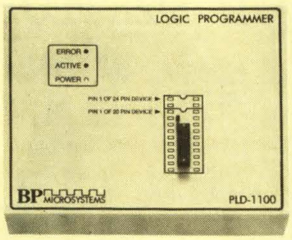

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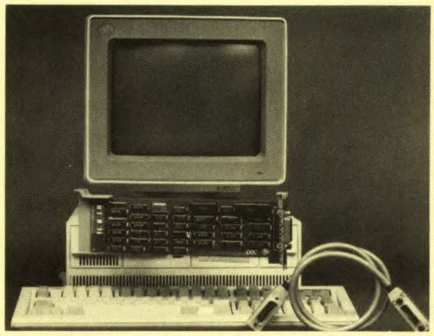

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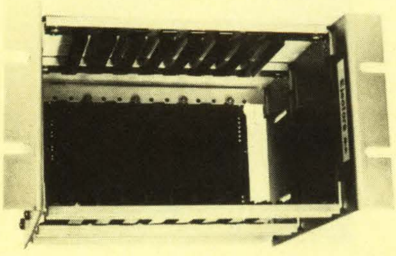

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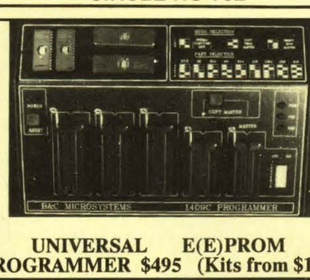

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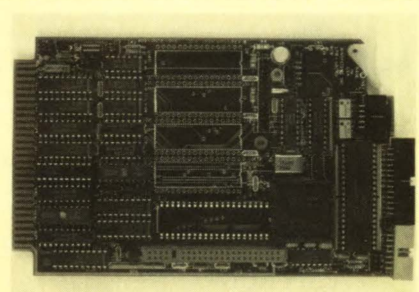

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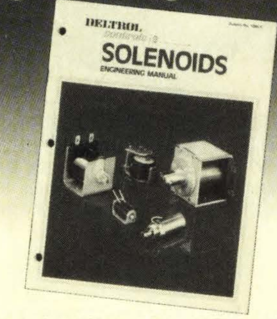

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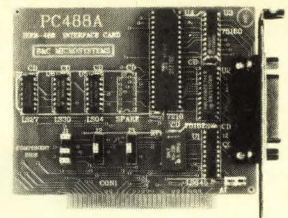

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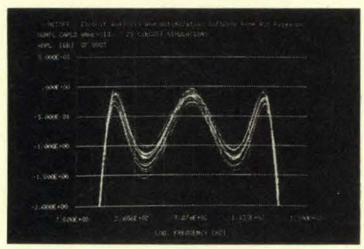

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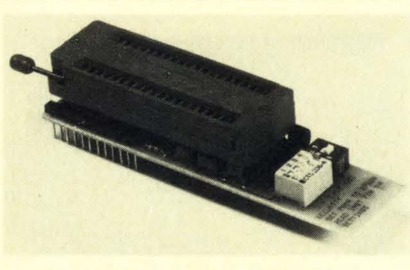

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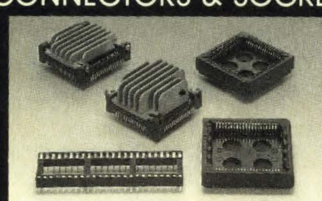

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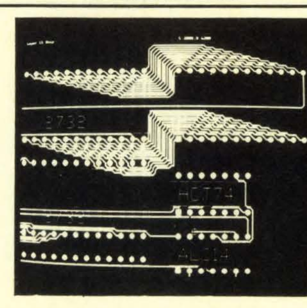

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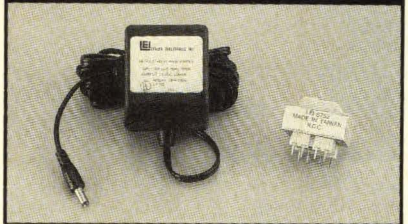

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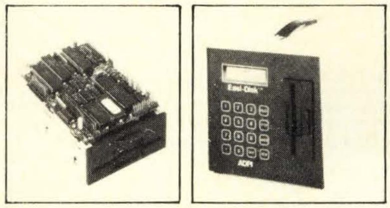

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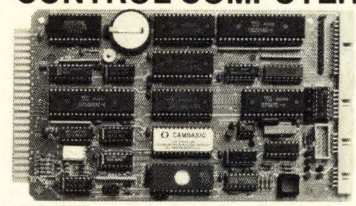

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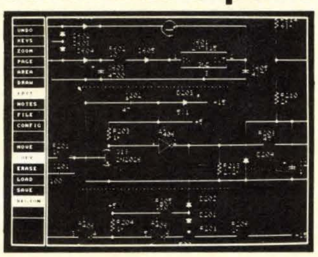

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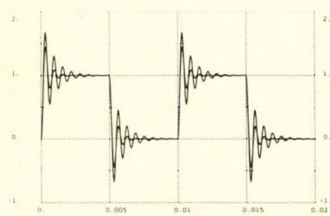

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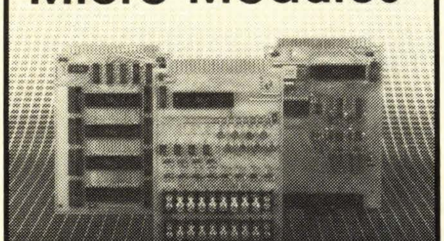

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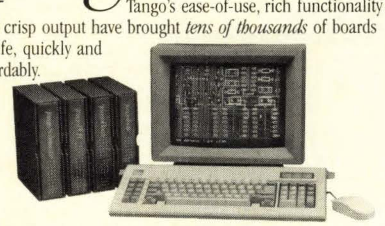

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CIRCLE NO 207

Video-based courses for database system, software

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Computer Technology Group, 310 S Michigan Ave, Chicago, IL 60604.

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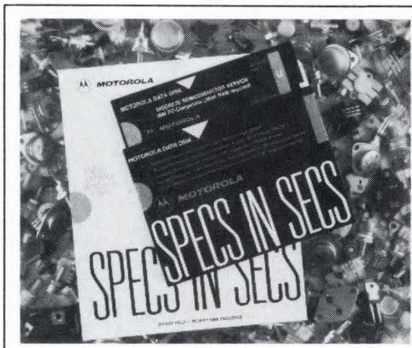

Search for discrete semiconductors on disk

The Discrete Semiconductor Version of *Specs in Secs* is the vendor's second catalog on disk, providing information on an entire line of discrete semiconductors. The selection encompasses bipolar power transistors, power MOSFETs, small-signal devices, RF devices, optoelectronic devices, rectifiers, zeners, thyristors, and sensors. The directory lists more than 6500 devices, 20,000 cross-references, 44 standard-package types, and 87,000 parameters. According to the vendor, when you make a search using either the part number or the parameter, the model numbers of the most suitable devices for your needs appear in order of suitability. You can then consult the appropriate data book or device data sheet to confirm your choice as the best selection. $2.

Motorola Semiconductor Products, Literature Distribution Center, Box 20912, Phoenix, AZ 85036.

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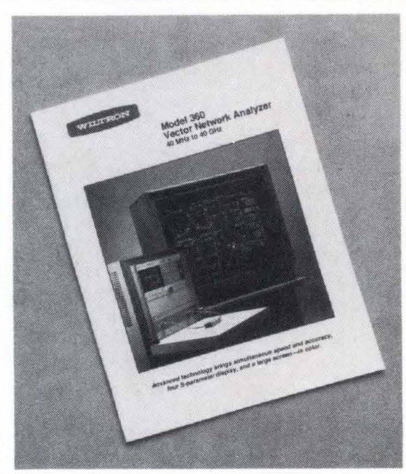

Booklet covers network analyzer

This 22-pg brochure describes the 360 vector network analyzer covering the 40-MHz to 40-GHz range. Application information includes measurement of complex impedance and transmission characteristics, amplitude and phase matching, group delay, semiconductor characteristics, insertion loss/gain and phase, and time domain. It illustrates the simultaneous display of four S parameters on a color screen. Further, it describes a 4-channel frequency converter that makes frequency-translation measurements. Specifications and ordering information complete the publication.

Wiltron, 490 Jarvis Dr, Morgan Hill, CA 95037.

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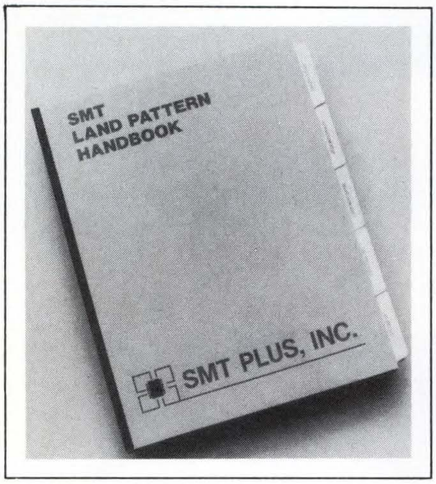

Handbook for SMT Land Patterns

The SMT Land Pattern Handbook consists of more than 80 completely dimensioned land patterns for SMT components. Each of its 12 sections begins with a list of instructions and suggestions. The categories of footprints used by the vendor are labeled SO (small-outline package) narrow body, SO medium body, SO wide body, SO metric, PLCC (plastic leaded chip carrier), LCC, quad flat packs, chip R/C (resistors and capacitors), tantalums, MELF (metal electrode face bonded), inductors, and SOT (small outline transistors). $99.95.

SMT Plus Inc, Box 612314, San Jose, CA 95161.

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Applications added to AutoCAD catalog

The new edition of the guide to third-party application development, the *AutoCAD Applications Catalog,* contains hundreds of entries. It covers application categories such as architectural engineering and construction, civil and

chemical engineering, computer-aided manufacturing, and desktop publishing.

AutoDesk Inc, 2320 Marinship Way, Sausalito, CA 94965.

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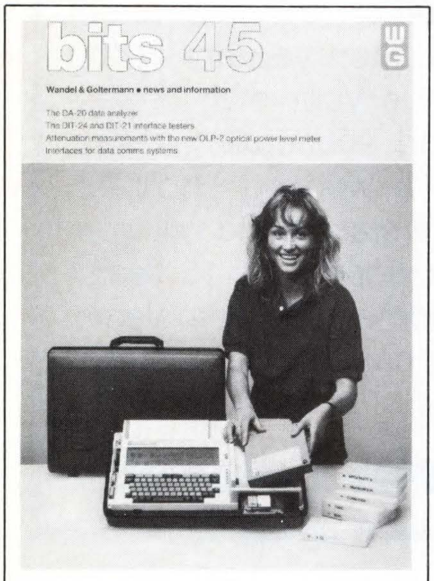


Periodical features test instruments

The latest issue (No 45) of *bits*, the vendor's magazine, highlights the DA-20 data analyzer, the DIT-24 and DIT-21 interface testers, attenuation measurements with the OLP-2 optical-power level meter, and interfaces for data-communications systems. This 32-pg edition comprises seven sections: current events, exhibitions, new products, glossary, product highlights, applications, and special reports. Photographs, diagrams, graphs, figures, and tables complete the publication.

Wandel & Goltermann GmbH & Co, Electronic Measurement Technology, Postfach 1262, D-7412 Eningen u A, West Germany.

Circle No 445

Booklet summarizes pc products

The vendor's compact 64-pg catalog (No 288) contains a listing of high-performance single-board computers and IBM PC/AT-compatible systems. Another section provides a list of components for packaging a passive-backplane system. The reference data section features such information as terminology, NEMA enclosure standards, an RS-232C pin guide, and RAM/ROM cross references.

Diversified Technology, Box 748, Ridgeland, MS 39158.

Circle No 446

Leaflet offers F-O multiplexer options

This 6-pg, fold-out brochure describes 15 port cards and their configurations. A chart provides detailed specifications, such as data rate or frequency response, interface type, number of channels, and signal type. The publication also includes photographs and diagrams.

Versitron Inc, 9005-8 Junction Dr, Annapolis Junction, MD 20701.

Circle No 447

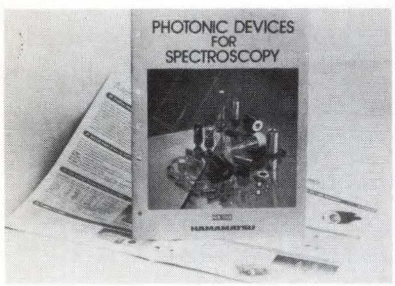
Reprint describes use of floating annular ring

This reprint of a paper published in *IEEE Transactions on Components, Hybrids, and Manufacturing Technology* discusses the "Advantages of a Floating Annular Ring in Three-Layer Tab Assembly." To help explain the advantages of using a floating support ring in tab assembly, it presents a figure with three drawings that show a comparison of three types of construction, one of which is the

annular-ring construction. The paper concludes with a discussion of applications and three additional figures.

Rogers Corp, Box 700, Chandler, AZ 85244.

Circle No 448



Catalog features devices for spectroscopy

This 1988 catalog of photonic devices describes more than 45 spectroscopic products, including 18 new devices. Among the products the catalog presents are photodiodes and photodiode arrays, photomultiplier tubes, detector tubes, and light-source lamps.

Hamamatsu Corp, Box 6910, Bridgewater, NJ 08807.

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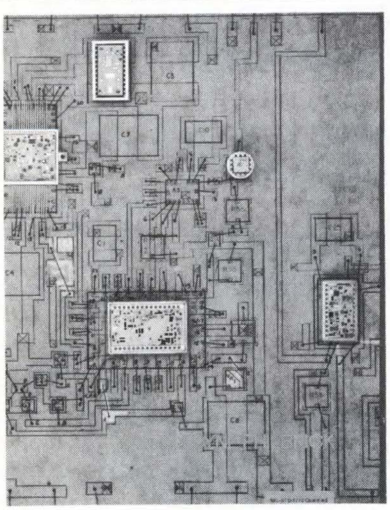

Publications present electronic circuits

An application note for A/D converters (AN-16) discusses bits effective bits in the role of measuring an ADC's ability to acquire a waveform and to represent it accurately. Equations, specifications, and a figure illustrate the material in the note's text. Another vendor's 8-pg brochure features a comprehensive product selection guide to its electronic products. The guide lists specifications for hybrid, monolithic, and module operational amplifiers; hybrid buffers; video display drivers; deglitchers; logarithmic, instrumentation, and track-and-hold amplifiers; ADCs; DACs; V/F, F/V, and sampling A/D converters; and modular power supplies.

Teledyne Philbrick, 40 Allied Dr, Dedham, MA 02026.

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EDN Databank Professional Profile

Announcing a new placement service for professional engineers!

To help you advance your career. Placement Services, Ltd. has formed the EDN Databank. What is the Databank? It is a computerized system of matching qualified candidates with positions that meet the applicant's professional needs and desires. What are the advantages of this new service?

- It's absolutely free. There are no fees or charges.
- The computer never forgets. When your type of job comes up, it remembers you're qualified.
- Service is nationwide. You'll be considered for openings across the U.S. by PSL and it's affiliated offices.
- Your identity is protected. Your resume is carefully screened to be sure it will not be sent to your company or parent organization.
- Your background and career objective will periodically be reviewed with you by a PSL professional placement person.

We hope you're happy in your current position. At the same time, chances are there is an ideal job you'd prefer if you knew about it. That's why it makes sense for you to register with the EDN Databank. To do so, just mail the completed form below, along with a copy of your resume, to: Placement Services, Ltd., Inc.

IDENTITY

Name ____
Home Address: ____
City ____ State: ____ Zip: ____
Home Phone (include area code): ____

PRESENT OR MOST RECENT EMPLOYER

Parent Company ____
Your division or subsidiary: ____
Location (City, State) ____
Business Phone if O.K. to use: ____

EDUCATION

Degrees (List)	Major Field	GPA	Year Degree Earned	College or University

EXPERIENCE Present or Most Recent Position From: To: Title:

Duties and Accomplishments: Industry of Current Employer:

Reason for Change:

POSITION DESIRED ____

PREVIOUS POSITION:

Job Title: ____
Employer: ____ From: ____ To: ____ City: ____ State: ____
Division: ____ Type of Industry: ____ Salary: ____
Duties and Accomplishments: ____

COMPENSATION/PERSONAL INFORMATION

Years Experience	Base Salary	Commission	Bonus	Total Compensation	Asking Compensation	Min. Compensation

Date Available ____ I Will Travel ☐ Light ☐ Moderate ☐ Heavy ☐ I own my home. How long? ____ I rent my home/apt. ☐

☐ Employed ☐ Self-Employed ☐ Unemployed ☐ Married ☐ Single Height ____ Weight ____

Level of Security Clearance ____ ☐ U.S. Citizen ☐ Non-U.S. Citizen My identity may be released to: ☐ Any employer ☐ All but present employer

☐ WILL RELOCATE ☐ WILL NOT RELOCATE ☐ OTHER ____

EDN Databank

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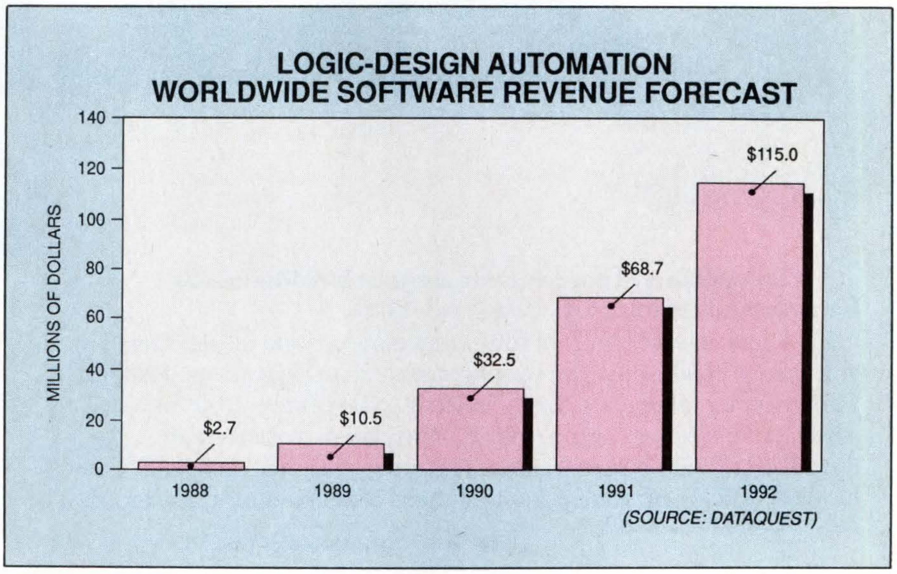


A relatively new area of CAE has the potential to revolutionize hardware design within the next few years, according to Dataquest Inc (San Jose, CA). Logic-design automation (LDA) tools help engineers specify, create, and optimize their designs. They promise to improve productivity and save both time and money. These software packages offer a complement to rather than a replacement for standard CAE tools. They solve up-front problems and, if properly integrated, feed easily into exisiting CAE setups. Although sales of these tools net just $5 million today, Dataquest predicts that the market will be worth $115 million by 1992.

Dataquest defines LDA tools as software that starts with a circuit description, either textual or schematic, and user-supplied objectives, like path delays. The software then generates, without operator intervention, a net list, a schematic, or recommendations for changing a schematic. LDA tools can thus include the complex tools that produce schematics from behavioral languages as well as the simplistic tools that convert truth tables into PLA formats.

Some engineers, particularly in academic circles, have applied the term "logic synthesis" to some of the tools that, by Dataquest's definition, are LDA tools. But LDA should really mean automation, not synthesis. It's a broader term than logic synthesis. LDA also defines a market niche, whereas synthesis describes a technology.

LDA tools can be divided into three function categories: specification and architectural analysis, logic optimization and minimization, and technology selection and instantiation. Specification and analysis tools can be simple mapping systems for PLD programming. Or they can be sophisticated ones, like those that let engineers express designs as high-level flows, controls, and timing in a variety of formats that the tools can then analyze.

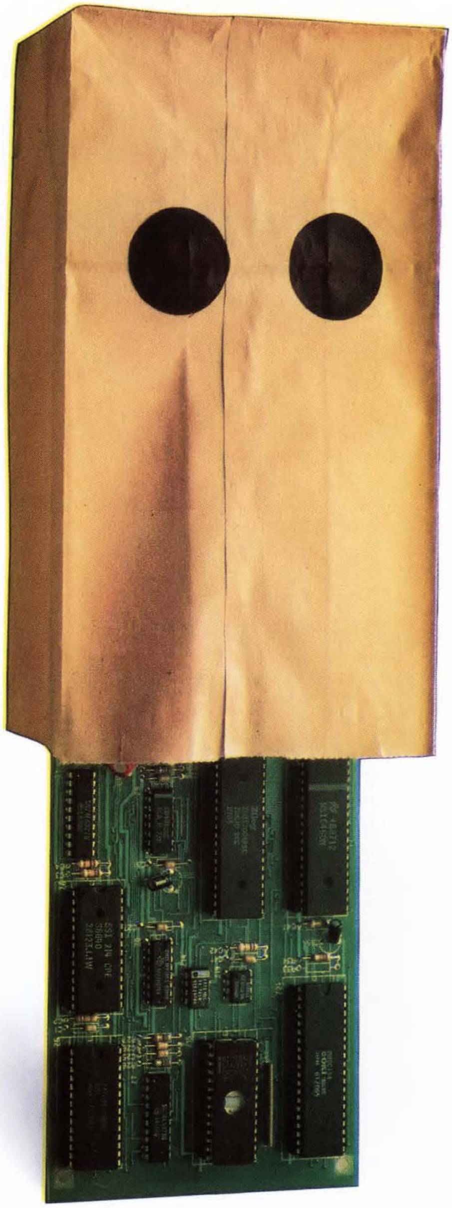
The category of logic optimization and minimization encompasses tools that use all the logic available as effectively as possible and then either modify the schematics directly or provide suggestions for improvements. These tools improve the quality of a design.

Technology selection and instantiation tools aid in both technology selection and the presentation of the design in a concrete form. Thus some packages might be able to predict the performance of a given design as a standard cell and as a gate array. Other tools might automatically convert an existing board schematic into a gate or transfer from one gate-array vendor's library to another. These options give the engineer a good deal of technology independence.

Potentially, LDA can give designers short-term dollar savings and long-term productivity gains. In the short run, designers can obtain quick access to the lowest-cost technology or ASIC vendor. They can also realize significant reductions in circuit size and cost, while reducing the time they spend on isolated schematic entry errors. In addition, the start-up costs of LDA are relatively low.

In the long run, engineers will find that they can evaluate technologies and architectures in parallel early on in the design process and optimize specifications and schematics simultaneously. Furthermore, they have some flexibility when it comes to technologies.

Dataquest predicts that companies will be quick to adopt these new tools and that the real issues that may slow market growth involve the quality of the LDA products themselves. Specifically, LDA vendors must deliver fully working tools that are reliable and produce correct designs. Secondly, LDA tools must preserve the customers' CAE equipment, working along with it. And thirdly, LDA vendors must consider other technologies that are moving into the CAE market. Trends toward system-level design, behavioral simulation, and description languages will be creating their own effects in the CAE marketplace. LDA tools should take these trends into account.



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