A CAHNERS PUBLICATION

MAY 14, 1987

EDN

SPECIAL ISSUE:
Analog technology

Evaluating op amps' ac characteristics

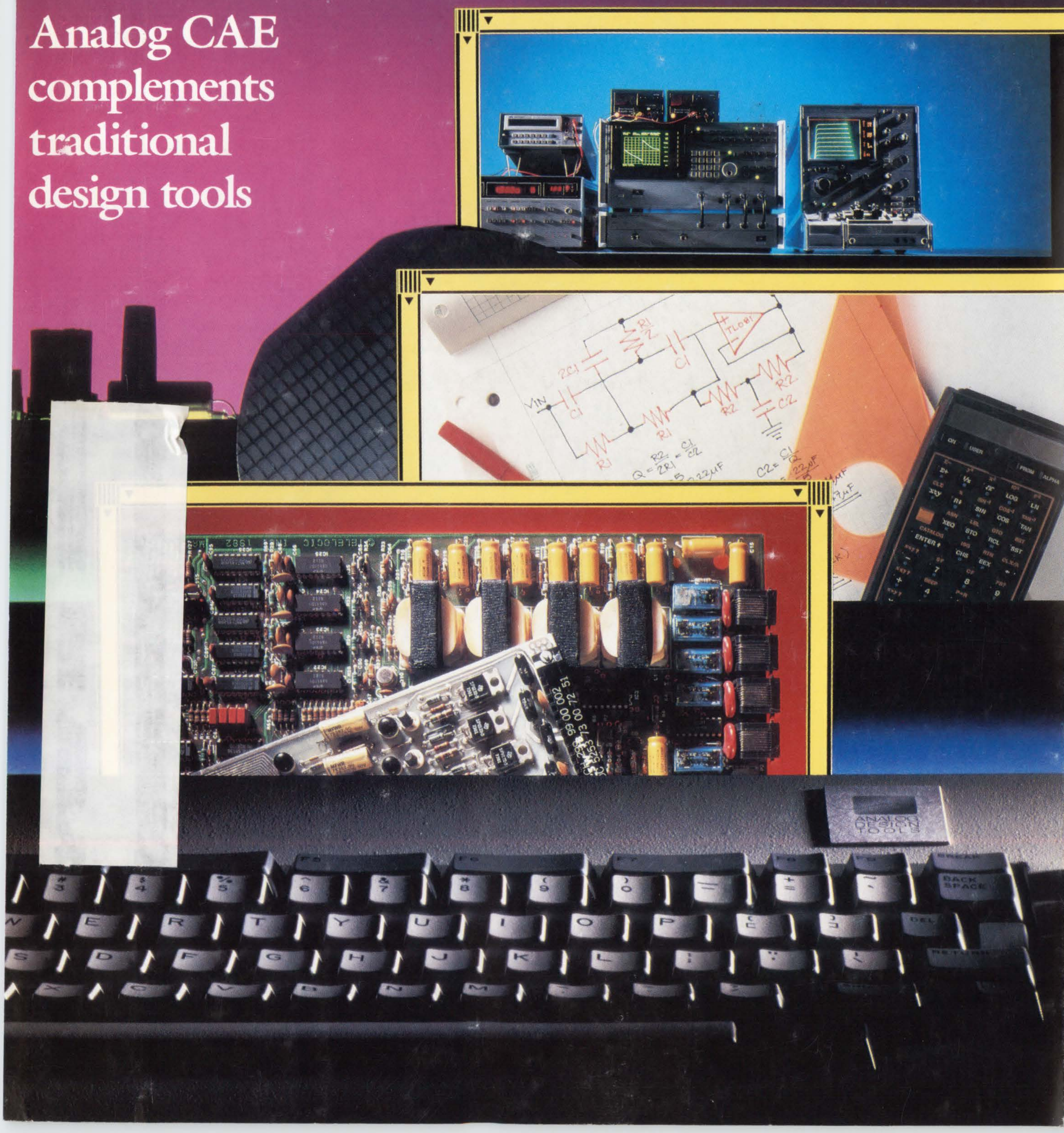
Analog multiplexers

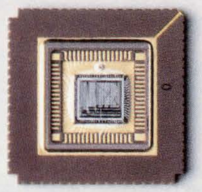
Video-interface circuits

JFET-input op amps

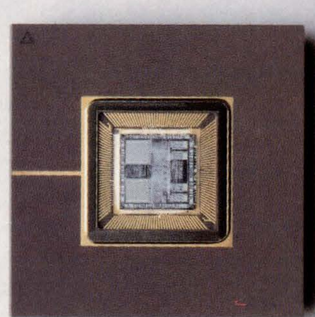
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Analog CAE complements traditional design tools

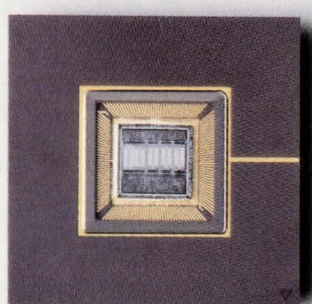




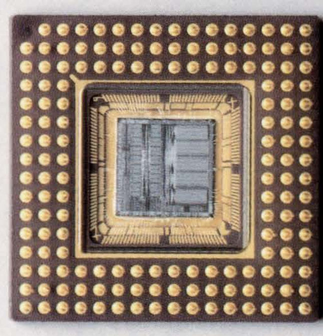
Our MACGEN silicon compiler developed the world's fastest 16-bit multiplier accumulator.



High Performance cell-based 1750 CPU combines logic, ROM and processors.

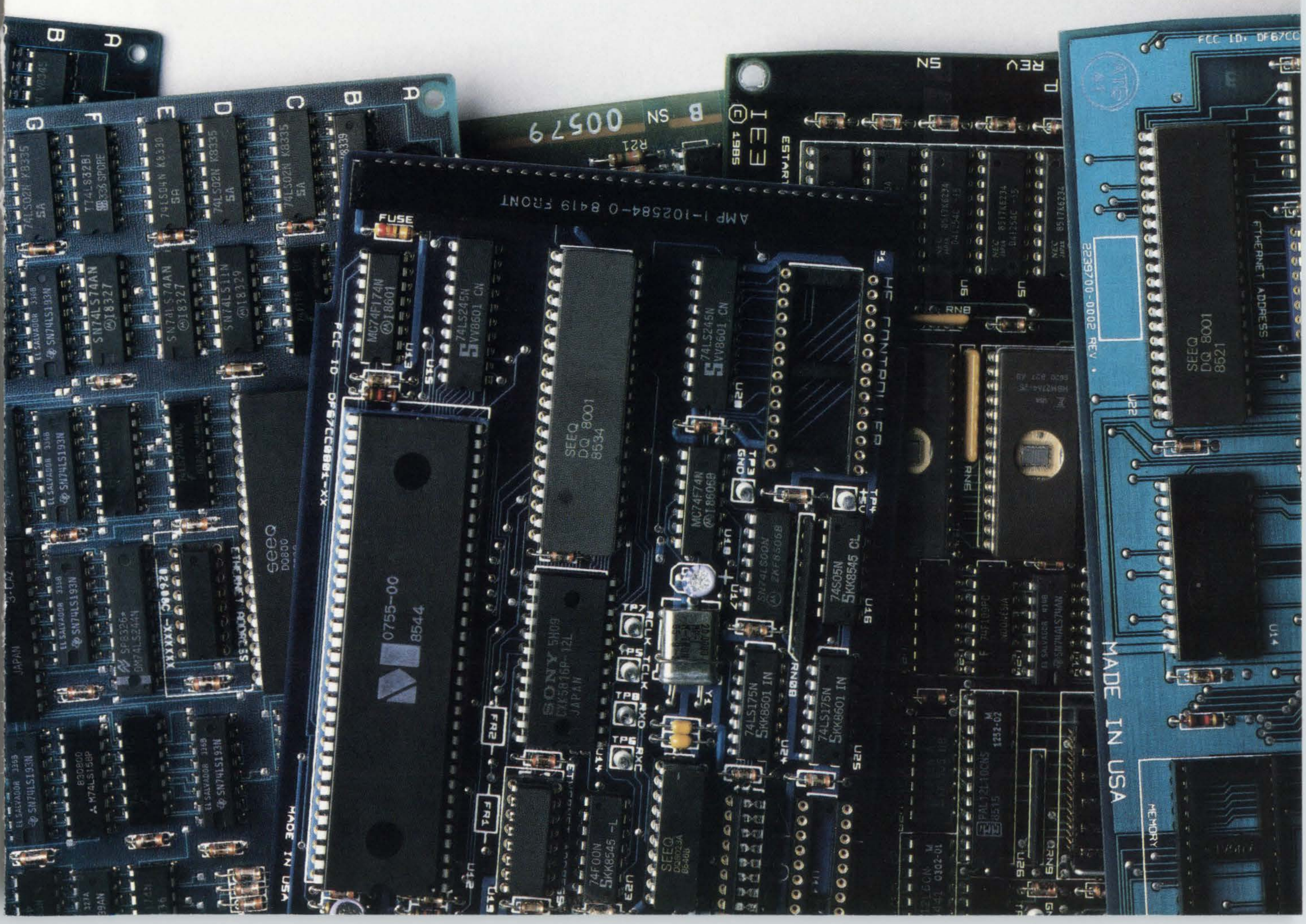


Structured Arrays combine high-density memories with up to 41,000 logic gates.



Channel-free Compacted Arrays combine logic and memory functions with up to 129,000 available (up to 70,000 utilized) gates.

HOW TO AVOID GOING OVERBOARD.



THIS PC/XT-COMPATIBLE INDUSTRIAL COMPUTER MAY HAVE ONE FAILING...EVERY 7 YEARS.

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System 2 comes with Microsoft's MS-DOS 3.2 operating system and runs **Lotus 1-2-3** and **Flight Simulator**. So it's PC/XT-compatible, right down to the chip level. Which is important for running industrial software, where real time response is needed.

Data acquisition, process monitoring and control, and multitasking software, plus a wide selection of editors, debuggers, and high-level languages are available. Many of them from Pro-Log.

HARD-WEARING HARDWARE

System 2 is based on the industry-standard STD BUS. So a wealth of industrial quality add-on products is available from over 100 STD BUS manufacturers.

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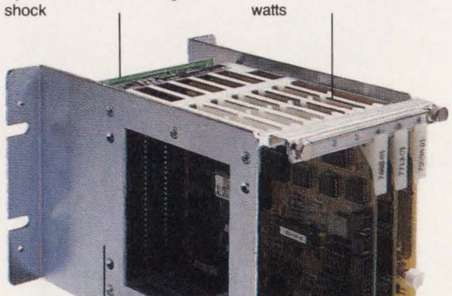
You expand System 2 by simply plugging in additional STD BUS cards. Up to 23 expansion slots are available and many options, such as 640K bytes of memory, EGA/Keyboard interface, and printer interface, can be factory installed.



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*Thermal and mechanical specifications are reduced by the use of mechanical disk drives.

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PL055

INDUSTRIAL COMPUTERS PRO-LOG IN CONTROL QUALITY

Circle 58 for literature request only

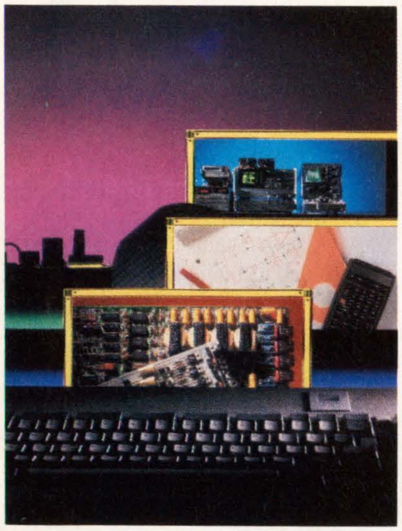
Circle 19 for direct factory response

Volume 32, Number 10

EDN

May 14, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Analog CAE systems are now among the tools you can select to speed your linear designs. But you'll need to develop the skill to know when to use the CAE systems and when to rely on the traditional benchtop instruments. See pg 138. (Photo courtesy Analog Design Tools)*

DESIGN FEATURES

Continued on page 7

BPA ABP

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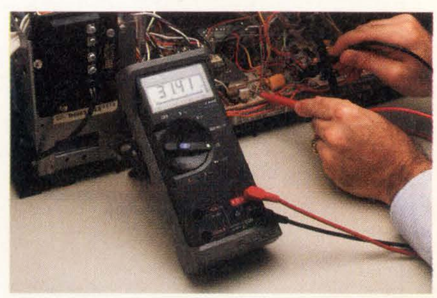

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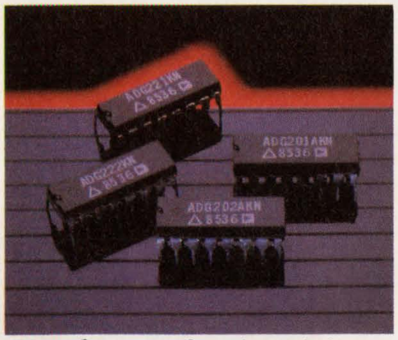
CIRCLE NO 72

Continued from page 5



***Manufacturers of analog switches and multiplexers** are reducing their products' on-resistances and internal capacitances, extending their bandwidths, and improving their breakdown-voltage tolerances (pg 65).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

Advertising and editorial offices: 275 Washington St, Newton, MA 02158. Phone (617) 964-3030. Subscription offices: 270 St Paul St, Denver, CO 80206. Phone (303) 388-4511. EDN® is circulated without charge to those qualified. Subscription to others: US, $95/year, $6/copy; Canada and Mexico, $110/year, $8/copy; Europe Air Mail, $135/year, $10/copy; all other nations surface mail, $135/year, $10/copy; all other nations Air Mail, $200/year. Special issue prices may vary. Send requests for qualification forms and/or change of address to subscription office.

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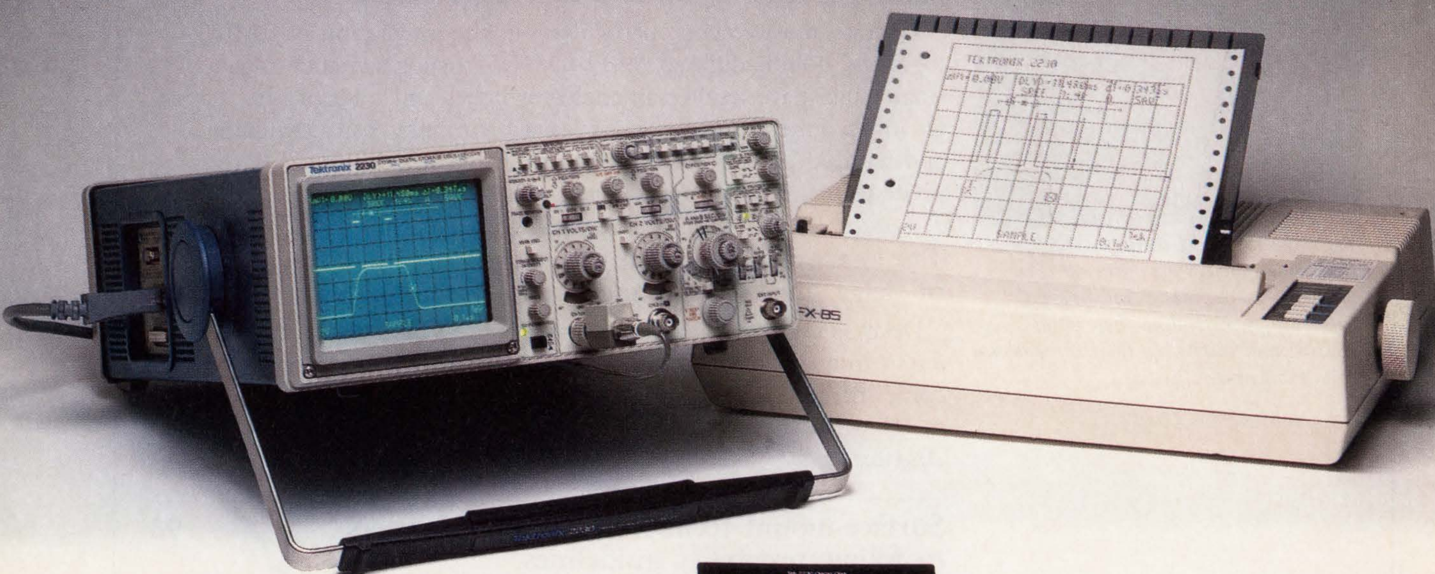

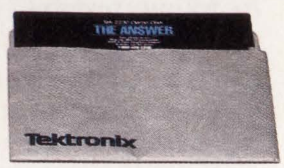

Now get automatic answers easily, economically, with immediate hard copy output. The 100 MHz Tek 2230 or 60 MHz 2220 are high-performance, high-value digital storage oscilloscopes. Equip either with an optional GPIB or RS-232-C interface and digitized data can be ported to your PC, sent over phone lines, or directed to your printer or plotter for hard copies.

With either option the 2230 includes battery-backed memory that provides 26K of keep-alive CMOS memory—for storing up to 26 waveform sets.

Expect the most for your money—and get it—with Tek. You can capture events as narrow as 100 ns at any sweep speed thanks to our proprietary peak detect mode. Trigger on complex waveforms using variable sweep holdoff. View events occurring prior to or after a trigger event with pre/post trigger. Eliminate noise with built-in signal averaging. Store acquired waveforms as either 1K or 4K records. And simply push a button for real-time display analysis — the 2230 and 2220 double as conventional analog scopes.

Features	2230	2220
Analog/Digital Storage BW	100 MHz	60 MHz
Max. Sampling Speed	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K
Save Reference Memory	One, 4K Three, 1K	One, 4K
Vertical Resolution	8 bits 10 bits (AVG mode) 12 bits (AVG mode over bus)	8 bits
CRT Readout	Yes	No
Cursor Measurements	Yes (storage mode)	No
GPIB/RS-232-C Options	Yes ($850)	Yes ($550)
Battery-Backed Memory (save 26 waveform sets)	Yes (inc. with 2230 communications options)	No
Price	$5150	$4150

You can increase vertical resolution—via the bus—from 8 to 12 bits with signal averaging. And Tek software is available to help you get the most from your systems configurations.

Call Tek direct for a free diskette demo. Or to place an order! Technical personnel will answer your questions, take an order and expedite delivery. Orders include complete documentation, operating manuals, worldwide service back-up and Tek's 3-year warranty that even covers the CRT.

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CIRCLE NO 73

Continued from page 7

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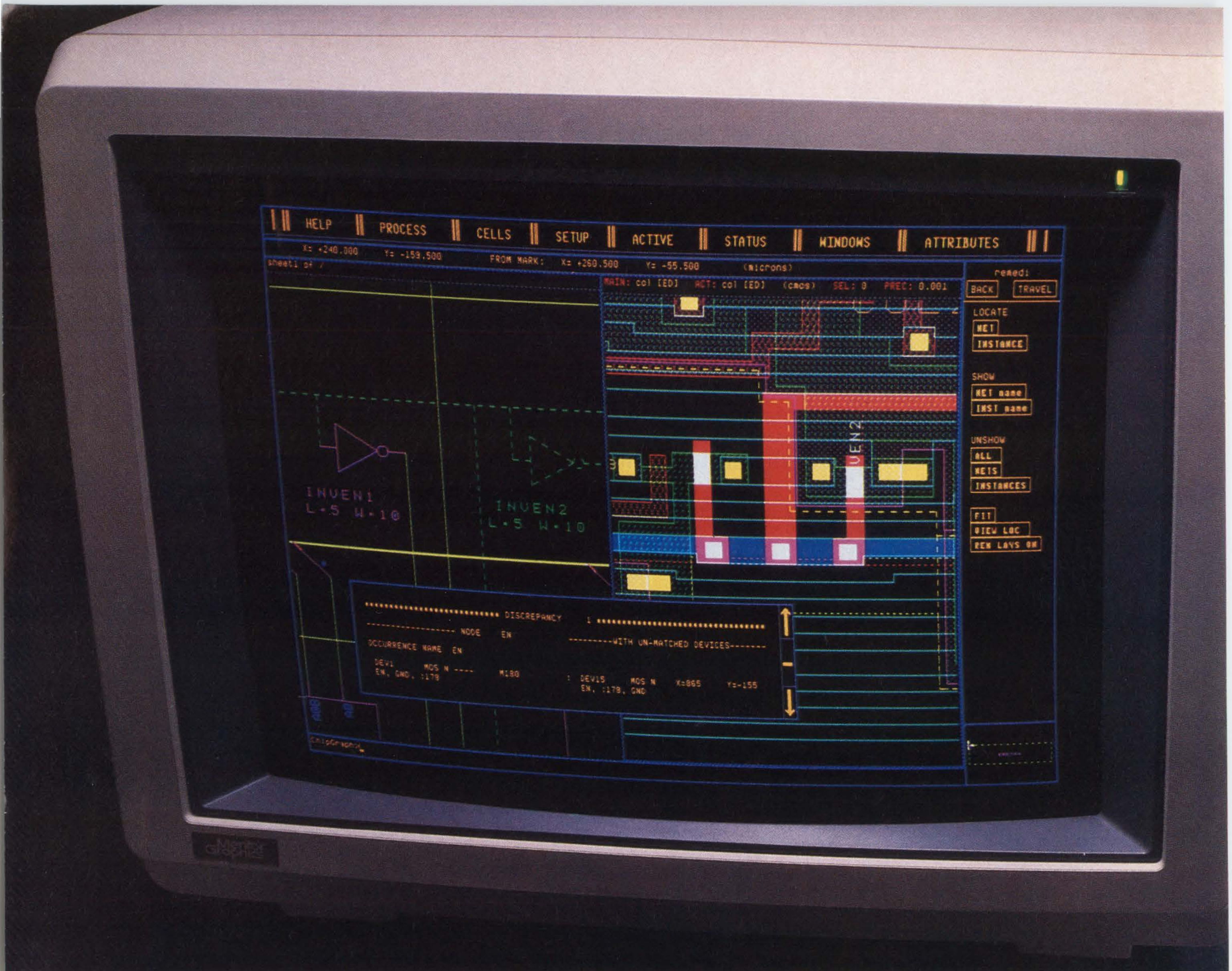


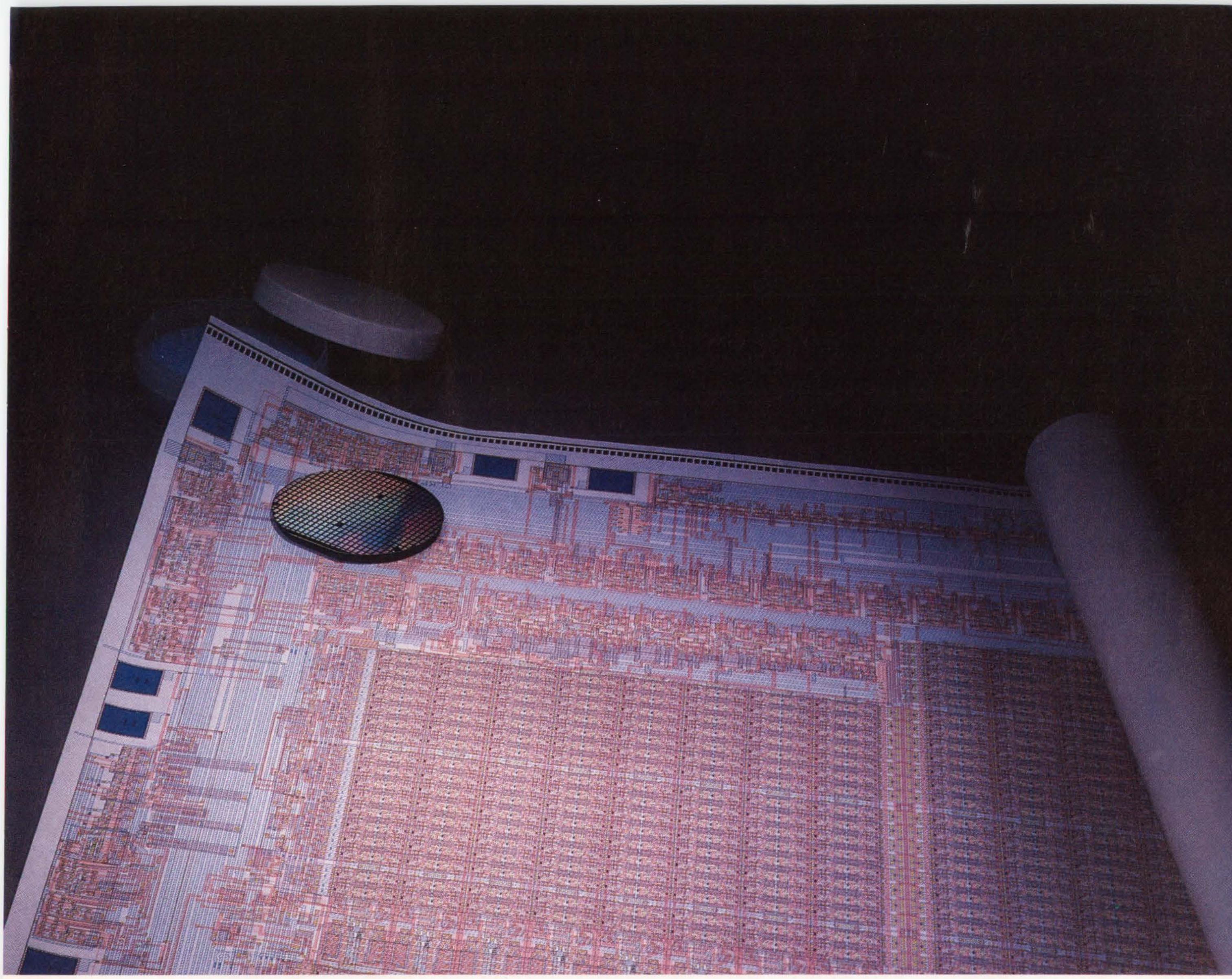
Only Mentor Graphics maps symbols to silicon.

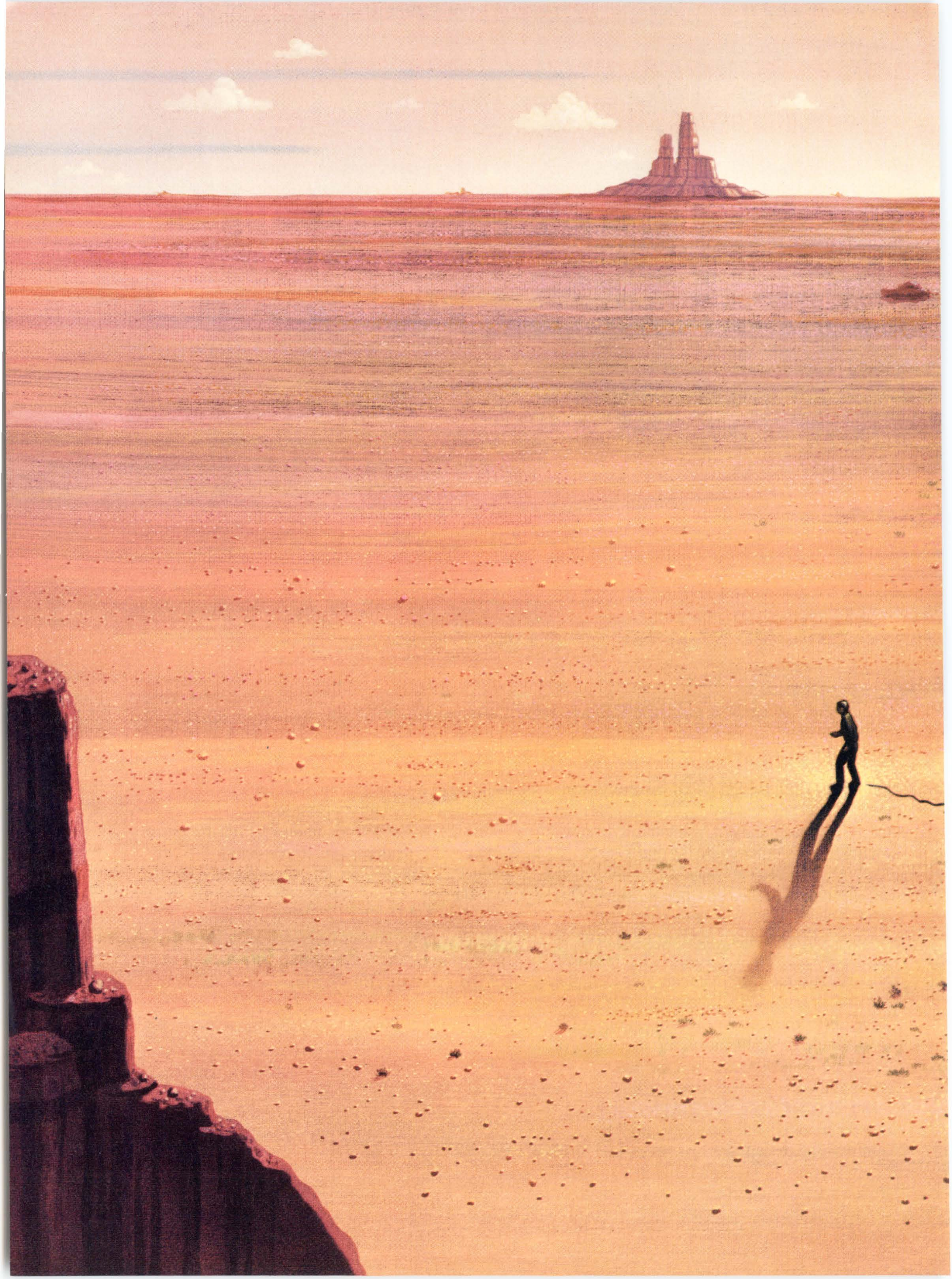
The bigger the IC design, the bigger the problem: you're trying to locate a discrepancy between the schematic and your IC layout, but all you have is an ASCII error report. It's like driving all over a strange city to find an address — without a map.

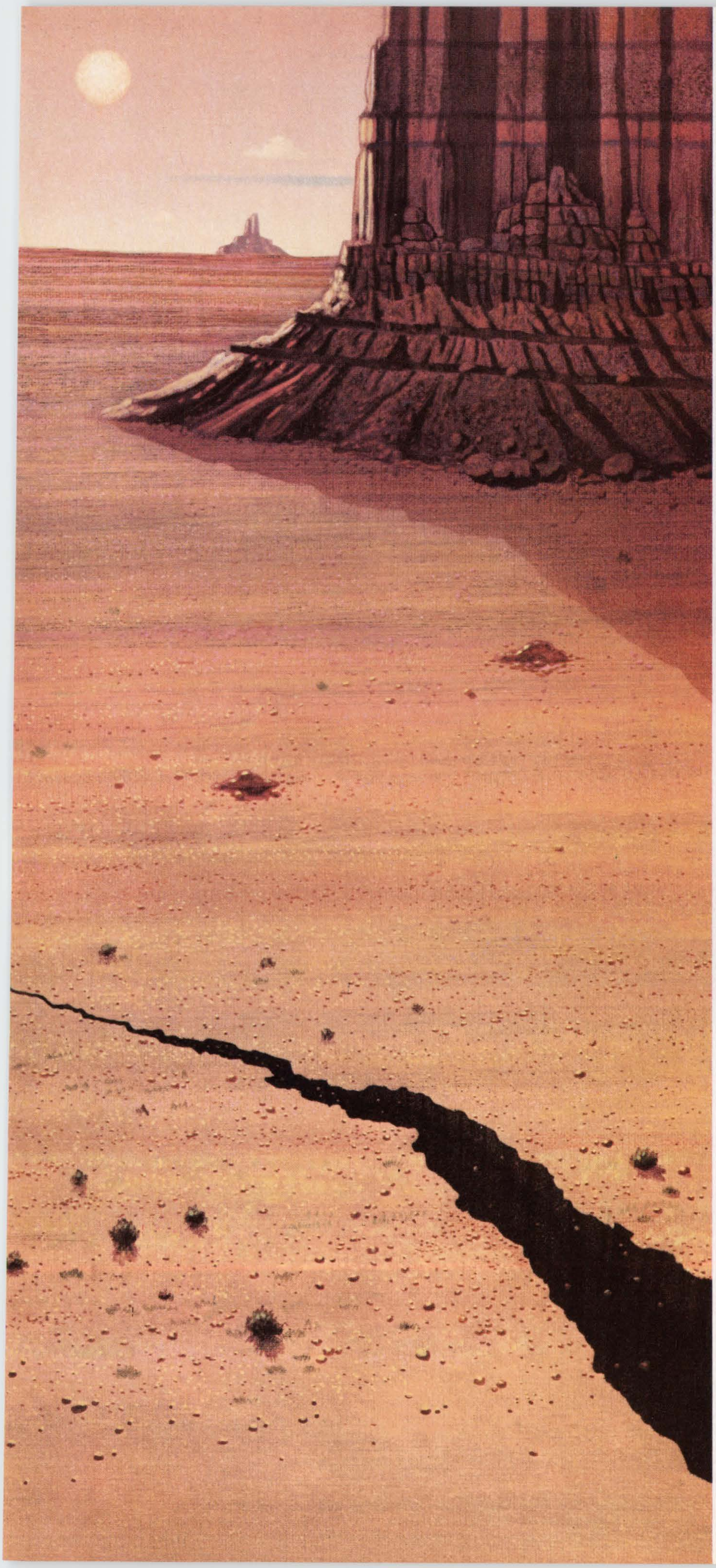
That's why Mentor Graphics created REMEDI,™ a graphical interface that helps debug complex layouts. REMEDI works with Dracula II, taking the leading layout verification package's layout-versus-schematic checks a step further. LVS errors detected with Dracula II can be quickly pinpointed on both the layout and schematic using REMEDI's interactive graphical correlation capabilities.

And, because REMEDI is part of ChipGraph,™ the powerful Mentor Graphics full custom IC layout editor, as soon as you find an error you can fix it. There's no need to move back and forth between the layout editor and the debugging tool to correct the design database.

Today's complex VLSI designs demand a layout tool that lets you create and navigate efficiently through a maze of mask data. So ChipGraph provides flexible geometry editing and fast cell-based layout tools. Beyond this,







Everything doesn't need to be your fault.

Designing a new system has enough risks. Why pass up an off-the-shelf sure thing like AMD's complete Ethernet chip set?

We designed the Am7990 Lance, Am7992B SIA, and the AM7996 Transceiver to work with one another. And what happened? They work with one another.

AMD can offer you something no one else can offer. Absolute confidence.

Our chip set has been around since the beginning of Ethernet. It's been proven by years of successful networking in systems. That means you won't be designing it in, then covering your tracks when it doesn't work. (And if you work with Cheapernet, you're still safe, because our chip set does, too.)

Look at it this way:

You're going to get blamed for a few things in life that are absolutely not your fault. Why not choose the AMD Ethernet chip set and pick up some easy praise?

Advanced Micro Devices

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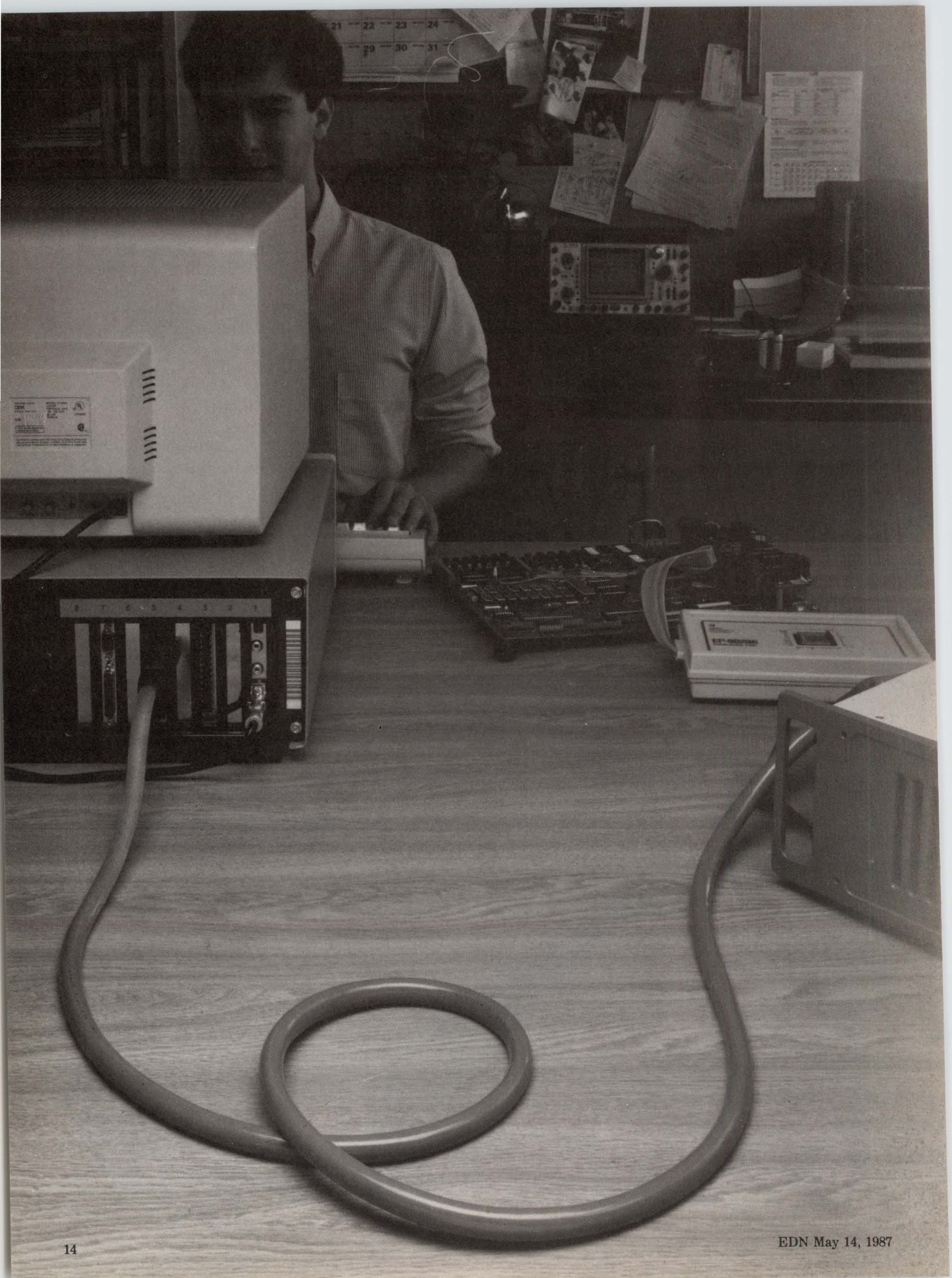

Are your suppliers giving you less attention than you deserve?

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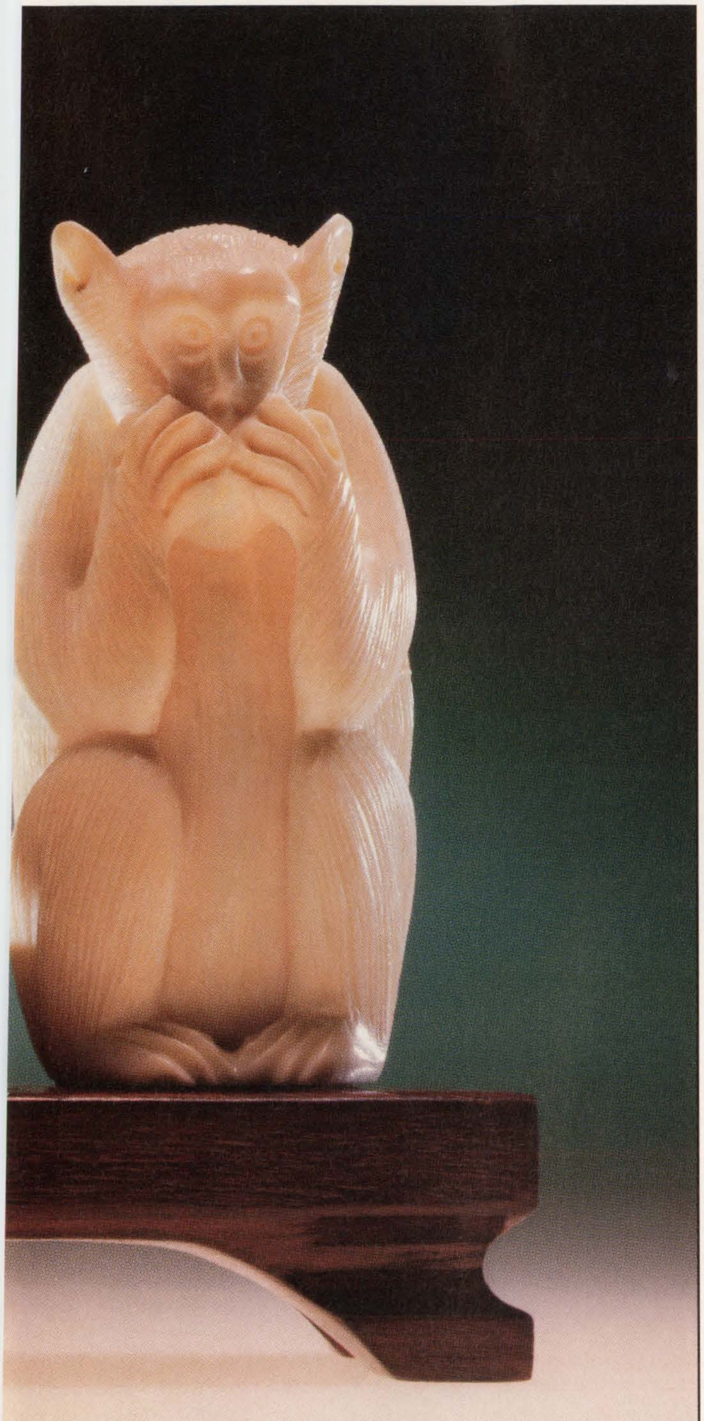

First, there's our network of Field Applications Engineers, 50 or so of the most highly evolved minds in the field.

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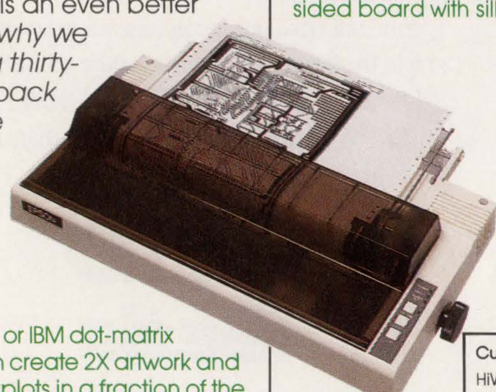
smARTWORK transforms your IBM PC into a PCB CAD system

Interactive routing, continual design-rule checking, pad shaving, and production-quality 2X artwork have always been a part of smARTWORK. And now that many customer suggestions have become a part of the software, smARTWORK is an even better value. *That's why we offer it with a thirty-day money-back no-nonsense guarantee.*



Using an Epson or IBM dot-matrix printer, you can create 2X artwork and 1X or 2X checkplots in a fraction of the time hand-taping requires

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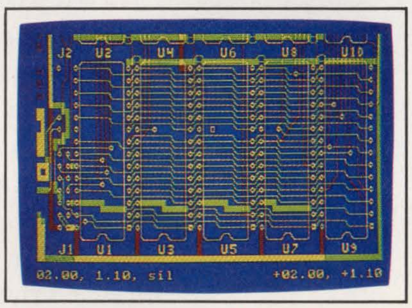

2" by 4" section of a 10" by 16" double-sided board with silkscreen layer

Current Versions	
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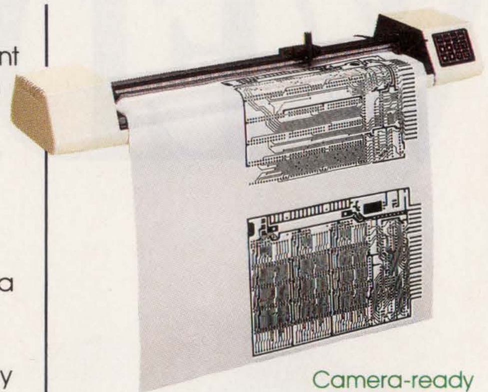

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- ☐ IBM Graphics Printer or Epson FX/MX/RX-series printer, and/or
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CIRCLE NO 78

EDITED BY JOAN MORROW

FUNCTIONAL LOGIC TESTERS TEST OVER −55 TO +177°C

A line of parallel functional testers for engineering, quality-assurance, and reliability applications will be shown by Aehr Test Systems (Menlo Park, CA) at Semicon/West '87 next week. (The show will be held in San Mateo, CA, on the 18th to the 21st.) The MBT-208 Series includes four burn-in/test systems designed for testing memory and logic devices over −55 to +177°C. Device capacity varies with IC package size and required test speeds. Typically, you can test as many as 3000 dynamic RAMs at one time.

The four models differ in their pattern-generation capabilities. The MBT-208 with the VSP pattern generator is optimized for logic quality/reliability applications. The other three pattern generators are optimized for memory quality/reliability or memory functional characterization applications.

Prices for the MBT-208 range from $198,000 to $300,000 depending on the pattern generator. (Production testers with higher throughput rates cost more than $500,000.) Models are complete turnkey systems that include host programmer/controller, software license, and operator training.—Chris Everett

SUB-$550 40M-BYTE DRIVE INCLUDES SCSI IN 3½-IN. PACKAGE

The Spartan LT4000 Winchester drive from Lapine Technology (Milpitas, CA, (408) 262-7077) serves the new generation of small computers that need 40M bytes of storage. The drive, which costs less than $550 (1000), includes an embedded SCSI (Small Computer System Interface) controller in the 3½-in. package. Although the drive employs a stepper motor to drive the actuator, it performs average seeks in less than 35 msec. Worst-case seeks finish in less than 80 msec. The drive dissipates 15W from 5 and 12V supplies.—Maury Wright

THREE AUTOROUTERS ACCELERATE PC-BOARD LAYOUT

Three CAD vendors are introducing autorouters for their pc-board layout systems. Each of the autorouters attempts to connect components on a layout without adding unnecessary vias and signal layers.

Racal-Redac (Westford, MA) hasn't changed its $24,000 Visula autorouter, but it has increased the operating speed of the software. The company has ported the autorouter to a superminicomputer developed by MIPS Computer Systems (Sunnyvale, CA). The Mipper superminicomputer specs an operating speed of 8 MIPS, which enables the router to run six times faster than it does on an Apollo DN3000 workstation. It includes a 337M-byte hard-disk drive, a streaming-tape drive, and 8M bytes of RAM and costs $79,950.

At the lower end of the price spectrum, Accel Technologies (San Diego, CA) is bringing out a $495 autorouter that runs on IBM PCs. The Tango-Route autorouter interfaces to the company's $495 pc-board layout system. Features of the autorouter include 90° and 45° routing, a maximum board size of 32×19 in., and as many as four layers.

The third autorouter combines IBM PC compatibility and a hardware accelerator. To use Bishop Graphics' (Westlake Village, CA) Pathfinder pc-board layout program, you run Autodesk's (Sausalito, CA) AutoCAD drafting package on an IBM PC and add a plug-in card for autorouting. The autorouter card is available in two configurations—

the standard version contains an 8-MHz, 8-bit μP; the second model uses a 25-MHz, 32-bit μP. The 25-MHz autorouter runs seven times faster than the 8-MHz card. The fast model costs $5990; the standard version costs $2995.—Eva Freeman

RCA TO INTRODUCE VIDEO-RATE DSP CHIPS

Look for RCA to introduce a new line of DSP chips aimed at high-end DSP applications. The chips should be introduced some time in early summer and will be suitable for video DSP applications. The line will include a programmable FIR filter, a least-means-squared adaptive FIR filter, and a programmable-length FIFO buffer. The parts will feature 8-bit, 14-MHz performance.—Jim Wiegand

SURFACE-MOUNTABLE THERMISTOR IS HERMETICALLY SEALED

The surface-mount-sensor (SMS) line of hermetically sealed thermistors from Midwest Components Inc (Muskegon, MI) offers designers low-cost devices for measuring temperature or providing thermal-compensation on SMT pc boards. Devices in the series come in cylindrical packages that resemble MELF diodes. They cost $0.30 (10,000) and are offered in resistance values ranging from 2 kΩ to 1 MΩ. The manufacturer also offers the device on tape-and-reel.—Steven H Leibson

ANALOG AND DIGITAL SIMULATORS EXPAND THEIR MODEL LIBRARIES

Mentor Graphics (Beaverton, OR) has increased the size of its analog-device library to 920 models. The library includes op amps, bipolar transistors, zener diodes, MOSFETs, and diodes. The library costs $20,000 for the first copy; additional licenses cost $2000.

Digital designers can use Quadtree's (Bridgewater, NJ) Designers' Choice behavioral models to simulate VHSIC (very-high-speed IC) systems. The models simulate a set of high-speed digital chips from TRW's Electronics and Technology Div (Redondo Beach, CA). The device library includes a window- and a content-addressable memory, a matrix switch, a microcontroller, an address generator, and a multiplier/accumulator. Models will be sold only to qualified US defense contractors. Each behavioral model costs $5000; the complete set of eight models costs $32,000. Shipments of the models will begin in August.—Eva Freeman

FORWARD-ERROR-CORRECTION CHIP IS FASTER THAN PREDECESSOR

Featuring a 20M-bps data rate, the SRT 241203-I Hyper-Fec III forward-error-correction IC can correct as many as three errors and detect as many as four errors in each 12-bit data word. Available from Space Research Technology Inc (Austin, TX), the device is pin compatible with the company's earlier, 2.5M-bps error-correction part and costs 40% less. The $75 chip contains an encoder and decoder that, respectively, convert each data word by adding or stripping 12 check bits to the 12 data bits. The encoder and decoder can operate at different data rates.—Steven H Leibson

Until today, the only way you could get a true video speed, 12-bit D/A converter was by compromising signal integrity, power dissipation and cost.

Now, TRW LSI Products Division, the leader in high-performance D/A converters, offers you the ideal alternative. Meet the TDC1012, a monolithic 12-bit D/A converter that operates at a 20MHz data rate and settles in an incredibly fast 30ns.

The TDC1012 not only leads the way in settling time, it also features rise/fall times of less than 4ns. And it does all this while holding output glitches to 25pV-sec... so you can forget about that expensive deglitcher circuit.

As for price—very attractive! The TDC1012 is available in a 24-lead plastic or ceramic package, with prices starting at $35.

For optimum flexibility and performance, the TDC1012's complementary outputs are capable of driving 40mA into a doubly terminated 50 ohm transmission line. Power dissipation is a cool 1.1W. And, of course, the TDC1012 is TTL compatible and operates from standard +5V and −5.2V power supplies.

This breakthrough in converter technology is made possible by TRW's Omicron-B™ one-micron triple diffused process. It's available now from Arrow Electronics, Hall-Mark and Hamilton-Avnet.

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8000 Muenchen 70, W. Germany,
089.7103.115

In the Orient, phone:
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Tokyo, 03.461.5121; Taipei, 751.2062;
Seoul, 2.553.0901

TRW

LSI Products Division
TRW Electronic Components Group

NEWS BREAKS: INTERNATIONAL

BIPOLAR POWER TRANSISTORS SUIT HIGH-FREQUENCY CONVERTERS

High-voltage, bipolar power transistors in the ETD (Easy-To-Drive) Series from Thomson Semiconducteurs (Paris, France, TLX 204780; in the US, (201) 438-2300) are capable of 100-kHz switching. The series includes 10 and 20A (IC_{SAT}) transistors with a V_{CEW} rating of 400V and V_{CEV} ratings of 850 or 1000V. All the transistors have a maximum fall time at 100°C of 0.15 μsec.

Operated without negative base bias, ETD transistors switch as fast as conventional bipolar transistors with negative base bias and therefore allow simplification of base-drive circuitry. In addition, their extended RBSOA (reverse bias safe operating area) allows you to use them without, or with smaller, snubber components. The BUF410, a 10A/850V transistor, sells for around Fr fr 11 (10,000).—Peter Harold

JAPANESE CAMERA INCORPORATES AMERICAN SEMICONDUCTORS

The recently introduced EOS 620 and EOS 650 35-mm, automatic-focus cameras from Canon (Tokyo) incorporate three different surface-mountable semiconductor devices developed and marketed by Motorola Inc (Phoenix, AZ). An MC68HC11 μC packaged in a 64-lead, gull-wing chip carrier acts as the camera's main processor and exposure-control element and communicates over a serial link with μCs embedded inside each lens in the EOS autofocus series. Two MPC1710 smart-power motor controllers operate the camera's shutter and film-movement motors, and an SFX10 power FET controls the internal power bus.—Steven H Leibson

SINGLE-BOARD COMPUTER ADAPTS TO OEM REQUIREMENTS

Targeted at workstation OEMs, the JT-68020 VME Bus-compatible single-board computer from Integrated Micro Products (Consett, UK, TLX 537747) accepts a piggyback 68851 paged-MMU module that allows it to run Uniplus+ v2.2 (version 3 is currently being ported). The board runs a 16-, 20-, or 25-MHz 68020 μP and an optional 68881 math coprocessor; it can be supplied with as much as 4M bytes of onboard dual-port RAM. Space for 2M bytes of EPROM and as much as 32k bytes of static or nonvolatile RAM is also provided.

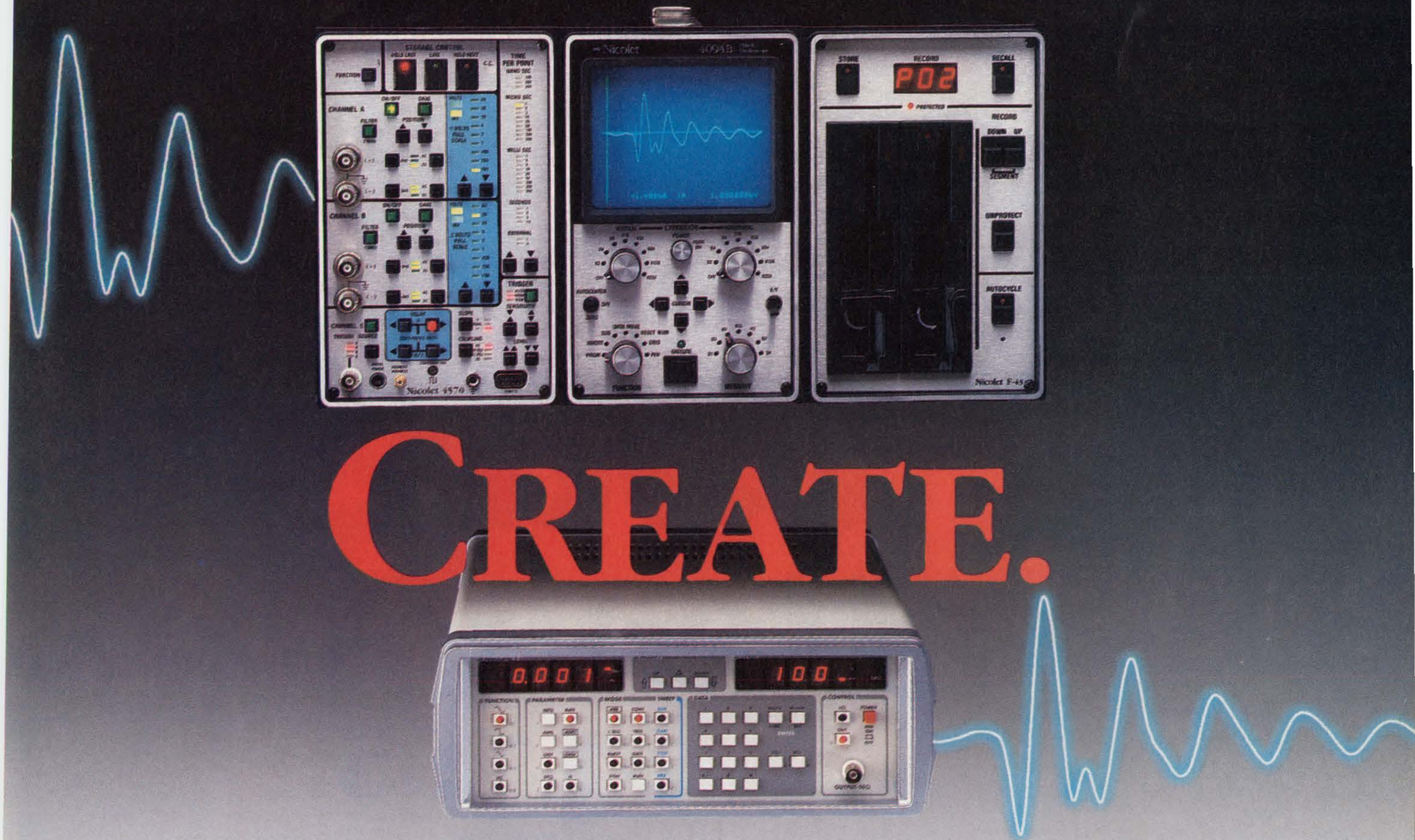
An expansion bus connector allows you to add as many as three daughter boards for additional serial I/O and RAM, a SCSI-bus interface, or for prototyping purposes. The board's VME Bus base address is software defined by data in nonvolatile RAM, and other board set-up parameters are stored in a PAL. The computer starts at £2950.

—Peter Harold

JOINT VENTURE TO OFFER ON-LINE SEMICONDUCTOR INFORMATION

A 10-company venture will offer next year an on-line information service on foreign and Japanese semiconductors and electronics components. Among the companies involved in this venture are Nippon Telegraph and Telephone Corp, Mitsubishi Corp, Hitachi, Toshiba, Fujitsu, and Oki Electric. Users will be able to access the database via PCs or facsimiles to obtain device specifications, photos, and circuit diagrams. When this service first begins, the database is expected to contain information on 15,000 catalogued items; after five years, the companies expect to have information on 900,000 devices.—Joan Morrow

CAPTURE.



CREATE.

Stimulate experiments with real-time analog waveforms reproduced from your actual captured data!

Connected via the GPIB interface, the Nicolet Model 4094 digital oscilloscope teamed up with the Nicolet Model 42 arbitrary function generator provides instantaneous waveform storage and generation.

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or 608/273-5008

Nicolet Digital Oscilloscopes

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NEW!

Outgoing signals are accurately generated from the 12-bit by 2k arbitrary waveform memory in the Model 42. Real-time duplication of the captured signal can be produced at speeds up to 1 μSec per data point.

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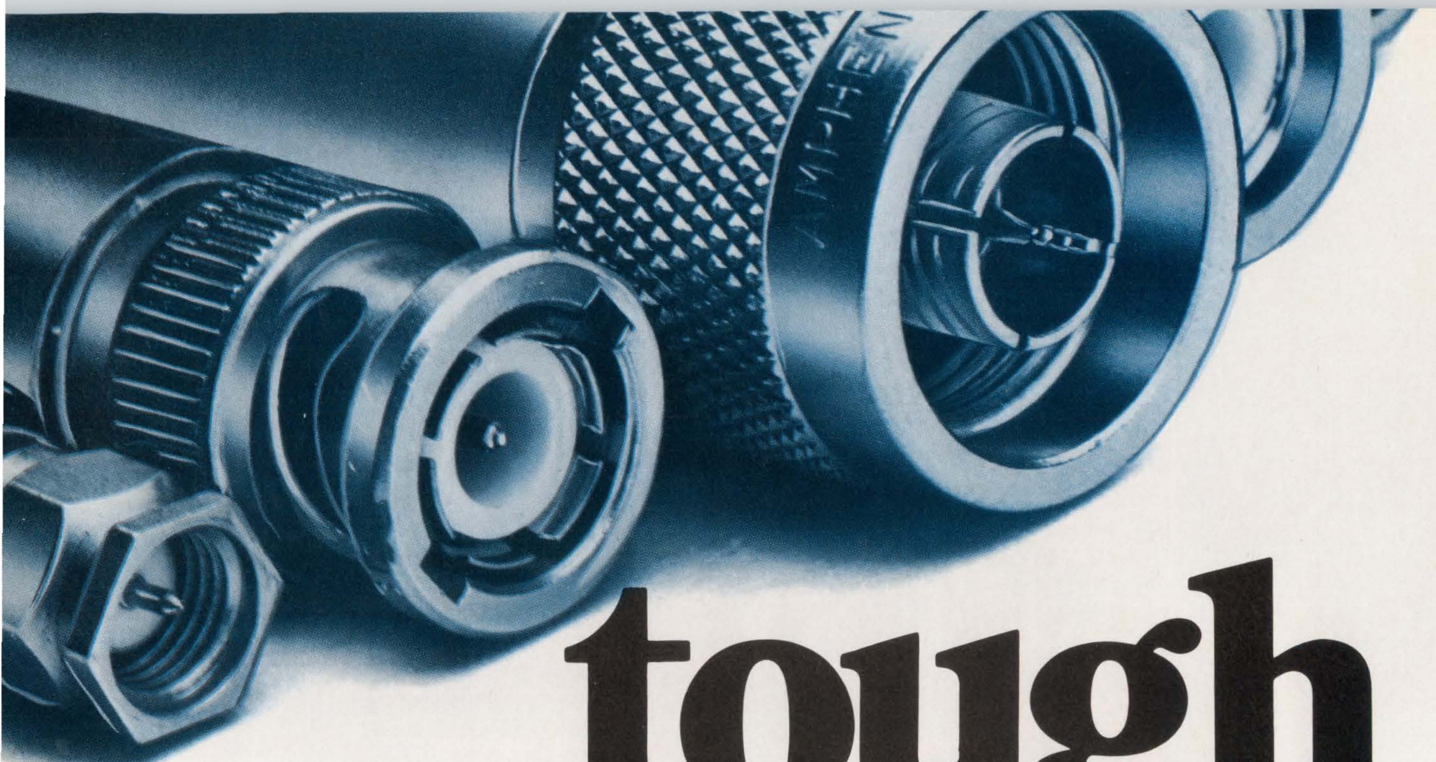

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one-piece design defies rough handling

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- ✓ BNC, SMA, N and TNC models
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SMA (model STRM-50), N (model NTRM-50)

*Freq. (MHz)	Atten. Tol. (Typ.)	Atten. Change, (Typ.) over Freq. Range		VSWR (Max.)	
		DC–1000	1000–1500	DC–1000 MHz	1000–1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC–1000 MHz (all 75 ohm or 30 dB models)   DC-500 MHz (all 40 dB models)

MODEL AVAILABILITY
Model no. = a series suffix and dash number of attenuation.
Example: CAT-3 is CAT series, 3 dB attenuation.
■ denotes 75 ohms; add −75 to model no.
● denotes 50 ohms

ATTEN	SAT (SMA)	CAT (BNC)	NAT (N)	TAT (TNC)
1	●	●	●	●
2	●	●	●	●
3	●	●■	●	●
4	●	●	●	●
5	●	●	●	●
6	●	●■	●	●
7	●	●	●	●
8	●	●	●	●
9	●	●	●	●
10	●	●■	●	●
12	●	●	●	●
15	●	●■	●	●
20	●	●■	●	●
30	●	●	●	●
40	●	●	●	●

PRICING (1-49 qty.): CAT (BNC)..$11.95, SAT (SMA)..$14.95
TAT (TNC)..$12.95, NAT (N)..$15.95

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C 92 REV. B

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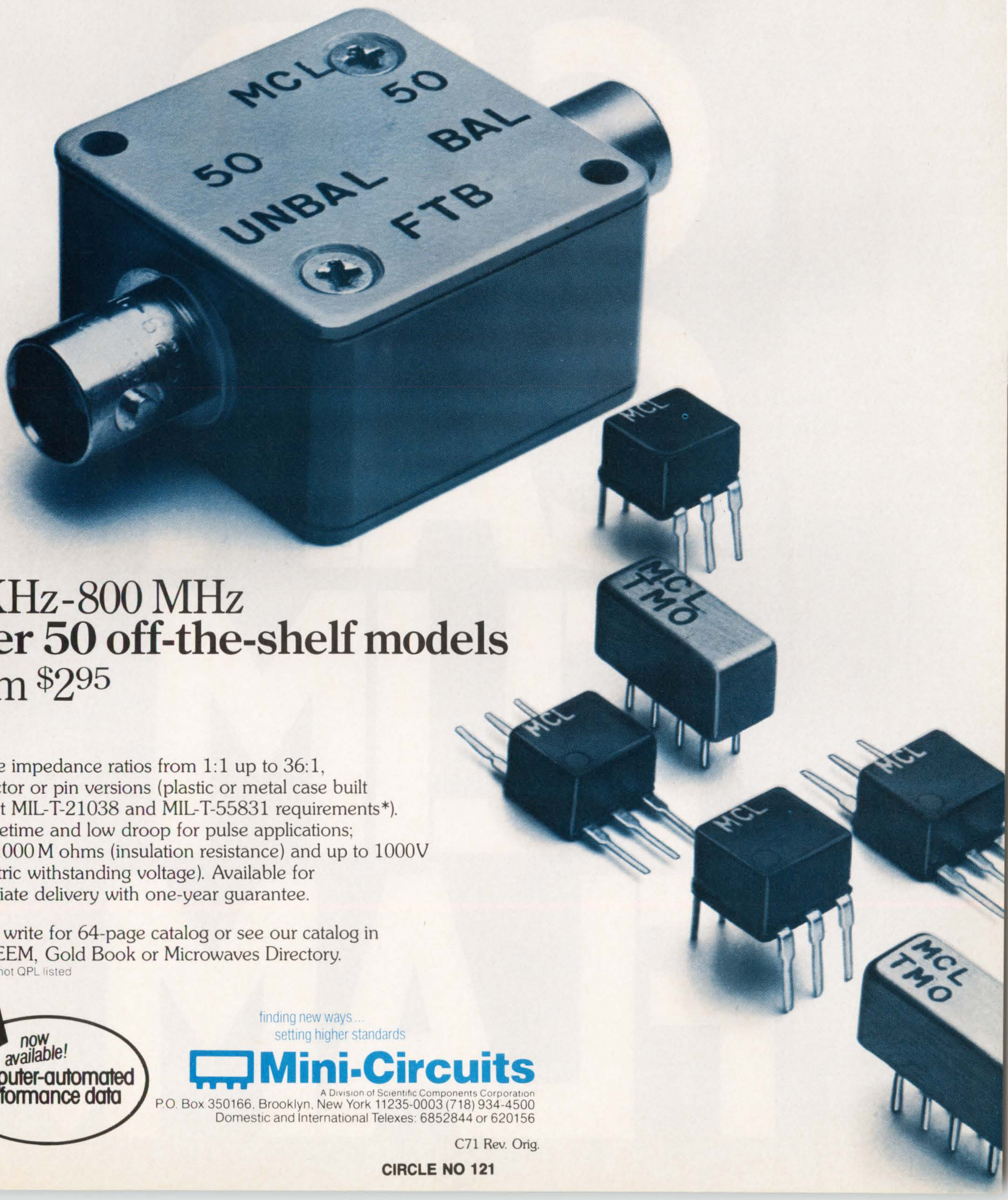

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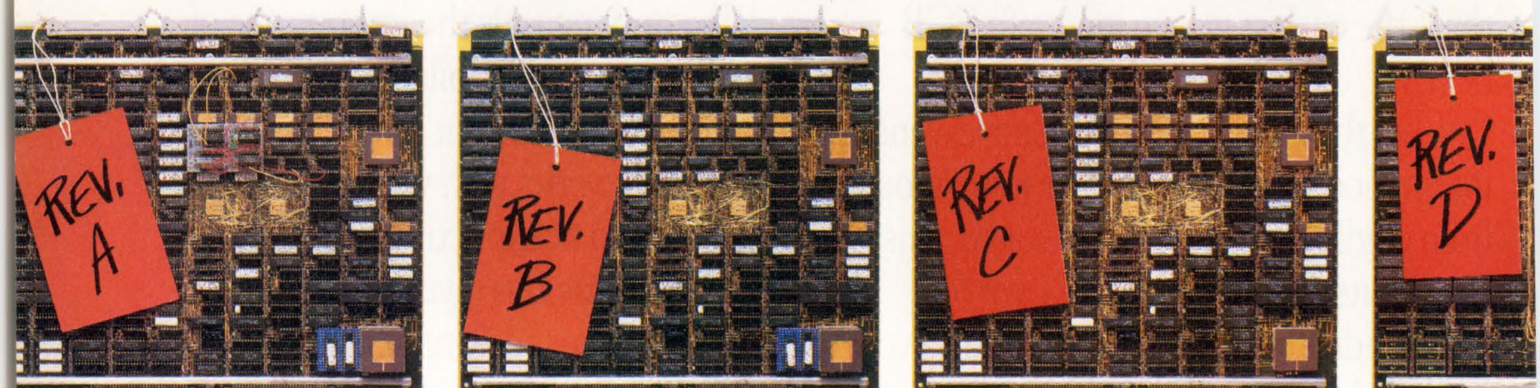

Teradyne's new CAE tools help you get to market faster by

Designing VLSI circuit boards that work the first time isn't child's play. You can't do it without fast, accurate feedback on design and test quality.

Now count on Teradyne to help. With our new family of CAE products, you'll uncover flaws before they're cast in hardware. So you'll be able to jump from initial design directly to final prototype. And from design to manufacturing test.

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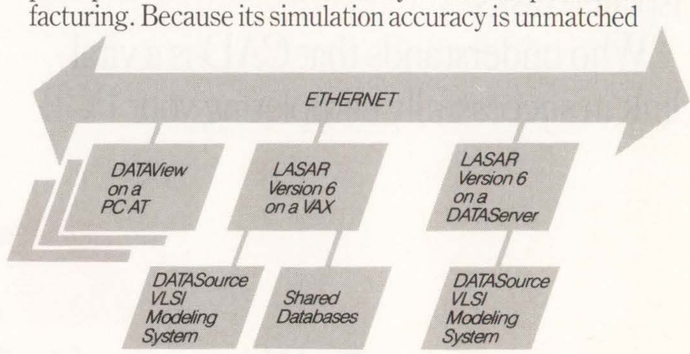
The process starts with DATAView our new design entry system. Running it on a standard AT-class PC, you can control the whole design process right at your desk. From schematic entry and waveform analysis on the PC to simulation and fault simulation on more powerful networked computers. All with the same mouse-and-menus, multiple-window interface.

You move from schematic capture to simulation effortlessly. DATAView's links with our LASAR Version 6 simulation system save hours of model compilation time. Incremental compiling lets you revise a design and resimulate in minutes.

Make your design work together before it comes together.

LASAR Version 6 is the only sure way to avoid multiple trips to artwork as well as costly rework steps in manufacturing. Because its simulation accuracy is unmatched



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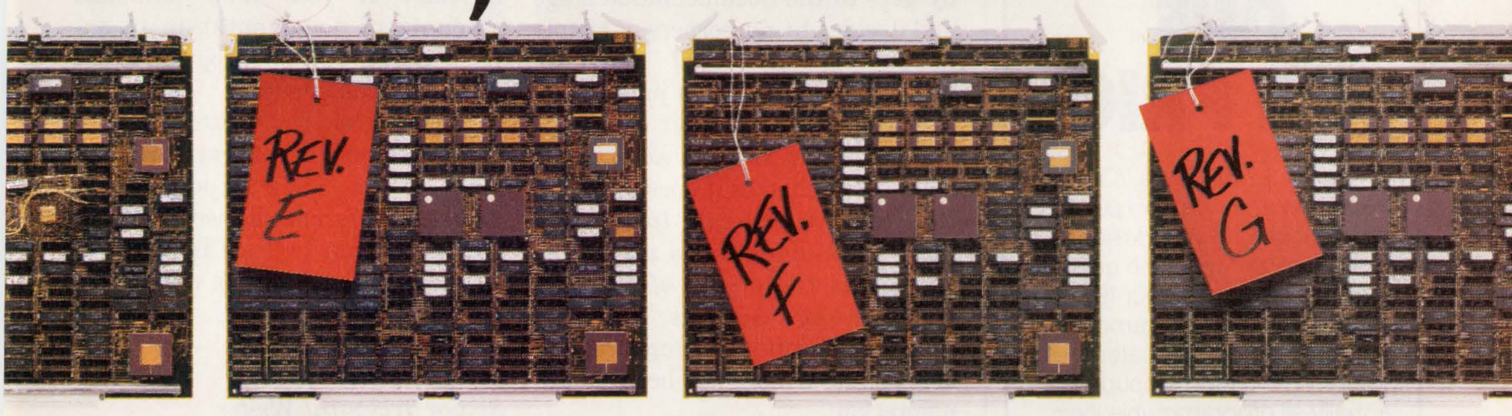

giving you a working prototype the first time.

for analyzing PC board designs prior to prototyping. For instance, LASAR takes full device timing specifications into account for true worst-case timing analysis. And it eliminates shared timing ambiguity in reconverging signals. Both of which mean LASAR finds real design errors reliably.

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For new VLSI parts, our DATASource hardware modeling system uses actual devices instead of software models. A single system supports multiple users and concurrent fault simulation. With extraordinarily fast response.

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If you want to avoid multiple prototypes and get to market faster with better products, Teradyne's new CAE system is the way. Why not call Daryl Layzer at (617) 482-2700, ext. 2808 for more information. Or write Teradyne, 321 Harrison Avenue, Boston, MA 02118.

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SIGNALS & NOISE

Technical writers aid software-design teams

Dear Editor:

In reference to the article "Expert designers evaluate pc-based schematic editors" (EDN, December 25, 1986, pg 82), I would like to say a few words in behalf of my profession. I designed and wrote the Dash-4C manuals; it was a real boost to see that Gary Strunc appreciated the soul-searching and agonizing I went through to produce what I felt was the best documentation possible.

In defense of my fellow technical writers in CAE, let me suggest that poor documentation is often the result of not using a technical writer to produce manuals. Often a company gets to the documentation stage and decides to cut corners or simply misunderstands what technical writers do ("We have a junior engineer here; we'll have her write it").

It takes just as much expertise to design a manual as it does to design the software package. In fact, the difficulty in designing a manual increases as the design of the software package worsens. A system that is not intuitively understandable requires more and better documentation.

As for understanding the needs of the engineer or designer, I personally am not an engineer. In fact, FutureNet was my first contact with electronics, engineers, and PCs: I came from a programmer-productivity-tool, IBM-mainframe background. However, I understand how people learn and think and remember, and I know that they don't all do it the same way. Unfortunately, the same can't be said for all the *engineers* who are designing software packages.

An electronic engineer designing software for other EEs is less likely to be concerned with writing intuitively understandable packages than, say, a software programmer would be. The engineer is more likely to say, "Well, I'm an EE and I understand it; if the user doesn't, he should find another job," forgetting that although he or she is computer oriented, the user may not be. FutureNet has discovered this fact, and to its credit, the company now spends huge amounts of development time in prototyping user interfaces to be sure that the final product is intuitively understandable, or user friendly.

As a technical writer, I feel that some of my best work is not what the user sees in the manual, but the contributions I make during product design. I serve as a user advocate, insisting on consistency and pushing for what's easiest for the user, even if it's harder for the programmer. My general rule of thumb is this: If you need immense amounts of documentation to explain a program, the program is not designed well enough.

In sum, technical writers are valuable members of software-development teams. Their expertise can make the difference between a package that is easy to learn and use and a package that wastes the user's time and gets returned.

Sincerely yours,
Pam Kayoumy
Senior Technical Writer
EEsof Inc
Westlake Village, CA

Chip implements RSA algorithm

Dear Editor:

The Technology Update article entitled, "Availability of cryptographic ICs augurs the increasing use of data encryption" (EDN, January 22, pg 63), incorrectly stated that "it would be very expensive (and perhaps impossible, at present) to implement [the RSA algorithm] in hardware."

In fact, our chip, the CY1024 cryptographic IC, does implement the RSA algorithm in hardware. The chip performs the computations

Text continued on pg 36

DIGITIZING

1 1 GHz. The 11402 Digitizing Oscilloscope features a full 1 GHz bandwidth right on the probe tip to help you make the most demanding voltage and timing measurements.

2 10-14 BIT VERTICAL/ 10 ps HORIZONTAL RESOLUTION. 10-bit vertical resolution is averageable to 14 bits. Self-calibration decreases error to less than 1% DC.

3 AUTOMATIC MEASUREMENTS. Up to six measurements can be made at the push of a button, with results simultaneously displayed and continuously updated.

4 PUSH-BUTTON HARD COPY. Plug in a Tek or compatible Epson dot matrix printer using the scopes' standard Centronics port.

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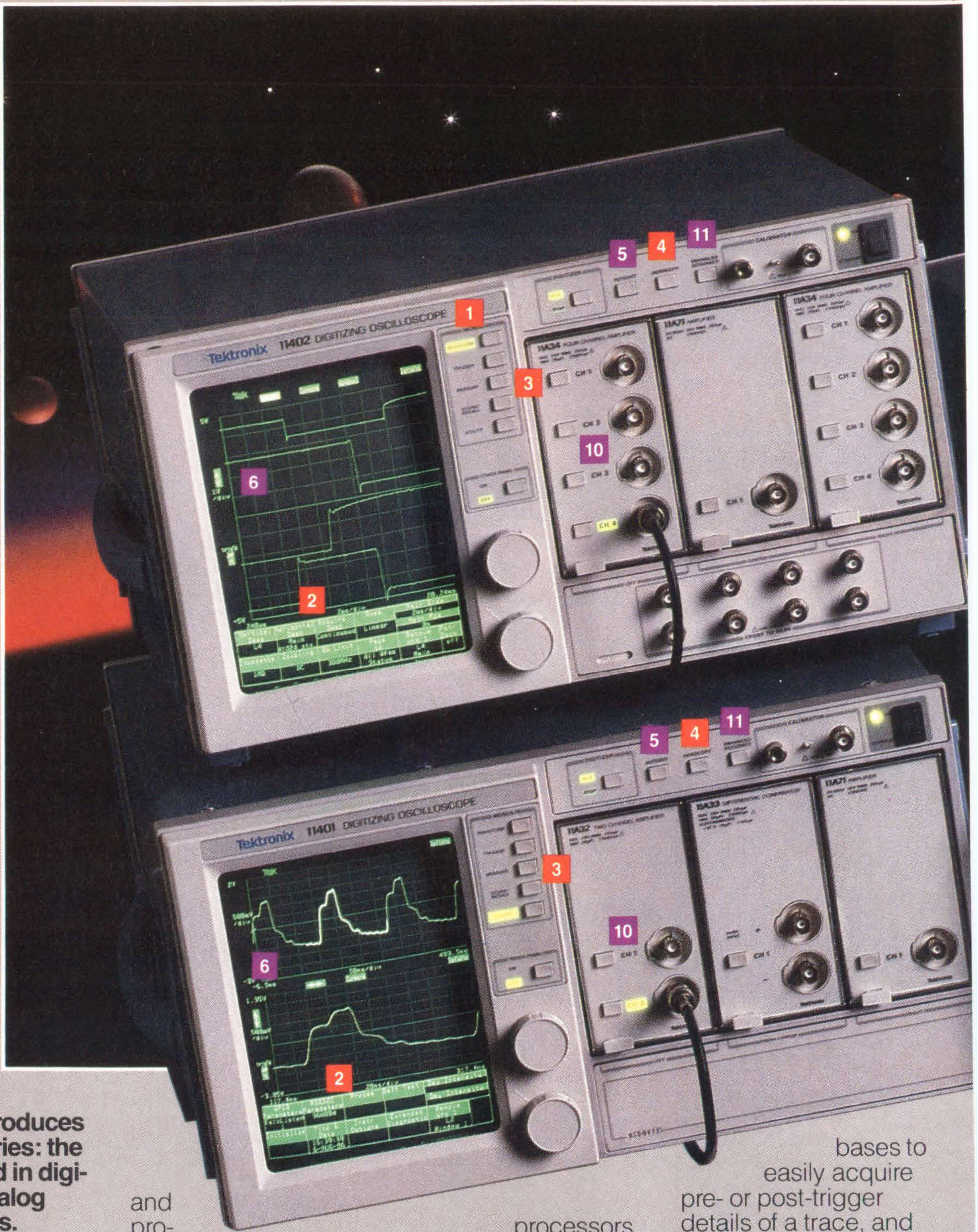
5 AUTOSET. Push a button on the front panel or on the probe to automatically set up the scope based on the signal characteristics of the selected trace.

6 TOUCH SCREEN. Select a trace, a trigger, a measurement or other function by touching the appropriate area of the screen or by selecting from pop-up menus: the closest, most natural link yet between user and scope.



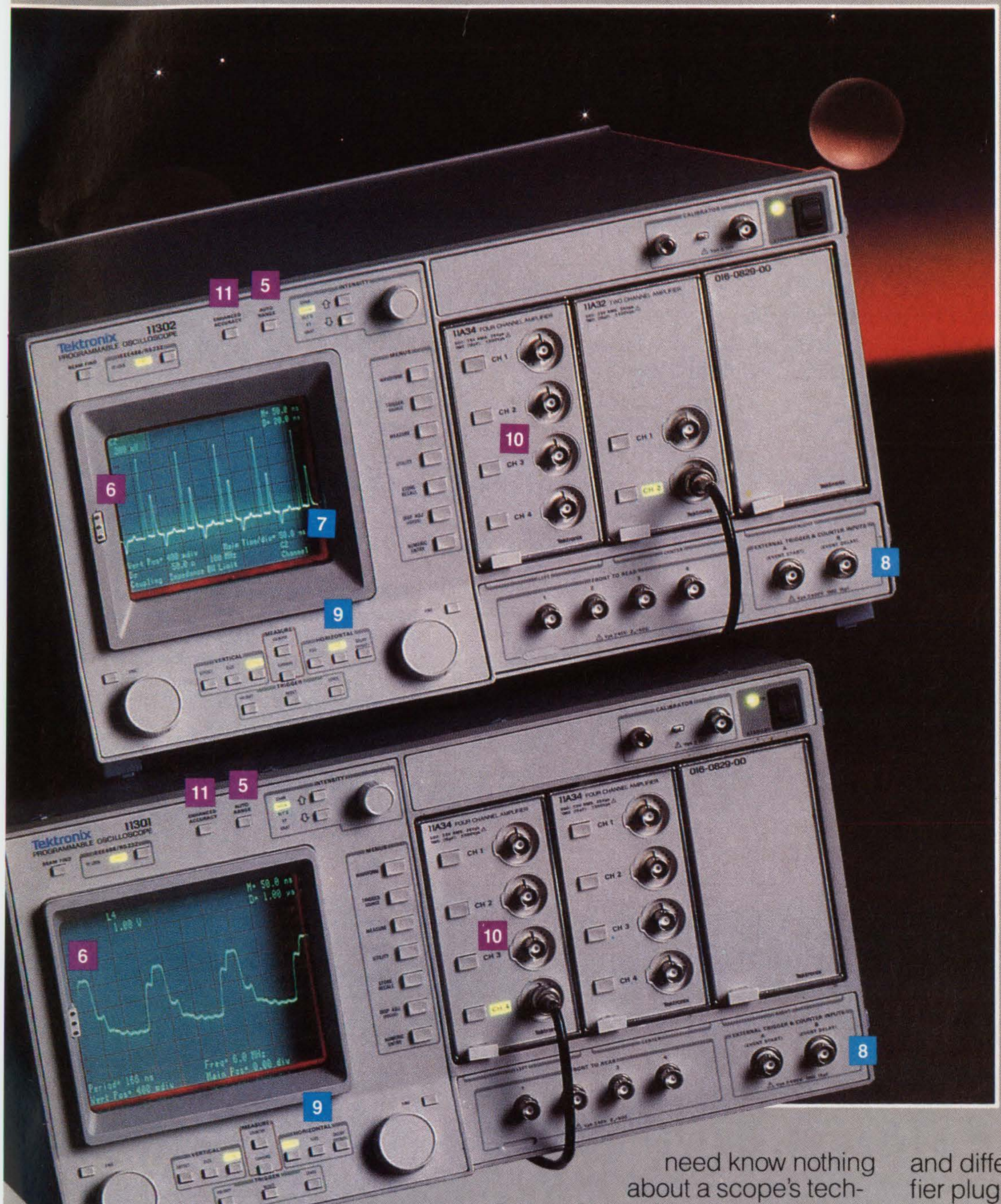
Tektronix introduces the 11000 Series: the new standard in digitizing and analog oscilloscopes.

These new fully programmable scopes display more traces (up to 8) at higher bandwidths (up to 1 GHz), with greater accuracy (up to 0.6% vertical), and include more new functions for expediting the capture and processing of data than can ever be listed here.

Two new digitizing scopes exert the power of three 16-bit processors, long records, the most powerful triggering and the highest throughput ever. Use their built-in dual timebases to easily acquire pre- or post-trigger details of a trace, and view both the whole trace and the details on screen at once.

Two analog scopes feature an integrated 500 MHz universal counter/timer for unequaled resolution, accuracy, and scope versatility — for the

THE NEW ERA IN DIGITIZING AND ANALOG OSCILLOSCOPES.



ANALOG

7 MICROCHANNEL PLATE. The single shot trace brightness of the Tek 11302 is almost 1000 times brighter than conventional scopes—enough to expose even the fastest transients to view.

8 500 MHz INTEGRATED COUNTER/TIMER. Use with dual delayed sweeps for precise timing measurements between selected points. Unique counter view trace lets you see exactly what you are triggering on.

9 CURSORS. Use to make precise measurements on any part of a displayed waveform.

10 1 mV/DIV SENSITIVITY. Achievable from four new plug-ins. These amplifiers feature fast overdrive recovery and wide dynamic range.

11 SELF-CALIBRATION. Push the Enhanced Accuracy button to calibrate the scope from amplifier input to CRT graticule, automatically, for the best vertical accuracy available in a scope today.

price of a scope alone. A unique counter view trace lets you see exactly what you are triggering on, for a sense of confidence no conventional counter/timer can offer.

Perhaps most startling is the simplification and automation of the whole measurement and analysis process. Larger displays, pop-up and touch-screen menus, plus automated setup and measurement capabilities help unclutter the front panel and keep eyes focused on the display. For the first time, users need know nothing about a scope's technology to get the most out of it.

The 11000 Series continues the plug-in versatility of the Tek 7000 Series. Five new plug-ins and three new probes tailor the new scopes to a full range of applications, from design and debug to production test. New single-ended amplifier and differential amplifier plug-ins combine high bandwidth with low noise and fast overdrive recovery.

Demonstrations are now in progress. For more information or a personal demonstration, get in touch with your local Tek sales engineer. Or call Tektronix at 1-800-547-1512.

Tektronix
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CIRCLE NO 87

necessary for SEEK, RSA, or Diffie-Hellman algorithms on numbers considerably larger than the 200-digit numbers cited in the article. The chip operates on numbers over 1000 bits, computes in less than 1 second, and costs less than $100 in OEM quantity.

Sincerely yours,
Lewis C Morris
President/CEO
Cylink Corp
Sunnyvale, CA

Corrected formula

Dear Editor:

EDN's January 8 issue contains an informative and interesting article by R F Cobb: "Use statistics to test communications systems efficiently" (pg 143). The approximations for Q(X) and Q(Y) are of particular interest to me because they are also widely useful outside the context of the article. Unfortunately, Mr Cobb presents an incorrect solution for Q(X) where X is negative (pg 147). This is evident when you inspect the formula for T, where, if X is set equal to $-1/p$, the value of T would be infinite.

Instead, for all values of X, the correct value of T is:

$$T = \frac{1}{1 + p\,|X|}.$$

Thank you for presenting articles such as Mr Cobb's. They attack important problems in ways that can be extended to many other applications. Mr Cobb, in particular, has provided helpful insight in many areas, not only in the present article but in the 4-part FFT series EDN published in 1984 (March 8, 1984, pg 209; April 5, 1984, pg 237; May 3, 1984, pg 265; and June 14, 1984, pg 183). Keep up the excellent work!

Sincerely yours,
David King
Manager, Advanced Programs
TRW Microwave Inc
Sunnyvale, CA

Please dial again

EDN's March 18 Product Update on Micro Linear's (San Jose, CA) ML2200 chip (pg 104) contained an incorrect phone number for the company. The correct number is (408) 262-5200.

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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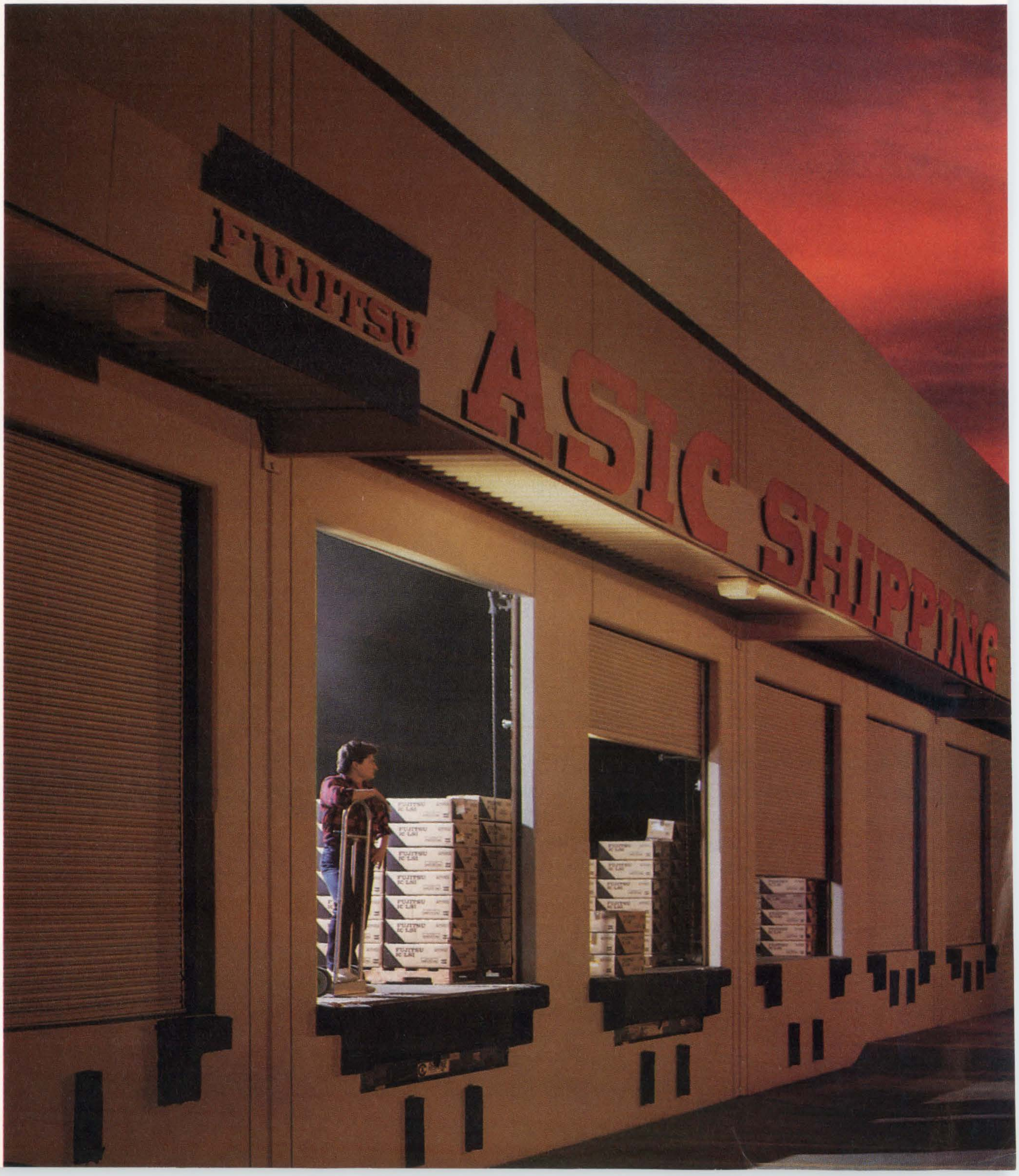
When you put a Fujitsu ASIC to work, you can rest assured it will work the way it should. And keep on doing its job for a very long time to come. In fact, when you look at our performance record over the years, you'll be hard pressed to find any field failures at all.

This is no empty promise. Product reliability has been a way of life for us for more than 15 years.



That's why we always take a conservative approach to the design process. Giving you realistic worst case specs that no production device will exceed.

Guaranteeing a minimum 90% utilization of all gates. And giving you a simulation-to-production correlation of 99%.

It's also why we control every step of the production process. From design to wafer fab to assembly and final test, including 100% AC testing at frequency. So nothing is left to chance.

To us, reliability in the field is everything. And when you remember we've taken over 8,000 ASIC devices from design through mass production, you can see that we'll give you a level of confidence no one else can offer.

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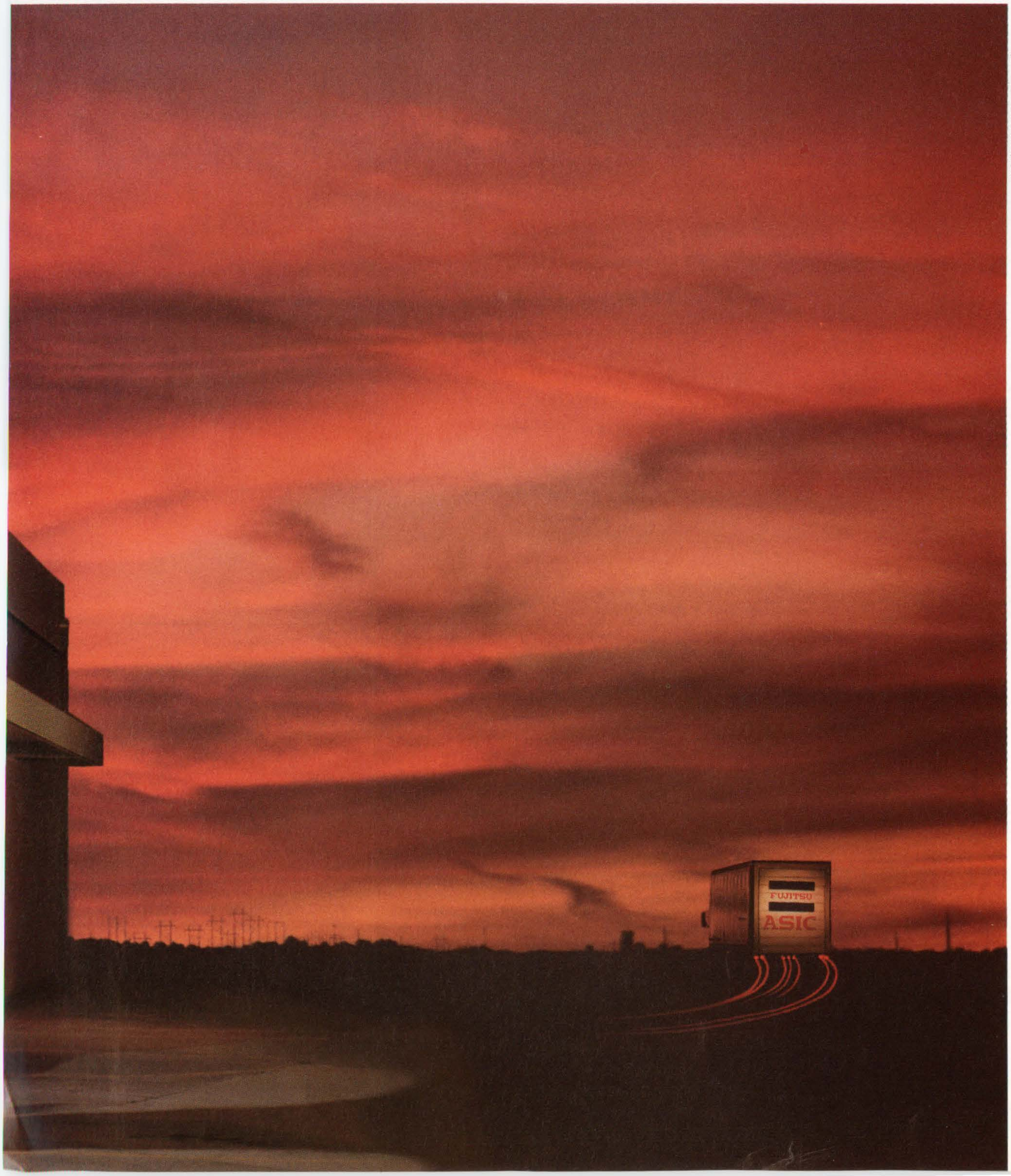

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		serial	disk	graphics
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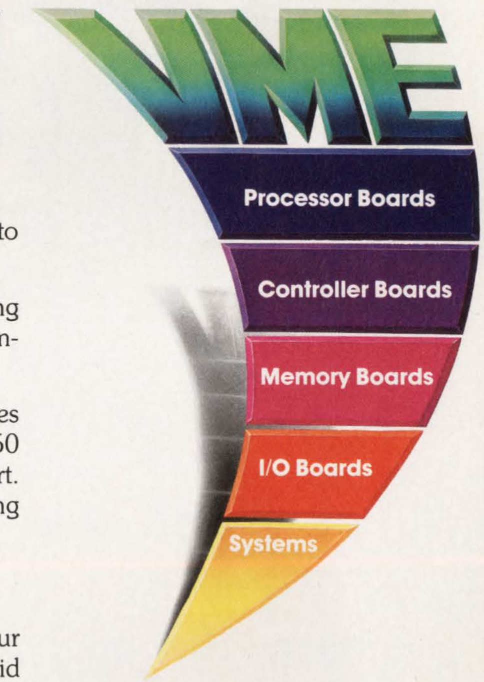
Hardware	Processor	68010/10 MHz	68010/10 MHz	63484/8 MHz
Hardware	Dual ported memory	128/512K no wait state	128/512K no wait state	2 MB no wait state
Hardware	Interface	8 x RS232/RS422	SCSI/SA 460	RS434 (RGB)
Hardware	Speed	RS232 : 38400 baud RS422 : 2 M baud	1.5 Mbit/sec	64 MHz pixel frequency 1600 x 1280 pixels
Software	Driver support	PDOS*, UNIX* V	PDOS*, UNIX* V	PDOS*, UNIX* V
Software	Unique SW packages	firmware based on real time kernel	hashing and caching firmware	GKS 2. 0b
	Availability	now	now	now

Whatever your VME need – CPUs, memories, controllers, software – FORCE has it. Each product comes with a 500 + page user's manual and with FORCE's proven quality and reliability.

intelligence



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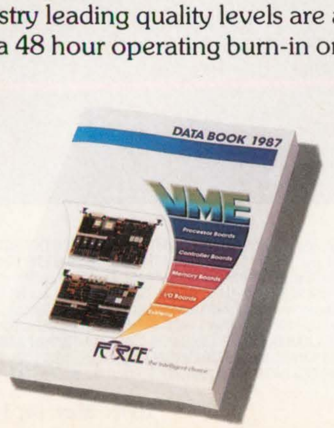

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CIRCLE NO 92

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We are the world leader in CMOS and NMOS static RAMs, in 16K, 64K and 256K byte wide memory products. We make the fastest 2K x 8 at 35 ns and also a 4K x 4 static RAM at 35 ns. We pioneered the 8K x 8 CMOS static RAM and are now offering a 64K x 1 (55 ns) and 32K x 8 CMOS static RAM.

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So you can see that we have the capability to supply the memory products you want—when you want them.

That's memory power; that's Toshiba.

TOSHIBA MEMORY PRODUCT SUMMARY

PART NO.	ORG.	PROCESS	SAMPLES	PROD.	SPEED SORTS AVAILABLE (ns)				PACKAGE OPTIONS
DYNAMIC RAMS									
TMM4164AP	64KX1	NMOS	YES	YES	150	200			P
TMM41256P	256KX1	NMOS	YES	YES	120	150			P/T
TMM41257P	256KX1	NMOS	YES	YES	120	150			P/T
TMM41464P	64KX4	NMOS	YES	YES	120	150			P
TC511000P/J	1MbX1	CMOS	YES	2Q'86	100	120			P/J
TC511001P/J	1MbX1	CMOS	YES	2Q'86	100	120			P/J
TC511002P/J	1MbX1	CMOS	YES	2Q'86	100	120			P/J
TC514256P/J	256KX4	CMOS	YES	2Q'86	100	120			P/J
TC514258P/J	256KX4	CMOS	YES	2Q'86	100	120			P/J
STATIC RAMS									
TMM2114AP	1KX4	NMOS	YES	YES	120	150			P
TMM2016AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2016BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2064P	8KX8	NMOS	YES	YES	100	120	150		P
TMM2063P	8KX8	NMOS	YES	YES	100	120	150		P
TC5504AP	4KX1	CMOS	YES	YES	200	300			P
TC5514AP	1KX4	CMOS	YES	YES	200	300			P
TC5516/17AP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18BP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18CP	2KX8	CMOS	YES	YES	150	200			PFY
TC5565P	8KX8	*CMOS	YES	YES	120	150			PFY
TC5565AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5563AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5564P	8KX8	CMOS	YES	YES	150	200			PY
TC55257P	32KX8	*CMOS	YES	YES	100	120	150		P
HIGH SPEED STATIC RAMS									
TMM2018D	2KX8	NMOS	YES	YES	35	45	55		D
TMM2068D	4KX4	NMOS	YES	YES	35	45	55		D
TMM2078D	4KX4	NMOS	YES	YES	35	45	55		D
TC5561P	64KX1	*CMOS	YES	YES	70				P
TC5562P	64KX1	*CMOS	YES	YES	45	55			P
EPROMS									
TMM2764D	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764DI	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764AD	8KX8	NMOS	YES	YES	150	200			D
TMM27128D	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128DI	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128AD	16KX8	NMOS	YES	YES	150	200			D
TMM27256D	32KX8	NMOS	YES	YES	150	200			D
TMM27256DI	32KX8	NMOS	YES	YES	150	200			D
TMM27256AD	32KX8	NMOS	YES	YES	150	200			D
TC57256D	32KX8	CMOS	YES	YES		200	250		D
TMM27512D	64KX8	NMOS	YES	YES		200	250		D
ONE TIME PROGRAMMABLES									
TMM2464AP	8KX8	NMOS	YES	YES	200				PF
TMM24128AP	16KX8	NMOS	YES	YES	200				PF
TMM24256AP	32KX8	NMOS	YES	YES	200				PF
TMM24512P	64KX8	NMOS	2Q'86	2Q'86	250				PF
MASK ROMS									
TC5364/5/6P	8KX8	CMOS	YES	YES	250				P28
TMM23256P	32KX8	NMOS	YES	YES	150				P28
TC53257P	32KX8	CMOS	YES	YES	200				FP28
TC53512P	64KX8	CMOS	YES	2Q'86	200				P28
TC531000P	128KX8	CMOS	YES	YES	200				P28
TC532000P	256KX8	CMOS	YES	2Q'86	200				P32

P-PLASTIC C-CERAMIC F-FLAT PACK D-CERDIP Y-DIE T-PLCC J-SOJ
*CMOS = 4 TRANSISTOR CELL LOW POWER

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CIRCLE NO 93

CALENDAR

Colorado Innovations in Electronics Trade Show, Denver, CO. CIETS Office, 9778 E Ida Circle, Englewood, CO 80111. (303) 771-9578. May 20 to 21.

41st Annual Frequency Control Symposium, Philadelphia, PA. Synergistic Management, Box 826, Belmar, NJ 07719. (201) 280-0410. May 27 to 29.

International Workshop on Computer-Aided Software Engineering, Cambridge, MA. Index Technology Corp, 101 Main St, Cambridge, MA 02142. (617) 491-2100, ext 8000. May 27 to 29.

Personal Computer Interfacing for Scientific Instrument Automation, Blacksburg, VA. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. May 28 to 30.

Comdex/Spring, Atlanta, GA. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 1 to 4.

Hands-On Programming in C, Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. June 2 to 5.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Arlington, TX. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239. June 2 to 5.

ICCE (International Conference on Consumer Electronics), Rosemont, IL. Geriann Van Calbergh, First National Bank of Chicago, 8528 W Gregory St, Chicago, IL 60656. (312) 399-1653. June 3 to 5.

ISHM Europe (European Microelectronics Conference and Exhibition), Bournemouth, UK. Concorde Services, 10 Wendell Rd, London W12 9RT UK. 01-743-3106. June 3 to 5.

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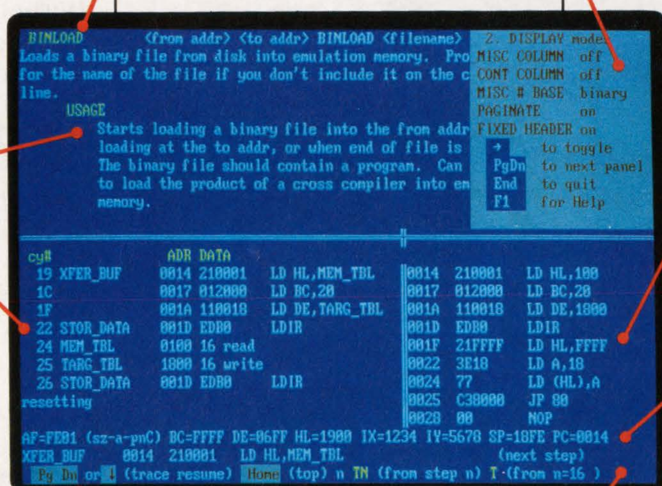
Context sensitive prompt line.



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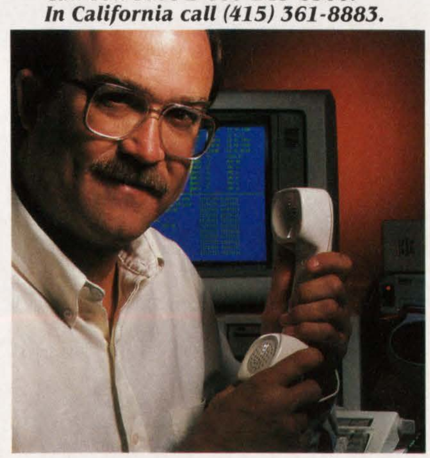

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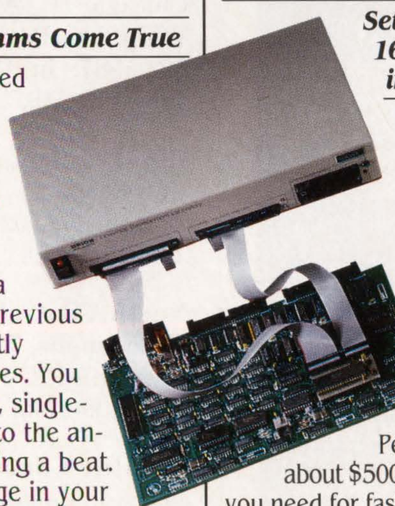

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CALENDAR

Single-Chip DSP Processors and VLSI Semicustom Architectures, Boston, MA. DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. June 8 to 9.

IEEE MTT-S International Microwave Symposium, Las Vegas, NV. Steven March, Symposium Steering Committee Chairman, Maury Microwave Corp, 8610 Helms Ave, Cucamonga, CA 91730. (714) 987-4715. June 9 to 11.

University / Government / Industry Microelectronics Symposium, Rochester, NY. Lynn Fuller, Rochester Institute of Technology, 1 Lomb Memorial Dr, Rochester, NY 14623. (716) 475-2035. June 9 to 11.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239. June 9 to 12.

Advanced Printed Circuit Board Design Techniques, Milwaukee, WI. Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N Sixth St, Milwaukee, WI 53203. (414) 227-3125. June 10 to 12.

National Computer Conference, Chicago, IL. AFIPS, 1899 Preston White Dr, Reston, VA 22091. (800) 622-1987; in VA, (703) 620-8955. June 15 to 18.

ISDN, Atlanta, GA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. June 15 to 19.

North Central Lightwave Expo, Minneapolis, MN. Lightwave, 235 Bear Hill Rd, Waltham, MA 02154. (617) 890-2700. June 16 to 18.

Satellite Communications (short course), Boston, MA. Continuing Education Institute, 21250 Califa St, Woodland Hills, CA 91367. (818) 710-1142. June 16 to 19.

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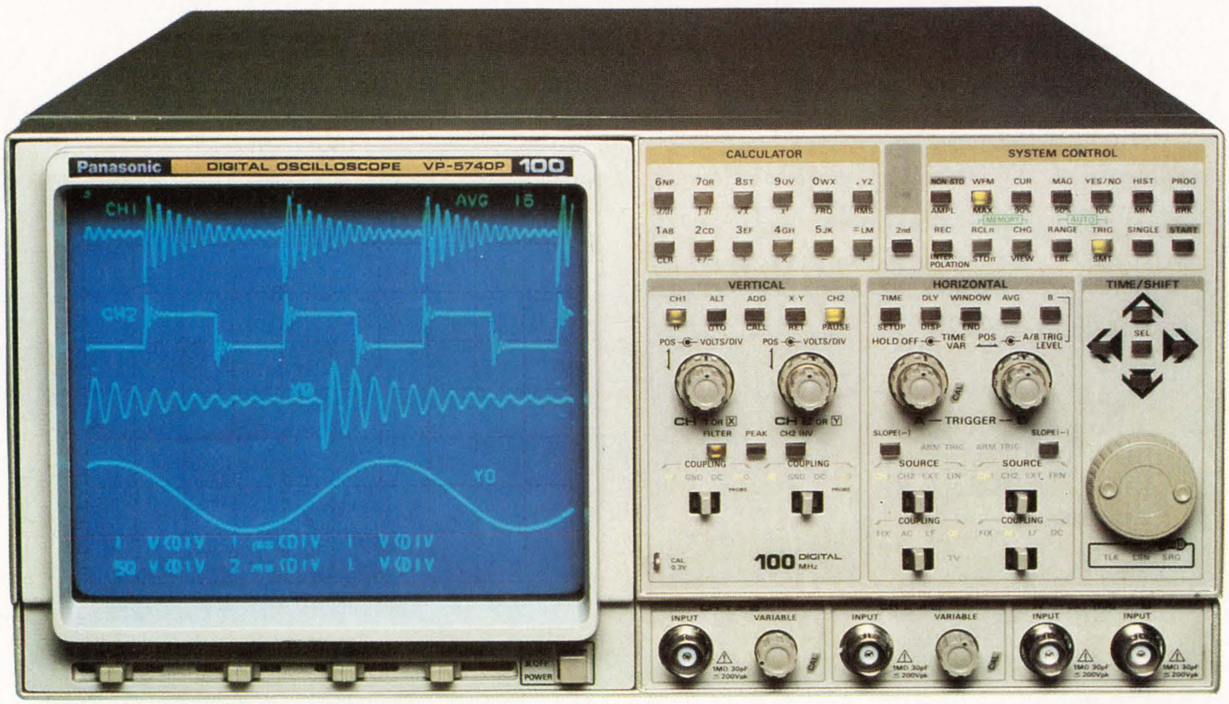

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- Future memory expandability

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CIRCLE NO 95

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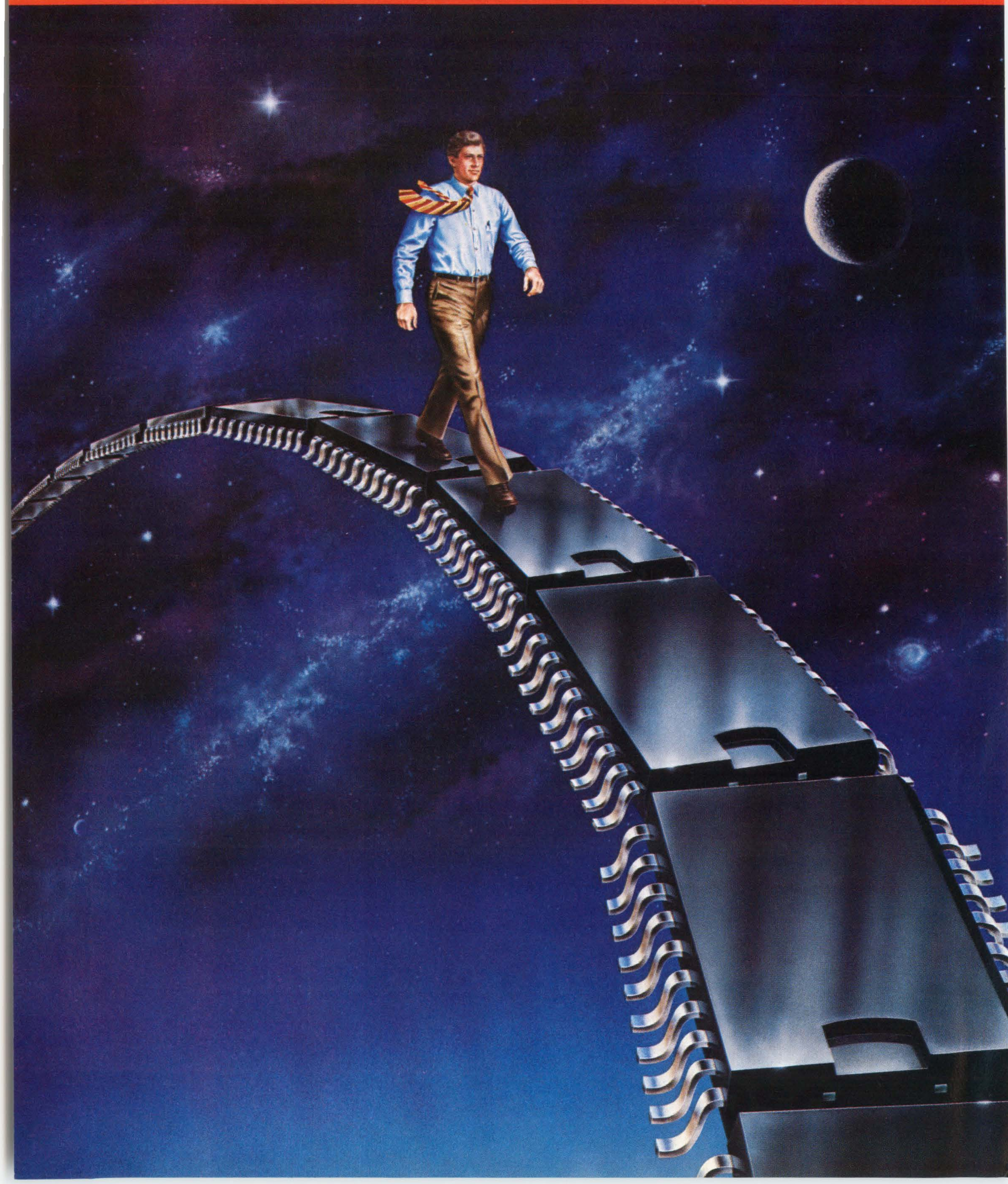

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- Built-in op amps for excellent linearity.
- Op-amp buffered demodulated output.
- A pin which indicates lock detect.
- 2 phase comparators to choose from.
- Applications: FM Modulation/Demodulation, Frequency Synthesis, Frequency Multiplexing, Voltage to Frequency/Frequency to Voltage Conversion, Servo Control Systems, Data Synchronization, Manchester Coding/Decoding.

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CIRCLE NO 97

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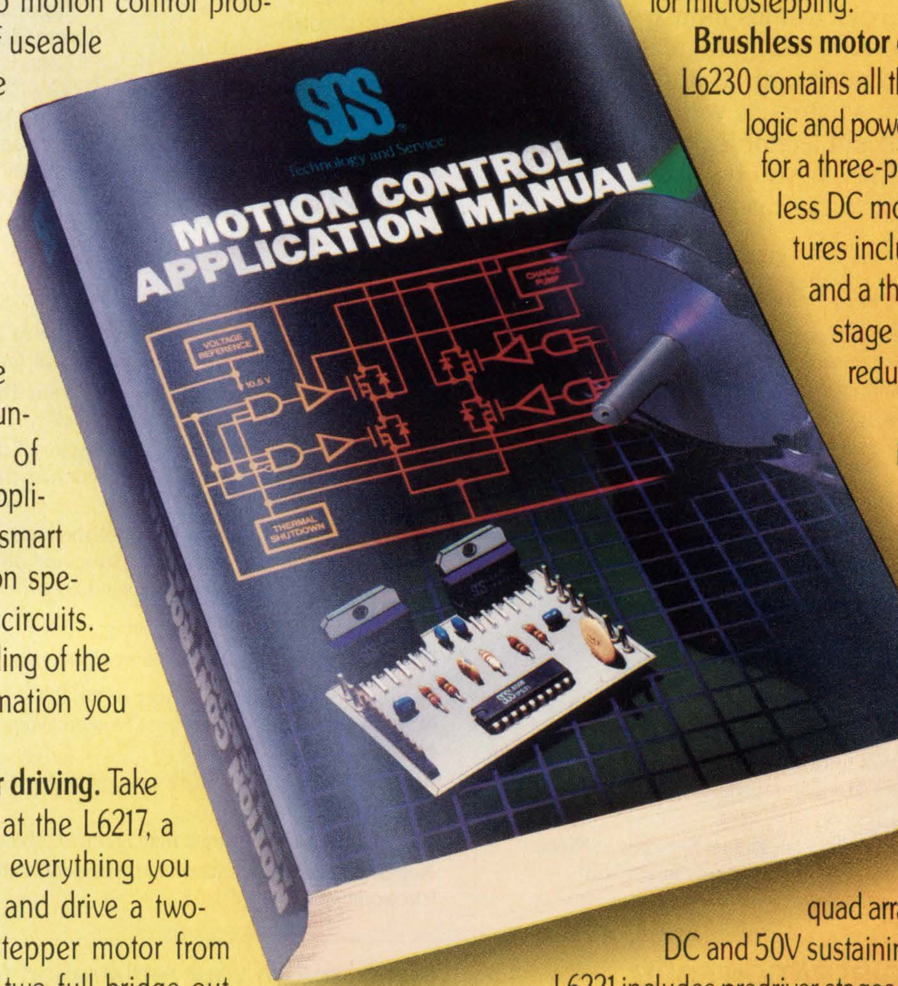

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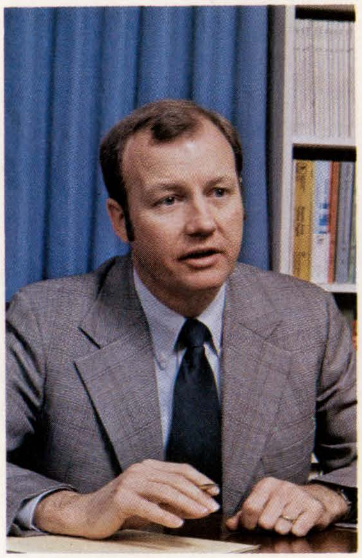
EDITORIAL

The hole-in-the-foot gang



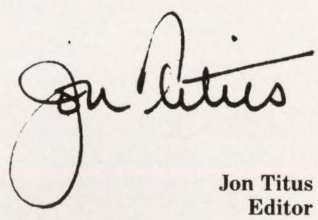
The US government is finally taking a firm stand on its Japanese trade imbalance, although it's shooting itself in the foot by doing so. Recently, Secretary of Commerce Malcolm Baldrige exerted Cabinet-level pressure that eventually crushed Fujitsu's purchase of Schlumberger's interest in Fairchild. Often overlooked in the aftermath of the aborted deal is one of Baldrige's explanations. It seems he didn't want Fujitsu to get into the US supercomputer market while Japan keeps American-made supercomputers out. Secretary Baldrige isn't alone in worrying about the market for US-built computers. Senator Howard Metzenbaum (D-OH) had similar concerns; the Fujitsu-Fairchild deal, he feared, would have let Fujitsu dominate the US supercomputer market.

Unfortunately, because we lack clear international trade goals and any plans to establish them, the US government goes out of its way to hand many supercomputer orders to competitors such as Fujitsu and NEC. For example, a White House export-control group vetoed the sale of a $20 million Cray Research 4-CPU supercomputer to India. India's Meteorological Center wants to duplicate a Cray computer system already used in Europe for weather research. The US will allow India to buy a scaled-down dual-processor version of the 4-CPU model. NEC, however, has also offered the Indians a dual-processor supercomputer, and the Japanese electronics giant has received from the Indian government a letter of intent to purchase another supercomputer system as well. And India isn't the only country that wants supercomputers.

The Commerce and Defense Departments are now arguing over whether or not to sell relatively old and obsolete technology to Iran. It appears the Iranians liked our TOW missiles so much that they have asked to buy our computers too. Specifically, they want DEC PDP 11/70, 11/84, and 11/73 computers for their electric-power authority and their press agency. The Commerce Department favors the sale, while the Defense Department opposes it. Look at it this way: If the sales deal stalls, the Japanese may dominate the world market for obsolete minicomputers. No comments yet from Baldrige or Metzenbaum.

As these events illustrate, trade policies are often inconsistent and diverge from current political and economic needs. Therefore, we must carefully and clearly redefine our international-trade goals so that we can apply them in a consistent manner. We can start by establishing a single committee that would identify inconsistencies in our policies and, after public debate, reorganize and administer those policies.

We need to get on with competitive international trade. It is senseless to divide the responsibility for major trade decisions among organizations that cannot resolve problems resulting from clashes between their parochial and conflicting policies.



Jon Titus
Editor

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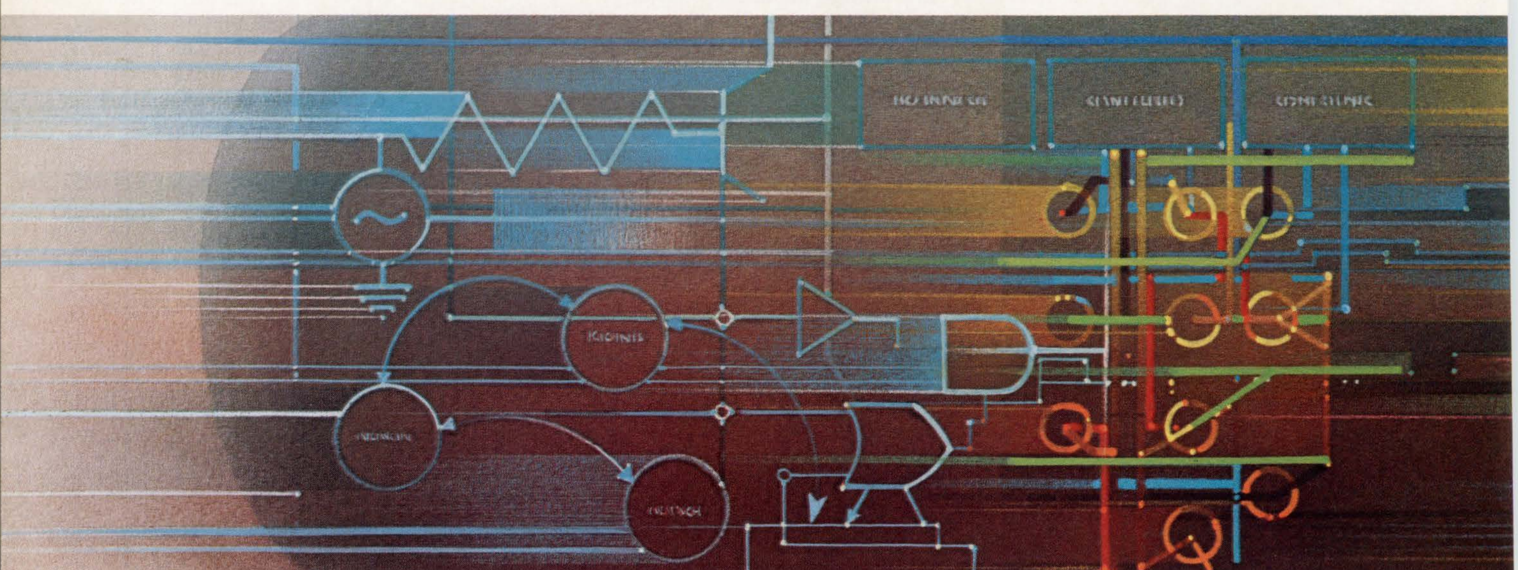

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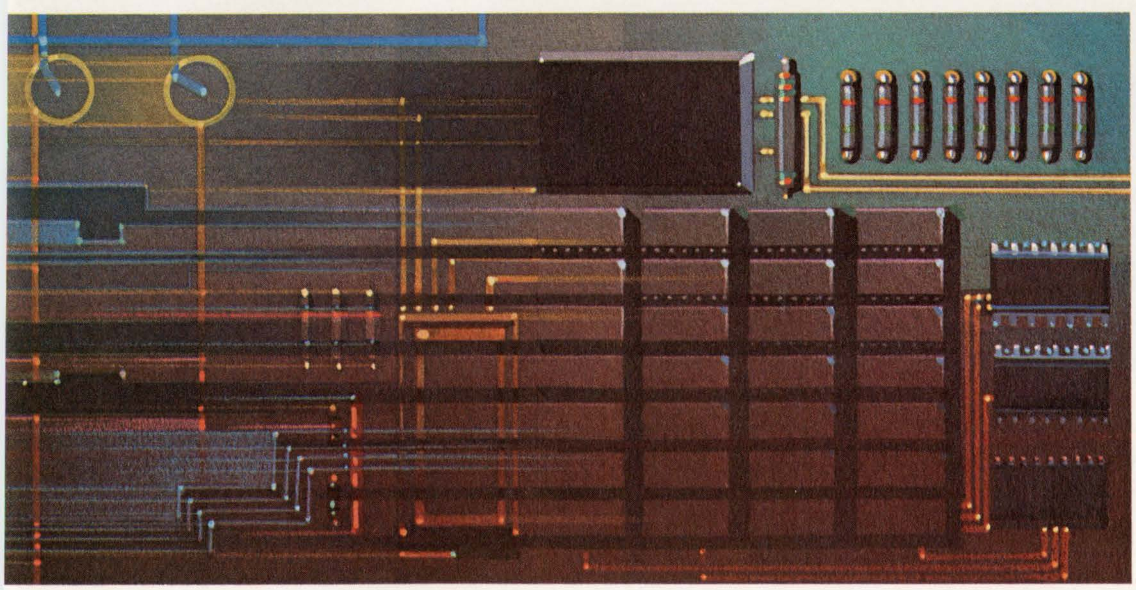

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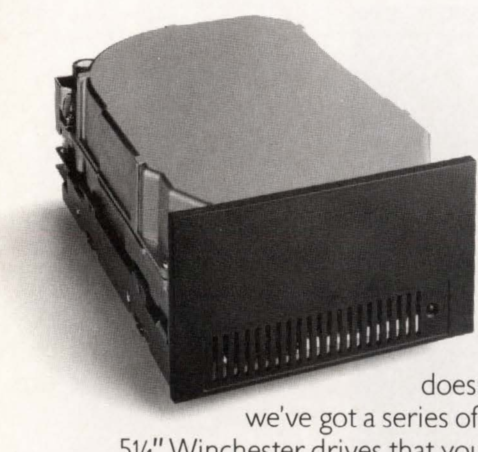

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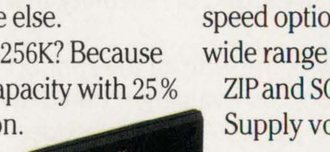

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μPD421000V				20-pin ZIP
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μPD421001LA				26-pin SOJ
μPD421001V				20-pin ZIP
μPD421002C			Static column	18-pin DIP
μPD421002LA				26-pin SOJ
μPD421002V				20-pin ZIP
μPD424256C	256K × 4		Fast page	20-pin DIP
μPD424256LA				26-pin SOJ
μPD424256V				20-pin ZIP
μPD424258C			Static column	20-pin DIP
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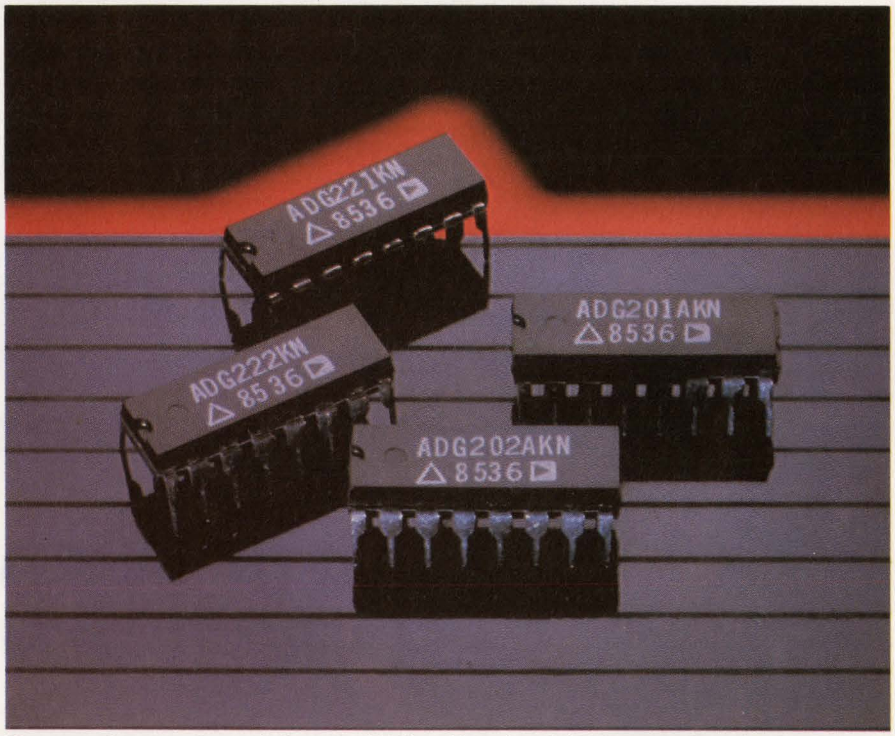
CIRCLE NO 101

Improved analog switches and multiplexers bring benefits to old and new applications

Peter Harold,
European Editor

Process improvements, particularly in the integration of CMOS logic and double-diffused MOS (DMOS) analog switches onto a single chip, have resulted in analog switches and multiplexers that offer lower on-resistance, reduced leakage currents, faster switching, and reduced power consumption compared with their predecessors. The combined effect of reduced on-resistance and reduced internal capacitance has yielded devices with analog bandwidths as high as 300 MHz. Improvements in breakdown-voltage tolerance have allowed manufacturers to produce analog switches with a signal range of ±70V and multiplexers capable of handling ±50V signals. In addition, the new multiplexers can withstand overvoltages on their analog inputs without damaging themselves or their signal sources.



These quad spst analog switches, *the ADG201A/202A and ADG221/222 from Analog Devices, feature approximately half the on-resistance and twice the switching speed of earlier pin-compatible parts.*

The new parts serve in a range of traditional applications, from low-level, precision signal switching to high-frequency switching, and some have inspired new applications—for example, in power switching and industrial control. For precision signal switching, Siliconix's DG Series analog switches and multiplexers have formed the template for a range of industry-standard devices, now available from several alternate sources. Some manufacturers have taken advantage of advances in process technologies to produce improved versions that are pin- and function-compatible with the DG Series parts.

Siliconix itself has introduced two such parts—the DGP201A and DG571. The DGP201A quad spst analog switch features an improved leakage current compared with the company's original DG201A device. Tested on ±16.5V supplies with ±15.5V analog signals, the DGP201A's source and drain off-state leakage currents over the full operating temperature range are 1 nA max for devices that operate over the −40 to +85°C extended industrial-temperature range and 10 nA max for military-temperature-range (−55 to +125°C) devices. These figures compare with 100 nA for the original DG201A.

The DGP201A also specs a 50-pC max charge-transfer error (or charge injection) at 25°C, plus a 100-nsec max switching-speed variation and a 15Ω max on-resistance (R_{ON}) variation between different switches in the same package over the full operating ranges—specifications that don't exist on the DG201A data sheet. In addition, DGP201A devices are tested over a ±10.8 to ±22V supply range, with several parameters tested for every device in each production run, to ensure thorough evaluations of your design. Prices range from $5.22 to $40.04, depending on the package type and grade (all prices quoted in this article are for quantities of 100 unless otherwise specified). You can obtain these devices processed to MIL-STD-883 requirements.

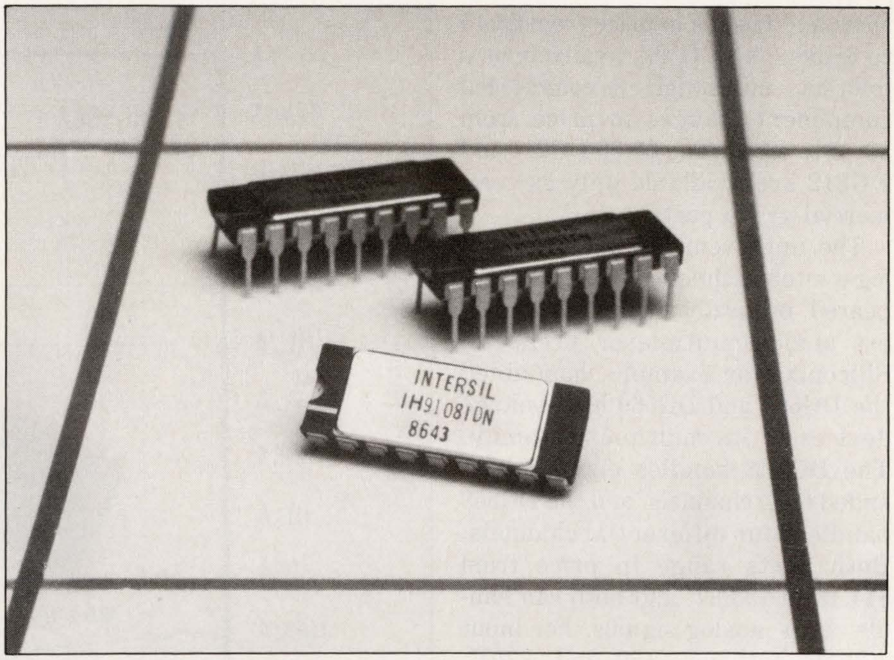
Switch handles ±50V

The DG571 quad spst analog switch is pin-compatible with the DG201A, but it handles input voltages as great as ±50V. For input signals between −50 and +30V, the military version features an on-resistance of 75Ω max, and the commercial (0 to 70°C) and extended-

industrial versions spec an on-resistance of 60Ω max over the full operating range (40Ω max at 25°C for all versions). The devices' quiescent power consumption is 270 μW max. Unlike the DG201A and DGP201A, which have TTL-compatible inputs, the DG571 requires input-low and input-high levels of ≤3.5V and ≥11.5V—compatible with CMOS logic operating from 15V supplies. Prices for the three grades range from $10.46 to $25.94.

Siliconix has recently extended the DG Series analog switches with the DG400 through DG405, DG411, DG412, and DG413 devices. The DG400, -01, -02, -03, -04, and -05 are analog switches providing one spst, two spst, one spdt, two spdt, one dpst, and two dpst switches per package, respectively. All nine new devices feature a ±15V input-signal range. The maximum full-temperature-range R_{ON} is 35Ω for the military versions and 50Ω for the extended-industrial parts (25Ω and 30Ω max at 25°C). The turn-on time (t_{ON}) is 125 nsec max, and the turn-off time (t_{OFF}) is 75 nsec max at 25°C. The military and extended-industrial versions consume respective maximum supply currents of 1 and 10 μA from both the positive and negative supplies. The spdt versions guarantee make-before-break operation. Prices for the DG400/05 group range from $2.13 to $20.74, depending on the grade and required switch configuration.

The DG411 and DG412 are quad spst analog switches with normally open (NO) and normally closed (NC) switches, respectively. The DG413 has two NO and two NC switches in the same package. In most cases, the switch specifications of all three devices are similar to those of the military versions of the DG400/05 group. Prices range from $3.51 to $26.97, depending on the grade and the package. The DG400/05 group and the DG411, DG412, and DG413 are available processed to MIL-STD-883 requirements.



Capable of handling ±50V signals, *the IH9108 8-channel multiplexer from GE-Intersil features a source off-state leakage of 2 nA and a drain off/on-state leakage of 15 nA.*

The $3.15 ADG201A and $2.95 ADG202A quad spst analog switches from Analog Devices are functionally compatible with their DG201A and DG202 counterparts, but they feature approximately half the R_{ON}. The maximum full-temperature-range R_{ON} value for the military, industrial (−25 to +85°C), and commercial ADG201A and ADG202A is 145Ω, compared with 250Ω for the original Siliconix equivalents. Switching times are approximately twice as fast; at 25°C, t_{ON} is 300 nsec max and t_{OFF} is 250 nsec max. Analog Devices also supplies the latched-digital-input versions of these switches, the $2.56 ADG221 and ADG222. Other recent introductions include the AD7590DI, AD7591DI and AD7592DI, all of which cost $4.95. These parts are pin-compatible, latched-digital-input versions of the AD7510DI Series overvoltage-protected analog switches.

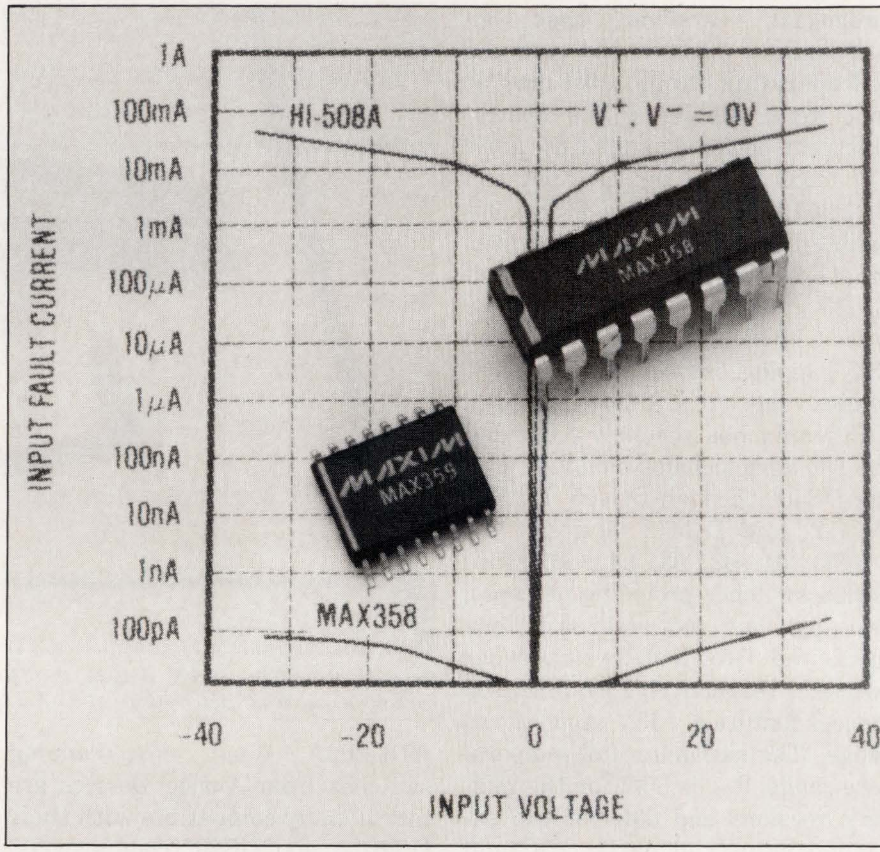
Maxim Integrated Products' DG201A, DG211, DG202, and DG212—all quad spst analog switches—have static and dynamic switch specifications that closely match those of the Siliconix's originals. What distinguishes the Maxim parts is a maximum current from their positive and negative supplies of 100 μA, suiting them for use in battery-powered and portable equipment. This figure compares with respective positive and negative supply currents of 2 and 1 mA max for the Siliconix DG201A and DG202, and 0.48 mA max for both supplies of Siliconix's DG211 and -212 members of the series.

In addition, the Maxim parts are specified for operation with supplies ranging from ±4.5 to ±18V, and unlike most DG211 and DG212 devices, the Maxim DG211 and DG212 don't require an additional 5V rail to supply their logic circuitry. The Maxim parts are also guaranteed not to latch up if the power supplies are removed with the analog signals still connected, although you must still take steps to limit the current that flows under such conditions.

By any other name . . .

The Maxim DG201A and DG202 are also available under the Maxim part numbers MAX331 and MAX332, respectively. The $8.80 MAX331 and MAX332 are available only as military components. The DG201A comes in commercial, extended-industrial, and military versions and ranges in price from $3.15 to $8.58. The DG202, available as a military, industrial, or commercial component, ranges in price from $3.55 to $8.80. The $1.60 DG211 and DG212 are available only as commercial-grade parts.

The improvements made in analog-switch technology have also appeared, naturally enough, in the latest analog-multiplexer products. Siliconix, for example, has added the DG568 and DG569 high-voltage devices to its multiplexer family. The DG568 handles eight single-ended (SE) channels, and the DG569 handles four differential channels. Both parts range in price from $14.13 to $33.67, and both can handle ±50V analog signals. For input signals between −50 and +30V, these multiplexers spec a maximum full-temperature-range R_{ON} of 75Ω for the military version and 60Ω for the industrial and commercial devices (40Ω max at 25°C for all devices). The multiplexers have on-chip latches with CMOS-compatible inputs to simplify the interface to μP systems.



***Analog inputs of ±35V,** when applied to unpowered MAX358, -359, -368, or -369 8-channel (SE) and 4-channel (differential) multiplexers from Maxim Integrated Products, typically result in less than 200 pA of input current.*

GE-Intersil also offers a ±50V, 8-channel multiplexer. The IH9108 is pin- and function-compatible with the DG568. Switch specifications for both devices are approximately equivalent, except that the military version of the former offers improved leakage-current specs. At 25°C (the preliminary IH9108 data sheet doesn't include figures for the full temperature range), the source off-state leakage, drain off-state leakage, and drain on-state leakage are 2, 15, and 15 nA, compared with figures of 5, 25, and 20 nA for the Siliconix DG568. Commercial, industrial, and military versions of the IH9108 cost $25.45, $30.45, and $50.70, respectively.

For applications that don't need to handle signals greater than ±15V, but that need protection against abnormal input voltages—for example, in data-acquisition systems where you have limited control over noise- and fault-induced input overvoltages—you can obtain multiplexers that suit the task. Harris Semiconductor provides input overvoltage protection on its HI546 through HI549 multiplexers. These versions of the company's HI506A through HI509A devices guarantee 7% max channel-R_{ON} matching within the same device. Products in the HI546/549 group range in price from $7.90 for a commercial version to $84.75 for a military part processed to MIL-STD-883.

All these devices withstand overvoltages on their analog inputs as great as 20V above the positive supply rail or below the negative supply rail; that is, when they're operating from ±15V supplies, the multiplexers are protected against overvoltages as great as ±35V. More important, unlike other manufacturers of parts that incorporate overvoltage protection, Harris guarantees that such overloads won't disturb the signal-handling performance of other multiplexer channels within the device. In a data-acquisition system, this feature can be a very important one, because it enables you to continue monitoring a system even when one of the signal sources develops an overvoltage fault.

Because the input impedance of an overvoltage input is approximately 1 kΩ, however, the input may draw several milliamperes of current from the signal source during overload conditions, and you must consider the resulting power dissipation, both with respect to the signal source's capabilities, and with respect to the allowable power dissipation in the multiplexer. In addition to handling overvoltage signals, the Harris parts also provide an input impedance of approximately 1 kΩ, even if the multiplexer's power supplies are removed while input signals are still present.

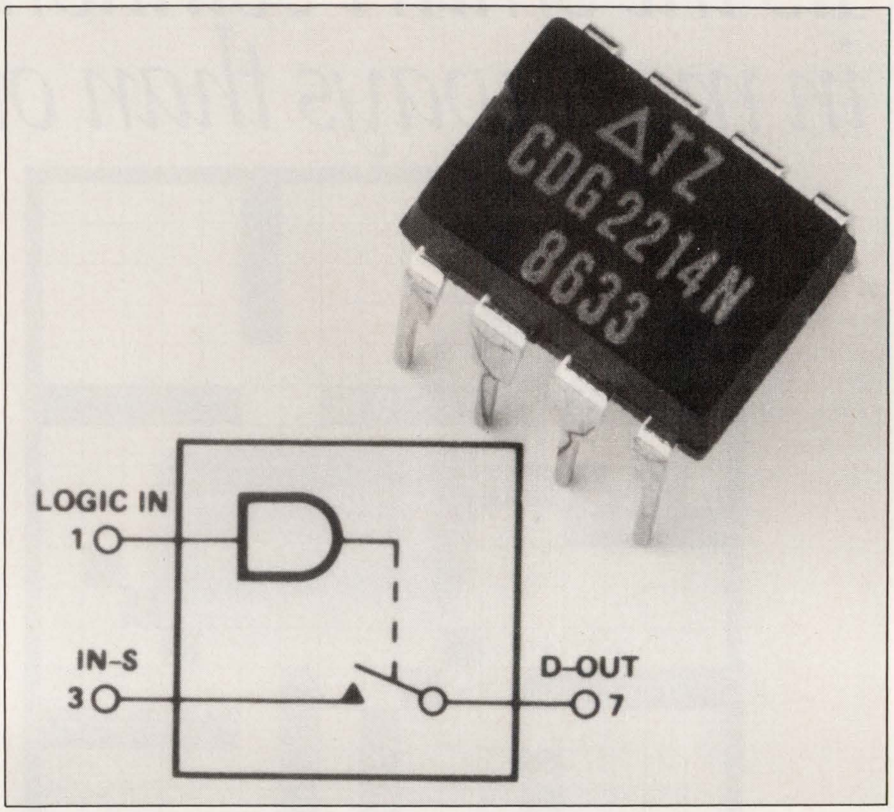
Maxim Integrated Products takes this measure of protection one step

further. On its HI508A and HI509A, and on its HI508L and HI509L latched-digital-input versions (which are all pin compatible with the corresponding Harris parts), an overvoltage condition on any input channel causes that channel to turn off. The input current is limited to 10 μA max for the commercial device and 5 μA for the military device.

If the multiplexer's power supplies are removed when analog input voltages are still present, all channels turn off and input currents are limited to 5 and 2 μA for the commercial and military components, respectively. Unlike other pin-compatible parts, these Maxim multiplexers are specified to operate from supplies in the ±4.5 to ±18V range, and they offer reduced power consumption (for example, the military versions of the 508A and 509A consume 0.7 mA max for the positive supply and 0.2 mA max for the negative supply).

Prices for the Maxim HI508A and HI509A start at $7.35 for a commercial-grade component and $17.35 for a military-grade component. The HI508L and HI509L versions sell for $7.95 to $18.75. The company also offers the devices as the MAX358, -359, -368, and -369. In addition, Maxim offers versions of the Intersil DG508A and DG509A with reduced R_{ON}, reduced leakage currents and power supply currents, and faster turn-on and turn-off times after assertion of the enable input.

If your application calls for the routing of high-frequency signals—for example, on video or RF channels—you'll welcome the recent introduction of analog switches and multiplexers that handle the required switching with acceptable levels of off-state isolation and crosstalk. In order to achieve sufficient off-state isolation at high frequencies, nearly all these switches and multiplexers employ T-switch configurations, which provide a shunt path to ground for those ac signals that break through from the input when the switch is open.



***A 3-dB bandwidth of 250 MHz** distinguishes the CDG2214 spst analog switch from Topaz Semiconductor. The device also specs off-state isolation figures of 100 and 200 MHz at 37 and 22 dB, respectively.*

GE-Intersil's 16-pin IH5352 quad spst RF/video switch and 14-pin IH5341 dual spst RF/video switch have a 100-MHz typ 3-dB bandwidth. The maximum full-temperature-range R_{ON} is 100Ω for ±5V inputs. For an individual switch operating at 10 MHz with 75Ω source and load impedances, both the off-isolation and the cross-coupling rejection ratio (or crosstalk) between a driven on-state switch and an off-state switch output are 60 dB typ. The IH5352 is priced from $7.75 to $15.50; the IH5341, from $3.90 to $8.90. (The price depends on the grade for both.) Maxim produces pin- and function-compatible devices under the same part numbers, but these devices spec a minimum off-isolation of 70 dB; the cross-coupling rejection ratio is 70 dB for the Maxim IH5341 and 66 dB for the Maxim IH5352.

Topaz Semiconductor's $2.45 CDG201B, which is pin compatible with the DG201, is also suited to switching high-frequency signals. The switch's on-state insertion loss of approximately 0.5 dB into a 1-kΩ load, or 5 dB into a 50Ω load, exhibits a typical roll-off of less than 1 dB at 100 MHz. At 10 MHz the minimum off-state isolation rejection ratio of the switch is 60 dB with a 50Ω load, and under similar conditions the channel-to-channel cross-coupling rejection ratio is 80 dB typ. The switch's source and drain capacitances are 3 and 0.3 pF, respectively. For analog signals between −10 and +2V, the switch's R_{ON} is 120Ω max at the device's maximum operating temperature of 85°C (80Ω max at 25°C). The CDG201B's control inputs are TTL compatible.

Topaz's $2.30 CDG308 and CDG309 quad spst analog switches target applications similar to those served by the CDG201B, but they have CMOS-compatible inputs and faster switching times (250-nsec

max t_{ON} and 220-nsec max t_{OFF}, compared with 600- and 300-nsec max for the CDG201B). The off-state isolation rejection ratio is 60 dB min at 10 MHz with a 50Ω load. In addition, the devices have a quiescent supply current (that is, the current drawn when all switches are off) of only 100 nA typ (500 nA max) at 25°C.

Topaz's $3.90 CDG4308 and CDG4309 analog switches use the same respective dies as the CDG308 and CDG309, but the -4308 and the -4309 come in 20-pin rather than 16-pin packages. The 20-pin package allows for an additional unconnected pin between each switch's input and output, providing an extra 6 dB of off-state isolation. For all these devices the analog signal range is limited to ±10V when the devices are operating from ±15V supplies.

The company's $3.76 CDG5341, a 14-pin, CMOS-compatible dual spst analog switch, has a 50 MHz min 3-dB bandwidth. When the device is operating at 10 MHz with a 50Ω load, both the off-state isolation and cross-coupling rejection ratio are 80 dB min. In contrast, the company's $1.25 CDG2214, a CMOS-compatible spst analog switch housed in an 8-pin miniature DIP, has a 3-dB bandwidth of 250 MHz and offers a minimum off-state isolation of 37 dB at 100 MHz and 22 dB at 200 MHz with a 50Ω load.

Muxes for professional video

Siliconix has recently introduced two 16-channel video multiplexer products, the DG536 and the lower cost DG535. Targeted at professional, broadcast-quality video applications, the $19.20 DG536 has an analog bandwidth of 300 MHz. At 5 MHz the device specs a minimum all-hostile crosstalk level (see **box**, "Definitions") of −60 dB, a multiplexer-disabled crosstalk level of −85 dB typ, and an adjacent-input crosstalk level of −92 dB typ. The company achieves the low adjacent-input crosstalk by providing ground pins, internally connected to ac ground, between each analog input pin.

The $14.40 DG535 is for industrial markets. It comes in a 28-pin DIP and lacks the additional ground pins between the multiplexer inputs. At 5 MHz the multiplexer specs a typical all-hostile crosstalk level of −60 dB, a typical multiplexer-disabled crosstalk level of −60 dB, and a typical adjacent input crosstalk level of −72 dB.

Maxim offers two 16-pin, 8-channel RF/video multiplexers, designated the MAX310 and MAX311. Both parts cost $8 to $14.40, depending on the grade. The MAX310 is an 8-channel (SE) multiplexer, while the MAX311 is configured to switch four differential-input channels. At 5 MHz both devices spec an all-hostile crosstalk of −58 dB typ with on-channel source and load resistances of 75Ω (−63 dB if you reduce the on-channel source impedance to 10Ω). At 5 MHz the multiplexer-disabled crosstalk is −63 dB typ, and the adjacent-input crosstalk is −72 dB typ. Topaz's $2.30 CDG4500, a 14-pin, 4-channel high frequency multiplexer, has a minimum 3-dB bandwidth of 100 MHz and specs a minimum all-hostile crosstalk level of −62 dB at 10 MHz with a 50Ω load.

Multiplexers capable of handling high frequencies are suited not only to analog signal routing, but also to digital-signal-routing functions. In some applications they can eliminate the need for ECL data multiplexers, with attendant reductions in system power consumption and cost.

Devices switch 140V p-p

Most analog switches and multiplexers find use in signal-switching applications—for example, in data-acquisition systems, programmable-gain amplifiers, and multiplexer systems—for which such parameters as leakage currents, R_{ON}, R_{ON} modulation effects, and switching speeds are the main influences on signal integrity. Supertex Inc, however, emphasizes power-switching and industrial-control applications for its high-voltage analog switches.

Operating from ±80V supplies, the company's HV10 to HV18 analog switches can switch analog signals as high as 140V p-p. Less expensive versions for operation from ±70V supplies can switch 120V p-p signals. The product family includes direct-input and latched-digital-input 4-channel switches and latched-input 8-channel switches. Measured with a switch current of 200 mA, the 4-channel switches spec a typical R_{ON} of 15Ω, and the 8-channel

Definitions

"All-hostile" crosstalk is the decibel ratio of the voltage that appears at a multiplexer output to a stimulus voltage that's applied simultaneously to all off-channel inputs. "Multiplexer-disabled" crosstalk is the decibel ratio of the voltage at the multiplexer output to a voltage applied simultaneously to all the inputs with the multiplexer disabled—that is, when all switches are off. "Adjacent-input" crosstalk is the decibel ratio of the voltage that appears at off-channel inputs to the voltage applied to an adjacent on-channel input.

These parameters represent the worst-case operating conditions for the multiplexer. You should use caution, however, when comparing different manufacturers' devices on the basis of these figures, because there's ample scope to massage them by choosing different load-resistor values for the on-channel inputs and multiplexer outputs, or by modifying the test conditions.

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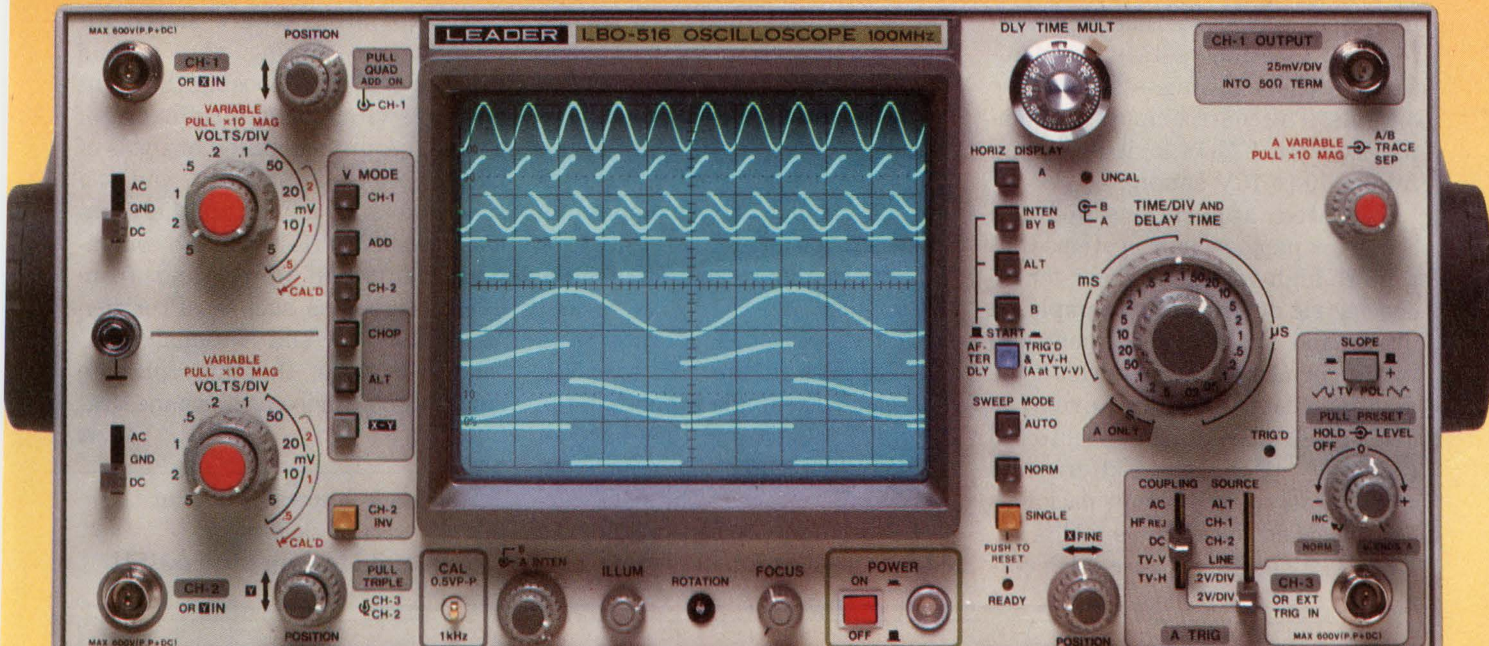

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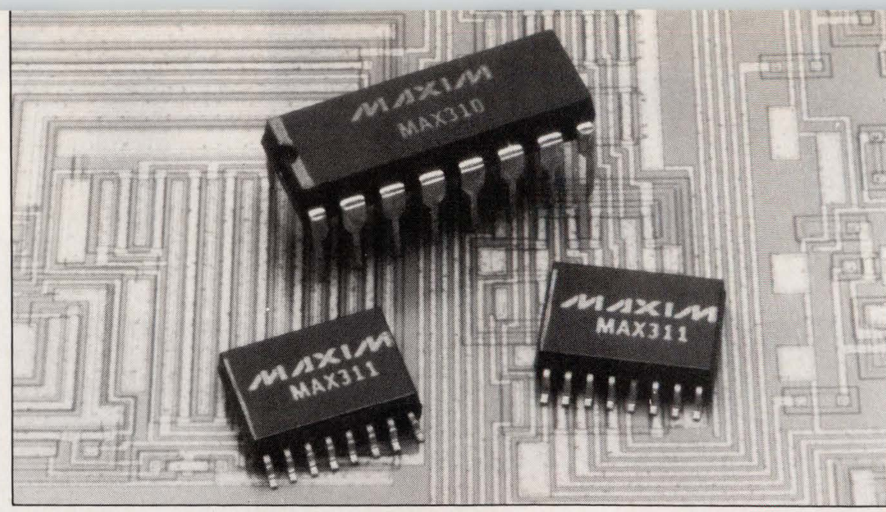
switches spec a typical R_{ON} of 25Ω. The 4-channel switches have a peak-current rating of 3A per channel; the 8-channel switches, 1.5A per channel. All the switches can handle analog signals from dc to 10 MHz, and they typically provide 45 dB of off-state isolation at 5 MHz.

The switches incorporate a metal-masked CMOS-logic array, which allows the company to provide a variety of different control mechanisms. These mechanisms include individual latched digital inputs, serial data entry into a shift register, and 3- to 8-line or dual 2- to 4-line binary decoders for switch selection. In addition to its 3- to 8-line decoder, the HV14 has a separate data input so that you can turn a selected switch on or off. All the devices except the HV17 have internal input latches so that your system can load new data without affecting the existing state of the outputs. The control inputs are compatible with CMOS logic operating from a 10 to 15V supply.

Targeted applications for the Supertex parts include systems that require high-voltage ac drive for piezoelectric devices—for example, in ultrasound imaging equipment and ink-jet printers. Because this type of application often requires the drive electronics to be built into the actuator, Supertex offers its switches in surface-mount packages and in naked die form as well as in DIPs. Prices for plastic-DIP versions range from approximately $16 to $19 (1000).



Channel phase-shift matching of less than 1° at 5 MHz *suits the MAX310 and MAX311 8-channel (SE) and 4-channel (differential) multiplexers from Maxim Integrated Products Inc to the routing of composite-video color signals.*

Both Maxim Integrated Products and Supertex Inc have recently introduced a family of high-voltage analog switches, designated the 341, 343, 345 and 348 (with a MAX prefix for the Maxim parts and HV for the Supertex parts). The Supertex 341, 343, and 345 are dual spst, dual spdt, and dual dpst analog switches, respectively; their maximum full-temperature-range R_{ON} is 100Ω. The equivalent spec for the Maxim parts is 160Ω. The 348 has the same dual-spst configuration as the 341, but it has a maximum full-temperature-range R_{ON} of 75Ω for the Supertex part and 80Ω for the Maxim part.

All the switches operate from split supplies in the ±20 to ±50V range, or from single supplies in the 20 to 60V range, and they have an analog signal range that equals the supply-rail voltages. The peak current rating is 0.5A per switch. The maximum continuous switch current is subject only to the package's power-dissipation limits. The manufacturers offer commercial, industrial (Supertex), extended-industrial (Maxim), and military versions of the parts. Prices from both manufacturers range from approximately $6 to $19, depending on the grade.

The products discussed in this article have been introduced in the last 18 months, or are slated for introduction during the second quarter of 1987. Choosing the right analog switch or multiplexer, of course, requires detailed analysis of all data-sheet parameters, and you should keep in mind that there are many earlier parts, from the companies mentioned above and from other companies such as Precision Monolithics Inc and National Semiconductor Corp, that may provide equally good price/performance ratios. **EDN**

Article Interest Quotient
(Circle One)
High 509 Medium 510 Low 511

For more information . . .

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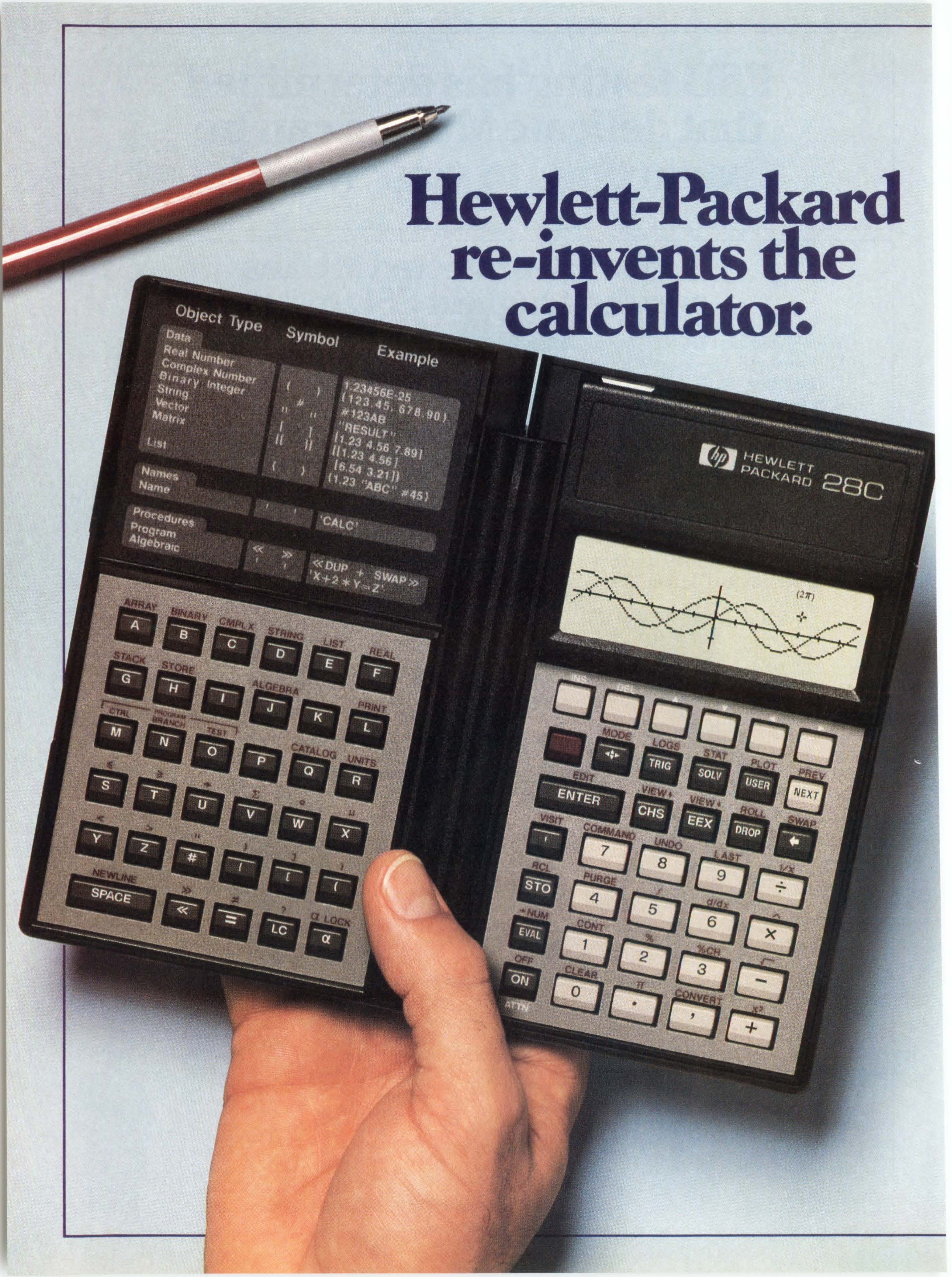
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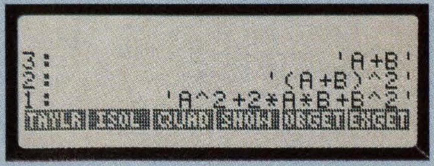

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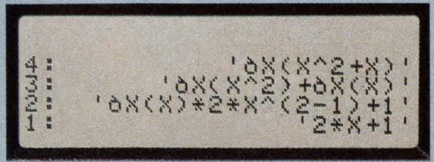

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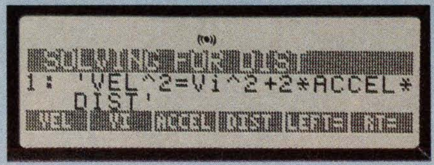

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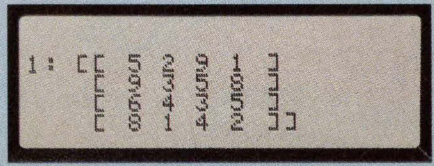

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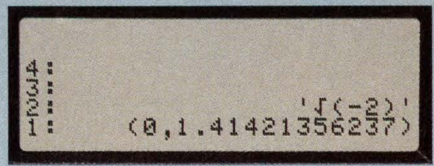

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The mature, yet evolving, technology of delay lines suits modern requirements

Tarlton Fleming,
Associate Editor

Delay lines, although available since the 1960s, aren't much different from the early versions: Most are manually assembled, hybrid components. Despite no quantum jumps or significant changes, though, delay lines don't suffer from the threat of obsolescence. Their technology has evolved and matured, easily matching increases in circuit operating speed. Because today's faster signals require shorter delay intervals, manufacturers are able to produce smaller and less-expensive lines.

Most delay-line products are electromagnetic LC types, with several cascaded sections. Each section consists of a series inductor and a shunt capacitor. Delay lines based on LC sections alone are called analog, or passive, delay lines **(Fig 1a)**. The more prevalent types, often called digital delay modules, add one or more hex-buffer ICs to produce an active delay line **(Fig 1b)**.

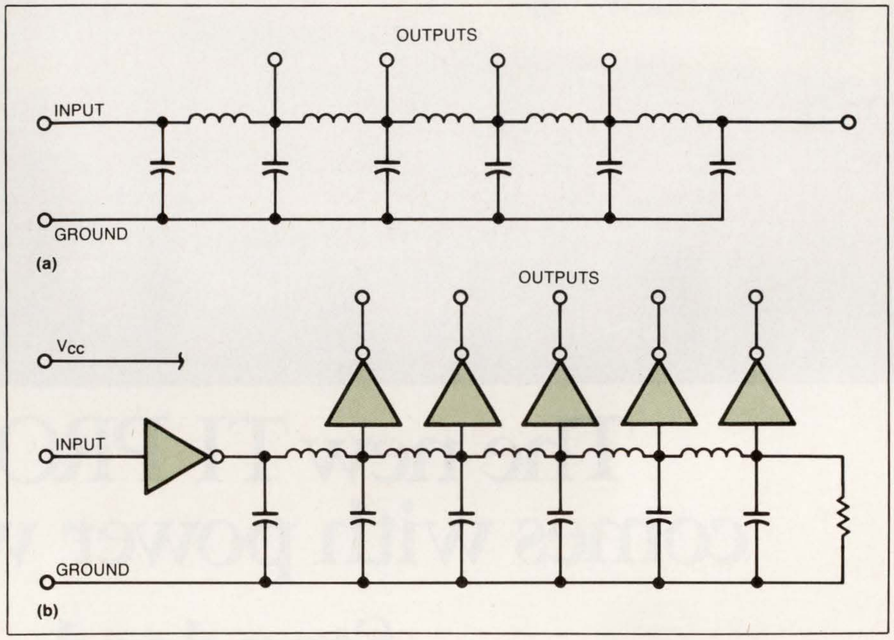

Fig 1—A passive LC delay line (a) *consists of sections in cascade, each containing a series inductor and a shunt capacitor. An active, digital delay line* ***(b)*** *includes inverter gates.*

Whereas passive delay lines can operate on either analog or digital waveforms, the digital types are suitable for use with digital waveforms only. Most delay-line applications are strictly digital, simply because of the prevalence of digital systems and because such applications often use delay lines to eliminate timing skew.

Of the many delay-line manufacturers, most offer similar product lines in which the various DIP, SIP, and surface-mount packages conform to industry-standard pinouts. Product variations include single-, dual-, and triple-line devices as well as variable, multiple-tap, and digitally programmable delay lines.

Technitrol's digital delay modules offer a choice of delays spanning 1 to 500 nsec and include devices compatible with most logic families: ECL, CMOS, and TTL (S, LS, AS, and ALS). The company guarantees a delay tolerance for these products over their specified operating-temperature and supply-voltage ranges that's ±2% of the maximum delay.

The company's TTLDL25 delay line is TTL compatible and provides five taps of 5 nsec each over the range of 5 to 25 nsec. (In most applications you use only one tap, the one that provides a delay interval closest to what you need.) Available in a 14-pin DIP as well as in a 14- or 16-pin surface-mount package, the part sells for $25 (100). Another member of the same family, the 5-tap TTLDL500, provides 100-nsec increments for the same price.

The manufacturer's other TTL-compatible delay modules include 3-tap and 10-tap devices. Further, you can buy 5-tap devices that are compatible with 10K ECL or 8-tap delay lines compatible with 100K ECL. The 100K ECL parts provide delays from 1.2 to 200 nsec in increments as short as 0.5 nsec.

Although few applications require dynamic control of delay time, test equipment and systems whose delay-time requirements change during operation may require programmable digital delay lines. These products have a single buffered output, and you set the delay by applying an appropriate input code.

Kappa Networks is one such manufacturer of programmable delay lines. The 3-bit (eight delay increments), STTL-compatible PT36 Series offers delay increments ranging from 1 to 50 nsec; each member of the series costs $12.85 (100). Similarly, the 4-bit (16 delay increments) STTL-compatible PT42 Series provides delay increments of 1 to 100 nsec. A device in this series costs $19.95 (100).

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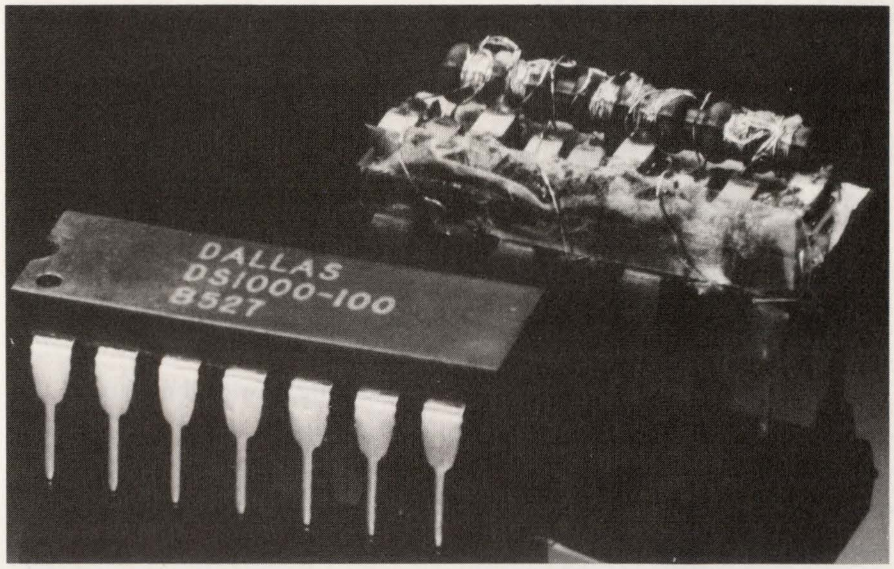
As mentioned, digital delay modules only work with digital signals, but passive delay lines are useful for analog video, radar, and sonar signals, as well as for digital signals. Because passive LC lines have no buffer ICs at the input and output, they can provide lower minimum delay times than the digital delay modules can.

On the other hand, the passive types introduce a new array of electrical parameters for the designer to worry about—parameters whose effects are buffered and hidden within a digital module. These include input-to-output attenuation, characteristic impedance, rise time, bandwidth, and distortion. Furthermore, some applications require that you provide compensation for the passive delay line to achieve a linear phase response.

Most companies that manufacture digital delay lines also sell passive ones. From ESC Electronics, you have a choice of single- or triple-line devices and a choice of 5, 10, or 20 taps. Delays per tap vary from 1 to 200 nsec. Package offerings include 14- and 16-pin DIPs; 3-, 7-, and 14-pin SIPs; and surface-mount types.

PCA Electronics' passive delay lines have 10, 20, or 24 taps, providing tap delays ranging from 1 to 50 nsec. The single-tap EP123 Series includes devices with fixed delays spanning 0.5 to 10 nsec in 0.5-nsec increments, 10 to 20 nsec in 1-nsec increments, and 20 to 40 nsec in 5-nsec increments. The series even boasts a 0-nsec device for those designers who decide they don't need a delay after all. The company charges the same—$2.60 (100)—for any member of the EP123 Series.

In addition, PCA offers a series of variable passive delay lines, which suit applications where fixed-tap devices don't provide enough resolution. Products in the EPA087 Series look like multiturn pc-mount trimming potentiometers and provide adjustment ranges from 10 to 100 nsec. Each costs $25 (100).



This monolithic CMOS delay line, a member of the DS1000 Series, *has five delay taps, each laser-trimmed to within 1 nsec of the desired delay value. The manufacturer, Dallas Semiconductor, claims the device is more reliable than the conventional LC hybrid type shown in the background (without its cover).*

Another form of delay line suitable for use only with analog signals is the charge-transfer device. This MOS IC shifts an analog signal from input to output in bucket-brigade fashion by transferring sample packets of charge from one capacitor to the next (**Fig 2**). Applications for these delay lines include voice scrambling, reverberation effects in stereo equipment, and the generation of vibrato, chorus, phaser/flanger, and tremolo effects in electronic musical instruments.

Each time the ϕ_1 clock signal goes high, the input transistor turns on, charging capacitor C_S with a sample of the input voltage. Subsequent clock cycles shift the charge packet along the chain one stage at a time, which means that the input-to-output delay depends on the clock frequency and the number of stages.

Charge of the bucket brigade

EG&G Reticon's delay lines of this type, for example, have a great number of stages that let you delay an analog signal from 300 μsec to more than 4 sec. The RD5106A, with 256 stages, costs $3.50; the RD5107A, with 512 stages, sells for

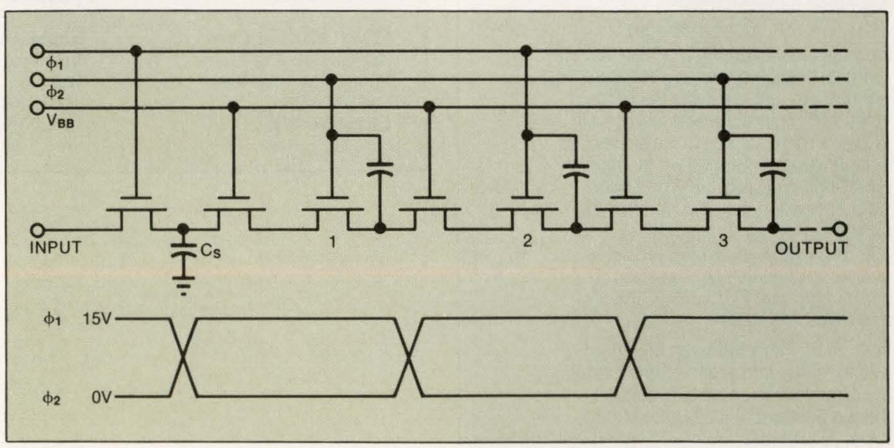


Fig 2—This structure is a bucket-brigade-type *of analog delay line, in which a signal in the form of discrete charge packets shifts one stage along the chain with each cycle of the clock waveforms ϕ_1 and ϕ_2. (V_{BB} is a dc voltage that biases the interstage transistors, which minimize the Miller capacitance between stages.)*

$6.30; and the RD5108A, with 1024 stages, is priced at $10.85 (100).

All charge-transfer devices achieve quantization of an analog signal without resorting to A/D converters. Because they sample the signal, it may be necessary to provide a lowpass filter at the input to prevent aliasing errors, and to include a smoothing filter at the output to remove quantization noise.

Something new and different

In a departure from the conventional types of delay lines, Dallas Semiconductor's DS1000 Series consists of monolithic CMOS chips, each of which gives you five delay taps and delay increments ranging from 10 to 100 nsec. The delay at each tap is simply the propagation time through the preceding amplifier stages.

Patented circuit-design techniques compensate for variations in propagation time caused by changes in the operating conditions, and laser trimming sets each tap delay within 1 nsec of the desired value. Prices for this series start around $4 (100).

All-silicon delay lines provide obvious advantages in reliability and assembly costs, but Dallas Semiconductor faces obstacles in gaining acceptance for these parts over the longstanding, entrenched hybrid types. The company bolsters its claims by noting that these delay lines occupy less space (a 5-tap device fits in an 8-pin miniature DIP) and provide equal precision for leading- and trailing-edge delays.

Delay-line customers and users, however, haven't yet swamped the firm with orders. They point out that the hybrid types do a satisfactory job, provide wider ranges of delay times and operating temperatures, and are comparable in price to the passive LC types. **EDN**

Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

For more information . . .

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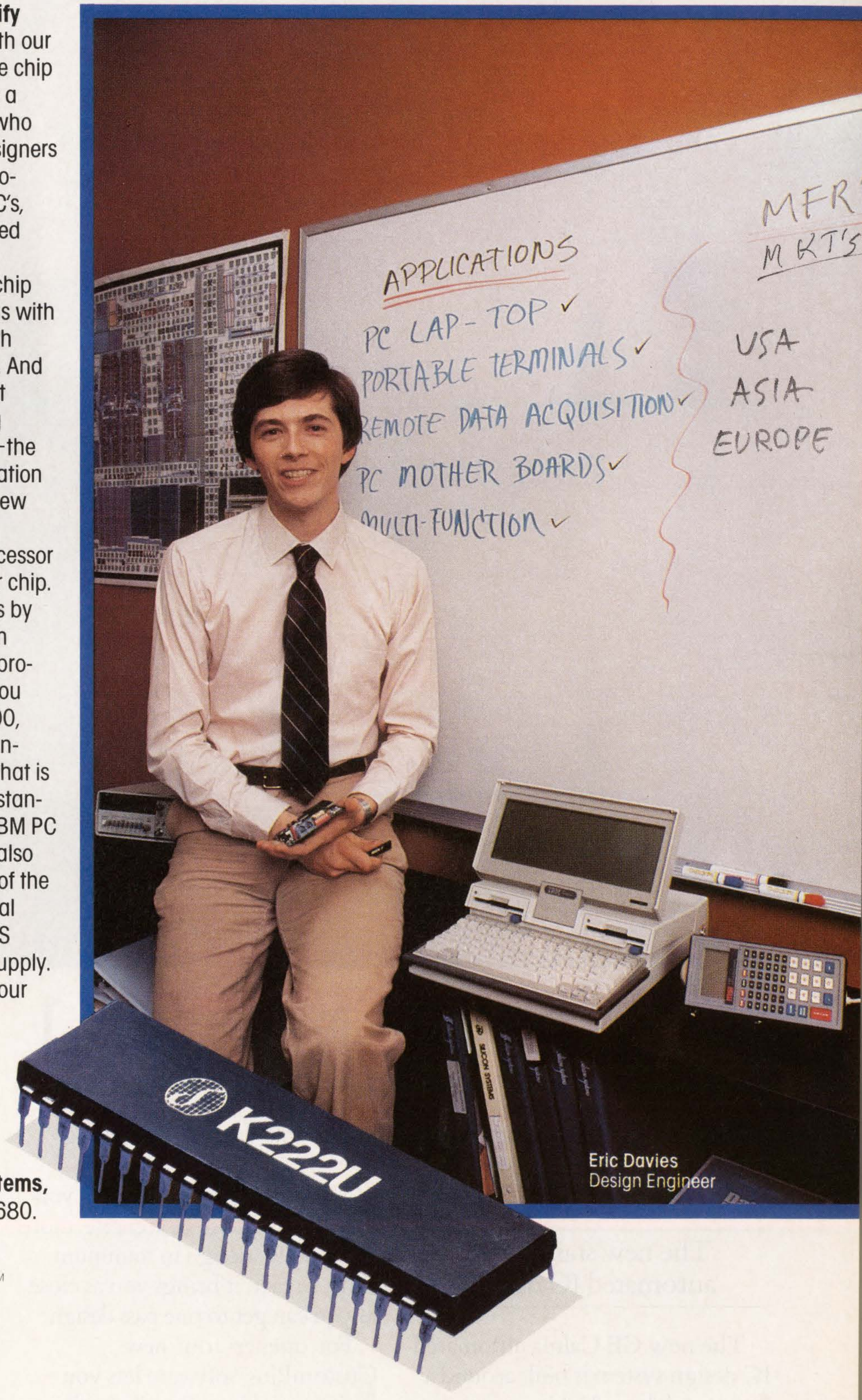

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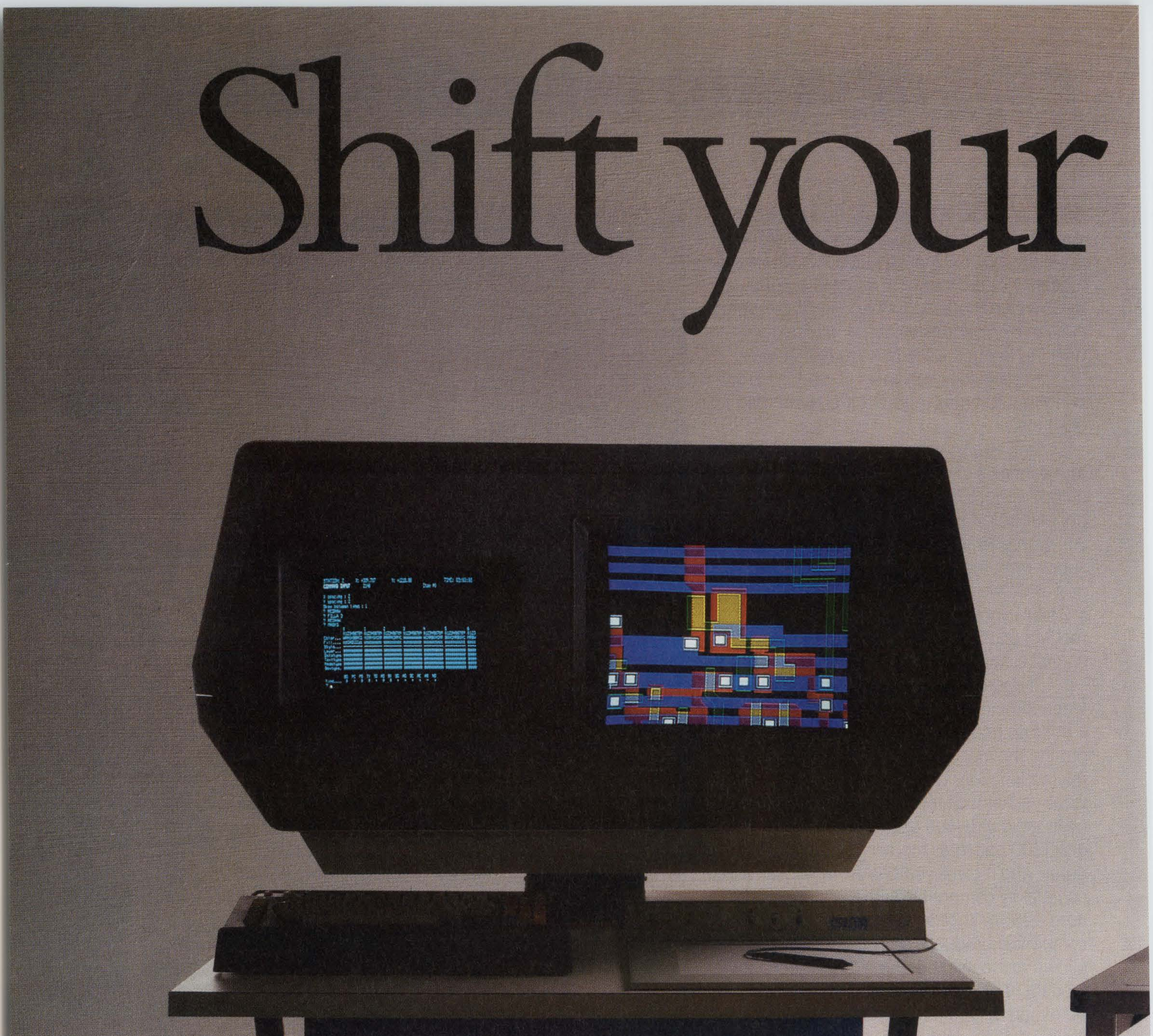

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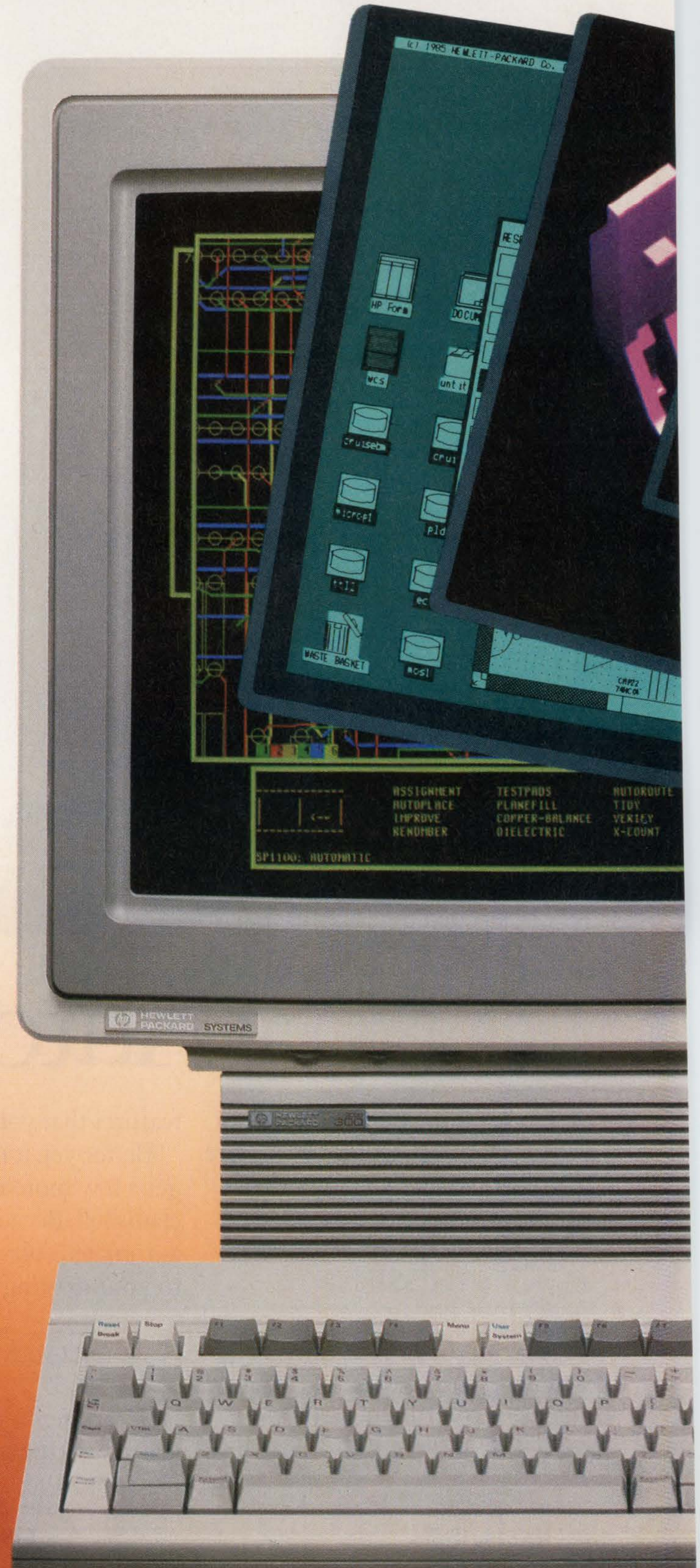

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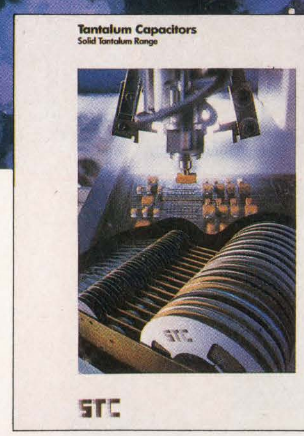

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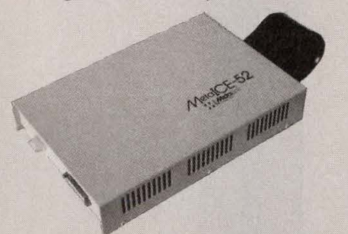

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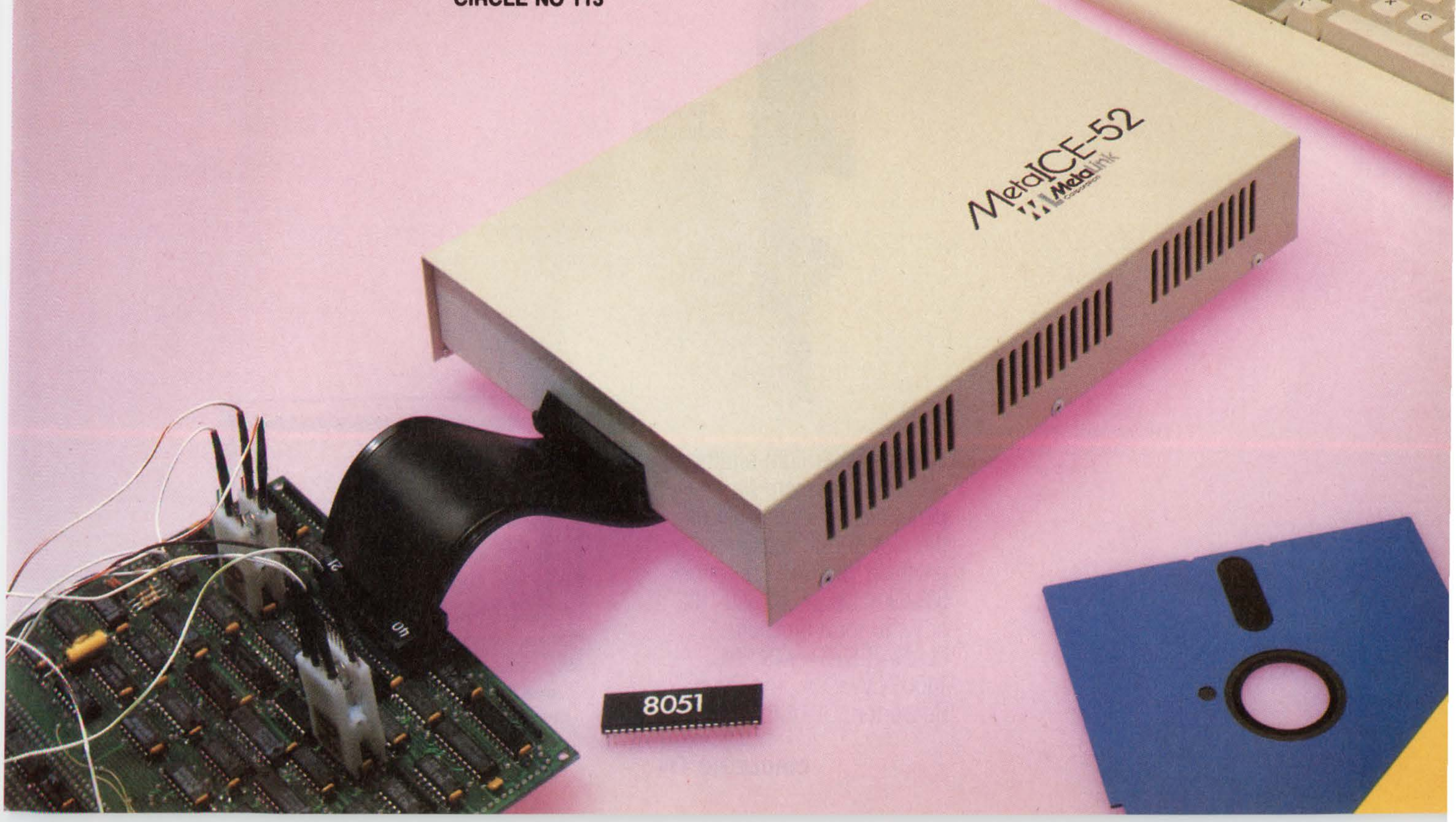

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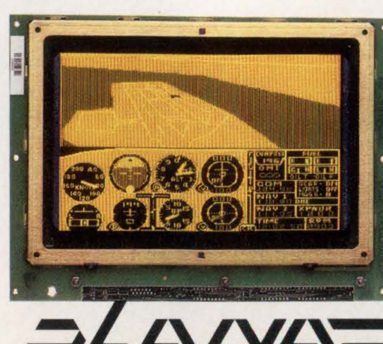

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CIRCLE NO 114

Surface-mount technology forces engineers to follow testability guidelines

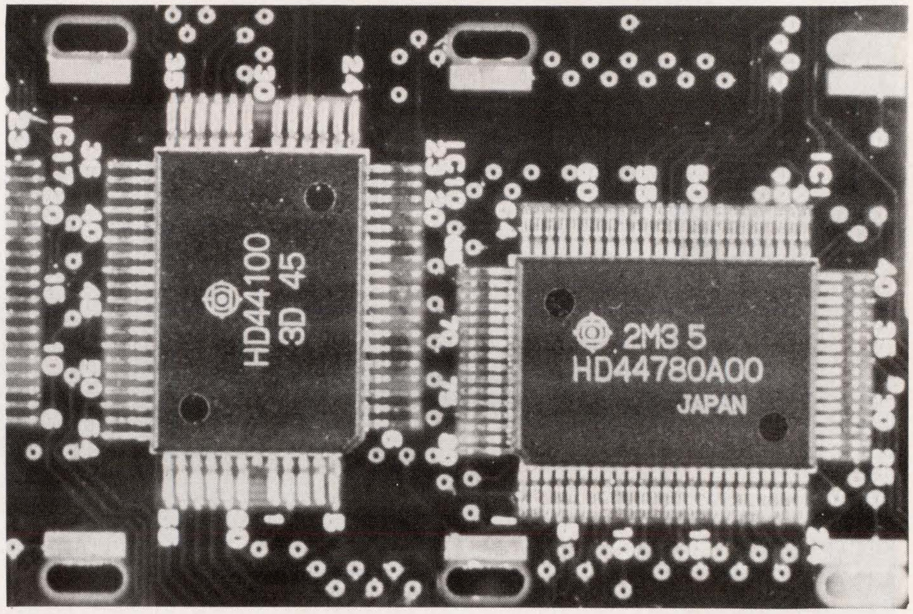
Charles H Small,
Associate Editor

Because surface-mount-technology (SMT) pc boards are so much harder to test than boards manufactured with other, less-dense technologies, design engineers will at long last have to follow the test-engineering community's guidelines for designing testability into boards. Test engineers claim that testing and reworking improperly designed and laid out SMT pc boards can eat up a major portion of the total cost of making a product.

With so much money at stake, engineering management may heed the recommendations of the test community and enforce design-for-testability guidelines. But these guidelines are far more than a simple collection of design ideas, tips, and standard-practice recommendations; the full scope of the test-engineering community's recommendations for SMT entails a fundamental restructuring of both design-engineering teams and the way a company accounts for productivity gains.

The test community is unanimously recommending that the traditional barrier between design and manufacturing be removed and that test engineers get involved in the design of SMT boards from the earliest stages. The test community maintains that managing the complex tradeoff between density and testability requires the full-time attention of a knowledgeable test engineer.

Further, test engineers recommend that companies change their accounting procedures so that the beneficial effects of designing for testability can be traced. Some experts claim that testing and rework can account for as much as 45% of the total cost of getting an SMT design out the door.



***The finer lead pitches and high pin counts** of SMT devices make pc boards bearing SMT devices harder to test than boards manufactured with older, less-dense technologies. (Photo courtesy Hewlett-Packard's Manufacturing Test Div)*

Because testing and rework consume so many production dollars, test engineers maintain that design engineers must compromise their design goals and be satisfied with packing somewhat fewer than the maximum possible number of devices onto a given SMT pc board.

Testability guidelines reduce an SMT board's density in two basic ways: Some guidelines require designers to include extra devices so that the test equipment can partition and isolate the circuits and devices under test, thereby gaining control of them; other guidelines require that pc-board designers open up the spacing between components and add extra pads and vias so that bed-of-nails fixtures can probe the circuits under test.

Many of the test community's circuit-design guidelines will sound familiar to any design engineer who has read testability articles in the past. The guidelines recommend that design engineers insert extra gates in clock circuits so that automatic test equipment (ATE) can control or back-drive the clock circuit. Similarly, they recommend that designers insert extra control gates or jumpers in critical circuit paths and feedback loops. (Design engineers in the past have been reluctant to add extra gates in critical circuit paths because of the extra delays the gates incur.)

Further, to ensure that ATE can isolate and back-drive individual components, designers should make certain that every unused input has its own pullup or pulldown resistor.

The testability guidelines also recommend that registers, counters, and state machines be easy to

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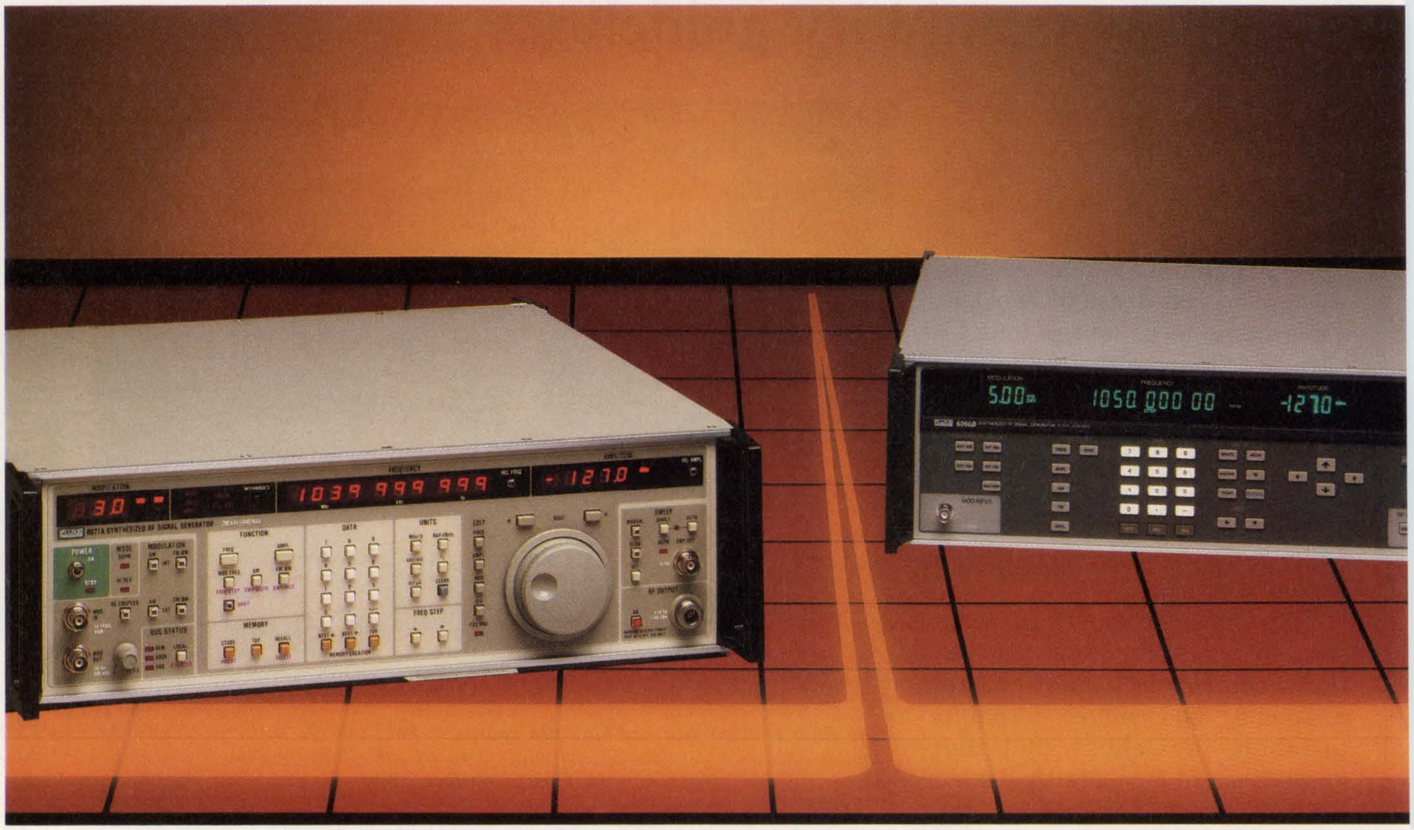

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CIRCLE NO 115

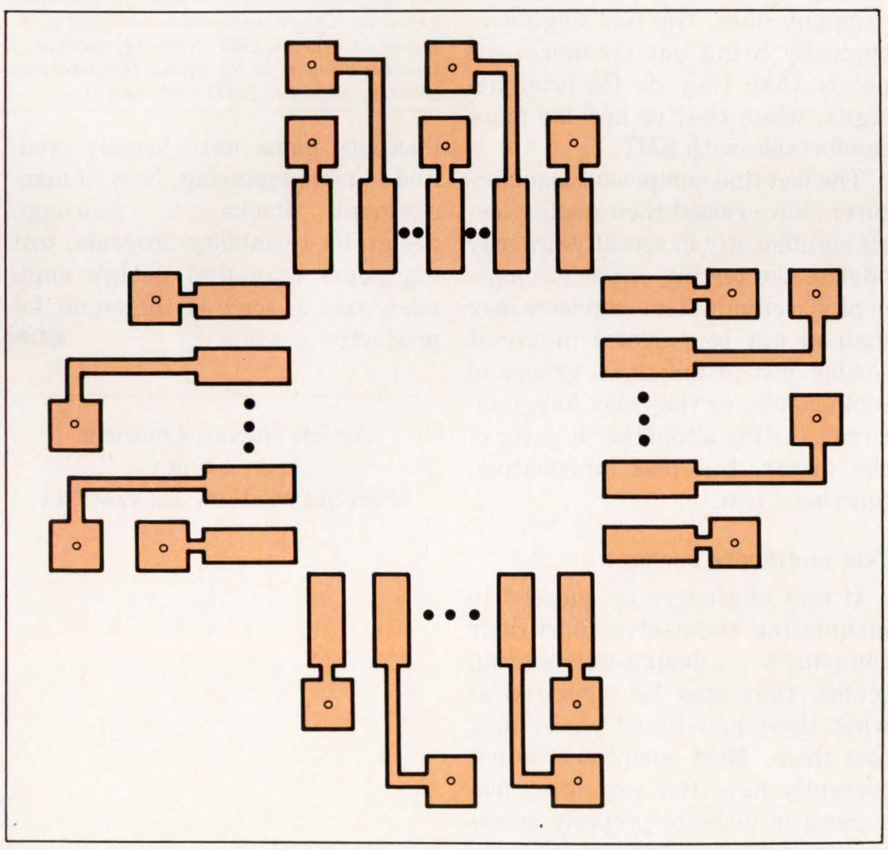
initialize. Note that the methods (such as level-sensitive scan design) employed in IC design to initialize the registers of an IC, work well when you're testing individual ICs before assembly. But test engineers find that the built-in test functions of such chips take too long to use after a number of the chips have been assembled onto a pc board. Test engineers also encourage design engineers to include more-extensive built-in test functions with µP-based boards.

One test-industry consulting firm, Logical Solutions Technology Inc (Campbell, CA), goes even further in suggesting extra devices. This company's solution to the problem of testability is to add special-purpose testing chips to a circuit. These chips can monitor and stimulate critical nodes in a circuit. The chips have their own, dedicated I/O bus, called the T-Bus (or testability bus).

Testability guidelines will also have a major impact on board layout and routing. And, indirectly, these guidelines will reflect on circuit designers, because the guidelines limit circuit designers' ability to pack SMT boards as densely as possible.

For example, the mechanical properties of so-called "pogo pins" (small spring-loaded probes, embedded in a test fixture, which touch various points on the pc board under test) impose several limitations on SMT pc-board density.

Test engineers will not allow a probe to come in direct contact with a device or a device's leads. Such direct probing has two disadvantages: First, it can bend or otherwise damage the probe if the part is not properly aligned, and second, the probe could push down an improperly soldered device or lead, causing a bad connection to test out as good.



***This SMT-pad pattern accommodates devices** having 50-mil-spaced leads. It also provides test points on 100-mil centers, which are suitable for conventional bed-of-nails fixtures. (Pattern courtesy Interconnect Technology Inc)*

Therefore, pc-board designers must provide an isolated target—a pad or a via—for the pogo pin to come in contact with. (The pc-board designer can't simply extend an SMT device's pads; an extended pad can disturb the surface tension of the molten solder that serves to align an SMT device during soldering.) These extra pads and vias reduce the board's density, because they use up portions of the pc board's real estate that would otherwise be devoted to working devices or traces.

Further, test engineers prefer to have test points all on one side of a board and to have them spaced on the older 100-mil grid rather than on the newer 50-mil (or smaller) grids of SMT boards. Having all the test points on one side of a pc board allows test engineers to employ a single-sided, bed-of-nails test fixture rather than the much more expensive and less reliable two-sided (or "clamshell") fixture. At present, pogo pins suitable for 50-mil spacing cost five times as much—and fail twice as often—as 100-mil pins do.

What's more, although two-sided fixtures are relatively new to pc-board assembly, makers of bare, multilayer pc boards already have considerable experience with two-sided test fixtures. These manufacturers find two-sided fixtures to be a high-maintenance item.

PC-board designers must be careful not to place too many test points in one area, or the combined pressure of many pogo pins concentrated in that area could deform the pc board under test.

Test engineers also do not care for pc-board traces that are buried inside multilayer boards and hidden under the SMT devices. They prefer to have traces out in the open where they can get at them.

All the foregoing constraints on the pc-board designer's options serve to increase testability at the expense of pc-board density.

Once the test engineers actually

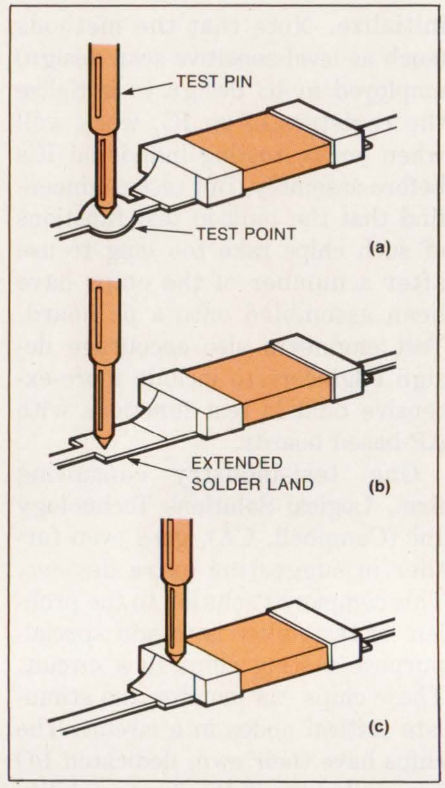
get their hands on the finished pc boards, however, they'll find that several developments in electronics —of which SMT is only one—are dealing test engineers a new hand. In the past, test engineers could take advantage of in-circuit testers having literally thousands of pogo pins to test not only all the devices on a board individually, but also the continuity of each trace. That way, they could isolate bad components and bad pc-board traces with one test. Knowing the exact location of bad components and traces allowed the test engineers to rework bad boards easily.

Now that even the least dense SMT board carries twice the circuitry of through-hole boards, SMT boards do not allow the probing of all the end points of a given trace. Test engineers may have to test the bare pc board for continuity first, and later settle for merely probing selected nodes on the loaded board. For the first few SMT designs that a company does, the test engineers typically bring out far more test points than they do for later designs, when they've become more comfortable with SMT.

The fact that component manufacturers have raised their quality levels significantly in recent years may obviate the testing of every component in a circuit. Test engineers may instead opt to perform in-circuit testing just of functional groups of components, or they may forego in-circuit testing altogether in favor of the faster, but less informative, functional test.

Test engineers beware!

If test engineers do succeed in insinuating themselves into their company's design-engineering teams, they may be surprised at what their new-found power may cost them. Most companies do not currently have the accounting machinery in place to properly assess the productivity savings that accrue from the extra time spent at the design stage. In the past, any pro-



Test points need to be close *to SMT devices* ***(a)****. Test engineers do not recommend extending the solder pad* ***(b)*** *because of soldering problems. They also do not recommend probing on or near an SMT device* ***(c)*** *because of possible damage to the probe. (Illustrations courtesy Signetics SMD Technology)*

ductivity gains were usually credited to manufacturing. Now, if management backs a thorough design-for-testability program, test engineers may find design engineers taking some of the credit for productivity gains. **EDN**

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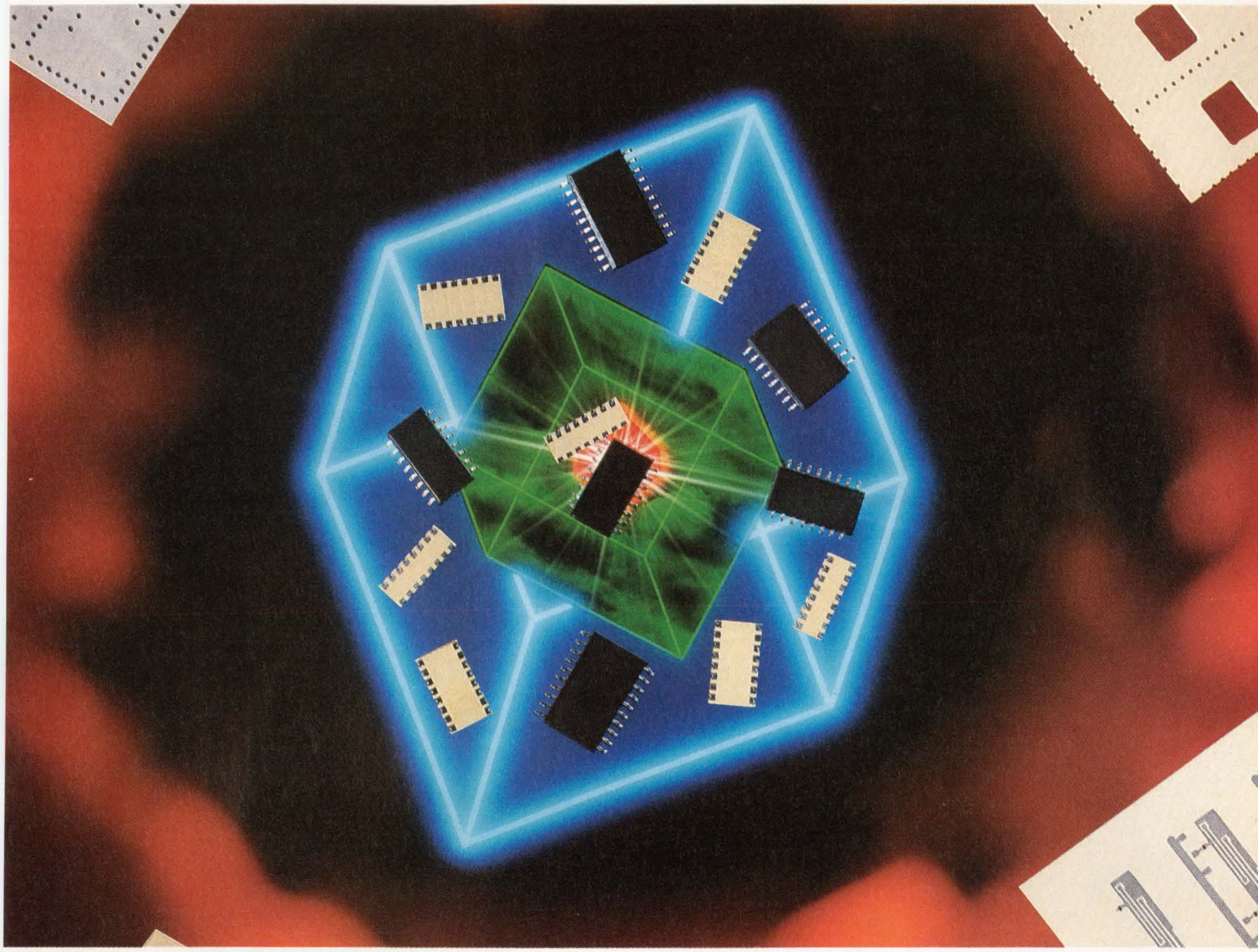

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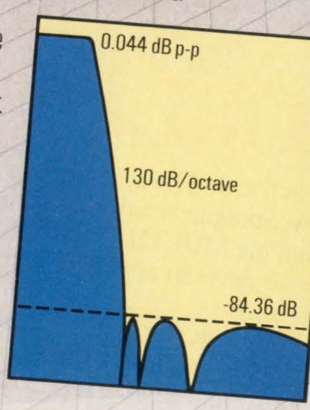

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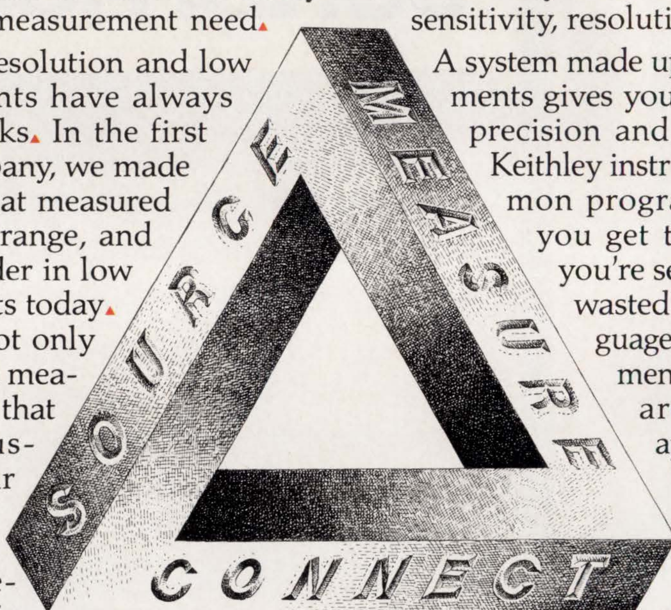

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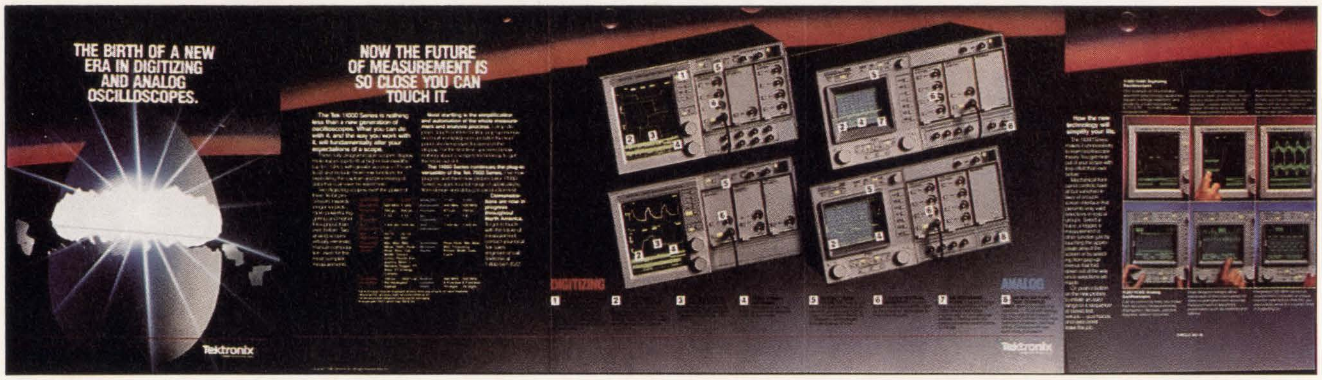

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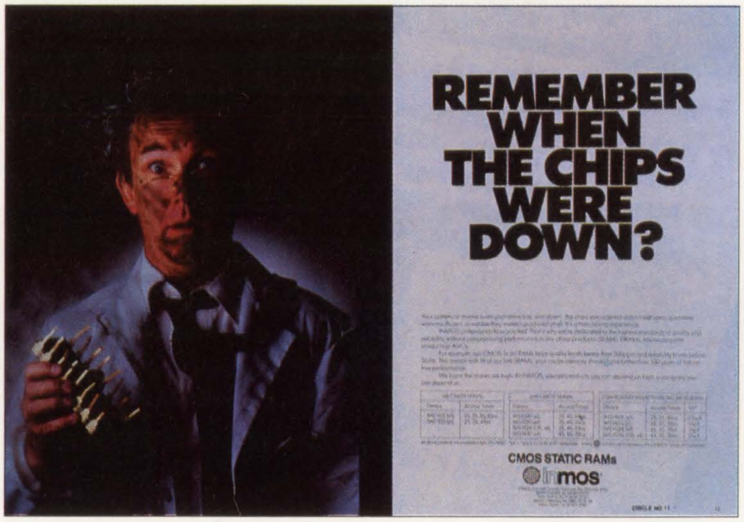

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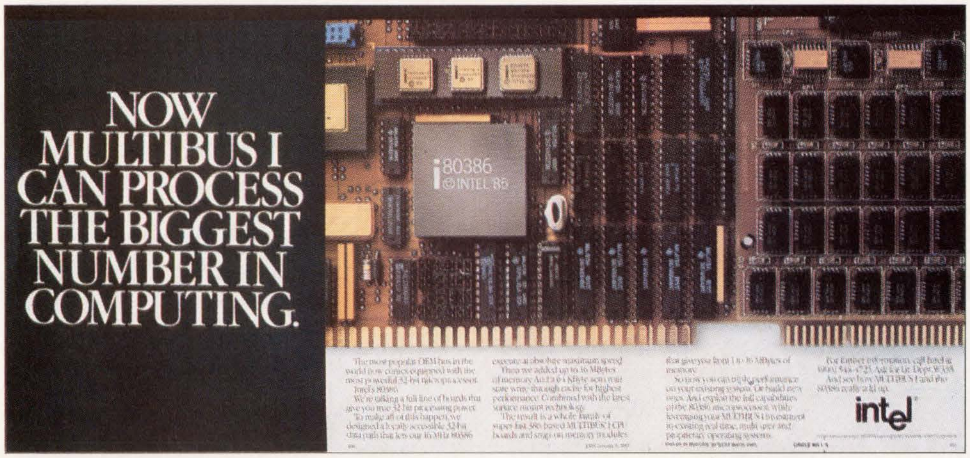

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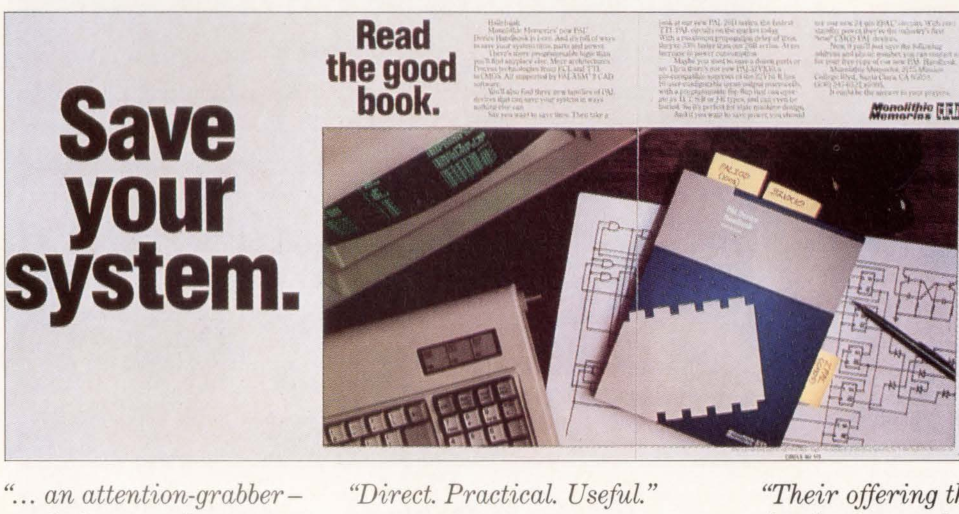

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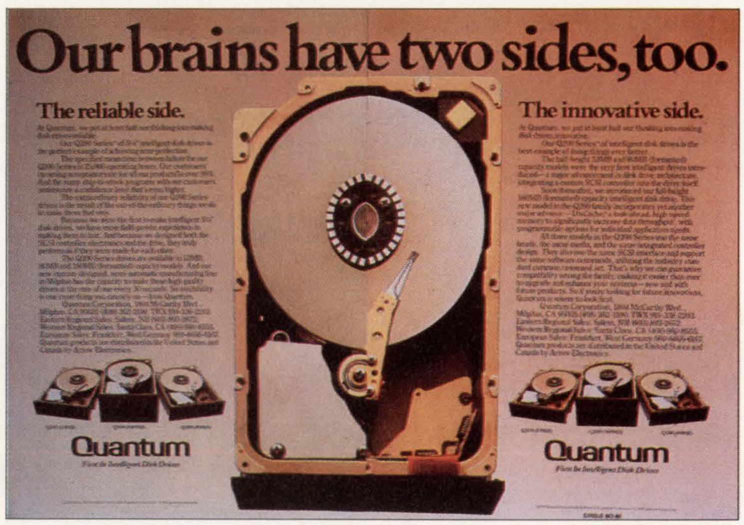

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Company: *Toshiba America, Inc.*
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"Simple, clean, to the point."
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"Visual comparison really fits the ad."
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"The design makes sense. Good, hard hitting information."
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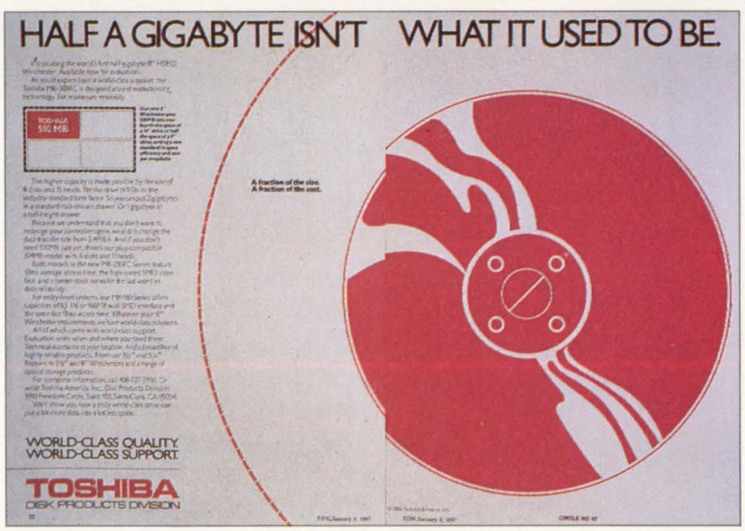
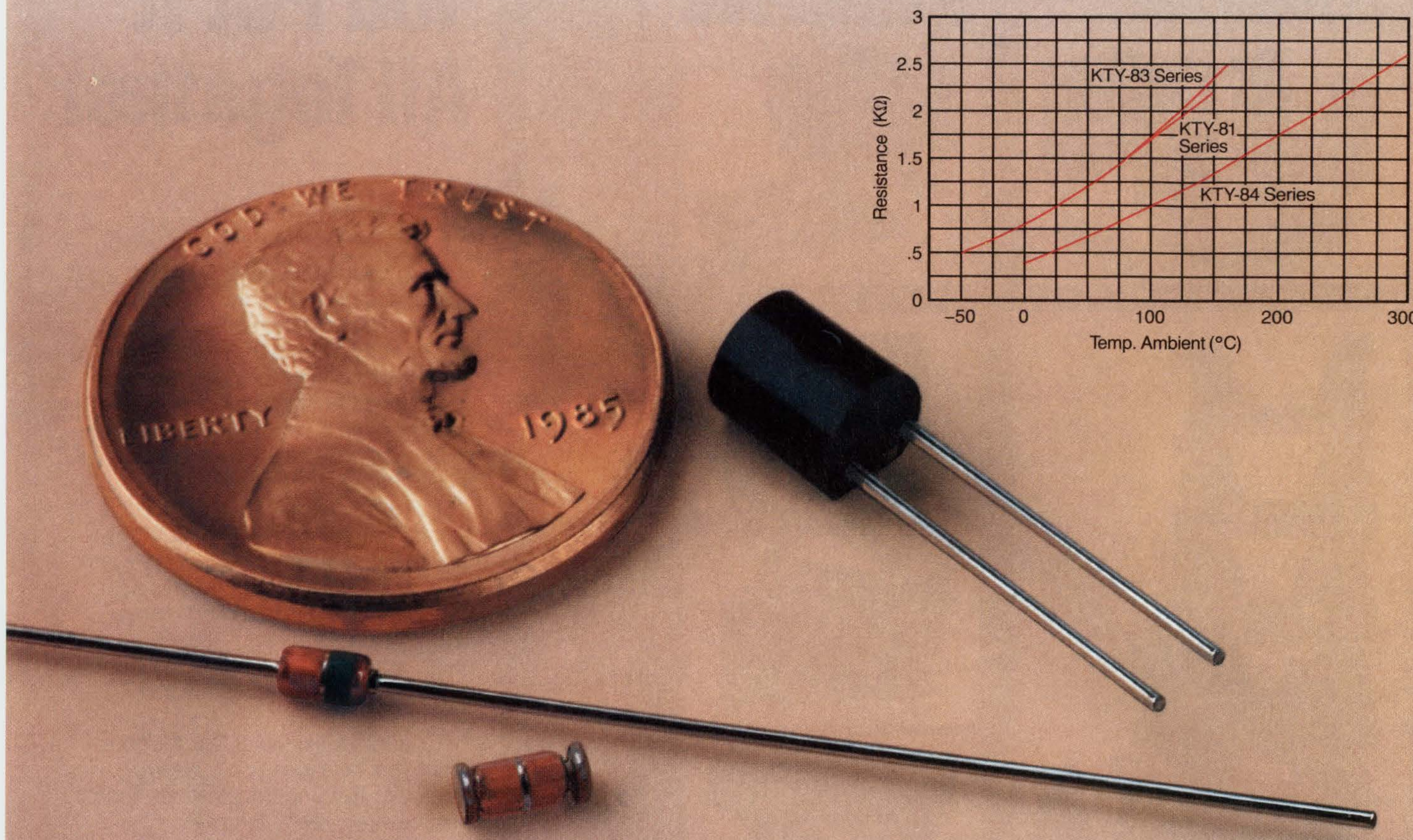
Rockwell International



Philips KTY sensors. For sensing a wider range of temperatures, for pennies.



Philips KTY silicon temperature sensors are not only attractively priced, they also monitor a wider range of temperatures than any other sensor.

Three models monitor temperature ranges from -55°C to +150°C; -55°C to +175°C; and 0°C to 300°C.

Wide operating range and excellent reproduceability are direct results of proven silicon planar technology.

By utilizing the nearly linear temperature-dependent resistivity of silicon, Philips KTY sensors can detect and respond to temperature changes in the broad ranges mentioned, with response times as fast as one second.

Exceptional accuracy of Philips KTY sensors results from a positive temperature coefficient (PTC) of 0.7 percent per degree Centigrade. They are available off the shelf in tolerances of ±1%, ±2%, and ±5%.

Because KTY sensors are small, are not polarity dependent, and need no special interfacing, they are ideal for applications involving solid-state circuitry. Configurations: plastic-encapsulated, axial lead glass bead, and surface-mounted device.

And remember, whatever the model, whatever the package, we're talking pennies.

To find out how Philips KTY sensors can fit into your measurement and control designs, call or write Amperex Electronic Corporation, A North American Philips Company, George Washington Highway, Smithfield, RI 02917. Phone (401) 232-0500; TWX 710-381-8808. In Canada contact Philips Electronics Ltd, ELCOMA Division.

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CIRCLE NO 11


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Everything For The Multibus

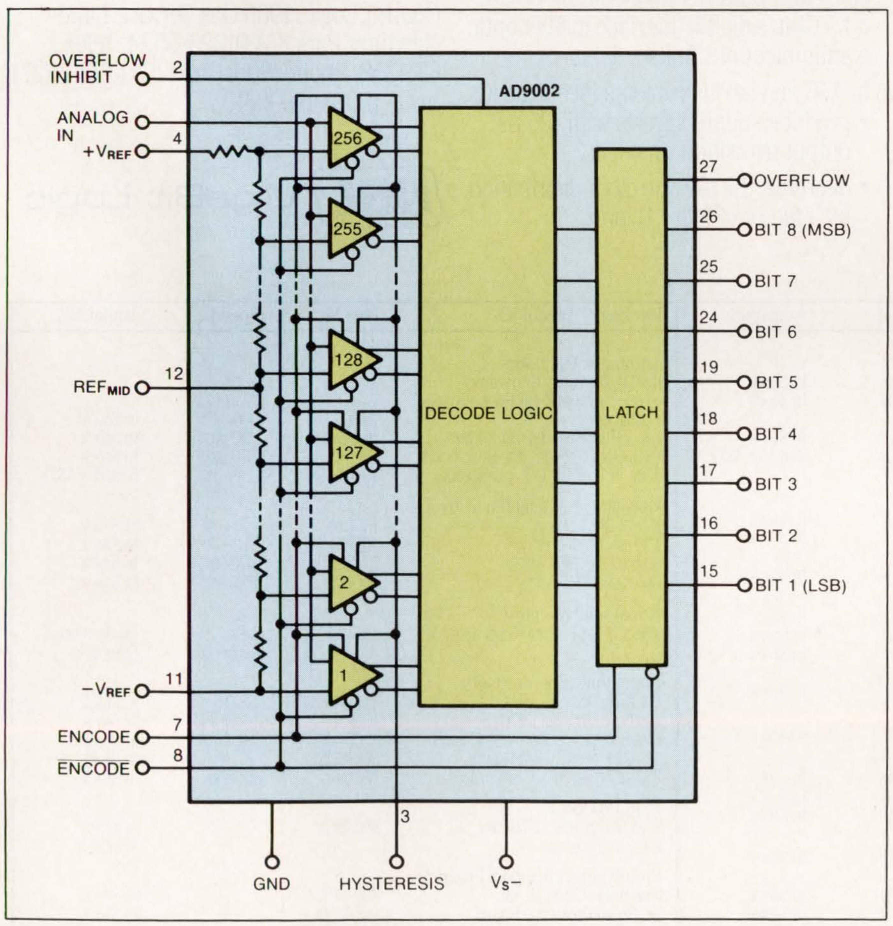
High-speed flash A/D converter features 115-MHz bandwidth, dissipates 750 mW

Fabricated in an advanced, high-density bipolar process, the AD9002 flash A/D converter features a sampling rate of 150M samples/sec and a 3-dB analog bandwidth of 115 MHz. According to the manufacturer, the converter also has the industry's lowest typical power dissipation (750 mW) and analog input capacitance (17 pF).

The AD9002 includes 256 parallel comparator stages whose outputs are decoded to drive the ECL-compatible output latches. The unusually wide analog input bandwidth of 115 MHz is a by-product of both the extremely dense bipolar process and the device's layout. This wide bandwidth, along with the high encoding rate, lets you use the part to acquire very accurate high-speed pulse inputs without using an external track/hold amplifier. The comparator's output-decoding scheme (in which the encoding cycle and the output latch both trigger on the rising edge of the encode signal) minimizes false codes, a capability that's critical for high-speed signals.

A feature that's particularly helpful in high-noise environments is the AD9002's external hysteresis-control pin, which you can use to optimize the comparator's sensitivity. The AD9002 also incorporates an overflow bit that signals over-range inputs. You can disable the overflow output by means of the overflow-inhibit pin.

Other key specifications for the converter include a signal-to-noise ratio of 43 dB at 1 MHz, harmonic suppression of 63 dB at 1 MHz and 50 dB at 40 MHz, and maximum differential linearity of 0.5 LSB. To operate, the AD9002 needs only a voltage reference, an encode signal, and a single −5.2V supply.



Featuring a sampling speed of 150M samples/sec and an analog bandwidth of 115 MHz, *the AD9002 8-bit flash A/D converter includes 256 parallel comparator stages whose outputs are decoded to drive the ECL-compatible output latches.*

The AD9002 ADC is suitable for a wide range of signal-acquisition uses that require high-speed digitization of analog and pulse waveforms. Specifically, it's useful in such applications as digital radio, ATE and digital oscilloscopes, radar guidance, laser/radar warning receivers, and electronic warfare.

The AD9002 is available with 0.5 LSB or 0.75 LSB linearity. Both of these parts come in industrial-grade (−25 to +85°C) and MIL-STD-883 Rev C (−55 to +125°C) versions. The industrial-grade parts come in 28-pin ceramic DIPs. The military grades are available in 28-pin ceramic DIPs or leadless chip carriers.

Unit pricing for the industrial-grade parts is $90 for the 0.75-LSB version and $135 for the 0.5-LSB version. The MIL-STD-883 parts are priced at $270 and $360 for the 0.75-LSB and 0.5-LSB versions, respectively. The industrial grades are available now; the MIL-STD-883 grades are scheduled for delivery in August.—***Dave Pryce***

Analog Devices, One Technology Way, Norwood, MA 02062. Phone (617) 329-4700. TWX 710-394-6577.

Circle No 729

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GBL GigaBit Logic

PicoLogic™ Digital ICs	Part No.	Speed	Availability
Gates			
Quad 3 Input NOR	10G000A	290 ps	In Stock
Quad 2 Input NOR	10G001	290 ps	In Stock
Quad Differential XOR/XNOR and Line Receiver	10G002	1.8 GHz	In Stock
5, 4, 3, 2/3, 2 Input AO/AOI	10G003	600 ps	4 weeks ARO
Drivers/Receivers/Comparators			
Dual Complementary Driver/Comparator	10G012B	1.8 GHz	In Stock
Dual 4:1 Fanout Buffer	10G011B	700 ps	In Stock
Dual Differential MUXed Fanout Buffer	10G010	1.5 GHz	In Stock
Flip Flops and Registers			
Dual Precision D Flip Flop	10G021A	2.7 GHz	In Stock
Quad MUXed Input D Flip Flop	10G023	2 GHz	In Stock
Quad XOR Input Flip Flop	10G024	2 GHz	In Stock
Octal Register/Shift Register and PN Code Generator	10G022	1.5 GHz	In Stock
Register Files			
16 x 4 3-Port Register File	10G030	1 ns	6 weeks ARO
Multiplexers/Demultiplexers			
Quad 4:1 or Dual 8:1 MUX	10G046	600 ps	In Stock
Quad 2:1 MUX	10G004	1.8 GHz	In Stock
3:8 or Dual 2:4 Decoder/DEMUX	10G044	700 ps	In Stock
Counters/Prescalers			
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4-Bit Synchronous Programmable Counter	10G061	1.6 GHz	In Stock
7-Stage Counter/Divider	10G065	3.0 GHz	In Stock
Variable Modulus Divider	10G070	2.0 GHz	In Stock

PicoLogic™ Digital ICs	Part No	Speed	Availability
Arithmetic Operators			
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Ultra-High Speed 4-Bit Adder	10G100	800 ps	In Stock
Ultra-High Speed Carry Lookahead	10G101	500 ps	In Stock
4-Bit ALU (10181 ECL equivalent)	10G181	2 ns	6 weeks ARO
Monolithic FET and Diode Arrays			
15 mA Diode Array	16G010	—	In Stock
100 mA Diode Array	16G011	—	In Stock
Single Gate FET Array	16G020	15 GHz	In Stock
Dual Gate FET Array	16G021	15 GHz	In Stock
NanoRam™ Memory			
256 x 4-Bit Pipelined Static RAM	12G014	3 ns cycle time	Production Sampling
Communication Products			
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1:8 Time Division DEMUX	10G041	1.5 Gb/s	In Stock
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Phase Frequency Comparator	16G044	1.0 GHz	In Stock
ASIC Products			
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Foundry Program	—	—	Available
Prototyping & Support Products			
Universal Prototype Kit	90GUPK	—	In Stock
Universal Prototype Board	90GUPB	—	In Stock
High Speed Socket (40L Package)	90GSKT-40L	—	In Stock

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CIRCLE NO 126

Library of voltage-vs-current functions accelerates analog-circuit simulation

By using an algorithm that interpolates parameters from electrical-data curves, the ACS circuit simulator can model devices four to 15 times as fast as Spice can. Furthermore, the simulator can model all analog devices—even ones that Spice must break into combinations of smaller components.

Simulations that use the Spice program require device models. The ACS package, however, simply extracts device parameters from measurements of electrical parameters.

To model an analog device with this simulator, you enter the current-vs-voltage, capacitance-vs-voltage, and inductance-vs-voltage functions of the device. Then, for each applied voltage in a simulation, the program consults the electrical-data files and finds the state of the device.

You can add electrical data to the simulator by performing measurements or by entering a graph. You can also use a Spice model.

The package's automodeler module translates device measurements into electrical-data files. To measure the capacitance, inductance, and resistance functions of a device, you must connect a Hewlett-Packard 4145B or 4280 test system to the company's workstation.

The simulator module runs directly from the electrical-parameter database. By using measurements supplied by the automodeler module, the simulator can provide results that are within 2% of the correct solution.

You don't need to measure every analog device that you want to simulate; the vendor offers a library of standard devices. Each standard-device file provides three sets of performance characteristics: maximum, typical, and minimum.

The library has typical resistors, capacitors, inductors, and diodes. It also includes bipolar junction transistors, junction FETs, MOSFETs, LEDs, and transformers.

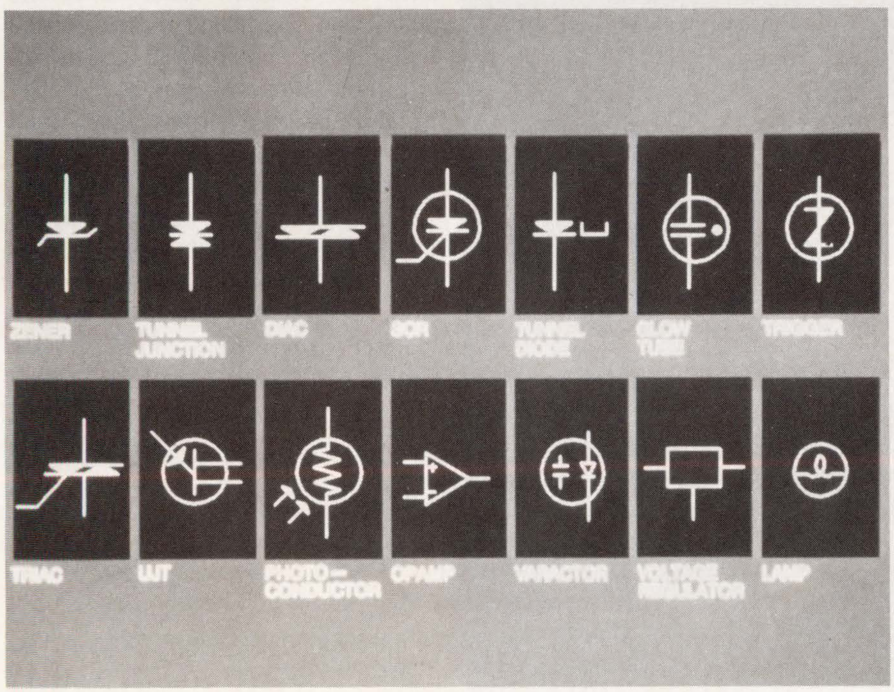
Because the simulator doesn't use device models, the ACS library can offer components that Spice-based simulations can't model. For example, the library includes zener diodes, tunnel diodes, tunnel junctions, diacs, triacs, and SCRs. Other devices included in the library are glow tubes, triggers, photoconductors, op amps, and voltage regulators.

You can set up an analog simulation the same way that you set up a simulation in a laboratory—by using a workbench. The package's software workbench module features a voltmeter, power supply, function generator, spectrum analyzer, and oscilloscope. Instead of controlling the instruments by turning knobs, you adjust the test settings with the workstation's keyboard or mouse.

ACS runs on the company's Interpro 32 ($15,000) and 32C ($25,000) workstations. The ACS automodeler and device-library modules each cost $20,000; the simulator and the workbench modules each cost $10,000.—***Eva Freeman***

Intergraph Corp, 1 Madison Industrial Park, Huntsville, AL 35807. Phone (205) 772-2000. TWX 810-726-2180.

Circle No 725



By consulting its tables of current-vs-voltage functions, *the ACS System can simulate circuits that contain such devices as SCRs, triacs, and lamps.*

16-MHz support peripherals for 80386 μP transfer system data via a 32-bit bus

Because the timing and I/O specs of the 80387, 82385, and 82380 support chips match the requirements of the 80386 μP, the four chips together form an optimized 32-bit computer. The support chips all use supersets of existing microinstruction sets, so you won't need to write new microcode. Moreover, the chips are compatible with the MS-DOS and Unix operating systems.

The 80387 accelerates floating-point calculations; the 82385 controls cache-memory functions. The 82380 Integrated System Peripheral combines DMA control with system-support functions.

The three support chips help 80386-based computers run faster. For example, because the 82380 DMA controller can use all the channels on a 32-bit bus, it eliminates I/O delays. In addition to its DMA controller, the 82380 includes a 20-level programmable interrupt controller, four 16-bit programmable interval timers, a programmable wait-state generator, dynamic RAM, a refresh controller, and system-reset control logic. This chip replaces about 20 LSI and VLSI components.

The 82385 accelerates the operation of 80386-based computers because it eliminates processor wait states. The cache-memory controller also reduces the number of bus calls to main memory. Using this chip, you can update a system's main memory after each write cycle without affecting the speed of the processor.

The 80387 also speeds system operation—it runs floating-point calculations four to six times faster than does the company's earlier 80287 floating-point coprocessor. Aside from its speed, the 80387 resembles the earlier model. The 80387 understands the same object-code instructions that the 80287 and 8087 coprocessor chips understand.

Communication between the 80386 and the 80387 is transparent to all application software. Whenever the μP needs to perform a floating-point calculation, it simply transfers the calculation to the coprocessor. The coprocessor's operation set comprises trigonometric, logarithmic, exponential, and arithmetic instructions.

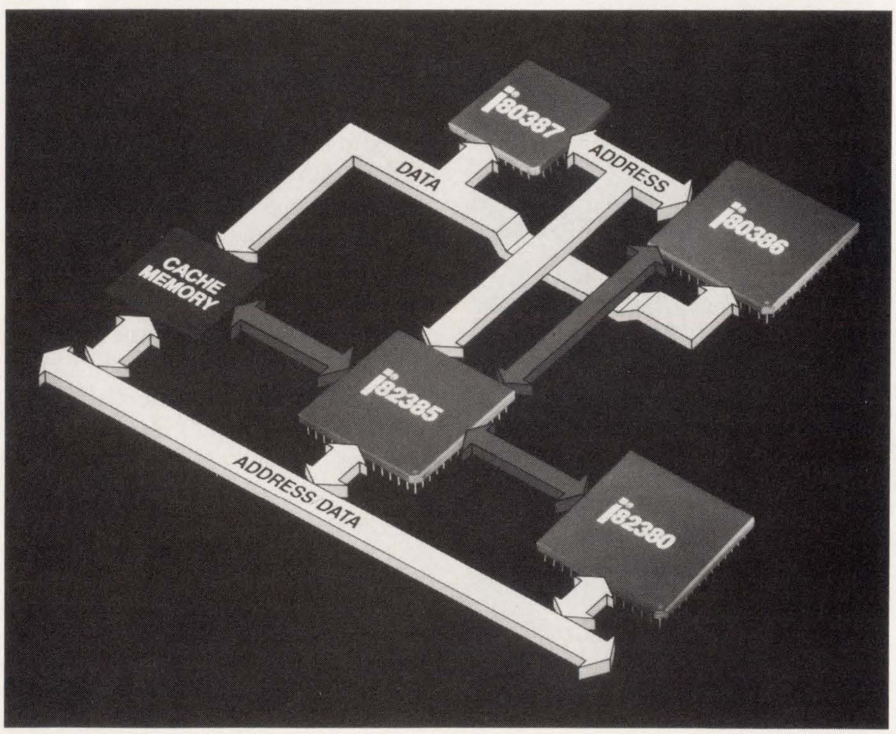
Because support chips are worthless without a fast μP, the vendor is introducing a 20-MHz version of the 80386. According to the vendor, the 20-MHz 80386 runs faster than the CPUs in Digital Equipment's VAX 8600 and IBM's 4381.

The 20-MHz 80386 is available now. The manufacturer plans to ship the 20-MHz versions of the 80387 and the 82380 in the second half of 1988; the 16-MHz models are available now. Shipments of the 16-MHz 82385 will not start until the second half of 1987; the vendor will announce the price at that time.

The 20-MHz 80386 costs $599; the 16-MHz 80387, $500. The 16-MHz 82380 costs $149; the 20-MHz version, $299 (100).—***Eva Freeman***

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone (408) 987-5730.

Circle No 726



A 20-MHz 80386 μP and its three 16-MHz support peripherals *form the core of a 32-bit computer. The support chips use the same microinstruction set that the μP uses.*

Looking for bargains in top quality peripherals? We've got your number.

Z85C30

Industry Standard SCC now in CMOS

The 8 MHz Z85C30 combines the features of its popular NMOS counterpart with the low-power benefits of CMOS.

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- Dual-channel/multi-protocol
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NOW IN 10 MHZ CMOS

$11.10*

Z8536

High integration, high value

The Z8536 CIO incorporates I/O and counter/timers in one chip.

- 2 and 1/2 parallel ports
- Three 16-bit counter/timers
- IEEE-488 compatible
- 4 handshake modes

$4.30*

Z8038

Ideal link between CPUs of different speeds

The Z8038 FIO is a skilled arbitrator with high-speed transfer logic.

- 128 x 8 asynch. bidirectional FIFO
- Bus or handshake-driven I/O
- Expandable with Z8560/Z8060

NEW LOW PRICE

$8.70*

Z9516

Offload your CPU

The Z9516 DTC is a low cost, full-feature 2-channel DMA controller.

- 16 Mbyte addressing range
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- Command chaining and pattern match logic
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Z765A

The standard FDC for PCs

Because Zilog is the volume manufacturer, the Z765A is the most cost effective FDC on the market today.

- Supports FM and MFM
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The Z7220A GDC supports high-performance computer graphics systems.

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Z9518

Encrypt/decrypt your data

The Z9518 Data Ciphering Processor is designed with three registers/master keys for improved security and throughput.

- National Bureau of Standards algorithms
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- Data rates greater than 1 Mbyte/sec
- Available in Z8068 version

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Z5380

NMOS 5380 compatible

The CMOS Z5380 SCSI Controller is the low power alternative to AMD and NCR devices – it gives you CMOS at NMOS prices.

- Standard ANSI X3T9.2 protocol
- Initiator & Target modes
- Arbitration & programmable DMA

CMOS SCSI

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CIRCLE NO 127

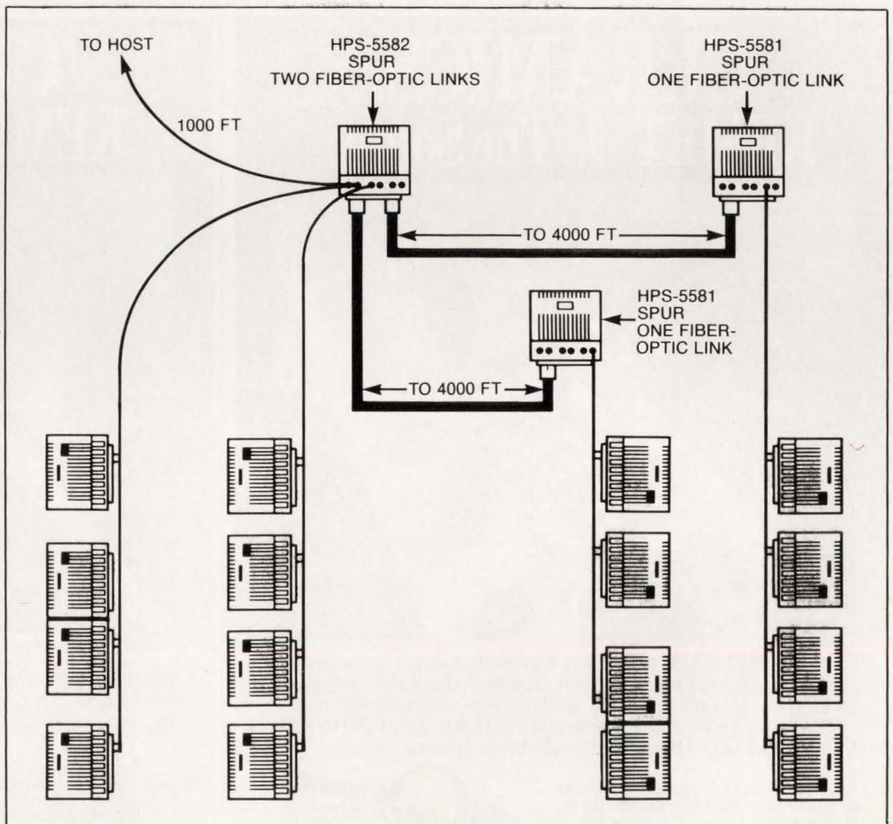
Repeaters for multiplexers stretch host/terminal lines

Users of the HPS distributed communication subsystem family of multiplexers can now spread clusters of RS-232C terminals over cable distances of as much as three miles by using Spurs (Systech Pluriaxial Unplug Repeaters).

The Spurs come in three versions: The HPS-5580 Spur has six coaxial connectors, the HPS-5581 has six coaxial connectors and one fiber-optic connector, and the HPS-5582 has six coaxial connectors and two fiber-optic connectors. Mixing the three different Spur products in a system allows you to use fiber-optic cable to provide electrical isolation and to increase the distance between the host and the terminals.

By using the Spurs in conjunction with the company's HPS host adapters and cluster controllers, designers of multiuser Multibus I-, Multibus II-, and VME Bus-based systems can simplify the cabling connecting hosts and RS-232C terminals. An HPS communication subsystem includes an intelligent host-adapter board that offloads system I/O functions from the CPU. Instead of providing direct connections to multiple terminals, the HPS host adapter provides a LAN connection at the host computer's back panel.

The LAN used by the HPS multi-

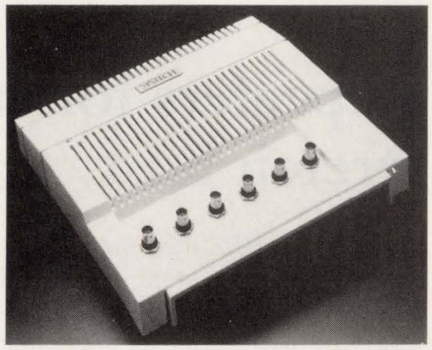


A combination of coaxial and fiber-optic links *between the HPS-5581 and HPS-5582 repeaters (Spurs) and HPS cluster controllers provides electrical isolation and flexible fan-outs to terminals. The Spurs also allow you to extend your computer-communication links to as much as three miles.*

plexers operates transparently to the user and connects to the cluster controllers via a single coaxial cable. The cluster controllers each serve 8 or 16 RS-232C terminals with traditional serial cables. The LAN employs a token-passing concept, similar to Arcnet, that allows each terminal to operate at 9600 baud. The cluster controllers can be daisy-chained, and the last one can be as far as 1000 ft from the host.

Because the LAN connects the various cluster controllers (sometimes via Spurs) in a virtual circle, the physical configuration of Spurs and cluster controllers does not affect the operation of the LAN. Theoretically, Spurs could connect 254 clusters, but at present the host-adapter firmware supports only 128 terminals.

The Spur products provide even more flexibility in implementing an I/O subsystem. You can connect a 5580 Spur to a host adapter, employ a 5580 as a repeater, or use a 5580 to provide coaxial cable connection to five cluster controllers, or you can do all three. If you don't connect cluster controllers between Spurs, the Spurs can be as far apart as 1500 ft; if you do connect clusters between the Spurs, the Spurs can be 1000 ft apart. The coaxial link between a host adapter and a Spur is limited to 1000 ft.



Allowing you to place terminals three miles from the host, *the HPS-5580 family of repeaters provides flexibility in distributed-communication-subsystem multiplexer schemes.*

The fiber-optic links connecting two Spurs can be as long as 4000 ft; you must link the fiber-optic connectors of the first 5581 or 5582 only with the fiber-optic connectors of the other 5581 or 5582. Further, you can't connect cluster controllers directly to an optical link; you must connect them to a coaxial connector.

All three Spur models are immediately available. Models HPS-5580, HPS-5581, and HPS-5582 cost $610, $1505, and $2205 (100), respectively. The same cluster controllers and Spurs work with Multibus and VME Bus host adapters.—***Maury Wright***

Systech Corp, 6465 Nancy Ridge Dr, San Diego, CA 92121. Phone (619) 453-8970. TLX 4990507.

Circle No 728

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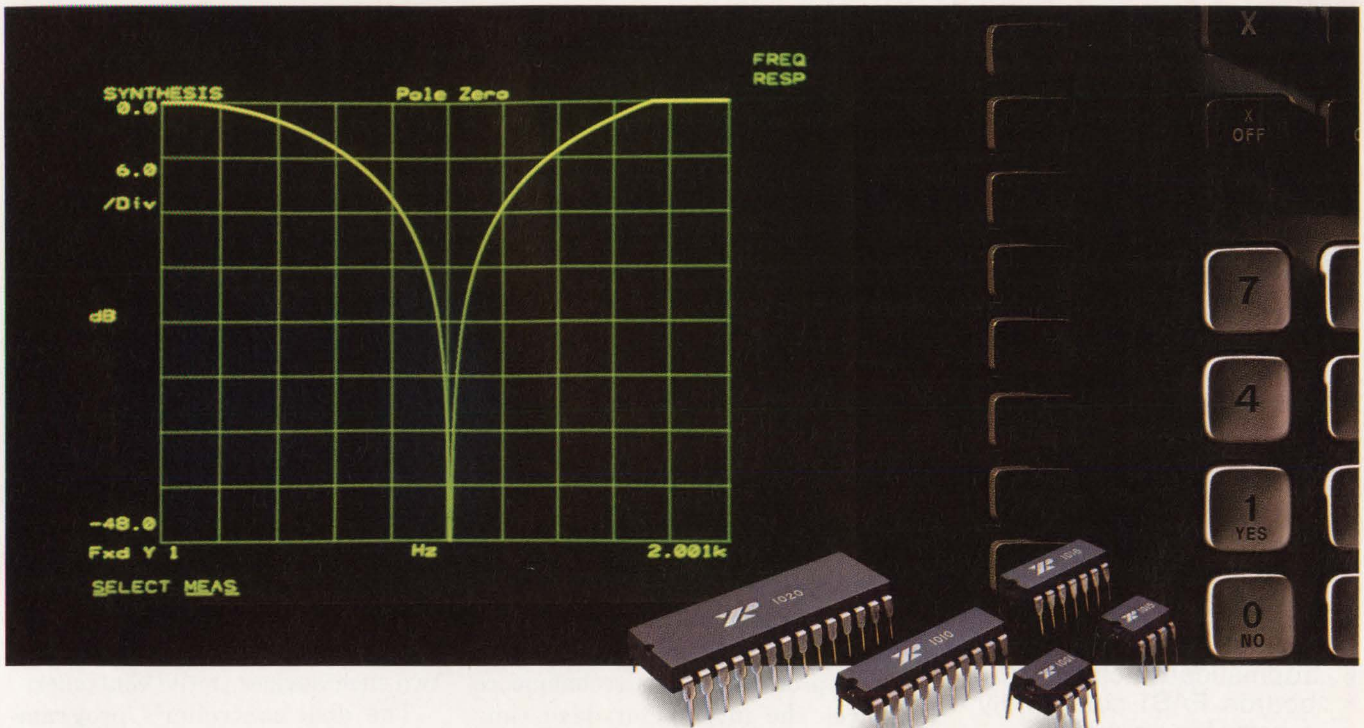

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EXAR filters give you the edge that no competition can match:

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- Lower Clock Feedthrough Voltage
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- Low Output Offset Voltage

THE EXAR FAMILY OF FILTERS

GENERAL PURPOSE FILTERS

	DEVICE	AVAILABILITY
XR-1015	7th-order Elliptic Lowpass Filter	NOW
XR-1016	7th-order Elliptic Lowpass Filter with two uncommitted operational amplifiers	NOW
XR-1010	Dual Second-order Switched Capacitor Building Block	NOW
XR-1020	Datacommunication Instrumentation Filter 10 filters used to Characterize the Phone Line	NOW
XR-1001	Fourth-order Lowpass Filter: Butterworth 100:1	NOW
XR-1002	Butterworth 50:1	NOW
XR-1003	Fourth-order Lowpass Filter: Bessel 100:1	NOW
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Available soon in military grade.

MODEM FILTERS

Device	Application	Type	Speed (BPS)	Technology	Features
(Filters) XR-2120	Bell 212A	PSK/ FSK	1200/300	CMOS	Low external component Small package (.4" wide, 22 pin)
XR-2126	Bell 212A/ CCITT V.22 CCITT V.22 bis	PSK/ FSK	1200/300/ 2400	CMOS	AMI S35212 compatible Reticon RM5632A compatible Call Progress monitoring
XR-2127	Bell 212A/ CCITT V.22 CCITT V.22 bis	PSK/ FSK	1200/300/ 2400	CMOS	AMI S35212A compatible ALB test mode Call Progress monitoring
XR-2128	Bell 212A/ CCITT V.22 CCITT V.22 bis	PSK/ FSK	1200/300/ 2400	CMOS	ALB test mode Enhanced Call Progress monitoring (fo/2.5)
XR-2129	Bell 212A/ CCITT V.22 CCITT V.22 bis	PSK/ FSK	1200/300/ 2400	CMOS	Designed to complement XR-2121/XR-2122/XR-2125 1.8432 MHz onboard oscillator Additional worst case line equalizer ALB test mode

EXAR offers you the quality and customer support needed for your filter applications. In addition, EXAR can address your specific filter requirements with **customized switched capacitor solutions.** Utilize our years of engineering expertise and know how in filters. Call or write EXAR for your filter needs. 750 Palomar Avenue, Sunnyvale, CA 94086 Tel. (408) 732-7970.

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Application ________

EXAR

750 Palomar Avenue, Sunnyvale, CA 94086 Tel. (408) 732-7970 TWX 910-339-9233

CIRCLE NO 128

VME Bus disk controller has 2.4M-byte/sec access time

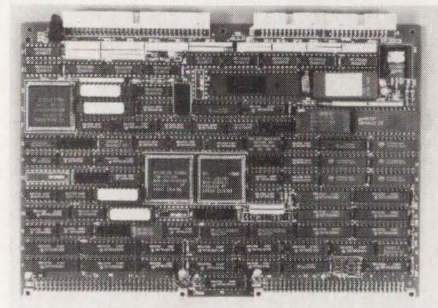
The 752 H-SMD disk controller uses an 8k-byte FIFO buffer, read-ahead techniques, and a proprietary sector-packetizing scheme to achieve a disk-transfer rate of 2.4M bytes/sec. According to the manufacturer, the controller exhibits a peak DMA rate of 18M bits/sec and an aggregate, or weighted average, rate of approximately 10M bits/sec.

The VME Bus disk controller uses a scheme the manufacturer calls "Dynathrottle" to create packets of as many as six disk sectors, which are then sent via DMA to the host processor. This technique reduces the intersector dead time, which can account for as much as 50% of the time required for data transfer between a disk and the host. The size of the packets is determined in part by the amount of data accumulated in the controller's onboard FIFO buffer, which operates as a cache for disk data.

The Dynathrottle scheme also allows you to use software to regulate the size of packets. For example, if you wish to emphasize fast disk-access time, you can use a large packet size; if you want to distribute bus time more evenly among the devices on the VME Bus, you can use smaller packets.

In conjunction with the Dynathrottle technique and the 8k-byte onboard FIFO buffer, the 752 employs a read-ahead technique. The controller reads ahead on the disk until the FIFO buffer is filled. Because most file systems require a number of sequential sections, this read-ahead technique provides a high hit rate, even for multiple block reads.

The disk controller supports any 5¼- to 14-in. SMD-interface drive having transfer rates from 1M to



By employing read-ahead and sector-packetizing techniques, *the 752 single-board disk controller achieves an aggregate DMA transfer rate of 10M bits/sec.*

2.4M bytes/sec. You can attach any two such devices to the controller.

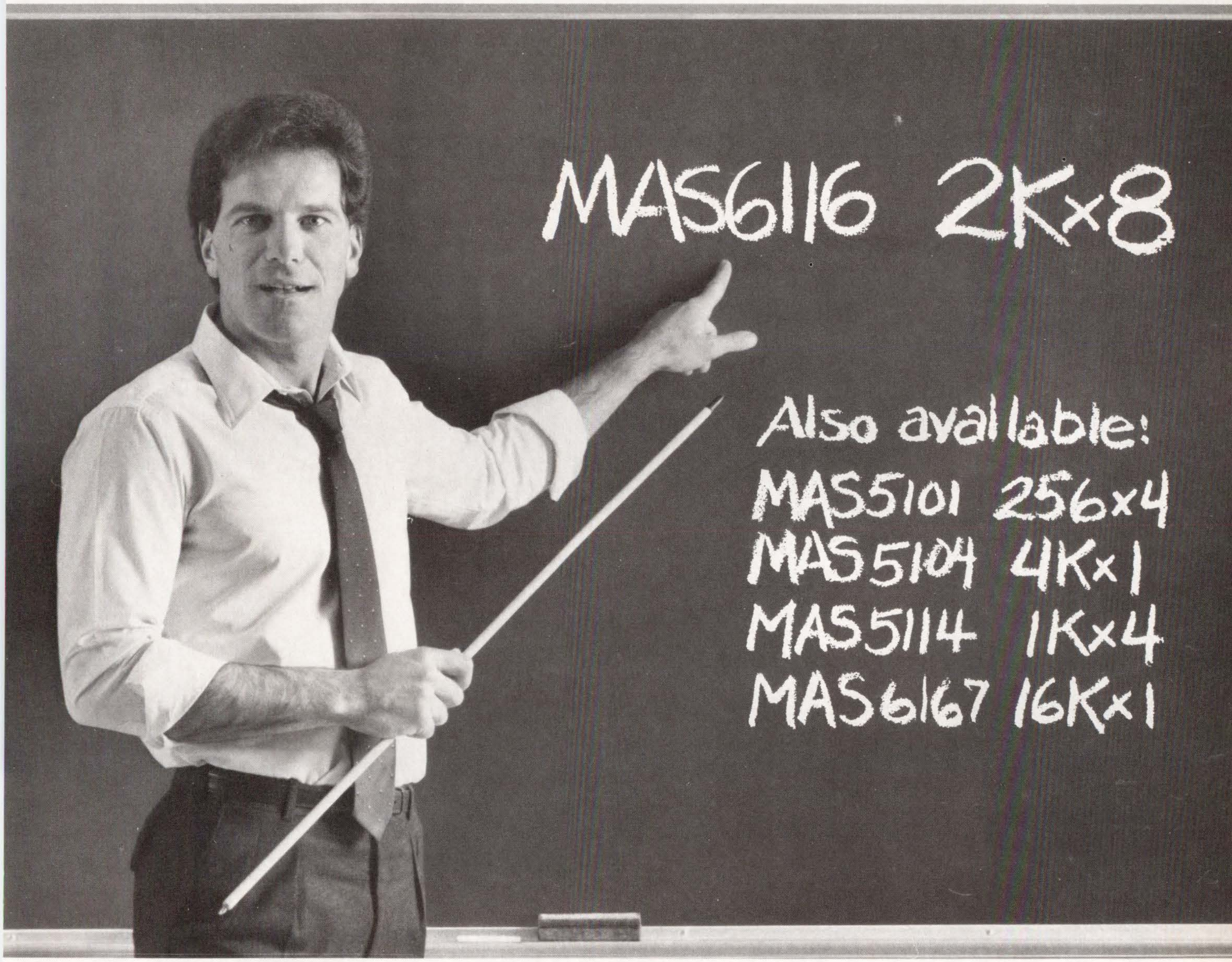
The disk controller's programmable interrupt levels, vectors, and address modifiers allow it to support multiple processors. The 752 also supports both 32- and 48-bit error-detection and -correction schemes. The board costs $2695.

—Jim Wiegand

Xylogics Inc, 144 Middlesex Tpk, Burlington, MA 01803. Phone (617) 272-8140.

Circle No 727

It takes a year to get these SOS RAMs—true or false?



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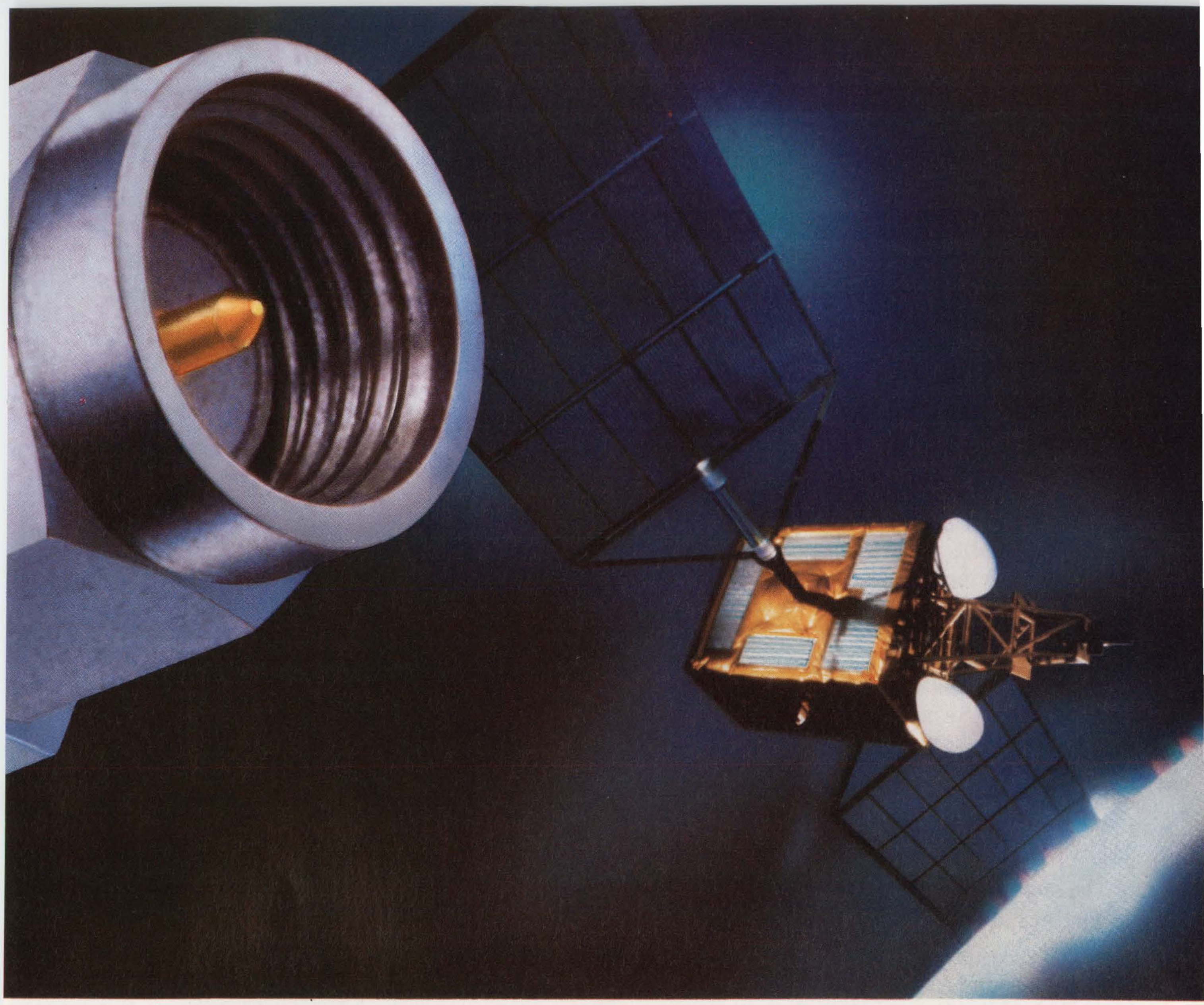
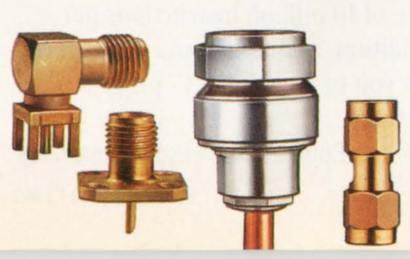
CIRCLE NO 15

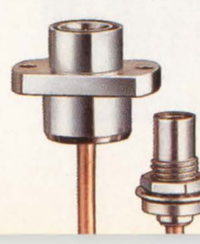
Crimp performance story. 26 GHz, and economy too.





Panel/bulkhead jacks and adaptors for easy mating with other configurations.

CIRCLE NO 129



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- Physical Modeling Engine: This engine simulates

introduces AE workstation.

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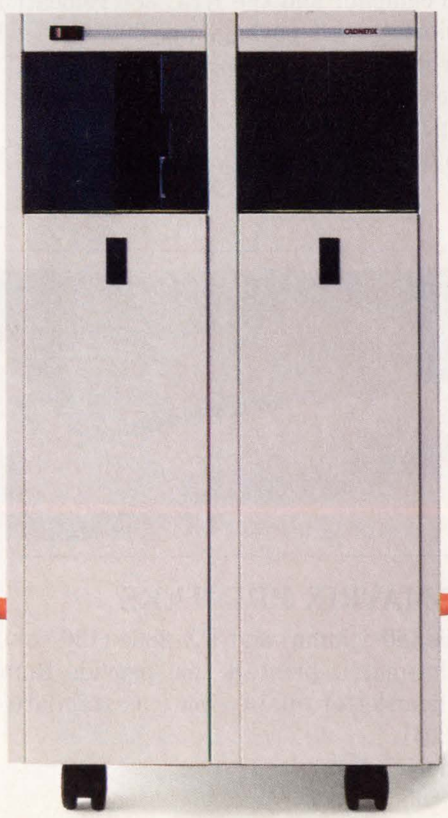

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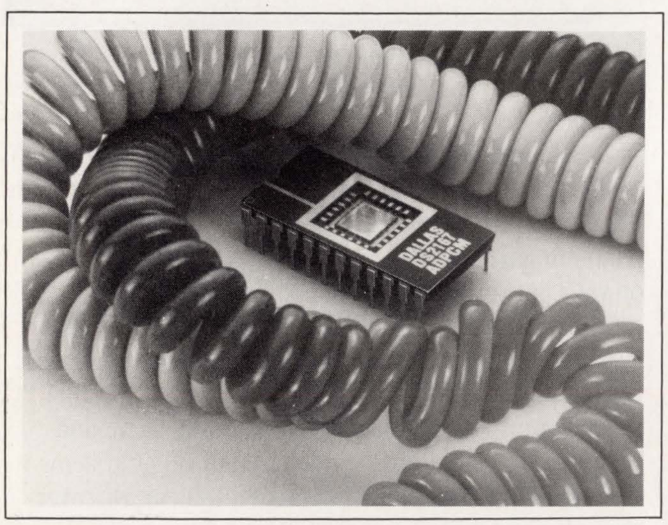
READERS' CHOICE

Of all the new products covered in EDN's **March 4, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **March 4, 1987,** issue.

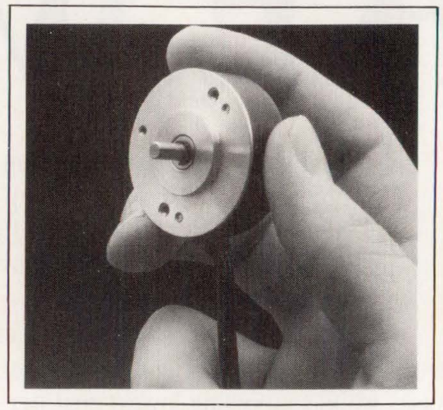
▲ DIGITAL PATTERN GENERATOR

The DataSource-8600 is a hardware/software package that turns an IBM PC or compatible computer into a low-cost, high-performance digital pattern generator, recorder, and analyzer (pg 99).
Analytic Instruments Corp.
Circle No 603



▲ VOICE-COMPRESSION CHIP

The DS2167 combines a digital signal processor with an algorithm known as Adaptive Differential Pulse Code Modulation on a single chip. The result is a 32k-bps voice-transmission rate, which doubles the capacity of T1 lines (pg 104).
Dallas Semiconductor Inc.
Circle No 601

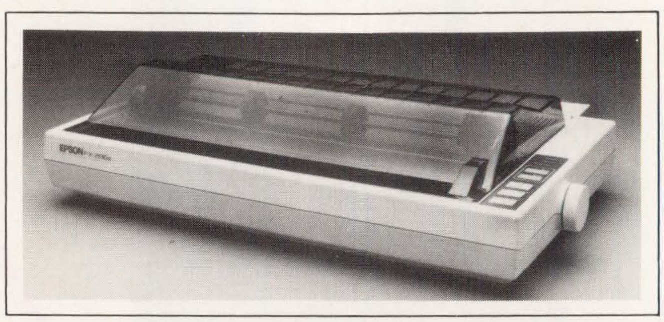


▲ ROTARY ENCODER

The Model RE10 magnetic rotary encoder bridges the gap between industrial encoders and open-frame kits. The compact, lightweight device is impervious to environmental hazards (pg 100).
National Machine Systems Inc.
Circle No 602

C COMPILER

The C 386 compiler and the RLL 386 relocation, linkage, and library tools package are 80386 software-development tools that run on the IBM PC/AT or compatibles (pg 203).
Intel Corp.
Circle No 604



▲ DOT-MATRIX PRINTERS

The FX-86e (80-column) and FX-286e (136-column) are 9-pin dot-matrix printers that provide Roman and sans serif near-letter-quality fonts as standard features (pg 204).
Epson America Inc.
Circle No 605

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ISDN INTERFACES

Primary Rate Interface for direct connection to 1.544 (23B + D) or 2.048 (30B + D) Mbps ISDN interface

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FINISHED SIMULATION AND ANALYSIS APPLICATION PACKAGES

- X.25 Official Qualification Procedures as used for the Department of Defense DDN Network
- X.75 Certification Procedures developed for interoperability testing by a major Bell Operating Company
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- Real Time display of interpreted traffic
- History display of interpreted traffic from the acquisition buffer
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COMPATIBILITY

Upward compatibility with Chameleon and Chameleon II applications allows you to run and expand existing test solutions on the Chameleon 32.

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With Tekelec's "C" programming capabilities for the Chameleon 32, you can write application specific programs tailored to your individual needs. Tekelec's "C" Programming Package includes specific libraries written by Tekelec for HDLC, SDLC and LAPD.

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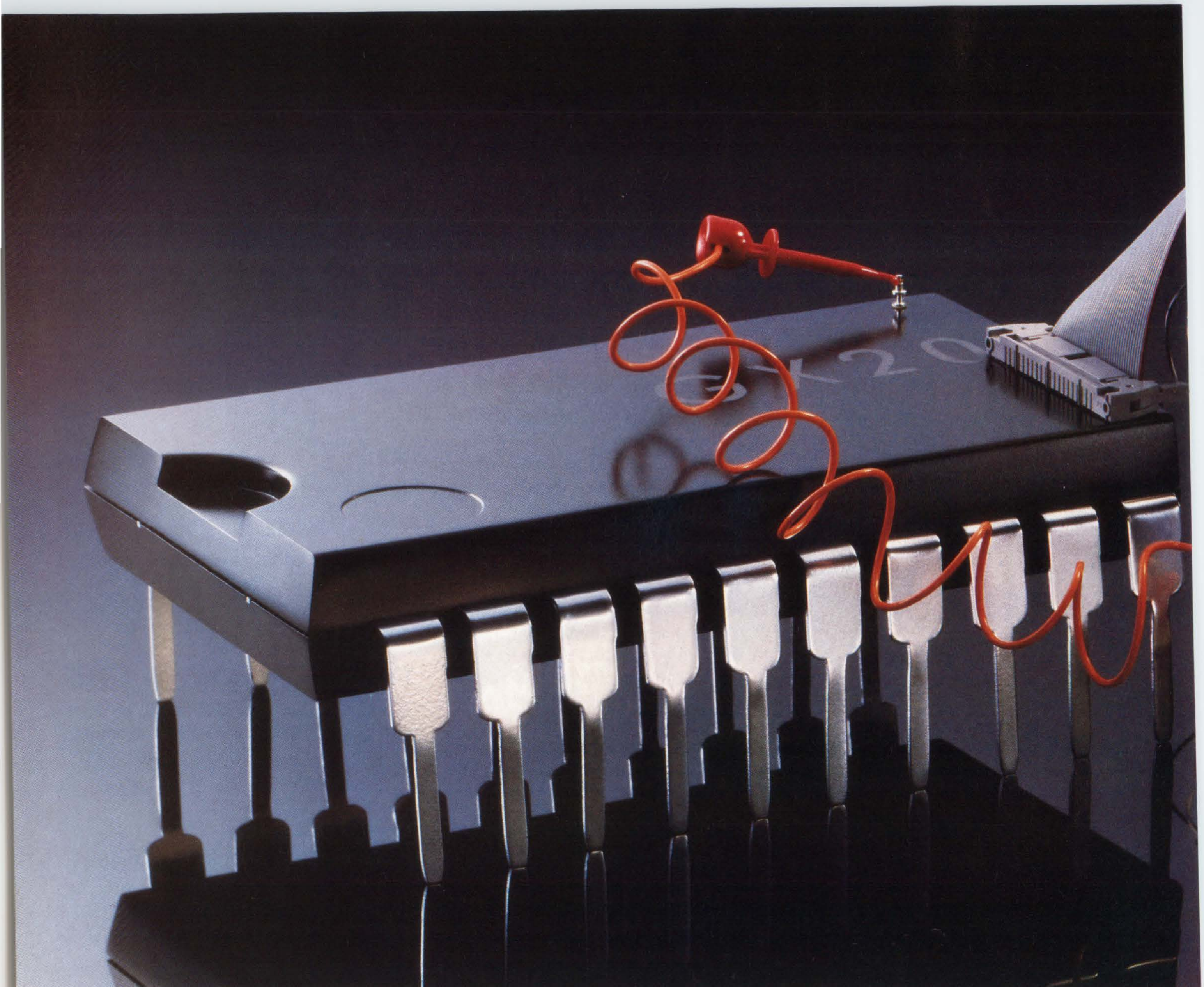


You wouldn't do this with your Analog VLSI devices.

You'll have to if you go to most ATE companies for a solution to today's sophisticated "system silicon" testing problems. Because all you'll get is a make-shift tester. And that means resigning yourself to man-months of custom hardware work integrating analog and digital instrumentation. And putting up with the long hours of low-level software development that go with custom solutions. Worse, you can expect these delays to cut your chances of getting your product to market on time.

Teradyne now has a simple answer to this complex testing problem. The A500 Analog VLSI Test System. It's the first of a new generation of systems specifically for AVLSI "system silicon" devices. A test system that can help you cut critical product development time by months or even years.

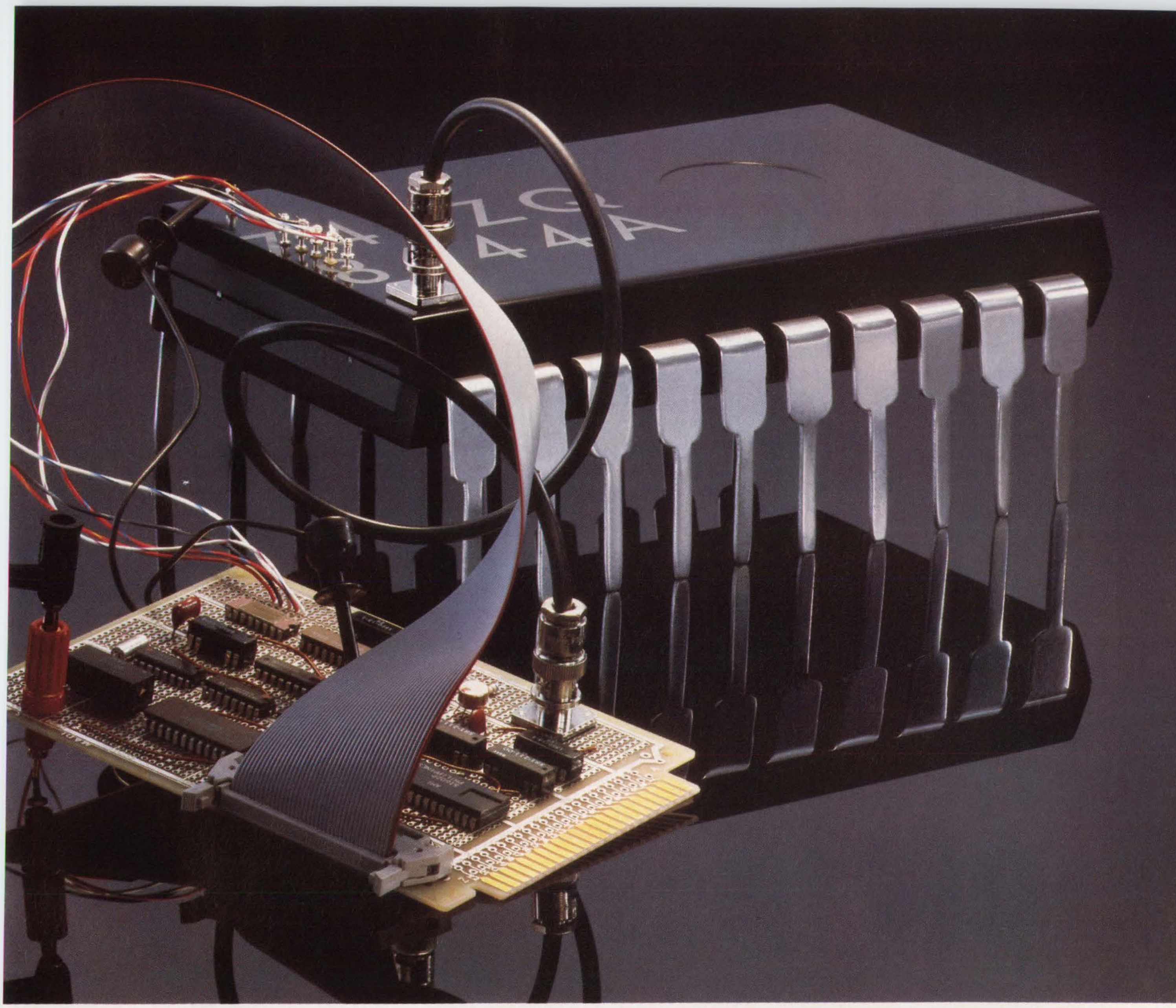
One Test System, Once and for All

With AVLSI devices you won't get fast design feedback, unless you test individual components—the "building blocks" of system silicon. And you won't comply with customer and industry requirements if you don't do complete "system" functional testing. With conventional test systems it means two of everything. Two testers, two test programs, two insertions, two data bases. And more than twice the time to get to market.

The A500 allows you to do it all with one system. So there's only one system to program. One insertion to make for both component and functional testing. And only one data base to work with. Which means significantly less time to market.

Vector Bus II™: the Great Integrator

The heart of the A500 is Teradyne's unique Vector Bus II architecture. It integrates analog and digital VLSI test capability at the system level. Which means you won't have to build special applications hardware for every new device you design. Vector Bus II eliminates that costly custom-work bottleneck



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LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	29	57	14	0	0	7.6	8.6
Pot-Core	0	25	63	12	0	0	7.7	9.6
Laminate (power)	11	28	61	0	0	0	5.7	8.1
CONNECTORS								
Military panel	0	40	40	20	0	0	7.5	10.8
Flat/Cable	20	47	27	6	0	0	4.6	6.6
Multipin circular	13	12	25	50	0	0	10.1	7.3
PC	20	30	50	0	0	0	4.9	6.4
RF/Coaxial	17	33	50	0	0	0	5.0	7.9
Socket	30	45	15	10	0	0	4.1	4.5
Terminal blocks	29	53	18	0	0	0	3.0	4.3
Edge card	36	14	43	7	0	0	5.0	6.0
Subminiature	33	22	45	0	0	0	4.2	6.2
Rack & panel	29	18	43	0	0	0	4.3	5.5
Power	20	50	30	0	0	0	3.9	5.4
PRINTED CIRCUIT BOARDS								
Single-sided	0	82	18	0	0	0	3.9	6.0
Double-sided	0	46	54	0	0	0	5.7	6.1
Multilayer	0	27	67	6	0	0	7.2	8.7
Prototype	9	81	10	0	0	0	3.2	4.9
RESISTORS								
Carbon film	48	28	24	0	0	0	2.8	5.0
Carbon composition	50	29	14	7	0	0	3.1	5.3
Metal film	47	21	21	11	0	0	3.9	6.2
Metal oxide	33	33	34	0	0	0	3.7	5.4
Wirewound	12	47	35	6	0	0	5.1	6.9
Potentiometers	22	35	30	13	0	0	5.5	6.8
Networks	36	21	21	22	0	0	5.7	7.9
FUSES	50	28	22	0	0	0	2.6	4.1
SWITCHES								
Pushbutton	24	33	29	9	5	0	6.0	5.5
Rotary	19	25	44	12	0	0	6.2	7.3
Rocker	29	43	21	7	0	0	4.1	4.6
Thumbwheel	10	40	40	10	0	0	6.0	6.4
Snap action	25	17	42	8	8	0	7.3	5.1
Momentary	10	40	30	10	10	0	7.7	7.4
Dual in-line	20	40	20	0	20	0	7.9	6.8
WIRE AND CABLE								
Coaxial	36	37	18	9	0	0	4.0	4.8
Flat ribbon	39	44	11	6	0	0	3.1	5.0
Multiconductor	44	19	37	0	0	0	3.6	4.8
Hookup	64	27	9	0	0	0	1.5	1.9
Wire wrap	73	18	9	0	0	0	1.3	2.8
Power cords	18	47	29	6	0	0	4.7	4.5
Other	0	0	100	0	0	0	8.0	6.0
POWER SUPPLIES								
Switching	12	31	38	19	0	0	6.8	9.4
Linear	10	40	40	10	0	0	6.6	8.6
CIRCUIT BREAKERS	15	31	39	15	0	0	6.4	5.4
HEAT SINKS	26	63	11	0	0	0	2.7	6.0

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	30	35	25	10	0	0	4.6	5.6
PC board	10	42	32	16	0	0	6.2	7.9
Dry reed	0	50	38	12	0	0	6.4	7.9
Mercury	0	33	67	0	0	0	6.3	10.1
Solid state	13	27	47	13	0	0	6.6	7.9
DISCRETE SEMICONDUCTORS								
Diode	42	23	31	4	0	0	3.8	6.3
Zener	41	18	29	12	0	0	4.7	6.9
Thyristor	13	37	38	12	0	0	6.1	8.3
Small signal transistor	31	23	38	8	0	0	5.0	7.6
FET, MOS	29	36	21	7	7	0	5.7	6.9
Power, bipolar	17	50	33	0	0	0	4.2	6.4
INTEGRATED CIRCUITS, DIGITAL								
CMOS	24	38	29	9	0	0	4.9	7.1
TTL	36	27	32	5	0	0	4.1	6.3
LS	35	35	25	5	0	0	3.8	6.8
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	8	33	42	17	0	0	6.9	8.2
OP amplifier	23	15	54	8	0	0	6.0	7.3
Voltage regulator	20	30	45	5	0	0	5.3	6.6
MEMORY CIRCUITS								
RAM 16k	25	42	33	0	0	0	3.9	7.1
RAM 64k	25	42	25	8	0	0	4.5	5.8
RAM 256k	27	46	18	9	0	0	4.2	8.2
ROM/PROM	27	46	27	0	0	0	3.5	6.7
EPROM	25	44	12	19	0	0	5.2	6.0
EEPROM	20	40	40	0	0	0	4.4	8.5
DISPLAYS								
Panel meters	10	30	50	10	0	0	6.5	8.2
Fluorescent	20	20	20	40	0	0	8.4	11.2
Incandescent	0	25	75	0	0	0	6.8	8.6
LED	25	25	40	10	0	0	5.5	6.4
Liquid crystal	12	31	38	19	0	0	6.8	9.6
MICROPROCESSOR ICs								
8-bit	29	28	43	0	0	0	4.3	7.8
16-bit	40	20	40	0	0	0	3.8	8.2
FUNCTION PACKAGES								
Amplifier	33	17	33	17	0	0	5.8	11.8
Converter, analog to digital	11	33	45	11	0	0	6.3	7.0
Converter, digital to analog	14	14	57	15	0	0	7.2	7.7
LINE FILTERS	22	22	56	0	0	0	5.1	8.3
CAPACITORS								
Ceramic	42	26	26	6	0	0	3.7	4.9
Ceramic monolithic	41	29	24	6	0	0	3.7	4.6
Ceramic disc	47	29	18	6	0	0	3.2	4.1
Film	44	11	45	0	0	0	3.9	5.0
Electrolytic	25	35	25	15	0	0	5.4	5.2
Tantalum	26	35	35	4	0	0	4.5	6.3
INDUCTORS	12	38	38	12	0	0	6.1	7.6

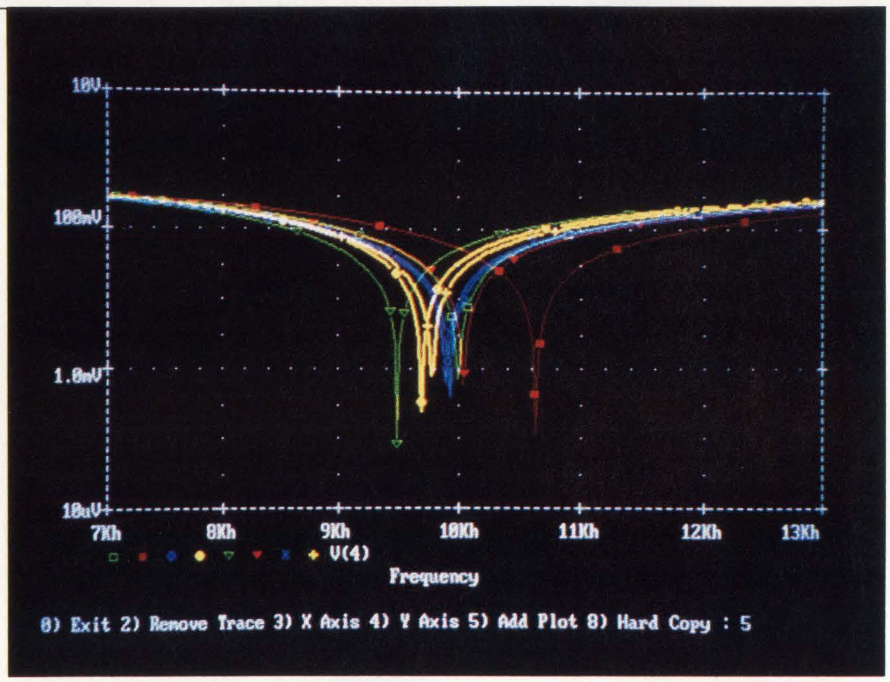
Source: *Electronics Purchasing* magazine's survey of buyers

HIGH PERFORMANCE ASICs

Analog CAE packages are steadily improving. Selecting one isn't easy, however. What's more, you might find it difficult to decide when the use of such systems is appropriate.

Board-level analog CAE

Special Report



Using Monte Carlo analysis *to determine the effect of component variations on circuit operation, MicroSim's PSpice can help you create designs that are tolerant of manufacturing inconsistencies.*

David Shear, *Regional Editor*

Selecting an analog CAE system can prove to be difficult and time consuming. You won't find benchmarks that enable you to readily compare the relative performance of systems like those listed in **Table 1** on pg 142. You'll have to balance such factors as the hardware the system requires, the circuit simulator it employs, and, of course, the cost. In addition, you'll have to evaluate such subjective criteria as the friendliness of the user interface and the importance to you of any high-level design aids (like behavioral modeling) the system might offer.

The packages range from low-cost personal-computer-based versions to ones costing $50,000 and more that run on minicomputers or mainframes. You might find use for systems at each end of this spectrum: A Spice derivative that runs on a PC might be best for obtaining a first look at a design's behavior; for more accuracy, you can later employ the more complex models of a more expensive CAE system.

Know when to use a system

But knowing *which* system to select isn't the only difficulty you'll face in adopting computer-aided analog design. Completing an accurate design on schedule will depend on your ability to know *when*

Computer simulations meet the real world *in today's sophisticated analog CAE packages. Features like behavioral modeling can prove to be invaluable when you need to model electromechanical equipment. You can't readily describe such equipment in a form that an electronic-device simulator like Spice can understand. (Photo courtesy Analogy)*

to use the system you do buy, which, after all, will be only one of many design tools at your disposal. Although many such systems offer features like virtual instruments, the systems don't replace scopes and soldering irons: You'll find times to use the analog CAE system, but at other times you'll remain at the bench. To effectively use the CAE tools, you'll have to develop the skills to know when each tool is appropriate.

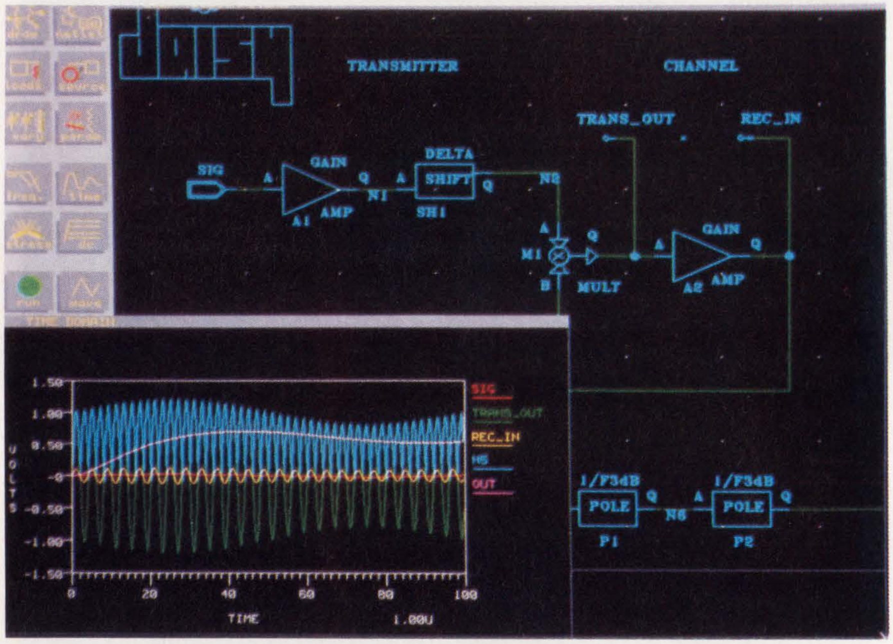
The ambiguity attendant to the selection and application of analog CAE systems mirrors the ambiguities of analog design itself. When you begin an analog design project, you can employ a textbook approach to develop an idealized analog model that meets your design goals, but when you substitute real components for your ideal models, you'll often as not find that parasitic effects preclude the results you wanted. You must then modify the circuit in an effort to achieve the desired goal.

No substitute for reality

Traditionally, such modifications have involved expensive, time-consuming pc-board rework. With an analog CAE system, you can quickly accomplish some of the manipulations involved in minimizing unwanted real-world effects before you ever sit down at the bench with a hand-wired prototype, but no system can model all of the par-

Compare available products with your notion of what an ideal analog CAE system should do.

Functional descriptions allow you *to quickly enter complex circuits without having to design each of the individual pieces. Daisy offers a library of functional descriptions. You can play what-if games at a very high level to check the architecture of your design before getting into the details of the component-level design.*



asitic elements that might influence a pc board's operation. Eventually, you must build the real-world device and see how it reacts. Nevertheless, judicious use of automated tools can help ensure that your first prototype comes close to meeting your original design goals.

You might begin the process of selecting an analog CAE package by imagining a version of the ideal analog CAE system (see **box,** "The ideal analog CAE system") and comparing the available products to your ideal. You can begin your comparison using **Table 1**; as a next step, you can evaluate the demos that many vendors offer. Demos help you determine if a program accepts and displays data in a format you are comfortable with.

Evaluating a demo should be one step in product selection, but it should never be your only step. Demos are invariably impressive, but quite often the displays you see are created from a file of precalculated data. Such demos don't actually run the vendors' simulators, for example, so the speed of screen update is not indicative of the systems' real-time response.

Use the system you might buy

Therefore, when you've made a tentative purchasing decision, use the system you plan to buy in an actual design. A short design session can help you determine not just how well the system works but also how well you work with the system. If you schedule such a session, be sure to explain to the CAE vendor in advance what you want to do so the vendor can be prepared to help you: Keep in mind that you won't be an expert in the operation of the system you're evaluating when you begin the session; you'll have to rely on the vendor to filter the instructions necessary for your test design from the system's documentation. Should you buy a particular vendor's product, you would be well advised to attend the classes that the vendor offers so that you can begin to master all the capabilities of what is probably a complex system.

The capabilities that you'll find as you evaluate the packages range from behavioral modeling, which lets you evaluate a design concept, to parameter-variation analysis, which lets you evaluate a design at the component level.

Behavioral modeling is useful because the vast majority of analog systems interact with an electromechanical device: a motor or a sensor, for example. You can't readily describe such devices in terms that standard analog modeling programs (Spice and its derivatives) can understand, but CAE systems that offer behavioral modeling allow you to use what vendors call templates to simulate any analog system that you can describe with a set of mathematical equations.

When you represent a system behaviorally, you're using a top-down methodology to create a design. First, you describe the entire system by defining the behavior of the various black boxes that make up the design. Once the high-level design functions properly, you begin the detailed design of the first black box. You design and simulate this black box separately from the entire system; then, you test the completed black box within the entire system, verifying that it performs its required function. You then progress to the other black boxes until the entire system has been designed and the system simulation is working.

You will also find it useful to be able to functionally describe the system you are designing. A feature that vendors call "functional description" allows you to implement a high-level representation of a functional block like a differentiator, integrator, or multiplier—you needn't model those functions at the device level.

The ideal analog CAE system

As a starting point in the selection of an analog CAE system, you might define what you consider the ideal system and then see how vendors' offerings measure up.

Your ideal CAE system might allow a hierarchical design input that begins with a description of your design goals. With this system, you would divide the design into separately created functional descriptions. These high-level descriptions in turn would allow you to try different architectures and approaches with relative ease. At this level, you wouldn't consider the compromises that your design would ultimately entail; you would simply test your basic theory. When satisfied with this functional design, you would verify it by using the ideal system's high-level simulator; then, you would modify the design as needed.

After you've designed and verified all of the functional blocks, the ideal CAE system would help you lay out the pc board. This process would be interactive so that you could bring your experience to bear to optimize component placement.

After layout, the ideal CAE system would model the parasitics that would plague the finished board to determine whether the board would meet spec. The layout and parasitic-modeling processes would repeat until the design worked in a simulated real-world environment.

When you are pleased with the design, the ideal analog CAE system would interface to a plotter (for the creation of the pc board artwork), to an automatic assembly system, and to automatic test equipment.

The ideal system would automatically create and update models by measuring real-world components and boards.

The ideal system would automatically conduct design verification at all levels; verification would consist of design-rule checking and simulation. Documentation would be hierarchical; the system would automatically update any changes to all affected documents.

The ideal system would be truly easy to use. You would not need to have a Unix guru on staff; you wouldn't even need to know one. The system would include virtual instruments that would work just like the real ones, allowing instantaneous changes of settings.

And of course, the ideal system would be affordable.

Improving product quality

Many of today's analog CAE systems automate tasks relating to the quality of the product you design. Such packages offer features like stress analysis to ensure not only that your design will work but that it will work over temperature, that all components will operate within their safe operating areas, and that your product will operate despite worst-case variations in component values.

Decisions on whether you should select a package that offers behavioral modeling, Monte Carlo analysis, and functional-description capability will depend on your personal design approach. Other factors, however, will be dictated by the complexity of the circuits you're designing. For example, if a system can handle a maximum of 200 parameters and a single op amp consumes 50 of them, the system won't be adequate for you if you're designing circuits with more than a few op amps.

Unfortunately, data regarding packages' capabilities in this area is scarce. Few vendors provide data on the number of nodes their packages accommodate, and very few state the number of nodes that a particular model would require. Thus, it's important that you attempt to implement a circuit that's representative of your designs when you try out a system.

Similarly difficult to quantify is

Text continued on pg 144

TABLE 1—REPRESENTATIVE ANALOG CAE PACKAGES

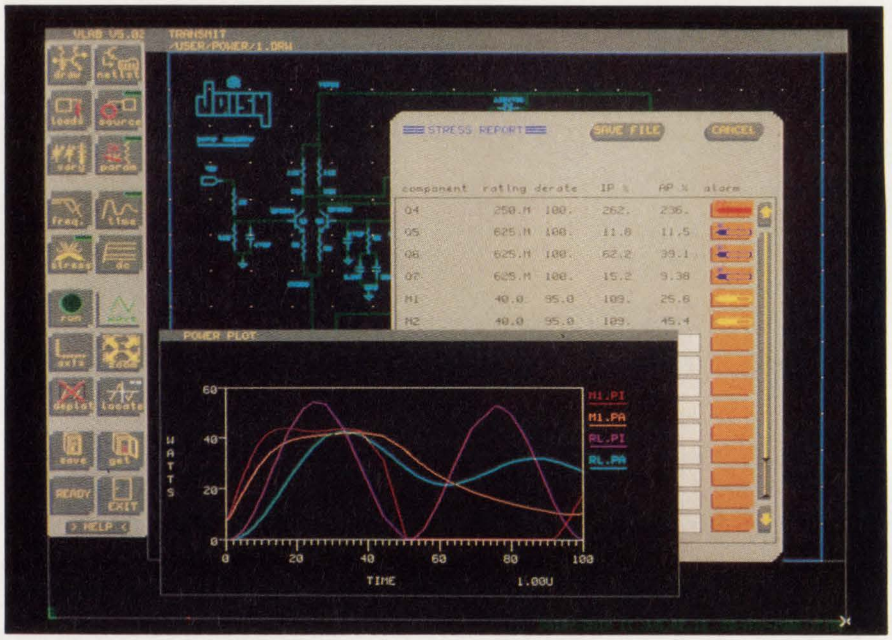
VENDOR	PRODUCT NAME	PRICE	COMPUTER
ACOTECH, 713 SANTA CRUZ AVE, SUITE 2, MENLO PARK, CA 94025. (415) 325-7999.	ALLSPICE II	$575	IBM PC
ANALOG DESIGN TOOLS, 1080 E ARQUES AVE, SUNNYVALE, CA 94088. (408) 737-7300.	ANALOG WORKBENCH	$14,500–$64,500	SUN*, APOLLO*, HP*
	PC WORKBENCH	$8000–$38,500	IBM PC/AT
ANALOGY INC, 8605 SW CREEKSIDE PL, SUITE D, BEAVERTON, OR 97005. (503) 626-9700.	SABER	$9000–$60,000	SUN*, APOLLO*, DEC VAX AND MICROVAX II, IBM MAINFRAMES
APPLIED I, 200 CALIFORNIA AVE, SUITE 214, PALO ALTO, CA 94306. (415) 325-4800.	TUTSIM	$39.95–$495	IBM PC
BRAINPOWER, 24009 VENTURA BLVD, CALABASAS, CA 91302. (818) 884-6911.	DESIGNSCOPE	$249.95	APPLE MACINTOSH (512k)
BV ENGINEERING, 2200 BUSINESS WAY, SUITE 207, RIVERSIDE, CA 92501 (714) 781-0252.	ACNAP, DCNAP, SPP	$72.95 EACH	IBM PC
CADNETIX CORP, 5757 CENTRAL AVE, BOULDER, CO 80301. (303) 444-8075.	SABER	$20,000	CADNETIX WORKSTATIONS
CASE TECHNOLOGY, 2141 LANDINGS DR, MOUNTAIN VIEW, CA 94043. (415) 962-1440; TLX 506513.	PSPICE	$2000–$4000	IBM PC, DEC VAX AND MICROVAX
COMPACT SOFTWARE, 52 HILLCREST DR, SADDLE RIVER, NJ 07458. (201) 881-1220; TLX 130073.	SUPER-COMPACT	$5000	DEC VAX, IBM MAINFRAMES, IBM PC, APOLLO*, HP*
DAISY SYSTEMS, 700 MIDDLEFIELD RD, MOUNTAIN VIEW, CA 94039. (415) 960-0123; TLX 858262.	VIRTUAL LAB	$10,000–$68,000	IBM PC/AT, DEC VAX AND MICROVAX, DAISY LOGICIAN
EESOF, 31194 LA BAYA DR, WESTLAKE VILLAGE, CA 91362. (818) 991-7530; TLX 384809.	TOUCHSTONE	$9900	IBM PC, DEC VAX, HP*, APOLLO*
	MICROWAVE SPICE	$8400	IBM PC
ELECTRICAL ENGINEERING SOFTWARE, 4675 STEVENS CREEK BLVD, SUITE 101, SANTA CLARA, CA 95051. (408) 296-8151; TLX 171201.	PRECISE	$10,000–$75,000	IBM PC, DEC VAX, SUN*, APOLLO*, IBM MAINFRAMES
FB CIRCUIT PRODUCTS, 5234 LONGFELLOW WAY, OXNARD, CA 93033. (805) 986-2276.	ACIRC, DCIRC	$95	IBM PC
FUTURENET CORP, 9310 TOPANGA CANYON BLVD, CHATSWORTH, CA 91311. (818) 700-0691; TWX 910-494-2681.	DASH ANALOG WORKBENCH	$11,800–$62,000	IBM PC/AT
INTERGRAPH CORP, 1 MADISON INDUSTRIAL PARK, HUNTSVILLE, AL 35807. (205) 772-2000; TWX 810-726-2180.	ACS SYSTEM	$10,000–$70,000	INTERPRO WORKSTATIONS
INTUSOFT, 3262 STARLINE DR, RANCHO PALOS VERDES, CA 90274. (213) 833-0710.	PRE_SPICE, IS_SPICE, INTU_SCOPE	$545	IBM PC
JENSEN TRANSFORMERS, 10735 BURBANK BLVD, NORTH HOLLYWOOD, CA 91601. (213) 876-0059; TWX 650-291-9207.	COMTRAN	$950–$5700	HP 300, 217, 9816, 9920, 9845, 9020
MENTOR GRAPHICS, 8500 SW CREEKSIDE PL, BEAVERTON, OR 97005. (503) 626-7000; TLX 160577 MENTOR UT.	MSPICE	$19,800–$73,700	APOLLO*
META-SOFTWARE, 50 CURTNER AVE, SUITE 16, CAMPBELL, CA 95008. (408) 371-5100; TWX 910-350-4928.	HSPICE	$15,000–$50,000	DEC*, APOLLO*, SUN*, IBM*
MICROSIM, 23175 LA CADENA DR, LAGUNA HILLS, CA 92653. (714) 770-3022 OR (800) 826-8603; TLX 265154 SPICE UR.	PSPICE	$950–$5100	IBM PC, DEC VAX
SOFCAD ELECTRONICS, BOX 21845, COLUMBUS, OH 43221. (614) 488-3400.	LINCAD	$99	IBM PC
SPECTRUM SOFTWARE, 1021 S WOLFE RD, SUNNYVALE, CA 94087. (408) 738-4387.	MICRO-CAP II	$895	IBM PC, HP 150
TATUM LABS, 1478 MARK TWAIN CT, ANN ARBOR, MI 48103. (313) 663-8810.	ECA-2	$675	IBM PC
TEKTRONIX CAE SYSTEMS, 5302 BETSY ROSS DR, SANTA CLARA, CA 95054. (408) 727-1234.	SPICE 2G6 INTERFACE	$5000	APOLLO*, DEC VAX
VALID LOGIC SYSTEMS, 2820 ORCHARD PARKWAY, SAN JOSE, CA 95134. (408) 945-9400.	ANALOG DESIGNER	$10,450–$84,500	IBM PC/AT, VALID SCALD
VENABLE INDUSTRIES, 3555 LOMITA BLVD, TORRANCE, CA 90505. (213) 539-2522; TLX 752421.	MODEL 350	$26,800	IBM PC

*VERSIONS ARE AVAILABLE FOR MANY OF THIS MANUFACTURER'S COMPUTERS

SIMULATOR	BEHAVIORAL MODELING	FUNCTIONAL DESCRIPTIONS	MODEL-GENERATION SOFTWARE	PARAMETER EXTRACTION FROM ACTUAL DEVICE	STRESS ANALYSIS	PARAMETER VARIATION ANALYSIS	MONTE CARLO WORST CASE ANALYSIS	ADDITIONAL CAPABILITIES	CIRCLE NO
SPICE						•			650
SPICE PLUS			•	•	•	•	•	POWER DESIGN MODULE, ABLE TO WORK WITH OTHER VERSIONS OF SPICE	651
SABER	•	•	•			•		SIMULATES ANYTHING DEFINABLE WITH EQUATION	652
PROPRIETARY	•	•						REAL-TIME OPTION INTERFACES SIMULATION TO REAL WORLD VIA ADC AND DAC	653
PROPRIETARY		•							654
SPICE		•				•	•		655
SABER	•	•	•			•		SIMULATES ANYTHING DEFINABLE WITH EQUATION	656
PSPICE			•				•	MAGNETICS MODELING	657
		•				•	•	HIGH FREQUENCY AND MICROWAVE	658
DSPICE		•	•	•	•	•	•		659
PROPRIETARY				•		•	•	HIGH FREQUENCY AND MICROWAVE	660
SPICE						•		MICROWAVE SIMULATION	
SPICE			•		•	•	•		661
PROPRIETARY						•			662
SPICE PLUS			•	•	•	•	•	POWER DESIGN MODULE	663
PROPRIETARY	•	•	•	•	•				664
IS_SPICE						•	•	CIRCUIT OPTIMIZER	665
PROPRIETARY			•			•	•	CIRCUIT OPTIMIZATION	666
SPICE			•		•	•		ADT GENERAL DEVICE LIBRARY AVAILABLE, ABLE TO WORK WITH OTHER VERSIONS OF SPICE	667
HSPICE*			•	•		•		MODELING OF RADIATION EFFECTS	668
PSPICE			•				•	MAGNETICS MODEL	669
SPICE						•	•	CIRCUIT OPTIMIZATION	670
SPICE			•				•		671
SPICE						•	•		672
SPICE								INTERFACES TO SUPER-COMPACT	673
VALID SPICE			•	•		•	•		674
PROPRIETARY		•	•	•		•		AUTOMATED MEASUREMENT AND DESIGN FOR FEEDBACK LOOPS USED IN SERVO SYSTEMS AND POWER SUPPLIES	675

The complexity of the circuits you're designing, as well as your personal design approach, will affect your selection of an analog CAE package.

To determine if your circuit *is operating within acceptable limits, Daisy's analog CAE package monitors each component. This display shows that Q_4 is stressed beyond its safe operating limits.*



the effectiveness of a system's component library. The number of components in the library is not as important as the quality of the models, although you shouldn't assume that if a vendor offers a large number of components, the quality of its library is poor. The quality, for you, depends upon what you might use the models in the library to represent. You must consider whether you'll be simulating operation at extremely low currents, high currents, or, perhaps, high frequencies. A model that is adequate for one of these conditions might not be adequate for the others.

In general, the accuracy of a model is an illusive concept. It's difficult to predict how closely a model will represent a real device under all possible operating conditions. Moreover, even when you determine that a model is not adequately representing a transistor, for example, you might have trouble telling which of a long list of parameters should be modified to improve the model's accuracy. (Nevertheless, you'll want to update your models whenever you're able to do so. The improved models could help you optimize your existing design or improve the quality of your new designs. Furthermore, vendors will be very interested in any improvements you find necessary to the models.)

Tools aid model creation

Creating the models initially is even more difficult. In an effort to solve this problem, many vendors are beginning to offer tools that assist you in the creation of models. With such tools, you might enter the model of an op amp, for instance, by entering the data-sheet specs into the CAE system, which in turn uses those specs to create the appropriate model. The resulting model can only approximate the real device because no data sheet can completely describe a device. Analog IC manufacturers are cautious about providing additional information for use in developing models; they fear becoming responsible for meeting some implied specifications as a result of this information.

Another way you can create models is to extract the model parameters from an actual device. Many vendors offer this option.

A related factor you'll consider is the simulator that the system employs. But unless you plan to create your own models, you needn't be overly concerned about whether the simulation program is Spice, Saber, or a proprietary version. One factor you might consider in this regard is that Spice traditionally has suffered from a well-publicized convergence problem. Most versions of Spice start with an initial set of conditions and continually calculate new sets that should converge to a solution. The process might, however, never converge, in which case the simulation effort would yield no data. Many vendors claim that with their Spice enhancements the convergence problem won't appear for the vast ma-

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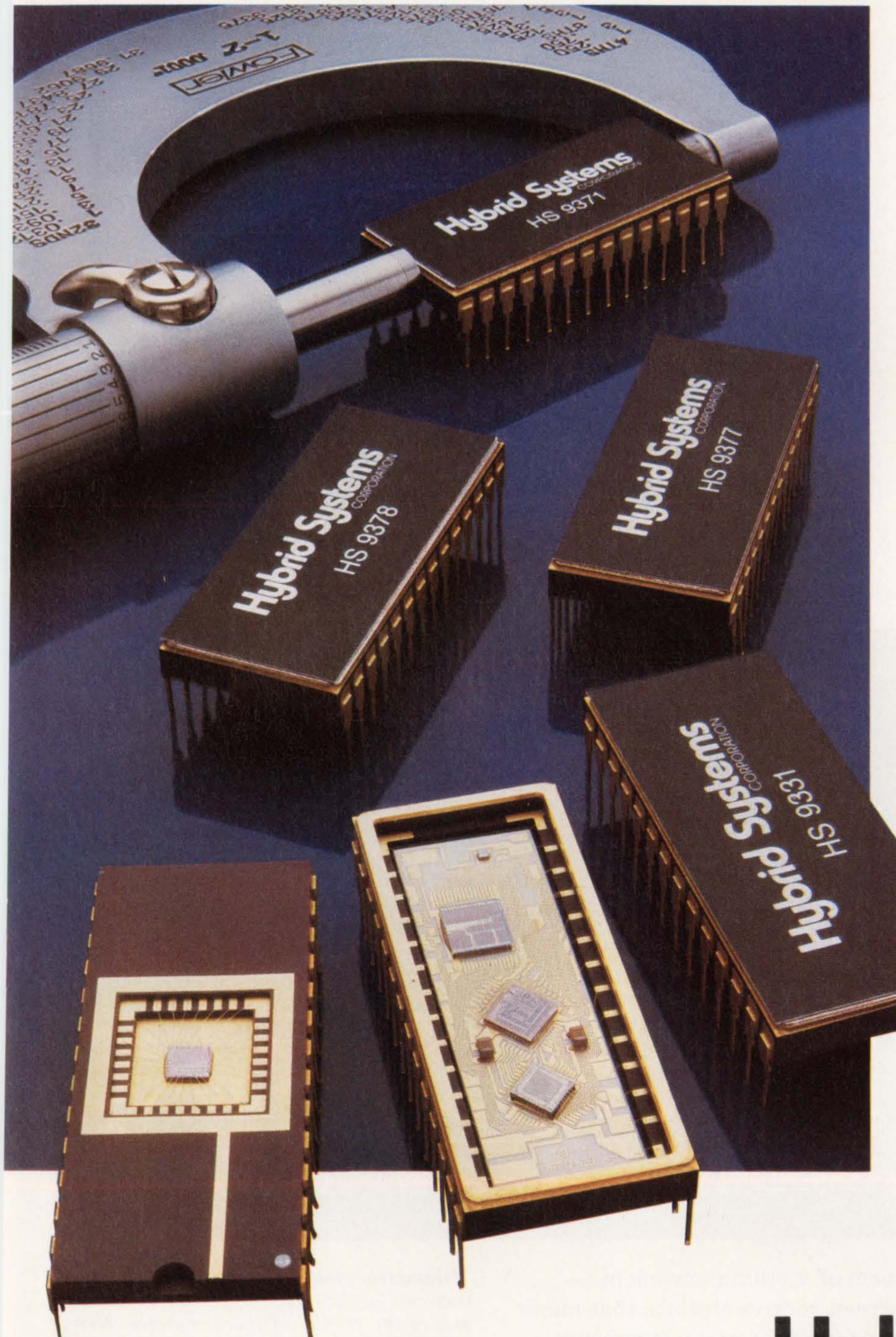

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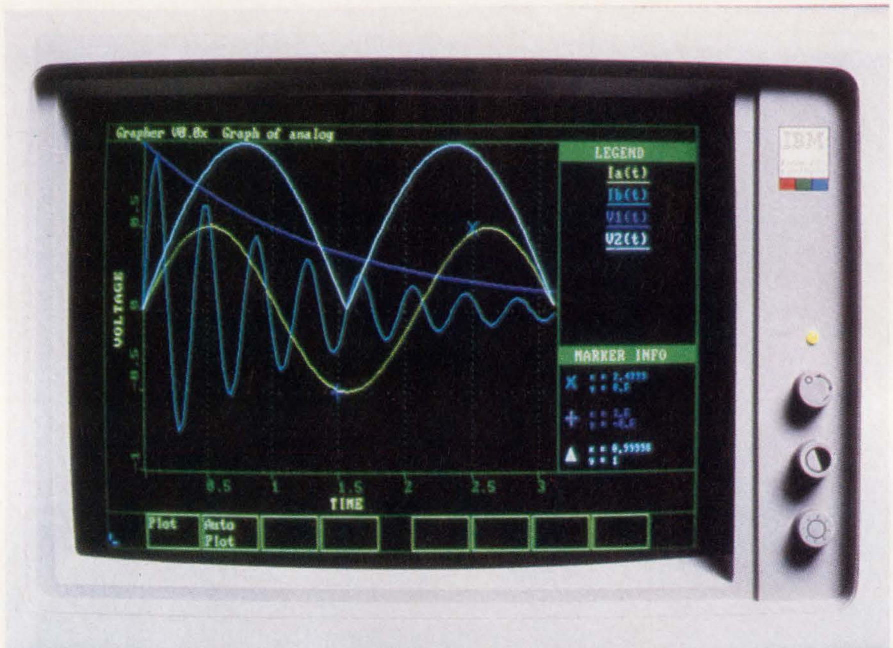
The majority of current analog CAE systems provide a schematic-capture option or can use another vendor's schematic-capture package.

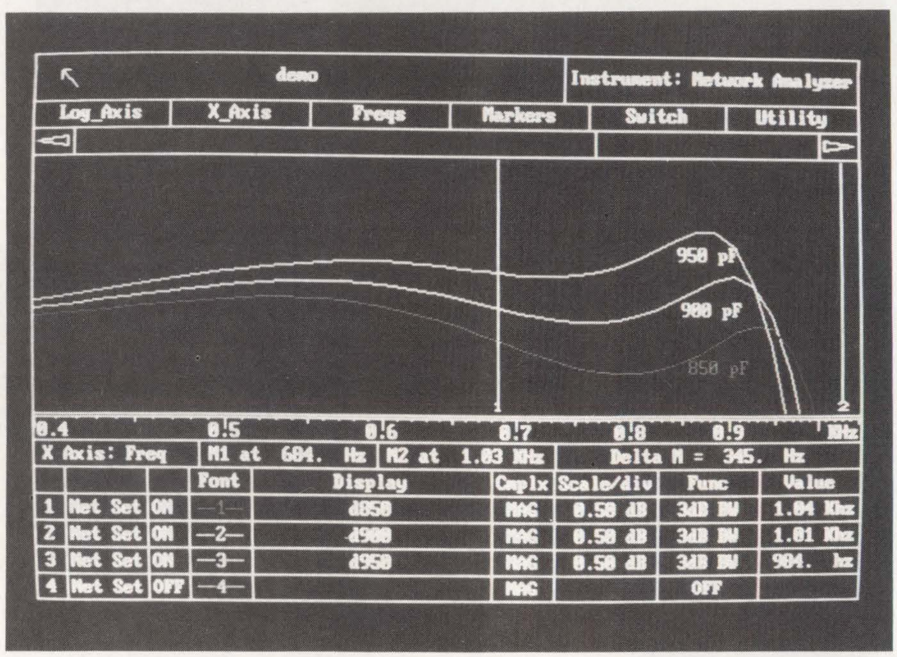
***A wide variety of graphic outputs** are available with analog CAE systems. The Grapher from Cadnetix includes a legend window and a marker window to help you interpret data.*



jority of simulations, but they don't offer a quantifiable value of the likelihood of convergence.

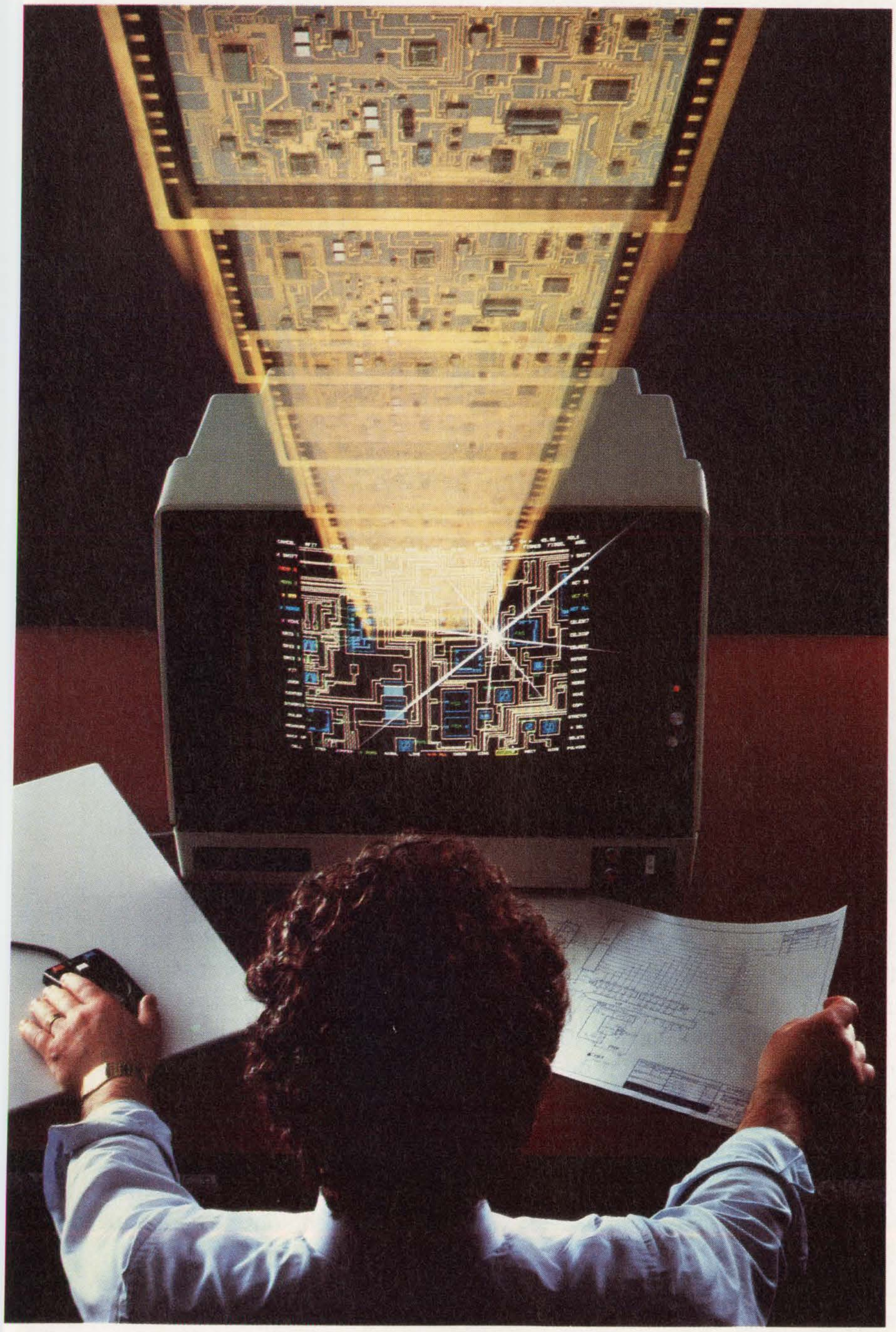
For day-to-day operation, much more apparent than the simulator's operation will be the way you communicate with the CAE system and the way the system communicates with other CAE products, like schematic-capture systems and photoplotters. If you find it difficult to enter a design and interpret the results, you will find the system to be of limited benefit. On the other hand, if the system accepts data in a form you are familiar with and presents the results of the simulation in a form you are familiar with, then the system will be more useful. Almost all of today's analog CAE systems provide a schematic-capture option or can use another vendor's schematic-capture package.

The wide variety of graphical aids make interpretation of the simulation results much easier. Many packages present data in the form of virtual instruments—screen representations that mimic the format of real instruments. You can perform advanced calculations on the data acquired from the simulator, and you have tremendous flexibility in selecting the pre-



***Parametric plotting** allows you to optimize a circuit by changing component values and seeing the results of these changes. Here, FutureNet's Dash-Analog Workbench displays the frequency response of a circuit with various values of a capacitor.*

Custom Hybrid Solutions



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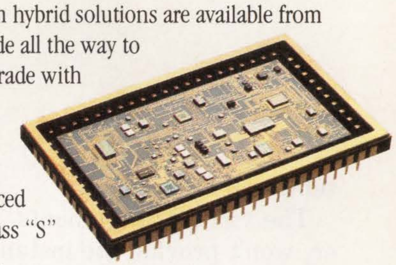

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CIRCLE NO 135

Many vendors are beginning to offer tools that assist you in the creation of models; the models, however, can only approximate the real device.

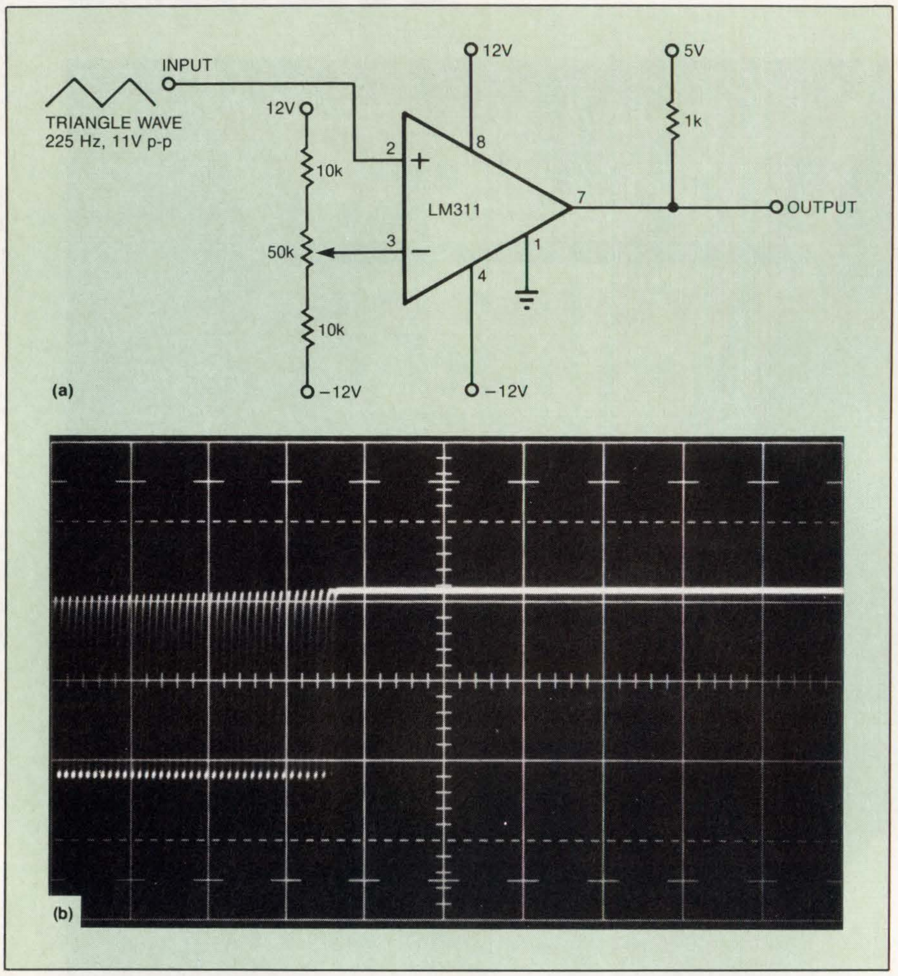

Fig 1—Analog CAE systems predicted stable operation *for this simple comparator circuit **(a)**, but when built, the circuit exhibited the instability that an experienced analog designer would have expected. Viewed on an oscilloscope **(b)**, the comparator's output produced many transitions (the scope triggered on the first), although the simulations only showed one. (Photo courtesy Linear Technology Corp).*

sentation of the data.

The virtual instruments, however, won't provide the instantaneous response of real instruments. On the bench, you can change the frequency of a oscillator or the sweep speed of a scope as fast as you can turn a knob, and you can monitor different circuit nodes as fast as you can move a probe. On the bench, therefore, you can interact with a circuit and get to know it. With the virtual instruments, in contrast, considerable time can elapse between the time you initiate a measurement command and the time you see the result. Depending upon the system and your tolerance to this delay, you might find that using the virtual instruments is very frustrating.

On the other hand, many measurements that you can make with an analog CAE system would be difficult or impossible with benchtop instruments. With CAE systems, you can measure the current in any branch, the instantaneous power of all components, the effects of extreme temperature, and the effect of worst-case component variations.

Try to be objective

Many engineers are overly optimistic about analog CAE because it seems to promise to ease their jobs. Many hope that the analog CAE systems will make up for what they don't already know. But even the what-if games that users can play with the system require that users know which questions to ask, and basic analog-circuit knowledge remains indispensible.

Consider, for example, the simple comparator circuit shown in **Fig 1a.** The high source impedance of the voltage reference and the lack of hysteresis suggest an inherently unstable design. However, several analog CAE systems predicted stable operation.

(Incidentally, modeling this simple circuit proved to be difficult. Some systems did not have the LM311 in their libraries. One com-

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CIRCLE NO 136

pany had its model of the LM311 in the shop for repairs—an upgrade to include the strobe pin—and another vendor had nine signals defined on the 8-pin device. The ninth signal, named C, was removed manually with the vendor's editor.)

When built and examined using a scope, the circuit produced, as expected, an output that exhibited multiple transitions each time the input crossed the reference **(Fig 1b)**. If this circuit were being used to condition a signal that was then to be counted, the error would be enormous.

Analog CAE is not the solution for a lack of knowledge in analog engineering techniques. In the comparator experiment, the design looked fine in simulation, but in the real world it was useless. The knowledge and experience of the analog designer is still very much a part of the design process.

Keep an eye on reality

You must keep an eye on reality when using an analog CAE system. It is easy for the simulator to put 100W into a ¼W resistor, but the actual circuit would soon fill the room with the sweet smell of a cooked resistor. When you are having a problem with the simulation, look at the voltages at each node and see if it's close to what you would expect. If a circuit node sits at 84V when the circuit's power-supply level is only 12V, then something is wrong.

There is more to using one of today's analog CAE systems than knowing how to run the program. You need to understand the limitations of the models you are using. There is no substitute for an understanding of methods used by the simulator. If you blindly accept the output of the simulator, you will quite often find yourself in trouble.

These tools are very complex, and you'll need time to acquire the experience to know when to use each tool. But the effort is well worth the time expended. Those engineers that only use a breadboard and have not learned to use these new tools are limiting themselves. The opposite is also true: Those who only know how to use the analog CAE system are going to have a hard time getting a circuit to work in the real world.

EDN

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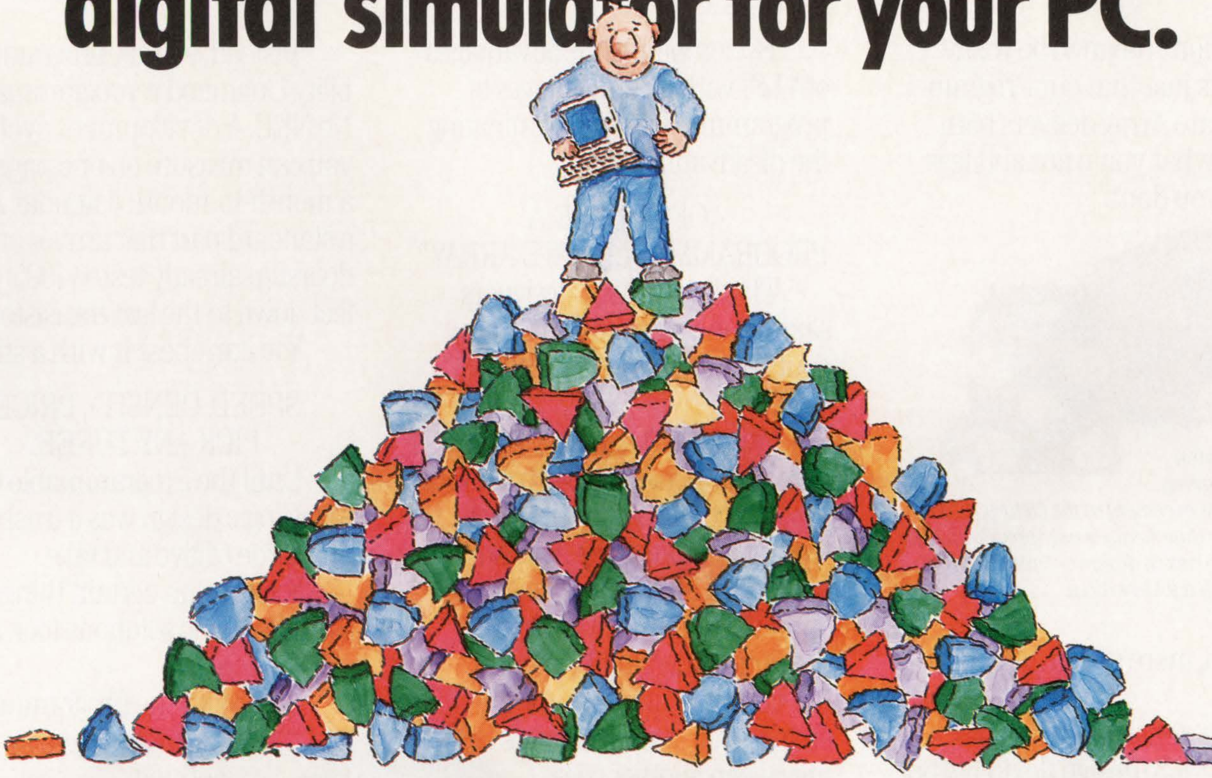

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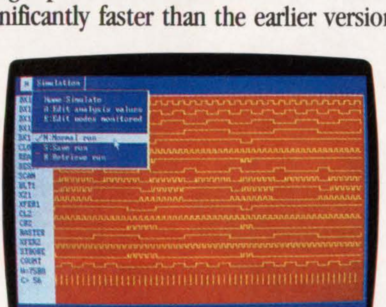

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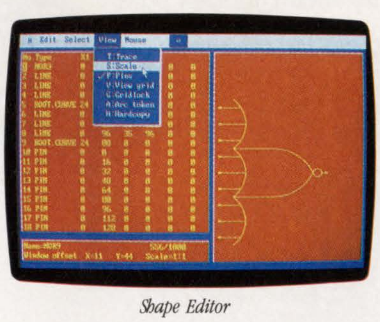

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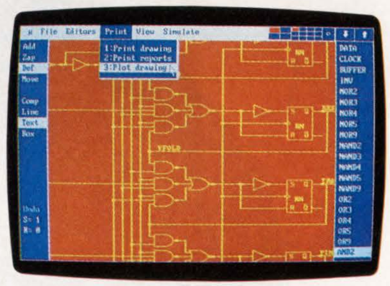

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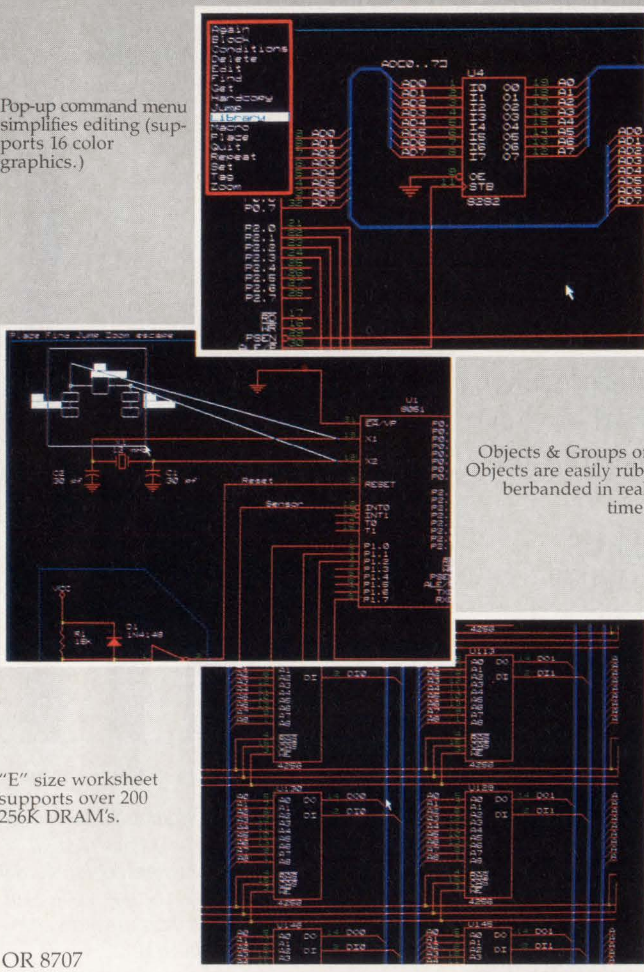

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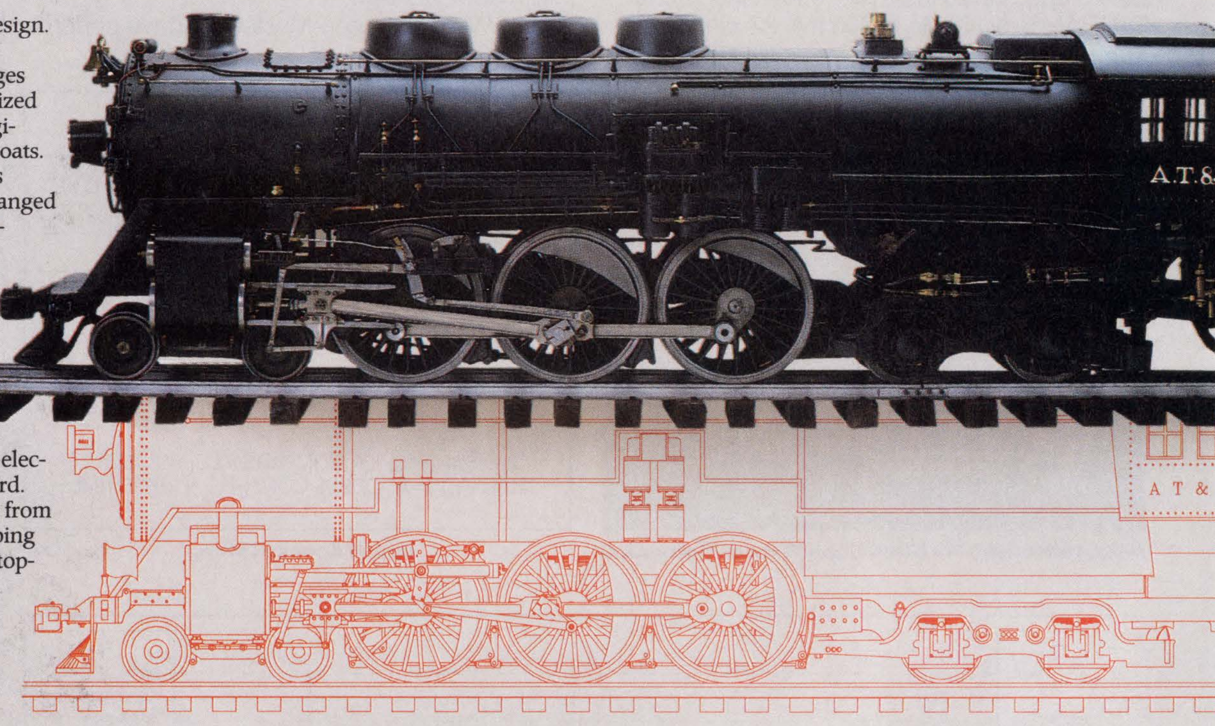

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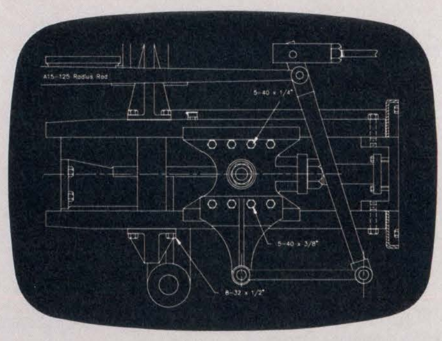

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JFET-input amps are unrivaled for speed and accuracy

JFET-input amplifiers provide an economical means of achieving high accuracy in applications that need wide bandwidths for large signals. They are ideal for pulse amplifiers, fast D/A converters, peak detectors, and logarithmic amplifiers.

Peter Henry, *Precision Monolithics Inc*

JFET-input operational amplifiers are an option for designers who require speeds greater than those provided by standard bipolar op amps such as the OP-07. The high slew rates of JFET-input amplifiers make these devices attractive for pulse amplification and other applications that require wide bandwidths and handle large signals. Their low bias currents make them equally suitable for peak detectors and logarithmic amplifiers. Furthermore, their fast settling rates make them ideal for fast, high-precision DACs.

To obtain the full performance of which JFET-input amplifiers are capable, you'll need to take all the standard precautions in designing and laying out your pc boards, along with a few extra precautions that are specific to JFET-input devices (see **box**, "Caveats, warnings, and design reminders," on pg 166).

An autozeroing JFET-input amplifier can help a CMOS D/A converter achieve a fast settling time while converting the DAC's current output into voltage levels and reducing output impedances. You'll obtain the fastest settling times from bipolar DACs, because they have lower output capacitance than their CMOS counterparts, but CMOS devices have the advantages of low price and the availability of a wide variety of interface options. The primary disadvantage of CMOS DACs is their large output capacitance, which can be 50 to 120 pF for an 8-bit DAC, and as much as 70 to 150 pF for a 12-bit DAC. This large capacitance increases the settling time. However, if you add a JFET-input amplifier (such as PMI's OP-42) to create a voltage output, you can compensate for the output capacitance. A CMOS DAC will then settle in approximately 3 μsec to within 0.01% of a 10V full-scale output step.

The offset voltage of many older JFET amplifiers suffered from large thermal drifts. However, newer state-of-the-art precision JFET-input amplifiers exhibit relatively little drift with temperature, and the resulting output error is generally insignificant unless you operate the amplifier at a high gain level. If your application requires the minimum possible offset error, however, you can use a servo loop that automatically corrects offset-voltage and drift errors. In **Fig 1**'s circuit, for example, IC_1 multiplexes eight analog channels to the input of an OP-42 or OP-44 amplifier, which has a gain of 100. One of the analog channels grounds

JFET-input amplifiers provide high slew rates and low offset and drift, and they have low input bias currents.

the amplifier input in order to correct for V_{OS} (offset) errors; the other channels are available for signals.

To correct V_{OS} errors during a conversion, you first drive the three multiplexer-address lines ($A_{1\text{-}3}$) high, so that multiplexer IC_1 grounds the input of JFET-input amplifier IC_2. At the same time, AND gate IC_3 drives the $\overline{\text{Zero}}$ line low and thereby causes the switching circuitry consisting of transistors Q_1 and Q_2 to turn on JFET switch Q_3. This action connects JFET-input amplifier IC_4 into the feedback path of IC_2 via that IC's null pins (1 and 5) and thereby forces the output of IC_2 to assume the value of the offset voltage at the input of IC_4. The current in the feedback loop then develops a voltage across hold capacitor C_H.

Keep leaks away from correction circuitry

After a time period that's determined by the RC time constant of R_1C_H and the current through Q_3, you can change the multiplexer address so that the $\overline{\text{Zero}}$ line goes high and turns off Q_3. The voltage across C_H holds the output of IC_4 (which is also the offset-voltage compensation for IC_2). IC_1 has a relatively long switching time, so Q_3 turns off before IC_1 connects a new input to IC_2; consequently, the signal cannot leak into offset-correction circuits.

If you use the component values shown in **Fig 1,** you should make sure that the $\overline{\text{Zero}}$ line remains low for at least 200 μsec to ensure proper nulling. You can achieve a faster nulling time by using a JFET switch that has a higher I_{DSS}, such as a 2N4393, but you'll do so at the expense of increased leakage and faster droop. Some error is induced by charge injection through Q_3 into C_H, but you can minimize this error by using a large value of C_H.

To minimize droop at the output of IC_4, make sure that hold capacitor C_H is a low-leakage type (such as a polystyrene device). For higher precision, add a potentiometer to null the offset voltage of IC_4. When you use the component values shown, the droop of the offset voltage at 25°C is only 1.3 μV/sec. Near the center of

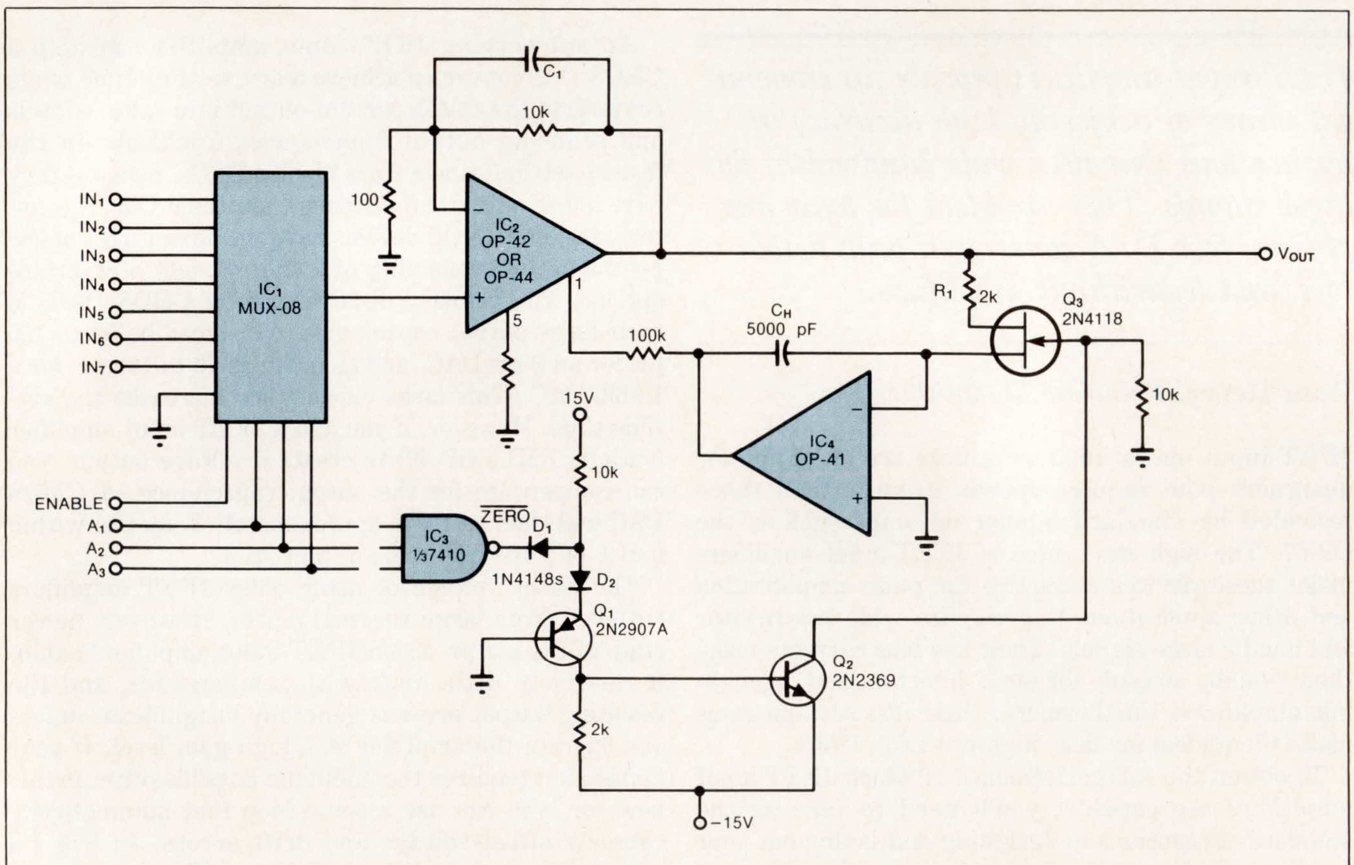


Fig 1—This autozeroing amplifier multiplexes seven inputs *to a common output. The eighth input grounds the input of IC_2 to zero the amplifier's offset voltage. Before you select a signal, hold the three address lines high for 200 μsec to ensure proper zeroing.*

the adjustment range, each 100 mV of swing at the output of IC_4 will cause a shift of 150 μV in the V_{OS} of IC_2. The circuit is capable of correcting as much as 10 mV of offset, so that it can handle some system offsets in addition to IC_2's offset.

You can substitute digital correction

If your application requires digital correction of the offset voltage, you can substitute an ADC/DAC combination for IC_4. With this scheme, when you ground IC_2's input, the ADC digitizes the IC's output (offset) voltage and passes a correction factor to the DAC, which in turn applies an analog nulling voltage to pin 1 of IC_2. This modification is of value in applications that digitize the output of IC_2, and it has the advantage that digital correction circuits do not droop with time. However, the scheme is a needless complication in systems that do not include a μP for other purposes.

The level-shifting circuitry (D_1 and D_2, Q_1 and Q_2) converts a TTL signal to the levels necessary to drive JFET switches, and you can use the same circuit in a wide variety of applications. When the TTL input signal ($\overline{\text{Zero}}$) goes low, it turns off transistor Q_1. This action forces the base of transistor Q_2 to -15V, turning off Q_2 and holding the gate of Q_3 at ground level. While these conditions continue, Q_3 presents a low impedance to the signal applied to it through R_1. Consequently, the inverting input of IC_4 follows the output signal of IC_2, and IC_2 charges C_H.

When the TTL $\overline{\text{Zero}}$ signal goes high again, it turns on Q_1 and Q_2, which in turn pull the gate of Q_3 to -15V. This action puts Q_3 into a high-impedance state, so that the switch disconnects the input of IC_4 from the output of IC_2, and IC_2 maintains the charge across C_H.

Fast S/H amplifier exhibits 0.01% accuracy

The characteristics of JFET-input amplifiers make them natural choices for fast sample-and-hold (S/H) amplifiers. **Fig 2a**'s circuit has an aperture time of 80 nsec and can acquire a 10V step in less than 1 μsec with an accuracy of 0.1%, and in 2 μsec with an accuracy of 0.01%. The corresponding settling times are 100 nsec and 300 nsec, respectively.

The $\overline{\text{Sample}}$/Hold control-input circuit uses the same level-shifting circuit used by the autozero circuit described above, with the addition of a Schottky clamping diode (D_3) and a pullup resistor R_1 to accelerate transitions. Diodes D_4 and D_5 prevent the forward-biasing of JFET switches Q_3 and Q_4. During the sampling time, the JFET switches conduct, so that amplifiers IC_1 and IC_2 both operate at unity gain and IC_1 charges hold capacitor C_{H1}. The V_{OUT} signal precisely tracks the V_{IN} signal.

When you switch the control line to the hold mode, the JFET switches present a high impedance, so that Q_3 disconnects the output of IC_1 from the input of IC_2, and Q_4 allows IC_2 to charge hold capacitor C_{H2}. The charges on the two hold capacitors then cause IC_2 to maintain the V_{OUT} signal at the sampled value.

Matched components reduce errors

The low bias current of the JFET-input amplifiers and the low leakage of the JFET switches combine to minimize leakage of the charges on C_{H1} and C_{H2}. Furthermore, you can closely match the remaining leakage by matching the capacitor values and by using a matched pair of JFET switches contained in the same housing. This configuration has two advantages. First, it matches the amounts of charge injection through the switches into capacitors C_{H1} and C_{H2} and thereby considerably reduces the hold step. In fact, adjusting a trimmer capacitor connected in parallel with one of the hold capacitors will let you reduce the hold step below 1 mV.

Second, the scheme causes the I_{OS} of IC_2 and the leakage through the matched JFET switches (rather than absolute leakage levels) to control the voltage droop at the output terminal. Furthermore, the output voltage is controlled by the differential voltage between the two capacitors. The absolute voltages across the capacitors droop because of IC_2's bias current, but both droop at the same rate, making this voltage change appear as a common-mode effect. The differential voltage is controlled by I_{OS}, which is usually much smaller than I_B. IC_2 can maintain a constant output voltage, even though the actual voltage levels on the two capacitors may change considerably during the hold period. In **Fig 2a**'s circuit, this scheme reduces the droop rate to 7 μV/msec. **Fig 2b** shows a sine wave applied to the S/H circuit, and the resulting samples at the output.

The control provided by these differential voltages breaks down when their absolute values fall below the minimum input voltage of IC_2. However, that condition will typically not occur until several seconds have elapsed. You can reduce both the hold step and the droop rate even more by using larger values for the capacitors, but you'll then sacrifice some speed. (For more on the examination of errors, see **box,** "Calculating error magnitudes," on pg 168.)

You can exploit the low bias currents inherent in a

Offset drift is most likely to create an error when you operate the amplifier at high gain.

JFET-input amplifier to create a fast peak detector (**Fig 3a**) that can capture a 10V peak only 2.5 μsec wide. This circuit uses the level shifter employed by the two previous circuits, but it does not drive any FET switches. Instead, a Reset command causes Q_2 to discharge hold capacitor C_H directly.

After a reset operation, the voltage across C_H is negative, so the circuit will detect very small peaks even if the ac signal has a negative dc offset. Be aware, however, that the reset method prevents this circuit from detecting negative peaks. The droop rate is 3 mV/msec and is mainly due to leakage of the charge on C_H through Q_2; diode D_5 contributes very little charge leakage, because it operates with only a small voltage across it. The action of the circuit is illustrated in **Fig 3b.**

You'll find that JFET-input amplifiers yield excellent performance in logarithmic amplifiers. **Fig 4's** circuit follows the usual log-amp configuration, in which the logarithm of the input voltage is derived from the

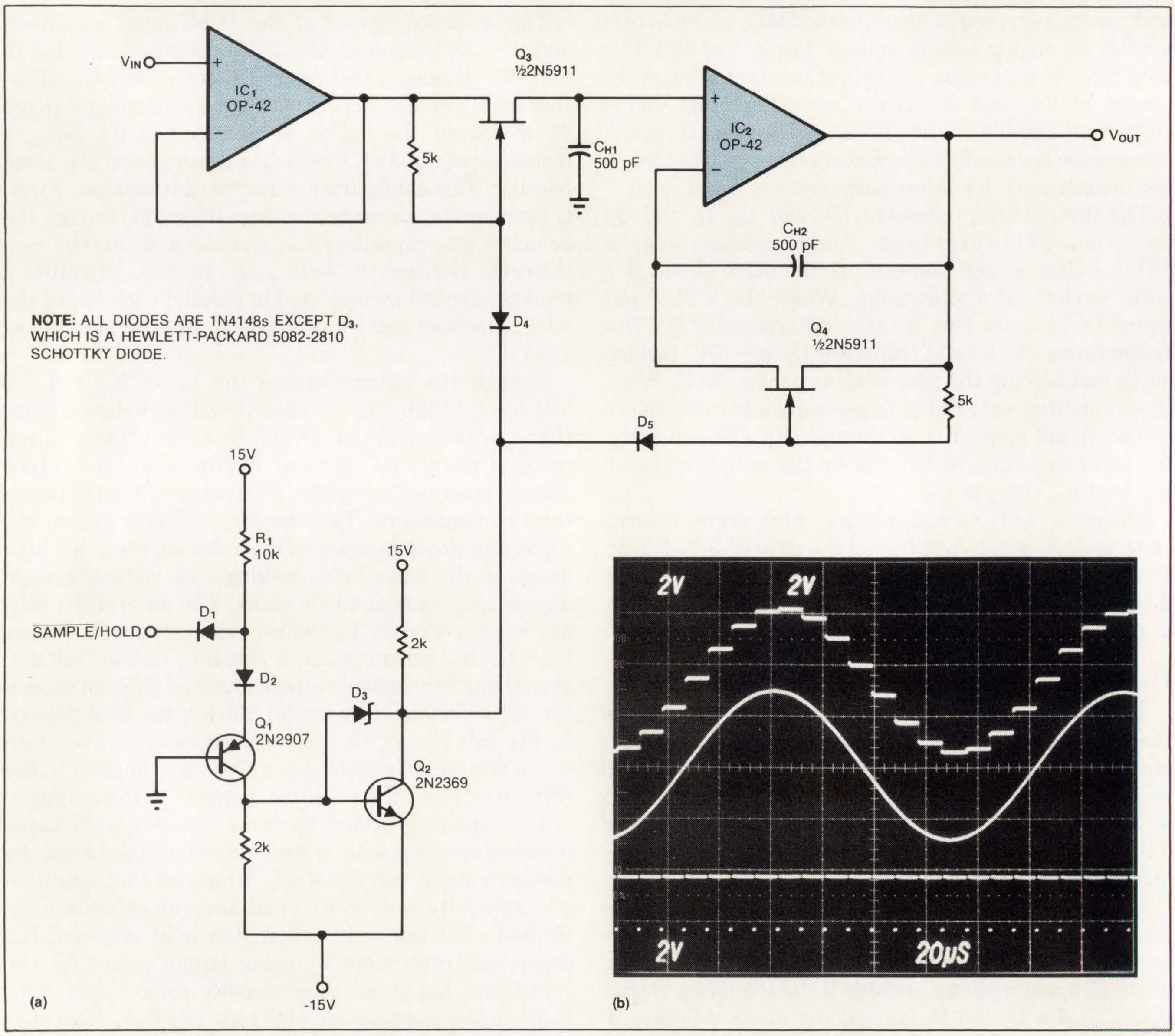


Fig 2—This fast sample/hold amplifier (a) uses two hold capacitors *to minimize both the hold-step effect and the output droop. You can see the very small hold step and the absence of droop in the scope photo **(b).***

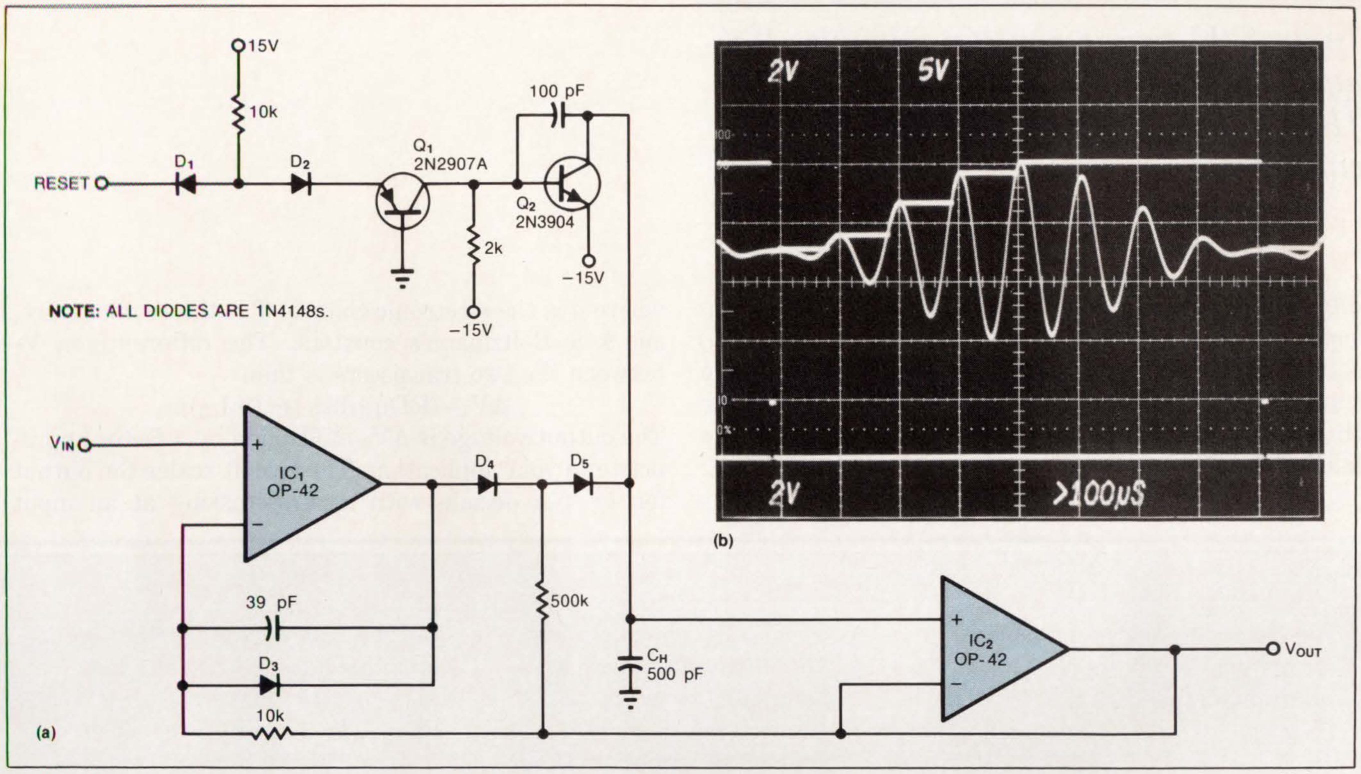


Fig 3—This peak detector (a) can capture a 10V peak *that's only 2.5 µsec wide. After a reset it can detect very small peaks even if the ac signal has a negative dc offset. The detector's JFET-input amplifiers have very low input bias currents and therefore minimize leakage from the hold capacitor. This low leakage is responsible for the absence of droop* ***(b).***

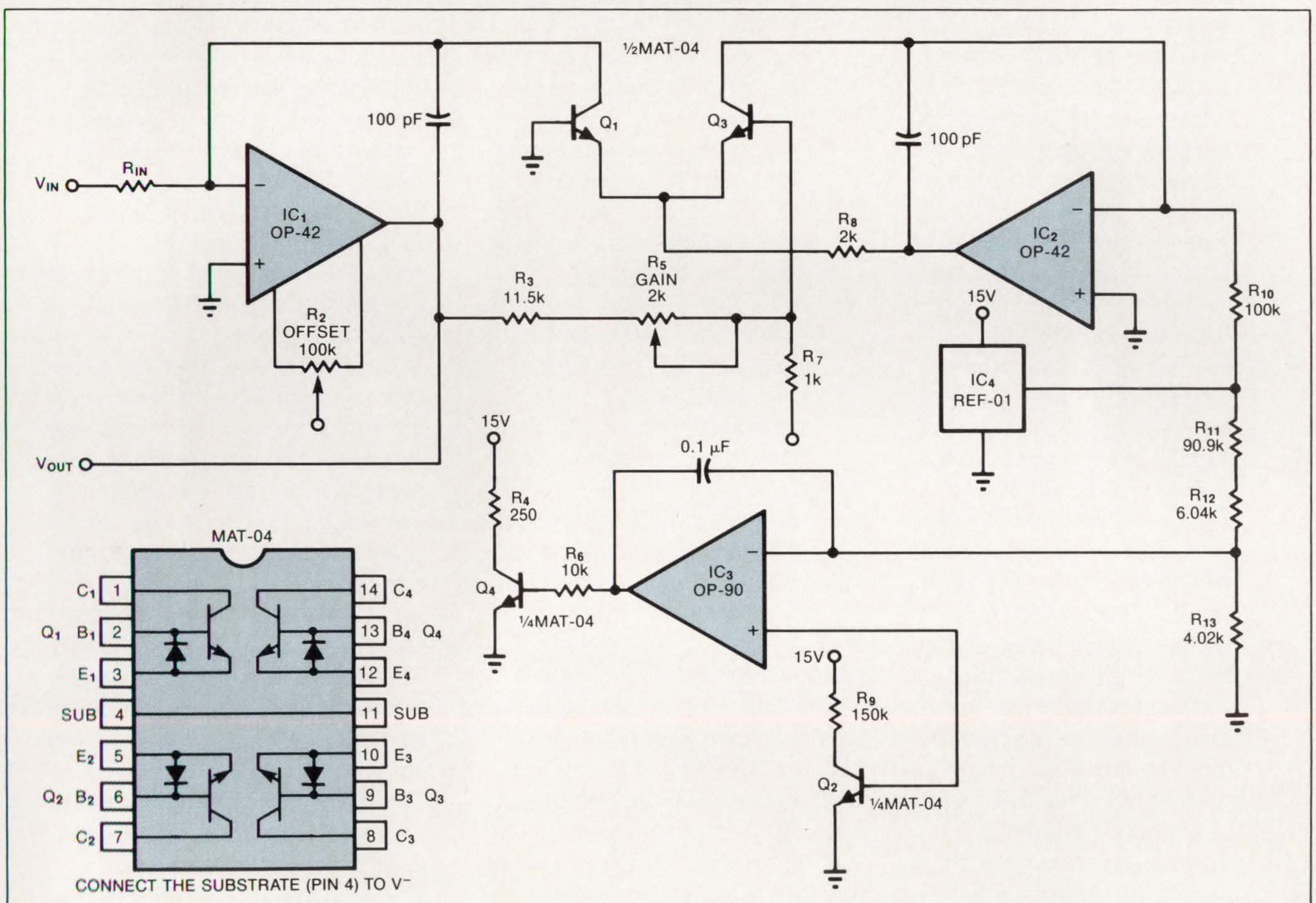


Fig 4—This logarithmic amplifier eliminates temperature effects *by ensuring that the two log-conversion transistors are always at the same temperature. The conversion transistors are on the same substrate as a heater transistor and a temperature sensor, which are connected to each other in a feedback loop.*

In an S/H circuit, you can minimize leakage from the hold capacitor by using JFET-input amplifiers that have low bias currents.

differential between the threshold voltages of two transistors (Q_1 and Q_3). A precision reference source (IC_1) sets the collector current of Q_3, and the input voltage controls the collector current of Q_1. You can derive the threshold voltages (V_T) of the transistors using the following equation:

$$V_T=(kT/q)\ln(I_C/I_S),$$

where q is the electronic charge, T is the temperature, and k is Boltzmann's constant. The difference in V_T between the two transistors is then

$$\Delta V_T=(kT/q)[(\ln I_{C1})-(\ln I_{C3})].$$

The output voltage is ΔV_T multiplied by a factor appropriate to your application. The circuit scales the output for 1V per decade with a zero-crossing at an input

Caveats, warnings, and design reminders

The following design principles are critical for the performance of any high-speed amplifier. They are included here as a check list.

- Use separate supply traces and grounds for each amplifier.
- Bypass each supply, right at each amplifier, with a 1- to 10-μF tantalum electrolytic capacitor connected in parallel with a glass or ceramic capacitor that has a value of 0.01 to 1 μF.
- Provide separate supply lines and ground lines for the digital and analog sections of your system.
- Switching power supplies can inject spikes of several hundred millivolts into the supply lines, and they can radiate EMI. Shield the analog sections and bypass all supply lines at the point where they enter the shielded enclosure.
- Be careful not to exceed an amplifier's maximum input-voltage specification. If a signal could be applied before the amplifier's supplies reach their full values, provide clamping diodes—but remember that these devices add leakage and capacitance to the circuit.
- Be careful not to exceed the maximum junction temperature or the maximum power-dissipation ratings of an amplifier. If you connect a capacitive load to the output of an op amp, be sure to include in your calculations the power dissipation caused by the rms ac currents delivered to the load.
- Internal power dissipation raises an IC's junction temperature. You can find the amount of the increase from the formula $\Delta T=P_D\theta_{JA}$, where P_D is the power dissipation and θ_{JA} is the thermal resistance of the package. For 8-pin packages lacking a heat sink, this parameter varies from 90°C/W (plastic DIP) to 200°C/W (TO-99 can). The junction temperature is the ambient temperature plus ΔT.

Precautions for JFET amps

The following design principles also have general application, but the focus here is on their implications for designing with JFET-input op amps.

First, remember that a rise in junction temperature increases the bias current of a JFET-input op amp; a rise of 10°C may double the bias current. JFET-input op amps have a naturally low bias current, however; for PMI's OP-42, for example, the current is only 200 pA at room temperature and less than 20 nA over the full military temperature range. The errors produced by such small currents are usually insignificant; at a slew rate of 100V/μsec, you would need a current of 1 mA to drive stray capacitances amounting to only 10 pF. Although some JFET-input op amps use cancellation methods to decrease bias current, these techniques can create excessive phase shifts in high-speed amplifiers.

Remember also that the slew rate of an op amp varies according to the voltage difference between its two inputs. If you want to achieve the maximum slew rate specified in the data sheet, you must ensure a difference of about 2V between the inputs of a JFET-input op amp so that one side of the op amp's differential-input circuit turns completely off. At unity gain, such voltages are normal, but in circuits that have a higher gain, the input-voltage levels—and hence the slew rate—decrease. A JFET-input op amp that yields a slew rate of 60V/μsec at unity gain might yield only 20V/μsec if you operate it at a gain voltage of 100 mV. For a V_{IN} greater than zero, this configuration yields a transfer function of

$$V_{OUT}=-[\log(V_{IN}/R_{IN})+4]$$

(for V_{OUT} in volts and the quantity V_{IN}/R_{IN} in amps). The circuit operates correctly for inputs from 1 mV to more than 10V.

The above equations show that the temperatures of the log-conversion transistors have a direct effect on the output voltage. Conventional circuits provide temperature correction by using a thermistor instead of a resistor in place of R_7. This circuit uses a special method to provide an isothermal environment for the log-conversion transistors.

The MAT-04 IC used in this circuit is a symmetric

---

of 100 with a ±100-mV input signal.

You should also keep in mind that an amplifier that has a high slew rate or a wide bandwidth doesn't necessarily settle fast. Many amplifiers with high slew rates obtain their speed at the cost of inducing excessive ringing in the output waveform; this ringing increases the settling time. Remember, too, that the ac characteristics of some amplifier types vary widely from part to part. Data sheets usually specify a typical settling time. Very few vendors guarantee a maximum value.

Varying compensation

Most JFET-input op amps have input capacitances from 4 to 8 pF. A small capacitor placed across the feedback resistor compensates for the pole created by the input capacitance. The amount of compensation needed depends on the performance you expect from the amplifier. Critical damping may give the fastest settling times to within very narrow error bands. In general, however, you'll improve the settling time, even to error bands as small as 0.01%, by providing compensation that yields slight underdamping. The optimum compensation is a function of the circuit and its layout, and you'll have to determine its value by experiment.

Proper compensation becomes critical when you use an op amp to convert the current output of a DAC to a voltage output. The output capacitance of the DAC, in parallel with stray capacitance and the input capacitance of the op amp, exacerbates any ringing and instability problems, and you'll have to optimize the compensation for the combination of settling speed and accuracy that you want.

The gain-bandwidth product (GBW) is adequate to describe the ac response, at any frequency, of single-pole amplifiers such as the 741. The more complex design of a JFET-input op amp such as PMI's OP-42 yields higher slew rates with greater stability, but it distorts the meaning of the GBW. Nevertheless, you can derive an approximation of the cutoff frequency for any closed-loop gain (A_{VCL}) from the following formula:

$$f_C=(GWB/A_{VCL}).$$

This approximation is adequate for most purposes and is valid for most amplifiers, including PMI's OP-42 and OP-44.

The slew rate (SR) of an amplifier largely determines the maximum frequency at which it can operate with large signals. You can calculate this frequency (known as the power bandwidth, or BW_P) from the equation $BW_P=SR/(\pi V\ p\text{-}p)$. An amplifier such as the OP-42, which has a 50V/μsec slew rate, can operate at frequencies above 800 kHz with only 1% distortion on a 20V p-p signal. The OP-44 has a BW_P that's greater than 1.5 MHz; it achieves a slew rate of 100V/μsec in applications that have a closed-loop gain greater than three.

PMI's OP-42 guarantees settling times of 1 μsec or less to an accuracy of 0.01%—that is, to within ±1-mV error bands—for a 10V input step. You can approximate settling times for input steps other than 10V by subtracting the slew time from the specification and adding the slew time for the desired output change. For example, to obtain the settling time for a 1V step, subtract the slew time for 10V (167 nsec at 60V/μsec) from the 800-nsec typ settling time. To this result (800−167=633 nsec) add the slew time for 1V (16.7 nsec) to obtain a calculated settling time of approximately 650 nsec to 0.01%. The OP-42's measured settling time for a 1V step is somewhat better, being less than 600 nsec.

Calculating error magnitudes

For a concrete example on which to base an examination of errors, assume a circuit consisting of the autozeroing amplifier of **Fig 1** on pg 162 as the first stage, and the S/H amplifier of **Fig 2** on pg 164 as the second stage. Provide zeroing pulses to the amplifier in the first stage once every millisecond to eliminate thermal drifts and offset problems.

For the purposes of this discussion, assume that IC_2 is a PMI OP-44, with a GBW of 50 MHz (think of the entire circuit of **Fig 1** as this gain stage). Because IC_2 operates with a gain of 100, the system bandwidth is 500 kHz before signals enter the S/H amplifier. The S/H circuit yields 2.5-μsec acquisition times and holds the output for 18 μsec; consequently, the sampling bandwidth is 50 kHz. Assume that the power supplies are well regulated so that you can ignore power-supply rejection. Also, ignore phase errors.

Assessing gain-stage errors

In the first stage, errors arise primarily from finite gain, common-mode rejection (CMR), and noise. Servo amplifier IC_4 nulls IC_2's offset voltage and drift; these values are no greater than 1 mV over the full temperature range, without additional adjustment. The drift is negligible during the periods between nulling. IC_4 also nulls the offset voltage caused by bias current flowing through the multiplexer. If you assume that source impedances are no greater than 1 kΩ, then the contribution traceable to bias current is less than 1.5 $\mu V \times A_{VCL}$, or an additional 1.5 mV. (This includes leakage current from the switches in the MUX-08.) At dc, the common-mode error is only 0.004% (essentially nonexistent), but at 50 kHz the CMR falls to 70 dB and can contribute an error of 0.03%.

You can express open-loop gain errors as a percentage of the signal; at dc, these errors are approximately equal to the percentage calculated from A_{VCL}/A_{VOL}. Both the OP-42 and the OP-44 have an open-loop gain of more than 500,000. At dc, the gain error is less than 0.02%, but at 50 kHz, gain errors can contribute amplitude errors as high as 0.5%. The amplitude error decreases rapidly as the operating frequency moves away from the 500-kHz cutoff frequency (f_C).

You can obtain an approximate value of the error, for any frequency f, from the formula

$$\epsilon_A \approx \tfrac{1}{2}(f/f_C)^2,$$

down to the frequency at which the formula yields a value that's less than the dc value. In **Fig 1**'s circuit, this point occurs at 10 kHz. Because the amplitude error is primarily a function of f_C, operating the amplifier at a lower closed-loop gain would result in a significantly smaller error at any given frequency.

You can calculate the noise by multiplying the square root of the bandwidth by the rms noise density. In a wideband amplifier, the noise is dominated by the high-frequency flatband noise, rather than by the higher-density low-frequency noise. For PMI's OP-42 amplifier, the flatband-noise density is typically 12 $nV/\sqrt{Hz}$. To get an idea of the worst-case performance, use 15 $nV/\sqrt{Hz}$, which yields a value of 10.6 μV rms at the input and 1 mV at the output. Always use the full bandwidth of the circuit for noise calculations, because noise frequencies higher than the maximum signal frequency can alias into the lower frequencies and affect the final value.

You'll see that, because error terms sum in an rms fashion, gain error is the dominant source of error. The OP-42 and OP-44 amplifiers minimize, but do not eliminate, these errors. Consequently, you'll find that the output of the autozeroing amplifier is accurate to within 0.5% at 50 kHz, and to within 0.02% at frequencies below 10 kHz, with the addition of a 7-mV noise contribution and 2.5 mV of offset error.

These gain-stage errors are passed on to the S/H amplifier, which has its own sources of error, arising from aperture time and aperture jitter, hold steps, droop, and finite CMR (think of the entire circuit of **Fig 2** as the S/H stage). However, because the amplifiers of the S/H stage operate at unity gain, they eliminate gain error that's caused by bandwidth limitations or high closed-loop gain, and they greatly reduce the other errors associated with the multiplexed stage.

You can simplify matters by

eliminating the input amplifier (IC_1) and driving the S/H buffer (IC_2) directly from the output of the multiplexed stage. Then the primary source of error affecting the output will consist of the hold step (1 mV) and acquisition error (0.01%). Errors arising from aperture uncertainty and aperture jitter will be minor and will add no more than 0.01%.

The CMR error can be more significant, depending on the frequency. It's difficult to estimate what frequency to use for calculating errors in the S/H stage; some designers use the dc specifications, on the assumption that the amplifier operates in dc mode after the hold settling time. This assumption would be true for long hold times, but in fact the S/H stage not only reproduces the primary waveform but also adds high-frequency components to form steps. For this reason you should always use actual operating frequencies in your error calculations. Consequently, at 50 kHz, the 70-dB CMR of the OP-42 amplifier can contribute 0.03% error. The error terms again sum in rms fashion to yield a total of slightly less than 0.04% error from the S/H stage. Noise is negligible in comparison with that delivered by the gain stage, and the dc offset is simply that of the OP-42, an additional 0.75 mV.

Improving performance

The total system error for both the gain stage and the S/H stage consequently becomes approximately 0.05% at frequencies less than 10 kHz and increases to 0.5% at 50 kHz. This is in addition to the 7-mV noise contribution and 2.25-mV dc offset. You could eliminate gain-stage errors by cascading two amplifiers, each with a gain of 10, instead of using a single amplifier with a gain of 100. The error terms contributed by the S/H stage would dominate in such a configuration.

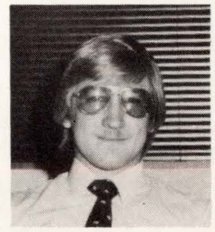
You can calibrate and eliminate many of the error terms discussed above. For example, in a system that uses a fast Fourier transform to examine the spectral content of a waveform, you could apply a correction factor to correct for gain roll-off at high frequencies. You could also correct for CMR errors by applying an additional correction factor based upon the signal level. DC offsets are simply eliminated by subtracting a constant term from the signal. Noise can be eliminated only by averaging many repetitive signals.

array of four transistors placed at the corners of a square. Two of these transistors, located at diagonally opposite corners, act as the log-conversion elements. Of the remaining two transistors, one (Q_4) acts as a heater and the other (Q_2) acts as a temperature sensor. IC_3 forces the V_T of Q_2 to a specific value by varying the current through Q_4, and it maintains this value by means of the thermal feedback between Q_2 and Q_4. The symmetrical layout of the IC ensures that the two log-conversion transistors are always at exactly the same temperature. The component values shown will maintain the MAT-04 die at approximately 60°C.

This operation may violate the rated specifications of the MAT-04 package and cause degradation of Q_4's β, but it does not hurt performance, because the characteristics of the heater are unimportant. You'll get the best results by encasing the MAT-04 package in thermally insulating foam, such as the urethane foam used for housing insulation.

To null the amplifier, you begin by setting the input voltage to 1 mV. Adjust the offset voltage of IC_1 for an output of 3V. Next, raise the input to 10V and adjust the gain for an output of -1V. These two adjustments are interactive, so you may have to repeat them several times. You can modify the zero-crossing point by changing the value of resistor R_3. **EDN**

Author's biography



Peter Henry is a product marketing engineer at Precision Monolithics Inc (Santa Clara, CA). He is responsible for the definition and introduction of new analog products. Peter joined PMI in 1985 after graduating from the University of California at Berkeley, where he earned a BA in physics. In his spare time he enjoys scuba diving and 4-wheel-driving.

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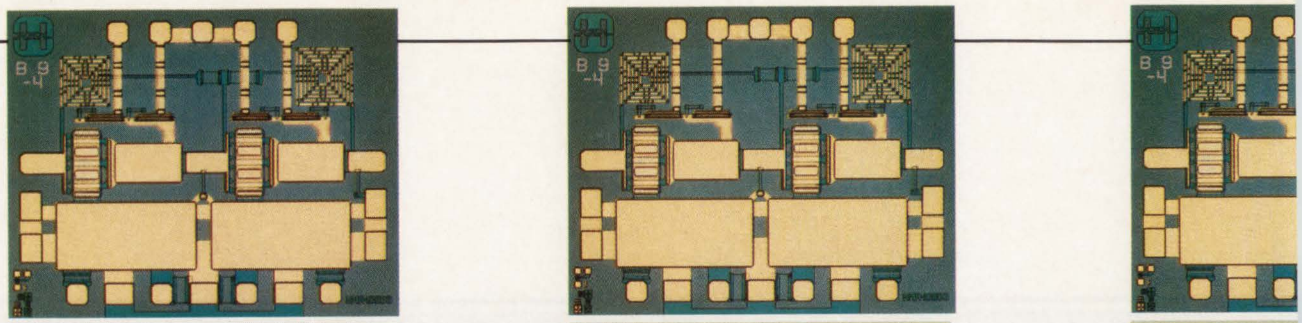

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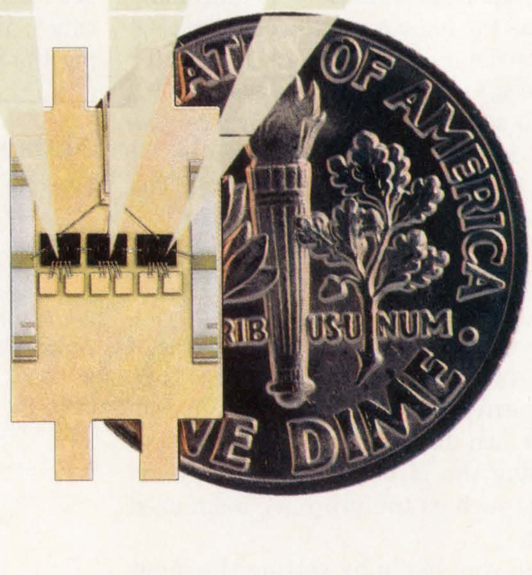

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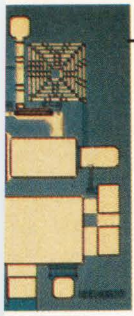

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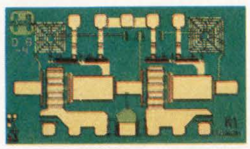

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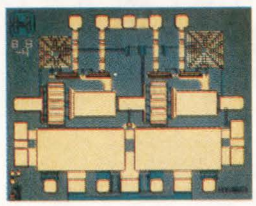

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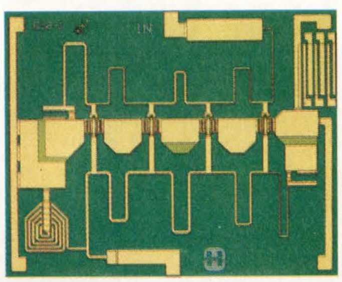

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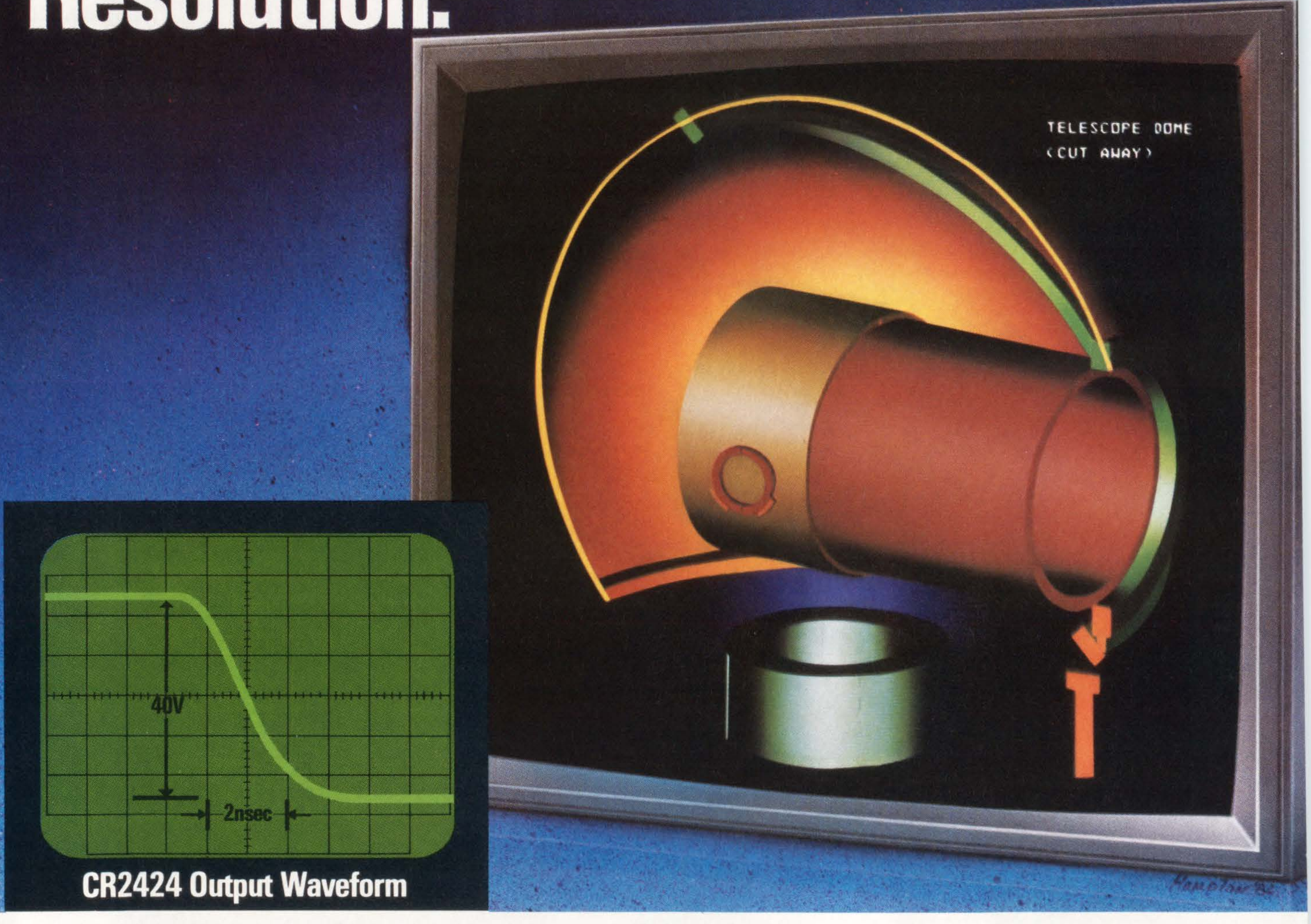

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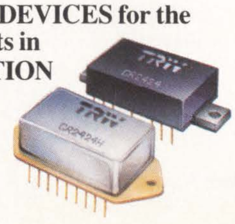

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CIRCLE NO 146

Simple circuits provide accurate ac testing of op amps

Op amps' dc characteristics are usually well controlled by vendor testing, but the parts' ac performance rarely is. You can use familiar test equipment and some simple test circuits to test op amps' ac characteristics.

Barry Harvey, *Elantec*

When designing with op amps, you often need to measure the parts' most commonly used ac parameters quickly and accurately. These ac characteristics often vary among parts from different vendors, and they can even vary among parts from different manufacturing lots. Further, over the life of a product, the vendor may insert subtle changes that render the part's data-sheet curves less than representative. You can use commercially available laboratory test equipment and some simple test circuits to test op amps for open-loop gain and phase, input and output impedance, power-supply rejection ratio (PSRR), and common-mode rejection ratio (CMRR). (**Ref 1** outlines a method for measuring an op amp's settling time.)

Just as the oscilloscope is the key instrument for taking voltage-vs-time measurements, the network analyzer with gain- and phase-measurement capability is the key instrument for taking steady-state ac measurements. To take these measurements, you can use an instrument like the Hewlett-Packard 3577A network analyzer and gain/phase meter or the 4192A (or 4194A) 4-wire ohmmeter and gain/phase meter. Each of these machines contains an oscillator that's controllable in frequency and amplitude and a gain/phase measurement system. The latter two each have a 4-wire (floating force and sense) ac ohmmeter. All their functions are programmable via the IEEE-488 bus. If you don't have one of these instruments, you can take all these measurements with a collection of other instruments: an oscillator, a gain/phase meter, a vector/impedance meter, and S-parameter equipment.

When you measure an op amp's open-loop characteristics, you don't have to run the op amp in open-loop mode. However, all op amps have too much dc gain for you to bias their outputs properly without feedback, so some feedback will be required. You can use a test circuit like the one shown in **Fig 1a** to measure the amplifier's open-loop characteristics. In the circuit, the op amp is connected in a "gain of −10" arrangement, a configuration in which almost all devices are stable.

The gain/phase meter measures the V_{OUT}/V_{IN} of the amplifier. V_{OUT}/V_{IN} is the precise definition of open-loop gain, assuming that the impedance of the parallel combination of R_L and C_L at the operating frequency (f_O) is much larger than the Z_{OUT} of the amplifier at that frequency. Alternatively, you can make the combination of R_L and C_L similar to the conditions under which the amplifier will actually be used, and then measure the effective open-loop characteristics of the amplifier.

The network analyzer with gain/phase measurement capability is the key instrument for steady-state ac measurement.

You can adjust the dc offset level of the oscillator to move the op amp's dc output level to your region of interest. This adjustment may be necessary at higher frequencies, where the behavior of most op amps changes significantly with the dc level.

Note that although the open-loop measurement is uncorrupted in **Fig 1a**, the closed-loop gain at high frequencies is affected by the probe capacitance at the inverting input to the op amp. Standard oscilloscope probes are compatible with gain/phase-meter inputs, but their capacitance may cause oscillations of the amplifier in a closed loop. A 1× probe will extend the dynamic range of measurement by 20 dB at the gain/phase meter (in comparison with a 10× probe), but the probe's large capacitance will require you to insert approximately 10 pF of feedback capacitance (C_F). A 10× probe may not require feedback capacitance. An active 1× FET probe is even better; the circuit is usually not disturbed by the small input capacitance of the probe, and the probe does not attenuate signals, so it enhances the signal-to-noise ratio and the dynamic range of the gain/phase measurement.

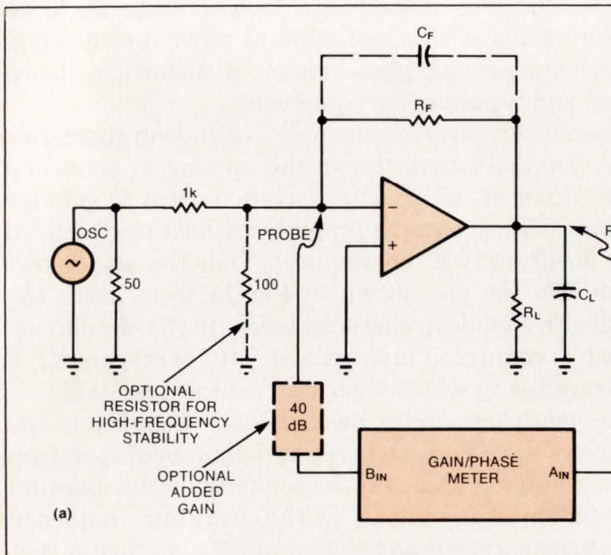
You can verify the ac balance of the probes by measuring the oscillator output with both probes connected, replacing the op amp with a shorting wire, and monitoring the deviation from 0 dB between them. You can log the 0-dB error and subtract it from future readings, or you can adjust the probes to balance by using their trimmers.

If you wish, you can use active circuit buffers instead of probes, but the buffers will require an additional gain calculation. Tektronix's P6201 probes can drive a 50Ω load at the gain/phase input, so you can use long cables (which should be of equal length) between the device and the meter.

When you're using the open-loop scheme, it's important that you maximize the signal levels to improve the S/N ratio of the measurements. Remember, the gain/phase meter will be called upon to deal with 100-dB ratios at low frequencies. The larger signal at the device output is the phase reference for the meter. You can increase the B input signal to the meter by adding an external 40 dB of gain. Of course, you'll have to calibrate the two probes, plus the 40-dB amplifier, by replacing the device under test with a wire from input to output as before.

The amplifier has three built-in limitations related to potential signal levels. The first is the slew-rate limitation of the output. In general, in order to preserve the linearity of the output, you should keep the output rms level to less than the quantity slew rate/($30f_O$). The second limitation is that the device's output voltage and current are limited by the power-supply voltage and the values of the load resistance (R_L) and load capacitance (C_L) at the operating frequency.

The third limitation is more subtle. The input stage



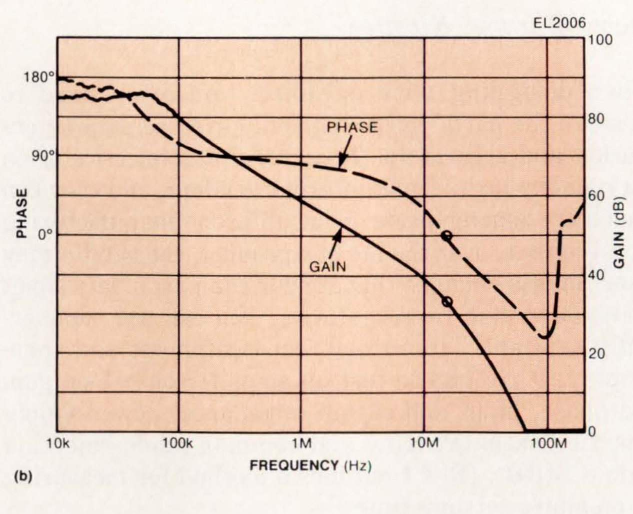


Fig 1—To measure an op amp's open-loop characteristics, *you can connect the op amp in a "gain of −10" arrangement* ***(a)****, in which most devices are stable. The gain/phase meter measures the V_{OUT}/V_{IN} of the amplifier. You can use the optional 40-dB gain block to increase the input signal to the meter. The plot* ***(b)*** *shows the gain and phase of the EL2006 op amp as a function of frequency. Where the gain is 34 dB, zero phase occurs at 15 MHz.*

will be linear for small inputs only. At high frequencies, the device's gain will fall and the inverting input signal level will rise. In general, you should keep the rms input level no higher than ~18 mV at any frequency.

You should use an oscilloscope to determine whether the circuit or its connections are causing the op amp to oscillate. To keep the test setup stable, you should always have a proper 50Ω termination for R_{IN}. Although the setup requires you to observe several rules, the measurement technique is accurate and repeatable once you've established the operating conditions under which you will test your op amp.

Fig 1b shows a plot of the gain and phase of an op amp, the EL2006, taken with the test setup in **Fig 1a,** minus the compensating capacitor. (The extra resistor at the summing junction of **Fig 1a** maintains closed-loop stability.) An HP 3577A was used both to take the measurements and to control the plotter. As the cursors in **Fig 1b** show, zero phase occurs at 15 MHz where the gain is 34 dB, or 50 V/V. The plot indicates that the op amp's closed-loop gain of 100 would have a −3-dB frequency of about 9.5 MHz and a phase margin of 38°, for an overall gain-bandwidth product of nearly 1 GHz.

To take this measurement, you should make a small RF-worthy fixture for the device and mount the fixture directly on the BNC connectors of the 3577A's front panel, thus eliminating cabling or loading effects. Solid coaxial cables within the box provide the best measurement accuracies when your test frequency is above 50 MHz. Also, unless you adhere to diligent construction practices, you're better off selecting 1-MΩ input impedance rather than 50Ω.

Use ac ohmmeter to measure input impedance

Fig 2 shows a very simple method of measuring an op amp's input impedance. The 4-wire ac ohmmeter arrangement of the 4192A is directly connected to the amplifier's input. H_{CURR} and L_{CURR} are the current-forcing terminals of the ohmmeter, and H_{POT} and L_{POT} are the potentiometric (voltage-sense) inputs. In this machine, the shields of the four coaxial cables (the cables should be of equal length) are connected to one another, but they are not connected to the device ground.

You perform the calibration for the open-circuit measurement with the device under test out of its socket so that the wiring and socket capacitances are zeroed out. You need to be aware of two operating considerations. First, you should use the smallest possible rms-signal drive level (5 mV, if the S/N ratio permits). And then, you should make certain that the input signal doesn't cause the output to flail about, because this large output signal can be fed back to the input via the feedback capacitance, severely affecting your measurements.

To this end, you need to set up a small dc input offset voltage to drive the device's output to the supply-voltage level. When you supply 5 mV of signal input to the test circuit, a 10-mV offset will clamp the output as long as the device's dc offset doesn't exceed about 2.5 mV. It's wise to monitor the device's output with an oscilloscope to ensure that the output sits at the supply level with a minimum of input offset voltage.

Measuring output impedance

You can measure an op amp's output impedance when the op amp is in either the closed-loop-gain or the open-loop-gain configuration. You can use the circuit shown in **Fig 3a** for testing an op amp connected as a unity-gain buffer. You zero the 4192A by replacing the device with a wire from output to ground at the socket. In this way, you effectively null the wiring inductance. The 10-kΩ resistor serves to isolate the low output impedance of the device from the 50Ω impedance of H_{CURR}.

This isolation ensures that currents smaller than the idling current of the output stage can be forced into the device so that any crossover distortion of the device will not affect the readings. You then vary the oscillator level to confirm that little measurement error is occurring. You can also adjust the dc level of the oscillator output to see if the output impedance of the device changes with current. You can use any gain-feedback

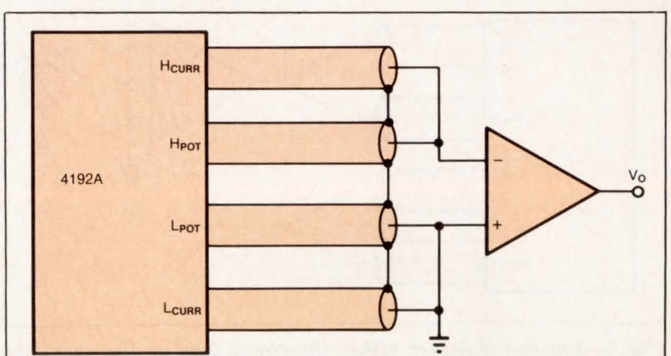


Fig 2—To measure an op amp's input impedance, *you connect the 4-wire ac ohmmeter arrangement of the HP 4192A directly to the input of the amplifier. To obtain accurate measurements, you should use the smallest possible drive signal.*

You can measure the open-loop characteristics of an op amp without running the op amp in open-loop mode.

configuration you desire, depending on how you're ultimately going to use the device.

Fig 3b shows a way to measure open-loop output impedance. The operating frequency is set high enough to limit the open-loop gain to <10,000. Thus, the device's closed-loop gain of 10,000 will not perturb the reading. The dc voltage source, V_{OS}, nulls the device's output offset near ground.

Measuring power-supply rejection ratio

The simplest way of measuring an amplifier's PSRR is to place a resistor of 10Ω or less (depending on the op amp you're testing) between the negative supply pin of the device and its bypassed power supply **(Fig 4a)** and couple a small ac signal across the resistor. You measure the positive supply's PSRR similarly. Because PSRR is a measure of the device's induced input offset voltage, which is caused by the supply signal, the quantity B/A on the gain/phase meter is a direct reading. As before, you connect the A input (phase reference) of the meter to the largest available signal to obtain the best noise performance.

This circuit has a few performance limitations. For example, at low frequencies, the PSRR of many op amps can exceed 100 dB, and little signal is available at the device output for you to measure without severe noise problems. Another limitation is that, at some power-supply slew rate, the output PSRR signal will be distorted and inaccurate. By varying the oscillator drive, you can observe the B/A ratio to vary at some large amplitude. You will have to reduce the drive to substantially below that amplitude level, and again, the low S/N ratio will affect the readings.

Fig 4b shows an improved setup. In this circuit, the feedback ratio requires the op amp to provide a gain of 1000, which enhances the low-frequency PSRR range by 60 dB at the frequencies where the PSRR is greatest. At most frequencies, the op amp will not be able to

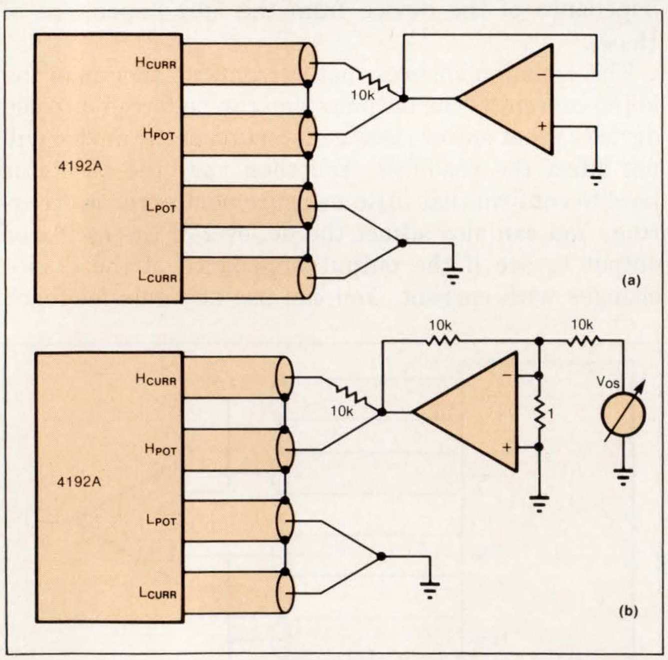


Fig 3—You can measure either the closed-loop or the open-loop output impedance of an op amp. *The circuit in **a** is for testing an op amp connected as a unity-gain buffer. The circuit in **b** measures open-loop output impedance. You should operate the device at a frequency high enough to limit the open-loop gain to less than 10,000.*

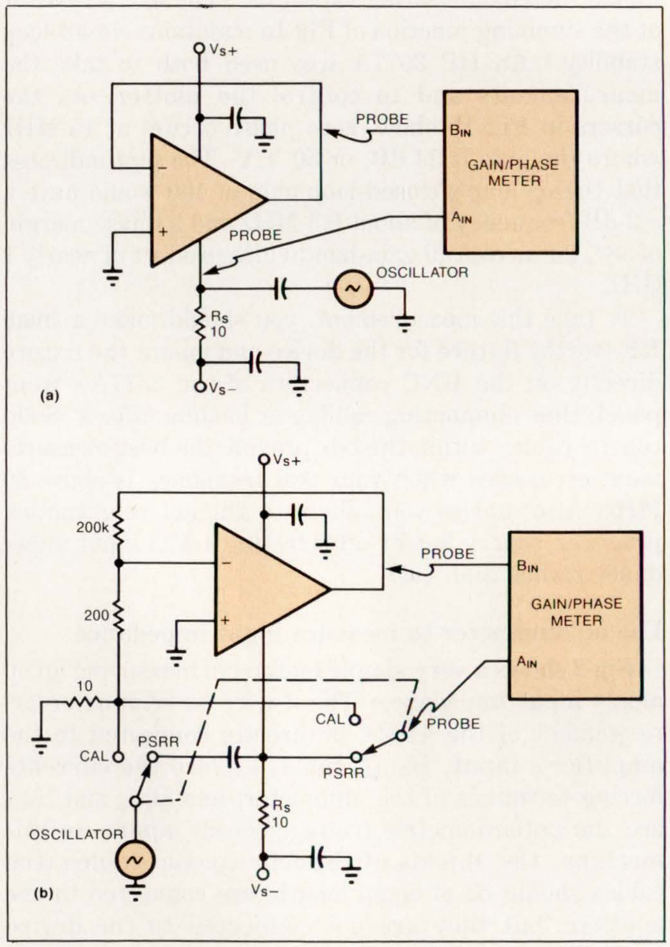


Fig 4—A simple way to measure an amplifier's PSRR *is shown in **a**, in which a small ac component from the oscillator is superimposed on the supply voltage. The quantity B/A on the gain/phase meter provides a direct reading of PSRR. The circuit in **b** provides an improved method of measuring PSRR. In this circuit, the op amp provides a gain of 1000. This gain enhances the low-frequency PSRR range by some 60 dB, and you must normalize B/A readings.*

provide the full gain, and your PSRR calibration will fail.

To provide a means of calibration, you can switch the oscillator and gain/phase meter to measure the actual gain at the operating frequency, and then you can use that gain when you perform the PSRR measurement. To normalize the PSRR reading, you can use the equation PSRR=$gain_f \times A/B$ when the test setup is in PSRR mode. For the test setup in **Fig 4b,** this equation holds true at a gain bandwidth beyond that of the device under test. The equation doesn't hold true for the setup in **Fig 4a**. Again, you must adjust the input signal so that the amplitude of the output signal remains within limits.

Measuring common-mode rejection ratio

Fig 5 shows the common method of measuring CMRR. This scheme requires that an oscillator drive the supplies with respect to the noninverting input of the op amp. The supply variations cause a variation in V_{OS} at the input of the amplifier; the variation, or CMRR, is measured at the B input of the gain/phase meter. The amplifier could operate at a closed-loop gain of 1000 or so to boost the signal available to the meter.

The problem with the approach shown in **Fig 5** is that the output of the circuit, which is expected to be at ground for a device with infinite CMRR, also sees the supply variations. To move the output by x volts with respect to ground (the supplies are at ac ground) will require an input signal of x/gain volts, where gain is measured at the operating frequency. This signal can't be distinguished from the valid CMRR-induced signal that is seen at the input. Thus, you can't measure a CMRR greater than the gain of the amplifier at the operating frequency.

The circuit shown in **Fig 6** uses the V_{OS} balance pins of the amplifier as a feedback path. By providing a means of feedback that is separate from the normal inputs of the amplifier, you can connect the inputs and drive them, instead of driving the supplies, with the oscillator. Thus, you can easily measure a CMRR greater than the open-loop gain over wide frequency ranges.

One of the offset null pins will provide the overall negative phase required to set a reasonable dc output. The 4-transistor circuit shown is basically a 2/100-kΩ transconductance feedback path into the offset null pins, which normally provide a forward conductance path to the device output. For supply voltages slightly greater than those provided to the op amp, the collectors of the transistors will comply with the internal bias level of the offset null pins.

This feedback arrangement provides a CMRR gain that is dependent on the device under test and is typically from 10 to 1000 with the resistor values and supply voltages shown. To find the forward gain at the operating frequency, you must switch to the calibrate mode. As before, the input signal must be in the linear range of the device. You then set the switch to the CMRR mode; the corrected CMRR value is $gain_f \times A/B$

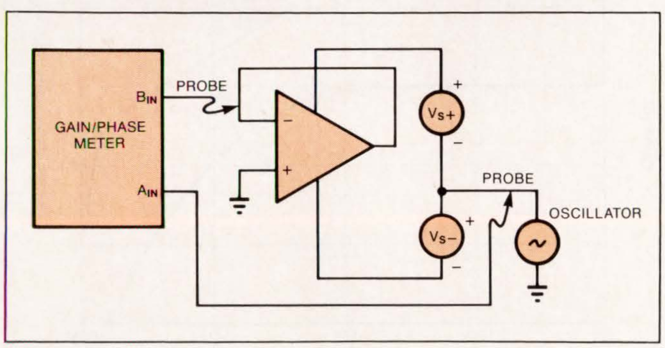


Fig 5—This circuit provides a common method of measuring an op amp's CMRR. *The oscillator drives the supplies with respect to the noninverting input of the op amp. Supply variations cause a V_{OS} variation at the amplifier's input; this variation is measured at the B input of the gain/phase meter. The problem with this approach is that the op amp's output also sees the supply-voltage variations.*

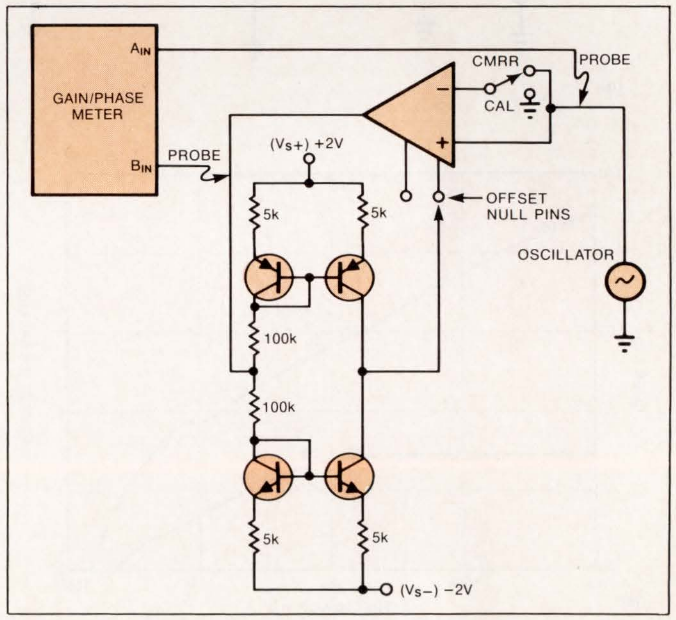


Fig 6—This circuit measures an op amp's CMRR. *The setup uses the V_{OS} balance pins of the amplifier as a feedback path. You connect the inputs and drive them with the oscillator. Thus, you can measure a CMRR greater than the open-loop gain over a wide frequency range.*

A gain/phase meter measures an op amp's V_{OUT}/V_{IN}, which is the precise definition of open-loop gain.

when the test setup is in the calibrate mode.

Fig 7a shows an even simpler method of measuring CMRR that you can use to test op amps (such as the EL2006 or ELH0032) that have balance, or offset null, pins. In this setup, the feedback path is simply a 62-kΩ resistor, a value that does not severely upset the bias of the EL2006. (This resistor value depends on the op amp under test.) You can offset the ac input with an external dc V_{CM} level. With the switch in the calibrate position, you take a normalization curve (output vs frequency). You then throw the switch to the measure position and multiply the resultant Y data (output vs frequency) by the previously taken calibration data to obtain the normalized CMRR.

Fig 7b shows the calibration and the normalized CMRR results for an EL2006 amplifier. Note that the scales are offset between the curves because of the large dynamic range. This method yields reasonably quiet data even at the 130-dB measurement obtained at 10 kHz. The EL2006 is an improved version of the

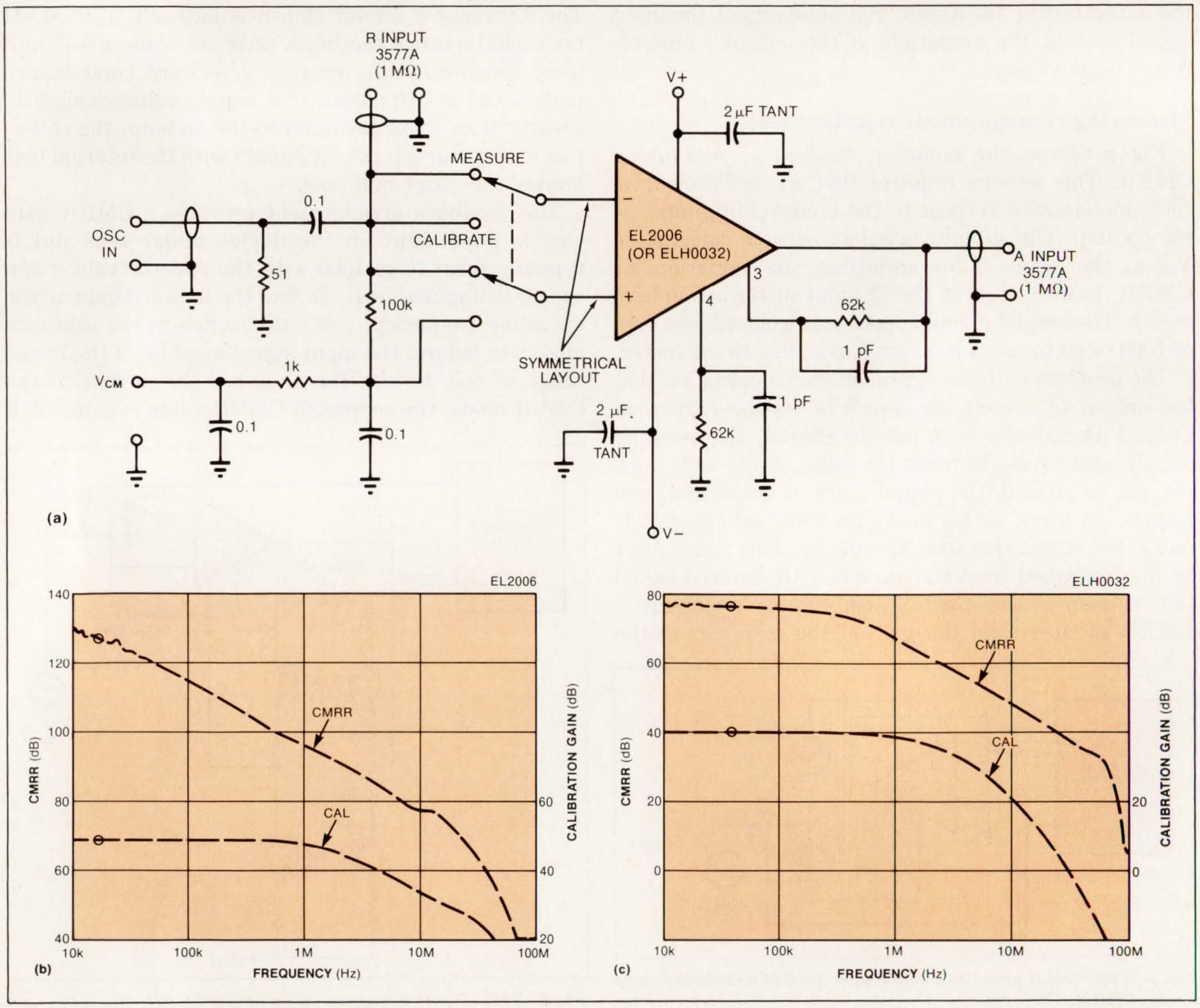


Fig 7—A simple method of measuring CMRR, *useful for op amps that have offset null pins (such as the EL2006 and ELH0032), is shown in* ***a.*** *The feedback path is a 62-kΩ resistor, and you can offset the ac input with an external dc V_{CM} level. Plot* ***b*** *shows the calibration and the normalized CMRR results for the EL2006. The scales are offset because of the large dynamic range. Plot* ***c*** *shows the curves for the earlier ELH0032 amplifier. At 1 MHz, the ELH0032 has a CMRR of only 68 dB, whereas the EL2006 has 96 dB.*

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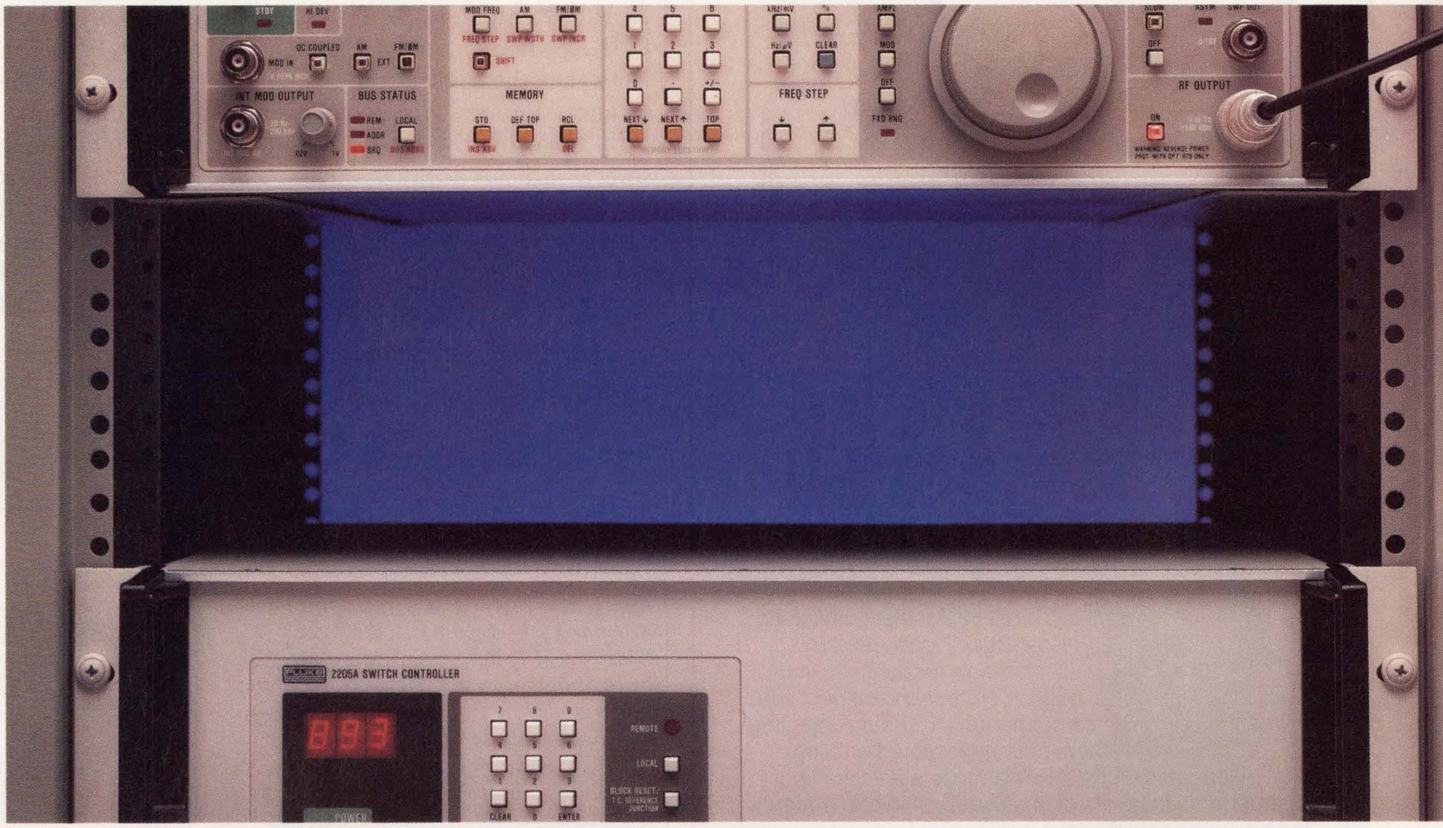

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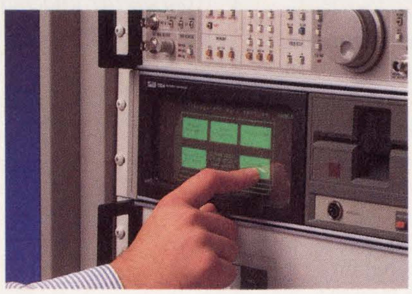

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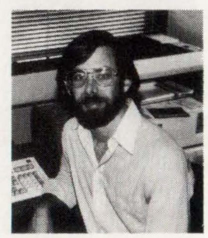
ELH0032 amplifier. At 1 MHz, the EL2006 has a 96-dB CMRR, whereas the ELH0032 has only 68 dB **(Fig 7c)**. Note that the calibration gain is different, because the op amps' internal circuit values are slightly different.

By following the procedures described, you can take several difficult ac measurements of op amps with only a few specialized instruments and a minimum of added circuitry. The key is to measure ratios, not absolute values, and to normalize the results with the same measurement equipment. **EDN**

Reference

1. Harvey, Barry, "Take the guesswork out of settling-time measurements," *EDN*, September 19, 1985, pg 177.

Author's biography



Barry Harvey is a senior design engineer for high-speed analog ICs at Elantec (Milpitas, CA), where he has worked for one year. He was previously employed at Precision Monolithics, Siliconix (both of Santa Clara, CA), and AMD (Sunnyvale, CA). Barry has an MSEE from Stanford University, and he has been granted two patents. In his spare time he enjoys playing guitar and mandolin and programming his Amiga computer.

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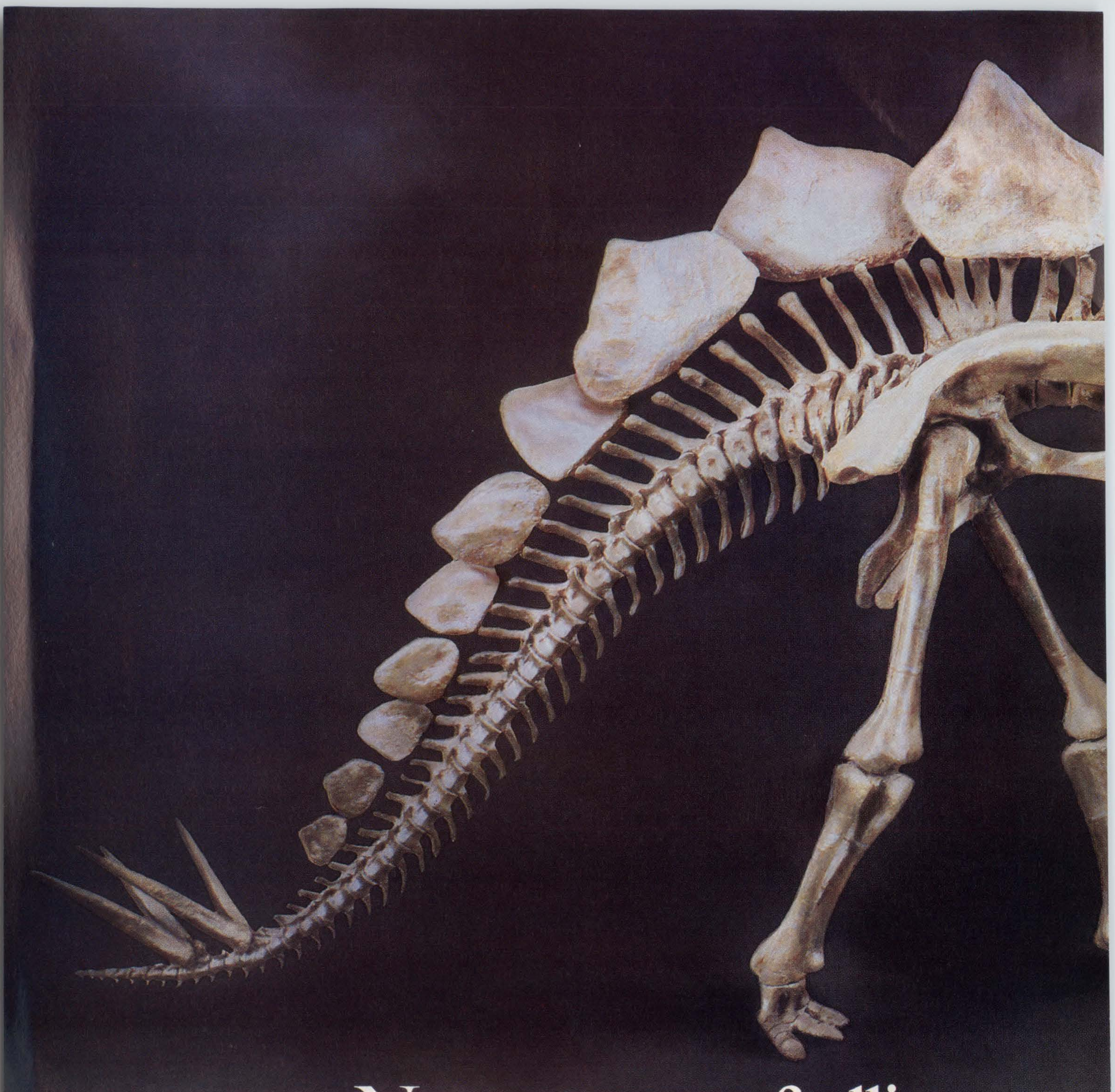

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TEXAS INSTRUMENTS REPORTS ON

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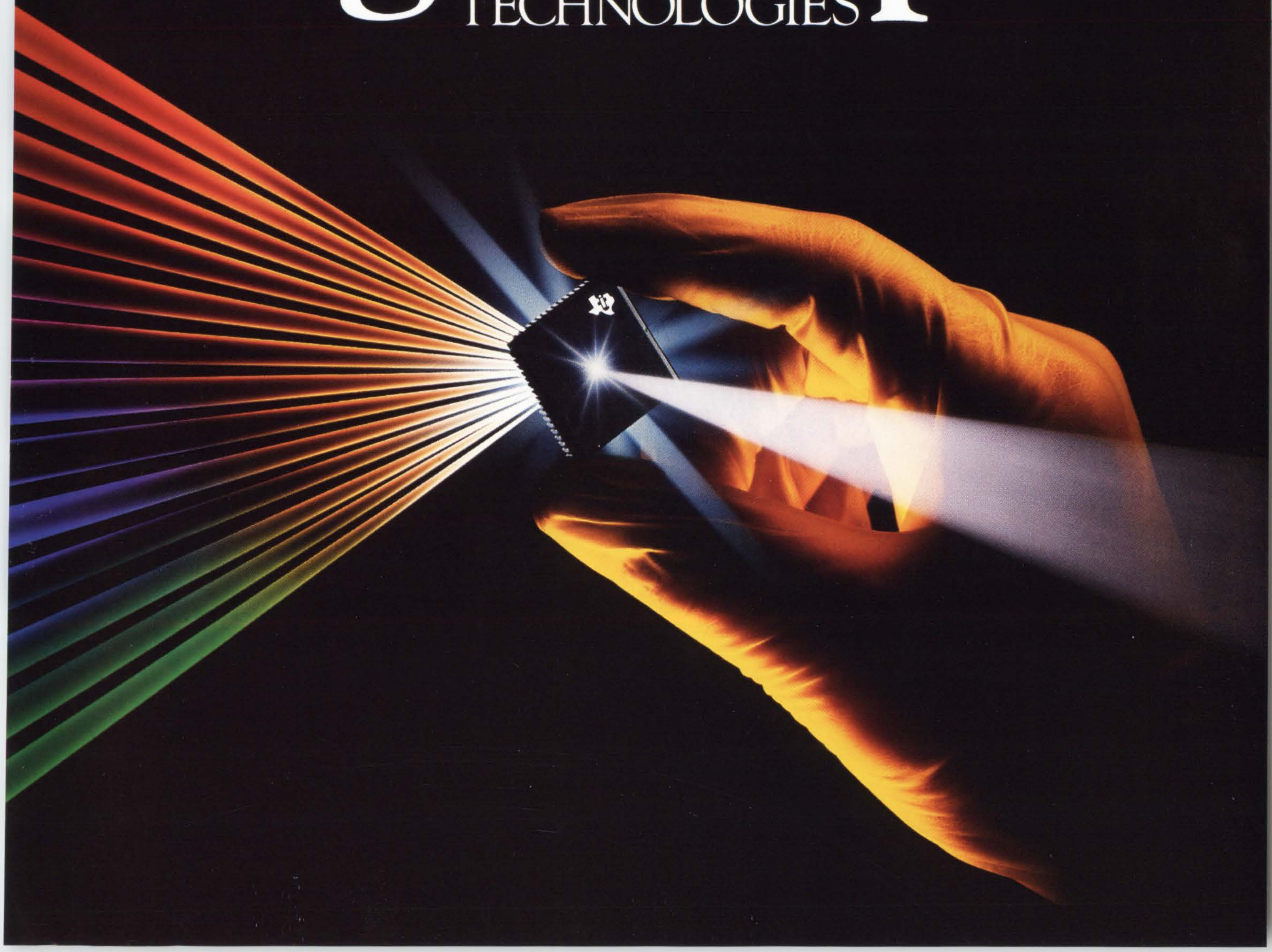

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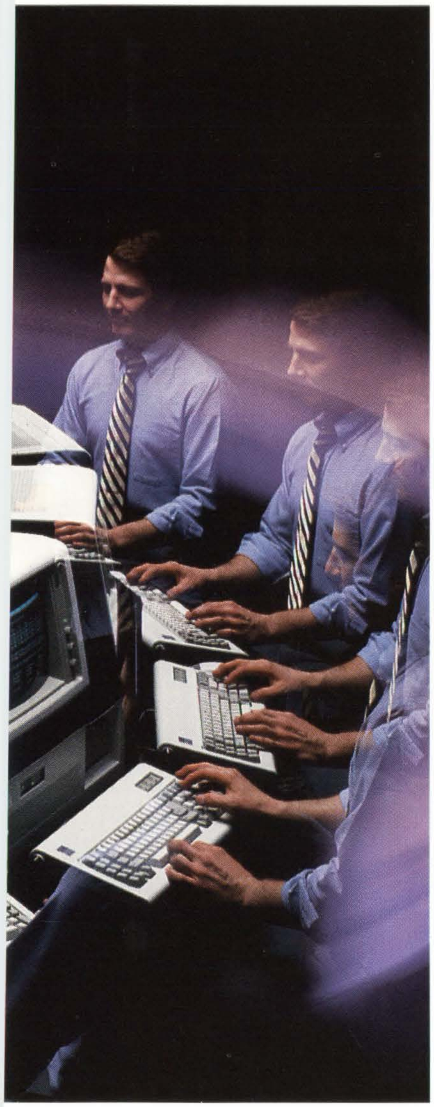

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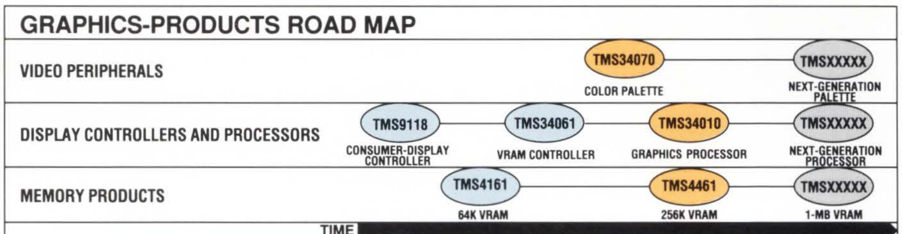

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ProDesign II™	American Small Business Computers
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TEXAS INSTRUMENTS

Low-cost circuits maintain quality of multiplexed video signals

Because video signals often pass through many black boxes and levels of interconnection, you must design your video switching circuitry to accommodate the attendant cumulative signal degradation.

Greg Schaffer, *Maxim Integrated Products*

Patching a video system together may seem as easy as hooking up some cables to the appropriate boxes and then turning on the power, and for existing video systems it may be just that simple. However, if you're designing the circuits that provide the link between several video signals, the seemingly simple task of switching the signals and driving them down 75Ω cables can prove troublesome.

Commercial television stations have assigned frequency bands that are 6 MHz wide. Television transmitters limit the bandwidth of their video signals to about 4 MHz. As a video signal travels from a camera to an antenna, it passes through many levels of interconnection, each of which contributes an error component. To minimize accumulative errors due to frequency and phase distortion, TV studio facilities normally maintain bandwidths about twice that of the transmitters; you must design your studio video conditioning and routing equipment such that it maintains a signal to within 1 dB at 8 MHz, even after the signal has gone through several cascaded circuits.

You can only achieve this level of signal preservation by keeping the error contribution from each individual circuit substantially lower than the 1-dB at 8-MHz figure might indicate. Note the following −3-dB bandwidths ($f_{-3\,dB}$) required of each of n cascaded circuits to give an overall frequency response of −1 dB at 8 MHz:

For n=1, f_{-3dB}=15.72 MHz
For n=2, f_{-3dB}=22.90 MHz
For n=3, f_{-3dB}=28.32 MHz
For n=4, f_{-3dB}=32.86 MHz
For n=5, f_{-3dB}=36.85 MHz
For n=6, f_{-3dB}=40.45 MHz.

Note that a system with six stages requires that each of the cascaded components have a −3-dB bandwidth of about 40 MHz to ensure a total system response of −1 dB at 8 MHz.

A brute-force approach to this problem of signal degradation will work. A wideband amplifier such as the 3554 (80 MHz) is effective, and it also provides enough current output (100 mA) to act as a distribution amplifier (a commonly used circuit in video applications). In **Fig 1**, the circuit is configured to run at a closed-loop gain of 2. This gain compensates for the loss due to the back-termination resistors. The signal response of the circuit falls to about −3 dB at 40 MHz.

A major difficulty with these high-speed amplifiers is that they are very layout-sensitive.

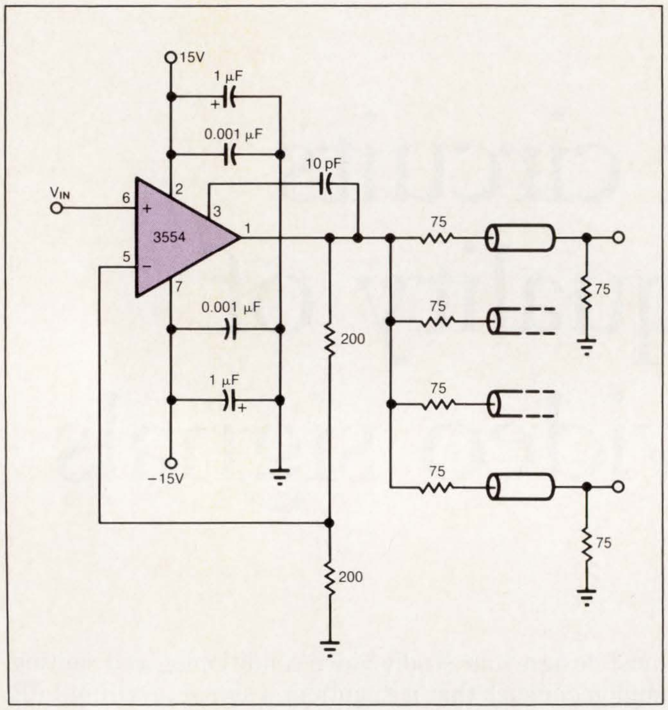

Fig 1—The 3554 amplifier has the drive capability *to drive several video cables; it's shown here configured as a distribution amplifier.*

High-speed power amplifiers such as the 3554 consume 1W—not an uncommon figure when driving several cables.

Another wideband, higher-speed, amplifier, the NE5539, has a −3-dB bandwidth of 100 MHz when operating at a gain of 2. This part has limited output-voltage-swing capabilities, but it is capable of driving a single video cable. When driving such a cable, the NE5539 generally requires a pull-down resistor from the output to the negative supply.

Although effective, high-speed amplifiers don't provide the optimal solution. High-quality video components—those that give a flat frequency response out to 10 MHz—tend to be expensive, power-hungry, and layout-sensitive. Among other things, you must carefully bypass the power supply pins on the chips; the bypass capacitors you use must have very short leads in order to minimize inductance. Also, when employing these parts, you should use ground planes extensively. To help you use the parts properly, however, manufacturers do provide drawings of proper pc-board layouts.

Fortunately, if your system doesn't have to have a flat frequency response to 10 MHz, and you only need to switch a couple of video signals, you can build low-cost

Video switches present their own peculiar problems

Video switches differ from conventional analog switches. Whereas traditional analog switches are optimized for dc operation, video switches are optimized for ac operation. Typically an analog switch will exhibit about 50 dB of off-isolation at 10 MHz; in contrast, a video switch's off-isolation at 10 MHz is 70 dB.

In a common video-switch configuration **(Fig A)**, two bilateral switches are configured in series, and another switch shunts them to form a T switch. The n_1, n_2, p_1, and p_2 regions are on while n_3 and p_3 are off and vice versa. In the off state, some of the input signal is coupled through to n_2 and p_2, but n_3 and p_3 are on, and thus the switch shunts most of the signal to ground. This T configuration provides the high off-isolation.

Often, a video switch is configured to directly drive 75Ω loads, but because the switch's on-resistance can go as high as 200Ω, the resulting signal loss through the switch can be significant. For example, a 100Ω switch driving a 75Ω load will cause a 7.4-dB loss in signal strength. The on-resistance also varies with voltage, which can cause differential-gain errors.

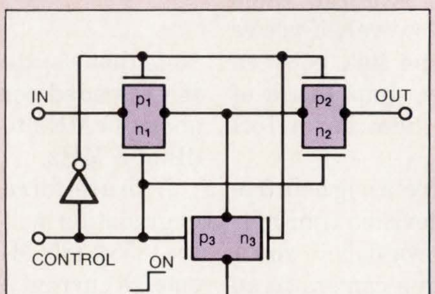

Fig A—A video switch's typical T configuration *improves off-isolation.*

When the switch is off, the cable is unterminated, but, when the switch is on, the cable is terminated with a 175Ω load—quite a mismatch between the cable and termination. To avoid mismatch problems, you should terminate the cable directly with a 75Ω resistor, then add the switch, and follow that with a buffer or amplifier to drive the output video cable.

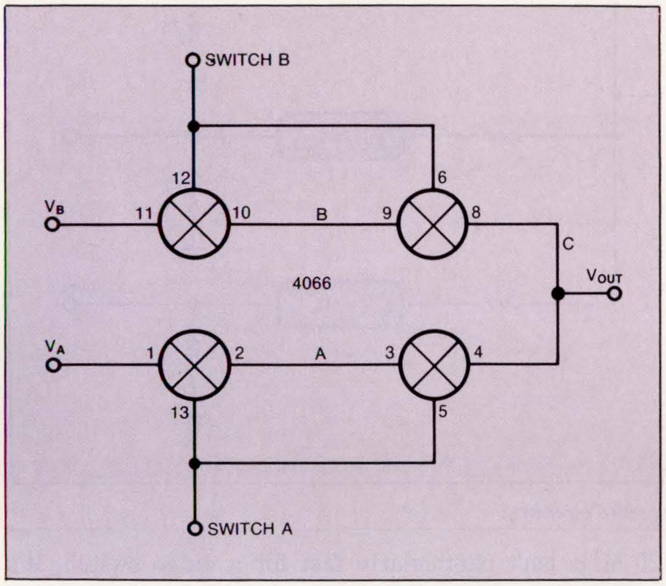

Fig 2—You can configure a 4066, *with its bilateral switches, as a video multiplexer.*

video-switching circuits that give −3-dB bandwidths as high as 10 MHz. The most basic element is the switch itself (see **box,** "Video switches present their own peculiar problems"). A good video switch is judged on the basis of three primary characteristics: off-isolation, crosstalk isolation, and bandwidth. Off-isolation is a measure of how much of a video signal gets through an off switch when the switch is supposed to be blocking the signal. Crosstalk isolation is a measure of how much of a signal is coupled inadvertently from channel to channel within the switch.

A CMOS 4066 switch shows promise as far as its bandwidth (−3 dB at 65 MHz) is concerned. However, feedthrough attenuation is only 50 dB at 1 MHz, and it should be an order of magnitude better than that. A 60-dB isolation at 4 MHz is satisfactory. You can achieve this level by using three bilateral switches of a 4066 in a T configuration, configuring two 4066s to make a 1-pole double-throw switch.

As an alternative solution to this feedthrough isola-

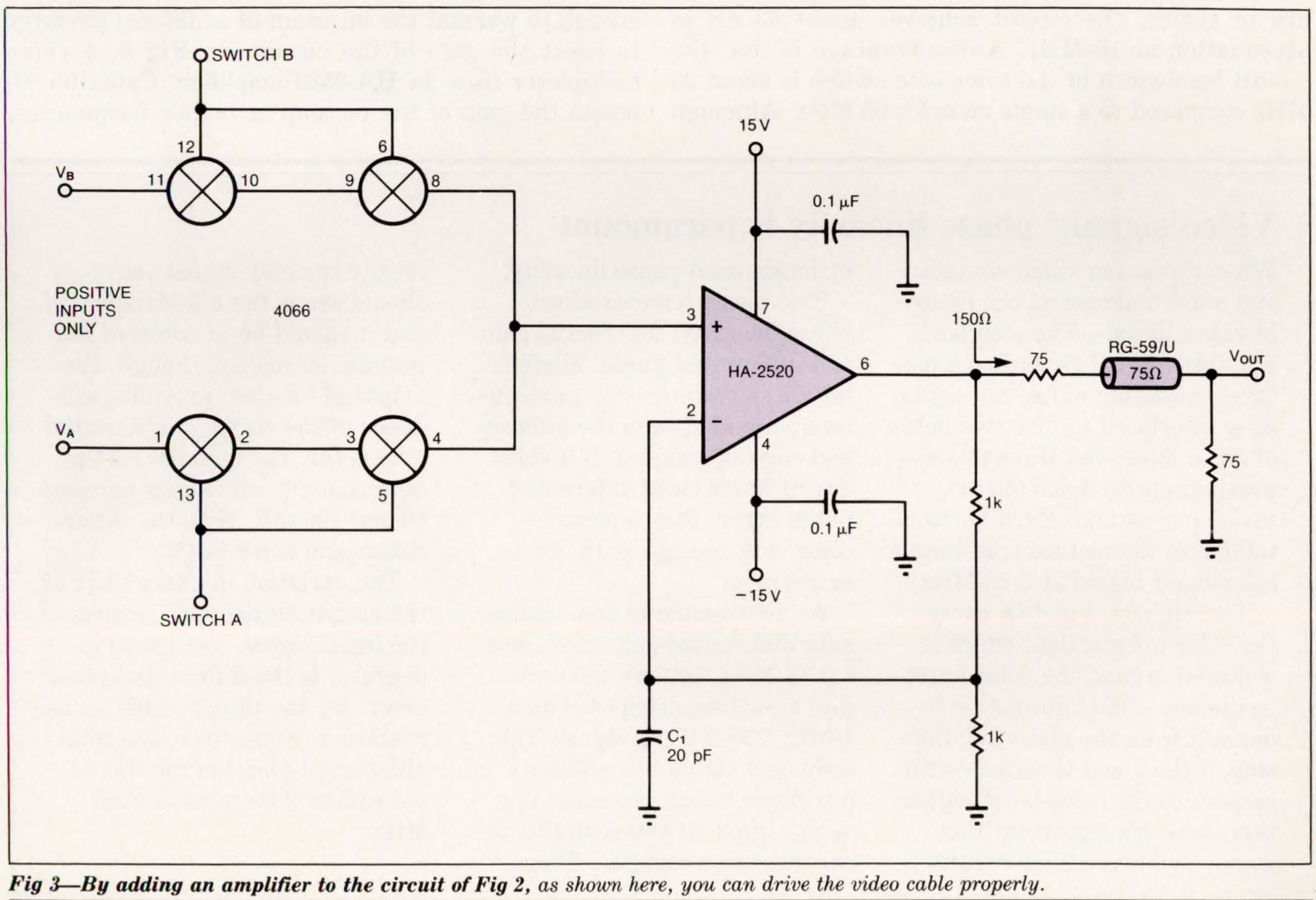

Fig 3—By adding an amplifier to the circuit of Fig 2, *as shown here, you can drive the video cable properly.*

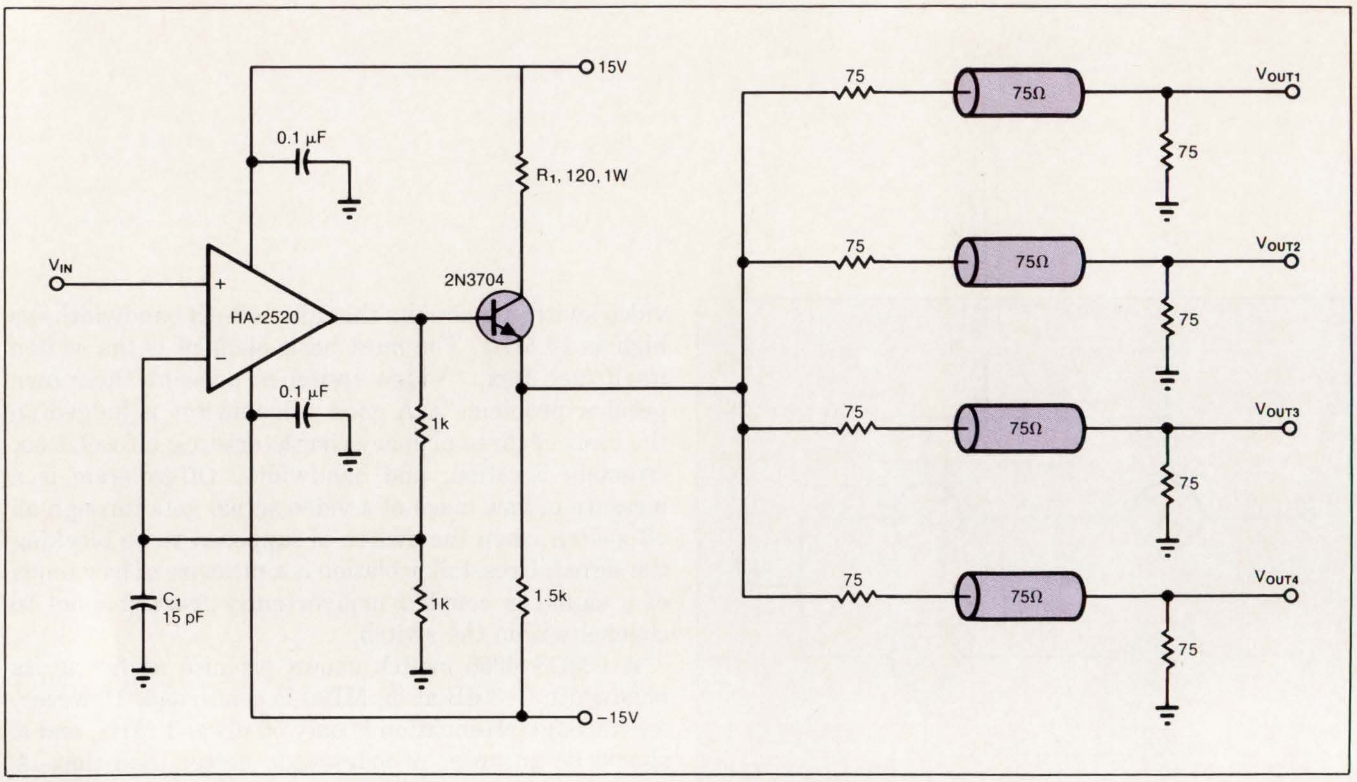

***Fig 4—An emitter-follower allows you** to boost the output drive of your video circuitry.*

tion problem, connect two bilateral switches in series to form a quasi-T switch (**Fig 2**). Parasitic capacitance at points A, B, and C shunt the signal to ground when the switches are in the off state. Because the two switches are in series, the circuit achieves about 63 dB of attenuation at 10 MHz. A disadvantage is that the −3-dB bandwidth of the composite switch is about 25 MHz compared to a single switch's 65 MHz. Although 25 MHz isn't particularly fast for a video switch, it's sufficient for many video switching applications.

A typical video application entails a circuit driving a 150Ω load, which can reduce the gain of an amplifier enough to warrant the inclusion of additional circuitry to boost the gain of the circuit. In **Fig 3**, a video multiplexer uses an HA-2520 amplifier. Capacitor C_1 boosts the gain of the op amp at higher frequencies,

Video signals' phase linearity is paramount

When designing video circuits, you must understand the nature of video signals. The standard US video signal generates a picture, consisting of 525 horizontal lines interlaced to give two fields of 262.5 lines, and transmits approximately 60 fields (30 pictures) per second. Each horizontal line of the picture transmits a color-burst signal at 3.58 MHz.

Two signals, I and Q, carry the color information, which is centered around the color-burst frequency. This information is derived from the phase relationship of the I and Q signals with respect to the color-burst signal; therefore, it's important that your video-processing circuits maintain good phase linearity.

Two measurements affect phase linearity: differential gain and differential phase. Minimizing these two prevents unwanted interaction between the intensity and color of a signal. If a video circuit has a lot of differential-phase error, then a picture's color will change with its brightness.

As an example of how to measure differential-gain error, use a 3.58-MHz, 100-mV (200 mV p-p) signal superimposed on a 1-kHz, 500-mV p-p signal. This combined signal has a 700-mV p-p range, about the same as a video signal. If you send the signal through a highpass filter, ideally the only signal you should see is the 3.5-MHz signal, and it should be of constant amplitude. In reality, though, the amplitude varies, providing evidence of the circuit's differential-gain error. For instance, if the output amplitude varies between 99 and 100 mV, then the differential-gain error is 1%.

The variation in phase shift of the output signal with respect to the input signal, expressed in degrees, is the differential-phase error. By the time a video signal reaches a transmitter, the total differential-phase error should not exceed 3 degrees at 3.58 MHz.

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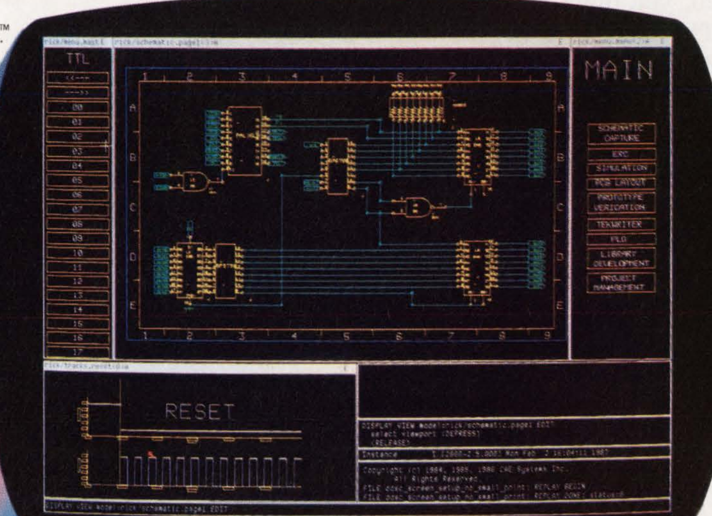

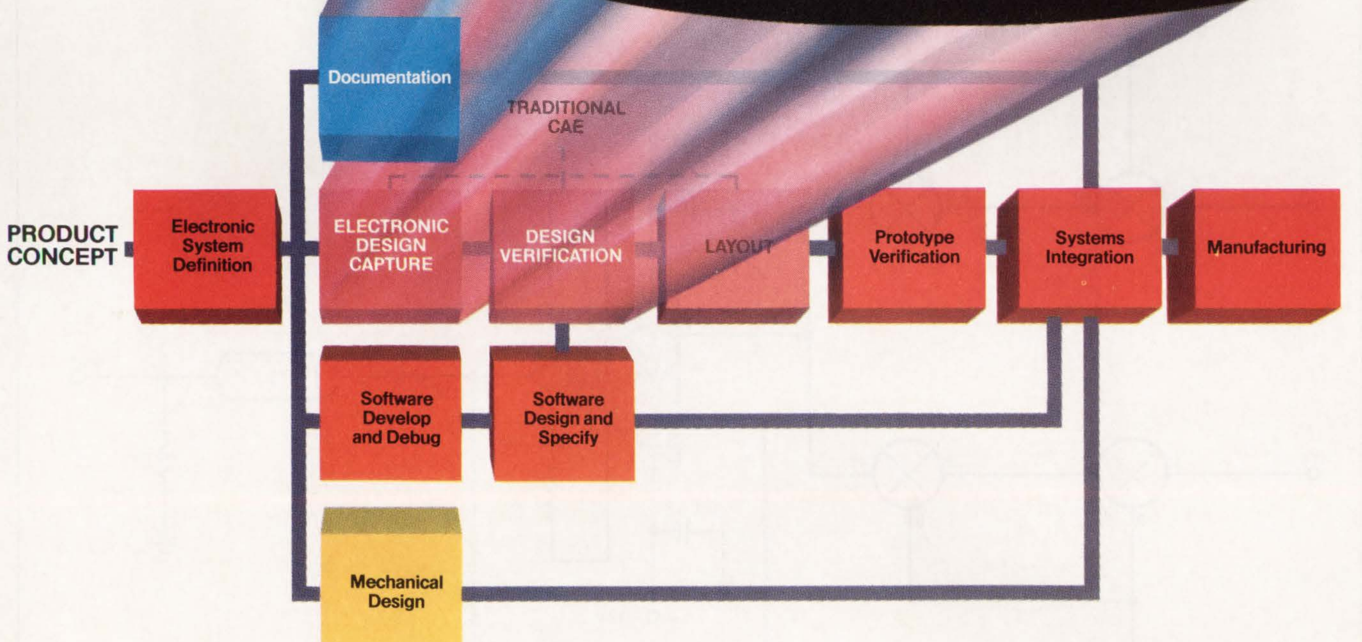

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Feedthrough attenuation should be about 60 dB at 4 MHz.

where both the op amp and multiplexer begin to roll off. The net result is a −3-dB response from the multiplexer input to the amplifier output of 7.3 MHz. Due to the peaking action of C_1, the −1-dB point is 5 MHz.

You can substitute another low-cost op amp, the LM318, in the circuits of **Fig 2** and 3 for simplicity's sake and enhanced performance. Because, at unity gain, the LM318's phase margin is less than that of the HA2520, you don't need to include the peaking capacitors. The resulting bandwidth is 20% less than the HA2520 circuit's.

You can also increase **Fig 3**'s bandwidth, as well as its drive capability, by adding an emitter-follower **(Fig 4)**. The circuit can drive four 75Ω doubly terminated cables, and it achieves a −3-dB bandwidth of 9.7 MHz. The resistor in the collector lead, R_1, limits the current flow through the transistor in the event of a short circuit. To reduce power consumption, you can operate the circuit from ±5V; however, the circuit's frequency response falls off about 15% at reduced power-supply voltages. If you do opt for ±5V operation, be sure to use the full ±5V to power the 4066 to minimize the part's on-resistance. You'll also need to change the

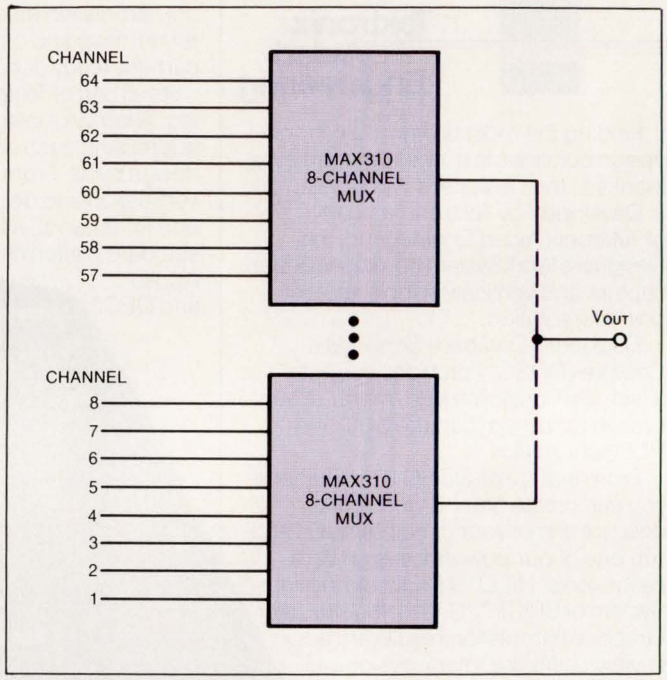


***Fig 6—This method of ganging multiplexers** degrades the bandwidth of your video circuitry.*

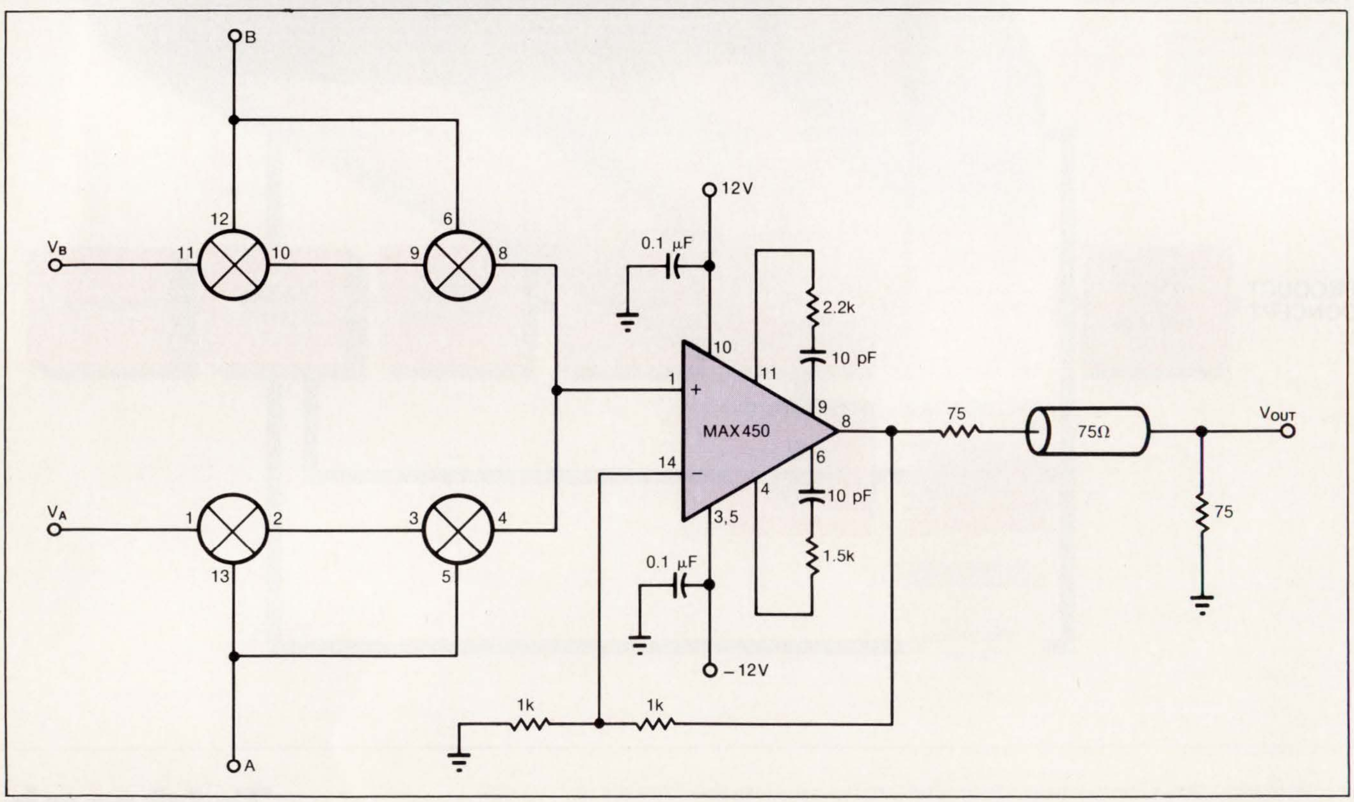


***Fig 5—A CMOS-input amplifier** such as the MAX450 presents a lighter load to your video switch.*

CIRCLE NO 165

You must be careful in your designs not to degrade the bandwidth of these parts.

protection resistor, R_1, to 20Ω.

The MAX450 op amp is yet another low-cost op amp suited to video switching applications. **Fig 5** shows a MAX450 connected to a 4066 video switch. This op amp has the disadvantage of operating with a relatively high quiescent current (25 mA), but because of its CMOS input, the input current is negligible compared to that of a bipolar op amp.

All the previous examples, which use 4066 switches to select one of two video signals, are fine for a limited number of input signals, but you shouldn't infer that you can switch more than two signals by just cascading a number of 4066s. As you increase the number of channels you want to switch, the bandwidth of the circuit decreases steadily. In addition, the number of devices necessary for multiplexing increases as you add decoder logic to control the switches. Using the 4066-switch approach to build an 8-channel multiplexer requires about six IC packages and a −3-dB circuit bandwidth in the 9- to 10-MHz range.

A better approach is to use one IC. The MAX310 8-channnel video multiplexer provides break-before-make switching and a −3-dB bandwidth of 15 to 20 MHz, depending on the bias conditions. You must be careful in your designs, though, not to degrade the part's bandwidth. **Fig 6** shows a circuit in which the MAX310 multiplexes 64 video channels onto one output line. Only one multiplexer is active at a time, and its output capacitance is 57 pF; that of the other multiplexers is 38 pF, and therefore the total output capacitance is 323 pF. The typical on-resistance of a channel is 150Ω. This 64-channel multiplexer's RC time constant is therefore 48 nsec. The corresponding −3-dB rolloff frequency is only 3.3 MHz, and you've wasted the part's bandwidth.

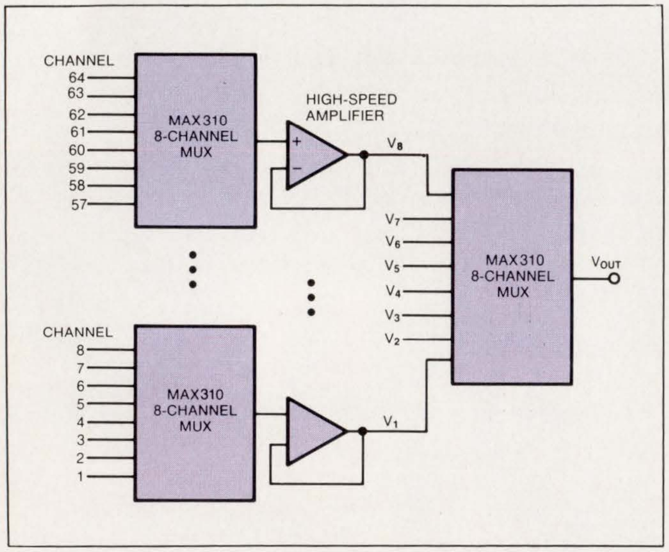


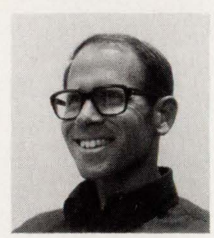
Fig 7—By adopting a 3-tiered approach *and adding high-speed amplifiers, you can significantly improve the frequency response of the multiplexing circuitry.*

You can double the bandwidth of the circuit to about 6.7 MHz by using the configuration of **Fig 7** (minus the amplifiers). In this circuit, the "on" channel path consists of two T switches connected in series. The path's resistance is 150Ω, and the capacitance is 60 pF (including pc-board traces). The RC time constant is therefore 9 nsec, and the corresponding −3-dB rolloff frequency for each switch is 18.6 MHz. The rolloff frequency of the combined switches is 6.7 MHz; adding one component doubles the circuit's bandwidth. Circuit path delays prevent you from obtaining any further bandwidth gains from this technique; using a 3-tiered technique won't confer any improvements in bandwidth.

To obtain a 12-MHz rolloff with this circuit, add the high-speed amplifiers as shown in **Fig 7.** Your amplifiers must exhibit negligible rolloff at that frequency, which in turn requires that the amplifiers have 50-MHz unity-gain frequencies. Unfortunately, amplifiers with 50-MHz unity-gain frequencies can be quite expensive, but you can substitute less-expensive high-speed buffers. These buffers are nothing more than emitter-followers with high bandwidths and gains close to 1. The BUF-03, for example, has a 50-MHz bandwidth, slews at 250V/μsec, and has an offset of only a few millivolts. The buffer's gain could prove troublesome, but if you substitute this part for the amplifiers in **Fig 7,** the gain is about 0.995, which causes very little loss in signal amplitude. **EDN**

Author's biography

Greg Schaffer is a senior member of the technical staff at Maxim Integrated Products in Sunnyvale, CA, where he is involved with analog IC design. Greg is a member of the IEEE and the ISA. He received his BSEE from MIT, his MSEE from UC Berkeley, and an MS in computer science from the University of Arizona. He has two patents to his credit and enjoys running, rock climbing, horse racing, and playing the piano.



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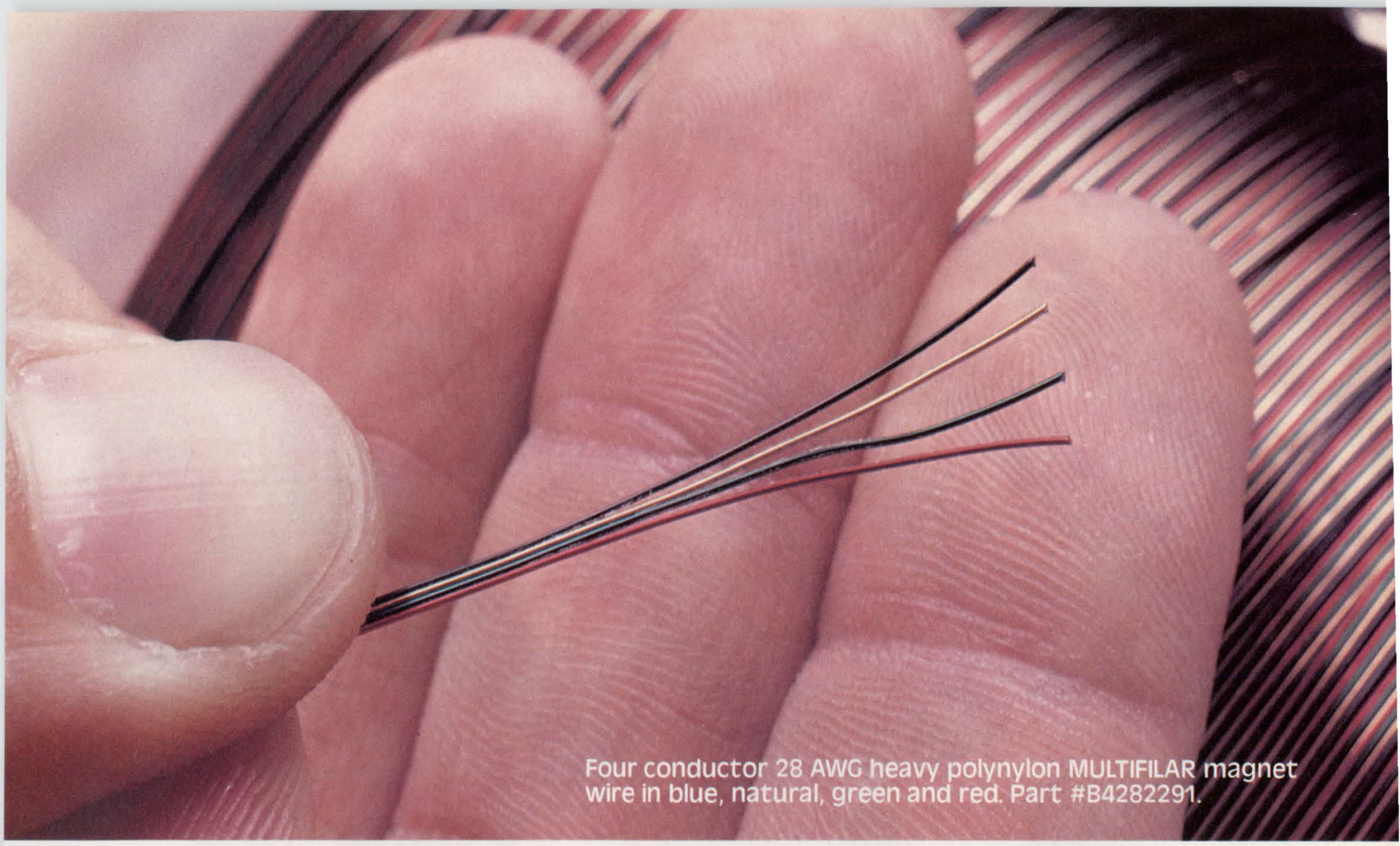

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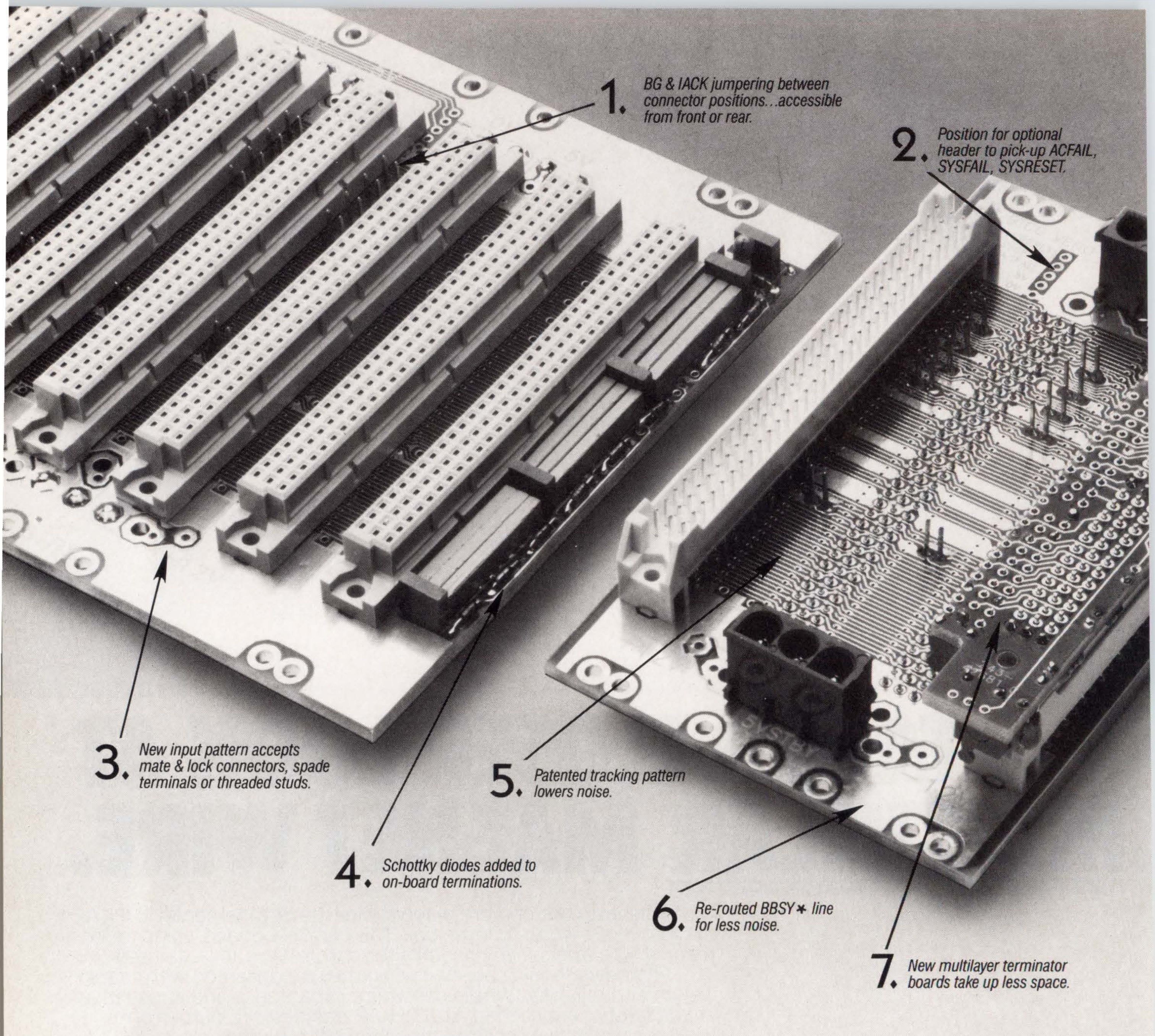
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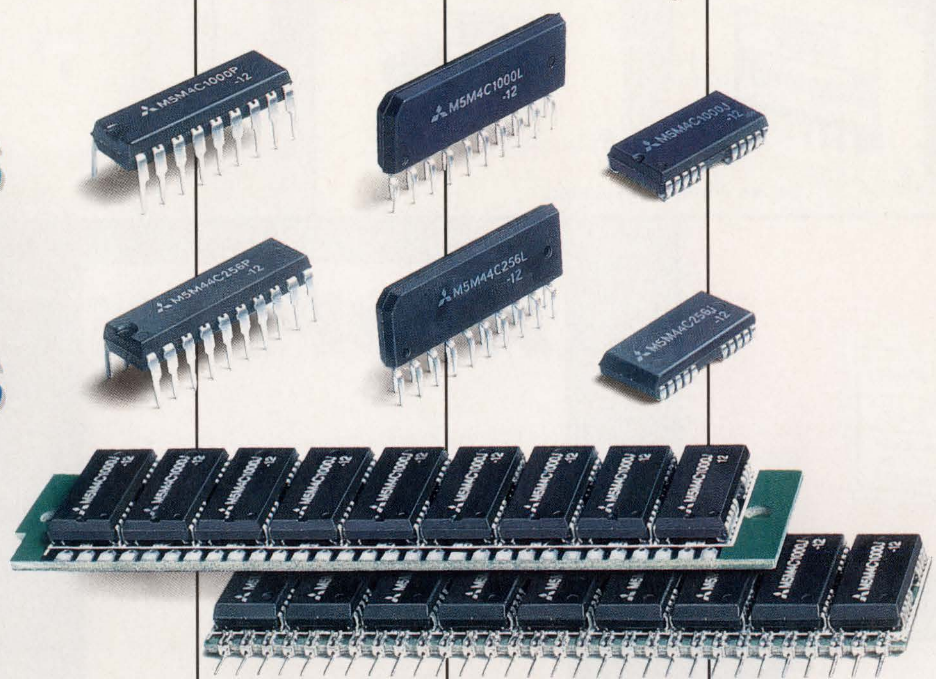

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M5M4C1000	1M × 1	Fast Page	•	•	•	100/25	120/30	150/40
M5M4C1001	1M × 1	Nibble	•	•	•	100/50	120/60	150/75
M5M4C1002	1M × 1	Static Column	•	•	•	100/25	120/30	150/40
M5M44C256	256K × 4	Fast Page	•	•	•	100/25	120/30	150/40
M5M44C258	256K × 4	Static Column	•	•	•	100/25	120/30	150/40
MH1M08	1M × 8	Fast Page	J (socketed), JA (pinned)			100/25	120/30	150/40
MH1M09	1M × 9	Fast Page	J (socketed), JA (pinned)			100/25	120/30	150/40

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SOJ (Small Outline J-Lead)	1.05* (2.1**)	1.1*	0.165
Module (1M × 9 Chips)	3.25/device	0.7/device	0.8

*Mounted only on one side of board.
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Proper testing can maximize performance in power MOSFETs

MOSFETs are a viable option when it comes to satisfying the needs of today's power electronics systems. Some problems do occur in certain applications, however, and you must address these problems by realistically testing the transistor to ensure successful system performance.

Kim Gauen and Warren Schultz, *Motorola Inc*

Most designers are quite satisfied with MOSFET performance, but others have experienced problems with applications involving multiple-transistor designs. In certain half- or full-bridge configurations, MOSFETs fail at apparently modest stress levels. The source of these failures is a set of three concurrent operating conditions, which collectively have become known as commutating dv/dt. A commutating safe-operating-area (CSOA) test circuit that follows a workable specification format can provide data that helps you counter the effects of these failure sources.

Several sources of problems

Before looking at the test spec and the test circuit, you should become familiar with the problem sources, of which there are a number. First, the MOSFET's diode must conduct during the switching cycle. Though it's a necessary condition of device failure, diode conduction cannot destroy the MOSFET by itself. Normally, the MOSFET is virtually immune to dv/dt-related failures, but it's much more sensitive when its intrinsic diode conducts current.

The change from majority to minority current carriers as the conduction mode changes is the problem source here. When the transistor operates as a MOSFET, it's not troubled by storage times or stored charge, because it's a majority-carrier device. On the other hand, its diode is a minority-carrier device. Consequently, it has forward- and reverse-recovery times because of charge storage. The stored charge associated with the diode is what degrades MOSFET performance. During reverse recovery, the rapid removal of stored charge increases the base-emitter voltage of the MOSFET's parasitic bipolar transistor, and this discharge increases the tendency for undesired turn-on.

This need to remove stored charge rapidly during reverse recovery is actually the second necessary condition for commutating stress failure. Fast charge removal increases current densities and peak electric fields. Because the turn-on speed of the transistor in the opposite leg of the half-bridge has the greatest effect on commutation speed, it has great influence on device stress.

There's a third failure condition: The stored charge must be extracted through a reapplied voltage of at least 30% to 50% of the device's maximum V_{DS} rating. If the bipolar transistor turns on, failures occur when operating conditions are outside the SOA. A bipolar transistor's BV_{CEO}, which is usually about 50% of its BV_{CES}, is one of the major factors that limit SOA.

Problems affect an exclusive club

These conditions exclude most circuits as candidates for commutating-dv/dt problems. All single-transistor designs are immune, and many multiple-transistor designs undergo no commutation stress, because the third failure condition is not fulfilled. The following examples can help you predict which multiple-transistor applications may develop problems. The first circuit described illustrates one of the most common problem areas. The second represents a design situation in which commutating dv/dt is not normally a concern.

Consider the bidirectional dc motor controller represented by **Fig 1.** Varying the duty cycle provides speed control, and the rotation direction depends on which transistor is controlling the motor speed. When one transistor is providing this control, the opposite transistor is inactive as a MOSFET, but its diode serves as a commutating rectifier. To reduce the audible noise, most designers operate their systems at frequencies greater than 20 kHz, so switching speeds are also high.

The turn-on of the drive transistor (Q_1 in this case) impresses commutating-dv/dt stress on Q_2's diode. As Q_1 turns on, the load current commutates from Q_2's diode to Q_1. More importantly, Q_1 also supplies the reverse-recovery charge for D_2. **Fig 2** shows Q_2's diode

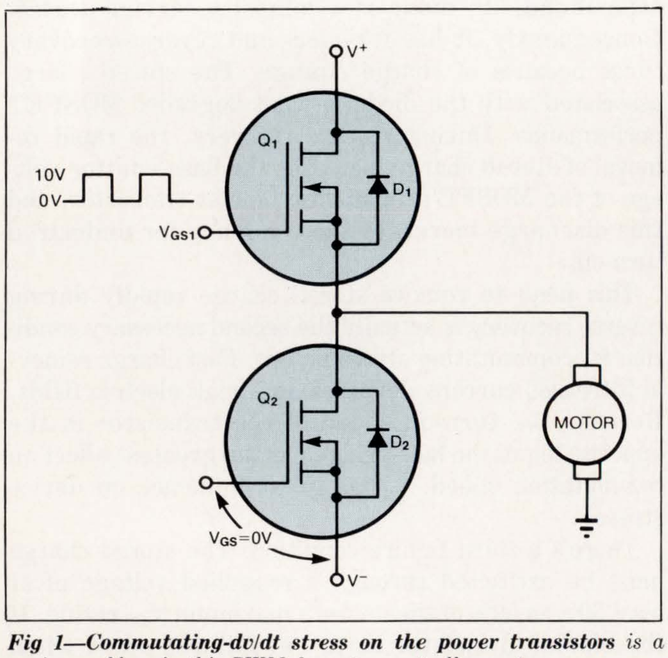

Fig 1—Commutating-dv/dt stress on the power transistors *is a major problem in this PWM dc motor-controller system.*

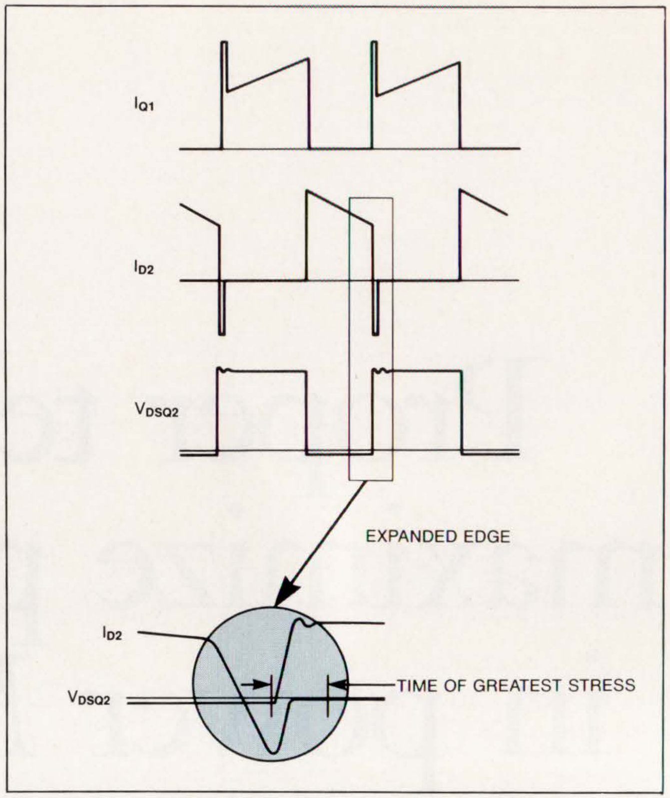

Fig 2—All three conditions for commutating-dv/dt failures *are evident in these motor-controller waveforms.* I_{D2} *shows the effect of the diode's conducting during the switching cycle,* I_{Q1} *reflects the need to remove stored charge rapidly during reverse recovery, and* V_{DSQ2} *shows the need to extract the stored charge through a high reapplied voltage.*

current, its drain-to-source voltage, and what many believe to be the most stressful time for failure. Note that the three elements required for commutating-dv/dt failure are present: As shown by the high dv/dt and high di/dt, Q_2's diode is experiencing the combined stress of reapplied high voltage, the presence of minority carriers, and the rapid extraction of charge.

The second example, a half-bridge switch-mode power supply **(Fig 3)**, usually has no problems with commutating-dv/dt stress. One crucial difference between this system and the motor-control circuit is that the transistors are switching alternately. Circuit analysis shows that, in the ideal case, output rectifiers D_1 and D_2 are the primary freewheeling rectifiers, and the MOSFET diodes are essentially inactive. In reality,

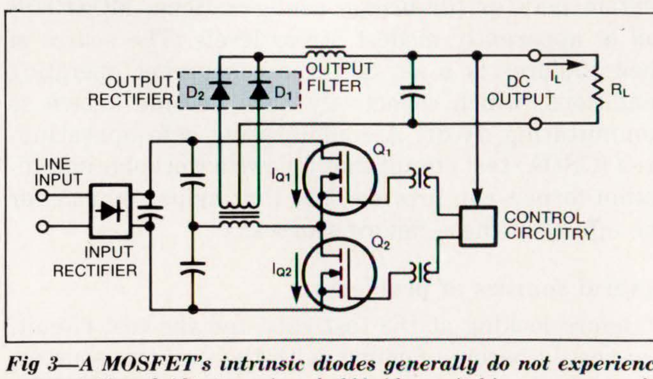

Fig 3—A MOSFET's intrinsic diodes generally do not experience commutating-dv/dt stress *in a half-bridge switching power supply, even though they act as freewheeling rectifiers.*

All single-transistor designs are immune to commutating-dv/dt stress problems.

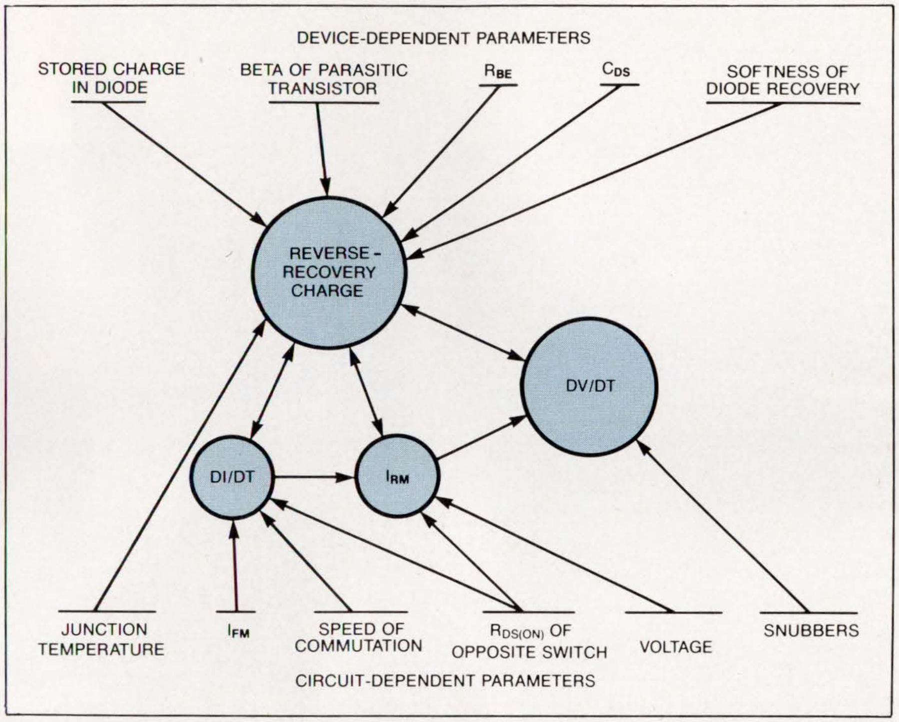

Fig 4—Many parameters affect *total device stress during commutating dv/dt, and it can be difficult to select the meaningful and convenient independent variables for CSOA testing. The CSOA spec begins with I_{FM}, the reapplied voltage, and the commutation speed.*

however, each intrinsic diode must clamp the energy in the transformer's leakage inductance when the opposite transistor turns off. Generally, this situation is acceptable, because the energies involved are small, diode conduction is brief, the reapplied voltage is only a fraction of the device rating, and reverse recovery is slowed by the parasitic inductance. Consequently, in these circumstances power-MOSFET commutating characteristics are usually not a problem.

You have cause for concern in half- or full-bridge circuits only if the load current does not pass through zero during each cycle. DC-to-ac inverters and the motor-control circuit are prime examples.

Establishing a CSOA spec format

To help eliminate problems associated with the MOSFET's intrinsic diode, MOSFET manufacturers can provide devices that are more immune to commutation stress, offer a test method that defines device capability, and publish ratings that detail the safe operating area for the commutating-dv/dt mode. This rating can come in the form of a commutating safe operating area.

Most manufacturers are striving to introduce devices with greater CSOA. Even when supplied with these devices, however, users will remain cautious (maybe unnecessarily) unless the new capability is defined and guaranteed. Lack of a universally accepted test method to standardize CSOA specs is now the major roadblock in this effort. This snag, though unfortunate, is understandable; it's simply very difficult to specify CSOA.

Fig 4 illustrates the relationships between the various parameters that influence CSOA. (Arrows represent a cause-effect relationship; for example, you work with the R_{BE} and C_{DS} factors to affect the reverse-recovery charge.) It's very difficult to select the most meaningful and convenient independent variables for testing. Selecting the three most critical circuit-dependent parameters seems to be the best approach. These parameters are the forward current in the diode just before commutation (I_{FM}), the reapplied voltage (or peak drain-to-source voltage when $V_{DS(PK)}>V_{DD}$), and commutation speed. To develop the format for a CSOA spec, you can start with these parameters and expand the format to include the effects of junction temperature, the effects of drive-transistor on-resistance, or the results of introducing snubbers to reduce dv/dt.

At least two methods proposed for specifying commutating dv/dt have become popular. Initially, design-

Text continued on pg 212

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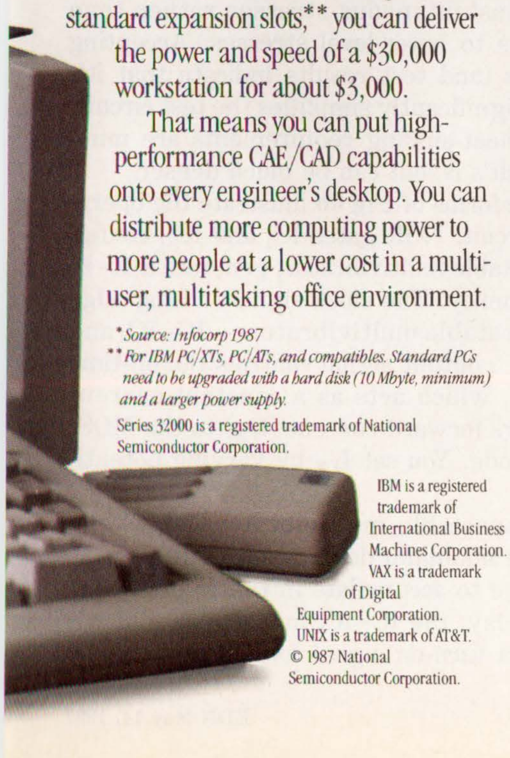
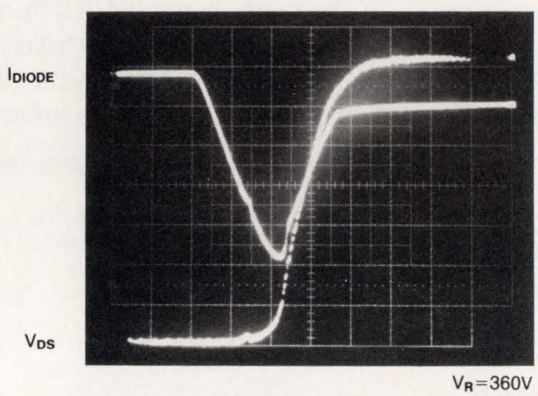


CIRCLE NO 149

There is cause for concern in half- or full-bridge circuits only if the load current doesn't pass through zero each cycle.

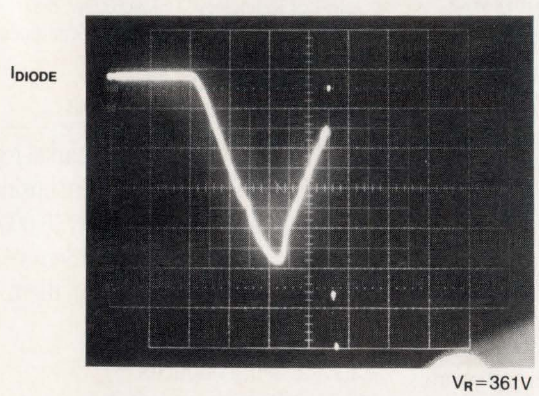
ers used a single dv/dt value, because it simplified matters, and they felt that failures were predominantly dv/dt-induced. This philosophy lost favor for several reasons. First, devices do not fail solely because of dv/dt. In fact, few failures occur during peak dv/dt; more are found later during periods of maximum voltage stress and reduced dv/dt **(Fig 5)**. Second, dv/dt varies considerably during reverse recovery, and it's very difficult (to say nothing of an oversimplification) to select a single representative value. Finally, dv/dt during commutation is a function of device characteristics and circuit conditions. You have little control over dv/dt unless you use snubbers.

Developing a curve of maximum di/dt vs peak dv/dt is the second specifying option. In this technique, you set di/dt by controlling the turn-on speed of a drive transistor and use snubbers to vary dv/dt. Unfortunately, this method has some drawbacks too. For one thing, the specification does not consider the two most critical parameters—forward diode current and reapplied voltage. Second, it's not wise to rely on snubbers in characterizing devices; it's far better to omit them from the design, and the newest MOSFETs have ample CSOA without them. What's more, the addition of snubbers only makes the task of characterizing the device more difficult, because they add another variable. Finally, some intrinsic diodes are much faster than others; they return the diode current from the reverse-recovery peak to zero very abruptly, and the rise in V_{DS} to V_R is very fast. These diodes must be able to withstand the dv/dt values that they inherently create.



(a)

TRACE	VERTICAL	HORIZONTAL
I_{DIODE}	4A/DIV	100 nSEC/DIV
V_{DS}	50V/DIV	100 nSEC/DIV



(b)

TRACE	VERTICAL	HORIZONTAL
I_{DIODE}	4A/DIV	100 nSEC/DIV

Fig 5—Instead of failing during peak dv/dt (a), *the 4A/450V device that was tested to generate these waveforms failed when the reapplied voltage was increased from 360 to 361V* ***(b).***

Dissecting the CSOA test fixture

The features of the CSOA test fixture discussed here **(Fig 6a)** reflect the format described earlier. Most important, the fixture and the test procedure truly characterize the device under test (DUT) by minimizing the effects of circuit parasitics. The fixture's design decreases stray inductances in critical portions of the circuit to practical minimums—an approach that provides the only means of correlating test results with those of other test circuits.

The circuit's design assumes that test results are independent of the duty cycle, and that failures occur because of peak instantaneous stresses rather than multiple exposures to lower-level stresses. Accepting these assumptions (and test results indicate that it's rational to do so) significantly simplifies the test circuit. And if the DUT heat-sinking requirements are minimal, the test circuit's layout can be much denser.

The timing waveforms of **Fig 6b** illustrate the operation of the test circuit. NOR gates IC_1 and IC_2, configured to form an astable multivibrator, generate a 10- to 100-Hz clock frequency. The clock signal's rising edge triggers two monostable multivibrators—IC_3-IC_4 and IC_5-IC_6. The IC_3-IC_4 output signal controls the on-time of the MJE13009, which acts as a constant-current source that delivers forward current (I_{FM}) to the MOSFET's intrinsic diode. You set I_{FM} by varying potentiometer R_1.

The IC_5-IC_6 monostable multivibrator delays the turn-on of Q_2. The minimum delay is set at 10 μsec to allow stored charge to accumulate in the diode's junction. After this delay, the IC_7-IC_8 monostable multivibrator generates a turn-on signal for Q_2 for 10 to 50

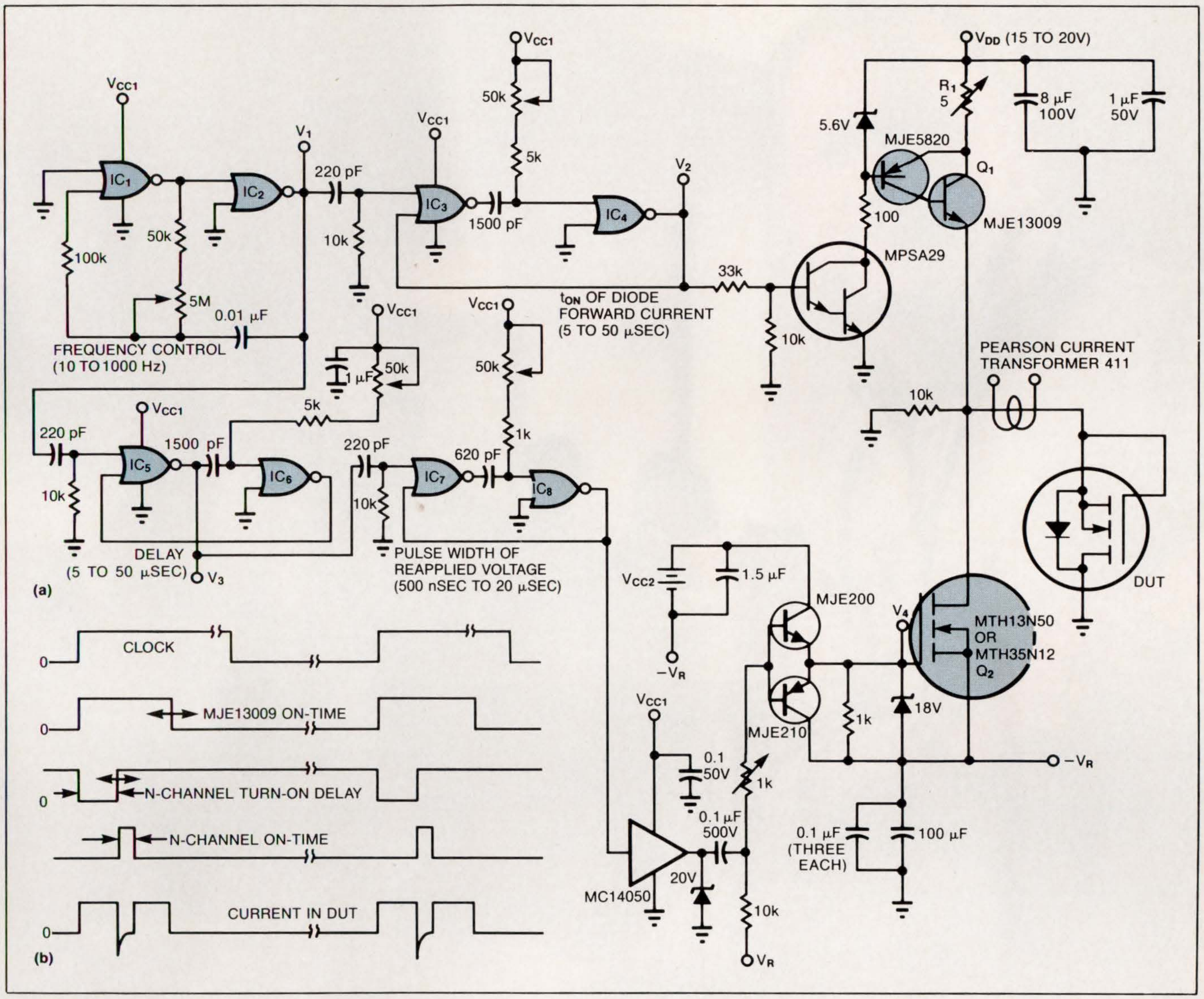


Fig 6—To determine the characteristics *of just the transistor under test, this CSOA test circuit's design and layout minimize the effects of circuit parasitics.*

µsec. For the duration of the turn-on pulse, Q_2 applies a reverse voltage to the DUT's drain-source diode and forcefully extracts the reverse-recovery charge. During the reverse-recovery interval, the circuit accurately simulates the same conditions that appear in the dc motor controller discussed previously.

A few additional circuit characteristics enhance device testing. First, the drain of the DUT attaches directly to the system ground plane. This direct connection greatly simplifies V_{DS} monitoring and improves measurement accuracy; there's no need to use differential measurement techniques or float an oscilloscope with this layout. This layout also allows you to use a probe-tip adapter rather than a conventional ground clip; the adapter provides an excellent ground connection for the scope. These precautions are necessary because the V_{DS} measurement is the most influential, and its rate of change can be greater than 10V/nsec.

The ability to withstand DUT failure is another, mundane, but necessary, feature of the test circuit. The $R_{DS(ON)}$ of driver-transistor Q_2, and Q_2's cutoff current level at the applied gate-to-source voltage, are the primary factors limiting the current surges that can appear at failure. In either case, the MOSFET's rug-

Text continued on pg 216

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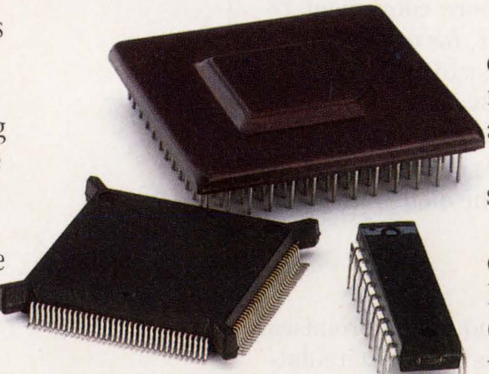

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gedness with respect to current surges and the test's low duty cycle provide Q_2 with the safety margin it needs to survive.

Other, simpler test circuits are more convenient to use in some aspects. In **Fig 7**'s circuit, for example, the test cycle begins when the drive transistor turns on and current ramps up in the coil. The drive transistor then turns off, and current commutates into the diode of the DUT. Before the diode current decays to zero, the drive transistor turns on again and forces the diode into rapid reverse recovery.

You trade simplicity for flexibility

The very simplicity of this technique compromises test flexibility. The biggest problem is that the circulating current, or forward current in the diode, is a function of the supply voltage, so it's difficult to change these two parameters independently of one another. Also, none of the elements in this circuit are subject to great amounts of loss; even low supply voltages and minimum driver duty cycles can pump the current in the coil to undesirably high levels. This factor complicates testing at high voltage levels. When the drive transistor operates at low duty cycles, the diode conducts most of the time, causing the MOSFET to heat up. The need to incorporate heat sinks results in an increase of the circuit's size.

As an option, you could feed a burst of pulses to the driver. This scheme reduces DUT heating problems and allows you to test at high supply-voltage levels. You'll also increase the complexity of the test circuit, however, and I_{FM} still depends to a great degree on the supply-voltage level. You'll also have to monitor the high-speed reverse-recovery interval at the end of the pulse train—an inconvenient thing to do.

Using the CSOA specification

The format of the CSOA rating makes it easy to use. Designers must only maintain V_{DS} and I_{FM} within specified limits. Also, t_{FRR} (or current fall time during reverse recovery) is specified as a minimum allowable value. Pushing devices to their limit in a half-bridge PWM dc motor controller produces failures that match those seen in the CSOA tester. Therefore, the test method and test circuit do indeed simulate stresses found in real-world applications. You must remember, however, the ways in which important test circuit parameters can skew the comparison.

The CSOA tester imparts maximum device stress for

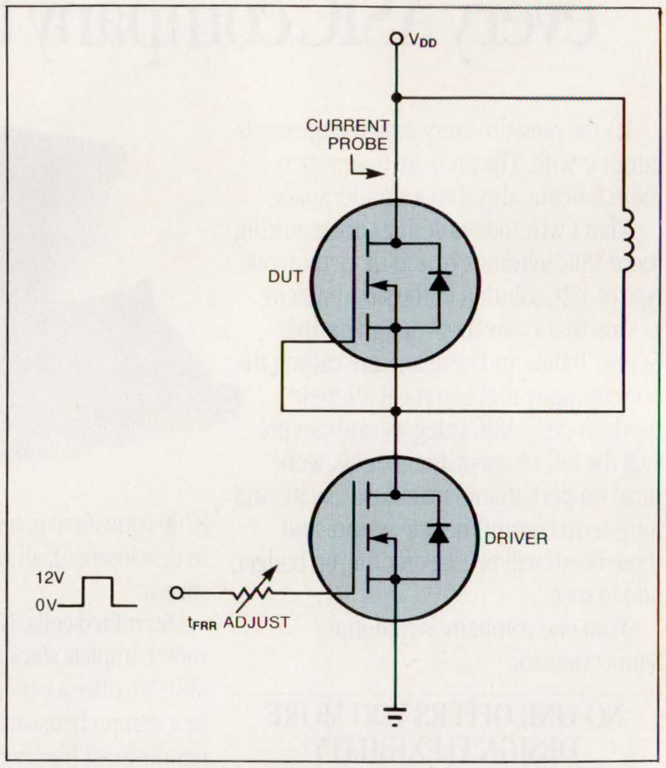


*Fig 7—**Although it's simpler** and more convenient than **Fig 6**'s circuit in some aspects, this CSOA test circuit lacks flexibility. The biggest problem is that circulating current is a function of supply voltage, so it's difficult to change these parameters independently of one another.*

a given I_{FM}, V_R, and t_{FRR}. Doing so typically yields a worst-case assessment of device capability and provides you with some guard bands. Test-circuit features include a reapplied voltage input with sufficient bypass capacitance to maximize dv/dt and voltage stress; a drive transistor (Q_2 in **Fig 6**) with a low $R_{DS(ON)}$ for high I_{RM}; and a complementary emitter-follower gate drive for Q_2 to reduce dv/dt effects on the driver when the diode under test turns off.

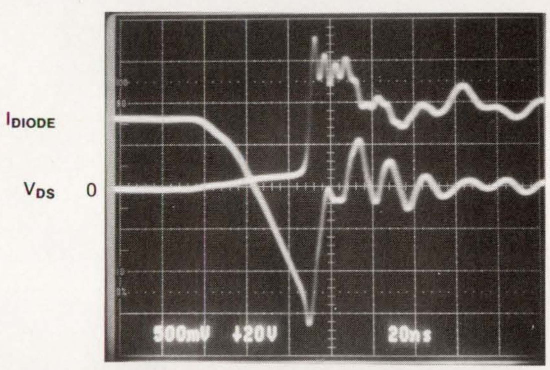
You should also be aware of three additional test-circuit parameters that can degrade CSOA. Unfortunately, the design engineer, rather than the manufacturer, specifies these parameters, so it's difficult to include them in a CSOA specification.

The first parameter is the gate-to-source resistance (R_{GS}) of the DUT. If R_{GS} or the gate-to-source inductance (L_{GS}) is high during reverse recovery, the intrinsic diode generates a large dv/dt that can cause V_{GS} to exceed its threshold value. Although the large dv/dt doesn't fully turn the MOSFET on, it does force the

You must decrease stray inductances in critical portions of your test circuit if you hope to correlate results with those from other test schemes.

device into the active region and slows the reverse-recovery process **(Fig 8)**. This operating mode increases commutation power losses and clearly involves dv/dt turn-on. Decreasing the gate-to-source impedance (Z_{GS}) is normally the best way to solve this problem. However, increasing Z_{GS} to slow reverse recovery can reduce V_{DS} peaks and may even prevent the MOSFET from avalanching.

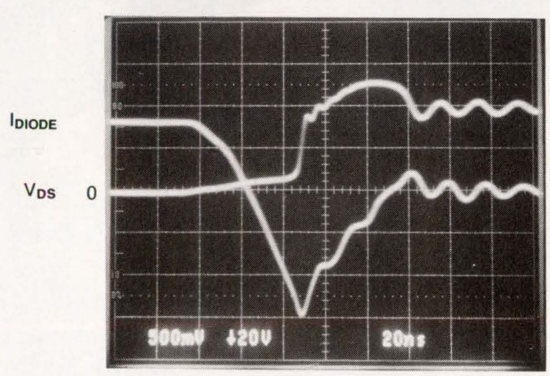
The test circuit's junction temperature is the second parameter that can degrade CSOA. Even so, although you might intuitively suspect that T_J has a major effect on CSOA, test results taken to date indicate that it does not. These results make sense when you recall that the reversed-biased safe operating area (RBSOA) of bipolar transistors is also relatively independent of T_J. The fact that commutating-dv/dt waveforms are fairly constant as T_J changes also indicates that T_J has a minor effect. Varying other, more dominant parameters often causes waveform changes that signal impending dv/dt DUT failure.



R_{GS}=10

(a)

TRACE	VERTICAL
I_{DIODE}	5A/DIV
V_{DS}	20V/DIV



R_{GS}=100

(b)

TRACE	VERTICAL
I_{DIODE}	5A/DIV
V_{DS}	20V/DIV

Fig 8—Increasing R_{GS} *slows the reverse-recovery process and increases commutation power losses. However, the higher impedance reduces peak instantaneous stress and may also keep the device from avalanching.*

The parasitic inductance between the positive and negative rails of the half-bridge in the test circuit is the final parameter under strict control of the design engineer. The test circuit does not clamp this inductance, and as a consequence the DUT may avalanche briefly at very high commutation speeds. As the following discussion on the effects of avalanching illustrates, it's most important to minimize this inductance in all cases.

The UIS test is not a viable alternative

Today, there are some designers who feel that a UIS (unclamped inductive switching) test is an adequate substitute for a CSOA test. This group argues that the common cause of device failure in the two testing modes occurs when a high base-emitter shorting resistance (R_{BE}) activates the parasitic bipolar transistor. Though this reasoning applies to most devices, it's flawed in two ways.

First, some devices may pass a UIS test and then fail in the commutating-dv/dt mode because of device deficiencies other than high R_{BE}. When you consider the MOSFET's voltage-termination rings, gate feeds, bonding pads, and cell interconnections, it's obvious that the device consists of much more than a few thousand paralleled cells. In some devices, these secondary features can clearly limit performance in one test and not in the other.

Second, a flaw in the current UIS test method makes it difficult to correlate UIS and CSOA test results. A study of UIS waveforms **(Fig 9)** clarifies this point. As the data shows, a device may react to overvoltage stress in at least three ways.

Three reactions to overvoltage stress

Some devices fail immediately in avalanche, and V_{DS} collapses to approximately 0V. Other MOSFETs can maintain their BV_{DSS} during the entire transient period if the current and pulse durations are not too great. Finally, the drain-to-source voltage of some devices may collapse to a lower level. This lower voltage indicates that the MOSFET's parasitic bipolar transistor

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Pushing devices to their limit in a half-bridge motor controller produces failures that track those seen in the CSOA tester.

has been activated. Consequently, the magnitude of V_{DS} during avalanche equals the transistor's BV_{CER}.

If you increase the UIS test's supply voltage above BV_{CER}, you have no mechanism to limit the avalanche current, and the DUT normally fails. The magnitude of the supply voltage can therefore have a great effect on a device's energy-handling capability. It's relatively easy to improve the present UIS test method so that it can detect devices that exhibit this BV_{CER} "snapback." Instead of checking only for device failure, you can sample the V_{DS} waveform in avalanche to ensure that it stays above the transistor's maximum V_{DS} rating.

As switching speeds increase in the commutating-dv/dt mode, CSOA operating conditions begin to mimic those of UIS testing. During the final phase of reverse recovery, the diode current is dropping toward zero from its negative peak. You can think of this current as decreasing drain current. If the diode recovers abruptly, the associated di/dt can be extremely large—perhaps greater than 1000A/μsec. Parasitic inductances oppose these rates of change in current, and the polarity of the induced voltages causes them to add to the reapplied voltage and increase the voltage stress on the DUT.

Fig 10, which illustrates the reverse-recovery behavior of a 10A/50V MOSFET device, clearly shows the effect of the unit's BV_{CER}. Clipping of the V_{DS} waveform at the device's BV_{CER} (which corresponds to the value observed in UIS testing) and the coincident drain current show that the device is in avalanche. Though the device passes this test, reliability in this operating mode is uncertain because the parasitic bipolar transistor is obviously being activated. If V_R should exceed BV_{CER}, device failure is likely. Because the device has a tendency to snap back to a BV_{CER}, it could fail in the commutating-dv/dt mode even though it survives a UIS test.

Reliability in the commutating-dv/dt mode

In determining and optimizing reliability in the commutating-dv/dt mode, designers face a situation that's similar to the one they face when working with the RBSOA of bipolar transistors. Standard reliability life and power-cycling tests aren't too helpful because the stresses they impose don't reflect the stresses seen during dynamic operating conditions. In addition, the curves in these tests describe operation in a typical

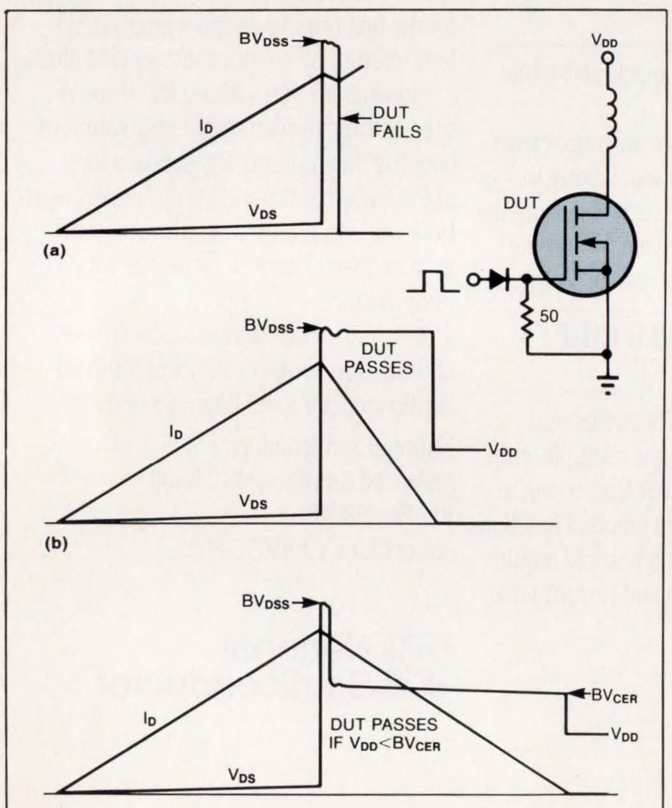
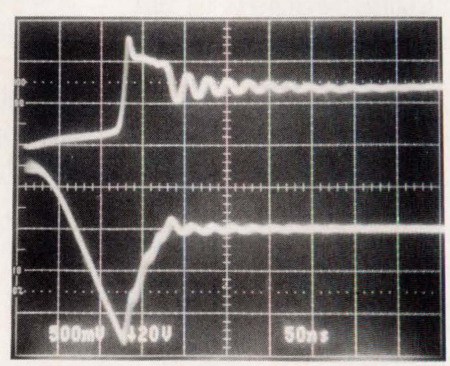


Fig 9—Because of defects in the present UIS test method, a device may fail in one of three ways. Some devices fail immediately in avalanche (a), while others can maintain their BV_{DSS} during the entire transient period (b). In the third case (c), the drain-to-source voltage of some devices may collapse to a lower level.



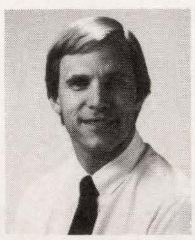
TRACE	VERTICAL
V_{DS}	20V/DIV
I_{DIODE}	5A/DIV

Fig 10—Commutation at very high speeds can cause avalanching in the device under test—an unreliable mode of operation.

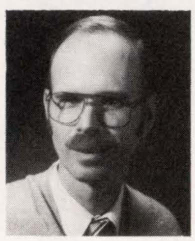
application, and they lose some of their meaning when the actual operating conditions are different.

There are a number of ways to guarantee reliability. First, make sure that the peak V_{DS} remains within its maximum rating, and that I_{FM} and I_{RM} do not exceed the intrinsic diode's pulsed current rating. Second, you can use the CSOA data to look for signs of bipolar turn-on. This should rarely be a limitation, because the CSOA is normally derated from conditions that cause any bipolar activation. Nevertheless, a small load change that causes an abrupt change in the reverse-recovery waveform is one of the signs of bipolar turn-on. Another sign is that, as circuit conditions change **(Fig 10)**, the drain-to-source voltage does not change in magnitude after reaching its plateau. **EDN**

Authors' biographies



Kim Gauen is a senior applications engineer for the semiconductor products sector of Motorola Inc (Phoenix, AZ), where he's responsible for developing applications for power products. He's been with the company for five years and holds a BS in elementary education from Southern Illinois University and a BSEE from the University of Missouri. In his spare time, Kim enjoys bicycling and reading.



Warren Schultz is principal engineer for the low-frequency power-transistor and thyristor group at Motorola. Previously employed by GE Aerospace, he's been with Motorola for 14 years. Warren holds a BSEE from Lehigh University and an MBA from Arizona State University. He's been granted one patent, and three more are pending, for his work with Motorola's Smartpower technology.

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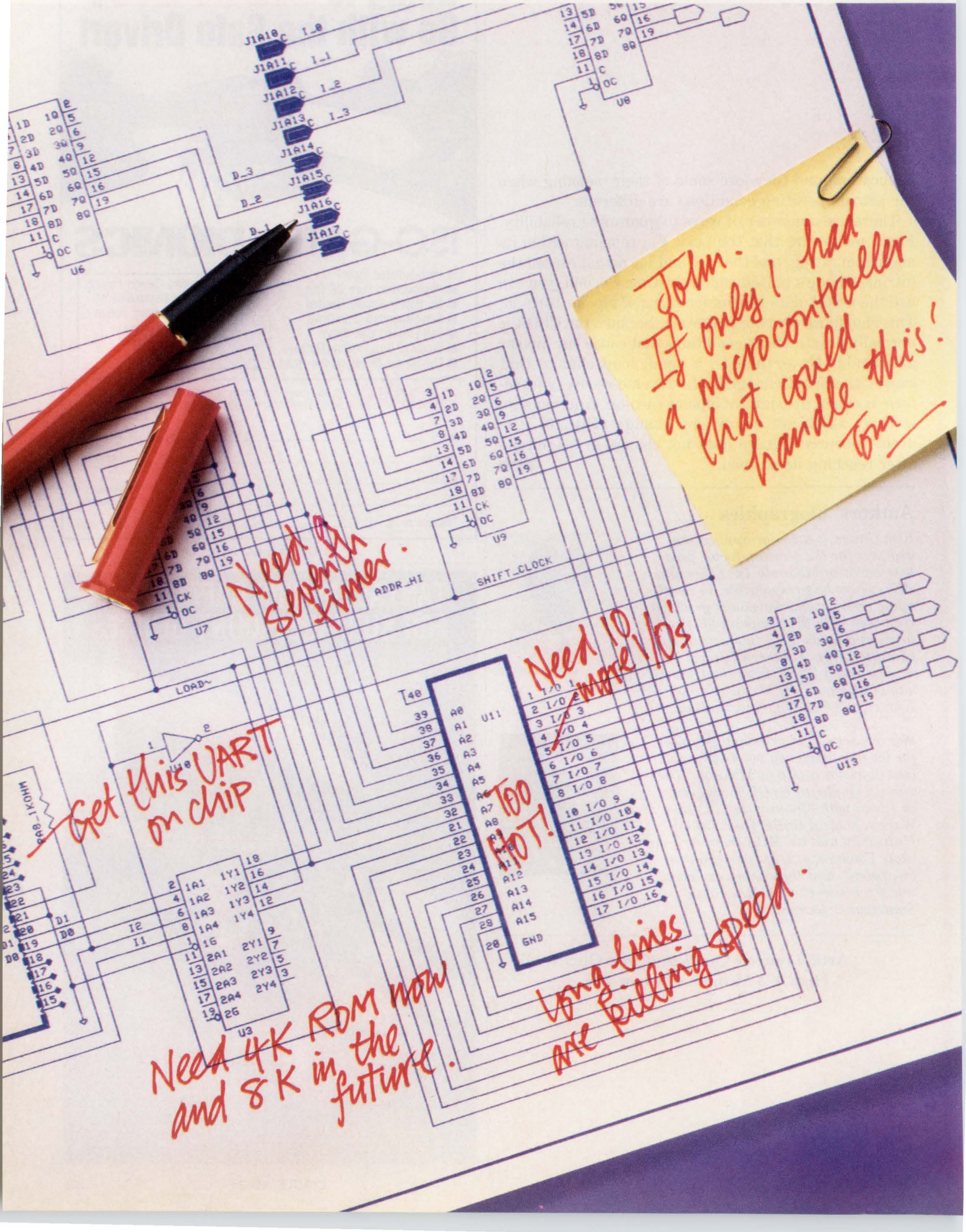

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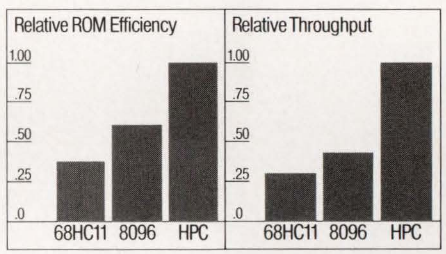

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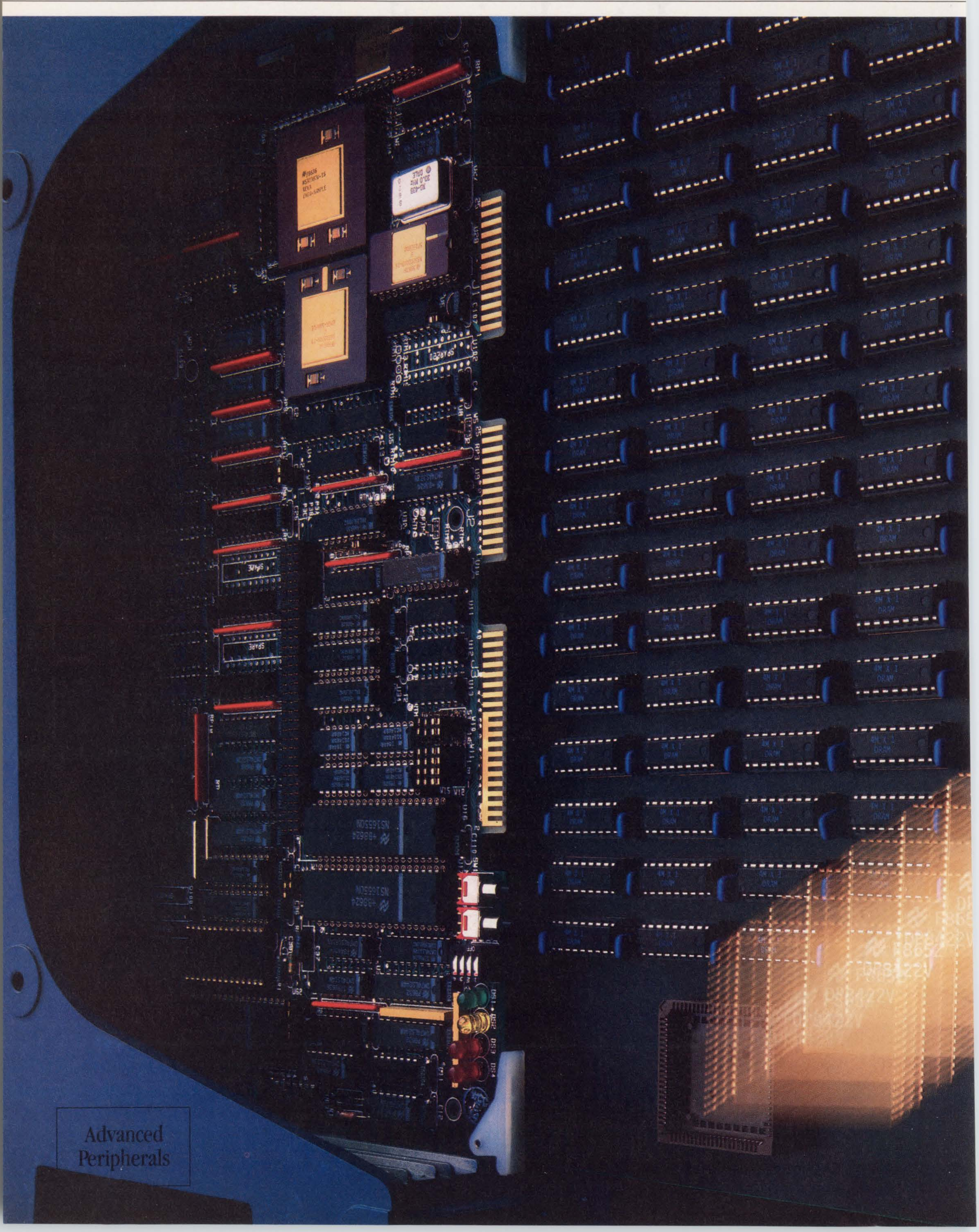

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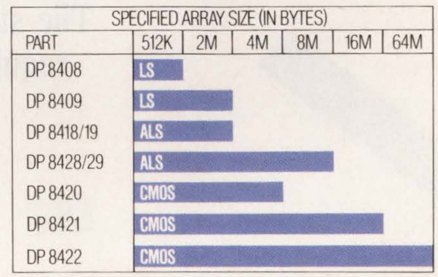

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Check advanced features and noise specs when selecting codecs

A codec—or coder/decoder—performs the analog-to-digital (encoding) and the digital-to-analog (decoding) conversion of the human voice. Part 1 of this 2-part series provided an overview of a codec's structure and function and described codecs' standard features. This article covers advanced codec features such as software control of operating modes, and it discusses noise considerations.

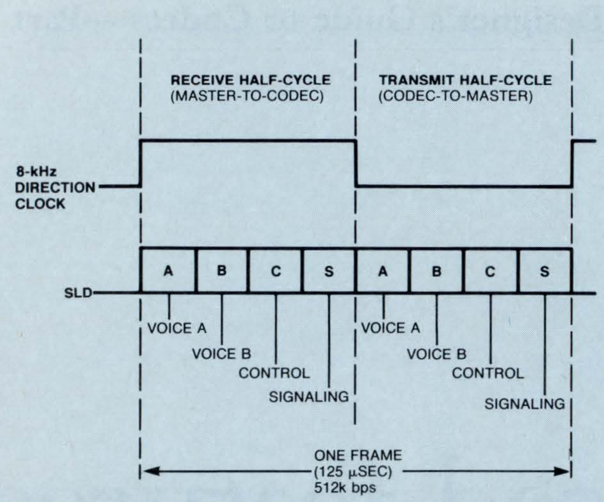
Brady Barnes, *Inter-Tel*

Almost any codec/filter combo chip that you find today offers standard features such as low power consumption and a minimal requirement for off-chip support circuitry, and many codecs offer features such as A/B signaling (see EDN, April 30, pg 211). But now, manufacturers are beginning to produce codec/filter combos that offer extra features that a microprocessor can access by using customized software (which you write). A microprocessor communicates serially with such a codec and programs the codec with appropriate control codes and data. The versatility and power made available by these codecs can lead to some very reliable and practical designs.

With some exceptions, such advanced codecs offer the following features:

Digital signal processing: Codecs that employ digital techniques (rather than analog ones) to process a voice signal offer several advantages, including highly predictable performance, better tolerance to temperature and process variations, a higher power-supply rejection ratio, less crosstalk, and better testability. Furthermore, DSP allows users to employ microprocessor commands to customize the analog characteristics of a codec to their specific circuit and application. Advanced Micro Devices' single-sourced Am7901 SLAC (Subscriber Line Audio-processing Circuit) and Siemens's PEB2060 (an SLD-compatible codec for which Philips is the alternate source) are examples of codecs that offer DSP capabilities.

SLD interface: The Subscriber Line Datalink (SLD) interface is a 3-wire digital interface that connects the codec to a master device. The master device oversees the switching of PCM voice data of eight to 16 codecs. The SLD interface combines the transmit and receive wires into one wire, thereby reducing the interconnect complexity between the codec and other devices. Furthermore, the SLD interface also allows for the exchange of control and signaling data between the codec and the microprocessor (**Fig 1.**) Intel's 29C48, 29C50,



NOTES:

1. VOICE DATA IS TYPICALLY TRANSMITTED ON JUST THE "VOICE A" CHANNEL. HOWEVER, IF TWO SLD-COMPATIBLE CODECS ARE RUNNING OFF THE SAME SLD DATA LINE, THEN BOTH VOICE CHANNELS ARE USED TO TRANSMIT VOICE DATA.
2. THE CONTROL CHANNEL (CHANNEL C) IS USED TO SEND CONTROL BYTES FROM THE MASTER DEVICE TO THE CODEC TO PROGRAM THE CODEC. THE ACTUAL CONTROL DATA COMES FROM A MICROPROCESSOR RUNNING UNDER CUSTOMIZED SOFTWARE THAT IS WRITTEN TO TAKE ADVANTAGE OF THE CODEC'S ADVANCED FEATURES. THE MICROPROCESSOR SENDS THE DATA TO THE MASTER DEVICE (SUCH AS A LINE-CARD CONTROLLER LIKE THE INTEL 2952), AND THE MASTER DEVICE SENDS THE CONTROL DATA TO THE CODEC.
3. THE SIGNALING DATA CHANNEL IS USED ONLY IF THE CODEC SUPPORTS SIGNALING.
4. ALL FOUR CHANNELS ARE OF EQUAL BANDWIDTH (EIGHT BITS OF DATA IN EACH DIRECTION EVERY 125 μSEC).

***Fig 1—The SLD interface provides** four channels to each codec: two channels for voice, one for control information to the codec, and one for signaling information.*

and 29C51 codecs (Matra-Harris is the alternate source for the 29C48) and Siemens's PEB2060 support the SLD.

Loopback test modes: Another advanced feature of codecs is loopback testing. The three basic types of loopback testing are analog, subscriber, and digital.

In the analog loopback mode, the analog output is tied (internally) to the analog input. This mode allows functional testing of the codec as well as gain adjustment.

The subscriber loopback mode is useful for analog-to-analog testing from the subscriber side of the codec. In this mode, the PCM output of the encoder is fed back around to the PCM input of the decoder. In this manner, the analog input is actually sent through the transmit filter and encoder and then back through the receive section's decoder and filter.

In the third mode, the digital loopback mode, the combo retransmits the PCM word it receives on the digital input back out on the PCM output. This loopback test is useful for evaluating the integrity of the path to the codec. A word of caution: Different manufacturers apply slightly different meanings to these loopback modes. Be sure you consult the data sheet regarding a specific codec's loopback mode or modes before assuming you understand the exact meaning of what's advertised.

Programmable gain, impedance matching, and trans-hybrid balancing: Some codecs allow for a programmable gain change of 12 dB in the transmit path and 15.5 dB in the receive path, and some employ programmable filters to implement the programmable impedance matching and trans-hybrid balancing. Others provide an alternate method of programmable balancing: These codecs allow you to connect external balance networks to three control pins. Then, under software control, such a codec can select one (or any combination) of these three networks.

Programmable filters: The AMD Am7901 and Siemens PEB2060 allow user programming of several different digital filters, thereby allowing you to customize the frequency response of the codec to correct for peculiarities in the analog circuitry that interfaces to the codec.

Secondary analog input: One SLD-compatible codec has an unfiltered secondary analog input. The secondary analog channel, which may be used for voice or for any 4-kHz, band-limited signal, is made possible only because of the SLD interface, which allows for two voice channels (an A and a B channel, not to be confused with A/B signaling).

Three-party conferencing: This feature, available only on SLD-compatible codecs, basically involves adding the voice data on the A and the B channels to effect a form of conferencing. This feature might have only limited usefulness now; nevertheless, when ISDN is in common use, the feature could be used for 3-party conferencing on 2-line phones. Even now, you might encounter applications for which the feature may prove beneficial. For example, it might be possible to use this feature to mix two single tones together to produce a DTMF tone.

A/B channel assignment: The SLD interface provides four channels to each codec: one for control information to the codec, one for signaling information, and two channels—labeled A and B—for voice. In most cases, the codec uses only the A channel for voice data; the B channel goes unused. However, because an SLD-compatible codec can be programmed via a pin to transmit and receive voice data on a particular channel, two codecs can share one SLD line: One codec operates on the A channel and the other codec operates on the B channel. The control data always has an address (A or B) associated with it, so even when two codecs share one SLD line, you can be assured that control data goes

Some codecs use digital techniques, rather than analog ones, to process a voice signal.

to the right codec. The A/B channel-assignment feature allows twice as many codecs (16 instead of eight) to interface with a single line-card controller (such as the Intel 2952).

Programmable SLIC chip select: Most applications involving codecs will have their analog side interfaced to a SLIC (subscriber-line interface circuit). In order to facilitate interfacing the codec to a SLIC, especially when two codecs share the same SLD line, codecs include a programmable SLIC chip-select input.

Signaling: Finally, a very important feature of advanced codecs is their signaling capability. Rather than sending signaling data by using A/B signaling (that is, 8th-bit signaling), these codecs provide several I/O pins to perform functions such as hookflashing, ringing, and pulse dialing, or to monitor for such conditions as hookflashing, ringing, and loss of loop current.

In the case of the SLD-compatible codecs, signaling information is passed back and forth between the codec and the microprocessor via the signaling channel (**Fig 1**). (As with all other channels, this channel is limited to 8-bit words.) This added capability can save you from having to add buffers and registers to your design.

Besides these advanced features, advanced codecs also have programmable power-down/standby modes as well as programmable μ-law or A-law encoding (except for the Am7901). Obviously, these advanced features aren't free. You can expect to pay anywhere from $6 to $12 per codec (in 10k quantities) for these devices. If you don't need or don't desire these extras in your design, you can probably select a no-frills codec somewhere in the $4 to $6 range.

A checklist of performance characteristics

Probably the most important specifications that describe a particular codec are its transmission, or performance, characteristics:

- Gain and dynamic range
- Frequency response
- Gain tracking
- Output drive capability
- Distortion
- Noise
- Crosstalk
- Power-supply rejection
- Power dissipation.

Because just about every codec's data sheet states that the codec meets CCITT and AT&T specs, you can expect the performance characteristics of all codecs to meet at least a base-line level. Make sure that the data sheet states that the codec meets all of the applicable CCITT and AT&T requirements, not just some of the specs.

Note, however, that meeting these specs may not be adequate. A case in point is that of idle-channel noise. EIA's RS-464 spec requires an idle-channel noise spec of no more than 16 dBrnC, port-to-port. This spec is more stringent than that required by CCITT and AT&T.

As you begin to compare manufacturers' data sheets for different codecs, you'll find that the one thing they all have in common is a lack of standardization in the way they present specs. Some manufacturers indicate only typical values, some indicate only minimum or maximum values, and others provide both. Moreover, the conditions and the units used will vary from codec to codec. This situation certainly is a deterrent to the engineer who is cross-comparing codecs. In fact, in some cases, it is nearly impossible to compare specs.

Understanding noise specifications

Several transmission characteristics—including frequency response, noise, distortion, crosstalk, and delay —describe a codec. Each of these characteristics is important in its own right; however, noise is an especially important consideration when you're selecting a codec.

The noise is called idle-channel noise (ICN). As the name implies, it is the noise that is heard when the line is idle (that is, when there is no talking). Most often, phone users hear this type of noise when making a long-distance call. But the noise is present on every call, whether local or long distance.

One source of noise in a codec is quantization noise (discussed in part 1 of this 2-part series). Theoretically, if the analog input to the codec is at 0V (that is, if the line is idle), then the digital output of the codec should remain constant. But in reality, the digital output of the codec will fluctuate ever so slightly about the binary value assigned to zero. This fluctuation (noise) is caused by the analog-to-digital circuitry of the codec. The digital-to-analog section of the codec also contributes noise, but generally does so to a lesser degree. This fluctuation is heard as idle-channel noise.

Every codec will have an associated noise specification listed on its data sheet. Trying to decipher these numbers, however, can be frustrating. Furthermore, not every codec has its noise characteristics specified in the same units. This lack of standardization of noise-data specs makes it very difficult for the design engi-

In most applications, a codec's analog side connects to a SLIC (subscriber-line interface circuit).

neer to compare codecs. Nevertheless, by understanding the meaning of the different units used to specify noise levels, you can, in most cases, make noise comparisons between different codecs.

First, the noise characteristic might state that it is either C-message weighted or P-message (psophometrically) weighted.

The pass band of a telephone system's voice channel (a VF channel) goes from 0 to 4 kHz, and speech is confined to about 300 to 3000 Hz. Hence, the idle-channel noise that a user hears is typically limited to these frequencies as well. What's important, though, is not how much total noise is present on the phone line, but rather how much noise is present that's an annoyance to the telephone user. For example, noise in the frequency range of 100 to 300 Hz does not bother a telephone user as much as noise in the 1- to 2-kHz frequency range does.

C-message weighting is common in the US

To represent the way the human ear responds to noise at various frequencies, a special weighting curve called the C-message weighting curve was developed. This curve is shown in **Fig 2.** C-message weighting is used primarily in the US. In Europe, a slightly different weighting scheme is used; it is called psophometric weighting, or P-message weighting. The International Telegraph and Telephone Consultative Committee (CCITT) has defined noise as measured on a psophometer (an instrument for measuring circuit noise). Consequently, European manufacturers commonly use noise measurements based on psophometric weighting.

Hence, when noise measurements are made for a voice-grade transmission line, the type of weighting filter employed (that is, C-message, psophometric, or 3-kHz flat) must be specified on any units. For example, if a C-message weighted filter was used, then the suffix "C" is added to the unit (dBrnC). Likewise, if a psophometrically weighted filter is used, then the suffix "p" is added to the unit (dBmp).

Fig 2 shows the relationship between C-message and psophometric weighting curves, which, as you can see, are slightly different. Unless the codec's data sheet specs both C- and P-message weighted characteristics, you'll find it hard to compare the two.

Now consider some of the terms that are used to spec

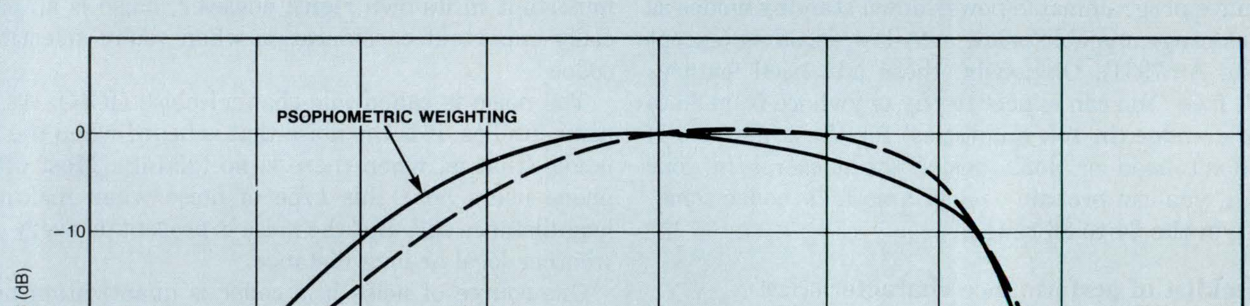


Fig 2—Telephone users are more irritated by noise *at certain frequencies than noise at other frequencies. Consequently, the C-message weighting curve, which represents the response of the human ear to noise at different frequencies, was developed for use in the US, and the slightly different P-message weighting curve is used in Europe.*

One thing codecs have in common is a lack of standardization in the way their specs are presented.

noise characteristics. Almost all engineers are familiar with the common units dB and dBm, but you might not have encountered dBm0, dBrn, dBrn0, etc.

Reference noise power is 1 pW

Recall that dB (decibel) is simply a unit of measure of relative power expressed logarithmically: $10\log(P_1/P_2)$. It is common to reference measured powers to one milliwatt and use units of dBm. However, because noise power levels are quite small (on the order of −40 to −90 dBm), it makes more sense to reference noise power to a much smaller reference power, such as one picowatt. Just as the suffix "m" of dBm indicates a power measurement relative to one milliwatt, so the suffix "rn" (as in dBrn) indicates a power measurement relative to reference-noise (rn) power, which is defined as one picowatt. Hence, 0 dBrn=−90 dBm, or 90 dBrn=0 dBm.

Sometimes values are expressed in units of dBp. Because no m or rn is inserted between the dB and the p, you might wonder what this unit means. Actually, dBp implies dBrnp, but data sheets don't include the "rn." Therefore, dBp is noise power (in dB) referenced to one picowatt and measured using a psophometrically weighted device.

Another suffix you might encounter is 0. The 0 implies that the measurement is referenced to or measured at a reference point in the system called the 0-dB transmission-level point (0TLP). The term 0TLP is somewhat confusing because the 0TLP is not necessarily a physical point in the system where you could attach a probe and measure the signal level. Instead, the 0TLP is simply a frame of reference (that is, a concept), and it may or may not have an associated physical point in the system that corresponds to the 0TLP.

The CCITT uses the concept of an 0TLP when it specifies the relationship between the PCM input of a codec and the level of the audio input in recommendation G.711 section 4. The G.711 recommendation specifies an 8-byte digital code (which represents a 1-kHz sine wave of a certain amplitude) that is to be fed into the decoder of the codec. Assuming that the gain through the decoder section of the codec is one, the analog output level should be 0 dBm0.

Consequently, data sheets for codecs will state the test conditions under which the transmission characteristics were measured. These test conditions usually state that the A/D and D/A sections are set for unity gain. Moreover, the test conditions also state the nominal input level (in dBm) that produces a level of 0 dBm0 (as defined by CCITT G.711). This level will vary from codec to codec.

For example, a codec's data sheet might state that an input of 4 dBm (across a 600Ω load) will produce a digital signal that, when decoded, produces an output of 0 dBm0. Hence, if you measure 23 dBrnC of noise at the analog output of this codec (assuming gain is one in both the A/D and D/A sections), you could restate this value as 19 dBrnC0 (19 dBrnC0=23 dBrnC−4 dB).

Measurements are referenced to 0TLP

All noise measurements are typically referenced to the 0TLP specified by CCITT G.711. That's good, because it lets you make apples-to-apples comparisons when examining noise characteristics of different codecs. In brief, any power measurement (whether it's expressed as dBm, dBrn, or some other unit) can be made at any point in the circuit or system and referred to 0 dB TLP (0TLP) by subtracting the transmission level from the power measurement. The transmission level is simply the ratio (in dB) of the power of a signal at some point to the power of the same signal at the 0TLP. The transmission level for a codec is usually stated in the test conditions of its transmission characteristics.

Two more considerations arise when you're evaluating a codec's noise performance. First, noise measurements are typically stated as two measurements, one for the transmit (A/D) section and one for the receive (D/A) section, so you may wonder how to combine these two noise measurements into one noise measurement for a port-to-port (that is, A/D-to-D/A) noise characteristic. Second, you'll want to know what noise specifications or recommendations a codec should meet.

Recall that these noise measurements are actually power measurements. You can't simply add the two numbers to get an overall noise figure. For example, if a codec has 14 dBrnC0 of transmit noise and 10 dBrnC0 of receive noise, the overall noise is not 24 dBrnC0. In order to combine the two noise measurements into one, you must first convert the numbers from dB (logarithmic form) to their linear values. Then you can algebraically add these two power measurements and convert the result back to dB.

One recommendation that codecs should meet is CCITT recommendation G.712, section 4, entitled "Idle-channel noise." In section 4.1, the recommendation states that the idle-channel noise should not exceed −65 dBm0p. The recommendation gives no value units of dBrnC0.

The other recommendation, which is probably more important to US manufacturers, is the EIA RS-464 specification regarding idle-channel noise for PBXs. The new recommendations (which EIA members have yet to vote on) will specify a maximum port-to-port noise value of 20 dBrnC and a recommended value of 16 dBrnC (these figures are for systems that use μ-law companding). As a point of comparison, AT&T's D3 spec allows a maximum idle-channel noise spec of 23 dBrnC0.

Despite the importance of the idle-channel noise spec, you should consider other noise characteristics as well when selecting a codec. For instance, the power-supply rejection ratio can have a great effect on the performance of a codec. Typical PSRR values range anywhere from 25 to 40 dB. These values should also weigh in your choice of a codec. For example, two different codecs may have very similar idle-channel noise characteristics, but one of the codecs may have a much better PSRR characteristic. This factor could help tip the balance when you're evaluating different codecs based on their transmission characteristics.

EDN

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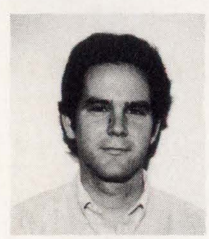
Author's biography



Brady Barnes is a member of the technical staff at Inter-Tel (Chandler, AZ), where he designs real-time software that controls telecommunications hardware; in addition, he designs digital-PBX hardware. He previously worked at Hewlett-Packard, and he received a BSEE degree from Arizona State University. He enjoys traveling, playing guitar, and conducting Bible studies.

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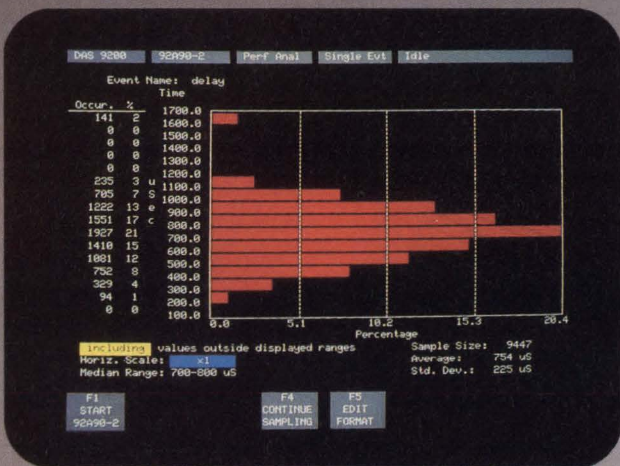

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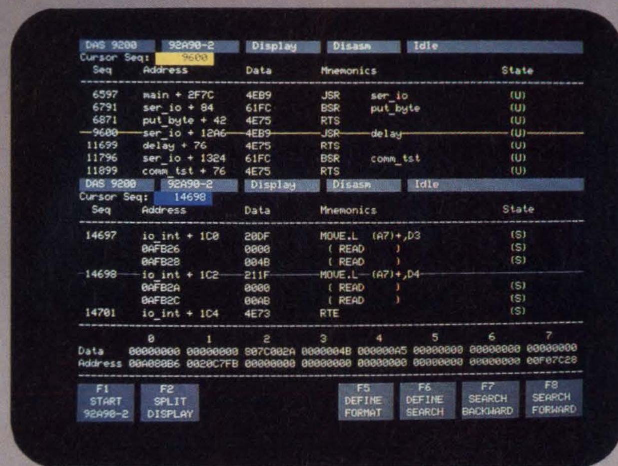

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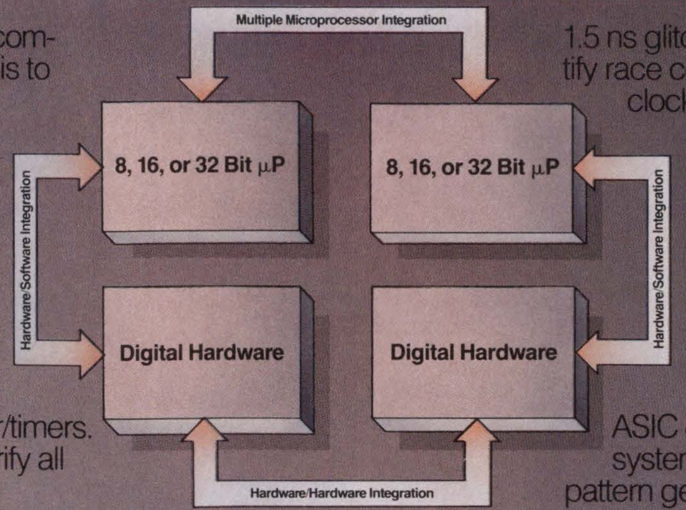

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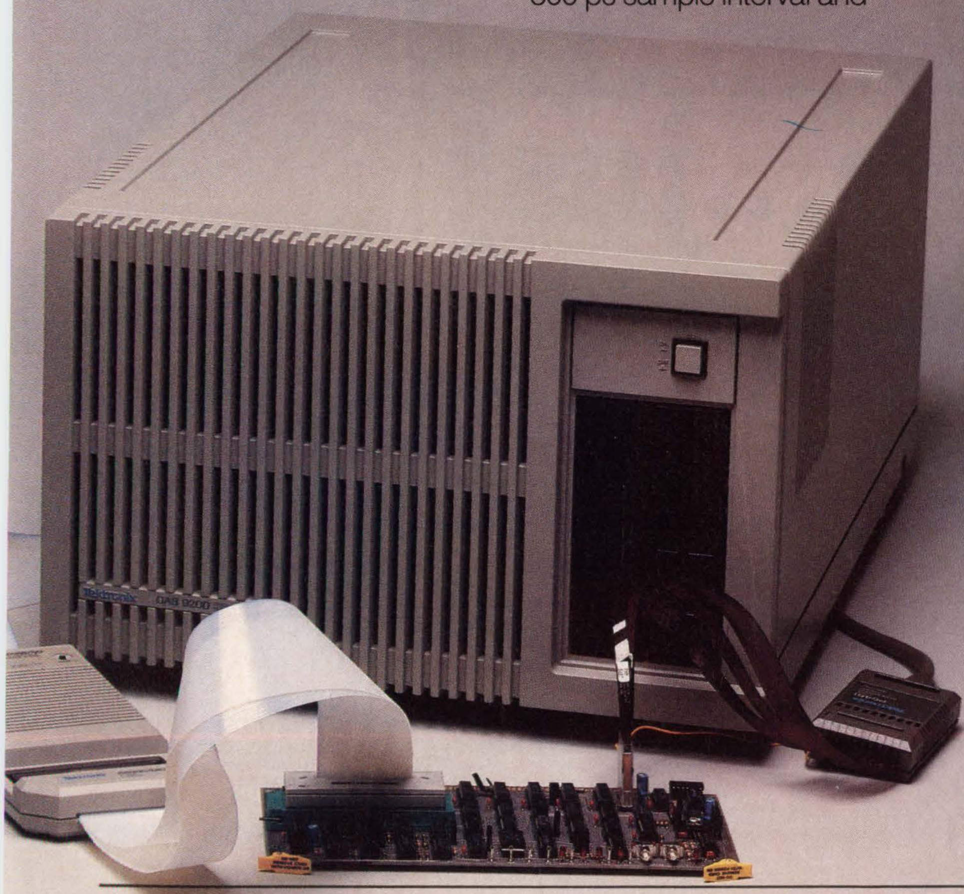

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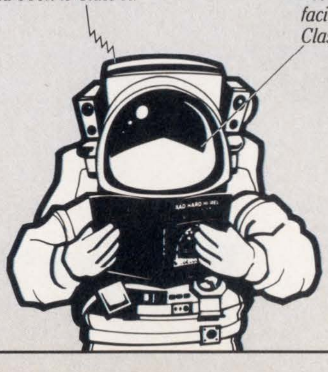

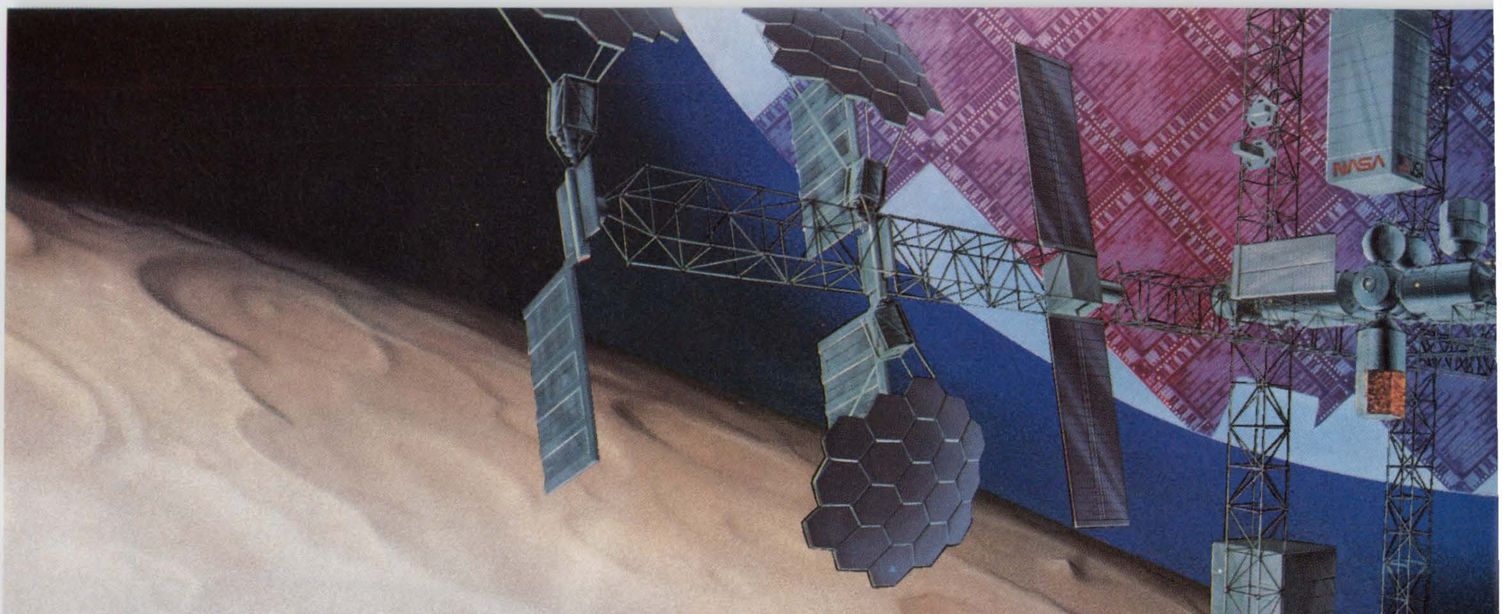

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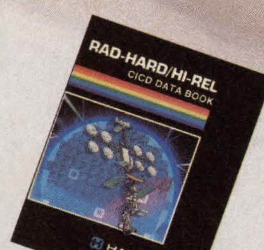

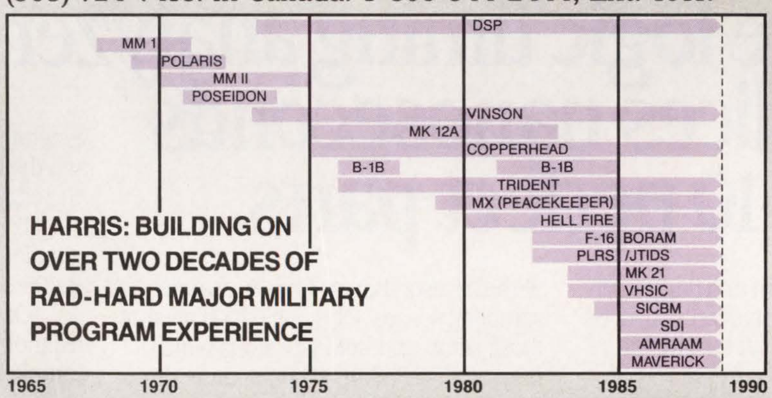

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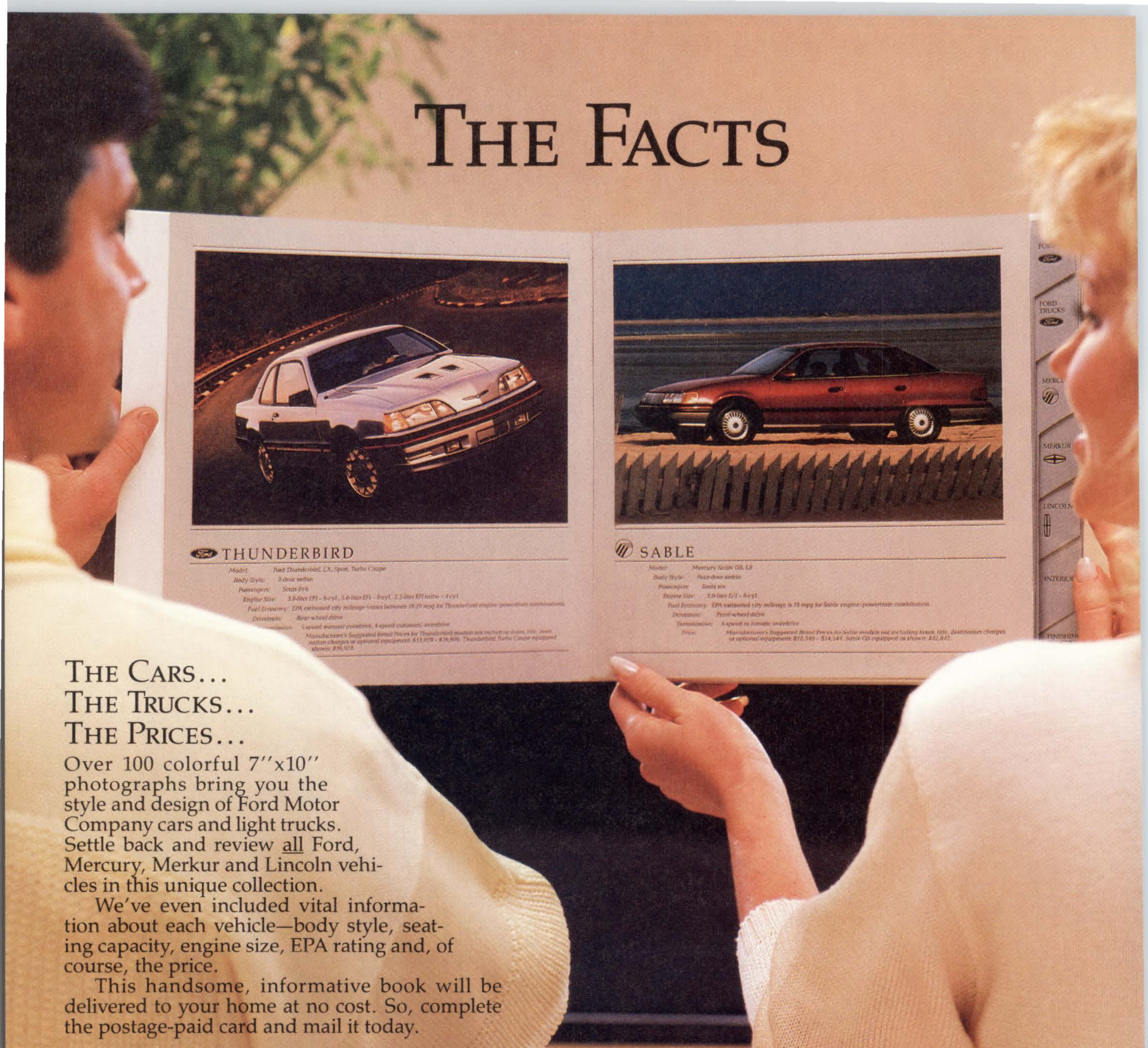

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Decode overlapped EPROM, RAM, and I/O

W H Payne
Sandia Labs, Albuquerque, NM

Today's large RAM and EPROM chips (32k and 64k bytes and up) let you reduce the size, the complexity, and even the cost of EPROM-based microcontroller systems. Using a physical memory composed of two 32k-byte RAM chips and two 32k-byte EPROM chips **(Fig 1)**, you can implement a 64k-byte memory in which the RAM and EPROM sections overlap almost completely.

This arrangement allows nearly full use of the addressable space because you can set the system's RAM/EPROM boundary where it belongs—near the application's highest EPROM location. A conventional system's boundary, on the other hand, must lie on an address location determined by the physical chip size (in bytes). For example, for a system based on three EPROM chips of 8k bytes each, the RAM must begin at the 24k-byte level. Therefore, if your application requires only 17k bytes of EPROM, you must forego 7k bytes of memory.

Fig 1's system also includes space for eight memory-mapped I/O devices, located at the top of the RAM for the convenience of microcontrollers such as the 8051, which lack an IO/$\overline{M}$ signal. The eight base addresses shown reserve 16 RAM locations for each device, leaving the top 128 RAM addresses inaccessible. You establish the RAM and EPROM boundary by using a DIP switch or jumpers to manually set the fence address B_{15}-B_8, shown in the memory's logical-organization diagram **(Fig 2)**.

In **Fig 3**, the magnitude comparator IC_1 compares the high byte of the fence address with the high-byte address lines and issues a signal (0 for RAM, 1 for ROM). (Comparing only the high bytes simplifies the decoding circuit but leaves as much as 256 bytes of RAM unaddressable.) Next, the 2- to 4-line decoder IC_2 uses the decoder signal and the A_{15} address line to activate the appropriate memory chip. The 8-input NAND gate IC_3 and the 3- to 8-line decoder IC_4 generate chip-select signals for the eight I/O devices. For active I/O devices, another 8-input NAND gate (IC_5) generates an IO/$\overline{M}$ signal that disables the selection of RAM. **EDN**

To Vote For This Design, Circle No 747

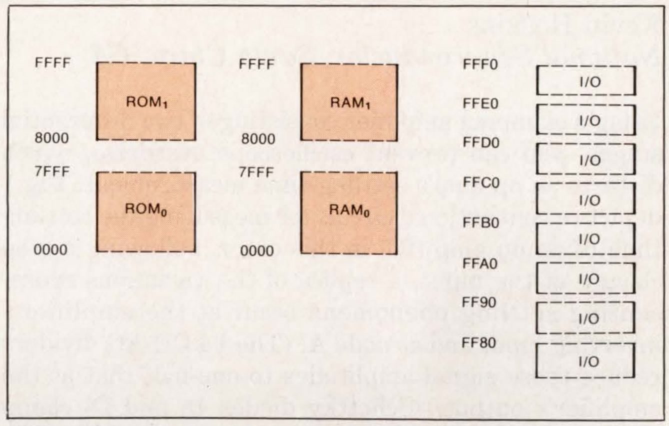

*Fig 1—**This 64k-byte memory system provides** 64k bytes of physical RAM virtually overlapped by 64k bytes of physical EPROM.*

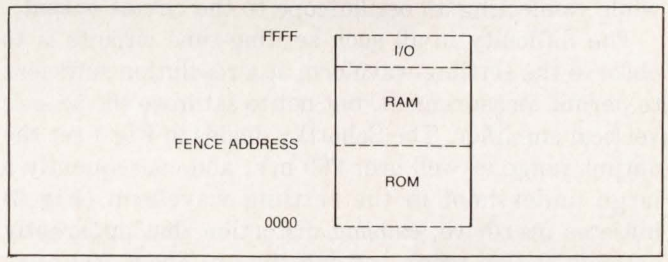

*Fig 2—**The logical organization of Fig 1's memory** locates memory-mapped I/O space at the top of the RAM and lets you set the boundary between the RAM and EPROM by manually setting a fence address.*

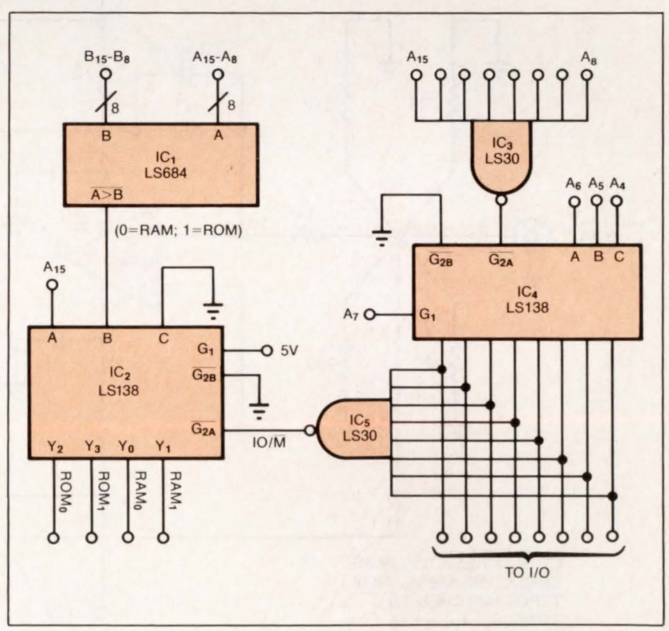

*Fig 3—**These ICs control Fig 1's memory.** IC_1 and IC_2 select the RAM and EPROM chips according to the fence-address position, and IC_3 and IC_4 decode I/O addresses. IC_5 generates an IO/$\overline{M}$ signal.*

Clamping amplifier simplifies measurement

Kevin Hoskins
National Semiconductor, Santa Clara, CA

Using a clamping amplifier consisting of two differential stages, you can prevent oscilloscope overdrive, which distorts an op amp's settling-time measurement. **Fig 1** depicts a conventional circuit for measuring the settling time of an op amp (IC_1 in this case). Following a step change at the input, a replica of the variations representing settling phenomena occur at the amplifier's inverting input and at node A. (The 1-kΩ/1-kΩ dividers reduce these signal amplitudes to one-half that at the amplifier's output.) Schottky diodes D_1 and D_2 clamp the signal excursions at node A, and the FET buffer (Q_1) allows you to preserve the fidelity of the signal while connecting an oscilloscope to the circuit output.

The difficulty in all such settling-time circuits is to observe the settling waveform at a resolution sufficient to permit measurement, but not to saturate the scope's vertical amplifier. The Schottky diodes in **Fig 1** set the output range at well over 200 mV, and consequently a large undershoot in the settling waveform **(Fig 2)** initiates overdrive, causing distortion that apparently extends the op amp's settling time to about 500 nsec. (The actual settling time is less.)

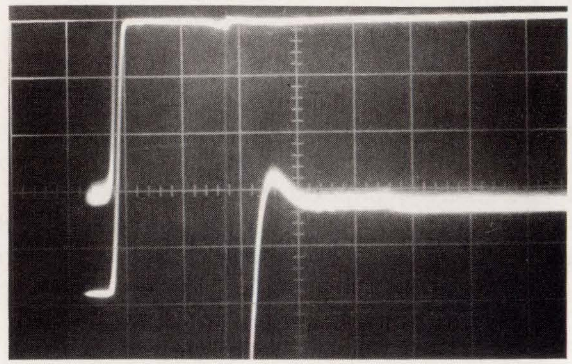

Fig 2—Fig 1's response to an approximate 10V-step input *shows an undershoot on the lower trace that overloads the scope. The resulting scope-recovery time produces an apparent 500-nsec settling time for the amplifier under test. Horizontal scale is 100 nsec/div; vertical scale is 2V/div for top trace, 5 mV/div for bottom trace.*

You can circumvent this distortion problem with a clamping amplifier that prevents scope overdrive by restricting the output range to ±125 mV **(Fig 3)**. Simply connect the amplifier's input to the circuit output of **Fig 1.** Another benefit of this configuration is that the voltage gain of 20 lets you display the signal at a lower sensitivity. In addition, the amplifier's 40-nsec

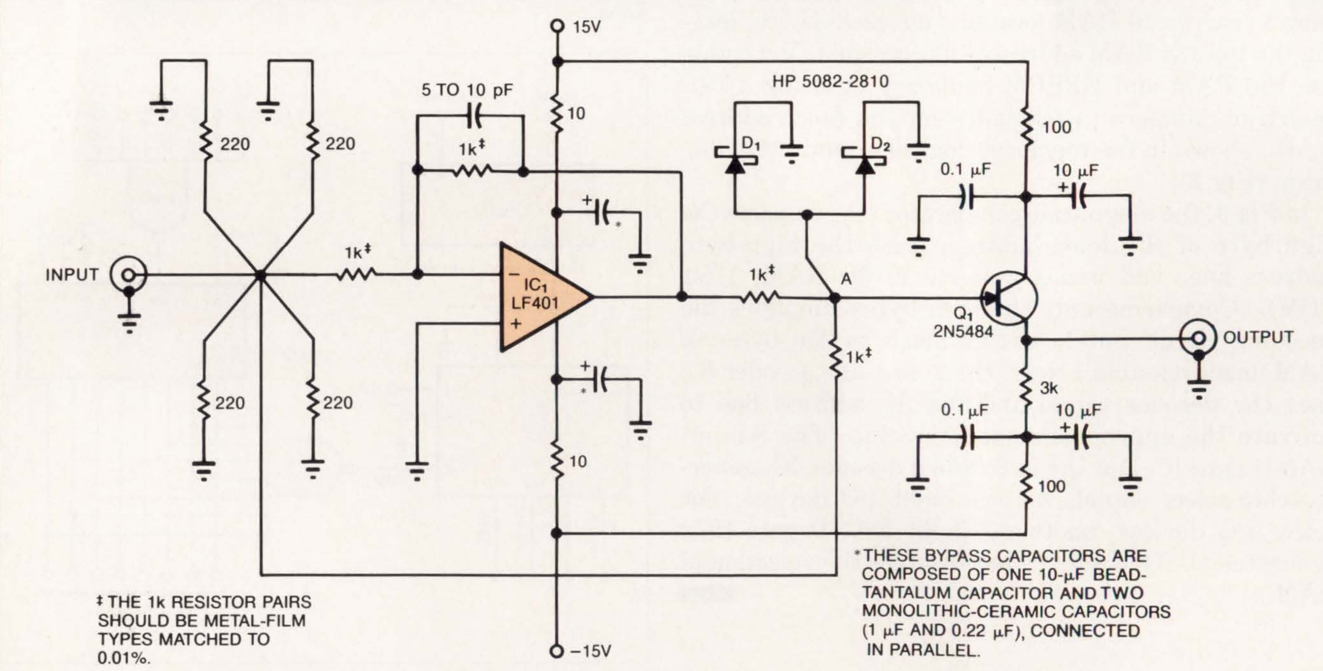

Fig 1—This circuit measures op-amp settling time *by creating a false summing node (A) at virtual ground, which tracks the amplifier's output settling excursions.*

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	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
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CIRCLE NO 173

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settling time (to within ±0.01%) doesn't affect the measurement of most monolithic op amps.

The clamping amplifier comprises two differential stages, Q_1-Q_2 and Q_3-Q_4, each consisting of RF transistors selected for a V_{BE} match of ±1 mV. For Q_1 and Q_2, resistor R_5 sets the transistors' emitter resistance R_E to 5.2Ω and sets the quiescent collector currents to 5 mA; R_{13} does the same for Q_3 and Q_4. The voltage gain for each stage then equals the equivalent right-hand collector resistance divided by $2R_E$.

Q_4's collector sees 25Ω (R_{10} in parallel with the 50Ω termination), and Q_2's collector sees 90Ω (R_2, R_{11}, and $2R_E\beta$ in parallel, where $\beta \approx 100$). Therefore, the first stage has a gain of 8, and the second has a gain of 2.5. The overall gain of 20 compensates for the gain of 0.5 in **Fig 1**'s circuit.

The second stage accommodates the ±125-mV clamping action, provided you load the output with a 50Ω resistor as shown. When Q_3 is off, the constant 10-mA current through R_{13} flows through Q_4's 25Ω collector load, producing a maximum output excursion of −250 mV. As a result, the settling waveform remains on the screen **(Fig 4)**. There is no recovery time because the waveform hasn't overdriven the scope. You can see that the actual settling time of **Fig 1**'s LF401 op amp is about 310 nsec.

To achieve maximum operating speed, the circuit layout should include a ground plane, and all connections to transistors Q_1-Q_4 should have the shortest possible lead lengths. The damping networks R_7-C_3 and R_{15}-C_{13} suppress parasitic oscillations in the two stages, and the 100-μF/100Ω CRC networks in the −15V line isolate the stages' supply voltage. If some oscillation persists, you can add a ferrite bead on the grounded lead of C_4, C_{14}, or both. **EDN**

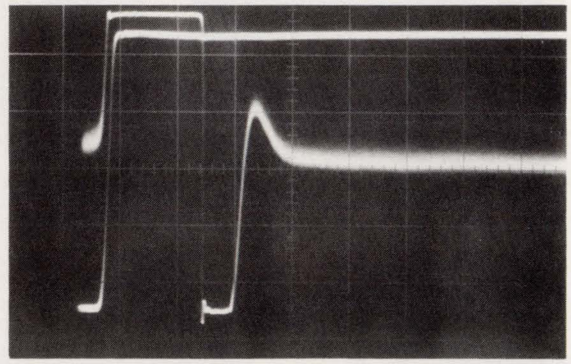

***Fig 4—This settling waveform shows that Fig 3's circuit** has clipped the undershoot (off the screen in **Fig 2**) at −250 mV, allowing accurate measurement of the amplifier's 310-nsec settling time. Horizontal scale is 100 nsec/div; vertical scale is 2V/div for top trace, 50 mV/div for bottom trace.*

To Vote For This Design, Circle No 746

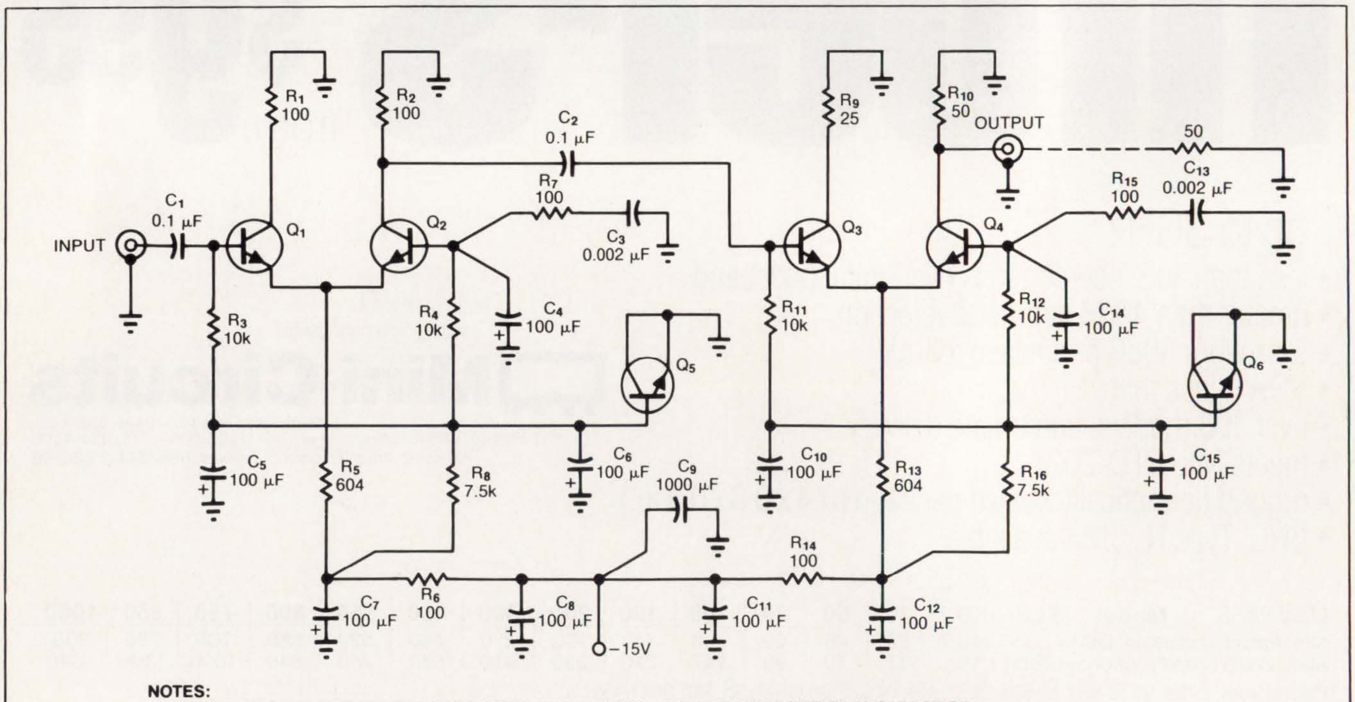

***Fig 3—This 2-stage RF amplifier amplifies and clamps** the output of **Fig 1**, letting you observe the final settling waveform at a resolution of ±1 mV without overdriving the oscilloscope's vertical amplifier.*


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Circuit deletes power-line cycles

Steve Ross
Kentrox Industries, Portland, OR

The circuit of **Fig 1** is useful in testing the response of equipment to a momentary loss of power. Each time you depress the normally on start switch, the circuit deletes zero to seven full or half cycles from the line voltage applied to the load. You can create various load-voltage waveforms by appropriate settings of the 8-pole DIP switch.

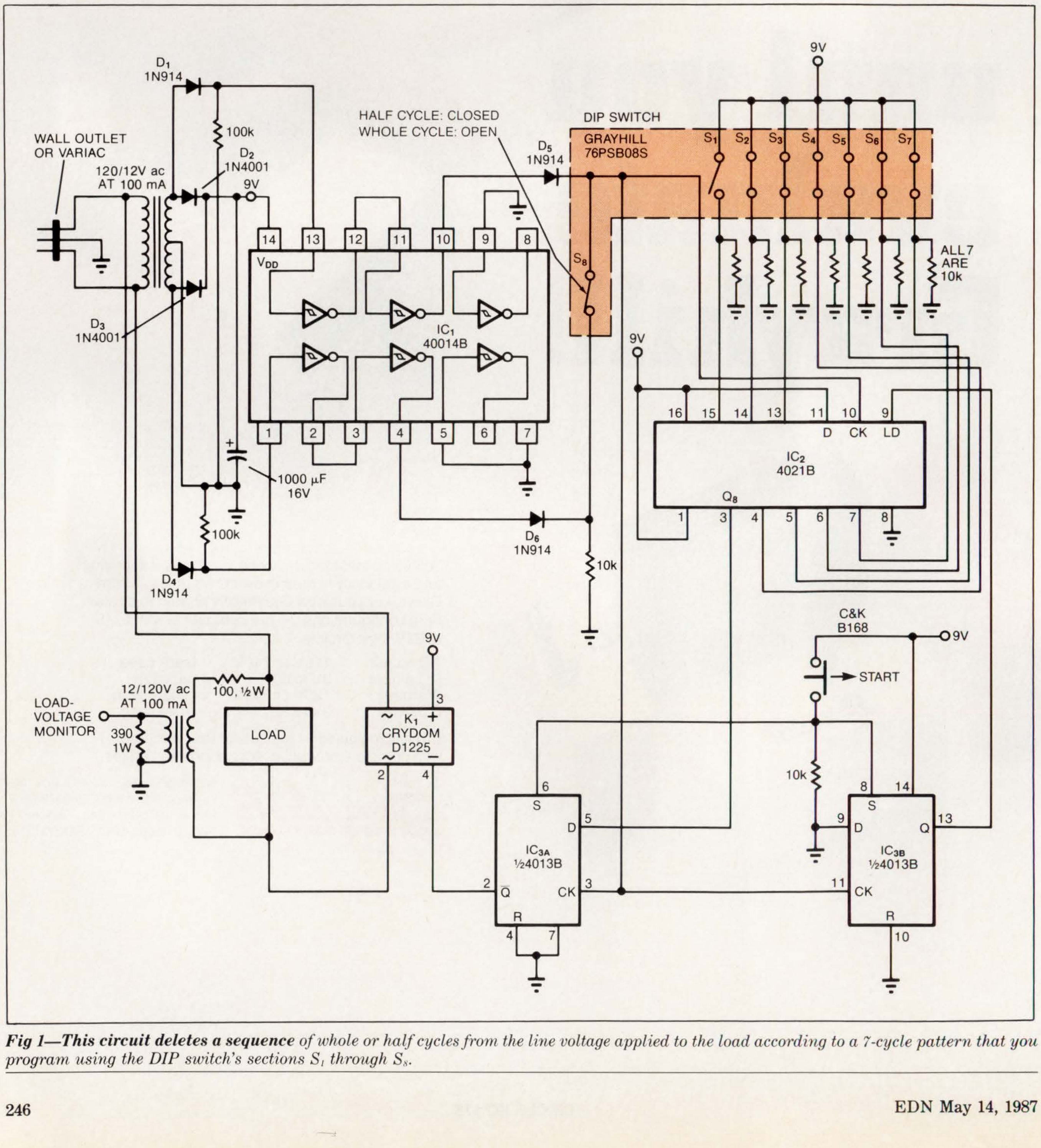

*Fig 1—**This circuit deletes a sequence** of whole or half cycles from the line voltage applied to the load according to a 7-cycle pattern that you program using the DIP switch's sections S_1 through S_8.*

The simple full-wave rectifier (diodes D_2 and D_3) supplies about 9V to the logic ICs. Diodes D_1 and D_4 also rectify the stepped-down line voltage and apply alternate half cycles to the Schmitt-trigger inverters in IC_1. The inverters square these half-sinusoidal waveforms, and diodes D_5 and D_6 constitute an OR gate that combines the inverter outputs for use as a clock signal to IC_2 and IC_3.

Section S_8 of the DIP switch determines whether the circuit deletes half or full cycles. The remaining sections (S_1 through S_7) determine the number and serial position of the cycles deleted. Shift register IC_2 converts the information in these sections to a serial bit stream, which controls the solid-state relay K_1 via flip-flop IC_{3A}. (An open switch deletes a full or half cycle by opening the relay, removing line voltage from the load during that period.)

In each scope photo of **Fig 2,** the top traces show the load voltage (which you measure at the monitor terminal,) and the bottom traces show the corresponding control voltage for the solid-state relay K_1 (which you measure at IC_{3A}, pin 2). You trigger the scope on the falling voltage (IC_3, pins 6 and 8), which you create by activating the start button. **EDN**

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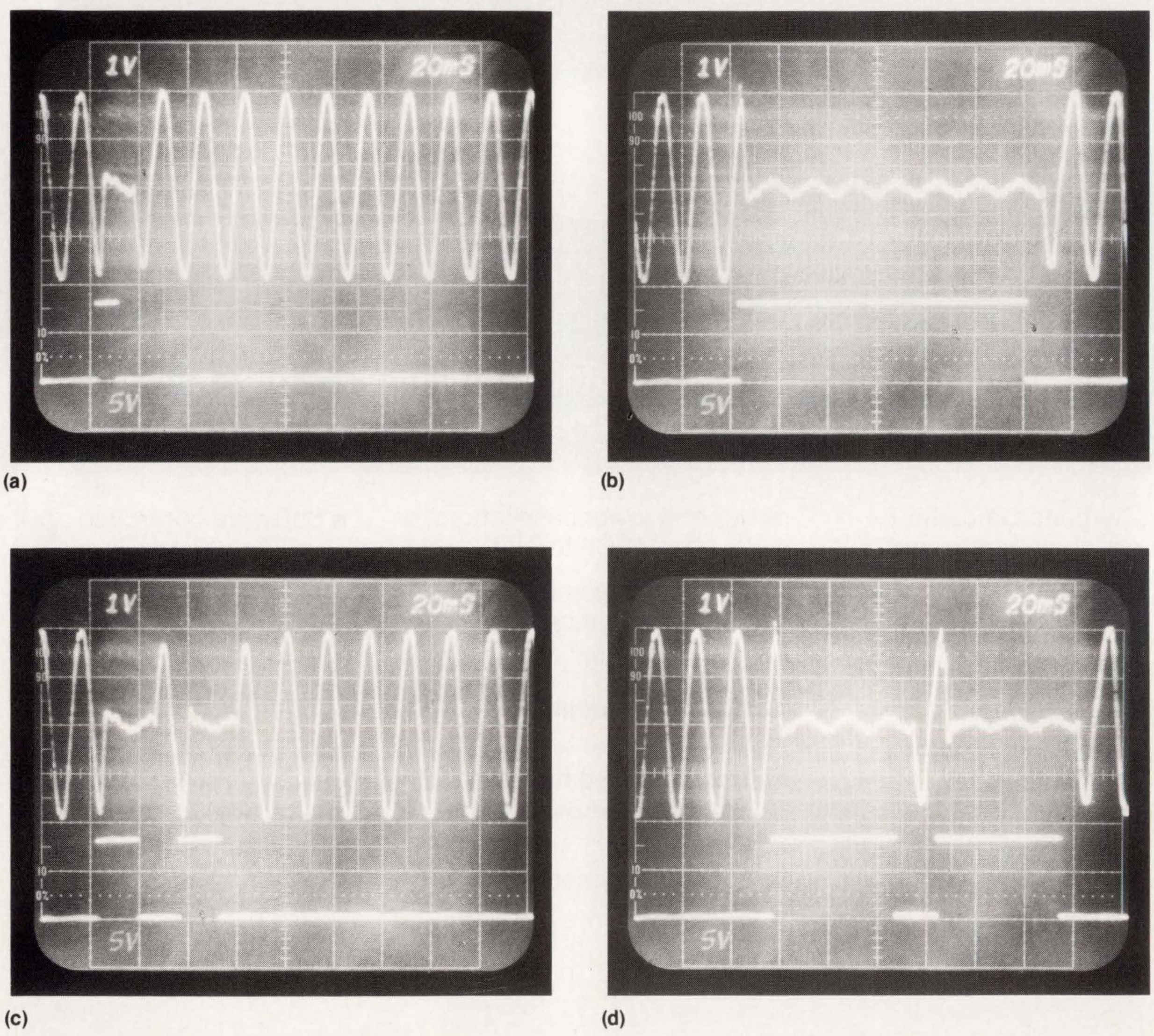

Fig 2—The top traces in these photos show the load-voltage waveforms, *following activation of the start switch, for various settings of the DIP switch: With S_1 open and all others closed, one half cycle is deleted **(a)**; with all switches open, seven full cycles are deleted **(b)**; with either S_1, S_2, S_5, and S_6 open or S_1, S_4, and S_8 open, two alternate full cycles are deleted **(c)**; and with all switches open except S_4, three full cycles on either side of a single full cycle are deleted **(d)**.*

Nonlinear load extends PLL frequency range

Basel F Azzam and Christopher R Paul
Coherent Communications, Hauppauge, NY

A PLL chip such as the 74HC4046 in **Fig 1** uses an external capacitor and resistor to set the frequency range for an internal voltage-controlled oscillator (VCO). By replacing the fixed resistor R_4 with a nonlinear one, you can extend the VCO's frequency range by a factor of 50 or more. For the component values shown, when pin 11 connects to R_4, the range is 17 to 300 kHz; in contrast, when the pin connects to the nonlinear load, the range is 2 kHz to 2 MHz.

Capacitor C_1 and the current through pin 11 control the PLL's output frequency. Higher current produces a higher frequency. When V_{11} equals 0.5V, for example, the high-β transistor Q_1 is off and the resistance from pin 11 to ground is R_2+R_3. As V_{11} increases, Q_1 turns on and draws more current from pin 11. Thus, the effective impedance, Z, is

$$Z=\frac{\dfrac{R_2R_3}{\beta(R_2+R_3)}+R_c}{\dfrac{R_3}{R_2+R_3}-\dfrac{V_{BE}}{V_{11}}},$$

where β is the transistor's beta and V_{BE} equals 0.75V. **EDN**

To Vote For This Design, Circle No 748

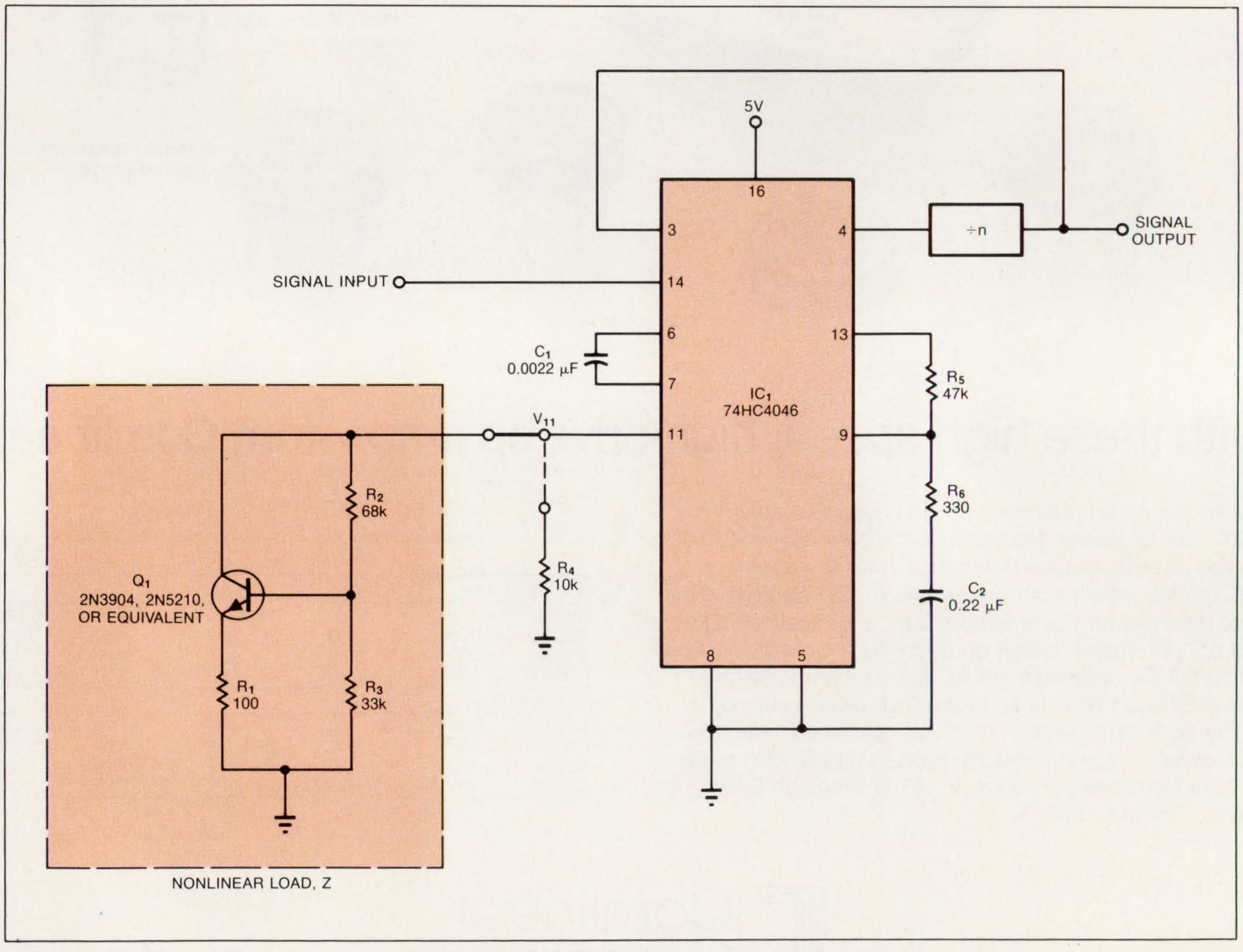

Fig 1—By connecting the nonlinear load Z *to pin 11 of the PLL chip IC_1, you can extend the PLL's frequency range by a factor of 50, as compared with that possible by using a fixed resistor (R_4).*

Model pnp-substrate capacitance correctly

Vincent Condito and Jerry Frazee
Fairchild Semiconductor, Mountain View, CA

A number of Spice programs incorrectly model the capacitance from a pnp transistor to the substrate. If you have such a program, you can correct the problem by creating a modified subcircuit model. Some Spice programs' models are incorrect because the capacitance to the substrate connects to the collector rather than the base. Other programs model the pnp transistor so that it does connect to the base, but they assign the wrong polarity of coefficient for the base-to-substrate voltage. Either of these can slow a circuit's operation during simulation.

Fig 1 shows the parasitic capacitance between a junction-isolated transistor and the substrate. Analysis programs model the capacitance between the substrate and the transistor's collector. (The substrate must connect to the circuit's most negative potential to ensure isolation of the transistors.) For lateral pnp transistors, however, the capacitance should connect between the substrate and the base.

First, a simple experiment will show how your program handles the pnp transistor. Connect the transistor (in software) as shown in **Fig 2.** With V_1 and V_2 set to 0V, the junction-to-substrate capacitance (CJS) should measure 2 pF (an .OP command causes the program to print Q_1's dc operating parameters). Next, change V_2 to 0.3V and run the program again—CJS should remain 2 pF. If the value changes, your program has incorrectly connected the capacitance to Q_1's collector. (Note that you enter this capacitance value as CJS, but the Spice printout labels it CCS.) Next, change V_2 back to 0V and V_3 to 0.3V. CJS should read 1.69 pF. If it reads more than 2 pF, the program is using the wrong polarity for the voltage coefficient of the capacitance.

If you find that your Spice program suffers from either of these two drawbacks, a different subcircuit model will take care of them **(Fig 3).** Eliminate the lumped substrate capacitance and instead add a simple diode from the base to the substrate. Use the same CJO, VJ, and M values that you used in connection with CJS. **EDN**

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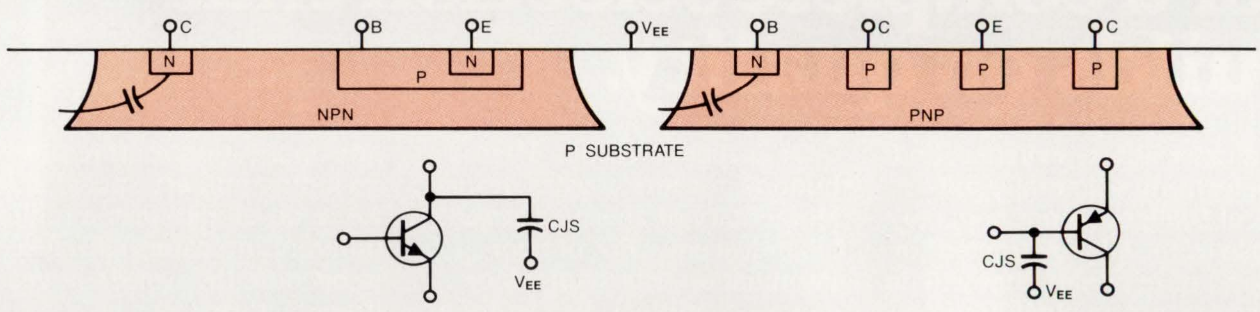

Fig 1—This wafer cross-section shows the structure of npn and pnp transistors used in bipolar-IC processes. As shown, the models for the junction-to-substrate capacitance (CJS) should connect to the npn's collector and to the pnp's base, respectively.

```
SPICE DECK TO CHECK FOR SUBSTRATE-CAP PLACEMENT ON PNP
.MODEL LPNP PNP CJS=2PF VJS=.5 MJS=.75

Q1   3  4  2  0  LPNP

I1   1  2  DC   50UA
V1   1  0  DC   10V
V2   3  0  DC    0V
V3   4  0  DC    0V

.OP
.END
```

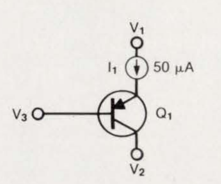

Fig 2—By representing a pnp transistor as shown, you can determine whether your Spice program is modeling it correctly.

```
.MODEL LPNP PNP CJS=0
.MODEL LSUB D CJO=2PF VJ=.5 M=.75

REM LATERAL PNP MODEL 1=COLLECTOR, 2=BASE, 3=EMITTER, 4=SUBSTRATE
.SUBCKT LATPNP 1  2  3  4
Q2  1  2  3  4  LPNP
D1  4  2  LSUB
.ENDS LATPNP
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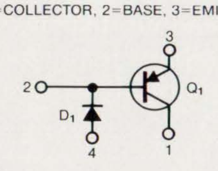

Fig 3—If your Spice program is incorrect, substitute this pnp-transistor model, which uses a diode to model the junction-substrate capacitance for the model in ***Fig 2.***

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✓	✓	✓		✓			PC TERMINALS
			✓				OCTAL-STYLE PLUG
						✓	DUAL COIL LATCHING
					✓		TIME DELAY
✓	✓						7.5 AMP CONTACTS
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✓	✓	✓	✓	✓		✓	2 AMP CONTACTS
✓	✓		✓	✓		✓	LOW LEVEL CONTACTS
✓	✓		✓	✓		✓	DRY CIRCUIT CONTACTS

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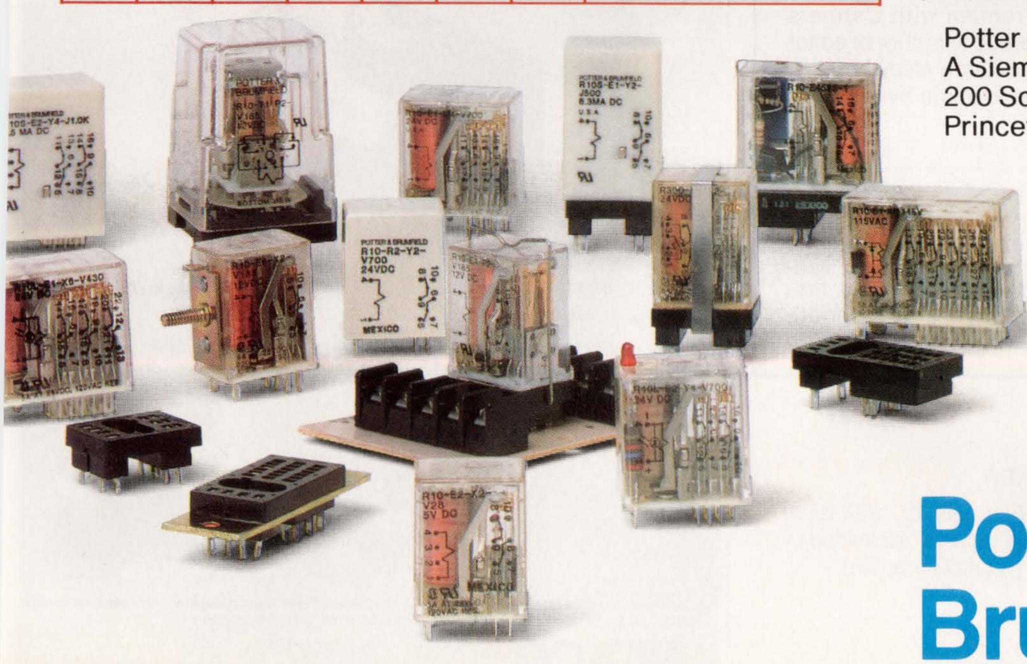

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Princeton, Indiana 47671-0001.

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CIRCLE NO 176

Design Entry Blank

$75 Cash Award for all entries selected by editors. An additional $100 Cash Award for the winning design of each issue, determined by vote of readers. Additional $1500 Cash Award for annual Grand Prize Design, selected among biweekly winners by vote of editors.

To: Design Ideas Editor, EDN Magazine
Cahners Publishing Co
275 Washington St, Newton, MA 02158

I hereby submit my Design Ideas entry.

Name ____________________

Title ____________ Phone ____________

Company ____________________

Division (if any) ____________________

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City ____________ State ________ Zip ________

Design Title ____________________

Home Address ____________________

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Social Security Number ____________________
(Must accompany all Design Ideas submitted by US authors)

Entry blank must accompany all entries. Design entered must be submitted exclusively to EDN, must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested.

Exclusive publishing rights remain with Cahners Publishing Co unless entry is returned to author or editor gives written permission for publication elsewhere.

In submitting my entry, I agree to abide by the rules of the Design Ideas Program.

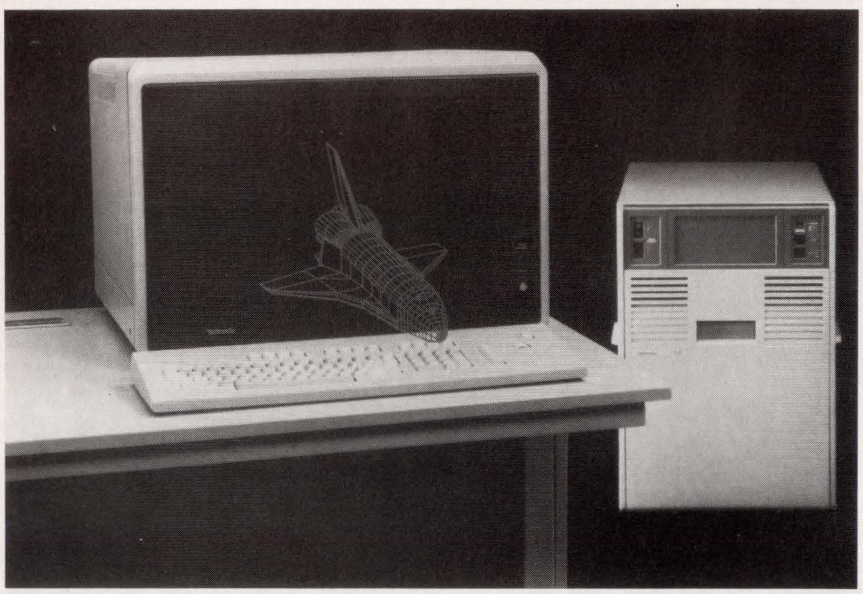
Signed ____________________

Date ____________________

Your vote determines this issue's winner. All designs published win $75 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now,** by circling the appropriate number on the reader inquiry card.

ISSUE WINNER

The winning Design Idea for the February 19, 1987, issue is entitled "Two-way amplifier uses few parts," submitted by Rudy Stefenel of Luma Telecom (Santa Clara, CA).



3-D WORKSTATION

- *Produces stereoscopic images*
- *Suitable for CAD/CAM applications*

The 4126 workstation displays a stereoscopic image by switching between two slightly offset views of an image. A liquid-crystal shutter polarizes views for the right and left eyes. The user wears glasses that distinguish between the right-eye- and left-eye polarization. The workstation can accept single 4128- or 4129-style 3-D picture files, run those workstations' software, and then create the appropriate left- and right-eye stereo images. The basic configuration consists of a 19-in. display with 1280×1024-pixel resolution, 2M bytes of user RAM, and a controller that displays 16 colors from a palette of 16 million. You can opt to boost the number of displayable colors to 256. Other options include shaded-surface stereoscopic viewing, as much as 6M bytes of memory, a DMA interface, floppy-disk drives, additional RS-232C interfaces, interfaces for a color copier and for mass storage, and a mouse. From $29,950.

Tektronix Inc, Box 15273, Portland, OR 97070. Phone (800) 225-5434; in OR, (503) 235-7202.

Circle No 351

32-BIT μC

- *Features an open-bus architecture*
- *Based on a 16-MHz 68020 μP*

The Macintosh II computer is a 32-bit computer that incorporates a 16-MHz Motorola 68020 μP and a 68881 floating-point coprocessor chip in its standard configuration. The μC also comes with 1M byte of RAM that's expandable to 8M bytes. With add-in boards, you can expand the RAM to as much as 1.5G bytes. The computer features an Appletalk network interface, a SCSI interface port, two RS-422 serial ports, and six 32-bit NuBus expansion slots. The NuBus's fair-arbitration and geographical-addressing procedures allow an add-in card to identify itself, eliminating the need to set DIP switches for system configuration. You can choose either a 12-in. monochrome monitor or a 13-in. RGB monitor. Both are analog monitors that allow the computer to display as many shades of gray or color as the human eye can distinguish. Basic unit, $3898; unit with 40M-byte hard disk, $5498.

Apple Computer Inc, 20525 Mariani Ave, Cupertino, CA 95014. Phone (408) 996-1010. TLX 171576.

Circle No 352

COLOR MONITOR

- *Provides 1600×1280-pixel resolution*
- *Features new shadow-mask and yoke technologies*

The HM-5219 color monitor has 1600×1280-pixel resolution. Incorporating a new yoke design, the monitor achieves an 89-kHz horizontal scan rate (as opposed to the 64-kHz scan rate of the previous design). The monitor increases the resolution of the company's 1280×1024-pixel monitor by 50%. The color monitor employs a proprietary transistor technology, which further enhances resolution. $5200.

Hitachi America Ltd, Office Automation Systems Div, 950 Elm Ave, Suite 170, San Bruno, CA 94066. Phone (415) 872-1902. TLX 176308.

Circle No 353

BUBBLE MEMORY

- *Uses removable bubble-memory cartridges*
- *Available as a military- or commercial-grade unit*

The PBU85D bubble-memory unit provides you with as much as 2M bytes of nonvolatile mass storage suitable for use in severe environments that would preclude the use of mechanical drives. The unit accepts two removable bubble-memory cartridges, which are available

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☐ Please rush me the free 1987 Sensym Handbook. *(This handbook contains over 160 pages of application information and product specifications.)*

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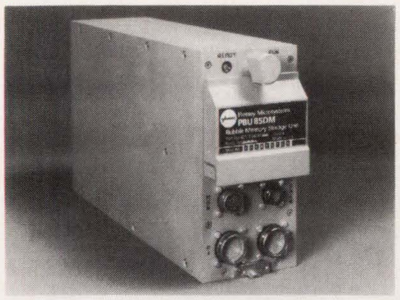
CIRCLE NO 112



with storage capacities of 512k bytes or 1M byte. The cartridges provide an average data-access time of 10 msec, and you can software-select the size of memory blocks from 256 to 4096 bytes per block. The cartridges measure 4.5×2.7×0.9 in. and are interchangeable between units. The memory unit interfaces to a host system via an RS-422 serial port at data rates of between 75 and 76.8k baud. A range of alternative serial and parallel interfaces is also available. The PBU85D has an operating-temperature range of −55 to +80°C and is available as a commercial- or military-grade component. From £3000 to £10,000, depending on grade and memory capacity.

Plessey Microsystems Ltd, Water Lane, Towcester, Northants NN12 7JN, UK. Phone (0327) 50312. TLX 31628.

Circle No 354

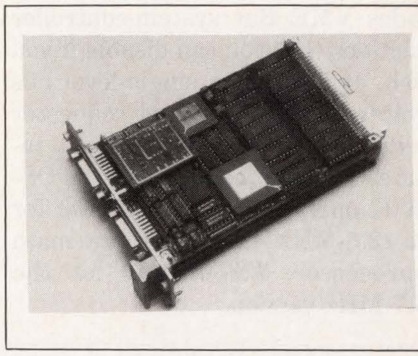
Plessey Microsystems Inc, One Blue Hill Plaza, Pearl River, NY 10965. Phone (914) 735-4661. TWX 710-541-1512.

Circle No 355

CPU CARD

- *Has 68020 µP and 1M byte of dual-port RAM*
- *Single-height Eurocard format*

The VMPM68KC provides you with a 68020-based VME Bus CPU system in a single-height Eurocard. The CPU system occupies two adjacent slots in a VME Bus J1 back-



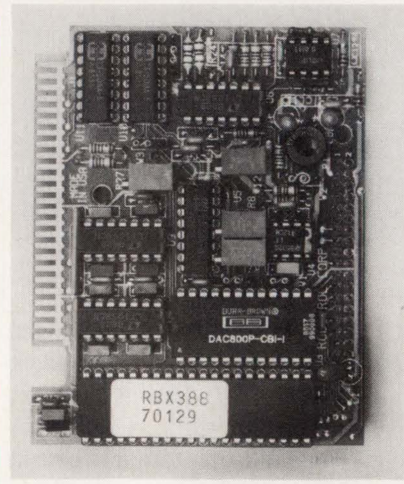
plane. It includes a 12.5- or 16.7-MHz 68020 µP, an optional 68881 math coprocessor, 1M byte of zero-wait-state static RAM, and 512k bytes of ROM/EPROM space. Its additional onboard facilities include two serial I/O ports and a real-time clock. The 68020 µP has 32-bit access to the static RAM and ROM/EPROM via a dedicated local bus. The static RAM is also ported to the VME Bus via an A24/D16 slave interface. The processor has an A24/D16 master/slave interface to the VME Bus. The processor board includes VME Bus system-controller functions that you can disable if you wish. It also has a single-level bus arbiter and an interrupt-requester module. Its software support includes a debug monitor and the OS-9/68K operating system. $2100 for the 12.5-MHz version with the math coprocessor; $2850 (100) for the 16.7-MHz version.

Pep Modular Computers GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 8974. TLX 541233.

Circle No 356

Pep Modular Computers Inc, 600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661. TLX 6711521.

Circle No 357



ANALOG I/O

- *Features eight differential or 16 single-ended inputs*
- *All inputs have 12-bit resolution*

The RBX388 analog I/O module has 16 single-ended or eight differential inputs and eight analog outputs on a single-width SBX module of less than 10 in^2. You can configure the 12-bit inputs as either bipolar or unipolar inputs with ranges from 100 mV to 10V or ±100 mV to ±10V. The analog output ranges are 0 to 5V, 0 to 10V, −5 to 5V, and −10 to 10V. Input protection on the analog lines is specified to ±32V. You can change the gain of the input amplifier, and, consequently, the full-scale range of the module, by changing a programming resistor. $525.

Robotrol Corp, 16100 Caputo Dr, Morgan Hill, CA 95037. Phone (408) 778-0400.

Circle No 358

ACCELERATOR

- *For PC/AT, Multibus II, NuBus, and VME Bus*
- *Executes 20M flops*

The Vortex accelerator board contains a vector preprocessor that brings 64-bit floating-point operation to the PC/AT, Multibus II, NuBus, and VME Bus environments. The board performs 20M flops (single precision) and 10M

flops (double precision). The vector preprocessor converts standard Fortran 77 programs to programs having vector-processing-compatible formats, thus making it easier to port existing applications to the accelerator. The board transfers data internally at the rate of 80M bytes/sec. The accelerator for the PC/AT performs over 2M flops in 64-bit mode. At the high end, in a system where the board uses its full speed—an 80M-byte/sec data-transfer rate—the board achieves 5M flops in 64-bit mode. PC/AT version, from \$9900; bus versions, from \$11,900.

Sky Computers Inc, Foot of John St, Lowell, MA 01852. Phone (617) 454-6200.

Circle No 359

GRAPHICS SYSTEMS

- *Include plug-in card and monitor for IBM PC/AT computers*
- *Provide 1024×768-pixel gray-scale or color displays*

The Xcellerator range of 1024×768-pixel display systems for the IBM PC/AT and compatible computers includes a monochrome version that provides eight shades of gray, and color versions that are capable of displaying 16 or 256 colors from a palette of 16 million. Versions are available for interlaced and non-interlaced displays. Each system comprises a CRT monitor and a plug-in card for the IBM PC/AT. Based on Texas Instruments' 34010 graphics-processor chip, the system is capable of continuous short-vector drawing at speeds of 80,000 vectors/sec, long-vector drawing at 1.25M

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Our Insta-Lok grades are unique patented technology; structural cyanoacrylates offering the strength and durability of an anaerobic and the cure time of an instant adhesive. Unlike anaerobics, these compounds perform well on platings, stainless steel and plastic fasteners without the use of surface activators.

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Campbell, CA 95008

Outside California (800) 538-3091, In California (408) 379-9701

PACER TECHNOLOGY

CIRCLE NO 180

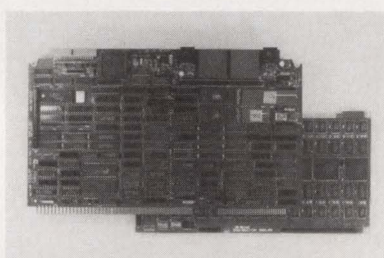
pixels/sec, and 8×16-pixel character generation at 25,000 characters/sec. The plug-in card's graphics processor can run application programs with minimal intervention from the host computer, and it can access as much as 7M bytes of memory. You can add an optional National Semiconductor 32081 floating-point processor to the card. The vendor offers program-development tools and driver software for a number of CAD and graphics packages. Monochrome version, £2495; color versions, from £4195 to £5395. The plug-in cards for the color systems are available separately at between £2195 and £2895.

Cambridge Computer Graphics Ltd, Unit 33, Clifton Rd, Cambridge CB1 4ZN, UK. Phone (0223) 214444. TLX 817274.

Circle No 360

Cambridge Computer Graphics, 6201 Ascot Dr, Oakland, CA 94611. Phone (415) 530-4148. TLX 797032.

Circle No 361



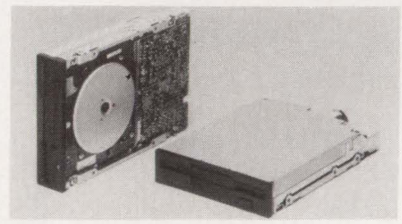
GRAPHICS PROCESSOR

- *For Multibus I architecture*
- *Features 1280×1024-pixel resolution*

The MG-1280 Multibus I card provides 1280×1024-pixel resolution and draws at a rate of 35,000 vectors/sec max. An 8-bit color-lookup table allows you to display 256 colors simultaneously from a palette of 16 million. An onboard 32016 CPU and HD63484 drawing processor together enable the board to draw as many as 15,000 characters/sec. The board performs bit-block tranfers at the rate of 13M transfers/sec. It also provides high-level graphics commands such as Draw Line and Fill Area. $4995.

Matrox Electronic Systems Ltd, 1055 St Regis Blvd, Dorval, Quebec, Canada H9P 2T4. Phone (514) 685-2630. TLX 05822798.

Circle No 362



DISK DRIVES

- *3½- and 5¼-in. floppy drives offer 2M and 3.2M bytes*
- *Use standard heads, media, and codes*

Two floppy-disk drives, the YD-701 and the YD-801, use standard heads, media, and encoding, so they are compatible with the 1.6M- and 1M-byte standards. The YD-701 is a 3½-in. floppy-disk drive that provides 2M bytes of storage. The YD-801 5¼-in. floppy-disk drive provides 3.2M bytes of storage. The manufacturer uses a new read circuit that allows greater recording densities. The YD-701 is fully read-write compatible with 2M- and 1.6M-byte drives that use high-density media. The drive is read-write compatible with 1M-byte media formats and read compatible with 500k-byte media formats. The YD-801 uses the same data-transfer rate, track density, and number of tracks as do 1.6M-byte drives. YD-701, $225; YD-801, $240.

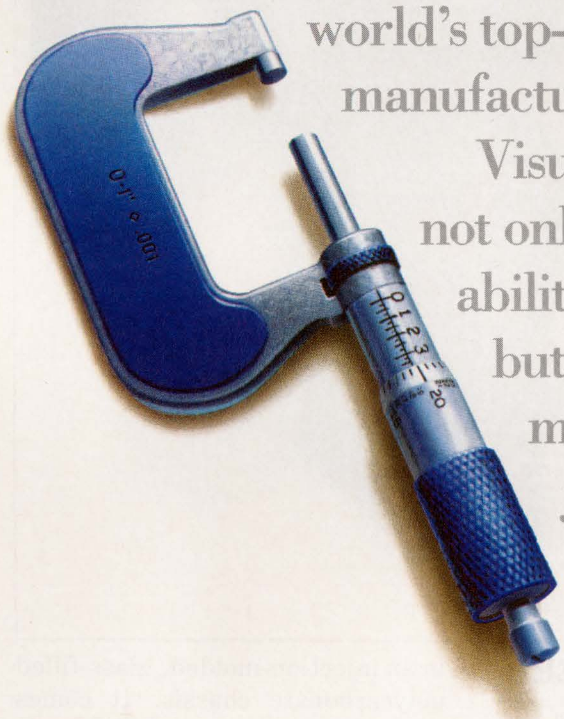
C Itoh Electronics Inc, 19300 S Hamilton Ave, Torrance, CA 90248. Phone (213) 327-9100.

Circle No 403

VISULA

END-TO-END ELECTRONIC DESIGN AUTOMATION

Design Accuracy is the bottom line in CAE/CAD performance. And Visula's precision has made it the world's top-of-the-line software for generating manufacturable PCBs.



Visula's integrated relational database not only enhances the CAE designer's ability to detect errors while designing, but to simulate designs prior to committing to a layout. And the system is just as useful to the CAD engineer, because of its gridless routing and its total compatibility with evolving technologies.

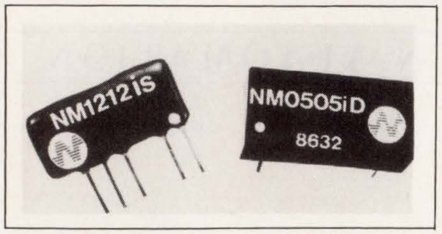
Experience the design accuracy of Visula from Racal-Redac. Call or write for more information.

4 Lyberty Way, Westford, MA 01886 Phone: (617) 692-4900 **RACAL-REDAC**

RACAL

CIRCLE NO 181

COMPONENTS & POWER SUPPLIES



DC/DC CONVERTERS

- *11-W/in³ power density*
- *500V dc I/O isolation*

The NM Series 0505i, 1212i, and 1515i dc/dc converters use state-of-the-art surface-mount technology to achieve power densities exceeding 11 W/in³. Operating from a 5V dc input, the converters generate ±5, ±12, and ±15V dc, respectively. The output power equals 750 mW; the input-to-output isolation is 500V dc. The converters' efficiency is 80%, and the operating temperature (with no derating) ranges from −25 to +80°C. The DIP models require 0.32 in² of board space, and the SIP versions take up 0.18 in². DIP model, $19.50; SIP model, $13 (1000).

International Power Sources Inc, 10 Cochituate St, Natick, MA 01760. Phone (617) 651-1818. TWX 510-100-3630.

Circle No 363

CAPACITORS

- *Designed for high-temperature applications*
- *2000-hour nominal load life*

DP Series radial-lead capacitors feature a solid tantalum electrolyte that ensures stable electrical performance over −55 to +125°C. They also feature a stable oxide layer, which minimizes leakage for long periods of time. The leakage current is ≤0.01 CV or 0.5 μA, whichever is greater. Capacitance values range from 0.1 to 150 μF, and the tolerance specs at ±20, ±10, or ±5%. The load life is 2000 (±12) hours at 85°C. The capacitors utilize a self-extinguishing epoxy resin, which avoids epoxy rundown on the leads. You can obtain the units on tape and reel. $0.069 (1000).

International Components Corp, 105 Maxess Rd, Melville, NY 11747. Phone (516) 293-1500.

Circle No 364

THERMAL RECORDER

- *200×800 dot/in. resolution*
- *Comes with demonstration software*

The AR-41 2-in. thermal recorder/printer can print graphics, text, bar codes, histograms, and waveforms. It uses curve-smoothing software to produce images with resolutions as high as 200×800 dots/in. The unit can use paginated and semiperforated or plain 50-mm roll paper, and it can print the 96-character ASCII set horizontally or vertically. It features an automatic paper-feed system. The recorder/printer is housed in an injection-molded, glass-filled polycarbonate chassis. It comes with demonstration software (a diskette-based program) that runs on IBM PCs and compatibles with MS DOS 2.0 or later versions. The software demonstrates the recorder features and standard operational modes and checks for proper functioning of the unit. A Centronics interface lets you send data directly from a PC to a printer. $420.

General Scanning Inc, Box 307, Watertown, MA 02272. Phone (617) 924-1010.

Circle No 365

LOOK WHAT YOU PAY.

LOOK WHAT YOU GET.

Single unit prices for KEPCO/TDK SERIES ERX SINGLE OUTPUT SWITCHING POWER SUPPLIES

240 WATTS
$210

Includes optional cover CA-18, $13.*
2.76″H x 12.91″D x 4.84″W
(70mm x 328mm x 123mm)
5.5 lbs (2.5Kg)

120 WATTS
$153

Includes optional cover CA-17, $11.*
2.76″H x 8.90″D x 4.84″W
(70mm x 226mm x 123mm)
3 lbs (1.4Kg)

60 WATTS
$94

Includes optional cover CA-16, $11.*
2.36″H x 7.09″D x 4.84″W
(60mm x 180mm x 123mm)
1.5 lbs (0.7Kg)

30 WATTS
$65

Includes optional cover CA-15, $11.*
2.17″H x 5.51″D x 4.84″W
(55mm x 140mm x 123mm)
1.5 lbs (0.7Kg)

(Substantial OEM quantity discounts available.)
**The optional cover is shipped separately.*

For complete specifications and 144-page Applications Handbook & Full-Line Catalog write Dept. JVF-12, KEPCO, INC., 131-38 Sanford Ave., Flushing, NY 11352 USA
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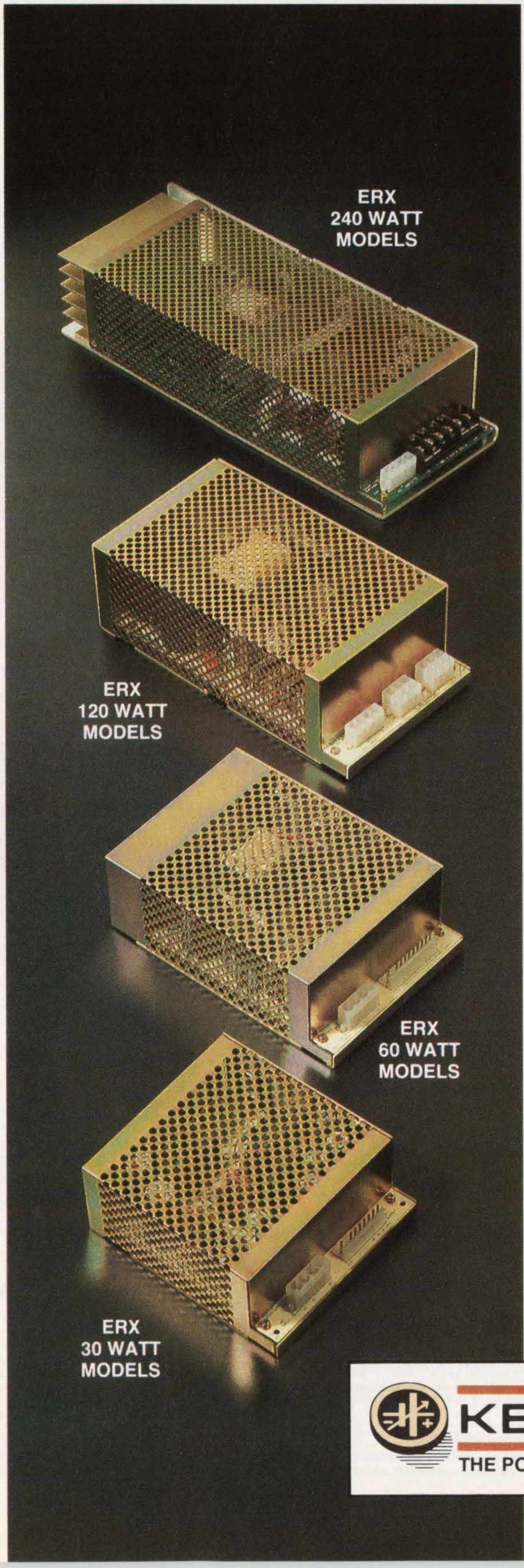
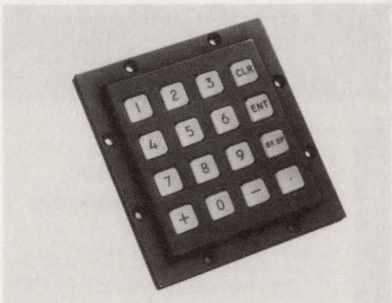


- **5V, 12V, 15V, and 24V models available in all sizes**
...output of 12V, 15V, and 24V models can be adjusted −30, +10% around the nominal; output of 5V models, −20%, +10%.
- **Overvoltage protection**
...shuts down the switching oscillator drive and reduces the output to zero when voltage reaches the OVP setting.
- **Rectangular current limiting**
...lets you drive non-linear loads without their high initial surge causing the power supply to "lock out." Allows operation in series or parallel.
- **Remote error sensing**
...compensates for voltage drops up to 0.35V per wire.
- **68-80% efficiency**
...240W model operates its FETs at 100 KHz.
- **Selectable 115/230V input**
...(85-132V or 170-264V.) Also operates from 260-340V d-c input.
- **Built-in EMI filter**
...attenuates line-conducted EMI below FCC 20780, Class B.
- **Soft start**
...limits a-c input surge.
- **8mm spacing and transformer insulation to meet IEC 380, VDE 0806**
...approved by TÜV Rheinland. Also listed by UL and certified by CSA.
- **Optional enclosure**
...for EMI shielding, & protection.
- **Quick connect**
...Molex input/output connectors (240 Watt model has a barrier strip). Optional cable kits available.

KEPCO®
THE POWER SUPPLIER™



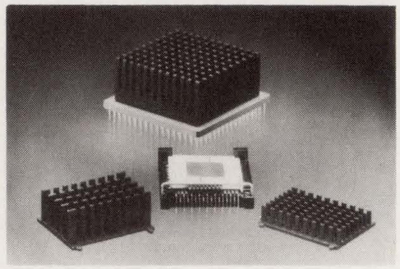
KEYBOARDS

- *Available with built-in background illumination*
- *Totally sealed construction*

Panelswitch keyboards are available in 3×4, 4×4, and 4×5 configurations. They feature gold-plated snap-dome switches, a polyester sealing membrane, and illuminated or nonilluminated keys mounted on a pc board—all securely retained by a low-profile bezel. The spst switches spec a 1Ω max contact resistance. X-Y matrix or single-pole common-bus outputs are standard. Panelswitches are available with built-in background illumination. The illuminated versions have black opaque characters on a white translucent key; nonilluminated models have white legends on a black background. Custom legends are available in both styles. EMI/RFI shielding is also available. $30 (25). Delivery, six to eight weeks ARO.

IEE Inc, Planar Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 366



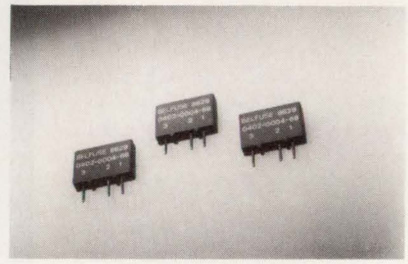
HEAT SINKS

- *Require no thermal grease or epoxy*
- *Thermal resistances to 4°C/W*

Designed for chip carriers and pin-grid arrays, these pin-fin heat sinks rely on impingement cooling techniques. Models 2305 and 2306 were specifically designed to become the latch cover for the 268-5400 leadless chip carrier socket from 3M-Textool. No thermal grease or epoxy is needed for attachment of the heat sinks. The 2305 stands 0.5 in. tall and has a thermal resistance of 3°C/W with 500 ft/minute impingement. The 2306 stands 0.26 in. tall and has a 4°C/W thermal resistance. Model 2330 is designed for pin-grid arrays in the 149-pin count range. It has a 1.3°C/W thermal resistance. Model 2306, $0.36 (1000).

Thermalloy Inc, Box 810839, Dallas, TX 75381. Phone (214) 243-4321.

Circle No 367

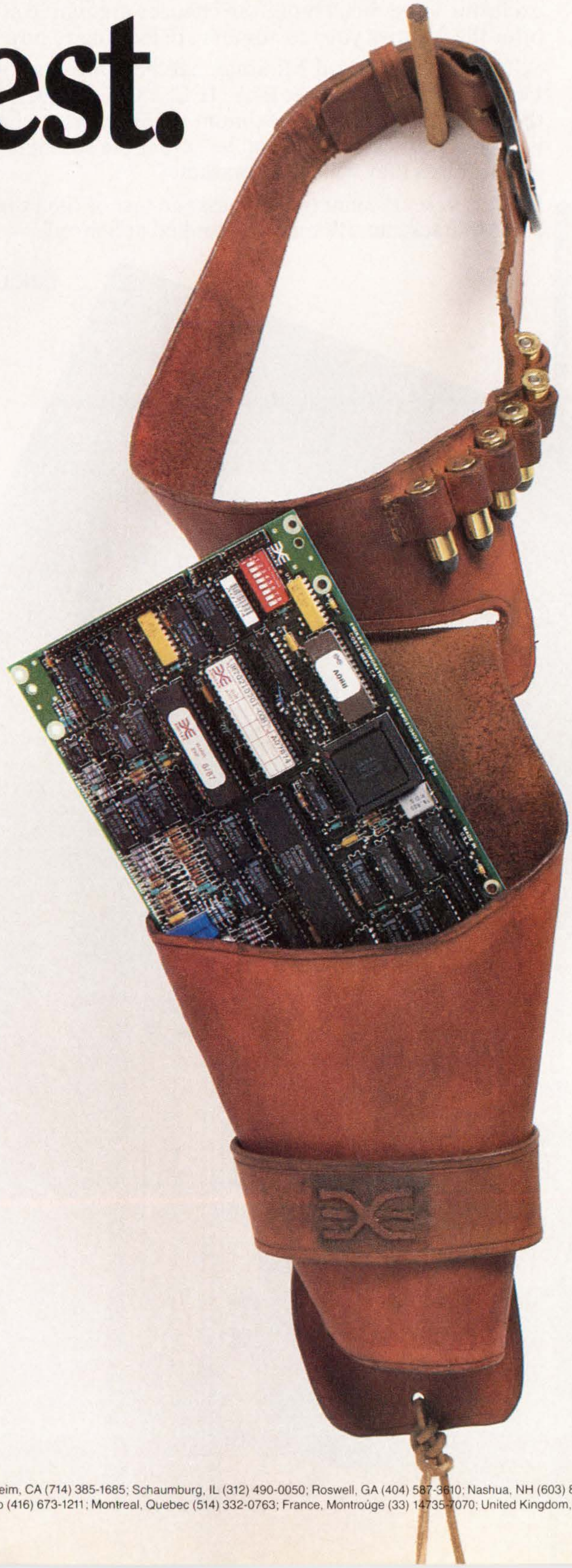


DELAY LINES

- *ECL and TTL compatible*
- *Delays of 100 to 1000 psec*

Delay lines in the 0402 Series are available in SIPs and feature delays of 100 to 1000 psec in 100-psec increments. They employ gold-plated pins to maximize conductivity and the precision of delays, and they are TTL and ECL compatible. Other specifications include output rise times (measured from 20% to 80%) of 0.9 to 1.5 nsec, a temperature coefficient of 100 ppm/°C max, and an operating range of −55 to

The fastest SCSI controllers in the West.



Emulex blows away the competition with lightning fast SCSI performance. Up to 24MHz disk interface transfer rates, the fastest in the industry, by using our own VLSI technology. Intelligent controller firmware for optimum efficiency, allowing overlapping operations on up to four peripherals to reduce system delays. And comprehensive implementation of the Common Command Set.

Our controllers even reduce SCSI overhead by 50% with command queing/linking. Plus, we provide peak SCSI bus optimization with a powerful disconnect/reconnect algorithm.

EMULEX SCSI PERFORMANCE MATRIX

CONTROLLER	MT02	MT03	MD01	MD21/S2	MD23
TYPE (# of Drives)	TAPE (1)	TAPE (1)	DISK (2)	DISK (2)	DISK (4)
FIFO	16KB	16KB	16KB	32KB	64KB
LOGICAL BLOCK SIZE (Bytes)	256/512	256/512	256/512	256/4096	256/4096
CCS	N/A	N/A	NO	YES	YES
ECC	16-Bit CRC	16-Bit CRC	48-Bit	48-Bit	48-Bit
DRIVE INTERFACE SPEED	90 KBYTES	90 KBYTES	Up to 24 MBits	Up to 24 MBits	Up to 24 MBits
DRIVES SUPPORTED	QIC-36 Type	QIC-44 Type	ST506	ESDI	ESDI

With this kind of commitment to performance and efficiency, it's easy to see why Emulex is the top gun in SCSI. To find out more about our fast SCSI solutions call 1-800-EMULEX3. In California (714) 662-5600. Or write Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626.

EMULEX

Emulex SCSI products are stocked nationally by Hamilton/Avnet, Kieruff Electronics and MTI Systems Corp.

Gotcha!

CIRCLE NO 183

U.S. Regional Offices: Anaheim, CA (714) 385-1685; Schaumburg, IL (312) 490-0050; Roswell, GA (404) 587-3610; Nashua, NH (603) 882-6269. **International Offices:** Australia, Eastwood, N.S.W. (61) 02-858-4833; Canada, Mississauga, Ontario (416) 673-1211; Montreal, Quebec (514) 332-0763; France, Montroúge (33) 14735-7070; United Kingdom, Bracknell, Berkshire (44) 344-484234; West Germany, Munich (49) 89304051.

Schroff®

OUR CABINETS WITHSTAND THE TOUGHEST TEST OF ALL – THE TEST OF TIME

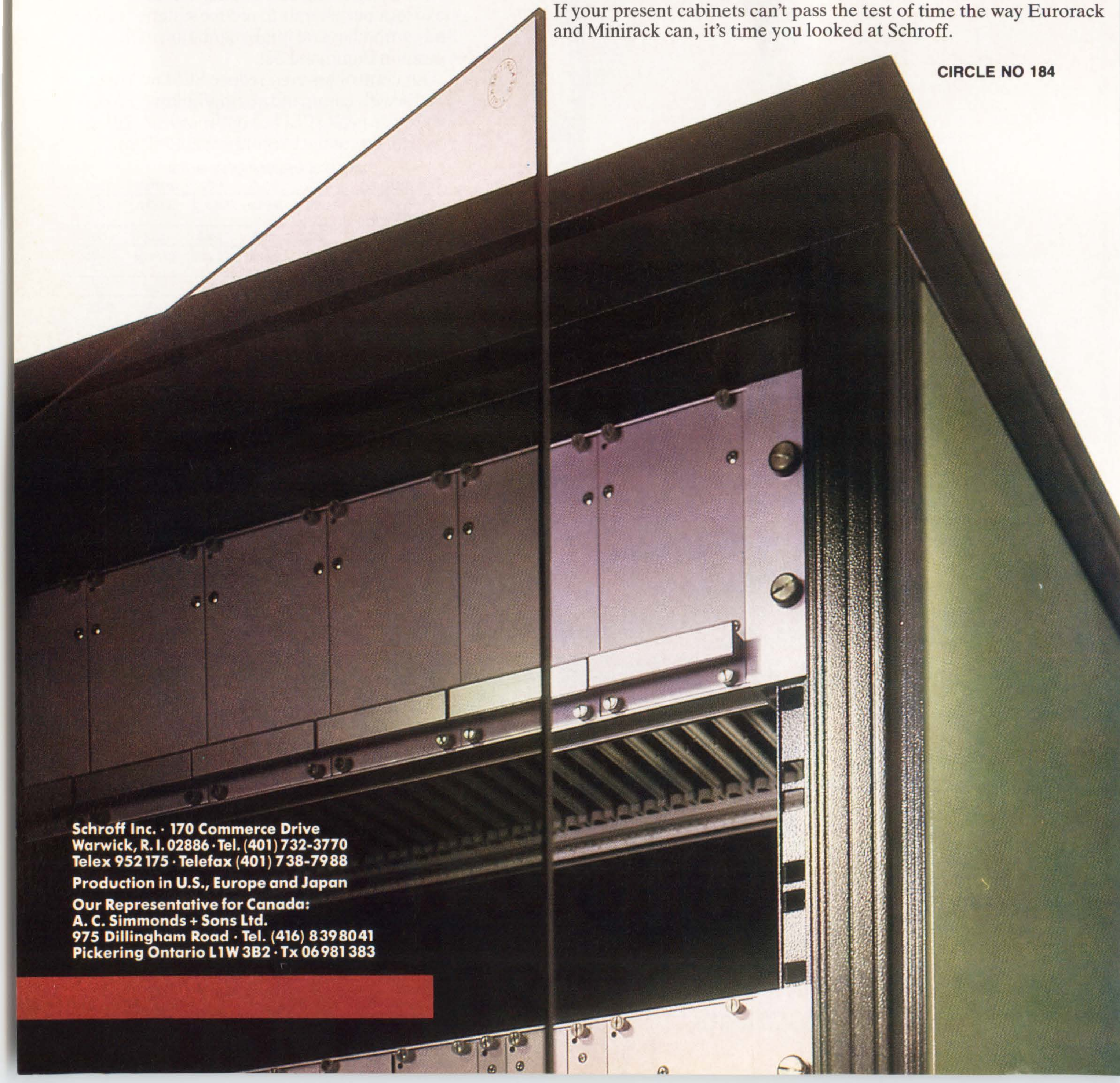
As a company dedicated to technical excellence, Schroff helps you prepare for the future. So you can be the first to take advantage of it.

For example, our Eurorack and Minirack cabinets are designed to help you meet changing market conditions. They're available in more than 45 different sizes, with a wide range of accessories and options, including RFI/EMI shielding, full glass doors (a Schroff exclusive), and much more. So chances are, you'll always be able to offer the features your customers are looking to buy.

Schroff Eurorack and Minirack cabinets are manufactured in the United States. They meet EIA, IEC, VDE and DIN standards. And they're made to deliver maximum rigidity and strength. As a result, you, and your customers, can be sure these cabinets will last as long on the job as they will in the market.

If your present cabinets can't pass the test of time the way Eurorack and Minirack can, it's time you looked at Schroff.

CIRCLE NO 184



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Warwick, R. I. 02886 · Tel. (401) 732-3770
Telex 952 175 · Telefax (401) 738-7988

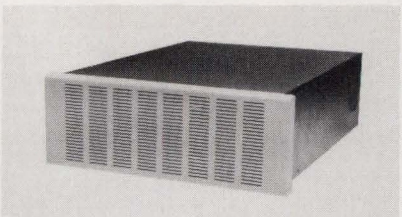
Production in U.S., Europe and Japan

Our Representative for Canada:
A. C. Simmonds + Sons Ltd.
975 Dillingham Road · Tel. (416) 839 8041
Pickering Ontario L1W 3B2 · Tx 06 981 383

+125°C. The working voltage equals 50V dc, and distortion measures 7.5% max. All units are bidirectional and built to conform to MIL-L-23859. $2.05 (1000).

Bel Fuse Inc, 198 Van Vorst St, Jersey City, NJ 07302. Phone (201) 432-0463.

Circle No 368



ENCLOSURE

- *Accommodates two disk drives*
- *Includes two power supplies*

The SA-H123S mounting enclosure accommodates two Fujitsu Winchester disk drives. Each drive has its own 175W power supply, rear on/off switch, and fan. Each supply provides 5V at 25A, −12V at 5A, and 24V at 5A. Two additional fans provide cooling with side exhaust to maximize air flow. The enclosure is available in two versions: a tabletop unit, which includes a front panel and rubber feet, and a version that mounts in a standard 19-in. Retma rack. The enclosure is designed to withstand operational temperatures of 0 to 50°C, and humidity ranging to 95%, noncondensing. $1392.

Sigma Information Systems, 3401 E La Palma Ave, Anaheim, CA 92806. Phone (714) 630-6553. TLX 298607.

Circle No 369

POWER SUPPLY

- *Provides a 3000W output*
- *0.5% line and load regulation*

The COM6000 provides a nominal output of 5V at 600A. The output is user adjustable over a 4.5 to 7.2V dc range. A full complement of inter-

How To Turn A Computer Into A Shock Absorber:

Surge and ESD are the most common cause of failure in semiconductor-based equipment. And with existing protection technology, it's all so unnecessary.

KeyTek manufactures the broadest line of surge and ESD test equipment in the world.

Every year, lightning, switching transients, human ESD and other "shocks" account for billions of dollars in downtime and repair costs and for untold numbers of disgruntled customers.

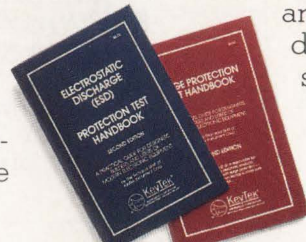
And we can't help but ask, "WHY?"

The facts are that, today, well-developed protection technologies, test standards and test instrumentation exist. And with a comprehensive, company-wide program, any computer, microprocessor, or semiconductor-based product can be turned into a nearly invincible "shock absorber" able to withstand thousands of volts of surge and ESD without failure, malfunction or the need for user-supplied protection.

At KeyTek, we provide the equipment and the expertise to help you test your product's vulnerability to surge and ESD at every step of the manufacturing process from design to the inspection of incoming components to the QA/QC testing of complete systems on the manufacturing floor to the interconnection and networking of systems in the field.

Among our customers are the biggest and most successful companies in the world. They manufacture computers, telecommunications equipment, manufacturing and process control systems, microprocessor-based appliances and other consumer goods. And their products are resistant to the ravages of surge and ESD. As a result, our customers enjoy considerably lower after sales costs, happy and satisfied customers, a superior competitive position and higher profits.

We'd like to convince you that you too can enjoy these benefits. Send for free copies of our Surge and ESD protection handbooks. They describe the common causes of surge and ESD as well as protection technologies, the latest relevent test standards and the most sophisticated test equipment.



You may get your copies by calling our Technical Services Department at (617) 658-0880.

Or send your request on a company letterhead to KeyTek Instrument Corporation, 260 Fordham Road, Wilmington, MA 01887.

KeyTek®

KeyTek Instrument Corporation, 260 Fordham Road
Wilmington, MA 01887 Phone: (617) 658-0880
TELEX: 951389

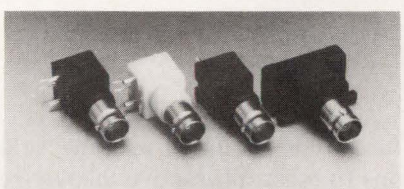
CIRCLE NO 185

COMPONENTS & POWER SUPPLIES

face signals includes remote-sense, remote-margin, power-good, and logic-inhibit signals, and an isolated sequence to enable the output. The supply features overvoltage protection and ac under- and overvoltage lockout. Self-testing front-panel lamps indicate power-on, overcurrent, overvoltage, and overtemperature conditions. The supply complies with the emission standards of FCC Docket 20780, Class B. Combined line and load regulation is better than 0.5%, and the temperature coefficient is less than 0.02%/°C over the 0 to 50°C operating range. The Output ripple and noise is less than 100 mV p-p, and the powerholdup time equals 12 msec. The efficiency exceeds 75%. $3500. Delivery, stock to six weeks ARO.

CEAG Electric Corp, 1324 Motor Parkway, Hauppauge, NY 11788. Phone (516) 582-4422.

Circle No 370



CONNECTORS

- *Provide pc-board-mounting BNC connections*
- *Incorporate a threaded section for securing into panels*

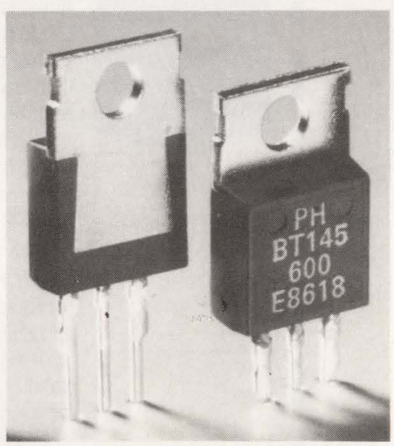
This family of pc-board-mounting BNC connectors includes versions for horizontal or vertical mounting. The body of each connector incorporates a molded thread to secure the connector into the panel, which can be 4 mm thick. A flat surface on one side of the thread resists the rotational torque associated with the insertion and removal of a mating plug. You can fix the socket to the pc board with self-tapping screws, or by soldering in special mounting pins. The body of the socket insulates the connector from the pc board and from the panel, and it incorporates standoffs, which allow solvent cleaners to penetrate beneath the connector assembly. The connectors have a nominal impedance of 50Ω and a working voltage of 500V dc or ac peak. Polypropylene insulation provides an insulation resistance greater than 500 MΩ, and the silver-plated contacts meet the requirements of BS-9210 N0001 Part 2 and MIL-C-39102. The connectors operate over −40 to +85°C. A low-profile version is available. Approximately $1 (OEM qty).

Greenpar Connectors, Cambridge Rd, Harlow, Essex CM20 2ER, UK. Phone (0279) 27192. TLX 81404.

Circle No 371

Automatic Connector Corp, 400 Moreland Rd, Commack, NY 11725. Phone (516) 543-5000.

Circle No 372



THYRISTORS

- *Handle 25A rms and surge currents as high as 300A*
- *Have a typical gate-controlled turn-on time of 2 μsec*

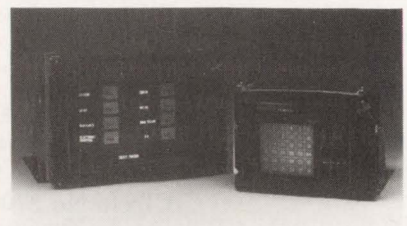
BT145 Series thyristors have an on-state current rating of 25A rms and are housed in TO-220 plastic packages. In addition, they can handle surge currents as high as 300A. The thyristors are available with voltage ratings of 500, 600, and 800V. The minimum gate current required to trigger the devices is 35 mA at 25°C, and the gate-controlled turn-on time is 2 μsec typ. The use of refined alloy-bonding techniques to mount the die inside the package contributes to the elimination of hot spots and improved thermal stability. Approximately $1.20 (10,000).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 373

Amperex Electronic Corp, George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500.

Circle No 374



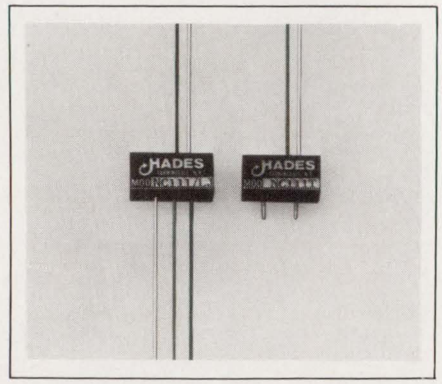
TOUCH DISPLAYS

- *Resolutions range from TV grade to fine*
- *Screen sizes to 19 in.*

The K7000 displays provide solutions to most interactive display requirements—graphics superimposed on video, high-quality RGB analog, NTSC, audio, etc. They employ proprietary Cyclops single-LED touch-screen technology. The displays are available in 13-, 15-, 18-, and 19-in. sizes and either as standard CRTs or as full-square, flat-faced tubes. The display resolutions range from TV grade (320×240 pixels) to fine (640×240 pixels). The built-in intelligent controller transmits X-Y data via an RS-232C interface. Custom sizes and configurations are available upon request. $700 to $800. Delivery, four to six weeks ARO.

Wells-Gardner Electronics Corp, 2701 N Kildare Ave, Chicago, IL 60639. Phone (312) 252-8220. TLX 253286.

Circle No 375



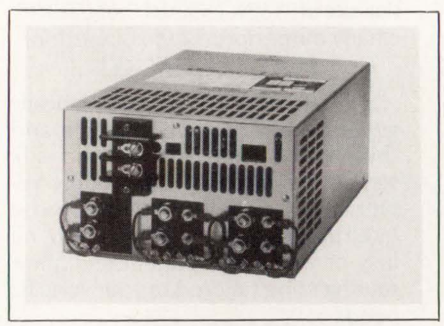
REFERENCE JUNCTION

- *Accuracy to within ±1°C*
- *Fully encapsulated package*

Model NC111 is a miniature, high-accuracy, half-bridge, cold-junction temperature-compensating network. Its compensation accuracy is within ±1°C over an ambient operating range of −54 to +100°C. A wide range of excitation voltages is available. The entire compensation network and the cold-junction thermocouples are encapsulated. The unit is available in pc-board-mountable versions or with leads. $27.20 (100).

Hades Manufacturing Corp, 151 Verdi St, Farmingdale, NY 11735. Phone (516) 249-4244.

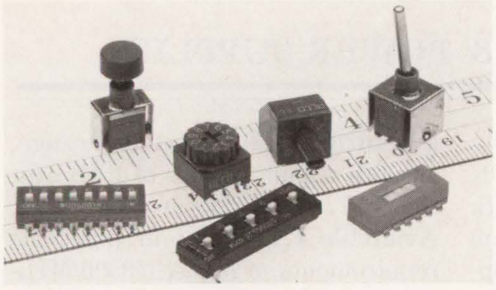
Circle No 376



SWITCHING SUPPLIES

- *Power outputs to 1750W*
- *80% standard efficiency*

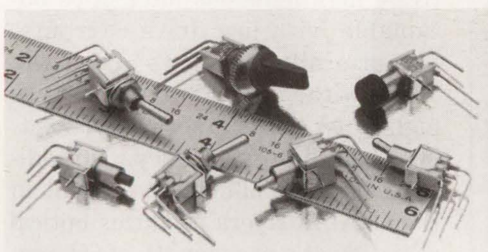
The seven units in the VF Series of 5-output switching power supplies offer outputs of 750, 1000, 1250, 1500, or 1750W. The standard output voltages are 5, 12, and 24V; 15, 18, and 48V units are available by



SURFACE MOUNT (SMD) SWITCHES

ALCOSWITCH has surface mount switches, consisting of: AD series DIP and AA/C, AR series DIP programming switches, sub-miniature toggle/push-button the SMT/P series switches, and the AS series auto-insertable slide switches. The DIP switches are available in 2 through 10 positions with optional integral pull up resistors or diodes. The SMT/P switches are in single or double-pole, while the AS slide switches are in one, two, four , or six-poll versions. All are molded from high temperature polymers, designed specifically to withstand vapor-phase or infra-red reflow soldering, and allow for aqueous or solvent cleaning. For more information Call (617) 685-4371, **ALCOSWITCH** 1551 Osgood Street, North Andover, MA 01845.

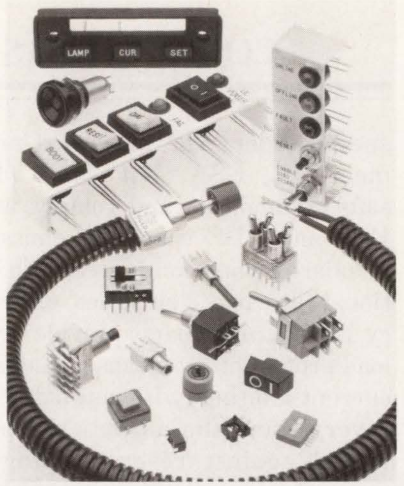
CIRCLE NO 45



"tiny" VRA TOGGLE AND PUSHBUTTON SWITCHES

ALCOSWITCH offers right angle & vertical right angle termination options for the extensive TT/TP Series subminiature "tiny" toggle and pushbutton switches. Intended for high density PC board layouts. The TT/TP-VRA options combine .3X .3X .2 case size with on-edge mounting. These features maximize switch space density, allowing the design engineer room for miniaturization or additional components. Rated at 0.4VA @ 20VDC maximum. For more information Call (617) 685-4371, **ALCOSWITCH**, 1551 Osgood Street, North Andover, MA 01845

CIRCLE NO 84



ADVERTISEMENT

CUSTOM SWITCHES

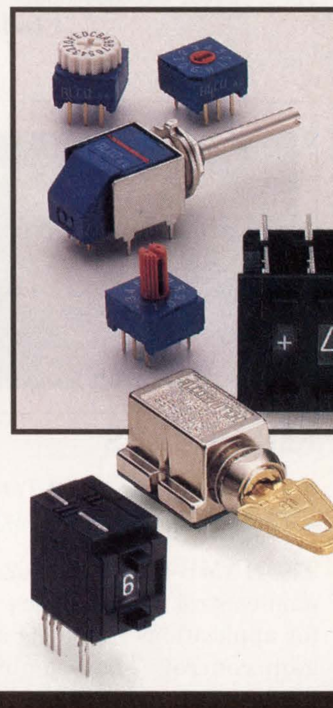
ALCOSWITCH has provided "Application Specific" switch designs to some of the industry's largest OEM's. From sub-miniature snap switches to large power rocker types, our engineers can custom design a switch to meet your unique switch application requirements. For more specific information on our custom design capabilities CALL TODAY, (617) 685-4371, **ALCOSWITCH** 1551 Osgood Street, North Andover, MA 01845.

CIRCLE NO 123

CODED SWITCHES

BCDiversity.

BCD—Better Coded Dependability.



Good reasons to switch:

Rotary DIPs
1. Four actuator styles.
2. Upright or right angle.
3. BCD and complement codes.
4. Hexidecimal and complement codes.
5. Permanently sealed for wave soldering and cleaning.

Pushwheels
1. Broadest line of codes and sizes.
2. Extended PC boards or PC terminals.
3. Panel mountable from front or rear.

Key Codes
1. Up to 31 different codes per switch.
2. PC or turret terminals.
3. Compact and pickproof.

For a catalog, applications help, free product samples, or a quotation, call or write ALCOSWITCH, 1551 Osgood Street, North Andover, MA 01845, (617) 685-4371. TWX: (710)342-0552. FAX: (617) 686-9545.

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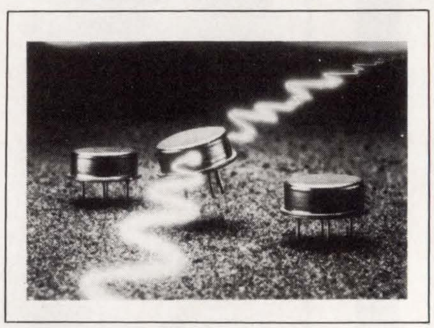
Quality and Innovation

CIRCLE NO 162

special order. The fan-cooled units meet UL, CSA, IEC, and VDE safety standards and comply with FCC and VDE conducted-emission standards when configured with optional filtering. The series' efficiency is 80%. All models provide overload protection by means of foldback current limiting (with automatic recovery), and the outputs are protected against reverse voltages. Overvoltage protection is standard on the main output and optional on other outputs. The supplies have a soft-start feature to protect critical components. Other protection options include line-monitor, logic-inhibit, and thermal-shutdown functions. Output margining is also available. $515 to $875 (OEM qty). Delivery, four to eight weeks ARO.

Deltron Inc, Box 1369, North Wales, PA 19454. Phone (215) 699-9261. TWX 510-661-8061.

Circle No 377



AMPLIFIERS

- *Housed in standard TO-8 cans*
- *Gain flatness to 1600 MHz*

The HAMP-4001 and -4002 variable-gain-control amplifiers are intended for applications requiring automatic gain control. They combine PIN-diode and microwave-transistor technologies in a circuit packaged in a standard TO-8 can. The HAMP-4001 provides a 22-dB gain, 30-dB gain control, and gain flatness over a 2- to 1250-MHz range. Response characteristics are maintained over both the gain-control range and the −55 to +85°C operating range. The HAMP-4002 provides a 17-dB gain and a 29-dB gain control, and it has a 2- to 1600-MHz frequency range, all with a gain flatness of 1 dB over the −55 to +85°C operating range. Available TXV versions meet the requirements of MIL-S-19500/MIL-STD-883. HAMP-4001, $100; HAMP-4002, $115 (100).

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 378

GaAlAs LEDS

- *Produce 200 mcd from 10-mA drive currents*
- *Maintain long lifetimes with drive currents as high as 1A*

This family of red GaAlAs LEDs includes versions with luminous intensities as high as 200 mcd for a drive current of 10 mA. A novel chip-passivation technique allows the devices' GaAlAs layers to contain a high level of aluminum. The resulting high electron-injection efficiency not only provides the relatively high luminous intensities obtainable with low drive currents, but also allows you to drive the LEDs with dc or pulsed currents as high as 1A without seriously affecting their life expectancy. In addition, the high aluminum content in the GaAlAs layers produces optical radiation at a wavelength of 650 nm. The human eye is more sensitive to this wavelength than to the 660- to 670-nm wavelengths typical of standard red LEDs. Approximately Gld 0.225 to Gld 0.275 (OEM qty).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 379

Dialight Corp, 203 Harrison Place, Brooklyn, NY 11237. Phone (718) 497-7600.

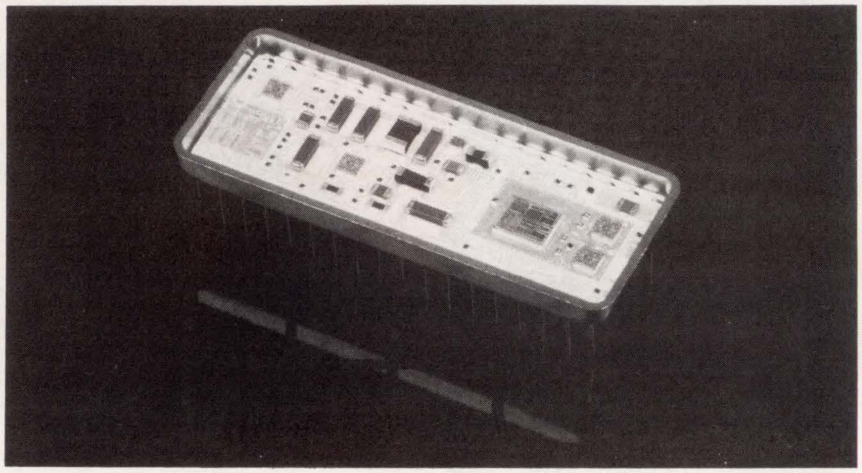
Circle No 380

NEW PRODUCTS

INTEGRATED CIRCUITS

S/D CONVERTER

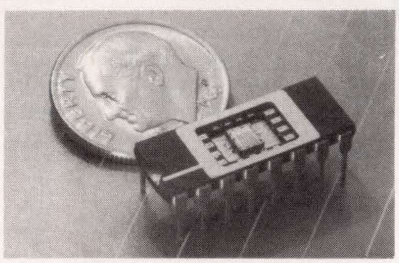
- *Operates from a 5V supply*
- *Tracks at 7200°/sec*



The HSRD1056 synchro-to-digital converter provides 16-bit resolution, 7200°/sec tracking, and 1.3-arc-minute accuracy when operating from a 5V supply. The power dissipation is 50 mW. The converter includes 3-state outputs configured as two 8-bit bytes, a μP interface, a circuit that prevents false lockup when subjected to a step input of 180°, and a reference-synthesizer circuit that reduces the effect of speed voltages at high rotational speeds. The outputs have a test bit that reads a logic one when the tracking error exceeds 1°, and a high-quality analog velocity signal that allows you to eliminate the mechanical tachometer in many applications. The package is a 36-pin double-width DIP. From $560. Delivery, six to eight weeks ARO.

Natel Engineering Co Inc, 4550 Runway St, Simi Valley, CA 93063. Phone (805) 581-3950. TWX 910-494-1959.

Circle No 381



D/A CONVERTER

- *Settles in 20 nsec*
- *Draws 25 mA from a 5V supply*

Fabricated with silicon-on-sapphire (SOS) technology, the 8-bit CA3338 D/A converter offers 1- and ¾-LSB max error figures for integral and differential linearity, respectively. The CA3338A version offers ¾- and ½-LSB errors for the same respective linearity specs. This CMOS converter operates at update rates as high as 50 MHz, settles in 20 nsec, and draws only 25 mA (during 10-MHz operation) from its 5V supply. It achieves low-glitch energy by processing the three most significant bits with a bar-graph decoder. It comes with TTL- or CMOS-compatible digital inputs, which are similar to the input circuitry of the company's HCT CMOS logic. Packages include 16-pin plastic and ceramic DIPs. From $6 (1000).

GE/RCA, Solid State Div, Box 2900, Somerville, NJ 08876. Phone (201) 685-6994.

INQUIRE DIRECT

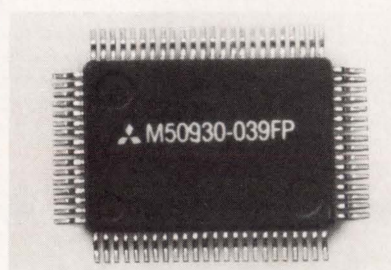
ANALOG SWITCH

- *70-dB off isolation at 10 MHz*
- *±10V analog-input range*

The CDG201B is a quad-spst analog switch with TTL-compatible control inputs. Pin- and function-compatible with industry-standard DG201 switches, the monolithic device combines CMOS and DMOS (double-diffused MOS) technology. The switches offer a wide bandwidth, with less than 1-dB rolloff at 100 MHz. The off isolation is 70 dB at 10 MHz, 40 dB at 100 MHz. The analog input range is ±10V using ±15V supplies. Chips are available in die form or housed in 16-pin DIPs. Industrial version, $2.45 (100). Delivery, six weeks ARO.

Topaz Semiconductor, 1971 N Capitol Ave, San Jose, CA 95132. Phone (408) 942-9100. TWX 910-338-0025.

Circle No 383



MICROCONTROLLERS

- *Feature onboard LCD drivers*
- *3V battery backup*

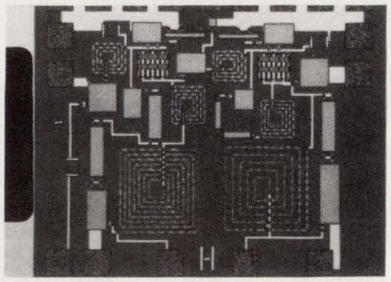
The M50930FP, M50931FP, and M50932FP monolithic, 8-bit CMOS microcontrollers can drive as many as 128 LCD segments. Low-power, 3V battery-backup operation renders the μCs suitable for portable


CASIO
SCIENTIFIC CALCULATOR
fx-4000P

applications. Each µC can operate in the µP, memory-expansion, single-chip, or evaluation modes. Instruction sets are upwardly compatible with that of the 6502 µP; the new devices offer augmented addressing modes and 13 additional instructions. The µCs offer 4k to 8k bytes of ROM and 128 to 512 bytes of RAM. Other features include five 8-bit timers (four when you use serial I/O), one 16-bit timer, a UART, and a 2-µsec min execution time for instructions. Development tools include in-circuit emulator boards, debugging systems, piggyback evaluation chips, and software that runs on the IBM PC, PC/XT, and PC/AT, and on CP/M-based systems. From $6.25 (5000). Delivery, six to eight weeks after ROM code is installed.

Mitsubishi Electronics America Inc, Semiconductor Div, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 384



GaAs AMPLIFIER

- *Operates from 2 to 6 GHz*
- *Provides 9.5-dB gain and 14.5-dBm output power*

The AWA20601 is a wideband GaAs MMIC (monolithic microwave IC) amplifier suitable for use in broadband electronics-countermeasures (ECM) and telecommunications systems. It operates at 2 to 6 GHz and provides 9.5-dB gain and 14.5-dBm output power. The device is available in an 8-pin flatpack or in die form for hybrid applications. It includes all necessary bias circuitry and operates from a single supply voltage. Input and output RF ports feature 50Ω matching; VSWR is better than 2:1. High reverse isolation lets you cascade the amplifiers. Packaged AWA20601 amplifiers, $76; in die form, $59 (100). AWA20601TFF evaluation kit, including 10 amplifiers, $1000; AWA-20601UTF dc to 26.5-GHz universal test fixture, including 10-amplifier die with carriers, $3150. Delivery for the kits, 30 to 90 days ARO.

Anadigics Inc, 35 Technology Dr, Warren, NJ 07060. Phone (201) 668-5000. TWX 510-600-5741.

Circle No 385

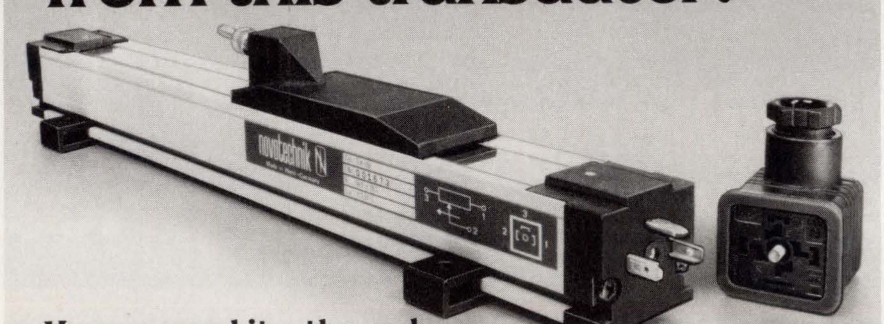
COPROCESSOR

- *Object-code compatible with earlier coprocessors*
- *Operation is transparent to application software*

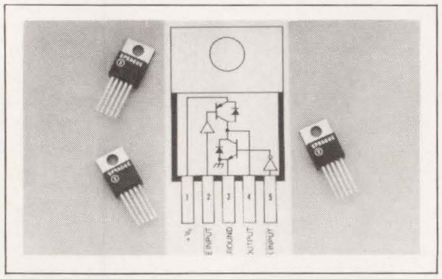
The 32-bit 80387, a numerics coprocessor for microcomputers based on the 80386 µP, is object-code compatible with the earlier 8087 and 80287 coprocessors. Optimized for floating-point operation with the 80386 µP, the 80387 enhances the 80386 by adding instructions for trigonometric, logarithmic, exponential, and arithmetic operations. The 80386 assembler and high-level-language compilers support the new instructions and data types, so special programming tools are not required. Communication between the 80386 and the 80387 is transparent to the application software, because the CPU controls the 80387 automatically. The computational, constant, and transcendental instructions are IEEE-compatible. These instructions simplify code development for solids modeling, mechanical simulation, robot control, and scientific analysis. The package is a 68-pin ceramic pin-grid array. $500 (100).

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone (408) 496-4580.

Circle No 386




SYVERSON



MOTOR DRIVER

- *Operates at 24V; delivers 1A*
- *Includes protection circuitry*

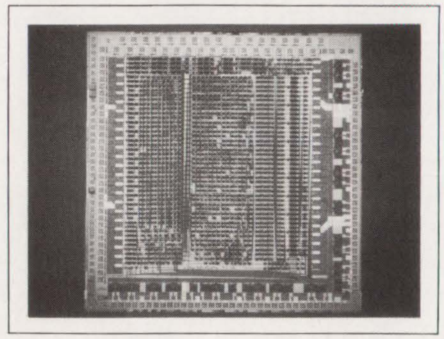
The UDN-2943Z is a half-bridge motor driver with extensive protection circuitry. The 24V/1A device drives dc servo motors. You can also use the driver in pairs for full-bridge applications, or as triplets for 3-phase brushless dc motors. On-chip safeguards include thermal and overvoltage shutdown, cross-over-current protection by means of an internally generated dead time, and short-circuit protection (when the source driver is shorted to ground). Input-logic lockout, which prevents the source and sink drivers from turning on simultaneously, and transient suppression are other safeguards. The pulse-width-modulated driver features saturated outputs, which minimize power consumption. The device comes in a modified 5-lead, power-tab TO-220 plastic package. $1.35 (100). Delivery, 10 to 12 weeks ARO.

Sprague Electric Co, Box 9102, Mansfield, MA 02048. Phone (617) 853-5000.

Circle No 387

16×16-BIT MAC

- *Multiply-accumulate time is 11 nsec*
- *Dissipates 5.5W typ*

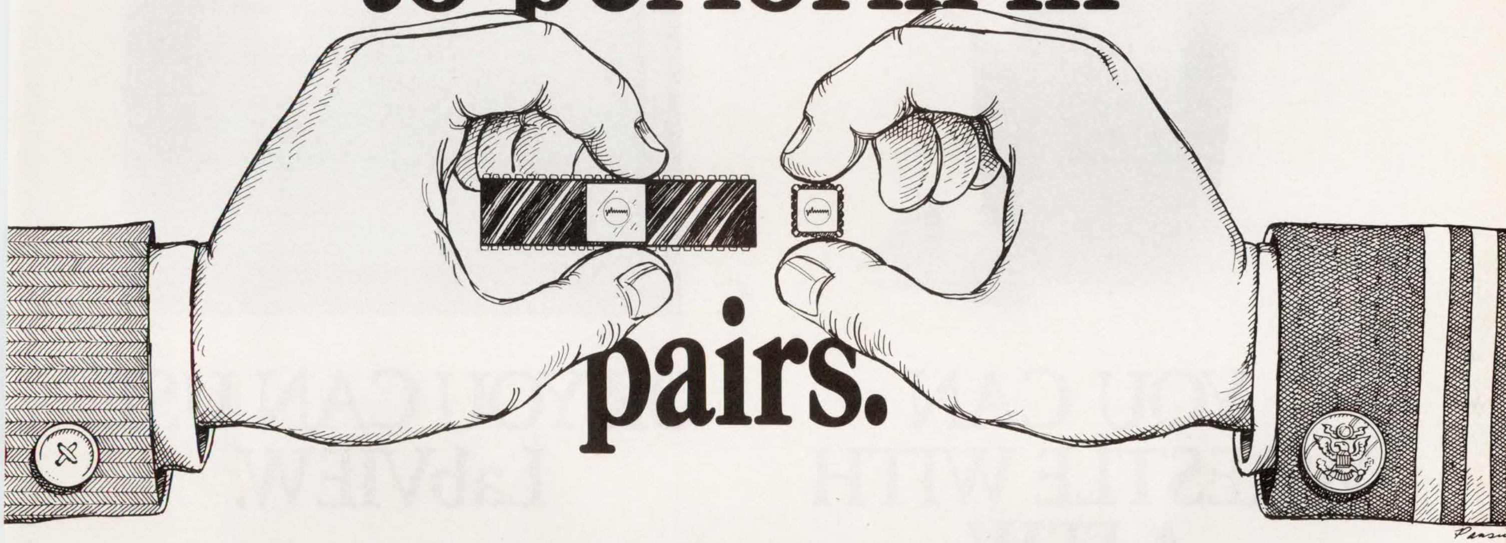


Based on the company's high-density bipolar VLSI process, the B3011 fixed-point multiplier-accumulator (MAC) provides an 11-nsec typ multiply-accumulate time for 16-bit inputs. This ECL-compatible chip is the industry's fastest, according to the manufacturer. The typical power dissipation is 5.5W. The chip's 40-bit accumulator, useful for complex-number and double-precision computations, has dual input registers and a 40-bit output. The package is a 132-pin pin-grid array. Commercial grade, $340 (100).

Bipolar Integrated Technology, 1050 NW Compton Dr, Beaverton, OR 97006. Phone (503) 629-5490.

Circle No 388

Only Plessey designs 8-bit, 110MHz ADCs and driver amps to perform in



pairs.

Only Plessey Semiconductors has both an 8-bit flash ADC with a guaranteed 110MHz conversion rate, and a companion amplifier with a unity gain bandwidth of 400MHz. Together, they can solve your data conversion problems in a lot less space using fewer components.

The SP97508 converter has accuracy better than ±0.5 LSB and features a full Nyquist analog bandwidth. Typical power dissipation is a low 1.2W, and it requires only a single −5.2V supply.

Equally impressive is the SL9999 amplifier. It gives you three times the performance of equivalent gallium arsenide devices, and features adjustable open loop gain and output current (±50mA) with a gain-bandwidth of 2GHz at 20dB. Typical slew rate is 1300V/μSec.

Both devices are available to MIL SPEC 833C. And they're part of a complete family of ADCs, DACs and other support circuits.

Let Plessey show you the answer to your data conversion problems. Call customer service in Swindon (0793) 726666. Fax: (0793) 726666 Ext. 250. After-hours Fax: (0793) 729412. Tx: 444410.

In the United States, call (800) 321-0871 or (714) 472-0303. Telex 701464. Fax: (714) 770-0627.

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	SP9756	6-bit 110 MHz
ADC Driver	SL9999	Driver amp.
Comparators	SP9680/5/7	2.2 nsec family
Support	SL9210	8-bit latches
DAC's	SP9768	8-bit 150 MHz
	SP9770	10-bit 75 MHz
	SP97618	8-bit 250 MHz graphics

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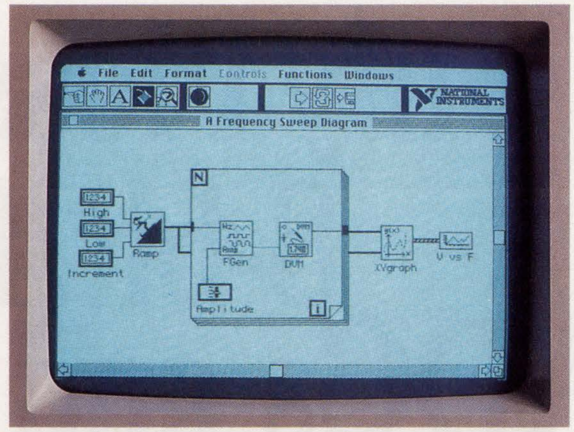
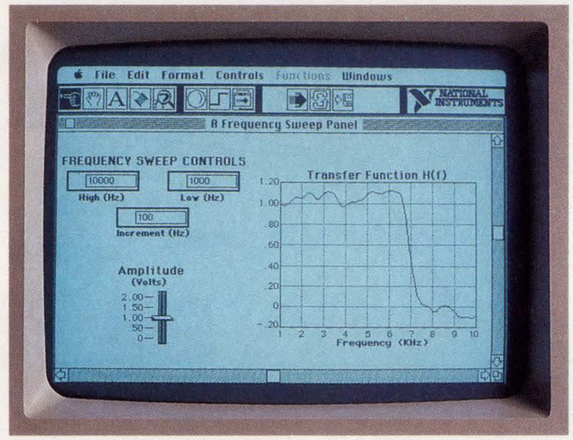
CIRCLE NO 190





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CIRCLE NO 191

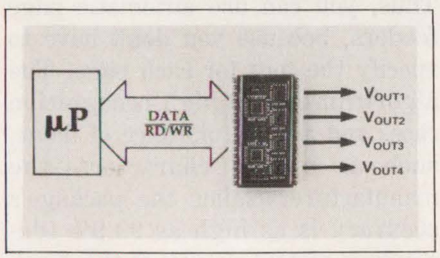
D/A CONVERTER

- *8-bit CMOS device dissipates 400 mW*
- *Resolution of more than 1280×1024 pixels*

The IDT75C18/28, an 8-bit, CMOS video D/A converter, can directly drive a 75Ω load at standard video levels with a resolution exceeding 1280×1024 pixels. It dissipates 400 mW. The device requires no additional registering, buffering, or deglitching for most applications. The IDT75C28 is TTL compatible, and the ECL-compatible IDT75C18 is pin compatible with the TRW TDC1018. Voltage levels at the IDT75C18's outputs conform to the RS-170 and RS-343 monitor standards; this feature simplifies connection to a graphics CRT. The device includes four inputs that control synchronization, blanking, intensified video, and all-white display. Packages include a 24-pin hermetic DIP, a 28-pin leaded chip carrier, and a 24-pin, 0.3-in. plastic DIP. Commercial-grade device in a ceramic DIP, $27.50 (100).

Integrated Device Technology Inc, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. TWX 910-338-2070.

Circle No 389



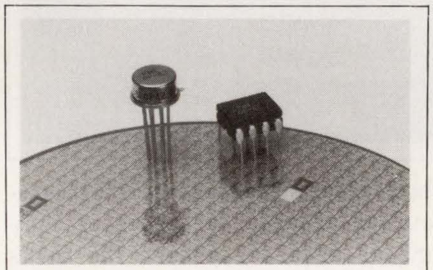
QUAD D/A CONVERTER

- *Performs read-back checks*
- *40-nsec bus-access time*

The AD392 quad 12-bit D/A converter offers a bus-access time of 40 nsec. It also features read-back checks, which let the μP verify that the data latched in the converter's registers is the same as that sent from the μP. The hybrid device includes control logic, registers, latches, and four voltage-output D/A converters. The power requirement is ±15V; the dissipation is 1.3W typ. The maximum integral- and differential-linearity errors are ±½ and ±1 LSB, respectively. An autozero function sets all converters to zero by addressing a single pin. The device comes in a 32-lead ceramic DIP. From $99 (100).

Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577. TLX 174059.

Circle No 390



HIGH-SPEED OP AMP

- *50V/μsec slew rate*
- *Settles to within 0.01% in 1 μsec*

The OP-42 op amp offers unity-gain stability and a symmetrical 50V/μsec min slew rate. The gain-bandwidth product is typically 10 MHz, and the 1-μsec settling time (to within ±0.01%) is guaranteed by an automated production-test system. Other specs include a 500k min open-loop gain into a 10-kΩ load (200k gain into a 2-kΩ load); an 88-dB min CMR; a 750-μV input-offset voltage; and an offset-voltage drift of 10-μV/°C. Input bias current is 200 pA max at 25°C. The op amp is available in an 8-pin ceramic miniature DIP, an 8-lead TO-99 can, and, for the industrial and military temperature ranges, a 20-lead ceramic leadless chip carrier. From $3.75 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218. TLX 172070.

Circle No 391

MOTION CONTROL

- *Lets you develop and test motion-control software on a PC*
- *Accepts input from command files as well as from keyboard*

The Max software package, which runs on an IBM PC or compatible machine, lets you develop and test motion-control software for process-control systems that use ac-brushless or dc-servomotor technology. You can use either the functions built into the software or the commands of the vendor's motion-programming language (MPL) to establish communications with individual motors or to monitor the performance of the process-control system. Certain Max functions can report the current system status (for example, the system position, system velocity, or condition of system inputs) or the current system configuration (for example, jog speed, index distance, or acceleration profile). Other functions display motion-control command files stored on your disk, let you find or change communications parameters, and let you execute PC-DOS commands while Max is running. You can enter commands directly from the keyboard or cause the program to execute a complex sequence of commands from a command file that's stored on disk. $249.

Ormec Systems Corp, 19 Linden Park, Rochester, NY 14625. Phone (716) 385-3520.

Circle No 392

CAE SYSTEM

- *Facilitates surface-mounting and double-sided placement*
- *Features multitasking and multiwindowing*

The Scicards system, an interactive software package for the design of pc boards and thick-film hybrid microcircuits, accepts schematic data from a CAE interface or from the vendor's Schemactive schematic-capture program. It assists you in component placement and routing; you can use automatic or manual placement strategies or a combination of both. The Scicards and Schemactive programs share a common database, so that changes and corrections made during layout automatically modify the schematic drawings. An audit file maintains a history of your work and allows you to go back through the file to remove steps that produced errors. The package runs under VAX/VMS on a VAXstation II/GPX enhanced with the vendor's Dragon graphics chip set, which accelerates graphics processing. $25,000.

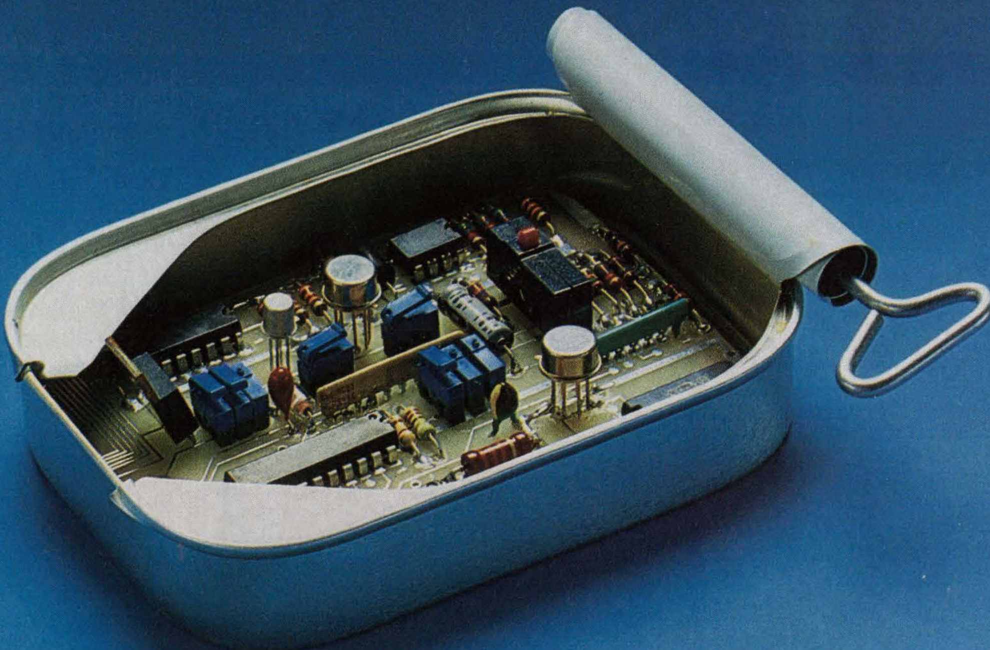
Scientific Calculations Inc, 7635 Main St, Fishers, NY 14453. Phone (800) 828-6552; in NY, (716) 924-9303.

Circle No 393

OCR SOFTWARE

- *Algorithms yield tolerance of flaws*
- *Reads at 600 wpm on a 6-MHz IBM PC/AT*

ReadRight is an optical character-recognition software package that operates with the vendor's Turbo-Scan optical page scanner. The software uses topological algorithms that allow it to read a large selection of font styles in sizes from 6 to 12 points, a pitch of 10 to 15 cpi, and a maximum line spacing of 8 lpi. The program can read reduced and enlarged photocopies, and you can mix fonts within a word, line, or page. Thus, you can use automatic page feeders, because you don't have to specify the font for each page. The algorithms yield high recognition rates and a high tolerance of flaws, such as broken characters—the manufacturer claims the package's accuracy is as high as 99.9% (depending on the quality of the document) at reading speeds as great as 600 wpm on a 6-MHz IBM PC/AT. The program converts scanned text to ASCII files that are compatible with most word processors, and it converts scanned images to binary code for processing by the computer. It uses data compression and DMA transfer of scanned data to achieve a maximum scanning time of 9.9 sec for an 8½×11-in. document.



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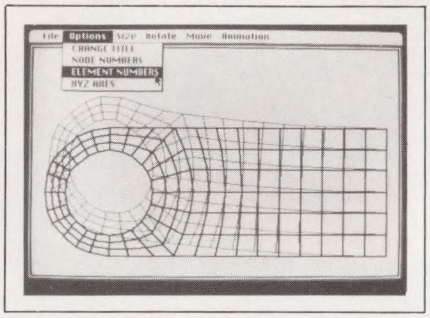
CIRCLE NO 192

To run the program you need an IBM PC/AT or a compatible computer equipped with at least 512k bytes of RAM. $695.

AST Research Inc, 2121 Alton Ave, Irvine, CA 92714. Phone (714) 863-1333.

Circle No 394



MECHANICAL CAE

- *Performs static and dynamic finite-element analysis*
- *Runs on Macintosh*

MSC/pal performs both static and dynamic finite-element analysis on the Apple Macintosh. The package is similar to the vendor's IBM PC-based product, but provides pull-down menus and dialogue boxes. Using it, you can break a structure or mechanical component into a number of discrete elements that the software then analyzes for tolerance to stress, vibration, pressure, and temperature. The program's element library includes beams, triangular and quadrilateral plates, plane-stress and plane-strain membranes, scaler springs, masses, dampers, and generalized mass and stiffness matrices. Its interactive graphics features include 3-D wireframe plotting, scaling, and rotating, as well as X-Y plotting for element-stress scanning and dynamic response. 300-node version for a 512k-byte Macintosh, $995; 500-node version for a 1M-byte Macintosh, $1495.

MacNeal-Schwendler Corp, 815 Colorado Blvd, Los Angeles, CA 90041. Phone (213) 258-9111. TLX 4720462.

Circle No 395

CASE ON VAX

- *Structured-analysis and -design tools*
- *Network users share common data dictionary*

Teamwork structured-analysis and -design tools, formerly available only for Apollo's Domain workstations, are now available for DEC's VAX/VMS machines in the 700, 8000, and MicroVAX II series. Teamwork/SA is a structured-analysis tool that uses the Yourdon-DeMarco techniques and data-flow diagrams to analyze system requirements and the flow of data through a system. The program performs consistency checks among the data dictionary, the mini-specifications, and all levels of the data-flow diagrams. Teamwork/RT provides the same facilities, but also lets you model the sequence, timing, and control aspects of real-time systems. Teamwork/SD lets you capture the module and subroutine details that are required during the coding phase. Teamwork/Access lets you access the Teamwork database of a project and extract any data for use by other tools, including document-production systems. One-time fee for installation of the database, $5500; Teamwork/SA, -RT, and -SD, $8900 each; Teamwork/SA plus -RT or -SD, $12,500.

Cadre Technologies Inc, 222 Richmond St, Providence, RI 02903. Phone (401) 351-5950.

Circle No 396

ACCELERATOR

- *Evaluates as many as 128,000 gates*
- *Speeds software simulation*

PerSim is a hardware-software coprocessor contained on a board that uses the IBM PC/AT bus and plugs into an Apollo DN3000 workstation. The coprocessor consists of a proprietary RISC (reduced-instruction-set computer) that accelerates the execution of the vendor's Logic- and

Fault-Simulation design tools. Two models are available: Model I can simulate as many as 64,000 gates and perform 1 million gate evaluations per second. Model II can simulate as many as 128,000 gates and perform 2.5 million gate evaluations per second. According to the vendor, comparable products from other sources cost $120,000 or more. Model I, $7500; Model II, $20,000.

Aida Corp, 3375 Scott Blvd, Suite 342, Santa Clara, CA 95054. Phone (408) 748-8571.

Circle No 397

ACQUISITION SOFTWARE

- *Collects digital and analog data from as many as 600 sources*
- *Can analyze data and issue alarms*

The Impulse software package, which runs on the IBM PC, PC/XT, PC/AT, or a compatible computer, accepts real-time analog or digital data from the vendor's Imp measurement pods. Each pod accepts signals from as many as 20 analog or digital channels, and each is sealed in a NEMA 4X enclosure for use in hostile environments. You can connect as many as 30 pods to a host IBM PC over the proprietary 2-wire serial bus, which has a data rate of 163k bits/sec; the cable can be as long as 1 km. The software can collect real-time data from current and voltage sensors, thermocouples, strain gauges, frequency counters, event counters, interval timers, and other measuring devices. You can apply linear conversions to all inputs in order to obtain results specified in engineering units. An 8-channel spreadsheet feature displays results in real time and allows immediate access to any channel in the system. You can store the incoming data in as many as 10 independent disk files. A field-installable graphics/alarm option lets you display trends and bar graphs and can initiate alarms if data from critical channels falls outside previously specified upper and lower limits. A communications option allows you to acquire data in the background while running other programs or DOS functions in the foreground, as well as providing bidirectional data transfers between the host PC and another computer. Impulse, $1495; graphics/alarm option, $1000; communications option, $1200.

Solartron Instruments, 2 Westchester Plaza, Elmsford, NY 10523. Phone (914) 592-9168.

Circle No 398

EXPERT-SYSTEM SHELL

- *Rule-based, extended inference mechanism*
- *Interfaces external files and telecommunication links*

Xi Plus is an expert-systems shell that runs on the IBM PC/AT and compatibles. It allows you to develop an expert system by collecting knowledge on a particular topic and integrating it in a knowledge base in a form that the inference mechanism can use. The inference mechanism is rule-based, and it uses both forward- and backward-chaining procedures. The program also provides interfaces to external files, graphics systems, and telecommunications links. In constructing the rules for the expert system under development, the program uses menus extensively to prompt the user for information. It accepts replies in conversational English, issuing further prompts as necessary to clarify these replies for the inference mechanism. You can use this tool to construct expert systems having as many as 1200 rules. $1250.

Expertech, 650 Blair Island Rd, Suite 204, Redwood City, CA 94063. Phone (415) 367-6293.

Circle No 399

PASCAL FOR PDOS

- *Single-pass compiler generates relocatable code for 68000*
- *Provides extensions for industrial-control software*

OmegaSoft Pascal, originally introduced for the Motorola 6809 μP, is now available in a version that runs under the PDOS operating system on Motorola's 68000 and 68020 processors. The fast, 1-pass compiler generates relocatable code that is ready for linking and can run under the host operating system or on a different target machine. The compiler conforms to the ISO (International Organization for Standardization) level 0 standard and has extensions that facilitate the development of process-control and other real-time applications. If a 68881 numeric coprocessor is present in the system, the compiler will generate code that makes use of it. The complete package includes an assembler, a linker, a debugger, a screen editor, a Pascal shell, and the source code of the run-time library. $900.

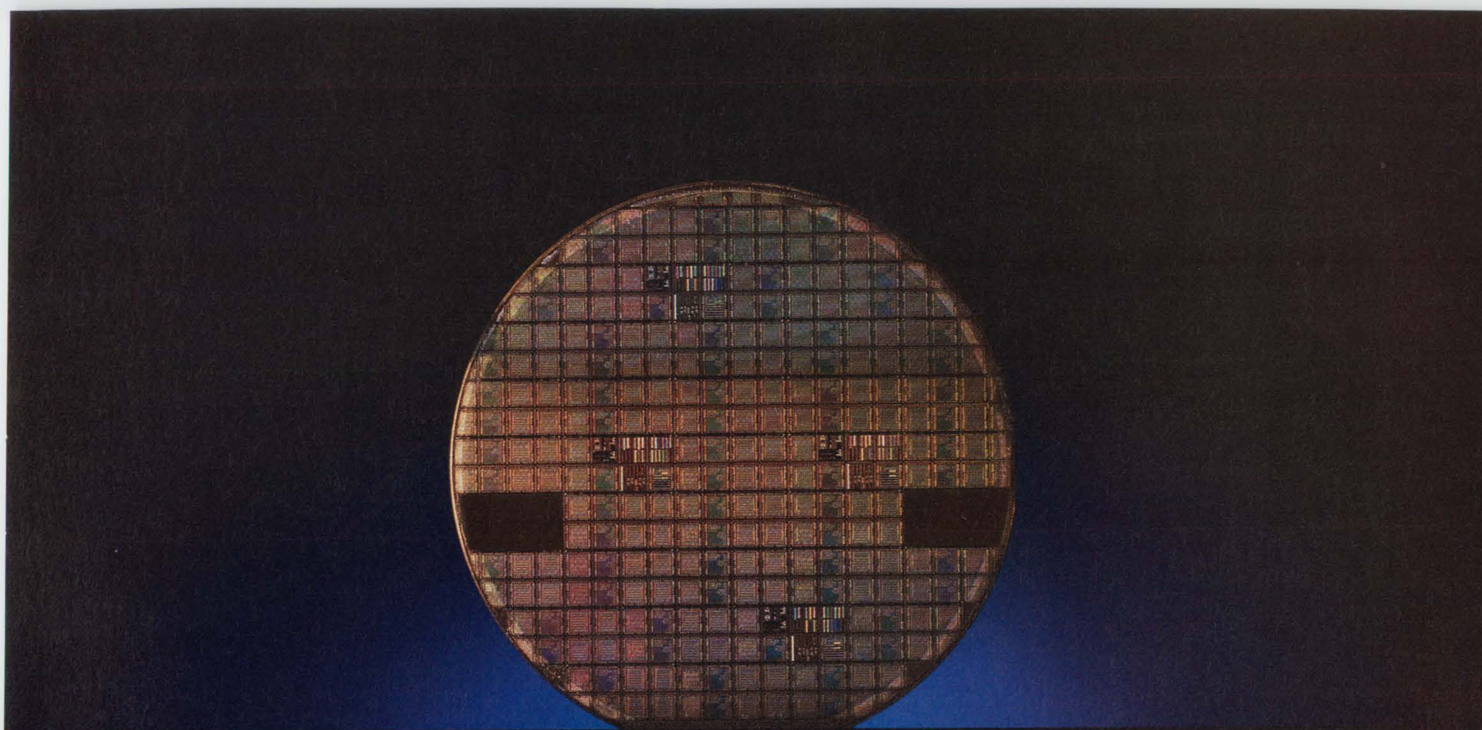
Certified Software Corp, 616 Camino Caballo, Nipomo, CA 93444. Phone (805) 929-1395.

Circle No 400

TERMINAL EMULATOR

- *Lets an IBM PC emulate a graphics terminal*
- *Features Kermit and Xmodem file-transfer protocols*

The Graphics 4000 is a software package that allows an IBM PC,



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CIRCLE NO 194

PC/AT, or compatible computer to emulate all the functions of Tektronix 4105, 4010/4014, and DEC VT100 color and monochrome graphics terminals. The software is compatible with the IBM EGA (enhanced graphics adapter) and CGA (color graphics adapter) cards, as well as with Hercules adapters. You can also use the built-in ADI-Autocad driver with most color-graphics boards. The package accepts input from a mouse or a graphics tablet and provides output in a format acceptable to most popular color and monochrome graphics printers. The package also lets you use either the Kermit or the Xmodem error-detection protocol to transfer files from the PC to another computer. To run the emulator software, you need an IBM PC or a compatible computer equipped with at least 256k bytes of RAM and a graphics-adapter board. $199.

Ultratek, 23520 Telo St, Suite 12, Torrance, CA 90505. Phone (213) 534-8244.

Circle No 401

PROGRAM TIMING

- *Lets you measure program-execution time in μsec*
- *Separate values for primary program and system functions*

Stopwatch is a memory-resident utility that runs on the IBM PC or a compatible computer and lets you measure program-execution times with a resolution of 1 μsec. The program's measurements use the standard IBM PC-family video clock; thus, the PC is not dependent on the type of processor or the system clock rate. You can request the program to report the total execution time of the program under test. Alternatively, the program can break this total into the separate subtotals attributable to the program under test, to disk access, and to the BIOS or other PC-DOS functions. You can use the program in conjunction with debuggers such as Debug, Symdeb, or Codeview to measure the execution time from a Go command to a breakpoint. The distribution disk includes sample Basic, dBASE, Lotus 1-2-3, C, and assembly-language programs that demonstrate the use of Stopwatch. $59.95.

Custom Real-Time Software, Box 1106, West Caldwell, NJ 07007. Phone (201) 228-7623.

Circle No 402

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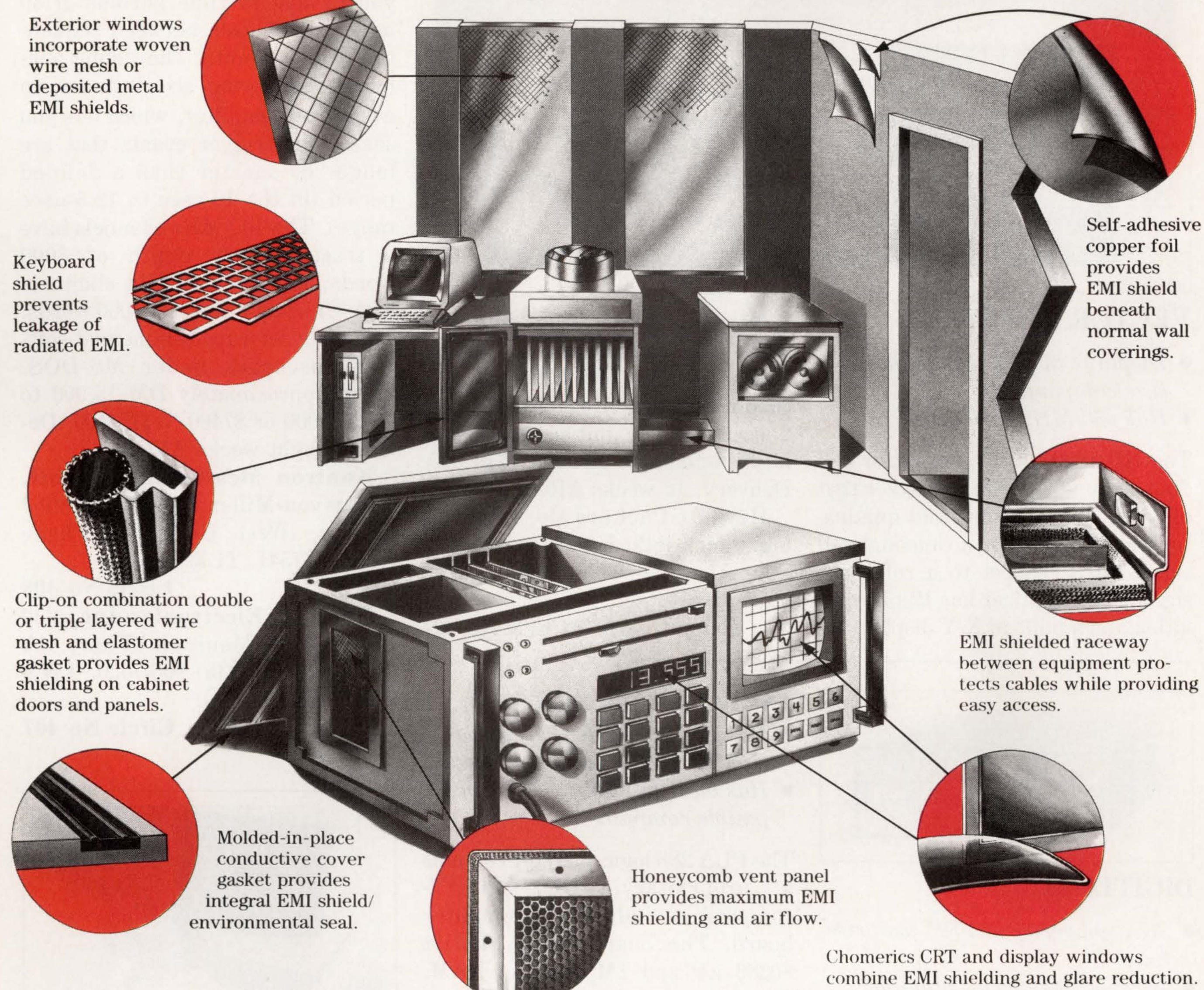

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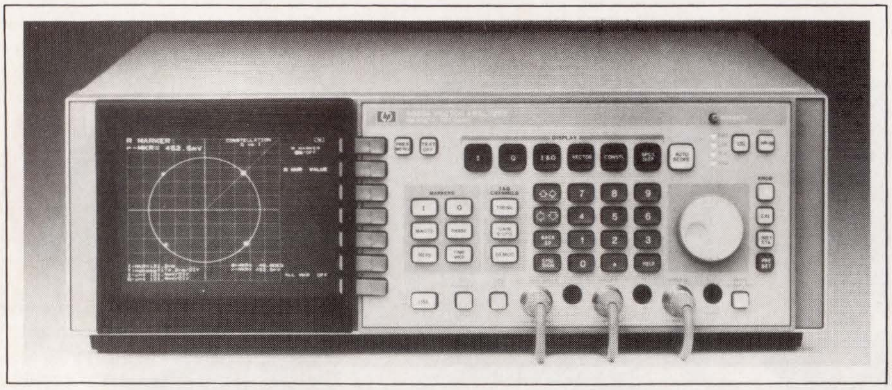


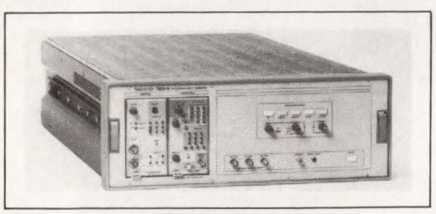
VECTOR ANALYZER

- *Displays in-phase and quadrature components*
- *Has 350-MHz bandwidth*

The HP 8980A vector analyzer is a dual-channel sampling analyzer that displays the in-phase and quadrature components of a demodulated signal with respect to a reference signal. The digitizer has 12-bit resolution and a built-in X/Y display. Its bandwidth ranges from dc to 350 MHz. The input sensitivity ranges from 5 mV/div to 1V/div, and the timebase ranges from 0.5 nsec/div to 2 msec/div. The unit accepts 50Ω or high-impedance probes. $19,000. Delivery, 12 weeks ARO.

Hewlett-Packard Co, Inquiries Manager, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 404



DIGITIZER

- *Scan converter has 525-psec rise time*
- *Accepts 7000 Series plug-ins*

The 7912HB scan-converter digitizer has 9-bit vertical resolution and 10-psec time resolution; its rise time is 525 psec. The unit accepts the maker's 7000 Series plug-ins for vertical amplifiers and timebases. You can program it over the IEEE-488 bus, and it can transfer 20 of its 512-sample waveforms per second over the IEEE-488 bus. $30,025.

Tektronix Inc, Box 1700, Beaverton, OR 97075. Phone (800) 547-1512; in OR, (800) 542-1877.

Circle No 405

LOGIC ANALYZER

- *Includes 100-MHz timing and 20-MHz state/timing analyzers*
- *Has built-in IBM PC/AT-compatible computer*

The PLA 286 logic analyzer contains a proprietary, IBM PC/AT-compatible industrial computer board. The board has a 10-MHz 80286 μP and 1M bytes of RAM. The instrument has a 3½-in. floppy-disk drive; a 3½-in. hard-disk drive is optional. The mother board has four slots for logic-analyzer boards and a fifth for other IBM PC boards. The vendor offers two logic-analyzer cards: the 4820, which has 48 20-MHz state/timing channels, and the 8100, which has eight 100-MHz timing channels. You can install a maximum of two 4820 and two 8100 boards, and you can use the full complement of timing and state channels together. The timing analyzer's triggering facilities include a window trigger mode, which allows you to specify time periods of 30 nsec to 12.5 μsec between sequential trigger events. The timing analyzer's triggering also includes an event-duration filter, which lets you search for trigger events that are longer or shorter than a defined period (in the 10-nsec to 12.5-μsec range). The 100-MHz channels have a trace-memory depth of 8000 words, and the 20-MHz channels have a memory depth of 4000 words. The analyzer runs commercial software packages under MS-DOS. From approximately DM 15,000 to DM 31,000 or $7400 to $15,400. Delivery, eight weeks ARO.

Kontron Messtechnik GmbH, Oskar-von-Miller-Strasse 1, 8057 Eching, West Germany. Phone (08165) 77541. TLX 526719.

Circle No 406

Kontron Electronics Inc, 630 Clyde Ave, Mountain View, CA 94039. Phone (415) 965-7020. TWX 910-378-5207.

Circle No 407

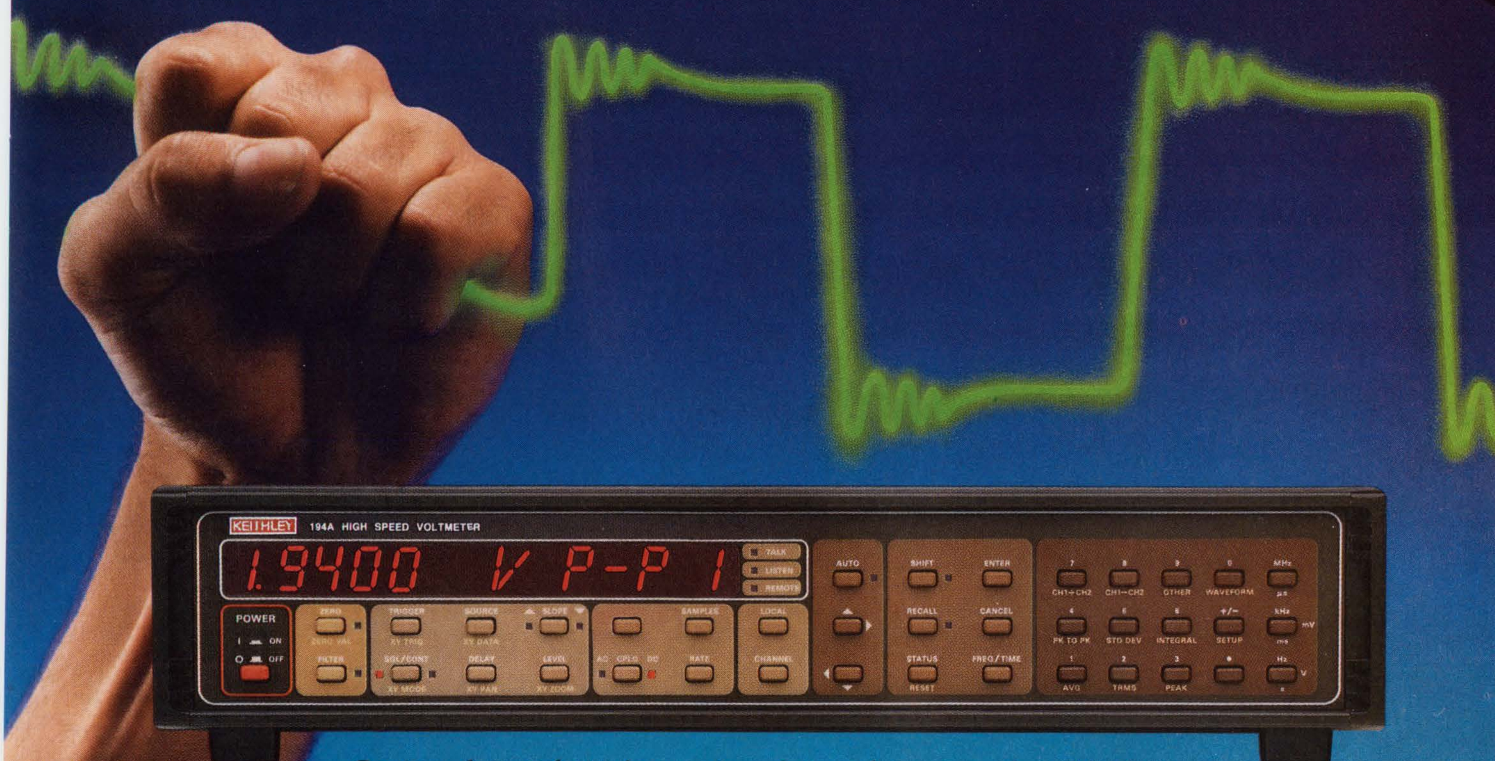
THERMOMETER BRIDGE

- *Measures PRT resistance with primary standards lab accuracy*
- *Includes an IEEE-488 control interface*

For use in primary standards labs, the Senator automatic thermometer bridge measures the resistance of platinum resistance thermometers (PRTs). The bridge has 1000, 100, and 10Ω ranges; the maximum resolution on the 10Ω range is 1 μΩ. The

NEW CAPABILITIES

CAPTURE IT



Capture data at fast trigger rates—internal or external—with the new Model 194A High Resolution Digitizer. Here are the advantages:

Faster, More Thorough Testing.

NOW—With the Model 194A High Speed Digitizer, you can acquire samples with external trigger pulses. Capture discrete samples synchronized to changes in position, distance, angle, log (time), a stimulus level, or other events. With trigger rates up to 1MHz, you can take more data in less time. That means more complete testing at lower cost.

Resolution of 16 bits. At rates up to 100kHz.

The Model 194A's 16-bit (4½-digit) resolution lets you detect 1 part in 32,000—far better than most digitizing devices. For higher frequency waveforms—up to 1MHz—the 194A samples with 8-bit resolution. And its 64k bytes of memory is up to 8 times that of other digitizers.

Add the 1944A Channel 2 option and acquire two different waveforms simultaneously, in time sync, or asynchronously. Each channel is independent, isolated, fully programmable, and has 64k bytes of memory.

The 194A provides 5 trigger options for initiating a measurement. Pre- and post-trigger data can be stored.

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At **$4095**, you won't find better performance. And the optional second channel for just **$1995** doubles acquisition capability. For complete details contact the **Product Information Center, Keithley Instruments, Inc., 28775 Aurora Road, Cleveland, Ohio 44139, (216) 248-0400.**

KEITHLEY

equivalent temperature accuracy is 0.0005°C. The bridge also has a ratiometric capability that allows you to compare PRTs. A multichannel, remote switching unit and an IEEE-488 interface, both optional, allow you to incorporate the bridge in data-logging and ATE systems. After linearizing the PRT in an external computer, you can download the corresponding temperature for display on the Senator's front panel. From approximately $20,000.

H Tinsley & Co Ltd, 61 Imperial Way, Croyden, Surrey CR0 4RR, UK. Phone 01-681-8431. TLX 8952453.

Circle No 408

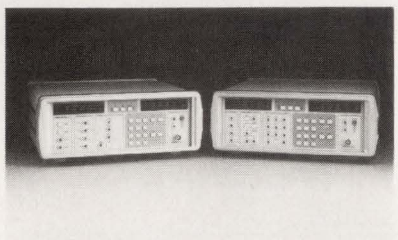
50-GHz SCOPE

- *Sampling scope uses superconducting circuitry*
- *Scope has 5-psec effective rise time*

The PSP-1000 50-GHz sampling digital oscilloscope has a built-in liquid-helium cooling system for its superconducting circuitry. The single- or dual-channel unit also accepts plug-ins that allow you to configure it as a time-domain reflectometer. The instrument has voltage ranges of 10 mV, 100 mV, and 1V. Its dynamic range is 46 dB, and it can store as many as 1024 data points. Its effective sampling-sweep speeds range from 5 psec/div to 1 nsec/div. The unit has built-in math functions for common waveform calculations, including FFTs. Its CRT can show four waveforms and markers. PSP-1000 mainframe, $120,000; plug-ins, from $20,000 to $45,000.

Hypres Inc, 500 Executive Blvd, Elmsford, NY 10523. Phone (914) 592-1190.

Circle No 409



FUNCTION GENERATORS

- *Include arbitrary-function model*
- *Units have ±0.005% frequency accuracy max*

The NIC-41 and NIC-42 function generators offer a maximum frequency accuracy of ±0.005%. The NIC-41 provides sine, triangle, and square waves over the dc to 4-MHz frequency range. The output of the NIC-42 can be as high as 2000 12-bit samples/sec, and the instrument can store as many as 99 front-panel settings. Both units offer linear and log sweep rates, along with AM and FM auxiliary inputs. The NIC-42 can also execute arbitrary sweep rates. The units have a ±10V output range (±5V into 50Ω). NIC-41, $1700; NIC-42, $3600. Delivery, 45 days ARO.

Nicolet, Test Instruments Div, Box 4288, Madison, WI 53711. Phone (608) 273-5008.

Circle No 410

SCAN CONVERTERS

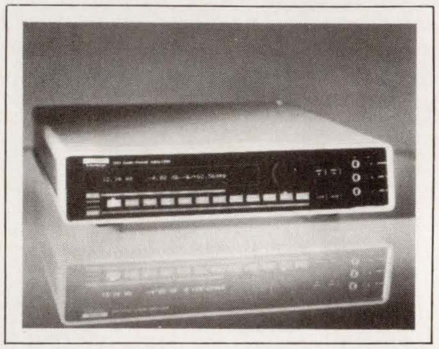
- *Units convert high-resolution CRT signals to NTSC format*
- *One model suits IBM PC displays*

The VSC line of video scan converters change high-resolution CRT signals into NTSC formats suitable for recording on a video cassette recorder (VCR). You need a computer or a graphics terminal having RGB and sync outputs. (The company can provide adapter kits for units without these outputs.) The Model VSC-6400 works with 1280×1000-pixel displays having 64-kHz scan rates. Model VSC-5500 converts resolutions as high as 1024×1024 pixels at

55 kHz; Model VSC-3400, which is suitable for use with IBM PCs, converts 800×500-pixel resolutions at 34 kHz. Model VSC-6400, $14,995; Model VSC-5500, $12,995; Model VSC-3400, $9995.

PDS Video Technology Inc, 1152 Santa Barbara St, San Diego, CA 92107. Phone (619) 222-7900.

Circle No 411



FREQUENCY ANALYZER

- *Signal analyzer makes gain and phase measurements*
- *Unit operates over 20 kHz to 1 MHz*

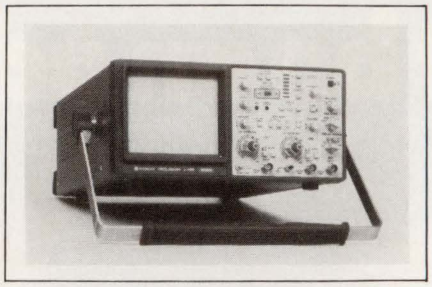
The 1253 gain/phase analyzer operates over a 20-kHz to 1-MHz frequency range. Its two input channels feed a common analyzer, and its gain and phase accuracies are 0.1 dB and 1.0°, respectively. The instrument digitizes input signals to 15-bit resolution. Its internal software can isolate the fundamental frequency being measured from extraneous noise. The instrument's nonvolatile memory allows you to program a sequence of measurement setups, which you can protect against alteration by operating a keyswitch. The unit is programmable over the IEEE-488 bus. $9500 or £4800.

Solartron Instruments Inc, 2 Westchester Plaza, Elmsford, NY 10523. Phone (914) 592-9168. TLX 145487.

Circle No 412

Solartron-Schlumberger, Victoria Rd, Farnborough, Hampshire GU14 7PW, UK. Phone (0252) 544433. TLX 858245.

Circle No 413



COMPACT SCOPES

- *Portable scopes have 8×10-cm CRTs*
- *Compact scopes weigh 13 lbs*

The four models of the Compact Series oscilloscopes have 8×10-cm CRTs. The scopes measure 11×14×5 in. and weigh 13 lbs. The V-1065 and V-160 have a 100-MHz bandwidth; the V-665 and V-660 spec 60 MHz. The V-1065 and V-665 have on-screen cursor readouts for voltage, time, and frequency. Their trigger circuits can lock onto a signal continuously even if the frequency and level change. V-1065, $1795; V-1060, $1495; V-665, $1395; V-660, $1095. The products will be available for delivery in June.

Hitachi Denshi America Ltd, 175 Crossways Park W, Woodbury, NY 11791. Phone (800) 645-7510; in NY, (516) 921-7200.

Circle No 414

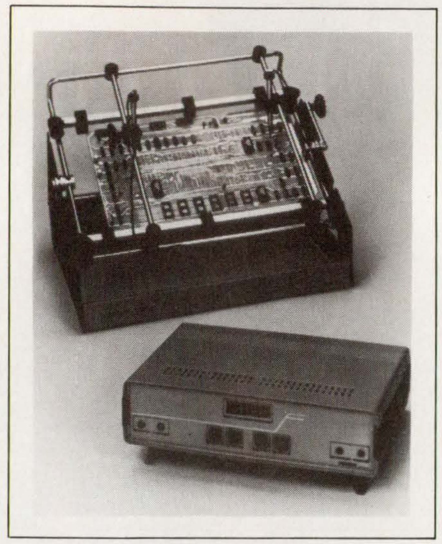
PC GENERATOR

- *IBM PC hosts instrument mainframe*
- *Pulse and waveform generators plug into mainframe*

The RC-200 is an IBM PC-hosted arbitrary-waveform and pulse generator. The unit comprises the RC-202 controller mainframe and two plug-ins—the RC-204 pulse generator and the RC-216 arbitrary-waveform generator. In addition to controlling the plug-ins, the RC-202 has 16 digital I/O lines and four D/A converters. The RC-204 has four pulse generators, and the RC-216 has a 16-bit arbitrary-waveform generator. The RC-216 can generate one to 64k samples; its time resolution ranges from 2 μsec/sample to 71 minutes/sample. The plug-in also has a programmable attenuator. The mainframe accepts as many as two generators. RC-202, $895; RC-204, $1195; RC-216, $1395; control software, $695.

RC Electronics Inc, 5386 Hollister Ave, Santa Barbara, CA 93111. Phone (805) 964-6708. TLX 295281.

Circle No 415



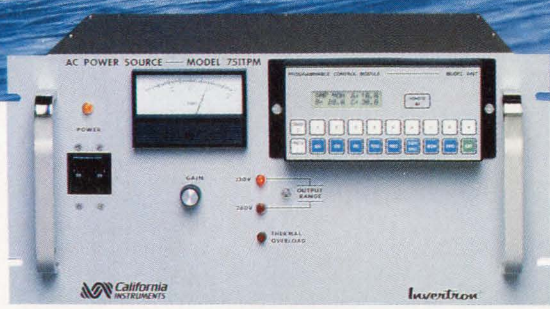
SHORTS LOCATOR

- *Pinpoints precise position of shorted traces*
- *Heat reveals location*

The Shortec 2020 PCB locates short circuits on loaded or bare pc boards. The device's spring-loaded probes measure the resistance of a short and then apply a controlled current through the shorted nodes on the pc board. A heat-sensitive film reveals the physical location of the short as it begins to heat up. Shortec 2020 PCB, $2890.

Asemtek, 17 Cummings Park, Woburn, MA 01801. Phone (617) 932-1815.

Circle No 416



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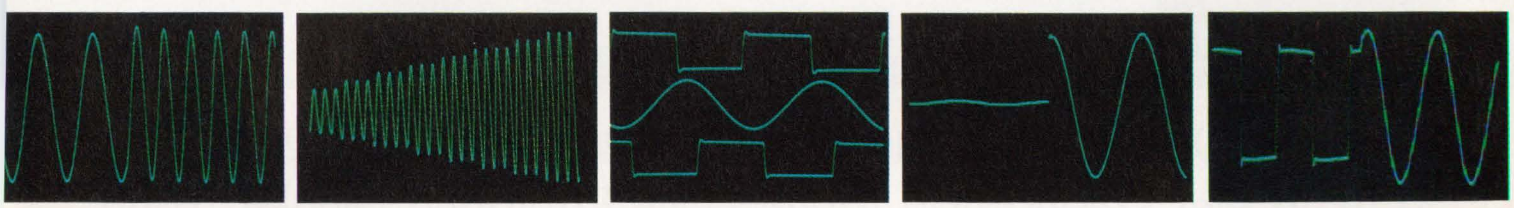

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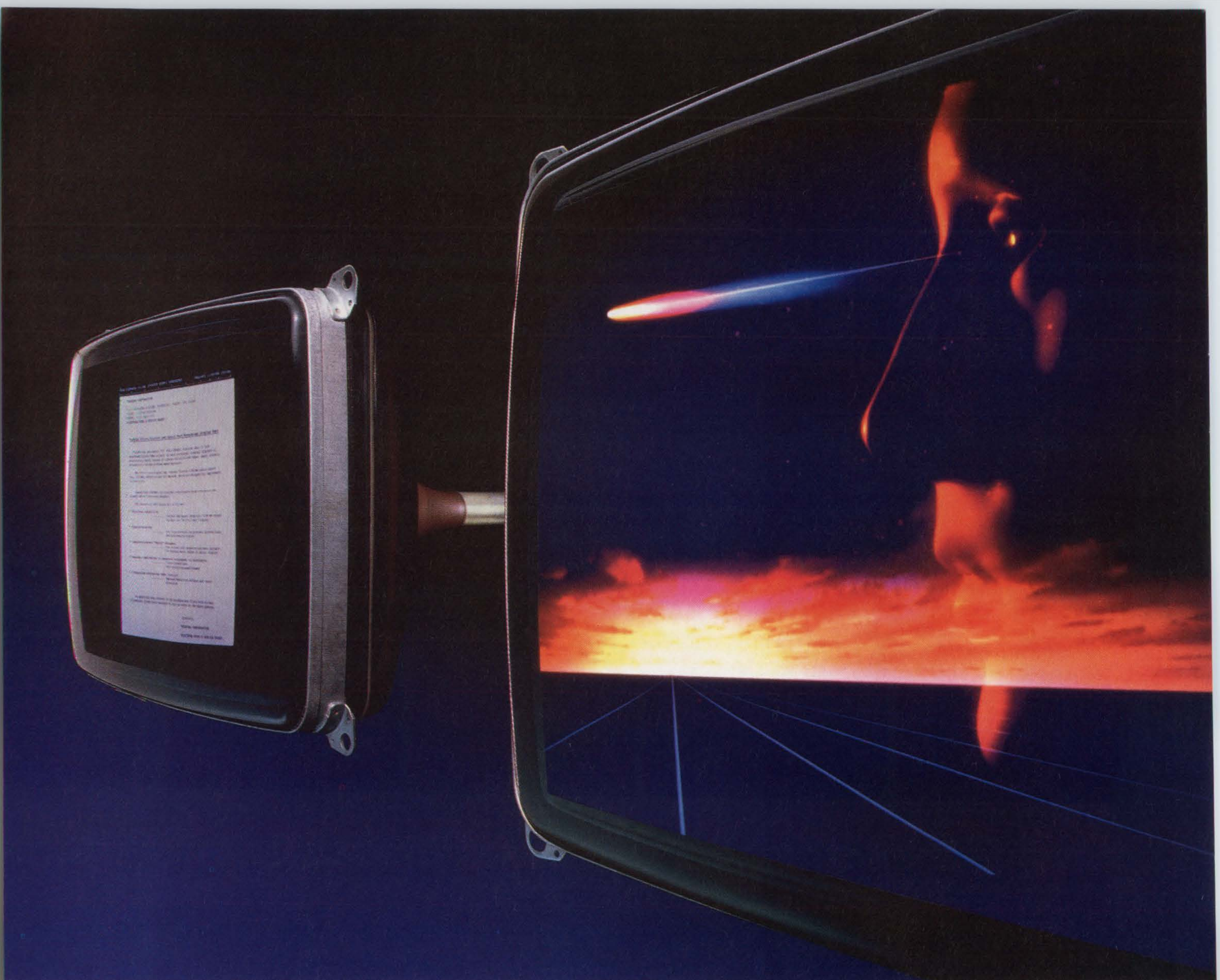

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15″ (14V) FS	E2995/E2994	0.39/0.31	260 × 190	610/770	1200
14″ (13V) Conventional	E2971/E2894	0.39/0.31	250 × 180	590/740	575
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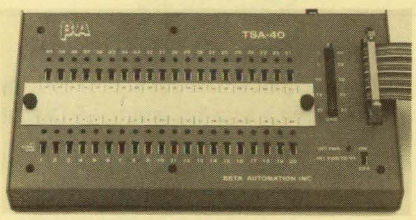

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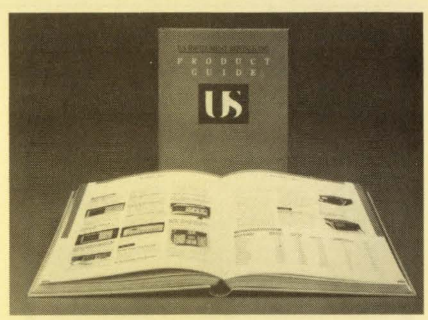

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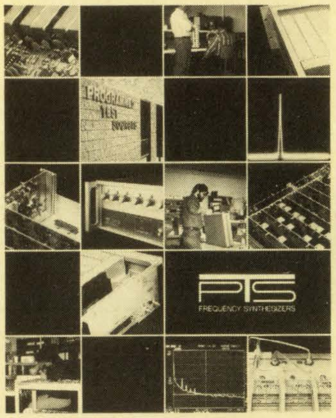

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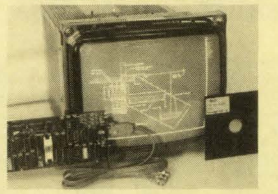

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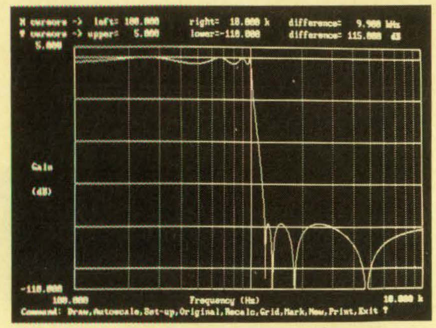

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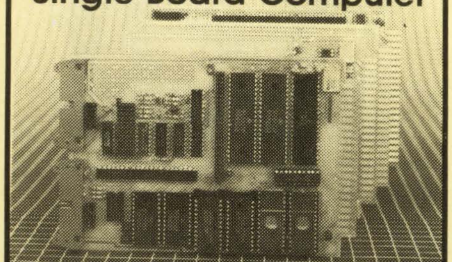

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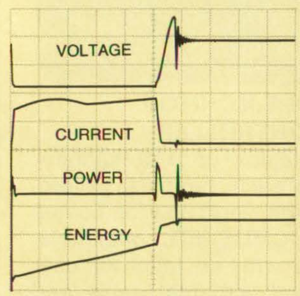

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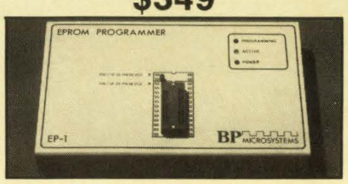

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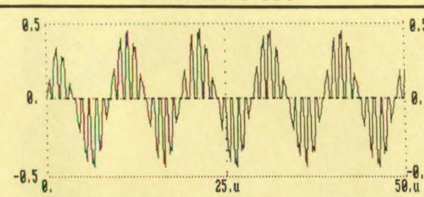

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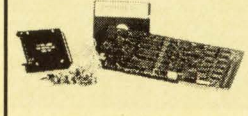

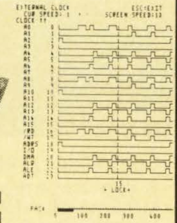

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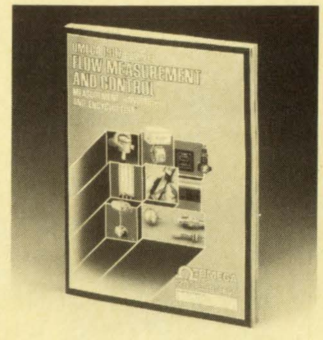

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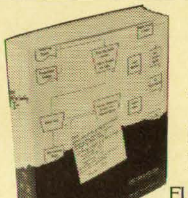

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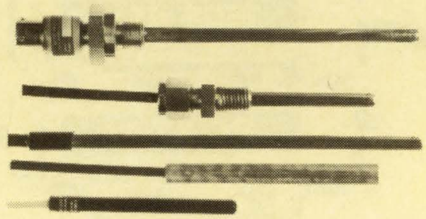
CIRCLE NO 343

TEMPERATURE TRANSDUCERS



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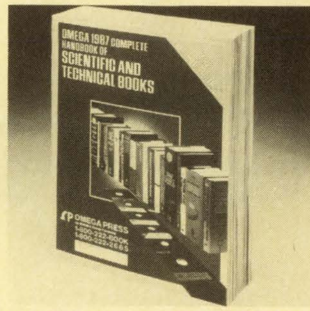

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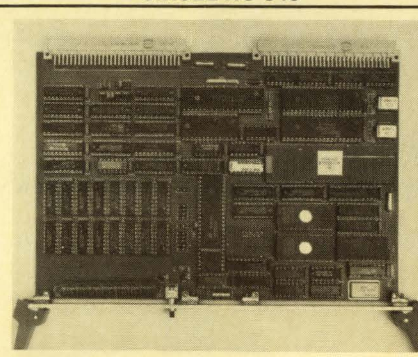

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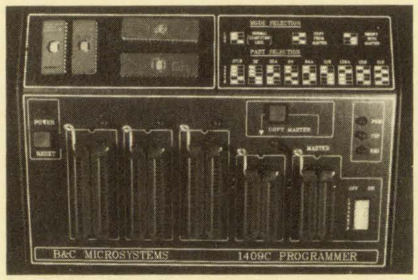

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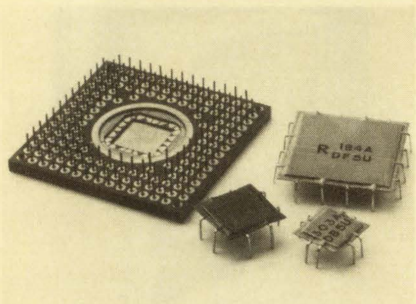

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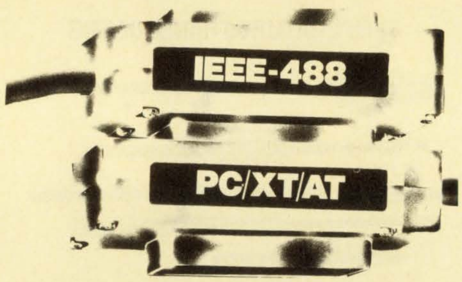

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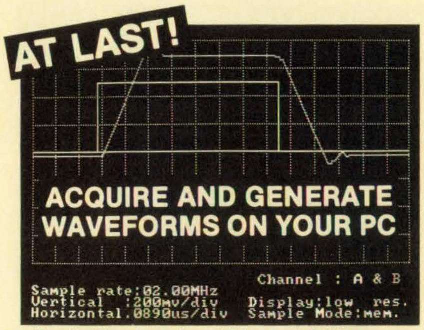

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Booklet explains new data-acquisition standard

The 56-pg product summary, *New Frontiers in Data Acquisition*, presents an overview of the company's System 1800 Series, a Fastbus (IEEE-960) line of instrumentation devices. It also describes the company's system-protocol and data-acquisition modules. Application notes and technical data sheets for the data-acquisition modules that meet the Fastbus standard are also included.

LeCroy Corp USA, 700 S Main St, Spring Valley, NY 10977.

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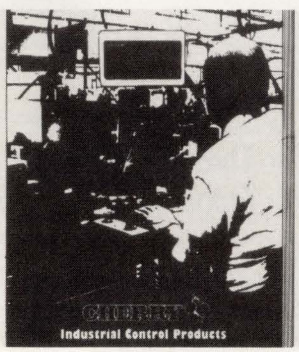

Catalog describes industrial-control devices

This 16-pg 4-color catalog lists the company's product line of intelligent and nonintelligent alphanumeric displays and accessories. It also describes the thumbwheel and pushwheel assemblies used with programmable controllers.

Cherry Electrical Products, 3600 Sunset Ave, Waukegan, IL 60087.

Circle No 418

Linear applications

The 350-pg manual, *Linear Applications Handbook: A Guide to Linear Circuit Design*, is written for system designers. Various chapters in the 360-pg book cover 3-terminal regulators, applications of

switched-capacitor-instrumentation building-block circuits, thermal techniques in measurement and control circuitry, and direct digitization of transducer outputs. Other chapters discuss high-speed comparator techniques, design of linear functions for 5V-only operation, and high-performance voltage-to-frequency converters. All applications include the schematics and parts values for the circuits described. $9.95.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

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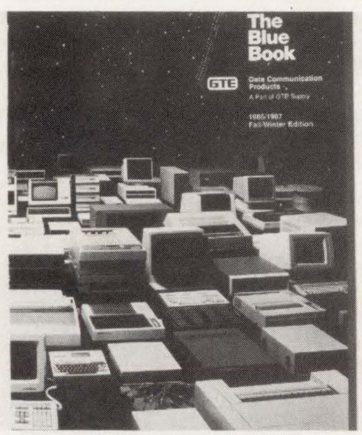

Datacomm products

The Blue Book includes more than 2000 data-communication products offered by 200 manufacturers. New listings in the 168-pg publication include the Genicom Series printers, which are IBM compatible; protocol converters from Adacom; and test-equipment supplies from Datacom Northwest. A full line of central-office, outside-plant, customer-premise, and data-communication supplies is available.

GTE Supply, 5225 Wiley Post Way, Lakeside Plaza 2, Salt Lake City, UT 84116.

Circle No 419

Tools for your PC

Each edition of *The Catalog of Personal Computing Tools for Scientists and Engineers* contains information on hard-to-find IBM PC-compatible products, which the publisher selects as part of an ongoing review of numerous hardware and software manufacturers. The products are evaluated in the book according to cost/performance tradeoffs, programming considerations, installation, and operation. The latest issue of the catalog presents such products as data-acquisition and -control systems, scientific software packages, image processors, oscilloscopes, logic analyzers, and data and function generators. Other offerings include digital multimeters, frequency counters, IEEE-488 controllers, LANs, design-automation systems, and data-line monitors. In addition to producing this catalog, the company provides applications assistance for the products over the telephone.

Personal Computing Tools, 101 Church St, Unit 12, Los Gatos, CA 95031.

Circle No 420

Two brochures address distributed-control system

These two brochures present information on Mycro II, an advanced distributed-control system. *Bulletin 3900* describes the system, detailing the configurable CRT operator station, the basic CRT operator station, the multiloop controller, various components and hardware associated with the system, the architecture, and services. *Bulletin 3901* offers an overview of Mycro II, including discussions of the ideal system architecture, integrated system elements, improved opera-

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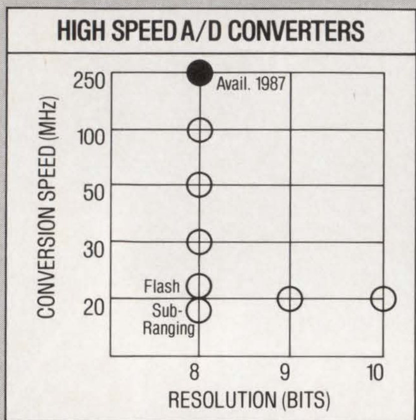

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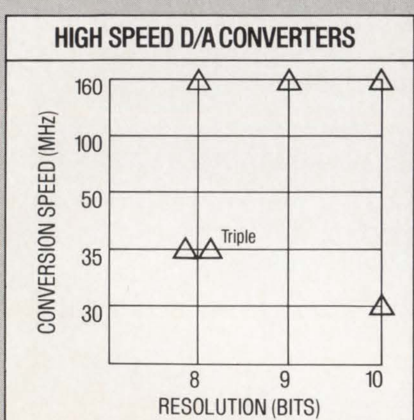

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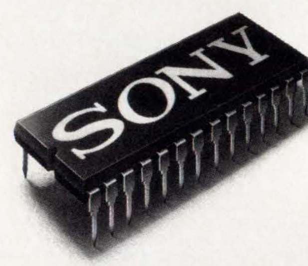

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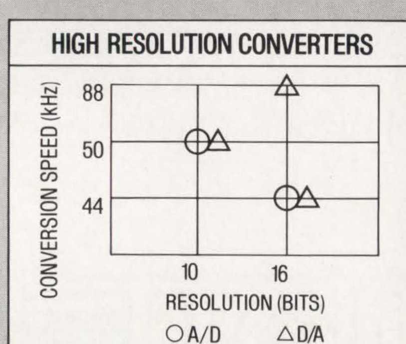

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Moore Products Co, Spring House, PA 19477.

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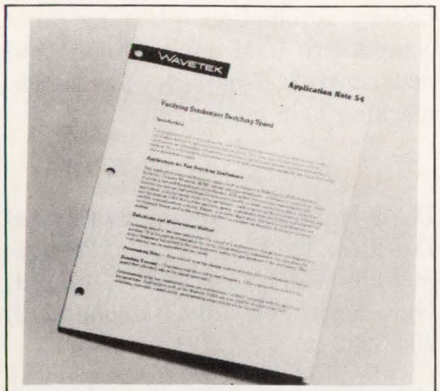

App note discusses measuring switching speed

This application note, *Verifying Synthesizer Switching Speed,* discusses a measurement method used in the final test calibration of fast-switching synthesizers. It includes definitions, measurement limitations, a typical test setup, and a detailed test procedure. The information is particularly useful to synthesizer users and to those working in calibration labs.

Wavetek Inc, Box 85265, San Diego, CA 92138.

Circle No 422

How to evaluate system-level testing

This 5-pg reprint, *Measurements on Optical Fiber Systems,* discusses the proper evaluation method for subsystem- and system-level testing. It examines fiber-optic-system features such as optical margin, bit error rate, eye diagram, and alarm and redundancy switch-overs. The reprint details the measurements required during the installation and troubleshooting periods.

Intelco Corp, 8 Craig Rd, Acton, MA 01720.

Circle No 423

How to choose a color monitor

A brochure entitled *Gaining the Color Advantage: How to Select a Color Monitor for Your PC* discusses many of the options and variables of color monitors. It suggests, for example, that buyers compare the brilliance of all colors to make sure that colors are bright and true, and that whites are actually white. The pamphlet offers other tips and tries to answer many of the important questions about how to evaluate color displays.

Princeton Graphic Systems, Box 853, Valley Forge, PA 19482.

Circle No 424

NEW BOOKS

Macro Programming for 1-2-3, by Daniel N Shaffer. 304 pgs; $19.95; Hayden Books, Indianapolis, IN, 1987. Phone (317) 298-5400.

Concentrating on the use of 1-2-3's keyboard macro facility in spreadsheet, graphics, and data-management functions, this book provides tips on how to make 1-2-3 spreadsheets faster and easier to use and more powerful by taking advantage of version 2.0. It addresses topics such as using range names, using 1-2-3's automatic typing features, and using 1-2-3's programming features.

Mastering Expert Systems with Turbo Prolog, by Carl Townsend. 272 pgs; $19.95; Howard W Sams & Co, Indianapolis, IN, 1987. Phone (317) 298-5566.

Using practical and tutorial examples and program listings, this book shows you how to design expert systems with Turbo Prolog. It provides the design elements necessary to make an expert system—from concept to application. After explaining the fundamentals, the book teaches you how to use Turbo Prolog, how to use databases, and how to control the flow of execution. It also has a section on special Prolog techniques.

Computer - Integrated Manufacturing Handbook, edited by Eric Teicholz and Joel N Orr. 466 pgs; $59.95; McGraw-Hill Book Co, New York, NY, 1987. Phone (609) 426-5254.

This handbook is a practical treatment of the technology of CIM (computer-integrated manufacturing) by more than 20 specialists in the field, with emphasis on the economics of CIM. It discusses the role of CAD/CAM in CIM and numerical control systems, and it give a projection of future trends and developments. Other topics the book examines include robotics, process planning, production planning and control, the role of materials handling, technology management and factory automation, planning for a competitive CIM environment, and how controls, feedback, and benchmarking help implementation.

Hy-Q Handbook of Quartz Crystal Devices, by David Salt. 229 pgs; $69.95; Van Nostrand Reinhold, New York, NY, 1987. Phone (212) 254-3232.

Intended for use by engineers concerned with frequency management, this book provides background material on both the design and manufacture of quartz devices to help you understand the practical

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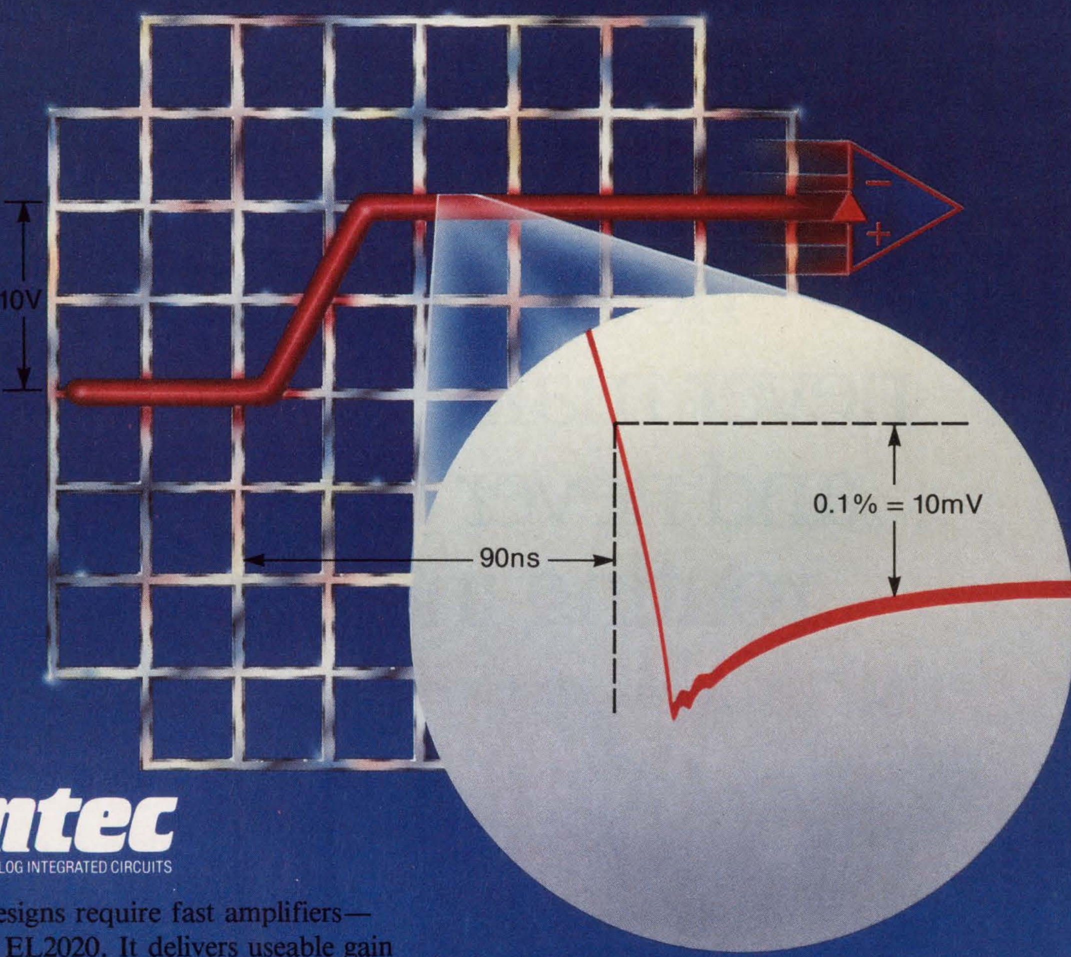

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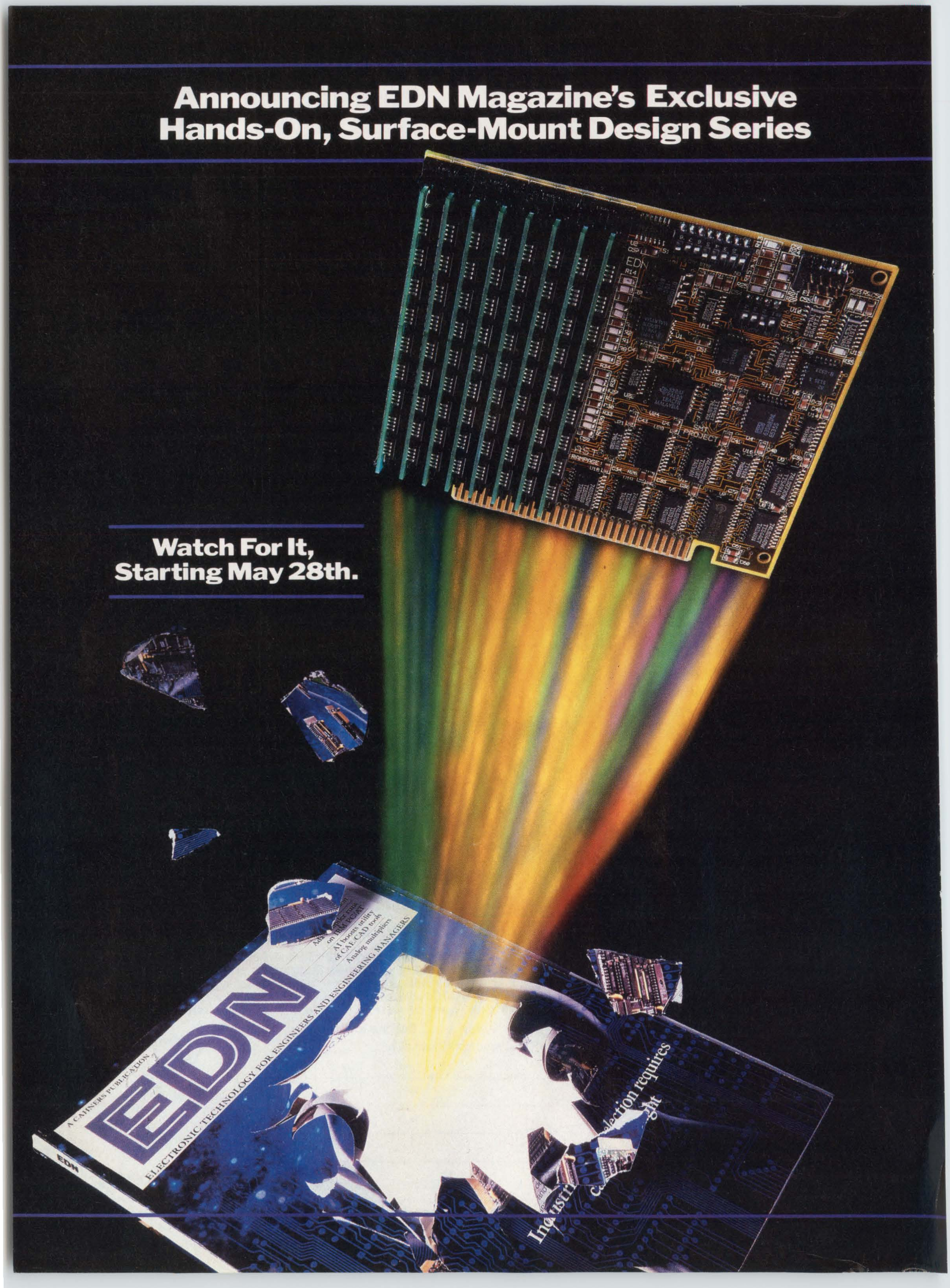
Being the Boss: The Craft of Managing People, by L Kent Lineback. 192 pgs; $18.70 (member); $24.95 (nonmember); IEEE Press, New York, NY, 1987. Phone (201) 981-9535.

This book stresses the fundamental activities required to manage people effectively. The book has three parts. It begins with a case history of a manager in a software development group, then goes on to present a plan to assist you in coordinating your day-to-day activities. Part II, the Fundamental Cycle of Management, explains the specific activities a manager repeats constantly. The third part examines problem solving and how to deal with situations such as hiring, firing, and appraising.

Effective Meetings for Busy People: Let's Decide It and Go Home, by William T Carnes. 348 pgs; $22.30 (member); $29.75 (nonmember); IEEE Press, New York, NY, 1987. Phone (201) 981-1393.

This book pinpoints the reasons behind unsuccessful meetings and presents a new methodology to make them more effective, interesting, and profitable. The principles discussed are valid for meetings in all kinds of organizations. The author reviews some established traditions and opens the way to new concepts, ideas, and techniques.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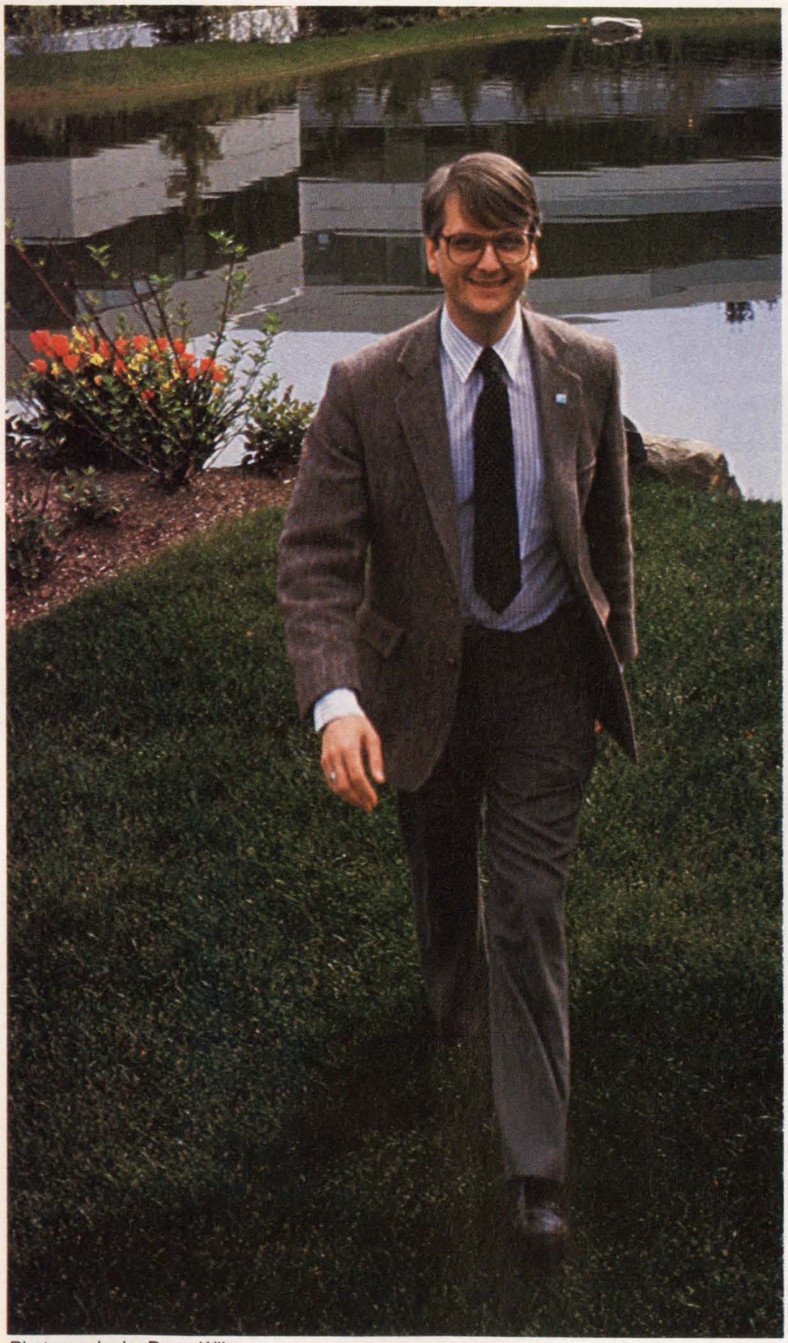
John Butler: Trading in a doctor's bag for a career in programming



Photographs by Doug Wilson

In the little spare time that John Butler had during his cardiology fellowship at the Medical College of Wisconsin, he always made an effort to read books and magazine articles on computer technology, a subject that had held his interest briefly before he began medical school.

Browsing through a bookstore, he came upon a volume on structured computer programs and began reading about finite mathematics. "I can't do analog math, which I thought meant I couldn't do math," Butler says. "It wasn't until I got that book that I discovered a whole new kind of math, the math of sets and relationships, the field of finite math."

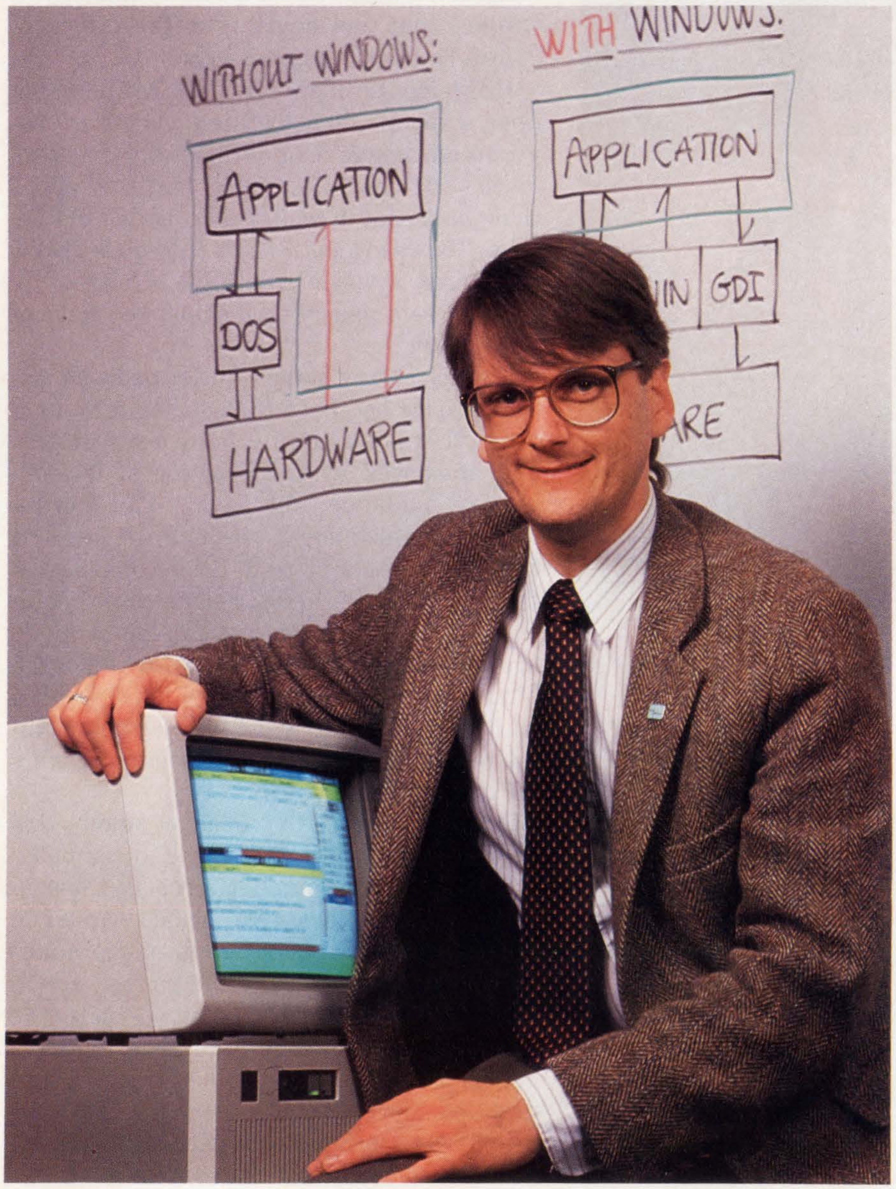
That discovery helped Butler make a decision that he had been considering for a long time. "I was excited by finite mathematics and unexcited by the practice of fee-for-service medicine," he says. "The more I looked at cardiology, the more it seemed that there was a place in it for computers." Deciding that he might better serve medicine by improving the medical community's use of technology than by working as a physician, Butler decided to leave behind both his position at St Luke's and the medical career for which he had been preparing for the last eight years.

After going back to school yet again—this time to earn a master's degree in computer science—Butler joined Microsoft Corp in Redmond, WA. Since 1982, he has worked on the development, marketing, and product support of Windows, the company's version of a windowing environment. Despite the twists and turns of his professional career, he has never really abandoned the goal that first led him to medicine—that of serving people. By continuing his work at Microsoft, he hopes someday to write easy-to-use medi-

One year shy of becoming a cardiologist and beginning the medical career for which he'd spent eight years preparing, John Butler abandoned medicine and switched to software. . .

cal application programs that will allow doctors to spend more time treating patients and practicing preventive medicine.

Choosing a medical career came naturally to Butler, whose family tree already included several physicians. After studying psychology as an undergraduate at the University of Washington in Seattle, he applied for admission to several medical schools. His acceptance by New York University was no doubt influenced to some extent by his application, in which his flair for the unusual was apparent. In a large blank space reserved for some form of personal expression, Butler wrote a limerick: "There once was a young man with a mission, which was to become a physician, so he wrote a short verse, which though rather terse, he hoped would amuse the commission."



In medical school, Butler's goals and attitudes proved equally unconventional compared with those of his fellow students. "Most of the students cared about learning the facts and doing whatever it is a doctor does to earn money," he says. He became part of a small group of NYU students who worked to bring humanistic changes to the school's grueling curriculum. They instituted a student note-taking service, for example, so that students who missed a class could obtain the lecture notes. They also argued successfully for a course that taught students how to ask basic medical questions in Spanish, an important tool for providing medical care in New York City, where a large part of the population is Hispanic.

Catching up with technology

In 1976, while a resident physician at the University of Pittsburgh's Presbyterian Hospital, Butler discovered that computer technology had come a long way since 1969 when he had taken an undergraduate course in the Algol language and submitted cards to large computers for processing. "I picked up a copy of *Popular Electronics* and learned that, for $1500, you could buy all of the parts used to build a computer as powerful as the ones I used to submit decks to."

Medicine, however, appeared to be extending a less than warm welcome to the new advancements. Though the medical community had quickly found use for the detailed x-rays that CAT scanners produced, it found the benefits of other ad-

. . .Butler hopes someday to put to use his combined knowledge of medicine and computers by writing medical application programs that free doctors to spend more time with their patients.

vanced equipment less readily apparent. In 1978, in the critical-care unit of Milwaukee County Hospital where Butler worked as a cardiologist, a minicomputer with a Fortran program for storing patient records went virtually unused. The machine's complicated user interface, Butler says, caused most doctors to shy away.

"Clearly what had happened was that nobody who was going to use the machine had been in on the design of the program," he says. Moreover, though the data was being presented to doctors in a new format, the information was not being analyzed any differently. "Some doctors were being trained how to get the data from the machine, but nobody was being trained to analyze the data." The result was that much of the new equipment was little more than technological window-dressing.

The timing of Butler's observation of the gap between technology and medicine was important for him. For a number of reasons, he found himself growing increasingly detached from the medical profession. An emphasis on good health was missing from much of the medical community's activities. Instead, Butler saw too many doctors managing their practices, and their patients, as proprietors running businesses.

He also grew uncomfortable with the skewed earning ratios in the medical profession. "I had a problem with the 40:1 ratio of earning power to responsibility," Butler says. While some doctors were earning large salaries for relatively few hours of work, technicians were working longer hours, providing crucial support services, and taking home much smaller paychecks. At one private hospital where Butler worked as a cardiology fellow, most of the teaching was done by a low-paid technician; the doctor, who was presumably teaching the resident physicians, spent six hours each week at the hospital and earned three times the technician's salary.

But two specific instances sealed Butler's decision to leave medicine. The first came when he discovered that, upon the orders of the attending physician, it was a technician—not the physician—who decided the critical moment at which fluid was to be drained from around the heart of a seriously ill patient. The second instance occurred when an attending cardiologist incorrectly diagnosed Butler's slightly irregular heartbeat, which Butler knew to be a normal variance, as a congenital heart defect. That diagnosis, based on a cardiogram of Butler's heart, had a chilling effect on him. "It was wrong," he says flatly. "Furthermore, it was insupportable on the basis of the evidence."

He was deeply disturbed by many of his medical colleagues' disinclination towards change; the notion that the practice of medicine could be improved seemed foreign to many of them.

"I thought that here's a system that pays the wrong people too much money and doesn't educate people," Butler recalls. He was deeply disturbed by many of his colleagues' disinclination towards change; the notion that the practice of medicine could be improved seemed foreign to many of them. Rather than continue as a physician, and despite strong support from the medical faculty, Butler chose to leave medicine, ending his fellowship a year early. "I had no hope," he explains. "The problems of the system seemed insurmountable."

As difficult as the decision was for Butler to make, it proved almost as difficult for his peers in medicine to understand. "I had never hung any of my identity on the label of 'doctor,' so that was not hard to give up. What was difficult to understand was the feeling among many doctors that I had failed as a physician."

With the financial support of a fellowship from the National Institute of Health, Butler returned to the University of Washington to conduct research at the Center for Bioengineering and study computer science. Lacking some of the math requirements needed for graduate study, he spent two quarters in undergraduate classes. "It was really hard being a student again. I had already been a freshman undergrad, a freshman in medical school, an intern, and a resident, and here I was at the bottom of the rung again."

Yet Butler was there with a specific purpose in mind. He had left his medical career, but he had not left behind his thoughts of improving medicine. The computing advances that had occurred paved the way for new ties between technology and medicine, and he saw himself, once he had studied computers, as someone who could help forge those ties. His goal for the computer knowledge he was acquiring was clear: "To make computers usable for doctors—to make sure that when a doctor decided to use a computer, it was going to be well used."

After graduating in 1982, Butler began looking for a job. Most companies he approached were unsure of what to do with "a lapsed physician," as he calls himself. At a neighbor's suggestion, Butler sent a résumé to Microsoft Corp. He had written a graphics program as a graduate student, and he found that his interests in graphics matched closely with Microsoft's. In early 1982, he joined the then seven-year-old company as employee number 180.

His original job was to build on the success of the company's GW Basic program and enhance it.

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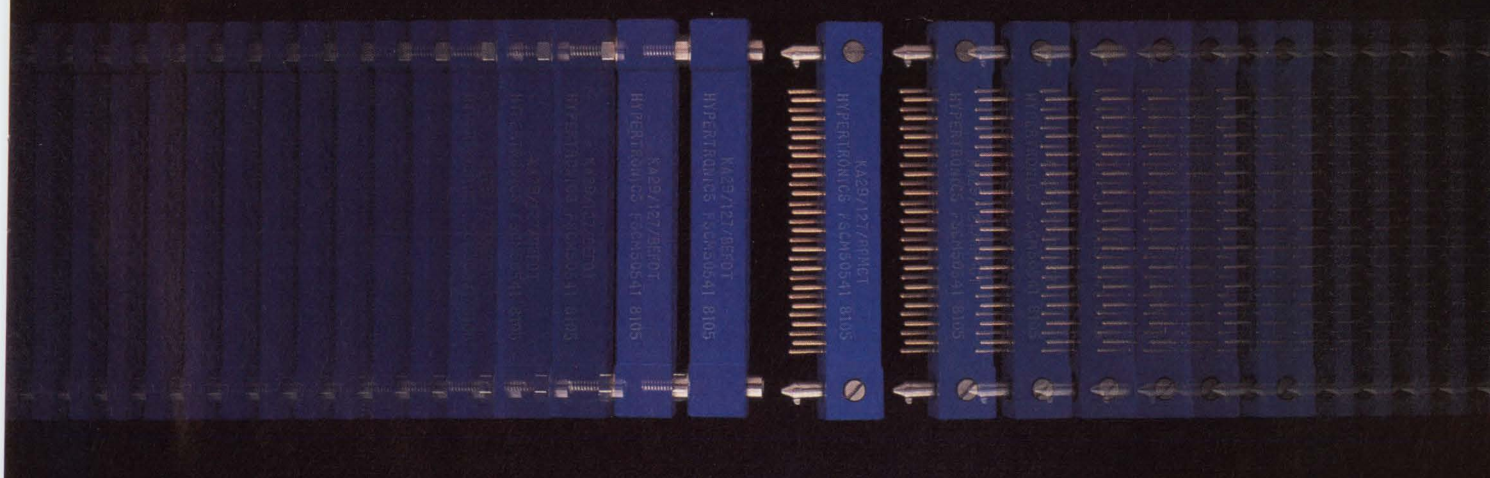

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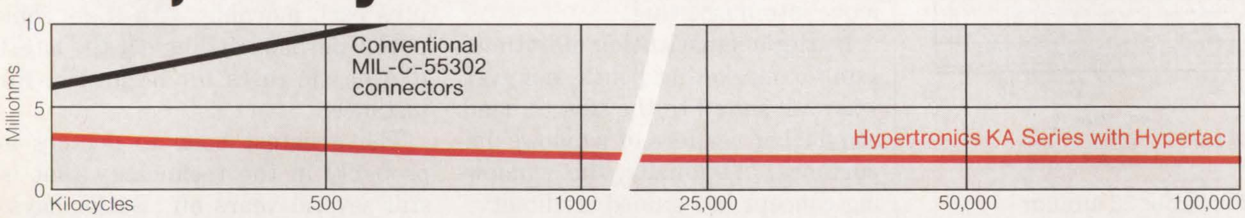

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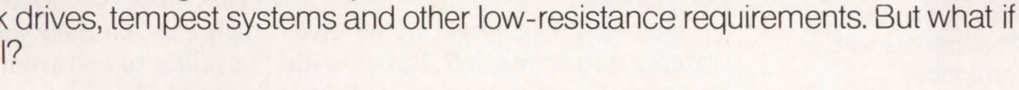

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From the beginning, though, he viewed windowing capabilities as the foundation that would make computers more usable. Indeed, he was more excited by the potential of windowing applications than by the graphics library on which he was working. Reluctantly, he says, "My boss and I made an agreement that I would only talk about windowing on Friday afternoons."

In early 1984, shortly after Microsoft introduced Windows, he moved to marketing. His entry to marketing, he says, is attributable to his enthusiasm for the product and to the company's shorthandedness. Had the company not experienced the spectacular growth it did over the past few years—from 180 employees when Butler was hired in 1983 to more than 1300 in early 1987—Butler says it's unlikely someone without experience would have been given the opportunity to move into marketing.

Butler's substitution of enthusiasm for marketing polish, however, was well suited to the task at hand: convincing vendors of windows' importance. "Gradually, the windowing concept has gained credibility," Butler says proudly. "After a while, the questions changed from 'Why windows?' to 'Why Windows vs [other window packages like] Gem or Topview?'"

Four years of work in the electronics sector has left Butler with no regrets about leaving medicine. "I feel daily that I've made the right decision," he says. He delights in the patterns of change and experimentation that characterize the computer industry. "In computer science, there's richer thinking, more ways of doing things, more unexplored territory," he says. "When you sort data, you realize there are lots of different ways to do it, and they're all right." In medicine, he says, there's a feeling that there's only one way to do something.

Working to promote expanded use of windowing applications gives him the ability to effect change that he missed in medicine, he says. "In medicine, I could have impacted the 3500 patients I cared for, I could add value to each life as I touched it, but I wouldn't have had a lot of leverage. In this position, though, I have tremendous leverage: We've sold 700,000 copies of the Windows program."

Still on his agenda, though, is the task of writing easy-to-use applications packages for doctors. Current software for medical-practice management tracks a physician's billing records, but nothing more, he says. Butler envisions a system that integrates continuing-education capabilities with spreadsheet capabilities. "The general practitioner is going to want to take the best advantage of the little time he's got, between patients, for example." He foresees doctors spending 30 minutes each morning with their computer, perhaps finding out the latest diagnostic tests for hepatitis, for instance.

The greatest boon to doctors is probably in the technology that is still several years off, Butler says. Voice printing, for example, will allow doctors who don't type to use computers. Talking computers will be an asset, he says, "because a great place to reach doctors is in their cars, on their way to work and traveling to and from three or four hospitals."

His rationale for choosing windows as a way of looping his career back towards medicine is simple: He believes it's the computer technology best able to help cardiologists because it will let doctors spend more of their time on medical care, the skill they are trained in. "That's all windowing is, a way to let people do what they do best." **EDN**

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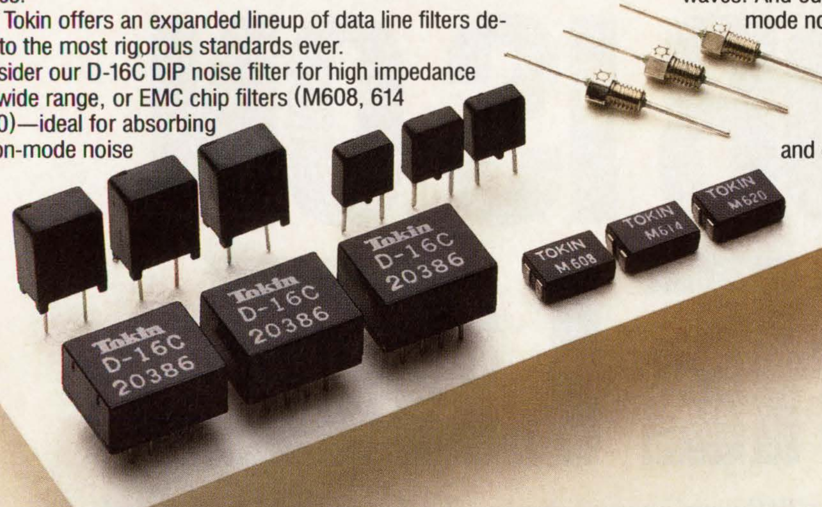

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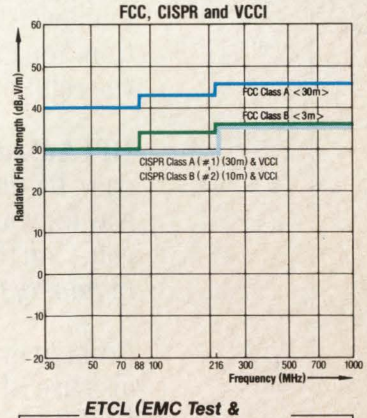

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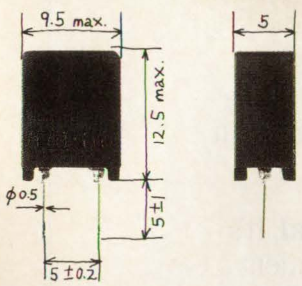

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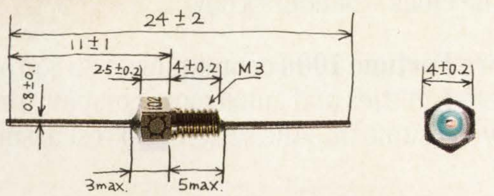

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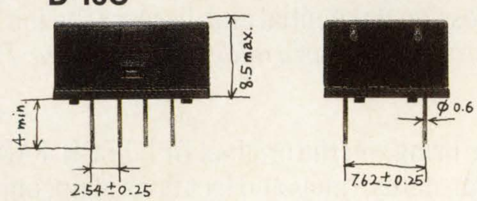

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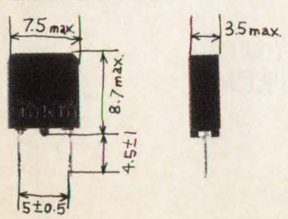

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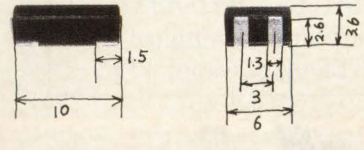

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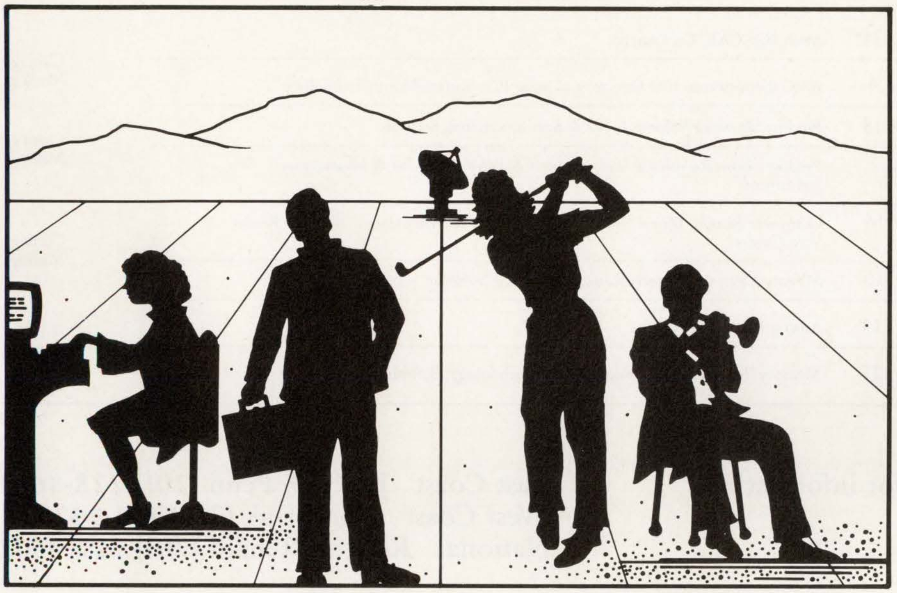

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June 25	June 4	ASIC (Semicustom ICs) Directory; Analog ICs; Surface-Mount Technology	
July 9	June 18	Product Showcase-Volume I; ICs & Semiconductors; Software	Closing: June 25 Mailing: July 16
July 23	July 2	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments	
Aug. 6	July 16	Computer Boards; Digital Signal Processing; Test & Measurement; Top Ten Reader Vote Contest	Closing: July 23 Mailing: Aug. 13
Aug. 20	July 30	Military Electronics Special Issue; Fiberoptics; Software	
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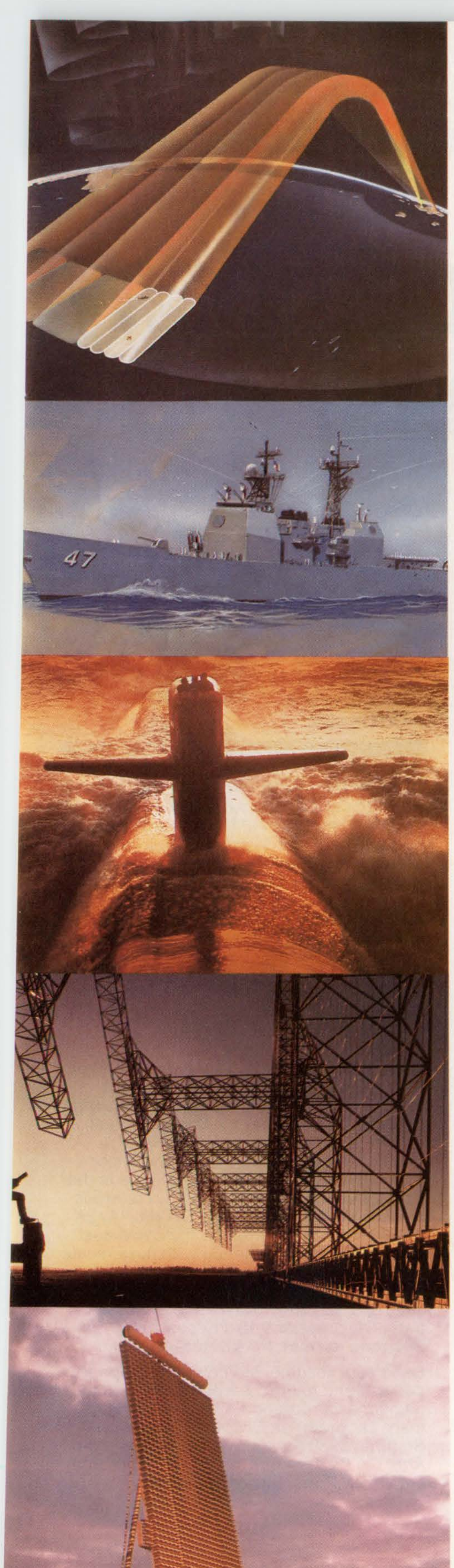

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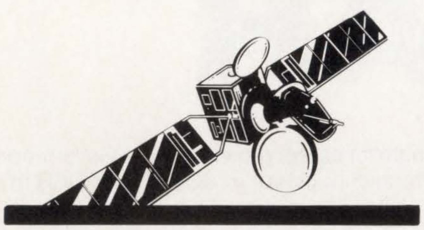

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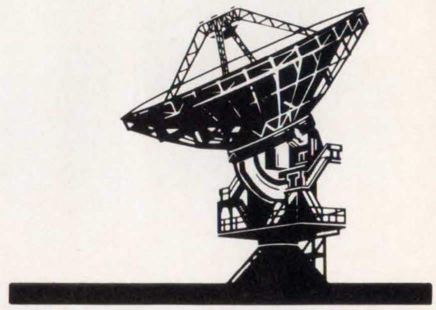

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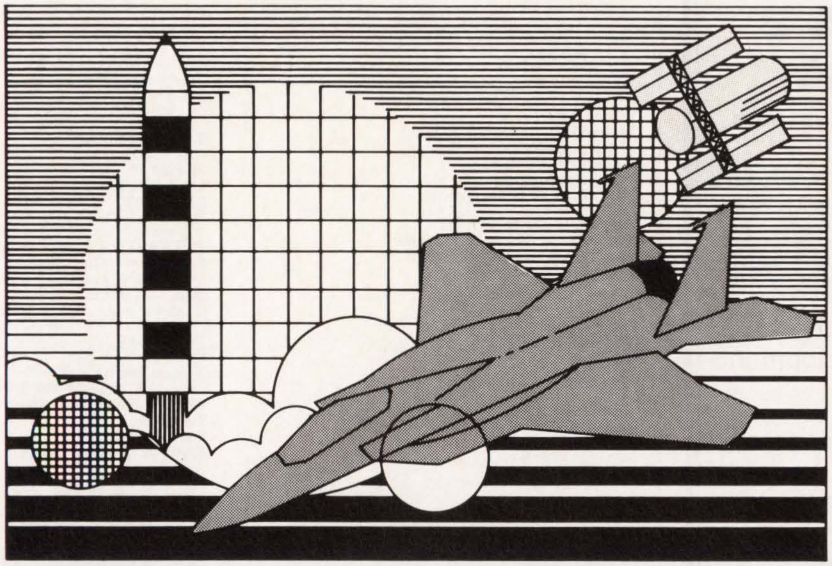

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Diann Siegel, Assistant

Peter D Coley
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Advertising Sales Director
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(201) 228-8608

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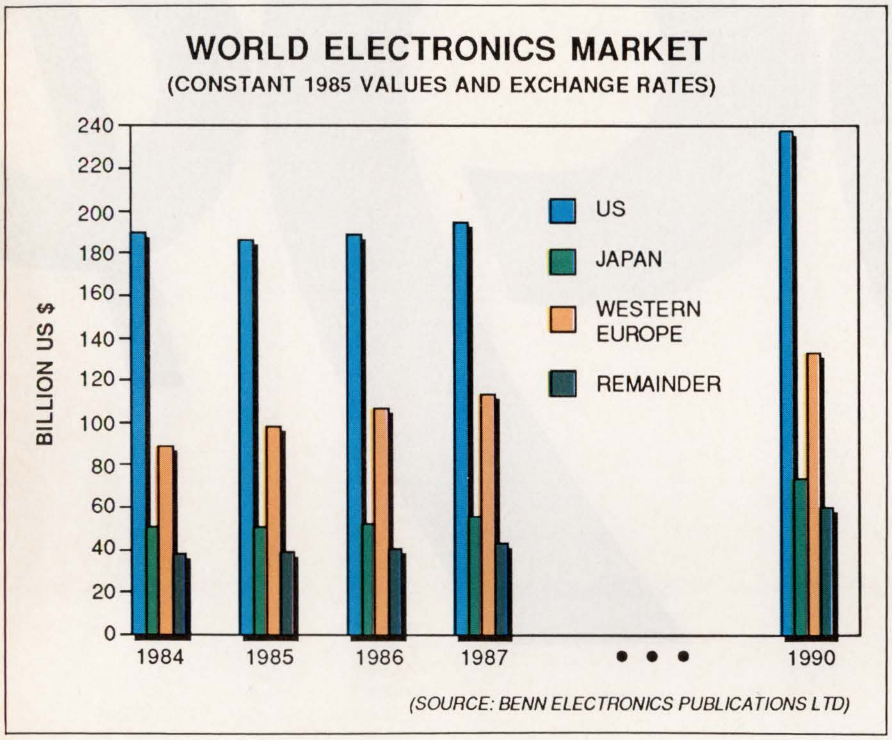

World electronics market to grow nearly 7% annually

The world market for electronic equipment and components is expected to grow at a 6.9% rate in 1987 and at an average annual rate of 6.6% throughout the remainder of the 1980s, according to the electronics-market research company Benn Electronics Publications Ltd (Luton, UK). The total dollar value of this market will be $413 billion in 1987 and $500 billion in 1990 (US dollars).

The "world," according to Benn Electronics, comprises the nations of Western Europe, North America, and the "Asia-Pacific" region—that is, the dominant free-market economies. In the United States, the 1986 market for electronic equipment and components grew at only a 0.9% rate, but the research company believes that that growth rate will be 5.7% in 1987. By contrast, the 1987 growth rates for Japan and Western European nations will be 8.2% and 7.5%, respectively. The remaining countries will see nearly 9% growth in 1987, with India showing the highest rate—18%.

Benn Electronics predicts that growth in the production of electronics equipment and components will be marginally higher than growth in consumption in the US and Western Europe. Far Eastern nations will be the chief beneficiaries of Japan's 1986 drop in production, which is traced to the appreciation of the yen and the consequent restrictions on exports. In South Korea, Singapore, Indonesia, Malaysia, and the Philippines, production growth will exceed 20%, and these countries will devote significant amounts of that productivity to exports. India will also experience an increase in production, but that increase will be largely stimulated by internal demand.

Benn Electronics divides the market into electronic-data-processing (EDP) equipment, consumer products, telecommunications products, military and related communications equipment, active and passive components, office equipment, control and instrumentation equipment, and medical and industrial equipment. The three largest market segments in 1987 will be components (25.2%), EDP (22.2%), and the military (15.3%).

Market for logic synthesis to boom in next few years

Logic synthesis—the automatic conversion of behavioral specifications into structural circuit descriptions—will offer the next major opportunity in the market for electronic-design tools, reports the Technology Research Group, a Boston-based consulting and market research company. The market for logic-synthesis tools is expected to grow from virtually nothing in 1986 to $200 million in 1990.

The group regards logic synthesis as the next logical step in design automation and the final step in bridging the gap between concept and design. "We expect logic synthesis will increase productivity more than any other electronic design tool in today's market," says Andrew S Rappaport, president of the research firm. "And where there's productivity, there's money. For 1987, we expect [that] logic synthesis will generate about $5 million in revenues as a handful of companies begin to offer products."

Logic synthesis will allow designers to experiment simply and quickly with different ways of improving a system's design, says Rappaport. The tool will eliminate much of the time-consuming drudgery involved in producing a detailed structural description for each new design. "The first customers for logic synthesis are already doing a primitive form of it—in developing programmable logic devices," Rappaport observes. "Logic-synthesis tools will offer a similar process, but they'll be able to handle much greater complexity, and more kinds of circuits, including gate arrays and other user-specific chips."

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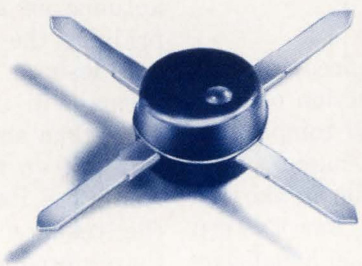

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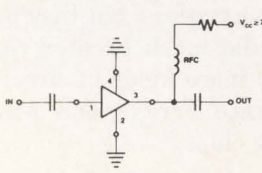

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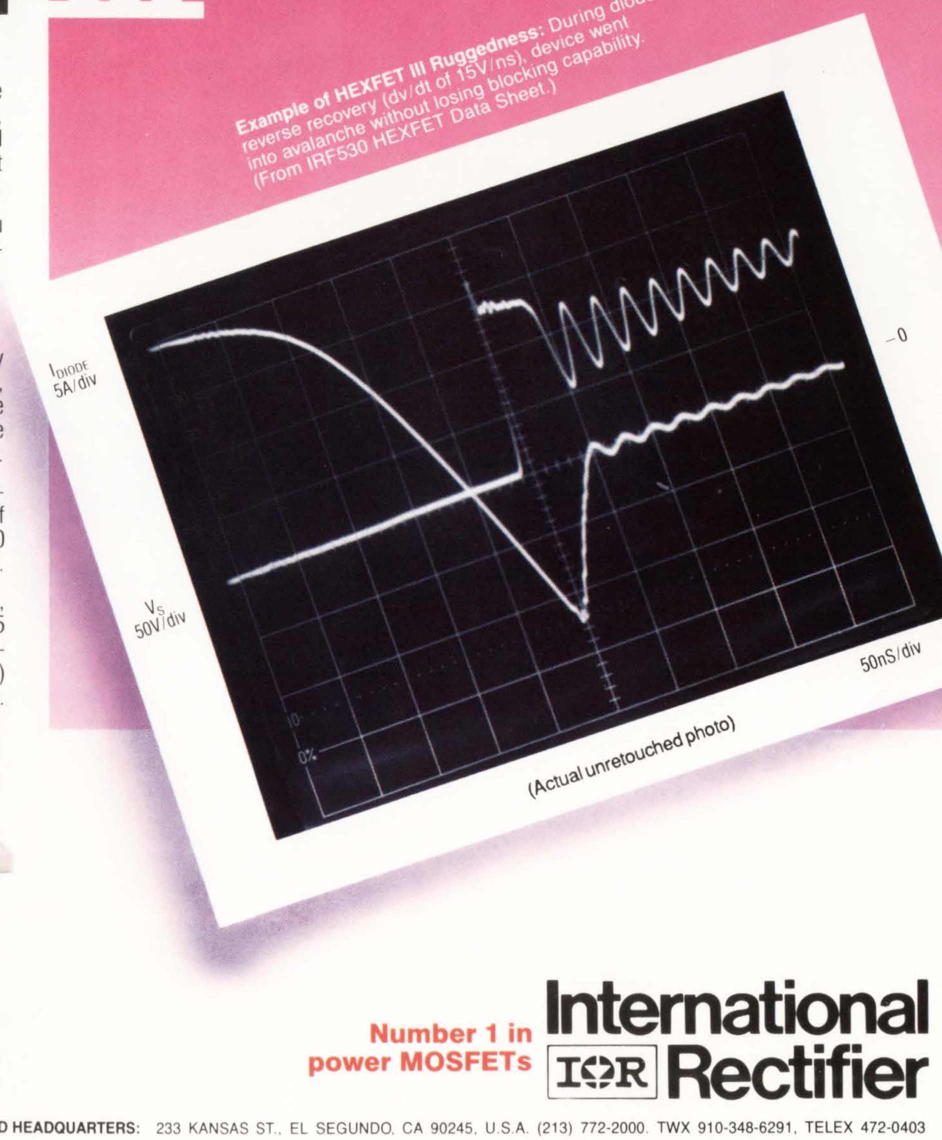

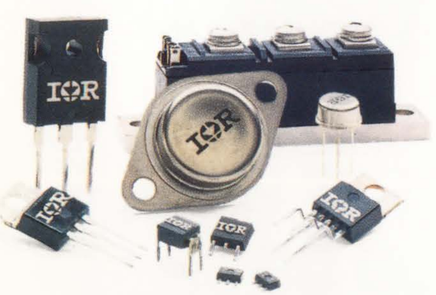

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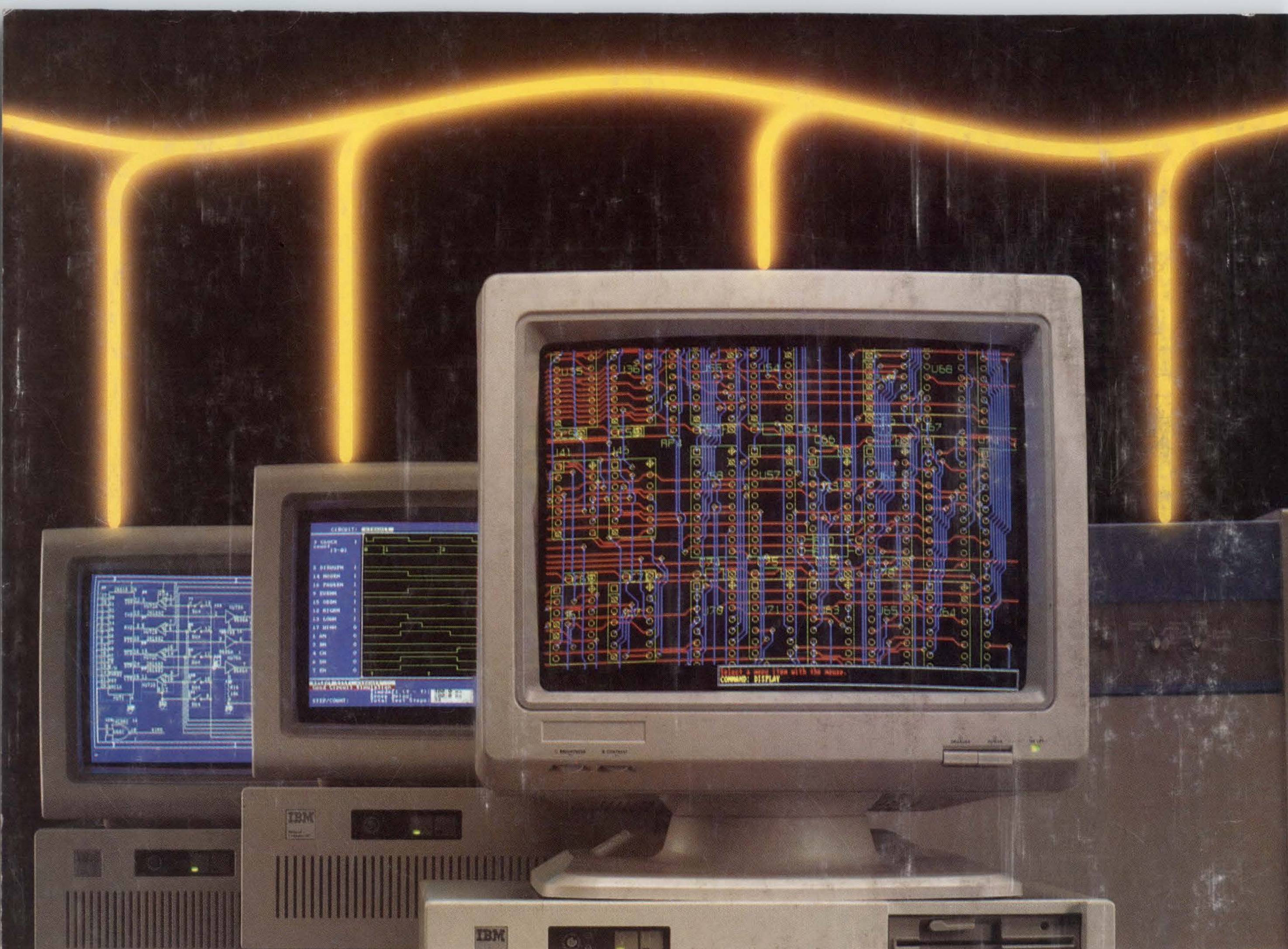

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