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EDN

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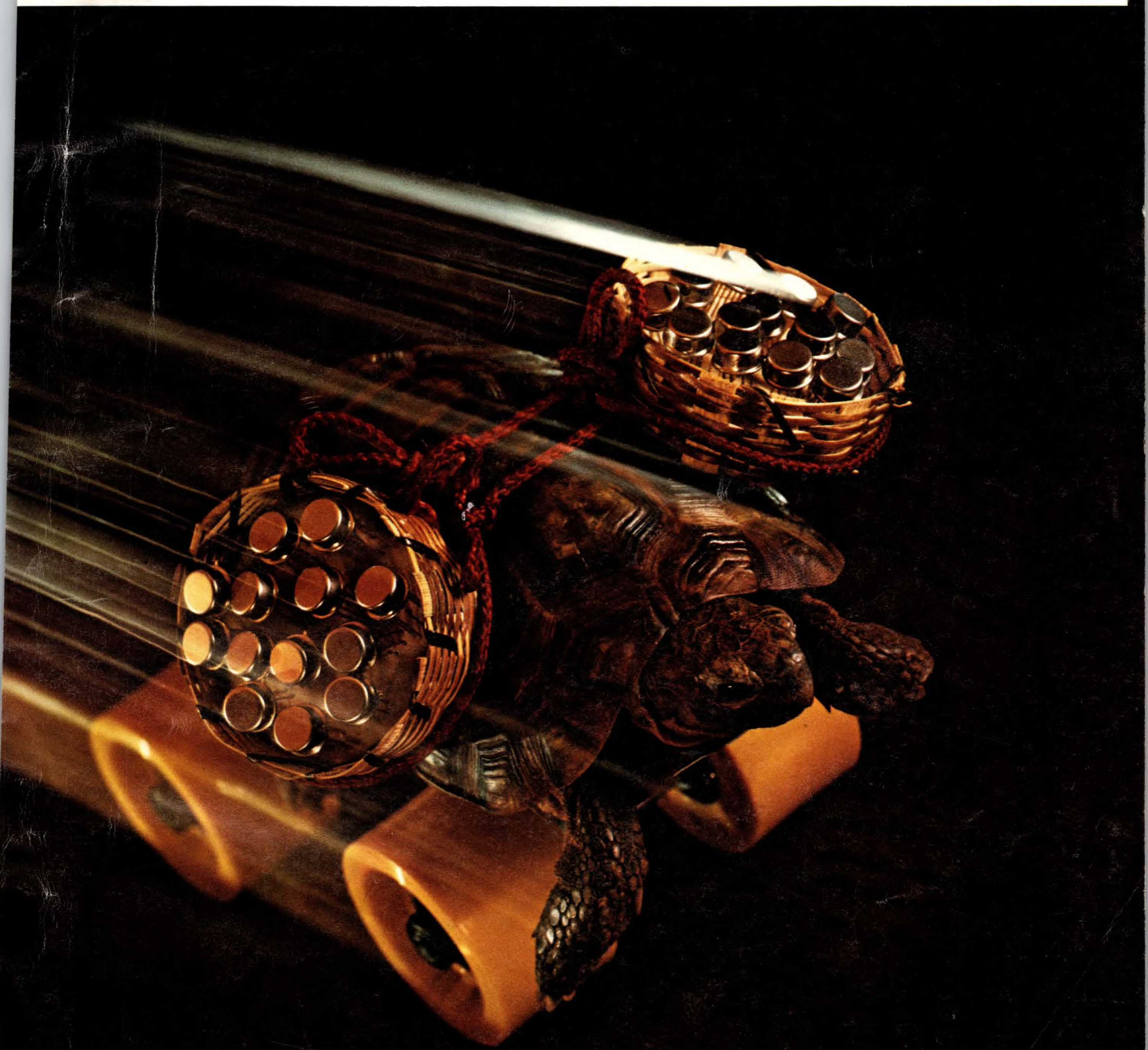
65, 73, 135 149.

Exploring 16-bit μCs — 32-bit architecture hides beneath 68000's lid

Powerful array processors speed number-crunching tasks

Cut switcher input drain with dynamic PF correction



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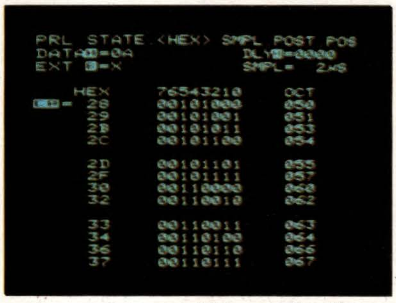
4. Press "start" and you're done. Now, you can view the acquired data in the format you want. Or, store the data in the reference memory by pressing the "store" key. Other function keys allow you to acquire new data and compare it with the reference memory.



In each data acquisition mode, all measurement parameters are displayed for your convenience.

Minimum keystroking with the new 308 Data Analyzer from Tektronix.

Of course, the 308 Data Analyzer can do a lot more than we've shown here. For example, there's a self-test routine at power-up, plus seven diagnostics, to ensure accurate results. And the 308 weighs only 8 pounds (3.6 kg), for easy portability.

For the full story, contact your local Tektronix Field Office, or write us.

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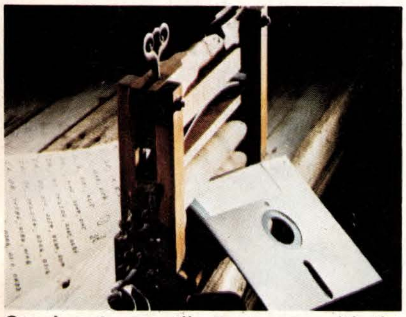

Crank out *versatile programs with the aid of automatic test generators (pg 38).*

Hybrid ADC *costs $205, achieves 600-nsec conversions (pg 69).*

On the cover: *Linear ICs achieve speedy performance as a result of gradual and steady process and design improvements (pg 96). (Photo by Patrick Tchrakian, courtesy National Semiconductor Corp)*

DESIGN FEATURES

TECHNOLOGY NEWS

NEW PRODUCTS

DEPARTMENTS

If you find a SUBSCRIPTION REQUALIFICATION CARD in the front of this issue, you MUST fill it out completely and mail it today if you wish to continue receiving EDN.

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and leave the analyzing to HP's 1610B.

If you're working with mini- or micro-based systems, you'll find that HP's 1610B is a very efficient dedicated-bus logic state analyzer.

But unlike other analyzers, the HP 1610B can also handle multiplexed-bus analysis just as effectively. The reason? Because with multiplexed buses, addresses and data appear at different times on the same lines. And first-generation logic analyzers, with their single-clock design, simply cannot demultiplex these correctly.

One popular solution to this problem has been to build a two-clock sequential acquisition system into a single package. While this approach will separate out address and read/write functions, it is still inferior to the 1610B. Why? Because this is still not true demultiplexing, in that this technique cannot correct for the real-time differential between the capture of address information and the capture of read/write data.

This means address and data information can be interleaved in the display. It requires the operator to interpret read or write functions. And it means that triggering may occur on false address/data combinations. In other words, it complicates analysis and may lead to false conclusions.

In comparison, the HP 1610B incorporates not two — but three clocks — plus a buffered memory to deliver true demultiplexing. In short, the 1610B can independently monitor addresses, plus read and write data, to demultiplex in real time for efficient and accurate analysis.

So with the 1610B, addresses and corresponding data are displayed as a single line of information, for easy comparison with your original programs. And you're sure that if you trigger on an address-data combination, the data is present at that address at that specific point in the program.

Other important capabilities.
In addition, the HP 1610B delivers other capabilities required for efficient state flow analysis of both bus structures. It will store information on a qualified basis, to permit selective editing. Which means you don't have to sort through unnecessary data. And it makes functional measurements, such as time interval analysis, on the state flow, which speeds analysis and troubleshooting.

Flexibility for the future.
Because the 1610B is a 32-bit analyzer with user-selected parameters, and a variety of options, you can use it with both mini and micro based systems, including 8-bit microprocessors such as the Motorola 6800 and the Intel 8085, as well as the newer 16-bit microprocessors such as the Z8000. And, of course, it includes HP's popular menu program format that speeds set-ups and analysis.

An economical solution to microprocessor-based systems analysis.
Another good answer to the problem of microprocessor demultiplexing is the 1611A Logic State Analyzer, with HP's general-purpose module. This module incorporates a seven-clock system that allows multiplexed information on common bus structures to be latched into 1611A inputs at the appropriate time for display. If you're already using. an HP 1611A, you'll find this module to be both an effective and cost-efficient solution.

For complete details.
The HP 1610B is priced at $12,500,* while the 1611A (including the general-purpose module) is $6,000.* For more information on these, and for an application note on state analysis of multiplexed microprocessors, write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 944-1500, Canada (416) 678-9430.

*Domestic U.S.A. price only

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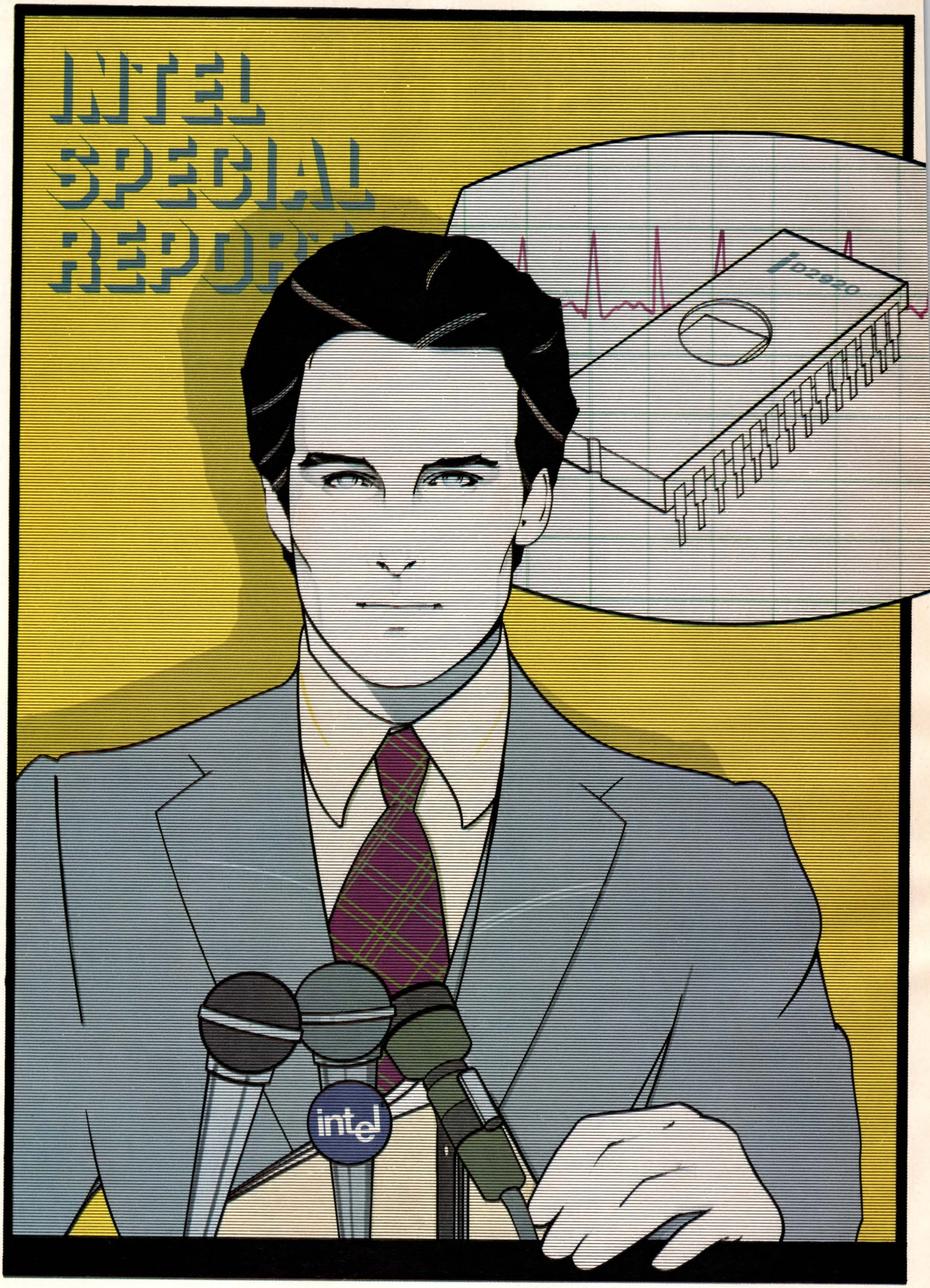

INTEL
SPECIAL
REPORT
D2920
intel

LSI Breakthrough for Analog

Intel announces the 2920 Signal Processor, first general purpose, real-time system on a chip.

Good news for analog designers. Intel breaks a new barrier in microelectronics: The first intelligent chip powerful enough to process analog signals in real time. Plus a computer-aided development package to help speed your systems to market faster than ever before.

Intel's 2920 is a complete, micro-sized signal processing system that packs the equivalent of over 18,000 transistors on a single chip. It operates hundreds of times faster than current digital processors. And best of all, the 2920 allows designers to *program* system values quickly, instead of having to match and tweak components.

A revolution in analog design

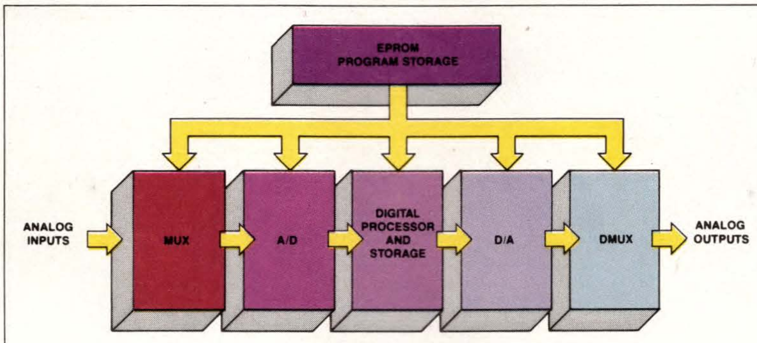
From the beginning, LSI technology has helped designers achieve dramatic improvements in product size, design cycles and manufacturing economics. But until now, the speed and complexity of analog processing has stood in the way of general purpose, single chip solutions for real-time applications.

Today, Intel's 2920 Signal Processor brings the power and flexibility of LSI to the analog world. Because of its size, the 2920 can fit in spaces too compact for traditional analog solutions. Because the 2920 is programmable, product development and time-to-market are speeded significantly. Finally, because the 2920 is a solid state device produced with Intel's proven NMOS process, reliability and manufacturing repeatability are assured to a degree not possible with previous methods.

Micro-processing for the real world

Applications for the 2920 are as broad as your imagination. Since analog designers can program the 2920 processor to perform a large number of standard building block functions, the chip can be used as an entire subsystem. Implement such functions as complex filtering, waveform generation, modulation/demodulation, adaptive processing, and even non-linear functions. This broad capability makes the 2920 an ideal single chip solution for virtually any application in the DC to 10 kHz range.

And like the digital microprocessor, the 2920 is destined to create entirely new classes of applications: products that are smaller, simpler, and less costly to produce. It gives a competitive advantage to companies in such areas as process control, test and instrumentation, guidance or control systems, telecommunications, speech processing, and seismic or sonar signal processing.



Functional Block Diagram of the 2920 Signal Processor

How the 2920 simplifies system development

Programming Intel's 2920 Signal Processor is fast and easy to learn—far less complex than the component matching it replaces. Most importantly, Intel provides the complete support tools and design workshops you need to start designing 2920 systems today.

Our SP20 Support Package and Intel's Intellec® Microcomputer Development System allow you to develop and debug by simulating your system in software. Just program functions according to your system schematic, then specify input and operating values. Together, Intel's development aids let you see how your system will work before you even build a prototype. Best of all, because you develop in digital code, your prototype system will be duplicated precisely in manufacturing.

Start making news with your product

Everything you need to begin designing a new generation of real-time analog processing systems is here today: Intel's 2920 Signal Processor, SP20 Support Package, and the Intellec Development System. For detailed information, including our new 2920 brochure, plus a schedule of Intel's nationwide 2920 Design Workshops and Seminars, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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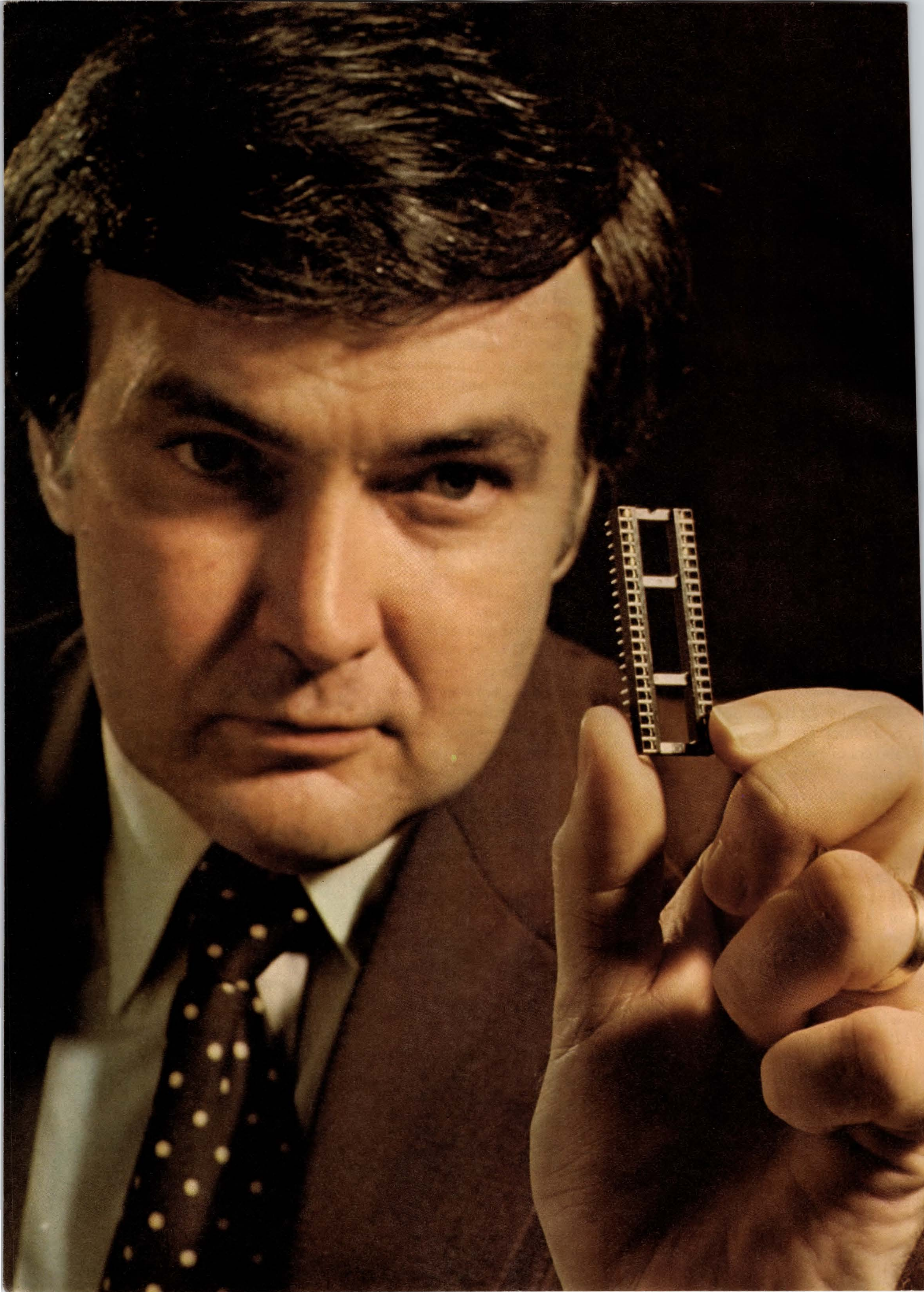
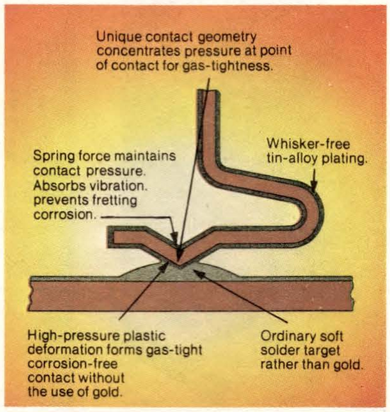


"No other DIP socket offers so much reliability, for so little cost."

Joe Bradley, VP/General Manager
Burndy Corporation

Patented GTH™ contact design.



It's our new P-11 DIP socket. And it's designed to deliver all the advantages of IC pluggability! In applications where you never dreamed of using DIP sockets before! At prices you never dreamed possible! And the reliability you always associated only with gold!

In short, it's the most economical DIP socket on the market today. With the same, proven Burndy GTH contact system that completely eliminates the need for gold—*without sacrificing reliability.*

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So before you trade-off IC pluggability because you think it costs too much—do what scores of other electronic equipment manufacturers have already done. Check our new P-11. Check the performance data. Then check our prices and start saving money right away. For fast action, call me direct: Joe Bradley, VP/General Manager, Burndy Corporation, Components Group, Norwalk, CT 06856. (203) 838-4444.

Good-as-gold GTH reliability at lower-than-ever cost.

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TEST PERFORMED	MIN.	MAX.	AVERAGE
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Mating Force (Lbs.) (Per Contact)	0.445	0.477	0.463
Contact Withdrawal Force (Oz.) (0.008 Blade) 0.5 Oz. Min.	1.120	3.280	2.332
Insulation Resist. (5000 Meg's Min.) 600 VAC for 1 Min.	$>9\times10^4$	$>2\times10^6$	—
Contact Resistance (1 Amp)	5.240	6.670	5.639
GROUP 2			
C.R. After Vibration & Mechanical Shock	3.800	5.170	4.335
Contact Withdrawal Force (Oz.) (0.008 Blade)	0.710	2.930	2.065
Durability (50 Cycles)	3.800	5.200	4.379
Contact Withdrawal Force (Oz.) (0.008 Blade)	1.480	3.120	2.187
Insulation Resist. (5000 Meg's Min.) 600 VAC for 1 Min.	$>2\times10^6$	$>2\times10^6$	—
GROUP 3			
Initial Contact Resistance	4.750	5.900	5.106
After Corrosive Atmosphere	4.850	5.900	5.120

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PMI Creates a Rosy New Variety of Analog Switches

In the Linear Wonderland garden, one coat of BIFET covers a lot of CMOS whitewash

In Lewis Carroll's Wonderland, no one was more dreaded than the Queen. She dealt with anyone who crossed her path by ordering their beheading. The gardeners on her croquet court (the Two, Five and Seven from a deck of playing cards) were well aware of the risks.

"Would you tell me please," said Alice, a little timidly, "why you are painting those roses?"

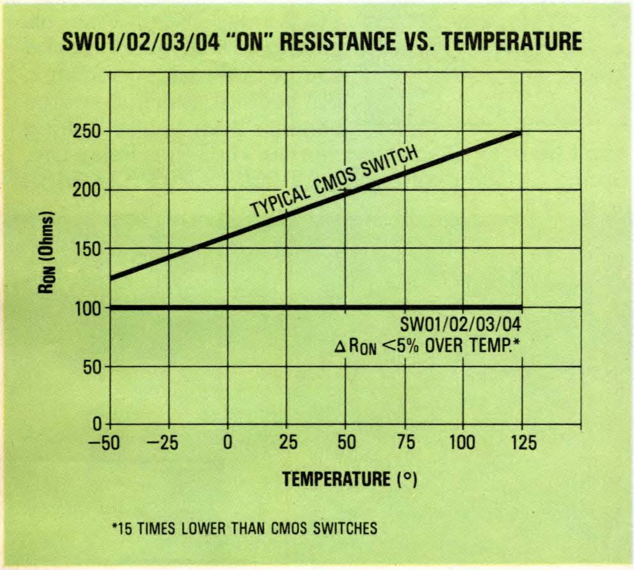
Two began, in a low voice, "The fact is, Miss, this here ought to have been a red rose tree and we put a white one in by mistake. If the Queen was to find out, we should all have our heads cut off."

In Linear Wonderland, engineers who pick their analog switches from the CMOS tree are often tempted to yell, "Off with their heads!," just as the Queen did when she found out her red roses weren't really red. What brings out the executioner instinct in every engineer are the thorny problems with "ON" resistance and voltage overload typical of CMOS analog switches.

When PMI decided to get into the analog switch market, we were determined not to lose our heads. So we looked at the best species of analog switches on the market and decided engineers would find them more attractive if they were grafted with PMI's proven BIFET technology, the same process used in our prized Multiplexer variety of circuits. It wasn't just a cover-up paint job, though; we started at the beginning and created something new: a family of Quad BIFET analog switches that fit the most popular CMOS pinouts but are more rugged electronically than CMOS can ever be.

Consider PMI's SW01/02/03/04. They're Quad BIFET analog switches with temperature-compensated R_{ON} coefficient (0.03%/°C), low R_{ON} vs. voltage (~4%) *and* a low absolute R_{ON} (100Ω maximum at 25°C). That's better performance than you get from CMOS, or even from the other BIFET switches on the market. In addition, you get low leakage (~0.2nA) and the protection against blowout that is inherent with PMI's BIFET technology.

ATTENTION DG201 USERS!



We didn't stop there, however. We know that most engineers are as forward-thinking as the White Queen in *Through the Looking Glass,* who told Alice her favorite things are those that happened the week after next. We kept going and developed the 7510/7511 analog switches which were designed to be pin-compatible with the well-known CMOS AD7510/11. These also eliminate the static discharge sensitivity in CMOS devices, improve leakage currents over temperature by two to five times, and there's no need for pull-up resistors to maintain TTL logic thresholds.

All in all, we think we've got the most beautiful Analog Switch Tree anywhere in Linear Wonderland. To prove it, we'd like you to use the coupon for your "BLOOMIN' SWITCH SAMPLE."

You'll find out that those CMOS guys don't have enough paint in their buckets to gloss over the advantages of PMI's Quad BIFET analog switches. The next time they try, you'll know what to say.

"Off with their heads!"

If someone beat you to the coupon, write to us for your sample. Or circle **#250** for literature.

SW01	—Normally ON, no disable. (Pin compatible to both DG201 and LF11201.)
SW02	—Normally OFF, no disable. (Pin compatible to the LF11202.)
SW03	—Normally ON, with disable.
SW04	—Normally OFF, with disable.
SW7510	—Normally OFF. (Pin compatible with the AD7510.)
SW7511	—Normally ON. (Pin compatible with the AD7511.)

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1500 Space Park Drive
Santa Clara, California 95050
(408) 246-9222 TWX: 910-338-0528 Cable: MONO

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Precision Monolithics, Incorporated
c/o Bourns Ag
ZUGERSTRASSE 74, 6340 Baar, Switzerland
Phone: 042/33 33 33 Telex: 78722

Check the box for the "BLOOMIN' SWITCH SAMPLE" you'd like to have.

☐ SW01—Normally ON, no disable. ☐ SW02—Normally OFF, no disable.
☐ SW03—Normally ON, with disable. ☐ SW04—Normally OFF, with disable.
☐ SW7510—Normally OFF. ☐ SW7511—Normally ON.
I am now using: ☐ DG201 ☐ HI201 ☐ LF11201 ☐ LF11202

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Series MA DPDT Dry Circuit to 2A	130	1,560	2.00
Series MS DPDT Dry Circuit to 2A	60	11,000	4.00

MM-5: THE COST-EFFICIENT COMMERCIAL ALTERNATIVE

Our MM-5 Series of TO-5 relays offers the commercial TO-5 user an opportunity to select a new and completely different alternative for his non-military, high performance application. The MM-5 is not only cost-effective through the use of extensive automated assembly techniques, but has less internal parts, thereby increasing its performance characteristics and reliability curves.

And that's two good reasons to think twice about your next TO-5 relay order. After all, getting a really good second source is always a good idea. But getting better first-source benefits than you're getting now can't be beat. Discover a winner: Hi-G Inc., Relay Div., 580 Spring St., Windsor Locks, CT 06096; 203/623-2481.

For more information, Circle No 5

Edited by Joan Morrow

News Breaks

VOICE INPUT CONTROLS CONSUMER EQUIPMENT

Taking remote control to its logical conclusion, Toshiba America Inc (New York, NY) introduced voice-actuated stereo and television units at last month's Consumer Electronics Show in Las Vegas. Prototype units indicate that the first generation will be speaker-dependent devices — a user must train them to recognize the actual controlling voice — with three operating modes: Register (for training), Recognition (for voice-actuated operation) and Manual (providing conventional use of the equipment).

An 8-bit μP controls the Acoustic Remote Control System, matching the characteristics of the user's voice to the digitized patterns stored in the Register mode. The stereo system recognizes 17 words that perform 21 different operations, such as "power on" and "power off." The TV recognizes 30 words, covering power, volume and channel selection.—ET

256k BUBBLE-MEMORY DEVICE SPORTS A 1.1-IN.-SQUARE FOOTPRINT

Users and evaluators of bubble-memory devices now have another source for these versatile components. National Semiconductor (Santa Clara, CA) now offers sample quantities of its Model MBM2256 ($500 (1-4)) and a companion evaluation board (NBS100, $1300).

When operating with a 100-kHz clock, the bubble memory specs a 7-msec average access time and a 100k-bps data rate. Its dual block-replicate architecture consists of 282 loops, each 1024 bits long (256 of these loops store data, six hold an error-correcting code and one stores the device's redundancy map). Chip size measures a trim 300 × 320 mils, and the unit's 16-pin dual-in-line package features a 1.1 × 1.1-in. footprint.

Four support chips are planned: The INS82851 controller will be available late this year, while the DS3615 function driver, DS3616 coil driver and DS3617 sense amplifier will all be introduced this summer.—WP

LAMP OUTSHINES STANDARD LEDs, OUTLIVES INCANDESCENTS

General Instrument's Optoelectronics Div (Palo Alto, CA) provides a cost-effective ($0.95 (1000)) solid-state alternative to incandescent backlighting with its Illuminator line. These advanced LED lamps backlight panels measuring up to 1 × 1-in. and feature more than 10 times the available light of a standard high-efficiency LED lamp.

Devices are available in yellow or orange; the orange version can be filtered to produce a high-efficiency red version. Employing two GaAsP/GaP chips wired in series, the lamp handles ½W of input power at 4.5V, dissipating heat through its large copper leads.—WT

MAGNETIC-TAPE HEAD FURNISHES 18 TRACKS AND DOUBLED DENSITY

Two heads aren't always as good as one, especially if the one is Nortronics' 18-track device. Besides doubling the standard number of read/write tracks, the head can also record as many as 20,000 flux reversals per inch (frpi), compared with a 9-track head's 9042 frpi. This design provides backward compatibility (it can read 9-track tapes), and when writing new tapes, it reduces the conventional 44-mil track width to 14 mils.

So far, no tape drives are available with the new head, but the Minneapolis, MN-based firm is delivering the devices in engineering-prototype quantities (final pricing has not been set). The company expects the high-density heads to find their way into drives that provide large quantities of archival backup for disc systems — to name one obvious application.—ET

"MINIATURE" DESCRIBES MODULAR SWITCHERS' SIZE AND PRICE

Small (4 × 1.5 × 9 in.) SB Series modular switching supplies fit comfortably into 5-in. racks for use in microcomputer and instrumentation applications. The KEC Electronics (Torrance, CA) supplies are available in six versions, ranging in output from 30 to 300W. OEM pricing begins at $141 (100) for the 30W model and reaches $355 (100) for the premium unit.—CW

HIGH GOLD COSTS SPUR FURTHER PRICING CHANGES

The fluctuating price of gold continues to wreak havoc in the electronics industry (News Breaks, January 20, pg 14), and at least two more manufacturers have had to re-evaluate their pricing schedules.

All RCL rotary switches and UID slide, pushbutton and rocker switches ordered from AMF Electro-Components Div (Hollywood, FL) will include a gold and/or silver surcharge, calculated on the basis of the New York price on the day of shipment. Prices quoted on these products had been predicated on gold's price not exceeding $200 per ounce and silver's staying below $15 per ounce. The surcharge base, therefore, rests on those prices.

Meanwhile, the Sibley Co, a Haddam, CT manufacturer of pc boards, approaches the gold-price problem in a different way: It will supply on its quotations both the unit price and the gold cost on which that price is based. In addition, the firm will indicate the effect on the unit price for each $20 change, both upward and downward, covering a $40 gold-cost range.

In a related move, General Electric Co (Stamford, CT) has announced a 10% list-price increase on all its high-current SCRs (devices 55A and higher, and 25A power modules) and also on rectifiers in the 100A and higher range. The firm attributes the hike to the unprecedented prices, not only of gold and silver, but also of copper, silicon and tungsten.—JM

PRINTER VENDOR WINS GSA APPROVAL

The General Services Administration (GSA) has recognized Digital Associates Corp (Stamford, CT) as an approved vendor of medium- and high-speed band printers for minicomputer applications. Several of the firm's units, including 300-, 600- and 900-lpm printers, now hold GSA approval.

Digital Associates claims it can provide band-printer users with 30 to 50% savings on printer list prices for either original purchase or system upgrading.—JM

PC-BOARD-TESTER MAKER ENTERS DEVICE-TESTER MARKET

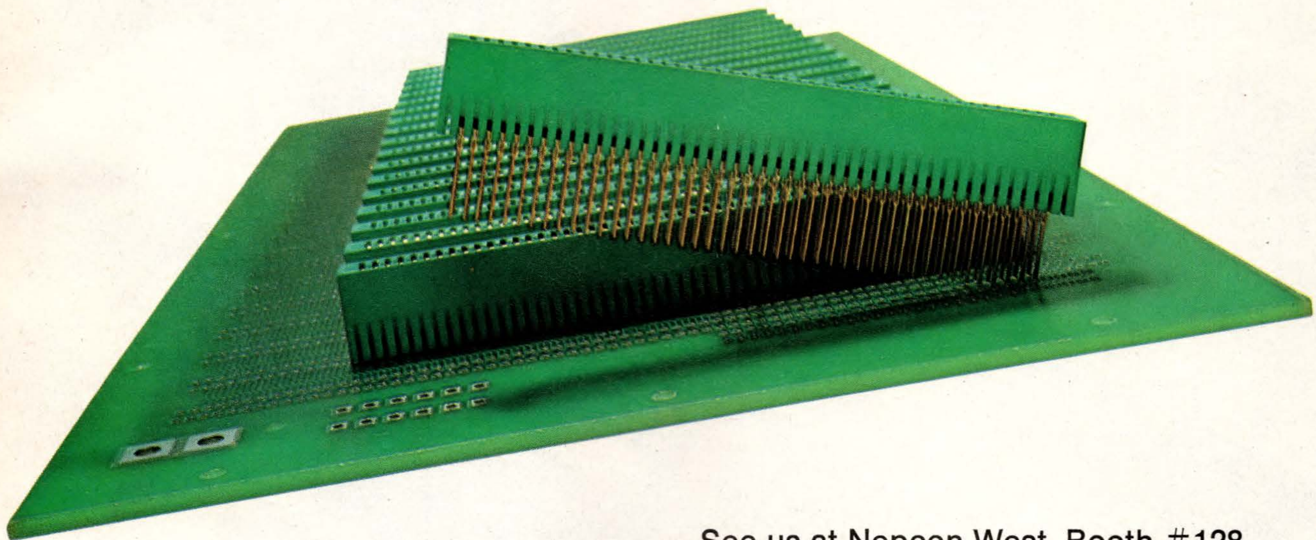
Expanding from its current pc-board-tester product line, GenRad Inc (Concord, MA) has established a subsidiary that will develop test systems for semiconductor manufacturers and users and testing labs. GenRad Semiconductor Test Inc will be located in Santa Clara, CA; its products will permit VLSI testing of MOS and bipolar devices. Brian Sear, current manager of venture development at the parent firm, will serve as president and general manager of the 80%-owned subsidiary.

In an unrelated development, another GenRad subsidiary has announced complete hardware and software support for the RCA 1802 microprocessor on its universal development systems and networks. GenRad/Futuredata (Culver City, CA) says its 2300 Series systems can now perform 1802 program execution and in-circuit emulation in concert with RCA's Cosmac Micromonitor; software development for the μP occurs by means of an operating system that features a file manager, CRT-based editor, 1802 relocatable macroassembler and linkage editor.—JB

FRANCHISE PROGRAM INCLUDES COMPUTER-SALES TRAINING

Planning to franchise 100 retail showrooms for commercial computer equipment over the next 2 yrs, MicroAge Computer Stores Inc (Tempe, AZ), a newly formed subsidiary of The Phoenix Group Inc, expects intensive sales training to play a key role in its success. Each franchisee, therefore, will attend more than 100 training hours at the MicroAge Learning Center.—ET

Building Backpanels? Elco's discrete press-fit card-edge connectors make it easier.



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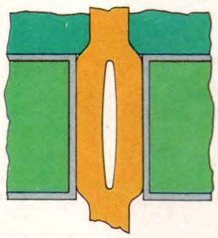
Lower costs

Elco's pre-assembled, press-fit card-edge connectors insert with simple tooling, and require low insertion forces due to a compliant press-fit section on the contacts. They achieve both mechanical stability and a reliable gas-tight electrical connection in one operation, without the use of solder, screws, or other fastening devices. This results in lower installation costs.



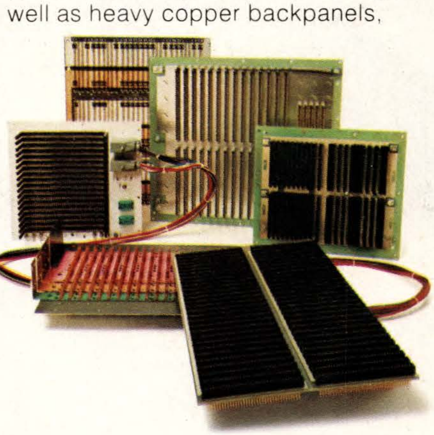
Since much circuitry can be etched on a Printed Circuit Board backpanel, wire wrapping can be dramatically reduced or even eliminated. When wire wrapping is required, Elco's discrete press-fit card-edge connectors make it easier because the PC board places the connector tails in a known position.

The discrete advantage

Now the advantages of a press-fit connector are available with no need to cut insulators and reels of contacts. Elco offers immediate delivery on one-piece connectors of any length up to 50 pairs, with a .100 x .200 grid pattern. Other grid patterns will soon be available. The standard finish is 20μ" gold, selectively plated over 50μ" nickel. However, other plating thicknesses and overall plating are available.

Total Interconnect Package

Of course, Elco will be pleased to build your backpanels for you. Our capabilities extend into a broad range of press-fit, metal plate and card-edge connectors, as well as heavy copper backpanels, sophisticated multilayer and aluminum backpanels and backpanel systems—all assembled to your specifications. For more information, call or write:



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Interconnect Systems Division
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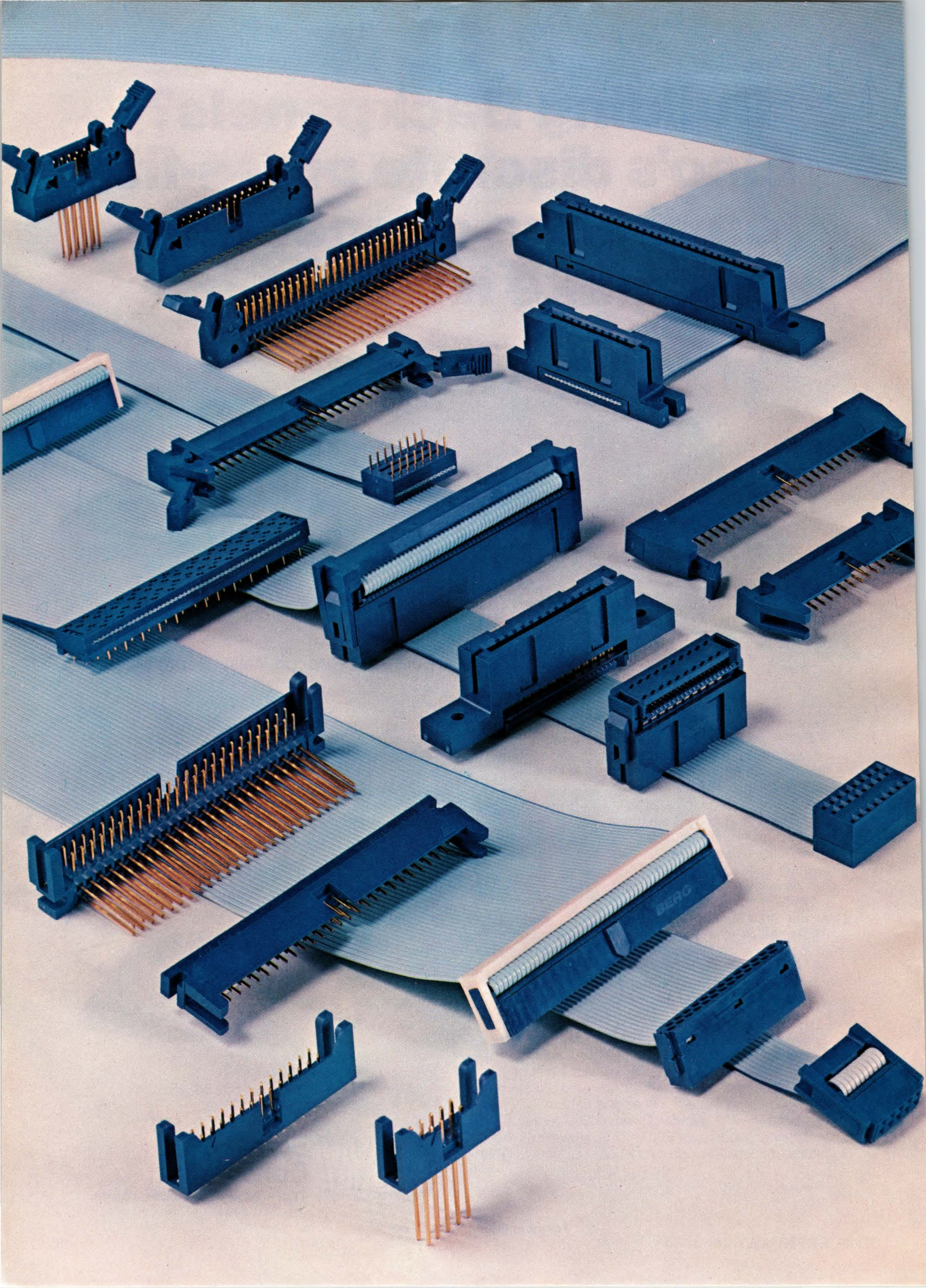
BERG

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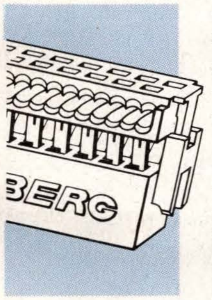

• Cable slot designed to precisely position conductor for reliable termination, higher yields.

• Sight holes in cover permit visual inspection before and after assembly assuring proper cable alignment.

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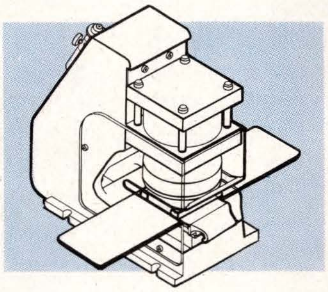

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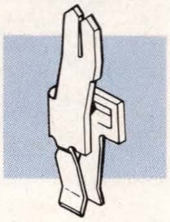

2. Dual-beam contact assures redundant positive pin connection, even when subjected to vibration.

3. High-strength plastics withstand severe environments.

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*Du Pont's trademark for its mass termination connectors, cable, presses and accessories.

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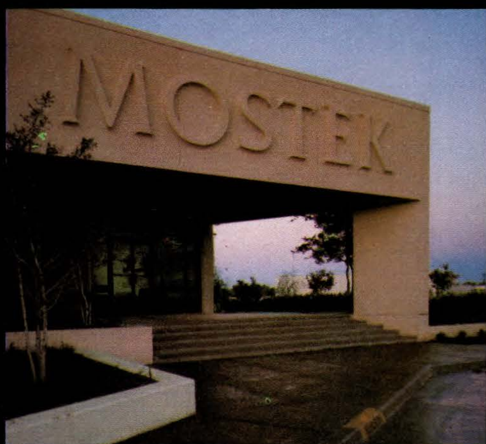
Not a destination.

—Ben Sweetland



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Signals & Noise

Stamp out discrimination

Dear Editor:

Far be it from me to disagree with Irwin Feerst (EDN, November 20, 1979, pg 27) that educators and corporate executives benefit when engineers produce cheaper and more copious output. They do. But that fundamental relationship is in no way the fault of our skilled colleagues who happen to have been born and educated in Bombay, Hong Kong, Cairo or Manchester.

By all means, dump tyranny into Boston Harbor. But let us be extra careful so as not to topple a great statue into New York Bay.

Unions have virtues and faults. If a long-overdue, serious engineers' association ever arises in our country, one hopes that it will embody some of the virtues and avoid a fault or two.

The cheap and easy route of discrimination on the basis of anything other than competence and solidarity leads to the very tyranny we decry. And blaming an immigrant minority for our ills only serves the interests of those we challenge. Let us rather address the problem at its source, which Feerst so ably recognizes.

Sincerely,
Sholom Kass
Staff Engineer
Barrett Electronics Corp
Mt View, CA

Who's to blame?

Dear Editor:

Although I agree with Irwin Feerst in his November 20, 1979 Signals and Noise rebuttal regarding the threat of foreign engineers, I still wonder who's to blame for engineers' plight.

Many engineers have sat back and waited for their employers to take care of them and give them their just due. But in many cases, engineering management is an engineer's worst enemy.

Actually, engineers really shouldn't complain. As I see it, they are getting exactly what they deserve.

Anonymous

PS: I prefere not to sign this letter because if I get fired, there are at least three engineers (or near engineers) ready to take my high-paying job for even less money.

For more information...

Dear Editor:

The corrected address for H C Electronics, which was included in your list of voice - I/O - equipment manufacturers (EDN, November 20, 1979, pg 167) should read: 250 Camino Alto, Mill Valley, CA 94941.

Yours truly,
Rob Rank
Media Coordinator
Hamilton Industries

Another voice heard

Heuristics Inc has sold almost 10,000 voice-recognition units as peripherals to Apple, S-100-bus and TRS-80 computers. For information on the firm's Speechlink H2000, H-1600 voice controller or other products, contact it at 1285 Hammerwood Ave, Sunnyvale, CA 94086. Phone (408) 734-8532.

Your turn...

EDN welcomes your comments, pro or con, on any issues raised in the magazine's articles. Address letters to **Signals and Noise Editor, EDN, 221 Columbus Ave, Boston, MA 02116.** Names will be withheld upon request. We reserve the right to edit letters for space and clarity.

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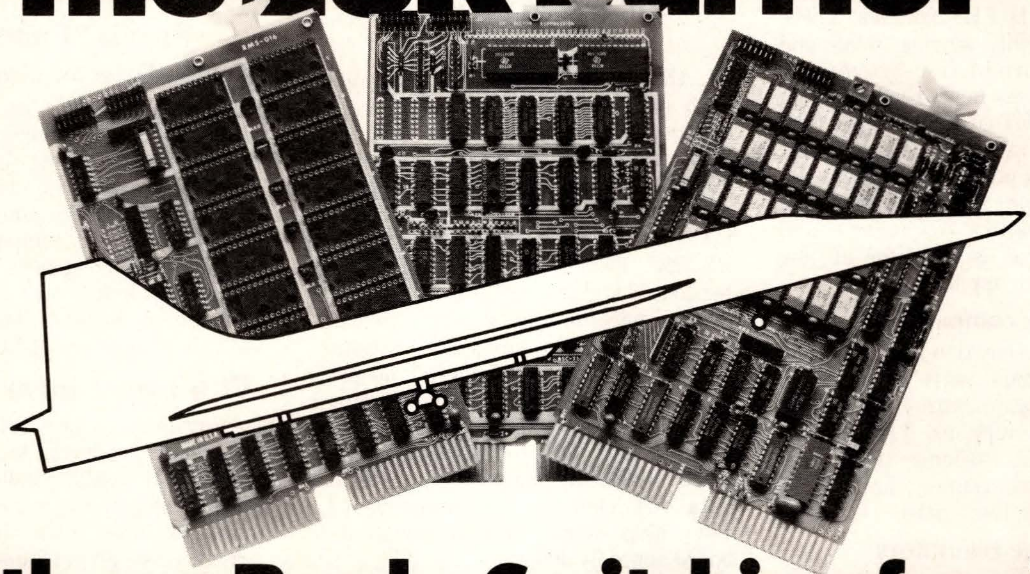

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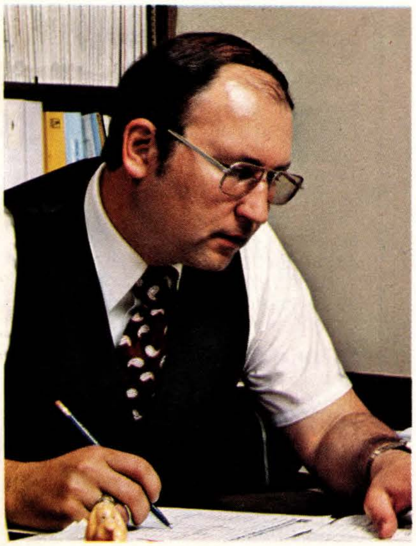
Editorial



A golden opportunity

Economists have observed that precious metals are never consumed like other natural resources; rather, they're continually recycled into new products. Imagine, then: The ring on your finger could have once been part of Julius Caesar's favorite wine goblet.

The madness in today's gold and silver markets supports this idea of recycled precious metals. And the lengths to which people are going to cash in on the markets' skyrocketing prices range from ingenious to humorous to just plain crazy. For example: Doctors are storing away old X-ray films for their heirs because of the films' silver content; people who formerly let their dentists keep old dental bridges when new ones were made are now demanding the old ones because of their gold content; scores of other people are selling to gold and silver dealers everything from heirloom jewelry to dental fillings.

The electronics industry, too, is feeling the adverse effect of rising precious-metal prices. But with a little ingenuity, perhaps this effect can become a positive one.

Think of all the old connectors, switches, relays, pc boards, transistors, integrated circuits, old instruments and old TV sets around—people are literally sitting on a gold mine, one that could lead to the biggest boom the industry will ever experience. For suppose some entrepreneur type starts a publicity campaign informing the public of the amount of gold that lies in electronic gear. If people are willing to sell their gold tooth fillings at today's prices, can't you see the masses queueing up just as readily at reclamation centers to sell old electronic equipment if prices continue to soar? The growth in the replacement-part/equipment business resulting from this action will be phenomenal—analogous to the much sought-after perpetual-motion machine.

Sounds farfetched, doesn't it? Well, it would have sounded just as crazy if 10 years ago, when gold cost just $35 an ounce, someone told you that the metal would go for $650 in January 1980.

So like the doctors saving old X-ray films, hunt up all those electronic parts. You can even give your sweetheart an old transistor next Valentine's Day. And about that $1000 selectively gold-plated edge connector just introduced....

Roy W. Forsberg

Roy Forsberg
Editorial Director

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1977 Contributed Series — Software Design Course
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1975 Staff-Written Series — Microprocessor Design Series

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Our thanks to the many readers who returned the circulation requalification card in the November 20, 1979 issue.
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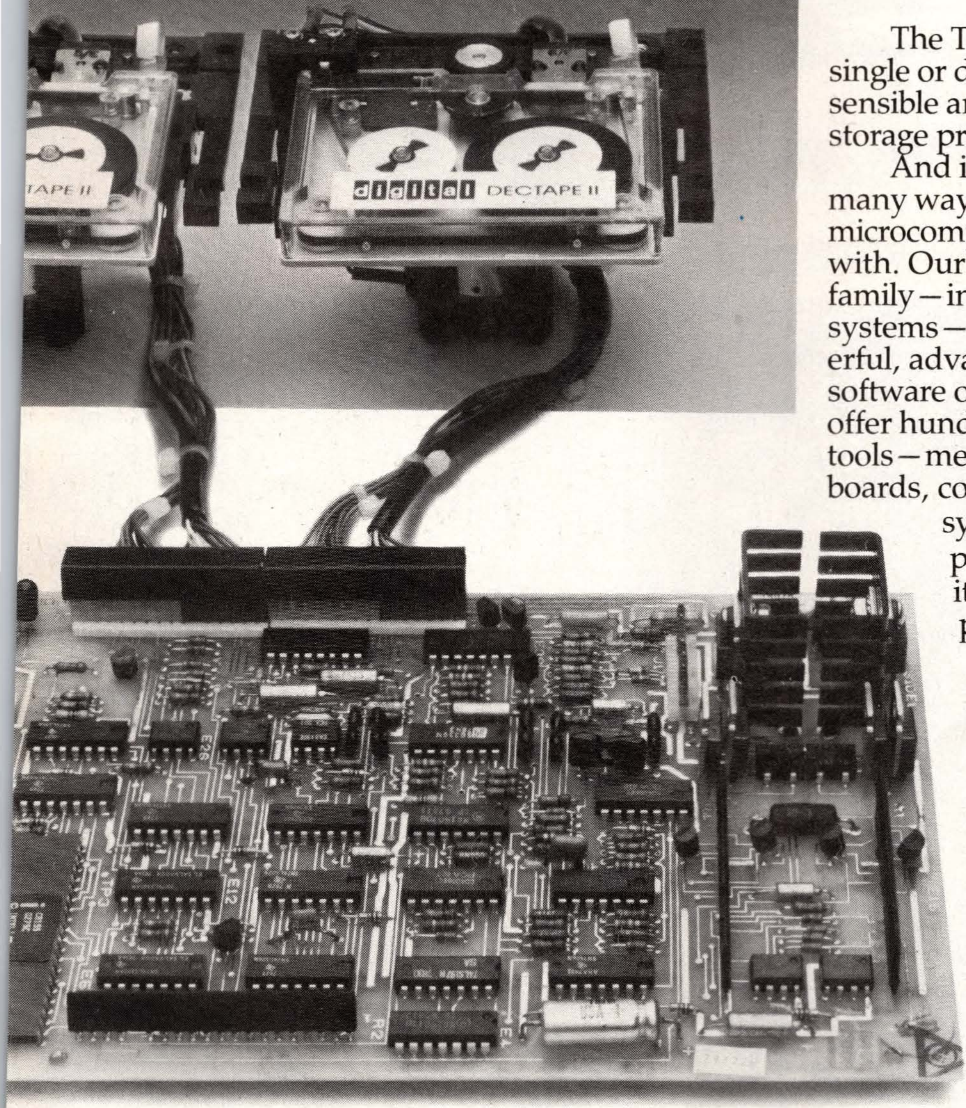
It costs like a tape, but thinks like a disk.



The TU58 cartridge tape, single or dual drive. It's the first sensible answer to micro mass storage problems.

And it's just one of the many ways Digital makes microcomputers easier to work with. Our 16-bit microcomputer family — in boards, boxes and systems — offers the most powerful, advanced and proven software on the market. We also offer hundreds of hardware tools — memory and interface boards, complete development systems, terminals and peripherals. And we back it all with over 11,000 support people worldwide.

It's the total approach to micros, only from Digital.

Digital's 512Kb TU58 cartridge tape subsystem. At $562 in 100's, it's priced like a tape device. But with random-access block addressing, and EIA serial interfacing, it's like no other tape drive on the market.

That's because the TU58's controller board has a built-in MPU that makes it think like a disk. It reads, writes and searches for data in blocks, instead of running serially through the whole tape like conventional systems. And the TU58's small size — the board measures just 5.2" x 10.4" (13.2 cm x 26.5 cm) — makes it easy to design into your product.

For more information, contact **Digital Equipment Corporation**, MR2-2/M70, One Iron Way, Marlborough, MA 01752. Or call toll-free 800-225-9220. (In MA, HA, AL, and Canada, call 617-481-7400, ext. 5144.) Or contact your local Hamilton/Avnet distributor.

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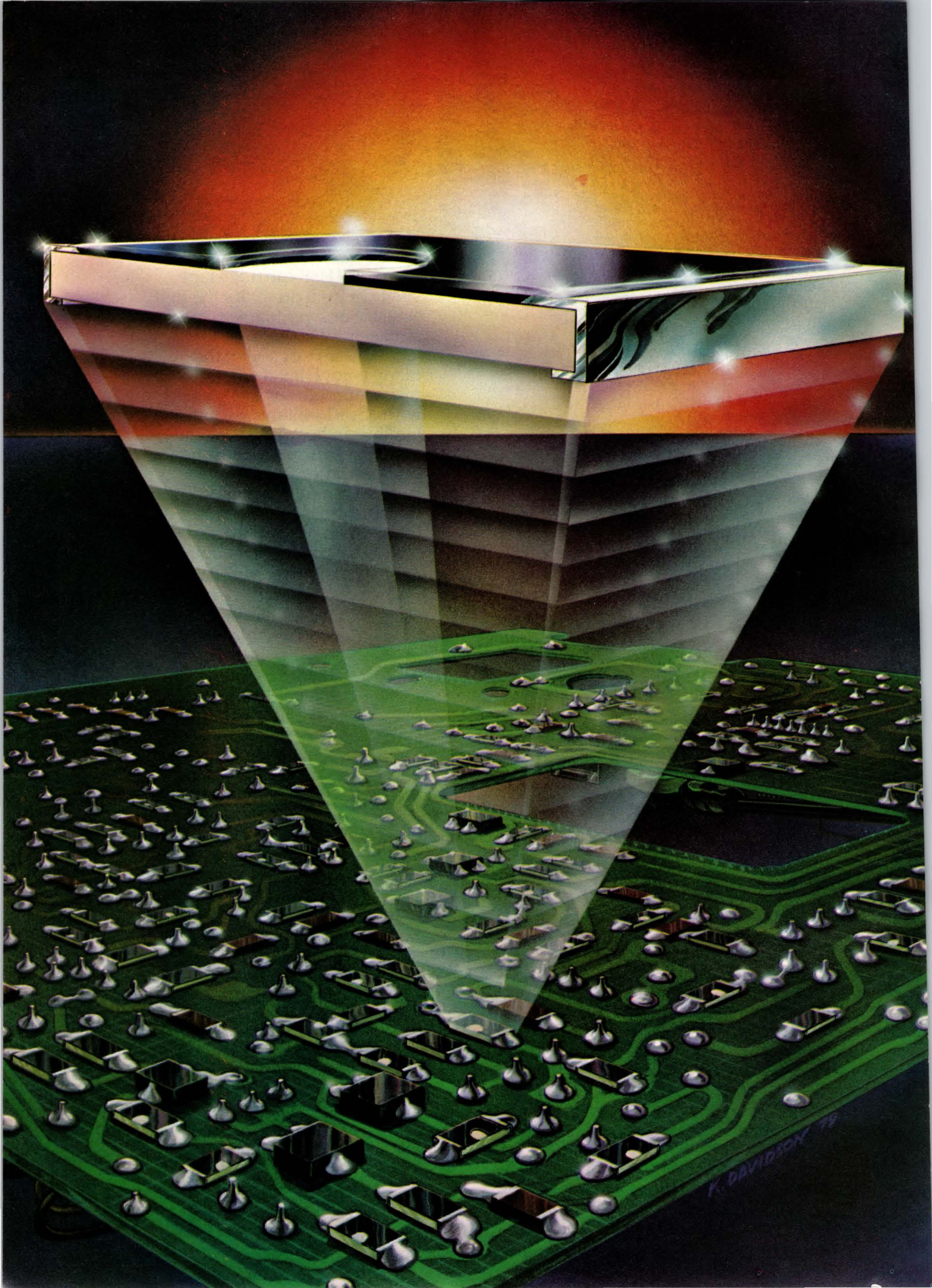
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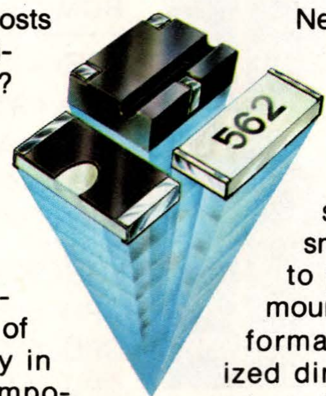
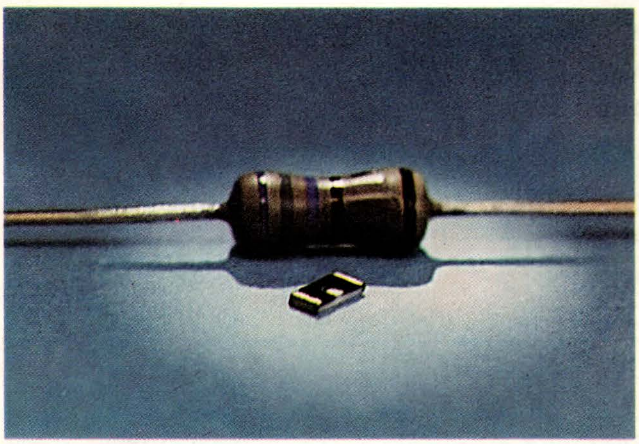
Now you can slash your assembly costs and create thinner, smaller, more reliable products at the same time. How? With our new flow-solderable resistor and semiconductor chips.



Start using both sides of your PC boards

Hundreds of these new chip components can be attached to either side of your PC boards in seconds. Already in widespread use in Japan, these components have fostered the development of high-speed magazine loading and tape and reel attachment methods. Once attached, the chips can be flow-soldered along with axial or radial-leaded components. Together, these developments are making dramatic reductions in assembly and labor costs possible.



Nearly 200 chip resistors (1/16W) can be mounted in just four square inches. This great density, coupled with the fact that the chips can be mounted on both sides, drastically reduces PC board size. The end result is thinner, smaller, lighter products that cost less to produce. In addition, the ability to mount chips opposite IC's provides performance improvements. And, standardized dimensions are making board layout and product design faster and more straightforward.

Make a solid connection to reliability

Flow-soldering directly to the chip instead of to leads provides a solid, more dependable connection — a connection you can trust even in the most severe environments.

R-Ohm already offers a wide variety of dependable chip components. Chip resistors are available for 1/16, 1/8 and 1/4W applications with 2%, 5% and 10% tolerances over a wide range of ohmic values. Chip transistors and diodes are offered for a variety of functions and applications. Many more components are on the way.

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For more information, Circle No 14

Leadtime Index

ACTIVE COMPONENTS

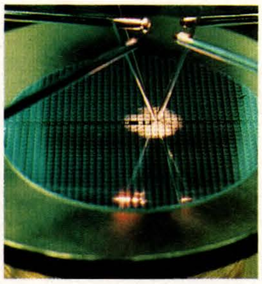
PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
DISCRETE SEMICONDUCTORS			
Diode, switching	4	8	=
Diode, zener	4	9	=
Rectifier, low-power	4	6	=
Rectifier, power	1	4	=
Thyristor, low-power	6	10	up
Thyristor, power	7	16	=
Transistor, bipolar power	8	15	=
Transistor, bipolar signal	8	20	=
FET, power	8	20	↓
FET, signal	8	24	↓
Transistor, RF power	10	35	↓
DISPLAYS			
Fluorescent	8	12	=
Gas-discharge	3	12	=
Incandescent	14	19	=
LED	14	20	up
Liquid crystal	5	16	up
Plasma panel	8	16	=
ELECTRON TUBES			
CRT, black and white TV	7	12	=
CRT, color TV	5	9	=
CRT, industrial	8	17	=
Industrial power	13	25	=
Light and image sensing	4	7	=
Microwave power	15	20	=
INTEGRATED CIRCUITS, DIGITAL			
CMOS	16	36	=
Diode transistor logic (DTL)	12	20	=
Emitter-coupled logic (ECL)	12	20	=
Low-power Schottky TTL	32	52	=
Standard Schottky TTL	28	40	up
Standard TTL	22	36	up
INTEGRATED CIRCUITS, LINEAR			
Communications circuit	16	28	=
Data converter	10	21	=
Interface circuit	8	15	up
Operational amplifier	9	19	=
Voltage regulator	10	20	=

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
MEMORY CIRCUITS			
EPROM	7	15	↓
PROM, bipolar	20	36	=
RAM, bipolar	7	16	=
RAM, CMOS	6	9	=
RAM, 4k MOS dynamic	10	14	=
RAM, 16k MOS dynamic	18	27	=
RAM, 1k MOS static	8	16	=
RAM, 4k MOS static	8	14	=
ROM, masked MOS	15	18	=
MICROCOMPUTER/MEMORY SYSTEMS			
Core memory board	8	12	=
IC memory board	6	12	=
Interface board	9	17	=
Microcomputer board	7	12	=
MICROPROCESSOR IC'S			
CPU, bipolar bit slice	6	17	=
CPU, 4-bit MOS	9	18	=
CPU, 8-bit MOS	13	20	=
CPU, 16-bit MOS	8	14	=
Peripheral chip	9	18	=
OPTOELECTRONIC DEVICES			
Coupler and isolator	4	10	=
Discrete light-emitting diode	4	13	=
PACKAGED FUNCTIONS			
Amplifier, instrumentation	8	11	=
Amplifier, operational	8	12	=
Amplifier, sample/hold	4	13	=
Converter, analog/digital	6	12	=
Converter, digital/analog	7	12	=
PANEL METERS			
Analog	14	27	=
Digital	15	23	=
POWER SUPPLIES			
Custom	14	27	=
Enclosed modular	10	16	up
Open-frame module	14	21	up
Printed circuit	12	16	=

Leadtimes are based on recent figures supplied to *Electronic Business* magazine by a composite group of major manufacturers and OEMs. They represent the typical times necessary to allocate manufacturing capacity to build and ship a medium-sized order for a moderately popular item. Trends represent changes expected for next month.

No compromise solutions.

The Tektronix S-3280 is the first test system specifically designed to test ECL, LSI devices. Every S-3280 has high-speed drivers, giving you a pulse source for every channel.



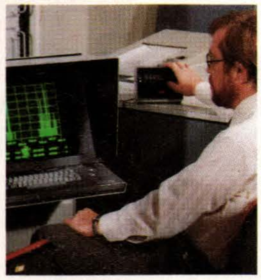
Precision fixturing allows you to connect the device to the tester with minimum signal distortion. And there are up to 64 channels of sampling for waveform analysis, ensuring high fidelity.

Flexibility.

Multiple pattern sources give you an effective, flexible means of implementing complex patterns. Choose the method of pattern generation that fits the device under test.

Compatibility.

Only one language to learn. All Tektronix S-3200 systems use TEKTEST, a test-oriented language very close to English. Your test engineers will quickly generate, edit, and debug device-testing programs.



Proven performance.

Semiconductor test systems are nothing new to Tektronix, we've been building them for years. In addition to the S-3280 ECL, LSI tester, there's the S-3270 for device characterization, and the S-3250 for production testing. Each has a 20 MHz clock rate. Our wide variety of options allows you to buy what you need now, and add to it anytime.

Training.

We'll support your test engineers with a comprehensive training program and thorough documentation.

Worldwide support.

We're a phone call away.

To find out which S-3200 system and its options best meet your needs, call your local Tektronix representative.

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COMMITTED TO EXCELLENCE

Another first from Tektronix. The high-speed solution for subnanosecond logic testing.

High-speed drivers.

Precision 50 ohm fixturing.

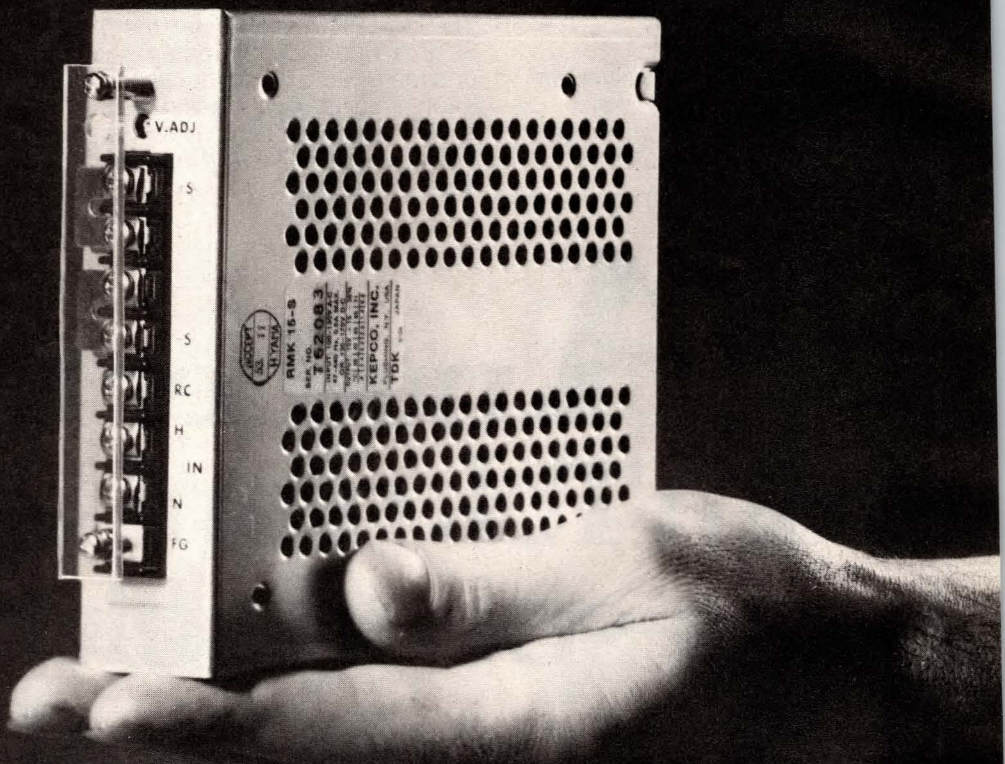
Waveform analysis.

We make moving ahead easy.

S-3280

think small

KEPCO/TDK switching power modules



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- HIGH EFFICIENCY SWITCHERS
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We can now offer a full line of ceramic, solid tantalum, miniature aluminum electrolytic, film, metallized polyester film, and stacked metallized film capacitors. One respected name, one quality source.

Siemens is the fifth largest electronics company in the world, producing some $700 million worth of components annually in more than 50,000 different configurations.

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In Canada: Siemens Electric Ltd., P.O. Box 7300, Point Claire, Quebec.

Specify Siemens and be secure.

For more information, Circle No 17

If you thought Panasonic only supplied 'lytics for TV...
FOR INDUSTRIAL APPLICATIONS
Z SERIES (Aluminum)
From 0.1µF to 2200µF and from 6.3 through 50 VDC. Axial or radial leads. Temp. range: −40°C to +85°C. Standard tolerance: ±20% (±10% available).
FOR CONSUMER APPLICATIONS
LS SERIES (Aluminum)
New Smaller Sizes From 0.47µF to 10,000µF and 6.3 through 100 VDC Axial or radial leads. Temp. range: −40°C to +85°C Standard tolerance: −10% to +50%.
ACE(W)
15
FOR HI-REL INDUSTRIAL APPLICATIONS
3H SERIES (Aluminum)
From 1µF to 1000µF and from 10 through 63 VDC Axial or radial leads. Temp. range: −40°C to +125°. Standard tolerance: ±20%.
FOR ALL HI-REL APPLICATIONS
4H SERIES (Aluminum)
Characteristics similar to our tantalum, but at lower prices. From 1µF to 220µF and from 16 through 63 VDC. Axial leads only. Temp. range: −70° to +155°C. Standard tolerance: ±20%.
CE
-70°~+150°C
ECE-B40X22
FOR GENERAL APPLICATIONS
SQ SERIES (Tantalums)
These solid tantalum capacitors provide high stability, good humidity characteristics and long life. They're available from 0.1µF to 220µF and from 3.15 to 50 VDC. Resin dipped radial leads. Temp. range: −55°C to +85°C. Standard tolerance: ±20% (±10% available).
FOR GENERAL APPLICATIONS
K SERIES (Aluminum)
Tantalum performance with no sacrifice in size. From 0.1µF to 100µF and 6.3 to 63 VDC. Temp. range −40°C to +85°C. Standard tolerance ±20% (±10% contact factory).
A choice of packaging, too.
Panasonic offers you a wide line of aluminum and tantalum electrolytic capacitors, plus the flexibility of bulk, reel or tape packaging for axial and radial lead units, and lead forming or crimping for both axial and radial units. And they can be ordered from your local Panasonic distributor or our Secaucus headquarters. Panasonic Electronic Components, One Panasonic Way, Secaucus, NJ 07094. (201) 348-7270.
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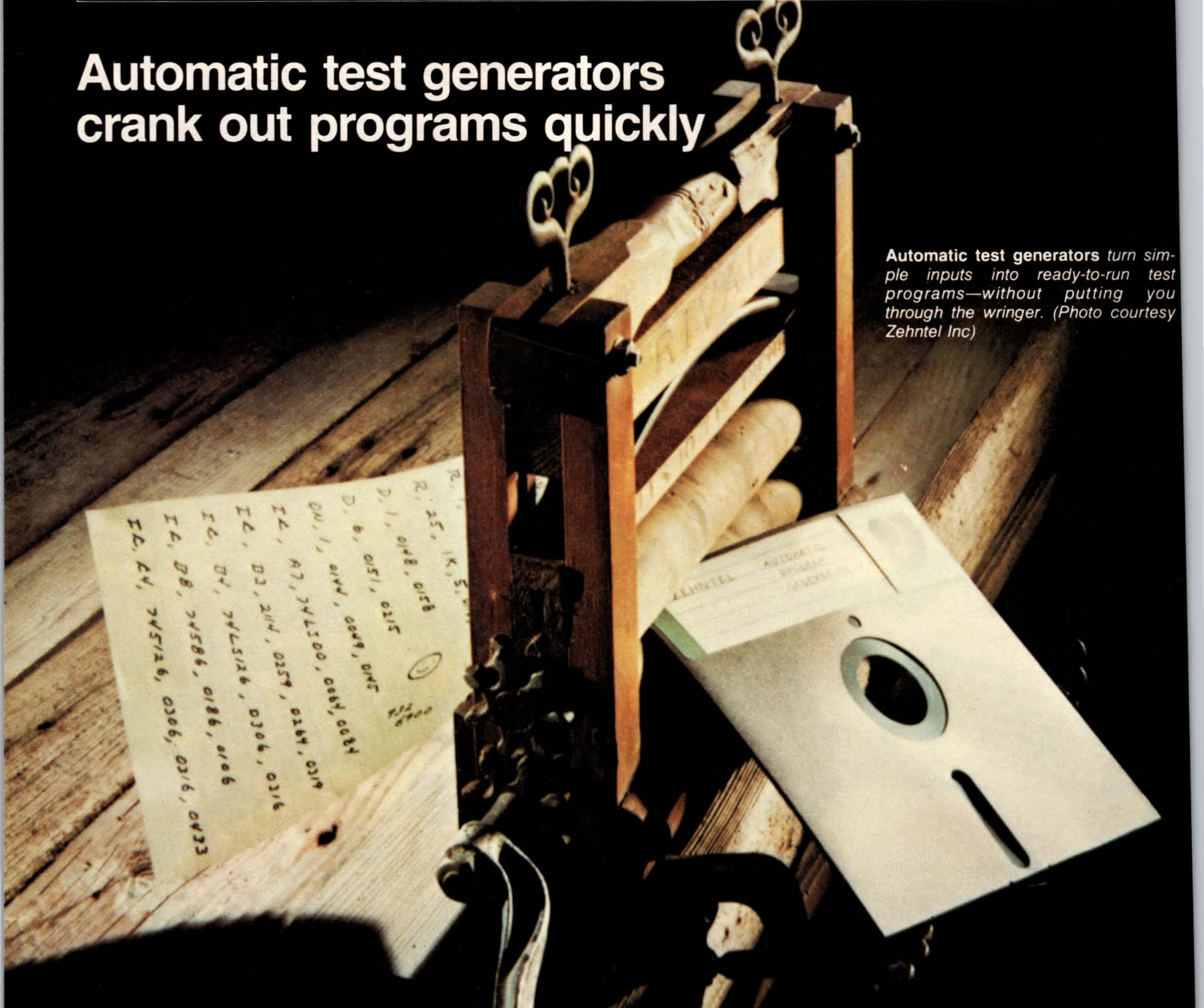
Technology News

Automatic test generators crank out programs quickly



Automatic test generators *turn simple inputs into ready-to-run test programs—without putting you through the wringer. (Photo courtesy Zehntel Inc)*

Andy Santoni, Western Editor

Automatic-test-equipment makers have developed versatile hardware and software packages that help cut the time and cost involved in writing programs to test devices and pc boards. The advantage provided by such combinations is no small matter: The cost (in programming time, hence in programmers' charges) to amass a library of tests for all devices and boards a company utilizes can easily outstrip the cost of even the most expensive ATE system, which in turn can run more than $1 million.

The most complex — and expensive — of the automatic-test-generation (ATG) programs help check out LSI devices. "In the days of SSI and MSI, it was still practical to write ONEs and ZEROs by hand," says Keiji Muranaga, technical director at Fairchild Test Systems Group. But today's LSI and VLSI devices require huge numbers of test patterns and precise control of timing parameters; an automatic test generator must thus develop and keep track of all the necessary data.

Fairchild's approach to ATG is LEAD — Learn, Execute And Diagnose. With the help of this software, you write inputs to a device under test in that device's assembly-language mnemonics, rather than tediously producing columns of

ONEs and ZEROs. And you can also devise a language to generate input test vectors for peripheral chips and nonintelligent devices without assembly languages of their own.

Once the inputs are written, you utilize a known-good device operating in a "friendly" environment to generate a set of "good" responses. Testing of devices in worst-case or true operating environments then proceeds by comparing the devices' responses with those of the known-good unit.

This technique leaves the definition of "good device" up to the user, explains Muranaga. It can merely be one that has worked well in a breadboard system, or one that has undergone extensive functional and parametric testing to verify that it meets all data-sheet specifications and any special requirements.

For complex devices, Muranaga claims, LEAD can cut total program-generation time from 6 to 2 or 3 months.

Simpler tests get help

While LSI devices benefit most from automatic test generation, even SSI- and MSI-device program generation can profit from software help, says Ken Lindsay, product marketing manager at Tektronix's Measurement Systems Div. This firm's computer - aided program-generation package helps cut software-writing time for relatively simple devices from a half-day to a half-hour.

With the Tektronix package, you tell the system a device's family and type and provide (in response to prompts) a pin list and the applicable parameters of forcing functions and output measurements. Software then generates the instructions the test system's computer requires to test the device for functionality, as well as dc voltages, currents, rise and fall times and propagation delays.

Such an ATG package saves time because it stores parameters common to all members of a device family, such as the minimum and maximum levels for input and output signals from TTL gates. Thus, you needn't enter these values into each program you write, but you *are* free to alter them to meet special requirements.

Computer-aided program-generation software *provides the skeleton for testing high volumes of relatively simple SSI and MSI devices on Tektronix ATE systems, such as Model S-3250.*

While Tektronix's package is aimed specifically at simplifying test generation for incoming inspection of SSI and MSI parts, it can also be extended to other applications and more complex devices, says Lindsay. It complements Tektronix testers whose prices start at more than $100,000 and run to $1 million.

Board-test writing grows easier

While it might be simpler to write test programs for pc boards than for LSI devices, pc-board testers can also profit from program-generation aids, says Ray Turner, manager of simulation systems at Computer Automation's Industrial Products Div. Thus, this firm recently introduced its Capable 4814 automatic - test - generation and logic-simulation system, a $110,000 hardware and software package that can cut the average test-program - generation time for a 75-IC pc board from a week or two to less than a day.

The Capable 4814 analyzes a software model of a circuit board, calculates a list of conditions under which the board might fail and generates programs to test for these faults. Older ATG programs used for this purpose employ a single algorithm to select a fault pattern from a table of undetected faults, determine a path that propagates the fault to the edge connector (where the tester can observe a failure) and generate a stimulus to drive the fault along that path. (The algorithm might be a backtracking technique from the card edge to specific nodes, or it might involve path sensitization from the node outward.) By contrast, the Capable 4814 can try as many as four different algorithms to guarantee that any fault on the board propagates to the edge connector and is detected.

The ATG system employs functional gate and flip-flop models and I/O tables for larger scale devices to determine how a signal propagates along a path. It's complex, and thus memory intensive: The 4814 incorporates a Naked Mini CPU with 320k bytes of memory, a 256k-byte floppy-disc drive and a 10M-byte dual-moving-head rigid-disc drive.

Iterations automatic

Another board - test - generation system, Teradyne's Model LF780,

Learn, Execute And Diagnose (LEAD) *software simplifies writing programs for complex device testing on Fairchild's Sentry ATE systems.*

employs a Digital Equipment Corp VAX-11/780 CPU with 500k to 1M bytes of memory, expandable to 8M bytes. This system can handle as many as eight rigid-disc drives, each storing 176M bytes.

Software for the LF780 comprises the LASAR test - generation language, developed in the early '70s by Digitest Corp, Dallas, TX. (Teradyne acquired Digitest in June 1978.) The language's latest version includes an Automatic LASAR Executive Control, which places all of LASAR's subsystems under a single control to permit automatic iterations of pattern - generation tests. (In older versions, a test engineer had to operate the system's software modules individually; iterations were painstaking.)

To supplement this automatic pattern generation, though, a Manual Pattern Processor permits the user to write patterns by hand at any time during a LASAR sequence.

Virtually painless programming

Programming Teradyne's L529 in-circuit automatic test system can prove even simpler than using the LF780. This system employs a "self-learning" technique to determine the values of components on a board and to set tolerance limits on those values.

To generate an in-circuit test program that checks for the proper part and orientation at each location on the board, you key in a list of all components connected to each node. The tester then makes resistance and impedance measurements at each node on a known-good board and stores the results. As more known-good boards run through the system, it alters its program to adjust the median value and tolerance band for each measured quantity whenever a new measurement differs from previous data.

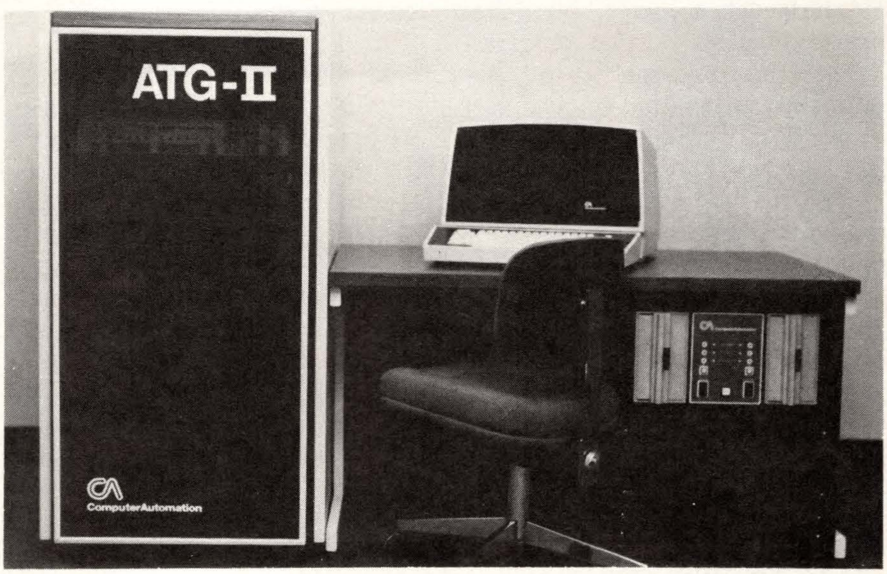
Specifically, the test system first assumes a "default" tolerance of 5% for each measurement. But the wider the variation a functionally acceptable board can have, the wider the tolerance the tester places on that measurement. In the end, tolerance can reach 40% or more.

Note the limitations

Despite the advantages of this approach, using a known - good board to generate test programs also has drawbacks, says Karl Knight, product applications manager at Zehntel. Specifically, the board chosen as representative might not be. Thus, Knight prefers to program a tester against a board's schematic, rather than with respect to a known-good unit.

Zehntel employs its test station's own processor and floppy disc to generate such test programs. You tell the machine what components are between each pair of pins on the pc board, and you determine where to locate the tester's probe pins. The tester then checks that all pins are actually in place on the test fixture and that all nodes in the test program are available on one pin or another.

You can install the probe pins so that they correspond to convenient



Off-line test-program generation *permits writing programs while a tester is used full-tilt for production tasks. This Computer Automation Capable 4814 program-generation station helps write functional board tests.*

points on the board's schematic, but this approach often leads to a bird's nest of wiring in the fixture that's hard to troubleshoot, says Knight. As a better alternative, you can position the pins at random but convenient locations in the fixture and wire them neatly to the fixture's interface connector. Then you examine each connection of each device on the board, and the machine determines at which fixture location that node is available.

Program generation in this case thus consists of walking through the node list on the board; the tester generates a program complete with such peripheral information as headings and power-on sequences. Debugging this program is the most time-consuming part of the job, but even so, the total test-generation process takes only about five working days, says Knight.

Off-line programming

There's yet another approach to test - generation simplification: Instead of using a test system itself for program generation—and perhaps tying up an expensive piece of equipment normally required on the production line—you can employ off-line programming stations like GenRad's Model 2290. (This station complements the company's Model 2270 in-circuit test system.)

An off-line system can quadruple in-circuit program productivity by allowing simultaneous program generation by up to four users, claims Ralph Anderson, test-systems product-line manager. As an additional benefit, off-line program generation can eliminate — or at least reduce — the need for programming new-board tests during second and third shifts (in many cases, the only times when a test system is not used for production testing).

The $50,000 Model 2290 includes a DEC CPU with 128k bytes of memory, expandable to 256k bytes; a Control Data Corp Hawk fixed-head disc drive provides it with 10M bytes of storage. One CRT terminal is standard; in addition to three more, options include an additional disc drive and line printers.

Simplifying programming

Hewlett-Packard's Model 3060A in-circuit tester utilizes an HP Model 9825A desktop computer. Thus, it, too, could function in an off-line manner—you could develop its programs on another 9825A normally used for other tasks.

The 9825A employs the HPL language, which borrows high-level commands from BASIC, FORTRAN and other languages and also makes use of formatted read/write commands to simplify data manipulation. The tester's Board Test Language extends HPL to further ease programming, adding 35 commands aimed specifically at board - testing applications. An in-circuit program-generation package then works from a board-topology list to generate and store the appropriate test program. **EDN**

Four programmers *can share this GenRad 2290 in-circuit test-generation station.*

For more information...

For more information on the automatic - test - generation products described in this article, circle the appropriate number on the Information Retrieval Service card or contact the following manufacturers directly.

Computer Automation Inc
Industrial Products Div
2181 Dupont Dr
Irvine, CA 92713
(714) 833-8830
Circle No 443

Fairchild Test Systems Group
1725 Technology Dr
San Jose, CA 95110
(408) 998-0123
Circle No 444

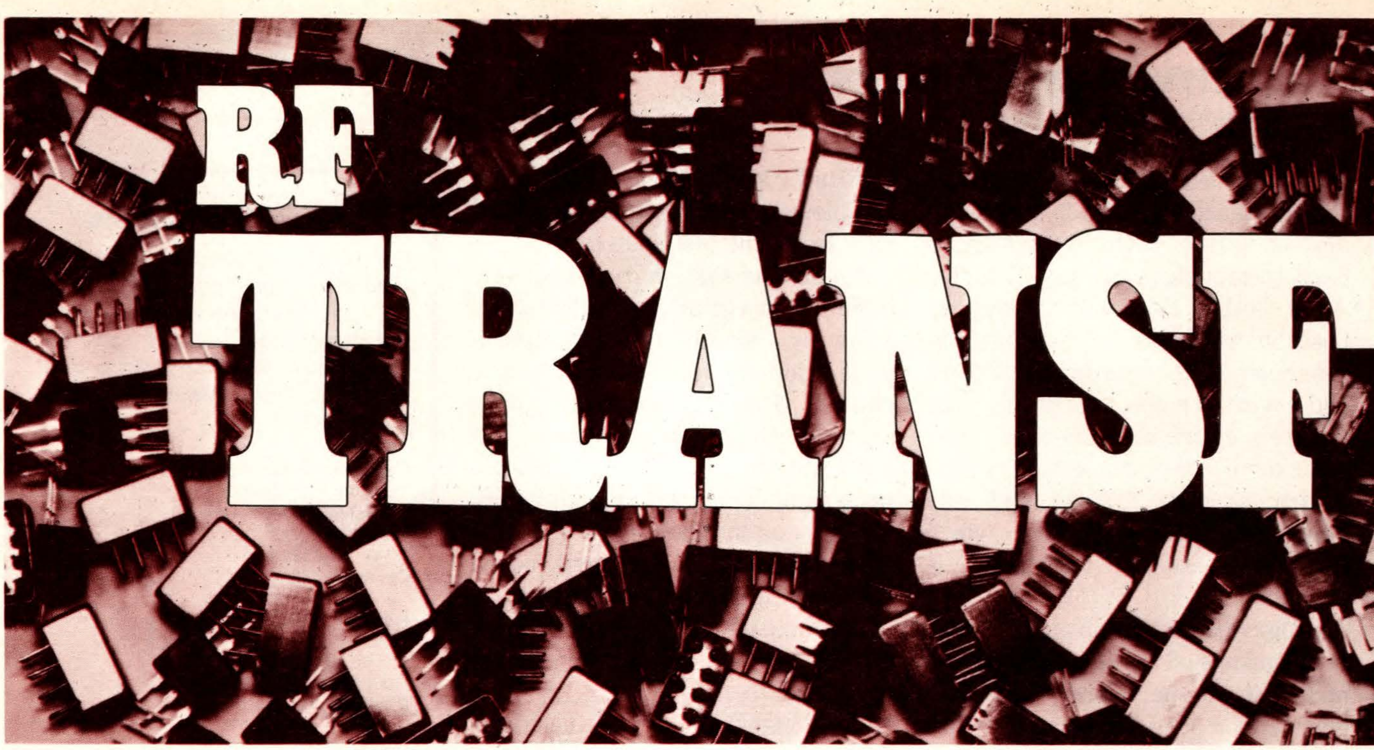
GenRad Inc
300 Baker Ave
Concord, MA 01742
(617) 369-4400
Circle No 445

Hewlett-Packard Co
1507 Page Mill Rd
Palo Alto, CA 94304
Phone local office
Circle No 446

Tektronix Inc
Box 1700
Beaverton, OR 97075
(503) 644-0161
Circle No 447

Teradyne Inc
183 Essex St
Boston, MA 02111
(617) 482-2700
Circle No 448

Zehntel Inc
2625 Shadelands Dr
Walnut Creek, CA 94598
(415) 932-6900
Circle No 449



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It costs less to buy Mini-Circuits wideband RF transformers. The T-series (plastic case) and TMO series (hermetically sealed metal case) RF transformers operate with impedance levels from 12.5 ohms to 800 ohms and have insertion loss, 0.5 dB typ. High reliability is associated with every transformer. Every production run is 100% tested, and every unit must pass our rigid inspection and high quality standards. Of course our one-year guarantee applies to these units.

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2 TRANSFORMERS OF EACH TYPE

T 1-1, T 2-1, T 4-1, T 9-1, T 16-1

Specify TK-1 **$32.00**

TMO 1-1, TMO 2-1, TMO 4-1
TMO 9-1, TMO 16-1

Specify TMK-2 **$49.50**

Schematics

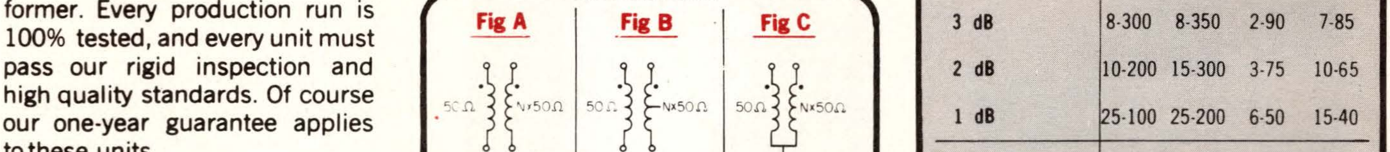
NEW MODELS

HIGH-LEVEL, PLASTIC CASE

Model	T1-1H Fig A	T4-1H Fig B	T9-1H Fig A	T16-1H Fig A
Freq. range, MHz	8-300	8-350	2-90	7-85
Impedance ratio	1	4	9	16
Max. insertion loss	MHz	MHz	MHz	MHz
3 dB	8-300	8-350	2-90	7-85
2 dB	10-200	15-300	3-75	10-65
1 dB	25-100	25-200	6-50	15-40
Price (10-49 qty.)	$4.95	$4.95	$5.45	$5.95

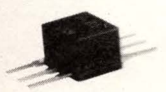
For complete specifications and performance curves, refer to 1979-80 Microwaves Product Data Directory pgs. 161 to 368 or 1979 EEM pgs. 2770 to 2974.

PERFORMANCE SATURATION CURVES T, TH SERIES (RF POWER & DC CURRENT AT WHICH SIGNAL SATURATION BEGINS)



R41-1 Rev A

10KHz-800MHz... From $2.95 (10-49)



T-H Series
T-Series
(Plastic case)

TMO-Series
(Metal case, hermetically sealed)

CENTER-TAPPED DC ISOLATED PRIMARY & SECONDARY Fig B

Model Metal case	TMO 1-1T	TMO 2-1T	TMO2.5-6T	TMO 3-1T	TMO 4-1	TMO 5-1T	TMO13-1T
Plastic case	T 1-1T	T 2-1T	T 2.5-6T	T 3-1T	T 4-1	T 5-1T	T 13-1T
Freq. range, MHz	.05-200	.07-200	.01-100	.05-200	.2-350	.3-300	.3-120
Impedance ratio	1	2	2.5	3	4	5	13
Max. inserton loss	MHz	MHz	MHz	MHz	MHz	MHz	MHz
3 dB	.05-200	.07-200	.01-100	.05-250	.2-350	.3-300	.3-120
2 dB	.08-150	.1-100	.02-50	.1-200	.35-300	.6-200	.7-80
1 dB	.2-80	.5-50	.05-20	.5-70	2-100	5-100	5-20
Maximum Amplitude Unbalance, MHz							
.1 dB	.5-80	1-50	.1-20	1-70	.5-100	10-100	5-20
.5 dB	.05-200	.07-200	.01-100	.05-250	.2-350	.3-300	.3-120
Maximum Phase Unbalance Degrees, MHz							
1°	.5-80	1-50	.1-20	1-70	5-100	10-100	5-20
5°	.05-200	.07-200	.01-100	.05-250	.2-350	.3-300	.3-120
Price (10-49) Model TMO	$6.45	$6.75	$6.75	$6.45	$4.95	$6.75	$6.75
Model T	$3.95	$4.25	$4.25	$3.95	$2.95	$4.25	$4.25

DC ISOLATED PRIMARY & SECONDARY Fig A

Model Metal case	TMO 1-1	TMO 1.5-1	TMO 2.5-6	TMO 4-6	TMO 9-1	TMO 16-1
Plastic case	T 1-1	T 1.5-1	T 2.5-6	T 4-6	T 9-1	T 16-1
Freq. range, MHz	.15-400	.1-300	.01-100	.02-200	.15-200	.3-120
Impedance ratio	1	1.5	2.5	4	9	16
Max. insertion loss	MHz	MHz	MHz	MHz	MHz	MHz
3 dB	.15-400	.1-300	.01-100	.02-200	.15-200	.3-120
2 dB	.35-200	.2-150	.02-50	.05-150	.3-150	.7-80
1 dB	2-50	.5-80	.05-20	.1-100	2-40	5-20
Price, Model TMO	$4.95	$6.75	$6.45	$6.45	$6.45	$6.45
(10-49) Model T	$2.95	$3.95	$3.95	$3.95	$3.45	$3.95

UNBALANCED PRIMARY & SECONDARY Fig C

Model Metal case	TMO 2-1	TMO 3-1	TMO 4-2	TMO 8-1	TMO 14-1
Plastic case	T 2-1	T 3-1	T 4-2	T 8-1	T 14-1
Freq. range, MHz	.025-600	.5-800	.5-600	.15-250	.2-150
Impedance ratio	2	3	4	8	14
Max. insertion loss	MHz	MHz	MHz	MHz	MHz
3 dB	.025-600	.5-800	.2-600	.15-250	.2-150
2 dB	.05-400	2-400	.5-500	.25-200	.5-100
1 dB	.05-200	—	2-250	2-100	2-50
Price, Model TMO	$5.95	$6.95	$5.95	$5.95	$6.75
(10-49) Model T	$3.45	$4.25	$3.45	$3.45	$4.25

Common specifications: Primary impedance, 50 ohms Total input power, ¼ watt
TMO Series .025 cu. inches, .07 ounces T Series .02 cu. inches, .01 ounces

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Mini-Circuits
MINI-CIRCUITS LABORATORY
A Division of Scientific Components Corp

R41-2-Rev A

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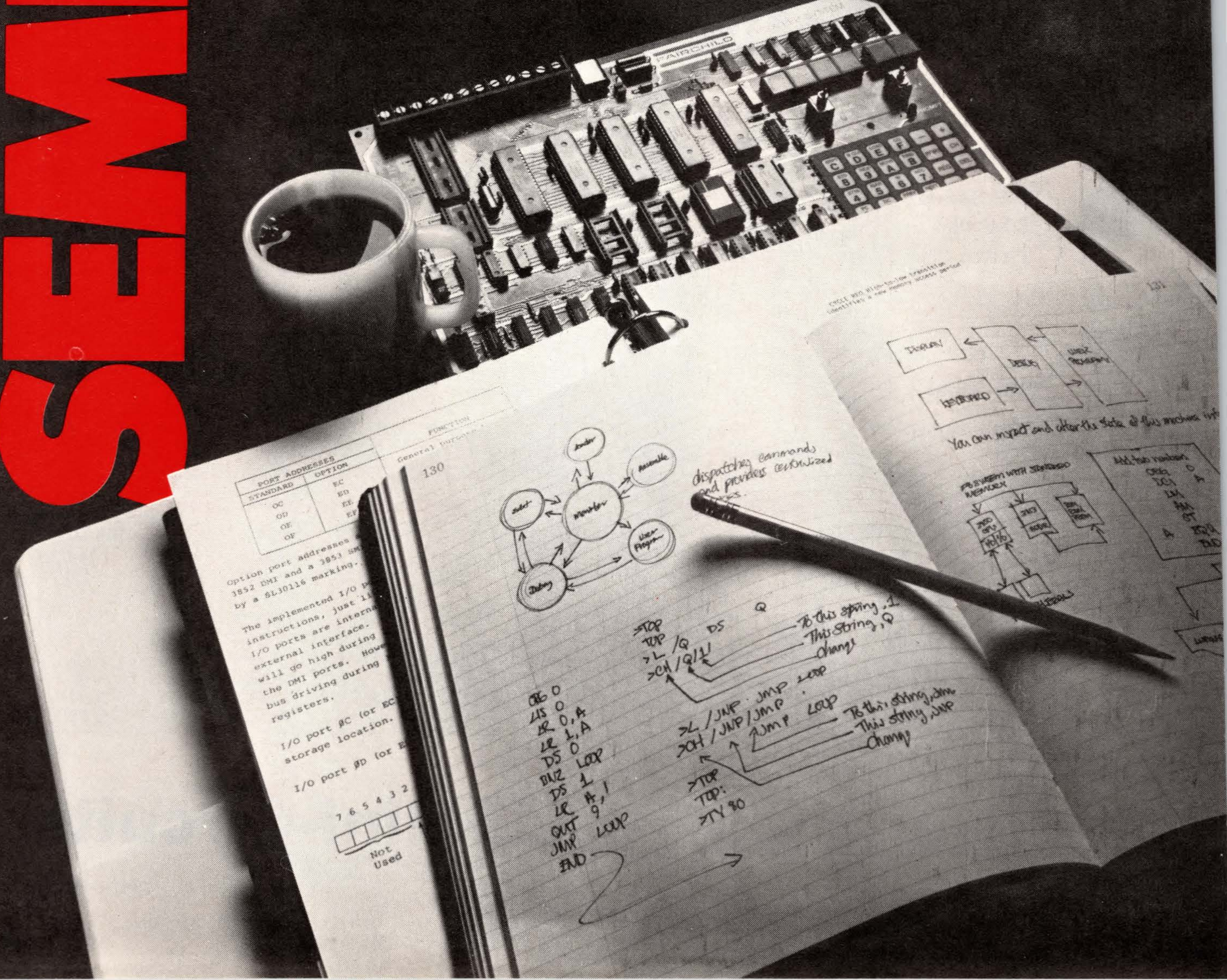
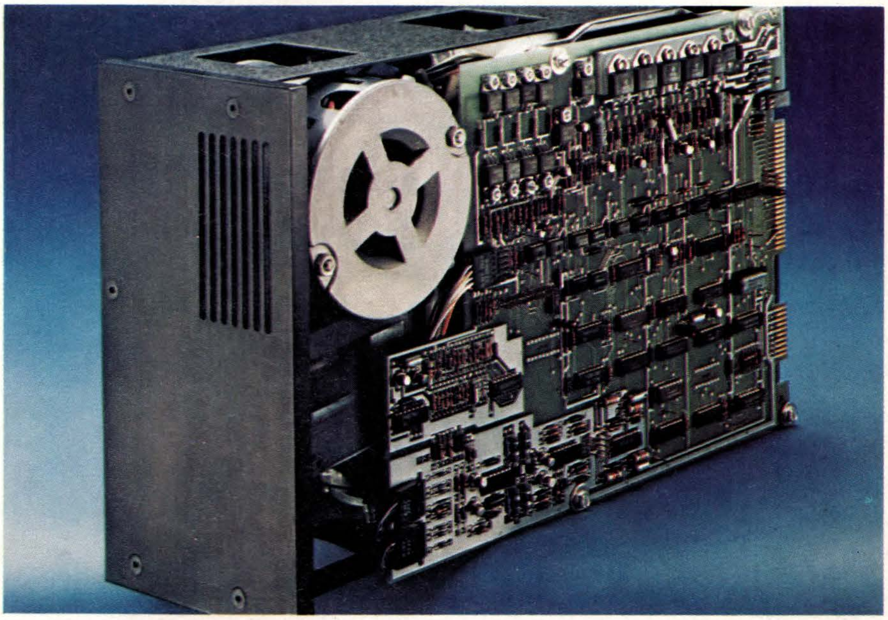


An 8-in.-hard-disc standard makes progress, but ANSI committee disagrees on details

Carl Warren, Western Editor



Efforts at standardizing an interface *for 8-in. rigid-disc drives (such as this Shugart Associates SA1004) progressed quickly at first but now face contention among the many manufacturers involved.*

Standardization has become the watchword of the computer industry—especially when it involves mass-storage technology such as the recently introduced 8-in. rigid-disc systems (EDN, February 5, pg 104). Standardizing this type of drive's interface is particularly important to avoid flooding the market with dozens of uncompatible units.

But standardization efforts reach far beyond this obvious factor. In its consideration of 8-in. drives, the American National Standards Institute (ANSI) X3T9.3 committee hopes to provide a standard interface definition that meets the following criteria:

- Low cost (achieved by specifying daisy-chain connections rather than radial cables, for example)
- Adequate speed to handle up to a 10-MHz data rate
- Ability of drives to communicate over their lowest common denominator — an 8-bit parallel command - and - status bus.

Based on these simple goals, the committee has accomplished a great deal, primarily because all the attendees have had common interests. As a result, its first four meetings produced a fairly clear definition of the proposed interface. Some problems in interface definition still exist, however.

Interface basics

ANSI's proposed 8-in.-hard-disc interface is relatively simple and for the most part meets the committee's pre-established goals. Basically, it consists of nothing more than a processor, a buffer, firmware and some line drivers. This design represents a vast improvement over the storage-module-device (SMD) interface, which requires a tremendous amount of electronics.

The ANSI interface for up to four drives sharing a controller defines an 8-bit bidirectional command/status bus, a bit-serial data bus, full handshaking, daisy chaining and specifications for one 50-pin ribbon connector. Notably, the definition applies only to higher capacity drives—20M bytes and above. Even so, it allows for upward expansion, the lack of which is a drawback with the SMD interface.

This expandability is apparent in the interface's proposed command-structure definition. As planned, command and control functions will occupy two bytes: the first to contain the command and the second to specify the relevant parameter. According to Pertec's committee member, Paul Toma, the standard allows a possible 128 commands in and 128 out and distinguishes between mandatory and optional commands, thus increasing the interface's flexibility.

Because of the interface's bidirectional command/status bus structure, the standard requires no select lines. The drives' unit-select function is embedded in the command, thus reducing the number of interface lines and consequently lowering cost.

Why isn't the standard ready?

With all this progress and apparent agreement among committee-meeting attendees, you might logically conclude that the 8-in.-rigid-disc standard is fully defined. Unfortunately, however, the proposed definitions represent the thoughts of only a few companies among the 39 listed on the committee roster.

The apparent reason for this discrepancy, explains Beau Vrolyk, International Memories Inc (IMI) committee member and acting secretary, is that "most of the companies on the committee didn't feel that things would move as fast as they did and didn't bother to come."

The real battle over the standard thus surfaced at the last meeting (held in December), which was attended by more than 33 representatives wanting to put in their two cents' worth.

One bone of contention at this meeting was some designers' desire to specify minimum-cost designs employing processors such as the 6801. Although this μP would serve well if drive parameters don't change in the future, it could narrow the expansion flexibility and adaptability of the interface electronics.

The choice of a processor has an important effect on the timing of events in a drive. When a controller sends a command, each drive in the chain must determine if it's been selected. Timing problems can occur when this command is received, however; the selected drive is frequently involved in a seek operation and might not have time to respond to the controller. Thus, designers must rely on clever software to provide timing. "However," notes Vrolyk, "no amount of clever software will take care of the lack of computing throughput."

Surprisingly enough, almost the entire committee agreed on the general concepts proposed at the December meeting. But decisions still remain on whether the drive should monitor the communication bus all the time, which type of processor would best suit low-cost requirements and how far away drives can be placed from their controller. Committee members will iron out these and a few other problems at a Deerfield, FL meeting on February 20.

A surprise standard

Although the committee has already invested a great deal of work in the standard, what could become the actual interface definition might not originate from ANSI at all. When the X3T9.3 committee

was formed and its goals mapped out, several of the companies involved (BASF, IMI, Micropolis, Pertec and Shugart, to name a few) had already fairly well defined what they wanted in an interface—a fact that prompted the committee to speed up its deliberations and develop the specification to its present state.

In the meantime, however, one firm (IMI) has begun shipping more than 200 drives a month, another (BASF) is beginning to ship drives, and almost every other manufacturer promises shipments in the third quarter. In addition, BASF and IMI offer similar interfaces that closely resemble the proposed ANSI definition. As a result, industry observers feel that if the ANSI standard is delayed for 6 months, the IMI/BASF interface will become the de facto standard.

3-level standard?

The industry could also play out a third scenario, according to David Krevanko of Fujitsu America: "From what I can see, it looks like there will be a threefold approach to the interface question—there will be a configuration based on a modified floppy interface (like the approach taken by Shugart), an SMD-type interface and the ANSI interface."

Whichever possibility ultimately comes about, most designers can only hope for the best. As one committee member moans, "I'm sitting here with three-fourths of a standard, with no idea what the other 25% will look like. It's impossible to create a design without that last bit of information."

ANSI committee chairman Gary Robinson requests that all inquiries regarding the interface - standard effort be directed to him at Datatrol Inc, Kane Industrial Dr, Hudson, MA 01749. You can phone him at (617) 568-1411. And watch EDN for the latest news in this key computer-peripherals area. **EDN**

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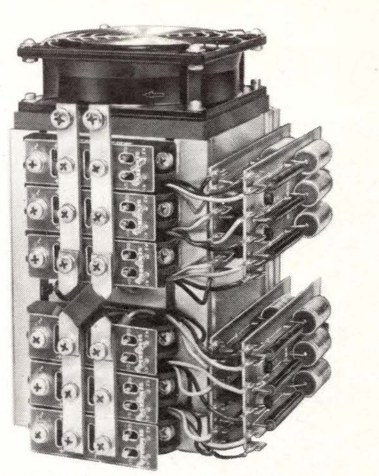

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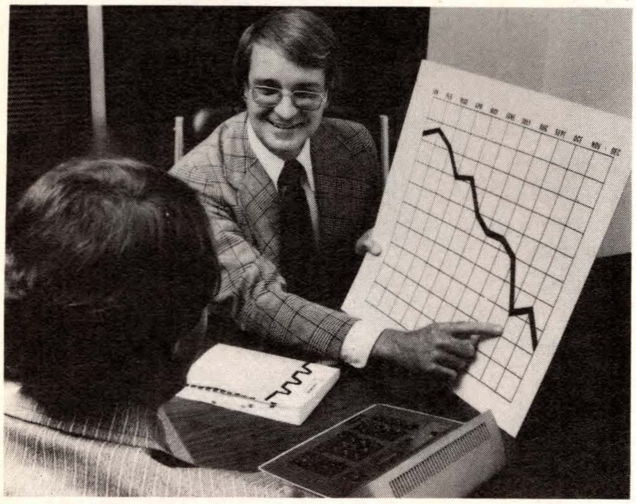

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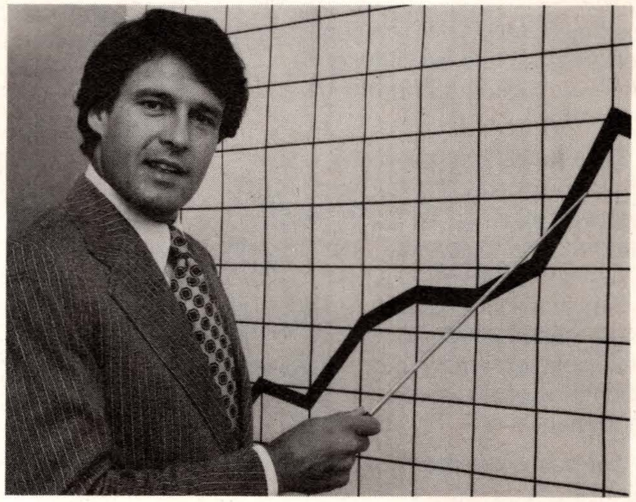

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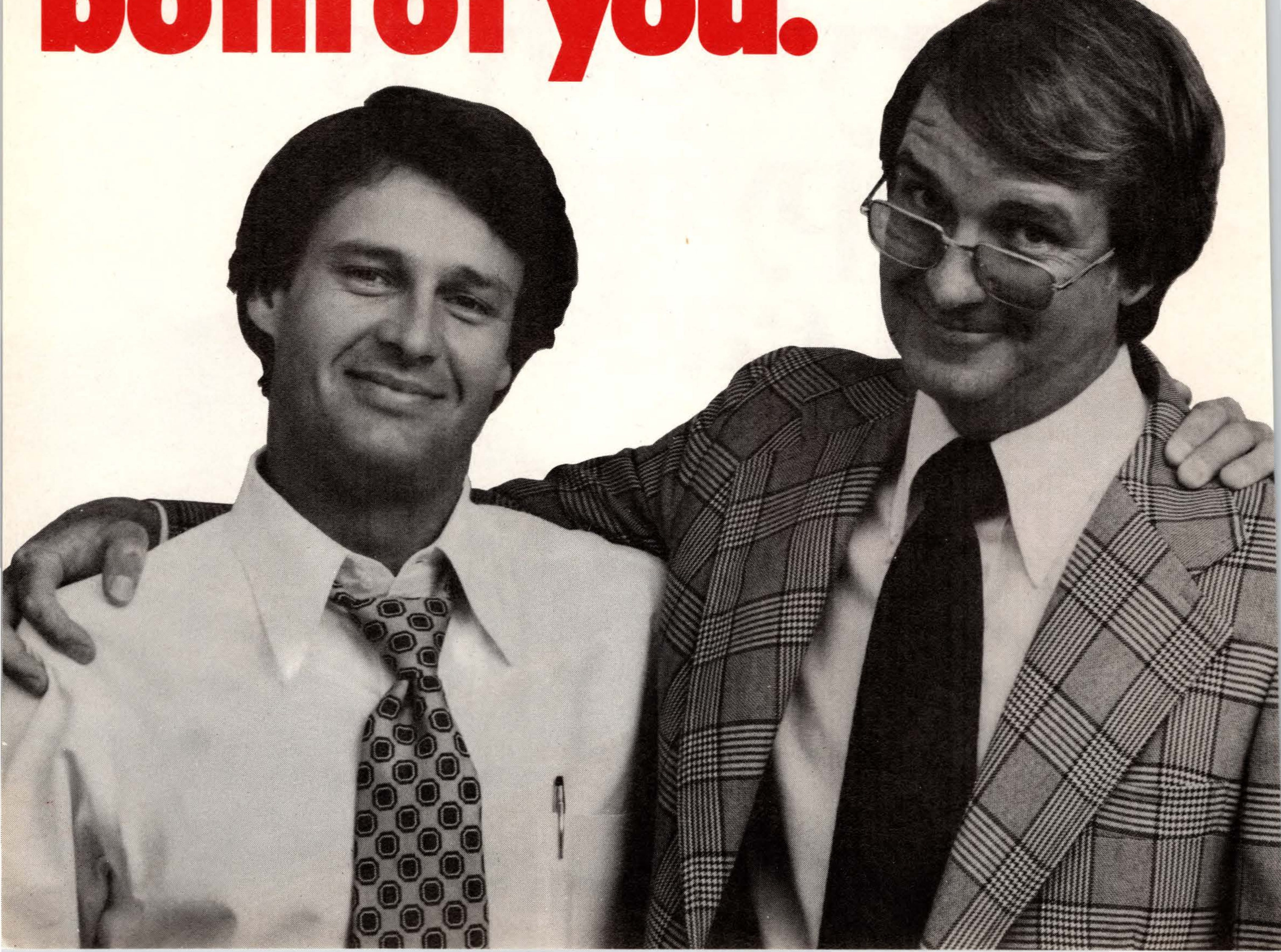

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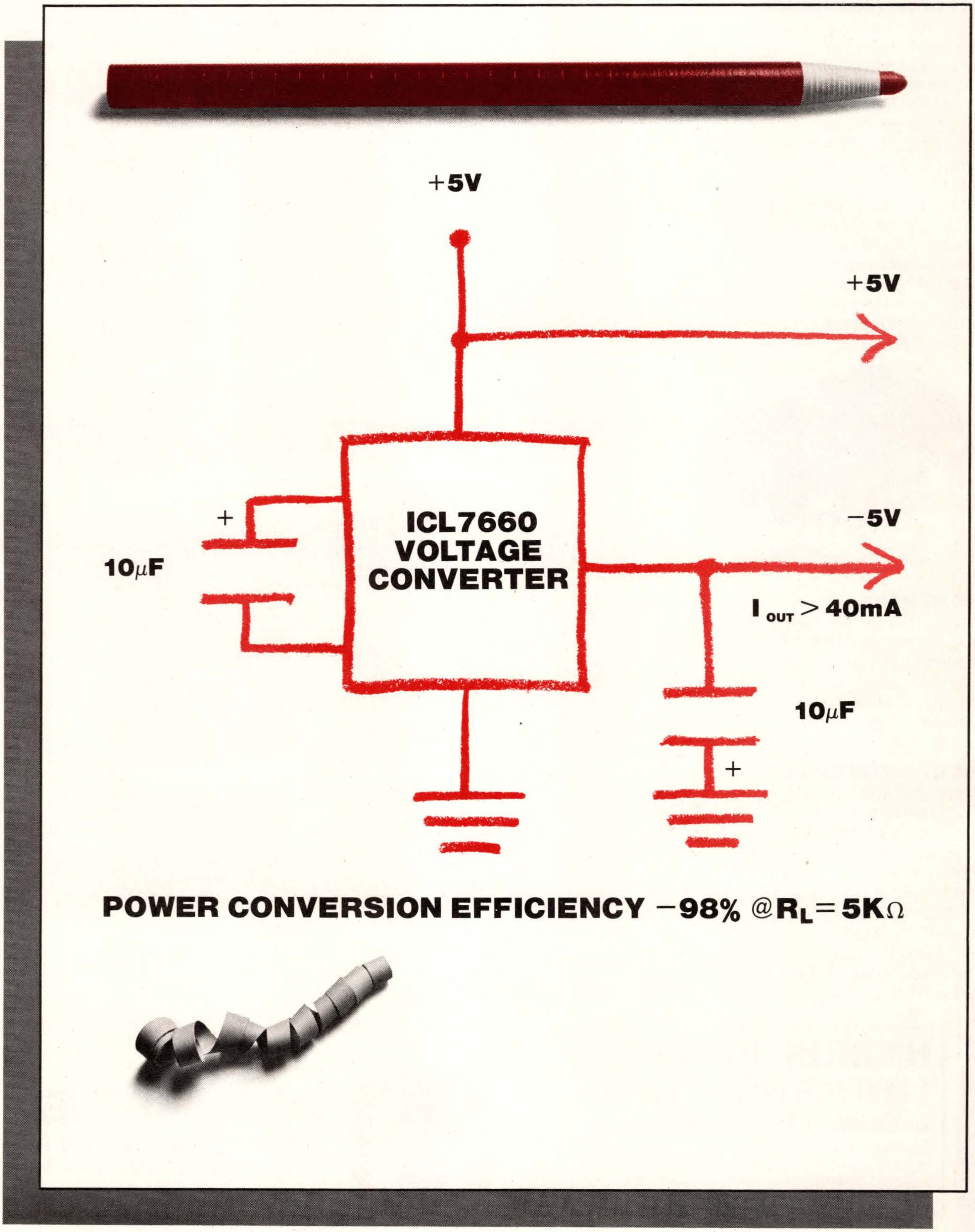

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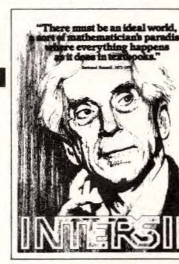

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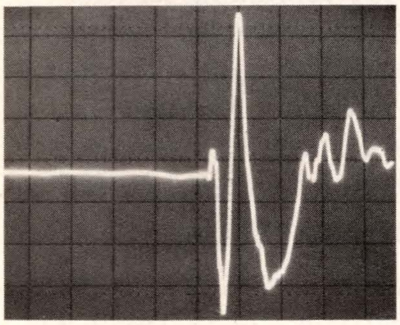

signals, converts them to digital data, then stores that data in semiconductor memory, provides display, plot or digital outputs of captured signals.

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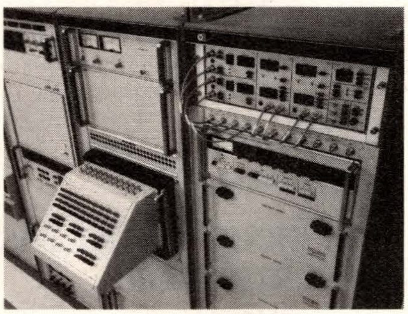

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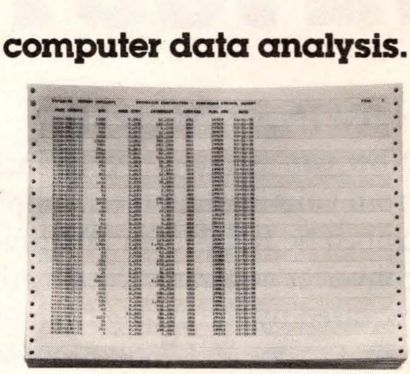

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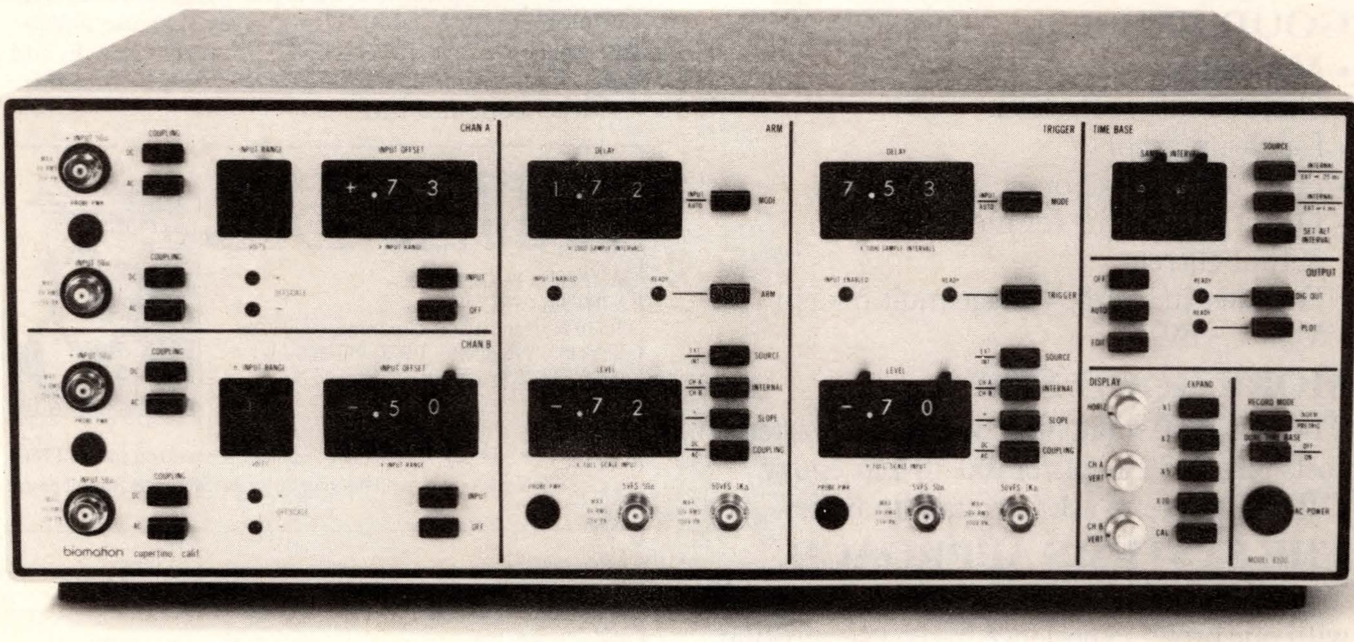


For more information, Circle No 28

Powercon 7 to feature MOSFET applications, fast switchers and effective modeling

Bob Peterson,
Assistant Managing Editor

Stressing an analytical yet practical approach to optimizing power systems, this year's Powercon will detail power-electronics technology's increased sophistication and technical maturity. The Seventh National Solid-State Power Conversion Conference will present design and application information on equipment and components, organized in more than 40 papers, 70 exhibits, seven short courses, several manufacturer's clinics and new material and device introductions of special importance to power-system engineers (see **table**).

Modeling developments

To emphasize the value of careful analytical design techniques as opposed to seat-of-the-pants approaches, Powercon will include a session **(G)** on modeling and analysis as well as one **(I)** on applying analytical methods. These modeling presentations will cover two aspects of the analysis process: Models can function as conceptual tools to aid the design effort in a general sense, and they also allow designers to experiment with many different circuit values without incurring the time and expense involved in actually building all the possible variations.

In a **session G** paper entitled "The Modeling and Design of Nondissipative LC Snubber Networks," for example, William Shaughnessy, manager of drives design at the Superior Electric Co, will describe an analytical tool that allows you to predict turn-off load lines and peak collector voltage, as well as the effects of circuit parameters on these characteristics.

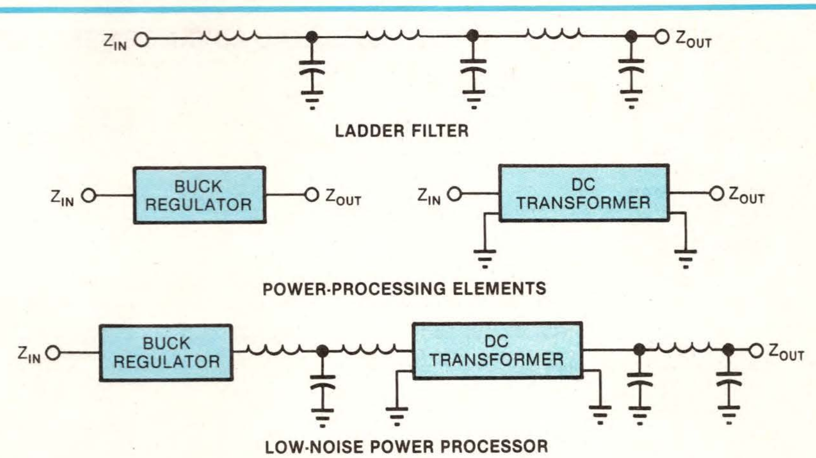
And "Computer Modeling of the PWM Converter," by Dr Vincent Bello of Norden Systems, will describe a FORTRAN subroutine that models the power and control portions of dc and ac small-signal and ac large-signal gain and phase information. To utilize this subroutine, you insert it into a standard circuit-analysis program (such as CSC TRAC or CDC SYSCAP II) that accepts FORTRAN subroutines; the model acts as the transfer-function specification in the standard program.

Bello's subroutine requires only one statement, indicating a converter's dc input, duty cycle, input node and output node. At the conference, he will also develop equations relating a converter's duty cycle to its error amplifier's control voltage, storage time and dead time.

Providing a conceptual tool as well as a hardware-applicable model will be David Blough and Walter Bradley, senior engineers in transmitter design and development and space and information systems, respectively, at Westinghouse Electric. In their **session G** paper, "Simplifying the Analysis of Power-Conditioning Circuits with a Straightforward Iterative Technique," they will outline a modeling approach that implements a piecewise-linear approximation—a method that deals with very short time increments during which a nonlinear circuit can be considered linear for analysis purposes.

By calculating a series of such approximations, you can predict how a circuit will operate. The technique thus perfectly suits computers' iterative capabilities; Blough and Bradley's model even runs on programmable calculators.

Powercon 7 also will include papers on many applications that could benefit from the use of modeling techniques — especially high-frequency switchers, which virtually mandate modeling to understand their operating characteristics. **Session A,** for example, will include "Applying Sine-Wave Power-Switching Techniques to the Design of High-Frequency Off-Line Converters," by D A Amin, a project manager at Hewlett-Packard. He will describe a 200-kHz switcher designed at HP that capitalizes on resonant circuits to keep its output's harmonic content low and thus minimize EMI



Reduce a switching converter's high-frequency-noise generation *by inserting the switcher's elements into a filter ladder designed to attenuate at the main switching frequency (the major source of noise). This approach will be covered in detail in a Powercon 7* ***session H*** *paper.*

generation.

Amin's unit also demonstrates that switchers can switch waveforms other than square waves. Supplies that generate sine waves offer advantages over square-wave units because sine waves are usually created by the interaction of inductors and capacitors rather than the brute-force method of turning a switch on and off; thus, a reactive sine-wave circuit never attempts to conduct full current while turning off full voltage (current follows a resonant pattern, as does voltage).

Sine - wave switchers' circuit components can operate at much higher frequencies than the devices required in square-wave units, and they fit in smaller packages. But you do pay a price: Sine-wave switchers produce a higher peak current.

Topology advances

Another area of interest to power-supply designers is a session

POWERCON® 7 CONFERENCE PROGRAM

Sessions will be held on March 24 through 27 in San Diego, CA at the Town and Country Hotel. Obtain additional information by contacting Powercon 7, Box 5226, Ventura, CA 93003. Phone (805) 985-6978 or (805) 486-5463.

	TUES MARCH 25	WED MARCH 26	THURS MARCH 27
8:30	**SESSION A: HIGH-FREQUENCY POWER CONVERSION** Applying sine-wave power-switching techniques to the design of high-frequency off-line converters Optimization of board-mounted high-frequency dc/dc switching regulators Designing a 400-kHz switching converter for bidirectional output power	**SESSION D: SEMICONDUCTORS FOR POWER CONVERSION** The power MOSFET as a switch, from a circuit designer's perspective A new bipolar high-frequency power-switching technology eliminates load-line shaping The effects of radiation on the characteristics of power MOSFETs Characterization and implementation of power MOSFETs in switching converters	**SESSION G: MODELING AND ANALYSIS OF POWER CONVERTERS** Switching-interval modeling in very high-frequency, high-power MOSFET converters Simplifying the analysis of power-conditioning circuits with a straightforward iterative technique Computer-modeling the PWM inverter Modeling and design of nondissipative LC snubber networks
10:30	**BREAK**	**BREAK**	**BREAK**
11:00	**SESSION B: MAGNETICS FOR POWER CONVERSION** Optimization of energy-storage inductors for high-frequency dc/dc converters A new high-flux, low-loss magnetic material for high-frequency applications Detecting impending core saturation in switched-mode power converters Designing a new low-distortion ferroresonant regulating transformer	**SESSION E: NEW CONVERTER CONFIGURATIONS** Simplifying switched-mode-converter design with a new variable-leakage transformer topology A new coupled-inductor 2-phase switching regulator improves device utilization A new sine-wave-output power-converter topology eliminates reactive elements A new magnetic switching technique technique simplifies off-line-converter design	**SESSION H: NEW CIRCUIT-DESIGN TECHNIQUES II** Optimizing dynamic behavior with input/output feedforward and current-mode control Improving converter performance and reliability with a new base-drive commutation method Designing high-power converters for very low output noise Improving the efficiency of low-output-voltage switched-mode converters with synchronous rectification
1:30	**LUNCH BREAK**	**POWERCON 7 LUNCHEON**	**LUNCH BREAK**
3:30 TO 6:00	**SESSION C: HIGH-POWER TECHNIQUES** Optimizing the design of very high-power, high-performance converters A new base-drive scheme for transistorized electric-vehicle propulsion Designing high-power pulsers using VMOS transistors Circuit techniques for maximizing the efficiency of solar-array power processors	**SESSION F: NEW CIRCUIT-DESIGN TECHNIQUES I** Designing optimal base drive for high-voltage switching transistors Circuit techniques for eliminating primary current unbalance in push/pull power converters Designing a low-cost intelligent inrush limiter for off-line converters Factors affecting the long-term reliability of off-line converters	**SESSION I: REDUCING ANALYTICAL METHODS TO PRACTICE** Modeling, analysis and design of a multi-output Cuk converter Practical techniques for analyzing, measuring and stabilizing feedback control loops in switching regulators and converters Automating the measurement of converter dynamic properties Techniques for computer-aiding the design of feedback and control circuits
6:30 TO 8:00		**INDUSTRY-SPONSORED COCKTAIL PARTY**	

PROFESSIONAL ADVANCEMENT PROGRAM

MON MARCH 24

9:00 AM TO 1:00 PM
The "business end" of the business: Market awareness
Bob Boschert, Boschert Inc; John O'Boyle, Gnostic Concepts; John Salzer, Salzer Technology; Alberto Socolovsky, Electronic Business *Magazine*

2:00 PM TO 5:30 PM
Designing very high-frequency switched-mode converters
Rudolf Severns, Intersil

2:00 PM TO 5:30 PM
Designing compact high-voltage converters for reliable performance
Dennis Hunt and Richard Kanthack, Eldec

TUES MARCH 25

2:30 PM TO 6:00 PM
Techniques for optimizing the design and application of high-frequency power magnetics
Steve Smith, Quatt-Wunkery; Charles Mullett, Mullett Associates Inc

TUES MARCH 25

3:00 PM
New devices and applications program
- Characterization and load-line optimization of ultrahigh-power switching transistors
- Using the power-MOSFET internal reverse rectifier
- A new ultrahigh-speed, high-voltage switching transistor
- Selecting soft ferrite materials for power-conversion frequencies to 1 MHz
- Simplifying converter power-stage design with complementary transistor switches
- Using microprocessors to internally monitor power-subsystem performance

6:30 PM TO 7:30 PM
Measurement clinic: Using spectrum analyzers for assessing and tracing switching-power-supply noise
Dave Leatherwood, Tektronix Power-Supply Design Group

WED MARCH 26

8:00 AM TO 11:30 AM
Techniques for developing new converter topologies
Rudolf Severns, Intersil

THURS MARCH 27

8:00 AM TO 11:30 AM
Power-MOSFET technologies
Chairman: Dave Hoffman, Siliconix

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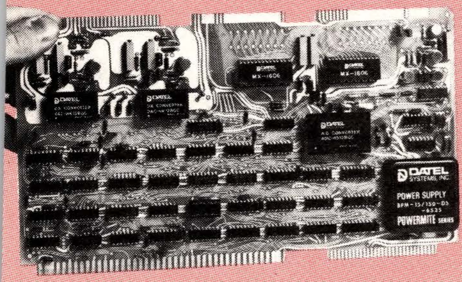
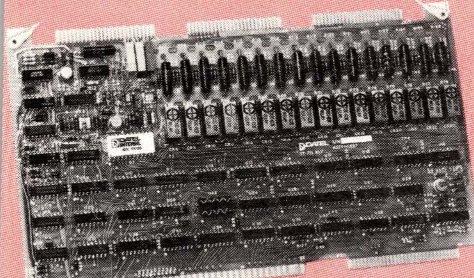


ST-711
ST-732



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(E) on new converter configurations. A paper by Dr Hiromitso Hirayama of TDK, for example, will describe a variable-leakage transformer topology that reduces a switched-mode supply's cost; the design regulates the supply's output voltage by means of a low-level dc current in its output transformer's control winding.

Also in **session E,** Wally Rippel, a member of the technical staff at the Cal Tech Jet Propulsion Lab, will introduce a 2 - phase switching regulator that employs negative coupling between its inductances to improve switching-device utilization and reduce inductor losses—yet retains the low input and output ripple characteristic of 2-phase systems.

Session H will provide some additional examples of new circuit configurations: In "Optimizing Dynamic Behavior with Input/Output Feedforward and Current-Mode Control," project engineer Richard Redl and president Nason Sokal of Design Automation will discuss current-load converters—supplies that switch current sources rather than voltage (an approach employed widely in Europe).

This session will also include "Designing High-Power Converters for Very Low Output Noise," by Steve Smith, director of research at Quatt - Wunkery. Smith suggests that if you must design a very low-noise power converter for an application such as a radar installation, you begin by eliminating the supply's major noise component before you design the actual power sections.

In a 30-kHz switcher, for example, the primary noise component occurs at 30 kHz, so you would first design a filter ladder that attenuates signals at that frequency **(figure).** Then you would insert the power converter's sections in series with certain filter-ladder elements, integrating the filter and converter into one unit capable of limiting noise to 100 dB down.

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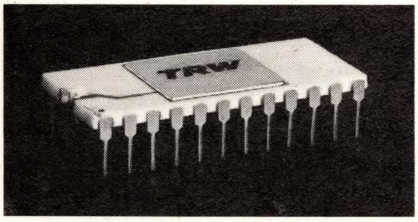

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News

Bipolar marries MOSFET

One of the factors that make new converter configurations possible is semiconductor innovation. A **session D** paper by staff engineer William Skanadore of General Semiconductor Industries Inc, entitled "A New Bipolar High-Frequency Power-Switching Technology Eliminates Load-Line Shaping," will introduce a device that should initiate improved converter designs. This component combines the high-power capabilities of bipolar technology with MOSFETs' high-frequency characteristics and further features an insensitivity to inductive load lines.

Several Powercon papers will also report on the value of more conventional MOSFETs for power-conversion purposes. Among these offerings are "Characterization and Implementation of Power MOSFETs in Switching Converters" (describing how the devices operate in actual circuits), by Cal Tech's Erickson, Behen, Middlebrook and Cúk; and "The Power MOSFET as a Switch, from a Circuit Designer's Perspective" (describing the devices' good and bad points), by Hewlett-Packard's Gyma, Hyde and Schwartz.

In addition to advanced-semiconductor coverage, Powercon will also include the introduction of "A New High-Flux, Low-Loss Magnetic Material for High-Frequency Applications" (**session B**), by research engineer David Nathasingh and project engineer Carl Smith of the Allied Chemical Corp. This amorphous metal/glass alloy provides such characteristics as a 16,100G saturation magnetization and losses at 125°C equal to half those of permalloy. Although the material isn't currently in production, its low-loss attributes could allow designers to develop much smaller high-frequency converters than are now possible. **EDN**

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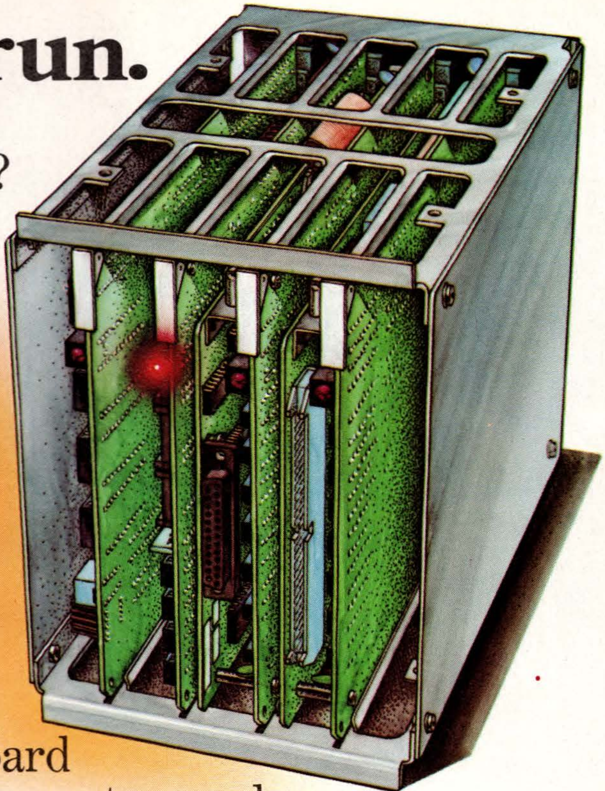

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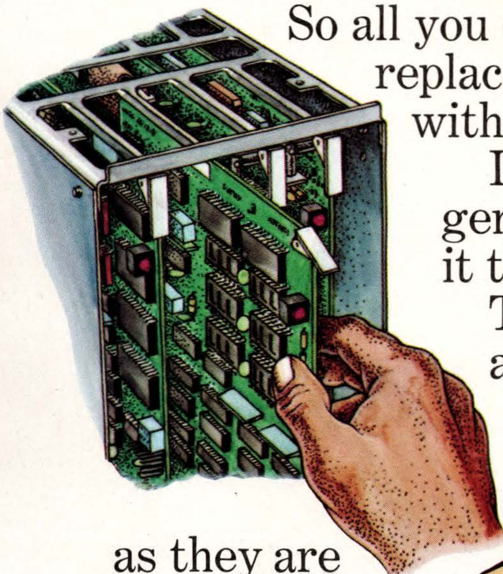

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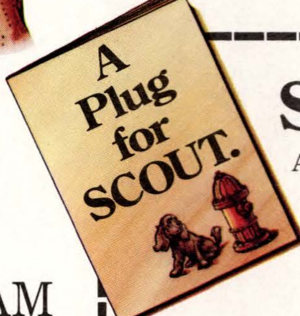

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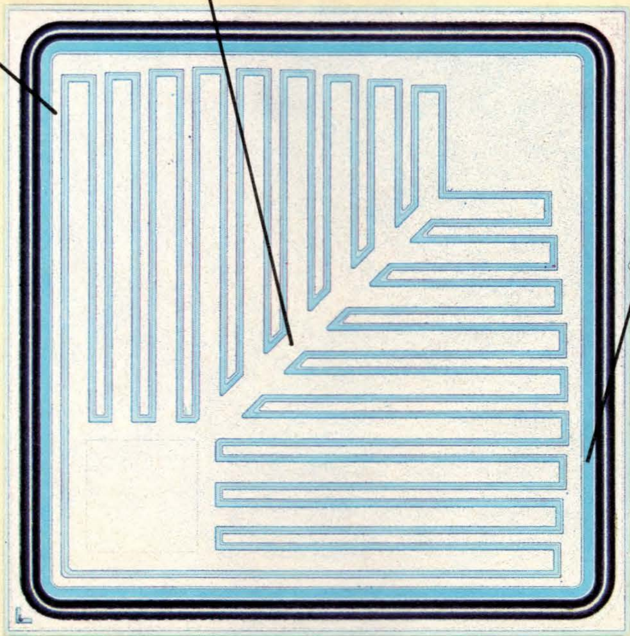

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For more information, Circle No 33

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For more information, Circle No 34

Computerized copilot with advanced skills could stem from control-system research

Recently initiated research might someday lead to machines that can understand, interpret and correct problems. The project aims at devising a computer that contains not only the data needed to fly an airliner, but also the knowledge needed to monitor inputs and interpret actual and potential problems, thus providing invaluable assistance to the flight crew.

Because the new computer would combine its data and programming into a single unit, it would be able to apply its knowledge of the data base, analyze a problem, compute the solution, warn the pilot through synthesized voice communication and provide instructions to correct the problem—all within a few seconds. To obtain further information, the pilot would merely voice a request to the computer as though it were a member of the crew.

4-level knowledge base

A team at the University of Illinois, Urbana - Champaign, is developing the experimental computer system. Headed by Prof R T Chien, director of the school's Coordinated Science Laboratory, the group is attempting to produce a comprehensive knowledge base for a particular type of airplane model so that the computer can determine the correct procedure to follow in unexpected situations.

The researchers have organized this knowledge base into four increasingly complex levels:

- **Flight plan**—The computer must monitor this data from take-off to landing.
- **Aircraft aerodynamics**—The computer must not stress the airframe beyond design limits.
- **Aircraft controls**—The computer must adjust control settings in response to changing environmental conditions.
- **Aircraft mechanical and electrical subsystems** — In addition to detecting malfunctions as they occur, the computer must monitor system trends to predict failures.

The research group expects to produce an operating laboratory model of the computer within 3 yrs. It will then turn over the design to a private company for adaptation to commercial use. EDN

Editor's Choice: New Products

500W open-frame switching supply offers many features at low cost

Providing 500W of power *to large memory systems, the open-frame 5J5 switching supply fits in the same space as similar boxed units. The four LEDs on the front display the switcher's operating status.*

Specifically designed to provide power for large logic systems, the 5J5 switcher furnishes many standard features that competitive units offer only as options. These features (including a logic - inhibit input, remote voltage - adjustment capability and a power-fail sense output), coupled with high-efficiency operation, suit the unit to supplying solid - state - memory power requirements.

One factor that helps the 5J5 achieve its high efficiency rating (80%) is its cooling - system design. This open-frame unit doesn't incorporate a fan—a low-efficiency device when operating in the voltage ranges required by memory systems. Instead, it utilizes a proprietary heat-sinking arrangement that involves no massive hardware.

The 500W supply accepts either of two input-voltage spreads—90 to 132V and 180 to 264V—and can operate in a 47- to 63-Hz range. Available output values include 5V at 100A, 12V at 41A, 15V at 34A and 24V at 22A.

Status reassurance

Perhaps the most notable special feature is a set of four LEDs mounted on the supply to display system status. These indicators tell the user if ac power is on, if dc output is on and if the unit is locked out because of an overtemperature or overvoltage condition. The LEDs primarily serve to reassure users that a nonoperating unit is in a protective mode rather than "blown."

Among the other standard features of the single - IC-controlled supply are several remote-sense and -adjustment provisions. A logic-inhibit input, for example, allows a TTL signal to turn the unit on and off—thus permitting you to sequence several supplies. You can also remotely adjust the supply's voltage via a pot connected across the appropriate terminals.

Dependable operation

To augment its remote-sense capability and overvoltage protection, the 5J5 incorporates several features to assure reliability. Foldback current limiting, for example, protects the unit against an overload or short-circuit condition by sensing both the output voltage and a reference voltage. And a thermal - protection function shuts down the supply if its temperature rises too high. (The 5J5 operates at full load between 0 and 40°C.)

In addition to protecting itself, the supply also helps prevent memory loss when the power-line voltage fails or falls below preset limits.

The 5J5 incorporates filters on both its input and output to prevent noise from arising on the power line and to avoid RFI problems. And each supply in the line is burned in and cycled before shipping; the unit carries an estimated MTBF of 100,000 hrs of continuous operation.

Because the switcher fits the industry - standard footprint (10×7.75×4.94 in.), it can directly replace existing units without modification. $395.

Sierracin Power Systems, 20536 Plummer St, Chatsworth, CA 91311. Phone (213) 998-9873. **Circle No 453**

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Editor's Choice: New Products

$205 hybrid A/D converter sports 600-nsec conversion time

Hybrid circuit technology is a means to an end, not an end in itself. In the ADC-815, that end is not small size, but *speed.*

The converter's conductor patterns, for example, are precisely laid out to achieve ultrahigh-speed operation. Also, the hybrid components are located as close together as possible to minimize delays. The result? A guaranteed 600-nsec conversion time.

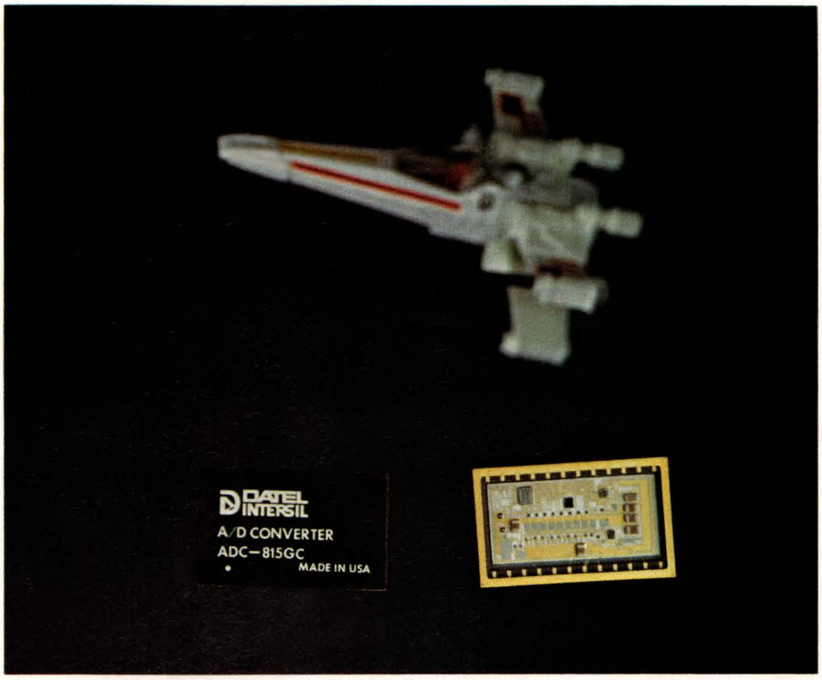
Interestingly, both the resistors and the conductor patterns in the data converter are fabricated by means of thin-film processes. The nichrome resistor networks are deposited directly on the 3-μin. ultrasmooth ceramic substrate, then actively laser trimmed to achieve ½-LSB max integral and differential nonlinearity.

Stability with respect to temperature is good: Gain TC measures 20 ppm/°C max over 0 to 70°C, zero drift is 100 μV/°C max, and offset TC is 10 ppm/°C max. The spec for long-term stability equals ±0.05%/yr typ.

Programmed input

In addition to its exceptionally fast conversion rate (up to 1.67 MHz), the ADC-815 features six pin-programmable input-voltage ranges—+5, +10, +20, ±2.5, ±5 and ±10V — for maximum application flexibility. A logic input switches the converter from unipolar to bipolar operation.

Output coding can be straight binary, offset binary or two's complement. The converter also provides outputs for serial data, clock and status.



Faster than a speeding starfighter? *Not really, but the competitively priced ADC-815 claims a 50% or better speed increase over its competition. A complete successive-approximation-type converter, the hybrid device incorporates programmable input ranges and output coding and specs 0.02%/% max power-supply rejection.*

Serves varied uses

Aimed at such demanding applications as pattern recognition, telecommunications, fast-servo and radar systems, computer typesetting and high-speed instrumentation and test equipment, the ADC-815 comes in a 24-pin hermetically sealed ceramic DIP with 0.6-in. pin rows. It requires ±15 and 5V supplies.

Extended-temperature-range versions and a slower 1-μsec model (ADC-825) are also offered. Delivery, 8 to 12 wks ARO.

Datel-Intersil, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. **Circle No 454**

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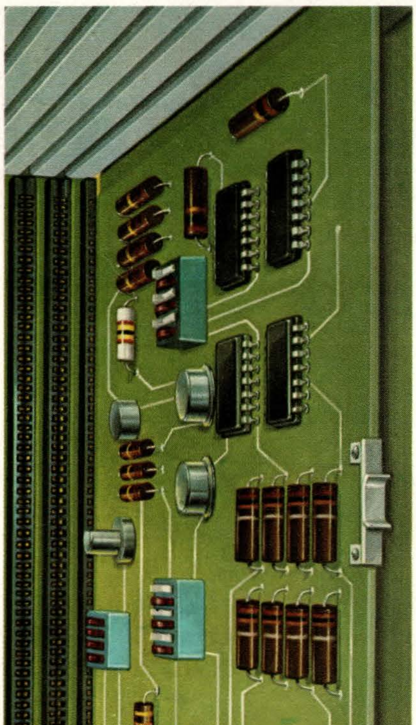
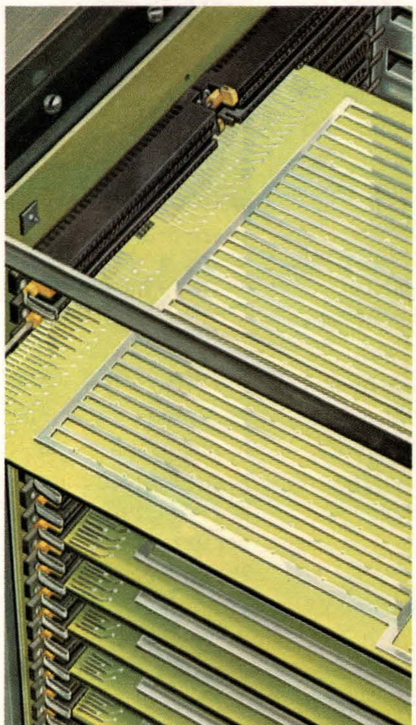
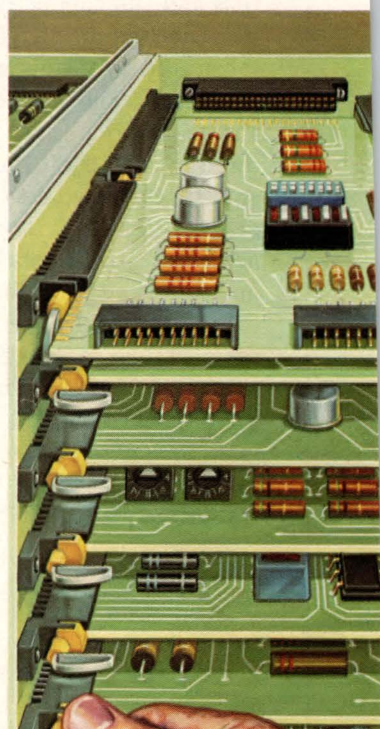


1. Large boards mate easily without damage



2. ZIF Connectors replace card guides



3. All board edges can be used for I/O's

AMP ZIF connectors—for Zero Insertion Force—give you more ways than ever to take advantage of microprocessor technology. While providing you with extra benefits of their own.

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ZIF connectors will also eliminate problems. Such as back panels, worn contacts, and board damage during test or insertion. And when you use ZIF connectors as card guides, all four sides of the board are available for interconnect, so you can shorten circuit traces, reduce voltage drops, and separate power and signal circuits, economically.

To help you accomplish all this, AMP provides three principal types of ZIF connectors: Rotary Cam Actuated Edge connectors, Linear Cam Actuated Edge connectors, and our exclusive Stacking connectors.

All of them are designed to enhance your interconnections while providing easy board insertion. Just open the contacts with the cam, slide in your board from the edge or the top, and close the contacts the same way. No auxiliary devices or mallets. And later access to the board is easier, too.

Of course, AMP ZIF connectors also come with full engineering support for technical assistance, whenever, or wherever you need it.

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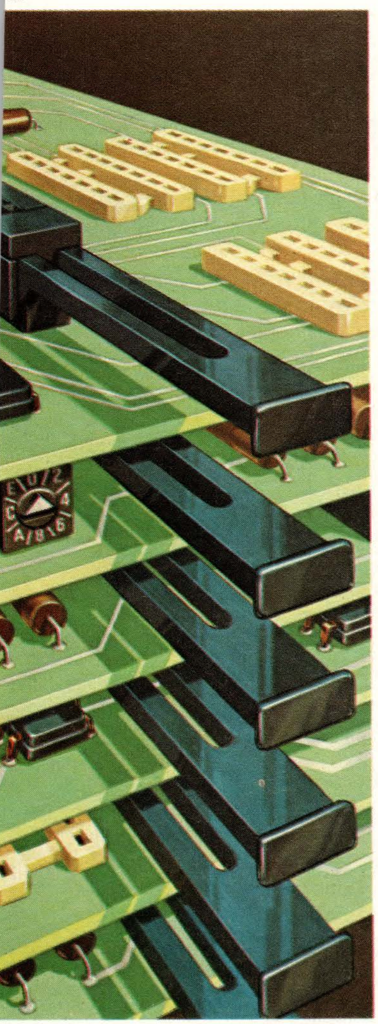
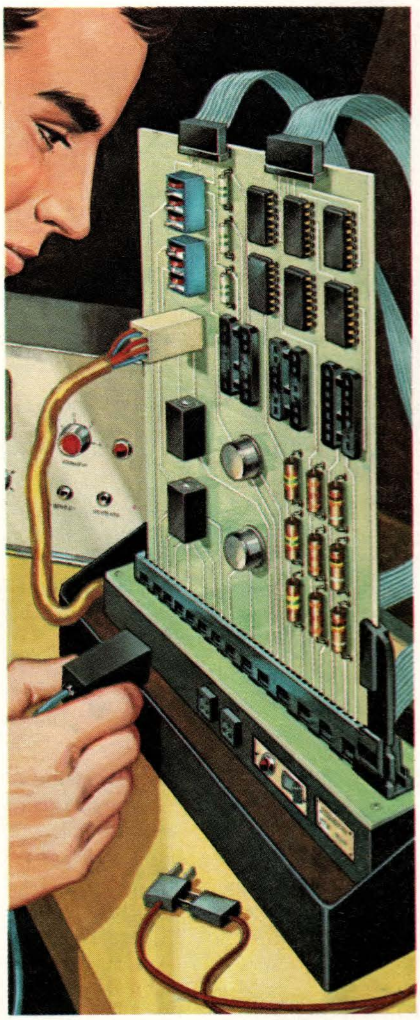


4. Stacking ZIF's eliminate backplanes



5. Ideal for test equipment

Some facts worth knowing about AMP ZIF connectors:

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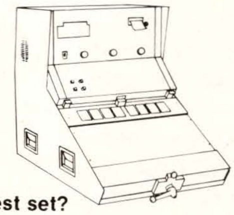
Where to write: AMP Incorporated, Harrisburg, PA 17105.

AMP

For more information, Circle No 36

Ask yourself some fitting questions about test fixturing.



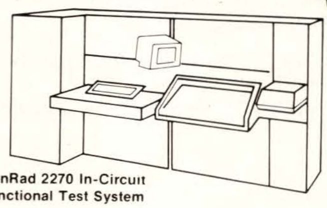
ATEC
Series 55-150

1.

Is there a fixturing system that fits perfectly with my present test set?
Yes. The ATEC Series 33. No matter what test set you presently use, ATEC Series 33 has test fixturing that fits. That means it mates with the GenRad 2270, the Teradyne L527, the Hewlett-Packard 3060A and, of course, the ATEC Series 55 test sets. The ATEC Series 33 fits perfectly with these and many more.

2.

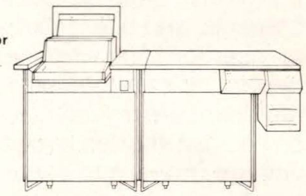
But will it fit different product sizes?
Yes! The Series 33 Interface Adaptor accepts a variety of product sizes by simply changing the test head. There's no need to purchase a different adaptor for different product sizes.
The Series 33 Interchangeable Test Heads are configured to the specific test point pattern of your product. They can accommodate products up to 20 x 24 inches with up to 2048 test points.



GenRad 2270 In-Circuit Functional Test System

3.

What if my product doesn't fit the standard fixturing?
Give us a sample product or suitable artwork, and we'll build fixturing to fit it. No problem, no trouble, no big expense. We've been making custom test fixturing a long time, and we're good at it.



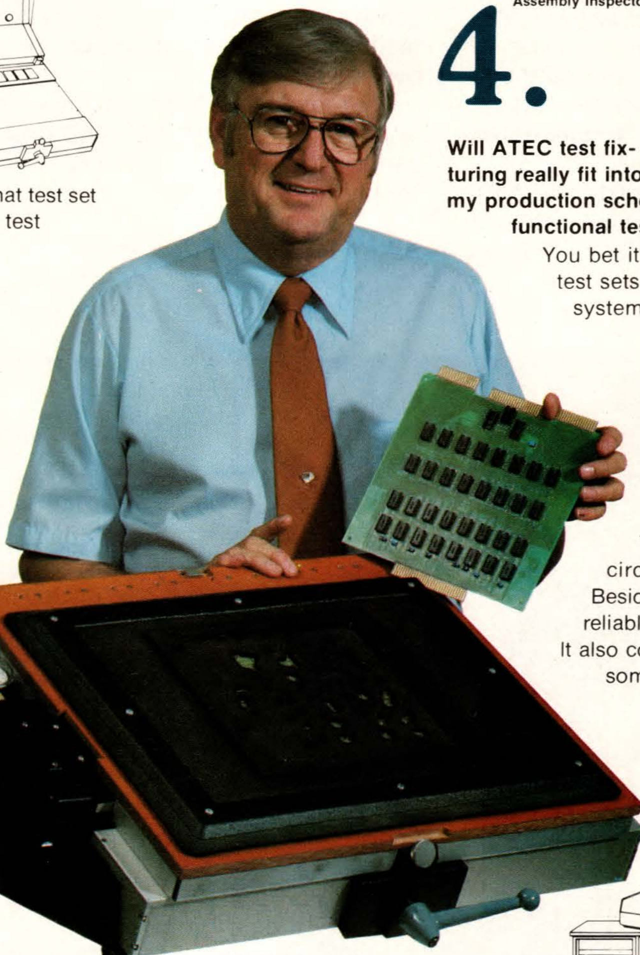
Teradyne L527
Assembly Inspector

4.

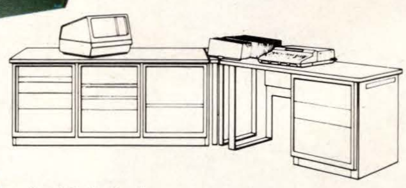
Will ATEC test fixturing really fit into my production scheme and solve my in-circuit and functional test problems?
You bet it will. We've fixtured hundreds of test sets for a variety of products. The system works, and it works well.

5.

Will the ATEC Series 33 fit my budget?
Yes! It's cost efficient for both in-circuit and functional test systems. Besides, every moment you don't have reliable test fixturing costs you money. It also costs you time and frustration, something nobody can afford.



HAROLD REDSHAW
Sales Coordinator
ATEC, Pomona



Hewlett-Packard
HP3060A Board Test System

6.

Does the ATEC Series 33 fit all my fixturing needs?
Definitely. The Series 33 has been expertly engineered for reliability, skillfully assembled for durability, economically priced for affordability. For test fixturing that fits any test system you're thinking about, there's no question about it. ATEC Series 33.

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AN EVERETT/CHARLES COMPANY

E/C™ EVERETT/CHARLES, INC

For more information, Circle No 37

Editor's Choice: New Products

Low-noise, low-distortion audio IC packs its capabilities in an 8-pin DIP

Lacking only a very high-power output stage, the MA-332-CP audio operational amplifier provides a nearly complete high-fidelity audio amplifier in one 8 - pin mini - DIP. This monolithic IC incorporates a low-noise bipolar differential input stage and a true complementary Class AB output stage.

Operating at ±24V, the device can drive a 600Ω load to ±20V with a *maximum* total harmonic distortion of 0.002%. And its input characteristics are equally impressive: With 1-kHz spot-noise specs of 3.5 nV/$\sqrt{\text{Hz}}$ and 400 pA/$\sqrt{\text{Hz}}$, the chip compares exactly with Signetics' low-noise NE5545 op amp.

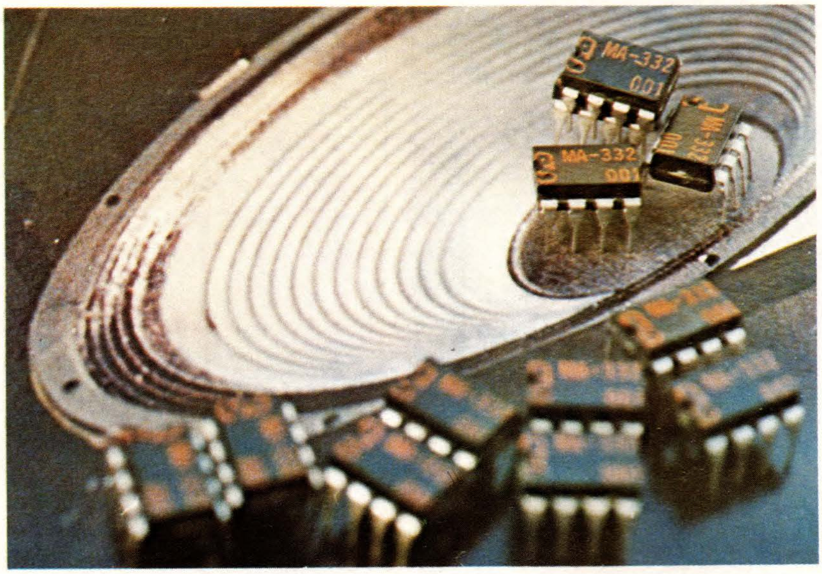
DC coupling permitted

In true op-amp style, the 332 boasts typical power-supply and common-mode rejection ratios of 100 dB. In addition, a 5-mV max input offset voltage (trimmable to zero by conventional methods), combined with a 1-μA max input bias-current requirement, suits the unit to dc applications.

The usual tradeoffs required among differential input-impedance (100 kΩ), input-bias-current and noise-performance specs are well balanced in the 332. Input noise-voltage spectral density typically amounts to only 3.5 nV/$\sqrt{\text{Hz}}$ from 100 Hz to 100 kHz; below the 100-Hz knee, a 1/f noise component appears, and this spec rises at a 3-dB/octave (10-dB/decade) rate to 7 nV/$\sqrt{\text{Hz}}$ typ at 30 Hz.

The knee of the input noise current occurs at 300 Hz: From this point up to 100 kHz, the parameter reaches a maximum of 400 pA/ $\sqrt{\text{Hz}}$; below the knee it also rises at a 3-dB/octave rate. These values equate to a broadband (20 Hz to 20 kHz) equivalent input noise voltage (referenced to 600Ω) of only 529 nV rms—an impressive figure, considering that a standard phonograph cartridge typically generates a 700-nV-rms equivalent output noise over the same bandwidth.

If high-speed capability relates to low total harmonic distortion, then the 332's typical 0.0005% THD figure isn't unexpected: The chip also sports a 20V/μsec slew rate and a 30-MHz gain-bandwidth product. An additional contributor to low-distortion performance is the device's high dynamic range—127 dB.



A nearly complete high-quality audio system, *the MA-332-CP combines a 3.5-nV/ $\sqrt{Hz}$ input-noise spec with a 100-dB open-loop gain and a ±20V output drive capability into a 600Ω load. Operating from ±24V, it draws a quiescent current of only 5 mA and operates stably enough for dc applications.*

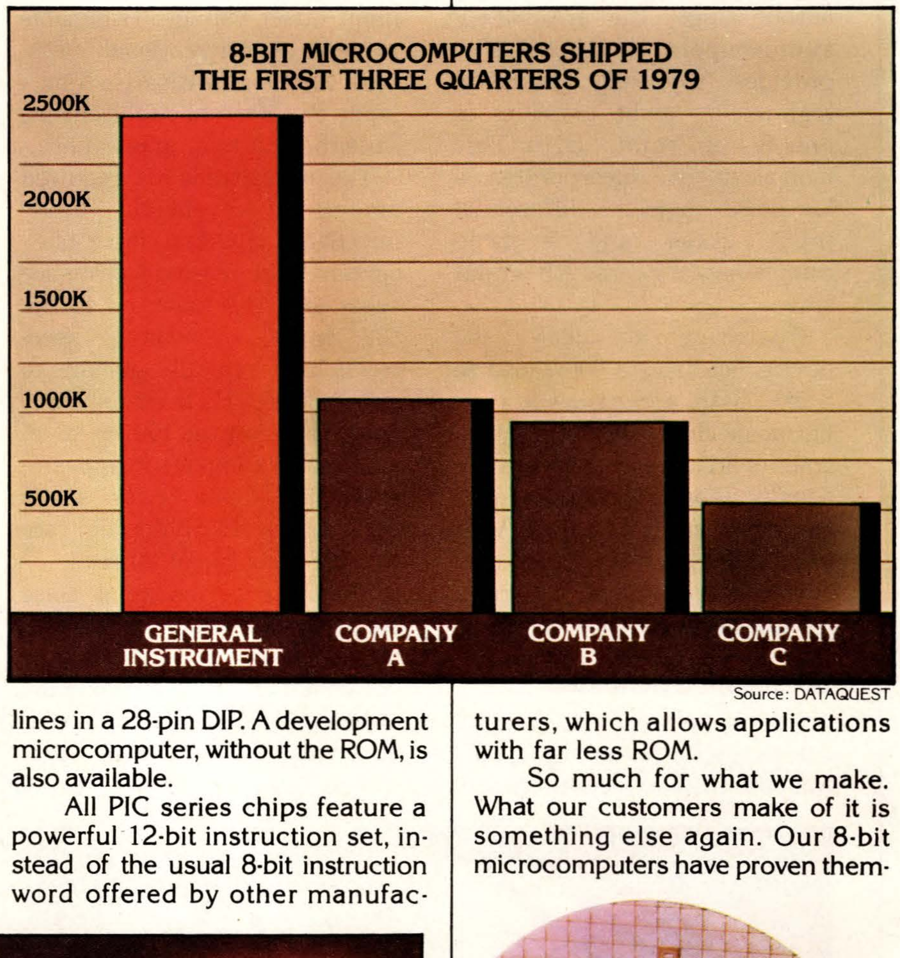
Applications abound

With these performance specs, the 332 should find its way into many sockets. Even without additional outboard power devices, it should work well in many servo applications, such as X-Y-recorder drivers (for which both power and speed are essential) and the control of magnetic-tape and floppy-disc heads.

The amplifier's low input-noise and high output-drive capabilities will also interest remote-instrumentation-system designers — especially for seismic-monitoring applications that can employ the device in direct - coupled arrangements. And obviously, high-fidelity audio-amplifier designs can put the part to good use. $6.75 (25).

Analog Systems, Box 35879, Tucson, AZ 85740. Phone (602) 299-9831. **Circle No 455**

We didn't get to the the most 8-bit



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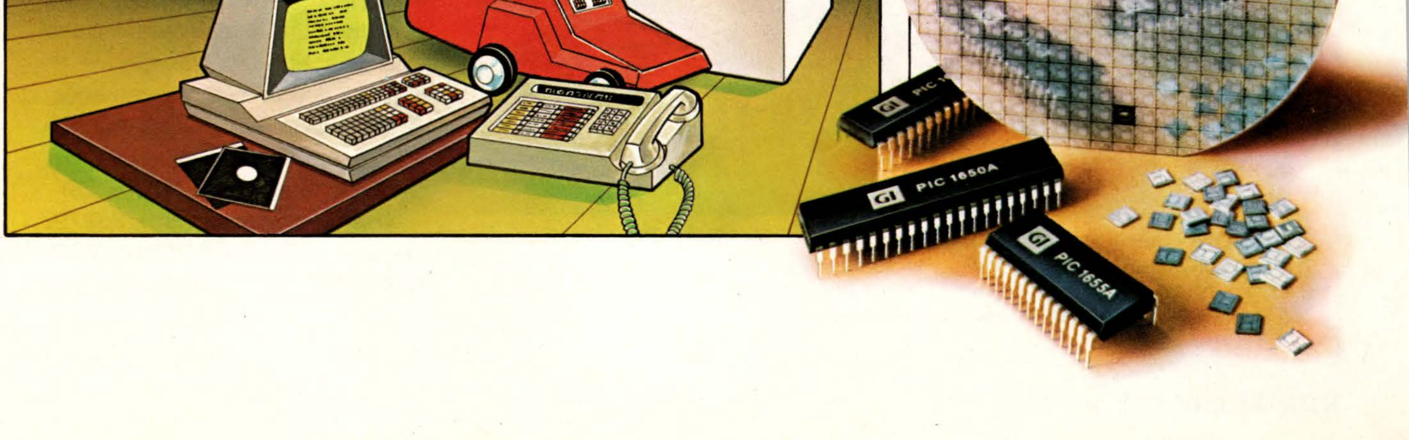
The record speaks for itself. An independent survey revealed that during the first 9 months of 1979 General Instrument had topped all rivals by delivering over two and one-half million 8-bit microcomputers. That's more than twice as much as our nearest competitor.

While it is a most impressive record, to be sure, it's a direct reflection of the success and acceptance of General Instrument's philosophy: To provide products of consistent high quality, backed by comprehensive support and customer service, at competitive prices. Simply stated, we deliver more 8-bit microcomputers, because our microcomputers deliver more to our customers.

Specifically, our popular PIC family consists of the PIC 1650A with 512, 12-bit words of Read-Only-Memory, 32, 8-bit bytes of RAM, 32 I/O lines, real-time clock counter and two-level stack, packaged in a 40-pin DIP. The PIC 1655A is a reduced I/O version,20 I/O lines, packaged in a space-saving 28-pin DIP. Another version, the PIC 1656, has both external and internal interrupts, three-level stack and 20 I/O lines in a 28-pin DIP. A development microcomputer, without the ROM, is also available.

All PIC series chips feature a powerful 12-bit instruction set, instead of the usual 8-bit instruction word offered by other manufacturers, which allows applications with far less ROM.

So much for what we make. What our customers make of it is something else again. Our 8-bit microcomputers have proven them-



top by just delivering microcomputers.

selves in a wide variety of applications, including vending machines, consumer appliances such as washing machines and vacuum cleaners, electronic games, keyboards, display drives, TV/radio tuning systems, industrial timers, motor controls, security systems and automotive dashboard instrumentation. And as long a list as we may come up with, it still isn't long enough, because even as you're reading this, someone is designing a PIC into yet another challenging product application.

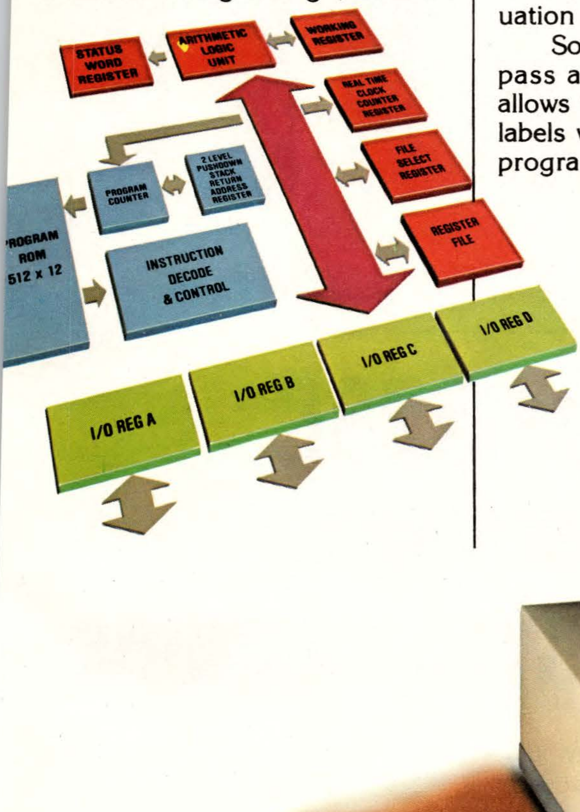
No matter how good a product may be — and ours is second to none — it needs the proper support to realize its full potential. Which is why we offer a complete, inexpensive set of hardware and software aids. This helps our customers in their design, development, and evaluation of a particular application.

Software includes PICAL, a two-pass assembler program, which allows the use of mnemonics and labels when writing the application program. By attaching our PICES In-Circuit Emulation System to any host computer, you instantly have a single-station PIC development system. Rounding out the support group is the PFD Series of PIC Field Demo systems which emulates the PIC Product Line, enabling the demonstration of an application program in the field before it's committed to a masked ROM.

And, as you'd expect, we provide a complete library of information documenting all there is to know about our systems, including a PICAL User Manual, PICES Data Manual, PIC Handbook and PFD Series Data Manual — all yours for the asking. For more information, write or call General Instrument Microelectronics, 600 West John Street, Hicksville, New York 11802, or call (516) 733-3107.

We help you compete.

GENERAL INSTRUMENT



µComputerist Corner

Interchange TRS-80 print statements

Henry G Riekers
Glen Burnie, MD

Interchanging PRINT (print to CRT) and LPRINT (print to line printer) statements when writing, debugging and documenting TRS-80 programs sometimes proves necessary. Although many methods to accomplish this task exist, they risk loss of program control and possible program loss as well.

```
31990 END:REM PRINT LPRINT EDIT ROUTINE
32000 INPUTA$
32010 IFA$="LPRINT"THENA=175:B=178
32020 IFA$<>"LPRINT"THENA=178:B=175
32030 FORM=17129TO20479
32040 IFPEEK(M)=BANDPEEK(M+1)=32THENPOKEM,A
32050 NEXTM
```

Tag this routine *at the end of your TRS-80 programs to provide dynamic interchange of PRINT and LPRINT statement types.*

The short routine shown in the **figure,** when located at the end of a program, alleviates these concerns. When activated, it searches through the program, automatically making the required changes.

The routine searches for PRINT or LPRINT commands followed by a space and makes the necessary replacement. (The trailing space is essential—it prevents the routine from becoming confused by line numbers or stored data with values equivalent to those of PRINT or LPRINT. Thus, leave a space after those specific PRINT or LPRINT statements you wish changed.)

Initiate the routine by typing RUN32000. When the question mark appears, enter PRINT (to change all LPRINTs to PRINTs) or LPRINT (to change all PRINTs to LPRINTs). If you enter any other input, the program automatically converts LPRINTs to PRINTs.

The routine edits in up to 4k of memory—in approximately 1 min of CPU time. To extend the edit to cover 16k, change line 32030 so that the larger number is 32766. **EDN**

Circuit generates pseudorandom numbers

Edward L Cordell
Teledyne Electronics, Newbury Park, CA

A simple random-number generator, such as the one outlined in **Fig 1,** provides 8-bit outputs; you can rewire it to furnish longer words if necessary. Fully static and self starting, this circuit has a maximal-length period of 1.7×10^9 yrs when clocked at 1 MHz.

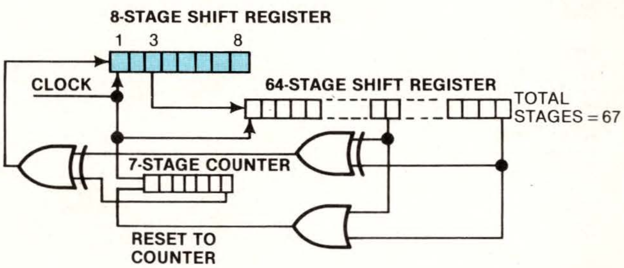


Fig 1—Pseudoindependent words *appear in the 8-bit shift register after every eight clock periods.*

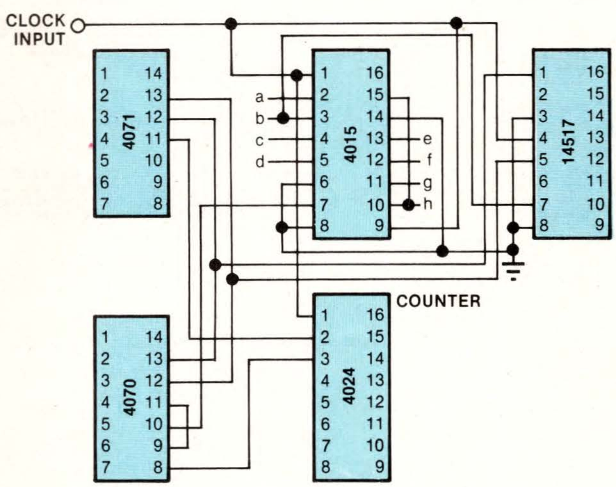


Fig 2—This CMOS circuit *generates pseudorandom bits in a continuous stream at each output of the 8-bit shift register.*

The circuit randomizes by feeding the output of an exclusive-OR gate to its input; its self-starting capability comes from including a binary counter's seventh-stage output (this counter counts clock pulses) in the feedback loop. The 64-stage shift register's 19th and 67th output stages OR together to reset the counter. The shift register's all-ZERO condition permits the counter to count the clock pulses—at a count of 64, ONEs enter the shift register, filling its first 19 stages; the counter then resets.

The actual circuit used to accomplish number generation (**Fig 2**) obtains pseudoindependent 8-bit words by clocking the shift register forward eight bits, then halting the clock while a word is read. You can also obtain longer words from any single shift-register output: Use the output as a source of continuous pseudorandom bits. **EDN**

EDN Software Note #44

Routines improve M6800 PSHX and PULX

David C Pheanis
Arizona State Univ, Tempe

EDN Software Note #5 (March 5, 1978, pg 36) detailed two subroutines (PSHX and PULX) that save the M6800's X register by means of the μP's stack. **Fig 1** illustrates an improved version of PSHX that preserves *all* registers and condition codes in this manner. This program listing is self documenting, and instructions are grouped into logical segments so that each group performs one small function.

Fig 2 presents a listing of an improved version of PULX. Because it preserves the A and B accumulators and the condition codes, you can always use it with no risk of unpleasant side effects.

Note that this PULX employs the same RAM variable (SAVEX) used by the companion PSHX. Sharing storage locations works because the two subroutines never execute simultaneously.

```
                     *      SUBROUTINE  PSHX  PUSHES THE VALUE OF THE  X  REGISTER
                     *  ONTO THE STACK AND REDUCES THE STACK POINTER BY TWO TO
                     *  ACCOUNT FOR THE FACT THAT TWO BYTES HAVE BEEN PUSHED ONTO
                     *  THE STACK.  SUBROUTINE  PSHX  THEREFORE AFFECTS THE STACK
                     *  AS FOLLOWS:

                     *    BEFORE CALLING PSHX              AFTER RETURNING FROM PSHX
                     *    -------------------              -------------------------

                     *           I            I                    I            I
                     *           I            I            SP ---> I            I
                     *           I            I                    I  XR (MSB)  I
                     *  SP ---> I  (UNUSED)  I                    I  XR (LSB)  I
                     *           I------------I                    I------------I

                     *      WHEN SUBROUTINE  PSHX  RETURNS CONTROL TO THE CALLING
                     *  PROGRAM, THE VALUE OF THE  X  REGISTER HAS BEEN PUSHED
                     *  ONTO THE STACK AS INDICATED ABOVE.   THE  A  ACCUMULATOR,
                     *  THE  B  ACCUMULATOR, THE  X  REGISTER, AND THE CONDITION
                     *  CODES ARE ALL PRESERVED.

0000 34       PSHX   DES                  FIRST, DECREMENT THE STACK POINTER
0001 34              DES              TWICE TO RESERVE TWO BYTES ON THE
              *                       STACK FOR THE RETURN ADDRESS.

0002 36              PSHA                 SAVE THE  A  ACCUMULATOR ON THE
0003 07              TPA              STACK, AND ALSO PUT THE CONDITION
0004 36              PSHA             CODES ONTO THE STACK.

0005 FF 0022         STX    SAVEX         SAVE THE VALUE OF THE  X  REGISTER,
0008 30              TSX              AND SET THE  X  REGISTER FOR INDEXING
              *                       INTO THE STACK.

0009 A6 04           LDAA   4,X           COPY THE RETURN ADDRESS FROM BYTES
000B A7 02           STAA   2,X       4 AND 5 OF THE STACK INTO BYTES 2 AND
000D A6 05           LDAA   5,X       3 OF THE STACK SO WE CAN LATER PUT THE
000F A7 03           STAA   3,X       X-REGISTER VALUE INTO BYTES 4 AND 5 OF
              *                       THE STACK.

0011 B6 0022         LDAA   SAVEX         NOW PUT THE X-REGISTER VALUE INTO
0014 A7 04           STAA   4,X       BYTES 4 AND 5 OF THE STACK.
0016 B6 0023         LDAA   SAVEX+1
0019 A7 05           STAA   5,X

001B FE 0022         LDX    SAVEX         FINALLY, RESTORE THE  X  REGISTER,
001E 32              PULA             THE CONDITION CODES, AND THE  A
001F 06              TAP              ACCUMULATOR, AND THEN RETURN TO THE
0020 32              PULA             CALLING PROGRAM.
0021 39              RTS

0022 0002     SAVEX  RMB    2             THESE TWO LOCATIONS, WHICH MUST
              *                       RESIDE IN RAM, ARE USED FOR SAVING THE
              *                       VALUE OF THE  X  REGISTER.

                     END
```

Fig 1—Improve a typical PSHX routine *to preserve all registers and condition codes.*

```
                     *      THIS SUBROUTINE PULLS A VALUE FOR THE  X  REGISTER
                     *  FROM THE STACK.  UPON ENTRY TO SUBROUTINE  PULX  THE STACK
                     *  IS ASSUMED TO BE ORGANIZED AS FOLLOWS:

                     *                       I            I
                     *  STACK POINTER --->I            I  SP + 0
                     *                       I  PR (MSB)  I  SP + 1
                     *                       I  PR (LSB)  I  SP + 2
                     *                       I  XR (MSB)  I  SP + 3
                     *                       I  XR (LSB)  I  SP + 4
                     *                       I------------I

                     *      WHEN SUBROUTINE  PULX  RETURNS CONTROL TO THE CALLING
                     *  PROGRAM, THE  PR  AND  XR  VALUES HAVE BEEN POPPED FROM
                     *  THE STACK, AND THE STACK POINTER HAS BEEN MODIFIED APPRO-
                     *  PRIATELY.   THE  A  ACCUMULATOR, THE  B  ACCUMULATOR, AND
                     *  THE CONDITION CODES ARE ALL PRESERVED.

0000 36       PULX   PSHA                 SAVE THE  A  ACCUMULATOR ON THE
0001 07              TPA              STACK, AND ALSO PUT THE CONDITION
0002 36              PSHA             CODES ONTO THE STACK.

0003 30              TSX                  GET THE X-REGISTER VALUE FROM THE
0004 EE 04           LDX    4,X       STACK, AND PUT IT INTO LOCAL STORAGE.
0006 FF 001B         STX    SAVEX

0009 30              TSX                  NOW COPY THE RETURN ADDRESS FROM
000A A6 02           LDAA   2,X       BYTES 2 AND 3 OF THE STACK INTO BYTES
000C A7 04           STAA   4,X       4 AND 5 OF THE STACK SO THE STACK WILL
000E A6 03           LDAA   3,X       BE CONFIGURED PROPERLY WHEN CONTROL
0010 A7 05           STAA   5,X       RETURNS TO THE CALLING PROGRAM.

0012 FE 001B         LDX    SAVEX         PUT THE X-REGISTER VALUE INTO THE  X
0015 32              PULA             REGISTER, RESTORE THE CONDITION CODES,
0016 06              TAP              AND RESTORE THE VALUE OF THE  A
0017 32              PULA             ACCUMULATOR.

0018 31              INS                  FINALLY, INCREMENT THE STACK POINTER
0019 31              INS              TWICE TO CONFIGURE THE STACK PROPERLY,
001A 39              RTS              AND RETURN TO THE CALLING PROGRAM.

                     END
```

Fig 2—An efficient PULX for general applications, *this routine saves the A and B accumulators and condition codes.*

μComputerist Corner

These two subroutines suit virtually any application. **Fig 3,** on the other hand, illustrates an innovative approach to PULX—one that isn't recommended for general-purpose use.

This PULX routine requires less ROM than the one detailed in **Fig 2,** and it uses no RAM other than the stack. Only one instruction (LDX) in the entire routine isn't a single-byte command. Furthermore, except for the TAP instruction, the single LDX command is the only one that alters the condition codes; the appearance of so many consecutive instructions that don't change condition codes is unusual. Finally, the subroutine's somewhat devious manipulation of the stack is interesting (although potentially confusing).

Although this PULX subroutine works perfectly in many applications, it doesn't function successfully in a system that supports external interrupts. The stack-pointer manipulation, which makes the program a clever one, also leaves it completely vulnerable to an interrupt. **EDN**

```
                  *     THIS SUBROUTINE PULLS A VALUE FOR THE  X  REGISTER
                  *  FROM THE STACK.  UPON ENTRY TO SUBROUTINE  PULX  THE STACK
                  *  IS ASSUMED TO BE ORGANIZED AS FOLLOWS:

                  *                     I              I
                  *  STACK POINTER --->I              I  SP + 0
                  *                     I  PR (MSB)   I  SP + 1
                  *                     I  PR (LSB)   I  SP + 2
                  *                     I  XR (MSB)   I  SP + 3
                  *                     I  XR (LSB)   I  SP + 4
                  *                     I-------------I

                  *     WHEN SUBROUTINE  PULX  RETURNS CONTROL TO THE CALLING
                  *  PROGRAM, THE  PR  AND  XR  VALUES HAVE BEEN POPPED FROM
                  *  THE STACK, AND THE STACK POINTER HAS BEEN MODIFIED APPRO-
                  *  PRIATELY.  THE  A  ACCUMULATOR, THE  B  ACCUMULATOR, AND
                  *  THE CONDITION CODES ARE ALL PRESERVED.

                  *     CAUTION:  THIS SUBROUTINE IS NOT RECOMMENDED FOR USE
                  *  IN SYSTEMS THAT SUPPORT EXTERNAL INTERRUPTS BECAUSE IT
                  *  FAILS IF IT IS INTERRUPTED AT CERTAIN CRITICAL TIMES.

0000 36           PULX   PSHA                 PUT THE  A  ACCUMULATOR AND THE  B
0001 37                  PSHB              ACCUMULATOR ONTO THE STACK SO THEIR
                  *                        VALUES CAN BE RESTORED LATER.

0002 30                  TSX                  GET THE X-REGISTER VALUE FROM THE
0003 07                  TPA               STACK INTO THE  X  REGISTER.  NOTICE
0004 EE 04               LDX    4,X        THAT THE CONDITION CODES ARE TEMPOR-
0006 06                  TAP               ARILY SAVED IN THE  A  ACCUMULATOR AND
                  *                        ARE RESTORED FOLLOWING THE  LDX
                  *                        INSTRUCTION.

0007 31                  INS                  INCREMENT THE STACK POINTER TWICE TO
0008 31                  INS               SKIP OVER THE SAVED VALUES OF THE  A
0009 32                  PULA              AND  B  ACCUMULATORS, AND GET THE
000A 33                  PULB              RETURN ADDRESS INTO THE ACCUMULATORS.

000B 31                  INS                  INCREMENT THE STACK POINTER TWICE,
000C 31                  INS               AND PUT THE RETURN ADDRESS INTO THE
000D 37                  PSHB              STACK WHERE THE X-REGISTER VALUE USED
000E 36                  PSHA              TO BE.

000F 34                  DES                  DECREMENT THE STACK POINTER FOUR
0010 34                  DES               TIMES TO COMPENSATE FOR THE FOUR  INS
0011 34                  DES               INSTRUCTIONS THAT HAVE BEEN EXECUTED.
0012 34                  DES

0013 33                  PULB                 RESTORE THE  B  ACCUMULATOR AND THE
0014 32                  PULA              A  ACCUMULATOR.

0015 31                  INS                  FINALLY, INCREMENT THE STACK POINTER
0016 31                  INS               TWICE TO SKIP OVER THE ORIGINAL RETURN
0017 39                  RTS               ADDRESS, AND RETURN TO THE CALLING
                  *                        PROGRAM.

                         END
```

Fig 3—An innovative approach to implementing PULX *saves both ROM and RAM but doesn't work in systems that support external interrupts.*

A Question of Law

Edited by Jesse Victor

Court upholds exchange agreement's limit on disclosure of confidential data

Professor H Newcomb Morse
Pepperdine University, Malibu, CA

Can a company disclose to another firm information and technology acquired in confidence under a technical exchange agreement once that agreement is terminated, even though the agreement prohibits such disclosure for 24 months after termination?

In the early 1970s, Com-Share Inc filed suit against Computer Complex Inc in US District Court for the Eastern District of Michigan. The suit asked injunctive relief in relation to Com-Share's claim of a breach of a contract providing for the sharing of technical information between the two corporations and for the nondisclosure to third parties of information supplied under that agreement.

Both computer-service corporations offered the use of computer systems on a time-sharing basis. Both were also engaged in developing and marketing computer software. The time-sharing business was a fast-moving operation: Developments in and improvements to technology and software were frequently made and were important not only for the service of existing customers but in attracting new ones.

Agreement provides for exchange of technology

The understanding between the two companies and the subject of the dispute was entered into on February 10, 1967 and termed the technical exchange agreement; the negotiations preceding this agreement began on or around January 1967. Computer Complex's stated objective in concluding such an agreement was to obtain workable systems of time-sharing software and all enhancements to and the maintenance of such software.

Briefly, Com - Share and Computer Complex agreed to provide to each other during the term of the agreement all information concerning hardware (e g, specifications, designs, production drawings, changes, improvements and new designs related to computer components) and software that came into the legal possession of either party. The exchange of applications software in any way proprietary to a user, however, was subject to the express permission of that user. Exchange of technology was to be accomplished by means of magnetic tapes, listings, printouts and other appropriate transfer media.

Consistent with the confidential nature of the information and technology to be exchanged, Section XI of the technical exchange agreement specifically stipulated the following:

"Com-Share and...[Computer Complex Inc] each agree not to lease, sell or otherwise divulge to any third-party interest, without the prior written consent of the other, any and all systems-software developments supplied to it by the other."

Further to safeguard the information and data thus supplied, the agreement also provided, in Section XII, paragraph (e), that:

"Notwithstanding the expiration or termination of this agreement, the limitations set forth in Section XI shall continue for a period of 24 months after such expiration or termination."

From approximately February 1967 through November 1, 1970, therefore, pursuant to the terms of the technical exchange agreement, Com-Share supplied to Computer Complex, in confidence, information, systems software and technology it had developed. In addition, certain of Computer Complex's employees received extensive technical training under the technical exchange agreement at Com-Share's offices.

In particular, pursuant to an amendment to the technical exchange agreement dated August 3, 1970, Com-Share delivered to Computer Complex software developments and technology pertaining to the SDS 940 computer, while such information was in the developmental stages prior to its release to Com-Share's customers.

The systems software supplied by Com-Share to Computer Complex under the technical exchange agreement included monitor and executive programs that were unique and new. Com-Share also provided a languages program, which allowed a user to develop programs of his own. The cost of the systems-software developments and technology supplied by Com-Share to Computer Complex was approximately $2 million.

Technical exchange agreement is terminated

Differences arose between the two parties, and

Continued on pg 89

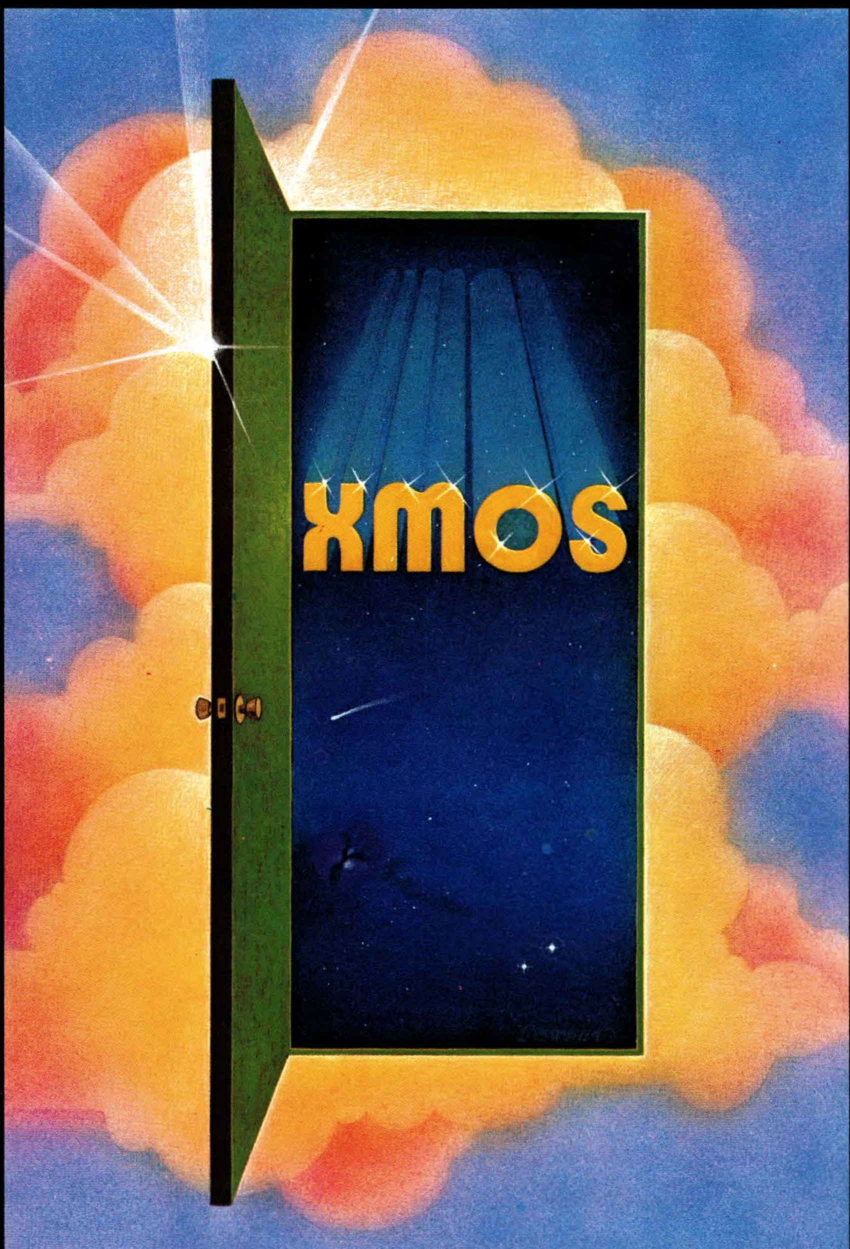
No. 6

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY

Introducing XMOS™ processing.

A new, more practical approach to the 8049 μC.



Introducing STARPLEX™ with I.S.E.™

Universal active filters cut costs

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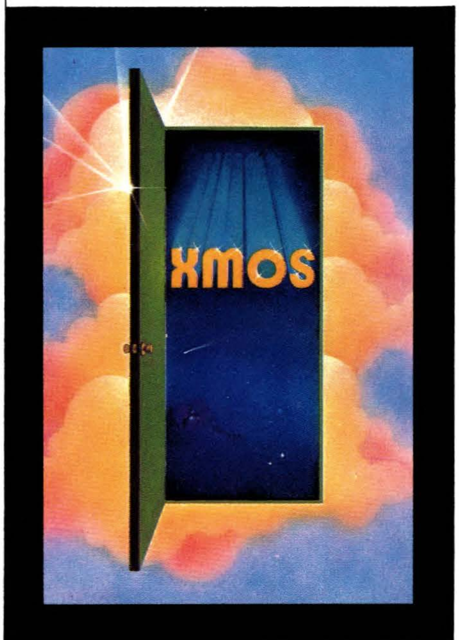
Practicality comes to microcomputing.



XMOS™ process a breakthrough in single-chip μCs.

By combining their new XMOS fabrication process with a modularized "macro" approach to chip layout, National has produced a version of the 8049 μC that is smaller, faster and consumes less power.

The new INS8049, which features 2K x 8 ROM, 128 x 8 RAM and 27 I/O lines on a single chip, is currently available in either 6MHz or 11MHz models. And due to their leading edge XMOS technology, National's INS8049 μCs boast 2.5 and 1.36 μsec cycle times for the 6 and 11MHz versions.

Transparent enhancements. There is also a myriad of transparent improvements that XMOS bestows upon the INS8049. All of which result in considerable reductions in systems costs.

The standby current for the on-chip RAM is mask-programmable depending on how much memory is required. Standby voltage is much less than on other 8049's, which results in a 12- to 35-fold reduction in standby power.

In addition, the INS8049 μC has two mask-programmable port drive options: TTL drive or open drain.

Also on-chip are a battery charging circuit and a Schmitt-triggered interrupt, making it ideal for sophisticated battery-operated applications.

Meet the family. National's 8049 μC is but one of several Series 48 family devices already in production. The INS8048 μC features 1K ROM and 64 bytes RAM. The readily available INS8039 and INS8035 μPs are ROMless versions of the 8049 and 8048.

The INS8050 is the largest member of the 8048 family with 256 bytes of RAM and 4K ROM. It eliminates the need for external memory devices without any software or hardware changes, letting you add more features without adding more components. The INS8040 μP is a ROMless 8050.

See the coupon for additional literature or check with your local distributor for National's INS8243 I/O expander and many other MICROBUS® compatible peripherals.

National's breakthrough XMOS technology gives you the kind of single-chip practicality you've been waiting for. For less than you ever thought possible.

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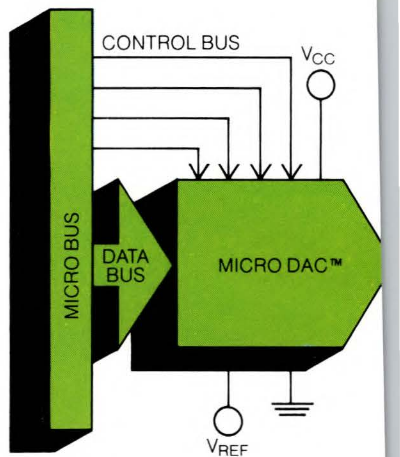
TRANSPARENT ENHANCEMENTS

	INS8049	OTHER 8049s
ACTIVE SUPPLY CURRENT (WORST CASE)	70mA (385mW)	140mA (770mW)
STANDBY SUPPLY CURRENT (WORST CASE)	MASK-PROGRAMMABLE 9mA – 128 WORDS (20mW) 7mA – 96 WORDS (16.5mW) 5mA – 64 WORDS (11mW) 3mA – 32 WORDS (6.6mW)	50mA @ 5V (250mW)
MINIMUM STANDBY VOLTAGE	2.2V (2 NICAD CELLS) $1.50-$2.00 SAVINGS	4.5V (4 to 5 NICADS)
BATTERY CHARGING	NO EXTERNAL COMPONENTS NEEDED	EXTERNAL NETWORK
INTERRUPT PIN	SCHMITT TRIGGER WITH HYSTERESIS	NO HYSTERESIS
PORT PINS	MASK-PROGRAMMABLE CURRENT DRIVE 1. TTL DRIVE 125μA @ 2.4V 2. OPEN DRAIN (10μA MAX)	ONE DRIVE CHARACTERISTIC TTL DRIVE 100μA @ 2.4V

MICRO-DAC Series is the easiest way from D to A.



The DAC1000 is the first of a series of 10-bit four-quadrant multiplying D/As that are truly μP-compatible. That's because each DAC looks like a memory location or an I/O port and has all control functions right on the chip. So you get easy interface with any 8- or 16-bit data bus.

With National's "end point" linearity spec only two adjustments are needed: Zero and Full Scale. Set these, and the linearity specification is met. And linearity is maintained even with a 10-to-1 reduction in reference voltage.

The MICRO-DAC 1000 Series can be used not only for D/A conversion systems, but also as building blocks for digitally controlled amps, alternators, active filters, and even oscillators.

These DACs are also more flexible than any other: 4-quadrant multiplying, double buffered, single supply operation from +5V to +15V, right- or left-justified data format, micropower operation (2mA max), and output current mode setting time of 500ns in a 20-pin DIP.

For non-μP interfacing needs, National has the DAC1020 and DAC1220. These DACs are direct replacements for, and are priced 30% to 300% lower than, the AD7520, AD7521, AD7530, AD7531 or AD7533.

These inexpensive D/As start at $4.00 at 100 pieces. And because of National's volume capacity, no one can sell for less.

MICRO-DAC is a trademark of National Semiconductor Corporation.

Introducing STARPLEX™ with ISE™

The fully developed development system.

The Practical Wizards have done it again.

They've created an easy-to-use development tool that helps design engineers do their whole job on the STARPLEX development system.

STARPLEX can not only develop software for 8080, 8048, 8049, 8050, 8070, NSC800, 8085, and Z-80 microprocessors plus BLC/SBC Series 80 boards, but now with ISE (in-system-emulation) you can also test, analyze and debug prototype hardware/software for the same products.

Multiprocessor capability.

The ISE module is a separate unit incorporating its own CPU, 32K bytes of user-programmable memory and all the necessary logic for breakpoints, tracing and memory mapping.

With ISE, you can simultaneously run two prototype microprocessors (in any combination). So for the first time, you can have real-time emulation or debugging in a multiprocessor environment.

Better yet, since ISE does not share the STARPLEX BUS, the system does not have to compete for memory access with its STARPLEX host. So ISE is the only development tool available that offers real-time emulation with 32K real-time map memory.

There's ISE and there's ISE.

National's easy-to-learn ISE software comes completely integrated into the STARPLEX system, including the unique Automatic Testing or "In-File" capability. In-File is an automatic testing mode that will implement a predefined sequence of tests. ISE can also record those results to show exactly how each part of the system performs during the tests.

Our symbolic debugging capability provides not only the usual breakpoint conditions, but also a "coast" command which allows you to continue executing a program after the breakpoint combination has been satisfied.

Look into our ISE.

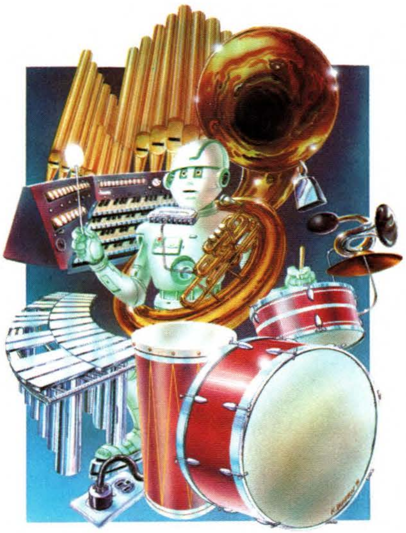
ISE 8048 has all the 8080 features mentioned above plus the ability to read and disassemble internal ROM; make patches in assembly code; support 11 MHz components; support the entire 8048 family; and use prototype crystal clocks.

The Z-80 ISE is a bus-compatible board that plugs directly into STARPLEX. It can support 2-4 MHz Z-80s; provide 4 tracing options; supply relational and regional breakpoints; and provide refresh for prototype memories.

STARPLEX with ISE offers features not found in any other development system, yet it costs substantially less to own and operate than any competitive system.

Practical Wizards, indeed.

Single-chip CRT controllers need less support.



DP8350 Series of programmable controllers most widely used among major CRT makers.

National's powerful CRT controllers require considerably less support circuitry than any other CRTC available. Due in part to single-chip bipolar circuitry, the DP8350 Series CRTCs serve as fully dedicated CRT display refresh circuits in 40-pin packages.

This, combined with the DP8350's enhanced versatility provides an unprecedented ease of system design.

Single-chip versatility.

The DP8350 Series, which includes the DP8350, DP8352 and DP8353 CRTCs, offers a wide range of programmability using internal mask programmable ROMs. In the character field, for example, both the total number of dots per field (up to a 16 x 16 dot matrix) and the number of scan lines per character may be specified. The number of characters per row (from 5 to 110) and character rows per video frame (from 1 to 64) may be programmed as well.

A complete set of video outputs is available including cursor enable, programmable vertical blanking and programmable horizontal and vertical sync.

In addition, the DP8350 CRTCs feature an internal dot rate crystal controlled oscillator. For those systems where a dot rate clock is already provided, the DP8350 Series may use an external clock input. Either way, the buffered dot rate clock output ensures system synchronization.

The DP8350s also provide such system sync and program inputs as 50/60 Hz control, system clear, external character/line rate clock and a character generator program. Also featured are three on-chip registers for external loading of the row starting address, cursor address, and top-of-page address. Twelve bits (4K) of bidirectional TRI-STATE® character memory addresses allow interface to character memory.

DP8350 at the heart of the best designs.

The popular DP8350 Series has already been designed into the terminals made by nearly every major CRT terminal manufacturer. Because the Wizards at National not only offer superior controllers, they also produce a wide variety of complementary design components. Character generators, μPs, memory products, just to name a few.

And what's more, it's all ready for immediate delivery.

Showcasing National's new family of 8-bit A/Ds.

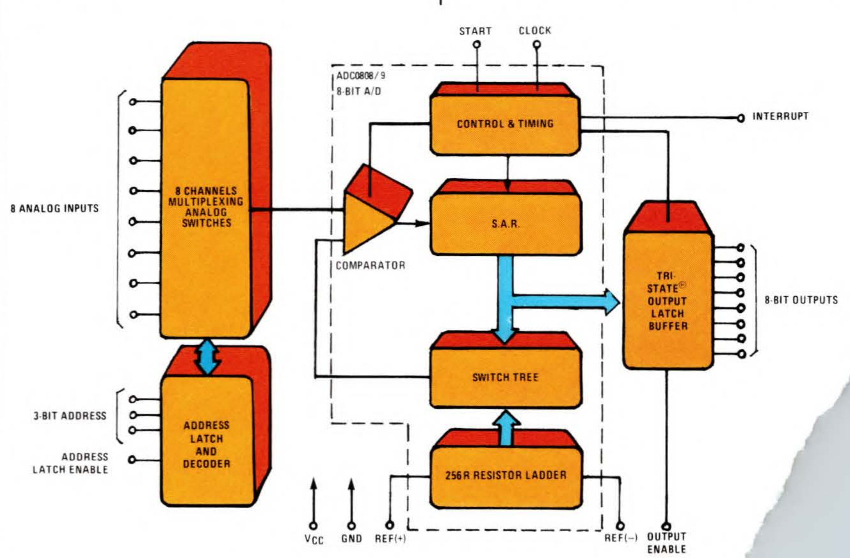
National's 8-bit A/Ds not only interface to any μP bus, they also feature absolute or ratiometric operation, and require just a single 5V supply at almost no current at all.

Of all the 8-bit A/Ds on the market, only National offers single-channel differential analog input A/Ds in 20-pin DIPs – the ADC0801/2/3/4. In addition, their ADC0808/9 8-bit converters feature 8-channel analog input multiplexers, each in a 28-pin DIP. The top-of-the-line ADC0816/17 each contain a 16-channel analog input mux in 40-pin DIPs.

The new line of 100μsec A/D converters eliminates the need for external zero and full-scale adjustments and features an absolute accuracy as good as $\pm$¼ LSB.

National, the leader in innovative, cost-effective data acquisition products, now has the best price/performance of any A/D available. In 100-piece lots, the ADC0804 costs only $2.95; the ADC0809 a low $3.60; the ADC080819 costs just $7.95.

Practical Wizardry strikes again – all the way down to the bottom line.



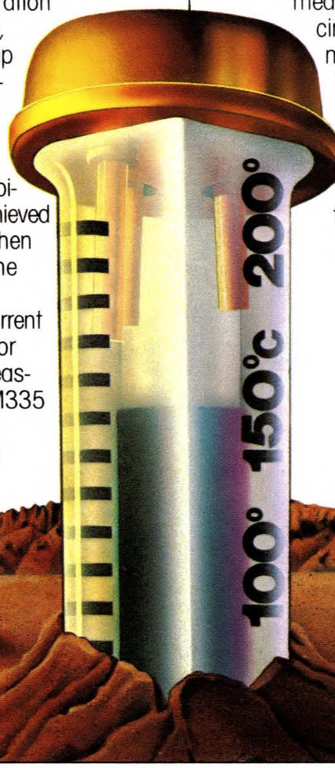
LM335–hot new linear temperature sensor.

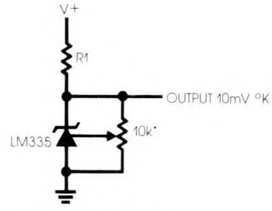
The LM335 is a two-terminal I.C. that looks like a zener with a +10mV/°K temperature coefficient. The LM335 is rated for operation over −55°C to +150°C, and has an over-range up to +200°C. Initial accuracies are available at 1°C, 3°C, 6°C but a third lead makes the LM335 very easy to calibrate. Typically, 1°C accuracy is achieved over the entire range when it's calibrated at only one temperature.

The low operating current means low error even for remote temperature measurement. Further, the LM335 eliminates the need for linearizing circuits, thus making interfacing to a readout or to control circuitry even simpler still.

Whether you're designing measurement control, protection circuitry, solar heating, environmental control or thermostats, National's new series of temperature sensors have a lot going for them.

At only $.95, it's time to start sensing temperature with I.C.s.





*Calibrate for 2.982V at 25° C

LM359 amplifies on current amplifiers.

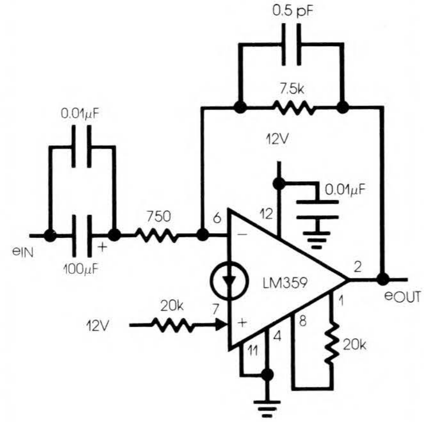
When design engineers said they needed a low-cost dual that was similar to the quad LM3900, but with operation in the video frequency range, the R&D Group at National Semiconductor came up with the answer. It's the LM359 Dual, High Speed, Programmable, Current Mode Norton Amplifier.

The primary design emphasis was placed on high frequency performance and providing user-programmable amplifier operating characteristics.

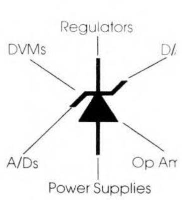
Each amplifier is broadbanded to provide a high gain bandwidth product, (up to 400 MHz), a high 60V/μsec slew rate and stable operation. They're designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

The LM359 solves a lot of applications problems: general purpose video amplifiers; high frequency, high Q active filters; photodiode amplifiers; wide frequency range waveform generation circuits.

Now design and application engineers have what they need, thanks to National Semiconductor.



New LM385 12μW micropower reference. The lowest power reference available.



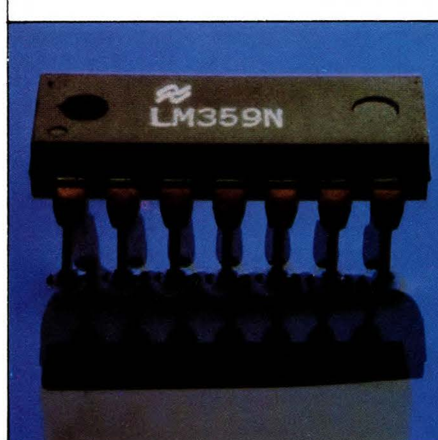
LM385 Design Features

- operating current of 10μA to 20mA
- 1% and 2% initial tolerance
- low voltage reference (1.235V)
- stable under large capacitive loading
- low temperature coefficient
- low noise, good long-term stability
- 1Ω dynamic impedance
- replaces older devices with a tighter tolerance

The new LM385 is yet another example of National Semiconductor's commitment to supply high-performance references. Where power is a primary concern (as in battery-powered equipment, portable meters, or general-purpose analog circuitry with battery life approaching shelf life), this device provides performance unmatched by traditional discrete devices.

For applications requiring other reference voltages or performance specifications, National Semiconductor has the device you're looking for. For example:
- Vref 2.5V; 5.0V; 6.9V; 10V
- Initial Tolerance as low as .01%
- TC max as low as 0.5ppm/°C

Is it any wonder that more and more design engineers are looking to National Semiconductor's linear references to solve problems?



AF100 active filters-a universal solution to cost problems.

In the past, the easiest and least expensive means of active filtering was with discretes. But this is no longer the case thanks to National's new AF100 universal active filters.

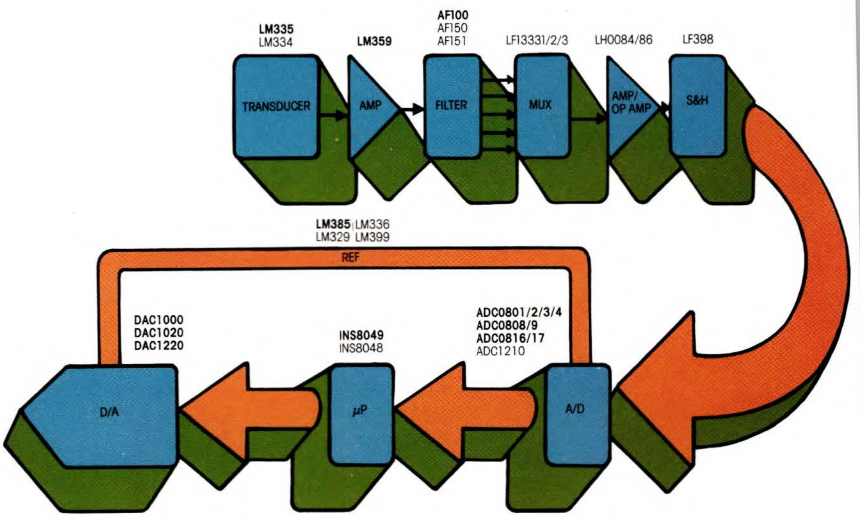
The AF100s are internally adjusted to provide center frequency accuracies of ±2.5% (for the AF100-1CN model) and ±1% (for the AF100-2CN model).

And because of their small size and low external parts count, the AF100 active filters lend themselves perfectly for use in MODEMs and many other telecommunications applications that require lowpass, highpass, or bandpass filter configurations.

But there's more to the price/performance story than just design versatility and decreased manufacturing costs. The AF100 universal active filters are attractively priced as well. By way of illustration, the AF100 is currently available in large quantities for less than $3.00 each.

Just another example of Practical Wizardry cutting your costs to the bone.

Data Acquisition-A National perspective.



Parts listed in bold face are featured in this issue of the National Anthem.

What's new from the National archives?

006 ☐ Special Functions Data Book ($6.00)
012 ☐ DAC 1000 Data Sheet
014 ☐ New Data Acquisition Products Brochure
016 ☐ LM159/359 Data Sheet
017 ☐ LM185/385 Data Sheet
018 ☐ LM135/235/335 Data Sheet
023 ☐ ADC0801, ADC0808, ADC0816 Data Sheets
024 ☐ DP8350 Series Application Notes 198, 199
026 ☐ AF100-1CN, AF100-2CN Data Sheet
028 ☐ STARPLEX Brochure and ISE Data Sheets
030 ☐ INS8049 Data Sheet
033 ☐ Additional Data Acquisition Info

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NA6

A Question of Law

they agreed by letter dated November 30, 1970 that the technical exchange agreement was effectively terminated as of November 1, 1970. This letter, drafted by Computer Complex, provided in part as follows:

"This letter signifies mutual termination of the technical exchange agreement dated February 10, 1967 between our two companies. This termination shall be effective as of November 1, 1970, as of which date neither company requires further performance by the other under the said agreement."

Com-Share's request for a preliminary injunction was triggered in large part by the circumstance that on August 5, 1971, Computer Complex publicly announced that it had entered into an agreement with Tymshare Inc, a California corporation, to sell substantially all of the assets and goodwill related to its computer time-sharing operations to Tymshare.

Com-Share, obviously disturbed by the implications of this development with respect to its confidential data, wrote to both Computer Complex and Tymshare on August 10, 1971 and cited to them the provisions of the relevant paragraphs of the technical exchange agreement. The letter, in addition, stated that Com-Share presumed that Computer Complex would not divulge to Tymshare any information about or pertaining to the systems-software developments that Com-Share had supplied to Computer Complex. Shortly afterward, Com-Share filed its suit.

District Court decides in favor of Com-Share

In 1971, the US District Court rendered a decree in favor of Com-Share and granted injunctive relief. The Court stated:

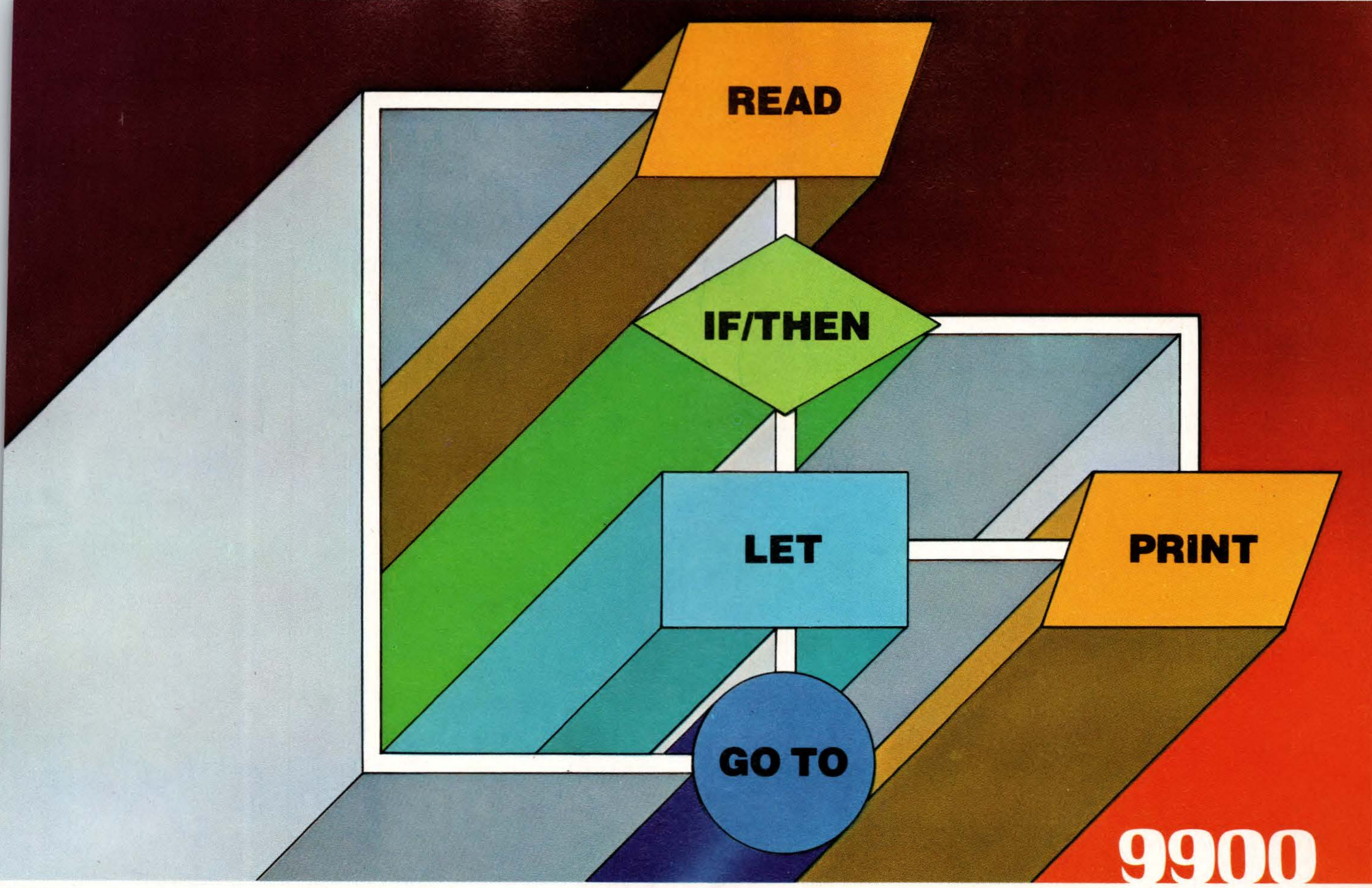
"It is our conclusion...that the disclosures we are about to describe, made by defendant [Computer Complex] were in willful and deliberate violation of the terms of the technical exchange agreement...all at the expense of the plaintiff [Com-Share]....As to the relationship between the parties and the materials furnished...the technical exchange agreement established a confidential relationship between plaintiff and defendant....The systems-software developments supplied by plaintiff to defendant were unique property that constituted trade secrets of plaintiff and were supplied to defendant in confidence under the restraints against sale, lease or disclosure set forth in the technical exchange agreement. The letter dated November 30, 1970 between the plaintiff and the defendant, which provided that 'termination shall be effective as of November 1, 1970, as of which date neither company requires further performance by the other under the said agreement,' is interpreted to mean that as of

A Question of Law

November 1, 1970, neither plaintiff nor defendant required the other to supply technology to the other under the technical exchange agreement. The provision in Section XII, paragraph (e) of the technical exchange agreement continuing the restraint supplied against lease, sale or disclosure of systems-software developments supplied by plaintiff to defendant for a period of 24 months after termination of the technical exchange agreement was not extinguished or waived by the termination letter dated November 30, 1970; this provision survives the termination of the technical exchange agreement and is interpreted to mean that defendant is restrained from selling, leasing or disclosing plaintiff's systems-software developments to any third party prior to November 1, 1972. At this moment, the first duty of this Court is to issue a preliminary injunction as the only adequate means of preserving the status quo. This injunction shall provide that, to the extent, if any, that defendant is unwilling or unable to extricate changes made by defendant to any software supplied to it by plaintiff, defendant cannot sell, transfer or disclose the whole or any part of that portion of the technology which defendant cannot or will not separate; that the injunction shall restrain and enjoin defendant, its directors, officers, employees, agents and all other persons acting in concert with them who receive notice thereof, pending the final determination of this action and thereafter until November 1, 1972, from leasing, selling, transferring or further disclosing to Tymshare Inc, or to any other third party, any of the systems-software developments and technology supplied by plaintiff to defendant pursuant to the technical exchange agreement."

Computer Complex appealed the decision, but the decree of the District Court was affirmed by the US Court of Appeals for the Sixth Circuit. **EDN**

H Newcomb Morse, JD, LL M, FAAFS, received the Juris Doctor degree from Tulane University and the Master of Laws degree from the University of Wisconsin. He was appointed by the late Mayor Richard Daley of Chicago to the Mayor's committee on organized-crime legislation and elected a Fellow of the American Academy of Forensic Sciences. Formerly Professor of Law at DePaul University and Memphis State University, Morse is currently Professor of Law at Pepperdine University. He is also a contributing editor of the *Lawyers' Medical Cyclopedia* and chief contributing editor of *Malpractice and Product Liability Actions Involving Drugs.*



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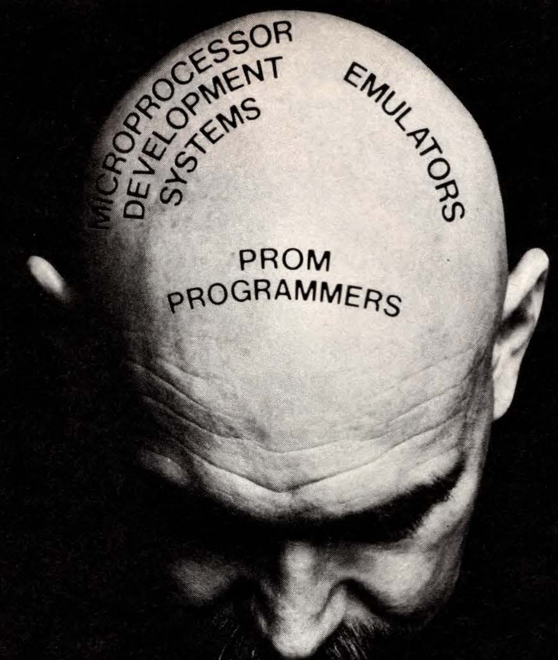

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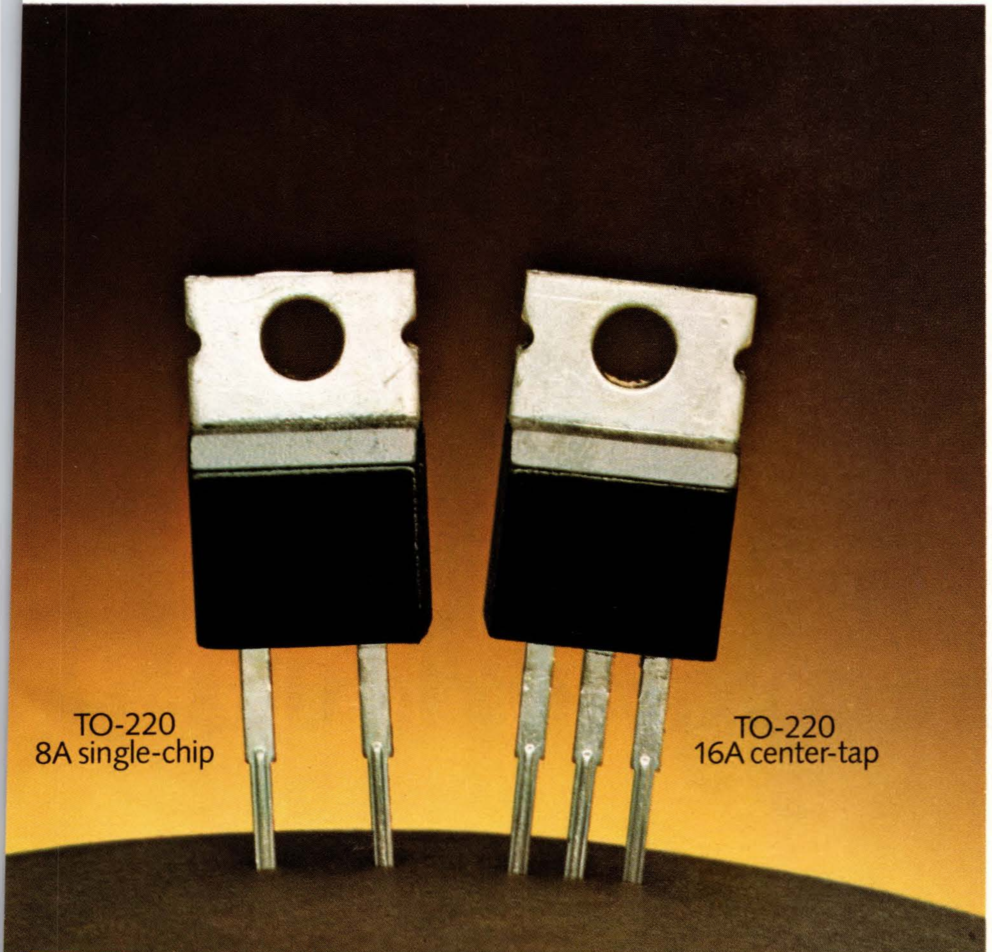

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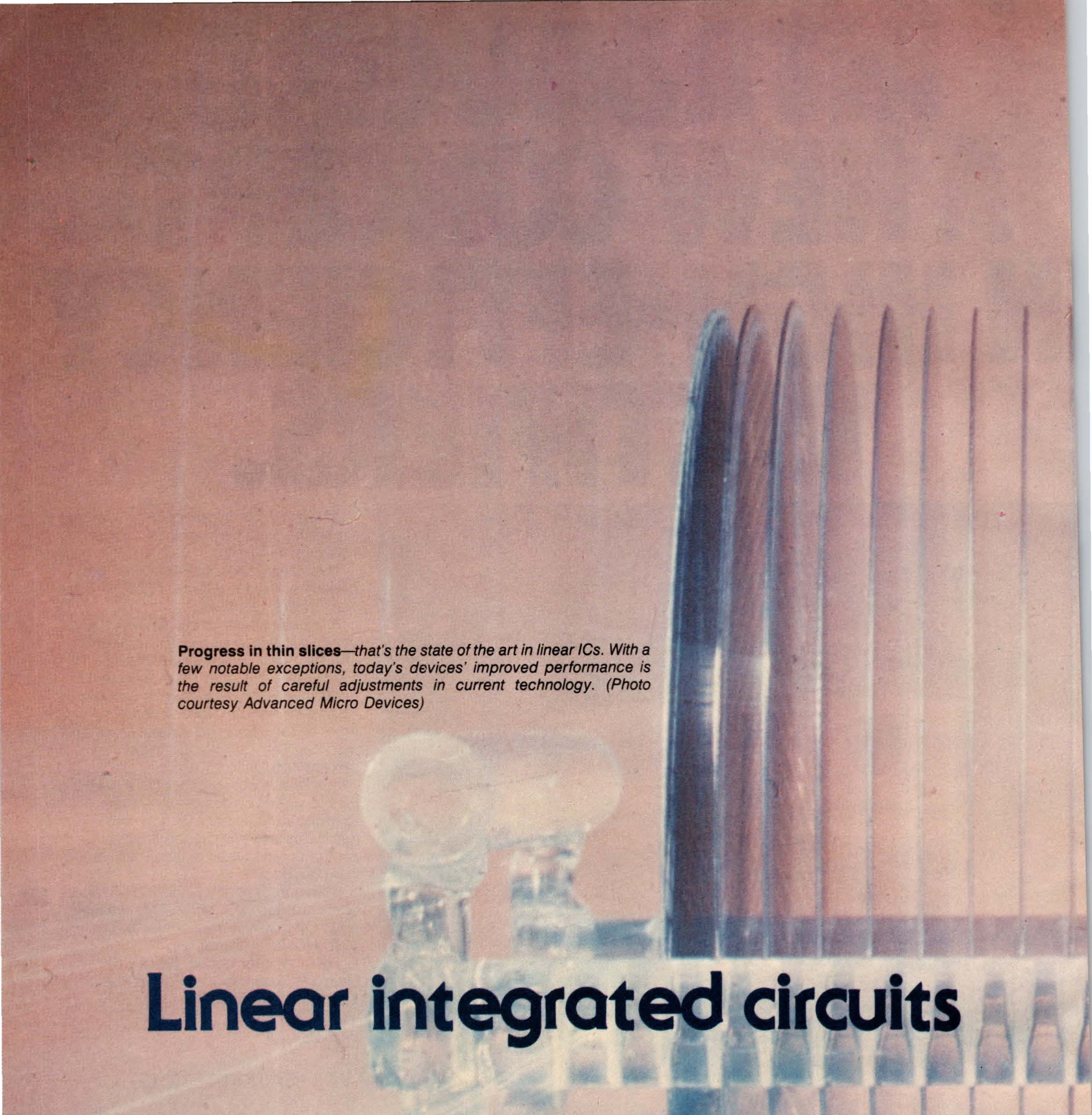


Progress in thin slices—*that's the state of the art in linear ICs. With a few notable exceptions, today's devices' improved performance is the result of careful adjustments in current technology. (Photo courtesy Advanced Micro Devices)*

Linear integrated circuits

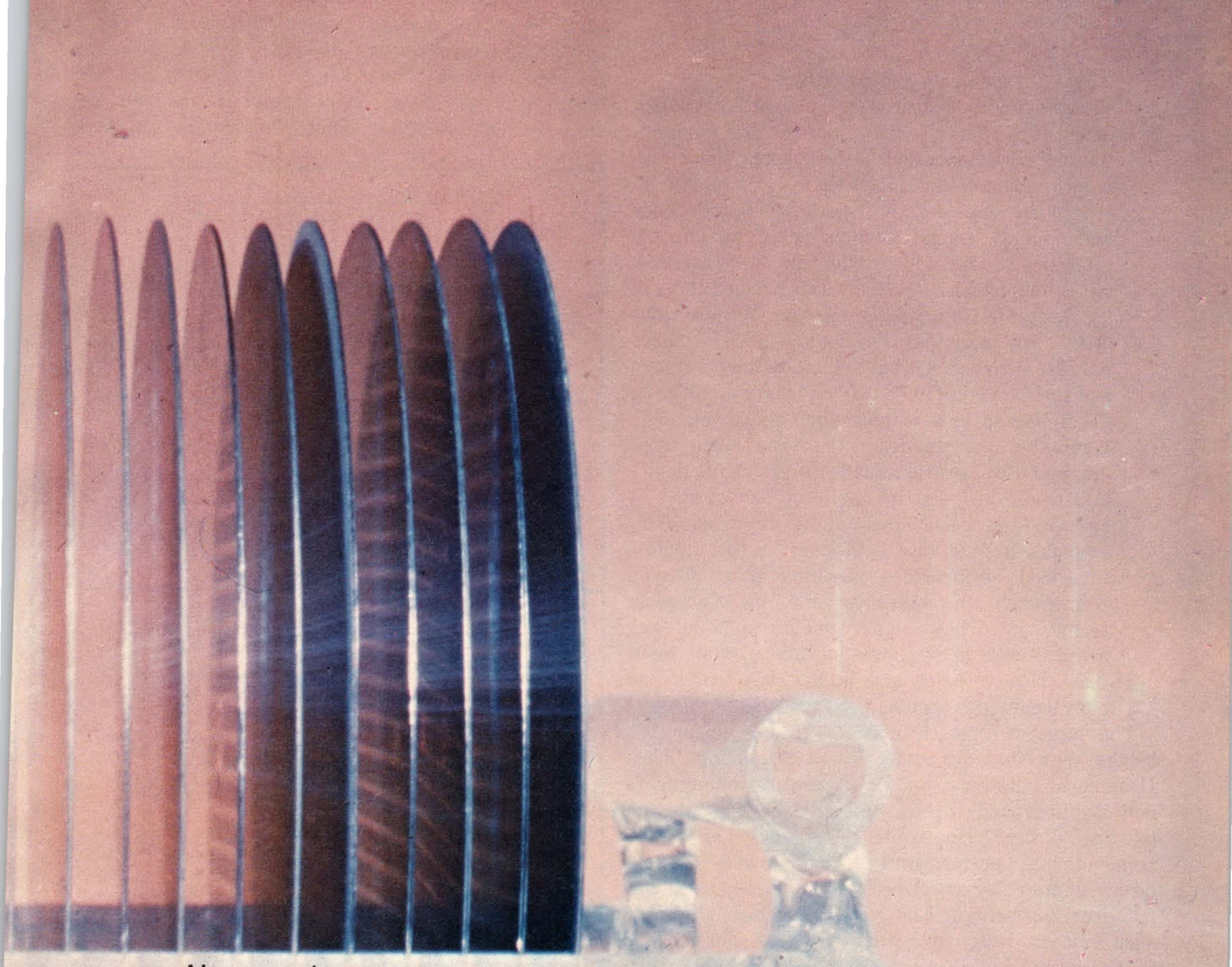
George Huffman, Associate Editor

Despite the sometimes seemingly slow pace of product development, linear ICs *have* come a long way in the past 5 yrs or so—quickly and very quietly. Overshadowed by the fanfare that accompanies each new crop of digital devices, some remarkable linear units—and, more importantly, their design advantages—might have escaped your notice.

The performance improvements of these new linear ICs have, in general, resulted from painstaking tweaking of existing technology. (A very noticeable exception is National's LM11 op amp, which achieves its high performance by means of innovative circuit design.) And the enhanced characteristics of these basic building blocks (amplifiers and comparators, in particular) could in turn enhance your future designs—especially with the aid of some application hints.

The need for such application data becomes apparent when you consider the broad scope of performance improvements in today's linear ICs—and hence the broad range of their potential use:

- Quiet, stable front ends – always sought by audiophiles and instrumentation designers—have achieved some impressive lows. Exar's Type XR-5534A and Signetics' NE5534A, featuring 1-kHz spot-noise characteristics of 3.5 nV/$\sqrt{\text{Hz}}$ and 0.4 pA/$\sqrt{\text{Hz}}$, are fairly representative of the



New-product announcements rarely tell designers just how innovative an IC might really be. A look at some design examples helps underline the considerably increased capabilities of state-of-the-art op amps and comparators.

bipolar breed. If even lower input current noise is a must, consider the FET-input class of devices; Motorola's MC34001 Series (see **box,** "Don't overlook instrumentation amps"), for example, sports a 0.01-pA/$\sqrt{\text{Hz}}$ spec. And in another class of applications in which low noise and high stability are of prime importance—dc power amplifiers—Fairchild's μA714 (one of the quietest op amps available) shines.

- The really fast ICs have become so speedy that you might require a short course in RF circuit-design techniques to apply them effectively. For example, Teledyne Philbrick's Model 1460 hybrid power op amp can output ±30V at 150 mA over a 10-MHz bandwidth. Signetics' NE5539 proves especially useful in video-amplifier circuits, and Precision Monolithics' BUF-03 stands out when employed in a swift and stable unity-gain buffer. Harris' fast comparator, the HA 4950, boasts a ⅛-LSB resolution referenced to 12 bits—extremely high stability for a device with a 40-nsec response time. And even faster comparators (with correspondingly decreased accuracy, of course) offer additional ingenious application possibilities: Advanced Micro Devices' Am687A 8-nsec device makes possible a 100M-bps pulse repeater, and a design employing PMI's CMP-04 demonstrates how one 14-pin DIP can function as a

Slew rate doesn't count at dc; only stability does

versatile time-delay generator.

- Versatility is the featured spec of another group of linear ICs. Not the fastest nor yet the quietest, these devices nonetheless help solve those niggling problems that always seem to crop up in an otherwise neat design. Operation over a very wide supply range, availability of an internal reference voltage and excellent input characteristics combined with a low slew rate are just three of the design-flexibility features many of these chips offer. For example, National's LM11 makes possible a clever self-balancing-amplifier scheme, and the firm's LM10 (EDN, February 5, 1979, pg 91) finds use in a wide-ranging thermometer.
- Even the old standby 741 - type linear IC—estimated by several manufacturers as *the* device still being designed into at least 70% of all new circuits—has been substantially improved. Now available from at least 14 sources, it, too, exhibits improved performance resulting from ongoing refinements in materials and manufacturing technology. These improvements span all key areas: Lower noise, lower and more stable input bias characteristics and higher slew rates and gain-bandwidth products are the results.

The improved performance of today's linear ICs brings with it a potential design stumbling block: Designers must be wary of merely plugging a new-and-improved version of any device into an existing design. For while lower noise or better behaved bias performance seldom upsets a well-designed amplifier or active filter, higher speed might not prove so benign. The compensation employed in such a circuit design hinges on the phase-gain margins of the original device; a faster chip thus might well turn an amplifier into an oscillator. You might even discover that the original power-supply bypassing is no longer adequate—tantalum capacitors are not particularly effective at high frequencies, for example.

All of these considerations hammer home three key interrelated facts: Linear ICs are better than ever; the designs they permit are more ingenious than ever; the care and knowledge required to implement those

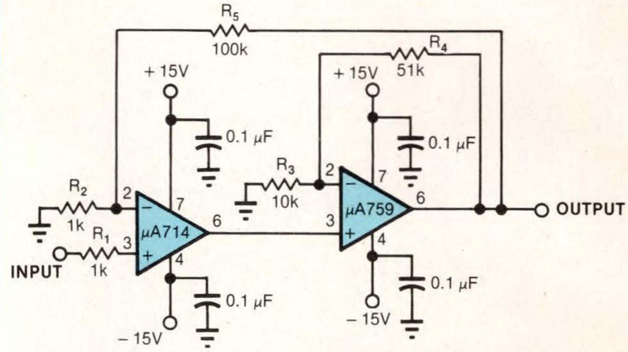


Fig 1—Configured just as is, *this dc-power-amp design sports an output offset of less than 10 mV—not bad, considering that it runs at a gain of 100. And if even that's too much offset, you can always balance the Fairchild μA714 op amp in the conventional manner.*

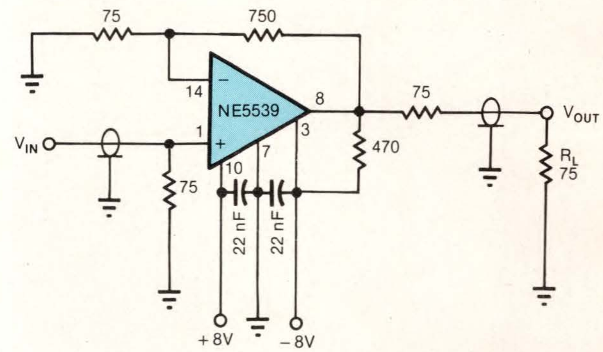
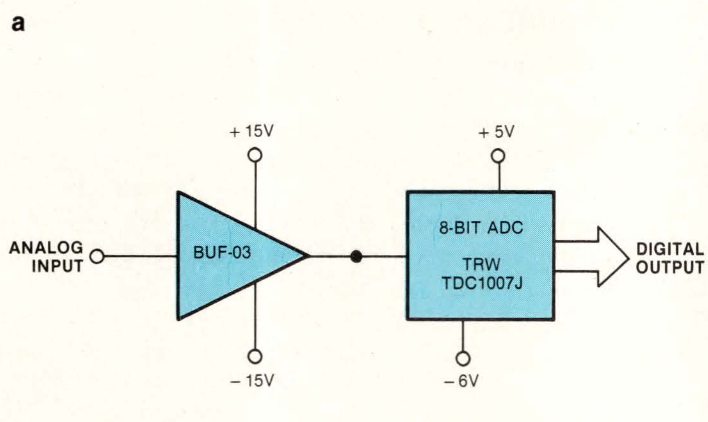


Fig 2—Color-video signals won't suffer *when passing through this Signetics NE5539-based amplifier. The stage's gain equals 20 dB, and total differential phase shift is less than 2°.*



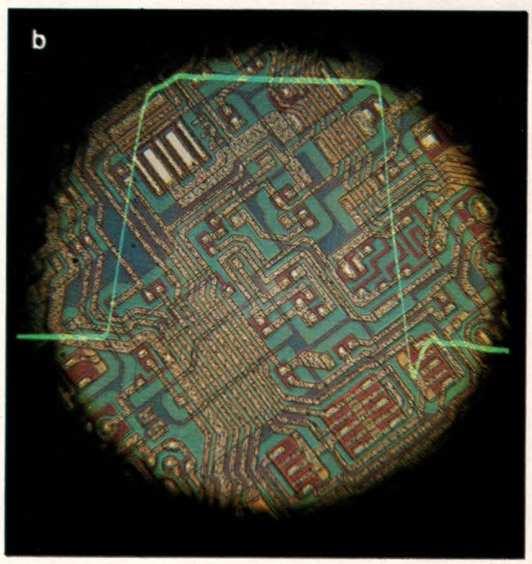


Fig 3—Driving a fast 8-bit ADC *could prove as easy as the block diagram* ***(a)*** *indicates. Both the leading and trailing edges of the 10V pulse* ***(b)*** *slew at 300V/μsec.*

designs are more crucial than ever. And it's this third fact that makes effective application hints an indispensable element of designing with today's linear devices.

DC power amps are still hard to design

This need is more crucial in some areas of circuit design than in others, of course. For example, the basics of low-noise circuit design are familiar: good signal shielding and grounding, careful attention to thermal gradients, use of low-leakage components, etc. Follow them in low-frequency settings and all you usually have to do is plug in a quieter chip, sit back and enjoy a better sounding audio system. One such quieter chip is Analog Systems' MA-332-CP high-performance audio op amp, which includes 1-kHz spot-noise specs of $3.5\ nV/\sqrt{Hz}$ and $400\ pA/\sqrt{Hz}$ among its key characteristics (see pg 73 in this issue).

Even in low-noise design, though, pitfalls can appear. As Fairchild applications engineer Jeff Thompson points out, "quiet isn't everything—not when total harmonic distortion has (perhaps) been sacrificed." The investigation of the relationship between THD and amplifier slew rate is one of Thompson's present projects, and his results should prove interesting.

An area where application hints are more critical, however, encompasses dc power amplifiers. The noninverting circuit shown in **Fig 1** employs the very low-noise Fairchild μA714, combining that device's very low offset with the 759's relatively high output-current capability. Overall gain equals 100 (R_5/R_2). With the component values shown, *output* offset is less than 10 mV, and the 759 can deliver as much as 100 mA at 10V dc when equipped with suitable heat sinking. You'll find a fairly standard method for reducing the offset even further in the μA714's data sheet.

Color-TV fidelity in a chip

If your designs call for higher frequency (1-GHz) operation, you'll appreciate Signetics' Type NE5539. This innocent-appearing 14-pin DIP boasts a 1.2-GHz gain-bandwidth product and a 600V/μsec slew rate. However, if you're not already familiar with color-video systems, coax-cable drivers or fast pulse amplifiers (and therefore with VHF-circuit design), you might have trouble taming this chip. Advanced Analog Systems, Los Altos, CA, offers an evaluation kit (circuit board, NE5539 and other components) to help you get started.

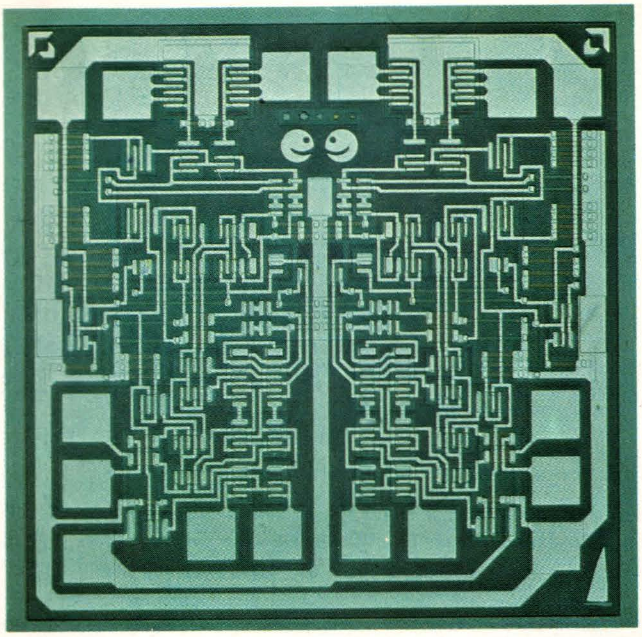


Fig 4—A pair of 8-nsec comparators *occupy this 56-mil^2 chip from Advanced Micro Devices. Providing direct interfacing to ECL and 50Ω lines, the Am687A is a capable pulse amplifier, too.*

Color fidelity in video systems is very sensitive to the differential phase errors accumulated between transmitter and receiver. The NE5539-based video-amplifier design depicted in **Fig 2** doesn't exhibit this difficulty; its overall differential phase error is less than 2°. The circuit is optimized for a 75Ω system at a voltage gain of 10 (20 dB), and if you're acquainted with broadband ferrite-loaded transmission-line-transformer designs, you've probably already thought up some interesting

The op-amp cross reference that almost was

In developing this Special Report, we attempted to compile and publish what would have been (as it turned out) an industry first—a completely up-to-date and unbiased op-amp cross reference, organized on a best-of-breed basis. With the help of this compendium, for example, if your next design's most critical performance parameters were low spot-noise voltage at 10 Hz and high CMRR, you would have been able to determine which devices from which manufacturers best meet those requirements, then ascertain the tradeoffs involved in employing them.

So much for idealism; unfortunately, reality intervened. Our first problem was lack of data; many devices simply aren't characterized thoroughly enough. For example, their spec sheets might contain noise-performance figures at two frequencies, but not at (or near enough to) the frequency of interest. And without knowing where the knee of this noise-performance curve is, a potential user can't even calculate the values needed.

Our second problem in attempting to compile the cross reference centered on the undefined test methods often employed in obtaining what data is available. Apparently, the industry has never standardized many test methods for op amps and other devices. Alternatively, if such standards *do* exist, they aren't being faithfully adhered to.

The bottom line? For now, if you need data on the best op amp for your design, perseverance and the use of United Technical Publications' *IC Master* still seem to be your best hope.

circuit modifications.

High-speed design can also pose other, equally difficult problems—for example, when you must interface a very high-impedance transducer with a low-impedance ADC. With an input resistance of $10^{11}\Omega$, an output resistance of only 2Ω and a 55-MHz bandwidth, PMI's BUF-03 gain-of-one buffer could be the solution in such cases.

Fast (33-nsec) 8-bit ADCs similar to TRW's TDC1007J have an input impedance of 5 kΩ and 300 pF—difficult to drive with most op amps. The answer to this dilemma could be as simple as the basic block diagram shown in **Fig 3a.** The BUF-03 requires ±15V and the ADC +5 and −6V; the circuit must be carefully laid out and bypassed, of course.

Comparators come in two forms—both improved

High speed also plays a part in the latest comparator product offerings: With a maximum propagation delay of only 8 nsec, Advanced Micro Devices' Type Am687A dual comparators (**Fig 4**) are very fast indeed. Operating from +5 and −5.2V supplies, these devices sport complementary ECL outputs and can directly drive 50Ω lines. Flash converters are obvious application candidates for these comparators; a very fast pulse repeater is less obvious but also feasible.

In this latter application, alternate bipolar encoding of standard serial digital information looks like the input signal depicted in **Fig 5:** ZEROs are represented by a zero level, but ONEs are indicated by either a positive or negative level—the signal changes polarity

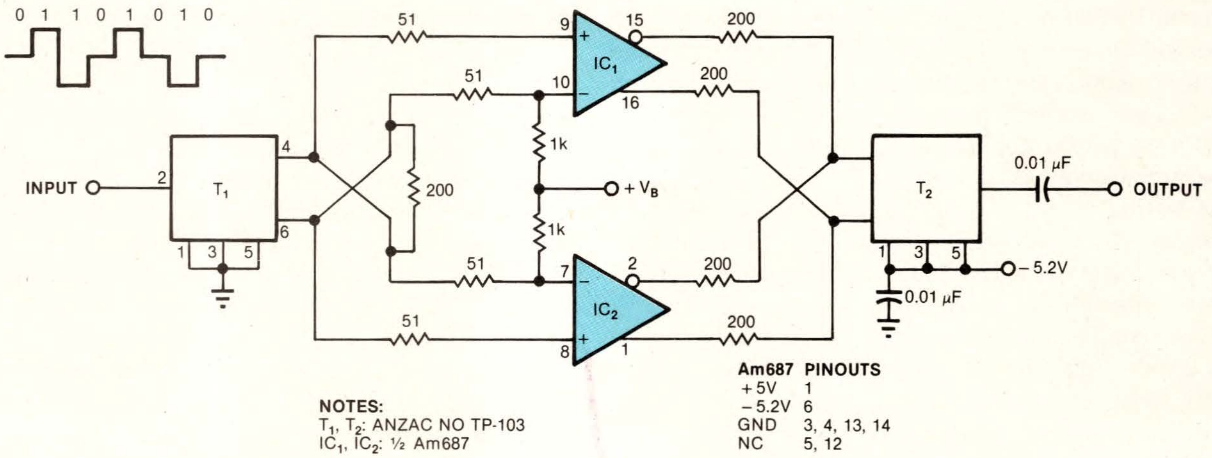


Fig 5—Balanced input and output *make this fast pulse repeater simple to implement. Requiring standard ECL-level power supplies, this design has achieved 100M-bps data rates.*

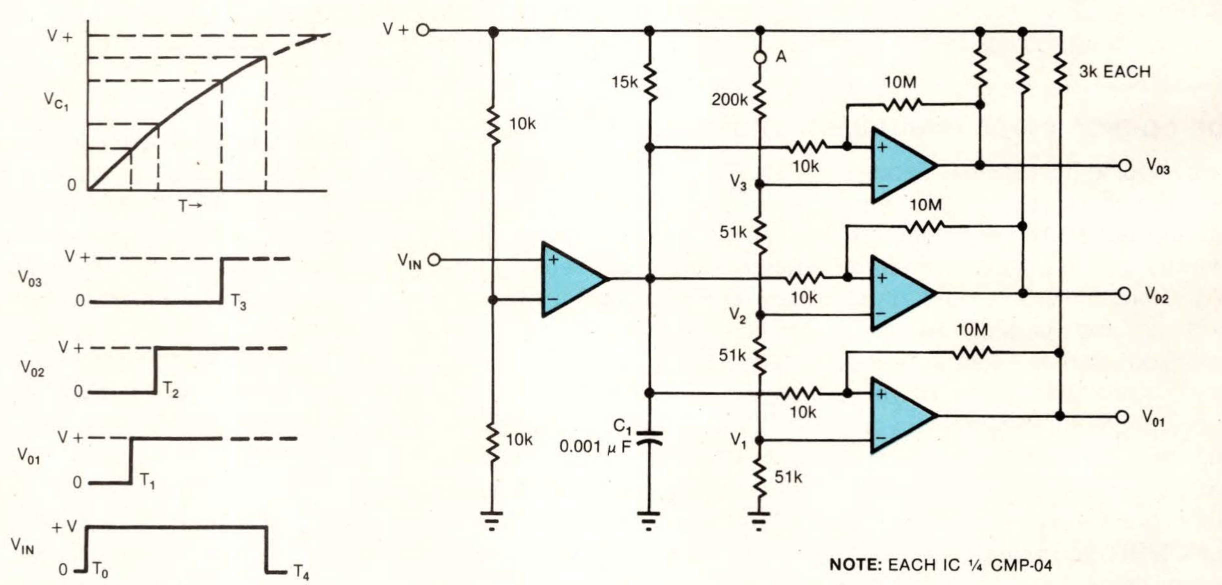


Fig 6—Shown here as a multistage fixed-delay generator, *this design could easily be modified to permit modulation of the various delay times. The four comparators, from Precision Monolithics Inc, are all housed in the same 14-pin DIP—thereby ensuring excellent thermal tracking.*

each time a ONE occurs. Such encoding offers two advantages. First, the spectral nulls that exist at both dc and the bit rate considerably simplify any subsequent signal filtering. Second, because dc restoration isn't required, ac coupling can be employed.

Detecting this type of code is simple: The comparators' inputs are biased and driven to form detectors for the positive and negative pulses—rather like a push-pull connection—and the outputs are wire ORed. Broadband transmission-line transformers handle signal division and phase inversion at the input and signal recombination at the output.

A low bias voltage (V_B) might prove necessary to set the ZERO-discrimination level. Although nothing more than a basic regenerative repeater, this circuit has functioned successfully with 30 dB of flat (equalized) attenuation at data-transmission rates up to 100M bps.

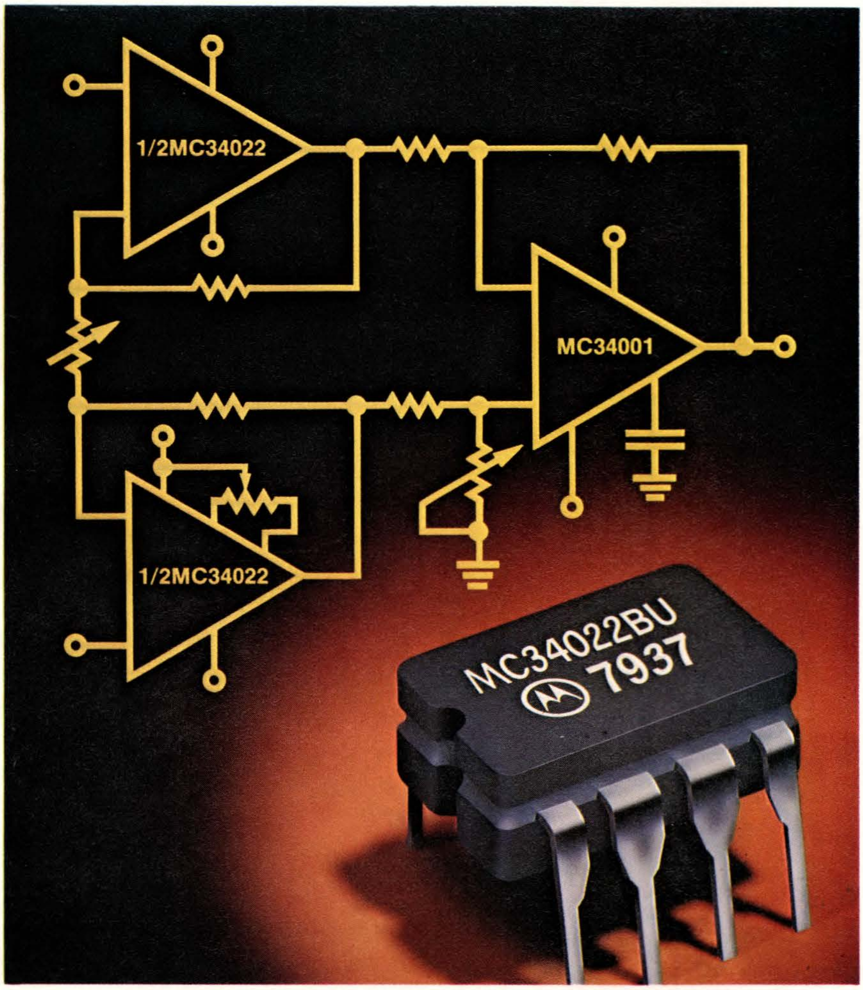
Another unusual comparator application appears in **Fig 6** and employs PMI's low-power quad unit, the CMP-04. With input offset voltage spec'd at 1 mV max and a 10-nA max input offset current, outboard offset adjustments aren't needed. Supply voltage can range from 5 to 36V, and the required current remains 2 mA—a feature that's very useful in battery-powered equipment.

Where's the tradeoff? In speed. Under standard test conditions, the CMP-04 responds in 1.3 μsec, as opposed to the Am687A's 8 nsec. In return for this lowered speed, though, you get much lower input offsets and total power requirements.

Don't overlook instrumentation amps

As Analog Devices' Jeff Riskin points out in his *A User's Guide to IC Instrumentation Amplifiers,* "an instrumentation amplifier is a precision differential-voltage-gain device optimized for operation in an environment hostile to precision measurement." By providing many of the classical cut-and-try design functions in a ready-to-use package, this class of linear ICs can greatly simplify real-world circuit design.

According to Riskin, such design is characterized by deviations from the ideal: "Temperature fluctuates, electrical noise exists and voltage drops caused by current through the resistance of leads from remote locations are dictated by the laws of physics. Furthermore, real transducers rarely exhibit zero output impedance and nice, neat 0 to 10V ranges. Induced, leaked or coupled electrical interference (noise) is always present to some extent. In brief, even the best 'cookbook' must be taken with a grain of salt."



The classical approach to instrumentation-amp design *involves utilizing op amps with low input bias current. (Motorola's FET-input MC34022 achieves a 30-pA figure for this spec.) In many cases, though, an IC instrumentation amp proves less troublesome.*

The classical approach to do-it-yourself instrumentation-amplifier design appears in the **photo**—you combine several op amps and resistors in the hope that somehow everything will track. Sometimes that's the only way you can attain the required performance.

However, sometimes all of the hard work has already been done. With Analog Devices' AD521 instrumentation amp, for example, gain is adjustable from 0.1 to 1000 by varying just two resistors. And you can achieve this wide gain range without upsetting the device's high (120 dB) CMRR and $3\times10^9\Omega$ input impedance. Output impedance equals 0.1Ω, and rated output swing is ±10V into 1 kΩ. Combined with a gain-bandwidth product of 40 MHz, these specs are hard to equal with the classical approach.

High-speed comparators provide several design opportunities

Fig 6's delay generator is very basic and therefore very versatile. For example, you could choose the threshold-determining resistors to provide any other ratio of delays. Furthermore, the point marked A could (instead of being referenced to the supply voltage) be tied to some other reference source capable of modulating the total delay time. The design possibilities are numerous.

If all else fails, invent it

There's no doubt about it: The newest crop of linear ICs provides the specific characteristics—low noise, high stability, high speed—often required to solve a particularly tricky design problem. Indeed, plugging the hard-to-fill gaps in a system block diagram can actually be fun. All you need is an awareness of the versatility of some of the available ICs—another case for the importance of detailed application information.

One recent linear IC whose application potential has been extensively documented is National's LM11 op amp (EDN, February 5, pg 119). Indeed, the device is so versatile that Bob Dobkin, the firm's director of advanced-circuit development, claims that "any (circuit) designer who requires the very highest stability and performance from a low-frequency amplifier will have to use it."

The composite-amplifier scheme pictured in **Fig 7** demonstrates this point. Intentionally employing the LM11's very low slew rate and its very high dc stability to control the LF351 wide-bandwidth FET amp's offset provides a best-of-both-worlds design. (Although not shown, still better performance is achievable by balancing out what little offset the LM11 does exhibit.)

Because the LM11 has a very low slew rate, it can accommodate very fast input transients without attempting to follow them and can therefore continuously servo out the LF351's offset errors. The result? The composite amplifier's range effectively extends down to dc without any appreciable effect on its upper frequency limit.

As another example of how you can exploit the "hidden" features of some of today's linear ICs, consider the electronic thermometer depicted in **Fig 8.** Even though the LM134 is usually described as a 3-terminal adjustable current source, it's also an accurate temperature sensor. Although not tested below 1.5V, it can generally operate down to 1V with 0.5°C accuracy. Furthermore, the LM10 op amp—in addition to featuring low-voltage capability—contains (and outputs) the stable voltage employed as the reference in this design.

Useful over the −55 to +150°C range, the LM134 develops a current proportional to absolute temperature. The reference and op amp provide this output with the desired zero offset (R_2) and range expansion (R_3). The resulting direct readout is in degrees Celsius (or degrees Fahrenheit if so calibrated). As shown, the 100-μA FS meter covers the 0 to 100°C span.

Further examples of linear ICs with "hidden" versatility include operational transconductance amplifiers such as the RCA CA3080 and 3280 and the LM13600 from National and Exar (EDN, August 20, 1979, pg 70), and National's LM359 dual current-differencing (Norton) amp (EDN, September 20, 1979, pg 99). Yet another such IC is Intersil's commutating autozero (CAZ) op amp (EDN, September 20, 1979, pg 46).

The CAZ amp employs what amounts to an internal sample-and-hold technique to achieve self balancing of

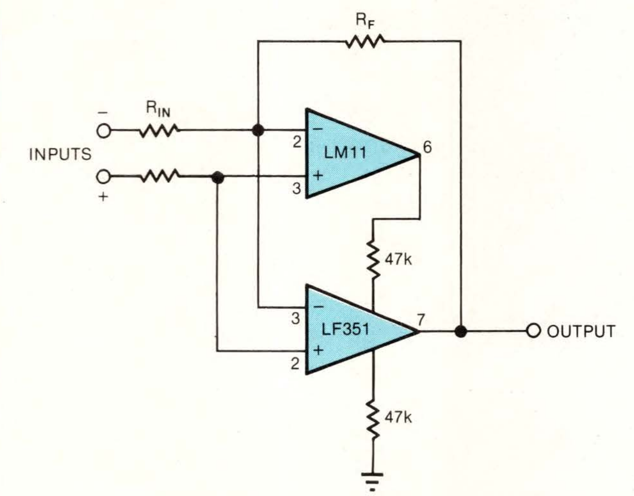


Fig 7—The low slew rate *of the National Semiconductor LM11 permits it to servo out the much faster LF351's offset voltages without compromising the latter device's speed. Achieving even higher stability is possible by also balancing out the LM11.*

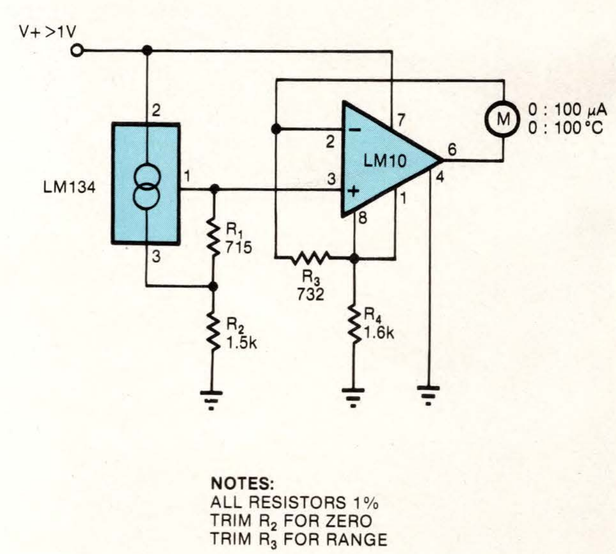


Fig 8—Operating from a single D cell, *this electronic thermometer employs the National LM10 as both a reference and an amplifier; the LM134 serves as a temperature sensor.*

Major linear-IC manufacturers

For more information on devices described in this article or on other linear ICs, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94086
(408) 732-2400
Circle No 404

Analog Devices Inc
Box 280
Norwood, MA 02062
(617) 329-4700
Circle No 405

Analog Systems
Box 35879
Tucson, AZ 85740
(602) 299-9831
Circle No 438

Beckman Instruments Inc
2500 Harbor Blvd
Fullerton, CA 92634
(714) 871-4848
Circle No 406

Burr-Brown
Box 11400
Tucson, AZ 85734
(602) 746-1111
Circle No 407

Cherry Semiconductor Corp
99 Bald Hill Rd
Cranston, RI 02920
(401) 463-6000
Circle No 408

Datel Systems Inc
11 Cabot Blvd
Mansfield, MA 02048
(617) 339-9341
Circle No 409

Dionics Inc
65 Rushmore St
Westbury, NY 11590
(516) 997-7474
Circle No 410

EG&G Reticon
345 Potrero Ave
Sunnyvale, CA 94086
(408) 738-4266
Circle No 411

Exar Integrated Systems
Box 62229
Sunnyvale, CA 94088
(408) 732-7970
Circle No 412

Fairchild Semiconductor
464 Ellis St
Mt View, CA 94042
(415) 962-5011
Circle No 413

Ferranti Electric
East Bethpage Rd
Plainview, NY 11803
(516) 293-8383
Circle No 414

General Instrument Corp
Microelectronics Div
600 W John St
Hicksville, NY 11802
(516) 733-3107
Circle No 415

Harris Corp
Semiconductor Products Div
Box 883
Melbourne, FL 32901
(305) 724-7407
Circle No 416

Intech/Function Modules Inc
282 Brokaw Rd
Santa Clara, CA 95050
(408) 244-0500
Circle 417

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-8080
Circle No 418

Intersil Inc
10710 N Tantau Ave
Cupertino, CA 95014
(408) 996-5000
Circle No 419

Intronics Inc
57 Chapel St
Newton, MA 02158
(617) 332-7350
Circle No 420

ITT Semiconductors
74 Commerce Way
Woburn, MA 01801
(617) 935-7910
Circle No 421

Micro Power Systems Inc
3100 Alfred St
Santa Clara, CA 95050
(408) 247-5350
Circle No 422

Motorola Semiconductor Products Inc
Box 20912
Phoenix, AZ 85036
(602) 244-6900
Circle No 423

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
(408) 737-5000
Circle No 424

NEC America Inc
3070 Lawrence Expressway
Santa Clara, CA 95051
(408) 738-2180
Circle No 425

Optical Electronics Inc
Box 11140
Tucson, AZ 85734
(602) 624-8358
Circle No 439

Panasonic
One Panasonic Way
Secaucus, NJ 07094
(201) 348-7000
Circle No 426

Plessey Semiconductors
1641 Kaiser Ave
Santa Ana, CA 92715
(714) 540-9979
Circle No 427

Precision Monolithics Inc
1500 Space Park Dr
Santa Clara, CA 95050
(408) 246-9222
Circle No 428

Raytheon Co
Semiconductor Div
350 Ellis St
Mt View, CA 94042
(415) 968-9211
Circle No 429

RCA
Solid State Div
Rte 202
Somerville, NJ 08876
(201) 685-6000
Circle No 430

SGS-ATES Semiconductor Corp
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Waltham, MA 02154
(617) 891-3710
Circle No 431

Siemens Corp
186 Wood Ave South
Iselin, NJ 08830
(201) 494-1000
Circle No 440

Signetics Corp
Box 9052
Sunnyvale, CA 94086
(408) 739-7700
Circle No 432

Silicon General Inc
11651 Monarch St
Garden Grove, CA 92641
(714) 892-5531
Circle No 433

Siliconix Inc
2201 Laurelwood Rd
Santa Clara, CA 95054
(408) 246-8000
Circle No 434

Sprague Electric Co
645 Marshall St
North Adams, MA 02147
(413) 664-4411
Circle No 435

Teledyne Philbrick
Allied Dr at Rte 128
Dedham, MA 02026
(617) 329-1600
Circle No 436

Texas Instruments Inc
Box 5012, MS 84
Dallas, TX 75222
(214) 238-2011
Circle No 437

TRW Semiconductor
14520 Aviation Blvd
Lawndale, CA 90260
(213) 679-4561
Circle No 403

input-bias offsets and drift. The result? A dc op amp with remarkable stability—input offset-voltage drift of 200 nV/yr and 5 nV/°C. A 100-dB open-loop gain and a 4 to 16V operating supply range put the CAZ-amp family in a class by itself; Intersil's ICL7600 and 7605 data sheets describe some interesting applications.

Many of these new devices are second sourced. Micro Power Systems, for example, produces most of the premier units offered by PMI, Analog Devices, Harris, Intersil and Siliconix and is probably working on the rest. Furthermore, MPS president John Hall understands low-noise-device technology and has written a paper (available from the firm) that discusses the sources of amplifier-noise and bias-stability problems. In it, he also points out some of the common errors made in specifying and measuring low-noise devices. The paper is quite useful and is one more source of the key application data so necessary to apply today's linear ICs effectively. **EDN**

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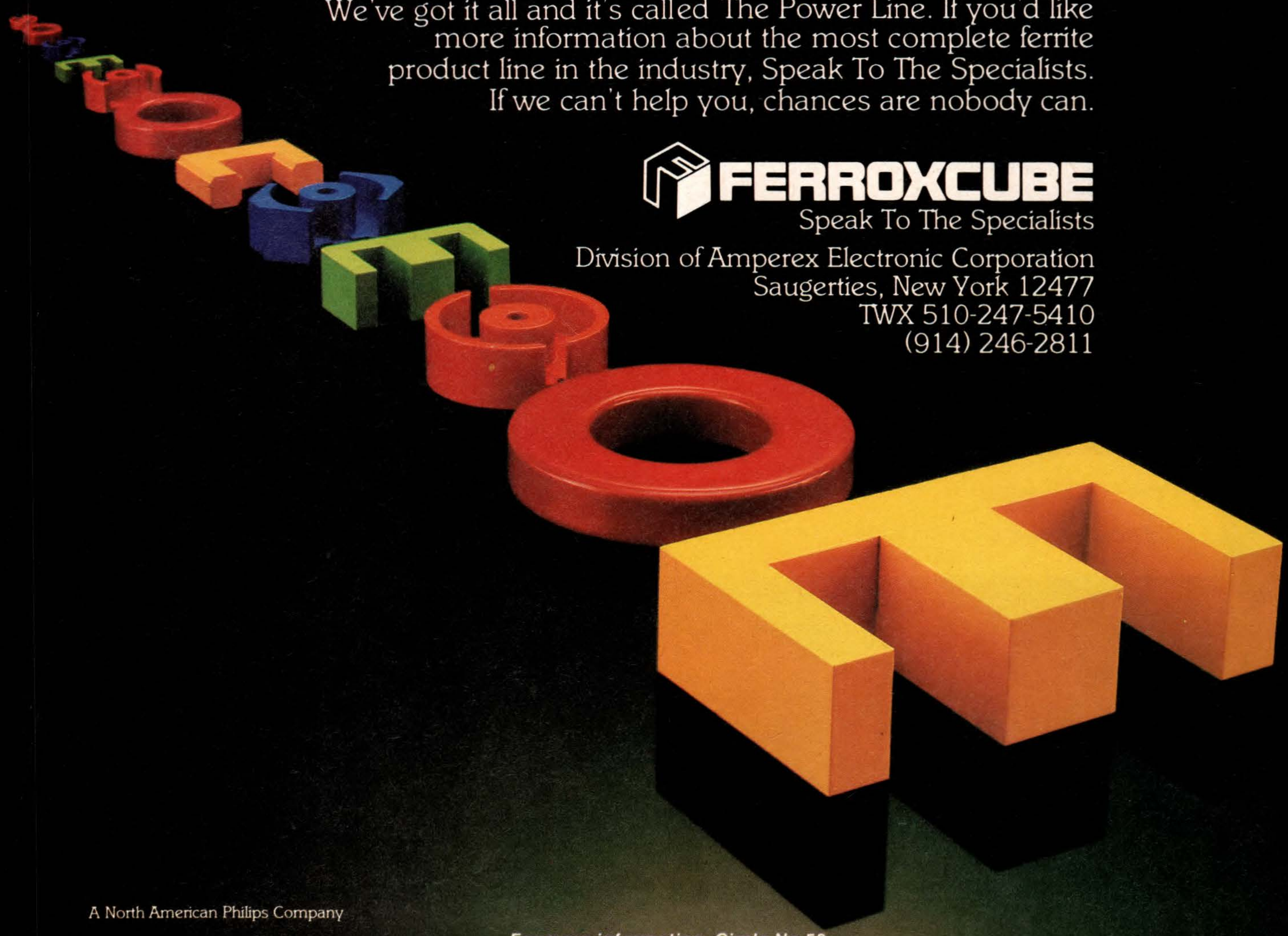

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Programmable array processors crunch numbers effortlessly

Special-purpose processors offer a low-cost alternative to expensive scientific computers for manipulating large data arrays.

Sam Martin, Floating Point Systems Inc

Programmable array processors find use in performing iterative computations on large data arrays because in such applications, mainframe computers cost too much and minicomputers possess restricted speeds. Interfaced to a general-purpose host computer, a dedicated array processor furnishes fast throughput, wide dynamic range and high precision—all under software control—to accommodate diverse data-array handling **(Fig 1)**.

The combination of an array processor and host CPU permits each machine to operate optimally on a computational problem. The host supplies overall system control, directing data flow and instructions between the array processor and the I/O devices. The array processor in turn executes complex data calculations more than 100 times faster than the host can.

Despite these outstanding advantages, though, many potential users avoid array processors because—at least on the surface—they appear extremely difficult to understand, utilize and program. But by grasping the basic array-processor hardware and software fundamentals, you can readily bring these versatile and flexible machines to bear on your intensive number-crunching applications.

Synchronous units rate over asynchronous types

Array processors are either synchronous or asynchronous machines. In a synchronous unit, all processing, memory and control elements adhere to the same clock cycle; in an asynchronous machine, various elements run at their own individual rates. In principle, an asynchronous machine possesses a throughput advantage because its inherently faster elements run unimpeded by its slower ones.

In practice, though, coordinating the operation of these asynchronous elements becomes complex; you must write a separate program to control each asynchronous function. Furthermore, the number of states in an asynchronous machine defies definition, making it difficult if not impossible to write a simulator for such a machine. Thus, you can only debug programs on the machine itself and therefore can't develop an application library in parallel with an asynchronous array processor's hardware development.

In contrast, synchronous array processors eliminate the need for programmer coordination of machine elements. Because you can write an exact simulator, program development gets a head start. Thus, the program libraries for synchronous array processors generally exceed those for asynchronous types.

Precision depends on bit format

A key factor underlying array-processor hardware centers on the achievable precision of calculations. In scientific computing, the required number of bits of accuracy depends on the application: Some uses call for the double precision (64 bits) commonly associated with large-scale scientific computers, while others need only 24 bits (six decimal digits). In the latter case, using either the entire data word (in an integer machine) or

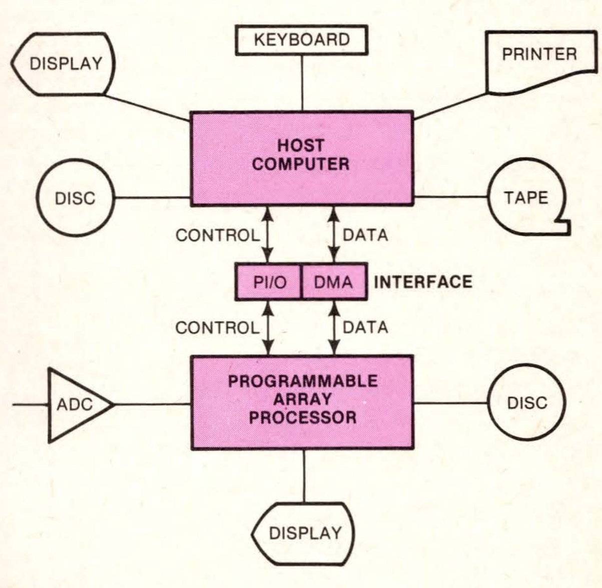


Fig 1—Combining a host computer with a programmable array processor *results in precise, fast, repetitive numerical calculations on large arrays of data. Bidirectional DMA transfers programs and data between the host and array processor, and programmed input/output (PI/O) enables the host to control the array processor.*

its mantissa portion (in a floating-point machine) provides the necessary precision.

Because scientific calculations in general span large dynamic ranges, floating-point array-processor architecture clearly wins over the integer configuration. In this respect, many common array processors adopt the standard 32-bit minicomputer word, usually divided into 24 bits for the mantissa and eight for the exponent. The result is a dynamic calculation range of $10^{\pm 38}$.

Obviously, this 32-bit hardware costs much less than a 64-bit double-precision configuration, but its 6-digit precision does lack adequacy for many applications. Therefore, a compromise solution of 38 bits employed in some array processors utilizes an extended-precision format. This approach divides the 38-bit word into a 28-bit mantissa and a 10-bit binary-encoded exponent to obtain 8-decimal-digit precision and a dynamic range of $10^{\pm 153}$—a marked performance improvement for a moderate increase in hardware complexity. And if full

Choosing an array processor

An array processor augments a host computer by providing the host with increased throughput and precision. But only if such an array processor offers at least a 38-bit data word (assuming a floating-point format) can it offer improved precision and dynamic range compared with a 32-bit minicomputer equipped with a floating-point-arithmetic option.

The degree of improvement in real working throughput by means of an array processor depends on whether the host computer, operating alone, is I/O bound or computation bound. If I/O operations consume the bulk of total processing time, with only a limited portion of that time spent on computation, an array processor won't help. On the other hand, it *will* speed throughput in cases where the bulk of the host's time involves iterative computations on large arrays of data. Such throughput improvements typically range from 10 to 200 times, depending on host speed, the characteristics of the chosen array processor and the application.

Array processors range in capability from 24-bit integer or block - floating - point machines to 38-bit extended - precision floating-point models with sophisticated architecture and software. In terms of flexibility, they encompass machines that are dedicated to a single host and provide no user programmability, as well as units that adapt to a variety of hosts and present a choice of programming modes. Prices range from \$7500 to nearly \$1 million; most processors cost less than \$50,000.

Under these circumstances, no one array processor suits all applications. The nearby checklist, however, will serve as a useful guide in choosing a processor suitable for your needs.

Before purchasing a specific array processor, run a benchmark test. Pick a problem typical of your most difficult or most common software program and request that potential vendors code and run the program on their array processors. Compare throughput, accuracy, cost/performance and other factors of particular importance to your application. You can also search the literature for benchmarks on problems similar to your own.

Key questions in array-processor evaluation

- ☐ Will an array processor help your application? Is your present (or potential) minicomputer computation bound or I/O bound?
- ☐ Will the contemplated array processor handle general scientific-computing applications or only a restricted subset such as signal processing?
- ☐ Is the array processor designed to operate with a variety of hosts or constrained only to one?
- ☐ Is the data format true floating point, block floating point or integer?
- ☐ Are precision and dynamic ranges adequate for the intended applications?
- ☐ Is the real working throughput adequate for the intended applications?
- ☐ Will the vendor perform a benchmark test for your application?
- ☐ Is the memory size adequate to handle anticipated problems? To what degree can it be extended?
- ☐ Is the memory access time fast enough to assure adequate throughput in anticipated applications?
- ☐ Do bottlenecks arise in the process of transferring data between memory and arithmetic units?
- ☐ Does the array processor offer direct high-speed I/O capability for applications in which the delay involved in interfacing through the host cannot be tolerated?
- ☐ Does the array processor offer real-time control capability?
- ☐ Does the array processor have a resident operating system for extended operation independent of the host?
- ☐ Can you write your own programs? How easy is the machine to program?
- ☐ How extensive is the processor's math library?
- ☐ How are programs debugged? Does an exact simulator exist?
- ☐ Is the price for a complete operating system low enough to allow dedicated (nontime-shared) use in your application?
- ☐ Does the quoted price include all options needed for your application, such as fast memory, real-time control, direct I/O and software?
- ☐ What is the processor's reliability rating (MTBF)?
- ☐ If yours is an OEM application, does the array processor meet your needs in terms of size, modularity, power consumption and supply voltages?
- ☐ Is the array processor easy to service?
- ☐ What support does the vendor offer?
- ☐ Is there a training program? Who pays for it?

Glossary of array-processor terms

This glossary assumes that you are familiar with basic computer terminology. Listed terms relate only to array processors and scientific computing or else present unique meanings in those contexts.

Array processor—A relatively low-cost computation machine that performs fast, precise and repetitive calculations on the large data arrays commonly associated with scientific calculations. This dedicated machine interfaces to a general-purpose host minicomputer or mainframe, which handles the necessary file manipulation and most I/O tasks. Generically, the term "array processor" refers to a processor capable of computations on large arrays of data and not to an array of processors, such as the Illiac IV.

Block floating point—A data format that normalizes all numbers in a set with respect to the same binary number. This format conserves memory hardware because only one common exponent must be stored for the entire set. However, block floating point loses precision in the smaller numbers of the set because of the large number of leading zeroes it introduces in those numbers.

Hardware pipelining—A technique that enhances a multistage ALU's throughput by flow-streaming calculations.

Megaflops — A throughput measurement of an array processor's floating-point ALU; equivalent to one million floating-point operations per second.

Mips—A measure of a computer's execution rate; equal to one million instructions per second. This measurement encompasses all machine operations (such as data fetches, address calculations, stores and I/O operations), not just floating-point-arithmetic operation.

Multiprocessor—A machine that consists of more than one processor (eg, an array of processors such as Illiac IV).

Parallel-processing hardware—Hardware elements that operate simultaneously to increase throughput. These elements need not be entire processors, but they do encompass such items as multiple floating-point-arithmetic units, multiple memory units, separate control arithmetic units and multiple data paths connecting the various elements. In many popular array processors, a separate command field in the instruction word controls each element.

Parallel processor—A computation system that performs more than one arithmetic operation simultaneously.

Potential throughput — The maximum rate at which an array processor (or other scientific computer) completes basic floating-point calculations. For a synchronous machine, this rate equals the product of the machine's clock rate and the total number of results produced by the floating-point-arithmetic units during each clock cycle.

Real application throughput—The rate at which an array processor (or other scientific computer) performs calculations in a given application. The degree to which this rate falls below the potential throughput depends on the application, the array-processor design and the software program's efficiency.

Software pipelining—A programming concept that resembles the throughput technique of hardware pipelining. It structures parallel command fields in the machine's instruction word; when an instruction loop performs iterations of the same calculation on a large data array, software pipelining permits closing the loop around a reduced set of instructions after the "pipe" is filled.

Uniprocessor — A processor that fetches an instruction word from a single memory and executes the instruction during a single machine cycle.

double precision becomes mandatory in applications involving such hardware, you can derive the necessary software routines in short order.

Between the integer and various floating-point approaches in terms of complexity lies a third format: block floating point. This approach normalizes the data words in a set with respect to a single binary number and assigns a common exponent to the set. Only when calculations cause an overflow are set renormalization and exponent changes required. The advantage? Cost savings result from the use of only one set of exponent hardware as opposed to including the exponent in each memory word.

However, employing a common binary normalization point leaves some numbers in the set with so many leading zeros that their precision deteriorates beyond usefulness. In fact, this lack of precision contaminates other data after repeated calculations. Block-floating-point architecture thus achieves accuracy if you are certain that all the numbers involved lie within a small dynamic range. But in that case, you'd be better off utilizing an inexpensive integer machine.

Parallel hardware promotes high throughput

Whatever its overall hardware configuration, an array processor minimizes hardware idle time by means of careful determination of the numbers and types of parallel elements and provision of multiple parallel data paths (**Fig 2**). Why the need for such parallel paths? A computer system performs multiple operations during each machine cycle: It locates and interprets an instruction, finds and transfers data to the central processor, performs arithmetic operations, stores intermediate results, returns the final results to

Multiple parallel data structures provide high processing speed

memory and controls I/O functions. If only one data bus exists, each of these functions occurs in sequence, thus limiting overall processing speed. Multiple parallel data paths, though, coupled with a subdivided 64-bit instruction word (**Fig 3**), allow up to 10 functions (such as data fetch, program index, add, multiply, data store and I/O) to take place simultaneously.

Consider the specific cases of multiplication and addition. By employing separate adder and multiplier hardware, an array processor can perform these two floating-point operations simultaneously. For while complete floating-point additions require two clock cycles and floating-point multiplications need three, pipelining the hardware elements permits one floating-point - addition operation and one floating - point-multiplication task to occur during each clock cycle.

For example, examine the floating-point multiplication cycle. Its three steps are (a) begin product of fractions, (b) add exponents and complete product of fractions and (c) normalize and round result. Without pipelining, the hardware idles for two of these three steps; with pipelining (**Fig 4**), it remains virtually active at all times. Specifically, during clock cycle 1, step 1 of the first multiplication completes, and its results move to the step 2 hardware. During clock cycle 2, a second multiplication begins in the step 1 hardware simultaneously with step 2 of the first multiplication. A third multiplication starts in the step 1 hardware during the third cycle; multiplication 1 moves to the step 3 hardware, and multiplication 2 moves to the step 2 hardware. After cycle 3, a result emerges at the end of each cycle.

The throughput advantages of such an approach are obvious. An array processor's clock usually runs at 4 or 6 MHz, depending on the logic family employed. A 6-MHz rate translates to a 12M-operations/sec computational throughput because of the simultaneous nature of the floating-point additions and multiplications. And that's for only two parallel operations. Because up to 10 functions can execute simultaneously, you can program an array processor to perform up to 60M operations/sec.

Performance demands high-speed memory access

This throughput improvement in turn calls for fast memory access, because fast floating-point-arithmetic units require high-speed delivery of arguments from memory and fast channeling of results back to memory. For example, in the architecture depicted in **Fig 2**, four arguments execute during each cycle—two for the adder and two for the multiplier. At a 6-MHz clock rate, a 24M-word/sec data-transfer rate supports the inputs to the floating-point-arithmetic units. Because the adder and multiplier operate simultaneously, another 12M-words/sec operation transfers the results back to

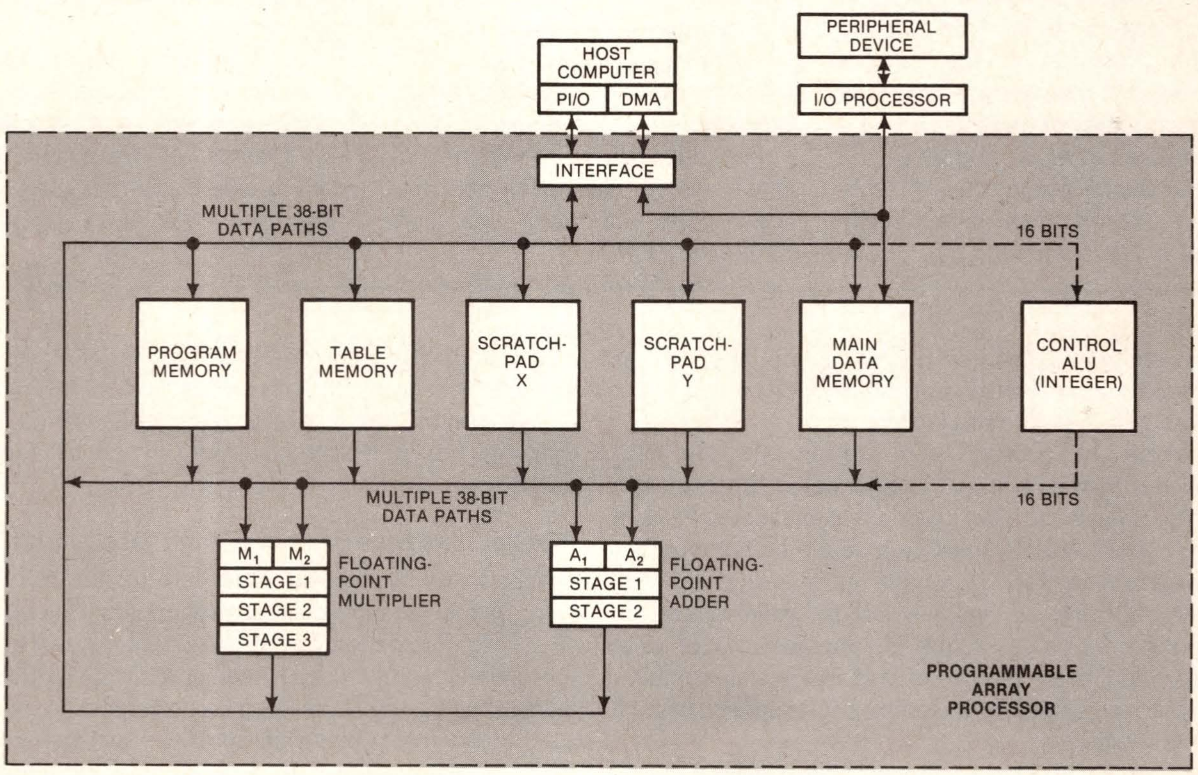


Fig 2—An array processor's high throughput *stems primarily from parallel arithmetic devices, memories and data paths. You can time-overlap all processor operations to achieve execution speeds consistent with scientific computations.*

memory. Thus, the array processor requires a minimum 36M-word/sec memory-transfer rate—without considering such management activities as program-memory transfers. (Because each 38-bit word equals 4.75 bytes, this rate corresponds to a 171M-bytes/sec transfer rate.)

If 10M words/sec represents a substantial memory-transfer rate, 36M words/sec signifies an intensive design effort. However, array-processor designers solve this problem by providing separate memories for data, programs and control, avoiding memory-access conflicts, providing multiple parallel data buses between memory and arithmetic elements and avoiding bus conflicts.

A further technique for speeding memory access provides two scratchpads, each containing 32 high-speed accumulators. These scratchpads function like cache memories in a minicomputer, supplying two arguments and storing two intermediate results during each machine cycle. The design restricts the number of parallel floating-point-arithmetic units to two in order to avoid compounding the memory-access problem, but it still allows very high throughput.

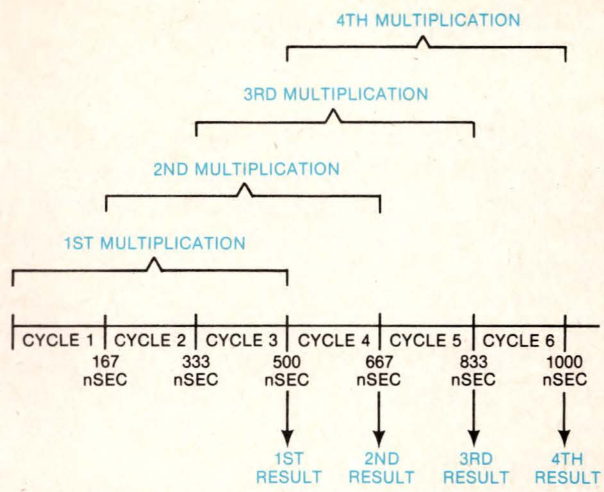


Fig 4—Hardware pipelining *achieves a factor-of-three increase in throughput for sequential floating-point multiplications by means of time-step overlapping.*

Software considerations involve three approaches

The foregoing hardware considerations represent only half of the array-processor story. The other half—software—focuses on programming ease, efficient coding and the number of available debugged subroutines covering standard mathematical operations. In general, a tradeoff exists between the first two factors: Higher level languages provide greater programming ease, but such compilers rarely achieve the coding efficiency possible by programming in the machine's assembly language.

For some less critical applications, though, quickly developed programs are more important than realizing maximum throughput. In others, a need for maximum throughput readily justifies the expenditure of time and effort necessary to obtain tightly coded programs. Thus, the availability of several programming options is desirable.

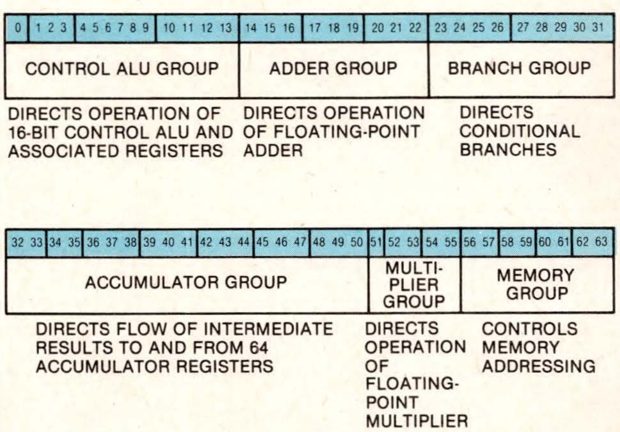


Fig 3—A 64-bit instruction word *permits up to 10 simultaneous control, memory and arithmetic operations. In conjunction with a 6-MHz clock, this instruction word directs up to 60M operations/sec, thereby ensuring that the floating-point units' throughput potential of 12 megaflops is realized.*

The array processor depicted in **Fig 2** provides three programming alternatives, listed in order ranging from the easiest to implement to the most efficient to code:

- Program in FORTRAN and use a host-resident FORTRAN compiler for conversion to the array processor's assembly language.
- Use a series of FORTRAN calls issued by the host.
- Program directly in the array processor's assembly language.

Using the first alternative's FORTRAN compiler requires a knowledge of conventional FORTRAN programming. This compiler automatically converts to FORTRAN statements all aspects of the array processor's assembly language; it also implements transformation from the straight-line coding (one instruction per line) of conventional FORTRAN programs to the parallel coding appropriate for the array processor's subdivided instruction word. Coding efficiency varies with the application but is high enough for you to employ this alternative for all but the most throughput-critical and/or frequently used programs.

The second programming alternative offers ease of use, but its software programs execute slowly because the host and array processor must communicate on each call. For example, a simple program needed to perform a complex fast Fourier transform (FFT) includes:

CALL APINIT	Initialize array processor
CALL APPUT (a_1---a_n)	Transfer data from host to array processor
CALL CFFT (a_1---a_n)	Perform complex FFT
CALL APGET (a_1---a_n)	Transfer results from array processor to host.

Where maximum possible throughput is required, the third alternative—programming directly in the array processor's assembly language—provides the

Software tradeoffs involve coding ease and efficiency

best application choice. This selection, of course, requires mastery of the language. However, experience shows that you can learn the basics of such assembly language in a few hours and attain reasonable proficiency in a few days.

Programming an array processor in assembly language achieves the coding-efficiency advantages usually associated with a program written in assembly language. Additionally, this hand coding typically results in more efficient use of the subdivided instruction word.

Both the FORTRAN and assembly-language programming approaches offer application simplicity and efficiency in cases where you have access to an extensive library of tightly coded, thoroughly debugged subroutines for standard mathematical functions. Such functions include real and complex vector operations, vector maximum/minimum and filtering tasks, matrix operations, FFTs and signal processing.

Software pipelining reduces loop time

Beyond the three basic programming alternatives, an array-processor consideration concerning both hardware *and* software centers on the means whereby a processor's subdivided instruction word permits a code-compression format termed software pipelining. This format overlaps (in time) the instructions for repetitive operations—just like the floating-point adder and multiplier hardware-pipelining technique.

You can more easily grasp the nature of software pipelining by tracing through a program example demonstrating the code compression made possible by the array processor's combined hardware and software parallelism. Begin by noting the following instruction definitions:

- NOP—No operation (allows time to complete a multicycle operation)
- FETCH A—Fetch operand A from memory
- FMUL A,B—Perform floating-point multiplication of A and B
- FADD A,B—Perform floating-point addition of A and B
- SAVEX A—Save operand or intermediate result in scratchpad X
- SAVEY A—Save operand or intermediate result in scratchpad Y
- STORE C—Store result C in memory
- DEC N—Decrement loop counter
- BGT LOOP—Branch to LOOP if loop count (N) is greater than zero; continue to next statement if N is equal to or less than zero.

When instructions FMUL and FADD lack operands,

TABLE 1 — ASSEMBLY-LANGUAGE PROGRAM FOR $C_i = A_i^2 + B_i^2$

LOOP:	FETCH A_i	FETCH A_i
	NOP	
	NOP	
	SAVEX A_i	
	FETCH B_i	FETCH B_i
	NOP	
	NOP	
	SAVEY B_i	
	FMUL A_i, A_i	FORM A_i^2
	FMUL	
	FMUL	
	SAVEX A_i^2	
	FMUL B_i, B_i	FORM B_i^2
	FMUL	
	FMUL	
	SAVEY B_i^2	
	FADD A_i^2, B_i^2	FORM $C_i = A_i^2 + B_i^2$
	FADD	
	STORE C_i	
	DEC N	DECREMENT LOOP COUNT
	BGT LOOP	AND BRANCH IF COUNT >0
DONE:	RETURN	EXIT WHEN COUNT = 0

TABLE 2 — SHORTER PROGRAM WITH HARDWARE AND SOFTWARE PARALLELISM

	FETCH PHASE	MULTIPLICATION PHASE	ADDITION PHASE
LOOP:	FETCH A_i		
	FETCH B_i		
	NOP		
	SAVEX A_i		
		FMUL A_i, A_i; SAVEY B_i	
		FMUL B_i, B_i	
		FMUL	
		FMUL; SAVEY A_i^2	
			FADD B_i^2, A_i^2
			FADD
			DEC N
			STORE C_i; BGT LOOP
DONE:	RETURN		

TABLE 3 — MINIMUM EXECUTION TIME WITH SOFTWARE PIPELINING

	FETCH PHASE	MULTIPLICATION PHASE	ADDITION PHASE
	FETCH A_1		
	FETCH B_1		
	NOP		
	SAVEX A_1		
	FETCH A_2;	FMUL A_1, A_i; SAVEY B_1	
	FETCH B_2;	FMUL B_1, B_1	
	NOP;	FMUL	
	SAVEX A_2;	FMUL; SAVEY A_1^2	
LOOP:	FETCH A_i;	FMUL A_{i-1}, A_{i-1}; SAVEY B_{i-1};	FADD B_{i-2}^2, A_{i-2}^2
	FETCH B_i;	FMUL B_{i-1}, B_{i-1};	FADD
	NOP;	FMUL;	DEC N
	SAVEX A_i;	FMUL; SAVEY A_{i-1}^2 ;	STORE C_{i-2}; BGT LOOP
DONE:	RETURN		

they execute simple multiplication and addition push instructions, respectively, to complete arithmetic operations requiring multiple clock cycles.

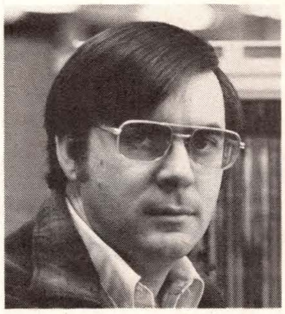
To perform the repetitive calculation $C_i=A_i^2+B_i^2$ (i=1 to N), the conventional straight-line-coded program shown in **Table 1** calls for 21 instructions. For a 6-MHz machine clock (167 nsec/cycle), each of the N iterations executes in 3.5 μsec. Taking advantage of the array processor's hardware parallelism and pipelined arithmetic units (as well as the machine's instruction-word parallelism) permits reducing the loop's program to 12 instructions (**Table 2**) and the execution time to 2 μsec for each iteration.

Thus far, hardware and software parallelism applies to only one of the N iterations at a time. Software pipelining, however, substantially compresses the loop's execution time by overlapping the N iterations (**Table 3**). Observe that the second calculation ($C_2=A_2^2+B_2^2$) starts without waiting for completion of the first ($C_1=A_1^2+B_1^2$). This time-compressed program still requires 12 instructions, but the first eight simply fill the "software pipe." After the pipe is filled, the loop closes around only the last four instructions to perform iterative calculations.

The offset organization of the three blocks of instructions in **Table 2** facilitates comparison with the corresponding blocks in **Table 3**. For the **Table 3** program, execution time further reduces to 668 nsec/iteration, compared with the 3.5-μsec iteration of the straight-line-coded program. Thus, throughput increases 5.25 times without a corresponding increase in hardware speed. **EDN**

Author's biography

Sam Martin serves as educational-services manager for Floating Point Systems Inc, Beaverton, OR. In this post, he supervises and teaches hardware and software courses concerning programmable array processors. Sam earned a BSEL at California State Polytechnic University.



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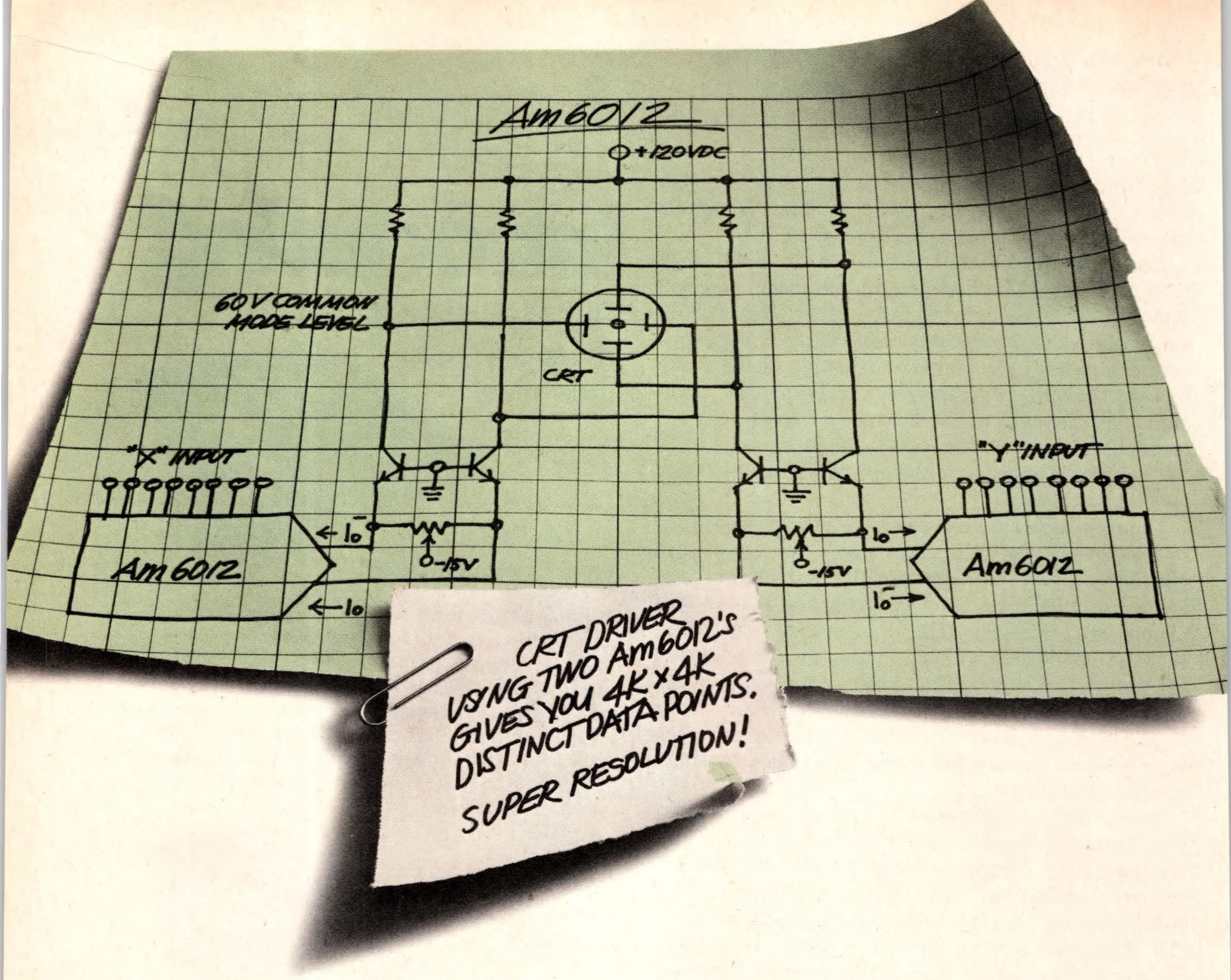

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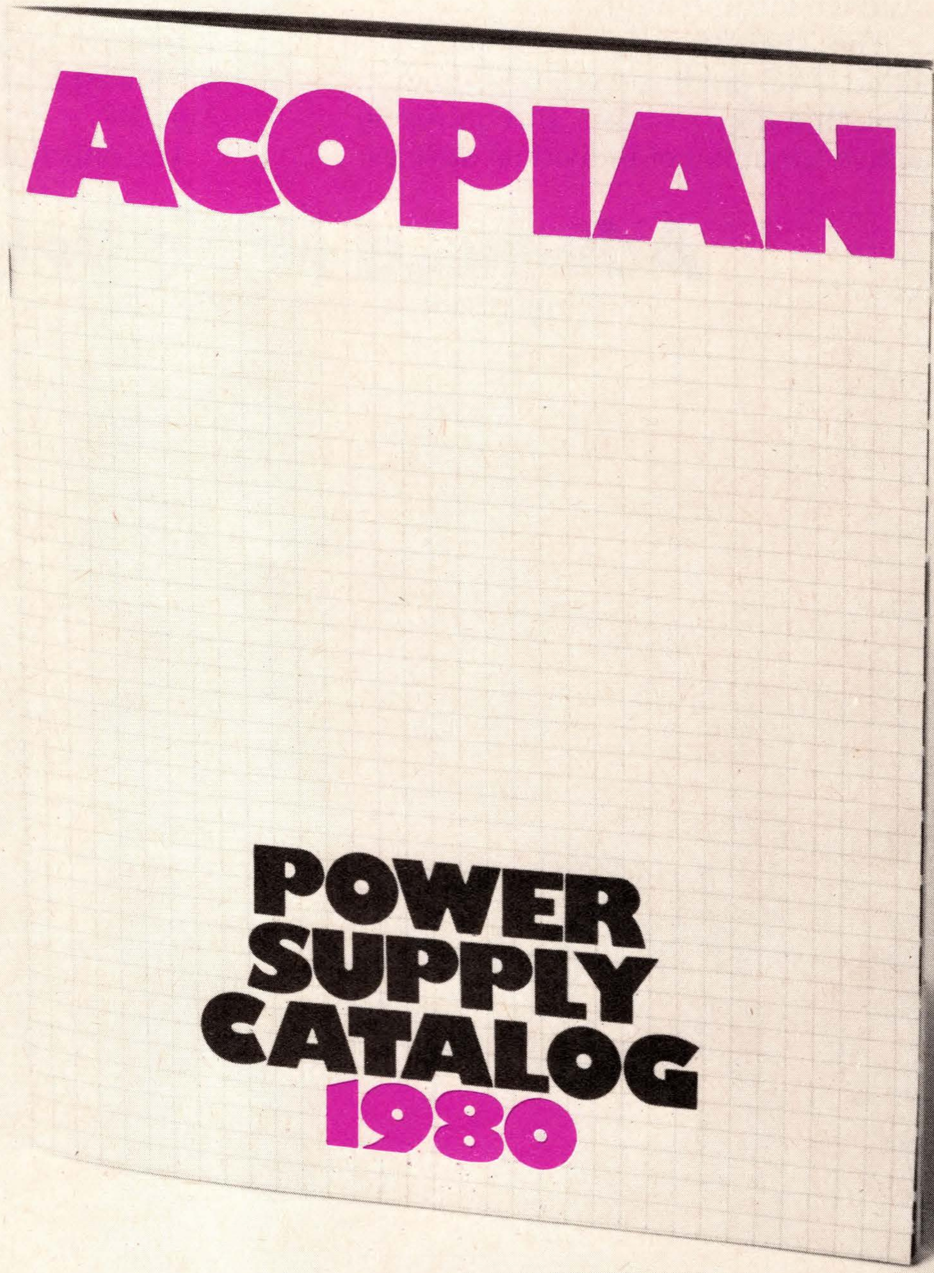

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Dynamic power-factor correction cuts switcher input-current drain

Excessive peak input current often limits the power-supply capacity that a standard 15A ac circuit can handle. But correcting a supply's PF to near unity lets you raise the allowable rating.

Derek Chambers and **Dee Wang,** Sorensen Co

You can use a modified flyback circuit to increase an off-line switching power supply's power factor (PF) from its typical value of 0.65 to near unity. The resulting improvement can prove especially important when you must power loads greater than 500W from conventional wall outlets.

Improving PF allows delivery of more useful power to a load without increasing rms input current. Operating with a near-unity power factor also reduces the peak current drawn from the line, causes less line drop, lowers cable losses and makes the overall installation less expensive.

As an example, consider a 1000W load connected to an off-line converter operating at 70% efficiency. With 115V input, line current equals approximately 19A at a PF of 0.65 but decreases to 13A if PF is 0.95. A standard 15A wall outlet can operate the converter in this latter case, but special circuits are required to furnish the necessary extra current when the PF is 0.65.

Why is PF so low?

Basically, the poor PF of conventional off-line capacitor-input supplies stems from input-current wave shape: Current is drawn from the line in relatively narrow pulses occurring at the peaks of the line waveform.

Fig 1 depicts a typical input circuit; in this circuit, large storage capacitors C_2 and C_3 (~1000 μF each) charge through the bridge rectifier and thermistors RT_1 and RT_2. If the impedance of the power-line, rectifier, thermistor and capacitor elements is low, the repetitive peak line current into the supply can be excessively high, causing high rms input current and

This article is based on a paper presented at POWERCON 6, the Sixth National Solid-State Power Conversion Conference, Miami Beach, FL, May 2-4, 1979.

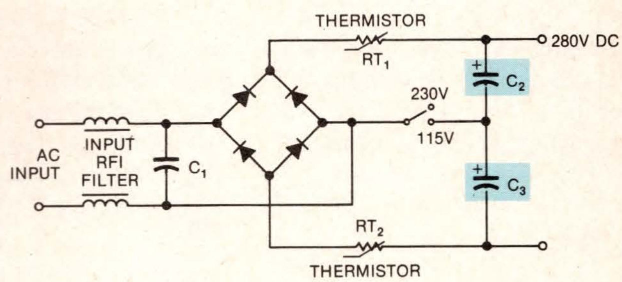


Fig 1—A typical off-line switcher input *charges large storage capacitors C_2 and C_3, which provide the dc to be chopped at a high frequency.*

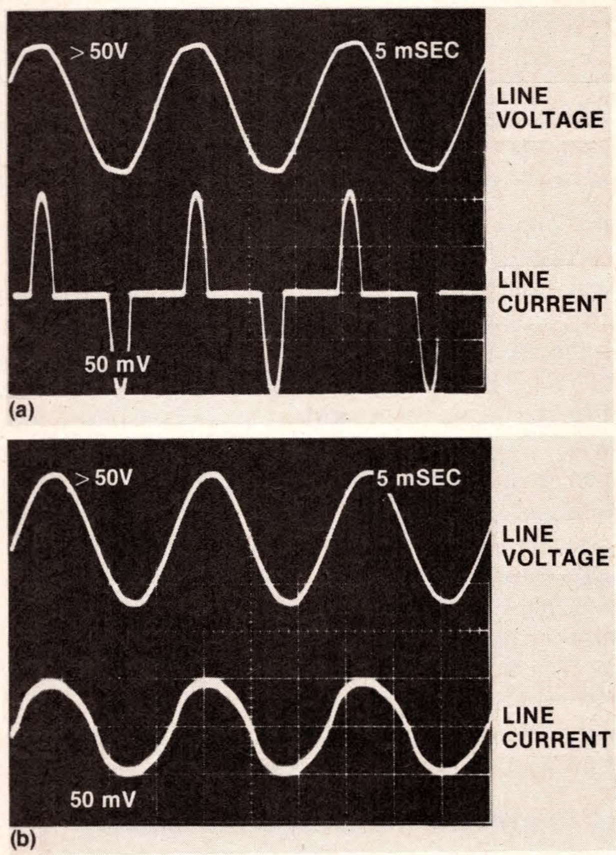


Fig 2—Input line voltage and current waveforms *differ dramatically without* **(a)** *and with* **(b)** *dynamic power-factor correction.*

PF correction changes pulsed line-current inputs to sine waves

low power factor. In most practical applications, the input circuitry contains sufficient series resistance to limit the repetitive peak current into a supply to a value between two and three times what would flow in a purely resistive circuit.

Achieving a high PF requires a new approach

Because the poor PF of conventional off-line supplies results mainly from the pulsed current waveform they draw, any improvement must correct this condition; it must spread out the power drain over the entire cycle and make the input current both sinusoidal and in phase with the voltage. Essentially, the current wave shape must approach that of a resistive load. **Fig 2** shows the relationship between input voltage and current for a typical off-line converter, with and without such dynamic power-factor correction. (Note the obvious visual improvement in current wave shape after correction.)

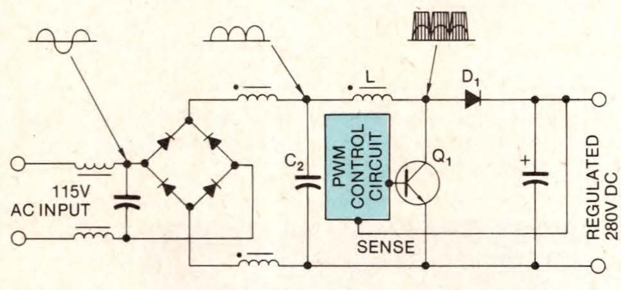


Fig 3—In this simplified power-factor-correction circuit, *note that the waveform to be chopped is not dc—rather, it's essentially an unfiltered full-wave-rectifier output.*

Achieving dynamic power-factor correction involves adapting the well-known flyback (up-chopper) circuit to chop the rectified line current at a high frequency—20 or 40 kHz. The basic system, shown in simplified form in **Fig 3,** takes the rectified *but unsmoothed* line voltage, chops it and applies the resulting high-frequency pulses to a flyback inductor (L).

Note that C_2, the capacitor preceding this choke, does not produce dc to be chopped. Instead, it provides only enough energy storage to supply the high-frequency current pulses into the flyback inductor. Furthermore, C_2 also smooths out these flyback-current pulses and helps prevent noise from feeding back into the line. It's this concept of chopping a rectified line voltage, rather than the use of dc stored in large electrolytic capacitors, that makes possible the PF improvement.

Details show how to implement the concept

In **Fig 3**'s circuit, power transistor Q_1 operates at the switching frequency, and base-drive pulse width is held constant during a line cycle. Thus, the peak current at

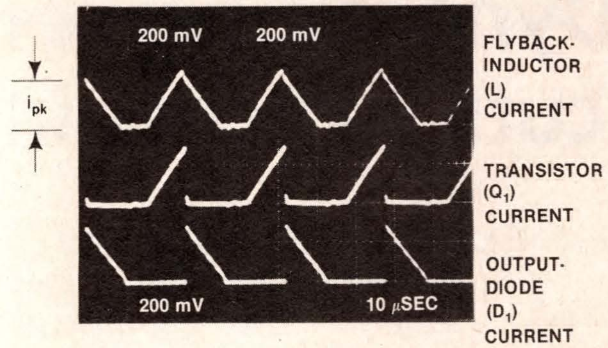


Fig 4—These typical current waveforms *in a PF-corrected circuit were captured near the peak of a rectified line-voltage excursion.*

the end of each chopping pulse varies directly with the full-wave-rectified line voltage applied to the flyback inductor. As in a conventional flyback circuit, energy is first stored in the inductor during the transistor ON time, then released through the output rectifier to the output load and smoothing capacitor during transistor turn-off.

Applying feedback sensing from the output to control the transistor's base-drive pulse duration achieves regulation of the dc output voltage against line and load changes. A large time constant for the feedback control helps satisfy the requirement for essentially constant chopper pulse width over a line cycle.

Fig 4 illustrates typical flyback-current waveforms through the circuit's inductor (L), transistor (Q_1) and output diode (D_1), captured near the peak of the rectified line voltage. Similar waveforms apply near the line-voltage trough, except that the current rise is slower and the output rectifier's flyback-current time decreases. The energy transferred to the output load during each flyback pulse is $\frac{1}{2}Li_{pk}^2$ joules, where i_{pk} is the peak value of the current at the instant of turn-off.

Peak flyback current in the inductor directly relates to the applied voltage from the line, assuming constant

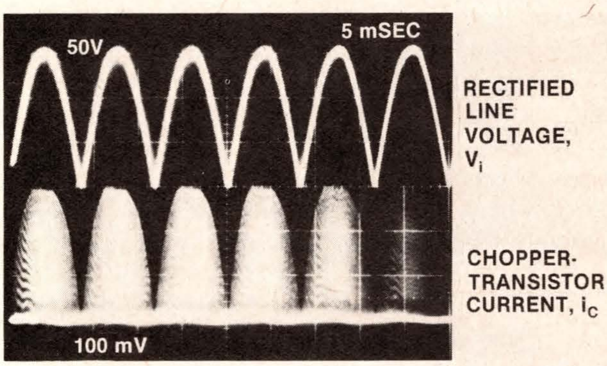


Fig 5—The modulated envelope of chopper-transistor current *faithfully follows the rectified line-voltage wave shape.*

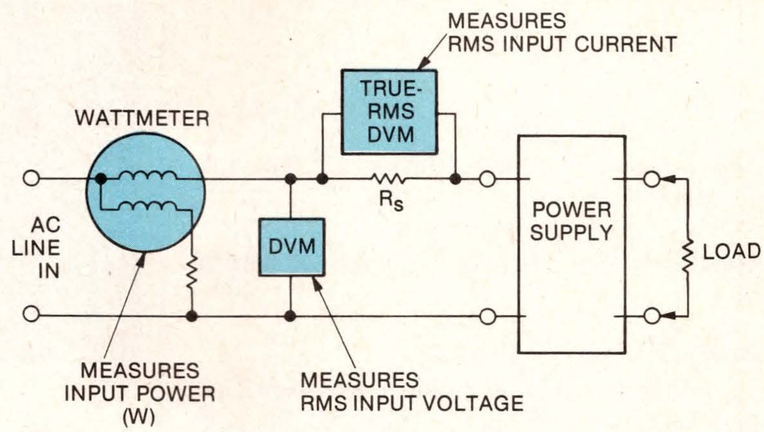
Measuring power factor

Power factor is the ratio of input power (measured in watts) to the product of rms voltage and current. Measuring the values necessary for this calculation can require some care.

Determining a supply's rms input voltage poses few problems, because the input waveform is usually sinusoidal and can be accurately indicated by a conventional ac voltmeter.

Current measurement, however, can pose problems. The preferred method of measuring current (see **figure**) employs a true-rms DVM to read the voltage drop across a calibrated low-resistance current shunt placed in series with the input line.

The familiar concept of defining power factor by means of the phase angle between voltage and current doesn't apply to switching supplies because their input-current waveforms are far from sinusoidal. For this same reason, connecting capacitors across the line doesn't improve switcher PF.



Power-factor measurement *requires relatively simple instrumentation.*

width of the chopper-transistor drive pulses during a line cycle. Therefore, input-current draw occurs all up and down the slopes of the rectified input-voltage waveform applied to the inductor, and its magnitude is proportional to the line voltage. **Fig 5** depicts this relationship; note particularly that the modulated current envelope closely follows the rectified line-voltage waveform and that current is drawn throughout the line cycle—satisfying the conditions necessary for producing a high PF.

Values for the required inductance and the resulting peak current for a particular output power are readily calculated. Peak current is a function of the instantaneous value of the full-wave-rectified line voltage (V_i) and

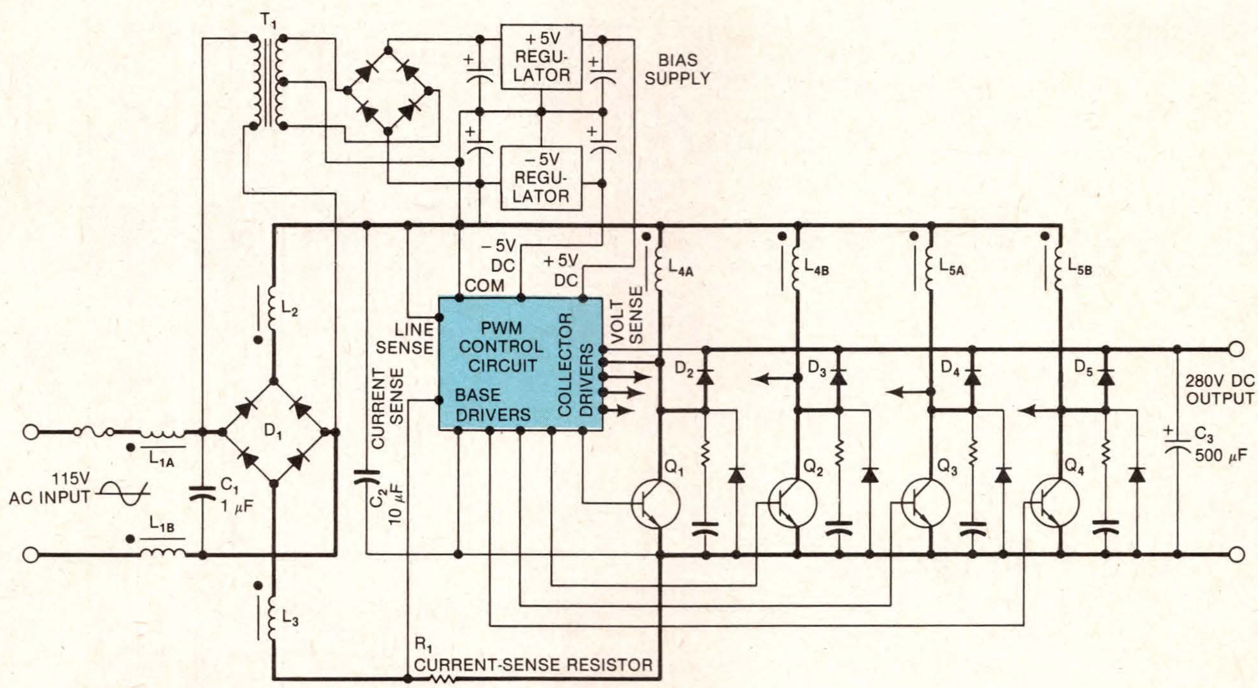


Fig 6—Main current-flow paths (bold lines) *help illustrate the nature of the power-factor-correction scheme.*

has magnitude

$$i_{pk}=V_i t/L$$

where t equals chopper ON time. Power available at the system output then becomes

$$P=\tfrac{1}{2}L(i_{pk}/\sqrt{2})^2 f \text{ watts}$$

where f represents the chopping frequency (40 kHz in this case).

A practical 800W high-PF example

In a design illustrating the foregoing PF-correction technique (**Fig 6**), the main current-flow path appears in bold lines. Four power transistors are driven in parallel; their choke outputs add through individual output rectifiers to feed the 500-μF smoothing capacitor and load. Input filtering comes from L_1, L_2, L_3, C_1 and C_2. The latter, a 10-μF unit, provides sufficient capacitance to handle the switching-choke currents and prevent noise from feeding back into the line. (As noted, it has a very minor smoothing effect on the full-wave-rectified line voltage chopped at 40 kHz.)

Voltage sensing, taken from the output dc bus, feeds input to the circuit controlling the pulse width at the base of each chopper transistor, providing regulation against both line and load variations. Under normal conditions, the voltage feedback handles regulation, but to control and limit the pulse width when excessive peak currents occur, the drop across current-sensing resistor R_1 furnishes a second control input. Under current-limit conditions, the current signal is compared

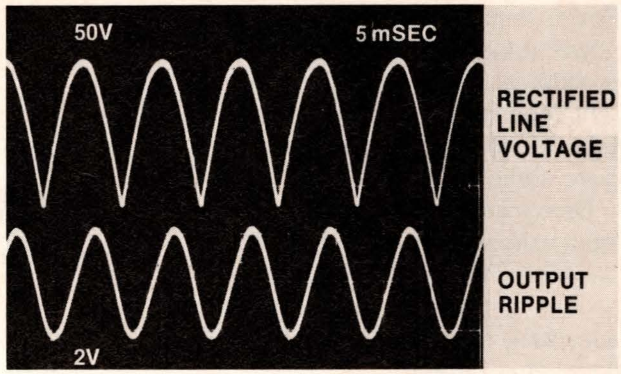


Fig 8—Out-of-phase relationship *between ripple on the dc output of the PF-correction circuit and the rectified line voltage mandates cancellation of the feedback signal's ripple component.*

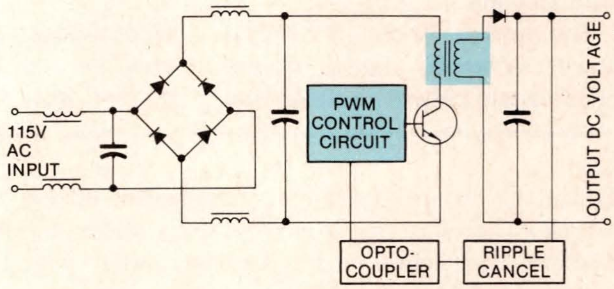


Fig 9—Adding a secondary winding *on the flyback choke provides isolation along with any desired output voltage.*

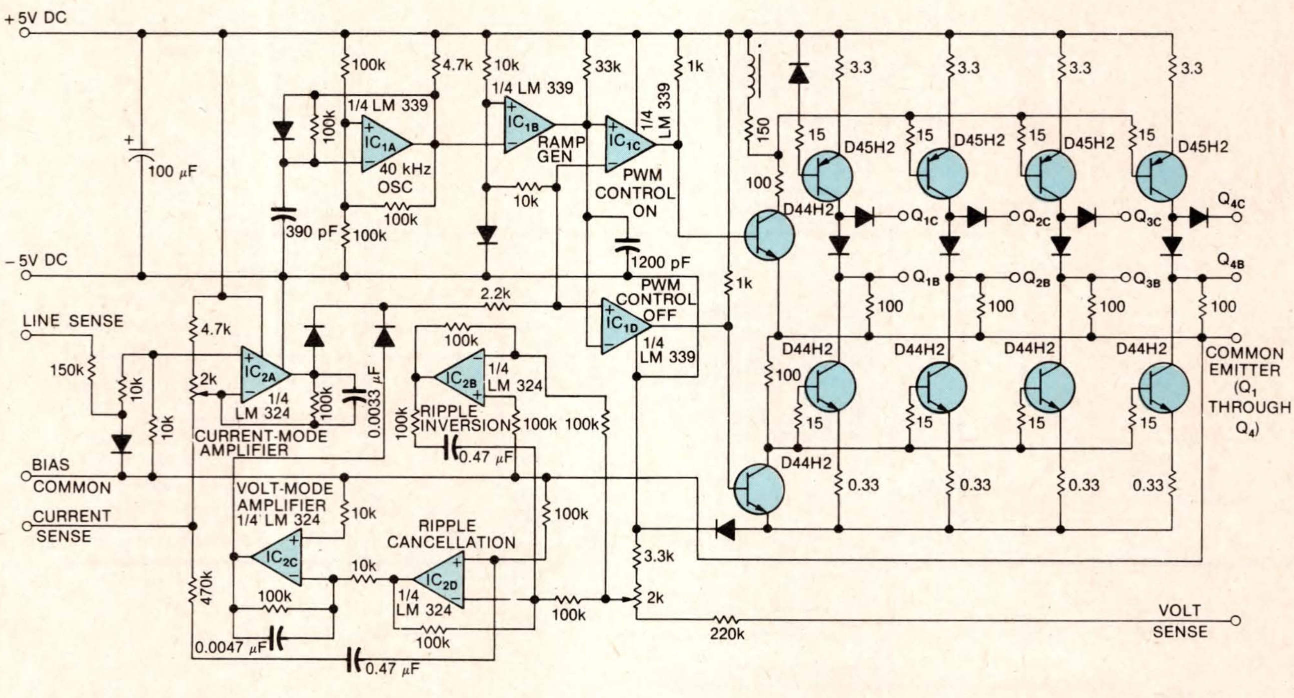


Fig 7—Details of the PWM control circuit *(block in* ***Fig 6****) reveal its relative simplicity.*

with the clamped input voltage and used to keep voltage and current in phase and to maintain a high PF.

Control and base-drive elements of the 800W system, shown as the PWM Control Circuit block in **Fig 6,** are detailed in **Fig 7.** The control circuits, employing a quad comparator IC (top left) are conventional. This comparator serves as a 40-kHz oscillator, ramp generator and pulse-width modulator.

Modulator outputs IC_{1C} and IC_{1D} supply a multiple-output driver section that feeds Q_1 through Q_4 of **Fig 6.** (Each of these 2N6547s handles up to 200W, so four are needed for the 800W load.) For normal control, a sample of the output voltage is compared with the −5V reference, and IC_{2C} amplifies the sample's dc component for application as the pulse-width modulator's control signal.

Ripple on the system's dc output (hence on the Volt Sense input) must be removed because it's not in phase with the rectified line voltage **(Fig 8).** (If allowed to remain, it would introduce a phase shift in input current relative to the line-voltage waveform, which would degrade the supply's PF.) The necessary ripple cancellation results from inverting the feedback voltage

OFF-LINE-CONVERTER INPUT-POWER MEASUREMENTS

WITHOUT PF CORRECTION	POWER LEVEL							
INPUT CURRENT (A RMS)	1.56	2.86	4.18	5.38	6.60	7.82	9.00	10.2
VOLT-AMPERES	178.2	331.6	485.1	624	764.7	905.3	1039	1174
INPUT WATTS	100	200	300	400	500	600	700	800
PF (W/VA)	0.561	0.603	0.618	0.641	0.653	0.662	0.672	0.681
WITH PF CORRECTION								
INPUT CURRENT (A RMS)	1.24	2.18	3.22	4.16	5.16	6.16	7.18	8.22
VOLT-AMPERES	141.5	252.5	372.3	482.1	596.9	711.3	828.5	947.6
INPUT WATTS	130	238	353	460	570	679	790	901
PF (W/VA)	0.918	0.942	0.948	0.954	0.955	0.955	0.954	0.951

in IC_{2B} and summing the ac component with the original signal in IC_{2D}. Should excessive line current occur, the output of IC_{2A} goes HIGH and overrides the voltage mode, narrowing the drive pulses in the output transistors.

The nearby **table** illustrates the 800W supply's operation both with and without dynamic power-factor correction. In both cases, PF increases somewhat as the load increases—a feature attributable to current being drawn over a larger portion of the power-line cycle. Additionally, note that although the line input current decreases greatly with PF correction, the total input power increases somewhat because of correction-circuit power consumption.

Want different output voltages?

Because the PF-correcting scheme just outlined is based upon a flyback circuit, the dc output voltage always exceeds the peak input-voltage value. Thus, with a 115V input, the system normally delivers a 250 to 325V dc output, corresponding to the input-voltage requirements of off-line converters intended for 115/230V operation.

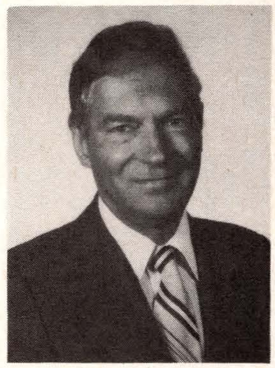
Adding secondary windings to the switching inductor (which now becomes a transformer; see **Fig 9**) can produce almost any desired output voltage of either polarity. These secondary voltages are isolated from the primary circuit, allowing the output voltages to float.

With isolation accomplished and any desired output voltage easy to achieve, the PF-correction circuit becomes a complete off-line switching supply. Feedback for voltage regulation still comes from the output but now requires an added optoisolator.

Look at the drawbacks

This PF-correction system can prove valuable when high PF is your prime consideration. Its major handicaps stem from the requirement for ripple cancellation in the feedback loop—this need lengthens response time and restricts usable loop gain. Thus, regulation, ripple and response time tend to be inferior to those of more conventional off-line switchers. And efficiency drops because of the power consumed by the added circuits. However, the method's reduction in peak load current suits it for high-power applications where fuse rating, wire size or peak demand current are the limiting factors. **EDN**

Authors' biographies



Derek Chambers, engineering manager (power supplies) at the Sorensen Co, Manchester, NH, when this article was written, was an employee of Sorensen's parent, Raytheon Co, for 16 yrs. He holds a BSC degree in electrical engineering from the University of Leeds, England, has been granted 12 patents and is a member of the IEE of Great Britain. Derek currently works for Exxon Enterprises, Florham Park, NJ.

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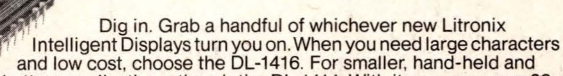

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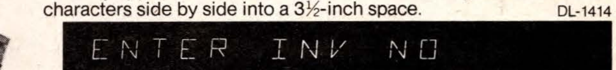

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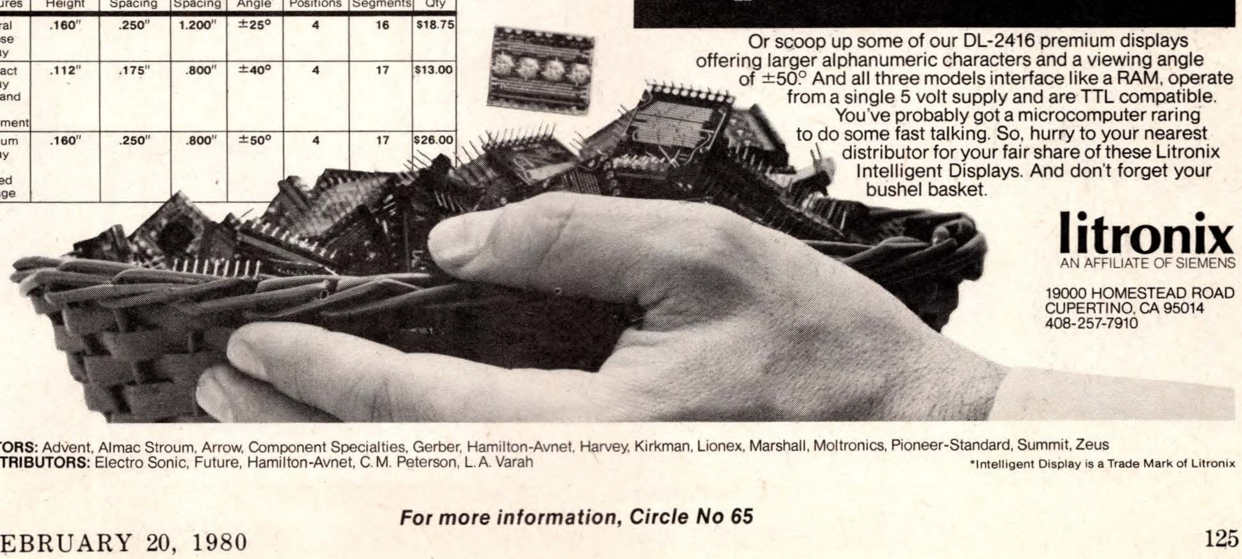

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The MC68000 — A 32-bit μP masquerading as a 16-bit device

The latest entry in the 16-bit-μP market sports 32-bit registers and an instruction set that facilitates the compilation and execution of block-structured languages such as PASCAL.

Robert Grappel*, Consultant,
and **Jack Hemenway,** Consulting Editor

In the previous two installments of this series (EDN, November 20, 1979, pg 185 and January 20, pg 119), we examined the Zilog Z8000. Now we turn to an investigation of the Motorola MC68000, making use of the general procedure outlined in the November 20 article to delve into the innards of this second-generation 16-bit μP.

First, a general description: The MC68000 (**Fig 1**) is the first advanced 16-bit μP with a 32-bit internal architecture and the first with 16M-byte nonsegmented direct memory addressing. Its 32-bit registers include eight for data and seven for addressing, plus a program counter and two stack pointers (user and supervisor). All address registers can function as stack pointers, and all data and address registers can also serve as index registers. The μP's six basic addressing modes are actually equivalent to 14 when you consider all variations among them. These addressing modes, combined with the device's data and instruction types, provide more than 1000 useful instructions.

Because all I/O is implemented via memory mapping, the MC68000 requires no I/O instructions; any memory-reference instruction can perform I/O if a peripheral resides at the specified address. An 8-MHz

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PASCAL and the MC68000

The MC68000 provides several instructions that ease the task of generating code in such high-level block-structured languages as PASCAL. Here's how the μP performs some of the operations required to implement common PASCAL constructs.

Procedure calls	The 68000 employs a stack, pointed to by one of the address registers, to build the nested environment.
Push parameters, address	The MOVE instruction pushes data, and the PEA instruction pushes calculated addresses onto the stack.
Call procedure	Jump to Subroutine
Establish local environment	The LINK instruction saves the old contents of the frame pointer on the stack, points the new frame pointer to the top of the stack and subtracts the local-storage need from the stack pointer.
Save a subset of registers	Move Multiple Registers (MOVEM to memory)
Reload saved registers	Move Multiple Registers (MOVEM from memory)
Re-establish environment	UNLK undoes the work of LINK.
Return from procedure	RETURN
Restore the stack	Add Immediate instruction applied to the stack pointer

A single address register implements stacks

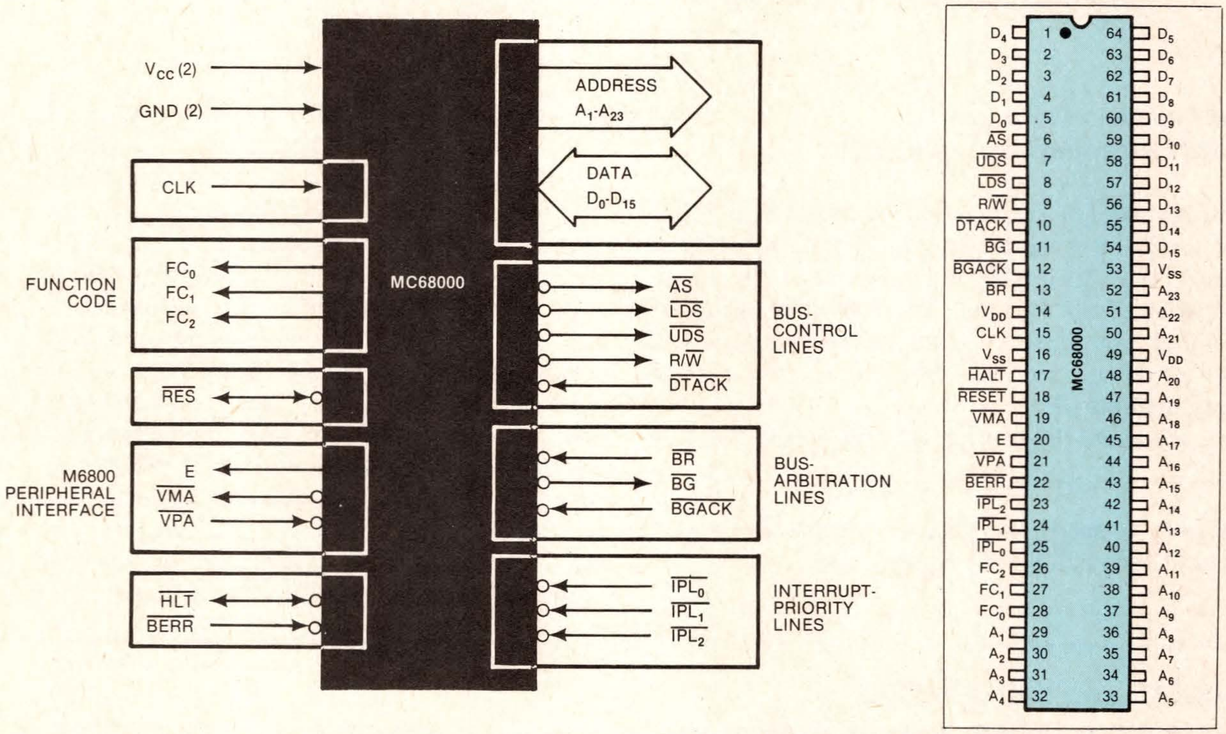
clock rate, combined with pipelining and the device's 32-bit internal registers, provides a system throughput of up to two million instructions and data transfers per second.

The μP supports five basic data types: bits, BCD digits, bytes, words and long words. It features a 16-bit nonmultiplexed data bus, a 24-bit address bus, an asynchronous bus for MC68000 peripherals and memory and a synchronous bus to accommodate MC6800 peripherals and memory. It also provides hardware- and software-interrupt capabilities, implements a Trace for software debugging, supports multiprocessing and can run in either supervisory or user states.

Data and address registers are 32 bits wide

In all, the CPU contains 17 32-bit registers (15 data and address registers plus two stack pointers), plus the 32-bit program counter and a 16-bit status register (**Fig 2**). The eight data registers support data operands of one, eight, 16 or 32 bits: Bit operands occupy any bit position, byte operands the low-order eight bits, word operands the lower 16 bits and long-word operands the entire 32 bits.

The address registers and stack pointers each hold a full 32-bit address. But address registers don't support byte-sized operands, so when such a register functions as a source operand, either the low-order word or the



A_1-A_{23}	ADDRESS LEADS	23-BIT ADDRESS BUS; CAPABLE OF ADDRESSING 16,777,216 BYTES IN CONJUNCTION WITH $\overline{UDS}$ AND $\overline{LDS}$
D_0-D_{15}	DATA LEADS	16-BIT DATA BUS, TRANSFERS EIGHT OR 16 BITS OF INFORMATION
$\overline{AS}$	ADDRESS STROBE	INDICATES VALID ADDRESS AND PROVIDES A BUS LOCK FOR INDIVISIBLE OPERATIONS
R/$\overline{W}$	READ/WRITE	DEFINES BUS OPERATION AS READ OR WRITE AND CONTROLS EXTERNAL BUS BUFFERS
$\overline{LDS}$, $\overline{UDS}$	DATA STROBES	IDENTIFIES THE BYTE(S) TO BE OPERATED ON ACCORDING TO R/$\overline{W}$ AND $\overline{AS}$
$\overline{DTACK}$	DATA TRANSFER ACKNOWLEDGE	ALLOWS THE BUS CYCLE TO SYNCHRONIZE WITH SLOW DEVICES OR MEMORIES
$\overline{BR}$	BUS REQUEST	INPUT TO THE PROCESSOR FROM A DEVICE REQUESTING CONTROL OF THE BUS
$\overline{BG}$	BUS GRANT	OUTPUT FROM THE PROCESSOR GRANTING BUS CONTROL
$\overline{BGACK}$	BUS GRANT ACKNOWLEDGE	CONFIRMATION SIGNAL FROM NEW BUS MASTER INDICATING THAT IT NOW HAS CONTROL OF THE BUS
$\overline{IPL_0}$, $\overline{IPL_1}$, $\overline{IPL_2}$	INTERRUPT PRIORITY LINES	PROVIDES THE PRIORITY LEVEL OF THE INTERRUPTING FUNCTION TO THE PROCESSOR
FC_0, FC_1, FC_2	FUNCTION CODE	PROVIDES EXTERNAL DEVICES WITH INFORMATION ABOUT THE CURRENT BUS CYCLE
CLK	CLOCK	MASTER TTL INPUT CLOCK TO THE PROCESSOR
$\overline{RES}$	RESET	PROVIDES RESET (INITIALIZATION) SIGNAL TO THE PROCESSOR AND PERIPHERAL DEVICES
$\overline{HLT}$	HALT	HALTS THE PROCESSOR
$\overline{BERR}$	BUS ERROR	INPUT FROM EXTERNAL CIRCUITRY TO CAUSE CURRENT BUS CYCLE TO TERMINATE
E	ENABLE	ENABLE CLOCK FOR M6800 SYSTEMS
$\overline{VPA}$	VALID PERIPHERAL ADDRESS	IDENTIFIES ADDRESSED AREA AS AN M6800-COMPATIBLE AREA
$\overline{VMA}$	VALID MEMORY ADDRESS	INDICATES TO M6800-FAMILY DEVICES THAT A VALID ADDRESS IS ON THE BUS (GENERATED WITH RESPECT TO ENABLE)
V_{CC}	5V (2 PINS)	—
GND	GROUND (2 PINS)	—

Fig 1—Housed in a 64-pin package, *the MC68000 requires a single 5V power supply.*

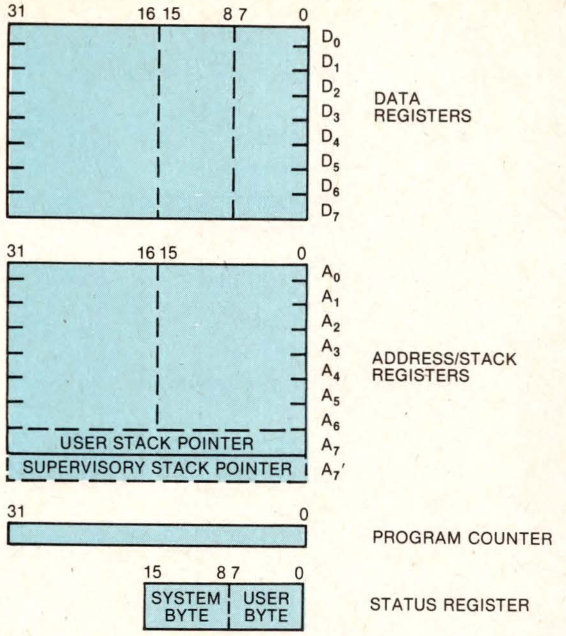


Fig 2—Register complement *of the MC68000 includes 18 32-bit configurations and a 16-bit unit.*

entire long-word operand is used, depending on the operation size. And when an address register serves as a destination operand, the entire register is affected, regardless of the operation size.

Implementing stacks and queues

The MC68000 supports stack and queue data structures by means of address-register-indirect post-increment and predecrement addressing modes. That is, employing a single address register, you can implement stacks that get filled starting at high memory locations and proceeding to low ones, or vice versa. Utilizing a pair of address registers allows you to implement queues that get filled similarly. (This process requires two registers—the put and get pointers—because queues are pushed from one end and pulled from the other.)

Address register A_7 is the system stack pointer (SP), functioning as either the supervisor stack pointer (SSP) or the user stack pointer (USP) depending on the state of the S bit in the status register. The program counter is saved on the SP stack at the start of subroutine calls and restored from the SP on returns. When processing traps and interrupts, the μP saves and restores both the program counter and the status register on the SP stack.

The status register **(Fig 3)** contains the MC68000's interrupt mask (eight levels available) as well as its condition codes: extend (X), negative (N), zero (Z), overflow (V) and carry (C). Additional status bits indicate that the μP is in a Trace (T) mode and/or a supervisor (S) state.

Performing efficient context switching

An interesting characteristic of the MC68000 is its ability to implement exception processing—a deviation from normal processing arising from either an internal instruction or error condition or an external request or error condition. The internal triggers come from instructions (TRAP, TRAPV, CHK, DIV), address errors or the Trace mode; the external types, from interrupts, bus errors or a reset. The μP implements seven prioritized interrupts, and 192 vectored address vectors are available (see **table**). Traps function to catch improper operation and serve as software interrupts.

To further aid in program development, the MC68000 includes a facility to allow instruction-by-instruction tracing. In the Trace state, forcing an exception after each instruction is executed allows a debugging program to monitor the execution of the program under test (see **box,** "Tracing software bugs").

Memory-addressing range—same as the IBM 370's

The MC68000 can directly address (without segmentation) more than 16M bytes of memory. This large address space is managed on a word or byte basis;

MC68000 EXCEPTION-VECTOR ASSIGNMENT

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial SSP
	4	004	SP	Reset: Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15*	60	03C	SD	(Unassigned, reserved)
16-23*	64	040	SD	(Unassigned, reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Auto-Vector
26	104	068	SD	Level 2 Interrupt Auto-Vector
27	108	06C	SD	Level 3 Interrupt Auto-Vector
28	112	070	SD	Level 4 Interrupt Auto-Vector
29	116	074	SD	Level 5 Interrupt Auto-Vector
30	120	078	SD	Level 6 Interrupt Auto-Vector
31	124	07C	SD	Level 7 Interrupt Auto-Vector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—

*Vector numbers 12 through 23 and 48 through 63 are reserved for future enhancements. No user peripheral devices should be assigned these numbers.

NOTE: Memory layout is 512 words long (1024 bytes); it starts at address 0 and proceeds through address 1023, providing 255 unique vectors (some of these are reserved for traps and other system functions). Of the 255, 192 are reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the system designer.

Exception processing aids software debugging

operand size is specified in the instruction. The use of Upper Data Strobe (UDS) and Lower Data Strobe (LDS) signals provides easy access to high-order bytes, low-order bytes or words.

Motorola also provides a memory-management unit (MMU) to implement address relocation and memory protection. This MMU permits definition of multiple segments; each segment defines a logical-address segment location, an offset to a physical address and the

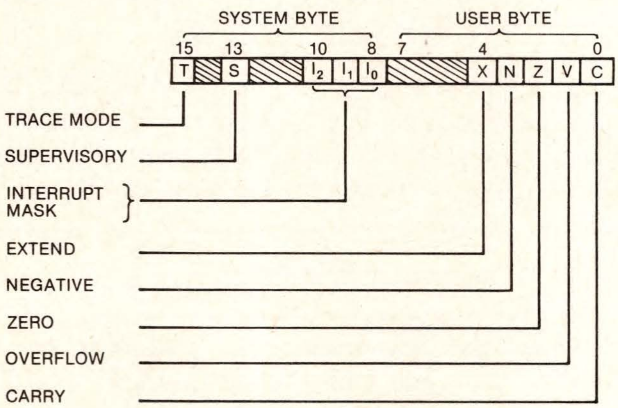


Fig 3—Unused bits *in the MC68000 status register are ZEROs and are reserved for future expansion.*

Mode	Generation
Register Direct Addressing	
Data register direct	$EA = D_n$
Address register direct	$EA = A_n$
Absolute Data Addressing	
Absolute short	EA = (Next Word)
Absolute long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with offset	$EA = (PC) + d_{16}$
Relative with index and offset	$EA = (PC) + (X_n) + d_8$
Register Indirect Addressing	
Register indirect	$EA = (A_n)$
Postincrement register indirect	$EA = (A_n), A_n \leftarrow A_n + N$
Predecrement register indirect	$A_n \leftarrow A_n - N, EA = (A_n)$
Register indirect with offset	$EA = (A_n) + d_{16}$
Indexed register indirect with offset	$EA = (A_n) + (X_n) + d_8$
Immediate Data Addressing	
Immediate	Data = Next words(s)
Quick immediate	inherent data
Implied Addressing	
Implied register	EA = SR, USP, SP, PC

NOTES:

EA = Effective address	d_8 = 8-bit offset (displacement)
A_n = Address register	D_{16} = 16-bit offset (displacement)
D_n = Data register	N = 1 for byte, 2 for words and 4 for long words
X_n = Address or data register used as index register	← = Replaces
SR = Status register	
PC = Program counter	
( ) = Contents of	

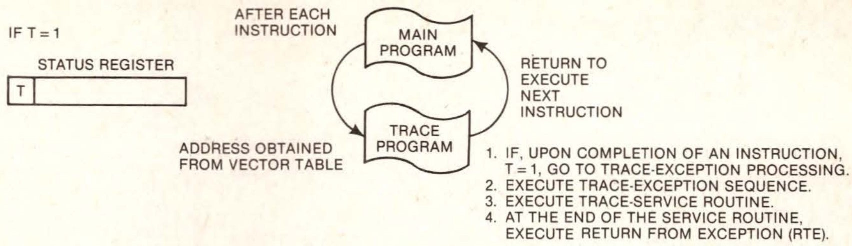
Fig 4—Considering variations, *the μP's six basic addressing modes actually consist of 14 types.*

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBCC	Test Cond, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral Data
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
SCC	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

Fig 5—Consisting of 56 basic types, *the MC68000's instruction set is very regular.*

Tracing software bugs

The MC68000's Trace mode permits instruction-by-instruction tracing of software by a debugging program. The nearby **figure** illustrates this operation.



Instruction Type	Variation	Description
ADD	**ADD**	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	**AND**	Logical AND
	ANDI	AND Immediate
CMP	**CMP**	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	**EOR**	Exclusive OR
	EORI	Exclusive OR Immediate

Instruction Type	Variation	Description
MOVE	**MOVE**	Move
	MOVEA	Move Address
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	**NEG**	Negate
	NEGX	Negate with Extend
OR	**OR**	Logical OR
	ORI	OR Immediate
SUB	**SUB**	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

Fig 6—Variations *on the basic instruction types complete the μP's instruction set.*

necessary address-space parameters for memory protection. Segments can have variable lengths (256 to 16M bytes in 256-byte increments), and you can cascade multiple MMUs for greater segment definition.

The MC68000's 14 flexible addressing modes **(Fig 4)** include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied.

Included in the Register Indirect mode is the ability to perform postincrementing, predecrementing, offset-

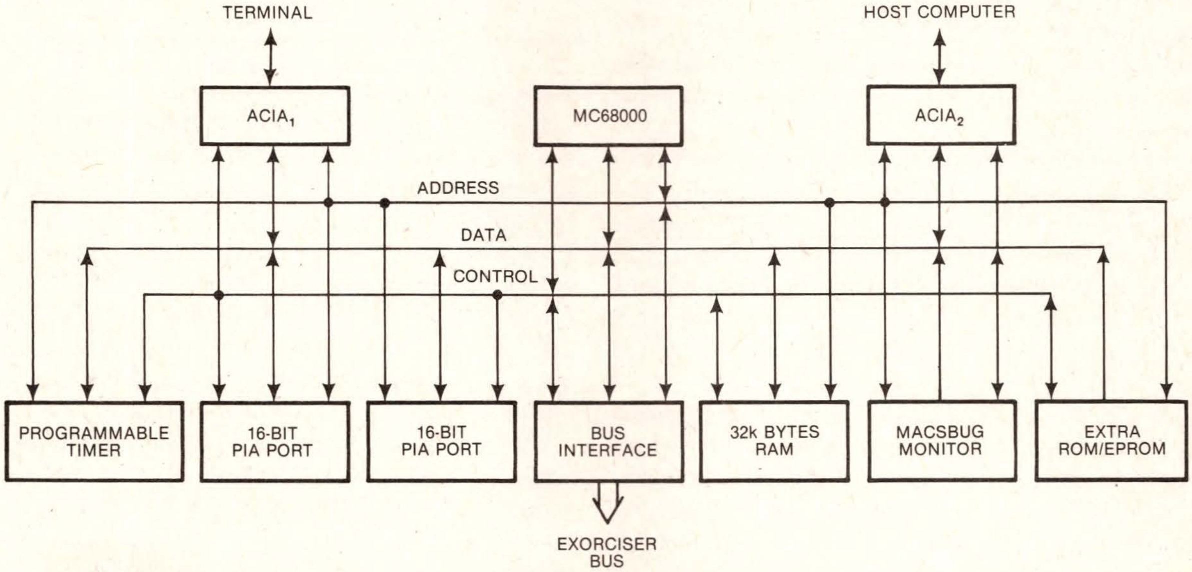


Fig 7—A powerful single-board computer, *the MC68000 Design Module permits evaluation of the μP.*

One mnemonic serves byte, word and long-word use

ting and indexing operations. Program Counter Relative mode can also be modified via indexing and offsetting.

By means of hardware and software interlocks, the MC68000 also supports multiprocessor systems. The μP contains bus-arbitration logic for use in a shared-bus and shared-memory environment (that is, shared with other MC68000s, with DMA devices, and so forth). Multiprocessor systems are also supported by means of software instructions (for example: TAS, the Test and Set operand).

A highly regular instruction set

The MC68000's instruction set appears in **Fig 5;** some additional instructions are variations or subsets of these basic commands and appear in **Fig 6.** The instructions fall into the following categories:

- Data movement
- Integer arithmetic
- Shifts and rotates
- Bit manipulation
- Binary coded decimal
- Program control
- System control.

Each instruction—with few exceptions—operates on bytes, words and long words, and most instructions can utilize any of the μP's 14 addressing modes. As a key advantage, no separate instructions are required for operation on bytes, words and long words—you remember just one mnemonic for each type of operation and merely specify the data size and source and destination addressing modes.

The MC68000 instruction set contains several instructions (unique to the μP world) that aid the generation of code from high-level block-structured languages (see **box,** "PASCAL and the MC68000"). Two of these instructions, LINK and UNLK, maintain a list of local data and parameter areas on the stack for nested subroutine calls.

LINK takes an address register and an immediate constant as its parameters: The constant specifies the number of stack bytes to reserve, and the address register functions as the pointer to the data area. The SP is then adjusted to clear the space, and the previous value of the address register is stacked. UNLK reverses this process, reclaiming the stack space and restoring the pointer value.

A single LINK instruction at the head of a subroutine sets up the storage for the subroutine and provides addressing. A single UNLK instruction at the subroutine's end restores the stack and the addressing pointer. Thus, you can nest procedures as desired; LINK and UNLK automatically accommodate local data addressing. Procedures using LINK and UNLK to allocate variable space are re-entrant, and data

COMMAND	DESCRIPTION
reg#	Print a register
reg# hexdata	Put a hex value in the register
reg# 'ASCII'	Put hex-equivalent characters in register
reg#:	Print the old value and request new value
class	Print all registers of a class (A or D)
class:	Sequence through—print old value request new
DM start end	Display memory, hex-ASCII memory dump
SM address data	Set memory with data
OPen address	Open memory for read/change
SYmbol NAME value	Define and print symbols
W#	Print the effective address of the window
W#. 1en EA	Define window length and addressing mode
M# data	Memory in window, same syntax as register
Go	Start running from address in program counter
Go address	Start running from this address
Go TILL add	Set temporary breakpoint and start running
BReakpoint	Print all breakpoint addresses
BR add: count	Set a new breakpoint and optional count
BR—address	Clear a breakpoint
BR CLEAR	Clear all breakpoints
TD	Print the trace display
TD reg#. format	Put a register in the display
TD Clear	Take all registers out of the display
TD ALl	Set all registers to appear in the display
TD A. 1 D. 1 L. c	Set register blocks or line separator
T	Trace one instruction
T count	Trace the specified number of instructions
T TILL Address	Trace until this address
:*(CR)	Carriage return—trace one instruction
OFfset address	Define the global offset
CV decimal	Convert decimal number to hex
CV $hex	Convert hex to decimal
CV value,value	Calculate offset or displacement
REad ; = text	Expect to receive 'S' records
VErify ; = text	Check memory against 'S' records
PUnch start end	Print 'S' records (tape image)
FOrmat hex	Program/initialize an ACIA
NUll hex	Set character null pads
CR hex	Set carriage return null pads
TErminal baud	Set terminal null pads to default values
CAll address	JSR to user utility routine
P2	Enter transparent mode
*..data..	Transmit command to host
Break	The BREAK key aborts most commands
CTL-A	The control A key ends transparent mode
CTL-D	The control D key redisplays the line
CTL-H	The control H key deletes the last character entered
CTL-W	The control W key suspends output until another character is entered
CTL-X	The control X key cancels the entire line
Rubout	The RUBOUT key deletes the last character entered
Del	The DEL key deletes the last character entered

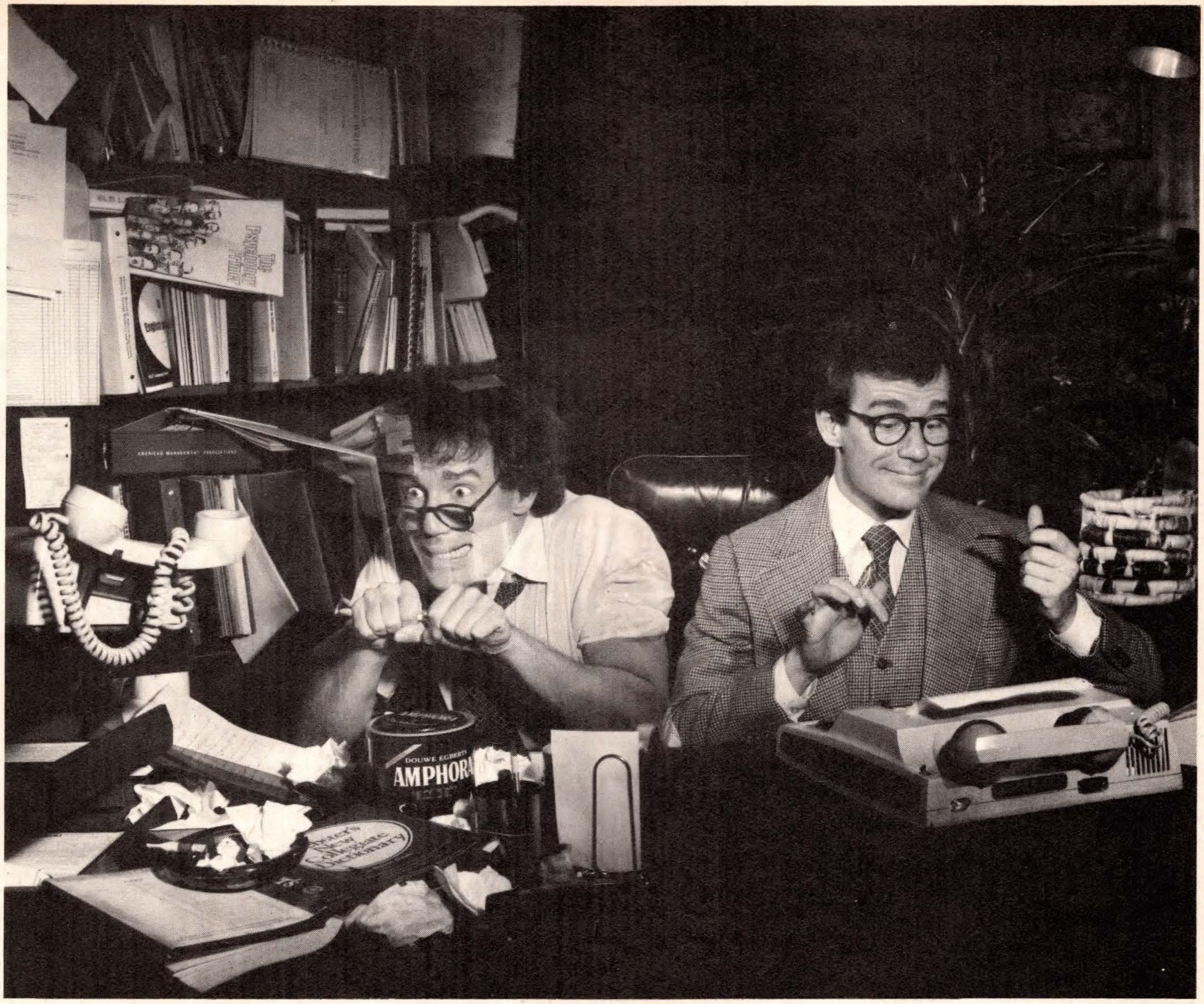
Fig 8—Perhaps the most powerful *and comprehensive μC monitor yet developed by a chip manufacturer, MACSBUG occupies 8k bytes.*

addressing is position independent.

Another instruction that simplifies the use of the stack is PEA (Push Effective Address). This command permits passing any addressable data to a subroutine by putting the subroutine's address on the stack. Using PEA with the μP's rich set of addressing modes makes subroutine parameter passing easy.

The MC68000's MOVEM (Move Multiple Registers) instruction also reduces subroutine-call programming overhead; it permits moving (via an effective address) multiple registers specified by the user.

The checking of array indices against boundary values, or other range checking, is a frequent task required of compiled code. To aid in this task, the CHK (Check) instruction causes a trap if a data register is either less than zero or greater than some specified value (which may be defined as an effective address). This single instruction does the job of several



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Design Module communicates through two ACIAs

commands on other μPs.

Finally, the MC68000's proprietary microcoded structure offers the possibility of producing specialized versions of the μP while retaining the device's basic structure. Rumor has it that Motorola has already implemented floating-point arithmetic by means of this microcoding.

Design Module permits device evaluation

The MC68000 Design Module (DM) (**Fig 7**) consists of a single-board μC and sports the following features:

- Exorciser-compatible bus
- 32k bytes of dynamic RAM
- 8k bytes of system monitor
- Extra ROM/EPROM user sockets
- Downloading host-computer port
- Two 16-bit parallel I/O ports
- Three 16-bit timers
- User wire-wrapping area
- Extensive debugging routines (monitor).

Communications to the DM occur through two asynchronous communications ports (ACIAs); one of these ports is configured for connection to a standard RS-232C terminal, while the other is configured as a standard RS-232C data terminal to communicate with a host computer. This arrangement permits placing the DM in series with a terminal and a host; a Transparent mode then bypasses the DM and allows creation of a program on the host and downloading of that program into the DM for execution and debugging—without reconfiguring the system's cabling.

The DM's programmable timer module (PTM) can time the execution of routines because it runs either at the fixed frequency of one-tenth the μP clock speed or from an external source. The PTM also permits variable frequency generation, pulse-width measurements and variable pulse-width generation.

The board's bus interface implements system expansion; the Exorciser bus accommodates a wide range of peripherals and memories. Specifically, the bus provides for a 16-bit data path and a 128k-byte address range and permits accessing of both asynchronous and synchronous peripherals.

On the software-support side, the DM's MACSBUG monitor (**Fig 8**) is an 8k-byte firmware program that provides for memory examination, program loading and controlled program execution. You also have the option of inserting three pairs of additional user ROMs; the board's four pairs of sockets have jumper options that accommodate a variety of EPROMs and masked ROMs. **EDN**

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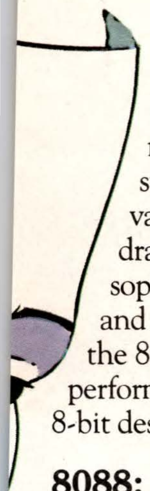

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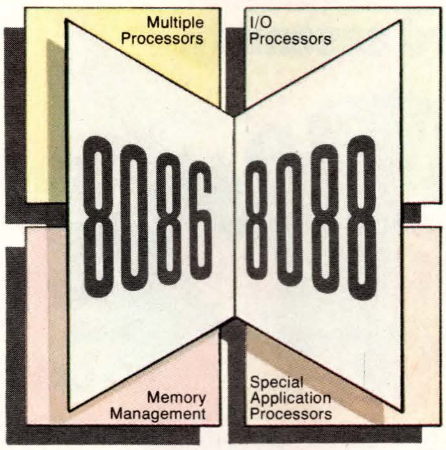

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Phase/frequency-locked loops handle random inputs

Now you need no longer suffer with the problems of phase-locked loops to accommodate random input data; phase/frequency-loop circuits offer narrow bandwidth and wide lock range.

Sid Ghosh and **Christian Foster,** TRW Vidar

Bandwidth and pull-in (acquisition) range pose two key considerations in the design of a phase-locked loop. The circuits presented here reflect these considerations, improving on basic PLL design in terms of both factors. To understand the concepts underlying the designs, start by considering some basics.

Loop bandwidth is given by **(Ref 1)**:

$$B_L = \frac{\omega_n}{2}\left(\rho + \frac{1}{4\rho}\right),$$

and lock-in range equals

$$\Delta\omega_L \approx 2\rho\omega_n.$$

These equations indicate that the two parameters are directly proportional.

When a PLL's input is random data, some applications require loop bandwidth to be extremely narrow in order to reject input jitter and maintain lock in the presence of long strings of ZEROs or ONEs. But with such a narrow bandwidth, the loop generally cannot acquire lock unaided. Several design schemes deal with this problem.

Take advantage of frequency detection

One frequently employed technique complements the usual phase comparator with a frequency comparator in the loop **(Fig 1)**. When the loop is out of lock, the input and VCO frequencies don't agree, and the frequency comparator's output helps the phase-comparator output achieve acquisition. Once the loop achieves lock, however, the frequency-comparator output vanishes, and the circuit operates like a standard PLL.

A simple discriminator suffices for the frequency comparator when both the input and VCO output are sinusoidal. Most practical digital data-transmission

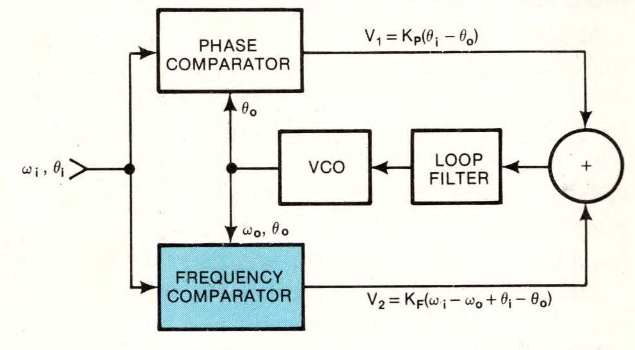

Fig 1—In a phase/frequency-locked loop, *an added frequency comparator inside the loop aids acquisition. Once the circuit achieves lock, the frequency-comparator output becomes zero.*

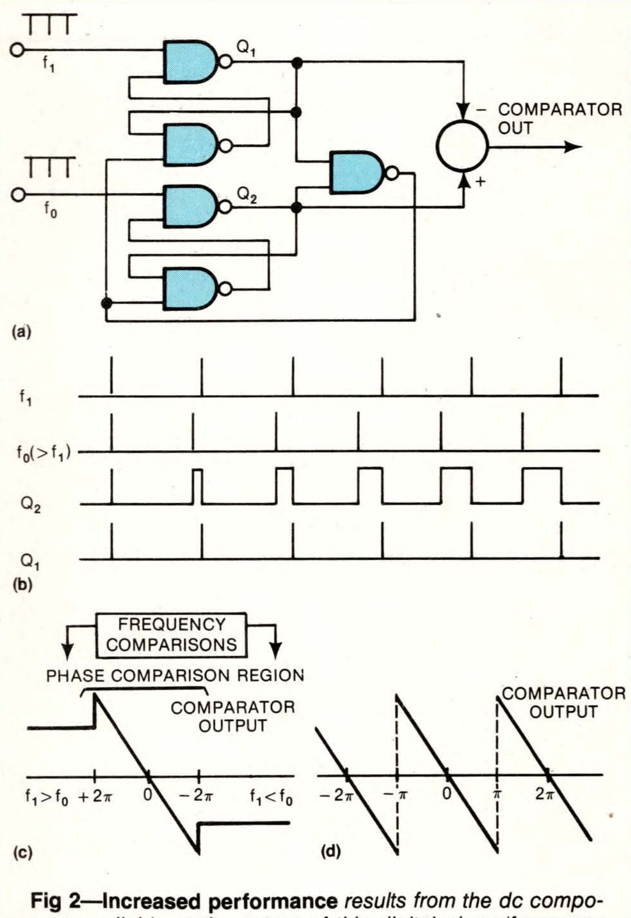

Fig 2—Increased performance *results from the dc component available at the output of this digital phase/frequency comparator. The dc component allows you to make loop bandwidth small while ensuring that the loop is able to achieve lock. Compare the comparator's transfer characteristics* **(c)** *with those of a simple phase comparator* **(d).**

Jitter rejection calls for very narrow bandwidth

systems, however, employ digital phase/frequency (ϕ/F) comparators (**Refs 2, 3**). The implementation and transfer characteristics of such a circuit appear in **Fig 2**, along with a typical phase comparator's transfer characteristics.

The phase-comparator output (**Fig 2d**) is bipolar, alternating in polarity at twice the local-oscillator beat frequency. For a simple PLL to achieve unconditional lock, its bandwidth must be wide enough to pass the fundamental component of this bipolar waveform with virtually no attenuation. In contrast, the digital ϕ/F comparator shows remarkable output characteristics: When the loop is out of lock, the correction voltage has a dc component. Thus, the loop bandwidth can be arbitrarily small, yet the loop is still able to achieve lock.

Despite its advantages, though, **Fig 2**'s ϕ/F comparator exhibits one problem. Under a lock condition, every transition of the input clock must coincide with a local-clock transition to ensure proper operation of the loop. Essentially, the circuit doesn't function at all if its input is synchronous random data.

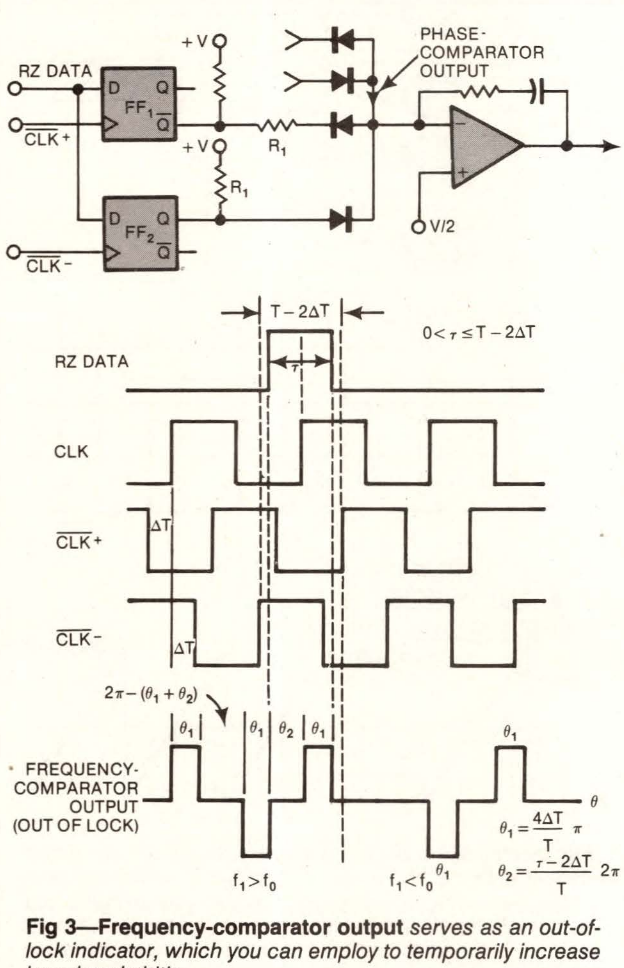

Fig 3—Frequency-comparator output *serves as an out-of-lock indicator, which you can employ to temporarily increase loop bandwidth.*

Bandwidth manipulation solves the problem

A technique that proves useful in handling such random input data involves increasing the bandwidth when the loop is out of lock and then considerably reducing it once the loop achieves lock (**Ref 4**). One previously published implementation of the technique does indeed result in a ϕ/F-locked loop suitable for handling random input data (**Ref 5**); this scheme requires analog multipliers. There are, however, alternative schemes—including designs that are totally digital.

In the digital frequency comparator used in one such scheme (**Fig 3**), two additional clocks (CLK^+ and CLK^-) are derived from the loop clock (CLK), which gates the comparator. Relative to CLK, CLK^+ and CLK^- are advanced by ΔT_1 and delayed by ΔT_2, respectively. While ΔT_1 and ΔT_2 need not be equal, assume that they are. The RZ data—whose width must be less than $T-2\Delta T$—is clocked into two flip flops by CLK^+ and CLK^-, and the comparator output reflects the difference in the two flip-flop outputs.

If the circuit is in a lock condition, the output of the frequency comparator is zero; hence the phase comparator controls the loop. Now suppose that an increase in the data rate causes the loop to lose lock. As the data advances relative to the clock, any input ONE clocks Q_2 HIGH and Q_1 LOW. Over the interval θ_1, the frequency comparator's output is thus positive. As the input data's phase advances, an input ONE is clocked into both flip flops, and the comparator output goes to zero. After a further interval θ_2, the flip flops reverse state, resulting in a negative comparator output.

In summary, the frequency-comparator output is zero in a lock condition and alternating when the loop is out of lock. You can thus add this output to that of the phase comparator to help achieve loop acquisition. Unfortunately, because the frequency-comparator output is bipolar, the loop filter bandwidth is still a constraint with respect to acquisition range. However, making R_1 very small results in a relatively large bandwidth under out-of-lock conditions. You can therefore consider the frequency-comparator output as an out-of-lock indicator, usable to temporarily increase loop bandwidth.

Modification adds dc component

While this performance might prove adequate in many applications, the presence of a dc component in the frequency-comparator output under out-of-lock conditions also proves highly useful, and you can modify **Fig 3**'s circuit to produce such a dc output component (**Fig 4a**). Now, the two flip-flop outputs trigger two monostables, which in turn set two latches. The latching sequence depends on whether the input clock is faster or slower than the local clock, but once the first latch sets, the other is disabled.

The latches reset only when both monostable outputs are ZERO. And once triggered, a monostable doesn't change state—even when the input data contains a long series of ZEROs. Therefore, once one of the latches

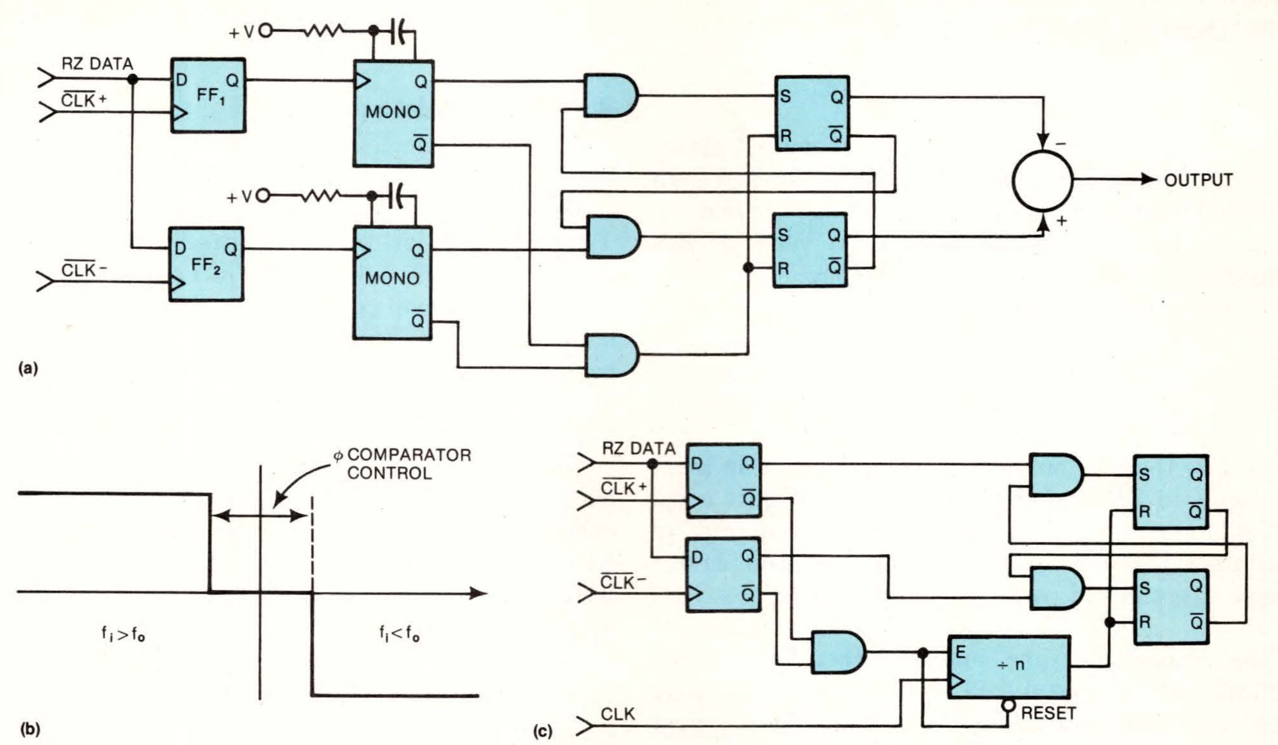

Fig 4—Handle random data easily *with this modified frequency comparator* ***(a)****, whose transfer characteristics appear in* ***(b)****. An alternative design* ***(c)*** *proves more appropriate for handling high-speed data.*

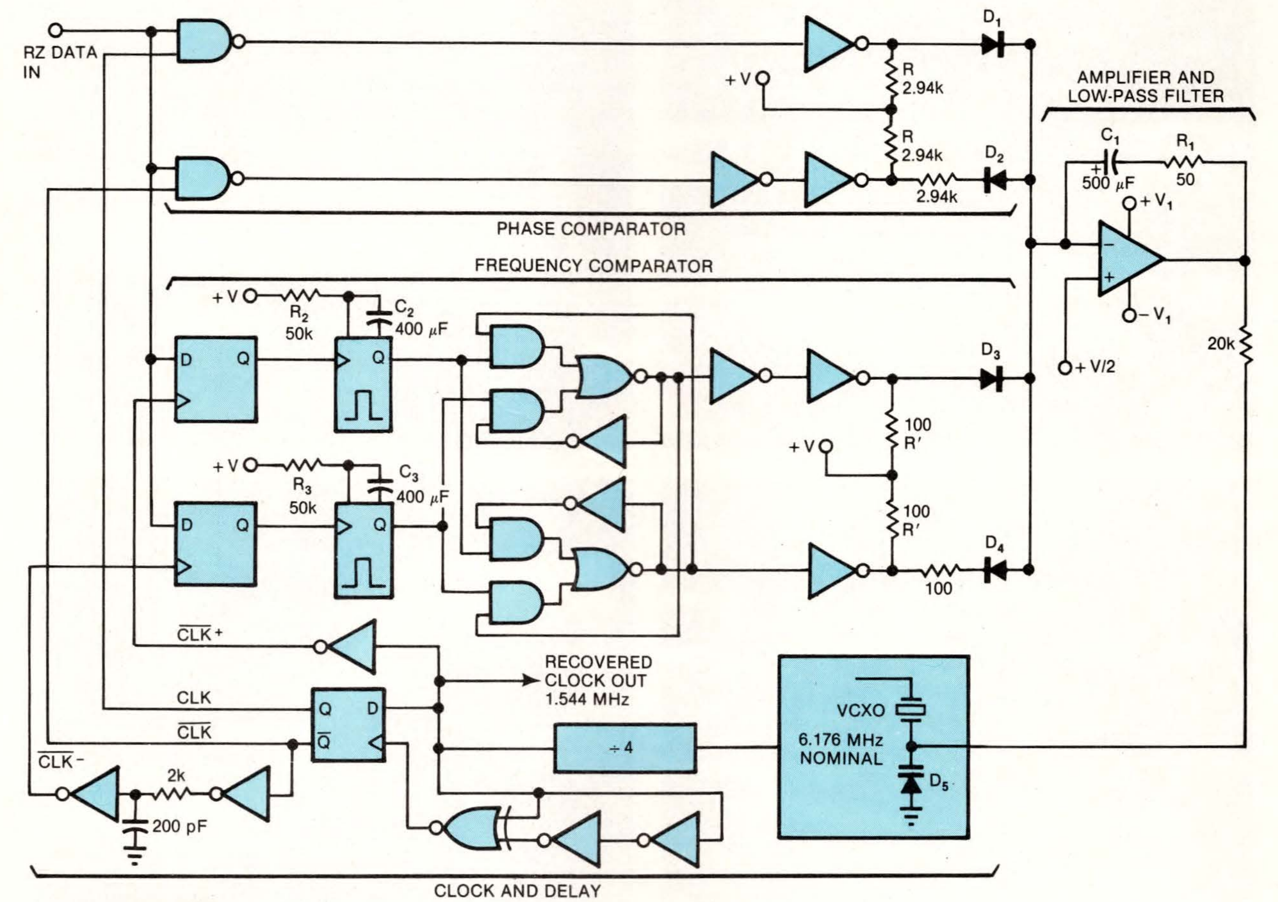

Fig 5—Complete freedom in the choice of bandwidth *is a prime feature of this phase/frequency-locked loop. However, the circuit does call for compromises between jitter rejection and acquisition time. R_2, R_3, C_2 and C_3 are selected to provide pulse length greater than the maximum time of all-ZERO input data; typical values are shown.*

sets, the frequency-comparator output doesn't disappear until the phase comparator takes over and both flip-flop outputs are ZERO for an extended period.

Here's how to compute the design value of this monostable delay period. Start by letting

T = 0.65 μsec (1.544M-bps bit rate)

τ = 0.35 μsec

ΔT = 0.1 μsec

Δf = 300 Hz (frequency difference between input data rate and local clock).

To ensure that the output won't change with an input string of 16 ZEROs, the minimum delay must equal $16T \approx 11$ μsec. The maximum delay required to guarantee that any data bit in the phase-comparator region is not forced past that region is thus

$$(T-\tau-2\Delta T)/T\Delta f \approx 500 \ \mu\text{sec}.$$

The monostable time constant, therefore, is not critical. For high-speed data, however, the alternative frequency-comparator design shown in **Fig 4c** might prove more convenient. Here, a divide-by-n counter replaces the two monostables. With this arrangement, the latches (once set) are reset when both flip flops are clear for n successive bits.

Putting theory into practice

A practical implementation of a ϕ/F-locked loop embodying the foregoing principles appears in **Fig 5.** To evaluate its performance, a test circuit generated RZ data with large low-frequency jitter. Test results **(Fig 6a)** show the ϕ/F-locked loop's jitter-rejection characteristics for a loop configuration with a very narrow bandwidth. The output of a basic PLL, with filter bandwidth adjusted to ensure lock, also appears **(Fig 6b)** for comparison. The ϕ/F-locked loop's performance improvement is obvious.

While the frequency comparator's dc output under out-of-lock conditions provides complete freedom in the choice of loop bandwidth, you must consider acquisition time *and* noise rejection when determining filter bandwidth. For a PLL, the former quantity is approximately **(Ref 1)**

$$T_A = \frac{4.2(\Delta f)^2}{B_L{}^3} \text{ for } \rho = 0.7.$$

For the ϕ/F-locked loop with dc output, however, if the

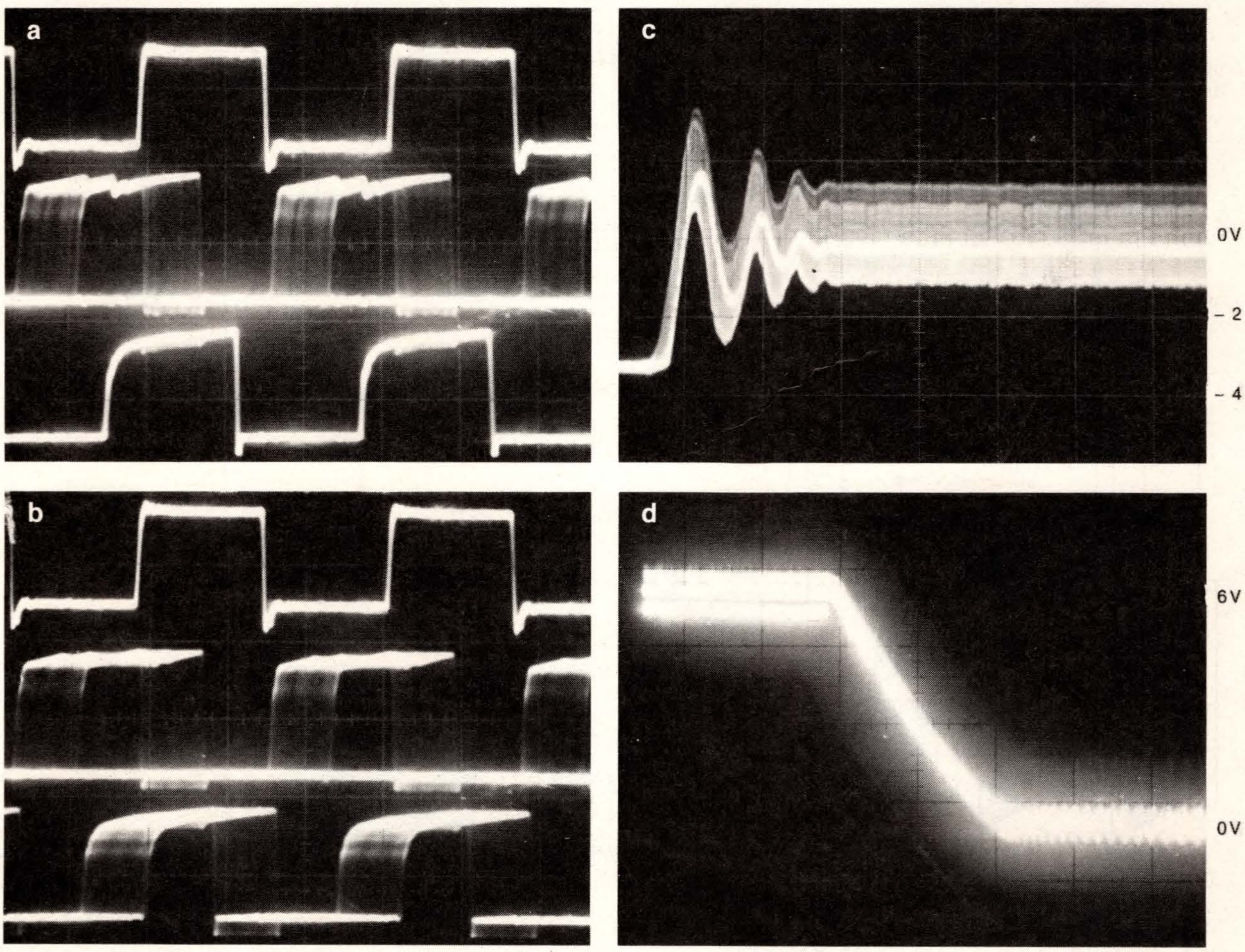

Fig 6—Jitter reduction *in recovered clock (bottom trace) is greater in the phase/frequency design* **(a)** *than in a simple phase-locked loop* **(b)**. *Acquisition behavior is also shown for phase-locked* **(c)** *and phase/frequency-locked* **(d)** *loops.*

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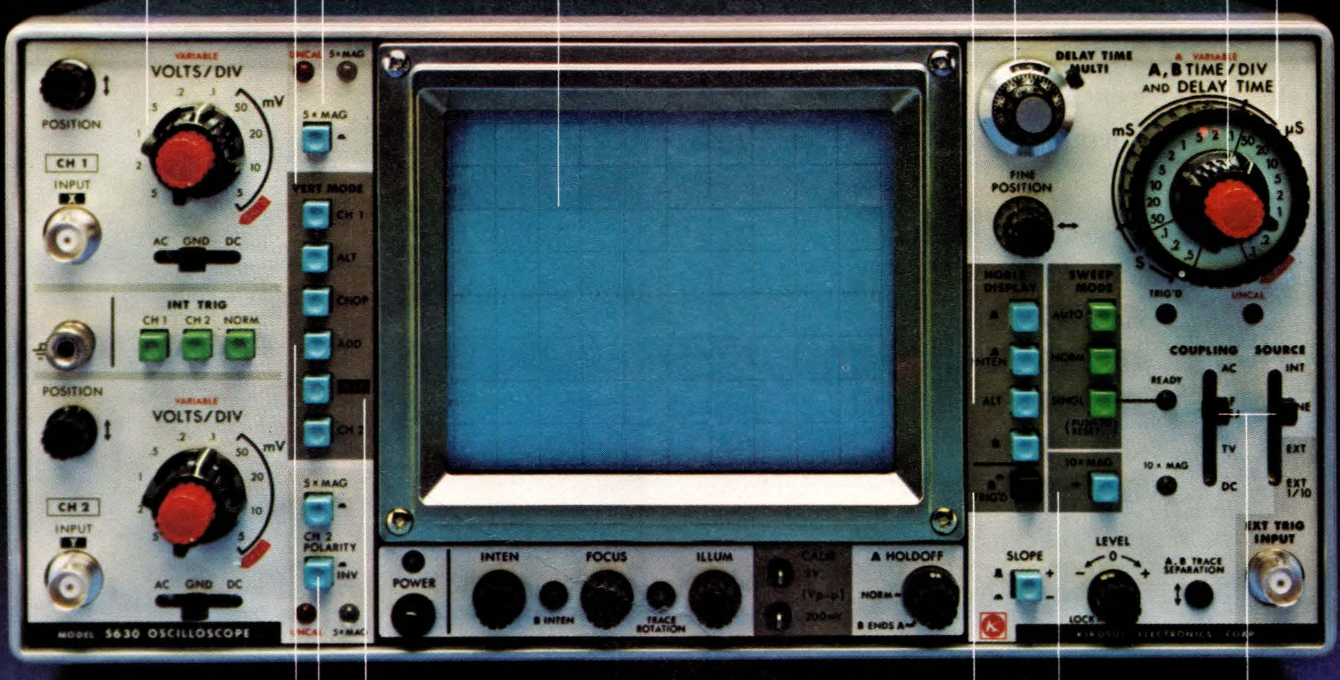

Performance improvements with the design are obvious

filter amplifier must change by $\overline{V}$ to acquire lock, the acquisition time (assuming the amplifier remains linear during the entire acquisition period) is

$$T_A = \frac{\overline{V}}{V}(2R'C_1).$$

Note that the filter bandwidth is determined by R, R_1 and C_1—not by R′. You can therefore make R′ very small to achieve rapid acquisition.

The difference in acquisition behavior for a simple phase-locked loop and a ϕ/F-locked loop is also shown (**Figs 6c** and **6d,** respectively). For practical reasons, both loops were underdamped (ρ=0.1). EDN

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Authors' biographies

Sid Ghosh is an engineering supervisor at TRW Vidar, Mt View, CA, where he designs and develops hardware for telephone systems. A graduate of London University, he's a member of the IEEE and holds seven patents.

Christian Foster is a design engineer at TRW Vidar. A recent graduate of Stanford University, he enjoys flying and skiing.

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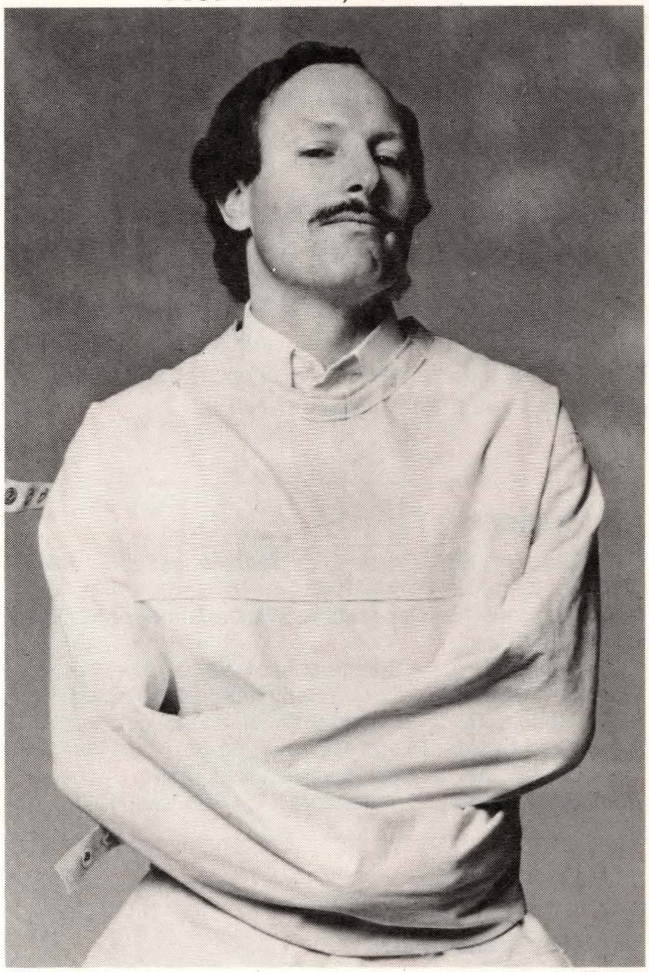

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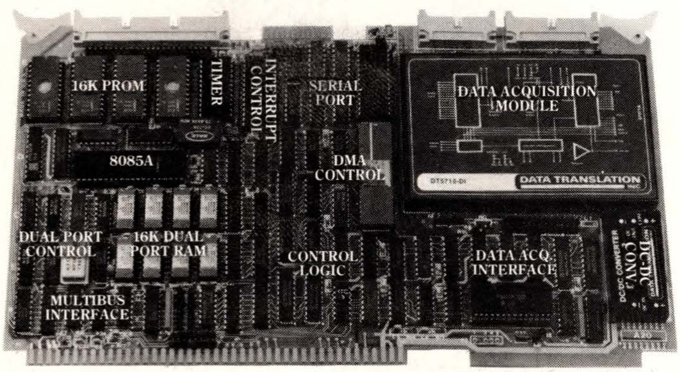

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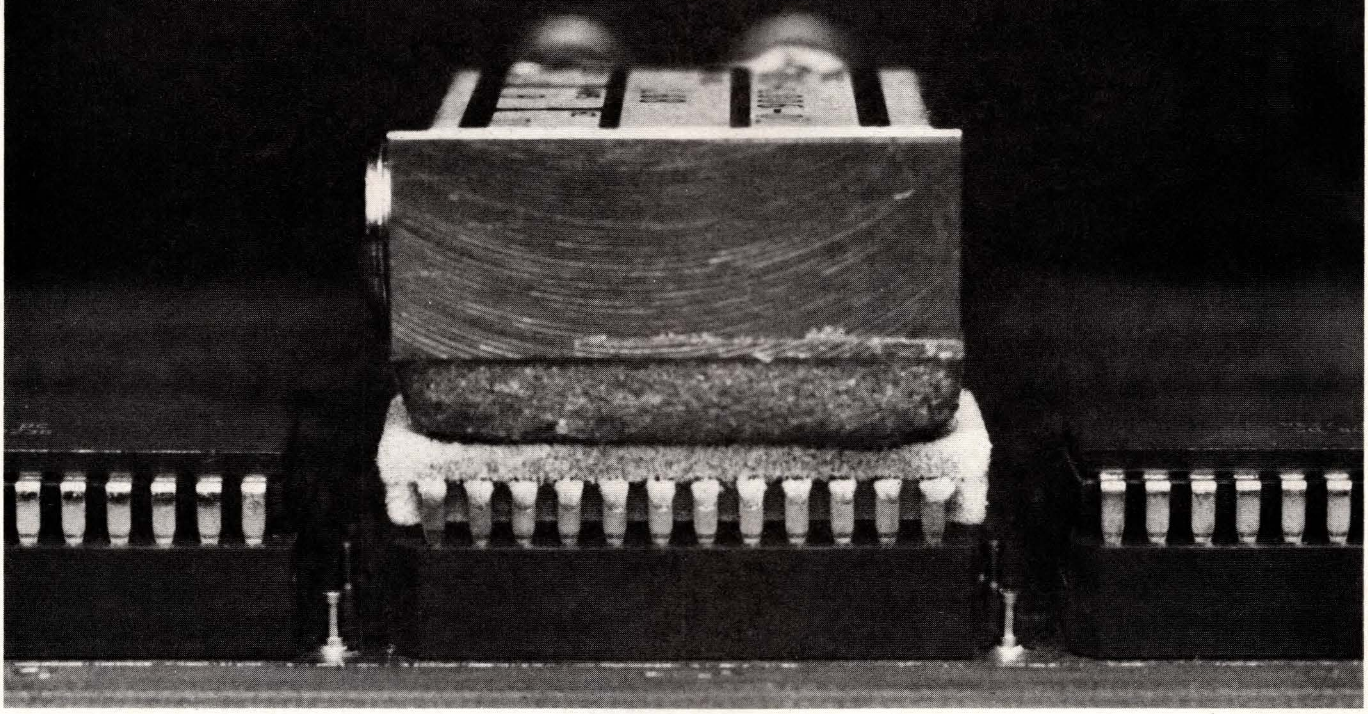

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When multiplexing analog inputs, avoid error traps

Connecting transducer lines to multiplexers presents inherent pitfalls that could undermine an A/D system's performance. Corrective design approaches help avoid potential signal-noise and interference hazards.

James V DiRocco, ADAC Corp

Effective design of front-end multiplexers for high-speed data-acquisition systems calls for careful investigation of the source, strength and effects of stray signals in addition to the expected range of transducer output levels. Performance problems generally arise from noise radiation, normal-mode pickup and lack of common-mode rejection, all of which exist in industrial and process-control A/D-conversion environments.

Indeed, even simple wiring and interconnection resistances demand strict attention, because common-ground returns and extraneous voltage drops add to a system's error budget. Resolving these widespread signal complexities involves taking advantage of proven grounding, source-impedance and cable-capacitance design techniques.

Proper grounding eliminates current loops

The most common complication in interfacing analog inputs to multiplexers concerns grounding. You can easily degrade a data-acquisition system's integrity by improperly grounding the input sources and their shielded lines.

Most computer-based systems require tying the computer power supply's return firmly to system power return, further complicating grounding considerations. Specifically, because the A/D converter communicates with the computer, designers generally connect the analog return to the digital return and the latter to power return—a scheme that minimizes digital-interference problems within the converter but increases the deleterious effects of ground loops.

Successful grounding in this case involves recalling a fundamental concept: A voltage exists across two points, not just one. A system measures the sum of the desirable source voltage plus any voltage induced in its leads to the multiplexer. Thus, you must keep extraneous currents from flowing in the signal-return lead as well as the signal-"hot" lead.

Fig 1 shows a single-ended-input source connected by shielded cable to a MUX (see **box,** "Multiplexers handle

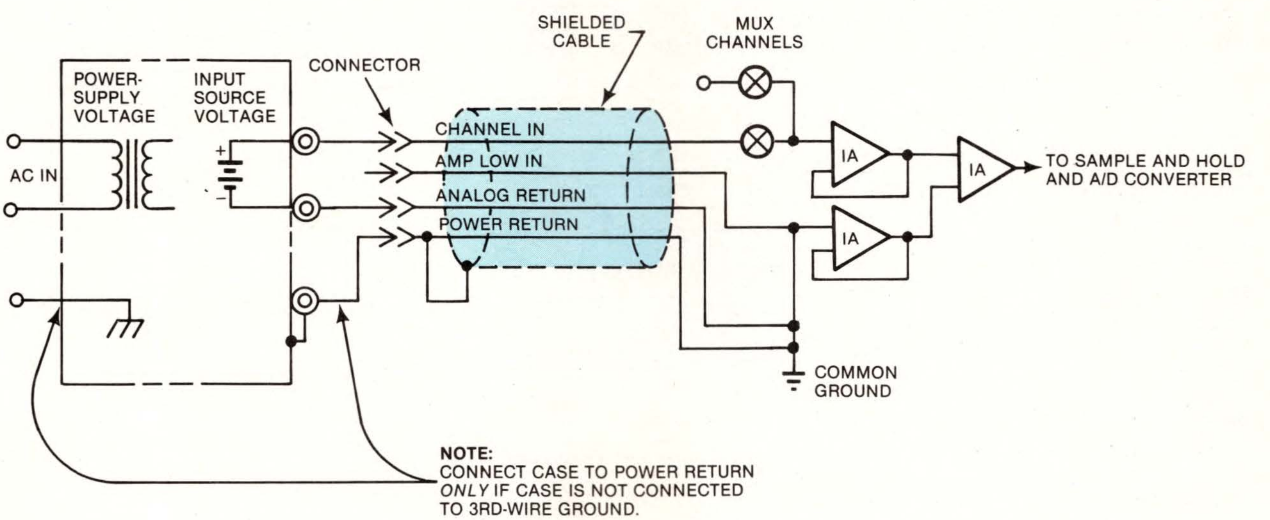


Fig 1—To prevent ground loops *in a single-ended-input MUX configuration, connect a shielded flat-ribbon cable to power return at only one point.*

Inadequate grounding tops the list of analog-input problems

varied input modes"). To minimize ground noise between this source and the MUX, use a flat-ribbon input cable with a copper mesh laminated to one side and a plastic insulating material laminated over the mesh.

The cable end that plugs into the data-acquisition system's board contains a mass-terminated connector. Solder the shield to a wire at the input end and connect this wire to the connector's power-return terminal. Then, at the system's board end, fasten the shielded cable's power-return line to common ground.

Ideally, an input source such as that depicted in **Fig 1** has isolated plus and minus output terminals and a separate case potential isolated from ac neutral. You should ground the source's case to the power-return pin to eliminate a possible power-frequency ground loop and reduce 60-Hz pickup. But if the case *must* be connected to ac neutral, don't also connect it to the power-return pin; otherwise, a ground loop develops.

When differential modes prove better

Whenever possible, do not join the input-source return to the ac neutral or to the case because this scheme forces the source to ride on any common-mode voltage differences that might exist between the A/D converter's ground and the source's ac neutral. Operating a system in this manner, however, calls for employing the pseudo- or fully differential mode (**Fig 2**). In this case, the system's integrity hinges on a differential amplifier's ability to reject common-mode signals.

In this respect, most 12-bit A/D converters provide approximately 70 dB of common-mode rejection. Thus, a 7.7V common-mode voltage results in a 1-bit error (2.4 mV) in a system configured for operation at 0 to 10V FS. These parameters indicate that either the pseudo- or fully differential mode proves better than the single-ended-MUX configuration if you question the source return's integrity.

Unfortunately, operating in either of the differential modes introduces another system constraint. For example, consider a system where the sum of the input signal and common-mode voltage cannot exceed 10.3V. If the input source is truly floating (e g, a nongrounded voltage), you must insert a resistor between the low side of the source and the analog return. Why? Because although the multiplexer presents a very high input impedance (more than 100 MΩ), a finite leakage current still flows (1 nA at 25°C or 20 nA at 60°C). Furthermore, because two input switch lines connect to the source, you must furnish a resistive path from source return to analog return to accommodate a 40-nA current.

Thus, if the source voltage is 10V FS, placing a 6.2-MΩ (max) resistor between the source's low terminal and the analog return meets the system constraint.

High source impedance produces MUX deviations

Next to grounding, the most dominant problem

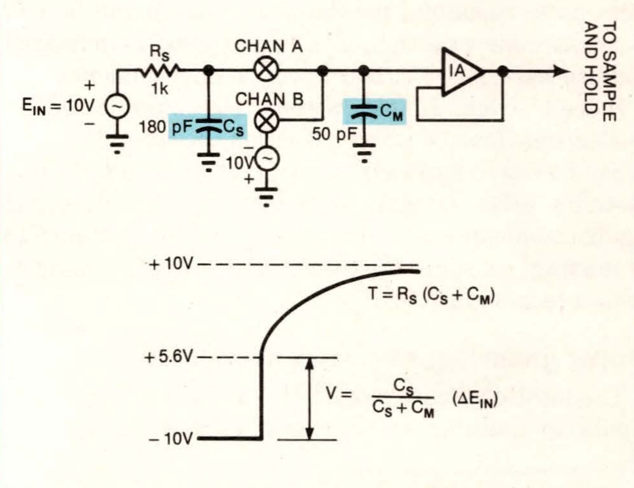


Fig 3—Stray input-cable and MUX-mode capacitances, *in conjunction with source impedance, determine the multiplexer's settling time as it switches over the full input range.*

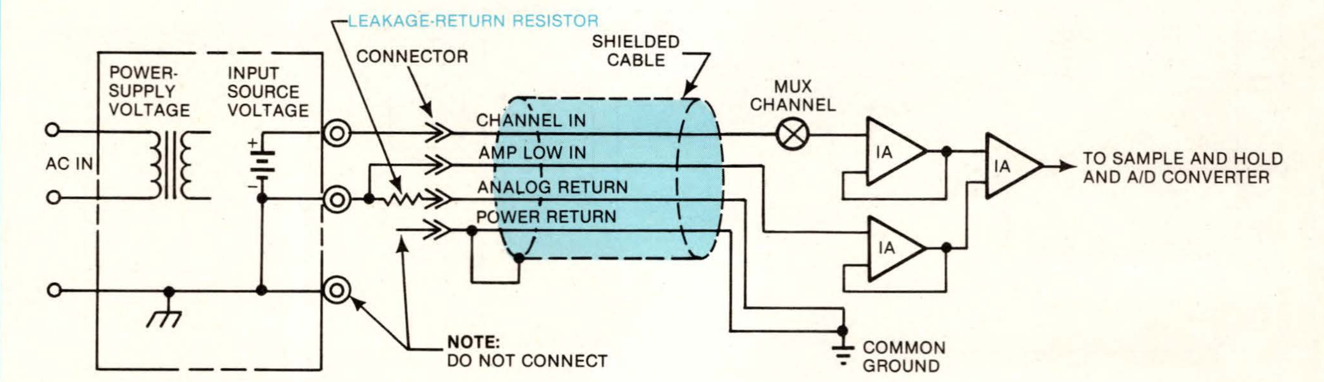


Fig 2—For a grounded input source *in either the pseudo- or fully differential MUX mode, insert a leakage-return resistor between the analog and source returns to control the common-mode voltage.*

encountered in connecting analog inputs to multiplexers involves high source impedance.

Standard data-acquisition systems connect the source to the multiplexer by means of a shielded analog cable. The multiplexer feeds a differential amplifier, which passes the signals to a programmable-gain amplifier, a S/H amplifier and an A/D converter. Generally, a word or byte transfers from the computer's memory to its multiplexer's address register concurrently with the converter's trigger signal. This trigger usually sets up a fixed delay time that allows the multiplexer and S/H amp to settle to within rated accuracy. The shunt input resistance arising from the differential amplifier imposes an impedance greater than $10^8\Omega$ on the source. However, stray capacitance can present the limiting factor governing the amount of source impedance tolerable before significant errors occur.

For worst-case considerations, assume that the multiplexer output resides at one full-scale extreme and then switches to the other extreme for several samples. The difference between the first digitized result after switching and any successive readings at the same input voltage indicates the potential problems caused by excessive source impedance.

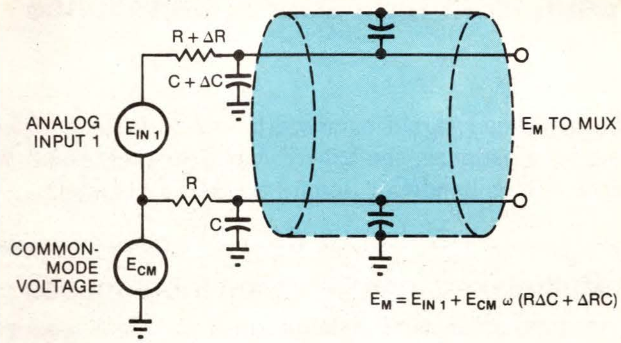


Fig 5—Microvolt- to millivolt-level multiplexing *calls for incorporating extensive shielding on the source signal lines and operating in either the pseudo- or fully differential-input MUX mode to overcome undesirable common-mode voltage.*

Fig 3 depicts this input condition. C_S is the stray capacitance to ground of all cabling from the source to the multiplexer, and C_M is the stray capacitance of the multiplexer node. Before selecting MUX channel A, assume that channel B is ON, thereby charging C_M to −10V. When channel A activates, an initial charge redistributes itself between C_S and C_M. Then both capacitors charge toward 10V with a time constant equal to the source resistance times the sum of C_S and C_M. Approximately 10 time constants later, the system has charged to within 0.01% of maximum voltage.

Assume that the cable's capacitance equals 30 pF/ft; thus, a 6-ft input cable has $C_S \approx 180$ pF. A typical value of C_M is approximately 50 pF, and assume that R_S totals 1000Ω. For these conditions, the initial redistribution causes the voltage across C_M to jump to 5.6V and then to further rise to 10V with a 230-nsec time constant. Achieving full charge requires 10 time constants or 2.3 μsec. Of course, the system's operation deteriorates if you use longer input cables or if the source impedance increases.

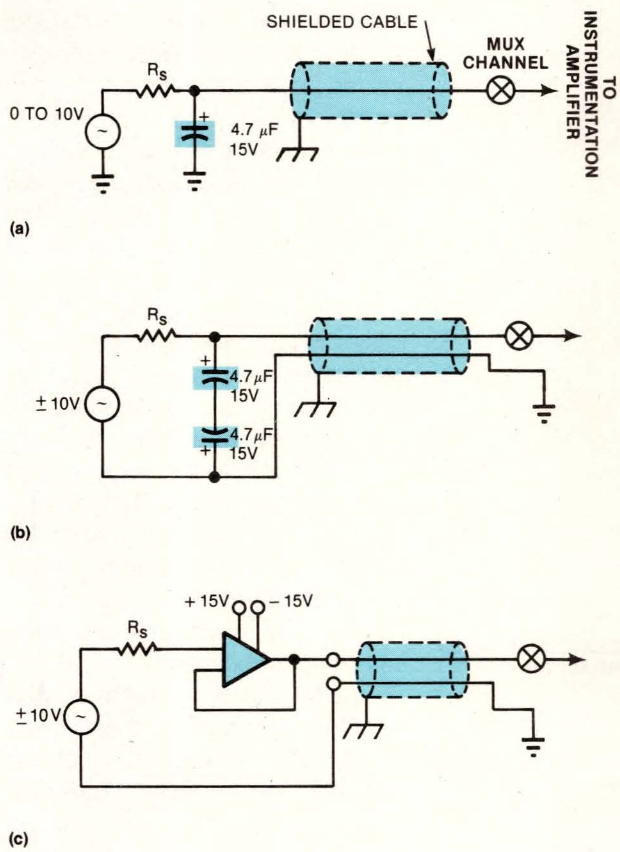


Fig 4—Properly delaying *the A/D converter's trigger after MUX-channel selection for narrow signal bandwidths involves overcoming source-impedance and stray-capacitance detriments by either connecting a 4.7-μF capacitor across a unipolar source* **(a),** *tying two 4.7-μF capacitors across a bipolar source* **(b)** *or inserting a buffer amplifier in series with a bipolar source* **(c).**

The need for a separate trigger

Certain applications call for triggering the A/D converter separately from the command that selects a multiplexer channel. Specifically, you transfer the multiplexer channel first and then (after an appropriate time delay) trigger the A/D converter.

One approach to combat source-impedance and stray capacitive effects in this case involves attaching a large capacitor across the source to reduce the effective source impedance. For unipolar sources **(Fig 4a),** a single 4.7-μF epoxy tantalum capacitor works well (bipolar sources call for placing two such capacitors in series **(Fig 4b)**). When you select a given channel, the multiplexer nodal capacitance draws its charge from the tantalum capacitor. Because this capacitor's value is so large, a negligible (~100 μV) change occurs in its voltage.

This filter-capacitor solution, of course, works only if

Multiplexer output differences result from high source impedance

the measured signal bandwidth is low. With a 10-kΩ source impedance, the 4.7-μF capacitor creates a 3-Hz filter, which bandwidth-limits the MUX channel.

Another solution to the source-impedance problem involves buffering the source impedance via a unity-gain follower amplifier **(Fig 4c)**. This approach lowers the effective source impedance seen by the multiplexer without affecting the bandwidth, but it presents difficulties in mounting parts on the data-acquisition-system pc board.

A third solution calls for increasing the amount of

Multiplexers handle varied input modes

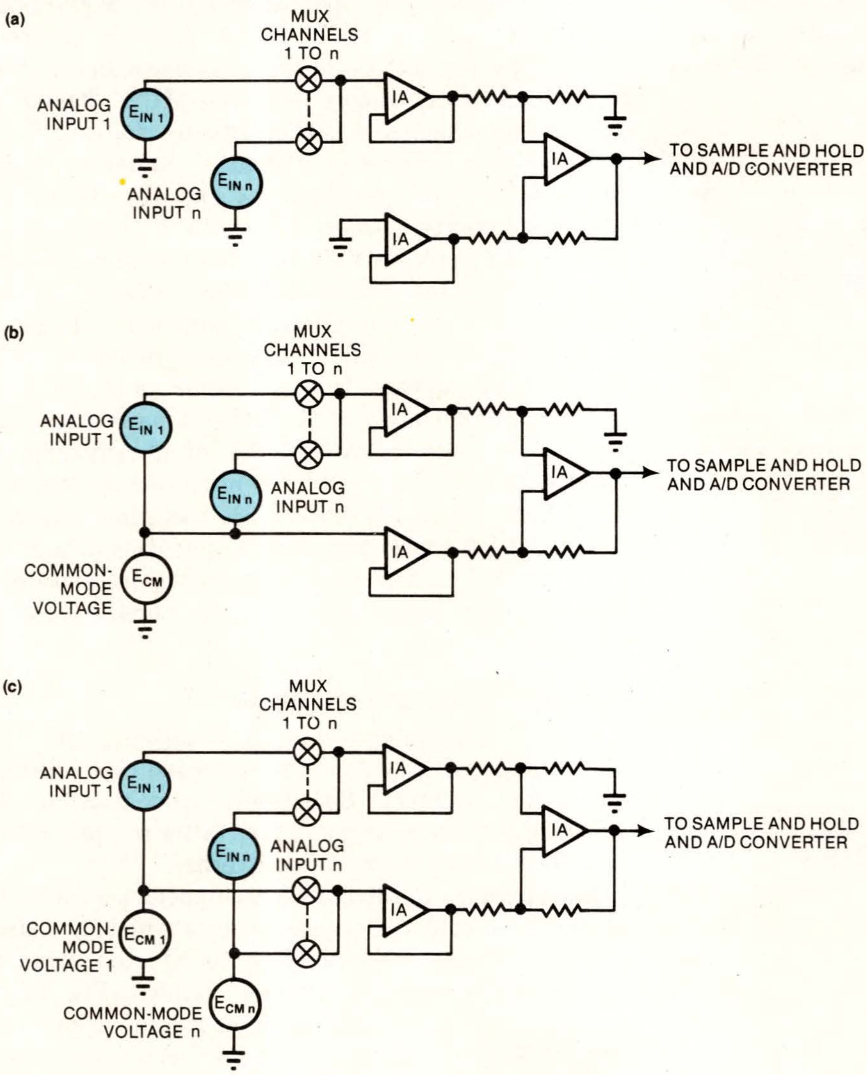
In data-acquisition systems, analog multiplexers (MUXs) scan multiple signal sources—such as the high-level (1 to 10V FS) outputs of signal-conditioning amplifiers and the direct low-level (10 to 500 mV FS) outputs of thermocouples and strain gauges—in a time - sequential manner. They then route these signals to instrumentation amplifiers for subsequent sample-and-hold and A/D-converter processing.

Because most A/D converters have single-ended inputs, such multiplexers must present them with accurate representations of the input voltages—even when the input sources are returned to a ground that resides at a potential different from that of the A/D-converter ground. The magnitude of this potential difference (common-mode voltage) usually dictates the multiplexer's input configuration **(figure).**

For example, input sources with a common return essentially at the potential of the A/D converter's common return (within ½ LSB) call for operating the MUX in the single-ended mode. A typical single-ended-mode application involves several signal-conditioning amplifiers mounted in a chassis with a common power supply. Making this approach work well involves physically locating the chassis as close as possible to the data-acquisition system.

For this same application, but in cases where the chassis must be physically remote from the system, employ the pseudodifferential configuration. This arrangement differs from the single-ended mode in that you do not directly ground the sources' common return. Thus, the system rejects any common-mode-voltage differences, yet does not sacrifice input-channel capacity.

Finally, signal sources located remotely from one another as well as from the A/D system call for operation in the fully differential mode. In this case, you connect half of the MUX channels to each side of the instrumentation amplifier. Because both sides of each input are switched, the number of multiplexer channels reduces by one-half, but each channel receives common-mode rejection.



In the single-ended MUX mode (a), *all inputs refer to the system board's analog ground. The pseudodifferential MUX mode* **(b)** *maintains the benefit of common-mode rejection and offers the same number of channels as the single-ended mode. Finally, the fully differential MUX mode* **(c)** *floats each input on a common-mode voltage but halves the number of channels.*

settling time allowed for the multiplexer. In many applications where conversion time is not critical, this approach proves the optimum choice.

Low-level multiplexing demands thorough design

Many transducers generate microvolt and millivolt outputs, which resist direct handling by standard high-level multiplexers. To complicate this additional multiplexer-design problem, these transducers generally operate in harsh environments that superimpose these low levels upon large common-mode voltages.

For low-level, high-bandwidth transducers (such as accelerometers), the solution lies in the use of a signal-conditioning amplifier for each channel and in multiplexing the resultant higher levels. However, for low-level, low-bandwidth transducers (such as load cells, strain gauges and thermocouples), direct signal multiplexing requires only one high-gain amplifier to serve all MUX channels in front of the A/D converter.

Low-level multiplexing produces significant reductions in cost as well as power and space requirements, and input filtering rejects unwanted signals on each channel. As another advantage, you can program the multiplexer output amplifier's gain to control the system's characteristics on a channel-to-channel basis.

But because of the extremely low signal levels involved, handling a transducer's direct output requires careful design to prevent source-signal contamination by extraneous power-line and RFI noise. For example, you must configure source signals in a differential-MUX mode and shield the signal wires to minimize pickup and preserve data integrity.

Fig 5 illustrates the input-cabling method required to bring true low-level signals to an A/D system. The E_{CM} term represents the difference in grounds or common-mode voltage. Resistors R and $R+\Delta R$ represent an unbalanced source resistance, arising from the difference in lead resistivity of thermocouple extension wires or from an unbalanced condition in a bridge circuit.

The unbalanced capacitance to ground is indicated by C and $C+\Delta C$. Because the shield connects to the low side of the input source (and to the common-mode voltage), capacitance from either input lead to shield doesn't affect system operation. However, leakage capacitance to ground does.

The unbalanced impedances in the input lines convert common-mode voltages into normal-mode noise, which then becomes difficult to separate from the true signals. For high source resistance (and its resultant imbalance), the capacitance between each input line and ground increases the problem's severity.

Calculate CMRR

The equation in **Fig 5** states that the system's input voltage (E_{IN}) equals the signal (E_S) plus an unwanted component proportional to the value and frequency of the common-mode voltage and the sum of the unbalanced input time constants. Optimum system design calls for making the second term approach zero.

The system's ability to reject the unwanted common-mode voltage is measured by the common-mode rejection ratio (CMRR):

$$CMRR=20\log_{10}[(CMV/E_{OUT})/A]\ dB$$

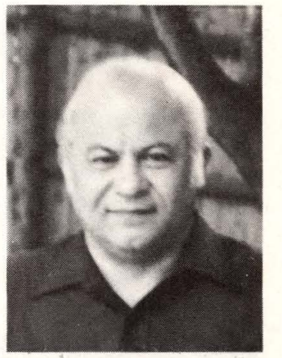
where CMV is the common-mode voltage, E_{OUT} is the change in the amplifier output voltage arising from this common-mode voltage and A is the amplifier gain.

Assume that a 1-kΩ source imbalance exists and that the common-mode frequency equals 60 Hz. Thus, only 3 pF of unbalanced stray capacitance causes the CMRR to deteriorate below 120 dB. Keeping stray capacitance below this level usually requires sophisticated and expensive double-shielding techniques. One low-level multiplexing technique useful in such cases switches three lines for each input; e g, two signal lines plus the shield.

Because stray capacitance to ground creates problems, you should connect the system's shield to the source of the common-mode voltage, then tie the switched shield to a guard surrounding the input amplifier. If the common-mode voltage is approximately 10V or less, this approach works well with solid-state switches and a differential-in, single-ended-out input amplifier. However, if the common-mode voltage reaches several hundred volts, the approach becomes extremely difficult and expensive to implement.

A simpler and more effective method of eliminating the common-mode-voltage effect for large values of CMV utilizes a flying - capacitor - type multiplexer (EDN, May 20, 1979, pg 169). Besides doing away with common-mode voltage from the input signals, the flying capacitor provides a low ac impedance across the source terminals, thereby reducing the effects of source resistance and resistive imbalance. Therefore, the system's common-mode rejection approximately equals the ratio of the flying-capacitor value to that of the stray capacitance to ground. **EDN**

Author's biography



James V DiRocco is president of ADAC Corp, Woburn, MA, which he cofounded 5 yrs ago. He previously served as president and vice president for engineering at Analogic Corp. The recipient of five patent grants, Mr DiRocco holds BSEE and MSEE degrees from Northeastern University and maintains memberships in the IEEE and ISA. His hobbies include sailing and traveling.

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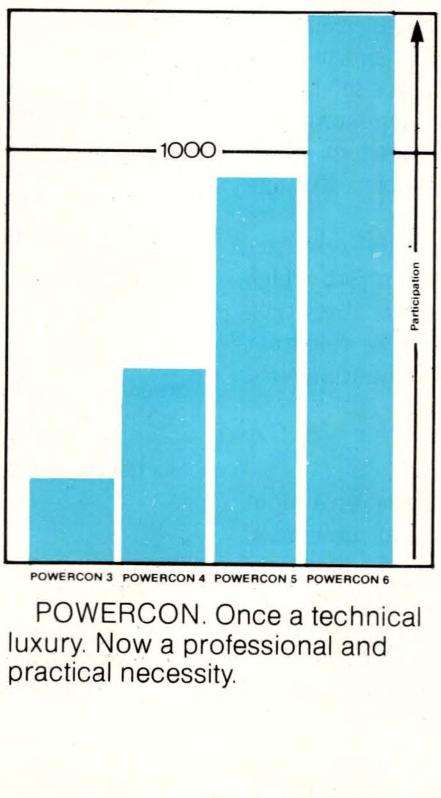

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5	60	150	300		
12	25	60	120	85	
15	25	50	100	70	
24	16	33	66	45	
28	13	27	54	40	
48	8	16	32	24	
CASE SIZE:	5"x8"x11"		5"x16"x11"	5"x8"x15"	5"x8"x11"

MULTIPLE OUTPUT MODELS

AC INPUT(3)		PM2675A	PM2676A	PM2677A	PM2678A	PM2679
DC INPUT(4)		PM2775(4)	PM2776(5)	PM2777(6)	PM2778(7)	
MAX. TOTAL OUTPUT		375W	600W	750W	850W	1000W
MAIN CHANNEL	OUTPUT VOLTS	2, 3, 5, 12, 15, 18, 21, 24, 28, 48VDC				
	MAX. POWER	250W	500W	600W	750W	875W
2nd & 3rd CHANNEL	OUTPUT VOLTS	5, 12, 15, 18, 21, 24, 28VDC				
	OUTPUT CURRENT	10	10	10	Check Factory	
4th CHANNEL	OUTPUT VOLTS	5, 12, 15, 18, 21, 24, 28VDC				
	OUTPUT CURRENT	4	4	4	4	4
CASE SIZE:		5"x8"x11"		5"x8"x12 9/16"		5"x8"x15"

SINGLE OUTPUT
1) 92 to 138 or 184 to 250 VRMS single input
2) 24 (to 375 Watts), 48, 120 or 240 VDC
MULTIPLE OUTPUT
3) 92 to 138 or 184 to 250 VRMS single input.
4) 24 (to 375 watts) 48, 120 or 240 VDC.
5) 48, 120, 240 VDC
6) 120, 240 VDC
7) 120, 240 VDC.

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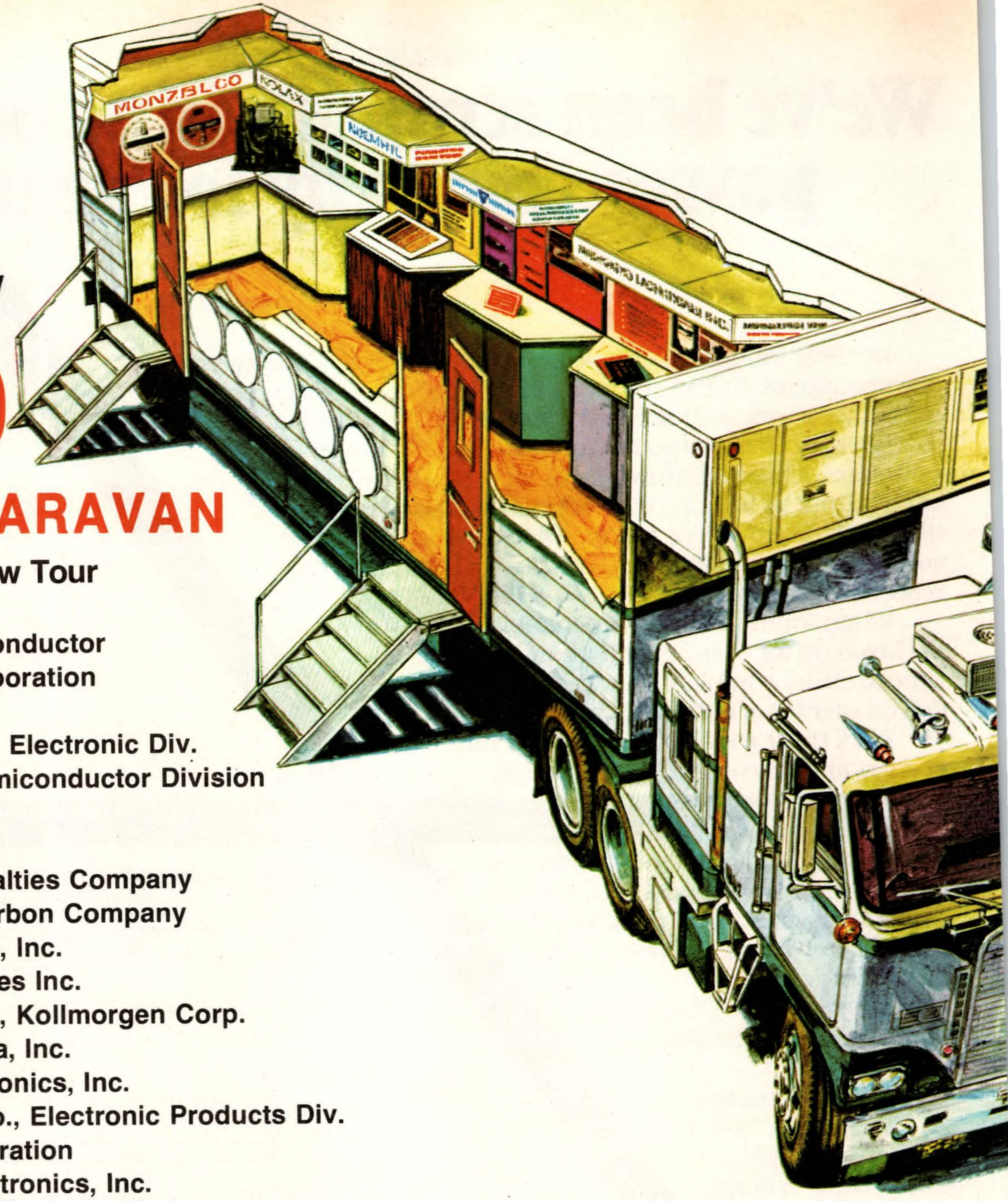

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Eastern Show Tour

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Mupac Corporation
Methode Electronics, Inc.
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Please check the itinerary for the date we visit you.

1980 EDN CARAVAN ELECTRONIC SHOW TOUR
February 18 to March 18 (first half)

DATE		TIME	SITE
2/18 AM	Monday	9-11	COULTER ELECTRONICS 590 W. 20th St, Hialeah, FL
* 2/18 PM	Monday	1-2:30	SYSTEMS ENGINEERING LABS 1800 NW 66th Av. Plantation, FL
2/18 PM	Monday	3:15-4:30	HARRIS COMPUTER SYSTEMS 2101 W. Cypress Creek Rd, Ft. Lauderdale, FL
* 2/19 AM	Tuesday	8:30-11	IBM CORPORATION 2000 NW 51st St, Boca Raton, FL
2/19 PM	Tuesday	1-2:30	MODULAR COMPUTER SYSTEMS 3101 SW 12th St, Pompano Beach, FL
2/19 PM	Tuesday	3-4:30	BENDIX CORPORATION 2100 NW 62nd St, Ft. Louderdale, FL
* 2/20 AM	Wednesday	8:30-12	HARRIS ELECTRONIC SYSTEMS PALM Bay Rd, Palm Bay, FL
2/20 PM	Wednesday	2-4	STROMBERG-CARLSON 1291 N Hwy 17/92, Longwood, FL
* 2/21 AM	Thursday	9-11:30	E-SYSTEMS, ELECTRONIC COMMUNICATIONS INC. 1501 72nd St, N, St. Petersburg, FL
2/21 PM	Thursday	1:30-4	HONEYWELL, INC. 13350 Hwy 19, St. Petersburg, FL
* 2/22 AM	Friday	8:30-11	MARTIN MARIETTA AEROSPACE E Sand Lake Rd, Orlando, FL
* 2/22 PM	Friday	2-4	GENERAL ELECTRIC CO. 1800 Volusia Av, Daytona Beach, FL
2/25 AM	Monday	8:30-10	CHRYSLER CORP., ELECTRONICS DIV. 102 Wynn Dr, Huntsville, AL
2/25 AM	Monday	11-12	UNIVERSAL DATA SYSTEMS 4900 Bradford Dr, Huntsville, AL
2/25 PM	Monday	2-4	SCI SYSTEMS, INC. 8600 S Memorial Prkwy, Huntsville, AL
2/26 AM	Tuesday	8:30-10 11-12	SCIENTIFIC-ATLANTA INC. 3845 Pleasantdale Rd, Doraville, GA 4386 Park Dr, Norcross, GA
2/27 AM	Wednesday	9-11	NCR CORPORATION 3325 Platt Springs Rd, W Columbia, SC
* 2/28 AM	Thursday	8:30-11:30	IBM CORPORATION Research Triangle Park, Durham, NC
PM		1-2	2520 North Blvd, Raleigh, NC
2/28 PM	Thursday	3-4:30	ITT TELECOMMUNICATIONS 2912 Wake Forest Rd, Raleigh, NC
2/29 AM	Friday	8-9	WESTERN ELECTRIC CO. 204 N Graham Hopedale Rd, Burlington, NC
* 2/29 AM	Friday	10-11:30	WESTERN ELECTRIC CO. Mt. Hope Church Rd, McLeansville, NC
* 2/29 PM	Friday	2-4	WESTERN ELECTRIC CO. 3300 Lexington Rd, Winston-Salem, NC
* 3/3 AM	Monday	8:30-9:30	ITT NORTH ELECTRIC CO. Gray Station, Johnson City, TN
3/3 AM	Monday	10:30-12	TEXAS INSTRUMENTS INC. 1923 Erwin Hwy, Johnson City, TN
3/3 PM	Monday	2-4	SPERRY UNIVAC Univac Rd, Bristol, TN
3/4 AM	Tuesday	9-11:30	GENERAL ELECTRIC CO. 1501 Roanoke Blvd, Salem, VA
3/4 PM	Tuesday	2-4:30	GENERAL ELECTRIC CO. Mountainview Rd, Lynchburg, VA
3/5 AM	Wednesday	9-11	GENERAL ELECTRIC CO. G. E. Dr, Waynesboro, NC
* 3/5 PM	Wednesday	1-2:30	SPERRY MARINE SYSTEMS Rt 29 N, Charlottesville, VA
3/5 PM	Wednesday	3:15-4:30	GENERAL ELECTRIC CO. 865 Rio Rd, Charlottesville, VA
3/6 AM	Thursday	8:30-11	IBM CORPORATION 9500 Godwin Dr, Manassas, VA
3/6 PM	Thursday	12:30-2	E-SYSTEMS MELPAR 7700 Arlongton Blvd, Falls Church, VA
3/6 PM	Thursday	3-4:30	LITTON SYSTEMS, AMECOM DIV. 5115 Calvert Rd, College Park, MD
3/7 AM	Friday	8:30-9:30	IBM CORPORATION 18100 Frederick Pike, Gaithersburg, MD
3/7 AM	Friday	10:30-12	BENDIX CORPORATION E Joppa Rd, Baltimore, MD
3/7 PM	Friday	2-4	WESTINGHOUSE ELECTRIC CO. 1111 Schilling Rd, Hunt Valley, MD
* 3/10 AM	Monday	9-11:30	RCA CORPORATION Front & Cooper St, Camden, NJ
3/10 PM	Monday	2-4	RCA CORPORATION Marne Hwy, Moorestown, NJ
* 3/11 AM	Tuesday	8:30-9:45	BURROUGHS CORPORATION Boot Rd, Downingtown, PA
3/11 AM	Tuesday	10:30-12	BURROUGHS CORPORATION, CSG Swedesford Rd, Paoli, PA
* 3/11 PM	Tuesday	2-4	HONEYWELL INC. 1100 Virginia Dr, Ft. Washington, PA
* 3/12 AM	Wednesday	8:30-12	LEEDS & NORTHRUP CO. Sumneytown Pike, N Wales, PA
3/12 PM	Wednesday	2-4:30	SPERRY UNIVAC Union & Jolly Rd, BlueBell, PA
* 3/13 AM	Thursday	9-11	FISCHER & PORTER CO. 125 E County Line Rd, Warminster, PA
3/13 PM	Thursday	1:30-4:30	BELL LABORATORIES Holmdel & Roberts Rd, Holmdel, NJ
* 3/14 AM	Friday	9-11:30	LOCKHEED ELECTRONICS CO. US Hwy 22, Plainfield, NJ
* 3/14 PM	Friday	1:30-4	BELL LABORATORIES 600 Mountain Av, Murray Hill, NJ
* 3/17 AM	Monday	9-11:30	BENDIX CORPORATION Rt 46, Teterboro, NJ
3/17 PM	Monday	1-2:45	ITT AVIONICS 390 Washington Av, Nutley, NJ
3/17 PM	Monday	3:15-4:30	ITT DEFENSE COMMUNICATIONS 492 River Rd, Nutley, NJ
* 3/18 AM	Tuesday	9-12	SINGER KEARFOTT DIV. 150 Totowa Rd, Wayne, NJ
* 3/18 PM	Tuesday	1:30-4:30	BELL LABORATORIES Whippany Rd, Whippany, NJ

* Indicates site closed to outside visitors. Exhibitor personnel only

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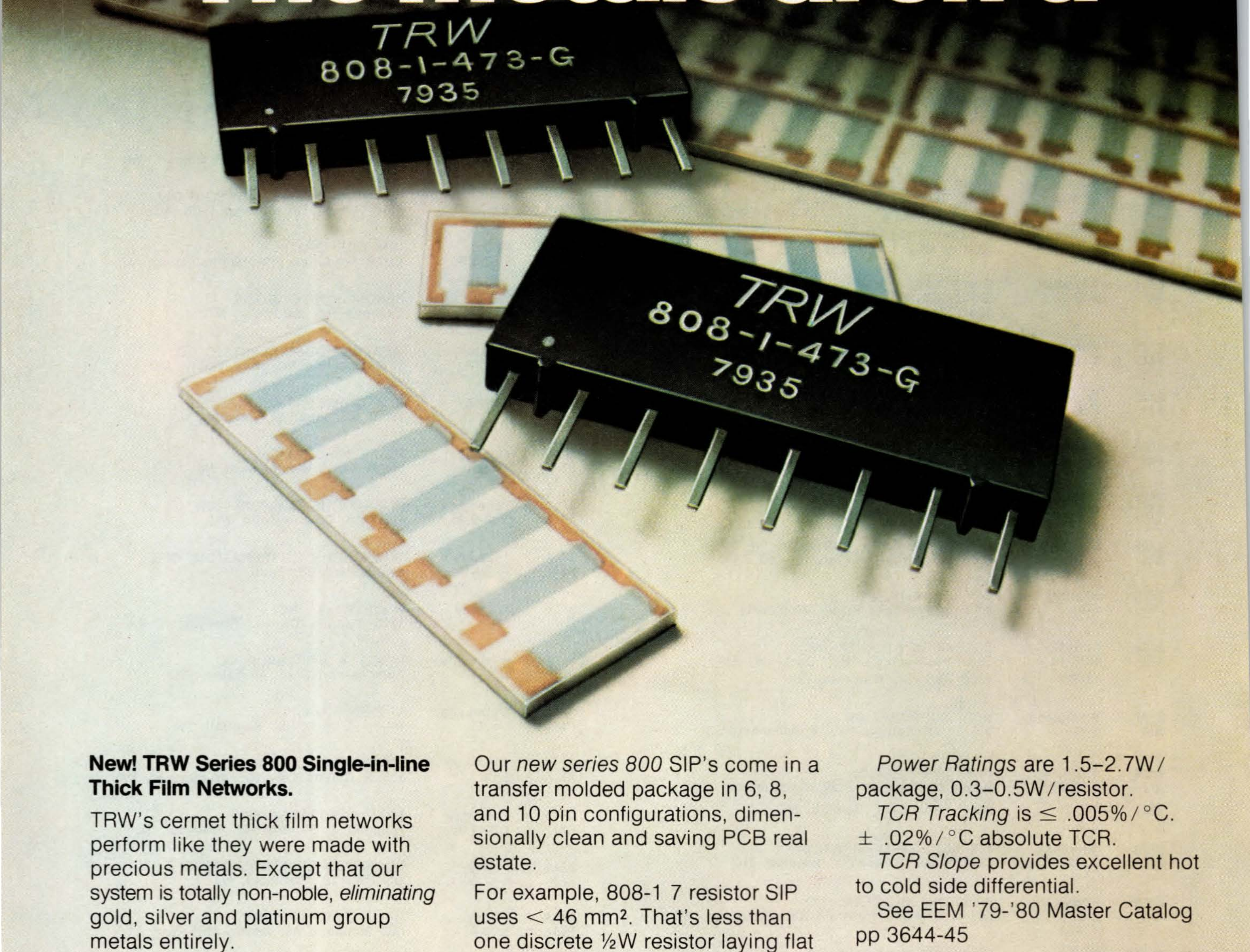

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For more information, Circle No 85

Simple alarm saves both engine and battery

Larry Smeins
Hewlett-Packard Co, Loveland, CO

The Design Idea "Reminder Circuit Saves Car Batteries" (September 20, 1979, pg 138) can easily be expanded to not only warn when lights are left on but also of engine overheating, a broken fan belt, loss of oil pressure and other conditions usually flagged by warning lights.

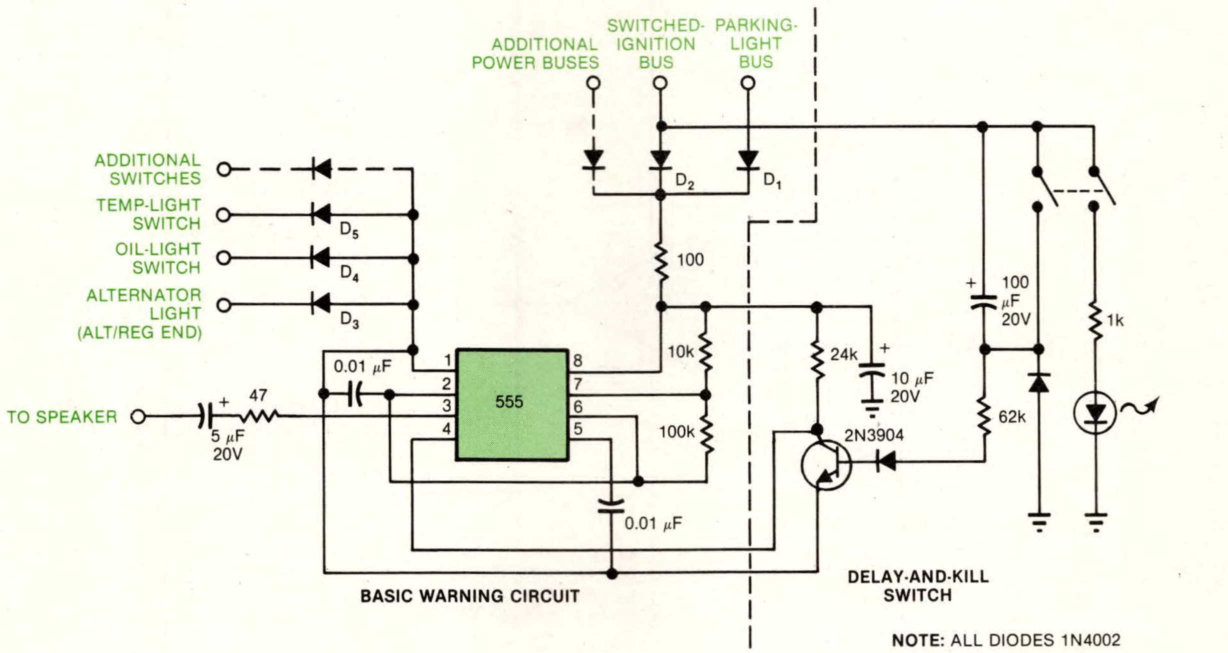
The basic circuit, as in the original, utilizes a 555 in a multivibrator configuration; however, the power busing is rearranged to sense the additional fault conditions. Additionally, the ground or low-level side of the circuit is no longer connected to the ignition bus; rather, it's diode ORed to the fault conditions indicated by closures to ground, i e, oil pressure, temperature, alternator, etc. (The alternator light senses the difference between the battery and alternator output, providing the effect of a switch closure when the alternator is inoperative.) The high-level side of the circuit is diode ORed to the parking-light bus and the switched-ignition bus.

During normal engine operation, positive power goes to the circuit from the ignition bus via D_2. Ground to the circuit is supplied via D_3, D_4 or D_5 when a fault occurs, thus producing a loud buzz. If the lights are on with the ignition off, positive power is supplied via D_1 from the parking-light bus, and ground is supplied via D_4 and D_3 by the oil-pressure switch and alternator, both of which are normally low when the engine is not running.

A delay added to the 555's reset pin allows 10 to 20 sec for starting the engine before the alarm is activated. And an added kill switch permits servicing the automobile without the annoyance of the warning buzzer; an LED indicator comes on when this switch is activated to warn that the system is inoperative.

Additional warning functions can be sensed by adding more diodes to either the high or low side of the circuit, depending on the nature of the sensed fault. **EDN**

To Vote For This Design, Circle No 450



Save your car battery and engine *with this expanded alarm circuit. Diode ORing monitors the headlights and idiot lights and signals faults through the radio speaker.*

Duty-cycle converter doubles frequency

Robert A Pease
National Semiconductor, Santa Clara, CA

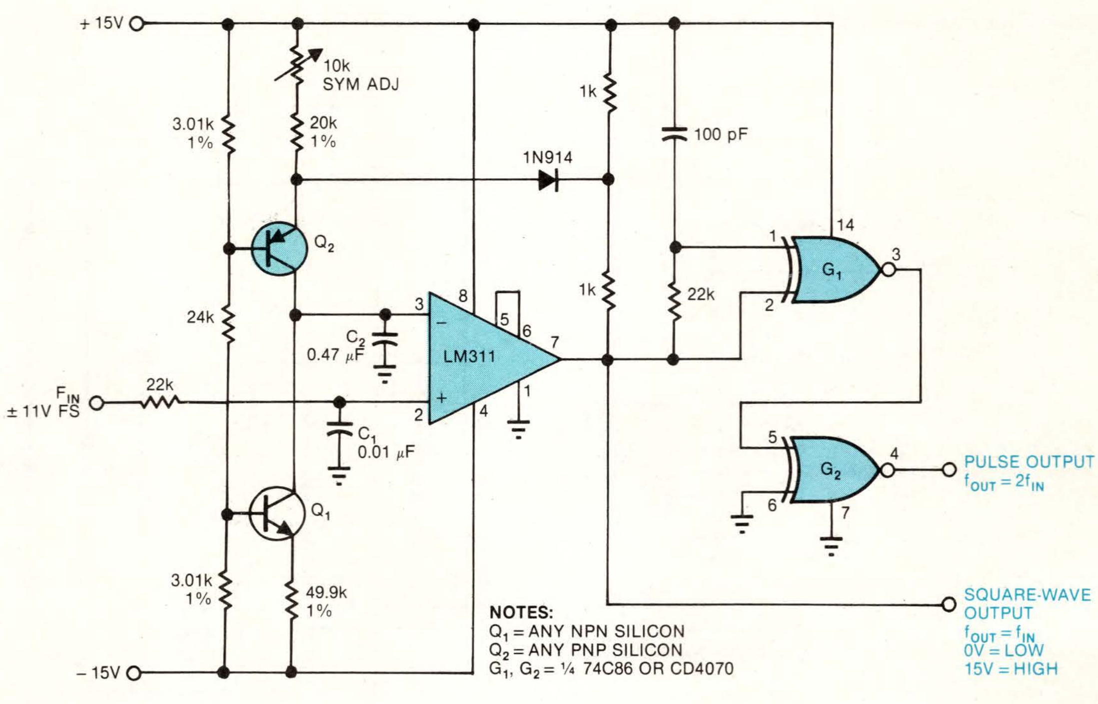
A square wave of frequency f can be converted to a pulse train of frequency 2f by means of an exclusive-OR gate. But a *pulse train* of a given frequency cannot normally be converted to one of a higher frequency because there is no way to predict when a pulse should occur. The circuit described here, however, can convert any pulse train or sine or square wave to a precise 50.0%-duty-cycle square wave. This square wave can then be converted to a pulse train of twice the frequency. And the process can repeat to provide pulses at quadruple or higher frequencies.

As shown in the **figure,** the LM311's output at pin 7, fed through resistors and a diode, turns Q_2 on and off. The duty cycle at pin 7 depends on the relative values of the average voltage at pin 3 and the nominal triangle wave at pin 2. Thus, if the duty cycle is too low, Q_2 stays OFF for a longer time, and the voltage at pin 3 falls until the duty cycle becomes 50%. Resistor R_1, a fine-adjustment pot, trims the collector current of Q_2 to a value double that of Q_1, thereby acting as a duty-cycle trimmer.

In practice, the duty cycle of the pin 7 output varies no more than ±0.01% from 50.0% as the input frequency changes by a factor of 10 or as the input duty cycle changes from 10 to 90%. The pin 7 output—a precise square wave—can be used directly and can also go to an MM74C86 or CD4070 XOR, which puts out a pulse train of frequency $f_{OUT}=2f_{IN}$. The second section of the XOR merely sharpens the output rise times.

The component values in this circuit are not too critical, but stability of the resistors labeled 1% is necessary to achieve good duty-cycle stability. Of course, if the collector current of Q_2 is n times larger than that of Q_1, the output duty cycle is 1/n; thus, you can choose duty cycles of 10%, 25% or other values.

For the circuit values shown, the output responds accurately (when $V_{IN}=15V$ p-p) over a frequency range of 200 Hz to 200 kHz when the input duty cycle lies between 40 and 60%. When the input duty cycle is between 10 and 90%, frequency spans 800 Hz to 100 kHz for the same V_{IN}. To accommodate higher



Accommodating a wide range of input-duty-cycle pulses, *the LM311 voltage comparator controls a current source (Q_2) to establish a symmetrical square wave, which the XOR gate then frequency-doubles.*

frequencies, you can reduce C_1 and C_2's values; for lower frequency ranges, increase them.

In general, the ratio of the widest input pulse width at low frequency to the narrowest input pulse width at short duty cycles and high frequency should not exceed to 1000:1 for best results. The input signal can have any nominal level, but for the widest frequency range, make it large (20V p-p is better than 3V p-p). **EDN**

To Vote For This Design, Circle No 451

Accurately count async-gated clock pulses

Marian Stofka
Bratislava, Czechoslovakia

Errors can occur when counting asynchronously gated free-running clock pulses with cascaded synchronous 4-bit IC counters—particularly when the gating signal terminates so as to narrow the input pulse to a value below that required to reliably trigger the counters (**Fig 1**).

A pulse applied to a counter system's input when several of the system's least significant 4-bit IC counters are in their maximum states causes a ripple-carry pulse to propagate through the ICs. The carry pulse—whose width is determined by the clock pulse—causes successive state transitions from maximum to zero in the least significant counters, while incrementing by one the state of the first, more significant counter (previously in a nonmaximum state). However, if the applied input pulse is less than the minimum (critical) width, the correct state transition might not result.

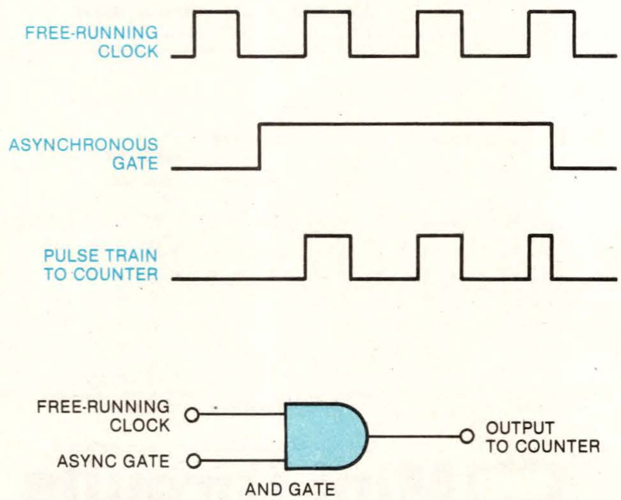


Fig 1—This gating circuit *can truncate the last pulse and cause cascaded synchronous counters to miss a beat: The ripple carry might not propagate through all of the counters before the shortened pulse disappears.*

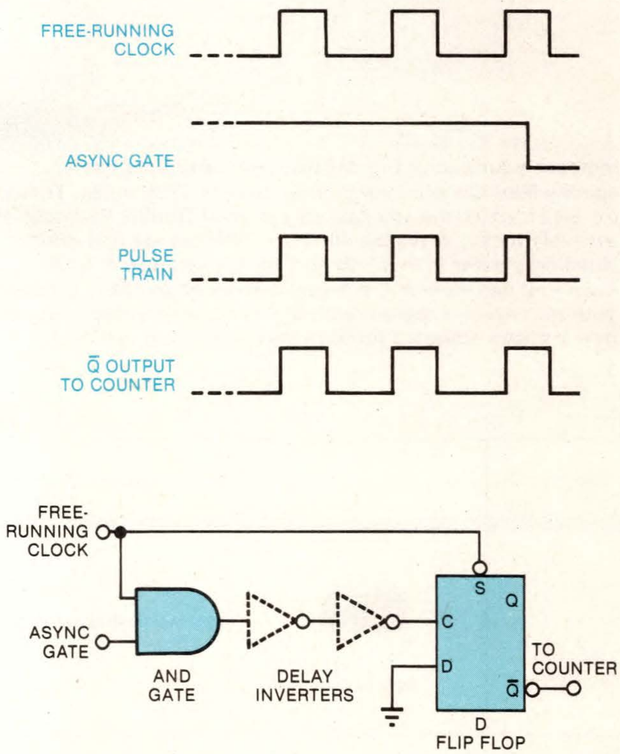


Fig 2—A single D flip flop *restores the last pulse to its original width. Additional circuit delay might be required if the flip flop recovers faster than the AND gate.*

For example: In a hex-decade BCD counter, a false transition with result 009XXX might occur instead of the correct 999XXX→000(X+1)XX. (Here, each character denotes a state of the corresponding 4-bit IC counter, and X denotes a number other than nine.) The states of the two least significant counters have changed as desired, but those of the third and fourth counters have not—the carry has frozen in. The maximum error appears if a counter with the state 99..9X receives an input pulse of the critical width and changes state to 00..0X instead of the

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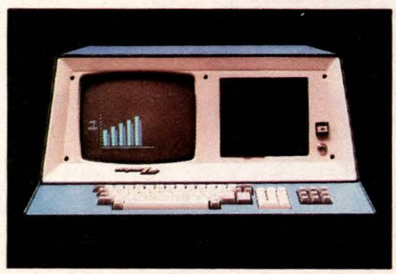

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For more information, Circle No 88

proper 00..0(X+1). The resulting error—10^{n-1} for an n-decade counter—is indeed large.

A similar problem arises in down counting—if the counter is reversible. In this case, a borrow pulse must propagate through the least significant counters if they have previously stored a zero state and a pulse has been applied to the down - counting input. Instead of the expected transition (000YYY→ 999(Y−1)YY, for example) a false one could be observed: 999YYY (Y is a nonzero number). Here, the maximum possible error is 1/10 the capacity of the BCD counter. With a synchronous binary counter, an error as large as 1/16 of counter capacity is possible.

The primary cause of error—the truncation of the last-in pulse—can be prevented by means of the simple circuitry shown in **Fig 2.** The added hardware replicates the pulse train (which is gated as before) and restores the width of the last-in pulse to its original value. The D flip flop is clocked to ZERO by the leading, positive-going edge of each pulse in the gated train and preset to ONE by the LOW interpulse level of the free-running clock pulses. The result is a glitch-free output. For proper circuit operation, the flip flop's preset recovery time must be less than the propagation delay of the AND gate. If it isn't, increase the delay by adding a pair of inverters. **EDN**

To Vote For This Design, Circle No 452

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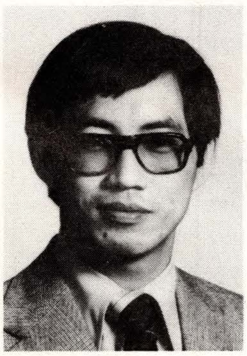

Ban Shin Bong cowinner of the January 5, 1979 US Savings Bond Award. His winning design is "Comparator provides μP power-up." Mr Bong is with Collins GTG, Rockwell International, Cedar Rapids, IA.

Lt Glenn Prescott cowinner of the January 5, 1979 US Savings Bond Award. His winning design is "MOSFETs convert triangles to sine waves." Lt Prescott is with the Air Force Communication Department at Scott AFB, IL.

Design Entry Blank

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ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 Min.	11 Typ.	+38 Typ.	+24V	0.6A	**199.00**	**(1.9)**
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Total safe input power +20 dBm, operating temperature 0° C to +60° C, storage temperature −55° C to +100° C, 50 ohm impedance, input and output VSWR 2:1 max. For detailed specs and curves, refer to 1979/80 MicroWaves Product Data Directory, p. 364-365 or EEM p. 2970-2971.

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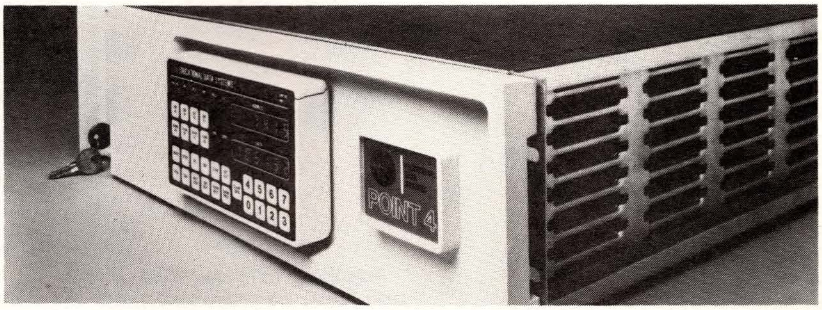
Feature Products

Computers' operator control panel increases their application flexibility

Meeting their manufacturer's goal of producing easier-to-use computers, units in the Point 4 minicomputer series can incorporate a control panel that offers:

- Removability (the panel can be used as a hand-held unit)
- Provision of all the displays and switches necessary to monitor the processor (including two octal displays for address and data and eight LEDs that show processor status)
- Memory examination and access capability
- An Automatic Program-Load switch.

The front panel is thus a key option for the minicomputers, providing systems houses with an important tool to employ when preparing systems for end users.



A detachable control panel *puts all the Point 4 minicomputer's necessary system controls—including Automatic Program Load—at operators' fingertips.*

Indeed, options such as the operator panel are more the rule than the exception with Point 4 machines. Such features as the IRIS operating system, battery backup and an interprocessor bus also contribute to the units' flexibility.

And in addition to flexibility benefits, these 16-bit machines also furnish performance advantages. For example, they perform a complete arithmetic or branch instruction in only 400 nsec—faster than DEC's PDP-11/45 or Data General's Eclipse, according to the manufacturer.

This speed is important, the company feels, because it provides systems houses with a more powerful machine for two-thirds the price of similar minis. Less than $5000 in a minimal configuration.

Educational Data Systems, 1682 Langley Ave, Irvine, CA 92714. Phone (714) 556-4242.
Circle No 456

Cartridge-disc-drive controller suits personal-computer systems

Although the Apple and TRS-80 are primarily intended for personal computing, you can also adapt them to business use by adding mass-storage capability. The DC-500 cartridge-drive controller allows you to accomplish this adaptation by interfacing to such popular hard-disc drives as Control Data Corp's Hawk or Ampex's DM-448.

With industry interest currently focused on 8-in. Winchesters, why choose a cartridge drive? The controller's manufacturer feels that a removable storage medium is the key: Business systems must provide "grandfather" capabilities (some means of permanently storing computerized data), and tape storage sometimes can't meet this need.

No need for modifications

The AMD 2910-based DC-500 acts as an intelligent interface that responds to commands from a host CPU. To accomplish this function, however, it must attach to the computer's bus in some manner.

To avoid modifying the computer's bus structure—an especially important consideration for Apple and Radio Shack systems—the controller utilizes adapters that bring out the necessary signals through existing ports. The Apple adapter connects to an open slot on the system's mother board, and the

Feature Products

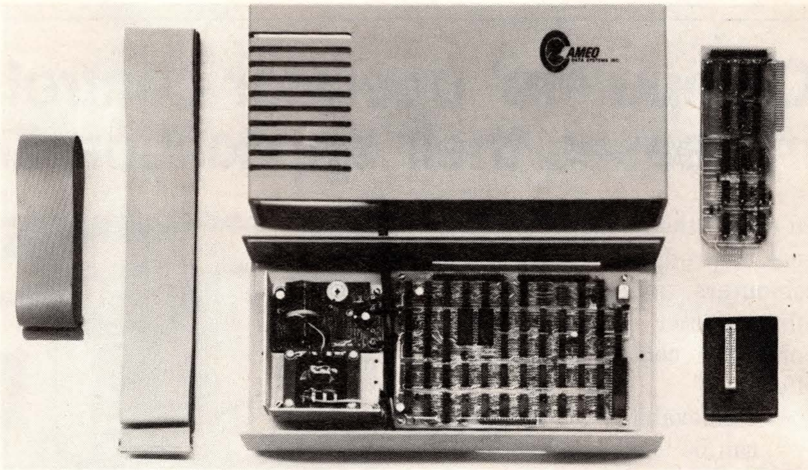
TRS-80 device plugs into the port designed for the μC's screen printer.

DMA functions

In operation, the DC-500's intelligence allows you to sequence commands from the computer to the drive. When the interface is advised that it has control of the data bus, it can read and write data directly to and from memory in DMA-type operations.

The controller incorporates a 512-byte data buffer with look-ahead capabilities that permit one transfer to continue while preparing the next 512-byte block. $1500 for controller and one adapter (OEM discounts available). Delivery, 45 days ARO.

(Special business software is also available for TRS-80 systems employing the controller. Contact LaSalle Computing Inc, Box 116, Blue Bell, PA 19422; phone (215) 825-5524. This software exploits the storage available on the hard-disc system, providing full-screen editing and fill-in-format functions.)



Adapting cartridge-disc drives to personal computers *(Apple and TRS-80 systems) via plug-in adapters, the Cameo Data Systems DC-500 controller allows these systems to serve business applications.*

Cameo Data Systems Inc, 1626 Clementine, Anaheim, CA 92802. Phone (714) 535-1682.

Circle No 457

Your Marketing department wants a new black box design. They want it to handle 37 bytes of information. It has to be solar energized. It has to fly. It has to speak. It has to reproduce. Naturally, it'll need special cable configurations. Call Belden.

We've developed workable wire, cable and cord answers for a lot of extraordinary new products. In fact, a lot of designers have found that working with Belden in the early stages of a design project usually pays dividends in compatibility, workability and lower overall costs.

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Just imagine a wire, cable or cord—and we'll come through with it. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374; 317-966-6661. Out West, contact our Regional Sales Office in Irvine, CA at 714-833-7700. 8-7-9B

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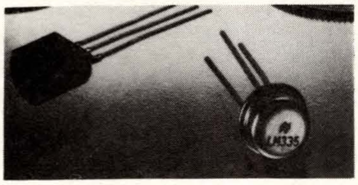
New Products

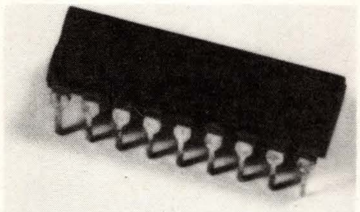
ICs & SEMI-CONDUCTORS



TEMPERATURE SENSORS. Capable of directly reading out temperature in degrees Kelvin, LM135 Series monolithic ICs are accurate to within 1°C and operate over a −55 to +200°C range. They provide 10 mV/°K output, and require only two wires for operation, minimizing wiring to remote locations. The units are available with initial accuracies of ±1, ±3 and ±6°C, but by adding a pot you can easily calibrate them to better than 1°C accuracy.

Suitable for heating and cooling control and for instrumentation and automotive applications, the sensors act as shunt regulators with the output voltage proportional to temperature. At 25°C or 298°K, the voltage is 2.98V; operating current can range from 0.5 to 5 mA with no change in electrical performance.

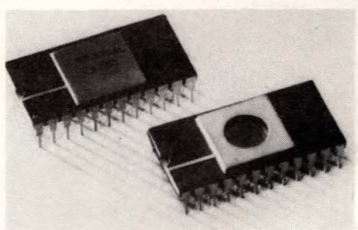
LM135 comes in a hermetic TO-46 package; the commercial version, LM335, comes in a TO-46 or TO-92 plastic package. LM335, $0.95 (100). **National Semiconductor,** 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 737-5856. **Circle No 221**



MULTIPLYING DACs. MP7530 and -7533 10-bit and -7531 12-bit monolithic devices are second-source replacements for the AD7530, AD7531 and AD7533. The 16-pin-DIP -7530 and the 18-pin-DIP -7531 are DTL/TTL/CMOS compatible, have a nonlinearity TC of 2 ppm of FSR/°C and 20-mW power dissipation (including the ladder network). Typical applications for the -7530 and -7531 include digital/analog multiplication, CRT-character generation and programmable power supplies; uses for the -7533 include digitally controlled attenuators and programmable-gain amplifiers. MP7530JN or MP7531JN, $7.90; MP7533JN, $5.80 (100). **Micro Power Systems Inc,** 3100 Alfred St, Santa Clara, CA 95050. Phone (408) 247-5350. **Circle No 222**

QUAD SWITCHES. SW-01, -02, -03 and -04 spst overvoltage-protected units combine an innovative circuit design with JFET technology immune to static-discharge destruction to provide temperature-compensated channel ON resistance of 100Ω max (achieved by on-board amplifiers) and 0.03%/°C TC—an eightfold improvement over CMOS devices relative to R_{ON} vs temperature.

Specified maximum turn-on and turn-off times for the 16-pin-hermetic-DIP devices are 400 and 300 nsec, respectively. Address inputs are TTL and CMOS compatible without external resistors. -01 and -03 models are normally closed; -02 and -04, normally open. MIL-grade (−55 to +125°C) units, from $13.50; industrial-grade (−25 to +85°C) models, from $8.50 (100). **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050. Phone (408) 246-9222. **Circle No 223**



64k EPROM. The MCM68764 is an 8k×8-bit n-channel silicon-gate MOS unit that uses one 5V supply and comes in a standard 24-pin ROM package. The use of 24 pins rather than 28 is made possible by placing a dual function on pin 20—during programming it handles the 25V programming pulses, and in read operation it serves as the chip enable. Access time is 450 nsec, and the unit dissipates <880 mW in active mode (<140 mW in standby). $164; -68A764 (350-nsec access time), $196 (100). **Motorola Inc,** 3501 Ed Bluestein Blvd, Austin, TX 78721. Phone (512) 928-6660. **Circle No 224**

Who debugged debugging?

Introducing one of The Glitch Grabbers™ from Philips: the PM3540, a new logic analyzer that's specifically designed for digital debugging. It gets the bugs out fast because the PM3540 is the only compact instrument in the field today that allows data to be displayed, analyzed and then be directly related to real-time situations.

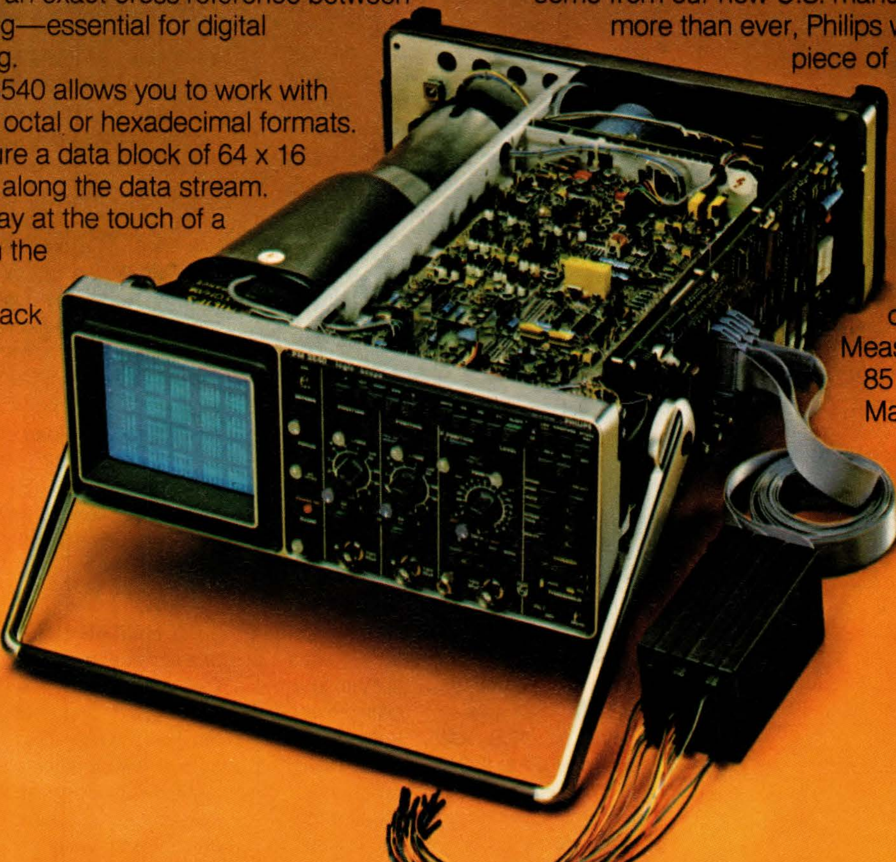
At the touch of a button the PM3540 changes from a logic analyzer to a two-channel oscilloscope, with interactive triggering from the same data word. This gives you an exact cross-reference between data and timing—essential for digital troubleshooting.

The PM3540 allows you to work with data in binary, octal or hexadecimal formats. You can capture a data block of 64 x 16 bits anywhere along the data stream. Page the display at the touch of a button through the data stream. Analyze and track down the fault and then set the PM3540 to trigger internally as an oscilloscope.

With the PM3540 you get both logic and real-time analysis in a single, compact, high-performance instrument. An instrument that speeds up your job of locating the bugs and correcting the digital faults.

When there's a better, more innovative way to design new test equipment, Philips will do it. And we'll do it and stand behind it right here in the USA. Philips intends to double sales by 1981. And this growth will come from our new U.S. manufacturing facilities. Now, more than ever, Philips wants to make *your* next piece of test equipment.

For more information call 800-631-7172, except in Hawaii, Alaska and New Jersey. In New Jersey call collect (201) 529-3800, or contact Philips Test & Measuring Instruments, Inc., 85 McKee Drive, Mahwah, NJ 07430.



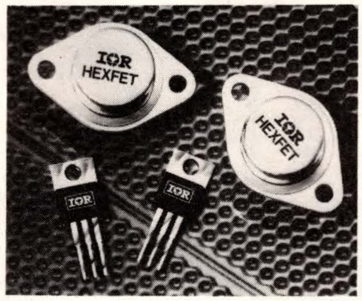
Philips, of course.

PHILIPS **Test & Measuring Instruments**

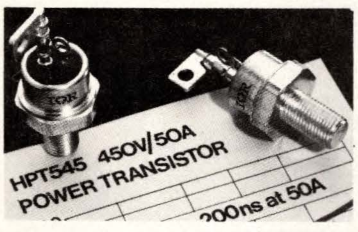
PHILIPS

For more information, Circle No 94

New Products

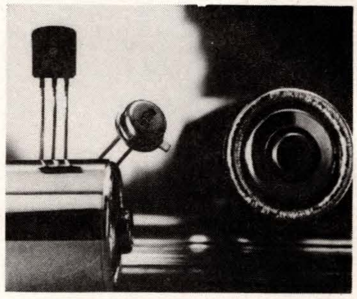


200V POWER TRANSISTORS. Suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits, these additions to the HexFET line furnish 4.5S typical transconductance, 30-nsec delay-time turn-on, 750-pF input capacitance and 250-pF output capacitance. TO-3 packaged, IRF230 models have a 200V rating, 0.4Ω on-resistance and 7A drain current; -231 types (with 150V ratings) share the same ON-resistance and drain-current specs. IFR230, $18.30; IRF231, $15.80 (10). **International Rectifier,** Semiconductor Div, 233 Kansas St, El Segundo, CA 90245. Phone (213) 772-2000. **Circle No 225**



NPN POWER TRANSISTORS. Rated at up to 50A continuous collector current (75A pk) with voltage ratings up to 450V, TO-83-packaged HPT540/545 and -440/445 Series devices furnish switching speeds of 200 nsec at 50A. -540 and -545 models feature $V_{CE(sat)}$ of 1V max at 50A, while -440 and -445 units provide 1V max at 40A. -545 Series units dissipate 300W at 2°C case temperature or 150W at 100°C case temperature. Maximum operating and storage-temperature range is −65 to +200°C. HPT440, $91.60; HPT445, $108.30; HPT540, $100; HPT545, $116.60 (10). **International Rectifier Semiconductor Div,** 233 Kansas St, El Segundo, CA 90245. Phone (213) 772-2000. **Circle No 226**

CALENDAR/CLOCK CIRCUIT. For use with any host μC, the μPD-1990C 14-pin CMOS serial input/output unit measures month, date, day of week, hr, min and sec. Specs include timing-pulse outputs of 64, 256 or 2048 Hz, a 32.768-Hz crystal-oscillator-generated reference frequency, 3.6V operating voltage and 100-μA max operating current (a 5V version is also available). Operating temperatures span −40 to +85°C. $3.50 (1000). **NEC Electron Inc,** 3120 Central Expressway, Santa Clara, CA 95051. Phone (408) 241-8222. **Circle No 227**



VOLTAGE REFERENCES. Using ion-implant technology with low operating currents, LM185/285/385 Series 1.2V diodes operate from 10 μA to 20 mA with virtually no change in performance. Dynamic impedance is typically 0.5Ω, and on-chip trimming gives tight tolerance. TCs typically equal 10 ppm. The LM385 is a low-noise bandgap voltage reference useful in battery-powered applications where low voltage (1.2V) and low power drain (12 μW) extend battery life. LM185 dissipates 12 μW when operating with 10 μA. LM385, available in 2-lead TO-46 hermetic package or TO-92 (commercial) plastic package, from $1.20 (100). **National Semiconductor,** 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 737-5856. **Circle No 228**

8-BIT MILITARY DACs. Military versions of a series of monolithic multiplying units, DAC-08 883 Series devices provide direct interfacing to all widely used logic families and full noise immunity furnished by high-swing adjustable-threshold logic inputs. For use in applications such as 1-μsec ADCs, servomotor and pen drivers and waveform generators, the 16-pin-plastic-DIP units have a power-supply range of 4.5 to 18V with essentially unchanged performance over the range. Features include 85-nsec output-current settling, 33 mW power consumption at ±5V and linearity to 0.1% over the −55 to +125°C operating-temperature range. From $1.70 (100). **Signetics,** 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-7700. **Circle No 229**

Our 64K ROM is like our 32K ROM is like our 16K ROM.

For new system designs and for upgrading existing systems, the flexibility of our totally static 64K ROM gives you that extra edge. And it's backed to the hilt with proven high performance.

The SY2364 is the latest addition to our family of 24-pin ROMs designed around a common industry standard pinout. That means maximum system flexibility. All three — 16K, 32K and 64K ROMs — can plug into the same socket. System upgrades are just a matter of substituting the new ROM for the old. With no increase in power.

We offer compatibility that's more than pin deep. All our ROMs are fully static (no clocks to worry about), so they all have the same timing waveforms. If speed is your concern, you can select one of our standard 450nsec versions or upgrade to our high performance 300nsec versions. All six are available now in quantity production.

	300ns	450ns
2K x 8	SY2316B-3	SY2316B
4K x 8	SY2332-3	SY2332
8K x 8	SY2364-3	SY2364

No matter what your needs, we have just the ROM for you. And that includes the SY2316A, SY4600 and SY2333 (pin compatible with the 2732/2732A 32K EPROM). For further information, contact Memory Product Marketing direct at (408) 988-5611. For Area Sales Offices and distribution references, call Headquarters Sales direct at (408) 988-5607. TWX: 910-338-0135.

For more information, Circle No 96

Synertek performs as a major MOS supplier of high volume parts with advanced technologies and techniques behind everything we make. ROMs. Static RAMs. EPROMs. Custom circuits. Single-chip Microcomputers. Systems. 6500 Microprocessors and Peripherals.

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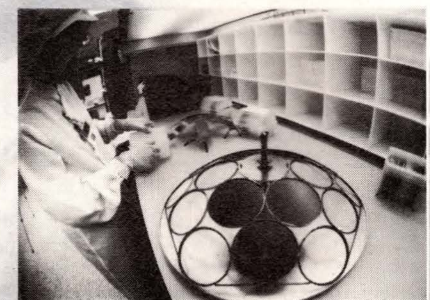
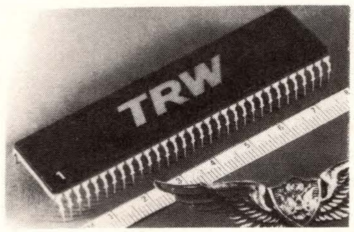


New Products

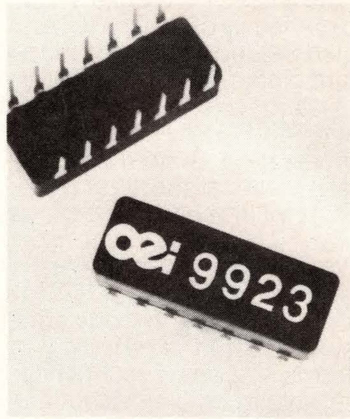


8-BIT MONOLITHIC ADC. A military-temperature - range version of the company's video-speed TDC-1007J ADC, TDC-1007J-M operates over a case - temperature range of −30 to +125°C and is also available tested to any of the MIL-STD-883B environmental test conditions. A replacement for bulky discrete and hybrid circuits in high-performance military radar and image-acquisition systems, the 64-pin-DIP unit can perform 30 million 8-bit conversions per sec while drawing 2.5W. It utilizes a fully parallel single chip that contains 20,000 closely matched bipolar components. \$781 (100); testing to 883B specs is additional. **TRW LSI Products,** Box 1125, Redondo Beach, CA 90278. Phone (213) 535-1831. **Circle No 230**

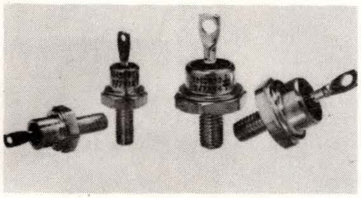
8-BIT DACs. NE/SE5118 and -5119 22-pin units feature ±0.19 (-5118) and ±0.1% (-5119) accuracy, 200-nsec settling time, zero-scale and gain TCs of 5 and 20 ppm/°C (independent of internal reference), <10-μA loading of data inputs, addressing capability and complying logic levels. The unit includes internal feedback and input resistors that provide good thermal tracking characteristics, and an on-chip low-TC short-circuit-protected voltage reference. \$6.95 (plastic); \$7.95 ceramic (100). **Signetics,** 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-7700.

Circle No 231

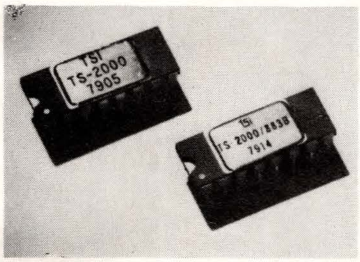
NONVOLATILE EAROMs. Fully decoded NC7051 (32×16-bit) and -7055 (64×8-bit) parts are second-source replacements for NCR's 2051 and 2055. Minimum data retention is 2×10^{11} read cycles per word before refresh, and the units provide unpowered nonvolatile data storage in excess of 10 yrs at 70°C. Data can be erased and rewritten in circuit up to 10^5 times. Applications include point - of - sale terminals, electronic games, nonmechanical TV tuners and automobile odometers. \$8.75 in ceramic, \$7 (100) in plastic. **Nitron,** 10420 Bubb Rd, Cupertino, CA 95014. Phone (408) 255-7550. **Circle No 232**



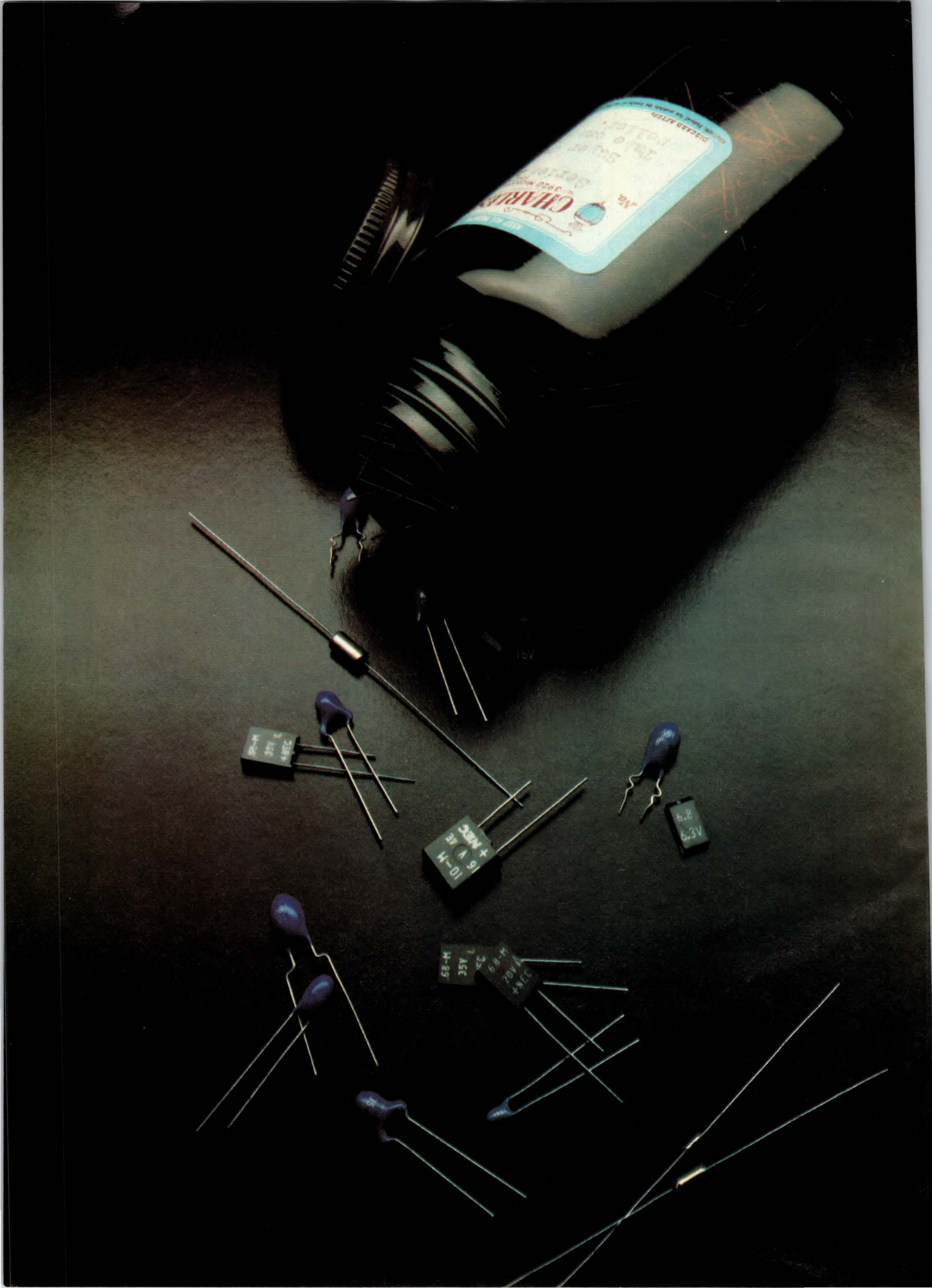
TRANSIMPEDANCE PREAMP. A 14-pin-DIP unit, Model 9923 features a 5-nV/$\sqrt{Hz}$ maximum spectral density with a 100-GΩ input impedance. Its 150V/μsec slew rate makes it useful in ultrasonic, sonar, communication and audio applications. Current noise is 30 fA/$\sqrt{Hz}$. The commercial-grade unit operates over a −65 to +125°C range. $31.50 (10). **Optical Electronics Inc,** Box 11140, Tucson, AZ 85734. Phone (602) 624-8358. **Circle No 233**



RECTIFIER DIODES. Diffused-junction silicon fast-recovery devices with ratings up to 400V, an average current rating of 6 to 30A and typical reverse-recovery time of 100 nsec, the IN3879 through -3913 Series of parts come in DO-4 or DO-5 stud-type hermetic packages. Typical V_F for 6A devices (-3879 through -3883) is 1.0V; for 30A units (-3909 through -3913), 1.1V. Applications include motor controls, dc/ac inverters and high-frequency rectification. From $2.14 (100). Delivery, 6 weeks ARO. **Ferranti Electric Inc,** Semiconductor Products, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200. **Circle No 234**



DUAL WINDOW DETECTOR. TS-2000 consists of two independent high-speed window detectors enclosed in a single 16-pin DIP to conserve space. Each detector provides three digital outputs (six outputs per package). Typically, the device has 300-nsec response time, 4-mV offset voltage and 25-nA offset current; it interfaces with TTL and/or CMOS and provides variable output-logic levels. Typical applications include multidecision-point monitors, out-of-limit indicators, feedback-controls, level detection and automatic test systems. $17.50 (100). **Transistor Specialtys Inc,** 3 Electronics Ave, Danvers, MA 01932. Phone (617) 774-8722. **Circle No 235**


NEC
6.3V

Super caps.

Our Solid Tantalum Capacitors are the perfect Rx for healthy performance and longer life.

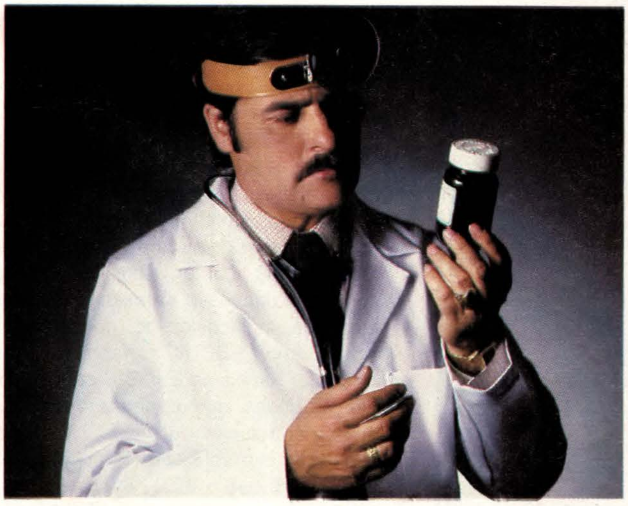
Get fussy.

Each new electronic product entering the market—whether it's a tiny watch or huge telecommunications system—is only as reliable as the components inside.

You must be as selective in ordering your standard electronic components as you are in choosing your new ICs or microprocessors.

Let's face it. A failure is a failure. And a leaky capacitor can work havoc on a "wonder product's" performance—no matter how fancy the electronic brain-center happens to be.

NEC has earned a worldwide reputation for delivering only the highest quality solid tantalum capacitors. During a 12-month period last year, NEC Electron shipped over 23 million without a single failure.



For immediate relief from all your capacitor problems, call "Doc" Roger Ferreira of NEC. His tantalums will make your system healthier in no time.

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We build our tantalums to last. Each capaccitor is burned in at 85° C at elevated voltages for extended periods of time to eliminate high leakage.

Our NEC tantalum line is broad, including: standard and miniature dips, bulk pack or lead tape and reel, epoxy end-sealed axials, and two types of chip capacitors. NEC tantalums feature working voltages from 3 to 50 volts, and capacitance ranges of .01 to 680 microfarads.

If you want your system to enjoy a long and healthy operating life, choose the capacitors you can specify with confidence. NEC solid tantalums. For more details, please fill out the coupon and send it to NEC today.

NEC

If you have designs on the future.

NEC Electron, Inc.
Mr. Roger Ferreira, Capacitor Product Manager
3120 Central Expressway
Santa Clara, CA 95051

Dear Roger:

I'm interested in giving my system a longer and healthier life. Please send me your capacitor catalog, reliability data, and sample request sheet as soon as possible.

Name __________

Title __________

Company __________

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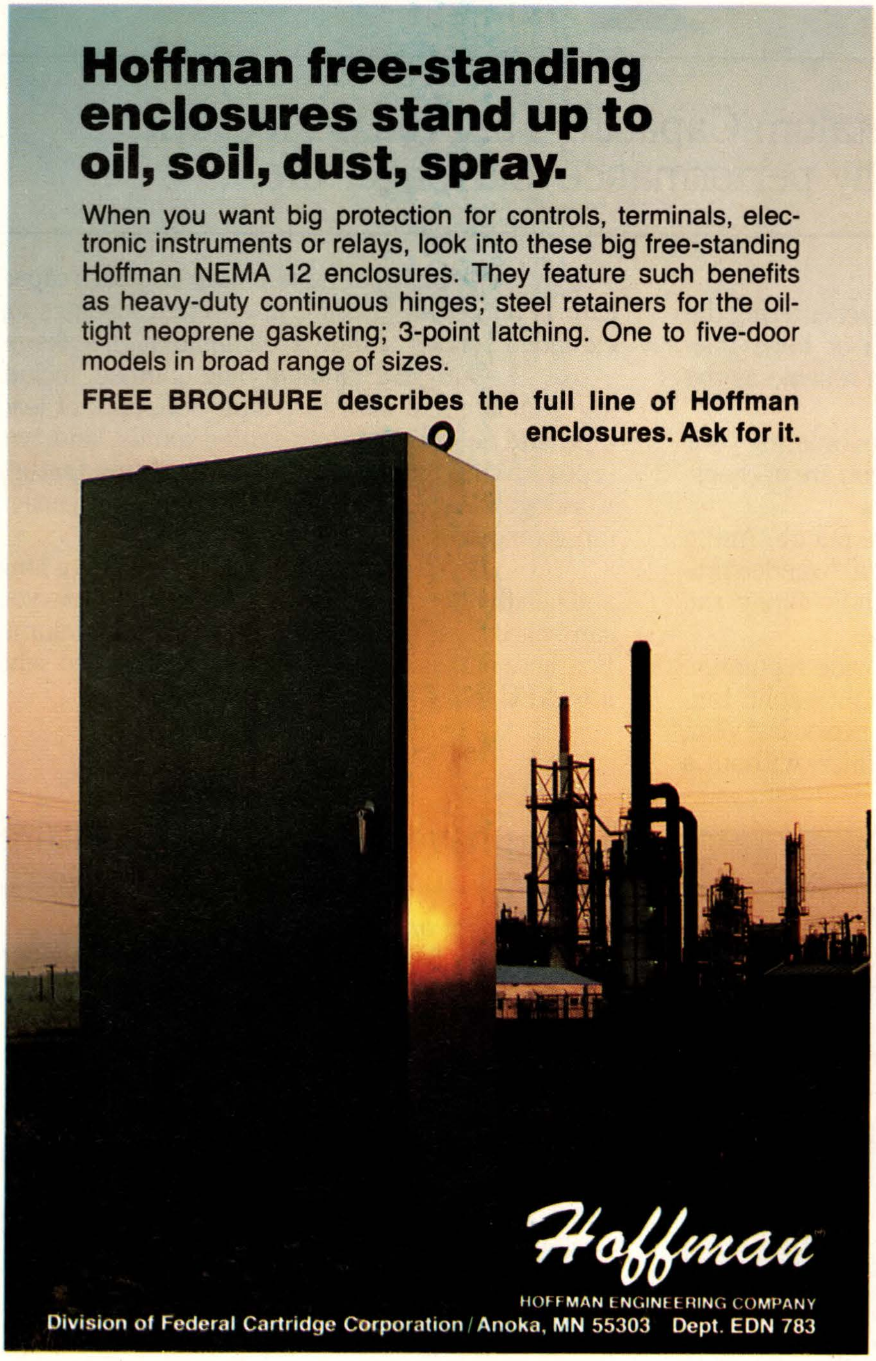
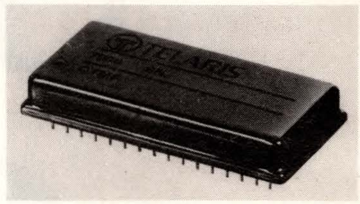
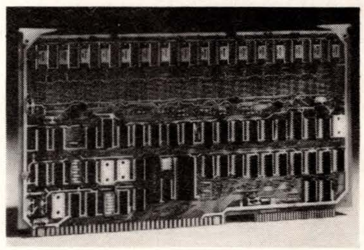
COMPUTER-SYSTEM SUBASSEMBLIES

A/D BOARD. Designed for industrial environments, and hardware and software compatible with the DEC LSI-11, LSI-11/2 and PDP-11/03/23 Series μCs, the 12-bit ST-LSI-RLY features eight differential A/D channels, ±½-LSB resolution, relay-isolated inputs, isolation of 250V rms to power ground, 126-dB CMRR and half-quad size. It can handle analog input signals ranging from ±10 mV to ±1V (bipolar) FSR (or 10 mV to 2V unipolar); overall system throughput time equals 36 msec sample to sample (28 samples/sec). $695. Delivery, 4 to 8 wks ARO. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341.
Circle No 202





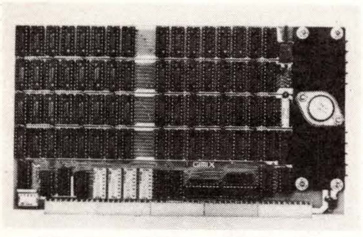
DTMF MODEM. Model 7900 is a binary-coded unit in a 32-pin package capable of interfacing directly between existing hexadecimal μP buses (without UARTs) for data-communication and electronic PABXs. Either half-duplex 2-wire or full-duplex 4-wire DTMF telephone data transmission can be implemented; only one external 3.58-MHz crystal is required. The modem suits key-telephone systems, autodialing applications and inexpensive handshake communications. $125 (50). **Telaris Telecommunications Inc,** 2772 Main St, Irvine, CA 92714. Phone (714) 754-7566. **Circle No 203**



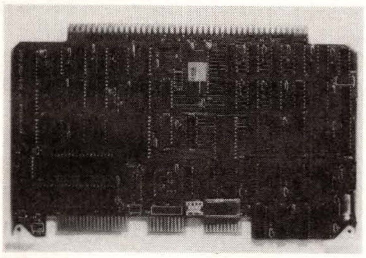
RAM BOARD. Fully compatible with Intel's iSBC-80 Multibus, RAM-032 contains 32k of dynamic RAM and has a memory-access time of 450 nsec. The unit is burned in at 55°C for 168 hrs before undergoing 16 hrs of reliability testing and comes with a 3-yr warranty. $950 (10). **Electronic Solutions Inc,** 5780 Chesapeake Ct, San Diego, CA 92123. Phone (714) 292-0242.
Circle No 204

LINE-PRINTER CONTROLLER. For use with IBM Series/1 computers, this unit can transmit 8-bit Japanese Industry Standard (JIS) code to all Printronix line printers as well as the Dataproducts Model 2530 printer, thus permitting printing of Japanese Katakana business language in addition to conventional ASCII and EBCDIC graphics. The controller translates EBCDIC codes into the JIS codes, outputs them to the line printer and furnishes the full graphics capability available with Printronix line printers. $1995. **MDB Systems Inc,** 1995 N Batavia St, Orange, CA 92665. Phone (714) 998-6900. **Circle No 205**

New Products



32k STATIC-RAM BOARD. This fully static 32k RAM board for use with the SS-50 (6800) and SS-50C (6809) bus features four independently DIP-switch-addressable 8k blocks; each 8k block can be addressed to any 8k boundary or disabled. The board can decode the four additional address lines of the SS-50C bus to allow memory decoding up to 1M bytes. The unit uses low-power 2114L RAM chips, typically draws 2A for 32k, is designed for high noise immunity, comes fully socketed and has gold bus connectors. $548.15. **Gimix Inc,** 1337 W 37 Pl, Chicago, IL 60609. Phone (312) 927-5510. **Circle No 206**

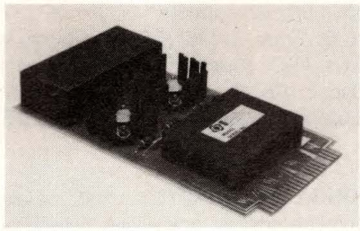


1-CARD CRT CONTROLLER. Exorciser - bus compatible and fully compatible with M6800, 6801E and 6809E µCs, MCG 6800 provides 128 characters (upper and lower case) and an 80×24 screen format with a 25th line for special command formats and queue requirements. Features include eight foreground and background colors; static RAM sections for display, FAC-code and graphics memory; 64 software dynamically definable characters that can be 128 firmware EPROM characters if required; and hardware control providing for scrolling, cursor and light-pen operation. An internal 16-MHz clock is also provided. From $595. **Phoenix Digital Corp,** 3027 N 33 Dr, Phoenix, AZ 85017. Phone (602) 278-3591. **Circle No 207**

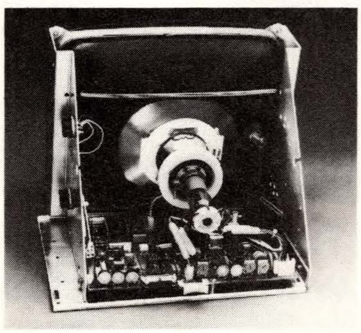
16-BIT ADC. Model ADC 1216 provides 14-µsec conversion speeds, ±0.003% accuracy, 16 - bit - binary or 2's-complement output and ±0.0015% linearity. Requiring no external reference-voltage source or amplifiers, it measures 5×4.5×1.5 in. and has an operating-temperature range of 0 to 70°C. From $1495. Delivery, 30 to 45 days ARO. **Phoenix Data Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017. Phone (602) 278-8528. **Circle No 208**

LONG-LINE ADAPTER. This parallel long-line adapter box allows line-printer controllers to operate almost any printer for full-speed parallel data transmission at distances up to 3000 ft. Suitable for controllers for computers such as the DEC PDP-8 and LSI-11 and IBM Series/1 Models, the 10×6×3½ in. rack-mountable unit can also be used to tie other peripheral devices such as card readers to a computer over long distances. $525. **MDB Systems Inc,** 1995 N Batavia St, Orange, CA 92665. Phone (714) 998-6900. **Circle No 209**

New Products



D/S CONVERTERS. The DSC40-PC-L-1 Series of 14-bit units can drive up to three Size 11 torque receiver synchros with ±6' accuracy. These 4.5×9.25×1-in. 400-Hz devices accept a 14-bit natural binary angle and convert it into 3-wire synchro or 4-wire resolver signals; output is short-circuit protected and current limited, and loading of 5 VA is standard. Available output voltages are 90 or 11.8V rms (60 or 400 Hz), digital inputs are TTL/DTL compatible, and the synchro output and reference are fully transformer isolated. Less than $475 (OEM qty). Delivery, 4 to 6 wks ARO. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731. Phone (516) 261-3300. **Circle No 210**

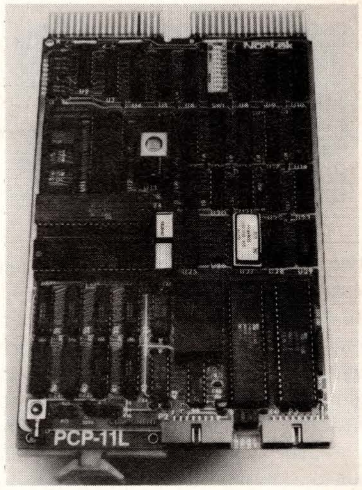


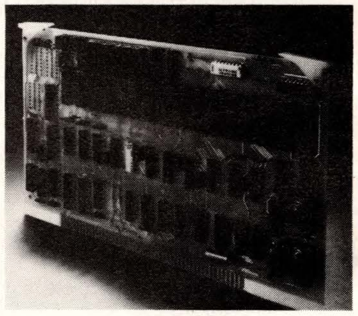
CRT MONITOR. Displaying more than 1920 characters in either white or green phosphor, HR-1500 provides 400 raster lines with a horizontal scan rate of 25 kHz, a refresh rate of 50 to 60 Hz, vertical step scan and dual intensity. The nonreflective 15-in.-diagonal CRT screen uses an etched, bonded faceplate to eliminate glare and provides an 110° deflection angle. $260 (OEM qty). Delivery, 60 days ARO. **Telex Computer Products Inc,** 6422 E 41 St, Tulsa, OK 74135. Phone (918) 627-1111.

Circle No 211

COMMUNICATIONS INTERFACE. A single-board peripheral computer compatible with the DEC LSI-11 family, the PCP-11L programmable communications processor furnishes a 24-line×40-column display and supports any mix of 8-bit parallel asynchronous or synchronous serial and color-video graphics. Used with an optional dialer interface, it can be programmed to provide autoanswer and autodial support for any serial-communications protocol. Data-transfer rates >48k baud can be employed. The board can be equipped with a mix of up to 8k bytes of RAM and/or 16k bytes of ROM. From $525 for basic unit with parallel port, 2k EPROM monitor and 1k of RAM. **Nortek Inc,** 2432 NW Johnson St, Portland, OR 97210. Phone (503) 226-3515.

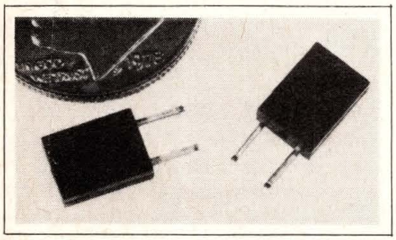
Circle No 212





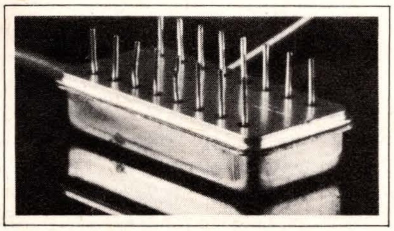
MEMORY PARITY CARD. For S-100-bus systems, MP100 maintains a continuous check on a computer's memory integrity during execution of software and halts a running program when a single bit of erroneous data is fetched by the CPU. Consisting of parity-generation circuitry and on-board RAM, the card features failed-location read by CPU (two ports), high-noise-immunity (Schmitt-trigger) bus interface, read data sampled on the same clock edge as CPU, board disable and force error for functional verification and 5V operation. $235. **IPDI,** 1708 Stierlin Rd, Mt View, CA 94043. Phone (415) 969-6086. **Circle No 213**

COMPONENTS & PACKAGING

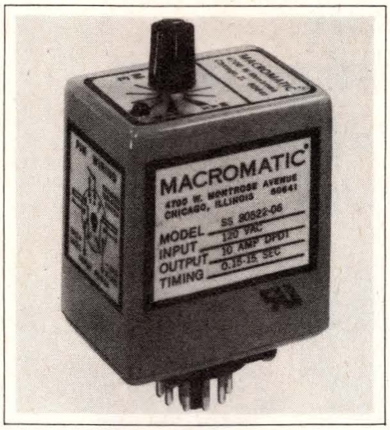


MICROMIN INDUCTORS. For use in IF and RF amplifiers, top-tunable ST Series units measure 0.275×0.1×0.2 in. to conserve space and permit denser packaging. Equipped with an internal adjusting screw, the devices are offered with inductance from 10 nH to 6 mH; typical Qs run from 30 to 50 over the range, and typical tolerances equal ±10%. Encapsulated in high-temperature molded epoxy, the units are constructed of military-grade materials and meet MIL-C-15305. From $2.33 (10k). **Piconics Inc,** 20 Cummings Rd, Tyngsboro, MA 01879. Phone (617) 649-7501. **Circle No 176**

DISPLAY SYSTEM. A 1-line, 40-character 5×10 dot-matrix LCD unit that can interface directly with μPs through a single peripheral parallel-interface device, LX140 has on-board custom CMOS LSI drive chips that incorporate an integral RAM for all 2000 display elements, with each dot addressable. On-board circuitry also generates all refresh signals, thus eliminating the need for continuous data transfer to the display module. Additional circuitry provides temperature compensation and a dc/dc converter for generating the required internal voltage. Compatible with 5V logic families, the system operates from one 5V power supply. $199 (100). **Kylex,** 420 Bernardo Ave, Mt View, CA 94043. Phone (415) 969-5200. **Circle No 177**



F-O DRIVER/LED. 16-pin-DIP LDT-256 combines a standard 75451B TTL driver chip with the manufacturer's pigtailed IRE-160F etched-well LED. The control circuit handles either NRZ or RZ codes; NRZ data rates can range to 40 MHz and RZ codes to 20 MHz. The IC drives up to 200 mA dc. The emitter couples >50 μW of core power into standard communication-grade fiber (55-μm core, 125-μm cladding), and the LED provides 10-nsec typ rise and fall times and a peak emission wavelength of 820 nm. $395. **Laser Diode Laboratories Inc,** 1130 Somerset St, New Brunswick, NJ 08901. Phone (201) 249-7000. **Circle No 178**

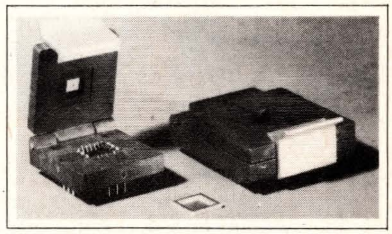


TIMING DEVICES. These digital SSD Series timers employ CMOS IC circuitry with on-board oscillators and come as on-delay, off-delay, retriggerable single-shot and interval-on units. All widely used timing ranges from 10 min to 24 hrs are available with a repeatable accuracy of ±0.05%. Features of the plug-in series include LED pilot lights, internal steel frames for added RF shielding and an operating-temperature range of −40 to +175°F. Input voltages include 12V dc, and output is accomplished with either a 10A dpdt electromechanical or 3A spdt solid-state relay. From $65. **Macromatic Inc,** 4700 W Montrose Ave, Chicago, IL 60641. Phone (312) 286-7977. **Circle No 179**

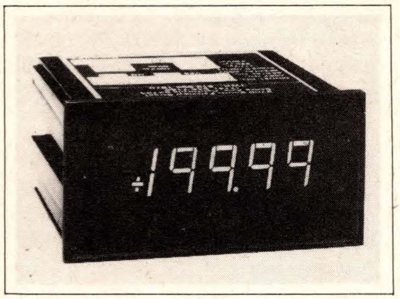
QUIL ADAPTER SOCKETS. 64-, 48- and 42-position units in the QUIL-15 Series convert any standard dual-in-line sockets with 0.3-in. centers or universal contacts in columns with 0.3-in. centers to an 0.050-in. off-set quadruple-in-line (QUIL) pattern. Model 664-QUIL-15 has 64 positions; 648-QUIL-15, 48; 642-QUIL-15, 42. The sockets are Swiss-screw-machined parts; contact sleeves are brass gold-plated over nickel with 4-tine beryllium spring clips, 25-μin. gold plated over 50- to 100-μin. nickel. $4.20 to $6. **Garry Mfg Co,** 1010 Jersey Ave, New Brunswick, NJ 08902. Phone (201) 545-2424. **Circle No 180**

EDGE-MOUNTING LEDs. PCV125 Series devices mount on 0.245-in. centers on the edge of a standard pc board with straddled leads soldered to opposite sides of the board; the units project 0.305 in. beyond the board edge. The 0.125-in.-diameter, 0.122-in.-thick LEDs come in both standard and superbright versions of red, amber and green with clear and diffused lenses. Operating voltages are 3.6 to 28V with an external resistor required in most cases. $0.32 (1k). **Data Display Products,** 303 N Oak St, Inglewood, CA 90302. Phone (213) 674-5940. **Circle No 181**

POWER ATTENUATORS. Conduction-cooled, flange-mounted PPA 50 units for microstrip applications dissipate 50W at a heat-sink temperature of 85°C. Rated input power is 100W for the 3-dB unit, 75W for the 6-dB unit and 50W for 10-dB or higher units. Specs include dc to 1000-MHz operation, 1.15 max VSWR from dc to 500 MHz (1.2 max from 500 to 1000 MHz) and attenuation accuracy of ±0.3 dB from dc to 500 mHz and ±0.5 dB from 500 to 1000 MHz. $25 (100). Delivery, stock to 6 wks. **KDI Pyrofilm Corp,** 60 S Jefferson Rd, Whippany, NJ 07981. Phone (201) 887-8100. **Circle No 182**

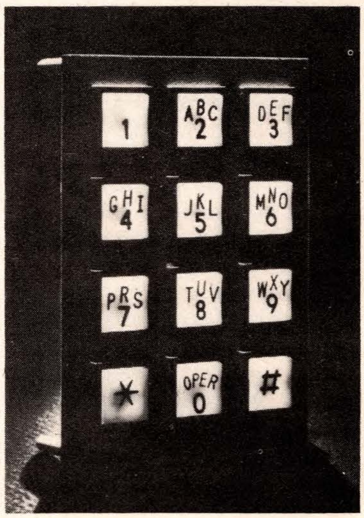


TEST SOCKETS. ZIF-connection LCS Series devices allow testing of individual leadless ceramic ICs meeting JEDEC packaging standards. Burn-in of hermetically sealed ICs can be accomplished at temperatures up to 220°C. Beryllium-copper contacts are mounted inside the units beneath their body surface to prevent damage during repeated use; a bottom hole in the base speeds extraction. Sockets are available in 24-, 32-, 40-, 48-, 64- and 84-lead sizes. $18.08 (100) for a typical unit. Delivery, 6 wks ARO. **Robinson-Nugent,** 800 E Eighth St, New Albany, IN 47150. Phone (812) 945-0211. **Circle No 183**



4½-DIGIT DPM. Model 479A provides full-scale reading of ±19999 counts, displayed by 0.56-in. LEDs in four ranges from 200 mV to 200V; ratio operation is optional. Reading error equals ±(0.005% of reading+1 count) with zero stability of ±0.1 μV/°C. Bias current is typically 20 pA. BCD outputs, available as either parallel or bit-character serial, are buffered and latched with a 3-state output for digital multiplexing or busing. Input power is 110/220V±20% (50 to 400 Hz); 5V-dc-powered models are also available. From $139. **Data Tech,** 2700 S Fairview St, Santa Ana, CA 92704. Phone (714) 546-7160. **Circle No 184**

ACTIVE-FILTER MODULE. The cutoff or center frequencies of this programmable unit can be set with the aid of binary-coded signals. Model AP-DP-8S-5P is a 5-pole 30-dB/octave low-pass filter, covering the cutoff-frequency range of 10 Hz to 100 kHz; eight cutoff frequencies can be selected in that range at f_o, $4f_o$, $8f_o$, $16f_o$, $32f_o$, $64f_o$ and $128f_o$. Response is maximum-flatness Butterworth, but an external switch can convert it to the linearized-phase type preferred in pulse work. The 3.5×2.5×0.5-in. unit requires ±17 mA with a ±6V supply. $255 (100). Delivery, 4 to 12 wks ARO. **A P Circuit Corp,** 865 West End Ave, New York, NY 10025. Phone (212) 222-0876. **Circle No 185**



TELEPHONE KEYPADS. Additions to the ET short-stroke line, these 12- and 16-key models have translucent keytops that permit backlighting. Replacing conventional opaque 2-shot-molded keytops, the units feature a sublimated legend transferred directly into their surface. A patented screened-Mylar-membrane technology provides crisp tactile feel, a life rating of 10 million operations per key and contact bounce of <3 msec. The transparent membrane circuit and plastic backer facilitate light transmission to the keytops. From $3.75 to $5.35 (1k). **Chomerics Inc,** 77 Dragon Ct, Woburn, MA 01801. Phone (617) 935-4850. **Circle No 186**

Photograph Courtesy of the National Archives

Brite-Lites® Stay Bright.

Our Brite-Lite LED lamps not only shine as bright as incandescents, they shine longer—more than 10 times longer. At 20 milliamps, they'll shine at least 10 years. Continuous or pulsed, they operate without life loss, using less than half the power of an incandescent. And they're 25 times brighter than other LED's on the market. That's dependability in the tradition of Boston Light.

Whether installed in sophisticated computer control panels or simple telephone pushbuttons, our Brite-Lites suit your requirements. Midget-flanged, snap-ins, PC lites, and wide-angle LEDY bugs,® are available in transparent or translucent red, amber, or green; from 1.6 to 48 volts; from 10 to 30 milliamps. And our LED lamps are American-made, so you're assured of dependable, prompt delivery.

When Digital Equipment Corporation conducted a series of tests for plug-compatible LED's which had both the brightness and long life they required, they chose Brite-Lite LED's with solid state reliability to replace their incandescent lamps.

For LED lamps that stay bright, isn't it time you switched to Brite-Lites.

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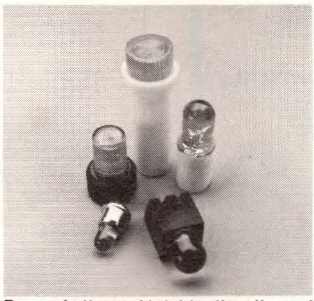
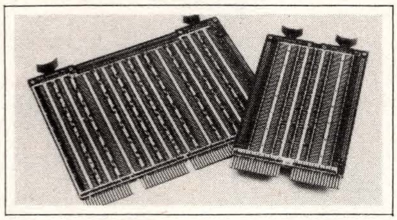


Proven better and brighter than the rest

DATA
DISPLAY
PRODUCTS

For more information, Circle No 105

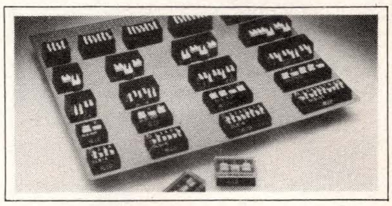
New Products



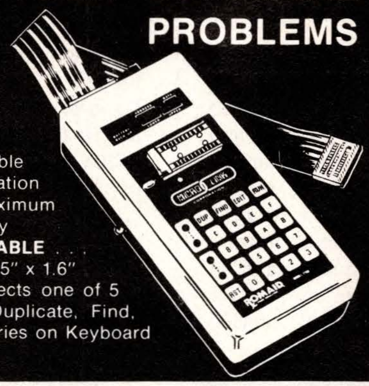
WIRE-WRAPPING BOARDS. These boards accommodate any combination of standard DIPs and feature two I/O edge-connector positions (100 pins each) that accept any ribbon-cable edge-connector configuration; wire-wrapping posts are on the component side, requiring only one chassis slot. W9501 universal module can be used in either the DEC LSI-11 or the PDP-11 computer and provides for up to 90 low-profile sockets or ICs with 14 to 40 pins. Power and ground decoupling pads with plated-through holes are furnished in the IC positions of this quad board. M91WW dual I/O module for PDP-11 computers provides for up to 28 sockets or ICs. W9501, $175; M91WW, $75. **MDB Systems Inc,** 1995 N Batavia St, Orange, CA 92665. Phone (714) 998-6900. **Circle No 187**

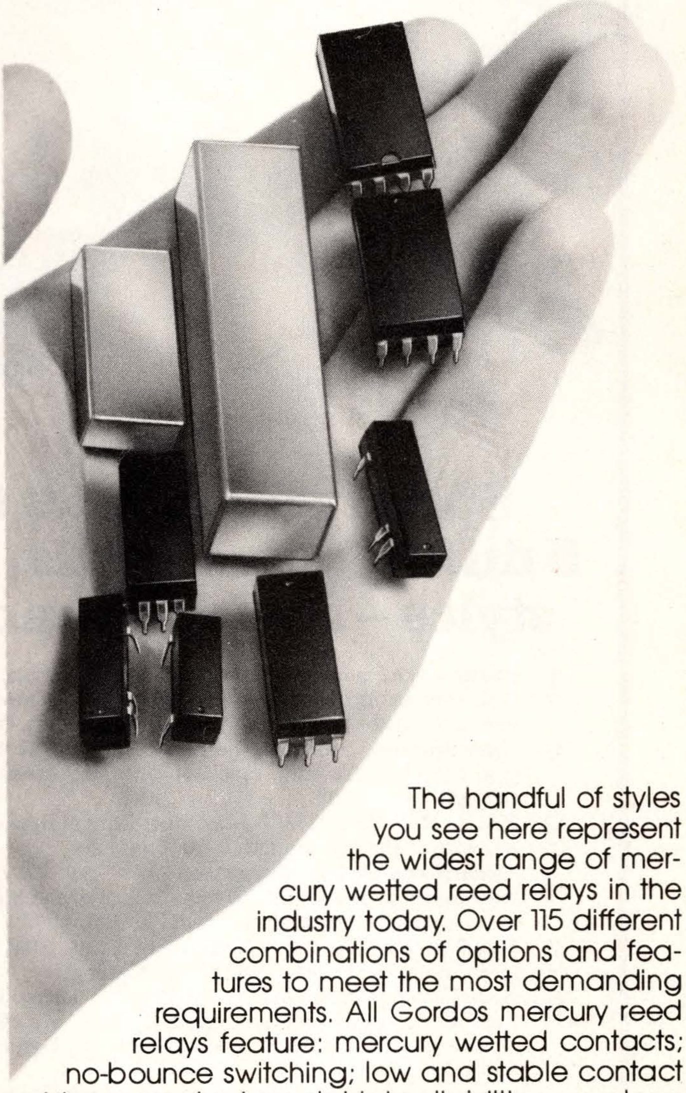
DRY-REED RELAY. This Form 2A epoxy-encapsulated unit provides good EMF stability for low-signal switching applications at $<10\ \mu V$ and comes in 5, 6 or 12V versions rated at 200V and 10W; initial maximum contact resistance is 0.1Ω. Features include small package size ($0.44\times0.38\times1.2$ in. with 100×1-in. grid), pc-board mounting and insulation resistance of $10^{12}\Omega$. An electrostatic shield is optional. <$3 (1k). Delivery, 4 to 6 wks ARO. **Electronic Instrument & Specialty Corp,** 42 Pleasant St, Stoneham, MA 02180. Phone (617) 438-5300. **Circle No 188**

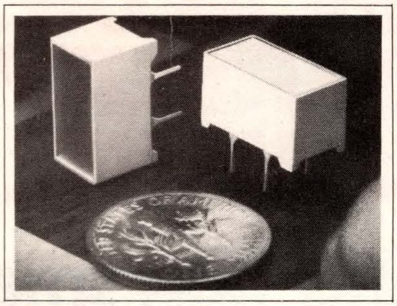
RECTANGULAR LEDs. 521 Series LEDs feature tinted and diffused rectangular epoxy encapsulation and can be stacked vertically or horizontally for flush mounting. Three colors are available: Series -9264 is a high-efficiency red GaAsP-on-GaP Model; Series -9265, a yellow GaAsP-on-GaP; Series -9266, a green GaP. Maximum ratings for all three lamps include power dissipation of 120 mW and an average forward current of 30 mA. Luminous intensity typically specs at 2.5 mcd at 25 mA. $0.60 (1k). **Dialight,** 203 Harrison Pl, Brooklyn, NY 11237. Phone (212) 497-7600. **Circle No 189**



DIP SWITCHES. For soldering onto pc boards or optional use with standard DIP sockets, these units are available in three basic types: rockers, slides and piano types with side actuation. They come in a choice of 4- through 10-pole configurations, either normally open or spdt. Terminals and contacts are of beryllium copper with heavy gold plate over nickel; terminals are either molded-in or epoxied to provide a full seal. Protective covers are available with an actuator-lock feature. **Alco Electronic Products Inc,** Box 568, Lawrence, MA 01842. Phone (617) 685-4371. **Circle No 190**

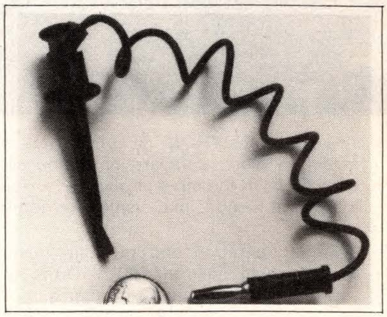






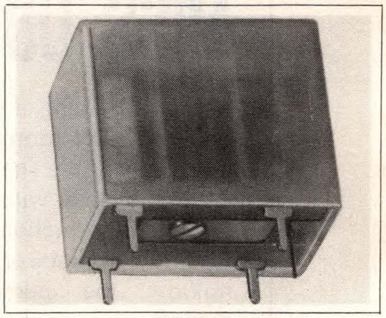
RECTANGULAR DUAL LED. MV57173, available in high-efficiency red, provides an 0.5×0.25-in. lighted area by using two LED chips with separate anodes and cathodes. End stackable, the 4-pin unit uses 0.2-in. DIP lead spacing and operates at temperatures ranging from −40 to +85°C. Continuous forward current per light (at 25°C) is rated at an absolute maximum of 35 mA; power dissipation, 200 mW. A special mounting grommet (MP73) simplifies assembly. MV57173, $1.20; MP73, $0.11 (1k). **General Instrument Optoelectronics Div,** 3400 Hillview Ave, Palo Alto, CA 94304. Phone (415) 493-0400.

Circle No 191



CLIP/PLUG ASSEMBLY. Model 4650 in-line unit consists of a Minigrabber, flexible lead and a banana plug made of spring 1-piece heat-treated beryllium copper; the plug's brass body is nickel plated and polypropylene insulated. The Minigrabber has a gold-plated 20-AWG beryllium-copper contact insulated with glass-filled nylon. The assembly comes in lengths of 12, 24, 36, 48 and 60 in. $1.85 to $2.05. **ITT Pomona Electronics,** 1500 E Ninth St, Pomona, CA 91766. Phone (714) 623-3463.

Circle No 192



SUBMINIATURE RELAYS. Series 1565 3A pc-board units come in a choice of spdt, spst normally open or spst normally closed switching configuration. Measuring 0.97×0.678×0.81 in. overall (including terminals), their molded nylon enclosures keep contacts free from dust and dirt. Terminals mount directly on a pc board. Specs include voltages of 3 to 24V dc, coil resistances of 11 to 720Ω dc, coil power of 800 mW nominal (450 mW min), expected mechanical life of 20 million operations and electrical life of 200,000 operations at rated load. **Guardian Electric Mfg Co,** 1550 W Carroll Ave, Chicago, IL 60607. Phone (312) 243-1100.

Circle No 193

SIEMENS

The fastest DIP Handler you can buy...

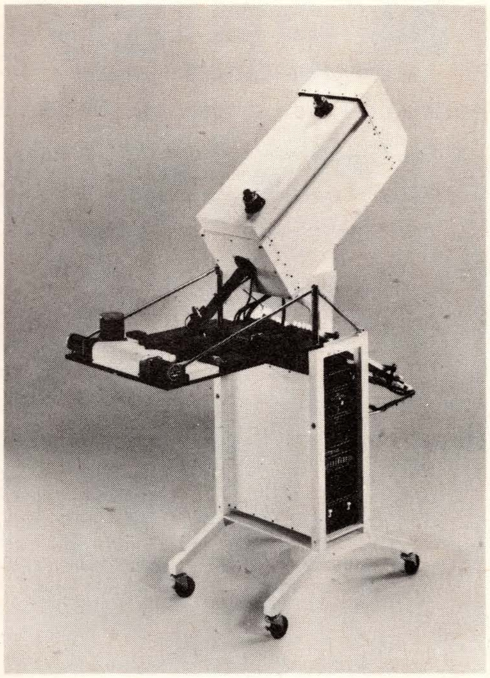
plus friendly tester interface.

In both configurations, ambient and hot, it's the fastest handler commercially available. A full 10,000 per hour (max.). Including 250ms of precious test time. With eight output sorts.

Because Siemens manufactures both testers and handlers, we designed the 1108 Series IC handlers to interface with virtually all testers. You can't expect that expertise from people who just make one or the other.

So if you need applications assistance, give us a call. We're sure that we can solve your problem quickly ... probably by phone. Which will give you some idea of how nice it is to work with a single source that can assume total responsibility for both sides of the interface.

For complete information on the 1108 Series IC handler, call or write Cliff Small.

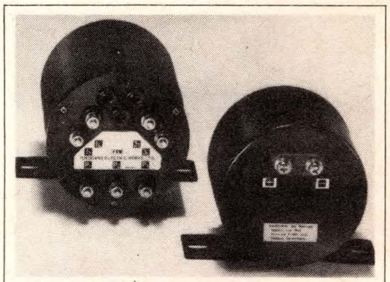


Siemens Corporation
Measurement Systems Division
2 Pin Oak Lane
Cherry Hill, New Jersey 08034 (609) 424-9210

It's what you'd expect from a leading tester manufacturer.

For more information, Circle No 111

New Products



TRANSDUCERS. For applications in which the output circuit is floated, these units contain built-in circuitry that provides ±0.5% accuracy for true-rms volts, amps, watts and reactive volt-amperes. They come in single-phase 2-wire amp and volt models and single-phase 2-wire, 3-phase 3-wire and 3-phase 4-wire models for watts and VARs. Other specs include current rating of 5A, voltage rating of 150V ac, watts and VARs rated for inputs of 5A/120V, crest factors as high as 3 and 0 to 1-mA dc output. Volt and amp units, $48; watt and VAR models, $125 to $160. **Yokogawa Corp of America,** 5 Westchester Plaza, Elmsford, NY 10523. Phone (914) 592-6767. **Circle No 194**

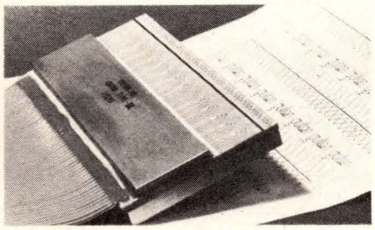
PRESSURE SENSORS. Potentiometer-type devices, Series 100 units provide a choice of pressure ranges from 0 to 100 psi to 0 to 5000 psi, gauge or absolute. The sensors furnish 1% accuracy, 0.1% repeatability, 1% hysteresis and linearity tolerances to 0.5% (independent). All units feature Resistofilm resistive elements that provide infinite resolution and operational-life expectancies of 25 million cycles. From $40. Delivery, 60 days ARO. **New England Instrument Co,** Kendall Lane, Natick, MA 01760. Phone (617) 875-9711. **Circle No 195**

ALPHANUMERIC DISPLAY. A compact, 12V-dc-operated 10½×5×4-in. 8-digit unit with minicomputer-based controller and 1-in.-high characters easily readable at 75 ft, Message Central has three colored lights mounted on its top that can be programmed to flash for attention or can be lighted in different combinations to communicate specific instructions. Up to 256 individually addressable units can be controlled from a centrally located CRT, computer or similar input device. One to eight separate RS-232 interfaces are possible, and an on-line display-lamp and circuit check can be made without shutdown. $990. **SMS,** 26 Olney Ave, Cherry Hill, NJ 08003. Phone (609) 424-5220. **Circle No 196**

New Products

Ku-BAND SOURCE. A high-power, solid-state microwave source, Model DMS-12418-50 YIG-tuned broadband oscillator covers 12.4 to 18 GHz and furnishes 50 mW into 50Ω (60 mW typ) over the full band. Other specs include frequency linearity of ±0.15%, −60-dBc spurious output, a maximum harmonic content of −20 dB and −10 to +50°C operating-temperature range. $1800. Delivery, 90 days ARO. **Weinschel Engineering,** Box 577, Gaithersburg, MD 20760. Phone (301) 948-3434.
Circle No 197

CHIP INDUCTORS. Supermicrominiature Series C devices are 2- to 500-nH gas-tight, ceramic-glass-encapsulated thin-film units that furnish an inductance TC <20 ppm°C and f_0 to 6 GHz. They have been cycled from −196 to +450°C with no change in value and are radiation qualified for space applications. Available singly or in matched sets with ±2% tolerances, the units are suitable for applications up to and including C Band. **Thinco,** Hatboro, PA 19040. Phone (215) 675-5000. **Circle No 198**



THERMAL PRINTHEADS. Series DM 48256, 48288 and 69414 dot-matrix units provide dot densities of 88, 91 and 100 dots/in., respectively, and printing speeds to 5 lps for alphanumeric text and up to 0.5 ips for graphics. The printheads, furnished with a soldered PVC ribbon cable on a standard heatsink, can be driven by simplified μC interface circuitry using standard 10-bit BiMOS-latched driver packages. Minimum MTBF is rated at 100 million dot pulses per dot element and 10 million character lines. $79.45 to $105.90 (100). **Gulton Industries Inc,** 212 Durham Ave, Metuchen, NJ 08840. Phone (212) 548-2800. **Circle No 199**

PLANAR DISPLAYS. The SP-450-018 (screened-image) and HB-233-01 (raised-cathode) are 14-segment alphanumeric gas-discharge displays that provide upper-case letters, numbers, many special characters and any symbol that can be made with 14 segments. HB-233-01 features three 0.28-in.-high 500-fL neon-orange characters for difficult viewing environments (expandable by threes on equal centerline spacing), viewable at a 130° angle. SP-450-018 features 20 0.5-in.-high 70-fL characters, visible over a 120° angle. Mounting depth for the screened-image unit (including tubulation) is 0.8 in., 0.5 in. for the HB-233-01. **Beckman Instruments,** 350 N Hayden Rd, Scottsdale, AZ 85257. Phone (602) 947-8371. **Circle No 201**

See EEM pp. 1329-1332

Circle No 98

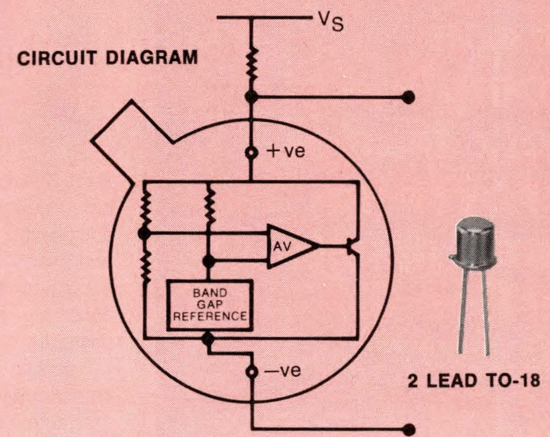
New Products

COMPUTERS & PERIPHERALS

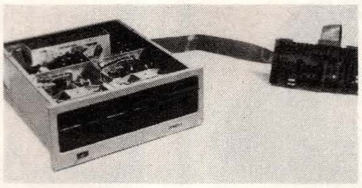
VIDEO DISPLAYS. Suited for a wide range of applications requiring high-speed interactive communication, Dasher D100 and D200 display up to 1920 7×11 dot-matrix alphanumeric characters arranged in 24 lines, each containing 80 characters. All 96 upper- and lower-case ASCII characters can be shown. D200 provides a main keypad, a 12-key screen-management keypad, a 14-key numeric keypad and a 15-key function keypad. Model D100 combines cursor and numeric keypads; certain function codes can be generated by depressing a combination of keys simultaneously.

Screen-management features include keys that move the cursor up, down, left, right and back to its home position. For information highlighting and forms design, you can select user-defined character attributes to differentiate portions of the displayed text. The block-fill cursor can be addressed either directly from the keyboard or indirectly from the processor to ease implementation of screen-oriented applications software. Model 6106 D100, $1750; Model 6108 D200, $1950. Delivery, 60 days ARO. **Data General Corp,** Rte 9, Westboro, MA 01581. Phone (617) 366-8911. **Circle No 214**

PRINTER ADAPTER. Capable of driving a printer with an RS-232 interface from the Commodore PET IEEE-488 bus, ADA 1400 is addressable, works with Commodore discs and prints upper- and lower-case ASCII characters. A PET IEEE-type port is provided for daisy-chaining other devices. The unit also comes with a cassette tape with programs for plot routines, data formatting and screen dumps. $179, including PET IEEE-bus cable, RS-232 cable, power supply, case, instructions and software. **Connecticut MicroComputer Inc,** 150 Pocono Rd, Brookfield, CT 06804. Phone (203) 775-9659. **Circle No 215**


CIRCUIT DIAGRAM
VS
+ve
AV
BAND GAP REFERENCE
—ve
2 LEAD TO-18

New Products



DISKETTE HARDWARE. This Multibus-compatible system is hardware and software compatible with Intel's MDS-800 and Series II computers. ZX-710/720 provides a complete bulk-storage system that can operate with single- or double-density recording formats and replaces Intel's MDS-710, -720, -2DS, -DDS and SBC-201, -202, -211 and -212 systems. Shugart SA801 drives are housed horizontally in a 19-in. rack-mountable chassis. $3900. **Zendex Corp,** 6398 Dougherty Rd, Dublin, CA 94566. Phone (415) 829-1284.

Circle No 216

BAR-CODE WAND. Designed to scan bar code and output a logic-level pulse-width representation of the bars and spaces, HEDS-3000 digital unit has a push-to-read switch and fits applications in portable data entry and microperipherals. The heart of the unit is a precision optical sensor that reads all common bar-code formats printed with a minimum bar width of 0.3 mm (0.012 in.). Signal-conditioning circuitry in the wand includes an analog amplifier, a digitizing circuit and an output transistor. Logic-level outputs are TTL and CMOS compatible. $99.50. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304. Phone (415) 856-1501.

Circle No 217

8086/8088 SOFTWARE. A relocatable macroassembler, linking loader and simulator for the 8086/8088 μP, these programs are written in ANSI-standard FORTRAN IV and run on any general-purpose computer, including 16-bit minicomputers. Assembler features include conditional assembly, macroassembly and a symbol or cross-reference table; the object-module output can be in a relocatable format or produced directly in Intel's hex format. Program, data, stack and common segments are provided. Assembler and linking loader, $1250; simulator, $1000; manual for any of the programs, $15. **Microtec,** Box 60337, Sunnyvale, CA 94088. Phone (408) 733-2919.

Circle No 218

TAPE SYSTEM. Model 2101 GPIB-compatible unit uses ½-in. tape and provides transfer rates in excess of 100k bytes/sec and a dual buffering capacity to 16,384 bytes. A dedicated Z80A μP manages bus-interface, formatter and tape-transport functions within the system. Systems can be 7 or 9 track and NRZI, phase encoded or dual mode in a variety of reel sizes, with or without code conversion. From $7995. **Dylon Corp,** 3670 Ruffin Rd, San Diego, CA 92123. Phone (714) 292-5584. **Circle No 219**

CLUSTERED SYSTEM. For general office applications requiring more than one workstation, Mini Cluster information-processing system performs data, communications and word/text processing with a common file structure for the word, data and communications data bases. The standard storage module combines a New World Computer 2M-byte Winchester hard disc with an 8-in. floppy disc. The standard system consists of a CPU, the New World Intelligent Information Storage Module, an NEC printer and up to four secondary processors. $27,000 to $45,000. **Xmark Corp,** 3176 Pullman St, Costa Mesa, CA 92626. Phone (714) 556-9210. **Circle No 220**

"Smart force" power from ERG puts electroluminescence in a whole new light!

PROBLEM:

As electroluminescent lamps age, their brightness drops off considerably. Until now, this characteristic has stymied many engineers who sought the exciting design advantages offered by EL technology.

OLD SOLUTION:

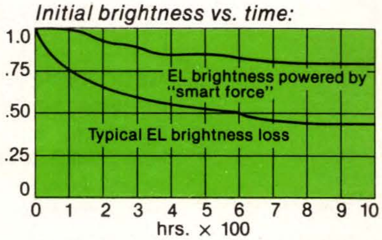
"Brute force" — continually increase voltage supplied to lamp to sustain EL brightness over lamp life duration. Method often contributed to premature lamp failure. And componentry was expensive!

NEW SOLUTION:

"Smart force" — achieve essentially constant EL brightness through self-correcting DC-to-AC power inversion. Energy-efficiency at *low* cost!

ERG DC-to-AC inverter
Patent pending

Initial brightness vs. time:



Luminescent Systems #20014-2 EL lamp (16 IN²) and ERG E613 - E0003 inverter (V IN = 12V).

ERG spearheads the EL power breakthru!

From Endicott Research Group comes an exciting new development in electroluminescent power technology! An economical, yet reliable, power source which overcomes the problem posed by EL aging.

Because it automatically adapts its own voltage and frequency over the course of EL lamp life, our "smart force" E600 DC-to-AC inverter delivers constant power output, maintaining essentially constant brightness.

"ERG" opens the door to the EL universe

Our E600 helps you open the door to almost limitless design options made possible by electroluminescence. Use EL to backlight LCD's, membrane switches and "dead-front" panels. Or put EL to work for lighting, for signalling, for decorating, in a host of consumer, industrial and military applications!

Tell us about your EL power needs

Our E600 has met the economy and reliability needs of the auto industry! And now, we can tailor EL power to your needs.

Let us know your: 1. EL surface area to be excited; **2.** type of EL phosphors; and **3.** brightness level desired.

Call or write today!

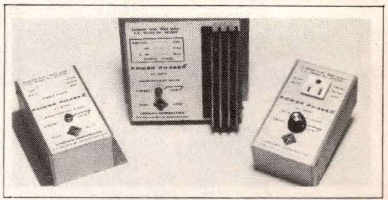
EL power starts here!

Endicott Research Group, Inc.
Subsidiary of Endicott Coil Co., Inc.
P.O. Box 128 Westview Station, Binghamton, N.Y. 13905
607-798-7846 TWX 510-252-0155

For more information, Circle No 117

New Products

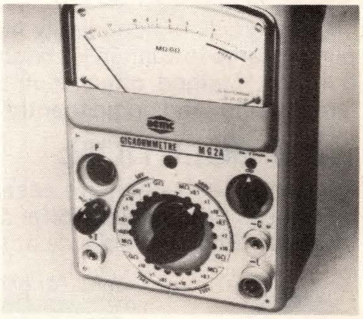
INSTRUMENTATION & POWER SOURCES



MOTOR CONTROLLER. Manufactured under license from NASA, these Power Phaser versions of the NASA induction-motor controller (EDN, September 5, 1979, pgs 185-189) can reduce motor operating cost up to 70%, improve power factor and extend operating life.

Model A1110C single - phase, 1 - hp 120V/15A rms max (50 or 60 Hz) unit connects to any grounded 120V receptacle and measures 5×2.6×2 in.; the motor to be controlled plugs directly into it. Model A1110 has the same ratings but wires into the motor circuit.

Single-phase 5×5×2-in. Model A5220 also wires directly into a motor circuit but can handle 240V/30A rms max (50 or 60 Hz). A 3-phase unit will be available in the near future. A1110C (consumer grade), $29.95; A1110 (industrial grade), $49.95; A5220 (industrial grade), $89.95. Delivery, 6 to 8 wks ARO. **Lincomm Corp,** Box 543, Bel Air, MD 21014. Phone (301) 838-8293. **Circle No 166**



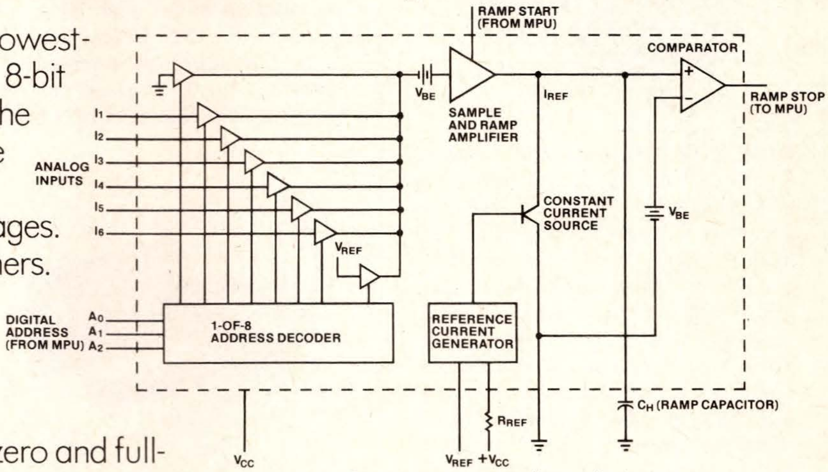
MEGOHMMETER. MG2A provides direct-reading measurements of high resistances and insulation resistances from 30 kΩ to 10^6 MΩ (1 TΩ) in 18 ranges. Features include three constant test voltages (50, 250 and 500V dc), adjustable time constant, built-in guard terminal, automatic discharge after measurement and battery check. The unit comes with batteries, (six AA cells), a line-voltage adapter for 120/220V ac power and test leads. $738.50. **AEMC Corp,** 729 Boylston St, Boston, MA 02116. Phone (617) 266-8506.

Circle No 167

A/D CONVERTER

We just devalued the µA9708.

It's now down to $1.89 per thousand.



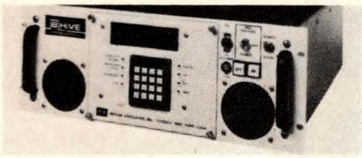
That makes it the lowest-cost multi-channel 8-bit A/D converter in the industry. And price is just one of its important advantages. Here are some others. F3870 and F6800 µP compatibility. High-reliability Bipolar processing. Auto zero and full-scale correction. 300 µs conversion time. ±0.2% maximum linearity over temperature. And 30-volt maximum analog and digital input range.

We'd like to tell you more about our remarkable product at a remarkable price. For a data sheet and an application note that demonstrate the µA9708's incredible versatility, call or write Linear Products at Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, California 94042. Telephone: (415) 962-4903. TWX: 910-379-6435.

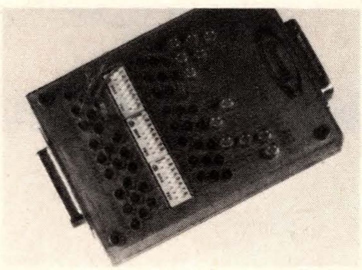
FAIRCHILD

For more information, Circle No 116

New Products



HIGH-VOLTAGE SYSTEM. With installation of any combination of up to 16 high-voltage modules and accessories, the B-HiVe enclosure allows full control of as many as 32 different and independent outputs. A dedicated μC and ROM-based software furnish remote-computer or front-panel control of output voltage and output current limit as well as front-panel or remote digital monitoring of output voltage and current. Available positive- and negative-polarity modules have output-voltage ranges up to 7.5 kV and output-power ranges up to 30W. From $6500. **Bertan Associates Inc,** 3 Aerial Way, Syosset, NY 11791. Phone (516) 433-3110. **Circle No 168**



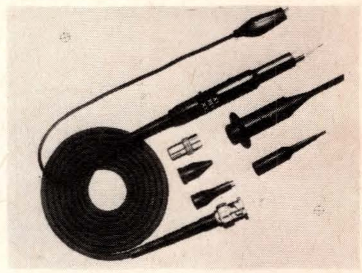
DATA MONITOR. CMC232LT provides an in-line status display and true 3-level monitoring for EIA RS-232 communication lines. Twelve dual-color (red and green) LEDs indicate red for mark (≥+3V) and green for space (≤−3V) and remain unlit for signal levels between +3 and −3V. The rugged, pocket-sized, Lexan-cased unit is powered from the communication lines, eliminating the need for batteries. Each signal line, except line 1 (protective ground) contains a DIP switch that allows it to be opened. $200. **Carroll Mfg,** 1212 Hagan St, Champaign, IL 61820. Phone (217) 351-1700. **Circle No 169**

ISOLATION TRANSFORMER. The PR57 Powerite 400W isolation transformer, line monitor and safety checker allows you to vary the ac output voltage from 0 to 140V and to check leakage (with probe) to the high and low sides of an ac line, reading it directly on a meter in microvolts. You can also use the meter (protected against overload should the probe touch the ac line) to monitor ac-voltage output from 0 to 150V, ac current from 0 to 4A and wattage (in VA) to 470W. The unit is protected by a magnetic circuit breaker and fuse and weighs 18 lbs. $375. **Sencore Inc,** 3200 Sencore Dr, Sioux Falls, SD 57107. Phone (605) 339-0100. **Circle No 170**

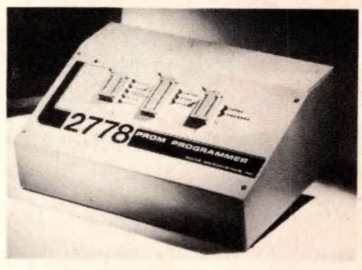
DUAL-OUTPUT SUPPLY. Delivering ±18 to ±24V at 2.4A, continuously variable, the 115W HCC24-2.4 features 115/230V ac ±10% input, ±0.05% line and load regulation and full protection against short circuits and overload. Maximum output ripple is 5 mV p-p, and full-load operating-temperature range is 0 to 50°C, with derated operation to 71°C. The unit meets MIL-STD-810C and carries a 2-yr warranty. $79.95. **Power-One Inc,** Power One Dr, Camarillo, CA 93010. Phone (805) 484-2806. **Circle No 171**

DC/DC CONVERTERS. For vacuum-fluorescent displays, these converters operate from 5V ±0.5V dc and provide a regulated dc output voltage and a regulated, isolated and floating ac output. Ambient operating temperature range is 0 to 50°C. Two converter sizes (C-2, C-3) are available based upon lamp power requirements. C-2, $5.35; C-3, $9.90 (100). **TDK Corp of America,** 2041 Rosecrans Ave, El Segundo, CA 90245. Phone (213) 644-8625. **Circle No 172**

MICRO DEVELOPMENT TOOLS. For 6500 Series μPs, MDT 1000 includes a 54-key keyboard and case, a 12-in. video monitor, dual cassette interface, power supply, EPROM programmer, a 4k-byte static RAM board, a CPU board with both serial and parallel printer interfaces and a video interface. It also provides sockets for four ROMs, system RAM AND ACIA for serial communications and a 4-slot mother board with two sockets installed. Software support comes as 12k bytes of ROM-resident firmware, a 4k monitor with debugging features and an 8k-byte assembler/editor which operates on line-numbered text. $1495. **Synertek Systems Corp,** 150 S Wolfe Rd, Sunnyvale, CA 94086. Phone (408) 988-5690. **Circle No 173**

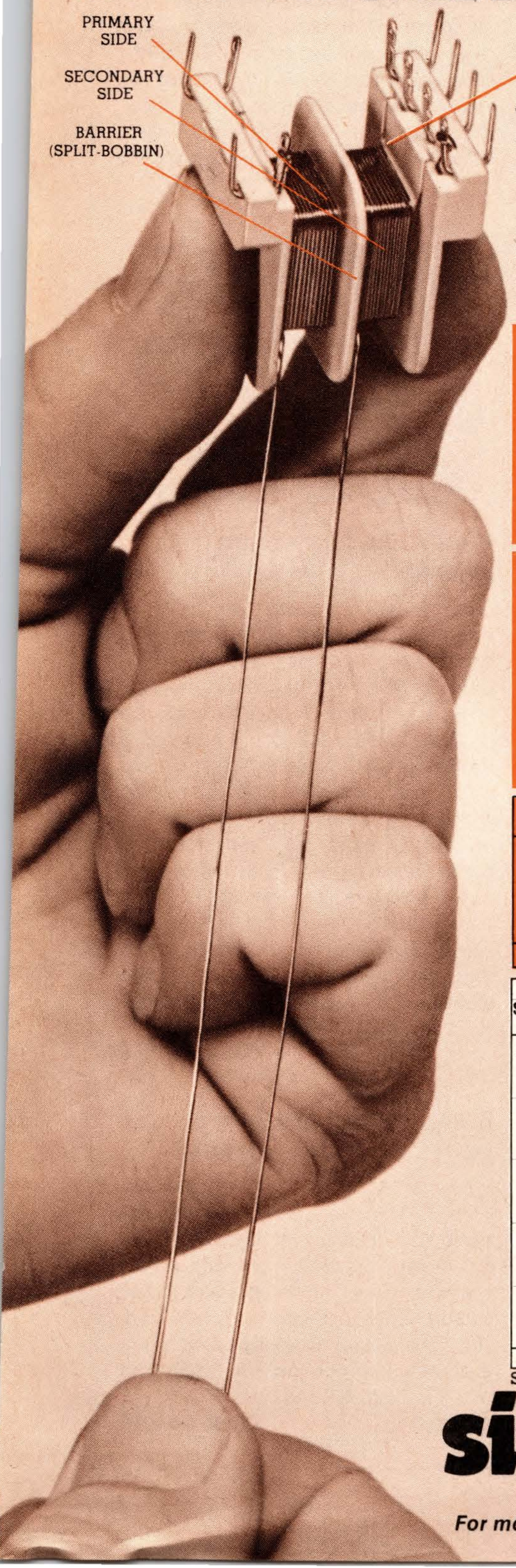


SCOPE PROBE. The SP100's ground-reference switch position allows an oscilloscope input to be grounded at the probe tip, facilitating ground reference location on the CRT display and also serving as a positive means of trace identification. A universal unit, the probe can be used with Tektronix, Hewlett-Packard, Philips and other scopes. Features include rugged and flexible construction, a 100-MHz bandwidth and a 10- to 60-pF compensation range. $36 for the probe with sprung hook, trimmer tool, BNC adapter, IC tip and insulating tip. **Test Probes Inc,** Box 2113, La Jolla, CA 92038. Phone (714) 459-4197. **Circle No 174**



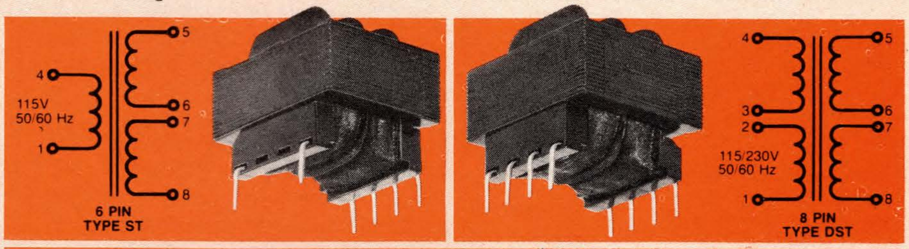
EPROM PROGRAMMER. Model 2778 programs 8k, 16k, 32k and 64k EPROMs, the 8748 μC and the 8755A expansion memory. Operating with the Intellec μC development system, it does not need personality modules; operation is through normal console devices, using software provided (on single and double diskettes) with the programmer. EPROMs that can be programmed include the 2708, 2716 and 2732; TMS 2516, 2532 and 2564; 8741A, 8748, 8755A, Intel 2764 and Motorola MCM 68764. $1295. Delivery, 4 to 6 wks ARO. **Texas Microsystems Inc,** 10530 Rockley Rd, Suite 108, Houston, TX 77099. Phone (713) 933-7503. **Circle No 175**

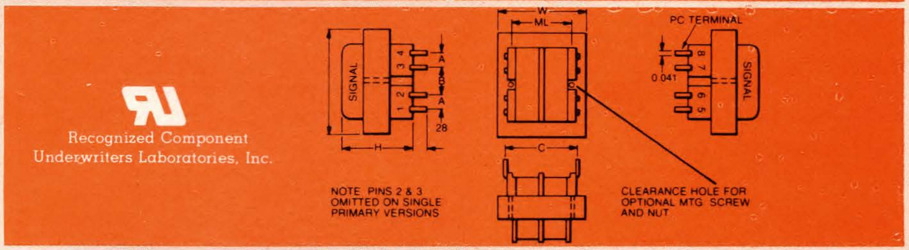
Announcing Split/Tran® — high isolation at prices lower than standard PC board transformers.



Split bobbin design makes the difference

• 2500V RMS HIPOT • NON-CONCENTRIC WINDINGS New from Signal —miniature PC board transformers with high isolation (2500V RMS HIPOT standard) and low capacitive coupling. All this and lower than standard transformer prices, too. Split/Tran is available with single 115V or dual 115/230V primaries. Secondary windings are split, so they can be series or parallel connected. Like all our other transformers and chokes, Split/Tran is always ready for Pronto delivery. Write or call: Signal Transformer Co., Inc., 500 Bayview Ave., Inwood, N.Y. 11696; Tel. (516) 239-7200.





Size	VA	L	W	H	ML	A	B	C	Optional Mtg. Screw & Nut*	Lbs.
3	2.4	1 3/8	1 1/8	1 3/16	1 15/16	.250	.250	1.200	None	0.25
4	6	1 5/8	1 5/16	1 5/16	1 1/16	.250	.350	1.280	4-40 x 1 3/8 Nylon	0.44
5	12	1 7/8	1 9/16	1 7/16	1 1/4	.300	.400	1.410	4-40 x 1 3/8 Nylon	0.70
6	20	2 1/4	1 7/8	1 7/16	1 1/2	.300	.400	1.600	4-40 x 1 3/8 Nylon	0.80

*Available from Signal: Part No. ST-MS (Screw) & Part No. ST-MN (Nut).

PART NUMBER* Single 115V 6 Pin	PART NUMBER* Dual 115/230V 8 Pin	SECONDARY RMS RATING Series	SECONDARY RMS RATING Parallel	PART NUMBER* Single 115V 6 Pin	PART NUMBER* Dual 115/230V 8 Pin	SECONDARY RMS RATING Series	SECONDARY RMS RATING Parallel
ST 3-10	DST 3-10	10V C.T. @ 0.25A	5V @ 0.5A	ST 3-28	DST 3-28	28V C.T. @ 0.085A	14V @ 0.17A
ST 4-10	DST 4-10	10V C.T. @ 0.6A	5V @ 1.2A	ST 4-28	DST 4-28	28V C.T. @ 0.2A	14V @ 0.4A
ST 5-10	DST 5-10	10V C.T. @ 1.2A	5V @ 2.4A	ST 5-28	DST 5-28	28V C.T. @ 0.42A	14V @ 0.84A
ST 6-10	DST 6-10	10V C.T. @ 2A	5V @ 4A	ST 6-28	DST 6-28	28V C.T. @ 0.7A	14V @ 1.4A
ST 3-12	DST 3-12	12.6V C.T. @ 0.2A	6.3V @ 0.4A	ST 3-36	DST 3-36	36V C.T. @ 0.065A	18V @ 0.13A
ST 4-12	DST 4-12	12.6V C.T. @ 0.5A	6.3V @ 1.0A	ST 4-36	DST 4-36	36V C.T. @ 0.17A	18V @ 0.34A
ST 5-12	DST 5-12	12.6V C.T. @ 1.0A	6.3V @ 2.0A	ST 5-36	DST 5-36	36V C.T. @ 0.35A	18V @ 0.7A
ST 6-12	DST 6-12	12.6V C.T. @ 1.6A	6.3V @ 3.2A	ST 6-36	DST 6-36	36V C.T. @ 0.55A	18V @ 1.1A
ST 3-16	DST 3-16	16V C.T. @ 0.15A	8V @ 0.3A	ST 3-48	DST 3-48	48V C.T. @ 0.05A	24V @ 0.1A
ST 4-16	DST 4-16	16V C.T. @ 0.4A	8V @ 0.8A	ST 4-48	DST 4-48	48V C.T. @ 0.125A	24V @ 0.25A
ST 5-16	DST 5-16	16V C.T. @ 0.8A	8V @ 1.6A	ST 5-48	DST 5-48	48V C.T. @ 0.25A	24V @ 0.5A
ST 6-16	DST 6-16	16V C.T. @ 1.25A	8V @ 2.5A	ST 6-48	DST 6-48	48V C.T. @ 0.4A	24V @ 0.8A
ST 3-20	DST 3-20	20V C.T. @ 0.12A	10V @ 0.24A	ST 3-56	DST 3-56	56V C.T. @ 0.045A	28V @ 0.09A
ST 4-20	DST 4-20	20V C.T. @ 0.3A	10V @ 0.6A	ST 4-56	DST 4-56	56V C.T. @ 0.11A	28V @ 0.22A
ST 5-20	DST 5-20	20V C.T. @ 0.6A	10V @ 1.2A	ST 5-56	DST 5-56	56V C.T. @ 0.22A	28V @ 0.44A
ST 6-20	DST 6-20	20V C.T. @ 1A	10V @ 2A	ST 6-56	DST 6-56	56V C.T. @ 0.35A	28V @ 0.7A
ST 3-24	DST 3-24	24V C.T. @ 0.1A	12V @ 0.2A	ST 3-120	DST 3-120	120V C.T. @ 0.02A	60V @ 0.04A
ST 4-24	DST 4-24	24V C.T. @ 0.25A	12V @ 0.5A	ST 4-120	DST 4-120	120V C.T. @ 0.05A	60V @ 0.1A
ST 5-24	DST 5-24	24V C.T. @ 0.5A	12V @ 1.0A	ST 5-120	DST 5-120	120V C.T. @ 0.1A	60V @ 0.2A
ST 6-24	DST 6-24	24V C.T. @ 0.8A	12V @ 1.6A	ST 6-120	DST 6-120	120V C.T. @ 0.16A	60V @ 0.32A

*Explanation of Part Number: Series—ST; Size 4; Series Secondary Volts—36

Special variations will be quoted and shipped promptly.

NET PRICES (1-9 pcs.)

ALL		ALL	
ST-3	$6.04	DST-3	$7.14
ST-4	6.18	DST-4	7.29
ST-5	6.77	DST-5	7.96
ST-6	8.48	DST-6	9.69

DISCOUNT SCHEDULE

10-24	25%
25-49	35%
50-99	43%
100-249	51%
250 Over	Quote

signal TRANSFORMER

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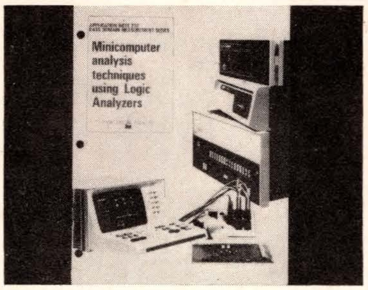
Literature

Maximize printing rate of thermal printheads

Application Report No 10 illustrates how you can maximize the printing rate of thick-film thermal printheads by using external compensation for the physical properties of the printing element. Increasing pulse power and decreasing pulse width offers one solution, which is discussed. The note also explains the use of a positive-temperature-coefficient disc thermistor bonded directly to the back of the heat sink to control temperature. A simple circuit decreases the power in successive print pulses so that a relatively constant print-element temperature can be maintained. **Gulton Industries Inc,** Hybrid Microcircuit Dept, 212 Durham Ave, Metuchen, NJ 08840.
Circle No 236

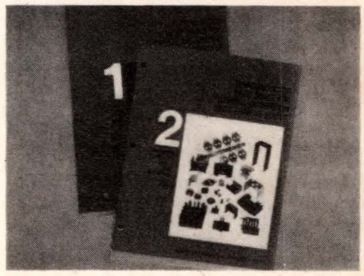


Analysis techniques for troubleshooting minis

"Minicomputer Analysis Techniques Using Logic Analyzers" includes theory and examples of procedures for software evaluation, code optimization, performance analysis and troubleshooting complex digital systems. Ten applications illustrate the use of logic analyzers with system crashes, complex program tracing, asynchronous buses and turn-on failures. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.
Circle No 237

Learn the basics about bubble memories

"Bubble Memory Devices" explains the principles of the magnetic-bubble memory and the technology developed by this company. Chapters include an explanation of what a bubble memory is, what magnetic bubbles are and how to use them for memory applications. The 16-pg booklet also details loop organization and the peripheral circuitry necessary for bubble memories to function. **Fujitsu America Inc,** Component Sales Div, 910 Sherwood Dr-23, Lake Bluff, IL 60044. **Circle No 238**

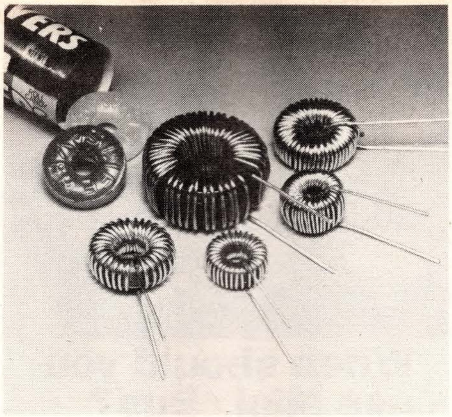


Heat sinks for cooling electronic devices

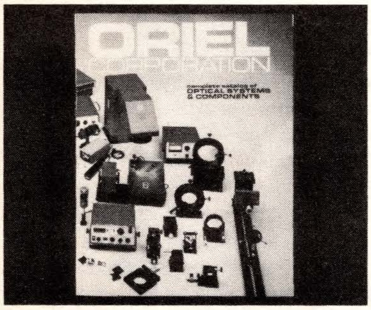
Catalog #1 contains 45 pgs of information and specs for heat sinks that dissipate 10W or more, while the 45-pg Catalog #2 covers devices for applications where less than 10W must be dissipated. In addition to ordering information on a wide selection of heat sinks and extrusions, each catalog contains a compendium section on heat-sink selection and heat-sink performance under both forced and natural convection conditions. The accessories section describes hardware, coatings and thermal compounds used with the company's devices. **EG&G Wakefield Engineering,** 60 Audubon Rd, Wakefield, MA 01880.
Circle No 239

A line of high-efficiency switching power supplies

Brochure 146-1396 covers in detail the RMK/RMX line of single-output designs with output ranging from 30 to 300W. The 4-pg sheet provides input and output characteristics, data on both built-in and add-on EMI-suppression devices, constructional details and outline dimensional drawings. **Kepco Inc,** 131-38 Sanford Ave, Flushing, NY 11352.
Circle No 240



Literature

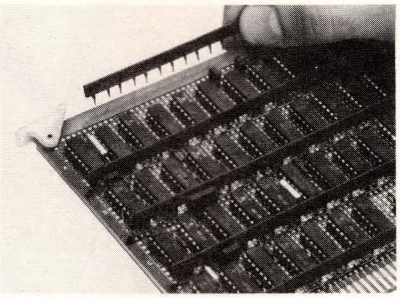


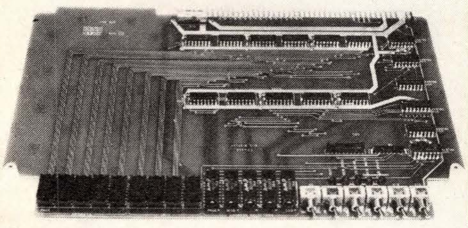
Comprehensive source for optical components

Divided into 10 product categories, this 152-pg handbook details optical benches and accessories; lasers and accessories; precision positioning devices; light sources; monochromators; radiometers and detectors; pulsed-light systems; optical filters; polarizing optics; and optical components and coatings. In-depth specs, features, photos, pricing information and application data combine for complete product descriptions. **Oriel Corp,** 15 Market St, Stamford, CT 06902. **Circle No 241**

Details on IEEE-488 programming procedures

App Note 401-1 explains the principles of programming instrument systems under the control of the company's HP 1000 computer systems, interconnected by means of the HPIB. Chapters discuss how to get started, system preparations, bus status and configuration utility, performance measurements and assigning logical unit numbers. The publication also lists 21 other available app notes, each of which gives specific details on programming an HPIB-interconnected computer system for use with a particular instrument. Request this app note on company letterhead. **Hewlett-Packard Data Systems Div,** 11000 Wolfe Rd, Cupertino, CA 94014. **INQUIRE DIRECT**





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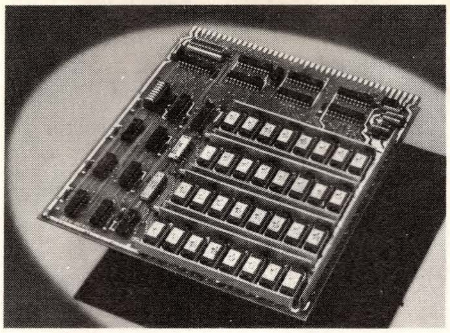

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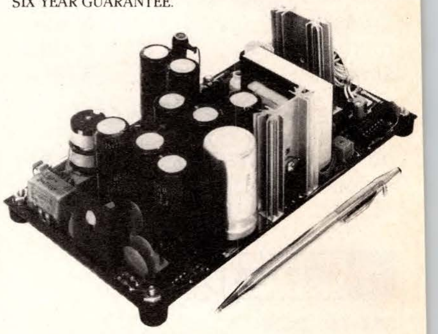

CONVER Corporation
10631 Bandley Drive Cupertino, CA 95014 (408) 255-0151

For more information, Circle No 132

Literature

Questions and answers on automated network analyzer

This 4-pg brochure answers frequently asked questions about the company's automated network-analyzer system for microwave test applications over the 10-MHz to 18-GHz range. It includes details on operation, accuracy, test times, programming, training and prices. Graphics illustrate controls, test sequence, hard-copy output, accuracy characteristics, test setup and system components. **Wiltron Co,** 825 E Middlefield Rd, Mt View, CA 94043.

Circle No 242

New products highlight data-conversion handbook

A 384-pg revised book contains information on A/D and D/A converters, data-acquisition systems, computer analog I/O peripherals, sample/holds, analog multiplexers, op amps, power supplies, dc/dc converters, digital panel meters and printers, digital voltage calibrators and data-logging instruments. Tabular selection guides categorize the broad line of data-conversion devices by performance. In addition, complete data sheets detail key products. **Datel-Intersil,** 11 Cabot Blvd, Mansfield. MA 02048.

Circle No 243

Real-time executive for popular μCs

A 60-pg introductory paper covers organization, design concepts, data structures and major facilities of the REX-80 real-time executive for 8080, 8085 and Z80 microcomputers. It discusses advantages of the real-time executive approach and gives several application examples. $5. **Systems and Software Inc,** 2801 Finley Rd, Downers Grove, IL 60515.

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20,000 ELECTRONIC COMPONENTS AND HARDWARE Specifications, tech. drawings and features proliferate in the new, H.H. Smith Engineering Reference Guide. The 104 page catalog details Smith's state-of-the-art component line and its new Terminal Blocks, Binding Posts, Test Leads, Adapters, Plugs, Jacks. Parts cross index is included. For free copy write: Herman H. Smith, Inc., 812 Snediker Ave., Brooklyn, N.Y. 11207, (212) 272-9400.

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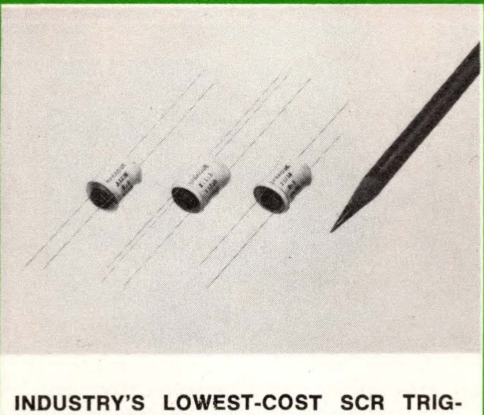

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Advertisers Index

Looking Ahead: Trends and Forecasts

US power-semi shipments to top $1B in 1983

US power-semiconductor shipments to world markets will rise from $894 million last year to $1.1 billion in 1983. Worldwide consumption, however, will increase at an even faster clip—between 10 and 12% annually, predicts Frost & Sullivan Inc.

The causes underlying these impressive gains, according to the New York City-based market-research firm, are manifold: strong industry backlogs, technology advances exemplified by the success of RF transistors in the 15-GHz range, improved product yield and many new applications.

Two major electronics market sectors will contribute heavily to the industry's growth.

• Power supplies: This market, which stood at $2.2 billion in 1978, will jump to $5 billion by 1984. Switching power supplies, in particular, will see a 25% annual growth rate.

POWER-DISCRETE SHIPMENTS BY US COMPANIES TO WORLD MARKETS

($ MILLIONS)	1979	1983
POWER TRANSISTORS		
GENERAL PURPOSE	286	370
RF AND MICROWAVE	74	95
RECTIFIERS		
0.5 TO 3A*	160	200
3 TO 35A	67	87
OVER 35A	63	83
THYRISTORS		
0 TO 55A	100	126
OVER 55A	70	104
ZENER DIODES	102	104
TOTAL POWER DISCRETES	894	1130

*INCLUDES RECTIFIERS OVER 1A, ALL THYRISTORS

POWER-SUPPLY MARKET FOR POWER SEMICONDUCTORS

($ MILLIONS)	1979	1984
POWER TRANSISTORS (INCLUDING DARLINGTONS)	125	245
DIODES/RECTIFIERS	55	90
THYRISTORS	38	65
ZENER DIODES	32	45

SOURCE: FROST & SULLIVAN INC

• Automotive electronics: The automobile market for nonentertainment electronics will rise from $267 million last year to $517 million in 1982.

Despite these significant gains, though, power-semi users will feel a price pinch. Costs will climb along with raw-materials prices, yielding annual price increases between 3 and 5% for established power products over the next 2 or 3 yrs.

Regulations won't stifle printer-paper market

The US computer - printer-supply industry (including producers of paper and ribbons) will grow dramatically over the next 5 yrs, reaching nearly $7.5 billion in 1984. And while alternative output forms such as microfilm and magnetic media will play an important part in office communications, paper will remain the primary tool in the 1980s, according to Creative Strategies International.

The printer-paper market will continue to grow, along with that of printers. However, most paper mills that produce the grades used as printer paper are already operating close to capacity. The San Jose, CA-based market-research firm projects only a 2 to 2½% increase in this capacity over the next 5 yrs, while demand for printer paper is expected to grow 8 to 10%.

Environmental regulations that control air and water pollution will affect this market growth; large capital outlays are necessary to reduce pollutants. In addition to causing an increase in the overall capital costs of paper production, the regulations raise energy requirements.

New laser applications will spur market growth

Portions of the laser market—the reprographics, biomedical, communications, research and point-of-sale sectors—are preparing for imminent and rapid expansion stemming from myriad new applications for these devices.

Gas - laser shipments will undergo significant growth, predicts Frost & Sullivan Inc; carbon-dioxide lasers alone will double in market growth, reaching $67 million during the 5-yr period from 1978 to 1983.

The solid-state-laser market, pegged at $11 million last year, will also more than double, reaching $25 million in 1983. In addition, the market for the Nd:YAG laser, which Frost & Sullivan describes as "a mainstay" in the commercial/industrial marketplace, will rise in total dollar value at an 18% annual rate.

LASER-BASED REPROGRAPHIC-INSTALLATION INCREASE

	1978 THROUGH 1983
TELECOPIERS	317%
COLOR SCANNERS	150%
PLATEMAKERS	400%
LINE PRINTERS	338%
COM	170%
WASHFAX TYPE	4400%
OCR	285%
OTHER	150%

SOURCE: FROST & SULLIVAN INC

Frost & Sullivan warns that semiconductor lasers will pose a long-term threat to HeNe-instrument business growth; it predicts that the former units' current $5.5 million market will approach a 35% annual growth rate through the early 1980s, reaching $20 million in 1983 and $60 million in 1986.

Material for this page developed from *Electronic Business* magazine and other sources by Joan Morrow, Production Editor, and Jesse Victor, Assistant/New Products Editor.

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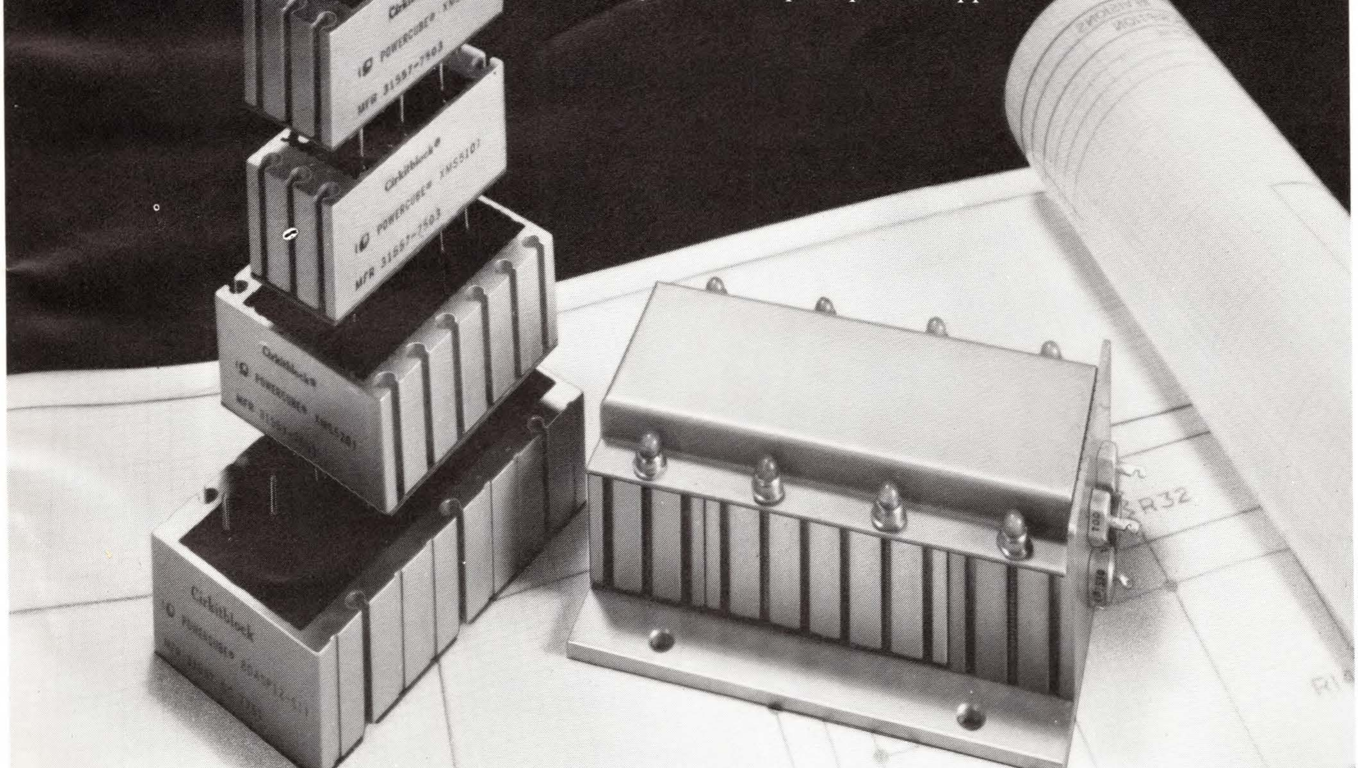

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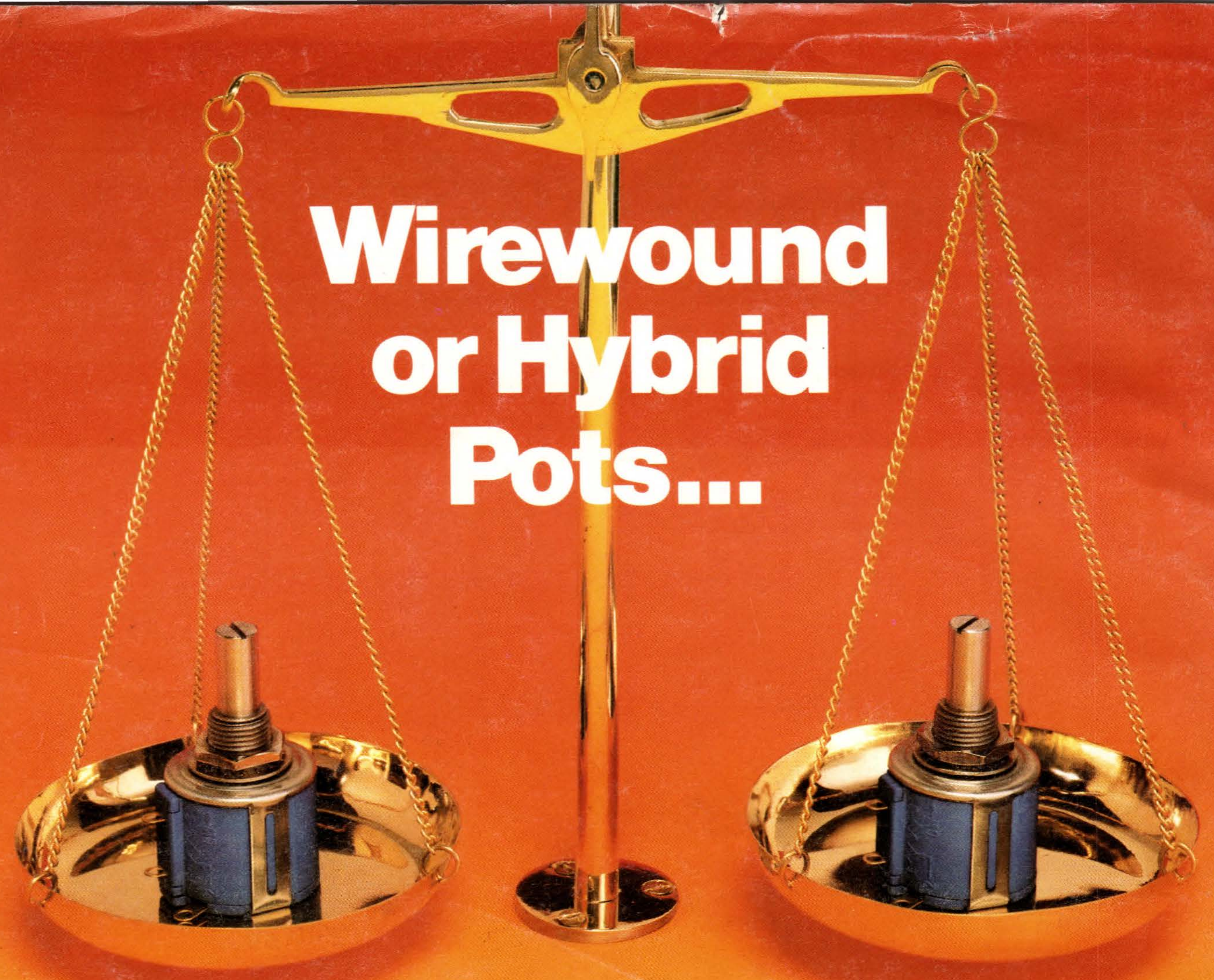

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