

October 1970 / Volume 18 / Number 10



EXCLUSIVELY FOR DESIGN DECISIONS

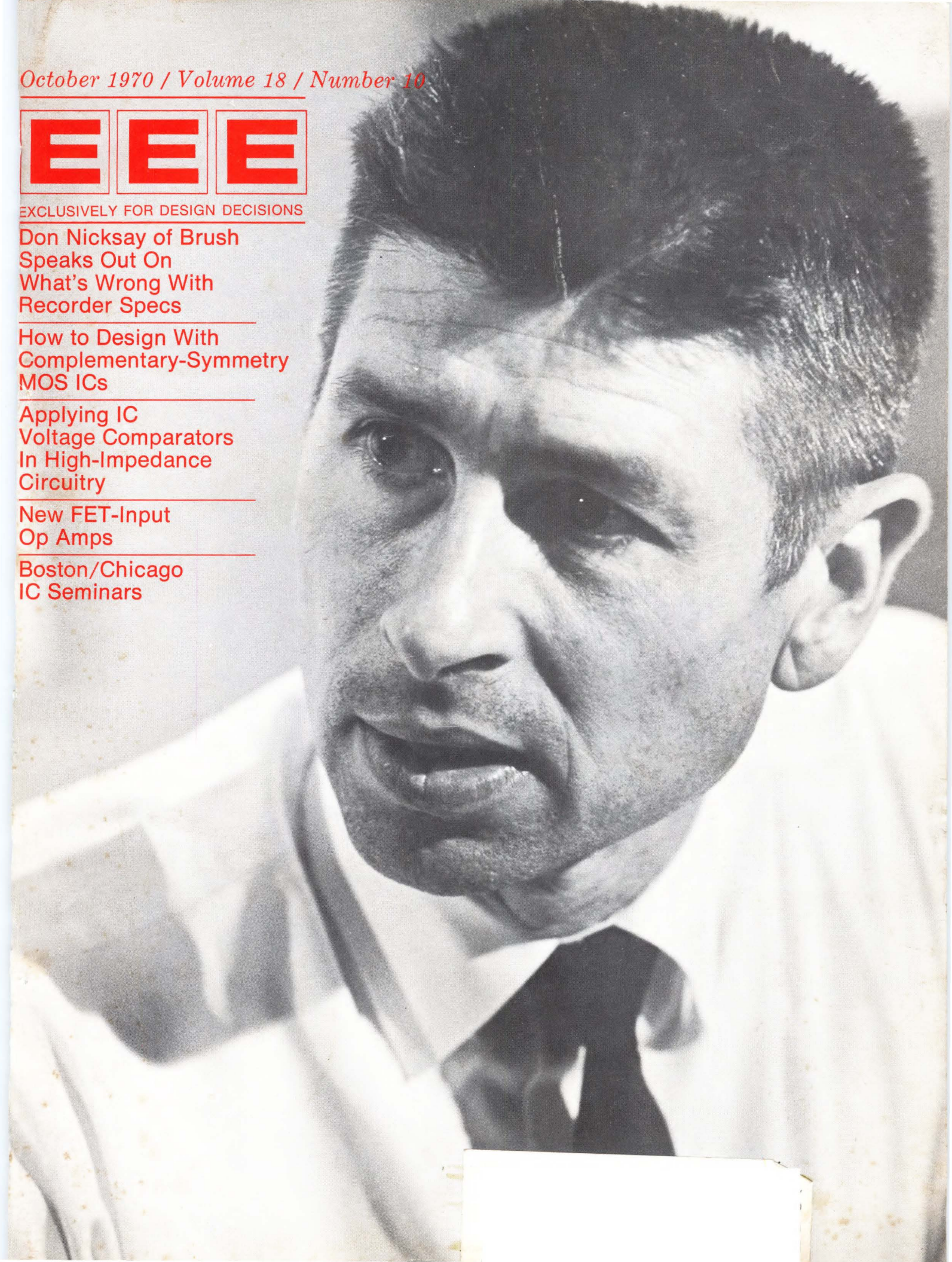
**Don Nicksay of Brush
Speaks Out On
What's Wrong With
Recorder Specs**

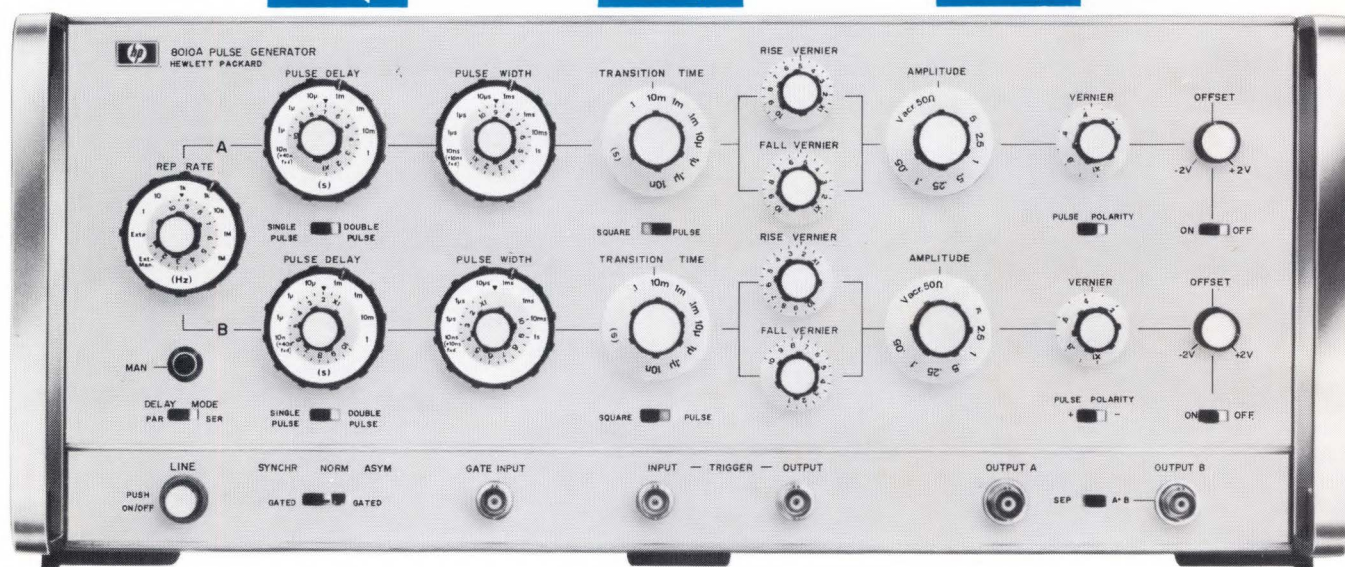
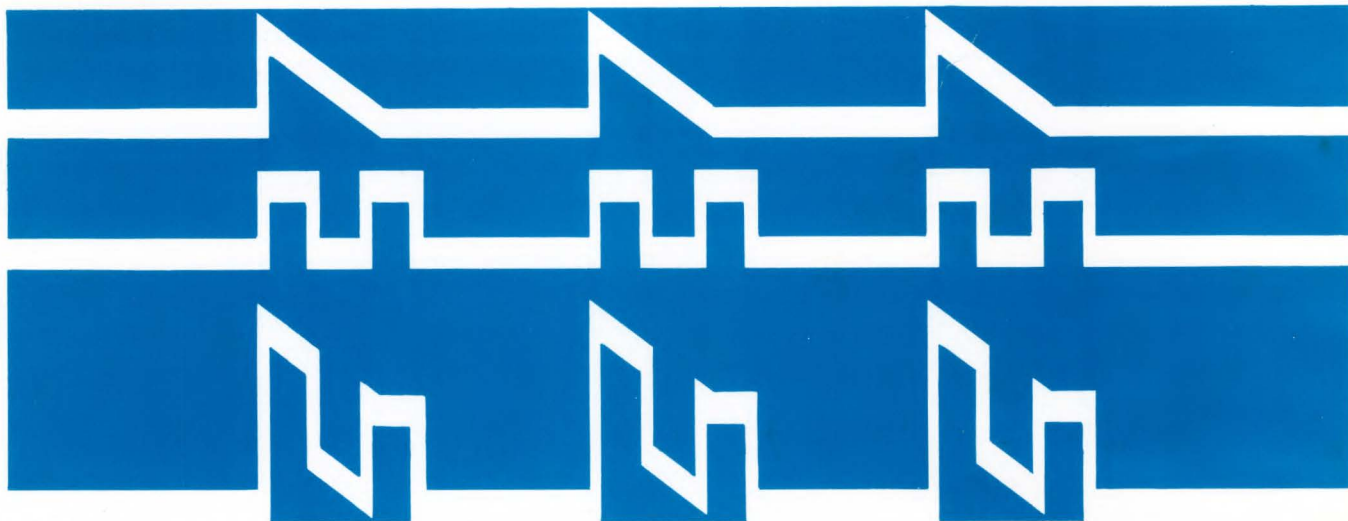
**How to Design With
Complementary-Symmetry
MOS ICs**

**Applying IC
Voltage Comparators
In High-Impedance
Circuitry**

**New FET-Input
Op Amps**

**Boston/Chicago
IC Seminars**





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EXCLUSIVELY FOR DESIGN DECISIONS



Photo by
William Richards
Story on page 34

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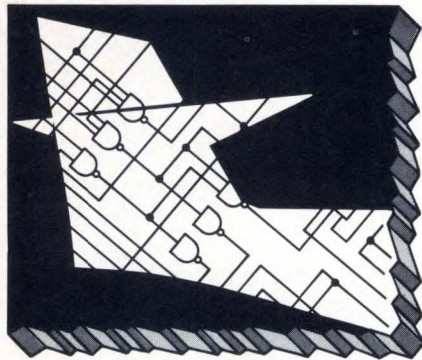
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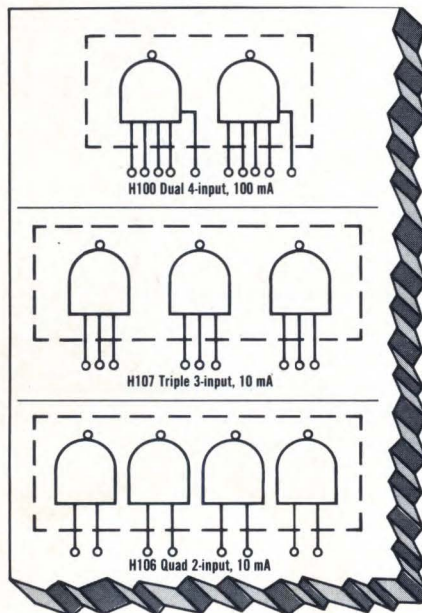
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EXCLUSIVELY FOR DESIGN DECISIONS

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Editorial Objectives

EEE serves electronic design engineers exclusively. EEE restricts its editorial coverage to material that can help engineers make design decisions. Such editorial material is intended to help an engineer:

- Decide for one design technique or design philosophy over another;
- Decide for one measurement technique over another;
- Decide for one packaging technique over another;
- Decide for one systems approach over another;
- Decide for one material, component, packaged circuit or instrument over another.

EEE does not publish general-interest material that cannot contribute to a design decision. Nor does it publish material aimed at peripheral interests of an individual.

EEE is dedicated to articulate expression and clear visual presentation. It is pledged to encourage the exchange of sound engineering ideas.

EEE's editorial pages are open to engineers for bylined articles and correspondence.

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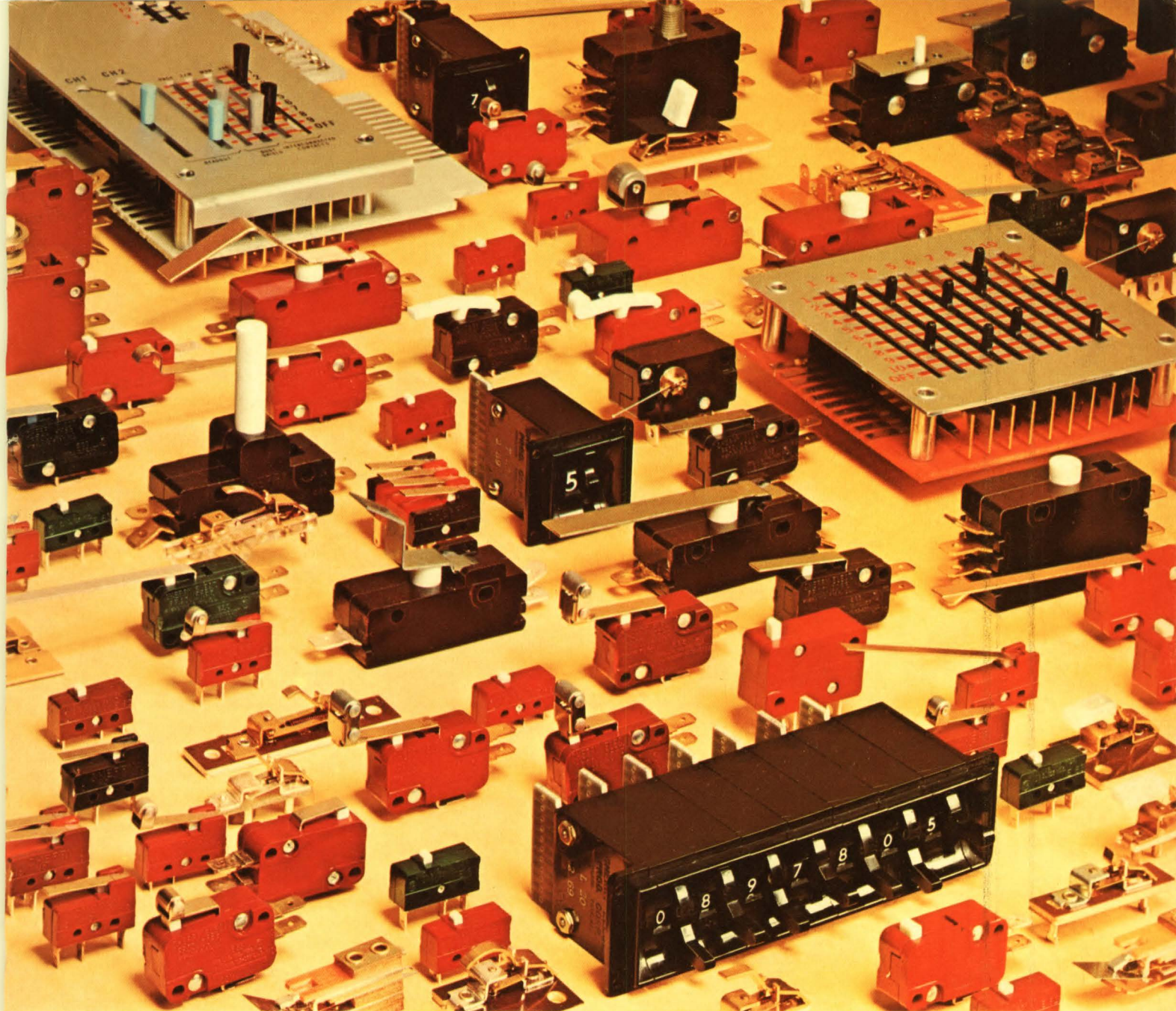
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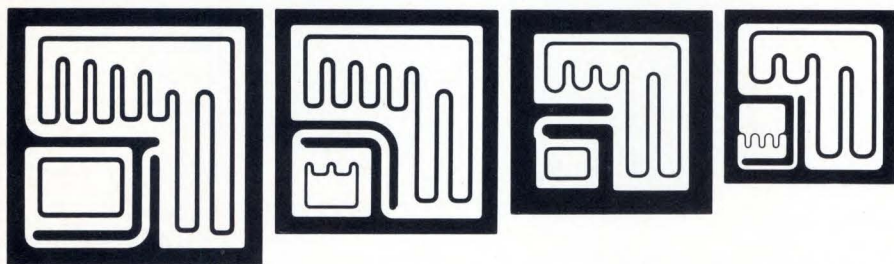
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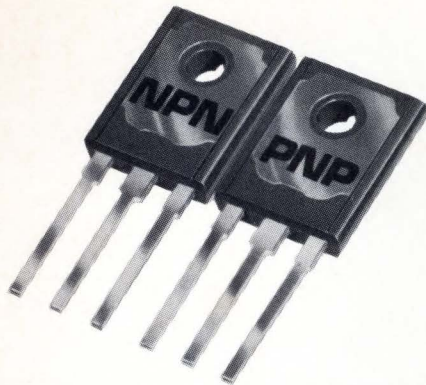
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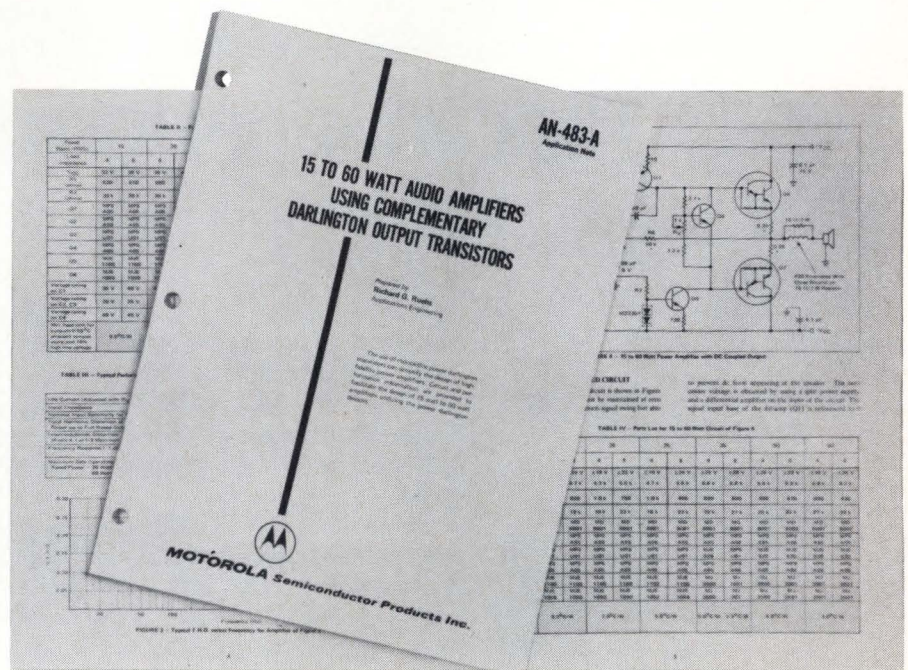


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Want more information on the *Linear Op Amp Family* from Qualidyne? Contact your Qualidyne representative, or contact us directly. If you need data on our diode arrays, monolithic duals, drivers/receivers or semiconductor memories, do likewise.

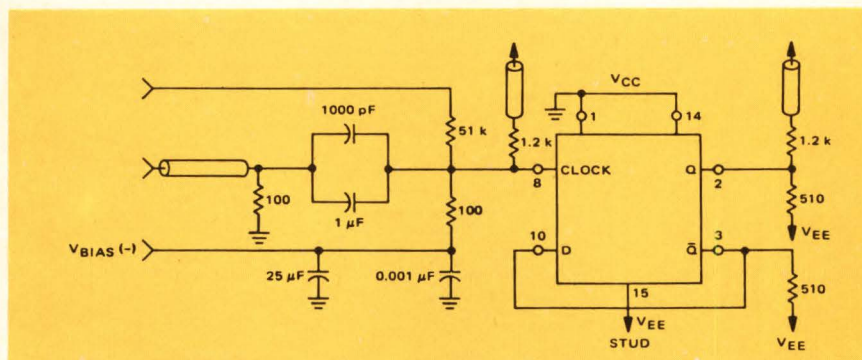
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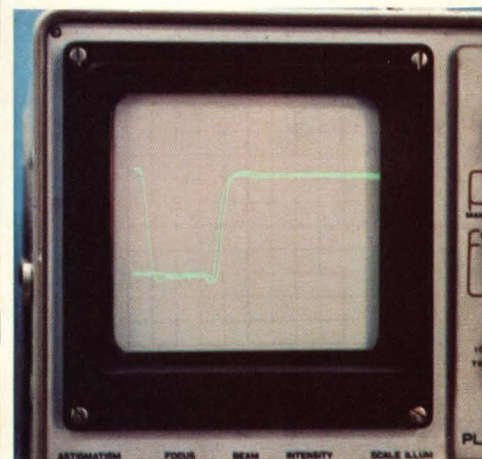
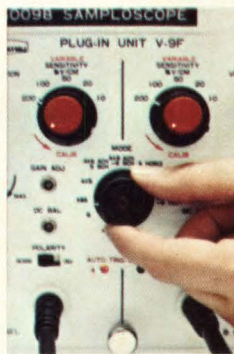
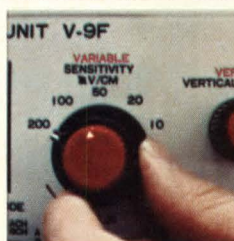
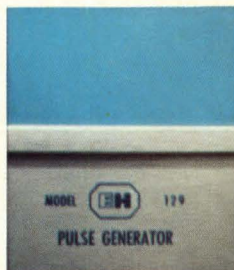
E-H breaks through with the **E-H 129 pulser** which is capable of driving the fastest digital logic circuits. Until this compact, all solid-state instrument came along, no practical commercial pulse generator offered repetition frequency capability beyond 200 MHz. The E-H 129 offers 500 MHz, 2-volt pulses with less than 500 ps risetime and such extras as baseline offset, pulse-top/baseline inversion function, and synchronous gating.

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Circle 105 on Reader Service Card

The background of the entire advertisement is a dense, overlapping field of Intel 2755 chips. These are black, rectangular integrated circuits with gold-plated pins on two long sides. Each chip has the number '1103' and '2755' printed on its surface. The chips are scattered across the entire page, creating a textured, high-tech environment.

THE END

**CORES LOSE
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TO NEW CHIP**

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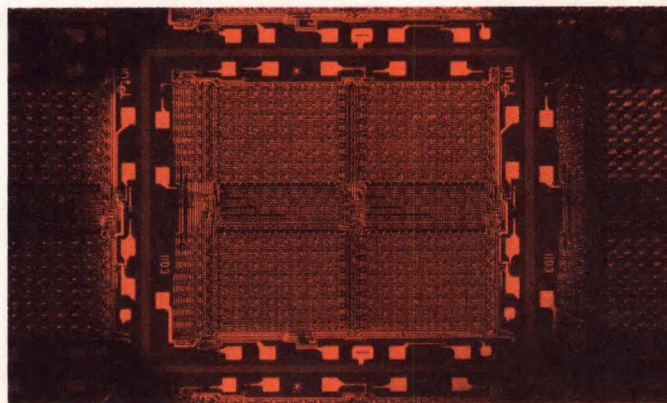
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Intel Corporation is in high-volume production at 365 Middlefield Road, Mountain View, California 94040.



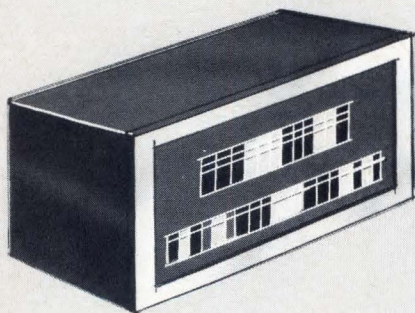
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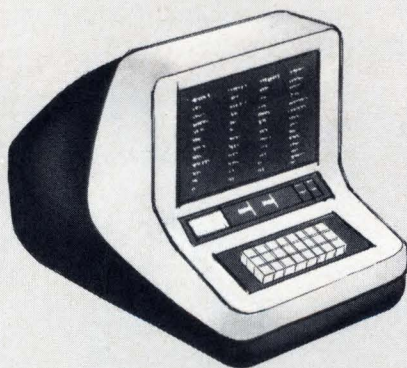
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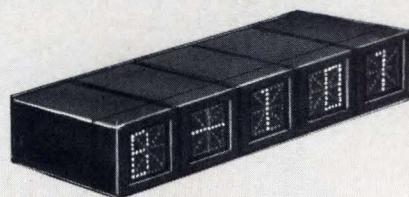
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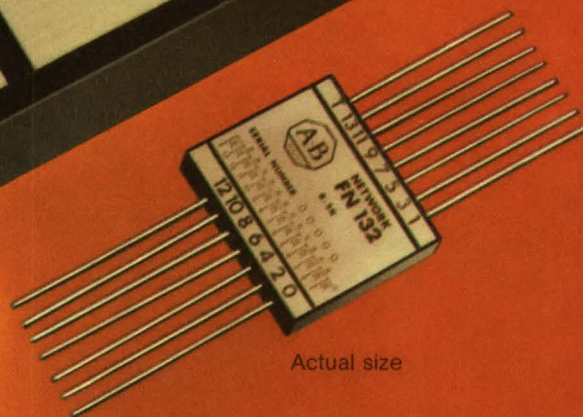
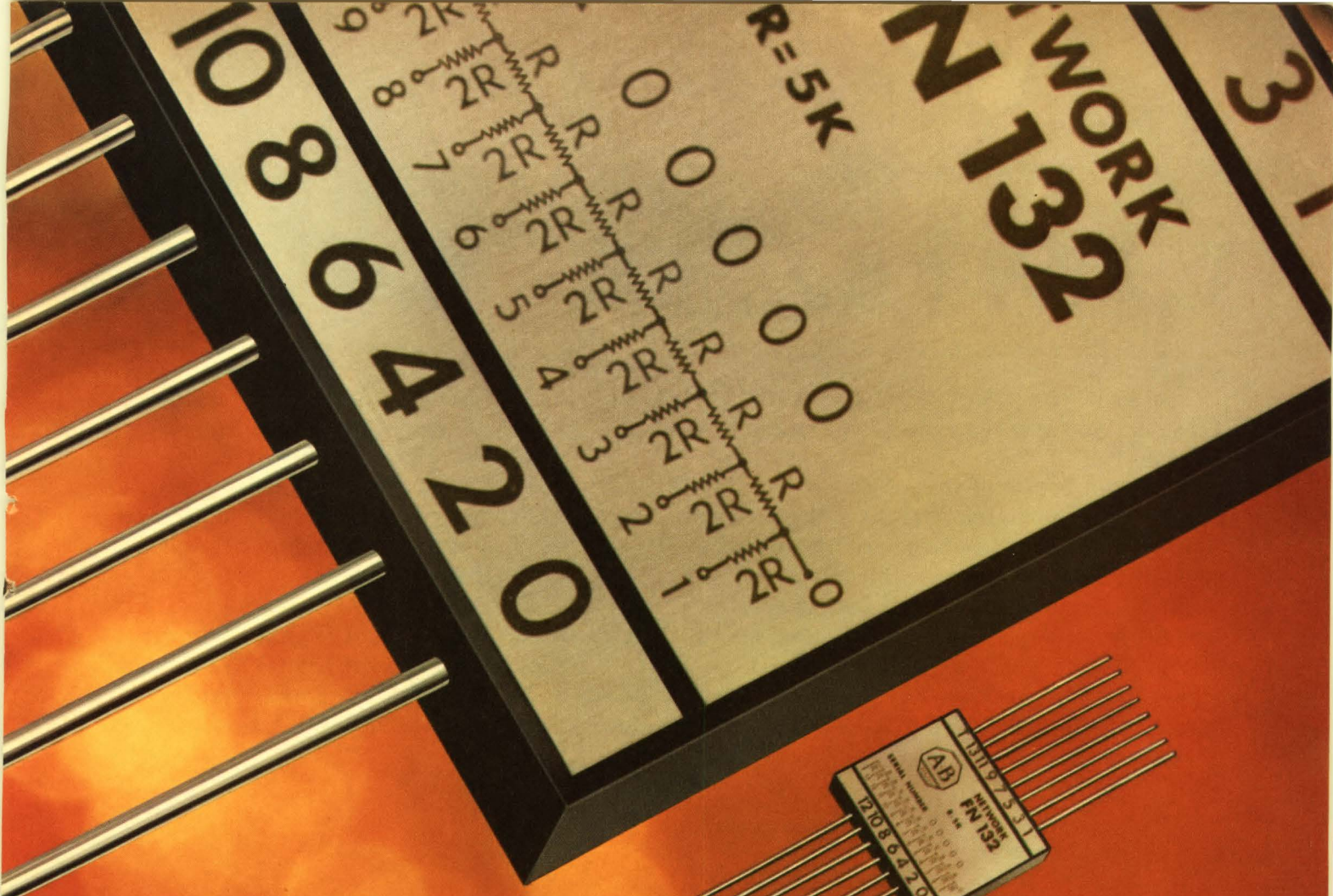
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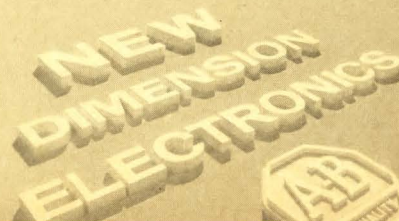
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8T80	High Voltage Quad 2-Input NAND
8T90	High Voltage HEX Inverter

Signetics 

Keeping up on IC "design news"

When EEE staged its first *informal* "no-paper" IC seminar (March 21, 1968, New York City), all 225 seats were sold out in advance. The program consisted entirely of panel discussions on subjects of controversial nature at the time.

Before the program started, some of the attendees wondered if the 15 IC applications engineers on the panel could find enough to say to last seven hours. They did.

EEE's editors found that the program taught us quite a bit — not only about ICs but also about informal seminars. For one thing, we saw that circuit/system designers were looking for circuit/system "design news". IC users were interested in hearing about what other users were doing. It would have been very difficult to prepare papers on this subject but as the discussion moved along, more and more "design news" was revealed.

By design news we mean news about new biasing networks, temperature stabilization techniques, frequency compensation methods, etc. We also mean news of trends among IC users such as what circuit concepts are gaining in popularity: which ones are losing ground. And, what devices are rising in use; also which ones are bombing.

We are going to run a "design news" type of seminar on Friday, November 6 at the new Holiday Inn in Boston. We plan to cover a great many IC subjects — admittedly not spending a great deal of time on any one of them. It's our intention that the attendee should leave the meeting with a better feeling for what's going on concerning the application of ICs.

The theme will be "Designing With Commercially Available Integrated Circuits." A panel of IC applications experts will be on hand to offer their opinions, to talk about the experiences of some of their customers and to debate the best ways for solving various IC problems. Linear and digital areas, including semiconductor memories, will be covered.

A program similar to the Boston one is planned for Chicago on Tuesday, December 8, but in this program there will be somewhat more emphasis on the consumer area. The meeting will be held in the Sheraton-Blackstone Hotel.

The advance admission charge for either meeting is \$35. Checks should be made payable to "EEE Seminars" and mailed to EEE Seminars, 820 Second Avenue, New York, N.Y. 10017. Please be sure to mention for which program the registration applies, Boston on Nov. 6, or Chicago on Dec. 8.



Jerry Eimbinder

JERRY EIMBINDER
EDITOR

ACROSS THE **Editor's Desk**

Call for action

August 25, 1970
Mr. Jerry Eimbinder
EEE Magazine
New York, N.Y. 10017

Dear Jerry:

A CALL FOR ACTION ON BEHALF OF OUR READERS

I am sure you are as concerned as I am about the number of our readers who have lost their jobs in the past year.

We have seen this happen before, and in every case we have all, to a greater or lesser degree, written editorials or otherwise sympathized with those of our readers who were affected.

Most of the past layoffs, however, came during the long economic boom of the 1960's, and we knew that, one way or another, the loss of jobs was temporary because another contract would swiftly come to replace the cancelled one.

Not now. While I admit that the defense cutbacks may be justified, and that a little belt-tightening might have a salutary effect on our industry, I don't see forthcoming any national commitments that would provide jobs for the many unemployed engineers. Moreover, I am greatly concerned that the medicine might be too strong and that our industry may suffer irreparable damage, with the attendant loss of a great number of very competent engineers. These same engineers, who have been responsible for the outstanding accomplishments that have put our country in its present position of leadership, are now wondering whether it was worth the effort, and where will next month's rent come from.

Therefore, this letter contains a call for action. I propose that we editors of electronic magazines request a joint audience with President Nixon, as well as with leaders of both the Senate and the House of Representatives, to explain the seriousness of this situation, the implications it could have for the future of U.S. technology, and, most importantly, to urge the President to set forth new technological goals for peace.

I am sending similar letters to the editors of COMPUTER DESIGN, EDN, ELECTRONIC DESIGN, ELECTRONIC NEWS, ELECTRONIC PRODUCTS, ELECTRONICS, IEEE SPECTRUM, MICROWAVE JOURNAL, MICROWAVES.

Also, the editorial in the September issue of THE ELECTRONIC ENGINEER carries a comment on this proposal, to let our reader know that he can look forward to the press speaking not just to him, but also on behalf of

his interests.

Please let me know your reaction to this suggestion as soon as possible. If you agree, let us get together for a coordinating meeting in New York City (for the convenience of most of the editors I'm contacting).

I am sure you are concerned with this problem. Let us now add action to our concern. If we can help our reader, we will also be helping ourselves.

Alberto Socolovsky
Editor
The Electronic Engineer
Bala-Cynwyd, Pa.

Yes Al, we are concerned. We welcome any genuine efforts to get out-of-work engineers back to gainful employment — both for their sake and the country's.

We hope that your concern is sincere. There is, for example, some question in our minds about your timing. Your readers were informed of your proposal for industry editors to march on Washington in your September issue. Why then did you delay so long after writing the editorial before contacting the editorial fraternity? We hope it wasn't just to make it clear that you originated the idea.

Perhaps you're right that the President and Congress need explanation of the seriousness of the engineering employment situation. Certainly more must be done.

But to say that new technological goals for peace must be set is not enough. Specific programs and recommendations are needed. If you have any specific ideas, we'd like to hear them. If the editors of the electronics industry are to do any good, a practical plan of action must be brought to Washington.

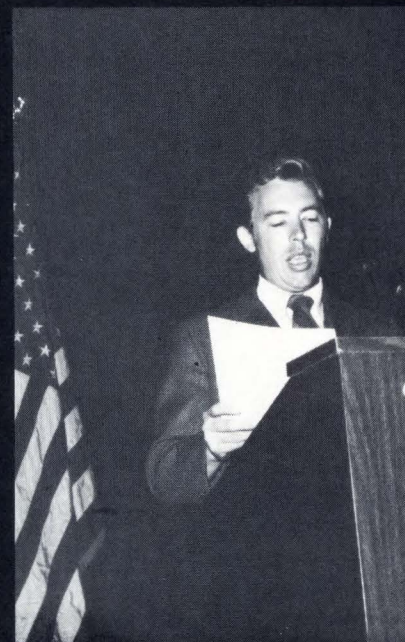
We are willing to participate. We hope that you're doing more than making a grandstand gesture. Tell us how you think this unemployment situation can be eased and we'll cooperate with heart and soul. We're waiting.

DTL has its place

Dear EEE:

Beautiful! Your article by Nick DeWolf in the August EEE is really on target. Everything he says is so true about digital IC speed and the related trade-offs. It was good to see such a practical, down-to-earth discussion of this subject. It certainly confirms my experience and beliefs on the subject.

I have just recently been through the decision-making process on a new



Mike Markkula
of Fairchild Semiconductor

This engineering / engineering management seminar will cover the positive aspects of designing with standard ICs. It'll analyze the degrees of flexibility that different standard ICs provide the circuit/system designer and it'll survey what can be accomplished with existing digital and linear ICs including bipolar and MOS MSI/LSI. The seminar's main goals are to show the IC user the ranges of capability offered by standard devices and the best ways from technical and economical viewpoints, to take advantage of these capabilities.

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Session One

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The controversies concerning which

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of competing IC approaches is best for various systems will be examined.

Session Three

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Friday, November 6
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9:15-11:45 Morning Session
11:45-1:00 Luncheon
1:00-3:00 First Afternoon Ses-
sion
3:00-3:15 Coffee/Coke Break
3:15-4:30 Second Afternoon
Session

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ACROSS THE Editor's Desk

(Continued from page 14)

special-purpose computer design here. My experience and general feelings said to use 930 type DTL. It's plenty fast for what I want to do, and the power supply problems are not as great. But everything still seems to lead me right to TTL. Why? Well, first of all, there's price. The TTL prices are so low that it's hard to fight it. In fact, recent pricing tells me that TTL is now lower than DTL. It's hard to even get an IC salesman to talk DTL. All they do is push TTL with lower prices. That's hard to pass up, especially when cost is a major factor as it is in my project.

Then, second, there is MSI. When an engineer can buy, for example, an 8-channel multiplexer, or an 8-bit shift register in TTL form at a lower cost than the equivalent in DTL circuits and this reduces package count by 70-90%, it's hardly a fight, despite the power supply problems. In other words, with low price and MSI going for TTL, the DTL trend is in for a long gradual downswing the way I see it. What we need perhaps is a line of DTL MSI. Despite all the tradeoffs available to the digital designer, it all boils down to an ultimate decision for TTL in the majority of cases.

But I haven't let it beat me yet. While I did decide in favor of TTL (and I'm not sorry), I did still manage to squeeze in some DTL in strategic places. It definitely has its place. I'm happy with the result, but I'm not too sure I will ever get used to designing without the wired-OR.

Louis E. Frenzel, Jr.
 Assistant Director
 National Radio Institute
 Washington, D.C.

Correction

Dear EEE:

I read with interest the articles on data acquisition in the May issue of EEE (pp. 62-75). While your listing of companies manufacturing data acquisition systems and components appears quite comprehensive and includes two Honeywell listings, I wish to call your attention to an omission: Honeywell Computer Control Div., Old Connecticut Path, Framingham, Mass. 01701. To the best of my knowledge this is the only division of Honeywell manufacturing the type of analog-digital data conversion equipment discussed in your article.

We manufacture and market a complete line of data conversion modules: A-to-D converters, sample-and-hold amplifiers, analog multiplexers, multiplexer sequencers, specialized power

supplies, (designed to power the modules plus additional logic), modular prewired connector planes to accommodate the above and 8, 10 and 12-bit D-to-A converters each packaged on a single PC card including ladder, ladder switches, reference, output amplifier and buffer storage register.

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Dan Strassberg
 Computer Control Div.
 Honeywell, Inc.
 Framingham, Mass.

Watch this

Dear EEE:

This is just to tell you how *much* I enjoyed the article about Hamilton's new solid-state watch in the July issue of EEE.

It's really humorous, and yet it gives a clear technical description of the new device. May I congratulate your author on a refreshingly creative piece of technical journalism.

Blair R. Martin
 IBM
 Binghamton, N. Y.

Filter Comments

Dear EEE:

I'd like to comment on Mr. Perry's statements in the March, 1970 issue of EEE and Mr. Wetherhold's letter in the July, 1970, issue regarding possible errors by Mr. Perry.

It seems to me that since there are standard definitions of insertion loss and attenuation published by both the American Standards Association (ASA C42.65, 1957) and the American Institute of Electrical and Electronic Engineers (AIEE 54 IRE 3.51), these should be accepted and used until such time as they are changed. The following definition, I believe, was originally published in the "Proceedings of IRE, Vol. 42, page 1111, July, 1954: *"Insertion Loss: The insertion loss resulting from the insertion of a transducer in a transmission system is the ratio of the power delivered before the insertion to that part of the system following the transducer to the power delivered to that same part after the insertion."* Definition 65.08.087. *"Foot Note: This ratio usually expressed in decibels."*

This definition was produced by a committee headed by E. I. Green of the Bell Telephone Laboratories and is the same one used in the Bell System for many years. Unfortunately it was not possible to check the latest American National Standard which has replaced the American Standards Association to

see if there has been any change.

It will be noted that nothing whatever is included concerning impedance of any part of the system; thus Mr. Geffe, as quoted by Mr. Wetherhold, is correct. However, since the definition is based on power measurements, it is necessary for the detectors to have the same impedance, before and after insertion of the transducer. This requirement is obviously met if the definition is used literally. Again there are no restrictions on impedance of source, transducer input or output, or load. They can all be different.

Of course it is true that in the majority of communication transmission systems an effort is made to match impedances to eliminate reflections at all junctions. This is vital in transmission of television signals to eliminate ghost images.

According to American National Standard C16.29-1957, paragraph 1.4 on measurements in audio systems, voltage attenuation is defined as "the ratio of the magnitude of the voltage across the input of a transducer to the magnitude of the voltage across a specified load impedance connected to the transducer. By custom, this attenuation is often expressed in decibels by multiplying the common logarithm of the ratio by 20." This corresponds to Mr. Perry's definition of attenuation.

In addition to insertion loss and voltage attenuation, the American National Standard also defines and gives methods of measurement of bridging loss, power loss, transducer loss, transformer loss, and transition loss. It also includes corresponding gain and amplification quantities.

G. W. Pentico
Lee's Summit, Missouri

Dear EEE:

Mr. Wetherhold has touched on a serious problem in communications within our scientific/engineering community (EEE, July, 1970 p. 20).

It is disheartening to receive a report or article comparing "systems" which are so many dB's better or worse than ??? (with reference to what?) What assumptions were made? The example given is for insertion loss in dB's where power is equated to a voltage/resistance ratio compared at two points in a circuit. Using 20 log of the voltage ratio is proper only if the resistances are essentially equal and/or can be ignored. For filter design (insertion loss and attenuation) the resistances can be ignored but what is permissible in this situation by "common usage" cannot be blithely transferred to other design areas (where a criteria may be given in dB's unless the specified or arbitrary references and assumptions are understood).

Sam Perry's basic statements are correct.

Thomas A. Rutter
Rutter and Sons Engineering
Bremerton, Washington

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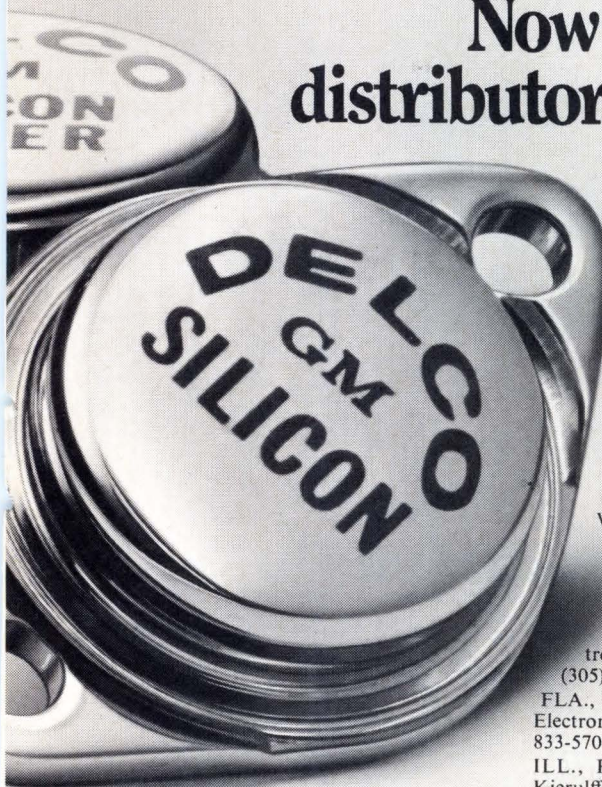


*Circle # 's	Transistor	V _{CEX} Voltage	Con- tinuous I _C	V _{CEO} (sus)	Maximum Power Dissipation	Typical Applications
113	DTS 103	80V	15A	60V	125W	Voltage regulators, power amplifiers, high efficiency switching circuits.
114	DTS 104	80V	15A	60V	125W	
115	DTS 105	100V	15A	75V	125W	
116	DTS 106	110V	15A	80V	125W	
117	DTS 107	120V	15A	85V	125W	
118	DTS 401	400V	2A*	300V		*I _C Peak = 5A Vertical magnetic CRT deflection, has good gain linearity.
119	DTS 402	700V	3.5A*	325V		*I _C Peak = 10A Horizontal magnetic CRT deflection, features fast switching time, high reliability under horizontal sweep fault condition.
120	DTS 410	200V	3.5A	200V	80W	
121	DTS 411	300V	3.5A	300V	100W	Voltage regulator, switching regulator, DC to DC converter, class A audio amplifiers.
122	DTS 413	400V	2.0A	325V	75W	
123	DTS 423	400V	3.5A*	325V	100W	*I _C Peak = 10A High V _{CB0} and V _{CEO} ratings make it practical to operate directly from rectifier 117V or 220V AC line.
124	DTS 424	700V	3.5A*	350V	100W	
125	DTS 425	700V	3.5A	400V	100W	*I _C Peak = 10A High V _{CB0} , V _{CEO} (sus) ratings make them ideal for use in deflection circuits, switching regulators and line operating amplifiers.
126	DTS 430	400V	5A	300V	125W	
127	DTS 431	400V	5A	325V	125W	Voltage regulators, power amplifiers, high voltage switching.
128	DTS 701	800V	1A	600V	50W	Vertical magnetic CRT deflection circuits.
129	DTS 702	1200V	3A	750V	50W	Horizontal magnetic CRT deflection circuits operating off-line.
130	DTS 704	1400V	3A	800V	50W	
131	DTS 721	1000V	3A	800V	50W	High voltage DC regulators.
132	DTS 723	1200V	3A	750V	50W	Very high voltage industrial and commercial switching.
133	DTS 801	1000V	2A	700V	100W	Color vertical magnetic CRT deflection circuits.
134	DTS 802	1200V	5A	750V	100W	Color horizontal magnetic CRT deflection circuits.
135	DTS 804	1400V	5A	800V	100W	
136	2N3902†	700V	3.5A*	325V	100W	*I _C Peak = 10A Ideal for switching applications. Can be operated from rectified 117 or 220 volt AC line.
137	2N5157	700V	3.5A*	400V	100W	
138	2N5241	400V	5A	325V	125W	
139	2N2580	400V	10A	325V	150W	For general use in electrical and electronic circuits such as converters, inverters, regulators, etc.
140	2N2581	400V	10A	325V	150W	
141	2N2582	500V	10A	325V	150W	
142	2N2583	500V	10A	325V	150W	
143	2N3079	200V	10A	200V		
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Progress in Design and Research

FET-input op amp offers low bias current

PROGRESS IN PACKAGED CIRCUITS

A PAIR OF NEW operational amplifiers from Intech have junction-FET input stages, yet their guaranteed input bias current is only 100 femtoamperes (0.1 pA). Thus the new amplifiers, type A-126 and A-127, provide a ten-fold improvement in bias current compared with competing FET-input amplifiers, and they challenge other, more exotic, types of op amps that use MOS FETs or varactors to achieve low input currents.

Challenge to varactors

Amplifiers with varactor bridge inputs (such as those made by Analog Devices and Burr-Brown) can still offer lower input currents than the new Intech units. The AD Model 310, for example, has a bias current of only 10 fA at one input, compared with 100 fA for the new FET-input amplifiers. But var-

actor-input amplifiers usually have asymmetrical input currents. The second input of the AD310 has a bias current of 1 nA, whereas the A-126 and A-127 have symmetrical inputs and can be used in either the inverting or noninverting mode.

Another disadvantage of varactor-input amplifiers is their limited bandwidth. Typically they have full-power responses of only 7 to 80 Hz whereas the A-126 and A-127 can produce full power at 2 kHz.

Yet another possible disadvantage of the varactor-bridge approach is that this type of circuit uses an internal oscillator that must be carefully shielded and decoupled to minimize radiated noise. This situation does not occur with FET-input amplifiers as there is no internal oscillator.

Critics of varactor-bridge amplifiers point out, also, that this type of amplifier achieves low offset voltage by bucking two capacitors against each other. Typically, a change of one percent in the value of one of the capacitors (due, perhaps, to aging or mechanical shock) could produce an offset-voltage change of approximately 15 mV. With a 1000 M Ω summing resistor, this offset change would be equivalent to a current-measuring error of 15 pA. Thus to hold the measuring error to 0.01 pA, the capacitors would need to main-

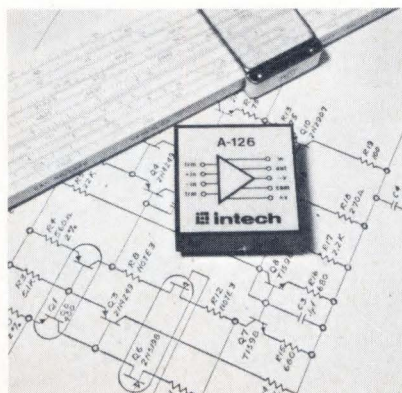
tain their value within 0.0007%.

Manufacturers of varactor-bridge amplifiers respond to the latter criticism by pointing out that FET-input amplifiers also have appreciable offset-voltage drift and, in a high-source-impedance application, could exhibit similar current-measuring errors. The A-126 and A-127 have offset-voltage drifts of 50 $\mu\text{V}/^\circ\text{C}$ and 25 $\mu\text{V}/^\circ\text{C}$, respectively, over the temperature range of zero to +60°C. The initial offset is 1 mV for both versions but can be externally zeroed.

Challenge to MOS FETs


Another possible method of achieving low input currents is to use MOS FETs for an amplifier's input stage. An example of a company using this approach is Keithley Instruments with its model 300 through 302 amplifiers. These amplifiers have input offset currents of 5 to 10 fA. But, though MOS FET amplifiers can offer low input currents and have much better bandwidths than varactor-bridge types, they, too, have some weaknesses when compared with junction-FET amplifiers.

The gates of MOS transistors, unless zener protected, can be easily destroyed by static voltages discharging through the gate-oxide layer. Most suppliers of MOS devices do zener-protect accessible gate terminals. But



(Continued on page 22)

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the diode used for protection introduces leakage current and noise just like any other pn junction. Therefore a MOS input stage will be unreliable if it's not protected, and with protection it can offer no improvement over a small junction FET.

Another disadvantage of MOS transistors is that their gate voltages (V_{GS}) are less stable than those of junction FETs. With MOS FETs, V_{GS} typically shifts several millivolts for normal operation at rated bias conditions. The shift is usually more pronounced and more rapid at elevated temperatures. The cause for the instability with MOS devices is related to oxide impurities, whereas the gate of a junction FET is buried in silicon and is almost impervious to surface conditions. Because MOS gates are sensitive to changes in

bias and temperature, manufacturers of amplifiers using these devices usually specify the amplifier drift that remains after a relatively long warm-up period. But, even after warm-up, drift with MOS-input amplifiers is usually much worse than for JFET-input circuits.

Yet another disadvantage of MOS-input amplifiers is that they have lower common-mode voltage ranges than amplifiers that use junction FETs. This is because the junction FET has a lower V_{GS} than the MOS FET. The new Intech amplifiers have a minimum common-mode voltage range of ± 10 V. The CMRR is typically 100 dB with ± 5 V of common-mode signal at 20 Hz.

Small-geometry FETs

According to Walter Kaelin, Intech's Vice President of Engi-

neering, the company achieved low bias current in the new amplifiers by employing junction FETs having very small geometry and, hence, low gate-leakage current. Also the circuit was designed so that the voltage across the FETs was held to less than a volt, thus further reducing leakage.

Among the other important features of the A-126 and A-127 are a typical input noise voltage of $2 \mu\text{V rms}$ (10 Hz to 100 Hz) and minimum open-loop gain of 100 dB. The operating temperature range is -25 to $+85^\circ\text{C}$.

Both types are packaged in encapsulated modules, $1.125 \times 1.125 \times 0.4$ inches. In quantities of 1 to 9, the A-126 costs \$49.50 and the A-127 costs \$58.50. ■

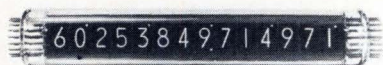
For more information on Intech's amplifiers, circle 341.

Two new multi-digit numeric displays

PROGRESS IN DISPLAY DEVICES

IF ANYBODY IS GOING to take over more of the readout market, Burroughs wants it to be Burroughs. The company dominates the market for single-digit display tubes with its gas-ionization Nixie readout and last year it introduced the Self-Scan panel for large (10 to 18 character) alphanumeric displays. This year, Burroughs and Amperex will fight it out in the market for multi-digit numeric displays. Just weeks apart, Amperex, then Burroughs, introduced the Pandicon ZM1200 and the Panaplex, respectively.

Both devices are aimed princi-



Amperex's 14 digit Pandicon which is equivalent to fourteen decade indicator tubes in one envelope. This display is 1.22 inches in diameter and 6.71 inches long.

pally at the calculator market, but beyond that they have little in common. Both are intended for numerics only, though the Burroughs can display a limited number of alphanumeric characters. Both are intended to time-share a decoder/driver so they obviate a large number of external connections. Amperex sells an IC decoder/driver for use with its Pandicon; Burroughs assumes a user will design or purchase his own, so the company furnishes rather complete application data for use with IC seven-segment decoders (like Fairchild's 9307 or TI's SN7447) plus additional IC gates.

Burroughs and Amperex have taken two different paths in their design approaches. Burroughs' Panaplex is a two-element, cold-cathode, multi-digit, in-plane display housed in a rectangular panel. It's available with 9 to 16 decade characters, each in a 9-segment configuration. (The 9-segment array eliminates the frequent complaints about the right-side "1" in 7-segment displays.)

Each of the nine cathode segments and a decimal cathode is



Burroughs Panaplex panel display uses 9 segments per character. A 12-character display is only 6.2 inches long, 1.62 inches high and 0.4 inches deep.

tied to the equivalent cathode segment of each of the 9 to 16 characters in the display and brought out to termination pins at the rear. In addition, one anode pin is brought out for each character. So a 12-character display would have 22 pin terminations.

In contrast, Amperex's Pandicon is so far available only in a 14-decade version (with 8, 10 and 12 decades to be available soon). Each decade has 10 formed-numeral cathodes (not in-plane), similar to those in the very popular single-decade gas-ionization tubes. Cathodes for

(Continued on page 26)



*“If you’re calling Radiation
and **Harris**
answers...*

Don’t hang up!”



RADIATION MICROELECTRONICS HAS CHANGED ITS NAME TO **HARRIS SEMICONDUCTOR**

NEW PLANT:



HARRIS SEMICONDUCTOR . . . a new name and a new IC manufacturing facility with approximately 113,000 sq. ft. of the latest innovations in wafer manufacturing and development.

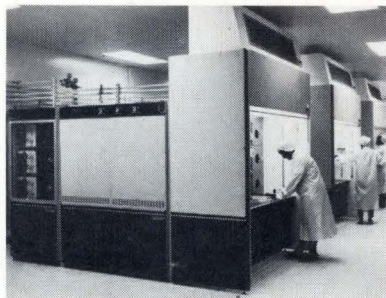
HARRIS SEMICONDUCTOR, the new name for Radiation Microelectronics, is just in time for the opening of one of the most up-to-date IC manufacturing facilities in the country. Smooth production flow and exacting quality control have been the keynote of its design. To assure environmental integrity there are four completely

isolated modules right in the heart of the building: two for wafer manufacturing and inspection . . . one for engineering development and assembly . . . and the fourth for photo-masking and process development. Each has its own vertical laminar-flow ventilation system which blankets the entire module with super-clean air kept at $72^{\circ} \pm 1^{\circ}\text{F}$ and $45\% \pm 1\%$ rela-

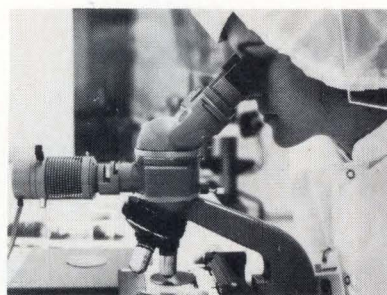
tive humidity. And as added environmental protection, the air is filtered again by the laminar-flow hoods at each individual production station. That assures us of maximum yield for our high-quality chips. And it assures Harris Semiconductor customers that they'll get IC's with the *best price/performance ratio on the market.*



SUPER-CLEAN AIR . . . In vertical laminar-flow hoods designed to provide additional air filtering, wafer photo resist is exposed to ultraviolet light after precise mask alignment.

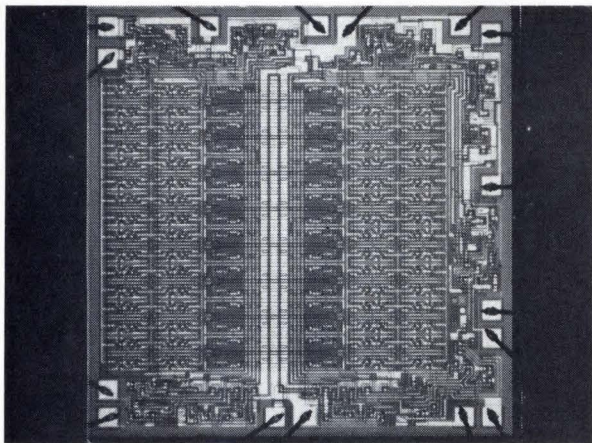


. . . THE LATEST DIFFUSION EQUIPMENT
Six furnace chambers on each of these Brute diffusion systems are regulated within 0.25°C for precise uniformity of wafer diffusion rates.



All material moving through the manufacturing process is continually monitored to assure conformance to the rigid standards of high quality Harris Semiconductor has been noted for.

NEW PRODUCTS

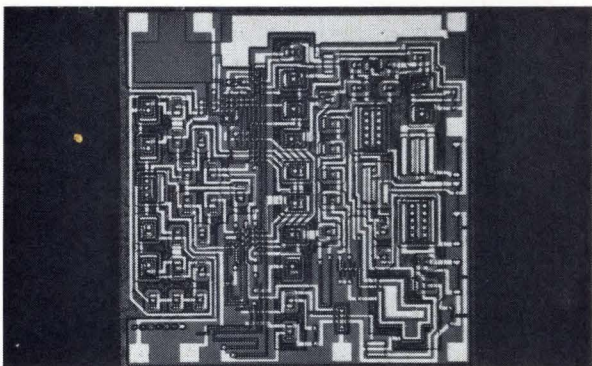


64-BIT BIPOLAR RAM WITH 35ns ACCESS

Using Schottky clamped transistors the Harris RAM-0064 is the first bipolar read/write memory capable of 35ns access times. As a high-speed scratch-pad memory, it provides:

- DTL/TTL compatibility
- Full decoding to 16 words by 4 bits per word
- Uses single 5 volt power supply
- Open collector output for "Wired-Or" expansion
- 16 pin dual in-line package
- 0° to +75°C, \$25.60*
- -55° to +125°C, \$32.00*

*100 to 999 unit price



NEW WIDE-BAND, HIGH-IMPEDANCE OP AMP

Harris' new RA-2620 and RA-2625 Wide Band Op Amps have gain bandwidths which are an order of magnitude better than standard op amps on the market today. In addition, they provide:

- Input impedance of 500Megohms
- Slew rate of 35 V/us
- Typical bias and offset currents of 2nA
- Ideal for high-input impedance comparators
- RA-2620 . . . -55° to +125°C, \$17.85*
- RA-2625 . . . 0° to +75°C, \$10.70*

*100 to 999 unit price

And in addition to our recently introduced PROM and 8-bit D/A Converter, watch for these new products soon to be announced:

MEMORIES

256 x 1 PROM
1024 BIPOLAR ROM
16 BIT BIPOLAR RAM
2560 MOS ROM

DIGITAL

9300 STORAGE REGISTER
9301 1/10 DECODER
9304 DUAL ADDER
9309 DUAL 4 INPUT MPX
9312 SINGLE 8 INPUT MPX
9316 HEX COUNTER

LINEAR

6-BIT CURRENT SOURCE
MONOLITHIC LADDER
NETWORKS

IF
HARRIS
ANSWERS
DON'T
HANG
UP!



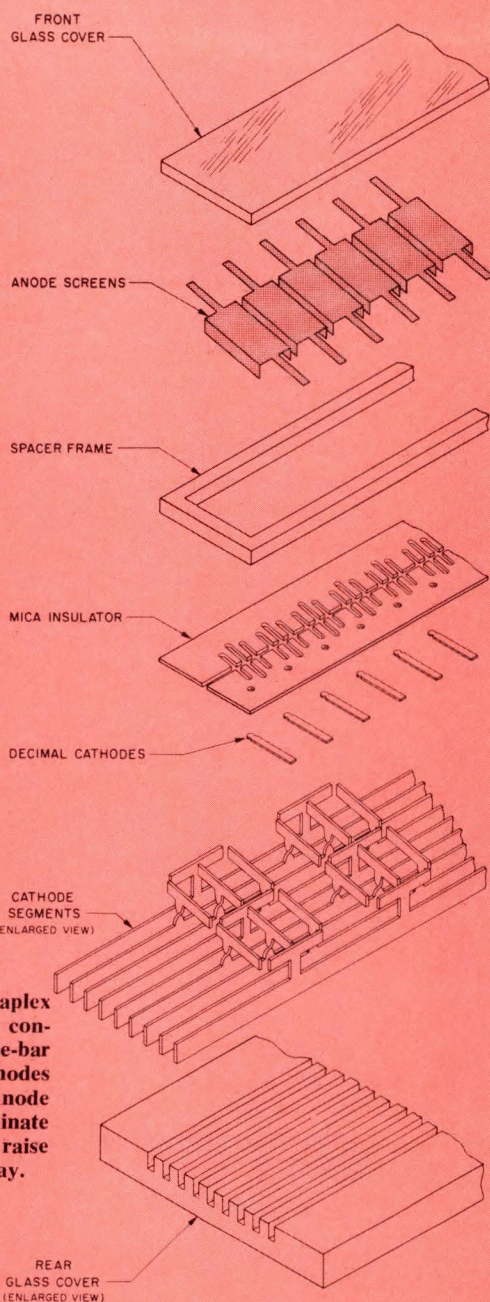
HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

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RADIATION MICROELECTRONICS HAS CHANGED ITS NAME TO **HARRIS SEMICONDUCTOR**



Exploded view of the Panaplex showing: sandwich type construction, commoned nine-bar cathodes, decimal cathodes and individual anodes. Anode tabs and cathode tabs eliminate welded connections and raise the reliability of the display.

each numeral are commoned and brought to pin terminals at one end of the cylindrical tube along with pins for a commoned decimal, a commoned punctuation mark and a single screen (to prevent crosstalk between decades). So 13 pins come out one end of the tube. An additional 14 pins, each going to one anode for each decade, come out the other end.

Thus, both the Burroughs and Amperex displays offer a substantial reduction in the number of pin terminations required per decade over what would be required with individual decade readouts. In both displays, the individual anodes are scanned as the cathodes time-share a common decoder/driver.

Each of the two displays has a character height of 0.4 inch and character spacing of 0.375 inch, center to center. The Amperex numerals are vertical and the Burroughs digits slant. The Panaplex requires 200 Vdc and its rival takes 175 Vdc. Pandicon brightness is 600 candles/meter but brightness data on the Panaplex are not available at this time. A 12-digit Panaplex is 6.2 inches long, 1.62 inches high and a skinny 0.4 inch deep. Amperex's unit is 1.22 inches in diameter and 6.71 inches long.

In the all important matter of price, Burroughs has the lower cost per digit for a 16-decade display, \$1.50 (1000-up), compared with Amperex's \$1.93 (1000-up).

For more information on Burrough's Panaplex, circle 348.

For more information on Amperex's Pandicon, circle 349.

DMM in a scope

PROGRESS IN INSTRUMENTATION

IN MOST RESPECTS, a new dc digital multimeter is quite ordinary. It has the same ranges you'd expect in almost any other; its accuracy is no better than what you find in many competitive units; and its maximum sensitivity, while matching that of most DMMs, falls short of what's found in a few.

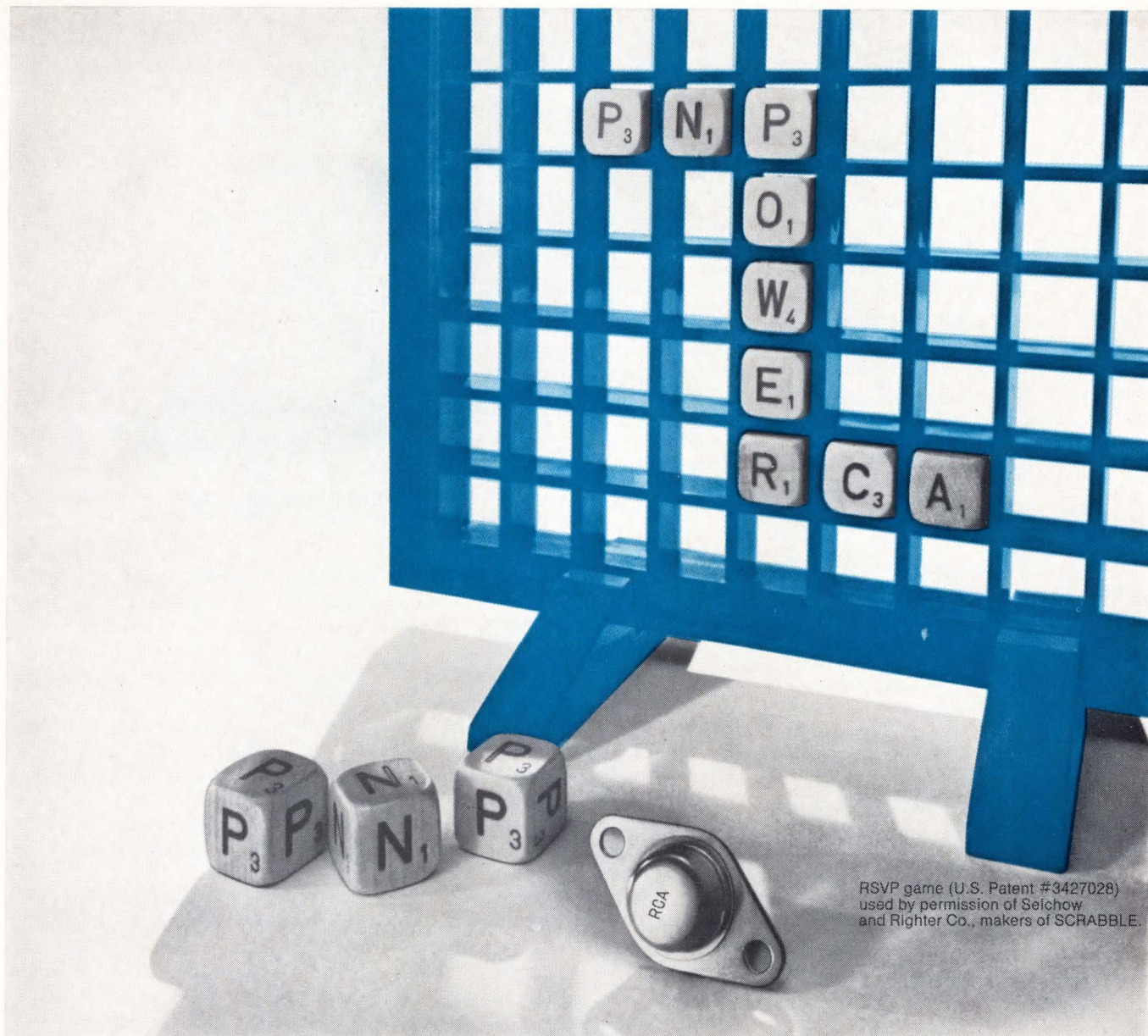
In three major respects, however, the instrument differs dramatically from any other on the market. First, it measures spot temperatures easily and quickly over the broad range of -55 to $+150^{\circ}\text{C}$ with $3\frac{1}{2}$ -digit readout and 1°C accuracy up to 125°C . Second, it provides an analog output of $10\text{ mV}/^{\circ}\text{C}$, which can be used to plot temperature on a chart recorder.

Third, and most challenging, the instrument does not include display devices for its full 3-digit readout plus an overrange "1."

Reads out on a scope

And here's where competitors will no doubt swing at it. For the Tektronix 7D13 works only as a plug-in for one of Tek's five 7000-series scope main frames.

(Continued on page 28)



RSVP game (U.S. Patent #3427028) used by permission of Seichow and Righter Co., makers of SCRABBLE.

You Win With RCA P-N-P Power... New 2N5954 Family (2N3054 Complement)

This new RCA p-n-p transistor has the qualifications that can make winners of you and your designs. The 2N5954 is a silicon power unit in a hermetically-sealed TO-66 package. Complementing the 2N3054 (already widely known in sockets in military, industrial, and commercial equipment), the 2N5954 features controlled second-breakdown ratings. To be sure, each transistor is individually tested to meet specified parameters before it is shipped.

The new 2N5954 family with its multiple epitaxial structure and emitter ballasting techniques add up to a traditionally rugged RCA power device...giving you the design capability to achieve high performance levels in your equipment. One of three new RCA p-n-p types now offered for switching and amplifier applications, 2N5954 (or its family types, 2N5955 or 2N5956), together with its n-p-n complement, provide bi-directional control and phase inversion advantages.

P-n-p/n-p-n complements are particularly advantageous if you're trying to cascade four or five stages. In a power supply design, for example, the use of complementary types can eliminate voltage build-up that would be encountered if cascaded n-p-n, or cascaded p-n-p types were employed.

Check the chart on these new types. For more information, consult your local RCA Representative or your RCA Distributor. For technical data, write: RCA Electronic Components, Commercial Engineering, Section 51J/UT8, Harrison, N. J. 07029. In Europe: RCA International Marketing S.A., 2-4 rue du Lièvre, 1227 Geneva, Switzerland.

Type No.	V_{CB0} (V)	V_{CEX} (sus) (V)	V_{CER} (sus) (V)	V_{CEO} (sus) (V)	I_C (A)	P_T (W) @ $T_C = 25^\circ C$
2N5954	85	85	80	75	-6	40
2N5955	70	70	65	60	-6	40
2N5956	50	50	45	40	-6	40

RCA

Its digital readout appears on the screen of the CRT, traced there by the character generator that Tek uses for automatic scale-factor readout.

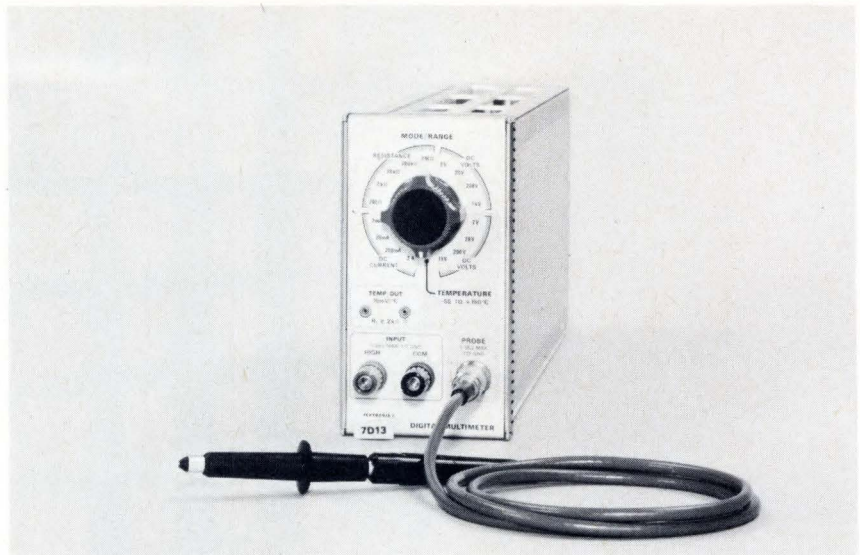
This can be extremely handy when a man uses a scope camera for permanent records of readings. And it can be convenient for a man who already owns or plans to get a 7000-series scope. But it can be argued that a man who's happy with the scope he has now may not be eager to shell out \$560 for a DMM plug-in plus \$1775 to \$3200 for a main frame (unless he's hungry for digital temperature measurements) when he can buy a digital multimeter (Honeywell's French-made Digitest 500) for as little as \$250.

Now it's true that the Honeywell meter, the lowest-cost DMM on the market, has drawbacks. (See "Many tradeoffs in smallest, lowest-cost DMM," *EEE*, October 1969, pp 32-34.) But it measures ac voltage and current as well as dc voltage, current and resistance. Tek's 7D13 measures only the dc parameters.

The Tektronix plug-in offers greater resolution, since it provides an overrange "1" in addition to the three full digits on all but the 1-kV range. Honeywell provides no more than three full digits but almost all other DMMs on the market include the overrange digit.

Most popular ranges only

Further, while the Tek unit covers the most popular dc-voltage, current and resistance ranges, many competing meters cover more. For example, the lowest voltage range is 2 V (which is equivalent to what oth-



Not merely another scope plug-in, this one is actually a digital multimeter — unique in providing digital measurements of temperature, too.

ers might call 1 V with 100% overrange), while several other meters have 100-mV ranges. The lowest current range is 2 mA (or 1 mA with 100% overrange) while others feature 100 μ A. The lowest resistance range is 200 ohms — and that's dandy. Only two meters (from Dana and Non-Linear Systems) have 10-ohm ranges and a brand-new Dana, the 4800, includes a 1-ohm range as an option.

Tek's top ranges are 1 kV, 2 A and 2 M Ω . Accuracy, from 15 to 40°C, is 0.5% rdg \pm 1 count for current and resistance, 0.1% rdg \pm 1 count for voltage. Input resistance is 10 M Ω for all voltage ranges and 0.2 V/full-scale current for current ranges.

The plug-in has two identical sets of dc-voltage ranges, one for use with a pair of test leads and one for a shielded probe, which Tek provides.

This probe also provides the

unique temperature-measurement capability. When the probe is used to measure temperature, the tip and a transistor built into the probe are heated or cooled by whatever is touched. Two currents from the plug-in are switched at a 40-kHz rate to supply different I_C values to the transistor. The difference between the resulting two V_{be} values is very linear with respect to temperature.

Actually, it's not even necessary to use the probe. One can use almost any transistor, mounted anywhere, and run wires to the probe input. For a worst-case temperature swing, the instrument requires about 10 seconds to settle at the proper temperature reading within the accuracy band.

The 7D13 costs \$495 without the voltage/temperature probe, \$560 with it.

For more information, circle 339.

Fast, tough-test LSI tester

PROGRESS IN INSTRUMENTATION

TWO NEW LSI TESTERS offer remarkable test speeds and impressively rigorous test patterns that may allay the concerns of many users that LSI can't really be tested.

The machines, Doctor 32 and

Doctor 64 from Adar Associates, derive great flexibility and the formidable test patterns from a microprogrammed address generator, which works from a Digital Equipment PDP-8 computer.

The advantage of using the address generator for pattern preparation, rather than the com-

puter itself, is that one can feed it a formula for the required word patterns, rather than the explicit address sequences. This simplifies computer programming and slashes the computer's memory requirements. It also saves a great deal of time and this accounts, in

(Continued on page 30)

That #!☆?!*! MIL-M-38510!

There, there, Signetics understands.

We not only understand MIL-M-38510, we can supply IC's to it. Right this minute.

Fact is, we've been using just about the same hard-nosed testing procedures it calls for, for better than five years.

Signetics S. U. R. E. program (Systematic Uniformity and Reliability Evaluation) includes practically all the Military Standard 883 tests plus a few more of our own.

So: send for our new Confidence Report on 38510/883 and for our new S. U. R. E./883 brochure.

And specify Signetics digital and linear circuits for your high reliability requirements.

You'll swear by them.

Signetics

Signetics Corporation / 811 E. Arques Ave., Sunnyvale, California 94086 / A subsidiary of Corning Glass Works

Circle 150 on Reader Service Card

part, for the very high speed of the Adar systems.

The address generator, based on a solid-state random-access memory with 16 12-bit microinstructions and looping capability, can prepare word patterns that

really put an LSI array through its paces. For example, it can generate a checkerboard pattern (with alternating ones and zeros in an array). An even nastier test includes "walking" ones and zeros.

This test involves writing a zero in a cell, writing ones around that cell many times, then checking the original cell for zero retention. This is followed by a ones-retention test, in which a one is surrounded by zeros. Repeated for every accessible cell in an array, this process is a dandy check for sensitivity to multiple-write disturbances.

While both Adar machines are intended for only functional (go/no-go truth table) testing and parametric testing (with actual measurements of voltage and current levels), the instruments can cheat a bit and simulate dynamic testing (involving time-related tests).

This is done by advancing or retarding one phase of the system clock in increments as small as 0.5 ns until a timing sensitive cell in an array just fails to switch. Doctor has a four-phase clock, a variable-width strobe and two timing signals, all derived from a sawtooth generator. Any phase relationship is established by detecting two user-defined volt-

age levels on the sawtooth as the stop and start times. The clock can operate in a continuous or burst mode.

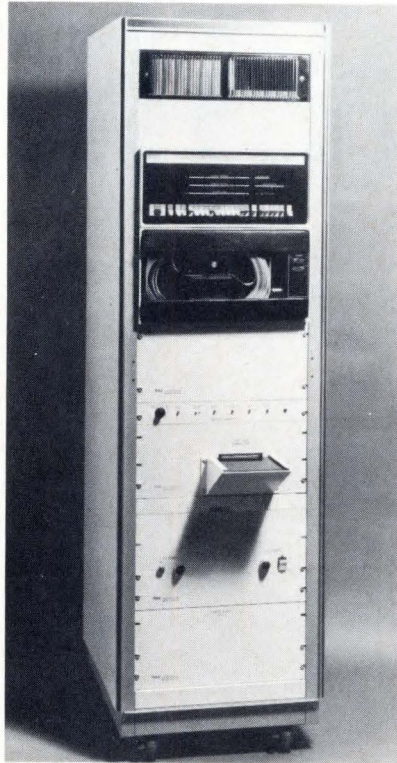
Doctor 32 (for devices with up to 32 pins) and Doctor 64 (for up to 64 pins) have cycle times as snappy as 125 ns and operating speeds to 8 MHz. Their drivers can whip out rise and fall rates of 1 volt per nanosecond at levels that can be set from -17.5 V to +17.5 V. Overshoot and undershoot are typically less than 0.1 V.

The 32 is intended mainly for testing ROMs, RAMs and shift registers while the 64 tests logic arrays, too. The smaller machine senses a single bit position in one reading, so a device with eight output bits requires eight tests. The larger one can multiplex four outputs into each of 16 sensors so, in effect, it senses all outputs of a 64-output device in four passes.

Either machine can be time shared—the 32 by up to eight independent test heads and the 64 by up to four—including wafer probes. Switching time between test heads, about 10 milliseconds, is brief—but long enough to reduce the overall test rate.

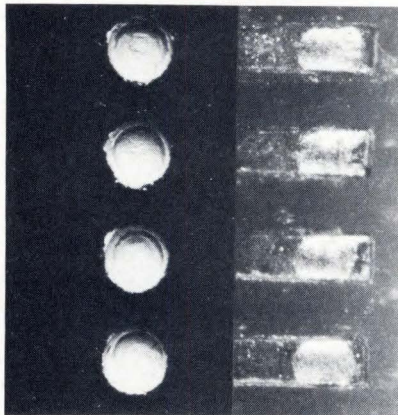
The Doctor 32 starts at \$61,400 while the 64 starts at \$75,600. ■

For more information, circle 343.



The Doctor 32, smaller of two LSI testers from Adar, has no knobs. It's completely under computer control.

A solderless connector for LSI/MSI IC flatpacks



The photograph (magnified 10 times) shows the contact areas of a tin-lead coated pc board after thermal cycling, vibration tests and an equivalent 5 year salt solution aging test. Note that the actual contact areas were unaffected by corrosion due to the gas free seal provided by the elastomeric contacts.

PROGRESS IN PACKAGING

HAVE YOU EVER unsoldered a flat-pack-type IC from a printed circuit board? For the unskilled, the results are usually disastrous and even skilled personnel can end up butchering both the IC and its mating board. Chomerics, Inc., Woburn, Mass., a company ordinarily thought of as an EMI-shielding material supplier, has done something to eliminate this slaughter of ICs and boards. Chomerics, has designed a completely new way of attaching a flat pack to a pc board.

In the new method, the flat pack is placed within an elastomer-contact connector, which in turn mates with the pc board.

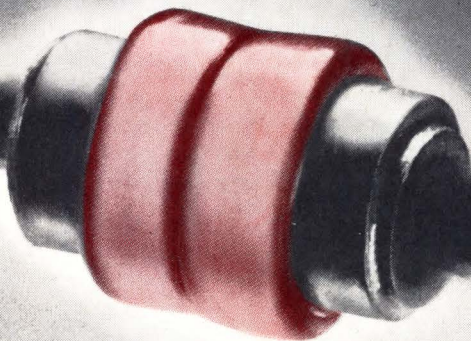
This new unit eliminates soldering, plated-through holes and doubles as an IC carrier. The flatpacks may be easily replaced and can be tested while inside the Chomerics connector. The connector has excellent vibration isolation by virtue of the elastomeric material used and can be designed for any lead format. The contact between the pc board and the connector is a copper to conductive plastic type, which eliminates metal to metal corrosion and formation of gas pockets. The connector has no effect on the IC's frequency cut-off and rise time.

The figure illustrates an exploded view of the new con-

(Continued on page 32)

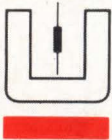
¢-LINE ZENERS 19¢

surge protection
doesn't
cost you more...



and it's nice to know it's there.

For the same prices as plastic devices, you can get up to 5 times greater surge protection. In fact, you can use ¢-line 1 and 5 watt zeners instead of conventional 10 and 50 watt chassis mounted types. And for far less money. Unitrode's unique fused-in-glass construction assures you of monolithic, void-free zener diodes with permanently stable electrical characteristics. And they'll withstand voltage surges high enough to make them hot enough to glow. They're in stock now, ready for immediate delivery. (1 watt ratings as low as 19¢ in 100k lots.) Can you afford not to use them? For fast action, call Sales Engineering collect at (617) 926-0404
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UNITRODE quality takes the worry out of paying less.

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☐ Please send ¢-line zener samples in ☐ 1 watt, ☐ 5 watt rating with complete specifications.

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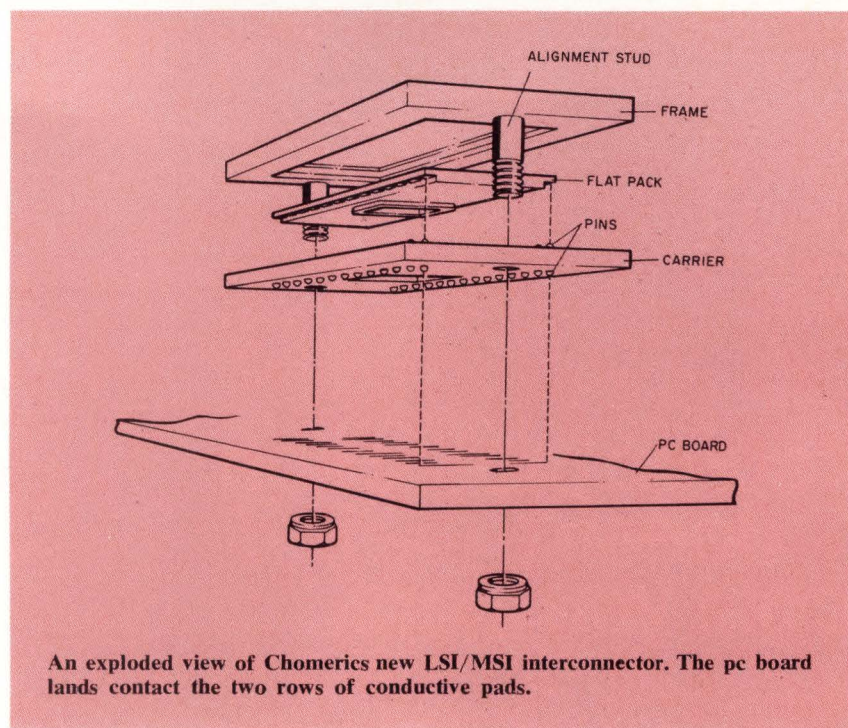
COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

nector (or socket) and a mating pc board. The connector is composed of two pieces: a top frame with alignment studs and the IC carrier which has two rows of conductive pads. These pads extend completely through the carrier portion of the device. In a complete assembly, the IC is placed on the carrier and its leads are aligned with the conductive pads. Then the frame is placed over the carrier piece and the pc board is positioned under the connector. The studs of the top piece align the entire assembly and the addition of two lock-nuts under the pc board complete the assembly. The alignment is such that the IC leads contact the conductive pads which in turn bear down on copper lands or segments of the circuit board.

The heart of the connector is the elastomer contact, a silicone and metal mixture which has a maximum resistance of 0.25Ω per pin and a contact rating of 30 mA. Chomerics has simply drawn on their experience in conductive materials and ap-



An exploded view of Chomerics new LSI/MSI interconnector. The pc board lands contact the two rows of conductive pads.

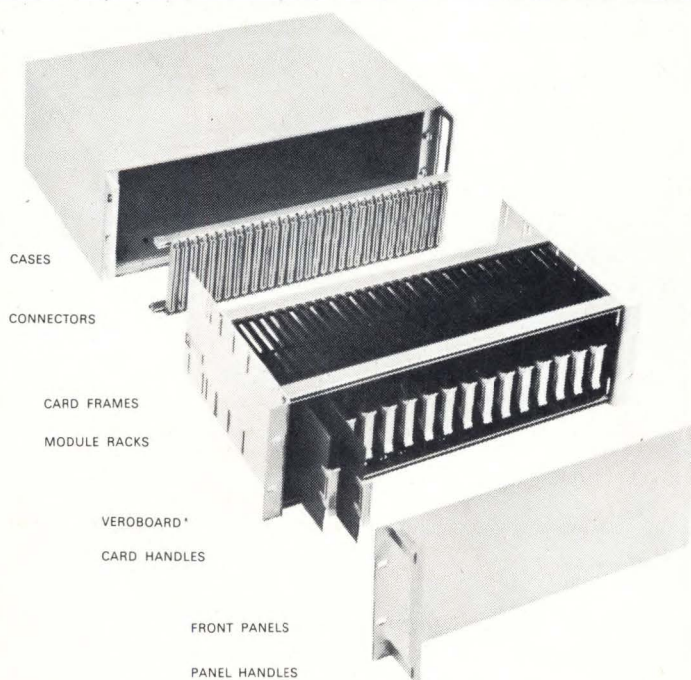
plied it toward another field.

Chomerics claims an assembly time of 15 seconds per connector and prices their units at one half a cent per pin. It remains to be seen whether their new unit

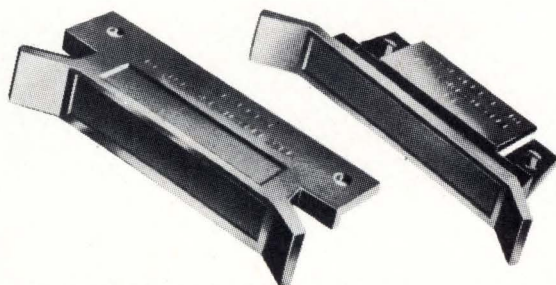
with its obvious advantages will put a dent into the wave-soldering method of flatpack insertion. ■

For more information on the Chomerics connector, circle 345.

COMPLETE PACKAGING CAPABILITY



P.C. CARD HANDLES



Molded of polycarbonate, these smartly styled handles mount without hardware in two styles, while the third may be riveted. The snap-in versions have molded lugs that snap into holes in the P.C. card and lock in place. This unique fixture saves time, labor and hardware costs while providing a positive attachment of handle to card, available from stock in black, white, red, green and blue.

vero

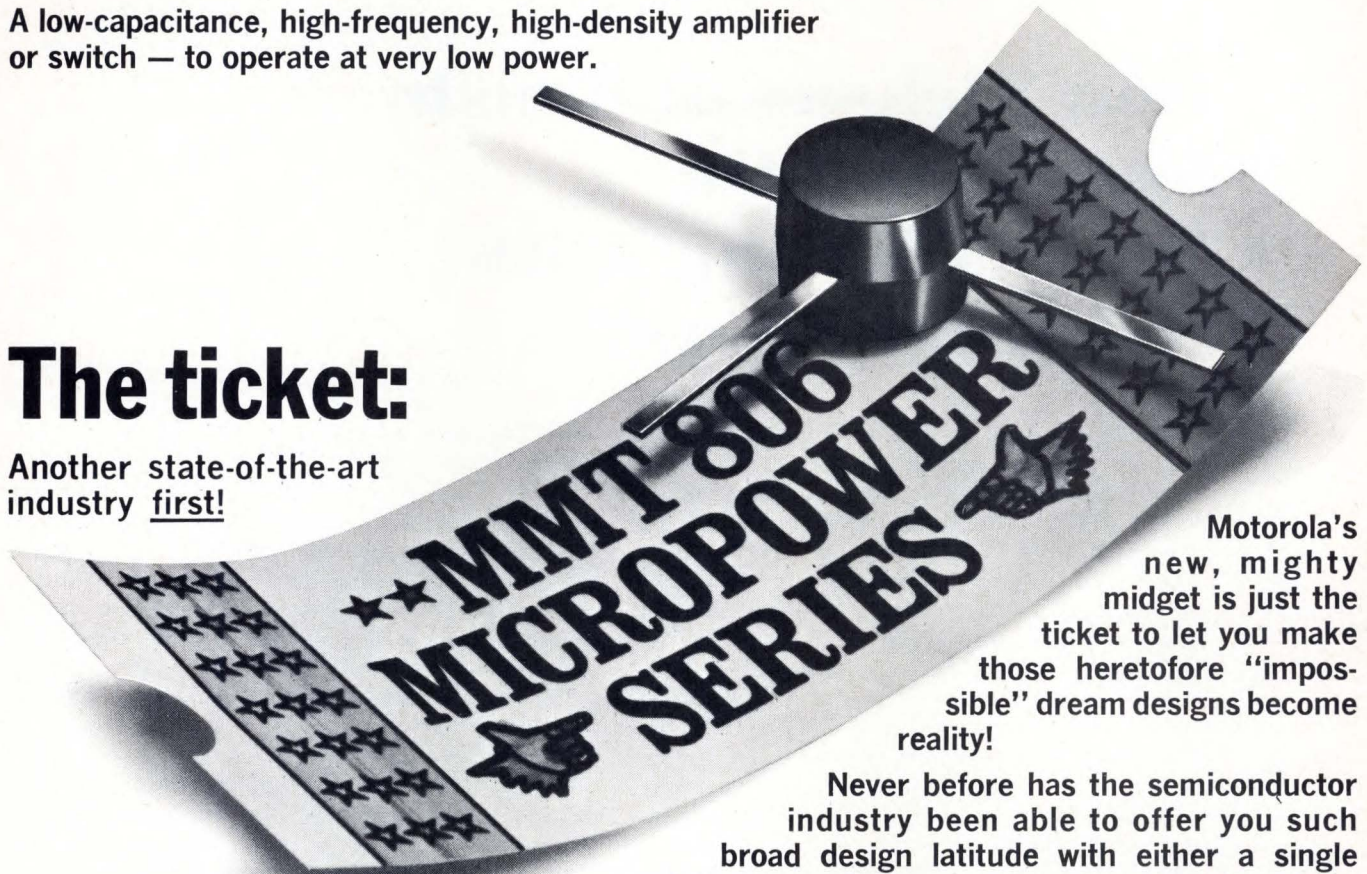
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The need:

A low-capacitance, high-frequency, high-density amplifier or switch — to operate at very low power.

The ticket:

Another state-of-the-art industry first!



Motorola's new, mighty midget is just the ticket to let you make those heretofore "impossible" dream designs become reality!

Never before has the semiconductor industry been able to offer you such broad design latitude with either a single device or multiple components, combining these unusual capabilities:



The unique combination of low-capacitance and high-frequency performance capabilities at low power levels makes the MMT806 micropower series ideal for portable communications gear, medical electronics, remote control monitoring systems and other such applications requiring extremely low battery drain and very little space.

The MMT806 series comprise the lowest-capacitance transistors in the industry to offer unsurpassed high-frequency amplification and fast switching at very low operating currents and voltages.

The introductory 100-up prices of \$13.00 for the MMT806/807, and \$15.00 for the MMT808/809 are really "low ticket" when you consider the contents. What's more, each device is rigidly tested for 12 parameters — your assurance of optimum performance and reliability!

Contact your nearest Motorola representative today and ask for complete details. Or, write us direct for your free data-sheet tickets to new design horizons! Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

Specification Highlights

Encapsulated in the rugged, voidless, Micro-T plastic package (case 28), the MMT806 silicon transistor series is comprised of two complementary pairs:							
		 MMT806 (NPN) and MMT808 (PNP) Micropower Switches		 MMT807 (NPN) and MMT809 (PNP) Micropower Amplifiers			
AMPLIFIER CHARACTERISTICS	Symbol	Min. NPN&PNP	Typ NPN	Typ PNP	Max NPN	Max PNP	Unit
Power Gain (matched) ($f = 200 \text{ MHz}$, $V_{CE} = 0.7 \text{ V}$, $I_C = 100 \mu\text{A}$)	G_p	—	18	17	—	—	dB
Noise Figure (Opt. Source) ($f = 200 \text{ MHz}$, $V_{CE} = 0.7 \text{ V}$, $I_C = 100 \mu\text{A}$)	NF	—	2.0	2.6	—	—	dB
Input Capacitance ($f = 1 \text{ MHz}$, $V_{CE} = 0.0 \text{ V}$, $I_C = 0$, collector guarded)	C_{ib}	—	0.27	0.34	0.45	0.50	pF
Output Capacitance ($f = 1 \text{ MHz}$, $V_{CE} = 0.5 \text{ V}$, $I_E = 0$, emitter guarded)	C_{ob}	—	0.34	0.47	0.55	0.80	pF
Current Gain Bandwidth Product ($f = 200 \text{ MHz}$, $I_C = 1 \text{ mA}$, $V_{CE} = 1 \text{ V}$)	f_r	1.2	2.1	2.5	—	—	GHz
DC Forward Current Gain ($I_C = 10 \mu\text{A}$, $V_{CE} = 1 \text{ V}$)	h_{FE}	20	125	70	—	—	—



MOTOROLA PLASTIC
—where the priceless ingredient is care!

Don Nicksay of Brush Speaks Out On What's Wrong With Recorder Specs

In a nutshell, it's accuracy superspecs. What do I mean by accuracy superspecs? I mean the commonly accepted preoccupation with creating a monumental specification document with total disregard for the job to be done.

Here's an example: Consider for a moment the engineer who specified a multiple-channel direct-writing oscillograph to record lengths and weights, respectively, of sawmill logs in millimeters and ounces. Of course it's ridiculous, yet such superspecs are not unusual. On the other hand, it's common to see customers trying to read chart paper to three-place accuracy when, at best, input data have one-place resolution. Kind of silly isn't it?

Not only are specs over-emphasized, but there is also a misconception as to what are proper spec ratings in the first place. For example, most recorder specs are for *static* conditions, but the recorder is used dynamically. So who knows how to translate static specs into dynamic specs?

For that matter, how many users really know what dynamic sensitivity and dynamic accuracy are needed? The problem is further compounded because specs usually aren't drawn up with consideration for environmental conditions — extreme temperature, high humidities, etc. Yet, in all probability these have more effect on the measurement result than the equipment specs.

Many users make the mistake of assuming that superspecs are somehow a guarantee of super results. Unless the instrument is properly applied by a knowledgeable user, the specs can turn out to be virtually useless.

A continuing problem is common understanding and agreement on spec definitions, and most manufacturers, including us, don't go out of their way to make their published literature easy to understand or easy to compare. What, for example, is the meaning of the word accuracy, and what is meant when we state 99.5% accuracy in a recording system? First, we de-

fine accuracy as the capability of an instrument to follow the true value of a given phenomenon. Then we state that accuracy is the sum of a number of errors including those caused by hysteresis, linearity shifts, thermal zero shift, thermal sensitivity shift, overload limits, calibration errors, and in some cases many more. Not all manufacturers include all potential accuracy errors in defining and listing total accuracy so an unqualified spec is almost meaningless.

My challenge to the validity of specs may seem unusual coming from the representative of a company that built its reputation and its business through specs. But we're not offering excuses to justify our unqualified stance for specs during the past 10 years because those were the years of what may be termed "forced specmanship." The attitude of placing great importance on specifications was the order of the day — especially in government procurement offices. Users needed detailed specs to justify the equipment they wanted to buy and procurement agencies needed specs to advertise for competitive bids and the whole art of specmanship grew into a great bureaucracy, again at the expense of the job to be done.

Specmanship became the end in itself rather than the reason. Brush, along with all other chart-recorder manufacturers, responded to the specs-mania requirements of customers. Users were pushing us to build ultra-sophisticated direct-writing recorders, particularly with respect to operating characteristics in the worst possible environments. These instruments often had higher frequency response than needed and were tested and qualified to perform without failure for extended periods in environments that no more than one instrument in 1000 would ever see.

Now don't get us wrong — there are many legitimate reasons for exacting specifications, such as called for by aerospace engineers who try for 99.9% accuracies. And vendors can supply very precise instruments for sophisticated applications in cases where they are needed. But that's the rub. Too many engineers in both government and industry are still call-

ing for the same superspecs to measure and record relatively mundane phenomena.

If all chart recorders were purchased on the basis of specs alone, there would be a lot of money floating down the drain.

Certainly the user knows that the cost of superspecs must ultimately be borne by him. To prevent this waste, it's the responsibility of the instrument manufacturers to clear up a

lot of specs misconceptions. We must present a realistic picture of the true function of multiple-channel chart recorders. We have to define their capabilities and limitations.

For example, there is a big cost difference between *practical* accuracy and *possible* accuracy — or repeatability — or frequency response. *Possible* measurement precision is where superspecs are born. If the user wants the job done as accurately as *practical*, there's no problem. However, when he specifies "as accurate as *possible*," he's loosened a barrel of monkeys. The



recorder manufacturer will eventually make a super complex instrument, but it's going to cost the user — from hundreds to even thousands of dollars extra.

Before we go any farther, let's review for a moment what the main function and advantages of multiple channel direct-writing recorders are — in the order of their value and importance to the user: (1) Instantaneous readout of dynamic phenomena. (2) Continuous analog-versus-time presentation. (3) Simultaneous display of multiple values on the same time base. (4) Permanent records without additional processing. (5) High accuracy, repeatability and resolution of data. (6) Chart records reproducible by any conventional process. (7) Unmatched flexibility and ease of operation.

I think it's also important to establish clearly what a basic direct-writing recorder is. It's simply a recording dc voltmeter. Its automatic writing system continuously translates electrical signals into visible traces on permanent charts.

An electrical signal is usually amplified, conditioned or attenuated in a preamplifier which feeds a pendrive amplifier. Its output drives a galvanometer or penmotor which produces a pen deflection that is directly proportional to the input signal. The pen writes on a moving chart providing a continuous analog-versus-time presentation.

One recorder can be used for many applications since practically all physical variables can now be converted into equivalent electrical signals by a large selection of standard transducers.

Other big factors in realistic recording system specifications are the many components that can affect accuracy, repeatability and resolution of data. The key components are: (1) Signal transducer. (2) Signal conditioner. (3) Preamplifier. (4) Drive (power) amplifier. (5) Penmotor or servomotor. (6) Chart drive. (7) Writing implements. (8) Chart paper.

The first factor, the signal transducer, is not a part of the recorder but is a part of the recording system. It has quite an effect on the overall accuracy of the system because at the very beginning it changes the physical characteristics of a phenomenon to an electrical signal. Therefore, before we even think about recorder specs, we should know the accuracy of the transducer.

We can use any one of about 1800 basic transducers that are on the market (as listed by IEEE). It's no simple task to pick the right transducer considering the wide scope of monitoring and recording applications that chart recorders can be called upon to handle. The electrical output characteristics of the transducer (signal source) fall into six classes, according to the output-circuit configuration of the transducer: (1) Single ended — grounded. (2) Single ended — floating. (3) Single ended — driven off ground. (4) Balanced — grounded.

(5) Balanced — floating. (6) Balanced — driven off ground.

The transducer used must be properly identified and matched with an appropriate signal-conditioning amplifier. Otherwise, final data may be useless.

Low-impedance transducers are preferred to reduce noise and to minimize the shunting effect that the measuring instrument imposes on the source. The point is that this information is fundamental in specifying an overall system.

The next component in the recording sequence is the signal conditioner. It accepts the signal and electronically conditions it, where necessary, before introduction into the preamplifier. The conditioner can also be used as a source for excitation output for special auxiliary elements. A signal conditioner and a preamplifier may be one and the same.

When a recorder requires performance at millivolt- or microvolt-sensitivity levels, the signal must be amplified through a preamplifier. Otherwise, the signal could be fed directly to the pendrive amplifier. The amplifier that accepts the signal from the source determines the electrical input characteristics of the recorder. These characteristics include frequency response, noise, drift, input sensitivity, impedance, transient response, common-mode rejection, type of input, and attenuator accuracy and range.

The magnitude of potential errors in systems with preamplifiers can be illustrated by starting right at the sensitivity dial and assessing some of the potential inaccuracies introduced right at that point. Those which immediately come to mind are (1) frequency response, (2) attenuation, (3) gain, (4) hysteresis, (5) amplitude distortion, and (6) phase nonlinearity.

(1) Frequency response is extremely variable. Up to certain limits of system performance the potential error is of little consequence, but beyond a certain threshold (usually not too clearly spelled out) the errors in response characteristics swamp out all other errors.

(2) Attenuation depends on known-tolerance resistor networks with inaccuracies equal to the sum of interrelated inaccuracies of the resistors in the network. While the cumulative error can be measured, it must be remembered that a relative error exists among all recorded variables.

(3) Gain errors are usually present as a result of changes in components with time. The errors are usually small, and are usually ignored, but they are nevertheless present.

(4) Hysteresis can contribute generous errors to sensitivity inaccuracy when the output assumes different values at a given input point as that variable rises and falls around that point.

(5) Amplitude distortions are built into the system particularly in penmotor linkages and penmotor magnetic fields, and in amplifier nonlinearities.

(6) Phase nonlinearities can occur when the time lags between pen movement and changing value of input vary with frequency. Across the frequency-response spectrum, these time lags are not always constant.

All of this is just a way of saying that the selection of a particular sensitivity setting does not guarantee that the recording pen will move the precise number of chart divisions in response to an input signal for that sensitivity setting.

Manufacturers seldom cover all these points in published literature, which means that the user's only recourse is to select an instrument whose limits of inaccuracy are known to him in advance. Otherwise the wiggle may not represent true signal variation.

The drive amplifier is the next system component behind the preamplifier. It's subject to many of the same inaccuracies as the preamplifier. Its purpose is to amplify the original or preamplified signal sufficiently to provide motion to the penmotor. Since the penmotor fluctuates from an inert to a moving mass, the amplifier power must change accordingly. Both units must be properly matched to reproduce the original signal faithfully.

The familiar d'Arsonval movement is the heart of a conventional spring-restored type of direct-writing recorder. It is generally called the penmotor. The moving coil is located in the field of a permanent magnet and restored to chart center by means of a torsion spring. Angular pen deflection is directly proportional to the current in the moving coil. It is a simple reliable mechanism. Its overall performance is limited by the stiffness of the torsion spring, mass of the pen, its writing pressure, and the writing technique employed.

The moving chart in these curvilinear writing systems exerts a force on the pen when the pen is at a point off chart center. The force is in a direction to deflect the pen back to chart center and is a potential cause of error.

The pen has a tendency to "anchor" into position, especially in the writing trough on thermal chart paper, which requires a force within the torsion spring of the penmotor to overcome this inertia component. It's another source of error, particularly in a penmotor with low restoring force.

The development of the position-feedback penmotor for high-frequency direct-writing recorders made it possible to combine the high-frequency characteristics of the spring-restored penmotor or galvanometer with the excellent accuracy characteristics of the potentiometric recorder.

An accurate non-contact feedback element with infinite resolution, no reactive force and zero maintenance, is very desirable in any servo system. This is especially true in high-frequency penmotors. A small position-sensing transducer called the Metrisite comes close to meeting all these requirements.

It's matched to the geometry of the pen linkage, has a low reactive force, is entirely non-contact, and has less than 0.1% linearity error. The output is always proportional to pen position. There is nothing to wear, or degrade performance with time or high velocities. This is a great improvement over a potentiometer or slide wire as a pen-position feedback element and is responsible for the high accuracy now available from a practical data recorder. Here, the history and reputation of the manufacturer is extremely important.

Generally speaking, chart drives have been refined to the degree that they are rugged, reliable and relatively trouble free. Manufacturing specifications are usually adequate in defining performance capabilities.

Four basic direct writing methods are used today. Here are the best and worst characteristics of each:

CAPILLARY INK provides a fine, uniform trace, low friction at the pen tip, low-cost chart paper and easy reproduction by conventional means. Reliability is poor due to clogging. It requires high maintenance and it certainly can be messy.

ELECTRIC writing is accomplished by a high dc voltage that burns away the top layer of a special teledeltos paper. It provides good reliability and produces a thin, uniform trace over a wide range of writing conditions. The paper cost is high, contrast is poor and reproduction is difficult.

THERMAL writing provides a trace as an electrically heated stylus writes over a knife edge on a special heat-sensitive paper. It is clean, simple and rectilinear without use of any linkages. The paper is soft, difficult to work with, easily smudged and expensive. The trace is nonuniform and frequently skips. Reproductive quality is poor.

FORCED-FLUID writing is accomplished by a completely closed fluid system that operates under pressure like a miniature hydraulic system, with fluid precisely metered out by pen movement. Pen pressures, many times higher than normal, are used to establish a positive liquid seal between the chart paper surface and the pen tip. This system produces true rectilinear writing on low-cost chart paper and provides permanent chart records of superior quality. The sharp, uniform trace does not change with pen velocity. The unique combination of high contrast and good resolution provides chart records that are easy to reproduce

by any conventional process.

Pressure systems are very reliable but there are infrequent failures. If failure occurs within the recorder at the reservoir or pump, there can be a terrible mess inside which requires extensive cleanup with special solvents. Pressures are adjusted for average writing speeds. At extra-slow recording speeds the forced-fluid systems have a tendency to put down excessive ink which produces a wider than normal trace.

Up to this point our discussion has considered recording-system hardware exclusive of chart paper. By minimizing all the errors we can produce a near-perfect system and still have a widely inaccurate chart record.

If any one thing makes me shake my head sadly, it's the universal obsession with recorder specs coupled with a total disregard of the influence of the chart paper. Too many users for too long a time have paid too little attention to chart paper, and they're long overdue to take corrective action in this vital point.

Chart-paper accuracy starts with engraving on a printing cylinder which is the result of an engineering drawing, a photographic negative and an etched surface on the cylinder. All steps must be executed with extreme care. Cylinder printing is usually done in a rotary gravure press which is recognized as an improvement over the flatbed method. The unprinted roll must be carefully mounted in the press, printed under controlled tension and precisely slit to proper width. After slitting, the rolls are re-spooled in 250 to 500 foot lengths (or length required), packaged and stored for shipment.

It goes without saying that the raw stock must be of the best quality, uniformly coated, without holes or surface blemishes. But even the finest paper does expand and contract with temperature and humidity, and therefore must be printed in a controlled atmosphere.

It is possible to produce accurate chart paper if enough attention is paid to required details, but it is impossible for the manufacturer to control the conditions under which the paper is used. And this is where the real problems begin. It is unlikely that the chart paper will ever again see the laboratory conditions of manufacture, and from this point on, the effects of temperature and humidity can introduce recording errors up to two (2) percent!

The roll of chart paper must be properly mounted in the recorder. The spool must be tight, located at the proper reference point, and the paper must track correctly under even tension. Even with care it's difficult to keep paper wander less than $\frac{1}{4}$ of a chart division!

If we sound as though we have made a career in chart paper, you're right, we have. To maintain top quality, some recorder manufacturers

print their own engineered chart paper in their own plants on highly accurate gravure presses. Charts are handled in special "white rooms," kept at constant temperature and humidity 365 days a year.

It should be clear by now that superspecs are only half the story. How about overall quality, and the requirement to operate troublefree year after year?

The specs must relate to quality which in turn must relate to the job to be done. The better vendors try to engage in "consultative" selling to assist the customer in matching his recording requirements to the result he wants to obtain. They are committed to a customer-oriented full-service approach including applications assistance, documentation and maintenance. In the final analysis, it costs little more to take the time to analyze the problem and select the best recorder available. We're convinced that the wise user will deal only with high-quality, qualified manufacturers and will rely on the advice of someone who really knows the business. How do you write a superspec about that?

EEE

Who is Don Nicksay

He's a Naval Academy graduate with a BS in Engineering and ex-Air Force fighter pilot who flew 85 combat missions in Korea, where he received the Distinguished Flying Cross and other medals.

To get as far away from the military as possible, Don joined Procter and Gamble in 1955 as a Production Supervisor in the soap works. His compulsion to be a peddler led him to Taylor Instruments in 1957 where he worked as a Sales Engineer.

The instruments business got into his blood and he switched to Brush in 1960 as a Sales Engineer in Washington, D.C. He was promoted to Branch Manager in the Chicago office in 1961. In 1963 he was transferred and promoted to General Sales Manager of Clevite Piezoelectric Division where he became General Manager in 1967. Back to Brush in 1969 and promoted to General Manager where he pursues his main hobby — work.

Don, who lives in Hudson, Ohio, belongs to the country club and often tees off on number twelve, a few steps from his backyard.

His wife, Claire, has her Master's in Education and is pursuing graduate studies at the University of Akron. His son, Dave, started at Hampshire College this Fall. And his daughter, Debbie, is a tenth grader at Hathaway Brown School.

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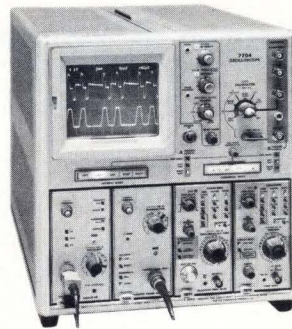
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Complementary-Symmetry MOS ICS

by Don DiMassimo

Let's review briefly a few basic characteristics of MOS insulated-gate field-effect transistors. These devices consist of two electrodes (source and drain) diffused into a silicon substrate. The source and drain are separated by a finite space, thus forming a majority-carrier conducting channel. A metal gate is placed above the channel and insulated from it.

An "n" channel device is normally operated with the drain at supply potential (V_{dd}), and the source and substrate at ground (V_{ss}) potential. If a positive potential is applied to the gate, a field is created between the gate electrode and the substrate. Since the field must terminate on charges, electrons move through the substrate and accumulate in a layer immediately beneath the silicon surface. This layer is termed an inversion layer, i.e., the "p" substrate is inverted to "n". Thus an ohmic path is formed between the drain and source, and current flow is established between supply and ground. If, however, the gate potential is reduced to ground potential, the inversion layer is immediately removed and the device current is cut off. In this situation, the drain is heavily reverse biased, so that the only current flow is leakage, normally in the picoampere range.

In enhancement MOS devices, such as those used in complementary-symmetry MOS (COS MOS) arrays, the gate voltage does not have to be reduced to ground potential to cutoff the device. Normally the cutoff point is established by the process above the minimum value required for good noise immunity. The gate voltage at cutoff is termed the threshold voltage (V_{th}).

A "p" channel FET performs in a manner similar to the n-channel device except that all signs are reversed, i.e., the potentials are nega-

tive. The source and drain electrodes are p + diffusions in an n-type substrate; the induced layer of charges is termed an "accumulation" layer and the carriers involved in conduction are holes.

DC Characteristics

The typical drain current characteristics of an "n" channel enhancement-type transistor are shown in Fig. 1. Two current regions are defined; the triode region, where

$$V_{DS} < V_{GS} - V_{TN} \quad (1A)$$

$$I_{DS} = K_N [2V_{DS} (V_{GS} - V_{TN}) - V_{DS}^2] \quad (1B)$$

and the saturated region, where

$$V_{DS} \geq V_{GS} - V_{TN} \quad (2A)$$

$$I_{DS} = K_N (V_{GS} - V_{TN})^2 \quad (2B)$$

In the above equations, the constant K_n is basically a function of design and processing and is given by $(\mu_n E_{ox} W)/2L T_{ox}$, μ_n = effective mobility of electrons, E_{ox} = permittivity of insulating oxide layer, W = channel width, L = channel length and T_{ox} = thickness of the insulating oxide (1000 Å typical).

The channel dimensions W and L , are design variables. Substituting typical process variable values for μ_n , E_{ox} and T_{ox} results in:

$$K_N = 5.7 \times 10^{-6} \quad (3)$$

Typical dimensions for an n-channel device are $L = 0.25$ mils and $W = 3.0$ mils. If $V_{gs} = 10V$, and $V_{tn} = 1.5V$, the saturation current from Equation 2B is:

$$I_{DS} = 5.7 \times 10^{-3} \left(\frac{3}{.25} \right) (10 - 1.5)^2 \\ = 4.9 \text{ mA}$$

The equations for p-channel devices are similar except for appropriate changes in sign and with V_{tp} and μ_p substituted for V_{tn} and μ_n . The slope of the drain-current characteristic in the FET triode region is termed r_{ds} . This value can be computed from:

Author: Donald V. DiMassimo is section head, research and development, G-V Controls, Sola Basic Industries, Inc., Livingston, New Jersey.

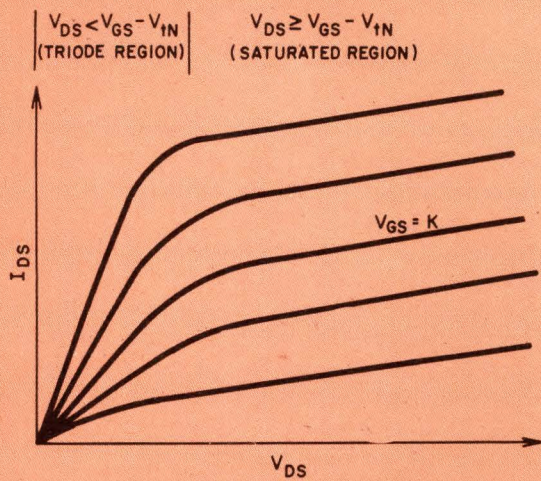


Fig. 1. Typical drain current characteristic for an n-channel MOS device.

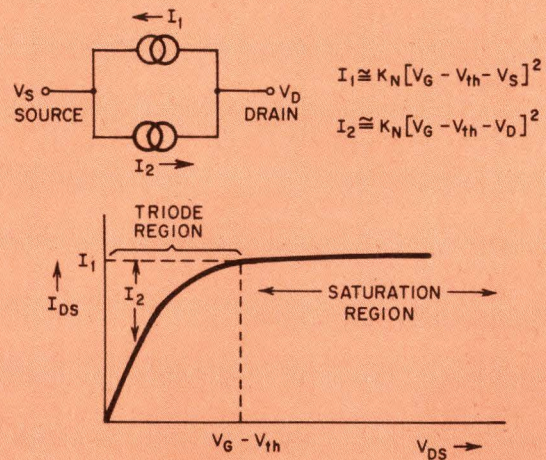


Fig. 2. Current-source equivalent circuit for an n-channel device.

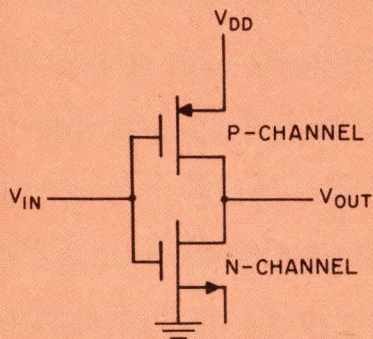


Fig. 3. Complementary MOS inverter circuit.

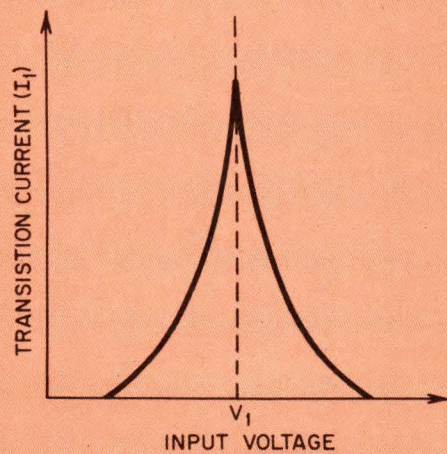


Fig. 5. Transition current characteristics.

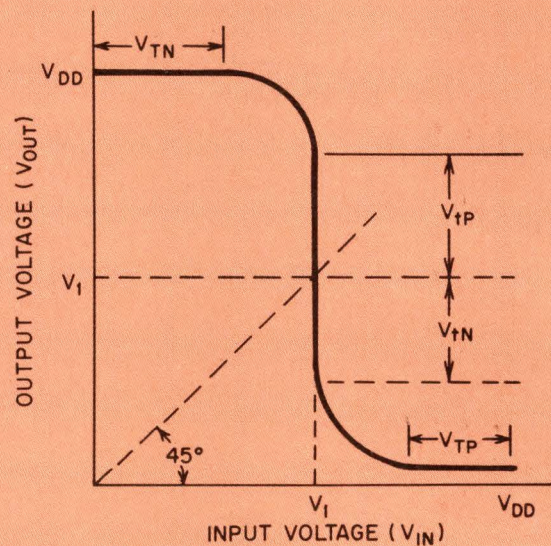


Fig. 4. COS MOS inverter transfer characteristics.

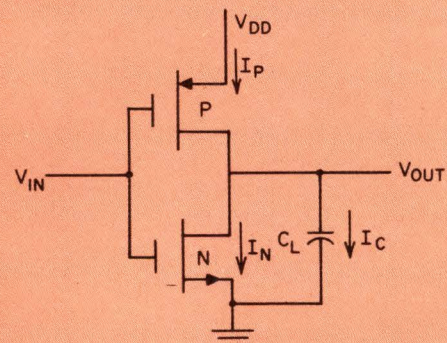


Fig. 6. COS MOS inverter driving a load capacitance.

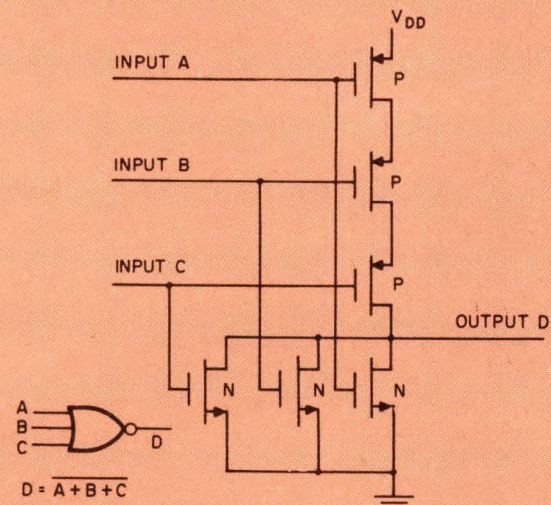


Fig. 7. Three-input COS MOS NOR gate.

$$R_{DS} = \left(\frac{\partial I}{\partial V_{DS}} \right)^{-1}_{V_{DS}=0} = \frac{1}{2K_N (V_{GS} - V_{TN})} \quad (4)$$

For the n-channel device mentioned above, this value will be:

$$R_{DS} = \frac{1}{(2)(5.7 \times 10^{-6}) \left(\frac{3}{.25} \right) (10 - 1.5)}$$

$$= 860 \, \Omega$$

An approximate current-source equivalent circuit is shown in Fig. 2.

The Complementary Inverter

The complementary inverter, shown in Fig. 3, will be used to illustrate the basic operation of COS MOS circuits. In this circuit, when V_{in} is equal to V_{dd} , the n-channel device is turned on, the p-channel device is off, and the output is at ground potential. Conversely, when the input voltage is at ground, the n-channel is off the p-channel device on and the output is at V_{dd} potential. Note that only during the actual switching period is there a direct connection between V_{dd} and ground; thus under static conditions essentially no power is dissipated in the circuit.

The transfer characteristics for this device are shown in Fig. 4. An important voltage, when noise immunity is being considered, is the voltage applied to the inverter which will cause both devices to be turned on. This is termed the transition voltage (V_i in Fig. 4.). For optimum noise immunity, this voltage should be $\frac{1}{2} V_{dd}$. The transition voltage can be computed from the following equation:

$$V_i = \frac{\sqrt{\frac{K_P}{K_N}} (1 - |V_{TP}|) + V_{TN}}{1 + \sqrt{\frac{K_P}{K_N}}} \quad (5)$$

Normally, in the design of a COS MOS array, the device channel length, L , is held to a minimum. This is done to maximize transconductance, speed, and packing density. The channel width, W , is then tailored to obtain the desired device characteristic. Therefore, substituting the average threshold voltage in Equation 5 and inserting typical K_n , K_p constants:

$$V_i = \frac{1}{2} V_{DD} \text{ if } W_P \cong 2W_N$$

The above widths expressed provide the width ratio desired for maximum speed.

The transition current (I_i) during the actual switching interval versus switching voltage characteristic is shown in Fig. 5. The maximum current can be computed from Equation 2:

$$I_i = I_P = I_N = K_N (V_{GS} - V_{TN})^2 \quad (6)$$

where $V_{GS} = V_i$

The switching response of the complementary inverter can be computed for an idealized case. Fig. 6 illustrates an inverter driving a load capacitance, C_L . If the assumption is made that C_L is high in comparison to the device capacitance, the following approximate relationship can be derived for a stage delay, T_d :

$$T_d \cong 0.9 \tau \left[\frac{1}{\left(1 - \frac{V_{TN}^2}{V_{DD}^2} \right)} + \frac{1}{\frac{K_P}{K_N} \left(1 - \frac{|V_{TP}|}{V_{DD}} \right)^2} \right] \quad (7)$$

where $\tau = C_L (K_N V_{DD})$

It can also be shown that for minimum delay and equal rise and fall times, the transconductance of the devices should be matched:

$$g_{mp} = g_{mn} \text{ if } W_P \cong 2W_N$$

This is the same transconductance value desired for maximum noise immunity.

Again referring to Fig. 6 the actual switching response is essentially determined by the capacitance and the amount of current available from the transistors to charge this capacitance.

$$I_P = I_N + I_C \text{ or}$$

$$C \frac{dV}{dt} = I_P - I_N \text{ and}$$

$$T = C \int_{V_0}^V \frac{dV}{(I_P - I_N)}$$

It is evident that minimum switching time is obtained when the current available to charge C for any voltage V is at a maximum.

Capacitance

Source and drain capacitances depend on substrate bias and diffusion dopant as shown in Table 1.

Internal COS MOS capacitances are generally very small (in the neighborhood of 1 pF) and therefore devices on the chip which drive other devices can be very small.

Complementary NAND or NOR Gates

Complex gates, such as a three-input NAND or NOR gate, involve the use of series and parallel devices such as shown in Fig. 7 and 8. When MOS devices are used in this manner, their individual characteristics must be compiled as conductances. If, in the inverter, the impedance of the 2-mil p-channel device is considered to be 1, then to provide the same impedance from the output to V_{pp} in the NOR gate, the three p-channel devices in series must also have a total impedance of 1; therefore each device will have an impedance of $1/3$. The width of each will then be $3/1 \times 2 = 6$ mils. Since any one of the parallel n-channel units, if turned on, will bring the output to ground, each one must have the same impedance as the inverter n-channel devices, and therefore should have a 1-mil width.

The switching response of even relatively simple circuits such as a two-input NAND gate cannot be readily calculated, since with series devices, the substrate-to-source capacitance and the threshold voltage are both functions of substrate bias, which is continually changing as the load capacitance is discharged.

Shift Register Stage

A shift-register stage illustrating the reduction of components obtained by use of the ca-

capacitance storage feature of MOS gates is shown in Fig. 9 and 10. As shown in Figure 9, S_1 and S_2 are in series with the cross-coupling connections of the flip-flop. When these switches are opened, two separate storage elements are formed, the left side and right side of the flip flop. Each side can store information for an extended but finite period of time. Digital information from the preceding stage is transferred to the left side through the gate, and can change the stage on the left side. At the same time, the right side transfers its information to the left side of the next stage. If switch S_2 is closed first, and then S_1 , the "1" or "0" information transferred from the preceding bit is locked into the left side. A shift register based on these principles and using MOS units for switching is shown in Fig. 10. Input data are given in Table 4. Essentially, this circuit is a simple two-phase MOS flip-flop.

Logic designs may be achieved by use of only NOR gates and inverters. However, a somewhat more economical gate-design approach is to consider that (1) common source and drain regions can exist in integrated-circuit form, and (2) the MOS transistor is topologically symmetrical.

Memory Cell and Read/Write Drivers

Figures 11 and 12 illustrate a 10-device basic memory cell, and an associated READ/WRITE driver. The WRITE driver is activated only upon a command common for the entire memory. An additional signal, the inverse of the WRITE command, is also generated to insure high-speed operation of the storage cell. These lines are then connected to appropriate points of the basic cell, shown in Fig. 12. The cell can be written into by means of two MOS transmission gates — one for opening the feedback loop from B to C, the other for entering the desired information into the cell at C from the digit line. After one pair-delay time, the potentials at B and C are identical and the feedback loop may be closed by bringing the write line down to ground potential, thereby leaving the information stored in the flip-flop. Readout from the memory is accomplished nondestructively by controlling the conductance of an n-type MOS device with the output voltage of the cell. Subsequent application of a READ command will result in the presence or absence of a current in the low impedance sense (DIGIT) line, indicating a stored "1" or "0". Current sensing with a low impedance device, such as a grounded-base bipolar transistor, is a very fast operation even if the capacitance of the digit line is large as it would be in a large memory.

Pair Delay

The switching response of a COS MOS logic circuit is determined solely by capacitance loading at the input and output and the amount of current available to charge this capacitance.

One of the most important parameters for a logic inverter is the circuit-pair delay, which is

defined as the time delay experienced by the signal in traversing two inversions as measured at the 50% points on the waveform.

Referring again to Equation 7 and Fig. 6 we can see that pair delay is a function of effective output loading capacitance, assuming that the input waveform is a square pulse.

The input capacitance of a COS MOS transistor is approximately:

$$C_{IN} = C_{GC} + C_{CS} + 2C_{GD} \quad (8)$$

$$\cong 0.135 \text{ pF/mil of channel width}$$

The total effective C_L of an inverter stage driving n like stages is approximately:

$$C_L = n [C_{IN(n)} + C_{IN(p)}] + C_{out} + C_{stray} \quad (9)$$

Where $C_{IN(n)}$ and $C_{IN(p)}$ represent C_{IN} values for the n-channel and p-channel devices.

As a typical example, let us assume an inverter stage is driving five others ($n=5$). The MOS device characteristics are given in Table 2. The supply voltage (V_{DD}) is 10V.

$$\tau = \frac{C_L}{K_N V_{DD}} = \frac{3.48 \times 10^{-12}}{24 \times 10^{-6} \times 10} = 14.5 \text{ ns}$$

$$T_D = .9 \tau \left[\frac{1}{\left(1 - \frac{V_{TN}}{V_{DD}}\right)^2} + \frac{1}{\frac{K_p}{K_N} \left(1 - \frac{V_{TP}}{V_{DD}}\right)^2} \right] \quad (10)$$

$$T_D = .9 \times 14.5 \times 10^{-9} \left[\frac{1}{\left(1 - \frac{2}{10}\right)^2} + \frac{1}{\left(1 - \frac{2}{10}\right)^2} \right] = 41 \text{ ns}$$

Table 1. Source and drain capacitance per unit area

Bias (V)	Diffusion	
	p+	n+
0	.12	.2
10	.03	.05

(Gate input capacitance = 0.14 pF/mil of W, L = .25 mil, $T_{ox} = 1000 \text{ \AA}$).

Table 2. MOS device characteristics

$W_N = 1 \text{ mil}$
$V_{tn} = 2 \text{ V}$
$W_p = 2 \text{ mil}$
$V_{tp} = 2 \text{ V}$
$L_N = L_p = 0.25 \text{ mil}$
$C_{stray \text{ wiring}} = 1 \text{ pF}$
$C_{out} \cong .46 \text{ pF}$
$t_{ox} = 1000 \text{ \AA}$
$E_{ox} = 35 \times 10^{-12} \text{ F/meter}$
$K_N = 6 \times 10^{-6} \text{ W}_N/L_N = 24 \times 10^{-6}$
$C_L = 5 [.135 \times 1 + .135 \times 2]$
$+ .46 + 1 = 3.48 \text{ pF}$

The above results are typical for COS MOS gates. The results, of course, are highly dependent on fan-out and geometry. For example, a gate used to drive many others can be larger than those driven so as to reduce T_D .

Power Dissipation

Power dissipation is an extremely important consideration in large-scale integrated circuits, and when large numbers of devices are involved, it may be the ultimate limitation in determining device packing density. Fortunately, the standby power dissipation of COS MOS circuits is only in the order of nanowatts. However, when a COS MOS circuit switches, a considerable amount of current flows during the switching interval. The average power dissipation during switching can be approximated by the following expression:

$$P = C_L V_{dd}^2 f \quad (11)$$

where f is the switching frequency. The total dissipation is given by:

$$P_{\text{total}} = P_{\text{static}} + C_L V_{dd}^2 f. \quad (12)$$

For example, if a 50-gate array is considered, the standby power will be approximately 50 nW (at $V_{dd} = 10$ V). If the switching rate is 1 MHz, and a total load capacitance of 50 pF is being driven, then:

$$P_t = 50 \times 10^{-9} + 50 \times 10^{-12} (10^2 \times 10^6) \text{ or} \\ P_t = 50 \text{ nW} + 5 \text{ mW} = 5.00005 \text{ mW}$$

If bipolar devices had been used to provide the fifty gates, the second term of this equation would not change appreciably, however, the static term would be 8 to 10 mW per gate, and the total power dissipation would be:

$$P_t = 50 \times 10 \text{ mW} + 5 \text{ mW} = 505 \text{ mW}.$$

A p-channel MOS array using multiphase clocking might have a static power dissipation of 1 mW per gate, or $P_t = 55 \text{ mW}$.

Speed Power Comparison

Various combinations of speed, dissipation and noise immunity are available with present bipolar, MOS, and COS MOS integrated circuits.

The speed-power-noise immunity relationships between bipolar, MOS and COS MOS integrated gates are shown in Figure 13. Curves 1 and 2 are for single gates (usually used to drive many other gates), and curves 3, 4, 5 apply for gates which are internal to arrays and which drive other gates on the same chip. These curves reveal that COS MOS devices offer a considerable range of operating characteristics. They can be designed with gate thresholds from 1.5 V to approximately 7-8 V in various channel widths and lengths, and with power supplies ranging from 6 V to 20 V. In addition, they offer extremely low static power dissipation.

COS MOS Advantages

The area required to perform many logic functions in an integrated COS MOS array is about one-tenth that required with bipolar technology. COS MOS processing requires fewer steps (30%

to 40% less) than used in the manufacture of bipolar ICs and COS MOS costs are dropping rapidly, although selling prices are still higher than bipolar prices. However, since COS MOS ICs are operated from a single power source, considerable flexibility is offered system designers for speed-power optimization.

Obviously, COS MOS cannot match the gate speed of ECL, TTL or even DTL bipolar types but size, system, cost, and cooling requirements can make COS MOS more favorable in moderate-speed applications.

Sequential Memories

Let's survey a number of applications where the characteristics of COS MOS can be used to advantage. The shift register is one of the most important and useful elements in the arithmetic unit of computers. It is commonly used as a delay line for digital signals, as well as for temporary storage registers.

A shift-register has both a primary and a secondary storage element at each stage. The primary-storage element holds the information. At a clocking command, this information is shifted to the secondary-storage element of the next stage. At the next command, the information is shifted to the respective primary storage element. The two-step process eliminates timing problems by preventing coupling of the primary-storage elements of successive stages. In a COS MOS IC, the primary- and secondary-storage functions may be combined in either a flip-flop or capacitor. An MOS gate provides the capacitance for temporary storage; a flip-flop permanent storage. If both primary and secondary storage are capacitive, an ac or dynamic shift register results.

Shift Registers

An elementary dynamic shift register stage is shown in Fig. 14. During clock time T_1 , gate N_3 is closed and gate P_4 is open; the reverse condition is obtained during T_2 . The capacitance represented by the gates of the first inverter P_1 and N_1 is the primary-storage medium, and that of P_2 and N_2 is the secondary-storage medium.

During T_2 , the output inverter, P_2 and N_2 , is decoupled from P_1 , N_1 because N_3 is open. Gate P_4 is conducting and information from the preceding stage can charge or discharge the capacitance of gates P_1 and N_1 . Simultaneously, the data output provides an information transfer to the next stage.

When the clock becomes positive (T_1), P_4 opens and N_3 conducts, and information is shifted to the data output. Therefore, the cycle is completed within one clocking pulse.

Static shift-registers offer permanent storage capability. A static shift-register stage using dual transmission gates has been described previously in connection with Figures 9 and 10.

Memories

The rapid development of IC technology has

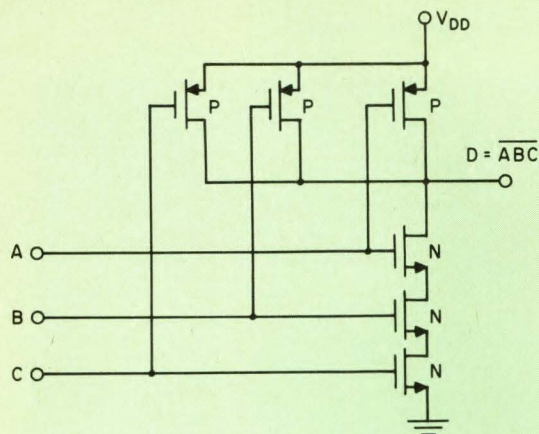


Fig. 8. Three-input NAND gate.

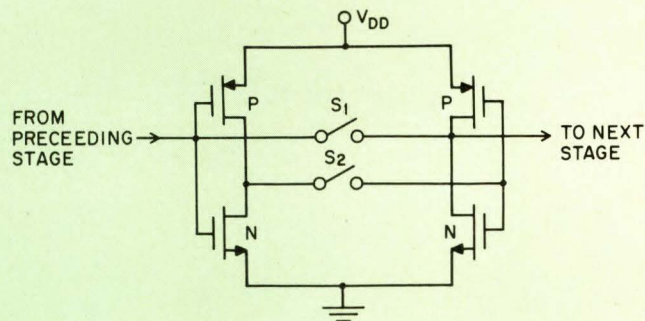


Fig. 9. Shift-register stage.

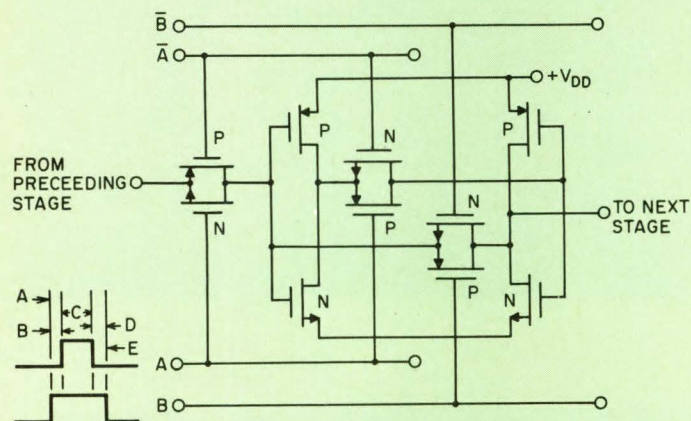


Fig. 10. COS MOS shift-register stage.

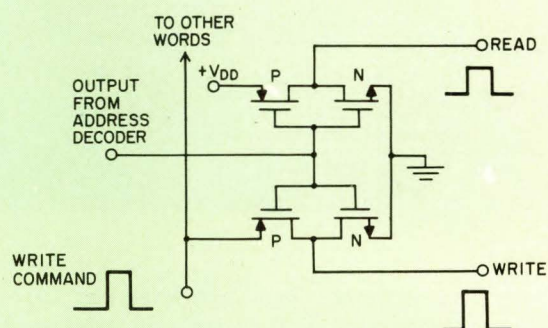


Fig. 11. MOS read-write drivers.

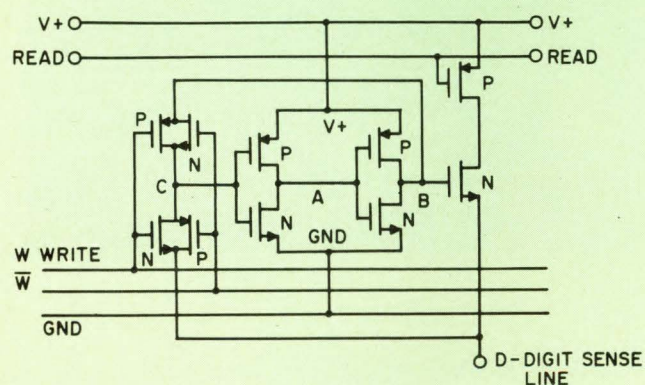


Fig. 12. MOS memory cell with nondestructive readout.

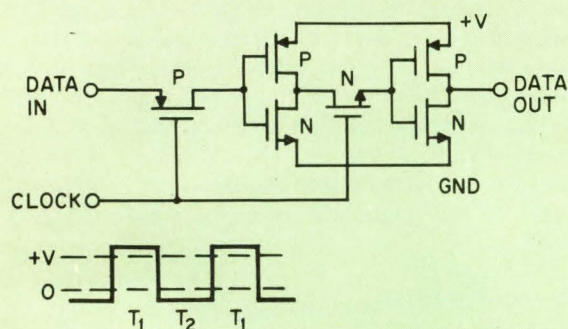


Fig. 14. Elementary dynamic shift-register stage.

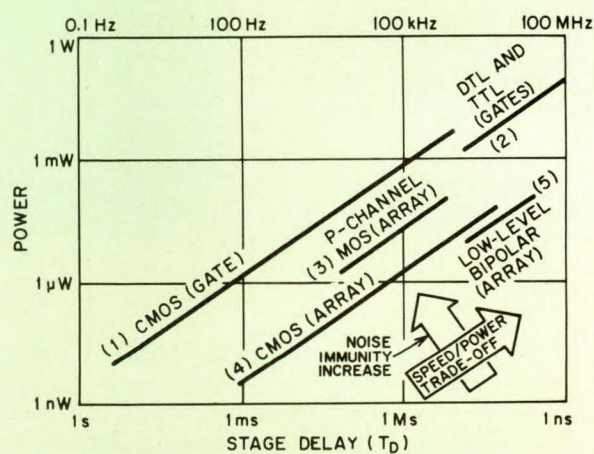


Fig. 13. Speed-power-noise immunity relationships between various types of integrated gates.

Table 3. Comparison of semiconductor and magnetic characteristics for a megabit memory.

	Readout	CMOS (NDRO)	Bipolar (NDRO)	Core (DRO)	Plated Wire (NDRO/DRO)	Thin-Film (DRO/NDRO)
Unit Cell	Read delay (ns)	10	5	150	20	10
	Write delay (ns)	25	5	150	20	10
	Standby power (μ W)	10	1000	0	0	0
Array Of Cells	Array size, bits	256×1	128×1	$16K \times 18$	$4K \times 128$	1024×64
	Word select I (mA)	1	20	425	900	200
	Digit write I (mA)	1	20	425	20	15
	Drive voltages (V)	5-15	2	30	20	10
	Readout signal	200 μ A	500 μ A	20-mV	10-mV	2-mV
	Packing density (bpsi)	(dc)	(dc)	pulse	pulse	pulse
		15K	7.2K	4.5K	1450	3200
	Rise time of read current (ns)	—	—	100	30	10-35
	Curie Temp. ($^{\circ}$ C)	—	—	500-600	600	600
10 ⁶ Bit Memory	Volatility	Yes	Yes	No	No	No
	Economic module, bits	2K-32K	1K-8K	256K	256K	64K
	Power dissipation (W)	50	1000	100	200	200
	Full cycle time (ns)	125	50-100	500	200	200
	Cost per bit (cents) in mass production	2-5	4-5	1-2	2-4	2-3
	Mode of organization Batch fabrication	LS	LS	2-1/2D	LS	LS
		Yes	Yes	No	Semi	Yes

LS = Linear Select

Table 4. Shift-register input data (see Fig. 10)

Data Input Path	Flip-Flop Load	Operation
A Open	Closed	Information locked in flip-flop
B Open	Feedback open	First inverter freed to accept new data
C Closed	Both paths open	Data from preceeding shifted into first inverter; stage data from output shifted to next stage
D Open	Feedback open	Data shifted dynamically from first to second inverter
E Open	Closed	Information locked in flip- flop.

made the semi-conductor memory an economical alternate for magnetic memories in capacities up to 4096 bits. The indications are that future high-speed scratch-pad and possibly main memories will be built entirely with large monolithic semi-conductor arrays.

The random-access storage matrix, and the address decoders used to select a particular memory cell location, can be processed simultaneously on a common substrate. Most active memory cells currently in use employ flip-flops to store binary information; logic gating is incorporated in the cell to ensure that information is written into, or read out of, only the selected memory location. To decrease cycle time, the state of the cell is usually sensed in a nondestructive read-out mode (NDRO).

Several COS MOS memory circuits and structures have been conceived; for example, the 10-

device memory cell has previously been described (Figures 11 and 12). Word-organized random-access memory modules complete with address decoders and word drivers have been built.

As an alternative to word-organized structures, designs using coincident voltage or XY memory cells in a so-called bit organized system are possible. In these memory cells the coincidence of a "1" in the X and Y lines is performed in the cell, while the rest of the decoding is done externally. In a system with N words, a word-organized memory would require N word drivers, while a bit organized memory would require $2N\frac{1}{2}$.

Memory Comparisons

Various forms of semiconductor and magnetic memories are compared in Table 3. A 10⁶ bit memory is assumed for reference. **EEE**

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RCA

Applications For IC Voltage Comparators In High-Impedance Circuitry

by Robert J. Widlar

The IC voltage comparators available in the past have been designed primarily for low-voltage, high-speed operation. As a result, these devices have high-input error currents, which limit their usefulness in high-impedance circuitry. However many applications exist that need drastically reduced error currents and can tolerate ICs with a moderate decrease in speed. By trading off some speed for reduced error currents, considerable improvement in circuit performance can be obtained.

The circuits described in this article demonstrate applications that work nicely despite the use of an IC slower than the 710, the LM106, and similar voltage-comparator ICs.

A zero crossing detector driving a MOS analog switch is shown in Fig. 1. The ground terminal of the IC is connected to V^- ; hence, with ± 15 V supplies, the signal swing delivered to the gate of Q_1 is also ± 15 V. This type of circuit is useful where the gain or feedback configuration of an op-amp circuit must be changed at some precisely determined signal level. Incidentally, it is a simple matter to modify the circuit to work with junction FETs.

A zero crossing detector for a magnetic pickup such as a magnetometer or shaft-position pickoff is shown in Fig. 2. It delivers the output signal directly to DTL or TTL logic circuits and operates from the 5-V logic supply. The resistive divider, R_1 and R_2 , biases the inputs 0.5 V above ground within the common-mode range of the device. An optional offset balancing circuit, R_3 and R_4 , is included.

An interface between high-level logic and DTL or TTL is illustrated in Fig. 3. The input signal, with 0-V and 30-V logic states, is attenuated to 0 V and 5 V by R_1 and R_2 . Resistors R_3 and R_4 set up a 2.5-V threshold level for the comparator so that it switches when the input goes through 15 V. The response time of the circuit can be controlled with C_1 , if desired, to make it insensitive to fast noise spikes. Strobe capability can be provided by the addition of Q_1 and R_5 . With a logic one on the base of Q_1 , approximately 2.5 mA is drawn out of the strobe terminal of the

LM 111 making the output high, independent of the input signal. Because of the low error currents of the LM111 ($0.02 \mu\text{A}$ input offset current and $0.15 \mu\text{A}$ input bias current), it is possible to get input impedances even higher than the $300 \text{ k}\Omega$ obtained with the indicated resistor values.

A comparator for a low-level photodiode operating with MOS logic is shown in Fig. 4. The output changes state when the diode current reaches $1 \mu\text{A}$. At the switching point, the voltage across the photodiode is nearly zero; as a result its leakage current won't cause an error. The output switches between ground and -10 V, driving the data inputs of MOS logic directly.

Peak detector

A positive peak detector is illustrated in Fig. 5. In this application, when the input signal is greater than the voltage retained on C_1 , the circuit behaves like an operational amplifier, forcing the voltage on C_1 to equal the input voltage. When the input voltage drops, the output stage cuts off, leaving the charge on the capacitor. An LM110 voltage follower buffers the output so the load does not rapidly discharge the capacitor. Resistor R_2 provides a controlled discharge on the capacitor and determines the rate at which the circuit will adjust to successive peaks of decreasing amplitude. Since the ground terminal is used as the output, the polarity of the input terminals is reversed, as shown.

In Fig. 6, a ground-referred load is driven from the ground terminal of the LM111. Again the input polarity is reversed. An incandescent lamp, which is the load here, has a cold resistance eight times lower than its resistance during normal operation. When the lamp is switched on, a large inrush current is produced; this can damage the switch. However, the current limiting by the LM111 holds this current to a safe value.

IC voltage comparators with low error currents extend the application range of monolithic comparators to circuits with impedance levels above $1 \text{ k}\Omega$. Although slower than older devices, a low-error-current comparator such as the LM111, with a 200-ns response time, is an order of magnitude faster than op amps used as comparators.

EEE

Author: Bob Widlar is Director of Advanced Circuit Development at National Semiconductor, Santa Clara, Calif.

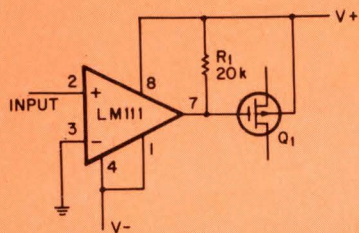


Fig. 1. Zero crossing detector driving analog switch.

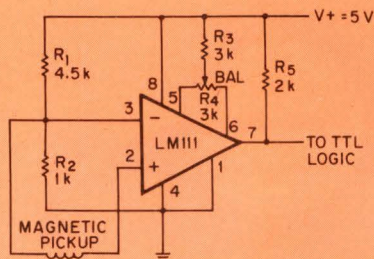


Fig. 2. Detector for magnetic transducer.

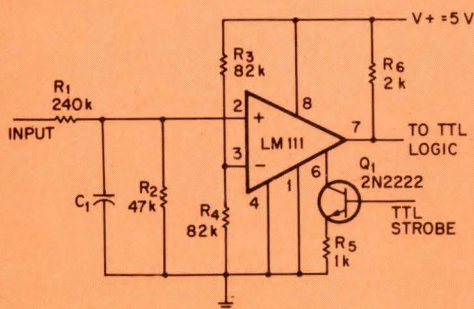


Fig. 3. TTL interface with high level logic.

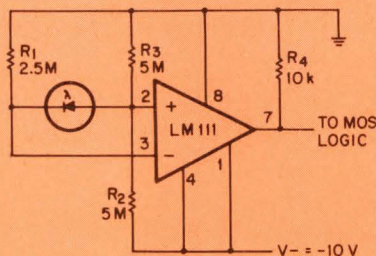


Fig. 4. Comparator for low-level photodiode.

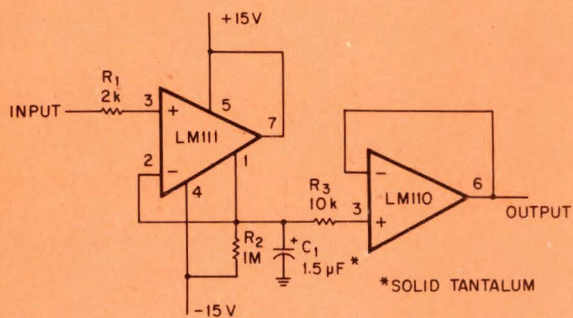


Fig. 5. Positive peak detector.

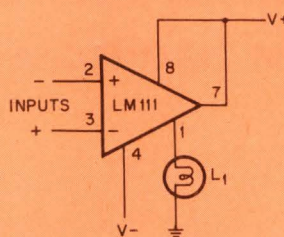


Fig. 6. Driving ground-referred load.

Measurements File



How to measure envelope-delay variation in bandpass filters

by James V. Delwood

□ Delay-measurement techniques have recently been discussed in *EEE* ("How to measure delay," by Sol Black, May 1969). That article was primarily concerned with pulse techniques. Dr. Delwood's article, however, illuminates rf aspects of delay measurements. The article gives two systems for envelope-delay measurement in bandpass filters — a null method and a direct one, using the variation of carrier phase across the filter's passband. □

ENVELOPE DELAY can be measured in different ways. Based on the definition

$$t_d = \frac{d\Phi}{d\omega} \quad (1)$$

Author: Dr. Delwood is bio-engineering consultant and lecturer at State Technical Institute, Memphis, Tenn.

where Φ is the phase and ω the angular frequency, the envelope delay t_d can be derived by differentiating the known phase curve $\Phi(\omega)$ of a given network. However, this method is tedious and time consuming.

Two more direct ways are: (A) by nulling two demodulated rf signals, from the network's input and output, and using their vector difference to find the phase change $\Delta\Phi$; (B) by noting a carrier phase change as its frequency is varied across the passband.

Method A, theory

In Fig. 1 the two demodulated signals from the filter's input and output are combined in such a way that by varying amplitudes and phase it is possible to obtain a null

voltage. The modulated carrier frequency is then shifted to some other portion of the passband and the demodulated signals are again nulled, but this time by manipulating only the amplitudes of the demodulated signals.

The resulting change in null is the measure of the phase change, provided this change is small (Fig. 2). The amplitude V_c is adjusted to null the reference voltage V_{ref} , established in the measurement procedure. The null voltage V_{null} is obtained vectorially as the adder's output:

$$\mathbf{V}_{null} = \mathbf{V}_{ref} + \mathbf{V}_{out} \quad (2)$$

where boldface type is used to indicate vectors.

If, in Fig. 2, $\Delta\Phi \ll \pi$, then $\sin \Delta\Phi \approx \Delta\Phi$. The phase change in radians is thus given by

$$\Delta\Phi = \frac{V_{null}}{V_c} = \frac{V_{null}}{V_{ref}} \quad (3)$$

where V_{null} , V_c and V_{ref} indicate amplitudes.

The time delay is given by

$$t_d = \frac{\Delta\Phi}{\omega_m} \quad (4)$$

where ω_m = angular frequency of the modulating signal in radians/second.

Since it is the slope of the phase curve that is of primary interest, the modulating frequency ω_m must be small with respect to the passband of the filter. Any type of modulation may be used but a-m is preferable.

To minimize errors due to amplitude variation within the passband, detectors and amplifiers are all operated with constant signal levels. This is possible if the signal applied to the network is increased to compensate for the filter loss at the band edges. The attenuator preceding the network under test (Fig. 1) provides this function. As the frequency of the signal is varied toward the band edges, the attenuation is reduced to keep the output of the filter constant.

Measurement procedure

The frequency of the signal generator (HP 606 in Fig. 1), is adjusted to coincide with the center of the filter passband and the

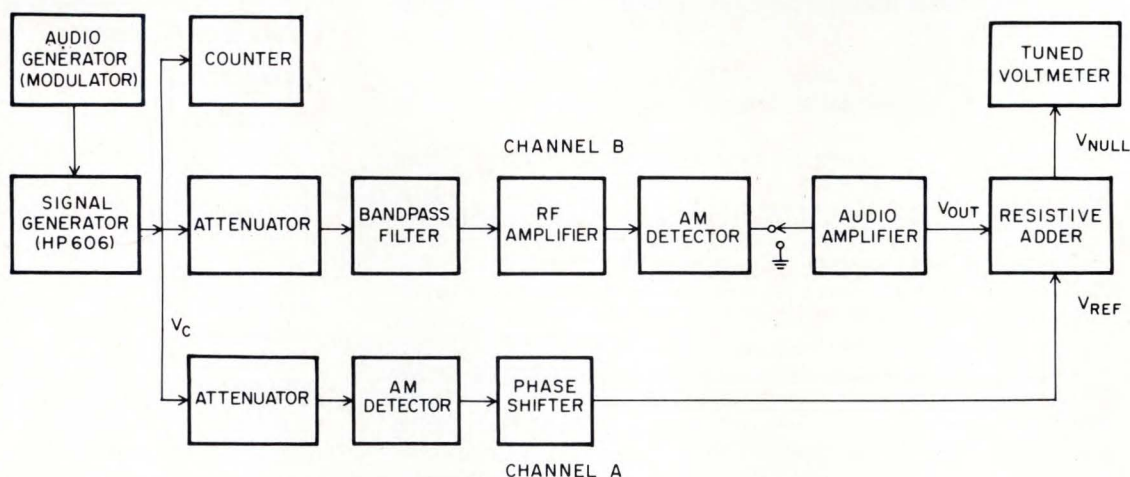


Fig. 1. Setup for envelope-delay measurement using a null system (Method A). An a-m signal is passed through channel A, which includes an a-m detector and phase shifter, and through channel B which includes the filter with the unknown delay and a detector. The output null voltage is directly proportional to the delay for small delays. An attenuator is used to compensate for filter losses at the edges of the passband.



Fig. 2. Vector diagram for null system in Fig. 1.

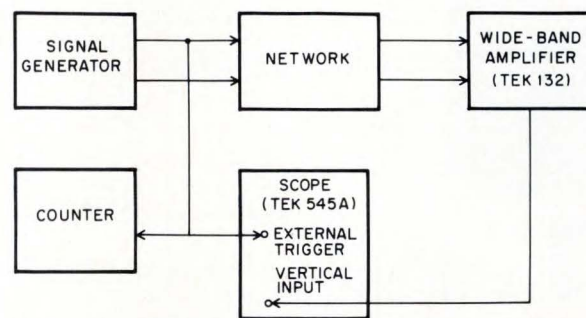


Fig. 3. Setup for envelope-delay measurement using a scope for direct reading of time-delay variation with frequency (Method B). The accuracy of this method is inferior to that of method A.

generator is modulated with a frequency which is very small compared to the bandwidth. Part of the generator's output is diverted into channel A for calibration. For this initial setting, the input to the audio amplifier is shorted while the output of the signal generator is adjusted to provide, say, 100 mV to the tuned voltmeter (HP 202A wave analyzer in Fig. 1). The audio amplifier is then returned to normal position.

The channel-B attenuator is initially set to 3 to 5 dB and the audio amplifier is adjusted to attempt null on the wave analyzer. The phase shifter in channel B must also be varied to obtain null. By varying those two controls, a stable null of about 10 microvolts can be obtained.

The envelope-delay change at

some other frequency can now be found. For example, if the delay at the -1-dB point in the filter is desired, remove 1 dB from the attenuator and vary the frequency of the signal source until a new null is obtained. No other controls are adjusted. The voltage of the new null is noted and the delay can now be computed.

For example, let

$$\omega_m = 2\pi 50 \text{ rad/s}$$

$$V_{ref} = 100 \text{ mV}$$

$$V_{null} = 10 \text{ } \mu\text{V}$$

$$V_{null} \text{ (at } -1\text{-dB point on slope of filter)} = 50 \text{ } \mu\text{V}$$

then according to Eq. 3

$$\Delta\Phi = \frac{(50 - 10) \times 10^{-6}}{100 \times 10^{-3}}$$

$$= 4 \times 10^{-4} \text{ radians}$$

$$t_d = \frac{4 \times 10^{-4}}{2\pi 50} = 1.27 \text{ } \mu\text{s}$$

The amplifier can be used as a fine-adjust amplitude control. To obtain the delay at the -2-dB point, remove an additional 1 dB from the attenuator. Other points in the passband are similarly obtained.

Reliability

The phase stability of the various elements must not contribute to the overall inaccuracy of the system. The setup in Fig. 1 is based on operation at a fixed amplitude level. The stability of the phase shifter has to be determined as well as that of any amplifier used. Careful monitoring of the frequency of the signal generator (using a counter), is needed to

BE CAREFUL

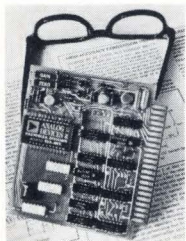
OF FALSE ECONOMY IN DO-IT-YOURSELF A/D CONVERTERS

Most engineers recognize that high accuracy A/D converters (12 bits and up) are most economical when purchased as finished products from specialized manufacturers.

Sometimes, however, it is tempting to make converters "in-house" when lesser accuracy is required (8 or 10 bits).

This is partly because if one considers only the obvious costs (parts, assembly time, etc.) the trade-offs seem attractive. Often overlooked, however, are the "hidden costs" such as test and inventory, "de-bugging" time, calibration time, etc. Also, lead time on parts may become critical, jeopardizing an entire program.

The key, of course, is quantity. Our experience indicates that the point at which it becomes profitable to build your own converter is around 750 units per year. *For 8 or 10 bit applications, we recommend our fully calibrated, tested and guaranteed, ADC-8H or ADC-10H.* A free pamphlet suggesting some things to consider regarding in-house-converter manufacturer is available from Analog Devices on request along with comprehensive data on the ADC-H series converters. Use the reader service card or contact your nearest Analog Devices Sales Office.



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Digital Control Inputs:	TTL, DTL Compatible
Analog Input Options:	0 to +10V, 0 to +5V 0 to -10V, ±10V, ±5V
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**ANALOG
DEVICES**

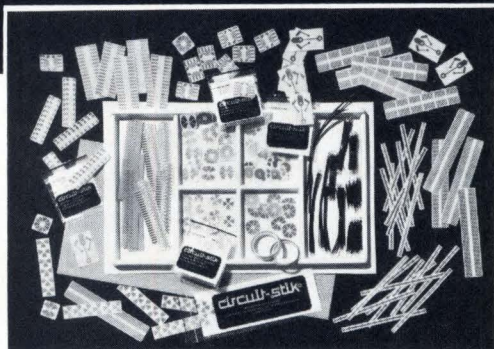
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Circle 192 on Reader Service Card

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check errors due to generator instability. The method presented in Fig. 1 permits measurements to a few microseconds.

Method B, theory

Based on scope readings, this method (Fig. 3) is slightly less accurate than method A. The scope is triggered with an unmodulated rf and the filter's output is applied to the scope's vertical input. An amplifier is used to assure stable triggering.

The frequency is then shifted slightly and the change in zero-crossing time is noted. From the definition of time delay

$$t_d = \frac{\Delta\Phi}{\Delta\omega} = \frac{\omega_2 t_2 - \omega_1 t_1}{\omega_2 - \omega_1} \quad (5)$$

where ω_1 = initial angular frequency.

ω_2 = shifted angular frequency

t_1 = initial time delay

t_2 = new time delay.

With $\omega_2 - \omega_1 = \Delta\omega$

$t_2 - t_1 = \Delta t$

and assuming

$$t_2 \Delta\omega \ll \omega_1 (t_2 - t_1), \quad (6)$$

a valid assumption for most band-pass filters having more than 2 poles, we get

$$t_d \simeq \frac{\Delta t \omega_1}{\Delta\omega} \quad (7)$$

$\Delta\omega$ must be kept small compared with ω_1 .

Application

Select a suitable time base such as 0.02 μ s/cm and obtain sync. Obtain a zero crossing which is centered on the screen. Vary the carrier frequency by a known amount, say ± 5 Hz, and note the crossing change. Assuming a 5-cm change and a center frequency of 5×10^5 Hz one gets, using Eq. 6,

$$t_d = \frac{0.02 \times 5 \times 2\pi \times 5 \times 10^5}{2\pi \times 10} = 5 \text{ ms}$$

Another frequency is then selected and the procedure repeated. The difference between the two readings is the time-delay variation. **EEE**

New Books

ELECTRONIC TEST AND MEASUREMENT HANDBOOK

by John J. Schultz. Tab Books. 220 pp. \$7.95

• This is an introduction to testing methods with bare, but adequate, use of theory and an emphasis on practical methods to bypass the snags likely to be encountered in testing. The coverage is mostly audio-thru-video communications and display equipment. An effort is made to show how to set up test equipment to accomplish specific performance or parameter measurements.

There are eight chapters. The first two cover procedure and equipment. This is followed by chapters on receiver and transmitter circuits, antennas and transmission lines, and audio and video equipment. One chapter outlines subjects such as teletype equipment, FSK converters, mobile power supplies, inverters and telephone line-patching equipment. The last chapter, covering system and interference tests might have been expanded. There is a short appendix with the usual color-code charts, dB-to-voltage conversions, etc.

Precision Dc Measurements and Standards. Davis S. Luppold. Addison-Wesley. 251 pp. \$14.50. ☐ Rather broad, dealing largely with resistance-bridge measurements.

Absolute Measurements in Electricity and Magnetism. Andrew Gray. Dover. 819 pp + index. \$4.00 (paperbound). ☐ Thorough coverage in reprint of a reference classic.

Theory of Optimal Control and Mathematical Programming. M. D. Canon, C. D. Cullum, Jr. and E. Polak. McGraw-Hill. 276 pp + glossary and index. \$18.50. ☐ Good technical information to be used as graduate or reference text.

Synthesis of RC Active Filter Networks. S. S. Haykin. McGraw-Hill. 166 pp + index. \$12.00. ☐ Examines the circuit properties of negative-impedance converters, amplifiers and gyrators and demonstrates their uses in the synthesis of inductorless filters.



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SU 2366A	10	10	20	100
SU 2367A	10	25	20	100
SU 2368A	15	25	20	100
SU 2369A	20	40	20	100
*Typical				

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SN54/7443	Excess-3-to-Decimal Decoder*
SN54/7444	Excess-3-Gray-to-Decimal Decoder*
SN54/7445	BCD-to-Decimal Decoder/Driver*
SN54/7446	BCD-to-7-Segment Decoder/Driver*(30V)
SN54/7447	BCD-to-7-Segment Decoder/Driver*(15V)
SN54/7448	BCD-to-7-Segment Decoder*
SN54/7449	BCD-to-7-Segment Decoder*
■ SN54/74141	BCD-to-Decimal Decoder/Driver*
SN54/74145	BCD-to-Decimal Decoder/Driver*
SN54/74154	4-to-16-Line Decoder/Demultiplexer*
■ SN54/74155	Dual 2-to-4-Line Decoder/Demultiplexer
■ SN54/74156	Dual 2-to-4-Line Decoder/Demultiplexer (0-C)

MEMORIES/LATCHES

SN54/7475	Quad Bistable Latch*
SN54/7477	Quad Bistable Latch*
SN54/7481	16-Bit RAM*
SN54/7484	16-Bit RAM, Gated Write Inputs*
■ SN54/7488	256-Bit ROM, Custom Programmed*
SN7489	64-Bit RAM*
SN54/74100	Dual Quad Bistable Latch
■ SN54/74170	4-by-4 Register File (Buffer Memory)

ARITHMETIC ELEMENTS

SN54/7480	Gated Full Adder*
SN54/7482	2-Bit Binary Full Adder*
SN54/7483	4-Bit Binary Full Adder*
■ SN54/7485	4-Bit Magnitude Comparator
■ SN54/74L85	4-Bit Magnitude Comparator*
SN54/7486	Quad 2-Input Exclusive-OR*
SN54/74L86	Quad 2-Input Exclusive-OR*
SN54/74H87	4-Bit True/Complement*
■ SN54/74181	4-Bit Arithmetic Logic Unit, Function Generator*
■ SN54/74182	Look-Ahead for Arithmetic Logic Unit*
■ SN54/74H183	Dual Carry-Save Full Adder

■ New circuit introduced 1970 *Multi-source product

SHIFT REGISTERS

SN54/7491A	8-Bit*
SN54/74L91	8-Bit
SN54/7494	4-Bit (Parallel-In, Serial-Out)*
SN54/7495	4-Bit Universal*
SN54/74L95	4-Bit Universal*
SN54/7496	5-Bit (Dual Parallel-In/Out)*
SN54/74L98	4-Bit Data Selector/Storage Register
SN54/74L99	4-Bit Universal
■ SN54/74164	8-Bit Serial-In, Parallel-Out*
■ SN54/74165	8-Bit Parallel-In, Serial-Out*
■ SN54/74166	Synchronous Parallel-Load 8-Bit
■ SN54/74198	Universal 8-Bit Parallel-In/Out, Left/Right
■ SN54/74199	8-Bit Parallel-In/Out, J-K Inputs

DATA SELECTORS/MULTIPLEXERS

SN54/74150	16-Bit Data Selector*
SN54/74151	8-Bit Data Selector*
SN54/74152	8-Bit Data Selector
SN54/74153	Dual 4-to-1-Line Data Sel./Multiplexer*

COUNTERS

SN54/7490	Decade*
SN54/74L90	Decade
SN54/7492	Divide-by-12*
SN54/7493	4-Bit Binary*
SN54/74L93	4-Bit Binary*
■ SN54/74160	Synchronous 4-Bit Decade*
■ SN54/74161	Synchronous 4-Bit Binary*
■ SN54/74162	Fully Synchronous 4-Bit Decade
■ SN54/74163	Fully Synchronous 4-Bit Binary
■ SN54/74190	Synchronous 4-Bit Up/Down Decade, 1-Line Mode Control*
■ SN54/74191	Synchronous 4-Bit Up/Down Binary, 1-Line Mode Control*
■ SN54/74192	Synchronous 4-Bit Up/Down Decade*
■ SN54/74193	Synchronous 4-Bit Up/Down Binary*
■ SN54/74196	Asynchronous Presettable Decade*
■ SN54/74197	Asynchronous Presettable Binary*

PARITY GENERATOR

SN54/74180	8-Bit Parity Generator/Checker
------------	--------------------------------

SCHOTTKY-CLAMPED TTL CIRCUITS:

These represent the latest development in TTL integrated circuits. A totally new technology, TI's Schottky-clamped TTL circuits combine the high speed of unsaturated logic and the low power of TTL saturated logic: 3 ns at 20 mW. Here's a brand-new list of recently announced devices. For more information on this fastest TTL family, circle 191 on the Reader Service Card.

■ SN74S00	Quad 2-Input Positive NAND Gate
■ SN74S01	Quad 2-Input NAND Gate, Open-Collector Outputs
■ SN74S04	Hex Inverter
■ SN74S10	Triple 3-Input NAND Gate
■ SN74S11	Triple 3-Input AND Gate
■ SN74S20	Dual 4-Input Positive NAND Gate
■ SN74S22	Dual 4-Input NAND Gate, Open-Collector Outputs
■ SN74S112	Dual J-K Negative-Edge Triggered Flip-Flop, Separate Preset, Clear and Clock
■ SN74S113	Dual J-K Flip-Flop, Separate Clock
■ SN74S114	Dual J-K Flip-Flop, Common Clock

SSI/TTL CIRCUITS:

STANDARD SSI CIRCUITS

SN54/7400	Quad 2-Input NAND Gate*
SN54/7401	Quad 2-Input NAND Gate, Open-Collector Output*
SN54/7402	Quad 2-Input NOR Gate*
SN54/7403	Quad 2-Input NAND Gate, Open-Collector Output*
SN54/7404	Hex Inverter*
SN54/7405	Hex Inverter, Open-Collector Output*
■ SN54/7406	Hex Inverter Buffer/Driver, Open-Collector High-Voltage Output
■ SN54/7407	Hex Buffer/Driver, Open-Collector High-Voltage Output
■ SN54/7408	Quad 2-Input Positive AND Gate*
■ SN54/7409	Quad 2-Input Positive AND Gate*
SN54/7410	Triple 3-Input NAND Gate*
■ SN54/7412	Triple 3-Input NAND Gate, Open-Collector Output
■ SN54/7413	Dual 4-Input NAND Schmitt Trigger*
■ SN54/7416	Hex Inverter Buffer/Driver, Open-Collector High-Voltage Output
■ SN54/7417	Hex Buffer/Driver, Open-Collector High-Voltage Output
■ SN54/7420	Dual 4-Input NAND Gate*
■ SN54/7423	Expandable Dual 4-Input Positive NOR Gate with Enable
■ SN54/7425	Dual 4-Input Positive NOR Gate with Enable*
■ SN54/7426	Quad 2-Input High-Voltage Interface NAND Gate*
■ SN54/7427	Triple 3-Input NOR Gate*
SN54/7430	8-Input NAND Gate*
■ SN54/7432	Quad 2-Input OR Gate*
■ SN54/7437	Quad 2-Input NAND Buffer*
■ SN54/7438	Quad 2-Input NAND Buffer with Open-Collector Output
SN54/7440	Dual 4-Input NAND Buffer*
SN54/7450	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate*
SN54/7451	Dual 2-Wide 2-Input AND-OR-INVERT Gate*
SN54/7453	Expandable 4-Wide 2-Input AND-OR-INVERT Gate*
SN54/7454	4-Wide 2-Input AND-OR-INVERT Gate*
SN54/7460	Dual 4-Input Expander*
SN54/7470	J-K Flip-Flop*
SN54/7472	J-K Master-Slave Flip-Flop*
SN54/7473	Dual J-K Master-Slave Flip-Flop*
SN54/7474	Dual D-Type Edge-Triggered Flip-Flop*
SN54/7476	Dual J-K Master-Slave Flip-Flop, Preset and Clear*
SN54/74104	Gated J-K Master-Slave Flip-Flop*
SN54/74105	Gated J-K Master-Slave Flip-Flop*
SN54/74107	Dual J-K Master-Slave Flip-Flop, Preset and Clear*
■ SN54/74110	Gated J-K Master-Slave Flip-Flop, Data Lockout
■ SN54/74111	Dual J-K Master-Slave Flip-Flop, Data Lockout
SN54/74121	Monostable Multivibrator*
■ SN54/74122	Retriggerable Resetttable Monostable Multivibrator*
■ SN54/74123	Dual Retriggerable Resetttable One-Shot*

HIGH-SPEED SSI CIRCUITS

SN54/74H00	Quad 2-Input NAND Gate*
SN54/74H01	Quad 2-Input NAND Gate, Open-Collector Output*
SN54/74H04	Hex Inverter*
SN54/74H05	Hex Inverter, Open-Collector Output*
SN54/74H10	Triple 3-Input NAND Gate*
SN54/74H11	Triple 3-Input AND Gate*
SN54/74H20	Dual 4-Input NAND Gate*
SN54/74H21	Dual 4-Input AND Gate*
SN54/74H22	Dual 4-Input NAND Gate, Open-Collector Output*
SN54/74H30	8-Input NAND Gate*
SN54/74H40	Dual 4-Input NAND Buffer*
SN54/74H50	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate*
SN54/74H51	Dual 2-Wide 2-Input AND-OR-INVERT Gate*
SN54/74H52	Expandable 4-Wide 2-2-2-3-Input AND-OR Gate*
SN54/74H53	Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate*
SN54/74H54	4-Wide 2-2-2-3-Input AND-OR-INVERT Gate*

SN54/74H55	Expandable 2-Wide 4-Input AND-OR-INVERT Gate*
SN54/74H60	Dual 4-Input Expander*
SN54/74H61	Triple 3-Input Expander*
SN54/74H62	4-Wide 3-2-2-3-Input AND-OR Expander*
SN54/74H71	J-K Flip-Flop with AND-OR Input*
SN54/74H72	J-K Master-Slave Flip-Flop*
SN54/74H73	Dual J-K Flip-Flop, Separate Clock*
SN54/74H74	Dual D-Type Edge-Triggered Flip-Flop*
SN54/74H76	Dual J-K Flip-Flop, Preset and Clear Inputs*
SN54/74H78	Dual J-K Flip-Flop, Preset and Clear Inputs*
SN54/74H101	J-K Flip-Flop, AND-OR Inputs
SN54/74H102	J-K Flip-Flop, AND Inputs
SN54/74H103	Dual J-K Flip-Flop, Separate Clock Inputs
SN54/74H106	Dual J-K Flip-Flop, Preset and Clear Inputs
SN54/74H108	Dual J-K Flip-Flop, Preset and Clear Inputs

LOW-POWER SSI CIRCUITS

SN54/74L00	Quad 2-Input NAND Gate*
■ SN54/74L01	Quad 2-Input NAND Gate, Open-Collector Output
■ SN54/74L02	Quad 2-Input NOR Gate
■ SN54/74L03	Quad 2-Input NAND Gate, Open-Collector Output
SN54/74L04	Hex Inverter*
SN54/74L10	Triple 3-Input NAND Gate*
SN54/74L20	Dual 4-Input NAND Gate*
SN54/74L30	Single 8-Input NAND Gate*
SN54/74L51	Dual 2-Wide 2-Input/2-Wide 3-Input AND-OR-INVERT Gate*
SN54/74L54	2-2-3-3-Input AND-OR-INVERT Gate*
SN54/74L55	2-Wide 4-Input AND-OR-INVERT Gate*
SN54/74L71	R-S Master-Slave Flip-Flop*
SN54/74L72	J-K Master-Slave Flip-Flop*
SN54/74L73	Dual J-K Master-Slave Flip-Flop*
SN54/74L74	Dual D-Type Edge-Triggered Flip-Flop*
SN54/74L78	Dual J-K Master-Slave Flip-Flop, Common Clear and Clock*

Looking for low-cost solutions to high-performance design problems?

**You'll find a lot of new ones in TI's 54/74 line
—still your broadest choice
of state-of-the-art TTL integrated circuits.**

If you're going to design the best equipment for your customers, you need the best tools available. Design after design has proven TTL the top logic tool from a standpoint of circuit efficiency and cost effectiveness.

Not for your state-of-the-art system? Look again. A lot has happened in the last few months. Enough to justify a careful review of your latest logic diagrams and product plans.

Take another look at the TTL leader—TI's 54/74 family.

MSI choice and complexity. Begin with the opposite page. Here, to help you reduce package count, simplify designs and improve performance, is an unmatched array of catalog MSI functions. The line has just about doubled in the past nine months and there are still more to come of ever-increasing complexity.

SSI back-up in depth. But in using TTL/MSI, you need the substantial back-up of versatile SSI circuits.

Check the opposite page again.

Four speed/power choices. Within TI's big TTL family, you have a selection of four speed/power ranges to help optimize your designs. There are 1 mW per gate low power circuits, standard- and high-speed circuits *plus* the revolutionary new Schottky-clamped TTL functions which attain speeds of 3 ns at 20 mW.

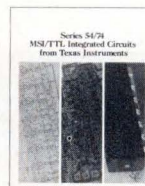
Complete compatibility. Even with this wide choice, you avoid compatibility problems. All members of TI's Series 54/74 family are designed to work together—saving you both design and component costs.

And TTL logic is also most economical on the basis of cost-per-function...in whatever package types you need: ceramic and plastic DIP or flat pack.

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parts alone) in all three packages and in both temperature ranges. More than 100 authorized distributor locations stock full inventories of TI's TTL circuits...representing an additional stock, in the field, of more than 300,000 MSI parts.

And if your system requires multiple sources, you'll find more of TI's 54/74 line is backed up by other reputable semiconductor suppliers. It makes good business sense. (Asterisks on opposite page indicate multiple-source devices.)



The time is now to consider TTL for today and tomorrow. The decision-making facts are in our new MSI brochure, CB-125.

For your copy, circle 189 on the Reader Service Card or write Texas Instruments Incorporated, P.O. Box 5012, M.S. 308, Dallas, Texas 75222. Your authorized TI Distributor has copies, too.



TEXAS INSTRUMENTS
INCORPORATED

Products Of The Month

Semiconductors

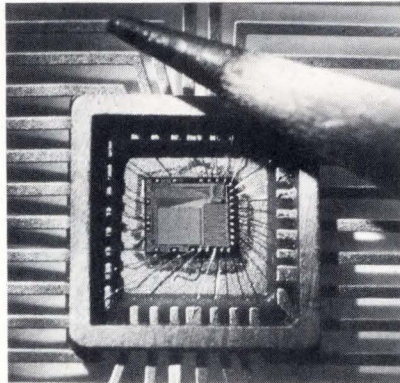
Boldface numbers following each product refer to those you can circle on the reader inquiry card for further information.

Schottky-diode 256-bit RAM, 3102, for main-frame memories. 512 memory units plus 32 decoders will store 4096 32-bit words. TTL compatible. Access time, 120 ns max, diss., 1.5 mW per bit. 16-lead DIP. \$51.20 (100-999). Decoder costs \$12.80 (100-999). INTEL. **305**

MOS 256-bit ROM, 8224, reads 32

eight-bit words. Compatible with DTL/TTL inputs, outputs. Converts 7-bit ASCII alphabet code to 8-bit EBCDIC alphabet code. Propagation delay time, 50 ns; diss, 310 mW. Full word decoding on chip. 16-pin DIP. \$17.00 (100 up). SIGNETICS. **306**

Static 3072-bit MOS ROM, UA2572, with 256-word by 12-bit memory or-



ganization. Access time, 750 ns. Bipolar compatible. Programmable chip select for expansion. Temp., -55°C to +125°C. UNISEM. **307**

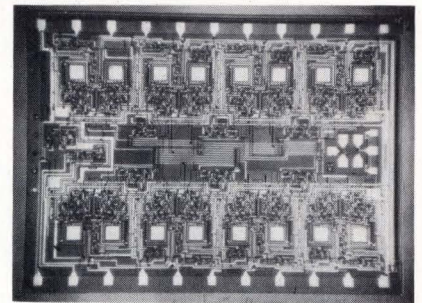
Silicon-nitride MOS shift-register, TMS3406LR, dual 100-bit type. First entry in low-threshold compatible shift-register field for manufacturer. Dynamic register. Propagation delay, 120 ns. 8-pin TO-100 metal can. \$6.50 (100-249). TEXAS INSTRUMENTS. **309**

Dynamic shift register, MM512, 512 bits. Standard +5 and -12 power supply. Bipolar compatible. Guaranteed operating frequency, 600 Hz with



output tap at 500th bit. TO-5 or DIP. \$5.00 (100-999). NATIONAL SEMICONDUCTOR. **308**

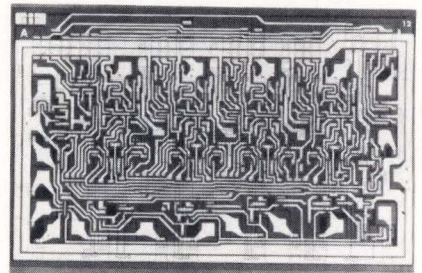
Shift registers, 64-word by 24-bit ROMs, 45-character alpha numeric decoders for segmented displays. 5-bit to 32-line binary decoders suitable for



decoding ASCII control characters, and 8-bit, synchronous binary counters and timing generators with preselected decoding of timing outputs. New company founded by ex-Honeywell employees. KENICS. **310**

Four-phase, dynamic shift register, 1024 bits. Diss rate, 0.15 mW/bit at 1 MHz max, frequency range, 10 KHz to 1 MHz. 10-lead TO-100. NORTH AMERICAN ROCKWELL. **311**

Up-down, counters, 9306/Am2501, replace Fairchild 9306 BCD synchronous counters. Binary Hexadecimal ver-



sion of 9306 designated Am2501 also available. Max turn-off, 23 ns, max turn-on, 39 ns. 24-pin DIP. ADVANCED MICRO DEVICES. **312**

Series 74, US7442A, 4- to 10-line decoder. Translates 4-wire BCD (1,2,4,8) signal into 10-wire decimal signal. May be used for 3-line binary to 8-line octal conversion. 16-pin plastic DIP. SPRAGUE. **313**

Series 74, new MSI devices, in ceramic DIPs. 7480 gated full adder, 7482 2-bit binary full adder, 7490 decade

This Month's ICs

Schottky-diode bipolar RAM, \$51.20. INTEL. **305**
MOS 256-bit ROM, \$17.00. SIGNETICS. **306**
Static 3072-bit MOS ROM. UNISEM. **307**
Dynamic 512-bit register, NATIONAL SEMICONDUCTOR. **308**
Dynamic silicon-nitride register, TEXAS INSTRUMENTS. **309**
ROMs, shift registers, KENICS. **310**
Dynamic, four-phase 1024-bit register, NAR. **311**
Counters, ADVANCED MICRO DEVICES. **312**
TTL ICs, SPRAGUE. **313**
Series 74 TTL, \$2.90. FAIRCHILD. **314**
Compensated ECL, \$2.05. FAIRCHILD. **315**
Power op amp, \$14.50. DICKSON. **316**
Op amps, \$3.25. SILICON GENERAL. **317**
Improved 741s, \$7.25. BURR-BROWN. **318**
LID-packaged 741s, \$8.00. DICKSON. **319**
Superior 741s, \$4.50. ANALOG DEVICES. **320**
Receiver, transmitter, \$18.70. GENERAL INSTRUMENT. **321**
Driver, receiver, \$6.00. MOTOROLA. **322**

This Month's Transistors and Diodes

Transistor chips, 89¢. POWER PHYSICS. **323**
High-voltage transistors, 41¢. FAIRCHILD. **324**
Power transistors, \$18.36. PIRGO. **325**
Infrared detectors. MULLARD. **326**
Varactor diodes. DOW CORNING. **327**
Silicon photosensors. CLAIREX. **328**
Varactor diodes. CRYSTALONICS. **329**

**...sometimes
it's the products
that make the
leaders...**



**ZM1000
Numerical Indicator**

The industry's first and only readout tube ever designed specifically for high volume users. More new products are using the ZM1000 today than any other readout tube on the market.



**ZM1200 PANDICON*
14-Decade Readout**

The only tried and proven multi-decade readout tube on the market. Needs only 27 external connections compared with 168 connections needed to display 14 decades with single-decade tubes.

Product-superiority ... and nothing else ... is what made Amperex a leading supplier of numerical indicator tubes. Our ZM1000 is being designed into more new products than any other readout tube and our ZM1200 is still the only tried and proven multi-decade readout tube available. If this isn't the perfect example of the products making the leader — what is?

At our Briarcliff Manor Laboratories we are studying "no-power" electro-chemical readouts, reflective-surface readouts visible in bright sunlight and several other "laboratory curiosities." We are also developing imminent new products including dot matrix readouts that can be programmed to display any desired character.

When it comes to applications, we support what we sell. Buy any Amperex readout tube and we'll supply you with just about every component your drive circuit requires, whether you choose IC's, discrete semiconductors or passive components.

Only one IC decoder-driver (Amperex FCL III, a standard 7400 series device) is needed to drive the

ZM1200. Technical details of the use of the FCL III and plans for a discrete-component alternative circuit are available on request. The ZM1200 offers floating decimal location at no extra cost, along with punctuation marks that permit "pointing-off" large numbers into convenient groups. In thousand-lot orders, the price per digit is less than \$2.00.

The ZM1000 at \$2.95 in thousand lots provides big economies in application as well as in initial cost. In volume, it sells for less than \$2.00. For anode-strobing, the ZM1005 is available.

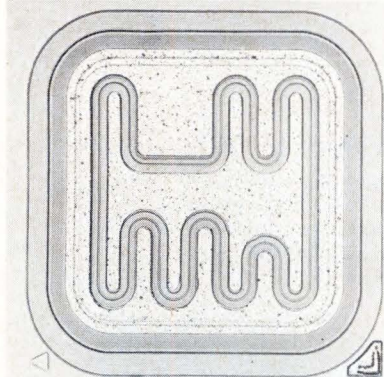
For specifications and drive-circuit information on the ZM1000, ZM1005 and ZM1200 PANDICON, write: Amperex Electronic Corporation, Semiconductor and Microcircuits Division, Slatersville, Rhode Island 02876.

Amperex®

TOMORROW'S THINKING IN TODAY'S PRODUCTS
A NORTH AMERICAN PHILIPS COMPANY

counter, 7491 8-bit shift register, 7492 divide-by-12 counter, 7493 4-bit binary counter, 7475 quad latch. Replace Texas Instruments devices. \$2.90 up (100-999). FAIRCHILD. **314**

Emitter-coupled-logic (ECL), 9500, new line. On-chip temperature compensation. OR/NOR gates, dual flip-flops, 8-input multiplexers. Typ propagation delays, 2 ns. 2-k Ω pulldown resistors. Multiplexer can be used as universal function generator. 16-pin



DIPs. \$2.05 to \$17.50 (100 up). FAIRCHILD. **315**

Power op amp, DPA500, with 2-W output. Internal frequency compensation. Complementary emitter follower. Two-transistor output stage with 741 op amp. \$14.50 (100-999). DICKSON. **316**

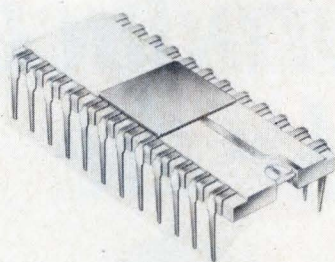
Op amps, SG101A series, replace National Semiconductor LM101A series. Offset voltage, 3 mV max; input current, 100 nA max, offset current, 20 nA max. TO-99 8-pin metal can and TO-116 14-pin DIP \$3.25 (100 up). SILICON GENERAL. **317**

Improved 741, 3500, input bias current 10 nA. Thermal drift, 0.3 nA/ $^{\circ}$ C, slew rate, 1.5 V/ μ s. Input impedance, 5,000 M Ω , common-mode, and 10 M Ω , differential. Common-mode rejection, 90 dB; gain, 100 dB. Power supply levels, ± 3 to ± 20 V. Power supply sensitivities, 0.2 dB/V, 20 μ V/V, and 0.1 nA/V. \$7.25 (100 up). BURRBROWN. **318**

741 LID, MH1A-741, also 709 in LID (leadless inverted device) package, for hybrid circuitry, with contamination-proof sealant covering device \$8.00 for 741; \$7.30 for 709. DICKSON. **319**

Superior 741 ICs, AD502J, K, 4-12 nA max offset current. Max bias current, 7-25 nA at 25 $^{\circ}$ C. Darlington input circuitry. TO-99. \$4.50-\$8.00 (100 up). ANALOG DEVICES. **320**

Terminal receiver, transmitter, AY-5-1008, 1010, silicon-nitride devices. Power consumption, 150 mW. Accepts up to 9 bits of parallel information, adds the required start and stop bits to convert serial data. AY-5-1008 is serial-in/10-bit parallel-out shift register with input word length externally selectable for 5, 6, 7, or 8 data bits. 24-lead DIPs. AY-5-1010,



\$18.70; AY-5-1008, \$24.15. GENERAL INSTRUMENT. **321**

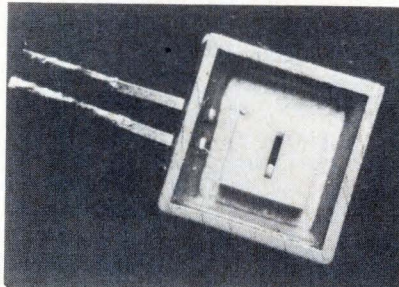
Quad line driver, line receiver, MC1488L, MC1489L, meet EAI interface standard RS-232-C. The MC1488L line driver consists of 4 NAND gates; 3 two-input gates and a single-input gate. Output voltage, 25V; output impedance, 300 Ω , output currents 5A; driver slew rate, 30 V max. Driver \$7.00, receiver, \$6.00. MOTOROLA. **322**

Power transistor chips, CH3055, CH3232, CH3226, for hybrid circuitry. Mounted on discs with nickel plated leads. Can dissipate 117 W, voltages 35 to 110 V, current gain 20 at 12 V; temp, 200 $^{\circ}$ C, 89¢ to 99¢. POWER PHYSICS. **323**

High-voltage npn transistors, 2N5964, 2N5830-3, complements to 2N4888 and 2N4889 pnp amplifiers. Capacitance, 4 pF max. Voltages to 180 V, diss to 700 mW, leakage, 50 nA max. 41¢ to 56¢ (100 up). FAIRCHILD. **324**

Power transistors, JAN approved line, 2N2880, 2N3749, 2N3996 - 2N3999. Available with JAN and JAN-TX (high-reliability) prefixes \$18.36 up (1-99). PIRGO. **325**

Infrared detectors, 801 series, cadmium mercury telluride. Spectral response



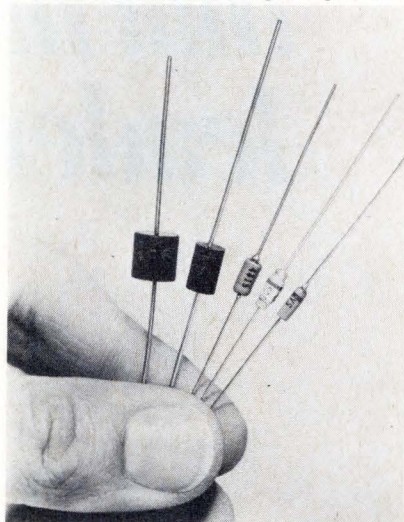
range 4-6 microns; time constant, 1.5 μ s max; response time, 300 ns. Sensitive area, 230 square microns; noise equivalent resistance less than 1 k Ω . MULLARD. **326**

Plastic varactor diodes, new series, 5-1 capacitance ratios from 3 to 30 V. Minimum Q, 300. Withstand 14-pound pull test. Axial-lead package. DOW CORNING. **327**

Silicon photosensors, CLT2010, cover light sensitivity range from 0.2 mA to 3 mA at 5 mW/cm 2 . Max collector-

to-emitter voltages, 15 to 50 V. Narrow 3:1 light sensitivity tolerance range. 3-lead TO-18 with flat window. CLAIREX. **328**

Varactor diodes, comprehensive line, 150-1500 pF. Diss, 500 mW, voltages to 100 V. DO-7, DO-14 packages, also

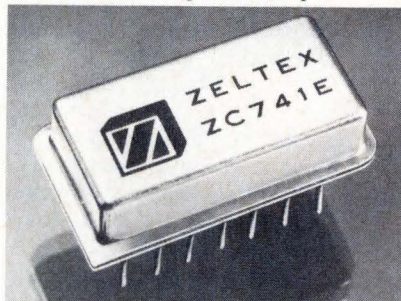


other packages available. For delay line, tuning, synthesizer, oscillator applications. CRYSTALONICS. **329**

Packaged Circuits

High-voltage op amps, A-300 and A-301, to operate with supply voltages from ± 50 V to ± 150 V. Input bias current below 10 pA. FET input stage. Accept common mode voltages to ± 115 V with typical CMRR of 100 dB. Open loop-gain 100 dB. Slew rate 10 V/ μ s. Input impedance $10^{11}\Omega$. Input offset 3 mV, adjustable to zero. Offset drift 50 μ V/ $^{\circ}$ C (A-300) or 25 μ V/ $^{\circ}$ C (A-301). 1.5 \times 1.5 \times 0.5 in. \$80 (A-300 in 1-9) or \$90 (A-301 in 1-9). Stock. INTECH. **216**

Programmable-gain amplifiers, ZC741E and ZC801E, with over 500 selectable gain and circuit configurations achieved by interconnecting terminal pins. Gain



programmable from 0.004 to 250. Built-in feedback and input network, has tolerance of 0.1% and tempco of 10 ppm/ $^{\circ}$ C. Dc gain 100,000. Gain-bandwidth product 4 MHz. Voltage drift 30 μ V/ $^{\circ}$ C. Input current 15 pA.

(Continued on page 60)



The trio that performs like an orchestra.



Andante. Start with the Trim Trio, a versatile concept that lets you use submini coax, machined or strip formed contacts intermixed in the same connector block.

Allegro. Use the *same contacts, same tooling* for rectangular MS Hyfen® connectors, or Bantam™ miniature round connectors. You get the convenience and savings of common contacts used

in a broad selection of connectors and hardware accessories. Countless design variations are possible for applications in computers, communications equipment, medical electronics, numerical controls and avionics equipment.

Fortissimo. Burndy installation tooling harmonizes with Trim Trio connectors for built-in quality control, whether you crimp one at a time with a hand tool, or

3000 per hour with a Hyfematic™.

Crescendo. For more details send for our catalog. See what beautiful music you can make—from breadboard to production—with the Trim Trio.

Encore! Encore!

 **BURNDY**
Bantam Products/Norwalk, Connecticut

INTERNATIONAL SALES HEADQUARTERS & MANUFACTURING FACILITIES

Hermetically-sealed 14-pin DIP-style package. \$20 (ZC741E in prod qty) or \$43 (ZC801E in prod qty). Stock. ZEL. **217**

Chopper-stabilized amplifier, A-241, with special circuitry that virtually eliminates noise spikes. Wideband current noise 100 pA pk-pk (10 Hz to 10 kHz). Noise voltage 0.8 μ V pk-pk (0.01 Hz to 1 Hz). Drift 50 nV/ $^{\circ}$ C. Offset voltage 10 μ V. Input bias current 15 pA. Current drift 0.5 pA/ $^{\circ}$ C. $1.5 \times 1.5 \times 0.5$ in. \$97 (1-9). Stock. INTECH. **218**

Fast-settling op amp, FST-152, with settling time of 0.6 μ s to within 0.01%. Overload recovery time 1 μ s. FET input. Slew rate 75 V/ μ s. Dc gain 150,000. Output ± 10 V at 20 mA. Guaranteed minimum CMRR 3000. Common-mode voltage ± 10 V. High CMRR allows amplifier to maintain settling speed in non-inverting mode. Unity gain freq 12 MHz. Offset-voltage drift 50 μ V/ $^{\circ}$ C (A version), 25 μ V/ $^{\circ}$ C (B version) or 10 μ V/ $^{\circ}$ C (C version). Bias current 30 pA (A) or 20 pA (B and C). Operating temp -25 to $+85^{\circ}$ C. $1.125 \times 1.125 \times 0.5$ in. \$37 (152A in 1-9), \$44 (152B in 1-9) or \$50 (152C in 1-9). Stock. DYNAMIC MEASUREMENTS. **219**

Instrumentation amplifier, FA601, with input impedance of $10^{11}\Omega$. Gains from 1 to 1000 programmable with single resistor. Input current 100 pA. Unity-gain bandwidth 1 MHz. CMRR 86 dB. Operates from ± 15 to ± 18 -V power supplies. Encapsulated module $2 \times 2 \times 0.625$ in. \$65 (1-9). INTRONICS. **220**

Low-cost FET amplifier, A104A, for general-purpose wideband applications. Small-signal bandwidth 10 MHz. Slew rate 25 V/ μ s. Settling time 1 μ s to within 0.01%. Voltage drift 50 μ V/ $^{\circ}$



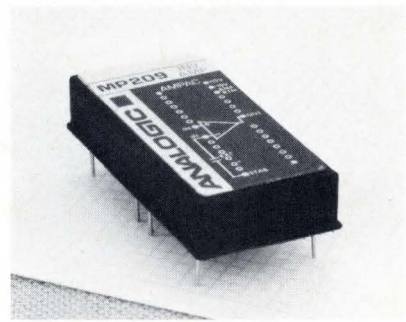
C. Input bias current 20 pA. Input impedance $10^{11}\Omega$. Open-loop gain 80 dB. $1\frac{1}{8} \times 1\frac{1}{8} \times 0.43$ in. \$29 (small qty). 2 wks. MONITOR SYSTEMS. **221**

Low-cost FET op amp, 1894, with CMRR of 50,000 over an input range of ± 10 V. Output ± 10 V at 5 mA. Full-power response 200 kHz. Unity-gain bandwidth 10 MHz. $1\frac{1}{8} \times 1\frac{1}{8} \times 0.5$ in. \$20 (production qty). MELCOR. **222**

Inexpensive FET op amp, P201C, with input impedance of $10^{12}\Omega$ and bias cur-

rent of 5 pA. Voltage gain 50,000. Voltage drift 35 μ V/ $^{\circ}$ C. Output ± 11 V at 5.5 mA $1.12 \times 1.12 \times 0.45$. \$10 (1-9). POLYTRON DEVICES. **223**

High-speed inverting amplifier, MP209 for critical current-summing applications. Slew rate 100 V/ μ s. Settling



time 1 μ s to within 0.01%. Small signal response 1.5 MHz. Open-loop gain 10^6 . Voltage drift 15 μ V/ $^{\circ}$ C. Input impedance 300 k Ω . Input bias current 1 μ A. Voltage noise 300 μ V rms. Output ± 10 V at 20 mA. Short-circuit-proof to ground. Electrically and mechanically shielded. PC-board or DIP-socket mounting $2 \times 1 \times 0.39$ in. \$56 (unit qty). 2 to 4 wks. ANALOGIC. **224**

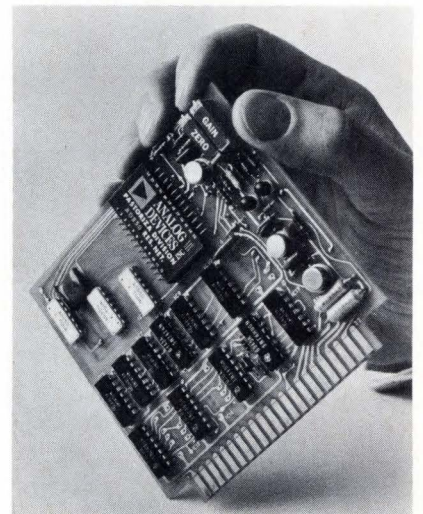
Isolated amplifier, 6119 Isoamp, for medical instrumentation and other applications that need isolated inputs. Isolation 1500 V, pk-pk or dc. Frequency response 15 Hz to 2 MHz. Isolation achieved by fiber-optic coupling of light diodes. Linearity $\pm 5\%$. CMRR 160 dB at 200 Hz and 80 dB at 2 MHz. Rise time 150 ns. Accepts inputs of up to 10 mV rms into 1 M Ω . Delivers up to 0.5 V pk-pk in 50 Ω . Compact lightweight case. \$500. Optional power supply \$78. DEVELCO. **225**

Low-cost analog multiplier, 426A, factory-trimmed for 1% accuracy. Needs no external trimming pots. Transconductance-type circuit. Can be connected as multiplier or divider. Customer can trim accuracy to 0.6% if required. Small-signal bandwidth 400 kHz. Phase shift 1° at 400 kHz. Output drift 2 mV/ $^{\circ}$ C. Linearity 0.6% (X channel) and 0.3% (Y channel). Encapsulated module. \$45 (unit qty). Stock. ANALOG DEVICES. **226**

Hybrid IC A/D converter, 871, compatible with MOS systems. Accuracy $\pm 0.05\%$ over the temperature range -20 to $+85^{\circ}$ C. "Successive-approximation" circuit. Consists of type 3751, thick-film ladder, bipolar IC comparator, bipolar-to-MOS translator, and MOS type-D flip-flop. Digital inputs permit external control of output word length (8, 9, 10 or 12 binary bits), and determine operating format. Power consumption 950 mW. Hermetically-sealed metal package. Also available with accuracy of $\pm 0.025\%$ or $\pm 0.1\%$. \$225 ($\pm 0.05\%$ version in 1-9). BECKMAN. **227**

12-bit A/D converter card, ADC-120, using company's own monolithic quad

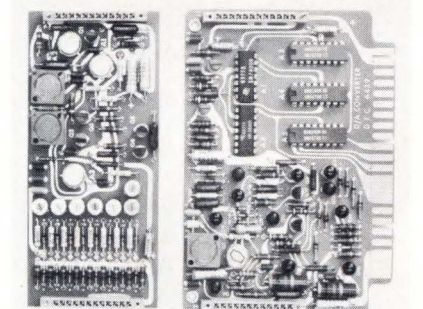
switches to form complete "successive-approximation" circuit. Tempco ± 5 ppm/ $^{\circ}$ C over temperature range -50 to $+100^{\circ}$ C. 12-bit monotonicity maintained over wide range of temperature. Includes TTL logic ICs, input buffer amplifier, comparator and high-gain reference amplifier. PC board, $3.75 \times 4.5 \times 0.412$ in., with 44-pin



dual edge connector. Relative error 0.125% (including buffer and comparator errors). Conversion time 20 μ s. Differential linearity $\pm \frac{1}{2}$ LSB. Diff linearity drift ± 3 pm/ $^{\circ}$ C. Input impedance 100 M Ω . Choice of input ranges and output codes. \$305 (1-9). Stock. ANALOG DEVICES. **228**

Low-cost 8-bit DAC, MP1808, with output slew rate of 10 V/ μ s. Includes thin-film resistor network, precision reference element and output amplifier. Conversion accuracy $\pm 0.1\%$ of F.S. at 23° C. Range tempco 100 ppm/ $^{\circ}$ C. Operating temperature 0 to $+70^{\circ}$ C. Mechanically and electrically shielded. Unipolar or bipolar output. Choice of input codes. Also available for 2-digit BCD. Field-repairable module, $2 \times 2 \times 0.39$ in. \$59 (1-9). 2-3 wks. ANALOGIC. **229**

9-bit D/A converter, 6439, for "glitch-free" operation at speeds to 1 million conversions/sec Typical settling time 500 ns. Unique "capacitance decoupler"



circuit. Packaged on double PC board with single-edge 44-pin connector. $4.5 \times 3.33 \times 0.75$ in. One board contains amplifier and sample/hold; other contains converter. Full-scale output

(Continued on page 62)

New IC's from Burr-Brown



a new monolithic op amp

with low bias current (15 nA), low drift ($5 \mu\text{V}/^\circ\text{C}$), low noise ($0.8 \mu\text{V}$, p-p), and wide supply range (± 3 to ± 20 Vdc).



two new hybrid multipliers

with $\pm 0.5\%$ linearity. No external components required. Miniature hermetically sealed package. Temperature range -55 to $+125^\circ\text{C}$.

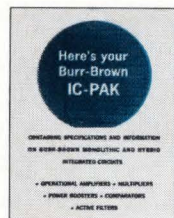


a new hybrid FET op amp

with ultra-low bias current (5 pA), low drift ($5 \mu\text{V}/^\circ\text{C}$), and fast slew rate ($6\text{V}/\mu\text{sec}$). Hermetically sealed TO-8 package.

...and you didn't think we made IC's!

These four new units join a rapidly growing family of Burr-Brown IC products. All have the high quality you've come to expect from Burr-Brown, quality that's assured in every processing step. In addition to the above, we have a POWER BOOSTER (± 10 V @ ± 100 mA) for use with any IC op amp, another series of HYBRID FET OP AMPS, and a series of low bias BIPOLAR OP AMPS . . . all in dual-in-line packages. We are also supplying HYBRID COMPARATORS and ACTIVE FILTERS.



Better get your Burr-Brown IC-PAK. For your copy of the Burr-Brown IC-PAK, containing complete information on all of our IC products, simply use this publication's reader service card or phone us.

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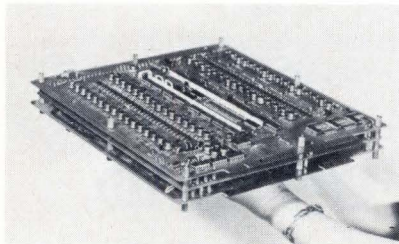


± 10 V into 2 k Ω . Accuracy $\pm 0.2\%$ $\pm \frac{1}{2}$ LSB. Tempco ± 50 ppm/ $^{\circ}\text{C}$. TTL input logic. \$350. 6-8 wks. DATA TECHNOLOGY. **230**

Level-converter cards, MLC5, MLC6, MLC7 and MLC8, to convert EIA logic levels to DTL/TTL or vice versa. MLC5 and 6 have 8 and 16 circuits, respectively, and convert from EIA to DTL/TTL. MLC7 and 8 also have 8 and 16 circuits and convert from DTL/TTL to EIA. Compatible with other Raytheon logic cards. 3×3.65 in. \$135 (MLC5), \$250 (MLC6), \$105 (MLC7) and \$198 (MLC8). 30 days. RAYTHEON COMPUTER. **231**

Automatic telephone dialer, ATD811, to dial up to 8 pre-determined telephone numbers consisting of up to 11 digits each. Completely electronic, with entire circuit on single plug-in PC board, $4\frac{1}{2} \times 5\frac{1}{2}$ in. If circuit cannot reach desired number, it "hangs up and dials again." Circuit uses ICs and discrete components. For use with remote computer terminals and other data acquisition systems. From \$120. Stock. NATIONAL MIDCO. **232**

Low-cost core memory, COMRAC 90, with full cycle time of 900 ns, including read/restore and clear/write modes. Buffer cycle time 600 ns including buffer read and buffer write. Split-cycle time $1.05 \mu\text{s}$ (read/modify/write). Basic memory capacity up to $8 \text{ k} \times 9$ bits or $4 \text{ k} \times 8$ bits. Field expandable to $32 \text{ k} \times 18$ bits. Basic system consists of three PC boards connected as single-plug assembly.



Overall dimensions $11 \times 12 \times 2$ in. \$1800 ($4 \text{ k} \times 18$ bit stack in qty of 100). Stock. INFORMATION CONTROL. **233**

Linearity-corrector circuit, LC123, to linearized deflection distortion (pincushioning) on CRT. Consists of three plug-in PC cards, for X-axis, Y-axis and off-axis signals. Linearity 0.1% for on-axis correction and 0.2% over useful screen diameter. Compatible with all CELCO deflection amplifiers and sweep generators. 30 days. CELCO. **234**

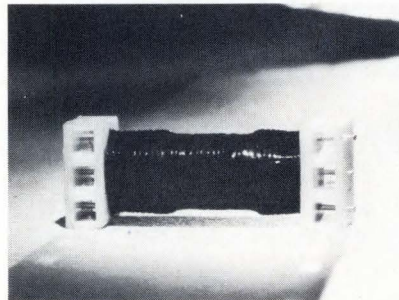
Compact VCXO, Series 190, to provide frequencies between 1 MHz and 200 MHz as specified by customer. Frequency tolerance $\pm 1 \times 10^{-6}$ over temperature range of 0 to $+60^{\circ}\text{C}$. Choice of output voltages and waveforms available, including compatibility with various types of IC logic. Typical performance available includes frequency deviation of $\pm 0.02\%$

with linearity of 15%. $2 \times 2 \times 4\frac{1}{2}$ in. Choice of header configurations. \$325 to \$575 depending on freq. 6 wks. ACCUTRONICS. **235**

Microelectronic log i-f amplifier, 58-588, to provide linear-to-log conversion over 60 dB signal range at 4.5 MHz with sensitivity of -80 dBm. Compact thick-film hybrid circuit on two-level ceramic substrate using multilayer printing techniques. Includes i-f coils. Hermetically sealed in shielded case $1.4 \times 1.9 \times 0.4$ in. Meets Mil-Std-883 specs. Needs +12 V and ± 5 V supplies. 50- Ω and 500- Ω outputs. Gain and log characteristics stable over temp range of -55 to $+100^{\circ}\text{C}$. One of series of hybrid IC components. HALLICRAFTERS. **236**

Switches & Relays

Plug-in reed relay with removable end cap to permit easy replacement of reed



capsule. Dry reed or mercury-wetted reed. DOUGLAS RANDALL. **238**

High speed, low-noise Hg-wetted-contact relay, HGJ, with 250-Hz rep rate. Noise slashed from usual $100 \mu\text{V}$ to $10 \mu\text{V}$ at 4 ms after coil energization, $1 \mu\text{V}$ typ at 5 ms. 10^{10} operations, with loads from picoamps to 2 A, 500 V. 750- μs response. 15 to 25-m Ω initial contact resistance, constant within 2 m Ω . CLARE. **237**

Logic-compatible reed relays with 14-pin DIP lead frames. RR-105 with internal transistor for drive from low-current source. RR-115 with internal current-sinking transistor forming one DTL/TTL unit load. Form A contacts to carry 1 A, break $\frac{1}{2}$ A. \$10 (prototype quantities). ASTRO-SPACE. **239**

Time-delay relay, ET553, with isolated form C contacts for ac or dc loads. Solid-state timing for delay-on-make or interval timing. Timing dial can be remote from relay contacts, connected by two wires. Pot allows customer calibration of pointer settings to 2% repeat acc. GE. **240**

Hydraulic-magnetic circuit breakers, AM1,2,3 for 1,2,3-pole switching of loads from under 1 A to 50 A at 65 Vdc or 250 Vac. UL recognized to 65 Vdc and 240 Vac. Many options. HEINEMANN. **241**

Pushbutton rotaries, 2900, with window

readout of switch position. Replaceable pushbutton caps in six colors. 8,



10, 12 positions in all standard codes. Make/break $\frac{1}{8}$ A, carry 3A. 3-m Ω initial contact resistance. Under \$4. JANCO. **242**

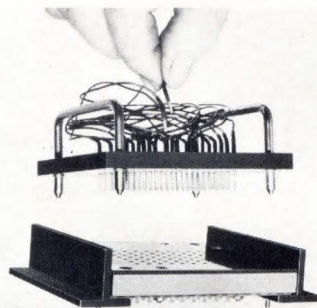
Lighted pushbutton, OA, combining snap and slide action. Actuator lifts moving contacts through air gap to mate with stationary contacts with sliding action. Said to eliminate migration, pitting, burning, contamination. To 6pdt. Turret or pin terminations. Momentary silent, momentary detent, push-lock/push-release, alternate. SWITCHCRAFT. **243**

Lighted pushbuttons, 1820, in any color or color combination for button, housing and nylon bezel. (Metal bezels in



chrome, black oxide, or brass-plated steel.) Spst or spdt. 2 to 9 A at 125/250 Vac. Diffusing screen. Integral (non-replaceable) neon or incandescent lamp. MOLEX. **244**

Pluggable program patchboard for 7×10 -terminal matrix. Teflon-insulated



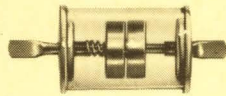
jumpers. Silver-plated contacts. Husky guide pins. SEAELECTRO. **247**

Keyboard pushbutton reed switches in add-on modules. Any number can be

(Continued on page 64)

"ZERO" Reaction Time

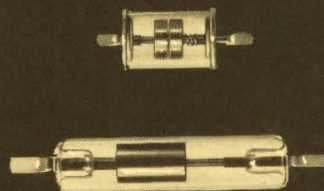
clip transients...



with the New Uni-Imp Voltage Surge Protector

- Impulse Ratio 1.1 to 1
- Trip Voltages 550V to 15kV
(constant up to 50 kV/microsec.)
- Life greater than 5,000 shots
@ max. rating
- Follow-on Current Compatible with normal
relay closure times

Now it is possible to protect sensitive components, even semi-conductor equipment, against voltage transients without concern for the rate of voltage rise. The "zero" reaction time of Signalite's new Uni-Imp is only one of its many unique features. Others including its Bi-Polarity, immunity to di/dt restrictions, infinite leakage resistance, are described in a new data sheet.



**AVAILABLE UPON
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Data Sheet ... on
Signalite's Uni-Imp
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Voltage Surge Pro-
tectors.

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(201) 775-2490

Circle 159 on Inquiry Card

stacked, 2.8 to 3.5/oz operating force, 0.2-in. full travel, 100 mA at 48 V. ALCO. **245**

Submin toggle switch with elongated toggle for advantages in recessed panels and dense switch arrays 1,2,3,4 pole. C&K. **246**

Packaging/Hardware

IC-packaging receptacle for mounting on PC laminate, allowing virtually any grid pattern. Accepts variety of IC-package types with round or rectangular leads. Anti-overstress feature assures proper insertion/withdrawal forces. Machine-installed receptacles compatible with all soldering techniques, and hand or machine wiring. AMP. **248**

DIP breadboard, 11-DE-1-S, to accept 12 DIPs plus discrete components. Layout includes two power-supply lines near each DIP location. 4.375 × 4.2-in. card takes 44-pin edge connector. \$19.50. DOUGLAS **249**

Burn-in socket modules to take 300°C. LMC 2696 for 3,4,6,8-lead TO-5s and TO-18s. LMC 2647, in building-block form, for DIPs, quad forms, spider packs and various MSI/LSI packages. LORANGER. **250**

Two-piece and card-edge PC connectors on OPL for Mil applications. Two-piece types with 17,23,29,35,41 contacts on 100-mil centers or 12,15, 18,22,26 contacts on 200 mils. 10-A, 6-mΩ contacts. Card-edge types with 15/30, 18/36, 22/44 single/dual contacts on 156-mil centers. 5-A, 6-mΩ contacts. ELCO. **251**

Right-angle rf coax connector with 360° swivel about cable axis for no strain on cable braid or center conductor. Sealed against moisture contamination. ITT GREMAR. **252**

Rf coax connectors, JCM, in seven types for PC or cable mounting. For use to 3 GHz. Interchangeable with and mateable with SMA types at much lower prices. E. F. JOHNSON. **253**

High-density circulars, Marc 63, with bayonet coupling, same insert patterns and layouts used in company's Marc 43,53,53RMD. Three configurations, four shell sizes. MICRODOT. **254**

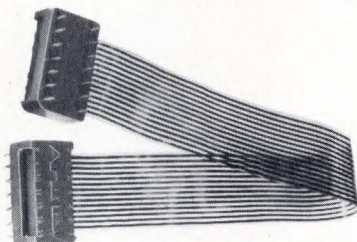
High-thermal-conductivity adhesive, Abletherm 12-1, of repairable silicone. Handy for bonds to heat sinks. 8 times thermal conductivity of unfilled silicone. Withstands continuous 400°F. IR 10¹⁴Ω-cm at 77°F. Easily cut with sharp blade. ABLESTIK. **256**

Light-insensitive substrates, AlSiMag 782, of opaque black alumina. Helium leak rate 10⁻⁸ cc/s at one atmosphere.

Can be reheated in oxygen atmosphere without color change. AMERICAN LAVA. **257**

Tape-controlled laser trimmer for 3000 thin- or thick-film resistors per hour. Resistor values trimmed to 0.5% for thick films, 0.1% for thin films in closed-loop system with 24 probes and vacuum chuck. X-Y table with 10 × 10-in. or 10 × 20-in. travel at 400 in./min. \$40,000-\$45,000. HUGHES. **258**

Flat cable jumpers with 14-pin DIP plugs. Any-length cable with dielectric



of vinyl, polyester, Teflon, Kapton. Gold over nickel over brass pins. ANSLEY. **255**

Computer-controlled laser trimmer, W102, for 3000 substrates per hour, each with 8 thick-film resistors. Based on J259 IC-test system, this system can be programmed for trimming, testing, constant-value monitoring, process analysis. Can include seven multiplex stations, with trimming at four. From \$77,900. TERADYNE. **259**

Numerically controlled insertion/termination system for low-volume component insertion on PCs and semi-automatic back-plane wire termination. Machine uses two heads with many options available on each. UNIVERSAL INSTRUMENTS. **260**

Cable binder, 14-090A, for tying wire bundles up to 1-in. diameter. Hand-held, pneumatically operated tool wraps, tensions, locks, cuts off tape with one trigger squeeze. Complete cycle in about one second. GARDNER-DENVER. **261**

Power Supplies

Constant-current module, 925, with output impedance greater than 100 MΩ at 10 mA. Output current 10 to 50 mA with a regulation of 0.001% on current and 0.001% voltage supply isolation at 10 mA. Up to 500 mA rating available. Tempco 0.01%/°C. Weighs 2 oz and is 1.5 × 1.5 × 7 in. \$78. CALIFORNIA ELECTRONIC. **262**

High-voltage supply, 23566, with 5-regulated outputs and a 6.3 Vac filament supply. Short-ckt protection for

dc outputs. Input: 115 Vac ±5% at 400 Hz ±5%. Outputs: 2500 Vdc at 0.8 mA, -65 Vdc at 1 mA, +315 Vdc at 1 mA, +160 Vdc at 30 mA, -60 Vdc at 30 mA and 6.3 Vac at 0.6 A. Regulation ±1% full load to no load plus line. Ripple 0.1% rms. Tempco 0.02%/°C. GLENTRONICS. **263**

Precision high-voltage supplies 180 and 190, for cathode-ray tubes and as laboratory standards. V adjustable from 1 kV to 20 kV at 3 mA on model 180, and 10 kV to 30 kV at 1 mA on model 190. Output V is within



0.25% of settings. Output V is line and load regulated to 20 ppm and 25 ppm respectively. Switchable-output polarity. Overload and short-ckt protection. \$1895 (model 180) and \$2295 (model 190). VELONEX. **264**

IC power-supply module, MIC5-7A, with 5 Vdc at 7 A. V out adjustable from 4.75 to 5.25 Vdc. Operates from 105-125 Vac, 60 to 400 Hz. Line and load reg ±25 mV. Ripple and noise 10 mV rms. Tempco 2.5 mV/°C. Operating range -20 to +50°C. Measures 5 × 6 × 6 in. Short ckt-proof std and over voltage protection optional. Guaranteed for 10 years. \$52. ARMOUR ELECTRONICS. **265**

Test Equipment

Magnitude, quadrature and in-phase detector, 1238, for extracting small signals from noise. 130-dB gain and



100-nV full scale sensitivity. 1-GΩ input Z. Protection against 200-V signals. Flat or tuned freq response from 10 Hz to 100 kHz. \$1300. GR. **266**

Logic probe, 30, with input-overload protection to +200 V continuous and -200 V for 3 seconds. Displays logic 1 and 0 conditions with lamp at probe end. Identifies single pulses as narrow as 30 ms. Also detects prfs up to 30-pps symmetrical or non-symmetrical wave forms. \$30. AUTOMATED CONTROL TECH. **267**

(Continued on page 66)

When the lights go out, the only really portable Digital Multimeter goes on



...and on.

Run the Fluke 8100A 0.02% digital multimeter anywhere, anytime up to 8 full hours off the rechargeable battery pack. Printer output now available.

There are twenty or thirty digital multimeters around that lay claim to portability. The only one you can move around easily and use without a nearby wall plug is ours. It's the only portable machine that works where you need a portable machine.

True portability is just part of the story. The Fluke 8100A, with an accuracy of 0.02% and a selling price of \$795, with rechargeable battery option, gives you nine times the accuracy of three digit instruments for half the price of comparable four digit multimeters. We've used a new A to D technique to give you an instrument with low power drain for eight-hour continuous battery operation without recharging. (line operation only \$695)

The Fluke 8100A measures ac and dc volts in four ranges to 1200 volts and ohms in five ranges to twelve megohms. Readout is four full digits plus "1" for 20% overranging. Features include an active 2-pole switchable filter and automatic polarity indicator. All functions are push-button selectable.

Also available are RF and high voltage probes, switched ac-dc current shunts, a ruggedized case, and data output (line operation only).

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268

8-channel high speed waveshape controller, FC-200, for digital signals at rates from single shot to 100 MHz. Width, delay, amplitude and offset controlled by front panel switches for each channel. Pulse width 4 ns to 10 ms. Complementary outputs give 100%-duty cycle. Delay fixed at zero or variable 0-10 ms in 6 ranges. Amplitude controlled by 8 attenuators covering a 10-dB range. Offset ± 3 V into 50 Ω . Rise and fall times 1.2 and 1.8 ns respectively. TAU-TRON

269

Low-cost pulse generator, PG-1, for research and educational applications. Compatible with RTL, DTL and TTL ICs. Freq 1 Hz to 1 MHz and pulse width 100 ns to 100 ms. Z_o 50 Ω . Rise and fall times 20 ns. Shock-proof steel case 4 \times 7-1/2 \times 6-1/2 in. Weight 4 lbs. \$150. EL INSTRUMENTS.

270

Differential thermometer, Delta-T 102 and 103, for measuring the difference between transistors and heat sinks. 3 ranges: 0 to $\pm 20^\circ\text{C}$, 0 to $\pm 50^\circ\text{C}$, and 0 to $\pm 100^\circ\text{C}$. 3 modes: probe A, probe B and A-B. Circuit acc 0.1°C and meter acc 2%. All probes linear



allowing auxiliary readout. Model 102 powered by self-contained battery pack and 103 by 117 V, 50 to 60 Hz. \$159 (102) and \$189 (103). TC PRODUCTS.

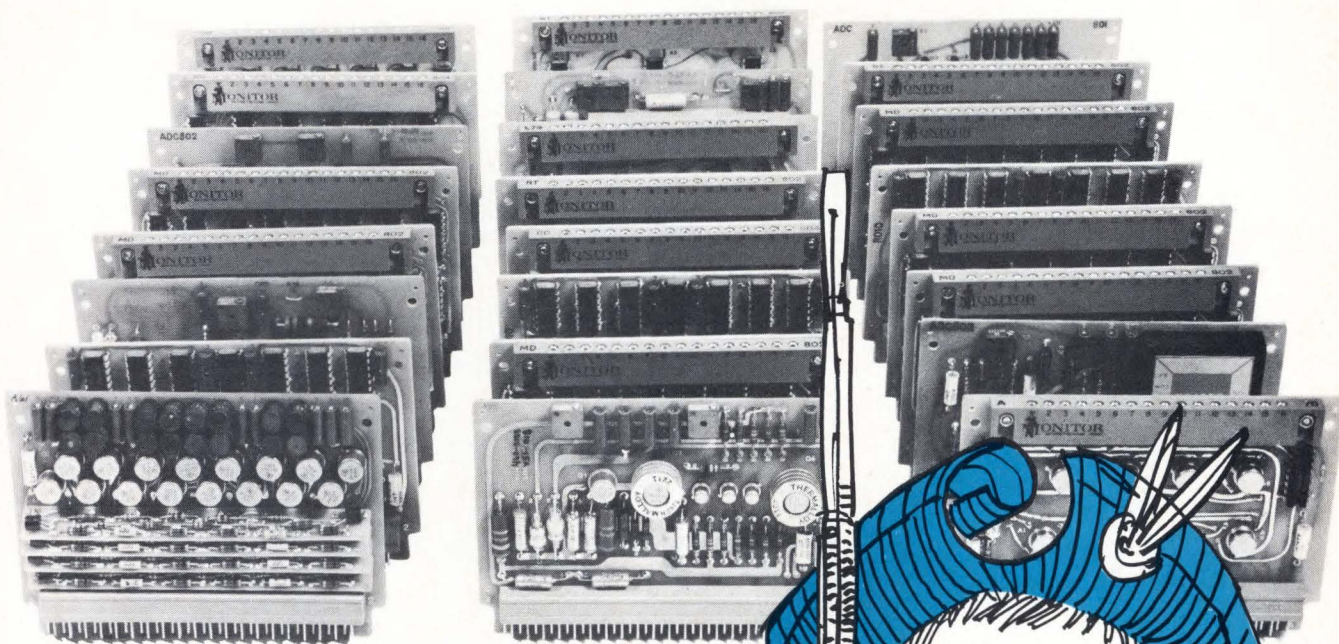
271

Integrating and Hall-effect gaussmeter, MF-1HR, for testing B-H or B-H vs H curves. Also used for general magnetic measurements. Fluxmeter range 100-99.9 $\times 10^4$ kilo Maxwell-turns, with a 1% accuracy. Drift rate ± 100 Maxwell-turns/min. Gaussmeter range 10-30,000 Gauss f.s. 115 V ac or battery powered. MSI Div, OS WALKER CO.

272

6-digit multimeter, 6853, with accuracy of 0.001%. Ranges: dc 100 mV to 1100 V, res 1 Ω f.s. to 100 M Ω f.s., ac 1 to 1000 V, ac/ac ratios and ac/ \pm dc ratios. Autodesense circuit provides hi-accuracy for noise-free sig-

(Continued on page 68)



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nals and optimum accuracy for noisy signals. Auto ranging, remote programming and out of-range indication standard. Input signal polarity detected automatically. All solid-state MOS FET circuitry used throughout instrument. \$4095 in single-lot quantities. CIMRON. **273**

Computing true rms DVM, 1860, for any combination of dc and ac, for periodic and random signals, for exponential and true-time averaging. Computes true rms, mean and mean-modulus values from dc to 10 kHz. True time averaging up to 3.4 hrs. Ext triggered time averaging. 100 mV to 300 V f.s. (100 μ V res). Acc $\pm 1\%$ of reading $\pm 0.3\%$ f.s. Zi 1 M Ω , \$3250. EMR. **274**

Low-cost active probe, 1124A, for hf oscilloscopes Converts 50 Ω input to 10 M Ω /10 pF Z at probe tip. Allows hf scopes to use 50- Ω input at hf but gives higher Z_{in} at lf. 2 switch-selected V ranges: ± 10 V with an attenuation of 10 or ± 100 V with an attenuation of 100. Max input ± 350 V on 10-V range and ± 500 V on 100-V range. Second switch selects ac or dc coupling. Freq range to 100 MHz. Probe obtains power from front panel connector or from optional p.s. \$95. HP. **275**

Display Devices

16-segment incandescent readout, TDS-514, for applications requiring a display of the complete alphabet plus numerals. Character size 0.40 high \times 0.40 wide. 500-ft Lamberts at 5 Vdc. Lamps replace from front. Single plane operation-viewing angle, 150°. Decoder-driver pc board optional. OPPENHEIMER. **295**

Incandescent digital read-out, DROD, with seven-bar readout uses fiber optics. 1/2 high \times 0.43 wide \times 1 inch-long. Character size 0.4 high \times 1/4 in. wide. Disposable 7-lamp module at rear of unit. Lamps selected for long life. RANK PRECISION INDUSTRIES. **296**

Field-resettable elapsed-time indicator, CP3, with a mercury coulometer, in which a visible gap travels along a mercury-filled tub according to the total flow of electric current through the instrument. Operates on ac or dc V or pulses. Current drain (dc) less than 3 μ A for 1000 hrs. 1 7/8 \times 3/8 \times 3/8 in. Adhesive mounting. \$4. CURTIS INST. **297**

Indicator light sampler kit, with 13 different indicator lights plus bulbs. Lamps include: low V incandescents

in sizes T-1, T-1 3/4 and T-3 1/4, line voltage neon in T-2 and line voltage incandescent in T-4 1/2. GENERAL ILLUMINATION. **298**

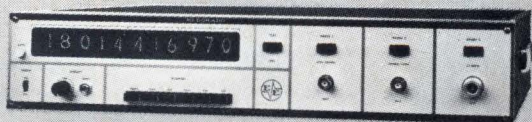
Digital-time display, for displaying time digitally in units of hours, minutes and seconds. Options: BCD output, memory, polarity, preset and relay output. 0.61 in. character height. 115 V, 50-60 Hz. Output BCD (1248) parallel, DTL compatible. Reset to zero via front-panel pushbutton. \$260. THETA. **299**

Digital temperature indicator, 1640-88-26, for 12 measurement channels. Measures temp 0 to +100°C with a resolution of 0.01°C and abs acc of 0.1°C (including error of sensor). Calibrated sensors and matching signal conditioner-linearizers provide this performance. 12-position switch selects channel. INSTRULAB. **300**

Taut-band miniature-edgewise meter, MCEIT, for more accurate readings and greater repeatability. 0.5 \times 1.75 in. Additional features: horizontal or vertical positioning, separate bezel and hardware for easy mounting, clear-plexiglas front covers and self-shielded core-magnet construction. Dc acc $\pm 2\%$ f.s. at 25° C and ac acc $\pm 3\%$ f.s. at 25°C. JEWELL. **301**

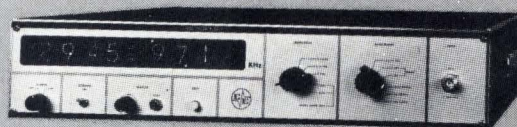
(Continued on page 70)

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SG301A	LM301A			SG300	LM300	SG1596	MC1596
SG101	LM101	SG1401	NEW SG design			SG1496	MC1496
SG201	LM201	SG2401	offering 20dB	SG105	LM105		
SG301	LM301	SG3401	gain at 100 MHz	SG205	LM205	SG1402	NEW SG design
				SG305	LM305	SG2402	w/var. gain and
						SG3402	> 50 MHz response
SG748	μ A748	COMPARATORS		SG723	μ A723		
SG748C	μ A748C	SG710/710A	μ A710	SG723C	μ A723C	SENSE AMPS	
SG741	μ A741	SG710B/710C	μ A710C	ARRAYS		SG7520	SN7520
SG741C	μ A741C	SG711/711A	μ A711			SG7521	SN7521
SG107	LM107	SG711B/711C	μ A711C	SG3821	CA3046	SG7522	SN7522
SG207	LM207			SG3822	CA3026	SG7523	SN7523
SG307	LM307			SG3823	CA3018	SG7524	SN7524
				SG3801	"QuikChip" —	SG7525	SN7525
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Data Handling

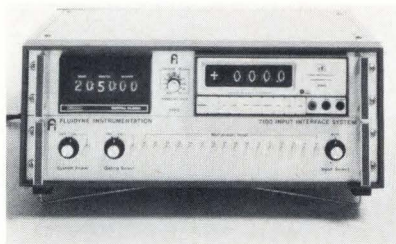
Price change

DATA GENERAL has reduced the price of the Supernova minicomputer. In a configuration with 4096 16-bit words of core memory, data channel and Teletype interface, the computer now costs \$9600 instead of \$11,700. Cost of the central processor alone is \$5600 instead of \$6850. **276**

Printing calculators, Series 100, for scientific or business applications. Available with either 6 or 14 special registers, thus providing up to 14 different calculators in single package. Claimed "first calculator in its price range to provide trig, degrees-to-radians and other functions at a single key stroke." Basic functions include X^2 , \sqrt{X} , π , $1/X$, e^x , $\log_e X$ and $[X]$. Uses TTL, DTL and MSI circuitry. MOS memory with capacity of 512 to 1024 bits. Capacity 12 digits plus sign and decimal print. Modularity allows user to buy basic machine and add extra features later. Programmable with 1 or 2 card readers, thus adding 60 to

120 program steps. Printing mechanism uses standard paper. From \$1495. 4 to 6 months. WANG. **277**

I/O interface units, 7000 series, to convert Wang 700 series electronic calculators to on-line data-acquisition and process-control systems. Compatible

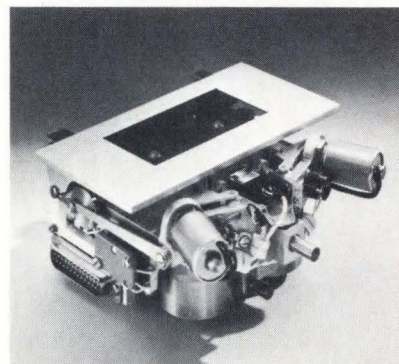


printers and incremental plotters available. Systems allow automatic measurement of both ac and dc voltage and resistance from any one of 16 random-access inputs with complete program control of measurement function, data storage and output-writer formatting. Cost claimed much lower than computer-based systems with similar performance. \$3950 (7100 interface with built-in DVM), \$3950 (7150 high-speed interface with 12-digit A/D converter) and \$1750 (7130 real-time clock interface). 60-90 days. FLUIDYNE. **278**

Computer terminal/typewriter, ADS-715, for use as data-communications terminal or as standard typewriter.

Built-in data set provides dial-up capability. All circuitry housed within case of standard 15-in. carriage typewriter. Portable. Choice of three code formats including ASCII at 110 bits/s and standard IBM codes at 135 bit/s. AMERICAN DATA SYSTEMS. **279**

Digital cassette recorder, Raycorder 6406-01, with interface circuitry for control from DTL/TTL logic. Circuitry contained on plug-in PC boards. Uses standard or improved Philips-type cassettes with clear leaders. Read/write speed maintained by



bi-directional motor drive. High-speed rewind in either direction. Data serial-phase encoded on input and output. $5.5 \times 5.6 \times 2.6$ in. RAYMOND ENGINEERING. **280**

(Continued on page 72)

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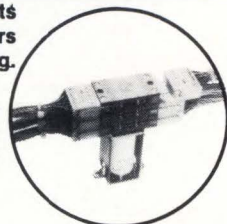
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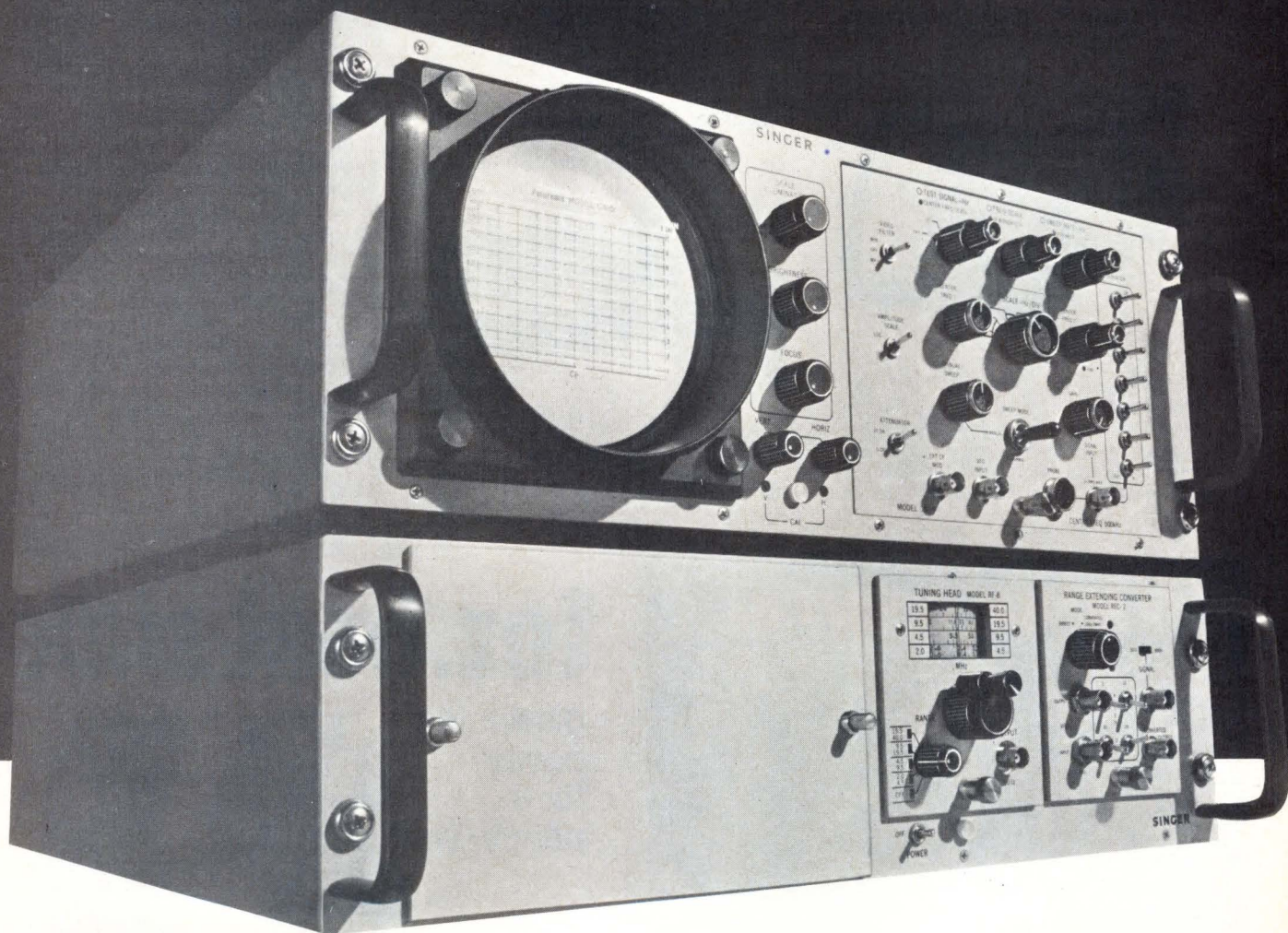
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Incremental cartridge recorder, IRC-1000, with simple bidirectional sprocket drive that eliminates slippage, cumulative error, homing inconsistencies and tape scuffing that can occur with pinch rollers. Rugged construction. Cost claimed competitive with paper-tape reader/perforators. Computer-grade cartridge holds 200 ft of 1.5 mil tape with width of 1/4 in. Tape contacts head during high-speed operation to allow automatic search. **MICRODYNE. 281**

Tape transport system, Computette 1210, using standard (4 × 2-1/2 ×



3/8 in.) cassette. Serial input and output. Read/write speed 5 in./s. Bidirectional read/write. Packing density variable to 1600 bits/in. Remote and manual control. Start/stop time 20 ms. Self-contained power supply. Built

around company's Model 1100 transport mechanism. \$980. 30 days. **COM-PUCORD. 282**

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High-speed A/D converter, Spectro-Logic S-1401, for use with Varian 620/i minicomputer. Internal sample/



hold module. Synchronous operation or conversion initiated by computer command. Resolution 8 or 13 bits

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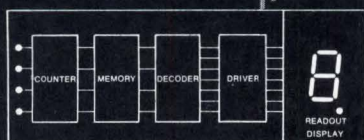
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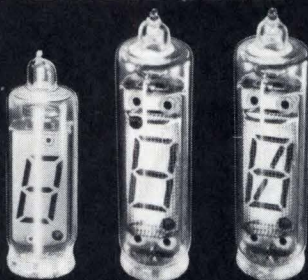
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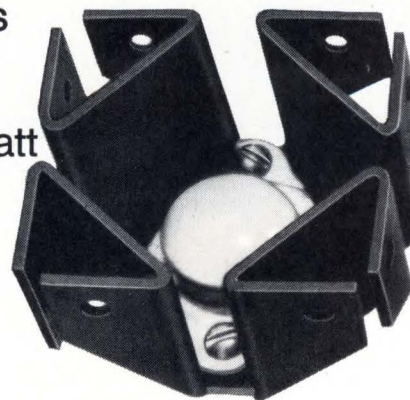
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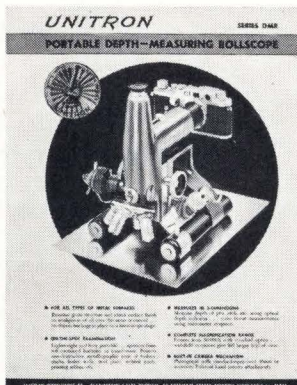
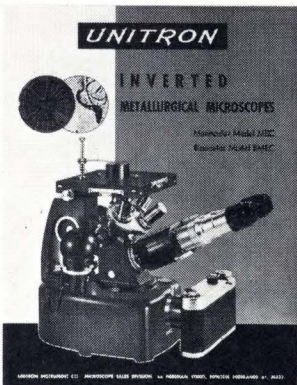
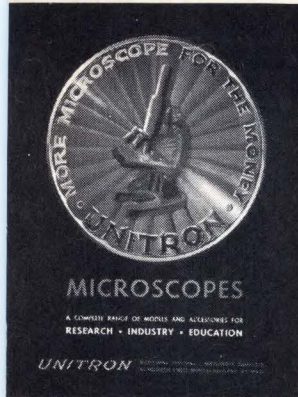
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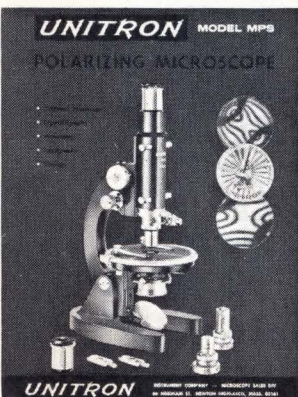
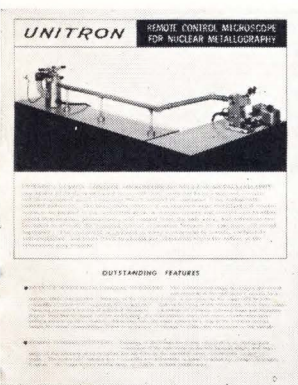
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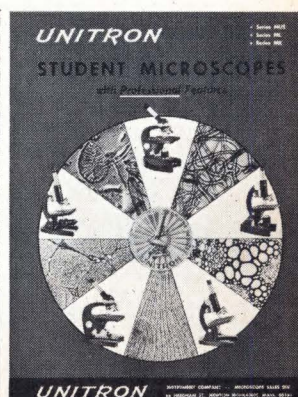
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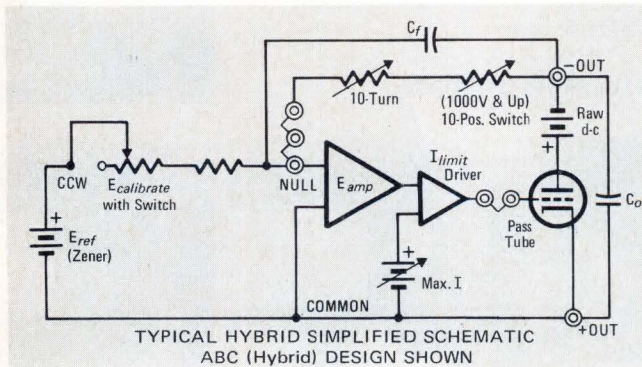
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Unusual Literature

Application Note on Fast-Settling Amplifiers

Michael S. Kennedy
DDC

Reading this, you can easily get the feeling you're reading one of *EEE's* "What's Wrong With . . ." articles. The style, a hard-hitting, no-holds-barred approach, is identical. Kennedy starts his app note quietly enough with a discussion of two of the three well-known types of amplifier damping — critical and underdamped.

Then he moves on to a more critical and more controversial question — how to measure settling time. He takes a stand firmly in favor of using a false summing junction for measurements. Then Kennedy really warms up.

Though he uses the "Specsmanship" headline for only one section, he whips out at misleading and "conveniently omitted" specs throughout the remainder of his paper. He shows, for example, the differ-

ences that can exist between actual voltages and settling times and those that might be measured. He discusses the influence of different types of scopes and different scale settings and makes strong comments like, "Don't be fooled by . . ."

When he covers the effects of stray capacitance, he's specific, providing a table showing the phase shift and amplitude error resulting from tiny capacitances (1pF and 5 pF) on resistances they shunt. He stresses the differences between ideal conditions and real ones where some amplifiers may be useless.

Kennedy occasionally drifts into a commercial for his company's products (the main departure from *EEE's* "What's Wrong With . . ." articles), but he's readily forgiven because of the great value in the information that can be used in selecting op amps from any vendor.

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Part 2 concentrates on methods of meeting specification requirements not readily achieved by standard circuits. In certain cases a simple modification to a standard circuit configuration is shown to be sufficient; in others a novel approach is given. Some of the standard circuits for which modified versions are provided include multivibrators, Schmitt triggers, and time interval circuits. Special designs included are meter-driving circuits and precise constant current sources. The well-written text is mostly non-mathematical and can be followed by anyone who has a basic knowledge of circuit design techniques.

Whether you're a practicing engineer ever alert to a source of new ideas, or an engineering support technician looking for an informative and definitive source of circuit design data, this book certainly belongs in your library. You'll find the text and illustrative material most informative, and the countless examples and problem solutions — worked out in minute detail — of enduring practical value. 224 pps., 114 illus. Hardbound.

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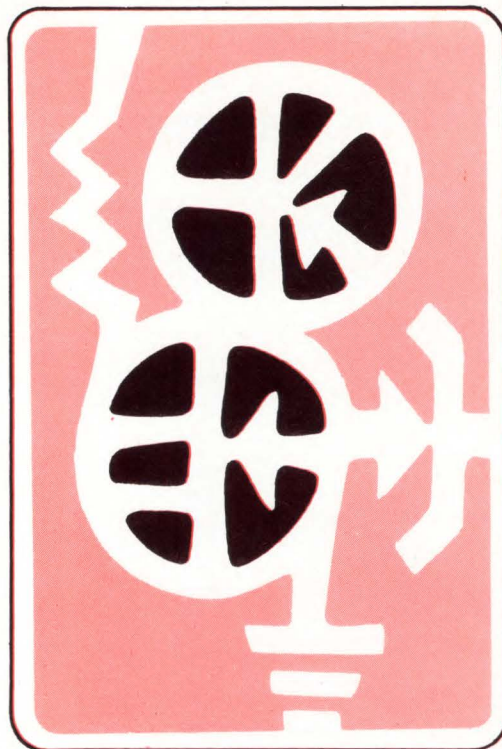
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EEE readers have voted Anthony C. Caggiano of Ridge, N.Y. winner of the \$100 Savings Bond for August. The winning circuit design is "Simple gyrator for L from C."

Step-servo motor slew generator

Circuit Design No. 600

by Charles R. Forbes

Univac

Salt Lake City, Utah

THE VARIABLE UJT oscillator shown in this schematic, operates a step-servo motor in either a slow or fast mode. The motor requires a pulse generator capable of providing a train of pulses at a slow rate, a fast (slew) rate and a variable rate providing a smooth transition between the two extremes. The smooth transition is required to prevent motor stall. This circuit meets all three requirements and has a transition time of 1.5 seconds. The input is compatible with standard-digital logic levels.

Q_1 and Q_2 are constant-current sources with Q_1 having twice the capacity of Q_2 . Q_3 , a JFET, acts as a voltage-controlled variable resistor in parallel with R_{10} . The FET's re-

sistance varies inversely with the charge on C_1 . R_{11} , R_9 , C_2 and the equivalent parallel resistance of Q_3 and R_{10} determine the repetition rate of UJT oscillator Q_4 .

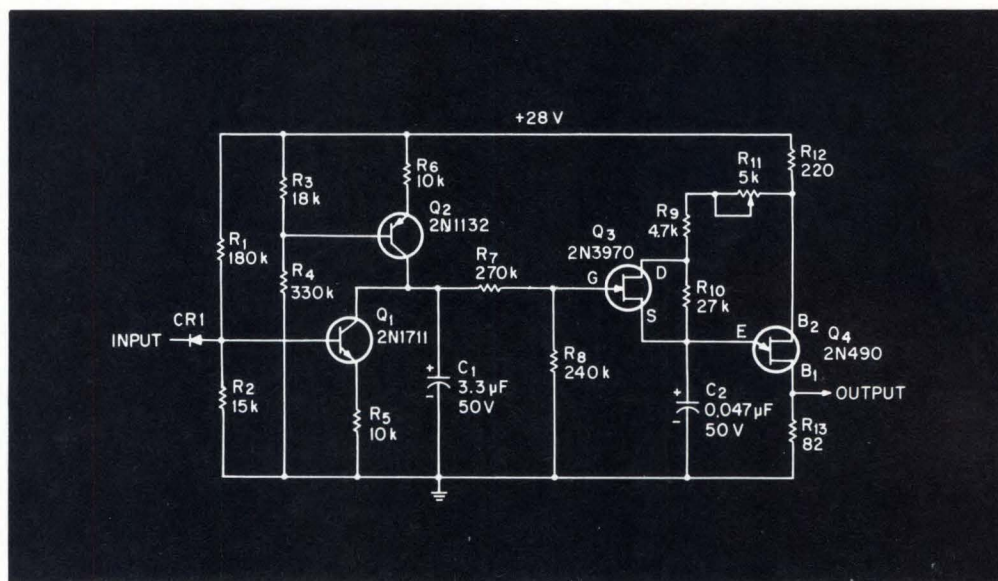
In the steady state condition

with a 1 at the input, Q_1 passes all the current generated by Q_2 , C_1 is discharged and Q_3 is off. These factors cause Q_4 to generate its low frequency pulse rate (1000 pps).

When the 1 at the input is

changed to 0, Q_1 cuts off. This causes Q_2 to charge C_1 at a uniform rate, which gradually reduces the source to drain resistance of Q_3 . This in turn increases the pulse rate of Q_4 .

With a steady state 0 at the



input, Q_1 is off and Q_2 maintains the charge on C_1 . Therefore, Q_3 is full on and oscillator Q_4 generates its highest rate (4400 pps).

When the "0" at the input is changed to a "1," Q_1 passes

all of Q_2 's current plus the discharge current of C_1 . C_1 discharges at a uniform rate thus increasing the equivalent resistance of Q_3 . This causes Q_4 to gradually decrease its pulse rate.

Modified 710 maintains accuracy at high input voltages

Circuit Design No. 601

by Leonard Accardi
Kollsman Instrument
Elmhurst, N.Y.

IT IS OFTEN NECESSARY to protect the inputs of comparators ($\mu A710$) against excessive voltage inputs. A typical application would be a zero-crossing detector placed at the output of an op amp with amplifier

output swinging ± 10 volts. The usual over-voltage protection circuit resembles the circuitry of Fig. 1. In this circuit, R_s is made relatively high to limit the drive current required of amplifier A_1 . This resistor reduces the accuracy of comparison by $I_{off} R_s$ where I_{off} is the offset current of the 710.

The circuit of Fig. 2 overcomes this problem. When V_{in} is more positive than V_{p1} (Pinch-off voltage of Q_1), Q_1

(Continued on page 78)

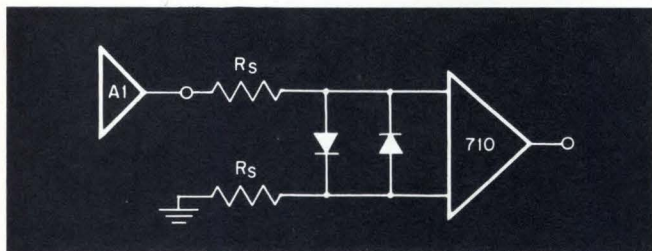


Fig. 1. Usual comparator protection circuit which introduces an error of $I_{off} R_s$.

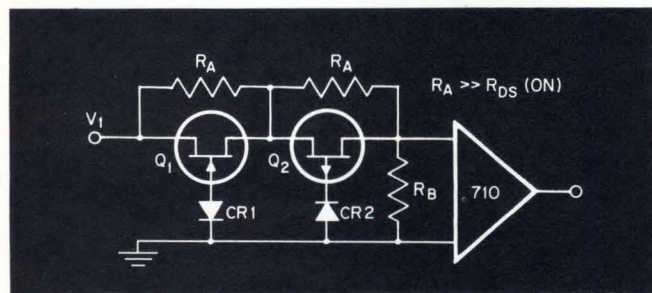


Fig. 2. New comparator protection circuit extends differential and input voltage ranges while maintaining accuracy.

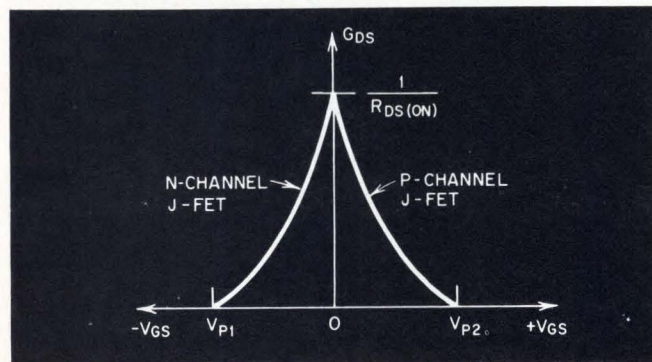


Fig. 3. Graph of FET conductance versus comparison points.

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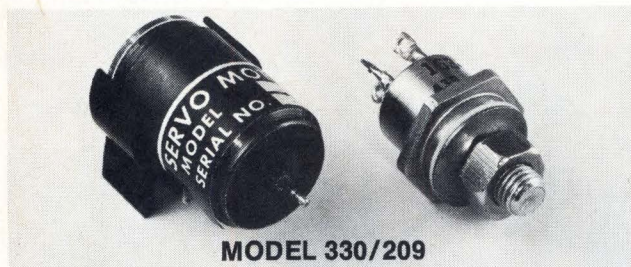
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is off and Q_2 is on since CR_2 is back biased. Thus the gate of Q_2 is allowed to float and assumes the same potential as the source with the result that Q_2 is on. When V_{in} is more negative than V_{p2} , Q_2 is off and Q_1 is on. In either case, the impedance seen by V_{in} is approximately $R_a + R_b$ and the input voltage of the comparator is $(V_{in})(R_b)/(r_a + r_b)$. The voltage and the pinch-off voltages should be chosen

to be less than the input and differential voltage ratings of the comparator (5 volts for the $\mu A710$).

Only when the difference between V_i and ground is less than the pinch-off voltages, do both FETs conduct resulting in a low impedance path to the 710's input. Maximum conductance (G_{ds} in Fig. 3) is obtained only near the comparison point where $V_{GS} = V_i - \text{ground} = 0$.

Simple one shot has complementary outputs

Circuit Design No. 602

by Gerald Lewis

Chief Engineer
 Transmagetics
 Farmingdale, N.Y.

THE CIRCUIT SHOWN in Fig. 1 is a one-shot multi that is capable of being pulse-width modulated. The circuit is actuated by a strobe input to G_1 which drives the output of G_1 to

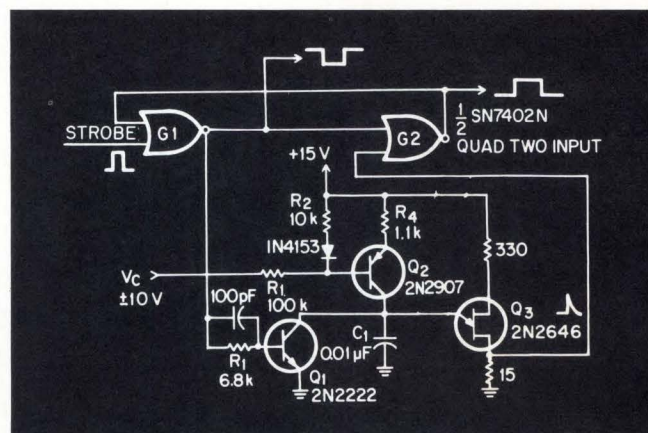


Fig. 1. This one shot is capable of being pulse-width modulated by V_c . It is capable of high duty cycles and can supply complementary outputs.

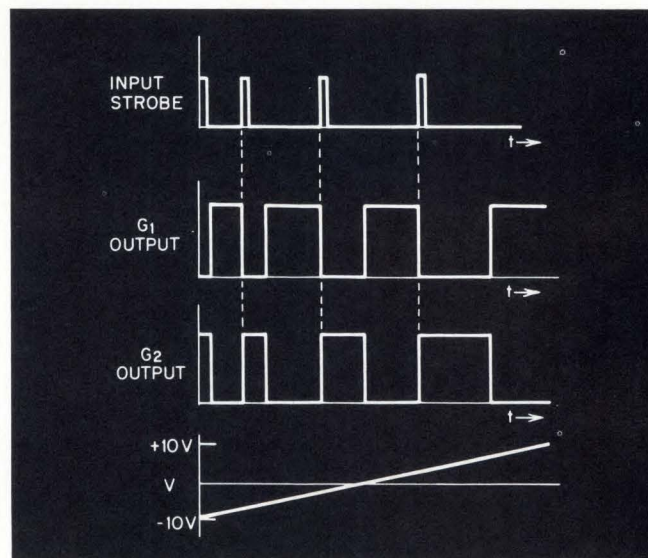


Fig. 2. Timing diagram of circuit operation. Note that the control voltage is bipolar.

binary 0. This level turns Q_1 off and allows the voltage across C_1 to build up according to $V_{C1} = it/C_1$. At a specified time, unijunction Q_3 will fire discharging C_1 . The output of the UJT drives the output of G_2 to binary 0. Fig. 2 is a timing diagram of circuit operation.

Q_2 is a linear current source to charge C_1 . Since Q_1 is normally on, the current of Q_2 is bypassed to ground thru Q_1 . V_C determines the amount of current delivered to C_1 . Linearity of 0.1% has been achieved with this circuit. Replacing

the current source with an op-amp single-ended current pump increases the linearity to 0.02%.

The duty cycle (not repetition rate) is determined by the speed of the logic used and the saturation storage time of Q_1 . Q_1 may be replaced by an hex inverter with an uncommitted collector (SN7405N-J) for increased speed. The control voltage V_C determines the amount of current to C_1 and therefore controls the output pulse width. The scale factor of supply voltage V_C is controlled by resistors R_3 and R_4 . ■

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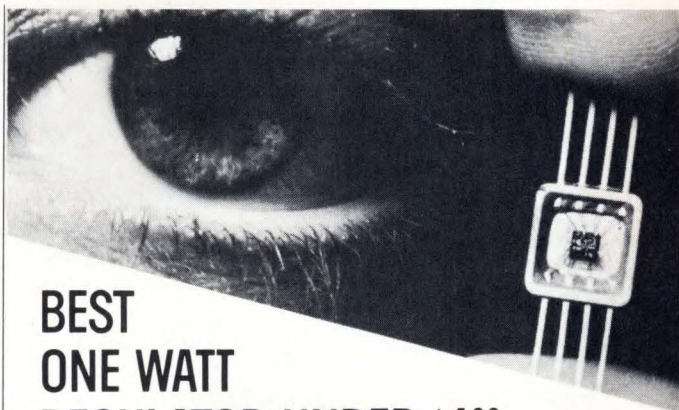
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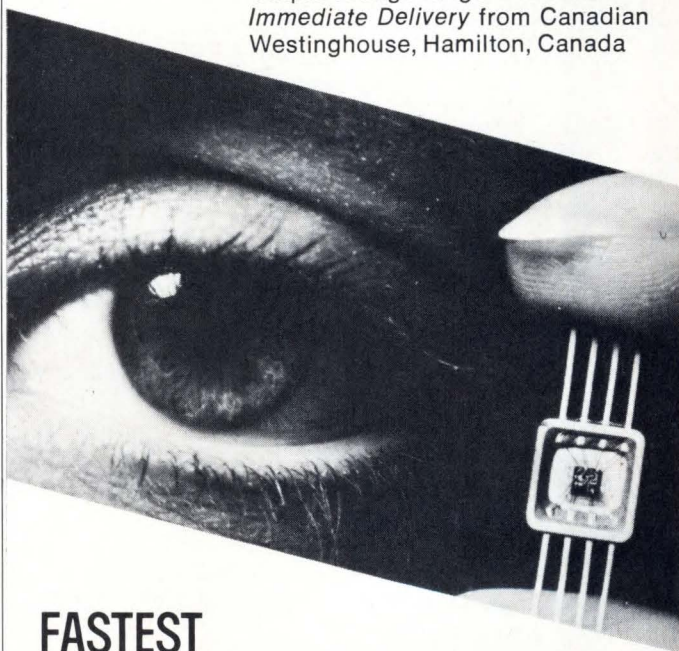


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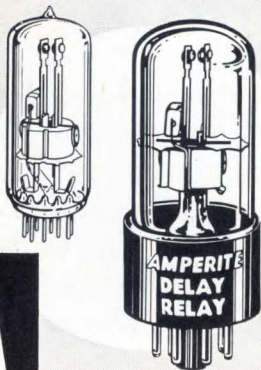
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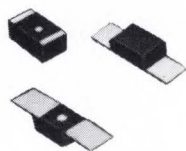
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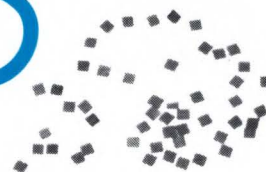
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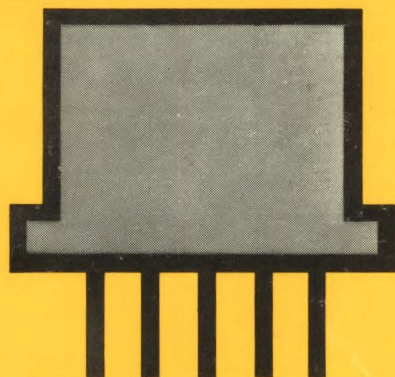
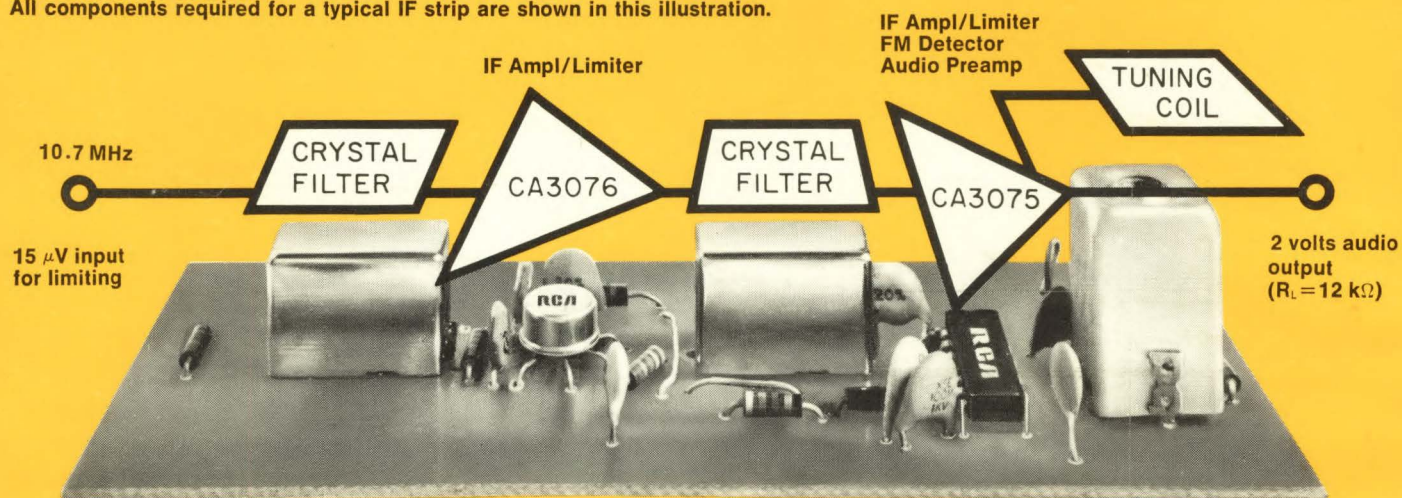
The CA3076 has an input limiting voltage (knee) of 50 μ V (typ.) and 80 dB (typ.) gain with 2-kilohm load at 10.7 MHz. It contains an integral voltage regulator, for operation at power supply voltages from 6 V to 15 V.

The CA3075 limits with an input voltage of 250 μ V (typ.) at 10.7 MHz. It has low harmonic distortion and excellent AM rejection—55 dB (typ.) at 10.7 MHz. Differential peak detection permits single-

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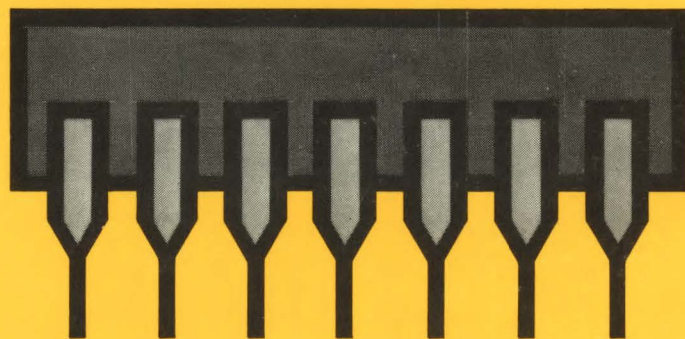
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All components required for a typical IF strip are shown in this illustration.



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Input limiting voltage: .. 50 μ V (typ.)
Freq. capability: Up to 20 MHz
Package: 8-lead TO-5
Price: \$1.60 (1000-unit level)



CA3075 IF ampl/limiter, peak detector, and audio preamp

Voltage gain (audio preamp): 21 dB (typ.)
Input limiting voltage: 250 μ V (typ.)
Freq. capability: Up to 20 MHz
Package: 14-lead DIP (formed leads)
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