



OSCILLOSCOPE SYSTEMS

What's new in HP Scopes? 18 GHz, dual-channel sampling! New, faster HP diodes now extend sampling capability through 18 GHz. For the first time, you can directly view and measure 18 GHz CW signals (or 20 psec risetime pulses).

But there are more new scope innovations from HP. There's the new, easy-to-use, 250 MHz real-time scope ... and new, direct read-out TDR with 1/4" resolution... and new variable persistence and storage scopes for measurements up to 100 MHz... and a whole new series of low-cost 500 kHz scopes.

AND, there are more eye-popping

scope ideas just around the corner!

Next time you see your HP field engineer, ask him what's new in scopes. You'll be surprised by all that's happening to give you better, more economical scope measurements. One thing, we bet you'll get a new (and better) answer, every time you ask!

Are you thinking about a new scope? Are you wondering whether you should continue down the same old road? Or is it time you took a look

at another manufacturer? The HP road means going with the demonstrated leader — maker of performance champs.

Call your HP field engineer, right now, if 18 GHz sampling is your interest. Complete 18 GHz sampling system available with delayed sweep, or w/o delayed sweep. If you already have an HP 12.4 GHz sampling system, add the new 18 GHz HP 1430B remote sampler. Write Hewlett-Packard, Palo Alto, California 94304. Europe: 1217 Meyrin-Geneva, Switzerland.

080/6







EXCLUSIVELY FOR DESIGN DECISIONS



Photo by Kemon Taschioglou Story on page 36

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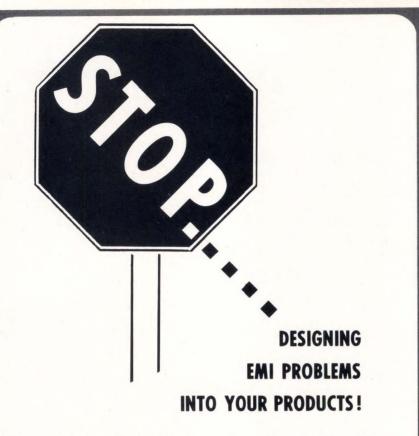
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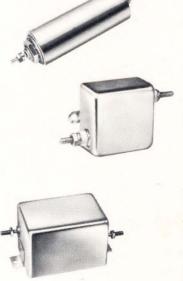


Electro-Magnetic interference problems can be eliminated by careful consideration to component design, layout and proper choice of filter networks. Standard Electronics devotes its entire facilities to electro-magnetic compatibility and susceptibility control. These services and products can be of assistance during your prototype design:

- PRODUCT TESTING
- SYSTEMS ANALYSIS
- ☐ FILTER ENGINEERING AND DESIGN
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STANDARD ELECTRONICS COMPANY DIVISION OF GULTON INDUSTRIES, INC.

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EXCLUSIVELY FOR DESIGN DECISIONS

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Editorial Objectives

EEE serves electronic design engineers exclusively. EEE restricts its editorial coverage to material that can help engineers make design decisions. Such editorial material is intended to help an engineer:

- Decide for one design technique or design
- philosophy over another;

 Decide for one measurement technique
- Decide for one packaging technique over another;
- Decide for one systems approach over
- Decide for one material, component, packaged circuit or instrument over another.

EEE does not publish general-interest material that cannot contribute to a design decision. Nor does it publish material aimed at peripheral interests of an individual.

EEE is dedicated to articulate expression and clear visual presentation. It is pledged to encourage the exchange of sound engineering ideas.

EEE's editorial pages are open to enneers for bylined articles and correspond-

A member of

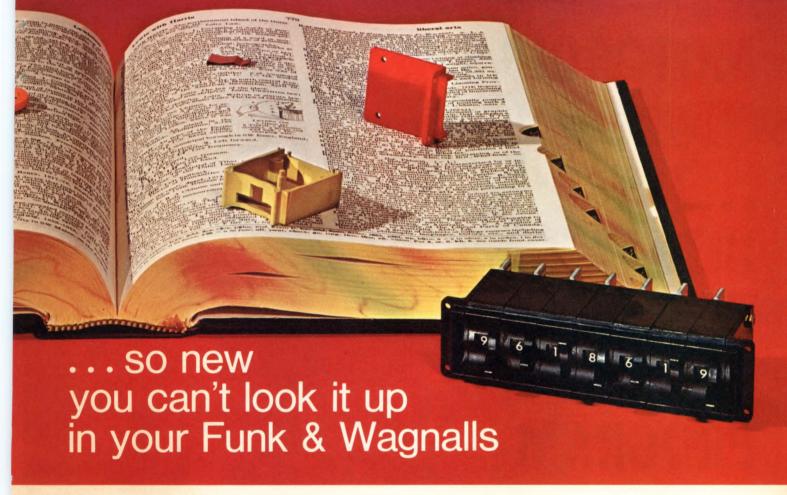




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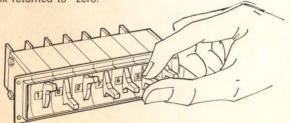
lev-er-wheel



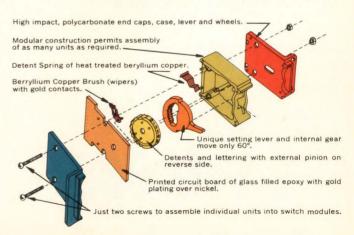
LEVERWHEEL SWITCH... a brand new concept ... Thumbwheel Lever-Action by CHERRY

FASTER SETTING: A single movement of the Leverwheel setting lever through its 60° arc is all that's necessary for a complete 10-Position cycle. (Compare *that* to plunking through the 360° rotation on conventional thumbwheel!)

Instant reset at no extra cost: A simple sweep with the hand and all levers return to home position with every switch in the bank returned to "zero."



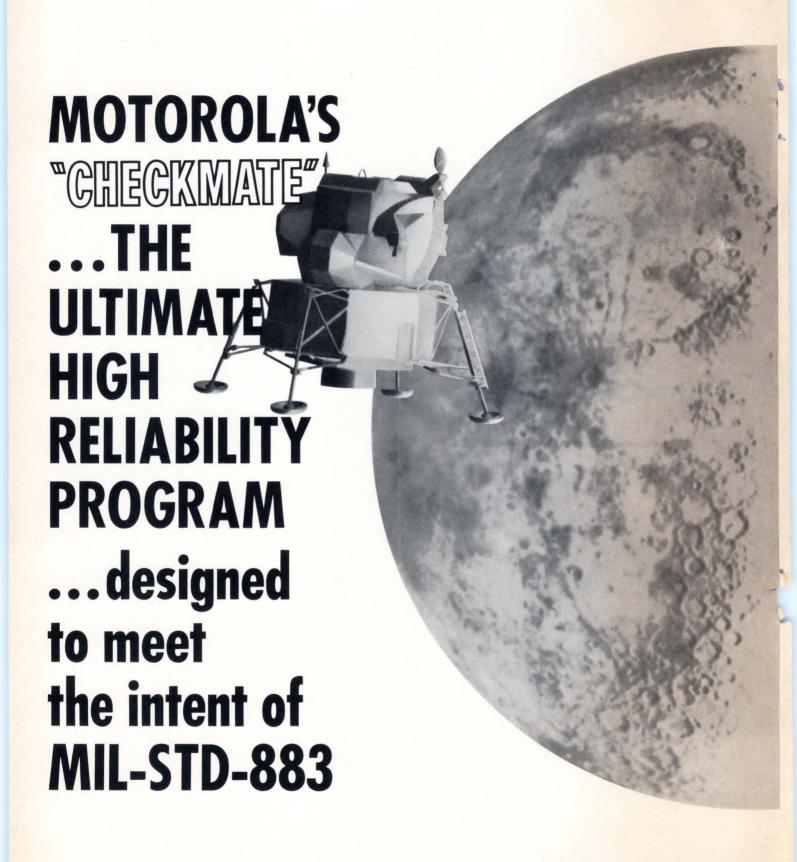
Cherry has new standard thumbwheel switches, too! Like the unique new Leverwheel, Cherry thumbwheel switches are available in miniature and subminiature sizes, totally-interchangeable with other leading thumbwheels.



SEE THE NEWEST and MOST ADVANCED ELECTRONIC KEY-BOARD at the WESCON SHOW Booth Nos. 2710-12 Sports Arena.









ESI takes the hit and myth out of laser resistance trimming:

Inset at top is full size thick film chip with 19 resistor L-cut trims, which do not show to the naked eye. Enlarged photo (approx. 8.5X magnification) shows detail of laser cuts.



Anyone who has looked into trimming resistors by laser knows: It has been a hit and myth affair.

The many variables that affect speed, accuracy and repeatability are not only difficult to control, they have been tough to classify. Film pastes, resistor or network configurations, cutting geometry, mechanical handling, laser parameters, bridge measurement capabilities, interfacing, noise . . . all affect the trimming process directly and hence design of the trimming system.

At ESI we have taken three major steps to overcome these problems and are passing these benefits on to you with the sale of each system:

- We have developed a complete family of systems to provide flexibility in trimming resistors from 1 Ω - 10 MΩ. The speed of the system depends upon accuracy required:
 - a) A high speed, low accuracy (0.1% and below) system, which employs a computer-controlled, continuous tracking bridge for closed-loop production at 5,000-10,000 trims/hr.
 - b) A medium speed, low accuracy (0.1% and below) system for lowcost research or pilot production (500-5,000 trims/hr.).
 - c) A high accuracy (0.1% to 0.001%), medium-speed system that can be either closed loop computer controlled or semi-automated by limited memory. Here a measure/ predict/trim, measure/predict/trim sequence is used.
- 2) In our test laboratory we have developed an extensive collection of data on paste variables, component handling techniques and effective cutting geometries. Specifications of the tracking bridges were determined by trimming a wide variety of thick film pastes using many aspect ratios over the complete range of resistance/square values. Lower precision cylindrical resistors were spiraled, thick films were L-cut and "top-hats" trimmed. Both YAG and CO2 lasers were used.

For thin films the measure/predict bridges have been used to cut loops and trim tabs on a wide variety of networks. These bridges are also being used in production to adjust tantalum nitride resistors by trim anodization.

3) We have assumed total responsibility for delivery of an operating system to your production or lab floor. The measurement subsystem and laser must be properly chosen to meet your particular application. Connection scanner, Q-switch, laser optics, table speed, table travel and resolution are all variables which must be tailored to your requirements.

For a no-nonsense discussion of the tradeoffs in laser trimming, get in touch with our special systems group via Ed Swenson or Bob Conway.

THE WHAT, WHY, WHEN, HOW AND WHOM OF COORS MICROCERAMICS

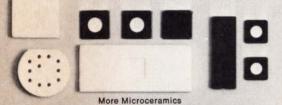
Typical Coors Microceramics

Q. WHAT ARE COORS MICROCERAMICS ANYWAY?

A. Glad you asked. They are small, precise parts of alumina or beryllia ceramic for microelectronic applications. We define small rather loosely as any part between, say, the size of a dime and a BB. The definition

of precise is more

precise: our standard tolerance is ±1%; tighter tolerances are available if needed.



Q. WHY SHOULD I USE COORS MICROCERAMICS?

A. (1) Because you can be sure they will be manufactured exactly to your specifications and not modified to suit our production capabilities; (2) Because

you can be sure they will be of uniformly high quality; (3) Because of (1) and (2) your yields will improve and your unit costs will be lower.



Q. WHEN SHOULD I USE COORS MICROCERAMICS?

A. When you want ceramic components of highest quality and reliability. Also when you need a ceramic producer with dependable, high-volume production capacity—or one that can turn out prototype and small-run quantities economically. We're geared to do both.

Q. HOW CAN I GET MORE INFORMATION ON COORS MICROCERAMICS?

A. Simply by asking. We'll be glad to counsel with you anytime by letter or phone. Or have our sales engineer in your area contact you for personal assistance. Or send you an informative data pack. Or all three.

Q. WHOM SHOULD I ASK?

A. Who else?

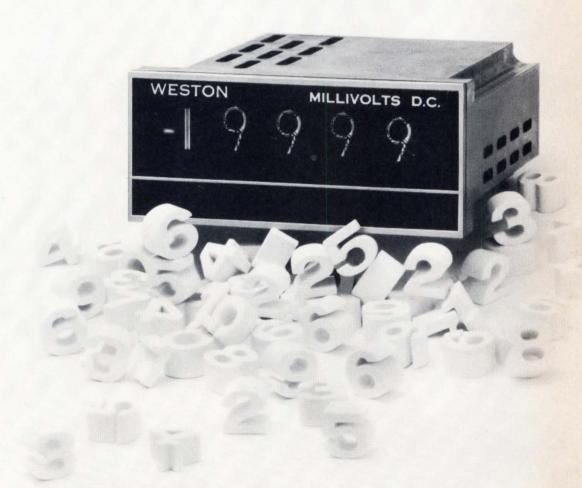
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CP-137

Still More

10 microvolt sensitivity with a lot of numbers.



40,000 to be precise.

Our latest bi-polar Model 1294 packs more numbers than any other into industry's smallest package! And it reads them with a sensitivity of 10 microvolts! The 1294 is a true bi-polar 4½-digit instrument with a display capability of 19999 and out-of-range indication. Its state-of-the-art electronics utilizes T²L logic and unique time-sharing circuitry that cuts power consumption to less than six watts. BCD output is optional. Input impedance is high: 10 meg-

ohms on the 100 millivolt range. Reading rate is 5 per second. Response time is well under one second. Accuracy is .05% of reading, ±1 digit.

Housed in the same 7 sq. in. front-

Housed in the same 7 sq. in. frontpanel-mountable case as our five other DPM's, the 1294 offers all the features that have distinguished this line... Weston's patented dual slope* integration, plug-in Nixie** tubes, repairable (non-potted) circuit boards, and ten standard voltage and current ranges. If you're sensitive about your numbers, Weston Model 1294 provides the ultimate at a reasonable price. See how the 1294 complements industry's broadest DPM line. Write for details from the DPM originators.

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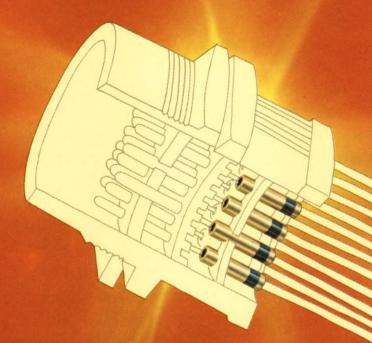
WESTON INSTRUMENTS DIVISION, Weston Instruments, Inc., Newark, N.J.

a Schlumberger company

WESTON®

^{*}U.S. Pat. #3,051,939

^{**}Registered trademark, Burroughs Corp.



Allen-Bradley type CL multi-layer feed-thru capacitors so small they fit around the head of a pin.

VOLUMETRIC EFFICIENCY. Big words that explain why Allen-Bradley type CL feed-thru capacitors are so small. Our unique multi-layer concept shaves size to a minimum, without affecting performance. It took Allen-Bradley to get filter capacitors down to their fighting weight. Now rolled capacitors are no longer a design alternative.

Concentric layers of proprietary Allen-Bradley ceramic and noble metal electrodes are fired together for unmatched protection against moisture and contamination. Rugged. Non-polar. With lower inductance and far less noise. Voltages to 200 WVDC. Temperatures to 125° C. Capacities to $1.0~\mu$ F. High dielectric strength and reliability.

Several styles and sizes are available through your appointed A-B industrial electronic distributors. For further information write: Marketing Department, Electronics Division, Allen-Bradley Co., 1201 South Second Street, Milwaukee,

Wisconsin 53204. Export office: 1293 Broad Street, Bloomfield, N.J. 07003 U.S.A. In Canada: Allen-Bradley Canada Ltd., 135 Dundas St., Galt, Ontario.

ALLEN-BRADLEY



Circle 108 on Inquiry Card

To put a priority encoder on a single chip,



Fairchild introduces the first MSI 8-input priority encoder ever put in a single package. In fact, it's the first encoder of any kind ever put in a single package.

The new 9318 accepts data from eight active low inputs, selects the most significant input signal, and provides a

binary representation of it on the three outputs. Input and output enables permit encoders to be cascaded without using additional components. This allows priority encoding of any number of input signals. Also, a group signal output is provided to show when any input is active.

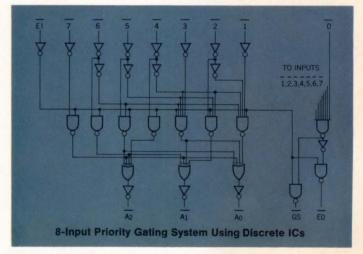
In the tradition of Fairchild's MSI family, the 9318 is a highly versatile, highly reliable device. It can be used in code conversions, multi-channel D/A conversions, and decimal to BCD conversions. It will find application

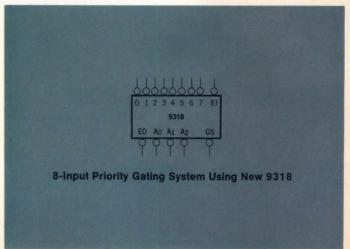
in priority interrupt systems, associative memories and keyboard encoders as well as a number of control applications.

The 9318 is TTL and DTL compatible and has a typical power dissipation of 200mW. It comes in DIP and Flatpak in both military and industrial temperature ranges.

To order the 9318	3, call your Fairchild	distributor and ask for:
-------------------	------------------------	--------------------------

(100-		PRICE		TEMPERATURE	PART	
999))	(25-99)	(1-24)	RANGE	PACKAGE	NUMBER
10.25	,	\$11.80	\$15.35	0°C to + 75°C	DIP	U7B931859X
20.50		23.60	30.70	−55°C to +125°C	DIP	U7B931851X
11.30		13.00	16.90	$0^{\circ}\text{C to} + 75^{\circ}\text{C}$	Flat	U4L931859X
22.55	1	26.00	33.80	−55°C to +125°C	Flat	U4L931851X
	1	23.60 13.00	30.70 16.90	-55°C to +125°C 0°C to + 75°C	DIP Flat	U7B931851X U4L931859X





you have to get serious about MSI family planning.

We put together a family plan by taking systems apart. All kinds of digital systems. Thousands of them.

First we looked for functional categories. We found them. Time after time, in a clear and recurrent pattern, seven basic categories popped up: Registers. Decoders and demultiplexers. Counters. Multiplexers. Encoders. Operators. Latches.

Inside each of the seven categories, we sifted by application. We wanted to design the minimum number of devices that could do the maximum number of things. That's why, for example, Fairchild MSI registers can be used in storage, in shifting, in counting and in conversion applications. And you'll find this sort of versatility throughout our entire MSI line.

Finally, we studied ancillary logic requirements and packed, wherever possible, our MSI devices with input

and output decoding, buffering and complementing functions. That's why Fairchild MSI reducesin many cases eliminates—the need for additional logic packages.

The Fairchild MSI family plan. A new approach to MSI that's as old as the industrial revolution. It started with functional simplicity, extended through multi-use component parts, and concluded with a sharp reduction in add-ons. Simplicity. Versatility. Compatibility.

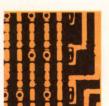
Available now. In military or industrial temperature ranges. In hermetic DIPs and Flatpaks. From any Fairchild Distributor.



REGISTERS -4-Bit Shift Register -Dual 8-Bit Shift Register



MULTIPLEXERS 9309 - Dual 4-Input Digital Multiplexer 9312 -8-Input Digital

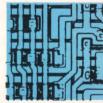


Multiplexer



COUNTERS 9306 - Decade Up/ Down Counter 9310 - Decade Counter 9316 - Hexidecimal

Counter



OPERATORS

Generator

9304 - Dual Full Adder/Parity

LATCHES 9308 - Dual 4-Bit Latch

9314 - Quad Latch

DECODERS AND DEMULTIPLEXERS

9301 - One-Of-Ten Decoder

9315 -One-Of-Ten

Decoder/Driver 9307 - Seven-Segment

Decoder 9311 -One-Of-16

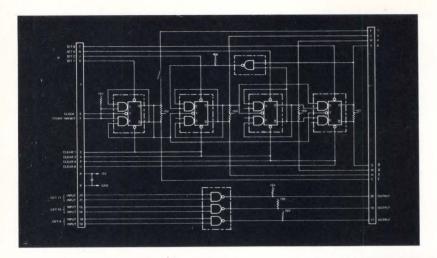
Decoder 9317 - Seven-Segment

Decoder/Driver 9327 - Seven-Segment Decoder/Driver



ENCODERS

9318 - Priority 8-Input Encoder





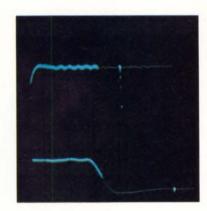








E-H the systematic solution



Whether you need a complete dynamic test system or the ideal components to integrate with your present system, look no further. E-H Research Laboratories, Inc. and its subsidiary, Automated Measurements Corporation, offer you the perfect solution.

For example, the **E-H 1139/1420 programmable timing unit and pulse driver combination** is a new generation in pulse instruments that fits the needs of any systems designer. These two rack-mounted units are so completely programmable that there are no front-panel knobs to twist. They're ideal for any systems applications requiring pulses from 1kHz to 10MHz. And they offer the designer such features as complete waveform control, with programmable width and delay from 10ns to $100\mu s$, amplitude from $\pm 3V$ to $\pm 10V$ with programmable attenuation from X1 to X40 and rise and fall times programmable from 5ns to $13\mu s$.

The perfect mate to the E-H 1139/1420 is the **AMC Model 1000 Waveform Analyzer.** The AMC 1000 was designed specifically for programmed systems application. It combines in one compact box the functions of sampling oscilloscope, digital counter and digital voltmeter to provide time and voltage measurements of sampled waveforms. The AMC 1000 is the most advanced instrument of its kind, with features including $\pm 1\%$ time measurements all ranges, fastest measurement rates, 10 remote sampling channels, all solid-state construction, serial-by-character or parallel programming, built-in program memories, stored BCD outputs, built-in floating DVM, and digital readout.

This is just a sample of the broad line of E-H and AMC equipment available from your E-H representative. He can offer you a complete system or the most advanced components to give you the systematic solution to your problems today. And tomorrow.



E-H RESEARCH LABORATORIES, INC.

Specmanship and self-regulation

Recently I received an invitation from Broadstreet's, a major clothing chain in this part of the country. It read:

To one of our most select customers: A very, very private sale at Broadstreet's. For the first time ever, we are holding a special private, private sale for four days only, June 10th, 11th, 12th, and 13th. For our special customers we are reducing just about everything (except advanced fall merchandise and formal wear) in our clothing department. Because this is a first for Broadstreet's, and the unusual nature of this private sale, you must present this invitation to take advantage of these fantastically reduced prices.

I showed up on June 11 and picked out some ties, shirts, slacks and tennis shorts. When I brought the merchandise to the cashier and presented my invitation I received a surprise — the store was charging the full price on every item.

A salesman explained to me that the sale only applied to clothing and, at Broadstreet's, only suits and sports jackets were considered "clothing." Everything else was called "men's furnishings," "wearing apparel" or assigned some classification other than clothing by the store.

Amazing.

By now you're well aware of our campaign against the practice of specmanship in the electronics industry. (Specmanship is the art of making your product appear better in your literature than it actually is.) This store's redefinition of the word "clothing," is a good illustration of how specmanship can be applied in other industries.

Specmanship, of course, isn't restricted to the electronics industry. The National Commission on Product Safety revealed a month ago that consumer-goods companies were applying it in describing the certification or endorsement of their products by private organizations using seals and other recognized approval symbols.

The Commission reported to Congress and the President that self-regulation in the consumer-goods industry is "patently inadequate" and federal regulation is "virtually nonexistent." To correct this situation, the Commission proposed establishment of a new regulatory body to standardize and enforce safety regulations for all household products including television sets and electrical appliances.

I suspect that few industries exercise effective self-regulation. The clothing industry may police itself. I don't know. (I know it can't prevent shirts and slacks from being defined as wearing apparel or accessories instead of clothing.)

It's unfortunate that Congress must consider establishing a new body to protect the consumer. But who can argue that industry has done an adequate job in providing consumer safeguards?

In the electronics industry, a small role in self-regulation is being played by the trade press. But certainly, customers are protected more by dealing with companies of known good reputation than by industry self-regulation.

In these days of increasing pressure for more federal regulatory authorities, it's time that our industry organizations paid more attention to the practice of specmanship. Unlike in many other industries, the victim of specmanship in our business often doesn't find out that he's been had until after he's made a major purchase.

Imagine the impact of an IEEE or EIA clearinghouse that would collect and analyze complaints from users of electronics products and disseminate this information on a regular basis.

Self-regulation is difficult to implement. But federal regulation is hardly a promising alternative.



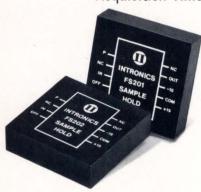
Jerry Eimbinder

JERRY EIMBINDER EDITOR

.02% Sampling Accuracy

10 mV/sec Hold Time

30 μSeC for ±10V Step Acquisition Time



Intronics' Models FS201 and FS202 low-cost sample-hold modules feature closed loop, buffered input circuitry to give maximum accuracy and high input impedance. Units are self-contained, and require only external offset adjustment for maximum accuracy. Both offer acquisition time of 30 μsec for $\pm\,10V$ step change, and turn-off time of less than 50 nsec. Low profile case allows mounting on closely spaced circuit cards.

Special features of Models FS201 and FS202:

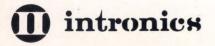
- .01% tracking accuracy
- .05% sampling accuracy for FS201, .02% for FS202
- 50 mV/sec for FS201,
 10 mV/sec hold time for FS202
- Non-inverting
- Low profile package 1.75 x 1.75 x 0.4 inches
- Cost (1-9): FS201 \$55, FS202 \$80

Models FS201 and FS202 are designed for:

- Signal multiplexing
- A/D conversion
- Pulse amplitude measurement
- Sample-data control systems

For further information or applications assistance, call or write INTRONICS, 57 Chapel Street, Newton, Massachusetts, 02158. Tel: (617) 332-7350; TWX: 710-335-6853. Or see a demonstration at . . .

WESCON, BOOTH 656, AUGUST 25 - 28



Editor's Desk

Multiplier equations

Dear EEE:

I would like to know how Bob Widlar derived the equations for the capacitance multiplier circuit on page 49 of the February, 1970 issue.

Leonard Accardi Kollsman Instrument Elmhurst, New York

Author's reply: If a current is injected into the capacitance terminal, the voltage on this terminal will be greater than the voltage on the non-inverting input and the output by

$$V = I\left(\frac{R_{\perp}R_{\beta}}{R_{\perp} + R_{\beta}}\right).$$

This defines an equivalent series resistance of $R_1 \mid \mid R_3$. For $R_1 >> R_3$, then,

$$\mathbf{R}_{5}=\mathbf{R}_{3}$$
.

The rate of change of output voltage will be (or the voltage on the capacitance terminal, for that matter)

$$\begin{split} \frac{dV}{dt} &= \frac{V}{R_{\perp}C_{\perp}} \\ &= \frac{I}{R_{\perp}C_{\perp}} \Big(\frac{R_{\perp}R_{3}}{R_{\perp}+R_{3}}\Big) \end{split}$$

which, for $R_1 >> R_3$, becomes

$$\frac{dV}{dt}\,=\,\frac{R_{\scriptscriptstyle 3}\,I}{R_{\scriptscriptstyle 1}\,C_{\scriptscriptstyle 1}}\cdot$$

Hence, the equivalent output capacitance is

$$C = \frac{R_{\perp}}{R_{\scriptscriptstyle 3}} \; C_{\scriptscriptstyle 1}.$$

With the output held at constant voltage, the current flowing will be the bias current of the non-inverting input plus the current through R_3 . The voltage across R_3 is equal to the equivalent input offset voltage with a source resistance equal to R_1 . Therefore,

$$\begin{split} I_{\text{L}} &= I_{\text{B}} + \frac{V_{\text{os}}'}{R_{\text{3}}} \\ &= I_{\text{B}} + \frac{V_{\text{os}} + I_{\text{os}} \; R_{\text{L}}}{R_{\text{3}}} \,. \end{split}$$

In practical circuits, the first term will be small by comparison to the second and can be neglected.

Robert Widlar National Semiconductor Santa Clara, Calif.

Approves comparison policy

Dear EEE:

I agree with your policy of comparing new products to old ones (*EEE* April editorial on product comparison articles, p. 15) and of giving bad points as well as good. Keep it up.

P. K. Trimble Senior Engineer General Motors Research Labs Warren, Mich.

True RMS measurements

Dear EEE:

Referring to the article "Techniques for true-RMS Conversion in DVMs" in your April 1970 issue (pp 50-52), the author Kenneth Jessen stresses the need for 0.1% accuracy, but, at the same time, limits frequency response to 45 Hz.

In almost all cases where a "true-RMS" measurement is required there is a dc component present. To ignore this dc component simply means that the indicated value is not the "true-RMS" value which is required.

Graham R. Phillips Design Engineer Century Electric Co. St. Louis, Miss.

Author's reply:

Dear EEE:

Mr. Phillips is certainly correct in stating that "true-RMS" measurement should consider not only the ac but also the dc components of a signal and that there is a need for such a measurement. It is for this reason that Hewlett-Packard's newest digital voltimeter, the 3480A, offers not only an ac coupled rms converter which gives the rms value of the ac, but also a dc coupled mode which will measure the rms value of the ac plus the dc components. The term "true-RMS" as used in the article referred only to the rms value of the ac portion of a signal.

Roger Youngberg Loveland Division Hewlett-Packard Loveland, Col.

Mr. Youngberg replied for Kenneth Jessen who is out of the country at this time.

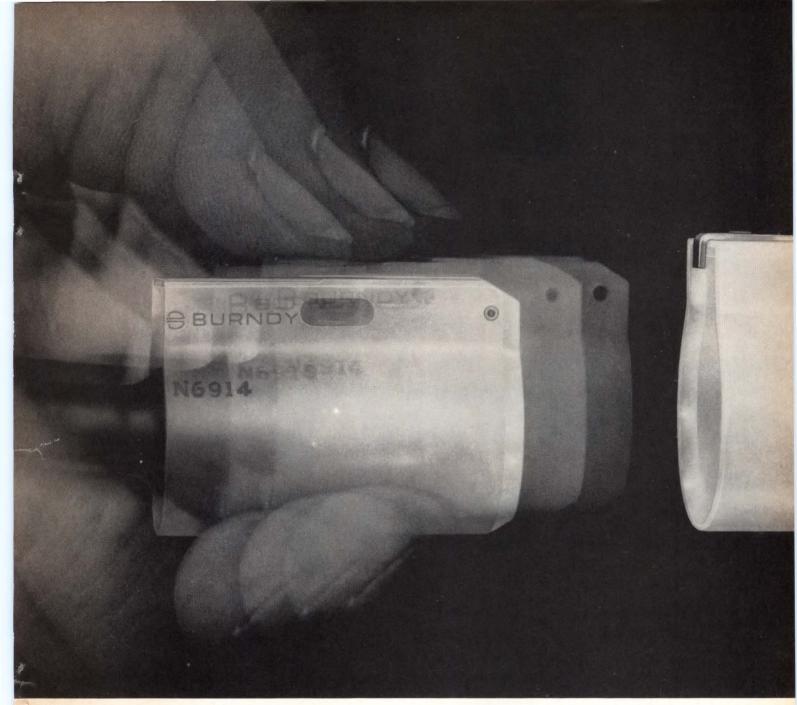
Change of address

Dear EEE:

Your April article concerning digital printers (pp. 60-69) was very interesting and informative but please note our correct address is 31 Park Road, New Shrewsbury, N.J., (P.O. Box 275 Eatontown), Thank you.

Michael Summers
DataTotal, Inc.
New Shrewsbury, N.J.

(Desk continued on page 80)



Fastest disconnect in the business

(And practically indestructible.)

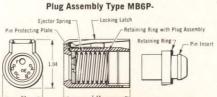
Apply gentle pressure on the locking latch of this coupling connector and the ejector spring pops the plug assembly into your hand.

It's the MB6 series, and it connects easily, too, especially in limited access areas. Manipulation for blind mating is convenient and safe, and a dead-front pin-protecting plate makes the plug "more than scoopproof". When inserted, a quick "click" lets you know it's connected . . . securely.

Burndy uses resilient nylon for both the plug and receptacle. Lightweight, reliable and low-cost, it will withstand many times more disconnects than a metal connector, without any wear or galling. Even if



ote imerination, morac

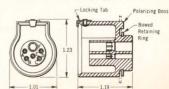


Unaffected by humidity, the MB6 is rated for temperatures from -55°C to $+100^{\circ}\text{C}$ and is shock and vibration resistant. Uses standard copper alloy gold-plated contacts installed with standard tools.

Burndy has more connectors like this, with and without the self-ejecting spring feature. Write for complete information, including test results.

accidentally stepped on, it cannot be deformed.

Receptacle Assembly Type MB6R-



Accepts five standard contacts for No. 24-20 wire, plus either one standard contact for No. 14-12 wire, or one coaxial cable contact.

National TTL/MSI tha

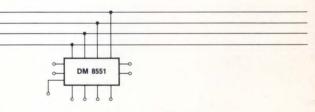
Delivery isn' the only rea

Say good-bye to slow bus systems. National is introducing Tri-State logic. A first-of-its kind family of TTL devices specifically designed to speed up bus-organized digital systems.

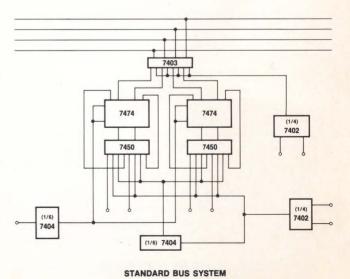
Tri-State logic allows you to work with fewer packages and without external open collector gates.

Our first off-the-shelf product in this new family is the DM8551 bus or-able quad D flip-flop. A unique device that lets you connect outputs of many circuits to a common bus line.

The DM8551 is organized as four D-type flip-flops operating from a common clock. The outputs are normal low-impedance, high-drive TTL types. Up to 128 can be tied together because, unlike other TTLs, the DM8551 can be gated into a state where both the



TRI-STATE BUS SYSTEM



sels more n Fairchild.

t som:

upper and lower output transistors are OFF. The output, therefore, appears as a high impedance. It neither delivers current nor demands significant current from the outputs to which it is connected. You get the economy of bus connection without losing output waveform integrity.

The DM8551 design eliminates the false clock-signal problem usually associated with D-type flip-flops. Internal data input disable lines feed the Q output back into the D input so there's no change of state during clocking.

Output disable lines are used for gating into the OFF state. NOR gate logic was chosen for this function since it is possible to select up to 128 DM8551s with only two BCD-to-Decimal decoders (DM8842s). You get

maximum decoding capability at minimum cost.

In addition to the DM8551, we're also introducing the DM8230 Tri-State Data Flow Gate for signal routing and the DM8831 Tri-State Party Line Driver for multiple signal driving. (They're also available off-the-shelf.)

Of course, Tri-State logic is only one reason National sells so many TTL/MSI circuits. Call any National distributor for prices and specs on twenty-seven other reasons.

National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, California 95051 / Phone (408) 732-5000 TWX (910) 339-9240

National

Significant Differences:



Most of the products that will appear and most that will be announced during WESCON will be routine. A few, like those that are described in these pages, will be significantly different.

Monolithic building blocks

A QUAD VOLTAGE SWITCH, type AD555, is the newest product in Analog Devices' line of $\mu \rm DAC$ monolithic ICs for digital-to-analog conversion. Earlier this year, the company introduced the AD550, a quad current switch.

Unlike the earlier unit, the AD555 can be used to build multiplying D/A converters (in which the output is the product of a reference signal and the digital input) as well as conventional D/A converters (in which the reference voltage remains fixed). Because the new µDAC accepts two reference inputs and because each of the references can be of either polarity (allowing four-quadrant multiplication) the circuit is extremely versatile. Its wide range of possible applications include digital-to-synchro conversion and digital gain control. Each of the four SPDT switches in the AD555 are fully buffered and can be driven from DTL or TTL logic.

Though Analog Devices calls the AD555 "the world's first monolithic multiplying D/A converter," it's not really a complete converter. In most applications it will need an external "R-2R" ladder resistor network. The company sells a packaged thinfilm ladder, type AD855, that's designed to be connected together with three AD555 quad switches to form a complete 12bit converter having an accuracy of $\pm \frac{1}{2}$ LSB. And, of course, the AD555 can be used as a building block for converters with resolutions lower than 12 bits. An 8bit converter, for example, would need only two µDAC units, plus an 8-bit ladder.

Dielectric isolation

Why didn't Analog build a complete monolithic D/A converter on one chip? The company uses dielectric isolation for the AD555, so it would have been feasible to deposit a thin-

film ladder on the same substrate — as Radiation did for its RI-1080 monolithic D/A converter. (See *EEE*, June 1970, pp. 32-38.)

Analog's engineers explain, however, that there are sound reasons for the separate-ladder approach. The major advantage of a separate ladder is that resistor values can be chosen, at will, to suit the specific application. In a 12-bit converter, for example, one would prefer to use a high-resistance ladder (say R = 50 k Ω) to minimize the errors caused by switch resistance. In low-resolution converters. the other hand, one would prefer low-resistance ladders — as these are easier to manufacture and are, therefore, less expen-

Another reason why Analog didn't put the ladder on the AD555 chip, is that the company's engineers wanted to keep the chip fairly small — to maximize yield and, ultimately, to offer a lower-cost device. This, also, was the reason why the switches were integrated in groups of four per chip rather than some higher multiple.

Also, Analog's engineers point out that, even with dielectric isolation, ladders deposited on a silicon substrate tend to be slow because of unwanted capacitances between resistors and the substrate.

The major reason why designers of the AD555 employed dielectric isolation is that the technique allows fabrication of complete wrap-around "buriedlayer" NPN transistors with saturation resistances of only 20 ohms or so. Conventional normal-sized monolithic NPN transistors, by contrast, typically have saturation resistances of 300 ohms or more. This is because conventional NPN transistors are contacted from the top through relatively high-resistance bulk silicon. Other advantages of dielectric isolation

for multiplying D/A conversion

are high breakdown voltages (allowing an input voltage range of ±4 volts for the AD555) and near-zero substrate depletion capacitance (allowing increased switching speed).

Bipolar switches

The important advantage of the voltage-switching µDAC (AD555) versus its currentswitching counterpart (AD550) is that the switches are operated in a saturated mode and, hence, will conduct in either direction. This makes it possible to use a reference voltage that's positive or negative with respect to the common output terminal. To use the AD555 as a multiplying D/A converter, an engineer can simply ground one reference terminal and apply ac to the other. Or he can use both reference terminals, injecting two reference signals of opposing polarities. Analog recommends the latter approach, wherever possible, because it results in better conversion accuracy. So that users can fully exploit the versatility of the AD555, the manufacturer is publishing an application note describing several recommended configura-

Though the AD555 can be used as a conventional D/A converter, Analog's application engineers recommend use of their current-switching AD550 for straightforward situations where the AD555's multiplying capability isn't needed. The AD555 is more versatile than the AD550, but the latter can offer better resolution and faster settling. The AD550 can provide accuracies suitable for resolutions up to 16 bits, whereas the AD555 is guaranteed to provide monotonic conversion up to 12 bits only. For 10 bits, the AD550 has a maximum settling time (to 0.05%) of only 0.8 μ s. This compares with a corresponding figure of 3.5 µs for the AD555.

The AD555 is available in

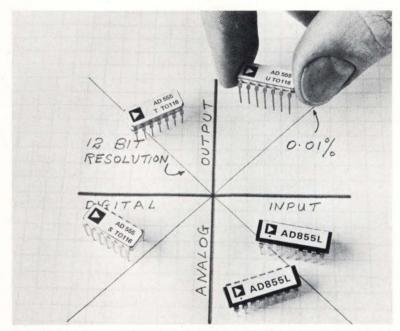
either a flatpack or a 14-lead DIP. Units meet MIL-STD-883. Versions are available for the full military temperature range (-55 to +125°C) and with tempcos as low as ± 5 ppm/°C.

AD555 units can be purchased individually (in various graded versions) or in matched sets. In quantities of 1 to 9, for the industrial temperature range, a

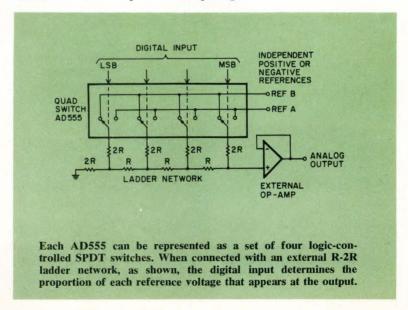
matched set of three (12 bits) costs \$96 for the AD555 units only — or \$151 complete with a precision 12-bit ladder. In 100 up, the price for three switches and a ladder drops to \$116.

We scon visitors can check out Analog's μDAC line at Booths 1206-7 (Sports Arena).

For more information on Analog Devices μDAC ICs, circle 649.



Analog Devices new AD555 IC can provide four-quadrant multiplying D/A conversion. The device and its compatible thin-film resistor network are available in either flatpack or DIP packages.

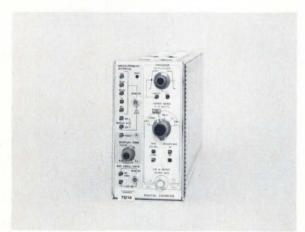


Significant Differences: Instrumentation

Scope plug-in takes fast-counter crown

THE FIRST COUNTER from Tektronix — a scope plug-in — measures higher frequencies than does any other counter without prescalers, transfer oscillators, samplers or heterodyne converters. With a frequency range to 500 MHz, the instrument snatches the high-frequency lead from Hewlett-Packard's 320-MHz 5360 which, in turn, took the crown from a Beckman 220-MHz machine last year. (See "Computing counter takes long lead in speed-accuracy," *EEE*, March 1969, pp 34-35.)

Though it now loses the top-frequency laurel, the 5360 remains the most sensational machine in the field — with far more capabilities than one would expect in a counter. The Tektronix



A scope's first counter plug-in, Tek's 7D14, allows direct measurement of frequency to 500 MHz...

. . . and provides 8-digit readout on the CRT of one of the three 7000-series scopes. When used alone, the counter plug-in can go in any of the main frame's holes. The 7704 main frame, shown here, gives a calibrated amplitude display at frequencies to 150 MHz.



7D14 doesn't match those capabilities and doesn't try. But it doesn't match the \$6500 price tag, either — even with a scope thrown in. The 7D14 costs \$1400.

To this must be added the cost of a rather expensive scope main frame — but the scope itself is sensational. (See "Feature-laden, four-plug-in scope has scale readout on CRT," *EEE*, August 1969, pp 17-18.)

Unlike all other counters, the 7D14 doesn't contain a bank of readout digits. Instead, its 8-digit readout appears on the face of a CRT, along with a legend for units like kHz or MHz. The display duration can be varied from 100 ms to 5 s or preset to infinity. The 7D14 serves as a plug-in for any of the three main frames in Tek's 7000 scope series. These main frames are the 150-MHz 7704 (\$2500), the 90-MHz 7504 (\$2000), both of which can accept four plug-ins, and the 90-MHz 7503 (\$1775), which can take three plug-ins.

Each main frame includes a character generator that's normally used for automatic scale-factor readout (V, mV, ms, μ s, etc.). When the 7D14 is plugged in, the character generator traces out an 8-digit display of frequency (to 500 MHz), frequency ratio (to 10⁵) or number of events (to 10⁸).

When a signal to be measured has a frequency within the bandwidth range of the main frame and a vertical plug-in, the signal can be displayed on the CRT and its amplitude measured along with its frequency. To trigger the counter, the signal must have an amplitude of at least 100 mV pk-pk.

Used with other plug-ins (like a delaying time base), the 7D14 permits fancy tricks like burst-frequency measurements with simultaneous display of a full signal and the burst portion, intensified and measured. For that measurement, one must use the delayed sweep as an external gate for the counter plug-in. The unit's internal gate has pushbutton selection of interval in decade steps from 1 ms to 10 s.

The instrument can accept an external timebase oscillator to provide accuracy that more closely approaches the 8-digit resolution. The internal oscillator, a 5-MHz unit, has a stability of 5×10^{-7} over 0 to $+50^{\circ}$ C and an aging rate of 1×10^{-7} per month.

Though the 7D14 is not a universal counter—it doesn't measure period or time interval—it offers great flexibility, especially when it's used with other plug-ins.

For more information, circle 643

Helipot Trims Price & Profile

89PR100K

The new Helipot Series 89 industrial cermet trimmers feature:

Low Cost:

\$1.35 each in 1-9 quantities; less than \$1.00 in quantities over 1,000.

Low Profile:

Maximum height of .250 inches allows for closer p-c board stacking.

Series 89 trimmers with two different pin spacings are available "off-the-shelf" from 17 locations across the country.

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Circle 114 on Inquiry Card

Significant Differences: Instrumentation

Self-contained digital filters arrive

IN THE PAST, the implementation of a digital filter has required extensive programming, input/output devices and a large general-purpose computer. But not any more. Now, two companies have compressed this large-scale system to rack-mounted drawer size. Both Rockland Systems, with its model 4100, and Electronic Communications, Inc., with the model 999, are producing self-contained, programmable digital filters in instrument form. These could be the start of a radical change in filter technology.

Why digital filters?

Unlike its analog cousin, the digital filter is insensitive to component-temperature variation. It does not require extremely precise components. And it requires no component changes for frequency shifting. The new filters use simple digital ICs, which remove the sensitivity problems of analog circuitry completely. However, they're a lot more expensive, at \$5000 to \$20,000, than active, fixed analog filters, at about \$50, or variable ones at about \$1000.

The digital filter can be multiplexed easily since its signals are already digitized. In contrast, an attempt to multiplex an analog filter is equivalent to introducing a step function, which produces ringing. Since the digital filter can be time shared, it can have either multichannel operation or recirculation of one line of data through the same section to simulate a cascaded filter. Either of these ap-

proaches would require many analog filters.

Since the digital filter is inherently capable of program control, it can be run in a mode that adapts to the incoming frequency. This opens the possibility of tracking filters. There are analog filters capable of this mode but they still suffer from sensitivity problems.

Both new instruments are, in effect, special-purpose computers. Each accepts analog signals and digitizes them with an A/D converter. The quantized signals are then processed in the computing section of the filter and reconverted to analog form by a D/A converter. The filtering circuitry is composed of MOS shift registers and TTL logic.

Effects of frequency range

The Rockland 4100 offers either recursive (poles and zeros) or non-recursive (zeros only) characteristics, while the ECI 999 offers only nonrecursive structures. Recursive filters are used for sharp (!) frequency cutoffs that approach the theoretical "brickwall" functions. Non-recursive filters provide extremely accurate (limited by the computer's bit capacity) phasevs-frequency characteristics, typically 100 times better than those of equivalent analog filters.

The 4100's 500-kHz sampling rate gives it several advantages over the 999, with its 10-kHz rate. The high sampling rate allows a 200-kHz input while the ECI unit accommodates only 3.5 kHz.

While in theory, any digital filter can be multiplexed, in practice, the number of channels is limited by the instrument's sampling rate. The switching circuitry may or may not be built into the instrument. Rockland has built-in multiplex capability while ECI will soon offer multiplexing as an extra-cost op-



ECI's digital filter, programmable with paper tape.



Rockland's multiplexable digital filter.

tion. Further, Rockland's high sampling rate permits multiplexing as many as 50 channels (at a 10-kHz sampling rate). And the 4100 can recirculate digitized data of a single input through one filter section 50 times at a 10-kHz rate, producing the equivalent of a 50-section filter.

Differences in programming

While the Rockland machine whips the ECI in speed and in its offering both recursive and non-recursive filtering, ECI comes out ahead on programming flexibility. The 999 is programmed for a particular filter type through a built-in paper-type reader. This provides a flexible input link to a MOS shift-register memory.

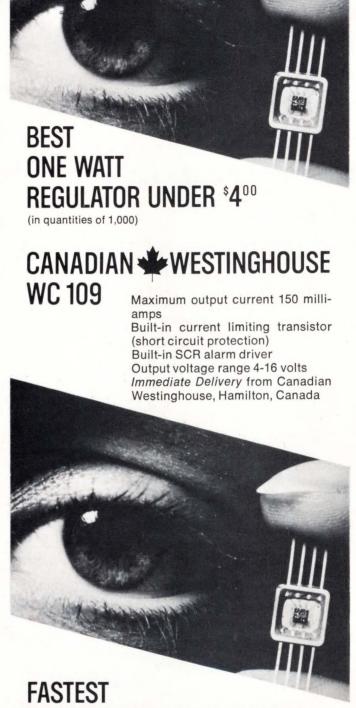
In contrast, the 4100 can be supplied with either a ROM or a read/write MOS shift-register memory. If supplied with a ROM, it's a fixed-instruction machine, requiring no external I/O devices. To change the filter program, one must purchase another ROM from Rockland. With the ROM, the machine can still multiplex, recirculate data and act as a tracking filter. With a read/write memory, the 4100 can be externally programmed with an optional keyboard or with other input links.

The ECI filter costs \$17,-300. Rockland's filter ranges from \$5000 for the basic unit to \$20,000 for the option-loaded model (keyboard, read/write memory, etc).

Rockland will also be offering five custom programmable digital filters — now on the drawing board. These include a narrow bandpass filter (the 4300), a comb filter (the 4400) and other specialized filters.

For more information on the Rockland filter, circle 641.

For more information on the ECI filter, circle 642.



OPERATIONAL AMPLIFIER WC 161 Q

Band width > 30 MHzSlew rate $> 150 \text{V}/\mu \text{ sec.}$ Low offsets and offset drifts.

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ARS LINEARS LINEARS LINEARS

Circle 115 on Inquiry Card

Significant Differences: Packaging

Adjustable cage for almost any PC

A CARD CAGE from Thermalloy, the 5201, offers more packaging flexibility than does any other on the market. It allows an engineer to mount PC cards of almost any height and depth with almost any card-to-card spacing with almost any connector. And it allows him to make changes quickly and easily.

Its restrictions are very few and unimportant for most applications. The cage does not accept a mix of card heights. It accepts only a single card thickness — 1/16 inch. And it's available off the shelf in only one overall width, suitable for a 19-in. rack, though Thermalloy can easily alter the width to suit individual requirements.

An engineer can mount cards in the new cage almost instantly since it's shipped fully assembled. He's likely to start by sliding the chrome-plated steel end plates up or down to accommodate his card height, then tightening

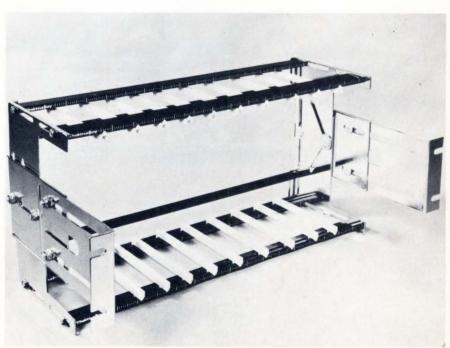
four 5/16-in. nuts. The cage accepts cards from 3-1/2 to 7 inches high.

Then he snaps in polycarbonate card guides anyplace along the width of the cage. A pointer index at the end of each card guide and silk-screened graduations, a tenth-of-an-inch apart on the black-anodized aluminum guide rails, help eliminate problems in top-to-bottom alignment. If a man finds that components on some cards are higher or lower than expected, he can quickly snap out the card guides and move them further apart or closer, then snap them in again.

Next, he can mount almost any connectors on rear rails that he can slide up or down then lock in place with a screwdriver. Finally, he can adjust the end plates to allow mounting cards up to 10 inches deep, lock the end plates with a nut driver and mount the entire package in a conventional 19-inch rack.

This remarkably flexible card cage costs \$24.95 (1-49), just a few dollars more than fixed or limited-adjustment cages. Card guides cost 18ϕ to 20ϕ apiece, depending on quantity.

For more information, circle 644



Mutually interdependent end plates on this new Thermalloy card cage permit symmetrical adjustment to accommodate cards of different lengths and heights.

Significant Differences: Microelectronics

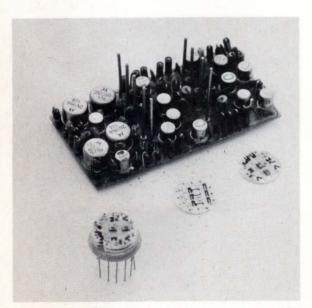
Tiny hybrid-IC amplifier slews at 1000 V/s

LAST YEAR, DDC (formerly Data Device Corp.) introduced a really fast wideband amplifier module, type VA-23, with a maximum slew rate of over 1000 V/µs. (See "New Leader in Fast Op-Amp Race," *EEE*, March 1969, p. 40.) Now the company has shrunk its original design to produce a tiny hybrid-IC version that offers the same excellent frequency response — but which is packaged in a TO-8 can.

Like its big brother, the new amplifier (designated HVA-23) is an inverting-only design — it's not a true differential op amp. But nevertheless, the HVA-23 should be able to fill the vast majority of wideband-amplifier applications.

For non-inverting applications, DDC has introduced another hybrid unit (type HFB-7). This is a high-power FET-input amplifier with an output-current capability of 50 milliamps. The HFB-7 however, is a unity-gain amplifier, whereas the HVA-23 has an open-loop gain of 106 dB. Thus the HFB-7 is expected to find use as a buffer amplifier, in sample-and-hold circuits, and as a current booster for IC amplifiers. Both the HVA-23 and the HFB-7 can slew at rates exceeding 1000 V/ μ s and have small-signal bandwidths of 100 MHz.

A third new hybrid unit, type HFS-23, is similar to the HVA-23, but has been designed specifically for fast-settling applications. Settling times for the HFS-23 are 300 ns (to 0.1%) and 600 ns (to 0.01%). Both the HFS-



Engineers at DDC took their discrete-component wideband-amplifier circuit and produced a hybrid-IC version in a TO-8 can. The hybrid amplifier has three substrates stacked one above the other.

23 and the HVA-23 can deliver ± 10 volts at 30 milliamps.

New hybrid facility

During the past year, DDC has been quietly setting up a production line for hybrid ICs. The new facility is geared for a moderate production level of around 50,000 completed substrates per year. These will be used to produce about 12,000 complete amplifiers, with from one to three substrates per amplifier. Other substrates will be used in data-conversion modules.

According to Jerry Heller, DDC's president, the company intends to place major emphasis on hybridizing standard products, rather than seeking custom business. Therefore, DDC's engineers are currently redesigning several of their successful discrete-component circuits for hybrid fabrication.

The hybrid versions, in many cases, will offer performance superior to that of their discrete counterparts. This is because the effects of circuit inductance and stray capacitance will be minimized, thus allowing greater bandwidth and faster settling. And, of course, hybrids offer small size, sealed packages, and operation over the full military temperature range. Each of the three newly announced amplifiers operates over the range -55 to +125°C.

Three-tier circuit

DDC's engineers found that hybridizing the old VA-23 hybrid amplifier was a tough assignment. Some of the capacitors and power transistors stubbornly refused to be squeezed into a TO-8 can. In the final design for the hybrid version, DDC used three thick-film substrates stacked one above the other inside the tiny can. To minimize internal dissipation (and resulting temperature drift) some of the output current was traded off. The HVA-23 delivers 30-milliamps at ± 10 volts, whereas the older VA-23 can deliver up to 60 milliamps. Also, current limiting was added to protect the internal circuitry from overload.

The unity-gain HFB-7 proved slightly easier to package. For this amplifier, DDC was able to get all the circuitry onto two substrates.

Evaluation quantities of the HVA-23, HFS-23 and HFB-7 are now available from stock. Production quantities will be available for delivery in mid-September. Unit quantity prices are expected to be around \$125 for the military-temperature-range circuits. Industrial versions will be available later at lower cost.

By the end of this year, DDC expects to have a complete line of wideband amplifiers, plus a number of data-conversion circuits, available in hybrid form.

For more information, circle 648.

Significant Differences: Power Sources

Mystery regulator cuts power-supply size, cost, noise

THE HIGH EFFICIENCY of a new regulator, even at low voltages, gives a new line of power supplies less internal dissipation, thus smaller size for a given output. Perhaps because of the new regulator or perhaps because Dynage wants to sell lots of supplies from its L series, the price is down, too. So a user gets more watts per cubic inch, or more watts per buck or, in many cases, both—a rare and attractive combination.

A first thought on learning of a small, high-efficiency supply is that it uses a switching regulator rather than a linear series regulator. Switching regulators, unfortunately, are noisy. Without careful filtering, they can shoot mean spikes out to the dc load and, in fact, can spray them around in the form of radiated interference.

The L series, however, doesn't use a switching regulator, nor does it use dc-dc conversion, another source of noise. The type of regulation is a guarded secret with engineers at Dynage, who say, only, that they use a "modified" series regulator with a choke-input filter.

The usual series regulator makes for overall inefficiency, especially at low voltages, because the drop across the pass transistor isn't negligible as a percentage of the output voltage. As an example, for 5-V output, the conventional series regulator provides typical efficiencies of 30 to 35%. Dynage's L series, at the 5-V level, boasts better than 50%.

That's on a par with efficiencies of SCR and dc-dc conversion types, but without the noise. At higher temperatures, this advantage becomes more pronounced, since the L requires less derating than almost any other supply on the market. One exception is the Trio Labs SP601, a dc-dc conversion type, whose maximum output at 71°C, 110 watts, is the same as its 50°C output, suggesting that the latter is specified very conservatively.

The Trio unit, with a maximum output of 5.5 V at 20 A in a 150-



Smallest of the new Dynage L-series supplies, which come in five case sizes, this one has dimensions of $3-3/16 \times 3-3/16 \times 7-1/4$ in., weighs four pounds and offers nominal voltages from 5.25 to 25.2 Vdc, each adjustable $\pm 5\%$.

cubic-inch package, has the best volumetric efficiency of any supply delivering 100 watts or more at nominal 5 volts. Though it's a dc-dc conversion type, it isn't very noisy, either. Maximum ripple and noise is 50 mV pk-pk as observed on a 50-MHz scope.

Worst-case regulation, 0.3% for line plus load, isn't bad either. But the price, \$400, gives a cost per watt of \$3.64, which is very rich for supplies in the 5-V 100-W class. This is one case where the Dynage L comes out behind on voltmetric efficiency, but way ahead on price.

A comparable unit, the Dynage L5.25-18, delivers 98 W at 5.5 V in a 218-cubic-inch package. That's 0.45 watts per cubic inch (which beats all units in this class except the Trio at 0.73 W/in.³). But at \$219, the unit has a cost per watt of only \$2.24, which makes one think twice about Trio's \$3.64.

In smaller units, Dynage gets beat in volumetric efficiency by ACDC Electronics, whose JRK10 delivers 47 watts from a 57-cubic inch package while the Dynage L5.25-14 gives 77 watts from 146 cubic inches. That's 0.77 W/in.³ for ACDC and 0.55 W/in.³ for Dynage. But again, Dynage runs ahead on price. At \$169, vs ACDC's \$290, the Dynage takes \$2.20 per watt while ACDC takes \$6.50.

Dynage's cost-per-watt advantage becomes even more startling at higher temperatures, where other supplies (except the Trio) suffer severe derating. Thus, in Dynage's five case sizes (from 74 to 1004 cubic inches), the power-output rating at 71°C ranges from 16.3 to 19.3 percent down from the 50°C rating. In competitive supplies, the derating at 71°C runs up to 76 percent (for an SCR supply from Lambda).

While Dynage's L beats competitive supplies on a dollars-perwatt basis and, in most cases, on a watts per-cubic-inch basis, it doesn't always win on regulation and noise specs.

Combined line plus load regulation is 0.5% max, which isn't bad, but it isn't great. And ripple plus noise (measured on a 50-MHz scope) is a very good 15 mV peak to peak, which is fine, but not spectacular.

All the Dynage supplies accept (with some derating at the extremes) line voltages from 95 to 132 Vac (or 210 to 250 V) and they can all be adjusted to ±5% of the nominal output voltage. All have built-in overvoltage and short protection and all permit remote programming, remote sensing and parallel operation.

For more information on the Dynage supplies, circle 647.

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immediate delivery on the above devices. (Except those noted*. They'll be available within 30 days.) Check with your Signetics Distributor. You'll find the price is right. And that's our final announcement.



Significant Differences: Display Devices

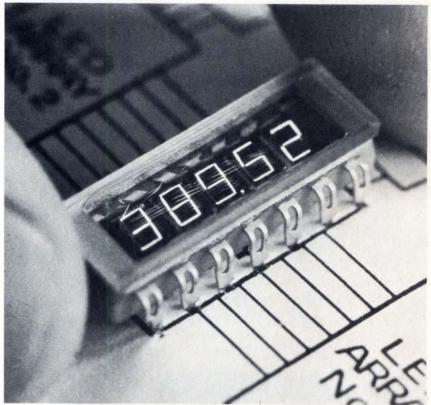
HP jumps past Monsanto in LED readouts

THE TWO-YEAR-OLD LED-readout war between Hewlett-Packard and Monsanto continues. It started when Monsanto introduced two expensive numeric readouts using gallium-arsenide-phosphide light-emitting diodes (see "Two more contenders for readout throne," *EEE*, June 1968, pp 26-28). That put Monsanto in the lead, for there was no competition.

HP entered the fray and jumped ahead later that year. (See HP outshines Monsanto with 28-dot GaAsP readout," *EEE*, Nov. 1968, p 26.) Then Monsanto came back. (See "Monsanto beams 7 bars at HP's 28 dots," *EEE*, July 1969, pp 18-22.) Trying to clinch its lead, Monsanto modified and reintroduced one of its original readouts and slashed its original prices. (See "Dots, filaments in five new readouts," *EEE*, Oct. 1969, pp 18-24.)

HP tried to close the gap early this year by cutting its own prices. But Monsanto jumped ahead again, just a few months ago, with the first commercial monolithic LED readout - a 7segment type that goes for \$12.45 in 1-9 and \$7.55 in 1000-up, prices that EEE described as "gorgeous." (See "Monolithic fabrication shoots down prices in LED readouts," EEE, May 1970, pp 30-32.) Since that article, Monsanto made two significant changes. It made the readout available in a dual-inline package as well as the original flat pack. And it cleared up what EEE had described as "a not-too-clean epoxy lens."

Now HP is ahead again. Just in time for introduction at WES-CON booth 1525, the company introduced monolithic 7-bar LED readouts at prices that are even more gorgeous than those from Monsanto — but just barely. With per-digit costs from \$11.95 (1-9) to \$7.05 (1000-up), HP



Newest and lowest-cost LED display, with 3, 4 or 5 digits per package, comes in an hermetically sealed DIP or flat pack. Wiring, apparent in this photo, isn't obvious in the actual device.

slides under Monsanto by 50 cents.

The new HP readouts differ in several ways from earlier ones. First, they're available only in 3-, 4- and 5-digit versions while all others are single-digit units. They're hermetically sealed, like earlier HP readouts and unlike Monsanto readouts.

The units require external decode/drive circuitry, as do Monsanto's displays. This is a departure for HP, whose earlier dot-matrix readouts included an on-board decode/drive IC.

Digits require even less power (1.6 V at 3 mA per segment) than does Monsanto's MAN-3 which, at 1.6 V at 5 mA per segment, takes less than any oth-

er readout. But the digits aren't as bright as Monsanto's (100 ft-lamberts vs 200) and they're a trifle smaller. Character height is 0.1 in. (vs Monsanto's 0.116 in.) and width is 0.06 in. (vs 0.067 in.). As with all LED readouts, the apparent character size is invariably larger than the actual size.

The units are available in flat packs and DIPs and HP plans to offer future versions with larger and smaller characters, in a variety of packages and with large-quantity prices as low as —now catch this—\$2 per digit.

For more information on HP's latest readout, circle 645.

For more information on Monsanto's latest, circle 646.

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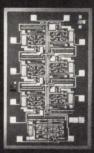
GENERAL PURPOSE 300-OHM SWITCH

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GENERAL PURPOSE 30-OHM SWITCH/ AMPLIFIER

HDGP1001. General purpose 30-ohm diode-protected P-channel enhancement mode device. For easy interface of DTL or TTL circuits to MOS levels. Ideal for low cost applications. 80c each (100 up).



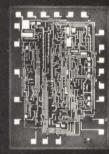
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Significant Differences: Instrumentation

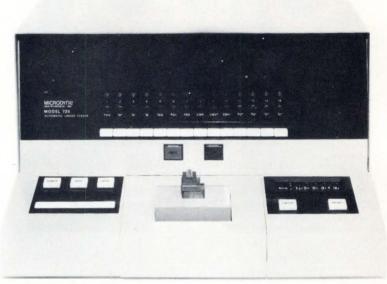
High-versatility LIC tester for op amps, comparators and voltage regulators

MICRODYNE HAS LEAPEROGGED ahead of its competitors with a versatile linear IC tester called the model 735A. This unit is the first type capable of testing IC op amps, comparators and monolithic voltage regulators. In addition, it will also check high-voltage and dual op amps. For each required parameter the unit displays the actual measurement and the test limit in engineering units on dual DPMs. Results are also displayed on individual "fail" lamps. The unit is capable of manual or automatic operation and has an optional data-logging mode.

The basic 735A measures 14 dc parameters. It measures input offset voltage (to an accuracy of 1%) positive bias current (to 3%), negative bias current (3%), average bias current (1%), input offset current (1%), open-loop voltage gain (1 dB), power-supply rejection (2 dB), commonmode rejection (2 dB), positive common-mode voltage range (3%), negative common-mode voltage range (3%), positive output-voltage limit (1%), negative voltage limit (1%), positive power-supply current (1%) and negative power-supply current (1%).

Programming

Before checking a particular linear IC, it is necessary to store its test limits in an internal MOS shift-register memory. Each limit is entered sequentially through



Microdyne's new versatile linear IC tester, for op amps, comparators and voltage regulators.

three thumbwheel switches. By rotating a dial (TEST TO BE PROGRAMMED) the operator may verify the limits on the test-limit DPM. The same limits may alternately be set by punched cards, teletypewriter or a computer interface.

Testing

The IC under test is plugged into a special adapter board which fits a unique IC in all its package forms. A performance board for dc-measurements is inserted in the 735A. The unit can then either be automatically stepped

through the fourteen tests in two seconds or tested manually. At each individual test, the value of the parameter in correct units is displayed on the "test result" and "limit" readouts. Each test has a separate test-indicator lamp and "fail" lamp. There is also a master fail-pass set of lamps. If desired, a failure in any position can be programmed to stop the testing operation. The tester may also be set to skip certain parameters if necessary.

If it is desired to test an op amp for such factors as slew rate or open-loop bandwidth, a differ-

Comparison of LIC testers

IC Tester	No of Tests	Test Readout	Automatic Limit Readout	Test Limits	Op Amp Slew Rate	Test HV Op Amp	Test Compar- ator	Test Regu- lator	Price (\$)
Microdyne 735A	14	DPM Abs units	DPM Abs val	Var	Yes	Yes	Yes	Yes	9350
Philbrick 5104	15	Meter Abs units	No	Var	Fall 70	No	Fall 70	Nó	4500
Signetics 1420	14	DPM % of limit	No	Fixed	Yes	No	Yes	No	7450

ent performance board and the same adapter are required. Performance boards for comparators and integrated voltage regulators are also available but they require new adapter boards.

The 735A has an option for a data-logging mode. It contains the necessary circuitry to interface with computers, printers, automatic handlers and other inputoutput devices.

Comparison with other testers

The table compares the Microdyne 735A with its two main competitors: the Teledyne Philbrick Nexus 5104 and the Signetics 1420. The following advantages of the 735A are apparent from the table:

- (1) It is the only unit with both the test result and the limit setting displayed on 3 digit DPMs in engineering units
- (2) Its test limits are variable affording a measure of flexibility.
- (3) It is the only unit to test high-voltage op amps and IC regulators.
- (4) It has all the desirable features of the other two units.

All three units provide automatic testing and the Microdyne and Philbrick offer manual testing as well. The Philbrick will offer tests of comparators and of op-amp slew rate at an additional cost of \$2000 in the fall of this year.

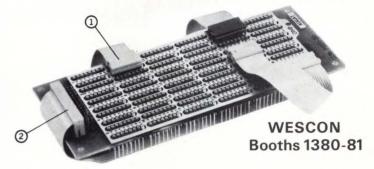
The main disadvantage of the Microdyne tester is its high cost. It should be noted that this includes the basic (dc op amp) cost of \$8000 plus the cost of an ac performance board, a comparator board and an IC regulator board. If any of these functions are not required the cost decreases accordingly.

For more information on the Microdyne tester, circle 650.

For more information on the Teledyne Philbrick Nexus tester, circle 651.

For more information on the Signetics tester, circle 652.

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Significant Differences: Microelectronics

First complete hybrid-IC analog multiplier

BOTH MONOLITHIC and discrete-component analog multipliers will face tough competition from a new hybrid-IC multiplier to be introduced at Wescon by Burr-Brown. Unlike monolithics, the new hybrid is fully tested and needs no external components to "make it fly." Unlike discrete-component modules, the new hybrid has a really tiny package and is available in a sealed metal-can version that meets military environmental specs. And the hybrid IC should prove more reliable than monolithic multipliers (with their external discrete components) and conventional modules (with their internal discrete components).

Burr-Brown's new hybrid multiplier comes in two basic versions. Model 4090 is an epoxyencapsulated unit for operation from -25 to $+85^{\circ}\mathrm{C}$, while Model 4091 is a cold-welded hermetically-sealed flat package for the full military range of -55 to $+125^{\circ}\mathrm{C}$. The epoxy version has dimensions of $0.75 \times 0.75 \times 0.25$ inches, and the flat pack is $0.9 \times 1.0 \times 0.25$ inches.

Multiplier within a multiplier

The circuitry inside the hybrid multiplier is an interesting combination of monolithic chips and thick-film networks. A monolithic multiplier chip and an op-amp chip are the key components; the rest of the circuit consists of 27 resistors and one zener diode. The monolithic multiplier, of course, provides the actual multiplication and the op amp provides the correct output levels. The remaining circuitry biases the chips, reduces sensitivity to power-supply variations and sets the overall gain.

Both the 4090 and 4091 are offered in "A" or "B" versions with total accuracies of ±2 percent and ±1 percent, respectively. Units meet these accuracy specs with no external trimming. The specified accuracy includes all contributing factors — output offset, input offsets, gain error and nonlinearity error. Burr-Brown also specifies linearity separately — even though this is included in the total accuracy spec. The linearity spec is useful because, in some applications, one may wish to adjust offsets and gain elsewhere in the system, leaving nonlinearity as the only error. The units with ±2-percent accuracy have ±1-percent linearity. Similarly, the versions with ±1-percent accuracy have ± 0.5 -percent linearity.

Burr-Brown's accuracy specs, however, do not include the effects of temperature varia-



tions. Accuracy drift is listed separately, and is ± 0.1 percent per degree C for all versions. As with the accuracy spec, accuracy drift includes all contributing factors — variations in offsets, gain and linearity.

Limited bandwidth

One possible disadvantage of the new hybrid-IC multiplier is that bandwidth is less than that provided by some discrete-component and monolithic multipliers. Though the transconductance technique can theoretically provide bandwidths of many megahertz, the Burr-Brown circuit has a small-signal bandwidth of only 100 kilohertz. Burr-Brown engineers explain that, in the 4090/4091, bandwidth is restricted by the response of the low-cost IC amplifier chip. Though better monolithic op amps are available, they tend to be much more expensive. Therefore, designers of the new multiplier decided to trade off bandwidth to minimize cost. The full-power response for the 4090/4091 is 50 kilohertz, and the frequency for one-degree phase shift is 3 kilohertz.

Like most discrete-component multipliers and op amps, the new hybrid multiplier operates from ±15-volt power supplies. Thus the hybrid version can be operated more conveniently than commercially available monolithic multipliers (such as the Motorola MC1595) which need either an additional 32-volt supply or extensive level-shifting circuitry to provide optimum performance. Another advantage of Burr-Brown's hybrid circuit is its power-supply rejection — typically ±100 millivolts of output variation per volt of supply variation.

Prices, in quantities of 1-9, are \$45 and \$75, respectively, for the "A" and "B" versions of the 4090. The "A" and "B" versions of the 4091 cost \$65 and \$95, respectively. Delivery for small quantities is from stock.

Burr Brown's new hybrid multipliers will be exhibited at booths 1135-6 (in the Sports Arena) during the Wescon show.

For more information, circle 647



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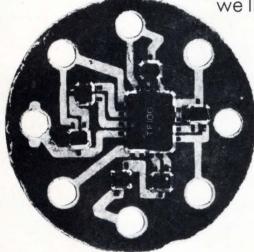
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RG320, 1, 2, 3: Triple 3 input NAND gate	Now
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RL40, 1, 2, 3: Independent Carry fast adder	Now
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Nick DeWolf Of Teradyne Speaks Out: Speed Kills

Speed kills

I'm talking about the kind of speed that otherwise sane engineers build into semiconductors at the expense of reliability, economy, safety and everything else that should be holy. They do it because it's fashionable to be fast, and the rest of the world eggs them on by overspecifying speed, by demanding nanoseconds where milliseconds would do.

It's not hard to understand the pressures for speed. After all, it's easy enough to build an adder that adds, so once you've done that, you start looking for some other measure of how much you've pushed yourself. An obvious test is how fast you can add. Another is how small you can make the adder. Another is how reliable or inexpensive you can make it, but somehow that doesn't sound as exciting to most people.

Now, I am perfectly aware that there is an honest, legitimate requirement for speed sometimes, and if you have to go fast, you have to go fast. My point is that most of us don't have to go as fast as fashion tells us to go. And when you lose sight of that fact you pay through the nose, because speed — in anything from automobiles to pep pills to transistors — is always a bad bargain.

Here we really have a question of engineering sanity in setting design priorities. If speed is at the top of the list, everything else suffers. If, instead, an engineer backs off on speed in his design criteria and looks at total economic justification, reliability, etc., letting speed fall where it may, he will design a better system.

The urge to make things small, incidentally, is a blood brother of the urge to make things fast. Miniaturization can kill, too. Interestingly enough, these two yahoo concepts — speed and size — are in mortal conflict. Fast things are usually bigger than slow things, because there is more power to be dissipated, and more crosstalk and shielding to worry about.

Let's look at cases. Suppose an engineer designing a small computer rules out "slow" TTL logic in favor of ECL, thinking that in so doing he has not only shaved his delay times but also solved his glitch problems. But he soon finds that instead of eliminating glitches he has just moved the problem up to X-band, and now he has magnetic-coupling problems he never dreamed of before. If he's clever, he winds up no worse off than when he started, except that he may find his 1/4-inch-square device burning up 600 milliwatts, or about enough to melt the markings.

But that's only part of the story. The speed freak also throws away noise rejection, which is really the name of the game in industrial design. A high-speed device is always going to be more sensitive to high-speed digital noise than a slow-speed device. And what happens when a stray 5-nanosecond glitch puts a wrong bit into memory? That wrong bit sends the computer to the wrong address, which then gives the whole computer a nervous breakdown. A computer can be operationally destroyed by the funniest little noise that occurs once every six hours.

The extra power needed to go fast, also means extra heat, and this often means a cute little fan with its dirty little filter to carry away that extra heat. Everyone knows that the filters never get cleaned, and common sense tells you that the very presence of a fan means that the equipment needs free air, so where does that leave you? With a piece of equipment that was born to destroy itself.

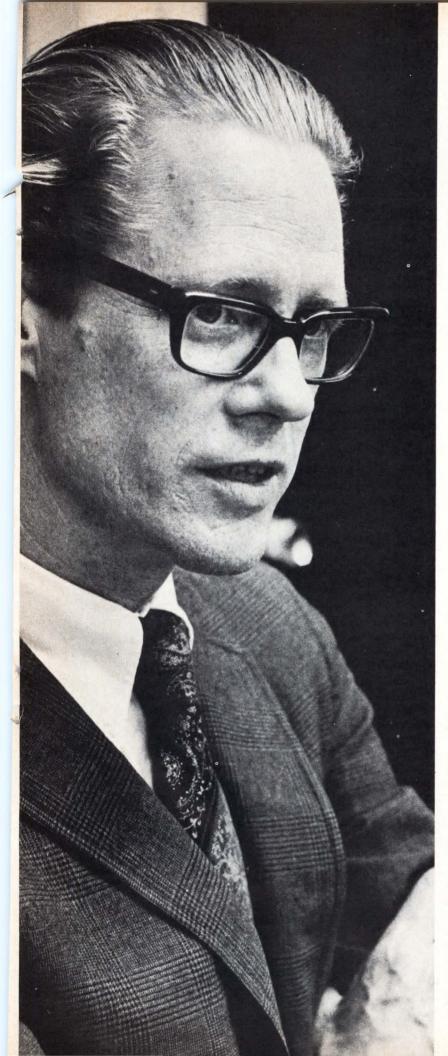
Extra power also means extra money to supply the power. In the speed world of TTL, every dollar's worth of ICs need a dollar's worth of power supply. At that rate, an eventual billion-dollar IC market means a billion-dollar power-supply market. Zowie.

People who design and build industrial test equipment are as subject to speed pressures as anyone. But I believe that we should put these in their proper priority, which is after the pressures to test reliably, safely, and economically. And when we look for reliability, safety, and economy, we quickly learn that slow is good.

For openers, "slow" rejects noise.

A "slow" DTL circuit in an instrument will generate 1/100 the noise and be only 1/10 as sensitive to noise as conventional TTL. Of course, that means going four or five times slower than you could with TTL, but in many





cases that's still plenty fast.

Slow consumes less power. That dollar's worth of power supplies I mentioned could come down to about a cent. Not to mention all those fans and filters (both air and noise-suppression) you don't have to use.

I really have no axe to grind on TTL, ECL, and other high-speed families. Where you honestly need all that speed, you need it, and that's that. But a good designer ought to know what he's paying to gain those nanoseconds. I wonder if most TTL users are aware of the egregious current transients TTL inflicts on the power supply, for instance. When a TTL gate bombs from one state to the other, it draws from six to eight times the current it draws at either one of those states. Moreover, when the TTL gates pulls up, it derives the current to pull up the output capacitances from the harassed power supply, whose glitches are transmitted to all the "up" outputs. Of course, the power supply has to be bigger in the first place to support the extra current. As if all this were not bad enough, TTL also does you out of any chance of using the "wired-OR" connection, which greatly simplifies so much circuit design.

The push for speed has been a dominant influence in the whole IC business, and it hasn't been a healthy influence. IC vendors who don't have to worry about the marketability of their transistors, gold-dope them to death and get away with it. Having proved that point, they should take a fresh look at the situation and consider other approaches. We've found, for instance, that we can achieve excellent noise rejection through the use of hole storage to utterly stall the gates — a pretty appalling idea to a confirmed "dope fiend."

If deliberately going slow sounds crazy, consider this crazy thought: If bipolars were designed with pinch resistors to go as slow as MOS devices, they could handily compete with MOS for packaging density, "real-estate" advantages, etc., revolutionizing the whole IC technology. The hang-up has been that the bipolar people, absurdly overplaying the importance of resistor tolerance, have been trying to make precision resistors.

How slow is slow?

This whole device-speed argument really involves the order of magnitude on either side of 50 nanoseconds. I feel comfortable with 500 nanoseconds, but 5 nanoseconds is a killer. So I leave 5 nanoseconds to those who are bent on suicide. In an IC test system that takes 10,000 nanoseconds per test, for example, I sure as blazes ought to be able to get along with 50-nanosecond propagation delays (and I'd prefer 200 nanoseconds, for noise rejection).

That leads to my next point, which is that

when I say "slow" with reference to IC characteristics I don't mean glacial. When you do something in 50 nanoseconds, you're taking less time than it takes a typewriter key to move a quarter the wavelength of light. That's speed, no matter how you cut it. The problem is that what most people really want, if they only realized it, is results, not speed. They want to perform a given job in the shortest amount of time. People who test devices often use the term "productivity." Let me use an example to show that productivity and speed are not the same thing.

Suppose you're testing transistors, many thousands of them a shift, making 10 tests on each one and throwing them into bins on the basis of tests passed. Suppose each test takes 20 milliseconds. You can double productivity by cutting that test time down to 10 milliseconds, right? Wrong.

First, you find yourself bumping into some laws of physics. The transistor needs some time to achieve the desired test state and a measurement made too early might be invalid. Second, at 20 milliseconds a test you are probably already testing transistors faster than your mechanical handlers can operate. Third, you can really increase productivity by working out a test procedure that will eliminate superfluous and redundant tests — in other words, one that will drop the transistor into the right bin with the smallest possible number of tests. This kind of planning can increase productivity by 30 or 40 percent.

Then figure out how to multiplex and timeshare and use distribution curves and yield data to set bin priorities, and you might raise throughput by another 100 percent or so. That's what productivity is all about — not trying to push ICs to their last nanoseconds.

Or, to put the matter in the latest context, consider the problems confronting those who want to test LSI devices. The fastest ICs anyone has dreamed up still fall pitifully short of doing the trick, because now you're involved in making, instead of a few dozen tests per device, n to the nth to the nth of them. Here speed doesn't kill; it simply fails. So again we attack the problem by reducing the number of tests required, through the generation of complex patterns.

Another factor that makes the speed race pretty academic is the amount of time required to program computer-controlled systems. And let's face it, computer control will soon overspread the whole range of electronic instrumentation. Once you enter the computer world, the key limitation isn't imposed by the speed of the magnetic memories, but by the level of complexity that you can tolerate. (Law: All things are as complex as the people involved can tolerate.)

A gang of monkeys sitting at typewriters for 40 years couldn't write the programs for what a computer-controlled test system can now accomplish in half a second. And future generations of test systems will even further outstrip programming ability.

That's the heart of the argument, really. We already have more speed than we know how to use. Our ability to absorb, reduce, and use information is limited not by some DTL gate plodding along at 50 nanoseconds but by the bandwidth of the people operating the system. There's a new paper shredder outside my office. It shreds the paper none of us has time to read, and I have a dark suspicion that it is the paper shredder that ultimately will set the pace for all of us.

Who is Nick DeWolf

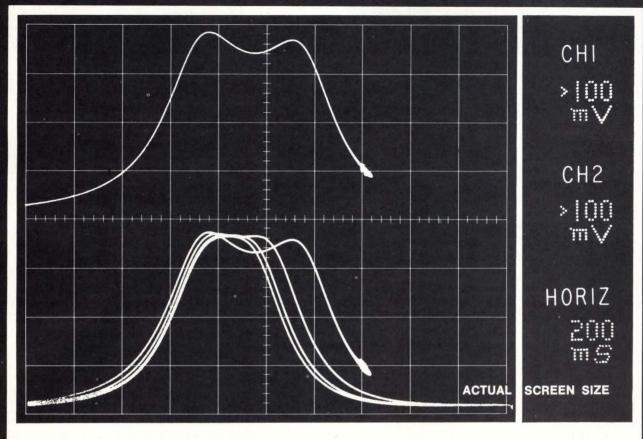
Even his friends feel that Nick DeWolf is a bit of a maverick. The president, director and cofounder of Teradyne just doesn't do things the way most of us would. When he left his job as chief electronics engineer of Transitron 10 years ago (he was the second employee), he didn't just shift into a job that was waiting for him. Instead, he took a year off to think and plan or, to use his own words, "to scheme."

He decided he wanted a partner so, instead of looking for a man with his own background and ideas, he sought one with entirely different experience. He found an old school buddy, Alex d'Arbeloff, who had been involved in South American real estate and who had worked for several companies that folded. This was Nick's way of preparing for lean years — but they never came. Teradyne has been an outstandingly successful manufacturer of equipment for automatic component testing.

Nick is a tall, gangly redhead who punctuates his remarks with frequent laughs, flailing gestures and a variety of sound effects. His family wanted him to be a banker but, as he expresses it, "I'm too skinny and I never played football well enough."

He calls his design philosophy creative pragmatism, which he spells out in terms of building better Mack trucks or doing well known things well. Despite his talk of sticking to "known" things, he's a compulsive inventor and has been since he took his BSEE at MIT in 1948. But he prefers to see himself as an architect. Thus, he didn't "invent" his company's SLOT machine (a Sequential LOgic Tester), he "architectured" it.

Nick, who walks to work (briskly), and his wife Maggie have six little DeWolfs and the biggest milk bill on Beacon Hill. When he's not running Teradyne, Nick is a sometimes (and expert) photographer, an avid skier and a civic leader who specializes in crossing the generation gap.



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Monolithic Ladder Networks-Thick and Thin Film

By Lyle F. Pittroff

During the last few years, monolithic integrated circuits have achieved a well deserved reputation for reliability, circuit density and low cost. Automated testing and refined batch processing have yielded continual improvement in all three

The resistor ladder network, a relatively new breed of packaged circuit, shares many of the attributes of monolithic ICs. And, like ICs, these networks are coming to be treated as "components," rather than as circuits, for the purposes of procurement and specification. Among the major "black-box" specifications. used to characterize ladder networks, are maximum input and reference voltages, output impedance, attenuation accuracy and temperature characteristics.

Two specific methods of ladder-network construction, "thick film" and "thin film," are closely analogous to monolithic IC fabrication. For both film ladder networks and monolithic ICs, fabrication begins with a single wafer of material known as the "substrate." The most common substrate materials for resistor networks include alumina (glazed or unglazed), glass and oxidized silicon. The network of resistors and conductors is securely bonded to the substrate, and, as with monolithic ICs, the complete assembly forms a single, truly monolithic structure. There are no internal solder connections between the functional circuit elements.

Matching and tracking

Both thick and thin films have a common advantage that makes the two techniques well suited for fabrication of ladder networks. With both methods, individual resistors within a network are simultaneously deposited onto the substrate, under precisely the same conditions. Each resistor in the network undergoes the same process, experiences the same environments, and is made from the same batch of materials. Consequently, as one would expect, the characteristics of all the resistors will very closely match and track under a common set of external stimuli.

Actual data taken on production line devices has demonstrated that ratio tracking better than 1 ppm/°C can be realized with both thick- and thin-film construction techniques. However, this order of accuracy is not achieved automatically or simply with either technology. In both cases,

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one must ensure that the "most-significant-bit" (MSB) resistors are physically located close together. And, for optimum tracking, the values of the resistors should be as nearly equal as circuit requirements will allow.

If temperature tracking is the major consideration (and conversion speed can be sacrificed) the standard "R-2R" configuration (Fig. 1) is perhaps the best suited configuration for film ladders. With this configuration, the resistor values have a maximum ratio of two-to-one, and, because values are repeated, the layout can be compact. The resistors which must track each other can be located in close physical and thermal proximity.

Specifying ladder networks

To choose a suitable ladder network for a specific application, the circuit designer must consider every parameter of the ladder that will ultimately affect his system. These parameters normally include the following:

- 1. Attenuation accuracy
 - a) initially at 25°C,
 - b) over the operating temperature range, and,
 - c) over normal operating life.
- 2. Output resistance and tolerance.
- 3. Capacitive and inductive characteristics (since these affect ladder settling).
- 4. Mechanical characteristics.
- 5. Environmental characteristics.
- 6. Packaging requirements.
- 7. Cost and availability.

Unfortunately, not all manufacturers define accuracy the same way. One type of accuracy specification consists of an absolute tolerance spec together with temperature-coefficient tracking specs. Another approach is to specify the "ladder attenuation ratio" over a specified (and tested) temperature range. In this case the ladder is tested by the manufacturer over the specified temperature range and worst-case error sums are measured.

Note that, whichever process is used to build a ladder, the ultimate objective is the same; to achieve an overall digital-to-analog (or analog-to-digital) conversion accuracy of some stated percentage, over a specified temperature range. In most cases an error budget is established so that various error sources can be evaluated. A typical digital-to-analog converter (DAC) configuration is shown in Fig. 2, and its error budget is shown in Table 1. The final choice of a suitable ladder usually results from some compromise between dollar savings and accuracy. In some special situations, the packaging

configuration, also, may be a deciding factor.

Both the film-material characteristics and manufacturing-process tolerances contribute to the inaccuracies of film ladder networks. Although thick- and thin-film ladder networks can have similar performance, their raw ingredients and manufacturing processes are quite different.

Thick-film processing

The typical thick-film ladder network begins with an unglazed 96-percent alumina (Al₂O₂) substrate. Thick-film materials are then screened onto the substrate surface. The process is completely analogous to the conventional silkscreen printing process used for posters, etc., except that the "silk" is replaced by a fine mesh stainless steel. Most of the holes in the screen mesh are blocked out by a photographic emulsion. Holes are left open in the areas where material is to be printed onto the substrate surface. Separate screens are used for the conductor and resistor areas. The prescribed firing-temperature profiles for the various cermet materials determine the actual screening sequence; the material with the highest firing temperature is screened first, followed by the next highest. etc.

Thick-film cermet materials are made by mixing powders of various noble metal and glass combinations. Organic vehicles and binders are added to give the liquid film (also called paste or ink) the necessary viscosity for proper screening. The liquids "dry" out of the film after screening and the organic binders are burned out during the firing process. The finished resistor consists of the metal particles spread uniformly throughout and fused into the glass, thus becoming a permanent part of the overall ceramic structure.

Thick-film resistors are normally between 0.5 and 1.5 mils thick. Because fired thick-film ladders are rugged glass/ceramic structures, they are extremely resistant to physical abrasion and damage. Consequently, parts can safely be stacked for automated handling during manufacture.

The initial tolerance of thick-film resistors after firing is normally ± 20 percent. Though it is possible to screen and fire to tighter tolerances, this is rarely done in quantity production. In the case of the ladder networks, where voltage ratio tolerances better than 0.01% are required, it certainly would not be practical to fire to the required tolerance. The usual method is to adjust the resistor to the desired tolerance by laser tailoring, air-abrasive techniques, or a

combination of the two methods.

For ladder networks, resistor tailoring is normally a two-step process. Since the removal of resistor material increases the resistor value, and since the "as-fired" resistor can have a tolerance of ±20 percent, the screening artwork is designed to produce a resistance 20-percent lower than the final value required. A first adjustment brings the resistor value into a narrower tolerance range (±1%), after which a much more precise second adjustment is made while monitoring a resistance ratio or voltage ratio.

Thick-film ladder network accuracies to $\pm \frac{1}{2}$ LSB in twelve bits ($\pm 0.0122\%$ or ± 122 ppm relative to full scale), over the range -55°C to +125°C, are being achieved regularly on a production basis, even though the absolute temperature coefficient of resistance (TCR or tempco) may be as large as 350ppm/°C. Again, the emphasis is on the functional characteristics of the network and not the individual resistor. The combination of nearly identical temperature coefficients from resistor to resistor, and the high thermal conductivity of the alumina substrate (which acts to keep the entire network at the same operating temperature), permits precision performance in spite of the absolute-tempco magnitude.

Some applications require that feedback-scaling resistors track the temperature characteristics of the ladder network. Thick-film ladder manufacturers can accommodate these requirements by including "application" resistors on the ladder network substrate. These resistors should be located physically close to the MSB resistors, thereby providing close temperature tracking with the resistors that play the biggest part in determining the network's accuracy.

Thin-film processing

The thin-film process uses entirely different deposition techniques. Actual film thickness is in the range of 0.4 to 20.0 micro-inches; or as much as one-hundred times thinner than "thick" film.

Necessarily, the substrate surface must be much smoother for thin films. Whereas unglazed alumina is used for thick film networks, a glazed version of the same substrate is often used for thin film deposition. Glass and silicondioxide substrates also find wide usage in thinfilm ladder networks since high power dissipation is not a requirement.

Thin-film resistors and conductors are deposited onto the substrate surface in a vacuum or inert gas environment. Vacuum evaporation and sputtering are currently the most common deposition techniques. Nickel-chromium (nichrome), tantalum-nitride and chromium-cobalt head the list of resistive films, with aluminum and gold being used for the interconnecting conductors. Each of the deposition processes involves coating the entire substrate surface with a thin uniform layer of film, and then selectively etching

away the film in unwanted areas.

As with the thick-film network, all of the thin-film resistors are deposited simultaneously from the same batch of material, and, consequently, exhibit excellent tempco tracking characteristics. Also, since the thin-film resistors consist primarily of metal alloys, their absolute temperature coefficient is much lower than that of thick-film materials. Currently advertised tempco limits for precision thin-film networks are around $\pm 50 \mathrm{ppm/^\circ C}$ to $\pm 25 \mathrm{ppm/^\circ C}$.

Trimming techniques

Thin-film and thick-film resistor adjustment methods are quite different. This results, indirectly, from the widely different resistivities of the two categories of film materials. Resistivities of thick-film materials can be altered to achieve a small aspect ratio at any of the resistance levels widely encountered in ladder network applications (5 k Ω to 100 k Ω); the minimum resistor size, therefore is limited by screening resolution. Consequently, thick-film resistor adjustment is most easily accomplished by cutting directly into the side of the printed material. This decreases the effective width of the resistor, thus increasing the length-to-width aspect ratio and the resistance.

Thin films, by contrast, have a more restricted resistivity range; therefore they rely on fine line resolution and large-aspect-ratio serpentine patterns to achieve high resistor values. Since cutting into the side of a one-mil line is out of the question, other production-line techniques have been developed. Anodization is commonly used to increase the resistance of tantalumnitride resistors by converting the resistor surface into an insulating oxide. Anodization of thin film resistors is somewhat analogous to the first adjustment described earlier for thick-film networks. Because all of the resistors are anodized simultaneously, individual adjustment is not possible at this stage. Therefore as with thick-film networks, resistors must be adjusted individually, in a final operation, to trim the exact ratio.

The most common methods of adjustment for individual thin-film resistors are shown in Fig. 3 and Fig. 4. In Fig. 3, some of the serpentine loops have been shorted out by shorting links of resistive film. The overall resistor value can be increased by cutting through a shorting link with a laser beam, or by an etching process, or by a hand scribing technique. The resolution of the adjustment is determined by the amount of resistance originally shorted by the link. Another variation of this technique is shown in Fig. 4. This approach allows finer trimming resolution and a slightly smaller substrate for a given circuit requirement. But it also requires a little more finesse during the trimming procedure.

D/A conversion with ladders

The ladder network can be regarded as a

Table 1: Typical Error Budget for Digital-to-Analog Converter

Error Source	Initial Tol. (+25°C)	Temperature Coefficient	
Switching errors without dynamic compen- sation trimming)	±2.5 mV	(included in initial tolerance)	
Reference errors $(V_{ref} = 10 \text{ Volts})$	±0.5 mV	±200 μV/°C	
Op-amp voltage offset	(preset to zero)	±5 μV/°C	
Op-amp current offset $(\Delta i \times R)$	(preset to zero)	±10 μV/°C	
Feedback scaling error	±1 mV	±10 μV/°C	
Ladder Network error (R = 10 k Ω)	±1 mV	±10 μV/°C	
Total error	±5 mV	±235 μV/°C	

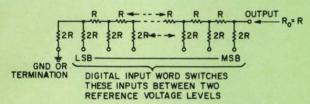


Fig. 1. Binary "R-2R" ladder network

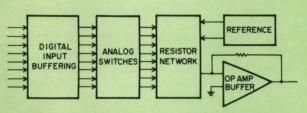


Fig. 2. Digital-to-analog converter

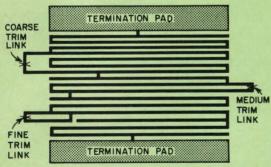


Fig. 3. Thin-film resistor trimming by opening shorting links.

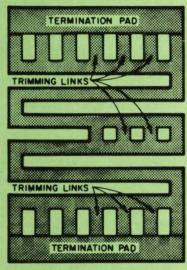


Fig. 4 Alternative geometry for thin-film resistor.

special-case attenuator, in that the several inputs can be used simultaneously in any combination (up to 2^n combinations where n is the number of bits). The output contribution of each bit remains the same regardless of the input condition of the other bits, and, by design, each of the bits provides a different output contribution or "weighting." Various output levels are established by "turning on" various combinations of bits. Semiconductor switches or relay contacts switch the input terminals to specific reference-voltage levels in response to a digital input "word." A slightly different approach is used with some "ladder" configurations that operate on a "current-steering" basis. With these networks, the input terminations are driven from current sources instead of voltage sources.

Since the ladder network is basically a proportioning device, it is conventional to describe the network accuracy in terms of its ability to correctly attenuate the reference voltage, which can be applied to any combination of input terminals. The measured difference between the actual output and the theoretical output is normally expressed as a percentage of the reference voltage or "full-scale" output voltage.

Most ladder-network specifications correlate the percentage inaccuracy with the percentage of full scale represented by the network's smallest bit weight. For example, a three-bit binary-weighted ladder network has an MSB which, alone, can cause the output to rise to 50 percent of the full-scale input voltage. The second bit can contribute an output weighting of 25 percent and the third bit (LSB) can contribute 12.5 percent. If the individual resistor errors are small enough, so that no input combination can cause an output error greater than ± 6.25 percent of the full scale output voltage, the network is said to be accurate within $\pm \frac{1}{2}$ LSB.

It follows that a four-bit binary ladder accuracy would have to be better than ± 3.125 percent to meet the $\pm \frac{1}{2}LSB$ spec, and a five-bit ladder better than ± 1.5625 percent, etc. The accuracy specification is cut in half each time the resolution is doubled. For a twelve-bit network, $\pm \frac{1}{2}LSB$ equals ± 0.0122 percent, but these accuracy levels are more commonly stated in "parts per million" (± 122 ppm in this case) instead of in percent (parts per hundred).

An earlier look at the "R-2R" binary configuration (Fig. 1) indicated that this network is well suited for thick- and thin-film fabrication because all the resistors are of similar value. Also, this type of network is a good example for analysis, because its attenuation characteristics are easily visualized. Normally, a single reference voltage is applied at each of the bit switches, and one can readily see that an LSB input will cause only a small change at the output terminal. The theoretical LSB increment for a 12-bit network is 0.0244 percent of the reference.

An important manufacturing consideration is

that as the network attenuates the voltage, it also attenuates the effect of individual resistor errors. For example, a one-percent absolute error in the LSB 2R resistor of an otherwise perfect twelve-bit network would cause an output voltage error less than 0.0002 percent. This implies that the LSB resistors in thick- and thinfilm ladder networks can merely be adjusted to absolute tolerances, and only the more-significant bits require sophisticated ratio adjustments since their error effects receive less attenuation. This general principle applies to other binary ladder-network configurations, as well as to BCD networks and networks with other coding formats.

Errors caused by the MSB must be less than the total contribution of the less-significant bits, if the smaller bits are to have any significance at all. If the total summation of worst-case bit errors never exceeds $\frac{1}{2}$ LSB, the network is said to be "monotonic," and its output response to consecutive input counting from all zeros to all ones would always change in an increasing direction without down-stepping. In order to be monotonic, a twelve-bit binary ladder must proportion the reference voltage within ± 122 ppm over the anticipated operating temperature range.

Thick versus thin

In high-speed conversion systems, dynamic characteristics of the ladder become significant in addition to the static characteristics described previously. Both thick- and thin-film networks, however, usually have inter-element capacitances and inductances much lower than those of the associated circuitry. Consequently, neither the thick-film ladder nor the thin-film ladder has a clear-cut advantage based on settling characteristics.

A nose-to-nose comparison of thick- and thinfilm ladder networks is not as one sided as some people have claimed. The most common requirements for resistance range, attenuation accuracy over temperature, mechanical configuration and settling characteristics are within the capabilities of both technologies. There are, however, two areas where specific advantages can be realized. In these areas, each process gets one vote.

Thin films inherently have lower absolute temperature coefficients. This gives them a definite advantage in certain applications. Thinfilm materials rely almost entirely on the metallic conduction mechanisms of low-resistivity metal alloys, whereas thick-film materials depend on additional conduction mechanisms — which allow higher resistivities but which also cause higher absolute temperature coefficient.

Thick films, however, have the advantage that manufacturing costs (and, hence, selling price) are lower than for thin films. This is because the physically wider and more rugged resistors produced by thick-film techniques are more suitable for automated production processing. **EEE**

clip transients...

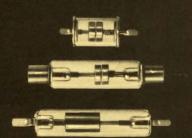


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Part Three August, 1970 Selecting and Applying Semiconductor Memories

MOS Read-Only Memories

The first MOS read-only memory available was small (256 bits), slow (2 μ s access time) and was scarcely capable of performing any function that could not be done better, faster and cheaper in some other way. But progress has been steady and MOS read-only memories can now be purchased in configurations providing speeds as fast as 750 ns, with capacities as large as 4096 bits and at a cost that cannot be approached by any other technology. These read-only memories are being delivered in volume. Each one is easily programmable to any fixed storage pattern that the user desires.

What is a read-only memory?

A read-only memory is a circuit which can take a digital code at its input terminals and provide a unique digital code on its output terminals. The relationship between the input and output codes is fixed and is usually alterable only by replacing all or part of the circuitry. The only difference between a read-only memory and a read-write memory is the level of difficulty required to change the stored information.

Most read-only memories are also random-access memories which means simply that all stored information is accessable in a fixed amount of time. It has been common practice (at least in the USA) to refer to random-access read-write memories simply as random-access memories. This is an oversimplification that will become obvious with the increasing use of the random-access read-only memory.

Read-only memories are not new although their usage in the past has been rather limited. The most common form of read-only memory is the diode matrix which has been used since the early days of diode production. More recently the transformer type of read-only memory has found its way into microprogrammed digital processors. MOS read-only memories will replace some of the present forms in those applications where its costs and size advantages are significant; more often, however, the MOS read-only

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by Michael R. McCoy

memory will create new applications which were not feasible prior to its development.

The MOS read-only memory

MOS technology is ideal for the fabrication of read-only memories. The high density attained in the memory matrix cannot be achieved by any other present technology. In addition, the circuitry required for address decoding and input-output buffering can be included on the same substrate containing the memory matrix. The result is a very dense, low-cost array that can be easily used. A block diagram for an MOS read-only memory is shown in Fig. 1. The memory illustrated is organized as a 16-word, 2-bits per word read-only memory. Such a configuration is too small for economical production but its simplified structure makes it easier to explain circuit operation.

The basic storage element of the MOS readonly memory is the MOS transistor. The memory matrix of Fig. 1 has 32 possible transistor locations; hence it can be coded with 32 bits of information. To code a logic "1" in a particular cell, the designer specifies that a transistor be located in that position. To specify a logic "0" in a cell, no transistor is inserted. Insertion or deletion of a transistor in the matrix can be accomplished by changing a single photomask that is used in the MOS fabrication process.

Because it is desirable to keep the number of circuit inputs to a minimum, almost all available MOS read-only memories have full address decoding on the same substrate as the memory matrix. Note that in Fig. 1 a coincidence select technique is used to address a particular cell. This technique is used for two reasons: the length/width ratio of the memory matrix is more manageable and three two-level decoder circuits require less circuitry and therefore, are less costly than one four-level decoder.

In the illustration of Fig. 1, the "Y" select circuits fully decode the two "Y" addresses (Y_{A1} and Y_{A2}) into four "Y" cell select lines 1, 2, 3, 4. There are two identical "Y" select circuits: one for each bit of the two-bit word. The single "X" decoder provides a select signal on one of its four outputs. Readout of a particular cell

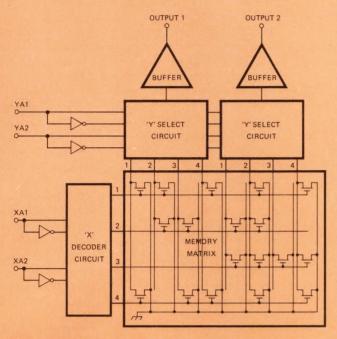


Fig. 1. Block diagram of a 16 word by 2 bits per word MOS read-only memory. A logic "1" in a cell is represented by a transistor at the intersection of the decoded X and Y address lines.

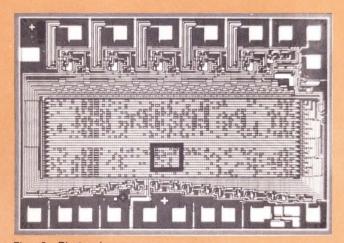
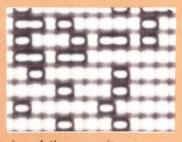


Fig. 2. Photomicrograph of the EA 3501, a 512 by 5 MOS read-only memory, which is coded as an ASCII to 5 × 7 dot matrix character generator. A portion of the memory matrix is enlarged to show the memory cells in more detail. The



size of the array is 69 x 94 mils.

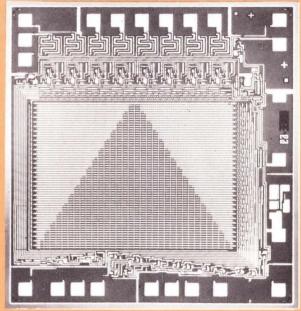


Fig. 3. Photomicrograph of the EA 3300, a 4096 bit MOS read-only memory in a 512×8 configuration. The triangular pattern in the memory matrix results from the use of a memory pattern to characterize worst case access time. The die measures 88×94 mils.

in the array is accomplished by sensing for current flow in the cell at the intersection of the selected "X" and "Y" lines. In the illustration of Fig. 1, two cells are always accessed simultaneously because of the two-bit word.

There are two different circuit techniques that can be used in the design of the decoder and buffer circuits-dc (unclocked, asynchronous) and dynamic (clocked, synchronous). While the dc circuits are in some cases easier to use because of the lack of a requirement for clock pulses to activate the array, the dynamic circuits are smaller which results in lower cost, faster access and synchronous operation. The synchronous nature allows use in sequential applications such as counters and sequence generators where a dc circuit cannot be used without the addition of external storage registers.

A photomicrograph of a 2560-bit read-only memory is shown in Fig. 2. A section of the memory matrix is expanded so that a bit cell can be clearly identified. The signal lines of the matrix provide all the essential components for the MOS transistors that they interconnect. The decoded "X" address line serves as the gate electrode, the decoded "Y" select line functions as the diffused ground return is the source electrode.

A photomicrograph of a 4096-bit MOS readonly memory is shown in Fig. 3. In mid-1970 this represents the largest single-chip memory in production. The triangular pattern in the memory matrix is a test configuration used to characterize for worst-case access time. The functional nature of the various sections of the array are shown in Fig. 4.

The custom bit pattern

One of the processes used to produce custom bit pattern read-only memories is shown in Fig. 5. Typically, the first step in the process is completion of the customer coding sheet. This coding sheet specifies the input-output correspondence required of the custom read-only memory. The coding sheet is transferred to a computer center which provides the three separate outputs shown. A relisting of the input data is returned to the customer for verification. This verification step insures that the data the computer used to generate the plot and test tapes is correct. The plot output is a scale drawing created by an automatic plotter showing the location of each transistor to be inserted in the memory matrix. The test tapes are also computer generated and consist of a punched paper tape that is used to directly load automated test equipment with the custom read-only memory outputs in order to perform a full functional test.

The next step in the process is fabrication of a custom mask. The plot output is used in conjunction with a master, typically 400X artwork, to create an image of the photographic mask with the customized memory matrix. This artwork is then photoreduced and stepped into an array of images for use in wafer fabrication.

Silicon wafers, containing an array of read-only memories, are then fabricated in the normal manner using the custom mask.

In order to avoid packaging circuits that are nonfunctional, each read-only memory on the wafer should be tested prior to packaging, using the test tapes produced at the computer center. Nonfunctional or marginal circuits can be marked and eliminated before packaging. The tested dice are then packaged, tested again and forwarded to the customer.

The whole process requires between six and eight weeks. Every effort should be taken to reduce the probability of an error. The customer can be given an opportunity to check an output of the computer generated at the same time that the plotter output and test tapes to be used in fabrication are generated. Provided the customer does a careful job of verification, the only reasonable possibility of error is in the mask fabrication process. Even if an error were to occur in the preparation of masks, the error should be caught at an intermediate stage when the wafers are first tested, thus keeping the loss of time to a minimum.

Applications for the MOS read-only memory

The applications of MOS read-only memories are numerous with new uses being discovered at an accelerating rate. Almost all new character generators are being designed using MOS read-only memories to convert the digital character code to a screen code for dot matrix characters. Another exciting application is in the fixed storage required for a micro-programmed digital processor. All forms of code converters are prime candidates for implementation as read-only memories.

The use of the MOS read-only memory in the character generator of an alpha-numeric display system is shown in Fig. 6. Here, the read-only memory converts the digitally coded alpha-numeric representations in the data store into a dot-matrix code that visually represents the character. For simplification in describing the function of the system let us assume that all we are going to display on the CRT face is the three character set shown.

During the first sweep (line 0), three lines from the sync and timing generator indicate to the read-only memory that line 0 is being displayed. As long as the line 0 code remains at the read-only memory inputs, no dot pattern will be displayed as line 0 corresponds to the vertical space between characters. After the line 0 sweep is completed, the line 1 sweep is started. The first character code (A) is clocked into the ROM from the refresh memory and in conjunction with the line 1 code from the sync and timing generator causes a 00100 to appear on the read-only memory outputs. As the sweep generator causes the electron beam to sweep across the CRT face, the 00100 code from the read-only memory is shifted into the CRT blanking circuit causing a single

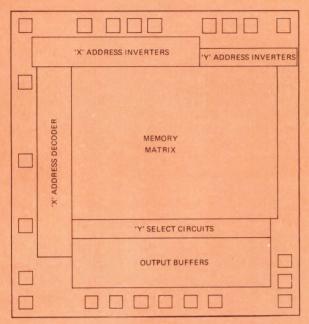


Fig. 4. Block diagram of the 4096-bit EA 3300 showing the location of the various components of the array. Refer to Fig. 3 for comparison with a photomicrograph of the array.

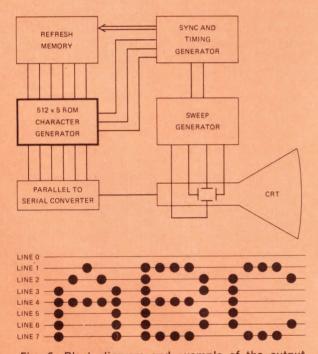
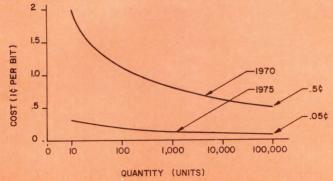


Fig. 6. Block diagram and example of the output pattern of a dot matrix character generator. The single ROM chip shown in Fig. 2 is designed to perform the function of the ROM illustrated above.



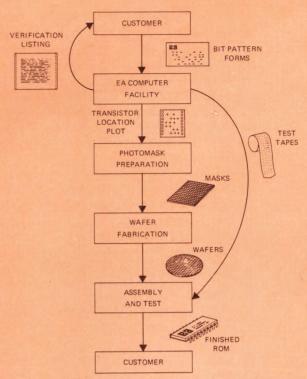


Fig. 5. The custom bit pattern ROM fabrication process. Time required from start to finish is six to eight weeks.

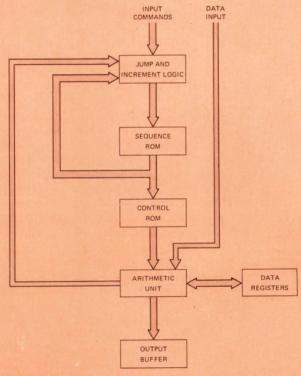


Fig. 7. Functional flow diagram of a microprogrammed digital processor. Microprogrammed digital processors are more flexible and often much less expensive to produce than an equivalent "hard logic" system.

Fig. 8. Present and projected 1975 cost per bit for a 4096-bit MOS read-only memory.

dot to occur on the CRT face in the middle of the line 1 position of the first character field.

Next, a new character (B) is shifted into the character code inputs of the read-only memory causing a 01111 code to appear on the read-only memory outputs. The code is then shifted into the blanking circuitry causing four dots in the first four dot locations of line 1 in the second character field. After the line 1 dot code for the third character is written, horizontal sweep return is initiated to start line 2.

The same three character codes will be sequenced into the read-only memory, but the new line code will cause dot representations appropriate for line 2 of the character field. This process is continued through line 7 when vertical sweep return occurs and starts another cycle.

The standard, off the shelf, 512 by 5 read-only memory shown in Fig. 2 contains a memory pattern that converts a 6-bit ASCII code and a 3 bit line code into 64.5×7 dot matrix characters of the form shown in Fig. 6. Changes in either the input code or the output code can be implemented with a custom bit pattern. The IC in Fig. 6 is the EA 3501 which is capable of operating at 1.3 MHz. To operate at higher rates, two 3501 units can be multiplexed. More complex dot patterns and more characters can be added by using more than one read-only memory.

A simplified block diagram of a microprogrammed digital processor is shown in Fig. 7. The processor contains two read-only memories. One is the sequence read-only memory, which is essentially a sophisticated counter; and the other is the control read-only memory, which converts the sequence state into control commands for the arithmetic unit. In general, the processor operation is as follows: First, an input command forces the sequence read-only memory into a particular initial state. The control read-only memory interprets the state and causes the arithmetic unit to perform an operation. The jump-and-increment logic detects when the sequence state is to be changed and initiates such action. The new sequence state is again interpreted by the control read-only memory and new commands are given to the aritmetic unit.

A processor of this type has many advantages. The arithmetic unit is simplified since the number of basic operations it must perform is limited. Having sequence and control logic implemented in read-only memories offers great flexibility. New operations can be added and design changes made simply by changing the memory pattern leaving the mechanical construction of the system completely intact. The cost of the system is reduced since the sequence and control read-only memories replace a great deal of logic. Many different functions could be performed by the same basic processor. The data registers and output buffer could be changed to fit the application with the basic processor left intact.

Another major application area for read-only memories is code converters and function generators. Many major manufacturers of digital equipment use their own unique character codes. A read-only memory can easily be used to convert one code to another. Two common character codes in use in the USA today are the American Standard (ASCII) and the code used in the IBM Selectric Typewriter. ICs are available, such as the EA 3101, which convert ASCII code to Selectric code or Selectric to ASCII depending on the state of one of its address inputs. A Sine ϕ generator is easily implemented with a read-only memory. An 8-bit Sine generator could be implemented with a single 2048-bit read-only memory. An eight-bit representation of ϕ could be applied to the inputs with a resulting 8-bit representation of Sine ϕ occurring on the device outputs.

Read-only memories can perform logic and counting functions as well. Any logic circuit with n inputs and m outputs can be replaced by a read-only memory with n inputs and m outputs. Any counter sequencer with n inputs and m flip-flops can be replaced by a sequential read-only memory with n + m inputs and m outputs. Since any digital system can be constructed as logic and counters/sequencers, it is easily seen that any digital system can be completely constructed of read-only memories. The question thus becomes not one of whether a read-only memory can be used, but whether it is the most economical approach and whether it can best meet the performance objectives.

Judging MOS read-only memory performance

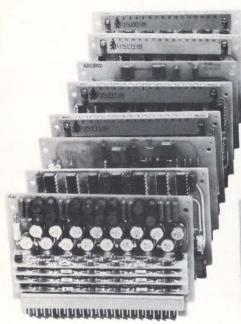
Selection of a technology usually involves a weighted analysis of the following factors: (1) Cost (present and projected), (2) Performance, (3) Physical size, and (4) Reliability.

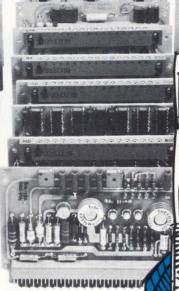
The approximate cost of a 4096-bit MOS readonly memory in 1970 and 1975 is depicted in Fig. 8. Note the strong influence of quantity. Circuits with lower bit capacities than this one will be priced slightly higher per bit.

The performance of MOS read-only memories is usually judged in terms of access time and power dissipation. The power dissipations of dc and dynamic type read-only memories are far apart. A dynamic unit consumes on the order of 50 mW where dc versions dissipate up to 500 mW. Current access time limits vary from 1.5 μ s to 750 ns guaranteed over full voltage and temperature ranges.

The future for MOS read-only memories

Crystal ball gazing is always a risky business, but the following should be achieved by 1975: (1) single chip memories as large as 16,000 bits, (2) access times less than 300 ns., (3) memory alterations accomplished in less than two weeks, (4) a wide variety of configurations to choose from, (5) high density multichip packages providing assemblies over 64,000 bits, and (6) several hundred off-the-shelf MOS read-only memories precoded with commonly required memory patterns.





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Op Amps or Instrumentation Amplifiers? by Tom Cate

Both can be used as signal conditioners. Which should you use? What are the design tradeoffs?

An ideal signal-conditioning amplifier would have high input impedance, accurate differential gain, good common-mode rejection and low output impedance. In addition, high gain is often needed to amplify the signal. Engineers have frequently used operational amplifiers for their signal-conditioning needs. As circuit requirements have become more stringent, though, it has become necessary to choose between op amps with carefully-trimmed summing networks and off-the-shelf modular instrumentation amplifiers. The choice is made difficult by differences in specification terminology between the operational-amplifier world and the instrumentation-amplifier world.

Fundamentally, an op amp is specified as an open-loop device to which must be added precision external resistors that set its operating characteristics as a gain block. An instrumentation amplifier contains its own resistor network, and its performance as a gain block is completely specified by the manufacturer.

To illustrate the design and performance differences between the two types of amplifiers, their characteristics will be discussed separately. Then we'll put them both in the same circuit and compare.

Ideal differential op amp

If we first assume an ideal op amp (see Fig. 1a), then no current will flow into the input and the differential voltage between the input terminals will be zero. This leads to

$$\frac{R_{0}}{R_{0} + R_{I}} E_{z} - \frac{R_{0}}{R_{0} + R_{I}} E_{I} = \frac{R_{I}}{R_{0} + R_{I}} E_{0}$$

$$E_{0} = \frac{R_{0}}{R_{I}} (E_{z} - E_{I}) = -\frac{R_{0}}{R_{I}} E_{z} \qquad (1)$$

Since there's zero volts between the input terminals, the differential input impedance is simply $2R_1$. The common-mode input impedance is $(R_\theta +$

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 R_1)/2. So, with an ideal op amp and the resistors perfectly matched, we have (see Fig. 2)

$$Z_d = 2R_t; Z_{cm} = \frac{R_0 + R_t}{2}; E_0 = \frac{R_0}{R_t} E_s$$
 (2)

For a real op amp, errors occur from both the external resistor network and the limitations of the op amp itself. First, consider what happens if the summing-network resistors each have some ΔR as shown in Fig. 3.

In an ideal amp, there is no input current and no differential voltage across the input terminals. The output will then be given by

$$E_0 = \frac{R_s}{R_t} \frac{R_t + R_o}{R_z + R_s} E_z - \frac{R_o}{R_t} E_t \tag{3}$$

where $R_0 + \Delta R_0$, $R_1 + \Delta R_1$, $R_2 + \Delta R_2$ and $R_3 + \Delta R_3$ should be substituted for R_0 , R_1 , R_2 and R_3 , respectively. This rather cumbersome expression can be put into a more useful form by breaking it up into differential and common-mode portions. This is done by defining the common-mode input (E_{cm}) to be

$$E_{cm} = \frac{E_1 + E_2}{2} \tag{4}$$

For signal conditioning, we want the amplifier to accurately amplify the differential signal E_s and to reject E_{cm} .

We define E_s as : $E_s = E_{\it 1} - E_{\it 2}$. The output $E_{\it 0}$ in terms of E_s and $E_{\it cm}$ is

$$E_{0} = \frac{R_{s}}{R_{z}} \left[\frac{1 - \frac{R_{o}R_{z}}{R_{I}R_{s}}}{1 + \frac{R_{s}}{R_{z}}} \right] E_{cm}$$

$$- \frac{R_{s}}{R_{z}} \left[\frac{\frac{R_{o}}{R_{I}} + \frac{1}{2} \left(1 + \frac{R_{o}R_{z}}{R_{I}R_{s}} \right)}{1 + \frac{R_{s}}{R_{z}}} \right] E_{s}$$
 (5)

where again, each R_n represents $R_n + \Delta R_n$. Making $R_0 = R_3$ and $R_1 = R_2$ will provide the desired rejection of the common-mode input E_{cm} . The differential gain will be R_0/R_1 .

If the ΔR 's are fairly small and if the differential gain (determined by R_θ/R_I and R_3/R_2) is large, then the common-mode gain can be approximated by

$$\frac{E_{o}}{E_{cm}} \approx 1 - \frac{\left(1 + \frac{\Delta R_{o}}{R_{o}}\right) \left(1 + \frac{\Delta R_{z}}{R_{z}}\right)}{\left(1 + \frac{\Delta R_{t}}{R_{t}}\right) \left(1 + \frac{\Delta R_{s}}{R_{s}}\right)} \tag{6}$$

If all the resistors are within $\pm 0.1\%$ of their nominal value, the common-mode "gain" can be as large as

$$\left(\frac{E_o}{E_{cm}}\right)_{max} \approx 0.004$$

The resistor tolerances affect both gain accuracy and common-mode rejection. You can trim one resistor pair or the other, but the adjustments interact. If the resistors are matched such that $\Delta R_0 = \Delta R_s$, and $\Delta R_1 = \Delta R_s$, then the common-mode error term drops out and the output is

$$E_0 = \frac{R_0 + \Delta R_0}{R_1 + \Delta R_1} (E_2 - E_1)$$

where

$$\Delta R_0 = \Delta R_3$$
 $\Delta R_1 = \Delta R_2$ and
$$\begin{cases} R_0 = R_3 \\ R_1 = R_2 \end{cases}$$

CMRR is the ratio of differential gain to common-mode gain. With resistor accuracies of $\pm 0.1\%$

$$CMRR \approx \frac{R_0/R_1}{0.004} = 250 \ R_0/R_1$$

The gain-accuracy expression is rather complex, but it is reasonable to expect gain accuracies of about $\pm 0.2\%$ when using 0.1% resistors.

Limitations of real op amps

The preceding assumed an ideal amplifier. However, there are three main limitations of real op amps:

1. The open-loop gain of the amplifier must be at least 30 to 40 dB greater than the closed-loop gain (R_{θ}/R_{I}) to ensure good gain linearity and gain stability. For example, a required closed-loop gain of 1000 would rule against the use of some of the very-low-cost IC op amps which have typical gains of only 70 to 80 dB.

2. The desired input impedance $(Z_{cm} \text{ and } Z_d)$ will determine the required value of R_I . Then the desired closed-loop gain (R_0/R_I) will determine R_0 . The op-amp differential offset current flowing through the external input and feedback network will cause offset and drift. Different op-amp types vary considerably in differential-input offset currents; a range of 0.01 nA to 100 nA is readily available.

For the op-amp circuit of Fig. 1a, the incremental output ΔE_o due to a differential offset current I_d is simply $R_o I_d$. Remember, the input offset current I_d varies

Remember, the input offset current I_d varies with temperature. Thus, offset-current drift shows up as voltage drift. Some typical numbers for an IC op amp are: maximum I_d of ± 60 nA at 25°C and drift of ± 0.4 nA/°C. If R_θ is 10 M Ω , then the offset ΔE_θ over the temperature range "T" will be

$$\Delta E_o = 10 \text{ M}\Omega \times 60 \text{ nA} + 10 \text{ M}\Omega \times 0.4 \text{ nA/°C} \times T$$

$$= \pm 0.6 \text{ V} \pm 0.004 \text{ V/°C} \times T$$

Using a FET-input op amp will greatly reduce the errors due to current offsets, but at the penalty of increased circuit cost.

3. The common-mode rejection of the op amp is also important. We have already discussed how imbalance in the external input and feedback network could allow some of the common-mode input to get through. But even if the external impedance network is perfect, there will still be some feed-through of the common-mode signal due to finite common-mode rejection of the op amp. With everything else but CMR perfect, the output of the op-amp circuit of Fig. 1a is

$$E_{0} = -\frac{R_{0}}{R_{I}} E_{\bullet} + \frac{R_{0}}{R_{I}} \left(\frac{R_{0}}{R_{0} + R_{I}}\right) \left(\frac{1}{CMRR}\right) E_{\bullet}$$
(8)

where CMRR is the common-mode rejection ratio. By convention, $CMR = 20 \log |CMRR|$.

Most op amps have CMR of at least 60 dB. The commonly available $\pm 10~{
m V}$ op amps have the restriction that

$$\left|rac{R_o}{R_o+R_1}\,E_{m{z}}
ight|< 10\;\mathrm{V}$$

As a typical situation, let's look at an op amp with 60-dB CMR, connected for a gain of 100. Then

Error Term from Op Amp CMR

=
$$100 \left(\frac{100}{101}\right) \left(\frac{1}{1000}\right) E_{z}$$

 $\approx 0.1 E_{z}$

This is a rather large error, so we might well have to use an op amp with better CMR in this application. Discrete op amps with bipolar inputs typically have CMR of over 80 dB.

Other factors also contribute error, but the three factors discussed here will generally guide you into the proper type of op amp. Some of these requirements conflict — a FET-input op amp will minimize errors due to offset currents, but the CMRR of inexpensive FET op amps is poor. Bipolar-input units offer lower voltage drifts for a given price, but their offset currents may be too high. IC op amps offer very low cost, but their performance will limit accuracy.

Up to this point, we have discussed each error source separately. At first glance, it might seem that CMR could be made infinite by deliberately trimming the resistor network to compensate for the op-amp gain unbalance. This can provide another 20 dB or so of CMR, but some op amps, particularly low-cost FET-input units, have very nonlinear CMR.

The analysis so far has assumed that the open-loop differential gain and the open-loop common-mode gain of the op amp are both linear. This assumption is not necessarily valid for low-cost ICs or low-cost FET-input units, though it is generally valid enough for discrete bipolar-input units. Any external compensating done to improve

CMR will be limited in effectivenesss by the nonlinearity and temperature stability of the op amp's CMR.

Ideal instrumentation diff amp

There are many types of instrumentation-amplifier circuits, but the circuit of Fig. 1b is perhaps one of the most popular. It can be designed and built by the instrumentation engineer or it can be purchased as a complete packaged module. The input ICs are selected matched pairs; this greatly minimizes the differential voltage drift. The output stage is an op amp connected for unity differential gain. Let's first take a look at the input stage of the instrumentation amplifier (see Fig. 4).

Assuming ideal op amps, we can write

$$E_{s} = \frac{R_{s} + \Delta R_{s}}{R_{I} + R_{s} + \Delta R_{s}} E_{I} + \frac{R_{I}}{R_{I} + R_{s} + \Delta R_{s}} E_{os}$$

$$E_{I} = \frac{R_{o} + \Delta R_{o}}{R_{I} + R_{o} + \Delta R_{o}} E_{s} + \frac{R_{I}}{R_{I} + R_{o} + \Delta R_{o}} E_{ot}$$

$$E_{os} = \frac{R_{I} + R_{s} + \Delta R_{s}}{R_{I}} E_{s} - \frac{R_{s} + \Delta R_{s}}{R_{I}} E_{I}$$

$$E_{oI} = \frac{R_{I} + R_{o} + \Delta R_{o}}{R_{I}} E_{I} - \frac{R_{o} + \Delta R_{o}}{R_{I}} E_{s}$$

If we make $R_{\theta} = R_{\beta}$, then the differential output will be

$$E_{0I}-E_{0ar{z}}= \overbrace{\left(1+2rac{R_{o}}{R_{I}}
ight)\left(E_{I}-E_{ar{z}}
ight)}^{ ext{Ideal Output}} \ + rac{(\Delta R_{I}-\Delta R_{ar{z}})}{R_{I}}\left(E_{I}-E_{ar{z}}
ight)$$

The output stage of the instrumentation amplifier of Fig. 1 is a unity-gain difference amplifier, so the output of the instrumentation amplifier (assuming ΔR 's of zero) is:

$$E_0 = E_{02} - E_{01} = -AE_s$$

where

$$A = 1 + 2 R_0/R_1$$
 and $E_s = E_1 - E_2$

The differential gain of the amplifier is set by varying one resistor, R_I . The significant factor about the input stage is that the inevitable mismatch of the R_0 's affects only the differential gain, not the common-mode gain of the circuit. Varying R_I will adjust the gain of the input stage without significally affecting common-mode gain.

Another virtue of this input circuit is that the input impedance is essentially independent of gain. Both input op amps are operating as noninverting buffer amplifiers, so both inputs see the input impedance of the op amps. The instrumentation amplifier has typically 50 $M\Omega$ differential input impedance and 50 $M\Omega$ common-mode input impedance.

One limitation of this circuit is that the common-mode input range and the differential input signal range are interdependent. The reason for this can be seen by putting $E_{\theta 1}$ and $E_{\theta 2}$ in terms of a common-mode input voltage E_{cm} and a differential input signal E_s . With $E_{cm}=(E_1+E_2)/2$, $R_1=R_3$, and neglecting both resistor and op-amp errors, the outputs are given by

$$E_{0\ell} = \frac{R_{I} + R_{0}}{R_{I}} \left(E_{cm} - \frac{E_{s}}{2} \right) - \frac{R_{0}}{R_{I}} \left(E_{cm} + \frac{E_{s}}{2} \right)$$

$$E_{0I} = \frac{R_{I} + R_{0}}{R_{I}} \left(E_{cm} + \frac{E_{s}}{2} \right) - \frac{R_{0}}{R_{I}} \left(E_{cm} - \frac{E_{s}}{2} \right)$$

$$E_{0\ell} = E_{cm} - \left(1 + 2 \frac{R_{0}}{R_{I}} \right) \frac{E_{s}}{2} = E_{cm} - A \frac{E_{s}}{2}$$

$$E_{0I} = E_{cm} + \left(1 + 2 \frac{R_{0}}{R_{I}} \right) \frac{E_{s}}{2} = E_{cm} + A \frac{E_{s}}{2}$$

If the op amps are limited to ± 10 V output range for linear operation, then both $E_{\theta I}$ and $E_{\theta 2}$ must be kept to less than 10 volts. This means that we must have

$$\left|E_{cm}\right| + \left|\frac{AE_s}{2}\right| \le 10 \text{ V}$$

With ±10 V op amps used in this type of instrumentation amplifier, some additional restrictions are

$$\mid E_{cm} \mid \leq 10 \text{ V}, \mid E_s \mid \leq 10 \text{ V} \text{ and } \mid AE_s \mid \leq 10 \text{ V}$$

These limitations seldom pose any hardship, but they must be kept in mind whenever the commonmode input E_{cm} is expected to exceed ± 5 V.

A typical signal-conditioning requirement will illustrate the tradeoffs in using op amps or modular instrumentation amplifiers. Consider a semi-active bridge with 350- Ω bridge elements and with a maximum ΔR of $\pm 10~\Omega$ (See Fig. 5). Assume that a $\pm 5~\mathrm{V}$ output signal is desired.

Op-amp circuit design

The differential input impedance (Z_d) will load the bridge such that

Gain Error Term Due To Loading $pprox rac{R_{\scriptscriptstyle B}\,+\,\Delta R}{Z_{\scriptscriptstyle d}}$

where

$$R_R << Z_d$$
 and $\Delta R << R_R$

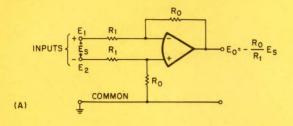
If we allow 0.5% error for this effect, then $Z_d \ge 70 \text{ k}\Omega$. This means that the R_i 's of the opamp circuit must each be 35 k Ω .

The required differential gain is approximately

$$A \approx \frac{5 \text{ V}}{\frac{10 \Omega}{4 \times 350 \Omega} \times 10 \text{ V}} = 70$$

The gain of the op-amp circuit is R_{θ}/R_{I} , so with A of 70 and R_{1} of 35 k Ω the feedback resistors must be 2.45 M Ω . The circuit is shown in Fig. 6. Full-scale output will be ± 5 V for ± 10 Ω of variation in R_{T} .

Another possible source of error is the degradation of CMR due to the bridge imbalance affecting the gain balance. In effect, the bridge imbalance



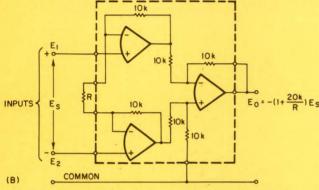


Fig. 1 Two methods of obtaining a data amplifier: (a) op-amp circuit and (b) instrumentation-amplifier circuit.

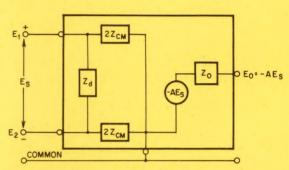


Fig. 2. Gain-block equivalent circuit.

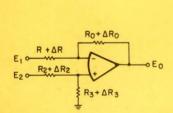


Fig. 3. Circuit of differential op amp with real resistors; matching R_{0} to R_{3} and R_{1} to R_{2} improves CMRR, but affects gain.

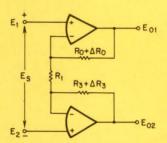


Fig. 4. Input stage of Fig. 1b. Trimming differential gain does not affect common-mode gain.

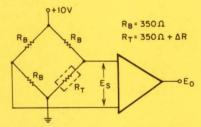


Fig. 5. Transducer bridge with signal-conditioning amplifier.

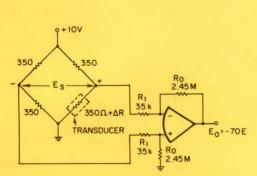


Fig. 6. Bridge amplifier using op amp.

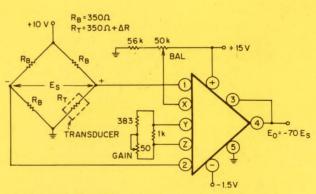


Fig. 7. Bridge amplifier using instrumentation amp.

TABLE 1 Cost/performance tradeoffs for two typical commercial instrumentation amps.

Key Specs	Inst. Amp. 1	Inst, Amp 2
		The second secon
Dc gain nonlinearity	± 0.02%	± 0.05%
Gain TC at X100	± 0.001%/°C	± 0.001%/°C
Input impedance (diff and CM)	50 ΜΩ	300 MΩ
CMR, dc to 100 Hz, gain of X10	80 dB (min)	80 dB (min)
Input blas current at 25°C vs. Temperature	± 20 nA 1 nA/°C	± 50 nA ± 2 nA/°C
Output offset vs. temperature at gain A	\pm (47 + 3XA) μ V/°C	$\pm (500 + 9.5 \text{XA}) \mu\text{V/°C}$
Rated output	± 10 V at ± 10 mA	± 10 V at ± 5 mA
Output impedance, dc to 1 kHz	0.1 Ω	10 Ω
Temperature range	- 25°C to + 85°C	- 25°C to + 85°C
Rated power supply	± 15 Vdc	± 15 Vdc
Unit price	\$95	\$39

appears as an error in the magnitude of the R_I on the inverting input. In this example, however, ΔR is so small relative to R_I that little error occurs.

If the amplifier must operate over a wide temperature range, then drift errors must be considered. Temperature variations will cause changes in the op-amp offsets, gain and CMR. Also, the external resistor network will change with temperature. This will vary the gain and CMR.

Offset and gain drifts. For this circuit, consider an IC op amp with a maximum voltage drift of $\pm 10~\mu V/^{\circ} C$ and a maximum input offset-current drift of $\pm 0.3~nA/^{\circ} C$. The output drift will be

$$\pm \frac{\Delta E_0}{\Delta T} = 2.45 \text{ M}\Omega \times 0.3 \text{ nA/°C} + 10 \,\mu\text{V/°C} \times 70$$

$$= \pm (0.735 \text{ mV/°C} + 0.7 \text{ mV/°C})$$

$$\approx + 1.5 \text{ mV/°C} \text{ (max.)}.$$

Since ± 5 V was already chosen to be full-scale output, the output drift will at most cause about $\pm 0.03\%/^{\circ}\text{C}$ error.

Transistor current gain decreases with decreasing temperature, but the transconductance increases with decreasing temperature. Therefore, if the amplifier is to be operated over the full temperature range of -25°C to +85°C, the possible decrease in open-loop gain should be considered. This gain decrease is typically 0.1 dB/°C. As a rule of thumb, just allow about 6 dB extra gain for this effect.

The IC op amp of this example has a minimum open-loop gain of 93 dB at 25°C, so we can be reasonably sure of having gain of 87 dB over the temperature range. Since only 30 dB of closed-loop gain is needed, there will b about 87 dB - 30 dB = 57 dB of loop gain for this example. Gain error for a differential op-amp circuit is approximately $1/(\mbox{loop gain})$. The exact expression for gain error is

$$ext{Gain Error} = rac{rac{1}{A_{ heta}}\left(1+rac{R_{ heta}}{R_{ heta}}
ight)}{1+rac{1}{A_{ heta}}\left(1+rac{R_{ heta}}{R_{ heta}}
ight)} \ ext{where } A_{ heta} = ext{open-loop gain} \ rac{R_{ heta}}{R_{ heta}} = ext{closed-loop gain} \ ext{}$$

So for this example, the gain error will be about 1/(60 dB), or 0.1%. This is negligible when compared with other errors. But if we had chosen an IC op amp with lower open-loop gain, we might have had a serious source of error.

CMR. The CMR of an op amp is almost always specified at 25°C. It will vary somewhat with temperature, but its drift is seldom specified by the op-amp manufacturer. Since the input transistors are of the same type and are matched in gain at 25°C, the gain through the inverting input tends to vary in the same manner as the gain through the noninverting input.

Thus the CMR change with temperature is generally small in a well-designed, low-drift amplifier.

External resistor network-drift

Resistance drift in the external gain network will cause gain and CMR to drift. Metal-film or wirewound resistors are often used to obtain reasonably low drifts. Metal-film resistors having TCs of $\pm 100~\rm ppm/\,^{\circ}C$ to $\pm 50~\rm ppm/\,^{\circ}C$ and wirewounds with $\pm 10~\rm ppm/\,^{\circ}C$ are available as standard units. Gain and CMR drift depends upon the change in resistor ratios rather than drift in absolute values. The match in drift between the two $2.45{\text{-M}\Omega}$ resistors and between the two $35{\text{-k}\Omega}$ resistors determines the CMR drift. Drift in the ratios between the $35{\text{-k}\Omega}$ and $2.45{\text{-M}\Omega}$ resistors determines gain drift.

One disadvantage of the op-amp circuit versus the instrumentation-amplifier circuit is that, for high gain, op-amp feedback generally requires large resistance values (2.45 M Ω in this example). Also, the resistors in the instrumentation-amplifier circuit are all the same value (except the gain-setting resistor), so good matching and tracking are much easier to obtain.

How good do the resistors need to be? If we assume that relatively inexpensive ± 100 ppm/°C metal-film resistors are used, we might have as much as $\pm 0.02\%$ /°C gain drift due to resistor ratio drift. Actually, since resistors of the same type tend to drift in the same manner, we would expect more like $\pm 0.01\%$ /°C of gain drift. This can sometimes be improved by purchasing the resistors as a network with specified tracking characteristics.

An inexpensive op amp used with untrimmed

and unmatched $\pm 0.1\%$ resistors can provide about $\pm 1\%$ to $\pm 3\%$ accuracy over a temperature range of $-25\,^{\circ}$ C to $+85\,^{\circ}$ C. Trimming improves this to ± 0.5 or 1.0%. A high-quality op amp plus a stable resistor with $\pm 0.01\%$ ratio accuracy could reduce temperature-drift error by a factor of ten, yielding an overall accuracy of $\pm 0.1\%$ to $\pm 0.5\%$ over the full temperature range. Some periodic trimming might be necessary to maintain this accuracy.

Instrumentation-amplifier circuit design

An instrumentation amplifier can be used to fulfill the signal-conditioning requirement as shown in Fig. 7. Although somewhat more expensive than the simple op-amp-circuit approach, performance is substantially better. An op-amp circuit of approximately equal performance would generally be more expensive than the instrumentation amplifier. Unlike op amps, instrumentation amplifiers are specified in terms of their overall performance as gain blocks. Table 1 gives some specifications representative of encapsulated instrumentation amplifiers. The cost/performance tradeoffs show up clearly.

The following are the chief instrumentation amp design considerations:

Gain. Gain trimming does not affect the CMR, as it does in the op-amp circuit. The gain is set by one external resistor according to the equation: $A=1+20~\mathrm{k}\Omega/R$. However, the gain nonlinearity of $\pm 0.02\%$ and the gain-pot resolution limit the accuracy with which the gain may be set. Even so, the gain may be easily calibrated to within $\pm 0.05\%$ of the desired value.

CMR. The differential gain is set at 70 and the common-mode input is +5 Vdc in this example. The worst-case error at the output due to the common-mode input is about 16 mV. Since the full-scale output for this example was chosen to be ±5 V, the error due to common-mode effects is about 0.3%. The common-mode input of this example stays almost constant, so the 16 mV appears as a dc offset. Some of this may be balanced out if desired, so CM effects will probably introduce less than 0.2% error.

Input impedance. One big advantage of the instrumentation amplifier over the op-amp circuit is that input impedance and gain do not interact. The $50\text{-M}\Omega$ input impedance is so high relative to a $350\text{-}\Omega$ bridge that any loading effects are negligible.

Input bias current. A bias current of ±20 nA can flow into each input terminal. The input error generated by this effect is negligible for this example:

$$\Delta E_i = 350 \Omega \times 20 \text{ nA} = 7 \mu\text{V}$$

This is less than ± 0.5 mV at the output.

Output impedance. The 0.1- Ω output impedance is low enough so that gain error due to output loading will be negligible. The gain error will be 0.1×10^{-4} or 0.001%.

Drift errors. Input voltage drift is the largest source of drift error. For this example the voltage drift at the output will be

$$\frac{\Delta E_o}{\Delta T} = \pm 47 \,\mu\text{V/°C} \pm 3 \,\mu\text{V/°C} \times 70 \text{ (max)}$$

$$= \pm 257 \,\mu\text{V/°C (max)}$$

Over a range of $\pm 50\,^{\circ}\mathrm{C}$ this would imply a voltage-drift error at the output of about $\pm 13\,\mathrm{mV}$, or $\pm 0.25\,\%$ of the $\pm 5\,\mathrm{V}$ output for full-scale signal. Offset-current drift of $\pm 1\,\mathrm{nA}/^{\circ}\mathrm{C}\,\times\,350\,\Omega$ is so small that it may be ignored.

A subtle problem may occur in using the voltagedrift specs over less than the full range of -25°C to +85°C. The drift spec is an average drift, and at any given temperature the drift may exceed the spec value. So if you're operating over less than full temperature range you should allow extra drift margin for this effect.

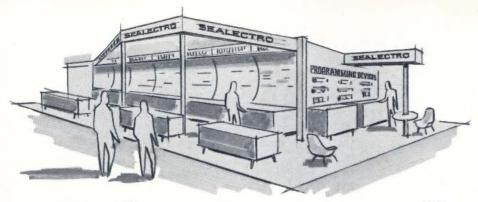
Another source of drift error will be the change in gain with temperature. It's very important that the gain-setting resistor be stable. Assuming that a stable wirewound is used for the $280-\Omega$ resistor, the gain drift will be on the order of $\pm 0.001\%$ /°C. This effect is small when compared to voltage drift, but should be included.

Thus, a standard modular instrumentation amplifier can easily provide an accuracy of $\pm 0.25\%$ at room temperature if the balance and gain are trimmed. Drift will be about $\pm 0.003\%$ /°C, or $\pm 0.3\%$ over a range of ± 50 °C. Overall accuracy over the full temperature range will be on the order of $\pm 0.5\%$, and certainly better than $\pm 1\%$, depending on the gain-resistor stability and care of adjustment.

The example given in this article illustrates the general design procedure in selecting operational amplifiers or modular instrumentation amplifiers for signal-conditioning needs. Both can be used as gain blocks where the primary factors to consider are the required gain and accuracy. Input impedance, CMR, and voltage drift will generally be the deciding parameters.

Operational amplifiers offer the lowest possible cost if the accuracy and gain requirements are not too stringent, particularly if the signal-source impedance is fairly low. When you're looking for guaranteed overall accuracy of better than $\pm 1\%$ over a wide temperature range, the cost of using an op amp goes up considerably. You have to buy a low-voltage-drift unit with good CMR, and then you have to buy a stable, precise feedback network. Remember that fine adjustments of CMR and gain will interact in the op-amp circuit.

On the other hand, an instrumentation amplifier in a modular, encapsulated package will easily provide an accuracy of $\pm 1\%$ to $\pm 0.25\%$ over the full temperature range. Only one stable resistor is required externally. The input impedance, differential gain and common-mode gain are essentially independent, and thus the adjustment procedure is simpler. Low drift is available at moderate cost. Instrumentation amplifiers will increasingly displace operational amplifiers as signal conditioners where a combination of high input impedance, high differential gain, good CMR and low drift is needed.



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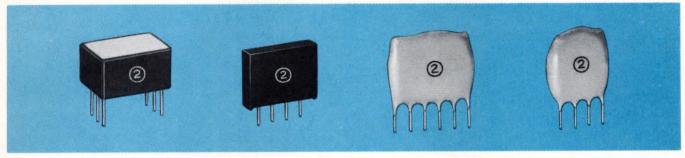
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Semiconductors

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Products Of The Month

Beam-lead linear ICs, TA5726, TA5830, for hybrid circuitry. TA5726 is 12-beam version of CA3015 op amp. TA5830 is 14-beam transistor array for use as building block; contains isolated and differentially connected transistors. Samples available. RCA.

Mini-DIP op amps, LM301AN, LM-307N, LM741CN, one-half size of flat pack. Two mini-DIPs fit in standard 16-pin DIP socket. Silicone package. LM301AN is reduced temp version of LM101A. \$3.25. NATIONAL SEMI-CONDUCTOR. 568

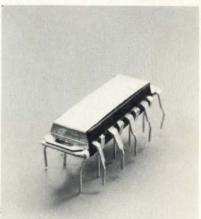
Wideband op amp, RA2620, for high-input-impedance comparator applications. Typ bias, offset currents of 2 nA; input resistance, $100~\text{m}\Omega$ min; max offset voltage, 4 mV (adjustable to zero). Internally compensated for closed loop gains greater than three with typ unity gain crossover at 35

MHz. Gain bandwidth product, 60 MHz at 20-dB closed-loop gain; 100 MHz from 40 to 100 dB gain. Full-power bandwidth, 600 kHz; slew rate, 35 V/ μ s. TO-99 or TO-116 DIP. \$10.70 (100-999). RADIATION. **569**

Video amplifier, SG733, for wideband applications. Gain stability can be set at fixed gain options of 10, 100, 400 without external components. Bandwidth, 120 MHz; input resistance, 250 kΩ. Differential voltage gain, 300-500 V/V. TO-100 or TO-116 DIP. SILICON GENERAL. 570

Micropower op amp, QC1735, similar to Fairchild μ A735. Power drain under 100 μ W; bias current, 3 nA; offset current, 1 nA. Delivers up to 10 mA. Supply, 18 V. \$9.60 (100-999). QUALIDYNE.

Linear consumer ICs, TA5914, TA-5625, TA5752, include complete video



i-f system on single chip. TA5914 consists of 85-dB video i-f amplifier, video detector, video amplifier, sound channel amplifier and detector, 4.5-MHz amplifier, keyed AGC-noise immunity circuit, tuner AGC delay amplifier, and zener diode for regulated voltage reference. TA5625 and TA5752 are designed for chroma systems. Packages: TA5914, 18-lead DIP; TA5625, TA5752, 16-lead DIP. RCA.

Dual preamplifier, PA239, for low noise applications. Consists of two identically matched 68-dB gain amplifiers fed from internal power-supply filter. Voltage gain, 65 dB min; channel separation, 90 dB min; power supply rejection, 55 dB typ; noise figure, 1.8 dB. 14-lead DIP. \$2.28. GE. **573**

Hex inverter, 332, contains 4 inverters and 2 input NAND gates. Addition to High Noise Immunity Logic (HNIL) line. Drives 12-V outputs. Output currents to 10 mA. 16-pin DIP. \$2.25 (100-999). AMELCO. 574

Series 74 NOR gates, US 7427A, 74-27A, TTL ICs. Triple 3-input and dual 4-input gates, respectively. Propagation delay, 10 ns; power dissipation per gate

This Month's ICs

Beam-lead linear ICs. RCA. 567 Mini-DIP op amps, \$3.25. NATIONAL SEMICONDUCTOR. 568 Wide-bandwidth op amp, \$10.70. RADIATION. 569 Video amplifier. SILICON GENERAL. 570 Low-power-drain op amp, \$9.60. QUALIDYNE. 571 Linear consumer ICs. RCA. 572 Dual audio amp, \$2.28. GE. **573** Hex inverter, \$2.25. AMELCO. **574** NOR gates, \$1.45. SPRAGUE. 575 50-MHz J-K flip-flops, \$3.15. SPRAGUE. **576** Line driver, receiver, \$7.50. FAIRCHILD. **577** 7-segment decoder/driver, \$4.84. SIGNETICS. **578** Up/down counters, \$5.85. ADVANCED MICRO DEVICES. **579** High-voltage TTL, \$1.75. NATIONAL SEMICONDUCTOR. 580 Content-addressable memories, \$13.30. SIGNETICS. 581 TTL 8-bit shift registers. TEXAS INSTRUMENTS. 582 2048-bit MOS ROM, \$18.80. TEXAS INSTRUMENTS. 583 Series 54/74 TTL line, \$1.09. MOTOROLA. 584 MSI TTL line, \$3.70. MOTOROLA. 585 Complementary MOS building blocks. RCA. 586 ECL 1.4-ns OR/NOR gates. RCA. 587

This Month's Transistors and Diodes

Dual junction FETs. AMELCO. **588**Dual MOS FETs, \$6.78. MOTOROLA. **589**Dual MOS FETs, \$1.65. RCA. **590**Rf power transistors, \$11.95. GENERAL SEMICONDUCTOR. **591**High-frequency power transistors, \$9.00. KERTRON. **592**UHF power transistor. \$185. TRW. **593**Photo transistor, \$3.80. SIEMENS. **594**Low-cost SCR, 32ϕ . TRANSITRON. **595**

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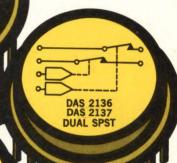




DAS 2114 SPDT/DPST

DAS 2107 DAS 2110 SPST

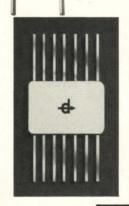
DAS 2126 SPDT/DPST





This enlarged family of Dickson hybrid analog switches undoubtedly contains the circuits you need for your data transmission systems. You can select from a variety of functions in standard 6, 10, 12, and 16 lead packages as well as the TO-87 14 lead flat-pack.

Models DAS 2126, 2132, 2133, 2136, and 2137 operate directly from DTL, RTL, or TTL logic. The other four switches require a 0 to +15V drive signal. All of these standard Dickson units provide fast switching-speeds, handle AC signals through 1 MHz, and have the quality and dependability you can expect from a leading supplier of high-reliability semiconductors. FOR COMPLETE TECHNICAL IN-FORMATION and details on Dickson custom hybrid capabilities, contact Dickson or use this publication's reader service card.



MODEL NUMBER	TYPE	LOGIC LEVEL	R _{on} Ω	t _{on} μsec	V _{out} volts	PACKAGE	PRICE 100-999
DAS 2107	SPST	high-level inverting	50	.3	5	TO-5 6 lead	\$ 5.50
DAS 2110	SPST	high-level inverting	30	.3	10	TO-5 6 lead	\$ 8.00
DAS 2114	SPDT/ DPST	high-level alternating	30	.9	10	TO-8 12 lead	\$15.00
DAS 2126	SPDT/ DPST	low-level alternating	30	1.5	10	TO-8 12 lead	\$18.00
						T0-87 14 lead	\$19.80
DAS 2128	QUAD SPST	high-level inverting	30	1.0	7	TO-8 16 lead	\$30.00
DAS 2132	DUAL SPST	low-level non-inverting	30	0.5	10	TO-5 10 lead	\$18.00
						T0-87 14 lead	\$19.80
DAS 2133	DUAL SPST	low-level non-inverting	30	0.5	10	T0-5 10 lead	\$19.75
						TO-87 14 lead	\$21.75
DAS 2136	DUAL SPST	low-level inverting	30	0.5	10	TO-5 10 lead	\$18.00
						TO-87 14 lead	\$19.80
DAS 2137	DUAL SPST	low-level inverting	30	0.5	10	T0-5 10 lead	\$19.75
						T0-87 14 lead	\$21.75

 New units designed to switch 20 V peak-to-peak, analog signals. Shipments are being made from stock Custom Analog Switches are also available



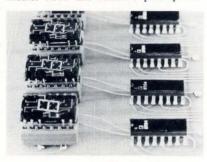
DICKSON ELECTRONICS CORPORATION

PHONE (602) 947-2231 TWX 910-950-1292 TELEX 667-406 P. O. BOX 1390 • SCOTTSDALE, ARIZONA 85252 function, 37 mW. 14-lead DIPs and flat packs. \$1.45 (100-999). SPRAGUE.

J-K flip-flops, US74H571-2A, with 50-MHz speed. Series 54, typ power dissipation, 60 mW. Logic input data is stored in appropriate capacitor when clock line is high and transferred to outputs during clock high-to-low transition pulse. Direct preset input provided on both devices. 14-lead DIPs. \$3.15 (100-999). SPRAGUE. 576

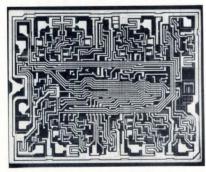
Line driver, receiver, 9614, 9615, operate from 5-V supplies. 9614 is dual differential line driver, with current sinking capability of 40 mA; 9615 is dual differential line receiver with 15-V common mode rejection. Open collector outputs allow 12 V swing via external resistors. ICs can be adapted for wired-OR applications. 16-pin DIPs. \$7.50, FAIRCHILD.

Seven-segment decoder/drivers, 8T04, 8T05, for driving lamps, interface elements. 8T05 has resistive pull-up out-



put circuit which provides source current to drive interfacing elements. Operating voltage for each unit, 5 V. Lamp test control provided to turn all segments on. 16-pin flat packs and DIPs. \$4.84 (100-999). SIGNETICS.

Up/down counters, 8284, 8285, pinfor-pin replacements for Signetics



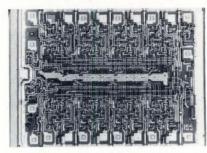
counters. Guaranteed clock frequency, 20 MHz. Compatible with DTL, TTL. Carry-look-ahead scheme allows cascading of stages. \$5.85 (100 up). AD-VANCED MICRO DEVICES. 579

High-voltage TTL, DM8810-12, for direct interfacing with MOS. DM8812, is hex inverter, DM8810, and DM8811 are TTL/MOS interface gates with different pinouts. 8812 can withstand 14 V on output. 14-lead DIP. \$1.75. NATIONAL SEMICONDUCTOR. 580

Content addressable memories, 8220, 2, incorporate addressing and compari-

son logic. Eight identical memory cells organized as four words, each two bits long. TTL circuitry. Dissipation: 8220, 590 mW; 8222, 300 mW. 16-pin DIP. \$13.30 (100-999). SIGNETICS. **581**

8-bit shift registers, SN74198-9, called truly universal shift registers. SN74198 has parallel inputs and parallel outputs on each flip-flop and serial inputs to



the first and last flip-flop. SN74199 has J-K inputs to first flip-flop for use in counting applications, a master clear line and gated clock inputs. Circuits have 87 equivalent gates. Input clock frequency, 32 MHz; Diss per bit 47 mW. 24-pin DIPs. \$7.28 (100-999). TEXAS INSTRUMENTS. 582

Static 2048-bit ROM, TMS2600JC, two different memory organizations are available. Can function as 512-word by 4, or 256-word by 8-bit read-only memory. Data for final programming of mask fed in by punched cards supplied by customer. Complete information given to aid in preparation of punched cards. 24-pin DIP. \$18.80 (100-249). TEXAS INSTRUMENTS.

Series 54 additions, MC5492, MC54107, MC5403, counter, J-K flip-flop and NAND gate. MC5492/MC7492 is a 4-bit counter comprised of a divide-by-two section and a divide-by-six section. MC 54107/MC74107 is a dual JK flip-flop. MC5403/MC7403 consists of four 2-input NAND gates with no output pullup circuits. DIPs. \$1.09. MOTOROLA.

MSI TTL line, MC9300/MC8300 series, replace older 9300/8300 devices. New line includes MC9300/MC8300, a universal 4-bit shift register consisting of four flip-flops operated in the synchronous mode; MC9304/MC8300, a dual full adder; MC9304/MC8309, a dual 4-channel data selector; MC9312/MC8312, an 8-Channel data selector. DIPs and flat packs. \$3.70. MOTOROLA.

COS MOS, four ICs, multiplexer, counters, shift register, all developmental types. Four-channel multiplexer TA5460 switches analog or digital signals. Divide-by-N counter TA5580 has 3-MHz typ speed. TA5683 8-stage asynchronous shift register has 5 μW diss. TA5776 is 14-stage ripple-carry binary counter/divider. Samples available for evaluation. RCA.

ECL OR/NOR gates, TA5746-7, with 1.4-ns delay time. Operate from 5-V supply. Input capacitance, 2.5 pF, diss., 35 mW per gate. Logic levels: 0.85,

1.65 V. 16-pin DIP. Samples available for evaluation. RCA. 587

Dual junction FETs, 2N5045-7, n-channel devices. Max transconductance ratio, 1; input capacitance, 8 pF; noise figure, 5 dB. FETS matched gate-to-source voltages. AMECO. **588**

Dual MOS FETs, MFE3020-1, for chopper or switching applications. Reverse gate current, 10 pA max at 25 V. On resistance, 250 Ω; input capacitance, 7 pF. TO-76. \$6.78. MOTOROLA. 589

Dual MOS FETs, 3N187, 3N200, for rf amplifier applications up to 300 MHz and 500 MHz. Back-to-back diodes protect gates. N-channel depletion types. 3N187, \$1.65; 3N200. \$2.65 (1000 up). RCA. 590

Rf power transistors, 2N2877-80, for inverter amplifier or switching applications. Diss., 30 W; f_T, 50 MHz. TO-111. \$11.95 (100 up). GENERAL SEMICONDUCTOR. **591**

High-frequency power transistors, 3TX620-1, operate at 12.5 V. 3TX620 delivers 1 W at 470 MHz with min 7



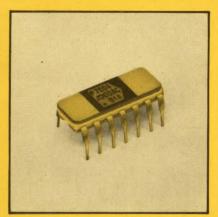
dB gain. 3T621 delivers 2 W. Molded packages. Devices also available in ceramic packages. \$9. KERTRON. **592**

UHF power transistor, JO-2001, internal matching circuitry reduces input reactance to essentially zero. Output power, 40 W across 225-400 MHz band at 24 V. Gain across 225-400 MHz, 5 dB; Min eff, 50%. \$185. TRW.

Photo transistor, BP101, for consumer applications. Typ photo current, 150 μA for an illumination of 1000 Lux.



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Resolution:	6 Bits
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Output:	0 to +10V
6 Bit Settling Time:	3 Microseconds
Input Logic Levels:	0 to +3V
Power Supply:	±12V to ±18V
Power Supply Rejection:	0.15% FS/V
Power Consumption:	250mW

That's the monoDAC-01:

The world's first commercial, completely selfcontained monolithic, 6-bit D/A Converter. Write for more information and/or contact the representative in your area given below!



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For further information, call: ALBUQUERQUE (505) 256-1749; ALEXANDRIA (703) 548-7818; ATLANTA (404) 876-2260; BALTIMORE (301) 944-8262; BURBANK (213) 846-9631; CHERRY HILL (609) 966-4070; COCHITUATE, MASS. (617) 653-8229; DALLAS (214) 348-6660; DAYTON (513) 298-9897; DENVER (303) 744-2821; FT. LAUDERDALE (305) 564-8000; HOUSTON (713) 782-5406; HUNTSVILLE (205) 539-4411; NEW YORK (212) 343-4630; ORLANDO (305) 425-5505; PALO ALTO (415) 326-6400; PAOLI (215) 644-3477; SALT LAKE CITY (801) 278-5022; SAN DIEGO (714) 222-1121; TULSA (918) 939-2848; WILLOUGHBY, OHIO (216) 946-6080; WINSTON-SALEM (919) 725-5384.

TO-18 with translucent cover. \$3.80 each. SIEMENS. 594

Low-cost SCR, RTCO2, in TO-18 case. Gate sensitivity under 1 mA. Holding current, 10 mA max. Handles 4 A at 80°C. 32¢ (1000 up). TRANSITRON.

Capacitors

High-Q capacitor, A7C-AY01, with silicone-epoxy body insulation. For low frequency, rf, vhf and uhf. Q greater than 5000 at 1 MHz. 300 V, TC + 95 ppm/°C. 1/8 in. square with silver ribbon leads. 76¢ (1000-up). ATC.

Metalized polycarbonates, 22, 0.001 μF to 50 μF . 50-V and 100-V case sizes. Tolerances to 1%. -55 to 105°C Cap change over temp \pm 1.5%. Insulation resistance 100 MΩ \times μF at 25°C. Tested to Mil-C-18312. SEI.

Ceramic chips, BB, for NPO or W dielectrics. 6 pF to 6800 pF in 50 and 100-V sizes. $0.050 \text{ in.}^2 \times 0.040 \text{ in.}$



Silver end terminations with gold and palladium silver also available. Meet Mil-C-1105 and Mil-C-39014. USCC.

NPO-ceramic chip kit, for use in hybrid circuits. Contains 300 chips. Ten chips of all std RETMA values from 3.9 pF to 1000 pF in 50-V size. In a 7 × 10-in. hard cover holder with individual see-through pockets. Contains complete specs and ordering info. \$99.50. MONOLITHIC DIELECTRICS.

Resistors

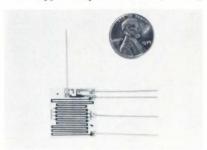
Low-cost single-turn film pot, C, with servo mount and bushing designs. 7/8 in. diameter with a choice of 1/8 in. or 1/4 in. dia shaft. Infinite resolution with resistance $1 \text{ k}\Omega$ to $10 \text{ k}\Omega$. Linearity 1% to 0.25%. Life 25 million revs. 1 watt at 70°C . \$4.99 (100-up). NEI.

Hybrid-resistor array, 863, with cermet thick-film 10-bit BCD ladder designed specifically for Fairchild μ A722 with compatible terminal arrangement. Resistor uses identical materials to insure close tracking -20 to +85°C. \$17.50. BECKMAN.

Thick-film chip resistors for hybrid-circuit applications. Four sizes from 0.050 in. 2 to 0.050 in. \times 0.150 in. Resistance 100Ω to 500kΩ Tolerance $\pm 20\%$ to $\pm 1\%$. TC ± 200 ppm/°C

from -55 to +150°C. 75 mW to 300 mW depending on size. Resistance material on a 95% alumina substrate with solder-tinned electrodes. DALE. 527

High-voltage divider, HD3042, on alumina substrate. 100.6 MΩ. 5-kV resistor tapped to provide $60M\Omega$, $40M\Omega$,



and two 300 k Ω . Tolerances for large resistor $\pm 10\%$. 300 k Ω units to 1%. R's track to 25 ppm/°C. Planar design minimizes stray L and C. \$30. MICROTEK. **528**

Packaged Circuits

Price Change

DDC has reduced prices of its EDAC series of D/A converter modules by approximately 50%. This series has a resolution of 11 bits and accuracies of 8, 9, 10 or 11 bits. Examples of new unit-qty prices are \$79 (formerly \$150) for EDAC-8-3, and \$189 (formerly \$400) for EDAC-11-1.

Differential data amplifier, 300, with CMRR that increases with gain. Absence of wirewound resistors ensures low electro-magnetic pickup. Bandwidth does not decrease inversely with gain. Input $Z = 10^{11}\Omega$. CMRR 60 dB (unity gain) and 96 dB (gain of 1000). Gain controlled by single external resistor. Offset-voltage drift $50\mu V/^{\circ}C$ (type 300A) or $25\mu V/^{\circ}C$ (type 300B). \$65 (300A in 1-9) and \$85 (300B in 1-9). Stock. DYNAMIC MEASUREMENTS,

Low-drift op amps, Series 184, with stability comparable to chopper-stabilized amplifiers. Differential configuration. Dual-monolithic input stage. Offset-voltage drift 1.5 μ V/°C (J version), 0.5 μ V/°C (K version) or 0.25 μ V/°C (L version). Offset voltage 250 μ V (J) or 100 μ V (K and L). Dc gain 300,000. Bandwidth 1 MHz. CMRR 100,000. Noise 1 μ V pk-pk (0.01 Hz to 1 Hz). Bias current 25 nA. Bias-current drift 0.25 nA/°C. Output \pm 10 V at 5 mA. 1.5 \times 1.5 \times 0.4 in. Unit prices: \$45 (184J), \$50 (184K) and \$75 (184L). Stock. ANALOG DEVICES.

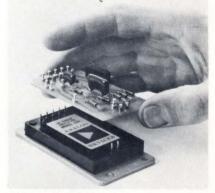
FET hybrid-IC op amp, 1407/140701, with gain-bandwidth product of 30 MHz. Packaged in low-profile TO-8



can. Input impedance $10^{11}\Omega$. Slew rate 8 V/ μ s. CMRR 10,000 at ± 10 V. Short-protected (output to ground). Initial offset ± 10 mV (can be trimmed to zero with external 250- $k\Omega$ pot). Open-loop de gain 20,000 (rated load). Output ± 11 V at ± 2.2 mA. Overload recovery time 0.1 μ s. Rated operating temp -25 to $+85^{\circ}$ C. Offset-voltage drift $\pm 55 \ \mu$ V/°C (14070) s72 (1407 in 1-9) and \$80 (140701 in 1-9). Stock. TELE-DYNE PHILBRICK.

Linear power amplifier, IC-50, with power dissipation of 50 W at case temperature of 90° C. Typical output impedance $0.01~\Omega$. Min voltage gain 100,000. Operates from power supplies of ± 15 to ± 30 V. Frequency response typically flat to 20 kHz at gain of 100. Compact module. Matching circuit cards provide space for scaling resistors, capacitors, diodes and test points. Matching power supplies available. Approximately \$140 (1-10). 2 wks. INLAND CONTROLS. 480

Power op amps, 402 and 403, with output of 60 W (\pm 12 V at 5 A or \pm 20 V at 3 A). Compact package 3.5 \times 1.8 \times 0.7 in., including heat sink. Can be bolted directly to motor frames, transducer equipment, etc.,



without introducing ground-loop problems. Open-loop dc gain 3000 (402) or 5000 (403). Small-signal bandwidth 400 kHz. Full-power response 10 kHz. Input impedance 300 k Ω . Voltage drift $\pm 50~\mu V/^{\circ} C$. Auxiliary clip-on socket accommodates external components. \$85 (either type in 1-9). \$15 (auxiliary socket). 2 wks. ANALOG DEVICES. 481

Fast-settling op amp, FST151, with settling time of $0.6~\mu s$ (to 0.01%). FET input. Input impedance $10^5~M\Omega$. Typical CMRR 40,000. Gain 250,000. Slew rate $100~V/\mu s$. Available in 2 (Continued on page 66)

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FET Applications Handbook

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Edited by Jerome Eimbinder, Managing Editor, EEE Magazine

Chock-Full of FET Circuit Design Data, Written Especially for the Practicing Design Engineer

 ${f T}$ his brand-new edition of a popular handbook contains current, practical material prepared by some of the most capable men in the field. Containing 25% more material than before, this completely revised and updated edition comprises a wealth of data on the FET and its various applications in practical circuit designs. The first 4 Chapters are devoted to basic FET types, parameters and characteristics, and operational modes. Additional Chapters — providing the real "meat" of the content — deal with linear applications, chopper and switching circuits, integrated circuits, and photo-FETs.

The early Chapters delve into current-voltage relationships, application areas, DC and AC amplifiers, voltage-controlled attenuators, and limiter and chopper circuits. So that the reader will be well grounded on the subject, several Chapters are devoted to biasing considerations, complete with transfer curves and graphical analyses. Also, an entire Chapter is devoted to the FET as a constant-current source, providing a detailed dissertation on the constant-current element and cascaded operation.

Considerable attention is also given to FET oscillators, describing various types and the necessary biasing arrangements. Entire Sections of the book, rounding out essential design data, include starting conditions, power output, frequency stability and efficiency. Another Chapter of vital interest covers FET noise measurement; unique new test procedures and accurate measurement methods are presented for the first time as a single, compact source of information. The same may be said for the chapters on amplifier design, encompassing types for both audio and VHF applications.

The in-depth information provided in this book will be of immediate value to anyone looking for new ideas and unique circuit applications, including many basic circuit descriptions. For the engineer interested in photo-FET design, two Chapters offer many practical and unusual applications, including an FET electrometer amplifier. Illustrated with over 250 circuit drawings and graphs, the content includes practical mathematical analyses to explain operation and design detail. Appendices contain often-needed design data and charts arranged to serve as a convenient quick-reference source. 352 pps., over 250 illus.

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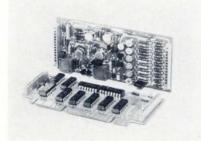
different versions: 151A and 151B. Voltage drift 35 mV/°C (151A) and 15 mV/°C (151B). Bias current 0.1 nA (151A) and 0.05 nA (151B). Output ± 10 V at ± 29 mA. $1.5 \times 1.5 \times 0.4$ in. Prices in 100 up: \$52 (151A) and \$62 (151B). Stock. DYNAMIC MEASUREMENTS.

Low-cost multiplier/divider, 4094/15C, using improved version of transconductance circuit technique. Accuracy 1% (after external adjustment) in all four quadrants. 3-dB bandwidth 1.4 MHz. Accuracy drift $\pm 0.1\%/^{\circ}$ C. Power-supply rejection ± 100 mV/V. Output noise 3mV rms. Rated output ± 10 V at ± 5 mA. Input impedance 20 k Ω (X and Y) and 7.5 k Ω (Z). Encapsulated module, $1.8 \times 1.2 \times 0.6$ in. \$35 (1-9). Stock to 4 wks. BURR-BROWN.

High-impedance multiplexer, MP4110, for low source loading and crosstalk in high-speed multiplexing. Operates in single-ended or differential mode. Includes buffered feedback for positive switch control. Suitable for 2-level operation. DTL/TTL circuitry. Electrically and mechanically shielded. Repairable module, 2 × 2 × 0.39 in. Requires ±15 V at 25 mA. \$150 (unit qty). 2-3 wks. ANALOGIC. 484

A/D converter card, DM-721, with 16 line BCD output, overrange bit, and minus-sign bit. Handles 4 full bipolar digits with 100% overrange. Accuracy $\pm 0.02\%$ ± 1 digit. Stability 0.003%/°C. $4-\frac{1}{2}$ × $4-\frac{3}{4}$ in., with 22-pin double-sided edge connector. \$250 (unit qty). 1 wk. DATASCAN. 485

High-speed A/D converter, 6409, for conversion speeds to 250,000 conversions per sec. 9-bit resolution. Unique "capacitance-decoupler" circuit reduces accumulated diode capacitance. TTL logic. Complete with internal reference, clock generator, control logic and data register. Full-scale input ±10 V. Can be "short cycled" for faster con-



version (with lower resolution and shorter word length). "A" version has input amplifier with $100\text{-}\mathrm{M}\Omega$ input impedance. Double PC board, $4.5 \times 2.16 \times 0.75$ in., with single 44-pin edge connector. \$335. Stock. DATA TECHNOLOGY.

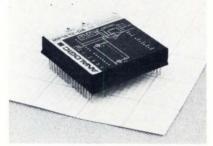
S/D converter modules, ESDC-6 series, with 14-bit resolution. Accuracy ±4 min ±0.9 LSB over full temperature range. Available in 2 versions, for 0 to +70°C (-1) or -55 to +85°C (-3). Accuracy specholds for power-supply variations of

 $\pm 5\%$ and input amplitude or frequency variations of $\pm 10\%$. DTL/TTL output logic. Designed for synchro input of 90 Vrms L-L, 50-60 Hz. Also available in versions for other voltages and frequencies. $2.6\times3.1\times0.8$ in., with separate transformer module 1.5×3.1 in. \$895 (ESDC-6-1 in 1-9) and \$795 (ESDC-6-3 in 1-9). Stock to 4 wks. DDC.

Synchro-to-dc converter, SLD202L, to convert synchro inputs into dc voltage linearly proportional to rotor shaft angle. Accuracy ± 30 min. Input freq 400 Hz $\pm 10\%$ (60 Hz available). Input voltage 11.8 Vrms or 90 Vrms L-L. Input impedance 50 k Ω L-L balanced. Operating temp 0 to +70°C ("A" version) or -55 to +85°C ("B" version). 2.6 \times 2.6 \times 1.5 in. Under \$300 (production qty). Stock to 4 wks. COMPUTER CONVERSIONS.

High-speed D/A converters, DAC-VR series, with output settling time of 2 μ s to within $\pm 0.025\%$ of final value. Accuracy, $\pm 0.01\%$ of F.S., $\pm 1/2$ LSB. Available with word lengths from 8 to 12 binary bits. Full-scale output ± 10 V at 10 mA. TTL/DTL compatible input logic. Operating temp 0 to +70°C. Long-term stability $\pm 0.02\%$ for 6 months. Low-profile plastic case, $2 \times 2 \times 0.4$ in. DIP-compatible pinning. \$229 (12-bit version). Stock to 2 weeks. DATEL.

Fast D/A converter module, DAC-PAC MP1612-DA, with accuracy of 0.01% at speeds to 1 MHz. Resolution 12 bits. All standard codings and output



ranges. DTL/TTL circuitry. Output current 10 mA. Settling time 10 μ s to 1/2 LSB. Offset tempco $\pm 0.01\%$ F.S. \star °C. Range tempco 12 ppm/°C. Shielded. Needs ± 15 -V supply. 2 \times 2 \times 0.39 in. Repairable. \$150 (unit qty). 2 to 3 wks, ANALOGIC: 490

Character-generator card, 8000, to convert 64-character subset of ASCII code to corresponding 5×7 dot matrix. TTL compatible. Complete with memory-address registers, level shifters, ROM, and all clocking and timing. Available for 7-line scan or 5-col scan. PC card, $4-1/4 \times 6-3/4$ in. ELECTRONIC ARRAYS.

TV-display driver, AAT-101, to convert any TV or 525-line video monitor into 256-character alphanumeric display. Modulated output connects directly to TV antenna terminals, and can drive up to 10 sets. Composite video and separated sync signals available for use with video monitors and

cameras. Data can be loaded, read or exchanged asynchronously at rates to 120 char/s. Plug-in PC board. \$695 (2-4). 15 days. ANN ARBOR TERMINALS. 492

Lumped-constant delay lines, Series 25, in 41 different versions with delays from 5 ns to 25 ns in increments of 0.5 ns. Rise times from 1 ns to 2.25 ns. Impedance 75 Ω ±10%. Attenuation 0.1 dB. Distortion 3%. Encapsulated



plastic cases with sizes from 0.5×1.3 \times 0.375 in., to $1.2 \times 1.3 \times 0.375$ in. From \$10 to \$80 (depending on quantity and size). Stock to 3 wks. ENGINEERED COMPONENTS CO. 493

Surface-wave delay lines, consisting of coupled transducer arrays on lithium niobate or quartz substrate. Spacing between adjacent interdigital structures determines fixed delay. Freq range 30-300 MHz, Delay range 0.5 μs to 10 μs. 3-db bandwidth .3%-30% of center freq. Size less than 1 in.³. Insertion loss 10-20 db. Spurious response 25 dB down. Versions available for full military temp, shock and vibration. 6-8 wks delivery for prototypes, DAMON.

Tiny crystal oscillator, X0-2007, in DIP-compatible encapsulated package. Freq range 18 to 25 MHz. Stability ±50 ppm over the range 0 to +50°C. Power requirement +5 Vdc, ±10%, at 22 to 30 mA. TTL-compatible squarewave output. Higher and lower frequencies available at slightly higher cost. \$58 (prototype qty). 2 to 3 wks. TMC SYSTEMS.

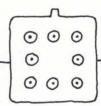
Thick-film LED arrays, LEA-400 series, with GaAs LEDs to provide infrared light sources for paper-tape reading, shaft encoding and other op-



toelectronic applications. Available with from 2 to 12 LEDs in standard DIP cases for plug-in mounting. Configurations mate with company's light-sensor arrays. Custom styles available. Light output up to 1.5 mW (continuous) or 125 mW (pulsed), HEI, 496

(Continued on page 68)

CENTIGHO* The Low Profile .100 Grid Relay



Packaging and Production Engineers please note:

CENTIGRID* Series 112 Relay's 8 leads, spaced on 0.100 centers — all on the periphery of the header — permit direct plug-in convenience on all PC boards. This relay won't be the highest component on the board. It's only .225 high, thereby minimizing board spacing. It's only .370 per side.

Design and Circuit Engineers please note: The CENTIGRID* has the same performance as our TO-5 relays. Coil voltages, in 6 choices, range from 5 to 26.5 VDC.

Using CENTIGRID* Series 112 relays permits compliance to Mil Std. 275B and Mil-P-55110A circuit board specifications without complicated lead spreading.

Space-wise Engineers please note: Ease of installation and inspection makes CENTIGRID* the perfect answer to any packaging density problem.

We're not complacent. We're relay innovators. We built the first relay with single or double diodes for polarity reversal protection.

The first relay with coil transients suppression, and an internal transistor driver. We added internal diode chips for built-in arc suppression, combined it with the internal transistor driver, and made it double as a transapad. That's our TO-5 relay. We built it from the leads up!

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Low-cost opto-isolator, MCT2, consisting of phototransistor and LED in inexpensive plastic package. 6-lead package is similar to DIP but has length of 0.34 in. Voltage isolation 1500 V. Isolation resistance 10¹¹Ω. Typical current transfer ratio 35%. Coupling capacitance 1.3 pF typ. Input voltage 1.5 V. Bandwidth 300 kHz. \$5.85 (1-9). Stock. MONSANTO. 497

Photodiode and op amp, 682, in single TO-5 package. Built-in amplifier reduces size, avoids design problems and

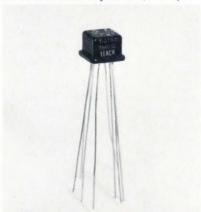


eliminates noise pick-up between detector and amplifier. Circuit contains $40\text{-}k\Omega$ feedback resistor. Amplifier output voltage equals product of photocurrent and feedback resistance. Feedback resistance is chosen to optimize frequency response but can be changed externally if required. \$79.50 (1-9). Stock. ELECTRO-NUCLEAR LABS.

Sensor modules to detect voltage, phase or frequency and actuate internal output relay. Output load can be ac or dc with currents to 10 A. Output relay can be specified to meet MIL-R-5757 or MIL-R-6106. Packages have 1-in. square headers. Operating temp -55 to +125°C, LEACH.

Switches & Relays

Square "TO-5" relay, T, with all-welded construction. Dpdt. 100,000 cycles



at 1 A. -65 to +125 °C. 0.09 oz. LEACH. 500

Rf latching relay, RFKL, in half crystal can. Dpdt. One or two poles terminated in 6 in. RG196 or in user-specified termination. Pull-in coil power 250 mW for 3 ms. Contacts carry 200 W (1 A) rf, switch 75 W. VSWR 1.1:1 to 500 MHz, insertion loss 0.16

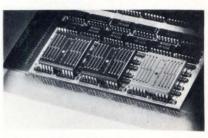
dB typ, crosstalk -50 dB typ. HI-G. 502

Half-crystal-can relay. Form A, B or C, 10 A 28 Vdc. -65 to +125°C.



Takes 20-g 2-kHz vibration, 50-g shock. BRANSON. 501

Low-profile reed relays, Tri-R, to mount on DIP centers. 0.5 in. high.



 0.8×1.25 in. with 14 leads max, 1.3 \times 1.25 in. with 24 leads max. AL-LIED CONTROL. 503

Low-cost reed relays with 10-W 200-V form A contacts. 39¢ (high volume). ELECTRONIC APPLICATIONS, 504

"Integrated" reed relay, IR2, with no glass capsule. Reeds, coil, coil terminations sandwiched in ceramic/glass polymer. Alumina substrate provides heat sinking. Chrome-plated steel cover for mag shielding. Form 1C or 2C. KAM.

505

Mercury-film relays, 9000, in 14-lead DIP. Insensitive to mounting position. 2.5-ms operate. 1- μ V thermal noise. Low-level loads and power loads can be switched alternately. 50-million operations, 50-mΩ initial contact resistance, varying ±1 mΩ over life, regardless of load (1 μ A to 1 A). Latch or non-latch. \$10 (production quantities). FIFTH DIMENSION. **506**

PC-mount rotary switches, T-Bird 212, with 8 terminals. 1/2-A 28-Vdc, 3/4-A 115-Vac contacts. 8- to 10-m Ω circuit resistance. Single wafers, less detent, from 21ψ . (2500-up). CTS. **507**

No-thumbwheel "thumbwheel," with one pushbutton to add to displayed number, one button to subtract. Deci-



(Continued on page 70)



For the engineer whose responsibility is checking out incoming precision components, the new Fluke 3330 Programmable Constant Current/Voltage Calibrator will shorten your day and heighten your nights. For the first time, computer programmed checkout over a wide range of voltages and currents is available with an off-the-shelf low priced quality instrument.

The Fluke 3330 is unique. It can be operated in either a constant current or constant voltage mode. Modes can be changed without turning the unit off. Voltage range is 0 to 1000 volts in three ranges with 10% overranging. Voltage accuracy is $\pm 0.005\%$. Resolution is 0.1 ppm. Stability is 25 ppm per month. Line and load regulation are 2 ppm of range. Ripple and noise are less than 50 μ v. Voltage trip is adjustable from 1 v to 1000 v. Output current is 100 ma in the 10 and 100 v ranges and 50 ma in the 1000 v range.

In the constant current mode, ranges are 0 to 100 ma in three ranges with 10% overranging. Accuracy is ±0.01%. Resolution is 1 ppm. Stability is 50 ppm/month. Line and load are 2 ppm of range. Compliance voltage is 1000 volts on the 1 and 10 ma ranges and 500 volts on the 100 ma range.

Crowbar effect through a programmable relay shorts output to limit voltage while changing loads.

Programmable functions are output range, mode, level and polarity, voltage and current limit, crowbar, and standby/operate. Programming time is tens of milliseconds. Price is \$2,995.

For full details write or call us today.

Fluke. Box 7428, Seattle, Washington 98133. Phone: (206) 774-2211. TWX: 910-449-2850.

In Europe, address Fluke Nederland (N.V.), P.O. Box 5053, Tilburg, Holland. Phone: (04250) 70130. Telex: 884-50237. In the U.K., address Fluke International Corp., Garnett Close, Watford, WD2 4TT. Phone: Watford 27769. Telex: 934583.

PRECISION TESTING AND CALIBRATION MADE EASY...

or how the new Fluke programmable constant current, constant voltage calibrator goes to work calibrating and testing precision instruments, semiconductors, resistors and sub-assemblies.





KEPCO'S LOW-COST VOLTAGE REGULATOR with CROWBAR



Kepco's new group of "BKF" modules are for circuit designers working with I-C's. Men who'll appreciate its simplicity of design—made possible by its integrated amplifier and reference on a *plug-in* "DIP"; experienced designers who've learned from experience the need for an overvoltage crowbar.

MODEL	VOLTS	AMPS	PRICE
BKF 5-3	5.0 ±10%	0-3	\$129.00
BKF 5-5	5.0 ±10%	0-5	148.00
BKF 12-1.4	12.0 ±10%	0-1.4	129.00
BKF 12-2.4	12.0 ±10%	0-2.4	148.00
BKF 15-1.2	15.0 ±10%	0-1.2	129.00
BKF 15-2	15.0 ±10%	0-2	148.00
BKF 24-0.8	24.0 ±10%	0-0.8	129.00
BKF 24-1.2	24.0 ±10%	0-1.2	148.00
BKF 28-0.6	28.0 ±10%	0-0.6	129.00
BKF 28-1	28.0 ±10%	0-1	148.00

For these engineers, Kepco offers the BKF modules in two power ratings, 15 watts and 25 watts, adjustable ±10% with a special built-in overvoltage crowbar and protected by a reentrant current overload circuit.

For complete specs-write Dept. DA-11



131-38 SANFORD AVE. • FLUSHING, N.Y. 11352 (212) 461-7000 • TWX #710-582-2631

Circle 132 on Inquiry Card

mal or BCD output. \$4.75 (decimal). DURANT. 508

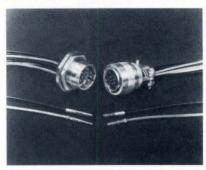
Tiny snap-action switch, Mini-Mite in $0.25 \times 0.3 \times 0.1$ in. case. Form C. 2 A 125/250 Vac, 30 Vdc. Pin plunger or various lever styles. McGILL. **509**

16-key keyboard with standard key, DC-16K, or low-profile, DC-16P, with each key closing to common via bounce-free elastic diaphragm. 12 V 20 mA max. "Infinite" life. 3-oz force for key model, 1 oz for key-less low-profile "Touch" model. \$1 per position (production quantities). DATANETICS.

Fully encoded solid-state keyboard, CDK, with up to seven rows including space bar. Typical typewriter format or keypunch type. 7- or 8-bit ASCII coding with or without parity. Two-key rollover protection. One- to four-mode operation. \$100 (1000-up). CONTROL DEVICES. 511

Packaging/Hardware

Circular connectors, Bantam Trim Trio, with removable crimp coax and power contacts. 4 to 48 contacts for



AWG 14 to 30 conductors. Glassfilled DAP insert. Bayonet coupling. BURNDY. 512

Ceramic-substrate connector for 1 × 2-in substrates. 40 contacts on two rows on 50-mil staggered centers. BeCu bellows contacts in DAP or phenolic body. Dip-solder termination tails, WINCHESTER. 513

Both-ways DIP socket to accept 14- or 16-pin DIPs with leads down or up (in "dead-bug" configuration). IC retained in rather than on socket. Wiping contacts. ROBINSON-NUGENT. 515

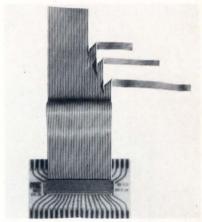
Insulated shorting jacks for 40-mil pins on 0.2- or 0.4-in. centers. Black,



red or blue polypropylene insulator. CAMBION. 516

Smaller DIP sockets with 2- or 3-level Wire-Wrap terminals. Bodies mount on centers of 0.4×0.8 in. (14 pin) or 0.4×0.9 in. (16 pin). SAE. 514

Round-conductor flat cable, Scotchflex, with "zip" construction for easy break-out of one or more conductors.



100-ft, rolls of up to 50 AWG 24-30 solid or stranded conductors in PVC insulation. 3M. 517

Diamond heat sinks for thermal conductivity six times that of copper, low electrical conductivity, low coefficient of expansion. Cylindrical disks or triangles. Any color. ENGINEERED MATERIALS.

518

Dry-transfer PC patterns, Jot Draft, in line of 128 pads, connector patterns, logic symbols, component outlines, etc. Samples available. DATAK.

519

R&D PC-etching kit with etchant, catalyst, 25 square inches of one-sided copper-clad, roll of pressure-sensitive black tape and tape symbols. HOULE. 520

Vacuum pickup. Lab-69, with interchangeable metal or Teflon tips in sizes from 0.5 to 6 mm. \$20 (1-24) with three metal tips. LABTRON.

Ultrasonic wire bonder, 2000 Bondsonic, with monitor to detect bad bonds and bonder malfunction. 45° microscope permits full view in deep packages. GTI. 523

Turns-counting dials, DFA Fairdial, with flip-lock lever for 25 in.-oz torque



to prevent accidental rotation. Resolution 1 × 10⁻³. 1-oz. FAIRCHILD. 524

PC engraver, Directron, in desk-top version, for making PCs directly and

automatically by scanning original drawing on cylinder with blank copperclad. For boards to $12-\frac{1}{2} \times 5-\frac{1}{4}$ in. Lines and spaces to 10 mils. \$87.50/mo rental. GRAPHIC ELECTRONICS.

efficiency at 300 A. Six models at 7.5 to 300 Vdc. Ripple 10 mV. Regulation 0.05% + 10 mV. Overvoltage and short ckt protected. Current limiting and remote sensing. TC 0.03% + 0.5 mV/°C. Imput $208 \pm 10\%$ V 57-63 Hz. LAMBDA. 542

Power Supplies

Bipolar module, 11C040, for reference input to control systems. \pm 10 V at 10mA. Stability 0.01%/8 hr and drift 0.01%/°C. Z out 0.1 Ω . Ripple and noise 1 mV rms. \$54.75, TIDEWATER TECHNOLOGICAL.

Low-cost power module, 5055, for 5 Vdc at 10 A. Regulation 0.5% for line and load combined. Overvoltage crowbar and short-ckt protection. Remote sensing provided. Ripple 3 mV rms or 5 mV peak. \$149. HI-G. 540

Op-amp supply, PM555, with separate transformer and regulators for each output. Output \pm 15 Vdc at 100 mA. Operates from 115 V 60 to 400 Hz. Line and load reg 0.03% and 0.02% respectively. Ripple and noise 1 Vrms.



TC 0.02%/°C. Temp range -25° to 71°C. Packaged in potted module 2.25 \times 3.50 \times 1.00 in. \$41.95. COMPUTER PRODUCTS. 538

Digitally-controlled voltage sources 6130B and 6131B, for fast acting



source of dc or low-frequency power. Voltage magnitude, polarity, range and current limit programmable. Coding 8421 BCD or 15-bit binary. Current limit 3-bit binary. 6130B for -50 to +50 V at 1 A. 6131B for -100 V to +100 V at 5 A. Second range on both models -10 to +10 V. Accuracy: low range 1 mV and high range 10 mV. Line and load reg 0.5 mV lo range and 5 mV hi range. Can be used as bipolar amp. \$1800. HP. 541

High-current supply, LB-720 series, for use in computer main frame. 80%

Test Equipment

Logic probe, with adjustable "1" and "0" thresholds. Detects open circuits, positive pulses, negative pulses and dc levels. Powered from ±3 to ±30 V.



Withstands ± 150 V for 30 seconds and ± 50 V indefinitely. Detects pulse widths from 5 ns to 1 ms. Input Z 20 k Ω . \$99.50. ACRON. 555

Non-destructive power-transistor tester, model 33, for measuring safe operating region. Tests either pnp or npn devices by applying variable $V_{\rm CB}$ and

I_E for a prescribed time. If breakdown occurs power is removed and failure light comes on. Various power supply options available. Test time variable from 10 ms to 10 seconds. \$7500. TEST EQUIPMENT CORP. 556

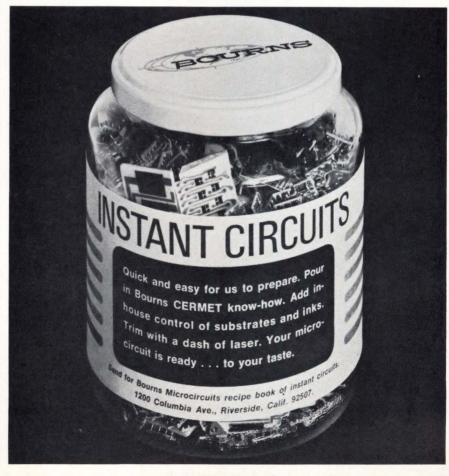
Programmable dc voltage standard, 381, with output voltage accuracy/stability to within 0.003%/year. Output voltage up to ± 122.221 volts. Current source limit 100 mA and current sink limit 10 mA. Load and line regulation 0.0005% of setting or 25 μ V. TC (0.0002% of setting + 1 μ V/°C.) Noise and hum 30 μ V rms. Needs parallel-entry BCD commands. COHU.

Low-cost pulse generator, 701, with rise and fall times less than 3 ns. 10



Hz to 8 MHz in six overlapping ranges. Output voltage 0 to +5 V across 50Ω . Pulse width 80 ns to 100 ms in six ranges. Duty factor 85%. \$160. DYTECH RESEARCH. 558

Dual-channel pulse generator, 8010A, with two independent channels. Channels can be used separately or com-(Continued on page 72)



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bined. Individual control of rise and fall times makes it possible to generate specialized waveforms. Pulse width 20 ns — 1 second, rise and fall times 10 ns — 1 second, amplitude +5 V, freq 1 Hz to 10 MHz with internal or external trig. \$1925. HP.

Sweep and marker generator, 159D, for 1 Vrms into 75 Ω over a 300 kHz-300 MHz range. Sweep width 200 kHz-300 MHz. Sweep modes: variable 0.01-1000 Hz, line lock 50 or 60 Hz, manual, cw and external mod. RF attenuator provides up to 79 dB. RF output AGC'd ±0.25 dB. Pulse markers are available in the PM7650 plug-in, which offers eight individually switched crystal marks at specified freqs. \$950. KAY. 560

Differential voltmeter, A-72A, with 0.1 µV or 0.0002% stability. Five ranges from 110 mV to 1100 Vdc. Six readout dials with best resolution 0.1 μV. Operates from line voltage or internal-rechargeable batteries. Zener-ref



oven comes to full operating temp in 2 minutes, \$1125, MEDISTOR.

Time interval meter, 915, with 5-digit display and 1-µs or 1-ms resolution. Range is either 0-99,999 µs or 0-99,999 ms. Accuracy ± 1 count \pm osc error. Sensitivity 1/V pk. Polarity and slope selectable by front-panel switch. Input Z 10 $k\Omega$ shunted by 30 pF. Freq standard 1-MHz temperature-compensated crystal oscillator with TC of 2 × 10-7/°C. \$555. CMC.

Real-time analyzer, SD301B, for looking at spectrum changes in the range from 0.03 Hz to 20,000 Hz. Input range -5 dB to -35 dB. Output gain to 26 dB. Calibration of frequency through internal freq standards. Sweeprate feedback for plotter mode of operation which has three sweep rates (30s, 60s and 21/2 min). SPECTRAL DYNAMICS.

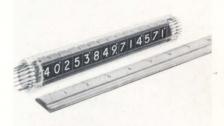
Lock-in amplifier, 124, for measuring amplitude and phase of weak signals buried in noise. Signals from 1 mV to 500 mV in range from 0.2 Hz to 210 kHz. Ref signal int or ext. In external mode the 124 locks onto and tracks a signal over a frequency range of 100:1. Time constants to 300 seconds with provision for longer time constants. \$2850. PAR.

Circuit-board analyzer, 1200P, for testing digital circuits. Uses controlled programming, for checks. Contains light banks, Nixie display, "stop-onfault" feature, meters, probes, power supplies, frequency generator (50 kHz to 100 kHz) and a 5-Hz square-wave source. BESA SCIENTIFICS.

Resistance-tolerance bridge, 57-2200, for displaying % deviation of an unknown resistance from a standard six decade resistance. ± percent deviation on front panel meter. Resistance range 1 Ω to 10M Ω (model 57-2200-1) and 1Ω to 1 M Ω (model 57-2200-2). Accuracy 0.1%. SOLARTRON. 566

Display Devices

Cold-cathode numerical indicator, ZM-1200 Pandicon, for displaying 14-digit numbers. 7 inches long and 1-1/6 inches in diameter. Each digit 3/8 in. high and 17/64 in. wide. Character brightness 600 candles/meter2. Power



1.5 to 2 watts. Accepts NBCD codes and is compatible with DTL and TTL. \$27. AMPEREX.

Digital counting unit, with 7 segment readout. 3/4 in. high. TTL integrated logic. Count rate 2 MHz. Can be viewed in direct sunlight. \$32.50 TEPRO.

Bi-directional counter, UD-2, for use with incremental shaft encoders, pulse generators, and photoelectric pickoffs. 6 digit range. 2-channel pulse or square wave input. 0 to 5 MHz rate. BCD and direction-sensing outputs. \$260. THE-TA.

Vertical indicator, S2000 series, with vertical yellow-white tape display. S 2000-888-1 3-wire synchro input. S 2000-888-2 0-5 Vdc input. S 2000-



888-3 same as -2 with potentiometer output. Requires 26 V at 400 Hz, 3.5 W and 28 Vdc at 0.5 A. 67/8 in. long \times 1½ in. wide \times 6% in. high. GAP.

DPM, 1294, with 41/2 digit display. TTL logic and time sharing circuitry. $10\mu V$ sensitivity. Z in 10 M Ω . Response time 0.7 seconds. Accuracy 0.05% of reading ± 1 digit $\pm 10\mu V$. Dual slope integration. Plug-in Nixies. Repairable ckt boards. Ten standard V and I ranges. WESTON.

Data Handling

Disc-memory systems, M5000 series, for "mini" and "midi" computers. Access time 8.5 ms, with transfer rate of 1.82 MHz. Head-per-track design. Storage capacities 250,000 bits (M5008), 500,000 bits (M5016) and 1,000,000 bits (M5032). Data tracks 8 (M5008), 16 (M5016) or 32 (M5032). 3 pre-recorded clock tracks. Overall dimensions 8.5 in. dia × 6 in. \$2200 (M5008) \$2500 (M5016) and \$3240 (M5032). 60-90 days. MAGNAFILE.

Extended memory unit, 9101A, to increase capability of company's 9100-series calculators. Has 10-k bipolar-transistor IC ROM that provides high-speed capability. Also includes diode ROM that provides basic control of sequences in larger ROM and controls read/write cycles of core memory in calculator. System provides additional 248 registers for calculator. Allows up to 3472 extra program steps. \$3690. Available September. HP. 549

On-line terminal, AJ841, designed to replace IBM 2741. Includes 2-charac-



ter buffer for handling bursts of up to 17 char/s. Can also be used off-line as general office typewriter. Built-in modem. Acoustic adaptor available. Uses MSI ICs. Plug-in PC boards allow simple maintenance. ANDERSON JACOBSON. 550

Digital synchro display, 1841, to accept 2-speed (1:1 and 36:1) synchro position information and provide 5-digit angle display. Uses no rotating mechanisms or optical devices (except readout tubes). 2 display ranges: 0 to



 360° and 0 to $\pm 180^{\circ}$, with same zero reference. High immunity to input noise allows long input leads without line drivers or amplifiers. Data display can be triggered internally or externally. Options include 8421 BCD output and adjustable zero-reference offset. \$2400 (plus options). 6-8 wks. SCIENTIFIC-ATLANTA.

Low-cost digital printer, 5055A, to provide permanent record of data from instruments that have BCD outputs. Up to 10 columns of data at 10 lines per sec. Individual, changeable, 16-character print wheels (1 per column). Prints in ink on regular paper or without ink on pressure sensitive paper. Continuously rotating ink roller. Accepts ±8421 BCD data at TTL-compatible levels. Half-rack width. Height 6 in. \$1150. Stock. HP. 551

Character generator, CG-100, for use with company's Statos-5 digital printer/plotters. Allows electrostatic recorder to function as on-line printer, using standard ASCII code inputs. Provides 126 characters per line in "print" mode. 2 type fonts available with characters in 1 of 4 possible orientations. Max print rate 1800 lines/min (226,800 char/min). \$3975. VARIAN.

Work station, DL-333, for use with Teletype terminals (ASR-33, 32 and 35). Handles all winding and unwinding functions for both perforator and



reader. Consists of electric winder, center-feed unwinder and storage cabinet. Available with optional extra reel for data speed transmissions. Uses new Teletype 8-½ in. split reel. \$130. 30° days. DATA-LINK. 554

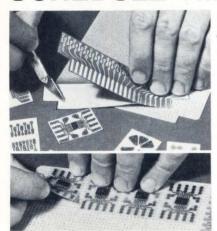
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Compact helium-neon laser, 3076H, with CW output of 3 mW (TEM₀₀

(Continued on page 74)



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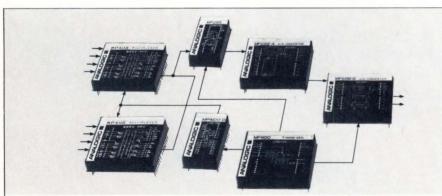
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mode), Cold-cathode coaxial discharge tube. Rugged design. Hermetically sealed tube and housing. Output wavelength 632.8 nm. Length of laser head 12-1/2 in. Complete with power supply. \$415. HUGHES. 543

Stabilized CO₂ laser, 941, with polarized output of 3 W (TEM₀₀ mode). Wavelength 10.6 μm. Sealed plasma tube, cooled by tap water at flow rate of about ½ gal/min. Laser head operates in vertical, horizontal or inverted



orientation. Available accessories include heat exchangers, Q-switches, attenuators and modulators. \$3,890. SYLVANIA. 544

Miniature tape heads, DKS series, for use in digital cassette recorders. Close track-placement tolerance of ± 0.002 in. eliminates need for tunnel erase and tunnel write techniques. Available in versions for read-after-write applications. Improved shielding minimizes crosstalk. Glass-filled housings eliminate "short-turn" losses. From \$2.65 to \$69.50. MICHIGAN MAGNETICS.

Tiny axial blower, Micro-Kool, for concentrated cooling of electronic components. Available in versions for bulkhead mounting, PC-board end mount-



ing and PC-board side mounting. Basic motor operates on 6 Vdc but can be adapted to 12- or 24-Vdc circuits. Power consumption approximately 0.8 W. Delivery 4-6 ft³/min. 15/16 in. dia × 1-3/16 in. Approximately \$13.95 (depending on type and qty). Stock to 2 wks. HICO. **546**

Compact synchronous motor, 86100 series, with torque of 7 oz-in at rotor shaft. Speed 300 rev/min. Operates from 115 Vac at 50 Hz. Fast start/stop eliminates need for clutches in many applications. Selection of 11 different gear trains available, for speeds from 1 thru 150 rev/min. Electrically reversible. NEMA configurations. Stock. A. W. HAYDON.

New Literature

Rf connectors in 162-pg Ben- Dry electrosensitive recording dix catalog. 400

MOS ICs in 24-pg National Semi reliability report. 401

PC connectors in Elco 56 pager and rack/panel connectors in 32 pager.

"Designing with Chopper-Stabilized Op Amps," 18-pg Analog Devices tech article.

ICs and other components in 60-pg TI condensed catalog and peripheral interface cir-404 cuits in 6-pg app note.

Pulsed-rf measurements in HP 16-pg app note and phase measurements to 15 MHz in 405 4 pager.

Capacitors in three Sprague tech articles. 406

Beryllium oxide semi packages in National Beryllia 4-pg bro-

MOS FETs in three Amelco data sheets.

Machine-applied pins, plugs, receptacles in Amp 24 pager. 409

Sequential logic testing in 410 Teradyne 8 pager.

Microwave tubes in Raytheon 48-pg condensed catalog. 411

Ferrite memories in RCA cross reference to products of six other vendors. 412

Pressure-sensitive copper patterns for PCs in Bishop Graphics data. 413

Instrument Rental Handbook in pocket folder with handy guidelines. 414

Electrical pollution in first issue of Elcor newsletter. 415 Mullard short forms.

in 16-pg Fitchburg manual. 416

3D scope displays in Optical Electronics app notes. 417

Time-delay relays in four A. W. Haydon bulletins. 418

A/D conversion in Datel handbook.

Semis in Siemens 32 pager. 420

High-voltage capacitors in Energy Labs 48 pager.

Specifying LC filters in Cambion 10-pg tech article. 422

4-pg Delay lines in Daven buyer's guide. 423

Determining capacitor inductance in Capacitor Specialists 9-pg tech article. 424

Monolithic memories in Cogar 14 pager. 425

"Hybrid Microelectronics Review," 4-pg newsletter from publisher of same name. 426

Audio spectrum analysis in first issue of "plain-English" Testronic house organ. 427

"Picopower" comparator/relays in DDC data. 428

Wirewound resistors in Ward Leonard 20 pager. 429

PC self-stick patterns in Brady 24 pager.

Metal-film resistors in Airco Speer 24-pg designer's guide.

Optoelectronic products in first

issue of Schweber newsletter. Variable active filters in three

Rockland app notes.

Zeners and IR detectors in 434

Unusual Literature

Spectrum Analysis Note 1

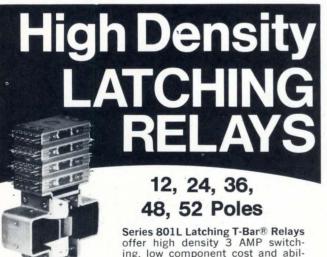
Ronald Tipton, Virginia Tipton Testronic Development Lab. It's a different approach to a

complex problem. Rather than try to treat audio spectrum analysis in a single comprehensive work, the authors (Continued on page 76)





Circle 139 on Inquiry Card



ing, low component cost and ability to maintain circuit integrity during power failure. Bistable operation, driven in

both modes . . . ideal where power drain by large relay switching arrays would strain power supplies or generate undesirable heat. Gold plated rhodium interface contacts available for dry circuit switching.

· Also environmentally or hermetically sealed

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eight-page notes. They justify this procedure on the grounds that the "bite-size" pieces are easier to read and easier to write.

The bites are easy to swallow. The style is superbly informal and easy-going, completely disarming a reader who's accustomed to pompous and dry lecture-style presentations.

Quite naturally and casually, the authors start their series by raising the question, "Why do analysis?" then answering it, first, simply, "to find out something about the frequency content of a time waveform, then, in greater depth.

They move on to discuss an ideal analyzer - one with many contiguous, ideally rectangular, narrowband filters in parallel. They advance to a discussion of ideal signal sources and the concepts of spectral density and degrees of freedom. They summarize neatly, provide a very clear but brief glossary, add a few references, then quit.

Borrowing a technique popularized in old-time movie serials, they offer a brief preview of what they'll cover in the next installment. The technique is still effective.

For a copy and, perhaps, a subscription to the entire series, circle 435.

GaAs Lite Tips

Monsanto

This is rather spotty. A 48 pager, it includes nine short articles, of uneven quality, written by five authors. After one gets used to the tiny type in the text, one finds a mixture of circuit-applications articles and articles that are

ESP 40 Feb '70 Monsanto SPECIAL PRODUCTS

elected to write a series of essentially descriptions of Monsanto products.

A few of the applications articles (like the one on pulsed operation of LEDS, another on constant-brightness light sources and still another on a modulated infrared-beam control system) can be useful with light-emitting diodes from several vendors but others can be used only with Monsanto LED arrays.

One can't fault the authors here since some of the products (like two different seven segment LED readouts) are available exclusively from Monsanto.

The articles are well written with different degrees of thoroughness.

For a copy, circle 440.

Laminated and Molded **Bus Bars**

Eldre Components

This looks like a straight technical description and commercial pitch for Eldre's bus bars. And that's what's obviously intended. But it's more than that. The information, with minor modification in a few cases, applies to bus bars made by any vendor.

The author fills this little 16 pager with loads of fine technical information and design considerations. He provides working equations an engineer can use to determine his own bus-bar requirements. And if a man wants to use another vendor's bus bars, he can use the same equations by simply plugging in different values for dielectric constant, permeability and conductivity.



The author includes two tables. One provides handy conversions from round wire to flat bus bar, with dimensions, current-carrying capability and dc resistance. The other compares the resistance, inductance and capacitance of twisted wire and bus bar.

Bus bars, laminated or otherwise, are not the most fascinating components used by engineers. Nevertheless, a man fighting noise in his equipment would do well to study this booklet

For a copy, circle 438.

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EEE readers have voted M. J. Prickett winner of the \$100 Savings Bond for June. The winning circuit design is "Peak detector for very narrow pulses." Mr. Prickett is with the Naval Electronics Lab Center, San Diego, Calif.

Fast-recovery integrator with adjustable threshold

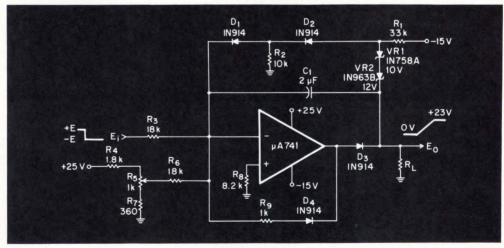
Circuit Design No. 9

by Kin S. Wong
Interstate Electronics
Anaheim, Calif.

BY PREVENTING the op amp from saturating we can make the recovery time of this integrator approximately equal to the amplifier's slew rate. Diodes D_1 and D_2 are normally biased off until the output voltage E_o exceeds the zener voltage of regulators VR_1 and VR_2 .

Further increase of the output voltage forward biases D_1 and D_2 . The output is then clamped to the sum of the zener and diode voltages, which is below the amplifier's saturation level.

Resistor R_2 bypasses the diode leakage current to the summing junction when D_2 is reverse biased. The adjustable threshold voltage and the input



Two diodes and two zeners clamp this integrator's output to below the op amp's saturation voltage, making for fast recovery. All resistors are 5%, 1/4-W carbon comps.

signal are summed at the inverting input.

Diode D_g rectifies and D_4 decouples the amplifier output to provide a circuit output that is always positive. Resistor R_g provides gain compensation to

prevent amplifier oscillation. The polarity of E_o may be made negative by reversing all diodes, the reference input and the zener supply.

reverse biased. The adjustable is always positive. Resistor R_g With the component values range of threshold voltage and the input provides gain compensation to shown and using +25-V and -10 V.

-15-V supplies, the integration time constant (C_1R_3) is 35.6 ms and the output is clamped at +23 V. The output linearity is $\pm 1\%$ and the threshold range of this circuit is -3 to -10 V.

(EEE cannot assume responsibility for circuits shown nor represent that they are free from patent infringements.)

Single NAND package improves one-shot

Circuit Design No. 10

by James E. McAlister Texas Instruments Government Products Div. Dallas, Texas

THE OUTPUT PULSE of the typical NAND one-shot of Fig. 1 is often subject to oscillation and pulse-width instability. Further, the range of pulse widths is sometimes quite limited.

The NAND one-shot in Fig. 2 overcomes these difficulties. The 1- kΩ feedback resistor eliminates the tendency to oscillate and the additional output gate provides more squaring of the output pulse.

All four NAND gates are

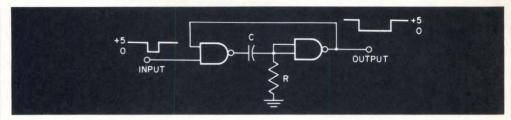


Fig. 1. The typical NAND one-shot suffers the likelihood of output instability and oscillation.

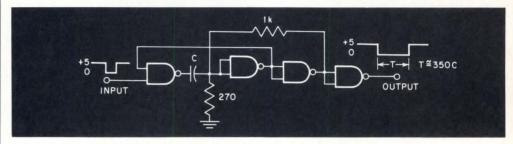


Fig. 2. Improved NAND one-shot provides cleaner, more stable output.

With these gates, the output | to T = 350 C. width, T, equals 1.3 RC and, part of a TI SN7400 package. with $R = 270\Omega$, this simplifies than 30 ns can initiate an out-been used successfully.

put. Timing capacitors ranging Input pulse widths longer from 100 pF to 100 µF have

Simple gyrator for L from C

Circuit Design No. 11

by Anthony C. Caggiano Ridge, N.Y.

THE ADVENT OF low-cost IC amplifiers has made it practical to use the gyrator circuit to provide inductive effects without the usual limitations of coils. The gyrator is a circuit portional to the reciprocal of its load impedance. So the input to a gyrator loaded with a capacitor looks like an inductor with higher Q than available in the usual commercial inductor.

Figure 1 shows a simple gyrator with a capacitive load. The gyrator (in dashed lines) includes two amplifiers with gain A, one inverting and one noninverting. Each amplifier whose input impedance is pro- has a Z_1 , Z_2 and R_L represent-

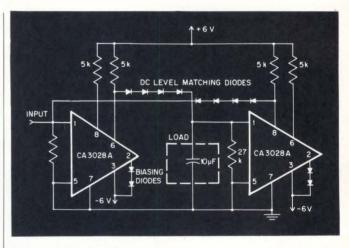


Fig. 2. This specific gyrator, with a 10-μF load, effectively forms a 12-µH inductor.

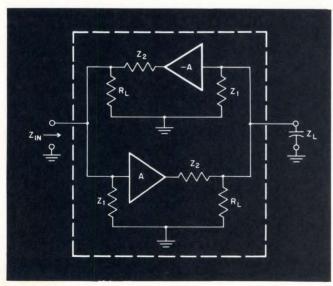


Fig. 1. This is a generalized gyrator circuit with a capacitive load.

ing, respectively, its input im- | pedance, output impedance and load resistance.

The input impedance of a gyrator loaded with capacitor C is

$$Z_{in} = \frac{P(P^2 + G^2 + \omega^2 C^2) + j_{\omega} G^2 C}{(P^2 + G^2)^2 + P^2 \omega^2 C^2}$$

where
$$P = \frac{1}{R_{\perp}} + \frac{1}{Z_{\perp}} + \frac{1}{Z_{2}}$$

and $G = A/Z_2$. The Q of the loaded circuit is

$$Q = \frac{\omega G^{2}C}{P(P^{2} + G^{2} + \omega^{2}C^{2})}$$

which has an approximate kHz.

maximum of G/2P at an angular frequency

$$\omega = \sqrt{\frac{P^2 + G^2}{C^2}}.$$

Figure 2 shows two RCA CA3028A ICs in a gyrator loaded with a 10-µF capacitor. In this circuit, the amplifiers had $A=1000, Z_1=2~\mathrm{k}\Omega,$ $Z_2=12~\mathrm{k}\Omega$ and $R_L=5~\mathrm{k}\Omega.$ These values give an effective and the state of the state of

tive 12-µH inductor which is quite constant over a range from 10 Hz to almost 1 MHz. The Q varies from 1 at 10 Hz to a maximum of 500 at 10

Long-delay timer

Circuit Design No. 12

by Robert W. Hilsher Bendix Towson, Md.

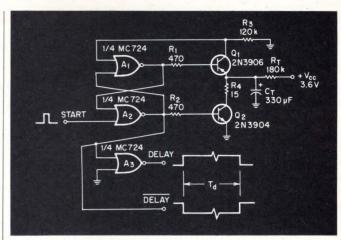
PRODUCING LONG DELAYS using the low voltage from which ICs operate can be difficult. The circuit shown provides delays up to more than one minute.

The delay period commences when a start pulse is applied to the R-S flip-flop formed by A_1 and A_2 . Q_2 turns off, allowing R_T to provide charging current for the timing capacitor C_T .

When the voltage across C_T exceeds the $V_{\rm be}$ of Q_I plus the level set at its base by the IC, Q_I turns on, resetting the flipflop, and terminating the delay period.

With a $V_{\rm ce}$ of 3.6 V the delay time $T_d = R_T C_T$ and, with the values given, T_d equals 60 seconds. Resistor R_s is used to provide some noise immunity, but it may be omitted if noise is not a problem. If used, R_s should equal 0.7 R_T to guarantee proper reset action.

Since loading A_i 's output will greatly affect the delay period, A_s is used to provide a buffered complementary output.



This circuit provides long delays, even with the low voltages used for ICs.

Low-component-count digital comparators

Circuit Design No. 13

by A. Kochergin Lockheed Missiles and Space Sunnyvale, Calif.

THE MOST STRAIGHTFORWARD method of comparing the state of a counter with a number selected by thumbwheel switches is to compare the outputs of

counter flip-flops and digital switches with an Exclusive-OR, as in Fig. 1. This approach is adequate if the number of switches is small. But as the quantity goes up, the logic becomes more complex since each switch requires a comparator.

A simpler solution is to add diodes to the thumbwheel switches to form an AND gate

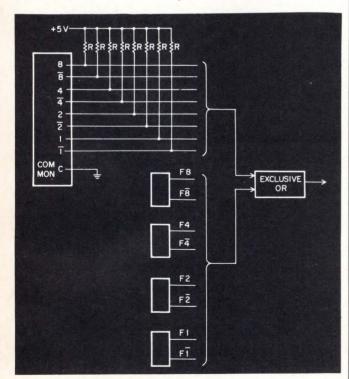


Fig. 1. The Exclusive-OR approach is the most direct one for comparing the output of a digital switch with that of counter flip-flops. But when several switches are used, each requires a comparator.

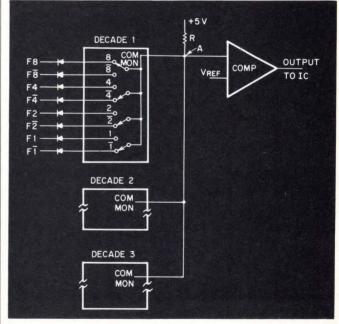


Fig. 2. In this approach, AND-gate diodes, driven by counter flip-flops, perform the comparisons

and drive this configuration with the flip-flops of the counter (Fig. 2). The output will be high (+5 V) only when the counter matches the setting of the switch (count 8 in the example). As long as there is a mismatch, at least one diode will provide a path to ground, keeping the output low.

While there is a mismatch, the output (A in Fig. 2) will be about ±1 V. That's the low output of the IC, typically 0.4 V, plus the forward drop of the

diode. This exceeds the highest "0" that most ICs will tolerate (+0.8 V typ).

To avoid erroneous circuit operation, one should place a voltage comparator in the line and use a reference of 2 to 3 Vdc. The comparator output will then be high only when the output is at +5 V.

If many decade switches are used, each decade is driven by the corresponding counter decade and the commons tied together to form one output.

Want ads

Dear EEE:

I have long admired your efforts to meet the needs of the EE profession and wonder if you have ever considered the creation of "want ads" for those "impossible" specifications that can be met but are not listed in the company catalogs. I find that after contacting salesmen at several large suppliers, and talking to the engineers within my own organization who specialize in working with these components, I reach the conclusion that the component needed does not exist. At the same time I have the nagging suspicion that someone, somewhere, does indeed make such a component and is looking for a customer.

As an example of such a "want ad" I submit the following request: Wanted: A resistor-capacitor combination of about 10k Ω and 0.001 to 0.01 μ F for which there is a 95 percent confidence that 99 percent of the RC products will meet the following specifications: (1) The temperature coefficient is ± 20 ppm/°C from 0 to 60°C. (2) The aging is less than 0.1 percent in 20 years. (3) The aging includes the effects of a 0 to 95 percent relative humidity. The resistor ratios and capacitor ratios - must track to the same specifications. The matched pair should cost under \$5 in lots of 1000, but this is negotiable. Application: audio frequency active filters (milliwatt power).

As I visualize its use, an engineer who has exhausted all of his own resources would write or telephone such an "ad" to you and thus invite any manufacturer who would meet them to

reply by phone or mail.

I am serious about needing this RC product and therefore it must be understood by the salesmen that I do not want their short form catalogs and I do not want to hear about their product if it only meets some of my specifications. In fact, my hope is that an alert salesman will talk to his product engineer(s) and have them contact me.

"Want ads" would serve as a means of advertising by the customer and as such would confirm the manufacturers marketing research. In fact, why not call it the Matchmakers Column? D. Hilberman

Bell Telephone Laboratories Holmdel, N.J.

Missed printer. We missed Keltron's DM-400 in the survey of lab digital printers in the April issue. Using the Seiko printing mechanism, the unit is designed for 5-1/4 in. half-rack mounting or an instrument case. A variety of plug-ins allows up to 21-column redblack printing with full programming and storage capabilities. Prices start at \$825 for a 5-column printer.

The company, based in Waltham, Mass., also makes the DM-300, for up to 12 columns and the DM-1, for up to 8 columns.

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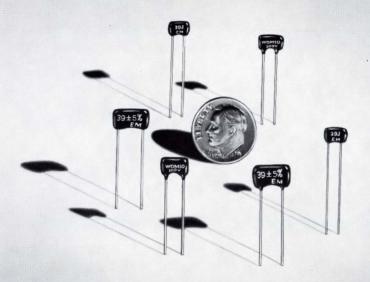
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		F	85pF thru 200pF
	1	C	1pF thru 400pF
DM10	10 100VDC	D, E	27pF thru 400pF
		F	85pF thru 400pF
		C	1pF thru 1500pF
DM15		D, E	27pF thru 1500pF
		F	85pF thru 1500pF
		C	1pF thru 120pF
DM5	1	D, E	27pF thru 120pF
		F	85pF thru 120pF
		C	1pF thru 300pF
DM10	300VDC	D, E	27pF thru 300pF
		F	85pF thru 300pF
	1	C	1pF thru 1200pF
DM15		D, E	27pF thru 1200pF
		F	85pF thru 1200pF
		C	1pF thru 250pF
DM10		D, E	27pF thru 250pF
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