A MORGAN-GRAMPIAN PUBLICATION

Digital Design

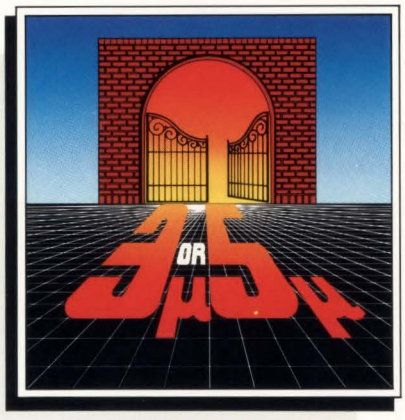
COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 8/83

Fault Tolerant Architectures

- Minicomputers
- DEC-Compatibility
- Graphics Boards
- Display Processors

VOL. 13
NO. 8

THE UNIVERSAL FAST CMOS GATE ARRAY SOLUTION. THREE OR FIVE MICRON TECHNOLOGY! 360 to 2400 GATES!



There are many sound reasons to select Universal as your CMOS gate array partner. Here are a few:

Advanced Technology—We don't buy technology from others—we make it! For toggle rates to 25MHz, our 5μ process serves nicely. For frequencies beyond, our 3μ process is employed. In either case, you're dealing with a company in full command of the technology behind its arrays.

Broad Array Selection—No other company has a more useful selection of arrays. There are 14 different arrays logically sized between 360 and 2400 gates available. Large or small, fast or faster performance, we have an array to serve your needs.

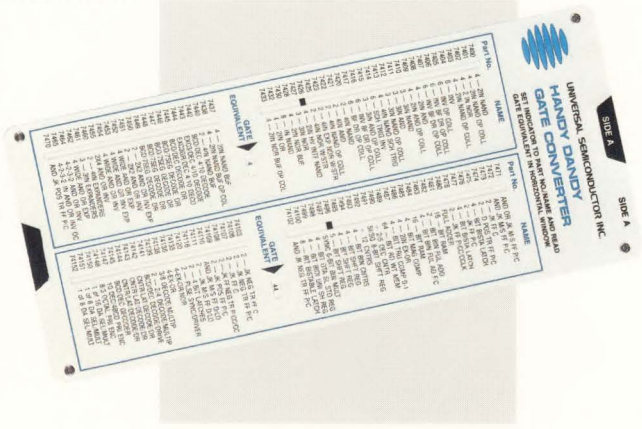
Type	Gates	Size	Speed	Pads
1S03 or 5A	360	118 × 140	50 or 25MHz	44
1S03 or 5B	540	132 × 167	50 or 25 MHz	58
1S03 or 5C	720	159 × 167	50 or 25 MHz	64
1S03 or 5D	960	161 × 208	50 or 25 MHz	70
1S03 or 5E	1200	188 × 208	50 or 25 MHz	74
1S03 or 5F	1500	188 × 244	50 or 25 MHz	80
1S03 or 5G	1800	202 × 230	50 or 25 MHz	92
1S03 or 5H	2400	232 × 252	50 or 25 MHz	110

Complete CAD Support—No other company has more sophisticated CAD tools. Every Universal array is completely simulated and verified prior to converting it to silicon. And that's not all:

- Macrocells are placed automatically
- Macrocells are routed automatically
- Logic and circuit functions are fully simulated
- The design is completely verified.
- Test program automatically generated

Fast Turnaround—For arrays of 800 gates or less, we guarantee an 8-week turnaround. For larger arrays, add one week per 150 gates. And because of our powerful CAD tools, when you get your prototypes, they'll work and perform to spec!

Start Today—What size array do you need? With our Handy Dandy Gate Counter, you can convert your TTL or LSTTL design to CMOS gate equivalents quickly. In less than an hour, you'll know exactly what size array will do your job. *Write* or *call* today for your *FREE* Handy Dandy. We'll also send you a full color brochure describing our products and services.



Write 43 on Reader Inquiry Card

UNIVERSAL SEMICONDUCTOR INC.

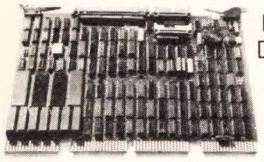
1925 Zanker Road San Jose, CA 95112 (408) 279-2830

Q-BUS* DISK CONTROLLERS

You can't beat the configuration flexibility DILOG's family of Q-BUS disk controllers provide you for systems integration. They interface the full line of DEC LSI-11 through 11/23 PLUS computers and wide range of today's high technology Winchester drives.

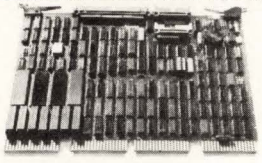
DILOG further insures this flexibility with exclusive Universal Formatting™...so you can change drives as newer models become available...all without changing on-board components or adding cost...thus making DILOG a real price/performance value.

SMD COMPATIBLE WINCHESTER DISK CONTROLLERS



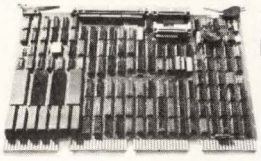
Model DQ228

- RM02/RM05/RM80 emulation
- 22-bit addressing
- Universal Formatting™
- 56-bit ECC
- RSX-11, RSTS and UNIX
- Drive capacities to 600MB



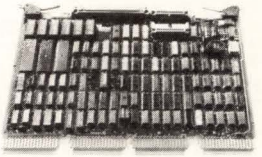
Model DQ215

- RK06/RK07 emulation
- 22-bit addressing
- Universal Formatting™
- 56-bit ECC
- RT-11, RSX-11, RSTS and TSX-Plus**
- Drive capacities to 160 MB



Model DQ214

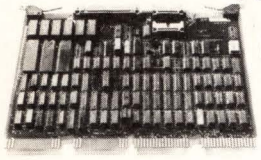
- RL01/RL02 emulation
- 22-bit addressing
- Universal Formatting™
- 56-bit ECC
- RT-11, RSX-11 and RSTS
- Drive capacities to 40 MB



Model DQ202A

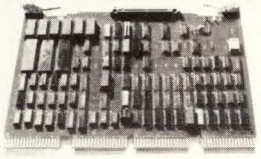
- RP02/RP03 emulation
- Universal Formatting™
- RT-11, RSX-11, RSTS and TSX-Plus
- Drive capacities to 160 MB

PROPRIETARY WINCHESTER DISK CONTROLLERS



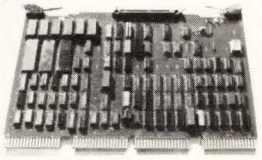
Model DQ404

- SA4000 I/O compatible
- RL01/RL02 emulation
- RT-11, RSX-11 and RSTS
- Drive capacities to 40 MB



Model DQ413

- Priam I/O compatible
- RP02/RP03 emulation
- RT-11, RSX-11 and RSTS
- Drive capacities to 154 MB



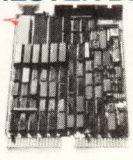
Model DQ414

- Priam I/O compatible
- RL01/RL02 emulation
- RT-11, RSX-11 and RSTS
- Drive capacities to 40 MB

ST506/412 WINCHESTER DISK CONTROLLERS

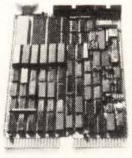
Model DQ615

- ST506 I/O compatible
- RK06/RK07 emulation
- Enhanced 32-bit ECC
- 22-bit addressing
- RT-11, RSX-11, RSTS and TSX-Plus



Model DQ634

- DMA Systems Micro Magnum compatible
- 22-bit addressing
- RL01 emulation
- Enhanced 32-bit ECC
- RT-11, RSX-11 and RSTS



Model DQ614

- ST506 I/O compatible
- RL01/RL02 emulation
- Enhanced 32-bit ECC
- 22-bit addressing
- RT-11, RSX-11, RSTS and TSX-Plus

In addition, DILOG also offers you a full range of removable disk and tape controllers for Q-BUS and UNIBUS* (PDP/VAX) computer systems.

Write or call for complete details and prices of DILOG's full line of Q-BUS and UNIBUS mass storage Disk and Tape Controllers.

*Trademark Digital Equipment Corporation
**Trademark s&h computer systems, inc.

DILOG

DISTRIBUTED LOGIC CORPORATION

12800 Garden Grove Blvd.
Garden Grove, CA 92643
(714) 534-8950
TLX 681399

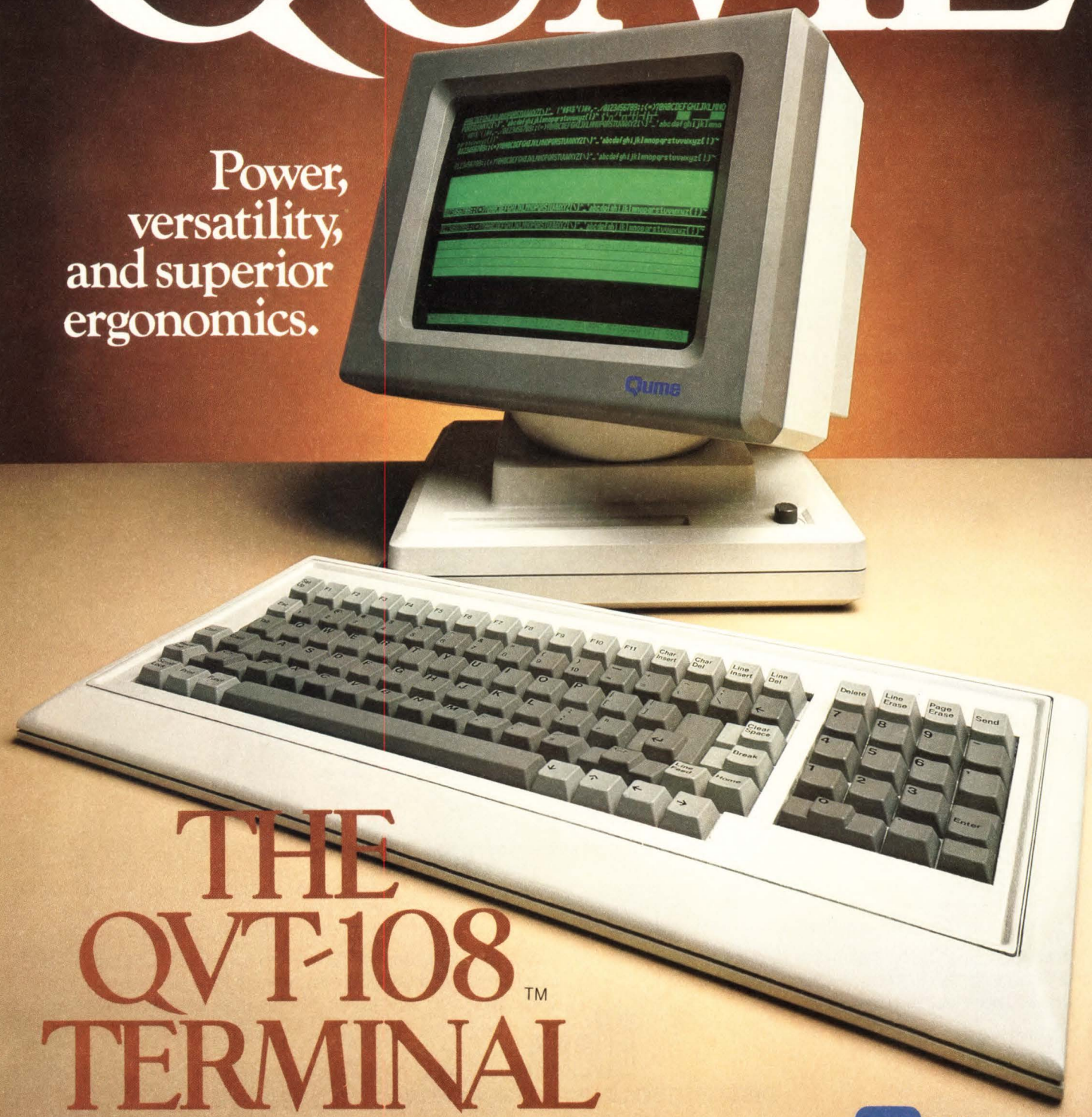
64-A White Street
Red Bank, NJ 07701
(201) 530-0044

12 Temple Square
Aylesbury, Buckinghamshire
England HP 20 # 2QL
(0296) 34319 TLX 837038

Write 1 on Reader Inquiry Card

QUME

Power, versatility, and superior ergonomics.



THE QVT-108™ TERMINAL

Qume®
A Subsidiary of ITT

QVT-108

The Great Emulator.

Qume's new QVT 108™ CRT terminal emulates Televideo models 925, 920 and 912, making it a perfect fit for operators familiar with any of these terminals. It more than matches the Televideo 925 with sophisticated features like 11 function keys, 12 editing functions, 25th status line, a menu set-up mode, two full pages of screen memory, and many other standard features.

The QVT 108 takes up minimal workspace, and operators will love its ergonomic design: a non-glare green or amber screen with full tilt and swivel, a big 9 x 12 character matrix to minimize eyestrain, and a low-profile, detached keyboard.

Engineered and built to Qume's exceptional reliability standards, the QVT 108 is backed by our six-month warranty and a nationwide service network. Features include:

• Local or duplex editing • 11 Function keys (22 functions total) • Bidirectional auxiliary port • Two pages of screen memory • Line drawing graphics character set • Tilt/swivel, non-glare, green screen (amber optional) • 9 x 12 character cell resolution, 7 x 9 character size • Detached, low-profile typewriter style keyboard with numeric pad • 24 lines x 80 characters with a 25th status/menu/user-programmable line • Screen-saver time out (an inactive terminal shuts off its screen after fifteen minutes with no screen data loss) • 5 video attributes; blink, blank, reverse video, underline, and half-intensity • Televideo model 925 code compatible • Emulations: Televideo 925 and 912/920 • Self test • Time of day • Monitor mode • Switching power supply (efficient operation and low power consumption)

Display Format
24 lines x 80 characters
25th status/set-up/user programmable line

Character Formation
7 x 9 matrix in a 9 x 12 cell

Displayed Character Set
96 ASCII characters, 32 control character symbols, and 15 line-drawing symbols

Editing (Local and Duplex)
Cursor: up, down, left, right, home. Character/line insert and delete, erase to end of line/page, tab, back tab, alternate page.

Communications Interface
EIA RS232-C, optional current loop (active or passive)

Communications Protocols
DTR and/or XON/XOFF

Communications Modes
Full or half duplex, block line or block page; 7 or 8 data bits

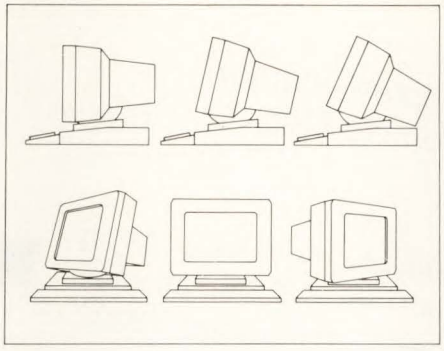
Baud Rates
16 selections from 50 to 19.2k

Auxiliary Port
Bidirectional. Modes: parallel, transparent, screen copy. EIA RS232-C

Screen
Tilt/swivel, 12-inch diagonal, non-glare green (optional non-glare amber)

Character Attributes
Blink, blank, underline, reverse video, half intensity

Keyboard
Detached, low-profile (home row 30mm from work surface), alphanumeric keys, 14-key numeric pad, 11 function keys (22 functions with shift), defeatable autorepeat and key click, 12 editing keys. Print, set-up, and scroll lock keys



Fields
Protected and unprotected

Parity
Odd, even, mark, space, none

Screen-Saver
Screen shuts off after 15 minutes of inactivity without data loss

Screen Memory
Two pages

Set-Up Mode
Menu-style preserved in non-volatile memory (lithium battery with 7-year life)

Power Supply
Switching-type (low power consumption)

Options
Amber screen
14″ screen
20mA current loop
Special character sets

Command Set
Televideo 925 compatible

Emulations
Televideo 925
Televideo 912/920

Power Requirements
95-125 VAC
200-264 VAC
50/60Hz, 30W

Dimensions
Keyboard 1.5″(H) x 18″(W) x 8″(D)
Display 14″(H) x 13″(W) x 12″(D)

Weight
Keyboard 3 lbs., display 19 lbs.

Command Codes

Address cursor, row, column	ESC =rc
Address cursor, page, row, column	ESC – prc
Auto page on	ESC v
Auto page off	ESC w
Back tab	ESC I
Bell	CTRL/G
Block mode on	ESC B
Transparent print on	ESC ‹
Transparent print off	ESC a
Carriage return	CTRL/M
Character delete	ESC W
Character insert	ESC Q
Clear all column tabs	ESC 3
Clear all to half intensity blank characters	ESC ,
Clear all to nulls	ESC *
Clear column tab	ESC 2
Clear unprotected to blank characters	ESC ; or CTRL Z or ESC +
Clear unprotected to nulls	ESC :
Conversation mode	ESC C
Copy print mode on	ESC @
Copy print mode off	ESC A
Cursor down	CTRL/V
Cursor home	CTRL/-
Cursor left	CTRL/H
Cursor right	CTRL/L
Cursor up	CTRL/K
Disable bidirectional port	CTRL/T
Disable XON/XOFF control	CTRL/N
Disable status line	ESC h
Display user line	ESC g
Duplex edit on	ESC l
Enable bidirectional port	CTRL/R
Enable XON/XOFF control	CTRL/O
Erase to EOL with blanks	ESC T
Erase to EOP with blanks	ESC Y
Field tab	ESC i
Keyclick off	ESC ‹
Keyclick on	ESC ›
Line delete	ESC R
Linefeed	CTRL/J
Line insert	ESC E
Load user line	ESC f (text) CR
Local edit on	ESC k
Lock keyboard	ESC #
Monitor mode off	ESC u or ESC X
Monitor mode on	ESC U
Next page	ESC K
Newline	CTRL/—
Normal video	ESC d
Previous page	ESC J
Print page	ESC P
Protect mode off	ESC ′
Protect mode on	ESC &
Read cursor, page, row, column	ESC /
Read cursor, row, column	ESC ?
Reverse video	ESC b
Reverse linefeed	ESC j
Screen, blank	ESC o
Screen, normal	ESC n
Select termination character	ESCx4(nn)
Send line all	ESC 6
Send line unprotected only	ESC 4
Send message all	ESC s
Send message unprotected	ESC S
Send page all	ESC 7
Send page unprotected only	ESC 5
Set column tab	ESC 1
Set cursor attributes	ESC .(n)
Set printer termination character	ESC p(n)
Set video attribute	ESC G(n)
Tab	CTRL/I
Unlock keyboard	ESC ″
Write protect off	ESC (
Write protect on	ESC)
Load time	ESC sp $n_1n_2n_3n_4n_5$
Read time	ESC sp 2
Special graphics off	ESC %
Special graphics on	ESC $

Authorized Qume Distributor/Dealer

Qume Corporation
2350 Qume Drive
San Jose, CA 95131

Qume Corporation
1754 Technology Drive
Suite 110
San Jose, CA 95110
(408) 942-4111

Qume Corporation
6011 Bristol Parkway
Suite 150
Culver City, CA 90230
(213) 410-1458

Qume Corporation
1820 East Gary Avenue
Suite 104
Santa Ana, CA 92705
(714) 957-4040

Qume Corporation
Shamrock Park Office
Suite 110G
2323 South Troy Street
Aurora, CO 80014
(303) 752-3000

Qume Corporation
909 Wilmette Road
Unit B-2
Palatine, IL 60067
(312) 991-7250

Qume Corporation
5335 Far Hills Avenue
Suite 107
Dayton, OH 45429
(513) 439-0469

Qume Corporation
1925 Westridge Drive
Irving, TX 75062
(214) 659-0745

Qume Corporation
20 Mayfield Rd.
Edison, NJ 08837
(201) 225-5005

Qume Corporation
19 Crosby Drive
Bedford, MA 01730
(617) 275-3200

Qume Corporation
4319 Covington Highway
Suite 212
Decatur, GA 30035
(404) 284-8500

GERMANY
QUME GmbH
Eicheisstr 31
4000 Düsseldorf 13
West Germany
PH: 0211743016

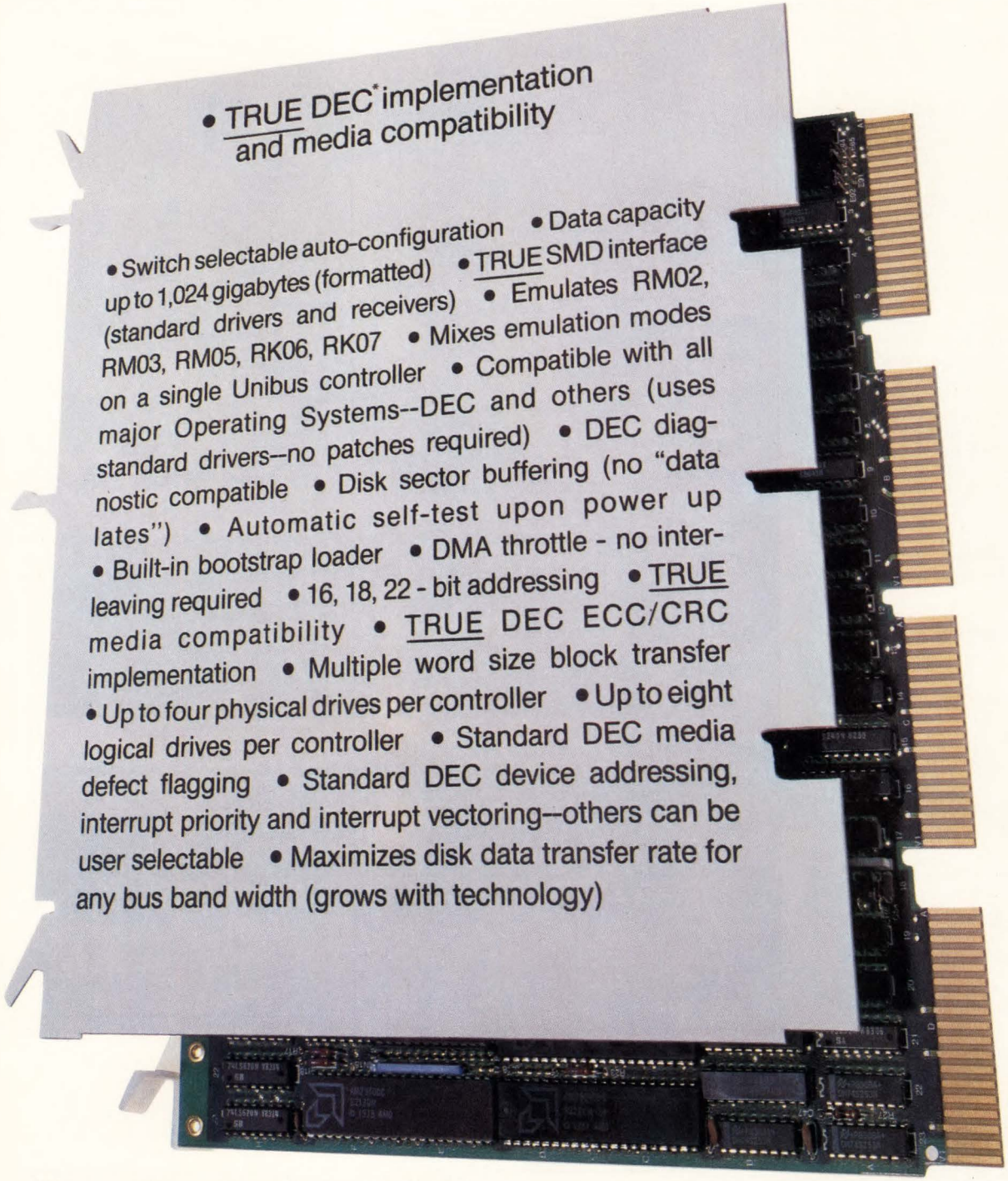
ENGLAND
QUME (UK) Ltd.
1 Bridgewater Close
Reading, Berkshire UK
PH: 734-584-646

FRANCE
QUME GmbH
Bureau de Liaison France
20, rue Thiers
92100 Boulogne, France
PH: (1) 6082334

CANADA
QUME Canadian Office
207 Place Frontenac
PTE Claire
Quebec, Canada H9R4Z7
(514) 695-3837

Qume®
A Subsidiary of ITT

20 major capabilities together for the first time on a single SMD controller!



Sometime a picture isn't as good as 10,000 words.

*TM Digital Equipment Corp.

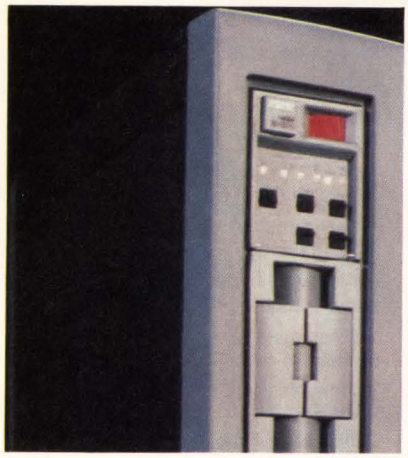
MDB SYSTEMS INC. | *THE WORLD'S LARGEST INDEPENDENT MANUFACTURER OF COMPUTER INTERFACES.*

1995 N. Batavia St., Orange CA 92665
(714) 998-6900 TWX 910-593-1339

Circle **4** for LSI-11 Circle. **6** for PDP-11

AUGUST 1983/VOL. 13, NO. 8

Digital Design



p. 28 *(Photo courtesy DEC)*

p. 48 *(Photo courtesy Honeywell)*

p. 70 *(Photo courtesy Intel Corp.)*

Cover

Shown on the cover are the 2-chip General Data Processor and single chip Interface Processor, part of Intel Corp.'s 5-chip iAPX 432 Fault Tolerant Multiprocessor system. Center photo by Rudi Legname. Cover graphics by Henry Jackson, Benjamin Morse, Inc.

Published monthly thirteen times a year with two issues in November. Second class postage paid at Boston, MA and at additional mailing offices. POSTMASTER: Send address changes to Morgan-Grampian Publishing Company, 1050 Commonwealth Ave., Boston, MA 02215. ISSN 0147-9245

COMPUTERS/SYSTEMS

Industry Spotlight: DEC-Compatible Market 28
DEC's solution to the increasing demand for software has led to new approaches to third-party products and software vendors.

Display Processors—The Design of Computer Graphics Systems 36
Enhanced semiconductor technology is forcing designers to improve display performance.

Minicomputers Face Stiff Competition 48
Minicomputer modification results in increased performance while maintaining hardware and software compatibility with earlier models.

Fault Tolerant Architectures 70
The key goals of a fault tolerant system are to maintain data integrity and maximize system uptime.

Unix Leads To Greater Flexibility 92
Use of a Unix operating system allows software development to expand easily.

Graphics System Design 26
Low Cost Automated Drafting—The Next Paperwork Revolution

Innovative Design 96
Communication Software Ties Development Systems To Minis

PERIPHERALS

Self-Testing Components Pinpoint Network Faults 84
Sophisticated diagnostics are being designed into an increasing number of products.

Innovative Design 96
Cartridge Tape Subsystem Provides Fast Backup/Restore Performance

COMPONENTS

Innovative Packaging Improves Color Graphics Boards' Resolution 64
Custom LSI devices and new packaging techniques solve PCB space constraints.

Self Diagnosis Of Single-Chip Computers 88
A key answer to the testing dilemma is to use the on-chip processor to test itself.

Graphics System Design 24
Color Graphics Display Uses 8K × 8 iRAMs

Application Notebook 103
Achieve High Speed Data Acquisition With A Fast ADC and DMA

News Update 10
Washington Report 12
Technology Trends 15
Market Trends 23
Product Index 98
Reader Service 99
Calendar 118
Advertiser Index 118
New Products 108
New Literature 116

Digital Design

Publisher	Jeffrey C. Hoopes
Editor-in-Chief	Jerry Borrell
Production Editor	Debra A. Lambert
Technical Editor	Dave Wilson
West Coast (408) 371-9620 Technical Editor	Doug Eidsmore
West Coast (213) 981-3300 Technical Editor	Mike Cashman
Associate Editor/ Directory Editor	Julie Pingry
Departments Editor	Mary Rose Hanrahan
Editorial Assistant	Andrea Coville
International Electronics Editor	Ron Neale
International Computers Editor	Eric Wignall
Contributing Editor Data Communications	Walter Bolter, Ph.D.
Contributing Editor Graphics Systems	Thomas DeFanti, Ph.D.
Contributing Editor Software	Andrew Rubel
Washington Correspondent	Anne Armstrong
Publication Services Manager	Charlotte King
Production Manager	Jon Buchbinder
Art Director	Richard D. Sarno
Associate Art Director	Tilly Berenson
Assistant Art Director	Maureen Bernardini
Production/Graphics	Martha Watjen, Judy Osburn, Joan Scheffler, Vete Saulenas, Don Schaff, Paul Christo
Promotion Manager	Elaine Bull
Research	Helen Obermayer, Peter Micheli
Circulation Manager	Hugh Dowling
Circulation	Sarah Binder, Gary Byrne, Deborah Goldstein, Lynda Neue
General Administration	Karen Melanson, Nancy Deveau, Dianna Lynn Reed, Leslie Saunders, Debra Sturm

Group Publishing Director
Albert J. Forman

Advertising Sales

Northeast: John C. Moon **(617) 232-5470,** 1050 Commonwealth Avenue, Boston, MA 02215

Middle Atlantic: Barbara L. Smith **(212) 340-9700,** Morgan-Grampian Publishing, 2 Park Avenue, New York, NY 10016

Southeast: Rich Santos **(404) 393-2505,** 1224 Mt. Vernon Road, Dunwoody, GA 30338

Midwest, South Central: Hank Bean **(312) 346-4611,** Morgan-Grampian Publishing, 2 North Riverside Plaza, Chicago, IL 60606

Northwest: Cassandra Ewing, Ralph Petersen **(408) 371-9620,** 1901 S. Bascom, Suite 1005, Campbell, CA 95008

Southwest: Pam Rock **(213) 981-3300,** 15910 Ventura Boulevard, Suite 1215, Encino, CA 91436

Telemarketing/Northwest: (408) 371-9620, 1901 S. Bascom, Suite 1005, Campbell, CA 95008

Telemarketing/Southwest: (213) 981-3300, 15910 Ventura Boulevard, Suite 1215, Encino, CA 91436

The Lundy UltraGraf® is absolutely the fastest draw in the West or anywhere else.

This is the fastest, most intelligent 3-D computer graphics workstation available. The superlatives would seem to indicate a high price, too. But the Lundy UltraGraf workstation is surprisingly low cost considering its unmatched performance features.

At Lundy we don't develop technology for its own sake; we develop it to meet your needs. In the case of 3-D computer graphics workstations, you needed more speed, higher IQ, larger display and easier operation. UltraGraf delivers all four.

The Lundy UltraGraf is first when it comes to speed and IQ.

Keys to UltraGraf's instant response are a high speed microcomputer and a high resolution vector display, both developed by Lundy.

Besides these features, we've designed more intelligence into the workstation, so UltraGraf places fewer demands on your host computer.

The result is unmatched interaction while freeing up your host computer to concentrate on other operations.

19 × 15 inches sets a new screen standard.

UltraGraf's 21-inch CRT has the largest viewing area—19 × 15 inches—in the industry. Fast vector drawing and minimum operator time produce easy-to-read, flicker-free images. Spot size is only one ten thousandths of an inch, which produces remarkable crispness and clarity.

Lundy UltraGraf sets 3-dimensional standards.

Furthermore, UltraGraf is easier to use. You send a picture only once, instead of resending over and over as with many other systems. And you have local storage of all control functions for the interactive input devices. This provides maximum input flexibility, with minimum keyboarding.

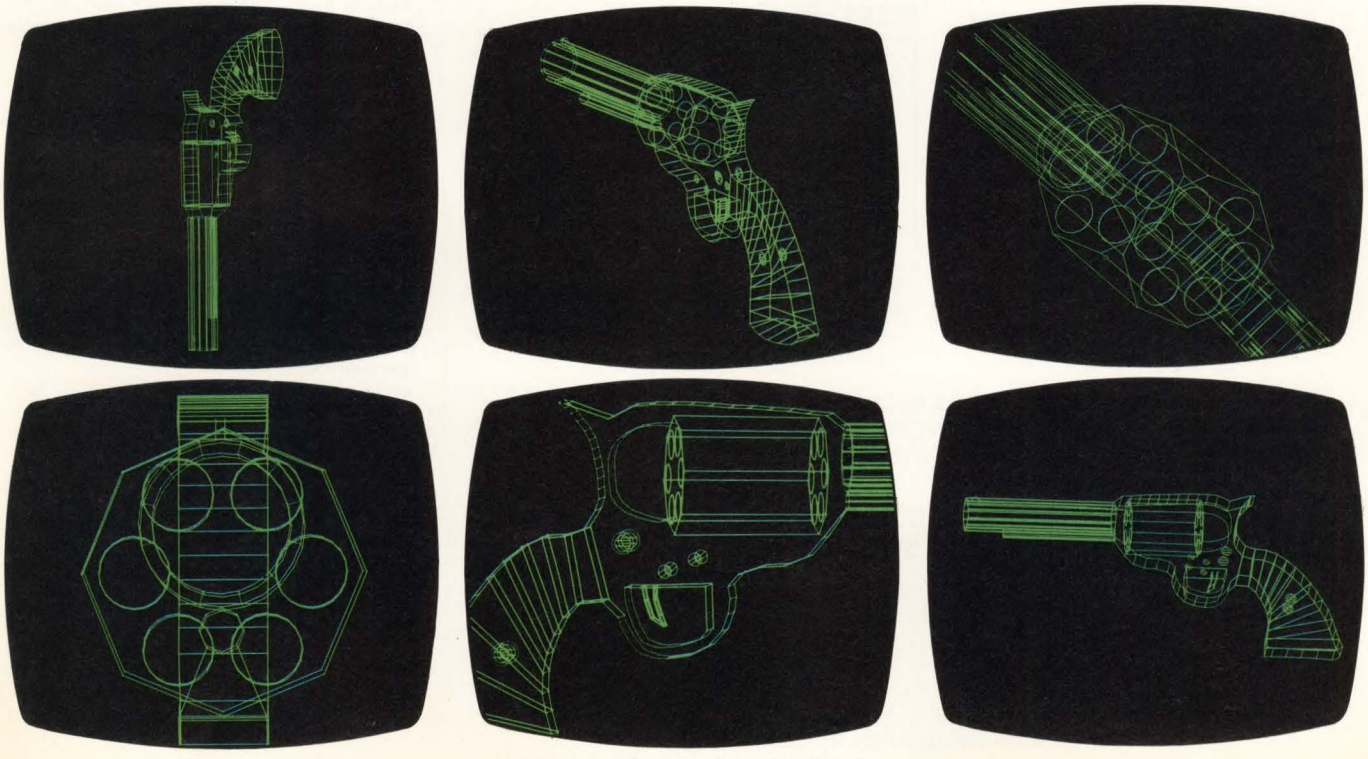
Lundy helps you see more in graphics.

When you take a close look at our graphics terminals, service, support, software, systems capability, enhancements—and our company—you'll understand why Lundy can help you see more in graphics now and in the long term.

For more information about our 3-D UltraGraf, or other CAD/CAM products, write Lundy Electronics & Systems, Inc., Glen Head, New York 11545, or call: (516) 671-9000.

LUNDY®

Get the draw on sluggish productivity with Lundy's UltraGraf. Shown here are six views of a six shooter generated in just a matter of seconds.



Write 7 on Reader Inquiry Card

Digital Design

EDITORIAL, SALES, AND CIRCULATION OFFICES
Digital Design
1050 Commonwealth Avenue
Boston, MA 02215
Telephone: (617) 232-5470

MORGAN-GRAMPIAN

CORPORATE HEADQUARTERS

Morgan-Grampian Publishing Company, 2 Park Avenue, New York, NY 10016, (212) 340-9700. Domenic A. Mucchetti, President.

EXPOSITIONS GROUP
Morgan-Grampian Expositions Group, 2 Park Avenue, New York, NY 10016 (212) 340-9700. Robert Poggi, Director.

The following is a list of conferences sponsored by the Expositions Group:

ATE West	CADCON East
CADCON West	ATE Central
ATE Northwest	CADCON Central
ATE East	

In addition to Digital Design, Morgan-Grampian publishes the following in the United States: Circuits Manufacturing • Electronic Imaging • Electronics Test • Computer & Electronics Marketing

New Publication Development
H.G. Buchbinder, Director

Morgan-Grampian also publishes the following in the United Kingdom: Electronic Engineering • Control & Instrumentation • Electronic Times • What's New in Electronics • What's New in Computers.

DIGITAL DESIGN serves the manufacturers of computer-related OEM products. This includes primary computer and systems manufacturers, systems integrators, components and peripheral manufacturers, integrating OEM's and commercial end users. These companies manufacture products used to control machinery, equipment and information in manufacturing, material processing, machine tools, packaging, health care, defense, data processing, communications, instrumentation, and scientific and business operations.

ABP BPA

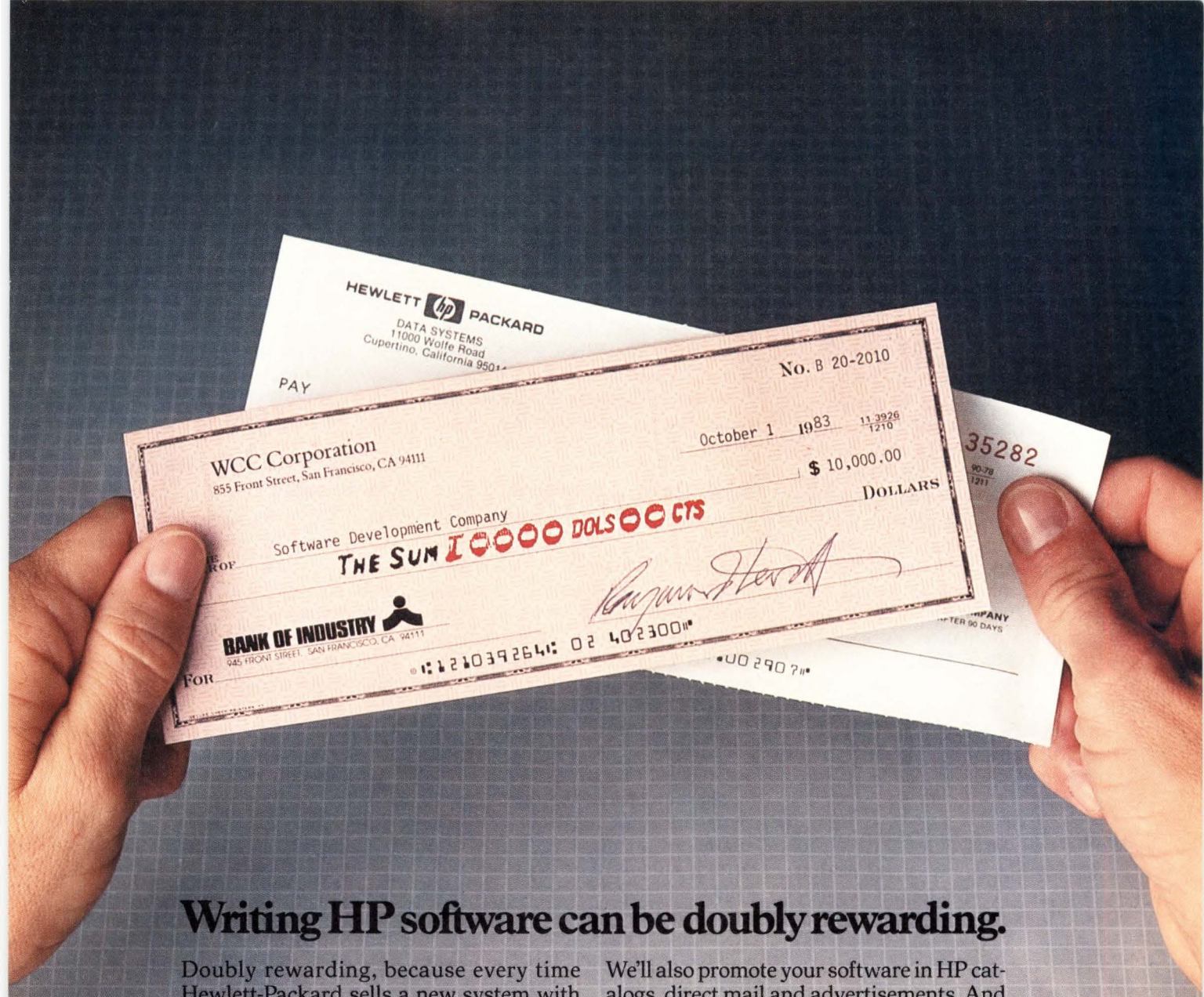
SUBSCRIPTION POLICY

DIGITAL DESIGN is circulated only to qualified research, development and design engineers and engineering managers primarily responsible for computer products and systems in OEM plants. To obtain a complimentary subscription, request (on company letterhead) a qualification card from Circulation Director. For change of address, attach old address label from recent issue to new company letterhead or note. Send this plus request for new qualification card to:

Circulation Department
DIGITAL DESIGN
1050 Commonwealth Avenue
Boston, MA 02215

Subscription rates: non-qualified subscribers (US and Canada) — $35/yr; foreign — surface mail — $45; air mail — $70. Single copies — $4.

DIGITAL DESIGN solicits editorial material and articles from engineers and scientists. Contributors should submit duplicate manuscripts typed with two spaces between lines. All illustrations should be clear; components on all schematics and line drawings should be labeled. The editors assume no responsibility for the safety or return of any unsolicted manuscripts.



Writing HP software can be doubly rewarding.

Doubly rewarding, because every time Hewlett-Packard sells a new system with your software, you'll not only get a check from the customer, but one from HP as well!

As thanks for writing software for our systems, we'll give you a bonus of 30% of your software's sales price—up to 6% of the net HP system's price. That could mean $3,000 on a $50,000 system... or as much as $30,000 on a $500,000 system. And you'll get it *every time a new system is sold with your software.*

We won't tell you what kind of program to write. What industry to write it for. Or even specify the system. Our only restriction is that, to qualify for the bonus, your software must sell for at least $10,000.

Of course, extra cash isn't the only incentive. To help you get started, we'll sell you a development computer at a 40% discount. We'll also promote your software in HP catalogs, direct mail and advertisements. And you'll have the benefits of being associated with HP—one of the worldwide leaders in computing systems. A company whose products range from widely-used business computers, like the HP 3000, to one of the world's most advanced 32-bit computers, the HP 9000.

If you'd like to learn more, write to Hewlett-Packard, Attn Gwen Miller, Dept. 91173, 19447 Pruneridge Avenue, Cupertino, CA 95014. In Europe, write to Henk van Lammeren, Hewlett-Packard, Dept. 91173, P.O. Box 529, 1180 AM Amstelveen, The Netherlands.

We'll give you all the details on our HP Plus Software Supplier program. And all the reasons why it will be rewarding for *you* to develop software for HP.

HEWLETT PACKARD

Write 54 on Reader Inquiry Card

U.S. List prices only.
BD-02301

NEWS UPDATE

Pilot Application

Concord Data Systems (Waltham, MA) announced that General Motors Manufacturing, Engineering and Development (ME&D) has selected its Token/Net local area network for use in GM's Multi-Vendor Node Development pilot project. The pilot application is the combined effort of the GM Assembly Division, ME&D and other General Motors divisions, and is designed to allow non-compatible computers and programmable devices within manufacturing to communicate with one another. Token/Net, a broadband token passing local area network, conforms to GM's Manufacturing Automation Protocol of IEEE-802 Token Bus. It will provide a physical and link layer (ISO layers 1 and 2) interconnection between IBM, DEC, Hewlett Packard, and other non-compatible computers used in GM's manufacturing.

Gould To Supply UPS To Intel

Intel Corp. stated it has arrived at an agreement with Gould Inc. for Gould to make and supply the Uninterruptible Power Systems (UPS) for Intel's FAST-3825 Semi-Conductor Disk System.

Gould's UPS is designed to supply automatically as much as 15 minutes of uninterrupted power if electrical service fails. Thus, Intel's FAST-3825 Random Access Memory (RAM) is protected while power is being restored to the CPU.

VMEbus Users Group Formed

The VMEbus, an international computer architecture that was introduced eighteen months ago by Motorola, Signetics, Mostek, Philips, and Thompson/EFCIS, has completed the acceptance cycle with the formation of the VMEbus Users Group. A small group, representative of the hundreds of companies that are currently using the VMEbus architecture in the U.S., met on May 18th, 1983 to approve the organizational charter, appoint an Advisory Board and initiate several ad hoc committees. The Users Group approved the preliminary charter, initiated a data base for VMEbus Users and committed to publishing two newsletters between now and the first official VMEbus Users Group meeting. The first meeting of the Users Group will be held during the WESCON Show in San Francisco the second week in November. Contact: Astraea Computer Corp., 846 Del Ray Ave., Sunnyvale, CA 94086.

AMI, Daisy Agreement

American Microsystems, Inc. (AMI), a subsidiary of Gould Inc., and Daisy Systems Corp. have reached an agreement in principle by which AMI will make a volume purchase of Daisy's family of engineering workstations. With the volume that is anticipated, AMI will be able to offer its customers a favorably priced turnkey system for design of MOS circuits and systems.

This agreement will allow system designers to use AMI's extensive libraries of standard cells and gate arrays, integrated in computer-aided-engineering (CAE) design system software and hardware. The AMI and Daisy joint agreement will be based on a volume purchase of Daisy's LOGICIAN and GATEMASTER systems by AMI. AMI and Daisy plan a joint marketing effort of these systems.

Mostek Receives JAN Qualification

United Technologies' Mostek Corp. has become the first 64K dynamic RAM supplier to receive Joint Army Navy (JAN) qualification. Designated the MIL-M-38510/244-02 under the JAN 38510 program, the Mostek 64K dynamic RAM provides an access time of 150ns, and uses the Mostek Scaled POLY 5™ process technology with advanced circuit techniques.

Foreign Trade Zone Attracts High Tech

Construction has begun at Boston's Logan Airport for the $200 million Bird Island Flats Development that will house the first Foreign Trade Zone at a U.S. international gateway. Groundbreaking ceremonies took place on April 4, and the zone is expected to receive final approval from the U.S. Customs Department soon. The zones were created by Congress as legal islands with the purpose of stimulating international trade by exempting products from import duties, excise taxes and bonding costs.

Micro-Style Software For Mainframe Users

The Mega Group, Inc. (Irvine, CA) has been formed to develop microcomputer-style software that will operate in mainframe system environments. The Mega Group's products will take concepts such as electronic spreadsheets, personal data bases, graphics and word processing, from the micro computer software library and integrate them into the installed mainframe market.

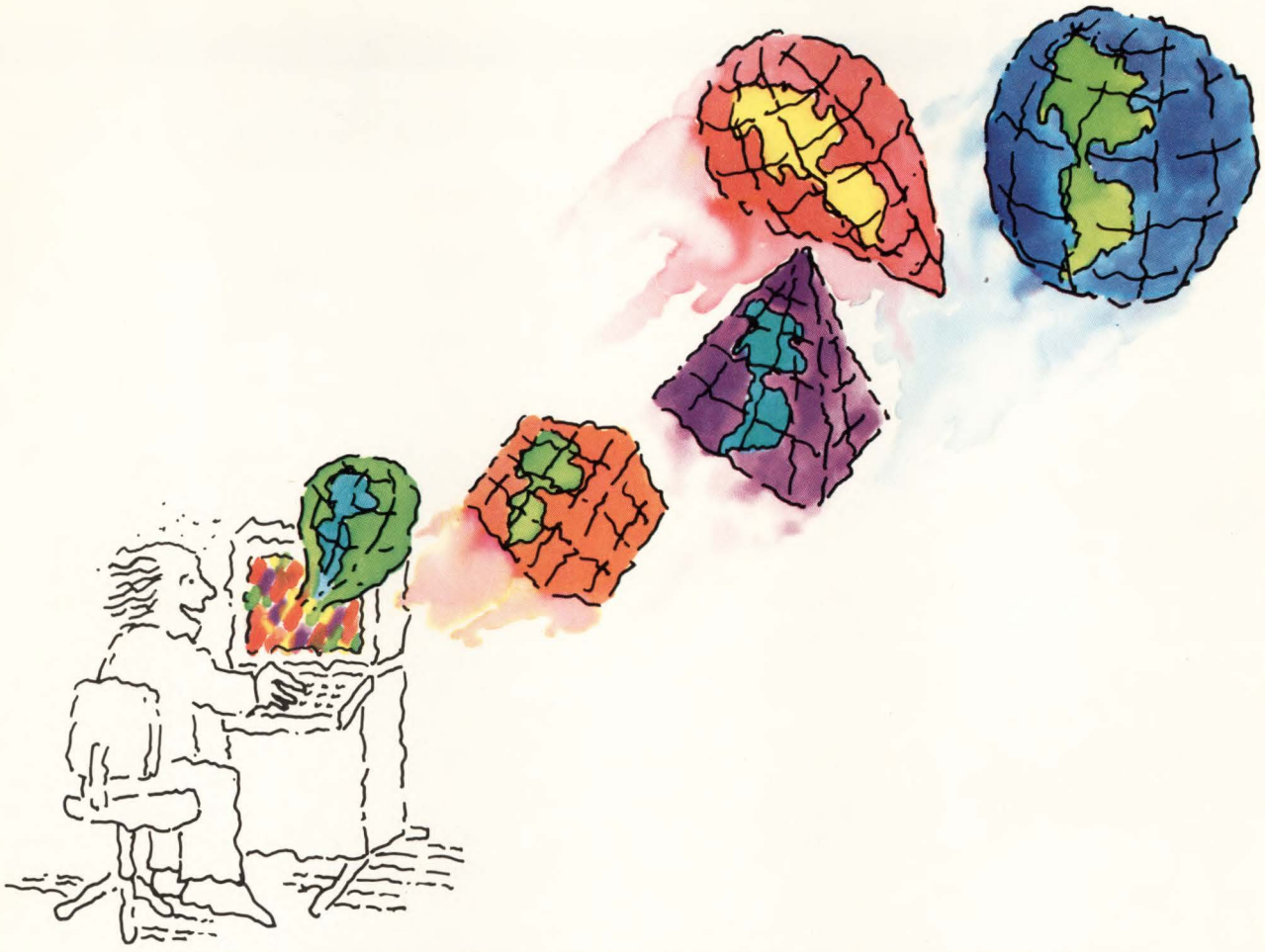
Emulogic Receives $3 Million

Emulogic, Inc. (Norwood, MA), a producer of universal microprocessor development systems, has received $3 million in venture capital financing. The funds will be used for working capital to finance rapidly accelerating demand for its products. Emulogic's ECL-3211 systems are sold to companies producing consumer and industrial products incorporating microprocessor chips.

High-Speed Logic Cross-License

Motorola, Inc. and Monolithic Memories, Inc. jointly announced the execution of a cross-license agreement covering a broad range of high-speed logic products.

Under terms of the agreement, Monolithic Memories is licensed to produce Motorola's ECL logic devices, specifically the MECL 10KH series logic circuits and MCA600ECL and MCA1200ECL macrocell arrays. Motorola is licensed to produce Monolithic Memories' ECL programmable array logic (PAL) circuits and 74LS series of buffers and dynamic RAM drivers.



CHANGE THE WORLD.

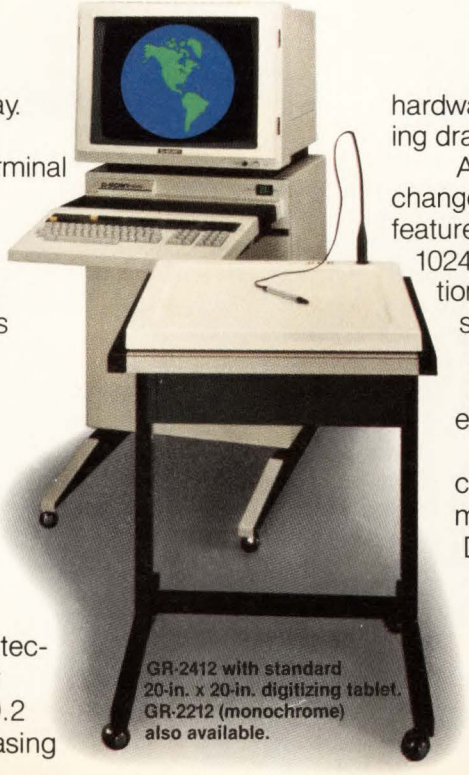
Or anything else you can display. Easier and faster than you imagine. Because D-SCAN's new GR-2412 terminal is changing the cost/performance standards for raster scan graphics.

Its world address space, for example, is a full 32K by 32K. Large enough to handle the most ambitious project. Yet easily manageable with dynamic zoom, pan, window, and viewport commands.

Its zoom operation faithfully preserves resolution and detail, instead of simulating it with pixel replication.

And those aren't all the improvements we've made.

Our dual microprocessor architecture draws 12,500 short vectors per second while transferring data at 19.2 kilobaud. And our exclusive anti-aliasing hardware removes jaggies without affecting drawing speed.



GR-2412 with standard 20-in. x 20-in. digitizing tablet. GR-2212 (monochrome) also available.

About the only thing we didn't change is our long list of standard features. Like our high resolution 1024x780 display. Local transformations. Up to 768K bytes of local segment memory. 4014 emulation mode. And the 10 years of Daini Seikosha (Seiko) craftsmanship in every D-SCAN product.

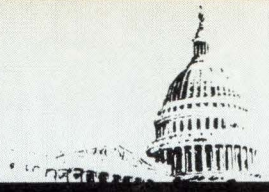
If you're ready to make some changes, contact us at Seiko Instruments U.S.A., Inc., 2620 Augustine Drive, Santa Clara, California 95051. Telephone (408) 727-0768.

We'll give you a terminal that can take on the world.

D-SCAN

Seiko Instruments U.S.A., Inc.

WASHINGTON REPORT



by Anne Armstrong

A secondary skirmish in the war over semiconductor chips has been the question of chip piracy. Everyone seems to agree that it's a growing problem and some type of legislation is needed to protect the investment which goes into designing and manufacturing chips. The disagreement has been whether patent, trademark, copyright or some new special protection is most suitable.

Recent discussions have focused on two similar bills introduced in the House and the Senate which would place chips and the masks used to produce them under the protection of a new section of the copyright law. Sponsored by Senators Charles M. Mathias, Jr. (R-Md.) and Gary Hart (D-Colo.), S. 1201, "The Semiconductor Chip Protection Act of 1983," is a refinement of several bills introduced in earlier years. (The House version is H.R. 1028.)

Basically, the legislation would create a new category of copyrightable work known as "mask works." These mask works would have a limited term of protection—10 years from first authorized use instead of copyright's normal 75—and would offer special protections for innocent or unknowing infringers.

"Current law gives only very limited protection to semiconductor chips," said Sen. Mathias. "Patent law can protect the basic electronic circuitry used in the chip, but not its carefully developed design. By giving chip engineers and manufacturers copyright protection for a 10-year period, S. 1201 will protect their R&D investment. It will also protect innocent purchasers of pirated chips, by including a compulsory licensing provision allowing them to use that chip after paying a royalty to the innovating firm, and by eliminating any liability for innocent infringement."

Although the obviously industrial nature of the semiconductor chip might lead observers to wonder why patent law would not be a better way to protect chips, none of the major players have suggested it. Patent law's rigid standards for novelty and invention eliminate most chips.

Trade secret protection wouldn't work either because it is based on the idea of keeping the components or parts secret, and chips are widely available and easily disassembled to reveal the design.

Although legislation protecting chips with copyright has been introduced and died quietly before, there is more attention focused on the problem today. Trade questions are getting more press interest and the dollars at stake keep going up. The Semiconductor Industry Association does not have figures on the losses each year due to chip piracy but Intel Corp, a major chip manufacturer, estimates that an investment of $80 million is required to bring a new family of chips to market. A simple photographic copy of the main chip would cost a pirate only $100,000. In fact, Intel's corporate counsel says that every new chip is evaluated for the risk of piracy, and as a result, many chip designs are cast aside because the threat of piracy makes the investment too risky.

Proponents of the legislation maintain that although American copyright law traditionally protected "writings" as described in the Constitution, the copyright concept has now been extended beyond works that convey ideas or have artistic merit. In fact, copyright has been granted on belt buckles, E.T. lunchboxes, ashtrays, pill boxes and a host of similar items.

Currently supporting the legislation is the Semiconductor Industry Association and with minor modifications, the Computer and Communications Industry Association. On the opposite side are the Association of American Publishers, the Association of Data Processing Service Organizations, the Information Industry Association, a committee of the American Bar Association, and the U.S. Copyright Office, all of whom for a variety of reasons believe that the copyright act is being twisted beyond its limits and is the wrong way to try and protect chips.

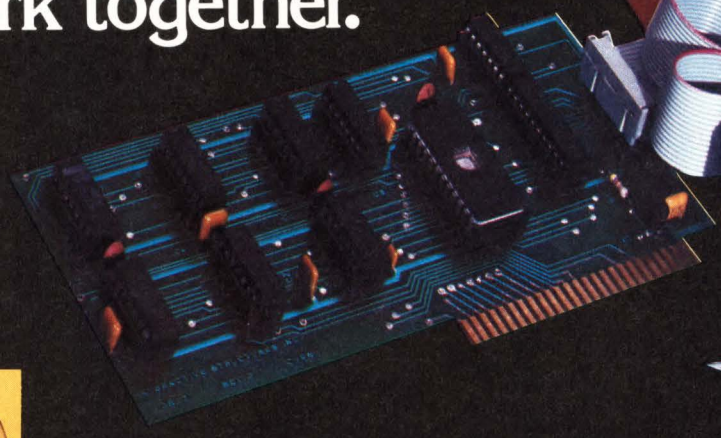
The opponents base their objection primarily on four arguments: copyright does not protect useful articles per se; it protects the design of a useful article only to the extent that it can be identified as separate from the article itself and can exist independently; copyright of a drawing does not protect against duplication of the article itself; and copyright protects only expression, not ideas, plans or processes. They also believe the question of legitimate reverse engineering has not been adequately addressed. The distinctions between photographically copying the masks and reproducing the chip, and photographically copying the masks for the purpose of studying and drawing new schematics is a fine and somewhat obscured line.

A compromise which has been mentioned by several organizations is new legislation which would not extend copyright, but provide copyright-like protection for works such as chip masks which do not fit into the copyright term "original works of authorship." One model suggested for this legislation is H.R. 2985, "Design Protection Act," a retooling of a bill introduced in the last Congress, H.R. 20. This bill provides protection for ornamental designs of useful articles. Counsel from many organizations want to "fix" the design bill so that it can be a model for chip protection. If the fixers do not destroy the fabric of the original legislation, it might prove the better avenue for manufacturers to pursue.

Even Mathias is not certain copyright is the best way. "Our aim is to deter and to punish chip piracy, without discouraging legitimate reverse engineering. The copyright law seems to be the best tool at hand to get the job done, but we must make sure that it isn't stretched out of shape in order to accommodate this new need."

PKASO™
Printer Interface Family

Welcomes the New Apple *IIe*... We work together.



PKASO Interfaces come complete with Cable, Instructional Diskette and Comprehensive Manual.

The PKASO family makes you and your Apple Computer a master of text and graphics.

PKASO makes it easy to use the features of your printer—select character sizes, vary line spacing, even print in colors. Simple PKASO commands make these features usable from the keyboard or a program.

PKASO also adds features to your system. Press a few keys and get a snapshot "dump" of the image you see on the screen—text or graphics. Add new characters and symbols that you couldn't print before, using our SuperFont™ system. Add our new PipeLine™ printing buffer and your printer can take its time while you and your Apple move on to the next task. The PipeLine is a modular add-on to the standard PKASO board.

The PKASO interface is designed for Apple II and Apple /// in all the popular configurations. It prints in full color on the IDS Prism Printer, and in striking black on C. Itoh, Centronics, Epson, IDS, NEC, and Okidata matrix printers.

NEW!

The IS Pipeline™ Printing Buffer with Random Access Printing stores paragraphs or pictures for printing in any order—any number of times!

- Universal—works with any parallel (Centronics style) computer/printer combinations.
- 8K to 128K Bytes of memory with data compression for efficient use of memory space.

Write 5 on Reader Inquiry Card

Interactive Structures Inc.
146 Montgomery Avenue
Bala Cynwyd, PA 19004
Telephone: (215) 667-1713

DEC* COMPATIBILITY PLUS
PERFORMANCE
DEPENDABILITY
ECONOMY

Monolithic Systems Corporation has provided reliable DEC compatible memory products for over 12 years. In fact, MSC patented the first semiconductor memory product in 1974! The success of Monolithic Systems has been attributed to products that perform better than any other in the business, products that have the modularity to grow with the systems that they're installed in and products that offer the best price in the market. These claims are supported by a one-year warranty which underscores MSC's superior quality in design and manufacturing.

In 1983 MSC will continue to lead the market with products for Q-BUS* and VAX* machines. These products will be very formidable contenders for years to come. As always, Monolithic Systems will be on the leading edge of memory technology and innovation with products to last the life of your machine.

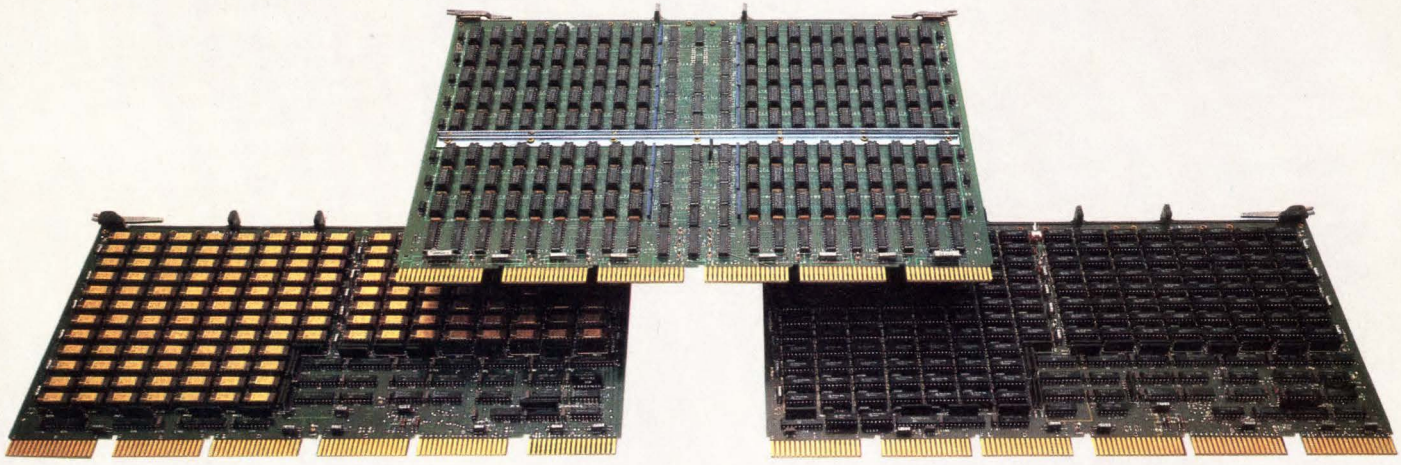
For further information on Monolithic Systems Corporation and how we may support your computer needs, call Toll Free 1-800-525-7661.

Monolithic Systems corp. *. . . means technically advanced solutions.*

USA
84 INVERNESS CIRCLE EAST
ENGLEWOOD
COLORADO 80112
303-770-7400
TELEX: 45-4498

EUROPE
JUSTINIANSTRASSE 22
6000 FRANKFURT aM MAIN 1
WEST GERMANY
611590061
TELEX: 41-4561

CANADA
6503 NORTHAM DRIVE
MISSISSAUGA
ONTARIO, CANADA L4V IJ2
416-678-1500
TELEX: 96-8769



DEC VAX - 11/730, VAX - 11/750 AND VAX - 11/780 MEMORY
TOTAL DEC HARDWARE AND SOFTWARE COMPATIBILITY
DEC EQUIVALENT PERFORMANCE AND CAPACITY
MSC RELIABILITY, QUALITY AND SERVICE

Write 3 for DEC Compatible Products Brochure.

Z800 Family Features Memory-Management And Cache

A new μP family that runs any software written for the Z80 CPU but offers up to five times greater performance through the use of on-chip peripherals, on-chip cache and instruction enhancements, has been announced by Zilog, originator of the Z80 device.

The family consists of the 8-bit bus Z8108 and Z8208 that are packaged in 40-pin and 64-pin dual in-line packages, and the 16-bit bus Z8116 and Z8216 in 40- and 64-pin packages.

Central to the Z800 μPs is an enhanced version of the Z80 Central Processing Unit (CPU). To better assure system integrity, the Z800 can operate in either User or System mode, allowing protection of system resources from user tasks and programs. System mode operation is supported by the addition of the System Stack Pointer to the working register set. The IX and IY registers have been modified so that in addition to their regular function as index registers, each register can be accessed as a 16-bit general-purpose register or as two single-byte registers.

The Z80 instruction set has been refined, meaning that the Z800 μPs are completely binary-code compatible with present Z80 code. The basic addressing modes of the Z80 μP have been augmented with the addition of Indexed mode with full 16-bit displacement, Program Counter Relative with 16-bit displacement, Stack Pointer Relative with 16-bit displacement, and Base Index mode. The new addressing modes are incorporated into many of the old Z80 instructions, resulting in greater flexibility and power. Some additions to the instruction set include 8- and 16-bit signed and unsigned multiply and divide, 8- and 16-bit sign extension, and a test and set instruction to support multiprocessing. The 16-bit instructions have been expanded to include 16-bit compare, memory increment, memory decrement, negate, add, and subtract, in addition to the previously mentioned multiply and divide.

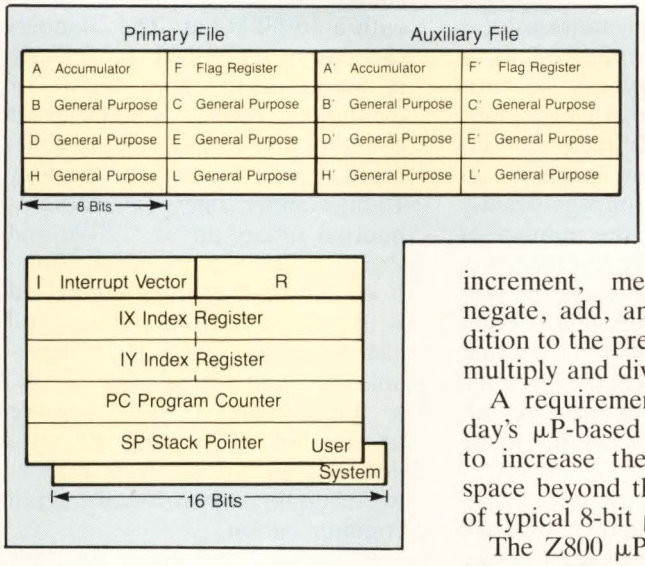


Figure 1: Configuration of CPU registers in Z800.

A requirement of many of today's μP-based system designs is to increase the memory address space beyond the 64K byte range of typical 8-bit μPs.

The Z800 μPs have an on-chip Memory Management Unit (MMU) that enables the μPs to address either 512K bytes or 16M bytes, depending on the package of the device. In addition to enabling the address space to be expanded, the MMU performs other memory management functions previously handled by dedicated off-chip memory management devices.

I/O address space has been expanded by the addition of an I/O page register used to select pages of I/O addresses. The 8-bit I/O page register can select one of 256 possible pages of I/O addresses to be active at one time, allowing a total of 64K I/O addresses to be accessed.

Peripheral Number	Peripheral Name
Z8108/Z8208 8-bit bus (Z80 control signals)	
Z8410	DMA Direct Memory Access Controller
Z8420	PIO Parallel Input/Output
Z8430	CTC Counter/Timer Circuit
Z8440/1/2	SIO Serial Input/Output Controller
Z8470	DART Dual Asynchronous Receiver/Transmitter
Z8516	DTC Direct Memory Access Transfer Controller
Z8530	SCC Serial Communications Controller
Z8531	ASCC Asynchronous Serial Communications Controller
Z8536	CIO Counter/Timer and Parallel I/O Unit
Z8038	Z-FIO FIFO Input/Output Interface Unit
Z8070	Floating Point Processor

Peripheral Number	Peripheral Name
Z8116/Z8216 16-bit bus (Z-BUS control signals)	
Z8016	DTC Direct Memory Access Transfer Controller
Z8030	Z-SCC Serial Communications Controller
Z8031	Z-ASCC Asynchronous Serial Communications Controller
Z8036	Z-CIO Counter/Timer and Parallel I/O Unit
Z8038	Z-FIO FIFO Input/Output Interface Unit
Z8060	FIFO Buffer Unit and Z-FIO Expander
Z8065	Z-BEP Burst Error Processor
Z8068	Z-DCP Data Ciphering Processor
Z8070	Floating Point Processor
Z8090	Z-UPC Universal Peripheral Controller

Table 1. Peripheral support for the Z800 Microprocessors

There are 256 bytes of on-chip memory present on all members of the Z800 family. This memory can be configured as a high-speed cache or as a fixed address local memory. When configured as a cache, the memory can be programmed to be instruction only, data only, or both data and instruction. The cache memory allows programs to run significantly faster by reducing the number of external bus accesses. Operation and update of the cache is performed automatically and is completely transparent to the user. When used as a local memory, the addresses are programmable, allowing "RAMless" systems to be used.

Many features that have traditionally been handled by external peripheral devices have been incorporated in the design of the Z800 μP. The "on-chip peripherals" reduce system chip count by reducing system interconnection on the external bus. All members of the Z800 family contain an on-chip clock oscillator. Also present is a refresh controller that provides 10-bit refresh addresses for dynamic memories.

The Z8208 and Z8216 contain additional on-chip peripherals to provide system design flexibility. To support high-bandwidth data transmission, four Direct Memory Access (DMA) channels are incorporated on-chip. Each DMA channel operates using full 24-bit source and destination addresses with a 16-bit count. The channels can be programmed to operate in single transaction, burst, or continuous mode. System event counting and timing requirements are met with the help of the four 16-bit counter/timers (available as internal timers on the Z8108 and Z8116). The counter/timer functions can be externally controlled with gate and trigger inputs, and can be programmed as retriggerable or non-retriggerable. Also, a full duplex UART, capable of handling a variety of data and character formats is present to facilitate asynchronous serial communication.

Regardless of whether the 8-bit or the 16-bit bus is used, all members of the Z800 family feature programmable bus timing in which the user can specify timing that is tailored to individual systems. Upon reset the Z800 μPs can be programmed to have system timing that is one-fourth, one-half, or equal to the speed of the CPU, with one-half being the default. In addition to clock scaling, programmable Wait states can be inserted during various bus transactions. Without the use of external hardware, zero to three Wait states can be inserted into Memory, I/O and Interrupt Acknowledge transactions. Furthermore, separate memory Wait states can be specified for upper and lower memory, enabling different speeds of ROMs and RAMs to be used in the same system.

A feature of the 16-bit Z8116/Z8216 bus interface is the ability to support "nibble-mode" Dynamic RAMs. Using this feature (known as burst mode), the bus bandwidth of memory read transactions is essentially doubled. Burst mode transactions have the further benefit of allowing the cache to operate more efficiently by guaranteeing a higher probability of the accessed memory to be present in the cache.

The Z800 family supports Zilog's Extended Processor Architecture in a number of ways. All members are capable of trapping External Processor Unit (EPU) instructions in order to perform software emulation of the EPU. The Z8216 directly interfaces with an EPU such as the Z8070 Floating Point Unit and operates in a manner that is completely transparent to the user and the program. The other members of the Z800 family can easily interface with EPUs with the aid of support software.

Write 235

Evaluators Speed Tape Drive Integration

Designed to ease integration of the company's 24 track, 160 Mbyte ½" tape streamer into computer based systems, Rosscomp's (Cerritos, CA) E Series Evaluators allow file and restore operations at 90 or 130 in/sec. The evaluators are used with low speed Q2000/SA1000 interfaces or the higher speed SMD interface. Each evaluation package includes a Rosscomp D160 tape drive, and exerciser plus cables and connectors. The exerciser is used to write data in forward and reverse directions, step the head, and analyze signals and windows using an oscilloscope. An intelligent controller is included that supports both on- and off-line data transfers between disk drives and the streamer. Five versions of the Evaluator are offered.

Model E160 is based on a D160 90 in/sec drive and a Rosscomp C160 single-board tape/disk controller. The C160 controller interfaces a Rosscomp drive to up to four Q2000/SA1000-compatible Winchesters, and to a host processor with a SASI bus. The E160 will support data transfer rates up to 8 MHz across the host interface.

The evaluator permits direct communication between the peripheral subsystem and the host processor and operates off-line for file backup and restore evaluations between the tape and disk drives. This evaluator can be used in the drive's split-drive mode with the 24-track format logically divided into drives of two, four, eight or twelve tracks, thus reduc-

ACCES™

"We've got what makes the difference in Local Area Networking..."

The ACC Exchange System (ACCES) is a product umbrella that incorporates a comprehensive approach for truly distributed networks.

ACC Knows Networking. For over a decade, ACC personnel have set the pace in network product development. Beginning with the ARPANET, ACC has designed and developed a broad range of high performance network access equipment for packet switched and local area networks.

It is this experience that makes the difference in our approach.

Everyone agrees that Local Area Networking is good. But no one seems to agree on much else. Coax versus twisted pair. Baseband versus broadband. Token ring versus random access. The list goes on and on. Our experience, however, has taught us that low level features are only a small part of a functioning network.

The ACCES Approach. Most Local Area Network products today are hardware solutions at the lowest networking levels. Before LANs can become truly useful, network users need to have higher level functions at their fingertips. The ACCES approach provides network services through the upper layers of the OSI model. By following the layered model, the ACCES product line does not rely on specific low level implementation (baseband, broadband, etc).

The ACCES Product Line. Some of the products under the ACCES umbrella:

- Intelligent Ethernet front ends (UNIBUS and VERSAbus)
- X.25/Ethernet Bridge
- IBM Channel/Ethernet interface
- Baseband/Broadband Converter
- Xerox Network Systems (NS) communications protocol package
- LAN industry news, over your terminal and modem, dial up On-Line Information at (408) 475-7940. And it's free.

If you'd like more information on the ACCES approach and product line, call us. Today. (408) 425-0937.

ACC LOCAL AREA NETWORK CENTER

Associated Computer Consultants
Local Area Network Center
2901 Park Avenue
Soquel, CA 95073
TWX 910 334-4907
(408) 425-0937

Write 10 on Reader Inquiry Card

ing access time to a record to 30 seconds on the average. $4455.

E163-90 and E163-130 versions have the same functional specifications as the E160 evaluators but also support a D160 ½″ tape drive operating at either 90 or 130 in/sec respectively and two SMD Winchester disk drives. Both are $4675.

Model E161 is designed for online analysis of file backup and restore using the D160 drive and a host processor. The system uses an intelligent controller that makes the D160 compatible with drives that use the ¼″ cartridge (QIC) interface.

The E161 provides an 8-bit parallel connection to the host processor, handles data separation, tape formatting, and error-detection and control. It is available in either a 90 in/sec version (the E161-90) or in a 130 in/sec version (the E161-130). Both are $3295.

The company claims these tape drive evaluators are, like the drives themselves, unique. For example, the D160 stores its 160 Mbytes on a self loading 4″ tape reel rather than the cartridges used in competing drives. The reel design is said, by the company, to be more stable at high speeds and high transfer rates than cartridge based products. The current drive is packaged in an 8″ Winchester form factor. A new drive using the same 4″ reel is in development with the same 90 or 130 in/sec speeds and capacity as the D160, yet packaged in a 5 ¼″ form factor. Interfaces being explored include: SASI/SCSI, QIC, STS06, ESDI, Q2000/SA1000, SMD and the 9-track Pertec type. Quantity pricing is expected to be approximately $300. **Write 231**

Figure 1: Rosscomp's E-Series evaluators.

3.5″ Winchester Uses Plated Media, Thin Film Heads

The Control Data Corp. (Minneapolis, MN) Cricket hard disk drive boasts an unformatted capacity of 6.38 Mbytes on a single 3.5″ disk. This high storage capacity is due primarily to the use of plated media and IBM 3380 type thin film. Both heads and media are nickel-cobalt plated. Recording densities are 15,390 bits/in and 450 tracks/in.

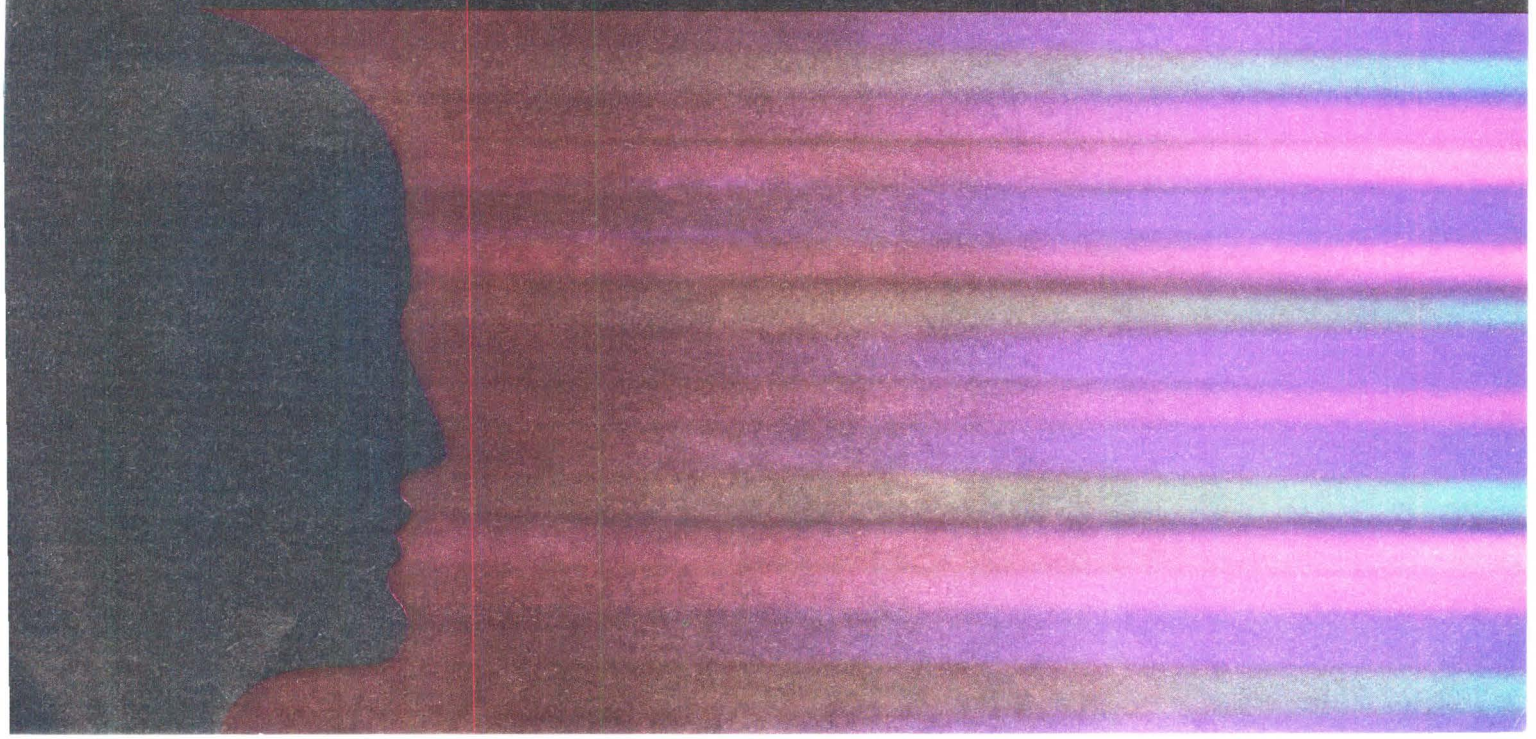
The thin film technology is shared by four other drives that were announced by the company at the same time. They include: two half-height 5.25″ floppy disk drives; an 80-Mbyte model in the "Wren" 5.25″ Winchester family; two 9″ Fixed Storage Drives that hold up to 516 Mbytes of data; and an 825-Mbyte, 14″ Winchester.

Because of LSI technology, including two custom chips for servo and read chain control, drive electronics are contained on a PCB that is roughly a third the size of boards used in 5.25″ Winchester drives. The result is a drive with the Sony form factor measuring 1.63″ × 4″ × 6.37″. It is the same height as a half height 5.25″ Winnie.

The Cricket is timing and format compatible with the ST506 interface with a 5 Mbits/sec transfer rate. Average seek time is 117 msecs using a band stepper positioning method. The microprocessor controlled, closed loop digital servo system uses information that is written on a servo surface embedded at the beginning of each track. $465. Initial evaluation units will be available in the third quarter of 1983. **Write 232**

The CDC 9290-6 Cricket.

Introducing the first array processor to break the $2,000/MFLOP barrier.



The FPS-5000 Series from

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words are available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the FPS-5000 Series sets a new standard for cost-effective computing, breaking the $2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

*Based on U.S. Domestic Prices

Typical performance examples of geophysical, medical imaging and signal/image processing applications.

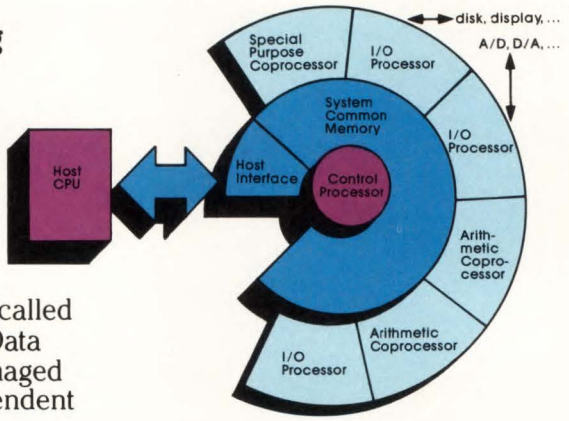
Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25.0 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

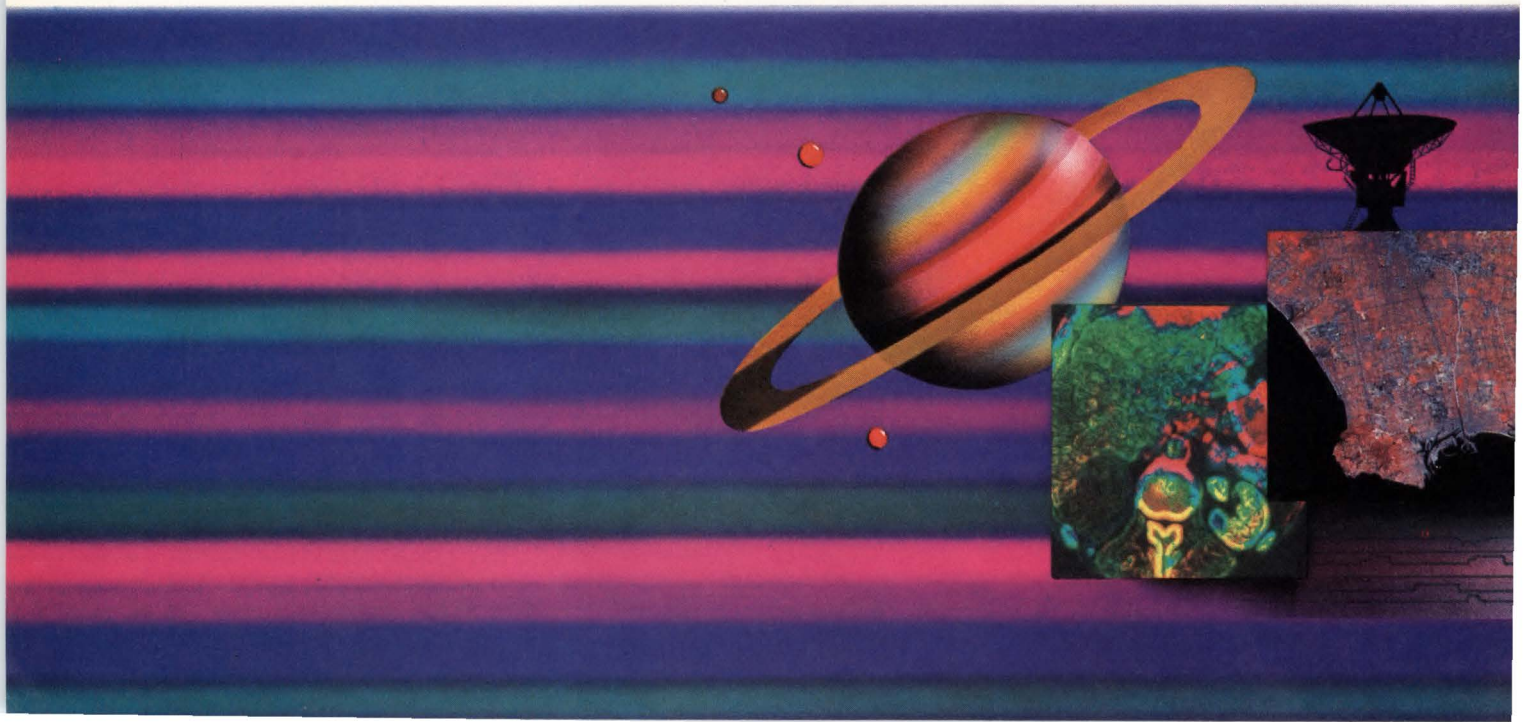
Based upon specifications subject to change.

Distributed processing architecture

The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called Arithmetic Coprocessors. Data flow is simultaneously managed by a combination of independent I/O Processors and the central Control Processor.

FPS-5000 Series Architecture



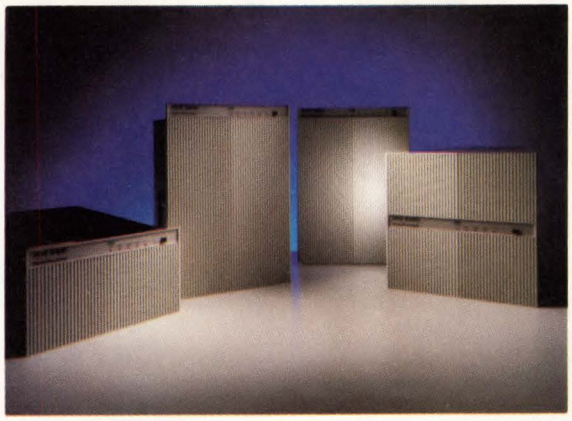


Floating Point Systems.

Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.



Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best meantime between failure (MTBF) rates in the industry.

The Series is backed by the same outstanding worldwide support services that distinguish Floating Point Systems from other manufacturers.

For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

The world leader in array processors.

FPS® FLOATING POINT SYSTEMS, INC.

P.O. Box 23489
Portland, OR 97223
(503) 641-3151
TLX: 360470 FLOATPOIN BEAV

FPS Sales and Service Worldwide.
U.S.: CA–Laguna Hills, Los Angeles, Mountain View. **CO**–Lakewood. **CT**–Simsbury. **FL**–Winter Park. **GA**–Atlanta. **IL**–Schaumburg. **LA**–New Orleans. **MD**–Rockville. **MA**–Dedham. **NJ**–Red Bank. **NM**–Corrales. **PA**–Philadelphia. **TX**–Grand Prairie, Houston. **WA**–Bellevue.
INTERNATIONAL: Canada, Calgary, Montreal, Ottawa; England, Bracknell, Berkshire; France, Rungis; Japan, Tokyo; Netherlands, Gouda; West Germany, Haar.

DISTRIBUTORS: Australia and New Zealand, Milsons Point–N.S.W., Melbourne-Victoria (Techway Pty., Ltd.); Austria, Vienna (Elektronische Bauelemente Und Gerate); Finland, Helsinki (OY Emmett AB); India, Bombay (Hinditron Computers PVT., Ltd.); Israel, Tel Aviv (Eastronics, Ltd.); Korea, Seoul (World Business Machine, Inc.); Singapore, Hong Kong; Brunei, Indonesia, and Malaysia (Scientek Engineering Co.); Southern Africa, Johannesburg (Anker Data Systems); Sweden and Norway, Vaxholm (Tre Konsulter AB); Taiwan, Taipei (Scientek Corporation).

Write 12 on Reader Inquiry Card

A unique combination.

Introducing a digitizer with a built-in mouse.

A unique combination unmatched by any digitizer on the market today, the MM™ Series can perform all your cursor steering, menu picking and graphics digitizing tasks. The MM outputs both absolute coordinate data like a digitizer and delta coordinate data like a mouse.

The MM Series was designed to offer builders of today's lower-cost terminals, graphic workstations and personal computers Maximum performance at Minimum cost. Maximum performance because you'll get all the features you need from a high resolution, remotely-controlled digitizer plus the versatility of a cursor steering mouse in one compact package. And Minimum cost because MM was designed, right from the start, to be inexpensive to purchase, integrate and maintain.

MM digitizers are available with either cursor or pen-like stylus.

Advanced packaging combining light weight, small overall size, and slim profile with built-in tilt mechanism make the MM Series an ideal addition to your user-friendly system.

Every MM Series digitizer is backed by Summagraphics, the leader in digitizers, and the emerging leader in graphics input devices.

Call or write Summagraphics Corporation, 35 Brentwood Avenue, P.O. Box 781, Fairfield, CT 06430. Telephone (203) 384-1344. Telex 96-4348.

Summagraphics® CORPORATION

Write 13 on Reader Inquiry Card

Disk Drive Market Holds Course

With the rising popularity of "Winchester" fixed media drives, many disk manufacturers were uncertain as to the effect, if any, it would have on cartridge disk drive sales. In a recently released analysis, Venture Development Corp. (Wellesley, MA) found that 5.25″, 8″, and 14″ cartridge disk drive sales will grow approximately five percent annually over the next five years, starting from 1982 sales of $1.2 billion. The fixed media, cartridge disk, and disk pack market will grow from $7.0 billion in 1981 to a predicted $17.8 billion in 1986.

The disk drive industry is rapidly growing because of three important factors: 1) escalating requirements for additional storage space; 2) the increasing reliability of hard disk technology; and 3) the appearance of new types of computer systems utilizing hard disk technology.

The growth of cartridge disk drive sales is contigent upon a host of variables including the development of the sub-8″ drive market, product standardization, plated media, and greater than 10 Mbyte ¼″ tape drives.

Plated media's success may largely determine the future of cartridge disk drives. Previously, this media has principally been used in fixed media drives. International Memories Inc., who purchases the plated media from Ampex and PolyDisk and incorporates it into a drive, has been a pioneer in selling plated media. This year they secured a $10 million contract with Data General for their H series 5.25″ drive with shipments beginning in 1983. 1983 will also be the first year that both Syquest and Disctron will be selling their plated media cartridge disk drives.

Quarter-inch cartridge tape drives are viable competitors within the removable media marketplace as well.

Graphics Terminal Vendors Making Shift to CAD

Several prominent graphics terminal manufacturers made announcements at the recent NCGA show in Chicago that indicates the continuing maturation of the vendors participating in graphics marketplace. Notable among them were Intecolor Company (Norcross, GA) and DataType (Mountain View, CA). Intecolor, part of the Intelligent Systems Corporation's growing number of firms discussed a 1024×1024 color monitor, which may have applications in future CAD products. Intecolor may soon launch a very substantial entry into low cost, high resolution CAD systems. DataType which announced further advances in its graphics terminals showed a product incorporating a Motorola 68000, allowing standalone or independent graphics operations. Of interest is that both of these were for years known primarily as suppliers of ASCII based graphics systems or in the case of DataType for retrofitting other manufacturers' products. As the cost of powerful processors decreases both of the companies are moving enhanced graphics into markets that they have exploited well for lower resolution products.

—Borrell

New Resource For Software Buyers

A new concept in cataloguing software was recently introduced by PC Telemart Inc. (Fairfax, VA). Over 1,000 pieces of software have been donated or loaned to the PC National Software Reference Library by distributors, publishers, hardware retailers and manufacturers.

The library, which is non-lending and requires a membership, was conceived as a resource for potential buyers who want to test a variety of software before purchase. The facility allows for individual testing and selection and is staffed by a thirty-person technical staff.

For members who cannot come to the facility in person, a network called "Telemart" has been devised. Information is obtained in "kiosks" which are leased by stores nationwide. The kiosks are outfitted with a terminal and printer accessing users to information on 30,000 software packages, their applications, manufacturers, as well as technical analysis and critical reviews. To access information the user goes to a kiosk which can be found anywhere from a 7–11 to a bookstore, or calls the leased property for a nominal connect charge. There are thirty pilot stores in Washington and ninety more in New York, Boston, Los Angeles, San Francisco, Denver, Chicago and Dallas.

The library will rely on consultants to teach seminars and write reviews on software and is designed with a main reference room and a theater for classes and films. It sponsors seminars and training courses for the novice to the advanced micro-technician. Membership is on a quarterly or annual basis. An initial charter subscription is $300, quarterly rate $100, and daily fee $25. For more information contact: PC Telemart, 11781 Lee-Jackson Highway, Fairfax, VA 22033 (703) 352-0721.

—Coville

Color Graphics Display Uses 8K × 8 iRAMs

Unlike the pseudostatic or quasi-static RAM devices which only incorporate a portion of the refresh circuitry onto the memory chip and still require much control from the CPU, an iRAM integrates all the components of a dynamic RAM system into a single device. The integration used in the iRAM includes the refresh timer, refresh address control and counter, address multiplexing, and memory cycle arbitration as well as an 8-bit wide memory array.

The design that follows shows the 2186/2187 iRAM in a specific application: a color graphics display memory.

In this example (**Figure 1**), the color display resolution is 65,536 (256 × 256 pixels) × 4 bits. The four bits select the color of the pixel by addressing a color lookup and video priority table. This programmable table permits up to 16 colors (out of 256 possible) per display frame. It also assigns priority. For example, a red disk crosses a green on the display. Does the red cross in front of the green disk, the green in front of the red, or does the area of the overlap become yellow? The priority encoding assigns answers to these questions.

By industry standards, this 256 × 256 pixel display has low-end to medium display resolution. For those unfamiliar with the capabilities at this level, visit a local video game parlor and examine some of the dazzling displays on the state-of-the-art video games such as Williams Electronics Defender. Advanced machines such as this are only beginning to approach this display density.

The iRAM used in this example is the synchronous 2187. Due to the sequential addressing scheme of video displays, video memory typically requires no additional circuitry for refresh. The 2187 is no exception, and in this design the $\overline{\text{REFEN}}$ pin is tied high. The sequential scanning by the video address generator automatically refreshes the internal array of the iRAM.

CPU addresses A_{14} and A_{15} are decoded to generate one of four iRAM chip selects so that the (assumed 8-bit) CPU can read or writer information to the individual memory planes (iRAMs). These chip selects are gated so that all four iRAMs can be simultaneously enabled by the V_{CS} signal from the video timing circuitry. A similar circuit (not shown) would allow $\overline{\text{OE}}$ for the iRAMs to be generated by either the CPU or the video timing generator. The iRAM addresses are generated by multiplexing the CPU addresses with video timing addresses. The 32-bit output from the iRAMs is loaded into four 8-bit shift regis-

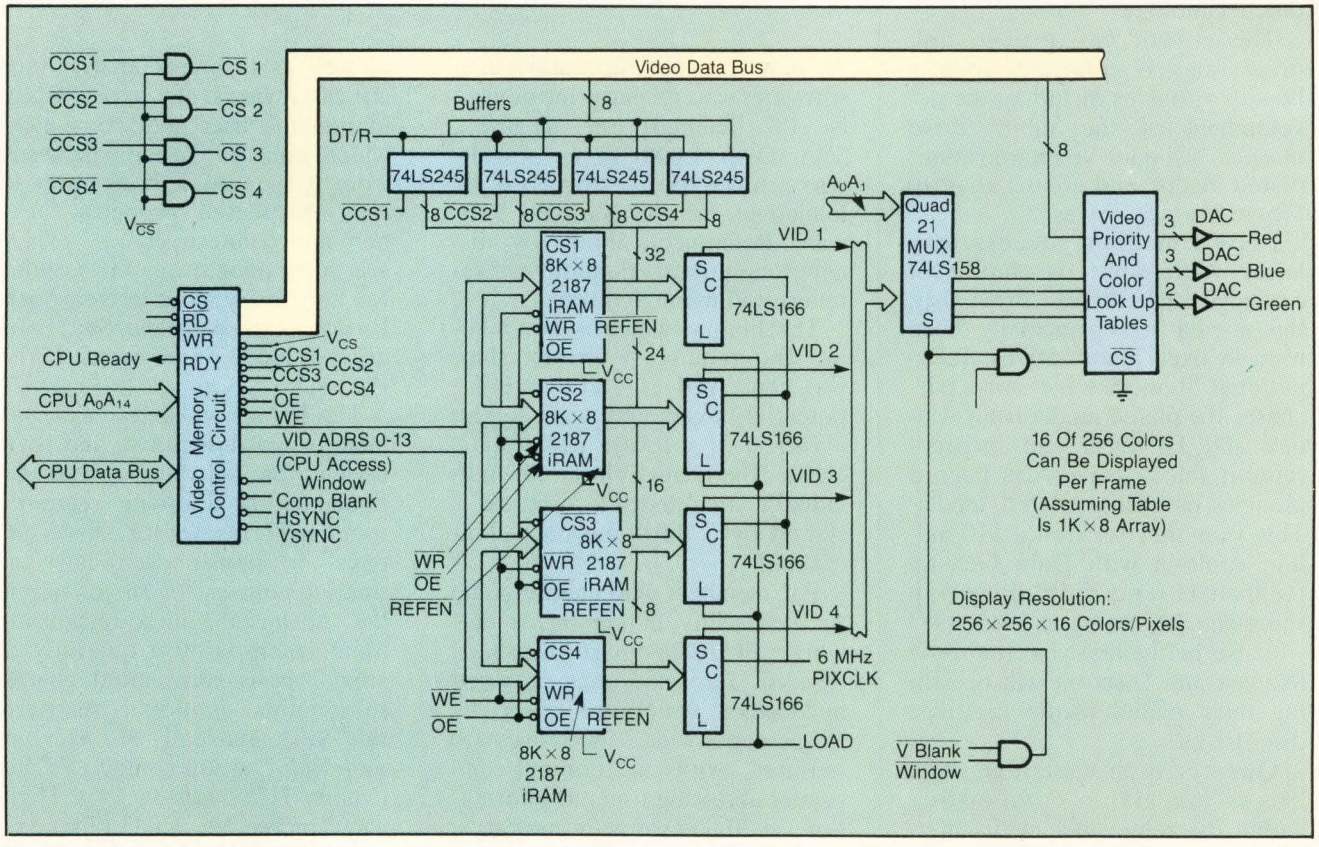


Figure 1: Using the 2187 iRAMs in a color graphics display memory.

Pro-Log. Rushing slowly into Systems with our new ABL-1™

We're taking the plunge into the systems business, one toe at a time.

Our first packaged solution is called ABL-1. ABL stands for "Auto-BIOS™ Logic," new firmware that lets you run thousands of existing CP/M®-based applications software packages. Just plug in the software and run it — without the need to write or modify the CP/M®-BIOS (Basic I/O System).

ABL-1 is a general purpose, fully integrated STD microcomputer system which you can use either as a cost-effective software development tool or as your target system. ABL-1 is ideally suited for developing your application software for use on STD BUS-based systems. Integrate your hardware and software quickly and easily — without the need for emulators or analyzers.

Until now, you've spent time and money putting together pieces from Pro-Log. Now there's ABL-1; all the bits and pieces in one piece. An instant solution instead of an eventual one.

You know we don't rush into things, so you know that all the pieces, and the new ABL-1 package, really work. No one ever called us "racy," even when we invented the STD BUS a few years ago (our design is now a worldwide industry standard), so ABL-1 isn't a quick fix, it's a reliable packaged solution. We're in the systems business now; anyone wanna race?

Rack mountable or stand-alone	Two-year warranty
Built-in modular self-test	Six months warranty on drives
Dual eight-inch floppies	RETMA 19" x 7" package
Separate CRT and printer ports	64K memory
Removable I/O panel	8085A and Z80A CPU

PRO-LOG® CORPORATION

2411 Garden Road
Monterey, California 93940
408-372-4593 TLX: 171879
Toll-Free 800-538-9570

Steady Pace Wins The Race

Offices and Telex: Australia, 35494; France, 842-696379; Germany, 971624; Italy, 68071; Sweden, 13695; Switzerland, 55448; United Kingdom, 858618.

*CP/M is a registered trademark of Digital Research Incorporated.

Write 67 on Reader Inquiry Card

ters and are serially shifted out as four bits of video information used to address the color lookup table. The four lines (Vid_1–Vid_4) are multiplexed with CPU addresses A_0–A_3 to create the actual addresses of the lookup table. Comprised of two 2148H RAMs, the eight data lines of the lookup table are directed to three digital-to-analog converters for generating 16 of 256 different display colors.

Due to the byte-wide organization of the iRAMs, there is plenty of time between video read cycles to allow CPU access to the memory. With a pixel rate of 6 MHz, the byte-wide iRAM has a video read rate of 6/8 MHz or once every 1.33 microseconds. Only 350 ns of this time is needed for a video read cycle. The balance of the time (approximately 1 μsec) can be used by the CPU to access the memory. This interleaving of CPU cycles with video timing cycles, combined with allowing the CPU unrestricted access to the memory during both horizontal and vertical blanking (retrace) periods permits the real time screen update required in an animated display.

Write 233

Low Cost Automated Drafting—The Next Paperwork Revolution

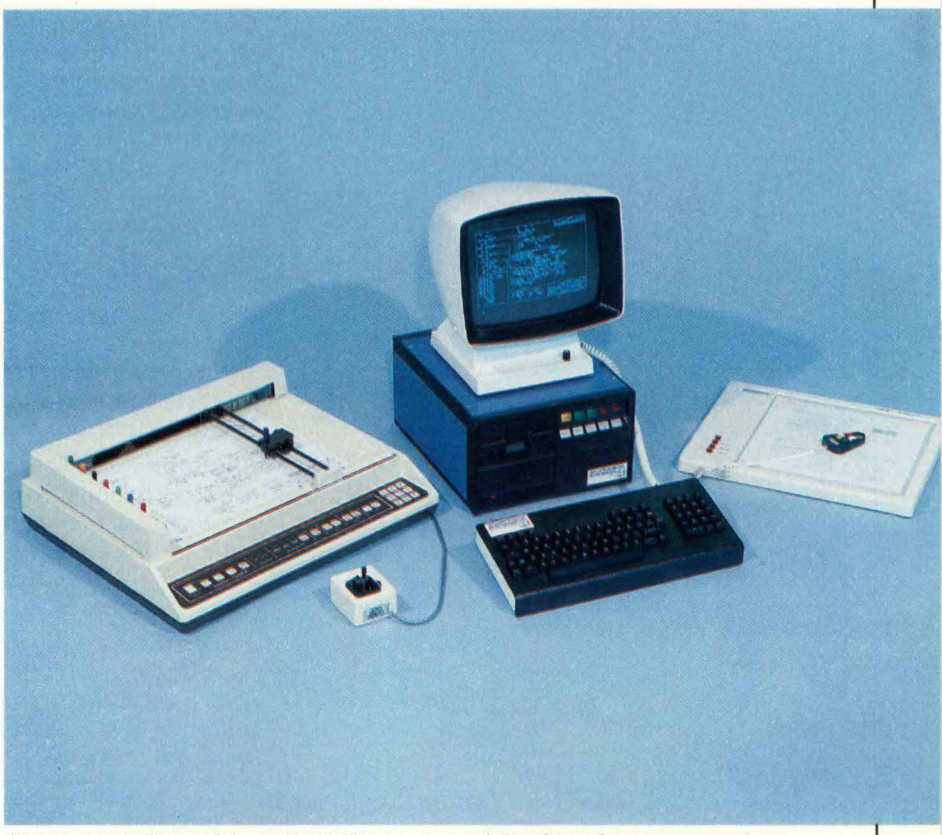


Figure 1: Andromeda's A-CADS/1 Automated Drafting System.

A new class of Computer-Aided-Drafting System (CADS) from the LSI-11 systems house, Andromeda Systems, Inc. (Canoga Park, CA) brings three dimensional CAD technology in at a $24K price tag for a complete turnkey system. The system includes software, CPU, CRT terminal, disks, a "B" size plotter and digitizer, and approximates the salary and overhead of a "B" draftsman.

Andromeda has utilized its standard products to assemble the A-CADS/1 system. The system card cage contains a DEC LSI-11/23 CPU, 64Kbyte RAM, five serial RS232C ports, a video display controller, a floppy/Winchester controller, joystick interface, and several expansion slots. Mass storage is a 5Mbyte Winchester, and removable storage is with a 512Kbyte floppy. The I/O devices include Andromeda's VDT11-C graphic display terminal with a 512H by 256V resolution raster display. The display can emulate the Tektronix 4010 in the graphics mode and DEC's VT52 in the alphanumeric mode for text processing. A joystick is the primary input device for creating drawings. The ability of the CRT terminal to handle both graphics and text eliminates the need for a second terminal, common with many earlier CAD systems. Completing the hardware complement is a "B" size plotter that can select, under system controls, up to eight pens for varying color or line width and an 11″ by 11″ digitizing pad with a four button cursor.

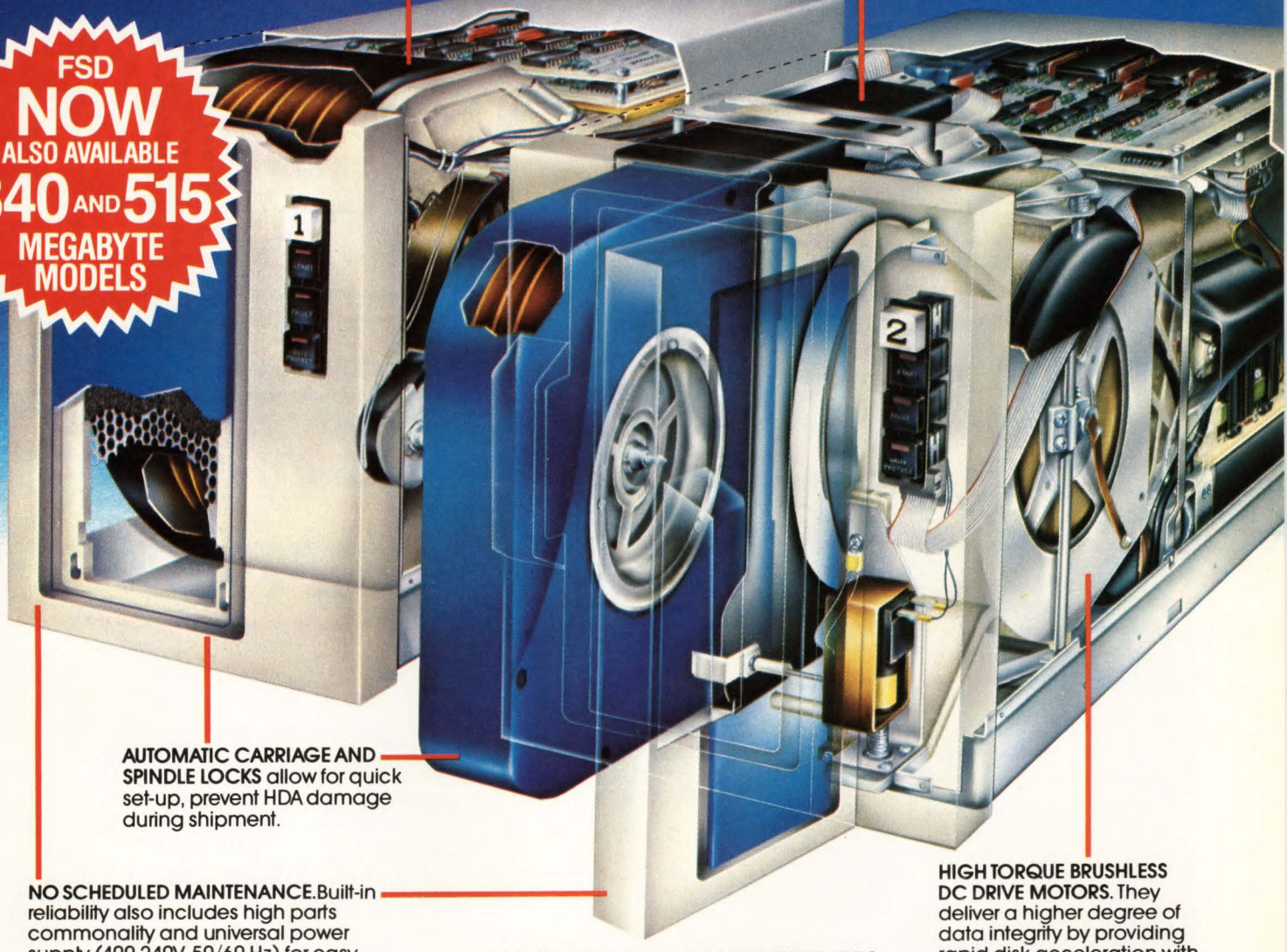
Andromeda Systems, Inc., 9000 Eton Ave., Canoga Park, CA 91304. **Write 315**

INTRODUCING LARGE-DISK PERFORMANCE IN DRIVES HALF THE SIZE

MODEL 9715 FSD. With 160 Mbytes in a sealed module, you get the same capacity, speed and performance as the CDC® Mini Module Drive (MMD) in a unit one-half the size.

MODEL 9710 RSD. With 80 Mbytes in removable data packs for unlimited storage. Has the same capacity, speed and performance as a CDC Storage Module Drive (SMD) in a unit one-half the size.

FSD NOW ALSO AVAILABLE 340 AND 515 MEGABYTE MODELS



AUTOMATIC CARRIAGE AND SPINDLE LOCKS allow for quick set-up, prevent HDA damage during shipment.

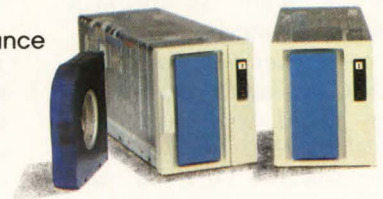
NO SCHEDULED MAINTENANCE. Built-in reliability also includes high parts commonality and universal power supply (100-240V, 50/60 Hz) for easy installation worldwide.

BOTH MEET FCC, UL, CSA, VDE STANDARDS FOR A STAND-ALONE UNIT.

HIGH TORQUE BRUSHLESS DC DRIVE MOTORS. They deliver a higher degree of data integrity by providing rapid disk acceleration with minimum head drag. (Both models)

THE FSD™ / RSD™ SERIES

Both 9710 and 9715 Drives use LSI circuitry for all read and write, fault, transmitter/receiver functions and a μP for servo control, for full performance in half the space. For more data call your local Control Data OEM Sales Representative or write: OEM Product Sales, HQW08X, Control Data Corporation, P.O. Box 0, Minneapolis, MN 55440.



CONTROL DATA

Information Hot Line 1-800-621-1776
in Illinois 1-800-572-6724

Write 14 on Reader Inquiry Card

Industry Spotlight: The DEC-Compatible Market

DEC and the plug-compatible vendors have a symbiotic relationship that has created prosperity for both.

Photo courtesy Digital Equipment Corp.

Adolf F. "Sonny" Monosson is chairman of American Computer Group companies that have been in the DEC market 15 years as distributors, OEM, and used computer dealers. He is the publisher of Monosson on DEC, *a subscriber newsletter for users of DEC products. American Computer Group, P.O. Box 68, Kenmore Station, Boston, MA 02215. (617) 437-1100.*

by Sonny Monosson

The DEC-compatible market is a phenomenon in the computer industry. Its size exceeds DEC's revenues, and if the spectacular 37% a year growth rate continues, as expected, it will become an industry exceeding $6 billion in sales in 1985.

DEC owes its amazing growth record (that has made it a $4 billion corporation in 26 years) partly to the OEM and DEC-compatible companies that have filled out its product line and helped it expand its markets. DEC and the plug-compatible vendors participate in a symbiotic relationship that has created prosperity for both. Although the relationship has changed in many respects over the years and is doing so right now, it shows every sign of

continuing to flourish.

What are some of the factors that have contributed to this growth and how are some of them in the process of change?

First, DEC's own rapid growth could not keep up with customers' needs. DEC's President Ken Olsen admitted to this at the company's last annual meeting when he said that if DEC did everything its customers demanded, it would be an $80 billion company; even DEC cannot grow that fast. The larger a company becomes, the slower its growth rate as it matures; the difference between the $4 billion the company is grossing today and the $80 billion demand for new products has opened up phenomenal opportunities for third-parties.

Second, because DEC CPUs created the first "user friendly" environment and have been widely dispersed in technical markets and in education, as well as to the third-party market, they have been in the hands of especially independent users. These people have been unusually enterprising in their use of third party products and services.

Third, the companies that have entered the DEC-compatible market are inventive. Unlike the case of IBM, where the plug-compatible market is heavily dominated by look alike products, the DEC-compatible market is unique in its diversity.

In the early days, DEC produced low-cost, high-quality relatively small computers. The main users were OEMs who integrated DEC computers into other products, such as test equipment in the case of Teradyne and Fairchild. Other users were timesharing companies such as UCC, Cybernetics, Tymshare, and Applied Logic Corporation.

Diverse 3rd Parties

OEMs still represent a sizeable share of the DEC-compatible market. DEC OEMs in CAD/CAM pioneered that field, and together with DEC's own position in CAD/CAM, they dominate that market with sales of about $700 million. Other new industries created around DEC are the fields of hardare plug compatible products such as add-on disk drives, tape drives, videos, printers, memories and communications equipment.

The DEC software compatible industry includes DEC commercial OEMs, $200 million industry that adds specialized or customer software to the hardware, and independent software vendors that gear their products to DEC computers. These companies range from those offering operating systems such as UNIX to run on DEC hardware, to those aiming at growing markets for vertical applications software that runs on DEC operating systems.

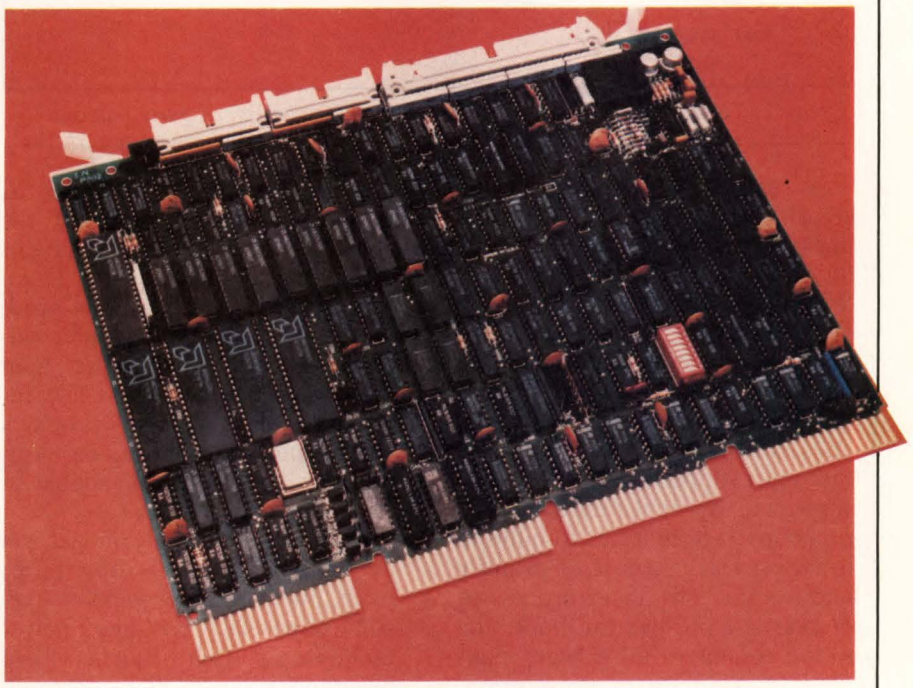
Other companies offer maintenance and other services for DEC systems—consulting, training education, publishing, seminars. The large base of purchased DEC equipment supports a used market in DEC hardware in excess of $200 million, second only to the IBM used market.

DEC's initial markets were those least interested in commercial applications software. Their approach to diversifying into many markets has been to provide the tools for writing applications programs to end users and third-party software suppliers—whether OEM system houses or independent software vendors.

DEC's public Unibus contributed to the ease with which third parties could attach special hardware devices. This was emphasized recently when IBM, trying to sell its 4300 into technical markets, developed its own Unibus interface so it could offer the advantage of special peripherals that were originated for DEC equipment to potential customers.

Poised For Action

The most important factor in the success and the future success of the DEC-compatible market, however, lies in its flexibility. Sometimes, new opportunities for third-party vendors arise by happenstance. For example, several factors have stimulated the growth of the third-party maintenance business. For some companies, major growth took place in 1978 when the Services Contract Act (setting wage and benefit standards for technicians working under maintenance contracts on government systems) was newly



MDB Disk Controller for LSI-11 systems.

interpreted to also include computer maintenance technicians. Vendors refused to bid contracts under the act at the outset giving third-party maintenance firms a much larger foothold in government business.

However, a larger factor in the growth of third-party maintenance is the maturity of DEC's own field service organization. Third-party firms depend heavily on manufacturers' documentation, diagnostics, spare parts availability and trained technicians, whom they are happy to hire away from computer vendors.

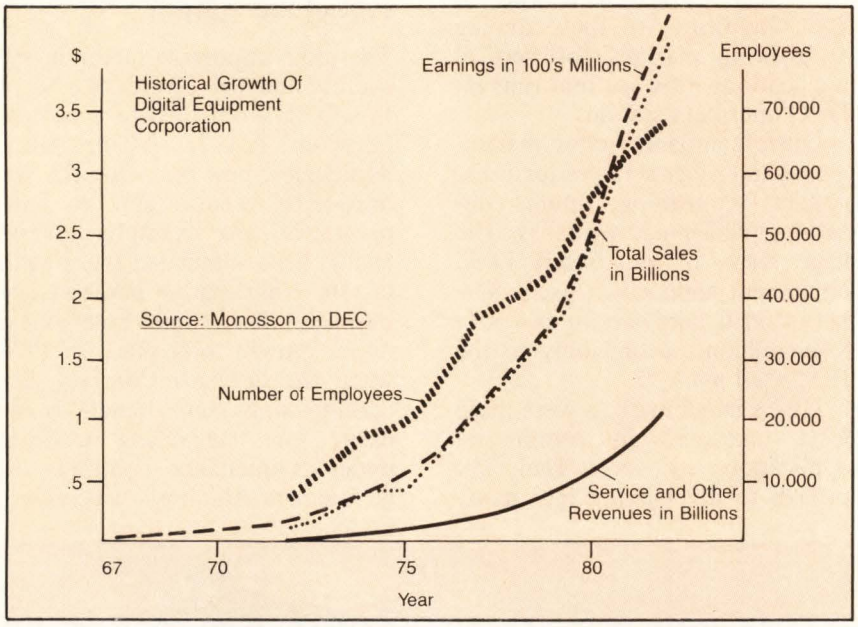


Figure 1: The rapid growth of DEC that has created vast third party markets.

As DEC has become an increasingly mature company, timeliness is a factor offering opportunities to the third party market. With its huge installed base, DEC now has many considerations to take into account when introducing new products. Factors include the number of operating systems and systems software packages that must support products and be supported by new products. The reliability factors it has to build in to support a system is of primary importance. The sheer process of preparing a product for marketing to the volume of DEC users mandates gearing up manufacturing, documentation of hardware or software, and training sales and service personnel support.

The Fit Survive

For many years mass storage provided a lucrative market for third-parties providing storage subsystems for DEC products, and propelled such companies as Emulex and System Industries into prominence as controller manufacturers and subsystem integrators. They could offer systems at 85% to less than 50% of the cost of buying them from DEC because DEC depended on a captive customer base for its low-cost CPUs to hold to the same approximate profit margins on storage peripherals. Even though those were based on products it bought from outside vendors, it cost DEC more than those they manufacture. The result is that the "buyout" products were especially high-priced compared to alternatives available in the independent market.

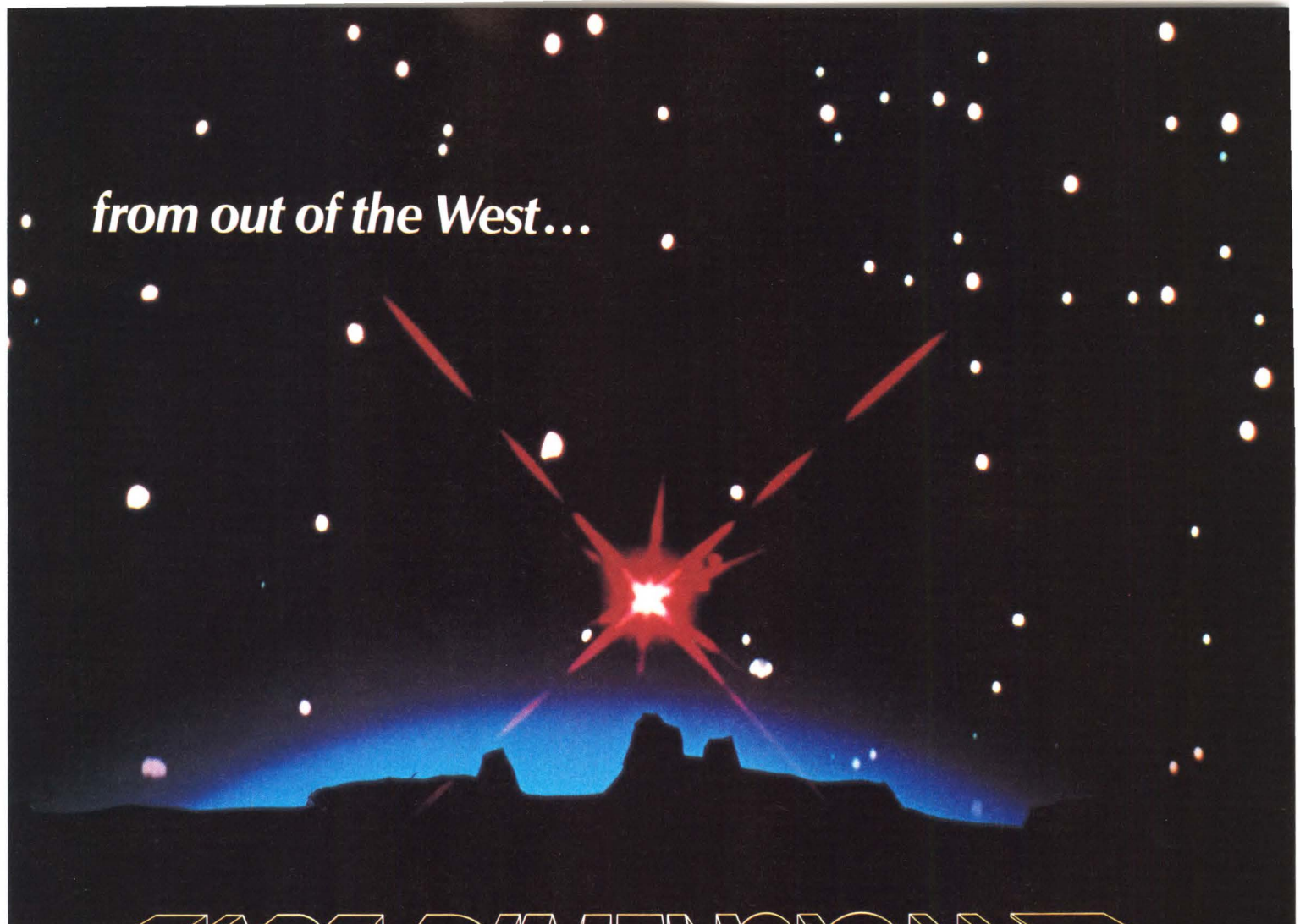
Obviously, price advantages can be undercut if DEC itself drops price, but third-party vendors may still shine in providing newer technology. Third-parties have benefited from offering more advanced technology first. In the case of memory, for example, third-party vendors usually offer new memory boards ahead of DEC, at a point when the ICs are only available in quantities too small for DEC to use. This happened in the case of 64K RAMs and no doubt will be repeated as 256K RAMs reach the market.

Alternatively, flexible companies find new products, filling niches in DEC's product line with solutions for the DEC user. When the 64K RAM was introduced, vendors sold them for VAX CPUs in 1 Mbyte boards with three blank boards interconnected to emulate DEC's four ¼ Mbyte boards before DEC supported 64K chips. With new competition from DEC storage products in the offing, Emulex, for example, is moving into communications controllers, doing well with direct memory access devices to add on to DEC's DMF-32 VAX interface.

Besides filling gaps in new DEC product lines, the third-party market often profits by becoming the saviour of users of older products, or in providing some of the aids to those users in the process of converting. Evans Griffiths and Hart, Inc. did this in offering ROSS, the first bridge to VAX computers for users of DEC's PDP-11 RSTS operating system.

Some of these examples illustrate a pattern in the relationship of the DEC-compatible market to DEC itself. That relationship is happiest when DEC-compatible vendors are providing products complementary to DEC's own products rather than in direct competition with them, offering products DEC has not yet gotten around to including in a new product line, filling gaps in the DEC line that are too small for it to bother with, or catering to users of older equipment when DEC has moved on.

Sometimes these opportunities are a double edged sword; compatible product vendors must be nimble to survive, because when opportunity becomes great enough, DEC will attempt to make the



TAPE DIMENSION III

DEC COMPATIBLE CONTROLLERS

Tape Dimension III is the only buffered tri-density (GCR/PE/NRZI) TS-II™-emulating controller on the market. The combination of its unique asynchronous handshake design and 64K byte buffer enables it to take full advantage of bus speeds without the risk of causing data late conditions in other bus transfer operations. It makes Tape Dimension III particularly adaptable to systems with high speed disk drives.

The 64K byte buffer provides total immunity to data late conditions, even at high-speed data rates on a highly populated peripheral bus. In fact, Tape Dimension III actually has greater capability than the TS-II!

Tape Dimension III is completely software-transparent to the VAX™ and PDP-II™ Unibus environment including diagnostics in VMS.

The Tape Dimension III controller supports up to four dual-density (Pertec compatible) drives or four tri-density (STC or TELEX type) drives. It is a single embedded hex PC board that fits into any standard SPC slot.

This new dimension in tape transfer dramatically reduces the ratio of protocol to information data. And tremendously increases the efficiency of Unibus utilization. Find out how much it can improve your system throughput. Call or write today for complete information. WESTERN PERIPHERALS, Div. of WESPERCORP, 14321 New Myford Rd., Tustin, CA 92680, Tel: (714) 730-6250, Cable WESPER, TWX 910-595-1775, Telex 472 0629. Wesper International GmbH, Tel: 089 982420. Wesper International (U.K.), Tel: (44) 0276-20934.

TS-11, VAX and PDP-11 are trademarks of Digital Equipment Corporation.

western peripherals

Division of WESPERCORP

Write 15 on Reader Inquiry Card

market its own, as in the case of storage products.

At present, those risks are greater in the case of hardware vendors than for independent software vendors. One reason is that DEC still proclaims itself to be a hardware vendor, first and foremost. It has concentrated on systems software, and as a result, applications software supported by DEC is limited to relatively few products with wide markets—word processing, for example. The second factor is that the company is in no position to keep up with the demand for software in a market where software increasingly sells the hardware.

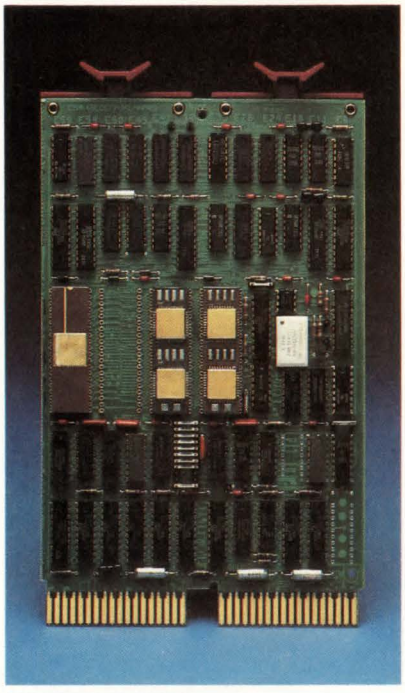
Software Drive

The company's initial response to the software challenge was its traditional attitude "we can do it better." In the case of its word processing software, it built on an outside product to create its own. DEC's approach to third-party products is cautious. Hardware vendors are all too aware that users are quick to forget a hardware vendor's disclaimers of responsibility for independent software it recommends to go with its products. If the software doesn't work, the user is inclined to refuse to pay for the hardware.

However, the increasing importance of software has led DEC to rely more on third-party products and new approaches to independent software vendors. Drawing third-party software more closely into alliance with them strengthens DEC's ability to offer total solutions to its customers.

Besides acquiring licensing rights to outside products and then enhancing them, new moves include an increase in third party software that DEC gives some kind of stamp of approval but does not support, as well as products that are available for DEC systems which it merely catalogs for referral purposes.

Timeliness is also an important factor, and DEC has one major precedent for the success of loose arrangements with independent



DEC's LSI-11/23

software vendors.

In the case of CAD/CAM, DEC acted quickly to build an arsenal of the best CAD software by ensuring that the most respected programs in the industry—mostly originated in the '60s and early '70s on IBM and CDC mainframes—were converted to run on VAX. The success of that drive has put more CAD software on DEC equipment than that of any other single manufacturer's and has been the largest factor in the adoption of VAX as the standard computer for CAD.

DEC jointly markets the packages, such as NASTRAN, PASTRAN, ANSYS with, respectively The MacNeal-Schwendler Corporation, PDA Engineering, Inc., and Swanson Analysis Systems, Inc., but the agreements are not exclusive and DEC does not support the products. In the manufacturing market, where it set out to develop exclusive marketing agreements with third party vendors and now has licensing agreements for such packages as Interactive Information Systems, Inc.'s MRPII software, which it support, it has taken longer for DEC to achieve a foothold in the market.

Changing Relationships

DEC's need for software and strategy for offering "turnkey" solutions to users in partnership with independent software vendors offers independent software suppliers a range of opportunities for gaining new prominence for their applications packages.

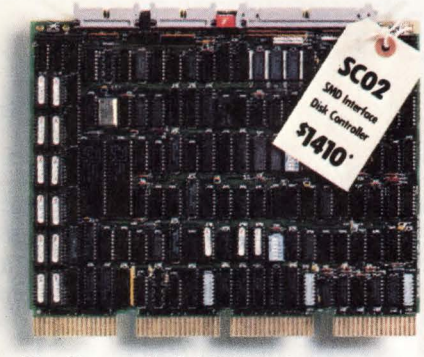
It also places DEC in more direct competition with its OEMs, a situation DEC recently recognized during its reorganization process. The reorganization eliminates separate sales responsibility for end user and OEM customers that in the past had end user product groups at DEC competing with its OEM product groups, when, in effect, OEM customers were trying to sell the same end user DEC was courting.

To improve that state, the most appropriate vendor is to be chosen in terms of the user's needs. The new system is backed up by a dual sales credit system whereby the sales representative receives credit for a sale whether he makes it directly or whether the OEM makes it.

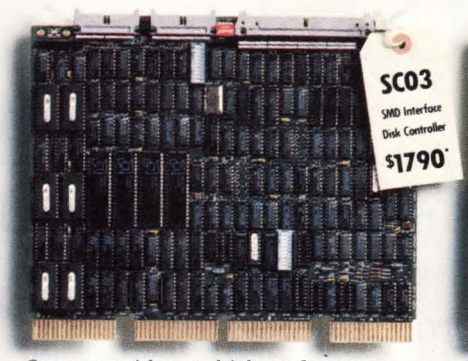
As software becomes the dominant ingredient of any system and the major source of revenue in the computer industry, can DEC leave these software revenues to the DEC-compatible market? Eventually, the answer has to be no. It must capture software revenues by developing and acquiring software and becoming a software publisher for independents. In different markets and at different times during the 1980s all these strategies will affect the DEC-compatible market, where such changes, and the flexibility they require of participants, are the name of the game.

They will be part of the continuing growth of the DEC-compatible industry. With its 600,000 computers in place, DEC has provided a market base for a unique entrepreneurial industry. It is one that has made many millionaires and will make many more to come. □

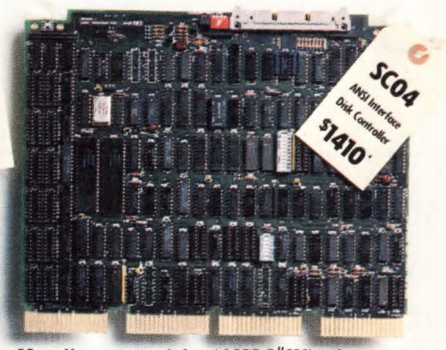
The LSI-11 controllers with features comptrollers love.



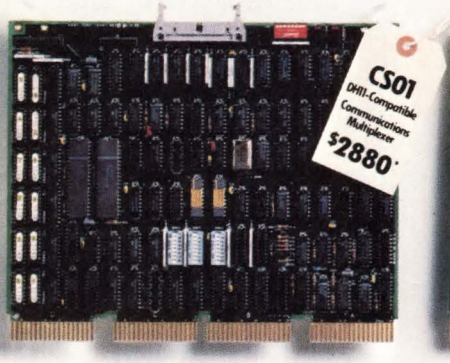
Handles small 12-80MB disks, emulates RP02/03, RK06/07 and RL01/02.



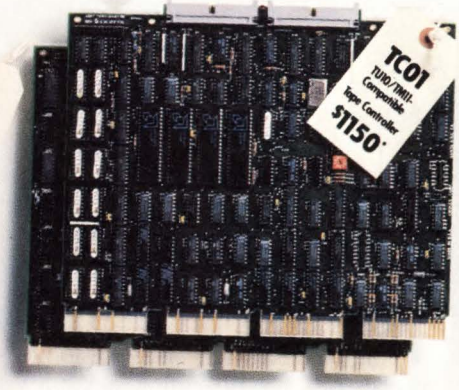
Operates with new high-performance 80MB and larger disks on LSI-11/23.



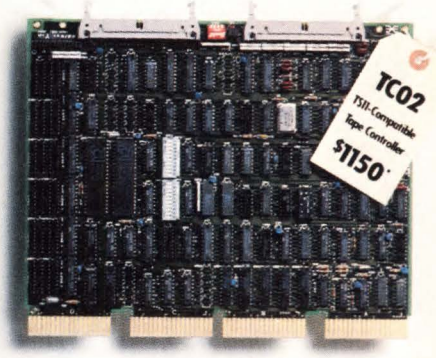
Handles up to eight ANSI 8″ Winchesters, emulates RK06/07 and RL01/02.



Handles 8-64 channels, 16-bit word transfers (DMA), 22-bit addressing. (16-channel price)



Dual density at up to 75 ips, handles up to four ½″ transports.



Coupler works with all NRZI, PE, GCR formatters at speeds from 12.5 to 125 ips.

*Quantity 100

Handles new cartridge Winchester disk drives, emulates RLV11/12.

Flinty-eyed finance types are push-overs for Emulex controllers.

And why not? Emulex controllers have great figures.

DEC LSI-11 users simply don't pay extra for higher Emulex quality, performance and reliability. In fact, Emulex controllers are priced to be highly competitive with the lower quality brands. And that's just the beginning.

There's no up-front investment because Emulex controllers are totally software transparent to LSI-11 CPUs. No special software drivers, handlers or tweaks required.

Smart comptrollers don't tie up cash in needless inventory. With Emulex's remarkably fast delivery, inventories can be kept economically small.

Quantity discounts are another opportunity for comptrollers with sharp pencils.

With Emulex you can mix and match across a very broad product line of Q-Bus, Unibus & VAX controllers so it doesn't take long to bring prices down even further.

Knowledge that Emulex products work (at up to 72,000 hours MTBF) is important, too. But when support is necessary, comptrollers are pleased to know that nationwide applications assistance, training, and technical support is only a quick phone call away.

Great figures?

Write or call Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626. Telephone (800) 854-7112 toll-free. In California call (714) 662-5600.

EMULEX

The genuine alternative.

Write 31 on Reader Inquiry Card

Display Processors–The Design of Computer Graphics Systems

A rapidly expanding marketplace, coupled with semiconductor technology enhancements are forcing designers to improve display performance.

by Jerry Borrell, Editor-in-Chief

The design of picture processors or graphics engines for use in computer graphics has become one of the hottest arenas of computer design. A rapidly expanding marketplace, coupled with semiconductor technology enhancements, are forcing designers to improve display performance and speed while minimizing cost. The marketplace has become so volatile that some designers indicate for the first time that graphics has begun to shape developments in semiconductor devices.

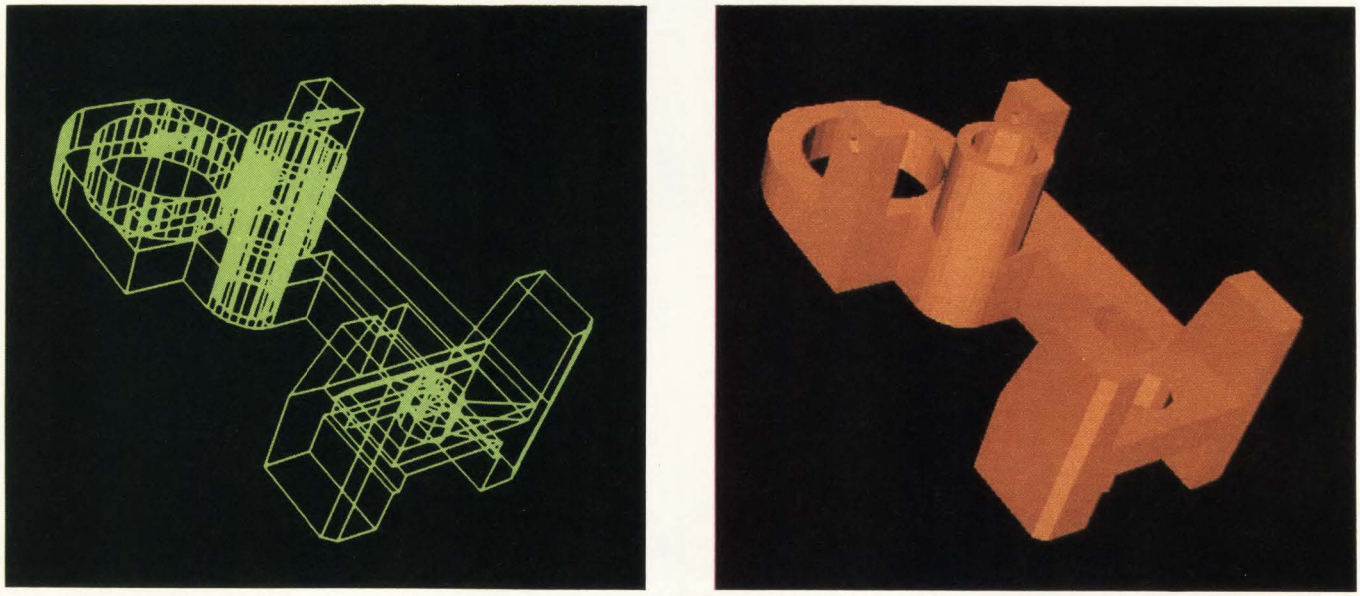
Four areas of development in these designs should be considered: the display requirements, the internal systems architecture, the semiconductor technology implemented, and the diagnostic functions.

One aspect of these changes that is of importance to computer system designers and OEMs relates to the areas where new graphics processors are providing flexibility —in board level products, in rack mountable systems, in standalone systems, or as terminal support for graphic workstations. All of these configurations indicate markets that graphics processors will enter.

Of less interest to the present markets for graphics processors, but of great potential importance, are the small companies making tremendous software investments to allow less powerful systems to emulate the capabilities of larger systems. The advantage these small companies have is in their low overhead and capital costs allowing their designers to squeeze the most performance from hardware through software development.

Display Technology

This summer's NCGA and SIGGRAPH shows demonstrated an industry-wide demand for higher resolution displays. If 1982 was the year of 1024×1024 developments, this year's events showed that 1280×1024 has become the new "benchmark". Another issue of prominence is the ability to refresh the display at 60 Hz, or non-interlaced performance rates—both for aesthetic purposes and to support dynamic displays. Manufacturers have voiced mixed reactions to



A solid model of a machine part displayed and rendered on Cubicomp Corporation's CS-5, a single board display processor for the IBM PC, at 512 × 512 resolution, and 16 bits of pixel memory.

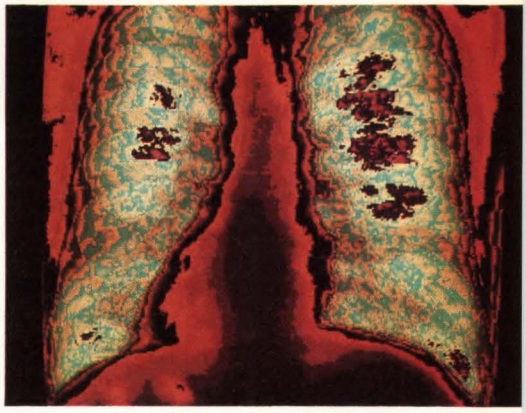
these trends; while some feel that the race for ever higher resolution and refresh are only part of the continuing "specsmanship" battles, others point out that ergonomic considerations for better quality displays should play a more important role. In CAD environments where developments are bringing image quality displays (solid models) and improved line drawing to the forefront, manufacturers note the genuine need for higher quality displays, some claiming that high resolution is an effective way to provide anti-aliasing. Whatever the justification, there is clearly a need for faster refresh rates if displays of 1280×1024 are to be used in normal light environments.

As the demand for higher resolution and refresh rates continues, the ability of manufacturers to meet it does not necessarily follow suit. The ability to refresh the one million plus pixels for a single screen at 60 Hz requires a communications bandwidth of over 100 MHz and affects considerations such as location of the display and processor, electro-magnetic emissions, and data processing. Others note that there is a shortage of digital to analog convertors that can be used to drive the electron guns of high resolution displays. Most manufacturers claim that many problems remain with the drive electronics, yoke design, and reliability of high resolution systems. In addition, the demand for tubes capable of supporting this type of display is taxing an already short supply. Questions such as these, raised by the continued demand for higher resolution will be examined in the October *Digital Design*.

System Architecture

Hardware. One of the most evident trends in the design of new graphics engines is in the physical size of the products. More powerful logic, processors, and semiconductor memory have made it possible to manufacture systems that offer a wide variety of display characteristics based upon the three key criteria of system design: cost, performance, and functionality. At the low end, graphics processing on a single board is offered by Metheus, Modgraph, Cubic, Ithaca, and Genisco, who have designed processors with extremely dense packaging. Using such a product in a minicomputer, for instance, allows a quick way for a company that may have relatively little experience in the field to add graphics capability. Some OEM accounts become so large for these vendors that they can afford to make custom modifications or interfaces available.

Many of these single board products approach the current practical and possible limits in terms of density—some containing as many as 400 to 500 ICs. Several of these manufacturers do not use computer aided design in their developments as one might expect, and many of their boards have been designed with manual techniques. Reasons cited include the lack of a system with sufficient software capability to handle aspects of the design such as multiple layer boards, circuit density, and circuit routing. Indeed, the great strength of young companies is the ability to implement designs ahead of other manufacturers who offer multiple board systems and who more typically use CAD in designing their PC cards.



An enhanced x-ray, taken using a Genisco GCT 3000, at the University of California at Irvine Medical Center.

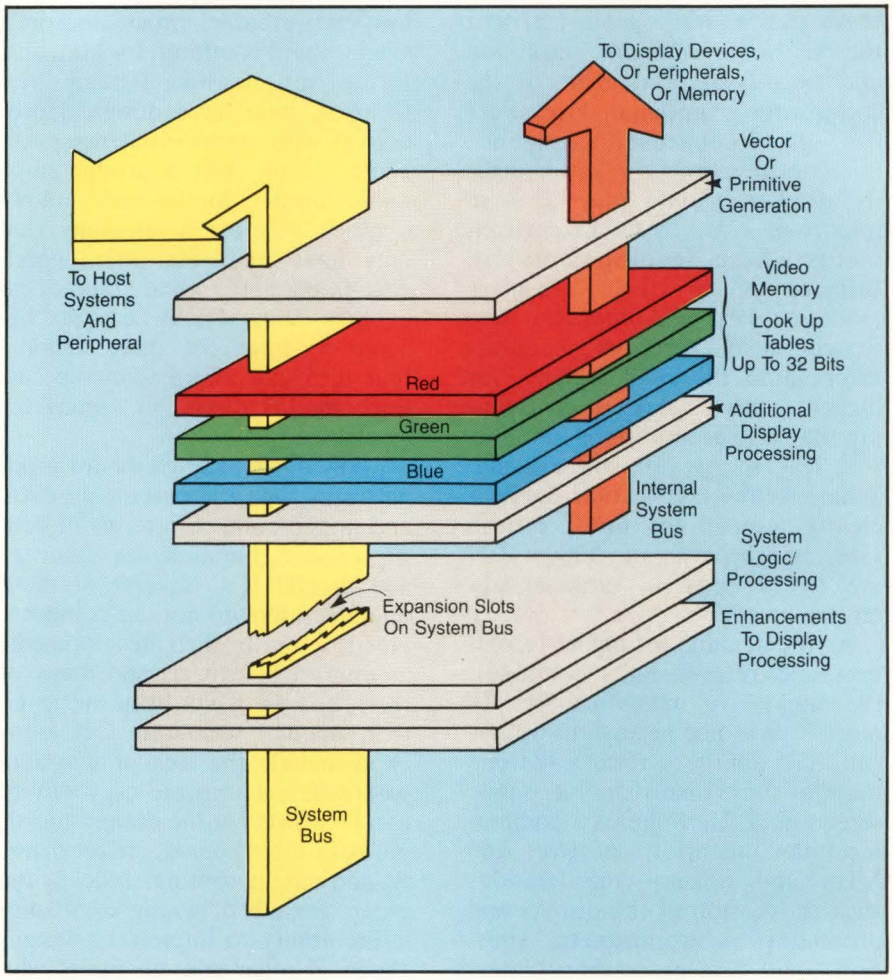
Communications/Architecture. Several manufacturers have traditionally provided systems with expandable backplanes. Their approach is to provide systems with "top end" capability which essentially means keeping a card cage arrangement. This summer's announcements have shown that firms such as Aydin, Comtal, Jupiter, Seiko, Adage, Megatek, and Ramtek are moving to stay ahead of the one/two board systems providers by upgrading capabilities of their larger systems. Because of their multiple board construction, the designers must make decisions concerning choice

The G-2000 Product 1 line from left to right configured as an OEM product, a standalone graphics system, and a system component for display processing, demonstrating the flexibility offered to manufacturers with today's display processors.

of bus structure and backplane construction. The amount of data used in this type of system is so vast that to support the fast refresh of pictures there must be internal bus connections for discrete portions of the system. For example, the video refresh memory planes may have a direct channel for the graphics processor or a vector display generator. These intra-system data communications links leave the system bus open for processing and screen update.

The majority of systems, however, take one of three approaches to internal communications: conforming to the structure of a well-defined bus such as Unibus, Multibus, Versabus, or Q–bus; closely emulating one of the former buses; or providing an interface through the system bus (possibly proprietary) that can connect directly to the more common bus. Metheus and Aydin for instance will provide interface cards for the Multibus that will slot into their display processor or chassis. Genisco has provided a Multibus connector as an integral part of its newest single card system. Ramtek has one of the more complex architectures with an internal 16–bit video bus, a 32–bit system bus for the processing architecture, and an additional number of channels for activities such as picture processor/video look-up table refresh.

It is usually typical for a graphics environment to have several input or output devices ported to a system such as plotters, printers, or digitizers. Unless a standard interface is provided these costly peripheral devices may become a reason for not acquiring a new system. Because memory requirements are so great in graphics systems, manufacturers must also insure adaptability through common disk storage interfaces such as SMD or SASI. The advantages of providing this sort of flexibility at a time when disk memory cost and capacity are changing so rapidly are self evident. Another reason for this conformance to standard buses, particularly for graphics applications is to insure access to the existing applications software—as the development for



High-end display processor system.

code is one of the most costly issues. Two manufacturers, Raster Technologies and Lexidata, bridge the gap between large multi-board systems and single board products. Both companies have had great success recently with OEM integration of their 2 or 3 board configurations.

Semiconductor Developments. There are three areas of primary interest in semiconductors to designers working with display processors: CPU functions, memory, and logic. Each of these areas has been developing at a different rate, necessitating that designers implement new semiconductor products not as they might wish but when they become available. Some of the more conservative manufacturers will not use a product until there is a second source manufacturer, introducing a further lag in new products. In the past, a good example has been 64K RAMs; today it is 256K RAMs that are in short supply.

Two areas of development potential are dedicated graphics chips (not withstanding the NEC 7220 which is more suitable for business graphics unless used in multiple configurations) and the use of gate arrays or custom logic. There are several graphics processors of advanced capacity under design but none are in a production stage to date. One of these (from Silicon Graphics) is based upon the Stanford Geometry Engine from Clark which was discussed at the SIGGRAPH 1982 event.

CPU/Processing Functions. The past two years have seen several techniques mature for the construction of graphics processors. The seeming lack of progress in dedi-

LEXIDATA·3700

The Lexidata 3700 has the speed and performance you've come to expect from the leader in high resolution displays.

In terms of speed, the 3700 writes in pixel blocks automatically (e.g. for fills and horizontal vectors). This is continuous speed, not burst speed, at 42 million pixels per second.

42 million pixels per second

Its pixel-by-pixel rate is also continuous and fast. Fast when you're generating vectors. Fast for individual pixel update–crucial for imaging applications.

This speed is augmented by state-of-the-art 1280 x 1024 color at a flicker free 60hz refresh.

In terms of performance, the 3700 comes standard with Writable Control Store (WCS), enabling the user to implement his own high speed routines. Additionally, WCS also gives direct access to the main processor, so even complex functions run fast. There's also separate storage for over 1000 characters in user-definable fonts.

Remember, too, that the 3700 stems from the 3000 family, the most popular high-performance line ever developed. The 3700 is a *complete* performance package offering speed and features that live up to your expectations.

The Lexidata 3700. Fasten your seat belts.

For quick response call 1-800-472-4747 (in Massachusetts, call 617-663-8550) or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

LEXIDATA

The clear choice in raster graphics.

Write 24 on Reader Inquiry Card

cated processors for graphics functions is due in part to the relatively low volume of demand for the products. While general purpose μPs may have tens of thousands of applications, a graphics chip is more likely to be produced in the thousands, due to the fact it is more specialized. Understandably, this inhibits the major semiconductor houses from introducing graphics products.

There have been a few predominant approaches to processing for graphics generators: dedicating a μP to both general processing functions as well as graphics processing; constructing custom logic configurations—for example 2901 bit slice processors of varying word length, processors from ECL or TTL logic; and implementing the NEC 7220 graphics chip which is second sourced by Intel. In the first case, the movement is continually towards the latest generations of μPs—with Motorola's 68000 family having been the most popular over the past two years. 2901s have dominated in custom logic configurations, but there are now many alternatives including the 29016 and 29032 16-bit processors from AMD. Programmable Array Logic and Programmable Logic Arrays are also making initial appearances. In the latter approach, use of the 7220 in multiple configurations has become the rule. Seiko uses up to five of the chips in its latest desktop terminal, Genisco two.

Each of these approaches has advantages and disadvantages. The obvious constraint in the use of a dedicated μP is that most are constructed for general applications and may prove to be too slow for graphics generators. Alternatively, these processors may be more easily programmed than devices such as TTL or ECL. What they lack in performance, their broader applications compensate for. Bit slice TTL processors (2901 type) are very fast and have become an industry mainstay, especially in creating wide word length for programming or in high speed applications. However, the devices must be programmed in microcode, which by some estimates has a 50:1 ratio in programming time when compared with assembly language. The speed is acquired by implementing software as firmware instructions, the tradeoff being that of inputting the code. In the last of the approaches (dedicated graphics chips) the NEC chip is widely popualr with many graphics system designers, since it allows a one-chip approach to implementing graphics capabilities. When an attempt is made to use it in applications where high resolution and color are a key, however, the chip must be implemented in groups of three because each may only adequately control one color gun at any one time. Thus, programming time for certain basic functions such as clipping and zoom are saved; however, the trade off is made when a wider range of colors is needed where several of the chips must be used.

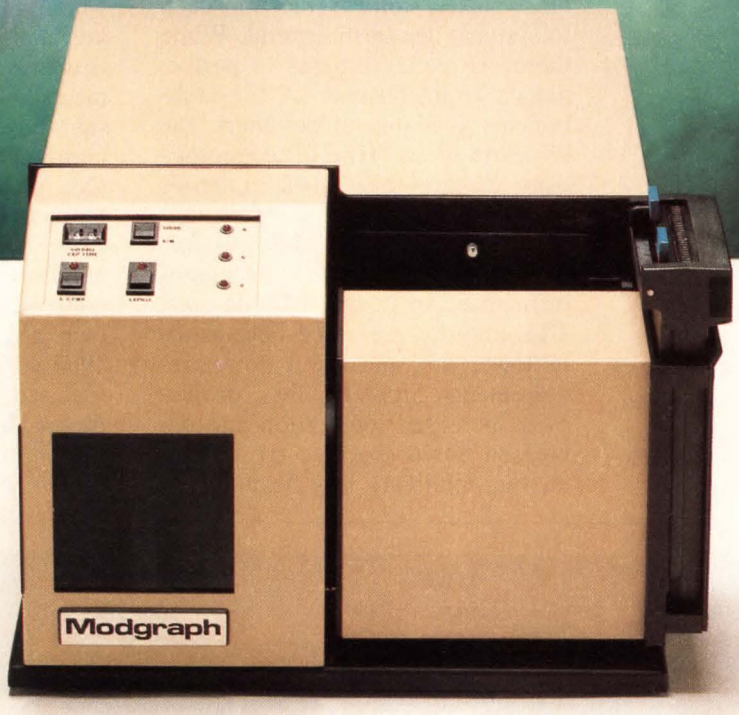
The Megatek 7200 Graphics Engine's PC layout and computer aided engineering displays. The system has both a 32 bit system bus and a 16 bit peripherals bus.

Memory. Memory is one of the crucial aspects in the design of graphics processors because of the massive amounts of data that must be accessed to create and manipulate displays. Designers are concerned not only with the amount of semiconductor memory that must be directly accessible but the speed with which the data can be read into and out of the memory. The trend towards more realistic imagery or graphics has the effect of increasing the need for memory. RAMS are even replacing ROMs and PROMs for instruction stores because of the need to perform fast calculations and to carry out elaborate programs as display lists.

Each plane of memory for a 1024×1024 system requires about one million bits and the number of planes used must increase if a display is to approach image quality. The availability of 64K RAMs has become important because it allows designers to minimize the amount of board space required for memory planes. However, several manufacturers indicate that the use of 64K RAMs can introduce further problems with the rate of data refresh because there is only one path from which the information can be read. Some engineers have pointed out that 16K static RAMs with their superior speed are a preferable alternative; however, they remain expensive. This situation may change because of developments from INMOS and others to provide a cache memory on board their 64K chips. Such a memory store would allow data to be read out at four bits at a time.

It is worth noting that one of the first applications of 256K DRAMs will be that of Aydin, who is implementing the chips on their processor board for direct access memory

The Modgraph Challenge.

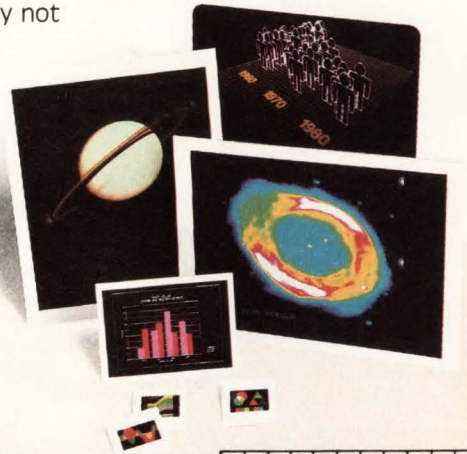


When you select a color graphics camera, are you buying image quality or bells and whistles?

Crisp clear lettering. Images so sharp that the colors seem to jump out at you. Multiple interlace that eliminates raster lines not just on SX-70 prints but also on 8 x 10 Polaroid® 808, 809, and 891 film. Images that fill the entire frame without a black border or fuzzy corners. Our images are judged the best — picture to picture, demonstration to demonstration.

Modgraph, the **Smart Graphics™** company, wants you to know what the proper combination of optics, high resolution flat face monitor, filters, and electronics can mean in terms of image quality. So if you are about to buy a color film camera to show your company's image, why not buy the camera that produces the best images. The Modgraph **Smart Graphics™** Color Camera.

Our color cameras produce the best 35 mm slides, SX-70 Polaroids® 4 x 5 or 8 x 10 color prints...You be the judge. Drop us a line, or give us a call. We'll arrange for a demonstration and show you how the best image quality can be yours.



Write 8 on Reader Inquiry Card

Modgraph

Modgraph, Inc., 1393 Main Street, Waltham, MA 02154 (617) 890-5764

Ramtek's 9645 may be a 16-bit display processor, or a 32-16 bit system with up to 5 68000 based cards for graphics operations.

for the 8086/8087 processor pair.

Seiko has taken a unique approach in the packaging of its 64K RAMs. In Seiko's new 2414, the RAMs are mounted as memory modules without DIPs, but with connectors on four sides. Eight of the memory chips are used in a module.

Logic. The changes occurring within the implementation of logic most closely follows the approach to systems design in general. While there are enhancements in performance characteristics of the components available to designers, the selection of one type of technology over another reflects the tradeoffs in cost, performance, and functionality. For instance, while performance of ECL parts may be superior in speed to that of TTL devices, TTL may be preferred because of its lower cost and lower power requirements. Similarly, PAL devices offer increased integration and decreased board space to the designer, but relatively less flexibility in programming and higher cost. They do, on the other hand, allow for the faster debugging of a board. Most manufacturers have made the most judicious selection possible in using these devices in terms of overall performance or cost despite the inevitable rush to make use of large scale integration.

ECL usage typically is found in the video refresh area of the system where the higher cost and power are justified by their ability to process more data. However, improvements in the complexity of TTL design have given these devices an additional advantage in flexibility. One of the events of most importance for custom logic is the use of gate arrays. To date, only Genisco indicate their use of gate arrays—while several others hint that their own use of arrays in the range of 1000 gates are in the near future. Genisco also uses 14 PALs in their design, indicating that graphics is a leader in applying newer semiconductor technology.

THE $9800 DEVELOPMENT STATION.

You need in-circuit emulation *and* editing.

Get both—with the Relms Icebox, for $40,000 less than you'd have to spend for a cumbersome development system.

Besides, who wants to spend $50,000 for something that only works on one manufacturer's chip? The Icebox works on the popular chips you're likely to be using, including the new CMOS chips.

The Icebox, edits, links, locates and loads code. It also emulates, and assembles code—at an impressive rate of up to 2500 LPM.

Take advantage of the compiling power you already have built-in to your company's existing computers. The Icebox can communicate with the Intel INTELLEC, the DEC PDP-11, VAX, RSX-11 and most CP/M systems—including the Osborne.

Used in conjunction with Relms SPICE (Special Purpose In-Circuit Emulator) the Icebox emulates the:

- Z80A,B,L • Z80 (CMOS)
- NSC 800 (2.5 and 4 MHz)
- 80C85
- 8085

Development System	• Compiles • Edits • Assembles • Programs Proms • Uploads/downloads to host machine • Emulates	$30–50,000
Development Station	• Edits • Assembles • Programs Proms • Uploads/downloads to host machine • Emulates	$ 8–11,000
Emulator	• Uploads/downloads to host machine • Emulates	$ 6–9,000

You can buy four Icebox development stations for the price of one development system. So, the Icebox can be used in the lab to develop systems, in production to debug and test, and for field servicing. This allows R&D, production and field service to coordinate activities when they have a common problem.

The Icebox weighs about 25 pounds, and measures less than 9″×11″×17″. It includes 256K of emulation RAM, four serial I/O channels for synchronous and asynchronous communications, with RS-232C and RS-422A connectors. It also supports IEEE-796, IEEE-488 and centronics parallel line printer interface standards. The Icebox is also self-diagnostic and has a prom programmer interface.

Relms is the leading supplier of non-Intel in-circuit emulators. That's how we know what you need to get the job done.

Relms Icebox does the job for a tidy $9800.

Call a Relms representative in your area for more information or a demonstration.

Representatives:
Pacific Northwest: EMA (206)282-6960; Southern California: Marketing Services Company (714)978-0721; Rocky Mountain Area: Trembly Associates (505)266-8616; Midwest (NE,KS,MO,AR): Paloma Sales (816)358-7272; Midwest: Sector Engineering (312)530-7850; Southeast: Teqspec (305)783-3444

Inquiries from European distributors invited.

Relational Memory Systems, Inc.
1650-B Berryessa Road
San Jose, CA 95133
(408) 729-3011
TWX: 910-379-0014

relms

Diagnostics

Diagnostics have become a key issue for graphics processor design. There have been four primary areas of the use of diagnostics/test in graphics processors to date: on-board test initiated on boot or start up; external diagnostics available on a board or system level through the use of logic analyzers, signature analyzers, or small computers; host based diagnostics; and software based diagnostics which are increasingly found as screen displays for the test operation.

Firms note that they must be able to provide customizable diagnostics for one or more of these types of tests to remain competitive. The producers of larger systems have less impetus to work with diagnostics, because typically there is host support and test. The most common area where new test techniques are being developed are among the single board or OEM processor manufacturers. These producers are moving to board level test with an active indicator such as an LED to allow field repair or replacement of a board with minimal down time for a system. The latter is an obvious consideration for companies that may have a significant part of their product used by one OEM.

Summary

The capabilities of today's graphics processors have come to rival that formerly known only in image processing systems because of designers' attempts to provide more performance while decreasing cost. It is evident that graphics systems and their increasing market are impacting semiconductor and display producers. The more important effect, however, may be in creating the demand for engineers, already in very short supply. Many manufacturers working with high speed ECL products for instance bemoan the shortage of engineers that are capable of working to achieve designs that improve on the state of the art.

Another interesting trend is that of the very small producers such as Cubic Systems and Vectrix who are building single board systems based upon 16-bit processors that have some of the functionality of much higher priced systems at a fraction of the cost. Their rapid growth has shown that there is a large market awaiting graphics capabilities who cannot obtain systems at current market cost. Unfortunately, it is inevitable that the developers of the lower cost systems evolve a second generation product that has a much greater cost. Many of the most well known display processor manufacturers continue to maintain very large systems that provide the user with the maximum amount of flexibility in terms of system expansion, while allowing the possibility of later upgrade of the system through software development.

Finally it is interesting to note that some producers such as Genisco have decided not to compete at all levels of performance, but have increased functionality by maintaining compatibility with existing bodies of software. □

The fastest...the largest memories... the easiest to program...

MARS-432 Array Processor Speed
A high-speed programmable arithmetic processor used as a peripheral to a general purpose computer.

MARS-432 Array Processor Memories
Program and data memories compatible with programs written for today's array processor applications.

MARS-432 Array Processor Software
An architecture specifically designed to support a FORTRAN compiler and other software development tools.

The state of the art in 32-bit floating point array processors. Direct addressability of up to 16 million words (64 megabytes) of data memory and direct access to the high-speed internal data bus assure the user of highest throughput rates.

MARS-432 Array Processor Features Include:

- Add and multiply times of 100ns
- Computational power of 30 megaflops
- Computes a 1024-point complex FFT in 1.7ms
- DMA transfers at I/O bus rates of 20 megabytes/sec
- Data memory read or write in 100 ns
- Memory paging for uninterrupted processing during I/O transactions.

Program Memory
Virtual and physical address space of 4K words – standard. Expanded configuration uses a 4K cache memory to extend total memory to 64K words.

Data Memory
Data I/O is supported by DMA transfers into data memory with a physical address space of 16 million words. A data memory page-loading feature provides the option of zero overhead background loading of data during time critical program execution. No DMA cycle stealing overhead is incurred. Uninterrupted processing can occur simultaneously with high-speed I/O transfers.

FORTRAN Development System (FDS)
FORTRAN compiler, linker, and trace/monitor provide high-level language access to the MARS-432.

Microcode Development System
Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

AP Run Time Executive Support Package (AREX)
As the interface to the MARS-432 at run time, AREX provides processor initialization, I/O operations, and array function execution.

Applications Libraries
Extensive applications libraries include math, signal processing, and image processing.

NUMERIX

For additional information on the MARS family of high-speed Array Processors, write or call:
Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500 TELEX 948032

Write 19 on Reader Inquiry Card

Tell us your thoughts

Digital Design is your forum — your inputs help keep the magazine interesting and vital to the design community. So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design,* the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

If you have thoughts your peers should know about, put them in a letter in *Digital Design.* Have your say in *your* magazine! Send letters and comments to: Editor, *Digital Design,* 1050 Commonwealth Ave., Boston, MA 02215.

Display Processor Manufacturers

To obtain more information on the following display processor manufacturers, write in the appropriate Write Number on the *Digital Design* reader inquiry card.

Adage
Billerica, MA
Write 339

Aydin
Fort Washington, PA
Write 340

Comtal
Costa Mesa, CA
Write 345

Cubic Systems
Berkeley, CA
Write 347

Genisco
Costa Mesa, CA
Write 349

GTI
San Diego, CA
Write 354

Jupiter Systems
Berkeley CA
Write 343

Lexidata
Billerica, MA
Write 341

Megatek
San Diego, CA
Write 350

Metheus
Portland, OR
Write 352

Modgraph
Waltham, MA
Write 351

Parallax Systems
Sunnyvale, CA
Write 355

Ramtek
Santa Clara, CA
Write 342

Raster Technologies
Billerica, MA
Write 353

Seiko
Costa Mesa, CA
Write 346

Silicon Graphics
San Jose, CA
Write 348

Vectrix
Greensboro, NC
Write 344

A lineage to be reckoned with.

Aydin introduces their Patriot™ fast scan monitors.

The 8835 (19-inch) and the 8815 (13-inch) Patriot™ fast scan color monitors are the latest additions to Aydin's successful Patriot Series. These monitors are made by Aydin, in the U.S.A.

Patriot fast scan monitors, with a range of 25 to 38KHz, feature electronic linearity correction, low power consumption, and high contrast glass for easy reading.

Ideal for high resolution (1280 x 1024) applications, the monitors are versatile enough to be used in a variety of configurations.

Test it, and see the quality for yourself!

For further information contact Aydin's Marketing Department for the name of your regional sales representative.

Aydin Controls

Command Performance in Color Graphics

414 Commerce Drive, Fort Washington, PA 19034 (215) 542-7800
TWX: 510-661-0518 Telex: 6851057

Write 22 on Reader Inquiry Card

Focusing on users' specific needs, every minicomputer manufacturer is creating a new model/version.

Minicomputers Face Stiff Competition

by Ramakanth Appalaraju

The concept of a computer was limited to large mainframes until the early sixties. Not much miniaturization was involved until Digital Equipment Corporation (Maynard, MA) brought out their first computer, the PDP-1 (Programmed Data Processor). In the mid '60s DEC released their improved version, the PDP-8. Since then, many companies have started to become involved in the manufacture of minicomputers.

Today, the definition of a minicomputer is quite blurred, with minicomputer offshoots, superminis (32-bit) and micros. The classification is essentially based on data path width, capacity of main memory and cost. The minicomputers considered here satisfy the following conditions:

- 16-bit data path
- A main memory capacity of less than 4 Mbytes
- Support at least 10 terminals and
- Cost less than $40,000 (in a minimum stand alone configuration).

The advent of the PDP-11 Series was a real breakthrough. Even today, the minicomputer market is dominated by different versions of PDP 11s. Behind DEC in revenues from minicomputers come Data General, Honeywell, Hewlett-Packard, Texas Instruments, IBM, Prime, Wang, etc. A survey by Industrial Data Corporation shows the percentage of market dominance by each of these manufacturers (**Table 1**).

Presently, an estimated seventy-five companies are involved in the making and marketing of minicomputers. Focusing on users' specific needs, every manufacturer is involved in creating a new model/version. Modification usually results in increased performance while maintaining hardware and software compatibility with earlier models. The advent of semiconductor memory and LSI circuitry has added to the minicomputer boom by allowing faster manipulation, greater accuracy, wider capabilities, smaller size and reduced cost.

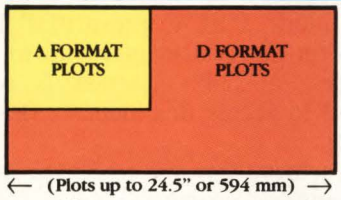
Manufacturer	% of Market
DEC	33.3
Data General	15.5
Hewlett-Packard	11.5
Computer Automation	6.2
IBM	5.6
Texas Instruments	5.3
Honeywell	2.9
Prime	0.9
Others	18.8

Table 1: Percentage of market dominance by minicomputer manufacturer.

Ram Appalaraju is a graduate student at Tufts University Department of Electrical Engineering, with a concentration in Computer Engineering. He is a student member of IEEE and can be contacted through **Digital Design**, *1050 Commonwealth Avenue, Boston, MA 02215.*

At last. A plotter designed to run both cut sheet and roll media.

The most flexible "D" format 8-pen plotter ever.

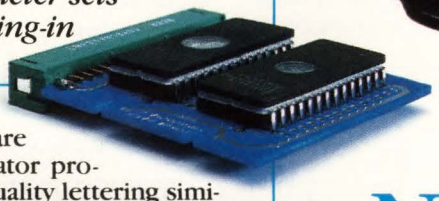


Now you can create virtually any size plots you want up to 24.5" wide, including ANSI sizes A-D and ISO sizes A4-A1, on cut sheet or roll media. Use standard bond paper, glossy bond, vellum, clear film or mylar.

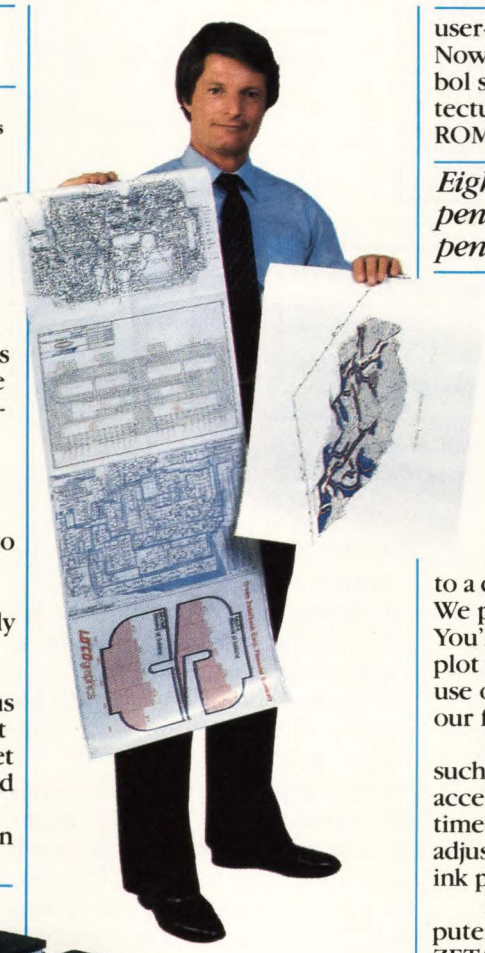
Run dozens of entirely different plots automatically thanks to a built-in microcomputer that can be pre-programmed to plot on roll media up to 170 feet. Then quickly switch to cut sheet plotting – great for your pre-printed forms. The ZETA 822 is the only plotter that can do both.

Best of all, we've got line quality and throughput at a price that makes us the cost-effective choice for just about anybody's plotter applications. You'll get vector independent speed of 25 ips. And 2 g acceleration insures the plotter reaches top speed fast. With resolution of one-one thousandth's of an inch.

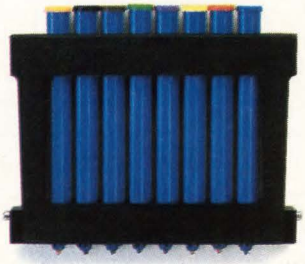
Change character sets just by plugging-in a ROM chip.



Our firmware character generator produces typeset quality lettering similar to the popular Helvetica font with user-controlled proportional spacing. Now you can add special character symbol sets for both engineering and architecture simply by plugging in a new ROM chip.



Eight color, carriage-mounted pens eliminate time-consuming pen changes.



Incredibly, some plotters still grind to a dead stop to change pens. Not ours. We put all eight pens on the carriage. You'll be amazed at what that does for plot throughput. And when you want to use our liquid ink option, just snap in our four-pen cartridge.

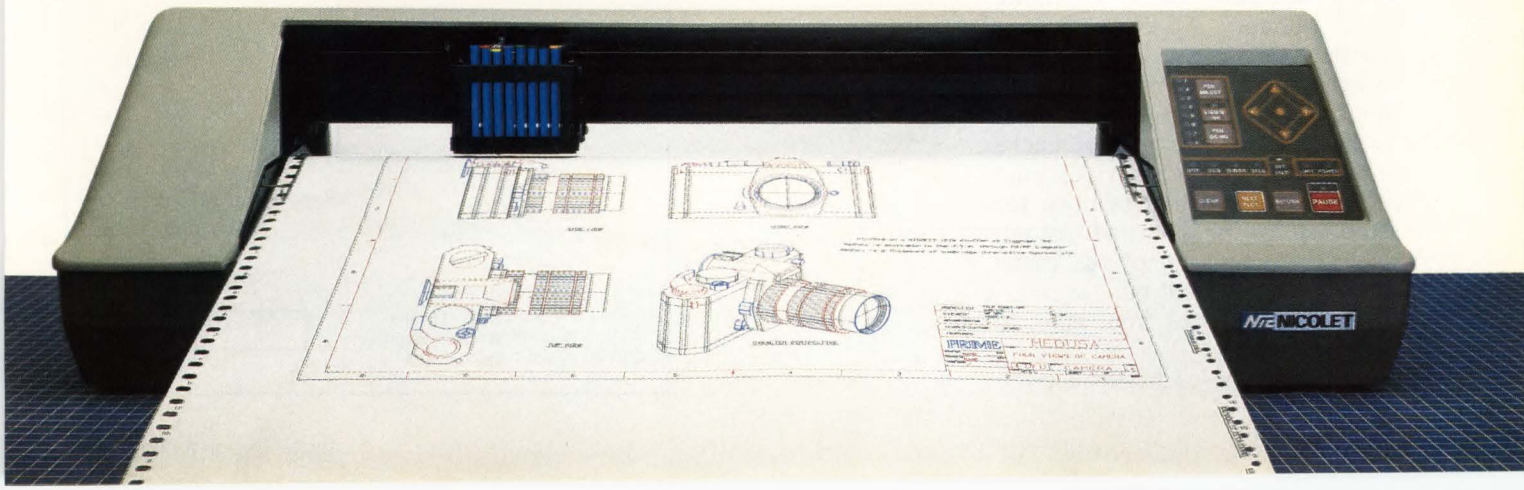
You have total user control over such variables as speed, pen pressure, acceleration and pen up/down delay times. Touch controls automatically adjust the ZETA 822 for perfect liquid ink plots.

Naturally, we support most computer protocols. And you can use the ZETA 822 on-line, off-line or remotely via RS 232C or IEEE 488 interfaces.

Call (415) 671-0600. Or write: Nicolet Zeta Corporation, 2300 Stanwell Drive, Concord, CA 94520 TWX 910-481-5951

Nicolet

Write 16 on Reader Inquiry Card



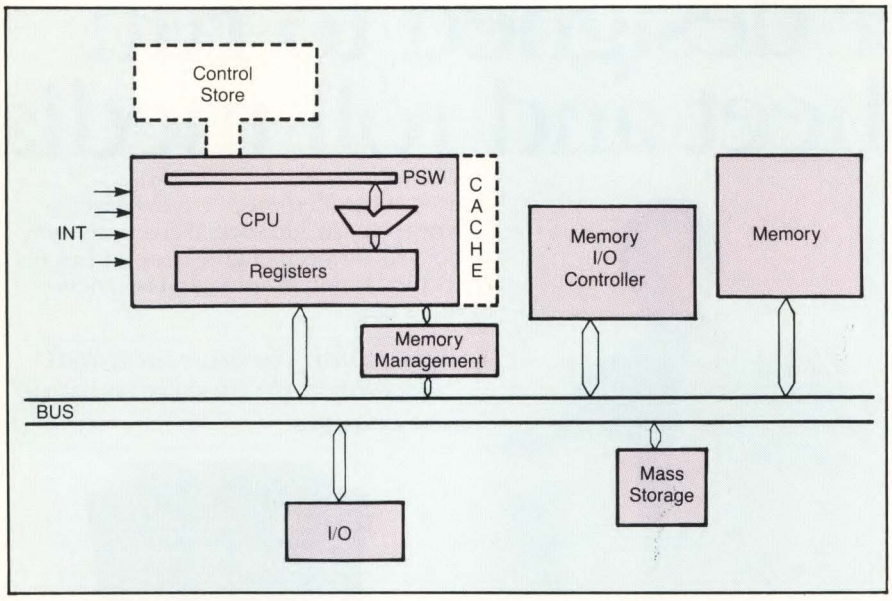


Figure 1: Generalized architecture of a minicomputer.

Minicomputer Structure

A generalized minicomputer architecture consists of a CPU, memory, I/O controllers, I/O devices, and a bidirectional communications path through which all these system components are allowed to interact. (**Figure 1**). The CPU consists of an arithmetic logic unit, general purpose registers, and a processor status register. The general purpose registers are classified as accumulators, program counters, index registers and user registers. The number of registers in the CPU is a function of factors such as word size, execution speed (MIPS), instruction set and ability to handle interrupts.

The time needed to perform an operation consists of access time, execution time and write time. In early minicomputers, the CPU took considerable time to access data from the memory. Now this delay is overcome by incorporating Direct Memory Access technique and cache memory.

Cache memory is a high speed (bipolar) memory, usually of about 4 Kbytes. The contents of cache memory is a copy of previously selected blocks of main memory, for faster *reaccess* of data and instructions. The operation of the cache memory is dependent on:

- Transfer of data from main to cache
- Space in the cache for a given word in main memory to be written.
- Management of handling primitive data/instructions in main as well cache memory.
- The method of selecting the location to write to in cache from main memory.

Some minicomptuers have control memory and/or Cache memory; the user may or may not have access to control memory. The control memory usually has the system programs and is directly connected to the CPU.

Another innovation currently incorporated in minicomputers is memory management. Without memory management, the CPU of a 16-bit machine can only access 64 Kbytes of memory. But by translating a virtual address into a physical address, memory management allows accessible memory to be expanded. DEC's micro/PDP-11 supports physical memory up to 4 Mbytes; a 22-bit address is required to access this memory (**Figure 2**).

To achieve this, the 64 Kbyte virtual address space is divided into eight pages of 8 Kbytes each, and each page is relocated separately into the physical address space. The upper three bits of 16-bit (virtual) address identify the page to which the address belongs. These three bits can select among eight 16-bit page registers. The upper 8 bits of page register supply the beginning address of the page in the physical memory space and the lower 8 bits of the page register supply access control, length and expansion information.

The bus to which all the devices are connected is responsible for reduced access time and miniaturization. Bus width is equal to the number of bits required for addressing. Most minis use one bus to connect all devices. However, systems such as Data General's Eclipse S/280 use multiple busses.

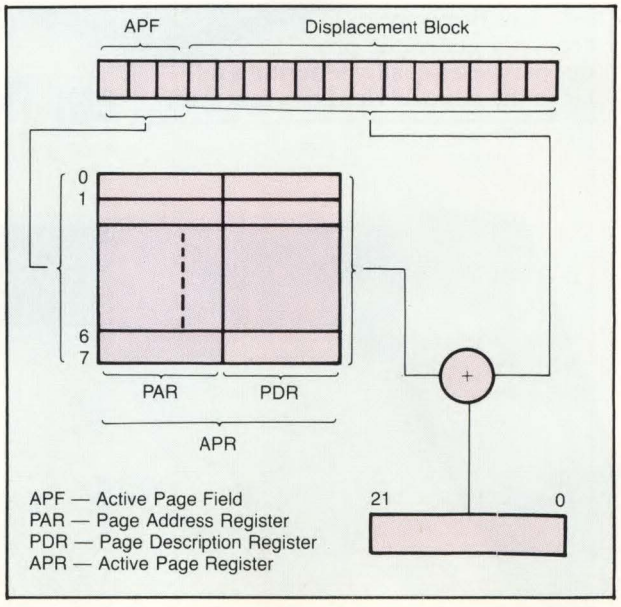
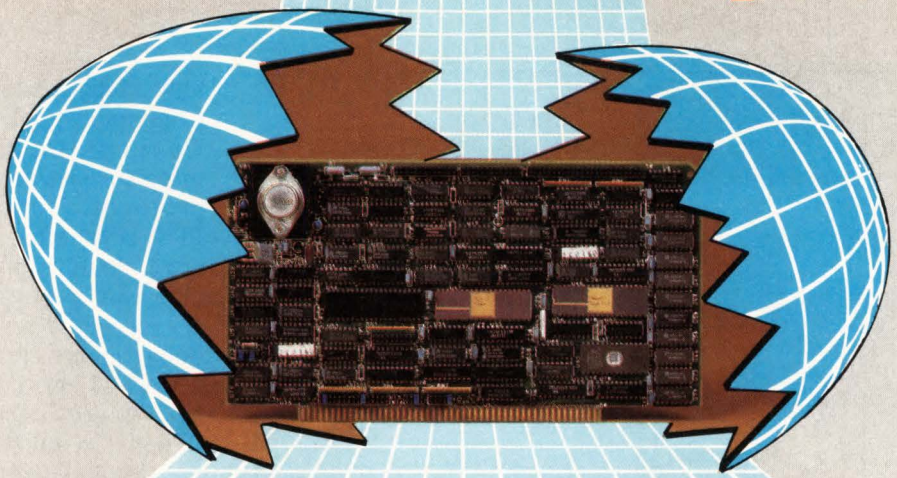


Figure 2: To access 4M bytes, a 22-bit address is required in DEC's Micro PDP–11.

Incubation Complete



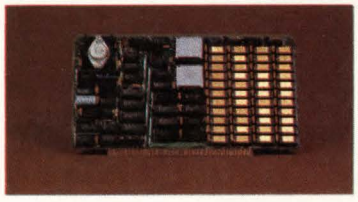
A Third Generation is Born

SBC 300

(Pictured above)

A Z80 based microcomputer board with memory and I/O functions

- ***Fully complies with IEEE 696 Standard***
- 4/6 MHz Z80 A/B
- Supports CP/M® Plus
- Operates as bus master/slave for multi-user, multi-processor architecture.
- 64K on board memory, dual ported, parity checked
- 2 serial ports, 1 SASI port
- All I/O drivers on board
- Memory management
- Full 24 bit address capability
- 3-16 bit CTC's



ExpandoRAM IV—Random access memory board utilizing 64K or 256K NMOS RAM chips

- ***Fully complies with IEEE 696 Standard***
- 256K capacity with 64K chips
- 1024K capacity with 256K chips
- Error checking and correction (2 bit detection, 1 bit correction)
- On board refresh
- Supports both 8 and 16 bit data transfers
- 24 bit addressing

SD300—A new series of compact yet expandable S-100 microcomputers.

- Compact size approximately 4" × 14" × 17"
- 6 Slot motherboard
- Rugged metal enclosure

OEM Version: **Designed for ease of integration and maximum flexibility**

- Z80 CPU
- 256K RAM
- Versafloppy II with free CP/M Plus™

Discless Version: **An ideal high performance system for disk intensive applications. Eliminates disk wait states for spread sheets, spelling checkers, and network operation. Utilizes SDSystems RAMDisc and ROMDisc modules.**

VFW-3: A single board controller for floppy and Winchester disk drives:

• ***Fully complies with IEEE 696 Standard*** • Up to 4 floppies and three Winchester drives may be controlled by VFW-3 • Data transfers to and from board under DMA or programmed I/O control • Supports 24 bit address space.

CP/M Plus™ high performance single user operating system.

• CP/M® 2.2. compatible—no modification! • When used with SDSystems 256K memory board speeds are up to 7 times faster than CP/M® 2.2. • High performance file system • MP/M® II file password protection • Time and date stamps on files • Support for 1 to 16 banks of RAM • Easy to use system utilities with HELP facility • Powerful batch facility • Sophisticated programmer utilities.

RAMDisc 256: A solid state disk emulator that greatly increases system performance by eliminating disk waits in disk intensive applications. Excellent for spreadsheets, spelling checkers and software development.

• 256K capacity • 1 mb total bus capacity • CP/M® 2.2, PLUS™ compatible • I/O port addresses user selectable • Storage locations addressed by on board 20 bit counter • On board refresh.

ROMDisc 128: An EPROM board that replaces a floppy disk drive for the purposes of booting CP/M® and loading application programs.

• Provides non volatile, permanent storage of programs and data • Utilizes 2732 or 2764 EPROMS, (16 max) • 128K capacity per board • 512K system capacity • Use with SDSystems RAMDisc to configure a stand alone or network discless system • Serial port provided.

SDSYSTEMS
A Syntech Company
10111 Miller Road • Dallas, Texas • (214) 340-0303 • TLX-682 9016

Write 23 on Reader Inquiry Card

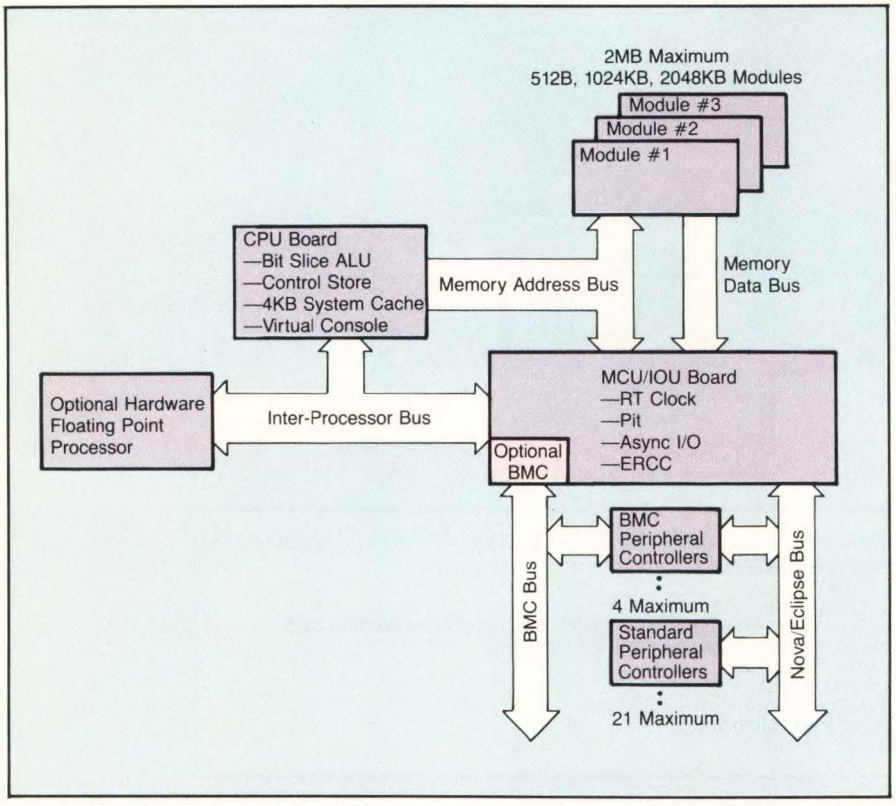


Figure 3: The Eclipse S/280 from Data General incorporates a multiple bus configuration.

Updated PDPs

Minicomputers from Digital Equipment Corporation may be classified into two groups based on bus structure. Among the latest versions, the PDP-11/24 and PDP-11/44 use the Unibus structure and the micro/PDP-11 uses the LSI-11 Q-bus structure.

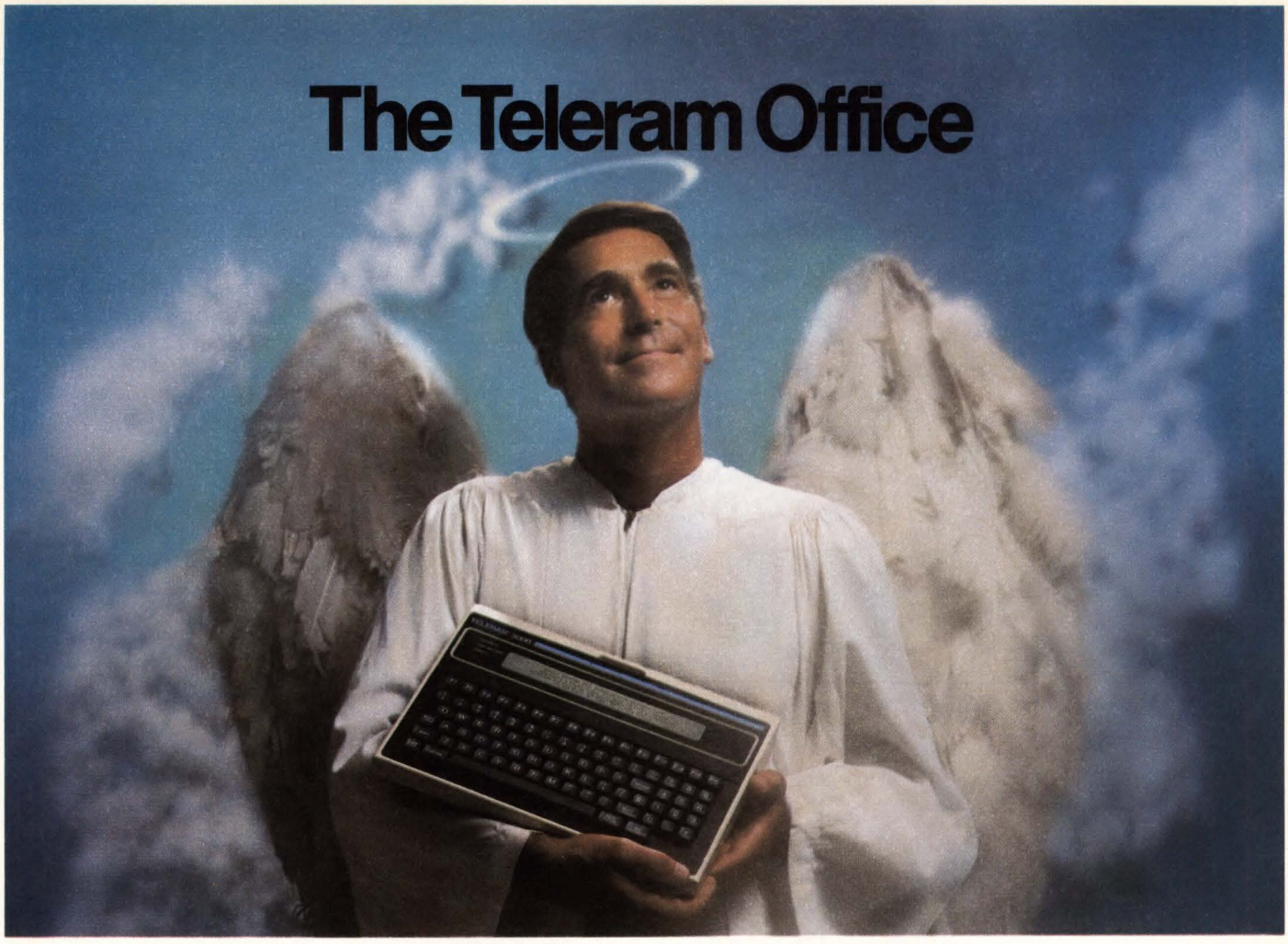
Unibus is a single high-speed asynchronous bidirectional communications path to which all the system components are connected. Communications take place on the Unibus in the master-slave mode using an asynchronous handshaking protocol. Both PDP-11/24 and PDP-11/44 offer an optional hardware floating point processor for improved performance. The 11/44 is best suited for larger, multi-user departmental-level applications. The 11/44 also includes an 8 Kbyte high speed cache memory. The PDP-11/24, on the other hand, has the capabilities of earlier, larger PDP-11s and is suited for low-cost applications.

The micro/PDP-11 is a table top multi-user minicomputer. The systems uses the LSI-11 Q-bus structure. The LSI-11 bus, like Unibus, is an asynchronous bus. Interactions between devices on the bus are limited only by the speed of the devices, not by a clock as in synchronous busses. The Q-bus has 44 lines, of which 22 are address lines corresponding to 22 bits of physical address space. Since the data path is only 16 bits wide, 16 of the lines in the bus are time-shared for data transfer. The system offers a hardware floating point processor board that enables faster execution of FORTRAN and BASIC programs.

PDP-11s have six 16-bit general purpose registers, a stack pointer and a program counter. In addition, the processor has a 16-bit processor-status word register. Apart from these registers, the later models of PDP-11s are equipped with floating point instructions, and have six 64-bit floating point accumulators. These are used to contain operands for floating point arithmetic and to exchange data with general registers. The processor is also equipped with a floating point status word register which describes the current status of floating point operations. Thus, all the latest models of PDP-11s are equipped with 16 registers.

The Unibus family of PDP-11s provide compatibility with peripherals such as Winchester disk (up to 456 Mbyte), removable disk (up to 205 Mbyte), cartridge disk (up to 10 Mbyte), floppy disk (0-5 Mbyte) and magnetic and cartridge tapes. Peripherals for the Micro/

Figure 4: Honeywell's DPS 6/31 tries to balance commercial and scientific capabilities.



You can take it with you.

Because the all-new Teleram 3000 is the first truly portable personal computer that operates everywhere, a Teleram Office is anywhere. Wherever business wants or needs to be.

Taking it with you.
Weighing less than 9 lbs. and hardly bigger than a 3" notebook, the Teleram 3000 is easy to take... in a standard briefcase. For operation anywhere on internal rechargeable batteries. For capabilities as powerful as desk top computers.

While others are stuck at their desks, take your Teleram Office home. Work on the way. In cars, planes, anywhere.

Leaving it behind.
Look at the spec's for the Teleram Office Station. For interface with networks and peripherals. Plus, cost-effective office pooling potential.

pat. pend.

In your office or out, the Teleram 3000. With non-volatile bubble memory up to 256kbytes. A standard-size keyboard. Flat panel display of 80 character lines. Standard CP/M* applications without modifications. More desirable features than hand-held and suitcase models put together. More versatility than any desk top.

The Teleram Office. The heavenly place and way to do business.

Specifications:

The Teleram 3000: 8 lbs.-13 oz. 13" x 9¾" x 3½"
Powered by 5-10 hr. internal battery, auto cigarette lighter or 110/220 VAC
Typewriter keyboard plus numeric/cursor keypad & 16 soft function keys
64k RAM/4K ROM
128k or 256kbyte non-volatile bubble memory
4-line x 80-character Liquid Crystal Display (LCD)
RS232C Interface (communications or printing)
CP/M 2.2® operating system

Expansion capabilities
Teleram Office Station which contains:
floppy disks and/or Winchester disk drive, text/graphics CRT display, additional bubble memory, networking and additional communication interfaces

TELERAM

Teleram Communications Corporation
2 Corporate Park Drive White Plains, N.Y. 10604
(914) 694-9270 TELEX 646658

*CP/M is a trademark of Digital Research.

Write 40 on Reader Inquiry Card

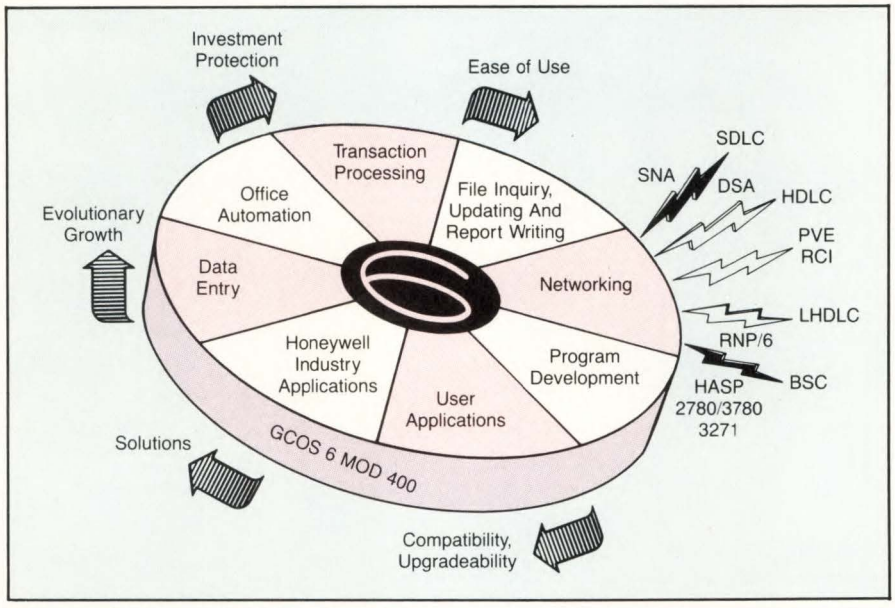


Figure 5: Honeywell's GCOS 6 MOD 40 operating system.

PDP-11 include cartridge disk, floppy disk and mini diskette subsystems.

Software for single user systems as well as multi-user systems is offered by DEC. The operating systems support all PDP-11s. The software offered is classified into five catagories: Operating System Software, Programming Languages, Data Management Packages, Word Processing, Graphics Packages and Applications Development Packages.

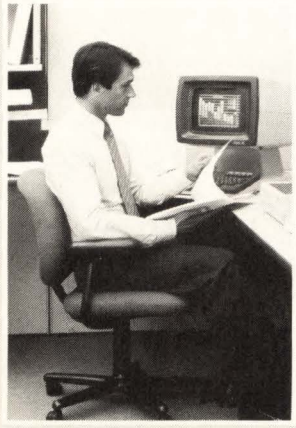
Nova, CS, Eclipse

Data General, who entered the mini-computer market with the NOVA series, are today second in the 16-bit machine competition. In the late '70s DG brought out the CS series models and Eclipse series models. The latest among these models are CS Series 200, Eclipse S/120 and Eclipse S/280. The Eclipse S/280 incorporates the CPU and system cache on a single board. The CPU consists of cascaded 4-bit microprocessor slices. The fast cycle time of the system (=150ns) is attributed to third generation bipolar technology.

The Eclipse S/280 incorporates a multiple bus configuration, with an interprocessor bus, memory address buts, and memory data bus. The 16-bit interprocessor bus is used for bidirectional communication between the CPU, control unit (memory and I/O) and the hardware floating point processor. (**Figure 3**).

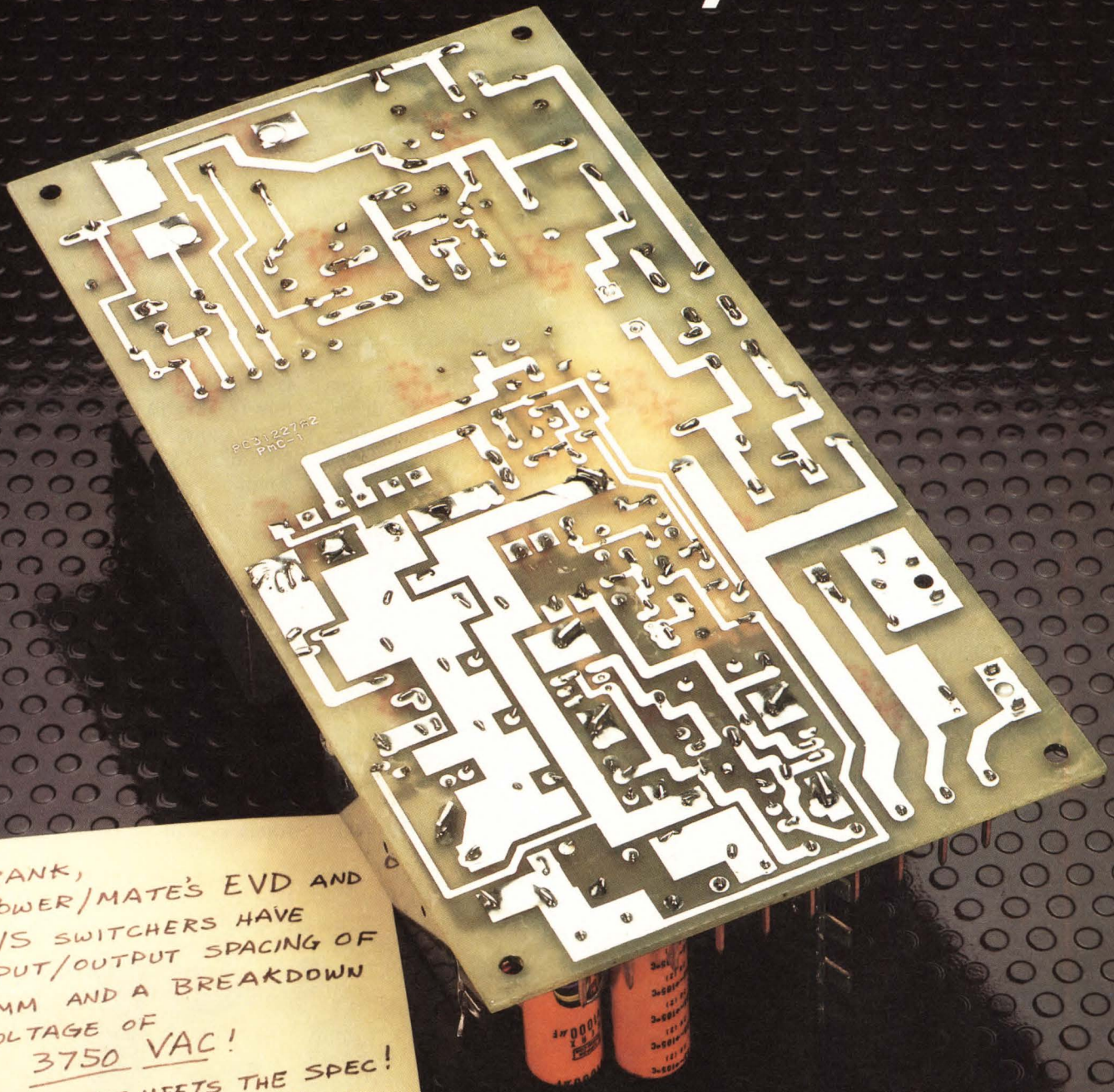
Apart from the main memory, the S/280 is provided with system cache memory (4 Kbytes) and a control store (4 Kbytes). The main memory is expandable up to 2 Mbytes by Eclipse MAP memory management. The CPU consists of eight accumulators, four of which are 16-bit general purpose registers and the four others are 64-bit floating point accumulators.

Mini Hardware Parameters Compared



	PDP 11/44	Micro/ PDP11	DG S/280	DG S/120	Honeywell 6/31	IBM 36	HP 100 A900	Wang 2200 LVPC
Main Memory	256K	256K	512K	128K	128K	512K	768K	64K
Memory Type	ECC MOS	MOS	MOS	MOS	MOS	MOS	MOS	MOS
Expanded Memory Capacity	4M	2M	2M	512K	1M	16M	6M	512K
Cache Memory	8K	—	4k	—	—	—	4K	—
Cycle Time (ns)	480	≈1100	450	500	550	200	188	600
Error Correction	Standard	Standard	Standard	Standard	Standard	Standard	Standard	Standard
Multiprocessing	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MBPS I/O Transfer Rate	2.0		13.3	2.0	6.6	2.5	3.7	0.5
No. of Workstations Supported	up to 127	64	64	64	16	30	64	13
Extended Precision	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Parity Checking	No		Standard	No	Standard	Standard	No	Standard

Even this side will convince you.



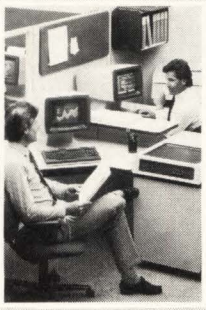
RTEPOWER/MATE

THE PACESETTER IN SWITCHING POWER SUPPLIES

POWER/MATE CO. 514 South River Street, Hackensack, NJ 07601-6697 • (201) 440-3100 TWX: 710-990-5023
10951 Coventry Place, Santa Ana, CA 92705-2315 • (213) 793-4070 TWX: 910-588-3285

Write 26 on Reader Inquiry Card

Software Support For Minis



Software Support	DEC	DG	HP	Honeywell	Wang
Assembler	Assembler, Macro Assembler	Assembler, Macro Assembler	Assembler	Assembler	Assembler, Macro Assembler
Compilers	Basic Fortran Cobol Cobol	Basic Fortran Algol Pascal	Fortran Pascal Basic	Cobol Fortran RPG Basic Pascal	Cobol Basic, RPG Fortran, PL/1
Operating System	Batch Real Time Multiuser	Real Time Multitasking	Real Time DBMS	On Line Multiuser	Interactive Multiuser
Languages Implemented Firmware	No	No	Partially	Partially	No
Operating System Implemented In Firmware	No	No	Partially	No	Partially

The Burst Multiplexor Channel (BMC) for the Eclipse S/280 minicomputer provides a wideband input/output path, independent of the standard data channel. With the BMC, data can be transferred directly at high speed in "bursts" in and out of memory, from very high speed/high capacity peripherals. The Eclipse S/280 accommodates a full range of magnetic mass storage devices. Up to 2.2 Gbytes of online storage can be configured on a BMC-equipped system. The peripheral support includes diskette, Winchester disk, fixed head disk, cartridge tape, cartridge disk and compatible magnetic tape.

The Eclipse S/280 is supported by an array of system software that includes operating systems, high-level languages, utilities, debugging aids, development tools, and communications packages.

Variety in DPS 6

Since the beginning of the eighties, Honeywell has created an impact in minicomputer markets with a wide variety of DPS 6 models. The latest in the series is DPS 6/31 (**Figure 4**), aimed at OEM and end user markets. The DPS 6 models, according to Honeywell, strike a balance in performance between commercial applications and scientific functions. All DPS 6 models use high density 64K chip technology and an asynchronous, bidirectional bus known as Megabus. Memory management in the system allows 24-bit addressing. The CPU uses 22 register. Peripheral support for the system includes floppy disk drive (up to 650K), diskette storage (up to 13 Mbytes), cartridge disk drive (up to 13 Mbytes) and a minimum disk storage of 26 Mbytes.

The DPS 6/31 runs on the company's GCOS 6 MOD 200 or MOD 400 operating systems and can be used as a satellite processor in both Honeywell and IBM distributed networks for data entry, office automation and user-developed applications. The system can accommodate up to 16 communciation ports to support video work stations, serial printers or communications lines to other computers.

Honeywell's GCOS 6 MOD 400 is a multifunctional operating system (**Figure 5**). The multifunctionality allows users of Honeywell's 16- and 32-bit minicomputers to combine several modes of local processing capabilities with communications under a single operating system. The distributed processing capabilities of this operating system include: data base management, networking, office automation, program development, transaction processing, industry applications, data entry and query and reports.

Giant's Minis

IBM, who has dominated the main frame systems market since incep-

Figure 6: In IBM's 5/36, separate microprocessors control each function.

Draw Your Own Conclusions*

*$995

RESOLUTION
800 × 480 High Speed Quality Graphics.

TEKTRONIX 4014 EMULATION
Most all the Tektronix features are supported including: 4010 and 4014 Emulation, Plot 10 Compatible, 4096 by 4096 Addressable Plot Area, Variable Line Types, Point Plot, Vector Plot, Incremental Plot, Write Thru Mode and built-in crosshair cursor.

SPECIAL FEATURES
Selanar Native Mode Command Structure, Area Fill, Circle, Arc and Box Commands.
Also variable scale factor for changing image size, relocatable origin, special write modes, switchable video.

SINGLE BOARD DESIGN
The SG480 is a small single board design (4.5 by 5 inches) and simply plugs into the VT100 STP port. Only one small cable is required. The SG480 comes with a replacement CRT tube and attached yoke —simple installation without critical adjustments.

DEC TERMINALS SUPPORTED
VT100, VT132. In addition Selanar has comparable products for the VT101 and VT102 plus other products for the VT100, VT103, VT105, and VT180.

HARDCOPY
Hardcopy is standard for the DEC LA34 format. Options currently available are for C.Itoh, Epson, Data South, Texas Instruments, and Selanar's SG120 PLUS with DEC's LA120.

OTHER SELANAR GRAPHICS™ PRODUCTS
Televideo 925, 950, 970. Lear Siegler ADM3A, 3A+, 5. Qume QVT Series Terminals (Exclusive). DEC LA120.

SELANAR GRAPHICS SG480

Sales and Marketing: 4212 N. Freeway Boulevard, Sacramento, CA 95834 (916) 921-9700

Write 25 on Reader Inquiry Card

Corporate Headquarters: 437-A Aldo Avenue, Santa Clara, CA 95050
European Headquarters: Selanar GmbH, Ahastrasse 5, 6100 Darmstadt, West Germany

tion, is relatively new to the minicomputer industry. Today they rank fifth in the competition. The models that have been on the market since the beginning of the eighties are Series 1 and System 38.

IBM expects a lot from their latest release, the System 36 (**Figure 6**), which combines data processing, word processing, color graphics and office management functions. The system architecture is based on multiprocessor design in which each microprocessor controls a separate system or function. The System 36 has provisions to support 30 terminals and 60 remote terminals.

The IBM personal computer can be used with the System 36 as a local or remote workstation. The best applications of System 36 are in business environments, hence software support is more oriented toward those applications. (Packages provided are for manufacturing, accounting, management and development applications.)

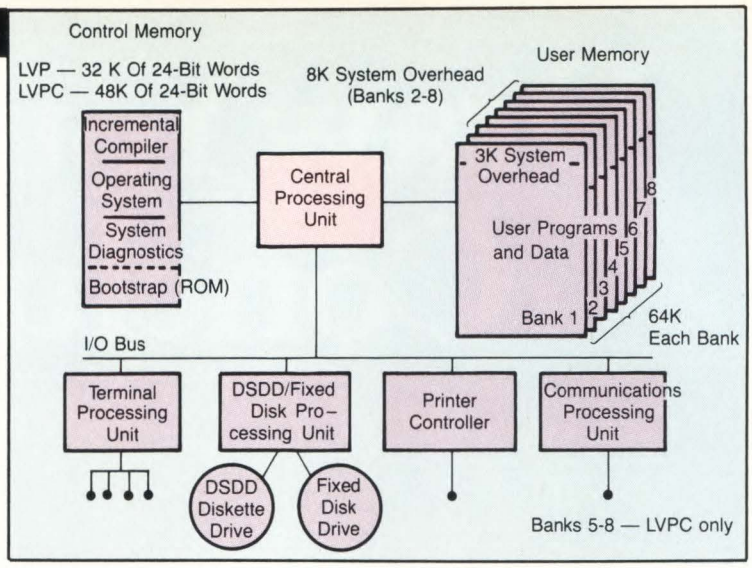


Figure 7: The 2200 series from Wang Labs.

2200s Use One Bus

The 2200 series of Wang Laboratories Inc. is aimed at office automation. The three models in this series, the 2200 SVP, 2200 MVP and 2200 LVP have similar architecture (**Figure 7**), based on a single bus. The control memory, which stores the system software, is connected not to the bus, but directly to the CPU for faster access. Multi-programming capabilities are provided by fixed-position memory.

The 2200 models can support up to 13 terminals and up to 16 jobs concurrently in a multi-programming environment. The 2200 LVP is the latest model in the series. An alternate version, the 2200 LVPC, incorporates all LVP features plus a larger control memory.

The peripherals for the 2200 LVP include two disk drive units: the dual-sided, double-density, diskette

Triad made line voltage regulators cooler and lighter.

Triad's Power Right™ voltage regulators and Power Master™ uninterruptible power supplies operate up to 20°C cooler than competitive models...and they weigh up to 15 percent less!

Perfect for small or large computers, point-of-sale terminals, word processors or virtually any microprocessor-based industrial control, Power Right voltage regulators protect equipment and operation with accurate voltage control. Available in portable and hard wire models, the Power Right has output VA ratings from 300 to 30,000.

The Power Master uninterruptible power supply ensures continuous power supply...with up to an hour of valuable battery back-up time to prevent loss of entries or memory.

For unsurpassed quality, competitive price and fast delivery, contact your nearest Triad-Utrad distributor or write: Triad-Utrad Standard Products, 1124 E. Franklin St., Huntington, IN 46750, 219-356-6500, TWX 810-333-1532.

Triad Winds Up The Best.

Litton

TRIAD-UTRAD
Standard Products

Write 28 on Reader Inquiry Card

Name of the Register	Number of Register	Width of the Register in bits
Standard	5	16
Instruction	1	16
Switch	1	8
Status Flag	2	1
LED	1	8
Process Control	4	16
Process Status	4	16
	3	8
Subroutine level	16	15
Stack	3	16
Memory Address	3	8
Micro Address Vector	1	15
	1	8

Table 2: HP 100 A900 registers are from 1 to 16 bits wide.

drive and the Winchester style fixed disk drive. The dual-sided double density diskette drive offers storage up to a Mbyte. Optional fixed disk drive is available to 32 Mbytes.

I/O, RTE Focus

Hewlett-Packard minicomputers constitute 11.5% of the minicomputer market. The HP 1000 series feature distributed intelligence for input/output. The design uses an I/O processor on each interface to maximize I/O efficiency. The E and F Series minicomputers of the HP 1000 Series have been on the market since the mid-seventies. The latest HP 1000s are the A series and the most recent version of it is A900. The A900 is Hewlett-Packard's fastest HP 1000, due to pipeline technology with cache memory and a hardware fast floating point chip. Execution speeds to 3 million instructions per sec and 500 thousand floating point operations per sec are achieved by A900.

The A900 minicomputer uses a hardwired MSI processor. The CPU uses various registers for various purposes (**Table 2**). In addition, the central processing register has the following scratch registers:

12 × 16 bits non-pipelined
12 × 16 bits pipelined
896 × 16 bits cache memory locations addressable as scratch registers.

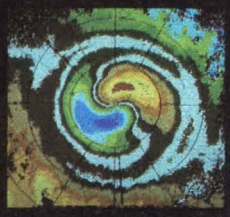
The A900 CPU has multiple bus structure. Two separable storage busses allow splitting of data paths. Main memory and I/O transactions are conducted on separate busses and are arbitrated by the cache. The A900 has a user-accessible control store of 2 Kbytes. The control store is bipolar LSI semiconductor type. The control store is microprogrammable by the user. The cache memory gives the A900 a fast 133 nsec cycle time for each successful cache memory access. The cache incorporates hardware address-created logic for next address generation (pipelining) and supports a 32-bit data bus to the

Only your imagination can limit the application of Comtal's new Vision Ten/24 Image Processing System.

Whether you're exploring the outer regions of space or exploring for oil in some remote area of the world, Comtal's new Vision Ten/24 is the only digital image processing system that processes and displays 1024 x 1024 high resolution images with a clarity never experienced before in image processing. It's a powerful tool for interpreting and analyzing images for such diverse applications as LANDSAT, meteorology, seismology, graphic arts, earth resource management, medical imagery, or something only you know about.

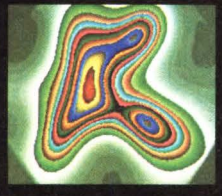
Four times the resolution at 30% lower cost.

The Vision Ten/24 is the only image processing system capable of processing and displaying images at a 1024 x 1024 resolution in real time (1/30 second) with a 40 MHz video output rate. That's four times the resolution of the industry-standard 512 x 512 systems. With it, whole new worlds open up. Interpretation and analysis become more precise. Best of all, the basic Vision Ten/24 system price is 30 percent less than our previous 1024 x 1024 system because of our design and manufacturing refinements. Giving you incomparable price/performance.



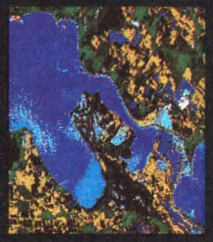
Building block flexibility.

Our modular design approach with the architecture of the Vision Ten/24 gives you flexibility along with easier system upgrades. You can increase video paths, memory size or processing power by simply adding modules. Making the Vision Ten/24 able to keep pace with your image processing requirements. In addition, the system can operate as a standalone image processor or can be interfaced to a variety of host computers.



Comtal—a generation ahead in image processing.

Our new Vision Ten/24 is a generation ahead of any other digital image processing system. It's not surprising since our systems have consistently been the state-of-the-art in image processing. For example, our 512 x 512 systems offer more exclusive features and options, and give you more standard models to choose from, than anyone else. With a decade of experience in image processing and more than 600 systems installed worldwide, only Comtal gives you the leading edge of image processing technology.



Put your imagination to work and give Comtal a call today for a firsthand look at our new Vision Ten/24. Comtal, a subsidiary of 3M, 505 West Woodbury Road, Altadena, California 91001, (213) 797-1175

COMTAL 3M

Write 21 on Reader Inquiry Card

memory controller.

The different operating systems from Hewlett-Packard are unified in a family of real time executive (RTE) software. The operating packages in RTE are: programming languages, database management, graphics, system executive routines, real time scheduling and multitasking. These systems support real time interactions and control in factory automation, data acquisition and scientific problem solving applications. The Graphics/1000–II software supports the HP 1000 family of minicomputers with a high resolution interactive and three dimensional graphics routines. For display as well as plotting devices.

Minis In The Market

The minicomputer boom has given way to microcomputers and 32-bit superminicomputers. In 1981, the percentage of dollars from superminis and micros was 25% as against 75% from 16-bit minicomputers.

Superminicomputers arose from architectural innovations such as internal 32-bit architecture, 32-bit registers, fast floating point units and expanded I/O capabilities. With maximum memory capacity of 12 Mbytes, superminis are suited to multi-user applications.

With the prices of superminis crashing fast, superminis may be expected to completely overtake minicomputers within the decade. However, the medium-range computer market on the whole is expected to triple by 1986. □

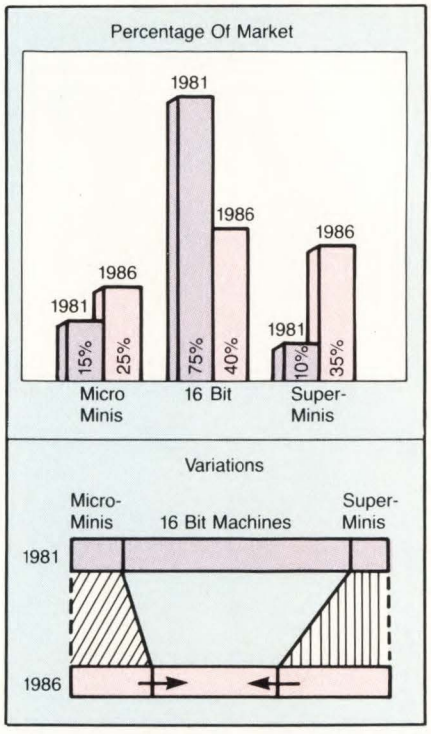


Figure 8: Market share for micros and superminis is squeezing the 16-bit mini market.

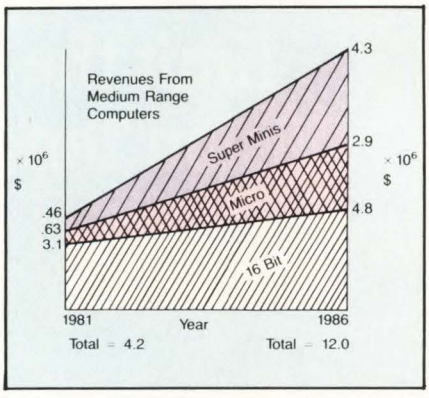


Figure 9: Projected revenues from medium-range computers.

Minicomputer Manufacturers

To obtain more information on the manufacturers mentioned in the preceding article, please enter the appropriate write number on the *Digital Design* Reader Inquiry Card.

Data General
Westboro, MA
Write 356

Digital Equipment Corp.
Maynard, MA
Write 357

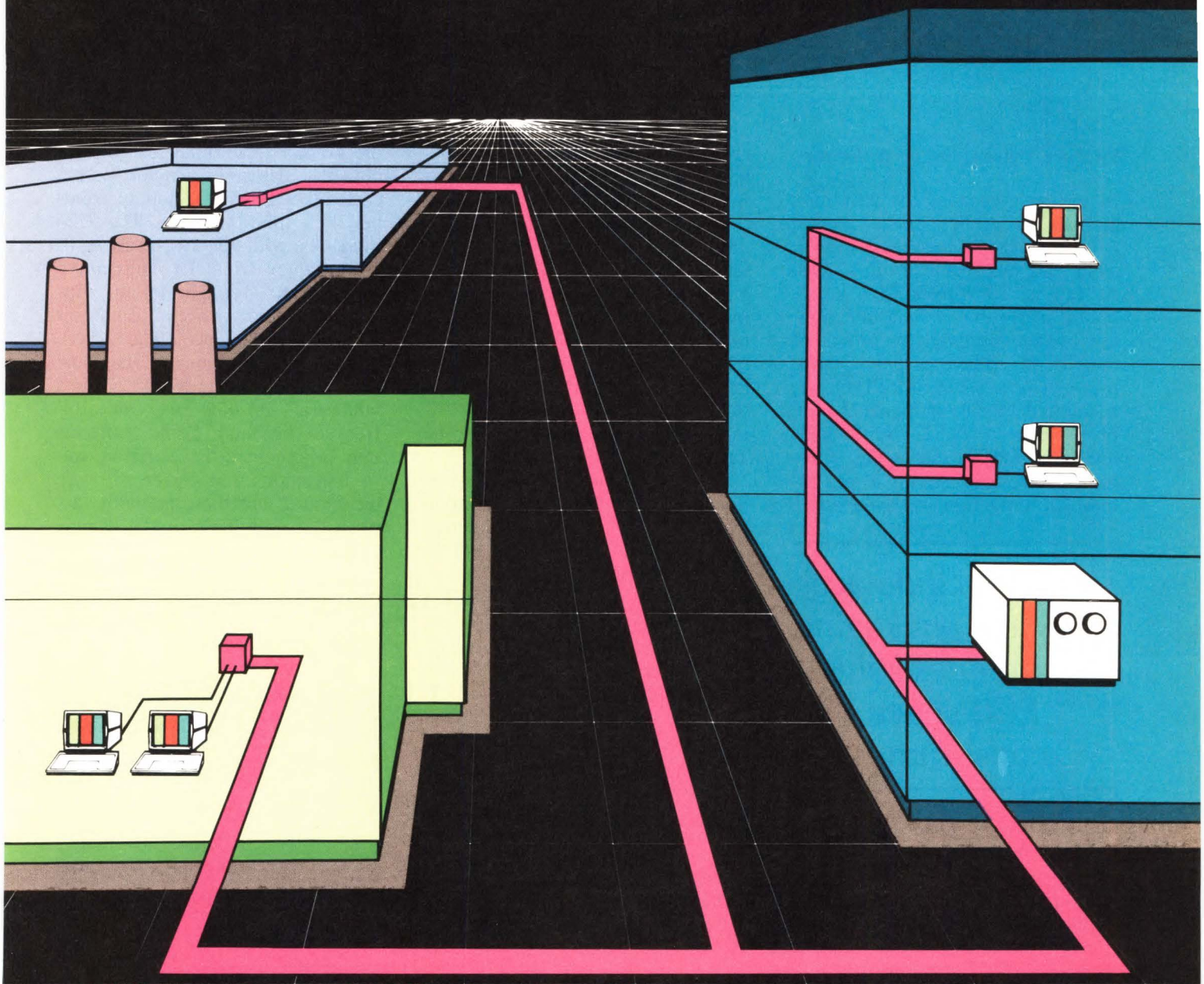
Hewlett Packard
Computer Products Group
Lexington, MA
Write 358

Honeywell Information Systems
Waltham, MA
Write 359

IBM Corp.
Port Chester, NY
Write 360

Wang Laboratories
Lowell, MA
Write 361

Remote Your Graphics Workstations...



With Artel Fiber Optics

Artel's fiber optic systems are the **only** way to remote your high resolution computer graphics workstations where you really want them, up to two miles away. Compare this to the 100 feet or so you get with coaxial cables.

Artel systems give you reliable, noise-free video and data transmission, freedom from ground faults, communications security, intrinsic safety, lightning immunity and a dramatic reduction in cable congestion.

You don't have to be a fiber optics expert to use Artel systems. These easy-to-use systems are plug-compatible with most makes of computer graphics equipment including:

- Adage/Ikonas
- Aydin Controls
- Calma
- Computervision
- Digital Equipment
- Gould De Anza
- IBM
- Lexidata
- Megatek
- Ramtek
- Sanders/CalComp

. . . and others

If you want to remote your graphics workstations, talk to Artel. We can help you design your entire communications network.

ARTEL COMMUNICATIONS CORPORATION

Write 32 on Reader Inquiry Card

P.O Box 100, West Side Station, Worcester, Massachusetts, 01602 (617) 752-5690 Cable: ARTEL

Innovative Packaging Improves Color Graphics Boards' Resolution

by Dave Wilson, Sr. Tech. Editor

In the past decade, the cost of a graphics controller has decreased from $20,000 to less than $2,000, while size has shrunk from a chassis full of electronics to a single board. Performance and functionality have improved by orders of magnitude. Today's graphics boards may include some or all of the functional blocks of **Figure 1**. Improvements in VLSI, custom logic and innovative packaging techniques have been driving forces behind size reduction and capability.

Custom LSI devices and new packaging techniques solve PCB space constraints.

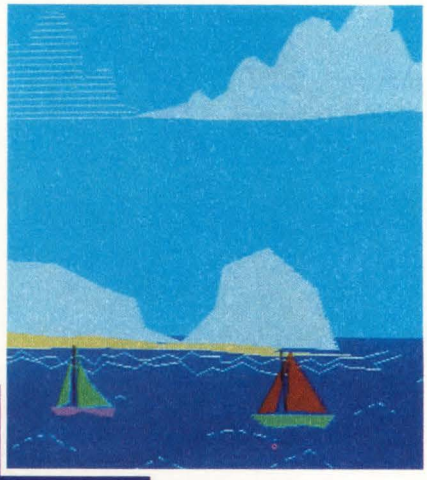
Controllers

Graphics boards are becoming increasingly intelligent, offloading many tasks that were conventionally handled by the CPU card. At present this may include drawing capability, but future boards may handle all modification of display memory, including area fill and shading, as well as anti-aliasing. Controllers may come in the form of discrete logic, a CPU, a dedicated VLSI device such as the NEC 7220, or a combination of both CPU and graphics controller.

Often designers look for controller implementations that occupy a small PCB space at a reasonable price, which is one of the reasons that the NEC 7220 has become an industry standard, having been implemented by Matrox, dy4, Ikier and Heurikon. Unlike CPU-based graphics boards, where the CPU handles the drawing and refresh functions, the 7220 graphics display controller offloads these tasks, drawing points, lines, arcs and rectangles. To facilitate systems integration, some manufacturers have incorporated front end microprocessors into their graphics boards, making the boards friendlier and more flexible. This allows for the capability to emulate existing graphics devices, such as the Textronix 4010 series.

The 7220, in performing its drawing operations, must read in from memory a "word" consisting of 16 single bits obtained from 16 consecutive pixel locations. Its internal registers must compute the proper display memory word address as well as which of the 16 pixels is to be modified to draw the line passing through the word. It then accounts for how this pixel should be modified, given its programmed line pattern and the type of modification to be performed. Finally, the 7220 reformats the display "word" and rewrites it into display memory. This process works well without modification in a black and white system where a "1" in memory means white and a "0" means black. When extending the GDC's functioning to color, a difficulty arises. In a color system each pixel is represented in memory by a multibit value. The 7220 must deal with a word consisting of 1-bit values from 16 consecutive pixels. The straightforward approach is to process each bit "plane" in sequence. Thus, in a 4-bit system, 4 draws of the same line would be required to write a white (all 1s) line over an arbitrary background. Some shortcuts may be obtained by restrictive color limitations and clever software techniques, but these methods sacrifice the usefulness of the display device.

Graphic Strategies has taken a different approach (see **Figure 2**). The Versabus-based VGM-1024 contains a color register external to



Color output from the STD-bus compatible DSTD-777 from dy4 Systems (Ottawa, Ontario, Canada).

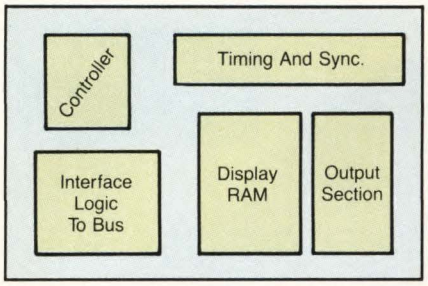


Figure 1: A typical graphics board includes some or all of these functions.

the 7220. Data in the color register is processed through an arithmetic logic unit (ALU) with data output from the display memory. This permits not only simultaneous writing of arbitrary data to all bits of the proper pixel, but also allows operations (selected via a separate mode register) to be performed between the drawing color and the previous contents of memory. Additionally, a plane mask is provided allowing modification only to the selected bit planes. This technique is transparent to the 7220 allowing high-speed line drawing (800 ns/pixel with 7220 at 5.0 MHz) with full line and area patterning capability. Since the additional registers are external to the 7220, it is necessary to coordinate their activity with the 7220. In particular, any drawing commands loaded into the 7220's front-end FIFO must be allowed to execute prior to changing the color, mask or mode register's contents.

The modes available by programming the ALU control register include LOAD, AND, OR, and other functions. EXCLUSIVE OR (EXOR) mode is very useful for viewing figures of a transitory nature such as cursors and for previewing graphic entries before entering them into memory. By redrawing a figure in EXOR mode, memory is restored to its previous contents. This feature enables the user to anchor one end of a line and move the other end on the screen in a "rubber band" fashion. This is accomplished by selecting EXOR mode and drawing the initial line. Then, when it is determined that the line is to be moved, the original line is redrawn (to erase it), coordinates are exchanged, and a new line is drawn. Once the final position has been established, LOAD mode is selected and the line is permanent.

The VGM-1024's video section processes the 4-bit video stream through a RAM look-up table to produce a 6-bit color code (2 bits per primary color). This code is then combined with blanking and sync signals to produce a standard composite video output.

Interfacing

To the system CPU, a graphics card may appear as memory or I/O. If it looks like memory, memory allocations are provided on the board for system access, an approach taken by Scion, with its IBM PC product, the PC640. The PC640's 256K memory can be mapped into the PC's address space starting at the selected address. The PC640 generates the first 150K of its 256K memory at the video frame rate. One of the advantages of this approach is that all but the final 64 Kbytes of the remaining 106 Kbytes in the 256 Kbyte memory are free for any other use as PC RAM.

Since the video memory is accessed from the system CPU, a hole is created in system memory using this approach. If the video memory is small, this is not critical, but in an STD system, where most processers can only address 64K, no memory would be left for the system after the addition to the graphics card.

The alternative is to organize video memory space as an I/O device, with DMA capability. This is an approach that Heurikon, Ikier and dy4 have all taken in their board design. Blocks of data can be transferred between system memory and on board display memory without intervention by the system computer. In the Heurikon and Ikier designs, this is executed by a hardware DMA controller that works in conjunction with the NEC 7220 GDC.

A new VME-based design, still under wraps at dy4, will bypass the NEC chip and allow the CPU to access memory directly, adding considerably to the speed of the system.

Output

The output section of graphics boards synthesize the color video output signals from display RAM data. The most common method, and one implemented by both Vermont Microsystems and Ikier, converts RGB digital via triple D/A converters.

Due to high rates involved in the generation of high resolution graphics, Ikier has implemented the video generator on its HRG 2 board with emitter coupled logic. Further speed advantages were obtained by the repackaging of the HRG 2's 4-bit D/A converters in a single custom hybrid IC, resulting in a 3:1 reduction in space and a 2:1 reduction in conversion time from 4 nsecs to 2 nsecs per conver-

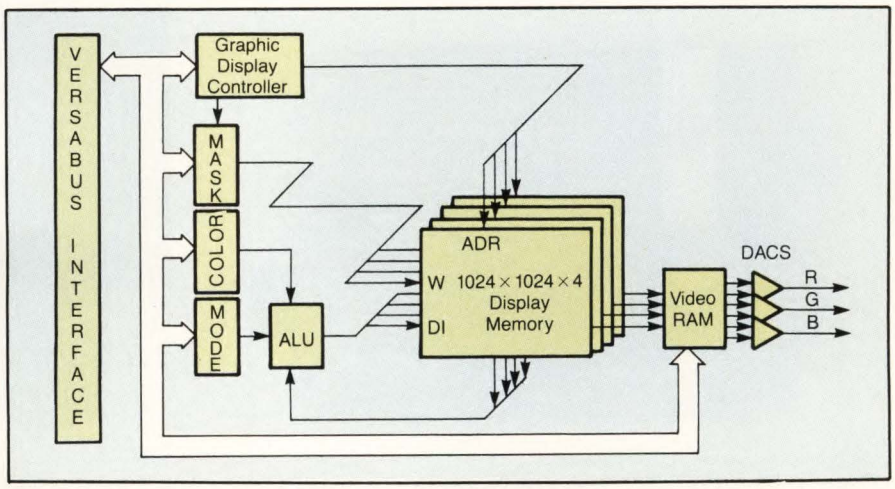


Figure 2: Graphic Strategies VGM-1024 Versabus design.

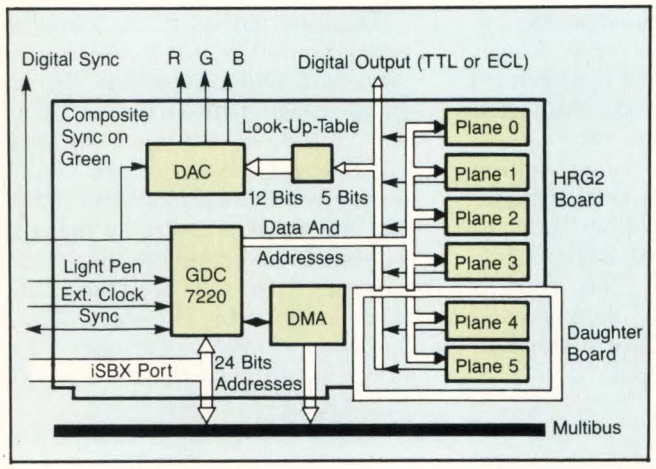
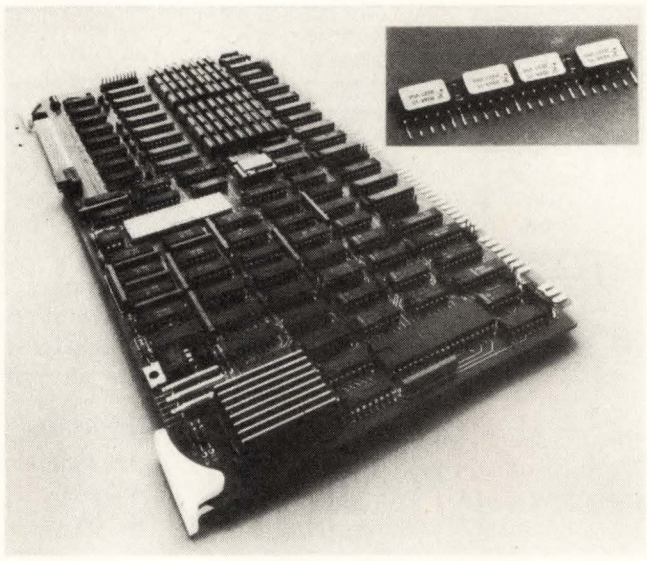


Figure 3: Ikier Technologies HRG2, a 1024×1024×4 raster graphics controller.



sion. The resolution and number of colors displayed on the screen is a function of the size of video memory of the graphics board. At the high end, squeezing more memory into PC boards with industry standard form factors has forced many companies to look at innovative packaging technologies.

The Heurikon controller, the MLZ-VDC, a Multibus video board, uses a stacked 64K technology to give 512K bytes of video memory arranged as 4 overlapping planes (1024 × 1024 pixels). The compact memory of the Ikier HRG-2, a 16-color raster graphics controller for the Multibus, is accomplished in part by mounting four 64K devices on a single in-line package (SIP), an approach recently used by Perkin-Elmer for the memory board of its under $10,000 supermini. Sixteen of the resulting 256K devices, occupying an area only 2″ × 5″, form a 512K byte array on the Ikier board (**Figure 3**).

Software Support

Graphics boards fall just short behind CPU boards when it comes to the amount of software needed to support them.

Typically, graphics software today will be written by the user in a high-level language, such as Fortan, C or Pascal. To aid in programming, many companies offer subsets of existing standards (such as Siggraph, Core and GKS). The most basic of these comprise about 20 or 30 routines that the programmer can call on to draw lines, set colors and erase pixels, etc. The rest of the standard may comprise transformations, data bases, etc.

Untypically, VMI have chosen to offer a driver that makes its product (the 8850) compatible with the DI-3000 library, provided by Precision Visuals. This allows the company to concentrate upon the hardware/software design involved with its Multibus board, while taking advantage of the comprehensive resources of PVI in supplying the software library.

Native Device Languages

Each graphics board may have unique capabilities that are not fully captured within a standard. To take advantage of these hardware features of the product, many manufacturers offer native device languages to be used at the graphics

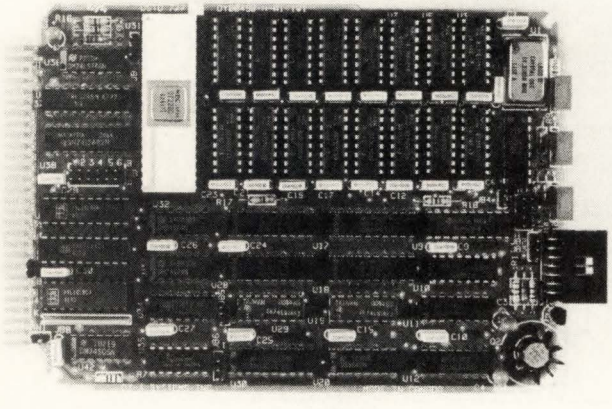


Figure 4: The DSTD-777 from dy4 Systems is configured with 128k bytes of video memory.

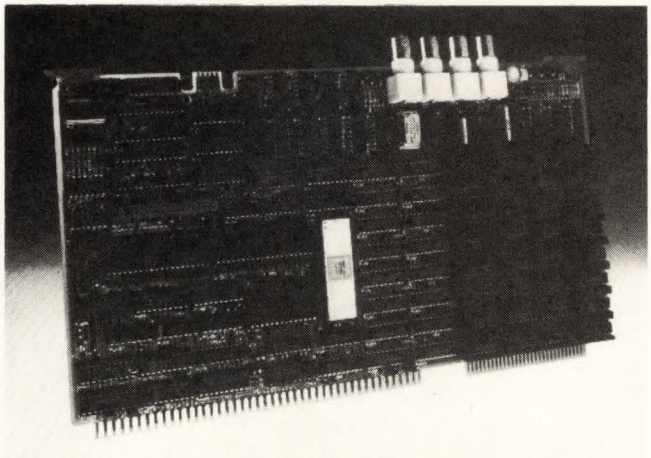
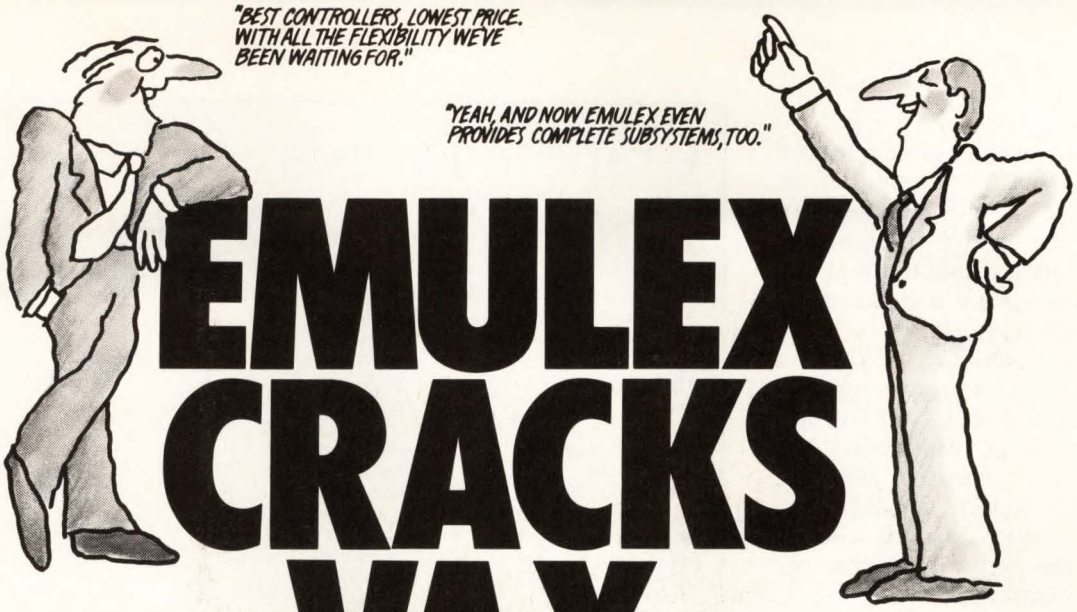


Figure 5: Heurikon MLZ-VDC incorporates innovative memory packaging technology.



EMULEX CRACKS VAX.

Emulex introduces the SC750 disk controller. And suddenly your VAX-11/750 disk drive options are wide open. It's the only DEC alternative.

You can mix brands. Mix storage capacities. Mix media types. All working off a single controller.

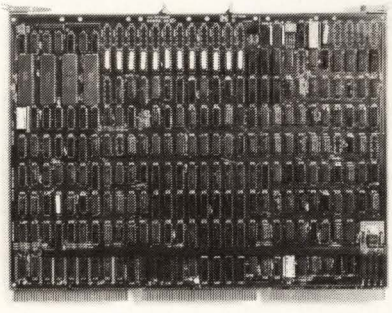
Better yet, the SC750 gives you all of this flexibility along with maximum system performance and media compatibility.

Our new controller is fully embedded and designed expressly for the VAX-11/750 CMI bus structure. Yet it costs thousands less than DEC and other "boat anchor" designs. This software transparent controller emulates the DEC RH750 Massbus adapter with attached RM03, RM05, RM80 or RP06 drives.

And all of the great features of the new SC750, like all Emulex controllers, are available as complete disk subsystems, pretested and installed by Emulex.

Read the facts below, then get the whole story on our total commitment to the VAX marketplace by writing or calling Emulex Corp., 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, California 92626, Toll-Free (800) 854-7112, In Calif. (714) 662-5600.

In Europe: Emulex Corp., 10th floor, Cory House, The Ring, Bracknell, Berkshire, England. Telephone: 0344-84234; Telex 851-849781.



SC750. THE ONLY ALTERNATIVE.

A single-board, embedded disk controller that interfaces directly to the VAX CMI bus. Functionally identical to the DEC RH750 with its disk adapters. Mix and match drive capacities from 80 to 675 MBytes. Serial data rates to 15 MHz to accommodate the new class of high-density drives. Features automatic self-test, intelligent buffer management, media compatibility, software transparency, low cost and single-board reliability. Available now.

EMULEX

Complete VAX-11 disk subsystems now available.

GSA Contract #: GS-OOC-03589

DEC and VAX are trademarks of Digital Equipment Corporation.

Write 33 on Reader Inquiry Card

card level, accessing some powerful commands that the standard at the Fortan level does not support. Whether the native device languages are used or not is a trade-off between investment and maximum performance in a product.

Most users who are looking for maintaining investment in software over a period of time will do most of their work in a high-level language, using subroutine libraries; since native device languages are specifically not standard (device specific), the user will sacrifice upward compatibility. □

Graphic Boards Manufacturers Listing

To obtain more information on the following manufacturers, write in the appropriate Write Number on the *Digital Design* reader inquiry card.

dy4
Ottawa, Ont.
Write 300

Graphic Strategies
San Jose, CA
Write 301

Heurikon
Madison, WI
Write 302

Ikier Technology
Bedford, MA
Write 303

NEC
Natick, MA
Write 304

Precision Visuals
Boulder, CO
Write 305

Scion
Reston, VA
Write 306

Vermont Microsystems
Winooski, VT
Write 307

256-Color Graphics for the Q-Bus

Peritek Corp. recently announced model VCH-Q, a compact, direct-access color graphics add-in memory suitable for use with any Q-Bus processor. The unit is configured to give 512×512 resolution for high resolution 8-bit color applications.

Packaged on a module which plugs directly into the Q-bus, the unit contains the necessary hardware to connect the Q-Bus μCs with a Peritek color or monochrome CRT monitor, as well as any standard RGB monitor. It can produce 256 colors or gray scale on screen from a palette of over 16 million. By adding accessory products, such as a Peritek keyboard or touchscreen, the user can create a complete modular graphics system at a much lower price than any standalone configuration. Peritek also supplies extensive software support for all its graphics interface cards including the VCH-Q.

Q-Bus μC users who require additional color will find expanded applications with the 256 colors on screen at one time. The VCH-Q contains two memories: a 128K × 16 graphic image display RAM (which houses the frame information), and a 256 × 24 bit color lookup RAM which controls the color selection associated with the 8-bit pixel values. In the graphics memory, each 16-bit word represents two 8-bit pixels in the 512 × 512 display frame. The 8-bit pixel value associated with each dot on the screen acts as an index into the color lookup RAM. This lookup memory contains color levels for red, green, and blue signals sent to the monitor. The VCH-Q can display 256 simultaneous colors or gray levels.

Access to the VCH-Q's graphics and color map memories is provided via the I/O of system memory. An array of 256 16-bit registers provides a window, one raster line at a time, to the image buffer. This array can be located on any 256-word boundary in the 4K word I/O page address space. A control/status register bit is provided which allows the user to select one of two 256-word registers to use as the color lookup RAM. This allows alternate color map settings on a frame-by-frame basis and provides the capability for special visual effects, animation, and similar uses. The VCH-Q's control/status register permits synchronous access to the color lookup RAM(s) (these functions can be performed during the vertical interval), ensuring that each display frame is complete.

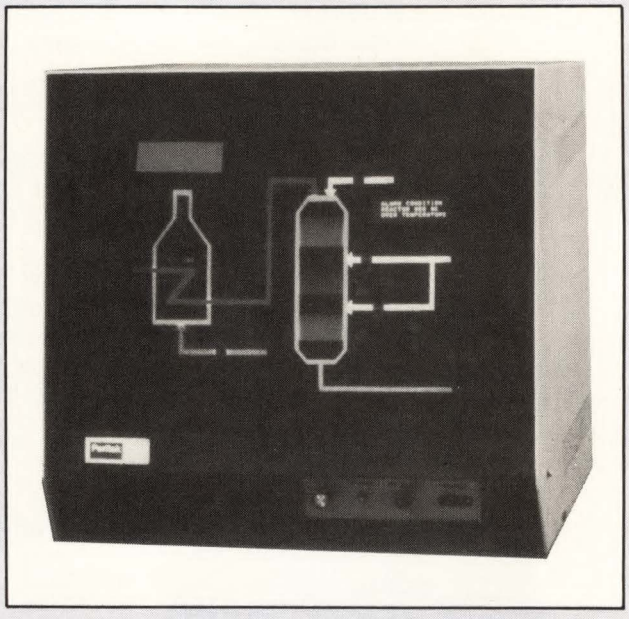


Figure 1: Suitable for use with any Q-Bus processor, Peritek's color graphics add-in memory gives 512 × 512 resolution for 8-bit applications.

The display may be scrolled, in multiples of 16 raster lines, under hardware control via hardware registers on the board. The VCH-Q produces a standard video signal which may be altered under program control to compensate for individual monitor characteristics.

Tom Birchell, Peritek Corp., 5550 Redwood Rd., Oakland, CA 94619. **Write 238**

DESIGNER UPDATE

AUGUST 1983

OUR MULTIBUS A/D-D/A BOARDS HAVE A LOT BEHIND THEM

The key ingredient for a reliable, high quality analog interface board is a realiable, high quality A/D and D/A converter. Our analog boards use Datel's proprietary hybrid microcircuit converters fabricated with our own high stability ladder networks.

Years of systems experience lie behind each board we build and we're experts at connecting computers to the analog world.

Our Sinetrac family incorporates features such as selectable base addressing, programmable scan start interrupt timers, start/final channel selection, programmable gain, 8 or 16 bit data transfer and 16/20 bit addressing. In addition, most boards directly connect to 4-20 mA industrial process loops.

The Sinetrac family of I/O boards plug right in to the latest 8086-series computers and are supplied with diagnostic disc software to get you started.

Choose from this popular MULTIBUS series:

ST-711/732
Direct replacement to iSBC-711/732.
32S/16D A/D and 2 D/A channels. 16/20-bit addressing. PGA and interrupt scan clock. 12-bit resolution. From $624. (1-4).

ST-724/728
4 or 8 channel, 12-bit D/A with 4-20 mA loops. 20-bit addressing (728). From $545. (1-4).

ST-716
4 or 8 channel D/A with 14-bit linearity. 16/20-bit addressing. From $690. (1-4).

Call or write for complete information.

DIAL 617 339-9341 Ext. 100

Literature Hot Line

DATEL INTERSIL

11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340 • Santa Ana, CA (714) 835-2751 • Sunnyvale, CA (408) 733-2424 • Los Angeles, CA (213) 933-7256 • OVERSEAS: DATEL (UK) Tel: Basingstoke (0256) 69085 • DATEL (France) 602-57-11 • DATEL (Germany) (89) 530741 • DATEL (Japan) Tokyo 793-1031.

See Us at MIDCON 83, Booths 3135-3137.

Write 34 on Reader Inquiry Card

Fault Tolerant Architectures

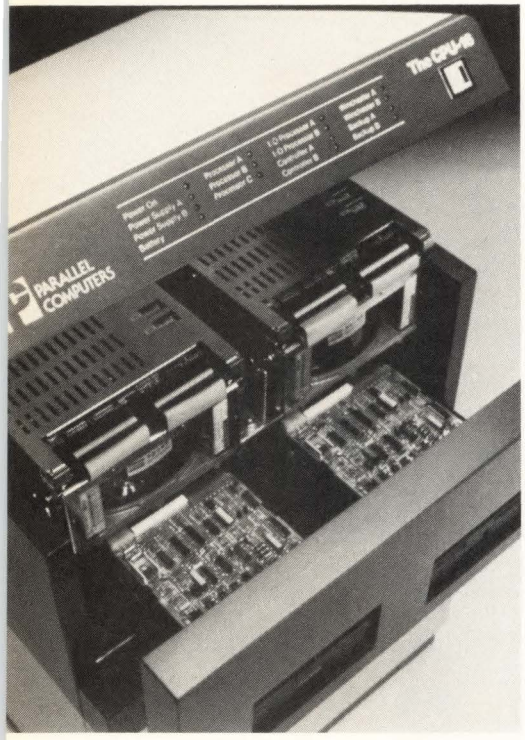


Photo courtesy Parallel Computers, Inc.

Demands for data integrity and system availability are promoting the design of new fault tolerant systems.

by Douglas Eidsmore, West Coast Technical Editor

Fault tolerance is no longer the privy of online transition processing and realtime control systems, but is proving cost effective in general business applications. With the cost of hardware dropping and the value of computer uptime increasing, fault tolerant systems are becoming more cost effective. This is especially true if they are designed to be easily repaired, as many of the new systems are.

The key goals of a fault tolerant system are to maintain data integrity and maximize system uptime. To meet these goals, a fault tolerant computer must detect and compensate for or correct faults. The methods of meeting these goals and needs are as varied as the online transaction processing, realtime process control, IBM compatible, and general business fault tolerant or fault resistant computers that are described in the following review.

Transaction Processing

Tandem Computers (Cupertino, CA) introduced their first dual processing system in 1976. Designed for high-volume transaction processing, their basic scheme was to run two processors in a loosely coupled fashion with periodic software checkpointing designed to transfer tasks from an errant processor to a backup. Today's Tandem NonStop II systems consist of multiple independent interprocessors. Each processor module is an autonomous computer system with its own memory, power supplies, diagnositc facilities, and I/O capabilities. A system can contain from two to sixteen processor modules. In addition, a network operating system allows users to network up to 255 NonStop II systems. Each system may have up to 16 processors for a total of 4,080.

Processors are interconnected by two independent 13 Mbyte/sec busses (Dynabus). The two busses provide a potential communications bandwidth of up to 26 Mbytes/sec among processors. In effect, the Dynabus unites the multiple processors into a single system. In conjunction with the Guardian operating system, the Dynabus hides the multiple processor architecture from an application program. Programs can therefore be written as though the system has a single processor.

Each processing module includes a central processing unit (CPU), main memory, a Dynabus interface unit, an I/O processor and a Diagnostic Data Transceiver (DDT) processor. Unlike the μP-based systems described below, Tandem's CPU is implemented using Schottky TTL logic and a stack architecture. The processor's internal data paths and registers are parity checked to ensure data integrity.

Memory boards contain either 512 Kbytes or 2 Mbytes of storage. Up to four boards may reside in one processor. A fully configured 16-processor system allows for up to 64 boards with a total of 128 Mbytes of memory. ECC is used to correct single-bit and detect any double-bit errors. The ECC also checks the address sent from the CPU to be sure the memory access is valid.

A separate buffered processor is dedicated to I/O operations. Because the I/O processor operates independently from the CPU, I/O transfers require a minimum of CPU intervention. A Diagnostic Data Transceiver (DDT) is included as part of each processor module. The DDT allows communication between a processor module and the Operations and Service Processor (OSP), and monitors the status of the central processing unit, Dynabus interface, memory and the I/O processor and reports errors to the OSP. The OSP is located in the system console. It provides an operations interface and acts as a diagnostic and maintenance tool.

Disk drives are dual ported. As an option, the system supports mirrored disk drives to ensure that the data base is available even if a disk fails. Mirrored disks are almost standard operating procedure in fault tolerant systems. A mirrored disk is a pair of physically indepen-

dent disk drives treated as a single volume. During write operations, the system writes the same data to both drives. During read operations, the system can access data from either drive, and can use this capability to reduce read head movement and seek time. When a failed member of a mirrored pair is restored to operation, the system automatically brings the disk up to date while it continues application processing using the other member of the pair. When a write command is issued, the operating system automatically and transparently updates both disks. In the event of a failure, the operating system sees that one disk is down and continues processing on the other disk.

The operation of the operating system is based on the concept of process pairs. (A process is a set of executable object code instructions.) The primary process is the active program. The backup process, which resides in a different processor, is a passive copy of the primary process; its demands on resources are minimal.

Although Tandem's design is older than recent, less expensive modular μP–based fault tolerant systems, the architecture has advantages. For example, their processors are in effect minicomputers designed to be part of a multiprocessor system. But, the initial cost of minicomputers running in tandem is high and so is expansion. Software development is also expensive and much of the checkpointing must be done by application developers. Primary programs can also be slowed by sending check points. The company is not standing still, however, and newly released options include: transfer, an information delivery system; SNAX, a communications services software package allowing computers using IBM's System Network Architecture to communicate with Tandem systems; and INFOSAT, a satellite communications system. In a sense, Tandem's approach to fault tolerance is (with the frequent checkpointing) to a large extent based on software.

The Stratus/32, from Stratus Computer Inc. (Natick, MA) is a Continuous Processing System composed of multiple, independent processors called Processing Modules. The Stratus approach is hardware based and the burden of fault tolerance is removed from the application developer. CPUs memory, controllers, and peripherals within a Processing Module are duplicated. The two CPUs on a processing module run in lockstep. The results of each computation are compared between the two onboard processors and between Processing Modules. Failed components are automatically taken out of service before erroneous processing occurs or data is corrupted and the system continues to process with the duplexed partner. A basic system contains a fully duplexed processing module. A system can expand to 32 selectively duplexed modules.

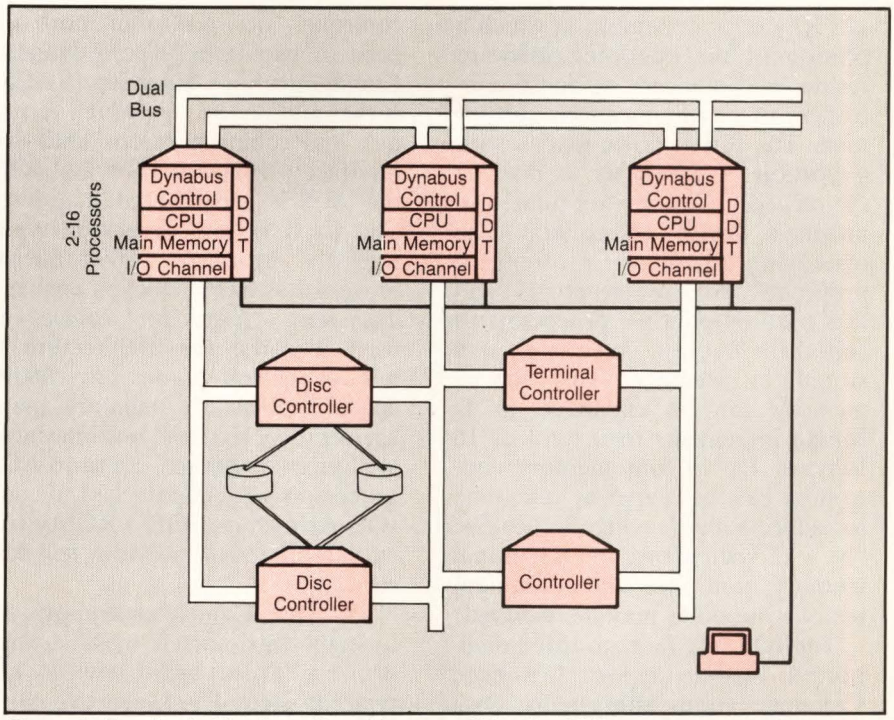


Figure 1: Tandem's NonStop II architecture. Schottky TTL processors are interconnected by two independent 13 Mbyte/sec busses. A Processor includes a buffered I/O processor, a diagnostic data transceiver, memory and a CPU. Processors are loosely coupled.

The processing modules are connected together by a ring network that transfers data at 1.4 Mbytes/sec. This network or StrataLINK allows modules to be located from several feet apart to many miles apart with the use of extenders. Without line extenders, modules may be up to 750 feet apart. An additional link ups the transfer rate to 2.8 Mbytes/sec.

Like the Stratus System, the Synapse N + 1 On-Line Transaction Processing System appears as a single processor to users and application programs. Unlike Stratus, Synapse Computer Corp. (Milpitas, CA) attains fault tolerance by adding one processor for fault tolerance to a system with N processors, thus the N + 1 designation. The theory is that a system only needs one extra of each type of resource. Performance is planned for the N level. With everything operating properly, superior performance should result from the additional hardware.

The system uses two types of processors. The General Purpose Processor (GPP) is the instruction processor that executes user programs and the majority of the Synthesis operating software from shared main memory.

The second type of processor is an Input/Output Processor (IOP). It also directly accesses main shared memory. Each IOP has a private

128-Kbyte local memory in which a portion of the operating software resides and manages up to 16 controllers or communications subsystems. The IOP is down-loaded with a portion of Synthesis to manage the physical I/O activities related to attached device controllers. The operating software, application programs, control structures and lists used by multiple processors to schedule system activities are stored in memory. This shared memory can be expanded in 1-Mbyte increments to a total of 16 Mbytes. Up to four memory controllers can be active at one time for address interleaving. To achieve "N + 1" redundance, an additional memory controller and additional memory modules may be included.

The IOP interfaces to three dual-ported module types: Advanced Communications Subsystems, Disk Controllers, and Multiple Purpose Controllers which interface to the power system, magnetic tape, line printer and system clocks. Up to sixteen of these modules may be attached to an IOP. All transfers between main shared memory and these modules are direct memory block transfers managed by the IOP. To assure multiple paths to all devices, all input/output modules on the system are dual-ported; each controller occupies one port on each of two IOPs. The Advanced Communications Subsystem (ACS) is the module through which terminals and communications lines are interfaced. Like the GPP and IOP, the ACS is a 68000-based processor. Each of the processor types uses the Motorola 68000 microprocessor as its "instruction engine." The term "instruction engine" is used, because the architecture is not dependent upon any 68000 characteristics. All memory management, caching and bus interfaces are Synapse's design. Up to 16 ACS processors may be attached to each IOP. As with the IOP, a ROM-driven sub-processor provides self-test capabilities.

The Disk Controller supports up to eight dual-ported mass storage devices. These eight devices are typically shared between two Disk Controllers. Overlapping disk head seeks-allows concurrent use of all devices.

Each Multiple Purpose Controller contains system clocks and a watchdog timer, and controls one line printer and up to four magnetic tape drives.

The Synapse Expansion Bus is composed of two independent busses that have an aggregate data transfer rate of 64 Mbytes/sec. All transfers between memory and processors occur on the bus, which arbitrates bus requests between the two independent pathways. Each bus has a 32 bit wide data/address path in addition to control and checking lines. If one bus fails, the system continues operating, using only the remaining bus.

Auragen Systems Corporation's (Fort Lee, NJ) 4000 Architecture is a mixture of tightly and loosely coupled processors. Multiple 68000s are grouped in tightly coupled multiprocessor units called Processor Clusters or Clusters. Each Processor Cluster consists of an Executive Processor Module, a Work Processor Module and a 1-Mbyte Memory Module. Each module has onboard diagnostic capabilities. A cluster can be expanded to contain up to four Disk/Tape Processor Modules, a maximum of four Communications Processor Modules and up to 8 Mbytes of Memory. Communications Processors are connected to external devices via Interface Modules. The modular system can consist of 2 to 32 loosely connected clusters. If one cluster should fail another is available to take over. Processors within a cluster communicate over a 20 Mbyte/sec Cluster Bus and clusters are connected via two 16 Mbyte/sec System Busses. If one System Bus fails, communication takes place over the other Bus.

Disk and tape drives are dual ported to Disk/Tape Processors in different Clusters. Data on the disk drives can be selectively or fully mirrored. Terminals and line printers are connected to Communications Processors in different Clusters via dual high speed 4 Mbyte/sec Communications Busses. Communications within the system continue when a Communications Processor or Communications Bus fails.

The UNIX System III compatible AUROS operating system provides fault tolerant computing and runs primarily in the Executive Processor. The Executive Processor is made up of a 68000 with onboard RAM and 16 Kbytes of ROM. It also has Cluster Bus and System Bus interface logic, direct

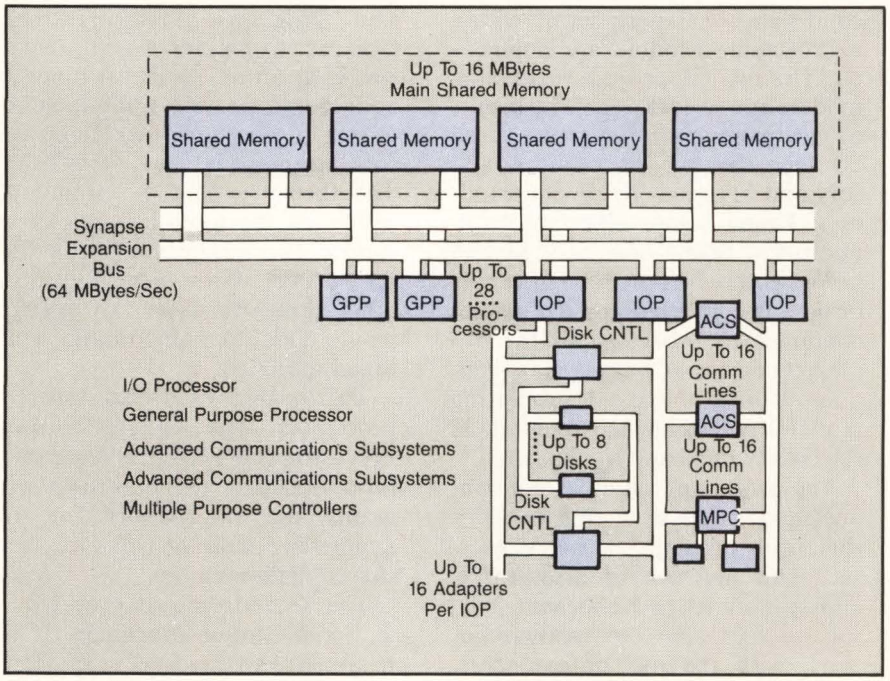


Figure 2: Synapse N + 1 system. One extra resource is added for fault tolerance.

adac...

The leader in LSI-11 I/O interfaces now offers software to match.

ADAC offers the widest selection of complete LSI-11 systems and function cards... both analog and digital. And now two new software subroutine libraries support all of ADAC's extensive line of interfaces for LSI-11. ADLIBRT is fully compatible with RT-11 (single user) real-time operating system software. ADLIBRSX enhances RSX-11M (multi-tasking/multi-user) operating system software.

Both ADLIB packages are simple to use, yet powerful, software tools that slash the time needed for program development.

ADLIBRT and ADLIBRSX support:

- mV Level A/D Conversion
- Temperature Measurements
- High Level, High Speed A/D Conversion
- TTL Level Digital I/O
- Discrete, High Voltage, AC/DC Interfaces
- Pulse Counters and Pulse Trains Out
- Optically Isolated Discrete I/O
- Contact Closure Sensing
- Discrete High Current Outputs
- Programmable Clock
- Serial Interfaces

Call, write or circle the number below to obtain our ADLIB data sheet and new catalog describing all of ADAC's LSI-11 compatible interfaces.

adac corporation

70 Tower Office Park • Woburn, MA 01801
(617) 935-6668

Write 35 on Reader Inquiry Card

memory access control logic, an onboard diagnostic processor, and a message buffer.

User programs execute in the Work Processor. This module consists of two 68010 CPUs which work simultaneously on separate programs. The Message System, which is a part of AUROS, automatically creates a backup copy of every executing program. This backup program does not execute, it simply receives and saves messages. These messages contain the same information that was sent to the executing primary process. If the primary fails, the backup can recreate and continue the work of the primary by processing its stored messages. This message system makes sure that backups read the available messages in the same order as the primary. The message system also ensures that when a backup process begins executing, it does not resend any messages already sent by the primary. Fault tolerance is transparent to both end users and programmers.

Tolerant Systems (San Jose, CA) is developing an expandable fault tolerant system based on flexible System Building Blocks (SBB). The internal operations of an SBB are segmented into an application processor, a file server, and a communications server. Each building block is capable of operating in any or all of the three functions—applications, file servicing, and communications. The blocks can be built up in an infinite number of combinations to meet a user's particular needs, from the basic requirements of a small business, to a complex, geographically distributed network of a large business. A complete system can be configured on a single SBB. Adding a second SBB creates a fault tolerant system and adding more SBBs increases performance by distributing software over the added hardware.

A single building block contains two μPs, 16 Mbytes of memory, a system bus and a highspeed I/O bus. National's 16032 is being used for prototyping, but the 32032 is planned as the production μP. One processor is used for realtime number crunching and I/O and the other for transaction processing. Diagnostics are run as background tasks. A cache memory with a 95% hit ratio is used to speed memory access. A UNIX operating system programmatic shell is used as interface to Tolerant's operating system.

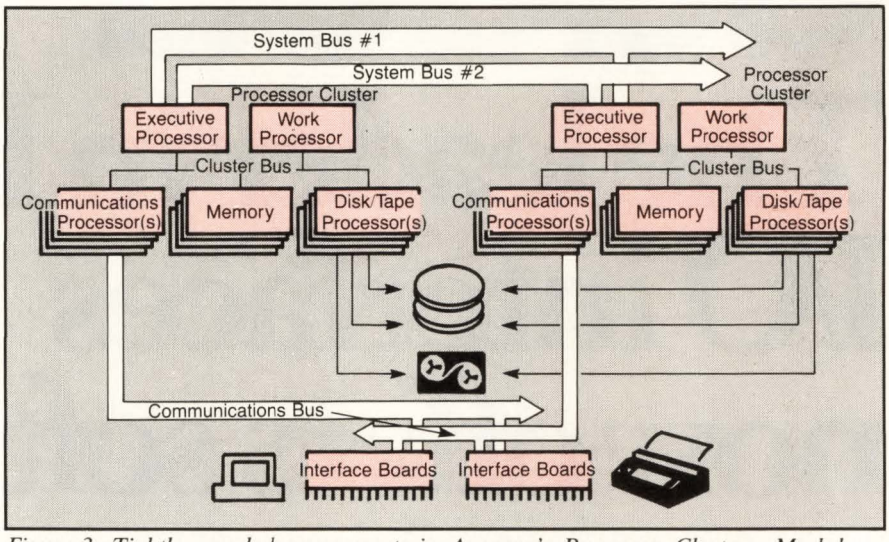


Figure 3: Tightly coupled components in Auragen's Processor Clusters. Modular system can contain 2 to 32 such clusters, all loosely coupled.

Realtime Control Systems

The reliability demands of a realtime process control system are at least as high or higher than they are for online transaction processing. A failure in a control system governing a powerplant can endanger life as well as property. Although realtime control and online transaction processing systems share the need for fault tolerance, other design considerations are quite different.

Realtime industrial control systems must monitor tens or hundreds of analog points. To deal with such a myriad of I/O, a realtime control system must have a large amount of RAM and high processing speeds. Unlike online transaction processors, disk access on a realtime control system is infrequent. John Willoughby, the President of August Systems (Tigard, OR) estimates that to design fault tolerance into their Can't-Fail Computer was much less demanding than designing process I/O and I/O to peripherals. Rather than using one control computer and another on standby, the Can't-Fail Computer uses three control computer modules (CCMS), each one separate and independent from the others with each module running its own copy of software. This redundancy appears as one control computer to the user and to the process.

All three of the control computer modules will independently read parameters and perform computations and vote. This voting takes place in a Process Interface Module. There are two basic types of cards, computer interface and process interface, in the module. The computer interface cards connect the control computer modules to the Process Interface Module. They route data to and from the various Process Interface cards. The Process Interface cards connect the Process Interface Module to the process itself. The Process Interface Module uses as many Process Interface cards as the application requires. The PI cards are designed to provide one of four functions; digital input or output, or analog input or output.

The Process Interface Module is also designed to detect failures within its own voting circuits. While the voting circuit itself is fault tolerant, once it has experienced a component failure it becomes vulnerable to a second fault.

DEC®-COMPATIBLE PERIPHERAL CONTROLLERS

LSI-11® compatible controller for 80-300MB SMD and Winchester drives from CDC, Ampex, and Fujitsu

Dataram Corporation offers the industry's widest range of DEC-compatible peripheral controllers — from comparatively simple NRZI tape controllers to complex 300 MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11, PDP®-11, or VAX® minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and, more importantly, space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

The chart shows our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.

CONTROLLER	DESCRIPTION	COMPATIBILITY
C03	Cartridge disk controller	RK05
C33	Cartridge disk controller	RK05
T03	NRZI mag tape controller	TM11/TU10
T04/C	Mag tape streamer coupler	TM11/TU10
T04/N	NRZI mag tape controller	TM11/TU10
T04/D	Dual density mag tape controller	TM11/TU10
T34/C	Mag tape streamer coupler	TM11/TU10
T34/N	NRZI mag tape controller	TM11/TU10
T34/D	Dual density mag tape controller	TM11/TU10
T36	Dual density mag tape controller	TM11/TU10
T34/T	GCR mag tape controller	TM11/TU10
S03/A, S04/A	80 MB/300 MB SMD controller	RM02/RM05
S03/A1, S04/A1	80 MB/160 MB SMD controller	RM02
S03/B	80 MB/300 MB SMD controller	RK07
S03/C	200 MB/300 MB SMD controller	RP06
S03/D, S04/D	96 MB CMD controller	RK06
S33/A	80 MB/300 MB SMD controller	RM02/RM05
S33/A1	80 MB/160 MB SMD controller	RM02
S33/B	80 MB/300 MB SMD controller	RK07
S33/C	200 MB/300 MB SMD controller	RP06
S33/D	96 MB CMD controller	RK06

Products printed in red are LSI-11 Bus compatible.
Products printed in black are UNIBUS® compatible for PDP-11 and/or VAX minicomputers.

DEC, LSI-11, PDP, UNIBUS and VAX are registered trademarks of Digital Equipment Corporation.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

Write 45 on Reader Inquiry Card

Should an initial failure occur, the system provides early warning via a self-testing sequence that monitors the output of the circuit while it cycles the inputs.

Even if one computer module should fail or produce an error, the process will never see the error. The two modules in agreement will act as a majority and control the process. At the same time, the incorrect computer will correct itself, based on the values of the agreeing computers, once the vote has taken place.

To prevent the propogation of errors from a bad module to a good one, the units are isolated from one another. Each module has two communicator ports that provide a read-only, point-to-point interconnection between the three units. Each communicator port consists of independent, asynchronous input and output sections. This independence allows the input side of a port to request a word from the memory of another unit, while the output side can be accessed by another CCM. By virtue of its read-only configuration, the communicator is incapable of writing into the memory of another unit; a faulty

Bus Interface And Memory Control Units Promote Fault-Tolerant Processing

Intel's recent addition of two new components to its iAPX 432 Micromainframe processor family (the iAPX 43204 Bus Interface Unit and the iAPX 43205 Memory Control Unit) provides the switching and interface circuitry needed to build fault-tolerant multiprocessor systems. Together they perform bus arbitration, dynamic RAM control, error-correction coding and error-confinement tasks.

The BIU and MCU detect failures and automatically switch to a redundant processor, bus or memory. Thus systems can be built that will endure the failure of any single component or bus. All the fault detection and recovery functions are transparent to the application software.

The BIU and MCU components give system designers the freedom to choose an optimum configuration that would be based on cost, performance and the desired level of fault tolerance. Systems can range from partial fault tolerance with Functional Redundancy Checking (FRC), to complete fault tolerance (in which any single component or bus's failing would not crash the system) with Quad Modular Redundancy (QMR).

Four processor components are involved in a QMR configuration: a master pair and a shadow pair (**Figure 1**). Each pair is made up of one functioning unit and a replica "checker unit" that observes the signal put out from its mate and reports any disagreement. If one of the master components fails, the master pair is disabled and the shadow pair immediately takes over. Fault detection and the disabling of a failed processor pair are transparent to both application and system software. The system software is notified that a failure occurred after the recovery. The error is confined, the system never crashes and performance does not vary.

An FRC configuration can be used if the application calls for a high degree of confidence in the system's calculations yet can tolerate a short disruption in task processing while the system software is responding to an error.

An FRC system uses two components: a single master unit and a replica unit that checks the master's results (**Figure 2**). This second checker component ensures that no single hardware failure will corrupt the results of a critical computation. System software still must disable the faulty resource and restart the system, but the FRC configuration prevents any hardware error from being incorporated into the computation. **Write 337**

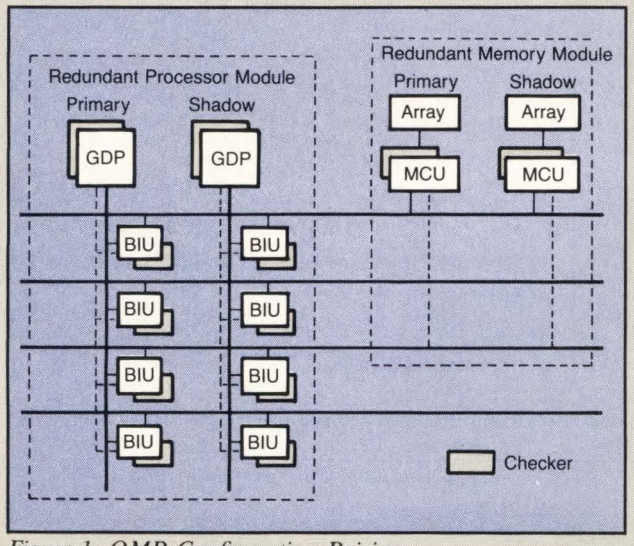


Figure 1: QMR Configuration Pairing

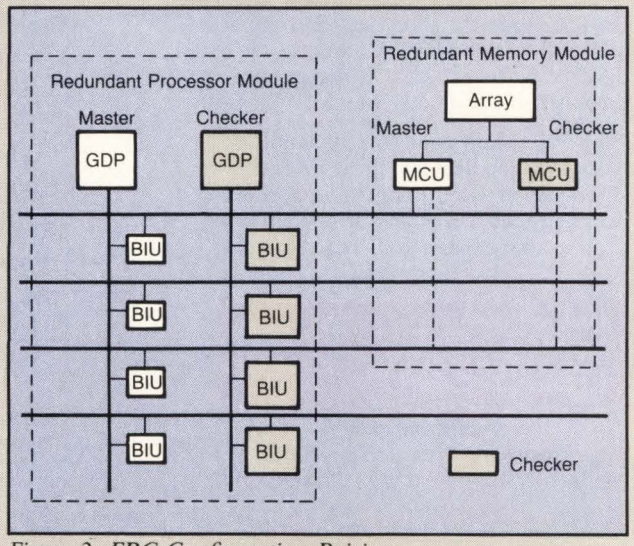
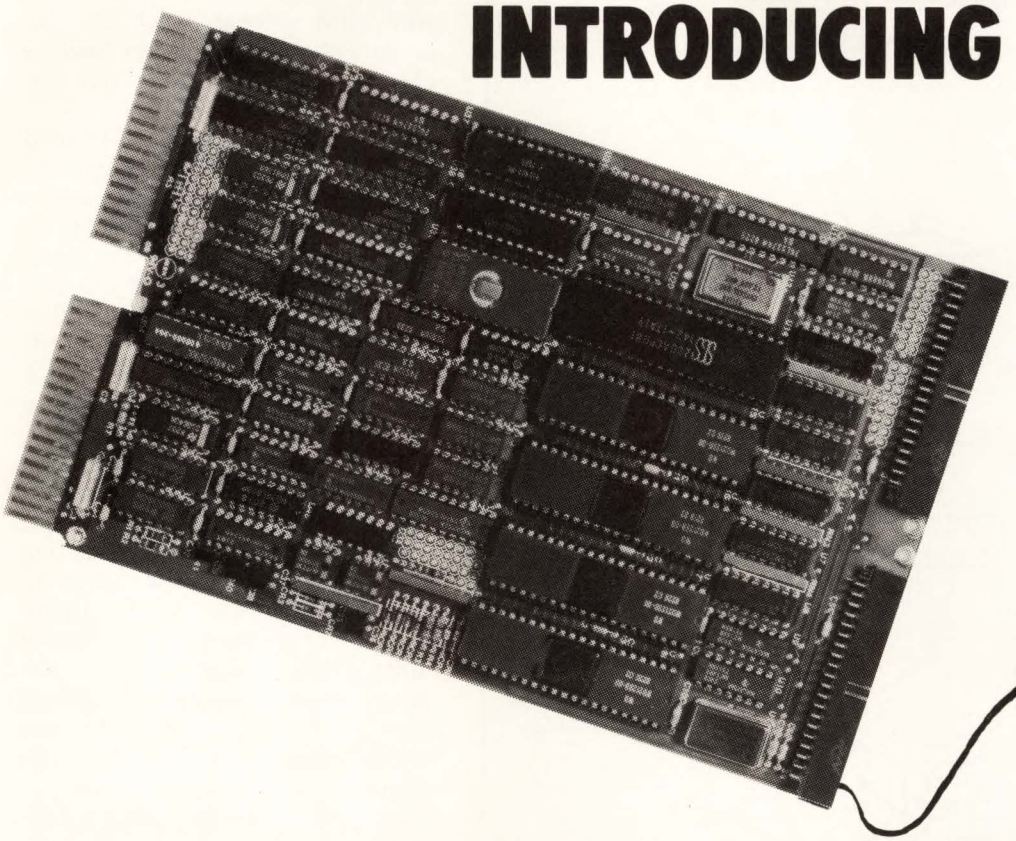


Figure 2: FRC Configuration Pairing

LSI-11 USERS:

INTRODUCING



A LOW COST

EIGHT-CHANNEL DZV 11.

SCD-DZV11 FEATURES:

+ Eight-channel asynchronous multiplexer
+ Fully compatible with DEC* operating systems and diagnostics designed for the DZ11
+ Programmable baud rates from 50 to 19.2K baud
+ Switch selectable address and vector assignments
+ Optional rackmount distribution panel
+ Can interface to full duplex modems such as the Bell Models 103 and 113 or equivalent
+ Includes two 40 pin ribbon cable connectors for connecting RS-232C type communication lines

SIGMA offers a complete line of DEC* compatible products for the LSI-11.

CALL your nearest sales office for information on all products.

ASK about Sigma's NEW 8-channel dual-wide DLV11J/8.

SIGMA'S DONE IT AGAIN!

Sigma Information Systems

6505C Serrano Avenue, Anaheim CA 92807
Telex 298607 SGMA (714) 974-0166

Orange CA (714) 633-0652 / 771-7320
San Jose CA (408) 243-9112 • Valencia CA (805) 259-6559
Arvada CO (303) 431-0551 • Winter Park FL (305) 628-8896
Boston MA (617) 938-1310 • Minneapolis MN (612) 881-5015
Edison NJ (201) 572-3722 • Albuquerque, NM (505) 294-5423
Gresham OR (503) 241-2216 • Houston TX (713) 451-0466 X71
Vienna VA (703) 448-6800

* Registered trademark of Digital Equipment Corporation

Write 37 on Reader Inquiry Card

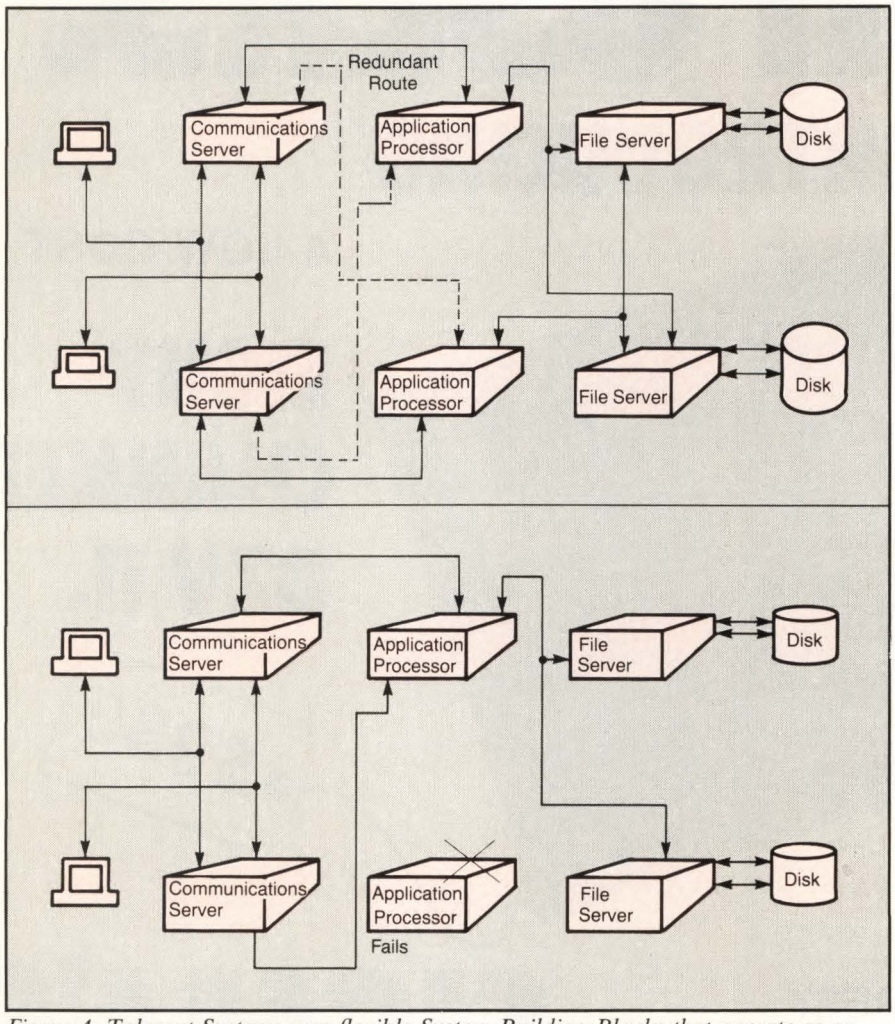


Figure 4: Tolerant Systems uses flexible System Building Blocks that operate as applications processors and file and communication servers (A). If one block fails, system switches to alternate resources (B). In addition to fault tolerance, the architecture allows users to define the system configuration.

unit cannot corrupt operation of the other units.

A Real Time Task Supervisor (RTTS) operating system handles all scheduling, dispatching, and inter-module coordination, including synchronization, voting, process I/O, message passing between tasks, and interrupt handling. RTTS relieves the user of the specific details of providing fault tolerant operation.

IBM Compatibility

One characteristic all the previous computers share is they all lack IBM compatibility. The following two systems are IBM 370 compatible and incorporate features that promote availability.

IPL System's, Inc. (Waltham, MA) 4480 Continuous Computer was not designed specifically for on-line transaction processing. With two tightly coupled CPUs accessing a shared memory, the architecture resembles IBM's 370/370 Multi Processor. The CPUs communicate over a signal processing path. The disadvantage of this approach is that they both run the same software; a software error on one CPU is propagated throughout the system. The advantage of such a system is that communication is memory rather than bus or message based, resulting in superior performance when operating normally.

The system runs IBM VM/370 and MVS operating systems. Neither operating system is designed with fault tolerance as a key factor, however MVS has some error detection and restart procedures. And IBM software such as IMS (a database manager) has built in checkpointing, journaling and logging.

The shared memory is divided into 8 or 16 1-Mbyte segments. Each segment has dual port access. One CPU can go down without effecting memory access by the other. Also, a 1-Mbyte block of memory can fail without effecting the other blocks. If a critical piece of software was residing in that block when it crashed, that software would be lost.

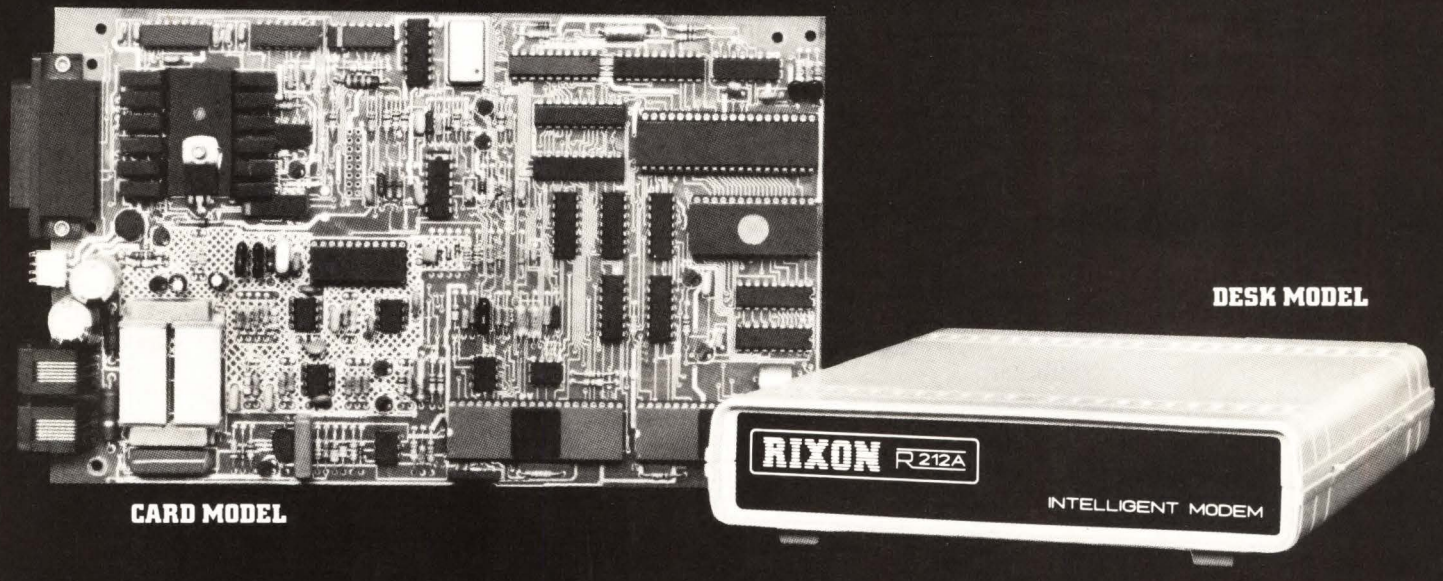
Formation Inc. (Mt. Laurel, NJ) has also announced a system for the IBM 370 software environment. Their Formation 4000 Information System uses a single bus architecture that supports a CPU, Input/Output Controllers and memory units. These system elements operate under the control of a System Control Processor (SCP). A two board processor set, the SCP constitutes a complete system with its own console, memory, floppy disk, and power.

The SCP performs power-on confidence tests on all system elements (including itself) each time the system is powered on or whenever the SCP detects a failure. Assuming multiple system elements are present, the SCP is then able to reconfigure the system automatically on the basis of these tests. The system software is designed to accommodate software but not recovery. It is therefore not truly fault tolerant. The F/4000 Model 300 provides the most complete fault resistant configuration. Models 100 and 200 may be expanded in modular increments to the same level.

Fault Tolerance As A Feature

Many computer visionaries see fault-tolerance as a worthwhile feature for a computer to have in any environment, not just in online realtime applications. Parallel Computers, Inc. (Santa Cruz, CA) envisions their CPU-32/16 fault tolerant computer in applications where fault tolerance hasn't been

OEM



INTELLIGENT 212A MODEMS

The Rixon® 212A Intelligent modems offer 300/1200 bps full duplex operation with auto dial, auto answer, and auto capabilities. All commands (including dialing) and options are controlled from the DTE keyboard and are stored in the battery protected modem memory. The auto dialer is operative in Rixon's own user-friendly format, and can store up to 10 numbers of 60 characters each including description field and log on characters for each number. A simple keystroke is all that is required to dial, and auto log on, or display stored numbers.

These OEM modems are the most versatile 212A Intelligent modems in todays marketplace. They are available with 4 different standard DTE and power interface combinations, or we can relay out and design to meet your exact specifications with the use of our CADDS system. For those of you wishing to OEM the desk top models, our stand-alone version can be delivered to you with a custom colored case labeled with your own corporate identification. So don't think of these as Rixon modems, think of them as yours.

The OEM 212A Intelligent modems are priced at $360. or less depending on OEM quantity and terms. For more information call Nick Whelan at 301-622-2121 or write to Rixon Inc. at 2120 Industrial Parkway, Silver Spring, Maryland 20904.

RIXON

Write 38 on Reader Inquiry Card

used before. CPU-32/16 was not designed for online transaction processing but rather as a reliable system to operate in traditional multiuser environments. Priced at $25,000 for a basic 32/16-bit end user system, the CPU-32/16 provides true hardware and software fault tolerance without a premium price.

Fault tolerance is worthwhile in any environment.

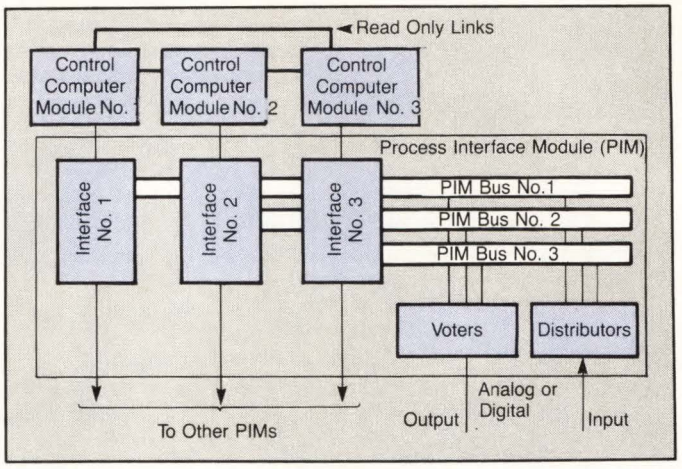


Figure 5: Realtime control system from August Systems uses triple redundancy for fault tolerance. Three control computer modules (CCM) process independently and vote on results. CCMs are connected by read-only links to prevent corruption. Each CCM reads all inputs and then reads input values obtained by other CCMs. A two-out-of-three vote removes input errors. After processing, the CCMs vote again and values are sent through PIMs to output circuit, where a hardware vote catches any errors introduced by a faulty PIM.

CPU-32/16 corrects for both hardware and software faults through a combination of redundant architecture, monitoring and fault recovery techniques. The system supports up to five Multibus based Parallel Processing Units (PPUs) with each PPU supporting up to 1 Mbyte of local memory. The PPU processing is done by a 68000 μP running at 10 MHz without wait states. Unlike the Stratus design, the coupled pair of PPUs do not run in lockstep or completely synchronously, although they both execute the same instruction stream. Instead, the second processor shadows the first. At specific spots in the UNIX kernel, comparison circuitry is used to determine the state of health of both processors. Up to 32 terminals communicate with the system through intelligent or unintelligent Input/Output Processors (IOPs). With an intelligent IOP, the terminal handling portion of the UNIX OS is offloaded to the IOP.

Modifications to UNIX that were necessary to achieve fault-tolerance are transparent to applications programs. Parallel's version of UNIX is a combination of Version 7, System III and System V. In addition, it includes many Berkeley enhancements, such as the VI editor and the "C" Shell.

On-line storage ranges from 20 Mbytes to 1.6 Gbytes of mirrored Winchester disk drives. Combinations of ¼" tape, ½" tape and 5¼" floppy disk are available for backup. An Ethernet compatible local area network is also available. The system will continue to operate for up to 10 minutes after power has failed from dual UPSs. Performance of the modular system can be increased by adding coupled pairs of PPUs.

NoHalt Computers, Farmingdale, NY, also offers a low cost system for traditional business applications. However their NoHalt NH-1000 only provides hardware redundancy. The system uses a CP/M and MP/M compatible operating system without fault tolerant provisions and can only accommodate hardware failures. The computer

Fault Tolerant Computer Companies

The following list, although not exhaustive, does include most companies building fault tolerant computers. To obtain more information write the appropriate write number on the *Digital Design* Reader Service Card.

August Systems
Tigard, OR
Write 326

Auragen Systems Corp.
Fort Lee, NJ
Write 327

Formation Inc.
Mt. Laurel, NJ
Write 328

IPL Systems, Inc.
Waltham, MA
Write 329

NoHalt Computers
Farmingdale, N.Y.
Write 330

Parallel Computers, Inc.
Santa Cruz, CA
Write 331

Stratus Computer, Inc.
Natick, MA
Write 333

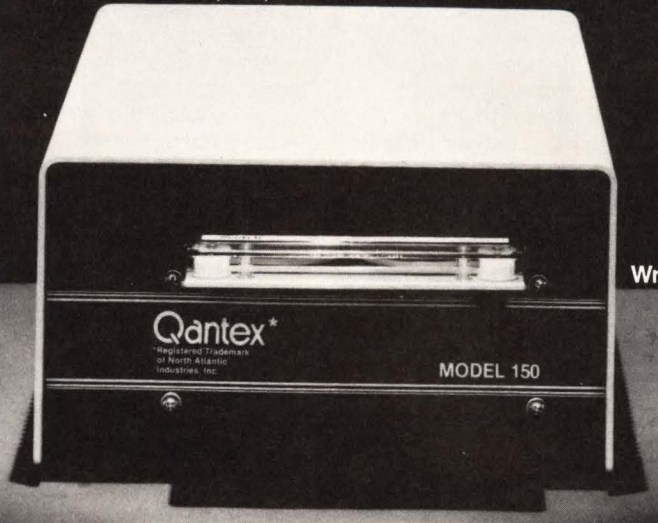
Synapse Computer Corp.
Milpitas, CA
Write 334

Tandem Computers
Cupertino, CA
Write 335

Tolerant Systems, Inc.
San Jose, CA
Write 336

THE WINCHESTER BACKUP SYSTEM

Just plug it in your computer system. No additional hardware or software is needed. Transfer data to a 17.2 megabyte tape cartridge. Perform file search, update records, edit and reformat data. Use it for Winchester backup, data logging, or archival storage applications. Interfaces are built-in for RS-232, Multibus, S-100, 8-bit parallel, or Ohio Scientific. For full details on the Model 150 contact: **North Atlantic Qantex,** 60 Plant Avenue, Hauppauge, NY 11788 (516) 582-6060



Write 62 on Reader Inquiry Card

consists of two redundant, distributed processing networks. There are two Z80B based system control processors with mirrored disks. Each system control processor/disk is connected to its own multi-channel data bus. As many as 16 slave processors can be installed in parallel between the two data busses. Each slave processor, with its own math processor, has four ports for connecting work stations, communications interfaces or other kinds of data devices. Should a slave processor fail, only the work stations connected to it are affected. Each of the two independent power busses terminates in its own power supply. A single UPS can be incorporated.

If the forecasters are correct, by the decade's end, fault tolerance will be an attribute of all or most computers. If so, the designers of many of those future systems will no doubt be indebted to the current pioneering systems. □

An Approach to Software Fault Tolerance

The Tolerant Systems' approach to software fault tolerance is based on the recognition that it is the tolerance to failure of the *transaction* that is important in a commercial environment. This recognition contrasts with design approaches whose primary goal is to support fault-tolerant computer system processes. In these latter approaches, significant system resources are expended in creating and maintaining shadow or backup processes whose state must be periodically updated based on primary process activity. In addition to the system throughput and necessary space penalties incurred in such systems, additional programming complexities are necessary which may sometimes decrease programmer productivity and increase application programming errors.

The Tolerant Systems design takes as its starting point the assertion that the "permanent" data in the system (the data resident in files, tables, etc. on the disk) represents the state of a company's business (or part of the business) and that it is this data which must at all times be, from an external viewpoint, consistent and correct. This data goes from one consistent state to another as a result of being manipulated in transaction. The business transaction must be guaranteed (by the system) to complete successfully even if a failure occurs in the system while the transaction is active. Note that a transaction that only reads data still stays in the general model—in this case the ending consistent state is identical to the beginning consistent state.

To guarantee fault tolerance of a transaction, the Tolerant system automatically performs a number of functions transparently to both the terminal and the programmer.

The communciations management system maintains an input log which is used to record all input to the transaction. In addition, the log is used to record each occurrence of transaction output (although not the actual output data). The log is transparently duplexed by the file management system to protect against failures.

The file/database management system maintains "before images" of all pages of data which are updated by the transaction. In addition to providing the file system/database transaction rollback facility (used in the event of a failure), the before images also facilitate an optimal level of multi-transaction concurrency by providing consistent views of the data for read transactions despite the concurrent existence of update transactions. This is a significant side benefit, as in most commercial environments the frequency of read-only transactions is much higher than that of update transactions.

Tolerant's Transaction Executive (an integral part of the operating system) maintains the state of execution environment by recording process state information. The information maintained defines a process in terms of its initial state and which transaction is currently being served by each process.

In the event of a failure, the system performs the following actions:

(1) The Transaction Executive identifies which transactions and which processes have been affected. The communications system and the file/database management system are informed of the identified transactions.

(2) The Transaction Executive recreates failed processes on a different System Building Block (this is only necessary if the failure took a System Building Block out of commission). The re-instituted processes are reconnected to their logical I/O channels.

(3) The file/database management system rolls back the affected transactions to their start points by use of the before images.

(4) The communications system initiates system re-execution of the affected transactions by reading the transaction input log. Output generated by the re-executing transactions is discarded up until the previous point of failure.

The rollback and re-execution of transactions is accomplished transparently to the terminal user. Through a brief degradation in system performance may be noticed.

Whenever a transaction ends (commits), the communication system cleans out the related information from the input log while the file/database management system, having applied data updates at the commit point clears out the related before images. Both these operations facilitate optimal space management.

It should be noticed that the mechanism described above can be built on to provide transaction rollback and re-execution from an intermediate waypoint in a transaction; this is useful in the case of lengthy transactions.

In summary, the Tolerant Systems approach to software fault tolerance is based on the concept of a business transaction and provides a transparent (to user and programmer) solution that requires no non-productive backup hardware and uses minimal system resources.

Eli Alon, President, Tolerant Systems, 81 East Daggett Drive, San Jose, CA 95134. **Write 338**

What you don't know about your DEC* computer can't help you.

DEXPO® West 83 can.

400 Reasons to Attend
Wouldn't you like to get just a little more out of your DEC* system? All it takes these days are the right DEC-compatibles. And you'll find them by the thousands at **DEXPO West 83.** Your most complete DEC-compatible resource.

Want *more* reasons? How about *more* compatible software, *more* compatible hardware, and *more* compatible services? **DEXPO West** features nearly 400 vendors with more for every DEC computer. Personals. Micros. Minis. Mainframes. All the latest DEC-compatibles designed to make your information systems work a little harder. And a lot smarter.

*DEC and DECUS are registered trademarks of Digital Equipment Corp.

Attending DECUS*?
Then, DEXPO is Free
If you're planning to be in Las Vegas for the DECUS meetings, make sure **DEXPO West** is on your schedule for Sunday . . . before the meetings start. Of course, you'll probably want to come back on Monday, Tuesday and Wednesday, too. So be sure to use our five-minute shuttle bus services. It's free. And so is the Show when you bring your DECUS badge.

Plus 60 In-Depth Sessions on How to Put the Latest DEC-Compatibles to Work

DEXPO® West 83

The Fourth National
DEC-Compatible Industry Exposition

Las Vegas Convention Center
October 23-26, 1983
Sunday-Wednesday

For more information, mail the attached reply card. Or, contact Expoconsul International, Inc., Dept. D-3, 55 Princeton-Hightstown Road, Princeton Junction, NJ 08550; Tel: 609-799-1661.

Self-Testing Components Pinpoint Network Faults

Despite increasing product complexity, μPs have provided the methodology for vendors to develop improved test capabilities for products.

by Joe Veni

There are a variety of reasons why sophisticated diagnostics are being designed into an increasing number of products. First, multi-vendor networks have burdened network managers with the responsibility of isolating problems to the precise network component before calling for service. (See **Figure 1**). On-site vendor service and down time is very expensive, therefore, accurate problem isolation is very important. The geographical nature of networks themselves further frustrates solving network problems. Attempting to resolve problems at remote sites can be extremely difficult. As a result, remote terminal users are frequently called upon to assist the computer center in diagnosing problems.

Second, vendors can reduce their field service costs by designing automated self-testing routines into their equipment. Self-testing techniques can provide fault isolation down to a board, and in some cases, component level. Typically, repairs can be performed over the phone, eliminating costly dispatches to customer locations.

Third, the growing use of μP technology is dominating the movement towards incorporating extensive diagnostic abilities in data network products. Despite increasing product complexity, μPs have provided the methodology for vendors to develop improved test capabilities for their products.

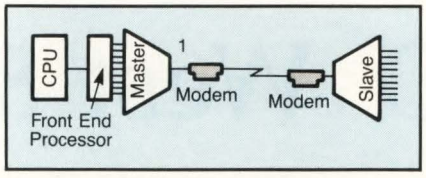


Figure 1: Each of the network elements may be supplied by a different vendor.

Fourth, the increasing scarcity and high cost of technical personnel has influenced diagnostic procedures. Automatic and user-friendly testing procedures have lessened the need for highly technical personnel, a big help for solving problems at remote network sites staffed only with non-technical personnel.

Diagnostics fall into two basic categories: internal (or self-testing) and network. In μP-based systems such as statistical multiplexers, self-testing is very common. Self-tests usually only occur during the period known as initialization, that is, after either a power-on of the unit or a re-start or re-set command has been given. During initialization a separate software routine, stored in what's known as "shadow PROM," is activated. Shadow PROM is responsible for performing the test of the hardware and software and, once completed, is not part of the normal operating system.

The amount of hardware and software tested in a system varies from one manufacturer to another. Generally, all software and 50% to 90% of the hardware is verified. In some cases, tests that verify external network components are also used.

Test Methodology

The technology behind self-testing is basically standard throughout the industry. Acting upon commands from the "shadow PROM," operating software residing in normal PROM is verified by performing a cyclic redundancy check (CRC). The philosophy behind CRC testing is that as the system operating

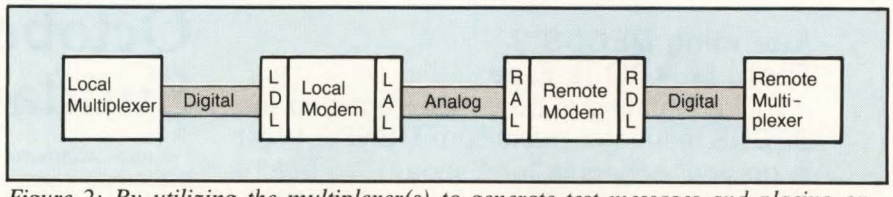


Figure 2: By utilizing the multiplexer(s) to generate test messages and placing or commanding loopbacks at various points on the link, link problems can be isolated without the use of external test gear.

Joe Veni is National Field Engineering Manager at Halcyon Communications, Inc., 2121 Zanker Road, San Jose, CA 95131

software is read, certain bits in each byte are added. Then, the sum is compared in a hexadecimal format to a pre-programmed value.

For example, if after reading the operating software, the check sum of all the pre-selected bits that were in the on (or logic 1) state is equal to hexadecimal C7FF, then C7FF must appear in the shadow PROM. If these values don't match, an error is assumed. These errors are commonly called CRC errors.

Verifying dynamic and static RAM (random access memory) is accomplished by writing into memory and reading the data back. All bits in RAM are exercised by writing in varying data patterns such as alternating hexadecimal value 55 and AA or "walking patterns." These test patterns check for any stuck memory bits and can also be used to verify addresses in memory.

Once all PROM and RAM tests are completed, additional hardware can be tested. In a statistical multiplexer, all I/O ports and links are verified through loopback tests.

Upon completion of all self-tests, the initialization procedure is terminated and usually a system status is displayed on the front panel, either in the form of LEDs, alpha-numeric displays or both.

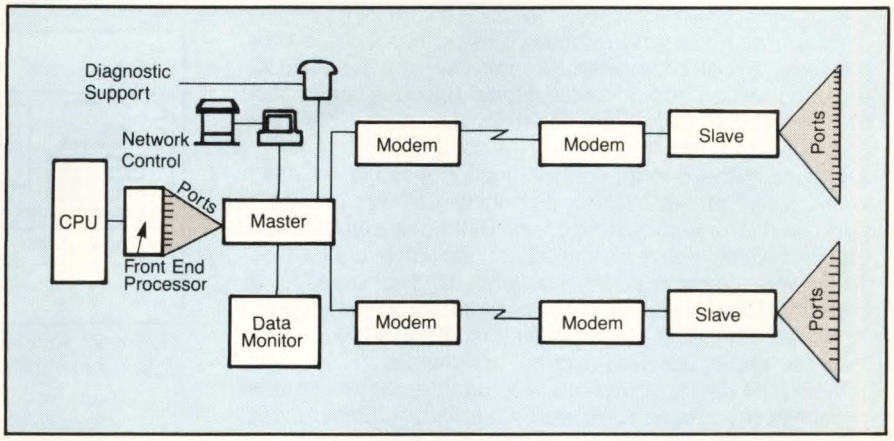


Figure 3: A network system with network control options. Centralized testing, statistics reporting, configuring of all links, I/O ports and system parameters on the master and slave nodes are possible.

Network Diagnostics

Network diagnostic capabilities can vary from basic LED status indication to more complex alpha-nu-

SMD Remote Control Testing

Multi-megabyte, hard disk drive subsystems require periodic maintenance to ensure proper computer system performance. One reason for computer system sensitivity to disk drive performance is that a vast amount of data is stored in the drives and must be virtually error-free.

One solution is to employ an engineer at a central location to control and monitor testing, using the telephone lines as a communications link to the drive under test. This requires a disk tester at the drive location and some means for accessing the test unit via the telephone lines. It also requires a test unit with the capability to operate under either local or remote control.

This remote control approach was demonstrated for the first time at the recent Comdex Show in Atlanta, GA. An 80 Mbyte Winchester drive in Atlanta was controlled, tested, exercised and monitored by an engineer in Santa Monica, CA. Western Electric recently conducted tests to simulate a similar application over a shorter range within their own company. In this case, a single engineer controlled testing of all drives within the immediate vicinity.

Available as an option, the remotely-controlled maintenance system is a part of the Pioneer Research PM-4000 Qualifier™ (**Figure 1**), which is a portable, intelligent test system for SMD (Storage Module Drive) interface disk drives. It contains "canned" error diagnostics that include self-test, sequential read, sequential write then read, random seek and read, butterfly seek, and others. In addition, it may be single-stepped, is operator-programmable, and can test any drive size or configuration. Hard and soft error

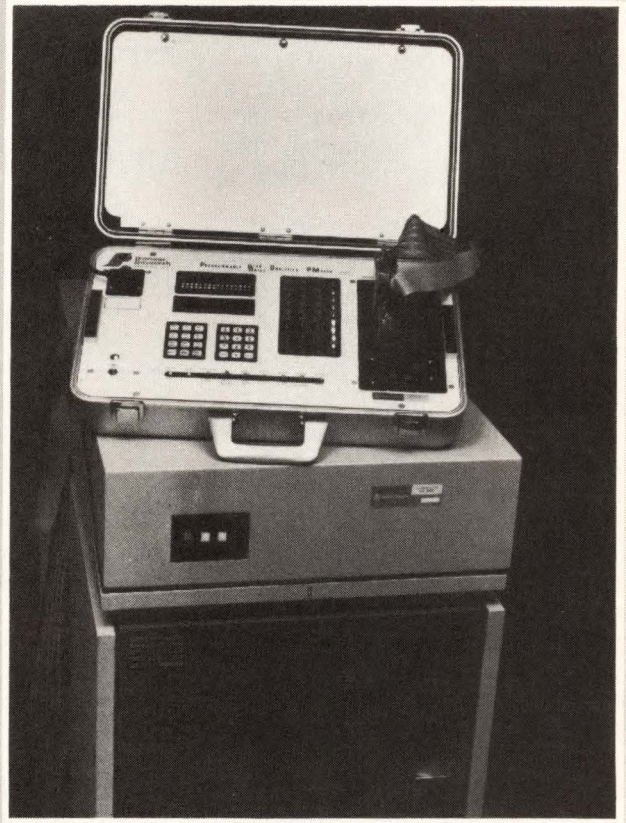


Figure 1: Pioneer Research PM4000 Disk Drive Qualifier.

detection and checking of specific track, head and sector problems are also provided through use of a 32-bit ECC (error correction code). An additional option is automatic, precision head alignment capability for removable disk pack drives.

Originally, the remote control function was not included in the design of the Qualifier. Its original use was only as a portable instrument developed for Bell Labs and Western Electric, which could be carried to the drive under test. Tests were controlled and monitored by two keypads, a group of toggle switches, a 16-character LED alphanumeric display and LED status indicators. An RS-232C interface allowed its use with external peripherals.

When the decision was made to add the remote control capability, the ground rules were that the circuit board was to remain as is and hardware changes were to be kept to a minimum. Another design consideration was that a "dumb" CRT terminal would communicate with the Qualifier via a modem and telephone lines. The CRT terminal was to provide the same control and display functions performed by the switches and LED displays on the existing system.

In the ensuing design enhancement, it was necessary to go from 2716 (2K×8) to 2732 (4K×8) EPROMs to accommodate the additional firmware requirements. The only hardware, however, that had to be added was an audible alarm buzzer and a counter IC to provide the standard choice of jumper-selectable baud rates.

A block diagram of the Qualifier system with remote control is shown in **Figure 2.** The RS-232C interface on the Qualifier is connected to an acoustic coupler or modem; a CRT terminal with a second coupler/modem provides the remote control and display functions.

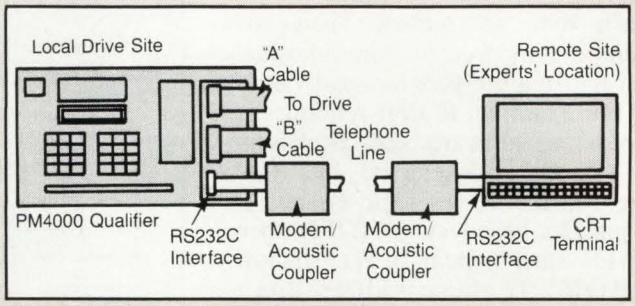


Figure 2: Remote control unit allows expert maintenance person to control and monitor testing of SMD drive.

One of the planned enhancements of this test system is the ability to accommodate additional disk drive interfaces. This would allow the instrument to work with the various other interfaces that are now being used, such as the small Winchester versions.

Another possibility for future disk drive testers is increased test capability. Additional features will be made possible primarily by the rapid advancement in semiconductor technology that continues to provide higher capacity EPROMs and RAM. **Write 325**

Sol Gindoff is President of Pioneer Research Inc., 1745 Berkeley Street, Santa Monica, CA 90404

meric displays and menu-driven testing formats. For example, a simple LED indication on a modem can advise a technician that carrier is lost and the facility is suspect.

Most modems also have loopback functions available which can further isolate problems. In addition, some modems have loopback functions that allow for the tying of transmit and receive data paths together, analog or digital, at the local or remote modem. (See **Figure 2.**) Further, some modems also use telemetry schemes to permit a local modem to command a loopback from a remote modem, which allows testing of unattended locations. However, to properly test facilities and modems, or if a problem develops outside the realm of the modems or facility, other network components (i.e. statistical multiplexers) must be called upon for assistance.

Link-testing is usually performed via a "fox-test" message generated by one or both ends. When both ends are generating the test message they in turn compare and analyze the message received to verify that there are no errors present. If end-to-end continuity is not present, one end must perform the test which requires a loopback at various points in the circuit. By using the modems to move the loopback through the network, a problem on the link can be quickly isolated. It is important to note these tests remove the link from service and are performed only if the link has already failed or is suspected of having problems.

Self-testing is a critical requirement for today's data communications system.

I/O port testing is available in most statistical multiplexers to assist in resolving individual user problems. Most networking systems allow for normal loopback testing of individual ports and can also generate fox-test messages out to a terminal or printer to further assist in problem solving. Thus testing of either a local or remote port is possible.

Many multiplexers also enable an end-user to perform an I/O loopback test from his own terminal. A pre-selected control character sent from the terminal allows the operator to enter a simple menu providing access to local or remote port loopbacks. In effect, an operator who has lost communication can quickly verify his terminal and/or his circuit to the remote end of the network before reporting a problem to the computer center.

Data Monitoring

Monitoring traffic data is another helpful diagnostic method for resolving individual-user line problems. Most technical control or

computer centers are equipped with data analyzers/monitor which are usually patched into a circuit via an RS-232 or similar patchfield. Data can be monitored in an active or passive mode. In the active mode the data analyzer emulates a specific end of the circuit. Some statistical multiplexers will allow monitoring of the I/O ports internally via a dedicated monitor port.

If a data monitor is used that has auto-monitoring capabilities, no hands-on re-adjusting of the data monitor is required, regardless of what type of traffic protocol is monitored, even synchronous. Auto-monitors can automatically detect the protocol, speed, bits per character and parity of the traffic on the port.

Sophisticated data systems allow for the retrieval of various network statistics. Link or port problems are frequently intermittent in nature and very hard to detect. Statistics provided by a statistical multiplexer, however, will usually help locate such problems.

These systems also have network control options which allow for complete system operation, diagnostics and statistics monitoring from a single location via a CRT, printer and a dial-up modem. (See **Figure 3**).

Conclusion

Data networks will continue to grow in number, size and complexity. Accordingly, vendors will continue to produce products that will facilitate the management of those networks. Network improvements must still be made in areas such as facility problem solving, remote dial-up diagnostic support, down line loading of software, and testing between networks and network internal layers.

Self-testing, network testing and statistics reporting are critical requirements for today's data communications system. Network products, such as statistical multiplexers, are helping to provide these features. Through these features, network down time, technical manpower and maintenance costs can be kept in line to satisfy users and management. □

Self Diagnosis of Single-Chip Computers

by Bill Huston

A key answer to the testing dilemma is to use the on-chip processor to test itself and the rest of the part.

A relatively simple computer can test the functionality of SSI, MSI and VLSI memory and peripherals. But with a single-chip microcomputer, an external test computer must exercise the on-chip processor, RAM, ROM, I/O ports, timers, and other peripheral functions. A key answer to the testing dilemma is to use the on-chip processor to test itself and the rest of the part. The M6805 family of μCs includes a diagnostic program that checks all major elements of the chip.

On-Chip Self-Check Routines

The self-check ROM is included in the address map of the processor, but is not included in the user programmed ROM. When a part is said to have 1 or 2 Kbytes of ROM, it is all available to the user. The 100 to 200 bytes of self-check area is in addition to the user ROM. **Figure 1** summarizes the flow of the self-check program for one particular single-chip, the MC6805R2. One section of the IC is tested at a time, and when all checks pass, the program starts over again. Some port output pins show the test mode of the IC. A continuous flashing of an LED connected to a port pin, for example bit 2 of port C in the case of the '05R2, indicates repeated successful running of the self-check program.

The I/O pins are checked as inputs for high and low levels, and as outputs for high and low levels. The checking is done by looping output port pins back into input pins. The program puts a binary pattern on the outputs and looks for the same pattern on the expected input pins. The one/zero pattern is reversed and checked again. Then the data direction bits are reversed to change inputs to outputs and vice-versa. The two binary patterns are repeated with the reversed data direction.

The timer self-check routine uses the on-chip oscillator to determine that the prescaler and the counter are dividing in a binary sequence.

The on-chip RAM is checked with a 'walking ones' pattern, which is written and then read from each byte. All RAM is written as a block then verified as a block. The

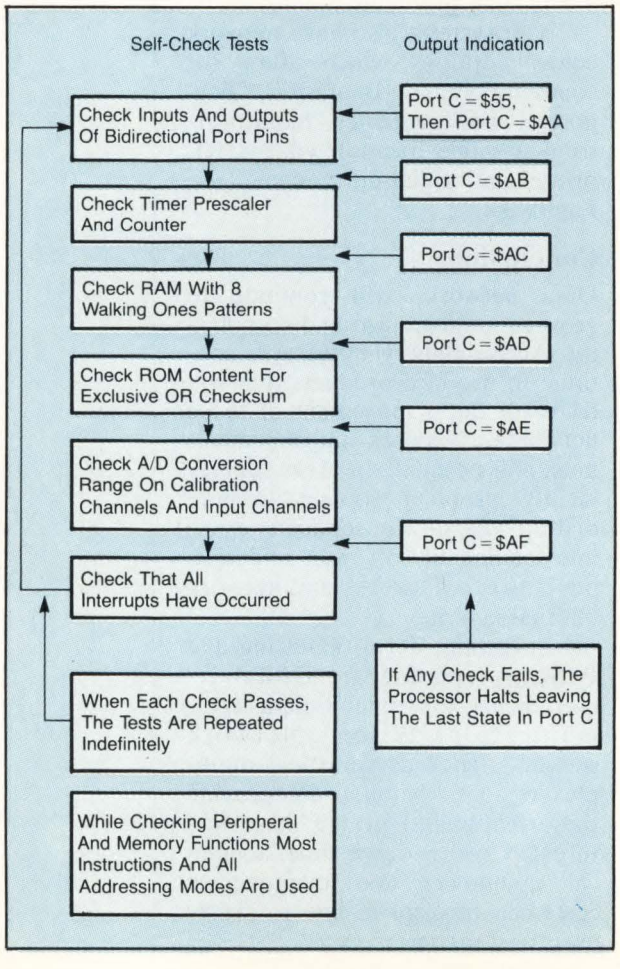


Figure 1: The diagnostic self-check program included on the M6805 family of single-chips checks functional operation of all major on-chip functions.

Bill Huston is Applications Engineering Manager for Single-Chip Microcomputers with Motorola Inc., 3501 Ed Bluestein Boulevard, Austin, TX 78721.

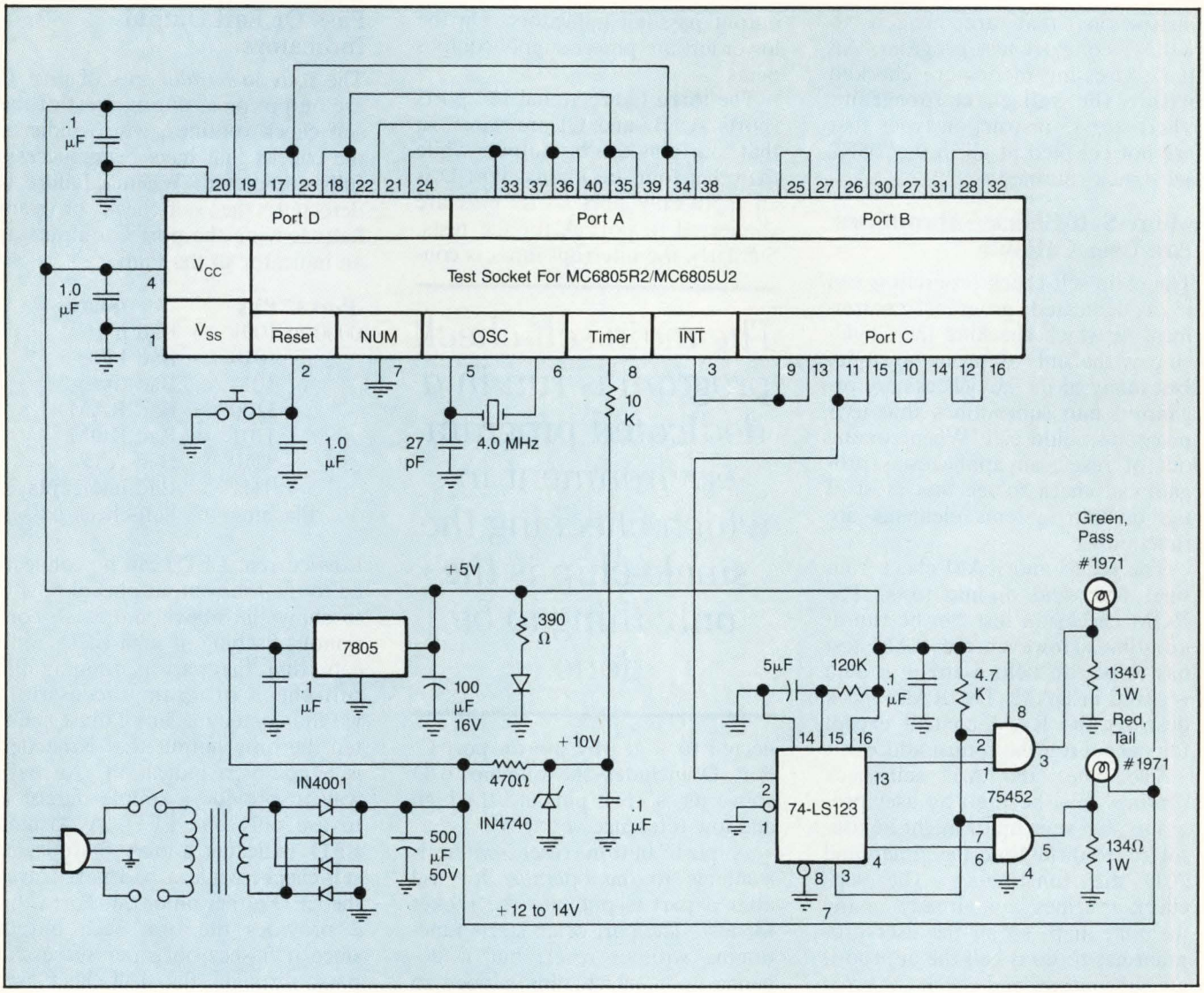


Figure 2: A self-contained self-check unit includes a socket to insert the single-chip under test, circuitry to drive results indicators, and power supply components.

test is repeated 8 times with different patterns to try the walking one in each bit position.

The content of the ROM is not directly verifiable since it contains a unique customer program. The self-check routine reads each ROM byte and calculates a checksum. The self-check ROM includes the vertical parity byte that allows the checksum to come out even.

The MC6805R2 single-chip includes an A/D converter, which is also tested with a self-check routine. Analog conversions from all input channels are compared to expected values with a margin for tolerance. The A/D includes special channels that allow the test to confirm the high and low references voltages, as well as some intermediate points.

While running the I/O, timer, and A/D checks, all interrupt conditions are initiated. Thus, the last step in **Figure 1** is to enable interrupts and confirm that each interrupt condition is received. When the interrupts are successfully checked, the test sequence is started over again.

There is less than 200 bytes of self-check ROM, so there is not enough space to include a complete instruction set diagnostic. If the ROM area devoted to self-check were doubled, the diminishing returns point is at the stage where only 1 or 2% more bad parts would be detected.

While running the other system checks, the program uses as many different instructions as possible to confirm successful operation of the processor. For that reason, the listing for the self-check program is not a good example of M6805 family programming. Some instruction usage is obtuse when testing different op codes.

The entire '05R2 self-check program is only 93 instructions long. But in that short program, 38 different op codes are used, impressive when considering all of the loads, subroutine calls, subroutine returns, and branch if not equals

instructions that are needed to write a compact test program. All ten addressing modes are checked within the self-check program. There are 13 instruction types that are not checked at all in the '05R2 self-check routines.

Many Self-Check Subroutines Are User Callable

The main self-check program is run in a dedicated program environment in which checking the single-chip is the only thing to be done. But many of the key checks are organized into subroutines that user programs could call. When coming out of reset, an applications progam can check to see that most of the on-chip systems elements are functioning.

The ROM and RAM check routines are valid on-line tests. The ROM checksum test can be run at any time. However, the RAM test has to be run before any user data is saved in RAM. The RAM check destroys the RAM content except for the subroutine return address.

The timer and A/D self-check routines may be used by user programs. On start up, it might be useful to confirm that the timer and A/D are functioning. The self-check routines are already in the memory map, so all the user program has to do is call the appropriate subroutines and check the error flag on subroutine exit.

The I/O port self-check routine, however, is not user callable. The I/O check assumes that the port pins are tied back to each other, which can not occur in a real application. So the start up of an application program would need to devise a way to check the ports for functionality based on the actual system connections.

A Self-Contained Self-Check Unit

The schematic in **Figure 2** illustrates a fully self-contained IC test computer. The circuitry can be built into a small enclosure. The test unit has three parts. The upper portion is the test socket, zero insertion type, where the single-chip computer is plugged in. The lower right portion is circuitry to drive output pass/fail indicators. On the lower left are power supply components.

The three bidirectional I/O ports (ports A, B, and C) are wired so that four pins can be outputs while the other four are inputs. Port D is an input-only port so its pins are connected to port A for the tests. Similarly, the interrupt input is connected to a nearby pin on port C. Port D includes the on-chip A/D converter, so two pins are the high and low reference voltages.

The main self-check program is run in a dedicated program environment in which checking the single-chip is the only thing to be done.

A push button reset switch is available to the operator for use after a part is put into the socket for test. The part often starts functioning without reset, but it depends upon which pins happen to connect first as the part is being plugged in.

The oscillator pins in the self-check unit should be configured the same as those in the end product. If the mask option on the IC has been selected for the RC time constant oscillator, the crystal components shown in the schematic should be changed. The self-check mode is selected with the MC6805R2 by putting a voltage between 9V and 12V on the timer input pin. **Figure 2** shows a pull up resistor from the timer pin to a 10V source. When the timer pin is at Vcc (5V) or below as the part comes out of reset (the RESET pin rises to 5V) the processor uses the normal reset vector to start the applications program. The special self-check vector is used instead when the timer input is above 9V at reset.

Pass Or Fail Output Indicators

The four low order bits of port C are output pins, during most of the self check routines, which indicate the checks that have been successfully completed. When a failure is detected, the self-check program halts leaving the port C outputs as an indicator of the fault:

Port C Bits	Status
0000 to 1001	Bad part
1010	Bad I/O
1011	Bad timer
1100	Bad RAM
1101	Bad ROM
1110	Bad A/D
1111	Bad interrupts
Flashing	Self-check passes

Low current LEDs can be connected to the four output pins of port C to show the above status. A continuous flashing of such LEDs indicate that the part is running the self-check program successfully without detecting any failures. Often the only output that is needed is a go/no-go indication. An easy way to provide a simple output is to use only one LED. A flashing LED indicates a part that passes self-check, while a bad part leaves the LED either on or off. Port C bit 2 provides the best such output since it flashes once per successful pass through the self-check sequence.

The schematic in the lower right portion of **Figure 2** makes the output indication even more straightforward. A green light is used to indicate that self-check is running successfully and a red light indicates a bad part.

A retriggerable one-shot, a 74LS123 in this case, is hooked up to convert the flashing status on port C bit 2 into a steady pass/fail indication. At the output of the one-shot, red and green LEDs could be driven. But, bright pilot lights provide a much more visible output. A high current driving IC such as the 75452 can drive a ¼A light bulb.

A self-check unit can easily be used as a quick screening test in production. As the end product is being assembled, each single-chip

IC can be put into the self-check unit before being inserted into the PC board. As with any high density IC, it is recommended that the assembly operator use a grounded wrist strap when handling the ICs. The power supply portion of **Figure 2** is conventional. A 5V source is needed for the single-chip under test, plus the one-shot and lamp driving ICs. A low current source of 10 or 11V is needed to select the self-check mode in the single-chip. An unregulated 12 to 14V is used with the lamps to allow brighter more attention getting lights. An LED is included to show that power is turned on.

Circuit Adjustments

If the circuit were to be mass produced, its detailed design might be different. For example, the analog one-shot could be replaced by a digital equivalent to assure repeatability.

First, the transformer should be selected to provide 12 to 14V at the unregulated output. A higher voltage shortens the life of the lamps and a lower voltage leaves the lights dim.

Then, before connecting the self-check output signal to the one-shot, the self-check time should be measured for the frequency of the single-chip oscillator in use. The time constant components (R and C) on the one-shot should then be selected to be 50% or more slower than the self-check cycle time. The one-shot time should expire only if the self-check program is not cycling. Once the one-shot time is properly adjusted, the retriggerable input can be connected to the single-chip output.

The last adjustment to be done before plugging in the lamp driver IC is to the lamp resistors. The high wattage resistor from the lamp to ground is selected to keep the lamp filament warm when the light is turned off. A cold light bulb draws a great deal of current when first turned on, which can damage the driver. A resistor value is chosen which keeps the filament to barely glowing. Two 67Ω 1W resistors worked fine with the #1891 bulbs used.

The cost of switching is not much different than the cost of building another unit.

Adapting For Other Single-Chips

The self-check unit described above is specifically for the MC6805R2, but the circuit is easily adapted to other versions of the family. All mask ROM single-chips in the M6805 family have on-chip self-check features very similar to that of the '05R2.

The wiring of the socket in the upper portion of **Figure 2** is in most cases at least somewhat different for each family version, and individual data sheets show the required connections. It is tempting to wire a self-check unit that can be switched to test a number of different versions. But there are some good reasons to consider constructing separate units for each single-chip type to be tested.

First, since the self-check units are low cost items, the cost of switching is not much different than the cost of building another unit. Secondly, switches that have to be in the right position introduce human errors that can cause good parts to test bad. So the risk of failing good parts, as well as the time lost discovering them, seems to outweigh the small added cost of an additional self-check unit.

The other adaptation needed to use the self-check circuit for other '05 family single-chips is to adjust the one-shot time constant. Versions of the family have different self-check cycle times. The R and C component values in **Figure 2** may, however, need to be somewhat different. □

Unix* Leads To Greater Flexibility

by Richard Churchill

Software development groups face several hard decisions when addressing the purchase of a development system. Most notable are choice of a vendor and size of the system. Does one opt for the expensive larger system that will permit growth for a reasonable period of time, or select the system that serves the organization's current needs and matches its financial capabilities?

Compatibility issues among systems from the same vendor are often difficult to resolve; compatibility issues among different vendors may be nearly impossible. A commitment to Unix as the development operating system environment dramatically reduces the impact (both administratively and financially) of the hardware vendor decision.

Expandability

Unix is an operating system developed for internal use at Bell Laboratories (Murray Hill, NJ) as a result of the frustrations and lack of flexibility in the (then) commercially available operating systems. Many of these original shortcomings have been addressed in one fashion or another by contemporary operating systems. None the less, satisfying the needs of a software development organization has been the hallmark of the Unix system and solutions of those needs have been continually expanded upon by Bell, and in recent years, by academic and commercial organizations.

Unix will allow an organization to purchase a machine to meet its immediate and short term needs and to later purchase additional systems to "increase" the original system's capabilities. Regardless of the size of the original system, additional systems of any size are easily networked together to provide flexibility across machine boundaries. Crossing boundaries of hardware vendors is also possible with Unix because the user interface and operation has a high probability of consistency. Also, much of the software developed on a Unix system is portable to other hardware.

Use of a Unix operating system allows a software development group to expand easily.

Communications Capability

The communications package distributed with Unix is generally known as UUCP. UUCP, Unix to Unix CoPy, is also one of the communications commands included in the package, along with CU (Call Unix) and UUX (Unix to Unix eXecute).

UUCP is serial data communications, the speed can be specified, and it works over modem and hardwired links. System networking consists of a single RS232 line between systems. This will allow one system to act as Master and initiate a session between the two systems. Two-way communication is accomplished when the Master completes all queued requests, and the Slave system assumes the Master role and executes all queued requests for the original Master (if there are any).

If it is desirable to have each system initiate sessions, then two serial lines need to exist with each line having a Master. Clearly, serial lines can be saved if modems and telco lines are utilized, since a Master can dial any slave system with only one modem link, whereas a separate line must be run for each hardwire link to a slave system.

The UUCP command executes in a batch mode environment. The user invokes the UUCP command specifying another system (by name) which will be party to the session and naming the source and destination files for the UUCP process to use. Interestingly, the UUCP command is capable of calling another system and retrieving file(s) from that system as well as transferring files to that system. For instance:

uucp blue!file1 red!afile

is the command string to copy file1 which resides on blue system and transfer it to another system (red in this case) and rename it "afile" on the other system (**Figure 1**). Reversing the order of blue! and red! would cause blue system to call red system and retrieve a file named "afile" and place it on blue.

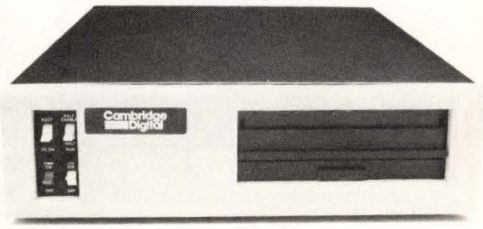
Both systems need to "know" the other system and the UUCP user must have log-in and appropriate read/write privileges on the other system. While UUCP allows entry into another system, access and security within the UUCP framework are as good as for any other Unix user. UUCP on the slave system logs in the Master system as would any system user and the Master system must pass the security checks of UUCP on the Slave system. Beyond that, the files specified in the

---

* *Unix is a trademark of Bell Laboratories.*

Richard Churchill is VP Software Division, Cambridge Digital, PO Box 568, 65 Bent St., Cambridge, MA 02139.

SOMETIMES, THE BEST PLACE TO GET A DEC PDP-11 SYSTEM ISN'T DEC



When you buy DEC PDP-11 based System 58 from Cambridge Digital, it's ready to get to work as soon as you hook it up. Because at Cambridge Digital, we sell enhanced-performance DEC systems that are fully integrated with DEC-compatible products. Products you can't buy from DEC. So you spend your time working on your system, instead of just trying to make it work. It's part of the edge you get when you buy from Cambridge Digital.

Take our ready-to-run System 58. It features a DEC LSI-11/02, 21, or 23 with internal RAM memory of 32Kb, expandable to 4Mb. The 11/23 based system directly addresses up to 4Mb of memory. Plus you get an RLV12 compatible Winchester disk with you choice of 10, 20 or 40Mb, and a floppy with usable capacity of 1.02Mb.

And, you get a full range of development tools from CDS, too. Like a fully-supported and enhanced operating system based upon UNIX* System III. Also TSX-Plus, RT-11, μ-power PASCAL, and RSX-11M.

It's all ready to run. Available for as little as $7,350. Available in as little as 10 days. But its not available from DEC, so call Cambridge Digital, instead, and get The Edge.

For more information on our System 58 and a copy of our Building Blocks For Systems Catalog, including a description of the seven guarantees you get when you get The Edge, call or write.

Main Office Dept. 7400, P.O. Box 568, 65 Bent Street, Cambridge, Massachusetts 02139. Telex 92-1401/ COMPUMART CAM 800-343-5504 In Massachusetts 617-491-2700

New York District Office 516-935-3111

*UNIX is a trademark of Bell Laboratories.

I want The Edge:

Name_____ Title_____

Organization/Company_____

Address_____

City_____ State/Province_____

Zip/Postal Code_____ Country_____

Phone No. ( )_____

My main product interests are: DEC ☐ NCR ☐

(7400) 58

Cambridge Digital

DIVISION OF COMPUMART

The Edge in System Integration

800-343-5504

In Massachusetts call 617-491-2700

Write 36 on Reader Inquiry Card

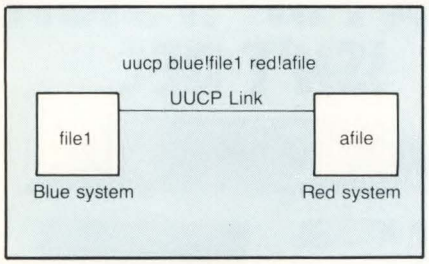


Figure 1: Simple UUCP link.

UUCP command string (and the directories they reside in) must all have access privileges set which allow the copy process to proceed. This means that even though two systems may be linked and have passed the UUCP log-in requirements, the UUCP user must have the privilege to access the requested file or the command will terminate.

As an administrative example of this usage, one of the UUCP setup files allows a time of day, day of week entry for the Master system to place calls to the Slave system. A software developer could set the time of day for 5–6 a.m. to call the administrative (Slave) system. A UUCP command to transfer certain source files to that machine would be invoked by the developer. Regardless of the time of day the command is invoked, it would be queued by the Master system until 5 a.m. Then the developer's system would call the administrative system and transfer the files, making for painless backups. Of course this can be carried even further by specifying to AT (another Unix command) that the UUCP command string be executed once a day at a particular time, say 5 a.m. Now the developer wouldn't have to remember to type the UUCP command each day; the system would automatically execute the command in his behalf.

Alternatively, the administrator's system could be the Master and call the developer's system at 5 a.m. Presuming the administrator's system didn't have any UUCP commands queued, the developer's system would be given the opportunity to become the Master and execute its queued UUCP commands (because it could never call out, the system simply queues all UUCP commands and waits for that system to call in). The result is the same as previously described: the developer's files would be copied to the administrator's system each day. In essence, the administrator's system polled the development system at 5 a.m. Thus, in an environment where there are several project-oriented Unix systems, a single administrative system could poll each project system to get specific file back-ups or to send files to each. If the project systems were linked to only the administrative system, files could be passed from one project system to another via the administrative system.

Another UUCP example would be writing specifications, status reports, and other documentation for the software. Files can be created on any system and forwarded to any other system via the UUCP command. This creates the big timesharing system feeling with small, project-oriented, system hardware. The system manager could be the administration system where all specifications, status, documentation, and source is maintained. This becomes a manageable task using Unix.

UUX Command

The UUX command offers even more flexibility than UUCP to the Unix user. This command is a batch mode command like UUCP; however, UUX allows execution of any valid Unix command on another system. Here again more than one system may be a part of the single UUX command. For instance, consider the following:

uux "blue!diff red!/demo green!/
demo › blue!nomatch"

This UUX command (**Figure 2**) involves three systems; blue, red, and green. The Unix command "diff" (located on the blue system) is to be executed. The "diff" Unix command compares two files and directs the result to the standard output device. In this UUX situation, one of the files is located on the red system and is known as demo; the other file is located on the green system and is known as demo. The output file containing the differences between these two files is redirected via the '›' character to a file known as nomatch on the blue system. As with the UUCP explanation, the systems can be changed around to place the results on even a fourth system or to compare a blue file with another system's file, etc.

UUX places the power of Unix commands within the whole network of Unix systems. However, it is still a batch mode command and execution occurs without the user participating in the process. While the capability of UUCP and UUX is wide, there are still many occasions where an interactive session between two systems is required.

CU Command

CU is an interactive command which causes the user's system to place a call to the specified Unix

Continued on p. 106

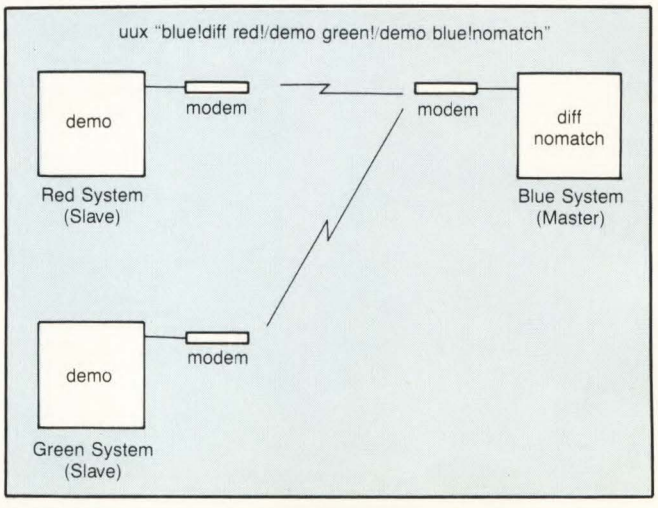
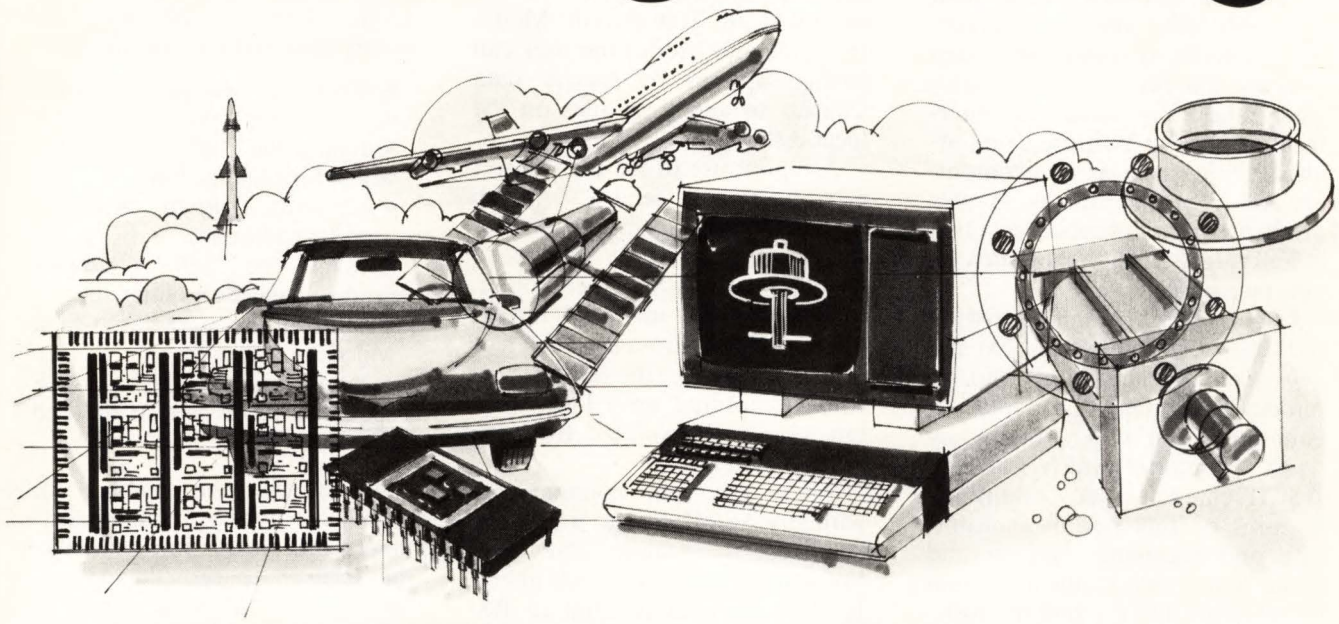


Figure 2: Departmental configuration involving three systems.

Keep up with CAD Engineering



CADCON™ EAST 83

COMPUTER-AIDED DESIGN ENGINEERING CONFERENCE

Park Plaza Hotel & Expositions Center
Boston, MA
October 11-12, 1983

The Only East Coast Conference and Exposition Dedicated to Computer-Aided Design Engineering for All Industries

Computer-aided engineering is generally recognized as one of the most vital and fastest growing technologies of the '80s. By the end of the decade it has been estimated that at least 1 out of every 5 engineers will be applying CAD routinely in everyday operations.

If you're involved with design, analysis, modeling, simulation, process control, productivity, geometrics, automated drafting and plotting in such industries as electronics, architecture, maritine, geology, meteorology, electrical, mechanics, hydraulics, machine tool, automotive, construction . . . and the list goes on and on, the CADCON Conference is a must attend event.

Technical Program – A wide ranging and comprehensive series of 6 Sessions consisting of 24 papers; 2 Workshops; 2 Minicourses; 2 Professional Advancement Courses; and 13 Commercial Clinics. The Technical program is chaired by the internationally recognized computer graphics expert Carl Machover, President of Machover Associates. Emphasis will be on application, user's views and current issues that need to be addressed in CAD.

Exhibits – See, compare, evaluate CAD equipment, software, methods and services of the nation's leading suppliers.
• Computer Systems • Disk Drives/Systems • Memory Devices/ Controllers • Digitizers • Test Equipment • Software/Software Development Systems • Compatible Peripherals • Factory Management Systems • Printers and Plotters • Inspection.

Keynote Address and Luncheon – James Berrett, President and CEO of Computervision will speak on "Migration and the Future of Computerized Technologies."

I am interested in attending CADCON East '83

Please send more information on the:
☐ Technical Program ☐ Exhibition

Complete and mail this coupon to:

CADCON East '83
Conference Registrar
Morgan-Grampian Expositions Group
Two Park Avenue
New York, New York 10016
Or call: (212) 340-9780

Name _____
Title _____
Company _____
Address _____
City/State/Zip _____
Telephone ( ) _____
Date _____

Communication Software Ties Development Systems to Minis

With the increasing size and complexity of software being built into embedded μPs, it is becoming apparent to many embedded systems builders that the hardware laboratory needs an interface to general purpose computing facilities such as minicomputers and even mainframes. A new product from Intermetrics, Inc. (Cambridge, MA) makes such an interface possible.

Called "Talk," this software package turns Intel series 200 and 300 development stations into interactive terminals capable of communication with virtually any "host" computer which uses the ASCII character set. Additional features of Talk permit transmitting and receiving data to and from local development system floppy disks and the remote host.

The Talk utility is implemented as a PL/M program running under the ISIS operating system on the Intel machine. When started, Talk takes control of the keyboard and the display of the system as well as the built-in RS-232 serial ports. In its default Transparent Mode, Talk routes keystrokes from the keyboard to the serial port as ASCII characters and routes characters received on the serial port to the CRT display. Thus, if the serial port is connected to a terminal port on a timesharing computer, the development system can be used as an interactive terminal.

The second mode of Talk is known as Command Mode and is entered whenever a particular "escape" character is typed on the keyboard in Transparent Mode. In Command Mode, the user can change options or specify data transfer to and from files on the local diskettes.

A typical use of the file transfer capabilities is to send a file, such as an assembler listing, from a local floppy to a file or high-speed printer on the remote computer. Similarly, a file in "hex" format produced by a cross-assembler or cross-compiler on the remote host can be captured on a local diskette as it is transmitted from the remote system.

Since Talk can communicate with any ASCII device, it can also be used to communicate with broad-level products which offer a ROM-based monitor and an RS-232 port such as Intel's SDK-86. If the serial port controlled by Talk is connected to the SDK-86 port, Talk can be used to interactively control the target 8086 μP system. By using Talk's file transfer capability, a hex format load file on local floppy disk can be "downloaded" through Talk into SDK-86 memory via the ROM monitor.

The Talk utility has options which let the user adapt it to match the characteristics of the remote ASCII device and to select the specific serial port to use. The Talk system also includes a utility which will set the transmission speed of any serial port to a user-specified rate. Most Talk options can be set in the command which starts Talk, or from Command Mode. Some of the most commonly used options let the user:

- define the "escape" character used to enter Command Mode
- define the "quit" character which terminates Talk
- define the "rubout" character used to backspace
- define the "kill" character used to cancel an entire line
- define the character which will send a "break"
- choose either a CR/LF of LF sequence to be sent at the end of a line.

The capability to connect common laboratory equipment to larger data processing installations has proven to provide a gain in productivity. The increasing size of new embedded software systems, particularly for 16-bit μPs, has forced software builders to use more powerful cross-development techniques to harness the greater capabilities of large data processing systems rather than rely solely upon traditional laboratory programming equipment. When the lab equipment fits well into the software development methodolgy, equipment productivity is enhanced.

The Talk system is sold as a PL/M source program on ISIS diskette for $500.

Intermetrics, Inc., 733 Concord Avenue, Cambridge, MA 02138.

Write 234

Cartridge Tape Subsystem Provides Fast Backup/Restore Performance

The DEC LSI-11 has become an industry standard in a variety of applications. As with other small computers, though, non-removable Winchester systems on the LSI-11 need backup/restore capabilities to optimize their performance. In response to this need, Alloy Computer Products (Natick, MA) has introduced the LSI-50 cartridge tape subsystem to provide fast backup/restore performance.

The LSI-50 controller integrates the Sentinel ¼″ streaming cartridge tape drive from Control Data Corporation with the LSI-11. Dual DMAs and a 64k RAM buffer provide overlapped I/O

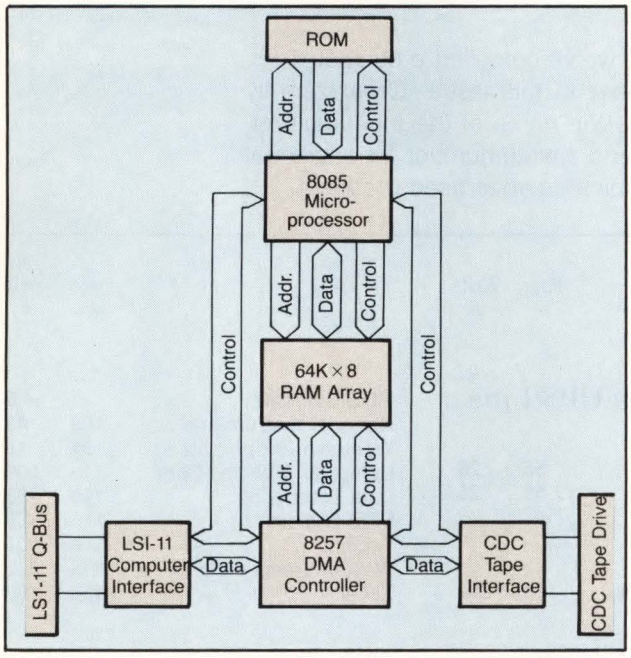


Figure 1: Communication paths between the six major components in the LSI-50.

with the disk without special programming. The subsystem provides efficient streaming (3 Mbytes per minute) by filling the buffer as far as possible before starting tape and emptying the buffer as much as possible before stopping tape. File-oriented operation is achieved by functionally emulating the DEC TU-10 and TM-11 9-track tape systems through the commands in the integral DEC chip set.

The LSI-50 provides file-oriented back-up/restore operations under DEC's PIP, FILEX, BRU, DUP, COPY, DSC, and PRESERVE utilities, and can be used under RT-11, RSX-11M, and UNIX/XENIX operating systems. The controller is designed for upward compatibility through programmable 22-bit addressing.

Controller Components

Six major components perform transfer functions. **Figure 1** shows their logical relationship, and the communication paths between them.

The 8085 microprocessor, with help from the EPROM and RAM, oversees data tranfer from the LSI-11 to the tape, using multiple INTERRUPT inputs to monitor external events. The EPROM contains the firmware, and is expandable for future additions, while the RAM buffer provides the storage space for data in transit through the system. The 8257 DMA controller synchronizes the transfer of data from RAM to either the tape drive or the LSI-11.

A DEC chipkit set has been incorporated into the controller to interface the LSI-11 bus. This set includes four bi-directional 4-bit buffers for driving and receiving the data and address lines, one register decoder, one interrupt control, one DMA controller, and two dual 8-bit registers/counters for byte count and address generation.

The CDC tape drive interface uses three basic components to link the 8257 DMA controller to the streamer. The command register contains the unit select bits and the command bits, the drive status register reports both "soft" and "hard" errors to the CPU via the DMA, and the data register, a bi-directional tri-state gate, acts as the data transmission path.

Data Transfer

Three distinct sections of the LSI-50 work to transfer data: the 8085 microprocessor and memory, the CDC tape drive interface, and the LSI-11 interface. The microprocessor and the DMA controller synchronize the data transfer to maintain maximum speed within the constraints of each section.

Let us assume we want to transfer a single block of 512 8-bit bytes of data from the LSI-11 to tape. The LSI-11 initiates the transfer process by sending instructions to the controller. The first 16-bit word is the number of

Continued on p. 107

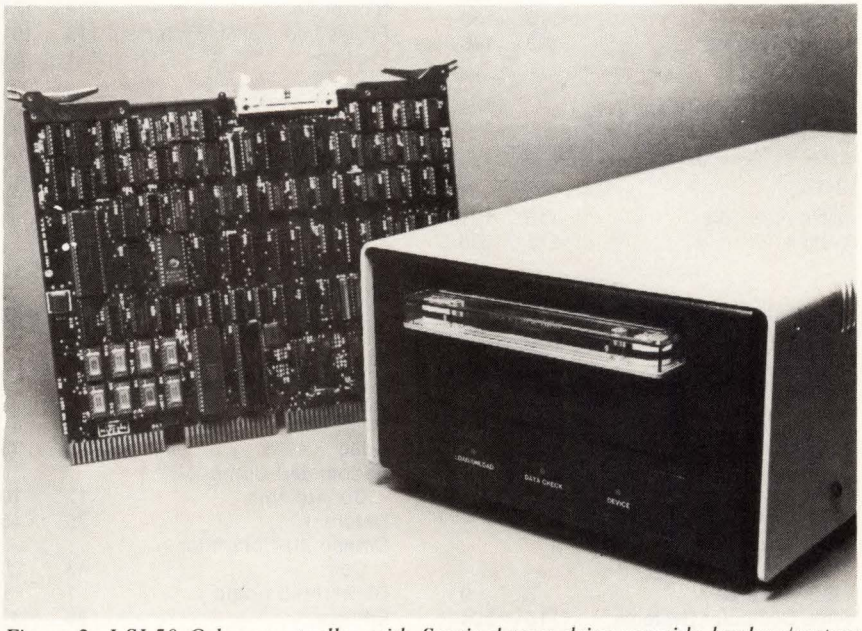


Figure 2: LSI-50 Q-bus controller with Sentinel tape drive provide backup/restore on LSI-11s.

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

Mini/Supermini Systems/ μCs

	Page #	Write #
Cambridge Digital	**93**	**45,36**
Comtal	**61**	**21**
Floating Point Systems	**19,20,21**	**12**
Hewlett Packard	**9**	**54**
Numerix	**45**	**19**
Pro-Log	**25**	**67**
Qume	**2,3**	
SD Systems	**51**	**23**
Teleram	**53**	**40**
Artel	108	212
Chancellor Computer Corp.	109	129
Kaypro	109	136
Mostek	108	211
Pacific Microcomputers	110	128
Pronto Computer	109	132
Rianda Electronics	108	137
Symbolics	110	127
Vector Graphic	112	175
Xybergraphics	112	172

Microprocessor Systems

Universal Semiconductor	**C2**	**43**
Comark	108	213
Intel	108	147
QMS	110	130
Vicom Systems	109	146

Integrated Circuits (μPs, A/D's, Multipliers, etc.)

Micro Networks	116	191
Weitek	115	206

Test Equipment

Relms	**43**	**11**
Dolch Logic Systems	109	143

Hardware/Backplanes, Packaging, Electromechanical Components

NSG America	**8**	**9**
Altos Computer Systems	115	204
Barksdale Controls	114	186

Power Supplies/UPS/Line Conditioners

Power/Mate	**55**	**26**
Triad-Utrad	**59**	**28**

Keyboards

Advanced Input Devices	115	202

Mass Storage/Drives

Chrislin	**91**	**44**
Control Data	**27**	**14**
Data Systems Design	**C4**	**52**
Emulex	**67**	**33**
Quantex	**81**	**62**
Rixon	**79**	**38**
Data Electronics	113	164
Data Systems Design	114	192
Microperipheral Corp.	111	168

Printers/Plotters

Epson	**C3**	**51**
Hecon	**87**	**42**
Nicolet Zeta	**49**	**16**
Anadex	112	178
Mitsubishi Electronics	112	158
Nicolet Zeta	112	177
Philips Information Systems	113	161
Printronix	111	165

Communications Equipment

Artel	**6**	**32**

Add-In Memory Boards

Monolithic Systems	**14**	**3**
Fujitsu Microelectronics	114	203

Controllers/Interface Boards

Adac	**73**	**35**
Associated Computer Consultants	**17**	**10**
Dataram	**75**	**45**
Datasouth Computer Corp.	**46**	**20**
Distributed Logic	**1**	**1**
Emulex	**35**	**31**
Interactive Structures	**13**	**5**
MDB Systems	**4**	**4,6**
National Instruments	**109**	**48**
Westerrn Peripherals	**31**	**15**
Computer Products Corp.	115	199
Data Translation	115	188
MDB Systems	115	189
Tecmar	114	230
Western Peripherals	115	205
Xebec	116	198

CPU Boards

Decmation	**62**	**30**
Sigma Information Systems	**77**	**37**
Altos	116	204

Color Graphics

Aydin Controls	**47**	**22**
Lexidata	**39**	**24**
Matrox	**44**	**18**
Modgraph	**41**	**8**
Princeton Graphic Systems	**58**	**27**
Seiko	**11**	—
Summagraphics	**22**	**13**
Electrohome	112	169
Intecolor Corp.	108	126

Data Terminals

Lundy	**7**	**7**
Selanar	**57**	**25**
Northern Technologies	110	133

Busses

Datel Intersil	**69**	**34**
dy4	**60**	**29**
Heurikon	**6**	**53**
IKIER Technology	**42**	**17**

Displays (LED, Vacuum, Fluorescent, Etc.)

UCE	114	200

Achieve High Speed Data Acquisition With A Fast ADC And DMA

High speed ADCs, with update rates faster than 500kHz, are much faster than μP instruction cycles. If μP programmed instructions are used to read data from these fast ADCs, either data will be wasted or the ADCs will have high idle time. The solution to this problem is to transfer the ADC output directly into memory without μP intervention.

A dedicated high speed circuit, the DMA controller, is used to accomplish this task. It halts the μP, takes over control of the Address, Data and Control Bus lines, and transfers data directly to memory, completely transparent to the μP.

The DMA Controller

Processor halt, cycle steal and memory sharing are techniques of DMA that are commonly used. Each offers advantages depending on the desired hardware and software complexity, the quantity of data to be transferred, and the required data transfer rate. With the processor halt technique, a control line is used to initiate an orderly halt to μP operation. In the halt state, the μP Address, Data and Control Bus lines are disabled. When the DMA transfer has been completed the halt control line is reset, and the μP resumes normal operation where it left off.

With the cycle steal technique, external control lines are used to initiate a μP pause in the middle of the instruction cycle. This is accomplished by momentarily halting the μP clock and disabling the μP Address, Data and Control Bus lines. The DMA controller "steals" several machine cycles to transfer data to memory. Upon completion of DMA transfer, the pause control lines are reset, the μP clock restarts, and the instruction cycle continues where it left off. With the memory sharing technique, the DMA controller is synchronized with the μP clock. It interleaves DMA transfers to memory during the portions of the machine cycle that the μP doesn't access memory. Of the three techniques, processor halt offers the best tradeoffs for high speed data acquisition, since high speed bursts of data must be transferred directly to memory and subsequently processed.

A typical sequence of operations for a μP initiated (halt mode) DMA transfer to memory would proceed as follows: the μP would use the Chip Select and R/W lines to initialize the DMA

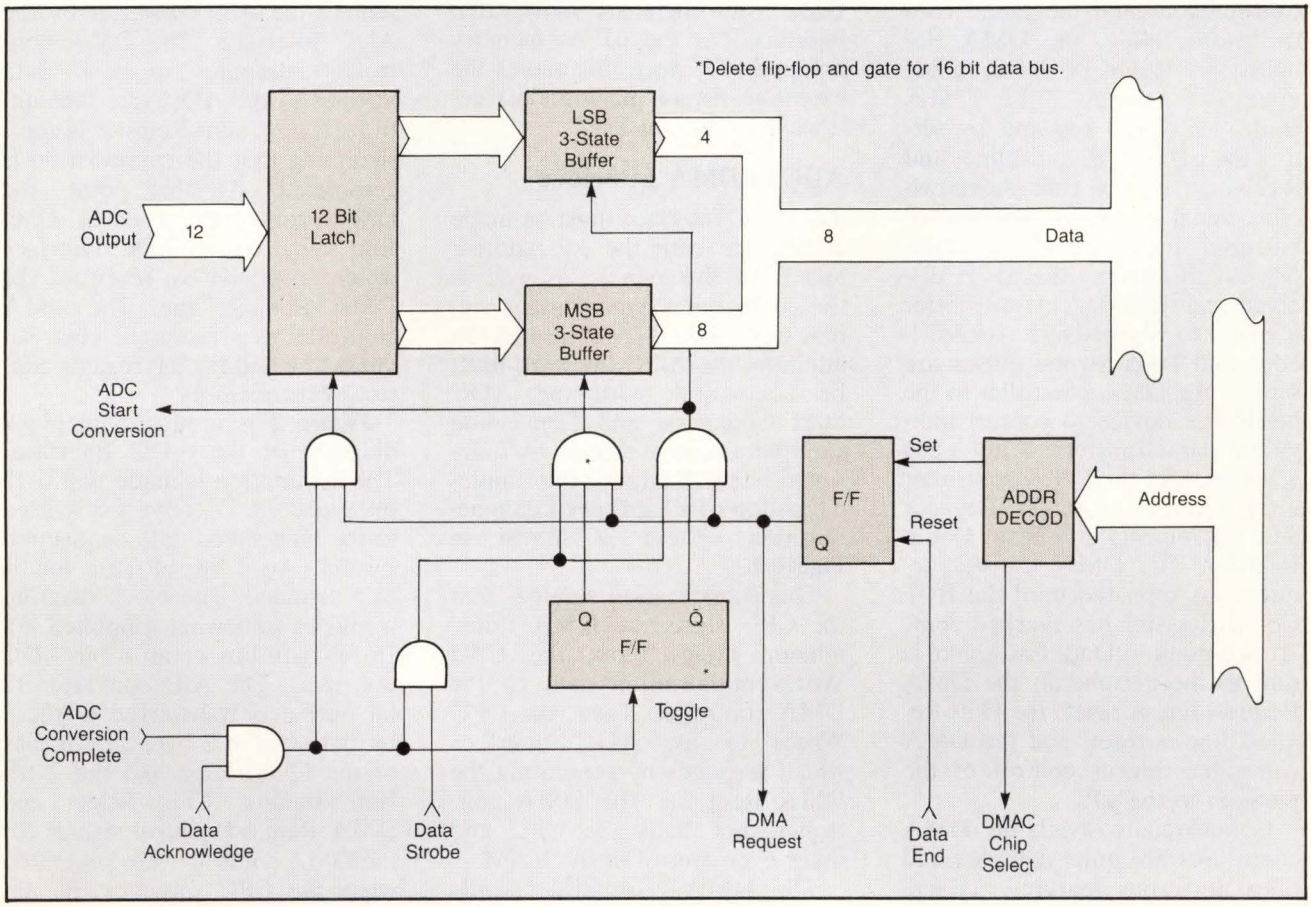


Figure 1: Block diagram of a high speed data acquisition system. Implementation is achieved with a fast ADC, an ADC Interface, a DMA Controller and a μP.

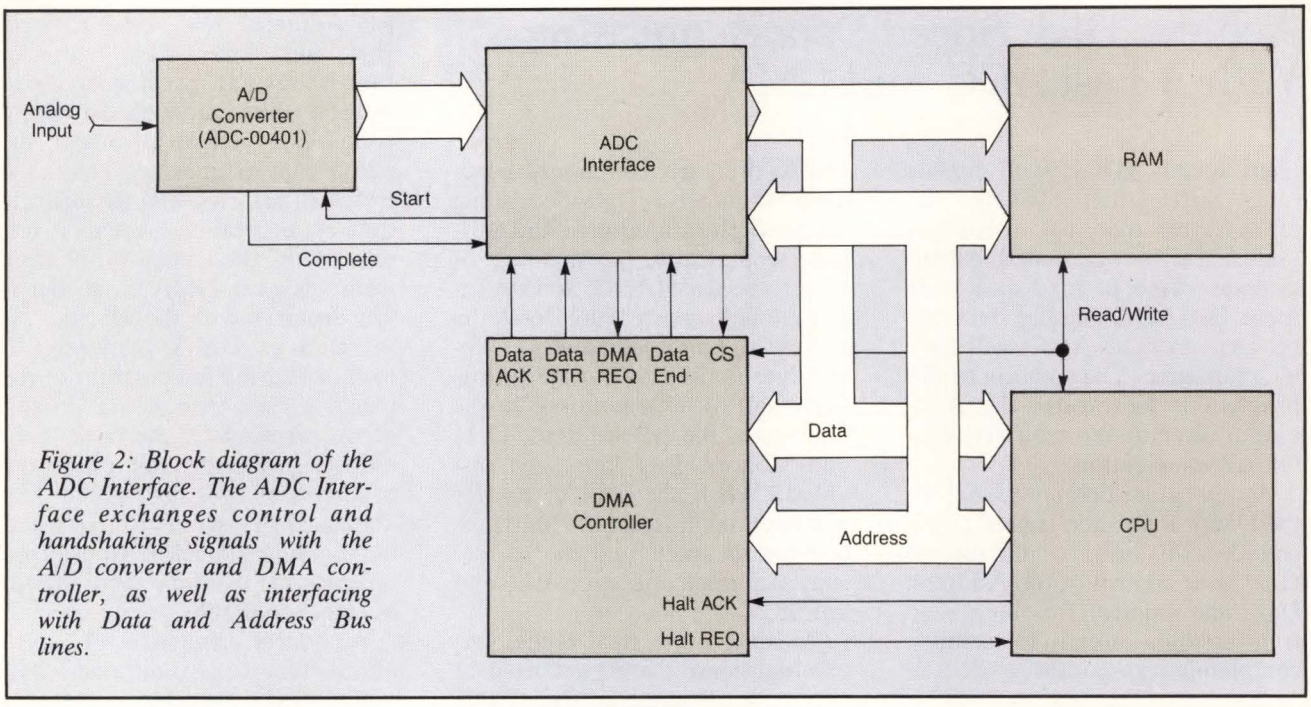


Figure 2: Block diagram of the ADC Interface. The ADC Interface exchanges control and handshaking signals with the A/D converter and DMA controller, as well as interfacing with Data and Address Bus lines.

controller registers with data for the starting memory address to be used, the number of words in the transmission, and the mode control word. Next, the DMA Request line would be set by a peripheral device. The DMA controller would respond by setting the μP Halt Request line, and receive in turn a Halt Acknowledge signal signifying that the μP has given up control of the memory. At this point, the μP is disabled and the DMA data transfer is ready to begin. Data Acknowledge and Data Strobe pulses are sent by the DMA controller to the peripheral device to control individual data transfers. After each word transfer the DMA controller increments its Address Register and decrements its Byte Count Register. The DMA transfer sequence is repeated until the Byte Count Register has reached zero. At this point, a Data End signal is sent to the peripheral, the DMA Request line is reset, the Halt Request line is reset, and the DMA controller returns control of the memory to the μP.

Commercially available DMA controllers are quite complex and offer numerous features. Typical of these features are multiple channel capability, programmable channel priority, address increment or decrement, and data chaining by combining channels. DMA controllers are most often interfaced to the μP as memory mapped I/O, since this makes the extensive list of memory instructions available for use.

ADC to DMA Interface

The ADC Interface must be made compatible with the μP Address and Data Bus signals, as well as the control and hand-shaking signals from the DMA controller. In addition, the ADC Interface must be compatible with the ADC Start Command and Conversion Complete control signals. A functional block diagram of an implementation of a high speed data acquisition system is shown in **Figure 1**.

This configuration assumes that the CPU starts the DMA transmission cycle. First, the CPU Writes initialization data to the DMA controller. Then, the CPU Writes to the ADC Interface which responds by generating the DMA Request. The DMA controller then halts the CPU and takes over control of the RAM.

The DMA controller sends Data Acknowledge and Data Strobe pulses to the ADC Interface to transfer each word to the RAM. Each Data Strobe causes a new Start Conversion signal to be sent to the A/D converter by the ADC Interface. The DMA controller continues to send data Strobes to the ADC Interface until its Byte Count Register is zero, signifying that the transmission is completed. At this point, the DMA controller sends a Data End signal to the ADC Interface which responds by resetting the DMA Request line. The DMA controller then resets the Halt Request line and the μP regains control of the memory.

Figure 2 is a functional block diagram of the ADC Interface. The assumption is made that a 12 bit 2 μsec A/D converter is used in the high speed data acquisition system. An 8 bit μP data bus is also assumed. The block diagram would be somewhat simplified if a 16 bit data bus or an 8 bit ADC was used. The A/D converter 12 bit output is transferred to the 8 bit data bus in 2 bytes, by means of the 12 bit latch and the 2 tri-state buffers. Chip Select and DMA Request control signals for the DMA controller are generated when the CPU provides the appropriate address to the Address Decoder. The Address Decoder

sets the DMA Request flip-flop. Conversion Complete, Data Acknowledge, Data Strobe and DMA Request signals are used to drive the gate circuits which generate strobes for the 12 bit latch, the 2 tri-state buffers, and the Start Conversion signal.

The DMA Request signal is used to enable the 3 gates which generate the strobe signals. When the transmission has been completed, and the Data End signal is received, the flip-flop is reset to disable the data transfer path. During a DMA transfer, the simultaneous occurrence of Conversion Complete and Data Acknowledge signals causes the ADC output data to be loaded into the 12 bit latch. Since the 12 bit ADC data requires 2 bytes to transfer to RAM, a toggle flip-flop is used to alternately enable the gates for MSB buffer strobe and LSB buffer strobe. If a 16 bit data bus was used the toggle flip-flop and one of the gates wouldn't be needed, since all 12 bits would be transferred at once. The Data Strobe signal from the DMA controller generates the actual strobe signals for the MSB and LSB buffers. The LSB buffer strobe signal, which transfers data to RAM, is also used as the A/D converter Start Conversion signal.

It should be noted that this ADC Interface implementation causes the first word of a given burst transmission to erroneously be the same as the last word of the previous burst transmission. This flaw results from the simple hardware gating scheme that is employed and can be overcome in software by ignoring the first memory location in subsequent μP computations.

Software Is Simple

Since the DMA controller and the ADC Interface provide most of the functions required of the DMA transmission from the A/D converter, the software requirements are quite simple. It was assumed, in the high speed data acquisition system described above, that the μP initiates the DMA transmission. For simplicity, the A/D conversions are controlled by the DMA controller and the ADC Interface. As a consequence of this implementation the software program needs only to initialize the DMA controller Address Register, Byte Count Register and Mode Control Register, and then Write to the ADC Interface to start the DMA cycle.

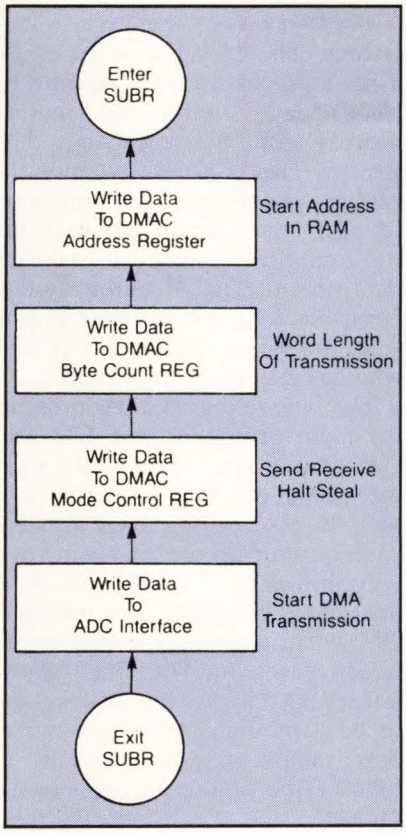


Figure 3: Software flow diagram. A simple 4 instruction program implements the μP initiated DMA transmission to memory.

Figure 3 is a Software flow diagram illustrating the μP program for the high speed DMA transmission. Immediately after the μP starts the DMA cycle it receives a Halt Request. It continues with the next program step when the DMA controller resets the Halt Request and returns bus control.

David C. Pinkowitz, Product Manager, Data Converters, ILC Data Device Corp., 105 Wilbur Place, Bohemia, NY 11716.

UPS Update

Dear Sir:

I would like to compliment your publication for the excellent article appearing in your June 1983 issue of *Digital Design* entitled "Diverse UPS Technologies Provide Design Alternatives" (p. 81), and as one of the few publications that presents an unbiased opinion on the relative merits, advantages and disadvantages of various types of power conditioning and UPS equipment available.

I would like to call your readers attention to a technical error in your description of RUPS™ operation. The article states "during normal utility power, the DC motor-generator becomes a motor, continuing to drive the AC generator with no effect on the load."

The statement should be revised as follows "during normal utility power operation, the AC motor drives both the AC generator and the DC motor-generator. The DC motor-generator operates as a generator battery charger to recharge/float charge the batteries while the AC generator provides clean power to the computer. During utility power outages (blackouts), the DC motor-generator operates as a motor and continues to drive the AC generator with no effect on the load."

In figure 10, the RUPS is shown having "reverse transfer" which is in error. The figure actually shows normal operation with an automatic bypass switch installed.

Lastly, in the manufacturers column under motor-generator sets, Computer Power Products is listed as only supplying equipment in the three phase range of 10–40 KVA. In actuality, CPP manufactures motor-generators in the single phase input or output range of 2.5 to 10 KVA in any combination of 50–60 or 415 hertz and in three phase input and output from 12.5 to 500 KVA.

R. N. Bowyer
Vice-President, Marketing/Sales
Computer Power Products
Gardenia, CA

Not The Only Ones

Dear Sir:

This letter is in reference to an article that appeared in the May issue of *Digital Design* entitled "Flat Electronic Displays In Computer Products and EDP Applications" (p. 22).

Since we at MH&W International are marketing two of the products discussed in the article (VFD's and LCD's), the information was of high interest to us. However, not all of the facts in the article by Mr. Castellano are complete as presented. I would like to draw your attention to page 22 col. 3 the subtitle, "All in Japan." The following statement is incorrect. "There are only three manufacturers of VFD's, all based in Japan and each controlling about one third of the world market." There are *four* manufacturers of VFD displays. The fourth manufacturer is Choa/Techna Display Corp. which is a member of the Techna Electronics Industrial Group in Tokyo, Japan. This company is not related to any of the others mentioned in your article.

In this article, it is mentioned that ISE Corporation announced the development of a 256×256 element VFD matrix display. Again for your information I think you should know that we have been demonstrating a 256×256 dot matrix VFD panel around the USA and Canada since July, 1981 and in fact have had these devices in a production status and have been sampling the market for more than a year.

Since I feel that our product is one of the emerging flat, dot matrix display technologies, I wanted to make you aware of its existence, so that any special features you may publish in the future on this subject may acknowledge this correction.

Thank you for your time and consideration in this matter.

Robert P. Kiernan
Product Manager
MH&W International Corp.
Mahwah, NJ

Continued from p. 94

system. The Master system establishes a process for the transmitting (send) data stream and another process for the receiving data stream. This is necessary since the calling system does some interpretation of the user's commands and thus requires a process for each data stream. The answering system is unable to distinguish a CU link from that of any other remote user who has called up for a login.

The answering system presents the login prompt to the CU user and the user must login with a valid user name on the answering system. In essence, the user also becomes a user on the answering system; however, CU offers a great deal more flexibility. For instance, CU, while allowing the user an interactive session with the remote system, also allows the local system to be a participant in the session. An example session would be as follows (the calling system is blue):

cu red!	. . .establishes the link
****	. . .red's login procedure must be negotiated
~%put file1 afile	. . .equivalent to UUCP example; afile is created on red from file 1 on blue
diff afile bfile	. . .compares afile and bfile on red and outputs the result on the user's terminal on blue (The diff command residing on red)
~diff file1 file2 >cfile	. . .compares file1 and file2 on blue and outputs the result to cfile on red (The diff command residing on blue)
	. . .terminates the session

The session was brief and made use of only the diff command. All of the Unix commands on both systems are available to the CU user. The tilde ~ character specifies a command on the local system while absence of the tilde specifies commands to be executed on the remote system.

Thus the unique capabilities of the Unix operating system in a software development environment diminishes the impact of hardware vendor decisions and allows the organization to purchase the size system which makes the most financial and organizational sense. With a built in communication scheme like the UUCP capability, the software development house can approach procurement of development hardware in a manner consistent with its growth. A small economical Unix system could be added to the development hardware base when a few new programmers have been added. Or a Unix system based on a different processor or vendor could be added without severely damaging the integrity of the development procedures. Multiple small "project" systems would grant a certain autonomy to the project group without sacrificing the overall development department's efficiency—in fact, it would probably enhance the efficiency.

Nothing restricts the development department from having all of these flexibilities if they choose to have one large multiuser development system. It is a heavy commitment in finances, a long term commitment to a system manufacturer, and requires a local networking requirement to all workstation areas from the large system. Several smaller machines can be placed in work areas with little networking, multiple vendors systems can be purchased if desired, and the financial commitment occurs as the expansion is needed.

Unix gives the software development organization additional flexibility in choosing the development system, flexibility in choosing the size of the development system, flexibility in assigning priorities for machine time, capability to carefully administer software development activities without depending on the developer or manufacturer, and capability to properly maintain software without complex administrative control. □

Innovative Design

Continued from p. 97

bytes to be fetched from the host's memory, and the second 16-bit word contains the starting address of the data that will be transferred. The LSI-11 then tells the controller to begin transferring the data block. Since the LSI-50 controller uses DMA and operates in an interrupt driven environment, the LSI-11 does not need to monitor the transfer after this time. The LSI-11 now gives complete control of the operation to the 8085 μP.

The 8085 then fetches the prescribed number of bytes (the microprocessor uses this parameter to program the 8257 DMA with the internal address to which the data transfers), signals the DMA controller to begin the programmed transfer, and awaits an INTERRUPT, signalling completion or error conditions. During the transfer time, both the microprocessor and the LSI-11 can perform other tasks since the DMA operates on a "cycle-stealing" basis.

Upon successful completion of its task, the DMA controller sends an INTERRUPT to the 8085, which then programs another channel in the same DMA controller in preparation for transfer of the data from the memory array to the Sentinel tape drive. The same byte count and address information is programmed as before, but a unique set of logic performs the transfer between the devices.

The CPU sees an INTERRUPT signal upon completion of this task. Once that has been received, the microprocessor stores the tape drive status in a host-accessible register, and forces an INTERRUPT onto the LSI-11 control lines.

Data transfer in the opposite direction, tape to LSI-11, works in the reverse sequence, although the LSI-11 still initiates the process.

James Ehrenfried, Alloy Computer Products, 100 Pennsylvania Ave., Natick, MA 01751.

Write 308

VIDEO COMMUNICATIONS SYSTEM

For Fiber Optic Computer Graphics

The T/R-2011 computer graphics system transmits ultra-high resolution computer-generated video. Applications include CAD/CAM, process control and image processing. The T-2011 and R-2011 are plug-in transmit/receive modules that transmit high resolution RS-170 video up to 10,000 ft. over fiber optic cables. The fiber optic system bandwidth accommodates either 640 × 512 or 512 × 512 pixel resolution. The T/R-2011 permits long distance interconnection between the workstation monitor and the computer video display generator without loss of video resolution. Both RGB (red-green-blue) color and monochrome video signals can be handled by the system. Dual BNC I/O connectors are plug compatible to virtually all monitors and display generators. The modules perform automatic self-monitoring, self-testing, alarming, and on-line without program interruption. Automatic gain control and DC clamping features assure stability of color and picture levels. **Artel,** Worcester, MA **Write 212**

COLOR GRAPHICS TERMINALS

UNIVAC U–200 PLUG-Compatible

The Intecolor Corp. family of computers offers two new color graphics terminals. These terminals were specifically designed for use by Univac 1100 Series MAPPER customers. Both Intecolor terminals emulate the U–200 protocol and both are plug-compatible with the U–200. Features include single station or up to 16 terminals clustered on a Univac multiplexer, U–200 emulation, 8 foreground background colors, and 32K RAM to support the MAPPER graphics "core" high resolution graphics interpreter. Also included are a down-line loaded from the 1100 host and 2 asynchronous RS–232 channels. **Intecolor Corp.,** Norcross, GA **Write 126**

μC SYSTEM

ATE And Data Acquisition

DISKSTOR M-2 is a μC system for applications such as data acquisition, factory automation, automatic test equipment, and office automation.

The system includes a 10 MHz 8086 16-bit processor, 128KB of memory with parity, serial and parallel interface ports, and dual double sided floppy disk drives. The entire chassis assembly may be removed from the front without unmounting the shell, thus providing access to all sub-assemblies for service or maintenance. A 200W switching power supply provides immunity to line voltage fluctuations. A removable communications panel organizes I/O cabling while providing expansion capability. Price is $8,590. **Comark Corp.,** Waltham, MA **Write 213**

TRANSACTION PROCESSOR

4 User Mainframe—Calibre Features

The desk top system provides mainframe-calibre features for up to four users and offers complete multiuser, multitasking and multiprogramming capabilities in an integrated package. The iTAPS package consists of an interactive application development facility, a run-time transaction monitor with an integrated relational database manager and an on-line query and update facility. In execution, the iTAPS transaction monitor performs an array of functions that include security, menu selection, data-base facilities, update logging, error recovery and on-line query/update capability. The 86/435 allows four independent users to concurrently execute applications. Price is $16,575. **Intel Corp.,** Santa Clara, CA **Write 147**

CP/M-COMPATIBLE OPERATING SYSTEM

Large Directory Capability

A version of Mostek's enhanced virtually CP/M-compatible μC is an operating system that features a large directory capability, high speed and wide user interface. Designated the M/OS-80 V6, it is designed to meet the growing need for a general-purpose operating system that can utilize the wide variety of prewritten application packages available for μC systems. The operating system supports a 5¼", 5Mbyte Winchester hard disk drive and MSC Xebec Corporation controller. This system offers 252 directory entries as compared with 64 entries for the M/OS-80 V3 operating system. The M/OS-80 V6 operating system is designed to be used with the Mostek MDX-SASI1 or MDX-SASI2 disk controller interface board. Price is $495. **Mostek Corp.,** Carrollton, TX **Write 211**

MULTIUSER μC

Designed Around Fairchild 9445

The Caribe is a line of multiuser μCs that offers a selection of two operating systems, five application languages and peripheral devices from 60 manufacturers. Blis/Cobol and Bits/Basic operating systems are available. Caribe allows execution of programs in application languages including BASIC, COBOL, FORTH, FORTRAN and PASCAL. Caribe contains a I/O controller board that accommodates peripheral devices and supports from one to 20 terminals. The central processor board is designed around the Fairchild 9445 μP which is specified for operation over a temperature range of −55°C to +125°C. $13,830. **Rianda Electronics,** Anaheim, CA **Write 137**

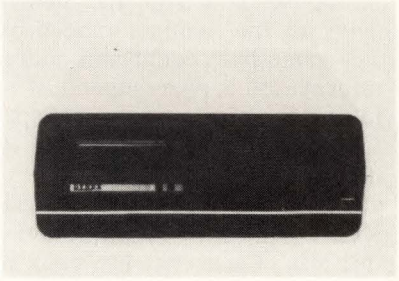


IMAGE-PROCESSING SYSTEM

70 Interactive Commands & Routines

Among the software commands in the Vicom Image Processing Software (VIPS) Library is an SVD/SGK image filtering command that eliminates "noise" and sharpens images input to the VICOM system. Geometric operations in the VIPS library enable the VICOM to rotate, expand and reduce images using its integral array processor. Other key features include implementation of a set of interactive graphics commands, permitting the user to construct plots of mathematical functions, trace outlines of objects, write text overlays and calculate areas of shapes as well as a variety of spatial linear and non-linear image enhancement operators. Price for existing VICOM users, $500. **Vicom Systems, Inc.,** Sunnyvale, CA

Write 146

PORTABLE COMPUTER

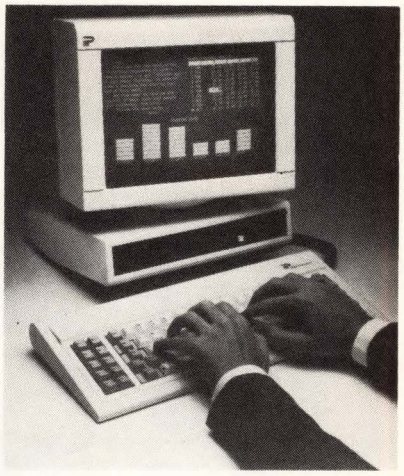
With Double Density Disks

The Kaypro 4 is designed for use with double-density disks with 394K memory each. The computer employs the 8-bit Z-80 μP and features a standard professional keyboard that includes 20 programmable keys plus a 14 key calculator-type numeric keyboard. It has a high-resolution 9″ green phosphor screen with a full page display capable of 80 columns across by 24 lines deep. $1,995. **Kaypro,** Solana Beach, CA **Write 136**

SUPER MICRO

16-Bit Bus

The Pronto Series 16, is a 16-bit super-μC with a 16-bit bus. It utilizes Intel's iAPX186 μP, and comes with 128 Kbytes of RAM. Serial and parallel ports, a clock/calendar, and a system security ROM are included. The computer is available in four configurations, with one 800K formatted floppy disk drive—$2995, two floppy disk drives with 1.6 MB total capacity—$3750, one floppy drive and one removable 5K hard disk drive—$4995, or two 5 MB removable hard disk drives—$5995. **Pronto Computer,** Torrance, CA **Write 132**



CAD/CAM ENGINEERING WORKSTATION

Ethernet LAN Capability

This workstation is intended to be used as a stand-alone multifunction workstation or as a node in an Ether-

net LAN communicating with other computer systems and peripherals. It features schematic capture, local simulation and layout for the design of integrated circuits and PC boards. The workstation's computer aided designed software is based on Cadcam Technology Inc.'s Cadgraph, Simulog and Skimcap products. These capabilities are supported by a hardware configuration which includes a 640 × 400 or 1K × 1K color high resolution monitor, ½ Mbytes of main memory, 10 Mbytes of disk storage, full scale graphics editing, 8087 floating point processor and an Ethernet LAN capability. **Chancellor Computer Corp.,** San Francisco, CA **Write 129**

GRAPHICS PROCESSING SYSTEMS

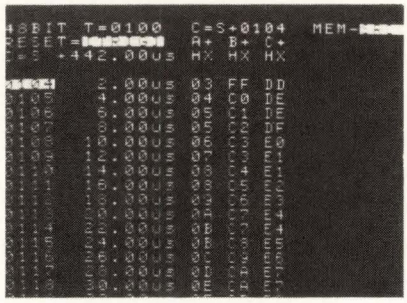
For Non-Impact Printers

The system, called the QUIC-RIP System, drives a 60 page/min Delphax ion deposition printer. The QMS QUIC-RIP System gives printers the ability to do letter-quality word processing, industrial graphics and barcoding, bit-mapped graphics for scientific and CAD/CAM applications, intermixed fonts, multiple forms overlay, EDP line printing, and multi-page collated document printing. Interfaces available on the graphics processing system are: Centronics, Dataproducts positive and negative true, RS232 and active and passive current loop with various protocols, IBM 3270, IBM 3271, IBM 3272, IBM 3274 A and B, IBM 3276, IBM System 34 and 38, IBM 2780, IBM 3780, IBM 8100, Burroughs TC500, and TC3500, Synchronous or Asynchronous TDI, NCR 8200, NCR 9020, RS449 serial, Wang VS and Ethernet. **QMS,** Mobile, AL **Write 130**

LOGIC ANALYZER

Selective Trace Trigger Function

The TSO 16 Time Stamp Option allows the LAM 4850A's user to measure the time between events when using the machine's selective trace trigger function. It enhances the 4850A's capabilities by permitting operations such as logging random events in real time, performing execu-



tion-timing measurements for software analysis and analyzing timing in multiprocessor applications. The TSO 16 Time Stamp Option permits timing measurements to 65,535 counts or 65,535 × internal clock rate seconds with a resolution (min clock period) of 50 nsecs to 500 msecs in 5–2–1 steps. A Start Recording signal is available for the synchronization of recordings in additional analyzers. In multiprocessor and communications applications, LAM 4850As can be synchronized for a real-time correlation among asynchronous events. **Dolch Logic Instruments,** San Jose, CA **Write 143**

INTERACTIVE WORKSTATION

Lisp-Based

The 3600 is a high-performance, interactive workstation for applications requiring large-scale problem-solving capabilities such as computer-aided design and artificial intelligence. The Symbolics 3600 has a 36-bit tagged architecture with 32-bit data paths and executes programs at an average of one million high-level instructions per second. The basic system hardware features 2.3 Mbytes of MOS memory with ECC (512K 36-bit words); one parallel and three standard serial I/O ports, a 10 mbit/sec Ethernet interface, a graphics console, and a 169 Mbyte SMD-compatible Winchester disk drive. Each memory board has single-bit error correction and double-bit error detection. Up to 15 memory boards can be installed in the standard chassis providing a total of 34 Mbytes of main memory. **Symbolics,** Anaheim, CA **Write 127**

CUSTOM CRT

VT100 ANSI and VT52 Compatibility

The Vision 1000 offers full VT100 ANSI and VT52 compatibility, including advanced video and printerport, 80 or 132-column display, and smooth-scroll. Standard features include a green phosphur screen, an English set-up menu, and a variable-speed smooth-scroll. A 25th status line has been added to provide feedback on the terminal's operating condition. When operating in an 80 column mode, the terminal extends its

own capability through a two page technique that reclaims unused 132-column display memory, giving the operator an additional page of memory. Four user-programmable function keys are included. **Northern Technologies,** Ontario, Canada **Write 133**

DUAL PORT 68000 SBCs

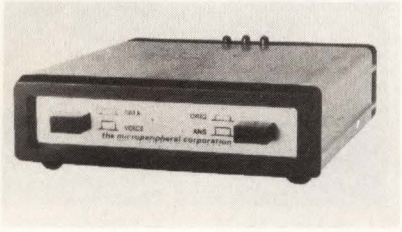
Memory Management

The PM68D, dual ported RAM and Memory Management enables support of up to 8 Mbytes of on-board memory and 16 Mbytes of Multibus memory. Also featured are interrupt handling facilities, dual port memory, hardware generated refresh, serial I/O, and parallel I/O. The PM68D utilizes the Motorola 68010 and supports the features of demand paging and virtual memory. **Pacific Microcomputers,** San Diego, CA **Write 128**

MODEM

Autodial, Autoanswer

The AutoPrint-Microconnection features both an autodial and auto-



answer capability, and has a built in Centronics compatible parallel printer port. It operates at 300 baud in either originate or answer mode and is FCC Type Accepted. The combination modem and printer interface plugs directly into the computer and telecommunications software is provided in the user manual. The printer port permits connecting conventional parallel printers such as the Epson and Oki. With the modem connected to the phone line, the printer will simultaneously provide hard copy of whatever appears on the screen. Word processing software is available which routes text to the printer via the modem. **Microperipheral Corp.**, Redmond, WA **Write 168**

DESK-TOP LINE PRINTER

For Stand-alone Hard-Disk μCs

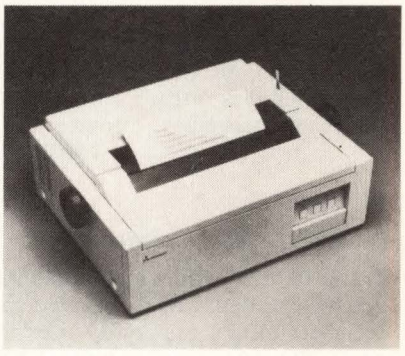
The MVP features a combination of matrix printer output with line printer performance for workhorse applica-

tions. It is designed for stand-alone, hard-disk based μC systems and can be used as a shared resource printer for workstation clusters or as a system printer for μC-based LANs. The MVP functions as a remote terminal printer for minicomputer and mainframe systems. Corresponding print speeds are 80, 150, and 200 LPM, with plot rates ranging from 8.3 to 27.8 IPM. $3,745. **Printronix**, Irvine, CA **Write 165**

THERMAL PRINTER

Centronics Compatible Interface

The color printer is a thermal hard copy output device designed for personal computers and μC systems with



color CRT displays. Capable of producing as many as seven colors for text highlighting and bit-map output, the printer utilizes a cassette-type, four-color or black only thermal transfer ribbon. The unit uses a

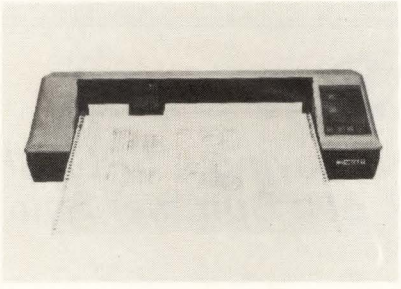
24×24 dot matrix format to provide correspondence quality text printing, with 1/6", 1/8" and 1/120" vernier line spacing pitch options, at speeds of 45 CPS. Bit-map output is supported with up to 1,440 dots/line at a resolution of 180 dots/in. Incorporating a μP in its structure, the device features an 8-bit Centronics compatible parallel interface, or optional RS232C serial interface. Other features include a 96 character ASCII set, bidirectional and doublewidth printing on plain paper, and pin or friction paper feed with continuous or cut forms. $1,500. **Mitsubishi Electronics,** Torrance, CA.

Write 158

PLOTTERS

Local and Remote Interfaces

The Zeta 822 provides high resolution graphics for both continuous feed and cut sheet media. Supported sizes include ISO A4 through A1 and ANSI A through D. Types of media available are translucent paper, vellum, glossy bond, mylar, and clear inking film for view graph presentations. Throughput is attained by using eight



capped pens on one μC controlled carriage. The ZETA 822 plots at 25 in./sec. with 2g acceleration. The plotter offers 0.025mm (0.001 inch) resolution. Both local and remote interfaces via RS-232 and IEEE-488, at eight different data rates, are user-selectable. $12,900. **Nicolet Zeta,** Concord, CA **Write 177**

PROJECTION MONITOR

Technical Training Applications

The ECP is a portable color data/graphics projection monitor, that projects full color images from sources such as color computer graphics terminals, video cameras, or video cassette recorders through a single lens. Typical uses include technical training applications, where videotaped demonstrations are alternated with computer images, technical presentations, where CAD/CAM or electronic imaging are viewed and discussed, teleconferencing, and sales presentations. The ECP 1000 can display data taken from most computer graphics terminals by running a cable from the terminal's video output plug to the ECP 1000's input plug. It has a resolution capability of 600 lines and can support output from most widely used computer graphics terminals. $14,800. **Electrohome Ltd.,** Kitchener, Ont.

Write 169

16-BIT OPERATING SYSTEM

Disk File Storage

CP/M-86 runs on all models of the 8/16 bit Vector 4, including the Vector 4/20 with 1.2 Mbytes of flexible disk

storage, the Vector 4/30 with 5 Mbytes of hard disk storage, and the new Vector 4/40 with a 10-Mbyte hard disk. Vector 4 computers can be used as standalone single-user systems, or as multi-user systems when attached to Vector's LINC LAN. The operating system has environment customizing options. The Vector 4's programmable function keys can be assigned string values for different applications, and those assignments can be stored in a disk file. **Vector Graphic Inc.,** Thousand Oaks, CA **Write 175**

DOT-MATRIX PRINTER

Prints At 500 cps

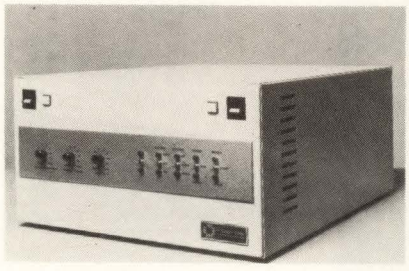
The DP6500 Rapid/Scribe data processing printer has speeds of 500 cps at 10 cpi and 540 cps at 12 cpi. Key to the printing is an 18-needle printhead consisting of two vertical columns of nine each. As the two columns of print needles are adjacent to each other, two identical columns of dots may be printed at one time. Features of the DP-6500 are enhanced mode printing with proportional spacing or at 10, 12, 15, and 16.4 cpi at speeds up to 410 cps. A dual-pass correspondence quality mode provides proportional spacing and 10, or 12 cpi at speeds of 100-120 cps. The high resolution graphics mode provides a dot resolution of either 72 or 144 dots/in. Options include character font downloading from the host computer, alternate character fonts in PROM, and UPC and Code 39 bar codes. Standard buffer storage is 4.5 Kbytes. $2,995. **Anadex,** Chatsworth, CA

Write 178

STEPPER MOTOR CONTROLLER

For Electromechanical Applications

The Axis III controller utilizes expandable Multibus architecture with an Intel 8086/8087 processor and custom designed motor drivers. The controller is intended for electromechanical applications as well as X-Y or X-Y-Z tables, computer controlled machinery and robots. Primary inter-



face to a host computer is via an RS-232 serial port. Positioning and speed data is supplied by the host computer via a structured command language. Speed (feed rate) may alternatively be set from controls at the controller's front panel. Limit sensing is standard. Spare Multibus slots are available for memory, peripheral or other expansion. $5,500. **Xybergraphics,** Mt. View, CA **Write 172**

GRAPHING APPLICATION

Editing Feature

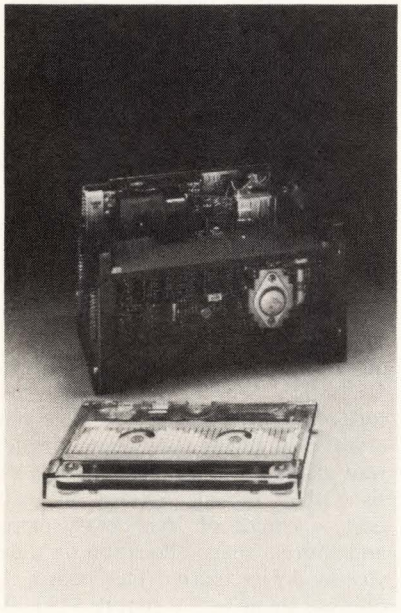
DR Graph is a presentation quality graphing application used to develop slide presentations, trend charts and

financial analysis reports. DR Graph is built on GSX, the graphics system extension for both the 8-bit and 16-bit CP/M operating systems. GSX gives CP/M the ability to interface with hardware devices ranging from plotters and printers to CRTs. Users can place up to four separate graphs on a page to simplify complex page layouts. In addition, graphs can be created using data from spreadsheet programs such as VisiCalc and SuperCalc. **Digital Research,** Pacific Grove, CA **Write 176**

FUNNEL DRIVE

Stores 50 MBytes

Designed for high capacity full function tape peripheral and Winchester back-up applications, the 50 Mbyte Super Funnel is fully compatible with cartridges written on any Funnel ¼" digital cartridge tape drives. This drive is μP controlled and features bi-directional serpentine recording, to eliminate the rewind time between tracks. Super Funnel can read data written at 6400 bpi on four tracks and write and read at 8533 bpi on seven tracks. The basic components of the



tape drive include R/W head with codec function, interface logic with motion control and status reporting, EOT/BOT sensing and management, drive motor and servo system controls. The drive has the capability of file search, track select, and of changing or adding to existing records. A high duty-cycle motor with continuous start/stop capability enables the Super Funnel to construct and read files with standard ANSI interblock gaps at 37.5 ips and locate these files at either 37.5 or 90 ips in both forward and reverse directions. Up to 4 drives can be connected together on a common bus. The drive has a data transfer rate of 40 Kbytes/sec. Power requirements are +5 and +24 V-dc. **Data Electronics,** San Diego, CA **Write 164**

FOUR COLOR PRINTER

70 Character Sets

Operating with the Philips 3000 Series information processing systems, the GP300L four color printer works at speeds of 300 characters/sec. The GP300L prints four colors (red, blue, yellow and black) and graphics in 95 character sets with 144 × 144 dots/in. resolution. It drafts at 120-300cps and prints letter quality at 60-120 cps. 70 character sets are programmed into the printer in resident ROM as well as semigraphics, bar codes, and addressable graphics. Each character set has 141 upper and lower case symbols. An optional Teletex set is available in ROM or loadable RAM. Special sets and logotypes are also optional. **Philips Information Systems,** San Francisco, CA. **Write 161**

TEST SYSTEM

For Production Test Environments

Designed for integrated circuit testing applications the Inspector 300M controller (I-300M) enables four users to simultaneously run test programs using any combination of the manufacturer's family of test heads. Each test head is totally static and is supported by its own control I/O interface, automatic handling equipment interface, hardware math processor and timing generator. The architecture of the system test heads and the operating system software (MP/M-86 based) enables offline program development, testing and debugging to be done on any station without affecting the operation of any others. All stations can datalog to the standard system floppy disks or to the optionally available hard disk or high speed memory disk. The system uses a dual processor 8085/8088 architecture to allow both 8- and 16-bit programs to run simultaneously. $19,400. **Pragmatic Designs,** Sunnyvale, CA **Write 170**

μC DEVELOPMENT TOOL

Front Display Panel

The Micro Tracer is intended for use with any of the async CRT terminals or microprinters. It displays its data on its panel. A 40-pin clip at the end of an 18" ribbon cable is placed over the μP. Micro Tracer traps data by one of two means: a 16-bit trap address entered via the front panel key-

board, or a separate trigger probe, which can be connected to any logic-level signal in the system. Once captured, the data in the trace buffer can be displayed or printed in sequential processor cycles, or can be disassembled and displayed in assembly mnemonics. Front panel control keys allow any portion of the captured data to be displayed, and data from a single trap event can be redisplayed in either format. **Spywood Systems,** Holliston, MA **Write 173**

FORMAT INTERFACES

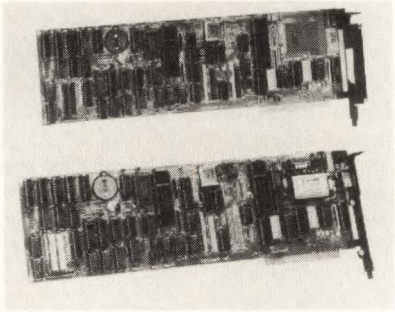
Automatic Formatting Capability

The IBM 5520 interface enables the Workless Station to operate in a bi-synchronous communications mode to the shared resource system. The interface automatically formats the document into IBM 5520 recognizable codes. The universal interface allows operation of the Workless Station with selected RS 232-interfaced computer systems. Both the IBM 5520 and universal interfaces operate on any of the Dest Series 200 page readers from the Model 201 Monofont to the new full-function Model 203 Turbofont. $1,495. **Dest Corp.,** San Jose, CA **Write 171**

FUNCTION BOARDS

For IBM PC

The 2ndMATE and 3rdMATE are two multifunction cards for the IBM PC. 2ndMATE provides two serial ports, two parallel ports, a real time

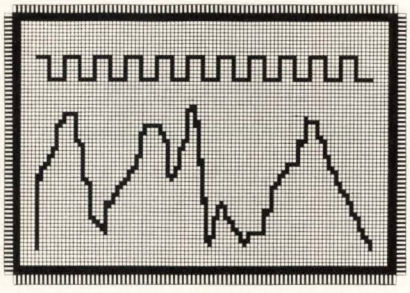


clock/calendar with system-independent battery power, a serial cable, a parallel cable and support circuitry for an optional PAL (programmable array logic). 3rdMATE offers a 300 baud (Bell 103 protocol) direct connect auto-answer modem (using standard RJ-11 modular telephone jack), a serial port, two parallel ports, a battery-powered real time clock/calendar, PAL support circuitry, a serial cable and a parallel cable. The PAL device can be used to provide a unique "fingerprint" that can help protect software or restrict access to files. $295 (2ndMATE), $445 (3rdMATE). **Tecmar, Inc.**, Cleveland, OH **Write 230**

LCD

For Graphics Presentations

The large, 6144 pixel dot matrix LCD graphics presentations is targeted for the portable industrial test and medi-

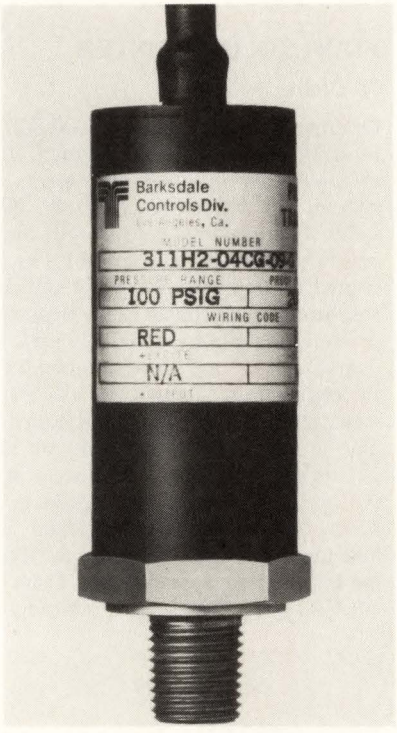


cal instrument markets. The matrix has 64 rows and 96 columns of continuous pixels with dot pitch at 0.044″ for viewing at distances of 6′ and more. The total current AC at 5V is 5μA (typical). The viewing mode can be negative or positive in the transflective or reflective modes. Color is also available as a function of polarizer or filters. The total viewing area is 4.2″×2.8″ with row contacts made on alternate left and right sides; column contacts are made on alternate top and bottom sides. All contacts are on the inside of the glass and on fingers 0.150″×0.100″ centerlines starting 0.050″ off the edge. **UCE, Inc.**, Norwalk, CT. **Write 200**

TRANSDUCER

11 KHz Output

The Series 311 Frequency Output Pressure Transducer directly interfaces with most computers and μP

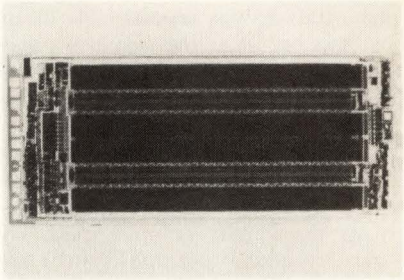


peripherals. It offers output from 1 to 11 KHz for pressure ranges from 0 to 10,000 psi. Options include Bendix connectors, potted free leads, unshielded or shielded jacketed cable. The unit is made with all stainless steel wetted material. It is designed to work with unregulated power supplies from 14 to 32 VDC. **Barksdale Controls**, Los Angeles, CA. **Write 186**

STATIC COLUMN RAM

For High Speed Processing

The Static Column Dynamic RAM, designated the MB8281, features a 64K×1 organization housed in the same 16-pin package used by current 64K DRAMs. The MB8281 has a column address access time of 55 nsecs and a cycle time of 60 nsecs. Chip-select access time is 20 nsecs (max) and the RAS access time is 120nsecs. Power consumption is 28 mW stand-

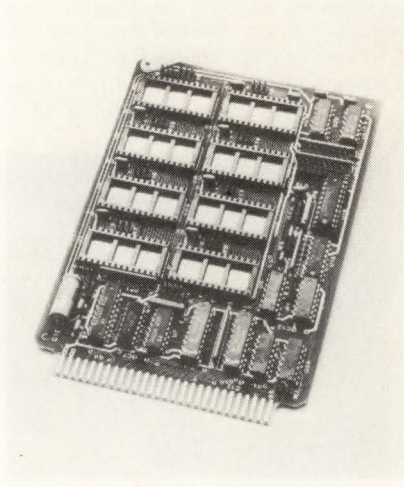


by, and 440 mW in Static Mode. The MB8281 is for high speed image processing and high speed buffer memory applications. It is available in 16 pin DIP or LCC packages for high density mounting. **Fujitsu Microelectronics**, Santa Clara, CA. **Write 203**

MEMORY BOARD

Supports STD Bus Systems

The SB8120 memory board operates with 16- and 20-bit memory addressing schemes, which permits its use with up to 64K bytes of memory for



all 8-bit processors and up to 1 Mbyte for 16-bit μPs of the 8088 type. A feature of the SB8120 is a wait state generator that allows the user to include wait states on a socket-by-socket basis. Others include Memex line support, a choice of 16 memory maps, and address space allocation on a device-by-device basis. The board requires a single +5 V supply. $130. **Micro/sys**, La Canada, CA. **Write 196**

KEYBOARD

For Test Equipment and Control Systems

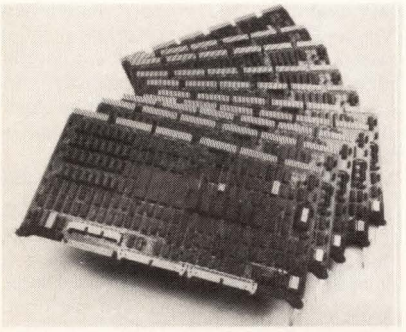
The Microkey Series MK158 keyboard combines conventional keytop sizes and standard ¾″ centers. It has

an operating force of 3.5 ± 1 ounce, a force at release of 1.7 ounces, total travel of 0.055″ (typical) and a profile height of 0.50″. Contact resistance is 200 Ω with a 10 msec contact bounce. The MK158's dome keyswitches are environmentally sealed to extend the keyboard life. Options include daughter board assemblies with standard ASCII encoding and RS232, RS422 interface connectors. Applications include high volume data entry applications including test equipment, μP control systems, medical terminals and equipment, numerical control machines and CRT displays. $68. **Advanced Input Devices,** Coeur d'Alene, ID. **Write 202**

TS-11 EMULATING TAPE CONTROLLER

Buffered Tri-Density

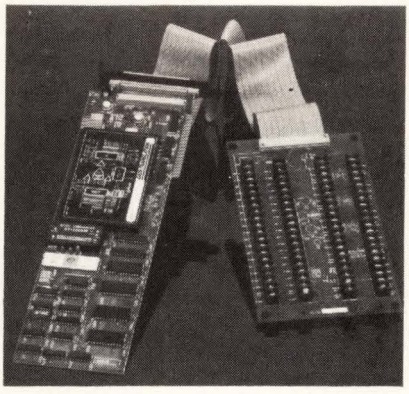
Tape Dimension III is a buffered tri-density (GCR/PE/NRZ1) TS-11 emulating tape controller which is designed to reside in a standard slot within the computer chassis, with no special backplane or cabinet required. The controller is connected to the user-selected formatter via two interface cable connectors. The 64 Kbyte buffer provides total immunity to data late conditions. Tape Dimension III will emulate up to four dual-density Pertec-compatible drives or four tri-density STC or Telex-type drives. Tape transports may be configured with tape speeds up to 125 ips. Recording densities may be intermixed in 9-track 800 bpi NRZ1 format, 9-track 1600 bpi PE format, or 6250 bpi GCR recording format. $1,983. **Western Peripherals,** North Hollywood, CA. **Write 205**



PLUG-IN BOARD LINE

With Programmable Clock

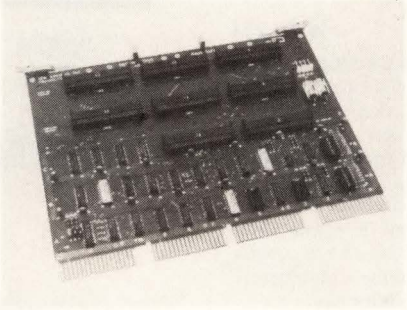
The DT2805, a plug-in data acquisition board, features low-level software selectable gains of 1, 10, 100 and 500. The board is a single board analog and digital I/O system which has 8 differential or 16 single-ended channels of 12-bit A/D, 2 channels D/A, 16 lines of digital I/O and an on-board programmable clock. $1,195. **Data Translation,** Marlboro, MA. **Write 188**



LONG LINE ADAPTER ASSEMBLY

Unibus And Q-bus DR11 W modules

The Long Line Adapter Assembly, designated the MDB/MLSI-WLL11, allows DR11-W high speed DMA I/O interface modules for Unibus, VAX and Q-bus computers to operate peripherals up to 1,000 feet away from the CPU. The quad-sized module converts standard TTL signals originating from the MDB DR11-W module to differential (RS-422) signals. It also converts differential to TTL signals, for use by the MDB-DR11-W modules. Design features include a pluggable jumper pack that provides for proper bus grant and DMA priority signals pass through, depending upon whether the module is inserted into a Q-bus or Unibus backplane. Included are a dual size, long line test board and test cables. **MDB Systems Inc.,** Orange, CA. **Write 189**



DISK CONTROLLER

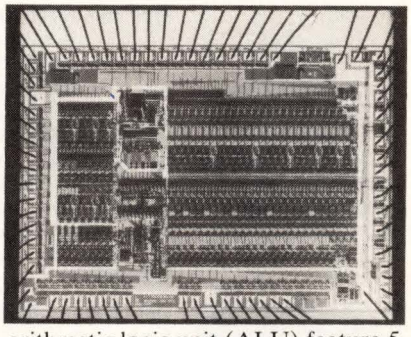
Multibus Compatible

The Rimfire 50 features an on-board processing system including an Intel 80186 16-bit μP, 16K bytes of PROM, up to 32K bytes of optional buffer RAM and a high speed (2MHz) disk interface with DMA. Two independent DMA devices, one internal to the 80186 and one discrete, transfer data simultaneously from the disk to the buffer and from buffer to system memory. Rimfire 50 employs a dual function ECC circuit and can generate two independent interrupts, which may also be polled. Features include an Attach command, whereby the controller will attach, or establish communications with, another system peripheral controller. $1,685. **Computer Products Corp.,** Plymouth, MA. **Write 199**

FLOATING POINT CHIP SET

With Software Portability

The WTL1032 floating point multiplier and the WTL1033 floating point arithmetic logic unit (ALU) feature 5-Mflop performance and compatibility with the proposed IEEE 754 floating-point standard, as well as 32-bit circuits which use low-power NMOS technology. The WTL1032/1033 chip set has add, subtract, multiply and absolute value capabilities, and handles conversion to and from 24-bit fixed-point arithmetic. The two chips combine all floating point functions and can operate in either pipeline or flow-through modes and have complete software portability. Inputs and outputs are fully registered, with separate load and unload controls. $325. **Weitek Corp.,** Palo Alto, CA. **Write 206**



New Products • COMPONENTS

A/D CONVERTER

μP-Compatible

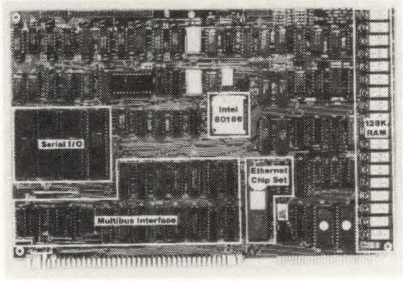
The MN574A is a 12-bit, high-speed, successive approximation A/D converter that contains the interface logic

and control circuitry necessary to directly mate with most 8- and 16-bit μPs and μCs. A silicon-gate CMOS gate array is used to implement all address-decoding, chip-select, R/W control, and output data formatting and three stating. Also included on the array is the converter clock circuit and the successive approximation register required to implement the complete 12-bit A/D conversion function. The MN574A is a 12-bit A/D converter with an internal clock and a 25 μsec conversion time. Six versions of the device are available which cover 0°C to +70°C and −55°C to +125°C temperature ranges. The MN574A is TTL compatible, requires ±15V (or ±12V) and +5V supplies, and consumes a maximum of 725 mW. **Micro Networks**, Worcester, MA. **Write 191**

μC MICROCOMPUTER HARDWARE AND SOFTWARE

Includes Ethernet Chip Set

The 8086-based system has been upgraded to include a Multibus expan-



sion board that supports the Intel Ethernet chip set, four additional RS-232 serial ports, ALTOS-NET, and a 1200 baud modem. Software based in the 586's main memory provides IBM 3780 and 3270 bisynchronous terminal emulation capabilities. The expansion board runs under the XENIX operating system, has an 80186 processor and 128 Kbytes of RAM memory. $1,450. **Altos Computer Systems,** San Jose, CA. **Write 204**

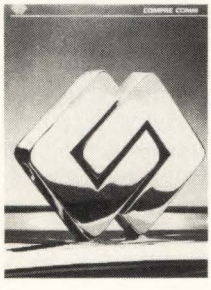
DISK DRIVE CONTROLLER

For 5.25″ Winchesters

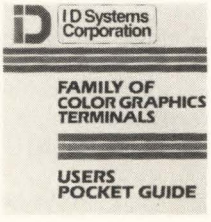
Features of the S1410A 5.25″ Winchester disk drive controller include automatic multisector transfer handling, a full-sector buffer, automatic seek and verify, fault detection, and error detection and correction. The S1410A controls two 5.25″ Winchester drives and connects to a host via the industry-standard SASI interface. The Winchesters' characteristics can be programmed into the controller. Programmable functions are fast step mode, sector size, sector interleave, and number of cylinders and heads. **Xebec,** Sunnyvale, CA. **Write 198**

New Literature

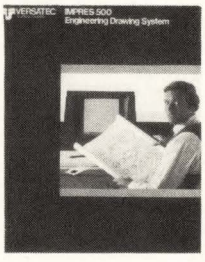
Tape Recorder Brochure. An eight-page product information brochure describes the features of Honeywell's Model 101, a large-reel, high-performance IRIG portable recorder with μC control and built-in calibration facility. The brochure diagrams the μC control system and details the programmable functions, data electronics, reeling system, and auto-test feature. Remote control options and accessories are also listed.
Honeywell **Write 254**



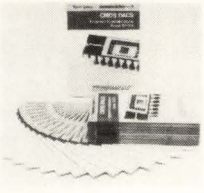
Data Communciations Catalog. Compre Comm Inc. offers an eight-page product catalog which describes their line of data communications equipment. The catalog includes a review of the implementation of the Data Xchange, Data Express, and Bi-Link statistical data concentrator families into information systems in which terminals are remotely located. Also covered are the ME-2 series of modem eliminators, and the MM-4 modem multiplier.
Compre Comm **Write 255**



User's Pocket Guide. ID Systems Corp., producer of color graphics computer terminals, offers a guide which explains set-up features, operations, and commands for the VT 100 color graphics computer terminal. The "User's Pocket Guide" also includes a complete, technical description of the product.
ID Systems **Write 262**

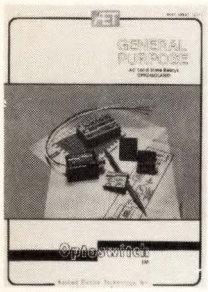


Scan/Edit/Plot System Brochure. This brochure describes a scan/edit/plot system for micrographics, reprographics, design and drafting. The brochure shows how Versatec's Impres 500 engineering drawing system digitizes aperture card images, displays locally stored images, supports interactive CAD drawing and editing functions, and sends image data to local or remote Versatec electrostatic plotters.
Versatec **Write 266**

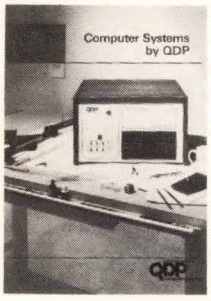


Application Bulletin On CMOS DACS. The 12 page bulletin discusses the design and application problems a user will have in applying high resolution DAC's. Discussions include DAC design and the trade-offs using R-2R, segmentation, and binary weighting. Also covered are application problems of temperature stability, output capacitance, settling time, digital feed-through, grounding, and output offset.
Hybrid Systems **Write 267**

Control Systems Brochure. This brochure from Liebert describes the Deluxe System/3 environmental control system. Features include five control systems, fan deck assembly, semi-hermetic dual compressor system and a precision heat rejection selection capability. It has a LED numerical display and a manual compressor sequence switch to change the lead/lag sequence of the compressors.
Liebert **Write 268**

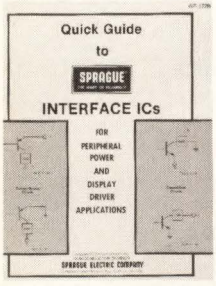


Solid State Relay Catalog. The Optoswitch solid state relays are encapsulated and recommended for harsh industrial environments where high shock or severe temperature excursions are encountered. Typical applications include industrial controls, process control systems, machine tools, traffic controls, computer peripherals, heat controls, sensors and such inductive load uses as solenoids, motors and transformers.
Applied Electro Technology **Write 256**

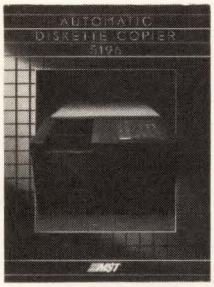


μC and Peripherals Brochure. Product information on the QDP-100, QDP-200 and QDO-300 μC systems and add-ons is included in a data package. Systems offer modular construction with an S-100 (IEEE-696) bus and up to six slots for expansion. RAM capability is 64KB to 512 KB with up to 16KB of EPROM. Other features are input buffering, improved cache memory for faster disk transfers and advanced utility programs.
QDP **Write 257**

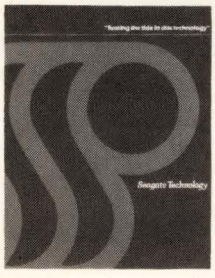
Statistical Multiplexers Data Sheet. This new data sheet describes the DP-1000 statistical multiplexer, which allows a user to mix eight asynchronous terminals on each end of a line. Features include a capability for the user to set individual ports to accommodate various terminal characteristics such as speed, flow control delay for mechanical response, line feed insertion and echoplex. The multiplexer has a bit-oriented protocol.
Dynapac **Write 259**



Quide To Interface IC's. This is a short-form guide to interface integrated circuits for peripheral power and display driver applications, Form WR-172B. The guide contains a list of the current-sink drivers and current-source drivers available for use with LED, vacuum-flourescent, gas-discharge and incandescent displays; inductive loads, including solenoids and motors, and thermal and electro-sensitive printers.
Sprague Electric Company **Write 260**



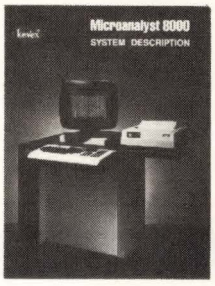
DEC-Compatible Copier Brochure. The data sheet describes how Model 5196 DEC-compatible diskette copier automates the copying of 5¼", 96 TPI diskettes in DEC RX-50 format. The 5196 is a complete desktop, standalone duplication system that automatically copies, verifies, and sorts diskettes. The 5196 features automatic two-level sorting that processes accepted and rejected diskettes into separate bins.
Media Systems Technology **Write 261**



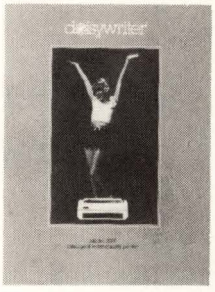
Winchester Disk Drive Brochure. This 12-page brochure from Seagate Technology describes 5¼" Winchester disk drives for μP-based personal computers, workstations, small business systems and word processors. The brochure illustrates and describes the manufacturing facility and production process as well as test procedures for head assemblies and active and passive electronic devices.
Seagate **Write 251**

Add-On Products Brochure. This brochure describes add-on and add-in products for the DEC Professional 300 Series personal computers, peripheral interfaces, disk controllers, and memories. Featured are an LP11 type line printer controller with cable for a Centronics compatible printer interface, an SMD controller, a DH11 type multiplexor, bus expansion chassis, 256KB memory, 8 inch floppy controller, and 5.25" winchester controller.
Pick **Write 269**

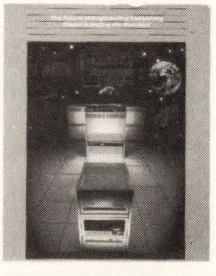
Desktop Computer Brochure. This brochure describes the Sord M343 Mark 41 desk top computer with an 8086 μP and 8087 floating processor for high speed arithmetic functioning. Sections on job system expansibility and color graphics are detailed as well as a selection of software such as an information management system that handles a range between spreadsheets and large scale data management.
Sord **Write 270**



Microanalysis Literature. The 20-page brochure is for the Kevex Microanalyst 8000, a system designed for x-ray microanalysis, as well as the analysis of all other signals available from today's electron columns. The brochure focuses on the power of the Quantex-Ray II software, on digital imaging as a key element of modern microanalysis, and on the design features of the 8000 including its multilingual capability and voice recognition package.
Kevex Corp. **Write 271**



Printer Brochure. This brochure describes the Daisywriter, a Z80-based computer-optomized printer interface and emulation system. It has a built in buffer memory of 16 Kbytes and CRT hard copy printout that allows dumping the full screen display instantly. Fifty interface signals and matching computer cable offer plug to plug compatibility. Other features are automatic margin justification, proportional spacing, and self diagnostic test.
Daisywriter **Write 272**



CAD/CAM Brochure. Digital's 16 page brochure is an overview of their products for the engineering CAD/CAM market including networking, databases, and 32-bit Vax architecture. A section on electronics engineering is devoted to the design of integrated circuits, printed circuit boards, and μP software. CAM, mechanical CAD, and finite element analysis are featured in the pages on mechanical engineering.
DEC **Write 264**

CMOS 80C86 Brochure. A 24-page shortform catalog describing the 16 bit, CMOS 80C86 μP family. The book is an overall look at the 80C86 family as well as individual product briefs on each industry standard device offered. Products highlighted in the book include: the 80C86 CMOS 16 bit μP, 82C82 CMOS octal latch, 82C54 CMOS programmable interval timer, and the 82C55A CMOS programmable peripheral interface.
Harris **Write 265**

Calendar

September 13–15

Midcon/83. High Technology Electronics Exhibition and Convention, Cobol Hall, Detroit, MI. Contact: Electronic Conventions, 8110 Airport Blvd., Los Angeles, CA 90045.

September 13–15

Mini-Micro-Midwest. O'Hare Exposition Center, Rosemont, IL. Contact: Electronics Conventions, 8110 Airport Blvd., Los Angeles, CA 90045.

September 19–23

IFIP '83. International Federation For Word Processing, Paris, France. Contact: CESV–Logotour, 1 Rue Jules-Lefévre, 75009, Paris.

September 19–23

Sixth International Conference on Digital Satellite Communications. Hyatt Regency, Phoenix, AZ. Contact: Conference Administrator, ICDSC-6 c/o Comstat, 950 L'Enfant Plaza, SW Washington, DC 20024.

September 19–21

Electronic and Aerospace Systems Convention. Shoreham Hotel, Washington, DC. Contact: Dr. John M. Walker (301) 765-7491.

September 19–22

International Conference on VLSI in Computers. New York Hilton, NY. Contact: Harry Hayman (301) 589-8142.

September 20

Mid-Term '83. Integrated Circuit Industry. Sheraton Tara Hotel, Framingham, MA. Contact: ICE, Pat Fruscello (602) 998-9780.

September 20–22

Nepcon Northwest '83. San Jose Convention Center, San Jose, CA. Contact: Dennis P. Stanczack (312) 299-9311.

September 20–22

Semicon East '83. Hynes Auditorium, Boston, MA. Contact: Mary Beth Kern (415) 964-5111.

September 22–25

New York Computer Showcase Expo. New York Colliseum. Contact: The Interface Group (617) 879-4502.

September 20–22

Informatics Carribean Exhibition and Conference. San Juan, Puerto Rico. Contact: Informatics, 3421 M St. N.W. Suite 219, Washington, DC 20007.

September 26–28

CompCon Fall '83. Delivering Computer Power to End-Users. Marriott Crystal Gateway Hotel, Arlington, VA. Contact: COMPCON Fall '83, Box 639, Silver Spring, MD 20901.

September 26–28

Maecon '83. High Technology Electronics Exhibition and Conference Convention Center, Kansas City, MO. Contact: Kent Keller (213) 772-2965.

September 27–29

Semiconductor/UK. National Exhibition Center, Birmingham, England. Contact: Ed Troogstad (312) 299-9311.

September 29–October 2

San Francisco Computer Showcase Exposition. Brooks Hall, San Francisco, CA. Contact: David Sudkin (617) 879-4502.

September 29–October 1

CP/M '83 East. Hynes Auditorium, Boston, MA. Contact: Northeast Expositions, 822 Boylston St., Chestnut Hill, MA 02167.

Advertiser Index

ADAC 73
Artel 63
Associated Computer Consultants 17
Aydin 47

CADCON EAST '83 95,107
Cambridge Digital Systems 93
Chrislin Industries 91
Comtal 61
Control Data 27

Data Systems Design C4
Datasouth 46
Dataram 75
Datel/Intersil 69
Decmation 62
DEXPO West '83 83
Distributed Logic 1
Dy4 Systems 60

Emulex 35,67
Epson America C3

Floating Point Systems . 19,20,21

Graphics Development Labs 87

Hecon 87
Heurikon 6
Hewlett Packard 9

IKIER Technology 42
Interactive Structures 13

Lexidata 39
Lundy 7

Matrox 44
MDB Systems 4
Modgraph 41
Monolithic 14

National Industries 109
Nicolet-Zeta 49
NSG America 8
Numerix 45
Power/Mate 55

Princeton Graphics 58
Pro-Log 25

Qantex 81
Qume 2,3

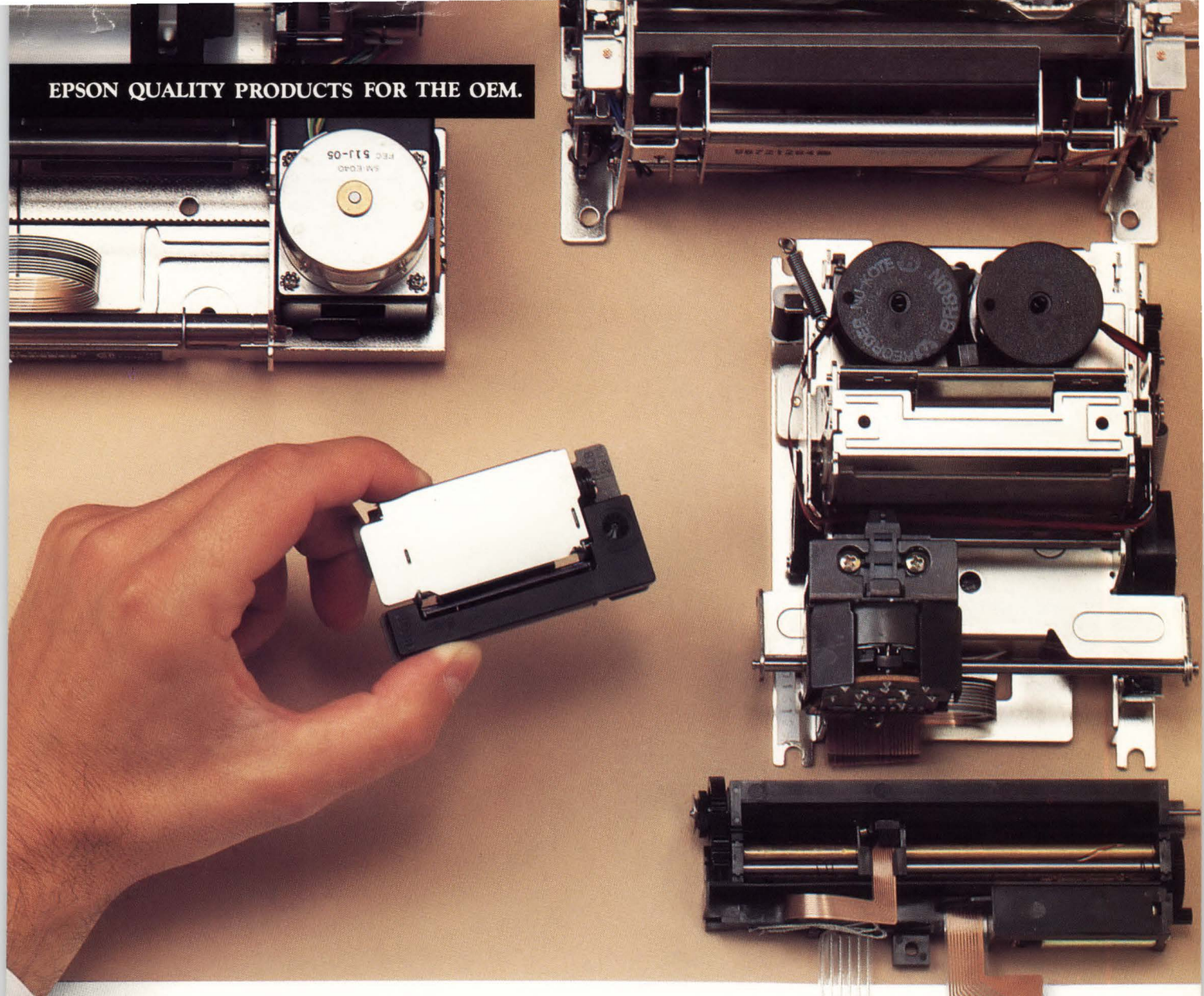
Relms 43
Rixon 79

Scherer's Mini Computer Mart 111
SD Systems 51
Seiko 11
Selanar 57
Sigma Information Systems . . . 77
Summagraphics 22

Teleram Communications 53
Triad-Utrad 59

Universal Semiconductor C2

Western Peripherals 31



EPSON PRINTER MECHANISMS: THEY COME WITH A HELPING HAND.

PORTABLE/HAND-HELD COMPUTER PRINTERS				
Model	**Head**	**Columns**	**Speed**	**Weight**
M1XX	Impact Shuttle	16 to 40	0.4 to 0.7 LPS	2.1 oz
M2XX	7 wire impact	21 to 31	2.4 LPS	28.0 oz
M5XX	7 wire impact	40	3.0 LPS	59.0 oz
M12XX	Thermal	40	0.5 LPS	5.2 oz
M3XXX	9 wire impact	80	80 CPS	4.4 lb

You've heard that Epson delivers more printer mechanisms than anyone else. That's true. More than 600,000 shipped per month.

You've heard that our out-of-box failure rate is measured in 10ths of a percent. True again.

But maybe you're concerned that the leader in ECR and POS printers is too busy to worry about your application. *Not a chance!*

That's how we got where we are. By caring about your problems. Lending you a helping hand in selecting a printer for your application. Helping you package it as an integral part or as a stand-alone. And always delivering a cost-effective, quality solution. On schedule.

The printer mechanisms shown here can easily be designed into portable and hand-held computers. We have many more. In many variations. For many applications. Call or write us today. Let us start by giving you a helping hand.

SW Region (714) 751-1919 • **NW Region** (408) 985-8828 • **SE Region** (404) 458-9666
NE Region (617) 245-8007 • **CENTRAL Region** - (815) 455-2570

EPSON

EPSON AMERICA, INC.

OEM Products Division
Printer Group
3415 Kashiwa Street, Torrance,
CA 90505 (213) 534-0360
Telex: 182412

Write 51 on Reader Inquiry Card

IF YOU'RE GOING TO MAKE IT DEC-COMPATIBLE, IT BETTER BE BETTER.

Some people think using anything other than Digital disk systems with Digital CPUs is nothing but trouble.

We think differently.

We know there's no sense making something DEC®-compatible unless you can make it better. Especially in the three critical areas of compatibility, reliability, and service.

That's why, while our floppy systems, Winchesters, and controllers start out being fully DEC-compatible, it's our advanced technology and design techniques that take them beyond mere compatibility.

What's more, they're more reliable. We use Winchesters, which are inherently reliable, the best floppy drives made, significantly fewer parts, and extensive burn-in procedures to make sure.

Even so, all this would mean nothing without better service and support. That's why we offer DSD exclusives like on-board self-diagnostics. A hotline to our remote diagnostic technicians. And a twenty-four hour or less module swap that just might change the way you think about the need for conventional service. Not to mention its cost.

We also offer one of the most comprehensive—yet inexpensive—extended service agreements in the industry.

Finally, all these products are priced economically, making them that much more sensible to own.

We do all this because we want you to buy our disk systems with as much confidence as you buy Digital's. And after all, why shouldn't you? We not only make them DEC-compatible, we make them better.

For complete information about our floppy systems, Winchesters or controllers, just contact us.

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. Eastern Region Sales and Service: Norwood, MA, (617) 769-7620. Central Region Sales: Dallas, TX, (214) 980-4884. Western Region Sales: Santa Clara, CA, (408) 727-3163.

DATA SYSTEMS DESIGN

Write 52 on Reader Inquiry Card

INTERNATIONAL SALES: Australia 03/544 3444; Belgium and Luxembourg 02/7209038; Canada 416/625 1907; Denmark 02/63 22 33; Finland 90/88 50 11; France 03/411 5454; Hong Kong and Peoples Republic of China 03/696231; Israel 52-52444; Italy 02/4047648; Japan, Osaka 06/323 1707, Tokyo 03/345 1411; Netherlands 02977-22456; New Zealand 04/693 008; Norway 02/78 94 60; Singapore, Malaysia, and Indonesia 2241077; Spain 01/433 2412; Sweden 08/38 03 70; Switzerland 01/741 41 11; United Kingdom 7073/34774; West Germany and Austria 089/1204-0; Yugoslavia 61/263 261