

Digital Design

National Computer Conference 1983

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 5/83

Industry Spotlight: Laura Conigliaro on Robotics

• Gate Arrays • Modems • Supercomputers

VOL. 13
NO. 5

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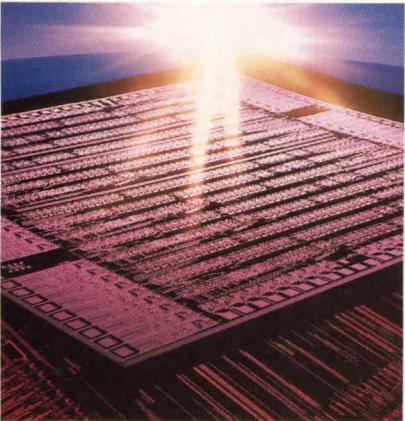
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Write 3 for LSI-11; Write 5 for PDP-11

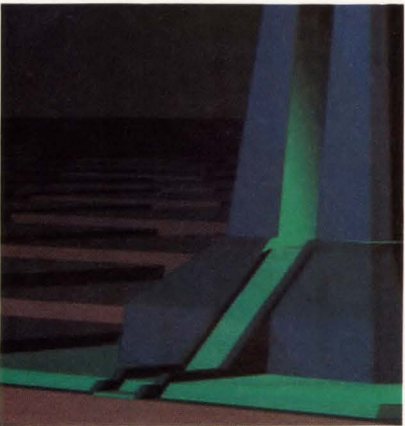
Digital Design



p. 32 (photo courtesy Cincinnati Milicron)



p. 59 (courtesy National Semiconductor)



p. 94 (photo courtesy Digital Productions)

Cover

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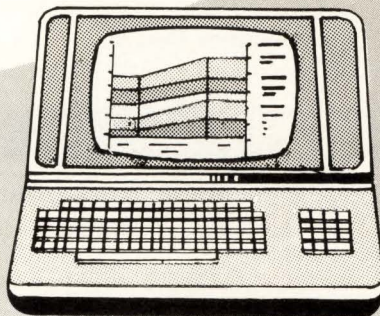
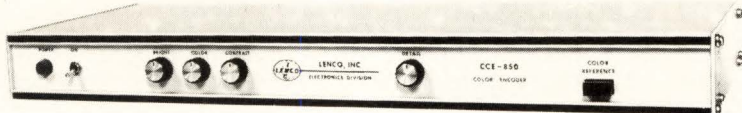
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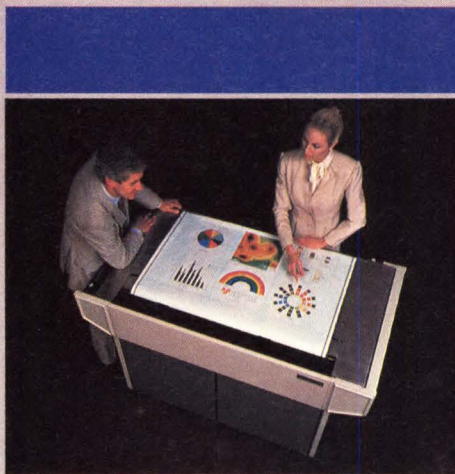
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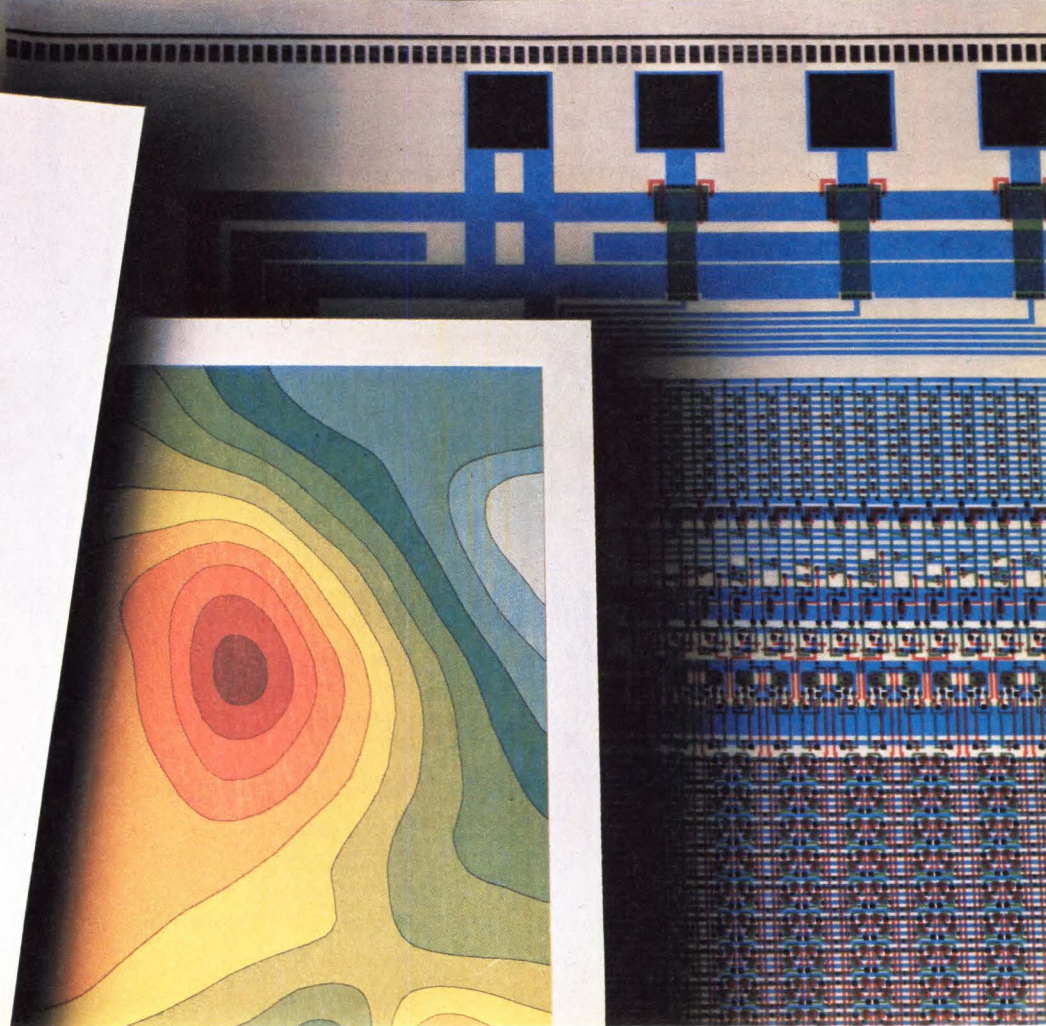
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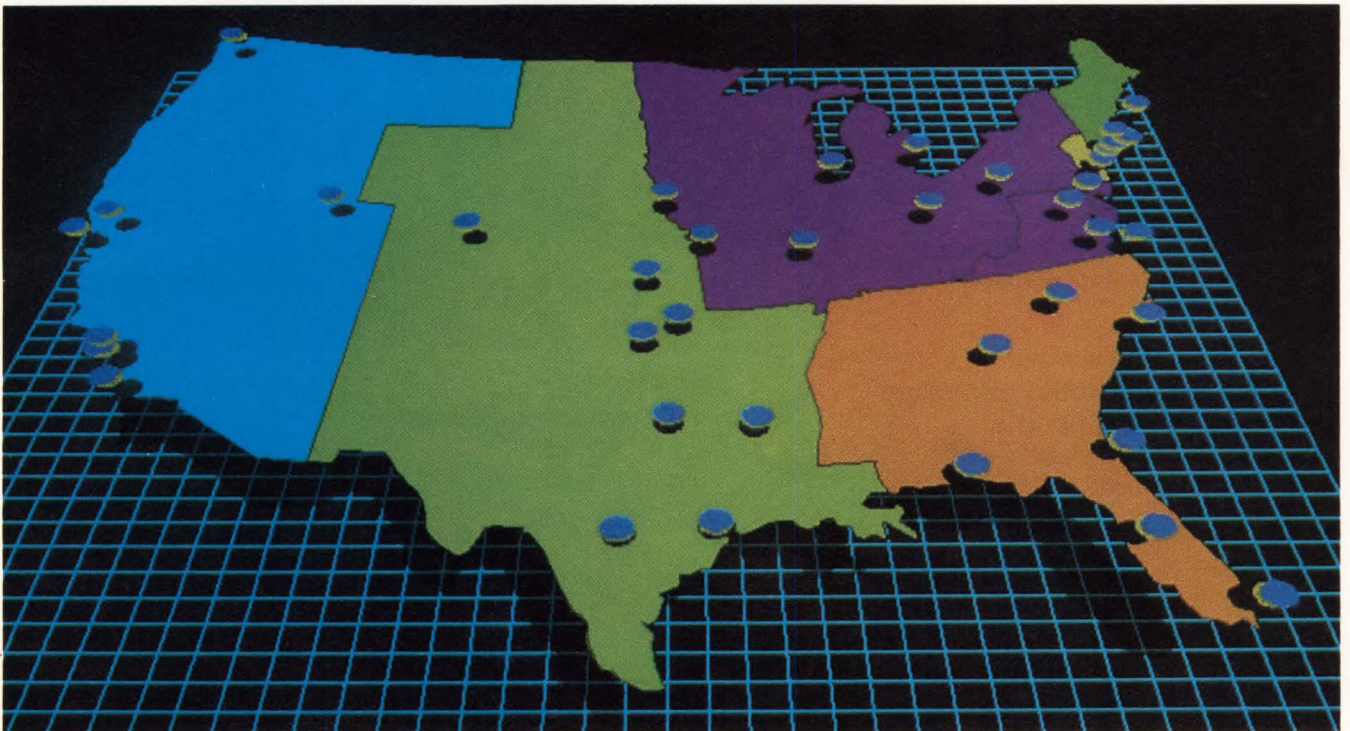
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LUNDY

The Lundy service map was generated on a Lundy T5688 raster terminal. Both Lundy products and Lundy service set industry standards.



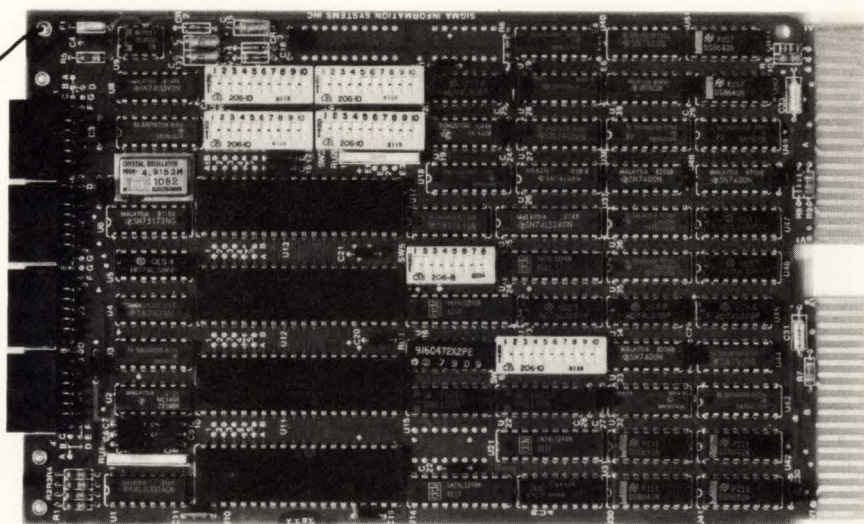
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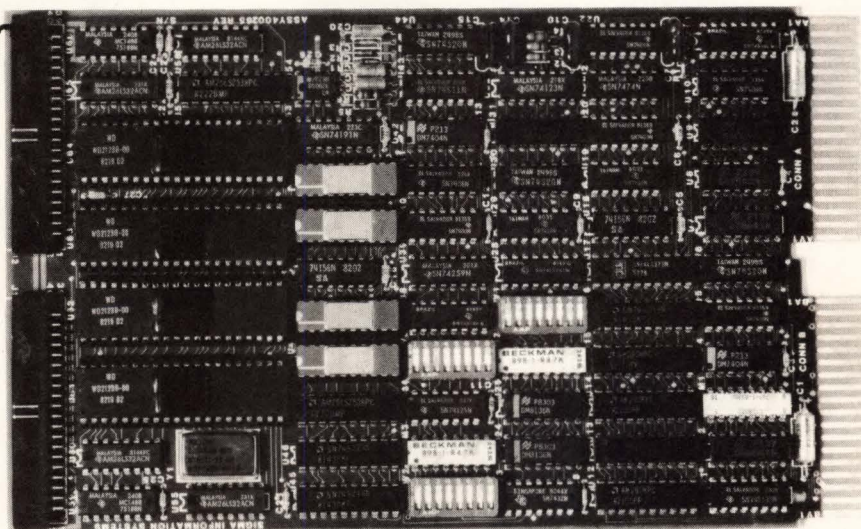
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Dear Editor:

Your March 1983 "News Update" use of the term "Japscam" is totally inappropriate. "Jap" (and your derivation, "Japscam") is a racial slur. This type of racist reporting falls below minimal professional journalistic standards, and it denigrates the engineering profession as well. Sir, you owe all of us an apology.

Larry Widigen
2918 Paseo del Refugio
Santa Barbara, CA 93105

Ed. Reply: We apologize to those who were offended by the term "Japscam" in our March News Update. It should be noted, however, that the term was enclosed in quotation marks to indicate that it was a colloquial term not coined by our staff, who were merely reporting the facts—one of which was that the controversy was commonly referred to as "Japscam." Also, it is our opinion that whoever

coined the term "Japscam" was probably following the trend to describe any national controversy by the first syllable of the country followed by "scam." As such, "Japscam" is probably as devoid of racist intent as would be "Amscam," "Mexiscam" or "Canscam".

Dear Editor:

Since we believe that Raster Technologies currently enjoys the distinction of being the fastest-growing supplier of intelligent color graphics controllers, we were quite surprised that we were omitted from your article on color graphics terminals and workstations in the February issue of *Digital Design*. Raster Technologies offers the fully compatible Model One family of color graphics controllers using 64K RAM memories for superior price/performance. (In fact, Raster was the first to use 64K RAM chips; its architecture was specifically de-

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Readers of *Digital Design* who wish further information should contact me directly.

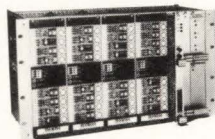
Roger P. Nielson
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Errata

The diagram used to lead our February feature on ergonomics (p. 24) ran without a credit line. The diagram was derived from a photograph supplied courtesy of Wright Line, Inc. *Digital Design* regrets the oversight.



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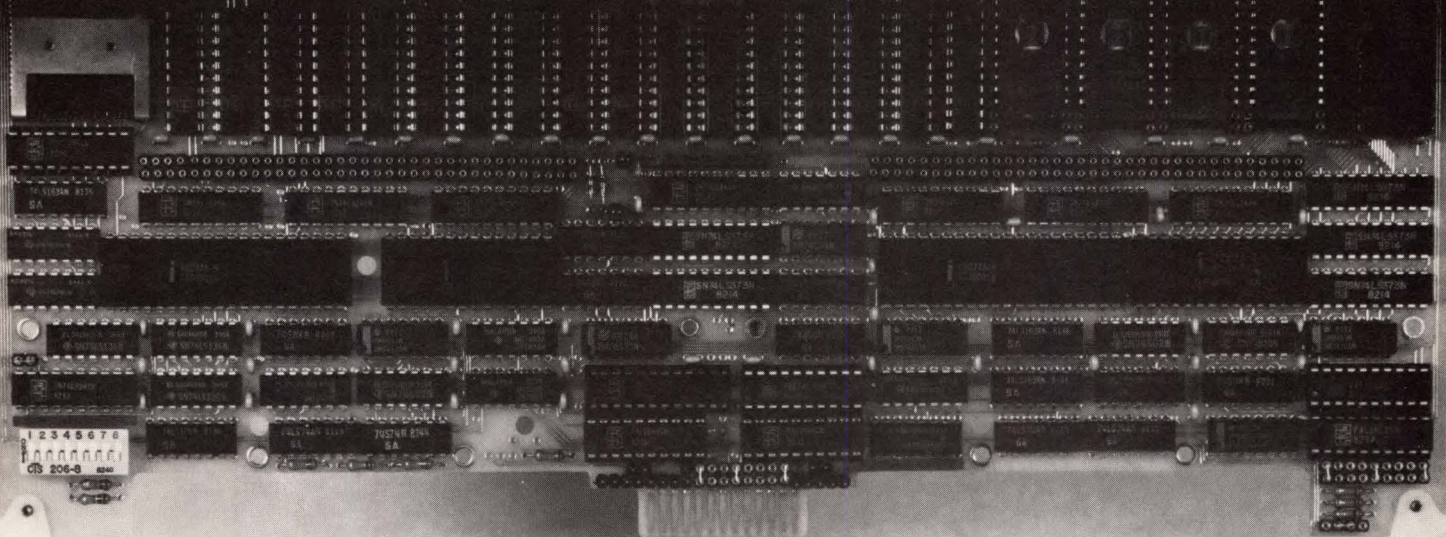
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June 1-3

ICA Conference & Expo. Anaheim Convention Center, Anaheim, CA. Contact: ICA (301)656-5794.

June 2

Personal Computer Workshop. Charlotte, NC; June 16-18, Reston, VA. Contact: CEC, Virginia Tech., Blacksburg, VA 24061. (703) 961-4848.

June 2-5

Seattle Computer Showcase Exposition. Seattle Center. Contact: The Interface Group (617)879-4502.

June 5-8

International Summer Consumer Electronics Show. McCormick Place, Chicago, IL. Contact: William Glassgow (312)861-1040.

June 6-7

IC Processing Techniques & Ion Implantation. Hyatt Palo Alto, Palo Alto, CA. Contact: Dept. 564 N, U of C Ext., 2223 Fulton St., Berkeley, CA 94720. (415) 642-4151.

June 6-10

Optical Storage Conference. Arlington, VA. Contact: SPIE, P.O. Box 10, Bel-
lingham, WA 98227. (206) 676-3290.

June 6-8

Interexpo. Monterrey, Nuevo Leon, Mexico. Contact: SME, One SME Drive, Dearborn, MI 48121. (313) 271-0023.

June 6-10

Cell Designer Course. Melbourne, FL. Contact: Harris Corp., P.O. Box 883, Semiconductor Group, Melbourne, FL 32901. (305) 724-7800.

June 6-12

Microprocessor Application Course. MIT, Cambridge, MA. Contact: MIT, 105 Mass. Ave., Cambridge, MA 02139. (617) 253-7406.

June 7-9

The Office Automation Show. Barbican Centre, London, England. Contact: Phone (301)657-3090.

June 7-9

Industrial Exposition. Milwaukee Exposition Ctr., Milwaukee, WI. Contact: SME, One SME Dr., Dearborn, MI 48128. (313) 271-0023.

June 7-10

Hong Kong Computer '83. Wanchai, Hong Kong. Contact: Terry Hill, Industrial and Trade Fairs International, Ltd. Radcliffe House, Blenheim Court, Solihull, West Midlands B91 2BG UK. (021)705-6707.

June 7-10

Network Design Course. Washington, D.C. Contact: ICS, 3304 Pico Blvd., Santa Monica, CA 90405. (213) 450-2060.

June 8-9

Robotics Overview. Indianapolis, IN. Contact: John McEachran (313)271-1500.

June 8-10

Computer Showcase Exposition. H. Roe Bartle Hall, Kansas City, MO. Contact: David Sudkin (617)879-4502.

June 8-10

X.25 Seminar. Hyatt Regency Crystal City, Arlington, VA. Contact: TTI, 741 10th St., Santa Monica, CA 90402. (213) 394-8305.

June 9-11

Microcomputer Education Workshop. Waretown, CT. Contact: TERC, 8 Eliot St., Cambridge, MA 02138. (617) 547-3890.

June 13-15

Production Project. Rochester, NY. Contact: The University of Rochester, Rochester, NY 14627. (716) 275-3106.

June 13-16

ATE East Conference. Hynes Auditorium, Boston, MA. Contact: Katherine Bochonko, Morgan-Grampian Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215. (212)340-9780.

June 13-16

Syntopican XI. San Francisco, CA. Contact: James L. Donlo, International Information/Word Processing Association, 1015 N. York Rd., Willow Gr., PA 19090. (215)657-6300.

June 13-16

Data Aquisition Seminar. Sunnyvale, CA. Contact: Continuing Education Institute, Oliver's Carriage House, 4510 Leaf Treader Way, Columbia, MD 21044. (301)596-0111.

June 13-17

Power Electronic Course. Los Angeles, CA. Contact: TESLaco, 490 S. Rosemead Blvd., Pasadena, CA 91107. (213)795-1699.

June 14-16

AFCEA 37th Annual Convention. Sheraton Washington, Washington, DC. Contact: John Spargo (703)820-5028.

June 14-16

Ohmcon '83. Contact: Jerry Fossler, Electronic Conventions, 8110 Airport Blvd., Los Angeles, CA 90045. (213)772-2965.

June 14-16

International Information/Word Processing Syntopican. Moscone Center, San Francisco, CA. Contact: H.G. Asmus (201)444-0505.

June 14-16

International Robot Conference. Long Beach Convention Center, Long Beach, CA. Contact: Bill Harrington (312)668-8100.

June 14-18

Technology Exhibition. Earls Court Exhibition Ctr., London. Contact: Radcliffe House, Blenheim Ct., Solihull, West Midlands, B912B6. (021) 705-6707.

June 14-18

Techtronica '83. Earls Court Exhibition Center, London, England. Contact: Industrial and Trade Fairs Ltd. (021)705-6707.

June 15-18

EMC Workshop. Washington, DC. Contact: Don White Consultants Inc., (703) 347-0030.

June 17-19

PC '83. San Francisco, CA. Contact: The National Computer Shows, Boylston St., Chestnut Hill, MA 02167. (800)841-7000.

June 20-22

Symposium on Computer Arithmetic. Aarhus, Denmark. Contact: Prof. T.R.N. Rao, USL, Box 44330, Lafayette, LA.

June 20-July 15

CE '83. Princeton, NJ. Contact: Institute for Professional Development, 245 Nassau St., Princeton, NJ 08540. (609)924-8333.

June 20-24

Seminar on Computer System Implementation. Jamestown, NY. Contact: Camconco, P.O. Box 53, Berne, NY 12023. (518)872-2426.

June 22-24

Computerama '83. Automotive Exhibition Place, Toronto, Ontario, Canada. Contact: James Mahon (416)967-6200.

June 23

ACM Symposium. Red Lion Motor Inn, Sacramento, CA. Contact: A. Hankinson, B266 Technology Bldg., National Bureau of Standards, Washington, DC 20234. (301)921-2208.

June 21-22

Digital Filters and Spectral Analysis Course. San Diego, CA. Contact: Ruth



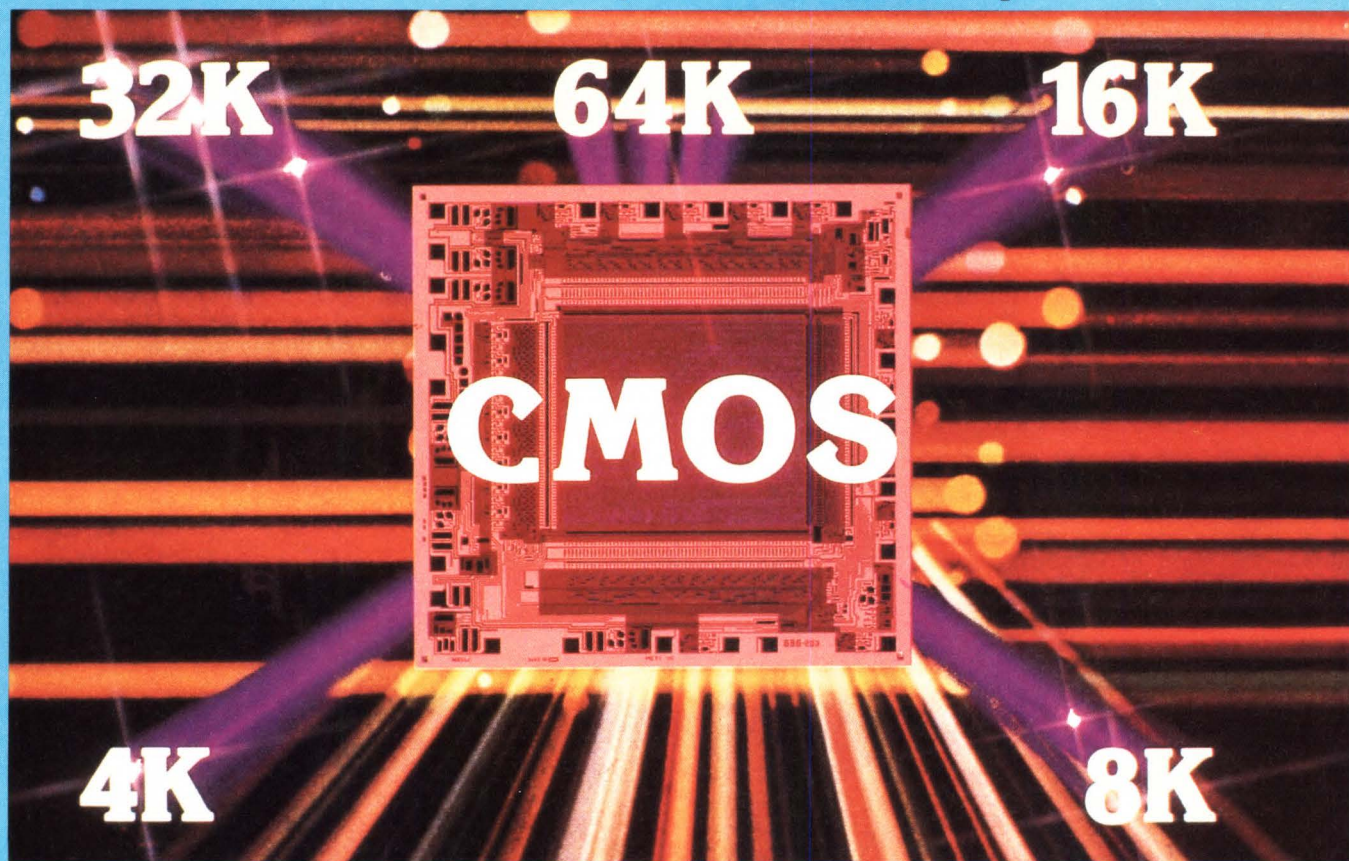
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Dordick, Integrated Computer Systems, 3304 Pico Blvd., Santa Monica, CA 90405. (213)450-2060.

June 26-30

National Computer Graphics Association. Chicago, IL. Contact: Nancy Lefebvre, NCGA, 8401 Arlington Blvd., Fairfax, VA 22031. (703)698-9600.

June 26-29

ACM/IEEE Design Automation Conference. Fountainbleu Hotel, Miami Beach, FL. Contact: American Federation of Image Processing Societies (301)589-8142.

June 27-29

Design Automation Conference. Fountainbleu Hotel, Miami Beach, FL. Contact: Hillel Ofek, IBM Corp., Columbia St., Poughkeepsie, NY 12602. (914)485-7763.

June 27-29

Localnet '83. The New York Hilton, New York, NY. Contact: On-Line Conference (212)563-1000.

June 27-29

Videotex '83. The New York Hilton, New York, NY. Contact: London On-Line Inc., 1133 Avenue of the Americas, New York, NY 10036. (212)692-9003.

June 27-July 1

Laser '83 Opto-Electronik. Trade Fair Center, Munich, Germany. Contact: Lallman Associates (201)652-7070.

June 28-30

Symposium on Fault-Tolerant Computing. Jolly Hotel, Milano, Italy. Contact: Luca Simoncini, I.E.I. C.N.R., Via Santa Maria 46, I-16100 Pisa PI, Italy +39 50 500159.

July 4-5

Optical Imaging Systems Meeting. International Conference Center, Kobe, Japan. Contact: Dr. Ichiro Kitano, Nippon Sheet Glass Co. Ltd. 1, Kaido Shita Konoiki, Itami, Hyogo 664 Japan.

July 8

System Documentation Seminar. Seattle, WA. Contact: TCA, 1250 Oakmead Pkwy., #210, Los Angeles, CA (800)792-0990.

July 9-12

NCC Board Conference. Las Vegas, NV. Contact: Ann-Marie Bartels, 1815 N. Lynn St., Arlington, VA 22209. (703)558-3641.

July 11-13

Summer Computer Simulation Conference. Hyatt Regency, Vancouver, B.C.,

Canada. Contact: The Society for Computer Simulation, P.O. Box 2228, La Jolla, CA 92038. (714)459-3888.

July 11-15

Digital Signal and Image Processing Course. Washington, DC. Contact: Integrated Computer Systems, 3304 Pico Blvd., Santa Monica, CA 90405. (213)450-2060.

July 12-13

Fiber Optics Course. Hyatt Regency Montreal, Canada. Contact: Information Gatekeepers Inc. (617)739-2022.

July 17-22

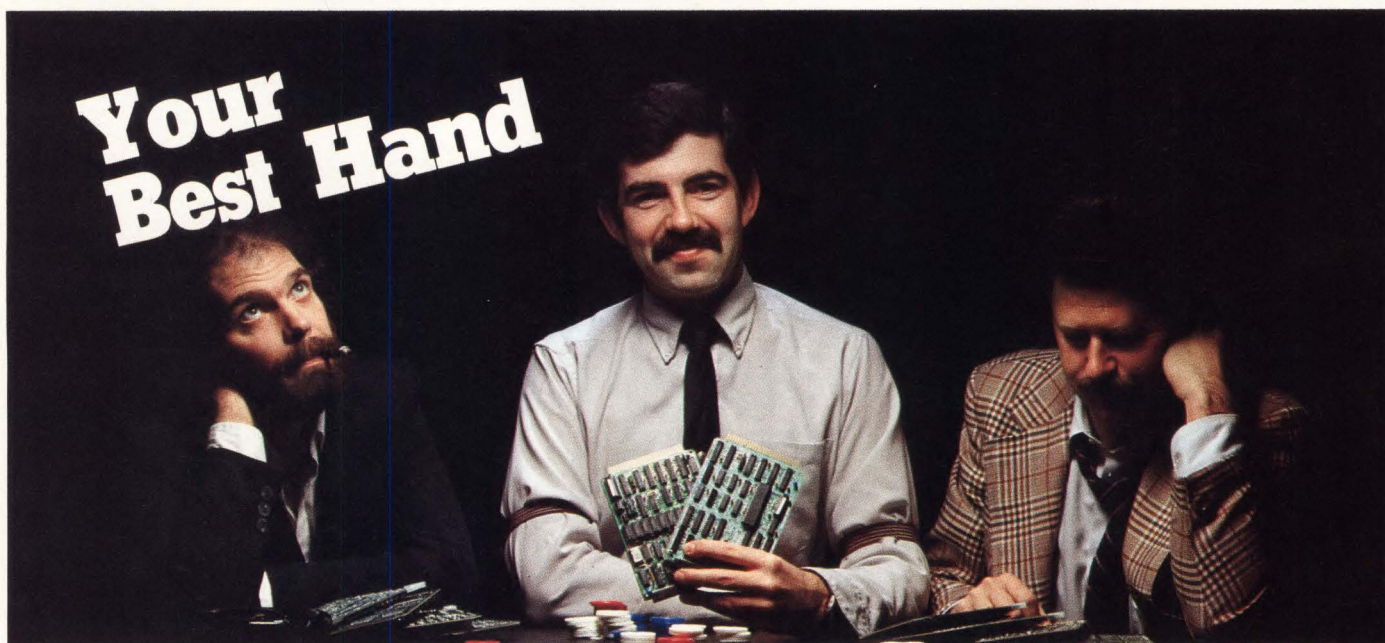
Power Engineering Society Summer Meeting. Los Angeles Hilton, Los Angeles, CA. Contact: Robert L. McMillen, Los Angeles Dept. of Water and Power, 11 N. Hope St., Los Angeles, CA 90051.

July 24-29

Siggraph '83. Detroit, MI. Contact: Siggraph '83 Conference Office, 111 E. Wacker Dr., Chicago, IL 60601. (312)644-6610.

July 27-28

Softfair. Hyatt Regency, Crystal City, Arlington, VA. Contact: IEEE, Harry Hayman (301)589-8142.



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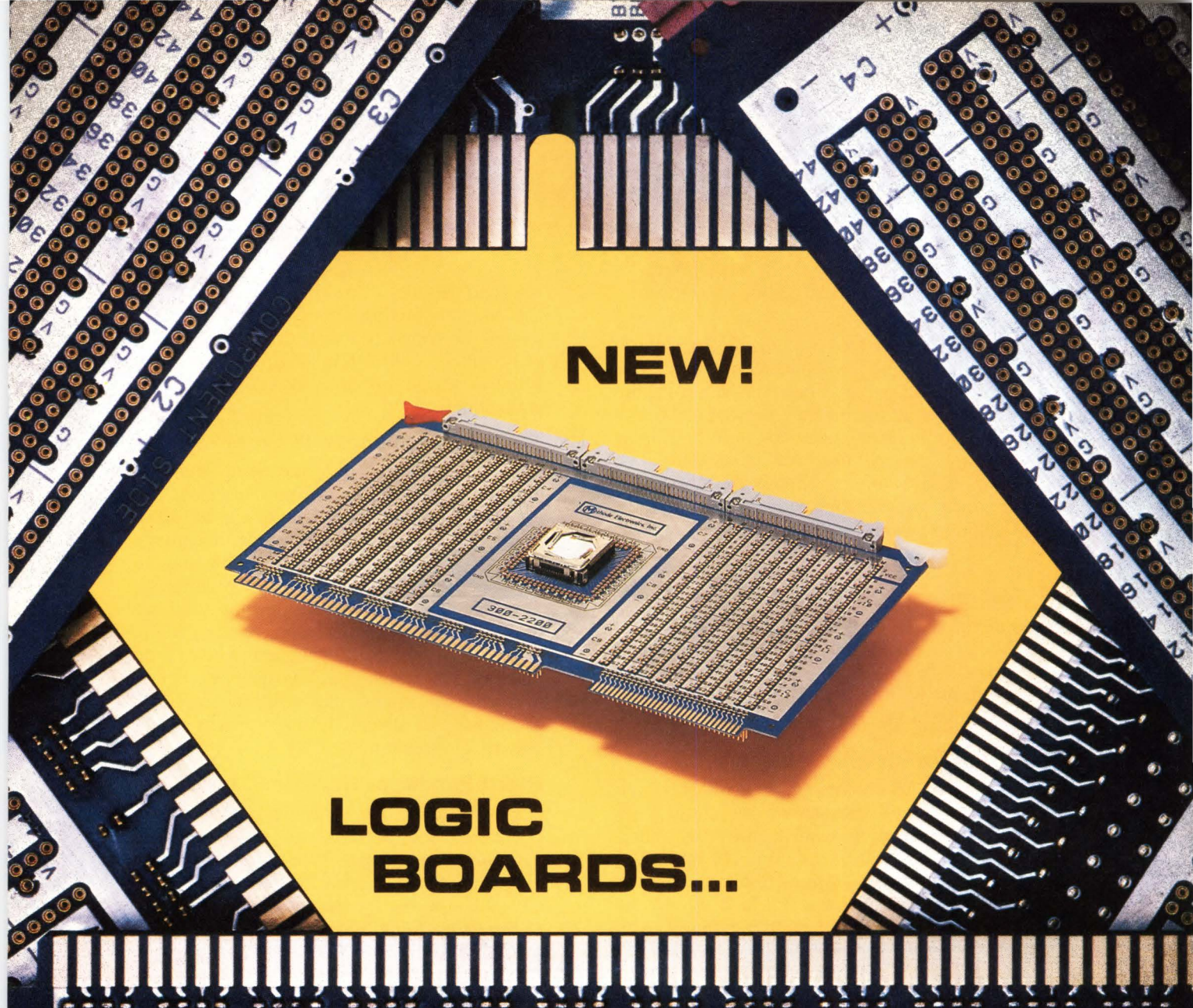
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News Update

Device Driver Development Program

Graphic Software Systems Inc. and Digital Research Inc. have announced that eleven major graphics peripherals manufacturers have agreed to participate in their joint device driver development program. Through the program, announced last month, graphic software and operating system specialists develop device drivers. These device drivers are then offered to customers through the Graphics System Extension (GSX) for the CP/M operating system.

Microcomputer Market

Intelligent Technologies International, Palo Alto, CA will introduce its first products; a series of board-level micro-to-micro and micro-to-mainframe communications packages for the IBM PC, within the next two months.

CTC/Allen-Bradley Agreement

Computer Technology Corp., Milford, OH has announced the signing of a marketing and investment agreement with the Allen-Bradley Co., Milwaukee, WI. The marketing agreement gives Allen-Bradley exclusive marketing rights of the IPS in computer applications. CTC maintains the manufacturing rights and will be the sole supplier of the IPS system components to Allen-Bradley. The investment agreement covers the purchase by Allen-Bradley of a minority equity position.

PolyComputers To Develop Desk-Top

PolyComputers, Inc. has announced that it has received \$800,000 in funding from a Research and Development Limited Partnership to develop a desk-top version of the Poly-Computer which will be capable of processing at a sustained rate of .7 million instructions per second ("MIPS") in concurrent time-sharing, real-time, and multiple batch stream modes, with virtual memory support.

James Tolley, President of PolyComputers, indicated that, "this new development funding will enable us to offer a complete line of multiprocessing virtual memory systems from well under \$20,000 to a 17-CPU, 16 MIPS version at under \$100,000.

Plated Media Joint Venture

Onyx + IMI, Inc has announced the formation of a joint venture between Onyx + IMI,

Inc. and Knudsen Systems, Inc. of Chino, CA to manufacture thin-film plated media for use in Winchester disk drives. The company will be called KSI Disk Products and will also engage in R&D for vertical recording technology.

TI, SEEQ Technology To Cross License

Texas Instruments, Inc., and Seeq Technology, Inc., have announced an agreement for the application of Seeq's nonvolatile E²ROM (electrically erasable, read-only memory) technology to TI's TMS7000 eight-bit, single-chip microcomputer family. Under the terms of the agreement, Seeq will develop versions of the TMS7000 family using Seeq's 2K x 8 five-volt-only E²ROM program memory in place of TI's standard ROM memory. Seeq, in turn, will make the resulting E²ROM TMS7000 and several future versions available to TI beginning in 1984.

Esprit Purchases Hazeltine Line

Esprit Systems, Inc. has announced it has completed the purchase of the Computer Terminal Equipment Product Line from Hazeltine Corp. Esprit Systems is a new company formed by the management group of this product line together with Rosenkranz & Co., a New York City based Investment Banking Firm, and Oxford Partners, a Stamford, Connecticut based Venture Capital Firm specializing in high technology investments.

Magnex Signs Benchmark Contract

Magnex Corp. has signed a "benchmark multi-million dollar contract" to provide its MIS-180 thin-film magnetic disk read-out heads to Storage Technology Corporation (STC). The Magnex MIS-180 heads will be used by STC in its 8380 disk drive subsystem, a data storage system with a capacity of 2.5 Gbytes that is plug-compatible with the IBM 3380 disk drive.

Archive Corp. Signs \$2.5M Contract

Archive Corp. has been awarded a \$2.5M contract to provide streaming cartridge tape drives to Sun Microsystems, Mountain View, CA. Under the terms of the agreement, Sun Microsystems will purchase both Archive's 20 and 45 Mbyte Intelligent Sidewinder and Super Sidewinder.

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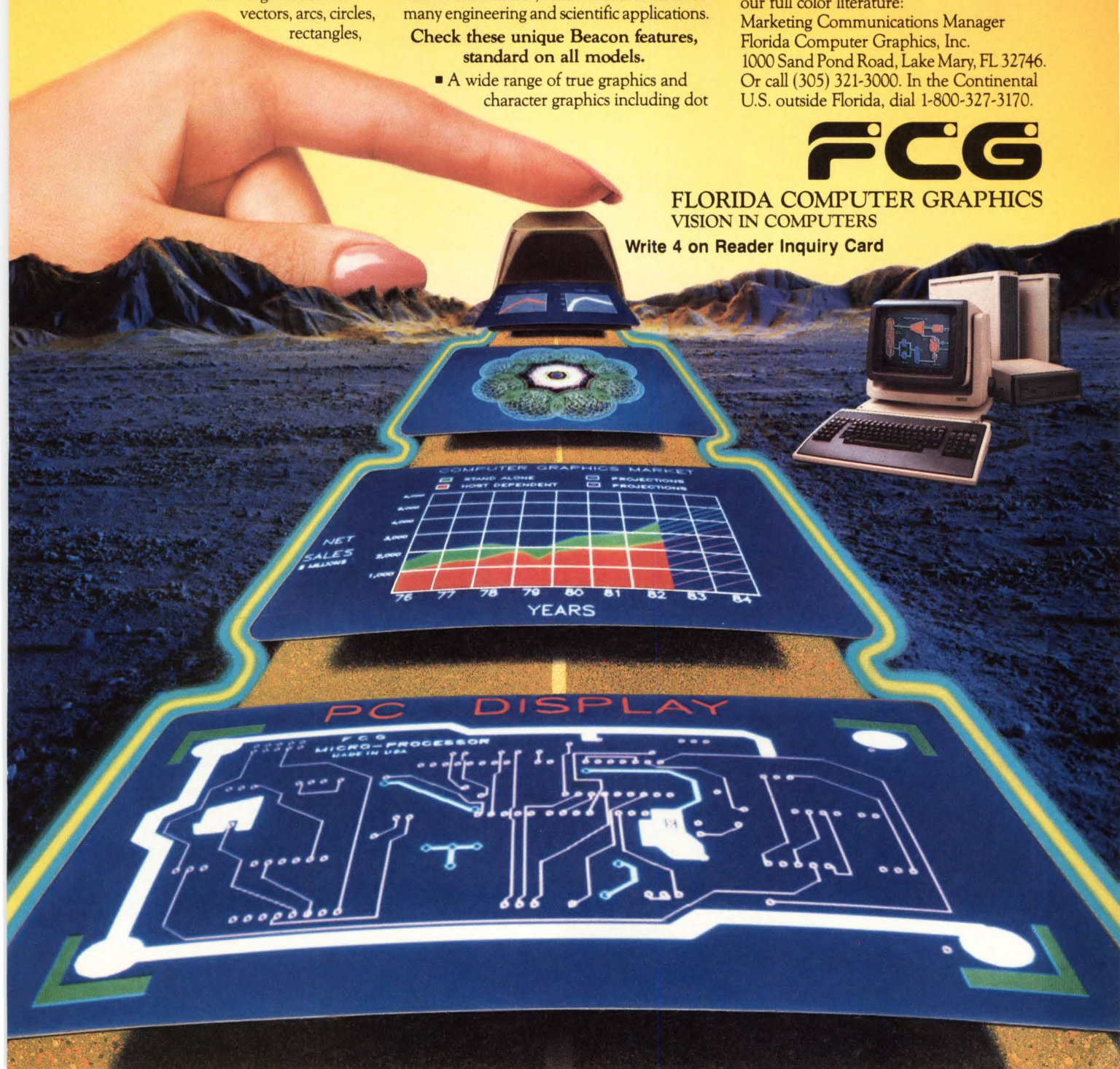
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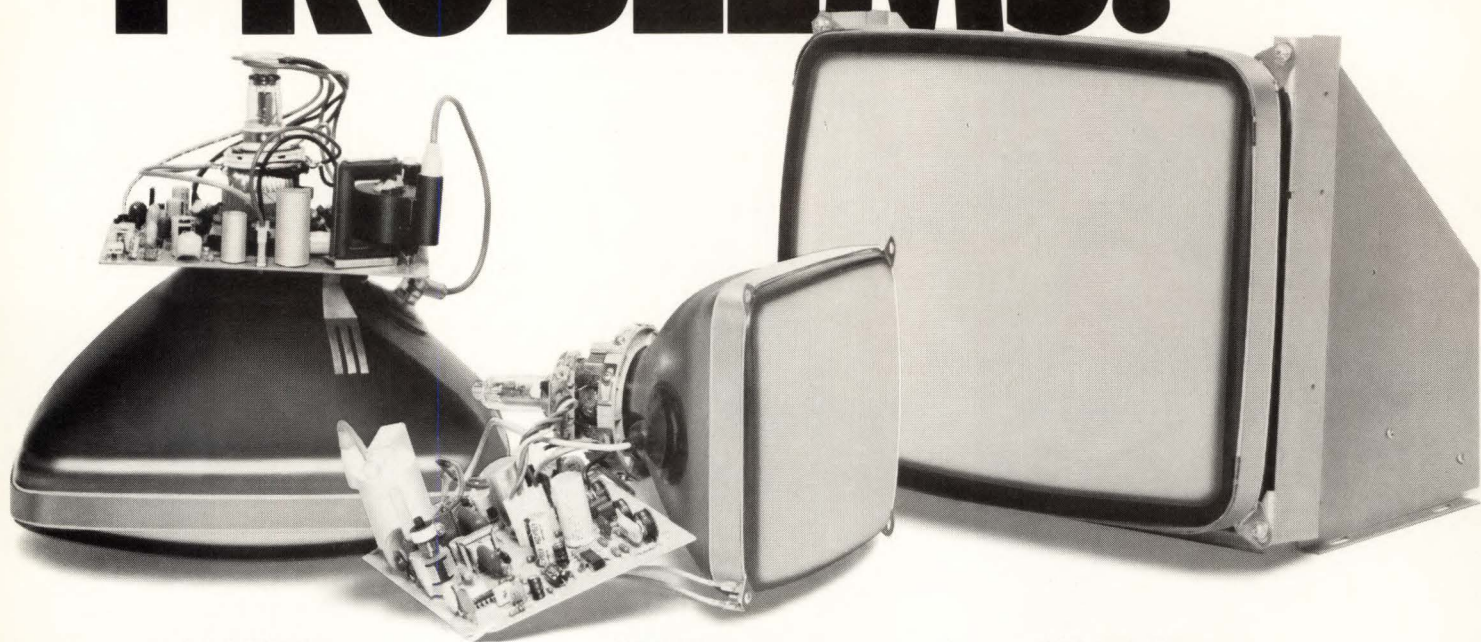
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MiniScribe V

MiniScribe will announce 3 and 4 platter 5¼" Winchester at NCC. Designated MiniScribe V, the hard disk systems are expected to have a maximum capacity of 40 Mbytes with oxide media and 52 Mbytes if plated media is used. The V features an access time of 65 ms, almost double the performance of the MiniScribe IV. OEM pricing is about \$700 or \$200 less than closed loop drives of similar capacities. Production is slated for the 3Q of 1983.

Winchester Disk Controller Board

Adaptec Inc., Milpitas, CA recently announced a new fully SASI/SCSI compatible Winchester disk controller board. The ACB-4000 is priced at \$150 in high volume OEM qty. The ACB-4000 is currently available as a board along with ACS-4000, a licensed chip-set version of the product.

Raster, Auto-trol Sign \$1.5M Deal

Raster Technologies, Inc. signed a 2-year OEM agreement worth approximately \$1.5M to supply Auto-trol Technology with color raster-scan controllers for their CAD workstations. Raster Technologies' Model One controller is capable of 1024 × 1024 resolution with four bit planes of image memory allowing simultaneous display of up to 16 colors.

DEC, Molecular Design Agreement

DEC and Molecular Design Ltd. (MDL) announced a cooperative marketing agreement to promote use of MDL application software packages on DEC's VAX superminicomputer systems. Under the agreement, MDL is adapting its line of chemistry-oriented application software packages to DEC's family of VAX 32-bit superminicomputers.

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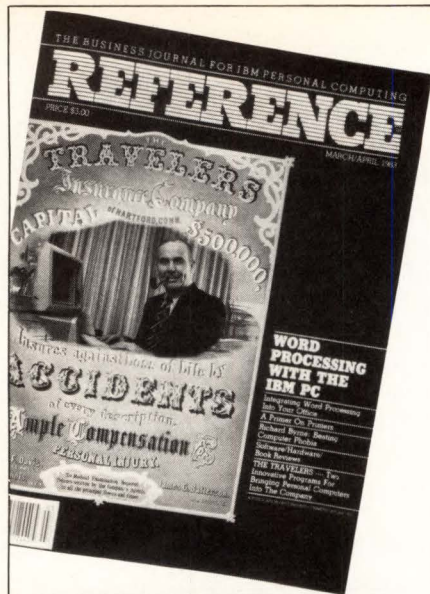
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Technology Trends

3M Preparing For New Media

The 3M company of St. Paul, Minnesota has one of the more optimistic outlooks on the market for magnetic media and storage products. The firm's St. Paul-based research laboratories reportedly have several technologies prepared for use in media products. In the area of micro floppy media, 3M is working on all sizes announced to date: 3.0, 3.25, 3.5 as well as the recent IBM announcement, 4.1. Representatives indicate, however, that they consider the media or sub-

strate their crucial consideration, rather than size. Vertical recording, particulate versus thin film, thin media applications processes, coercive recording processes and stable recording substrates are among the key issues being studied. The company is likely to bring a great deal of hidden strength to the field, being the largest producer of magnetic media in the world, or second after TDK if flexible media only are considered.

—Borrell
 Write 232

IBM Introduces 4" Diskette Drive

IBM recently introduced their new 4" diskette drive at the January 26, 1983 ANSI meeting in San Diego. ANSI is currently considering three proposals: the 3", 3.25" and 3.5" media format. IBM's introduction could produce even longer delays in setting standards should they decide to push for support.

The IBM 0341 diskette drive records on one side of the 4" IBM

DemiDiskette using FM encoding. Capacity is 358 Kbytes unformatted. Other specs include: 46 tracks, 6865 bpi, and 68 tpi. The drive has both read and write capabilities and contains the required power drivers for controlling the drive.

The drive is available now and is priced at \$600 in single quantity and at \$165 each for OEM quantity 10,000.

Write 231

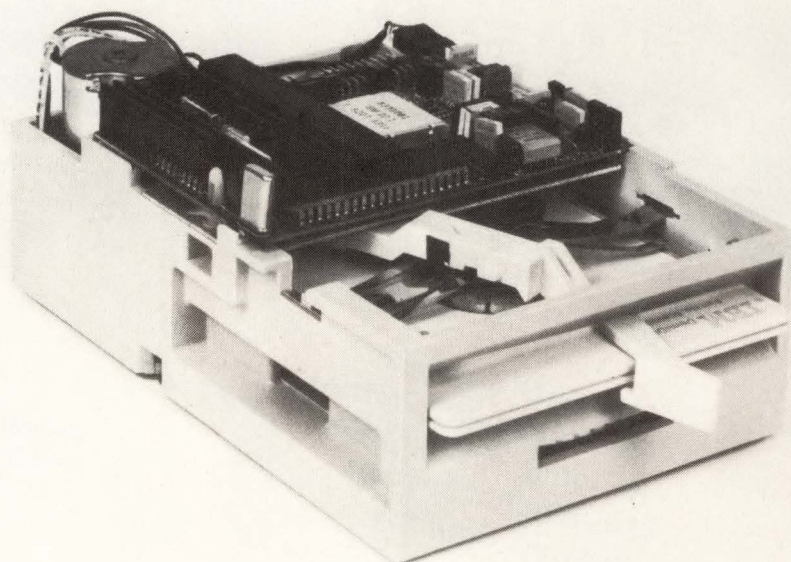
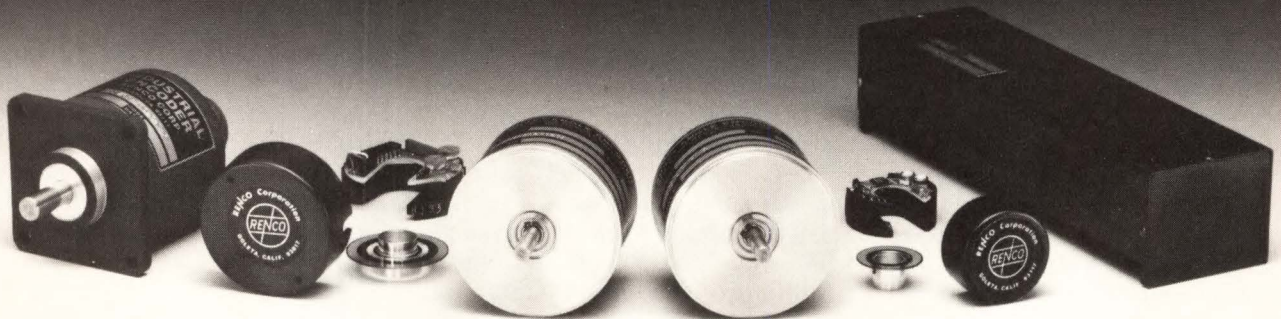


Figure 1: IBM 0341 4" diskette drive.

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Flat Electronic Displays In Computer Products & EDP Applications

The current and anticipated growth in the computer terminal display market is a reflection of the ever expanding market for computers and related equipment.

The traditional CRT display will continue to dominate as the major display technology used in computer terminals, at least through the end of this decade. The CRT's ability to display several thousand characters and its tremendous cost effectiveness (4 to 6 cents/character) are the main reasons for this projected domination. By comparison, the emerging flat, dot matrix display technologies will be limited to smaller numbers of characters, and will be more expensive on a per character basis.

Competing Technologies

During the next seven years, we see a number of competing flat panel display technology types emerging: flat CRTs, LCDs (Liquid Crystal Displays), VFDs (Vacuum Fluorescent Displays), PDPs (Plasma Display Panels), EL (Electroluminescent), GEP (Gas-Electron-Phosphor), and Electrophoretic Information Displays (EPID). At present, LCDs, VFDs, PDPs and EL panels are being used in computer/EDP applications but only on a limited basis.

The projected U.S. and worldwide markets for flat panel displays used in computer applications are shown graphically in **Figure 1**. The U.S. market will grow from \$24 million this year to nearly \$40 million by 1985 and to over \$90 million by 1990. This year's worldwide market will be just over \$65 million. As the economy improves this year and next, the worldwide market for these displays will grow by 30% in 1984. An average annual growth rate of 25-30% is expected between 1985 and 1990; the worldwide market should exceed \$270

million by the end of the decade.

Dedicated CRT

All desk-top and nearly all μ Cs now incorporate dedicated CRT displays, with diagonal screen sizes ranging from 10 to 15 inches. The CRTs used in these systems have a resolution of 300 to 500 lines and can routinely display about 2000 characters. The flat CRTs currently under development by Sony, Philips and others will most likely be introduced on the market for computer application during 1984. Sony has already introduced a hand-held TV using their flat CRT concept while Philips has demonstrated a prototype of their channel electron multiplier faceplate device. The U.S. market for flat CRTs will be about \$0.5 million initially but should grow to over \$10 million by the end of the decade. On a worldwide basis, the flat CRT data display market is expected to reach \$45 million by 1990, 16.6% of the total market (**Figure 2**). Because of the relatively higher cost of the flat device, this represents only about 6% of the projected \$676 million worldwide market for all CRTs (value of

bulb, yoke, and E-gun) used in non-consumer applications.

Currently, the most commonly manufactured VFDs are the blue-green segmented displays for use in digital clocks, radio/TV tuner indicators, stereo equipment, VCRs, vending and gaming machines. The dot matrix type VFDs are designed for use in computer terminals, word processors, and graphical display applications.

All In Japan

There are only three manufacturers of VFDs, all based in Japan and each controlling about one third of the world market. One of the three, ISE Electronics, Ltd., is concentrating its efforts on the development of large area, dot matrix panels for eventual application to PCs and data processing equipment. ISE now offers 45 models of their "ITRON" series VFDs which can display from a minimum of 8 characters (14 segment arrays) to as many as 480 characters. They also offer continuous dot matrix arrays in various sizes and in 1982 announced the development of a 256 $\times$ 256 element VFD matrix display.

The other VFD manufacturers

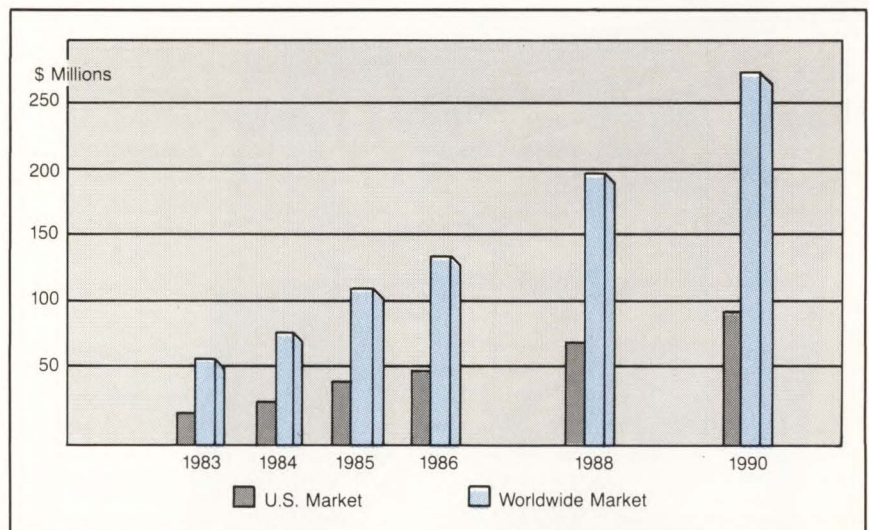
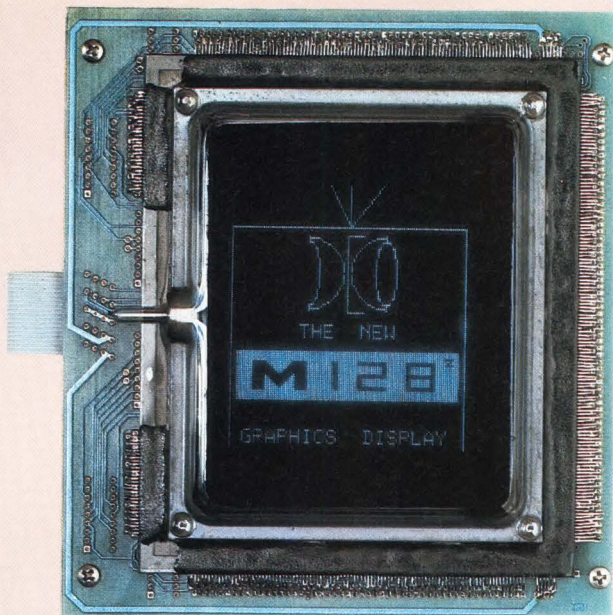


Figure 1: Projected U.S. and worldwide markets for flat panel displays used in computer related equipment.



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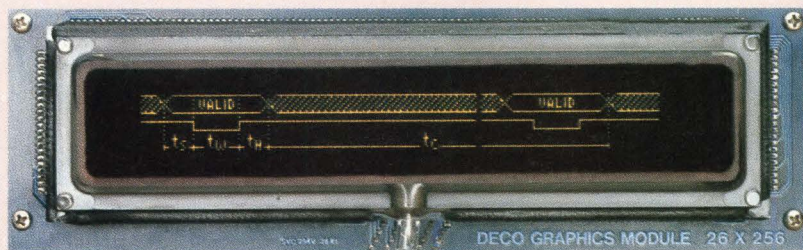
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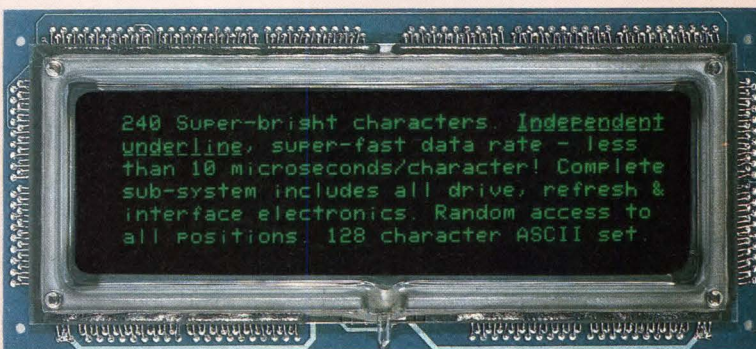
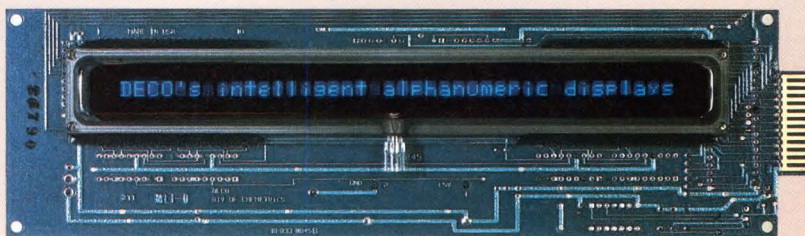
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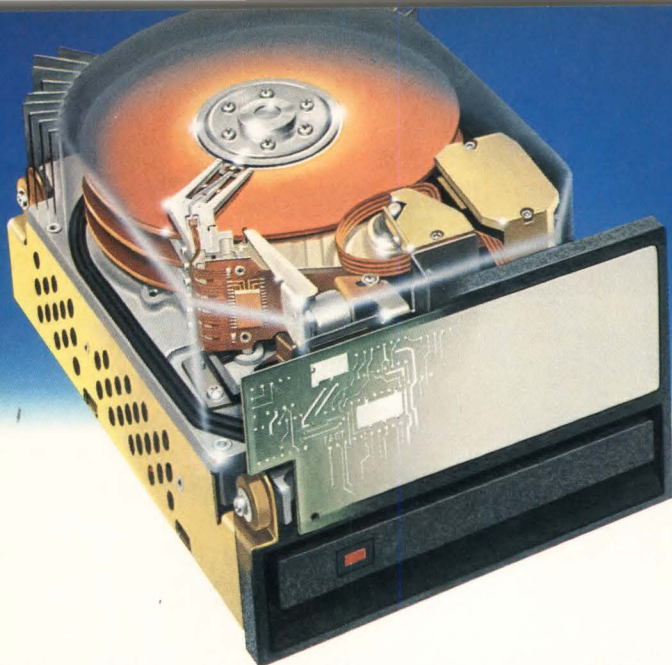
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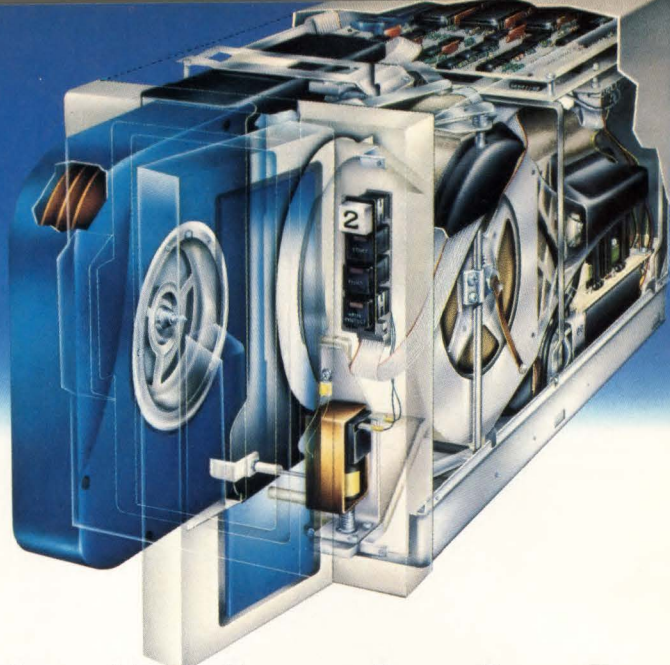
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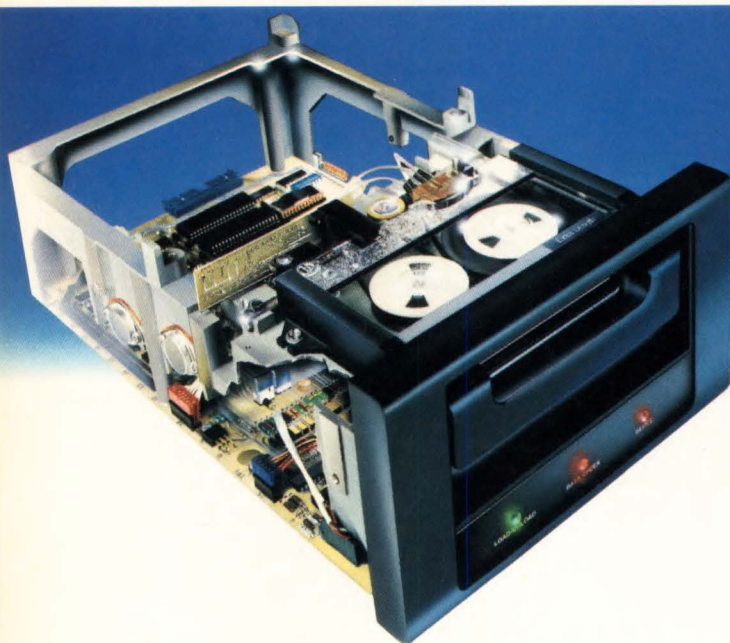
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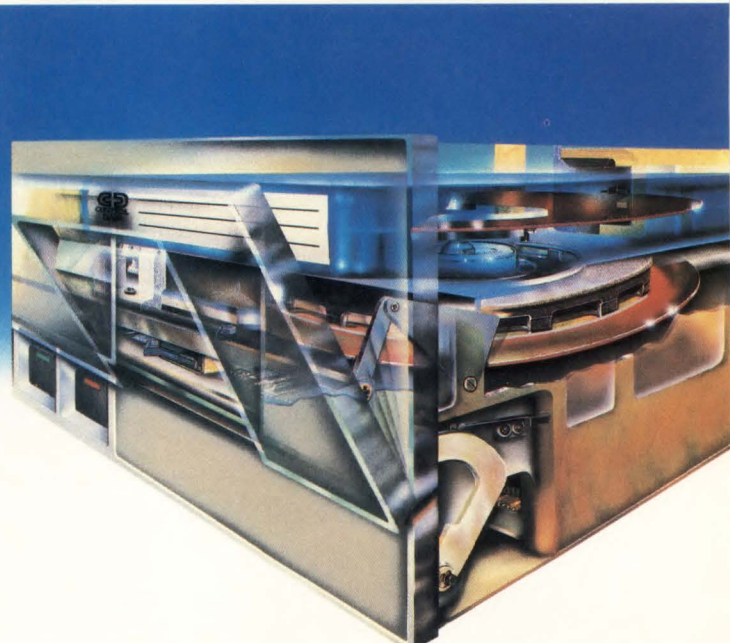
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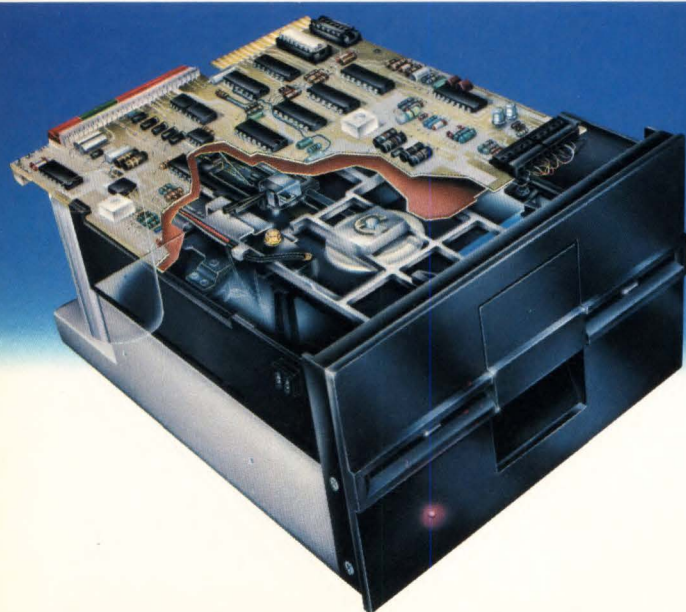
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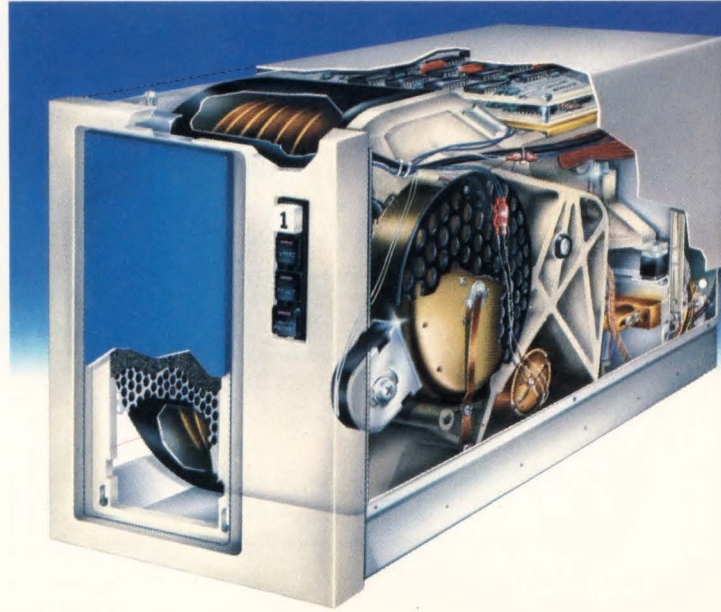
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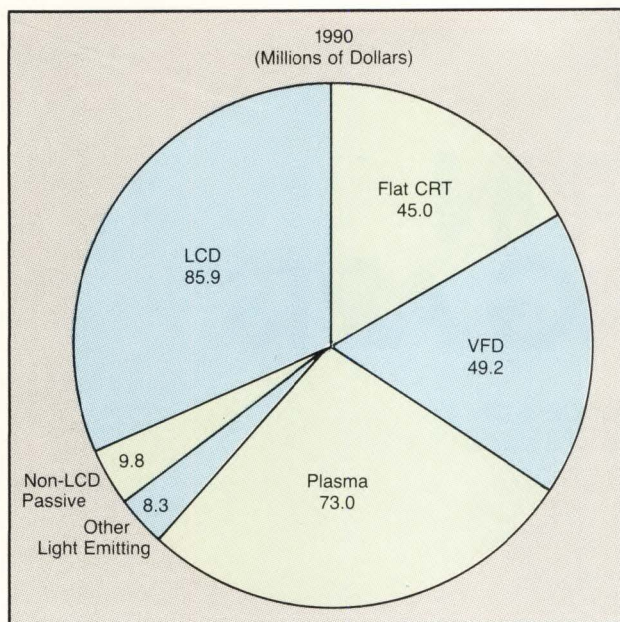


Figure 2: Projected worldwide market shares by technology type.

are Nippon Electric Company (NEC) of Tokyo and Futaba Corp., based in Akihabara, Japan. Most of both companies' products are sold to consumer electronic manufacturers but they are also concentrating their efforts on the emerging office equipment and automotive markets. Futaba now offers a variety of dot matrix VFDs with up to 15 lines of 80 characters per line for use in electronic memory typewriters and computer terminals.

The U.S. market for dot matrix VFDs for computer related equipment is expected to grow from less than \$4 million this year to about \$12 million by 1990. The worldwide market should exceed \$49 million or 18% of the flat display market by the end of the decade (Figure 2).

play market by the end of the decade (Figure 2).

Of all the flat panel display technologies used in computer related products, PDPs have thus far captured the largest market share. Burroughs is conceded to be the world's largest producer of all types of PDPs. Industrial Electronic Engineers (IEE) is believed to be second only to Burroughs in U.S. sales, although the company buys all of its PDP units from Oki and Okaya of Japan. Cherry Electrical, Beckman, NEC and Fujitsu are also major suppliers. Burroughs is now building a 25 line $\times$ 80 character PDP for use in computer systems. The company expects to build at least 2000 units in 1983. Although initially it will

be offered at a higher price, company spokesmen believe that the product's price will be reduced to \$500 or less within the next several years as volume increases.

Companies such as Electro-Plasma, Interstate, Photonics and Science Applications, Inc. (SAI) produce displays for military applications under government contract; the PDPs are usually part of some larger system which includes peripheral components and software. Electro-Plasma has recently introduced a PDP for computer terminal application with up to 51 lines of 80 characters per line for the commercial market.

The worldwide PDP market will grow from \$30 million in 1983 to \$73 million by 1990, making it second only to LCDs in market share (Figure 2). The potential cost effectiveness of PDPs on a per character basis for a large number of characters, will create markets for PDPs in graphics terminals, other EDP applications and perhaps even the "portable" or "transportable" personal computer market.

The only other light emitting technology which will show a significant increase in market share during the next few years is the dot matrix Electroluminescent (EL) panel. Sharp Corporation is presently the only manufacturer of these devices, which emit yellow-orange light. Most of the units sold in 1982 were consumed by Grid Systems and several other μ C makers for evaluation purposes. If Sharp solves the techni-

PROJECTED U.S. MARKET FOR FLAT DOT MATRIX DISPLAYS FOR COMPUTERS/EDP APPLICATIONS

(Millions of Constant 1982 Dollars)

Display Technology Type	1983	1984	1985	1986	1987	1988	1989	1990
CRT (Flat)	--	0.50	1.00	2.00	3.00	4.50	6.75	10.13
LCD	2.70	4.05	5.67	7.65	9.95	12.44	15.55	18.66
VFD	3.80	4.56	5.47	6.57	7.88	9.30	10.79	12.40
Plasma (Gas-Discharge)	17.00	20.40	23.66	26.50	29.15	31.49	34.01	36.05
Other Light Emitting	0.80	1.60	2.56	3.84	5.38	6.45	7.42	8.16
Other Flat Passive	--	0.00	0.50	1.00	2.00	3.00	4.20	5.46
Total	24.30	31.11	38.87	47.56	57.36	67.17	78.71	90.85

Table 1: Projected U.S. market for Flat Dot Matrix Displays for computers/EDP applications.

**PROJECTED WORLDWIDE MARKET FOR FLAT DOT MATRIX DISPLAYS FOR
COMPUTERS/EDP APPLICATIONS**

(Millions of Constant 1982 Dollars)

Display Technology Type	1983	1984	1985	1986	1987	1988	1989	1990
CRT (Flat)	--	1.00	2.00	4.00	10.00	20.00	30.00	45.00
LCD	24.10	30.13	37.66	47.07	56.48	64.96	74.70	85.91
VFD	10.00	14.00	18.90	24.57	30.71	36.86	42.75	49.16
Plasma (Gas-Discharge)	30.00	37.50	45.00	51.75	57.96	63.76	68.86	72.99
Other Light Emitting	1.50	2.40	3.36	4.37	5.46	6.55	7.53	8.29
Other Flat Passive	--	0.00	0.90	1.80	3.60	5.40	7.56	9.83
Total	65.60	85.03	107.82	133.56	164.22	197.52	231.40	271.17

Table 2: Projected worldwide market for Flat Dot Matrix Displays for computers/EDP applications.

cal (reliability) problems associated with the manufacture of these devices, the price of the thin-film EL could become competitive with those of the other flat panel technologies. However, lack of a second source and the uncertainty regarding reliability makes it unlikely that EL will make as great an impact on the market as the other discussed here. Gas-electron-phosphor (GEP) displays, which are presently under development by Siemens, will not make an impact on the market until late in the decade. If Siemens is successful with its development of a cost-effective, full-color, computer

terminal display, this GEP technology could begin to displace some of the CRTs pre-eminent position in color graphics terminals. For these reasons, the worldwide market for other light emitting displays is only projected to be \$8.3 million by 1990 (**Figure 2**).

Non-LCD Market

The markets for non-LCD passive displays are essentially the same ones that are now served by LCDs. Unfortunately, many of the technologies are under development and it would appear that products using these technologies

will not appear on the market until 1985 or later. The worldwide market for these displays is projected to approach \$10 million by 1990. The leading candidate for application to computer products is the electrophoretic (EPID) display using the control electrode concept. The EPID display has received the most attention in recent years and companies such as Exxon Information Systems, North American Philips, Tektronix and Xerox have active development programs.

*Joseph A. Castellano, Ph.D.,
Stanford Resources, Inc., San
Jose, CA*

Sleeping Giant To Enter CAD/CAM 32 Bit Market

Gerber Systems Technology, subsidiary of Gerber Scientific Inc. (\$115 million sales in 1983), is quietly gearing up for major announcements in CAD workstation systems for the summer conference season. The company's main strength lies in CAD for mechanical products, but its electrical/electronic products are growing rapidly. Gerber Systems has had a

great deal of success over the past year with its 16 bit Autograph product line, particularly in Southern California where it claims to be displacing Computer vision in small installations. The Autograph is a monochrome, standalone workstation with a price range of \$80k to over \$100k. Success for the product is due to the fact that at \$100k the cost of a

system makes it roughly equivalent to a commodity, that is approximately equal to the cost of capital equipment for the engineer in a design lab. Over 50 of the systems have been sold at an average cost of \$110k.

Based upon this success for standalone products, GST is planning to enter the market with an even more powerful, but less costly, system over the course of the summer. Early indications are that the company will take a twofold approach in evaluating or producing such systems: one to be based upon the newly released Hewlett-Packard 9000 Desktop Main-

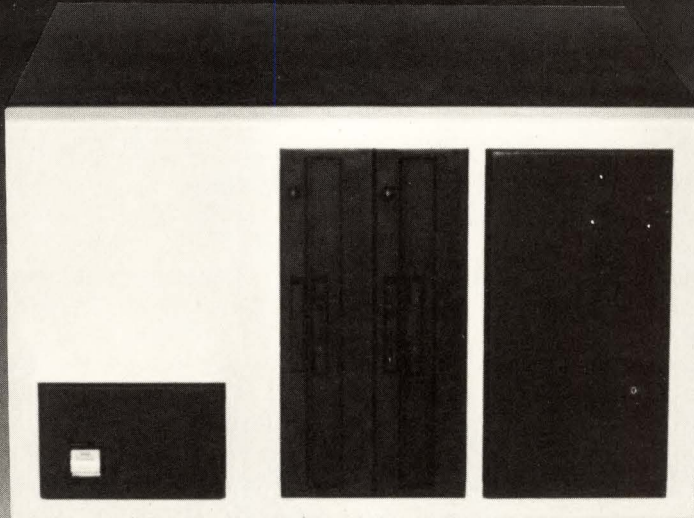
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Market Trends

frame, and another around a National Semiconductor 32 bit μ P. The company feels that 32 bit systems are the key because they will allow engineers to perform analysis rather than merely draft. The primary market for such systems is felt to be in companies with annual revenues under \$100k annually.

Under the HP 9000 based approach, the system would be approximately \$80k to \$90k, but would have 80% again the capability of its existing IDS system. Such a system would also be designed with the implementation of solids modelling software in mind. The Romulus Software now provided by Evans and Sutherland is already under consideration for such an application.

With a Motorola chip, a lower cost but also color system could be configured in the price range of \$40 to \$60k; such a system might have a 50 Mbyte Winchester tape backup. While both hardware approaches are spoken of, a single set of Unix, Fortran and Pascal/C programs would be developed for both. However, while the Motorola based system would be oriented for the lower cost single workstation approach, the HP model would form part of a networking system, based around HP's Ungermann/Bass networking or around some type of Ethernet controller. The former approach would be provided with additional market appeal through the strength of HP's international marketing capabilities.

The real importance of these scenarios, however, is found in the other operating subsidiaries of Gerber Scientific—in its Scientific Instruments and Garment Technology Groups where CAM applications provide a hidden base of technology available to no other major CAD vendor. These are the company's original areas of expertise, and if coupled with 32 bit CAD capabilities, the firm will have a chance to become significantly larger in the entire field of process technology.

Write 233
—Borrell

Fujitsu's MBM27C64 — A Step Ahead

Introduction

The Fujitsu MBM27C64 is a high speed 64K UV Eraseable Programmable Read Only Memory (EPROM), organized into a μ P compatible 8K words by 8 bits.

The MBM27C64 is available in speeds of 300, 250 and 200 ns. Operating with a single 5V ($\pm 10\%$) supply (for read operation) it features fully static switching circuitry to eliminate the need for external clock circuitry. All devices are available in the commercial temperature range of 0 to 70°C. Selected devices are available in extended (-40° to $+85^\circ\text{C}$) and high reliability (-55° to $+125^\circ\text{C}$) temperature ranges. All devices are available with the MIL-STD-883B test flow processing.

Two Dimensional Output Buffer Control

The G control input and the P/G control input provide the user with a two dimensional high-speed output-enable accessing feature with accessing times of less than 150 ns. Each output-enable input allows the user to OR-TIE the respective outputs without invoking bus contention. This feature also simplifies future system memory expansion.

Single Input Power Down Control

The MBM27C64 will enter one of two standby modes dependent on the level of the E input. Applying a TTL compatible input will invoke a power down operation, yielding a current consumption equal to 1 mA (ISB1). Applying a CMOS compatible input (from $V_{CC} - 0.3\text{V}$ to $V_{CC} + 0.3\text{V}$) to this E input yields a typical device current consumption of 1 μA (ISB2) compared to ISB1 for the TTL input. An internal pull-up resistor to V_{CC} on the E pin eliminates the need for an external pull-up. The three control signals E, G and P (P/G) provide the

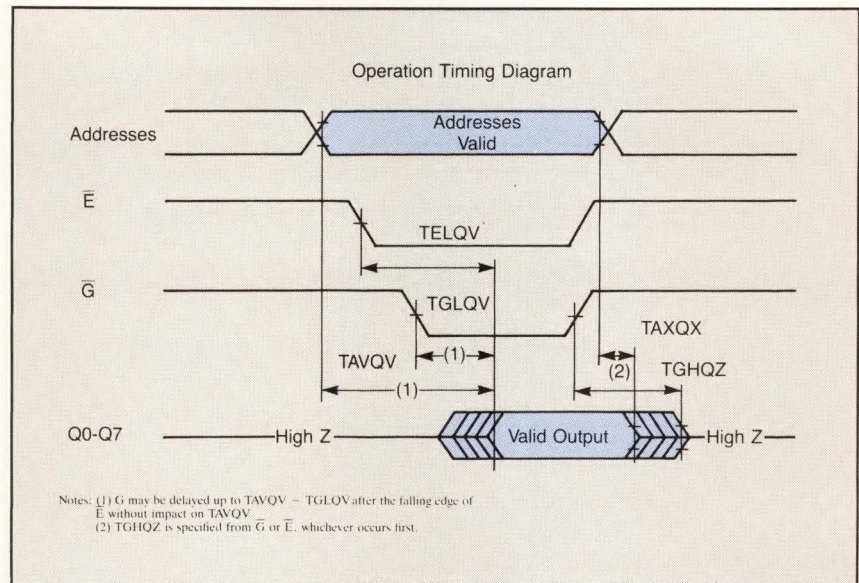


Figure 1: Read operation timing diagram.

user with an easy read operation timing sequence (**Figure 1**).

Power Consumption Savings

As is the case in all CMOS devices, the power consumption of the MBM27C64 depends on the frequency in which the device is operating. Operating at 5 MHz, the MBM27C64 draws a maximum of 100 mW over the entire temperature range, approximately $\frac{1}{5}$ that of industry available 64K NMOS EPROMs. Typically ($T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$), this device draws approximately 33 mW for 4 MHz operation.

The standby current (ISB1 and ISB2) consumption of the MBM27C64 is 3 or 4 orders of magnitude less than its NMOS counterpart. Typically, the MBM27C64 draws 5.5 μW for a CMOS ($V_{CC} + 0.3\text{V}$ to $V_{CC} - 0.3\text{V}$) input level on the E input. Expressed as a power-per-bit ratio, the MBM27C64 consumes approximately 0.27% (8.0nW to 2900 mW) that of its NMOS competition.

Programming

The standard 50 ms programming pulse width can be utilized with

the MBM27C64. This algorithm is available on many commercially available PROM Programmers. However, the device will achieve extremely high data retention characteristics even when pulse width is reduced to 25 ms.

In addition to the standard 25–50 ms pulse width programming procedure, the MBM27C64 can be programmed with a fast programming algorithm designed by Fujitsu called QuickPro. The algorithm (**Figure 2**) uses a sequence of 1 ms pulses to program each location and will typically yield a savings of 86% in programming time per device. In custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the V_{CC} pin followed by applying +21V to the V_{PP} pin. A TTL low input must be applied to the E input, and a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 ms pulses must be applied to the P pin for programming. After each pulse, a counter must be stepped and the location

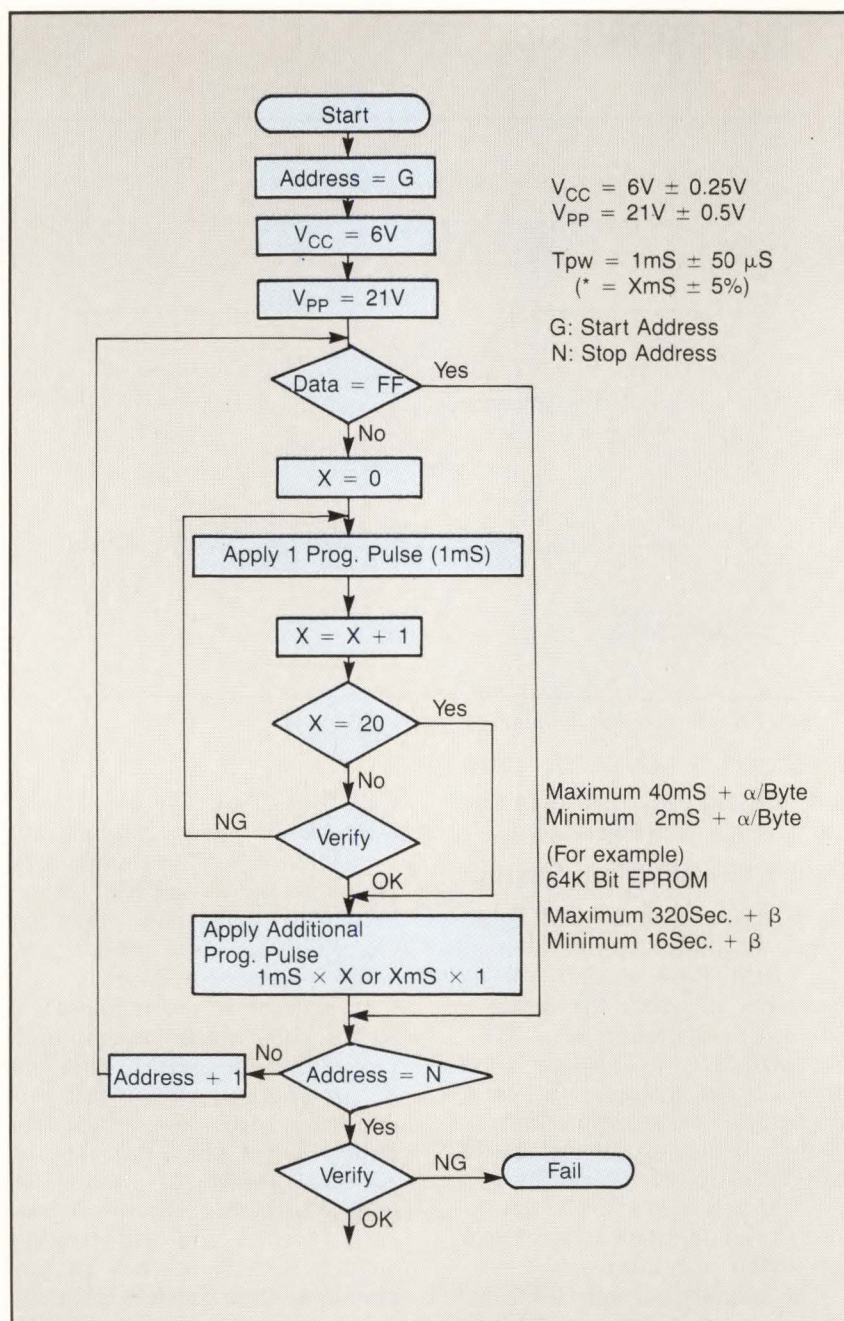


Figure 2: Quick programming flow chart for MBM27C64 EPROM.

should be checked for accuracy. Upon verification, an additional sequence of 1 ms pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge.

An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 ms. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu MBM27C64 devices will typically require only two 1 ms pulses (one initial and one additional) to reach proper stored charge levels.

Typical Applications

Due to the non-volatile characteristics of EPROMs, the majority of applications for EPROMs are in a μP -based system's development cycles. Since micro-code frequently involves many iterations before the released revision of the code is produced, non-volatile, quickly and easily alterable devices are necessary. The popular μP s of today can be seen in **Table 1** with their corresponding access time requirements. As can be seen by the table, the speed versions of the MBM27C64 accommodate many μP systems.

Packaging

The MBM27C64 is available in a Jedec Standard 28 pin dual-in-line

PROCESSOR	MBL8086			Z8000		68000	8085A		6809			Z80		NSC800	
DEVICE/MHz	5	8	10	4	5	8	3	5	1	1.5	2	2.5	4	2.5	5
MBM27C64-30	X			M			X		X	X		X		X	
MBM27C64-25	X			X	X		X	X	X	X	X	X		X	
MBM27C64-20	X	M		X	X	M	X	X	X	X	X	X	X	X	M

Note: M = Marginal compatibility

Table 1: The MBM27C64 series devices are compatible with many popular μP s, limited by the required access time of each μP .

package (DIP). The package is manufactured in ceramic with a transparent crystal window for ultra violet memory array erasing. This device is also available in a 32 pin leadless chip carrier. With dimensions of $450 \times 550 \text{ mm}^2$ (typical), this LCC is also manufactured in ceramic with a transparent crystal window and a metal seal. Additional hybrid packaging techniques are also available upon request.

Conclusion

The CMOS 64K MBM27C64 EPROM provides a high density, low power consumptive and easily alterable EPROM primarily for use in μP based systems. The 5.5 μW typical standby current drain and 150ns typical access times combine to offer the designer a program storage device with no "trade-offs." The NMOS MBM2764 is also available in similar speeds and packaging options for users who don't require the advantages that the CMOS device offers. *Rob Stransky, Applications Engineer, Fujitsu Microelectronics Inc., 2985 Kifer Rd., Santa Clara, CA. 95051. (408) 727-1700. Write 234*

Attention 8K $\times$ 8 EPROM Users! Free Samples. . .

If you are interested in obtaining samples of the Fujitsu CMOS MBM27C64 or its NMOS counterpart the MBM2764, please write on company letterhead to Bob Sykes, Product Marketing Engineer, Byte-Wide Memories, Fujitsu Microelectronics, Inc., 2985 Kifer Rd., Santa Clara, CA 95051. To receive the free part you must include description of your 8K $\times$ 8 EPROM application, including total memory size, speed and power consumption requirements, and packaging needs. One free MBM27C64 or one free MBM2764 will be delivered to the first 500 qualified inquiries.

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Industry Spotlight: Trends in the Robotics Industry

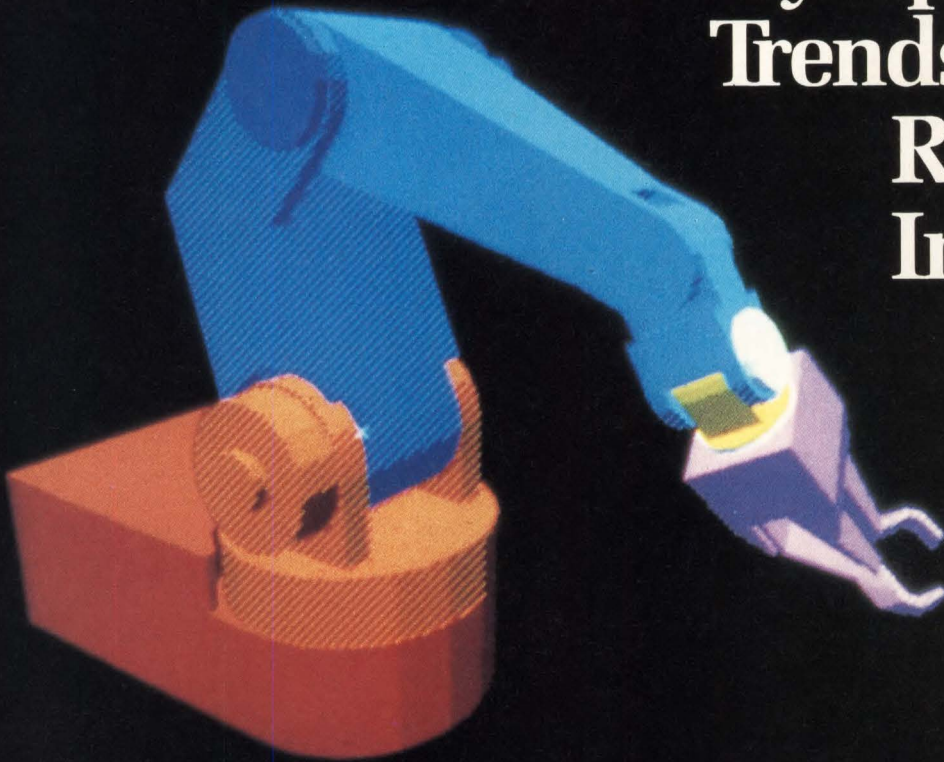


Photo courtesy General Electric CAE International Inc.

Robots are performing as contributing assets, not as inevitable costs.

Laura Conigliaro is Vice President in the Research Department at Prudential-Bache Securities Inc. As an analyst, she covers the field of factory automation, including robotics, computer-based vision systems, advanced technology machine tools, and CAD/CAM, both from an industry and company perspective. Ms. Conigliaro's previous employment includes several years spent as an intelligence analyst at the National Security Agency. She was contributing author to a book on investment and, more recently, has contributed numerous articles to various publications and studies done about robotics, including her own "Robotics Newsletter."

by Laura Conigliaro

When did the robot industry begin? Clearly, the use of the first industrial robot commercially, in 1961, occurred many years before the more recent frenetic focus on the industry. But robotics was not even an industry during the 1960s. It was an occasional order, sometimes a multiple order and, in terms of dollar value, it was primarily whatever business Unimation and Versatran, and later Prab, managed to get.

Historic though they may be, I believe it is important to view these so-called "phases" in order to put what is now occurring in

perspective (**Figure 1**). Not until the mid- to late-1970s did robotics actually become the beginnings of an industry. Between 1975 and 1977, it is estimated that unit sales for Unimation—the company that virtually *was* the entire robotics industry in terms of dollar volume—jumped by over 2.5 times. Prab had its first \$1M year by calendar 1977. Cincinnati Milacron had decided to become a serious participant in robotics. Copperweld Robotics (then Autoplace), DeVilbiss and Asea pretty much rounded out the industry and added a few million dollars more to dollar volume. And the auto industry, having "discovered" robots years earlier and used them on a modest scale, began a major retooling program in which robots figured prominently.

As a result of all these events, robot sales jumped from about \$15M in 1976 to about \$45M in 1979, and the rest of the country slowly began to discover robots.

Robotics during Phase I was a

series of uses, a few users and a few vendors, but not really an industry. During Phase II, the few more companies selling robots experienced rapid growth; the few users wanted more as they began to learn what the early robots could do. By the third phase, robotics had evolved from a novelty to an industry, with far more companies in it and far more users aware of it.

A year ago, a euphoric atmosphere pervaded the robotics industry. The thoughts were that this would be an ever onwards-and-upwards industry and that fast growth was virtually inevitable. But thanks to the recession, what *was* inevitable was that this industry—still so tied to the automotive industry and very much dependent on capital spending—would slow.

Over the past year, corporate balance sheets got worse and worse: Braniff, Penn Square Bank of Oklahoma, Wickes Cos., and others filed under the Bankruptcy Act; huge operating losses were recorded by hosts of companies; Caterpillar, Deere, GM, Ford and multitudes of others were forced to slash capital spending budgets. I, for one, cut my own forecasts for estimated sales in 1982 by US-based robot vendors from \$250M to \$190M. For 1983, forecasts shrank from \$300M to about \$225M, with even these numbers predicated only on the assumption that an economic recovery will have slowly begun building some strength by mid-1983.

Does this mean that robotics will go back to being more a fad than a strongly growing industry? Does it lessen the importance of robotics? Not at all—it means quite the opposite. Companies have, in fact, cut back their capital spending plans and have also cut back on certain product lines or pared away certain assets. They have also recognized that in a slower growing environment there must be a far sharper focus on the process of manufacturing in order to get as much profit out of what little growth there is.

Concurrently, we have been bombarded with publicity about Japan. It may not all be accurate, but the challenge is there nonetheless. The robotics industry may have slowed in its growth temporarily but it is inevitable that companies will upgrade their manufacturing technology. Since robots are an important part of this scheme, the industry is just marking time.

Japan's Impact

Whenever the issue of Japanese manufacturing prowess arises in a conversation with well-informed American manufacturers, someone will always note that the Japanese are not really ahead of us technologically, but that it is merely a *perception*.

ed that, if taken apart part-by-part, some of their newest models would compare quite favorably with Japanese models? And yet imports have commanded a rising share of automotive consumption. Apparently, perception is often more important than reality.

In terms of the manufacturing process, many Japanese companies have implemented available technologies in efficient and useful ways. Are they ahead technologically in this area? Probably not—but it probably does not matter much. They have emphasized the factory floor, cut costs by doing so, improved quality and automated facilities where possible. In short, they have turned manufacturing into an asset.

Most Japanese companies,



Cincinnati Milicron's electric-driven T³-726 Robot performs a plasma arc cutting operation on a steel pipe.

This may be true, but the quick dismissal of that point as merely "perceived" (and presumably, then, not real) is to overlook the importance of perception. How many consumer products are bought on the basis of the *perceived* value of one versus another? How many times have US automotive manufacturers assert-

however, haven't yet done this. In fact, Japan's manufacturing process spans a broader spectrum than our own. There are companies even in Japan that will argue forcefully that automated facilities built, for example, by Fanuc and Yamazaki are merely showplaces that are not cost effective. The truth of this is hard to determine,

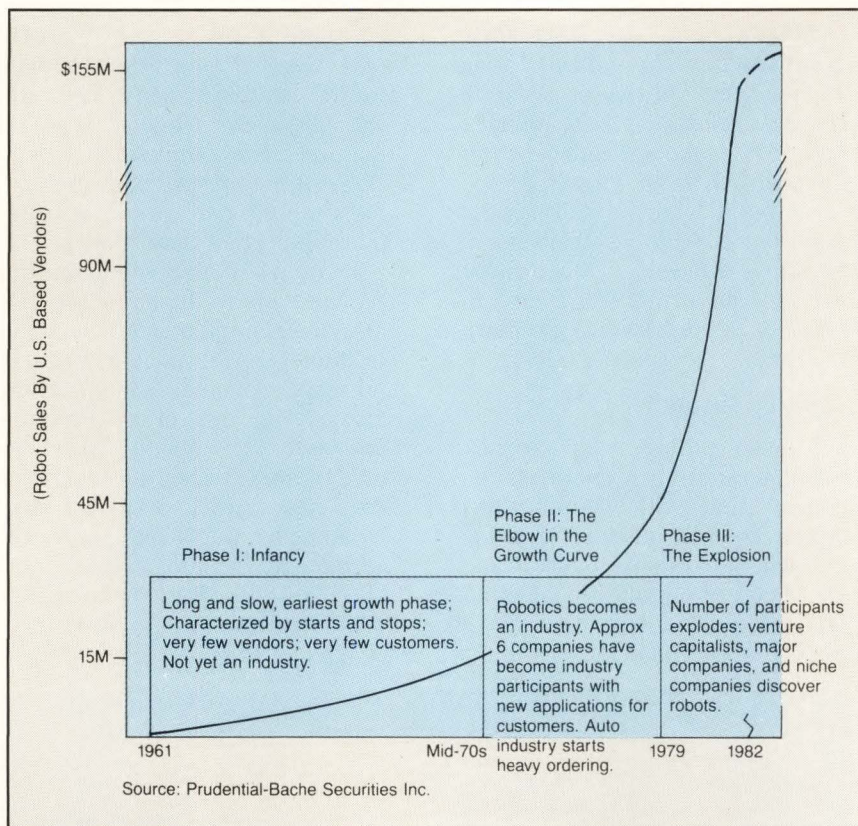


Figure 1: The three phases of the Robot Industry.

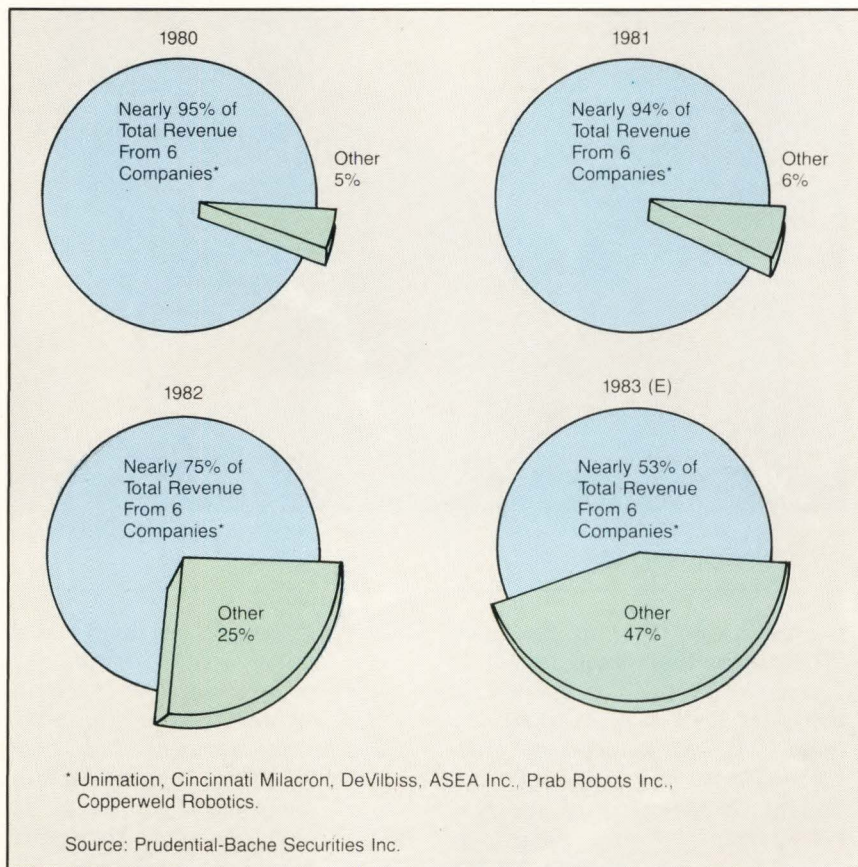


Figure 2: Changes in market share composition 1980-1983.

although it is important to bear in mind that Japan has a lower cost of capital than the US; that labor often works only one shift there; and that Japan is really a production-oriented and not a market-oriented society. In short, what may be cost effective in Japan may not be so in the US.

Nevertheless, it is difficult to believe that, over time, the automation seen at the best of these companies will not be more cost effective than conventional manufacturing seen at many other companies. Manufacturing is probably not an area where one company will "leapfrog" over another. Solutions will more likely come about through slow and steady incremental types of improvements. This means that companies cannot continue to wait indefinitely before improving their manufacturing.

US companies know that competition is now just as likely to come from anywhere in the world as it is from their own country. As a result, even in a period of slower growth and more modest capital spending over the next several years, priorities will change from adding more production capacity and product lines to modernizing and improving current manufacturing facilities. This should favor robots and related technologies.

Who Will Be Successful?

The fact that there are so many robot companies—nearly 100 in the US, over 250 in Japan and several dozen in Europe—and yet still so small an industry, clearly presents an imbalance. Also, several of the newest members of the robotics community are so large that they could absorb the entire 1981 US robot industry with negligible effect on their corporate sales (**Table 1**). And yet all of the companies, as well as the new start-ups, the medium-sized companies that have newly-formed robot divisions, and the original six or so companies are having important effects on the industry (**Figure 2**).

What is it that will make one company stand out against another? For one thing, just as companies recognize their competitors' weaknesses and use these for their own benefit, they must also recognize and use their competitors' strengths. Some of the licensing agreements US companies have signed with Japanese vendors are prime evidence of such recognition. Why duplicate what already exists if you can use it to your own advantage? Japanese companies are offering low-priced, high-quality manipulators. Some smart US vendors will take these manipulators, add value to them in the form of better computer controls, software, pre- and post-installation support and other ancillary equipment, and create a value-added premium-priced robot system.

Some companies have adopted the philosophy of recognizing competitors' overwhelming

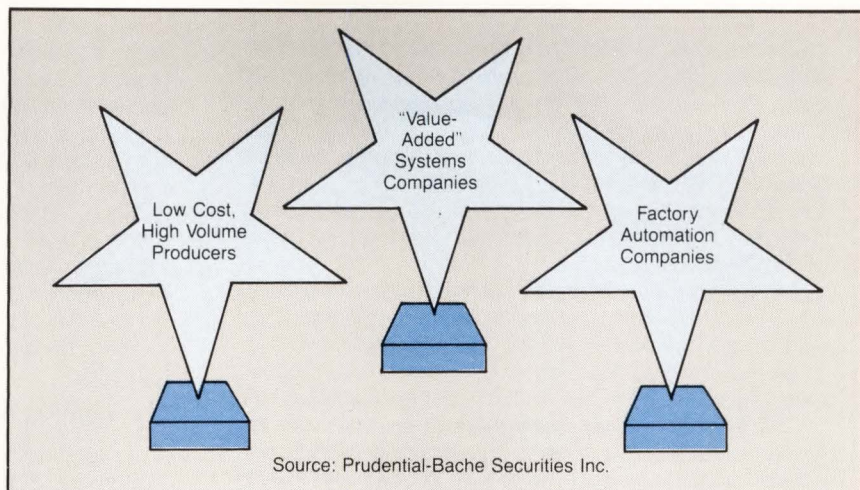


Figure 3: The core of the robot industry is divisible into three groups.

strengths and not even attempting to go head-to-head against them. For example, Control Automation, a venture-financed start-up, is emphasizing its universal communications capability—thereby admitting that the probability of

its imposing its own networking standards on the entire robot industry is slim to none.

Furthermore, it seems likely that companies that attempt to compete with Japanese robot vendors on a product-to-product

Robotics And Vision

A robot is basically a controlled arm ceaselessly moving from one position to another. The movement might be complex, as in programmed arc welding of a triple-dimensioned joint, but the cycle is invariant unless some sensor is involved to feedback new information or orders.

The robot arm is extremely well articulated, using up to eight axial movements in a given motion (torso, shoulder rotate, shoulder bend, elbow bend, elbow rotate, wrist bend & rotate, hand closure). However, in order to function, the workpiece and the components used must be oriented and positioned correctly. There are a host of tasks that such a non-sensory robot can do well. These include: spot welding, cast forging, spray painting, palletizing and depalletizing, machining, assembly, and arc welding.

The market volumes for the various types of robots is essentially in the order listed above. In most cases, one really can't call pick and place automatons "robots." More sophisticated quasi-prehensile robot arms, without sensory feedback, must not get out of sequence, lest they produce remarkably reproducible junk. More intelligent robot generations require sensory feedback to monitor progress.

There are two main types of sensors: tactile and vision. *Tactile sensors* respond to the degree of fit, to the correct location of a part or to its orientation by a sense of touch. Discounting the single point sensors on the effectors or graspers themselves, there are no real multi-

point tactile sensors. Many methods have been proposed and one of them may be useful. But it has been demonstrated time and again that to move an idea into production takes some fifteen years. Quite aptly, this was the case for electronic vision (CCD, CID, and Photodiode arrays).

Vision Sensors, developed in 1970, were the first real imagers (although at the time they were promoted as anything but imagers). These were the Charge Coupled Devices (CCDs). By 1980, imagers were commercially available at near reasonable cost (reasonable, that is, for R&D experiments). At that point, thanks to American innovation, they were more than adequate for any robotic application. At this point, thanks to Japanese pricing strategy, they have become practical, cost-effective tools.

Electronic Vision

Excluding Vidicons, which present some problems for accurate positional location due to eddy currents, etc., most electronic cameras employ silicon to sense the light reflected from a target. The silicon chip provides an electronic image capable of being analyzed by other electronics. Resolution is achieved by arraying large numbers of light sensitive capacitors or diodes on the chip. Each element records a small section of the target and stores its intensity level as a proportionate number of electrons.

The arrays come in endless formats from 32×32

(1024) to 1000×1000 (10^6) (the latter is not commercially available). They also come in three varieties: Self Scan Photodiodes (SSPD), whose photoelements are photodiodes; Charge Coupled Devices (CCD), whose photoelements are capacitors; and Charge Injection Devices (CID), whose photoelements are also capacitors. In the first case, the charge has to be read out serially and in the last it can be read out randomly, when so desired.

All three are equally useful, although there are trade-offs in size, blooming control, speed and specmanship. The long term winner will be the one that lowers its price the most quickly. For robotic vision, an array significantly larger than 256×256 is especially desirable.

Once the target has been imaged on the array (by using some suitable lensing system and often using special illumination such as lasers, strobes and sheets of light), the next step is to read it out and to adapt its format so that it can be seen on a monitor (for setup) and processed by the follow-on image processor (called the Vision Module).

Read out is accomplished by other integrated circuits on the imager chip itself. Formatting is performed by printed circuit boards (following NTSC or CCIR standards) that are placed within the camera housing itself. The final step is to feed this formatted signal into the Vision Module so that it can be identified, recognized, inspected, located, gauged or counted.

Just a few years ago, robotic vision was the slowest module in the robot package. The target was to get vision to perform its analysis in two seconds to keep up with the robot. At that time image analysis took 2 minutes; in 1980 this was reduced to 20 sec. It is now $\frac{1}{30}$ sec, which equates to 1,000,000 parts/shift.

Vision Modules

A robot needs only one type of information to perform its task. It needs to know where a part is; it asks simply for location and nothing else. It is true that robots can be used for other tasks besides grabbing and sticking, but if they are not primarily being employed to move to some point, then their size and cost shall be neither space nor cost effective. Once a robot locates a part and grasps it, then it can be effectively used for other add-on tasks such as inspection, identification or gauging before it moves the component to its secondary location.

A robot has one of two other recognizable application traits. It either works in an environment hostile or hum-

drum to humans or it is employed in an effort to increase productivity. To a lesser extent, it does enhance quality or, at least, it ensures that any defect in workmanship is uniformly present. In all cases, the added vision system is constrained to the robot's work ethic and environment.

Since location is quintessential, most robot vision modules have location software or location hardware. The most general need is to locate the center of something; often it is a hole into which a pin or a rivet has to be inserted. To accomplish this, only the centroid (first moment divided by area) has to be calculated. This is given by:

$$\bar{X} = (1/A) \sum X_i, \bar{Y} = (1/A) \sum Y_i$$

This algorithm is relatively straightforward and simple to implement. Since the round hole has pure 2D symmetry and a square peg is seldom to be inserted, centroid data alone suffices to service this application class.

If there are various hole sizes on the target, then the correct one has to be recognized first. This is done by measuring either the diameters (maximum widths) or areas; again, straightforward problems. If the hole or other features to be located is of lesser symmetry (ovals, squares) and/or other is randomly oriented, then the image needs to be electronically derotated until it is aligned with robot coordinates. With this angular knowledge and prior knowledge as to how the pin or rivet sits in the robot's grasp, the hand can be rotated until the pin lies precisely over the hole.

Robotics is the simplest field for Vision Modules to service. But it is not an easy field for vision to penetrate. Over the past few years, robot companies have been application-driven—and there are many applications. In addition, they try to discourage their customers from purchasing the top of the line robot to try out, lest it sit unused on the production floor. Even though robot manufacturers believe much of their future growth will come from vision and that half of the robots will be sighted, there is a definite reluctance to either retrofit on-line robots with vision or to add it to new generations.

Robotic vision itself might become application-driven and have to be proven out on an individual basis. As a result, sighted robots sit at the edge of a long lead time to acceptance.

—Lawrence A. Murray, Vuebotics Corp. 6068 Corte Del Cedro, Carlsbad, CA 92008. **Write 350**

price-to-price basis are going to have difficulty succeeding. Japanese robots, many of which are of acceptably high quality (many of which are, in fact, being used by US robot vendors through licensing agreements) are almost invariably going to command a lower price. Their per unit production costs are lower. Were end-users simply interested in purchasing a

robot at the lowest possible price and willing to do their own engineering, applications software, support and hardware and software integration, most US robot companies would be unable to compete. However, a majority of US end-users will want more than simply a robot and directly related equipment. They will be far more demanding and, given the

number of vendors presently in the industry, they can afford to be just that.

Successful companies in the US will have to be strong in the areas of management, research and development, marketing and sales, support and field service. Robot vendors which may have previously been able to get away with simply taking orders will have to

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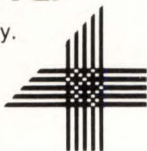
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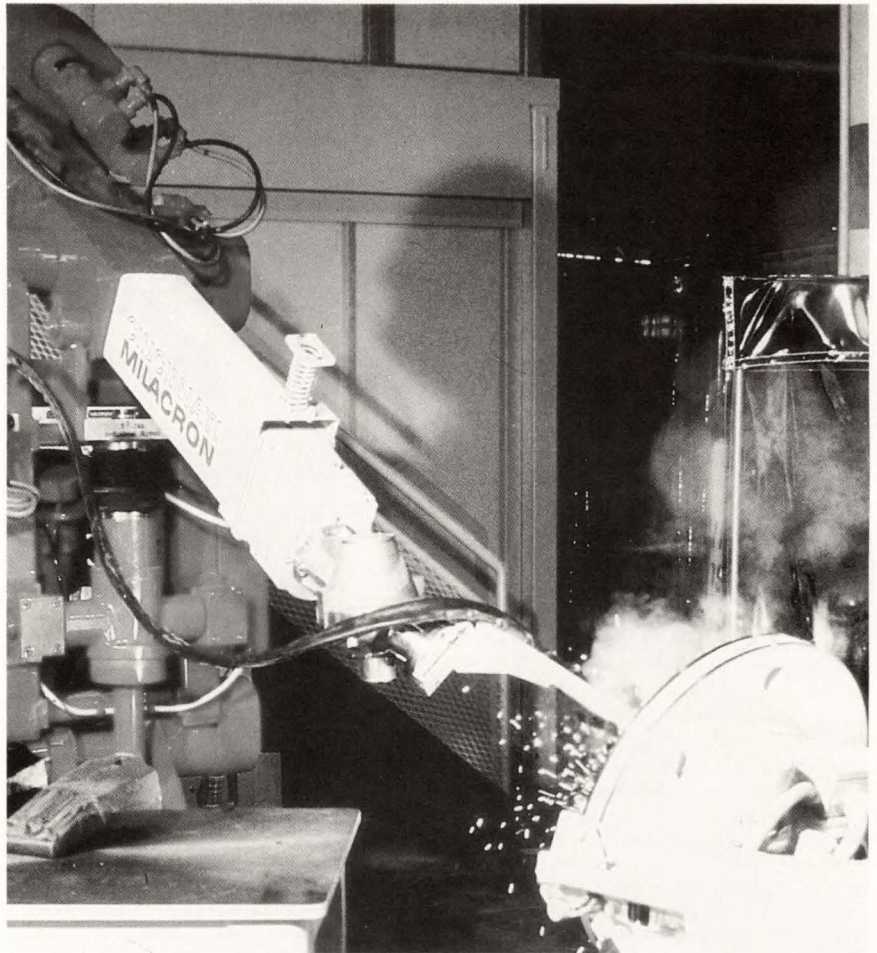
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Robotics



Cincinnati Milicron offers its computer-controlled T³ Robots as the basic tools in turnkey welding packages.

Company	1981 Corporate Sales	Entire 1981 Robot Industry as a Percentage of Company Sales
General Motors	\$62.7B	0.2%
IBM	\$29.1B	0.5%
General Electric	\$27.2B	0.6%
United Technologies	\$13.7B	1.1%
Westinghouse	\$ 9.4B	1.7%
Bendix	\$ 4.4B	3.5%
Textron	\$ 3.3B	4.7%
Allegheny International	\$ 1.9B	8.1%

Source: Prudential-Bache Securities, Inc.

Table 1: 1981 Robot Industry as a percentage of some of its participants' sales.

learn to sell. Although this may sound fairly basic, it represents a fundamental change in business strategy.

The core of the robot industry—the most successful companies, discounting those companies that will be marginal but will survive anyway—will fall into three

groups (**Figure 3**).

Low cost, high volume producers. This group will primarily consist of about a dozen large Japanese robot vendors selling basically commodity robots for various applications.

Value-added, systems oriented companies. This group will in-

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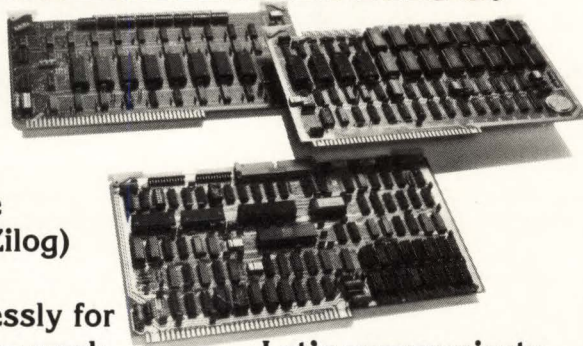
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Robotics

clude many of the successful US robotics companies. Value added can come in the form of turnkey systems, computer controls, or service, but whatever form it takes, it will have to be measurably beneficial to the customer who will therefore be willing to pay a higher price for it. Ironically, nearly all US robot vendors I queried responded that they were value added companies, offering systems, superior software, etc. In the end, customers will tend to cluster around those few where the added value is more real than ephemeral and has the greatest depth. Although it is still far too early to be certain of the names, I believe it possible that some of the most distinguished value added will emanate from smaller companies germinating on the sidelines—companies that have been formed with this in mind.

Factory automation companies. This will consist mainly of the largest corporations in the industry. These companies may not make a great deal of money from robots, their margins may not be nearly as attractive as those of the first two groups, but they will sell robots as parts of a far broader line of single-source systems for automating portions of the factory floor.

Robotics Realism

During the euphoria of a year ago, hardly a week went by that did not see a significant article on robots in a major newspaper or journal. The robot industry may not have been new, but its break into stardom was.

The atmosphere this year is quite different, grounded in cold and hard realism. Robots are not a panacea nor is their installation entirely a painless effort. But they are part of the solution to bringing the manufacturing process out of the dark ages, and to making it perform as a contributing asset and not merely an inevitable cost of doing business. □

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Industry Firsts at ISSCC

by Dave Wilson, Sr. Technical Editor

This year's prestigious International Solid State Circuits Conference featured a number of notable industry firsts.

The phrase "industry first" continues to remain very close to the heart of Seeq Technology's President, Gordon Campbell. His company, innovators of the first 5V only EEROM and the Ethernet controller, has introduced the "industry's first" five volt only EEROM 8-bit microcomputer. Based on TI's 7000 family, the new chip (the Seeq 72720) is self-programmable and uses a 2K × 8 EEROM in place of TI's traditional ROM. (Figure 1).

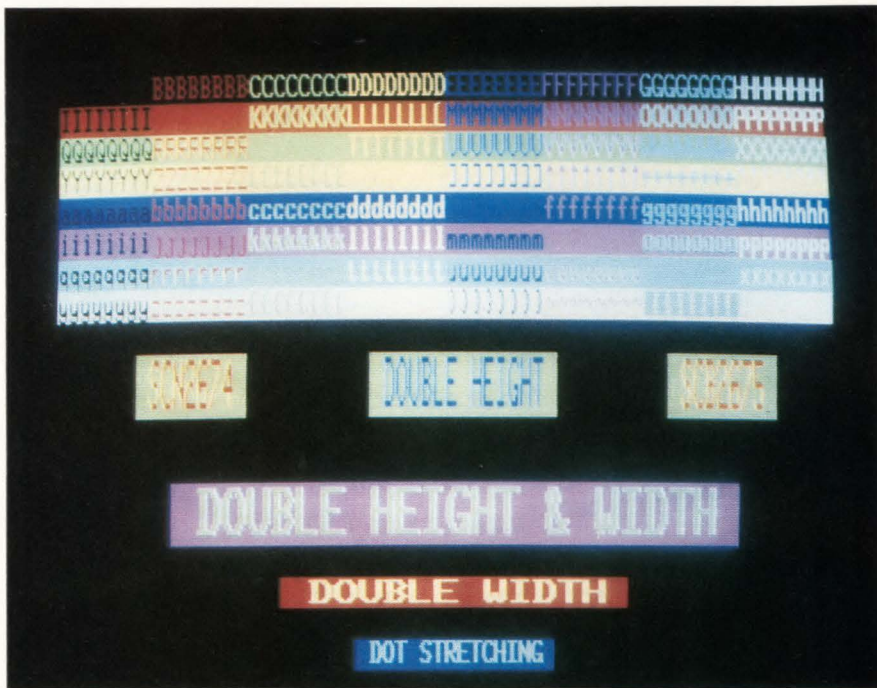
ISSCC highlights included recent developments in memory, μ Cs and graphics.

Seeq has also announced that it has come to a technology exchange agreement with Texas Instruments. TI will supply Seeq with TMS7000 information in exchange for future production rights to Seeq's 72720 and future TMS7000 products employing non-volatile technology.

At present, TI's 7000 series has not gained a wide market acceptance; Campbell feels his EEROM part will have a volatile effect upon that fact.

And although the part is an "industry first", other companies including Intel and Motorola with expertise in EEROM and a widely installed base of 8-bit μ Cs are certain to introduce parts later that will offer strong competition to Seeq.

As the role of 8-bit μ Cs has moved towards the use of CMOS,



Typical output on screen using Signetics Devices.

it is inevitable that a Seeq/TI part using this technology is on the designers table. It has been reported that the marriage of an EEROM with CMOS is at present a headache but "not an insolvable one" according to Campbell.

EEROM memory runs about 2 or 3 times the cost of UV EPROM today, a fact which may also influence the buying decisions of 8-bit μ C users.

One Motorola spokesman felt that the aspect ratio of the Seeq chip would lead to poor production yields, packaging difficulties and high cost. "It looks more like a memory" he said. Campbell seemed unconcerned, but did comment that the next μ C from Seeq Technology would have different dimensions.

As Figure 1 illustrates, the next primary targets for EEPROM may well be the RAM and the micro-code control store, offering a truly versatile μ C product into the marketplace.

John Heightly, President of In-

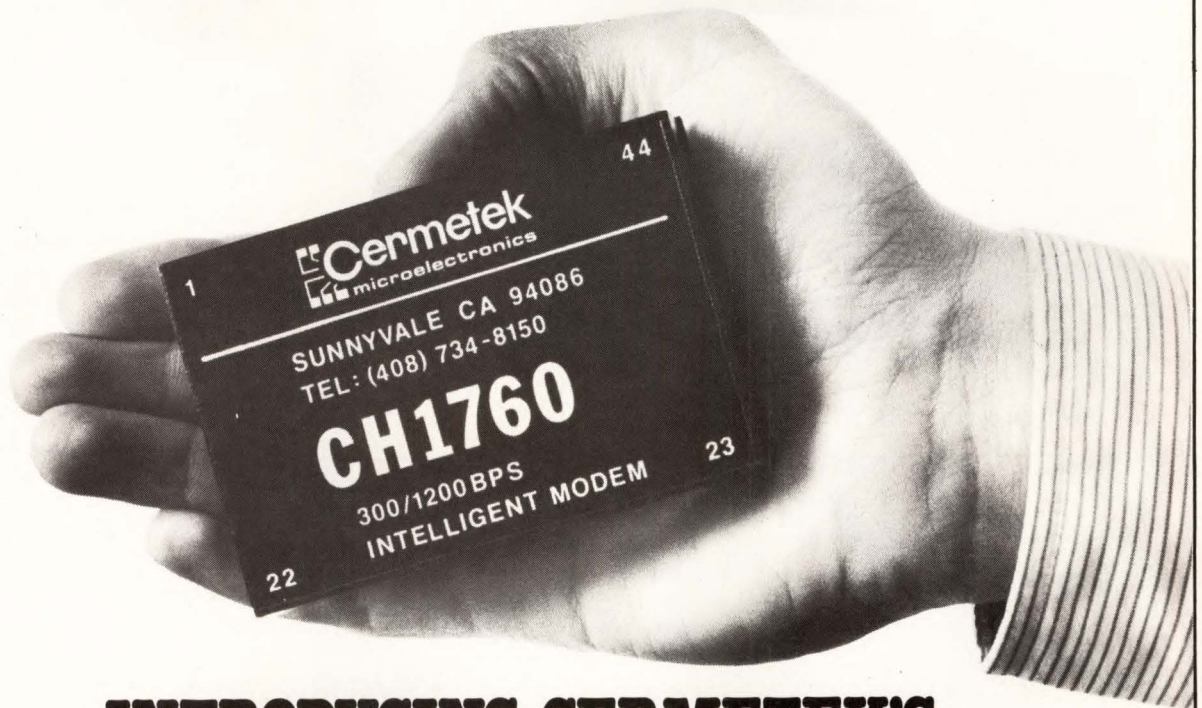
mos, discussed his company's solution to electrically-erasable memory. 5V operation for all modes is a must these days, and the Inmos IMS3630 8K × 8 bit part is no exception (Figure 2). The part uses Inmos' own NITROX process, differing from the Seeq/Intel floating gate approach. At present both technologies only offer 10⁴ cycle endurance, an indication of how many times the part may be read to. In the race to boost this figure past 10⁶ cycles, it will be interesting to observe which technology wins the day.

Graphic Displays

On February 22, Signetics introduced two new ICs to extend the range of its CRT controller family. A demonstration model of a typical system threw up some impressive graphic displays.

In a typical display terminal using the Signetics SCN2670, SCN2671, SCN2674 and SCB2675 CRT terminal devices, the CPU examines inputs from the data com-

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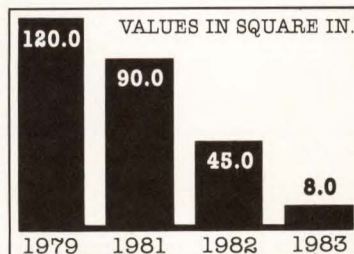
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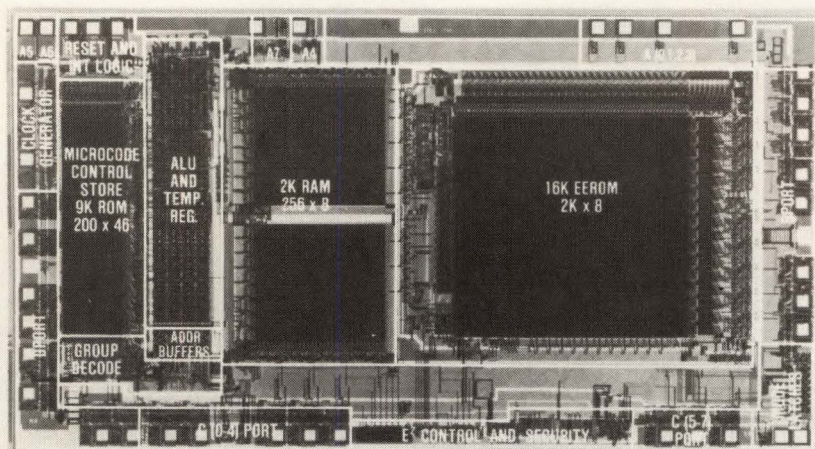


Figure 1: Seeq's single chip EEROM microcomputer.

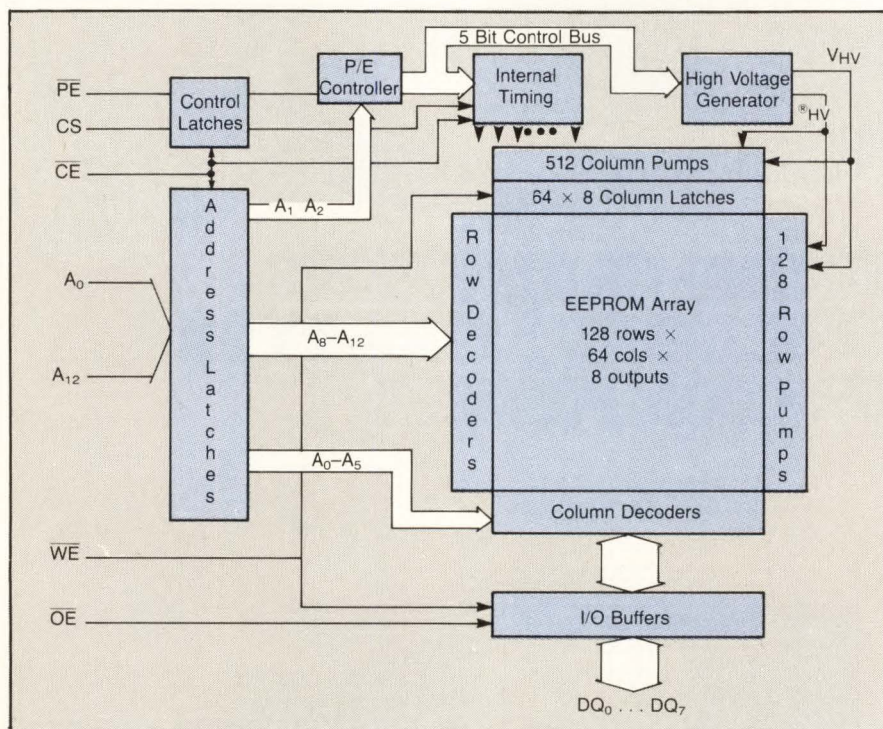


Figure 2: The Inmos IMS3630 8K x 8 bit EEPROM.

munications line and the keyboard and places the data to be displayed in the display buffer memory. This buffer is typically a RAM which holds the data for a single or multiple screen lead (page) or for a single character row.

The SCN2674 Advanced Video Display Controller (AVDC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques.

The AVDC generates the vertical

and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. The AVDC supports four common system configurations of display buffer memory, designated the independent, transparent, shared and row buffer modes.

The first three modes utilize a single or multiple or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of

a single row buffer (which can be a shift register or a small RAM) that is updated in real-time to contain the appropriate display data.

The SCB2675 Color/Monochrome Attributes Controller (CMAC) contains a programmable dot clock divider to generate a character clock, a high-speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the screen.

Both new ICs are available in two standard speed versions: 25 and 18MHz with higher speeds available on a special order basis.

At the same time, Motorola, and Signetics signed an alternate source agreement involving Motorola's M6804 and M6805 families of 8-bit μ Cs and Signetics' 267X family of CRT controllers. As a result of this agreement each company has an assured alternative manufacturing source, thus strengthening their respective product lines.

Motorola is licensed to alternate source the following Signetics parts:

- SCN2670 Display Character and Graphics Generator
- SCN2671 Programmable Keyboard and Communications Controller
- SCN2672 Programmable Video Timing Controller
- SCB2673 Video Attributes Controller
- SCN2674 Advanced Video Display Controller
- SCB2675 Color/Monochrome Attributes Controller

Signetics is licensed to alternate source Motorola's M6804 and M6805 families of 8-bit micro-processor in both HMOS and HCMOS process technologies.

The first seven members of the Motorola M6805 μ C family involved in the agreement are: MC6805P2, MC6805P4, MC6805R2 with A/D Converter, MC6805R3 with A/D Converter, MC6805T2 with Phased Locked Loop, MC6805U2, and MC6805U3.

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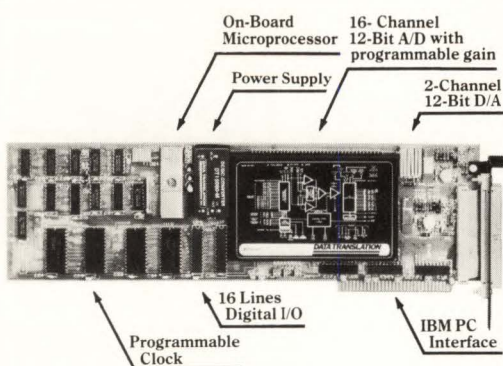
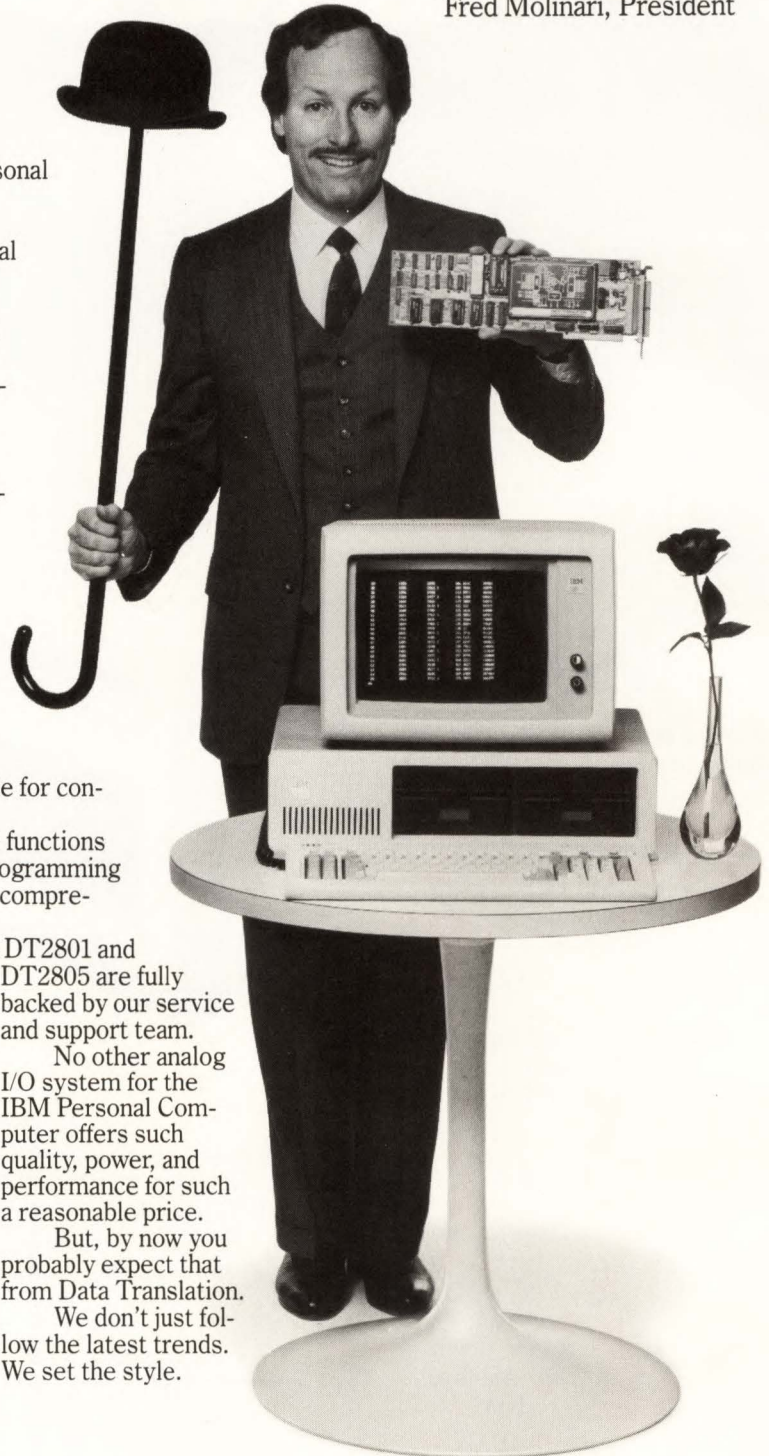
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IBM Compatibility— The IBM PC Comes Of Age



Figure 1: Hercules Computer card replaces the 10M display/printer adapter (display illustrates Lotus Development Corp's 1-2-3 program).

by Jerry Borrell

After two years of explosive sales growth, the IBM PC (personal computer) has not only become a primary contender for the role of top-selling μ C, but is being acquired for a broad range of scientific, technical, and industrial roles as a low-cost alternative computer. In the process, the PC is spawning an enormous cottage industry of suppliers who are applying the system in robotics, signal acquisition, CAD, process control, laboratory functions, and other technical applications. The marketplace for the system is developing so fast that IBM has to change its outlook on

existing markets and refocus its technology announcements in light of new developments for the PC. These industrial/technical developments for the IBM PC indicate shifts likely to occur in the design of related systems.

The PC Marketplace

The announcement of the PC was almost concurrent with changes in the entire marketing structure of IBM, and it is said that both were an indication of the company's ability to change and adapt in response to shifts in the purchasing habits of computer consumers. Industry consultants say that while the PC was not a dramatic advancement in

The ready market that the IBM PC helped develop has led to a migration of the system's application into a quickly broadening industrial/technical market.

small computers, it was effective in establishing the company in the market. It was apparent from its reception shortly after its announcement that the imprimatur of the company had provided the sort of credibility for consumers that guaranteed its success. Other actions by IBM (i.e., providing design diagrams for the product—**Figure 2**) and initiating a program for third party software development insured that it would follow in the successful path of the Apple. One of Apple's greatest strengths has proven to be the army of independent hardware and software suppliers that have adopted the Apple for hundreds of applications. So too have developers provided peripherals, software, and compatible hardware products for the IBM PC. The announcement on March 8th by IBM of a 10 Mbyte hard disk, expansion unit, enhanced system (the XT—which has eight PC card slots), color monitor, upgraded

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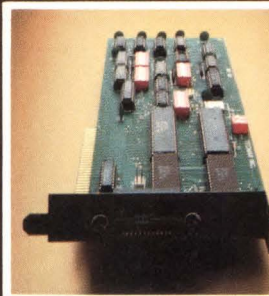
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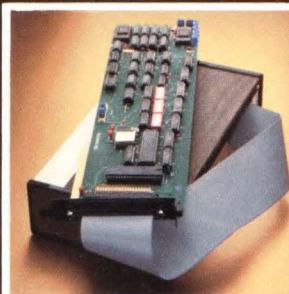
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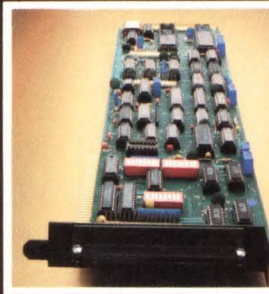
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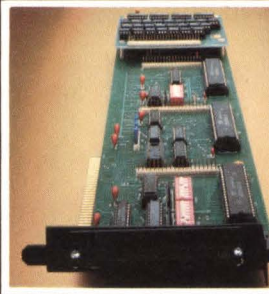
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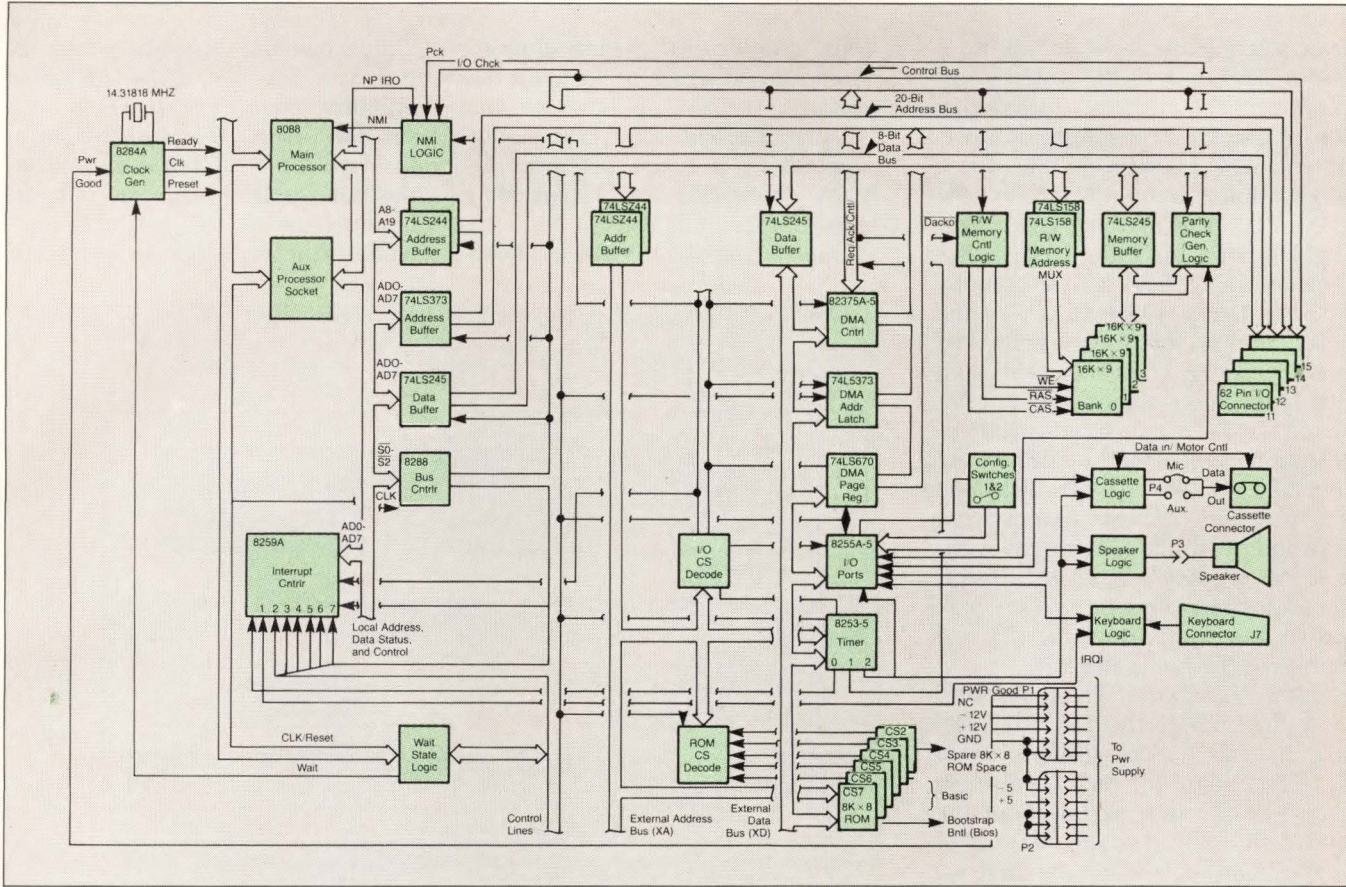


Figure 2: Motherboard diagram for the original IBM PC. XT version retains original cabinet but incorporates a fixed disk drive and 3 additional PC slots.

RAM memory, and additional software indicate that while the company is going to compete for the commodity market of PC related products, it is not going to compete directly with the companies developing specialized products.

International Data Corp. estimates that IBM sold about 195,000 units in 1982, at an average cost of approximately \$5055, for a total market volume of over one billion dollars. Its projections for 1983 are even larger, indicating the sale of 350,000 units in the US and the development of an overseas market of up to 200,000 units. (Brian Jefferey of Strategic Inc. predicts an even larger market for the system of 1 to 1.5 million of the systems to be sold in 1983). To assist in the latter market the firm has announced its intent to invest \$13 million in a plant for Scotland. The company is also said to be negotiating for the rights to distribute the system in Ja-

pan. Newer predictions will be needed in light of the higher price range of the recently announced XT product (prices vary from under \$5,000 to over \$7,000). Early indications are that the company will have greater success in increasing production than was the case after the initial announcement. If successful it will rival Apple and Tandy as the largest producer of a small computer. Analysts also expect further announcements from IBM in this market including a low-end computer suitable for home or personal applications, and a high-end machine that would be designed around a 32-bit processor. It has shown unusual foresight in encouraging the growth of software by removing the \$100,000 dollar royalty limit for authors.

Another emerging market window is in the area of emulation and communication with the 3270 series of terminals. There are estimated

to be over one million 3278's alone installed, and if the IBM can emulate and communicate with this installed base its attractiveness will become even greater. Finally the company is implementing further change in its marketing and distribution channels to insure an increased market share. While the Sears Business Store Centers have proven effective, there are only about 25 at present. Two additional programs are the Dealer Associate Value-Added Reseller, and the Authorized IBM Personal Computer Value Added Dealers (VADS). The dealer associates will deal directly with Sears, Computerland, or other retailers of the PC. VADS will become independent dealers with a direct relationship to IBM.

Industrial/Technical Systems

The ready market that IBM recognition helped to develop in business and education for the PC has,

over the past year, been followed with a migration of the systems' application and related technology into a quickly broadening industrial/technical market. While these applications are nascent for the IBM PC, Andrew Davis, Marketing Director for Data Translation expects that they will eventually grow to between 3% to 6% of the total market for the system. The market is the classic chicken and egg syndrome—users would not demand the PC for such industrial application until the boards were available to allow its use; IBM and the suppliers for the system were unwilling to build the boards without existing demand. In retrospect, the industrial/scientific market may prove more important for the system than the home market.

Data Translation. This Marlboro, MA firm builds the DT2801 (**Figure 3**) and a soon-to-be-released DT 2805 board for the PC; a single board device that performs analog and digital I/O through the use of an on-board μ P. While the 2801 offers 16 channels of 12 bit analog input with a software programmable gain of 1, 2, 4, or 8, the 2805 will offer 1, 10, 100 and 500 signal gain functions. These two products are suited for data acquisition in laboratory and process control environments. Initial system applications include industrial cooking systems, where the board allows remote sensors to monitor temperature and fuel consumption. Analysis and maintenance of process records can also be handled by the PC. In laboratory and instrumentation applications, scientists performing analysis of spectrographic and chromatographic functions require a similar sampling of signals. They may also need to do some post-processing of data, such as Fast Fourier Transforms. Chemical processes in particular require a relatively slow rate of sampling (i.e., 2 times per second) although the PC is capable of much higher rates (13,000 per second). The IBM PC is, however, now merely another instrument for the laboratory, because the user also has the capability to perform report generating and analysis func-

tions, graphics for documentation, and a tool on which to write up the research. In these applications, the PC may become an OEM device supplied by a board producer already configured for a particular industrial/scientific use.

Data Acquisition Systems. DAS

Ohio, has the broadest series of products for the IBM including graphics, memory, expansion chassis, and others. It has also been at the forefront of laboratory and industrial applications. Part of the impetus for its PC products have come from its S-100 bus products,

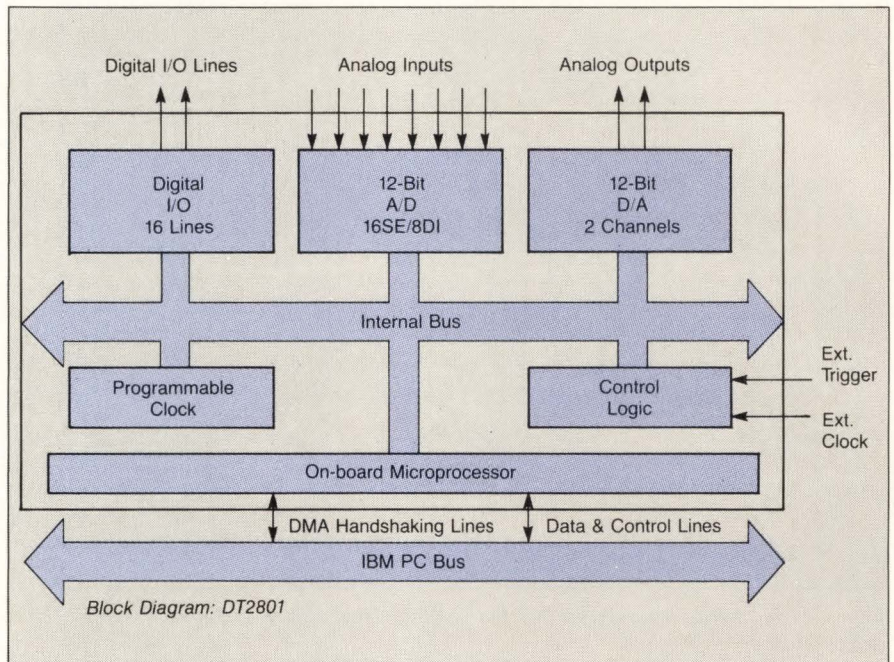


Figure 3: Data Translation's DT 2801 signal acquisition system which is being used in industrial, and scientific system designs.

is a Boston-based firm which offers in its 500 Series three different board-based products for a broad range of measurement and control devices. Capacity may be expanded to 336 channels of 12- or 14-bit analog-to-digital (A/D) single-ended input, and many other combinations of different input, digital-to-analog (D/A) output, pulse counting, and AC and DC power control. Two or more DAS Series 500 systems can be interfaced to the same computer.

The system also includes a software package, called Soft500, that extends BASIC to measurement and control functions, adding more than 40 new data acquisition and control statements. Soft500's foreground/background architecture allows the user to collect and analyze data simultaneously.

Tecmar. Tecmar of Cleveland,

which are paralleled now in PC systems. The DADIO (Digital to Analog, and Digital Input/Output) board has a data conversion rate of 200 kHz, with 12-bit resolution, and is directed towards a variety of control functions. Among current applications is Koch Hydrocarbon of Oklahoma which uses the board for monitoring fire control in pipeline systems. Another of its products allows for simultaneous independent control of two stepper motors. The board implements a CY512 peripheral controller chip to control step rate, acceleration, number and direction of steps. Application areas for this board include robotic devices. The company's Lab Master board system is designed for D/A and A/D conversion with 12, 14, or 16 bit resolution for up to 256 channels with the use of expansion boards, and 1, 10,

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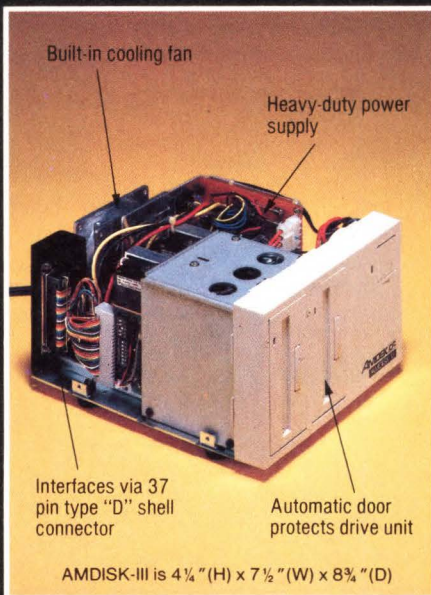
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Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	1
Disk Speed	rpm	300
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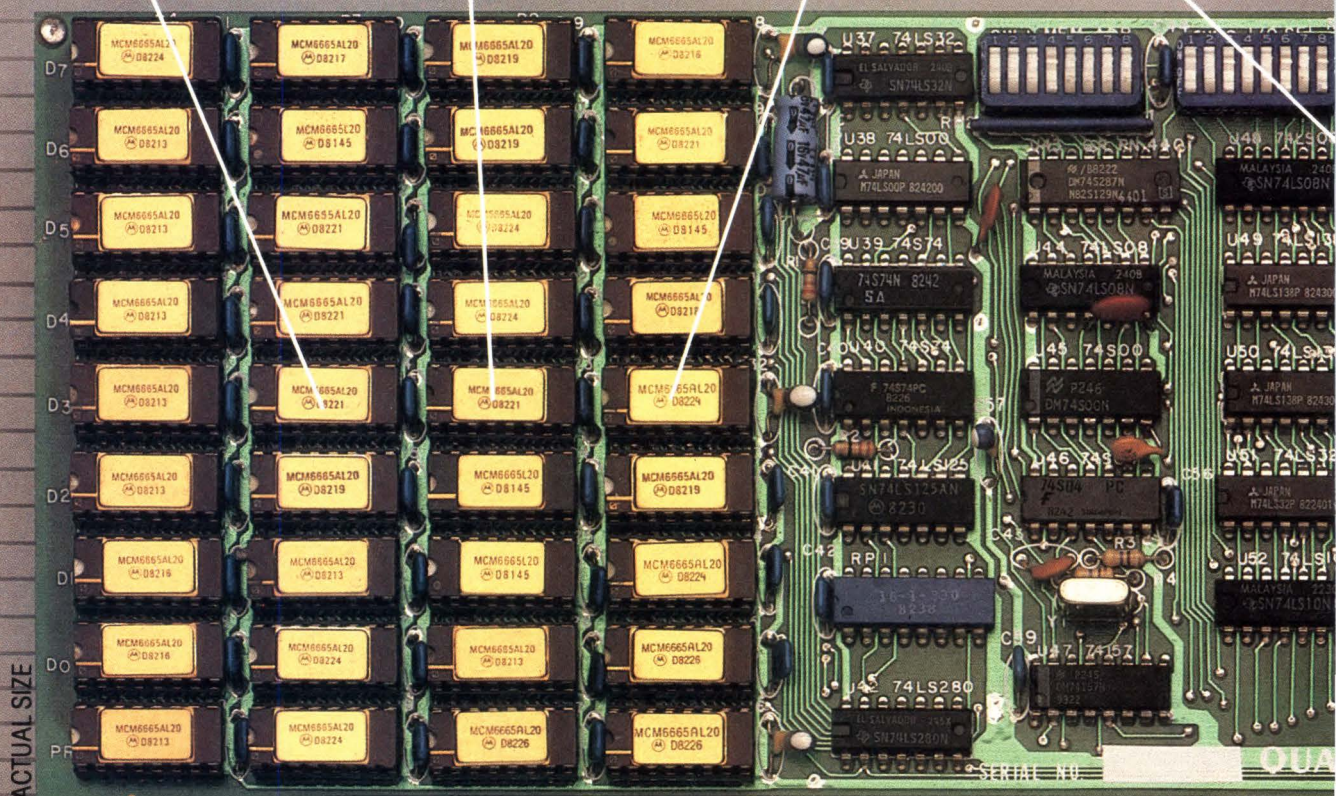
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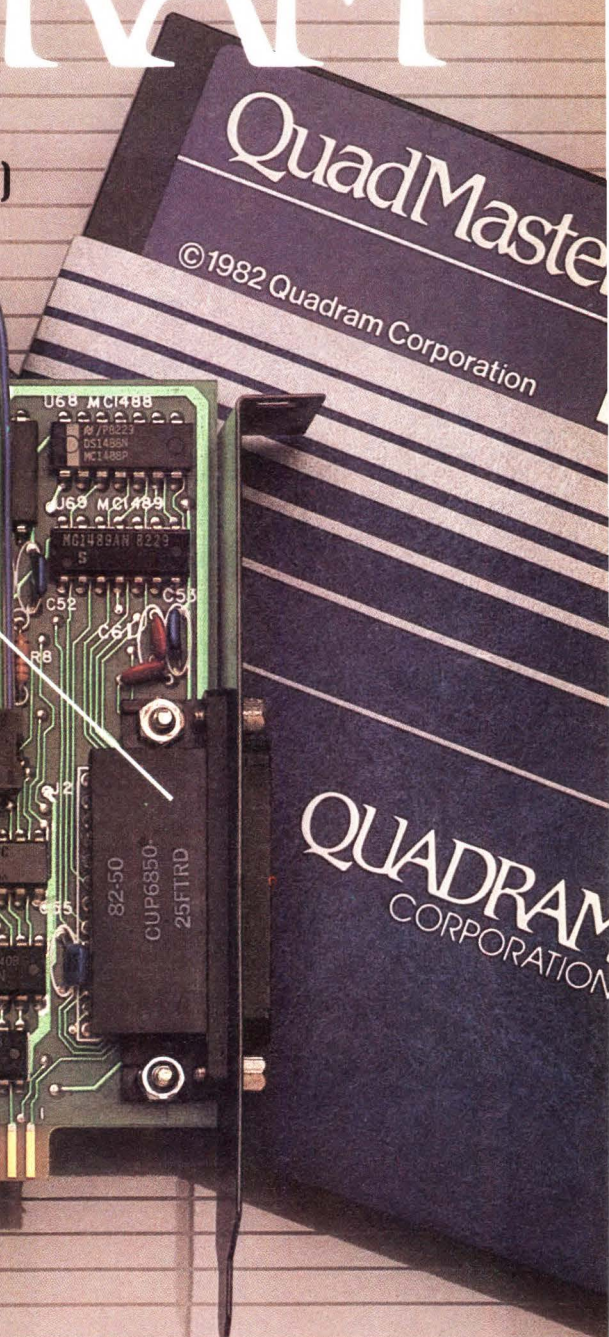
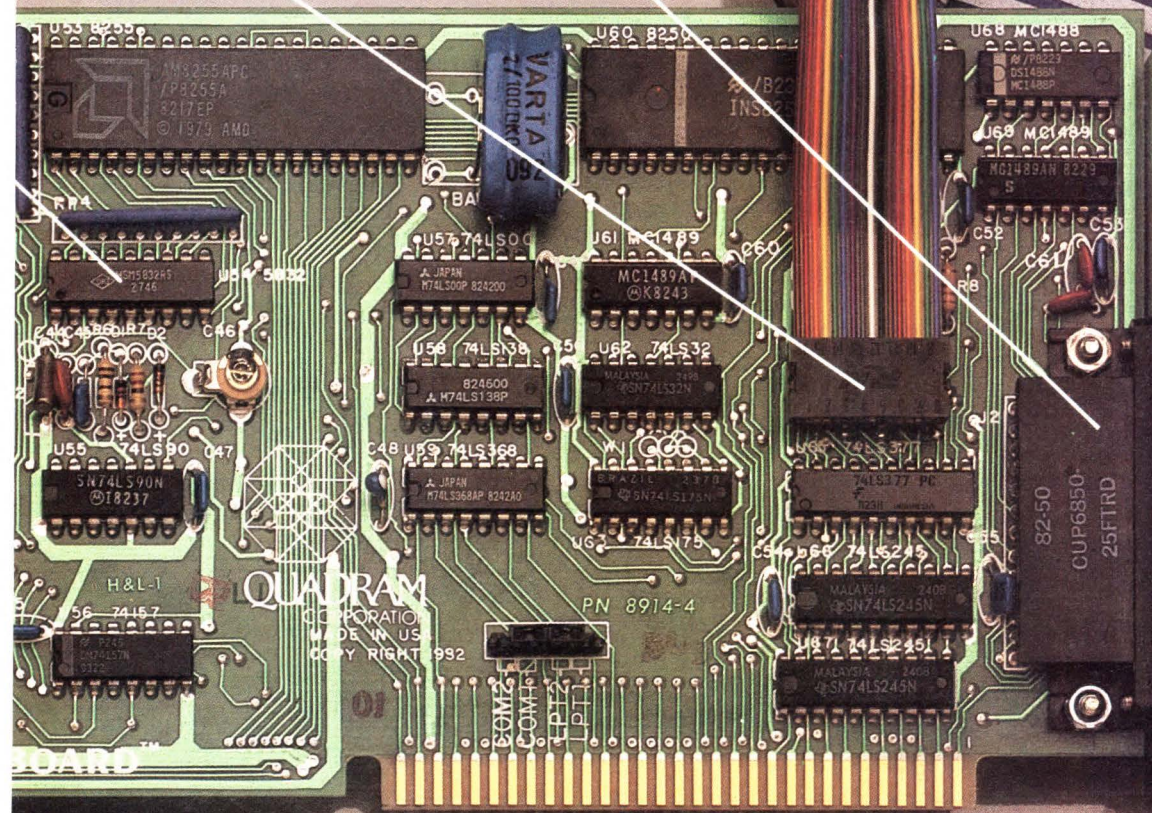
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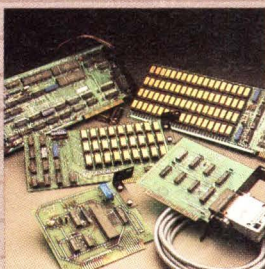
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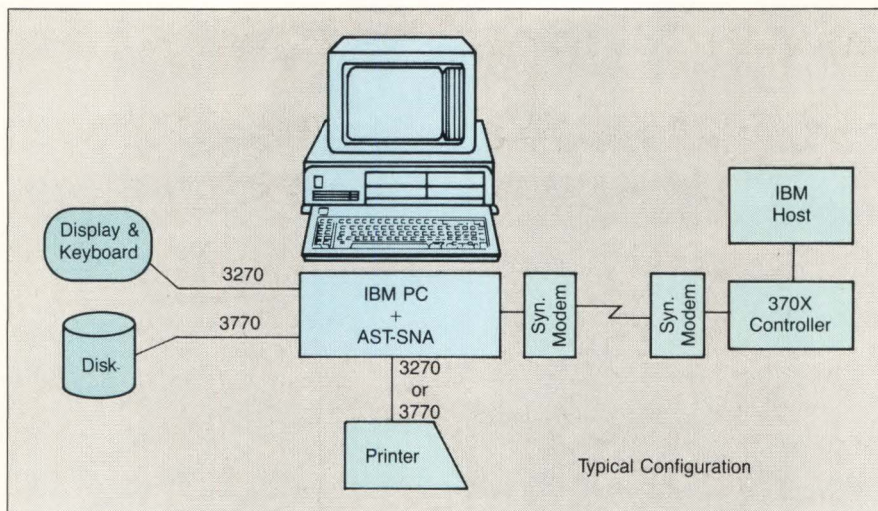


Figure 4: AST Research system diagram for 3270 terminal emulation. AST offers comprehensive facilities for terminal emulation or the PC providing access to several mainframe manufacturers.

100, and 500 signal gain options (with other configurations possible). The board uses 2 DAC80 converters, an AMD 9513 timer, and an 8255 parallel port and can support up to 24 digital I/O signals. An IEEE 488 interface board provides talker, listener, and controller functions. As such the board is directed at instrumentation interfaces for process monitoring, offering programmable data transfer rates, and selectable hardware interrupts.

Two more advanced products are designed to allow the PC to be implemented for newer computer applications including machine vision and voice I/O. The Video Van Gogh board is a video digitizer interface which can accept camera signals from either NTSC or industrial composite (EIA) video. The signal can address up to 256×256 pixels, and with 8-bit value for intensity; it is capable of 256 levels of grey scale. While the company promotes the system for applications in microscopics, signature recognition, robotics, and pattern recognition (for assembly line inspection) there is probably little developed software for the IBM system in this area. The company's parallel product for the S-100 board is in use at Ford for a pattern recognition application. Given large companies' penchant for the purchase of well-known manufacturers' products,

the device will no doubt have a large growth potential.

The PC-Mate (expansion unit) supports the Speech Master voice digitizer, and Speech Mate software. The company claims this is being considered for factory automation applications in which workers may call out the status of a process or project to control an action or supply of materials.

Computer Graphics

In some ways computer graphics appear to have been neglected by IBM. While the resolution support-

ed with the initial announcement was at 640×200 , IBM offered a color graphics card but no color monitor. However, with its XT System announcement the company has introduced an IBM RGB monitor with 16 displayable colors selected from a palette of 256. While the system still lacks any IBM interface to I/O devices such as tablet, mouse, or digitizers, other are actively seeking to fill the marketplace. Riva Terminals Ltd, of England is one of the first companies to have addressed the graphics market. The company's PC 1024 is a 20" monochrome device, with a resolution of 1024×780 (as a window on a total display capability of 1024×1024). In a terminal mode, the system can emulate the Tektronix 4014, as well as DEC VT52 terminals.

Quadram Corp. of Norcross, GA also supplies a large format (17") monochrome, raster display for the PC but has chosen to keep resolution at 480×260 . The terminal is DEC VT 100 compatible, and may be sold with a Plot-10 graphics option. More recently, the company has introduced a 12" RGB monitor, with 690×480 resolution. Quadram also produces three 16-color PC boards for use with its monitors with 640×200 or 640×400 resolution. Other RGB monitors for the system are now produced by Amdek, Sony, and Electrohome (as well as IBM itself for the XT ver-

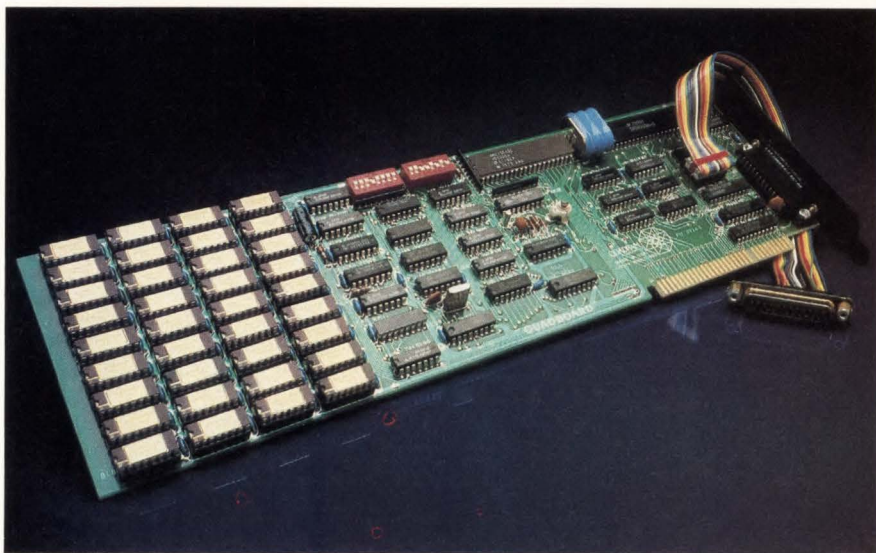


Figure 5: Quadram Corp's Quadboard for up to 512K of additional RAM.

sion of the system).

Hercules Computer Corp. of Berkeley, CA produces a card which replaces the IBM Display/Printer Adapter and allows a monochrome display of 720×348 on the IBM monochrome monitor (**Figure 1**). The board also offers a light pen interface. The Hercules board is currently being implemented in 3D CAD applications and for 2D PC board design.

Terminal Emulation

One of the recurring demands for the PC has been to use it as an IBM terminal emulator. In the fall of 1982 the first such emulation hardware/software packages were released by DataSource Systems Corp. of Minneapolis, MN. IBM quickly followed suit to ensure that it would maintain control of the market for terminals compatible with its mainframe products. There are two protocols supported by IBM for the PC, the Synchronous Data Link Control (SDLC) for the SNA environment, and the Binary Synchronous Communications (BSC) Protocol. IBM also provides a 3101 emulation package, and a 2.0 version of Asynchronous Support Communications Support Package, allowing the PC to work as an asynchronous teletype terminal.

Other companies providing emulation packages include Forte Data Systems of Santa Clara, CA who offer a 3278-2 terminal emulator, Aztek, of Ottawa, Canada, also selling a 3278 emulator, and Techland of Mt. Vernon, New York (any 3270 device is emulated under SDLC).

AST Research of Irvine, CA probably offers the widest selection of IBM terminal emulation software/hardware products. AST-SNA (**Figure 4**) provides the PC with the ability to emulate the 3274, 3278, and 3770 communication terminal, while AST-3780 allows the terminal to emulate IBM 2780/3780 RJE workstations. The latter has particular importance because it will provide the PC with the ability to communicate with IBM 370, 4300, & 3000 series computers as well as

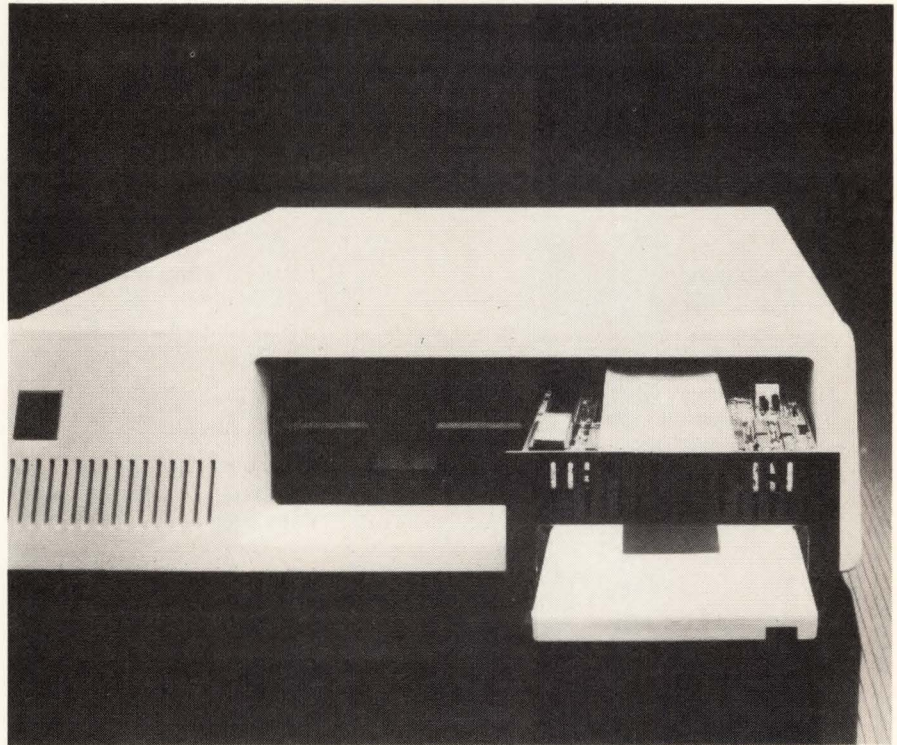


Figure 6: Mbyte cartridge Winchester drive from Tecmar, Cleveland, OH.

UNIVAC, CDC, Data General, DEC, Wang, Honeywell, and others. Microlog of Suffern, NY, which makes Z-80B based Baby Blue products for 3270, 2780/3780 emulation, may be the first company to offer 3279 graphics terminal emulation for the PC. This will allow designers to consider implementing more advanced, high resolution packages of systems as such offered by the Spectragraphics Corp. Dennis Murray, VP sales of Microlog, indicates 3279 development is possible under the XT version of the PC. The Baby Blue products have an additional advantage in that they allow the PC to run CP/M 80 based applications.

The most important implication of the emulation work is that the PC becomes even more attractive for acquisition or for developing applications software—the installed base of IBM terminals is well over one million. The advantages occur through the benefit of acquiring additional terminals for mainframes that have standalone capability, or of adding access to mainframe processing and data for a μ C. There

are further advantages for the industrial and scientific developments mentioned earlier in that the PC's functions become enhanced by mainframe access. In addition the company released simultaneously with its XT product a conversion kit for its 3270 terminals which will allow it to become a PC. The additional push that this is likely to give to applications development is not to be underestimated.

Memory and Peripherals

One of the primary constraints mentioned by applications developers for the PC has been the limitation of PC slots. Only five are available on the original product, and all of them can quickly be filled up by memory expansion, clock, communications adapter, and other basic cards. The XT announcement was based upon a redesigned motherboard with eight slots, but if the XT is configured with communications, and hard and floppy disk drive interfaces, then only five remain. In addition the expansion comes at a cost of width to the cards, which are now only al-

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Microlog Corporation
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Write, 342

Quadram Corp.
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Riva Terminals Ltd.
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Woking, Surrey GU21 5JY
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Tecmar Inc.
Personal Computer
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Cleveland, OH 44122
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lowed $\frac{3}{4}$ " per slot—a problem for any of the cards that have piggy-backed ICs, analog devices or sub assembly cards. This internal limitation has had two results: designers have developed multiple function boards, and expansion chassis to allow the implementer more freedom.

Quadram. Quadram Corp. of Norcross, GA (recently merged with Intelligent Systems Corp.) is one of the largest producers of IBM PC products in the country. The firm has acquired recognition for its multiple function board for the PC—Quadboard II for example combines six functions: 2 serial ports, chronograph, up to 256K of expanded memory RAM drive, and printer spooler. Other products of the company will provide up to $\frac{1}{2}$ Mbyte of memory and a communi-

cations interface (**Figure 5**). Similar boards are provided by Profit Systems (clock calendar and 512 on board RAM), Seattle Computer and several others. Seattle also sells an 8087 co-processor for the IBM cpu (8086) which considerably enhances speed of operations.

For those designing applications with the PC, Apparat Inc. of Denver makes an EPROM programmer at a very low cost, but which is suitable only for low volume production of PROMs. In terms of additional memory, Tecmar, mentioned above has offered 10 Mbyte drives, and a 5 Mbyte removable Winchester for several months (**Figure 6**). The announcement of a hard disk by IBM may affect the price and profitability of secondary suppliers, but other sub-systems are being designed based on the new XT.

Summary

The rapidly developing marketplace for the system has changed IBM strategy concerning existing markets and has led them to refocus in light of new PC developments. The response to the PC is pushing secondary suppliers into the industrial and scientific market rapidly. One of the greatest problems for designers is in developing the analog interfaces (both software and hardware) to the outside world. However, the results are providing scientists and industrial users of computers with new avenues of access to digital technology. The opportunity with the system today is for the designer who must have an understanding of both the application, and the likely shifts by IBM to retain the largest product markets. □

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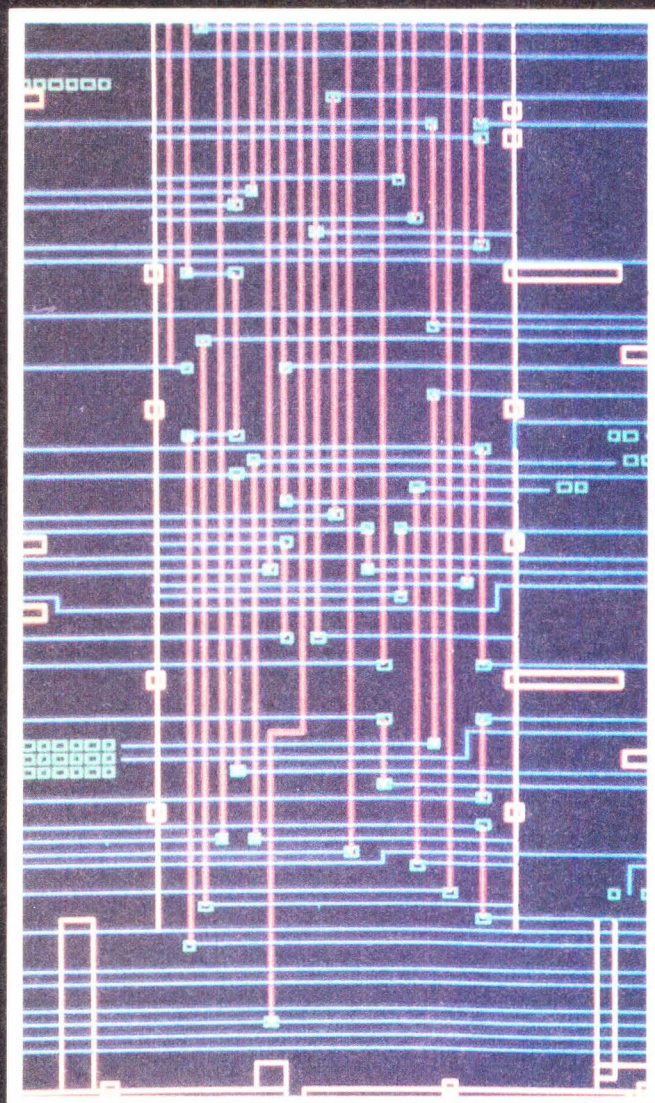
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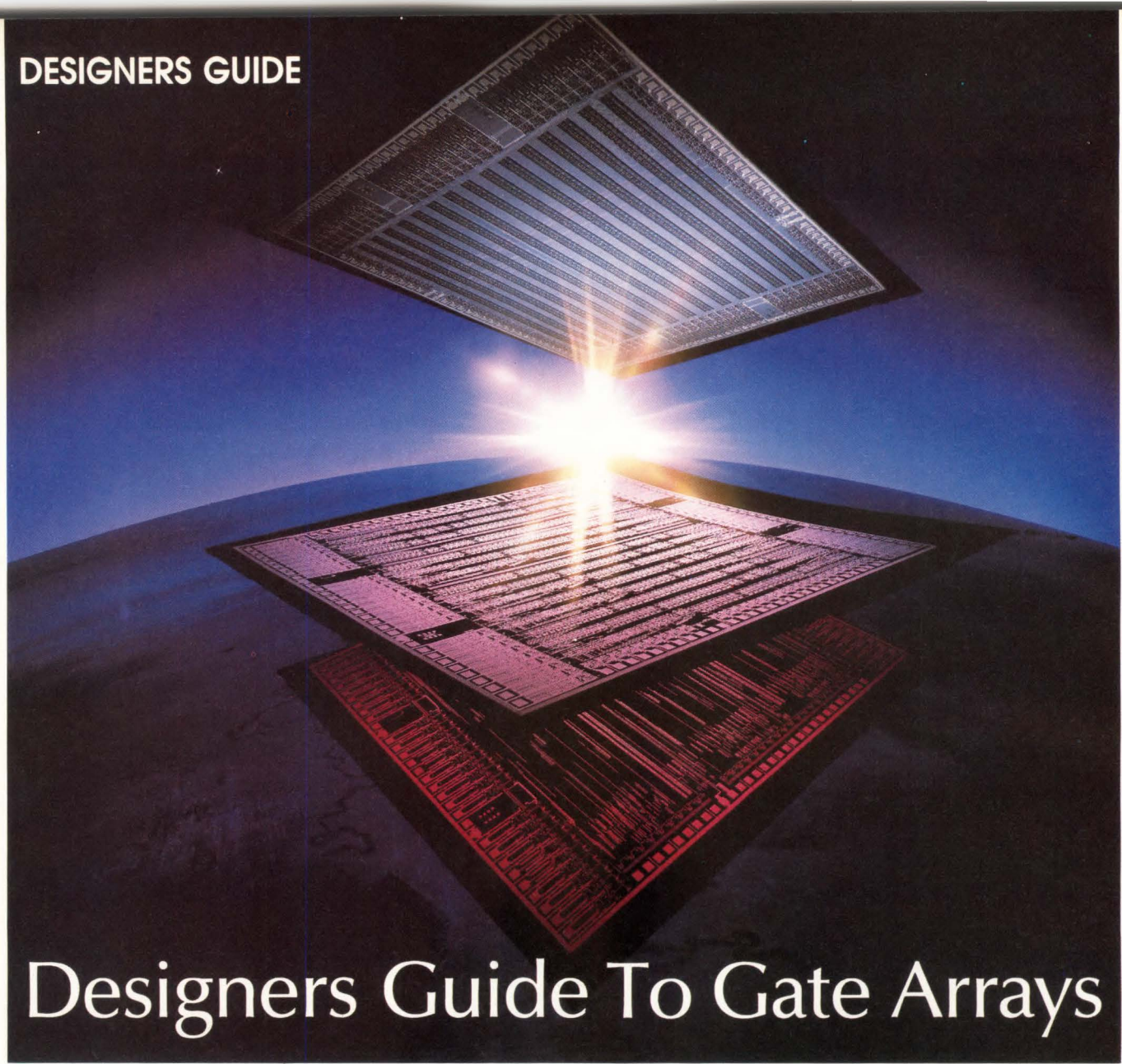
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Designers Guide Series



Gate Arrays



Designers Guide To Gate Arrays

photo courtesy National Semiconductor

by Douglas Eidsmore, West Coast Technical Editor

Larger, faster gate arrays and more powerful design tools are the trend but upfront decisions can make or break a design

Driven by design automation hardware and software, the demand for new circuitry and a shortage of IC designers, the gate array market should reach \$9 billion in 10 years. There are now over 60 vendors on the gate array bandwagon. Indications are that designers are rapidly shifting from redesigns of existing systems to new designs that take advantage of the performance, privacy and reliability of the semi-custom approach. The technology is now so advanced that it is used by semiconductor companies to produce standard parts.

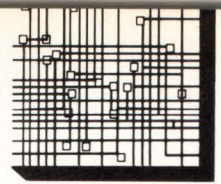
Gate Array Benefits

The advantages of gate arrays are numerous and well-documented. When compared with discrete ICs, implementing a system on a gate array can save money both in the circuitry used and in supporting hardware, such as power supplies. Because parts count is lowered, inventory and associated inspection and maintenance costs are also reduced.

Fewer parts also means improved reliability. Some failure analyses show that 70% of printed circuit board system failures are due to faulty interconnection—i.e., device to circuit board, bonding wire to package pin, bonding wire to die, and die to package. A 2400 gate array device can replace over 70 SSI/MSI ICs, resulting in a system with 10% of the interconnects of a discrete-based system. Putting interconnects on-chip also means improved performance with higher speeds and increased throughput. Power savings over discrete designs are an added benefit.

Which Technology?

One of the first tasks is to decide if the gate array approach is appropriate. The characteristics of gate ar-



rays must be compared with competing custom technologies: standard cells, full custom and programmable logic arrays. None of the custom approaches is a panacea but each is appropriate for its own set of applications.

Full custom offers full functional freedom but, even with CAD and silicon compilers to streamline development, is costly in both time and dollars. High volumes and/or high performance must be required to justify the relatively high investment.

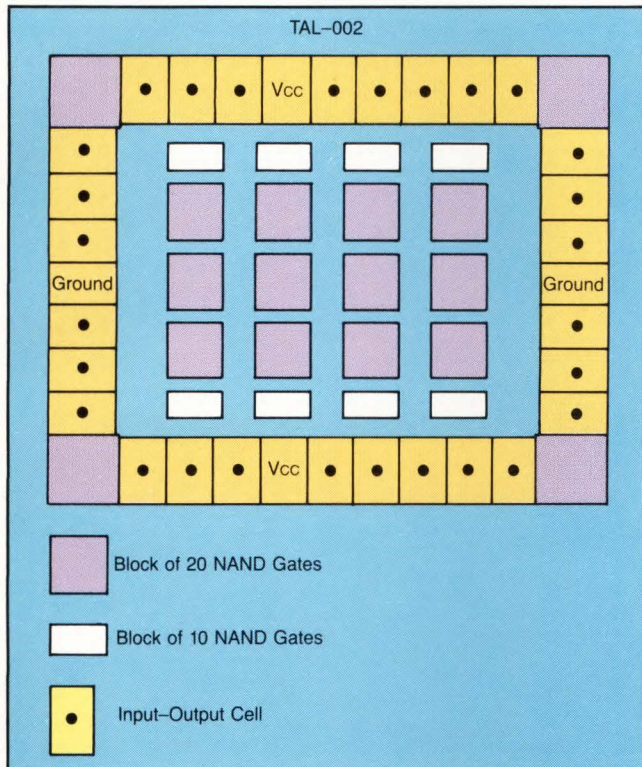


Figure 1: Small arrays such as Texas Instruments' TAL-004 with 500 gates and TAL-002 with 320 gates can easily be placed by hand. Grids representing macrocells can be pasted onto layout sheets similar to the one above.

Programmable logic arrays (PLAs) are excellent where low volumes and low gate counts are all that are required. Personalized with a PROM programmer, PLAs are often used to create prototypes of parts to be built using other custom technologies. Semi Processes Inc. recently announced a series of silicon gate CMOS arrays that can be programmed using the logic equations used to create a PLA. This conversion is so simple that the company is quoting 8 weeks turn-around from receipt of PLA equations to CMOS arrays.

At one time PLAs were slower than the discrete ICs they were designed to replace. But programmable logic array performance is continually improving. Monolithic Memories' (Sunnyvale, CA) latest programmable logic arrays are implemented in a self-aligned washed emitter process to attain propagation and frequency time improvements of 36% and 50%, respec-

tively, over previous offerings. PLAs are available from several manufacturers, including Monolithic Memories, AMD and Signetics.

Standard cells compete most directly with gate arrays. They are especially attractive as a gate array alternative when special functions, such as high function comparators or differential amplifiers, need to be implemented. Gate arrays, on the other hand, are a fixed grid of logic cells and are most useful in implementing circuits composed of random or sequential logic.

Since standard cells must be processed from the ground up, development is typically more costly and time consuming than with gate arrays. However, this is not always the case. Some circuits are a poor gate array fit, and a standard cell solution is easier and faster than cramming or gerryrigging the circuit onto a gate array. George Stephan, President of Universal Semiconductor, describes standard cells as "characterized by elegant engineering and inelegant manufacturing." The reverse is true of gate arrays, he claims. Gate array design is restricted by fixed logic geometries, inability to implement complex macros, and fixed I/O buffers. Standard cells can be designed with special cells, easily accommodate hierarchical design and are not limited by I/O restrictions.

On the other hand, standard cells are less flexible in terms of making design changes and in varying production quantities than are gate arrays. Gate arrays, with their reliance on partially processed wafers, require fewer masks for personalization and therefore for redesign. Another less obvious reason for the flexibility

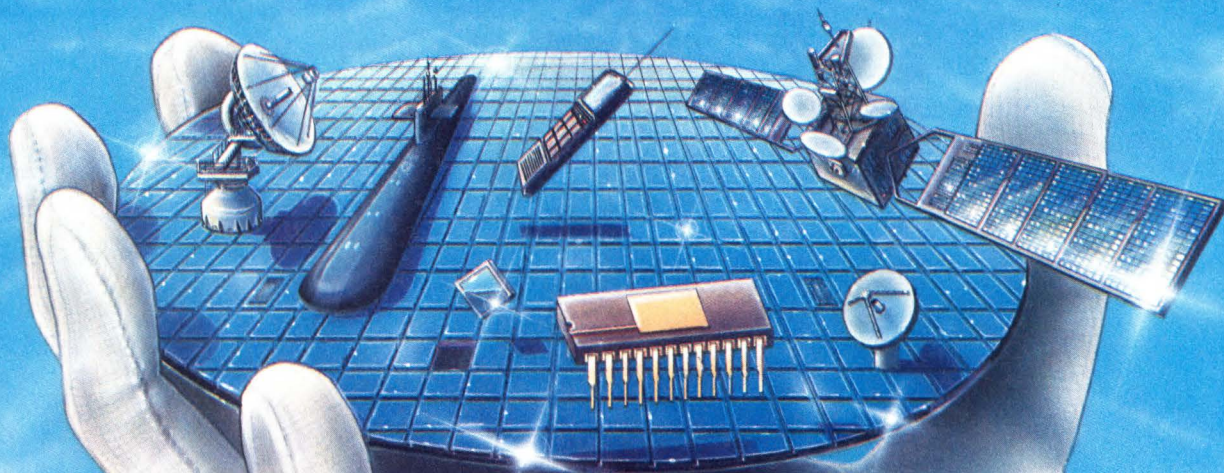
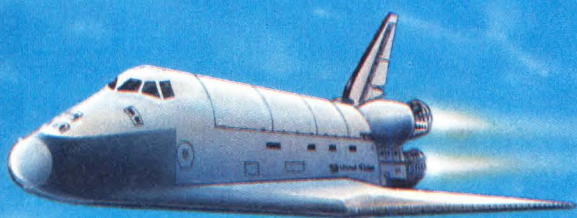


Figure 2: Motorola metalization mask patterns. Company's MOSAIC process is used to fabricate low power Schottky arrays, including MCA2800 ALS as well as ECL arrays. Three masks are required: one for each metal level and one for via holes.

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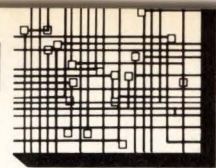
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of gate array manufacturing is that since the gates in an array are never fully utilized, the remaining gates can be used to implement a last minute design change or to add features in a redesign.

Matching the attributes of the various custom approaches with turnaround and production requirements of the circuit, as well as size and operational needs, will allow selection of a custom technique. If gate array technology seems promising, the next step is to start looking at the circuit in question as a gate array.

Circuit Partitioning

Partitioning the circuit into logical modules is a first step in fitting the circuit to an array. The goal is to identify the circuitry that is "arrayable" and that which should be implemented with standard parts. Because each vendor has his own "modus operandi" there is some disagreement about whether vendors should be approached before or after partitioning. Bill White, Director of Gate Array/Standard Cell Products with Harris Corp., feels the vendor can help the designer avoid sending out RFQs for a gate array with 500

gates and 400 pins. In most cases, a rough partitioning will be required before selecting an array vendor.

Fitting an existing PCB-based or new design to an array are somewhat different processes. Partitioning of existing logic involves blocking out and combining as many TTL glue chips as possible with an eye towards minimizing I/O. If a new system is under development, the designer works from his logic diagram and builds abstract blocks such as ALUs, register files or multiplexers.

The next step is counting or estimating the number of gates in the circuit. A crude estimate can be made by using the rule of thumb that a typical MSI circuit will require 60-75 gates. LSI Logic Corp and other vendors publish gate equivalents for popular TTL components; Universal Semiconductor offers a slide rule that makes the conversion almost automatic. Such a gate count conversion should take into account the processing technology. Flip/flops are implemented in fewer gates with CMOS than bipolar, for example.

Selecting a fabrication technology is another early design task. The performance and I/O of the array must meet the requirements of the system. Fortunately,

The Economics of Gate Arrays

by Allan M. Cox, Marketing Manager Digital Products, Interdesign, Scotts Valley, CA

The cost savings of moving electronic products based on MSI standard IC families to LSI semi-custom gate arrays have become too significant for the product designer to ignore. Also, the gate array based product manufacturer can get to market fast, with significant advantages in addition to cost. It is hard to envision designs in the 80's being implemented in anything other than LSI/VLSI standards (such as μ P families and codecs), standard memory and semi-custom.

The relative costs for custom, standard cells and gate arrays are generally summarized by the curves in **Figure 1**. Designers strive to follow the minimum cost curve. To do that, it's necessary to know the cross-over points A, B and C. A, B and C, however, can vary by as much as two orders, due mainly to device complexity. Device complexity and hence silicon area is a major factor in device cost. However, at the lower complexities, die cost tends to become less significant, and product cost is dominated by packaging, testing and labor costs. The vendor with access to a high yielding process and low

wafer costs has the ability to push the gate array/standard cell cross-over point (the annual volume between A and B) to a very impressive limit.

It is not uncommon today to find gate arrays meeting volume requirements of 50 thousand to 250 thousand units per year, and occasionally up to 500 thousand per year. Efficiently utilized arrays are even now

filling annual production requirements of over 1 million units annually.

With the prospect of continued learning curve and volume production economics coupled with the inherent flexibility, fast response and design cycle of gate arrays, the product and system designer has available the tools he needs to meet his challenges in the 80's.

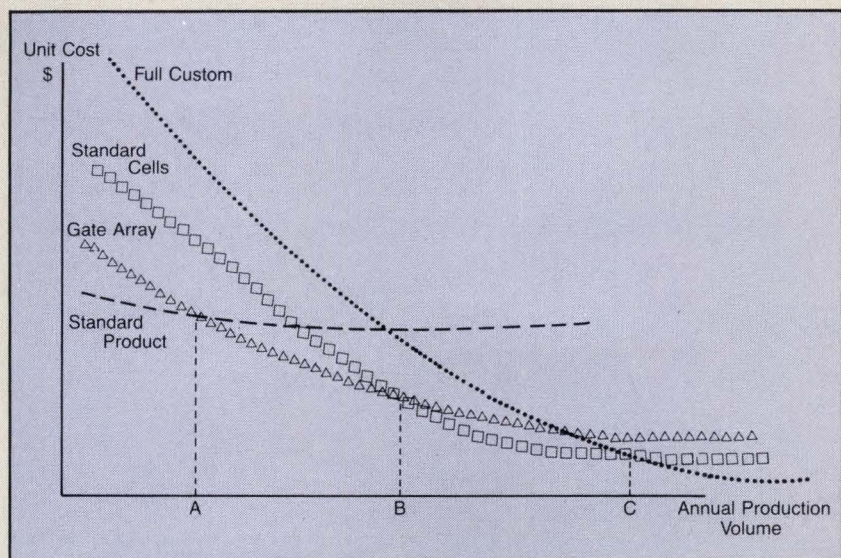


Figure 1: These curves represent the costs of full-custom, standard cell, gate arrays, and standard product approaches based on annual production volume. Points A, B, and C represent the cross-over points of the various approaches.

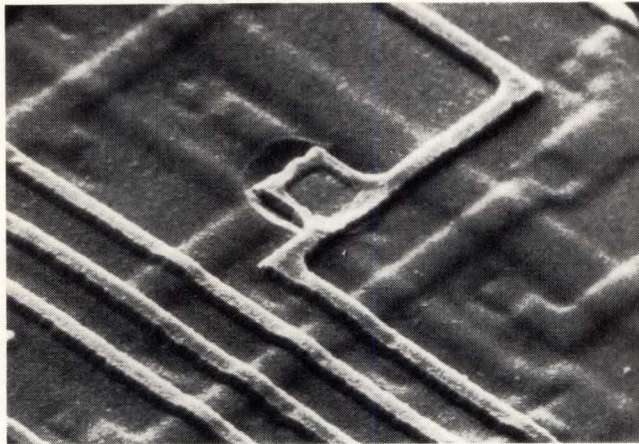


Figure 3: Electron microscope photo of double level metal CMOS array from International Microcircuits, Inc. Via holes connecting first and second mask can be seen.

gate arrays are fabricated in a range of processes, each with unique density, speed and power characteristics. The trend is clearly towards CMOS and ECL. CMOS clock rates are 40 MHz and better, with 2ns delays and very low power consumption. ECL boasts 300 MHz clock rates and gate delays of less than 500ps. Low power Schottky TTL is also a solution for many applications and has proved to be very durable in the marketplace.

CMOS is available in metal gate and silicon gate versions. Silicon gate CMOS is faster and denser than

metal gate. Metal gate CMOS arrays are limited to about 500 gates, whereas 3 μ silicon gate arrays with 10,000 gates and extremely high speeds have been announced. As line widths drop, even higher gate counts and speeds will be available, especially with oxide-isolated silicon gate technology. CMOS arrays have been used to great advantage as collectors of the glue circuitry surrounding μ Ps. With 2 μ and finer geometries, CMOS arrays will challenge ECL as the technology of choice for semicustom CPU circuitry. Storage Technology (Sunnyvale, CA) is developing their new line of IBM-compatible mainframes from such technology.

Arrays are presently personalized by one or two metal levels. Double level metal results in a denser array than single level. Interconnections, and therefore, delays, are correspondingly shorter, and as a result higher speeds are obtained.

Double level architecture offers much greater layout flexibility than single level configurations with double level metal arrays. Automatic placement and routing can therefore be used effectively. Single level arrays are almost always placed and routed by hand or interactively at a CAD station. However, Signetics now offers automatic routing and placement on its new single level metal CMOS arrays.

When reviewing a vendor's product line, attention should be paid to more than technology and gate count. The positioning of the product line and the gate count iterations are also important. One tactic for achieving high silicon utilization is effectively matching the gate count of the circuit to be implemented, with

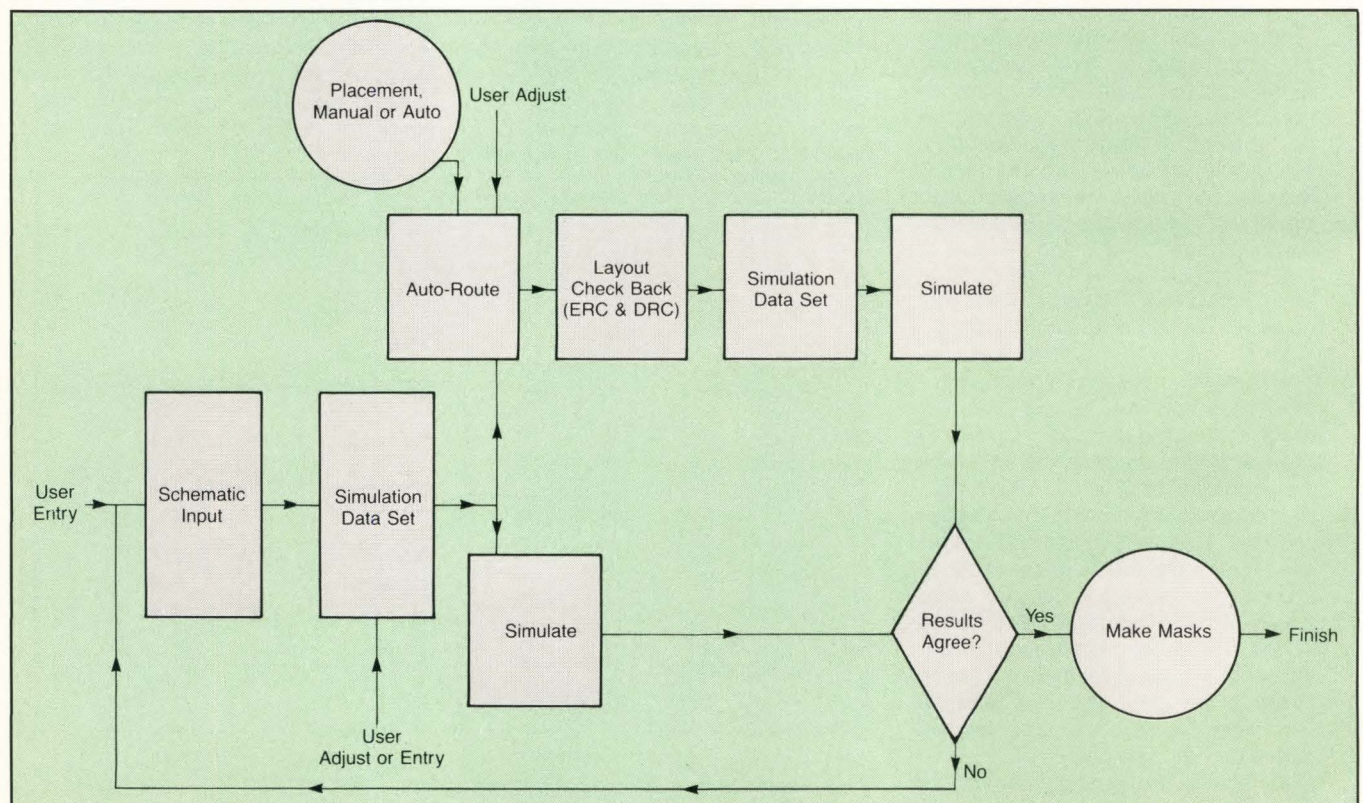
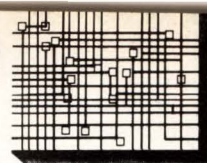


Figure 4: Plessey Semiconductors' semi-custom array mask production (SCAMP) flow chart.



the number of gates on an array. Placing a 480 gate circuit on a 600 gate array uses silicon more efficiently than if it were placed on a 800 gate array.

Design Cycle

An important consideration in selecting a vendor is the design cycle used, not only in terms of turnaround time but in terms of the type of user participation required or allowed by the vendor. Working with a gate array vendor is much more intimate than purchasing parts off the shelf. Some vendors encourage customer participation through the design cycle, while others do not. Most are flexible and allow customers to enter a design cycle just about anywhere. The customer may do none of the design, or he may submit a final design on a pattern generation tape. In general customers can save money by accepting part of the design responsibility, but they also assume a greater risk if the part is discovered to have designed-in flaws.

If a customer chooses to participate in some phase of the design, the location is another consideration. Usually, customers go to a vendor's facility for training and to do the design. A cozier situation would be to work at one's own facility. In such a situation the customer would either do a hand layout (for a small array), use a company-owned Engineering Work Station (Daisy or Mentor Graphics) or larger CAD system, or

work at a terminal with a line, such as Harris' Dial a Chip, to a vendor's CAD system. The problem with such arrangements is lack of vendor support.

Many companies have established or are establishing regional design centers. Such centers combine the best of both worlds: vendor support and a facility near the customer's home. Motorola and Texas Instruments were among the first to establish design centers. But the idea is catching on. Some companies are adding design centers to their regional sales offices.

Lack of alternate sources has been, in some people's eyes, a major flaw in using gate array technology. In reality, most customers' volumes are small enough that the risk in using a single source is fairly small. If a problem should occur during production most vendors can fall back on their own alternate foundry sources. A greater problem could arise if a disaster were to occur to a customer's design facility at a crucial point in a design. For many users both problems have been solved because several gate array vendors have agreed to share processing technologies and design tools. Some of these agreements include: Texas Instruments and Harris Semiconductor, Motorola and National, LSI Logic with Toshiba and Advanced Micro Devices, Universal Semiconductor with Siliconix and Nitron, California Devices and Telmos, and Interdesign and GTE Microcircuits.

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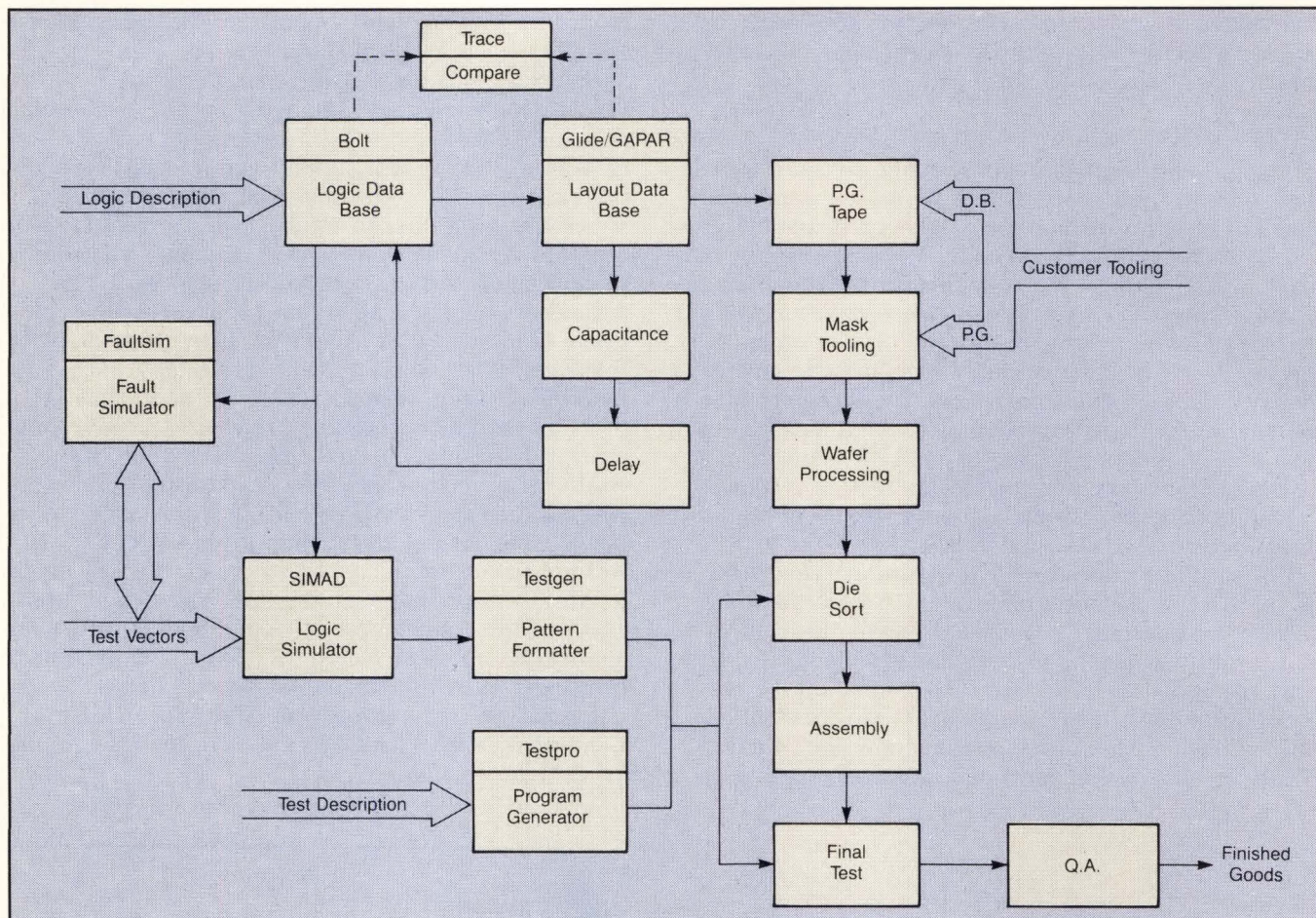


Figure 5: AMI's GA series development flow. The heart of the system is BOLT logic data base. Using common data base allows conversion of gate array to standard cell or full custom circuit with minimal risk.

Design Process

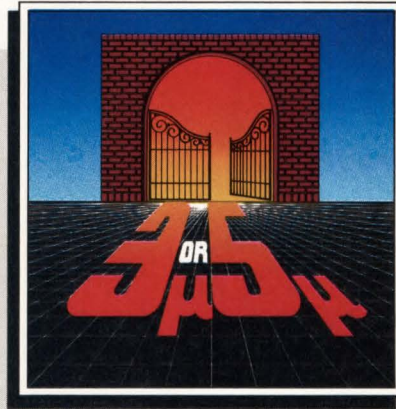
Once the vendor and virgin array have been selected, the design cycle begins. Each vendor has his own unique design process, but there are some universal tasks that must be completed. The functional logic design has to be entered into the vendor's system. This is often called schematic entry. It may occur at a work station as the logic design takes place or it may be entered via a digitizer from a layout drawing. The entered logic description is often said to have been "captured." In some systems, the logic is defined as it is entered in the format of the vendor's macrocells. The macrocells are used to create a network of higher and higher levels of integration. This process is called net list or network entry.

A simulation of the entered logic is then performed. The operation of the entire gate array or blocks of it may be simulated. The purpose of the simulation is to verify that the description entered into the CAD system truly represents the circuit as the designer intended it to. The simulation is usually run using TEGAS software from COMSAT Corp (Austin, TX). Many companies use their own simulation/verification software and some of them have developed translators to convert to TEGAS formats. COMSAT has developed

a new software package called TEXTSIM that accesses a library of delay data, rather than relying on the unit delays used in TEGAS. LSI Logic is probably the first vendor to incorporate TEXTSIM into a design system. Their LDS system goes a step further. They use nominal delays that are based on estimated wire lengths before layout for a more accurate simulation. After layout the simulation is repeated.

The simulation data is fed into a test verification program. Critical timing paths are scrutinized at this point and race conditions investigated. Some vendors automatically evaluate the nodal activity as part of the test program generation. Such an evaluation is performed in an effort to determine the testability of the array. This evaluation may include a complete fault grading. In fault grading each node is examined to make sure that, if the node were stuck at 0 or 1, the fault would be detected from the array's I/O. This procedure is an option with most vendors because it eats up so much computer time. Even using mini-computers, fault grading can take several hours. Instead, an estimate of the node coverage or nodal activity can be made and a testability percentage determined. The latter procedure is usually adequate and saves hours of expensive computer time.

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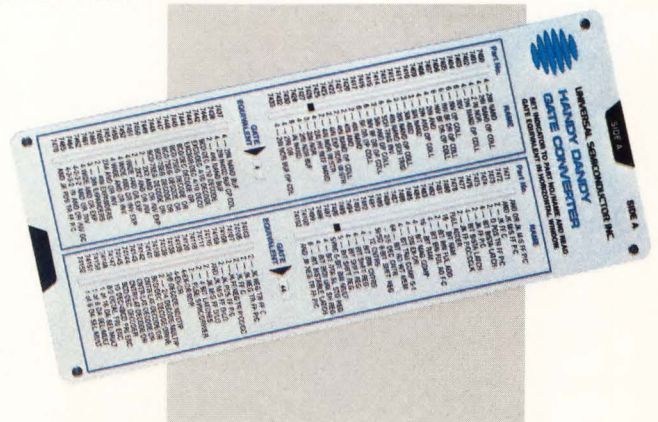
Type	Gates	Size	Speed	Pads
1S03 or 5A	360	118 x 140	50 or 25MHz	44
1S03 or 5B	540	132 x 167	50 or 25 MHz	58
1S03 or 5C	720	159 x 167	50 or 25 MHz	64
1S03 or 5D	960	161 x 208	50 or 25 MHz	70
1S03 or 5E	1200	188 x 208	50 or 25 MHz	74
1S03 or 5F	1500	188 x 244	50 or 25 MHz	80
1S03 or 5G	1800	202 x 230	50 or 25 MHz	92
1S03 or 5H	2400	232 x 252	50 or 25 MHz	110

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- Macrocells are routed automatically
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When you start a design with GateMark, you go from idea to PG tape in a matter of days.

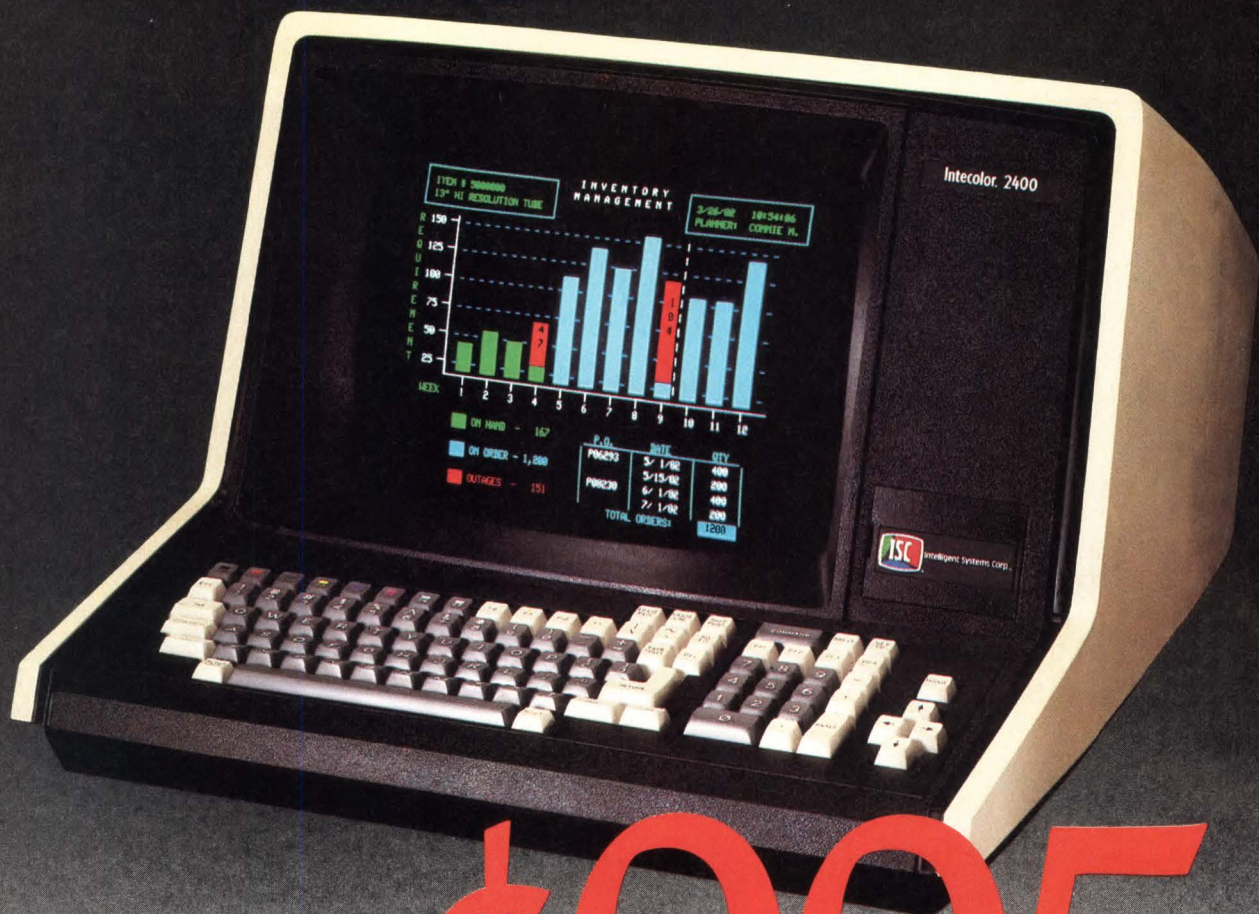
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MA 800	800	1.5 nsec	54
MA 1200	1,200	1.5 nsec	66



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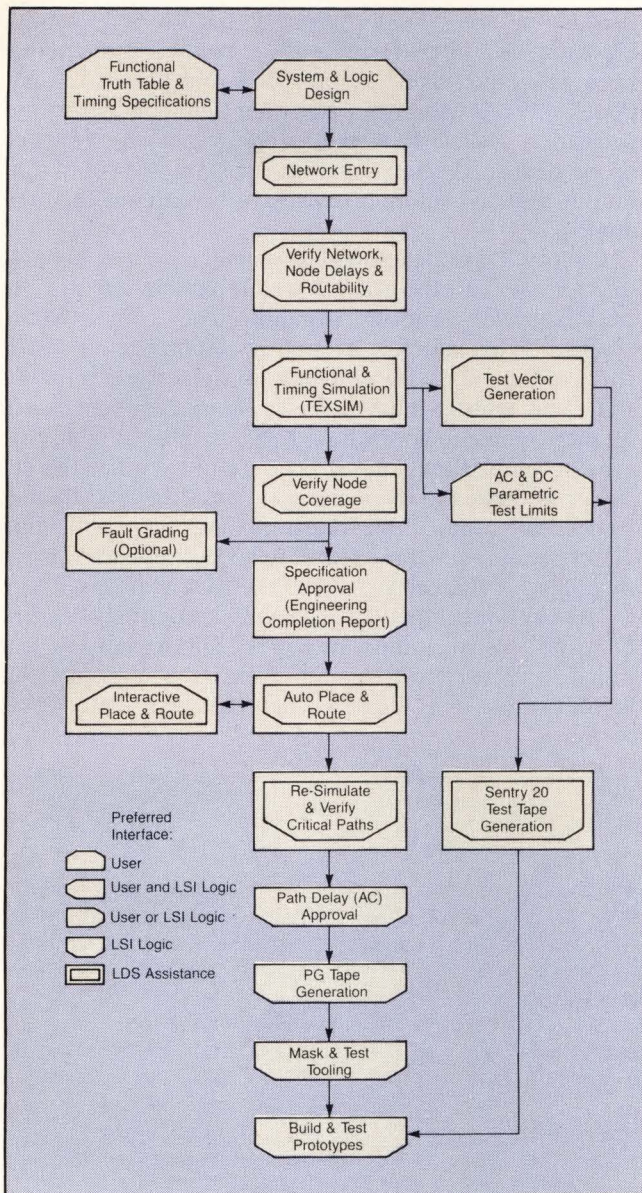
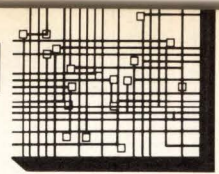


Figure 6: LSI Logic's LDS Design Automation System. The design verifier provides propagation delays through each network for both rising and falling inputs. Delays are used by the TEXSIM simulator. Interactive place and route is compared with design data to avoid layout violations. Following completion of layout, the actual metal (double layer) and metal/poly (single layer) lengths are recorded and the capacitance and resistance are calculated. These are then incorporated for use in recalculating the network delays and verifying the design.

Designing the array layout is the next step. Most vendors feel customers should not be bothered by layout and prefer that they bow out at this point. Layout means that macrocells are placed and routed. This can be done interactively on a CAD system or automatically. Automatic place and route is faster than the interactive method, and it guarantees an accurate translation of logic to silicon, but high silicon utilization is rarely attained. Low silicon utilization is costly: 60% utilization will double the size of a chip!

International Microcircuits Inc. uses an interactive placement system. As cells are placed, a net list is automatically generated, to ensure that an accurate translation is made. This placement net list is compared with the schematic net list to validate the layout.

Routing can be done automatically after the cells have been placed. Computers do a poor job at pattern recognition, which is required in cell placement, but they do a good job as routers. Most auto-routed arrays still require some interactive routing. Once the cells are placed and routed, the layout is re-simulated and performance is verified. If the circuit "runs" as designed, a pattern generation tape is created and tooling is produced for a prototype run. The prototypes are tested using the test vectors generated in the early stages of the design. If the prototypes check out, the production run of packaged arrays begins. Gate arrays can be housed in a variety of packages including: flat packages, leadless chip carriers (LCC), leaded chip carriers, and pin grid arrays.

Gate Array Trends

With so much activity on the gate array front, it has become nearly impossible to describe every array currently on the market. But some of the more recent announcements are indicative of technology trends. Some recent CMOS arrays include: LSI Logic's LL7000, with 2μ line widths, up to 10,000 gates, and propagation delays of 1.3ns; National Semiconductor's 3μ , 2400 gate SCX6324 with 2ns internal gate delays (a 2μ part with ins delays will be available this summer); Universal Semiconductor's ISO-36 and -56, 3μ and 5μ arrays with 1800 gates and 92 bonding pads, Signetic's 330 to 1700 gate LS/TTL compatible 3 and 4μ arrays, and AMI's 3μ GA series with up to 5000 gates and 2ns delays.

ECL arrays have also progressed. The Electron Division of NEC Electronics USA announced three arrays ranging from 300 to 3000 gates. Internal gate de-

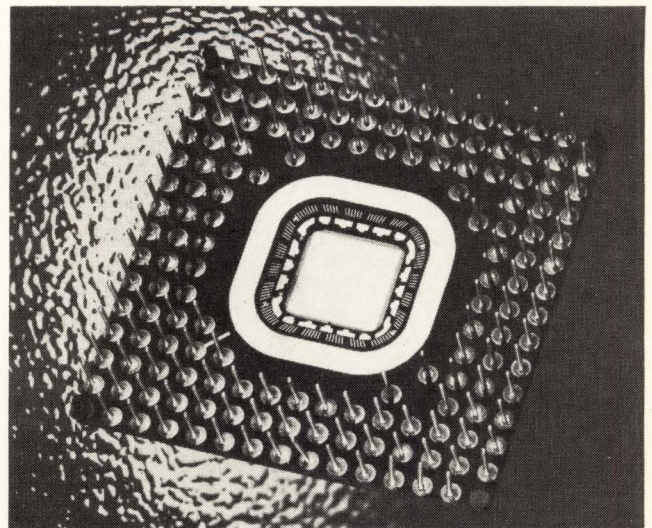


Figure 7: Motorola's MCA2800 ALS array is supplied in this 149 pin grid array. The TTL compatible array has 2800 gate equivalent and 130 cells. Propagation delay is 600ps.

lays are 0.5ns for the 300-gate array, and 0.7ns for the 1,100 and 2,000-gate arrays. By virtue of its agreement with Motorola, National Semiconductor announced 600 and 1200 MCA ECL arrays. Both devices feature a typical gate speed of 1ns. The MCA1200 includes 48 major internal macrocells while the MCA600 includes 24.

Integrated Schottky Logic (ISL) arrays are based on single-input NAND functions. The technology rivals I²L for density and STL for speed. Raytheon's Semiconductor Div. (Mountain View, CA) introduced a family of ISL arrays with gate counts from 800 to 2400. Typical propagation is 2.3 ns/gate.

Fujitsu Microelectronics will introduce a family of STTL arrays with 224 to 1120 gates in the second quarter of '83. Arrays with specialized functions are also available. Telmos and Interdesign both offer silicon CMOS arrays with A/D conversion on chip. Silicon Systems (Tustin, CA) recently announced a CMOS switched capacitor array to use in developing filters.

The array technology that will be offered to systems designers in the near future can be seen today at captive semiconductor manufacturers and at technical conferences. Control Data (St. Paul, MN) has developed 6000 gate silicon CMOS arrays with 2500 addi-

tional non-alterable peripheral gates for self testing. Designed for internal use only, the 2 or 3 μ circuits were developed using layout rules and processing parameters from Motorola, National Semiconductor and Fairchild. The self testing circuitry acts as a wafer probe device. Onchip function registers and input and output registers allow operands to be entered through input pins.

Control Data developed a variable macro technology for use with the array. Variable macros are flexible both vertically and horizontally. They can also be stacked. For example, assume an 8-bit register needs to be designed. With conventional macro technology, four 2-bit register macrocells would be used, each with its own duplicate controlling register. The variable macros developed by Control Data do not require the designer to duplicate the control circuitry. Instead the designer calls four 2-bit registers and the controlling circuitry as a separate "hat" that, because of vertical flexibility, is stacked on top of the four registers.

IBM has developed a four-level metal process for increased density in bipolar arrays. The fourth level of metal, combined with metalization advancements, resulted in a 75% density increase over three-level arrays.

Up Front Decisions

by Joe Conway
Marketing/Applications Manager
Applied Micro Circuits Corporation
San Diego, CA

Users can save themselves and vendors time and grief by making the right decisions up front in a gate array design. Some questions should be answered early. Can the circuit be partitioned into uniform slices? How big are those slices? Are both very high speed and lower speed logic required? What kind of I/O is needed? Is military qualification required? When are prototypes required? When are production parts needed? How many parts are needed?

Each gate array technology has advantages, based on performance and temperature range requirements. The smart user matches the array technology to the circuit requirements—not the other way around. The list of technologies includes: Metal Gate CMOS, Silicon Gate CMOS, I²L (Integrated Injection Logic) Bipolar, ISL (Integrated Schottky Logic) Bipolar, STL (Schottky Transistor Logic) Bipolar, ECL (Emitter Coupled Logic) low and high power.

Gate array suppliers are each seeking a niche. AMCC, for example, supports the low power ECL market

with the availability of TTL or ECL (or both) I/O in a device family up to 1500 gates with full MIL availability. This product offering supports only the customers who require high performance with TTL I/O, mixed TTL and ECL I/O or complete ECL I/O requirements with up to full MIL temperature range.

Array users should understand the circuit's performance requirements and narrow down the range of options prior to contacting suppliers. If an array user discusses a circuit requiring ECL performance with a CMOS or TTL array vendor or a CMOS or TTL performance circuit with ECL vendors, both the prospective array user and the logic array vendors are wasting time.

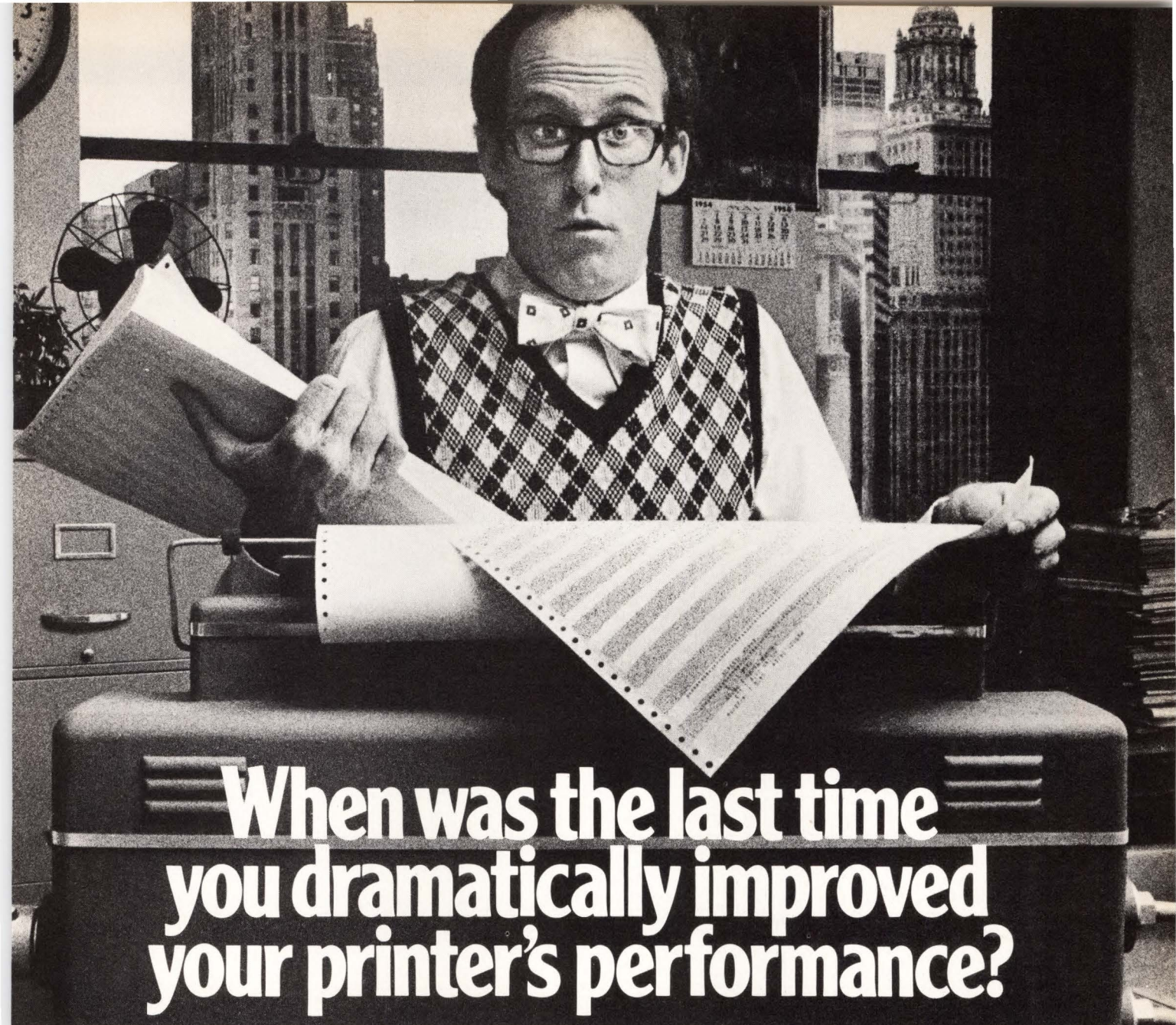
Since the array concept is new to most of the electronics industry, many users enter the hunt for an array ill-prepared for the detailed discussions that are required. Simply circling a piece of logic on a schematic of an existing design often is not enough. Usually a leftover collection circled on a logic print will end up being a poorly utilized array. For example, the circuit density versus the amount of I/O required or the mixture of required logic speeds often poorly matches the capability of the chosen

array. Instead the gate array user should have the circuit defined well enough to describe the array to the vendor in terms of these characteristics:

- The technology(s) needed.
- The approximate circuit size.
- The level of screening required (i.e., MIL temp. range, burn in).
- The critical performance paths.
- The type of I/O desired (i.e., MOS, TTL, ECL, Mixed).
- The number of I/Os needed.
- The packaging required.

Some vendors require the customer to do a large part of the work in defining the circuit in the vendor's logic or simulation conventions using expensive, dedicated equipment while others will work from customer drawings and provide the talent for circuit conversion and simulation. Users should know their needs and determine the vendor's capability at an early stage.

Also, consider whether the prospective vendor is a viable and reputable supplier. If the prospective vendor is simply a store front which offers designs implemented in another manufacturer's array, do they have the engineering and manufacturing expertise to solve problems should they arise?

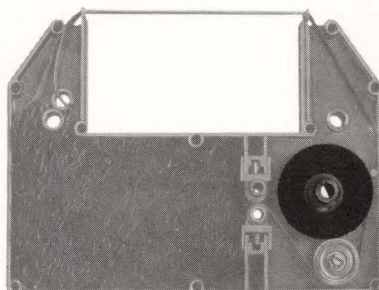


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Standard Cell Design: An Alternative to Gate Arrays

by Bill Loesch, Director of Marketing and Sales, ZyMOS Corp, Sunnyvale, CA

Gate arrays are pre-processed with fixed patterns of unit-size transistors, characteristics that inherently limit design flexibility and production economy. Consequently, as design complexity increases, die size, and therefore production cost, increase disproportionately because of the increasing percentage of unused silicon area. Moreover, present gate-array designs are restricted to systems not requiring on-chip complexities such as RAM, ROM and special I/O.

A standard-cell design does not use pre-defined mask layers. Instead, this method generates a customized set of masks defining the interconnects between completely characterized building blocks or cells. Each cell is a full-custom circuit handcrafted by the IC maker to minimize silicon area and optimize performance.

Advanced cell libraries comprise a rich variety of functions from which to choose. For example, ZyMOS Corp maintains several cell libraries in support of its ZyP automated design system: Zy4000 silicon-gate CMOS cell library, Zy2000 metal-gate CMOS cell library, and, available in June, an advanced 3 μ silicon gate CMOS cell library. Over 350 digital standard cells, ranging in complexity from simple gates to macro functions such as UARTs, DACs, A/D converters, ROM, RAM and core μ P's are available in the Zy40000 series library.

In addition, the Zy40000 Series analog standard cell library offers over 70 analog functions, including operational amplifiers, oscillators, switches and switch drivers, comparators and current references. These cells can be combined with digital cells on the same chip.

Thus, standard-cell design provides a higher degree of design flexibility than is possible with gate arrays, including the ultimate flexibility of allowing a designer to specify a new cell to meet performance requirements precisely. Standard-cell design time is somewhat longer than that for gate arrays, and so the direct cost of development is slightly higher. However, this cost differential is mini-

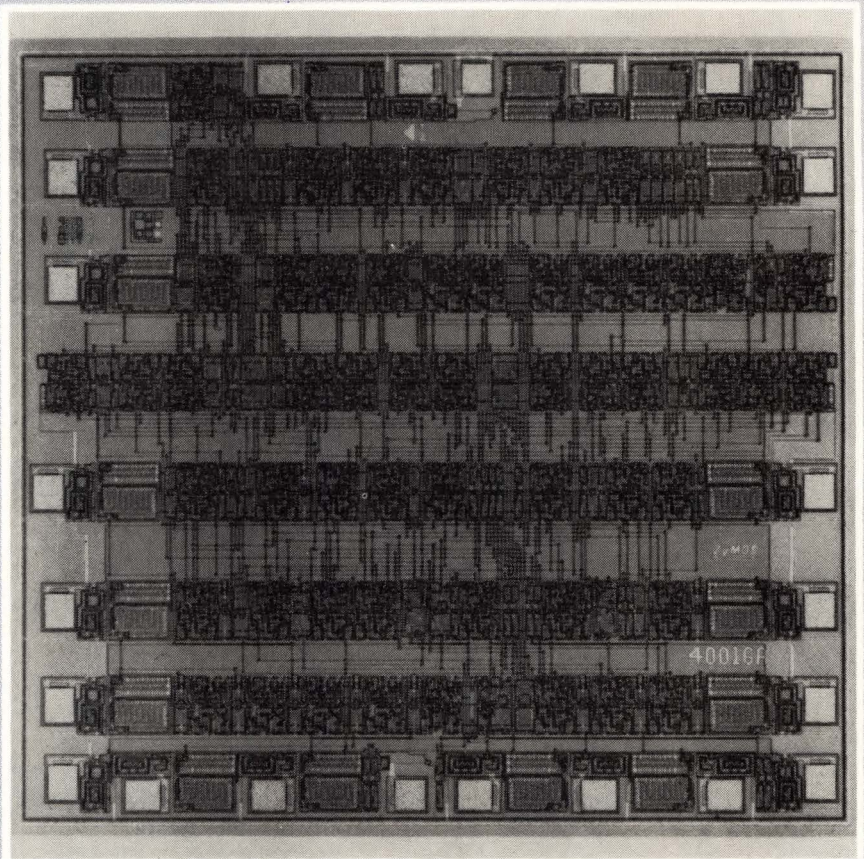


Figure 1: Custom chip designed with standard cell technology from ZyMOS. Developed by Cain Encoder Co., circuit is used in miniature electric-field sensor.

mized by the use of CAD techniques.

Standard-cell design is supported by CAD logic simulation, which predicts system timing and functionality without the need for breadboarding. Automatic place-and-route software ensures continuity between logic design and photomask tooling. CAD software also automatically generates a test program while prototype parts are being fabricated.

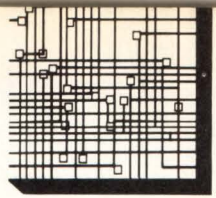
State-of-the-art CAD workstations such as the ZyPAWS (ZyP Automated Workstation) from ZyMOS have color graphics capability for performing all phases of the design cycle, including artwork generation. These workstations are supported by original and mature software packages tied to libraries of well-modeled standard cells. Such CAD tools minimize indi-

rect development cost since the user controls the development schedule, and computerized design virtually ensures working prototypes on the first attempt.

From the standpoint of production cost, standard-cell designs cost less than gate arrays. This is because gate arrays may require from 50% to 100% more silicon area for a given design. For very low complexity chips the cost difference is small since packaging and testing costs dominate production costs.

System designers can look forward to a proliferation of comprehensive standard cell libraries as well as the creation of new cells like the ZyCOMP-4 core μ P, to greatly improve system design in this decade.

Write 236



Several new arrays were described at the 1983 International Solid State Circuits Conference. A 1.5μ CMOS gate array with 4,268 gates and a 2,304-bit configurable memory was developed by NEC (Kanagawa, Japan). The memory can be configured with regard to word depth and bit width by changing the metalization pattern. Hitachi (Tokyo, Japan) also presented a CMOS array with variable memory. Called "CMOS Building Block VLSIs," the circuits use 2μ technology and two metal and one poly-silicon layer for interconnections. RAM and ROM is composed of several basic cells. Memory size can be varied simply by changing the number and combination of basic cells. A third CMOS array was described by Toshiba's R & D Center (Kawasaki, Japan). Their device is a 20K-gate CMOS gate array, implemented with 2μ design rules. A three-level metalization technology is used. A $32b \times 32b$ parallel multiplier designed on the gate array offers a multiplying speed of 150ns with a 300mW power dissipation at a 5MHz clock rate. The typical gate delay is 1.5ns for a fanout of 3 and a 3mm interconnect length.

In addition, a 5,000 gate ECL-compatible bipolar array was presented by Nippon Tel & Tel (Tokyo, Japan). With a power dissipation of less than 6W/chip, it has a .5ns loaded gate delay.



Figure 9: Daisy Systems' Gatemaster work station dedicated to gate array design. Station is used for schematic capture, simulation, layout and verification.

Work Stations Bring Array Design Home

Engineering work stations (EWS) dedicated to gate array design are an inevitable addition to semi-custom design. Two EWS are especially useful during the early stages of a design. The first is Daisy Systems' (Sunnyvale, CA) Gatemaster gate array development system. Gatemaster provides engineers with a set of tools for Logic Design (including the conversion of traditional logic to gate array logic), Interactive Logic Simulation, Timing Verification, Test Vector Generation, Placement and Routing and output to manufacturer's formats. By automating each design step and by tying all of the steps together through a single data base, Gatemaster reduces gate array design to a graphics-aided software process. Gatemaster is based on the company's Logician engineering work station and has a 19", high-resolution color monitor. The Multibus architecture supports 8 different processors, 1.5M of dynamic RAM, a 40M Winchester hard disk for data storage, a 1M floppy disk, and interface electronics for mainframe communications. Options include magnetic tape, bit pad tablet, electrostatic plotter, and high speed networking.

The designer creates logic and schematic drawings at the station. The work station provides programs to aid in conversion from TTL to gate array logic, syntax checking of the schematic, and local simulation routines to verify the boolean functionality of the design as well as its timing delays. It is especially useful during this upfront state. Once the logic design is created and verified locally, the option exists to translate the data base into any number of different input formats for direct interface to mainframe-based design automation programs.

The physical layout of the array is created interac-

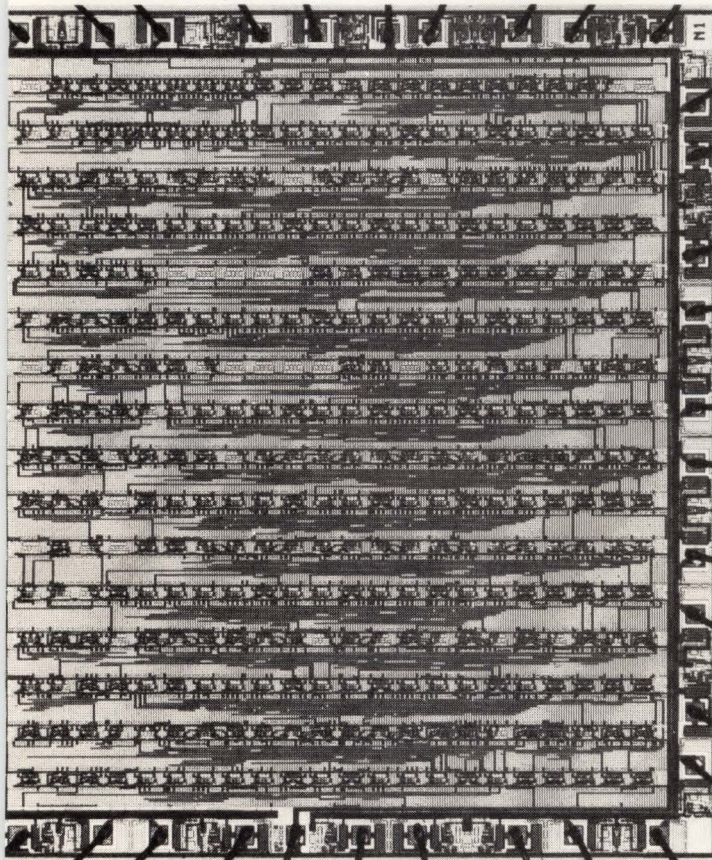
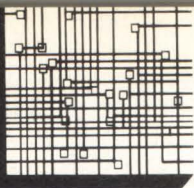


Figure 8: SCC CMOS array. Signetics' single level metal arrays are among first with auto route and place support. 98% utilization was attained with auto connection.



Gate Arrays

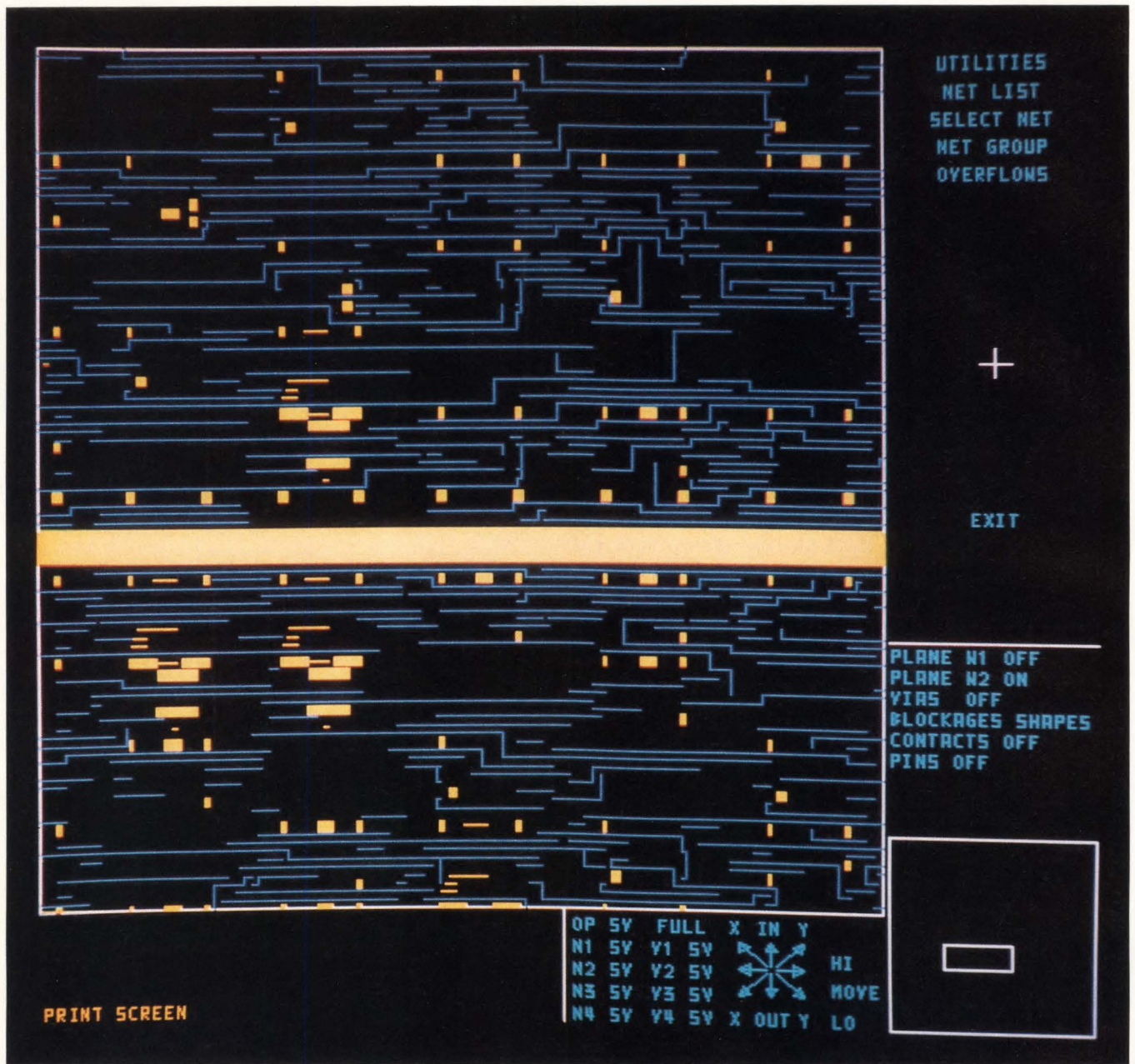


Figure 10: Layout display on Mentor Graphics work station with gate array software from California Automated Design, Inc. CADIPACE and CADIRoute automatically place and route. CADIGRAPH is interactive and is used to complete connections and modify routes.

tively. The system will not allow mistakes to be entered once the electrical net list description of the circuit has been defined. This list, generated by the Logician schematic database, contains all component and signal names as well as other parametric information. It is compared in real time with layout entries, and the system will not allow any electrical errors. This feature eliminates the need for external electrical and design rule verification programs.

The Gatemaster can be used to design arrays from several companies. Daisy has acquired the rights to macro cell libraries and processing parameters from National Semiconductor, Motorola, Fairchild, Mitel,

AMCC and Semi Processes.

Mentor Graphics Corp (Portland, OR) announced a package of automatic gate array software for its Idea 1000 Apollo-based engineering work station. The software streamlines gate array logic design and layout. Like Gatemaster it automatically satisfies electrical constraints so that final mask data meets design rules, electrical checks, and logical connectivity.

The software has been made available exclusively for Mentor engineering work stations through a marketing agreement between Mentor Graphics and California Automated Design, Inc. (Santa Clara, CA). Mentor/CADISYS consists of automatic placement

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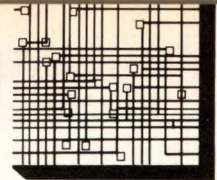
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(CADIPLACE), automatic routing (CADIROUTE), and interactive graphics (CADIGRAPH). Before placement occurs, the input design data is captured and verified. The data design is then supplied from the Mentor data base to the placement and routing programs. Using hierarchical methods, CADIPLACE automatically places function blocks consisting of gates, macros, or clusters.

In contrast to most current CAE/CAD tools, CADIPLACE does not require fixed block sizes or shapes. The placement software accounts for internal partitioning, critical nets, wire length, pre-assigned elements, and anticipated interconnect paths. CADIROUTE automatically routes the circuit connections, after determining a grid and connection list from technology and design files.

CADIGRAPH can be used to complete residual connections, to modify routes to pre-wire critical nets, or to complete the total wiring interactively. Designed

to handle a wide variety of technologies, CADISYS also operates on IBM, DEC VAX, Data General, and Prime mainframes. Programs are written in Pascal or Fortran to ensure portability. These programs are used by many gate array vendors.

Conclusion

For the gate array boom to continue, gate array technology must continue to improve. To compete with standard cells, gate arrays will have to be designed with expanded capabilities, such as on-chip memory, now seen only in the laboratory. Customers are going to have to assume a greater role in the design process, relieving vendors of much of the hand-holding they now do. For customers to do more design, they will need friendly CAD systems with standardized software. Indications are that these events are starting to take place. If so, the semicustom approach and those involved in it have a rosy future. □

COMPANIES IN THE GATE ARRAY INDUSTRY

The following list of suppliers, although not exhaustive, does include most companies selling gate arrays in the U.S. Use the accompanying write numbers and the *Digital Design* inquiry card to obtain further information.

Advanced Micro Devices (AMD)
Sunnyvale, CA
Write 214

American Microsystems, Inc. (AMI)
Santa Clara, CA
Write 215

Analog Innovations, Inc.
Los Gatos, CA
Write 216

Applied Micro Circuits Corporation (AMCC)
San Diego, CA
Write 217

Array Devices, Inc.
San Diego, CA
Write 218

Array Technology, Inc.
Sunnyvale Road
San Jose, CA
Write 219

California Devices, Inc.
San Jose, CA
Write 220

Cherry Semiconductor
E. Greenwich, RI
Write 221

Custom Integrated Circuits
Minneapolis, MN
Write 222

Custom MOS Arrays, Inc.
Milpitas, CA
Write 223

Datel-Intersil
Mansfield, MA
Write 224

EXAR Integrated Circuits
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Fairchild Semiconductor
Mountain View, CA
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Ferranti Electric
Commack, NY
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Fujitsu MicroElectronics
Santa Clara, CA
Write 228

General Instruments Corporation
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For the decision maker:
A new report analyzing
gate array technology
and markets.

Gate Arrays: Implementing LSI Technology

A REPORT BY

SOURCE III, INC.

HIGHLIGHTS OF THE REPORT

Gate array technology represents a viable approach for "Systems on Silicon" implementation. The 1980's will see the worldwide gate array marketplace pass the \$1 billion mark. There are many issues which the decision maker involved in considering LSI implementation must face.

In a systematic approach, the report provides both a **strategic and tactical planning** tool for assessing future trends and reaching immediate decisions involving semicustom LSI implementation. The report contains **over 100 supporting charts and figures** along with **fact-filled analysis and data**. In addition, more than 50 gate array companies are listed with a comprehensive profile.

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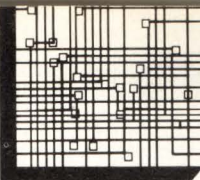
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Gate Arrays



COMPANIES IN THE GATE ARRAY INDUSTRY

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Intersil, Inc.
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Black and white facts about color graphics.

Fact 1.

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Fact 2.

Software redevelopment is even more expensive.

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Fact 3.

Performance is a lot more than good specs.

Graphics performance goes beyond pixel and vector timing specs. It is the ability to display a complex picture without having to wait. Provide instantaneous interaction between an application program and its user. And efficiently communicate with a host computer. The kind of total graphics performance you should measure before you buy.

Fact 4.

Graphics applications demand flexibility.

The Model One family from Raster Technologies offers maximum flexibility at the lowest cost. Because it lets the user select the combinations of display resolution, color and refresh rates that are right for that particular application. Factors that are different for every application.

Fact 5.

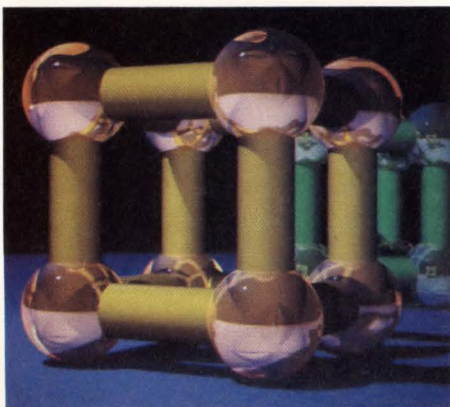
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Fact 6.

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The Model One/25 features vivid full color imaging performance with 512 x 512 resolution. The Model One/40 features ultra high 1024 x 1024 resolution. The Model One/60 features 100% flicker-free 60 Hz non-interlaced display with 768 x 576 resolution. All support our Advanced Graphics Application Development Firmware and powerful display list package. Put the Model One family to the test.



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CalComp's \$1 vs. their \$16,0

Why settle for a plodding plotter when you can double your throughput with an all-new Model 945 or Model 965 beltbed plotter from CalComp for approximately the same price?

Productivity gains can range from 25% to more than 500%. It's like having up to two plotters for the price of one.

CalComp Model 945 beltbed plotter (left) for sheets up to ANSI size D (or ISO size A1), and Model 965 plotter for drawings up to sheet size E (or size A0).



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CalComp's Model 945 and Model 965 plotters, by comparison, allow you to map up to 16 logical pens to four physical pens continuously poised over the plot surface—ready to be activated



6,000 plotter 00 plodder.



in a fraction of a second. If more than four pens are needed, the plotter performs an automatic stop and prompts the operator to change pens.

Plus the user-friendly control panel provides local control and plot manipulation with easily understood English language messages.

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Floppy Emulation, Data Recording For Harsh Environments

by Gavin McClintock

Today's bubble memory is non-volatile and reliable storage for use in a variety of "difficult" environments. While many portable electronic equipment manufacturers are incorporating this technology into some of their component and board level products, one Canadian company, Targa, has built a family of ruggedized data recording systems employing Intel's 1 Mbit bubble device in a removable cartridge format.

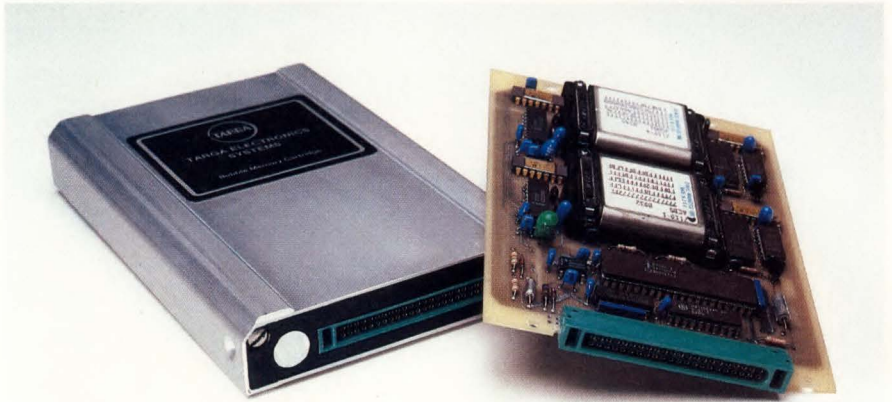


Figure 1: The Targa removable cartridge uses Intel bubble devices.

Using Intel's newest bubble devices, these floppy disk emulators and data recorders provide highly reliable mass memory under extreme conditions.

Targa offers three products: a data recorder; floppy disk emulators (fixed or removable); and OEM Cartridge Holder Interfaces. The removable cartridge used for all three systems is about the size of an 8-track stereo cassette, and contains one or two Intel devices (2 Mbits) and interface electronics.

The DR3101 data recorder connects to a host system through either its RS232C or IEEE 488 port.

Gavin McClintock is President of Targa Electronics Systems, Inc., P.O. Box 8485, 3101 B Hawthorne Rd., Ottawa, Canada K1G 3H9.

In the RS232C mode, the unit acts as a "tape recorder" with fast data access speed (48 msec average) and can receive or transmit data at up to 38,400 bits/sec. In the IEEE 488 operation, the unit emulates a disk drive. The data recorder's software allows communication to it as to an HP82902 or DEC TU-58.

The bubble memory floppy disk emulators are package, protocol and electrically plug-compatible with most 5-1/4" and 8" floppy disk units. By replacing the mechanical drive with this floppy drive, the unit operates transparently to the host system. A fixed media version is also available.

The Cartridge Holder Interface (CH2100), is a hardware component consisting of a metal holder with cartridge release mechanism and associated PCB to support the connector and host system interface. Used in place of a built-in disk drive or tape unit, the CH2100 provides a serial or parallel port to the internal μ controller board.

Reliable Media

These bubble memory devices evolved in an effort to build a more

rugged and reliable data recording system for use on small boats for the Canadian government. After an investigation of all storage media applicable for harsh environment usage, bubble memories proved to be the most error-free and reliable data storage media available. The 1 Mbit Intel Magnetics 7110 bubble device used at 70°C has the following failure rates per Mbit compared to alternatives:

— 7110 Bubble Memory	0.8% per 1 kHour
— Dynamic RAM	1.1% per 1 kHour
— EPROM	4.0% per 1 kHour

The Intel device has an MTBF of 30 years of continuous operation at maximum temperature ranges. This compares favorably to all rotating media (disks and tapes), which require routine maintenance and usually need servicing about every 6 months. It is also virtually error-free, with an estimated error rate of 1 to 10^{-16} .

Operating temperatures range from 0°C to 55°C, with non-volatile

	Targa Bubble Memory Systems	Tape Recorders	Floppy Disks	Ruggedized Tape or Disk	CMOS EPROM
Storage Media	Solid State	Magnetic Plastic Tape	Magnetic Plastic Disk	Magnetic Plastic	Solid State
Access	Fast	Slow	Medium	Medium	Very Fast
On-Going Maintenance	Virtually Non- Existent	About every 6 months	About every 6 months	About every 6 months	Little Maintenance Required
Ruggedness	High Level	Low Level	Low Level	Medium- High Level	Medium Level
Mechanical Failure Prone	No	Yes	Yes	Yes	No
Reliability-Failure* rates per megabit at 70°C (per 1khour)	0.8%	>4.0	>4.0	—Unknown	Dynamic RAM 1.1% EPROM 4.0%
Initial System Cost	High	Low	Low	High	High
Integrated Package Cost of Ownership	Med	High	High	High	High
Harsh Environment Suitability	High	Low	Low	Med-High	Med-High
Non-Volatility	Yes	Yes	Yes	Yes	Limited by Battery
Removable Media	Yes	Yes	Yes	Yes	No
Power	Low	Med-High	Med-High	High	Low
Security of Data on Media	System Needed	— Universally Reproducible —			Media not Removable
Electrical Susceptibility	Low	Med-High	Med-High	Med	Med-High

*Data supplied from Intel Magnetics.

Table 1: Characteristics of bubble memory compared with other data storage media.

storage from -40°C to $+100^{\circ}\text{C}$. The media can also withstand operating vibrations of 20G and non-operating shock of 200G.

Thus, compared to alternative solid state memories, bubbles have lower failure rate per Mbit and are infinitely non-volatile. Bubbles have equivalent or better error rates compared to other magnetic media, and are highly durable and reliable in harsh environments while offering few maintenance problems, hence low cost of ownership.

Intel's Bubble

About the size of a matchbook, Intel's 7110 bubble memory device is a magnetic, non-volatile, solid state device capable of operating under a variety of environments. This component consists of a garnet substrate surrounded by two layers of copper coils overlapped at right angles to each other, all sandwiched between two magnets and surrounded by a metal shield. Patterns are deposited on the substrate material similar to those in semicon-

ductor memory chips; the user controls the creation, destruction and location of bubbles within the device. The existence or non-existence of bubbles equate to the "ones and zeros" of the binary form of data encoding.

As data is "recorded" onto the substrate by the "write" lead, it shifts along the chevrons towards preferred regions of magnetism on "strings." The "read" conductor can retrieve the data as the string rotates within the memory devices and "duplicate" that data for trans-

mission to the requesting host equipment for processing or display. Each device contains 1,048,576 bits of usable data storage in a binary organization consisting of 512 bits per page over the 2048 pages. The device operates in serial-parallel-serial mode, with each of its 256 data loops containing up to 4096 bits per loop. Separate read and write tracks are implemented.

Design Considerations

The original data recorder was a heavier, more power-consuming piece of marine equipment with the bubble memory built-in. The prototype worked fine, but the client wanted a new design, to be smaller, lighter in weight and 19" rack mountable, with reduced power consumption and media removability. The reworking also included a standard interchangeable cartridge (2 capacities, 2 operating temperature ranges), more software, a visual LCD for operational data, and choice of virtually any power supply. The new version, DR3101, was successfully field tested in the late summer of 1982 and production commenced in November 1982.

Designing the bubble into a cartridge had definite advantages for harsh/mobile environments. Standard plug-in boards with edge connectors cannot stand up to the same physical abuse as can the cartridge's rugged connector and metal casing. The connector alone is warranted by the manufacturer for 20,000 insertion/removal cycles. Also, fixed PCBs are, by definition, less portable. It's easier to bring a cartridge back for processing than a heavy piece of field gear.

Another design criterion was to provide for future technological changes at the lowest possible cost and inconvenience to the customer. As things change, only what is *inside* the cartridge changes, *not* the interface hardware customers have already purchased. For example, once new 4 Mbit devices are available later this year, a 256 kByte cartridge user can return a cartridge to Targa for upgrade to a 1 Mbyte device. All interfacing and



Figure 2: The data recorder, floppy emulator, and cartridge holder all use the same removable cartridge.

system software remain the same. This also holds true for future advances in solid-state memory technologies.

The designers also realized that not everyone working in these rough applications needs a fully-equipped peripheral device. Thus a family of less expensive systems which could utilize the same cartridges was designed, namely the floppy disk emulators and cartridge holder interfaces.

Harsh Environments

These products are geared to the high reliability demands of users operating in mobile and harsh environments. Applications include airborne, truck and ship recording and program load functions, as well as replacements for less reliable media for use in factories, chemical and laboratory situations.

The original proponents of the DR3101, the Canadian Federal Government's Canada Centre for Inland Waters (CCIW) use the device for hydrographic recording on the Great Lakes. The CCIW uses the system on board small 26 foot launches travelling at high speeds

to record lake bottom profiling and other data. Recently, other systems have been sold to private sector clients for similar marine applications and to customers who record data from a magnetometer in an airborne situation.

Although the system has yet to be MIL tested, the military has expressed a great deal of interest for a variety of applications. One μ C manufacturer has incorporated the OEM Cartridge Holder Interface into its military μ C. The aerospace community is interested in the system as an on-board systems monitoring recorder for preventive maintenance applications. Program load and quality assurances uses have also been suggested.

Other Applications

Other harsh environment applications include factory Q.A., data acquisition and control, environmental monitoring, geophysical and seismic recording, robotics, and navigational buoys. Future developments will probably include increased memory capacity, broader operating specs, and user-oriented adaptation of new technology. □

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LSI Circuit Design Gives Modems More Capabilities



Photo courtesy Racal-Milgo

by Racal-Milgo Staff

The field of data communications has expanded tremendously as a result of advancements in LSI circuit design and its partnership with μ P development. One of the product areas most affected is modem development. New offerings show an ever-increasing variety of modem products ranging from integral to stand-alone devices. Common to each of these products are enhanced features and options, making them suitable for many specialized applications.

A total network environment, where each component supports and complements the other—the modem meeting the needs of all network components—is the objective of the 'system approach' to modem design. Other primary design considerations include ease of operation and maintenance, product life, and cost.

The first modem in the Omni-mode series served as a model for the design and development of the firmware-based line. This 4800 bit/sec. modem operates over 3002 type of M1040 (international) lines without special line conditioning and supports switched/constant car-

rier and dedicated/dial backup operations. It can be configured for compatibility with earlier 4800 bit/sec. Racal-Milgo modems, such as the MPS 48 (CCITT V.27) or MPS 4827 (CCITT V.27 bis). Additional proprietary training sequences and lengths can be selected for specialized applications.

*LSI circuit design,
modular
construction and
firmware-controlled
functions simplify
upgrading and
integration of
options.*

Two major options are available: intelligent multiport (two or four port versions), and remote modem control (RMC) options. LSI circuit design, modular construction and firmware-controlled functions simplify upgrading and integration of options while supporting reduced maintenance, improved reliability

and easier fault diagnosis. Each major function and its associated features is built on a single PC board. These functions—the main modem, intelligent multiport option and remote modem control option—are interconnected by a high speed common data bus managed by the option control processor. The block diagram in **Figure 1** represents the signal management and option integration of the design.

Each block in **Figure 1** signifies a modem function and its activity in the overall functional operation. The analog circuits and converters control the analog/digital and digital/analog conversions in conjunction with the transmit and receive line levels and receive sensitivity and filtering. The LSI circuit design used for the signal processor element can simultaneously perform two real-time functions, i.e. the complete modulation/demodulation processes for both transmit and receive. The control processor and option control processor also belong to the main modem function.

The control processor provides the signal processor with sequencing information for training elements in response to the interface signals. All communication between the main modem, multiport option, RMC option and modem front panel is managed by the op-

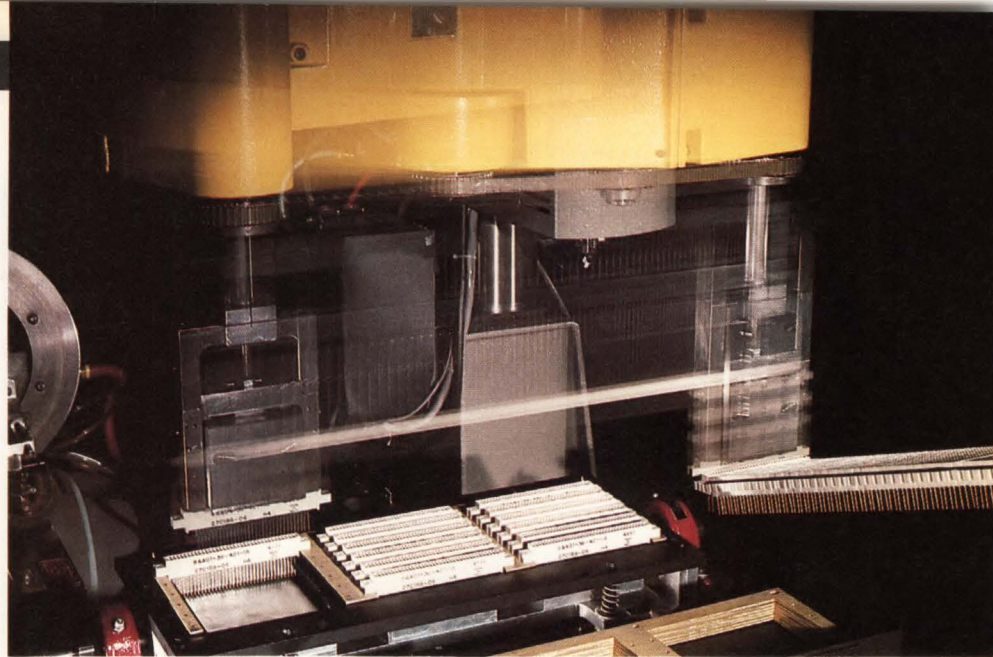
Racal-Milgo, 8600 N.W. 41st Street, Miami, FL 33166.

tion control processor (OCP). The OCP governs all modem operating parameters, such as data rate, soft-strap (software strapping) program and option configurations.

The OCP integrates the functions of the multiport and RMC options with the main modem functions via the common data bus managed by the OCP. The multiport option, fully contained on its own PC board, provides time-division multiplexing for two or four port rate combination (depending on option selection) totalling the aggregate channel rate. The RMC board contains the test and control processor which generates and interprets all commands to and from the network controller or a controlling front panel, depending on how the RMC option is selected to function. The RMC option also provides direct access to the analog circuits and converters for secondary channel operations.

The combination of firmware-based functions form the framework for the design of the modem. Data rate selection monitoring, testing and soft-strapping to select modem operating are all activated from the front panel. An eight-digit display screen acts as the interface between the operator and the modem, providing all information in an easy to interpret manner.

The soft-strapping feature eliminates traditional hardware strapping and its restrictions, allowing the operator to reconfigure the mo-



The backplane assembly of a Racal-Milgo modem.

dem operating parameters from the front panel for special network requirements. For many end users this eliminates the field service calls generally required to make adjustments of modem operating parameters.

The first step in designing the product for future flexibility was selecting the ICs to comprise the signal processing element. A custom chip set was chosen, since a bipolar bit slice approach would have been too power-consumptive and area-intensive. This led to the development of the custom signal processor with a primary constraint of providing external memory and re-write memory. With these provisions met, the same custom chip set can be used for a wide variety of products and a large selection of

modulators/demodulators within a single architecture, as well as providing reliability and improved thermal performance.

The logic of the custom signal processor is partitioned into a memory control unit (MCU), arithmetic logic unit (ALU) and interface analog/digital chip (IAD). The ALU and MCU are organized into a two-bus architecture with an address bus and data bus. Both instructions and data are formatted into 16-bit words. Instructions are further organized into operand/operation fields, so that for each operation there is a fetch rule for locating the associated operand.

Figure 2 represents the signal processing flow as implemented with the custom chip set. The IAD (Interface Analog and Digital) chip provides the interface between the transmitter digital/analog circuits, the receiver digital/analog circuits, the MCU (memory control unit) and a standard μP . It also generates the transmitter and receiver bit rate and baud rate clocks. Its primary responsibilities are determining the location of the next instruction and data word and providing the control for intermixing and pipelining the data fetches and instruction fetches. The IAD also interfaces with the control processor via the μP memory of the IAD chip. The data is then shifted to the MCU via the serial output port.

The MCU provides buffering on the serial port from the IAD. It also generates the memory location (address) of the next command to

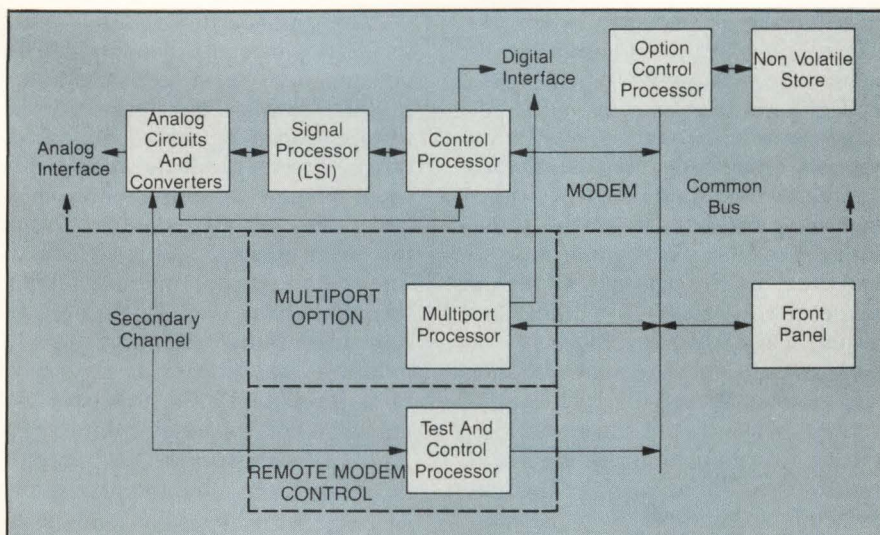


Figure 1: Overview of signal paths and function management in Omnimode.

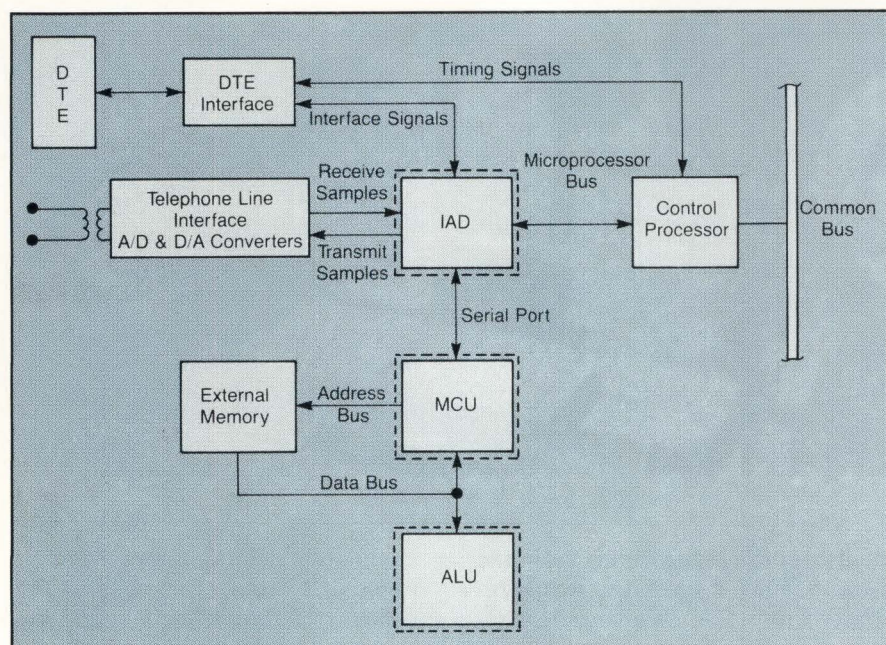


Figure 2: Simplified block diagram of Signal Processing Flow by Omnimode Custom Chip Set.

be executed or the next data which can be used by the MCU and ALU chips. The timing control signals for the ALU chip are also generated via the MCU. Decisions such as jumps and go to subroutines as well as performance of loops are accomplished by the MCU. The loop controller, located in the MCU, allows inner loops of routines to be performed without software overhead.

The third chip of the custom set is the ALU, which performs all arithmetic and logic functions on the data. It is organized with dual accumulators, which facilitates complex arithmetic operations. The ALU also provides input stacks on both the instructions and the data; this allows the elasticity for both to be efficiently pipelined.

An Option Control Processor provides the pivot for the system design architecture. All options interact via the common data bus through the OCP. The design is based on a master/slave approach. This approach was particularly viable since an OCP was already required for management of the front panel and non-volatile memory.

Each major option as managed by the option control processor includes a group of specialized features to support its operation.

The multiport option, available in two port or four port configurations, includes the Control Signal Simulation feature and Dynamode. The CSS feature has two aspects: Request to Send—Data Carrier Detect Signal Simulation, and Switched Network Remoting adapter. RTS-DCD simulation imitates controlled line carrier when required by the DTE. The switched Network Remoting Adapter allows a remote modem to be switched into the public network. Dynamode provides automatic internal adjustment of active ports and their assigned rates by the Omnimode to achieve maximum data throughput.

The RMC option is a major advancement in the control offered by modem products. It establishes complete front panel control from a central point over remote Omnimode modems. This option may be exercised in two ways: without an external controller (from the front panel of a controlling modem), or with an external network controller such as the Racal-Milgo CMS controller. With the inclusion of this option, all monitoring, testing and selection of modem operating parameters for remote units is managed from a central control point.

From the product's earliest stages,

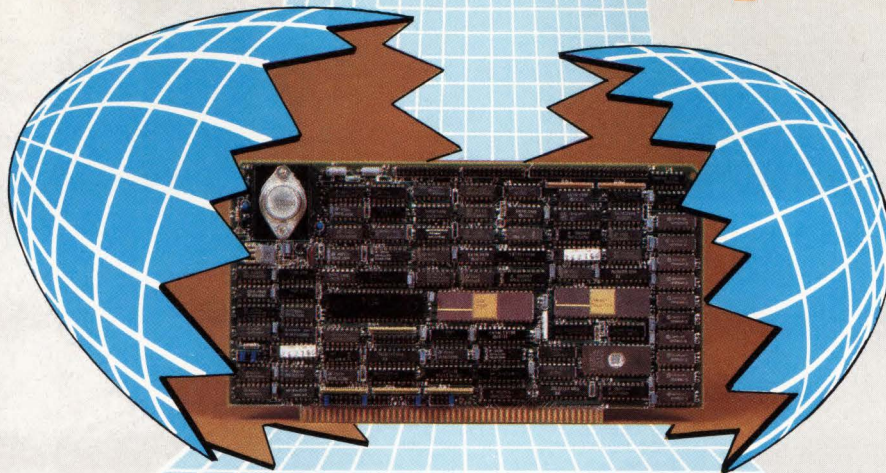
manufacturing took an active part in its development while design engineering kept in mind the production cost. One of the first design features that reduced manufacturing costs was the use of a standard size case for the entire series as well as for other products. The standard size circuit boards used in the series also eliminate much of the retooling generally involved in the manufacturing process. The PC boards of the Omnimode design were 98% auto-inserted, which reduced manufacturing time more than 300%. Three different pieces of manufacturing equipment, a Dual-In-Line Package (DIP) Inserter, a Variable Center Distance (VCD) Axial Lead Inserter and a Pin Machine were used to perform the auto-insertion. This computer-controlled equipment inserts integrated circuits, diodes, capacitors, resistors, and pins.

With the modular design of the product, the reduction of interconnects required between the option boards was a consideration of vital importance. A decision for ribbon interconnect resulted in significant cost savings by eliminating much of the chassis hardware.

The touch-pad assembly of the front panel offers multiple manufacturing advantages. There was a significant reduction in manufacturing labor costs, since there was little of the standard mechanical assembly usually required for indicators and switches.

Both engineering and manufacturing departments also worked to develop a system of automated product testing. Not only do the testing procedures reduce manufacturing costs (reducing man-hours spent testing by more than one-half), they also streamline testing for field service representatives. The aim of continuous testing throughout the manufacturing process, from initial incoming chips to final test, was to provide a product of high reliability. With the increasing demands on today's data communications networks, the need for flexibility and reliability can only be met with continued advancements in LSI design and efficient implementation of those designs. □

Incubation Complete



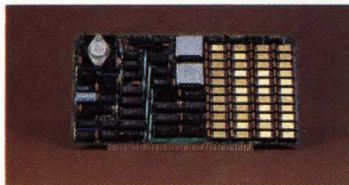
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Supercomputers for the Eighties



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by Edward W. Kozdrowicki

In 1974, a study on the first generation of supercomputers had two models and a total of eleven installations to consider. These first large-scale computers to concentrate on efficient pipeline array processing and take advantage of the parallelism available when processing vectors, or numerical arrays, in scientific work were Control Data Corporation's Star-100 (String Array processor) and Texas Instruments' ASC (Advanced Scientific Computer). Four Star-100s and seven ASC systems had been installed before the first generation of supercomputers gave way to the second.

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Supercomputers of today are still basically uniprocessors; in the 1990s, they may involve as many as 16,000 processors operating in parallel on a problem.

The Cray Computer

The second generation of vector supercomputers began in 1975 when Cray Research, Inc. announced the Cray-1. It was widely billed as the world's biggest computer, but there was initial skepticism. Little software was available at first and it required a large mainframe such as a Univac 1108 or IBM 3033 as a front-end computer.

In 1977, Auerbach Publishers suggested that the Cray computer would be limited initially to a small circle of scientific users in nuclear research, seismic analysis and weather modeling. Now, models for

aerodynamics, computer-assisted tomography, human organ modeling, fusion power and such exotic ideas as artificial intelligence experimentation have been prepared for execution on supercomputers.

Since the first installation in 1976, the Cray-1 has demonstrated reliability, high-speed secondary storage and interfacing to many front-end computers; extensive software support has also become available. As of September 1980, there were 20 Cray-1 machines at user facilities, and there are now over 50 installations. The original Cray-1 has been updated to the

Cray-1S and to the Cray X-MP/22, a dual CPU system announced in April, 1982.

The most obvious architectural improvement of second-generation supercomputers over first is the inclusion of a scalar processor for nonvector operations. These second generation machines do well for scalar operation benchmarks. In fact, the Cray-1 was the world's fastest scalar computer throughout the 1970s, with a basic cycle time of 12.5 ns. This is a distinction it will hold for some time before newer versions of supercomputers become established in the 1980s. The Cray-1's closest competitor for the 1970s was the CDC 7600 or the Cyber 176, with a 27.5 ns cycle time.

The Cray-1 was a new architecture developed by Seymour Cray when he started his own company. Since Cray was the principal architect of the CDC 6600 and CDC 7600, the Cray-1 has evolutionary similarities to those designs. Cray-1 extends the pipeline concepts of those CDC architectures and adds vector processing. **Figure 1** is a block diagram of the Cray-1S. The fully integrated, segmented functional units needed for scalar and vector processing at the 12.5 ns clock rate are accomplished with 225 operation codes. These codes are either 16-bit or 32-bit instructions.

The CPU has 13 functional units which can chain operation codes. By chaining, the results are available for another unit in the next clock period. A large number of internal CPU registers store the intermediate results of the units as they operate in parallel.

The Cray-1 can be used stand-alone, but use of a front-end IBM 370, CDC Cyber or Univac 1100 is recommended. A channel adaptor is required between the front-end computer channel and the Cray main memory. The main memory is 4K ECL Fairchild or Motorola chips and can hold up to 4M 64-bit words.

The I/O subsystem is two, three or four Cray-designed 16-bit mini-computer processor stations. These processors have a 50 ns cycle time (bipolar memory) and up to 64K 16-bit word capacity. There is a

Complex color graphics are a chief application for supercomputers (photo courtesy Air Force Weapons Lab, Kirtland AFB, New Mexico, 87117).

large buffer memory between the I/O subsystem and the main memory ports of the Cray-1; each port has up to 850 Mbits/sec. bandwidth.

The device control unit uses one of 12 bidirectional standard 50 Mbits/sec. channels for CDC 819 disk memory. Using eight controllers, a large Cray-1 system can handle up to 32 double-density, 600 Mbyte capacity 819 on-line disks.

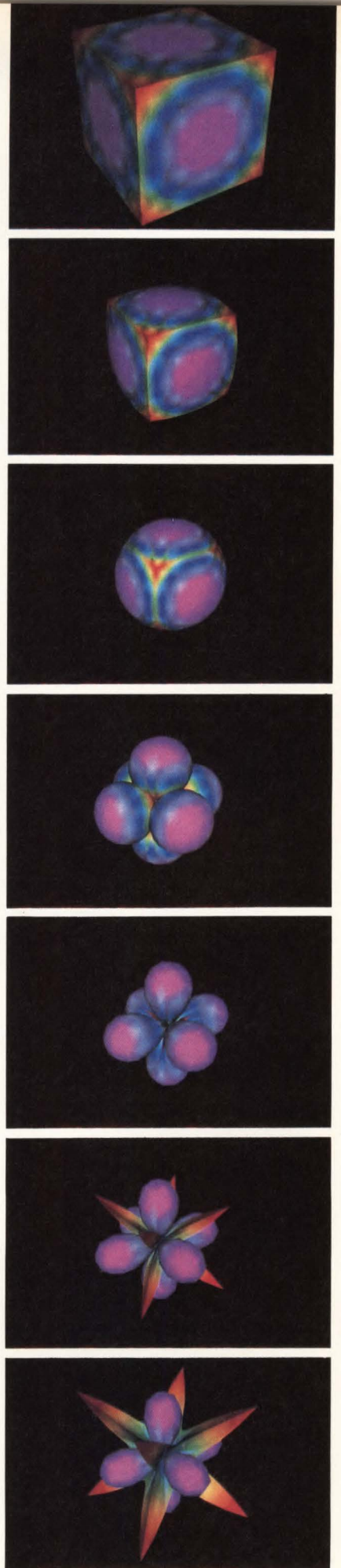
The Cyber 205

A fierce competitor to the Cray supercomputer is the highly successful Control Data Corporation Cyber 205. In 1976, the Cyber 203 was introduced; only one was delivered. The Cyber 205, a significantly improved version of the Cyber 203, was announced in 1980. It is an all-LSI version of the 203 that also uses newer technology to upgrade CDC's Star-100 architecture. To date, Control Data has 14 of its Cyber Series 200 computer systems installed.

The University of Manchester in the United Kingdom has ordered a Cyber 205 supercomputer, to be installed in April 1983. It will serve some 30 universities, polytechnics and research institutions. This is the second leading European university to install a Cyber 205; one was installed at the University of Bochum, Germany, earlier in 1982. It is interesting that these supercomputers are now making their way into universities, since in the 1970s they were only used in advanced research institutions.

Building on the architecture of the 203, the Cyber 205 includes a scalar processor unit that provides instructions that are fully compatible with the vector stream processor unit but independent of parallel operations (**Figure 2**).

All instructions from central memory are received and decoded by the scalar processor; decoded vector and string instructions are sent to their respective processors for execution. The scalar processor also provides buffering and execution of load and store instructions.



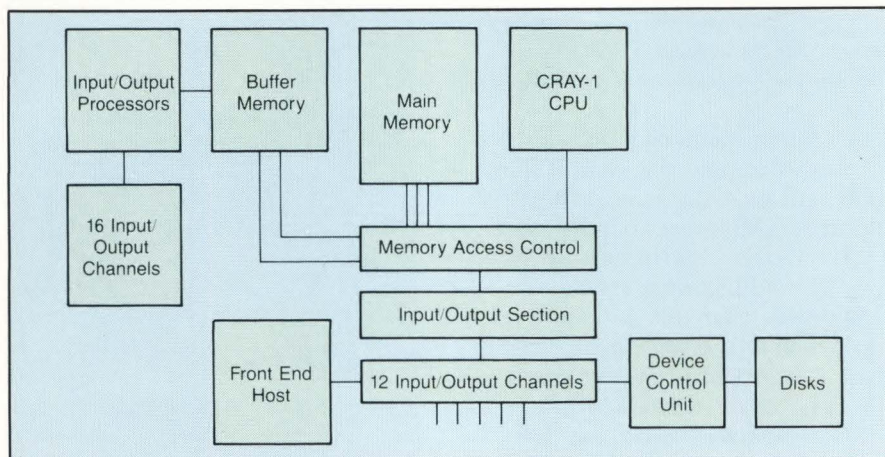


Figure 1: The Cray-1 extends CDC's early pipeline concepts.

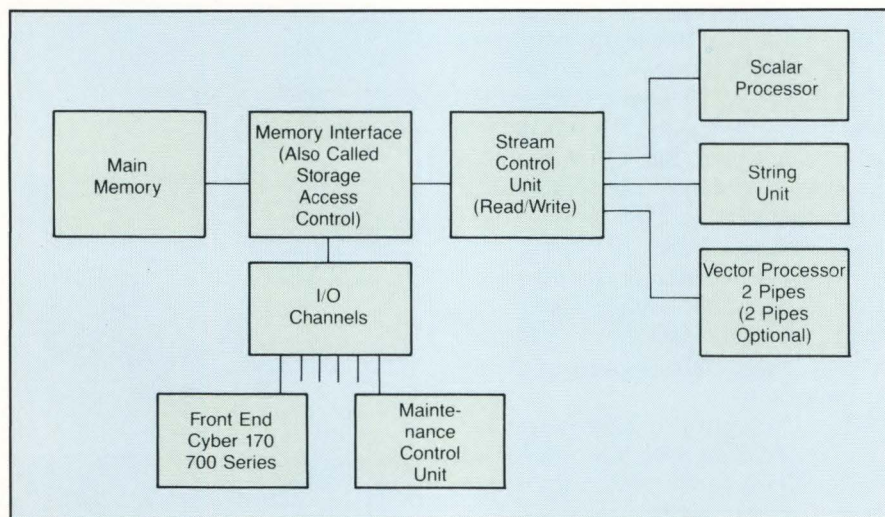


Figure 2: CDC's Cyber 205 utilizes a scalar processor unit.

The scalar processor instruction stack accommodates eight virtually addressed (64-bit) words, which consist of 64 64-bit instructions, 128 32-bit instructions or a combination of both. The instruction issue pipe can issue one instruction every 20 ns. With independent vector and scalar instruction controls operating on a single stream, the scalar processor can execute scalar instructions in parallel with most vector instructions if there are no memory references generated by the scalar instruction. The scalar processor has five pipelined floating-point functional units capable of accepting operands every 20 ns.

The vector processor contains two floating-point pipeline arithmetic units. The stream unit manages the data streams between central memory and the vector pipelines. Pipelined arithmetic units provide vector addition, subtraction, multiplication, division or square root with one 64-bit or two 32-bit results. The 205 system has two pipelines with 20 ns clocking per 64-bit result without chaining or linking, and an option of two additional pipes. The string unit processes the control vectors during streaming operations.

The Cyber 205 has 16 16-bit input/output channels. The I/O sys-

	MPP	Cyber 205	Cray 1
Instruction Word Lengths	32-bits, 64-bits	32-bits, 64-bits	16-bits, 32-bits
Clock Period	100 ns	20 ns	12.5 ns
Programmable Addressable Registers	(5) 16,384-bits (1) 491,520-bits	(256) 64-bits	(72) 24-bits (584) 64-bits
Instruction Stack	16 vector calls	64 words	64 words
Hardware Look-ahead/Overlap	Vector/Scalar/IO overlap	16-32 instructions	256 instructions
Functional (e.g.)	1 unit (16,384 bit-serial PEs)	14 (6 vector: 2 FL PT, 1 String; 5 Scalar: ADD/SUB, MULT, LOG, SHIFT, DIV/SQ)	13
Pipeline Segments	none	Up to 26	Up to 14 segments with a result every clock
Maximum Vector Results Rate	$2500/16,384 = .153$ ns (8-bit addition)	$20/2 = 10$ ns (2 pipes)	12.5 ns

Table 1: Comparison of CPU organizations.



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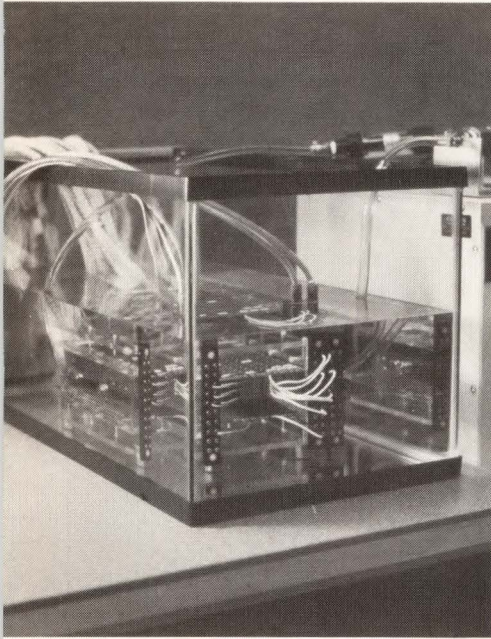


Figure 3: Cray-2 Technology involves the immersion of the computer in a clear, inert fluorocarbon liquid to provide cooling for the system.

tem consists of 16-bit word mini-computers; up to 10 disk stations can be put on the 205. Each station can accommodate eight disk drives; the system now uses CDC 819 double-density 600 MByte disks.

Japanese Supercomputers

In Japan, Hitachi Ltd. has announced the "S-810/10 and S-810/20 Array Processor Systems," new supercomputers that will be marketed only in Japan for the next four years. They claim that the S-810/10 has an execution rate of 315 million floating operations per sec-

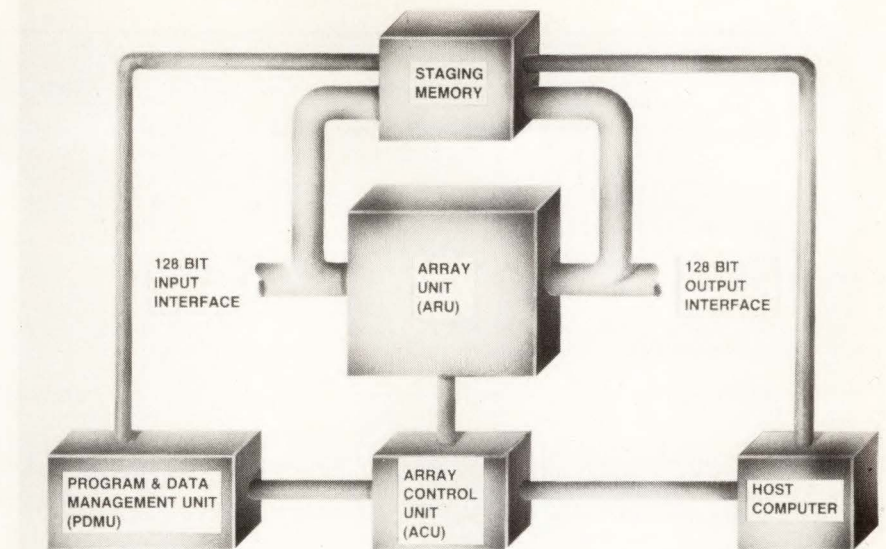


Figure 4: Goodyear Aerospace's MPP comprises four hardware components.

ond (Mflops), while the S-810/20 model executes 630 Mflops and has up to 32 channels rated at 96 Mbytes/sec. Their main storage capacity is 128 Mbytes.

Fujitsu Ltd., also in Japan, has unveiled their intention to produce two new supercomputer models, the "Vector Processor 200" and the "Vector Processor 100," with shipments in Japan to begin in the fall of 1983. According to the company, the VP-200 is available with 64 Mbytes of main memory, upgradable to 256 Mbytes. It has a maximum of 32 channels with a speed of 48 Mbytes/sec. They have also claimed that the processing rate (in Mflops) will outperform both the Cray and Cyber machines. Appar-

ently Nippon Electric Corp. of Japan also plans to introduce a supercomputer in the near future.

The Cray-2

Seymour Cray's ingenuity and dedication was demonstrated again on November 19, 1981, with the announcement of technology that will allow development of the Cray-2 computer system. The Cray-2 is predicted to be six to 12 times faster than the Cray-1. It will have a 32 million word memory and a CPU cycle time of 4 ns, as compared to the Cray-1's four million word memory and 12.5 ns cycle. It will be a 4-processor multiprocessing system.

The technological breakthrough involved immersing the computer in a bath of clear, inert fluorocarbon cooling liquid (Figure 3). The liquid will be approximately room temperature (72° F) and flow amongst the densely packed circuit elements to cool the unit.

The fluorocarbon liquid is normally quite clear with the consistency of salad oil and becomes turbulent due to heat generation; the turbulence indicates hot spots in the computer and has also been described as "quite beautiful to watch." For these two reasons, the company may enclose the Cray-2 in a clear frame.

The Cray-2 CPU will be one-tenth the size of the Cray-1, stand-

	MPP	Cyber 205	Cray-1
8-bit Operands			
Addition	$6553 \times 10^6/s$	—	—
Multiplication	$1861 \times 10^6/s$	—	—
Division	$1531 \times 10^6/s$	—	—
32-bit Operands			
Addition	$470 \times 10^6/s$	$200 \times 10^6/s$	$80 \times 10^6/s$
Multiplication	$291 \times 10^6/s$	$200 \times 10^6/s$	$80 \times 10^6/s$
Division	$149 \times 10^6/s$	$25 \times 10^6/s$ (square root also)	$25 \times 10^6/s$ (reciprocal approx.)
64-bit Operands			
Addition	—	$100 \times 10^6/s$	$80 \times 10^6/s$
Multiplication	—	$100 \times 10^6/s$	$80 \times 10^6/s$
Division	—	$12.5 \times 10^6/s$ (square root also)	$25 \times 10^6/s$ (reciprocal approx.)

Table 2: Computation rates of the various CPUs.

	MPP	Cyber 205	Cray-1
Memory Word Length	Programmable Word Length (e.g., 8, 16, 32, 64 etc. bits)	64 bits (+ 7 bits SECDED /32 bit Half Word)	64 bits (+ 8 bits SECDED)
Memory Access Increment (i.e., Effective Data Path Width)	16,384 words (1 bit from each) (plus 2048 parity bits)	512 bits (i.e., Sword = 8 Words)	64 bits
Address Field	16 bits	48 bits	24 bits
Standard Working Hardware (capacity) Configuration	16M bits	1M Words	1M Words
Incremental Hardware Additions	16M bits, 48M bits	½M, 1M, 2M Words	¼, ½, 1M Words
Maximum Hardware Capacity	1×10^9 bits	4M Words	4M Words
Maximum Virtual Capacity	Not Used	4×10^{12} Words (2^{42} Words)	16×10^6 Words (2^{22} Words)

Table 3: Central memory organization of the MPP, Cyber 205 and Cray-1.

ing 26 inches high and 38 inches long. The eight layer modules for the Cray-2 will be closely packed in three dimensions, to reduce the lengths of the connecting wires and take advantage of the greater potential speed with shorter interconnects. The longest wire in the Cray-2 will be 16", as compared to 4 ft. in the Cray-1.

The Fifth Generation

MITI and six Japanese mainframers have set 1989 as a target date for the development of a new supercomputer able to perform 10 billion floating point operations per second. In the US, the Defense Advanced Research Projects Agency (DARPA) is seeking congressional approval for a plan to spur development of a new generation of supercomputers.

DARPA Chief Dr. Robert Cooper has said that the aim will be to take developing technologies like artificial intelligence, multiprocessor architectures, gallium arsenide semiconductors and machine-generated software and integrate them into single systems. "The goals are something like the Japanese fifth-generation computer program, but theirs is meant for commercial applications. Ours is targeted at military applications," he said.

Developers in both the US and Japan believe that architectures combining up to 10,000 individual

processors will have to be developed. The successful supercomputers of today, including the Hitachi S-810/20, Fujitsu VP-200 and the Cray-2 are still basically uniprocessor architectures, even though as many as four CPUs may cooperate on a problem.

Massively Parallel Processor

Under contract to NASA/Goddard Space Flight Center (GSFC), the Goodyear Aerospace Corporation is developing the Massively Parallel Processor (MPP). Delivery was set for April 1983; in June, 1983, a fully operational MPP is to be delivered to the NASA/GSFC for multi-

agency algorithm development. This machine has 16,384 (16K) processors operating in parallel and can perform over six billion 8 bit additions or 1.8 billion multiplies per second. There have been continuing attempts to build machines with parallel processors, but 16,384 processors operating in parallel is certainly the most ever contemplated.

MPP was originally and principally intended for ultra-high speed ground-based processing of two dimensional imagery. However, preliminary studies indicate that it can support such diverse applications as general image processing, weather

	MPP	Cyber 205	Cray-1
Memory Cycle Time	100 ns	80 ns	50 ns
N-way Interleave	None in central memory	32 Banks	16 Banks
Maximum Bandwidth (Words/sec)	2500×10^6 (for 64-bit Words)	400×10^6 (64-bit Words) with 4 MW Capacity	320×10^6 (64-bit Words) (80×10^6 per Bank $\times$ 4 Banks)
Maximum Bandwidth	163.0×10^9	25.6×10^9	20.48×10^9 (4×80 MW/s $\times$ 64 bit Words)

NOTE: CYBER 205. The memory is bipolar, 80-nanosecond cycle time with 4-word interleave resulting in 20-nanosecond effective cycle times. It has the provision for more memory banks.

Table 4: Characteristics of the central memories.

Parallelism And Mflops

To better understand parallelism, one must consider the definition for computational speed scientific programmers now accept for numerical analysis work: millions of floating point operations per second, or Mflops. Consider the following program segment:

```
DO I = 1, 1000
  Y(I) = A(I)*B(I) + C(I)
END DO
```

Each pass through this DO loop accomplishes two useful floating point operations. Therefore, any computer that could execute this DO loop one thousand times in 1 ms would be computing at a rate of two million floating point operations per second, or 2 Mflops. This measurement refers to accomplished useful operations.

Clearly, more work is done in each pass through this DO loop than one multiplication and one addition. The operands must be fetched from main memory storage and inserted into intermediate registers before they can be fed to the units that perform the floating point operation. The index, labeled I, must be incremented, and some procedure must determine completion of the entire DO loop. About five individual operations must generally take place to complete one useful floating point operation.

In early machines, each of these operations took place individually and in sequence. Later machines, such as the CDC 6600, introduced some simultaneity. Current supercomputers can execute all five operations concurrently and sustain parallel operation for

large percentages of the total time. It is this performance of many operations in parallel that makes the second generation of supercomputers powerful.

Consider the following DO loop for parallel instruction execution:

```
DO I = 1, 64
  Y(I) = A(I)*B(I)
END DO
```

On the Cray-1, this DO loop would be executed and actually produce one answer every 12.5 ns or each clock period. This rate would be sustained from the time the first answer is produced until the 64th answer is produced. For this period of time, the Cray would be computing at a rate of

$1000/12.5 \text{ ns/answer} = 80 \text{ Mflops}$.

For the Cyber 205, the corresponding figure would be

$1000/20 \text{ ns/answer} = 50 \text{ Mflops}$,

although, in some instances, it can operate two pipes to give a 100 Mflop rate.

Note that these are burst rates measured from the time the first answer appears until the 64th answer appears. It takes extra time to set up the operation, and if the length of the DO loop is greater than 64, the entire operation must be grouped in successive segments, since 64 is the maximum vector length on the Cray and the Cyber 205. This procedure does not apply to the MPP. The tables comparing architectures show what each manufacturer did to implement parallel capabilities. They have achieved from tens to over a hundred million floating point operations per second.

simulation/forecasting, aerodynamic simulation/analyses, radar signal processing, reactor diffusion analysis, numerical analysis and matrix processing.

The arithmetic units contain a 128-by-128 array of bit-serial μ Ps with basic cycle rates of 100 ns and, to support its high computation rate, the MPP has an I/O rate of 320 Mbytes/sec. Two-by-four sub-arrays of processors are packaged in a custom VLSI HCMOS chip.

The MPP comprises four principal hardware components (**Figure 4**). Its architecture comprises an array unit (ARU) that processes arrays of data; an array control unit (ACU) that controls the operation of the ARU and performs scalar arithmetic; a program and data management unit (PDMU) that controls the flow of data; and a unique staging memory (SM) that buffers and permutes data.

The array unit contains a 128-by-128 array of bit-serial processing

elements (PEs). The staging memory is a large multidimensional-access memory that performs a "corner-turning" operation which converts data stored in convention-

al format to the bit plane format required for the 16,384 processing elements.

A fully-implemented main stager would hold 67 Mbytes of data. A

	MPP	Cyber 205	Cray-1
Plug-in Modules	190	1760	1700 (× 2 DIES)
Module/Card Types	22	8	115
PC Cards (Boards)	6-9 Layers	15 Layers (150 chips/BD)	5 Layers
Circuitry (equiv. no. of Transistors)	16M (ARU only) 8000 Transistors/ Chip	10.5M (1420 Transistors/ Chip)	2.5M
Chip Types	1 custom chip plus many others	26 (7303 chips total)	4
Logic	ECL	ECL, 6 picojoules 168 gate chips 600 Picoseconds gate delay	ECL, 1 ns per gate delay
High Density Logic	VLSI	LSI-20 ns	SSI

Table 5: Physical hardware/electronics of the various supercomputers.

32-bank main stager can accept and present data at the 160 MByte/sec rate of the Array Unit I/O ports (128 bits every 100 ns). This machine is completely programmable. Both the basic applications programs and the micro-coded routines that drive the processing elements for arithmetic, logic and data manipulation operations are programmable.

The Illiac IV and The BSP

One of the best known attempts at parallel processing is the ill-fated Illiac IV, which was an attempt to make 64 processors operate in parallel. The only Illiac IV ever put into production was at the Ames NASA Research Center at Moffet Field, CA. Its reliability was such that it had difficulty maintaining itself long enough to get to the end of a problem solution. Nonetheless, it worked well enough to be considered a valuable experiment.

Possibly one of the most significant parallel processing experi-

ments ever attempted was the Burroughs Scientific Processor (BSP). The BSP was an advanced array architecture that evolved from Burroughs' significant experience in designing and building the Illiac IV and the PEPE (parallel elements of processing ensemble) machine for the Army's Advanced Ballistic Missile Program.

The BSP, with its 160 ns clock cycle, was to be a more manageable 16-processor system than the 64-processor Illiac IV. The basic arithmetic instruction execution times are 320 ns. (two machine cycles) times 16 arithmetic elements for a maximum rate of 50 Mflops when all 16 processors execute synchronously.

It would be unfair to look at these figures, however, and conclude that the BSP is 25.6 times slower than the Cray. In fact, Burroughs intended to use slower logic, to allow effective use of parallelism.

The BSP was to be direct compe-

tition to the Cray-1 and the Cyber 205. With its 64M word solid state file memory for secondary memory, it would have been one of the first computers to handle programs with data spaces in the tens of millions of words. In 1981, Burroughs had actually taken orders for 1981 deliveries of their machines when they decided to drop its production.

Element Processor

The Heterogenous Element Processor (HEP) developed by Denelcor, Inc. (Denver, CO) is a supercomputer system that can have up to 16 element processors operating in parallel. Each processor can execute one instruction every 100 ns (10 MIPS) and their claim is that 16 units could, therefore, perform at 160 MIPS. It is a 64-bit machine with a maximal system containing 1024 Mbytes of data memory and 8 Mbytes of program memory per processor. At least seven Element Processors were actually installed by the end of 1982.

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Conclusion

A supercomputer is generally characterized by three features: high computational speed, large main memory and fast and large secondary memory. **Tables 1-5** compare the characteristics of some of the supercomputers available today.

The high computational speed is obviously desirable. A large main memory is useful in processing large amounts of data as units and in operating large, complicated programs without time-consuming overlay procedures.

Secondary memory is important in many scientific applications because the data simply will not fit in main memory. In such cases, secondary storage may be regarded as an overflow of main memory. Many scientific programmers spend the bulk of their effort in optimizing such data transfers between memories—i.e., on input/output. Cray and CDC have solved their secondary memory problem with sophis-

ticated disk systems. Vector supercomputers have very fast scalar computation speeds, but their success is directly related to the execution of very large programs with a high degree of parallelism.

The Goodyear MPP, with its 16,384 arithmetic processors, has major architectural differences from the more conventional and relatively similar Cyber 205 and Cray-1, with their combined vector and scalar CPU organizations. Yet the Cray and Cyber have demonstrated marvelous strides in parallel computation due to effective use of pipelining and chaining. It now appears that these machines may face competition from the Japanese front.

The new generation of supercomputers, both in the US and in Japan, may involve a very large number of processors operating in parallel. Several developments with many parallel processors (Illiad IV, BSP, etc.) have failed over the last two decades. The MPP may be one

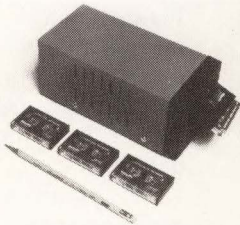
of the first systems with this form of parallel processing to be successful.

Demonstrated success may pave the way for supercomputing in the 1990s. Meanwhile, more conventional innovations such as Cray-2 development assure steady progress.

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- (3) Edward W. Kozdrowicki and Douglas J. Theis, "Second Generation of Vector Supercomputers," *Computer*, Nov. 1980.
- (4) D. J. Theis, "Special Tutorial: Vector Supercomputers," *Computer*, Vol. 7, No. 4, April 1974, pp. 52-61. □

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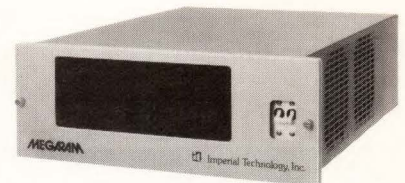
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Off-The-Shelf ICs Simplify Modem Design

by Stephen J. Durham

Only recently in modem design has it become possible to use integral components rather than the more traditional custom printed circuit boards. Now, design engineers can use new monolithic modem ICs to design modems into products easily, because all critical analog functions are provided for them in IC form. Data terminal equipment designers only need to extend the design of their serial I/O port past the Universal Synchronous/Asynchronous Receiver Transmitter (UART or USART) to include a modem. They needn't consider separate PCBs or cables.

There are several key reasons why integrated components are preferred over custom boards. There is no need for RS-232C type drivers/receivers, connectors and cables; therefore system integration is increased. There is no need for an external modem power supply since the integral unit takes its power from the host. Since power

Designing with integrated modem components may very well make the difference between the success and failure of a product.

supplies are typically a system's greatest weak point, reliability is better. Integral modems can extend a product's features beyond their intended scope and open an entirely new market. For example, a CAD workstation with an integral modem can add remote diagnostic and electronic mail features. Using integrated component modems can also result in a 66% profit margin since the modem's cost is only 33% of the market value.

Integral Component-Based Modems

Nearly all low-to-medium speed modems (300-1200 bits/sec) may be

described as shown in the block diagram of **Figure 1**. The modem spans the functional distance from the system μ P bus to the telephone line. At the bus, a compatible UART or USART serializes the parallel data bus for transmission through the modem. At the other end the data coupler connects the modem to the telephone line.

Acoustic and direct connect are the two most practical data couplers. The acoustic method uses audio data carriers generated by the modem and couples them onto the telephone through the phone handset. The direct connect method couples the data carriers directly on the phone line through a Direct Access Arrangement (DAA).

Modem Signal Processor

Figure 2 shows the five fundamental jobs that the modem signal processor performs: modulation, demodulation, transmit and receive carrier filtration, and carrier energy detection.

The modulator for most low-to-medium speed modems is a frequency shift keyed (FSK) type which transmits one frequency for a serial one (mark) and another frequency for a serial zero (space).

Stephen J. Durham, Cermetek Microelectronics, Inc., 1308 Forregas Ave., Sunnyvale, CA 94086.

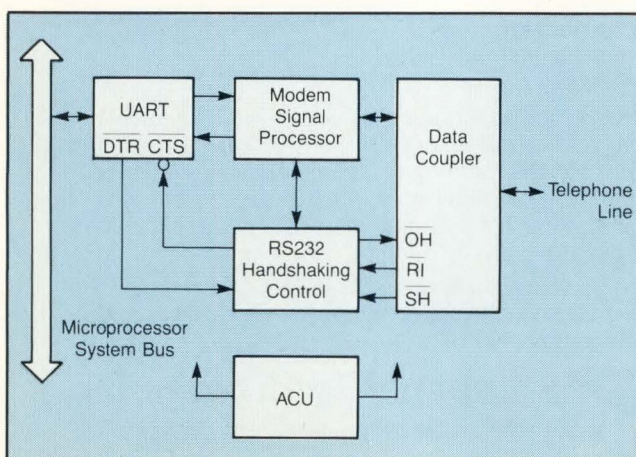


Figure 1: Integrated modem block diagram.

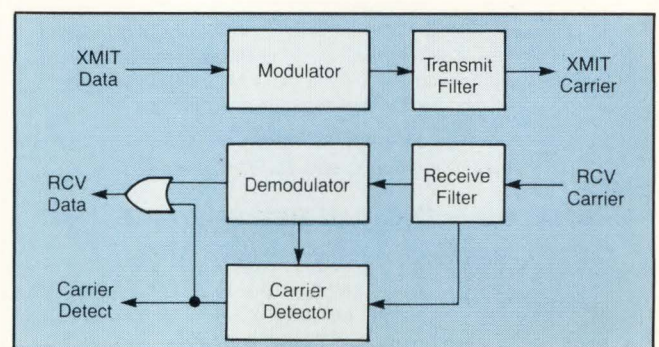


Figure 2: Modem signal processor operation.

Switching from one frequency to another is done phase coherently to minimize generation of needless carrier sidebands.

The modulated carrier is then passed through a transmit filter which rejects modulator signal components outside the transmit signaling band. It is important to limit the transmit carrier energy in the local receiver's frequency band and also in the frequency range above 4 KHz to meet the FCC's Part 68 requirement for out of band energy.

Potential performance level of a modem is determined by the receive filter. It selects the receive carrier signal off the telephone line while rejecting all other frequency bands. The local transmit carrier band, often reflected back by the phone line interface at relatively high levels, is typically rejected using high Q notch filter stages.

The group delay of the transmit and receive filters is also very important. Group delay relates to the propagation time difference for a mark frequency to pass through the filter as compared with a space frequency. Group delay time should be kept small as compared with the modem's baud rate to lessen the effect of bias jitter.

The signal processor's demodulator monitors the extracted receive carrier to decode the amount of

mark or space energy in the receive carrier. Its serial data output reflects the outcome of this weighting function.

The carrier detector monitors the receive carrier's signal strength and sequencing. When an inadequate receive carrier is detected, the demodulated serial data line is clamped to a "1" or a "mark" level. This guards against random or spurious transitions on the receive data line during signal fade-outs or complete carrier loss.

When adequate receive mark energy is detected continuously over a specified period (usually around 150 ms), the carrier detector unclamps the receive data line. If initial space energy is received, the receive data line will remain clamped. Only after initial mark energy carrier detection will the carrier detector consider space frequencies as valid energy. This form of initial OFF to ON carrier detect sequencing is called "mark before space turn ON." The loss of carrier is considered valid only after a specified time of continuous carrier loss (usually 17 ms).

Modem Signal Processors

There are eight monolithic signal processing chips currently on the market. Motorola's MC6860 and MC14412, Advanced Micro Devices' AMD7910, Texas Instru-

ments' TMS99532 and TCM3101, and National Semiconductor's TP3320 and 3321. The Motorola devices have been available for many years, while the AMD and TI chips have been sampled only recently by key customers. The Cermetek CH1760 is a Bell 212A compatible modem component that incorporates the complete modem function, including the direct connect telephone line interface. Many semiconductor manufacturers—Synertek, Mostek, Harris and AMI—are planning to introduce second generation devices this year. Those devices, because they are not yet finalized, are not included in the Signal Processor Summary (Table 1).

Modem Handshaking

When a data telephone connection is set up, set sequence or handshaking protocol must be followed. Most Bell and CCITT compatible modems follow similar sequences.

Modem control can be done with dedicated hardware or with software. In the integrated modem, software control is readily available via the μ P bus, but this implies a level of understanding of the telephone system that the software designer does not always have.

For this reason, modem sequencing is usually provided in hardware and often included in the monolithic modem IC (see Table 1). In any

Device P/N	Mfg.	2nd Source	Technology	Modem Type	Included Functions			Power	Comments
					Mod/Demod	Filters	Control		
MC6860	Motorola	No	NMOS	103	X		X	+5	Filters supplied by Cermetek's Hybrid Filters.
MC11412	Motorola	Yes	CMOS	103, V.21	X			+5	Filters supplied by Cermetek's Hybrid Filters.
AMD7910	AMD	No	NMOS	103, V.21	X	X		+5 -5	Partial auto answer control supplied.
TMS99532	TI	No	NMOS	103	X	X		+5 -5 +12	
TCM3101	TI	No	CMOS	202, V.23	X	X		+5 -5	
TP3320/ 3321	NSC	No	CMOS	203, V.23	X	X		+5 -5 +12	
CH1760	CERME- TEK	No	CMOS, HYBRID	212A	X	X	X	+5 +12 -12	Complete 212A Modem 30011200 BPS with phone line interface and auto-dial/auto-answer.

Table 1: Summary of modem signal processor features.

case, the hardware necessary to provide this function is minimal. Typical modem handshaking is shown in **Figure 3**.

Modem Idle

The integrated modem is idle when the telephone line has not been seized or is ON HOOK. The modem is forced out of its ON HOOK state when it detects a telephone line ringing signal for auto-answer or a transition of the telephone DATA exclusion KEY.

Originate Mode

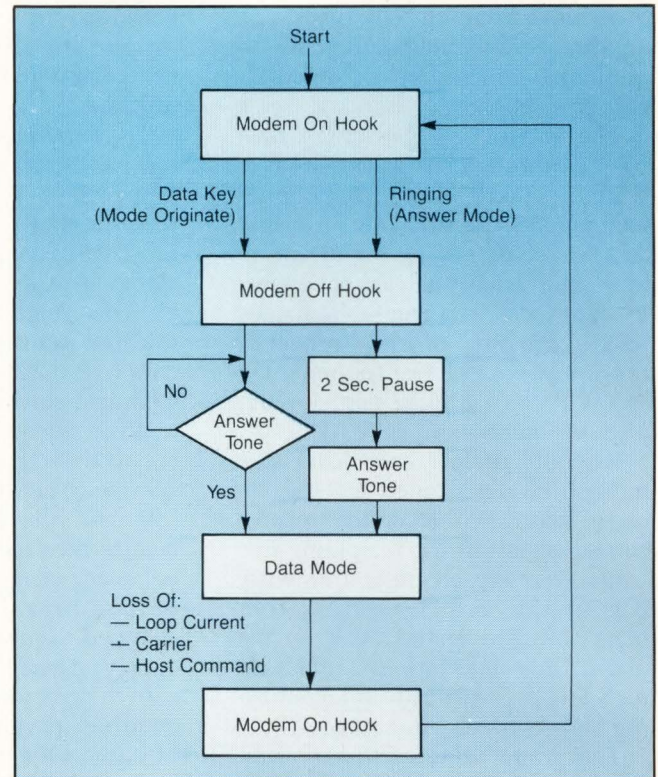
Originate mode is begun after telephone dialing is completed. Dialing can be done via an external data-phone or by an internal auto-dialer. In either case the integral modem begins its sequencing when an initialing DATA KEY signal is received. This signal could come from a manually operated button (dialing through an exclusion key-type telephone) or through the auto-dialer. After dialing, the modem must direct the telephone line to go OFF HOOK and wait for the far end modem to return answer tone. At that time it may unsquelch its modulator and transmit a data carrier, thereby entering the DATA MODE.

Answer Mode

On integrated modems where auto-answer is necessary, the detection of ringing on the telephone line places the modem in the ANSWER MODE. The natural response to this is to take the modem OFF HOOK or seize the telephone line, but the modem should wait for the inter-ringing interval before going OFF HOOK. The wait prevents needless contact degradation of the Direct Connect Protective Hybrid's (DCPH) OFF HOOK relay caused by high ringing voltage line transients.

After going OFF HOOK, the integrated modem's transmitter must be silent for a minimum of 2 seconds to comply with the FCC Part 68 silent billing delay period. After that delay, ANSWER TONE may be sent to the calling or originating modem and a transition to the DATA MODE may be made.

Figure 3: Typical modem handshaking.



Data Mode

In DATA MODE, the modem's signal processor does all the work. Its primary function is to modulate and demodulate frequency shift keyed (FSK) data. DATA MODE continues until conditions indicate that data communications have ended. For full duplex modems like the Bell 103 or Bell 212A, two primary conditions signal the end of a data link: loss of receive FSK carrier, and the host controller's software command to disconnect.

On half-duplex modems such as the Bell 202, loss of receive FSK carrier cannot be used as a disconnect signal because this condition exists normally during periods while communication direction changes. For this reason, it is the host command that forces half-duplex modems to disconnect. At that point, the modem control asserts an ON HOOK condition to the telephone line and returns its sequencing to the start, or ON HOOK mode.

Telephone Line Interface

The modem data coupler joins the transmit and receive data carriers

onto the telephone line either acoustically, or metalically by an FCC Part 68 registered Direct Access Arrangement (DAA).

Acoustic coupling uses the telephone handset (usually through tightly fitting rubber caps) to send and receive data through the handset's speaker and carbon microphone. The major advantages of this technique are that it does not require Part 68 registration and that it is portable. In places where direct telephone line connection is not possible, such as a phone booth, you can couple through the telephone handset.

Unfortunately, the conveniences of acoustic coupling are often outweighed by the disadvantages. The standard telephone handset was never intended to transmit data. Its carbon microphone is fine for voice but presents signal distortion problems for data. But more importantly, the acoustic technique does not allow auto-answer and auto-dial operations which are a desired feature when the modem is integrated within the host data terminal equipment.

Direct connect coupling eliminates the non-linear telephone

Feature	CH 1810	CH 1812
1. FCC Registered	Yes	On Users PCB
2. Small Size	2" x 2"	1" x 2"
3. Lighting Surge, Isolation, And Hazardous Voltage Protection	Yes	Yes
4. Ringing Detect	Yes	Yes
5. On/Off Hook Control	Yes	Yes
6. Line Powered	No	Yes
7. Xmit Level Squelch	Yes	No
8. Xmit Band Limiting	Yes	No
9. Billing Silence	Yes	No
10. Price (1K)	\$50	\$15

handset, allows clear data transmission, and also permits two key functional modem operations: auto-answer and auto-dial. FCC rules and regulations covering direct connect links to the public telephone network require careful design and selection of discrete components to be connected to the phone lines. In addition, a fairly complex FCC application must be filed and *approved* before the interface is certified by the FCC for legal direct connection to the telephone network.

Cermetek provides a family of DAA components to meet FCC requirements and simplify the coupling. The family of Direct Connect Protective Hybrids (DCPH) consists of two DAA devices, the CH1810 and CH1812 (Figure 4).

The key differences between the DAA interfaces is FCC registration and cost. The CH1810 is Part 68 registered and conveys that registration to the host modem and data system, provided that the Cermetek-supplied registration label is displayed on the outside of the host data system. The CH1810 necessarily duplicates many of the FCC required functions typically found in a modem in order to convey its FCC registration. Examples are transmit level and billing delay control. The minimal cost of the function duplication is more than outweighed in low-to-medium volume applications by the savings gained in avoiding the lengthy FCC registration cycle.

In high-volume use where cost is a key factor to the success of the product, the CH1812 DAA is a better choice than the CH1810. It

is more cost effective because it is tailored to the modem application with no modem feature duplication.

However, the data system must go through Part 68 registration with the CH1812 integrated onto the host printed circuit board.

In the long run the expense and costly time delays associated with FCC registration are not major concerns, but the two to six month registration cycle may prove to be prohibitively long and seriously af-

The CH1810 may be used initially as the host's DAA, enabling immediate registered product introduction.

fect product sales. For this reason the CH1810 also serves well in high-volume applications. The CH1810 may be used initially as the host's DAA, enabling immediate registered product introduction. When time permits, the CH1810 can be replaced with the CH1812 at less cost and without concern for registration delay times.

Integrated Auto-Dialing

A fundamental feature of an integral modem is auto-dialing. This

Figure 4: Features of the Direct Connect Protective Hybrids (DCPH) family DAA devices.

enables the host machine to use its communication facilities with or without an operator.

Five major circuit elements are needed to design an auto-dialer into an integral modem: a pulse dial generator, a DTMF generator, a call progress tone detector, telephone number storage, and a controller that sequences the dialing process. Cermetek's CH1820 Automatic Call Processing Unit provides all these functions on one IC (Table 2).

CH1820 Application

Figure 5 shows how the CH1820 integrates easily into typical modem architecture. The IC obtains its digits to be dialed over the same serial data lines that the host uses to transmit and receive modem data. This simplifies the interface with the host since it eliminates additional ports required to communicate with the auto-dialer. The CH1820 uses the serial data lines (TXD, RXD) to receive commands and return status only when the modem's clear to send (CTS) line is OFF. This indicates that the modem is not ready to transmit data over the telephone line and, therefore, transmit and receive data lines are not in use. When the modem's CTS line is ON, the CH1820 no longer monitors the serial data lines and becomes transparent to modem operation.

The modem's CTS line is looped through the CH1820 enroute to the host UART. When the modem is IDLE (its ON HOOK, OH, line low, and its CTS line is OFF) the CH1820 asserts CTS to the host UART ON to enable dialer communication. After auto-dialing is complete and remote modem answer tone is detected, the CH1820 simply loops the logic state of the CTS line from modem to UART. The modem is given indication to begin its originate call sequencing at this time by the assertion of COS (Call Originate Status).

Pulse or DTMF dialing is accom-

P/N	Mfg.	Pulse Dial	DTMF Dial	Number Storage	Call Progress Tone Detect	Dialing Sequencer
CH1820	Cermetek	Yes	Yes	Yes (7)	Yes Dial Busy Ring Back Modem Answer Voice	Yes
TMS 99531	TI	Yes	Yes	No	No	No
MM5393	National	Yes	No	Yes (1)	No	No
MM5395	National	No	Yes	No	No	No
MK5494	MOSTEK	No	Yes	Yes (1)	No	No
MK50981	MOSTEK	Yes	No	Yes (1)	No	No
S2560A	AMI	Yes	No	No	No	No
S2860	AMI	No	Yes	No	No	No

Table 2: Comparison of auto-dialer features of various devices.

plished simply by allowing the CH1820 to respectively pulse the DAA's OH (ON HOOK) line or assert DTMF tones on the DAA's TRXCAR (Transmit Carrier) line. The CH1820 gains access to both of these signal lines by looping them through itself. When the CH1820 is not dialing, the looped modem signals are passed unaltered.

CH1820 Call Sequencing

The CH1820 takes its dialing commands serially from the host UART. These commands are decoded in ASCII as indicated in **Table 3**. Before these commands are accepted, however, the auto-dialer must be prompted or awakened. This is done by transmitting two consecutive Carriage Returns (CRs) to the CH1820. The CH1820 responds by entering the DIAL mode and returning the serial ASCII status:

DIAL: Once a dial command has been given, the CH1820 sets up to dial the number as referenced in the command or as addressed in on-chip memory. Call dialing is initiated by seizing the telephone line (asserting ON HOOK, OH, HIGH) and waiting for dial tone.

Failure to receive dial tone within 2 seconds causes the CH1820 to issue the status: No Dial Tone. It will then continue to try and dial the number anyway. This enables the CH1820 to be used in areas where dial tone does not match the

US domestic standard. If this is not desired, the host may issue a quit command; Q, to terminate dialing.

Automatic Dial Mode

The CH1820 supports the feature

of Automatic Dial Mode Selection between pulse and DTMF dialing (**Figure 6**).

Once the dialing mode is selected, dialing continues without further evaluation until the end of the

Figure 5: General CH1820 auto-dial configuration.

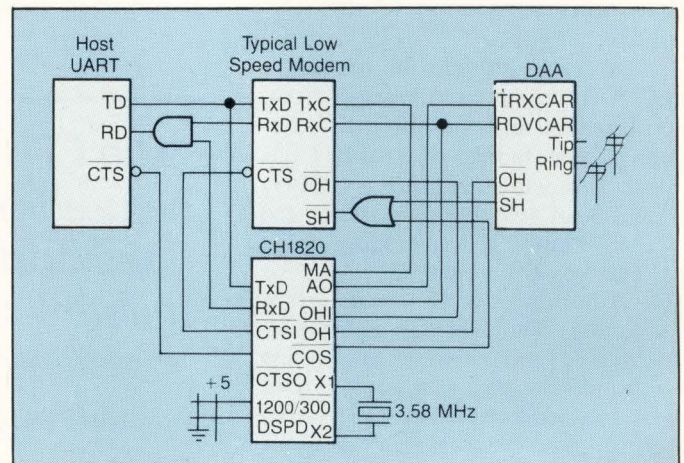
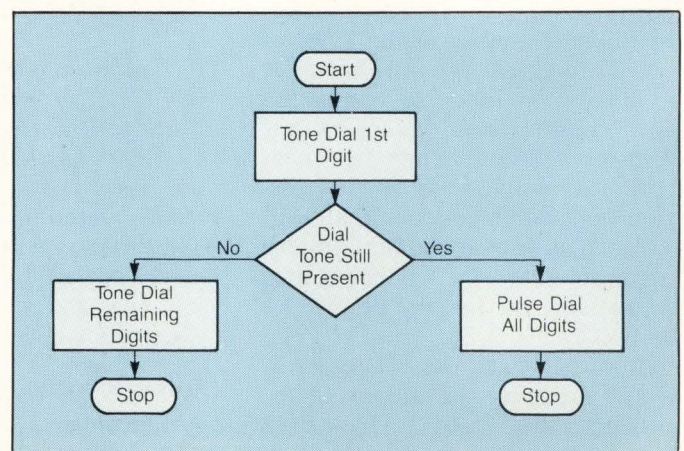


Figure 6: Auto-dial mode selection.



COMMAND SYNTAX	RESPONSE
1. D: NUMBER ^[1] CR	Dial (Number)
2. D L	Dial Last Number Dialed
3. D R N	Dial from Memory Location N
4. D R N M	Dial from Memory Location N, M Times or Until Answered
5. S N NUMBER ^[1] CR	Store NUMBER in Location N
6. L	List all stored Numbers
7. Q	Quit Dialing Process
8. (Null Line) CR	Exit Dialing Environment
9. H	Help, List Command Summary

NOTE 1: "NUMBER" represents an ASCII digit string telephone number. Only digits 0-9, # ad*, and 2 pause characters (=,.) are accepted as valid string characters.

Table 3: CH1820 command summary.

telephone number is reached or until a ">" pause detector is encountered while dialing. If a ">" is decoded within the dial NUMBER string, the dial mode is re-evaluated (**Figure 6**). Dial mode re-evaluation during dialing can be useful for carrier facility access from a pulse only subscriber exchange. Value-added carriers like MCI and SPRINT require that after a user dials into their access trunk and waits for a secondary dial tone, the user's ID and called number be entered via DTMF. Without mid-stream dial mode re-evaluation this would not be possible.

Dial Wait Characters

The host may insert wait characters within the telephone NUMBER string to slow down or control the dialing sequence. This is typically done to wait for a secondary dial tone, as is found when dialing through a PABX, to get an outside line or when accessing SPRINT, MCI or similar systems.

The CH1820 supports two wait character types as shown in **Table 3**. The first (>) inserts a 2 second dial tone wait. After receiving dial tone it then auto-selects DIAL MODE. The second (=) simply inserts a 2 second pause in the dialing process. No dial mode alteration or

dial tone monitoring is done.

Call Progress Tone Monitoring

After the actual dialing process is over, the auto-dialer must monitor the telephone line for such indications as BUSY, RINGING, QUIET LINE, MODEM ANSWER and VOICE, and then act.

The CH1820 uses digital signal

The CH1810 may be used initially as the host's DAA, enabling immediate registered product introduction.

processing techniques to detect the call progress tones found throughout North America and many other locals. Since the tone detection characteristics are microcoded on the CH1820, simple code changes can result in compatible detection characteristics for other locals, such as are found in Europe and Asia.

No Tones: If, after dialing, no call progress tones are detected for

17 seconds, the auto-dialer assumes a mis-dial happened or there is a telephone line-related problem and terminates the call with the status message: Try Again.

Ring-Back Tone: After each detected ringing tone, the CH1820 returns the messages: Ringing. If after 6 rings there is no answer, the CH1820 hangs up and returns the message: No Answer.

Busy Tone: If busy tone is detected, the CH1820 hangs up and returns: Busy.

Voice: If, after the 2nd ring, a human instead of a modem answers the dialed number and speaks, the CH1820 detects the syllable nature of the audio and returns a disconnect tone to the human caller, then hangs up and returns the status message: Voice, Try Again.

Modem Answer Tone

When modem answer tone is detected, the modem transfers the call to the companion modem by asserting COS low. The auto-dialer then goes to sleep, ignoring all serial UART commands until the data call is over, indicated by the modem's CTS signals becoming false. Status is returned with the message: Answered-Data Mode.

Conclusion

In the early 1980s we are seeing a trend toward integral modems made of components, which integrate easily into the host data system. This step forward in the efficient use of LSI technology will produce lower communication system costs and higher reliability.

The trend for second generation modem IC manufacturers will be to include the modem handshaking control on board with the signal processing and, eventually, the auto-dialer as well. These modems will continue to be connected to the telephone line with DAA components.

In the mid-'80s third generation monolithic modem ICs should appear and will include the DAA on the chip as well. The chip will also be able to support the high voltage necessary for the DAA to control the telephone line interface. □

Tektronix Introduces Color Graphics Products

In an attempt to widen their customer base, Tektronix has just introduced a group of very low cost color graphics products of considerable interest to graphics system designers. They include a high performance color raster display terminal for \$19,950, a family of color desk top display terminals starting at \$3995, a local graphics processing unit based around Intel's 8086 and 8087 processors for \$5500, and a desk-top ink jet color copier for \$1950.

Ergonomics and speed were primary concerns in the design of the Model 4115 high performance display. High resolution greatly enhances the terminal's display quality: graphic images stored in the terminal's 32-bit coordinate space are displayed at a resolution of 1280×1024 pixels. In addition to this large number of displayed pixels, the 4115's 60Hz non-interlaced display greatly reduces flicker, thus allowing the user to work at the terminal with less eye fatigue.

Writing rates in excess of 50,000 vectors per second are achieved through the use of a bipolar bit-slice graphics processor operating in tandem with the 4115's 8086/8087 CPU. The display list coordinate space is user selectable, ranging from 12 to 32 bits on 12 or 32 bit coordinate space, providing an optimum match to the application. The display list is then traversed by the graphics processor which applies two-dimensional transformations (translate, rotate, scale and clip) and the resultant image is presented to the user on the 1280×1024 color display. The features of pan and true zoom provide the user with fast access to any part of the locally stored graphics data, always displayed with maximum resolution.

The 4100 family of color desk-top terminals, starting at \$3995, range in display size from 13" to 19". Each terminal incorporates a

60 Hz non-interlaced raster-scan display and an anti-glare screen. The terminals can display graphics of up to eight colors at one time from a palette of 64 colors. Resolutions range from 480×360 pixels to 640×480 pixels.

The 4170 Local Graphics Processing Unit converts any one of the 4100 series terminals into a standalone computer specialized for graphics tasks. The unit is designed to bring distributed processing to a host environment. Host data is downloaded to the terminal for interactive graphics, accessing graphic firmware features, and controlling peripherals connected to the terminal.

The 4170 consists of two Intel processors, the 8086 and the 8087 numeric co-processor for data intensive functions, 256 Kbytes of RAM, two $5\frac{1}{4}$ " floppy disks, four RS-232C interface ports with data rates adjustable to 19.2K baud, and three circuit board option slots. The unit is housed in a compact cabinet which fits beneath a bench or alongside a desk.

Using on-demand ink-jet technology, the 4695 color copier produces eight-color copies from computer graphics displays. The 4695 is intended for such applications as data analysis, presentation graphing, and CAD previewing.

The copier can place 120 dots per inch in both horizontal and vertical directions, allowing up to 1280×960 dots per A-size (8.5" $\times$ 11") image. Ink is supplied from separate cartridges containing yellow, cyan and magenta which can be mixed to also print red, green and blue. A separate black ink supply provides a true, dense black. In addition to the standard colors, up to 125 half-tones are available under program control.

A variety of media can be used: A/A4 cut-sheet paper, paper rolls, and, available in September, overhead transparency media. Copy



Figure 1: The Model 4115 computer display terminal features a high performance color raster scan display which displays 1280×1024 pixels at a 60 Hz non-interlaced refresh rate.

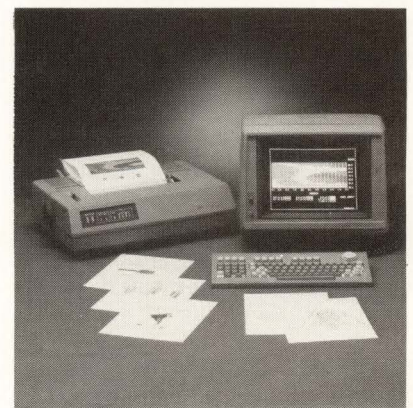


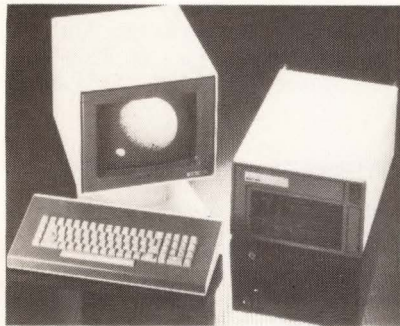
Figure 2: The Model 4105 computer display terminal and the 4695 color graphics copier provide a personal graphics tool to technical and professional users.

speed is about 2.5 minutes/page for a typical copy. Cost per copy will be less than 20 cents. The unit also allows functions as a bi-directional printer at speeds of 20 cps. The Tektronix-designed ASCII font uses a 12×6 dot matrix to form each character. **Write 237**

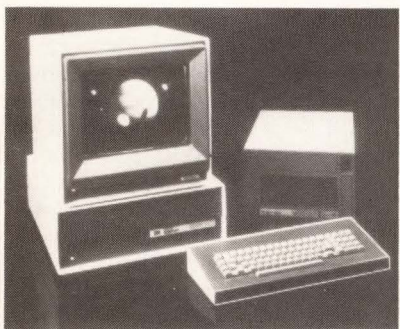
COLOR GRAPHICS

For Distributed Processing Environment

The 8600 is a raster scan color graphics computer that will operate as a stand-alone system or as an intelligent



TERAK 8510 Computer Graphics System



TERAK 8600 Color Graphics Display System

workstation in a distributed processing environment. Its high-quality monitor, standard at $640 \times 480 \times 3$, upgradable to $640 \times 480 \times 6$, offers up to 64 displayable colors from a display palette of 512. A compact unit, the system comprises four components. The color processor contains a 16-bit Intel 8086 μ P, raster scanner and frame buffer. The 13" cathode ray tube (CRT) monitor features an inline color gun, and the keyboard is a 128 ASCII set, with function keys, cursor control group and numeric keypad. The heart of the system is the DEC LSI-11 CPU memory with communication and auxiliary storage, including 2.4 Mbytes of 8" floppy disk storage and four standard RS-232C serial ports. **Terak**, 13444 N. 32nd St., Suite 19, Phoenix, AZ 85032.

Write 126

STANDALONE CAD SYSTEMS

With Vector Refresh

Information Displays, Inc. has introduced a family of standalone CAD systems. CADalyst employs seven independent processing sub-systems, each with their own local program

and data storage facilities. Each unit supports up to 16 Mbytes of addressable memory, features both vector refresh and color raster displays, light pen or data tablet, streaming mag tape drive, and Winchester technology disk with fixed/removable media. Each CADalyst system supports peripherals such as plotters, printers, and telecommunications equipment. CADalyst can be configured in a network that allows it to communicate with other computers and commonly pooled peripherals. On-screen command menus speed task execution on the system. The floating keyboard can be positioned in either a flat or tilt setting and features ergonomically designed keys and functionally placed key pads. Instantaneous response to the light pen and data tablet allows the operator to interactively position, rotate, and scale graphic entities in a continuous stream of motion, facilitating throughput and productivity. Price is \$100,000. **Information Displays, Inc.**, 28 Kaysal Ct., Armonk, NY 10504.

Write 127

ROBOT

For Electronics Assembly

The Model 605 is programmable through a PC and is based on a number of industry standard components. The Intellex Model 605 Robot consists of the robot arm and end-effector, a control computer, a separate



safety computer and an optional, fully integrated vision system. Because vision is integrated into both the hardware and software of the Model 605 the optional vision capability can be plugged into the robot. Features in-

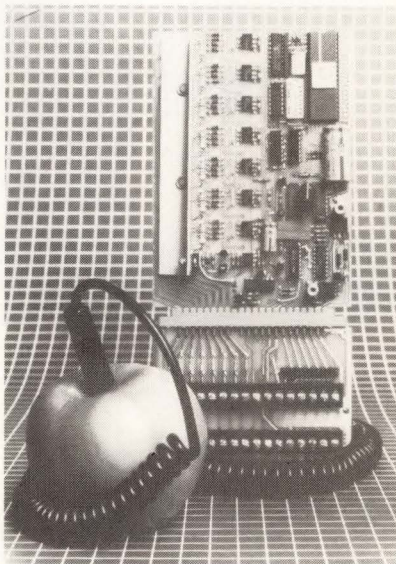
clude software and proprietary stepper-motor control technology, a cpu that addresses one million bytes of system memory, and a design that blends into the automated environment. Price is \$48,000. **Intellex, Inc.**, 33840 Eastgate Circle, Corvallis, OR 97333.

Write 130

APPLE II SOFTWARE

Industrial Control And Monitoring

In this program package the Apple is the controlling computer in a network



using Wintek's 6801 Micro Control System. The MCS is a SBC incorporating both analog and power I/O on a $4.5" \times 6.5"$ card. The software can be customized to fit a wide variety of applications. Price is \$198. **Wintek Corp.**, 1801 Lafayette, IN 47904.

Write 145

CAD WORKSTATION

Produces Publication Quality Documents

The Qubix system is designed as a CAD workstation, and has software that merges text with graphics and interactively produces fully composed pages ready for publication. The resolution of the monitor allows system users to see fonts on the screen in exact size from 4.5 to 120 point in size. The number of font styles available to the user is unlimited. The workstation produces composed pages with text and graphics which are output on high and medium resolution devices. **Qubix**, 18835 Cox Ave., Saratoga, CA 95070.

Write 131

SUPERMINICOMPUTER SYSTEM

With Library Of Application Software Packages

Applications of the Edition VII Workbench include generalized software development, office automation



including word and text processing, timesharing, software configuration management, networking, and applications development and testing. A library of application software packages, developed under Unix, is also available to the user. The system includes a processor with 1/2MB of memory, 65MB of disc memory, eight communications lines, a Model 550B console terminal, and an 8-port Edition VII Workbench license. Price is \$49,950. **Perkin Elmer**, 2 Crescent Pl, Oceanport, NJ 07757. **Write 135**

NETWORK BUILDING BLOCKS

Flexible Remote Access

The NETWAY family can be configured as a multiplexor data concentrator, protocol converter, cluster controller, packet processor and nodal processor. It includes distributed communications-oriented hardware and a proprietary communications operating system. Features include a communications processor, local network interface, device interface processor, and a network interface processor. The networking software provides automatic alternate routing, on-line configuration from any workstation and allows any workstation to communicate with any host on the network. Price is \$11,040. **Tri-Data**, 505 E. Middlefield Rd., Mountain View, CA 94043. **Write 143**

MINICOMPUTER SYSTEM

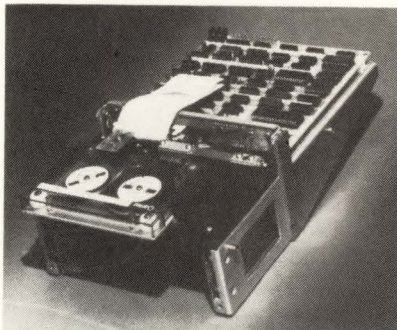
For Vax-11 Users

ULTRAVAX systems substitute firmware-driven controllers on each Uni-bus, CMI-bus or SBI-bus for the more traditional, discrete logic-driven controllers used in DEC's standard configurations. These μ P-based controllers permit integration of peripherals with large capacities. The controllers comprise bipolar, bit-slice μ P designs incorporated onto single-board or single-board-extended packages that fit into available VAX backplane slots without modifications. All basic control, status and data transfer operations are implemented by micro-code. ULTRAVAX controllers are software-transparent to VAX/VMS, UNIX and DEC diagnostics. **California Computer Group, Inc.**, 3303 Harbor Blvd., Costa Mesa, CA 92626. **Write 128**

1/4" STREAMING TAPE SYSTEM

Extended Storage Capacity

The 1/4" streaming tape system operates at a speed of 90 inches/sec and at a maximum data-transfer rate of up



to 72 kbytes/sec. Called the Streamer 410, the cartridge-based system stores a minimum of 45 Mbytes of formatted data on a standard DC300XL cartridge.

Designed to provide backup storage for Winchester disks of 30 Mbytes and greater capacity, the Model 410's storage capacity increases to 60 Mbytes when equipped with a 600 ft. DC600A cartridge in place of the standard 450ft. DC300XL. The drive's two-channel bidirectional tape head with its separate erase bar records data on eight tracks.

The Streamer 410 is controlled by two separate μ Ps—one for the tape drive, the other for the controller. μ P control permits features such as an automatic tape reference to ensure cartridge interchange, automatic identification of cartridge type, and a se-

ries of automatic diagnostic tests at power-up and cartridge insertion. Diagnostic tests include a RAM and ROM check, exercising of the tape drive, locating the edge of the tape and track identification. A standard command allows the tape to run from end-to-end to initialize the cartridge. Price is \$1,625. **Qantex Div.**, North Atlantic Industries, Inc., 60 Plant Ave., Hauppauge, NY 11788. **Write 203**

TURNKEY WORKSTATION

For Automated Custom IC Design

The ZyPAWS workstation uses the 32-bit virtual memory Prime 2250 computer, which supports 20 users. It is a front-end workstation used for logic simulation, circuit simulation and test-program generation and is a fully integrated workstation with color graphics capability for performing automatic cell placement and routing. ZySPICE is a circuit simulation program based on SPICE version 2.E and modified by ZyMOS to include enhanced small-geometry transistor models. ZyPSIM is a proprietary event-driven logic simulator. ZyTEST is a suite of proprietary ZyMOS software modules that converts to the output of the ZyPSIM simulator into Sentry series compatible automatic



test programs. ZyPART, available with ZyPAWS II, is a collection of proprietary ZyMOS programs which automatically generate a cell placement and routing directly from the ZyPSIM network file. Price is \$100 to \$150. **Zymos**, 477 N. Mathilda Ave., Sunnyvale, CA 94088. **Write 136**

IBM-COMPATIBLE COMPUTER SYSTEM

Customizing Ability

The Raytronics computer system enables the user to customize a system to individual needs. Called an IBM



PC "work-alike" computer system, it is fully compatible with the IBM Personal Computer. The chassis contains a plug-in 8088 CPU board, a 12-slot bus for expansion, and a heavy-duty 80W power supply. The front panel cutout accepts two thinline, 5¼" floppy disk drives or Winchester. When the CPU board is removed, the cabinet can be used as an expansion chassis. It will accept all IBM PC-compatible circuit boards. The computer system can be configured with both its manufacturer's expansion and interface cards and those from other third-party vendors. **Vitek**, 930-G Boardwalk Ave., San Marcos, CA 92069 **Write 149**

COLOR GRAPHICS SYSTEM

Interfaces with IBM, DEC, And PE

The System 1500 provides a full range of interactive features. The controller supports from one to four workstations. When configured with a communications controller, it can support up to 64 workstations. It is offered with 32-bit parallel interfaces for IBM, Perkin-Elmer, and Digital Equipment Corp. host processors. It can accommodate graphic applications such as: CAD/CAM, Signal Processing, Seismic Interpretation, Command and Control, Simulation, and Mapping. Price is \$19,900. **Spec-tragraphics**, 10260 Sorrento Valley Rd., San Diego, CA 92121. **Write 209**

COMPUTER-AIDED-ENGINEERING WORKSTATION

For Design And Analysis

TEGASation, a digital design workstation, is intended for the design and analysis of digital electronic circuits and systems. The workstation provides design capture, simulation and

analysis software, all of which can be used at the designer's workplace. Price is \$60,000. **CGIS**, 7701 North Lamar Blvd., Austin, TX 78752

Write 208

IMAGE DISPLAY AND ENHANCEMENT SYSTEM

For High Speed Graphics

The Model 280-62 Graphics Image Display and Image Enhancement System is a member of the newly introduced Series 2800 family of raster scan image processing, image display, and computer graphics peripheral equipment. It is a 1024 × 1024 resolution system for the display and enhancement of digital images, the generation of computer graphics, or the merging of graphics information with digital images. The system can handle up to three banks of 1024 × 1024 by 8-bit memory, each bank with up to four overlays. The configuration is programmable and permits four bit greyscale, eight bit greyscale, 10 × 12 pseudo-color or 24 × 24 full color displays. Features include memory

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Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

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New Products • COMPUTERS/SYSTEMS

boards equipped with a 10-bit input by a 12-bit output video lookup table. Price is \$27,000. **Grinnell Systems Corp.**, 6410 Via Del Oro Dr., San Jose, CA 95119. **Write 132**

CAD SYSTEM

For Process Plants

The Design Station I combines computer graphics with local plant design intelligence. Plant views appear in color and can be interactively moved, rescaled, and viewed from several directions at the same time. The DS1 offers the designer hidden line plant



views in color, which can involve the routing of 1,000,000 individual components. The workstation also has a multiple viewport facility which allows the user to look at several different views of a design simultaneously. Price is \$89,500. **Cadtrak**, 823 Kifer Rd., Sunnyvale, CA 94086. **Write 129**

DATA MANAGEMENT SYSTEM

3-D Graphics Capabilities

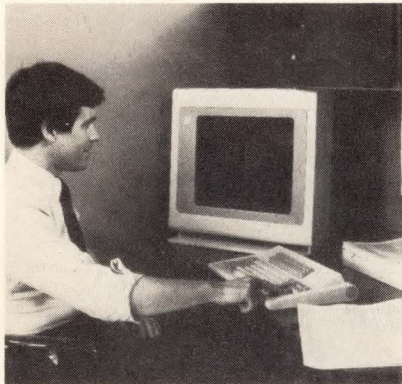
In addition to its data management, statistics, and modeling features, the RS/1 has two and three dimensional graphics capabilities. These graphics include plotting of data points, control over rotation and perspective, terminal and plotter independence, and are completely integrated with the rest of the system. As a research system the RS/1 gives the user access to data entry and retrieval, data transformation and analysis, statistical analysis, and curve filling. It has a list of RPL functions and analytic capabilities. Price is \$13,400-\$32,500. **BBN Research Systems**, 10 Moulton St., Cambridge, MA 02238. **Write 148**

New Products • PERIPHERALS

LARGE-SCREEN DISPLAY

Gas Panel Technology

The IBM 3290 information panel uses a state-of-the-art flat gas panel to display up to 9,920 characters of data on a distortion-free screen that is 10.7"



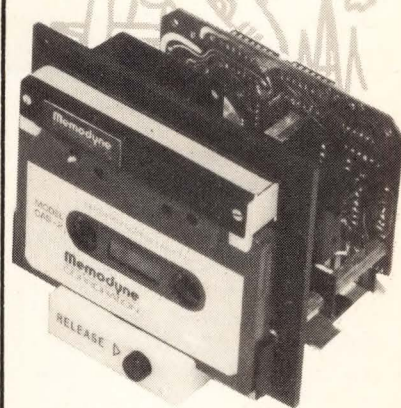
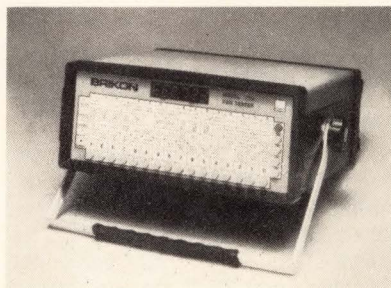
by 13.4". The 3290 can simultaneously display text in various character fonts, line drawings, charts and sketches. The large viewing area can be divided into quadrants to provide access to four different applications or data bases in one or more computers. The 3290 attaches to IBM System/370,

30XX, and 4300 series computers, and to the 8100 information system, via an IBM 3274 control unit. Price \$7,100. **IBM**, 900 King St., Rye Brook, NY 10573. **Write 188**

AUTOMATIC TESTER/EXERCISER

Counts Passes And Errors

Designated the Brikon 723S, the tester/exerciser is aimed at field maintenance, production-test and quality-control applications, and can simultaneously handle up to eight diskette drives. It incorporates a Z80 μ P tied to 4K bytes of (RAM) and 16K bytes of (EPROM).



(MODEL 201 SHOWN)

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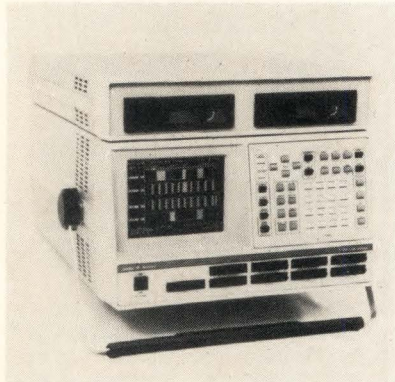
Write 59 on Reader Inquiry Card

When connected to one of the drives, the 723S will automatically verify R/W functions using random worst-case data patterns, depending on the recording format (FM/MFM), or using optional 15-byte patterns entered manually by the operator. The tester counts passes and errors, and will display error information such as date pattern, byte number, error byte and expected byte. The 723S can also operate in a read-only mode using diskettes previously recorded with worst-case patterns. Price is \$4195. **Brikon, Inc.**, 22981 Alcalde Dr., Laguna Hills, CA 92653. **Write 187**

LOGIC ANALYZER

Built-In Data Reduction

Gould Biomation's K105-D is an up-to-72-input logic analyzer intended for digital system design and develop-



ment, including software analysis, hardware analysis and hardware and software integration. Slots in the analyzer's chassis accommodate boards to expand or reconfigure its capabilities. Menu-driven screens enable the user to easily set up the logic analyzer. System activity can be sampled synchronously by using eight external clock inputs that can be combined into four Boolean expressions. The K105-D also includes optional disassemblers for the 68000, 8086, 8088, Z80, 8085 and 8080 μ Ps. The storage system provides additional memory through two formatted 328 Kbyte, 5 $\frac{1}{4}$ " floppy disk drives. The Storage System can store up to 70 setup and measurement data files for more than one user or for later reuse or reference. Price is \$8,995. **Gould Inc.**, 4600 Old Ironsides Dr., Santa Clara, CA. **Write 191**

DESKTOP TERMINAL

High Pixel Resolution

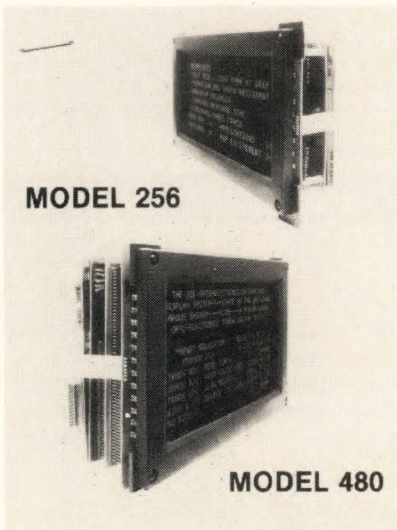
The Whizzard 1645 is a monochrome engineering desktop terminal that

provides high resolution interactive graphics concurrent with alphanumeric capability. Digital VT-100/52 compatibility allows users to perform a full range of graphic design functions as well as software development, documentation and report generation. The 1645 is the black and white version of the 1650 color terminal, and it features higher pixel resolution—1280 $\times$ 980—and is well-suited for intricate design applications. **Megatek Corp.**, 3187C Airway Ave., Costa Mesa, CA 92626. **Write 157**

INTERACTIVE TOUCH DISPLAY

Evaluation Kits

The 256 and 480-character models are featured with options and accessories for the needs of the evaluating engineer. PEP utilizes DC plasma technology with an invisible optoelectronic switch matrix system,



sequential or random data loading, and both on-board refresh and character generating memories. Each model is available with a choice of four interfaces (parallel, serial RS232, differential TTL or 20mA loop). The 256-PEP measures 11.8"W $\times$ 6.64"H $\times$ 3.5"D and the 480 measures 10.2"W $\times$ 7"H $\times$ 3.75"D. **IEE Special Products Division**, 7740 Lemona Ave., Van Nuys, CA 91405. **Write 185**

1/2" STREAMING TAPE DRIVE

Extended Gap

The Vindicator 1/2" streaming tape drive has auto-loading, drawer mount transport and is engineered with extended gap start/stop performance. Its extended gap feature is front panel selectable, and allows for the optimi-



zation of throughput and capacity. The gap is selectable from 0.6" to 10". Designed for traditional and backup applications, the Vindicator provides either 46 or 92 Mbyte unformatted capacity. Other front panel selectable features are auto-power restart and load on-line commands which bring the drive back to ready state after a power failure without operator intervention. Price is \$2,825. **Pertec Peripherals Corp.**, 3151 Airway Ave., Costa Mesa, CA 92626. **Write 189**

COMPUTER TERMINAL

Menu Driven Configurations

The Z-29 terminal features on-screen, menu-driven configurations for user-defined parameter settings to meet desired specifications such as even/odd parity, baud rates, and even handshaking. The Z-29 is compatible with ANSI protocol units and the DEC-VT 52. In addition, it can emulate the majority of DEC-VT 100 functions (in the 80-character mode), Lear Siegler ADM-3A and the Hazeltine 1500. The keyboard has 77 typewriter-style keys (including nine special function keys) and a separate 14-



key numeric keypad to simplify mathematical data entry. On-screen editing includes character or line insertion and deletion, erase functions, tab sets and protected fields. Price is \$849. **Zenith Data System**, 1000 Milwaukee Ave., Glenview IL 60025. **Write 190**

CLUSTER CONTROLLER

For Dealers and OEM's

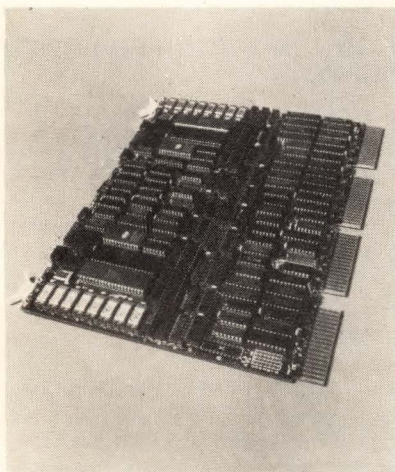
The Z-80 based cluster controller with 16K to 64K of dynamically allocated RAM, is capable of handling a variety of interfaces and protocol translation duties. The Diplomat is a multi-channel interface switch box that allows a cluster of up to four devices of different protocols or interfaces to be linked together for intercommunication and co-sharing of printers. Any configuration can be accommodated, whether it be multiple μ Cs and modems with one printer, or one micro and a variety of peripherals. In addition, the Diplomat contains an internal printer driver, capable of driving a Qume or Diablo-style printer directly. Price is \$595.-\$895. **Intel**, 780 Charcot Ave., San Jose, CA 95131.

Write 205

8- AND 16-BIT CP/M BOARD

For PDP-11 and VAX

The UCP-11 is a board that allows DEC PDP-11 and VAX computers to run CP/M programs. The UCP-11 plugs into the back of a VAX or PDP-11 computer and transforms users' terminals into CP/M workstations ca-



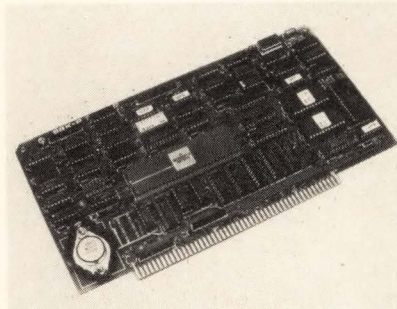
pable of interacting with the DEC computer's peripherals. The UCP-11 acts as a co-processor, operating in parallel with the DEC processor without degrading the latter's performance. The PCP-11 or VAX is called upon only to perform CP/M requested I/O activities. The UCP-11 can be activated from any terminal already attached to a DEC mini network. It is available under RT, TSX-Plus and RSX11 M-Plus. **Alloy Computer Products**, 12 Mercer Rd., Natick, MA 01760.

Write 192

68000 BASED S-100 PROCESSOR BOARD

With FORTH Based Monitor

The MC68000L-based processor board runs at 12MHz but 16, 12MHz



also available. It can address 16 Mbytes of RAM. It features 3 16-bit interval timers that can be used as watch-dog or task switching timers in a multitasking environment. It can accommodate 8K of ROM and is supplied with a powerful FORTH based monitor called bug-FORTH. The on-board language is suitable for many applications and allows the user to write ROMable code. Features include an 8 MHz MC68000L, 16 bit data transfers, and 8 vectored interrupt lines. It supports the standard 246 I/O mapped ports plus an extended 64K of I/O mapped port capability. An extended vectored ID interrupt capability is also available as a jumper option. Price is \$695 in single units, \$349 in OEM quantities. **Inner Access Corp.**, 517-K Marine View, Belmont, CA 94002.

Write 195

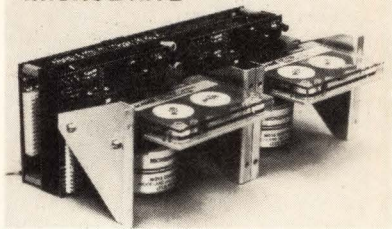
VIDEO TERMINAL BOARD

μ P Based

The Mostek CRT-80E video terminal board is a μ P-based video terminal controller system which emulates the DEC VT100 video terminal. The Mostek CRT-80E card features a printer channel, protected fields, seven separate European character sets plus a built-in ASCII character set, 16 user-defined characters and a 120 x 132-point graphics standard. The board also supports both the RS170 composite video and discrete video/sync formats. The CRT-80E board also includes features such as a programmable-font PROM for up to 768 characters, keyboard-programmable user options stored in EAROM, and five programmable attributes on a per-character basis. Price is \$456. **Mostek**, 1215 W. Crosby Rd., Carrollton, TX 75006.

Write 139

MICRODRIVE



DC100 CARTRIDGE DRIVE HAS SMART I/O

MicroDrive/OEM now features a micro processor based I/O. This unit performs all control and formatting for quick systems integration. A high level command set (22 commands) allows full peripheral status for the model 125I/O. Serial and parallel options are available priced as low as \$400 in OEM qty.

MOYA CORPORATION

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COGNEX

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VME 68000-BASED SBC

No Wait-State 12 MHz Operation

The IV-1600 is a SBC suitable for applications such as industrial robotics, data processing, and high resolution graphics. The system features dual port RAM, which allows access to other CPUs and DM controllers. EE-PROMS in its memory sockets make chip removal and system shut down unnecessary. Price is \$2995.-\$8995. **Ironics Inc.**, 117 Eastern Heights Dr., Ithaca, NY 14850. **Write 199**

ONE MBIT CMOS ROM

For Speech Synthesis

Applications for the CMOS ROM range from speech synthesis products to language processing devices and hand-held translators. The one M-bit ROM is organized 128K-words by 8-bits and uses two-micron technology. Operating on a single five-volt power supply with a ± 10 percent supply tolerance, it has a maximum access time of three μ secs. Power dissipation is 60 milliwatts. It draws 12 mAs maximum power when active, and 10 μ A in standby mode. The CMOS ROM is available in a 52-pin flat pack (D731000G) and a 40-pin DIP package (D731000C). The 52-pin package, for high-density applications, interfaces directly with industry standard CMOS 8-bit μ Ps. Price is \$70. **NEC Electronics U.S.A. Inc.**, 550 E. Middlefield Rd., Mountain View, CA 94043. **Write 138**

FLOPPY DISK INTERFACE

Duplicates DEC TU-58 Cassette Drive

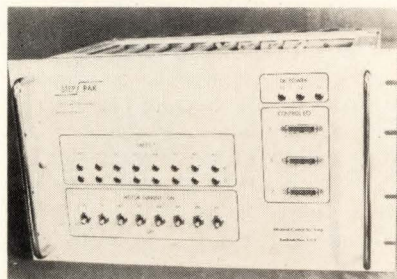
The Z2800 is a single card floppy disk interface featuring a Z80A processor with 2K RAM and 4K ROM, a floppy disk port and a RS-232C port. It is supplied with firmware to duplicate the DEC TU-58 Cassette Drive protocol and a jumper selectable execu-

tive program to enable users to develop their own customer interface. It is designed to provide storage in applications including: program storage for numeric controls, robotics and process controls, data logging, remote processing, and data entry. The Z2800 memory is expandable to a total of 40K RAM/ROM and a second RS-232C port is available. Baud rates and stop bits for the RS-232C port are selectable. The disk port can accommodate single or double sided, single or double density floppy disks from Shugart and other manufacturers. IBM 3740 and IBM 40 formats are standard. Price is \$195.00. **Greco Systems**, 10020 Prospect Ave., Suite A15, Santee, CA 92071 **Write 140**

STEPPING MOTOR DRIVES PACKAGE

Eight Axis

Step-Pak, Model MDU-8 can drive eight stepping motors, currents up to six Amp per motor phase, and occupies only 10.5" of standard 19" rack space. Bi-level driver design offers high performance and efficiency.

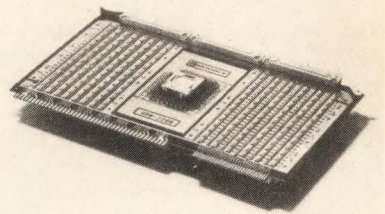


Eight connectors on the back panel provide motor connections and limit inputs. The other features are: forced air cooling, internal logic power supply, eight motor current cut-off switches, and three power status LEDs. MDU-8 requires step and direction input signals for each channel and dual motor power supply 10 VDC and 36 VDC. Current requirements depend on the assortment of motors being used. Price is \$3,600. **Advanced Control Systems Corp.**, 24 Teed Dr., Randolph, MA 02368. **Write 144**

WRAPPABLE LOGIC BOARD

JEDEC Type "A" Chip Carrier Socket.

The new series 2200 wrappable logic board is specifically designed for the Intel Multibus and features a universal layout for .300", .400", .600" and



.900" spaced devices, plus a 68 pin JEDEC type "A" leadless chip carrier socket with wrappable pin-out. The series 2200 board has an IC field of 28 columns of 53 pins. Board capacity is forty-eight 16 pin IC's, plus 4 columns of .600" spaced devices (or 36 additional 16 pin IC's). Additional I/O includes three 50 pin wrappable headers for female ribbon cable connectors including 25 grounded contacts for twisted pair terminations. Additional features are a common ground plane on both sides in socket area, alternate ground terminals for twisted-pair terminations and hollow terminals for inter-device connections. There are locations for 12 plane-committed electrolytic capacitors. **Methode Electronics, Inc.**, 7447 W. Wilson Ave., Chicago, IL 60656. **Write 137**

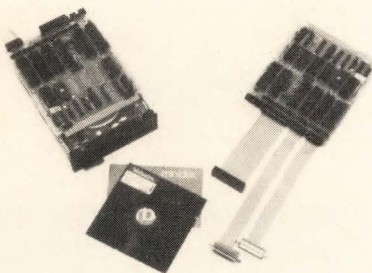
5 OUTPUT SWITCHING POWER SUPPLY

5 DC Output Voltages

The model M7935 is a 240W power supply with 5 DC output voltages. The output, 5VDC at 15 A; +12VDC at 4A; +15VDC at 2A; -15VDC at 2A and +28VDC at 2A are developed using CEAG's modular construction system.

The input voltage is 115VAC at 400Hz. The operating temperatures are -40°C to +85°C; maximum cold plate temp of +75°C using conduction cooling. The size is 10.00" x 8" x 2 1/2" high and weight is 9 pounds. Its packaging density is 5 W/in³ and it is 75% efficient.

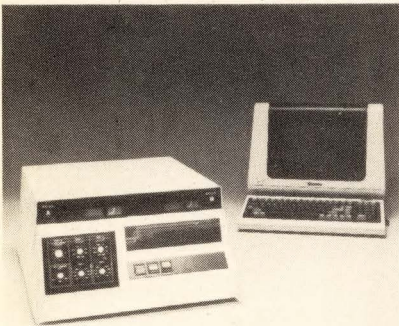
Model M7935 uses as its main rail the 5V output, and the auxillary outputs achieve high efficiency and synchronization to the main rail through the use of a magnetic amplifier post regulated module. There are no high power switching or linear pass transistors used. The unit is manufactured to MIL-T-28800B and MIL-STD-454. **CEAG Electric Corp.**, 1324 Motor Pkwy, Hauppauge, NY 11788. **Write 210**



BIT-SLICE/MICROCODE DEVELOPMENT STATION

Emulates High-Speed Memory

The STEP-7/FITS Firmware Integration and Test Station, an engineering design tool, supports all microprogrammed designs—bit-slices, high speed controllers and digital signal



processing circuits. In addition, any high-performance μP designs get real-time support (to 36nsec access times) from the memory and ROM emulation capabilities of the STEP FITS. The STEP-7 emulates high-speed memory, controls the target system clock and analyzes the logic state of the target. The station is a single unit supported by a full sized CRT terminal and includes 6 slots (expandable to 10) for memory emulation and logic state analyzer boards. Two floppy disk drives and the CP/M operating system provide the instrument with over 1.5 Mbytes of storage for code files, command files, machine state definitions and an on-line command summary. Price is \$8,500. to \$60,000. **STEP**, 757 N. Pastoria Ave., PO Box 61166, Sunnyvale, CA 94086.

Write 206

HIGH-SPEED DRAM MODULE

For Multibus Systems

A high-density, Multibus-compatible DRAM module with 197 nsec access times and 303-nsec cycle times is offered with up to 512K bytes of on-board RAM, and provides cost-effective, reliable memory expansion for all Intel iSBC80 and iSBC86 systems. Moreover, it is designed to allow even denser on-board memory—it can be upgraded to 2 Mbytes using compatible 256K DRAM chips, when these become available. The TMM40020 operates in an address space of up to 16MB and supports word transfers, as well as high, swap, and low-byte transfers. The lower and upper memory addresses are independently se-

lectable in 4K-byte sections. It features a control-status register with selectable I/O address. Other features include LEDs which indicate an error, as well as the bank of the failing DRAM chip. The module also permits the use of a battery backup and ROM overlay. Price is \$925-\$1795.

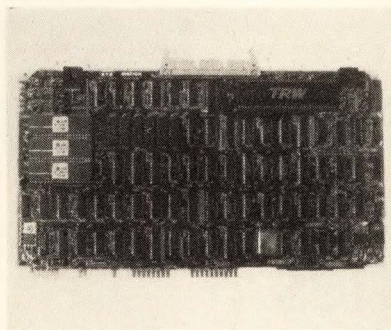
Texas Instruments Semiconductor Group, Literature Response Ctr. (SC-404) P.O. Box 401560, Dallas, TX 75240.

Write 207

VIDEO DIGITIZER BOARDS

Includes Hardware Vector Generator

The VAF-512 and QVAF-512 cards are designed to work with the existing Matrox RGB-GRAPH and QRGB-GRAPH frame buffers to provide a complete Multibus or Q-bus 512 $\times$ 512 $\times$ 8 bit imaging system. The VAF-512 board provides two features

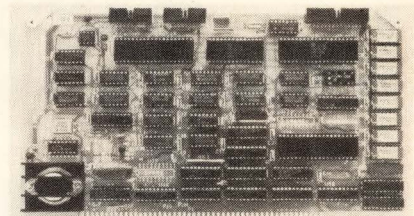


over the video I/O conversion. A high speed (800 sec pixel) hardware vector generator is provided for drawing graphics in the frame buffer memory. The VAF-512 contains an on-board 10MHz A/D flash converter for "grabbing" entire fields of video data with a spatial resolution of 512 $\times$ 512 dots. A contrast control circuit allows the user to focus the digitizing range of the A/D converter to that part of the vde signal which contains most of the useful information. The VAF-512 also contains an on-board hardware vector generator. Price is \$2150. **Matrox**, 5800 Andover Ave., T.M.R., Que., H4T 1H4, Canada. Write 142

S-100 SLAVE

Available In Four Versions

The CPS-MX features memory transfer rates of 517 Kbytes/sec, DMA, memory mapping and host to slave requests via interrupt control. Fully compatible with Turbo-DOS, the slaves are available in four versions, synchronous or asynchronous serial



port, 4MHz or 6MHz. The CPS-MX also allows the bus master to utilize slave memory at the user's discretion. part, 4MHz or 6MHz. The CPS-MX also allows the bus master to utilize slave memory at the user's discretion. The slave then acts as a 65K RAM card. The CPS-MX integrates with Intercontinental's line of S-100 products: CPZ-48000SBC with 64K on board RAM, 4 I/O channels, memory management; on board floppy controller, DMA and vectored priority interrupts; and 256K bank selectable or contiguous memory. A complete line of personality boards allows interface to a wide body of peripherals. Price is \$475.00. **Intercontinental Micro Systems**, 1733 S. Douglass Rd., Anaheim, CA 92806.

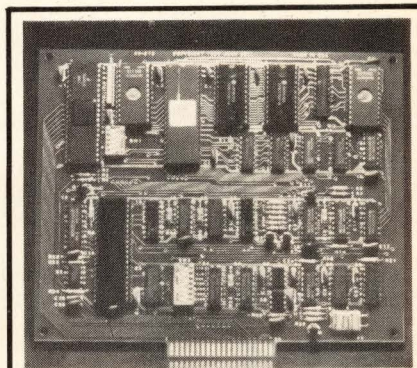
Write 194

RANDOM ACCESS MEMORY

Buffer Storage Applications

The 1024-bit Random Access Memory is organized as 1024 words by 1 bit. Called the MCM10415/10415A, it is designed with a separate data in line, a non-inverting data output and an active-low chip select. **Motorola**, P.O. Box 20912, Phoenix, AZ 85036.

Write 197



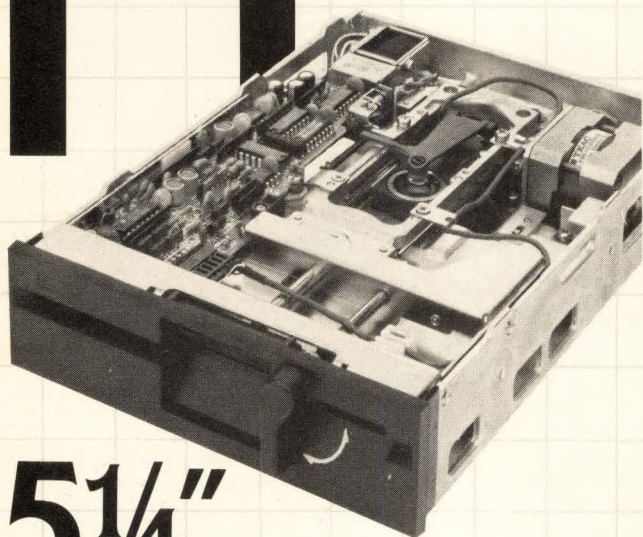
VIDEO TERMINAL BOARD

This board uses a 6502 Microprocessor and a 6545-1 CRT controller. It displays 80 columns by 25 lines of UPPER and lower case characters. Data is transferred by RS232 at rates of 110 baud to 9600 baud. Assembled and tested #82-018A \$199.95 We have a complete line of Industrial Control Products. OEM Pricing Available.

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(415) 592-8411

Write 62 on Reader Inquiry Card

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DC + 5V $\pm 5\%$ 0.5A typical, 0.7A max.

Phone, write or wire TEAC Corporation of America for complete technical data, price and delivery.

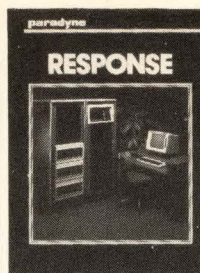


TEAC Corporation of America
Industrial Products Division
7733 Telegraph Road
Montebello, CA 90640
213/726-0303

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MP82501M

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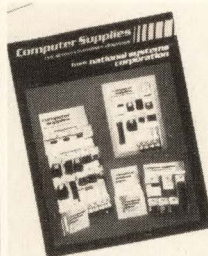
New Literature



Response System Brochure. The pamphlet describes RESPONSE, an information processing system which provides data entry, word processing, data base management, and distributed data processing at remote sites. The system allows network communication to continue when the host CPU is down and is designed for business applications. All peripherals and terminals appear as locally attached devices to any processor in the network.

Paradyne

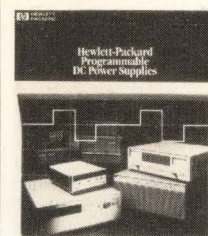
Write 263



Computer Supplies. The 4-page brochure describes retail merchandiser displays and starter packs of computer supplies. The merchandisers require no computer expertise by the sales personnel. All displays include restocking information.

National Systems Corp.

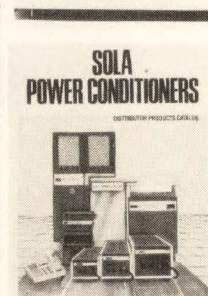
Write 262



DC Power Supplies. Different types of HP-IB (IEEE-488) power supplies are highlighted in the brochure which features products for the automatic test-system designer. It is a guide for selecting HP-IB power supplies, which are organized into three major categories: general-purpose, precision, and bipolar-system supplies.

Hewlett Packard

Write 255

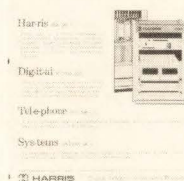


New Power Conditioners Catalog. The catalog features power conditioners intended to guard voltage-sensitive equipment, including micro/minicomputers, POS and data terminals, process control systems and mainframe computers. Voltage transformers offer voltage regulation and two types of Solatron/Acuvoilt Line Conditioners are also described.

Sola Electric

Write 257

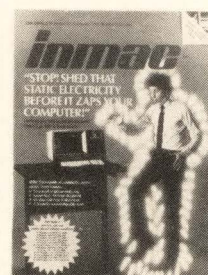
The Profitable Resale Telephone Network, Defined.



Telephone Network Brochure. The pamphlet details de-regulation in the telecommunications industry which now permits entrepreneurs, interconnect companies, the hotel industry, and others to profitably re-sell the services of common carriers, satellite networks, AT&T, and others. The publication highlights features of tandem switching systems, automatic route selection and station message accounting.

Harris Corp.

Write 260



Computer Accessory Catalog. The product/manufacture catalog contains products, price reductions, and editorials on computer products and maintenance. Featured are two security devices; Inmac's new Station II for Apple II computers, and a locking diskette file for floppies as well as business accounting forms in continuous feed mini-packs.

Inmac

Write 259

IC Packaging Systems Catalog. A 28 page catalog detailing Multibus compatible IC packaging systems includes 11 card rack sizes for packaging up to 26 boards, and sideplate kits for mounting racks into cabinets. New Multibus backplane features are GND/GND/GND bus lines and resistors of equal value at both ends of the busses. Data sheets contain information on accessory items.

Mupac

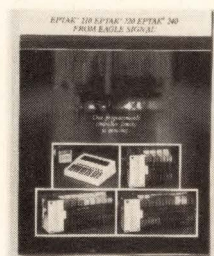
Write 266



μP-Based Programmable Controllers. The brochure gives benefits, application information and specifications for three EPTAK PCs, the EPTAK 210, 220 and 240. There is a portable programmer common to all three models that retains programs for 10 years without an external power source, has I/O tracks, I/O modules and a DAD/M.

Eagle Signal Controls

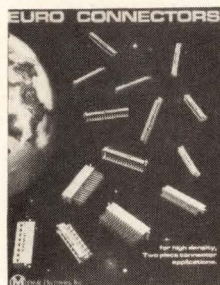
Write 254



Euro-Connector Catalog. Methode Electronics, Inc., describes the firm's line of Din-41612 Euro-connectors in a 12-page catalog. DIN-41612 types R, B, C, D, F, G, and H on .100" (2.54 mm) centers with 2, 3, and 4 row pin and socket configurations are presented with specifications, dimensional drawings and application data. Featured in the catalog is the new type "R (inverted)" version for backplanes and pressfit applications.

Methode Electronics Inc.

Write 253



Laboratory Tape System. Honeywell Test Instruments high density digital laboratory tape system, HD-96, is detailed in a brochure containing diagrams of its capstan drive and illustrations of components. Also covered are the panel and transport controls and indicators, record/reproduce heads, reproduce amplifier/bit synchronizer, and balanced tension transport.

Honeywell

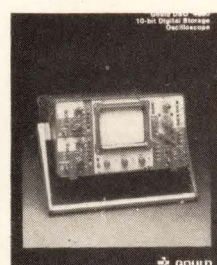
Write 252



Digital Storage Bulletin. The subject of this eight-page bulletin from Gould Inc. is a dual-trace digital storage oscilloscope. Features include 25% pre-trigger viewing, split-trace facility, maximum sensitivity of 100 uV/cm, and high vertical and horizontal resolution via a 10-bit × 4K store. The scope is capable of selecting stored waveform portions and expanding them to X10 vertically and X50 horizontally.

Gould Inc.

Write 251



Communications Systems Brochure. The RCS-10 Nurse Call Communications System is explained in a 6-page brochure from Bunting. The RCS-10 addresses, scans, receives, stores, displays and transmits information throughout the hospital. Included are automatic staff locators which emit an inaudible high frequency signal that allows the central console operator to scan and locate the entire nursing staff.

Bunting Inc.

Write 250



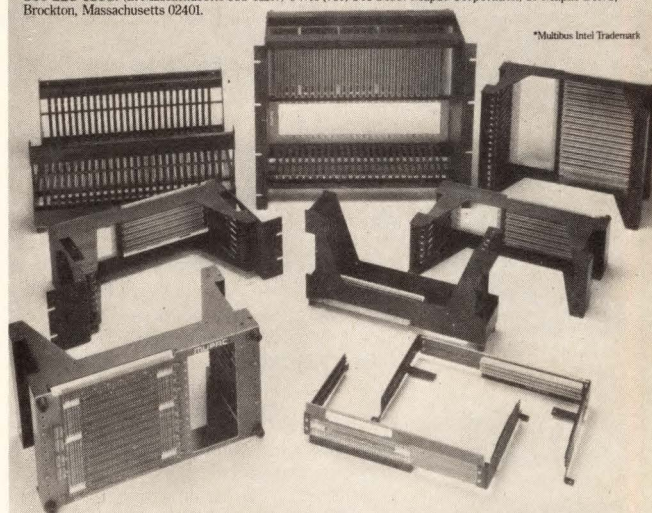
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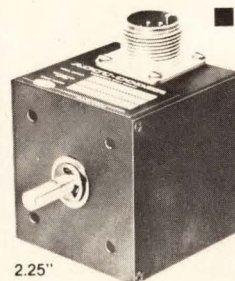
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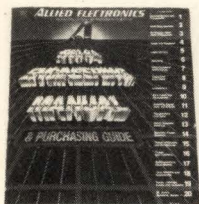
TWX 510-776-1595

Write 65 on Reader Inquiry Card



DEC Terminal Brochure. The pamphlet provides specifications on the ANSI-conforming terminal and uses full-color product photography and schematic art. It describes features of the AVT Terminal which include four pages of memory standard, 43 programmable functions, switchable 80/132-column format; windowing, and multiple computer capabilities.

Human Designed Systems Write 273



Engineering Manual and Purchasing Guide. Allied Electronics' edition is a guide for anyone who uses or specifies electronic parts. Its 320 pages include "best values" throughout the book on lines of components. It contains illustrations, dimensions, technical data and specifications, descriptions and prices (as well as bulk pricing for large-quantity buyers).

Allied Electronics Write 272



Computer Graphics Pamphlet. The brochure describes computer graphics services in the mechanical design field. Listed are applications such as machine design and numerical control, product design, HVAC systems, instrumentation, and plant layout. Included are examples of experiences in software development. Additional examples include 2-D to 3-D conversions and generation of parts lists and bills of materials from drawings.

Minigraph, Inc.

Write 271



Short Form Catalog. The 12-page illustrated catalog covers MICOM's data communications equipment. The booklet includes brief descriptions of most product lines—data concentrators, data PABXs, local networking equipment, modems, multiplexors, and local datasets, as well as complete U.S. pricing for all currently-available products.

MICOM Systems, Inc.

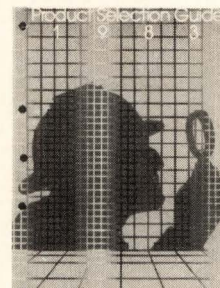
Write 258



IC Publications. Four publications are available to assist the design engineer in developing gate array and semi-custom ISO-CMOS or silicon-on-sapphire LSI circuits. The literature presents an analysis and description of the various routes available to the designer. If desired, CTI will design, verify, fabricate, test and deliver a packaged IC to MIL-STD-883B. The customer can supply "black box" requirements or his own created logic.

Circuit Tech. Inc.

Write 265



1983 Product Selection Guide. The catalog includes basic specifications and performance data for standard PMI products. The reference guide contains information about the following product groups: operational amplifiers, voltage comparators and PCM repeater amplifiers. Additionally, selection charts show the matrices of primary characteristics of operational amplifiers and digital-to-analog converters.

Precision Monolithics

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SRM2017C15	2Kx8	150ns	50μA	35mA	5V
SRM2018C15	2Kx8	150ns	50μA	35mA	5V
SRM2016C20	2Kx8	200ns	100μA	35mA	5V
SRM2017C20	2Kx8	200ns	100μA	35mA	5V
SRM2018C20	2Kx8	200ns	100μA	35mA	5V
SRM2016C25	2Kx8	250ns	100μA	35mA	5V
SRM2017C25	2Kx8	250ns	100μA	35mA	5V
SRM2018C25	2Kx8	250ns	100μA	35mA	5V

Get the best of both worlds — CMOS power at near NMOS speeds. And get the total commitment to quality that has made the name of Epson a byword for performance and reliability around the world.

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