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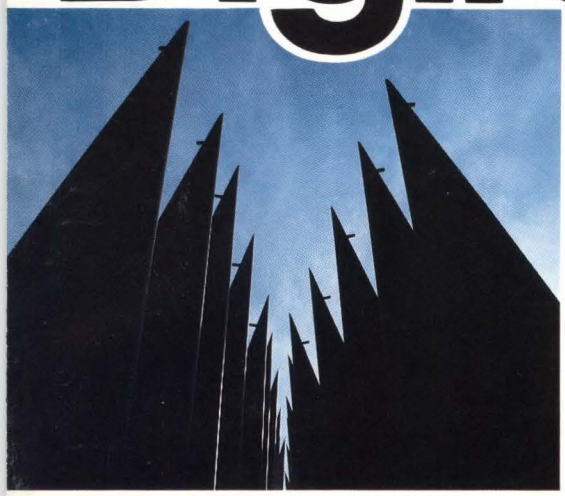
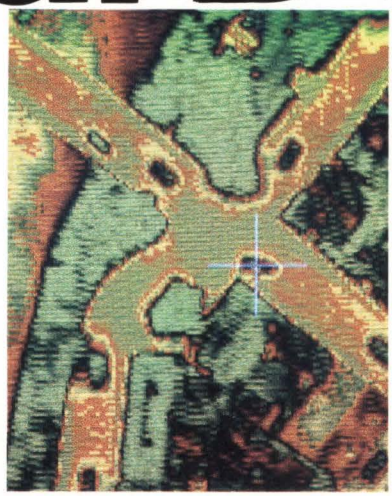
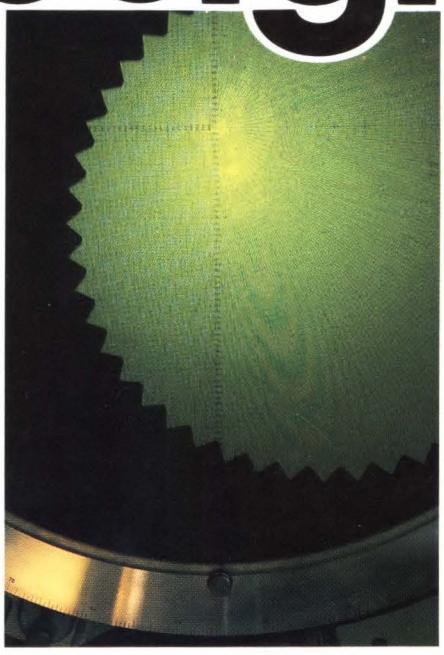
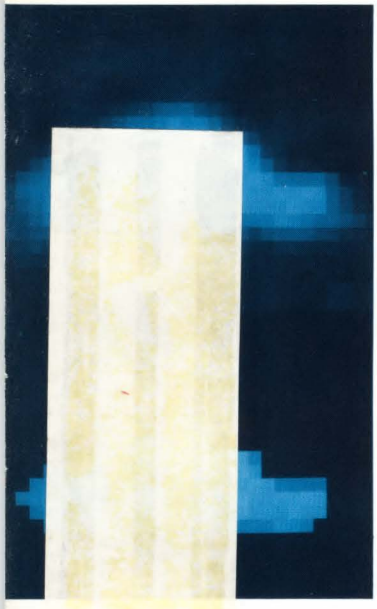
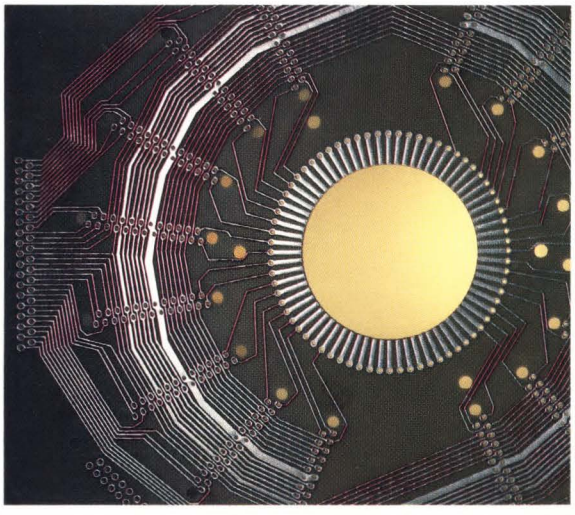
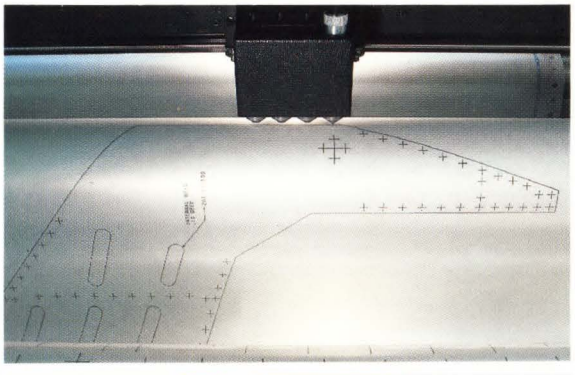


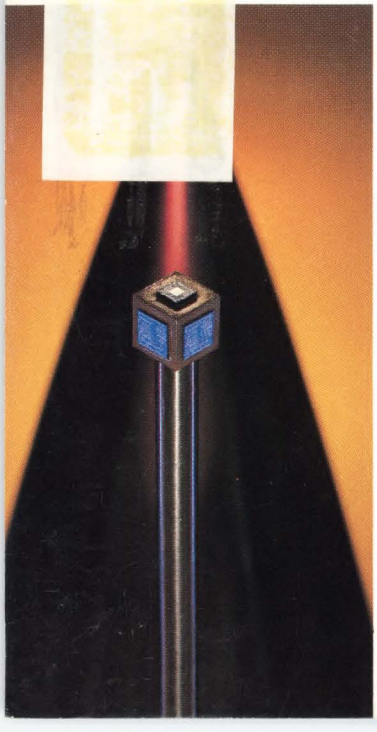












Industry Spotlight

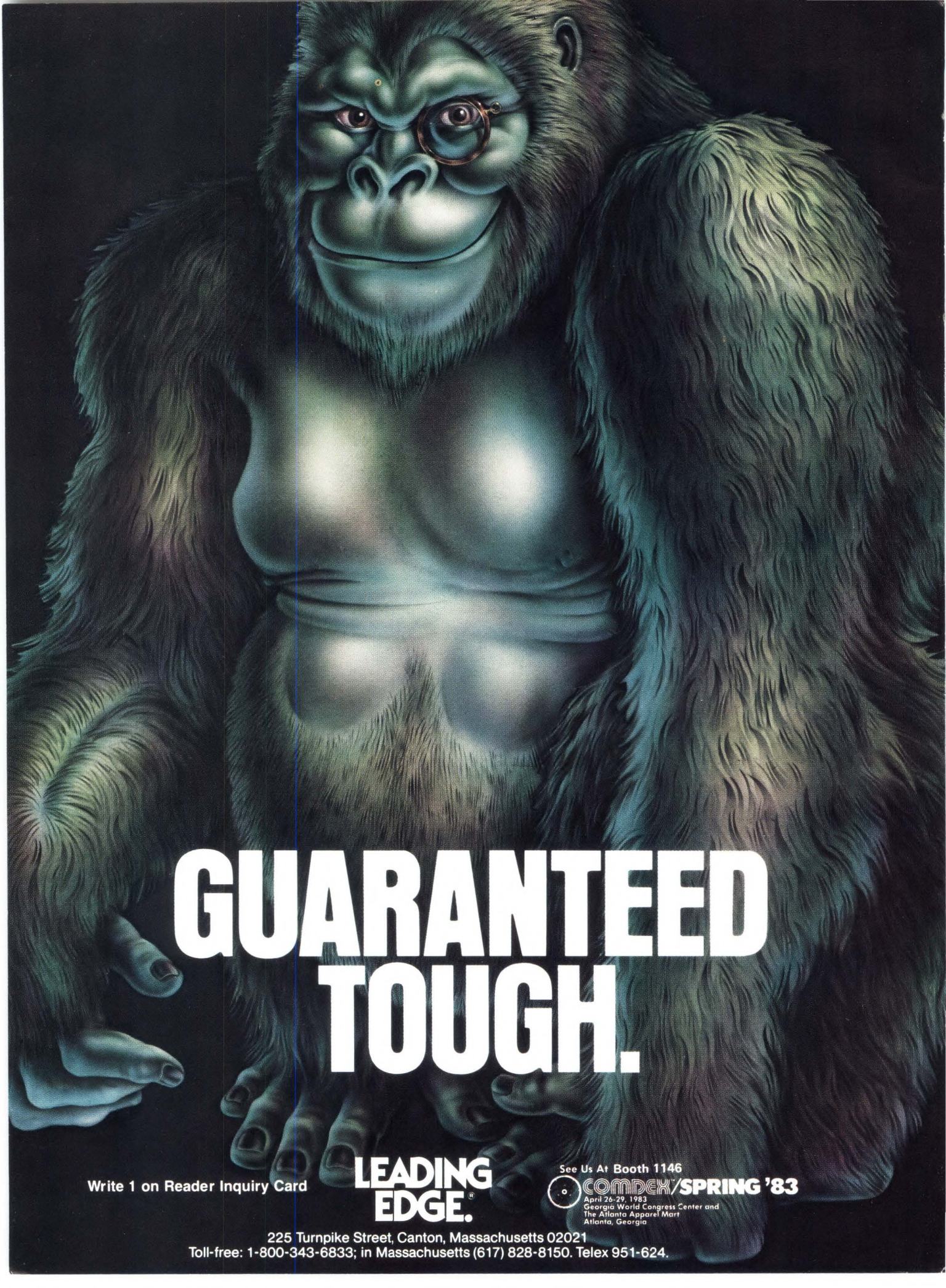
Admiral Jon L. Boyes on

Military Electronics

- Keyboard Design
- Array Processors
- Data Acquisition
- RAM Refreshing

COMPUTERS/SYSTEMS · PERIPHERALS · COMPONENTS · 4/83

VOL. 13
NO. 4



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"Racal-Vadic's Invisible Modem Gives Grid's Ultra-Portable Computer Access to a Whole World of Data!"

Dave Hanna — V.P. Marketing and Sales, Grid Systems, Inc., Palo Alto, California

One of the hottest personal computers on the market is the new Grid Compass. It weighs about 10 pounds and takes up less than half of a standard briefcase.

Business Week calls Compass "a Porsche for top executives."

A custom Racal-Vadic modem is behind the smashing success of Compass. This VS212A/103 modem — complete with auto dial and auto answer — is built on a 6" by 6" PC board. "Without this built-in modem we couldn't have made the product," says Glenn Edens, V.P. of Development for Grid Systems, Inc., Palo Alto, California.

Racal-Vadic's incredibly small modem is vital because it gives Compass a unique communication capability, setting it apart from other portable computers. For example, Compass can "talk" to another Compass... or to Compass Central, a user-owned, 240 Mbyte desk-top computer, which is designed to support a number of Compass computers in the field. It can also access Grid Central, a Grid-owned mainframe which distributes new software and provides data storage for its users. And there's more! The ultra-portable Compass can access corporate mainframes and public data bases.

Imagine... a Fortune 500 executive in a hotel room with the whole wide world of data at his or her fingertips — using the dial-up telephone.

Why Racal-Vadic? Because we invented 1200 bps full-duplex technology. Because we ship more modems than anyone. Because we utilize the most advanced automated production equipment and superb quality control. And because our custom modem department is dedicated to creating integral modems for OEMs.

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The black facts about c

Fact 1.
Software development is expensive.

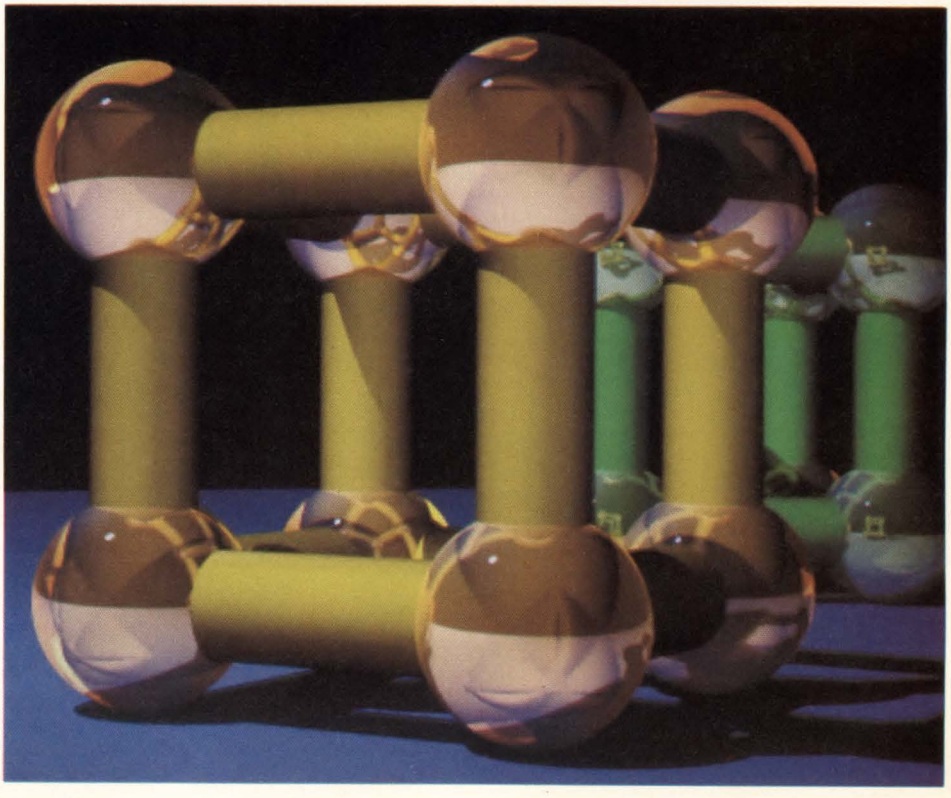
Raster Technologies' Model One graphics systems feature software tools that speed application development. Like an integrated local debugger. Command stream translator. Local command execution. A complete HELP facility. And truly easy to use macro programming. These unmatched software tools save you time and money.

Fact 2.
Software redevelopment is even more expensive.

With Raster Technologies' fully compatible Model One family, you can take advantage of the latest hardware without any software rewrites. This means an easy upgrade to a more powerful product while still using the same graphic commands, program development tools and host library. So the application developed for the best hardware today can run on the best hardware tomorrow. Without modification.

Fact 3.
Performance is a lot more than good specs.

Graphics performance goes beyond pixel and vector timing specs. It is the ability to display a complex picture without having to wait. Provide instantaneous interaction between an application program and its user. And efficiently communicate with a host computer. The kind of total graphics performance you should measure before you buy.



and white olor graphics.

Fact 4.

Graphics applications demand flexibility.

The Model One family from Raster Technologies offers maximum flexibility at the lowest cost. Because it lets the user select the combinations of display resolution, color and refresh rates that are right for that particular application. Factors that are different for every application.

Fact 5.

Graphics technology is moving fast.

Raster Technologies is dedicated to one business: graphics. All our development efforts focus on advancing graphics technologies. With the latest microcircuitry. The newest and fastest microprocessors. The most advanced display list architectures. And the most innovative pipelined multiple processor designs. All to advance graphics capabilities compatibly. And keep today's customers with us tomorrow.

Fact 6.

You should benchmark the Model One.

All three Model One graphics systems – the Model One/25, Model One/40 and Model One/60 – offer the best software development tools. Total compatibility to eliminate software redevelopment problems. Total systems performance. Maximum flexibility. And a dedication to the graphics business.

The Model One/25 features vivid full color imaging performance with 512 x 512 resolution. The Model One/40 features ultra high 1024 x 1024 resolution. The Model One/60 features 100% flicker-free 60 Hz non-interlaced display with 768 x 576 resolution. All support our Advanced Graphics Application Development Firmware and powerful display list package.

Put the Model One family to the test.

Raster Technologies

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High speed data acquisition can be a real headache. Especially during peak I/O rates when transfer can exceed the CPU's capacity and key bits of information go off in thin air.

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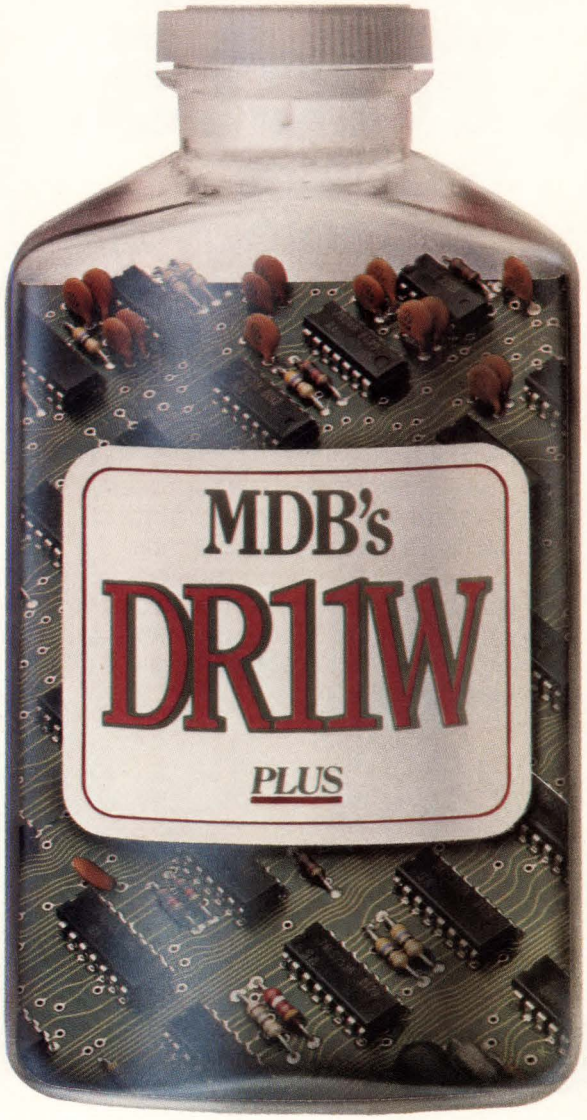
- Micro-sequencer driven, self-test diagnostics
- Long lines capability
- Switch selectable 22-bit addressing (Q-Bus)



- Bus Address Extension for memory transfer throughout the 4 megabyte range (Q-Bus)
- Switch selectable, 4-level or single level interrupt arbitration (Q-Bus)
- Compatibility with 16, 18 and 22-bit backplanes (Q-Bus)

This high speed, digital input/output device is prescribed for such typical applications as:

- High speed graphics
- Digital data acquisition
- Parallel information processing
- Interprocessor linking between a Unibus and Q-Bus

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APRIL 1983/VOL. 13, NO. 4

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p. 28 *(photo courtesy Motorola)*

p. 44
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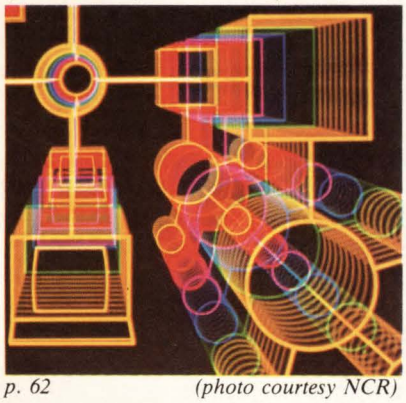

p. 62 *(photo courtesy NCR)*

Cover

Increases in government spending have spurred unprecedented interest in military electronics. This month's Industry Spotlight (p. 28) examines this growing field and its significance to the system designer. Cover illustration courtesy of Northrup, Electro-Mechanical Div., 500 E. Orangethorpe Ave., Anaheim, CA 92804.

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COMPUTERS/SYSTEMS

Industry Spotlight: Technologies and Trends Affecting The Military Computer Market 28
Incorporating state-of-the-art commercial systems into the Defense Department is of primary concern to the military computer field.

Real Time Graphics With An Array Processor 51
To operate in real time a combination of specialized graphics with high speed pipelined processor is required.

FIFO Buffers Insure Continuous Array Processor Performance 56
Today's array processors achieve high performance through the use of multiple processing elements.

CP/M '83 And Unicom Highlights 62
A trend toward stability is good news for software developers.

STD System Cuts Software Costs 74
The Approach Series of STD Development Systems cuts cost and aids development.

Graphics System Design..... 101
Stand Alone Systems Ease IC Design

Innovative Design 102
New Hardware Supports Enhanced Multibus Architecture

Technology Trends..... 23
Gould's SuperMini

PERIPHERALS

RFI/EMI Shielding Scheme For FTM Keyboard..... 44
FTM offers low cost solutions to the problems of both emitted and received energy.

Technology Trends..... 23
Half-Height Drives • Microfloppy Standards • The Bubble Drive

COMPONENTS

Building A Data Acquisition System From Board Level 66
Analog interface is the key obstacle to successful factory automation.

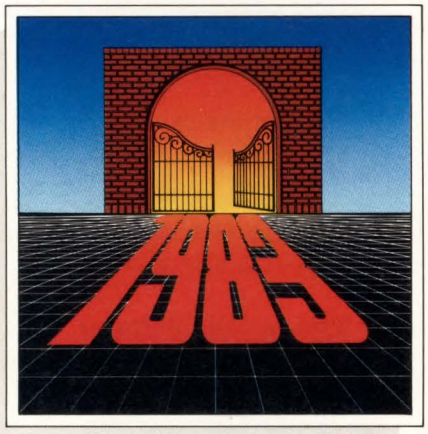
New Concepts In Dynamic And Static Memory Cell Storage 78
This article examines memory refresh options and their implementation.

Graphics Chip Makes Low-Cost, High Resolution Color Displays Possible 84
Intelligent peripheral ICs offload processing tasks from the CPU.

Applications Notebook..... 42
7-1 Communications Line Multiplexer

Calendar..... 12
News Update..... 14
Market Trends..... 18
Product Index..... 96
Reader Service 97
New Products..... 104
New Literature 114
Advertiser Index 116

THE CROWNING OF MISS UNIVERSAL LAUNCHES A BANNER YEAR FOR HIGH SPEED CMOS GATE ARRAYS!



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Lundy's 5484 color raster design workstation.

Currently, our terminals can be driven by many of the leading software products. And the list is growing rapidly. Because Lundy is committed to an aggressive third-party software development program to provide the most comprehensive application packages.

Lundy will help you see more in graphics.

When you look at our 5480 Series, take a close look at Lundy, too. We're a company that's as good as its products.

A company that balances high tech with solid business sense.

A company as proud of its service (one of the largest service organizations in the industry—39 locations nationwide) as its engineering expertise.

A company you can count on to help you see more in graphics—and get more out of graphics—both now and in the long term.

For more information, write Lundy, Glen Head, New York 11545, or call: (516) 671-9000.

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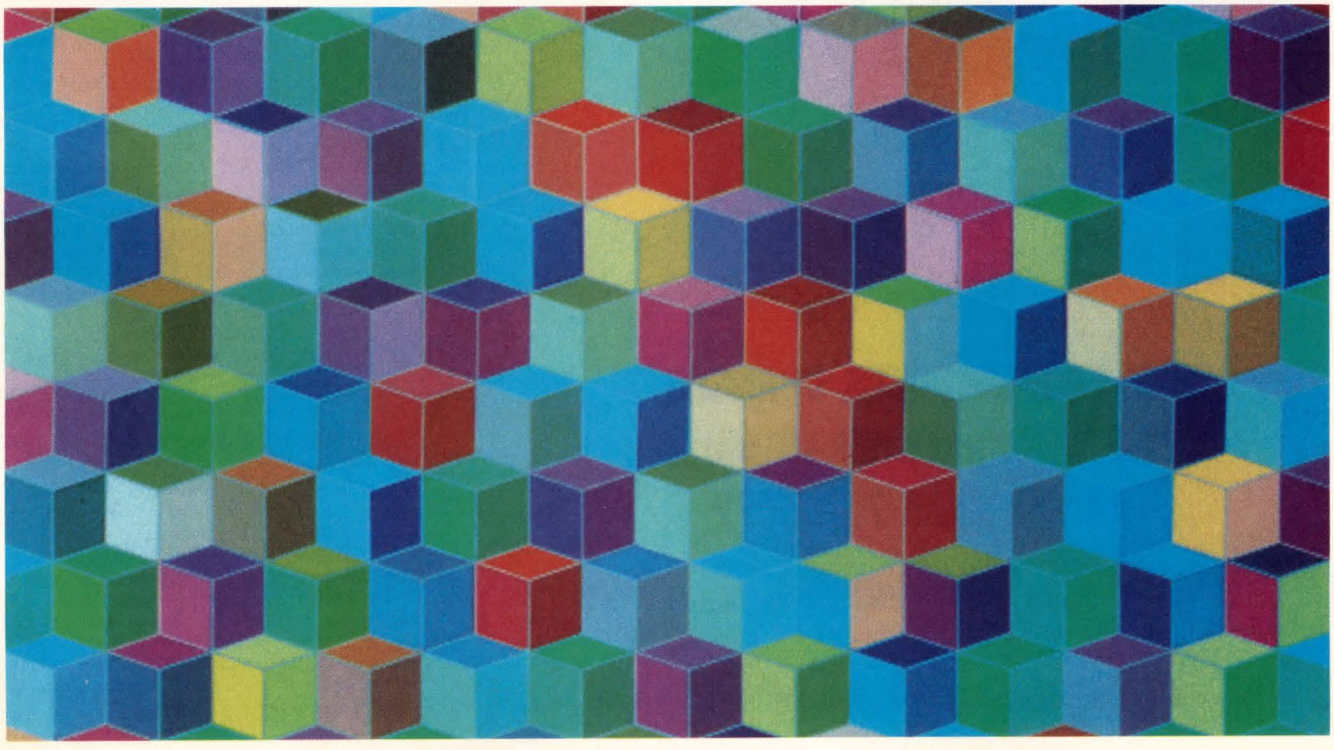
The Lundy 5688 displays 256 high resolution colors at a time. User downloadable character fonts; programmable character sizes.



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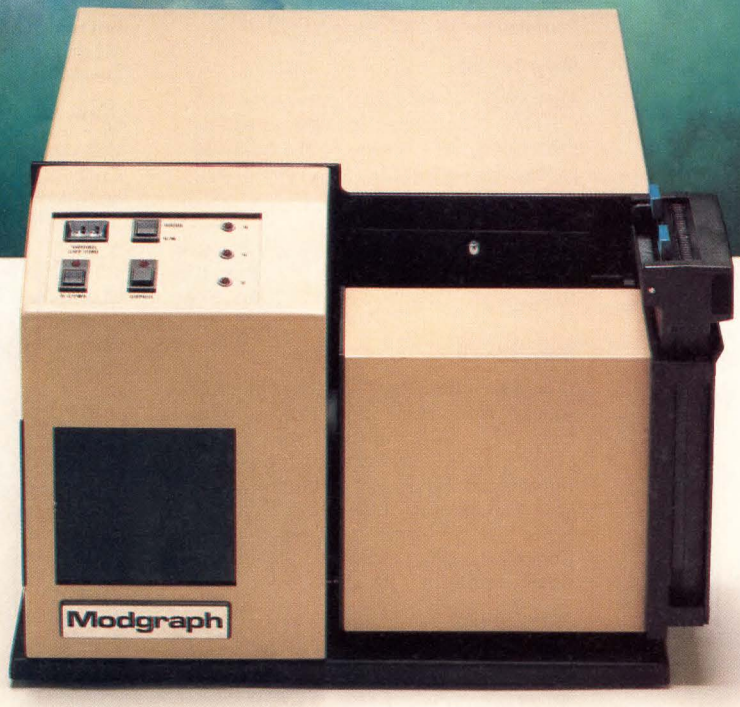

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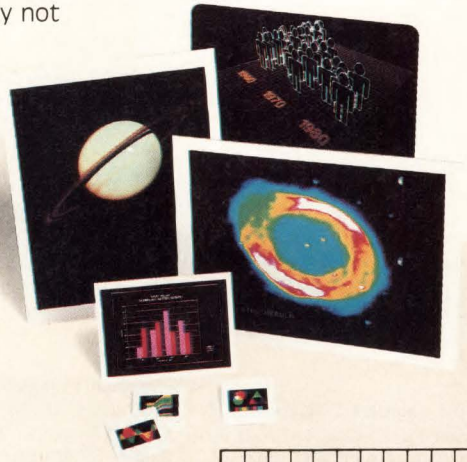
Our color cameras produce the best 35 mm slides, SX-70 Polaroids® 4 x 5 or 8 x 10 color prints...You be the judge. Drop us a line, or give us a call. We'll arrange for a demonstration and show you how the best image quality can be yours.



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Calendar

May 1–3

Document-Based Optical Mass Memory Systems. Highlands Inn, Carmel, CA. Contact: Institute for Graphic Communication, 375 Commonwealth Ave., Boston, MA 02115. (617) 267-9425.

May 3–6

Unix Workshop. Human Computing Resource Offices, Ontario, Canada. Contact: HCR, 10 St. Mary St., Toronto, Ontario. M4Y IP9 Canada. (416) 922-1937.

May 4–6

Rocky Mountain Data Processing Expo. Currigan Hall, Denver, CO. Contact: Industrial Presentations West, 3090 S. Jamaica Court, Suite 304, Aurora, CO 80014. (303) 696-6100.

May 9–11

VLSI Design. A Structured Approach to Custom IC Design. Boston, MA. Contact: Hellman Associates, Inc., 299 S. California Ave., Palo Alto, CA. 94306. (415) 328-4091.

May 9–11

MVS/XA, IBM 308x Seminar. Hyatt Regency, San Francisco, CA. Hyatt Arlington, May 23–25. Contact: TTI, 741 10th St., Santa Monica, CA 90402. (213) 394-8305.

May 9–13

Graphics Interface '83. Edmonton, Canada. Contact: Graphics Interface '83, CIPS Edmonton, PO Box 1881, Edmonton, Alberta, Canada T5J 2P3. (403) 427-9416.

May 10–12

Northcon/'83 and Mini/Micro-Northwest/'83. Portland, OR. Contact: Electronic Conventions, Inc., Worldway Postal Center, PO Box 92275, Los Angeles, CA 90009. (800) 421-6816.

May 10–12

International Computer Show. Salon International de l'Ordinateur, Velodrome, Montreal, Canada. Contact: Jim Steinhart, Media Consultant, 559 Deloraine Ave., Toronto M5M 2C5. (416) 787-2138.

May 12–13

Dataplot. Academic Center, Washington, DC. Contact: Continuing Engineering Education Program, George Washington University, Washington, DC 20052. (202) 676-6106.

May 16–18

Electronic Components Conference. Orlando, FL. Contact: Electronic Industries Association, 2001 Eye St. NW, Washington, DC 20006.

May 16–19

NCC '83. National Computer Conference. Anaheim and Disneyland Hotel Convention Centers. Contact: American Federation of Information Processing Societies, Inc., 1815 N. Lynn St., Arlington, VA 22209. (703) 558-3612.

May 16–30

Intel Microcomputer Workshops. Various locations. Contact: Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051.

May 17–20

Engineering Seminar. Gaithersburg, MD. Contact: R. Hocken, B104 Metrology Building, National Bureau of Standards, Washington, DC 20234. (301) 921-2577.

May 18–20

Man-Machine Interface. Palo Alto, CA. Contact: Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Treader Way, Columbia, MD. (301) 596-0111.

May 22–25

PACS II. Alameda Plaza Hotel, Kansas City, MO. Contact: SPIE, P.O. Box 10, Bellingham, WA 98227-0010. (206) 679-3290.

May 23–25

Computer Hardware Description Languages And Their Applications. Pittsburgh, PA. Sixth International Symposium. Contact: Takao Uehara, Information Processing Laboratory, Fujisitso Laboratories LTD., 1014 Kawasaki, Japan 211 or Mario Barbacci, Dept. of Computer Science, Carnegie-Mellon University, Pittsburgh, PA 15213.

May 24–26

SME Exhibition. Fort Worth, TX. Contact: SME, One SME Drive, Dearborn, MI 48128. (313) 271-1500.

May 24–26

PC Conference. New York Hilton, NYC, NY. Contact: Morgan Grampian, 2 Park Ave., NYC, NY 10016. (212) 340-9780.

May 24–27

Image Processing Course. Philadelphia, PA. Contact: Integrated Computer Systems, 3304 Pico Blvd., P.O. Box 5339, Santa Monica, CA 90405. (213) 450-2060.

May 24–27

Digital Control System. San Diego, CA. Contact: Integrated Computer Systems, 3304 Pico Blvd., P.O. Box 5339, Santa Monica, CA 90405. (213) 450-2060.

May 31–June 2

CAD/CAM & Robotics. Toronto International Center of Commerce, Toronto, Canada. Contact: Macgregor & Assoc., 662 Queen St., Toronto, Ont., M6JIE5. (416) 363-2201.

June 2

Personal Computer Workshop. Charlotte, NC, June 16–18, Reston, VA. Contact: CEC, Virginia Tech., Blacksburg, VA 24061. (703) 961-4848.

June 6, 7

IC Processing Techniques & Ion Implantation. Hyatt Palo Alto, Palo Alto, CA. Contact: Dept. 564 N, U of C Ext., 2223 Fulton St., Berkeley, CA 94720. (415) 642-4151.

June 6–10

Optical Storage Conference. Arlington, VA. Contact: SPIE, P.O. Box 10, Bellingham, WA 98227. (206) 676-3290.

June 6–8

Intermexpo. Monterrey, Nuevo Leon, Mexico. Contact: SME, One SME Drive, Dearborn, MI 48121. (313) 271-0023.

June 6–10

Cell Designer Course. Melbourne, FL. Contact: Harris Corp., P.O. Box 883, Semiconductor Group, Melbourne, FL 32901. (305) 724-7800.

June 6–12

Microprocessor Application Course. MIT, Cambridge, MA. Contact: MIT, 105 Mass. Ave., Cambridge, MA 02139. (617) 253-7406.

June 7–9

Industrial Exposition. Milwaukee Exposition Ctr., Milwaukee, WI. Contact: SME, One SME Drive, Dearborn, MI 48128. (313) 271-0023.

June 7–10

Network Design Course. Washington, D.C. Contact: ICS, 3304 Pico Blvd., Santa Monica, CA 90405. (213) 450-2060.

June 8–10

X.25 Seminar. Hyatt Regency Crystal City, Arlington, VA. Contact: TTI, 741 10th St., Santa Monica, CA 90402. (213) 394-8305.

June 9–11

Microcomputer Education Workshop. Watertown, CT. Contact: TERC, 8 Eliot St., Cambridge, MA 02138. (617) 547-3890.

June 13–15

Production Project. Rochester, NY. Contact: The University of Rochester, Rochester, NY 14627. (716) 275-3106.

June 14–16

Ohmcon Exhibition. Cobo Hall, Detroit, MI. Contact: EC, 999 N. Sepulveda Blvd., El Segundo, CA 90245. (213) 772-2965.

June 14–16

Robot Conference. Long Beach Convention Ctr., Long Beach, CA. Contact: TCMC, 143 N. Hale St., Wheaton, IL 60187. (312) 668-8100.

June 14–18

Technology Exhibition. Earls Court Exhibition Ctr., London. Contact: Radcliffe House, Blenheim Ct., Solihull, West Midlands, B912B6. (021) 705-6707.

AYCON 16/SERIES

brings high performance color graphics down to earth.

Only AYDIN CONTROLS' 15 years of experience in raster scan color graphics could bring you a display computer with the total capability of the AYCON 16/SERIES...and now at such an affordable price!

The overwhelming acceptance of the AYDIN original Model 5216 allows us to offer an enhanced version of this field-proven unit. Check this unmatched combination of **systems/hardware features available with the AYCON 16/SERIES:**

- Up to 1024 x 1024 pixel x 16 bit (Z-axis) color display.
- Refresh at up to 60Hz.
- A variety of video modules.
- Characters in three sizes.
- Vectors at 800 ns per pixel.
- 80 x 48 character A/N overlay.
- Multiple 16-bit micro's. AYDIN software or you program them... even up to 14!
- Single or multiple WORK-STATIONS...up to four!
- High-resolution RGB monitors - delta or in-line gun.

And when it comes to Software/ Firmware:

- Graphics Firmware with fill and zoom standard!
- AYGRAF/CORE 2-dimensional Firmware/Software with World-to-Screen translation, rotation, and scaling...world coordinates of 64K x 64K!
- Plus AYGRAF/3D, AYGRAF/ LIST, and support Software.

But if all this is not enough to excite you, how about more economy with standard PACKAGED SYSTEMS, single or multiple WORKSTATION pre-engineered for the most common color display applications?

If you're ready to fly with your color graphics display application, we can help you "get off the ground" with a system to meet your industrial, business, scientific or commerical requirements.

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News Update

3M Will Announce PECOS

3M will announce at the NCC a device called PECOS which will allow its tape drive storage products to emulate and act as a hard drive (and to interface with its hard disk drive product). This will allow for easy access to formatted backup and require only one controller for both devices. Both systems will have the same operating systems and the controller will perform data conversion and error correction.

CADCON '83 Highlights

CADCON '83, the first annual conference on the practices, techniques, and economics of computer-aided technologies was held at the Disneyland Convention Center, Anaheim, CA, January 17–19, 1983. The high-level, 3-day technical program was aimed at industrial engineers, manufacturing engineers, PC designers, VLSI design engineers, and graphics specialists.

Sponsored by the Morgan-Grampian Expositions Group, the Conference included five technical sessions with over 500 participants. The conference was chaired by Carl Machover, an internationally known industry consultant on CAD/CAM. Subject papers discussed included: CAD for architects, engineers and constructors; CAD for PC/IC/VLSI; modular CAD/CAM; CAD Systems and Components; and management issues. Among those directing workshops on various aspects of CAD were Ray Kush of Arthur D. Little, lecturing on "Factory of the Future: Developing a Strategic Manufacturing Plan;" Jerry Borrell, Editor in Chief of Digital Design on Solid Modeling; and Richard Jennings, VP Marketing of VIA Systems on "VLSI Design and Implementation Using CAD/CAM."

Featured Speaker at the Keynote Luncheon, "The Challenge of a Computer-Aided Future," was Ed Zimmerman, former consultant on information handling to the Reagan and Carter Administrations.

According to Robert A. Poggi, Director of the Expositions Group, 3000 attended the show. The Expositions Group will sponsor ATE East 1983 on June 14–16, in Boston, and ATE Central on October 3–6 in Chicago.

Intel Provides Ada Compiler

Intel Corp. announced a new family of computer language translators to compile the Ada high-level language for its iAPX 86 series of 16-bit microprocessors. The new Ada 86 compiler is a specialized tool that simplifies large-scale software development for a variety of applications. The compiler will meet U.S. Department of Defense standards, and will be hosted on VAX minicomputers and on a variety of Intel-based products.

Memorex And DMA Systems Announce Agreement

Memorex Corp. and DMA Systems Corp. announced the signing of an agreement today for joint sponsorship of a family of 5¼″ Winchester disk products to meet the requirements of the OEM market and of Memorex's parent company, Burroughs Corporation. Under the agreement, Memorex acquires a $1.5 million minority interest in DMA Systems.

Merger Agreement

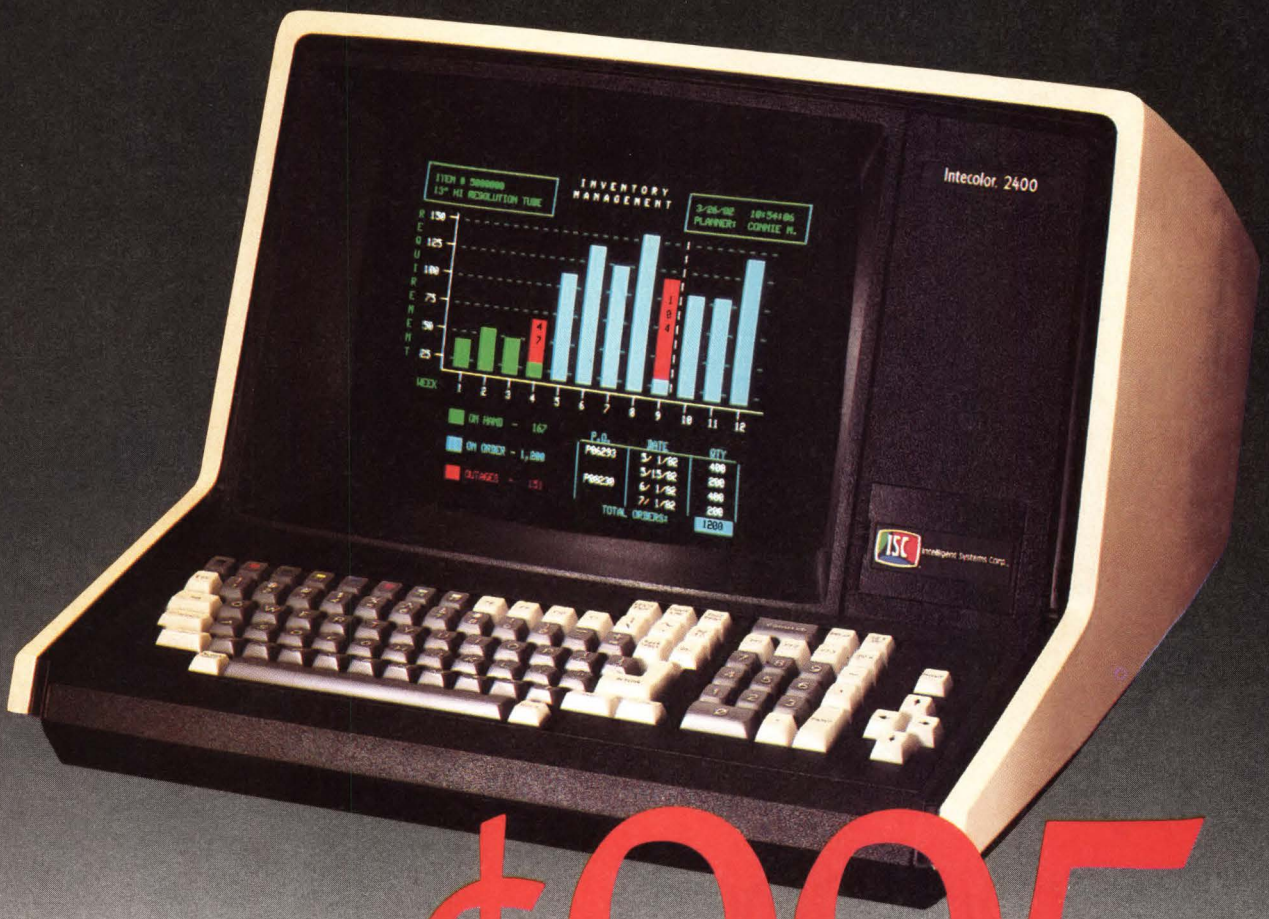
National Semiconductor Corporation and Data Terminal Systems, Inc. (DTS) jointly announced that they have executed a definitive merger agreement providing for the acquisition of DTS by National Semiconductor, in a transaction valued at up to approximately $50 million.

Full 32-Bit μP Available

National's 32032 μP is now available in sample quantities, an indication that extensions to the family are arriving on schedule. The part has a 32-bit data bus and boasts a 40% improvement in performance over the 16032. It supplies ECC bus handling and is capable of high speed parallel processing.

Digital Reduces Microcomputer Prices

Digital Equipment Corporation announced price reductions of up to 36% for its LSI-11/23 CPU boards and up to 18% for its PDP-11/23 PLUS packaged CPU ("boxed") assemblies. The new prices, which are effective immediately, cover two board-level microcomputer products and four box-level assemblies.



$995

Our ANSI X3.64 terminal has all the VT100 features you'll ever need in a conversational terminal. Plus color and vector graphics.

Special offer. Immediate delivery.

The logical switch to color has never cost less. Now you can buy an Intecolor 2405 single evaluation unit at the 100-piece price of $995 (U.S. domestic only). You get the advantage of vector graphics on an 80 column by 24 line screen, without sacrificing the most important capabilities you want from a VT100 terminal. Plus, the 2405's vibrant color conveys more information, more quickly and with greater comprehension than monochrome.

ANSI X3.64 system compatibility. The 2405 is the ideal replacement or add-on terminal. Highly compatible with VT100 and numerous other ANSI X3.64 terminals, the 2405 is easily integrated into any ANSI X3.64 environment. It also includes ASCII codes and a VT52 mode.

With all the features you need. Eight foreground and eight background colors. Terminal based vector graphics. Data transmission baud rates from 50 to 19,200. English language menu set-up mode. Non-volatile set-up memory. *Two* full pages of screen RAM. In-line CRT. Auto degaussing. Powerful, 6 MHz 8085 microprocessor with four hardware interrupts. Plus, up to 72 function key definitions, optional.

Introductory price good through May 31, 1983. After that, our regular single-piece price of $1195 goes into effect. So act now. Take full advantage of the color, vector graphics and flexibility of the Intecolor 2405—at the 100-piece price. Once you do, we're confident that you'll enthusiastically agree with the growing number of OEMs and users who are making it dramatically clear that, "The future belongs to color!"

For the name of the distributor or sales representative in your area, or for complete specs, ask about our $995 special:
Call 404/449-5961.

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Intecolor Drive, 225 Technology Park, Norcross, GA 30092, TWX 810-766-1581

News Update

$100 Million Merger

Sensormatic Electronics Corporation and MSI Data Corporation announced an agreement in principle for Sensormatic to acquire MSI through a merger for approximately $100 million. The agreement provides for the exchange of nine-tenths of one share of Sensormatic common stock for each common share of MSI, but in no event will the value of the Sensormatic stock exchanged per MSI share be less than $35 or greater than $50.

Floating Point Systems To Support Apollo DOMAIN

Floating Point Systems and Apollo Computer announced that the Apollo DOMAIN will be supported as a host for the FPS-164 Attached Processor. Availability is scheduled for July, 1983, from Floating Point Systems. Support will include software and hardware interfaces, as well as Floating Point Systems' FPS-164 Program Development Software and FORTRAN 77 Compiler. The FPS-164 will run under the Single Job Executive (SJE) Operating System. Floating Point Systems will develop and support all components of the interface.

Alphacom, Timex Sign OEM Agreement

Alphacom has signed a multi-year agreement with Timex Computer Corporation to provide computer output printers for use with Timex/Sinclair computers. The printer is specifically designed for Timex and will be sold under the Timex/Sinclair trademark.

VRTX Selected By Hewlett-Packard

Hunter & Ready's VRTX operating system is the first product chosen by the Hewlett-Packard Logic Systems Division for recommendation to customers through the HP PLUS program. Hunter & Ready's VRTX is the only operating system originally designed as a silicon software component. It is used primarily for embedded systems in communications, instrumentation, process control and other real-time, multi-function applications. VRTX is available for 68000-, Z8002-, 8086/88 and 186/188-based systems.

Here's a smart addit to our family of intelligent plotters.

IBM SNA/SDLC COMPATIBLE

Zeta 3610 Intelligent Plotter
A four-pen, 36-inch intelligent plotter with speeds up to 20 inches, 2g acceleration and resolution of .001".

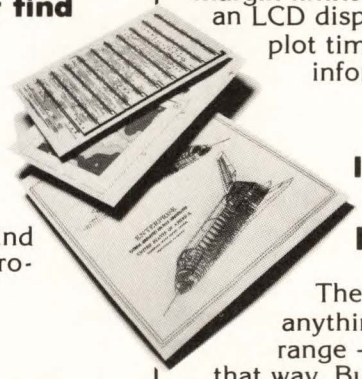
A high-performance plotter with a remarkably low price tag.

Our newest model, a four-pen, 36-inch intelligent plotter, is just as smart as the rest of our line — we've just made it more affordable. To do so we had to sacrifice a little speed and resolution.

Even so, look what you get: An impressive 20 inches per second, 2g acceleration and a resolution of one one-thousandth of an inch.

Features you won't find on other, more costly plotters.

Beginning with our proprietary design DC servo-motor drive and linear actuator pen system. The brains behind it all are two 16-bit microprocessors.



Other advanced standard features include semi-automatic paper loading, windowing, electronic margin limits with indicator and an LCD display used to report plot time and diagnostic information.

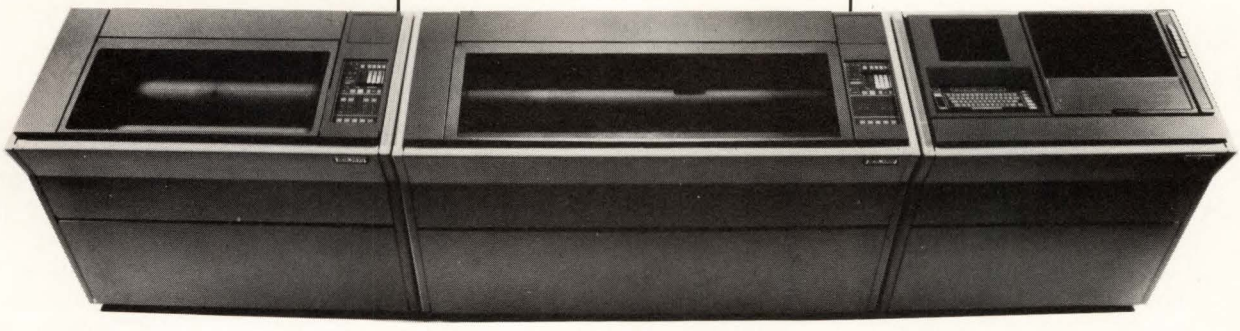
If you need the very best, look no further.

The Zeta 3610 beats anything in its price range — we designed it that way. But if you need even greater speed and precision, we've got it.

Our other 36" and 54" plotters run at speeds up to 50 inches per second vector dependent with 4g acceleration and resolution of 0.0125mm (0.00049 inches). And our on-line, off-line plotter work station makes these units even more powerful and efficient.

ZETA PLOTTERS

NICOLET ZETA CORPORATION
A NICOLET INSTRUMENT SUBSIDIARY
2300 Stanwell Drive
Concord, California 94520
TWX 910-481-5951
Tel. 415-671-0600



Zeta 3620 Intelligent Plotter
A four-pen, 36-inch intelligent plotter. Speeds up to 50 ips with 4g acceleration and resolution of 0.0125mm (0.00049 inches).

Zeta 5400 Intelligent Plotter
A four-pen, 54-inch intelligent plotter. Speeds up to 50 ips with 4g acceleration and resolution of 0.0125mm (0.00049 inches).

Zeta C63 Intelligent Plotter
Complete workstation with read/write tape drive, built-in CRT and keyboard and plotter controller.

Write 25 on Reader Inquiry Card

CRT Shipments Slow

The 1982 recessionary economy and continuing deflationary pressures have had an effect on the high growth CRT terminal market. 1982 shipments of CRT terminals were up only 15.6% over 1981 levels, down from past growth rates in the 20% range. Dollar revenues in the CRT terminal market grew a disappointing 6.5% over 1981 levels, reflecting intense price competition in all sectors.

According to a recent study by Advanced Resources Development, Medfield, MA, improved price/performance ratios were responsible for 1982's still healthy rate of unit shipments. Manufacturers have found methods to differentiate products enough to perpetuate use. Overall, the greatest strength in shipments came from new products or consistent price cutting on existing products. Higher priced terminals, such as IBM 3270 type terminals and clustered intelligent terminals, grew at slower rates than lower priced units.

"Dumb" and "Smart" (non 3270) terminals were about equal in total 1982 unit shipments, with dumb units totalling 232,000 units and smart terminals totaling 234,000 units. Both categories grew at similar rates in 1982, with dumb unit shipments up 16% over 1981, and smart units up 17% over 1981. Despite predictions that shipments of dumb terminals would drop off in favor of smart units, dumb terminals showed a good performance due to continued popularity of DEC's VT100, and new products such as the ADDS' Viewpoint, Hazeltine's Esprit, and Televideo's 910. Competitive price cuts on existing products to combat the aggressive pricing of new products boosted unit sales but lowered revenues. Dollar revenues grew 10.2% in 1982 for dumb terminals, compared to 10.8% for smart terminals.

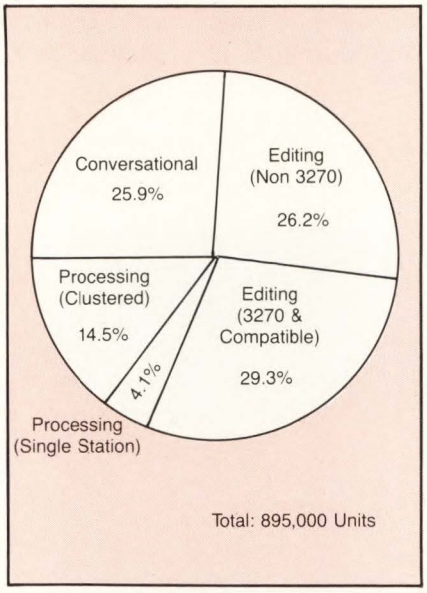


Figure 1: 1982 U.S. CRT Terminal Shipments.

Dumb units are not dropping off significantly in favor of more fully featured terminals, according to Mary Owen, a consultant with ARD. "Instead there has been surprising strength in shipments in this category in 1982. Dumb terminals have rebounded based not only on lower prices and new products, but also on important new applications which have appeared and will ensure their continued strength through 1987." Owen added that the market for terminals sold as separate units is threatened by the buying trend for total workstations and desktop units.

Shipments of the IBM 3270 and 3270 plug-compatible editing terminals led all terminal categories in unit volume. Nearly 30% of 1982 CRT terminal shipments were 3270-type editing terminals. These terminals showed a 1982 unit growth rate of 13.9% over 1981 unit shipments.

It is projected that more than 6,500,000 CRT terminals will be shipped from 1983 through 1987. The highest unit shipment growth rates will be seen in smart/editing terminals as well as IBM 3270 and compatible terminals.

The market study, "CRT Terminals: Markets and Strategies" is available from *Advanced Resources Development, 28A Park Street Station, Medfield, MA 02052. (617) 359-8090.*

Microelectronics And Computer Technology Corp. (MCC) Begins Activities

The recent appointment of Robert Inman, formerly Deputy Director of the CIA, has enhanced the efforts of the founding members of MCC in the eyes of potential contributors. Original members include: Advanced Micro Devices, Control Data, Digital Equipment Corp., Harris Corp., Honeywell, Motorola, NCR, National Semiconductor, RCA and Sperry.

The consortium is the offshoot of Robert Price and William Norris of CDC who have overseen the development of four successful technology sharing agreements with several other groups of companies. The idea to form the group was expressed by Price in a speech to the 1980 CBEMA meeting. This led to a 1982 invitation from Norris to 22 CEOs of high technology companies to meet and work towards realizing the program. The meeting allowed 15 of the participants' companies to form committees—six task forces—to examine how the concept would be realized, the amount of

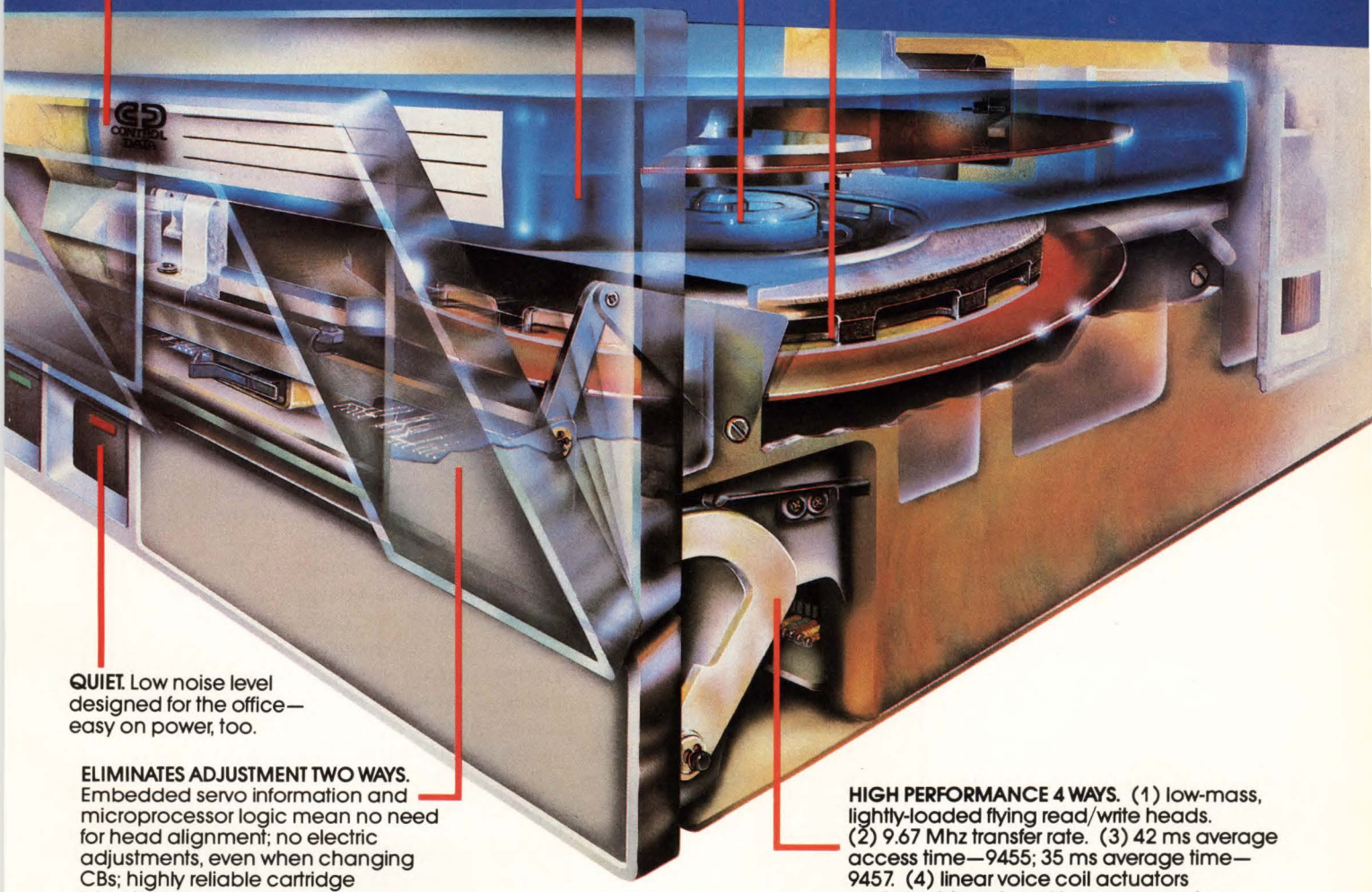
NOW TWO FIXED/REMOVABLE 8" DRIVES DOUBLE YOUR STORAGE OPTIONS.

50-MBYTE VERSION ADDED. New LARK Model 9457, with 25 Mbytes of fixed storage plus 25 Mbytes of removable storage per cartridge, joins the 16-Mbyte Model 9455 (8 Mbytes fixed, 8 Mbytes removable).

INTERFACE FLEXIBILITY. Both 16-Mbyte and 50-Mbyte LARKs come with SMD interface or LARK Device Interface (LDI). Plus new optional 9050 Control Module brings you ISI—the Intelligent Standard Interface.

COMPACT SIZE—STANDARD PACKAGE. Both LARK models are identical in size, shape and mounting; both are the width of an 8" FDD—just right for more space-efficient system.

EXCEPTIONAL RELIABILITY. LARKs are totally sealed during operation. No external air is forced across fixed module or cartridge disk surfaces.



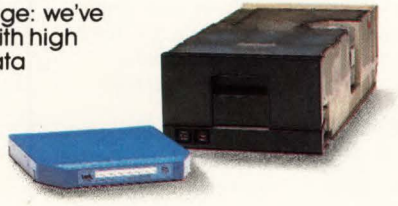
QUIET. Low noise level designed for the office—easy on power, too.

ELIMINATES ADJUSTMENT TWO WAYS. Embedded servo information and microprocessor logic mean no need for head alignment; no electric adjustments, even when changing CBs; highly reliable cartridge interchange.

HIGH PERFORMANCE 4 WAYS. (1) low-mass, lightly-loaded flying read/write heads. (2) 9.67 Mhz transfer rate. (3) 42 ms average access time—9455; 35 ms average time—9457. (4) linear voice coil actuators and precision closed-loop servo system.

THE LARK™ FAMILY

Now LARK doubles your options for built-in back-up with unlimited shelf storage: we've added the 50-Mbyte Model 9457 to the 16-Mbyte Model 9455. Both come with high quality and reliability built in. For more information, call your local Control Data OEM Sales representative or write: OEM Product Sales, HQNO8H, Control Data Corporation, P.O. Box 0, Minneapolis, MN 55440.



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CONTROL DATA

Addressing society's major unmet needs as profitable business opportunities

Market Trends

funding, the location, the work to be pursued, etc. By August of 1982, the MCC was incorporated in Delaware to pursue four R&D programs. In January of this year, Inman was selected as President and CEO and began to implement the plans. The participants have assured that the Justice Department will be kept abreast of their work so that there will be no claim of anti-competition made against the MCC once in place. To date, the Justice Department has said only that it will monitor events.

Events leading to the establishment of the MCC are complex and involve problems internal to the computer industry as well as external factors. Of the external motives, the effort of the Japanese to organize a Fifth Generation project is seen as a major impetus, but the resulting lack of response from Washington about coordinating a similar effort in the US is what actually brought the participants together. In terms of internal problems, the shortage of talent, tight money, a long time span required to design and develop a computer product, and the explosion of technologies are the most important. In the latter case, it has become almost impossible for firms to maintain experts in the 20 to 40 disciplines needed (ranging from sub-atomic physics to semiconductors) to stay on the leading edge of computers. All of these factors point to the need for cooperation in basic research.

Bubble memories are cited as one example where several companies spent millions of dollars to determine whether the bubble or semiconductor memory would be more productive. MCC intends to provide its members with an opportunity to evaluate the "usefulness of a technology" and then to allow them to use the technology to their own specific advantage. The final effect is seen as being the enhancement of competition.

A basic ground rule for the group, as is the case in other cooperatives in which CDC has been involved, is that there shall be no manufacturing or marketing of the technologies by the group. However, unlike the earlier formed Semiconductor Research Corp. (founded by the Semiconductor Industries Association), which funneled corporate dollars to Universities, MCC will be a research organization. Staffing will be scientific and technical personnel who will do the research.

The announced goals of the MCC are similiar to those announced by Professor Moto-Oka in the Japanese project for a fifth generation system: microelectronics, advanced computer architecture, computer aided design, and software productivity. One of the difficulties in pursuing such broad areas of research will be to select managers who can oversee the overlap of the four areas of work. Not all of the companies that are underwriting the MCC will participate in all of the programs. Each member will be assessed by the number of programs to which it subscribes, and share in the administrative and overhead costs of the consortium.

As of January 24, there were 10 member companies; another two dozen are evaluating participation in the group. An associates program is under consideration, which is initially considered a vehicle for information dissemination or as sponsors of seminars. The basic organization has three levels of participation: associates who would access the type of research being done at MCC, an intermediate group who would have somewhat more access, and finally, MCC full members who would access the analytic and predictive types of research performed.

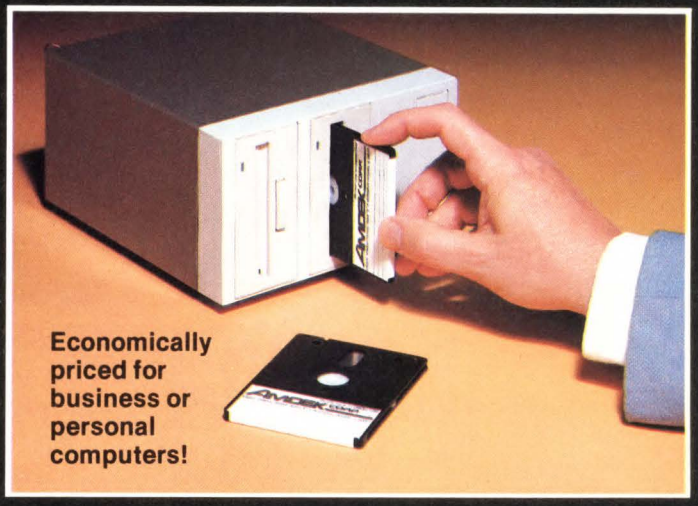
William Schaffer (from Control Data Corp.), the acting Public Relations representative of MCC, notes that the MCC isn't the only answer to foreign competition. Other needs are regulation, legislation, changes in the methods of manufacture, and improvements in company organization.

—*Borrell* **Write 240**

New Amdek 3″ micro-floppydisk drive system!

AMDISK-III . . . the engineer's choice:

- New 3″ hard plastic encased diskette.
- Up to 1 megabyte storage. (unformatted)
- Plug-in compatible with 5¼″ drives.
- Compatible with - IBM-PC.



Specifications

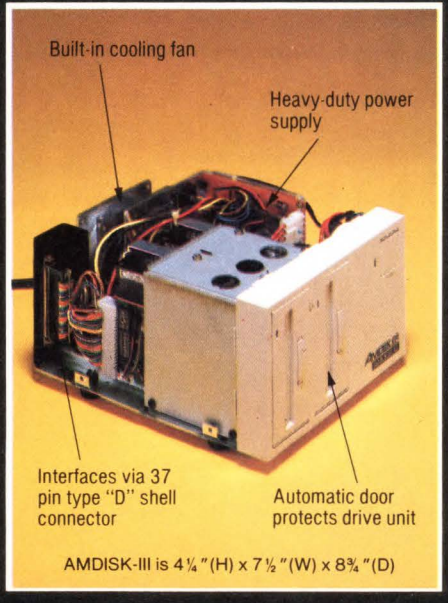
	Unit	Double Density
Capacity		
Unformatted Per Surface	Bytes	250K
Media		
Record Surfaces	2	
Tracks	80	
Recording		
Max Recording Density	Bpi	8946
Track Density	Tpi	100
Transfer Rate	bits/sec	250K
Access Time		
Average Access Time	msec	55
Track to Track	msec	3
Setting Time	msec	15
Average Latency Time	msec	100
Motor Start Time	sec	1
Disk Speed	rpm	300
Reliability		
Error Rates		
Soft Error		10^{-9}
Hard Error		10^{-12}
Seek Error		10^{-6}
Media	3-inch Cartridge	
Drive Interface	Plug Compatible with 5.25 inch FDD	

External Interface

Connector: 37-pin "D" shell connector

Pin No.	Signal	Pin No.	Signal
1-5	Unused	13	Write data
6	Index	14	Write enable
7	Motor enable C	15	Track 00
8	Drive select D	16	Write protect
9	Drive select C	17	Read data
10	Motor enable D	18*	Select head 1
11	Direction	19	GND
12	Step pulse	20-37	GND

*drives are single head



AMDISK-III is 4¼″(H) x 7½″(W) x 8¾″(D)

Evaluation samples $480

Includes two-drive Amdisk unit with built-in power supply, 4 diskettes and application literature . . . Call (312) 364-1180.

The AMDISK-III Micro-floppydisk System is an engineering breakthrough in disk size, storage capacity, media protection and user convenience. Designed for microcomputers for many applications, the Amdek system is ruggedly constructed to provide years of trouble-free operation. Warranty is 90 days (parts & labor).

Put the new AMDISK-III to test . . . its recording format, data transfer rate and disk rotation speed are compatible with 5¼″ floppydisk drives. Call, or write for evaluation samples at only $480.00 . . . or circle the reader service number for full technical details.

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(312) 364-1180 TLX: 25-4786

AMDEK CORP.

See us at NCC/83 Booth P7638

Amdek . . . your guide to innovative computing!

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Our 8" Slimline disk drives are the smallest and our 5¼" half heights are rolling out by the truck load.

That's R&D you can bank on: Response and Delivery.

You say you need drives that are half the height but all-the-way reliable? From a source that's equally reliable? And you want a choice of configurations too?

Our response is a line of 5¼" Slimline™ drives built with three different bezels and door styles, your choice of direct or belt drive motors, and either of two densities, 48 TPI or 96 TPI. But only one quality standard: the highest.

They come single or double-sided, with capacities from 250 Kbytes to 1 Mbyte. And for those who can do with a little less speed MPI responds with a consumer model at a lower price tag.

And when you wanted smaller, compact 8" drives, we replied with the smallest ones there are. Our 8" Slimline™ series. Only 2" thick and 11.5" deep. The selection doesn't end there. You can also get a 4.6" bezel as well as a half size version at 2.3".

To the cry for ever-smaller disks, MPI answered with the smallest disk drive ever. A 3" micro floppy that interfaces with 5¼" systems, handles 500 Kbytes of data and uses media protected by a hard shell so you can carry it in your shirt pocket safely.

That's how MPI operates. By responding with what you need. Then delivering. By the truck load from the West Coast. By the ship load from Singapore. Our own second source in the Orient that duplicates the precision production of our California plant. What's more, we are manufacturing our own heads.

That all adds up to MPI's kind of R & D. Response and Delivery. And that makes us the company to bank on.

MPI
MICRO PERIPHERALS, INC.

Write 26 on Reader Inquiry Card

Micro Peripherals, Inc., 9754 Deering Ave., Chatsworth, CA 91311. Phone (213) 709-4202. TWX (910) 494-1213.
MPI, Inc. Europe, 11A Reading Rd., Pangbourne, Berkshire, RG8 7LR England. Phone 7357-4711. Telex 848-135-MPI EURG.

Streamlined Electronics Key to Half-Height Designs

Dramatic decreases in the size of mini- and micro-Winchesters and flexible disk drives result from not-so-dramatic advances in technology. "The major factor facilitating the design of half-height drives and microfloppy products is the availability of low-profile DC spindle motors," says David A. Eeg, Director of Marketing for Shugart Assoc. (Sunnyvale, CA).

In addition to being slimmer, these direct drive DC motors allow elimination of the belt, pulley and bearings found in standard-height floppy and minifloppy products. This factor also contributes to higher reliability through fewer parts, and longer component life through less heat dissipation.

"Other factors enabling Shugart to design a half-height rigid series are use of a smaller stepper motor and a streamlined head-actuator carriage (HAC) assembly," adds Eeg.

The smaller stepper motor is actually more accurate than that of the standard-height drives. It sends a more consistent level of torque to the head and reduces hysterisis: the difference between the intended and actual location of the head. With greater positioning accuracy, the track density increased from 256 tpi in standard-height drives to 360 tpi in the half-heights. With more tracks per surface, higher capacity is achieved: Shugart's SA706 (**Figure 1**) offers a 6.67 Mbytes on one platter and 13.33 Mbytes on two platters—about double the amount of their standard heights 5.25″ rigids.

Figure 1: Decreased height in today's half-height Winchester drives (such as the Shugart SA706, above right), as well as in flexible disk drives, resulted primarily from a streamlined DC spindle motor design.

The new HAC assembly enables the stepper pulses to be transmitted directly from the band actuators to the heads, rather than through a secondary arm and actuator spindle used in full height-drives.

Reduced-sized printed circuit boards also facilitated the design of half-height drives. The smaller boards, achieved principally through use of custom LSI circuitry, occupy less space and therefore offer greater flexibility in the placement of the drive's other components.

Write 270

Microfloppy Standards—The Race Heats Up

Currently on the floor of the American National Standards Institute (ANSI) there are three microfloppy standards work papers proposed: the 3″, 3.25″ and the 3.5″. Proponents for the 3.5″ microfloppy include Sony, Verbatim and the 19-company Microfloppy Industry Committee (MIC). Included on the side of the 3.25″ format are Seagate, Tabor, Dysan and Brown Disc. The Japanese combination of Hitachi Ltd., Hitachi Maxell Ltd., and Matsushita Electric are pushing the 3″ drive.

A few months ago, the 3.5″ microfloppy appeared to be the strongest contender due to a big push from Sony. At present, however, there is growing support for the 3.25″ design. This is evidenced by Tabor Corp's (Westford, MA) recent announcement of a major agreement to sell their TC500 Drivette 3.25″ microfloppy disk drives to Soroc Technology. Soroc will use the Drivette in its new Execline Series desktop computer. George Rea, VP of Marketing at Tabor said, "This is our first OEM contract and represents a significant step not only for Tabor, but for all advocates of the flexible jacket microfloppy media format." Committed to supplying the 3.25″ media are Dysan, Brown Disc, BASF and 3M. Tabor has also licensed Seagate Technology as a second-source manufacturer of the Drivette.

At the January 26-28 ANSI meeting in San Diego, there were two papers presented. Dysan described their 3.25″ soft jacket media and the Tabor drive that is de-

signed to use it. MIC and Sony jointly presented a draft of the work paper to standardize the 3.5″ hard case cartridge. There was no additional information from 3″ cartridge proponents, who had previously presented their paper at the September meeting.

Official action taken by ANSI included a letter ballot to be mailed out to the 49 member companies. It called for a vote on the motion from MIC to accept their paper as the working draft for the ANSI committee. There were no other motions from the other groups, and it is anticipated that the MIC motion will not carry. According to Jim Barnes, Chairman of ANSI Technical Committee X3B8, "There was some discussion that it's much too early to choose one of the three, or maybe an additional fourth one once we learn more about IBM."

And what about IBM? Ten minutes after the meeting adjourned, Roger Chenoweth received approval from IBM, via a phone call, to release the information on their new 100mm drive. It has 358 Kbyte unformatted capacity, single sided recording, FM encoding, 6865 bpi, 68 tpi, 46 tracks, and utilizes a constant wave length recording so the bit density is the same on all tracks. IBM will be supplying the media but expects other media vendors to offer it also.

The stakes are high in the race for microfloppy standards. A recent Dataquest study projects that microfloppy disk drive sales will grow from approximately $30 million in 1983 to over $200 million in 1985. It appears that the battle will continue for some time, both in the ANSI committee and in the marketplace.

—Hawkins

Gould SuperMini—Newest Addition To Concept 32/67 Line of Products

Gould S.E.L. has announced a mid-range supermini computer for its Concept/32 family of 32 bit computers in what appears to be a substantive attempt to lead the market for superminis. S.E.L. already claims to be the 2nd fastest computer company in terms of growth for 1982, with a revenue of $170 million. The efforts are part of a larger move by Gould Inc. to increase revenues of electronic products from 35% of the company total to 70% by 1993. Of its existing computer market share, the companies' products are found in simulation (54%), utilities (33%), sci-tech (16%), oil and gas (12%), industrial automation (14%), CAE and imaging (10%), and security and communications (5%).

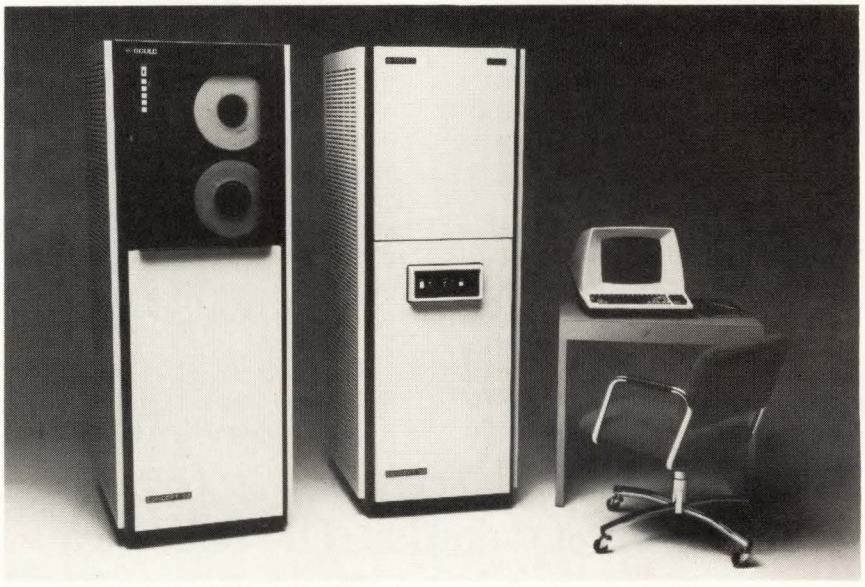


Figure 1: The Gould Concept 32/67 computers provide up to 2 million instructions per second in a compact package.

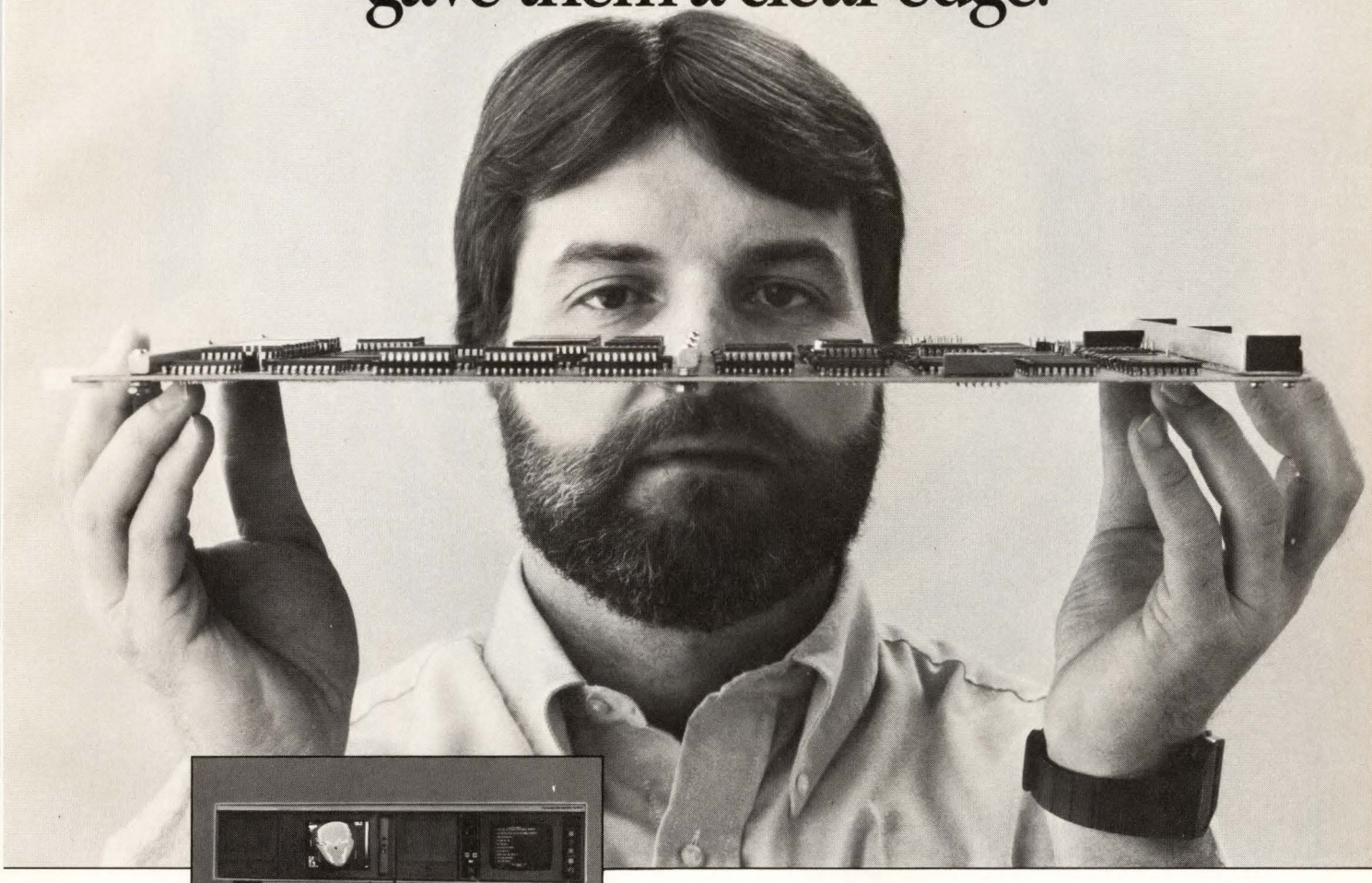
The company claims that its 32 series now provides the "broadest range" of minicomputers available, and that it has gone to great pains to assure that all products for any member of the line are compatible.

With a Whetstone rating of 1.7 to 3.0 MIPS (within the three different configurations available for the 32/67), the systems are most appropriate for real time, scientific/technical or process applications.

Three architectural strategies are employed: a memory hierarchy, a specialization of components, and a replication of functions. The series wide S.E.L. bus is used—a synchronous link with up to 26.7 Mbyte/sec transfer rate. The memory hierarchy is organized into 32 Kbyte of cache memory (subdivided into 16 Kbyte of data and 16 Kbyte instruction cache), up to 16 Mbyte of main memory, and up to 600 Mbyte of disk memory per disk drive. The top end (32/6780 computer), which employs the CPU and IPU, is 80% faster than the low end 32/6705. The communications multiplexer is a Z80A-based board that uses X.25 (level 2, synchronous) format. The three configurations

Picker International had a clear picture of their CT imaging needs.

The MSP-5 ARRAY PROCESSOR from CDA gave them a clear edge.



When Picker International was selecting an array processor for their new line of CT imaging systems, they looked for three things.

Ease of integration. Flexibility. And cost effectiveness.

Computer Design and Applications' MSP-5 array processor met all three qualifications.

As Jim Pexa, Engineering Manager, says, "CDA's MSP-5 array processor gives us a full range of performance for our new systems. Our highest performance unit uses 5 MSP-5s, our lowest, 1. So we purchase only as much processing power as we need. We really didn't need the more costly array processor, when it was so easy to implement our very specific algorithm on the MSP-5. And all we have to do is plug it into the computer chassis, and it's ready to go."

The MSP-5 can give you a clear edge, too. Write for more information.

CDA array processors are available for Digital Equipment Corporation, Data General and Perkin-Elmer computers. Priced at $5850 in OEM quantities. If you need full floating point 32-bit performance, the very programmable MSP-3000 will meet your most demanding requirements.

CDA COMPUTER DESIGN & APPLICATIONS INC.

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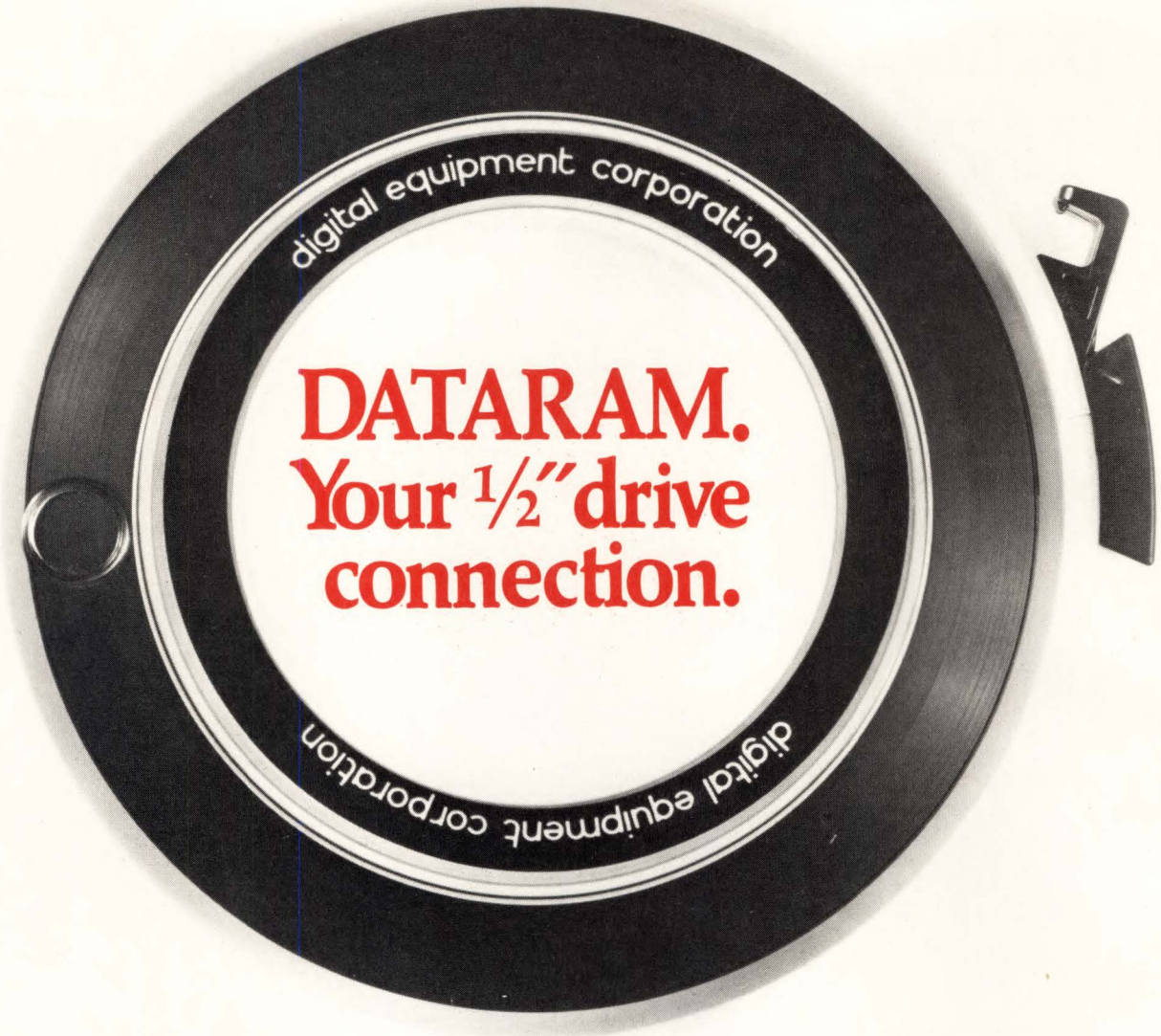

It's easy to interface your ½" drive to a DEC computer. When you have connections.

Dataram provides tape drive connections to your host LSI-11, PDP-11, or VAX computer, with a family of couplers/controllers that operate in NRZI, PE, or GCR modes. Dataram's couplers/controllers operate with ½" tape drives from all major manufacturers. As slow as 25 ips — or as fast as 125 ips. 200 BPI to 6250 BPI. With TM11 and TS11 emulations.

Start-stop or streaming. Efficient streaming is supported by a unique RSX-11M utility, FASTSAVE-11M, which provides optional backup and save capability for Dataram's streamer coupler. A full one-year warranty is standard.

For more information about ½" drive connections, call (609) 799-0071. We'll help you make the connection you need!

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DATARAM

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are designed to fit into the same cabinet, requiring only air cooling, and may be constructed with a reel-to-reel or multiple Winchester disks on user request.

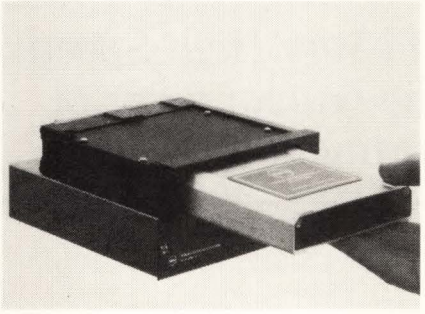
The company is justifiably proud of the software products announced with the systems, including: MPX-32 and UNIX Operating Systems; UNIX, C, Ada, Pascal and Fortran 77 languages; software development tools; and a library of programs including graphics, math, database management, and others to come. The math packages are said to be of the SPSS type to allow statistical routines to be processed, and the graphics packages include Versaplot, Template, and a Plot 10 emulator—an uncommonly wide initial offering by any standard.

—Borrell

Write 243

The Bubble Drive: An Alternative To Floppy Disks

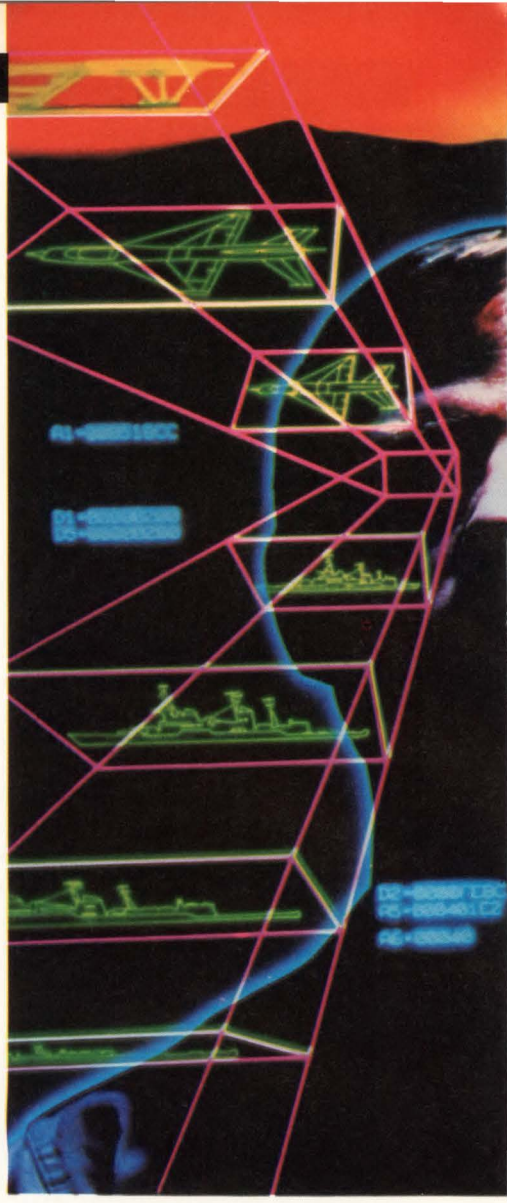
Aimed at harsh environment applications where the convenience of floppy disk is desirable but impractical, the emulation system consists of a housing and plug compatible unit. A choice of four removable bubble memory cartridges is available offering 128 or 256 Kbyte capacity over the temperature ranges of either 0–55°C or 10–40°C. Connected to a μC or other equipment, this floppy disk emulator operates transparently to the host and is suited for harsh and mobile situations. The major advantages of using bubble technology lies in its maintenance-free operation (no moving parts), non-volatility, extreme resistance to moisture vibration, dust, chemical and other field environments.



The non-removable hard disk version is to be announced by Targa shortly, and system level prices for the removable floppy-disk emulator with cartridge start at $3,240. *Targa Electronics Systems, 3101B Hawthorne Rd., Ottawa, Canada K1G 3H9.*

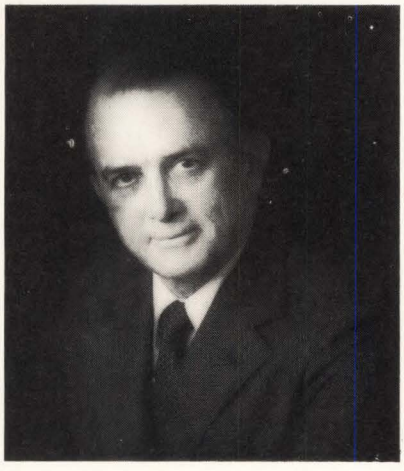
Write 241

Technologies And Trends Affecting The Military Computer Market



Standardization and Very High Speed Logic are two of the crucial areas of interest to the Department of Defense.

by Dr. Jon L. Boyes



Retiring from the Navy after a distinguished thirty-four year career, Admiral Boyes has experience in destroyers and submarines and in the technical and operational command, control and communications fields.

He has served in the rank of Admiral as Plans Officer, Defense Communications Agency; Director Communications, Europe; Director Naval Communications; Director Naval Command, Control and Communications; and Deputy Director General NATO Integrated Communications Systems Agency. His educational background includes graduate work in communications and ADP, a Masters degree in International Law (Honors) and Political Science (Honors) and a Ph.D. in International Affairs.

He is a member of several Scholastic Honor Fraternal Societies, and belongs to Lions International, The International City Managers' Association, AFCEA, the American Institute of Aeronautics and Astronautics, the American Society of Association Managers, and IEEE. Admiral Boyes has had a long association with AFCEA, having served as a National Vice President, an Associate Director, and as a Regional Vice President. He has been the author of several articles in the AFCEA Magazine, SIGNAL, as well as being an AFCEA convention moderator and panelist.

Today's proliferation of computers in the military may not be garnering the same level of national enthusiasm that surrounded the early space programs; however, elevated stature officially attached to high-technology endeavors has greatly bolstered interest in the field.

Part of this interest is a matter of dollars and cents. Frost & Sullivan (New York, NY) forecast the market for computer equipment produced in the U.S. for military and aerospace applications at $4.3 billion by 1986 (**Table 1**).

What may cause some downtime for the military computer market is the projected budget deficits and the resulting lack of public understanding and support of high dollar computer projects. It would be helpful if the public could be made aware of a *Computerworld* estimate that, "If the

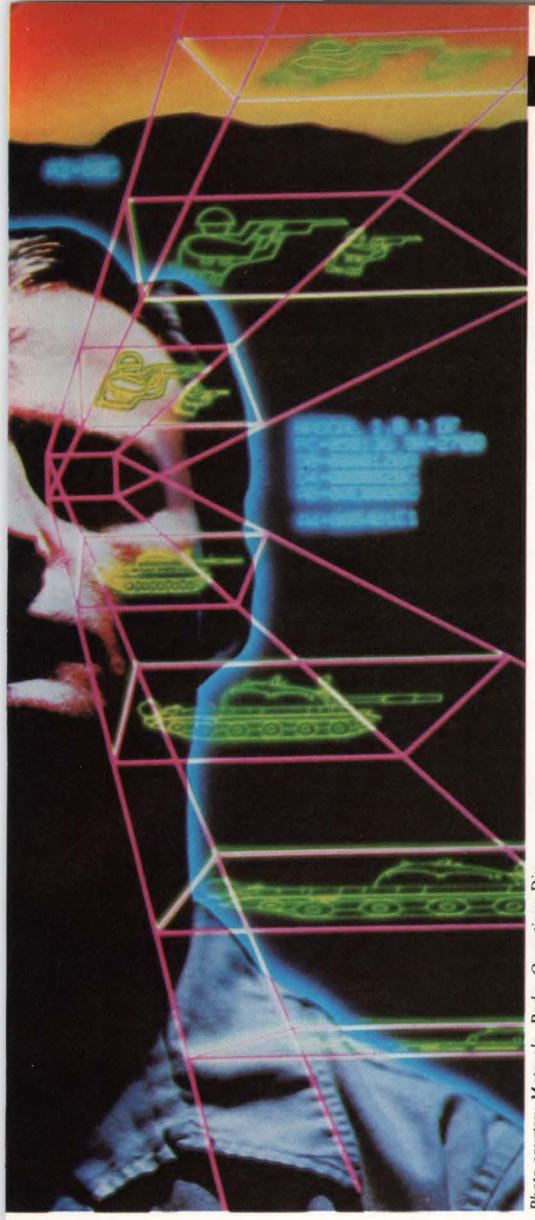


Photo courtesy Motorola, Radar Operations Div.

auto industry had done what the computer industry has done in the last 30 years, a Rolls-Royce would cost $2.50 and get 2,000,000 miles per gallon."

Due to phenomenal advances, computers have become nearly as important to the military commander as his weapons and logistics. In addition, there is less separation between the instruments of war and deterrence and the machinery of everyday business as usual. Many of the same skills and processes are used by a colonel controlling his border patrols as by a vice president managing his production forces.

The differences between civilian and defense R&D also dim. Sophisticated systems technologies may be used on either side of the fence, making every engineer and manager in and out of defense an integral part of the free world security picture.

It is the race to control the high speeds and power of electrons for the battlefield that very well may determine the real winner of the arms race. The winning command, control, communications and intelligence (C^3I) capability could be the strongest factor towards keeping the peace—or surviving the war.

From ENIAC To VHSIC

In 1946, the U.S. Army Ordinance Department contracted for the U.S. military's first electronic digital computer. Known as the Electronic Numerical Integrator and Computer (ENIAC), it performed computations of ballistic tables with the help of 18,000 vacuum tubes. Initially, programming was done by unplugging and rearranging patchcords.

Although the system made calculations hundreds of times faster than any previous methods, its capabilities shrink in comparison to those envisioned from the Department of Defense's most promising technology: very high speed integrated circuits (VHSIC).

VHSIC is a joint program to develop very large scale integrated circuits for high throughput data processors specifically designed to support unique military system requirements within stringent military environments.

The goal of the VHSIC program is to obtain a submicrometer chip with a 10^{13} gate-Hz/cm^2 functional throughput rate by 1986. An estimate of military signal processing—just one of the proposed applications—calls for a requirement of 5 billion arithmetic operations per second (**Table 2**).

To help accomplish this, the Defense budget is calling for RDT&E outlays of $79.6 million for fiscal year '83 and $125.1 million for fiscal year '84. The program is developing 28 complex integrated circuits for application in functional brassboards (**Table 3**).

VHSIC will allow for systems interoperability at all tactical levels and contribute to greater reliability, accuracy, jam resistance, security and ultimately maintenance-free systems. With the rapid solidifying of the technology to be used, $220 million has been set aside for a broad range of military applications including: command, control and communications (C^3), electronic warfare (EW), acoustics and tactical missiles.

Because of the enormous investments involved in design and production, only large companies such as IBM Corp., Intel Corp., Motorola Inc., Texas Instruments Inc. and Western Electric will eventually be able to enter the manufacturing market.

Semiconductor Technology

Major research efforts are also being conducted to overcome heat and power dissipation limitations which restrict both the speed and number of logic devices which can be placed on one silicon chip.

An alternate chip material to silicon, gallium arsenide, operates at higher temperatures and frequencies. Advanced gallium arsenide and silicon logic devices operated at gigabit rates will become available in the mid-80's.

Semiconductor specialists are now predicting that 100K bit chips will have access times of 10 nsecs by 1995 and eventually of only one nsec.

Work is also being done with charge coupled devices which may have three or four times as much potential storage density as conventional semiconductor memory.

The electrical conductivity of materials under near absolute zero temperatures is known as Josephson Junction. It is the focal point of research to make memory and logic circuits that will run at higher speeds but that will occupy less space and consume less power than conventional circuits.

Parallel Architectures

Since the invention of the computer in the 40s, logic aspects have been more expensive than communications. In the large scale and very large scale integration era, that cost structure has reversed.

Due to this change, most com-

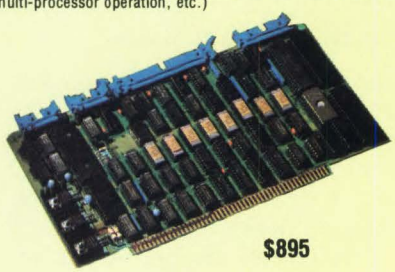
EXCEEDS S-100 IEEE 696 SPECS!

HIGH TECH, INDUSTRIAL QUALITY, SINGLE BOARD COMPUTERS

Sierra Data Sciences
SBC-100 Single Board Computer

High reliability is always a key factor when designing new systems or simply upgrading existing products. The Sierra Data Sciences SBC-100 offers the designer ease of integration, IEEE 696 compatibility with the hardened INDUSTRIAL quality necessary for State-of-the-Art product development.

- Z80A 4MHz Processor
- Zilog Dart (Z80ADART) serial 1/O chip. This part provides two (2) RS-232 ports with baud rates up to 19.2K baud
- ZPIO Parallel I/O chip. Two full parallel ports are provided with this chip
- NEC 765 Floppy disk controller chip. This LSI Floppy Disk Controller contains the circuitry and control functions for the support of up to four (4) full size (8") or mini (5¼") drives
- 64K Dynamic Random Access Memory. 64K of RAM is provided with the board. Ths SBC-100 is designed to permit the on-board RAM to execute with no wait states
- One 2732 EPROM is supported by the board. Ths 2732 EPROM provides up to 4K of user PROM space. The PROM address space may be "phantomed" on or off by a simple output command to a special on-board global control port
- Adherence to the IEEE 696 proposed standards. The SBC-100 was designed to meet the proposed IEEE 696 standard
- The SBC-100 was designed to meet the needs of a single-user systems as well as multi-user systems in a number of configurations (i.e., Time sliced single processor operation, loosely-coupled multi-processor operation, etc.)



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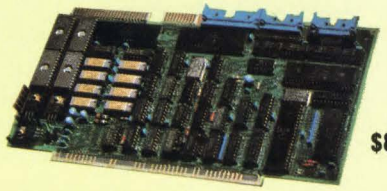
Sierra Data Sciences
SBC-100 Slave Single Board Computer

The implementation of multi-processor systems is an easy task to accomplish at a cost that will please any purchasing department. The SBC-100 Slave brings minicomputer speed and flexibility at "realistic" microcomputer prices. For existing 8086, Z8000 or M68000 systems the entire SBC-100 product line offers simple system expansion.

- Z80A Processor
- Zilog Dart (SIO optional) Serial I/O chip. This part provides two (2) RS-232 ports with baud rates to 19.2K baud
- Two (2) ZPIO Parallel I/O chips. Four full parallel ports are provided with this chip.Two ports are available through a connector located at the top of the board. The remaining two ports operate on the S-100 Bus as a highspeed data channel, and are used for I/O transfer operations during multi-processor communications



$825

- 64K Dynamic Random Access Memory. 64K of RAM is provided with the board. The SBC-100S is designed to permit the on-board RAM to execute with no wait states
- Four (4) 2732 EPROMs are supported by the board. The EPROMs provide up to 16K of user PROM space. The PROM address space may be "phantomed" on or off by a simple output command to a special on-board global control port
- EPROM Programmer (Optional). This optional allows the user to program his or her own 2732 EPROMs. EPROM programming software is provided with the purchase of his option
- Software Controlled Reset Inhibit. This feature permits any hardwar reset (i.e., front-panel reset key) to be ignored or recognized via a software controlled global control port
- Adherence to the IEEE 696 proposed standards. The SBC-100 was designed to meet the proposed IEEE 696 standard for the lines that it accesses.

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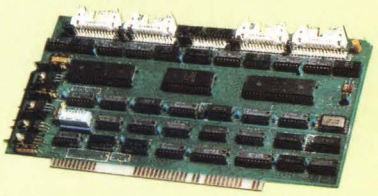
Sierra Data Sciences
Z-SIO Four Port RS-232 Module



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By establishing an interface that is STANDARDIZED, microprocessor based systems can EASILY communicate with the Real World. The ZSIO gives you this flexibility at minimal cost.

ADVANTAGES

- Can be completely Interrupt Driven, with no additional hardware required to process RESTART Instructions or Interrupt Vectors
- Incorporats a REAL TIME CLOCK that is programmable in increments of 1 to 255 times 1/60 second
- Can be configured to appear as a Modem or a Terminal with solderless berg jumpers
- Unique Interrupt Vectors can be generated for the following conditions
  - A. Transmitter Buffer Empty
  - B. External Status Change (DCD or CTS changes)
  - C. Received Characters Available
  - D. Special Receive Characters (Parity, Error, Overrun, Framing Error, End of Frame in SDLC model)

FEATURES:

• Baud rates programmable from 75 to 19.2K • Four Independent Full Duplex RS-232 Channels • 0-880K Bits/Second transfer • Doubly-buffered Transmitter data registers • Quadruply-buffered Receiver data registers • Program control of Asynchronous Characteristics such as stop bits, bits/character and parity • Program control of Sync Characters in Synchronous Mode • CRC Generation and Checking • HDLC and SDLC Communication Protocols

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MARKET SEGMENT	1979	1980	1981	1982	1983	1984	1985	1986
Military Aircraft	880	1350	1560	1780	1850	1860	1660	1600
Naval Shipboard	440	520	590	720	820	920	1040	1180
Battlefield	340	390	480	610	590	640	700	750
Military Communications and Control	16	54	94	106	104	122	131	64
Civilian Aircraft (CY)*	30	40	60	70	100	120	130	140
Missiles and Spacecraft	80	140	180	270	420	480	480	480
Air Traffic Control	14	17	19	22	48	67	75	82
TOTALS (rounded-billions)	$1.8	2.5	3.0	3.6	3.9	4.2	4.2	4.3

** Values for civilian aircraft segment are for calendar year periods. Other segments are presented for U.S. Government fiscal years.*

Table 1: U.S. market of computers in military and aerospace equipment and systems; value of U.S. production ($ million stated in current dollars) estimated and forecast, fiscal years 1979 through 1986 (Source: Frost & Sullivan).

puters in the mid-80s and 90s will take a new look: they will employ thousands of small, inexpensive processors. These small processors will have a very limited ability to send messages; however, they will be able simultaneously to attack small segments of large problems. This arrangement will yield a new generation of highly parallel computers (HPC).

Properly developed, HPC's will make major contributions in the areas of signal processing and large scale scientific and engineering computation, two pressing national problems. Signal processing has developed many new techniques in the area of electronic surveillance that could be of crucial value to the national defense. However, it requires so much computational "horsepower" that no existing computer can implement the requirements in real time.

It is projected that HPCs will be able to provide hundreds of millions of operations per second, and will be adequate for acoustic signal processing. Other areas, such as radar signal processing, require computing power which may surpass even HPC capacities.

Software

In software the military is running into basic problems of high cost and poor reliability. Lines of code per programmer per day has shown little improvement. Right now the technical community is trying to look at software production and maintenance from a life cycle view to determine how to better define software needs from the start. They are also developing a more structured design process to keep down high maintenance costs.

DoD is starting a new program beginning in 1984 and running through 1990 to obtain higher quality software products and improvements in software productivity. To make the programmer's environment "user friendly" greater emphasis will be put on automated methods and human engineering. Adaptation of personal computers for use as intelligent terminals with a library of software packages will also be part of the program.

Finally, DoD will establish a Software Engineering Institute to generate dialogue between the R&D world and the real system users.

The Perfect Language?

Classical scholars used to debate which was the perfect language. The search for the heavenly dialect usually focused on Greek, Hebrew or Latin. Today computer linguists are acclaiming the arrival of Ada*, a high order, standard programming language which will become the standard for mission-critical system software.

Prior to a DoD Directive in the mid-70s which halted the creation of new programming languages, hundreds were developed, although a vast range of DoD applications had similar requirements.

The High Order Language Working Group (HOLWG) was chartered to define what requirements were needed to meet all software needs in the mission critical area. They found no existing language met the requirements, and so sponsored an international design competition for a language with structured programming, top down design and information hiding. Honeywell eventually won a run off out of a field of 17 competitors. Specifications for the language are contained in the DoD "Steelman" document.

Since then the Army has contracted with SofTech for development of an Ada programming support environment called the Ada Language Systems (ALS). The Air Force has contracted with Intermetrics for development of the Ada Integrated Enviroment (AIE). And the Navy, which plans to go out with a procurement in 1984, has distributed their own specification for the industry to review.

When Ada is mature, the military will require all future real time embedded systems to use Ada. As yet no compilers have been validated, but several companies have indicated they will come in for validation in the first half of 1983. An example of one

*Ada is the trademark of the U.S. Government (Ada Joint Program Office).

of the program environments containing an Ada compiler is shown in **Figure 1**.

Ada is highly transportable; simplifies program maintenance; has self-documenting and user friendly features; enhances software reusability; increases application program reliability and reduces software life cycle costs.

Some experts believe Ada will expand significantly inside and outside DoD with some possible applications in data processing areas.

In the non-tactical arena, Fourth Generation non-procedural languages will most likely replace Third Generation languages like COBOL and other traditional high level procedural languages. These new languages are extremely user friendly. Instead of producing a "how to" program, the user defines what he wants and the system generates the appropriate software—a very important capability when one considers that there is already a shortage of trained programmers.

The leading languages include FOCUS by Information Builders, Inc.; INFO by Henco; MAPPER by Univac; RAMUS by Mathematica and some of the newer relational query languages. The Navy is conducting in-depth evaluation tests of FOCUS at the Naval Regional Data Automation Center (NARDAC) in Washington, D. C. and of MAPPER and INFO at NARDAC, New Orleans. Evaluation is ongoing at many Navy activities of relational query languages like SQL/DS from IBM.

VHSIC technology

- **INCREASE IN FUNCTIONAL THROUGHPUT RATE**

CURRENT:	1.5×10^{11}	GATE • Hz/cm^2
VHSIC-I:	5×10^{11}	GATE • Hz/cm^2
VHSIC-II:	10^{13}	GATE • Hz/cm^2

- **TECHNOLOGY TRANSPARENCY**
  EASY INSERTION OF NEW TECHNOLOGY
- **RADIATION TOLERANCE**

DOSE:	10^4 rad (SI)
DOSE RATE:	10^8 rad (SI)/S
NEUTRONS:	10^{11}/cm^2

- **AVAILABILITY**
  OBTAINABLE FOR APPLICATION IN ANY MILITARY SYSTEM
- **BUILT-IN-TEST**
  AT CHIP LEVEL

Table 2: Goals of the Department of Defense VHSIC technology project.

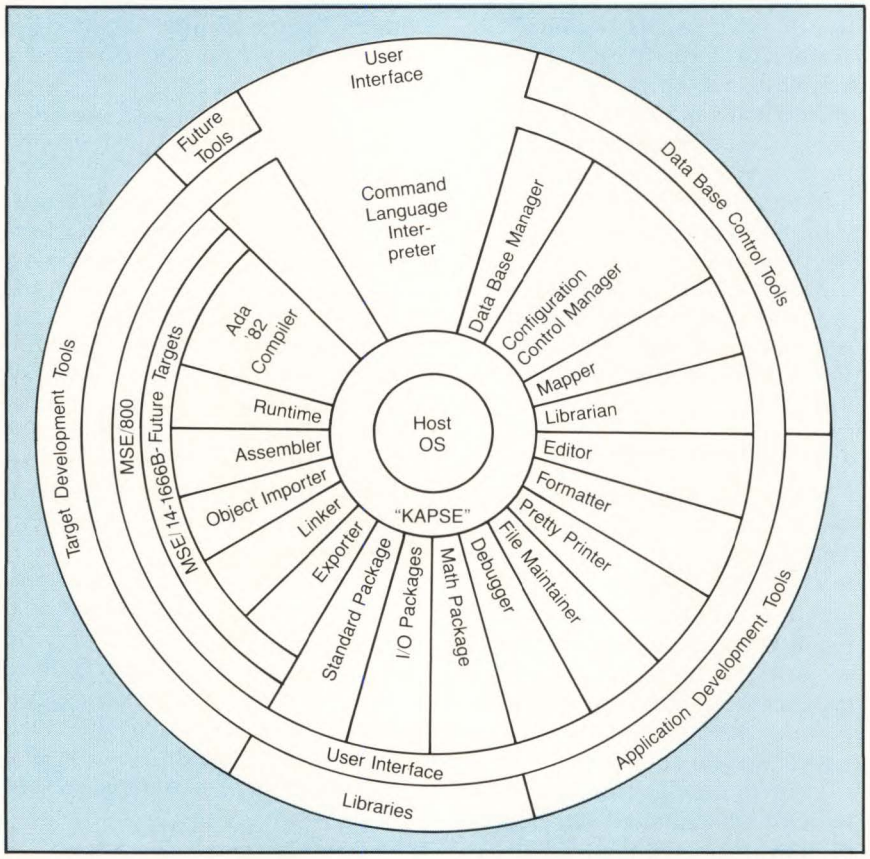


Figure 1: ADE-Ada development environment from ROLM features full DoD Spec, and ANSI 1982 Standard Ada Compiler.

Distributed Processing

A grassroots phenomenon has spurred the development of distributed processing throughout the armed services. It was started by officers who began using their own personal computers on the job. When the officer—and his computer—were reassigned, it left a department desperate to regain the missing capability.

As a result of this and other factors, the Air Force is planning to put out several different contracts for business-size, personal and portable computers.

Several hundred business-size computers have already been purchased from Cromenco to improve productivity in flight planning, scheduling and other Air

Force operations. Initially to be used as stand-alone computers, they will eventually be hooked into a base level system to form a distributed network.

The U. S. Army also is gaining revolutionary capabilities through the use of microcomputers. Their Theater Target Analysis system used commercially available desk top systems. The diminishing costs of μPs will undoubtedly fuel this trend.

Distributive processing will also move onto the battlefield. By putting computing devices on the spot, and in some cases, into the weapons themselves, a commander can increase the overall computing capacity while at the same time freeing his technicians for different tasks. For example, when VHSIC makes fire-and-forget missiles a reality, the embedded computer in the missile will take over the navigation controls, allowing the operator to move on to the next target.

Data Based Machines

Data Based Machines (DBM), currently being tested by the Navy, perform data based management processing independently of the host computer and then return the information to the host. The DBM is a back-end processor which takes data storage and manipulation tasks out of the host general purpose computer.

One advantage Data Based Machines have over the older data based management systems is that they can interface with two or more dissimilar hosts. Also they can operate without competing for time.

The Navy Data Based Machine Working Group, chaired by the Naval Data Automation Command, is currently coordinating a number of tests using several Britton-Lee DBMs (IDM-500 Series) connected to several host computers including UNIVAC, Digital Equipment Corp. and Hewlett-Packard Co. Evaluation of the only other commercially available DBM (iDBP), from Intel Corp., is planned in the near future.

More efficient hardware, friendly user interface, improved query capability, and portability of data are some of the advantages looked for in Data Based Machines. It could help solve DoD's growing requirement to effectively manage, distribute and integrate growing numbers and sizes of data bases.

Computer Graphics

One of the first uses of computer graphics by the U.S. armed forces was the Air Force's Semi-Automatic Ground Equipment console (SAGE), an air defense command and control system installed in the mid-50s.

As with many developing technologies in the commercial world, raster-scan CRTs used for most military computer graphics are very difficult to ruggedize. Consequently, efforts by such companies as Tektronix, Inc. focus on speeding up the drawing time and improving the resolution of flat-panel technologies that may one day replace CRTs for military use.

R&D in the military concentrates on techniques to combine imaging and graphics. Also charge coupled devices may be used in the direct storage and readout of images optically projected onto chips. Other areas of experimentation include electro-luminescence and liquid crystal displays.

Computer Switched Communications Networks

There has already been a successful push to link defense information systems with a high bandwidth state-of-the-art communications system. The new Defense Data Network (DDN), based on ARPANET packet switched technology, handles the large quantities of data from the intelligence

CONTRACTOR (SUBCONTRACTOR)	TECHNOLOGY	BRASSBOARD	DESIGN APPROACH	SPECIAL FEATURES
Honeywell	Bipolar-ISL, CML	Electro-Optic Signal Processor	Custom Chips Based Macrocell Library	Radiation Hardness Responsive Generic Architecture
Hughes (Signetics) (Perkin-Elmer)	CMOS/SOS	AJ Communications	Standard And Custom Reconfigurable Chips	Radiation Hardness Photolithography Contractor Highly Specialized Chips
IBM	NMOS	Acoustic Signal Processor	Master Image With Macrocell Library	Software Strength Design Approach
TI	Bipolar-STL NMOS	Multimode Fire-And-Forget Missile	Programmable Chip Set	Operational Fabrication Facility Design Utility System
TRW (Sperry-Univac) (Motorola)	Bipolar-3D T^2L CMOS	Electronic Warfare Signal Processor	Standard Chip Set	Innovative Memory Chips Versatile Chip Set
Westinghouse (National) (Control Data) (Harris)	CMOS/Bulk	Advanced Tactical Radar Processor	Standard Chip Set	Highest Speeds Good System Perspective

Table 3: VHSIC phase I contractors.

Artificial Intelligence To Enter Commercial Market

by Dr. John Clippinger

The next three to five years will witness the commercialization of Artificial Intelligence (AI) technologies. Also known as symbolic or fifth generation computing technologies, they are based upon symbolic and logical computing methods rather than the standard arithmetic and data processing hardware and software architectures today.

Due to the commercialization of special computers designed to run LISP—the unique language of AI—and the precipitous drop in the cost of computer hardware, it is now possible for computers to achieve new levels of intelligence. Applications requiring the interpretative and problem solving skills of experts in a variety of areas such as data analysis, VLSI design, threat assessment, information management, C^3I, budget analysis, instrument and test equipment interpretation, and training and support are all suitable for AI technology automation and support.

In the next three to five years, we can expect to see speaker-independent voice recognition systems for vocabularies in excess of 10,000 words, natural language interfaces to data bases, intelligent alerting and monitoring systems, three-dimensional computer vision with object recognition, and highly intelligent computer assistance for software development.

The importance of Artificial Intelligence is widely recognized by major corporations such as IBM, Hewlett-Packard, Xerox, Schlumberger and others. Governments world-wide also realize AI's potential, and have sponsored numerous research efforts, such as the Fifth Generation Computer Project in Japan, and the Informatique effort in France. The United States Department of Defense has earmarked AI as one of its top priority technologies for this decade.

A major multi-client study forecasting the technology and its applications for the next five years is currently available. The study is authored by leading experts in the field and covers the following areas: natural language processing, speech recognition, expert systems, vision, intelligence manipulation and control, and software development technologies. **Brattle Research Corp.**, 6 Faneuil Hall, Boston, MA 02109. (617) 720-0051. **Write 244**

and command and control communities to the world of logistics, finance and personnel. The DDN, managed by the Defense Communications Agency, will be the defense establishment's backbone data communications system for the next two decades.

C^3I Support

Some analysts would like to add computers to C^3I (command, control, communications and intelligence). Whether or not C^4I catches on, the role of computers will increase.

Many new systems now in R&D such as NAVSTAR GPS (Global Positioning Satellite); JTIDS (Joint Tactical Information Distribution System); sensor and intelligence systems, longer range weapons systems and EW systems, to name a few, will put new demands on computer operations when they are fielded. In combination with systems already on line, these newcomers will increase the amount of data commanders and staff must rapidly digest, making advanced data processing a necessity.

Frost & Sullivan reports that "there are a number of relatively small companies (or divisions) that have garnered a place in the market by virtue of a particular expertise. The point is, that the competitive environment in military C^3I is such that small new companies can successfully compete."

Defense budget figures for C^3I are shown in **Table 4**.

Computer Security

A significant thrust is underway to develop trusted computer systems that can simultaneously process mulitple levels of sensitive or classified information. The Defense Department Computer Security Evaluation Center established in 1981, assists DoD departments in evaluating computer system integrity and encourages the computer manufacturing community to develop trusted computer systems.

The Center works with computer vendors on a voluntary basis to determine the security capabilities of their commercial products. Honeywell, IBM, DEC, Control Data and Univac all are currently having systems rated.

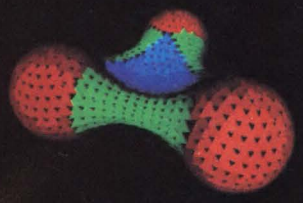
It is projected that many spin-offs of this program will benefit banking, insurance and other industries which process sensitive information.

Engineering Pool

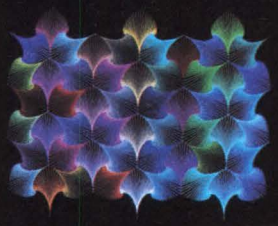
The Bureau of Labor Statistics forecasts that the U.S. will be short of 16,000 engineers each year through 1990. This, along with the absolute demand for lower costs, will drive the market to produce more and more maintenance-free, user friendly and self-diagnostic systems. Computer aided design (CAD) and computer aided manufacturing (CAM), along with increased robotics applications, show promise for helping to fill future manpower gaps.

Engineering shortages will also cause relationships between government, industry and academia to be restructured. Already corporations are finding it necessary to increase their share of the country's total R&D expendi-

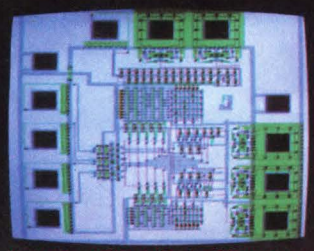
SUPERIOR GRAPHICS HAVE COME DOWN TO EARTH.



"Three Atoms" Courtesy of Greg Abram, University of North Carolina at Chapel Hill



"Aurora" By Richard Katz, Vectrix Corporation



"Integrated Circuit Design" Courtesy of Floyd J. James, University of North Carolina at Chapel Hill

"In The Beginning" By Richard Katz, Vectrix Corporation

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	Fiscal year ($ millions)*							
	80	81	82	83	84	85	86	87
Intelligence Programs	762.0	1,086.6	1,429.6	1,726.8	1,808.0	1,918.0	2,027.0	2,185.0
Strategic Surveillance and Warning	437.2	497.5	836.4	794.4	650.5	624.0	596.0	592.0
Strategic Command and Control	193.7	223.8	266.4	442.7	458.0	194.0	180.0	173.0
Strategic Communications	236.9	302.4	295.3	445.6	440.2	441.8	470.7	485.5
Tactical Reconn., Surv., and Target Acq.	308.8	327.6	360.2	397.6	406.0	447.0	462.0	481.0
Tactical Command and Control	720.5	758.0	688.4	1,040.3	478.0	487.0	291.0	531.0
Tactical Communications Systems	295.1	462.0	631.0	679.2	689.0	643.0	557.0	523.0
Defense Communications System	205.0	306.0	349.9	428.4	412.7	283.8	335.9	413.1
Global Positioning System	158.9	163.0	304.9	295.3	280.0	316.0	270.0	200.0
Navy Tactical C^3I	164.4	183.6	215.2	254.7	299.5	322.1	337.2	333.5
Space Mission Support	14.7	22.7	89.4	67.5	81.0	104.0	112.0	128.0
Other Advanced Development	82.5	81.3	111.0	135.8	142.2	147.0	153.6	162.0
TOTAL MARKET	3,579.7	4,414.5	5,577.7	6,663.3	6,145.1	5,927.7	5,792.4	6,207.1

**Current Dollars*

Table 4: U.S. military C^3I market forecast summary (Source: Frost & Sullivan).

Fiber Optics In The Military

by Frederic Quan

Optical fibers will first replace standard copper cables in interconnecting military computers to retrofit systems. The chief benefit in these applications will be fiber optic's Electromagnetic Interference (EMI) and Electromagnetic Pulse (EMP) immunity. The electrically quiet and accurate transmissions from fiber optic lines will ensure low bit error rates and prevent ground loop currents. As more of these systems are deployed, other benefits of optical transmission will become apparent (**Figure 1**).

Optical transmission will give military designers more freedom in dispersing equipment where it will most benefit the user. Bandwidth increases will give distributed data networks more power and speed, and make the transmission medium the limiting factor for the system. The small size and light weight of fiber optics will add up to portability and ease of hookup. Lower costs projected for optical systems should ensure cost effectiveness.

At the present, the absence of low cost optical couplers has been the technical hurdle limiting the growth of this technology. This situation is expected to change in the next few years, as more vendors recognize the growing market for optical transmission.

The next generation military computer systems will be designed with fiber optic interconnects as an integral part of the system (**Figure 2**). This is in contrast to the retrofit situation today. This evolutionary change will result in new computer architectures which will maximize the benefits of optical transmission.

ADVANTAGES:

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- Low Weight
- Flexibility
- Immunity to Electromagnetic Interference (EMI)
- Excellent Security
- High Temperature Capability
- Dielectric (No Electrical Hazards)
- Radiation Resistance

Figure 1: Advantages of fiber optics include large bandwidth and noise immunity.

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New Transmission Media Offers New Design Freedoms

Distributed Intelligent Networks Can Be A Reality

- No Repeaters Necessary For Most Applications
- Fast Transmission of Data, Voice, Or Video
- EMP Tolerance
- Low Bit Error Rate
- Total Electrical Isolation—No Extraneous Ground Loops

Figure 2: A number of new tactical network architectures are possible with fiber optics.

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What's more, the fast start/stop time permits greater data compression per inch of tape, setting the ECR-40 apart from existing cartridge recorders and providing an accurate, cost effective approach to data recording, storage, retrieval and reproduction. Spanning undersea, ground/mobil and airborne applications, this ruggedized MIL-SPEC Recorder is equally at ease in commercial aviation, geophysical exploration, petrochemical processing, nuclear power plants, telecommunications, medical research and diagnostics, oceanography, numerical machine control and numerous industrial applications.

To optimize performance, the ECR-40 powers up on 28 VDC with only 100 watts maximum and idles at a low 35 watts in standby. Tape contamination is minimized through a quick, easy loading cartridge design and the positive locking mechanism of the tape drive.

Proven Tri-Service Performance

The ECR-10 (AN/UYH-5) Digital Cartridge Recorder provides a ruggedized, MIL-SPEC alternative to its high capacity counterpart, the ECR-40. Offering a 4.3 megabyte storage capacity on ½″ tape, the ECR-10 measures only 4.0″W (×) 8.7″H (×) 12.7″L, and weighs in at a mere 15 lbs.

The ECR-10 has proven itself in numerous tri-service military programs, including: TRI-TAC, the Army's worldwide communications program, SEA NYMPH, TSQ-73 and TFCC. Using a 9-track, 800 bpi NRZI ANSI read while write format, this computer compatible unit is available with data transfer rate 12K bytes/second or 20K bytes/second yet consumes only 40 watts (nominal) in run mode and 10 watts in standby on 28 VDC input voltage.

Meeting the requirements of MIL-E-5400, the ECR-10 has an operational temperature range of 0 °C to + 50 °C and non-operational range of − 10 °C to + 65 °C, with an operating shock level of 15 g's, 11 milliseconds, half-sinewave and MIL-E-5400R Curve 11 vibration rating.

Tough Analog Designs Too

Applications requiring analog data (e.g., military sensor recordings; aircraft flight test applications; air, sea and ground data acquisition, monitoring and control systems, etc.) can also benefit from Genisco's ECR-20 Bi-Directional Analog Cartridge Recorder.

Utilizing 8-tracks on 4 passes of 2 channel record/reproduce electronics, the ECR-20 features a servo capstan motor drive with optical tack and bi-directional tape drive for added reliability and performance. At tape speeds of 1.875 ips and 60 ips, the ECR-20 maintains a frequency response of 100 Kz to 5 KHz., and 3.2 KHz to 160 KHz., respectively, and a signal-to-noise ratio of 33 dbM rms to rms at 1.875 ips thru 60 ips.

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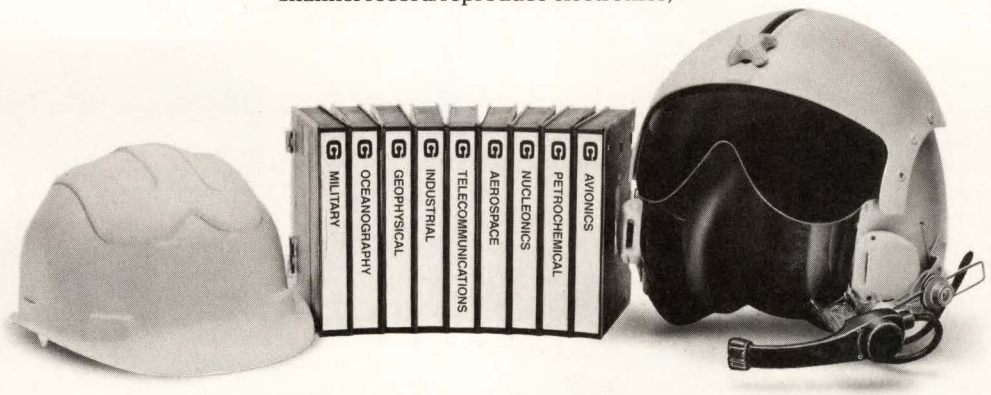

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tures. They are also beginning to allocate millions of dollars to fund research laboratories in major universities, a trend that is on the upswing. And in the military, such programs as The AFCEA Educational Fund and the Partnership for the Development of National Engineering Resources under the leadership of LTGen. William Hilsman, USA, are just two of the bridges between corporate resources and student needs.

Strategic Minerals

Even if the future does supply more engineers than is anticipated, they may not have enough key materials to work with.

Many metals which are today considered to be on an "endangered species" list are used in the production of computers, printed circuits, and other computer related instruments. Like oil, these minerals are an important factor in U.S. security interests abroad, where unstable political conditions could tip the balance against the U.S. It is an area to watch closely, not only by the military but by industry as a whole.

Technology Transfer

A recent reorganization of the Defense Department calls for stricter measures to control the spread of sensitive technology to other countries. The many reports of export abuses and the expansive level of Soviet interest in Western technology explain why.

At the January 1983 Armed Forces Communications and Electronic's Conference and Exposition in San Francisco, RAdm. E. A. Burkhalter, Jr., USN, Director Intelligence Community Staff said, "For about 70% of its technology acquisition requirements, the Soviet State Committee for Science and Technology turns to the Soviet intelligence services: the KGB and the military intelligence service, the GRU. This effort saves the Soviets billions of dollars in research and development costs."

There are other moves afoot, including the Customs Service's new Operation Exodus, to detect and prevent illegal exports of technology. However, there is one note of caution I would add. We must be careful to avoid the pitfalls of technology transfer witch hunts and other equally harmful over-reactions that could occur.

Continued on p. 92

Window Shopping For Government Equipment

Commerical off-the-shelf products are now available with value added to meet specific government requirements. An example is State of the Art Systems' (SOTAS, Inc.) Telecomputing System. The system consists of a portable terminal designed for single button access to data bases (**Figure 1**). It is probably the closest data equivalent of the telephone.

The battery-powered unit measures only 7½" × 1¼" × 4½", and includes a full typewriter-style keyboard, one-line liquid crystal display, and a built-in modem. The unit plugs into any modular telephone jack. The Telecomputer remotely accesses and communicates with a host computer through the use of plain English prompts and responses. A variety of peripherals are available for use with the terminal.

Although the Telecomputing System offers a three level security system to protect information, SOTAS can integrate this hand-held device with various COMSEC encryption systems. SOTAS has demonstrated the feasibility of using this device in conjunction with a small, low-cost data satellite terminal which allows the device to be used as the keyboard to enter messages and as a display to receive messages. The equipment can be integrated into the satellite terminal, and the electronic package can fit into an attaché case. If required, the Telecomputing system can be detached and with its internal modem be used at remote locations for sending and/or receiving satellite information.

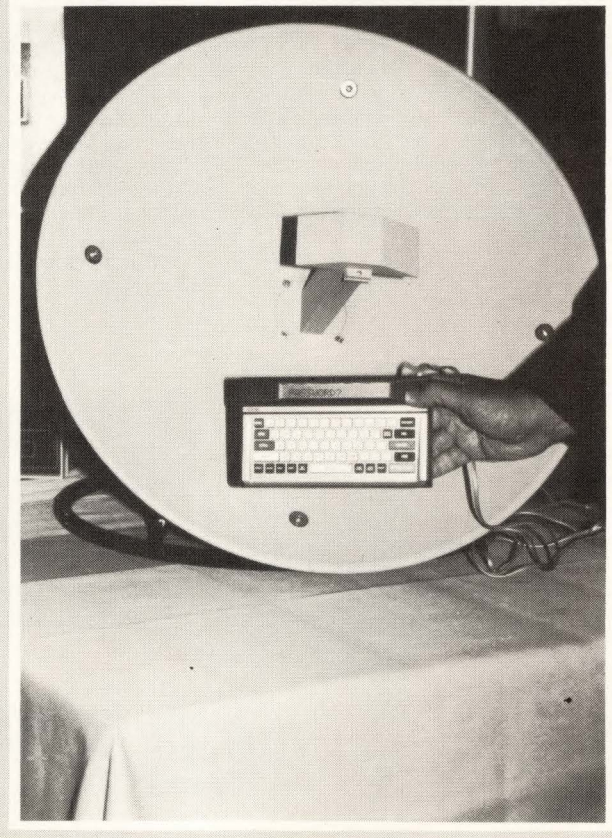

Figure 1: This SOTAS terminal provides single button access to data bases.

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A senior-level Electronic Engineer with a strong background in electronic design, testing, and test procedures is required to review, prepare and implement engineering changes. An active knowledge of missile guidance, microwave, and digital circuitry is required.*

ELECTRONIC ENGINEERS

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Weapon Systems Engineers with a broad background in radar, servo systems and missile systems test requirements. Will design, and test digital circuitry for advanced guidance systems. Signal processing and ability to work with data analysis and statistical tools required.**

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SENIOR COMPONENT ENGINEERS

We're seeking Component Engineers in the following areas: Electronic Components, RF Electronic Components, Mechanical Components. Responsibilities will include providing technical support to designers in the selection and standardization of component parts, solving component-related production, technical and procurement problems, preparing and maintaining component specifications and verification of failure diagnosis. Must have working knowledge of military specifications. Three years' experience required, degree preferred.**

RESEARCH & DEVELOPMENT

Engineers experienced in development of silicon gate CMOS technology; knowledge of discrete time signal processing with emphasis on spectral analysis; millimeter wave component subsystem design, test and evaluation for seeker technology related IRAD and CRAD. Experience and successful history of laboratory accomplishments with electromagnetic fields and plasma physics essential.**

SOFTWARE

Design, test and documentation of guidance electronics software; design and test logic all AROYS and develop test procedures for large scale hybrid microelectronic assemblies (HMAS); development of software procedures for computer graphics application (Computer-Vision and/or Limited).**

PRODUCT SUPPORT

Must have experience with MIL-Spec tech manual and publications; understanding of engineering principles, drawings and electronics; prepare provisioning parts list in MIL-STD 1552 format, prepare DLMF plans and operating documents; hands-on shipboard or aircraft weapon systems.**

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Manufacturing Engineers with experience in production and final assembly process involving flex harness fabrication, tooling and CAD/CAM fusion and heliarc resistance welding. Quality Engineers with experience in softward Q.A., development/production programs, hybrid microelectronics. Must be able to define quality requirements for process, materials and systems.**

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7 To 1 Active Communications Line Multiplexer

Plugging and unplugging, changing and redistributing time share communications lines is not only cumbersome to users but also hard on equipment connectors and cables. This multiplexer system was designed to alleviate this problem. It was developed for use in a multiuser environment, where each connected user was frequently on-line for short periods. It is particularly useful in office configurations of small personal/business μCs which require frequent communications with a main computer system.

Up to seven users can be connected via the multiplexer to one port on the main system, using RS-232 interface techniques. This allows greater system flexibility of system port configuration and allocation. Remote users have total control over the multiplexed line while on-line, preventing accidental loss of line or "time out" due to lack of activity sensed.

One minor modification to the system software driver is necessary for resetting the multiplexer upon user log-off—the transmission by the host system of a 4 sec break signal after log-off. The break command is sensed by the multiplexer and the line is made available to the next user. Access to obtain the line is accomplished by any activity on the remote keyboards. It will then accept the first activity and deny all others until the line is again made available. This is a particularly useful feature when used for down loading and up loading programs to and from remote μCs and the host system.

This multiplexing system allows using both hardware handshaking and software control of non-hardware handshaking. To use the hardware handshaking method, the Data Set Ready signal from the remote user is transmitted to request the on-line link to the host system. If the line is available, the Data Terminal Ready

Continued on p. 92

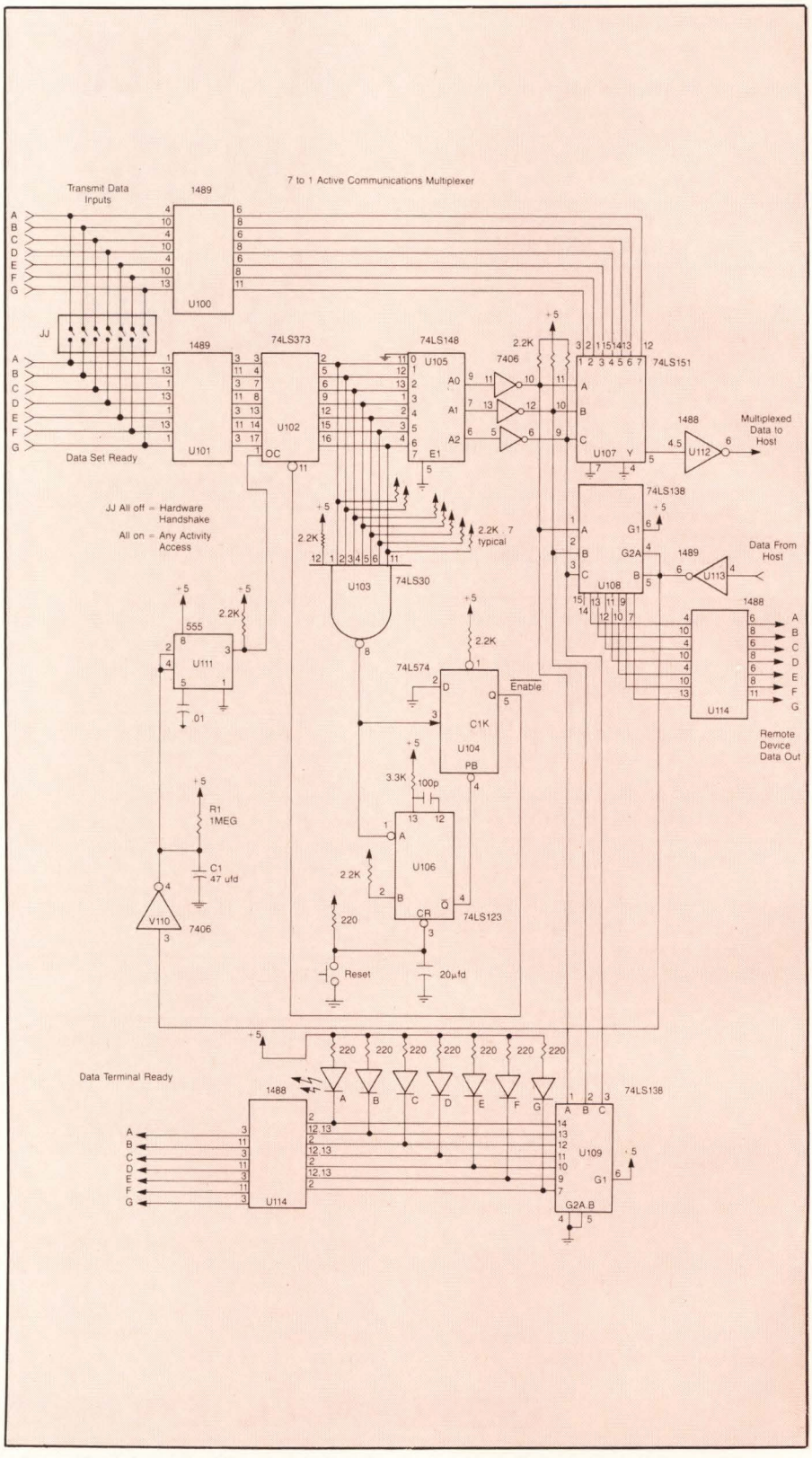

Figure 1: Schematic diagram of 7 to 1 active communications multiplexer.

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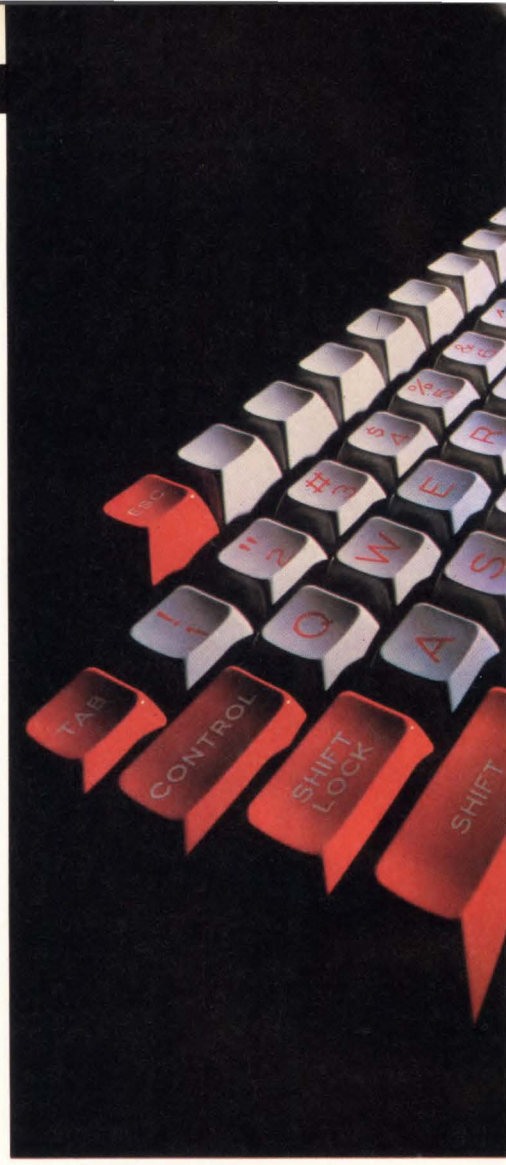
RFI/EMI Shielding Scheme For FTM Keyboard

Development of the full-travel membrane (FTM) opens low cost solutions to the problems of both emitted and received energy.



by Joe Jesson and Russ Krawczyk

Some computer equipment designers view the new Federal Communications Commission (FCC) regulations limiting radio frequency and electromagnetic interference to be expensive and burdensome. Due to these new regulations, all components making up a computer system have come in for attention with the goal of designing economical RFI/EMI barriers.

Underlying the FCC regulations (particularly part 15, see box) are the many interference complaints resulting from the operation of digital equipment near receivers. These receivers can range from "safe" radio and television sets used solely for home entertainment to communications systems used by aircraft, where RFI/EMI interferences can be potentially life-threatening.

Among the concerns of computer manufacturers is the deadline imposed by the FCC. The problems associated with designing into computer systems the ability to meet the interference regulations have already led to two postponements: first from January 1 to October 1, 1981, and then to October 1, 1983. It's widely believed that the last date will be enforced with no further postponements.

To meet the FCC regulations, designers have been coping with the cost of additional components, additional labor, and overall design and redesign efforts needed for compliance.

Since 1981, component suppliers have been making headway in designing cost-effective, shielded components. These needs have been filled with various low-cost interference barriers, including: Paints (silver, carbon/silver, copper/graphite), vacuum metallization (aluminum), flame spray (zinc, aluminum), ion plating, and composite plastics.

One of the components that has come in for a great deal of study with respect to shielding is the keyboard. Keyboards based on traditional technologies are difficult to shield because of the physical nature of individual switches. To effectively shield nonplanar switch elements, intricate metallization and metal braiding must be used. The recent development of the full-travel membrane keyboard, however, opens low-cost solutions to the problems of both emitted and received energy.

Joe Jesson is the Product Manager and Russ Krawczyk is the Senior Developmental Engineer for Oak Switch Systems Inc., Crystal Lake, IL.

Field Generation Analysis

The design of RFI/EMI shielding schemes derives from the basic physics of field generation in logic switching systems.

The nonstatic current configurations that exist in these systems (**Figure 1**) cannot be treated with static source considerations—that is, the calculation of E(r,t) and B(r,t) per existing source configurations at each time increment cannot be applied for two reasons. First, when there is a current change, the electric and magnetic fields at some given distance experience this change as a result of field disturbances. These disturbances radiate outward from the source at a certain velocity—C in a free space and kC in an enclosed space (k being the material's dielectric constant). The field values at some point at a given time depend on the source configuration at an earlier time—t − (r/c), free-space, where r is the distance to the point in question.

Second, because the fields at the arbitrary point (above) change with respect to time, other fields are generated. From Faraday, a changing magnetic field generates an electric field, or:

$$\S \mathbf{E} \cdot \mathbf{dl} = \frac{-d\phi_B}{dt}$$

and, from Maxwell, a changing electric field generates a magnetic field, or:

$$\S \mathbf{B} \cdot \mathbf{dl} = \mu_0\epsilon_0 \frac{d\phi_E}{dt}$$

This field generation also depends on the speed of flux change—that is, for a particular change in flux, as the frequency of switching increases, the intensity of the generated field increases. This is a problem of special concern in today's efforts to increase switching speeds in logic systems.

Energy Transmitted

The amount of energy transmitted by these fields per unit area is given by a vector term S (the Poynting vector). This vector is a measure of the combined energies of the magnetic and electric components:

$$dU = dU_E + dU_B = (U_E + U_B)(Adx)$$

where Adx is an incremental volume of free space,

$$dU = (\tfrac{1}{2}\epsilon_0 E^2 + \frac{1}{2\mu_0} B^2)(Adx)$$

Using C = E/B,

$$dU = [(\tfrac{1}{2}\epsilon_0 E(cB)] + \frac{1}{2\mu_0} B(E/C)(Adx)$$

After combining terms,

$$dU = \frac{EBAdx}{\mu_0 c}$$

And, finally,

$$S = \frac{dU}{dt} A = \frac{1}{\mu_0} E \times B$$

This equation shows that the amount of energy is a function of the two fields, and the direction of propagation is given vectorially by the right-hand rule.

Figure 2 illustrates this by showing current direction, electric field, B-field (by right-hand rule), and the resulting Poynting vector. The key to shielding, then, is to place an obstacle that will attenuate the signal in the path of the conductor.

For a simple case (normal incidence), **Figure 3** illustrates what occurs when the wave encounters a shield. The incident wave meets the initial interface of the shield and a loss occurs immediately through reflection. The energy transmitted through the first interface is further degraded by energy absorption within the shield and, finally, by a second reflection at the secondary interface.

The absorption component is a function of shield thickness and skin depth, which, in turn, is a function of applied frequency.

The total energy per unit volume transmitted is then a function of the incident energy. To obtain an approximation of this energy for a uniform, homogeneous medium:

$$\mathbf{S_t = C(\omega\epsilon_0/\sigma)e^{-t/\zeta}\ Si}$$

In this equation, C = constant; σ = conductivity; ω = angular velocity; t = shield thickness; ϵ_0 = permittivity; ζ = skin depth.

The permittivity constant ϵ_0 may be derived using the relation $C = (\mu_0\epsilon_0)^{-1/2}$, since the value incorporates the permeability constant, which has an assigned value ($4\pi \times 10^{-7}$ Weber/amp-m) rather than a measured value. The conductivity of the material is the reciprocal of the resistivity:

$$\sigma = 1/\rho = L/RA$$

Angular velocity ω (or, more precisely, the time rate of angular displacement) is related directly to the applied frequency of the incident energy, $\omega = 2\pi f$.

The skin depth or depth of penetration ζ in a "good" conductor is

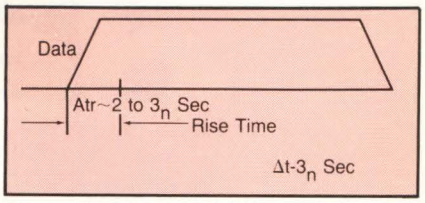


Figure 1: This graph illustrates the current switching profile of a typical TTL output of an integrated circuit.

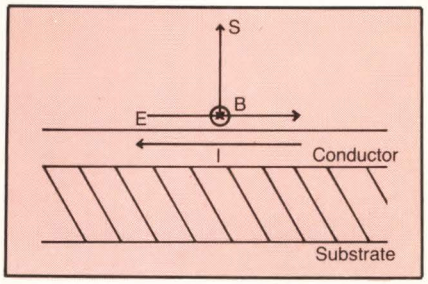


Figure 2: The amount of energy transmitted by a field per unit area is given by the Poynting vector S, which is a measure of the combined energies of the field's magnetic and electric components. The amount of energy is actually a function of the two fields and the direction of propagation is given vectorially by the right-hand rule.

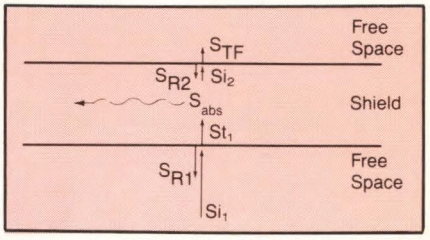


Figure 3: When an incident wave encounters a shield, the wave meets the shield's initial interface and a loss occurs immediately through reflection. Energy transmitted through the first interface is further degraded by energy absorption within the shield and then by another reflection at the secondary interface. (S_{TF} = Transmitted final; S_R = Reflected; S_{abs} = Absorbed)

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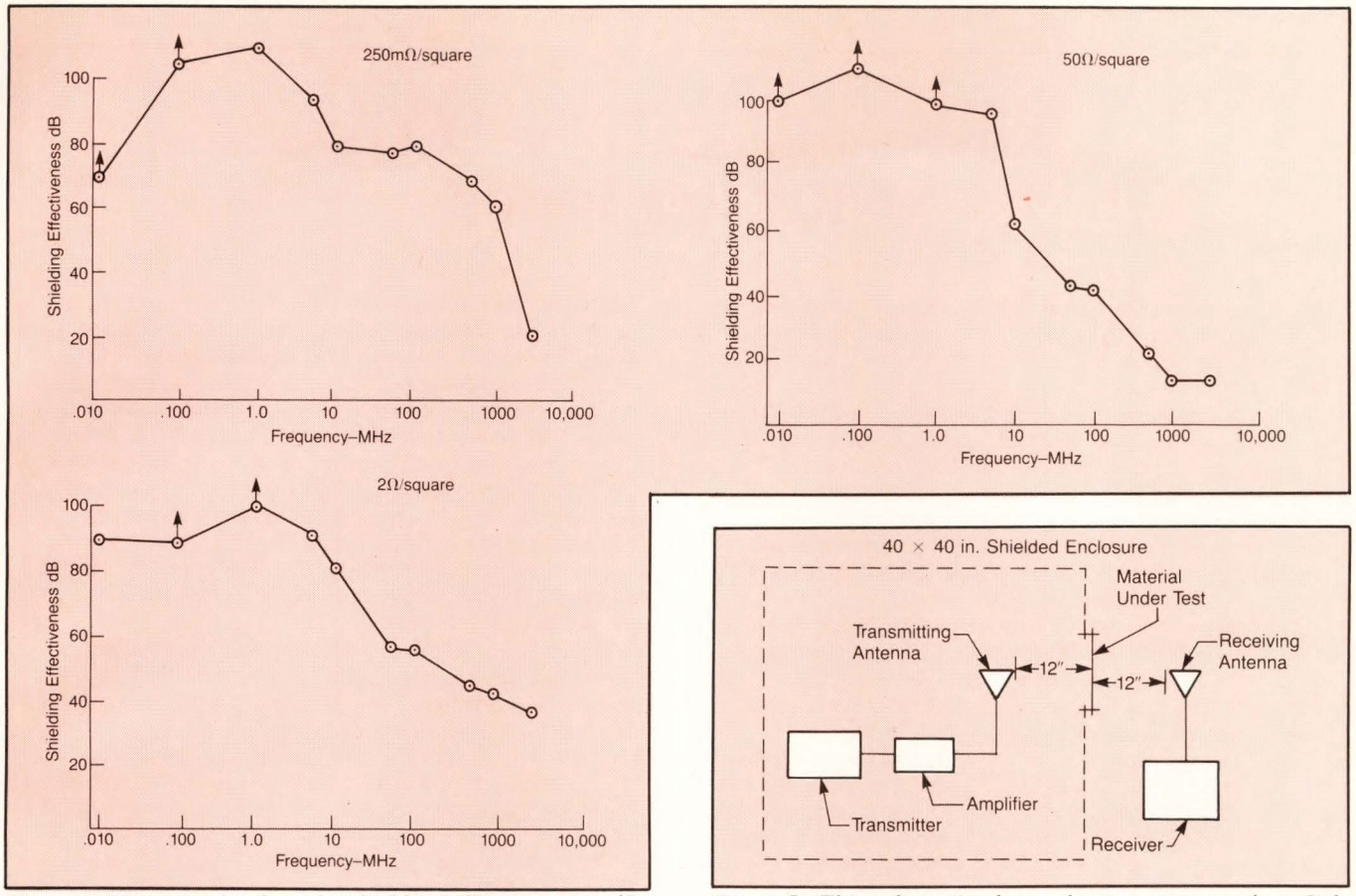

Figure 4: These graphs show the shielding effectiveness in dB of some conductive media.

Figure 5: This schematic shows the test setup used at Oak Switch for determining shielding effectiveness.

FCC Regulations—RFI/EMI Shielding Of Small Computers

The following is a summary of Section 15 of the FCC regulations covering RFI/EMI shielding of small computers.

15.4 (n) Computing Device. This paragraph covers any electronic device or system that generates and uses timing signals or pulses of more than 10,000 pulses (cycles) per second and uses digital techniques; inclusive of telephone equipment that uses digital techniques or any device or system that generates and uses radio frequency energy for data processing functions, such as electronic computations, operations, transformations, recording, filing, sorting, storage, retrieval, or transfer. Radio transmitters, receivers, industrial, scientific, and medical equipment, and any other radio frequency device specifically subject to an emanation requirement are excluded from this definition.

15.4 (o) Class A Computing Devices. A computing device for use in a commercial, industrial, or business environment; exclusive of a device marketed for use by the general public or intended to be used in the home.

15.4 (p) Class B Computing Devices. A computing device marketed for use in a residential environment notwithstanding use to commercial, business, and industrial environment. Examples of such devices include electronic games, personal computers, calculators, and similar electronic devices marketed for use by the general public.

15.4 (g) Personal Computer. An electronic computer marketed for use in the home, notwithstanding business applications. Such computers are considered Class B computing devices. Computers that use a standard TV receiver as a display device or meet these conditions are considered examples of personal computers: marketed through a retail outlet or direct mail order catalog; notices of sale of advertisements are distributed or directed to general public or hobbyist users rather than restricted to commercial users; operates on a battery or 120-volt electrical supply.

15.4 (r) Verification. An approval procedure where the manufacturer or importer takes the necessary steps (including testing) to ensure that the equipment complies with the technical provisions of this part. The unit verified by the manufacturer or importer shall be representative of all future production units. The manufacturer or importer shall be responsible for maintaining records to show what steps were taken to ensure that each device sold complies with the provisions of this part.

Keyboards And The FCC's EMI/RFI Regulations

An important consideration to remember when reading the FCC part 15 regulations is that they encompass the complete system, not only the keyboard, whose emissions are very small compared to the system as a whole. Differences in keyboard switch technologies cause differing rates of emissions. In general, mechanically-based technologies emit less than solid state. This is because solid state keyboards have an AC signal coupled through the switch to indicate a key closure. It is the signal itself that is the source of emissions. However, the signal that passes through this switch has a low power value and causes minor emissions problems.

The biggest problem to be faced by keyboard manufacturers is shielding the electronics. Fully encoded boards use a similar design, sharing a processor, multiplexor, and sense circuitry. The electronics cause emission problems, specifically the processor and crystal.

The low emission levels of the switches in a keyboard can be masked by connecting a ground to the metal keyboard frame, if there is one. If not, a special conductive layer or material must be added. Masking the emissions of electronics is a much more difficult task, but they can be reduced in several ways. By careful layout of the components and keeping the traces as short as possible, emissions can be reduced to meet FCC requirements but not eliminated. The only way of completely masking emissions is to place a grounded conductive shield around the electronics. This is achieved by painting the inside of the keyboard enclosure with a conductive paint and then grounding it. All keyboards have some electronics, whether on a daughter board mounted in the keyboard enclosure or integrated into the host system. When considering a keyboard you should know what is connected to it. The electronics are somewhere and removing them is only passing on the problem. Remember that emissions must be regarded on a total system basis not just as a keyboard.

Key Tronic has had several of its keyboards tested to the FCC Class B level and has been given FCC certification. A result of this testing, which emphasized that the system must be considered as a whole, is that the cable connecting the keyboard to the host system must be shielded. The system must make provisions for connecting the cable shield to ground.

When a keyboard (that meets FCC requirements) is connected to a system (that also meets those requirements) the combination may not meet FCC standards unless the interface is well designed. The primary control on emissions, both radiated and conducted, must come from the host system. If the host system is designed with emissions in mind there should be few problems with the keyboard.

There is no easy solution to the problem of emissions. Because of the economics of the system as a whole, shielding can only be taken to finite limits. Emissions cannot be removed, only reduced to acceptable levels. The earlier the keyboard manufacturer is involved with the design the more effective he/she can be.

Ian G. Evans, Keyboard Marketing Manager, Key Tronic, PO Box 14687, Spokane, WA 99214. (509) 928-8000.

equal to the radian length χ, or $\zeta = \chi = (2/\omega\sigma\mu)^{1/2}$.

A good conductor is one in which the conduction current density is much greater than its displacement current density. The physical meaning of the depth of penetration is the depth of the material that will attenuate the Poynting vector by a factor of $(1/e^2)$, or attenuate the amplitude of the wave by a factor of $(1/e)$.

The skin depth decreases as frequency, conductivity, or permeability increases. What this tells us is that as frequency increases, the required thickness of a given material needed to obtain the same shielding performance decreases.

This leads to a rule of thumb: Design the shield to provide the desired attenuation at the lowest foreseen frequency. In this way, as higher frequencies are encountered, the designed thickness of the material will always provide attenuation greater than the minimum critical limit.

Membrane Keyboard Shielding Design

In the FTM keyboard designed by Oak Switch Systems, an effective ground plane is obtained by using a rigid aluminum supporting plate.

When needed, the low-cost plate functions as many distributed decoupling capacitors to ground potential (assuming a good ground is provided from the aluminum plate to the host ground system).

Also, as **Figure 3** implies, the mounting plate offers a physically lower shielding surface to the membrane switch. An upper shield is applied by simply screening a hybrid conductive medium on the membrane surface. Various options for terminating the metallic surface include connecting the aluminum plate directly, with several eyelets or other fasteners, or grounding to the interfacing flat flex ribbon.

Results of initial testing with this design have shown that the typical attenuated noise level approaches the ambient noise level of a screened room. The three graphs in **Figure 4** show the shielding effectiveness in dB of some conductive media plotted against applied frequency. Variations in sheet resistivity range from 20 mξΩ per square to 80 Ω per square. The test setup is shown schematically in **Figure 5.**

Empirical results indicate the effectiveness of the polymer conductive blends when used to shield the FTM keyboard. □

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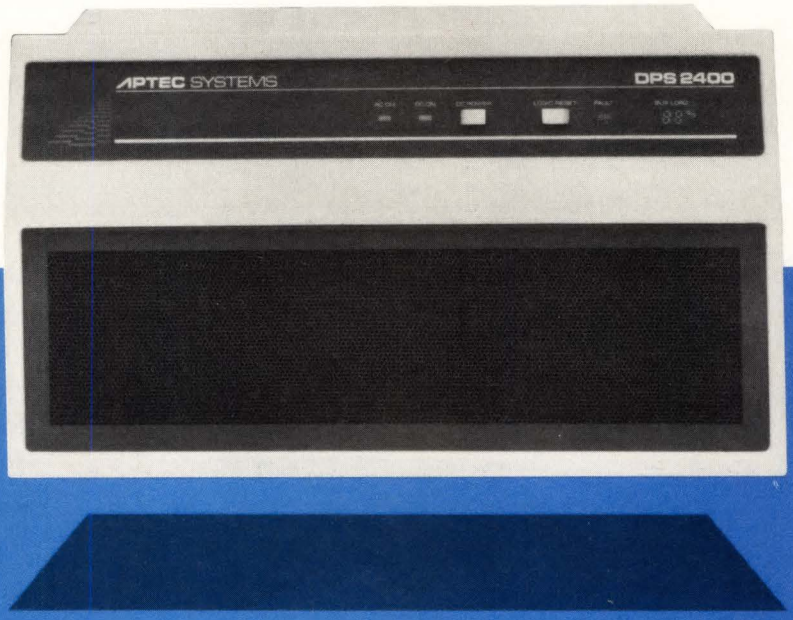

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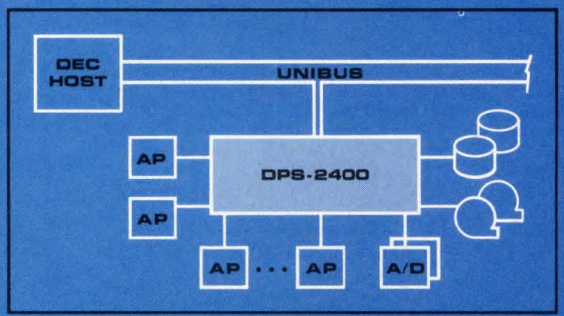

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Real Time Graphics With An Array Processor

The use of an array processor combines the speed of specialized graphics processors with the generality of a high speed pipelined processor.

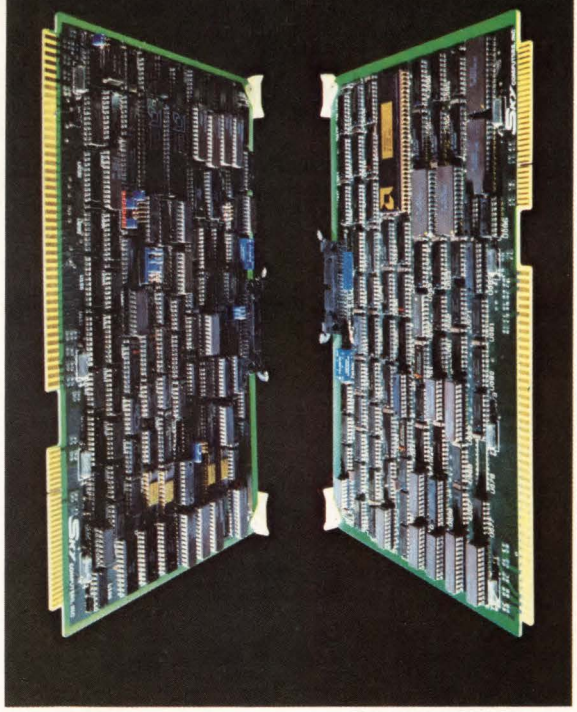

Photo courtesy SKY Computers

by Jay Zagorsky

Matrix operations are the basic building blocks of many graphic operations. Rotating or scaling a three dimensional scene is easily accomplished by changing the point matrix that defines the picture. To operate in real time, however, a graphics program must be able to change the point matrix as fast as the display can be refreshed. By increasing the number of points that define a scene or by increasing the number of times the scene is changed, the illusion of a real time response can be lost. Decreasing speed, however, increases user frustration and lowers productivity. In the step-wise refinement which follows, four methods of performing three dimensional transformations are described. The first two, which use FORTRAN code only, work in real time—but for a limited number of cases. The last two, which use the SKYMNK array processor, perform three dimensional transformations at real time speed in all cases.

Transformation Matrix

Scenes and objects can be rotated, sheared, reflected, translated, locally and overall scaled, and have their perspective changed by simple matrix operations. Any point in the scene can be defined by a one by four row matrix (X, Y, Z, W). X, Y, and Z represent the point's position in the standard coordinate system. W represents the homogeneous coordinates which are used in the transformation of the X, Y, Z. Homogeneous coordinates are useful if the scene's coordinate system is different from the display's coordinate system. For example, if the scene is internally represented as points less than one and the screen is addressed as integers, changing the homogeneous coordinate can map internal points like [.1, .2, .3, 1] to displayable points like [1, 2, 3, 10]. The graphic operations are done by multiplying the points by a 4 × 4 transformation matrix.

The transformation matrix partitions into four sections: A) a 3 × 3 matrix scales, shears, and rotates; B) a 3 × 1 matrix changes the perspective; C) a 1 × 3 matrix produces translation; D) a 1 × 1 matrix does the overall scaling. The matrix multiplications easily code into a FORTRAN routine with triple loops. This algorithm (**Table 1**) is the slowest of the four. It takes .60267 secs to multiply a 64 point scene. With a display refreshing 30 times/sec, this algorithm can use only 1.6 of the refreshes per sec. If used in a graphics program, the user would encounter even slower speeds since the program would also have to handle other computation.

Three refinements can improve the algorithm's speed: First, it can be rewritten in assembly language; second, loops and variable sub-

Number Points	Routine 1 FORTRAN	Routine 2 Optimized	Routine 3 Pivot	Routine 4 Horner's Rule
32	.301	.215	.015	.013
64	.602	.430	.019	.015
128	1.204	.859	.030	.030
256	2.410	1.719	.053	.061
512	4.820	3.437	.102	.122
1024	9.641	6.875	.199	.243
		Time in Seconds		

Table 1: The time it takes for each routine to transform six different length matrices. The timings were run on a PDP-11/23 under RT-11 using Sky Computer's SKYMNK Array Processor.

Jay Zagorsky, Sky Computers, Foot of John St., Lowell, MA 01852. (617) 454-6200.

scripts can be eliminated; and third, it can be customized for a specific matrix. With a good optimizing compiler and the use of the second refinement, recoding in assembly language will not speed up the algorithm to any marked degree. By eliminating the two inner loops, N * 16 loop initializations are bypassed. Time can also be saved by using constant array subscripts, which are computed during compile time instead of during execution time. Recoding the first routine using these methods makes the routine run 33% faster. The algorithm can now compute 2.3 new 64 point frames per sec. But 2.3 frames per sec is still not the required real time speed of 30 frames a sec.

A third way of increasing the algorithm's speed is to customize it to the transformation matrix. If the transformation matrix is sparse, substantial time can be gained by eliminating unneeded multiplies and divides. With this method the transformation algorithm can be made fast enough for real time response. But now it is no longer general. Each type of transformation must now be coded separately. Some of the time that is gained in computing the transformation will be lost in deciding which routine to use.

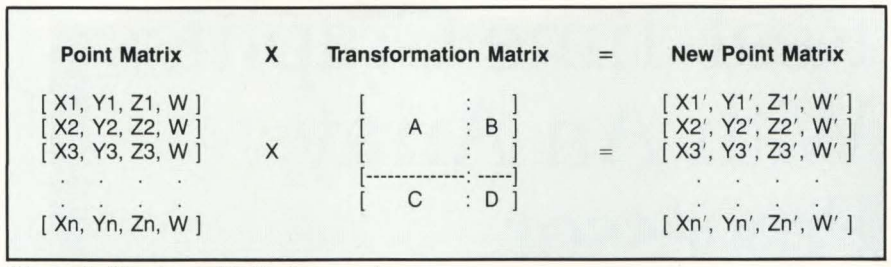

Figure 1: Matrix multiplications code.

```
C----Algorithm one,    N X 4 Matrix transform.
C----Input Matrix      Point(I,1) = X        Point(I,2) = Y        Point(I,3) = Z
C----                  Point(I,4) = Homogeneous Point = 1
C----Output Matrix     PntPrm(I,1) = X       PntPrm(I,2) = Y       PntPrm(I,3) = Z
       DO 20 I = 1,N
         DO 10 J = 1,4
         Tmp2(J) = 0.0
           DO 10 K = 1,4
10         Tmp2(J) = Tmp2(J) + Point(I,K) * Trans(K,J)
C- Homogeneous calculation
       DO 20 K = 1,3
       Point(I,K) = Point(I,K) / Point(I,4)
20     CONTINUE
```

Figure 2: Algorithm One

```
C----Algorithm two, N × 4 Matrix transform optimized.
C----Input vectors X, Y, Z      Output vectors Xprime, Yprime, Zprime
       DO 10 I    =  1,N
       TEMP       =  X(I)*Trans(1,4) + Y(I)*Trans(2,4) + Z(I)*Trans(3,4)
     1                + Trans(4,4)
       Xprime(I)  =  (X(I)*Trans(1,1) + Y(I)*Trans(2,1) + Z(I)*Trans(3,1)
     1                + Trans(4,1)) / TEMP
       Yprime(I)  =  (X(I)*Trans(1,2) + Y(I)*Trans(2,2) + Z(I)*Trans(3,2)
     1                + Trans(4,2)) / TEMP
       Zprime(I)  =  (X(I)*Trans(1,3) + Y(I)*Trans(2,3) + Z(I)*Trans(3,3)
     1                + Trans(4,3)) / TEMP
10     CONTINUE
```

Figure 3: Algorithm Two

Array Processing Power

In order to solve the problem, many specialized graphics processors have been produced. The use of an array processor, however, gives the speed of these specialized units with the generality of a high speed pipelined processor. The array processor efficiently handles all operations on one dimensional arrays or frequently called vectors.

The SKYMNK array processor, used to produce these results, is called like a FORTRAN subroutine. For example, one SKYMNK routine is the vector dot product. The dot product routine multiplies two vectors together element by element and sums these products to produce a real number. Each line of code from the second routine performs a dot product and then a divide. A shortcoming of this method is that it does not take advantage of the array processor's speed on long vectors, since the processor is working only on vectors of length four.

Even more useful and efficient is the vector pivot routine. This routine multiplies a vector by a constant and then adds this vector to a second vector. This allows two distinct operations to be combined. Instead of working with vectors of length four, the pivot routine is working with vectors of length N. The element Trans(1,1) is multiplied by all the elements in the X array. The element Trans(1,2) is multiplied by all elements in the Y array. These two new vectors are added together. By continuing this operation on all elements of the transformation matrix the new matrix can be derived. The vectors and transformation elements that are passed to the pivot routine are each followed by a number. The SKYMNK interprets that as the number of elements to skip in the vector. A zero increment means that the same element is used repeatedly throughout the operation. An increment of one indicates that consecutive elements are to be used, and an increment of two means that every second element is to be used.

Using the array processor, over 52 frames per sec can be calculated. The program is no longer compute-bound but, with 12 frames per sec excess capacity, is I/O bound.

The last routine, which uses Horner's Factoring Rule, eliminates the need for temporary stor-

Image manipulations in seconds, not hours.

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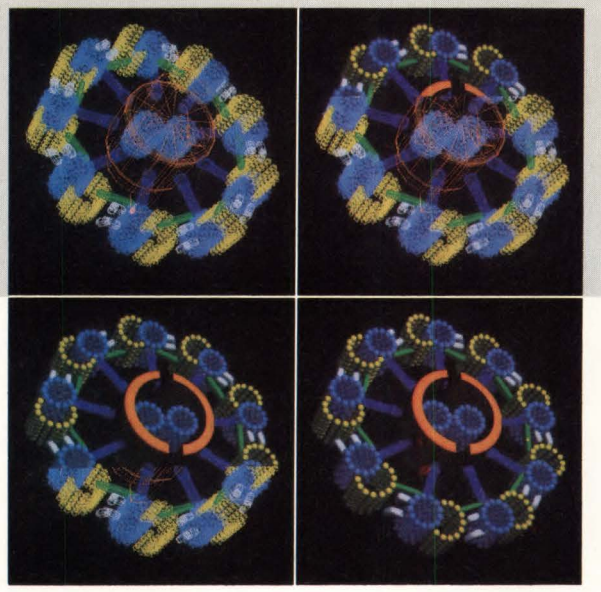

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For tough image processing problems like pixel rotation, picture regeneration, or hidden line removal from wire frame models, Mini-MAP gets results in seconds, not hours. Attach a Mini-MAP, model MM-111, to a PDP-11 UNIBUS and you have an interactive number cruncher that is ideal for image processing, CAD/CAM, solid modeling, simulation, and animation.

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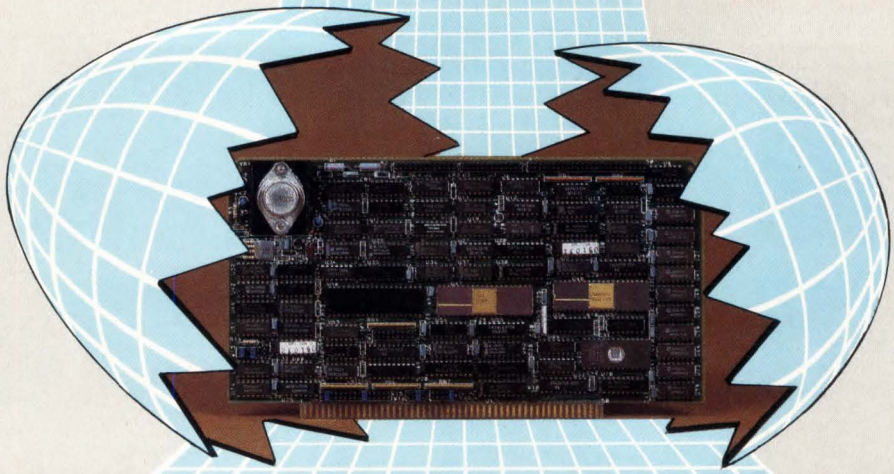

A Third Generation is Born

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A Z80 based microcomputer board with memory and I/O functions

- ***Fully complies with IEEE 696 Standard***
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- Supports CP/M® Plus
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- 64K on board memory, dual ported, parity checked
- 2 serial ports, 1 full SASI port
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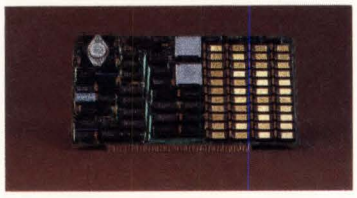

ExpandoRAM IV—Random access memory board utilizing 64K or 256K NMOS RAM chips

- ***Fully complies with IEEEE 696 Standard***
- 256K capacity with 64K chips
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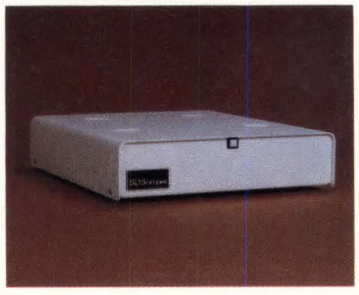

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- Compact size approximately 4" × 14" × 17"
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```
C----Algorithm three, transform using the array processors pivot.
C----Input vectors X, Y, Z                    Output vectors Xprime, Yprime, Zprime
C--- X-POINT CALCULATION
      CALL VPIV (Trans(1,1),0, X(1),1,        Trans(4,1),0,        Tmp1(1),1,   N)
      CALL VPIV (Trans(2,1),0, Y(1),1,        Tmp1(1),1,           Tmp1(1),1,   N)
      CALL VPIV (Trans(3,1),0, Z(1),1,        Tmp1(1),1,           Xprime(1),1, N)
C--- Y-POINT CALCULATION
      CALL VPIV (Trans(1,2),0, X(1),1,        Trans(4,2),0,        Tmp1(1),1,   N)
      CALL VPIV (Trans(2,2),0, Y(1),1,        Tmp1(1),1,           Tmp1(1),1,   N)
      CALL VPIV (Trans(3,2),0, Z(1),1,        Tmp1(1),1,           Yprime(1),1, N)
C--- Z-POINT CALCULATION
      CALL VPIV (Trans(1,3),0, X(1),1,        Trans(4,3),0,        Tmp1(1),1,   N)
      CALL VPIV (Trans(2,3),0, Y(1),1,        Tmp1(1),1,           Tmp1(1),1,   N)
      CALL VPIV (Trans(3,3),0, Z(1),1,        Tmp1(1),1,           Zprime(1),1, N)
C--- W-POINT CALCULATION
      CALL VPIV (Trans(1,4),0, X(1),1,        Trans(4,4),0,        Tmp1(1),1,   N)
      CALL VPIV (Trans(2,4),0, Y(1),1,        Tmp1(1),1,           Tmp1(1),1,   N)
      CALL VPIV (Trans(3,4),0, Z(1),1,        Tmp1(1),1,           Tmp1(1),1,   N)
      CALL VWAIT
C--- CONVERT BACK TO HOMOGENEOUS COORDINATES
      CALL VDIV (Xprime(1),1, Tmp1(1),1, Xprime(1),1, N)
      CALL VDIV (Yprime(1),1, Tmp1(1),1, Yprime(1),1, N)
      CALL VDIV (Zprime(1),1, Tmp1(1),1, Zprime(1),1, N)
```

Figure 4: Algorithm Three

(Xvector * T(1,1) + (Yvector * T(2,1) + (Zvector * T(3,1) + T(4,1)

Horner's Rule says that this can be converted into:

(((((Xvector * T1′) + Yvector) * T2′) + Zvector) * T3′ + T4

where T1′ and T2′ are:

T1′ = T(1,1) / T(2,1) T3′ = T(3,1)

T2′ = T(2,1) / T(3,1) T4′ = T(4,1)

Figure 5: Solution in the X dimension.

Do T1PRM	*	X vector	=>	Accumulator
Do Y vector	+	Accumulator	=>	Accumulator
Do T2PRM	*	Accumulator	=>	Accumulator
Do Z vector	+	Accumulator	=>	Accumulator
Do T3	*	Accumulator	=>	Accumulator
Do T4	+	Accumulator	=>	Accumulator
Do Accumulator / W Vector			=>	Answer Vector

Figure 6: Coded elements of transform matrix column.

age, and optimizes sparse matrices. Horner's Rule used once for each dimension optimizes the code done for each transformation matrix. Solving in the X dimension, the Pivot routine uses:

Temporary storage is eliminated by placing the intermediate values in the array processor's internal accumulator, which is 64 real numbers long. Sparse Matrices are automatically optimized by Horner's Rule, for it must look at all values of the transformation in order to avoid a host computer zero divide. By examining the values of Trans at the start of the routine, cases where the transformation matrix is zero can factor into trivial cases. For example, if T1 and T2 are not equal to 0 but T2 and T3 are equal to 0, then the expression factors into Xvector * T1 + T4. By checking all sixteen cases the most efficient array processor code is executed for each transformation. The expressions easily transform into array processor calls. The worst case, where all elements of a transform matrix column are non zero, is coded:

The Horner's Rule takes only .015 sec to compute the 64 point scene. This is a rate of almost 64 frames per sec. Even with a double buffered display the program is still I/O bound. This rate is far faster than the 1.5 frames/sec that the original FORTRAN algorithm computed.

The final step to increasing the speed is to micro-code the algorithm and implement the routine directly in the array processor's firmware. One estimation is that the times for computing the matrix will be ten times faster than the Horner's Rule times. For many applications this additional speed will not be needed, but as graphics displays grow faster and objects grow even more complex the extra speed will be used.

The Horner's Rule timings were produced using the worst case transformation matrix. The Pivot routine, even though it needs a temporary vector and does not optimize for each transformation matrix, is simple to program. It is only 16 lines of code, while the Horner's Rule is almost 200 lines long. Unless many sparse transformation matrices are used, or memory is a factor, the simple to program Pivot method is superior to Horner's Rule.

The array processor has other advantages, in addition to speed, doing matrix processing. The array processor computes the transformation in either 32 or 48 bit floating point format so no accuracy is lost. Secondly, the array processor works in parallel with the host so that other processing can occur simultaneously. Most importantly, the array processor can be used to speed set-up time. After coding the transformation in the array processor the time taken in computing the 4 × 4 transformation matrix can become a rate determining step. Computing these values in the array processor can decrease overall time. Vectoring the algorithm changes the transformation program from compute bound to I/O bound. At this point both the complexity of the frame and the speed at which it is changed can be increased at no detriment to real time graphics speeds.

Summary

Four general algorithms to do three dimensional matrix transformations were examined in this article. By utilizing the array processor, real time response is achieved in three dimensional graphics, a response rate which increases users' productivity and decreases their frustration.

□

FIFO Buffers Insure Continuous Array Processor Performance

by Andy Lukas

In a typical array processor, a special purpose μC generates addresses, the memory system provides data at rates over 10 Mbytes/sec., and the floating point processor performs the required arithmetic operations. These independent units are linked together through general purpose control and data buses. Special purpose peripherals also have access to the memory system. First-in, first-out buffers (FIFOs) may be used in the interface between these elements to permit continuous computation rates up to 5 million floating point operations per second.

Array Processor Architecture

In a complex vector by vector multiply, a typical array processor function, the following operations are concurrently performed every 1.6 μsecs:

- Generate 2–input and 1–output addresses.
- Read two complex data (64-bits each) and write one complex datum.
- Compute 4 floating point multiplies and 2 floating point add/subtracts.

A brief review of the architecture will highlight the importance of the FIFOs; **Figure 1** summarizes the key elements and buses.

The Instruction Set Processor (ISP) is a 32-bit stored program μC. Its eight 2901 ALUs can calculate array addresses at a rate of 200 nsecs per address. It controls the Floating Point Processor with command directives over its control bus. The ISP microcode also implements a minicomputer instruction set used for overall array processor control.

The Floating Point Processor (FPP) performs high speed arithmetics with a 400 nsec floating point multiplier and 400 nsec floating point ALU. The FPP Memory Interface Unit contains FIFOs holding the addresses generated by the ISP and FIFOs buffering the data between the FPP and memory system.

Today's array processors achieve high performance through the use of multiple processing elements.

The memory system contains the high speed 64K × 1 bit dynamic RAMs used for storing data, coefficients and control programs. The memory can be accessed one 32-bit word at a time, but devices will often ask for, or provide, a burst of data if convenient. For example, the ISP mini-instruction pre-fetcher always reads 64 bits of data. Similarly, whenever the FPP is reading or writing complex numbers, two 32-bit words will be burst-accessed.

This feature takes advantage of the two banks of interleaved memory. A single memory read (32-bit) takes 400 nsecs. In multiple word burst reads, the next 32-bits are available 100 nsecs later. FIFO buffers at the requesting device handle this high data rate.

The DPG raster display generator takes data directly from the memory system and displays it on a high resolution monitor. It can operate concurrently with the execution of array operations.

High speed transfers of commands and data between the units are implemented using a data bus and a control bus.

Data Bus

The Localbus is used for data transfers between the ISP, FPP, or DPG and the memory system. It is a high speed synchronous arbitrated data/address bus which cycles in 100 nsecs. During each cycle, a 32-bit address or a 32-bit data can be

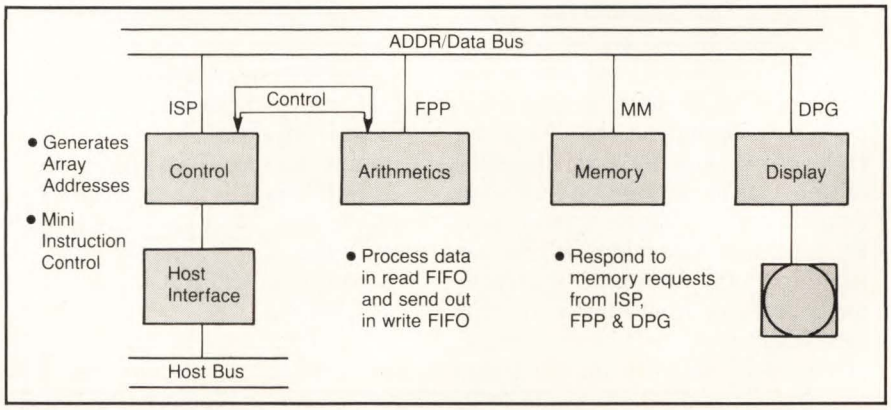


Figure 1: Array processor elements and buses.

Andy Lukas, Product Manager, Computer Design & Applications Inc., 411 Waverly Oaks Rd., Waltham, MA 02154.

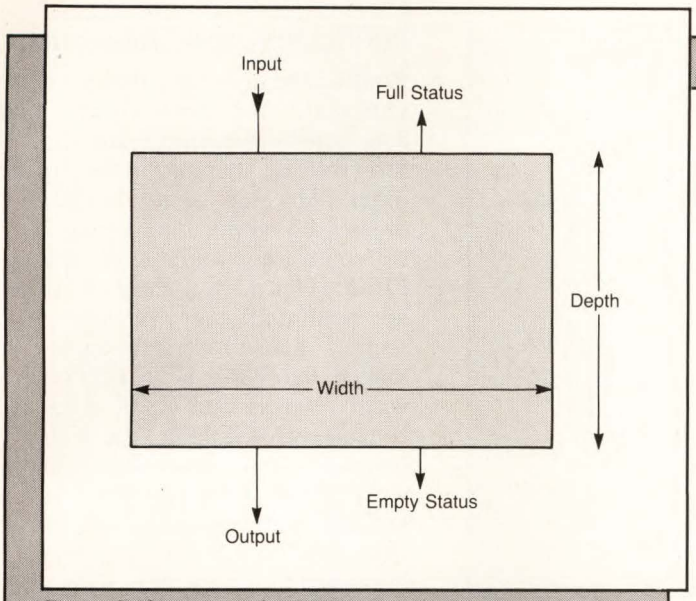
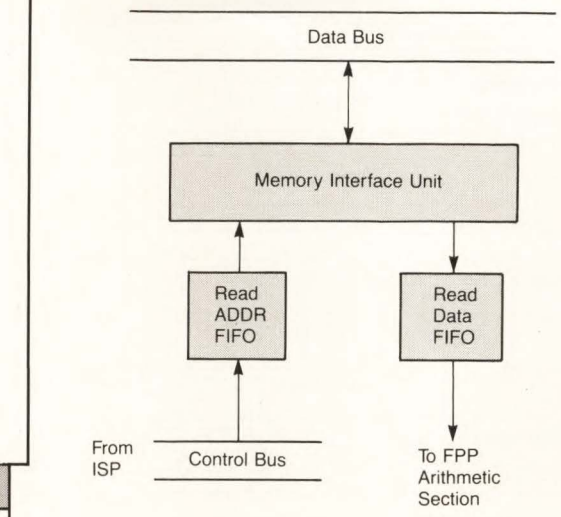


Figure 2: Structure of a FIFO.

Figure 3: Read address/data FIFOs.



transferred.

Similar to contemporary minicomputers, such as DEC's VAX, deferred reads are used to ensure that the Localbus does not become busy due to memory access times. In a deferred read, the requesting device places a 32-bit address on the bus, then releases it. After the data is accessed from memory, it is placed on the bus with the destination device number. Only two 100 nsec bus cycles are required for a 32-bit data read. Overlapped read and write transactions may occur simultaneously.

Multiple word read and write formats take advantage of the two-way interleaved memory. Two 32-bit data reads or writes can be initiated with a single address. FIFOs in each of the independent processors hold the data until it is needed.

Control Bus

An additional bus provides the ISP direct access to registers and FIFOs in the FPP. This 32-bit bus is an extension of the ISP's microarchitecture off-board and allows intimate high speed control where necessary. The ISP can load FIFOs on the bus at a 200 nsec rate.

FIFO Buffers In Computers

Stacks or last-in first-out (LIFO) buffers are commonly used in contemporary GP computers to simplify user access for temporary storage. This structure is effective for subroutine linkage where items are retrieved in the reverse of the order in which they were stored. LIFO stacks are a key element of the PDP-11 and VAX architectures.

Multiple word read and write formats take advantage of the two-way interleaved memory.

FIFO buffers are generally found in computer interfaces for high speed devices such as disks (**Figure 2**). In these cases, the data must be read in the same order as it is loaded. FIFOs buffer data between two devices with different speeds and availabilities. The device loading the FIFO makes sure space is available; the device reading the FIFO waits for data then transfers it out at its own rate. The depth of the FIFO is an important design consideration. It is a function of the difference in the loading and reading rate. It can vary from 2 words for a simple control interface to 1024 or more words for a high speed disk.

Nine FIFOs in the MSP-3000 smooth the flow of data between the ISP, FPP, memory and display. These buffers eliminate the "wait" state often encountered in general purpose computers. **Table 1** briefly introduces each of these structures.

FPP/Memory Interface

The Read and Write Address FIFOs hold the data addresses for the Floating Point Processors Memory Interface Unit. These FIFOs may be continuously loaded by the ISP. Each FIFO stores up to eight 32 bit addresses.

The Read and Write Data FIFOs are each sixteen 32-bit words. The Memory Interface Unit attempts to keep the Read Data FIFO as full as possible using addresses provided by the Read Address FIFO. Similarly, the Write Data FIFO is emptied as quickly as possible using addresses available in the Write Address FIFO.

Often a single address in the address FIFO is used to invoke a complex read or write. For this reason, the data FIFOs are twice as

Name	Function	Width	Depth
FPP/Memory Interface	Read Address	32	8
	Write Address	32	8
	Read Data	32	16
	Write Data	32	16
Instruction Prefetch	ISP Mini-Instruction	16	8
FPP Instruction	Directives from ISP	16	4
Memory	Address	32	2
	Write Data	32	4
Display Input	Data from Memory	32	64

Table 1: MSP-3000 FIFOs.

long as the address FIFOs.

Getting Data Into The FPP

The combination of the read address FIFO and read data FIFO ensures that data is always available for the floating point processor (**Figure 3**).

Following the path of a single data access, the following events occur. The ISP generates a 32-bit data address that is loaded over the control bus into the read address FIFO if space is available. If not, the ISP loops on a microcondition until the FIFO is no longer full. The FPP Memory Interface unit then requests a memory read only if the read data FIFO is not full. When the read data is returned, it is loaded into the Read Data FIFO. If the FPP arithmetic section tries to access an empty Read Data FIFO, the FPP will automatically suspend operation until this resource is available.

Putting Processed Data Back

Routing the addresses into separate read and write FIFOs ensures that data will be accessed from and returned to the memory in the proper order. The ISP sends 32-bit addresses of output data arrays over the control bus to the write address FIFO (**Figure 4**). These numbers are held until the FPP arithmetic section has processed data and loaded the Write Data FIFO. If a write address and write data are concurrently available, the Memory Interface Unit initiates a memory write. The FPP arithmetic section will automatically stall if the Write Data FIFO is full. As soon as space in the FIFO is available, FPP operation will resume.

Instruction Prefetch FIFO

To significantly increase mini-instruction execution speed, the Instruction Set Processor contains an instruction prefetcher with an eight word FIFO (**Figure 5**). Microcode interprets the instruction set while independent logic loads the FIFO. Mini-instruction execution rates vary from 400 nsecs to several μsecs. As in any pipelined instruction execution architecture, the FIFO must be cleared if a program branch is taken.

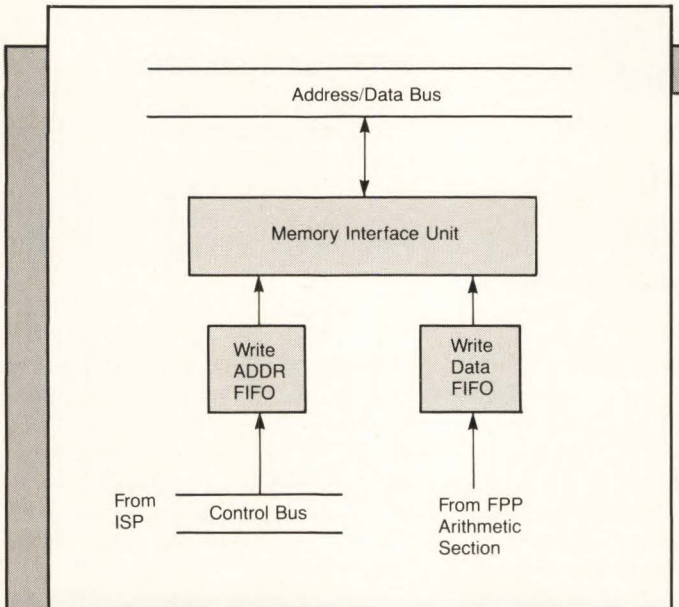


Figure 4: Write address/data FIFOs.

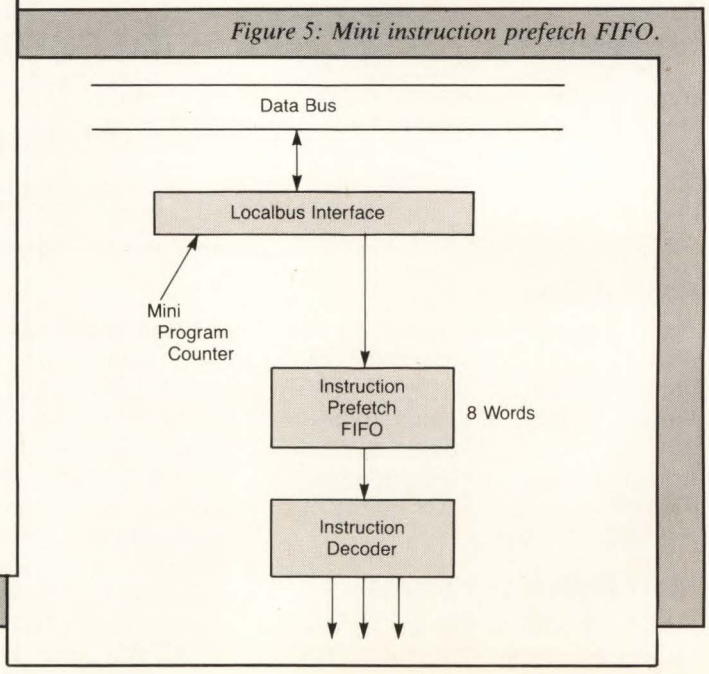
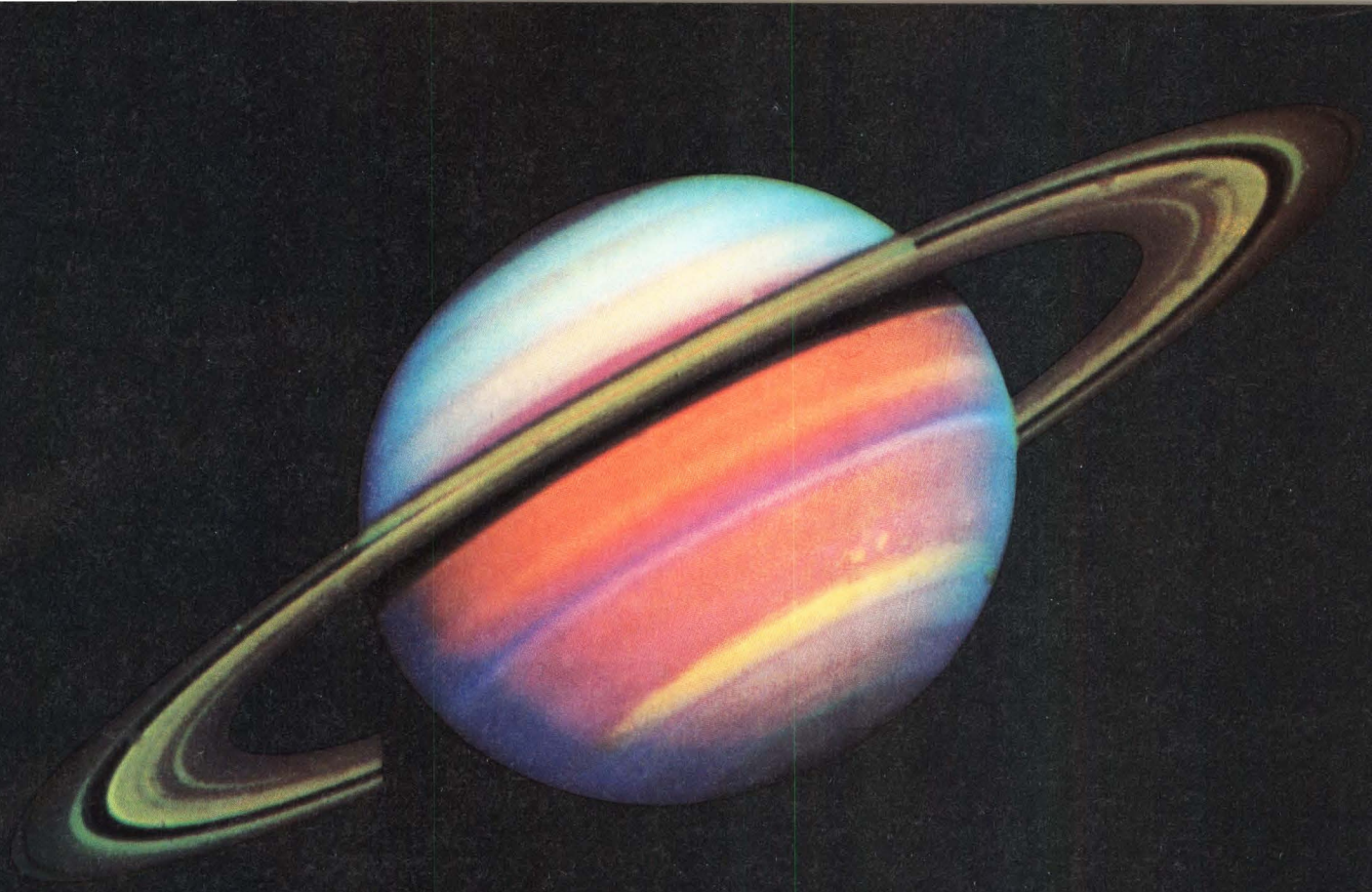


Figure 5: Mini instruction prefetch FIFO.



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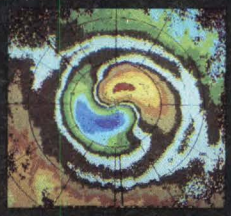

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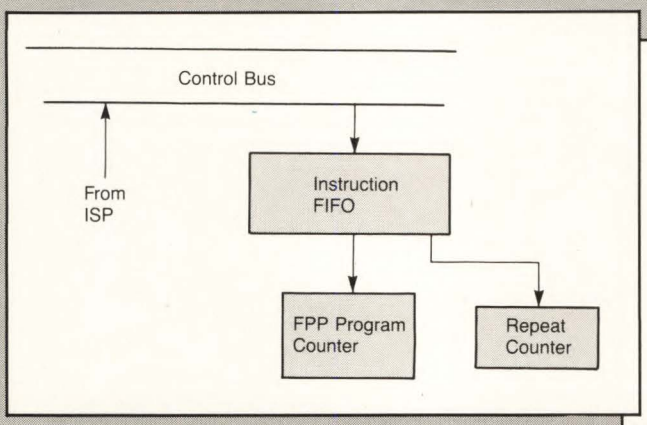
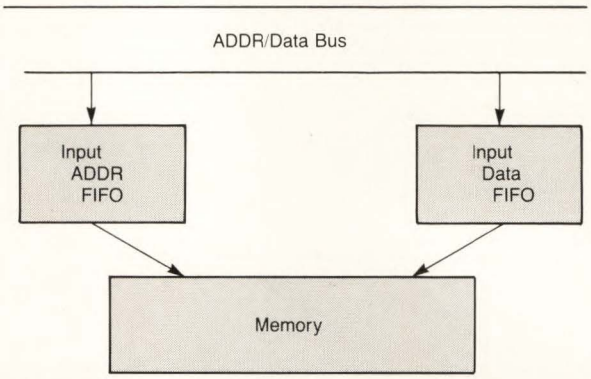


Figure 6: FPP instruction FIFO.

Figure 7: Memory FIFOs.



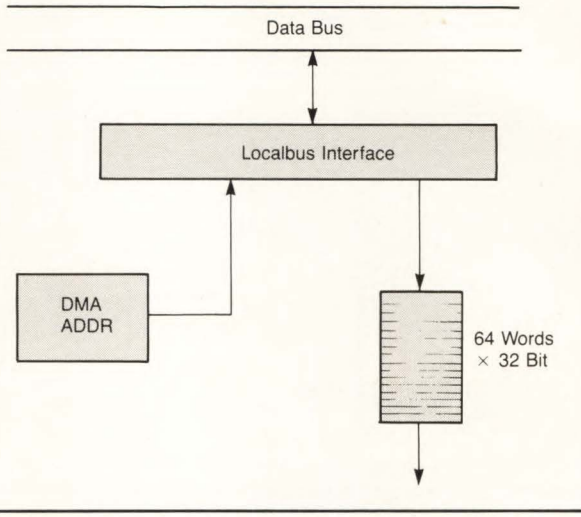


Figure 8: Display data FIFO.

ISP To FPP Instruction FIFO

The Instruction FIFO lets the ISP provide directives to the FPP and is 4 words deep (**Figure 6**). The instruction consists of an FPP opcode or a repeat field. The Opcode selects a particular Microroutine and the repeat count specifies the number of times to repeat this routine. For example, if the square root function is applied to an array of 1000 elements, the address of the square root arithmetic microcode and a repeat count of 1000 are loaded into the Instruction FIFO.

Memory Input FIFO

The key to high performance is having data there when you need it. This is especially true for the memory system (**Figure 7**). A 2 word deep input address FIFO and a 4 word deep input data FIFO insure that the memory can be used at its maximum rate. Before a device like the FPP writes into memory, it checks that these FIFOs are not full.

Display Data FIFO

The MSP-3000 has a high speed raster display controller directly on its data bus. The display data FIFO (**Figure 8**) ensures that the screen refresh in uninterrupted. This is the longest FIFO in the array processor because data is retrieved in large blocks. When the display board gets control of the high speed bus, it requests data in blocks of thirty-two, 32-bit words. Data is transferred from the memory system at a rate of 4 bytes per 100 nsecs and loaded into the FIFO. The bus is then available for other devices such as the Floating Point Processor.

FIFOs And The Programmer

In many array processors, the programmer must be acutely aware of memory and interface timing relationships. FIFOs provide the obvious direct benefit of eliminating any concern of the sequence and timing of data interchange operations.

Extensive use of FIFOs in the array processor has another direct benefit to the microprogrammer: micro instructions control the transfer of data between registers, the sequence and timing of events, the selection of operands and the specification of arithmetic functions.

FIFOs permit linking of the address generator (ISP) and arithmetic processor (FPP) into a powerful system. The programmer can specify independent addressing sequences and separate arithmetic functions. A single ISP addressing routine will often support a dozen array operations. For example, the VOPV program produces addresses for one input vector and one output vector. This addressing function is used by vector move, negate, reciprocal, scalar add, scalar multiply, square, absolute value, threshold, log, exponental and many others.

In some cases, creating a new array operation requires only a new addressing sequence or a new data calculation program. □

Analogic's AP500, the Emancipated Array Processor

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The Emancipation

Analogic's AP500 32-bit Floating Point Array Processor is the first truly independent array processor. It offers the performance and throughput capabilities needed to meet most time-critical, complex, and I/O-bound applications.

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The AP500 supports virtually ANY system configuration. You can build your system from a wide range of Multibus-compatible peripherals including disks, tapes, A/Ds, D/As, display monitors, CPUs and LAN controllers; or configure data acquisition and data display devices to the high-speed Auxiliary I/O Ports.

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CP/M '83 And UNICOM Highlights

Operating system and language refinements in a stable software industry are good news for applications software developers.

by Doug Eidsmore,
West Coast Technical Editor

If the CP/M '83 and UNICOM shows are reliable windows into the software world, the trend at the moment seems to be stability. Not that the heady growth of the software industry is expected to diminish, for any forecaster worth his salt is still predicting system software will outstrip the cost of hardware in the 80s, but the industry has matured. Buzzwords at both shows included: documentation, accessibility, standards and support.

It was no surprise that Digital Research and Bell Labs dominated both shows. At CP/M '83 Digital Research announced a host of new software products. At UNICOM Bell Labs released UNIX System V, a refined System III. Converting from System III to System V is expected to be much less cumbersome than making a Version 7 to System III conversion; one reason is that Bell will be supporting their software for the first time, supplying license holders with transition documents.

CP/M '83 was the first computer conference for suppliers of software, hardware and related services for the CP/M operating system. Developed by Gary Kildall in the mid-70s using Intel's PL/M language, CP/M was the first disk based 8-bit operating system and was licensed for internal applications at computer manufacturing companies in 1975. By 1976 the demand was great enough that Kildall formed Digital Research to support the product.

CP/M Compatible Hardware

Microcomputer mania owes as much to standardized system software such as operating systems, graphics languages and programming tools as it does to low cost, reliable μC based hardware.

Digital Research products are compatible with the 8080, 8085, Z80, 8086, 8088, 80286, 68000, and Z8000. Currently 700 computer manufacturers and system integrators offer the company's products on their μCs.

NCR (Dayton, OH) released single and dual processor NCR Decision Mate V personal computers at the show. The single processor model runs CP/M-80 and the dual processor model runs CP/M-80, CP/M-86 or MS-DOS. NCR is also licensed to make CP/M Plus, Concurrent CP/M, CP/NET and CP/M graphics software available.

NCR also announced the Decision Net local area network. The Omninet-based system transmits at 1 Mbit/s over a twisted pair cable. Up to 64 devices can be linked. A file sharer (dubbed NCR Modus) allows personal computers to share memory and peripherals. The LAN sells for $9,995 plus $500 per computer connection. The 8-bit monochrome computer is priced at $2,800 and the dual processor model with color starts at $3,340. Both machines come with dual disks, 64 Kbytes RAM and high speed graphics. The 8-bit computer is available now and the other products will be available in June.

Three companies announced multiprocessor/multiuser systems that allow for the addition of processing power as the number of users increases.

MicroSystems International (Natick, MA) released their CP/M compatible computer, the MultiNet System. Designed for OEMs and systems integrators, the S100/IEEE 696 based computer has a Z80A based central processor that manages up to 8 users. Each user has his own dedicated 8- or 16-bit processor card. The 8-bit Z80 processor runs CP/M-80 and has 128-K of memory; the 16-bit 8086 processor with optional 8087 runs CP/M-86, and includes up to 1 Mbyte of memory. 8- and 16-bit programs can be mixed and run simultaneously on the distributed processing system bus. The basic two-user system with a 20 Mbyte 5¼" Winchester, ¼" tape and 1.2 Mbyte 8" floppy costs $9,995. Up to 16 systems can be networked and accommodate up to 150 users.

Molecular Computer (San Jose, CA) demonstrated their new enhanced Supermicro, the " X " series. Boasting four times the File

Processor memory and twice the disk capacity and bus transfer rates over their previous 64- and 32-user systems, the Supermicro 64X and Supermicro 32X feature a multiprocessor architecture. Each user has an application processor with a Z80A and 64K RAM and a file processor that manages disk and peripheral sharing. The application and file processors are all linked by a proprietary high speed contention bus design that uses a Carrier Sense Multiple Access with Collision Detection protocol to reduce system overhead. The series is compatible with CP/M and CP/M-86 application software. The top of the line 64X with 136-Mbyte hard disk, 500-Kbyte floppy and 32 application slots lists for $22,995. The 32x with a 60-Mbyte Winchester and a floppy is priced at $18,995.

Action Computer Enterprise (Pasadena, CA) announced 8- and 16-bit multiprocessor systems including a single board user processor designed to take advantage of Digital Research's newest 8-bit operating system CP/M Plus. Designated dpc-183, the processor will support large 32 Mbyte files and 512 Mbytes per logical drive, password protection, time/date stamping and I/O device reassignment. The processor is used in the company's Discovery Multiprocessor system.

Running CP/M And UNIX

The ability to run programs under both CP/M and UNIX gives application software developers the best of both worlds. A new Digital Research "C" compiler permits independent software vendors to write programs that can be ported between versions of CP/M and other operating systems. This initial version of the "C" compiler was designed for use with 16-bit 8086- and 8088-based machines, and is compatible with Bell Labs' UNIX Version 7. The new language is a complete implementation of "C" and includes single and double precision floating point with 8087 math co-processor support. A relocating linker and assembler are part of the package. The compiler has many features of the UNIX program LINT, an error checking program.

TouchStone Software (Seal Beach, CA) has developed a UNIX subsystem that provides compatibility with CP/M programs and files. It can be used either to transfer existing systems in use on a Z80 μC to a UNIX system, or to use UNIX to develop CP/M applications. MIMIX modules and programs will transfer files between CP/M and UNIX systems. It is capable of structuring CP/M files into "pseudo-disks" running under UNIX. It then executes the transferred control program, application program, and related files with full support of Z80 instructions and CP/M calls.

For example, MIMIX was adapted for Zilog's System 8000 by TouchStone. Simulating Z80 CP/M operations gives the 16-bit multiuser system compatibility with Z80 object programs which run under CP/M and their associated files. The Zilog package includes a set of UNIX commands for CP/M file transfers and features user-friendly menu operation. The interactive nature of this link allows the entire CP/M system to be used as a slave processor to the System 8000. MIMIX for the System 8000 will be available from Zilog (Campbell, CA) beginning in March 1983. It is priced at $1,000 per copy.

Friendlier Computing

Gary Kildall is high on LOGO as the home computer programming language of the 80s. Most often thought of as a programming language for children, LOGO has been running for some time on TI 99/4, Apple II and Radio Shack computers and was recently made available on Atari home computers. Digital Research's DR LOGO is an enhanced version of Apple LOGO with "LISP like" features that Kildall feels will provide a friendly programming environment for professionals as well.

DR LOGO is a 16-bit language and runs on the IBM PC and on the TI Professional Computer. It takes advantage of the address space of 16-bit computers, with over 100,000 workspace nodes. Workspace commands provide capabilities found in Apple LOGO, plus additional commands that allow cross-referencing. For example, FOLLOW is used to reorder procedures. DR LOGO also features text windowing, upper/lower case characters, string processing, and a full screen editor. It is expected to sell for under $200.

User-friendly should imply a universal user interface. Such an interface would allow a user to use information from one application program in another program. Apple's LISA has such an interface linking its six application programs.

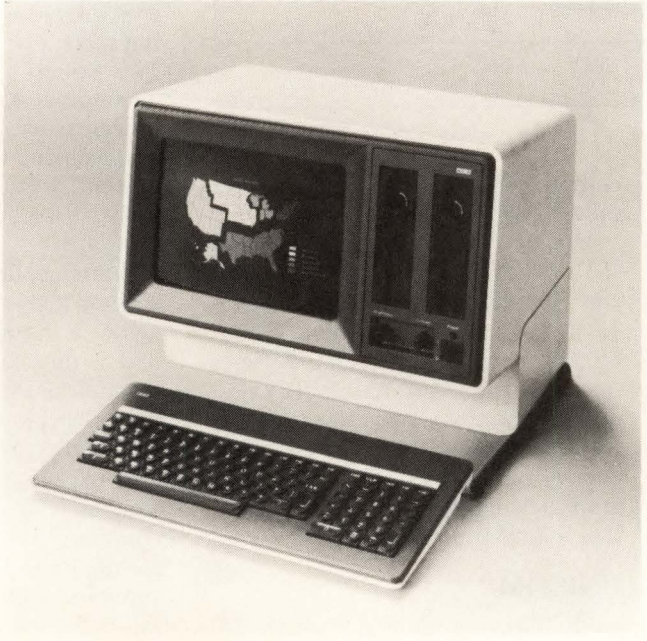

Figure 1: NCR Decision Mate V has external plugs allowing users to add peripherals, memory and a diagnostic module without opening the cabinet.

Figure 2: Multinet is an integrated multiuser system with hard disk and streaming tape.

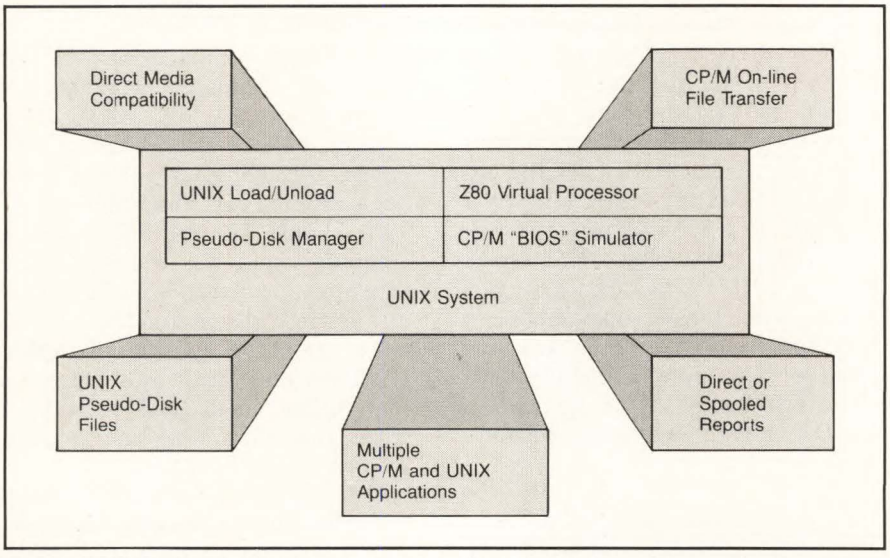

Figure 3: MIMIX subsystem runs CP/M on UNIX systems.

Software vendors are working on similar systems. VISICORP's (San Jose, CA) VISIOn, is an umbrella interface covering application programs. Multiple windowing allows users to simultaneously view or combine information from a spread sheet and word processing package, for example.

More than 35 companies distribute RM/COBOL for CP/M and CP/M 86 systems. RM/COBOL was recently installed on the DECmate II by Ryan-McFarland (Rolling Hills, CA). Availability of RM/COBOL means that users of the DEC computer have access to approximately 300 software packages.

Does the world need a friendlier BASIC? APCBASIC, from American Planning Corp (Alexandria, VA), runs under CP/M and CP/M-86, and is claimed to run 2–5 times faster than garden variety BASIC. The company says features such as trace/conditional trace, cross-referencing and global edit reduce program development time up to 25%. It is available now for $400.

UNICOM

UNICOM was the first joint UNIX user conference. Sponsored by O/USR/Group, the USENIX Association and the Software Tools Users Group, participants included people from technical and commercial communities.

UNIX is to the 16-bit mini and high end micro world what CP/M is to the 8-bit world. UNIX development was begun by Bell Telephone Laboratories in 1969, with the goal of designing an operating system that would support coordinated teams of programmers in the development of application programs. Early UNIX users were all within Bell Labs. As late as 1979, Bell System installations dominated UNIX sites with 55% of the total user population; the bulk of the remaining users were universities and government institutions. Only 3% of the user sites were commercial. These proportions have changed dramatically. By the second quarter of 1982, Bell System users were second to commercial users who had grown to represent 54% of the total user population. By the end of 1983, it is estimated that commercial licensees will be approximately 93% of the user population.

At UNICOM Bell announced the availability of UNIX System V for internal and commercial users. (System 4.0 was an internal OS and was never made available commercially.) "Performance enhancement is the significant improvement that is available with the UNIX operating system V," according to AT&T's W. Robert Guffey, Director of Technology Licensing. Of equal significance to end-users was the announcement that Bell will support System V; the first time the company has supported external software.

Source code licensees can receive several levels of support which include a hotline, system updates, and a newsletter. Improved documentation that is targeted to end-users, programmers, and system developers will be offered. Bell also expressed the desire to make System V a machine independent commercial operating system and, for the first time, will work with the software industry in determining the evolution of future releases.

UNIX System V incorporates over 1,000 modifications that were requested by System III users, and includes a screen oriented editor for use with asynchronous CRT terminals that was developed at the University of California at Berkeley. 1 Kbyte block file systems are supported on VAX series equipment and the larger block size results in significantly improved file system throughout. Internal algorithms have been improved, resulting in improved computation and data throughput. Source code for UNIX System V is available on the VAX 11/780, VAX 11/750 and PDP-11/70 computers.

"C" is an integral part of UNIX Operating Systems. System V offers enhancements to the C language, along with several new language utilities which ease program development. The operating system also contains an enhanced version of FORTRAN 77, containing both compile and run-time improvements over previous versions.

UNIX Compatible Hardware

Cosmos Systems (Sunnyvale, CA) revealed their MC68000 based μC series. Designated the Starfield Series, all of the computers are Multibus compatible and run Bell Labs' V.7 UNIX with Berkeley enhancements. Intended for OEMs and system integrators, Antares was designed to support large development projects. It has been configured with a fully integrated 40 Mbyte 8" Winchester disk drive for program and data storage and a ¼" streaming tape for quick backup. A 16 channel intelligent I/O multiplexor interfaces the micro to 8 or 16 modems or terminals. The standard Antares system is supplied with "C"; Pascal, Cobol, Fortran and Basic are available as options. The standard Antares configuration is priced in quantity one at $25,950 and quantity discounts are available.

Perkin-Elmer Corp. (Oceanport, NJ) announced the availability of a minicomputer system based on the Edition VII Workbench version of the UNIX from the Woolongong Group. The minicomputer is based on Perkin-Elmer's Model 3210. Priced at $49,950, the system includes ½ Mbyte of memory, 64 Mbyte of disk memory, 8 communications lines, a console terminal, and an 8-port Edition VII Workbench license. Options include a 96 Mbyte disk drive, substitution of 1 Mbyte or 2 Mbyte of memory expansion in place of the 512 Kbyte offered, 8 port expansion, and one week of installation and training.

The two major systems software vendors are striving to create a stable environment for applications software developers and systems integrators.

Software Products

Interactive Systems Corp. (Santa Monica, CA) announced a family of UNIX-based software products for increasing productivity in software development and documentation efforts. The top of the line is called the Advanced Productivity System (APS). APS includes facilities for the development and maintenance of programs, for the control of changes, for electronic mail, and for the preparation of technical publications or other documents. Intended for use in all types of programming groups, it can be used to develop programs for mainframe computers, minicomputers, and μPs. Prices for new installations range from $11,000 to $47,500 and include licensing, installation, training, and one year of support and maintenance.

Uniq Computer Corp. (Batavia, IL) unveiled Unibase, a high speed database management system utilizing back-end processor technology and UNIX System III software

Continued on p. 95

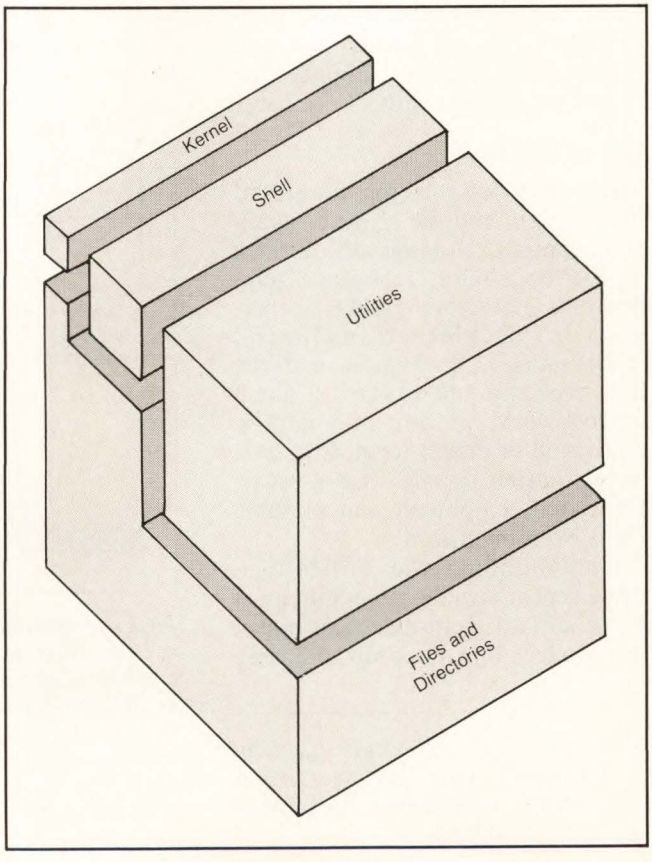

Figure 4: Basic UNIX components. The basic UNIX kernel is now locked.

Building A Data Acquisition System From Board Level

by John Sylvan

Linking the analog and sensor industrial environment to the digital computer environment can prove challenging to the systems designer.

The key obstacle to successful factory automation frequently lies in the interface between the computer and the industrial process. In typical industrial environments characterized by high electrical noise, long wiring runs, and large common mode voltages, transforming low level, often nonlinear sensor signals into their linearized digital equivalents, presents a serious challenge. Digital system integrators not well-versed in the mysteries of analog interface can find these challenges particularly thwarting.

Fortunately, manufacturers of analog interface products now offer a growing host of solutions ranging from modular signal conditioners to complete, fully conditioned board-level intelligent I/O sybsystems. Screw terminal sensor connections and advanced software drivers dramatically simplify the system integrator's job.

DAS Options

Figure 1 illustrates the nature of the problem and the range of available solutions. Analog sensors such as thermocouples, resistance temperature detectors (RTDs), thermistors, pressure transducers, strain gauges, flowmeters and the like typically operate in a harsh analog world. Before they can be converted to digital form, low level sensor output signals often must be translated, amplified, and in some cases even linearized.

Compounding the difficulties, these sensor signals frequently must be separated from electrical noise, often exceeding hundreds of peak volts, generated by motors, relays, induction furnaces, and other plant equipment, including in some cases the data acquisition system itself. And common mode voltage differences of more than 1,000 volts between the ground at the sensor and the ground at the distant computer must be protected against.

System integrators have a variety of options in bridging the gap between the analog or sensor world and the computer world. Where great physical distances separate sensor and computer, μP-based intelligent front ends **(Figure 2),** located up to 10,000 feet from the host processor, can interface direct-

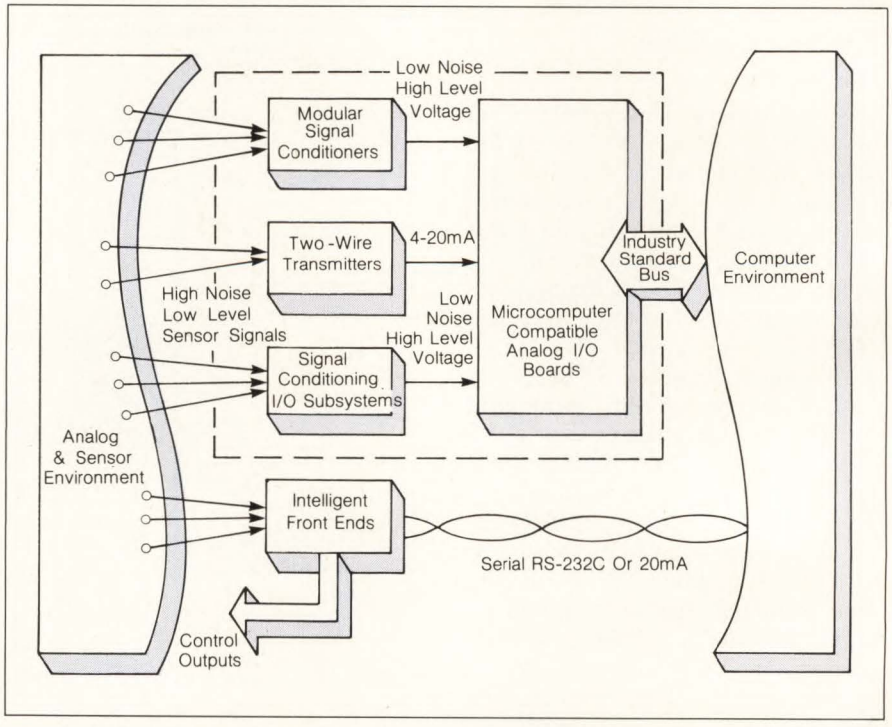

Figure 1: Manufacturers offer a host of modular and board-level analog I/O products to help bridge the gap between the harsh analog world and the world of the computer. Where great physical distances (up to two miles) separate the sensor and computer, fully independent intelligent front-ends can condition and multiplex hundreds of sensor and control signals onto a single serial data link, thereby saving considerable wiring installation expense. Alternatively, system integrators can pursue a building block approach employing modular signal conditioning products in combination with board level analog I/O subsystems that connect directly to the host processor's backplane bus.

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ly to a range of sensors providing signal filtering, isolation, scaling, and linearization. Under local firmware control, the front end automatically scans and stores in on-board RAM the outputs of multiple sensors. In response to host processor commands, the front end transmits sensor data at rates of up to 9600 baud over a single RS–232C or 20 mA serial communications link **(Figure 1).**

With suitable expander boards, Analog Devices' μMAC, for example, can connect a total of 384 analog and 1088 digital sensor inputs, and 256 analog and 1088 digital control outputs to a distant host computer all on that single serial data link. With typical industrial wiring installation costs ranging from $3 per foot to $16 per foot for conduit housed connections, the μMAC can lead to substantial installed cost savings.

Available software drivers for some of the more popular host processors (such as the HP-85, IBM personal computer, the Apple II, and DEC hardware operating

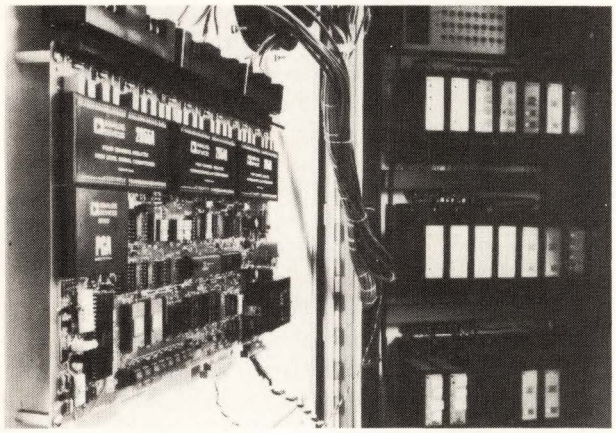
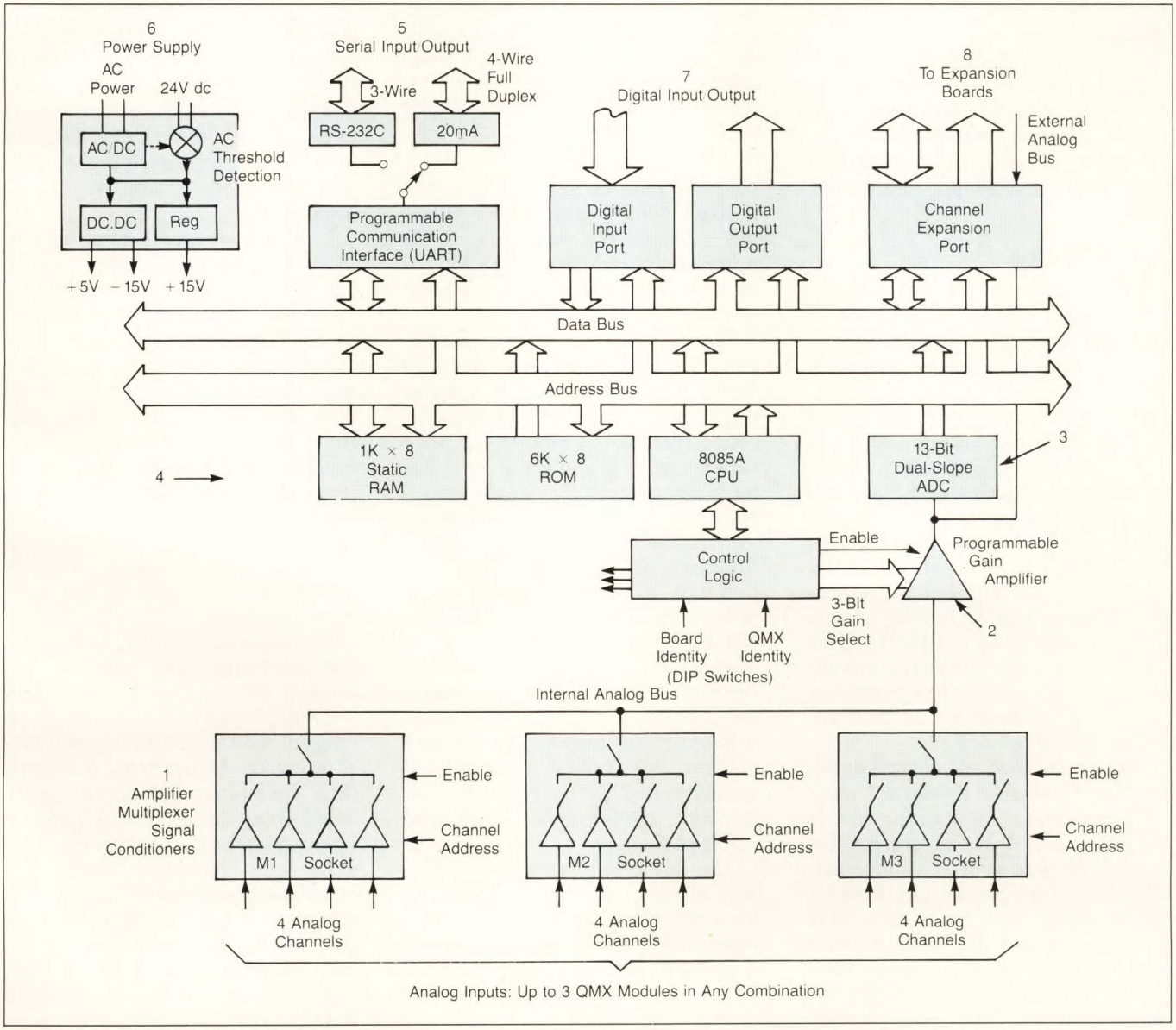


Figure 2A, B: Operating as a remote intelligent front-end, the Analog Devices μMAC-4000, in combination with expander boards connect up to 384 analog and 1088 digital sensor inputs, and 256 analog and 1088 digital control outputs to a remote host over a single serial data link.



RSX–11 software) convert all μMAC–4000 commands to high level callable subroutines. This frees the system integrator from having to write I/O software.

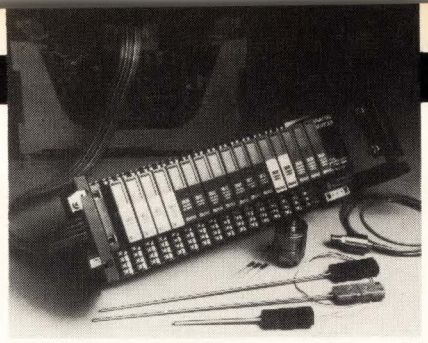
But for applications where less distance separates sensors and the host computer, many designers prefer the building block approach also depicted by Figure 1. This approach employs modular signal conditioning products in combination with board level analog I/O subsystems connected directly to the host processor's backplane. Signal conditioning products **(Figure 3)** convert low level, noisy, often nonlinear sensor outputs to their low noise, high level equivalents, thereby facilitating analog to digital conversion and further signal processing.

That analog to digital conversion typically takes place on the analog I/O board, which in turn provides a direct memory mapped interface between popular microcomputer buses and analog input and output signals.

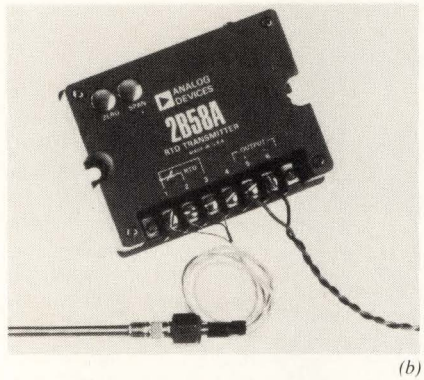
Bus Selection

Design of a board level data acquisition system often begins with a designation of the host processor and/or bus structure. However, since analog I/O product manufacturers do not support all buses equally well, the system integrator must fully consider the application's analog I/O requirements before settling on a bus and processor. In addition, the user should select his bus carefully in light not only of the present, but perhaps equally important, future system needs. In this regard, most DAS designers prefer the more popular industry standard bus structures that allow for maximum system flexibility in incorporating future options.

For simple low cost control applications involving repetitive tasks and minimum computation, such as might be found in discrete process control or in control of a single machine, an 8-bit bus usually suffices. Of available 8-bit buses, the STD bus has perhaps the best hardware and software support among both computer and analog I/O product manufacturers. Other popular 8-bit



(a)



(b)

Figure 3: Data acquisition system building blocks such Analog Devices' 3B Signal Conditioning Subsystem (a) and the 2B series of modular signal conditioners (b) convert low level often noisy sensor signals into high level voltages or currents providing isolation and input protection as well.

buses supported by analog I/O product makers include the Multibus (which also supports 16-bit processors), and Motorola's Micromodule/EXORcisor bus, among others.

For applications demanding greater speed, computational capability, or memory capacity, such as might be found in continuous process control environments, or laboratory/scientific applications, a 16-bit bus makes the most sense. Here, the system integrator can select from a variety of buses. Intel's Multibus (IEEE–P796) was the first bus to provide 16-bit backplane support. In fact, Multibus can support processors from 8 to 32-bits. DEC's LSI-11 and Texas Instrument's TM–990 receive popular support from both hardware, software, and analog I/O product vendors. Motorola's Versabus, originally geared for the 68000 processor, also handles other 8, 16, and 32-bit processors.

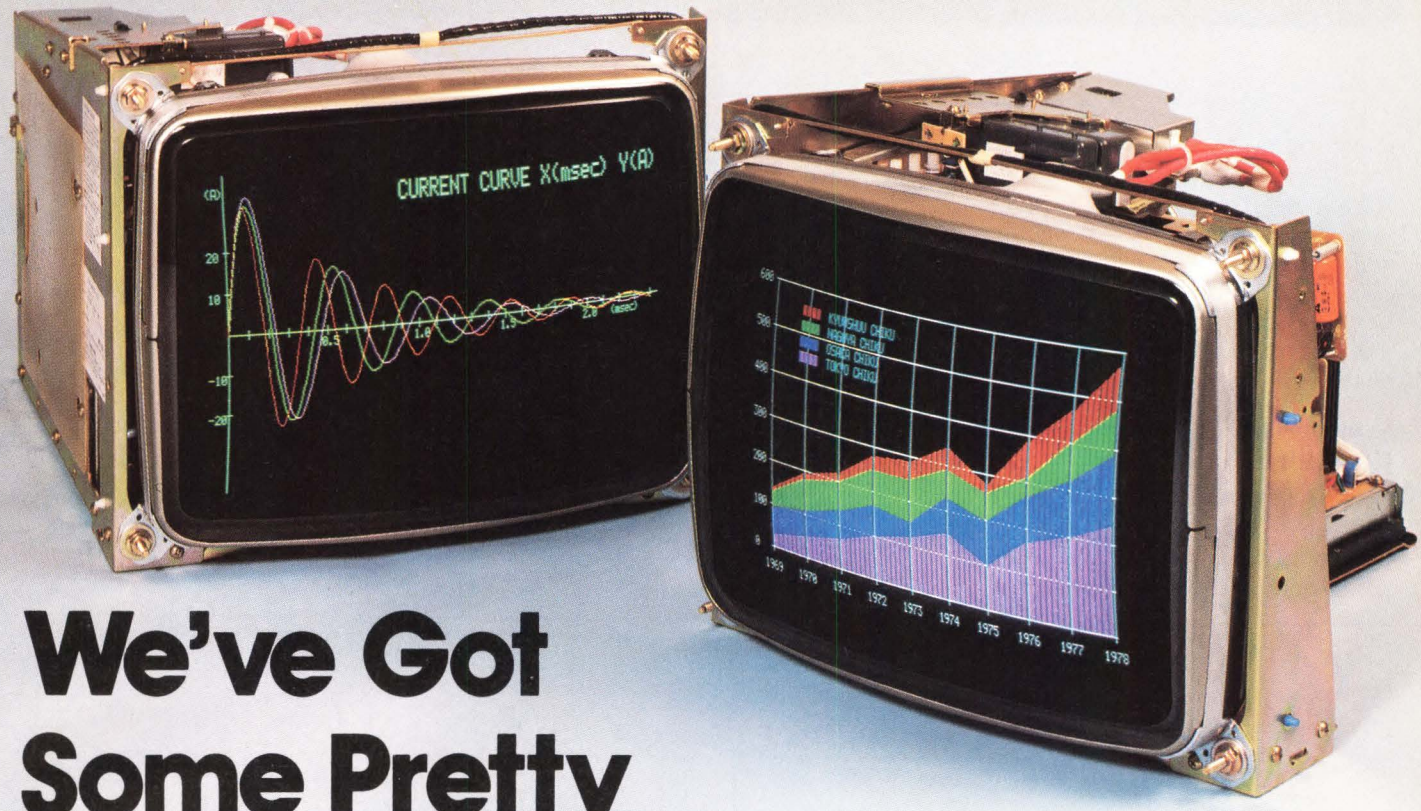
The agreement between Motorola, Mostek, and Signetics/Phillips to support the Versa Module Europe, or VME bus may be the most significant recent development in bus structures. The VME bus handles 8, 16, and 32 bit processors and calls for boards, connectors, and card cages in the Eurocard physical format. Its ability to handle almost limitless multiprocessor applications, combined with its speed, flexibility, and detailed system error status recording account for its growing popularity not only in Europe, but in the United States and other markets as well. Although the VME bus is not yet widely supported by analog I/O product manufacturers, this will undoubtedly soon change.

Board Selection

Available board level analog I/O products from a variety of manufacturers range in capabilities from completely dumb boards lacking even modest intelligence to μp-based fully independent intelligent subsystems with on-board sensor signal conditioning. Analog signal handling capabilities range from 4 to 64 channels with signals digitized to 8, 10, 12, 14, or 16-bits at conversion rates exceeding 100 kHz in some cases.

Low cost so-called dumb analog I/O boards were developed with an eye toward simplifying the system integrator's hardware development efforts. However, with many such components, the host processor must directly control all I/O functions including channel addressing, A/D conversion start time, and transfer of converted data to or from memory. Although initial board costs may appear low, use of dumb analog I/O boards entails significant system software development costs and hidden system overhead expenses.

In response, analog I/O board manufacturers have recently addressed the needs of the system software designer in developing intelligent data acquisition board level products. As μp-based products, they resemble dedicated single board computers. Although analog signal handling capabilities vary, most fully intelligent analog I/O boards automatically scan analog sensor outputs, adjust channel gains, linearize sensor signals, convert raw data to engineering units, and store the results in on-board RAM. Some boards detect mini-



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mums or maximums, or set limits for alarm purposes. The analog I/O RAM maps to the host processor as a contiguous block of memory which the host accesses when necessary. The fully intelligent analog I/O therefore almost completely unburdens the host from routine analog I/O tasks.

Intelligence and Conditioning Combined

Analog I/O product manufacturers pack increasing functionality onto bus compatible boards. For example, Analog Devices' recently in-

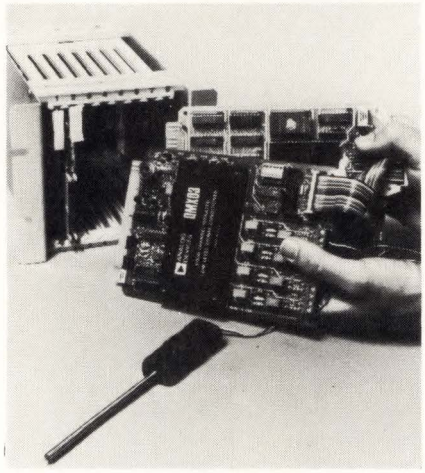
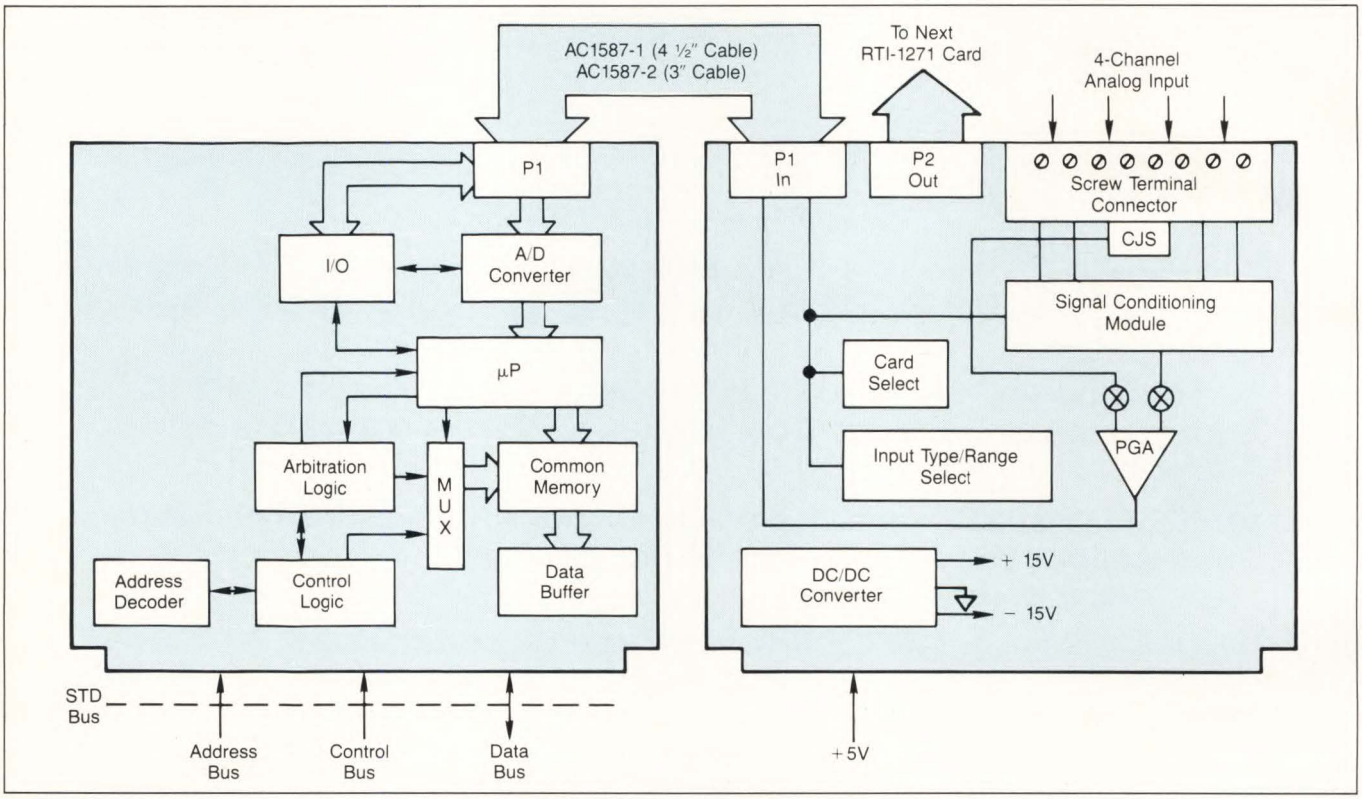
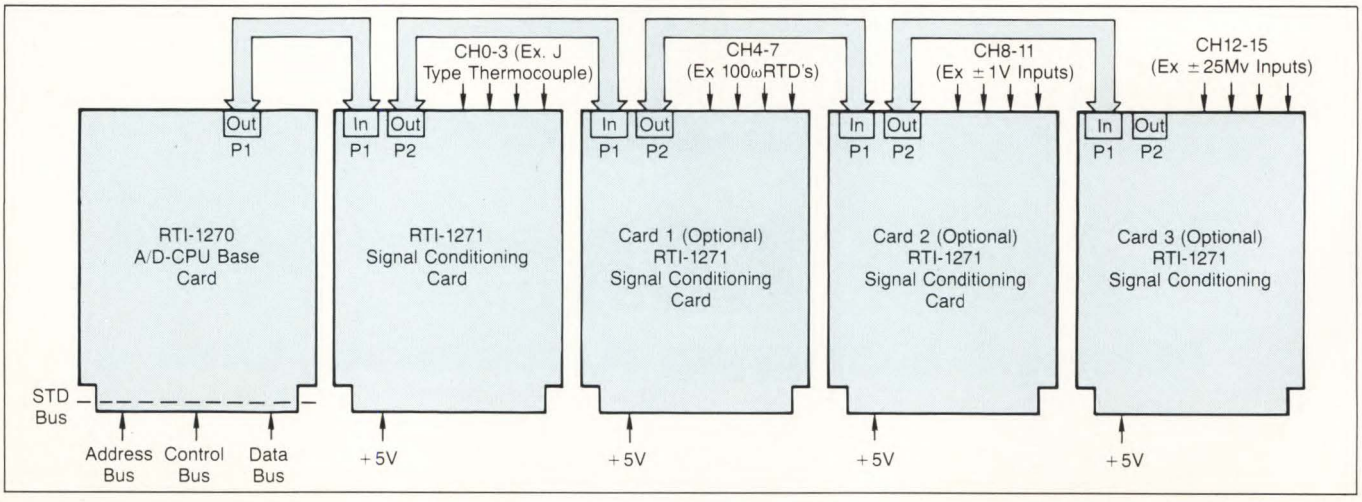


Figure 4A: This board set combines signal conditioning, A/D conversion, and μP-based intelligent data manipulation onto STD bus compatible boards.

Figure 4: The system integrator can cascade up to four RTI 1271 Signal Conditioning Cards (c) to handle up to sixteen sensor inputs.





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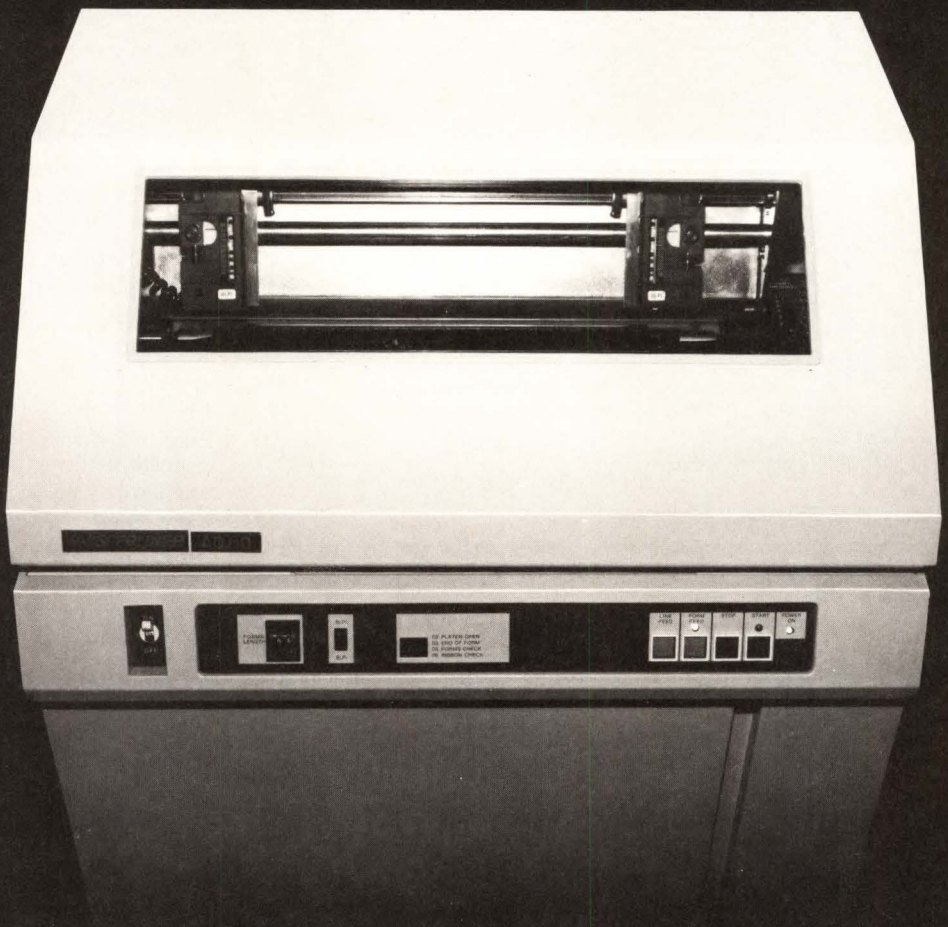

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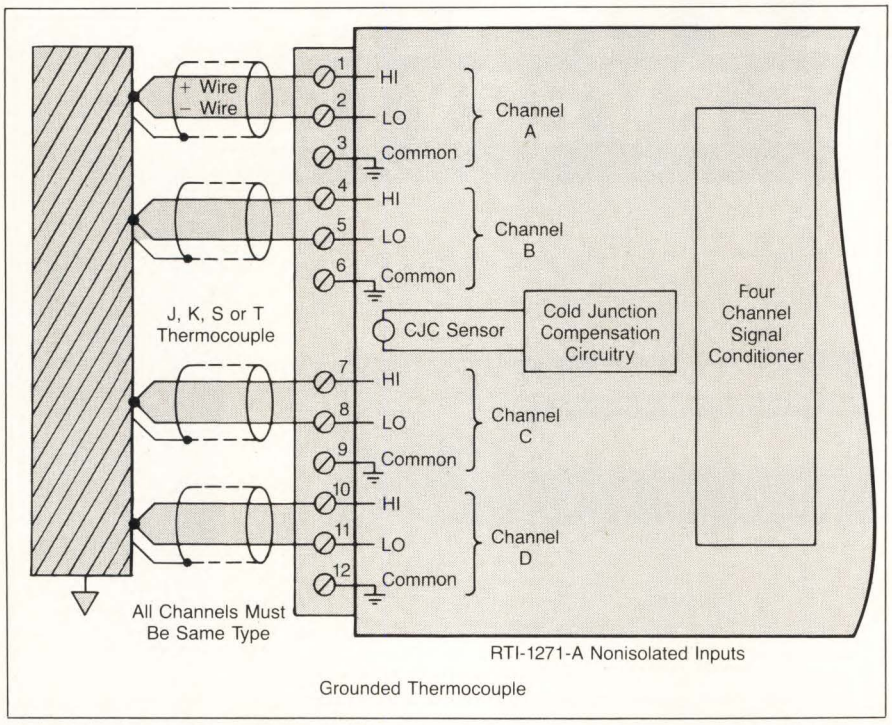


Figure 5: An accurate thermocouple temperature measurement requires at least one temperature referenced junction.

troduced Series RTI-1270 intelligent analog I/O for the STD bus brings all sensor signal conditioning in addition to intelligence onto the board. With the series RTI-1270, the STD bus system integrator need only plug the I/O boards into the STD bus backplane, attach sensors directly to screw terminal connectors on the boards, and turn on the power.

The series RTI-1270 allows STD bus system integrators to interface to thermocouples (J,K,S,T type), RTDs (100-ohm platinum types), mV, V, or mA signals in the presence of electrical noise, ground loops, and high common mode voltages. The product performs all sensor signal conditioning including cold junction compensation for thermocouples, excitation for RTDs, scaling and linearization of sensor outputs, and automatic conversion of data to engineering units. Sensor data is stored in on-board RAM that maps as a 1K block of STD bus memory. The system provides up to 1000 volt input to output isolation, 16-channel analog multiplexing, and 13-bit analog to digital conversion. It requires a single 5-volt supply.

The series **(Figure 3)** consists of a RTI-1270 A/D-CPU Base card and up to four RTI-1271 Signal Conditioning / Multiplexer cards, all electrically and mechanically compatible with the STD bus. Each of the Signal Conditioning / Multiplexer cards accepts four differential analog signals and provides analog signal conditioning such as input overvoltage protection, I/O isolation, common mode noise rejection, filtering, signal amplification, and channel multiplexing. The system integrator can configure the cards to accept a wide range of analog inputs by simple jumper and DIP switch programming.

The A/D-Base Card forms the heart of the system. It includes the analog to digital converter, μp, memory, and STD bus interface logic. On-board firmware drives the RTI-1270 independent of STD bus control, automatically scanning the channels, performing the A/D conversion, linearizing and scaling the results as necessary, and converting the digital output into engineering units. The system then stores the data in three formats—binary, BCD, and ASCII in 1K of RAM addressable by the STD bus as a 1K ROM. The system integrator jumper selects the location of the memory within the STD memory map.

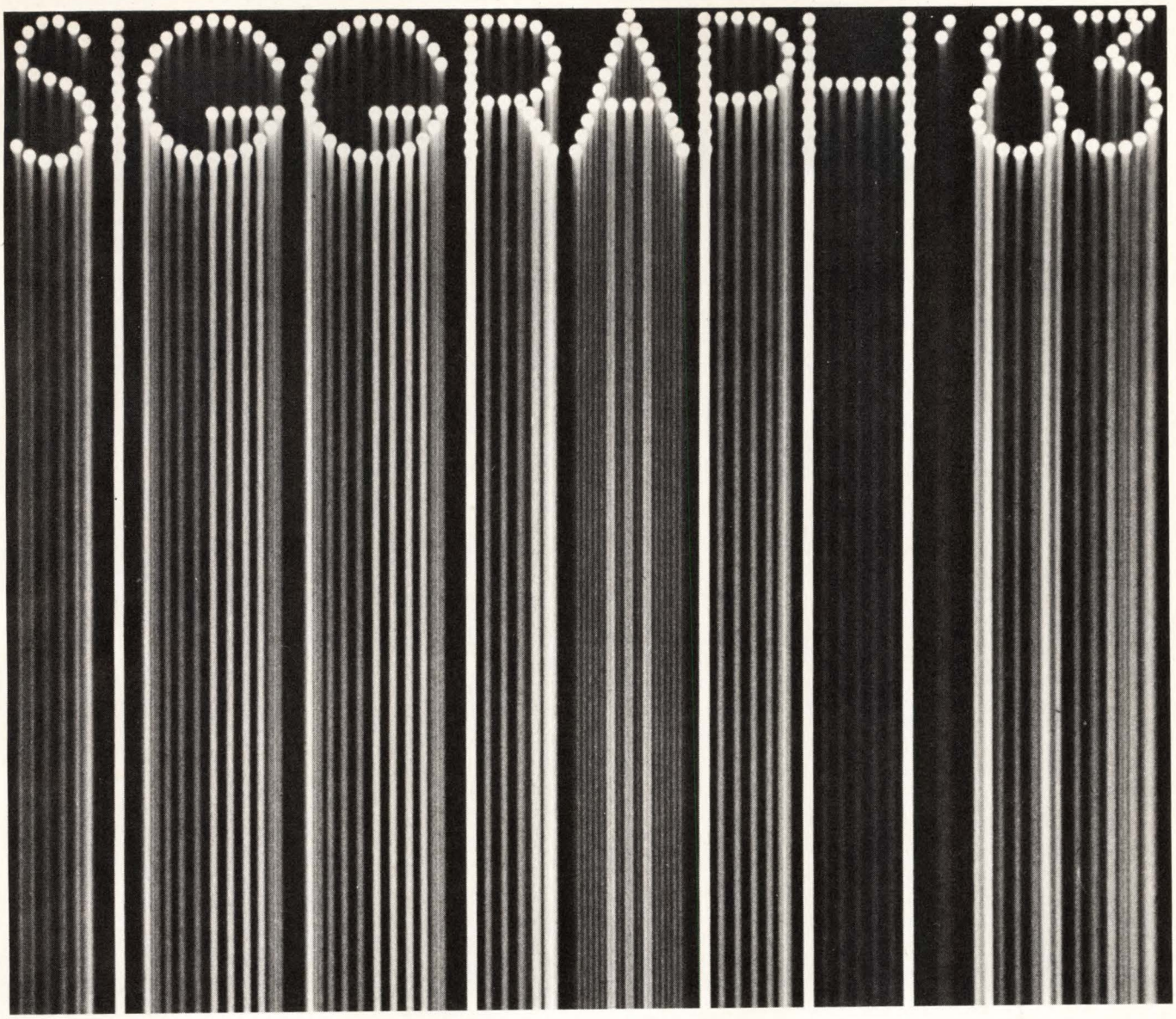
Simple Sensor Interface

Digital system designers not experienced in analog interface often despair at connecting their systems to sensors located in harsh factory environments. Electrical noise, ground loops, and high common mode voltages can lead to faulty sensor readings, and can even seriously damage equipment. The new generations of analog I/O boards, however, eliminate most of these concerns.

For instance, take the case of perhaps the most common of industrial sensors, the thermocouple. Thermocouples operate under the principle that two pieces of dissimilar metal in contact generate a small yet repeatable voltage (often only microvolts) as a function of temperature. Yet, since every pair of dissimilar metals in contact constitutes a thermocouple (even copper/solder junctions), successful use of thermocouples requires a minimum of extraneous connections, and the use of at least one temperature referenced junction. Furthermore, many thermocouples generate voltage as a nonlinear function of temperature.

Figure 5 illustrates a further and potentially disastrous difficulty in the use of thermocouples. Since thermocouples often electrically contact the object whose temperature they measure, ground loops and large common mode voltages between the ground at the sensor and the ground at the instrumentation can result. These voltages can sometimes rise as high as 1000 volts. If instrumentation circuitry exhibits insufficient isolation, equipment damage and even shock hazards can ensue.

The new generations of analog I/O products defy such obstacles thereby greatly easing the system designer's job. Signal Conditioning / Multiplexer cards now available **(Figure 5)** automatically protect against common mode voltages of 1000 volts. The user simply connects his thermocouple to screw



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STD System Cuts Software Costs

by Larry Hanger

Engineers involved with development work, whether machine control or facility management (lights, heating, robotics, home management), soon realize that the real cost is in software. These costs can range from $35 to $150 per hour. Assuming $50 per hour per programmer, a project requiring twelve weeks with four programmers would cost $96,000. If the project runs over budget and requires two additional programmers for two weeks, the cost now approaches $104,000. Add in the cost of a development system(s) and the expense could easily reach $120,000 to $150,000.

The Approach Series of STD Development Systems can cut these costs through the use of a user friendly menu driven software package which aids the user during development. A resident software package leads the user through yes/no decisions covering each facet of the STD cards set-up procedure. These answers literally configure the system (**Table 1**).

A software library contains preprogrammed control words such as: PRINT, TRANSMIT/RECEIVE, TIME, STORE/RETRIEVE, A/D, D/A, etc. These words are designed to make use of the functions of the cards selected in the menu. A program could be as simple as METER READ DISPLAY. The user no longer needs to know the hardware configuration of the card to talk to it. Time is spent "driving" the application vs. "building" the wheel.

Using the previous example and the Approach II System, the same project is estimated to require six man/days or about $3,600.

The systems integrator may find his main expense is in software development.

A typical example of such a procedure would be a system designed to continuously scan several channels of analog information and display it on a CRT screen. Perhaps this information consists of seven independent temperature measurements and three related voltage measurements in a stand-alone enclosure. The traditional approach would require the purchase of a CPU, CRT and a 16 channel analog-to-digital card and many hours of learning to operate them before beginning software development.

As engineering projects generally progress, the warranty may run out before any successful measurements have been made, or the cards may have to be returned to the manufacturer because the user could not understand all the documentation. With the Micro-Link menu driven Approach Software and the Approach II Development System, the user could almost immediately determine that the hardware (at the board level) was functioning correctly.

Through the menu, the Approach II asks questions which allow the user to set-up the card for the application. As shown in the "set card" routine (**Figure 1**) the user is queried as to the I/O address of the card, the number of channels, full scale range, and allows each channel to be permanently named. For example, rather than sending out the proper codes (perhaps 10 or 12 assembly language statements) to read channel 7, the user could name channel 7 "TEMP-PROBE" (or anything else) and declare TEMP-PROBE READ.

The TEMP-PROBE READ statement is the entire program which then provides the following sequence of events:

1. Get the channel number of temp-probe (7).
2. Index in to the I/O map address of the A/D card and set input stages to channel 7.
3. Tell the converter to make a reading.
4. Wait until reading is completed.
5. Get data (12 bits).
6. Store reading in variable for further processing.
7. Display if desired.
8. Return to calling program.

Approach performs the functions diagrammed in the "READ" routine on channel 7 (**Figure 2**).

Since the basic routines (read—wait for end of conversion—set channel) are inherent to the Ap-

CARD SELECTION MENU

WHICH CARD DO YOU WISH TO CONFIGURE?

1) STD-098 CRT CARD
2) STD-134 64 CHANNEL TTL I/O CARD
3) STD-135 MASTER USART CARD
4) STD-136 SLAVE USART CARD
5) STD-137 8085 CPU CARD
6) STD-138 MODEM CARD
7) STD-140 32 CHANNEL MED POWER CARD
8) STD-141 12 BIT A TO D CARD
9) CONTINUE

Table 1: To aid system configuration, the Approach II resident software package leads users through yes/no decisions covering the Micro-Link STD cards set-up procedure.

Larry Hanger is Director of Engineering, Micro-Link Corp., 624 S. Range Line Road, Carmel, IN 46032.

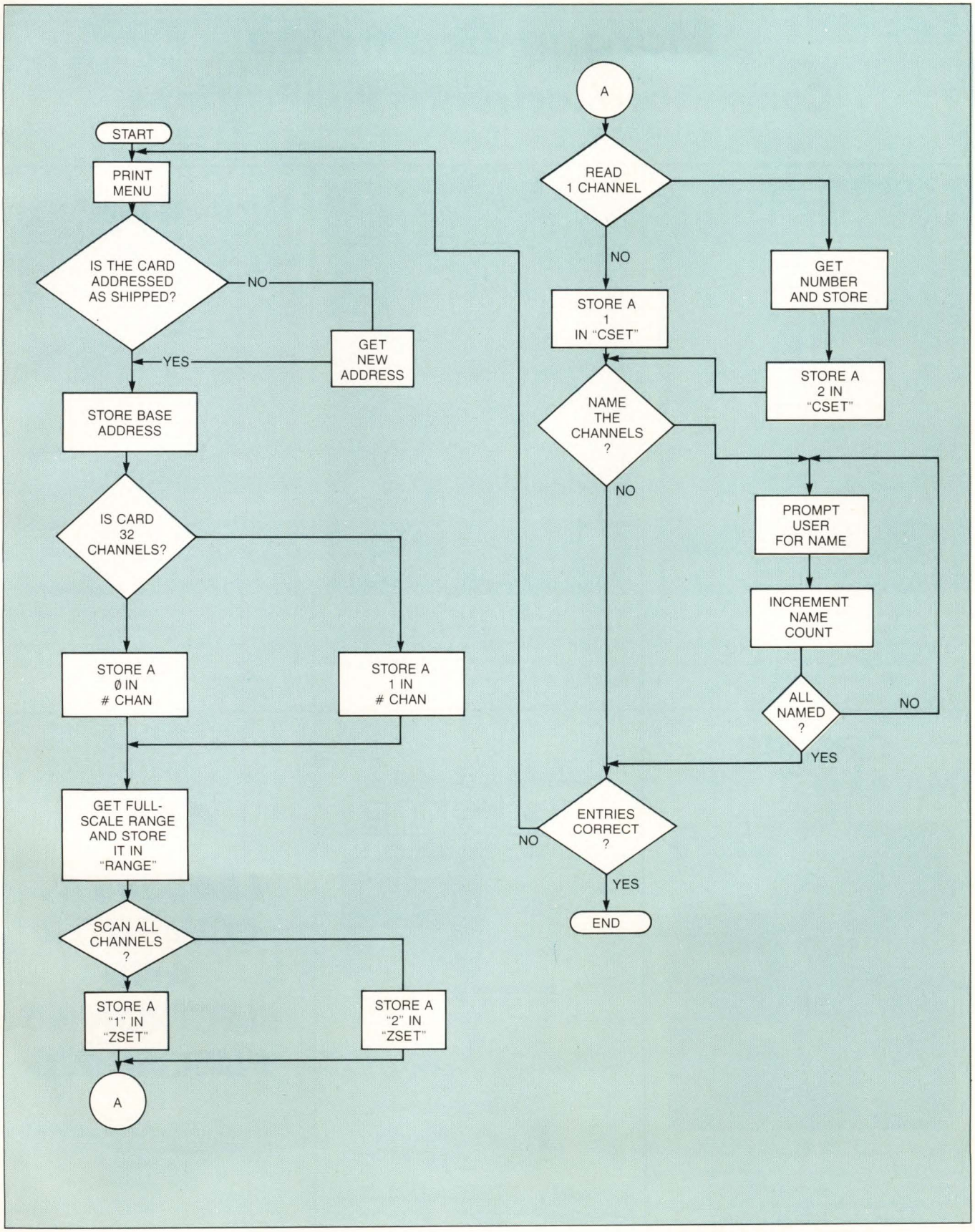

Figure 1: The "SET CARD" routine asks questions which allow the user to set-up the card for the application.

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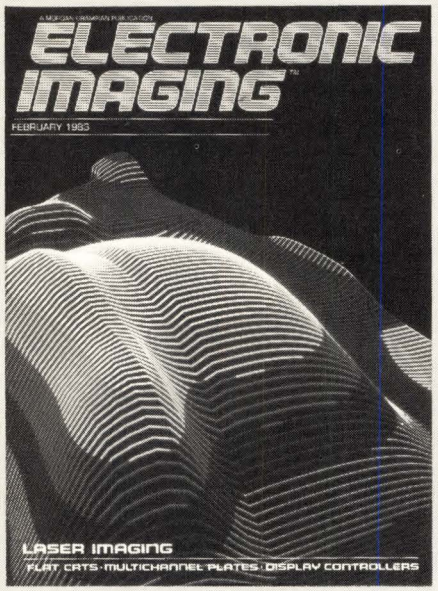

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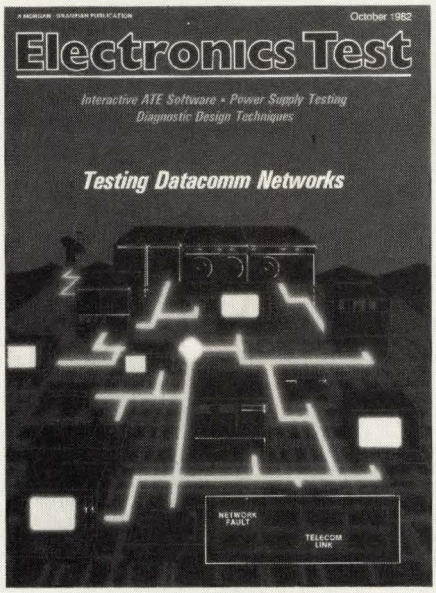

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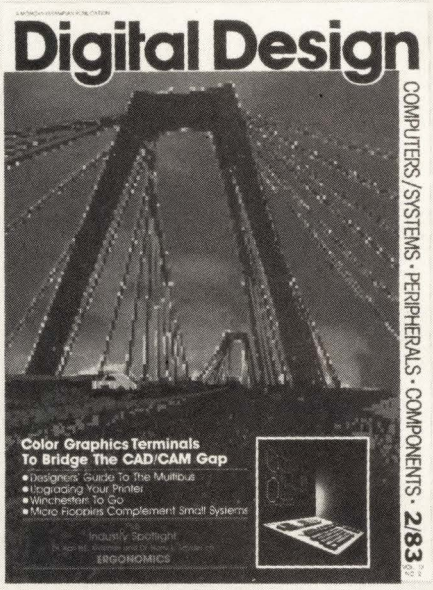

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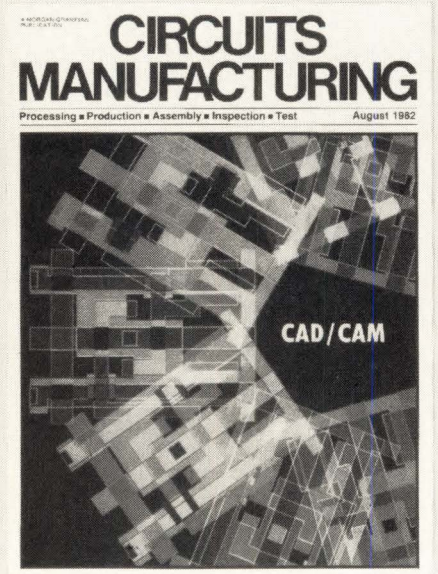

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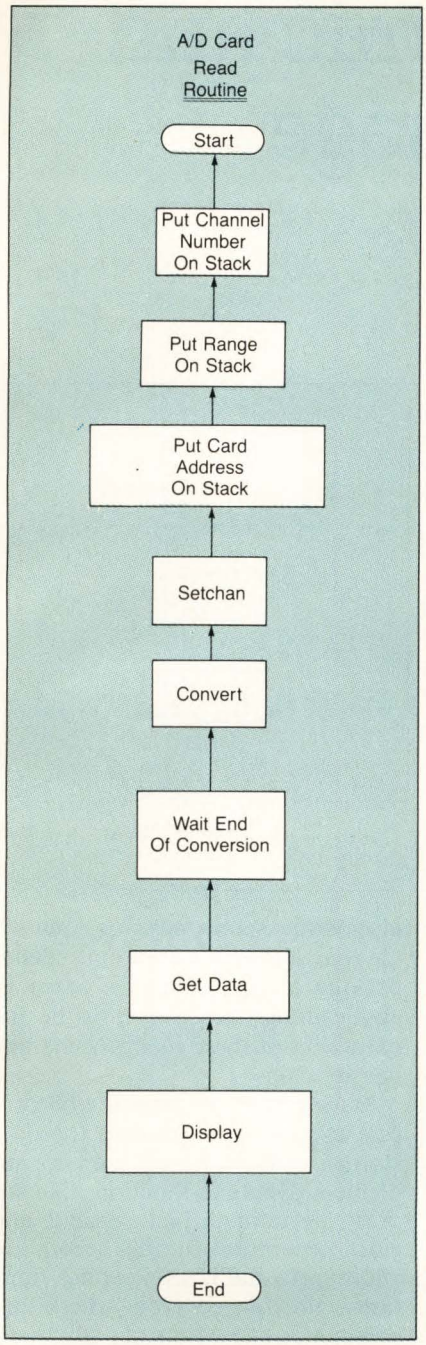

Figure 2: Approach performs the functions diagrammed in the "READ" routine on channel 7.

proach, the user may spend time developing the flow of the particular application.

Once the application has been fully tested, the user may then program EPROMs directly from the Approach keyboard for insertion in the CPU card of the target machine. □

New Concepts in Dynamic and Static Memory Cell Storage

by Al Reddy

Spurred by a much broader customer base than was the case with 16K RAMs, demand for the 64K RAM devices could grow more than tenfold in three years, from $61 million in 1982 to $710 million in 1985, according to the latest Rosen Research Letter. A major part of this increase is due to rapid erosion in the price structure of the 64K RAM. Currently some TTL interface devices are more expensive and harder to get than thousand-times-more-complex devices like the 16K dynamic memory. Due to the ever-increasing demands being placed on memory size by software, the 5 volt, TTL compatible single supply 64K RAM is being incorporated more and more into designs that were once the realm of the static memories.

Dynamic memories have come of age and are no longer the domain of the mainframe or mini-computer manufacturer alone. Several new horizons in their applications are being pursued. The memory designer today is no longer intimidated from using dynamic memory, due to its inherent refresh characteristics that are essentially asynchronous to the CPU operations. In this article memory refresh options available will be explored, as will implementation of refresh in typical systems.

RAM Progress

Semiconductor random access memories developed at a very rapid pace throughout the last decade and continue to do so today, with NMOS process being the dominant manufacturing technology. The breakthrough of storing binary data by using a single transistor memory cell to increase storage densities is a direct result of the rapid pace of development in the field of very large scale circuit integration (VLSI) techniques. VLSI monolithic semiconductor technology has allowed increasingly dense packing of chip elements. Memory applications have proven to be the natural fit of these inexpensive high density chips.

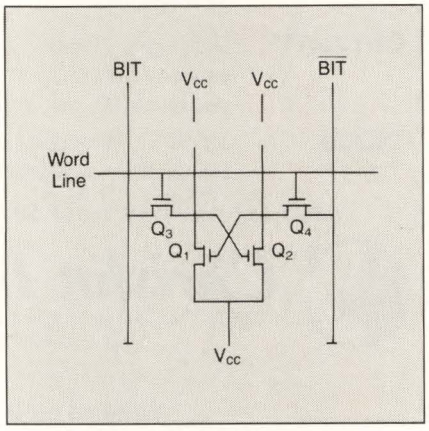

Figure 1: A typical four-transistor static storage cell.

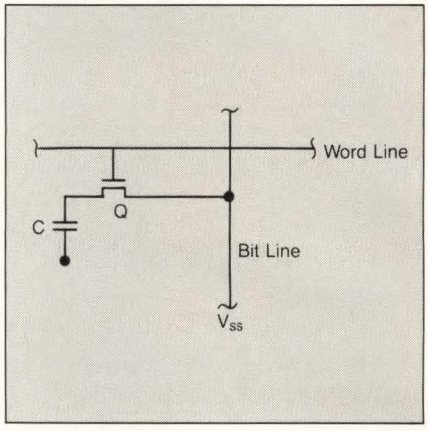

Figure 2: A single-transistor dynamic storage cell.

Dynamic Memories have come of age; no longer are they in the domain of the mainframe or mini-computer manufacturer alone.

During the last decade, the process used to manufacture the data storage cells was also used to implement overhead functions like address decoding, data sensing and clock generation. In this decade, in addition to the housekeeping functions already covered, there are companies like Motorola who have additionally implemented intelligent functions such as optionally selectable Pin 1 refresh mode and transparent substrate bias generation on their 64K dynamic memory. Thus the 64K RAM provides a compatible single TTL power supply requirement of 5 volts and at the same time eases the refresh design task, by using the Pin 1 function described later in this article.

All the above functions have been supported by keeping the number of leads on a memory package at 16 pins, which is the

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smallest pin count for a memory device today when compared to storage density. For large memory systems where low cost per bit and minimum size are the dominant design considerations, dynamic RAMs are the obvious choice. They offer the lowest cost and package count per bit of any semiconductor memory component. The high density memory devices individually packaged may easily be combined to yield very large memory systems tailored to the desired word width and memory depth.

MOS Technology

The process used to manufacture dense memories today has predominantly been N-Channel MOS technology for the following reasons:

- Manufacturing ease through ion implantation for accurate control in the injection of impurities to reduce internal MOS thresholds to manageable external TTL levels.
- Performance advantages of low operating voltage and higher speed, especially when scaling of device internal geometries is performed. NMOS technology is inherently faster than PMOS technology, as electron mobility is the medium of charge transfer in NMOS and this medium is two to three times faster than hole mobility (the medium employed in the PMOS process).
- NMOS structures are smaller, thereby permitting greater circuit density.

Due to the above factors NMOS has become the dominant process and is being used in the manufacture of state of the art memories today. A close look at a typical cell structure that is being implemented at present on both static and dynamic memories will help explain the function of storing and retrieving data from the cell.

Static Memory Cell

Early memory devices had static storage cells with data being retained as long as the device was powered-up. The bistable flip-flop is the basic storage unit for a static MOS memory cell (**Figure 1**).

The flip-flop consists of a pair of cross-coupled transistors with one or the other conducting depending upon the data stored. In the memory array, all cells in a column share the bit lines while all cells in a row are selected by a common word line. Bit lines are normally held at a higher potential than the non-energized word line and the cell is maintained in a deselected mode by not providing any gate drive to the two word line transistors Q_3 and Q_4. When the potential of the word line is raised, the gates of transistors Q_3 and Q_4 allow the proper connection to be made to their respective bit lines, thereby enabling the state of the storage cell to be read. The write operation is similarly carried out by turning on Q_3 and Q_4 and setting the logic state desired to correspond to voltages on the two bit lines. Since either transistor Q_1 or Q_2 is always turned on in the bistable flip-flop, the static cell is dissipating power constantly even when the cell is not accessed, thereby consuming considerable power when the complete memory array is taken into account. A static cell is therefore characterized by high power dissipation and a much larger cell structure compared to a dynamic cell.

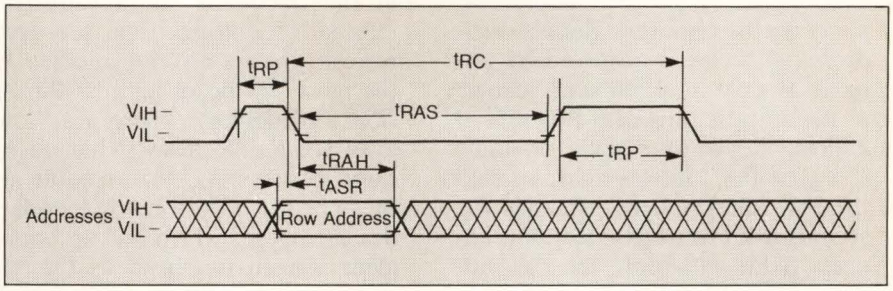

Figure 3: $\overline{RAS}$-Only refresh cycle (Data-In and Write are Don't Care; CAS is HIGH).

Dynamic Memory Cell

Dynamic NMOS memory cells have evolved ever since they have been introduced in the early 70s from a four transistor cell to the present single transistor storage cell. The simplest charge storage random access cell is illustrated in **Figure 2**. It consists of a capacitor upon which information is stored as charge and is accessed through a single gating transistor. The cell is written by establishing the bit line level on the capacitor through the gating transistor, and reading occurs by connecting the capacitor to the bit line again through the gating transistor. Sensing the change on the capacitor is usually done by means of detecting a quasi-voltage change on the bit line capacitance. One of the drawbacks of this cell is that the readout is destructive, but in actual practice there are restore circuits that transparently write back the original charge stored in the cell before the cycle in progress is completed. Another major drawback inherent with the dynamic cell, is that there are junction leakage currents, at the capacitive nodes in the cell, which work against the stored charge of the cell capacitor and cause the charge to degrade with time and temperature.

The single transistor cell therefore must have its initial charge restored periodically to maintain correct stored data, and overcome charge loss—this essentially is the reason for calling the cell "dynamic." The periodic restoration, or reinforcement, of the cell charge in dynamic devices is termed "refresh" in semi-conductor parlance, and at present the standard requirement is to refresh all the cells in the memory array at least once every two msecs.

Mechanics of Refresh

In a dynamic memory device the particular row address decoded (selected) during any valid memory cycle, be it a read, write or refresh, serves the additional function of refreshing all the cells that are associated with that single row decoded. The available address pins on dynamic memory devices today are

exactly half of the total number of address pins required. Reduced address pin count is achieved by utilizing a time multiplexing scheme of the address pins with two sets of address fields to decode a single cell. The first address field is called the row address field, whereas the second is known as the column address field, with only the row address field needed to do a refresh.

A 64K dynamic memory device with a refresh requirement of 128 refresh cycles every 2 msecs, implies that for the device to maintain correct data, refresh cycles must be performed on the memory cells using all 128 combinations of the lower order 7-bit row address field. Thus one refresh cycle must be performed on each of these row addresses in 128 separate cycles within the maximum allowed refresh internal of 2 msecs. The 128 cycle refresh devices are not affected by the most significant address Pin A_7 (Pin 9 of device). There are, however, some 64K RAMs that do require address A_7, for an 8-bit address field, to perform 256 cycle 4 msec. refresh, which has an equivalent refresh overhead as the 127 cycle 2 msec. refresh. The 256K RAMs that have been announced by major vendors have a refresh requirement of 256 cycles in 4 msecs.

A refresh only cycle (**Figure 3**) in which only the row addresses occur should not be confused with normal data store and retrieve cycles where both row and column addresses occur. The implementation of a memory refresh can be performed in one of two methods: *distributed mode* where the cycles are spaced in intervals of approximately one every 15 μsecs over the defined refresh period (2 msec. or 4 msec.) in discrete non-adjacent cycles; or the *burst mode*, where all the 128 or 256 refresh cycles are performed consecutively until complete (**Figure 4**).

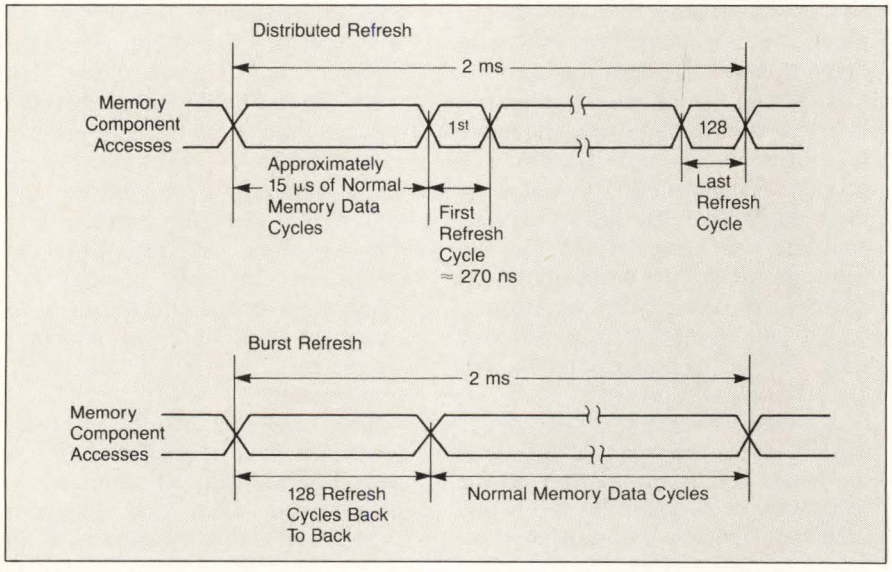

Figure 4: Memory refresh may be implemented in a distributed mode (a) or in a burst mode (b).

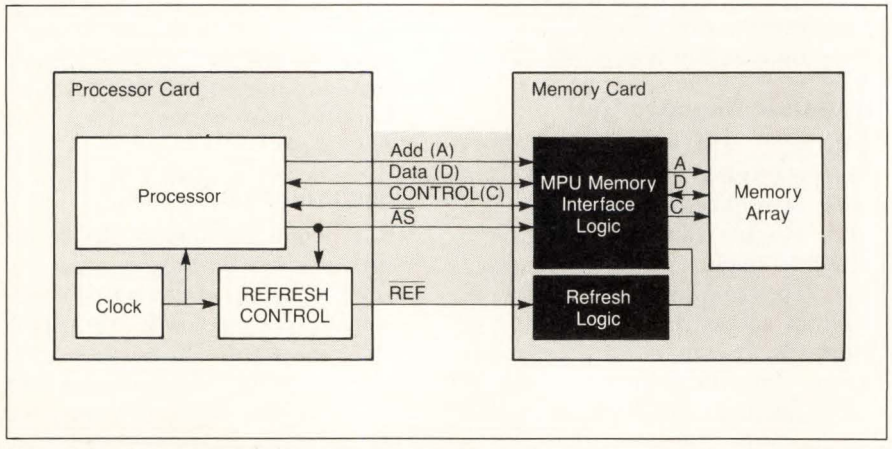

Figure 5: Memory hardware refresh control.

The selection of these two refresh techniques is based upon the time memory available, and also the ease of integrating it into the system. During both burst as well as distributed refresh modes, the normal central processor cycles are interrupted while the higher priority refresh cycles are performed by some means of arbitration between processor and refresh controller. The problem that has to be tackled during memory refresh is to synchronize the refresh cycle, which is occurring asynchronous, with the normal processor cycles.

Hardware designers of μPs and small computers were initially reluctant to take on dynamic memory that required additional complicated hardware to implement refresh, and thus used the simpler static memory instead. To an extent, static memories at the time made sense for the small memory size required for μPs and small computers, because the refresh hardware needed could not justify the cost. This was not the case with large mainframe memory system designs where the external circuitry and complex timing required for dynamic RAM refreshing is not a severe disadvantage. The added cost of refresh circuitry is spread over a large number of memory devices on mainframe memory, which again yielded a cost per bit that was lower than expensive static RAMs, with the added bonus of lower power.

Memory refresh operations detract from system performance since data cannot be accessed during a refresh interval. Therefore, system hardware to do refresh must be designed such that minimum system latency results due to refresh overhead. The designer should study the various options open and select a design that correctly addresses his needs with the highest system performance.

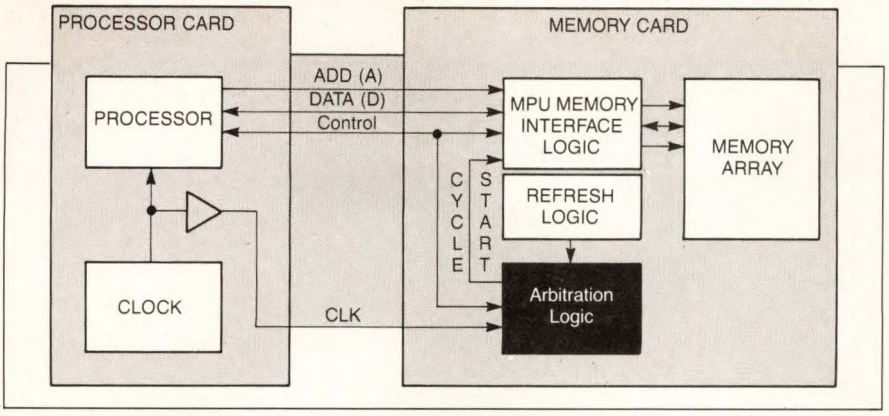

Figure 6: Processor hardware refresh control.

Methods of Implementing Refresh

Refresh requirements of dynamic memory can be satisfied by using one of two distinct methods: software refresh technique or hardware refresh technique. In software refresh the burden of providing the refresh cycle falls entirely on the processor, and it must execute some kind of software routine to refresh dynamic memory. To accomplish refresh, an interrupt service routine of the processor can be used such that whenever the interrupt is recognized, a hardware enable will allow the refresh routine to be executed. Another method that could be used is to employ a software counter that directs the processor to halt all I/O operations and to execute instead a subroutine of 128 dummy reads during each 2 msec interval.

Advantages to software refresh are that it is very simple to implement and requires little, if any, additional hardware. Disadvantages include the use of vital storage space in main memory for the refresh subroutine, and lower performance due to the time spent in executing the refresh subroutine.

Hardware configured refresh offers system performance with very minimal impact on data throughput of the processor. The additional hardware can be added to the memory card **(Figure 5)** or onto the processor card **(Figure 6)** so that at the appropriate time the refresh controller will generate the refresh request cycle and simultaneously place on the address bus a unique low order 7- or 8-bit refresh address to enable the memory component to decode the row to be refreshed. The advantage in having the refresh hardware on the memory card is that the card can be made to emulate static memory with universal application to most processors.

The disadvantage with refresh hardware on the memory card is that arbitration has to be accommodated, to decide bus access priority at the beginning of each cycle. Arbitration can add up to 75 ns of access latency on each cycle and lower system performance. The better approach is to provide refresh logic on the processor card where processor cycles will be interrupted only during a valid refresh request cycle, thereby improving system performance with the elimination of refresh arbitration overhead and interface bus delays on every cycle.

Before discussing the different hardware refresh options possible, the characteristics of the processor and the available bus handshake signals for interfacing must be evaluated. Interconnecting the two systems (Memory, CPU and/or MPU) and providing for their suitable communication must achieve the proper synchronization of the two, because the refresh operation is basically an asynchronous function. In systems where all operations are occurring sequentially with respect to a system clock, the interface problems are minimal; the interface designs are not as complicated as the synchronization between the refresh controls, and the MPU is handled by a common clock. Therefore, processors where all system functions considered are being timed by the same clock are called synchronous systems. Conversely, in asynchronous systems, data transfer manipulations or information exchanges are not timed by a common clock but events occur independently in multiples of processor clock. For proper synchronization in these systems, some form of handshake and acknowledge routine is required to provide effective system level communication between various subsystems.

Table I gives a listing of various refresh options and the validity of their usage for the type of CPU selected.

Pin 1 Refresh

Under hardware refresh options, the user of a Motorola 64K dynamic RAM (MCM 6664A) has the additional benefit of a refresh assist available on the device. This refresh feature on Pin 1 of the memory component is in addition to the regular RAS only refresh cycles already discussed. Pin 1 refresh cycles offer the user the benefit of making use of an on-chip refresh counter that generates the required refresh addresses internal to the device and an internally generated RAS strobe. The only hardware conditions that have to be met for this mode of operation are that the RAS and CAS strobes have to be inactive (high) and Pin 1 must be

HARDWARE REFRESH TYPE	PROCESSOR TYPE	
	SYNCHRONOUS	ASYNCHRONOUS
1) PIN 1 CYCLE	YES	YES
2) TRANSPARENT OR HIDDEN	YES	NO
3) CYCLE STRETCH	YES	YES
4) CYCLE STEAL	YES	YES

Table 1: Listing of various refresh options and the validity of their usage for the type of CPU selected.

pulsed low for refresh to be accomplished at the internal row address generated.

Both distributed and burst mode refresh cycles are possible with Pin 1 cycles and, in addition, memory devices can be kept in an indefinite refresh mode by keeping Pin 1 active low. Using the latter feature available on Pin 1, memory refresh can be performed while saving considerable hardware to the system designer contemplating memory battery back-up type applications. As a direct result of using the Pin 1 feature, considerable savings in power dissipation on the memory card can be realized, as the RAS and CAS strobes are the only memory device inputs that must remain high plus Pin 1 maintained low (steady state conditions).

The drivers to the other pins can be powered down because their functions are a "don't care" in this mode. As long as RAS and CAS remain high and Pin 1 remains low, the RAM will save data by performing refresh cycles internally. This internal sequence repeats asynchronously every 12 to 15 μsecs. At the end of each 2 msec interval, the on-chip refresh-address counter will advance through all 128 combinations of the low order seven bit row addresses. Processor constraints to this mode of refresh are once again dictated by the type of refresh being implemented as shown in types 2, 3, and 4 of Table 1.

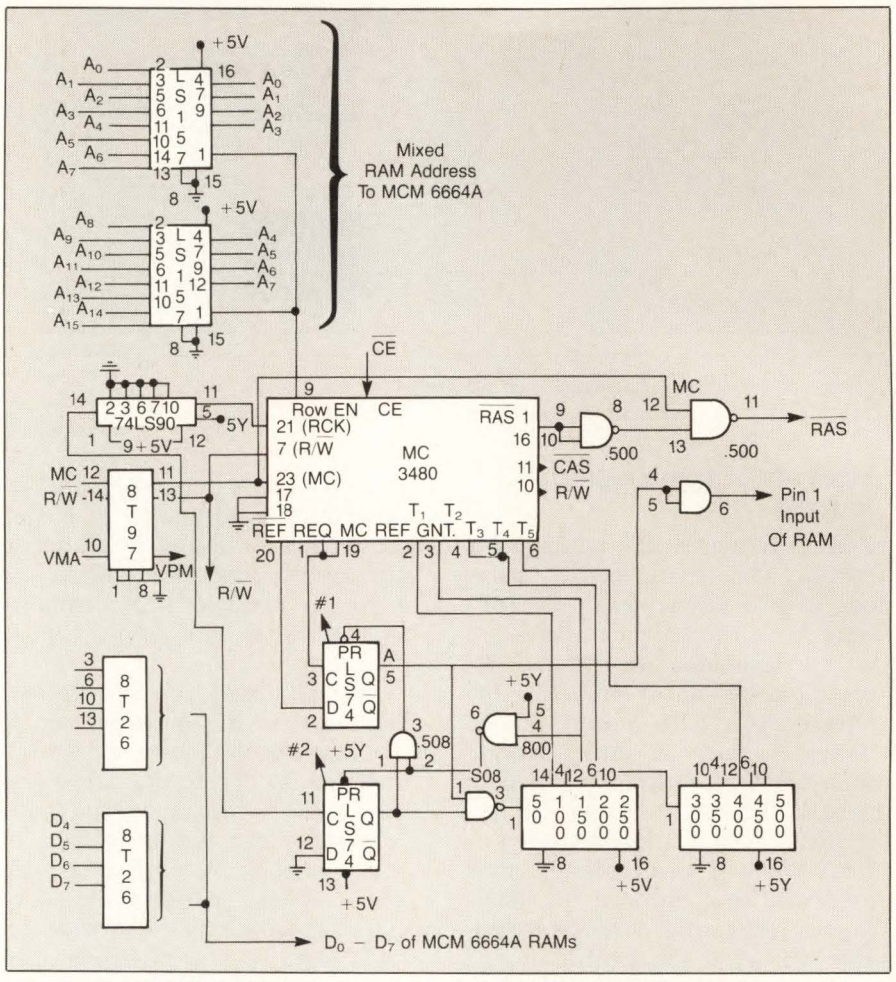

Figure 7: MC6800 CPU interface to MCM6664A dynamic memory with transparent synchronous Pin 1 refresh.

Transparent Refresh Mode

Transparent refresh implies that during regular central processor cycles, a refresh cycle is also being performed on the memory, with no interference with the processor cycles. Another name for this refresh scheme at the system level is also called "hidden refresh" because the refresh cycles are occurring during the time when no processor cycles can occur. This type of refresh is performed during the early or first half of a processor clock phase, as there are no valid memory addresses occurring during that portion of the cycle.

With a transparent refresh scheme, the processor clock speeds will be limited to around a maximum of 1.5 MHz or less when used with the dynamic RAMs available today. The inclusion of all gate delays to the RAM and back to the CPU adds to the cycle time of the memory component; in addition, the refresh cycle has to be fitted into the processor clock phase when the CPU is not executing.

The complete absence of system interference is possible in designs that use a refresh cycle which is transparent or hidden to normal processor cycles. An example of transparent refresh design is shown in **Figure 7**, where the MC6800 synchronous processor clock is also being used to generate the refresh request. The timing **(Figure 8)** explains the action of the refresh function.

There is a new connotation to the term "hidden refresh" which applies to the function available at the memory device level. This so called hidden refresh on the device is another mode of refresh wherein the refresh cycle is disguised with a normal read cycle in progress. After the read cycle is initiated, the data-out from the device is held valid by holding the CAS strobe active low, while the RAS strobe is being clocked with the appropriate row address to refresh the memory. The hidden refresh feature allows the saving of a data latch in low performance systems where data has to be maintained valid until the data can be accepted.

Cycle Steal Mode

In asynchronous systems it is not possible to do a refresh cycle without interfering with the processor cycles. With this type of processor, a high priority refresh request is generated and a refresh cycle is initiated at the completion of a processor cycle in progress. This re-

fresh scheme involves the interruption of a memory request from processor and, in its place, insertion of a refresh cycle. This results in stealing a cycle from the normal processor cycles to accommodate refresh. In doing a cycle steal refresh scheme, the loss in processor throughput will be around 2% to 4%, due to refresh requests being done in a distributed mode, which results in lowering the probability of a refresh and a processor request occurring simultaneously.

Cycle steal refresh can easily be designed into a multiprocessor system also, but the design must insure that a refresh request gets the highest priority in acquiring the system bus once the request is asserted. The highest priority for refresh should be built into the arbiter circuits so that the direct memory address (DMA) controller is prevented from gaining control of every bus cycle once the processor requests are not being processed.

In a system that is using a cycle steal refresh scheme and having a 500 nsec execute cycle, one refresh cycle is required out of every 30 processor cycles. When this refresh technique is applied in small systems with only one bus master, the arbitration overhead at the front end of each cycle can be eliminated, as the arbitration is replaced by a simple handshake approach of a request, grant and acknowledge routine occurring only when needed. An example of a cycle steal refresh scheme that could be used on asynchronous processors such as the MC68000 is shown in **Figure 9**.

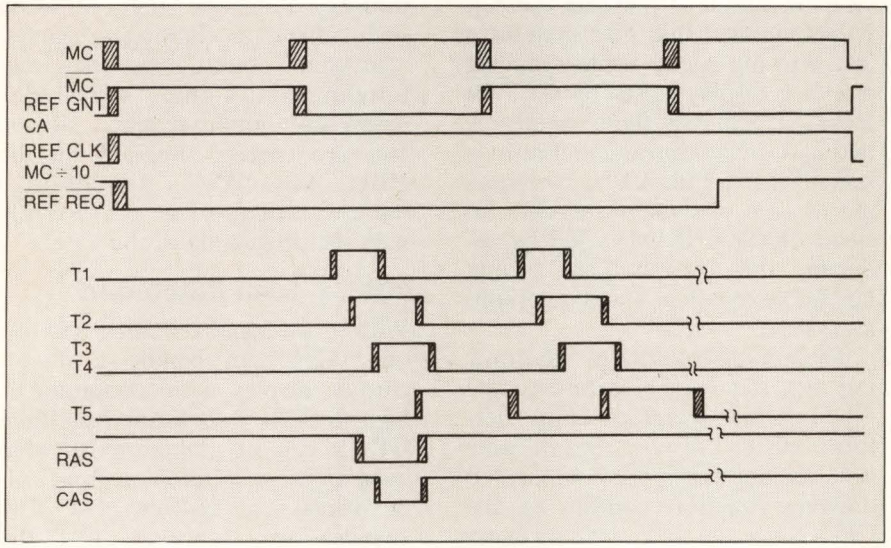

Figure 8: Timing for circuit illustrated in Figure 7.

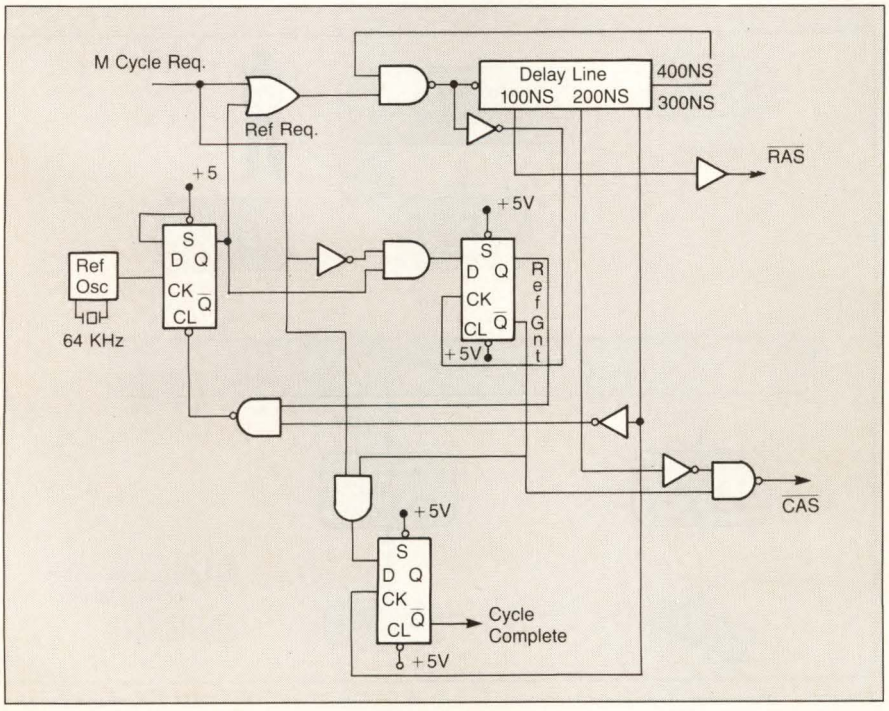

Figure 9: Cycle steal refresh scheme for asynchronous processors.

Cycle Stretch Mode

Certain components and functions of the sytem affect the system clock requirements. If slow dynamic memories are being used in a synchronous system with clock speeds in excess of 3 MHz, then the clock may have to be stopped momentarily (stretched). This same stretch method could be used to advantage in implementing refresh of dynamic memory by holding the clock off and completing the refresh requested cycle at the end of a cycle in progress. A word of caution in using this technique is that the processor clock should not be held off too long beyond a μsec, as it is possible that dynamic nodes in the processor might decay. Therefore it goes without saying that a burst refresh scheme should be avoided with stretch clock cycles. The clock stretch mode can be implemented on processors such as the MC6809.

Another variation of cycle stretch involves the introduction of WAIT states, such as in an asynchronous processor, to accommodate the pending refresh cycle request and then granting the bus back to the processor. This method could be used on any clocked CPU such as the MC68000.

Not discussed in this article are the use of memory controllers which can simplify the task of managing dynamic memory. The limitation in using memory controllers is that they might not have all the features that you need, especially if you are considering the interleaving of memory banks. The system designer should carefully weigh the contributing factors to optimize system cost and performance as there are a large number of tradeoffs which must be made. □

Graphics Chip Makes Low-Cost, High Resolution Color Displays Possible

by Mark Olson and Brad May

The making of displays that are both high-resolution and low-cost is the key to producing equipment for both the automated office and the engineering workstation. Through the introduction of 16-bit μPs such as Intel's iAPX 8088, 80186 and 80286, the processing power has been made available to perform very sophisticated functions for the user while making the human interface very simple.

That processing power can be unnecessarily drained, however, if the μP is burdened with the entire task of graphics display. Such a burden can fill up a significant part of the processor's I/O bandwidth, slow down the refresh rate of the display, and decrease the computational power of the CPU.

Intelligent peripheral ICs offload processing tasks from the CPU.

The logical way to avoid such limitations is to dedicate a specialized processor to the handling of display function. It should be capable of accepting high-level commands to minimize the burden on the CPU, as well as optimizing the execution of such commands through raster operations implemented in hardware at the device level.

Such a chip is Intel's 82720 Graphics Display Controller (GDC). It has features that give systems a fast drawing speed while reducing graphics display costs by 60% or more. It achieves these results by taking over the drawing and refresh functions from the CPU, by allowing the use of dynamic RAM's instead of static RAM's, and by reducing the overall parts count needed to create a complete graphics system.

The implementation of the drawing task is a major feature of the GDC. Other graphics chips perform only the display refresh function, leaving the more complicated drawing function entirely to the CPU. Since the CPU is doing every pixel of the drawing function on these systems, they also require faster bit map RAM than with the GDC. The GDC, on the other hand, is capable of handling the drawing function itself, drawing such objects as characters, slanted characters, points, lines, arcs, rectangles, and slanted rectangles based only upon lengths, slopes, and arc centers supplied by the CPU. The GDC's processing, moreover, takes place concurrently with the processing of the CPU.

2048 × 2048 Resolution

With its 4 Megapixel addressability, one GDC can handle a monochrome display with resolution as high as 2048 × 2048, and multiple GDC's can be linked to provide even higher resolution, such as color displays at 2048 × 2048. The chances are, however, that the GDC's full power will not be used in most applications. The typical

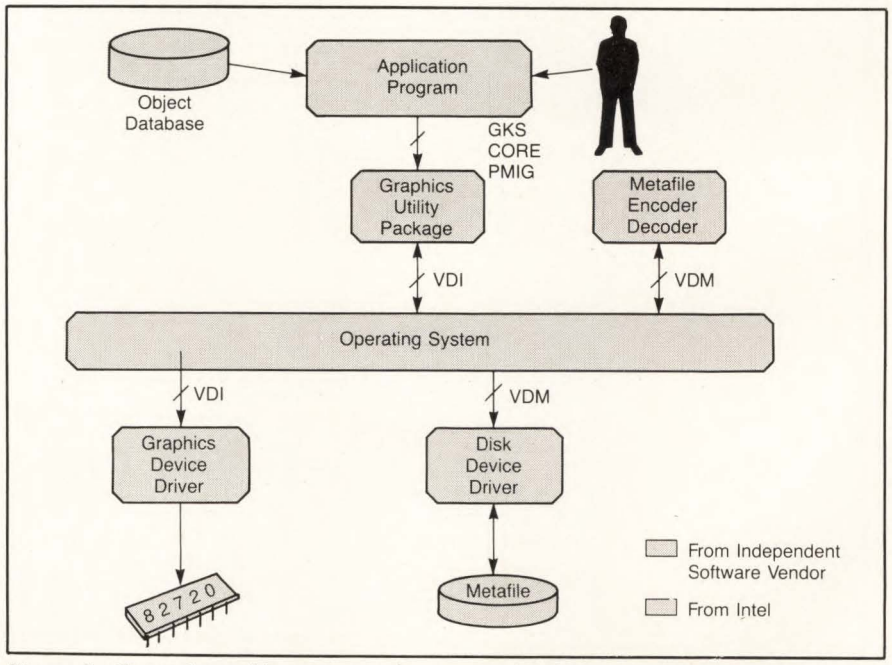

Figure 1: General graphics commands are translated into the VDI interface level and then into driver device commands.

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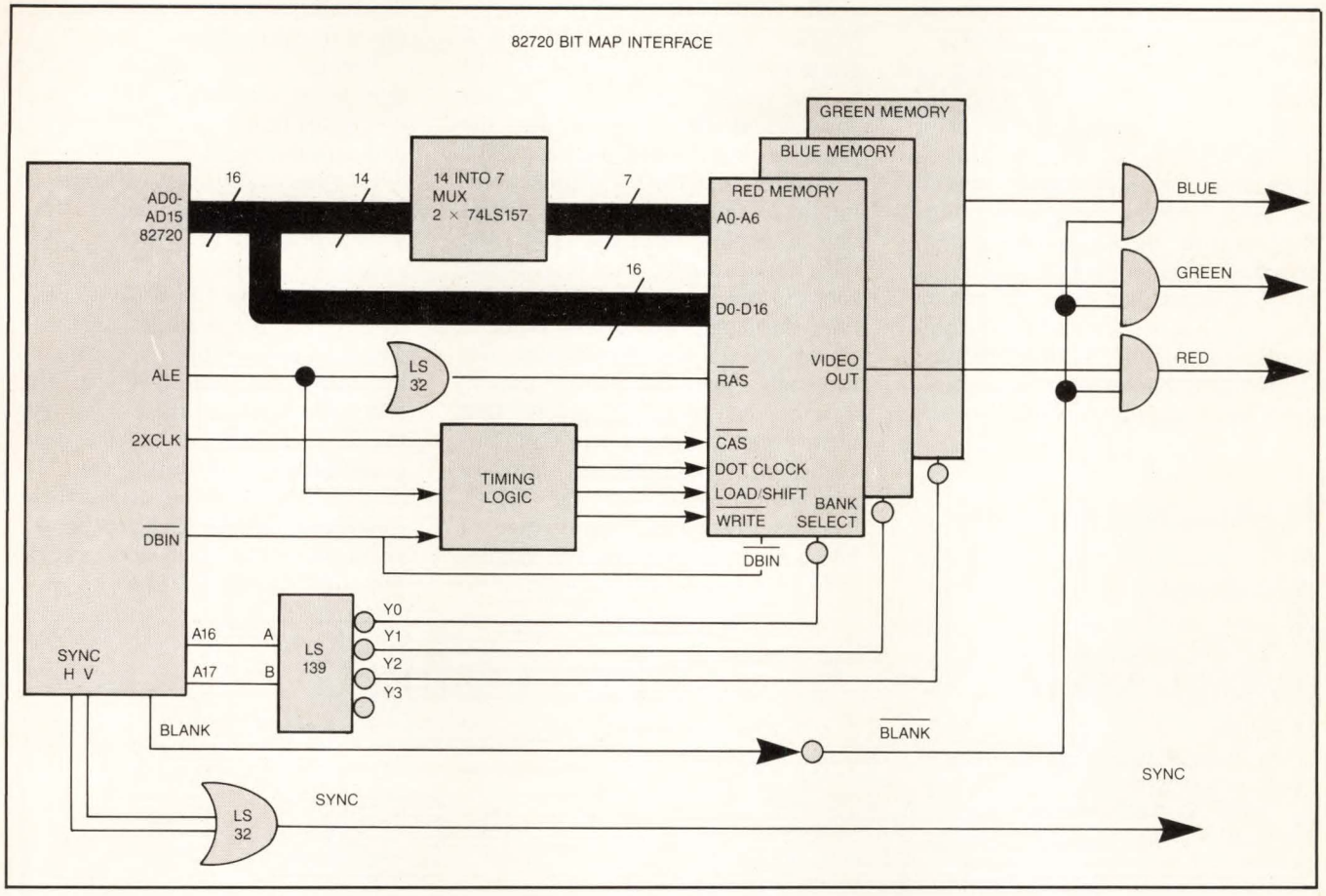

Figure 2: The memory is broken up into three planes, with each plane feeding one of the primary color guns of the CRT.

product considered high resolution for office automation applications is a 512 × 512 pixel monochrome or color display.

These latter restrictions are not imposed by the GDC, but rather have more to do with the cost of display monitors, the amount of RAM memory needed to support such displays, and the adequacy of such displays for most applications. It is possible to build "super graphics" boards with a GDC, such as the 1K by 1K pixel by 8 color plane graphics display designed by Phoenix Computer Graphics (Lafayette, LA). Such a display is capable of rendering 256 different colors on a high resolution screen.

Even higher performance can be achieved through the use of multiple GDC's to support multiple display windows, increased drawing speed, or increased bits per pixel. For multiple display windows, each GDC can be used to control one window of the display. For increased drawing speed, multiple GDC's can be operated in parallel. For increased bits/pixel, each GDC can contribute a portion of the number of bits necessary for a pixel.

Although the GDC is intended primarily for raster-scan graphics, it can also be used as a character display controller. It is capable of supporting up to four screens of data containing 25 rows by 80 columns, or one screen containing up to 100 rows by 256 characters.

Office Automation Display

High performance applications can stretch the usage of the GDC from low-end to high-end engineering displays, but research has shown that for office automation products, a 512 × 512 pixel display is quite acceptable, and that color is often a requirement. These requirements mesh with a major factor in display—the cost of the CRT. In OEM quantities, for example, one could expect to find a 512 × 512 monochrome display for under $100, a 256 × 256 color display (TV quality) for about $150, a 512 × 512 color CRT in the $300 range, and a 1K × 1K color display in the $800–$1000 category.

To give an example of the type of display that can be built for new office products using the GDC, consider a 512 × 512 pixel by 3 color plane combination CPU and graphics display on a single 12″ by 12″ board. Such a display is capable of generating 8 colors.

The list of parts (**Table 2**) comes to about $175 for 85 IC's taking up 104 square inches of board space. Even that parts count could be reduced by replacing the 48 16K DRAMs with 12 64K DRAMs—if a 4K × 16 bit DRAM were available. A very important note about the parts list is that the design is implemented with inexpensive 2118 dynamic RAMs. The design does

not require the faster, more expensive, and less dense static RAMs.

The parts count is low enough so that the processor and graphics controller can be placed together in a single 12″ by 12″ board. This is important because small overall size and footpad are selling points for desktop workstations. System speed is also enhanced when the graphics controller and CPU are on the same board, because their communication need not take up bus, inter-board bandwidth or experience any additional delays.

Pipelining Transformations

More important than putting the graphics display on the same board as the CPU is the level of communication between the CPU and graphics controller. If the burden of transformation processing is left entirely to the CPU while the graphics chip is used only as a CRT controller, then the CPU must communicate one bit per pixel to update a display. With the GDC, the CPU input takes higher level forms such as the slope and length of a line, the length and center point of an arc, or the key coordinates of a rectangle. Since the average line on a screen is about 25 pixels, that means that 25 times fewer CPU bus cycles are required to draw a graphical object with the GDC. These CPU cycles (an average of 50 μs each to calculate the graphical object and communicate it to the GDC) are the determining factor in drawing rate.

Viewed from a larger perspective, there are four tasks that must be performed by a CPU-graphics chip combination:

(1.) The CPU must calculate the higher-level graphics operations. This is done by the CPU and it involves the processing of macro-operations such as the CORE, GKS, PMIG or other graphics protocols. These general graphics commands are translated into an intermediate level, the VDI interface level (**Figure 1**) and then into device driver commands by software in the CPU.

(2.) Then, these lower-level graphical objects such as the key parameters for lines, arcs, characters, and rectangles, must be trans-

VLSI Takes Aim At Text Processing

The concept of co-processing is not a new one. Intended as a way of offloading computationally intensive tasks from a host CPU, it has been around at Intel since the introduction of the 8087 numerics processor and the 8089 I/O machine. A more recently developed product, the 82720 Graphics Display Controller is designed to bolster system performance by offloading graphics control chores from the CPU. The chip accepts high level commands from the CPU and, using its own drawing processor, accesses the required positions in the bit-map and handles the processing and display control functions.

Building on the success of these parts come two new co-processors designed to partition system intelligence even further. The 82586 is a communications co-processor designed to bridge the characteristics of CPU and network data rates. Its FIFO buffer and DMA facilities make it possible for a CPU to operate at the full Ethernet 10 Mbits/s transfer rate even in the face of continuous bursts of network data traffic.

Intel's most recent introduction is the 82730 text co-processor. Printers and other hard copy peripherals have supported additional text processing features such as proportional spacing and simultaneous superscript and subscript for some time. Implementing these features on the display screen has traditionally been a costly procedure. Thus, it is typically not done and screen displays often are not identical to their hard-copy printouts. Aimed to solve this designers headache, the 82730 has its own DMA capability and communicates asynchronously with the CPU via shared memory messages. It supports the generation of high quality text displays through features like proportional spacing, simultaneous superscript/subscript, dynamically reloadable fonts and user programmable field and character attributes. In addition, when coupled with the 82720 Graphics Display Controller (**Figure 1**) the 82730 provides flexible mixing of text and graphics simultaneously on the same display.

—*Wilson*

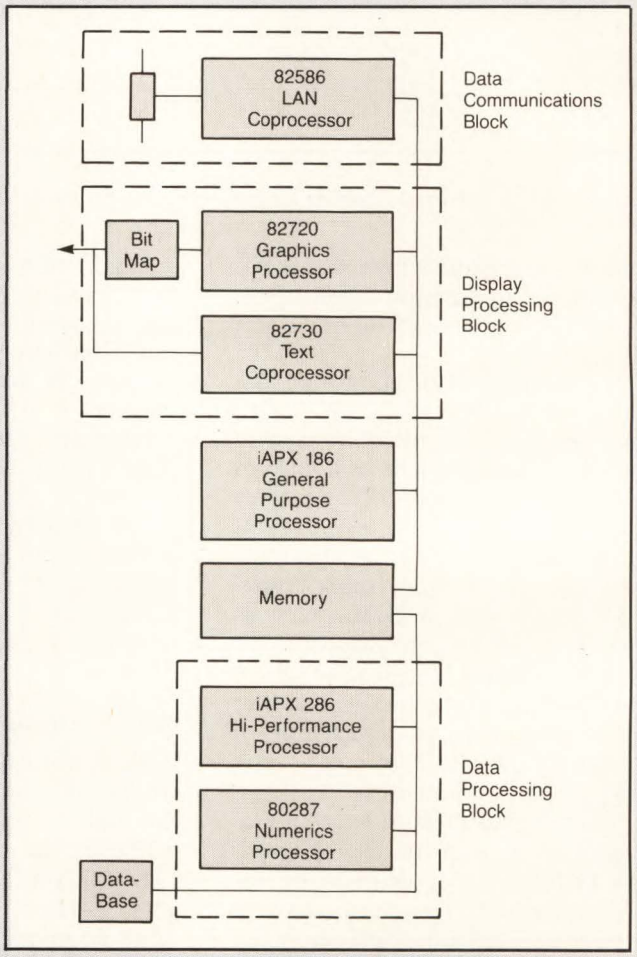

Figure 1: Offloading system tasks is simplified by new VLSI devices.

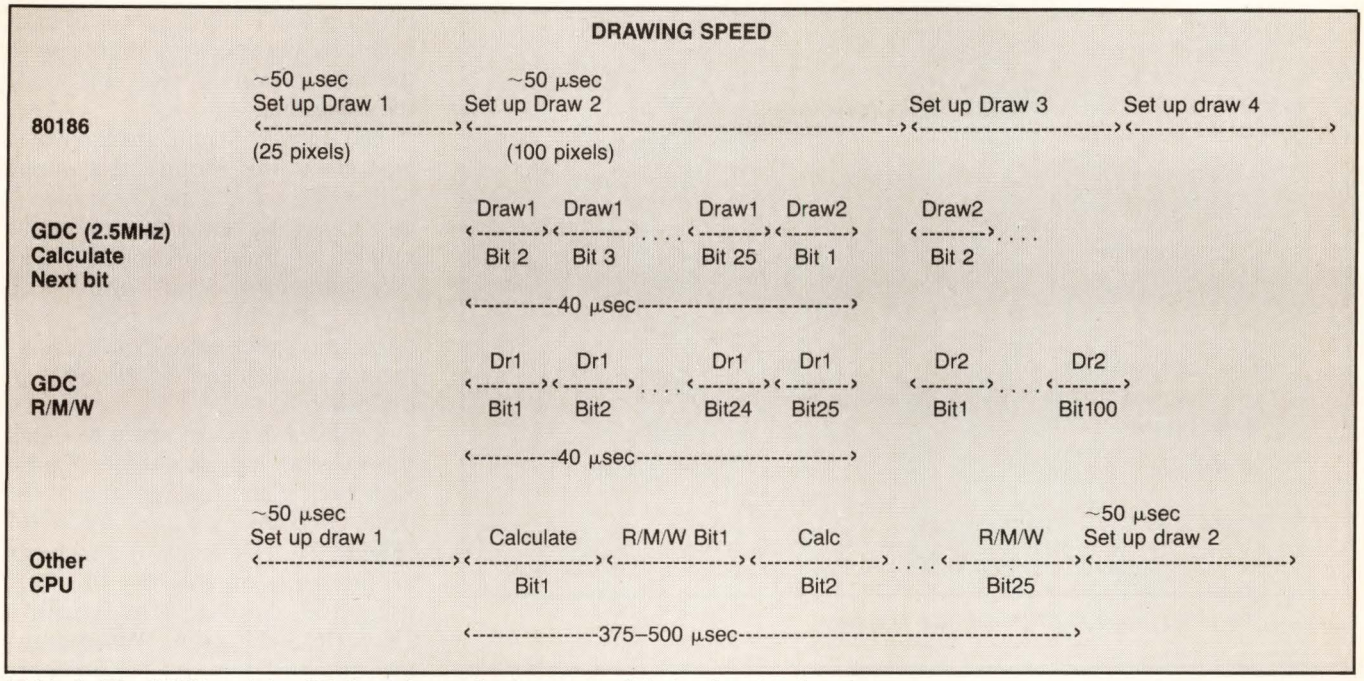

Table 1: The 80186 and the GDC work together to accomplish the drawing function.

formed into changes in the actual bits. This function is performed in hardware in the GDC concurrently with any level one processing done by the CPU. Other graphics controllers leave this task to the CPU to execute in software. The contrast is that, in such systems, the CPU must resolve the graphical object down to every point on a line, while with the GDC it need only designate the endpoints.

(3.) With the actual bits for the bit map calculated, they must be placed in the bit map memory. This involves a read-modify-write operation that requires three CPU cycles using other methods. With the GDC these operations are not the responsibility of the CPU. The GDC pipelines its execution so that it is calculating the next bit to change while it is executing the read-modify-write cycles.

(4.) Finally, the bit map memory must be dumped into the CRT. This is the refresh function performed by other graphics chips as well as the GDC.

The summation is that other systems require the CPU to process steps one to three serially, leaving only step four for the graphics controller. Systems with the GDC require the CPU to process only step one, with the GDC concurrently processing steps two through four. The GDC has another advantage in that during the transformation process in step three, the GDC executes the algorithms in hardware while a CPU must execute the algorithms in software. The algorithms are exactly the same in both cases. They are the Bresenam algorithms from IBM, in which the next pixel to be drawn becomes a binary decision between two pixels.

The execution of these algorithms is a crucial drawing time factor, because they are invoked many times for each updated screen. Consider that, in the inner loop of Bresenam's "line drawing algorithm," there are two or three additions, two comparisons or tests, and the masking of the proper value into the word for each pixel. The algorithms for drawing circles or filling areas are even more complex. In the inner loop of a fill algorithm, the old word must be read from the bit map, then tested to see if all, some, or none of the pixels are within the area to be filled. Next, it tests whether some or all of the pixels must be modified. Finally, the word must be returned to the bit map.

These algorithms are heavily used and the speed with which they can be executed has a direct effect upon the overall system efficiency. If they must be executed by a μP, the instruction fetching process slows down the calculations to a drawing rate of 15–20 μs per pixel. With a hardware implementation of these algorithms in the GDC, the calculations can be speeded up to achieve a drawing rate of 1600 ns (2.5 MHz version) or 800 ns (5 MHz version) per pixel.

Methods Of Refresh

In the fourth step, the dumping of bit map memory into the CRT, there are some differences between graphics controller chips. Motorola's MC6845 CRT controller, for example, uses a split-cycle refresh method in which each refresh cycle is alternated with a drawing cycle in which the μP updates the bit map. This gives the MC6845 a 50% drawing bandwidth.

With the GDC there are two drawing modes. The first is a "draw anytime" mode which replaces CRT refresh cycles with drawing cycles. This is the fastest mode, but it does result in on-screen disruptions. The second mode, which does not disrupt the on-screen display, draws only during the vertical and horizontal retracing periods. This gives the GDC about a 25%

1	80186	1	74LS04	1	20 MHz Clock
1	82720	1	74LS73	2	27128
2	74LS157	9	74LS244	2	2186
1	74LS139	8	74LS166	1	8274
1	74LS161	3	74LS32	1	8042
1	74LS11	2	8286	3	Connectors
1	74LS00	1	8 MHz Crystal	1	12×12 2 Layer PC

SUMMARY:

4 VLSI Controllers	80186	Processor
	82720	Graphics
	8274	Serial Link
	8042	Keyboard
4 VLSI Memory	27128	EPROM
	2186	IRAM
4816K DRAMs	2118	DRAM
29 MSI/SSI	—	Buffers/Glue

TOTAL: 85 IC'S →104 Sq. Inches

Parts Cost →About $175

Table 2: Parts list for 512×512×4 Color Display.

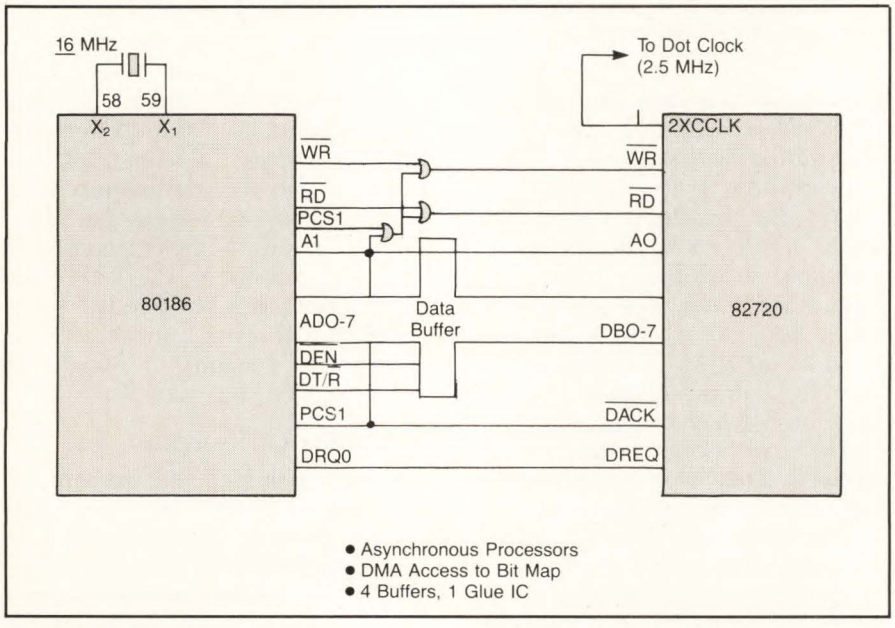

Figure 3: The two chip selects are OR'd together to qualify the R/W signals.

drawing bandwidth. At first glance that gives the GDC a disadvantage in drawing rate, but the fact is, with its pipelining and hardware execution of transformations, the GDC makes much more efficient use of its bandwidth. The critical timing factor is the amount of CPU participation in the drawing process, not the refresh bandwidth of the graphics controller. Another tradeoff is that, with its split-cycle architecture, the MC6845 requires RAM memory that is twice as fast as that required by the GDC in the same application.

Inexpensive RAM Is Fast Enough

Applying this perspective, one can begin to build the display with parts listed in **Table 2**. First one notes that a square display, as indicated by the 512×512 pixel initial specification, is not pleasing to the eye. It is much more appealing to have an aspect ratio of about 4:3, in which the number of pixels horizontally is 4/3 the number vertically. If the resolution is such that the total number of pixels is not a power of two, it will be necessary to round up to the next power of two and waste the extra bits.

The pixel arrangement which best meets this requirement is one with a 432 × 576 pixel format. It also meets the requirement that the number of pixels horizontally be an even number of 16-bit words. With three color bits per pixel (red, blue, and green), the total display memory is then about 500×500×3, or 750k bits.

It makes the most sense to break the memory up into three planes, with each plane feeding one of the primary color guns of the CRT (**Figure 2**). This leads to a memory arrangement of 16K × 16 × 3, using 16K dynamic RAMs with a 1K × 16 architecture. When drawing graphics figures, the memory can be treated as one large plane, split into the three primary colors. Drawing in low-order memory could represent red, middle-order could be used for green, and high-order for blue.

One advantage of this 3D memory is that drawing with a primary color requires setting only one bit per pixel. Drawing with a secondary color such as cyan, yellow, or magenta would take two GDC cycles, and creating white from all three colors would take three GDC cycles. If this were an issue, additional hardware could be used to draw more than one plane at a time. As the results will show, however, the drawing speed requirements can be exceeded without any added hardware.

Calculate The Drawing Rate

To see if the proposed design is practical, one should first calculate the drawing rate to see what the user interface will be like. Then one should check the refresh rate to make sure the design is uninterrupted and without flicker.

The proof of the assumption that CPU participation is the dominating factor lies in the 50 μs average time that it takes the CPU to calculate a graphical object and communicate its key parameters to the GDC. Assume that the graphical object is an average line containing

25 pixels, and that there are about 500 vectors on the average screen display.

The GDC's normal clock rate is 2.5 MHz, giving it a 400 ns period (the maximum clock rate is 5 MHz, with a 200 ns period.) It takes four GDC cycles to execute a read-modify-write on a bit (because two read cycles are required), so that the GDC's normal drawing rate is one pixel per 1600 ns. To draw the 25 pixels involved in the average line, then, would take 25×1600 ns, or 40 μs. Since this operation is done concurrently with CPU processing, the GDC will be waiting for the next graphical object by the time the CPU is ready.

If the screen were filled with nothing but 25-pixel vectors, then the drawing rate would be determined by the 50 μs average CPU calculation and transfer cycle, averaging about 2 μs per pixel. If all the vectors were white (worst case), then it would take 1.5 secs of drawing time to update the white screen. Since, in the undisturbed-screen mode, drawing is only done during the 25% of the time that the screen is undergoing horizontal or vertical blanking, this would mean 6 secs between updates.

In reality, however, the screen will not be filled with vectors. It will have an average of 500 vectors, and the color distribution could be presumed to be evenly distributed as one-third primary colors, one-third secondary colors, and one-third white. The 500 vectors will require the drawing of 12.5K pixels in monochrome, or 25K pixels with distributed colors. At a drawing rate of 2 μs per pixel, this takes 50 ms to draw. Drawing only during blanking, the screen would be updated in 200 ms.

Under these conditions, it would not help to use the maximum clock rate GDC (5 MHz), but if in some applications the average vector length is 100 pixels, then the CPU calculation-and-bus cycle (50 μs) would remain the same and the GDC's drawing cycle (1600 ns × 100 = 160 μs) would become a limiting factor. Using the 5 MHz GDC would cut that drawing time down to 800 ns/pixel, or 80 μs/vector. The 500 vector average screen would then contain 100K pixels with distributed colors and could be drawn in 80 ms. Multiplying by four because the drawing is done during blanking (25% of the time), that is 320 ms. That is a screen update in less than one-third second for a "busy" screen.

Calculate The Refresh Rate

These calculations are of little importance if the display flickers due to lack of refresh. This exercise is actually a demonstration of how the basic GDC clock rate was derived. Assume a non-interlaced display that must be refreshed 60 times per second. That gives a screen refresh rate of 16.67 ms, but on a typical CRT some 4.27 ms of that is blanked, leaving 12.4 ms of active display time. The dot sweep period is the 12.4 ms divided by the number of pixels (432 × 576 = 248.8K), or 49.8 ns. The inverse gives a 20.07 MHz dot clock.

Since the GDC dumps 16 bits from the bit map memory into the

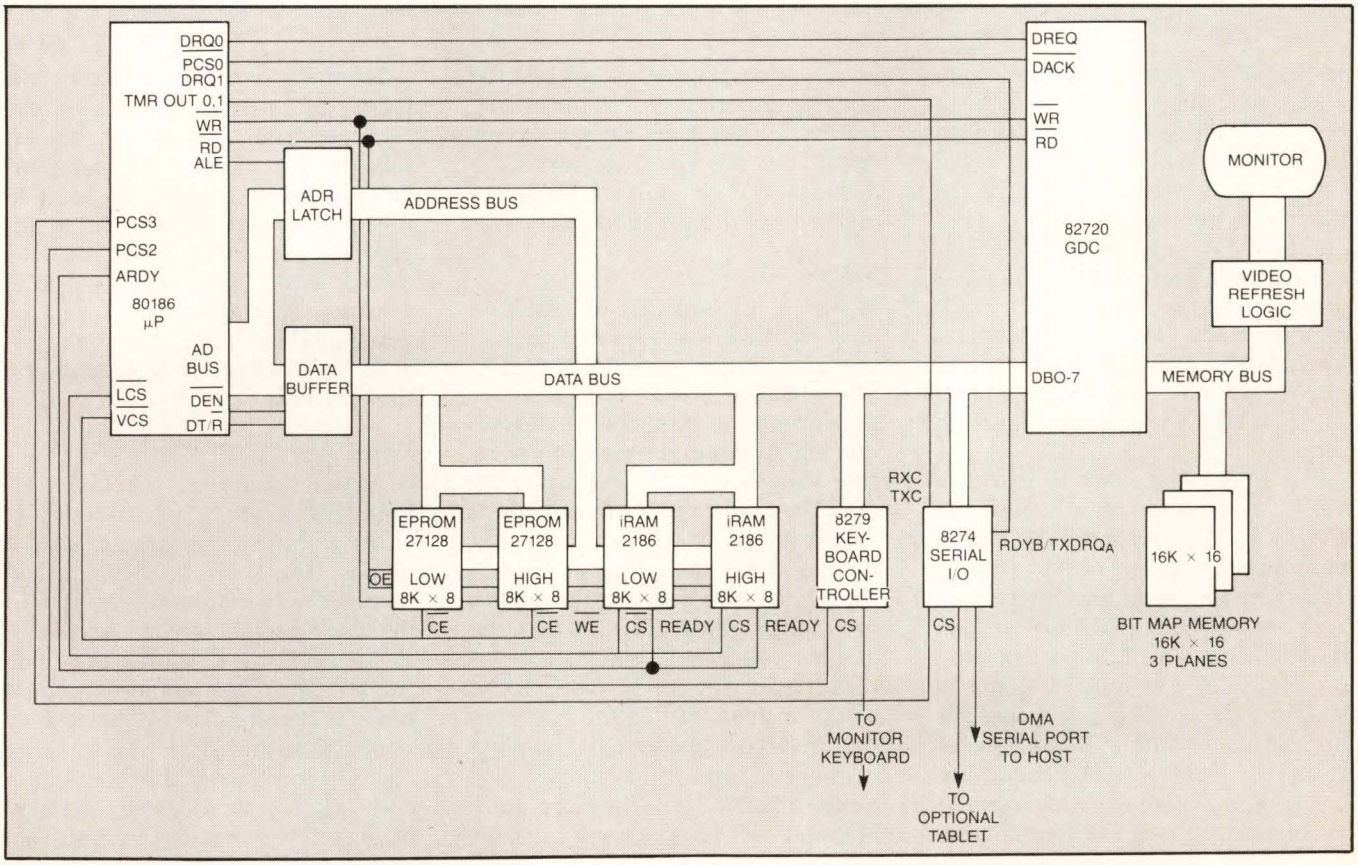

Figure 4: Completed graphics system uses the 80186 and 82720 GDC.

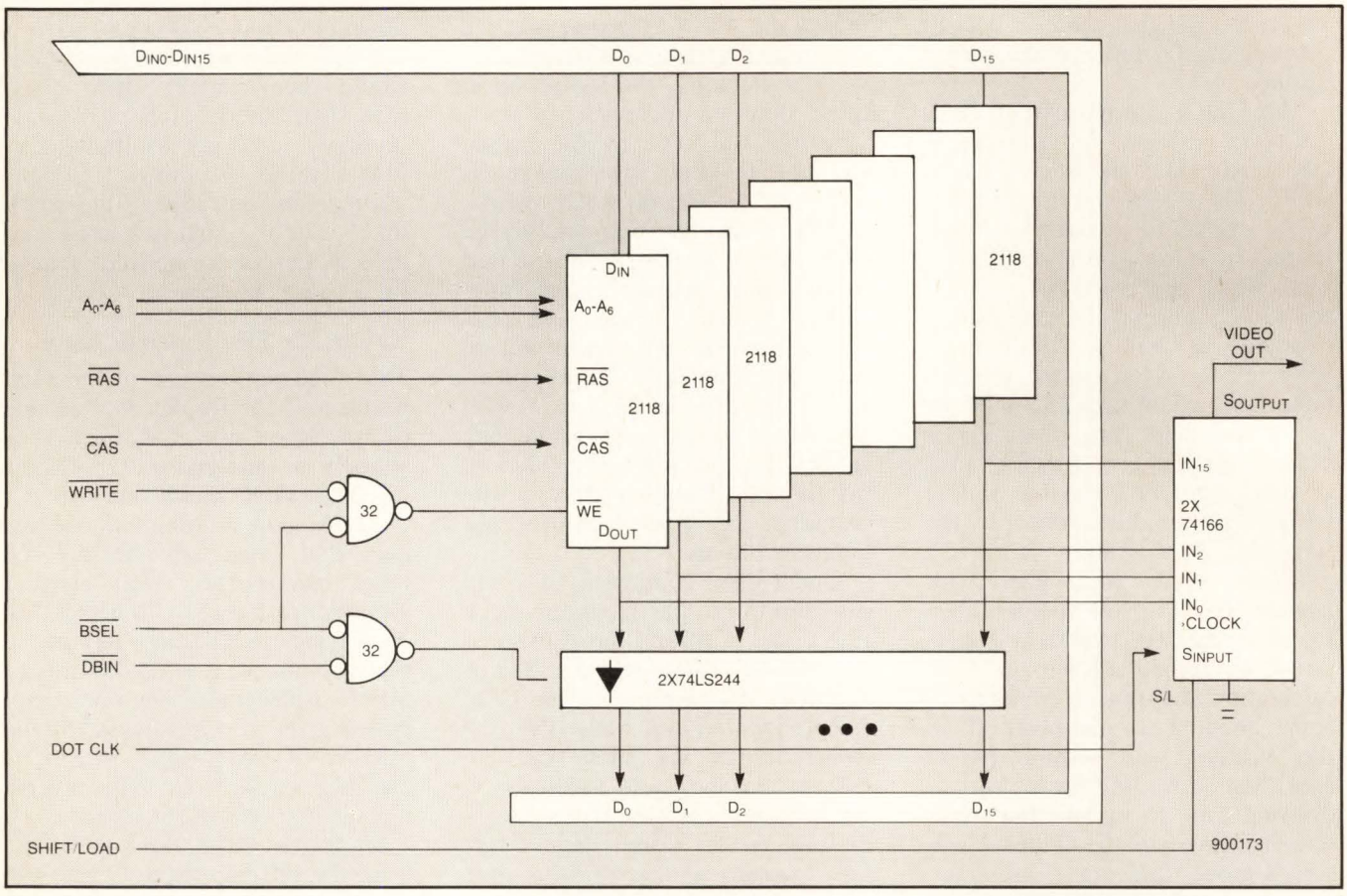

Figure 5: Since the 186 is a fully byte addressable machine, it is possible to write bytes as well as words into the RAMs.

16-bit shift register during each read, and since the shift register then feeds these bits out serially to the CRT, it makes sense that the GDC's read period should be 16 times the dot sweep period. That gives a GDC read period of about 800 ns. With each GDC read taking two cycles, the basic GDC clock period is then 400 ns, or 2.5 MHz. This gives a rock-solid display, and one would only want to go to the 5 MHz GDC to improve drawing rate.

For those who want to examine the blanking intervals to see if the CRT is indeed "typical," the blanking can be further broken down. The vertical blanking interval is 1.25 ms, leaving 15.42 ms to scan the 432 lines on the active portion of the display. Dividing 15.42 ms by 432 lines gives a 35.7 μs period per line, or a horizontal sweep rate of 28 KHz. Time is also needed for horizontal retrace, in this case, 7 μs of horizontal blanking per line. This leaves 28.7 μs to scan the 576 pixels on each line, resulting in the dot sweep period of 49.8 ns. Using a 20 MHz CRT helps keep the costs down, but the GDC can use CRT displays as fast as 80 MHz when higher resolution is required.

Mixed Mode

While it is possible to generate 8×8 characters and slanted characters in the graphics mode, the GDC also offers a mixed mode memory organization to display both characters and graphics drawn from separate windows in the display memory. The advantage of this mode is that it allows characters to be manipulated as 8-bit entities instead of the 64 bits that each would require in graphics mode. Of necessity, the graphics window display memory is reduced in this mode (64K 16-bit words instead of 256K), but even the reduced maximum graphics memory is still a megapixel and quite sufficient for both office automation and engineering display purposes.

In the character window, the GDC operates as it does in the pure character mode, with the exception that the line counter must be implemented externally. In addition to the two windows used for graphics and characters in the mixed mode, two other windows can be supported. These can be designated as either character or graphics windows by a selection on the A17 line.

Panning, Zooming, Light Pen

As special features, the GDC allows both panning and zooming in either graphics, character, or mixed modes. The zoom is accomplished by effectively increasing the size of the dots on the screen. Vertically, this is done by repeating the same display line. The number of repeat times is determined by the display zoom parameter. Horizontally, zoom is accomplished by extending each display word cycle and displaying fewer words per line, according to the zoom factor.

Panning is accomplished simply by changing the starting address of the display window. In this way, panning is possible in any direction, vertically on a line by line basis and horizontally on a word by word basis.

The GDC also features a light pen input with built-in debouncer circuitry. Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system μP that the light pen register contains a valid address.

Finishing The Design

With the basic graphics parameters of the GDC in hand, one can look back at the parts list in **Table 2** to complete the design of the graphics section. Interfacing the 82720 to the 80186 is an easy task, since the data, read, and write signals are completely compatible. However, there is no chip select input on the graphics chip. This requires that the R/W signals be qualified with a chip select signal. This can be done with two gates. The DMA channel on the 80186 uses a second chip select as an acknowledge signal, and the two chip selects are OR'd together to qualify the read and write signals (**Figure 3**).

Another piece of interfacing that must be done is the buffering of the 2.5 MHz version of the GDC on the 80186 bus. The 2.5 MHz version accesses the bus for 100 ns, while the 80186 requires that peripherals and memory be off the bus in less than 85 ns. A couple of buffers take care of this, and they are more cost-effective than going to the 5 MHz version of the GDC with its attendant faster ROMS.

Serial communication to the host system and the optional joystick and data tablet are provided by the 8274. It handles the tablet's asynchronous requirements and a host's synchronous requirements. Its interface requires the connecting of the buffered data bus, the latched lower-address lines, the R/W signals, and the chip select. One last connection brings the time/counter output from the 80186 to the 8274 to be used as the baud rate clock. No buffering of TTL glue is needed. (**Figure 4**)

The 8042 keyboard controller is used because of its clean interface to the μP. In addition, it can be programmed to scan and interpret many special function keys as well as standard alphanumeric keys.

Finally, 32 Kbytes of EPROM and 16 Kbytes of RAM are added for the μPs program and display list. The EPROM's are two 27128's which provide 32 Kbytes in two, 28-pin packages, thereby saving board space.

Interfacing the RAM chips takes more care. Since the 186 is a fully byte addressable machine, it is possible that it will want to write bytes as well as words into the RAMs. The chip select for the low (even) address RAM must be qualified with address AO at logic zero. The high (odd) address RAM must be qualified with the processor's Byte High Enable (BHE) signal. The RAMs used are the 2186 integrated RAMs; these are dynamic RAMs with built-in controllers. (**Figure 5**)

Since dynamic memories latch the address at the leading edge of the chip select, they must be qualified with the processor's address latch enable signal to insure that they are selected only after the address is valid. The 2186 latches the data to be written on the leading edge of the write pulse. This means that the 80186's write signal must be delayed by half a clock cycle to guarantee that the data is valid at the correct time.

Faster, Lower-Cost Graphics

The net result of this example is putting the graphics function on the same board as the processor at lower cost and with a much higher drawing rate than is possible with other graphics controller chips. The lower parts count results in higher reliability, greater ease of design, and a faster development cycle for getting product to market. The drawing rate can be clearly seen from a comparison to a μP-CRT controller combination. Such a system was measured at a drawing rate of 15–20 μs per pixel, compared to 1.6 μs per pixel using the standard GDC, and 800 ns per pixel using the 5 MHz GDC. □

Continued from p. 40

Acquisitions

The traditional weapon/platform acquisition process, still used for many command and control systems, follows a sequential approach from requirements definition, to advanced development, to engineering development, to fielding and support. It is a method that gives the real user little influence over the systems upon which he will eventually depend.

A new process known as Evolutionary Acquisition will provide flexibility to accommodate growth and insertion of new technology within existing systems' architecture, hardware and software. It was the subject of an official study conducted by AFCEA for the Department of Defense. In EA, a basic requirement is established, and "core" equipment designed and fielded as early as possible.

Problems of hardware and software obsolescence, saturation, decreasing maintenance support and personnel shortages will be minimized by another idea. When the United States Army decided to modernize its ADP resources, they adhered to the A-109 Major Systems Acquisition process as promulgated by the Office of Management and Budget. This required evaluation of technical proposals representing the best ADP technology available, testing alternate solutions prior to selection, and contracting with a computer services firm to ensure that the hardware and software resources procured remained state-of-the-art throughout the 10 year life-cycle.

The project, known as VIABLE, represents the first OMB Circular A-109 Major Systems Acquisition successfully completed by the federal government. Many believe this approach to be a positive trend in the acquisition and utilization of ADP resources, and one of the best ways to ensure that proven technology is transferred from the private sector to the federal government. The 10 year, $656 million dollar project managed by the U.S. Army Computer Systems Command will propel the Army 20 years in ADP technology.

Problem Areas

New acquisition strategies may solve some Service-wide problems, but others remain.

With dozens of computer makes and numerous languages in use, standardization will be receiving a top priority. Ada will help in some areas, but some believe it is not the best language for all applications. Furthermore, the high costs involved with a mammoth standardization drive make it a very political issue.

The management problem of achieving standardization while encouraging new commercial technology transfer is enormous. The balancing act calls for a projection of inventory changes to keep pace with high technology opportunities without sacrificing standardization while at the same time maintaining a training base that provides qualified personnel.

Another important area that causes grave pessimism in some circles about the utility of microelectronics is the succeptibility of chips to EMI and EMP. Major efforts are underway to find practical ways of hardening electrical circuits of all types.

Conclusion

The hardening of Free World electronic defense systems, the insertion of VHSIC into a variety of military platforms, the standardization of technologies through Ada and other means, and the incorporation of state-of-the-art commercial systems into the Defense Department lead the list of concerns in the military computer field.

If there was ever a budget item for the time and energy spent searching for solutions, it would probably be the biggest portion of the Defense pie. Much of the next two decades will be spent looking for the answers that will bring all of these systems to maturity. □

Continued from p. 42

signal is sent back to that remote location allowing the communications link to be established. Both these signals are of RS-232 EIA levels. This method works very well if the necessary software on the user's end is available to acknowledge or deny use of the communications line.

The other method of non-hardware handshaking is somewhat easier to implement since no user software is required for control. This increases flexibility, particularly where computer terminals are the remote devices, rather than μCs. This involves direct connection of the remote terminals Transmit Data line to it's associated Data Set Ready line on the multiplexer inputs. This will allow any keyboard activity to access the communications line to the host system. Since there is no "time out" provision in the multiplexer, the user has complete control of the communications link. Any other access attempts will be ignored during this "line busy" time. When the on-line user logs off, the host system must be programmed to transmit a 4 sec break signal on this port.

This configuration has proved very successful in office situations where it has been implemented and where the parameters described above are required. One minor drawback is the initial activity to access the communications link—the transmitted code does not necessarily correspond to the key pressed. This is due to the delay of the line latch-up during the serial transmission of that first character. After that, the communications link is established and all codes are completely transparent to the multiplexer and transmitted correctly. Since all remote devices are essentially sharing the same host port, they should all be configured to the same serial communications format.

Theory of Operation

The multiplexing system is accom-

plished in the following manner. Assuming that no hardware handshaking is to be used, the remote devices—Transmit Data and Data Set Ready inputs—are jumpered together. As the first keyboard activity is sensed, that associated Data Set Ready input goes high and is translated to TTL level low by U101. This is presented to U102, which is in the output follow input mode. U103 goes high, clocking U104 to generate the active low enable signal. This enable latches the outputs of U102 to their present states regardless of what the inputs do. U105 priority encoder then generates a unique address code determined by which input went low. This code in turn decodes the outputs of U107, U108, and U109 which determines which remote device is to be connected on line to the host system.

U112 and U113 are EIA level transmitters and receivers for the common communications line. U109 decodes the light emitting diodes and the Data Terminal Ready acknowledgement transmitter.

Upon log-off, the host system must transmit a 4 sec break command. This signal is translated to TTL level by U113 and presented to U110. Since this is an undisplayable code, the remote device ignores it. U110, R1, and C1 comprise a 2 sec delay to trigger only on the break command. This output is then sent to U111, a 555 high input impedance device, resulting in a high impedance state of U102. U103 changes state back to logic zero causing U106 to generate a 200 nsec low pulse to U104. This in turn presets U104 to its high state on the enable signal. U102 is now unlatched and U105 decodes this as an address which indicates the line is now free for the next user. Power supply requirements for this circuit are +5V at 1A and +/−12V at 500mA each.

Michael Sjulstad, St. Olaf College, Northfield, MN 55057.

Continued from p. 72

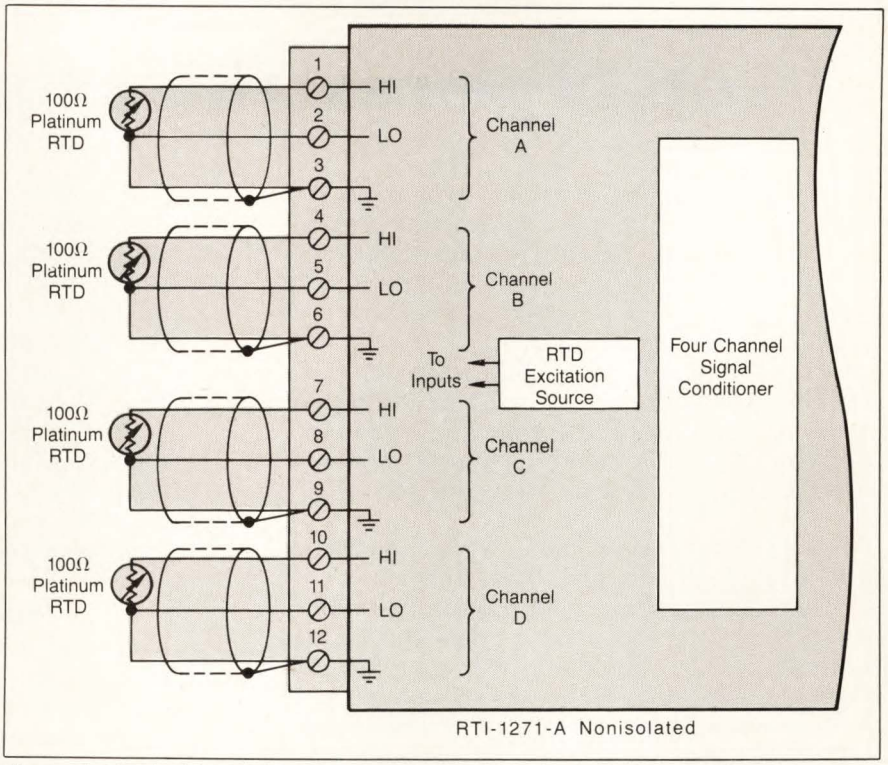

Figure 6: For highly nonlinear powered sensors such as platinum RTDs, the analog I/O provides excitation as well as all the necessary signal conditioning and linearization.

terminals on the board, and sets on-board DIP switches and jumpers to specify the thermocouple's type. With input from a reference temperature sensor located at the screw terminals, on-board firmware provides linearization and cold junction compensation of the thermocouple's output.

For highly nonlinear powered sensors such as platinum RTDs **(Figure 6)**, the analog I/O board automatically provides excitation as well as all the necessary signal conditioning.

Software, Hardware, and Service

When comparing board level analog I/O offerings from competing manufacturers, the system integrator should look carefully at both the product and manufacturer's capabilities in hardware, software and in service and support.

In comparing hardware, for instance, the user must carefully match his requirements against each analog I/O product's ability to handle the needed sensors, quantity of channels, conversion speeds, etc. In addition, bus compatibility, available on-board memory, ease of sensor interconnect and board installation, and board operating temperature range should be compared.

Although often subtle, software differences can lead to substantial savings in system development costs. On-board preprogrammed linearization, scaling, cold junction compensation, and data manipulation and format routines significantly unburden the host processor. For remote systems operating over long distance serial communications links, prospective users should closely examine the manufacturer's support of host processor communication software drivers.

Finally, and perhaps most important, the prospective user must consider the availability and reliability of technical support and service. Although factory automation can lead to substantial increases in productivity and appendant cost savings, prolonged down-time of crucial control elements can devastate the user's profitability. □

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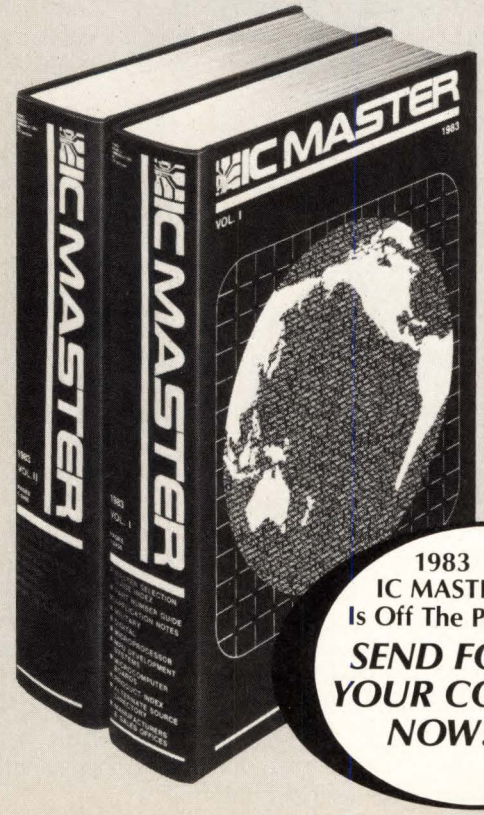

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Signature .....

Continued from p. 65

combined with Digital's VAX. Unibase claims to process data management functions up to 10 times faster than conventional software-based DBMS. Unibase consists of two processors: host and back-end. The host processor may be any member of the VAX series of interactive computers. Actual database management functions are carried out by the back-end processor, a Britton-Lee Intelligent Database Machine (IDM). Unibase prices start at approximately $120,000, including VAX 11/730, IDM 200, Unibase Software Package and 100 Mbyte of disk storage capacity.

New UNIX Ports

UniPlus, a UNIX-like operating system, has been ported to Apple's LISA personal office computer by UniSoft Systems Corp. (Berkeley, CA). UniPlus is derived from Bell Laboratories' UNIX System III and incorporates enhancements developed at the University of California, Berkeley. The Apple LISA port was completed in June 1982 to prototype hardware provided by Apple.

Human Computing Resource Corp. (Toronto, Canada) announced the availability of its version of the UNIX Operating System (UNITY) for the National 16032 μP. This development places the National 16032 μP, with its unique demand paging, under UNIX in a competitive position with the other major μPs, the Z8000, Intel 8086, and MC68000 running versions of the UNIX Operating System.

Conclusion

The software industry seems to have passed through its adolescence. The two major systems software vendors are striving to create a stable environment for applications software developers and systems integrators. Documentation, training and after-the-sale technical support are more than afterthoughts. The emphasis on standards, portability and common interfaces is an indication that the industry is willing to post some signs in the wilderness. □

Figure 5: Starfield computers combine UNIX, MC68000 and the Multibus.

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

	Page #	Write #
Add-In/Add-On Memory		
dy-4 Systems	111	194
Communications		
Acromag	105	132
Components, Hardware, Packaging		
Adirondack	**111**	**47**
Keytronic	**43**	**19**
NSG	**8**	**41**
BEI Electronics	113	202
Data Instruments	110	200
Computer I/O		
Amkey	**46**	**14**
Cortron	110	163
Texas Instruments	104	149
U.S.I. International	110	197
Computers/Systems		
Advanced Technology Labs	**103**	**43**
Analogic	**61**	**18**
Andromeda Systems Inc.	**107**	**36**
Aptec Computer Systems Inc.	**50**	**31**
CDA	**25**	**35**
Chrislin	**77**	**46**
CSPI	**53**	**15**
Distributed Computer Systems	**113**	**49**
Florida Computer Graphics	**37**	**4**
Leading Edge	**2**	**1**
Racal-Vadic	**1**	**2**
SD Systems	**54**	**11**
Sonics	**30**	**39**
SKY Computers	**95**	**33**
Vectrix	**35**	**24**
Molecular Computer	105	137
Oracle Corp.	104	143
Pheonix Data Systems	105	145
RAIR Computer Corp.	106	146
Robotrol	113	191
SKY Computers	111	189
Wild Heerbrug Instruments	106	155
Controllers, Interfaces		
Data Systems Design	**C4**	**5**
MDB	**4**	**3**
Huerikon Corp.	111	199
Hard Copy		
General Electric	**49**	**30**
Nicolet Zeta	**17**	**25**
NSA	**69**	**37**
Envision	108	184
Hewlett Packard	108	185
Sanyo	106	178
Veisatec	108	174
Mass Memory		
Amdek	**21**	**12**
Camintonn Corp.	**111**	**48**
Control Data	**19**	**10**
Dataram	**26**	**28**
Genisco	**38**	**20**
Innovative Data Technology	**115**	**42**
Memodyne	**20**	**45**
Moya	**91**	**91**
MPI	**22**	**26**
TEAC	**16**	**50**
Cipher Data Products	110	165
Dylon	106	180
IDT	113	42
Imperial Tech. Inc.	106	173
Innovative Data Tech	108	166
Remex	108	177
Power Supplies, UPS, Line Conditioners		
ACDC Electronics	113	203
Semiconductors, ICs, μPs		
Universal Semiconductor	**6**	**6**
General Instrument	110	198
Software		
International Micro-Systems	104	135
Oregon Software	105	144
Silvar Lisco	105	148
Test, Instrumentation, Development		
Optum Electronics Corp.	104	142
Tektronix	110	171
Video Display, Image Processing		
Aydin	**13**	**27**
Comtal	**59**	**21**
Datacube	**10**	**29**
Elector	**27**	**22**
Epson	**C3**	**16**
Intelligent Systems	**15**	
Lundy	**9**	**7**
Modgraph	**11**	**8**
Raster Technologies	**2**	**17**
Vectrix	**35**	**24**

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IC Design: Stand Alone Systems Are Now The Way To Go

The concept of totally integrated computer IC design parallels the developments in computer aided mechanical design. Both fields have opened market niches that have been attacked by start-up companies offering solutions to specialized sections of the design problem. These systems offer an inexpensive way for the engineering manager to introduce his staff to the concept of computer aided design since many are based around μP board level products.

However, a closer examination of the engineering problems involved in both IC and mechanical design shows that there is no quick "stand-alone" or "under $10,000 solution" at present.

For this reason, some managers are wary of entering the field at all, preferring to wait until the "perfect solution" walks through the door.

A more positive approach may be to invest in a system that offers the capabilities for inexpensive expansion and utilization of existing computer power. CAE Systems of Sunnyvale, CA feels that the purchase of a stand alone system with proprietary hardware will restrict the "room for expansion" concept. For this reason they have chosen to offer a system (the CAE 2000) based around the Apollo Domain that incorporates a Multibus backplane.

When they defined the engineering workstation, they addressed the electrical design cycle from behavioral definition through physical layout and testing. Other companies have concentrated on the front or back end of the process. Some have limited themselves to PCB or IC design, but not both.

On the 2000, users are guided by a series of menus using a "mouse" and graphics tablet, which positions the cursor over the on-screen menu instructions. The user then touches a button on the mouse to execute the command. Using a component library, a designer can call up models and structures previously defined and use them to construct schematics. Chip area, power estimates, resistance, and signal path timing provide the designer with comparative measures to aid in the design process.

Analysis spreadsheets can be placed anywhere on the screen. As an engineer modifies a design, he can observe the values change on screen and try a number of design possibilities. The CAE 2000 emulates both a programmable pulse generator for stimulus input and oscilloscope for circuit outputs. The programmable pulse generator lets the designer construct each waveform and change the time domain. Setting parameters specifies pulse waveforms for logic stimulation; continuous waveforms for circuit stimulation can be generated mathematically or drawn with a movement of the input device.

The CAE 2000 is available in two configurations: the CAE 2000-A, priced at $88,690 (quantity one) comes with four software packages that contain a basic schematic capture capability with on-line help and electronic mail, documentation for an engineering notebook, waveform capability and a modeling language that lets users interface to mainframe simulators. It also includes the timing verifier and the logic simulator.

The CAE 2000-B priced at $39,990 includes a software package that contains the basic schematic capture capability with on-line help and electronic mail.

—Wilson

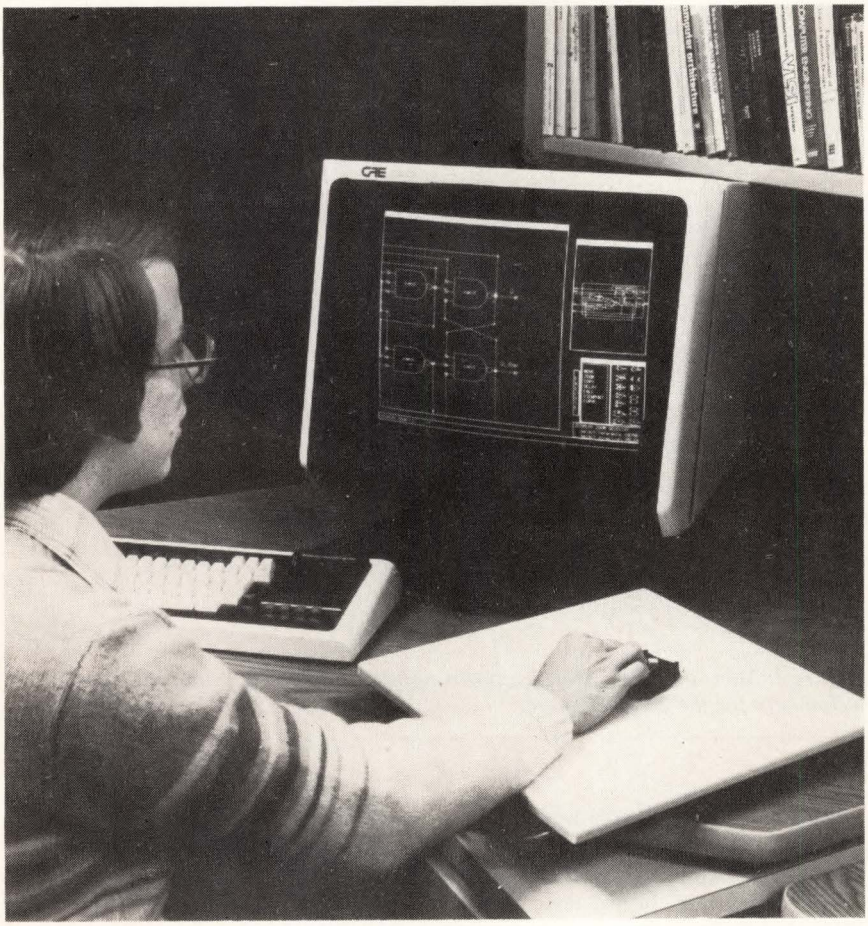


Figure 1: A "mouse" guides the CAE 2000 workstation.

New Hardware Supports Enhanced Multibus Architecture

Following quickly behind the announcements of the iLBX and Multichannel enhancements to the Multibus will come six new board level products from Intel.

The new family contains the iSBC 286 single board computer, three high performance RAM boards, a new universal memory expansion board, and a link to the high speed Multichannel I/O Bus (**Figure 1**). The iSBC 286/10 SBC sits at the high end of Intel's SBC spectrum. Fully compatible with software written for the iSBC 86 and 88, the iSBC 286/10 improves performance two to three times over the earlier system.

The iSBC 286/10 provides what Intel calls Universal memory site expansion, allowing the designer to custom configure memory on the board. Designers can mix different kinds of byte-wide memory devices such as RAM, iRAM, EPROM and EEPROM throughout the board's eight, 28-pin JEDEC sockets. Each site is organized into two 4-site blocks, one of which can be dual ported.

In these configurations, EPROM memory is expandable to 192 kbytes using twelve 27128 16k × 8 EPROMs. On board RAM can be upgraded to 80 Kbytes using ten 2186 iRAMs.

Adding to the versatility of the Multibus iLBX bus environment are the new iSBC CX memory boards. Three CX memory expansion boards are supported with capacities of 128k, 256k, and 512k bytes. Each has error correction and detection capabilities via Intel's 8206 ECC device. Dual porting gives the board access to both the Multibus and the iLBX-bus. In addition, a new iLBX bus compatible universal site memory board, the iSBC 428, will be available for flexible EPROM, EEPROM and RAM configurations.

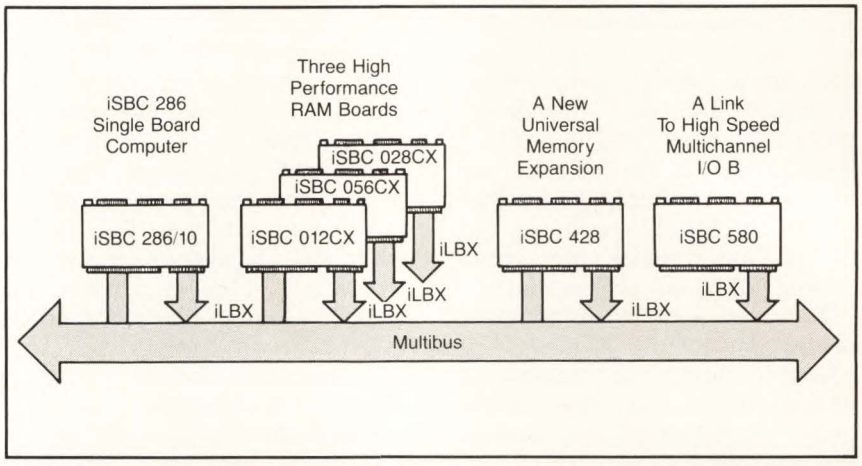


Figure 1: Six new board level products are available to support 286-based designs.

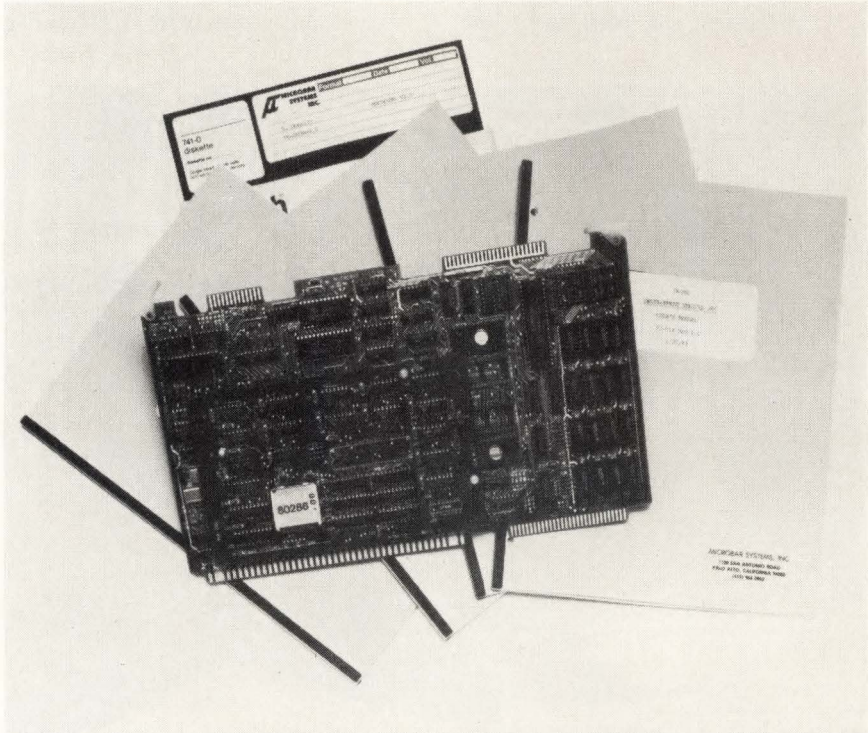


Figure 2: Microbar Systems development vehicle, the DV286, supports software development for the 286 processor.

Total system performance can be further enhanced by combining the Multichannel with the iLBX bus, with a new board (the iSBC 580) supplying the link. Acting as a talker and listener on the Multichannel, the iSBC 580 transfers data between the Multichannel and system memory via the iLBX bus, thus bypassing the Multibus.

This procedure allows other system tasks to use the Mutibus resource while high speed I/O block transfers are taking place.

Operating system support comes from iRMX 286R and Xenix. Each has features suitable for real time or general purpose data processing systems in industrial and commercial markets. Further, the iSBC 286/10 is supported by Intel's Intellec Series III development system via a new debug monitor, the iSDM 286. There is also a host of programming languages including ASM 86, PL/M 86, Pascal and Fortran in the 8086-compatibility mode. Pascal and C will be available later for the protected mode.

In advance of the iSBC 286/10, customers can begin software and system development with the iSBC 286/10ES evaluation kit. Included are the iSBC 286/10ES CPU board, an iSBC 012CXES 512 Kbyte RAM board, an iSDM 286ES System Debug Monitor and system documentation.

Software development for the 286 processor is also supported by Microbar Systems recent development vehicle, the DV286, that works with CP/M 86 and CP/M 80 based development systems, or Intel development systems running the 8086 assembler.

The 80286 Development Vehicle is utilized by first installing MACRO286, Microbar's 80286 instruction macro package, and by installing the "execution vehicle" on a host development system. The "execution vehicle" is a Multibus, IEEE 796, compatible board (**Figure 2**) containing the iAPX286 μP and has full virtual memory capability.

Software can be developed on the host system and then loaded to the execution vehicle over an RS-232 port for execution, testing and debugging. Debugging is facilitated with PROM based DEBUG286 which provides single instruction execution, breakpoint setting, memory disassembly, and examine/modify of memory, I/O, and registers.

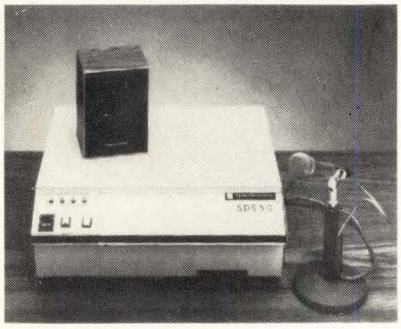
The DV286 is priced at $2495 and consists of the "execution vehicle," a single Multibus board featuring the Intel 80286 μP, 128 Kbytes of on board memory expandable to 16 Mbytes; DEBUG286, a PROM based 80286 debugger; MACRO286, a set of 80286 instruction macros; and documentation.

—Wilson

SPEECH DEVELOPMENT SYSTEM

Real-Time Speech Processing Capabilities

As a real-time speech-development system, the SDS50 can instantly translate spoken words into LPC (linear predictive coding) speech data and produce synthesized speech. It also allows users to edit LPC speech data via any RS-232C compatible terminal. The pitch, energy, and vocal-tract



configuration can be modified by the user, then produced through the loudspeaker to immediately hear the result. Commands can also be given to store the results in EPROMs by use of an optional built-in EPROM programmer. Words and phrases processed by the SDS50 require less than 1.8 Kbit/sec of memory space. Up to 12 sec of speech can be accommodated in the system's 16 Kbytes of available RAM. The SDS50 consists primarily of 4 μC boards: a custom processor board, TM990/101MA CPU board, TM990/201-43 memory board, and one of a choice of speech synthesizer boards. The enclosure can also accommodate a TM990/302 PROM programmer for users that want the EPROM programming option. **Texas Instruments**, PO Box 401560, Dallas, TX 75240. **Write 149**

MEASUREMENT SYSTEM

Fully Automated, Multi-Channel System

Optilog PLUS incorporates the Optilog Integrated Data Acquisition and Control System, the Apple II Plus Computer with dual floppy disk drives and Optim's MAGS (Measurement And Graphics System) software, Featuring 16-bit resolution and scanning speeds up to 250 samples/sec, it can be configured with 10 to over 1000 channels (analog or digital/input or output). Integral signal conditioning includes internal cold junction compensation and constant current and constant voltage and energization

sources which are fully programmable on a channel-by-channel basis. Interactive software routines allow menu selection of functions. Additional programs can be written in BASIC or FORTRAN and any Optilog units in the system can be connected to other host computers. **Optim Electronics Corp**, 16021 Industrial Dr., Gaithersburg, MD 20877. **Write 142**

EPROM PROGRAMMING SOFTWARE

Automates Use Of IM Multi-Master EPROM Programmers

For the production manager who has large quantities of EPROMs to burn, this software package can solve "housekeeping" problems associated with EPROM production inventories. Software is written in "C". It produces user-friendly graphics on most operating systems to facilitate downloading to the programmer, identifies

human and EPROM errors and maximizes throughput. The system eliminates the need for master EPROMs in the production environment. The program allows operator interaction on three levels of computer control. The first level permits setting the typical parameters associated with every set of EPROMs. The second level incorporates the first with the addition of logging pass/fail information. The third level adds complete external computer control of the production programmer's display and keyboard. Interfacing is compatible with the IM3016 Multi-Master EPROM Programmer featuring 16 programming sockets. The system is capable of programming any number of sets and set sizes by using a series of IM3016s. Complete systems including software and one IM3016 Multi-Master EPROM Programmer with 16 socket EPROM module begin at $9,985. Software only for installed IM3016s is $2,995. **International Microsystems, Inc.**, 11554 C Ave., Auburn, CA 95603. **Write 135**

RELATIONAL DBMS

For Use On Mainframe, Mini, And μCs

As a large-scale DBMS, ORACLE offers multi-user capabilities and automatic recovery from system failure in batch and on-line environments involving data bases as large as billions of characters of data. In addition, ORACLE provides an interactive application generator; report writer; word processing and document preparation system; and integrated

data dictionary. Version 3 currently runs on IBM mainframes with the VM/CMS operating system; DEC VAX-11 and PDP-11 minicomputers; Data General 16- and 32-bit Eclipse minicomputers; and Motorola 68000-based μCs running under UNIX. ORACLE will soon be available on other 68000-based operating systems, as well as on Intel 8086-based operating systems, as well as on Intel 8086-based μCs and on IBM mainframes with the MVS operating system. The Version 3 ranges between $600–$48,000. **Oracle Corp**, 3000 Sand Hill Rd., Menlo Park, CA 94025. **Write 143**

CAD SYSTEM

For VLSI Design Verification

Logic may be simulated more comprehensively—up to 99 states are possible—with virtually no restriction on device size due to LOGCAP 400's 10 million node capacity. Multiple logic states are generated to discern interactions between logic level, logic mode and logic strength at each node. There are three levels (0, 1, X), three modes, (Driven, Stored and Unknown) and 16 strengths for each driven and stored mode. Its fault simulation capability verifies design simulation integrity; faults may be introduced singly or concurrently. After fault simulation, LOGCAP's test grading feature reports the percentage of faults detected. The input patterns and simulated ouputs may be saved and automatically converted into VLSI tester programs. The system also provides an English-like language with subcircuit nesting, an extensive element library and user-defined network descriptions. **Phoenix Data Systems, Inc,** 80 Wolf Rd, Albany, NY 12205. **Write 145**

MULTI-USER

Support 32 or 64 Users

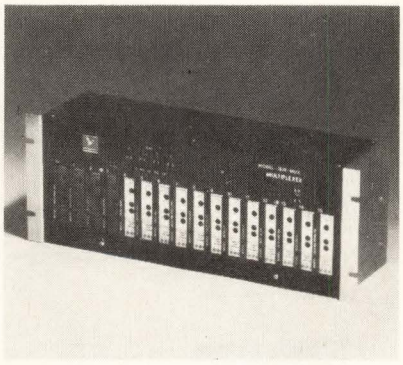
The Supermicro 64X supports 64 concurrent users and has a 136 Mbyte disk capacity expandable to 272 Mbyte. The Supermicro 32X supports 32 concurrent users and has a

60 Mbyte disk capacity expandable to 240 Mbyte. Both systems feature Z80B-based File Processor with 256K of RAM and doubled bus transfer rates of 400 Kbytes/sec. New "X" series Application Processors (individual Z80A 64K processing boards, one for each Supermicro user) are available. Operating under its own proprietary n/STAR Network Operating System, the Supermicro series is compatible with all CP/M and CP/M-86 application software packages. n/STAR provides extensive file management facilities including all CP/M operations plus powerful record locking features for concurrent file sharing, system password security, private and common user files and print spooling. All Supermicros are modularly designed to support increased disk capacity, streamer tape backup and 16-bit shared processing options. The basic Supermicro 64X with 136 Mbyte disk capacity. 500 Kbyte floppy and 32 Application Processor slots lists for $22,995. The Supermicro 32X with 60 Mbyte capacity, 500 Kbyte floppy and 32 Application Processor slots lists for $18,995. "X" series Application Processors list for $995. **Molecular Computer**, 251 River Oaks Parkway, San Jose, CA 95134. **Write 137**

ANALOG MULTIPLEXING SYSTEM

Provides Parallel Or Serial Interface

The 1874-S Serial Version of the 1874-MUX interfaces to the host device via an RS-232C, RS-422, or isolated 20mA current loop (user selectable). It features selectable baud rates from 110 to 19.2K baud, throughput speeds of 300 channels/sec (at 19.2K baud), and a pre-formatted ASCII command/reply set. Multiple 1874-S units may be connected via a multidrop



configuration providing a maximum capacity for interfacing up to 16,384 analog channels. The 1874-P Parallel Version provides a parallel digital interface for analog I/O signals. It employs a simple "handshake" protocol and interfaces directly through the host's thumbwheel switch cards or TTL I/O cards. The data is transferred between the host and the 1874-P over logic lines, on a per-channel basis, in either 12-bit binary code, or as a 3- or 4-digit (field selectable) binary coded decimal (BCD). **Acromag, Inc,** 30765 Wixom Rd, Wixom, MI 48096. **Write 132**

INTEGRATED SOFTWARE SYSTEM

Automatic Placement and Routing

The SL-2000 software set accommodates the entire gate-array or standard-cell-based design cycle from architectural definition to chip layout without the need for device physics expertise or topological design experience. The system can also assist in the design of printed circuit boards, back-

planes and programmable logic arrays. Automatic functions are design iterations, interface to simulators, interactive hierarchical mapping, automatic placement and routing, and design-rule checks. SL-2000 is designed to execute VLSI designs on any IBM-compatible CPU, DEC and PRIME minicomputers, APOLLO workstations and a wide variety of graphics terminals. Output tapes from the design program interface directly with interactive graphics systems from CALMA, COMPUTERVISION and APPLICON, for generation of artwork. **Silvar Lisco,** 1801 Page Mill Hill Rd., Palto Alto, CA 94304. **Write 148**

PASCAL COMPILER

For PDP-11 UNIX Systems

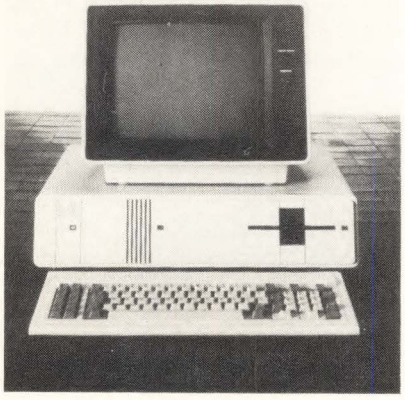
Pascal-2, a second-generation Pascal compiler, features a multipass operation. It generates compiled code that is 30% to 40% smaller and twice as fast as the Pascal-1 compiler. Pascal-2 compiler and debugger are targeted to users of PDP-11 hardware with the UNIX-operating system. The debugger allows the programmer interactively to solve—at the level of the source program—logic errors in applications, thus simplifying and speeding development. The debugger runs separately from the application code being debugged, keeps track of multiple compilation units and performs breakpoint debugging without slowing the application code. The profiler aids the applications programmer by identifying execution bottlenecks. License fees for Pascal-2/UNIX begin at $3950. **Oregon Software**, 2340 SW Canyon Rd., Portland, OR 97201. **Write 144**

New Products • COMPUTERS/SYSTEMS

MULTIUSER μC SYSTEM

Multiworkstation Computer For The Business Environment

This desktop business system supports up to four user workstations with 19 Mbytes of Winchester storage, up to 1 Mbyte of user RAM, and



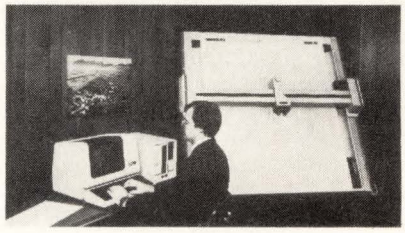
8 and 16-bit μPs to run 8 and 16-bit applications software concurrently. The multitasking operating system is compatible with both 8 and 16-bit versions of popular CP/M and MP/M programs—plus PC-DOS as used on the IBM Personal Computer, 16-bit implementations of BASIC, COBOL and Pascal are supported, as well as electronic spreadsheet, word processing, database management and communications packages. Each workstation comprises an ergonomic low-profile keyboard and high-resolution color display. Optional workstation printers are available eliminating the need for sharing a central printer. An entry-level, single-user system, configured with 19 Mbyte Winchester and 1 Mbyte floppy drives and 256 Kbytes of RAM is $8,500. Memory upgrades in 256 Kbyte increments are $1,500. User workstations are $1,500. Quantity, OEM and dealer discounts available. **RAIR Computer Corp,** 4101 Burton Dr., Santa Clara, CA 95050.

Write 146

CAD/CAM SYSTEM

2D System For Precision Layout

This system, designed around the Wild TA2 precision plotting table, can produce either pen plots, scribed Mylar or cut Rubylith with .0008″ accuracy and in any scale up to the full 48×48″ table surface. The Fortran software program uses English language prompts and incorporates linear and circular interpolation, scaling, rotation, macro generation and storage, on-line editing and cutter offset (etch factor compensation). Uses in-



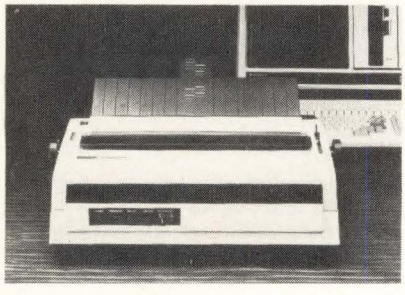
clude the production of precision artwork and layouts, such as optical comparator charts, site gauges, templates, circuit masks or chemical machining masks. Completing the CAD/CAM system is a DEC LSI 11/23 computer, a DEC VT100 terminal with graphics board, a 10 Mbyte Winchester disk and additional 1 Mbyte floppy disk. Complete turnkey system is $99,950. **Wild Heerbrugg Instruments, Inc.,** 465 Smith St., Farmingdale, NY 11735. **Write 155**

New Products • PERIPHERALS

DAISY WHEEL PRINTER

Adjustable Typing Pitch

Features include adjustable typing pitch, bi-directional printing and will handle 17″ wide paper. Minute horizontal ($^1/_{120}$″) and vertical ($^1/_{48}$″)

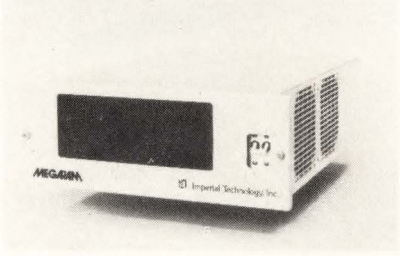


movements allow a range of printing functions. The PR5500 has bold-face, subscript, superscript, double strike, underline as well as microjustification to interface with the software supplied with the computers. The PR5500 is compatible with most word processors and any other computer offering a centronics parallel interface. $995. **Sanyo,** 51 Joseph St., Moonachie, NJ 07074 **Write 178**

DISK EMULATING SYSTEM

Rotating Unit Equivalent

The MegaRam-11 is configured with a Unibus interface and can be used on the PDP-11, PDP-11/70 and VAX series of computers. The system is avail-



able with a dual port capability and can be equipped with an internal battery back-up option. The unit is packaged in a 19″ rack-mounted chassis requiring only 7″ of vertical rack space and up to 8 Mbytes of storage. Expansion up to 28 Mbytes can be accomplished by daisy-chaining chassis. the system can be configured in 2 Mbyte increments. **Imperial Technology, Inc.,** 831 S. Douglas St., El Segundo, CA 90245. **Write 173**

MAGNETIC TAPE SYSTEMS

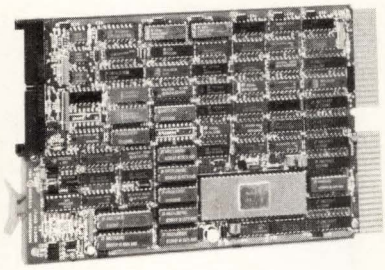
Compatible With H-P Computers

Features include tape speeds to 125 ips and densities of 800/1600 or 6250 bytes per inch, reel sizes of 10½″, 8½″ and 7″ fit any H-P computer system.

The family also includes HP-IB and IEEE-488 controllers for ½″ reel to reel and ¼″ cartridge recorders. **Dylon,** 9561 Ridgehaven Court, San Diego, CA 92123. **Write 180**

GET THE POWER YOUR Q-BUS SYSTEM WAS DESIGNED TO GIVE

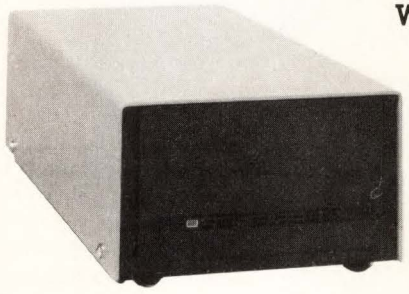
It's Plug-In Simple with Remarkable DEC-Compatible Technology from Andromeda Systems



The WDC11 Triple Function Compatible Controller: Its Power is Amazing Versatility

Interfaces with 8- and 5¼-inch Winchester and floppy disk drives, and includes an intelligent bootstrap ROM. This LSI-11 compatible Controller emulates these standard DEC devices: RK-05, RL-01/2, RP-02, RX02.

That's only a **sampling** of the freedom of selection you have with the WDC11 Controller. It adds performance to your LSI-11 computer system. Easily and cost-effectively.



Winchester Add-On Subsystems: Their Power is Speed, Storage Capacity, Reliability, Compactness, and Low Cost

Get major throughput gains from your LSI-11 floppy-based system at a cost you can live with. Andromeda's popular MDS series, with a 5¼-inch Winchester drive, has a data transfer rate **over eight times** that of an RX02 floppy! Standard DEC emulations are available. Includes built-in bootstrap and formatting.

All Andromeda Winchester Subsystems will quickly and conveniently cover your mass storage needs for today and tomorrow.

Complete Turn-Key Computer Systems: Their Power is Big Overall Performance for Small Space and Cost

One totally integrated package includes computer and disk drives. For example, the 11/M1-W (pictured) holds a standard 5¼-inch Winchester disk drive, 2 x 5 card cage, control panel, and power supply.

Andromeda Turn-Key Computer Systems are easily expandable, and may be custom-configured to fit your processing requirements, space constraints and budget. Specify 8-inch disks if you wish, or dual drives, or floppies...or a combination.

Andromeda is the Q-Bus specialist. Our single objective is to develop fine products that unleash the power that is inherent in your DEC LSI-11 system.

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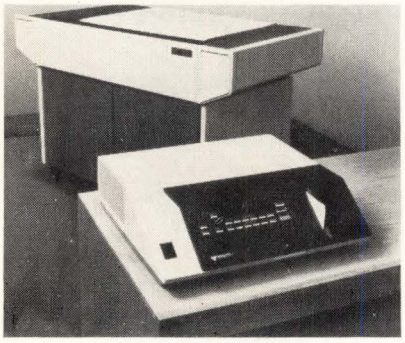
Write 36 on Reader Inquiry Card

APERTURE CARD RASTER

Translates Card Images To Hard Copy Plots

Scanning 200 lines per second, ACRIS reads up to three card/min. with output resolution of 200 by 200 scans per inch. Plots can be scaled up or down in size. Features include thresholding,



background adaptability, line detection, and line growth minimization. Self calibration of lamp and denity concurrent with the initial lines of each scan maintains image quality. Functional diagnostics provide continuous monitoring. Versatec plotters offer compatible 200 point resolution, selectable line enhancement, and a paper and polyester film media. ACRIS connects directly to Versatec 11, 22, 24 and 36″ plotters via standard Verstec interface. Communications interface supports line speeds from 1200 to 56K baud via RS-232 or RS-449 modems. Data is sent in compressed raster format under SDLC subset protocol. ACRIS Model 930 is $13,500. **Versatec,** 2710 Walsh Ave., Santa Clara, CA 95051. **Write 174**

5¼″ FLOPPY DRIVE

Half Height

The RFD 485 (48 tpi) and RFD 965 (96 tpi) double-sided drives (single-sided versions are available) are half the height of a standard minifloppy drive. Measuring 1.61″ behind the bezel, these new drives allow users to expand existing capacity by replacing one full-size drive with two half heights. 1 Mbyte of capacity is available on the RFD 965 and 500 Kbytes on the RFD 485. Features include a self-centering clutch and spindle design which improves media to spindle registration and LSI circuitry that reduces the size of the logic board. The bezel is removable and interchangeable with three sizes which can be installed in the field. One model provides complete interchangeability with existing full size units and can reduce problems in the transistion from full to half size drives. The head(s) on the RFD 485/96 is loaded onto and unloaded from the media surface via a mechanism engineered into the door operation. The RFD 965 drive has a 3ms track-to-track access time (5ms for RFD 485), and the MTBF of the direct drive brushless DC motor is 30,000 hours. **Remex Div.,** 1733 Alton St., Irvine, CA 92713. **Write 177**

PLOTTER MODULE

For Handheld Computers.

The HP-41 handheld computer, with the plotter module, is connected to the HP 7470 graphics plotter via the Hewlett-Packard Interface Loop (HP-IL). For remote applications, the HP-41C is attached to the HP-IL interface loop during the actual recording of measurements. The module stores information gathered by instruments in the HP-IL loop and the HP-41C is brought back to a central base where it is attached to the HP 7470 to pro-

duce plots. For bench-top use, the plotter and HP-41C with a plotter module are linked together with the HP-IL. With the plotter module connected to an HP-41 handheld computer and an HP 7470 graphics plotter, bar code can be created for the HP 82153A optical wand and scanning devices in other bar-code systems. Multi-color line graphs, bar charts and text pages also can be created with the HP-41, plotter module and HP 7470 graphics plotter. The plotter module is $75. **Hewlett Packard,** 1820 Embarcadero Rd., Palo Alto, CA 94303. **Write 185**

5¼″ WINCHESTER DRIVE

Removable Media, Fixed Media, Dual Media

The Cardiff family of 5¼″ Winchester drives are fully compatible in size, power requirements, interface and data transfer rate with currently available μCs and controllers. Features in-

clude a Closed Loop Servo Positioner with a voice coil linear motor that makes high speed positioning of the R/W heads possible with no increase in drive depth over standard 5¼″ floppy drives. Dynamically loaded R/W Heads are loaded on a rotating disk surface. Any possibility of damage during shipment is eliminated. Low power consumption and the use of only +5V and +12V supplies allows drive to be powered by any standard 5¼″ floppy or Winchester disk drive power supply. Demonstration units will be available during the first quarter of 1983. **Innovative Data Technology**, 4060 Morena Blvd., San Diego, CA 92117 **Write 166**

COLOR PRINTER

Pen Plotter Capability And Letter-Quality Printing.

The VectorPrinter combines pen plotter capability with high-speed, letter-quality alphanumeric printing, without the need for vector-to-raster converter. Its features include: a simple software interface for easy programming, compatible with Hewlett-Packard's HGL plotter protocol for color graphics, letter-quality alphanumerics, printed at 125 cps, and high-resolution graphics, using 300 dots per inch horizontally. It also includes a variety of type fonts, including elite, pica, orator, italics and bold, and an ability to print multi-part forms. **Envision,** 505 Hamilton Ave., Palo Alto, CA 94301. **Write 184**

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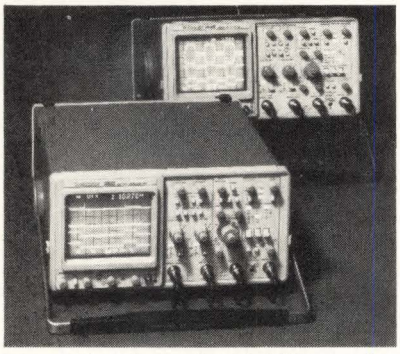
New Products • PERIPHERALS

OSCILLOSCOPES

Front Panel Layout

The 2445 and 2465 analog scopes are designed to replace the 465B and 475. The 2465 has 300 MHz bandwidth, 500 picosecond per division sweep speed, and an auto-level trigger feature with trigger bandwidth greater than 500 MHz. The 2445 has 150 MHz bandwidth, 1 ns per division sweep speed, and the same triggering features with trigger bandwidth to 250 MHz. The 20.3-pound scopes have four full-bandwidth vertical channels, each with calibrated scale factors and positioning controls. The CRT readout generates cursors which the user can superimpose on the waveform to measure delta voltage, delta time, frequency, phase, and ratio. The readout displays trigger threshold voltage, sweep delay and delta delay times, and vertical and horizontal scale factors. **Tektronix Inc.**, PO Box 500, Beaverton, OR 97077. **Write 171**



½" TAPE DRIVE

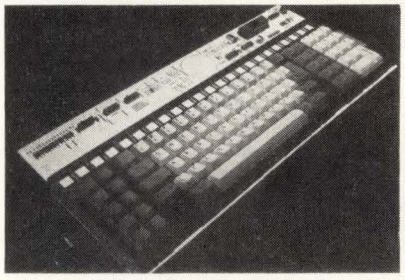
File Sort Capabilites And Tape Processing

Cache Tape 75 ips tape drive provides file sort capabilities and tape processing, in addition to the traditional file save/restore functions of ½" backup and performs backup functions in an on-line environment. It allows users to continue primary processing without interruption, and provides background file save/restore functions. The tape drive backs up 80 to 300 Mbyte high performance Winchester disk drives. A 3200 bpi version is also available for increased capacity. Its functional capabilities include: file-oriented disk backup, physical disk image backup, transactional journaling, tape merge/sort, tape interchange, data archiving, and data acquisition. $2,820. **Cipher Data Products, Inc.**, P.O. Box 85170, San Diego, CA 92138. **Write 165**

LOW PROFILE KEYBOARD

Full Surface Multistation Keytop

Features of the FC 2500 keyboard are solid state ferrite core linear or tactile "feel" keyswitches and full multistation keytop, as well as +5VDC operation, LED indicator, and selectible baud rates. The keyboard is TTL compatible with ergonomically designed keytops and has a multiple mode selection. **Cortron**, 400 W. Grand Ave., Elmhurst, IL 60126. **Write 163**

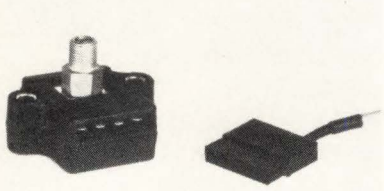


New Products • COMPONENTS

PRESSURE TRANSDUCER

For μP Based Applications

The EAF pressure transducer's output signal is a frequency modulated square wave with a nominal 5kHz range, set from 1kHz to 6kHz. The EAF features 11 pressure ranges from 0–6 psi to 0–5000 psi. Each unit is computer trimmed for calibration and temperature compensation to insure unit to unit interchangeability of +/− 1%. Unit accuracy, including effects of non-linearity, hysteresis and repeatability, is within +/− 0.5% of span from best fit line. Typical applications include refrigeration systems, agricultural sprayers, engine controls and monitors, compressors, transmissions and medical instruments. $68 in 1000 piece quantities. **Data Instruments Inc.**, 4 Hartwell Place, Lexington, MA 02173. **Write 200**



32K ROMs

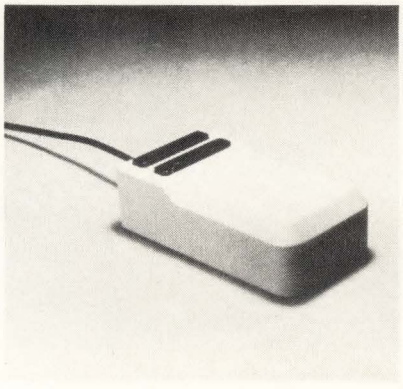
Electrostatic Discharge Protection

Designated the RO94132B, RO94132C and RO94132D, the ROMs feature MOS N-Channel Silicon Gate ION-implanted technology, 4096 × 8 organization, fully static operation (no clocks required), single +5V ± 5% operation, and TTL compatibility. Access times are 450ns for the RO94132B, 300ns for the RO94132C, and 250ns for the RO94132D. Pricing in 10,000 piece quantities is $1.65 for the RO94132B, $1.71 for the RO94132C, and $1.82 for the RO94132D. **General Instrument Corp.**, 600 W. John St., Hicksville, NY 11802. **Write 198**

OPTICAL MOUSE

Uses 5 Volts of Power

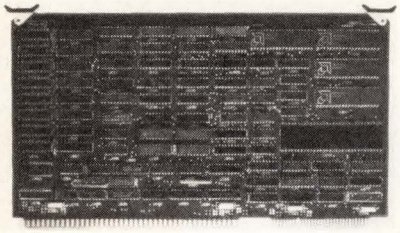
The OptoMouse requires 5V of power from the host system. Controlled by its own μP, it can emulate existing graphics protocols such as Tektronix Plot 10 and Summagraphics bit pad, and the required host interface is reduced to a simple RS-232C serial port. OptoMouse functions include scaling, relative position or directional speed and will address any pixel on the CRT screen. It is available in several configurations to meet specific user needs and CRT types. **USI International**, 71 Park Lane, Brisbane, CA 94005. **Write 197**



FLOATING POINT HARDWARE

For MC68000

The SKYFFP single card processor is capable of a 3.0 μsec floating point add/subtract/multiply on 32-bit single precision data, and 12.0 μsecs for 64-

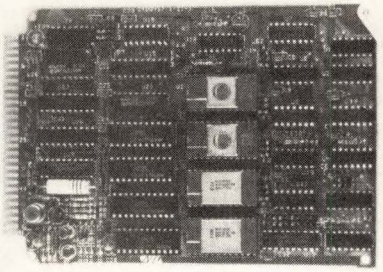


bit double precision data. The SKYFFP performs basic operations such as add, subtract, multiply, and divide, as well as square root, logarithmic and trignometric functions on IEEE standard 32-bit single precision and 64-bit double precision floating-point data. It is designed to be completely transparent to the user, requiring no modification to existing FORTRAN, Pascal or C programs. Under $1000. **SKY Computers, Inc.**, Foot of John St., Lowell, MA 01852. **Write 189**

MEMORY MODULE

12 Byte Wide Sockets

The board provides 12 byte wide memory sockets that can be individually configured for any type of byte wide memory device. Each socket can



be positioned independently anywhere in the processors address space on 4K boundaries. The card supports memory paging through the use of a high speed mapping RAM allowing use with either the Z80 or 8088 processor on the STD bus. The DSTD-503 allows the use of a variety of byte memory devices including RAM, ROM, EPROM and EEPROM in 2K × 8, 4K × 8, 8K × 8 and 16K × 8 configurations. The DSTD-503 is available in both 2.5 and 4.0 MHz version. **dy-4 Systems Inc.**, 888 Lady Ellen Place, Ottawa, Ontario, Canada K1Z 5M1. **Write 194**

GRAPHICS CONTROLLER

Programmable Color Look-Up Table

MLZ-VDC is an intelligent graphics controller with Z80-A CPU, DMA controller, 132 byte FIFO on the Multibus for buffering command flow. It has up to four 28-pin sockets allowing up to 32K of EPROM/ROM and 16K of RAM, 24 bit addressing with complete master/slave or multimaster capabilities, bus map to define board position, and one Intel compatible iSBX expansion module connector. It has a μPD7220 Graphics Display Controller for both graphics and character generation, 512 Kbytes of on-board memory organized as 1024 × 1024 × 4, standard display window of 640 × 480 × 4 either interlaced or non-interlaced, programmable color look-up table allowing a display of 16 colors out of a palette of 4096, and an integral light pen interface. **Heurikon Corp.**, 3001 Latham Dr., Madison, WI. **Write 199**

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800/262-4208.

Mini/Micro 83

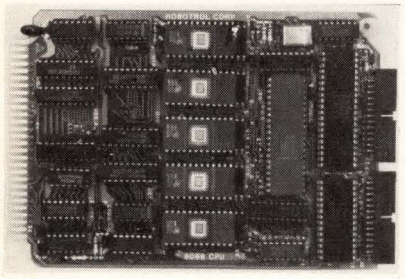
Mini/Micro Northeast New York Coliseum, New York, NY	April 19 - 21	**Mini/Micro Midwest** O'Hare Exposition Center, Chicago, IL	Sept. 13 - 15
Mini/Micro Northwest Portland Coliseum, Portland, OR	May 10 - 12	**Mini/Micro West** Brooks Hall, San Francisco, CA	Nov. 8 - 11

Produced by Electronic Conventions, Inc., 8110 Airport Blvd., Los Angeles, CA 90045, 213 772-2965.

SINGLE BOARD COMPUTER

For STD Bus

The RSD-8088 features the 8088 μP whose internal architecture provides 16 bit wide registers, a 16 bit ALU and a set of 16 bit instructions identical to that found in the 8086 μP. Features include: 16 bit 8088 CPU running at 4.77 MHz; RS-232 serial I/O channel with software programmable baud rate; 20 programmable parallel I/O lines usable with or without handshaking; five 28 pin bytewide memory sockets jumper configurable for 24 pin or 28 pin EPROM or RAM. It also has bytewide memory sockets to support nonvolatile EEPROM; 256 bytes of additional on-board RAM; wait state generator, and on-board interrupts for serial and parallel I/O. **Robotrol Corp**, 1250 Oakmead Pkwy, Suite 210, Sunnyvale, CA 94086.

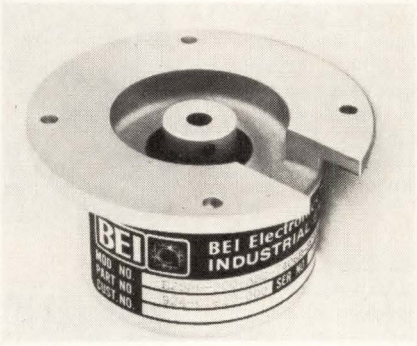


Write 191

ENCODER

Integral Coupling

The E25 Series has patent pending integral coupling that allows the user to have less than perfect mechanical interface, accepting axial play to ± .030″, radial misalignment to .010″ and angular misalignment to 5°. Designed for the OEM market, this unit is available in resolutions up to 2540 counts per turn in quadrature with or without zero reference. It features easy mounting, no alignment, self-centering, no signal degradation with time or temperature (0° to 70°C) and is a warranted separable product. **BEI Electronics, Inc.**, 7230 Hollister Ave., Goleta, CA 93117.



Write 202

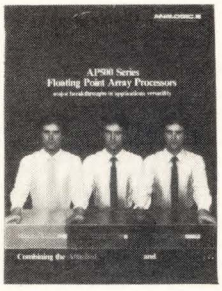
SWITCHING POWER SUPPLIES

Use UL/CSA Components For High MTBF

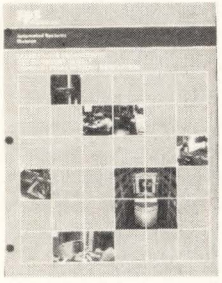
RE800 Series features include: 24V, semi-regulated forth channel available for motors, solenoids, relays, etc.; auxiliary output currents of up to 30A (RE802); industry standard 5″ × 8″ × 11″ profile, mounting patterns and connections; wide input range (90-132 VAC, 165-250 VAC, 180-264 VAC), user selectable; and a complete 800W family of singles, duals, triples and quad output models. The range of standard options include AC power fail, output-out-of-tolerance, and direct parallel. From $875, OEM discounts available. **ACDC Electronics**, 401 Jones Rd., Oceanside, CA 92054.

Write 203

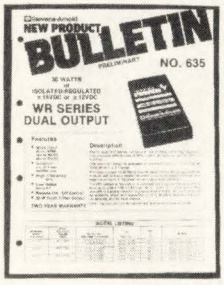
New Literature



Point Array Processor Brochure. A new 16-page, four-color brochure, introducing the new AP500 Series Floating Point Array Processor available from Analogic. The brochure contains sections on hardware/software design concepts, configuring a system, application versatility, as well as complete specifications.
Analogic Corp. **Write 261**



Automation Systems Pamphlet. Six-page full-color brochure details the design, engineering, and project installation capabilities of the SPS Technologies Automated Systems Division. The hardware subsystems include rotating carousel storage, miniload stacker cranes, storage shelving, wireguided order pickers, robotic vehicles, and pneumatic tube transport. Realtime data management and control systems maximize total system productivity.
SPS Technologies **Write 260**



DC/DC Converter Data Sheet. A two-page technical data sheet provides product descriptions, applications information, and electrical/mechanical specifications on Stevens-Arnold's new WR Series 30-watt DC/DC converters. The WR Series consists of six dual output DC/DC converters that provide outputs of ±12VDC @ 1.25A or ±15VDC @ 1.0A from inputs of 12, 24, or 48VDC.
Stevens-Arnold **Write 259**

Data Communication Devices Catalog. Black Box Catalog, Inc. announces the publication of the 1983 Edition of their Black Box Catalog of Data Communication Devices. This Data Communicator's "Bible" contains 282 data communications oriented products, many never before offered. Every product is carefully described and illustrated with photos and diagrams and includes prices.
Black Box Catalog **Write 258**

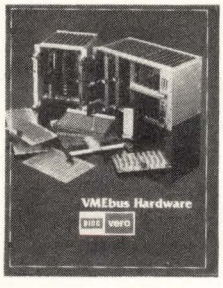
Circuit Board Brochure. An 8-page brochure describing double-sided and multilayer printed circuit board production capabilities is being offered by Microfab. Illustrated with color photos, the 4-color brochure lists all major equipment for prototype to production quantity manufacture of PCBs with 7 mil or greater lines and spaces for a wide range of commercial and military applications.
Microfab **Write 257**

Monitors And Accessories. Six new Amdek monitors with special interface cables are featured in a new 4-color, 10-page catalog. The new monitors (Models Video 300, Video 310, Color I, Color II, Color III, and Color IV) are designed for use with most personal or small business computers. The catalog includes compatibility charts and specifications for all the monitors.
AMDEK Corp. **Write 256**

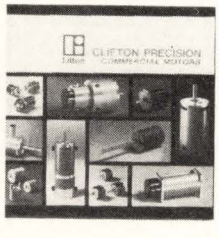
Keyswitch Series. A 4-page brochure describes the new DN series keyswitch series from Mechanical Enterprises Incorporated. The series features SilverLock, a proprietary contact design using a silicone rubber tube to protect high performance silver contacts from the effects of the environment. It shows the range of switch styles and mounting configurations.
MEI **Write 255**

Membrane Keyboards Brochure. SMK Electronics is offering an 8-page brochure that details their custom membrane keyboards. The brochure provides technical information including membrane types, typical specifications, membrane keyboard construction, conductive circuitry, graphic overlays, shielding, special features and more.
SMK Electronics Corp. **Write 254**

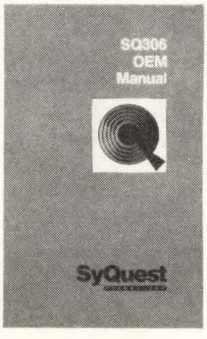
Access Control Products. Cardkey Systems full-color brochure was designed to highlight each product on separate insert pages. The products shown range from a simple two-door card access system to a computer-based system that can monitor multiple high-rise buildings and assist in facility management.
Cardkey **Write 252**



VMEbus Compatible Products Catalog. Bicc-Vero Electronics, Inc. has designed a μP bus for the Motorola 68000 series processors to implement the current 16 bit devices as well as future 32 bit devices. The 8-page catalog contains all the mechanical items needed by the designer working with the VMEbus including backplanes, extender boards, prototyping boards, card cages, power supplies, and connectors.
Bicc-Vero Electronics, Inc. **Write 266**



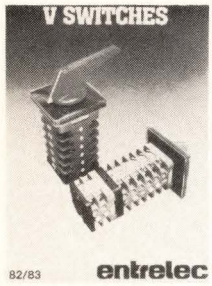
Commercial Motors Catalog. Clifton Precision has published a 30 page catalog of control motors. The line of servomotors, tachometers, encoders, and stepper motors have found applications in digital tape transports, line head, and disk memory head positioners. Variations of models are available as well as designs for unique applications.
Litton **Write 251**



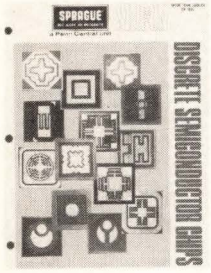
Winchester Disk Drive Manual. SyQuest manufactures and markets 100mm removable and fixed Winchester disk drives. Model descriptions for the drives are as follows: 100mm removable Winchester disk drive, 100mm fixed Winchester disk drive, and cartridge disk for the SQ306R.
SyQuest **Write 250**

New Literature

Sequential Controller Brochure. A comprehensive 8-pp. brochure describes the new 2020 programmable controller featuring 24 general-purpose inputs, 16 open-collector outputs and a switch mode power supply for world-wide compatibility. The brochure contains sections on system capabilities, and a programming worksheet to set up 256 steps of machine control operations including time delays, monitoring and counting functions.
Control Technology Corp. **Write 268**

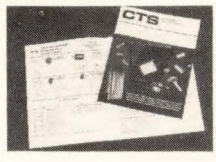


V-Switches Catalog. Entrelec, Division of Cogenel, Inc., has published a detailed, 36-pp. catalog of its cam-operated, type V, modular rotary switches for on/off, selector, and power control operations in instrumentation, motor control, distribution panels, and machine tools. Included in the catalog are complete technical specifications, mounting diagrams, and application drawings for 10, 18, 32, and 55 ampere sizes.
Entrelec **Write 267**



Semiconductor Update. Sprague Electric Company's expanded line of discrete semiconductors for hybrid-circuit assembly is described in a newly revised short-form catalog, CN-164J. The updated 20-pp. catalog contains dice geometries and technical information on hundreds of popular U.S. and European transistors and diodes, jumper chips and MOS capacitor chips, and a description of semiconductor-chip packaging.
Sprague Electric Co. **Write 263**

CM2020 Card Modem Brochure. Intertel's CM2020 modem, the smallest 1200 bps single-card modem commercially available, is featured in this 4-pp. brochure. The CM2020 is an FCC-registered Direct Connect device compatible with Bell's 202S for half duplex operation on a 2-wire switched network. The brochure highlights the modem's microprocessor-based design which allows full on-board auto dialing, self testing and auto answering.
Intertel **Write 262**



OEM Electronic Components Catalog. Complete electrical and mechanical specifications for 46 CTS OEM electronic component lines are detailed in a new 36 page condensed catalog just published by CTS Corporation. Products covered include cermet resistor networks; trimmers; DIP and rotary switches; hybrid circuits and loudspeakers. Each product series has fully detailed photographs and illustrative drawings.
CTS Corp. **Write 264**

Data Communication Products. IDS' complete line of data communications equipment, including a variety of synchronous and asynchronous limited distance modems, terminal, port and modem sharing devices, and modem eliminators is described in an expanded, free catalog. This current catalog represents the consolidation of the company's several guides into one 41-page publication.
International Data Service **Write 265**

Advertiser Index

Adirondack Wire & Cable . . . 111
Advanced Technology Labs . . . 103
Amdeck . . . 21
Amkey . . . 46
Analogic . . . 61
Andromeda Systems . . . 107
Aptec Computer Systems . . . 50
Aydin Controls . . . 13

Camintonn . . . 111
Chrislin Industries . . . 77
Computer Design & Application . . . 25
Comtal . . . 59
Control Data . . . 19
CSPI . . . 53

Datacube . . . 10
Dataram . . . 26
Data Systems Design . . . C4
Distributed Computer Systems . . . 113

Elector . . . 27
Epson . . . C3

Florida Computer Graphics . . . 37
Ford Aerospace . . . 116

General Dynamics . . . 41
General Electric . . . 49
Genisco . . . 38,39

IC Master . . . 94
Innovative Data Technology . . . 115
Intelligent Systems . . . 15

Keytronic . . . 43

Leading Edge Products . . . C2
Lundy Electronics & Systems . . . 9

Moya . . . 91
MDB Systems . . . 4
Memodyne . . . 20
Micro Peripherals . . . 22
Mini Micro . . . 112
Modgraph . . . 11

NCC . . . 109
Nicolet Zeta . . . 17
Nissei Sangyo America Ltd. . . . 69,71
NSG America . . . 8

Raster Technologies . . . 2,3
Racal Vadic . . . 1

SD Systems . . . 54
Siggraph '83 . . . 73
Sky Computer . . . 95
Standard Data . . . 30

TEAC . . . 16

Universal Semiconductor . . . 6,7

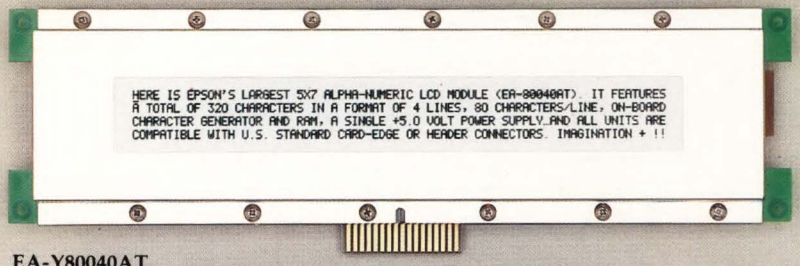
Vectrix . . . 35

LARGE CAPACITY LCD MODULES FROM EPSON...

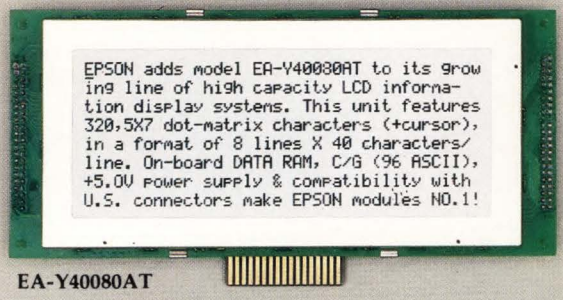
MEETING THE CHALLENGE OF THE MICRO COMPUTER AGE

Epson, the world's leading manufacturer of large-area, alphanumeric liquid crystal information display systems, adds five new formats to its growing product line. Both alphanumeric and graphic formats are available.

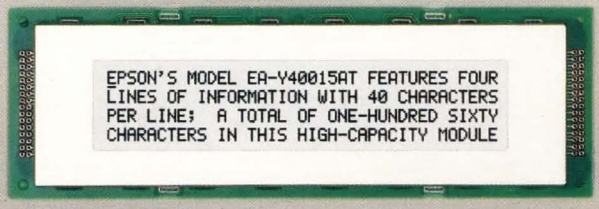
Contact Epson LCD Marketing for information on how these intelligent large-area LCD modules can meet your application requirements.



EA-Y80040AT



EA-Y40080AT



EA-Y40040AT

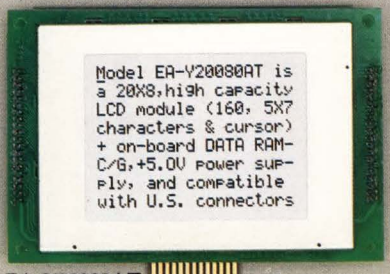
Features

- Compact size and light weight
- Low power consumption
- 5V single power supply
- High contrast and wide viewing angle
- Easy-to-read character size (5×7 dot matrix format)
- Built-in DATA RAM and CHARACTER GENERATOR (96 character ASCII)
- Backlighting possible with EL panel

Applications

- Hand-held Terminals (portable)
- Computer Terminals
- Word Processors/Typewriters
- POS Terminals
- Instrumentation
- Telecommunications
- Games/Toys

EG-Y84320AT



EA-Y20080AT

EA SERIES

Model Number	*Character Format (characters × lines)*	*Character Size (with cursor)*	*Effective Viewing Area*	*Module Size (W × H × D)*
EA-Y16015AZ	16 × 1	2.9 × 4.8 (6.2)	62 × 20	84 × 44 × 14.2
EA-Y16025AZ	16 × 2	2.9 × 4.1 (5.3)	62 × 20	84 × 44 × 14.2
EA-Y20015AZ	20 × 1	3.4 × 5.15 (6.65)	88.2 × 20	125 × 44 × 14.2
EA-Y20025AZ	20 × 2	3.4 × 5.15 (6.65)	88.2 × 20	125 × 44 × 14.2
EA-Y20080AT	20 × 8	3.0 × 4.8 (6.2)	84 × 64	140 × 95 × 19.2
EA-Y24015AZ	24 × 1	2.9 × 4.45 (5.75)	93 × 20	125 × 44 × 14.2
EA-Y40015AT	40 × 1	3.0 × 4.8 (6.2)	156 × 20	192 × 45 × 14.2
EA-Y40025AT	40 × 2	3.0 × 4.8 (6.2)	156 × 20	192 × 45 × 14.2
EA-Y40040AT	40 × 4	3.0 × 4.8 (6.2)	156 × 34	200 × 71 × 25.4
EA-Y40080AT	40 × 8	3.0 × 4.8 (6.2)	157 × 63	205 × 93 × 19.2
EA-Y80015AT	80 × 1	2.1 × 3.38 (4.32)	212 × 18	264 × 53 × 20.7
EA-Y80025AT	80 × 2	2.1 × 3.38 (4.32)	212 × 18	264 × 53 × 20.7
EA-Y80040AT	80 × 4	2.1 × 3.38 (4.32)	212 × 28	293 × 80 × 31.0

EG SERIES

Model Number	*Dot Format (column × row)*	*Dot Size*	*Effective Viewing Area*	*Module Size (W × H × D)*
EG-Y84320AT	84 × 32	0.75 × 0.75	76.3 × 33	132 × 60 × 15.7

Unit: mm

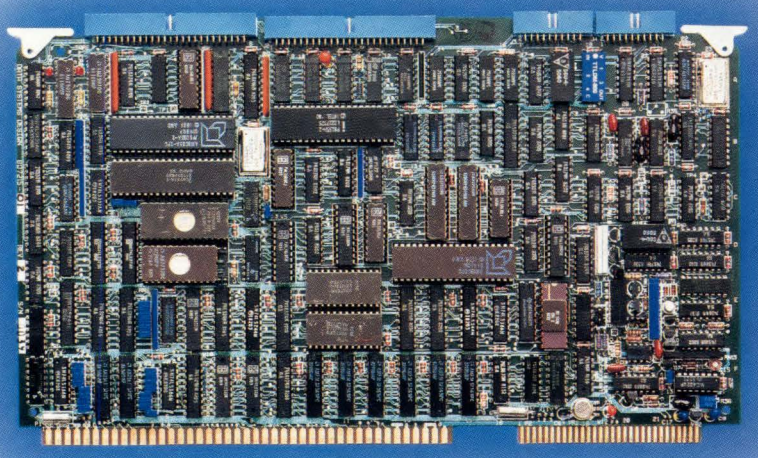
EPSON

EPSON AMERICA, INC.

3415 Kashiwa Street • Torrance, CA 90505
Telephone (213) 534-0360 • TELEX 182412

Write 16 on Reader Inquiry Card

ONE SLOT SHOPPING.



INTRODUCING THE WINCHESTER/FLOPPY/TAPE THREE-IN-ONE MULTIBUS CONTROLLER.

Try this on for size.

DSD's new 7215 single-board Multibus® controller/interface handles two SA1000-type 40Mb Winchesters, a ¼" streamer, and two 8" floppies.

Plus on-board data separation, 32-bit ECC, and self-diagnostics. All on the same board.

There's also a version for 5¼" drives, the 5215, with similar capabilities.

And both are very, very quick.

Thanks to a pipelined architecture that moves data at non-interleaved speeds.

Top-of-the-line performance.

The 7215 and 5215 are the highest performance controllers on the market for 8" and 5¼" drives.

And that makes them ideal for multiuser and UNIX™ applications.

They also emulate Intel®iSBC® 215 and iSBX™ 218 controllers so you can run RMX 86 anytime.

And with 24-bit addressing support, you can take advantage of high performance microprocessors like the 68000 and the new inexpensive memory chips to address larger physical RAM memory.

To tune system performance, both boards offer four alternatives for bus arbitration. As well as having the capability to boost system performance by performing overlapped seeks and multisector operations.

Plus the convenience to match.

The best part about all this performance is that it comes on one board. So it only takes up one backplane slot. And there are no extra boards to fool with.

As easy as that sounds, there are those of you who'd rather not do-it-yourself. For you, the 7215 controller is also available in our 770 storage systems.

And like all DSD products, our Multibus boards and systems are supported by our exclusive Rapid Module Exchange™ and regional service centers.

Shop around.

Compare our incomparable Multibus boards and systems to anything else you like. To make it easy, just send your business card to DSD Corporate Headquarters, Marketing Communications Department, for a free copy of "The Multibus Buyers Guide."

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. **Eastern Region Sales and Service:** Norwood, MA, (617) 769-7620. **Central Region Sales and Service:** Dallas, TX, (214) 980-4884. **Western Region Sales:** Santa Clara, CA, (408) 727-3163. **International Sales:** San Jose, CA, (408) 946-5800.

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DATA SYSTEMS DESIGN

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