



Bruce Bourbon on
System-level design

A PENNWELL PUBLICATION

DECEMBER 1, 1990

COMPUTER DESIGN

*Technology
and Design
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

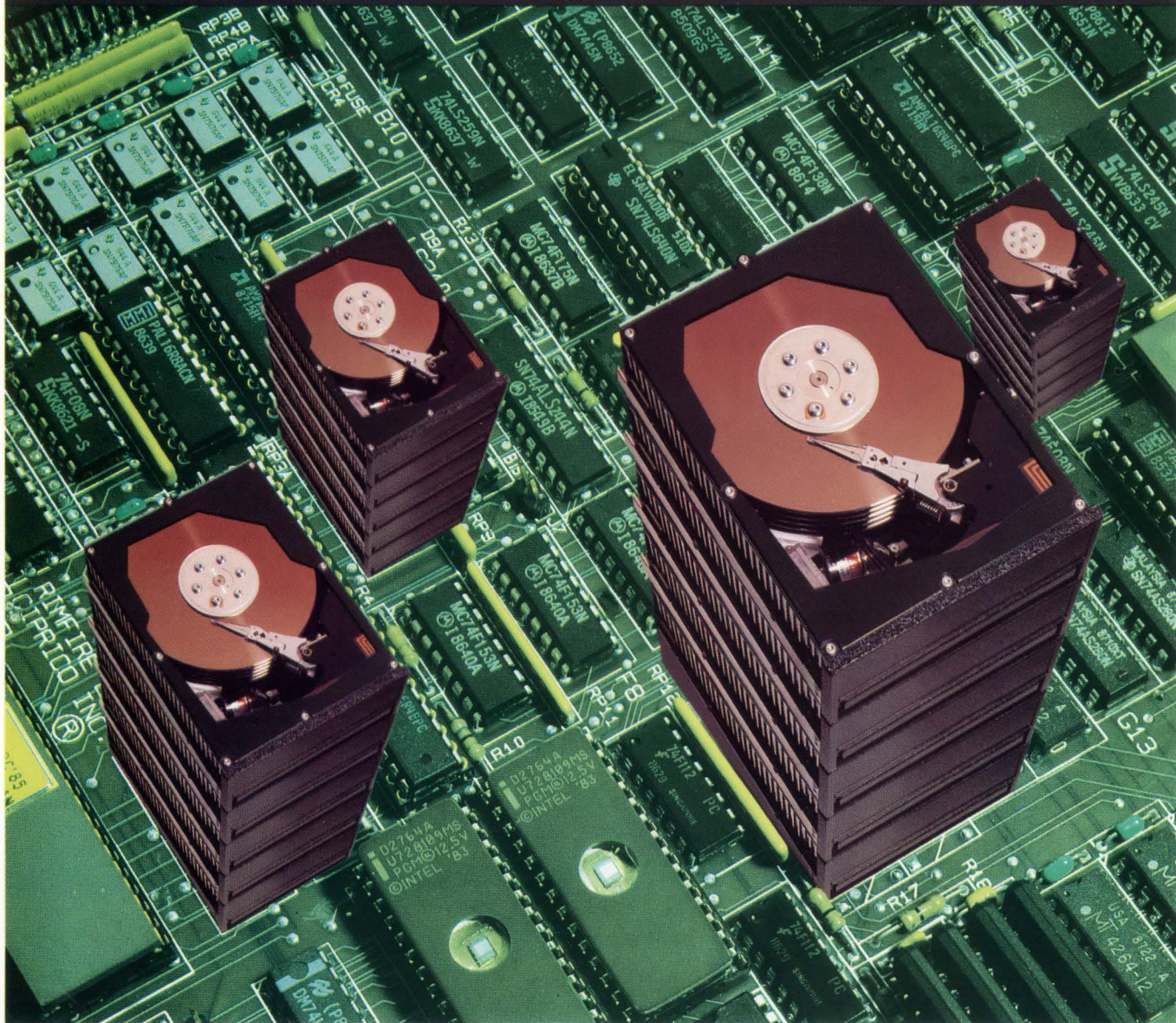
Application determines best approach to multiprocessing

Design entry tools
evolve to meet future needs

DRAM vendors address
increasing specialization



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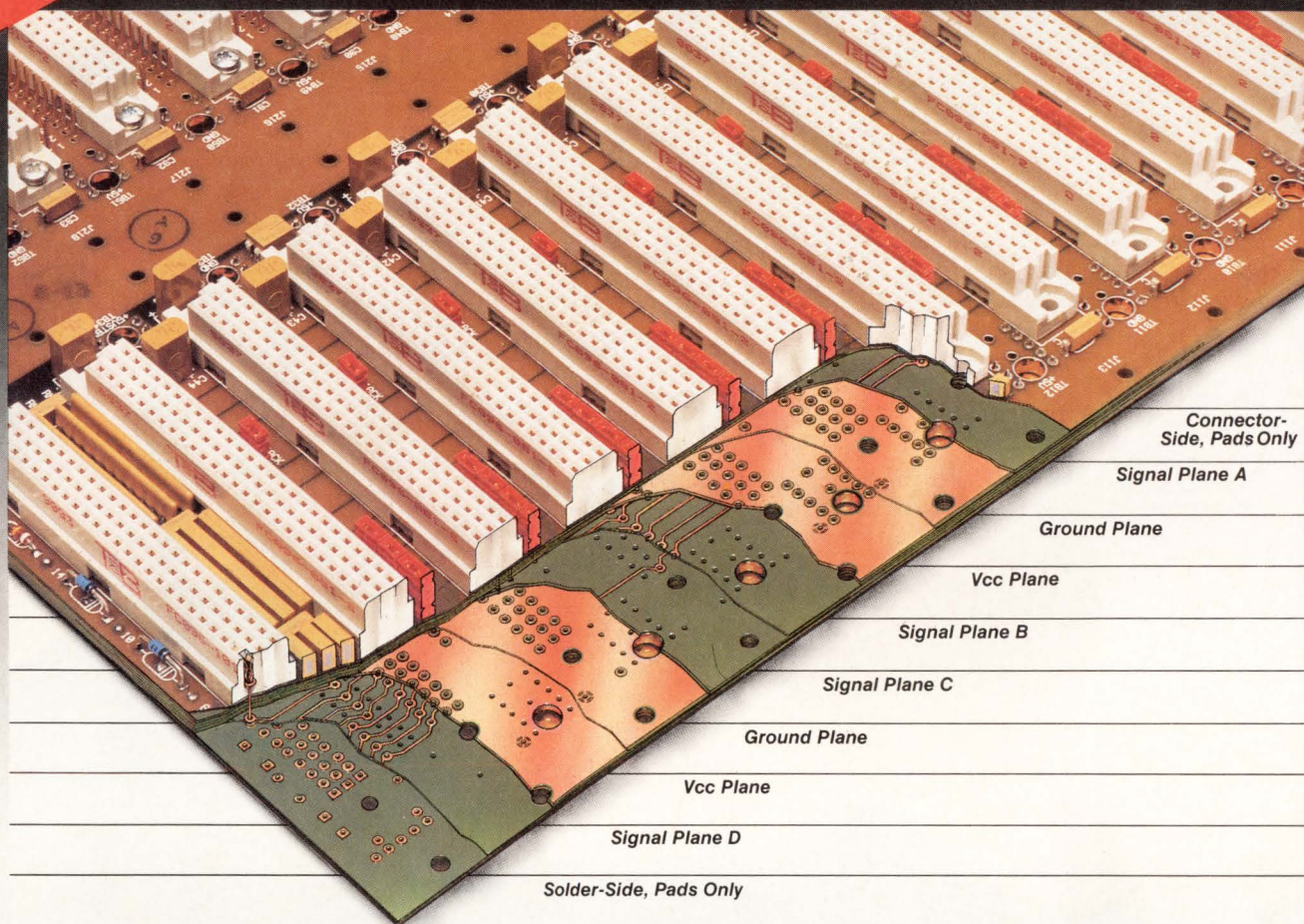
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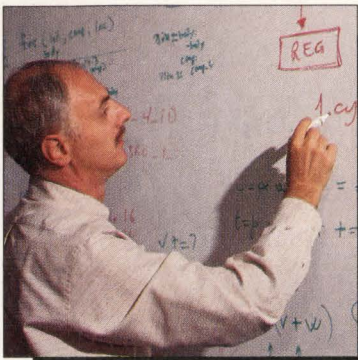


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*Technology
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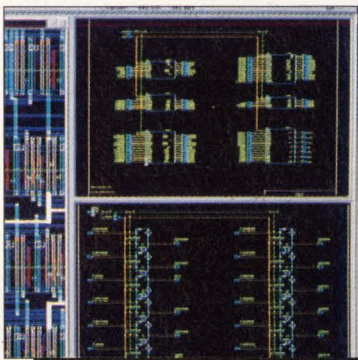
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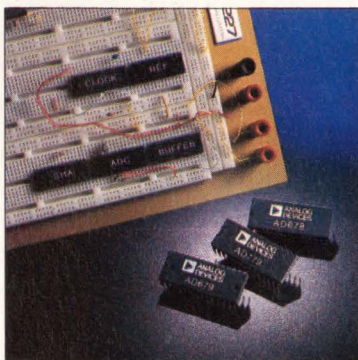
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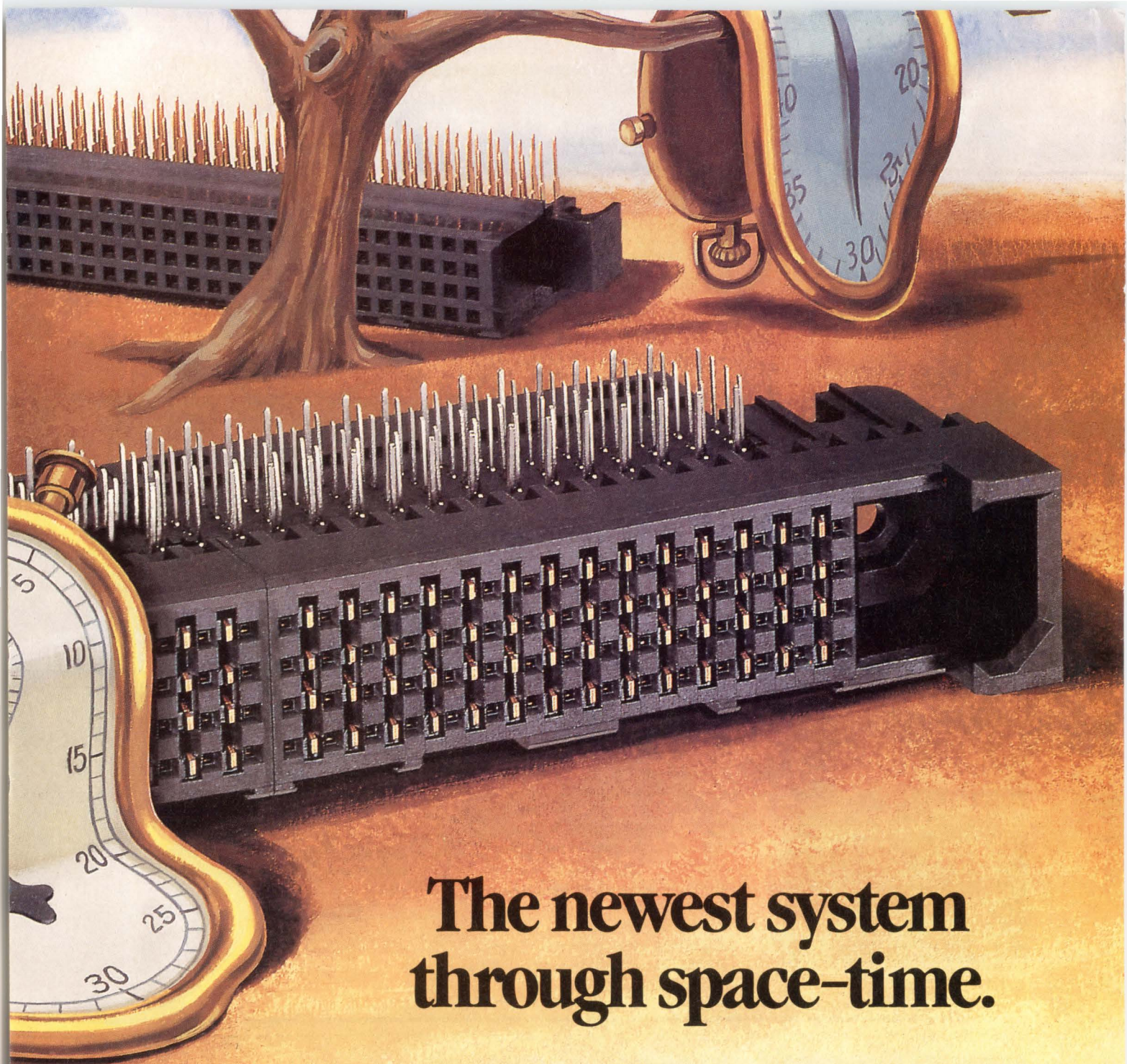
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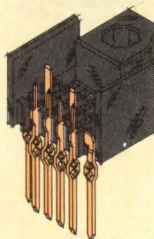
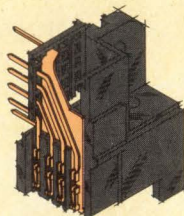
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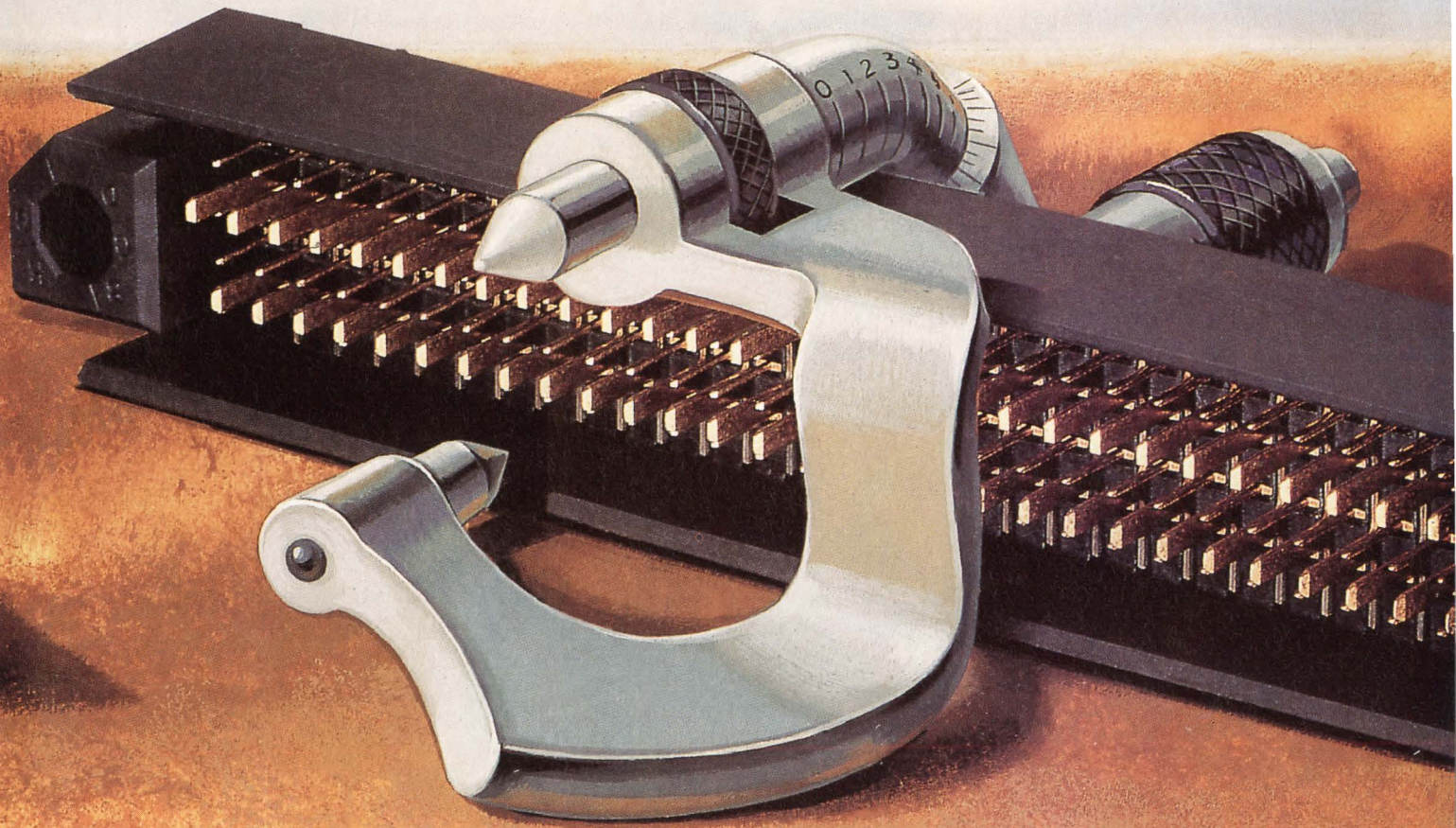
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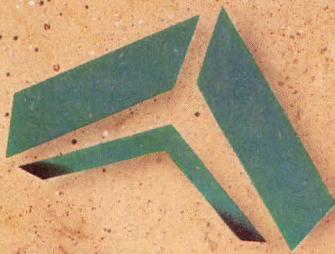
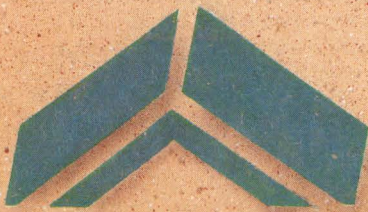
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CIRCLE NO. 5

**TI samples
16-Mbit DRAM**

Texas Instruments (Dallas, TX) has begun sampling its 16-Mbit DRAM to a privileged few customers. TI is the first domestic supplier to sample the parts, joining the exclusive club that previously included only Hitachi, Toshiba and—to the consternation of the Japanese vendors—Korean giant Samsung. NEC is expected to begin sampling by the end of the month as well. TI is reportedly building the parts, which are said to be small enough for mass production, on a 0.6- μ m line in Dallas. The next batch of parts will come from a new facility in Avezano, Italy.

The pattern of announcements on 16-Mbit parts seems to indicate that DRAM design expertise has not become concentrated in Japan after all. The fact that a U.S. vendor, admittedly working with Hitachi on development, is among the first to sample parts, and that Samsung, going solo, has been able to leapfrog into the fledgling market, discredits the notion that one country could corner the market for advanced parts.

The number of entrants in the market at this early date must be keeping some executives awake nights. If price competition develops along national boundaries, erosion could severely harm all the players' efforts to recover their enormous investment in the 16-Mbit technology. —Ron Wilson

**Force and Sun ink deal
in strategy tango**

Under the terms of an agreement being completed between Force Computers (Campbell, CA) and Sun Microsystems (Mountain View, CA), Force will manufacture and market the Sun 1E, 6U VMEbus Sparc-based CPU card. While the move would seemingly end speculation as to what the two companies have been talking about—rumors had it that some Force equity was to be swapped for growth financing—the deal raises other significant questions. Is Sun abandoning the 6U

VMEbus-board business? Will Force drop development efforts on the Motorola 88000 family?

Industry sources voice affirmation to both. Force's Fred Rehausser, vice-president of operations, has been heard grumbling about Motorola's delay in introducing the next-generation parts. In addition, he claims the company has not properly promoted the chip, leaving it to Force (and other board and system vendors) to promote the architecture. Sounds like a variation of the restaurant quip, "The food is terrible, and besides, the portions are too small."

According to the same sources, Force will "have access" to Sun's proprietary ASICs, which are key to the board's performance and compactness. These include Sun's VME interface, its SCSI and Ethernet chips, and other internal drivers. No further terms of the deal—royalty payments, purchase agreements, other 6U Sun boards to be included at a future date, or exclusivity—were disclosed.

The move seems somewhat consistent with Sun's recent directions, which have been verbalized by Scott McNealy, the company's president, in numerous interviews: "We're going to put all our wood behind one arrow." And that arrow seems to be its workstation business. The board business could be interpreted as diluting the company's efforts.

By jumping on the Sparc bandwagon, Force might just be trading one set of problems for another. Sun is obviously going after the leading-edge workstation market, and to retain some significant share it must keep its position as performance leader. To do that, it has to maintain an edge in processor performance and in applications. Sun has already signaled its moves, shifting away from the Fujitsu processor to a next generation of its own design, to which it will have proprietary rights for at least the first iteration. This leaves all the clone makers hoping to compete in a "standards-driven marketplace" high and dry.

—Warren Andrews

**Intel unveils plans
for fastest supercomputer**

Intel (Santa Clara, CA) has announced plans to build a \$10 million, massively parallel behemoth for the California Institute of Technology (Pasadena, CA) that theoretically will have a top speed of 30 GFlops. The supercomputer will contain 512 of Intel's 64-bit RISC i860 microprocessors, which is four times as many as used in Intel's largest supercomputer to date—a 128-processor system built for NASA's Ames Research Center. Plans for the new machine are a result of development efforts at Cal Tech and at the DARPA-funded Touchstone project, aimed at researching massively parallel microprocessor architectures.

—Tom Williams

**IBM sets record
for fastest RISC**

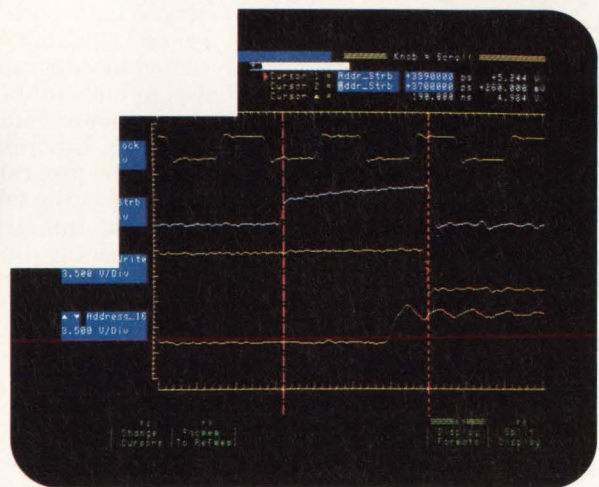
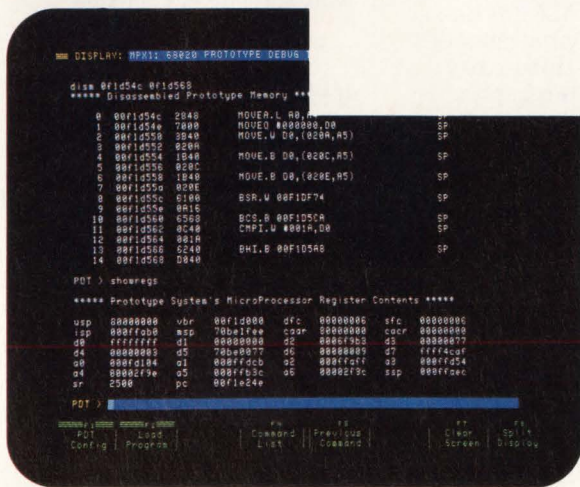
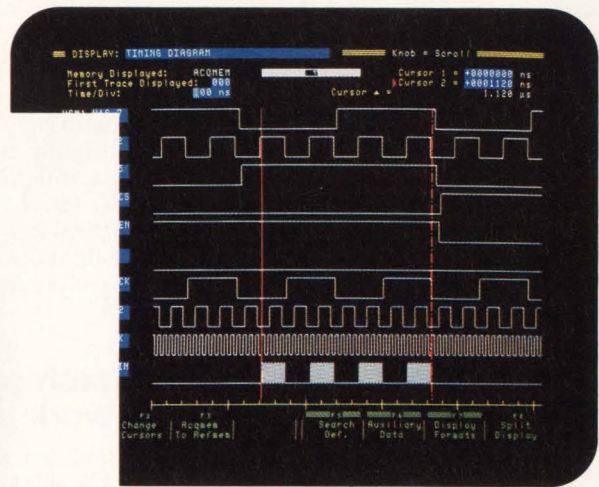
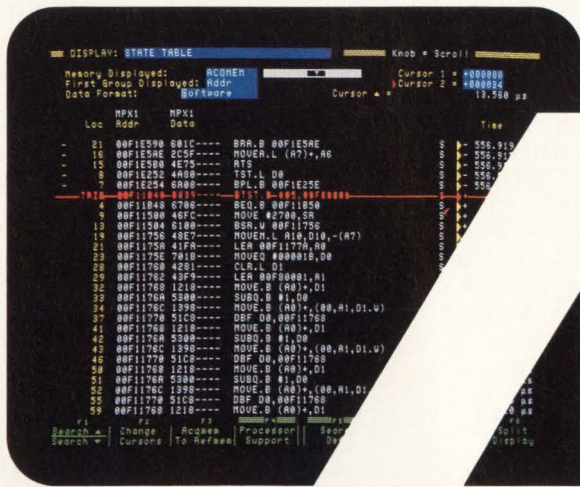
Reaching just over 54 SPECmarks, the latest version of the IBM RISC System/6000 family is the current record holder for RISC workstation performance, edging out even the ECL-based Mips R6000. According to IBM (Armonk, NY), the speed of the new box, the Powerstation/Powerserver 550, comes from new silicon, rather than from architectural changes. The 550 uses new CPU components, fabricated in IBM's latest 0.5- μ m CMOS technology and clocking at 41.6 MHz. This figure makes the multichip CPU faster than any announced single-chip CMOS RISC processor from merchant IC houses.

IBM's ability to achieve this speed and still maintain a good clocks-per-instruction ratio—as indicated by the nominal 56-Mips rating—are a further indication of the scalability of the R6000. The underlying architecture of the workstation is in fact that of the pioneering IBM 801 project, brought up to current thinking.

This architecture, in the hands of IBM, may well overcome a woefully late start to emerge as the machine to beat in high-end workstation applications.

—Ron Wilson

Continued on page 10



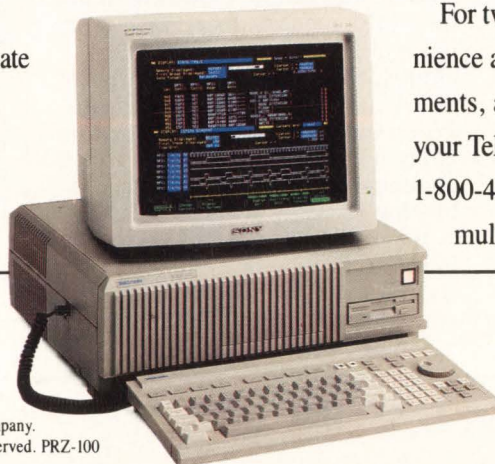
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CIRCLE NO. 6

Continued from page 8

VUGI balks at Futurebus+

Martin Timmerman, chairman of the VMEbus Users Group International (VUGI), appeared a little less enthusiastic about Futurebus+ than one might have expected in a recent editorial in VUGI's regular newsletter.

"Futurebus+ is intended for parallel architecture(s) with RISC processors where cache is intensively used," he says. "These types of architectures are not likely to be used in an industrial market where people are actually screaming after 68000-based boards."

Timmerman continues, "This observation shows us that for industrial applications, VMEbus and the complementary buses such as VSB and VXIbus will still go a long way and will easily reach the year 2000." Yet more, "This is one of the fundamental reasons why our organization will not follow VITA, which stands now for VFEA International Trade Association (VFEA = VMEbus Futurebus+ Extended Architecture), which tries by all means to push as much as possible for the Futurebus+."

— Warren Andrews

LSI Logic marches to its own beat

The individualism and aggressiveness of LSI Logic (Milpitas, CA) is hard to miss in an industry that has too few leaders. One doesn't have to agree with the company's strategy or believe that it will work to acknowledge that it's a gutsy one.

As an ASIC vendor pushing software tools, LSI has been bucking the trend to surrender software concerns to EDA vendors. Its presence among participating software vendors at the fall meeting of the VHDL Users' Group in Oakland, CA made LSI conspicuous as it supported its Silicon 1076 VHDL design environment. Silicon 1076 very aggressively addresses top-down design.

Another area where LSI is taking a lead is in offering its customers a conversion path from FPGAs to gate arrays. In the first quarter of next year, LSI will release a de-

sign tool that will convert an Actel FPGA into an LSI Logic mask-programmable gate array. Though other gate array vendors are talking about doing the same, only Texas Instruments (Dallas, TX) and AT&T (Berkeley Heights, NJ), both of which began shipping FPGAs this month, supply customers with conversion software.

— Barbara Tuck

Intergraph seeks framework partners

In an attempt to grab a larger share of the EDA market, Intergraph (Huntsville, AL) has unveiled InterLink, a program designed to integrate third-party design tools into Intergraph's newly named Simultaneous Engineering Environment framework. The program already encompasses existing OEM relationships, but Intergraph is aggressively seeking alliances with other tool vendors to broaden its base of EDA products—an area in which it's been relatively weak. By labeling and publicizing a framework that it's had for some time, Intergraph is signaling a more competitive stance against rivals Mentor Graphics (Beaverton, OR) and Cadence Design Systems (San Jose, CA), who traditionally tout the benefits of their framework offerings. Though strong in mechanical CAD, Intergraph's market share is small—about 1.5 percent in 1989, according to Dataquest figures.

— Mike Donlin

S Bus the sub choice for Futurebus+

Many companies within the VMEbus community have complained about the large number of sub- or mezzanine buses there are for VME. At last count, with everyone's proprietary approach included, the total was well over 25 totally different mezzanine buses. What with all the standardization going on, there's been some recent clamor for a standard mezzanine bus for VME—but which one?

It's unlikely a resolution will be found in the foreseeable future. But in order to avoid that problem going forward, the VFEA Inter-

national Trade Association (VITA) is looking for some kind of bus to standardize for Futurebus+.

At a recent VITA technical committee meeting, the idea of a standard mezzanine bus was discussed and a straw poll was taken to see which bus was most popular. With only a single dissension and one abstention, S Bus took the ballot. But it's interesting to note that most of the regular VITA members were not present, and of those who were, at least one felt "blackmailed" because he felt an important proposal for VME would be voted down if he didn't "go along with the powers that be."

— Warren Andrews

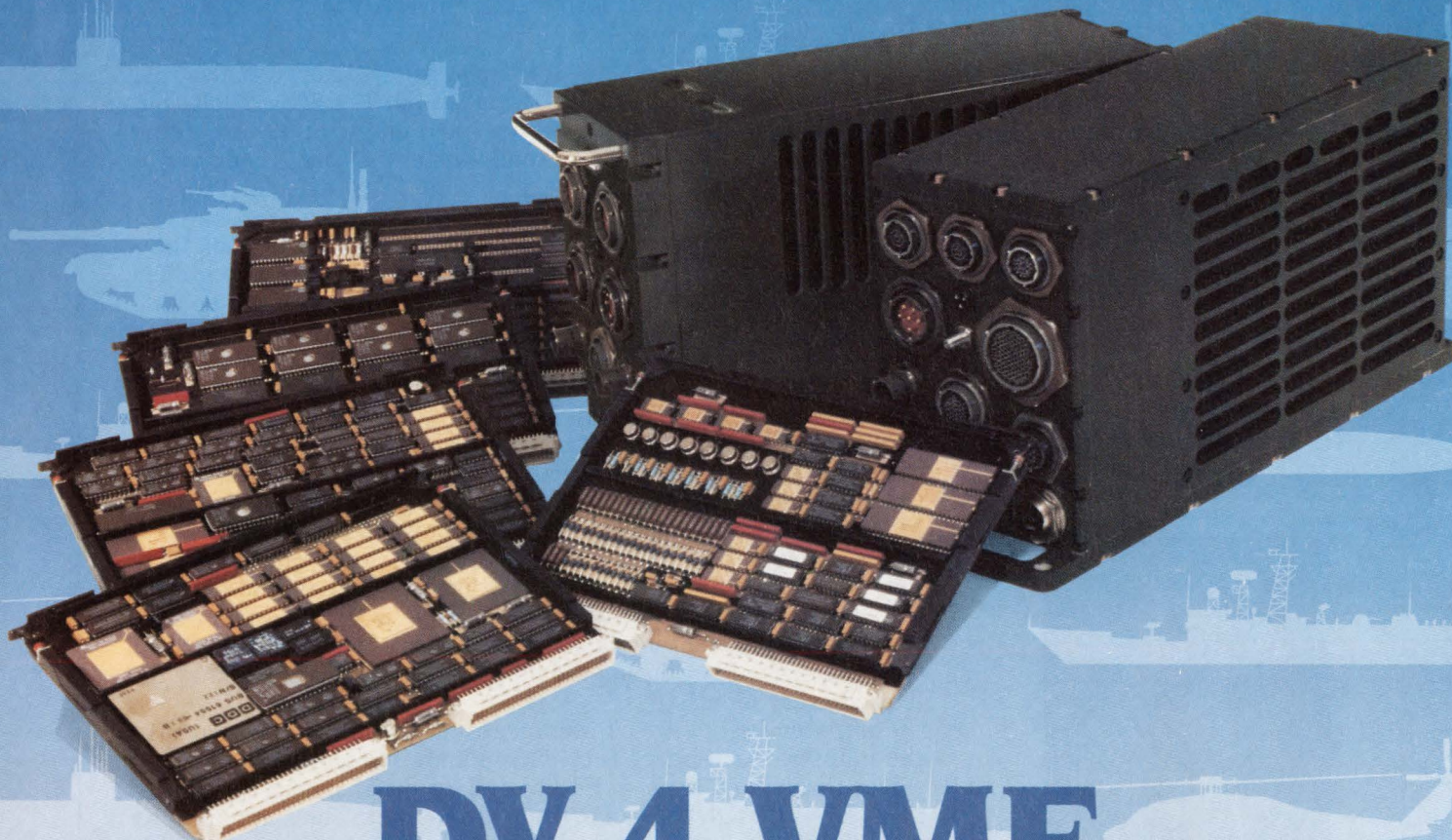
VHDL prepares for 1992 face-lift

As part of a 1992 restandardization phase for VHDL, the VHDL Users' Group (VUG) has issued a request for requirements to VHDL, with February set as the deadline for submitting required changes. The IEEE, which adopted VHDL 1076 in 1987, rules that every standard it backs must come up for reballoting at least once every five years.

Prioritizing requirement requests submitted by VUG members is a measured process. First, a priority ranking is assigned to each requirement by a VUG area leader after negotiating with the company from which the requirement originates. As the requirement is passed on, the battle over priorities continues. The last say on changes resides with the subcommittee—ultimately responsible for the design of the language.

It's hoped that identifying fixes and enhancements to the language will smooth out ambiguities and inconsistencies in VHDL. Beyond that, major areas of support will be considered. Probably the most significant area to be reviewed will be analog support—how to extend VHDL, which thinks in terms of events, to support time-domain analog. At this point, it's expected that the 1992 VHDL version is more likely to support a subset of analog than it is to support full analog.

— Barbara Tuck



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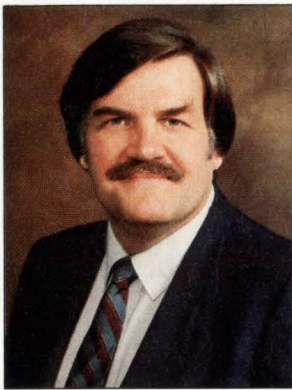
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I can never seem to get my decades straight. Everyone else celebrated the end of the '80s last December, but I've always felt you should start counting a decade with 1 and end with 10. According to this logic, December 1990 is really the end of the decade and January is the beginning of the next—and last—decade of the century.

Regardless of how you count the decades, the last 10 years have been turbulent ones for the electronics/computer industry and for the publications, like *Computer Design*, that serve its engineers and managers. First, we had the boom years of the early '80s, when the industry was virtually exploding with activity and the trade publications were keeping pace. But hard times hit the industry in late 1984 and early 1985, and nearly every publication serving the industry felt the reverberations.

As readers, you felt the shock waves because hard times in the industry meant cutbacks in advertising pages, which, in turn, brought about changes in editorial and cutbacks in editorial pages. Some publications, trying hard to hold onto their advertising base, subjected themselves to editorial gyrations that abandoned, neglected or confused readers. Some were so hard hit that they ultimately went out of business, while a few others weathered the storm by reducing the number of editorial pages they delivered every month.

Computer Design wasn't immune from the hard times that hit the industry. As readers, though, you know we didn't put ourselves through editorial gyrations and we didn't go out of business. Even though we couldn't provide you with the same number of editorial pages per month that we did in the boom years of the '80s, we stuck to our guns when it came to providing quality editorial on technology and design directions in ICs, ASICs, buses and board-level subsystems, software, CAE/CAD and development tools.

That dedication paid off for us this year as *Computer Design* ended the decade with a dramatic increase in advertising pages while its competitors showed dramatic decreases.

What that means to you is that we've been able to increase the editorial pages we deliver, increase our circulation so that we reach more of you, and add to our editorial staff. With the recent addition of senior editor Barbara Tuck to cover ASICs and the promotion of Mike Donlin to senior editor responsible for CAE/CAD and development tools, for example, we've been able to carry through on the promise made earlier this year: to fill the void left by the demise of publications that you may have read.

Yes, the last few years of the past decade have been rough, but we stood up through it all and we're stronger now than we've ever been. You'll really start seeing this strength next year, in the first year of the new decade.

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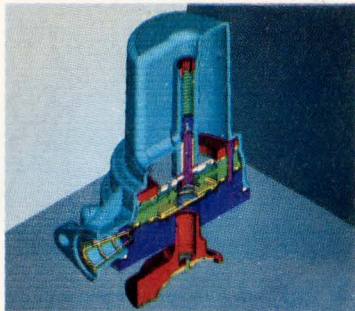
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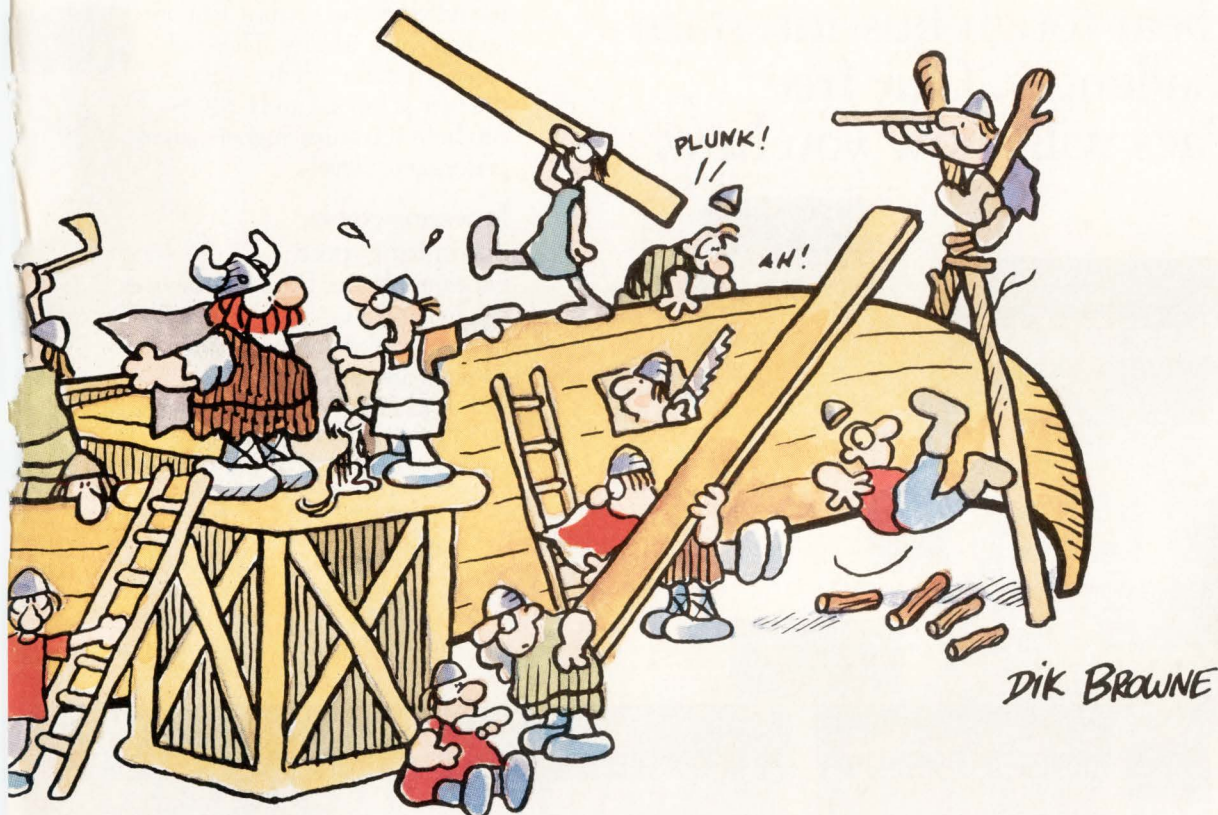
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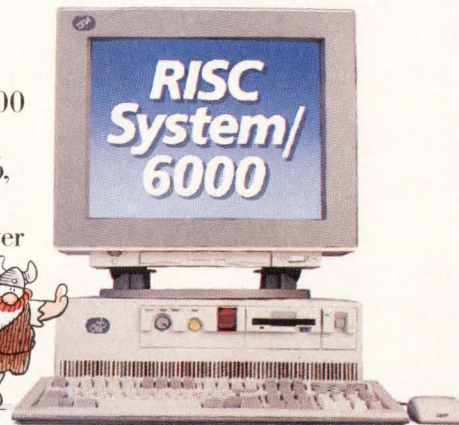


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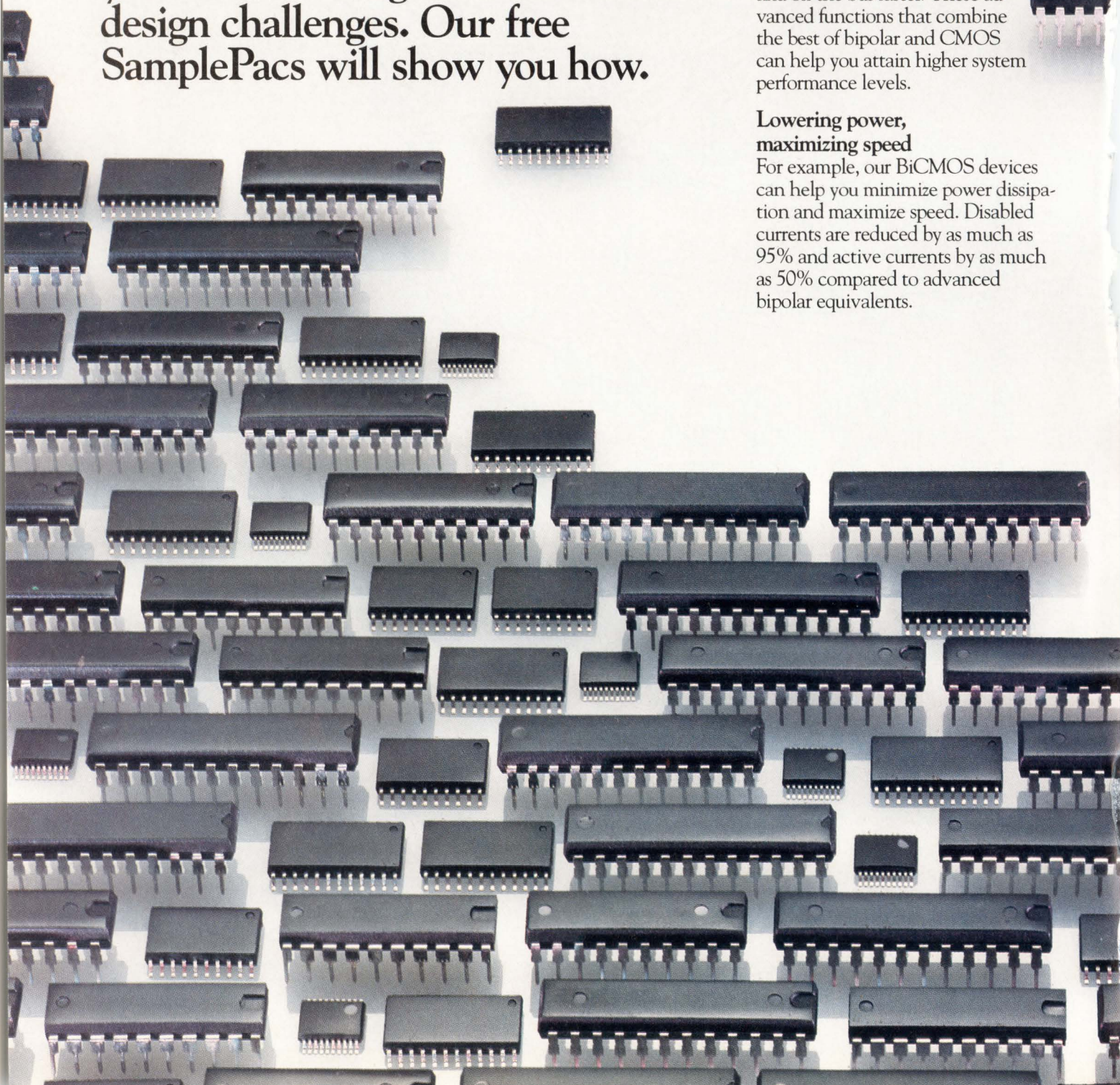
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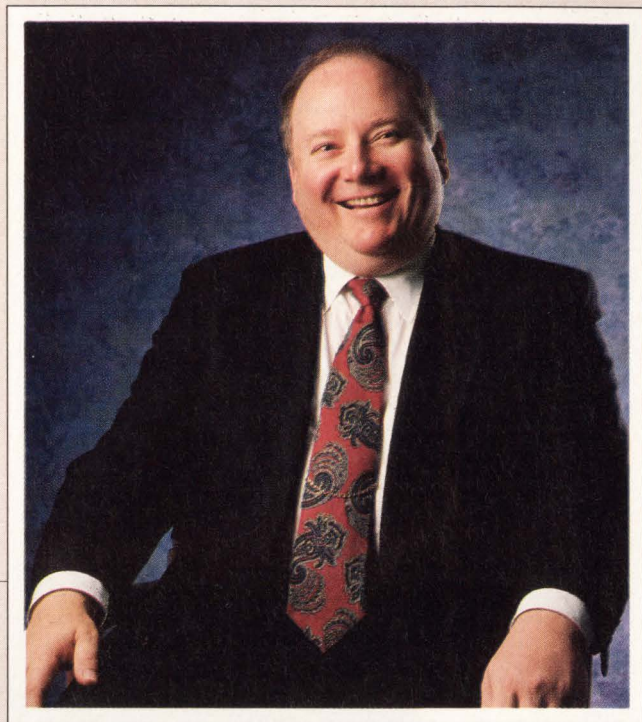
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Bruce Bourbon on: System-level design



Fifty percent of ASIC designs don't work once implemented in the system. This bit of ASIC folklore has become the marketing cry of ASIC vendors who claim to solve the problem with their design methodologies and EDA software tools. The long version of the problem statement, though, runs as follows: "Fifty percent of ASIC prototypes don't work in the system environment because of chip specification errors, chip interaction problems or electrical effects related to board implementation." What the ASIC industry needs is a reliable design methodology to implement multichip ASIC solutions that work the first time.

But what is system-level ASIC design and what is the ideal design methodology for minimizing the risk that the ASIC chip set won't function as expected? And how can we design ASIC chip sets containing hundreds of thousands of gates quickly enough to exploit market windows that open and close every 18 months?

First, a definition. "System-level ASIC design" is an expression of complexity level. Specifically, it's a complexity level where the implementation of a solution to the design problem will require many ASIC devices. System-level ASIC design demands the use of a top-down design style, where design intent is captured in a hardware description language (HDL), using both behavioral and high-level structural models. System-level ASIC design is also that level of complexity where the use of design-for-testability strategies becomes mandatory.

The answer to the system-level ASIC design challenge lies in greatly improved design methods and tools. The lack of adequate EDA software is the major barrier to the exploitation of the level of integration possible in today's most advanced fabrication processes. Silicon is considered free; it's the design effort that's expensive, both in terms of development cost and in terms of time. And let's not forget design risk. Design engineers tend to select a design implementation strategy that they think will minimize the risk that the first prototypes won't work.

Look at the two-edged sword the design engineer must skillfully wield. Design complexity has grown

by two orders of magnitude in the last 10 years. Meanwhile, system life cycles have declined from five years to 18 months. Exploiting the available integration density is critical to the success of a system product, but there's no room for error. The system product better work the first time. And it must be testable.

The ideal EDA system for system-level ASIC design reduces design risk to a tolerable level while permitting the use of all the integration density allowed by the fabrication process. This ideal software system must also let the designer wring the last possible picosecond of performance out of the fabrication process. In the competitive world, performance still rules.

The ideal design philosophy must also embrace a fully synchronous design style, so that the timing behavior of the logic design is totally deterministic, verifiable and unambiguous. A design strategy of risk minimization leaves no room for asynchronous timing approaches that appear clever when implemented yet wreak havoc in the real world of silicon, voltage and temperature variations.

A multichip ASIC design automation system must employ the following elements:

- HDL support to capture design intent at a high level of abstraction;
- System- and chip-level design verification through the use of functional simulation or proof-of-equivalence methods, coupled with exhaustive static timing analysis;
- Interactive design partitioning software to help the system engineer partition a large design into the optimal set of ASIC devices;
- Logic synthesis technology to optimize the design at the logical and physical design steps;
- Pervasive use of DFT methods to make chip and board testing practical;
- Chip-level physical design methods to optimize

the performance of each chip design.

Each of these six fundamental techniques contributes to the handling of design complexity and the reduction of design risk in multichip ASIC projects.

■ Capturing design intent

It's surprising how many of today's complex ASIC designs are still captured in gate-level structural form. At a complexity level of a few tens of thousands of gates, a validated gate-level structural netlist is still possible to create, although the designer who does so won't willingly do so a second time. At 50,000 gate equivalents and above, the only practical approach is a top-down design style where design intent is captured in an HDL using behavioral or high-level structural models.

The de facto HDL in today's ASIC design community is Verilog HDL from Cadence Design Systems, while U.S. government support is behind VHDL, now shepherded by an IEEE standards committee. In Japan, there's a coalition of electronics companies sponsoring the development of yet another HDL—UDL/I. It's inevitable that there will be many HDLs in use, so the ideal design automation system must support all the popular ones.

Third-party companies will build businesses around providing HDL behavioral models for ASIC "megacells," such as RISC processors. ASIC design groups will invest in the development of proprietary behavioral and high-level structural models of functional blocks that they repeatedly use to implement ASIC solutions for their types of design applications. Once developed in the favored HDLs, these models will create tremendous inertia to change, inhibiting moves to other HDLs.

■ System-level design verification

Once the design intent is captured in HDL form, the next step is to simulate the design to verify functionality. This simulation typically requires a mixed-level approach (combining both behavioral and structural simulation), given that a systems-level design probably contains HDL fragments at various levels of abstraction. This simulation deals only with the functional correctness of the design, not with its timing behavior.

With the design functionality verified, those portions of the design that are described in behavioral or high-level structural form must be transformed to that level of structure for which timing behavior can be accurately assessed. In most cases, the structural form will be a gate-level representation. This transformation or synthesis process must map behavior to structure in a way that's independent of the final implementation technology (such as CMOS or ECL). Until an unconstrained behavior-to-structure synthesis capability emerges—and don't hold your breath—the synthesis process will predominantly be from a high-level to a gate-structure transformation.

At this point in the design process, system-level static timing analysis must be performed on the entire structural design. With this complexity level, tradi-

tional timing simulation is simply inadequate. It takes too long and only those paths exercised by the applied functional vectors are verified. The only practical way to verify timing behavior comprehensively is through the use of static timing analysis, separating timing verification from functional verification. Timing analysis exhaustively analyzes all circuit paths using complex timing models to ensure that the resulting path delay calculations are accurate.

At this juncture we have a system-level ASIC description that has been verified to perform as functionally expected, meeting all the timing constraints placed on the design. If, however, the system design is to be implemented in several ASICs, design partitioning must be accomplished before timing validation can be declared complete.

■ Interactive design partitioning

Intelligent partitioning of system-level design descriptions into multiple ASIC devices is truly on the forefront of EDA technology. Vertex Semiconductor has been working on partitioning technology for more than six years and considers its current tools to be at the level of a bright five-year-old.

The number of constraints placed on the partitioning process is very large, so an interactive approach to the task is best. Interactive partitioning with graphical feedback marries the power of the computer to the designer's ability to perform trade-off analyses quickly. The computer is charged with keeping track of the design structure and supporting a graph-

ical method for assigning circuitry to partition buck-ets and boxes.

Some of the issues to be considered in partitioning include logic functional boundaries; package-related I/O pin limitations; package physical constraints, such as die cavity size limits; testability issues; I/O pin restrictions due to simultaneous switching limitations; selection of I/O drivers based on the target interconnect technology; and printed circuit board or multichip module (MCM) thermal considerations.

Once partitioning has been completed, it's time to turn to the design of each ASIC in the chip set.

■ Logic synthesis and optimization

After partitioning the overall system design into multiple ASIC designs, the functionality of each chip is usually verified by functional simulation. A preferable alternative to this traditional method is to use proof-of-equivalency software (also known as Boolean verification) to verify that the partitioned design is functionally identical to the system-level representation. Once functional correctness has been reverified, the logic optimization process can begin.

The chip logic must be transformed to find the optimum trade-off between operating speed and gate count, while mapping the logic to a target library. This is the typical methodology of today's logic synthesis tools. In addition, if a gate array implementation is to be used, specialized transformations must be executed to maximize gate utilization and minimize physical wirability problems.

*Exploiting the available
integration density is critical
to the success of
a system product.*



Since each chip represents a section of a system-level design, the next step is to modify the chip description by adding the necessary I/O cells. In doing this, chip-to-chip drive requirements must be considered, the effect of I/O delays on critical paths must be calculated, and clock signals and power must be distributed to the chip.

■ DFT an imperative

Because of the complexity level of a system-level ASIC design, DFT isn't an option—it's an imperative. A strategy for testing each chip must be implemented and a means for testing the chip set on a board or MCM must be devised.

In the Vertex design methodology, the DFT approach is a scan-testing method, augmented with built-in self-test (BIST) for any memory cells embedded in the design. Internal scan rings are created to permit convenient testing of the chip and a boundary scan ring is added to simplify wafer and board testing.

At this stage in the design process, the test logic must be automatically synthesized or inserted in the design description. Because the designer may damage the design by modifying it after test logic insertion is completed, a logical design-rule check must be performed to ensure the design conforms to all scan-testing rules.

Because of the major logic transformations and additions done during the logic synthesis and test logic insertion steps, as well as the possibility of manual tuning, it's necessary at this point to reverify that the logic function hasn't been changed.

Before committing to the physical design of each chip, exhaustive static timing analysis must again be done with timing models that account for the estimated effects of interconnect delays.

■ Physical design

Chip-level physical design is the process of placing functional cells and then automatically interconnecting them in conformance with a validated netlist. The first step is floorplanning or global placement, which assigns all the cells in the design to physical locations in a 2-D view of the chip layout.

Global placement is followed by scan-chain reordering to minimize wiring congestion when the scan chains are interconnected. Static timing analysis is then performed for a third time, using manhattan wiring (points connected using right-angle segments) length assumptions based on the global placement. A clock grid is then automatically generated and physical synthesis and optimization is employed to minimize wiring delays and clock skew across the chip.

The next step is interconnect routing, where nets are assigned to channels in the design and detailed interconnect routing is completed. Then static timing analysis is done one last time, using extracted interconnect parasitic information to reflect actual delays.

Finally, test vectors are automatically generated by test-pattern-generation software that's compatible with the DFT strategy used in the system design. The test vectors are then used as input to a final functional simulation to verify correct operation of the test logic.

It's clear by now that a reliable system-level ASIC design methodology isn't simple. While it has been described as if it were a well-honed, mature and highly

automated process, it's now time to face the realities of the methodology by exposing the myths.

■ Exposing the myths

The first big myth is the state of behavioral synthesis technology. In their desire to land new customers, EDA vendors who market synthesis software products tend to talk glibly about behavioral synthesis. Let's be precise. Until circuit behavior can be abstractly described in an HDL without a hint of structure and then automatically transformed to a desired structural form, behavioral synthesis hasn't been realized.

There are at least two fundamental problems with true behavioral synthesis. First, the range of architectural choices is enormous. Some assumptions about the target architecture are necessary to make behavioral synthesis tractable. Second, a true behavioral description serves to hide many gate-level structures because they're irrelevant at the behavioral level of abstraction.

Myth number two is the concept of automatic design partitioning. Partitioning is still an art. At the present state of development for partitioning software, we are able to provide aids to the partitioning process. The designer is relieved of the drudgery of manipulating large design descriptions by an interactive graphical interface to the partitioning software. The designer is still involved, however, and responsible for making the trade-offs that will ensure the best set of partitions.

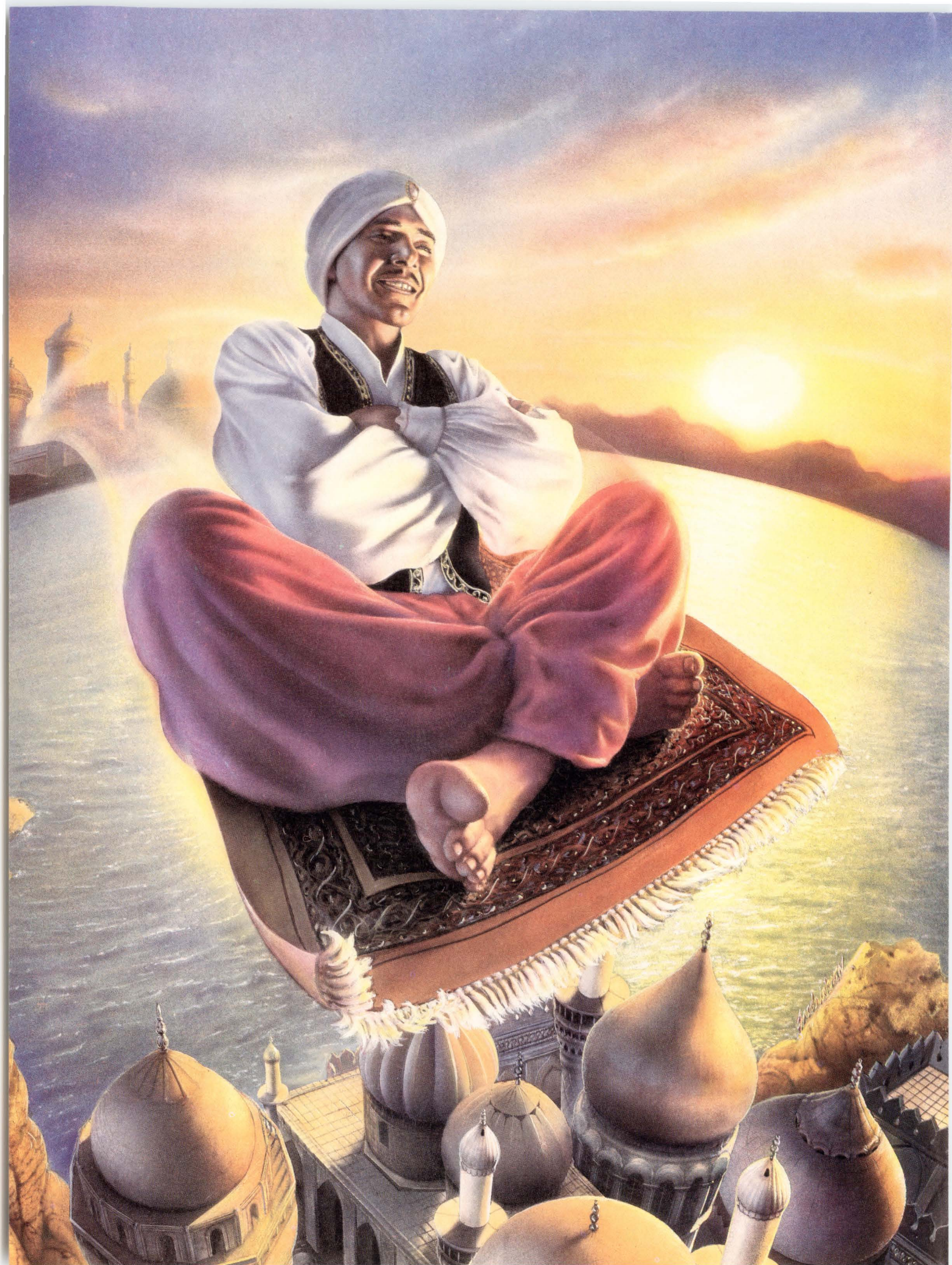
Then there's the myth of multicycle paths in timing analysis. Static timing analysis is predicated on use of a synchronous design style with a derated clock period used to validate timing conformance for every path in the design. This is fine in theory, but what about paths that are deliberately designed to be multicycle paths? While these are now handled on an exception basis, a more automatic means of handling multicycle paths is needed.

Myth number four concerns timing-driven placement and routing. In the physical design realm, the methodology described above uses static timing analysis to guarantee that the design still meets the timing constraints after global placement and final routing. The availability of timing-driven placement and routing would eliminate these timing analysis steps, simplifying the physical design effort.

But before timing-driven placement and routing can be considered a reality, the software must be able to consider the totality of the timing problem in an efficient manner. Current techniques using net prioritization and path delay specification don't adequately achieve the goals of timing-driven layout. The real solution requires the merger of the block placement step with logic optimization methods.

The lack of adequate EDA tools is preventing the exploitation of the level of integration possible with today's advanced ASIC fabrication processes. Only with significant improvements in design methods can the two-edged sword of increasing complexity and ever-shortening life cycles be handled skillfully by the ASIC industry.

Bruce R. Bourbon is president and CEO of Vertex Semiconductor (San Jose, CA).



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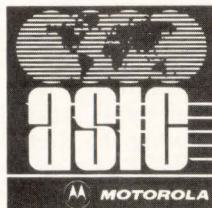
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INTEGRATED CIRCUITS

New chips whittle away at networking costs

Ron Wilson, Senior Editor

At the heart of the success of LANs is the plummeting cost of networking hardware. Here, as usual, silicon vendors are at the leading edge, using the twin tools of high integration and sophisticated data encoding to whittle away at the interface and media costs for a network connection. Recent weeks have seen advances all across the LAN performance spectrum, from 10-Mbit/s 10Base-T to the 100-Mbit/s FDDI (Fiber Distributed Data Interface).

At the low end, the news is in repeater silicon. The 10Base-T network uses twisted-pair wiring in a star configuration to provide a physical layer for Ethernet service. That makes for big savings in wiring, but it means that each small cluster of a few to a few dozen nodes must have a hub—a set of repeaters with control and network management circuitry.

None of these items represents a staggering technical challenge, but the cost of a hub adds up when it's implemented with discrete components, according to Anders Swahn, marketing manager at Advanced Micro Devices (Sunnyvale, CA). "Today, even with the simplest components, a hub will cost you about \$100 per port," he says. That price keeps 10Base-T from competing directly against cheaper low-performance networks such as Appletalk.

■ Cutting into hub prices

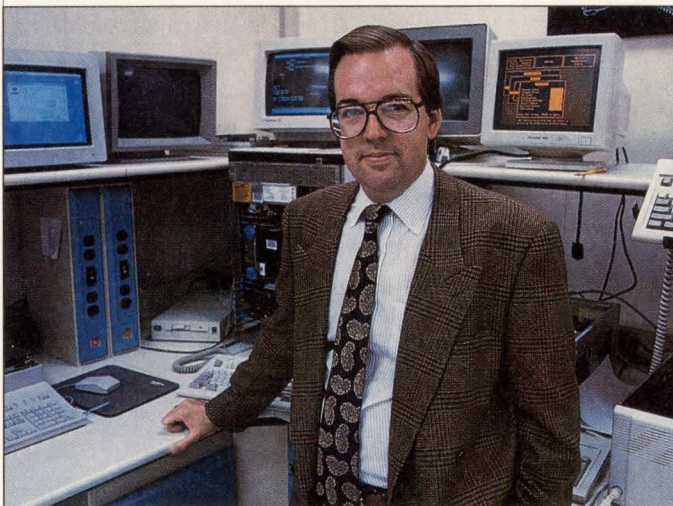
Springing to the rescue, AMD has integrated its proven 79C98 TPEX twisted-pair transceiver technology with hub control logic to produce a single-chip hub product: the 79C980 Integrated Multiport Repeater (IMR). The part combines eight standard transceivers, one attachment unit interface dedicated transceiver, repeater and timing logic, an external port for connection to a network management processor and a cascading port. Jointly developed with Hewlett-Packard, the CMOS part comes in an 84-pin PLCC.

Swahn expects the device to cut

deeply into hub prices. "Current second-generation solutions use gate arrays to implement the repeater and end up taking 12 to 15 chips," he claims. "We believe the IMR will bring hub prices down to about \$30 per port at once, and with further development we have the opportunity to cut that in half again. That

loop," says Fujitsu director of product marketing Alex Goldberger. "It's mainly done in standard-cell technology, but with one corner dedicated to fast analog circuitry."

Since the Nice chip combines Ethernet hardware with a buffer manager and an endec, all that's left for the interface designer to provide is buffer memory, a media access unit and bus interface glue. Fujitsu has simplified this problem too, by gathering up the glue for a personal computer bus into a gate array, sold as the MB86953. The part by itself provides an 8-bit connection to the



Steve Bell, LAN group manager at National Semiconductor, has seen the industry become enthusiastic about 100-Mbit/s twisted-pair LANs. He believes that innovation in signaling and control of crosstalk are keys to continued improvement in our ability to use inexpensive LAN media.

will make possible the 'velcro' hub: an inexpensive box that you can just stick to the wall of your cubicle to serve a small group of users."

While AMD is working on the hub cost, Fujitsu's Advanced Products Division (San Jose, CA)—the creator of the Etherstar LAN chip—has been busy integrating at the node end of the wire. The company has just released a pair of products that make up a virtually turnkey three-chip logic solution to an Ethernet interface, whether for twisted pair or coaxial.

The big news is essentially a combination of the Etherstar controller and a Manchester endec (encoder/decoder) onto a single piece of silicon. The MB86960 Nice (Network Integrated Controller with an endec) chip is yet more proof that designers are solving the riddles of fast analog and fast digital on a single substrate. "The chip has one analog and one digital phase-locked

ISA bus, and with a couple of additional packages, it can do a 16-bit interface.

■ FDDI on twisted pair

There are always some power users for whom 10-Mbit/s LANs won't do the job at any price. These users look to the rising star of FDDI. But many site managers have flatly refused to pull fiber for an individual desktop, reserving the optical network for corporate backbone applications.

In response, there has been a good deal of theoretical work on running full-bore 100-Mbit/s FDDI on copper—specifically, on shielded twisted pairs. It actually takes a minimum of two pairs to connect a node, since FDDI's token-ring topology has at least one input and one output line to each node. But two shielded twisted pairs still represents a significant cost savings—and less emotional trauma—than a fiber and its associated transceivers.



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"Two or three years from now, the site manager will be able to economically put a user directly on the corporate backbone just by putting a shielded-twisted-pair port in his concentrator," predicts Steve Bell, manager of the LAN Business

Development Group at National Semiconductor (Santa Clara, CA). This promise is a step closer to reality since National, in conjunction with networking specialists Cabletron Systems, has announced plans to produce shielded-twisted-

pair interface chips for National's FDDI chip set.

Bell claims that the technical issues with 100 Mbits/s on copper are well understood. "We're just introducing some new signaling techniques," he says. "It's a matter of making the right trade-offs, and of having access to some powerful simulation tools." National isn't leaving much room for surprises—in six to eight months the company plans to have an interim device that will go between the passive hardware and National's existing Player physical-layer chip.

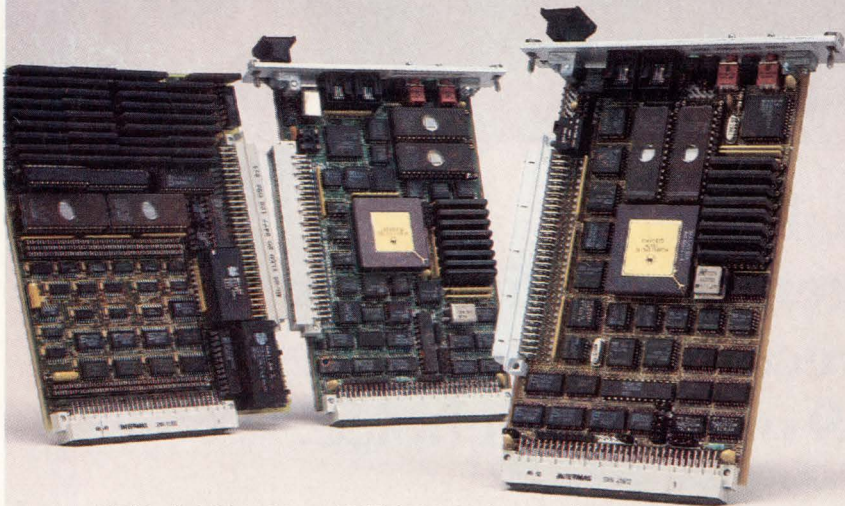
As a follow-on, National plans an expanded Player chip that will include the twisted-pair support. "That part will make the design job tremendously easier for board developers," Bell says. "With discrete parts, you have to do a 100-MHz-strip line design between the controller and the connector. With the new Player chip, all of that technology will be inside the silicon."

Such hardware will increase the importance of twisted pair tremendously. It will be possible to provide Ethernet-level networking on a simple, unshielded twisted pair to virtually any location that can have a telephone. With copper FDDI, shielded twisted pair can deliver staggering bandwidth to desktop stations. And there's already investigation of yet another possibility. Theoretically, there should be enough bandwidth in an unshielded twisted pair to do FDDI, if everything works right.

No one claims to know how to do that job yet, but as Bell observes, "A few years ago you couldn't do Ethernet on an unshielded twisted pair. Then someone said 'What if we try it like this?' The only firm prediction I can make is that the company with a solid understanding of shielded-twisted-pair technology will have a head start for unshielded." ■

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INTEGRATED CIRCUITS

As RISC wars escalate, simplicity seems to be first casualty

Ron Wilson, Senior Editor

The original concept of reduced-instruction-set computing had the beauty of simplicity. If you simplified the instruction set of a CPU to an absolute minimum, you could implement the processor in very simple hardware. Such simple hardware would be inherently fast, and could easily be re-implemented on the latest processes to always be a step ahead of the CISC chips in speed.

But in the street fight that has developed among RISC vendors, simplicity seems to be the first civilian casualty. The latest announcements of future products from Sparc originator Fujitsu (San Jose, CA) and go-it-alone Motorola (Austin, TX) indicate a new trend. RISC chips are getting faster and more competitive by—you guessed it—getting more complex.

The complexity is coming in three areas: instruction set, peripheral environment and execution units. All of the changes are responses to the needs of either the workstation/server market, where the demand for Mips has outrun any possible process improvement curve, or the needs of the embedded environment, where many of RISC's principles were not quite right to begin with.

The exploding core

It has become obvious that just making the clock of a RISC CPU run faster isn't enough to keep up with our unceasing demands for Mips. In the struggle to wring more Mips out of a given clock frequency, most RISC vendors are looking at some version of the superscalar concept. Intel started the ball rolling with a superscalar version of the 80960 processor. Fujitsu developed, then abandoned, the superscalar Sparc-H. Cypress Semiconductor and Texas Instruments are both said to be working on Sparc processors using the concept. And now Motorola, in mapping out its strategy for the 88000 architecture, is showing a superscalar approach

as well.

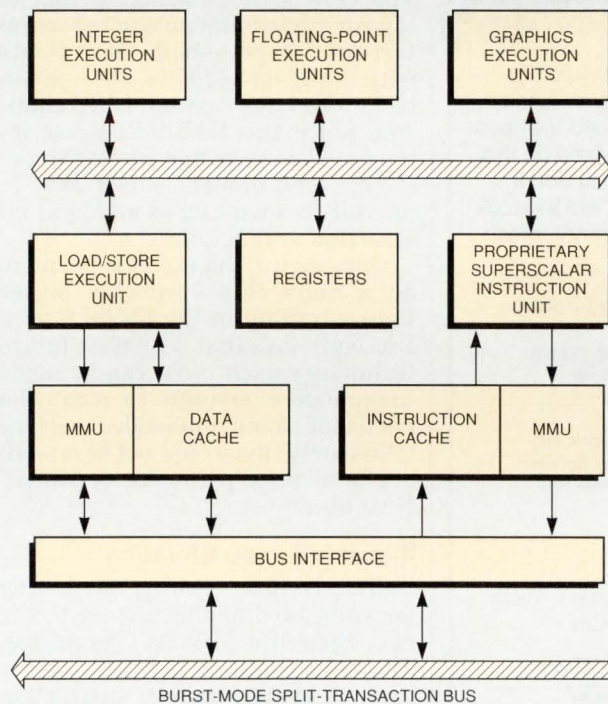
The Motorola approach is to assume multiple execution units, then try to partition the task of instruction scheduling between the compiler and the on-chip dispatch hardware. "You need to find a balance between the burden placed on the compiler and the hardware," argues Jeff Nutt, 88000 marketing manager. "In the long run, everyone changes hardware implementations

very general road map, starting with the 88110 execution unit. The part integrates the MMUs and caches from the old 88200 chips onto the CPU die. But more important, it combines a number of integer, floating-point and specialized execution units under one dispatch unit and register file. Under Motorola's scheme, the exact number of execution units and their design would be no more than an implementation detail.

CPU die gets bigger

Motorola claims that the 88110 and its relatives will be capable of three to four times the performance of today's RISC chips. But this speed

MOTOROLA'S SUPERSCALAR APPROACH



A concept diagram of Motorola's 88110 processor chip suggests its close affinity to other superscalar architectures. But the device is more ambitious than existing superscalar devices, potentially using a large number of execution units and a symmetric dispatch algorithm to execute six to eight instructions per clock.

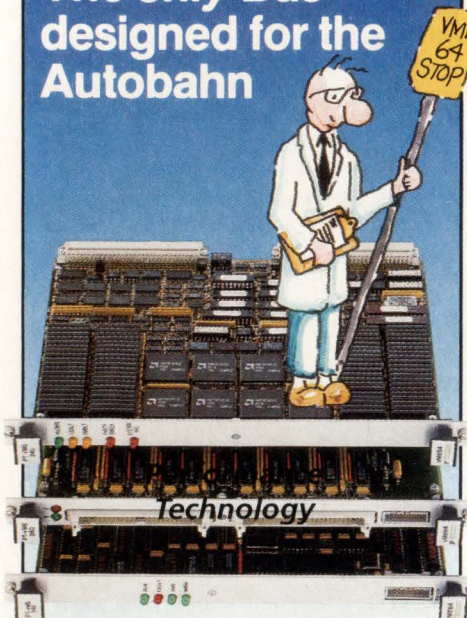
of their architecture from time to time. But you don't want to have to recompile all the old code when you do. So you try to put architecture-related optimization tasks—things that won't change from version to version of the chip—in the compiler and put implementation-related optimization tasks, such as instruction dispatch, in the silicon."

This concept lets Motorola draw a

has not come from a big boost in clock frequency; it has come from making the CPU die enormous. A similar trend is taking shape in the embedded computing world, but for a quite different reason. Here, one of the initial objections to RISC processors was their size—it took 20 to 30 packages to actually make a working computer out of the RISC microprocessor. Vendors are now

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solving that problem by putting much of the supporting circuitry for embedded RISC applications on the CPU die. And again, the die is getting bigger.

Motorola has taken an obvious step in this direction by combining the Inter-Module Bus (IMB) architecture of its 68300 series microcontrollers with the 88000 core. The resulting family of products, which will have the 88300 name when it's formally announced, will provide the same sort of peripheral options as in the 68300 family, but presumably with higher CPU speeds and 88000, not 68000, instruction compatibility.

Adopting the 88000 to the IMB, though, is more than just a matter of editing in a new library cell. The 88000 core requires some significant modifications, according to Nutt. The core logic is being revised to improve determinism and reduce interrupt latency—both sore points with many embedded-system architects who have rejected RISC chips. And since the IMB was never intended as a cache bus, an 88000 core in this environment would have to provide its own caches and local instruction and data buses.

Once again, the result is bound to be a huge chip—probably bigger than anything in the 68300 family. But Nutt says that with near-future technology such a die can be made inexpensive enough to meet the needs of some embedded niches. "Obviously this would not be a product for all price/performance points," Nutt observes.

Instruction proliferation

Fujitsu is also pursuing integration for embedded applications with the new Sparclite MB86930 processor. The chip contains a Sparc integer unit, 2 kbytes each of instruction and data cache, most of a page-mode DRAM controller, and dedicated real-time debug hardware. A second chip, the 86940 Companion Chip, augments the 86930's hardware with an interrupt controller, four timer modules and two USARTs (universal synchronous/asynchronous receiver/transmitter). But the most interesting story about Sparclite may not be in the hardware integration—similar to that of embedded Sparc chips

recently announced by other vendors—but in the instruction set.

"This chip was designed from day one to be an embedded Sparc device," says Tony Bozzini, director of worldwide sales and marketing at Fujitsu. One of the results of this focus is that the company abandoned the strictures of the original Sparc instruction set and added codes to meet the needs of its embedded processing customers.

The new Sparc device has a multiply instruction—a first for Sparc chips—backed by a 32x32-bit hardware multiplier. This permits the device to achieve a peak rate of 12 MOPS on multiply-accumulates, operations that were a particular annoyance to the classic Sparc. Another operation that proved tedious in the old instruction set was finding the first zero in a string—this too is implemented in a new instruction.

In adding new codes, Fujitsu has attempted to comply with the latest thinking from Sparc International. "This will be the first chip implementation compatible with Sparc version seven," Bozzini claims.

Motorola's 88000 road map and Fujitsu's new CPU seem to confirm the pattern that announcements from Integrated Device Technology and LSI Logic suggested earlier in the fall. The original simplicity of RISC is giving way to increasing, often application-directed elaboration. The trend will probably hamstring RISC founders' original idea of a fast, nimble chip that could quickly hurdle process boundaries. But this move from elegantly simple beginnings to more complex implementations is familiar—it is the natural evolution pursued by computer architectures since the dawn of the industry.

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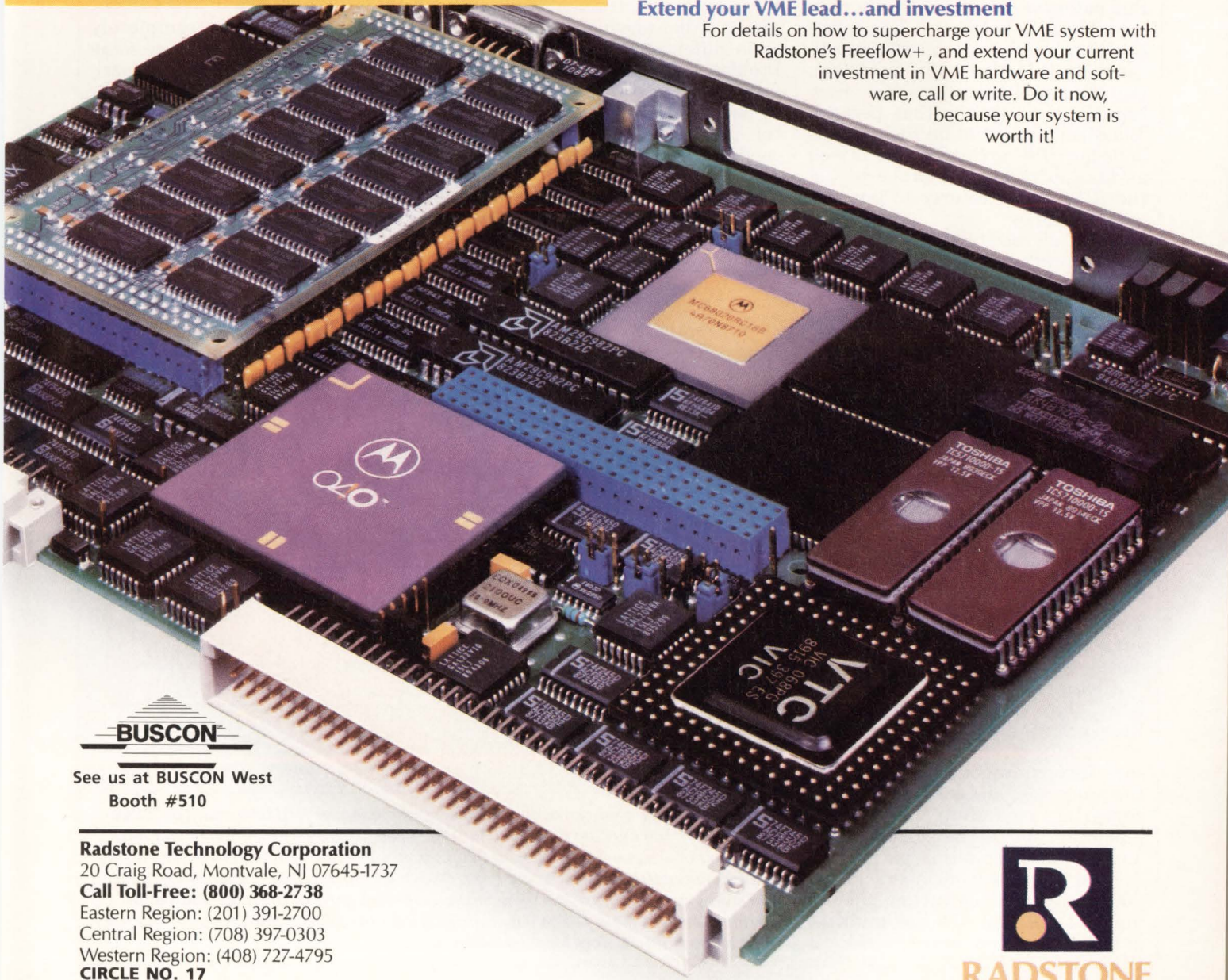
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RADSTONE
TECHNOLOGY

Two compilers squeeze more performance out of RISC chips

Tom Williams, Senior Editor

Advances in processor technology are today being lumped together with varying degrees of justification under the title of RISC architectures. For some time, these advances have borne the promise of greatly enhanced performance through pipelining, multiple execution units and generally more-efficient code execution.

The ability to take advantage of this potential hasn't been fully realized, though, because it has taken compiler technology much longer to catch up to advances in hardware. Optimizing compilers are now beginning to appear that perform "classical" optimization such as that done for CISC architectures, as well as take advantage of properties of the RISC architectures to improve code efficiency.

Although there are different RISC designs and an ongoing argument as to what constitutes "pure" RISC, the major goal remains the same: to do more operations per unit of time, aiming at one instruction per cycle or better. Simplified instructions and addressing modes help RISC processors run faster, and pipelined architectures and multiple instruction units aid parallelism. RISC machines are load/store architectures with rich register sets to minimize memory accesses that slow down operations. But how to put all this to work?

Addressing pipelining

Two compilers for Intel RISC processors have recently been introduced—one from Alliant Computer (Littleton, MA) for the 860 64-bit RISC chip, and one from Microtec Research (Santa Clara, CA) for the 960 family of 32-bit RISC processors. Two characteristics shared by the processors and addressed by the compilers are their instruction pipelining and (in the case of the 860 and the 960CA) multiple parallel execution units. All members of the 960 family have instruction pipelining, but only the CA has multiple parallel execution units.

Pipelining is the answer to the fact that some instructions, such as multiply, divide and floating-point operations, inherently take several cycles. By prefetching and lining up instructions in the pipeline, the processor can output a result every cycle once the sequence gets going, and the pipeline continues to be fed with instructions. Even if each individual instruction takes, say, three cycles, instructions following can be either moving in the pipeline or in different stages of execution. Problems arise when a three-cycle instruction is immediately followed by one that depends on the result of the preceding instruction. Such a condition can cause the pipeline to stall.

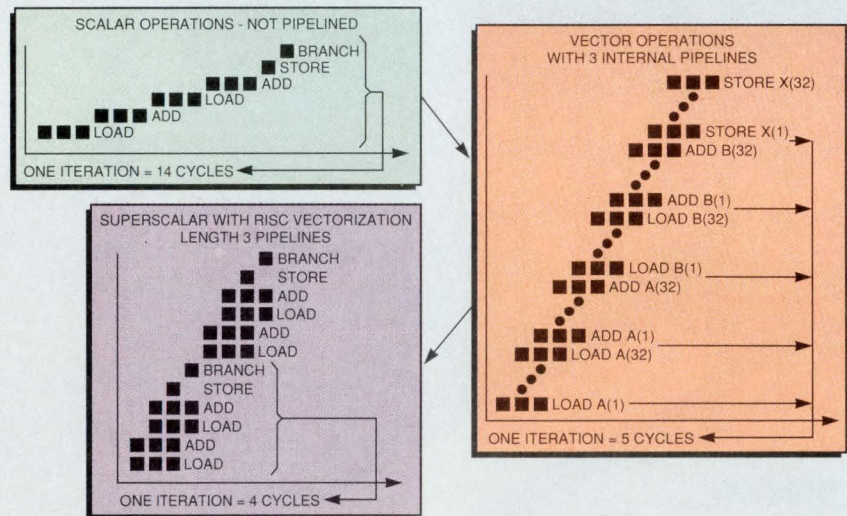
One could insert instructions into the stream to delay execution of any following instructions until the result needed by the next real instruc-

tion is available, but that isn't satisfactory for performance. Both Alliant's and Microtec's compilers perform instruction scheduling within basic blocks to try to find instructions that can be executed independently while dependent instructions are waiting for results to appear. The compiler generates assembly code from the source lines, and then analyzes it, looking for as many instructions as it can find that can be executed independently from each other. It then rearranges the code to minimize delays, inserting independent instructions into the sequence between dependent ones.

Exploiting parallel architectures

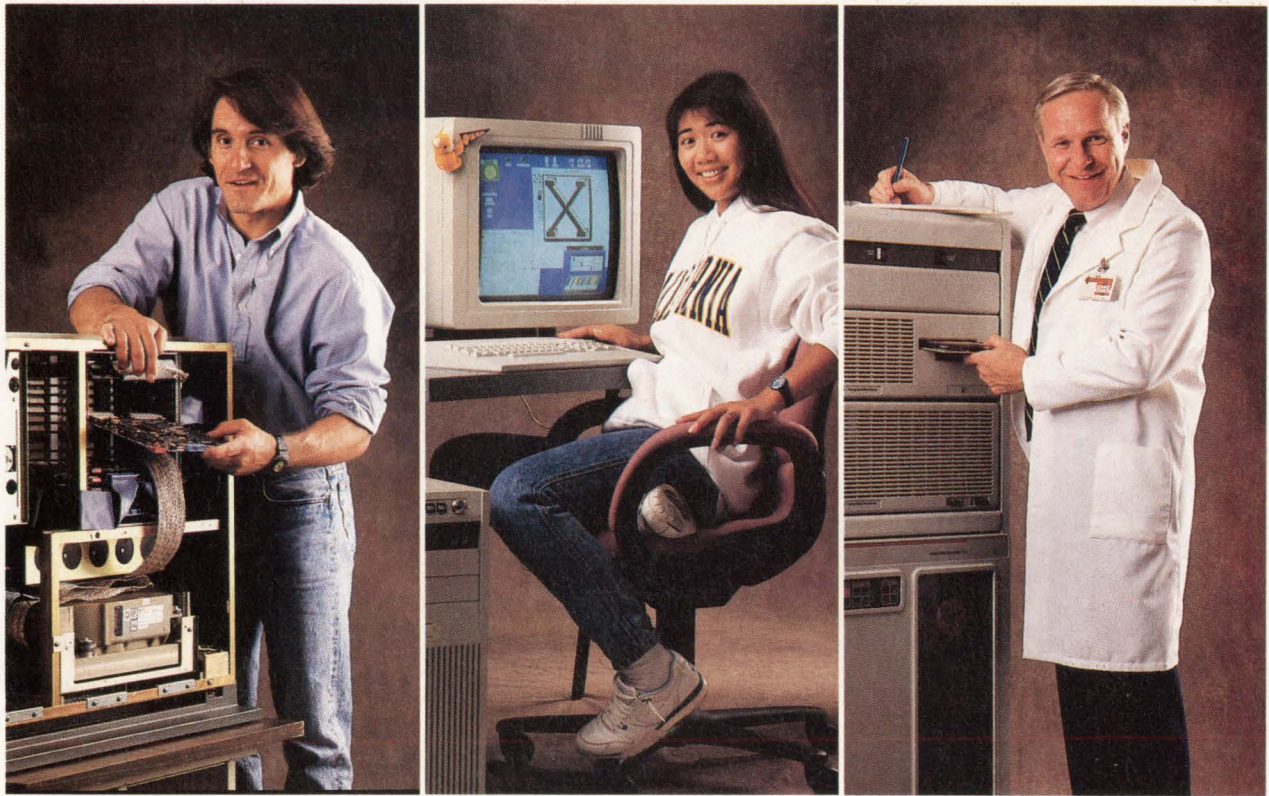
The process is never completely ideal; there will always be some delays. And, says Antonio Bigazzi, Microtec's director of compiler technology, "As the number of instructions in a basic block increases linearly, the complexity of solving their optimization increases exponentially." But since the optimization process isn't I/O-bound and most basic blocks are manageable, the process doesn't seriously affect

INSTRUCTION-LEVEL PARALLELISM



Vector operations on a conventional scalar machine (upper left) take many cycles because everything must be done sequentially. Alliant's RISC vectorization (lower left) rivals that of a true vector processor thanks to its pipelined architecture and its ability to execute several instructions per cycle. Once the loop gets going, then loads, adds and stores can be done at the same time on different parts of the loop. The vector machine involves more preliminary overhead than the 860 because its vector registers must all be loaded before loop execution begins.

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CIRCLE NO. 19

SOFTWARE

compile time, he says.

The analysis of basic blocks for dependency relationships identifies groups of instructions that, since they aren't dependent on each other, could be executed in parallel. In superscalar architectures—which have multiple execution units and thus can execute more than one instruction per clock cycle—nondependent instructions that can run on separate units can execute in parallel.

done in sequence.

Microtec has added another trick, called migration, to improve parallelism even more in some cases. Migration takes advantage of some of the 960's complex addressing modes (not strictly a RISC feature) to do some arithmetic operations in the memory unit that would normally require the register unit. An instruction to add the contents of two registers and store the result in a third,

in several percentage points of improvement overall. In RISC optimization, improvements of 2 percent or 3 percent are considered major advances.

Eating up vector operations

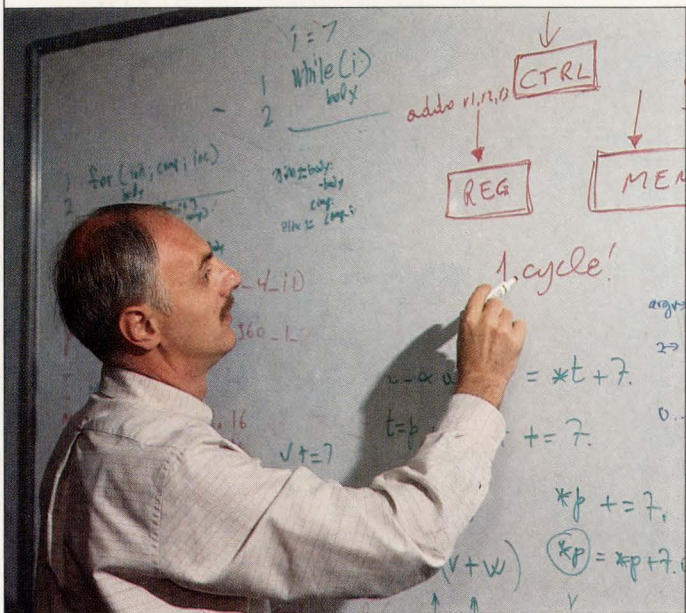
Alliant's latest machine, the FX/2800, is a multiprocessor, 860-based supercomputer aimed at scientific applications in which operations on large arrays of data are commonplace. Alliant has developed a technique on the 860 that it calls RISC vectorization. Microtec has a similar technique for the 960 it calls software pipelining.

"The machine itself doesn't look like what you would consider a conventional vector machine. It doesn't have vector registers," says Alliant's compiler architect, Stephen Hobbs. Still, it's possible to run the machine so that it keeps memory going at full speed while going through vector-like code, he says. The technique takes advantage of the 860's pipelines and its multiple execution units.

A single precision add or multiply takes three instruction cycles from the time you push it into the add or multiply pipe to the time you get a result. So when you push two operands into the pipe, you have to wait three instructions for results. Once the adder and multiplier get going, though, they can output a result every cycle as long as their pipelines are kept supplied with data. In addition, the 860 can do both a load from memory and a floating-point instruction at the same time; memory loads are pipelined as well.

Addressing cost/performance

It's possible to construct a very tight, two-cycle loop—and in a two-cycle loop, it's possible to execute four (sometimes six) instructions, according to Hobbs. Once it gets going, the loop can be fetching from memory, doing arithmetic operations and storing data back every cycle. "And that's as good as a vector machine can do," Hobbs says. "We're getting the same performance out of a simple RISC machine that we would have gotten out of a complicated vector machine. Namely, we're able to do a memory reference every single memory cycle by stepping through a vector." Of course, there are very



Microtec Research's director of compiler technology, Antonio Bigazzi, says that in addition to special RISC-related optimizations, more-classical optimizations such as register coloring can be of great importance because they minimize memory references. "In a RISC architecture, you should never touch memory. Memory is a terrible bottleneck," Bigazzi says.

allel. The 860, for example, is an n=4 superscalar processor with parallel address, register execution, control and floating-point units, while the 960CA is n=3 with memory, register and control units. Intel is expected to introduce an 960CB in the near future, which will add an FPU, making it n=4.

For these Intel processors, the compiler's job is to look at the code scheduled for pipeline optimization. The compiler must then pick out those instructions that can be simultaneously dispatched to separate units and put them in the proper order. In the 960, the dispatcher hardware looks at four instructions at a time and can send three of them to the three units at once, if the instructions are of the proper type and in the correct sequence. The optimizer, for instance, will help the dispatcher hardware by trying not to have two memory instructions in a row because they would have to be

for example, might be followed by an instruction to shift the contents of a register two places left and store the result in a second register. Both operations would normally require the register unit and would have to be done sequentially. Microtec's Bigazzi says it's possible to "smuggle an instruction from one unit to another" by disguising it.

The Microtec compiler can spot instances where the memory unit could do one of the required calculations. Since shifting left two places is the same as multiplying by four, an address instruction can be used to compute an address from the initial value (multiplying it by four) and store it in the desired register. Now the two required operations—those that produce the intended results—can be done simultaneously by the memory and the register execution units. While actual improvement depends a great deal on the nature of the program, it can result

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SOFTWARE

complex and expensive vector machines that may perform better, but Hobbs' point is addressed to a cost/performance target.

The Alliant compiler does a higher level of scheduling to produce parallel code in that it can also distribute

independent portions of code to run on the multiple 860s in the system. To do this, it must not only decide which pieces of code can run on separate processors; it must also know which loops or segments of rescheduled code must remain on a

single processor. For very large matrices or loops, the Alliant compiler can allocate portions of the 860's on-chip cache for vector data or other variables.

Since the Alliant compiler is available through Intel for other 860-based designs, it provides a parameter table for the user to enter a description of the machine architecture (different cache configurations, memory and so on). It also supports the Intel parallel architecture extended (PAX) specification to let other designers use the 860 to develop parallel systems.

More tricks

RISC architectures are going to be big playgrounds for compiler designers because of the advantages of squeezing ever more efficiency out of code. Optimizing compilers for RISC by rescheduling instructions makes hand tweaking assembly code impractical, because with instructions rearranged, it's impossible to analyze the flow of execution at that level. "We manipulate the loops—sometimes we mangle them—to make them work better," says Microtec's Bigazzi.

Alliant's Hobbs agrees. "The loop you get from the compiler's point of view is very difficult to analyze. You really can't do this by hand. This is definitely a machine you want to use a compiler for," he says. In fact, Bigazzi jokes, RISC stands for "Relinquish Important Stuff to the Compiler." And compilers will continue to be refined to do the kind of tweaking automatically that used to be done at the assembler level.

Two additional examples of the kind of optimization that's being done at the compiler level are branch prediction and splicing. Branch prediction makes use of the 960's prediction bit. That bit is used to indicate that the program will probably branch at a given instruction. If the processor jumps, it has to flush the dispatch queue, decode the next sequence of instructions and then continue. A correct prediction of a branch lets the processor decode in advance the next four instructions at the target label and have them ready. A correct prediction of not branching lets the processor run on normally. A wrong guess costs two cycles.



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CIRCLE NO. 21

SOFTWARE

In static prediction, based on statistics gathered from running millions of lines of code, you simply set for the most probable action. In loops, you can predict that the code will probably jump back to the beginning of the loop—except for the last iteration. In IF statements, the ELSE path is taken more often, because the THEN path represents the exception condition. Statistics show that code is 67 percent more likely not to jump in IF statements. Over the long haul, that approximate 2:1 advantage can save a lot of overhead.

Microtec is working on a dynamic form of branch prediction in which real application code is run using a tool called Hindsight. Hindsight gathers run-time statistics on branches and helps tell which way to set the prediction bit for each possible branch.

Splicing is another branch optimization technique that can actually decide to substitute a more appropriate instruction for a given situation. The 960 has an instruction called COBR that compares two registers and branches if they are different. COBR takes three cycles. The traditional method is to execute a compare instruction (three cycles) and then a branch (one cycle) if there's a difference. Doing the latter with no instructions executing while the compare is waiting for results is very inefficient because there are useless delay cycles. The best method is to insert unrelated instructions between the start of the compare and the branch so the pipeline is busy. The next best method is simply to use the COBR instruction.

The Microtec compiler first generates the worst-case scenario for all the branches in a block—the compare, delay, delay, branch. It then looks for instructions it can insert between compare and branch instructions to make maximum use of cycles. For those compare/branch instruction pairs the compiler can't fill in, it substitutes the second-best COBR instruction.

Development of new optimizations techniques for RISC processors is an ongoing science, and we can expect even more-exotic methods as the discipline matures and newer architectures begin to emerge. Although it's difficult to

give real numbers that cover a general range of actual programs, Microtec's Bigazzi says the effort is well worth it because "with RISC architectures, the difference between 'just decent' code and good code can be staggering." ■

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SOFTWARE

Consortium moves toward a real-time BIOS standard

Tom Williams, Senior Editor

The Real-Time Consortium (Sunnyvale, CA) is getting closer to its primary goal of establishing a low-level software interface between hardware and operating system software. Called the Open Basic I/O System (OBIOS), the standard is aimed at relieving programmers of much of the tedium of writing device drivers for different hardware platforms.

The consortium is a group of software vendors and board manufacturers that has been congealing over the last few months to promote real-time computing standards. Its charter members include board makers Force Computers and Heurikon, and software vendors Ready Systems, Wind River Systems and Lynx. In addition to working toward the OBIOS standard, the Real-Time Consortium is supporting real-time standards efforts in the IEEE-1003.4 extensions to Posix and the Executive Processor Interface Specification (EPIS) developed by the 88Open consortium.

EPIS concerns the interface between a real-time operating system and the CPU/memory upon which it runs. It has initially been implemented for the Motorola 88000 but can be adapted to other CPUs.

Focus on I/O

OBIOS, on the other hand, concentrates on I/O issues to let a common interface for device drivers access all sorts of hardware peripheral devices. OBIOS is conceived as a passive server that's called by operating system-level clients. The application (through the operating system) sees an abstract interface to such devices as counters, timers, SCSI controllers, UARTS, disks and Ethernet controllers. The details and data structures for actually manipulating the hardware are behind the OBIOS interface.

Currently, system designers must write device drivers that contain code segments specific to both the hardware and the operating system. And for every change of hardware,

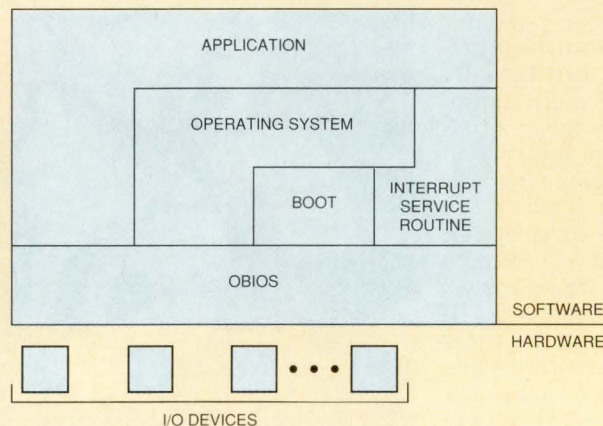
new driver code must be written that explicitly manipulates the details of hardware devices (registers, addresses and configuration codes). This problem has long since been solved in the personal computer arena by the existence of a BIOS. The same sort of solution is hoped for in the real-time world.

OBIOS is operating-system-independent and doesn't have any references to semaphores or mailboxes,

calls to functional units include: START, ABORT, POLL, RESET and commands to enable and disable the unit and/or interrupts. With this simple interface specification, device drivers can be written to read and write data, set baud rates, poll for activity on a device and do everything device drivers need to do without the programmer needing to know the internal physical details of the hardware.

The Real-Time Consortium has put out a final call for technical input to its draft for an OBIOS standard and expects to have a document ready for public comment by the time of the Buscon/91-West show in January. The draft will in-

OBIOS: COMMON INTERFACE TO HARDWARE



The purpose of the Open Basic I/O System (OBIOS) is to provide a common, abstract interface between all other system- and application-level software and the underlying hardware. Even interrupt service routines, which operate outside the OBIOS, are its clients when accessing hardware functions.

nor does it allocate or deallocate memory or queue OBIOS requests. In addition, interrupt service routines (ISRs) are the responsibility of the client. During an ISR, the client may make calls to the OBIOS to handle I/O functions that may be part of the ISR. But at that time, the actual function and logic of the ISR is defined by the application.

OBIOS recognizes modules (devices or parts of devices such as ICs, boards or even parts of ICs). Modules are composed of functional units that are normally seen as the services provided by physical devices—that is, serial lines, timers and so on.

Clients interact with OBIOS via calls to modules that include GET_MODULE_INFO, INITIALIZE, TERMINATE and GET_MOD-

clude driver code that provides interfaces to several important classes of drivers, including serial I/O, networks, SCSI, timers and counters, according to Greg Buzzard, engineering project manager for Ready Systems (Sunnyvale, CA) and director of the Real-Time Consortium. It's hoped that once a standard is established, there will be a flurry of activity to write OBIOS code for a wide range of existing hardware to which drivers can then be written. ■

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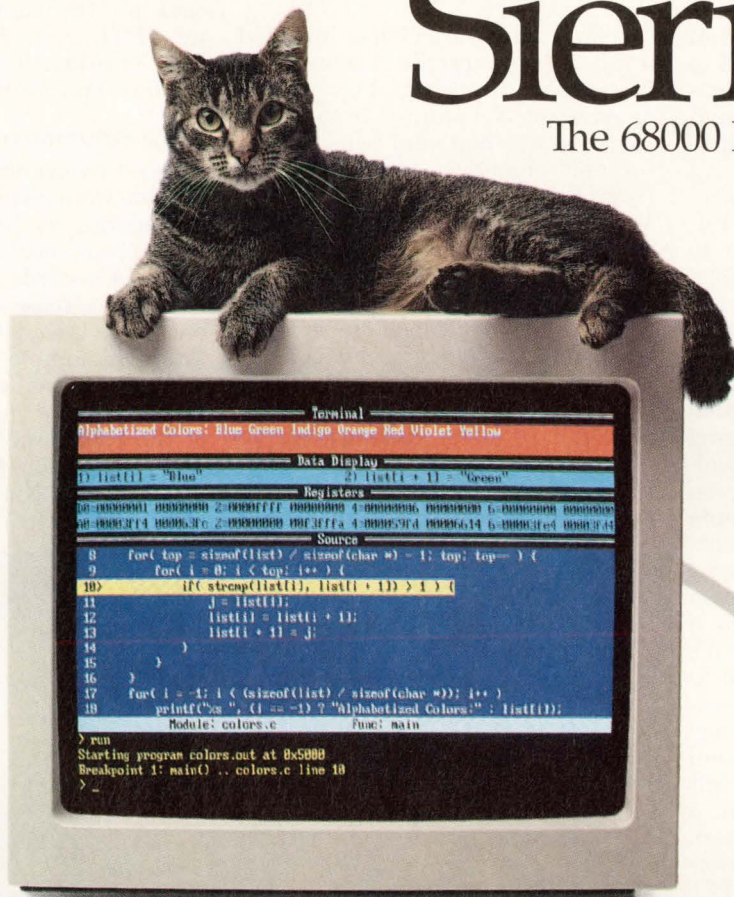
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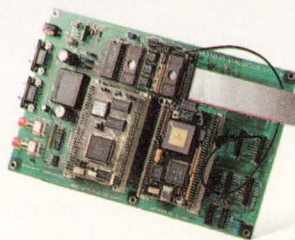


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CIRCLE NO. 23

Futurebus+ closes reality gap

Warren Andrews, Senior Editor

Futurebus+ is rounding the final turn and starting its sprint to the finish line to become a completed IEEE specification. Although few, if any, changes are expected to the basic specification (P896.1), it's likely there will be some to the profiles section (P896.2) as the Futurebus+ developers look to clean up and perhaps reduce the numerous and sometimes confusing profiles.

At the same time, a number of vendors—chip makers, backplane developers, connector fabricators, and board makers—have assembled early prototypes with encouraging results. In addition, emerging developments show promise of even greater performance enhancements and early commercial development.

While there's good news on some fronts, there have been setbacks on others. Tektronix, champion of the F (for fast) profile, announced that it's leaving the high-performance workstation business and therefore abandoning its efforts on the high-performance profile. Also, a personnel shuffle at Hewlett-Packard has left the committee that's working on a desktop profile without a chairman. Joe Trainor, director of North American business development at ITT Cannon, who was serving as vice-chairman, is filling in.

First working parts

Despite these setbacks, the mood of Futurebus+ advocates ranges from up-beat to euphoric over the prospects of seeing the specification completed. Yet some level of caution is advocated even by staunch Futurebus+ supporters. "The various committees, composed of 100 or more of the world's top engineers, have been working all-out over the past 18 months. One cannot expect them simply to put on the brakes and stop once the project is done. They'll have to come to a halt gradually—and that will probably mean a new specification or two before they're finished," comments one Futurebus+ supporter.

One of the highlights of Buscon/East held in October was the first real showing of working Fu-

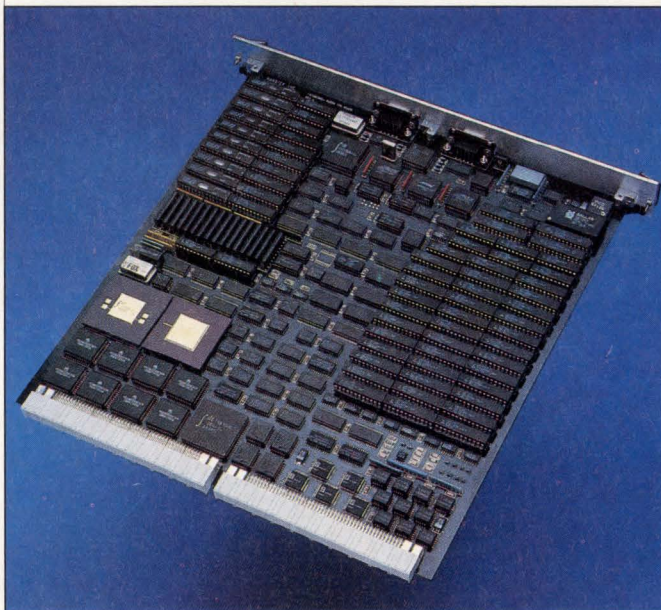
turebus+ hardware. These included a full, working profile A board from Nanotek; working bus interface/transceiver silicon from Texas Instruments, National Semiconductor and Signetics; and backplanes from Bicc-Vero and Mupac. Bicc-Vero (Hamden, CT) even boasted a functioning system—that is, a board powered up in a card cage. The board was one of the proof-of-concept boards developed under contract with the Navy and was actually on a soft metric platform (6U+480) instead of the recently approved hard metric dimensions.

And while these parts were essentially in complete conformance with the specifications, they didn't reflect

a few modifications possible with the somewhat larger board size," says Joe George, president of Nanotek. "This represents the first time we know of that all the components—connectors, BTL transceivers and Futurebus+ interface logic—have been assembled on a working card."

The Futurebus+ backplane

At least two vendors, Bicc-Vero and Mupac, were displaying Futurebus+ backplanes at Buscon. A working Futurebus+ enclosure with one of Nanotek's cards performing some random exercise was on display. The enclosure included a bottom section to provide ample forced-air cooling, while the actual card cage included plenty of space on the connector-end of the backplane for the Safenet 1 and 2 connectors that the Navy contract calls for. Neither of the Safenet cards was in the enclosure.



Nanotek demonstrated what is probably the industry's first Futurebus+ board to include all of the Futurebus+ 896.1 specifications as defined in profile A. The only exception is that the board was developed prior to the adoption of the hard metric sizing and before the arbitration scheme was changed.

the recent changes adopted at the most recent Futurebus+ meeting in Pittsburgh—for example, the decision to allow both a central arbiter as well as distributed arbitration. This affects both backplane and board design—changes not reflected in the demonstrated products.

The most dramatic of the working parts on display at the show was the R3000-based profile A CPU board from Nanotek (Idaho Falls, ID). "The board is a commercial version of the one we developed for the Navy, with

"Though much the same as any conventional passive backplane," says Michael Humphrey, vice-president of strategic marketing at Bicc-Vero, "Futurebus+ backplanes call for a little bit of special magic even at today's performance levels, and perhaps a lot more going forward."

The backplane on display at Buscon was a 6U-sized (as opposed to full profile A), 64-bit, 20-or-more-slot board. But to assemble the board while maintaining the signal-layer characteristics that are consis-

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tent with high performance while maintaining the current-carrying capacity that will be required for a full suite of boards, the board had to include 21 active layers. If the backplane were to include the additional lines called for by the just-approved central arbiter, the layer count could

lems have required considerable attention. Managing the power rails has called for some tricky fabrication techniques as well as special power connectors from the supply to the board. These connectors include multiple-pin pads to deliver the required power and eliminate spuri-

formance-related functionality. He sees many systems, particularly those appearing in the immediate future, requiring a relatively small number of Futurebus+ CPU cards and some number of additional I/O functions.

"The simple solution," he says, "is to provide a single card cage with three or four Futurebus+ slots and perhaps an additional eight or 10 slots to accept VMEbus boards to handle the I/O requirements." This basic concept was one of the early concepts of the Futurebus+ developers and, therefore, the concentration on the Futurebus+-to-VME bridge.

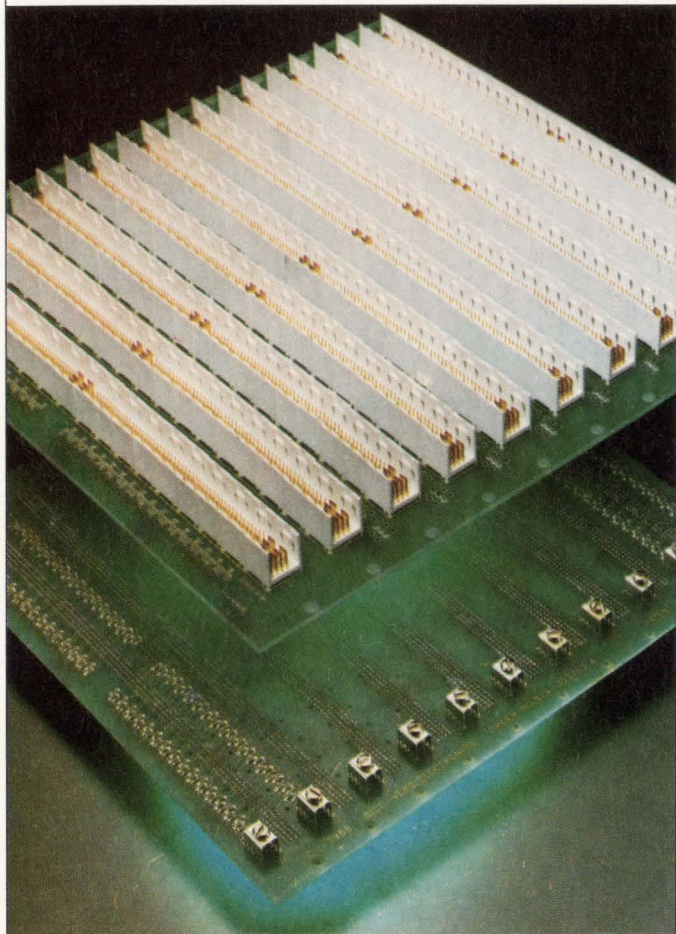
And while the concept of a hybrid (Futurebus+ and VME or Multibus) solution will reduce costs in some applications, it doesn't necessarily solve all the Futurebus+ backplane problems. The B profile, for example, has been defined primarily as an I/O profile, stripped of many high-performance Futurebus+ features. It's not unlikely that higher board counts might be called for when Futurebus+ is used as an I/O bus rather than as a processor bus.

But while it would be possible to fabricate a backplane specifically for an I/O version of the bus—that is, particularly for the B profile—it wouldn't be a Futurebus+ backplane. And a full-scale backplane with some 20 slots could be prohibitively priced as an I/O backplane. The solution may well turn out to be "implementation dependent," another way of defining a nonstandard standard.

The connector

Backplane issues aren't the only mechanical ones to keep Futurebus+ vendors on their toes. The 2-mm connector defined as part of the hard metric standard also has vendors scrambling to maintain both mechanical and electrical integrity. Factors of little prior concern, such as stub length (the distance from board to backplane termination), are suddenly crucial to system performance. At least two vendors have defined the Futurebus+ connector technology and are providing prototype devices. E.I. Du Pont has developed a connector it calls Metral, and ITT Cannon (Santa Ana, CA) calls its version of the connector Tempus.

Shaving off even relatively small



Bicc-Vero was one of two vendors showing Futurebus+ backplanes at the recent Buscon show. For a full-sized backplane, some 21 layers of printed circuit board are required between all the data lines, address lines, signal lines, power, and grounds. When the recently approved arbitration scheme is implemented, the backplane will probably require additional layers.

conceivably go as high as 24.

Humphrey concedes that the layer count for full-scale Futurebus+ systems will be high, as will be the associated prices. He scoffs at the \$10,000 to \$15,000 price tags discussed by some Futurebus+ detractors but admits such a backplane could easily exceed \$5,000 or \$6,000. "The big thing is that there are few systems that will call for a backplane full of Futurebus+ boards.

"The high layer count of the backplane is required to guarantee the signal integrity across the length of the backplane, as well as to supply the current required to each of the boards," he continues. "Both prob-

lem noise on the power bus."

But Humphrey says the backplane problem isn't insurmountable. "Backplane complexity is directly proportional to the number of slots," he says. "Backplanes with only four or six slots don't require the same elaborate construction." A four-slot backplane can be manufactured with as few as six layers, and certainly eight, 10 or 12 layers will suffice for slightly larger backplanes with up to six slots, he says.

Many—particularly early—Futurebus+ systems, believes Humphrey, will probably be somewhat limited in the number of boards required for the basic Futurebus+ per-

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CIRCLE NO. 25

COMPUTERS AND SUBSYSTEMS

distances that signals have to travel reduces signal skew that could be fatal to high-speed operations. "Even the small distance saved by eliminating the right angle of the leads from the connector block to the board is critical in a Futurebus+ application," says ITT Cannon's Trainor. The type of connection to the board is also critical to mounting ease as well as signal integrity, he says. "We're just now seeing the tip of the iceberg compared with what's coming only a few years down the road."

While not revealing any direct associations, Trainor says ITT Cannon is in negotiation with at least one semiconductor company to develop active connector technology. By including a transceiver in the body of the connector, he says, connector stub length can be significantly reduced. "While the level of performance possible today isn't going to call for this technology, the timeta-

ble is shrinking."

Though progress has been incredibly rapid thanks to an unprecedented spirit of cooperation from a broad cross section of competitors in the computer and electronics business, there's still some time to go before we'll see practical implementations of Futurebus+. It has been rumored that Digital Equipment Corp was going to make a formal announcement of the B profile at the recent Buscon show but was dissuaded by other Futurebus+ committee members who claimed the spec wasn't sufficiently tied down.

The next milestones will probably surface at January's Buscon in Santa Clara, CA, as DEC will parade its profile, and there will probably be at least one system demonstrated with more than a single board. In the meantime, it's likely that the Futurebus+ working groups will be looking to reduce rather than

increase the number of profiles to be offered. While there's no comment now as to how this will be done, it looks as if profiles may become subsets of other profiles.

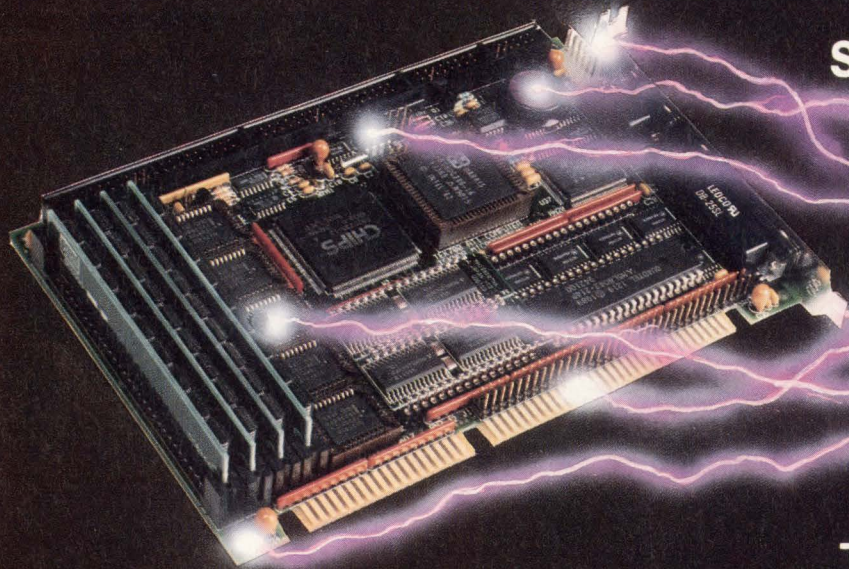
And while we'll see the beginnings of systems emerge in January, it's likely to be at least another six months before we see the first of any commercial Futurebus+ offerings. Most system vendors aren't much beyond the definition stage and have set hardware target dates sometime in 1992. ■

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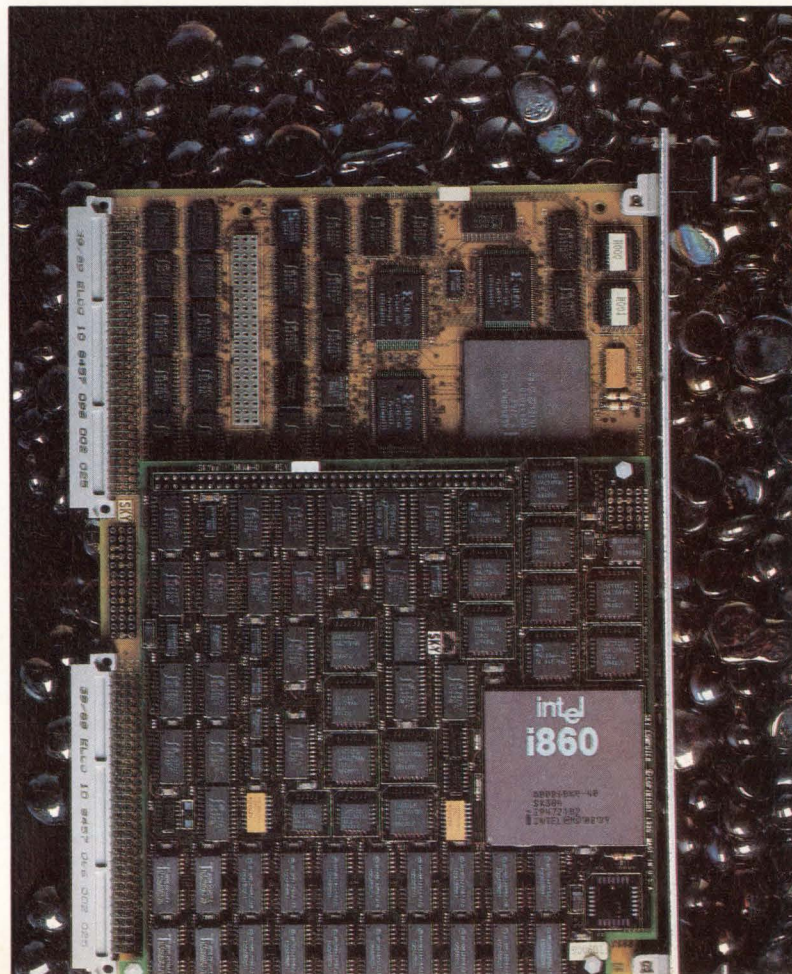
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CIRCLE NO. 27



Chase for process portability prompts advances in cell library tools

Barbara Tuck, Senior Editor

With the trend toward technology-independent design, library developers require parameterized cell representations that can be modified and reused as design rules and process technologies change. Compaction technology is key to porting these library elements to new processes.

Very often ASIC vendors have a new process ready months before library elements are available. Or ASIC and full-custom IC designers, working within a fixed design cycle, need to quickly develop libraries that can be retargeted to multiple vendors' processes. The process independence of library elements is crucial to library developers, as are automated tools that will yield accurate models. Instead of libraries of fixed cells with life expectancies of perhaps two years, libraries of parameterizable building-block elements are what ASIC vendors and designers are demanding.

Easing the creation of process-portable library elements or module generators (see "What is a module generator?" on p 49) is the idea behind a recent enhancement to the library development toolset from Mentor Graphics (Beaverton, OR). This toolset is based upon the GDT Designer module generation system. According to Richard Gordon, marketing director within Mentor's Silicon Design Division (Warren, NJ), the demand for tools that create prefabricated, reusable blocks is on the rise. What designers are ultimately after, says Gordon, is a chip that "looks something like a mosaic, with islands of recognizable structures in an ocean of routing."

Real-time connectivity

Building a module generator requires an integrated view of the design flow. Design data for creating behavioral, structural and physical views of a design, therefore, have to be accessible. With GDT Designer 5.0, Mentor has added a procedural interface that gives users read/write access to GDT's database. That da-

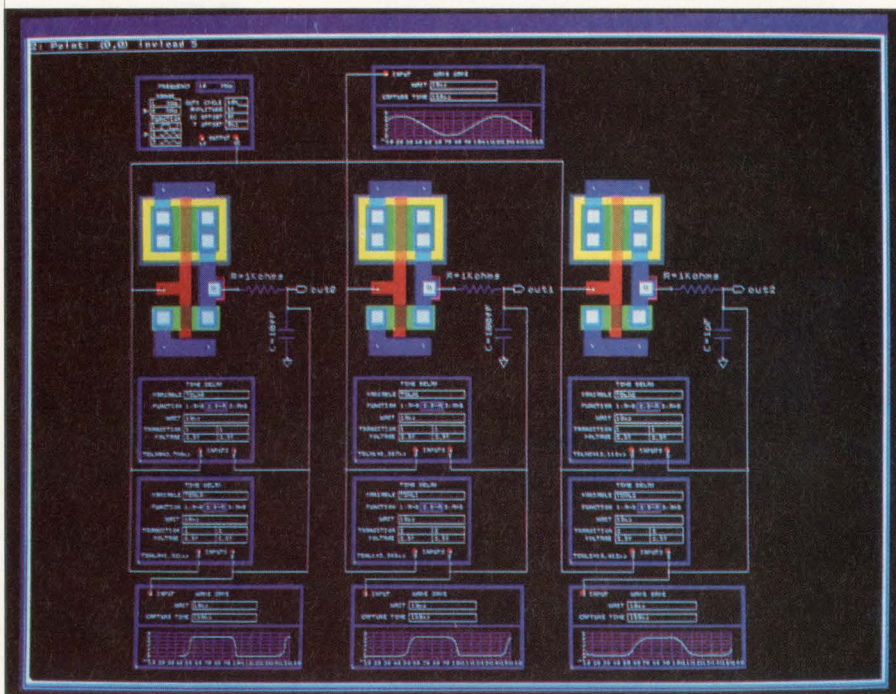
tabase is structured in such a way that it can recognize design objects and retain the associations between geometric data and connectivity data. With the new interface, users can access geometric and connectivity data concurrently when creating the different views of a module generator design.

In module generation systems with partitioned databases, connectivity data is stored separately from geometric data. When doing a task with such systems that requires integration—such as layout vs. schematic checking—the associations between the connectivity and geometric data of a module generator have to be reformed through the use of extraction and verification tools. The tools have to extract the netlist from the layout and verify that the layout matches the schematic. Since schematic and layout are bound to-

gether at the database level in GDT Designer, those intermediate steps are eliminated.

Like GDT Designer, the library development system from Valid Logic Systems (San Jose, CA) also has a single technology database that gives users real-time connectivity and eliminates the requirement for an extraction mechanism. Valid has just recently added a graphical interface to its module generation tool, which is dubbed Graph-A-Cell since users can sketch a device without regard for design rules or efficient use of area.

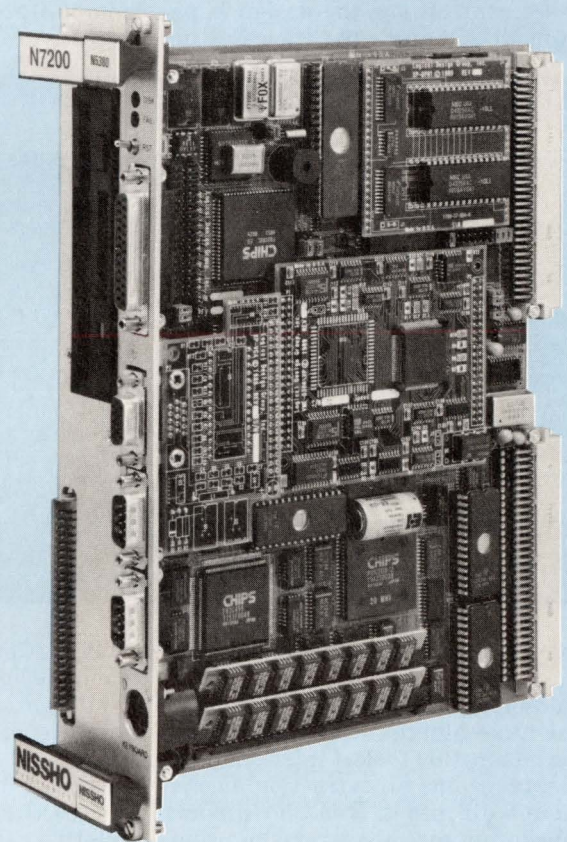
Graph-A-Cell incorporates a scanning technology that scans these loosely sketched geometries, reads the design-rule database and assigns design constraints to generate parameterized cells, or PCELLS. Users can modify automatically assigned constraints in addition to defining their own. A C code program from Graph-A-Cell can be stored in a device library and called up during layout editing to generate PCELLS. For anything more complex than a flip-flop or counter, as well as for complex geometries and odd angles,



Mentor Graphics has combined the analog behavioral modeling capabilities of its Explorer Lsim mixed-signal, multilevel simulator with circuit simulation to create behavioral models that emulate test equipment. GDT Designer 5.0, claims Mentor, adapts this technique to automatically characterize the generic standard-cell library it makes available, as well as user-defined libraries.

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users can modify the C program by adding code.

Valid's director of marketing, Dirk Wauters, claims that by not requiring users to do any programming, Graph-A-Cell distinguishes itself from the ModuleMaker module generation tool developed by Cadence Design Systems (San Jose, CA). Though ModuleMaker features Design-by-Example, which lets users draw graphical representations, users then have to produce procedural design code from the graphics. By assigning properties to the graphics, users control how the design is parameterized and what the resulting

turn." The Cadence ModuleMaker tool can handle most complex geometries, including 45° angles, according to Cho, who says that up until now most tools that maintain real-time connectivity have been restricted to 90° geometries.

■ A push-pull situation

The key to making module generators or any other cell library representation portable to a new set of design rules is compaction technology. Symbolic layout and compaction present an alternative method to manually creating a module generator layout and editing it at the

Compactors are the enabling technology behind the fast expansion or reduction of layout geometries when porting to alternative processes.

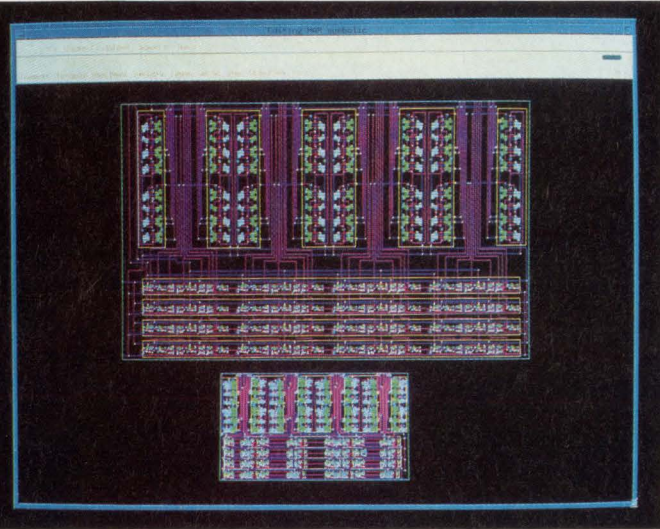
Mentor has added incremental compaction techniques to constraint-graph-based compaction techniques in GDT Designer 5.0. Because incremental compaction involves more user interaction, it will take the layout designer using that technique longer to specify a module generator layout. But Mentor's Gordon claims that incremental compaction offers the advantage of total control over the layout and 100 percent predictability.

Cadence's Cho, a pioneer in compaction technologies, has difficulty seeing any benefit to incremental compaction over the more traditional constraint-graph-based compaction. "The Cadence constraint-graph-based compactor is the only commercially available production-proven compactor," claims Cho, who says that Intel, Motorola and Toshiba are among the customers who have used the Cadence compactor. "Not one customer has requested incremental compaction," he says. "With constraint-graph-based compaction, Cadence customers can take advantage of new design rules when migrating to another process a lot more efficiently with regard to area."

On the merits of incremental compaction, Valid's Wauters says that "a powerful constraint-graph-based compactor eliminates the need for incremental compaction." With its recent enhancements, Valid has added a device-level compactor, which brings process independence to Valid's Construct (now called Construct P.I. for process independent) IC layout editor. That compactor is now in beta site and will be available for shipping by the end of this quarter. The new compactor complements the mixed block/cell chip-level compactor in the company's Compose chip assembly tool.

■ Limits to portability

VLSI Technology (San Jose, CA) has championed efforts in library development tools and compaction technologies. Though VLSI doesn't offer its customers compactors to automate the generation of a large number of cells, the company does make



Cadence Virtuoso compactor users report that more than 80 percent of their cells can be designed with symbolic layout and compaction to generate layouts comparable in area to manual polygon layout. Shown here is a cell of several hundred transistors before compaction (top) and after (bottom).

code will look like. That code can then be modified and used within module generators.

Unlike Mentor's and Valid's module generation tools, Cadence's ModuleMaker has an extraction mechanism built into it. Eric Cho, product marketing director for custom solutions at Cadence, sees the on-line extraction program as an advantage, not a disadvantage. "In general, for complex designs, it's difficult to maintain connectivity in real time," he says. Parasitic extraction on demand lets designers extract parasitics from a layout and relate that data to a new netlist, thus giving users greater ability to handle complex geometries, says Cho.

"If a module generator designer has a gate with two pins that he wants to connect, for instance, he might save area if he draws a wire at a 45° turn instead of a sharp 90°

turn. Instead of encoding each design rule as a spacing or width variable and placing each device according to design rules when laying out a module generator, the designer using a compactor tool spaces the devices and connections relative to each other with arbitrary spacing. He then calls upon the compactor to squeeze objects together or pull them apart so that the layout conforms to design rules and manufacturing guidelines. By maintaining tight control over module generator and individual cell layouts, compactors often achieve a density that matches that of handcrafted designs.

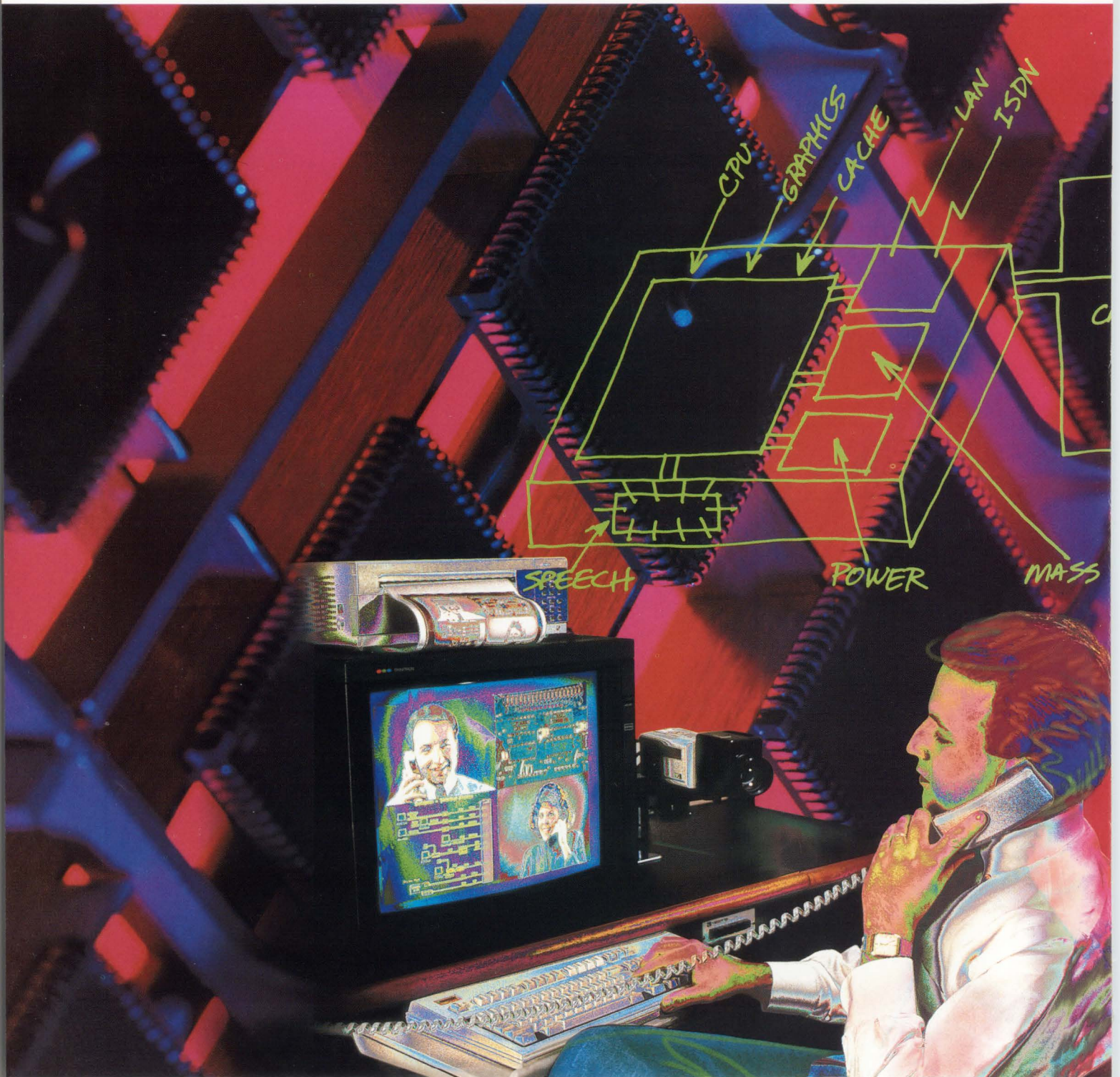
"Instead of handcrafting the layout," says Mentor's Gordon, "the designer plunks down Tinkertoy-like objects on the screen loosely and then calls on the compactor to push them together or pull them apart."

What do computer makers really want?



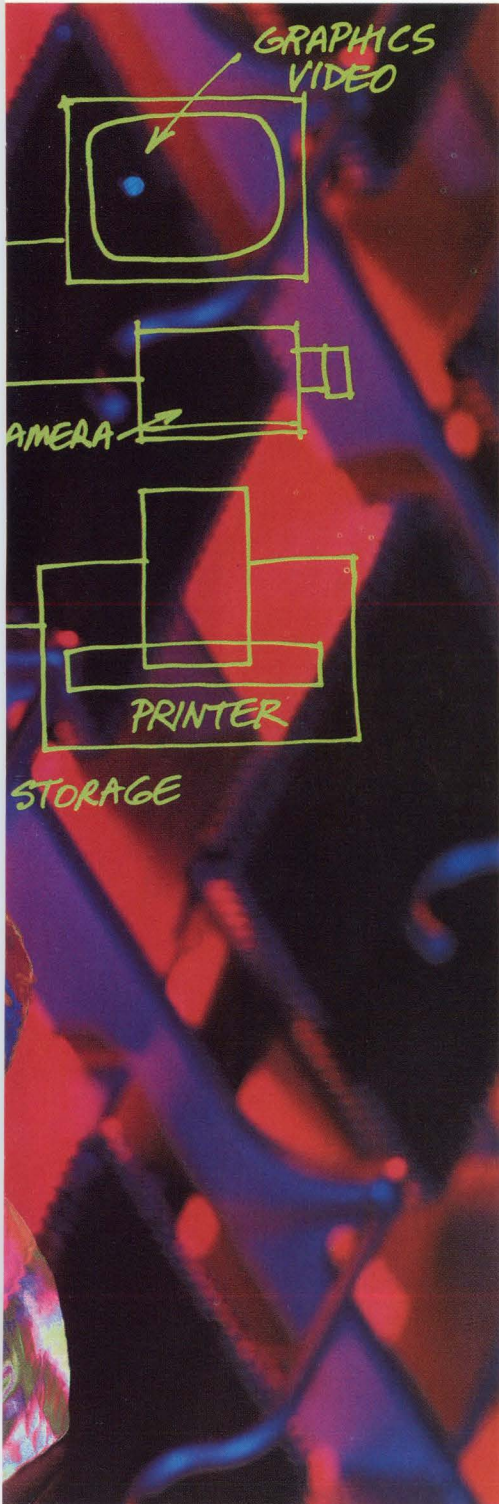
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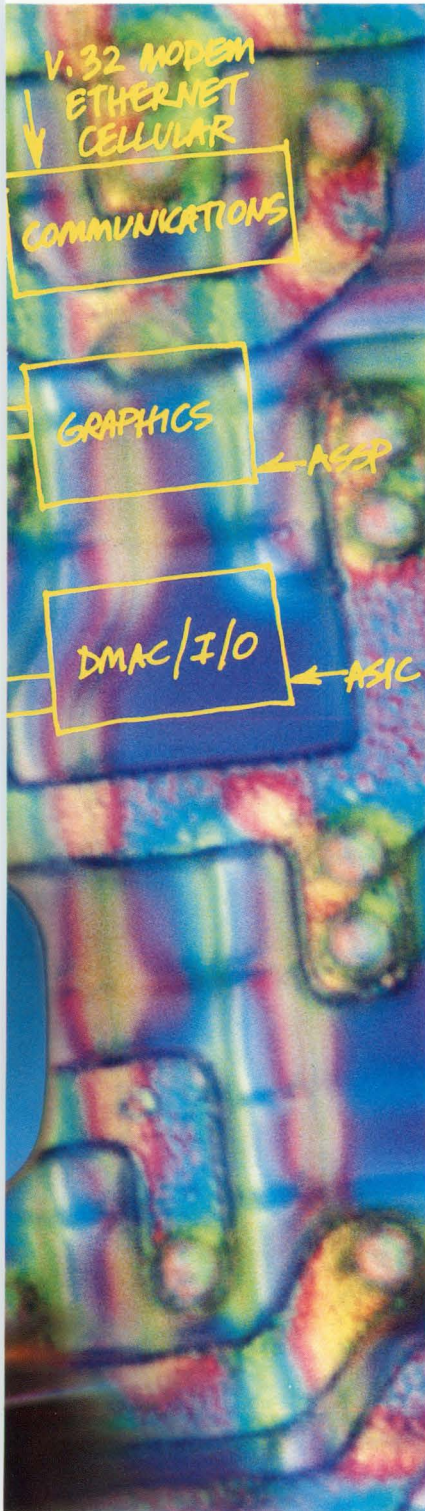
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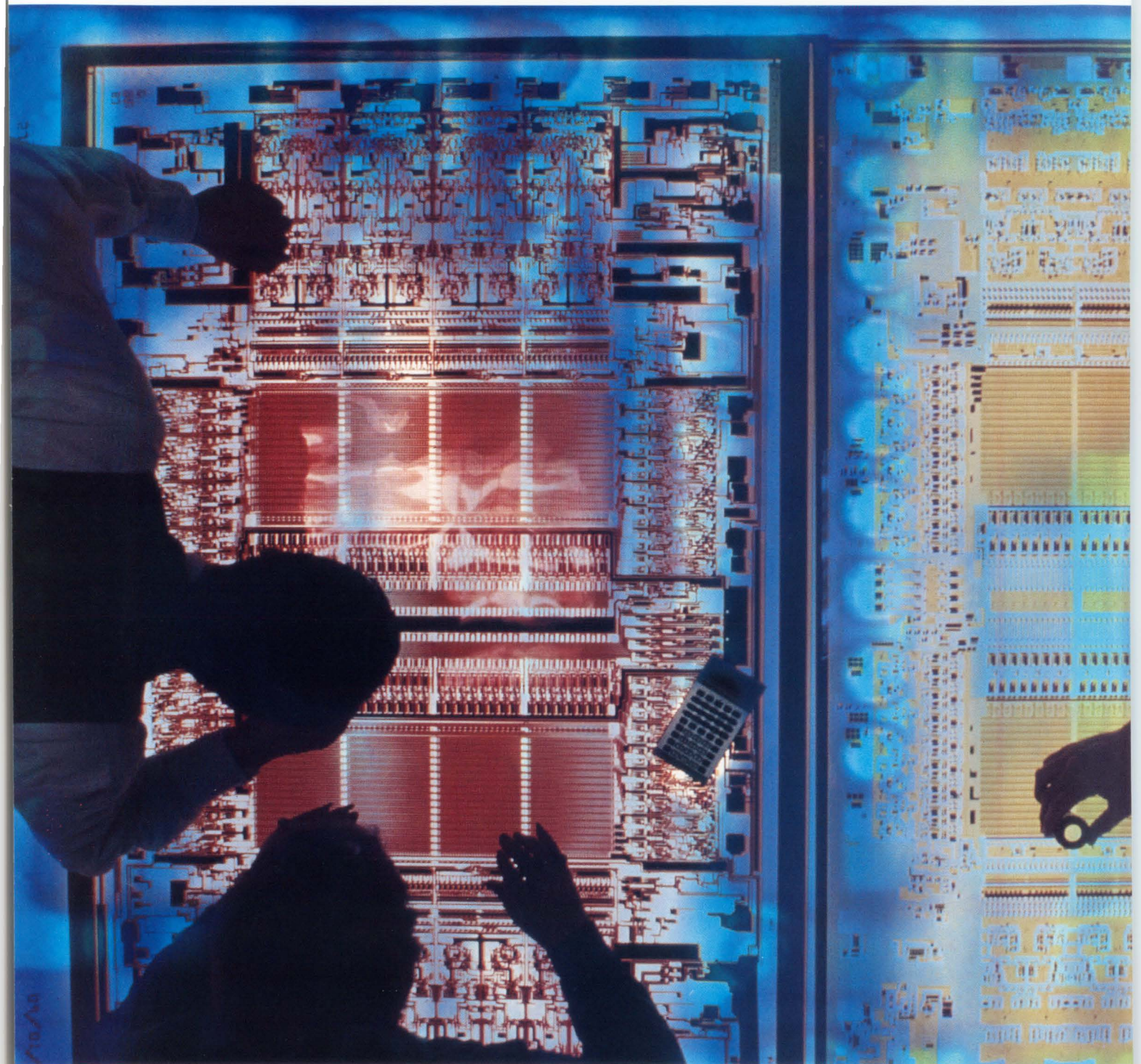
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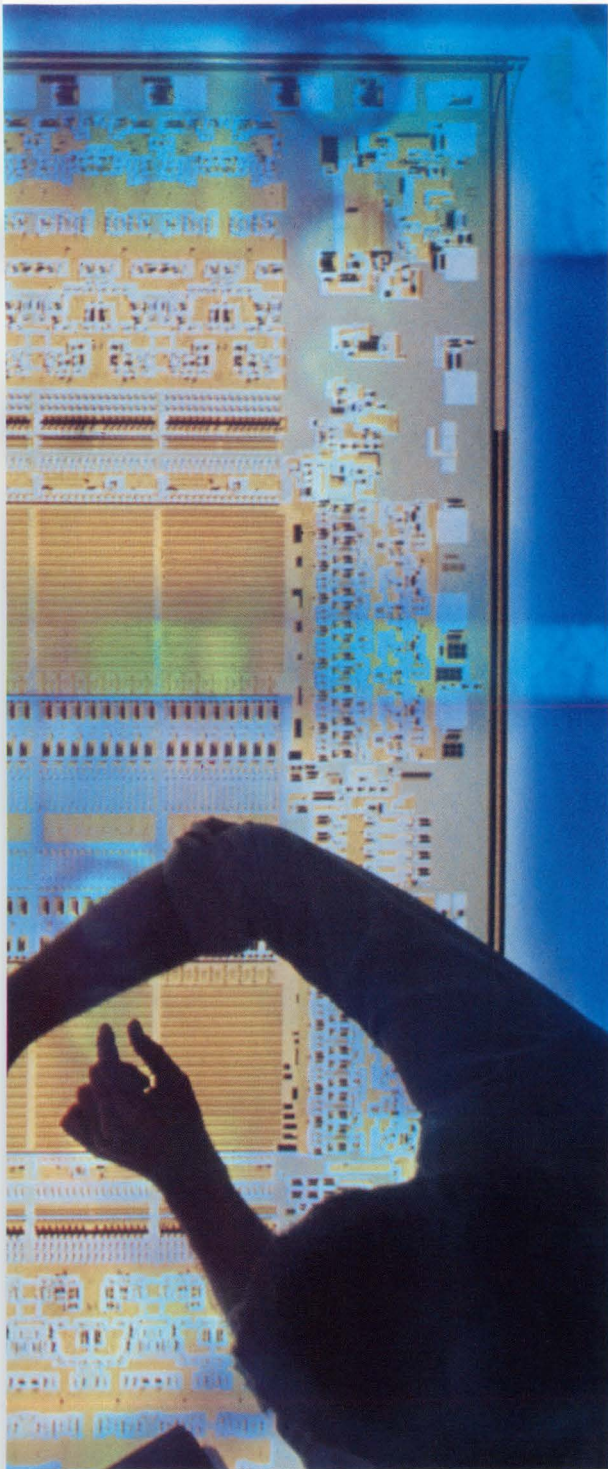


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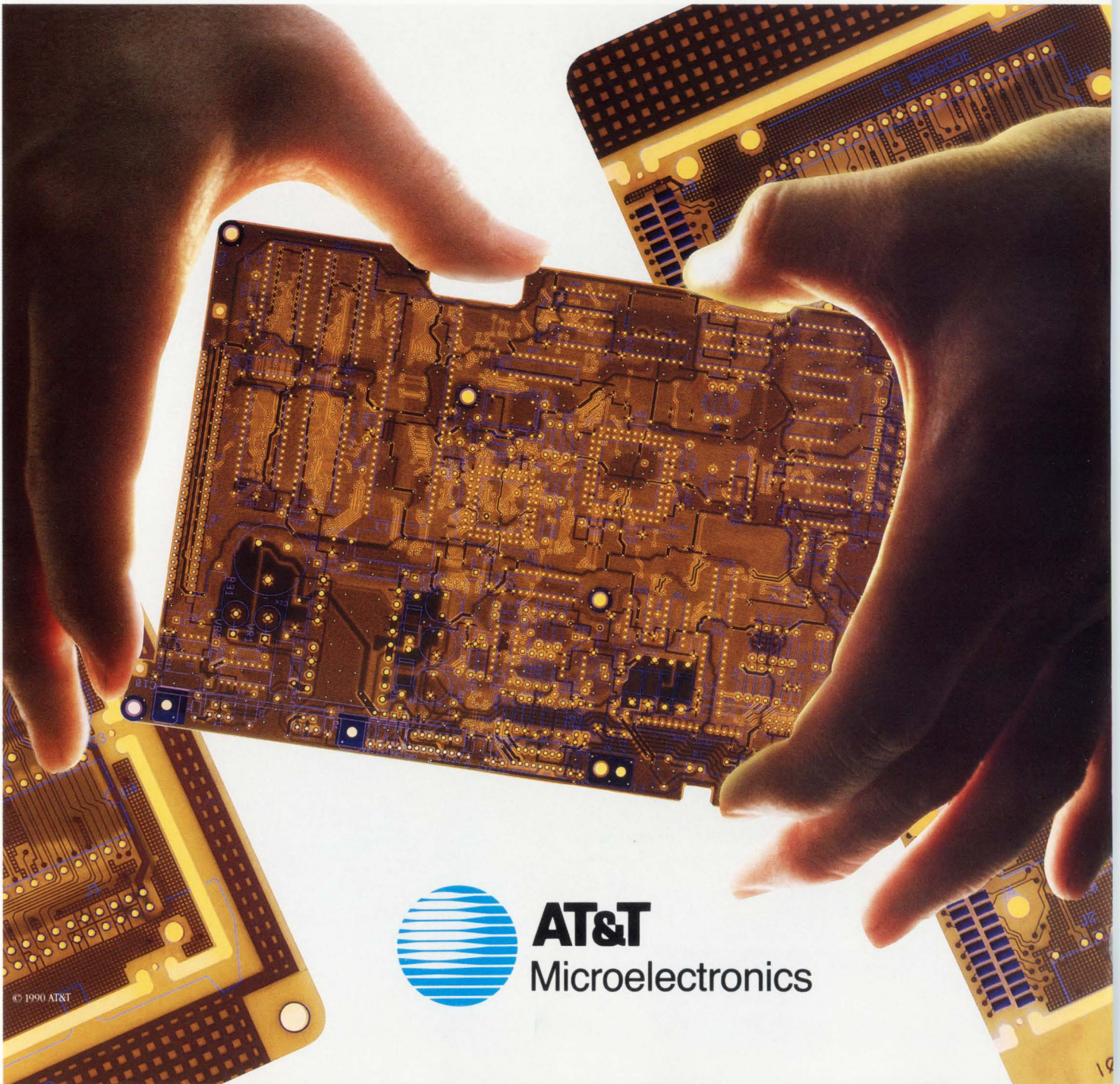
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available customer-generated compaction within design rules for MSI-level library components. Manager of library development software Duane Edgington reports that VLSI has used a combination of constraint-graph-based and incremental compaction internally for quite some time. Incremental compaction is beneficial, he says, for laying out very large blocks and also for handling nonrectangular layouts.

Though VLSI's internal development tools are among the best and allow for process portability through recompacted layouts of cell representations according to design rules,

What is a module generator?

Library development involves more than one type of designer and more than one type of design tool and, therefore, more than one view of each cell design a library supports. Among the views required for each library cell are a behavioral model for the system designer and system-level simulator, a structural view for the circuit designer and schematic editor, and a physical view for the layout designer and place, route and verification tools. A module generator is a compilation of the complete descriptions of all design views. Since it has access to all pertinent design data, a module generator can be reconfigured if either the design goals or the targeted silicon process changes.

Designers can build generators for NAND gates, flip-flops, counters or even RAMs, ROMs and ALUs. Those generators can be parameterized for size, function, drive, power, and so on.

Once a module generator is complete, it can be stored in a library for later use. Storing process-specific information separately from module generators ensures process portability and reusability. When a designer has to port a library to a new process, he simply calls upon the module generators he has built and modifies parameters to accommodate for changes. He then calls upon a compactor tool to produce an optimized design-rule-correct layout. By thus capturing design expertise in a reusable form, module generators automate the creation of cell library representations—from schematic symbols to the actual layout.

there's a point at which library elements aren't portable to a new process. In going from 1- μ m to 0.8- μ m CMOS, for instance, the design rules change enough, says Edgington, that VLSI has to lay out all the library cells again. The new cells will be scalable to future technologies, he says. Edgington also says that "the logic doesn't port when going from CMOS to BiCMOS or from CMOS to ECL. The design technologies and cell implementations are just too different." In that situation, logic synthesis is required for the remapping of technologies.

Edgington also raises the issue of backing up library representations with silicon. VLSI sometimes prototypes all library elements in silicon, and at other times, assumes correct design methodology for certain elements and prototypes subsets. "We run RAMs and ROMs into silicon because they don't behave very well when ported to new generations," Edgington says.

Still more questions

"The real issue for the ASIC vendor is giving customers the functionality that they want—whether that functionality comes in the form of module generators, compilers, or whatever," says Robert Nalesnik, VLSI product line manager for silicon and packaging. "From our experience, layout is only a small part of the library development effort. Significant questions remain—such as, can you get test vectors for the library? And can you simulate the library elements?"

Arun Kelapure, product marketing manager of compiler technology at LSI Logic (Milpitas, CA), agrees that the ability to simulate library elements to match silicon performance is at the top on the list of priorities. And that is more difficult with submicron process technologies, according to Kelapure. LSI Logic's new Concurrent Modular Design Environment (CMDE) incorporates a toolset called Charms (Characterization and Modeling System). Charms, which will be used internally to address issues of modeling for submicron processes, will feature multidimensional models for delay prediction.

Both LSI's current design system, the Modular Design Environment, and the CMDE—in beta site now

and expected to be available in the second quarter of 1991—employ a combination of incremental and constraint-graph-based compaction for layouts of library cell representations. Like the Mentor and Valid systems, the CMDE will have a shared database from which users can access geometric and connectivity data concurrently when building library elements.

Though time is of the essence when it comes to developing library models, there's really no accurate method for reporting how long it actually takes to develop and characterize a library with the various vendors' tools. One vendor may say that a library can be developed and characterized in a few days, and another vendor may say a few months. Without information on all the variables involved, these stated times mean very little. One library development task might involve the use of simplified delay equations to characterize 50 cells with simulation done on powerful machines running in parallel. Another task might involve a 300-cell library, complicated delay equations and a simulation situation in which the computer was a limiting factor.

Though some of the issues concerning library development tools are changing, the basic underlying one continues to be the delicate balance that must be struck between the accuracy with which library cells are characterized and the length of time it takes for that characterization. As essential as timeliness is, no ASIC vendor or designer is willing to trade the accuracy with which cell models are characterized for a greater degree of automation. ■

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DESIGN AND DEVELOPMENT TOOLS

Innovative designs mean lower costs for ATE systems

Mike Donlin, Senior Editor

ASIC verification and test equipment vendors are facing some tough challenges these days. They're being told by ASIC designers that they must produce test systems that will keep up with the increasing gate counts, speeds and pin counts of the latest devices, but that they must deliver this performance at lower costs.

Design engineers have long been frustrated by the amount of ASIC verification and test capabilities that they could afford. They've had to choose between test systems that were inadequate for their designs, or else commit hundreds of thousands or millions of dollars to systems that might be obsolete before they were even paid for.

Automatic test equipment (ATE) and device verification vendors have answered these complaints with systems that promise performance at lower—or at least not spiraling—prices. Though today's systems sport price tags ranging from less than \$50,000 to more than \$3 million, they all have one thing in common—they use innovative technologies to deliver the needed price/performance.

"We've gotten a clear message from the semiconductor industry that they want to hold us to the same price/performance curve that they have to live with," says Wayne Ponik, VLSI product manager at Teradyne (Agoura Hills, CA). "They produce a new generation of devices every three to five years that doubles the performance of the previous generation, and after a time, when volume production and competition set in, the price is about equal to what it was before. They've let us know that they need testers that follow these same guidelines."

■ Balancing price/performance

Teradyne's answer to this dilemma is the recently unveiled J971 series of VLSI test systems. The series provides testing capabilities for devices with up to 512 pins at about half the cost of Teradyne's previous

generation of test equipment. The key to balancing this price/performance equation lies in a proprietary technology that Teradyne has dubbed E/MOS—a system-level combination of ECL and CMOS technologies—that implements 90

percent of the timing and formatting circuitry in low-cost CMOS while providing the performance of ECL. "We've known for some time that the key to lowering price was to incorporate more CMOS in the tester," says Ponik, "but CMOS sacrifices accuracy because edge placement varies with the frequency of the device being tested, and you get timing errors. We've found a way to sur-

round the CMOS, if you will, so that it has ECL coming in and ECL going out to keep the system accurate. Doing this allows us to cut the cost of each channel by half, so we've ended up with a 200-MHz tester that is about half the price of our 50-MHz system."

Though not every ATE vendor can claim the dramatic price/performance improvement that Teradyne has achieved, the message from the ASIC industry is clear—equipment costs translate directly into develop-



Teradyne's J971 series of VLSI testers uses a combination of proprietary E/MOS technology and plug-in hardware upgrades called performance cells to cut costs by about half over the previous generation of test equipment. An interactive graphics software package streamlines the process of developing test programs by separating test parameters and test data definitions from the creation of program code.

round the CMOS, if you will, so that it has ECL coming in and ECL going out to keep the system accurate. Doing this allows us to cut the cost of each channel by half, so we've ended up with a 200-MHz tester that is about half the price of our 50-MHz system."

ment costs—and other high-end tester manufacturers are responding in kind. Schlumberger Technologies (San Jose, CA) has recently rolled out its ITS 9000 test family, which costs a hefty \$1.8 to \$4.8 million but boasts a reduction in program generation time by an order of magnitude. This capability translates directly into increased productivity and decreased time-to-

DESIGN AND DEVELOPMENT TOOLS

market, the company says.

"We can't claim the lowest price right now because of the high cost of developing the system," says Nadim Ahmad, product marketing manager at Schlumberger. "We expect that to come down in time, but the most important aspects of our system are its multifunctionality and programming speed, which can translate into an enhanced return on a customer's investment. We've accomplished these capabilities with our new sequencer-per-pin (SPP) architecture, based on proprietary ASIC technology, that allows a true replication of the simulator environment on the tester. This lets you take the output from any industry-standard simulator and map it directly on the tester. The tester architecture mimics the simulator's output so it becomes a hardware extension of the simulator."

■ Break from tradition

The ITS 9000 is a break from traditional ATE designs that used either a shared-resource approach or a test generator-per-pin design. In the case of the shared-resource systems, a number of timing resources were multiplexed to the tester-pin electronics via switching matrices, while the test generator-per-pin systems provided an independent timing generator for every pin.

"Both architectures have drawbacks," Ahmad points out. "The shared-resource approach forces you to rob resources from one pin to benefit another. The test generator-per-pin was definitely an improvement because it provided the flexibility of different formats but still limited the number of transactions per pin to three or four. Our SPP design defines timing in terms of events occurring at precisely calibrated times. Each tester pin in this architecture can store up to 192 events per test sequence and generate sequences of events of any length in one tester period."

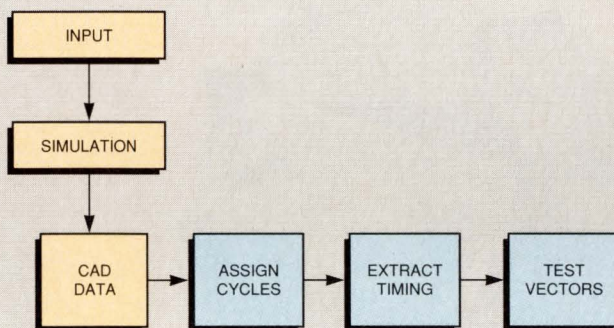
Schlumberger's SPP architecture is coupled with its advanced symbolic ATE programming (ASAP) software, an icon-driven environment that uses interactive windows to create, test, debug and modify test programs in real time without the need to recompile. Device test

programs are written with a mouse and test icons, which are each stand-alone and usable in any order. The C program created by ASAP is invisible to the user unless it's needed for the creation of customized icons. The interaction between SPP and ASAP affects the simulation-to-test integration and reduces program development time.

192 and 512 pins, respectively. The benchtop systems, which boast a \$300-per-pin price tag, feature programmable timing generators with 500-ps resolution and per-pin programmability.

"To get the price down, we did two things," says Bjorn Dahlberg, president of Hilevel. "We eliminated 80 percent of the ECL components and

SEQUENCER-PER-PIN ARCHITECTURE



The ITS 9000 component test family from Schlumberger is based on a sequencer-per-pin architecture that allows a true replication of a simulator environment on the tester. It provides a direct path from simulation output to test vector generation.

"This approach relieves an engineer of having to write a lot of code," Ahmad says. "Test throughput is two to three times better, and test development time is cut in half."

All the attention given to reducing price and increasing performance isn't concentrated just on the high-end ATE systems. In the under-\$100,000 category, manufacturers

only paid a 50 percent penalty in performance. Of course, we had to keep some essential ECL, but by using mostly CMOS we reduced the price by 50 percent compared with the ETS 7000, the top of our benchtop unit line. We also removed the programmable drivers from the system. They're expensive, and many of our customers only need to analyze timing. They don't need to test the levels of the signals."

■ Targeting low-end needs

Hilevel's decision to offer a lower-performance system was based on a large segment of applications that simply don't need testing capabilities above 50 MHz. "There are a lot of devices out there with clock speeds of only 33 MHz or so, and the chip certainly won't be running instructions at that rate," says Dahlberg. "We offer a 50-MHz clock to feed the device under test, which usually has a data rate that's only one-fourth or one-half of the clock rate."

Meeting the needs of ASIC vendors who might not require all of the high speed and throughput of the most-expensive verification systems is also the strategy adopted by Integrated Measurement Systems

"We've known for some time that the key to lowering price was to incorporate more CMOS in the tester."

—Wayne Ponik, Teradyne



are looking for ways to offer more functions at lower costs. Hilevel Technology (Irvine, CA), for instance, is complementing the Topaz V, its top-of-the-line ASIC verification system, with the ETS 200 and 270 systems, which offer a 50-MHz clock rate to test devices with up to

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(Beaverton, OR). Its Logic Master XL series is aimed at ASIC manufacturers who need to test devices with clock rates from 60 to 100 MHz, but who don't need the high-volume capabilities of the multimillion-dollar systems.

"Small-volume ASIC vendors are demanding a lower-priced tester," says Steve Morris, director of marketing at IMS. "Paying \$3 million for a tester makes sense if you're going to test millions of parts, but median production volumes of

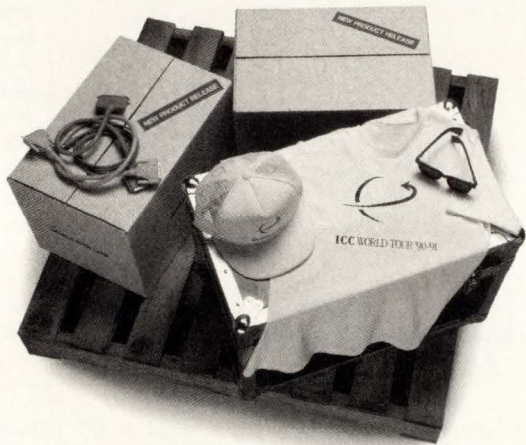
ASICs are plummeting, and that's causing people to look hard at the cost per device."

Testing challenges

ASICs do, however, present some unique test challenges. First of all, since the ASIC design is owned by the designer and not necessarily the ASIC fab, the fab can't guarantee the device's fitness for a customer's application. As a result, the designer must take responsibility for verification of the device. After the prototype has been verified, ASIC production must then be monitored to ensure that the vagaries of the semiconductor process don't adversely affect a critical feature of the finished product. These needs demand tester accuracy, but low-volume production often doesn't justify a high-priced system.

"Our price is anywhere from one-fifth to one-tenth of a high-end system," Morris says, "and you pay for that in throughput. But while a large system may take months to program and set up before the high-volume testing starts, ours takes only days. A user could then use the months saved to test maybe two years of an ASIC's production volume."

So the challenge for tester vendors is to meet the sophisticated demands and shrinking budgets of ASIC designers. There will probably always be a demand for full-featured, high-ticket ATE systems. But as low-volume ASICs gain a larger foothold in systems, and competition drives down device costs, verification and test equipment manufacturers will need to draw on design expertise and hard assessment of industry needs to survive.



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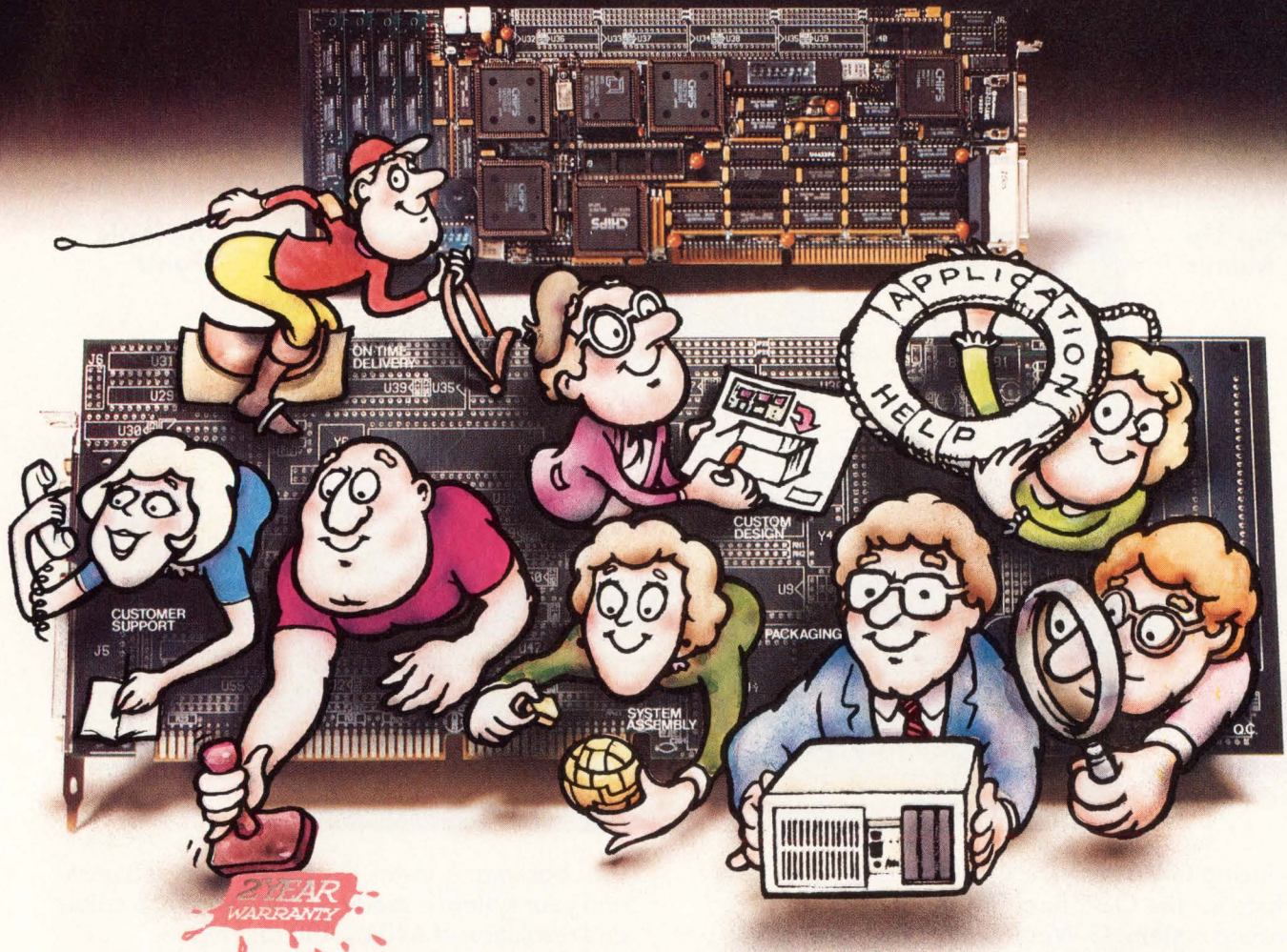
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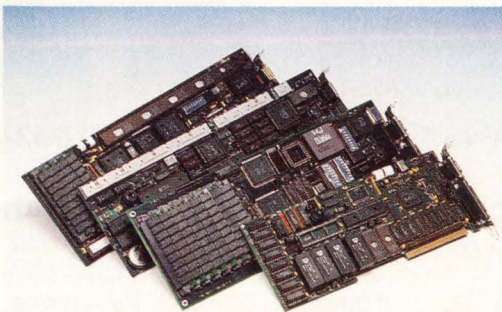
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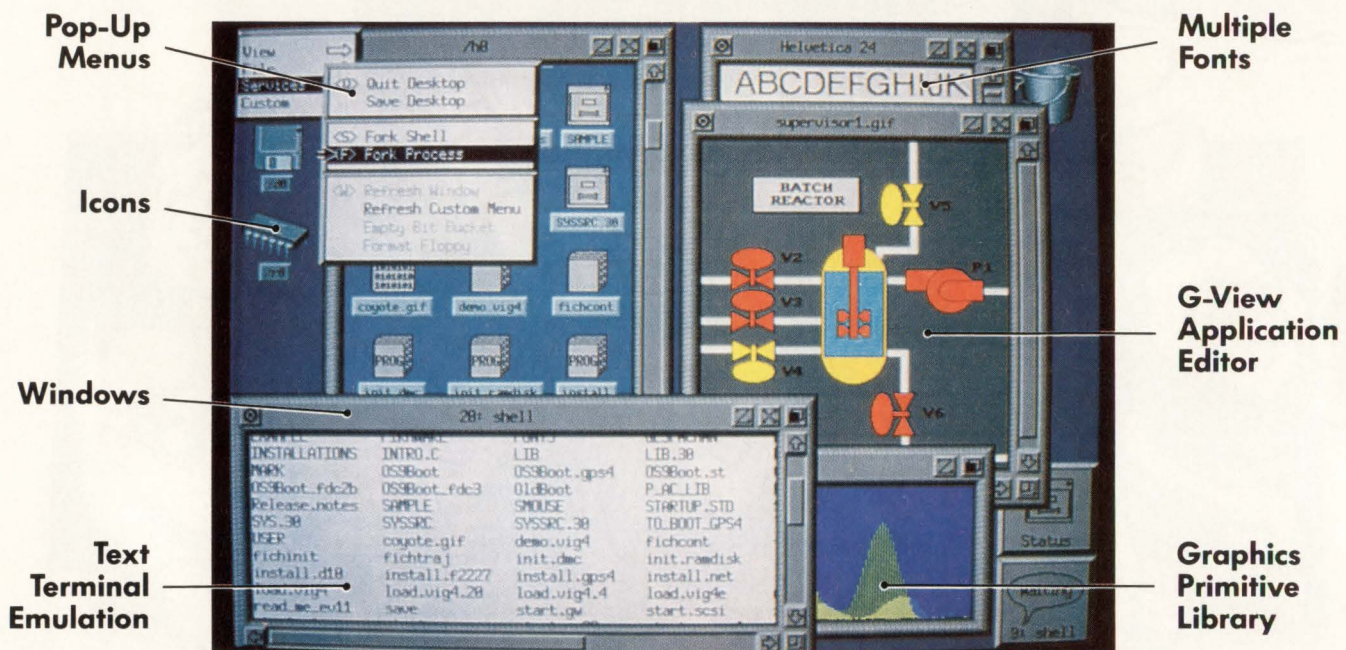
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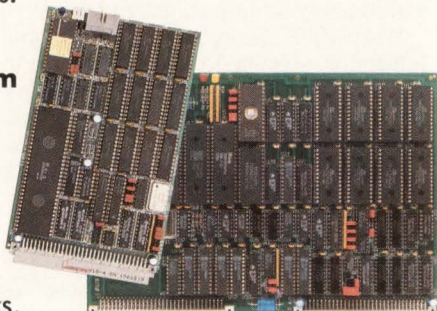
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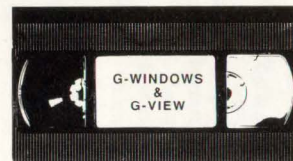
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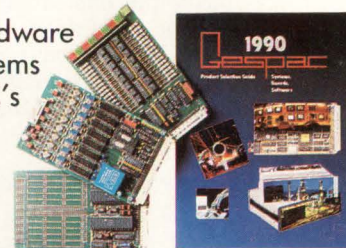
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CIRCLE NO. 32

Design entry tools evolve to meet future needs

EDA vendors are developing design entry tools that meet the demands of complex systems without forcing engineers into radical reeducation programs.

Mike Donlin
Senior Editor

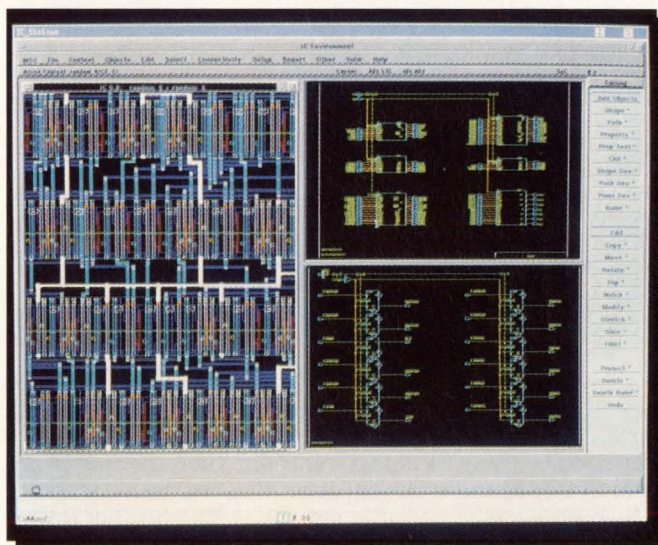
The growing complexity of today's systems, at the chip and board level, as well as the ever-spiralling gate count of today's ASICs are forcing engineers from the comfort zone of schematic capture into alternative design capture techniques such as hardware description languages (HDLs). The transition from a purely graphical representation of a design into the hierarchical or behavioral descriptions of an HDL isn't an easy one, particularly for engineers used to thinking in schematic terms.

"In the mid 1970s, designers worked with X-Acto knives to lay out designs," says Bob Smith, director of marketing at Synopsys (Mountain View, CA). "It was a very physical way of approaching a project. The '80s saw a transition to using the power of a computer to capture the schematic, but the process was still very visual. Now ASIC vendors are pushing the envelope. If it takes 15 months to design a 15,000-gate ASIC, how long will it take to design a 1 million-gate device? People have to think about architectures now, and write programs. It's a major change in how an engineer approaches a design."

This need for higher levels of abstraction in complex designs is presenting challenges for CAE tool vendors, who must provide transitional entry techniques that will bridge the gap between HDLs and traditional schematic capture methods. First of all, schematic capture is far from dead. For the foreseeable future, there will be a need for graphical representations of the components of complex ASICs and circuit boards, not only because users still need the graphical depiction of a circuit but because they need such representations for documentation, simulation and manufacturing purposes.

"It's easier to design some functions with pictures," says Bruce Rodgers, division marketing manager at Data I/O (Redmond, WA). "If someone's creating a unique symbol for a microcontroller or memory device, for instance, there's no reason to describe the function in behavioral terms—it would take forever. But if you have a standard function such as a counter, it's probably harder to draw than it is to write two or three equations to describe what's going to happen to data when it hits that part of the circuit."

To answer these different but interrelated sets of demands, tool vendors are scurrying to provide design environments that will allow seamless migration between the different worlds of schematic capture and HDLs. Currently, several vendors offer toolsets that let designers choose from a palette of entry techniques such as waveforms, state machine and Boolean equations, as well



Mentor Graphics' Design Architect lets users cross-correlate between the logical/circuit view of a device and other design views such as simulation, layout and mechanical packaging. It's possible to select the schematic view of a circuit, for example, and have the corresponding layout highlighted.

DESIGN ENTRY TOOLS



"Designers using today's top-down design approaches still need to see good, clear drawings," says Dick Albright (left), director of CAE product marketing at Valid Logic Systems. "And, even with the revolution in design methodologies, it's still necessary to produce schematics for manufacture and test."

components that make up a design.

"We believe that design capture has to be more than just logic capture and entering gates," says Bill Hostmann, product manager in the design and synthesis division at Mentor. "It must encompass a behavioral as well as the typical gate and logic aspects. Our customers are telling us that they're spending one-third of a product's development time in capturing the design specification. The best way we can help reduce that time is to let them specify a design, capture it at a high level and move down from a behavioral to a logical description."

Mentor's toolset supports multiple-window editing, allowing users to have several schematic, symbol or VHDL editing windows open at any given time. Because Design Architect integrates both VHDL and schematic editors, a designer can call upon several levels of model abstractions. If a VHDL model contains a component defined by a schematic-based model, for instance, a user can select the VHDL component and then traverse to its underlying schematic model. If a schematic model contains a component defined by a VHDL model, the user can traverse through the component's symbol to its underlying VHDL description.

Capabilities such as these not only give designers multiple ways of visualizing and entering a design, they also serve as teaching tools for engineers who haven't used an HDL and need to see the relationship between the HDL code and the corresponding schematic. "It's hard to get a designer who's used to connecting gates to sit down and write code,"

as schematic capture and HDLs. But while users can choose a method that best suits the device under consideration or their own preferences, a completely seamless integration of all techniques isn't possible yet.

"Ideally a person could make a change in one mode and see the result in another," says Scott Sandler, product marketing manager in the advanced CAE division at Cadence Design Systems (San Jose, CA). "But the range of operations and abstractions among the different entry methods makes it difficult to come up with a data model that would allow instant communication from one technique to another. There have been different data mod-

els built on various database techniques in the past, but they haven't proven effective. Right now, no one has the necessary software tools, but we're working hard to achieve this level of integration."

■ A multiple-window approach

For now, about the best a designer can hope for is the capability to edit specific portions of a circuit or board in the appropriate format and move to an alternate entry technique as needs dictate. The Design Architect from Mentor Graphics (Beaverton, OR) was one of the first design entry environments that let an engineer create and edit the mixture of VHDL, architectural and schematic

The power of the PC

If hardware description languages (HDLs) are ever to make inroads into board design tools, they will have to win over not only workstation-based but personal computer-based seats as well. Packages such as SDT III from OrCAD (Hillsboro, OR) offer sophisticated design tools that run on PCs having as little as 640 kbytes of memory. Performance is, of course, limited on a basic PC, but the ability to produce a design from schematic capture through simulation to board layout without the larger investment of a workstation has won many converts.

The OrCAD tool, for instance, can perform board layout with autorouting for boards up to 32x32 in., and can accommodate up to 10,000 segments and 16 circuit layers. Some PC-based tool vendors, such as Cadam (Burbank, CA), have ported their tools to workstations, but the reason is usually not for increased performance but rather to offer products that will work in a typical multisystem environment. As a matter of fact, PC tools seem to be able to hold their own, particularly in schematic capture and layout applications.

"I've always contended that there's

no significant hardware advantage between comparably priced PCs and workstations," says John Durbetaki, CEO at OrCAD. "Performance depends on the application.

"We've had some benchmarks presented to us by workstation vendors, and we've only seen a difference of 3 or 4 Mips when comparing a Sparc, a 68040 and a 486-based system. My contention is that the majority of the performance difference is in the compiler. A good compiler on a slower machine is still able to outperform a mediocre compiler on a fast one."

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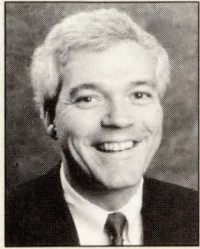
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CIRCLE NO. 33

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Removing barriers to automation



While the concept of alternate forms of design entry isn't new to the EDA world, the lack of alternate forms of entry remains a major impediment to market accep-

tance of design automation tools.

Design automation tools such as those for synthesis have focused on optimization and implementation efficiency. These tools are useful if the designer is willing to conform to the vendor's design entry form. To get maximum productivity from designers, however, CAE tools must provide users with the entry form that best fits the design and the designer. Put another way, the right entry form is the one that the user is familiar with, or that offers the format best suited to the design.

In a broad sense, alternate forms of entry have been around for many years. The first of these were tools for hand-crafted netlists, digitized schematics and schematic capture. These tools held fast for about a decade with little change. Then VHDL entered to lead the second wave of alternate forms of entry. While VHDL is a powerful tool, it again forces the hardware designer to learn an unfamiliar entry form and think like a software engineer.

Another generation of alternate forms of entry is needed—one that allows designers to operate in a familiar environment, gives them the fastest entry of their designs and allows access to analysis tools and advanced enabling technologies—such as synthesis. Integration into a CAE environment is a critical factor for this to happen.

Design entry: the next step

The tools described below are some of the alternate forms of entry necessary for today's designer, and they can be grouped into tools that take existing user files as input and tools that take input directly from the user. The former will translate those files into a format that can be both simulated and synthesized. The latter will let the user specify, graphically or with text, a function or set of functions. The tools will gener-

ate both a model and a symbol.

A bubble-diagram entry tool is geared toward state-machine development. This graphical tool will let the user define the functionality of state machines by drawing a diagram indicating the states and the transition paths between states. The capture will be augmented by special error checking and give the user the option of automatically generating a VHDL model for simulation and synthesis.

Truth-table tools will feature special editors for the entry of truth tables and the importation of text files that represent truth tables. The tools will offer the

To get maximum productivity from designers, CAE tools must provide users with the entry form that best fits the design and the designer.



FIFOs, flip-flop registers, latch registers, memories, multipliers, and other standard logic. The user can connect these components with buses and assign widths to the buses. The system can then be compiled for simulation.

Translational tools will enable the user to translate Abel, Cpl, Palasm and other languages directly into the CAE system. This lets the designer reuse existing programmable device libraries with synthesis tools to generate ASICs. The user can also write new descriptions of the system in Abel, Cpl or Palasm and generate VHDL that can be simulated and synthesized.

Although there are many other forms of entry, such as Boolean equations and waveforms, the key to a good entry tool is designer productivity. And the key to optimal performance is alternate forms of entry that let users design in a familiar manner while leveraging advanced enabling technologies in a transparent manner—thus removing the barrier to automation.

says Larry Ciaccia, section head of DSP product development at Harris Semiconductor (Melbourne, FL). "But the people coming out of school today have more computer experience than engineers did in the past and the industry is moving toward HDLs for complex circuits, so we're starting extensive VHDL training. The trick is to bring our experienced engineers up to speed without spending too much time doing it."

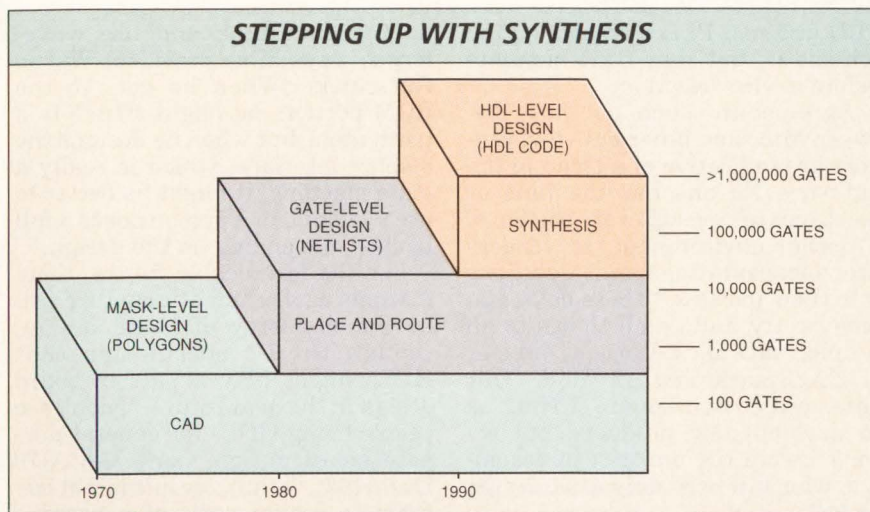
To help engineers inexperienced in HDLs, tool vendors are offering features that let users compare language descriptions with corresponding schematic elements. "Our utilities take an HDL description, parse it and automatically draw a symbol with the correct pin names assigned," says Bob Broady, marketing manager for design and data entry at Cadence. "A user can then place that element in a schematic and wire it up."

With all of the interaction between schematic capture tools and HDLs, it would seem that the transition between one and the other would be simple. There is, however, a problem. "There isn't always a one-to-one relationship between the VHDL code and the schematic," explains Broady. "Just because you change something in the HDL doesn't necessarily dictate a change in the schematic. Our tools do provide warnings, however, when a change has occurred in the HDL that would necessitate a change in the schematic, so users can decide whether to keep the change and regenerate the schematic."

The very nature of an HDL, then, precludes it from having each line of code relate directly to a component in a schematic. But the value of an HDL's broad-based architectural descriptions is important in bridging the gap between concept and component. "We're building on tools of the past," says Mark Milligan, application engineer at Teradyne (Boston, MA). "Just as schematic capture was born because typing netlists was time consuming, HDLs are becoming popular because designs are too complex to capture every component. We've expanded schematic capture to include block diagrams for functional modules, and then we use VHDL to describe the behavior of these modules. That way we can look at the diagram and understand how a system is connected up."

The struggle to entice reluctant engineers to use HDLs might have

Ray McCann, BSEE, marketing manager, Viewlogic Systems



As gate counts increased over the last 20 years, design entry techniques kept pace with mask-level, gate-level and HDL-level tools. The enabling technologies of CAD, automatic placement and routing and, most recently, synthesis will keep these techniques effective as designs reach over 1 million gates by the mid 1990s.

continued a lot longer if it weren't for the introduction of synthesis tools that took high-level descriptions and translated them down to gate-level entities. "The enabling technology here is synthesis," says Synopsys' Smith. "Large ASIC companies have had their HDLs in the past, but there was a disconnect between the global design and the physical layout, a manual translation if you will. With synthesis, a

user can think about a design, enter it in VHDL and let the computer do the work. Correct-by-construction is no longer guesswork, it's just a mapping into a logic-level netlist."

The need for a variety of entry tools isn't limited only to full-custom ASIC design—there are other areas, notably programmable logic device design, where a full palette of tools is essential. The most popular packages let users define logic in tradi-

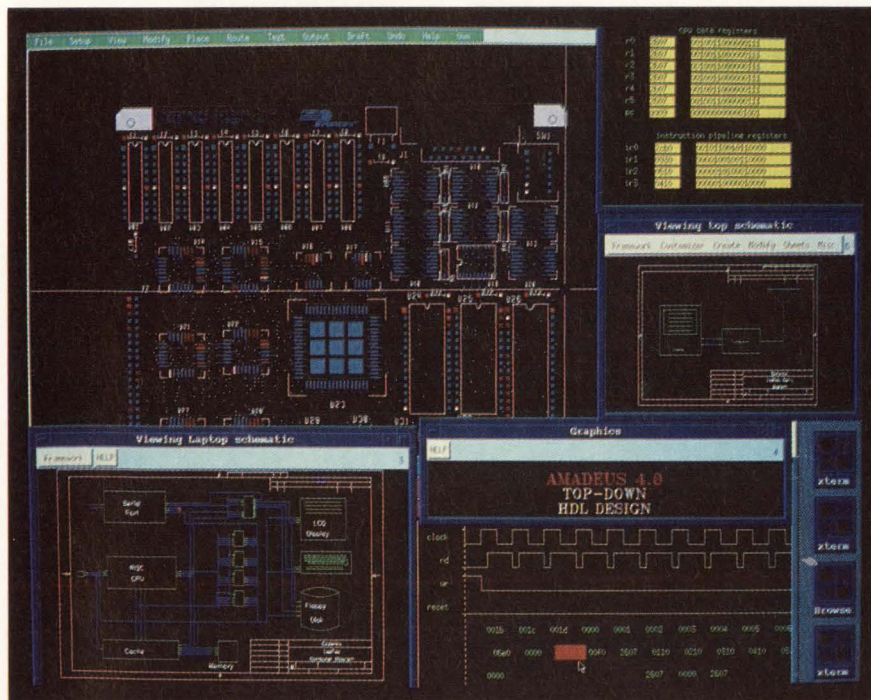
tional ways, such as Boolean equations and truth tables, as well as in higher-level languages. "It's necessary to offer different levels of PLD design," says John Durbetaki, CEO at OrCAD (Hillsboro, OR). "In PLDs, for instance, you can only do so much with Boolean equations before you need to synthesize from abstract equations."

In addition to offering several ways to enter a design, depending on application and user expertise, the latest tools also allow users to complete a major portion of a design without specifying the actual device. "A lot of times, when people start a PLD design, they're not sure of the device that they'll end up with," says Ray McCann, marketing manager of synthesis products at Viewlogic Systems (Marlborough, MA). "Most designers have a general idea—that the final product will be in 1- μ m CMOS, maybe—but device independence lets designers hold off on the particulars until their needs are more completely fleshed out."

Ties with PLD tool vendors

Because of the increasing demand for programmable logic-based designs, several EDA vendors have entered into agreements with PLD tool companies rather than spend time and resources on proprietary tools. Valid Logic Systems (San Jose, CA), for instance, has just introduced System PLD and System PGA, two products that incorporate Minc's logic synthesis tools with Valid's schematic capture and simulation tools. With the Minc (Colorado Springs, CO) tools, users can enter designs as waveform descriptions, truth tables, state-machine syntax and Boolean equations. Like other popular programmable logic tools, the Valid/Minc tools enter the logic portion of a design, and then the user can work with the tools' automatic device selection and partitioning capabilities.

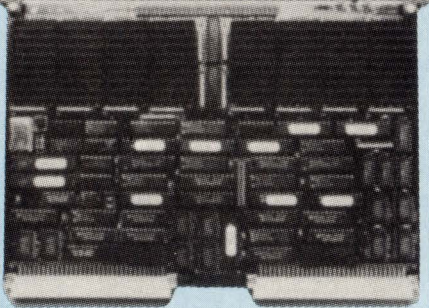
Valid isn't the only vendor that has incorporated the Minc tools into its environment, however. Mentor, Teradyne, Racal-Redac (Mahwah, NJ) and Intergraph (Huntsville, AL) all resell Minc's PLDesigner. But Valid offers several unique features, such as the ability to mix PLD and non-PLD logic on the same schematic. According to Valid, other EDA systems need to create a separate schematic for the PLD logic. Users of Mentor's PLDSynthesis (Mentor's version of the Minc tool) can mix



CAD frameworks have allowed EDA vendors to port information across different design entry techniques and display it via multiple windows. Cadence Design Systems' Amadeus Design Series, based on Design Framework II, supports multiple processes from system definition, design entry and analysis to board layout.

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CICRLE NO. 34

DESIGN ENTRY TOOLS

PLD and non-PLD elements on the schematic, but they can't simulate before device selection.

Agreements such as those between Minc and other EDA tool vendors are indicative of a trend in the industry. No one has the time or resources to develop every portion of a design environment, so vendors are encapsulating point solutions into their toolsets. "These days, you have to try and be all things to all people," says Dick Albright, director of CAE marketing at Valid. "Our advanced customers are driving us to develop new products, but we can't ignore the majority of designers, who still need only basic design tools."

Boards present problems

While HDLs have certainly found their place in complex ASIC and PLD designs, they don't translate so easily into the world of printed circuit boards. And though there's no reason why a board's description can't be made with the broad architectural brushstrokes of an HDL, board designs don't lend themselves to the total top-down approach that can often be used for ASIC designs.

"First of all, HDLs don't work well with standard parts," says Teradyne's Milligan. "With boards you start out with givens, such as a certain kind of microprocessor, interfaces and even some ASICs. So a mixed-level design such as a board calls for a mixture of tools. Board design is a top-down process with bottom-up constraints."

While some tool vendors claim that HDLs will eventually have a larger role in designing boards and whole systems, schematic capture is still the principal method for entering designs. This is partially because of the limitations of HDLs and the user expertise behind them, but is also a result of the limitations of today's synthesis tools. "Synthesis isn't mature enough across all technologies to take a high-level design and produce a schematic for a board," says Cadence's Broady. "Besides, when it's time to produce the board, you need a schematic, so I can't see a 100 percent text-only world."

Because of the mixed technologies that reside on a board, some designers use a mix of waveforms, truth tables, an HDL and a schematic entry tool to design a board. "If a designer has a board that uses a 68000, for instance, he might open

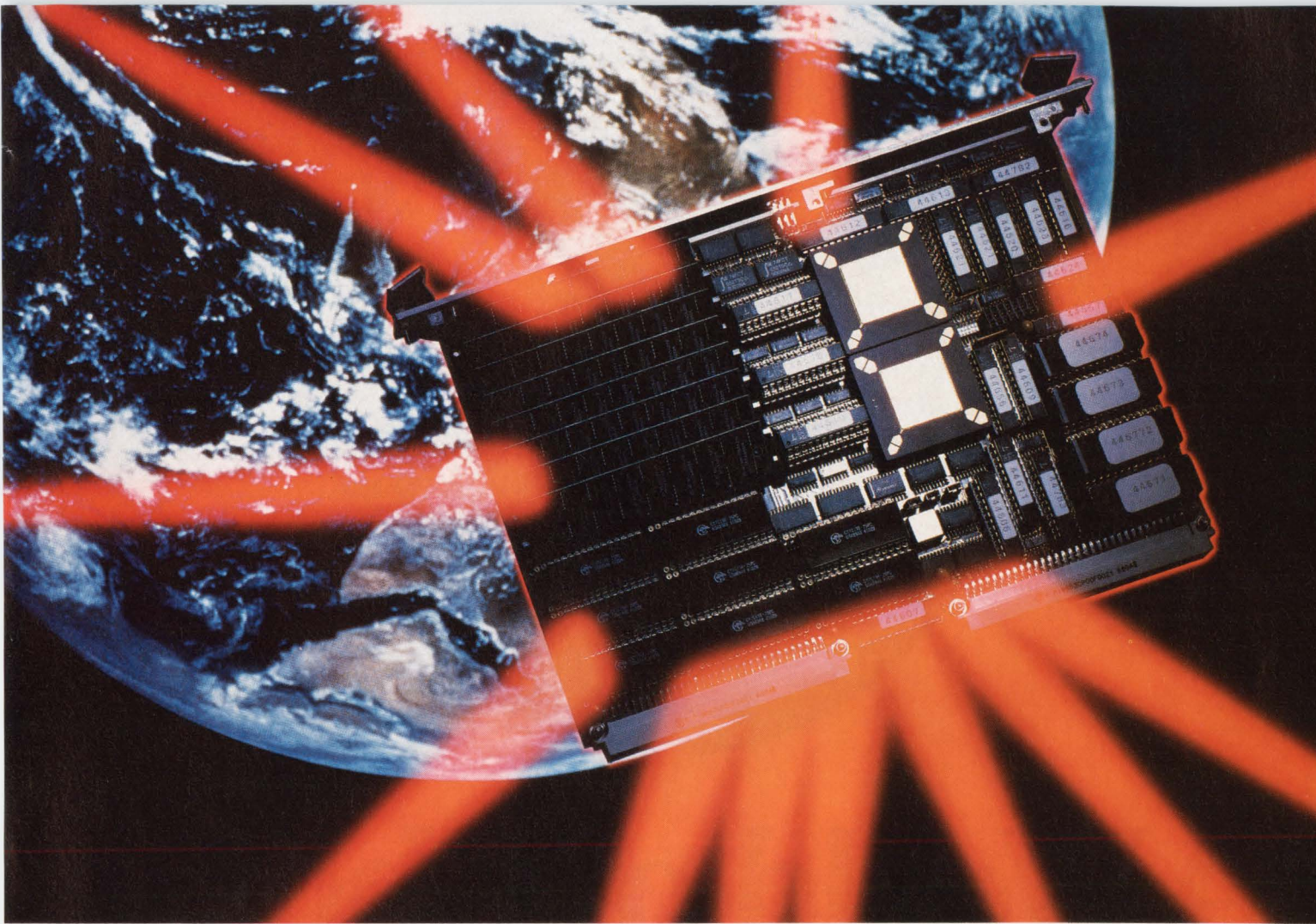
up the data book and use waveforms," says Minc president Wayne Gutschick. "When he gets to the ROM portion, he might switch to a truth table, but when he designs the display interface, which is really a state machine, it might be better to use a language. A person needs a full toolbox, depending on the design."

For the foreseeable future, then, it seems as if schematic capture will be the mainstay of board design, though there's speculation that HDLs might play a part in board design in the near future. "I don't see people using HDLs for general-purpose board design," says OrCAD's Durbetaki. "I think people might use them to design parts of a board—such as a RAM array—but I don't think HDLs will replace schematic capture for some time, if ever."

The challenge, then, is for tool vendors to produce products that will bridge the gap between the most basic entry tools and the most advanced. "There used to be two camps," says Cadence's Broady. "A PC-based board-level designer would say 'Simulation will never work—I just need to enter my design.' The other camp would say that they would never dip their hands in the muddy waters of schematics: 'I'm a pure HDL text person.' Both camps are realizing that they need the other to succeed." ■

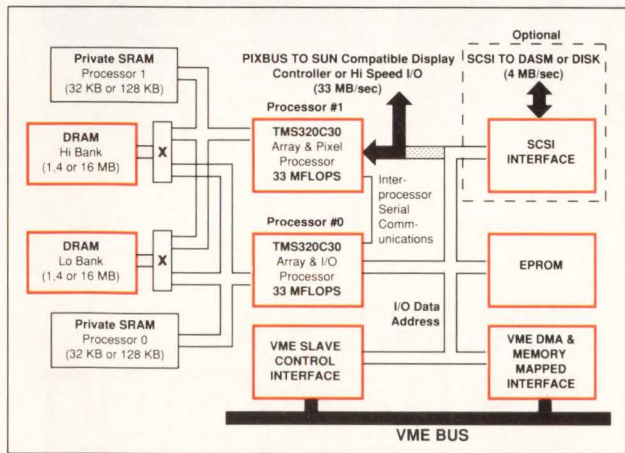
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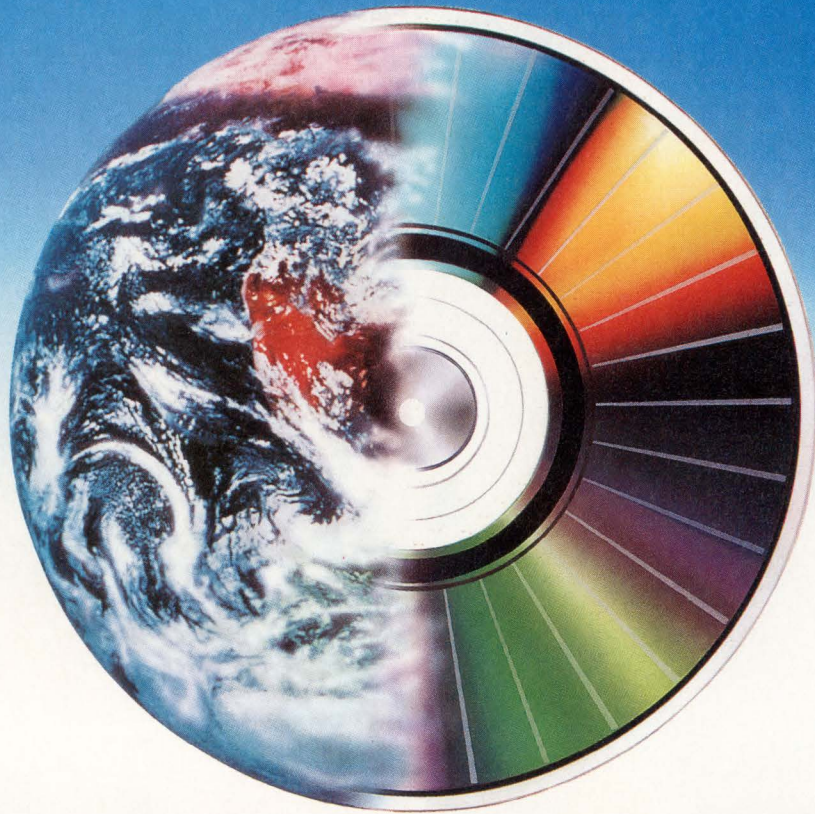
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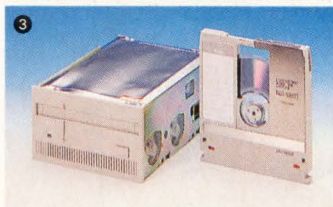
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CIRCLE NO. 37

DRAM vendors address increasing specialization

Although vanilla parts still make up most shipments, wide-word, high-speed, low-power and application-specific DRAMs are a growing force in memory systems design.

Ron Wilson
Senior Editor

Everybody knows there's only one important trend in DRAM technology: every few years they get bigger. But lately, the gradual murmur of feature innovation—the force that gave us fast page-mode and video RAM (VRAM)—has grown to a roar. Suddenly we get to choose word widths from 1 to 18 bits, speeds from 80 to 55 ns and features from the essential to the unfathomable. Driven by competitive pressures, technology shifts and real customer feedback, the DRAM vendors are working overtime to bring out new products.

It might be natural to assume that the beneficiaries of all this innovation will be the people who use enormous quantities of the parts: mainframe computer and image-processing vendors. But in fact, these architects are likely to stay with the most vanilla—that is, cheapest—parts, while the real impact of feature explosion will be on embedded systems, midrange personal computers, palmtops and consumer electronics. To see why, we have to look individually at the major trends in specialty DRAM design.

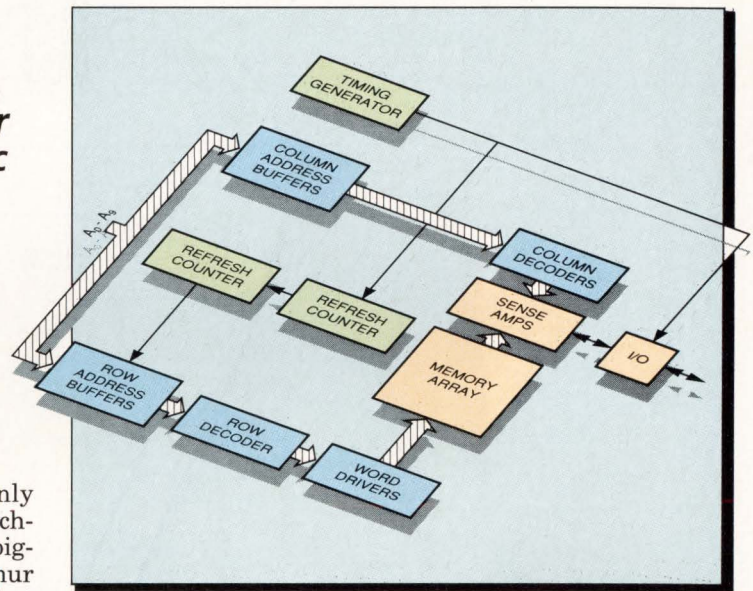
"The biggest change taking place in the DRAM business right now is in chip organization," says Avo Kanadjian, marketing manager at Toshiba (Irvine, CA). "We introduced the 64k×16 part, and at 4 Mbits we're planning a full line of ×8, ×9, ×16 and ×18 devices."

■ Finally, wide RAMs

Toshiba isn't alone; anyone who intends to stay in the DRAM mainstream is rushing to develop wide-word parts because the new organizations meet two critical needs of system designers: modularity and bandwidth.

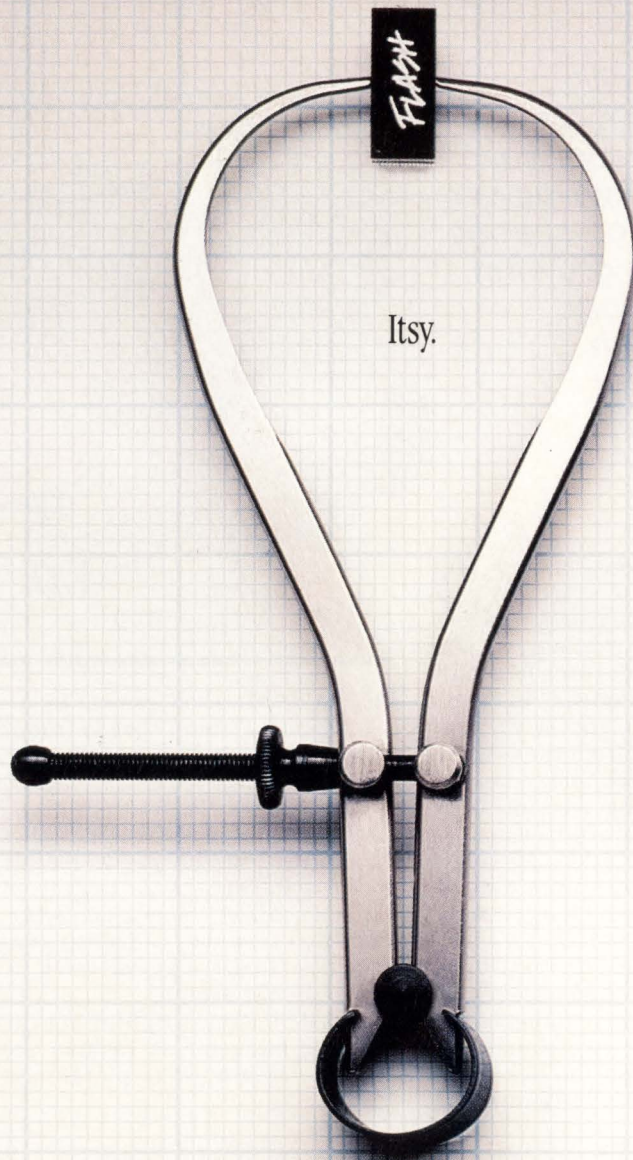
The modularity issue arises because modern DRAMs have so much capacity. With 4M×1 chips, the smallest 32-bit memory bank you can assemble will need 32 chips and hold 16 Mbytes. That's just great if you're building a file server, but it's useless in the midrange PC market. "Many applications can't use very deep memories," Kanadjian says. "The PC people like to work in 1-Mbyte increments, and graphics applications are more comfortable with 256k."

Conversely, designers of fast workstations and signal-processing systems prefer the wider parts for speed. If you're using 64k×16 parts, for instance, you can arrange 1 Mword of memory as 16 parallel banks and get impressive bandwidth out of standard-speed devices.



The internal structure of a standard DRAM is rife with possibilities for specialization. Most modern parts produce a full row of data in one access, and then throw away all but one bit. And most parts now have a distinctly under-utilized refresh counter on board. Vendors are exploiting these resources to make high-margin specialties.

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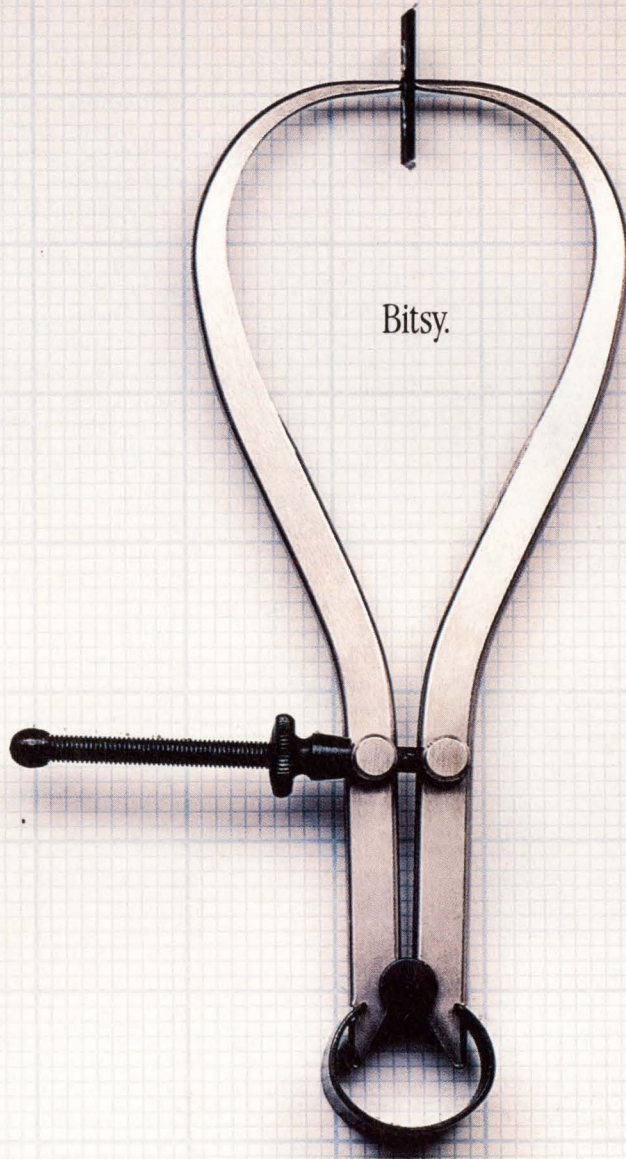
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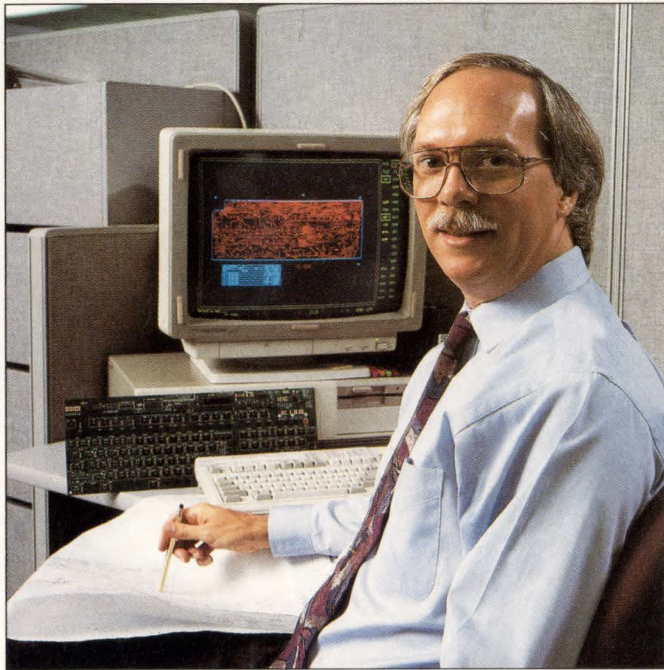
But the advantages of wide-word DRAMs haven't come without costs, for both chip vendors and customers. The fundamental problem with the parts is noise. "In wide DRAMs, you have the same ground issues you find in fast SRAMs," says Kendall Pope, strategic program manager for memory and mass storage at Hitachi (Brisbane, CA). "When all those output drivers switch together, you have to do things to keep the substrate quiet and protect your data."

Jeff Mailloux, specialty DRAMs group manager at Micron Technology (Boise, ID), adds, "On our $\times 16$ parts, we've gone to a supply and a ground pin for every eight I/O pins. We use lighter drive and lower edge

trically just like their $\times 1s$ and $\times 4s$, in practice the user sometimes has to help out with timing and noise-control issues at the board level.

One obvious place for a wide-word DRAM is within the confines of a notebook or a palmtop computer, where 4-Mbit parts might achieve a one-chip main memory. Next to space, the most critical resource in these little machines is power. That fact has created a whole new specialty in DRAMs: low-power parts.

So far, low power has meant extended refresh time. The big issue in DRAM power consumption isn't the active power, but the standby power—the current that eats away at your battery while the machine is in sleep mode. And this current is



NMB Technologies has made a specialty of very fast DRAMs. David Snyder, director of market development, says that the NMB designers achieve high performance not by major architectural changes but by careful design and tuning of every detail in the part and the process.

rates, and we stagger the edges during simultaneous switching. These are the same sorts of techniques we've been shipping in our $\times 16$ SRAM products, and we know they solve the problems."

Solving problems for the chip designer, though, doesn't necessarily translate into solving problems for the system designer. All of those noise-control measures can subtly change the output characteristics of the DRAM. And wider parts organized into multiple banks usually mean more load on the address line drivers. These factors combine to become an issue in larger systems. One vendor applications engineer suggests that, while all suppliers want to make their wide parts elec-

due almost entirely to refresh cycles. So if you can stretch out refresh cycles, you can reduce power drain.

Today, vendors accomplish longer refresh times by selecting parts from their standard DRAM lines. "It's not a matter of a unique low-power design," says Hitachi's Pope. "Refresh time is purely a process issue—a function of the oxide quality, mainly. We put a huge guard band around our spec for the standard parts, and that yields us devices with extended refresh times."

Selecting standard parts for extended refresh has a number of advantages, including the fact that low-power parts are automatically available in all common DRAM configurations. But as system designers

grow even stingier about DRAM current, vendors are talking about designing a low-power part from the ground up. Some vendor engineers suggest a systematic attack on power consumption at the chip level.

Such a new design would take into account the special operating modes on battery-operated computers, especially standby. During standby, high-current devices such as the back-bias pump and internal voltage reference could be slowed or shut down, and refresh cycles could be staggered so that all the cell arrays on a $\times 16$ die wouldn't draw current at once. Such efforts would not only reduce instantaneous current demands, but they would also reduce electrical disturbances on the die, probably lengthening the allowable refresh interval. The sum of all these changes would be to reduce standby current from the 200 or 300 μA common today to possibly 100 μA in active standby.

The final assault on power consumption, though, will come through more drastic measures. "Future low-power designs are likely to use 3.3 V," says Earnest Powell, systems marketing manager at Texas Instruments (Houston, TX).

Bharat Gupte, standard products marketing manager at Oki Semiconductor (Sunnyvale, CA), agrees. "We need to move to lower operating voltages for two reasons: to reduce power consumption in portable equipment, and to get smaller geometries to work at all. I think we'll probably see 16-Mbit parts that use 3.3 V internally but still have a 5-V interface," Gupte continues. "By the 64-Mbit generation, we'll be using pure 3.3-V parts. These things aren't so necessary for laptop or notebook computers but for things that are coming. For instance, I know of a palmtop television with a built-in mini-laser-disk player that's in design right now."

■ Accent on speed

While some vendors contemplate new DRAM mask sets to optimize refresh time, others are doing variant designs for almost the opposite reason—speed. Oddly, the demand for high-speed DRAMs comes not from high-end, super-speed RISC workstations but from midrange personal computing machines.

The explanation for this is economics. High-end CPUs are already

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A dissenting view on features

While many DRAM vendors scramble with unbound enthusiasm to come up with yet another ingenious feature for their parts, most will admit that even the best features are under-utilized in the market. In fact, there seems to be something of a backlash developing among the biggest DRAM customers.

Nowhere is this trend—if trend it turns out to be—more apparent than in the video RAM (VRAM) business. The parts have become so complex that product managers sometimes have to call in their applications engineers just to get through a list of features on a data sheet. Modern VRAMs have bidirectional serial ports, double-buffering capability, write masks, bit-block-transfer hardware, block-fill registers and uncounted other little gimmicks, each of which undoubtedly saved a ma-

nor customer a chip or two somewhere along the line.

But Kurt Akeley, vice-president and chief engineer at Silicon Graphics (Mountain View, CA), speaks for a growing body of users when he issues a note of dissent. "I see a lot of featurism in VRAMs," he says. "There's far too much in these parts, and that makes them too expensive. What we need is just a fast page-mode DRAM with a shift register. No project I know of is just dying to have something like a three-port video memory."

When less is more

Surprisingly, some vendors are beginning to concur. "I tend to agree with the customer," admits Texas Instruments systems marketing manager Earnest Powell. "All these added features are just driving up the price of the VRAMs. And customers won't use this

stuff unless the features are available from a second source. We're coming to a policy of releasing only a minimum feature set on the initial offering of a new VRAM, and then waiting to see what else customers ask for."

Whether other vendors agree or not, the big VRAM customers have the last word in the discussion. "The bottom line is that VRAM costs more per bit," Akeley says. "In the future, we'll be more careful where we use it. We put frame buffers of from 20 to 80 Mbytes in our products, so expensive memory chips get extremely painful. And with our excellent in-house ASIC capability, the trade-off of doing more work in ASICs and substituting faster generic DRAMs for more-expensive VRAMs looks very attractive." That could be the handwriting on the wall for all specialty DRAM vendors.

running so fast that no DRAM—even from the misty drawing boards in Japan—could keep up cycle-for-cycle. Therefore, fast systems have to have a cache. But once the system designer has put in a cache, the economics of fast memory changes. A dollar invested in a better cache to cut the miss rate may be much more effective than a dollar spent on faster DRAMs to reduce the miss penalty. This is particularly the case because fast systems tend to have lots of memory, multiplying the incremental cost of fast DRAM by a very large integer.

Eliminating the cache

"We've just started shipping a 53-ns, 1-Mbit part," says David Snyder, director of market development at NMB Technologies (San Jose, CA). "Fifty-three is a magic number, because it's the speed at which you can build a cacheless 20-MHz PC with no wait states." Snyder says that theoretically, faster systems could also use the part to increase their Mips rate by cutting cache miss latency. "But right now," he says, "we see the part getting designed into midrange 386 SX and DX systems where it can eliminate the cache altogether. The premium for these parts over 80-ns ones will eventually get down to around \$1. At that point, the cost of upgrading

to fast DRAM is much less than the cost of putting in a cache. So we see the parts in a midrange strategy."

Just how fast DRAMs will get is an interesting point of contention among vendors. Some houses that concentrate on mass-market products see 70 ns as a specialty part. Speed demon NMB, on the other hand, claims that the majority of its production is faster than 70 ns. The company has made a business of refining the design of the conventional CMOS DRAM—improving drivers, cutting the impedance of internal runs and tweaking everything to produce the fastest possible memory. And the results have been amazing. "We expect to ship some early samples of 60- to 80-ns, 4-Mbit parts toward the end of the year," says Snyder. "Once that part is in production, it looks like it will be possible to lift out the internal 1-Mbit memory cells, which would give us 1-Mbit parts running at about 40 ns."

Domestic vendor Vitelic (San Jose, CA) is also in pursuit of speed through clever design. "I can certainly see 45-ns access times in the cards; it will take some innovation, but nothing spectacular," says marketing manager Shubha Tuljapurkar. "You have to be willing to compromise die size a little. Then getting speed is just a process of

using the latest technology—0.7- μ m in our case—controlling channel lengths and not wasting time in setting up the row addresses."

Other vendors are pursuing speed through process innovation. Hitachi, for instance, expects to see 25- to 35-ns BiCMOS DRAMs soon. Such parts would have nonmultiplexed (broadside) address loading to save time, and would use bipolar transistor extensively inside the memory and in the driver circuitry.

Mitsubishi (Sunnyvale, CA) is also keeping an eye on the potential of BiCMOS, according to Charles Hart, marketing manager for memory products. "But you have to watch the cost/performance," he warns. "The most important use of BiCMOS may be in ECL memory systems, where you could do an ECL-I/O DRAM with 35- to 40-ns access time and a 70-ns cycle. It's not that ECL helps the speed of the DRAM so much as it simplifies things for people who have moved to ECL cache controllers."

A myriad of modes

Fast random access times are an important contributor to system performance. But as any architect knows, they aren't the whole story. Increasingly, cache-based systems are taking advantage of the special operating modes available on most

DRAMs: nibble mode, static-column mode, fast page mode, and so forth. Any self-respecting standard part has at least one fast operating mode.

As chip designers wax creative, though, and the modes get more complex, it's becoming difficult to draw the line between a standard part with an obscure operating mode and an application-specific DRAM. This is particularly the case as some of the features developed for VRAMs begin to show up in supposedly standard parts.

Nearly all fast access modes—nibble mode is the big exception—are based on the internal structure of the modern DRAM. Down inside, the chip contains one or more rectangular arrays of memory cells. When the chip gets a row address, it moves the contents of an entire row of bits out to an entire row of sense-amp outputs. This takes a lot of current and, relatively speaking, a lot of time—row selection accounts for most of the random access time of the part. But once row selection is finished, all the bits in the row are theoretically available.

The problem, of course, is that there aren't 256 I/O pins on the package to bring out a whole row of bits. So the DRAM multiplexes out the bits selected by the column address. If you don't change the row address, this multiplexing can happen very quickly. A part with a 160-ns cycle time and an 80-ns row access time, for example, may only need 20 ns to pick a bit from within the current row.

Other approaches

One recent variation on this theme is suggested by Vitelic's Tuljapurkar. "You can do a pipelined fast page mode. Essentially, you pipeline the row accesses so you would have the full row access time for the first access, then perhaps 30 ns for access to the next row."

Another approach is to blend the access capabilities of the DRAM to the timing requirements of a particular microprocessor. "We're looking at a burst mode, for instance," Tuljapurkar continues. "Given the way the internal cache controller in the 486 works, a burst-mode DRAM might reduce the need for a secondary cache." In such a part, presumably, the column access logic would be designed to deliver an entire line to the 486 cache at burst speed.

In addition to the more-traditional modes for fast access, vendors are

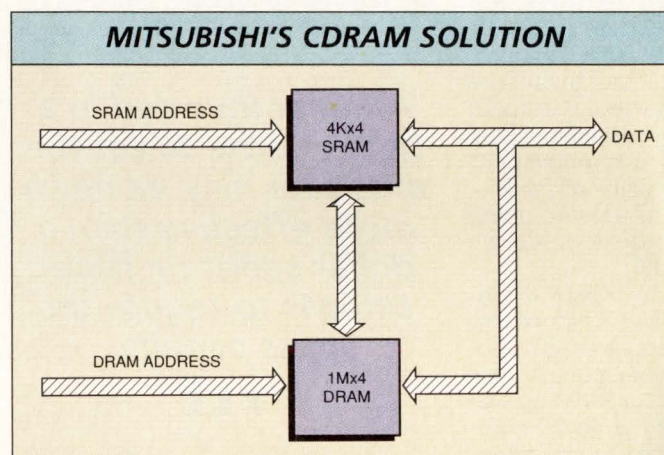
looking at new modes to solve particular application problems. Toshiba, for instance, has borrowed the write-per-bit mode from its VRAM family for use in a conventional $\times 4$ DRAM. "The mode gives an alternative to the read-modify-write cycle," says Kanadjian, "potentially saving a lot of time in some systems."

A similar result comes from an entirely different need at TI. Powell says the company needed an efficient way to store parity bits in its memory modules. Since the modules typically come in byte-multiple widths, the company needed, in effect, a $128k \times 1$ or $256k \times 1$ part to store parity bits. Rather than build

simply adding some timing and control logic, vendors produced a part that was virtually pin-compatible with SRAMs, but at a fraction of the cost per bit. An address multiplexer and timing generator took in the address broadside, divided it up into row and column components and strobed it into the selectors. A refresh controller kept track of the refresh count and did a refresh cycle in response to an external signal.

Appeal of pseudo-statics

Originally, pseudo-statics were seen as a low-cost alternative to large SRAM chips in embedded systems. But with the advent of big, wide-



Mitsubishi has taken an extra step in trying to shrink memory systems for small computers. The CDRAM combines standard DRAM and cache data memory on a single die. The device reduces parts count and keeps the critical cache-to-DRAM data path on chip.

a DRAM at such an uneconomical density, the company came up with a new idea, which it christened a parity DRAM.

"The device is a $256k \times 4$ DRAM, but with four column address strobe (CAS) lines," says Powell. "With one CAS per bit, we can individually select each of the four bits at each address on the chip." In addition to TI's original application, the device apparently can be used to provide write-per-bit functionality for graphics memories.

Such elaborate operating modes require a good deal of peripheral logic to be added to the DRAM's memory array. Sometimes this logic grows so complex as to change the functionality of the DRAM entirely. Such is the case for two of the original specialty DRAM products—pseudo-static DRAMs and VRAMs.

Pseudo-static DRAMs were a natural outgrowth of the mode proliferation in standard parts. The vanilla DRAMs had already incorporated their own refresh address counters to do automatic CAS-before-RAS (row address strobe) refresh. By

word parts, the emphasis is changing. If the main memory of a palmtop computer consists of one $256k \times 16$ DRAM, it's far more economical to use a $256k \times 16$ pseudo-static than to include a separate DRAM controller. In addition, the pseudo-static, because it controls its own refresh timing, can potentially use less standby power than an equivalent low-power generic DRAM. These facts may come as a rude surprise to PC core logic chip set designers, who have been busily incorporating DRAM controllers into their compact chip sets.

DRAM vendor Mitsubishi has done a good deal more than mimic an SRAM. In its new CDRAM, the company has added a $4k \times 4$ cache data RAM to a $1M \times 4$ DRAM die. "The on-chip 64-bit data path between the two memories lets you transmit a small block of data very quickly to the cache," says Mitsubishi's Hart. Used with an external cache controller and tag RAM, the part offers a novel solution to small, cache-based memory systems.

While the pseudo-statics focus on

■ SPECIAL-PURPOSE DRAMS

low power for the battery market, the other classical example of specialty DRAMs, VRAMs, is moving in the opposite direction. Driven by a need to differentiate—perhaps to justify high prices—and easily pushed around by big customers, VRAMs seem to be caught in the throes of rampant feature proliferation.

■ VRAM complexities multiply

Customers have been complaining for some time that VRAMs are difficult to use, primarily because every vendor has its own feature set, and so—though everybody makes VRAMs—all the parts end up being single-sourced if you use their best features. “Extended features are very important, but how to decide when to use a new feature is tough,” warns Desi Rhoden, a member of the technical staff at Hewlett-Packard’s graphics technology division (Fort Collins, CO). “Design management has to look at it in terms of goals—can we meet this goal without using a single-sourced feature, or do we have to take the risk?”

JEDEC has tried to help by developing a standard VRAM feature set, but the committee proposal isn’t public yet. And if the proposal isn’t very aggressive about incorporating the latest thinking, by the time the standard is out vendors will have trampled it in their rush to differentiate.

“We started out with a 1-Mbit part with essentially JEDEC features,” says Toshiba’s Kanadjian. “Now we’ve added flash write, in which one command can erase an entire row of bits; block write, in which we load a data pattern into a register and then strobe it into memory with repeated writes; and split transfer, in which we divide the serial register in two and then double buffer to permit uninterrupted output at the serial port.”

This ambitious feature set is being adopted in one form or another by most VRAM vendors. But there’s more to come. In the next generation, Toshiba has decided on a 2-Mbit part—“Customers told us it was more useful than a full 4-Mbit,” says Kanadjian—with even more features available as metal mask options.

One trick will be a pipelined fast page mode, related to the mode Vitelic plans for its DRAMs. Another goody will be a stop register to mark the end of data in the serial register. This will let designers essentially fix the length of the serial register in

hardware to fit the number of pixels on their CRT lines, regardless of the internal organization of the VRAM.

But the grand prize for fancy may go to another vendor, Micron, for a three-port VRAM. Other vendors have already made the VRAM’s serial port bidirectional, so the chip can capture serial data as well as regurgitate it. Micron, though, learning from some customers that the bidirectional serial port was a bottleneck, has added an entirely separate second serial port. “Basically, the part is a 1-Mbit VRAM with an additional serial register,” says Micron’s Mailloux. “The two registers work independently except during register-to-register transfers.”

For good measure, the part man-

A dollar invested in a better cache to cut the miss rate may be much more effective than a dollar spent on faster DRAMs to reduce the miss penalty.



ages to include most of the other trendy VRAM features, including split transfers, a bit-masked write operation and Boolean operations between rows. “In some sense, you can think of the part not as a VRAM but as an intelligent FIFO,” says Phil Martin, Micron product marketing manager for multiport DRAMs. “We’re having fun watching customers come up with applications.”

The VRAM idea has spawned a whole series of parts that are only DRAMs in a technical sense. Field memories and line memories—DRAMs with only serial inputs and outputs but no random-access port at all—will play key roles in the evolution of digital television and eventually high-definition television. Such chips offer huge storage capacity and moderate speed at low cost-per-bit—just the prescription for big digital imaging systems where one frame may gobble up several megabytes.

As the amount of application-specific logic around the DRAM array increases, one is led to a logical question: “Why not put the DRAM on an ASIC, rather than put full-custom

logic around the DRAM?” After all, most of the features on existing production DRAMs are metal-mask options, anyway.

Toshiba’s Kanadjian offers an intriguing answer to the question. “Technically, it would be quite possible to put down a DRAM block with a gate array,” he says. “In fact, we heard quite a lot of interest when we presented a paper on the subject a while ago. But we haven’t any immediate plans that I know of.”

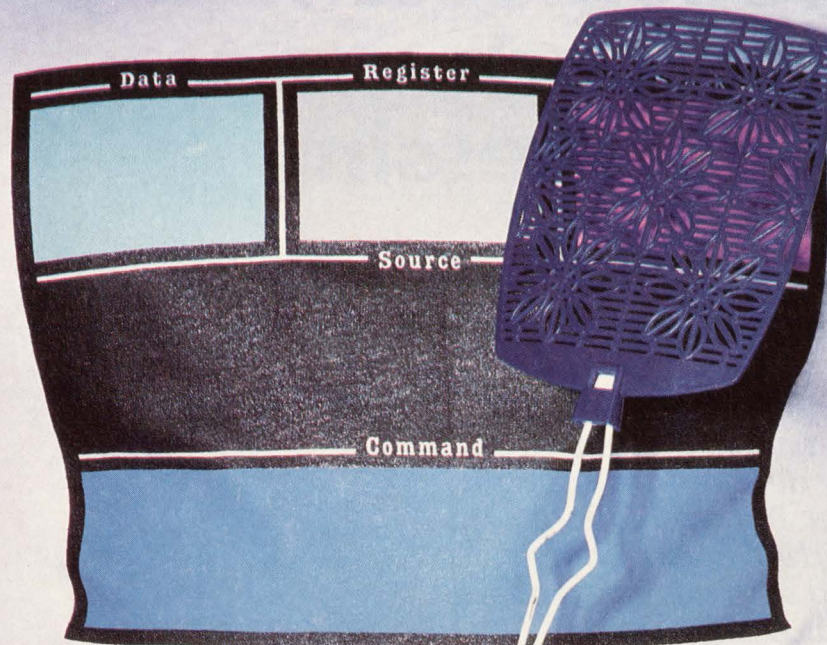
It could be that with the increasing proliferation of modes, features and I/O styles, a semicustom product is the end of the specialty DRAM evolution. In this view of the future, wide-word standard parts would become the dominant products. The $\times 1$ and $\times 4$ chips would be virtual specialty products, used only in enormous arrays. There would continue to be specialty development for extra-fast and extra-low-power DRAMs. But the bulk of what are today specialty needs—niches for pseudo-statics, VRAMs and so forth—would be met by a few master slices, producing a range of semicustom and semistandard products through gate-array, or perhaps standard-cell, techniques.

Such a situation would provide solutions for the well-heeled customer with peculiar design ideas and for the small DRAM vendor who chooses to serve niche markets. It would also couple the whole range of DRAM applications, from the most generic to the most obscure, into the inexorable march to higher density and higher speed. ■

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Application determines best approach to multiprocessing

Warren Andrews
Senior Editor

Multiprocessing gets around some of the shortcomings inherent in microprocessor design—not enough compute power. But applications determine which of a variety of multiprocessing schemes on standard or proprietary buses are used.

Multiprocessing—putting more than a single microprocessor to work on a problem—is becoming an increasingly popular technique for boosting system horsepower. However, simply adding processors to a system doesn't necessarily guarantee an increase in performance if it's not accompanied by the proper application and operating system software. The issue becomes even more complex when designers are dealing with real-time solutions where deterministic behavior is essential. Finally, within a standard-bus environment, there are further constraints on how information is transferred from one part of a system to another across a system bus. The real problem is how to implement such multiprocessing mechanisms without affecting either determinism or performance.

Despite these obstacles, multiprocessing approaches are mushrooming in popularity in both industrial real-time and commercial Unix environments. Today's systems, whether supplying real-time control for a multidimensional flight simu-

lator or lightning response for a compute or file server, are demanding more power than silicon vendors are able to put on a single die or in a single package. While the individual multiprocessing approaches are as varied as the applications served, they generally fall into one of two basic camps: tightly or loosely coupled.

Certainly it's convenient to define multiprocessing solutions as one or the other of these approaches but it's not always accurate. It's possible—and in many cases, being done—to combine the approaches to satisfy specific requirements. Furthermore, the applications themselves go a long way to dictate exactly how a multiprocessing scheme is implemented. In addition, it's easy to be trapped by fallacious reasoning that's a result of some illusion about multiprocessing.

■ Multiprocessing illusions

"It's sometimes easy to look at multiprocessing and draw some incorrect conclusions," says John Hyde, Multibus II marketing manager at

Intel (Hillsboro, OR). "The first illusion about multiprocessing is that it's simple. There's a tendency on the part of some designers to minimize the complexity of multiprocessor design." Hyde says that too often processors or processor systems are thrown together without enough thought as to how they will work together. And when poorly implemented, a multiprocessing design can actually detract from, rather than add to, a system's performance, he adds.

"Another common illusion is that loosely coupled architectures necessarily provide less performance than tightly coupled approaches—particularly in Unix applications," says Hyde. "But in many cases loosely coupled architectures can outperform tightly coupled systems—especially when dealing with standard bus/system architectures. And despite elaborate models indicating that large numbers of processors can be closely coupled on a standard architecture bus—such as Futurebus+—there may be a gap between the model and reality when the number of processors exceeds four in

a conventional shared-memory, multiprocessor architecture.”

Other illusions, says Hyde, deal with inconsistencies between the fundamental operating characteristics of tightly coupled systems and their real-time performance. Error rate differences between the two approaches and software and real-world constraints to concatenating a large number of processors in a coherent system can interfere with critical timing parameters. “These issues, as well as other issues specific to the application, all become part of the problem of defining and implementing a multiprocessing system,” he says. And almost every multiprocessing approach calls for sitting on one side of the fence or the other—either loosely or tightly coupled processing.

Loosely coupled and tightly coupled architectures are widely discussed, yet there’s often little consensus about what’s meant. For example, terms such as “massively parallel compute engine” are often used, but mean different things to different people. And far too often



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tightly coupled architectures are thought of as performance winners while loosely coupled architectures are considered at the bottom of the performance spectrum.

When real computing power is required, though, loosely coupled approaches are almost exclusively invoked (see "The power and simplicity of distributed computing," on p 75). When Digital Equipment Corp wanted to do an exhaustive simulation of Futurebus+, for example, the company tied 34 of its latest 8800 VAX machines together through some kind of network

owned by each processor so that any other processor requiring data must request it, and it can be exchanged—but not shared.

Conversely, a tightly coupled architecture comprises identical processors sharing a common memory. And this model serves well if it were not for multilevel memory. If nothing more than the sharing of a common memory was required in a tightly coupled architecture, implementation would be relatively straightforward. But today's processors (especially RISC machines) fly along at such quick execution speeds

provides any mechanism for maintaining consistent cache memory content—or cache coherency.

To provide cache coherency, a bus must make provision for such signals as bus snooping or snarfing. Snooping is when a cache monitors all cache-coherent transactions on a processor or system bus. Snooping allows a cache to change its cache-line state when reading certain transactions. For example, if a cache snoops a read-modified, invalidate, or write-invalid transaction, it must change the state of the cache line to invalid.

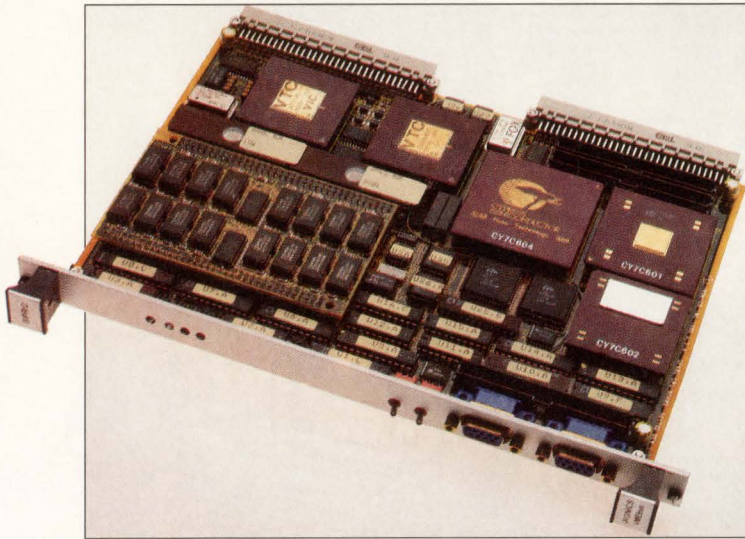
In some cases a cache is allowed to convert a transaction occurring on the bus to a broadcast operation and "snarf," or capture, the data. This allows the cache to retain a shared copy of a cache line without an additional transaction. In most cases, system modules are permitted to snarf read-shared, copy-back, read-invalid and shared-response transactions.

In addition, there must be a mechanism and protocols in place to allow for updating multiple caches simultaneously. Finally, the bus must provide a transfer mechanism that lets caches be updated quickly enough so that the system isn't paralyzed during cache updates.

"Many companies have tried, but there have been few successful efforts at running multiple tightly coupled processors sharing a common memory joined by standard buses such as VME," says Ed Schuman, vice-president of marketing at Ironics (Ithaca, NY). He explains that while many companies, including Ironics, have been successful in implementing limited cache-coherency techniques on VME through the clever application of software, performance has been too slow to be of much practical use.

■ Loosely coupled

"Although manufacturers will claim their approaches are different," says Hyde, "almost all of those boasting that they're doing multiprocessing on a standard bus—VME and Multibus II vendors alike—are really involved in what boils down to be loosely coupled systems." It's far easier to execute multiprocessor systems on Multibus II than on VME, Hyde says, because Multibus II was developed specifically to operate in a multiprocessing environment. VME, on the other hand, must use special software to operate mul-



Ironics' IV-SPRC-25A board has provision for two separate buses: a standard VME system bus and a high-speed, cache-coherent secondary M bus. Because of the board's relative size and the number of chips involved, a full-sized 6U×160-mm VME card must be used as a neighbor board to add additional clusters to the M bus.

scheme, and these machines—totaling \$1.7 million in compute power—completed the simulation in eight days.

The basic concept of loosely coupled multiprocessing is using two or more similar (or dissimilar) computer systems coupled together to attack a single task. Fundamental to this concept is the idea that each processor is its own encapsulated entity, complete with processor, program and data memory, some kind of interface or communication scheme for talking to other processors, and the I/O it needs to do its job.

The concept of each board being, in essence, a complete single-board computer (SBC) is key to how a loosely coupled system operates. Each board has the ability to communicate with other boards in the system so that data or control information can be exchanged. One of the more significant characteristics of the loosely coupled architecture is that the SBCs in a system don't share data. Data is exclusively

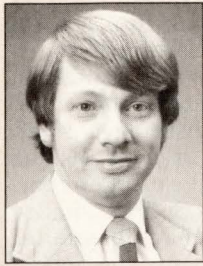
that keeping their data and instruction queues filled is a big problem. The idea of incorporating cache memory therefore looms significantly.

■ Cache coherency

In a single-processor system the concept of cache has worked well: the processor looks first to the high-speed cache to read and write data. Depending on the particular cache scheme (such as copy-back or write-through), the cache is updated and eventually the main memory is brought up to date. But where multiple processors must share the same memory space, there could easily be problems when the data that one processor grabs hasn't yet been updated from another's cache, creating significant system errors.

Maintaining consistency in the content of multiple cache memories in a tightly coupled, multiprocessing system is a major cause of problems in both standard and proprietary bus-based systems. None of the standard, open-architecture buses (with the exception of Futurebus+)

The power and simplicity of distributed computing



It's late in the evening and, once again, you're the only one left in the office. If only your personal computer/workstation was 10 times more powerful, or the file server faster, then you could have completed your project and been home hours ago! But a solution is close at hand, almost within reach.

Like most people, you view the network you're connected to as a way of passing information from one independent system to another—information such as electronic mail or data exchange between your client system and file/printer server systems. It's possible to view your network as a single system of parallel processors, and all you need is the operating software to unlock and control the latent power of this multiprocessor system.

When the term "multiprocessing" is discussed, the symmetric multiprocessing model shown at the top of the diagram is most often used. Here multiple CPUs are physically close to each other and share the same memory; this model is complicated by the fact that modern microprocessors have internal cache memories and elaborate algorithms must be used to ensure that data in memory is consistent. The fundamental goal of this symmetric model is to produce a more powerful CPU using multiple microprocessors. It's understood that all of the microprocessors must be identical, and that some low-level kernel software will manage the dispersion of software tasks (off-the-shelf software that does this, however, isn't available).

Returning to the network of PCs, the basic architecture shown at the bottom of the diagram is similar to the symmetric model. The major difference is that the network processors are physically far apart, so the communication between them is slower, hence the term "loosely coupled." It's possible to have non-PCs, such as VAXes and Macintoshes, on this network since these could have a hardware connection and adhere to the same communications protocols, but for now, let's assume that all of the CPUs on this network are X86-based PCs.

The dominant operating system that has been used on the PC for many years is DOS. Although DOS has undergone many enhancements since its introduction in 1982, it's still a single-thread operating system—that is, it runs a single task or program at a time. Creative engineers have written elegant interrupt service routines that allow a variety of functions (such as print spooling, receiving electronic mail, network monitoring, and so on) to operate "in the background," but the limitations of DOS have stifled the notion that a network of PCs could be viewed as a large parallel processor system.

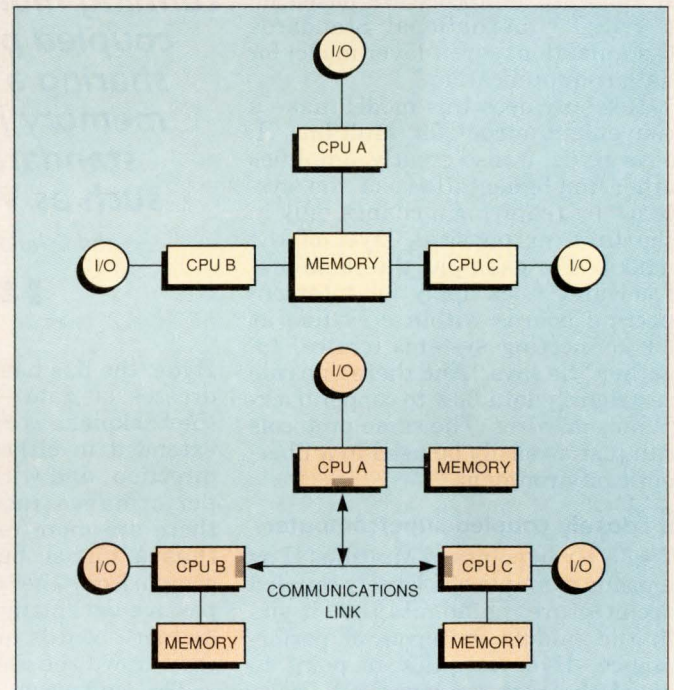
The introduction of OS/2, QNX and Unix with the necessary communications capabilities, multitasking functions and client-server constructs has fueled network-based applications. The client-server model is particularly important since it allows an application to be divided into several tasks that may be run concurrently on different machines on the network. In other words, we can distribute the processing across all of the network's computing resources and gain the performance increase directly. Furthermore, since each distributed task operates in the background of a multitasking system at low priority, the visible performance of each PC isn't adversely affected.

A recent demonstration of distributed processing power was set up by Novell—the company used 100 286-based PCs, running at 6 MHz or 8 MHz and linked by Ethernet, to calculate a Mandelbrot set. A distributed Mandelbrot application was implemented as a background server task available to other agents on the network; when client tasks made a request of the Man-

delbrot server, the server would in turn start many agent tasks on many processors. The single-system plot was benchmarked at 22 hr and 23 min. Novell's network completed the plot in 17 min—80 times faster than the single machine.

It's interesting to note that while this benchmark was running, many of the machines on the network were being used for text editing and inventory-order processing. The agent tasks ran at a lower priority than the user tasks, so no one on the network was aware of any degradation in system performance.

Intel has used this network model of distributed computing in two of its prod-



uct lines: Multibus II and the Parallel Supercomputer. The model fits well with the ever-increasing levels of silicon integration and allows the latest silicon technology to be easily absorbed into a practical application.

There's a lot of talk in the industry about multiprocessing—symmetric multiprocessing components are being designed and symmetric multiprocessing software is being written. In the meantime there are many practical problems that can be solved with a distributed multiprocessing approach.

John Hyde, BS in electronics, Multibus II marketing manager, Intel

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multiple processors in a system.

"Multibus II is essentially a LAN operating on the backplane of a card cage, and each card is a node on that network," says Hyde. The key to keeping the processors operating together is the message-passing protocols built into the specification. Messages are generated by one processor and passed to one or more others in the system via the main parallel system bus. Because the bus is completely decoupled from each processor in the system, there's never any impediment to system or individual processor performance.

"The MPCs (Message-Passing Co-processors) manage all the bus traffic and decouple the processors from the system bus," Hyde says. "Messages provide the interprocessor communications. Also, the Multibus II software protocols are based on the ISO (International Standards Organization) seven-layer model for data communication."

Not only does this model make a convenient model for Multibus II, says Hyde, it also greatly simplifies other implementations of the system—by requiring a change only in the first, or physical, layer of the model. "For example, the same protocol and rules apply for interconnecting boards within a system as for connecting systems (crates) together," he says. "And there's no rule restricting data flow to copper backplanes or wires. The same protocols can just as easily be used in a fiber-optic environment."

■ Loosely coupled supercomputer

While Hyde points to Multibus II as a prime example of a loosely coupled architecture, he admits that it sits in the middle in terms of performance. Hyde is quick to point to another Intel achievement, however, as an example of how performance isn't limited in a loosely coupled scheme. Hyde's example is Intel's hypercube supercomputer. Hyde explains that the hypercube architecture has undergone a name change to a "mesh" architecture because of a conflict over the use of the name.

He says the mesh architecture in the supercomputer is much like Multibus II in that each computer node is a complete entity with processor and memory, and communication between processors is based on the ISO seven-layer stack. However, he maintains, that's about where the similarity ends. Multibus

II is a passive backplane (limiting implementations to about 21 slots), while the mesh architecture uses an active backplane resembling a crossbar switch with little limitation on expansion.

The mesh provides an active x, y switched backplane. It has a component called a mesh interface chip that ties each board to the mesh. The interface has three 8-bit inputs and three similar outputs that allow packets to be routed from an x in to a y out at the same time. Data is always handled in packets that have a limited amount of header information and some data. In fact, says

"There have been few successful efforts at running multiple tightly coupled processors sharing a common memory joined by standard buses such as VMEbus."

—Ed Schulman, Ironics



Hyde, the bus has no concept of addresses or data—only packets. As the backplane is extended, it can be extended in either the x or the y direction, and with each extension, performance increases—because there are more routing paths, and thus a higher bus bandwidth. In comparison, the performance of a passive-backplane system decreases as more boards are added because they crowd the limited bandwidth.

The software interface to the mesh is in fact a network—the same scheme as Multibus II except the modules in the mesh architecture only allow message passing. There's no concept of memory space or I/O space on the mesh—the entire system involves the high-speed routing of packets from one processor to another. Despite the differences in how the backplane is physically connected, both the supercomputer and Multibus II share the same logical operating mechanisms. If, for example, a program is made to operate in a networking environment, says Hyde, it will run with no major modification on Multibus II or on a mesh supercomputer.

But more germane to many real-time applications is an architecture with a number of functional units operating almost autonomously with only a loose link to a central organization processor. Such an architecture, which Ironics' Schulman calls "partitioned multiprocessing" offers a variety of advantages. First, a task can be partitioned, letting different CPUs handle different portions of the problem. Second, similar tasks can be assigned to similar processors, simplifying the job of control. Third, it's easier to write code for separate processors doing separate jobs, and the approach lends itself to a top-down design methodology. Finally, it's possible to tailor each CPU in the system to the type of job it's expected to do.

For example, if one part of a project requires a lot of fast Fourier transforms or filtering, a digital signal processor could be invoked. Other CPUs could be optimized for graphics or selected for economy or performance, allowing designers to optimize a system totally to a prescribed set of priorities.

■ On a standard bus

While such partitioned approaches provide a high level of flexibility and performance, tying a system together, maintaining synchronization and handling inputs and outputs can result in additional problems that are often exacerbated by the constraints of standard-bus protocols and architectures. Furthermore, each application has its own unique requirements both in terms of the CPUs used and how they're programmed and in terms of how and what they communicate to other CPUs in the system.

"Multibus II provides the most convenient approach for handling interprocessor communications through its message-passing protocols," says Schulman. It provides an MPC, which handles interboard communications. The MPC decouples the main processor on board from the bus so that under no circumstances can the bus impede the operation of the processor. All transfers—on and off the board—are handled through the FIFO in the MPC.

In VMEbus-based systems, on the other hand, designers have had to develop other techniques for buffering the processor from the bus and transferring information from board to board without interfering with the processors. Techniques such as

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mailboxes, semaphores or similar devices have emerged to create something similar to a message-passing environment.

One of the keys to implementing such "message passing" on VME is the use of cleverly designed interface chips. One of the first to offer total message-passing capability was the FGA002 interface chip developed by Force Computers (Campbell, CA). This chip lets message blocks be passed to mailboxes established by the FGA002. However, the chip is a relatively large device incorporating a lot more than a message-passing capability and VMEbus interface, and as a result, it hasn't seen wide use outside of

Force. In addition, it's sold exclusively by Force, and it's unlikely that competitors would purchase the chip from Force unless necessary.

The VMEbus Interface Controller (VIC) chip, developed by the consortium of VMEbus makers and manufactured by VTC (Bloomington, IN), also has provision for message passing via mailboxes and is just now starting to see wide use. In addition to being used by Radstone, the chip is used by Ironics, Matrix, Omnibyte, Heurikon and others. Still other interface chips use slightly modified approaches to essentially achieve the same result.

The AVICS (Advanced VMEbus Interface Chip Set) interface solu-

tion from DY-4 Systems (Nepean, Ontario), for example, incorporates most of the necessary multiprocessing hooks, including a memory map control to facilitate interprocessor message passing and a location monitor with a built-in FIFO message queue. Key to the operation of the AVICS is the DARF (data/address register file), which provides the physical interface between the local microprocessor, local bus and the VMEbus. This serves to decouple the processor from the bus when not involved in a VMEbus transfer. It also holds the location monitor and handles what the company calls "linear addressing"—a scheme whereby message-passing software can be simplified.

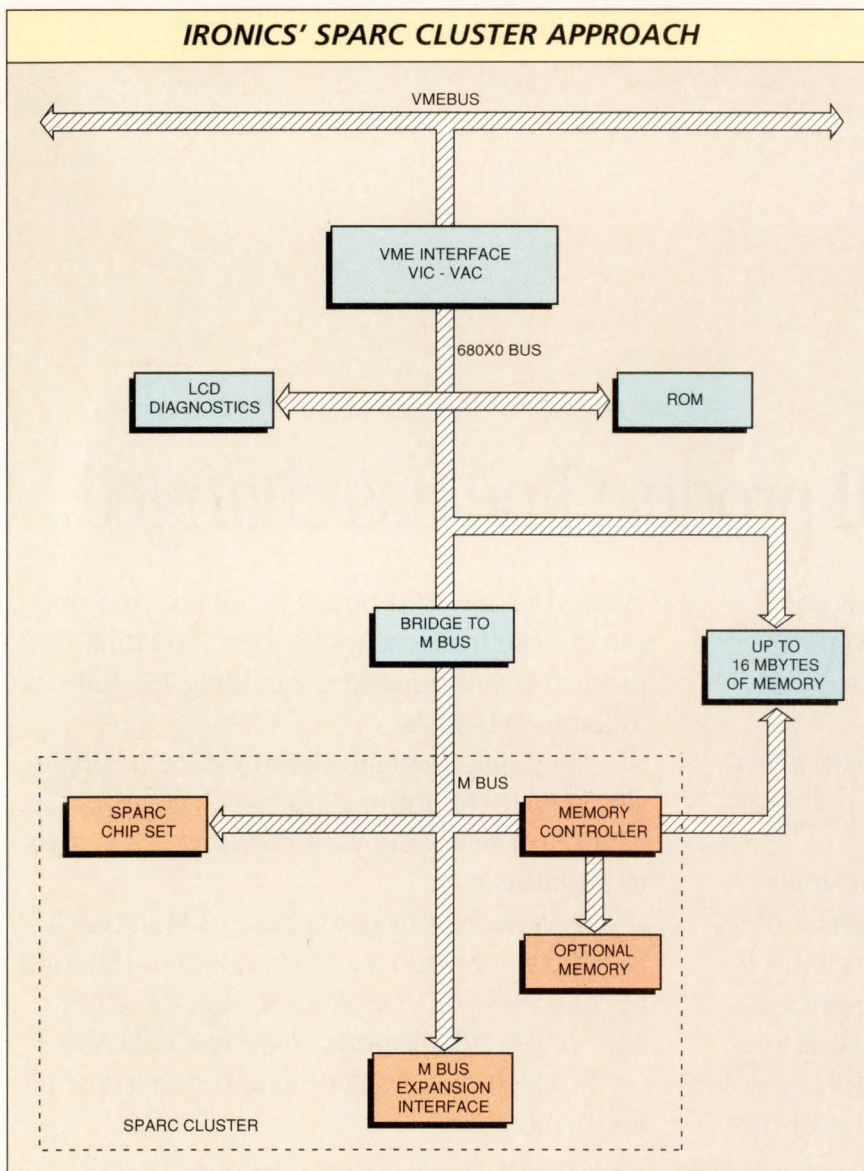
But, despite efforts to try and standardize as much of the multiprocessing structure on VME as possible, applications vary widely and call for even more creative software solutions. "It turns out," says Kim Rowe, president of Multiprocessor Tool-smiths (Nepean, Ontario), "that each application has its own special requirements. In some cases, exchanges between processors are minimal; in others, so much information needs to be exchanged that the VMEbus is insufficient." In such cases, bus traffic must be off-loaded to a secondary bus such as the VME subsystem bus (VSB), or directed through other bus channels such as those residing on daughterboards.

Keeping processors at top speed

Each application also has other requirements, in addition to simply the quantity of data that has to be transferred. "In most cases of real-time multiprocessing," says Radstone's Silverman, "there's little need to transfer large blocks of data—most transfers require relatively small block transfers." But one of the keys to any real-time system, he says, is keeping each processor running at top speed so that it can service its real-time tasks.

To do that, it's essential to let the processor run as unhindered as possible from any I/O activity. "This means that a processor shouldn't be bothered by any I/O," says Silverman. "Access from the I/O to the processor should be restricted to a 'need-to-know' basis." Radstone has developed a "free-flow" architecture to solve this problem and keep as much unnecessary traffic away from the processor as possible.

Key to Radstone's free-flow archi-

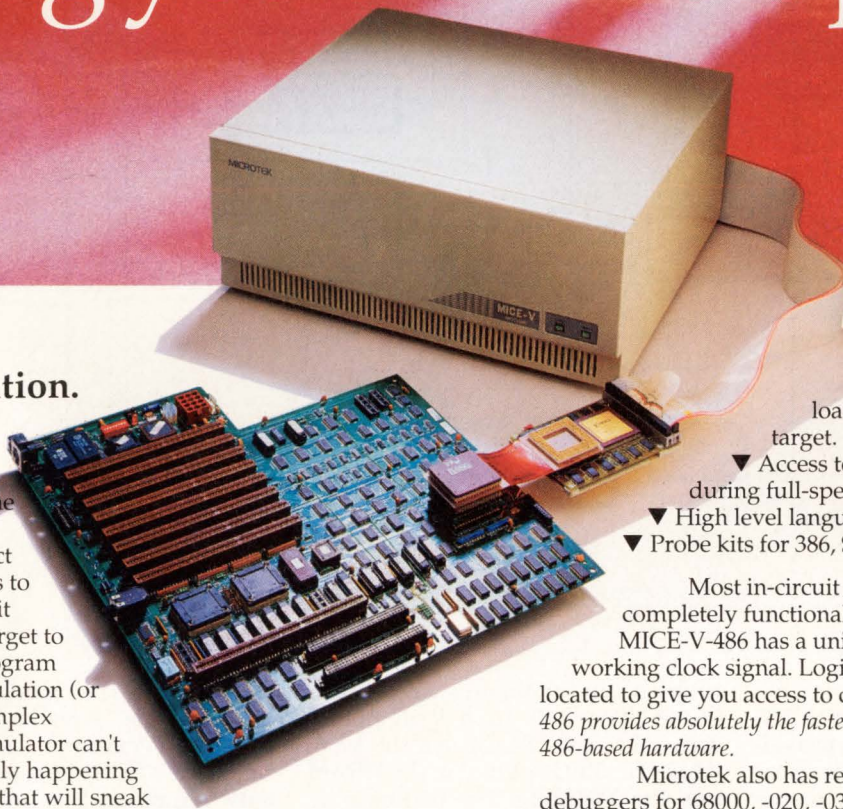


Ironics' latest RISC-based CPU board uses a Cypress Semiconductor implementation of the Sparc chip set. The chip set is tied to memory via Sun's M bus, which also allows multiple-processor chip sets—Sparc clusters—to share the same cache-coherent, processor/memory bus.

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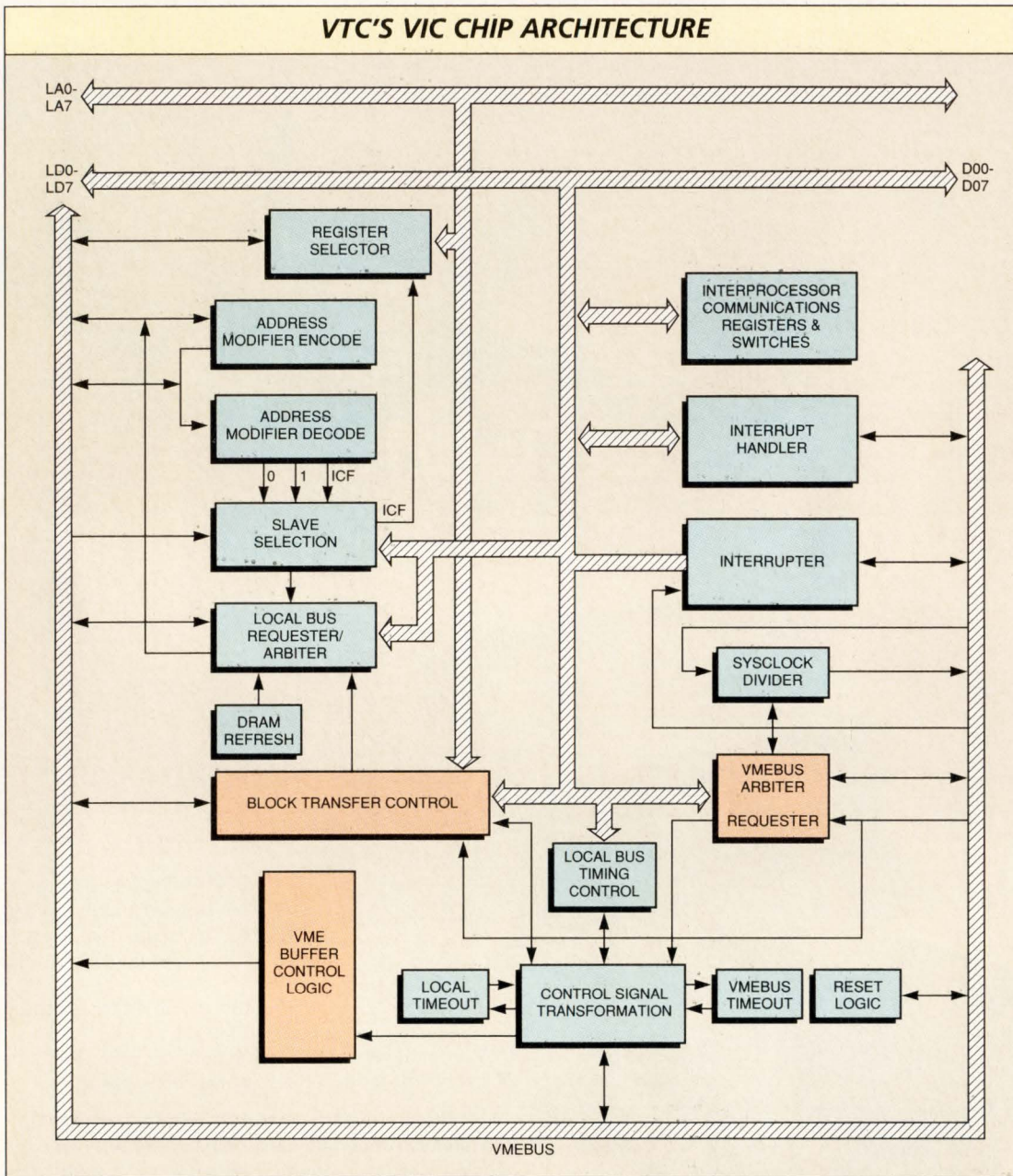
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VTC's VMEbus Interface Controller chip comprises a complete VMEbus interface function with all the inter-processor communications registers and switches required to handle multiprocessing solutions. In addition, the chip includes master/slave bus arbitration, block-transfer control logic and buffer control logic.

ecture is the efficient use of on-board buses and the secondary VME bus, or VSB. "In addition to providing fast interprocessor communications when necessary, VSB makes it possible to more tightly couple certain subsystems where necessary," says Silverman. "Though a few vendors continue to use VSB for additional I/O, many of the VME makers as well as the five major companies that have signed onto VSB as the way to go in multiprocessing configurations use the bus only for high-speed interprocessor messages."

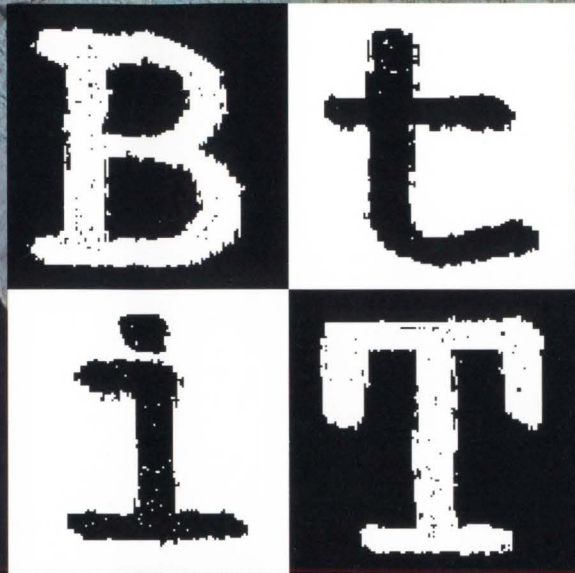
In its latest board, Radstone uses a Motorola 68040 in conjunction with a 68020 to provide a tightly

coupled subsystem on a single VME board. The 040 on a local bus is coupled to the DRAM and the VSB, while the 020 is ported to the DRAM and the VMEbus. The 040 uses its on-chip bus-snooping resources to make sure that the DRAM and cache match, so that the 020 doesn't get caught with stale data.

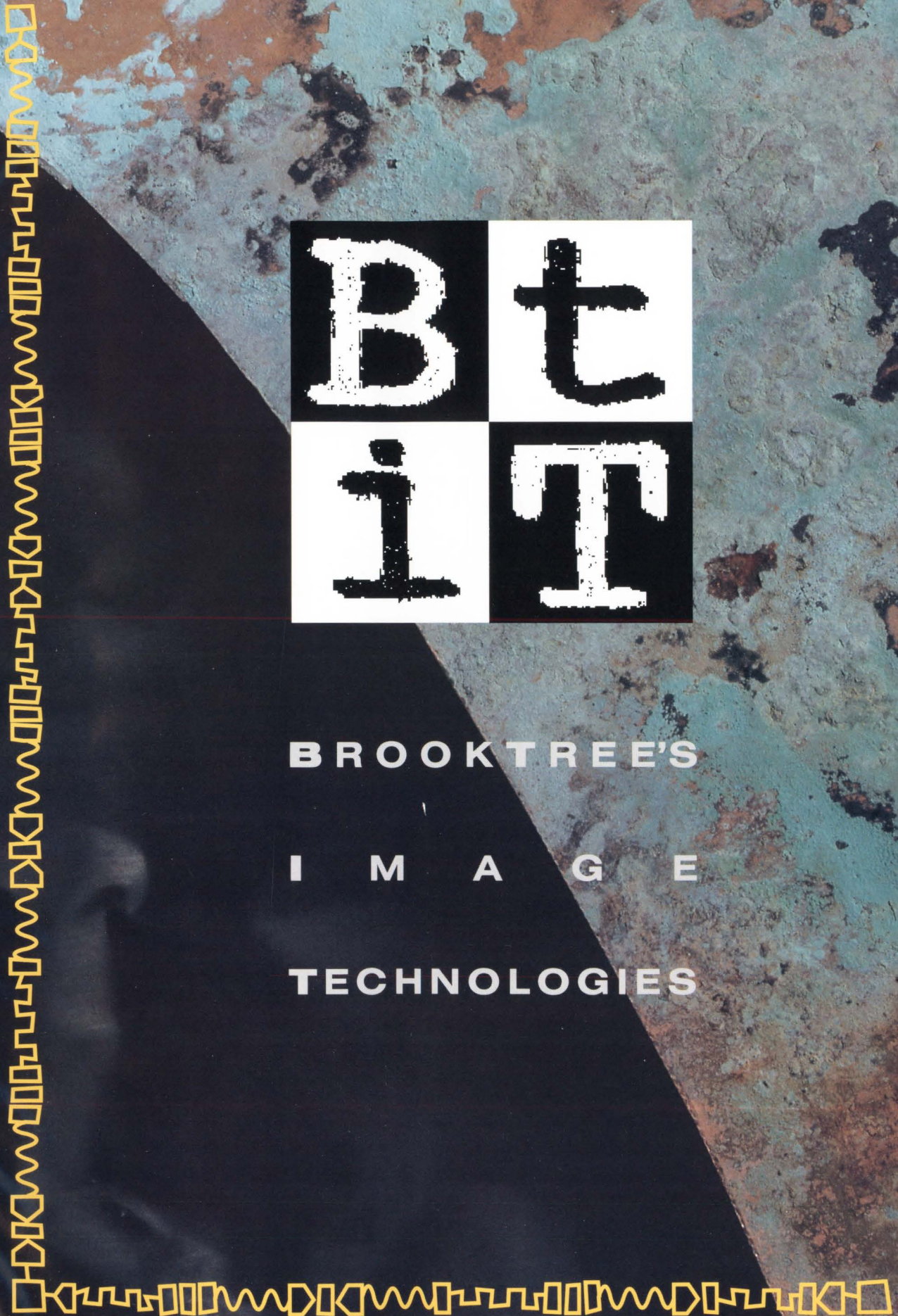
In some cases, CPUs in multiprocessing systems manage bus traffic as well as some kind of I/O. And, in such applications, the distinction between an intelligent I/O controller and an I/O processor becomes somewhat blurred. "The big difference that I see is that simple intelligent I/O serves a single function and

doesn't have the capability of making decisions," says Radstone president Pete Yeatman. "For example, Radstone's SCSI 11 board allows not only handling the information on and off the SCSI bus, but the processor has its own program and data memory such that it can take control of the VMEbus and/or VSB and direct data to other members of the system."

Mike Strang, vice-president of advanced technology at SBE (Concord, CA), basically agrees with Yeatman's explanation of intelligent I/O vs. processor node. However, in many of the communications boards SBE sells, the applications are



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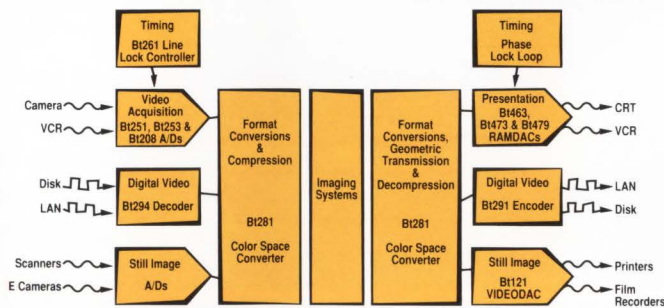
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Bt261: HSYNC Line Lock Controller, 30 MHz Pixel Clock Generation, MPU Programmable Video Timing, Programmable Noise Gating, Generate HSYNC, Recovers VSYNC and FIELD, External VCO or High Speed Crystal Oscillator Clock Generation, 28-Pin PLCC Package.

M A N I P U L A T I O N

Bt281: Color Space Converter, Three 256X8 Input Look-up Table, Programmable Matrix Coefficients, Optional Input Interpolation/Output Decimation, Standard MPU Interface, 36 MHz, 84-Pin Package.

T R A N S M I S S I O N

Bt291: RGB to CCIR 601/SMPTE RP125 Encoder, RGB Input Look-up Tables, RGB to YCrCb Conversion, Flexible Digital Filtering of YCrCb, 16-Bit YCrCb I/O Bus, Ancillary Input Port, Handles Video Timing Control, 100-Pin PLCC Package.

Bt294: YCrCb to CCIR 601/SMPTE RP125 Decoder, Handles Video Timing Recovery, Ancillary Output Port, Error Checking, 16-Bit YCrCb I/O Bus, YCrCb to RGB Output Look-up Tables, 100-Pin PLCC Package.

P R E S E N T A T I O N

Bt463: TrueVu RAMDAC, 4:1, 2:1 MUX's, Switch on a Pixel Basis Between True Color and Pseudo Color of Multiple Plane Depths with Multiple Colormaps, Two 8 Plane Overlay Cursors, Variable Palette Size, Reconfigurable Pixel Port, Advanced Diagnostics including JTAG Port, 170, 135 and 110 MHz Operation, 169-Pin PGA.

Bt473: True-Color RAMDAC VGA Compatible, Compatible with Bt253 Output Formats—24-Bit, 15-Bit and 8-Bit True-Color, 6/8-Bit Pseudo-Color, Programmable Setup (0 or 7.5 IRE), Internal/External Voltage Reference, RS-343A/RS-170 Compatible Outputs, 80, 66, 50 and 35 MHz Operation, 68-Pin PLCC Package.

Multiprocessor software considerations



The effort and skilled personnel required to build quality real-time multiprocessor systems dictate that an off-the-shelf real-time multiprocessor operating system be used. During selection, it's extremely important to carefully consider all aspects of the solution. This should include the hardware, all the software support required on the target, the development environment, system performance, upgrade paths, the total project cost and the implementation time.

The first key software consideration is the availability of reusable components, because of the savings that can be achieved when such components are purchased. Typical add-on components are a file system, terminal support, tape archive support, network support, network file system, remote procedure call, and their associated hardware support. Make sure that benchmarks are available and can be measured to identify performance bottlenecks early on during design and eliminate rework.

Industry standards are an essential ingredient when designers are choosing a real-time operating system. The important standards to be considered are Orkid and Unix. They offer advantages including vendor independence, ease of porting and high performance. There are three complete solutions available that address both of these standards: the Motorola VMEexec environment, the Software Components Group pSOS+ with associated components, and the Multiprocessor Toolsmiths Unison real-time operating system.

A third key consideration in the evaluation of a multiprocessor operating system is the resource constraints that exist in the proposed solution, and the ability of the software to deal with these constraints. Generally, designers choose a processor and/or board for the job at hand in order to minimize price/performance. If the application has mixed requirements for signal processing, high-performance I/O, and file support, a mix of processors is best; for signal processing use an i860 or an AM29K, for high-performance networking use an AM29K, and for moderate-performance I/O with

a variety of functions, use an MC68K.

One main software consideration for these mixed processors is that they all should run the same real-time operating system simultaneously, and this real-time operating system should offer the ability to debug the complete application. If these processors run in this manner, the design, implementation and maintenance of the application software becomes substantially simpler, and the effort required to upgrade performance is reduced to recompilation and minor rework.

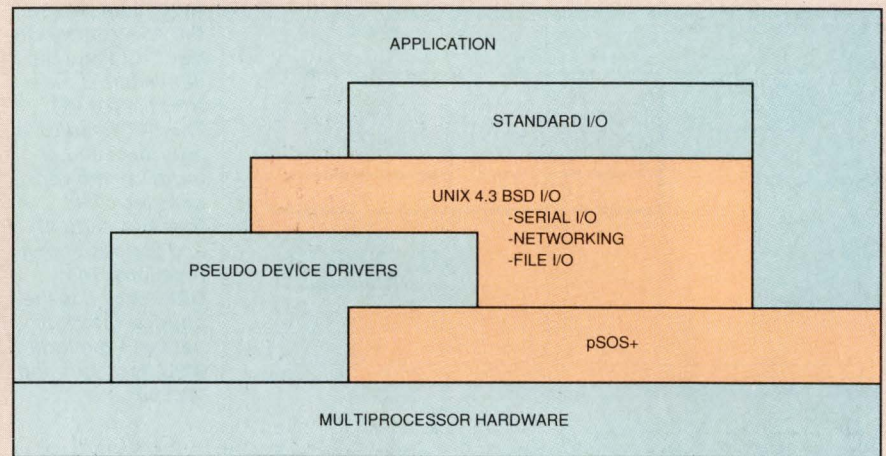
Another consideration in the area of resource constraints is the issue of application-induced bus or network saturation. The operating system must be tailorable to insure that performance criteria can be met.

The fourth key software consideration is transparency for all system calls, or the ability to make all system calls independent of the underlying processor that the software is executing on. This

and system-level debugging, simulation capability for the target, and upper and middle computer-aided software engineering tools. These tools will insure that these complex applications can be completed quickly and easily.

At the real-time operating system level, the debugger must support mixed processor debugging, debugging at the task and processor level, source- and assembly-level support, dynamic target displays, a small target size and impact (to make sure that the debugger is useful during the critical system integration phase), and remote debugging over multiple channels.

The upper and middle CASE tools should provide the capability to automate and accelerate the process of development considerably. Some key features to look for are graphical system descriptions; automated drawing, placement and connection; automatic makefiles; automatic code generation; performance analysis; temporal behav-



CASEworks/RT includes the Unison operating system, a superset of pSOS+ and VMEexec target modules. The architecture of all these solutions is identical, providing vendor independence and easy porting. Unison offers transparent multiprocessing, industry standards, reusable components and a rich support environment.

simplifies applications considerably since all processors have direct access to all I/O services. It also simplifies system design and scheduling, and supports modular expansion to meet new requirements or eliminate bottlenecks.

The last key software area is tool support. Users should look for complete environments, not just a real-time operating system. These environments should include mixed multiprocessor source-

ior analysis; standard interfaces, such as emacs and dbxtool; automatic document generation; and near real-time simulation.

Taking this type of approach during evaluation will lead to a solution meeting both short-term and long-term requirements, reduce project risk to a minimum, minimize cost, and insure that project development and maintenance time is minimized.

Kim Rowe, MEng, president, Multiprocessor Toolsmiths

MULTIPROCESSING

somewhat different and therefore the definitions have to be a little different. Strang describes a system where a main processor is running Unix, or some other general-purpose operating system, and a secondary system is simultaneously running a communications protocol such as the Transmission Control Protocol/Internet Protocol or X.25.

"Simple intelligent I/O, in comparison to multiprocessing solutions, generally only carries the networking solution through the link layer of the seven-level ISO model," says Strang. "Processor boards, to fit

the data on and off the cards fast enough. The problem is exaggerated when communications protocols such as FDDI (Fiber Distributed Data Interface), capable of transferring data at 100 Mbits/s, swallow up the bandwidth. VME64 should provide enough additional bandwidth to keep VME viable for at least another processor generation."

Although Strang sees VME64 as a salvation for VME multiprocessing, his opinion isn't necessarily echoed by the vendors involved in solving real-time problems. "Because of the type of transfers and the

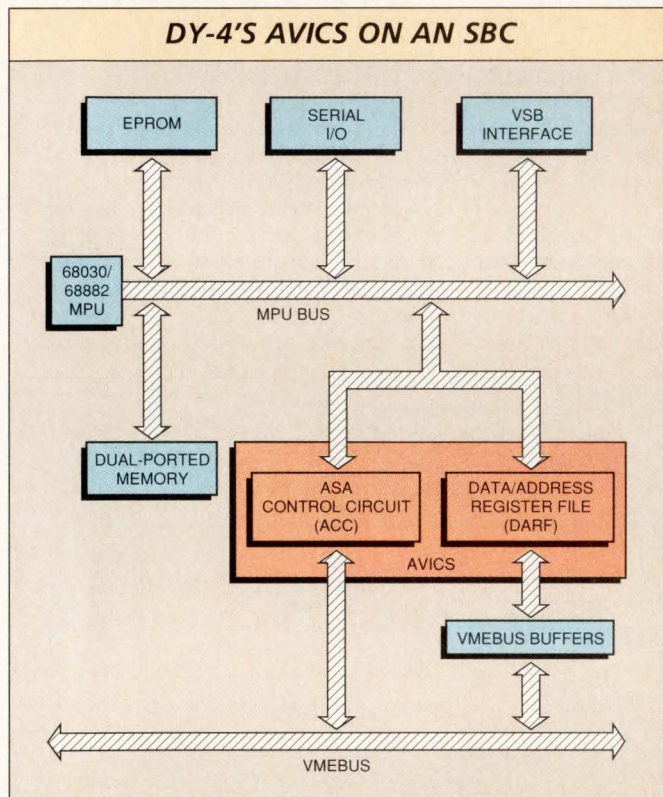
called a shared-memory multiprocessing system. One of the keys to this approach—diametrically opposed to loosely coupled—is that all data is shared. Basically, the technology in shared-memory multiprocessing is well known—the real trick is implementing it in a cost-effective way.

The tightly coupled approach has become an answer to adding more Mips in cases where a single CPU was insufficient to meet the system requirements. Inherent in the concept of multiple closely coupled processors is the concept of symmetry: that all the processors in the system be identical. While from a hardware point of view it's quite possible to interconnect a variety of processors—such as an 80486, 68040, MIPS R3000 and Sparc—in a system, it's unlikely that many programmers would volunteer to write code for such a combination. (As will be discussed, multiple different processors are both accepted and widely used in loosely coupled systems.)

Inherent too in the concept of tightly coupled multiprocessing is the idea that it requires special software. Standard single-threaded software will show no advantage running on a closely coupled multiprocessing system since its program flow is sequential. To gain the advantages of such architectures, software (either application or operating system) must be partitioned to schedule different elements of the overall program to each of the included CPUs. And when writing such multithreaded software it's critical that programmers link timing so that sequential operations are handled efficiently. Poor programming could result in one processor being idle during most of the time that it must wait for another to complete its calculations.

The two major problems are how to schedule tasks among processors and how to handle such things as interrupts when a task is being partitioned among multiple processors. Each company pursuing a symmetric multiprocessing project is developing its own set of rules to handle these problems. "At Intel there are efforts going on in the direction of symmetrical multiprocessing as well as in loosely coupled architectures," says Hyde.

Intel's current effort in tightly coupled symmetrical processing is perhaps exemplary of what's happening at other companies. "Though



A typical single-board computer takes advantage of DY-4's Advanced VMEbus Interface Chip Set (AVICS) with a 680920/030/040 processor and provides the full VME interface, master/slave capability and high bandwidth. The two main functional units of the AVICS chip set are the ASA control circuit (ACC) and the data/address register file (DARF). The ACC handles interrupts and arbitration and contains local bus time-out, auto ID and various timing functions. The DARF provides the physical interface between the local MPU, local bus and VMEbus.

into a true multiprocessing environment, have to be able to handle transactions through the transport layer." And while many multiprocessing applications—particularly real-time applications—call for only a few block transfers over the bus to keep the nodes cruising along, communications boards frequently call for a lot more bandwidth.

"VME64, the 64-bit data mode for speeding VME transfers in long contiguous blocks, looks like it will be a major benefit to many VME communications applications," says Strang. "One of the major problems we have with VME now is that VMEbus bandwidth is so limited. In some cases, we've had to use VSB to get

reality of memory speeds, it doesn't pay to do VME64 in high-performance real-time multiprocessing systems," says Radstone's Silverman. There are few occasions in real-time transactions where large blocks of data have to be transferred. And in those cases, it may not be advisable to tie up the system bus (VMEbus); doing so could cause problems in responding to real-time stimuli. It would probably be better to handle such transfers with the VSB or another external bus.

Tightly coupled systems

The alternative to such loosely coupled multiprocessing systems is the tightly coupled system, sometimes

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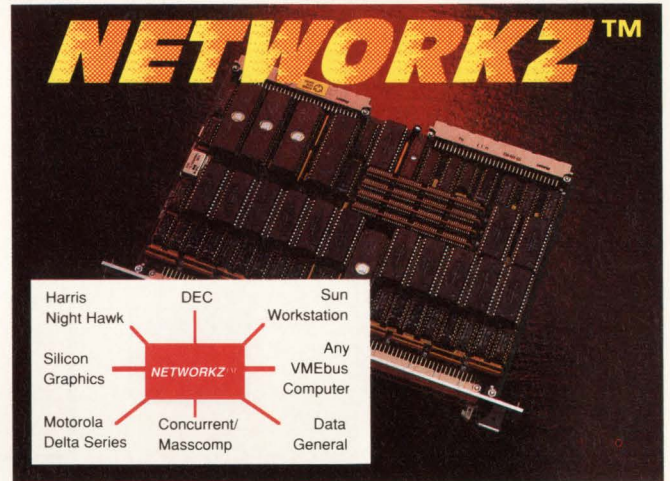
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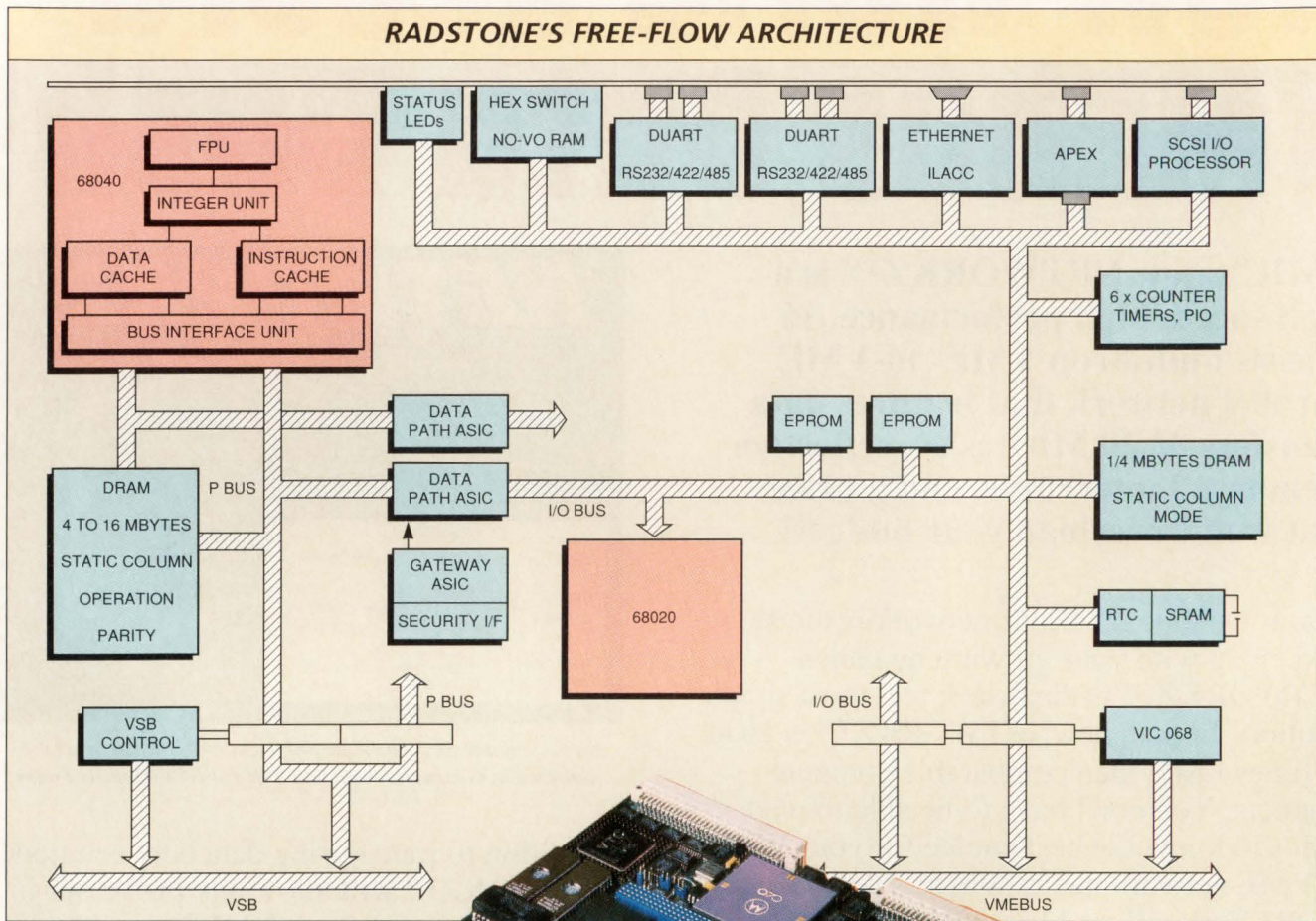
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In its latest single-board computer, Radstone Technology uses a dual Motorola 68000 structure on a single card. The 68040 shares memory with both the 68020 and the VME subsystem bus, while the 68020 shares the system VMEbus. Bus snooping on the 68040 is used to maintain cache consistency between the two processors. The card can serve as a stand-alone CPU in a dedicated system or as a node in a loosely coupled multiprocessing system.

it's most likely to show up first in some personal computer implementation, where there seems to be an insatiable thirst for performance (as well as a seemingly bottomless pocket)," says Hyde, "a similar approach would be applicable to other buses." An earlier effort in the supercomputer area, worked on jointly with Siemens and known as BIIN, was abandoned earlier this year.

The current effort contains symmetrical processing modules including a processor, a second-level cache controller, a bus controller and a currency unit. The currency unit is really nothing more than an interrupt controller with a fancy name, explains Hyde. The bus tying the memory to the bottom side of the

second-level caches hasn't yet been defined.

According to Hyde, Futurebus+ could be used only if the specification was "boiled down to a shared-memory, symmetric processing subset such as what the Multibus Manufacturers Group has been requesting for over the past 18 months. As it is, Futurebus+ comes with so much extra baggage that it couldn't easily fill the bill of the internal cache-coherent multiprocessing bus."

Interestingly, the Intel chip makers call the multiprocessing bus a "differentiation" bus. It's referred to as a differentiation bus because its actual implementation is determined by the system maker. It can

be wide (64, 128 or 256 bits) for ultimate-performance systems, or smaller for more cost-effective implementations. Therefore, it's unlikely to become a standardized bus, at least on the silicon level.

Bus on bus

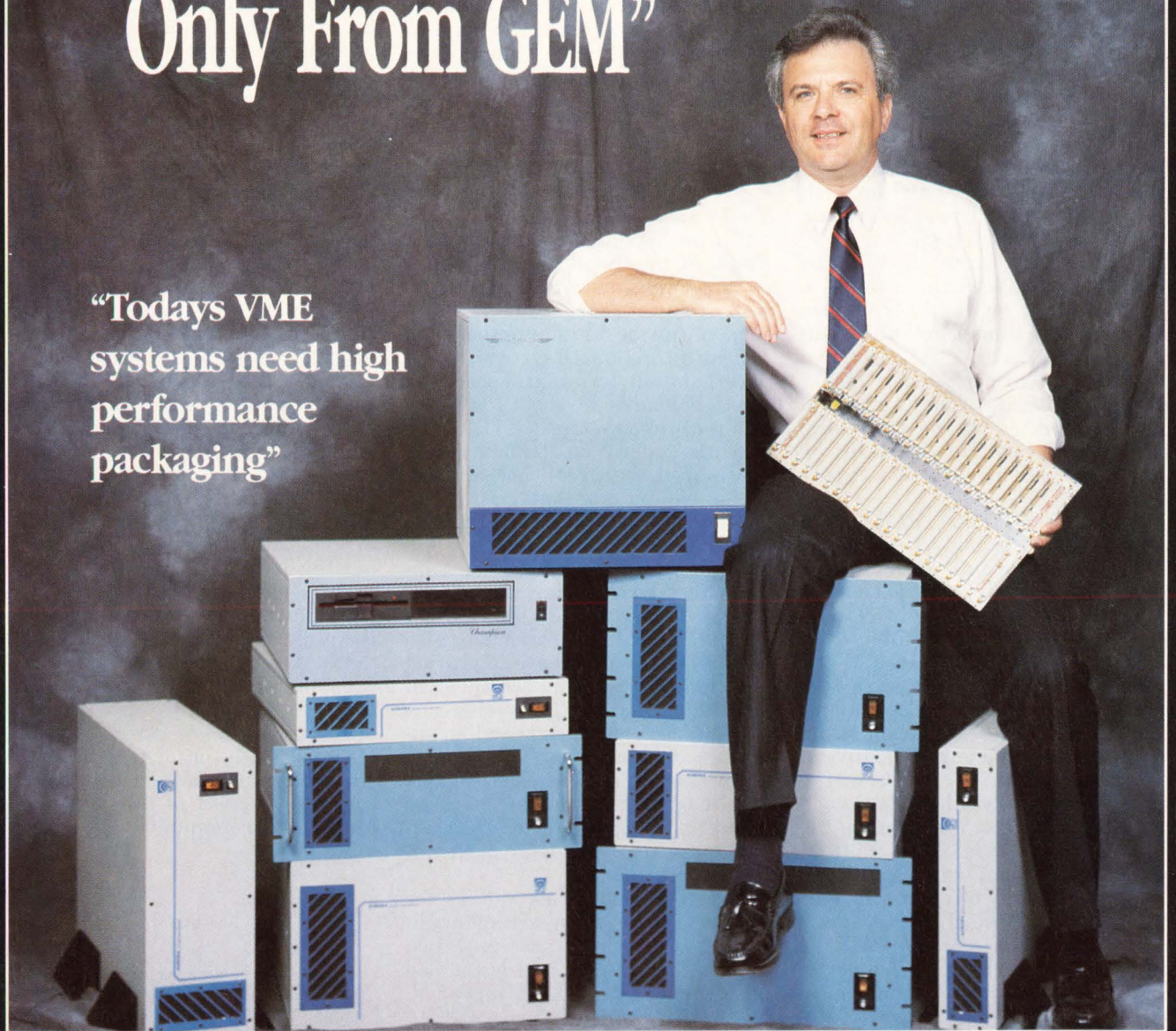
Functionally, the differentiation bus as described by Intel doesn't differ significantly from the M bus defined by both Motorola in its 88000 architecture and Sun in its Sparc architecture. Primarily a memory bus, the M bus is extremely processor-specific and has to be updated with each chip revision, so it's not likely to become a standard.

Motorola (Phoenix, AZ) uses its M bus in its 88000 Hypermodule,

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which it sells independently, and also on many of its top-performing VMEbus cards. Inherently the bus is cache-coherent and takes advantage of the cache-coherency features of the 88000 processor. The advantage of the M bus is that it allows tight coupling of the 88000 processors without any impact on the system bus (in this case VME).

A more open implementation of the M bus on a Sparc processor in a tightly coupled multiprocessing system is Ironics' latest CPU product. The VMEbus board, says Schulman, comprises a VME interface using the VIC and VAC chips (the VMEbus Address Controller chip is simply a set of buffers required for certain interface functions), an intermediate 680X0 bus, a bridge to M bus and a Cypress Sparc processor, MMU, cache, floating-point unit and memory all connected via their own local bus—the M bus. He refers to the four chips plus memory as a "Sparc cluster."

"When the CY7604 MMU is replaced with a CY7605 multiprocessing, cache-coherent MMU," says Schulman, "multiple Sparc clusters can be tied together and share a common memory over the M bus." In Ironics' implementation, the M bus is 64 bits wide and has a transfer rate of 200 Mbytes/s. The M bus, thanks to Cypress' implementation, includes bus snarfing to maintain coherency of all the caches in the system. "The only other place such a snarfing protocol is used is in the 896.1, logical layer of the Futurebus+ specification," says Schulman.

Ironics' initial offering provides the basic CPU board with a single Sparc processor offering 25-Mips performance. Additional Sparc clusters can be added with the multiprocessing, cache-coherent MMU. Because of constraints on the size of the main board, though, and because of the number of chips required in each cluster, additional clusters don't fit on what's normally considered a daughterboard.

"Instead, we use a secondary 6U VME-sized board, which we call a neighbor board, that actually plugs into the VME backplane but gets only power and ground from that backplane," says Schulman. Transfers from the main CPU—the one with the VME interface—to secondary clusters occur across a separate ribbon cable, which allows for the high-speed 64-bit 200-Mbyte/s bus.

Schulman warns, though, that

even with the cache-coherent, shared-memory M bus, it's probably unwise to increase the number of processor clusters beyond four. The demand on the main memory—and therefore the bus traffic—could begin to have a significant impact on system performance. Should the size of the available cache be increased, he continues, it might be possible to increase the number of processors beyond four.

■ Application-dependent

These solutions, whether a single CPU, an 88000 Hypermodule or a Sparc M bus implementation such as that from Ironics, basically represent one processing node in a system. It can be the only processing node in a Unix-based system such as a workstation, terminal or server, or it can be one of several CPU nodes in a real-time system.

"Unix applications tend to be less specialized than real-time applications—calling more often for a single high-speed CPU engine than for multiple medium-performance engines," says Joel Silverman, commercial products marketing manager at Radstone Technology (Montvale, NJ). "Further, because Unix systems don't have to provide deterministic performance, they can use things such as cache-coherency mechanisms, which can result in unpredictable response." For example, a processor in a cache-coherent system may have to update a cache before it's able to service an interrupt, resulting in a delay in the interrupt routine.

For that reason as well as for problems involved in writing applications programs, most real-time applications rely on loosely coupled multiprocessing architectures. Often such systems have one CPU—or a tightly coupled 'cluster' of CPUs—running Unix to serve as a housekeeping and communications center and multiple other CPUs running versions of the same system or different operating systems.

■ Looking to the future

While Multibus II and VMEbus slug it out for dominance in the 32-bit market, Futurebus+ looms as a strong contender for a variety of multiprocessing applications. It's the only standard bus that has full provision for cache coherency across the bus, letting multiple CPUs be closely coupled on the backplane. Futurebus+ also has message-pass-

ing capability, which lets loosely coupled architectures reside on a Futurebus+ backplane. And, as it's currently defined in profile A, the board is large enough to accommodate a large component count per board, which might even lead to another level of multiprocessing.

Furthermore, the Futurebus+ protocols are such that both loosely coupled and tightly coupled architectures can coexist on Futurebus+ simultaneously. Nevertheless, while it would appear that the bus has everything—including a 64-bit backplane—there is perhaps not as much excitement surrounding the bus as could be expected, particularly from the traditional VME board makers and designers engineering real-time systems.

No one seems bold enough to say that Futurebus+ won't happen, but there's apprehension about actually using the bus. Skeptics see cost as a major obstacle, while others believe that the profiles have been optimized for a workstation environment and that everything—including the form factor of the existing profiles—will have to be revised before Futurebus+ finds its way into the real-time control business.

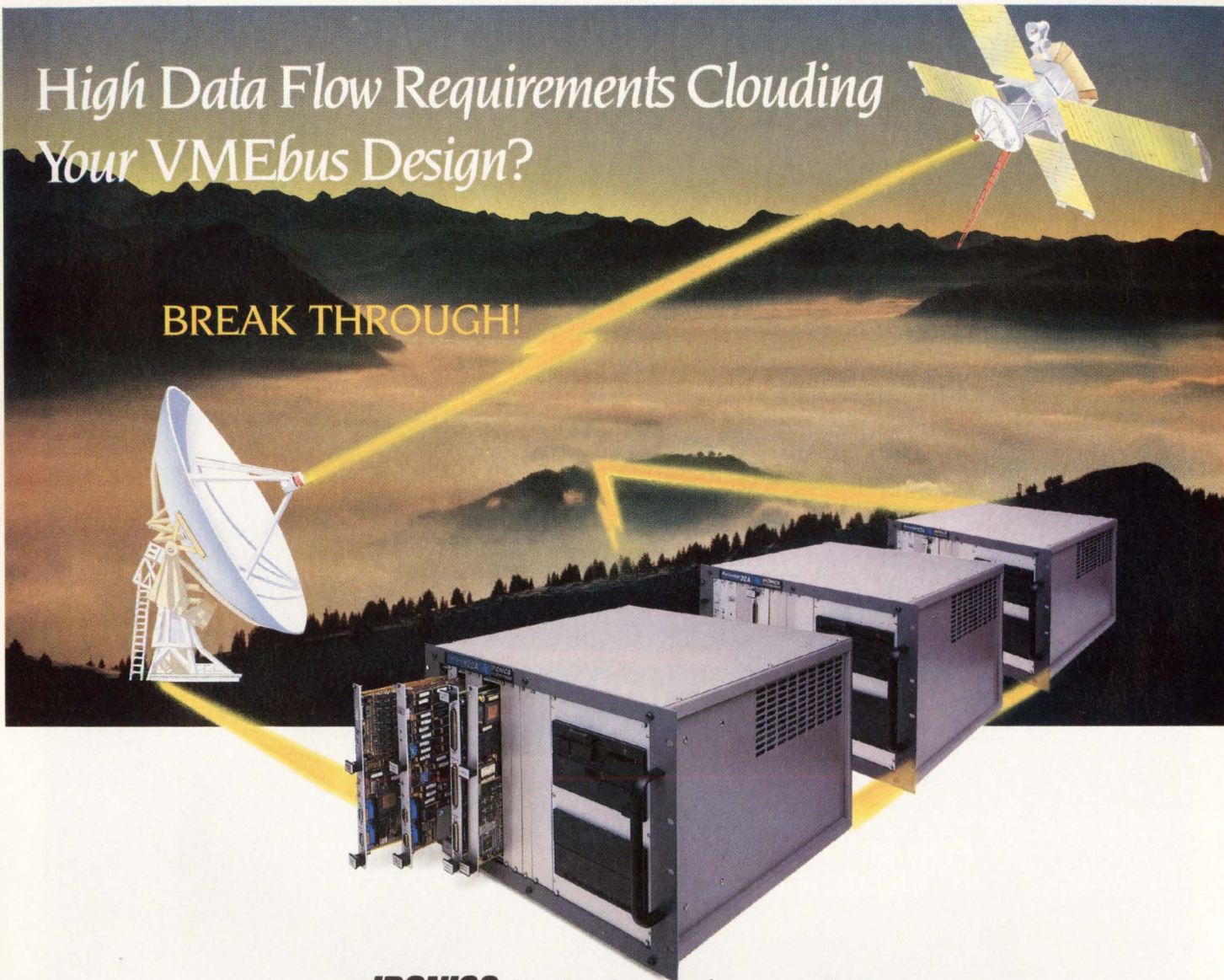
It's estimated that Futurebus+ won't develop a strong position until the existing buses—VMEbus and Multibus II—move closer to being technologically obsolete, and until an industrial profile emerges with complete support of the VME and Multibus II community. ■

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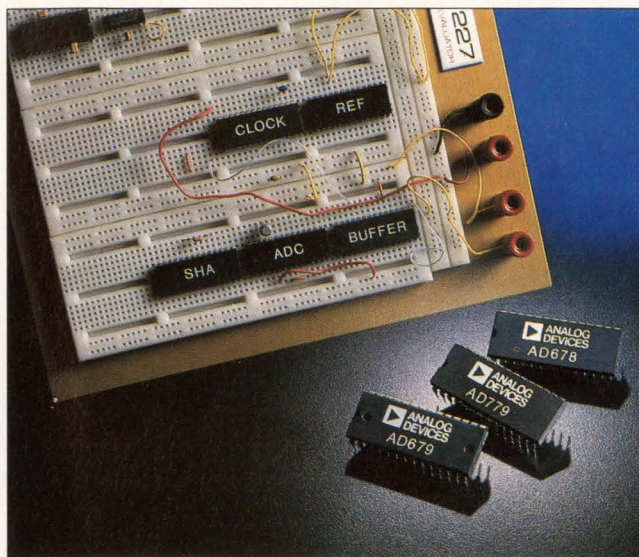
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High-resolution ADCs gain speed and on-chip functions

Jeffrey Child, Associate Editor



Part flash and part successive approximation, the AD679 and AD779 from Analog Devices are both 14-bit A-D converters offering a 100-kHz sampling rate and an input bandwidth of 1 MHz. Included on each is an S/H amplifier, internal reference, a clock and bus interface circuitry.

As devices on the digital side—from microprocessors to digital signal processors—get faster and more complex, system designers hunger for faster and more accurate high-resolution analog-to-digital conversion. And to keep up with today's shorter design cycles, high-resolution A-D converter makers are integrating more functions on their latest monolithic and hybrid A-D converters.

While hybrids hold a performance lead with new 16-bit parts sampling at rates up to 500 kHz, the latest monolithic A-D converters are rapidly improving upon the specifications of existing hybrids. In addition, new sampling techniques such as sigma-delta have given birth to some 16- through 24-bit application-specific converters with a cost edge over devices using more traditional conversion methods.

"The specifications that were previously only available in hybrid and modular devices are now available in monolithic form," says Ian Bruce, technical marketing engineer at Analog Devices (Norwood, MA), adding that they have appeared only in the last year or so. Analog's AD679 and AD779 devices exemplify the trend in monolithic A-D converters toward increased performance and more on-chip functions.

Subranging architecture

Both converters use a recursive subranging architecture. Part flash and part successive approximation,

this scheme allows the speed of flash conversion at high-resolution levels. These 14-bit devices offer a 100-kHz sampling rate and an input bandwidth of 1 MHz. Included on each is an S/H amplifier, a clock and bus interface circuitry. The AD679 and AD779 also have an on-chip +5 V

"One advantage of sigma-delta converters is that the filtering tracks exactly with the conversion rate."

Craig Ensley, Crystal Semiconductor



reference—which is traditionally very difficult to provide in a monolithic device. Previously, a designer would have to match and test each supporting component, each with its own ac specifications. By offering the S/H amplifier, A-D converter and interface circuitry on a single chip, Analog has eased the designer's task substantially.

Micro Networks (Worcester, MA) also offers a combined solution with its MN6400 A-D converter. This device features self-calibration in addition to its other functions. The 16-bit MN6400 is capable of digitizing analog input signals at a 50-kHz rate while providing 16-bit no-missing-

code performance. Self-calibration upon power-up achieves specified performance, even in extended temperature range applications.

The MN6400 offers a complete set of functions, with an inherent track-and-hold amplifier function, analog input buffer, reference, clock and control logic circuitry, and a parallel data bus driver. All of these functions are contained in a single 28-pin double-wide hybrid DIP. When sampling 1-kHz full-scale analog input signals, the MN6400 yields an 88 dB S/N ratio and -98 dB harmonics.

Despite the advantages of self-calibration, some debate exists in the industry regarding its usefulness. "Self-calibrating A-D converters tend to produce good linearity and S/N ratios," says George Hill, marketing staff engineering specialist at Burr-Brown (Tucson, AZ). "But, even when an A-D converter is self-calibrating, a user must still worry about the gain and offset from other parts of the system." Also, it's still an open question whether self-calibration on power-up or a one-time calibration done at the factory provides the better S/N ratio and linearity.

Interfacing to DSP chips

In addition to the trend toward integration, there's a growing trend of interest in DSP chips among system designers. This interest coaxed A-D converter manufacturers such as Burr-Brown to develop an A-D converter specifically designed to support DSP. Their goal was to provide

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AD779	14	100	1,000	NMC	0.56	Y	Y	monolithic	\$29.70	same as above
AD7871	14	83	41.5	NMC	0.06	Y	Y	monolithic	\$29.70	serial/parallel interface
AD7872	14	83	41.5	NMC	0.06	Y	Y	monolithic	\$29.70	complete serial interface
AD9014	14	10,000	4.3	NMC	11.5	N	N	hybrid	\$2,800	—
AD77001	16	—	0.01	NMC	0.04	N	N	monolithic	\$15	sigma-delta, 10 μ W low-power mode
AD1382	16	500	2.0	NMC	2.8	Y	Y	hybrid	\$595	sampling ADC
AD1175	22	0.02	2.0	NMC	1.8	N	Y	module	\$495	—
Analog Solutions 85 W Tasman Dr, San Jose, CA 95134-1703 (408) 433-1900										Circle 302
ZAD2716	16	100	1,400	0.5	2.3	Y	Y	module	\$220	—
ZAD1605	16	500	2,800	0.5	3.0	Y	Y	module	\$625	—
ZAD1610	16	1,000	5,300	0.8	6.2	Y	Y	module	\$825	—
ZAD2718	18	100	300	0.75	2.3	Y	Y	module	\$275	—
Analogic 360 Audubon Rd, Wakefield, MA 01880 (508) 977-3000										Circle 303
ADC3214	14	1,000	1.5	0.75	2.6	Y	Y	module	\$191	subranging ADC
ADC3110	14	2,000	2.0	0.75	4.1	Y	Y	module	\$522.75	same as above
ADC4344	16	1,000	1.0	0.75	4.0	Y	Y	module	\$685.50	2-pass subranging ADC
AH30217	17	512 μ s	0.3	0.026	0.6	N	Y	hybrid	\$139	triple slope integrating ADC
ADC5020	18	144	1,000	0.8	2.1	Y	Y	module	\$249	FFT tested
ADC5120	20	48	142	2.0	2.38	Y	Y	module	\$361	FFT tested, oversampling ADC
ADC5041	24	0.001	0.03	67	0.5	N	Y	module	\$76.75	resolution and speed programmable, 6 channels, UART interface
ADC5042	24	0.001	0.03	67	0.5	N	Y	module	\$79.50	resolution and speed programmable, 6 channels, microprocessor interface
Burr-Brown PO Box 11400, Tucson, AZ 85734 (602) 746-1111										Circle 304
ADC71	16	20	—	2.0	0.55	N	Y	hybrid	\$53.40	industry standard
ADC76	16	60	—	2.0	0.525	N	Y	hybrid	\$95	same as above
ADC700	16	60	—	2.0	0.645	N	Y	hybrid	\$103.90	microprocessor interface
ADC701	16	500	—	1.0	2.0	N	Y	hybrid	\$475	same as above
PCM78	16	200	—	—	0.6	N	Y	hybrid	\$32.50	audio applications
PCM1750	18	200	25	—	0.2	Y	Y	monolithic	—	same as above
DSP101 DSP102	18	200	100	0.002	0.25	Y	Y	hybrid	\$29.95 to \$37.45	DSP102 has 2 channels
ADC604	12	5,000	10,000	—	6.1	Y	Y	hybrid	\$1,100	14-bit accuracy
Crystal Semiconductor 4210 S Industrial Dr, Austin, TX 78744 (512) 445-7222										Circle 305
CS5014	14	56	—	0.25	0.12	Y	N	monolithic	\$45	successive approximation
CS5016	16	50	—	NMC	0.12	Y	N	monolithic	\$69.20	same as above
CS5101	16	100	—	NMC	0.28	Y	N	monolithic	\$57.60	same as above

Model	Resolution (bits)	Sample rate (ksamples/s) or conversion time	Input bandwidth (kHz)	Linearity error (\pm LSB)/NMC (no missing codes)	Power dissipation (W)	Sample & hold (Y/N)	Internal reference (Y/N)	Package type	Price	Comments
Crystal Semiconductor 4210 S Industrial Dr, Austin, TX 78744 (512) 445-7222										Circle 305
CS5102	16	20	—	NMC	0.044	Y	N	monolithic	\$39.70	same as above
CS5126	16	100	24	NMC	0.28	Y	N	monolithic	\$39.90	same as above
CS5317	16	20	10	NMC	0.22	Y	Y	monolithic	\$29.40	same as above
CS5322/3	24	—	0.5	NMC	0.22	Y	Y	monolithic	\$269.70	delta-sigma, 2-chip set
CS5324	24	—	0.5	NMC	0.15	Y	N	monolithic	\$217	delta-sigma
CS5326/7/8/9	16/18	50	20 to 22	NMC	0.45	Y	Y	monolithic	\$70.56 to \$97	delta-sigma for digital audio
CS5336/7/8/9	16	50	20 to 22	NMC	0.4	Y	Y	monolithic	\$56.40 to \$73.40	same as above
CS5501	16	4	0.01	0.125	0.025	Y	N	monolithic	\$18.20	delta-sigma
CS5503	20	4	0.01	NMC	0.025	Y	N	monolithic	\$27.70	same as above
CS5505	16	0.02	0.01	0.125	0.002	Y	Y	monolithic	—	same as above
Datel 11 Cabot Blvd, Mansfield, MA 02048 (508) 339-3000										Circle 306
ADS-930	16	500	8,000	1.0	2.1	Y	Y	hybrid	\$374	full military temperature range, on-board FIFO, overflow pin, 3-state outputs
ADS-976	16	200	6,000	1.5	1.6	Y	Y	hybrid	\$245	on-board FIFO, 3-state outputs, standard ADC-76 pinout
ADS-942	14	2,000	6,000	0.5	2.9	Y	Y	hybrid	\$374	32-pin DIP
ADS-941	14	1,000	6,000	0.5	2.8	Y	Y	hybrid	\$337	same as above
ADS-928	14	500	6,000	0.5	3.1	Y	Y	hybrid	\$299	overflow pin, 3-state outputs, 32-pin DIP
ADS-924	14	300	4,500	0.5	1.4	Y	Y	hybrid	\$199	32-pin DIP
ADC-908	14	1.0	—	0.5	2.7	N	Y	hybrid	\$243	on-board clock, overflow pin, 3-state outputs
ADC-914	14	0.3	—	0.5	0.925	N	Y	hybrid	\$175	24-pin DIP
Dymec 8 Lowell Ave, Winchester, MA 01890 (617) 729-7870										Circle 307
2840	20	0.01	0.01	0.1	1.2	N	Y	hybrid	\$69	variable conversion time/sample rate
2824	24	0.001	0.01	0.1	1.3	N	Y	module	\$199	variable conversion time, 2 channels
Fujitsu Microelectronics, IC Division 3545 N First St, San Jose, CA 95134 (800) 642-7616										Circle 308
MB87020	16	50	2,500	—	0.5	Y	Y	monolithic	\$22.91	on-board DAC
ILC Data Device 105 Wilbur Pl, Bohemia, NY 11716 (516) 567-5600										Circle 309
ADC-00145	14	5,000	10,000	0.5	4	Y	Y	hybrid	\$1,250	75 dB S/N ratio, 80 dB spurious-free dynamic range
Micro Networks 324 Clark St, Worcester, MA 01606 (508) 852-5400										Circle 310
MN6290/91	16	20	10	0.5	1.15	Y	Y	hybrid	\$180	84 dB S/N ratio, -88 dB harmonics, multi-range
MN6295/96	16	50	25	0.5	1.32	Y	Y	hybrid	\$187	84 dB S/N ratio, -88 dB harmonics, multi-range
MN6400 series	16	50	12	1.0	0.74	Y	Y	hybrid	\$175	self-calibrated bus-driver circuit, multi-range
MN5284 series	16	50 μ s	—	0.5	0.255	N	Y	hybrid	\$249	15-bit NMC

PRODUCT FOCUS/High-resolution ADCs

Model	Resolution (bits)	Sample rate (ksamples/s) or conversion time	Input bandwidth (kHz)	Linearity error (\pm LSB)/NMC (no missing codes)	Power dissipation (W)	Sample & hold (Y/N)	Internal reference (Y/N)	Package type	Price	Comments
Micro Networks 324 Clark St, Worcester, MA 01606 (508) 852-5400										Circle 310
MN5290/91	16	40 μ s	—	0.5	0.810	N	Y	hybrid	\$175	military temperature range
MN5295/96	16	17 μ s	—	0.5	0.945	N	Y	hybrid	\$194	—
MN5280	16	100 μ s	—	0.5	1.4	N	Y	hybrid	\$169	—
MN5282	16	50 μ s	—	0.5	1.4	N	Y	hybrid	\$187	—
MN5420	20	320	160	—	6.7	Y	Y	module	\$1,295	auto-ranging
Motorola DSP Operation 6501 William Cannon Dr W, Austin, TX 78735-8598 (512) 891-2030										Circle 311
DSP56ADC16	16	100	45.5	0.5	0.4	Y	Y	monolithic	\$42	12-bit samples at 400 kHz, single 5 V supply, zero-glue interface to DSP
National Semiconductor 2900 Semiconductor Dr, Santa Clara, CA 95052 (408) 721-5000										Circle 312
ADC12441	13	55	20	0.5	0.07	Y	N	monolithic	\$13.90	self-calibrating, \pm 5 V operation
ADC12451	13	83	20	0.5	0.113	Y	N	monolithic	\$14.90	self-calibrating, \pm 5 V operation
ADC1241	13	59	32	0.5	0.07	Y	N	monolithic	\$15.90	self-calibrating, \pm 5 V operation
ADC1251	13	87	32	0.5	0.113	Y	N	monolithic	\$17.50	self-calibrating, \pm 5 V operation
Prema Precision Electronics 4650 Arrow Hwy #E5, Montclair, CA 91763 (714) 621-7292										Circle 313
5601	25	20 s	—	—	0.6	N	N	module	\$360	true continuous integration
Sipex 6 Fortune Dr, Billerica, MA 01821 (508) 663-7811										Circle 314
SP9478	14	500	250	1.0	2.75	Y	Y	hybrid	\$385	-80 dB S/N ratio, 3-state outputs, military versions available
HS9476	16	50	200	2.0	1.5	Y	Y	hybrid	\$195	military version available, -92 dB spurious-free dynamic range
HS9516	16	10	50	0.5	1.2	N	Y	hybrid	\$268	military version available
HS9576	16	58	—	1.0	1.1	N	Y	hybrid	\$120	military version available

interface logic on the A-D converter to simplify connection to DSP chips. To make that same interface out of discrete logic would, according to Hill, take 24 14-bit logic packages. Typically this would require an ASIC, he maintains.

The single-channel DSP-101 and the dual-channel DSP-102 are complete successive-approximation converters. Both devices provide sampling and conversion at rates up to 200 kHz. Internal reference, timing/clock circuit and all of the DSP interface logic are included on these devices. With 18 bits of serial data output, the DSP-101 lets users drive 16-, 24- or 32-bit DSP ports. The

two-channel DSP-102 offers conversion with either two 18-bit ports or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

■ Sigma-delta sampling

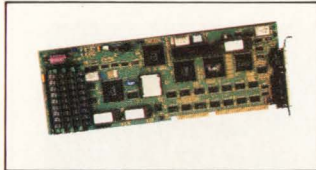
Another emerging trend in high-resolution A-D converters is one toward using a technique called oversampling—or sigma-delta. This sampling method provides a more application-specific solution than successive approximation or other conversion methods. In sigma-delta a fast 1-bit converter oversamples the input signal. The sigma-delta converter then does some DSP on that signal to produce a 16-bit paral-

lel output representation of the input. The signal is then sampled at a high data rate and produces a low-frequency parallel digital output.

Using a sigma-delta converter forces some trade-offs, however. At a low cost, sigma-delta converters offer high resolution, high accuracy and stability. The disadvantage, however, is speed. Sampling rates in the low kHz range and input bandwidths typically around 10 Hz tend to restrict these devices to specific applications. The AD77001 from Analog Devices, for example, is a 16-bit sigma-delta A-D converter with an input bandwidth of 10 Hz. Devices such as this are useful in data-acqui-

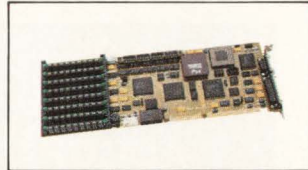


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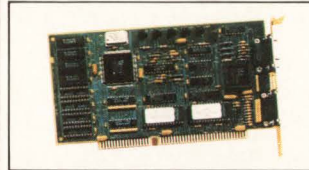
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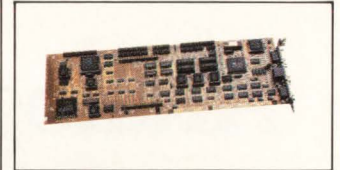
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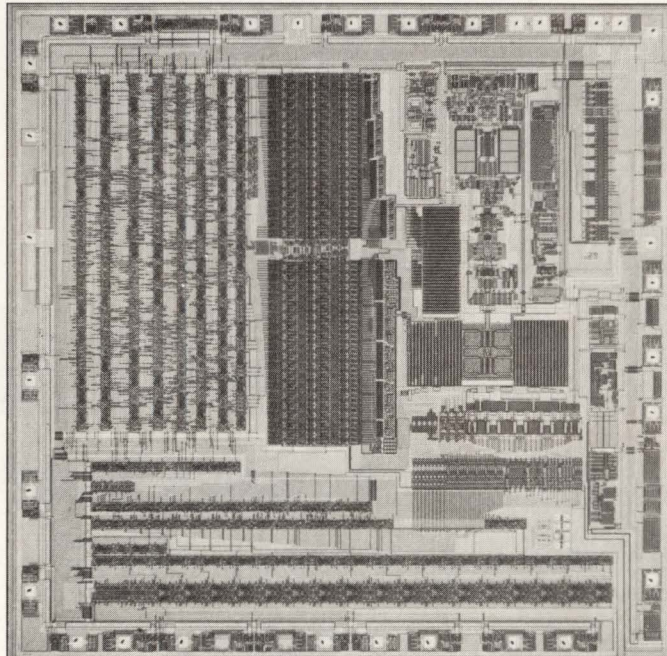
INTEGRATED CIRCUITS

sition systems dealing with small changes in input—such as temperature-reading or seismic systems.

While several companies are working on sigma-delta parts with bandwidths in the 20-kHz voice band frequencies, at least one has an actual sigma-delta A-D converter available today. Targeted for the multimedia system designer, the CS5336 from Crystal Semiconductor (Austin, TX) is a 16-bit, two-channel sigma-delta A-D converter with 50-kHz sampling and input bandwidths from 20 to 22 kHz. At this level of conversion speed, the advantages of sigma-delta come back into play.

“One advantage of sigma-delta converters is that the filtering tracks exactly with the conversion rate,” says Craig Ensley, vice-president of marketing at Crystal. “Changing the chip’s master clock inherently changes the sampling rate and the

Continued on page 96



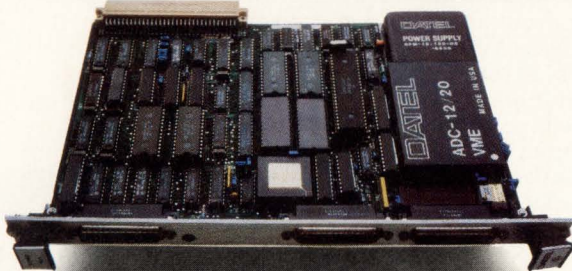
The CS5101 from Crystal Semiconductor is a 16-bit, 100-kHz A-D converter featuring industrial grade, two-channel performance. Self-calibration guarantees integral non-linearity below ±0.0015 percent, full-scale at 8 μs. Three timing modes are provided for easy interface to microcomputers and shift registers.

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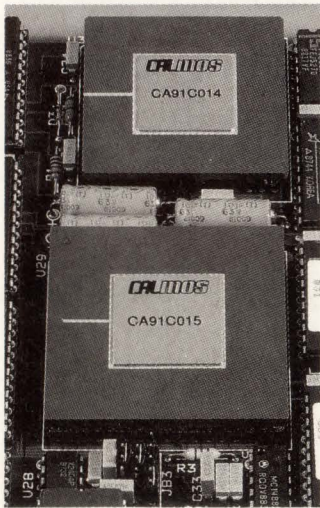
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CIRCLE NO. 58

INTEGRATED CIRCUITS

Continued from page 94
filtering rate." This allows a multimedia system designer to adjust the CS5336's input frequency to match that of the input device—CD-ROM, digital audio tape player, or modem, for example. Unlike successive-approximation A-D converters, sigma-delta converters let in less noise.

While most 16-bit, 500-kHz sampling A-D converters are packaged in either large 3x5-in. modules or two-chip hybrids, the latest A-D converter from Datal (Mansfield, MA) offers those specifications in a single 40-pin hybrid. Called the ADS-930, this sampling A-D converter is based on a two-pass, subranging architecture. Key to the performance of the ADS-930 are proprietary laser trimming techniques and an advanced gate array. Requiring ±15-V and +5-V power supplies, the ADS-930 dissipates power at 2.1 W typical and 2.4 W maximum. There is no requirement for an additional -5-V power supply. Also featured is a differential input that can reject common mode noise resulting from sensitive ground layouts.

What's more, the ADS-930 offers an on-board FIFO memory capability—a unique feature among high-resolution A-D converters. This 16-bit-wide, 16-word-deep FIFO can be simultaneously filled and emptied. Two control pins on the ADS-930 let the user access memory when half full or on command. ■

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CIRCLE NO. 60

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October 1, 1990

(This statement is published in compliance with the Act of October 23, 1962.)

Published twice monthly.

Publisher: David L. Allen, Westford, MA

Editor: John C. Miklosz, Westford, MA

Managing Editor: John W. Donovan, Westford, MA.

The owner is: Advanced Technology Group, One Technology Drive, Westford, MA 01886, PennWell Publishing Co., 1421 S. Sheridan, Tulsa, OK.

Stockholders holding 1 percent or more of total amount of stock of PennWell Publishing Co.: Successors to estate trust of Helen B. Lauinger of Tulsa, OK. Known stockholders, mortgagees and other security holders holding 1 percent or more of the total amount of bonds, mortgages or other securities: None.

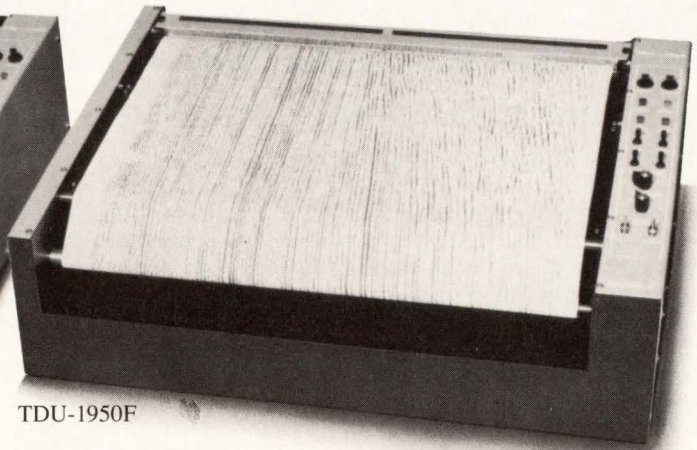
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Raytheon has added a series of wide "flatbed" models to its quality line of thermal hard copy recorders. The new TDU-1950F and TDU-1200F units, in 19.5 inch (49.5 cm) and 12 inch (30 cm) configurations, respectively, provide enhanced vertical integration of data for a broad range of specialized applications.

The flatbed models join Raytheon's established family of "free fall" thermal recorders - the TDU-850, with an 8.5 inch (21 cm) printing width, and the TDU-1200, with a 12 inch (30 cm) printing width.

Raytheon's thermal recorders produce high resolution copy at high speeds and can generate full tonal images up to 256 multi-shade levels of true grey. Alternately, they can display digital data in crisp graphic or alphanumeric form using an optional IEEE 488 interface.

Traditional uses include CRT hard copy, military surveillance, spectrum analysis, LOFAR gram displays, ultrasonic production control, and facsimile transmissions. New and evolving applications include support for computer assembly testing and chromosome analysis in genetic research.

TDU's print on paper, plastics or transparencies. They feature clean, odor-free, maintenance-free operation.

Make hard copy easy with today's most versatile and reasonably priced thermal recorders. Call or write Marketing Manager, Production Components, Raytheon Company, Submarine Signal Division, 1847 West Main Road, Portsmouth, RI, USA 02871-1087. Phone 401 847-8000.



TDU-1200



TDU-850

Raytheon

Modular VME image-processing board meets varied requirements

When creating an image-processing system, designers typically need to mix and match boards with varying input, processing and display capabilities, configuring them to meet specific application requirements. This can have drawbacks because the specific processing capabilities are likely to overlap, producing elements that are redundant.

The amount of flexibility required in an image-processing system will, of course, vary among OEMs. While one OEM user might need to perform simple arithmetic operations, another may want to do more complex histogram transformations. Or perhaps a user wants to process images without displaying them. These varied requirements demand

a modular single-board, pipelined image processor for specific application requirements. To meet these needs, Datacube has developed MaxVideo 20, a single-board VME-based image processor.

Built around a 640-Mbyte/s crosspoint switch, this image-processing engine boasts an effective processing performance of 3,500 Mips. Optional plug-in modules let users perform, in real time, point, arithmetic and spatial transforms. Occupying two slots of a VME backplane, MaxVideo 20 is backward-compatible with Datacube's previous-generation MaxVideo family.

Forming the heart of the MaxVideo motherboard is a crosspoint switch that links together all of the

processing elements on the board. With 32 8-bit inputs and 32 8-bit outputs, this path-switching mechanism links the optional video inputs, pipelined processors and graphic output sections.

A basic configuration of the board has a 1k×1k×8-bit triple-ported region-of-interest (ROI) image memory, a 12-bit in/16-bit out lookup table and an arithmetic logic unit. Configured this way, image data can be transferred to and from other VME image processors over Datacube's Maxbus interface. In addition, two MaxVideo 20 boards can be connected via the P2 expansion bus.

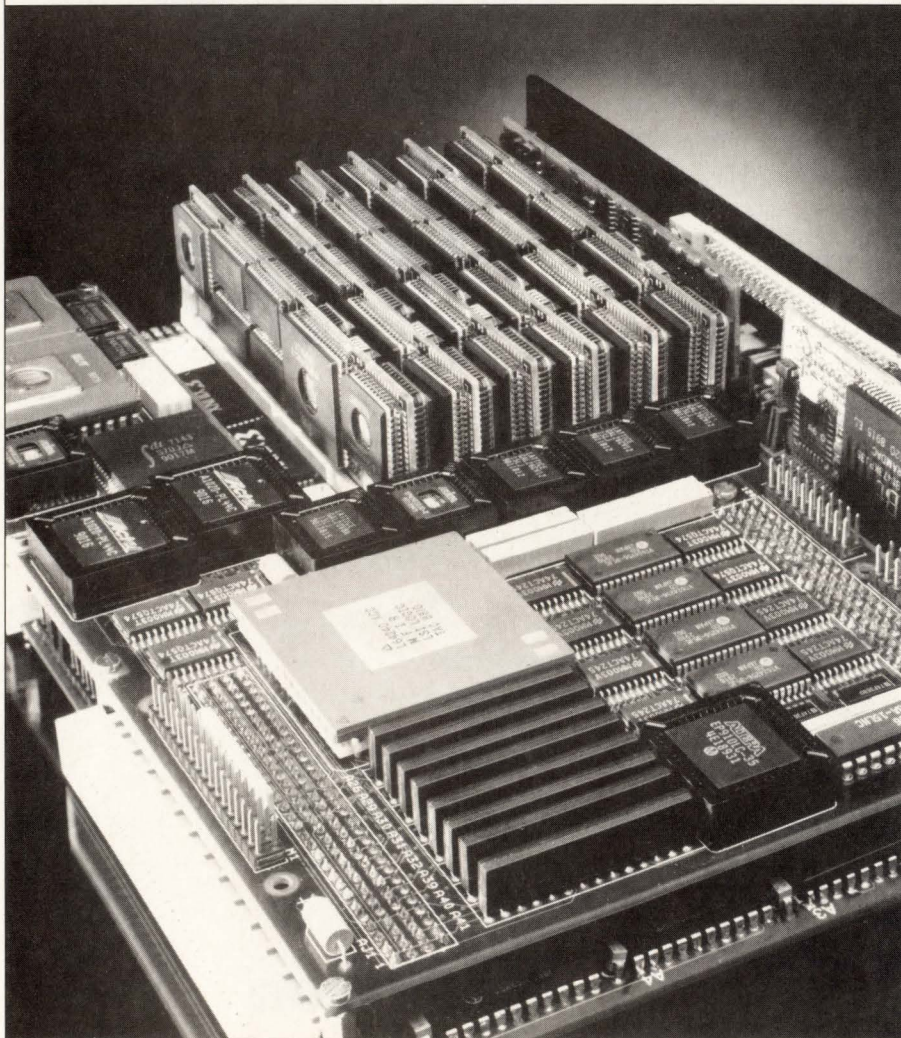
Datacube has also developed several modules that let the board act as a single-board image processor. Among these are an advanced pipelined processor, optional pipelined processors, and additional ROI image memory. An analog scanner module facilitates the input of video images, while an analog generator module supports the display of 24-bit RGB true-color images. These modules let images be digitized, processed at frame rates and displayed in real time. Both the video digitizer and display controller are supplied as modules. While the video digitizer option supports standard and nonstandard cameras up to 26 MHz, the display controller can show images as large as 1k×1k×24 bits.

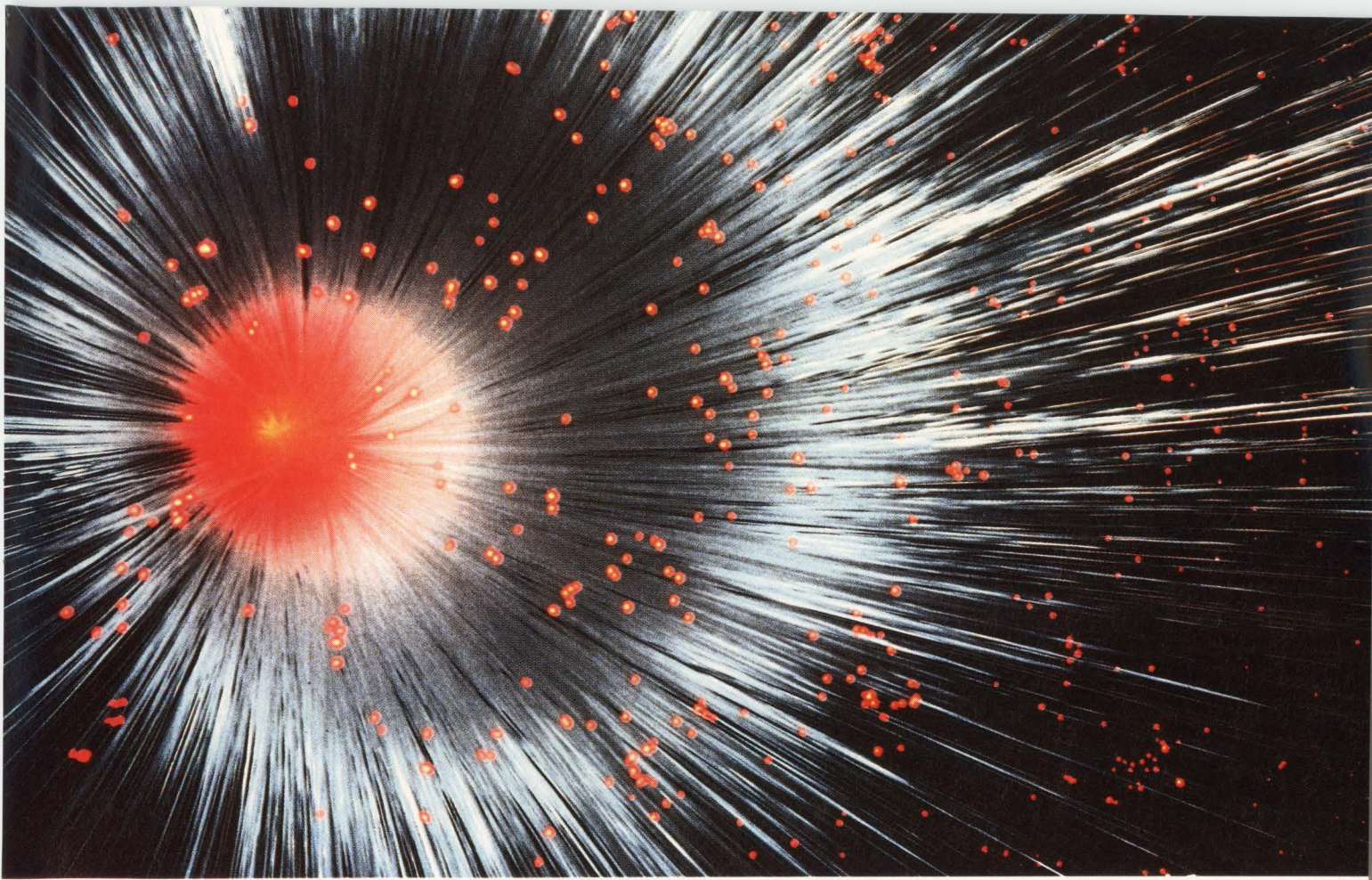
ImageFlow software

Datacube has incorporated such elements to develop ImageFlow, a software library of C-callable functions. ImageFlow uses icons to let the user view the board as a collection of image-processing elements. Using software commands, these elements can be assembled into one or more pipelines.

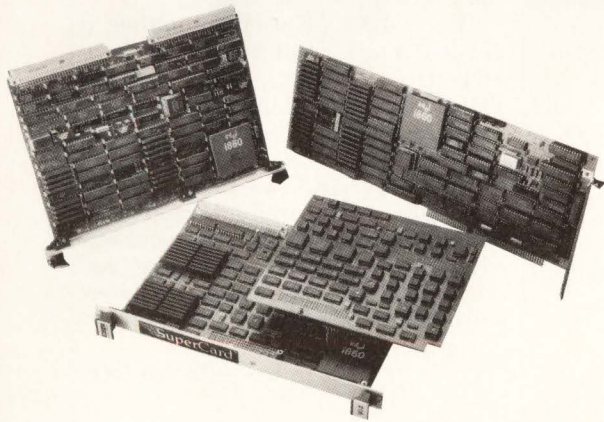
ImageFlow solves the problem of specification and control of multiple complex-image-processing pipelines required to perform real-time video-rate imaging applications. The software produces optimized, event-driven code that fully supports real-time operation of MaxVideo hardware. It's compatible with all MaxVideo products, including the high-precision 16-bit pipelines in newer products. ImageFlow functions are applied consistently

Continued on page 100





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CIRCLE NO. 53

COMPUTERS & SUBSYSTEMS

Continued from page 98

across the entire MaxViedo product line, so the addition or reconfiguration of hardware has minimal impact on the application program.

Concealing the hardware complexity from the application programmer, ImageFlow automatically resolves all data transfer timing and pipeline delay parameters, which are inherent characteristics of pipe-

lined image processors. The software supports one-shot and continuous data transfers. These can be performed immediately or in response to a user-specified event.

Other key components of ImageFlow include an error handler, a configuration file reader, and graphics and generalized input functions.

Available this month, a fully configured MaxVideo 20 system costs

\$10,000 in quantity; the unit price is \$24,000. A single-user license fee for ImageFlow is priced at \$6,000.

—Jeff Child

Datacube
4 Dearborn Rd
Peabody, MA 01960
(508) 535-6644

Circle 354

INTEGRATED CIRCUITS

GaAs gate arrays integrate over 100k usable gates

The first two devices in the Vitesse FX series of gallium-arsenide gate arrays have 102,000 and 195,000 gates and typical gate utilizations that vary from 50 percent to 70 percent. Fabricated in Vitesse's H-GaAs III process, the VGFX100K and the VGFX200K provide 196 and 256 signal I/Os, respectively, all configurable to ECL, TTL or GaAs levels.

The GaAs FX series has advantages over both ECL and BiCMOS gate arrays, according to Bob Nunn, director of gate array products at Vitesse. "Compared with ECL, the FX series offers a level of integration that is unheard of, while offering all of ECL's speed at a fraction of its

power," Nunn says. "Compared with BiCMOS, FX arrays provide up to 10 times the performance and, with the static power consumption of the GaAs Direct-Coupled FET Logic (DCFL), lower power than BiCMOS for applications operating at greater than 80 MHz." An unbuffered two-input NOR gate in the FX series has a worst-case delay of 50 ps (unloaded) and consumes only 0.14 mW of power. Typical power dissipation, assuming a 50 percent gate utilization, is 14 W for the VGFX100K and 25 W for the VGFX200K.

Unlike CMOS or BiCMOS, DCFL GaAs circuits have a power dissipation that's independent of logic state

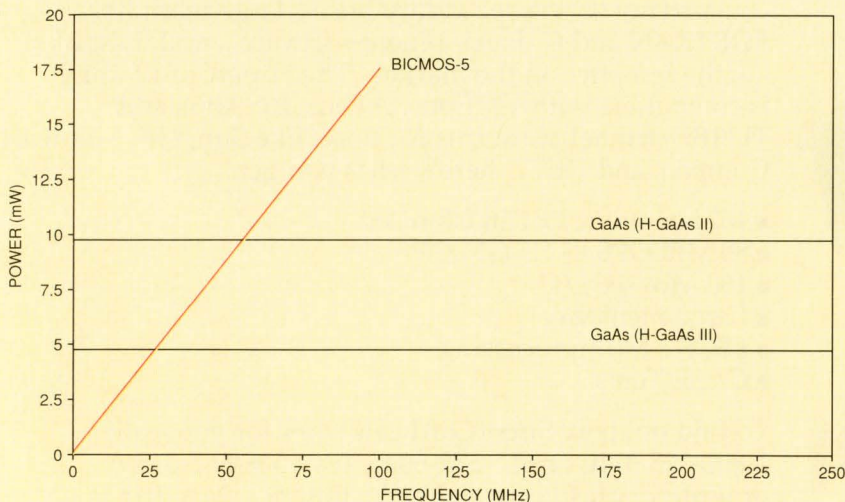
or frequency of operation. In normal operation, the current consumption of a DCFL logic gate is constant. (A NOR gate is composed of a pull-up depletion FET and one or more pull-down enhancement FETs.) Current is steered either into the pull-down FET in a logic low condition or into the gate to source diode of a subsequent logic gate in a logic high condition. When calculating the power dissipation of the DCFL-based GaAs FX series, therefore, the power dissipation reported for an individual logic macro is valid for any frequency at which it can operate.

Vitesse claims that the density of the FX series will reach 350,000 raw gates, or over one million transistors, by early next year. The availability of embedded RAM blocks of various configurations is also expected at that time. Typical access times for the RAM embedded in the GaAs arrays will be 3 ns.

The VGFX100K comes in either a 211-pin ceramic pin grid array or a 264-pin ceramic LDCC. The VGFX200K is available in a 344-pin ceramic LDCC. The typical NRE (nonrecurring engineering expense) charge for the VGFX100K is \$125,000, with production prices ranging from 0.5 to 1.5 cents per used gate. Design inputs are being accepted now, and production volumes will begin shipping in the first quarter of 1991.

—Barbara Tuck

POWER DISSIPATION VS. FREQUENCY



SOURCE: VITESSE APPLICATION NOTE AN-10
NEC BICMOS-5 DESIGN MANUAL, OCT. 1989
VITESSE FURY DESIGN MANUAL, V. 3.0

Vitesse Semiconductor
741 Calle Plano
Camarillo, CA 93012
(805) 388-3700

Circle 353

■ 8-bit MCU gets 16-bit math speed

When a cost-sensitive design switches from 8- to 16-bit, the decision is almost always painful. It's often forced by some design requirement—usually speed. The additional cost of a 16-bit microcontroller and the time needed to retool for a new architecture cannot be taken lightly. Many customers and more than a few vendors have been carefully analyzing the pressures that force a move to 16 bits, and they've been trying to find an alternative to going all the way.

"When we surveyed our customers, we found that 80 percent of the time the reason they looked at 16-bit MCUs was speed—specifically multiply and divide speed," reports Paul Vroomen, director of consumer products at Zilog. This data suggests that a stock 8-bit MCU with additional arithmetic hardware might just save a lot of people from having to make the 16-bit jump. Now Zilog has decided to test this theory with a part: the Z86C93.

The design starts with what is possibly the fastest—and least appreciated—MCU architecture in the industry. The Z8, introduced years ago with a rich, register-intensive architecture and very fast execution, was ahead of its time in concept and blazingly fast. Today, with 20-MHz parts available, the family is still a performance leader.

The 86C93 uses an existing ROM-less member of the Z8 family, the 86C91 as a core, and adds peripherals to achieve a pin-compatible, fast-math relation. The choice of a ROM-less first product was dictated, according to Vroomen, by market needs. "We see this part as particularly important to the SCSI disk market, where logical-to-physical translations require fast multiplies," he says. "MCUs in this application typically use about 64 kbytes of code, far too much for on-chip ROM, and so most of the parts that go into SCSI disk controllers are ROMless."

To the core, Zilog has added a 16x16 hardware multiply/divide unit. In a 20-MHz part, the new cell can produce a 32-bit product from two 16-bit arguments in 1.7 microseconds, and can come up with the result of a 32x16 divide in 2 micro-

seconds. These figures give the part 16-bit arithmetic performance better than that of most full 16-bit MCUs.

Zilog chose to design the new hardware not as an extension of the Z8 ALU, but as a peripheral device in the part's extended register space. This means that the 86C93 remains code-compatible with other Z8s. A multiplication or division is initiated by putting the arguments into specific general registers via any of the Z8's register-oriented instructions, and then setting a command bit.

In addition to the arithmetic hardware, the 86C93 carries a new set of three timers, all considerably more powerful than those on the predecessor 86C91. One of the new timers can clock at one-half, rather than one-eighth, of the crystal frequency, giving the 86C93 time resolution superior to that of nearly any other 8-bit MCU.

To go with the faster hardware, Zilog felt that a new compiler was in order. "Existing C compilers for the Z8 have been based on the accumulator-oriented model used in other microcontrollers," explains Vroomen. "They didn't really take advantage of the Z8 registers, and so they only delivered about 60 percent of the chip's real performance. Now we've had a compiler developed specifically for the Z8, using the registers properly and even including features like an instruction-use history file that improves code efficiency over time. The vendor claims to be seeing code with 95 percent efficiency."

Another support issue addressed by Zilog is real-time emulation. At 20 MHz, MCUs can be notoriously difficult to emulate. The company has attacked the problem by adding three additional pads on the die to bring out emulation controls.

The 86C93 is sampling now and will go into production in January. The 12-MHz version of the chip, in PLCC, will cost \$4.75 in thousands.

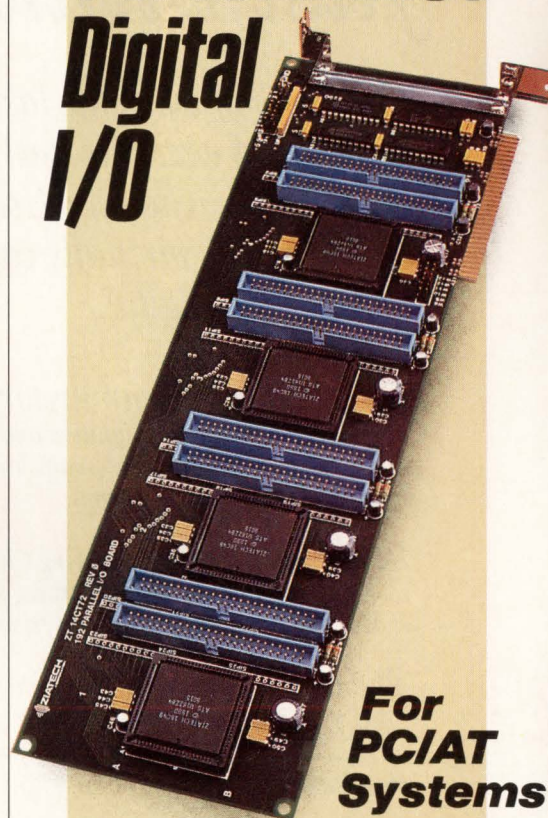
—Ron Wilson

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CIRCLE NO. 29

Just think ...

Just think of what the last 30 years have been like ... and what the next 10 will be the next 10, when the transformation of electronics is virtually complete and the world has become digital.

Distributors and carburetors in automobiles have given way to microprocessor-controlled ignition and fuel-injection systems. By the year 2000, they'll be joined by automatic braking systems, collision avoidance systems, and navigation systems.

Radar, with its simple, sweeping CRT display, has given way to sophisticated digital signal processing systems that can find, identify, characterize and track aircraft in friendly or hostile skies.

The telephone and all its switches have given way to digital PBXs and FAXs, and by the year 2000 will have given way to the integrated digital services network (ISDN), fiberoptic transmission and digital videotelephones.

Music aficionados may deplore the passing of the LP but the Compact Digital Disc and DAT (digital audio tape) have brought a quality and functionality to home entertainment undreamed of in the traditional analog era. Couple this with digital signal processing and listeners will be hearing the real thing by the year 2000.

And when they're not listening to real music, they'll be watching digital television in the form of HDTV or some variation, and interacting with their TVs in a way that will make the distinction between TV and computers a blur.

And at work, in the factory, they'll be supervising computerized machines and robots that displaced older electromechanical controlled and operated tools: they'll be overseeing chemical processes where messages about temperatures and pressures and chemical mixtures are transmitted over digital networks, analyzed and then adjusted to yield optimum products. In hospitals, physicians and nurses will be capturing the tiny signals from spinning or splitting atoms and looking at complex, enhanced images of organs deep inside the human body and at the biological processes going on in those organs.

Just think ... what the last 30 years have been like ... and what the next 10 will be ... the next 10, when the transformation of electronics is virtually complete and the world has become digital.

THE

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SYSTEMS ERA

The Last Thirty Years & The Next Decade

January 1991, Computer Design Celebrates Its 30th Year
With A Major Analysis Of The Systems Era

those brought on by the development of the steam engine, the telegraph, the automobile or the vacuum tube which started the electronics age. What began 30 years ago was the digitization of electronics and, even more important, the digitization of the world we live in.

The next 10 years will see the completion of this digitization of our world.

Computer Design has the unique ability to provide this editorial perspective because it was created with the express purpose of covering the transformation of electronics into digital, computer-based products and systems. **Computer Design** has covered the transformation with 400 consecutive issues dedicated to pointing the way; to looking at

the technology and design directions that were driving the transformation.

The editorial package for this 40-year look at the transformation of electronics —1960 to 2000—is being jointly developed by John Miklosz, **Computer Design's** Associate Publisher/Editor-in-Chief, Stephen Ohr, a well-respected longtime reporter of electronics and computer technology, and the entire **Computer Design** senior technical staff.

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DESIGN AND DEVELOPMENT TOOLS

PCB tool targets high-density, mixed-technology architectures

The latest release of the Crystal Design System, Version 2.1, from Shared Resources adds an engineering change system, 3-D spacing checker and Gerber data viewer and editor to its existing capabilities.

The tool set contains a transmission-line sequencer that sequences nets to multiple rule sets and auto-

corporate wiring and component changes in a completely routed design without rerouting unmodified wires. Changes are incorporated using the transmission line, coupling and length rules from the original design.

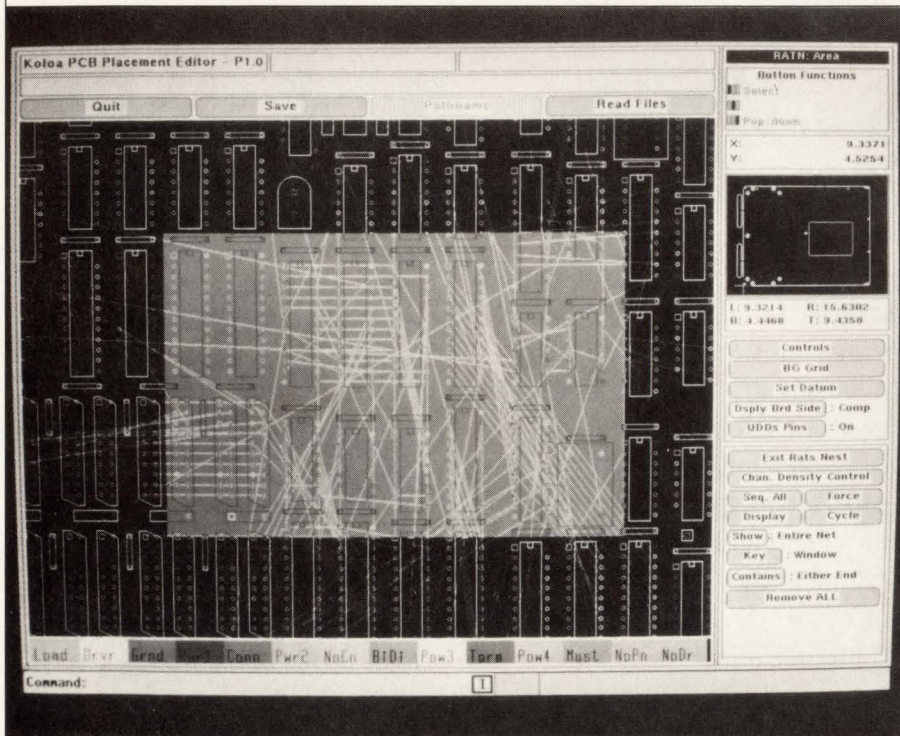
The 3-D spacing checker compares routed Gerber data with spac-

high-density circuit boards, the Crystal Design System can place and route multilayer designs with a component density of up to 200 pins per square inch. The system allows a broad range of technologies to be used in any combination and can handle buried and blind vias. In addition, the tool set features an ECL transmission-line management routing system with a multilayer router that addresses problems in board layout that stem from the dense packaging of pin grid arrays and surface-mount devices.

Crystal's pre-route analysis and transmission-line engineering subsystem can be used interactively with a simulator to ensure that all critical paths are properly managed for time delay and transmission-line structure prior to routing. This assures that routing will comply with transmission-line rules.

The Crystal Design System is available now with prices starting at \$50,000 depending on configuration and platform. Previously only available for Apollo workstations, Version 2.1 offers a port to Sun Microsystems' Sparcstation working under X Windows. Delivery is four weeks after receipt of order.

—Mike Donlin



matically determines the need for multiple values of terminators, including assignments using minimum-length wires. In addition, the system contains a set of database checking routines that test for proper component use and net construction.

Other features let users view a single net or wire and determine its length, view all nets or wires connected to a single component or group of components and view all nets of a given class of wires in a specific area. The tool also allows movement of a component or group of components with automatic resequencing of all nets.

The new engineering change system lets the user automatically in-

ing and clearance rules to ensure that no violations are created. Spacing checks can be simultaneously performed on all circuit layers of a board, including vias, component holes, mounting holes and keep-out areas.

The Gerber viewer and editor lets users view any combination of Gerber layers on a color graphics display. The editor can pan and zoom the circuit board surface and measure feature sizes and clearance with a built-in ruler. Gerber segments can be moved and changed in size as needed to resolve clearance problems. The tool can also be used with the 3-D spacing checker to display areas of spacing violations.

Designed for routing high-speed,

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Circle 352

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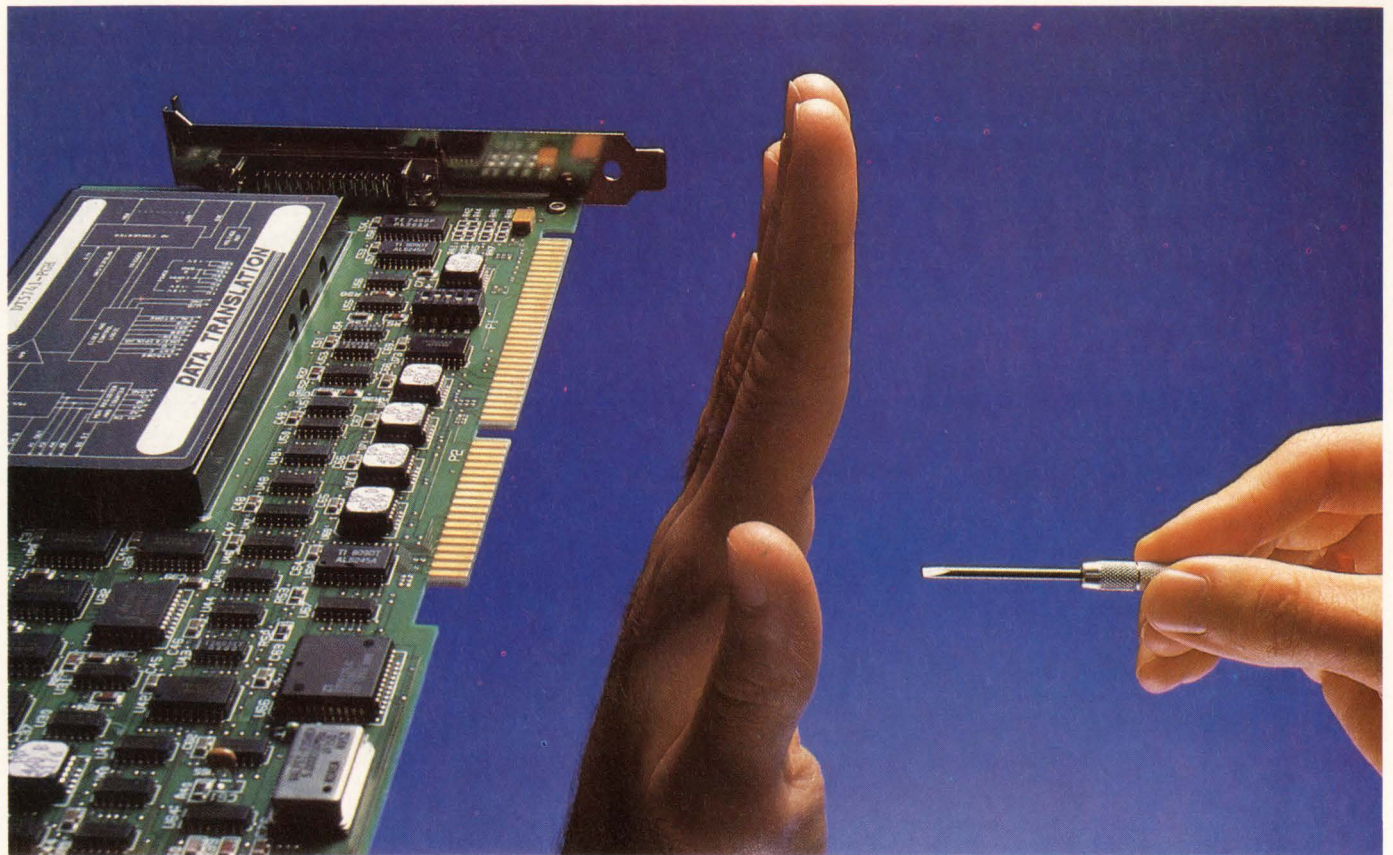
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February 1 Buscon-W	Workstation buses <i>Warren Andrews</i>	FDDI ICs — <i>Ron Wilson</i> Design capture — <i>Mike Donlin</i>	High-speed D-A converters <i>Jeff Child</i>
March 1*	Fuzzy logic in embedded control <i>Tom Williams</i>	Mixed CMOS, ECL & BiCMOS — <i>Barbara Tuck</i> LAN controllers ICs — <i>Ron Wilson</i>	VME CPU boards <i>Jeff Child</i>
April 1 Electro	PCB layout tools <i>Mike Donlin</i>	Communication with standard buses — <i>Warren Andrews</i> Designing ASICs for testability — <i>Barbara Tuck</i>	Static RAMs <i>Jeff Child</i>
May 1* CICC Comdex	Superfast processors <i>Ron Wilson</i>	High-level design languages — <i>Mike Donlin</i> Object-oriented programming — <i>Tom Williams</i>	Emulators <i>Jeff Child</i>
June 1 DAC	Design synthesis <i>Barbara Tuck</i>	Mil-Spec standard buses — <i>Warren Andrews</i> Disk controller ICs — <i>Ron Wilson</i>	Op amps <i>Jeff Child</i>
July 1	CASE for real-time programming <i>Tom Williams</i>	Mezzanine buses — <i>Warren Andrews</i> Device modeling — <i>Mike Donlin</i>	Multibus CPU boards <i>Jeff Child</i>
August 1* Siggraph	Mixed-signal ASICs <i>Barbara Tuck</i>	Display controller ICs — <i>Ron Wilson</i> Software-management tools — <i>Tom Williams</i>	DRAMs <i>Jeff Child</i>
September 2 Buscon-E ESC	Enhanced-performance standard buses <i>Warren Andrews</i>	CAD frameworks — <i>Mike Donlin</i> RISC in real-time — <i>Tom Williams</i>	Device programmers <i>Jeff Child</i>
October 1*	32-bit microcontrollers <i>Ron Wilson</i>	Fast PLDs — <i>Barbara Tuck</i> RISC-based CPU boards — <i>Warren Andrews</i>	Flash EPROMs <i>Jeff Child</i>
November 1 Wescon ITC	System simulation and verification <i>Mike Donlin</i>	High-density ASIC packaging — <i>Jeff Child</i> Multiprocessing in real-time — <i>Tom Williams</i>	STD CPU boards <i>Jeff Child</i>
December 2	Migrating PLDs to full ASICs <i>Barbara Tuck</i>	Accelerators to boost standard-bus performance <i>Warren Andrews</i> 8- and 16-bit microcontrollers — <i>Ron Wilson</i>	High-resolution A-D converters <i>Jeff Child</i>

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SOFTWARE

Image scaler/rotator teams with software in development toolkit

A single-chip image scaling and rotation engine has been teamed with a software toolkit to allow designers to develop electronic document imaging systems. The Bt710 orthogonal rotator/scaler chip from Brooktree incorporates an algorithm that can scale bi-level (2-bit) images to produce a 4-bit gray scale result. The value of gray scale document images is that on gray scale and color monitors, a gray scale image has the effect of anti-aliasing the image and thus shows enhanced image quality.

The Bt710 provides autonomous operation by means of two DMA channels that manage read operations from source buffers and write operations to destination buffers.

The DMA channels lend themselves to the data-flow-intensive nature of scaling and rotation as opposed to the instruction flow orientation of conventional processors. Once the Bt710 is pointed to the beginning of a source buffer, it will read the source data, rotate and scale the image, and write it to the destination buffer until the task is complete. In addition to reducing CPU overhead, the DMA feature makes it possible to do continuous operations in a system where the main CPU may have to respond to random interrupts.

Scaling range

The Bt710's scaling range is from approximately 6 percent scale down to 760 percent scale up from the original size. In addition to scaling, the chip can perform orthogonal rotation, cropping and bitblt (bit boundary block transfers) for precise placement of images in frame buffers. During the scaling process, the Bt710 computes a 4-bit gray scale value that indexes a lookup table. The lookup table can be 1-, 4- or 8-bit pixels. By loading appropriate values in the lookup table, certain global operations such as inversion can be performed instantly.

To aid system developers with design and prototyping of peripherals as well as applications, Brooktree has also announced PixelVu, an open architecture imaging software

toolkit that can emulate the functions of the Bt710 exactly, albeit much more slowly. PixelVu is a set of C routines that can be called by the developer's program. In addition to scaling and rotation operations ala the Bt710, PixelVu can also compress and decompress images according to CCITT Group 3, 1D, 2D, and Group 4 image standards.

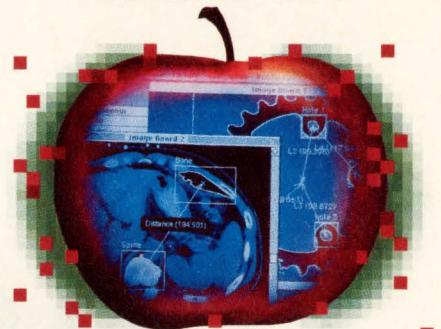
PixelVu is designed to be portable and is available for three different platform environments: MS-DOS and Microsoft Windows 3.0, Macintosh under Quickdraw, and Sun platforms running X-Windows and Sun Unix. In addition, PixelVu aims at device independence by using object-oriented programming structures to support devices and system resources. An image is obtained from some image object (such as a scanner object or a file object), manipulated and sent to another image object (such as a display). The base toolkit contains many standard objects, and additional devices can be supported via user-defined custom image objects.

Brooktree is also supplying a Bt710 evaluation kit that consists of an AT add-in board containing the Bt710, demonstration software and documentation. The evaluation kit is priced at \$995. The Bt710 chip itself is currently sampling and is available now at a (100-piece) quantity price of \$132. The PixelVu developer's kit—the software toolkit—for the PC platform to run under MS-DOS and Windows 3.0 is priced at \$1,990; the Macintosh version is priced at \$2,490; and the Sun Unix/X-Window version is priced at \$2,290. —Tom Williams

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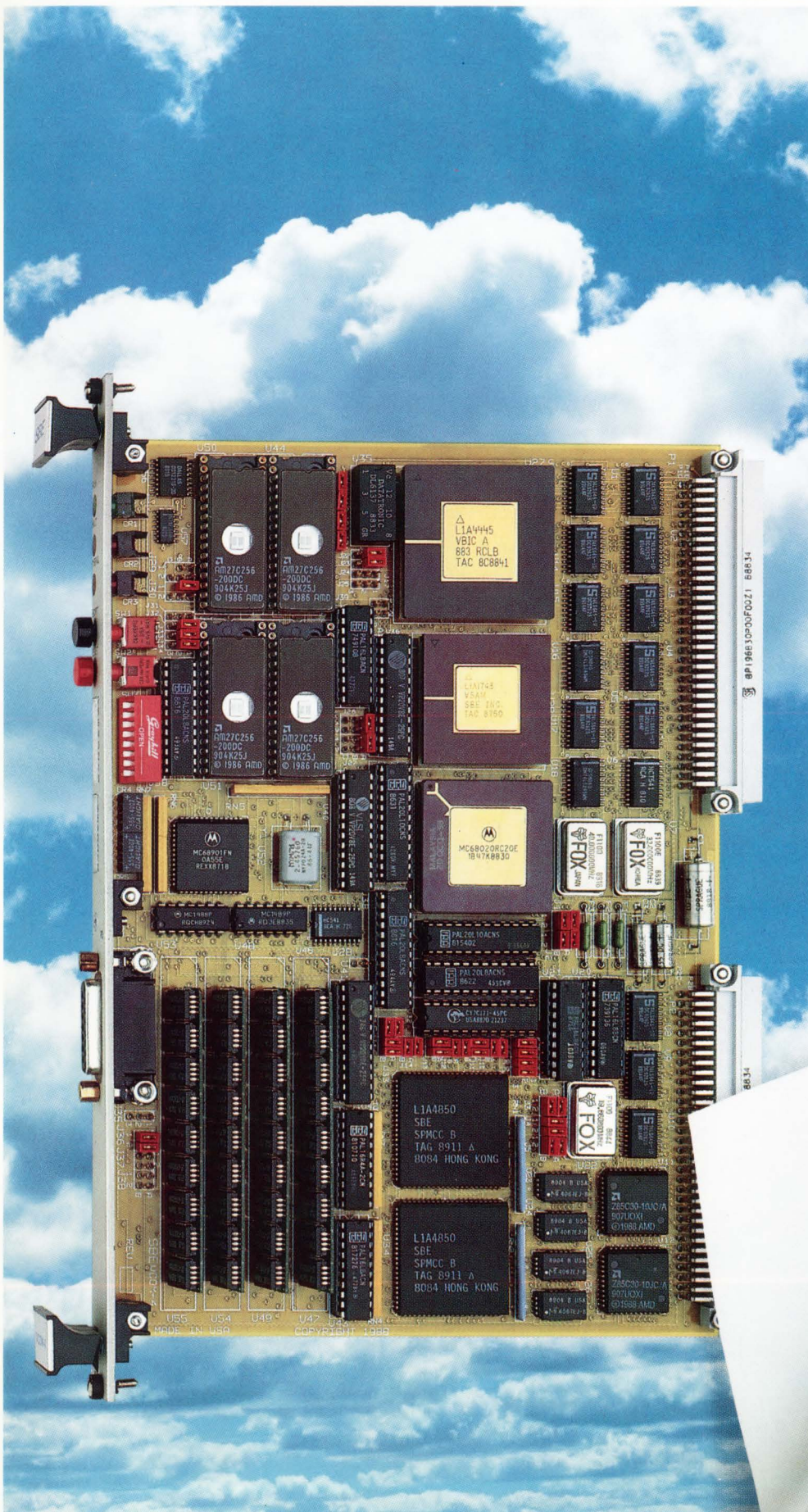
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