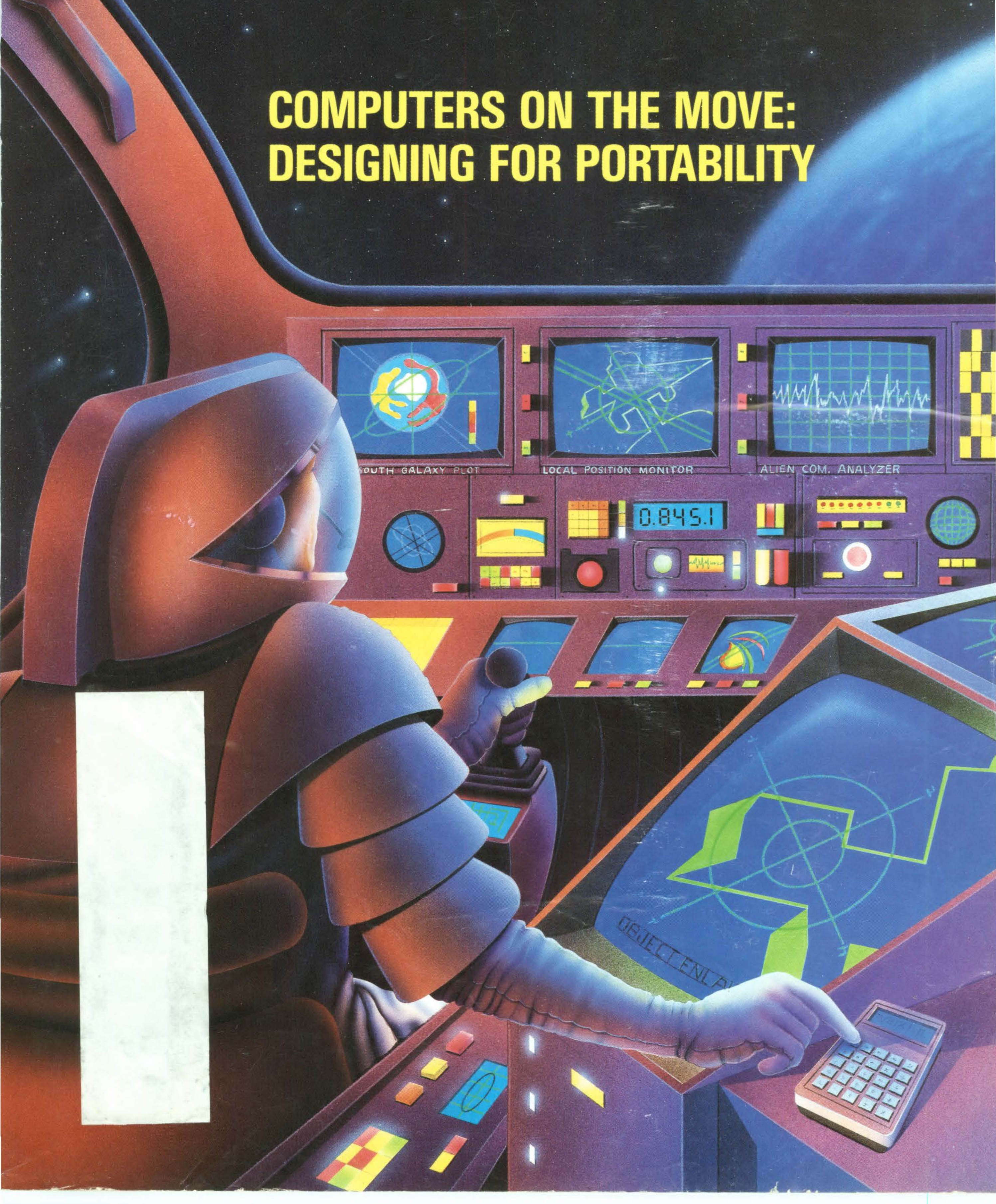
A PennWell Publication

COMPUTER DESIGN

JULY 1988

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

COMPUTERS ON THE MOVE: DESIGNING FOR PORTABILITY



New Simple To Use Network Expands Power of STD Systems

Turnkey industrial networking for STD Bus and personal computers

Z-NET is a complete, simple to use network for industrial applications. Z-NET extends the capabilities of Ziatech's PC DOS-based STD Bus systems by allowing them to share information and resources with other STD systems and IBM-compatible personal computers.

ARCNET hardware protocol, ViaNet software

Ziatech's STD and PC network controllers are based on the well-established ARCNET protocol, and are supported by ViaNet, a software package from Western Digital that makes using the network as easy as making simple DOS calls.

Remote control for embedded systems

Z-NET was designed to meet the specific network needs of industrial STD Bus computers, which are typically unattended or embedded in equipment. Z-NET makes an ideal sub-network in a large factory or a total solution for smaller applications.

Ziatech's exclusive Virtual Network Console (VNC) lets a network manager control a remote node from his local STD or PC console. VNC capabilities let operators remotely reboot a node and remotely execute or download programs, eliminating the need for PROM installation or replacement.

A single network source

Z-NET is a complete network solution for industrial STD and personal computers, available now from an established source. The necessary hardware, software, cables, documentation, and applications support are all available from Ziatech, a leading manufacturer of STD Bus and IEEE 488 products.

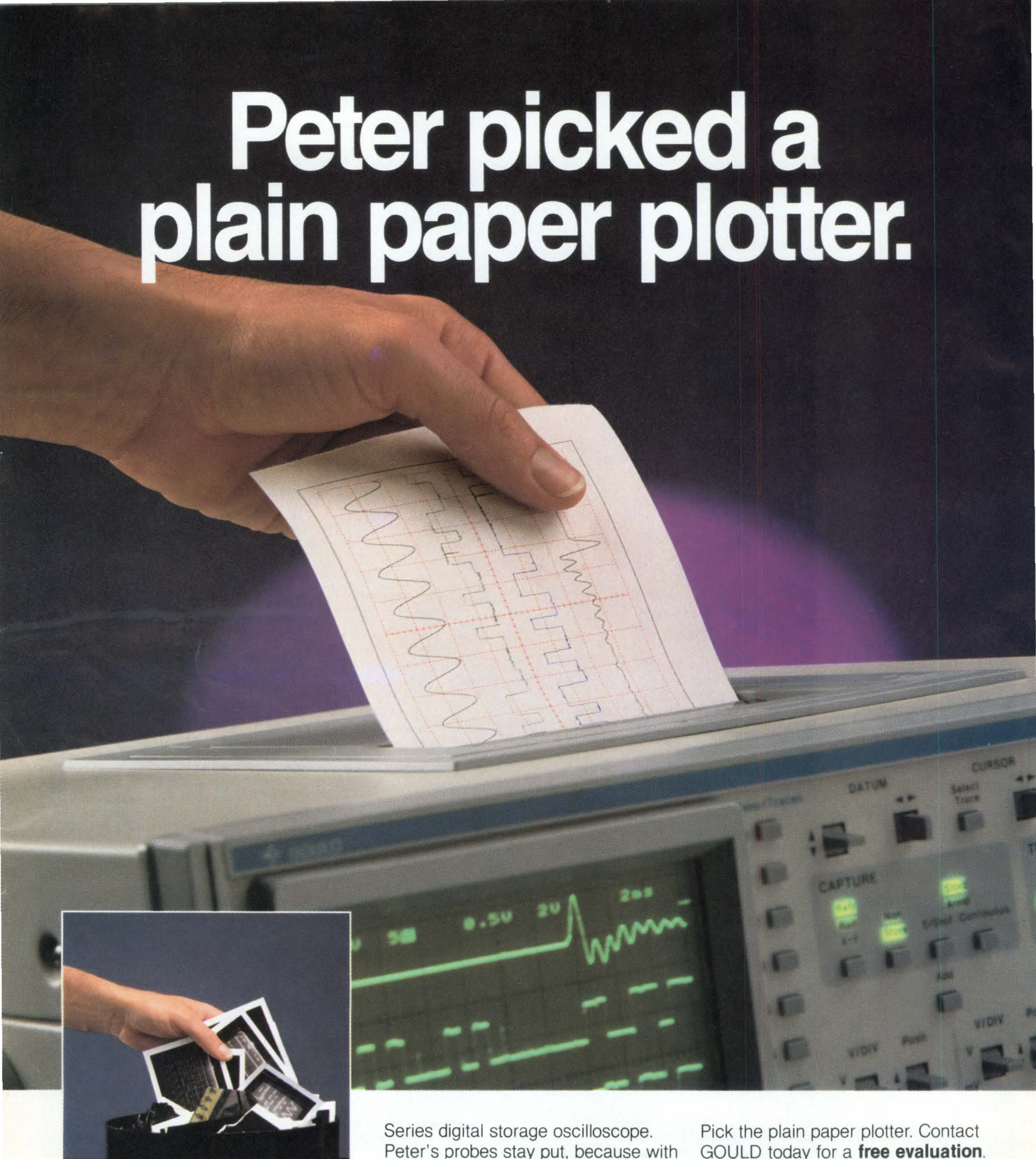
Free industrial networking guide

For a complete technical brochure and configuration guide to a complete STD and PC network, call Ziatech today. **(805) 541-0488**

ZIATECH CORPORATION

3433 Roberto Court
San Luis Obispo, CA 93401 USA
ITT Telex 4992316
FAX (805) 541-5088
Telephone (805) 541-0488

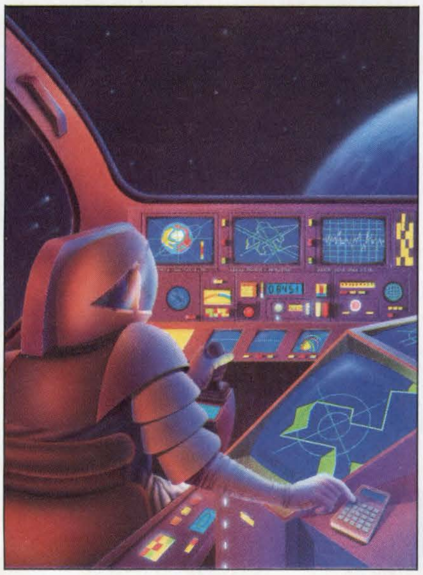
ARCNET is a registered trademark of Datapoint Corporation.
ViaNet is a registered trademark of Western Digital Corporation.
PC DOS and IBM are registered trademarks of International Business Machines, Incorporated.


Peter picked a
plain paper plotter.
DATUM
CURSOR
CAPTURE

Vol 27, No. 13 July 1988

COMPUTER DESIGN®

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION



This issue's cover was designed by Sergio Roffo.

SPECIAL REPORT ON DESIGNING FOR PORTABILITY

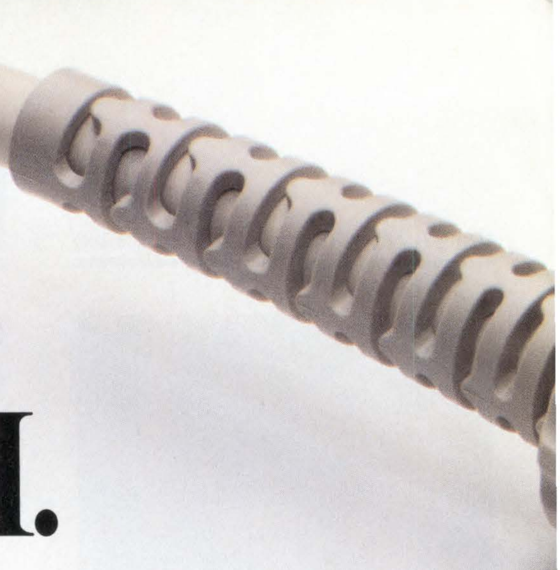
SYSTEM TECHNOLOGY

SYSTEM PRODUCTS

DEPARTMENTS

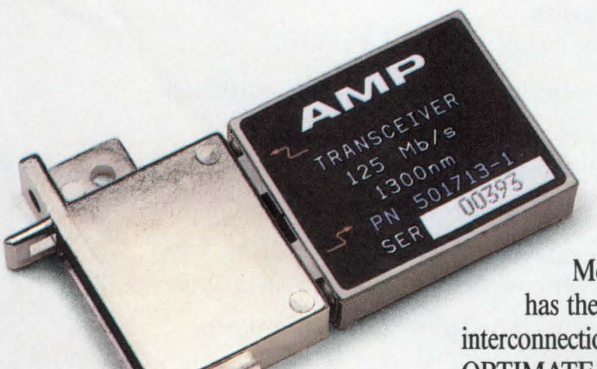
COMPUTER DESIGN© 1988 (ISSN-0010-4566) is published twice monthly, except one issue in July and December, by the Advanced Technology Group of PennWell Publishing Company, PO Box 417, 119 Russell St., Littleton, MA 01460. Second-class postage paid at Tulsa, OK 74112. Rates for non-qualified subscribers: $70 in U.S.A. and $95 elsewhere. Single-copy price is $6.00 in U.S.A. and $8.50 elsewhere. SUBSCRIPTION INQUIRIES: (918) 831-9401, 8 am-5 pm E.S.T.

POSTMASTER: Send change of address form 3579 to COMPUTER DESIGN, Circulation Department, Box 3466, Tulsa, OK 74101 (USPS 127-340).



FDDI.

From deskwork to network.

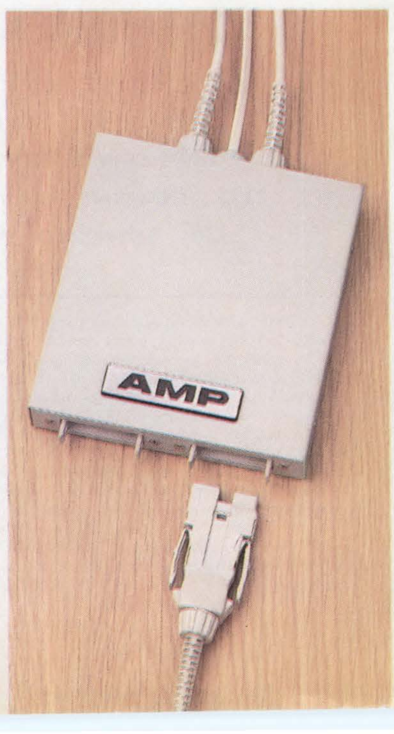


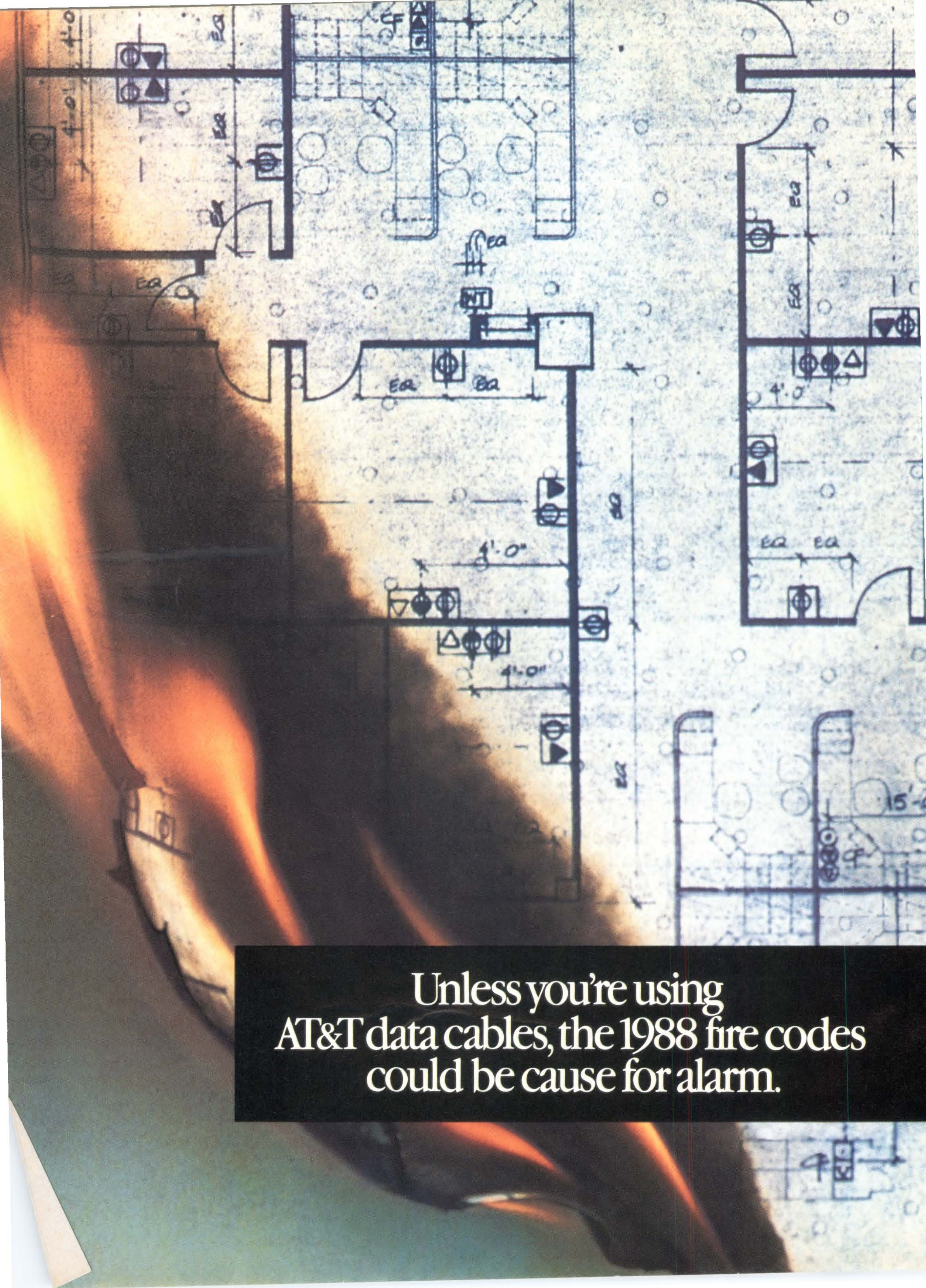
Good news for networks!

<u>The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document</u>.

More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

Of special note: the transceiver —the first of its kind—is capable of operating at data rates up to 125 Mb/s. Available in standard or raised (+5v) ECL logic, it gives you a compact, board-mount data link in a single 24-pin module. Reliable duplex mating and electro-optic conversion are now easier than ever.




Unless you're using
AT&T data cables, the 1988 fire codes
could be cause for alarm.

IF YOU'RE DESIGNING DISK DRIVES AND HAVE ONLY USED OUR READ/WRITE CIRCUITS- THIS CHART IS FOR YOU.

Our Extended Family

If you're designing disk drives, you're probably already familiar with Silicon Systems. Chances are good that you are presently using one or more of Silicon Systems' Read/Write amplifier IC's in your HDD designs. But maybe you don't know that we also offer the industry's most extensive line of mass storage ASIC's.

The adjacent chart illustrates that Silicon Systems can also provide more than a score of circuits for pulse detection, data recovery, head positioning, spindle motor control, and controller electronics. And the list continues to grow.

The Mix-and-Match Design Approach

With Silicon Systems growing families of IC's for all the electronic functions in hard disk drives, many leading HDD designers are finding they can now easily mix-and-match SSi products to implement their specific design features. This powerful design approach allows them to reduce board area, eliminate external passives, and lower costs by simplifying their designs.

Call Now!
(714) 731-7110, Ext. 575

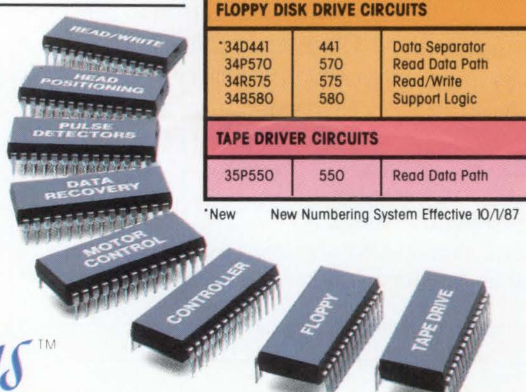
For more information, send for our Disk Drive mailers. **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680.

MICROPERIPHERAL IC SELECTION CHART

SSI Device Numbers		Head Type	# of Channels	Max Input Noise nV/√Hz	Max Input Capacitance (pf)	Read Gain (typ)	Write Current Range (mA)	Power Supplies	Read/Write Data Port(s)
New	Old								
HDD READ/WRITE AMPLIFIERS									
32R104B	104	Ferrite	4	2.4	23	35	15 to 45	+6V, −4V	Differential, Bi-directional
32R104BLN	104L	Ferrite	4	1.7	23	35	15 to 45	+6V, −4V	Differential, Bi-directional
32R114	114	Thin Film	4	1.1	65	123	55 to 110	±5V	Differential/Differential
32R115	115	Ferrite	2, 4, 5	1.8	20	40	30 to 50	±5V	Differential, Bi-directional
32R117	117	Ferrite	2, 4, 6	2.1	•23	100	10 to 50	+5V,+12V	Differential/TTL
32R117A	117A	Ferrite	2, 4, 6	1.7	20	100	10 to 50	+5V,+12V	Differential/TTL
32R188	188	Ferrite	4	2.4	18	43	35 to 70	+6V, −5V	Differential, Bi-directional
32R501	501	Ferrite	4, 6, 8	1.5	23	100	10 to 50	+5V,+12V	Differential/TTL
*32R510A	510A	Ferrite	2, 4, 6	1.5	20	100	10 to 40	+5V,+12V	Differential/TTL
*32R511	511	Ferrite	4, 6, 8	1.5	20	100	10 to 40	+5V,+12V	Differential/TTL
*32R512	512	Thin Film	8	0.9	32	150	10 to 40	+5V,+12V	Differential/TTL
*32R514	514	Ferrite	2, 4, 6	1.5	20	150	10 to 40	+5V,+12V	Differential/TTL
32R520	520	Thin Film	4	0.9	65	123	30 to 75	±5V	Differential/Differential
32R521	521	Thin Film	6	0.9	65	100	20 to 70	+5V,+12V	Differential/TTL
*32R522	522	Thin Film	4, 6	1.0	32	100	6 to 35	+5V,+12V	Differential/TTL

SSI Device Numbers		Circuit Function	Features
New	Old		
HDD PULSE DETECTION			
32P540	540	Read Data Processor	Time Domain Filter
32P541	541	Read Data Processor	AGC, Amplitude & Time Pulse Qualification, RLL Compatible
HDD DATA RECOVERY			
32D531	531	Data Synchronizer	Data Synchronizer/Write Precompensation
*32D532	532	Data Separator	Data Synchronizer/2, 7 RLL ENDEC
*32D533	533	Data Synchronizer	Data Synchronizer/Write Precompensation
*32D534	534	Data Separator	Data Synchronizer/MFM ENDEC/Write Precompensation
*32D535	535	Data Separator	Data Synchronizer/2, 7 RLL ENDEC/Write Precompensation
HDD HEAD POSITIONING			
32H101A	101A	Preamplifier-Ferrite Head	AV = 93, BW = 10MHz, e_n = 7.0nV/√Hz
32H116	116	Preamplifier-Thin Film Head	AV = 250, BW = 20MHz, e_n = 0.94nV/√Hz
*32H567	567	Servo Demodulator	Di-bit Quadrature Servo Pattern: PLL Synchronization
*32H568	568	Servo Controller	Track & Seek Mode Operation; Microprocessor Interface
*32H569	569	Servo Motor Driver	Head Parking, Spindle Motor Braking
HDD SPINDLE MOTOR CONTROL			
32M590	590	2-Phase Motor Speed Control	±0.035% Speed Accuracy; Unipolar Operation
32M591	591	3-Phase Motor Speed Control	±0.05% Speed Accuracy; Unipolar Operation
*32M593	593	3-Phase Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation
HDD CONTROLLER/INTERFACE			
*32B450A	450A	SCSI Controller	Async transfer to 2MBPS; Initiate/Target Modes; Internal Drivers; CMOS
*32C452	452	Storage Controller	20Mbits/sec; CMOS; Programmable; AIC-010 Compatible
*32C453	453	Buffer Controller	Non-mux addressing to 16K; CMOS; AIC-300 Compatible
32B545	545	Support Logic	Includes ST506 Bus Drivers/Receivers
FLOPPY DISK DRIVE CIRCUITS			
*34D441	441	Data Separator	High Performance Analog Data Separator, NEC 765 Compatible
34P570	570	Read Data Path	2 Channel Read/Write With Read Data Path
34R575	575	Read/Write	2, 4 Channel Read/Write Circuit
34B580	580	Support Logic	Port Expander, Includes SA400 Interface Drivers/Receivers
TAPE DRIVER CIRCUITS			
35P550	550	Read Data Path	4 Channel Read/Write With Read Data Path

*New New Numbering System Effective 10/1/87



CIRCLE NO. 6 FOR PRODUCT INFORMATION
CIRCLE NO. 7 FOR CAREER INFORMATION

silicon systems™
INNOVATORS IN INTEGRATION

"Where we design to your applications."

UP FRONT

Supercomputer token ring network breaks 1-Gbyte/s barrier

Rather than being used in isolation, supercomputers usually form the nucleus of computing networks that include other mainframes, superminis and workstations. As the interactivity of applications increases, these supercomputer networks require communications bandwidths much greater than those available from Ethernet. Now supercomputer vendor Scientific Computer Systems (San Diego, CA) offers a solution: a 1.4-Gbyte/s token ring network. The new scheme, called Vectornet, rests on an interface processor to provide gateways to existing LANs, and on an ECL-based interface adapter to permit direct connection of computing equipment to the network. The network medium can be either optical fiber or copper cable.—*Ron Wilson*

VLSI chip speeds Phong shading in 3-D workstation

Phong shading adds realism to three-dimensional solids modeling by giving the impression of truly curved surfaces that can reflect multiple light. It's especially known for its rendering of specular highlights, such as the "twinkle" when incident light reflects directly at the eye. But Phong shading, which can also model multiple light sources, requires a complex lighting calculation for every pixel. Seiko Instruments (San Jose, CA) has now developed a shading engine for its GR4000 series of 3-D display systems that does Phong shading in hardware. The shading engine is based on Seiko's new pixel rendering engine (PRE) chip. In addition to doing the Phong lighting equation, the chip performs hidden surface removal based on pixel values stored in the system's Z-buffer. The shading engine uses two PREs and can do lighting calculations at the rate of 60,000 pixels/s. The chip is designed to be ganged in parallel, offering the possibility of much larger and faster shading hardware in the future.—*Tom Williams*

DEC favors fiberoptics for the factory LAN backbone of the future

Digital Equipment Corp (Maynard, MA), which claims that most installed LANs are based on Ethernet, has long been promoting its Ethernet as the available LAN in lieu of those based on the Manufacturing Automation Protocol/Technical and Office Protocol chosen for new installations by MAP/TOP organizations. Now, in its push to be the major force in factory LANs, DEC has selected the MAP/TOP-sponsored Enterprise Networking Event '88 to announce its choice of fiberoptics as the backbone medium for future factory LANs. DEC will develop products to bridge its 10-Mbit/s Ethernet LANs to the 100-Mbit/s fiberoptic backbone evolving as the Fiber Distributed Data Interface (FDDI). By integrating the company's DECconnect system with FDDI, up to 100 Ethernet LANs—each with up to 1,024 attached devices—can be interfaced to a fiberoptic backbone, according to Karl Pieper, extended LAN marketing manager.—*Sydney Shapiro*

National Semiconductor becomes an EDA vendor

With the introduction of its DA4 design system, National Semiconductor (Santa Clara, CA) has taken the plunge into the electronic design automation business. The DA4 system includes schematic entry, design

(continued on page 10)

 (continued from page 9)

analysis, critical path analysis, behavioral simulation, fault simulation, automatic test vector generation, and automatic placement and routing. By signing an OEM agreement with Gateway Design Automation (Westford, MA) for the Verilog simulator, National becomes the first application-specific IC vendor to sell a commercial, foundry-independent logic simulator. National also announced an agreement with Vantage Analysis Systems (Fremont, CA) to develop simulation models in the VHSIC Hardware Description Language.—*Richard Goering*

PS/2: poised to reverse the trend of standalone computing?

If a recent report by the International Technology Group (Los Altos, CA) is correct, IBM's Personal System/2, OS/2 and Micro Channel architecture will be "interim offerings" that will gradually help "reverse the trend toward standalone desktop computing." According to the report, PS/2 Models 25, 30 and 50 will eventually merge with a current line of dumb ASCII terminals as IBM's products evolve into a host coprocessing environment intended to return firm control of an organization's computing activities to MIS managers—IBM's traditional customers. The report also suggests that Models 60 and 80 will merge with IBM's midrange systems. Model 80 will function as a bridge from the OS/2 environment to the 9370 and to IBM's newest intended "DEC-killer," the S/3X, or "Silverlake."—*David Lieberman*

Motorola pushes 68030 clock to 33 MHz

Motorola Microprocessor Products Group (Austin, TX) will release in August a 33-MHz version of the 68030 microprocessor. The announcement, coming soon after the introduction of Motorola's 88000 reduced-instruction-set CPU, should assure users of the 68000 family that the older complex-instruction-set computing architecture will continue to benefit from speed enhancements. Although 33-MHz operation puts severe strain on bus design and memory access time, the new part will still offer 68000 users an easy upgrade path, compared to a switch to the 88000. One such user, Hewlett-Packard (Palo Alto, CA), has already announced plans to incorporate the 33-MHz part in a new Series 9000 workstation.—*Ron Wilson*

CAD framework initiative unites EDA vendors

In a rare show of cooperation, electronic design automation vendors and major end-users have kicked off an effort to develop an open CAE/CAD environment. The CAD Framework Initiative (CFI) is searching for user-interface, data-modeling and data-management techniques that will let tools coexist in multivendor environments. CFI is supported by 38 organizations from the end-user community, government, research and academia, as well as from the design-automation, computer and semiconductor industries. A steering committee includes representatives from Cadence Design Systems, Digital Equipment Corp, EDA Systems, Hewlett-Packard, Honeywell, Mentor Graphics, Motorola and Valid Logic Systems.—*Richard Goering*

Microfilm copies of COMPUTER DESIGN are available and may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Rd., Ann Arbor, MI 48106. Officers of PennWell Publishing Company, 1421 S. Sheridan, Tulsa, OK 74101; Philip C. Lauinger, Jr., Chairman and Chief Executive; Joseph A. Wolking, President; L. John Ford, Senior Vice President; Carl J. Lawrence, Senior Vice President; V. John Maney, Vice President/Finance.

When it comes to ASICs, you need more than technology that works.

You need a partne

No one can sol but we solve

Everyone thought gate arrays would be a great solution to their semi-custom design needs. Then they designed one and discovered that "semi-custom" translated into "expensive," "time consuming" and "risky."

The solution to the solution.

Meet the Logic Cell™ Array—the first Programmable Gate Array. It's a high density CMOS chip of unmatched technology that's user programmable where it's easiest for you to program—in software.

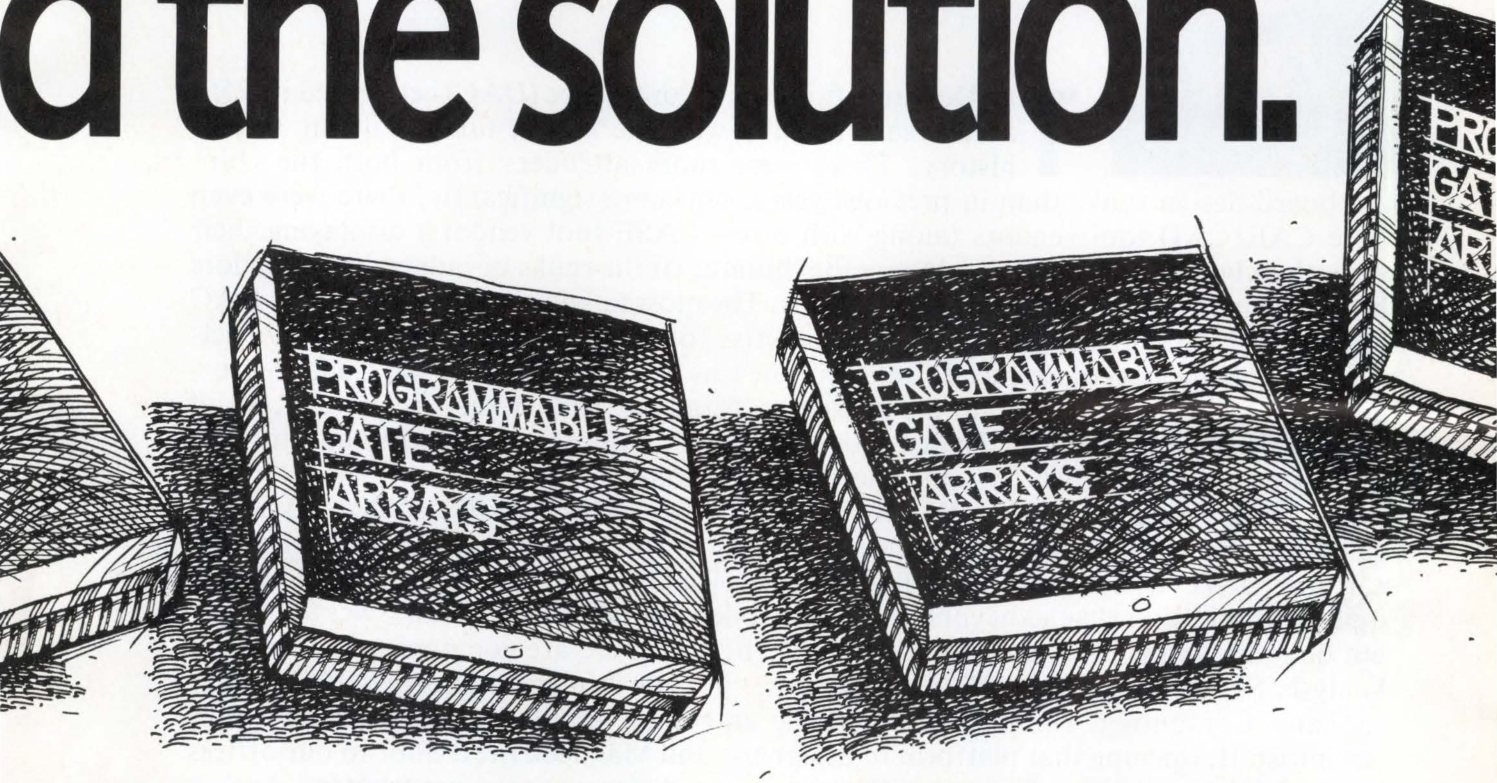
Your development cycle is cut to a week or two instead of six months. So you can get your product to market that much sooner.

PGAs let you spot system problems before they become a real headache. No more risking large sums of money and time to verify your design in hardware. And if you need to change your design you can do it in a matter of minutes. Not months. And you won't have to spend any more money.

9000 ways to get ahead of schedule.

The Am2000 series has densities from 1000 to 2000 usable gates and the Am3000 series has densities from 2000 to 9000 usable gates. With those densities (we'll have even higher densities later), you need fewer parts to get the same functions as

ve the problem,
d the solution.



EPLDs or discrete logic.

There is no other PGA technology available today. And over 5000 designers are already using it.

Even getting started is easy.

Your investment is minimal. You don't have to finance months of NRE. You can get started for the price of a PC (which you probably already have) and some software.

PGAs are the epitome of the just-in-time product. They are the only gate arrays stocked in production quantities at your distributor. And they're programmable instantly. Which means you can go from design to production as fast as you need to. Even overnight.

See for yourself.

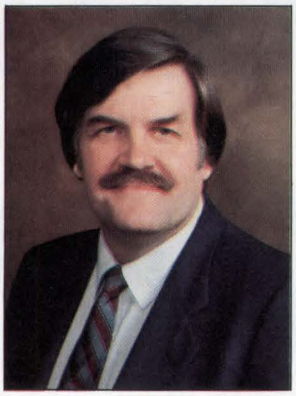
Contact us for a free diskette that gives you a detailed product overview, an interactive session where you can plug in your own design criteria and find out how PGAs can help your design. Part of the PGA development software is included so you can get started saving time and money right away.

Just call (800) 222-9323. Or drop us a line.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

CIRCLE NO. 10



Bigger and better; fewer, but more

The Design Automation Conference (DAC) celebrated its 25th anniversary in June with the largest turnout in the show's history. There were more attendees from both the chip- and board-design ranks than in previous years, but more significantly, there were even more CAE/CAD tool vendors (along with a few CASE tool vendors) displaying their wares than before. And this was despite the thinning of the ranks of independent vendors through some recent mergers and acquisitions. The most talked about acquisition at DAC was probably that of HHB Systems by Cadnetix, following, as it did, hard on the heels of HHB's acquisition of Simucad. But everyone was also interested in what Cadence (formerly ECAD and SDA) was up to, as well as Teradyne/Aida/Case Technology, Valid Logic/Telesis/Calma, Zycad/Endot and, of course, Mentor Graphics, with the remnants of Tektronix's failed CAE Systems and CASE efforts.

The vendors' ranks never really get thinned, however, because like soldiers in a holy war, there will always be venturesome souls ready to fill an empty space. Relatively new startups, such as Synopsys and Silc Technologies, for example, have entered the field with logic-synthesis tools that go beyond silicon compilers, once touted as the answer to the system designer's prayers about chip design. Then, too, there are companies like Vantage Analysis Systems, giving VHDL a push with its full implementation of IEEE-1076; Capilano Computing, running its schematic entry and simulation tools on an Apple Macintosh II, opening that platform to designers; and Massteck (next door to our offices here in Littleton, MA), offering another new printed circuit board autorouter.

Mergers and acquisitions are a mixed blessing because they often limit a user's choices. A perfect example of this is the Cadnetix/HHB merger and the effect it will have on the users of third-party CAE tools that had incorporated HHB's Cadat simulator. Odds are, these third-party vendors will have to switch simulators and, in turn, so will the users. On the plus side, mergers and acquisitions generally result in a product mix—along with the support—that simplifies the integration of the varied tools needed to fully automate the chip- or board-design process.

But perhaps a more significant plus to mergers and acquisitions is that they recycle venture capital, much of it finding its way into new CAE/CAD startups. What's more, they recycle people, providing the entrepreneurial, engineering and management talent at the core of most new CAE/CAD startups. With a life cycle like this for money and talent, there will always be an abundance of choices, and DAC is sure to grow even bigger—in both attendees and vendors—for some time to come.

John Miklosz

John C. Miklosz
Associate Publisher/Editor-in-Chief

How To Wring Workstation-Level PCB Designs Out Of Your PC.

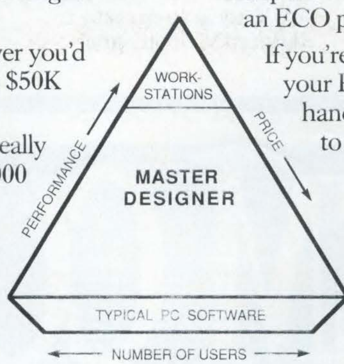
P-CAD's new Master Designer turns an ordinary PC into a full-fledged PCB workstation.

When you need to wring every drop of performance out of your next PCB design, you need Master Designer™ software.

Master Designer provides all the horsepower you'd expect only from workstations priced from $50K up to as much as $200K.

With Master Designer you can tackle the really big jobs. Board designs with 500 EICs, 32,000 pins and 2,500 nets are just the beginning.

P-CAD's Master Designer routes multiple layers simultaneously cutting the number of vias and unrouted subnets in half. So, you'll wring out cleaner designs and higher completion rates (up to 100%).



For forward annotation of logic changes and "history independent" back annotation, Master Designer also has an ECO processing option.

If you're interested in wringing every penny out of your PCB design station instead of wringing your hands, ring P-CAD. Let P-CAD show you how to turn a PC into a high-powered workstation.

p-cad®
PERSONAL CAD SYSTEMS INC.

1290 Parkmoor Ave., San Jose, CA 95126 USA
Telex: 371-7199 FAX: 408-279-3752

800-628-8748 CA 800-523-5207 U.S.

CIRCLE NO. 11

Tandem's powerful NonStop VLX™ computer systems are packed with proprietary technology. Including bi-polar and CMOS gate array logic designed with Tandem's own CAD system. When it came to connecting it all, however, Tandem chose to rely on interconnection specialists: Teradyne Connection Systems.

WE NEEDED CONNECTION TECHNOLOGY AS SOPHISTICATED AS OUR DEVICE TECHNOLOGY.

"We needed connection technology every bit as sophisticated as our VLSI technology," says Larry Laurich, V.P. of the Transaction Systems Division at Tandem. "And Teradyne's High Density Plus™ backplane system solves many of the

THE MODULAR DESIGN OF HIGH DENSITY PLUS PROVIDES THE FLEXIBILITY WE NEED.

problems associated with interconnecting VLSI. Everything from controlled impedance and low inductance to preserve signal integrity, to high contact density and solid power and ground returns."

"On top of all that, Teradyne's modular design provides the

High Performance, High Density: 700+ equivalent signal contacts help Tandem interconnect advanced VLSI circuitry.

TANDEM CONNECTS

COMPUTER DESIGN®

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

PUBLISHER
David L. Allen

ASSOCIATE PUBLISHER/EDITOR-IN-CHIEF:
John C. Miklosz

TECHNOLOGY EDITORS:
Ron Wilson, *Integrated Circuits* (Portland)
Richard Goering, *Design & Development Tools* (Santa Clara)
David Lieberman, *Computers & Computer Subsystems*
Tom Williams, *Graphics & Imaging* (Santa Clara)
John H. Mayer, *Computers & Computer Subsystems*
Sydney F. Shapiro, *Data Acquisition & Control*

CONTRIBUTING EDITORS:
Warren Andrews, *Integrated Circuits*
S. Louis Martin, *Integrated Circuits*
Howard Falk, *Software*
Art DeSena, *Testing & Manufacturing*

RESEARCH/SPECIAL PROJECTS MANAGER:
Sydney F. Shapiro

SECTION/SPECIAL PROJECT EDITORS:
Ron Wilson, *System Technology*
David Lieberman, *System Design*
Michael G. Donlin, *System Products*
Patti Villandry, *Directories*

MANAGING EDITOR: Susan R. Nykamp

COPY EDITORS: Richard Dagley, Kerstin L. Rosenquist, Barbara-Ann Scofidio

EDITORIAL ASSISTANTS: Claire Coupal, Claire Ellis

WEST COAST OFFICES
MANAGING EDITOR: Tom Williams
3333 Bowers Ave, Suite 100
Santa Clara, CA 95054, Tel: (408) 982-0288
1111 S.W. Gaines, No. 8
Portland, OR 97201, Tel: (503) 224-9396

MARKETING SERVICES MANAGER: Mary M. Gregory
CIRCULATION DIRECTOR: Robert P. Dromgoole

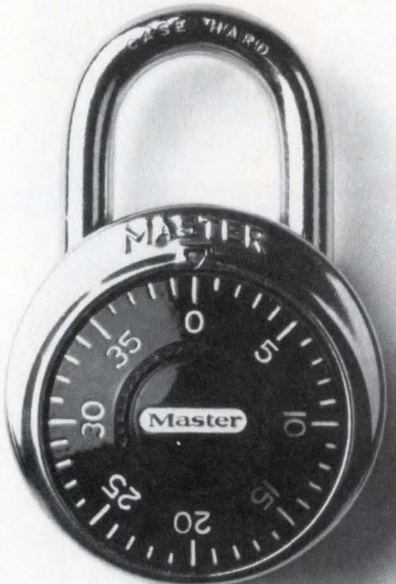
ART DIRECTOR: Jan Horner
ILLUSTRATOR: Christopher Hipp

PRODUCTION DIRECTOR: Jan M. Lopez
PRODUCTION MANAGER: Mari Rodriguez
ADVERTISING COORDINATOR: Shari L. Hasche
COMPOSITION MANAGER: Holly Kersey

PennWell
PUBLISHING COMPANY

Advanced Technology Group
L. John Ford, Senior Vice-President
P.O. Box 417
119 Russell St, Littleton, MA 01460
Tel: (617) 486-9501

PHASE LOCK LOOP. ANALOG/DIGITAL ASIC.



NO ONE ELSE HAS THE COMBINATION.

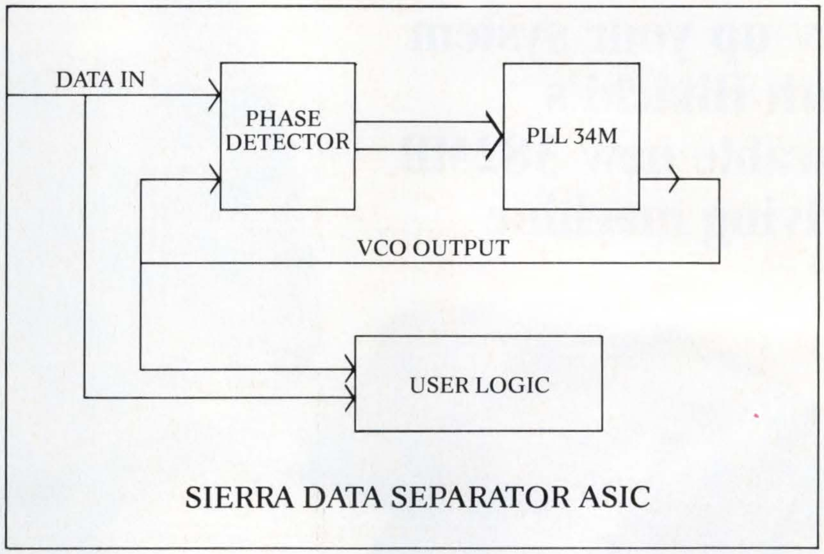
System level designers can access new levels of integration designing products with a combination of advanced analog/digital circuitry on a single ASIC. Obtaining the smallest form factor, lowest power, and highest performance in data capture applications is now possible.

Consider our 34MHz Phase lock loop subsystem – the PLL34M – an ideal solution for data separators.

The PLL34M is an open loop phase lock subsystem containing a voltage controlled oscillator, digitally controlled charge pump, trimmable reference voltage, and high speed driver I/O circuitry.

Combined with our other analog and digital standard cells, the PLL34M is ideal for increasing system integration of disk drive systems. (See application diagram.)

SIERRA integrates PLL onto a single data separator ASIC.



For designers seeking to incorporate analog processing functions, such as amplification, filtering, and data conversion, Sierra offers a wide range of solutions for applications in disk and tape drive systems, local area networks, and servo controllers.

Lock into our CMOS standard cell library which includes over 250 digital standard cells, 50 analog standard cells, and 20 EEPROM standard cells. Our Triple Technology™ gives you the flexibility to combine analog, digital, and E^2 on the same chip.

Sierra reduces packaging size and cost by offering low profile, surface mount packages including SOIC, PLCC, and PQFP Gull wing packages.

CMOS analog standard cells are available now in the same design environment as digital. Importantly, on-site mixed analog/digital simulation is easily achieved through access to our MIXsim™ software tools, which verify design functionality and assure first time silicon success.

Access the unbeatable combination of analog/digital ASIC from Sierra. Lock into the latest data on our CMOS standard cell library and provide your customers with the most advanced products. Just write or call today for our complete library card.

Sierra Semiconductor
Triple Technology.™ In CMOS.

2075 North Capitol Avenue, San Jose, California 95132. Telephone (408) 263-9300

CIRCLE NO. 14

For Long Life. In the Fast Lane.

Rev-up your system with Hitachi's durable new 382MB driving machine

Hitachi DK514-38 382MB 5.25" Winchester
16ms seek
1.8MB/sec. transfer
ESDI, E-SMD, SCSI interface
30,000 MTBF

Who says fast can't last? Not Hitachi. Our new DK514-38 382MB 5.25-inch drive brings you lightning-fast performance with unbeatable reliability.

Sophisticated technology has cut average seek time to a scorching 16ms, and increased the data transfer rate to 1.8MB/sec. Normally, you'd expect such speed to cost endurance. Not with Hitachi. In-house design and production of all major components and the most stringent quality assurance program in the industry give the DK514-38 30,000-hour MTBF.

If your super-micro, mini or workstation demands a drive that can keep up with your processor, and do it over the long haul, our DK514-38 is one machine you can't afford to pass up.

To learn more about this powerful, dependable performer, contact your best partner for mass-storage solutions... Hitachi. We'll show you the right way to drive. Fast.

Fast Action:

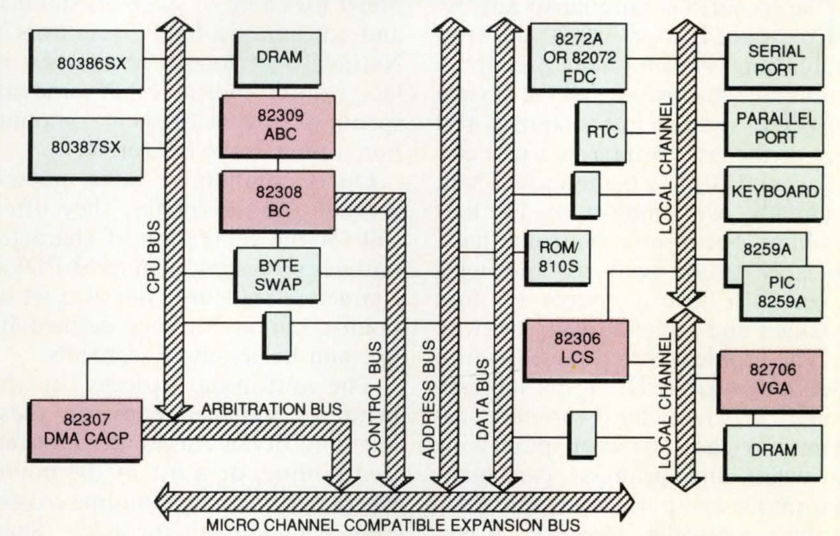
To get product literature immediately, CALL TOLL FREE 1-800-538-8157, Ext. 877. *In California,* 1-800-672-3470, Ext. 877. Ask for literature number PB-514.

Regional Sales Offices: Natick, MA 617/655-5501 • Dallas, TX 214/991-7983 • Brea, CA 714/993-1610 • San Bruno, CA 415/872-1902

Hitachi America, Ltd.
Computer Division
950 Elm Avenue, Suite 100
San Bruno, CA 94066

HITACHI®

New chips shrink Intel 32-bit systems



Intel's 80386SX offers a full 80386 implementation with 16-bit data and 24-bit address buses. The part is supported by the 82310 chip set, which provides a complete register-level emulation of the IBM Personal System/2, including the Micro Channel and the Video Graphics Array.

Two new processors, a full 80386 CPU with a 16-bit external bus from Intel (Santa Clara, CA) and a single-chip 1167 floating-point accelerator from Weitek (Sunnyvale, CA), will contribute to the rapid shrinking of computer boards based on Intel's 32-bit architecture. While the Weitek part is clearly a convenience for high-end system developers, the new Intel CPU may actually alter the ground rules that make up the heart of the personal computer market.

"The 80386 is established as the CPU for high-end personal computing and workstations," says Marc Rayacich, product-line manager at Intel. "Now we intend to proliferate the 80386 architecture through the entire range of the PC market."

The first vehicle for this proliferation is the long-awaited 80386SX, a full 80386 CPU with a 16-bit external data bus. "There are three performance segments in the PC market: 8088-based machines that run at about 0.3 Mips; 80286 machines that run at approximately 1.5 Mips; and 80386 systems in the 4- to 7-Mips range. The 80386SX, operating at 16 MHz, is aimed at the 80286 segment of the market. But the 80386SX will offer higher performance than the 12-MHz 80286, and it will have a full 80386 instruction-set architecture," says Rayacich.

Intel views the extension of the 80386 instruction architecture to mid-range systems as the key impact of the 80386SX. "It's more than just a faster clock," says product manager Bruce Schechter. "For many applications, the 32-bit architecture provides inherently greater performance." Borland (Scotts Valley, CA), for example, reports that its Paradox application runs five times faster on the 80386SX than on the 80286, according to Schechter.

In addition, applications, user interface environments and operating systems are becoming available specifically for the 80386 architecture. Many of these will never be ported to the more confining 80286 architecture, Schechter points out. Introduction of a mid-range version of the 80386, therefore, gives the largest segment of the personal computing market access to full 32-bit software.

Ron Wilson
Senior Editor

Hardware considerations

While the 80386SX is exactly compatible with the 80386 at the instruction-set level, it's incompatible with both the 80286 and the 80386 at the bus level. This will leave suppliers of system support chip sets temporarily aground. Taking advantage of the opportunity, Intel introduced its own highly integrated system of chip sets for the 80386SX. The H2230, H2231 and H2335 create an AT-bus system, while the 82310 chip set provides a complete register-level emulation of the IBM Personal System/2 environment.

Rounding out the product line, Intel announced the 80387SX, a math coprocessor that provides floating-point support on the 80386SX 16-bit bus. For customers in the embedded computing market who are using the previously announced 80376 CPU, the 80387SX will support that processor as well.

Shrinking the floating-point unit

At the same time that Intel extended its 32-bit architecture to another segment of the PC market, Weitek announced a significant improvement in the packaging of its 1167 floating-point unit: the reduction from a three-chip set to a single chip.

The 1167 is an incredibly fast FPU that interfaces to 80386 systems (not 80386SX systems). "On the double-precision Linpac benchmark, where 80386/80387 combination rates are 0.22 MFlops and the VAX 8600 with floating-point accelerator rates 0.61 MFlops, the 80386 with the Weitek chip comes in at 0.7 MFlops," says John Oxaal, coprocessor marketing manager at Weitek.

With a price of around $900 in production quantities, the new Weitek chip is clearly targeted at high-end workstations. Its remarkable performance and new single-chip packaging make the device another promising step forward for high-end desktop workstations. **CD**

Printer controller ICs take on PDL bottlenecks

The scenario is familiar to any experienced user of a desktop publishing system: You prepare a multipage document, tell the system to print, and the pages start to roll out of the laser printer at a nice clip of around 10 or 12 per minute. Then, suddenly, everything stops. For half an hour, the printer controller inexplicably grinds away, composing a page with just a couple of font changes and a line drawing or two.

The problem is that page-description languages (PDLs), the sophisticated, efficient, hardware-independent interfaces between publishing software and printers, can make enormous computing demands on a printer controller. However, a new generation of microprocessors and coprocessors is appearing, intended specifically to control printers that use PDLs. The new chips are designed to meet PDLs' insatiable demands for computing power, without pricing the finished printers right out of the desktop market.

The PDL pipeline

Design of the new parts hinges on an understanding of how PDLs are interpreted by a printer. Silicon architects have studied the task structure of the modern printer controller and have found a graphics pipeline with some logical, some floating-point-intensive and some data-moving stages. These chip designers have discovered that computing bottlenecks can appear at any point along this pipeline, depending not only on the system hardware and software, but also on the composition of the page being printed.

Commands in a PDL pass through a number of distinct processes in the printer controller, the first of which is an interpreter. "In a lot of ways, Postscript is similar to the Forth language," says Les Wilson, corporate manager for imaging technology at National Semiconductor (Santa Clara, CA). "The Postscript interpreter uses a lot of stack operations, and consumes a lot of resources." National's performance analysis on laser printers indicates that some can spend 30 percent of their computational time in the interpreter.

Once commands have passed through the interpreter, they often call for the generation of character outlines or graphics. In most PDLs, characters are stored not as a set of points, but as outlines defined by line and Bezier-curve segments.

The outlining process in the printer controller converts these lines and Bezier curves into a rasterized outline, or a list of the points where the character's outline crosses each scan line on the page. Since each Bezier curve—and there can be many in one character—is described by two third-order polynomials, the computations to generate the character outline are taxing. It's common for a 32-bit microcomputer to require tens of minutes to generate the outlines for a new font.

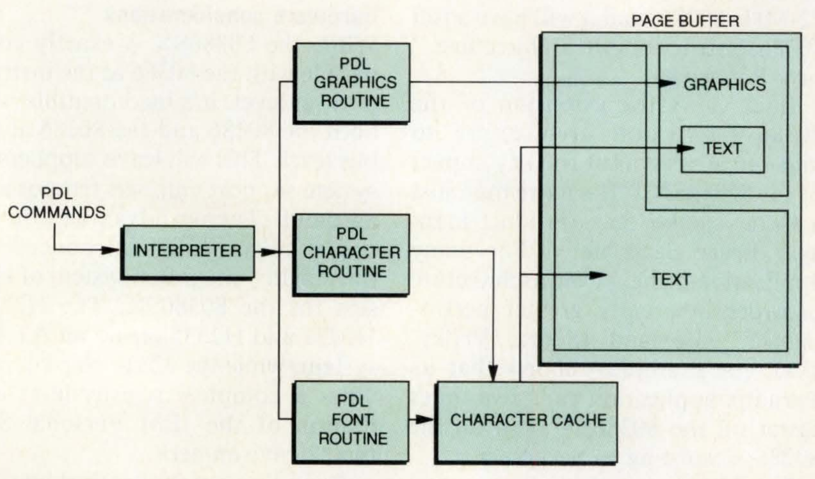
Drawing routines for graphics usually write directly into the printer's page buffer. Character outline routines, however, usually write their outlines into a character cache. That way, after a font is chosen, the characters are put in the cache and don't have to be regenerated each time they are used.

But having the character outlines in a cache creates the need for yet another process: a bit boundary block transfer (bitblt). When a PDL command requests a capital "A" at a particular location, the printer controller picks up the "A" outline from the character cache, fills it in with the appropriate pattern and transfers it into the page buffer.

Once all the PDL commands for a page have been interpreted, the graphics drawn, new outlines generated and cached, and characters transferred to the page buffer, the page buffer will finally contain all the pixel information necessary to drive the laser engine. At this point, printing begins.

Vendors seek solutions

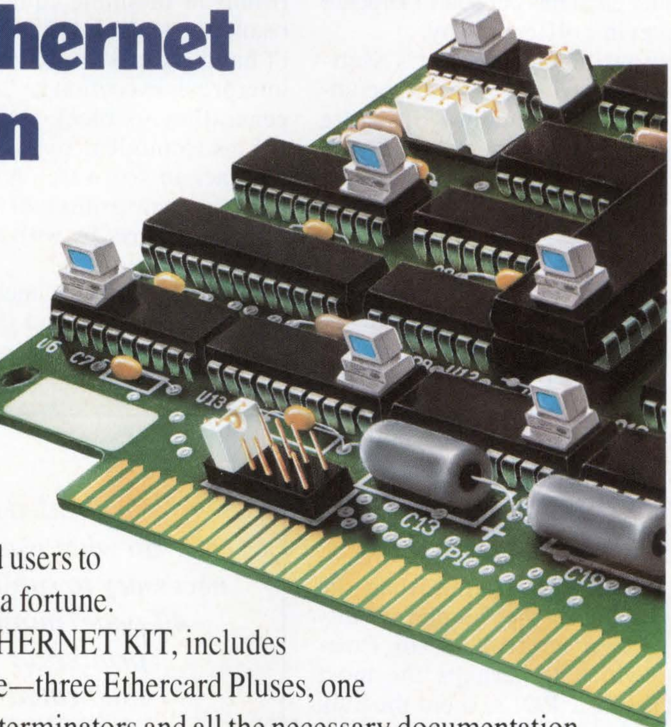
At least three silicon vendors—Weitek (Sunnyvale, CA), National Semiconductor and Cirrus Logic (Milpitas, CA)—have focused on designing hardware to implement this PDL interpretation process. Each has aimed at a different



Page-definition languages (PDLs) require a sophisticated pipeline. Stages in the pipe include a command interpreter, a floating-point stage that produces endpoints from Bezier functions, a character cache, and a page buffer in which the page is composed before printing.

Ron Wilson
Senior Editor

Hall-Mark makes networking easier with Ethernet Solutions from Western Digital



Hall-Mark and Western Digital have packaged LAN Solutions to make it easy for first time and experienced users to get networking benefits without spending a fortune.

Our Basic Starter Solution, the ETHERNET KIT, includes everything you need to bring 3 PCs on-line—three Ethercard Pluses, one Novell ELS Netware, two 20′ cables, two terminators and all the necessary documentation.

If you are wanting to expand existing networks, our ETHERCARD KIT may be just the answer. This package includes three Ethercard Pluses, three "T" connectors and documentation.

Or maybe you'd like to add a single user to your network or upgrade our Basic Starter Solution to 4 users. You need the ETHERCARD PLUS PACKAGE which includes an Ethercard Plus, one "T" connector and documentation.

The Novell ELS Software Package gives you the ability to use ELS Netware with other hardware providing the hardware is compatible. This package is especially helpful to first-time network users.

20′ cables and terminators are also available in cost saving packages from Hall-Mark.

So let Western Digital and Hall-Mark help you to expand your networking capabilities. Call us today for the kit that best fits your needs.

HALL-MARK Delivering Western Digital Technology

Hall-Mark Electronics Corp. • Dallas, Texas • Subsidiary of Tyler Corp.

Alabama
Huntsville (205) 837-8700
Arizona
Phoenix (602) 437-1200
California
Bay Area (408) 432-0900
Orange County (714) 669-4100
Sacramento (916) 722-8600
San Diego (619) 268-1201
San Fernando Valley (818) 716-3300
West Los Angeles (213) 217-8400

Colorado
Denver (303) 790-1662
Connecticut
Connecticut (203) 269-0100
Florida
Ft. Lauderdale (305) 971-9280
Orlando (305) 855-4020
Tampa Bay (813) 855-5773
Georgia
Atlanta (404) 447-8000
Illinois
Chicago (312) 860-3800

Indiana
Indianapolis (317) 872-8875
Kansas
Kansas City (913) 888-4747
Maryland
Baltimore (301) 988-9800
Massachusetts
Boston (617) 935-9777
Michigan
Detroit (313) 462-1205
Minnesota
Minneapolis (612) 941-2600

Missouri
St. Louis (314) 291-5350
New Jersey
Fairfield (201) 575-4415
New York
Long Island (516) 737-0600
Rochester (716) 244-9290
North Carolina
Raleigh (919) 872-0712
Ohio
Cleveland (216) 349-4632
Southern Ohio (614) 888-3313

Oklahoma
Tulsa (918) 251-1108
Pennsylvania
Philadelphia (215) 355-7300
Texas
Austin (512) 258-8848
Dallas (214) 553-4300
Houston (713) 781-6100
Utah
Salt Lake City (801) 972-1008
Wisonsin
Milwaukee (414) 797-7844

CIRCLE NO. 16

price/performance point, and consequently each has chosen to allocate resources in a different way.

National Semiconductor's strategy was to provide a base microcomputer capable of handling the entire procedure in software at a moderate speed. As speed demands increase, the system designer can add floating-point and bitblt coprocessors to improve performance.

National targets its printer controller chip, the 32CG16, at print engines capable of up to 20 pages/min. Such speed puts the product at the heart of the personal-computer-based office automation market, where system price is a key issue.

The company examined typical job loads for printers in this market and noted that highly complex pages were the exception rather than the rule. In fact, the company discovered that controllers for Postscript, which is perhaps the most popular of the PDLs, spent the bulk of their time running the interpreter itself. Floating-point computations and block-transfer operations weren't so frequent that they were a bottleneck. So National chose an architecture that focused on accelerating the interpreter and minimizing the amount of specialized hardware necessary to implement the printer controller.

The hardware of choice was readily available: an application-specific IC core version of the 32000-family CPU. "The regular complex-instruction-set architecture and rich addressing modes of the 32000 family are an excellent match for the needs of PDL interpreters," says P.S. Kohli, market development manager. But the 32000 instruction set was less prepared to cope with the drawing and block-transfer needs of the PDL pipeline.

"We added a collection of drawing, bit-manipulation and block-transfer instructions to the basic 32000 set," explains Les Wilson, corporate manager for imaging technology at National. Taking the notion of trading instructions for hardware a bit further, the designers added instructions for the CCITT-specified data-compression algorithms in facsimile equipment. The result was a 32-bit CPU chip capable of handling tasks ranging from PDL interpreter execution to Bezier-curve generation to block-transfer algorithms to modem signal-processing routines in software. A moderate-performance printer or FAX controller could get by with a minimum amount of hardware.

National's strategy included using coprocessors to extend the range of the base system. "Some systems, such as a printer using Hewlett-Packard's PDL, aren't at all critical about floating-point performance, so we chose not to build a floating-point unit onto the chip," explains Wilson. "But other applications that can have modest page/minute requirements can be quite demanding. For instance, a Kanji printer must cope with far more complex characters, and there are so many Kanji characters that caching them is impractical. So, using an FPU to accelerate outline generation becomes critical." To meet these needs, the company offers either the 32081 or the 32381 floating-point coprocessor. These chips serve to expand the 32-CG16 instruction set with a range of fast floating-point instructions.

The designers also saw a similar need for a swift block-transfer operation. As the page rate of the printer increases, the need for fast transfers from cache to page buffer quickly outstrips the 32CG16's new instructions. So National provides a block-transfer coprocessor, the DP8510, which effectively adds a set of bitblt instructions to the 32CG16. "The DP8510 will execute 2-operand bitblt operations essentially as fast as the bus will allow," claims Wilson.

National recognized that the introduction of a new architecture into the 68000-dominated printer market would require excellent language tools. Customers would be moving existing PDL software from other systems that weren't like the 32000 and had none of the 32CG16's specialized instructions. "We decided to build a set of compilers from the ground up for the chip," says Wilson. "We felt it would be a mistake to make the compilers nonstandard by trying to incorporate all the chip's specialized instructions, so we went for standard optimizing compilers. Then we supported the new instructions with library routines."

"We decided to do what was necessary to run 15- to 40-page/minute printers at their rated speeds on realistic pages."
—Dan Karr
Cirrus Logic

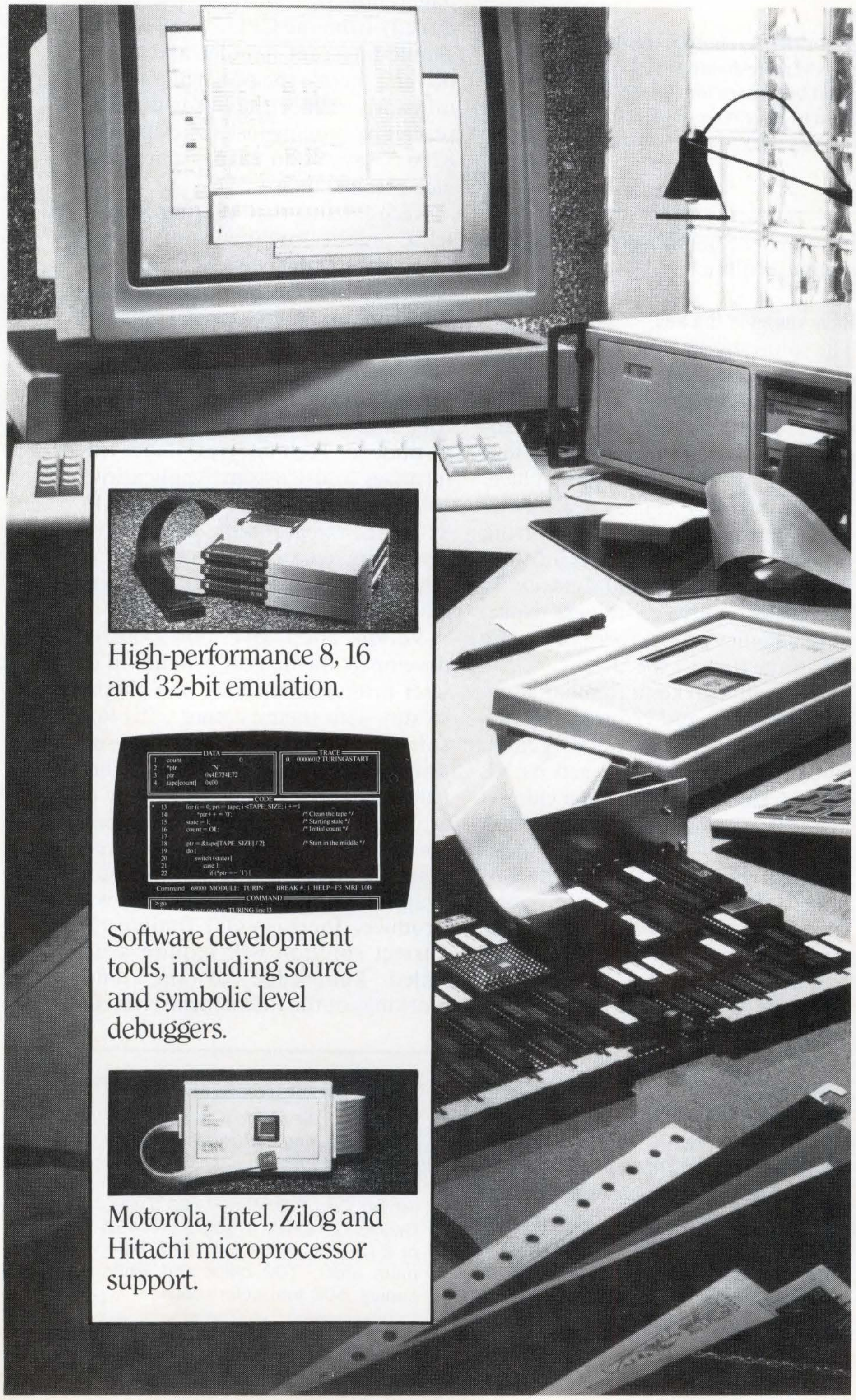
Focusing on transfers

Cirrus Logic set out with a higher page/min goal than National and developed a solution that was very different. "We decided to do what was necessary to run 15- to 40-page/min printers at their rated speeds on realistic pages," says Dan Karr, marketing manager for raster controller products.

The primary difference is that Cirrus' product, the GP 340 raster printer accelerator (RPX), isn't a microprocessor. "The best way to look at this part is as a graphics coprocessor for printers," says Mark Singer, manager of marketing communications at Cirrus.

The company had two strong reasons for taking the coprocessor approach. The first was that customers preserve their investment in existing code. "Customers find they can incorporate the RPX into their existing interpreter in literally two or three weeks," says Karr. "The RPX commands almost directly replace the subroutines that the interpreter already has.

The complex world of microprocessor development just got simpler.



High-performance 8, 16 and 32-bit emulation.

Software development tools, including source and symbolic level debuggers.

Motorola, Intel, Zilog and Hitachi microprocessor support.

As the challenges of developing and debugging embedded microprocessor designs becomes more and more complex, you need the best development tools possible.

And nobody offers you higher reliability, better performance or a quicker way to develop and debug your 8, 16 or 32-bit systems than Applied Microsystems.

Our emulators, for example, can be controlled from the host computer you work with (VAX, Sun, Apollo, IBM PC or compatible). Your target system will run exactly as if its microprocessor were in place. And you'll get a clear picture of your design and how it interfaces with interrupts, clocks and the flow of software.

Our emulators are designed to work with easy-to-use VALIDATE software to give you powerful source level or symbolic debugging capabilities. You also get our powerful Event Monitor System, a hierarchical, real-time breakpoint and triggering system.

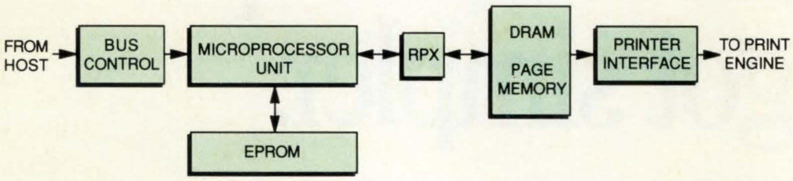
The list of benefits goes on and on; but the end result is a faster, easier and more accurate approach to developing, debugging and integrating your design.

To find out more, write Applied Microsystems Corporation, P.O. Box 97002, Redmond, Washington, USA 98073-9702. Or call (800) 426-3925, in WA call (206) 882-2000.

In Europe contact Applied Microsystems Corporation Ltd., Chiltern Court, High Street, Wendover, Aylesbury, Bucks, HP22 6EP, United Kingdom. Telephone 44-(0)-296-625462.
AMC-230

Applied Microsystems Corporation

CIRCLE NO. 17



Cirrus Logic's GP340 raster printer accelerator (RPX) chip acts both as a system support chip, performing dynamic RAM refresh and DMA control functions, and as a sophisticated intelligent bit boundary block transfer (bitblt) processor. The chip's close connection to page memory lets it accelerate the pattern fill and bitblt operations necessary to place characters in the page buffer.

"We studied a lot of Postscript implementations. We found that just about everybody goes through the process of calculating endpoints for character outlines, then bitblts a pattern into the line segment between the endpoints," he continues. At the speeds Cirrus sought, it was the bitblt operation that created the bottleneck. So the company devised a sophisticated bitblt processor that could fetch lists of endpoints from a CPU's memory and use them to load a pattern into the page buffer with a swift 3-operand bitblt.

With the bitblt engine, Cirrus integrated a number of the other functions that normally would require separate chips at these speeds. The RPX sits between the CPU and the page memory. The chip serves as a bitblt engine, an XY-to-memory address translator, a dynamic RAM refresh generator, a DMA controller and a video controller.

The result of offloading the translation from endpoints to filled characters is remarkable performance. According to Cirrus, the GP 340 can run at up to 40 pages/min at 300-dot/in. resolution with 5,000 10-point characters/page. The GP 315, a less ambitious part designed for 15- to 20-page/min operation, will be pin-compatible but will implement some GP 340 features in firmware instead of hardware.

Cirrus claims that its solution lets printer vendors use their existing microcomputer hardware and most of their existing PDL software to reach a range of performance well beyond the capabilities of the microcomputer alone.

Raw speed is the key

The solutions devised by both Cirrus and National didn't address the one remaining segment of the market. In this segment, complex fonts, uncachable fonts such as Kanji, and complex graphics are commonplace. Page rates may run as high as 60 pages/min. Resolutions can go from the laser printer's 300 dots/in. to a phototypesetter's 2,400 dots/in. In this realm, where customers expect to pay higher prices, there can be no substitute for raw speed.

All of this makes a familiar situation for FPU and reduced-instruction-set processor vendor Weitek. The company has packaged its XL RISC CPU architecture in a chip set aimed at the high-end laser-printer market. A two-chip set, the XL-8200 reaches 12-Mips integer performance. By adding a floating-point chip, the set becomes the XL-8232, with top performance of 12 Mips and 24 MFlops. Both chip sets are available in a range of speed grades, from inexpensive to very fast.

Rather than make specific hardware adaptations or instruction-set extensions for printer graphics, Weitek chose to focus on sheer speed. Thus far, the results seem to justify the means. The company claims that its highest speed-grade chip set can place 6,000 10-point characters/s, generate new fonts at the rate of 750 characters/s and compute Bezier endpoints at 750,000 points/s.

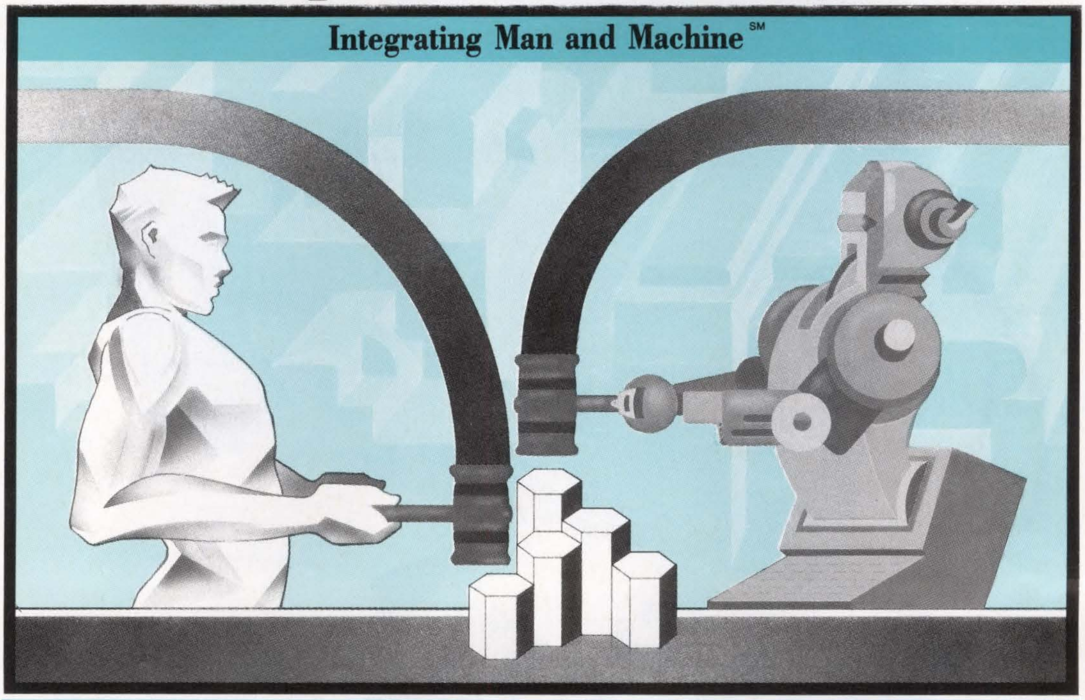
With that kind of speed, software can replace hardware in less demanding systems. "There is sufficient computing speed in the XL-8200 to handle tasks like network interfaces in addition to the printer control functions. Up to about 40 pages/min we can drive the video directly from the CPU. With a fairly simple interrupt handler and set of drivers, there's the possibility to significantly reduce the hardware in a printer by moving tasks into the XL-8200," says John Rizzo, marketing vice-president.

Recognizing that the XL-8200's RISC architecture is entirely foreign to most printer vendors, Weitek carefully covered its bases on software support. The chip set was introduced not only with the XL-8200 CPU's customary compiler support, but also with numerous PDL and font alternatives. PDL vendors such as Phoenix Technologies, Bauer Enterprises and Custom Applications will port their interpreters to the XL-8200. Bitstream will provide its Postscript-compatible fonts, and Nippon Information Sciences will develop Kanji typefaces.

Various alternatives now exist for developers of the next generation of laser printers. Designers can choose to stay with their existing CPU and software and accelerate specific sections of the PDL pipeline. Or they can move to a new CPU, either to reduce parts cost or to increase performance. In any case, the correct solution will depend on the font/graphics mix their customers will produce. Increasingly, finding the correct solution will require a detailed knowledge of the inner workings of the PDLs themselves. **CD**

FlexOS™

Systems Software Solutions for Top to Bottom Integration



TM

Real-time . . . multitasking . . . networking . . . graphics . . . protected file system
FlexOS—a full-feature software platform from Digital Research®

Real-time performance and raw computing power are only part of the mix needed to build integrated solutions. Managing data acquisition, alarm detection and annunciation, real-time trending, and on-line calculations requires a full-featured software platform that can quickly respond, dynamically process, securely store, and intelligently display data.

FlexOS is a modular operating system with a full set of real-time process and device management features – features that reduce your program development effort but don't get in your way when you need the performance.

Asynchronous I/O with two-tiered interrupt management for the development of systems with predictable real-time response

Fast multitasking kernel with pre-emptive, event-driven dispatcher and priority scheduler for versatile process management

ISO-model network interface with dynamic device mapping for application-transparent, peer-to-peer connectivity

Multitasking graphics interface for easy-to-learn and -use control panels and displays

Protected file access for secure distributed file systems

Hardware independence for application portability across CPUs ... across busses ... across devices ... across networks

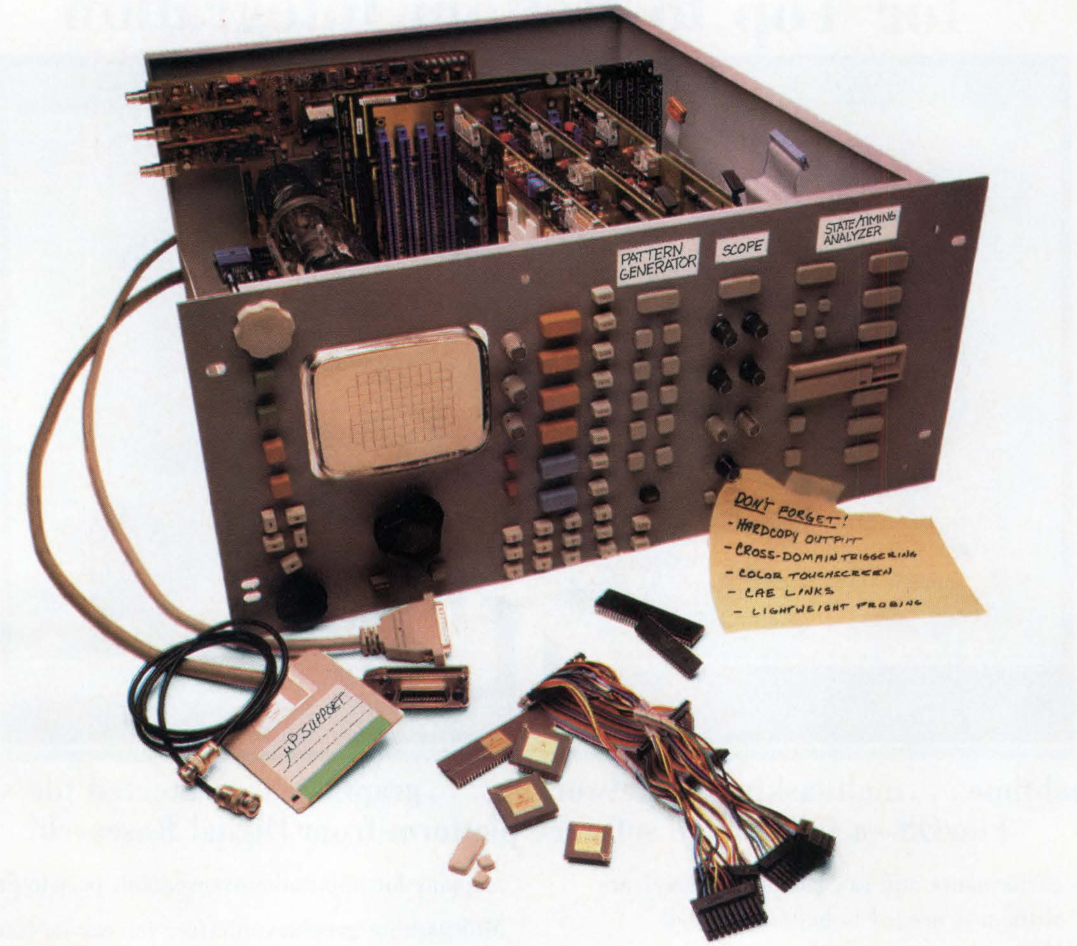
Modular architecture for building-block flexibility and easy configuration

Whether you're building a discrete data acquisition application or an integrated multiprocessor plant management system, the FlexOS product family gives you maximum flexibility with optimum performance. For more information on FlexOS™ 186, FlexOS™ 286, FlexOS™ 386, FlexNET™, and Multibus II™ Driver Pack call (800) 443-4200 or write

FlexOS Customer Service
Digital Research Inc.
Box DRI
Monterey, CA 93942

DIGITAL RESEARCH®

CIRCLE NO. 18



If you built your own logic analyzer... ...it would be

Why make just an analyzer when you could build a complete, flexible logic analysis system? A modular system with a 400 megasample/s digitizing oscilloscope, an interactive 50 Mbit/s pattern generator, up to 400 state/timing channels available, and a variety of features that make it versatile and easy to use. Plus a configurable price that you could easily justify to the boss.

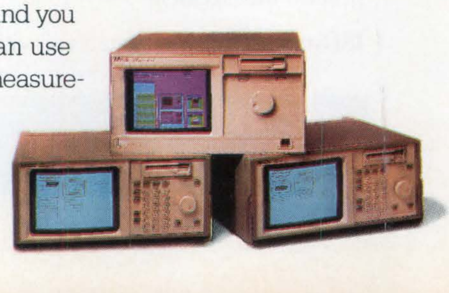
Fortunately, you don't have to build it yourself to get all this. Just choose the modular HP 16500A Logic Analysis System. HP has already done it for you.

HP Logic Analyzers: the extra measure.

Like all HP logic analysis tools, the HP 16500A delivers an extra measure of value. There are four different measurement modules to choose from. To maximize your investment, configure the HP 16500A, using its five mainframe slots, with the module combination that best matches your budget and application. Just imagine the possibilities for mixing and matching:

- 80-channel, 25MHz state/100MHz transitional timing module (400 channels maximum)
- 2-channel, 400 megasample/s digitizing scope module (8 channels maximum)
- 50 Mbit/s pattern generator module (204 channels maximum)
- 16-channel, 1 GHz timing analyzer module (80 channels maximum)

If your applications are in hardware, powerful inter-module cross-domain triggering allows high speed waveforms from both the scope and analyzer modules to be time correlated, giving you unmatched analysis capability. And you can use measure-



we never stop asking

What if...

more than a logic analyzer.

ment results for simulation by using HP's bi-directional CAE link.

If you're a software developer, the HP 16500A offers complete support for popular 8-, 16- and 32-bit microprocessors. You can also develop your own support package for use with your custom processors or ASICs.

But we didn't stop there. We designed a full set of features into the HP 16500A that make it easy to use. A touch screen or mouse controls functions through pop-up menus. Use your choice of a front panel knob or screen keyboard to change values. Plus, there are two built-in disc drives for data set-up and storage, HP Auto-Scale, and color hardcopy output at the push of a button. And the proverbial much more.

Call for your *free* video!
1-800-752-0900, Ext. H786.

See for yourself how the modular HP 16500A Logic Analysis System is the logic analysis tool you'd design yourself. Like every logic analyzer in the HP family, it delivers *the extra measure* of value you're looking for!

HEWLETT PACKARD

Vendors look outside to strengthen their simulation environments

No single simulator can handle all simulation requirements, from architectural and behavioral simulation at the system level to gate and circuit simulation at the IC level. Each phase of the design cycle requires a simulator tailored to its specific function. Since the internal development of a full range of simulators can be both technically and financially prohibitive, many vendors are looking to the outside for compatible products to enhance their simulation environments.

Evidence of this trend can be seen in various recent acquisitions, mergers and technology exchanges. HHB Systems (Mahwah, NJ) has been particularly active, having acquired Simucad (Menlo Park, CA). HHB also obtained the rights to the Dash-Cadat Plus simulator and Acculib modeling technology from Data I/O's Futurenet division (Redmond, WA), and the Saber/Cadat simulator from Analogy (Beaverton, OR).

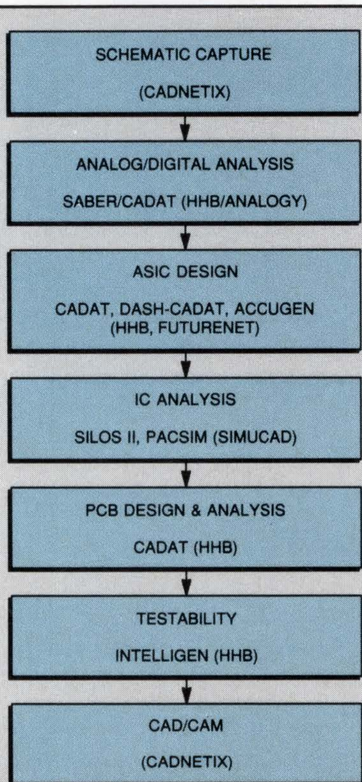
In its latest move, HHB and Cadnetix (Boulder, CO) entered into a merger under which HHB becomes a wholly owned subsidiary of Cadnetix. Although this merger doesn't directly affect HHB's simulation capability, it extends HHB's CAE strength to Cadnetix's printed circuit board CAD and CAM strengths.

Another company that's looking to strengthen its simulation capability is Silvar-Lisco (Menlo Park, CA), which signed a technology agreement with HHB, thus gaining access to HHB's Cadat simulator product line. Silvar-Lisco will use its Helix simulator for architectural-level analysis and will use Cadat for logic simulation.

HHB moves beyond board support

HHB Systems' various moves expand the company's capabilities beyond traditional printed circuit board support. The company's basic strength is its Cadat system, which consists of the Cadat integrated logic, fault and performance-analysis simulator, supported by the Cats simulation accelerator and the Cats hardware-modeling system.

Historically, the Cadat system has been strong in printed circuit board



HHB Systems has extended its product line well beyond the company's traditional printed circuit board design capability by combining its own technology development with acquisitions of, and technology agreements with, other companies. The merger with Cadnetix adds a new schematic capture capability and provides links to CAD/CAM tools.

design, but not in architectural, IC, application-specific IC or analog design. HHBs' recent moves were designed to enhance its product offerings in three areas: ASIC and IC design, ASIC and IC design analysis, and complex system analysis.

The company is expanding its ASIC design capability through a combination of internal developments and outside acquisitions. The acquisition of the Futurenet technologies and of Simucad strengthen HHB Systems' abilities in both IC and ASIC design and analysis, as well as in the analog area, says Hal Barbour, vice-president of marketing at HHB Systems.

Through its agreement with Futurenet, HHB Systems strengthened its ASIC support by acquiring the rights to both the Dash-Cadat simulator and the Acculib set of ASIC library development and maintenance tools. Dash-Cadat is based on HHB Systems' Cadat, with Futurenet enhancements in the areas of waveform display and human interface. Acculib provides a set of standard functions that can be mapped into ASIC cells, reducing the need to define detailed cell functions and cutting ASIC library development time by more than half. HHB integrated Acculib into its product line under the name Accugen, which was introduced last month.

The HHB Systems/Futurenet agreement is unusual in that HHB Systems acquired not only the Futurenet Dash-Cadat and Acculib simulation technologies, but also the nucleus of the design team that was developing them. HHB Systems also assumed responsibility for supporting Futurenet's installed base of Dash-Cadat and Acculib customers.

The Simucad acquisition enhances HHB Systems' ASIC design analysis capabilities. It brings to the company two new simulators, Silos II and Pacsim, along with an installed base of over 1,000. Silos II is a logic and fault simulator that's streamlined for precise switch-level IC design simulation. It's further enhanced with a system behavioral language for behavioral modeling and analysis. Pacsim is a circuit simulator that's compatible with the Spice simulator.

HHB's system-level design analysis is enhanced by the development of Saber/Cadat in conjunction with Analogy. Saber/Cadat provides simultaneous behavioral simulation in

Bill Harding
Contributing Editor

analog and digital domains through the use of tightly coupled analog and digital simulators, both with behavioral modeling capabilities.

Uniting Helix and Cadat

The agreement between HHB Systems and Silvar-Lisco is primarily an OEM arrangement under which Silvar-Lisco gains access to the Cadat simulator and its support tools. Cadat is optimized for gate- and switch-level simulations, while Silvar-Lisco's Helix is optimized for architectural and behavioral simulations. Silvar-Lisco's objective, therefore, is to create a simulation environment in which Helix handles high-level simulations and Cadat handles gate-level, switch-level and fault simulations.

Integrating Helix and Cadat will be a gradual process. Phase one, expected to be completed by September, will provide a common input system under Silvar-Lisco's schematic entry and data base system (SDS), and will adapt Silvar-Lisco's Logan logic-analyzer tool to display Cadat output and Helix output.

Once these two steps are completed, users will be able to create their blocks and schematics with SDS, do architectural simulation with Helix and look at results with Logan, says Herman Beke, vice-president of marketing at Silvar-Lisco. They can then push down into the schematic and do gate-level simulation with Cadat, look at results with Logan, and compare the architectural-level simulation results with the gate-level simulation results to determine whether the detailed design meets the specifications.

Phase two, scheduled for completion by the end of the year, will add the ability to perform multilevel simulations involving both behavioral- and gate-level designs. Initially, multilevel simulations will run on Helix. The key to accomplishing this phase is making Cadat models available to Helix, including those in the HHB Systems' Cats modeler.

Phase three and beyond in the Helix/Cadat integration process will involve providing a single modeling language for both the Helix and Cadat simulators and optimizing multilevel simulations by making Cadat work as a slave under Helix.

Mergers and technology exchanges offer a way around constraints imposed by limited technological or financial resources or by limited market windows. Such arrangements, however, don't offer immediate solutions. To be effective, companies must solve such problems as incompatible data bases, overlapping functionality, different human interfaces and varying platforms. **CD**

VHDL toolsets support design verification

With a mandate from the Department of Defense looming for the VHSIC Hardware Description Language (VHDL), many designers are seeking ways to implement this design language. Coming to the rescue are several new toolsets with simulation environments that conform to the recent IEEE standard, VHDL 1076.

VHDL is an executable hardware description language that supports a mix of behavioral and structural design descriptions. With enough backing from government and industry, this Ada-based language will become an industry-standard mechanism for generating portable simulation models. The first big boost for VHDL will come after the fourth quarter of 1988, when the DOD will require that all electronic designs intended for use in military systems be specified and verifiable in VHDL.

The first commercial VHDL 1076 simulator was introduced by Vantage Analysis Systems (Fremont, CA) in May (see "VHDL simulator provides interactive verification," *Computer Design*, May 15, p 24). Since then, Zycad (St. Paul, MN) and Intermetrics (Cambridge, MA) have introduced VHDL simulators. And CAD Language Systems (Potomac, MD) is working with electronic design automation (EDA) users and vendors to build VHDL interfaces to existing simulators.

Richard Goering
Senior Editor

Designers must decide whether to use a VHDL interface to an existing logic simulator or to start over with a new simulator that fully implements VHDL 1076. VHDL is so rich in features that existing simulators can't implement the entire language. "Most logic simulators have a fairly restricted set of functionality," says David Coelho, executive vice-president of Vantage. "When you build an interface to an existing simulator, you can use only those features of VHDL that map easily."

But VHDL 1076 simulators don't provide capabilities such as worst-case timing verification or critical-path analysis. VHDL also doesn't provide any standardized way to support fault simulation, a key concern for military-aerospace contractors. Moreover, VHDL models are just now becoming available.

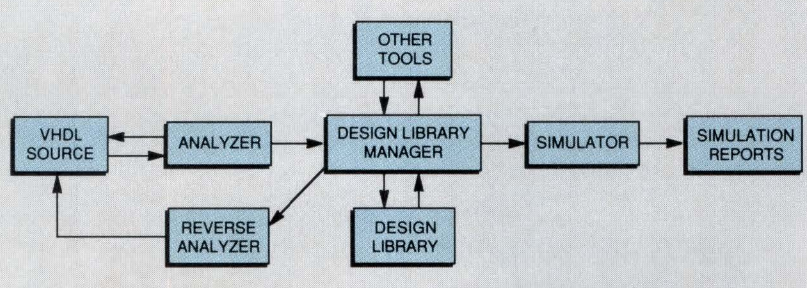
An intermediate format

Most VHDL toolsets start with an analyzer that compiles VHDL code into something a simulator can read. Intermetrics, for example, provides an analyzer that compiles VHDL models into its Intermediate VHDL Attributed Notation (Ivan) format. Meanwhile, CAD Language Systems has developed its own graph-structured intermediate format and is working with the IEEE's VHDL Analysis and Standardization Group to define an industry-standard VHDL intermediate format.

To manage the data stored in intermediate formats, both Intermetrics and CAD Language Systems provide design library systems. These libraries keep track of VHDL program modules for various components. Library-management systems provide revision control, and procedural interfaces supply access to library data.

If an intermediate format is well documented, users can build interfaces between the format and their own EDA tools. Translating models in and out of an intermediate format can be time-consuming, however. "We compile directly into executable code, which gives us a faster turnaround time," says Fred Hinchliffe, director of Endot product marketing at Zycad.

Intermetrics provides both batch and interactive VHDL 1076 simulators in the VAX/VMS environment, and will support its VHDL tools on Sun Microsystems workstations under Unix. The Endot-VHDL from Zycad is now available on Sun, Apollo and VAX workstations. And Vantage Analysis Systems' Vantage Spreadsheet runs on Mentor Graphics workstations.



Most VHDL toolsets include an analyzer that compiles VHDL code into something a simulator can read. In Intermetrics' toolset, the analyzer compiles VHDL into an intermediate format, and a reverse analyzer generates VHDL source code from this format. A design library manager keeps track of the intermediate format descriptions stored in the design library. Users of any VHDL toolset can build interfaces between an intermediate format—if well-documented—and their own design tools.

Freedom or chaos?

Because the Intermetrics, Zycad and Vantage simulators fully implement VHDL 1076, they can exploit all the features of the language. These simulators can, for example, freely mix behavioral and structural design descriptions and can operate on a number of different levels of abstraction. VHDL models can range from the architectural level to the gate level, a capability provided by only a few simulators today.

Zycad's Endot-VHDL simulator provides many of the same features as the system-level N.2 simulator, built by Endot before that company was acquired by Zycad. Users of either simulator can build an abstract architectural model before a system is partitioned into components, and they can also use an instruction-set architecture model to simulate microcode. But VHDL doesn't support stochastic performance modeling, a probabilistic technique used at the architectural level by N.2 to predict throughput in computer subsystems.

VHDL gives users a great deal of flexibility in defining data types. Most commercial simulators, in contrast, provide a single data type for multivalued logic, which defines a selection of states (such as 0, 1 or unknown) and strengths (such as active or passive). With VHDL, model builders can define their own states and strengths and can use other data types such as integers, records, arrays and pointers. At a very high level of abstraction, for example, it might be simpler to simulate an integer input into an ALU than to deal with an assortment of states and strengths on individual pins.

This freedom to define data types may be alluring, but it may also defeat one of the main purposes of VHDL, which is to provide portable simulation models. "If you want to move a VHDL model from one company to another, you need to have an agreement beforehand on which data types will be used," explains Erich Marschner, technical director of CAD Language Systems. "This is true even when two VHDL 1076 simulators are involved." To avoid potential chaos, VHDL standardization groups are now trying to agree on definitions for multivalued logic.

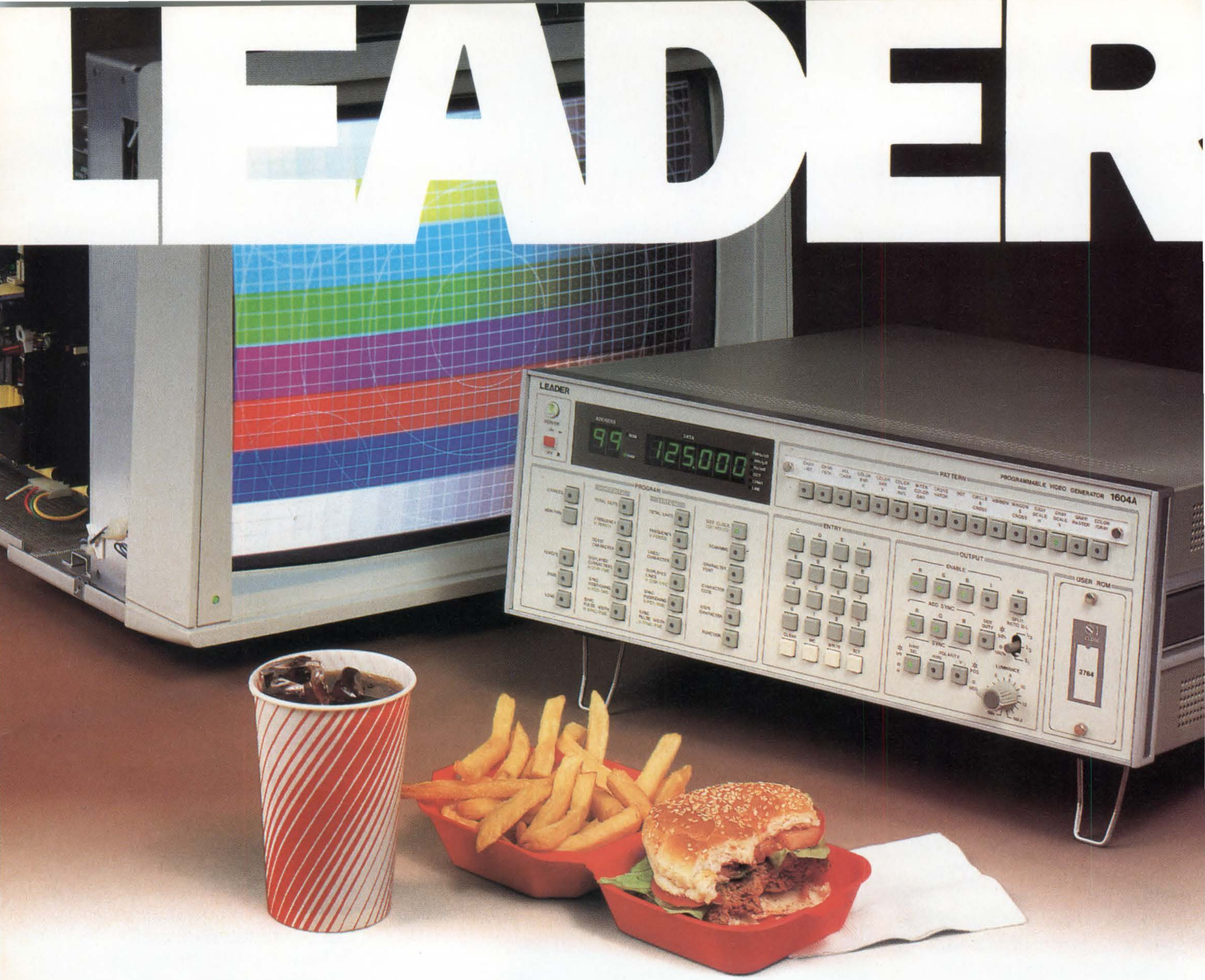
An accelerated solution

Since VHDL is a very complex language, the speed at which VHDL simulators execute has become a major concern. Zycad intends to address that concern by running some portions of Endot-VHDL on its own family of simulation accelerators.

Zycad is now working on interfaces that can compile VHDL into the primitives that run on the company's accelerators. According to Steve Marriner, marketing vice-president at Zycad, "There's a subset of VHDL that's fairly structured, and we'll be able to reduce that subset to Zycad primitives." Portions of the language that can't be accelerated will instead run on the accelerator's host computer.

Another big concern for VHDL simulation users is the availability of models. With agreements by Logic Automation (Beaverton, OR) and Quadtree (Bridgewater, NJ) to supply models for the Vantage Spreadsheet, it now appears that VHDL component models will be available in the near future. **CD**


We believed so strongly in
Plessey Microsystems' commercial
and military computer products,
we bought the company.



"At lunch today, I learned to use this programmable video generator. And still had time to eat."

While other RGB video generators take weeks to learn, ours take minutes. No digital training needed. No countless key combinations to learn. No need to use your PC unless you want to. Unlike other generators, Leader's have an integral programmer (LVG-1604A and 1603A) or are available with a programmer unit (1601A). And you can get any of dozens of test patterns simply by touching one clearly marked key.

All the functions you need.

The LVG-1604A lets you test even the most advanced high-resolution CRT's and wide-band video transmission systems. Present or future.

Analog, TTL and ECL outputs. 125 MHz. 64-color capability. Storage of up to 200 display formats. Wide range of raster architectures, and most common test patterns with both stock and user-designed characters. Ability to change format conditions. These features are easy to learn—but hard to beat.

Select a Leader Video Generator with all the features you need.

CIRCLE NO. 23 FOR PRODUCT DEMONSTRATION

Now you can choose.

You shouldn't pay for more functions than you need. So call us for a free copy of our full-line catalog. Pick the video generator that's right for you. Then, in just 30 minutes, we'll show you how to use it. It'll be up and running before you finish your lunch.

Call toll-free
1 800 645-5104
In NY State
516 231-6900

Leader Instruments Corporation
380 Oser Avenue, Hauppauge, New York 11788
Regional Offices:
Chicago, Dallas, Los Angeles, Boston, Atlanta
In Canada call Omnitronix Ltd. 416 828-6221

LEADER

FOR PROFESSIONALS WHO KNOW THE DIFFERENCE

CIRCLE NO. 24 FOR PRODUCT INFORMATION

Variety of enhancements revitalize 16-bit buses

Although several 32-bit buses are enjoying extraordinary market acceptance, 16-bit buses have so far refused to give up the ghost. In fact, because of the maturity, familiarity, product breadth and cost effectiveness of the 16-bit world, many system designers would rather stretch their 16-bit technology than make the leap to 32 bits.

Many designers see no sense in paying the price of moving to a 32-bit Micro Channel, Multibus II or VAX BI bus, for example, when a 16-bit AT bus, Multibus I or Q-bus will do. At the same time, the 16-bit buses offer a mature technology base for 8-bit applications in search of a performance lift.

That's not to say that the 16-bit world has nothing to offer in the way of technical innovation and evolution. Quite the contrary. Surface-mount technology, advanced microprocessors, dense memory chips and the like work the same wonders on 8- and 16-bit bus boards as they do on 32-bit boards. And, in fact, the ongoing evolution toward more on-board memory, functions and intelligence can often alleviate the need for moving to a wider system bus by reducing bus traffic. Nevertheless, there's been a substantial number of bus enhancements and bus-width expansion schemes designed to bring new life and design activity to the popular 8- and 16-bit buses.

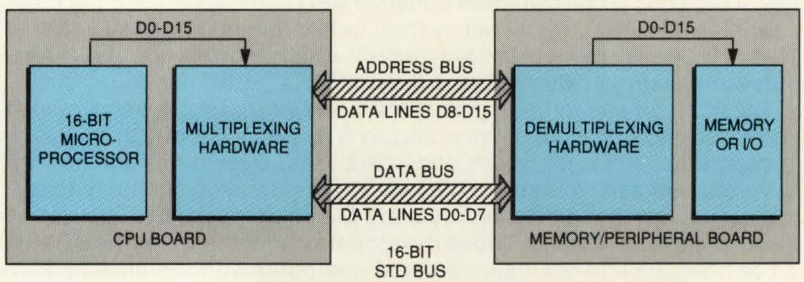
Recent times have seen, for example, a 16-bit extension to the 8-bit STD Bus and the development by Gespac (Mesa, AZ) of the 16-bit G96 Bus—which enhances the 16-bit G64 Bus by adding an extra row of connectors, increasing the address range and interrupt levels, and implementing a multiprocessing arbitration scheme. (Thirty-two-bit extensions are also in the works for both buses.) Micro Industries (Westerville, OH) has just begun domestic marketing of a Eurocard version of Multibus I dubbed AMS (Advanced Multibus System), a 1984 IEC standard bus created by Siemens AG (Munich, West Germany). And two 32-bit extensions for Multibus I—Tru-32 from Zendex (Dublin, CA) and Multibus Plus from Synergy Microsystems (Encinitas, CA)—have appeared, as has a 32-bit S-100 extension called Sky Bus from Compupro/Viasyn (Hayward, CA).

David Lieberman
Senior Editor

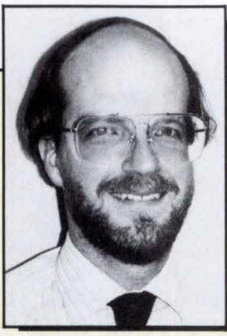
"Pushing a bus spec can be like trying to teach a pig how to sing: it wastes a great deal of time, and it's generally annoying to the pig."
—Ray Alderman
Matrix

There's considerable debate over how far a bus spec can be extended before it either runs out of steam or strays too far from the original form to be useful. "Pushing a bus spec can sometimes be like trying to teach a pig how to sing: it wastes a great deal of time, and it's generally annoying to the pig," says Ray Alderman, vice-president at Matrix (Raleigh, NC). Technically successful or not, all the extension schemes have essentially the same two-pronged goal: to let designers avoid the time, trouble and expense of having to learn a completely new bus structure, and to maintain interoperability with the installed base of standard bus products.

All this extension activity, according to Alderman, is a result of two factors: market saturation and product-line extension. "There are certain driving motivations for board vendors within all the bus structures," he explains. "Once you've satisfied the 8-bit market, for example—say, by implementing the latest microprocessor and the densest RAM—you can stop and become stagnant or you can go on to another



The 16-bit extension to the 8-bit STD Bus multiplexes 1 byte of a data word over the address bus at the end of each memory cycle, maintaining standardized system timing and backplane structure.



Alan Beverly
Engineering Manager
Ziatech

STD Bus stretches to 16 bits

The STD Bus was originally designed to support the operation of 8-bit processors such as the 8085 and the Z80, which continue to perform adequately in thousands of simple monitoring and control applications. But many applications have outgrown their 8-bit processor's power and memory limits. The need to provide an evolutionary growth path for these applications, as well as higher performance capabilities for new applications, prompted the STD Bus Manufacturers' Group to implement the Intel 8088 on the STD Bus in 1983 and, more recently, to develop a 16-bit data-transfer capability for the bus. The primary goal of the STD-8088 committee, for both the original STD-8088 specification and the new 16-bit extension, has been to give designers a higher performance STD Bus that retains compatibility with existing STD Bus products.

The STD Bus receives a significant performance boost from the 8088 processor because it combines a 16-bit internal data path with an 8-bit external data bus. The STD-8088 specification improves system performance but maintains the 8-bit STD Bus.

STD Bus applications continue to demand more processing power, and two approaches have been developed to meet these needs. The first, an extension to the STD-8088 specification, allows 16-bit data transfers over the STD Bus. This extension involves multiplexing a second byte of data over the address bus at the end of each memory cycle. All devices that require frequent access to external memory, such as video controllers, will benefit greatly from this extension of the STD-8088 specification.

This extension, originally proposed by Winsystems (Arlington, TX), provides for the faster transfer of data to or from memory and I/O boards without requiring any physical changes to the STD Bus backplane. It does require, however, that memory boards are designed to latch the address prior to the data's being multiplexed on the address bus. Processor and memory boards that support this technique are just now becoming available.

The second approach to achieving 16-bit capability on the STD Bus also maintains compatibility with the original STD-8088 specification. This approach puts 16-bit processors on STD Bus single-board computers, but it limits 16-bit data transfers between the CPU and memory to the single-board computer itself and maintains the current 8-bit external data bus. Data transfers between CPU and memory are the most crucial in determining overall system performance. The availability of 16-bit CPU-to-memory data transfers on a single-board computer thus puts processing power where it most affects performance.

These 16-bit capabilities give system integrators more performance and more choices when developing an STD Bus system, but they also necessitate some important considerations. Developers looking for the improved performance of the new 16-bit extension should research the availability of 16-bit memory and I/O boards needed to realize the performance advantage. Those developers choosing to restrict the 16-bit performance to their single-board computer with the current STD-8088 specification should be certain that the computer has adequate on-board memory to handle their application. Otherwise, if they decide to add extra memory at a later date, they should be prepared to settle for 8-bit speeds.

bus structure. The barriers to changing buses, though, are pretty severe, and the least risky of all the approaches is to adapt newer technology to an established platform."

Multibus I on the move

Multibus I, itself a former migrant from 8 to 16 bits, seems to be undergoing a resurgence. Sales are reportedly healthy, export business is reportedly brisk and a modest, though increasing, number of new board designs are appearing.

"A lot of people are realizing that they can still do what they need to do for the majority of applications with Multibus I," says Mike Pritchard, Multibus product marketing manager at Intel's OEM Modules Operation (Hillsboro, OR). As Bob Hanson, Hillsboro general manager, sees it, "Multibus I will probably live forever because of the many dedicated users who are absolutely fanatic about it. It's hard to rationalize a 32-bit bus if you're not going to use its advanced features, and if people can stick with a PC in the office environment or Multibus I in the industrial arena, they will."

Craig Fredericks, vice-president of sales and marketing at SBE (Concord, CA), agrees. "The industrial arena won't swap out its installed Multibus I base overnight," he says. "Since CPU boards have 68020s and lots of memory on-board, bus bandwidth isn't that critical, so there's no need to move to something else."

Several Multibus I board vendors are targeting their new designs directly at real-time industrial-control applications, where bus width and even compute power may be less important than low power, noise immunity, extended operating temperature range and extensive I/O. But Alan Beverly, engineering manager at STD vendor Ziatech (San Luis Obispo, CA), points out that new entries into the industrial-control arena will find it no mean feat to meet all of the three major requirements: reliable real-time acquisition of real-world data, low power operation and extended temperature range (−40 to +85 °C).

With Inmos, the B-1B's radar system got off the ground.

TECHNOLOGY · FOR · DEFENSE

In fact, INMOS military devices are utilized by every major subcontractor in numerous defense and space programs. Last year fifty percent of our U.S. memory business was with the military, and the number of INMOS Transputer and DSP design wins is steadily increasing.

You don't remain a successful supplier of military devices without doing a lot of things right.

Our success stems from an ongoing commitment to Quality and Reliability Assurance – the most important operating priority at INMOS.

Our approach is one of designing and manufacturing quality and reliability into every INMOS part instead of relying upon screening to inspect for quality.

Send the coupon in today to learn what this approach means to you, what MIL-STD-883C compliance means to INMOS, and why we are the supplier often selected for important defense programs. You'll receive your free copy of our military brochure "Technology for Defense".

inmos®

INMOS, Colorado Springs, Colorado 80935.
Tel. (719) 630-4000

Orange County – 714-957-6018
Denver – 303-368-0561
Dallas – 214-490-9522
Baltimore – 301-995-6952
Santa Clara – 408-727-7771
Minneapolis – 612-932-7121
Boston – 617-229-2550
Atlanta – 404-242-7444
New York – 914-897-2422

Please send me a copy of the INMOS military brochure "Technology for Defense".

Name ____________________

Title ____________________

Company ____________________

Address ____________________

____

Zip ____________ Tel ____________

CD 7/88

CIRCLE NO. 25

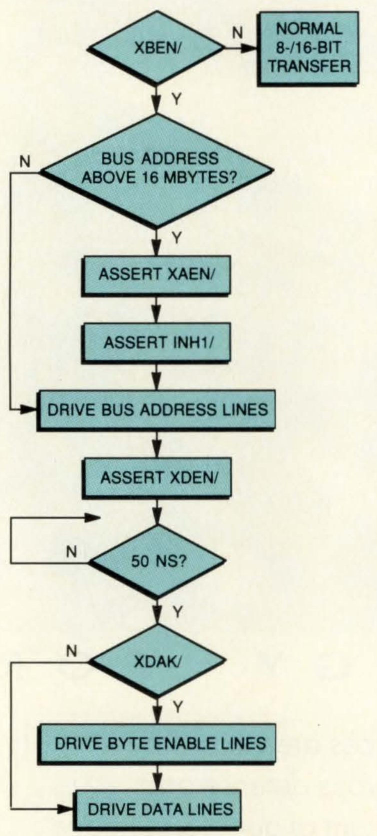
Certain features can be drawbacks

Even the most ardent Multibus I defenders will admit that certain Multibus I features represent drawbacks for certain applications. These features include the bus's 16-bit-wide data path and 10-Mbyte/s maximum transfer rate, the 24-bit memory addressing and 16-Mbyte address range limitations, the lack of a block-transfer function, and the use of edge-card connectors and a non-Eurocard form factor. Several companies have come up with bus-enhancement schemes to revamp various of these features.

Siemens' AMS bus, for example, is basically a 6U Eurocard version of Multibus I that brings the benefits of DIN connectors, tightly toleranced signal routing, single-connector (P1 only) implementation, and 21-board (vs. 16) maximum configuration to the industrial automation arena. While standard Multibus I requires four of the signal lines on P2 to perform extended 24-bit addressing, the entire AMS interface is implemented on P1, leaving P2 completely free for system designers to implement their own I/O bus or an interface to Siemens' 8-bit SMP (Subsystem Microprocessor Product) Bus. The AMS represents more than just a bus strategy. Rather, it's a total system strategy that integrates—via common RMOS real-time operating system drivers—the 8-bit SMP, the 16-bit AMS and the 32-bit Multibus II.

Last year's Tru-32 from Zendex, endorsed this spring by Microbar Systems (Sunnyvale, CA), and this year's Multibus Plus from Synergy Microsystems share two common goals: to provide the kind of fast single-board computer-to-memory transfers that have exceeded the ability of Multibus I's aging iLBX auxiliary bus, and to provide the bandwidth necessary for effective communications in multiprocessing systems. Both schemes use the undefined pins on the P2 connector—which are no longer available for iLBX or vendor-unique I/O—to expand the data bus from 16 to 32 bits and the address bus from 24 to 28 bits, thus increasing physical address space from 16 to 256 Mbytes.

"A lot of our customers are in a quandry as to whether Multibus I can meet their future needs or whether they have to bite the bullet and move to another bus like VMEbus or Multibus II," says Tom Powell, Synergy director of marketing. "Since most don't want to change buses, they're looking for an upgrade path that lets them retain their investment in existing products."



In the Zendex Tru-32 enhancement scheme for Multibus I, one board queries another to determine whether the second board is equipped for extended data transfers or addressing. If it isn't, operations occur within the parameters of the traditional Multibus I specification.

To maintain compatibility with existing Multibus I boards, both Tru-32 and Multibus Plus implement a protocol for determining which system boards are capable, and which are incapable, of extended transfers and addressing. For garden-variety 16-bit Multibus I boards, operations occur within the parameters of the Multibus I spec.

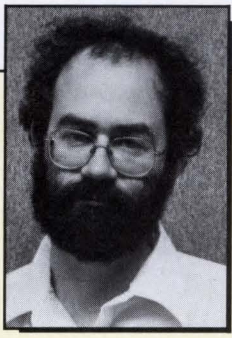
"The 32 bits alone doesn't get you VME-type performance, though," cautions Synergy's president, Stan Skowronski. So Synergy's Multibus Plus goes a step further, overlaying a burst-transfer mode on the Multibus I spec. In standard Multibus I, each time a current bus master performs a data transfer, it must give up and rearbitrate for the bus, introducing at least 100 ns of overhead for each piece of data transferred. The Multibus Plus burst-transfer technique, in contrast, lets a master perform four transfers without giving up the bus. This, plus the use of nibble-mode RAM chips, according to Skowronski, lets data transfers occur at up to 32 Mbytes/s.

According to Russ Gamble, Zendex vice-president/general manager, the added costs for a board maker to implement a Tru-32 scheme, in addition to nonrecurring expenses, are "about $4 for some very simple logic circuitry and a little bit of real estate." Multibus Plus, according to Synergy's Powell, can be implemented in five chips: four driver/receiver chips and a single PAL.

Using small boards

In addition to the 16-bit activity on larger bus boards—6.75- × 12-in. Multibus I and 6U (about 6.4- × 9.3-in.) VMEbus, for example—there's quite a bit of action among the small bus boards. These include the 4.5- × 6.5-in. STD Bus and the 3U (about 6.4- × 4-in.) G64/96 and VMEbus. "There are applications that simply can't afford the cost and real estate of a big bus," says Ziatech's Beverly, "such as blood analyzers, underwater radars, wafer steppers and so forth."

The smaller-form-factor boards generally provide less functionality than do larger boards, simply because there's less usable real estate to work with. According to Rick Main, analyst at Databus Marketing Reports (Sunnyvale, CA), for example, "The VME interface takes up a lot



Leonard A. Lehmann
President
VME Specialists

VMEbus carves a niche in the 16-bit market

The VMEbus board market is splitting into two distinct segments: the single-height (3U), 16-bit segment, and the double-height (6U), 32-bit segment. This segmentation means that market forecasts, comparative performance evaluations and cost analyses that address VMEbus products as a whole are no longer appropriate. The 3U and 6U products differ in size, performance and price and, hence, serve vastly different needs.

Besides the board size, the major difference between the two form factors is the 6U system's use of a second (P2) connector/backplane to extend memory addressing from 24 to 32 bits (and addressable memory from 16 Mbytes to 4 Gbytes), data-transfer bandwidth from 20 Mbytes/s to 40 Mbytes/s, and data-transfer width from 16 to 32 bits. Both form factors support the full interrupt and bus-arbitration capabilities, utility lines and so forth of the VMEbus.

The 3U VMEbus market is experiencing spectacular growth because new chip technology and surface-mount packaging and assembly techniques are providing powerful capabilities on the smaller, 3U boards. The 3U boards thus have a size, cost and power advantage over 6U products. Single-height boards are also being used in 6U-sized chassis when a mix of both board sizes is desired.

Many former STD Bus and Multibus I users are upgrading to 3U VMEbus, which offers the ruggedness of the Eurocard format and its DIN connectors but without the space and price premium of full 32-bit VMEbus. Users who need a relatively compact package with at least 90 percent of the performance of 6U VMEbus at about half the price are generating a rapidly growing 3U market within the VMEbus field.

Users give up little performance in going to the 3U format. The advantage of 6U VMEbus lies in its 32-bit transfers. But most peripheral boards on the VMEbus market can perform only 16-bit transfers, so this advantage is lost. When these boards are using the bus, the second backplane is dead wood but still draws power from the system.

Bus data-transfer rates have, in fact, become less important as higher levels of integration let more functionality be packed onto single-board computers and as local intelligence is incorporated into peripheral and I/O boards. System designers have discovered that 32-bit transfers often only marginally help the actual performance of real-world systems. Processors spend so little time on the backplane these days that a wider transfer width affects performance by a few percent at most. If the code is on the CPU board, the data is on the VMEbus and the software is set up for 32-bit data, a 68020 performing memory transfers over the bus, for example, executes just 15 percent faster on a full 32-bit VMEbus than it does on a 16-bit VMEbus.

In the past, the bus was used as an extension of the processor. Data and, often, code were stored on a separate memory board on the bus; I/O boards were simple, dumb and unbuffered; and a DMA controller, if the system had one, was a separate board. This is no longer the case. Now the bus is used primarily to pass messages between intelligent subsystems. Processors typically execute all their code, and access most of their data, locally. And when data does move across the bus, it's typically structured into blocks, often with unnecessary information removed, achieving greater data-transfer efficiency than would be achieved by doubling the data-transfer width.

of real estate—as much as 25 percent of a 6U board and almost 50 percent of a 3U board, so there's not much room left to do anything useful."

According to Matrix's Alderman, however, the limited functionality of a small board can be a virtue, since designers can economically and incrementally expand the system with just the functions they need. "If someone is doing a 6U VMEbus system," he says, "and he needs to add four I/O ports, for example, he'll have the choice between a big-ticket, eight-port 6U board or an inexpensive, four-port 3U board with a 6U front panel."

But smaller boards don't necessarily need to have limited functionality in comparison to their larger counterparts. The relatively large amount of available real estate on a 6U board, for example, is sometimes an excuse for sloppy layout. And the relatively limited room on a 3U board sometimes drives a company to implement the latest technology.

Up from 8 bits

Like the 32-bit Multibus extension schemes, the 16-bit STD Bus extension maintains compatibility with standard, 8-bit STD boards and involves relatively little cost. "The extension adds probably one square inch and about $10," says Jim Eckford, Ziatech vice-president of sales and marketing. "That's pretty negligible, but when you're trying to make the most of an STD card, one square inch can be worth a lot."

Those STD Bus board manufacturers that see a pressing need for an external 16-bit data path are in the minority, with most preferring to implement 16 bits within the confines of a board, if at all. Most do, however, believe that an external 16-bit data bus will extend the viability of the bus. "We wanted to make sure we had a growth path through evolution, not revolution," says Robert Burckle, vice-president at Winsystems (Arlington, TX). "The fundamental question that has to be asked before making the change is, given the economics of the application, do you really need it?" **CD**


2J3
2J4

Optimizing compilers address debugging and user control constraints

Armed with parser generation, syntax-directed translation and flow analysis, the knight on the cover of a 1986 textbook on compilers prepared to slay the dragon of optimized compiler design. Today, that fight has been successfully waged, and optimizing compilers using a variety of code-transformation techniques are widely available. But the question of how much control the compiler user should have over choice of optimizations remains unresolved, and the victory of optimization has conjured up the new, and perhaps fiercer, dragon of optimized code debugging.

Techniques for compiler optimization, designed to transform code to improve speed or size, or both, offer the user a way to improve software performance without resorting to tedious hand manipulation of assembly code. In many cases, optimizations provide an automatic and inexpensive route to code improvement—but in other cases, the results are just the opposite. Optimizing compilers can evoke code problems that weren't evident in nonoptimized code, or they may even break the code. Vendors are working to avoid those problems and to find the best techniques for optimization.

Howard Falk
Contributing Editor

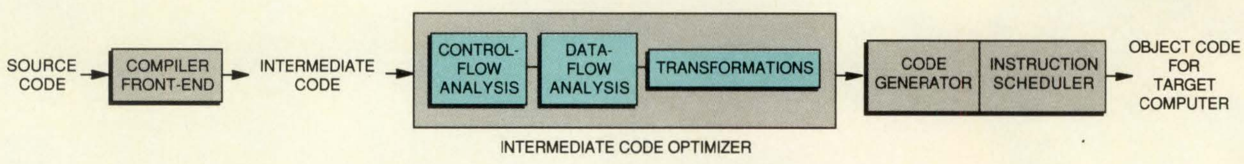
Because optimization techniques are relatively new to vendors of compilers for microprocessor systems, it isn't surprising that different vendors seem to have disparate ideas about which optimizations are appropriate and how best to implement them. From the grab bag of available techniques, each vendor has chosen optimizations to meet particular product goals, in some cases adding innovative touches to existing techniques.

One vendor that has been investing heavily in optimization is Intermetrics (Cambridge, MA), which is focusing its development effort on a global optimizer designed to be used with the company's entire line of Intertools C cross-compilers. To perform automatic register allocation, the Intermetrics optimizer transforms source code into a graph representation of data and control flow in the memory of the host computer. The compiler then walks the graph to locate possibilities for optimization. For example, if the compiler finds two loops with execution periods that don't overlap, variables from those two loops can safely share the same registers.

The compiler can also look for and mark common subexpressions that the source code computes repeatedly. These subexpressions may then be stored in registers so they can be reused rather than recomputed.

During and after code generation, Intermetrics compilers use information generated by flow analysis to make register assignments and decide on execution sequences for the computer on which the object code will run. For processors such as the Z80 that have few internal registers, the ability to implement register allocation optimizations is limited. At the other extreme, reduced-instruction-set computers—with their numerous registers—provide fertile ground for such optimizations.

To make use of available registers and to take advantage of the pipelining provided by some processors, code in an optimizing compiler can be reordered by a final instruction-scheduling procedure. Intermetrics has developed a scheduling algorithm as part of the compiler the company is building for the NEC V60 processor, which has many registers and is heavily pipelined. By changing the order of instruction sequences, the algorithm increases performance. The scheduling algorithm is designed to anticipate pipeline activity. "We believe we'll be able to enhance the speed of programs generated by a 68020 compiler by applying technology we've developed for



In the optimization process, the compiler's front-end converts source code provided by the user into intermediate code. Then optimization transformations involving loops, procedure calls and address calculations are typically performed, as are data- and control-flow analyses needed for global optimizations. The transformed intermediate code then passes through a code generator and an optimizing instruction scheduler, where peephole transformations and assignments to registers—as well as other optimizations designed for specific machines—may take place.

main () {	Optimized Code		Nonoptimized Code	
	pushm	#0x4c	prepare	#24
int a,b,c,d,e,f;				
a = (b + c) + e	mov.w	r5, r2	mov.w	-0x8[fp], r23
	add.w	r4, r2	add.w	-0xc[fp], r23
	add.w	r3, r2	add.w	-0x14[fp], r23
	mov.w	r2, r6	mov.w	r23, -0x4[fp]
d = (b + c) + e	mov.w	r2, r3	mov.w	-0x8[fp], r24
			add.w	-0xc[fp], r24
			add.w	-0x14[fp], r24
			mov.w	r24, -0x10[fp]
f = (b + c)	mov.w	r5, r2	mov.w	-0x8[fp], r25
	add.w	r4, r2	add.w	-0xc[fp], r25
			mov.w	r25, -0x18[fp]
	popm	#0x4c	dispose	
	ret	#0	ret	#0
	35 bytes		53 bytes	

Common subexpression elimination is performed by the Intertools global optimizer from Intermetrics. In this example, the optimizer decided that the subexpression (b + c) + e should be saved in a register for reuse. The optimizer also selects variables for placement in registers to eliminate unnecessary memory references and thus speed code execution.

the V60," says Ronald Kole, director of software product development. Intermetrics has C compilers for 68000/10/20, 68HC11, 8086, 80186/286 and Z80 processors. The company is also developing optimizing compilers for the NEC V70 and Advanced Micro Devices 29000 chips, according to Kole.

The MCC86 C compiler from Microtec Research (Santa Clara, CA) for 8086-, 80186- and 80286-based computers performs optimizations such as constant folding (performing arithmetic on constants during compilation rather than at run time), strength reduction (substitution of equivalent operations to reduce compute time), and elimination of unreachable or redundant code. The compiler also does peephole optimizations that examine and transform only small code segments. A special Microtec optimization generates efficient code for the switch statement by evaluating which of three possible coding methods will give the best results in each situation. Optimization of jump instructions is performed iteratively until no further improvements occur. Optimizations specific to 8086, 80186 and 80286 processors are also performed.

The Microtec MCC68K C compiler for 68000/10/20 and 68881 processors performs many of the same optimizations and takes advantage of the many registers made available by the 68000 architecture. The MCC68K does register allocation using a coloring algorithm (a technique that minimizes the cost of using memory to store variables and instructions that can't be fitted into available registers) and in-line multiplication (use of in-line code rather than a multiplication subroutine). The compiler also moves invariant computations out of loops. Microtec plans future optimizations such as passing parameters in registers rather than on the stack and bringing subroutines in-line for optimization with the rest of the code.

Focusing on register allocation

Borland International (Scotts Valley, CA), which has compilers for target systems based only on Intel-type chips, concentrates on optimizations involving register allocation. Because there are few registers on chips such as the 8088 and 80286, which are used in the personal computers on which Borland compilers run, those registers have to be carefully allocated to attain efficient execution. Borland's Turbo C compiler automatically assigns variables to registers and suppresses reloads from memory for values already in registers. Turbo C also does peephole optimization and eliminates redundant execution of some identical code sequences. "We're doing the machine-dependent optimizations that make sense," says David Intersimone, director of languages and tools at Borland. "Of course, we'll add machine-independent optimizations as well, because users don't always write perfect code." Although reluctant to discuss future plans, Intersimone indicated that Borland will develop a global optimizer that will operate on entire programs rather than on individual functions.

A similar optimization strategy is followed at Computer Innovations (Tinton Falls, NJ) with the C86Plus v.1.0 optimizing compiler for 80386-based computers. "A lot of compute cycles can be spent in flushing out 80386 registers and moving data from one to another," says George Eberhardt, president of the com-

	Optimized Code		Nonoptimized Code	
	move.l	d0,d3	move.l	d0,d1
	move.l	d3,d1	move.l	d4,d0
	move.l	d1,d0	jsr	ulmult
	mulu	d2,d3	move.w	d3,d0
	swap	d1	muls	d2,d0
	mulu	d2,d1		
i = j * k	swap	d2		
	mulu	d2,d0		
	add.l	d1,d0		
	swap	d0		
	clr.w	d0		
	add.l	d0,d3		
	move.w	d5,d0		
	muls	d4,d0		
	364 cycles		488 cycles	

The MCC68K optimizing compiler from Microtec Research expands 32-bit multiplications into in-line code, instead of using the library routine for multiplication (ulmult). The optimized code from the compiler contains more statements but runs faster than nonoptimized code.

pany. Optimizations can reduce the amount of code to be processed, but the time gained can be lost if too many register moves are involved. For that reason, the company decided that the most important optimizations to include were those that deal with register allocation.

Register allocation optimization, along with several other techniques, is used in the C-386 compiler from Green Hills Software (Glendale, CA). The C-386 is a C optimizing compiler for computers that use the 80386 chip. This compiler performs register allocation by coloring, peephole optimizations and loop optimizations that involve invariant analysis (identifying invariant expressions in loops and calculating them outside the loops). The compiler also determines each variable's use-lifetime, providing a basis for reusing registers by storing more than one variable in a register during a procedure. The result of this technique is that local variables are usually stored in registers rather than in memory.

Not every compiler vendor that works with Intel-based target machines has fastened upon register allocation as the key to optimization. High C compilers from Meta Ware (Santa Cruz, CA) use special optimizations that obtain up to a 5 percent reduction in the code around some jump instructions. Meta Ware is working on a global optimizing version of the C compiler, and the new version is expected to see performance improvements of 20 to 40 percent over the old version, according to Thomas Pennello, vice-president.

Using a template-matching technique, the Logic Systems Division of Hewlett-Packard (Colorado Springs, CO) has produced optimizing C cross-compilers for the Motorola 68000 and 68020, and similar compilers are being developed for Intel processor chips. Template matching takes advantage of special addressing patterns that chips like the 68020 can perform very rapidly. These patterns are often complex and may involve indirect or memory-referenced addressing with offsets. The compiler compares templates describing these patterns against the user's code to discover where machine cycles can be saved by substituting the patterned forms for existing addressing sequences.

Template matching, says Chris Jones, software design engineer at HP, has let the compilers achieve favorable optimization results with relatively little use of global optimizations. In the future, though, more-global compiler optimizations will probably also be used, Jones says.

Based on ANSI C language standard specifications for library functions, the compilers from HP replace many C calls with in-line code. Trigonometric functions and string operations, for example, are automatically placed in-line wherever calls to those functions exist in the source code. This eliminates the machine cycles required to execute the function calls and also makes the function code available to the compiler, along with other in-line code, for transformation by peephole and other optimizations.

Diab Systems (Foster City, CA) has an optimizing compiler that makes use of scratch registers and in-line multiplication. The D-cc compiler produces code for processors such as the 68000, the 68020 and the 32000. Variables tagged with the C register declaration are placed in registers by D-cc. The compiler then assigns the most frequently used of the remaining variables to whatever registers are available, including registers usually designated for scratch operations. Multiplications are performed in-line by shift, add and subtract machine instructions, rather than by subroutine calls.

C compilers from Sierra Systems (Oakland, CA) generate code for 68000, 68010 and 68020 processors. According to Sierra owner Larry Rosenthal, these compilers pay a lot of attention to placing as many items as possible into registers. Results are placed in registers, where they can be used during subsequent operations.

User controls needed

Although optimization can be a powerful weapon to increase code speed and decrease code size, it's a two-edged sword that can also produce undesirable effects. If loop optimizations are performed indiscriminately, for example, a lot of compile time may be spent in optimizing rarely executed loops. Many other problems can arise through optimizations, including code breaking.

These potentially destructive aspects of optimization create a dilemma for compiler vendors. Users want as much optimization as they can get, but powerful optimization can sometimes disrupt, rather than improve, some programs. In the marketing battles that rage between compiler vendors, an optimizing compiler that breaks user's code is viewed by vendors not as a powerful tool that has to be carefully handled, but as an unacceptable liability. The result is that many compiler vendors have chosen to limit the optimizations they provide to those that they believe can be safely employed and offer users little or no control over the choice of optimizations.

At the same time, an alternative approach appears to be taking shape, in which compilers are equipped with optimizations that are as powerful as possible, while users are offered the option of selecting which optimizations will be brought into play for their applications.

Virtually all optimizing compilers offer user control in the form of a software switch that will turn all, or most, optimizations on or off. Most of these compilers also offer a switch to select between optimization for speed and for code size. Some compilers, like those from Green Hills Software, offer a much larger variety of optimization controls. In addition to on-off and speed-size controls, the Green Hills C-386 compiler provides switches for peephole optimizations; deletion of code that stores into or reads from variables that the program never uses; assignment of user-defined local variables to registers only when the user specifies them as register variables; and automatic assignment of frequently used code and data addresses to registers. Users can also turn on or off optimizations that move invariant expressions out of loops, and they can order the optimizer to perform advanced loop optimizations.

The implications of user controls can be complex. There's a Green Hills compiler switch, for example, that causes all user-defined variables declared as register variables to be allocated in memory. This switch is specifically designed to overcome C setjmp-longjmp problems that arise in some Unix programs. The setjmp function saves the contents of registers, stack context and program counter. The longjmp function restores this information and continues execution where it left off. If a variable is modified after setjmp, however, the modified value will be lost when the variable is retrieved by longjmp. If a program's outcome depends on restoration of all variables by longjmp, the optimizing C compiler may break that program.

The user controls made available by Green Hills by no means exhaust the possibilities. The Portable Code Optimizer from HCR (Toronto, Ontario, Canada), for example, gives the user control over whether the compiler will generate in-line code that includes procedures called by the source code. This in-line procedure expansion eliminates calls made by the source code and places copies of the called procedures into the in-line code, giving the optimizer a more comprehensive view of all the code to be executed.

Optimizing C compilers generally respond not only to switch controls, but also to the keywords called for by the upcoming ANSI standard for C. Thus, when a variable is tagged with the C volatile keyword, the compiler will go to memory for that variable and won't attempt to use optimizations that rely on the presence of that variable in a register. Thus, if a variable can be changed by an interrupt, that variable should be declared volatile in the source code. The C no-alias keyword declares that a variable can be changed by name only, not through pointers or other manipulations. Given that information, the compiler can use optimizations that aren't trustworthy when aliasing can exist.

Use of numerous controls to steer the optimization process raises the possibility of overly complex compiler-use procedures that could wipe out the labor-saving advantages offered by automatic optimization. Some vendors, such as Silicon Valley Software (Cupertino, CA), are trying to reduce the complexity by limiting user choices to a few levels of optimization. Silicon Valley Software's C compiler offers a choice of full optimization or an intermediate level of optimization, in which in-line use of library functions is restricted and registers are used for only one variable during a block of code. A third level offers minimal optimization. In the company's Fortran compiler, there are five switch-selectable levels of optimization.

Tackling optimized bugs

"Debugging highly optimized code can be a real nightmare," says Steve Glanville, president of Silicon Valley Software, and most vendors of optimizing compilers agree. Users want the best optimizations they can get. If they find a way to save a byte or a machine cycle in the compiler output, they want to know why the optimizer didn't squeeze that added performance out of the code. At the same time, they want to do source-level debugging of the optimized code. But with the currently available debugging tools, source-level debugging of highly optimized code doesn't appear to be available.

Optimization can make it difficult to unravel what a program is doing and to locate problems that have to be fixed. After optimization, the relationship between statements in object code and in the original source code can become ambiguous. Instructions from one source statement can be scattered widely, for example, or instructions from different source statements can be com-

```
int array[500] [50];
int total;
column_total(column)
int column;
(
        int row;

        for( row = 0; row < 500; row + + )
            total + = array[row][column];
)
```

Optimized Code

```
_column_total:
        moveq     #0,d1
        move.w    (6,sp),d0
        lea       _array,a1
        asl.w     #2,d0
        adda.w    d0,a1
        movea.w   #500,a0
L16:
        move.l    (a1),d0
        add.l     d0,_total
        lea       (200,a1),a1
        addq.l    #1,d1
        cmp.l     a0,d1
        blt       L16
        rts
```

Nonoptimized Code

```
_column_total:
        move.l    d3,-(sp)
        move.l    (8,sp),d3
        moveq     #0,d1
        movea.w   #500,a1
        lea       _array,a0
L16:
        move.l    d1,d0
        move.w    d3,d2
        mulu.l    #50,d0
        ext.l     d2
        add.l     d2,d0
        move.l    (0,a0,d0.l*4),d0
        add.l     d0,_total
        addq.l    #1,d1
        cmp.l     a1,d1
        blt       L16
        move.l    (sp)+,d3
        rts
```

The Sierra Systems C compiler can eliminate a time-consuming multiplication from a loop computation, replacing it with an addition. This improvement is possible because a new variable is created that remains proportional to the loop control variable. The address of the first array element to be referenced is loaded into register a0. In the optimized object code, the constant 500 is moved into a register outside the loop to save compute time. Also, the loop control variable is tested at the bottom of the loop, so there's no need for a possibly time-consuming unconditional branch.

bined so that an object code statement can perform an operation called for by two different source code statements. In such situations, there seems to be no accurate way to show a source statement that corresponds to the optimized object code.

There may also be ambiguity in variable values. During execution of optimized code, users may find that changes in variable values don't follow the order suggested by the original source code. When breakpoints are set in source code, their application to optimized object code can also be ambiguous. These ambiguities make it difficult to debug optimized code. When global optimization is performed over entire procedures, there's frequently no way to resolve the ambiguities, and the usefulness of information that's offered by conventional debuggers becomes very limited. Debugging optimized code is a particularly nasty problem because it tends to come at the end of the code-development process, when schedules are tight.

Source-level debugging software

There are several vendors that offer source-level debugging software on the basis that it can handle optimized code, but Silicon Valley Software appears to have moved further than most toward that goal. The company's debugger relies heavily on information passed to it from optimizing compilers. The optimizer may decide, for example, to use a stack pointer instead of a base pointer for local variables, and the debugger must know of this so it will use correct relative addressing. Or, after optimization, a variable may be in a register for 10 statements, then returned to memory and later moved to another register. The debugger must be informed of these movements. The Silicon Valley Software debugger keeps track of such information. The debugger doesn't attempt to keep track of pieces of source code statements that may become scattered in optimized object code; instead, it looks only for the result of each statement.

But the Silicon Valley Software debugger can do its work only because the optimizations that the company's compiler performs have been carefully chosen. "In some places, we don't generate code that might be better because we wouldn't be able to keep the debugger working properly with that code," says Glanville. For example, dead variables not used to produce output could be removed by the optimizer, but such variables may be needed for checking during debugging. With the optimizations currently in use at Silicon Valley Software, the resulting effects on variables during execution occur in the same order as they were called for in the source code. Optimizations that could change that order simply aren't used in the company's compilers. "We're doing a code generator for the Motorola 88000 RISC processor, and we're finding that we can do amazing amounts of optimization for that chip. We want to pull out all the optimization stops," Glanville says. "But if users can't figure out what their optimized programs are doing, all that will be of little use."

"Debugging highly optimized code can be a real nightmare."
—Steve Glanville
Silicon Valley Software

As experience with optimization accumulates, compilers will offer increasing capabilities to automatically make code faster and more compact. Users are likely to insist on greater ability to control optimization and tune it to their specific applications. Debugging optimized code will continue to be a problem until new techniques are developed, but as long as auto-optimizing plus debugging takes less time than manual optimizing plus debugging, optimizing compilers will continue to improve programming productivity. **CD**

Our ASICs

are boring.

They're easy to design. They're ready on time. And first-time success is virtually 100%.

You've heard all about the excitement of ASICs.

They improve performance, lower costs and make many new designs possible.

But, unfortunately, you've probably also heard about one big potential problem: while many ASICs pass the tests specified by the designer, they don't always work in the real world. And that causes excitement you can do without.

How to get first-time success.

It starts with our Design Simulation Software. It's been rated the best in the industry by the people who should know—designers who have used it. Within three days, you can be up to speed, working at any of the major workstations in the industry, creating and revising your ASIC with ease.

The standard cell advantage.

You'll really appreciate the power of our standard cells, which allow you to integrate a whole system, including macros, memories, logic and peripherals, onto a single chip.

We have cells with effective gate length as small as 1.5μ (.9μ coming soon). And double-level metal for higher-density chips that can handle higher clock speeds.

You can choose from a wide range of Supercells, including the leading-edge RS20C51 core micro, RAMs, analog functions, bit-slice processors, HC/HCT logic, Advanced CMOS Logic, and high-voltage cells.

If they aren't enough, we can even generate Supercells to your specs.

And we're also in the forefront of silicon compiler technology. So we can offer you the ability to create designs that are heavily BUS-structured, with your ROMs, RAMs, PLAs and ALUs compiled right into the design.

We also bring you the resources of some very powerful partners, thanks to our alternate-source agreements with VLSI on standard cells; WSI on macrocells and EPROMs; and a joint-development agreement with Siemens and Toshiba on the Advancell® library of small-geometry cells.

Gate arrays, too.

If gate arrays are better for your design, you'll be able to choose from our full line up to 50,000 gates, with effective gate length as small as 1.2μ and sub 1 ns gate delays.

These gate arrays use "continuous gate" technology for up to 75% utilization. They are an alternate source to VLSI Technology arrays.

We also alternate source the LSI Logic 5000 series.

And we have a unique capability in high-rel ASICs, including SOS. Our outstanding production facilities here in the U.S. produce high-quality ASICs in high volume at very low costs.

It almost sounds exciting for something so boring, doesn't it?

For more information, call toll-free today 800-443-7364, ext. 25. Or contact your local GE Solid State sales office or distributor.

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

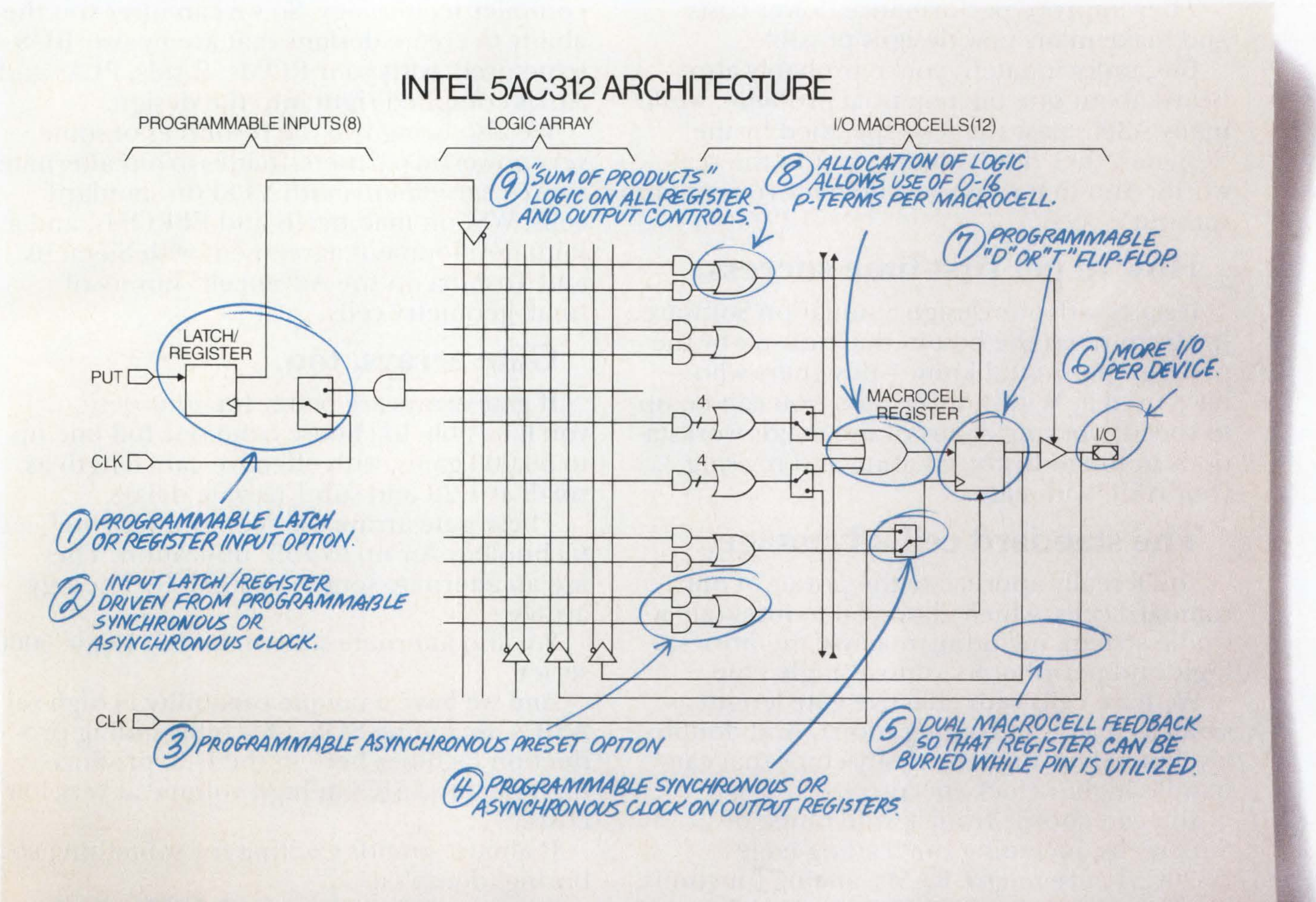
USA

GE Solid State

GE/RCA/Intersil Semiconductors

Three great brands. One leading-edge company.

9 REASONS TO CHOOSE INTEL FOR YOUR EPLD DESIGN.



If you're looking for architecturally advanced EPLDs, look no further than Intel's innovative product family.

Start with our 5AC312. Based on Intel's 1.0-micron CHMOS* EPROM technology, this high-performance EPLD clips along at 50MHz with a very low power consumption of only 50mA, 150μA while idling in low power mode. And its enhanced programmable inputs can be configured as latches, allowing the 5AC312 to latch and hold data—a must for complex microprocessor-

AND 12 MORE.

and microcontroller-based systems. Plus you'll save valuable board real estate and improve overall system performance.

In addition, the 5AC312 has an exclusive programmable product term allocation scheme. It improves device utilization up to 33% and boosts performance by allowing implementation of applications requiring complex logic functions.

But we didn't stop there. These 5AC312 features are being incorporated into future EPLDs with even higher integration. So your upgrade path is assured.

But, architectural innovation is not the only reason to design with Intel's highly advanced EPLDs.

Even though these EPLDs offer more than six times the logic density per chip than other PLDs, we've dramatically simplified your design process. With our inexpensive and powerful PC-based development tool, iPLDS II, you can use your PC/XT,* PC/AT,* PS/2* or fully compatible system to turn EPLD design concepts into working silicon quickly, automatically and efficiently.

Of course, we provide extensive technical documentation to help you in system design. And, to make it even easier, we've taken service one step further. To ensure that the design process is as smooth as possible, users have access to Intel's toll-free EPLD "Logical Hotline" and a 24-hour electronic bulletin board for any technical assistance they might need. It saves hours of valuable time.

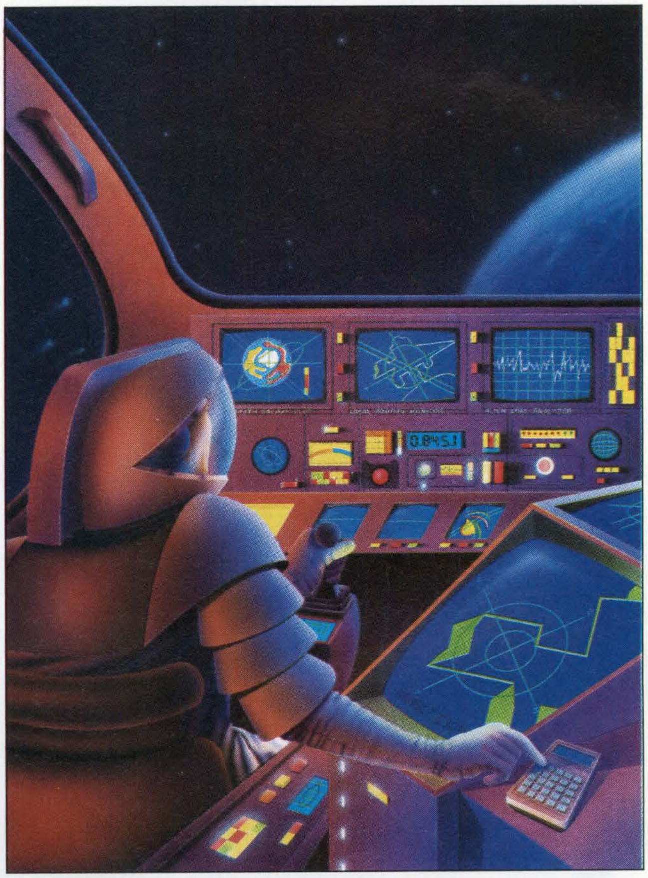
Best of all, the entire Intel EPLD family and all the development support you need are available now.

So call (800) 548-4725 and ask for Literature Dept. #W457. We'll tell you everything you need to know about the most technologically innovative EPLDs around.

Intel's 5AC312.
And family.

intel®

Computers on the move: Designing for portability



Whether they're portable, transportable or mobile, and whatever form they take—whether an inexpensive hand-held calculator, a laptop computer, a digital oscilloscope, a laser printer, or a heart monitor—computers on the move are the quintessential example of the importance of system design.

Unencumbered by limitations of size, weight or power consumption, designers of computers 15 to 25 years ago could tackle the design of individual computer components more or less independently of each other. The size and shape of the input—usually a keyboard—didn't pose serious ergonomic consideration. The CRT reigned as king of the display technologies, and because few people needed to move the display from place to place, a little extra bulk in a power supply didn't give a designer sleepless nights. Who worried about packing 40 Mbytes of storage into a tiny package that could withstand the shock of falling off an airplane seat? And so what if the guts—the electronics—burned up 1 or 2 kW?

No designer has these luxuries today. The demand for high performance, compactness, user-friendliness, low power and, if not low cost, then optimal cost, is forcing design teams to take the system view of design. This calls for trade-offs to be made between *every* component in a product. This means trade-offs between the type of display and power consumption; between the type and price of the input and the ergonomics of the input; between the performance of the system and the cost, size, number and power drain of the ICs used; and between the cost, capacity, durability and power consumption of the mass storage.

We hope that this Special Report will give designers, and especially design managers, some extra insight into these trade-offs—and, consequently, some extra insight into system design.

Size and power constraints guide IC design choices

Ron Wilson, Senior Editor

The demand for increased portability poses obvious problems for mechanical designers, display designers and power-supply engineers. For circuit designers, the challenges—though less apparent—are just as real. Digital designs, from the "luggable" personal computer to the hand-held instrument, are evolving to accommodate the requirements of smaller spaces and limited power. Whether the changes take place at the system, module or chip level seems to depend on the degree of portability the design requires.

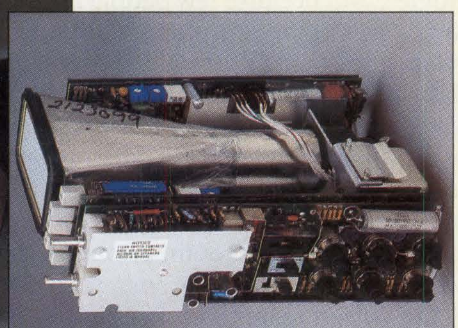
Luggable systems, the largest portables, are those that can be carried by an average-sized person or that can fit under an airline seat. This definition encompasses a variety of products, from early portable PCs—such as the Osborn and Kaypro models—to the most recent and considerably more compact lunchbox-style machines. Also included are instruments designed for in-field use, such as portable oscilloscopes.

For the electronics system designer, luggable systems have two key characteristics that distinguish them from smaller portables. First, space, while limited, isn't so constrained that it forces the designer into highly integrated technologies. Second, luggable systems include a power cord and aren't intended for battery-based operation.

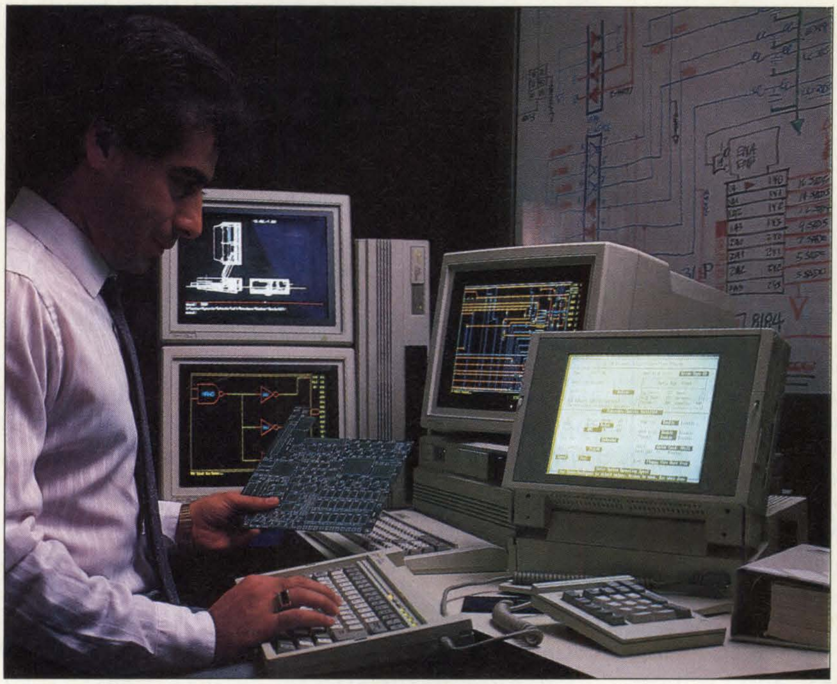
These two factors make luggable portable systems much more like desktop than laptop designs. "Portability necessarily means limited real estate and crowded air flow. But to understand the implications of that generalization, portability has to be defined further," explains Volker Dolch, president and founder of Dolch American Instruments (San Jose, CA).

"A lunchbox-sized system, for instance, requires diligence in packaging design and in cooling," he continues. "But it doesn't require compromises in performance relative to desktop systems." For example, Dolch's 386 portable PCs use essentially the same architecture as 386 desktop machines. With advanced architectural features such as RAM caching, the portable 386 boasts the same 4- to 5-Mips performance as the fastest desktop 386 machine.

Luggable portability, then, requires careful attention to detail, but doesn't necessarily require changes in architecture from that of desktop systems. Space, power and cooling in a luggable design



Calvin Diller, business unit engineering manager for hand-held products at Tektronix, studies design data for the new TX213 hand-held oscilloscope. As portable systems shrink from the luggable to the laptop to the hand-held level, the influence of size and power constraints increases.



A Zenith Data Systems engineer designs the company's Turbosport 386, an 80386-based laptop computer. Representing significant advances in display technology and intelligent power management, the Turbosport 386 and the company's 80286-based Supersport 286 rival the performance of desktop IBM PC compatibles.

are generally sufficient for the needs of desktop PC hardware.

When a system shrinks from a 20-lb box to a laptop package, however, the design ground rules rapidly begin to change. Space is painfully scarce in a laptop system, and any space there is must be reserved for unshrinkable modules such as displays, disk drives and connectors. Enclosures are designed for appearance and size, leaving no room for considerations like air flow. Perhaps most critical, the laptop device has to operate for extended periods on battery power.

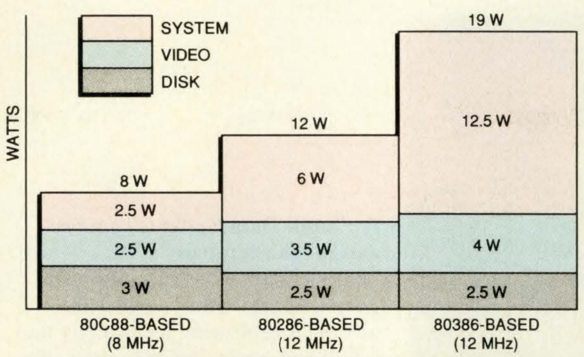
These constraints prevent the designer from simply repackaging a desktop system, with a few changes in peripherals, to make a laptop system. Design strategies to minimize local heating and reduce operating current must be incorporated at the system level, before hardware implementation even gets underway.

The first step for most vendors in designing a laptop system is to use CMOS circuitry exclusively. "Use of CMOS is fundamental to our design approach," says Kevin Mankin, product development manager for computer systems at Zenith Data Systems (Glenview, IL). "It offers us three characteristics. First is the level of integration we need to fit a high-performance computer into a laptop package. Second is partitioning flexibility. Third is the ability to manage power consumption."

According to Mankin, power management goes beyond simply using low-power circuitry. "We can use a number of more active techniques to limit current consumption. One is to operate the CPU at a lower clock frequency when high computing performance isn't necessary," he says. Since CMOS power dissipation is more or less proportional to operating frequency, running the CPU at reduced speeds can dramatically cut CPU, peripheral-chip and memory current requirements.

A more radical approach to power management for laptop systems involves discretionary powering of subsystems. Most PC users are familiar with this technique for floppy disk drives, in which the drive is kept rotating only when the controller believes it's in use. The same concept can be applied to circuits, resulting in significant power savings. "In our video controller, for instance, the section that controls the LCD panel operates at CMOS logic levels, conserving power. The RGB outputs for an external CRT, which will be used only when the laptop computer is sitting on a desk and plugged into the wall, run at higher-power TTL levels. But this section of the controller is shut down when we are running on the battery," says Mankin.

Chips and Technologies (San Jose, CA), a company that has taken an active interest in the special needs of highly portable PCs, has also addressed the problem of selectively powering down the system. "At the laptop level, the system has to use its intelligence to minimize power consumption," explains Sikander Naqvi, product marketing manager



While a portable computer's display and disk drive(s) have a significant impact on the total power demand, the particular chips used in a system, amount of electronics included and nature of the internal architecture also take their toll. All other things being equal, a higher-speed CPU and support components carry a power penalty since CMOS power dissipation is approximately proportional to operating frequency.

at Chips and Technologies. "This means knowing when to cycle power on floppy disks, and even on hard disk drives.

"In addition, the electronics itself has to be involved in power management," he continues. "For instance, processors and support chips, such as our Neat chip set used in Zenith's Supersport, must be able to run at a range of clock rates. The shift between 8 and 20 MHz in a PC AT has great influence on power consumption."

To conserve power during the long idle periods that characterize PC use, the processor chip set must be able to go to sleep gracefully, as well as to wake up gracefully when something important happens. Laptop vendors use various techniques for powering up and down. "For the chip vendor, that means we have to provide support chips that can get register contents into nonvolatile RAM when the system goes down, but can still monitor modem or keyboard activity and get the CPU to resume normal operation when data comes in," explains Keith Angelo, graphics operation product manager at Chips and Technologies.

It's evident that at the laptop level, system designers seem content to take a modular approach to power management. They identify modules that don't have to operate all the time, isolate them from circuitry that must run continuously and selectively shut them down when they aren't needed. This coarse-grained approach to current-hoarding has brought about laptop machines that can operate for several hours on an internal battery pack and can even support intermittent operation of a hard disk drive for limited periods.

As systems grow even smaller, moving from the users' laps into the palms of their hands, size and power constraints inspire even more radical design techniques. There is also more concern in the hand-held market regarding cost. "Customer expectations are different for hand-held systems," says Calvin Diller, business unit engineering manager for hand-held products at Tektronix (Beaverton, OR). "Customers believe that hand-held products ought to be less expensive than larger models and that they must be light."

These two factors work together to focus the system designer's attention on power consumption, according to Diller. If the device's circuitry consumes a little more current, then it will need a little more battery power, thus increasing both the size and the weight. In addition, added current consumption eats away at battery operating time.

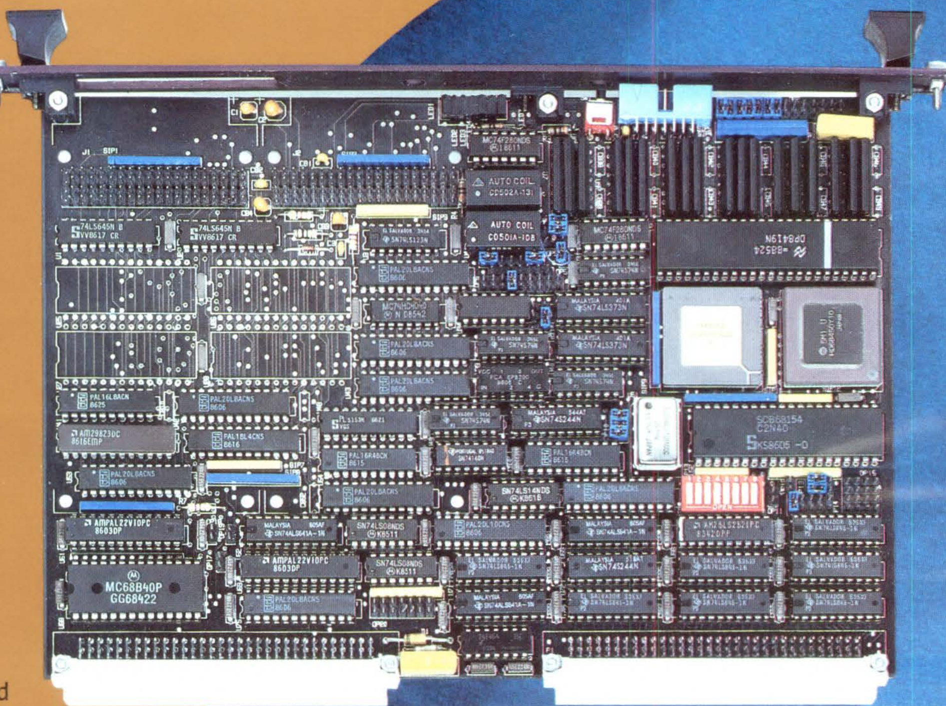
Under such severe constraints, power management must begin in the planning stages and carry on through the design process. "The architectural choices you make early on will drive cost and power dissipation all through the project," says Diller.

One weapon in the unrelenting war fought by designers is system partitioning. Originally, in all-CMOS systems, the most common technique was to identify power-hungry devices and isolate them from devices that could be run at lower power. The bulk of the system's circuitry could be designed for minimum current using the best CMOS process available. The isolated high-current circuits, such as analog devices or very fast logic, could be fabricated separately. Thus, the number of components fabricated in power-hungry technologies could be held to an absolute minimum.

With the availability of semicustom BiCMOS processes, a new strategy is available to designers. Now it's possible to mix high-current and very low-current devices on a single chip. "Using the new mixed technologies, you can eliminate power-hungry interface circuits that ship data from chip to chip," says Diller. "For instance, you may be able to combine an amplifier, an analog-to-digital converter and supporting logic on one chip. This way you can avoid the interconnect and package pin-related capacitive loading that requires high-output drivers."

Diller points out that cooling under difficult circumstances is also typically a problem for the small systems. "Hand-held equipment is subject to greater extremes of operating temperature than are less portable systems. This can create a real problem, because you may find that you are operating outside the commercial temperature limits, but you can't afford the additional cost of military-grade

Over 3800 Standard Configurations From Our New VME SBC



OB68K/VSBC1™ With OMNIMODULE™ I/O Modules

The OB68K/VSBC1 with its OMNIMODULE modular I/O and other options can be configured over 3800 unique ways. This gives you an off the shelf VME single board computer that is customized for your application.

Whether your quantity requirements are large or small, you get a cost effective board with just the features you need. And, you get it when you need it, without long lead times or custom engineering charges.

The standard features include:
- 12.5 MHz 68000
- 512KB of dual-access, zero-wait-state RAM with parity.
- (4) 28-pin ROM sockets (up to 256KB).
- (3) 16-bit timer/counters.
- (2) OMNIMODULE I/O module sockets.

Optional features include:
- 10 MHz 68000 or 10 or 12.5 MHz 68010.
- 2 or 4 channel DMA.
- VME bus interrupt generator (68154).
- 4 level VME BUS arbiter.
- Up to (2) OMNIMODULE I/O modules.

Fully loaded, even with 2 OMNIMODULE's, this board fits into just one VME slot.

Today your choice of OMNIMODULE's include:
- Kluge prototyping module
- (2) asynchronous RS232C serial ports.
- (2) synch/asynch RS232C serial ports.
- (2) asynchronous RS422 serial ports.
- (20) lines of parallel I/O.
- And more to come!

OMNIMODULE I/O lines are brought out to your choice of front panel or P2 connector.

For a free data sheet, to learn about the latest OMNIMODULE or to find out how you can have a custom SBC for your application, contact our Marketing Manager, Peter Czuchra at **1-800-638-5022** or **(312) 231-6880** in Illinois. Send $10.00 for a detailed technical manual or a copy of our OMNIMODULE specification.

OMNIBYTE™

OMNIBYTE CORPORATION
245 W. Roosevelt Road
West Chicago, IL 60185-3790
In IL (312) 231-6880
Intl. Telex: 210070 MAGEX UR
Fax No. 312-231-7042
CALL TOLL FREE
1-800-638-5022

A Look At Today . . . A Vision Of Tomorrow.

parts.'' Partitioning to spread out power dissipation can help in some cases.

In general, Diller believes that designers have to reassess their system architecture in the light of each new IC technology. ''The switch from separate technologies to BiCMOS has major implications for portable systems,'' he says. ''With these mixed technologies available, you shouldn't trust your old partitioning assumptions anymore.''

Just as power management is critical at the system partitioning level, it's important within the IC. A whole range of techniques, from reducing frequency to putting subsystems to sleep, is used by chip designers in highly integrated semicustom work. Some of the most commonly used tools for managing power are cells with sleep modes and a range of fully static cells that can be halted for indefinite periods without loss of data. Exploiting these tools results in a chip with extremely sophisticated power-management functions.

One example of an existing design that has used a variety of power-management techniques is the new 32CG16 printer/display processor from National Semiconductor (Santa Clara, CA). ''For applications such as portable facsimile machines, we felt it was imperative to manage power within the CPU,'' says Robert Freund, group director for microcomputer systems software at National.

One factor Freund claims can improve power consumption is the instruction-level architecture of the CPU. ''A rich complex-instruction-set computing architecture can significantly reduce the amount of code needed for a given task, decreasing the amount of static RAM the system must support. Also, the architecture must provide enough registers to maintain keep-alive data in a sleeping system, where the memory has been powered down and the CPU is on standby.''

At the hardware level, the 32CG16's designers have taken several measures to conserve power. Implementation of a fully static CPU that could be halted between clocks proved impractical. So designers of the National chip opted to implement a standby mode. In standby, an on-chip clock divider, under software control, divides the clock frequency by eight. This cuts current dramatically. Selected portions of the CPU circuitry are allowed to sleep, so the CPU only has to clock parts of the chip needed for the instruction being executed.

Such thorough measures in power management indicate the seriousness with which system and chip designers are treating the requirements of portability. In a market where laptop PCs are beginning to replace some desktop machines, where spelling checkers and telephone directories are expected to fit in a vest pocket, and where digital radio receivers have to ride along on a pair of headphones, designing for power management may become a pervasive discipline among semicustom architects. **CD**

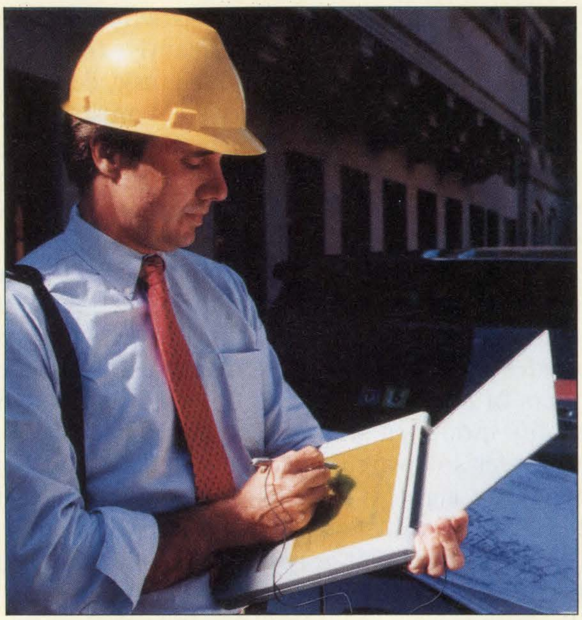
Keyboards shrink and other options emerge to boost portability

John H. Mayer, Senior Associate Editor

In many respects, input technology has been the weak link in portable-computer design. Over the last five years, IC manufacturers have migrated to low-power, high-speed CMOS; switching power supply designers have turned to higher switching frequencies and surface-mount technology to boost density by a factor of two or three; and disk drive vendors have found ways to pack 20 Mbytes of hard disk storage into a 1-in.-high box. Meanwhile, input technology has remained relatively static.

True, some developments foreshadow dramatic change in the near future. For desktop systems, application developers are increasingly using the mouse as a fundamental input vehicle. Trackballs and bar-code readers are also being used more. For deskless systems, touch screens provide an attractive method of data input as a menu-selection or low-volume data-entry device. And voice recognition will likely one day redefine the role of the user.

But despite these promising technologies, the prevailing vehicle for input on portable systems continues to be the traditional keyboard or keypad—with evolutionary advances. Keyboard designs have steadily decreased in parts count, incorporated higher-reliability switches, and used more compact and efficient layouts. More and more frequently, keyboard designs feature intelligence and



Because keyboard space isn't always guaranteed in certain environments, other input options such as touch screens are often necessary. With Linus Technologies' Write-Top portable computer, for example, handwritten alphanumeric data, signatures and hand-drawn sketches are entered via a stylus.

memory on-board, and some desktop versions even add other input peripherals such as bar-code readers or touch pads. Ergonomic issues are also playing a larger role in keyboard design, as system designers begin to realize how a seemingly minor issue like keystroke feel can have a strong impact on a product's success.

Indeed, designers must consider a variety of attributes when selecting a keyboard. Keyboards are available as custom or off-the-shelf items in an assortment of styles, shapes and technologies. Designers must also consider the feel of a keystroke, the key profile, the length of key travel and even the design of the keytops and key legends.

The keyboard represents one of the two primary points of user-system interaction (the other being the display). For that reason, the feel of the keys on a keyboard can significantly affect user acceptance. Since the late 1970s, keyboard designers, pushed by user demand, have moved toward a tactile rather than linear feel. Unlike a linear switch, which progresses consistently to the bottom of a key's stroke, a tactile switch reaches a threshold of resistance, usually marked by a click, followed by a reduction in resistance. That peak resistance gives the operator a clear message that the switch has made contact. "Tactile feel is attractive because it gives the operator an indication of a switch closure without having to fully travel the switch," says Craig Moss, senior electrical engineer at Advanced Input Devices (Coeur d'Alene, ID). "As soon as an indication is given, the operator can get off the switch and move to the next key, thus enhancing throughput."

For low-cost, portable applications in harsh environments, conductive elastomer switches can provide complete environmental sealing while retaining the tactile feel of full-travel keyboards. Not only do these switches seal the keyboard from water, corrosion and dust, but they also withstand significant amounts of mechanical abuse.

Conductive elastomer keyboards come in two types: silicone rubber and nonsilicone elastomer. Rubber keyboards keep cost to a minimum, but their shortened life expectancy limits them to micromotion tasks. For high-speed data-entry applications, nonsilicone elastomer keyboards have life spans of up to 60 million operations.

Advanced Input Devices offers a keyboard that uses a thin elastomer sheet molded into dome shapes containing carbon pads. When pressed, the dome collapses and the carbon pad makes contact with a printed circuit board underneath, shorting the circuit and closing the x-y switch. The buckling action of the dome delivers a natural tactile feel without the use of springs or complicated return mechanisms. Once pressure is relieved, the dome's inherent nature returns it to its original shape. By reducing parts count, the switch not only increases reliability, but limits keyboard cost and weight.

Conductive-rubber keyboards like the SF62000 series from the Microsystems Division of Marconi (Hauppauge, NY) offer a similar tactile feel. Each keyboard uses a profiled one-piece silicone-rubber mat that covers a prestudded 1.6-mm metal plate, sealing the flexible-polymer, thick-film switch elements from the environment. A lip around the edge of the silicone-rubber molding provides an environmental seal between the keyboard and the front panel. The keyboards can be scrubbed down or cleaned in any manner. For maximum positioner/connector versatility, a flexible, insulated tail fitted with a female 2.54-mm pitch plug connects with any male connector.

To provide tactile feedback, the silicone-rubber molding deforms when pressed and travels 1.4 mm. Inserts molded into the silicone rubber provide the moving-switch contacts. Each switch features a maximum contact bounce of 5 ms and a maximum contact resistance of 200 Ω. According to Marconi, the silicone rubber typically has a life span of 2 million operations. The series is configured in 4-, 12-

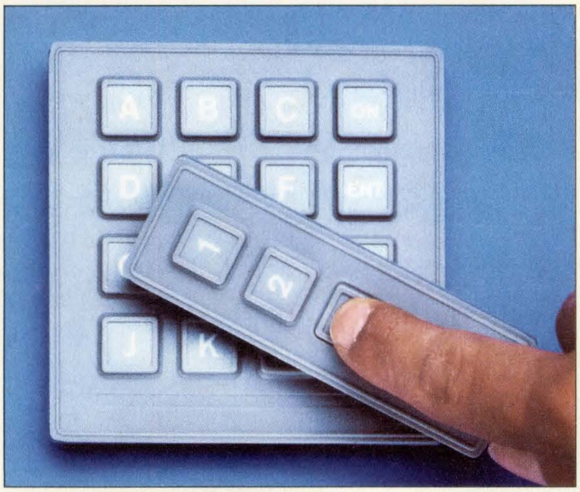
386/AT CHIP SET COMPARISON

	G2	C&T
CHIP COUNT	3	7
PROCESSOR SPEED	25MHz	20MHz
ADDITIONAL CHIPS NEEDED FOR FULL SYSTEM	14	33
MAXIMUM MEMORY	24MB	16MB
REGISTER PROGRAMMABLE CONFIGURATION OPTIONS		
MEMORY MANAGEMENT	106	NOT EVEN CLOSE
HARDWARE OPTIONS	28	NOT EVEN CLOSE
I/O CONFIGURATION OPTIONS	30	NOT EVEN CLOSE
CLOCK OPTIONS	26	NOT EVEN CLOSE

We have one more number for you.
408/943-0224.

G2

CIRCLE NO. 32



Marconi's SF62000 keypads combine the benefits of an environmentally secure rugged construction with the tactile feedback usually associated with full-travel keys. To meet military environments, the keypads operate over a $-55°$ to $+125°$ C range.

and 16-key keypads and a QWERTY keyboard. Custom versions are also available.

For truly low-cost implementations, few technologies can beat the standard membrane switch. The typical membrane switch sandwiches a sheet of polyester with holes in the contact areas between two layers of polyester film screened with a pattern of conductive silver inks. An overlay or keytop is attached to the top of the switch, and the entire package is attached to a rigid substrate.

Because of its sealed overlay, the switch is particularly advantageous in rugged environments. But its lack of tactile feel precludes it from fast data-entry tasks. In fact, this lack of tactile feel may drive designers away from the membrane switch even in settings that aren't speed-critical. At least one system designer has noted a recent trend by some printer manufacturers to move from membrane to other keyswitch technologies for setting printer options. "It's the stroke that really seems to be the determining factor," says Michel Burton, director of research and development at Datavue (Norcross, GA). "I think a lot of people just don't like the fact that the membrane switch doesn't move when you touch it."

To provide a full-travel feel with a membrane switch, vendors such as Keytronic (Spokane, WA) and Honeywell (El Paso, TX) offer keyboards in which the operator touches the membrane switch with a moving key. Honeywell mounts a rubber boot and a plunger mechanism over its contact and capacitance membrane switches. Called a silent tactile switch, the key gives a tactile feel but doesn't make an audible click.

One of the toughest challenges designers of portable systems face is implementing the functionality of a full keyboard in a constricted space. Most portable computer systems feature keyboards with 70 to 85 keys, well short of the 101 keys found on the popular IBM PC AT keyboard. "If you have a 79-key abbreviation, the market demands you have all the ways of generating every key and scan code that a 101-key keyboard provides," says Kevin Mankin, product development manager for Zenith Data Systems (Glenview, IL). Jim Bartlett, marketing manager at NEC (Wood Dale, IL), agrees. "To get the most use out of the space you have in a machine, you either have to use dual functions or become more creative in the way you lay things out."

Keyboard designers for portables have benefited from an early decision by IBM to put a function key, FN, on the lower left of its portable keyboard, notes Mankin. This particular key acts as a supershift key. It lets the designer combine, for example, FN with F1 and F2 on the portable keyboard to generate F11 and F12, which are found only on the larger, 101-key keyboards. "They could have screwed it up by moving the FN key to the desktops as well," he says. "But they kept it on the portables and made sure the software people wouldn't write special keys dependent on FN."

While adhering to the general space and weight limitations of a portable system's keyboard, the designer must provide the standard left-to-right spacing between keys and up-to-down spacing between rows found on typical desktops. "The size of the keyboard is pretty much fixed by the size of people's hands," claims Datavue's Burton.

There may be some ways around those limitations, however. One solution comes from Mechanical Enterprises (Herndon, VA). A direct replacement for the standard 101-key keyboard, its Microtype keyboard squeezes 100 keys into a footprint only 10¾ × 6 in., or roughly 60 percent the size of the standard 101-key keyboard. With only the redundant "Enter" key left off, Microtype saves space by bending the rules a bit. "We kept the spacing left to right the same because if you tighten it up you can't touch type on it," says company president Robert Twyford. "But we shortened the distance row-to-row and took advantage of that shortening by bringing the number, cursor and function keys above the alphanumeric section." In addition, the design uses a smaller key size, 3/4 in. wide × 5/8 in. high. Normal key size is 3/4 × 3/4 in.

Another way of gaining space while providing full 101-key compatibility is through a separate numeric keypad. Zenith offers a numeric keypad option on all three of its portable computers. Initially intended to satisfy the accounting community, the company's keypad provides an exact duplication of the adding-machine format accountants traditionally use. As a byproduct, the combination keyboard-keypad provides dedicated keys comparable to a desktop version. "You can take a compact 79-key package and take it up to 103 keys," says Zenith's Mankin.

For applications requiring quick menu selection and the repeated use of a few commands, touch screens offer an attractive input alternative in portable environments where desktop space isn't guaranteed. Touch screens are also useful in field environments, where portability is required and the user, often a technician, may not have complete knowledge of the portable test or measurement system in use. In addition, touch screens let the user focus on just the screen, rather than having to look from screen to keyboard while coordinating head and eye movements.

Four touch-screen technologies are being used. Optical, or infrared, panels cover the screen with a grid of invisible light beamed just in front of the display surface. Resistive overlay screens operate similarly to membrane keyswitches: a membrane substrate placed over the surface of the screen creates a uniform voltage gradient across the screen. Touching the screen causes electrical contact between the two layers of the substrate, sending a voltage measurement to the controller. Capacitive touch screens, on the other hand, have a glass substrate over the screen. When the screen is touched, the user's body capacitance activates the system. Surface-acoustic-wave screens, the fourth technology, transmit sound waves through a glass substrate. When a touch occurs, the pointing device absorbs a portion of the energy flowing in both the x and y directions, changing the energy that's measured at the surface.

Touch technology hasn't made dramatic inroads in portable systems for a number of reasons. For one, the screen's controller occupies a precious expansion slot and consumes some power. Image clarity has also been a concern. All touch systems that require a substrate placed on the system display involve some visual obstruction between the operator and the image on the screen. Some overlays on popular resistive-membrane screens can reduce light coming from the screen by 50 percent. For portable systems using marginally legible flat-panel displays, a loss in image clarity can be critical.

The image-clarity issue, together with cost and power issues, is a major reason why most touch-panel applications are on transportable rather than strictly portable instrumentation. Transportable systems usually aren't battery-powered and can afford to use power-hungry, yet bright, CRTs. One such example is the HP 16500 logic analyzer from Hewlett-Packard (Colorado Springs, CO). The HP 16500 features a very clean, button-free front panel. Instead of pushing keys and switches to set parameters and initialize operations, users operate the analyzer through a menu-intensive interface activated by an infrared touch system. Users can set parameters and initialize operations through a menu-intensive interface activated by touch.

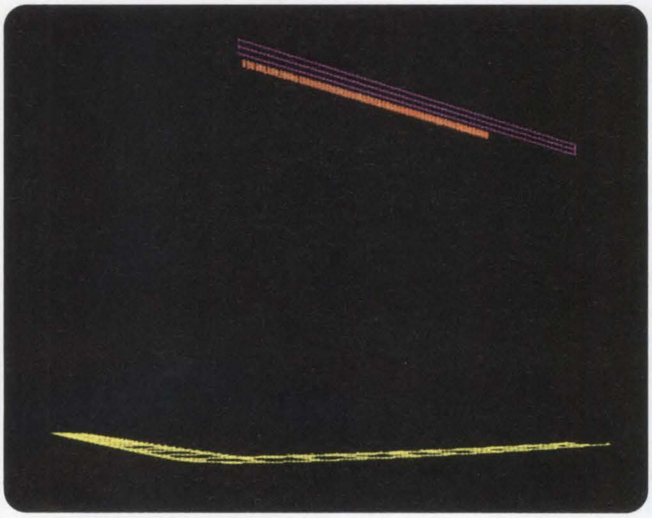
The cost, power and image-clarity issues don't entirely rule out touch screens in flat-panel applications. Ohmeda (Englewood, CO), for example, mounts a customized infrared touch system from Carroll Touch (Round Rock, TX) on a 512- × 256-pixel electroluminescent (EL) display as part of its multigas monitoring system. The monitor is wheeled into a patient's room or an operating room and is attached to a larger gas-generating machine. Medical personnel use the touch display to administer and monitor the level of gas.

Linus Technologies (Reston, VA) carries the touch-screen idea a step further. The company's Write-Top is a portable 8088-based DOS computer

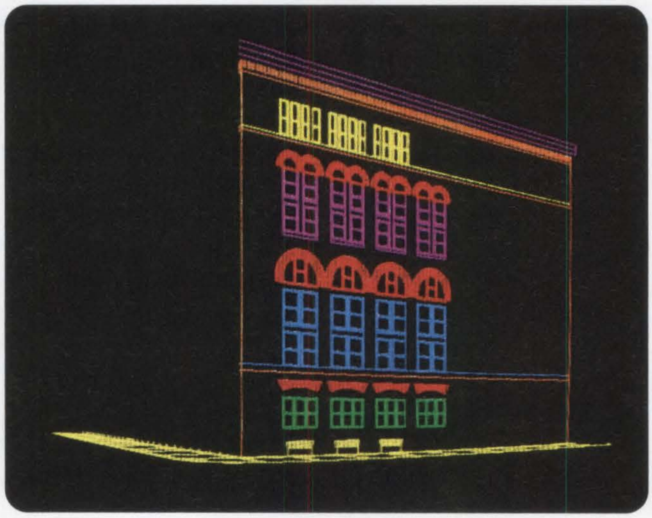
The addition of optional numeric keypads to laptop computers such as the Mitsubishi mp286L extends keyboard functionality to desktop levels. With the keyboard-keypad combination, compound actions on the base keyboard alone can be accessed with a single dedicated key.

National Semiconductor

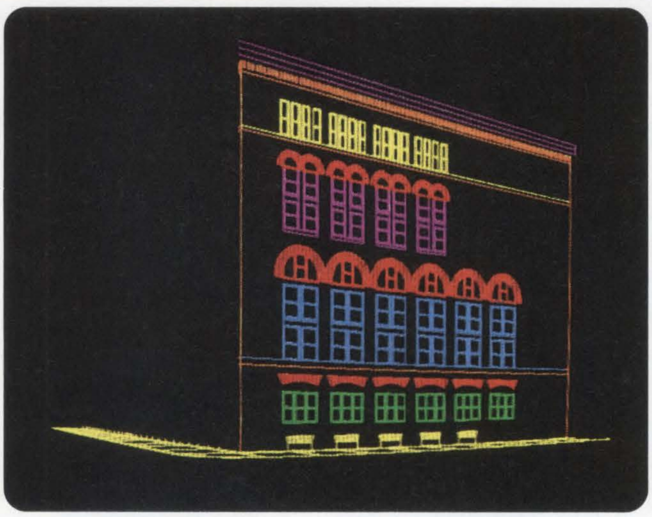
In the time it takes other graphics engines to draw a few lines...



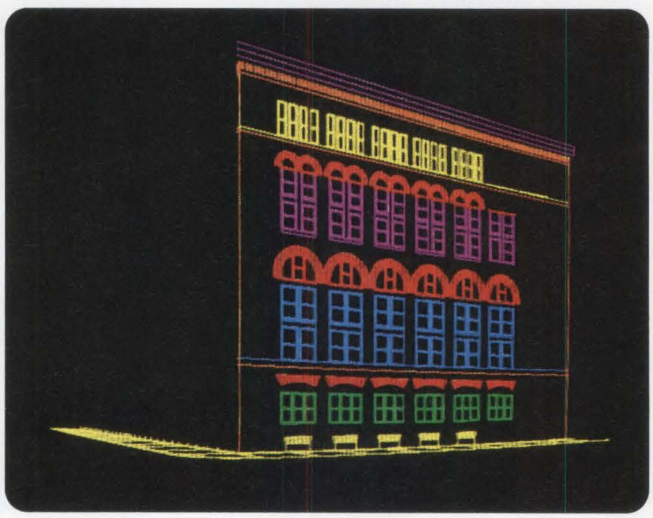
Texas Instruments TMS 34010 (2%)



AMD Am95C60 (17%)



Hitachi HD63484 (20%)



Intel 82786 (25%)

Simulated performance based on maximum patterned line-drawing rates in an eight-bit color system with a resolution of 1024 by 768. Of course, performance ultimately depends on system elements like memory speed.

ours gives you the whole picture.

THE FIRST FULLY PROGRAMMABLE GRAPHICS PROCESSOR WITH ON-CHIP ACCELERATION

You can have the fastest calculations in the world but if your system's graphics are slow, your system is slow. National's latest addition to its Advanced Graphics Chip Set — the DP8500 Raster Graphics Processor (RGP) — is the fastest graphics engine on the market.

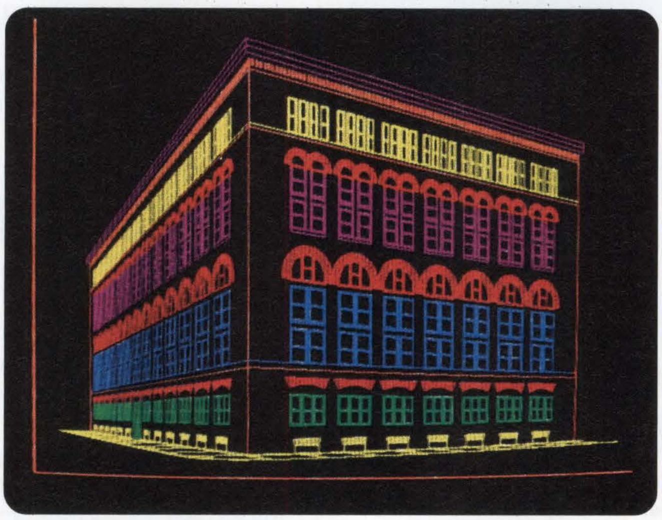
This 20-Mhz CMOS chip features a bus cycle time of 100 nanoseconds on back-to-back vector and block operations.

It gives you blazing speed in line drawing, BitBLT, fills, polygons, character drawing, and windowing — regardless of the number of bit planes. It also controls screen refresh.

COMPLETE FLEXIBILITY

The RGP gives you the programmability of a general-purpose processor, so you can optimize your system for specific applications. Or differentiate it from your competitors through proprietary algorithms.

The RGP, with our DP8511 BitBLT processing unit, is also the only graphics solution that effectively allows you to select either planar- or pixel-oriented operation on-the-fly. So you no longer have to lock yourself into one architecture or the other.



National DP8500 Raster Graphics Processor

The RGP handles the very highest-resolution CRTs and printers, including laser printers. And it supports any type of memory.

It also gives you the right "hooks" and the right architecture for moving into 3D and solids modeling applications.

A COMPLETE SET OF CHIPS

Our Advanced Graphics Chip Set also includes

- two BitBLT processing units
- four video clock generators
- four video shift registers
- three video RAM controllers
- a growing list of video DACs

They're all part of National's unique modular approach — the only approach that addresses the complete graphics pipeline. And the only one with the performance and flexibility you need to carry you into the 1990s.

COMPLETE SUPPORT

We offer a wide range of software tools — including assembler, debugger, librarian, linker, software utilities, graphics kernel packages, and a C compiler package.

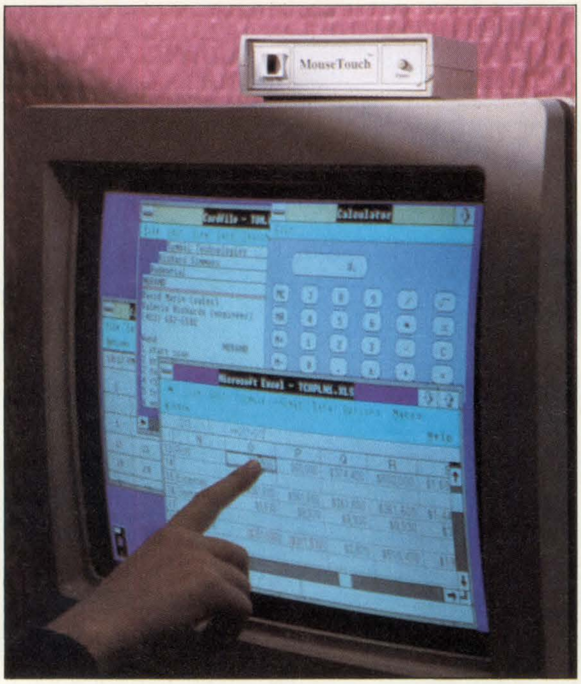
Nova Graphics International is providing full support for graphics software standards, including GKS and CGI.

Check it all out for yourself with the DP850EB demo/evaluation board for only $1495. Buy the board and we'll include a coupon good for ten free RGPs on your first order of 100 or more.

To order today, call National Semiconductor at (408) 721-5404. Or for a copy of our system-level comparison brochure, circle the reader service number.

National Semiconductor

CIRCLE NO. 33



All mouse functions, including single clicks, double clicks, and drag and cursor move operations, are executed by touch on Information Strategies' Mousetouch. The high-resolution (4,096- × 4,096-pixel) resistive-membrane screen from Elographics plugs directly into a serial mouse port.

that lets users write in script over its flat display. The system places a transparent digitizer over a supertwist, EL-backlight liquid crystal display. Users write directly on the display with a stylus, and a symbol-recognition algorithm recognizes the symbols based on a preestablished dictionary and translates them into ASCII.

"We take a sequence of points that is your writing, compare it to a lookup table of previously entered patterns and find the match," explains Ralph Sklarew, research and development director for Linus Technologies. "Then we take that character and stuff it in a keyboard buffer." Weighing only 9 lb, Write-Top is easily portable and sports 640 kbytes of internal static RAM, a memory card port, an optional 3½-in. disk drive, a modem and a keyboard interface.

As touch-screen resolution increases, designers can move to denser menu interfaces and input by devices more precise than the fingertip. Microtouch Systems (Woburn, MA) has developed an input device with light-pen functionality that's highly applicable to portable applications. Called the Penpoint Tablet, it's the first light-pen-type device designed for use with LCD, EL and plasma flat-panel displays. The low-cost transparent tablet also comes in a curved version for CRT environments.

The tablet combines a transparent glass sensor that mounts over the display with a low-power controller and a lightweight passive stylus. A durable resistive coating bonded to the surface of the glass sensor allows for almost complete light transmission. Power consumption doesn't restrict this input device from portable applications—the tablet consumes less than 0.1 W. Microtouch will also sell the sensor and stylus without the controller to OEMs desiring to build their own electronics.

Although portable systems offer many advantages, their very transportability can limit the use of certain input options. The best examples are the "point and pick" tools increasingly used by application developers. The ease-of-use of graphics-oriented interfaces like the Windows development environment developed by Microsoft (Redmond, WA) and the success of the Macintosh computer from Apple Computer (Cupertino, CA) have convinced many application developers of the benefits of the mouse as a fundamental input device. Complex applications like CAD and CAE use such input tools to simplify user interaction with the system. But how does one use a mouse on a portable system that's no longer tied to a desktop?

One solution may come from Information Strategies (Richardson, TX). That company's Mousetouch bundles a touch screen from Elographics (Oak Ridge, TN) with a specialized controller board to deliver complete emulation of all mouse functions. The touch screen plugs directly into a serial mouse port and offers complete mouse functionality without any application development, additional drivers or programming.

The screen used is Elographics' Accutouch, a high-resolution, 4,096- × 4,096-pixel resistive-membrane screen. Users imitate the mouse by simply touching the screen, similar to a single-click function on a traditional mouse. Two touches of the screen generates a double click. For drag operations, users hold their finger to the screen and move it to the desired location. "We have some timing algorithms that determine if you're in drag mode. If so, they automatically turn on our screaming mode, a function equivalent to holding down the button on a mouse," says John Baker, president of Information Strategies.

At present, Mousetouch is only compatible with desktops, including the Macintosh II, the IBM PC, PC XT and PC AT family, and 80386-based systems. But Information Strategies is moving quickly to accommodate the flat screens on portable sys-

TEK'S 1241 MICRO ANALYSIS SYSTEM: AT $9,950, THE CHIPS ARE REALLY STACKED IN YOUR FAVOR!

Tek's 1241 microprocessor analysis system includes the Tek 1241 Logic Analyzer. The micro support package of your choosing. Plus performance analysis, storage and communications options. At a total price of $9,950. If you're looking for a system to minimize your risk and maximize your return, this is the package you can bet on.

It's proven. The 1241 is known and accepted worldwide as the best of the leading logic analyzers.

It supports more than 45 microprocessors, microcontrollers and digital signal processors. That's more than any other logic analyzer. You can add additional micro support for as little as $400.

It comes with a specialist. Tek's dedicated logic analysis sales and applications engineers give you expert support whenever you need it.

It's the best deal on the table. For immediate value and long-term practicality, nothing else can touch it.

Call us. Talk to your local Tek sales representative, or call 1-800-245-2036 for more information about the total Tek 1241 package.

CIRCLE NO. 34 FOR LITERATURE
CIRCLE NO. 35 FOR DEMONSTRATION

Tektronix®
COMMITTED TO EXCELLENCE

tems. "It makes sense for portable applications because in a portable application you don't want to carry a mouse around with you," says Baker. "The only difference with a flat screen is that you use a light and flexible plastic touch screen rather than a glass-membrane screen."

The plastic screens, called Duratouch, are designed for use with EL, gas plasma and liquid crystal displays, and they're built in 4- × 8-in. and 6- × 9-in. formats. As on any resistive-membrane touch screen, the screen membranes consist of two thin sheets of plastic with transparent, conductive coatings on the facing sides of the plastic sheets. An array of clear, tiny elastic dots is sandwiched between the sheets, holding the sheets 0.001 in. apart. When a finger or stylus touches the screen, the outer sheet makes electrical contact with the inner sheet at the touched position. **CD**

LCDs make the leap to display of choice for low-cost portables

David Lieberman, Senior Editor

Today's three dominant display technologies for portable computing—liquid crystal (LCD), plasma (also known as gas discharge), and thin-film electroluminescent (TFEL)—have changed considerably within just a few years and continue to evolve. In the display arena, yesterday's truisms can quickly become passe. LCD, for example, no longer necessarily means a low-cost display of a correspondingly low aesthetic quality, nor does plasma or TFEL necessarily mean an overly expensive and power-hungry display. The old distinctions among flat-panel alternatives have started to blur. Tomorrow's incremental improvements and the development of new display technologies will likely keep this a dynamic market.

It's been about seven years since the first CRT-based portable computers appeared and about four since full-screen flat-panel portables made their debut and—by virtue of their slim profile, light weight and battery operability—forever changed the perception of portability. Just two years later, the inferior optical quality of standard twisted-nematic (TN) LCD technology for a 25-line × 80-character display was giving portability a bad name, though improved thick-film EL backlights were giving the technology a slight aesthetic boost and the ability to operate under dim ambient lighting conditions. At that time, there were rumors of a new technology—the supertwisted birefringence effect (SBE), or supertwist LCD—that might challenge the dominance of the TN display by significantly improving readability.

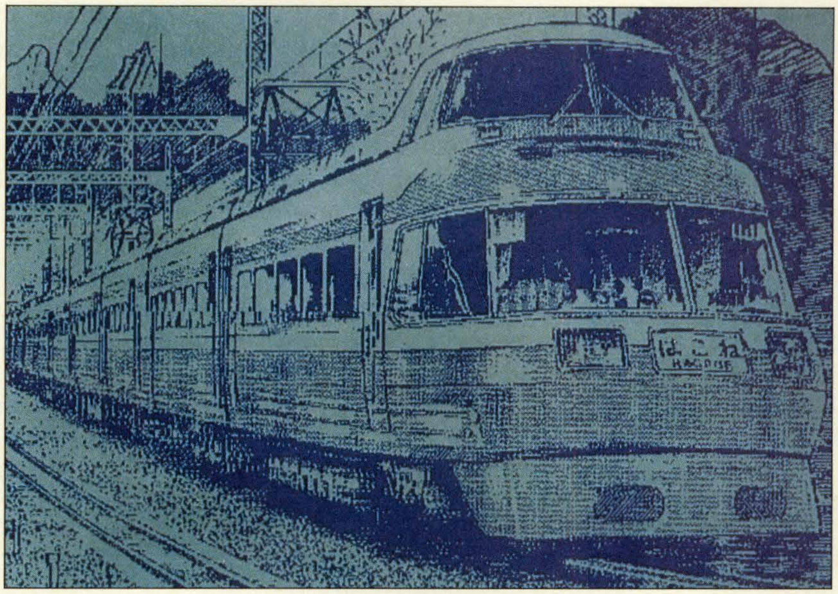
We're now in the heyday of the supertwist LCD, which rapidly replaced the TN LCD as the display technology of choice for low- and medium-cost portables and portables capable of long-term battery operation. With the appearance, however, of a new type of LCD—variously called neutral, neutralized, compensated and double-twist LCD—at this year's Spring Comdex and at this year's Society for Information Display conference, it looks as if the supertwists will soon be challenged.

The optics of supertwisted LCD molecules treat one narrow band of light differently from all the others, over- or under-rotating it in relation to the rest of the spectrum. "That one band is the stray band that gives the display its characteristic tinge," explains Kevin Mankin, product development manager at Zenith Data Systems.

Though the supertwist LCD makes for a substantially more readable display than a TN, its coloration (most commonly a blue tinge but, in some models, green, yellow or red) hasn't been well received by some segments of the user community, according to Jim Aden, vice-president and general manager of the Electron Tube Division of Hitachi America (Schaumburg, IL).

"Supertwisted LCDs improved contrast and viewing angle substantially and created a lot of excitement," says Aden. "Because of them, LCDs made a quantum leap forward in terms of acceptance. But one of their inherent problems is their coloration, and many people—engineers, marketing staff and users alike—were never comfortable with the color cosmetically." The temperature sensitivity of the supertwists, which causes them to darken perceptibly after a few hours of use, is also something some users have never gotten used to, according to Dave Matthews, national distributor sales manager at Sharp Electronics (Mahwah, NJ).

The double-twist display achieves its superior readability from the addition of an extra LCD layer that recaptures the light component lost in super-



The supertwist liquid crystal display is today's display of choice for low- to mid-range portables and for those that require extended battery operation.

Source: Densitron

twist. Though electronically passive, the compensating layer is always optically active, reorienting all bands of light to the same polarity to get brighter brights and darker darks than supertwists. "No matter what stray band the supertwist has," says Mankin, "the second layer will recapture the stray and give maximum contrast ratio."

The double twist is a black (or, at least, very deep blue) on white display whose color correspondence to paper and ink (still the dominant means of storing and sharing information) has a lot of aesthetic appeal. As Matthews says, "Double twist gives you double the contrast and a much cleaner looking background." Essentially, it looks like a printed page. The first double-twist screens appeared this spring—in 10½- and 11-in. diagonals, respectively—on a new high-end portable from Zenith and on the first portable offering from the Computer Systems Division of Mitsubishi Electronics America (Torrance, CA).

The readability demonstrated by double-twist LCD monitors is reportedly excellent and, says Mankin, it approaches or equals that of a CRT. "We watched the use of portables being hampered by poor readability," says Jens Moder, product manager at Mitsubishi. "But when we saw this display, we knew the time for the portable had come."

But double-twist LCDs (many of which are double supertwists) aren't without drawbacks. In these displays, it's primarily the greater twist angle of the LCD molecules—from 180° to 270°, compared to 90° for TN—that enhances their ability to efficiently block and transmit light. Yet the supertwisting and untwisting of molecules typically come at the cost of response time, and many of these displays have some difficulty providing smooth scrolling and cursor movement. "The greater twist and longer resistance to change buys you contrast," Mankin says, "but you have to pay attention to the circuitry to make sure that your response time isn't suffering."

Also, while backlighting is an enhancement that users have come to demand for TN and supertwist LCDs, it's an absolute necessity for the high-contrast, black-on-white double twist. "If you tried to use the double twist in a reflective mode, you'd need an awful lot of incoming light to make it readable," says Matthews.

The double twists also tend to need more intense backlighting than the familiar thick-film EL lamp can provide, fueling a movement to the fluorescent tube—which, of course, involves trade-offs (see "Let there be backlighting" on p 80). The high contrast of double twists and the larger screen sizes that this contrast permits makes greater demands on backlighting in terms of both brightness and coverage. The extra compensating layer of the double twist also contributes to light attenuation.

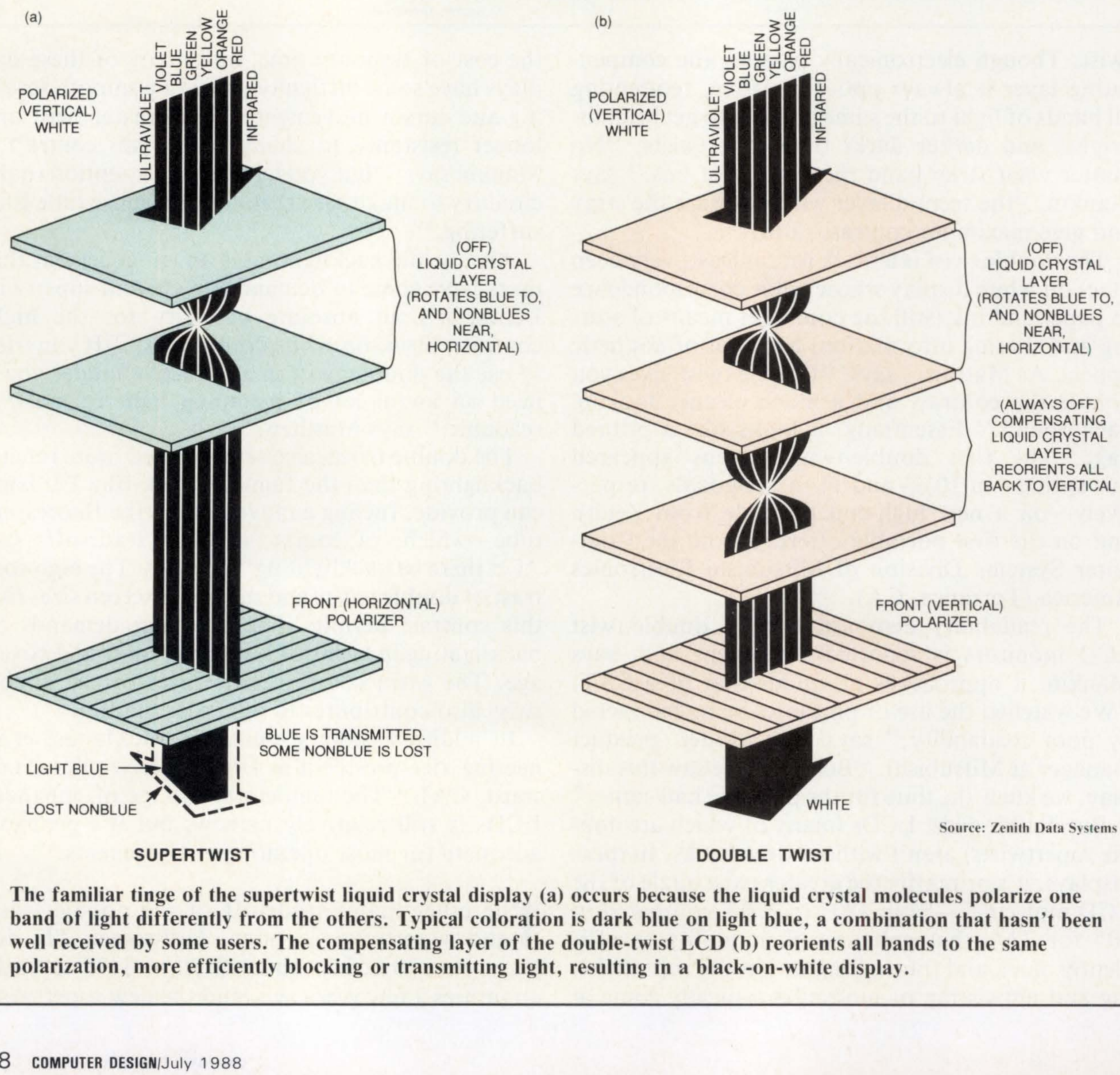
In addition, points out Colin McManus, engineering vice-president at Digital Electronics (Hayward, CA), "The temperature range of enhanced LCDs is still relatively narrow, but it's probably adequate for most operating environments."

The other major trade-off of the double twists and supertwists is price. Full-screen TN displays were priced at about $150 to $175 in OEM quantities a few years ago, and the new supertwists were then projected to cost about 5 to 10 percent more. Yet, even after several years down the learning curve, the actual price for the supertwists is in the $200 to $300 range. Reportedly, the LCD manufacturers liberally quoted forward pricing that they based on high-yield expectations for the supertwist, underestimating the difficulty in achieving the much more precise manufacturing tolerances of the newer displays.

Double twists are expected to cost about $400—even without the manufacturability and yield of the displays yet established. And prices for EL and plasma displays are descending from the $800 to $1,000 heights into the $400 to $600 range. So the familiar low-cost LCD vs. high-cost EL/plasma comparison is eroding.

Another variable that plays into the display pricing story is the fact that the majority of LCD manufacturers are Japanese. Those in high-volume production are seeing good economies of scale, and they've been rigorous in reducing production costs—by using denser driver chips, for example, and by implementing chip-on-flex or chip-on-glass driver mounting and so forth. But the greatly changed yen/dollar ratio has washed out much of the gain. Add to this dramatic price reductions in TFEL, and, says Mankin, "While TFEL used to cost three times what LCD cost, it has become more like a 50 percent premium."

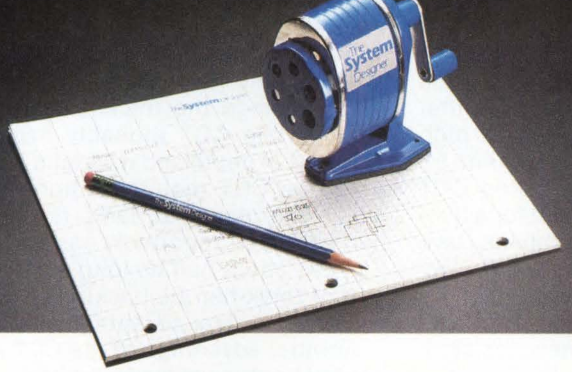
The differential in power between TFEL and LCD has also changed dramatically within a relatively short time. The major TFEL manufacturers—Sharp, Planar Systems (Beaverton, OR)

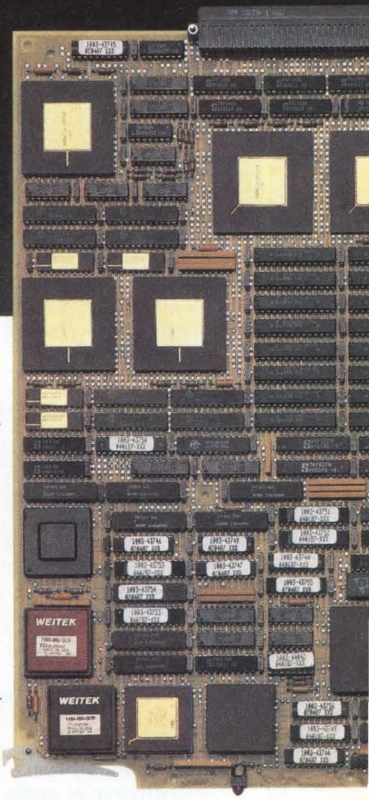


Source: Zenith Data Systems

The familiar tinge of the supertwist liquid crystal display (a) occurs because the liquid crystal molecules polarize one band of light differently from the others. Typical coloration is dark blue on light blue, a combination that hasn't been well received by some users. The compensating layer of the double-twist LCD (b) reorients all bands to the same polarization, more efficiently blocking or transmitting light, resulting in a black-on-white display.

This year, you'll hear a lot of claims that "systems" design automation has arrived.





This 32-bit processor board was designed and simulated on Mentor Graphics workstations by Sequent Computer Systems for its multi-processor Symmetry computer system. It contains over 175 IC components including 80386 processors, a 14,000-gate standard cell and two 10,000-gate arrays.

At Mentor Graphics, we know better. And so do our customers.

They preach. We practice.

Skeptical about "systems" electronic design automation?

You should be. Because in many cases, it's a triumph of form over content. In the end, there's only one practical yardstick for evaluating a systems design solution. And that's how many successful products it has produced.

Apply this measure and the field narrows dramatically. Essentially, down to a single vendor.

Mentor Graphics.

For over five years, our customers have been turning out sophisticated board products with our EDA tool set.

Test their claims.

Here are some interesting (and essential) questions that you should ask any potential EDA vendor:

Does your tool set have a common database and user interface? Does it extend from design definition through to PCB layout and output to manufacturing?

Do you have more ASIC libraries supported on your workstation than any other EDA vendor? Can you include ASICs in board simulations?

Are your tools capable of managing over 1000-page product documentation projects from start to finish?

Have you integrated mechanical packaging and analysis into the electronic design and layout process?

Anything less than a perfect score is a total loss. And a perfect score does not mean just a check in every box. Each item must be backed with the production-proven performance only Mentor Graphics can provide.

Experience makes the difference.

When we speak about systems design automation, we speak from experience. We have the largest customer base in the electronic design automation industry. And with good reason. Over 70% are repeat customers who've realized genuine value added from our products and seek to expand their competitive advantage.

It's all part of a vision unique to Mentor Graphics, the leader in electronic design automation. Let us show you where this vision can take you.

Call us toll-free for an overview brochure and the number of your nearest sales office.

Phone 1-800-547-7390. (In Oregon, call 284-7357).

Mentor Graphics®

CIRCLE NO. 36

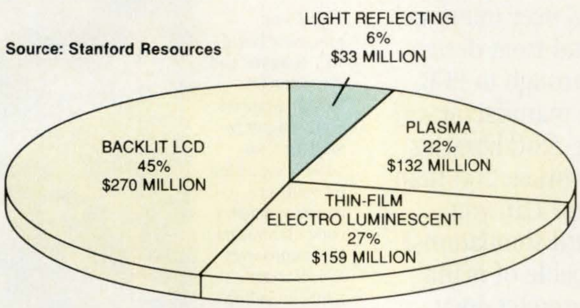
Your ideas. Our experience.

Let there be backlighting

While the flat-panel display design decision used to be one between light-emitting (plasma and thin-film electroluminescent) and light-reflecting (liquid crystal) displays, user demand for LCDs with backlighting has, in one sense, eliminated the distinction. "There's been a tremendous movement toward backlighting in the last couple of years," says Jim Aden, vice-president of the Electron Tube Division of Hitachi America (Schaumburg, IL), "from the smallest LCDs that can use LEDs or incandescent backlighting to high information content LCDs using a thick-film EL lamp or a CCT." What's commonly called CCT (cold cathode tube) is "just a fancy name for a fluorescent tube without a heater in it," explains Dave Matthews, national sales manager at Sharp Electronics (Mahwah, NJ).

Now that backlighting has become more or less a necessity, designers are left with a new decision:

Source: Stanford Resources



1990
HIGH INFORMATION CONTENT DISPLAYS
$594 MILLION

The acquired taste for brightness, a prerequisite for effective gray scale and color, is expected to reduce light-reflecting liquid crystal displays to only 6 percent of the high information content display market by 1990.

how to backlight the LCD they've chosen. The EL vs. CCT backlight decision is one fraught with trade-offs. While the CCT backlight has a slight edge in power, the EL backlight has the edge in price. The CCT is brighter and far more efficient (in lumens/W) than EL, delivering more white light for equivalent power.

But, cautions John Eng, LCD product manager at Panasonic (Secaucus, NJ), "EL doesn't appreciably change the thickness of a standard LCD panel, while CCT probably needs an additional half-inch in depth and it weighs a good deal more." Also, the CCT requires a light-diffusing system, which the planar EL lamp doesn't. On the other hand, the CCT reportedly has a 20,000-hr life, while EL lives about half as long. Until the next generation of thick-film EL backlights show up, the CCT will enjoy a clear advantage.

Another advantage of the CCT is that users can control brightness levels, while EL "can't be properly dimmed to user specification," says Aden. An EL backlight can be turned off, however, and the LCD can be operated in reflective mode, giving the user the option of extended battery operation when sufficient ambient light is available. "You could shut a CCT off, but you wouldn't be able to see a double-twist display," says Matthews. "It would be possible to put a transflector in front of the CCT and use the display with the backlight on or off, but this set-up would diminish the available light when the CCT's on, so nobody's really doing that."

Brightness is more than an aesthetic necessity these days; whether for LCD, TFEL or plasma displays, it's the path to success in future portables. "No-compromise" portables that deliver desktop performance need gray scale, and future portable workstations will need color. Brightness is a prerequisite for the effective implementation of both.

---

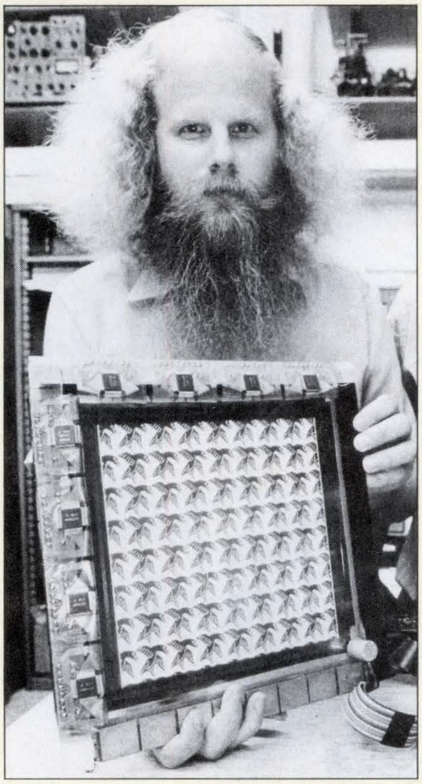
and Finlux (Cupertino, CA)—have replaced their early asymmetric drive schemes with LCD-like symmetric drive schemes using newly developed driver ICs from such companies as Texas Instruments (Dallas, TX), Siliconix (Santa Clara, CA), Supertex (Sunnyvale, CA) and Sprague Electric (Worcester, MA).

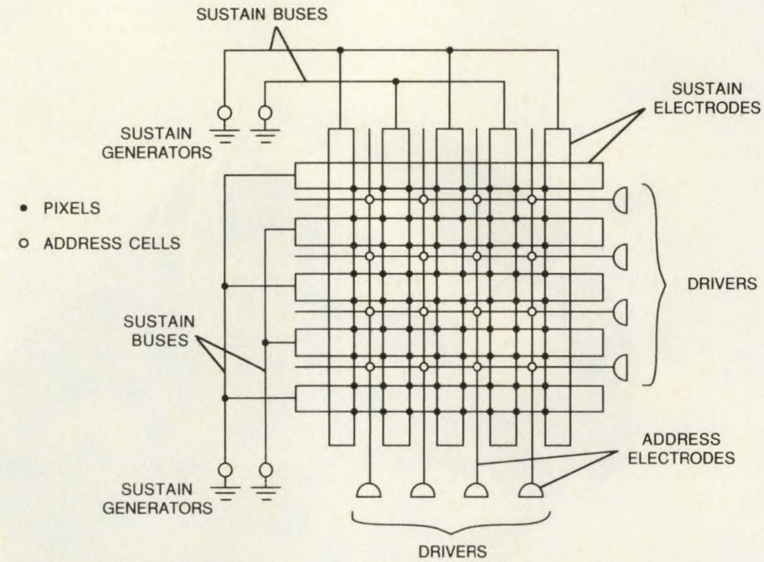
Symmetric drive permits the use of lower-voltage column drivers. In addition to being expensive, "high-voltage column drivers waste most of the power in the display," says McManus of Digital Electronics. "And since wasted power varies as the square of the voltage, you can get the same brightness level with a great deal less power if you balance the charges."

The symmetric drive technique was initially implemented to solve a problem TFEL had with retained images, according to Rolland Von Stroh, vice-president of marketing at Planar. If the image of a menu or command line, for example, was maintained on-screen for long periods of time, it was likely to become a permanent fixture. Besides solving this problem, symmetric drive provides an important side benefit: lower power demand, and hence lower subsystem and overall system cost.

This side benefit is important because the bane of the light-emitting displays has been their need for high-voltage and/or high-current drivers—both are high-cost parts that are also relatively power-inefficient. Though driver density continues to increase and per-line cost continues to decline, the drivers still represent the major price and power dilemma of the light-emitting displays. As Von Stroh explains, "It takes just 2 W to light a half-page TFEL panel; the rest of the power that's required is due to the inefficiency of stepping voltages and moving signals around."

All in all, with new drivers, drive schemes and





The ac plasma display, invented at the University of Illinois in 1964, got a boost a few years ago when associate research professor Larry Weber (left) and colleagues at the facility developed a low-power plasma display structure requiring half the typical number of drivers. This reduction in drivers is achieved by dividing address and sustain functions between separate address and sustain electrodes. The technology is being commercialized by Plasmaco, a new company founded by Weber and three former employees of IBM's defunct plasma display operation.

other incremental improvements, the power to run a TFEL panel has dropped as much as 40 percent from two years ago—from about 25 W maximum to about 15 W maximum. All of the TFEL companies and some ac plasma display manufacturers are working on energy-recovery schemes, and some of them have already implemented them. Typically, these power reclamation techniques, implemented with an extremely simple inductive circuit, take the power that was formerly vented to the atmosphere and recycle it to drive the display.

"There's still a lot of power lost to inefficiency in the circuitry," says Matthews, "and we can get down to under 10 W by further enhancing power-saving circuitry and with better driver, perhaps CMOS, technology. There's still a lot of room for improvement in the electronics. Everybody in TFEL pretty much uses the same types of materials; today, the black magic lies in the driver technology and power-saving circuitry."

The dc plasma display has enjoyed good success in the portable marketplace and elsewhere and—with driver advances, some chip-on-glass packaging, economies of scale, and maturity—it's been able to maintain a price advantage (though diminishing) over TFEL. Aesthetically, red-and-red dc plasma is perceived as less readable than red-and-black ac plasma or yellow-and-black TFEL, especially as far as contrast is concerned. And, as far as power is concerned, the power penalty of dc plasma is still upwards of 30 W. Moreover, unlike TFEL and ac plasma, dc plasma isn't a capacitive display technology and so isn't a candidate for energy recovery. Though the power drain of a full-screen dc plasma display is only about 12 W in typical conditions, the maximum figure is the one that determines power supply requirements, points out Planar's Von Stroh.

Schemes are afoot, however, to enhance the contrast and lower the power drain of dc plasma displays. A great deal of effort is also going into gray scale and color. Two years ago, there was no gray-scale dc plasma. Last year, Panasonic (Secaucus, NJ) introduced a four-level display; this year, a 16-level model. And hybrid plasma/phosphor displays—being developed at many companies—were demonstrated by Panasonic this year in both green and amber versions.

Unlike the dc plasma display, ac plasma hasn't had much of an effect on the portable marketplace lately. One strength of the techonology—relatively easy scaling up to very large sizes—has seemed to suit it better for fixed operation. A new company called Plasmaco (Highland, NY), however, has stated its intention to establish ac plasma as a player in the full-screen marketplace. "The aesthetic quality of the ac plasma display has always made it very desirable," says Jim Kehoe, Plasmaco president, "but customers weren't willing to pay double the price for it."

Plasmaco—founded by ac plasma guru Larry Weber, associate research professor at the Computer-Based Education Research Laboratory at the University of Illinois (Champaign-Urbana), and three former employees of IBM's defunct plasma display division—comes to the game armed with the division's manufacturing expertise, equipment and patent licenses. The company is also equipped with Weber's Independent Sustain and Address (ISA) display structure and an energy-recovery technique. The ISA scheme permits the use of lower-current drivers and requires half the number of drivers of a comparable standard display. A major appeal of the ISA structure is that it can be built "through a simple electrode mask change that doesn't require any panel manufacturing process changes," Weber says.

In a traditional ac plasma display, a single set of X-Y electrodes serves both address and sustain functions, and the sustain function has no place in pixel selection. In operation, the address voltage turns pixels on, while the sustain voltage (applied to the entire panel) maintains selected pixels in an "on" condition.

The ISA scheme separates the address and sustain functions. With ISA, each address electrode services a pair of sustain electrodes, which form the actual pixels; only the address electrodes require driver ICs. The ISA structure consists of address cells (the intersection of X-Y address electrodes) and pixels (the intersection of X-Y sustain electrodes); each address cell is charge-coupled to the four pixels that are surrounding it. The sustain electrodes in the panel are connected to sustain voltage generator circuits, which control the phase of signals to determine which of the four pixels in a group will be selected.

According to Weber, the sustain generators of the new structure can be built using inexpensive discrete circuitry, and busing the sustain voltage lets four of the circuits (two for the X axis, two for the Y) handle a plasma panel of any size.

In addition to using ISA, the Plasmaco panels will use inductive energy reclamation. "Most 512- × 512-pixel panels lose 10 W charging and discharging pixels, but we think we can get that down to 1 W," Weber says.

The current dominance of LCD, TFEL and plasma in the portable marketplace doesn't assure their dominance in days to come; too many other promising flat-panel technologies are waiting in the wings. But regardless of whether one of the three turns out to be the ultimate portable display technology of tomorrow, the maturation of these displays has changed one major decision for designers of portables. Whereas a few years ago, the primary portable display issue boiled down to the CRT vs. the flat-panel display, it has now become a matter of choosing among the flat-panel displays. **CD**

Mass-storage options rise to the challenges of size, ruggedness

Tom Williams, Western Managing Editor

Meeting the requirements of portable systems—ruggedness, small size, high capacity and low power—is especially difficult for mass-storage peripherals. Disk drives, particularly hard disk drives, are mechanically delicate and much more sensitive to shock, vibration and contamination than are many other system parts. It's not surprising that as systems become smaller, manufacturers are not only looking for ways to make traditional means of mass storage meet more rigid requirements, but are also exploring alternative, nonmechanical means of removable storage, including bubble memory and battery-backed memory cards and cartridges.

The issue of designing for portability isn't limited to laptop computers; it also extends to those systems that require mobility and are used in harsh environments. Such systems may be mounted or built into aircraft, ships or trucks, or may be dragged around a factory floor or oil field. The need for removability in harsh environments is forcing system designers to look for alternatives to Winchester and floppy drives in such situations. And, eventually, some technologies such as battery-backed memory cards, developed in response to the need for ruggedness, may even replace the mechanical floppy disk drive in office applications.

Laptop computers that use 32-bit microprocessors, such as the new Turbosport 386 from Zenith Data Systems (Glenview, IL), have storage demands that match those of desktop systems, according to Alan Kronisch, engineering projects manager for Conner Peripherals (San Jose, CA). Currently, the highest capacity hard disk in such a system is the "power miser" 40-Mbyte drive used in the Turbosport. This drive has a typical power consumption of 2 W. Jointly developed by Zenith and Conner Peripherals, it's a modified version of the Conner 432 40-Mbyte 3½-in. drive. The new drive has a modified controller that includes more CMOS parts to save power, and it uses power-management commands that partially or fully power down the drive when it's not in use.

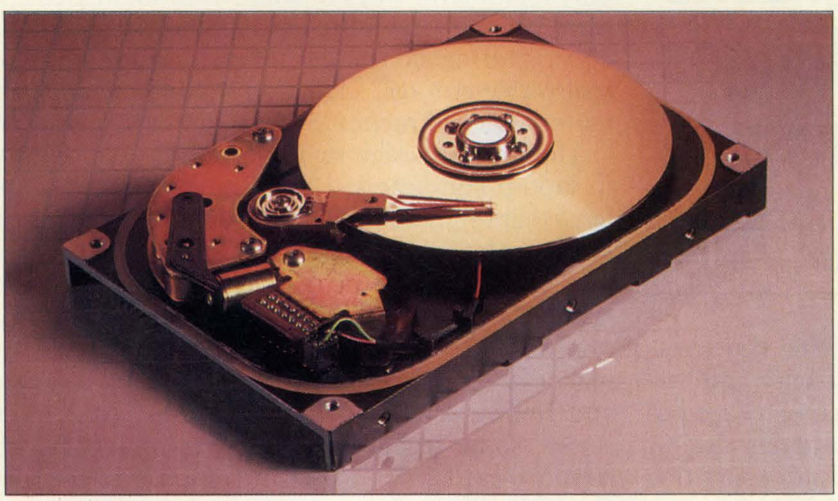
Conner is also shipping a compact, 3½-in. 20-Mbyte Winchester, the CP-3022, which incorporates a built-in interface that can be tailored to IBM's PC AT or Personal System/2, or to the small computer system interface (SCSI). When the 1-in.-high drive receives a command asking for data, it enters spin-up mode; it takes about 5 s before the disk is spinning at the right speed for data access. This spin-up mode consumes as much as 9 W of power for a short part of its spin-up cycle. The drive consumes only 2 W, however, in idle mode (that is, when the drive isn't reading, writing or seeking, but the spindle motor is running at speed).

In order to even further conserve power in battery-operated systems, drive manufacturers are coming up with programmable option modes that let the user trade system performance for battery life. The CP-3022, for example, has a standby mode, in which the drive consumes only 0.5 W. In the standby mode, the spindle motor and all electronics except the interface control are shut down. The drive will enter standby mode if it doesn't receive any commands within the time-out interval set by the user, which can be between 15 s and 18 min. The typical time chosen is about 5 min, according to Kronisch. A sleep mode, using only 0.4 W, turns the entire drive off, requiring a reset signal from the host to start up again.

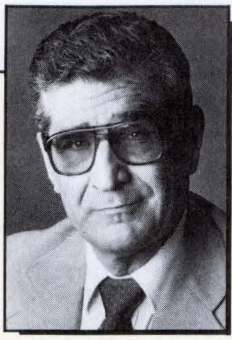
Another 20-Mbyte Winchester designed for use in laptop systems is Litedrive II from CMS Enhancements (Tustin, CA). Litedrive II uses a separate controller board with a bus interface that can be tailored to suit a variety of laptop systems. It consumes 4.58 W in idle mode and, like the Conner 3022, has a sleep mode. Stoplite, a software utility, can be used to set time-outs to shut down Litedrive II and restart it when access is required.

To best use the programmable power-saving strategies of Winchesters in battery-powered systems, users must make some intelligent choices about the needs of their applications for immediate response vs. power consumption. Since an electric motor uses a lot more current when powering up than when idling, recognizing the optimal way of handling time-outs may be beyond the grasp of the average user, thus making it a matter of mere guesswork. On the other hand, many users are capable of making the decision to shut down the hard drive altogether during an application that doesn't require the hard drive except to load the program and perhaps save the results upon completion.

While there's no viable alternative to hard disk drives in their price-per-megabyte range, there are removable—and hence portable—memory technologies that can equal or surpass the capacity and performance of floppy drives. The price for



The CP-3022 Winchester disk drive from Conner Peripherals packs 20 Mbytes into a package a mere 1 in. high, making it the thinnest drive available. It can be manufactured with a variety of interfaces, including IBM PC AT and SCSI. Power-management commands let the user optimize disk availability and power consumption.



Guido Galli
Chief Scientist
Magnesys

Bubble memory overcomes "too expensive" tag

Bubble memory has historically been viewed as the most reliable nonvolatile memory available. Because it's a solid-state memory, no moving parts are required for operation. In addition, it offers unlimited read/write cycles and requires no batteries to maintain data. But there have been arguments against the use of bubble memory, especially concerning its cost and its ability to operate over wide temperature ranges.

Although the problem of having a too-narrow temperature range appears to be a technical one, the solution has been one of both technology and cost. Through design improvements in its bubble-memory components, Magnesys (Santa Clara, CA) has manufactured bubble-memory dies that operate in an uncompensated mode in −40° to +85° C temperature ranges. Further efforts, however, were required before this basic technology development could be commercialized.

Many manufacturers of bubble-memory devices have been unable to provide uncompensated products with such wide operating temperature ranges because manufacturing processes limit their ability to both test and sort individual dies in the early stages of component manufacture. These manufacturers have paid the high cost of gadolinium gallium garnet (GGG) wafers ($350 to $400 for a 4-in. wafer) required to produce bubble memory, only to scrap a large portion of materials due to low yields. This initial high cost of the GGG wafer and the high scrap rates have caused bubble-memory prices to remain higher than those of competitive silicon devices.

In order to reduce costs, manufacturers of bubble memory must be able to fully test each individual die before it's cut out of the wafer. If they don't, they add significant cost to the dies by performing packaging steps before even minimal functionality can be tested. As a result, a single bad die in a multiple-die package can result in the loss of good dies. This has led to an increase in component cost for multiple-die packaging as well as an increase in system cost through the use of multiple single-die packages. Using individually packaged 1-Mbit devices to manufacture a 1-Mbyte system, for example, requires eight complete, packaged components, a number that can be cut in half or less by using multiple-die packages.

The packaging cost for bubble memory includes the integration of permanent magnets as well as materials that are more expensive than other semiconductor products. These secondary costs add more to the already high basic cost of bubble memory. But by testing and matching multiple dies at the wafer level, Magnesys has been able to significantly reduce the raw production cost of bubble-memory components. Dies can be sorted so that product pricing can be related to the yield of devices with various temperature ranges.

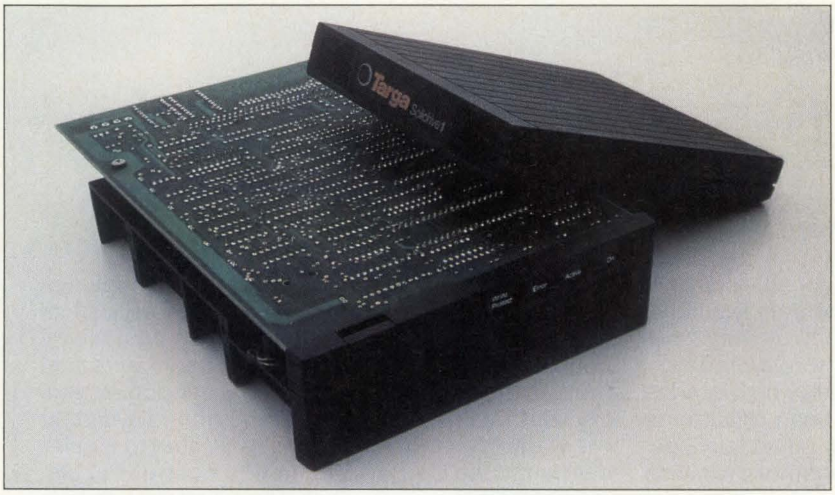
The highest die yields are in devices with a constrained operating temperature in the 0° to 50° C "standard" range. These are also the least expensive. A lower yield of dies operating over a 0° to 70° C "industrial" range is available. And there's an even lower yield of dies operating in the −20° to 70° C "extended" range. The lowest yield of dies operates over the −40° to 85° C "severe" range and usually is required only by military customers that are operating in extremely severe environments. Severe-temperature devices are, of course, the most expensive.

The lower production cost as well as the sorting at the wafer level have made bubble memory price-competitive with other nonvolatile semiconductor technologies such as battery-backed static RAM. Industry pricing, for example, for 720 kbytes of battery-backed SRAM integrated into a PC card ranges from $500 to $900, depending on the power requirements of the components used. Because of the operational limitations of batteries over temperature, battery-backed SRAM is an effective nonvolatile memory choice only over the 0° to 50° C temperature range. Because of Magnesys' sorting and testing process, the company is able to offer an equivalent-capacity, PC-based product for a single-quantity price of $713, declining to under $500 in volume.

At the other extreme of temperatures, −40° to 85° C, these manufacturing techniques have allowed equivalent levels of price competitiveness. Alternative technologies such as severe-temperature EEPROM and low-capacity militarized disks are available at prices of around $8,000/Mbyte, while bubble memory from Magnesys is competitively priced at under $5,000/Mbyte or less at capacities of 5 to 10 Mbytes.

such memories is higher than that of floppy drives, but it's offset by the needed high data reliability under hostile environmental conditions.

One such technology possibly making a comeback is bubble memory. One reason bubble memory failed to catch on when it was first introduced was that the bubble-memory ICs were very difficult to integrate into a working memory subsystem, re-



The Targa FD4500A nonvolatile cartridge RAM drives are electronically compatible with half-height, 5¼-in. floppy drives and controllers. Cartridges with capacities of 360 and 720 kbytes are available. The drive can be used with an existing floppy controller in the system, and the system can boot from the cartridge drive just like from a floppy drive.

quiring both digital and analog engineering expertise. Very few customers had the resources to effectively use the chips as delivered by the semiconductor manufacturers, and the semiconductor companies didn't see themselves in the role of selling board-level products. Today's bubble-memory suppliers either buy the bubble-memory chips from semiconductor manufacturers or fabricate them themselves. And they do the integration work, offering system designers either plug-and-play or custom-designed memory subsystems.

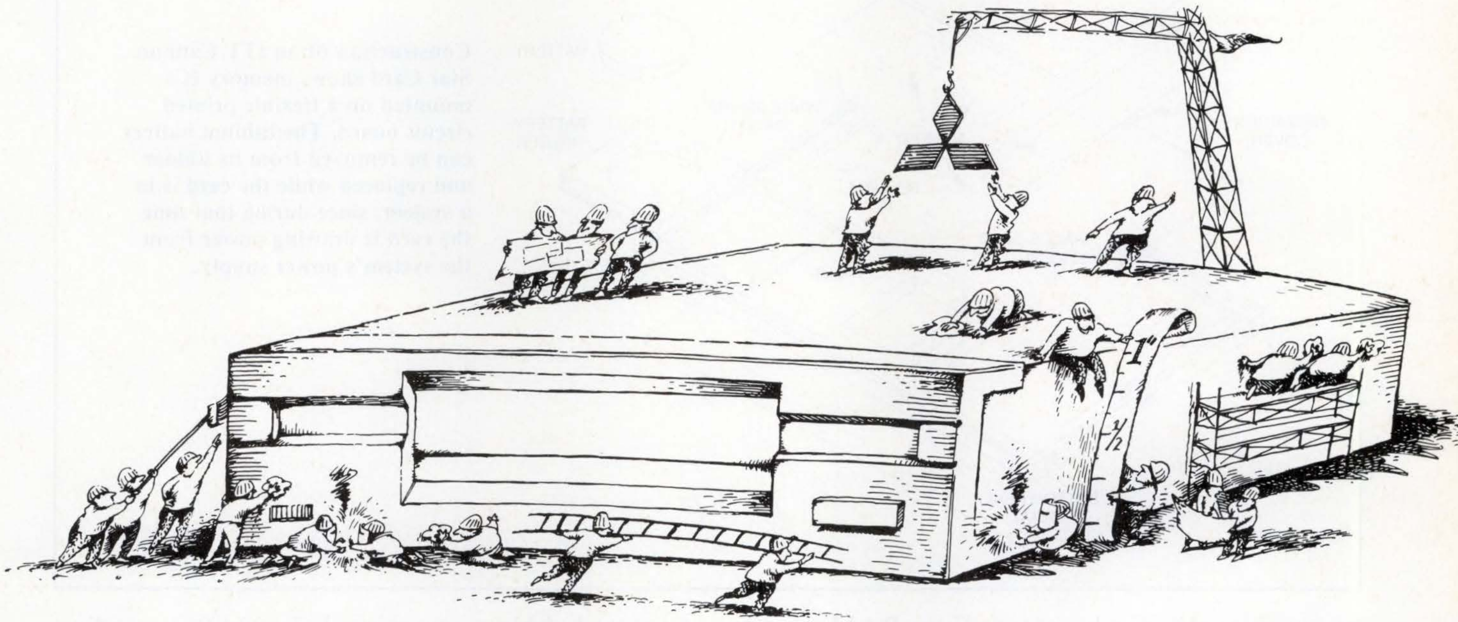
Magnesys (Santa Clara, CA) manufactures both the bubble-memory dies and the storage subsystems that let system integrators easily incorporate bubble storage into their designs. In addition, Magnesys produces custom bubble-based storage subsystems. According to Bill Morrison, vice-president of sales and marketing at Magnesys, bubble memory is focused primarily on factory-automation, military and telecommunications applications that have two main requirements: surviving extreme environments and providing the highest reliability.

Since bubble memories—whether located in removable cartridges or sealed inside systems—have no mechanical parts, they can be protected from dirt and moisture. The major environmental concern, therefore, is temperature. Magnesys provides four temperature ranges, from the standard 0° to 50° C range to the severe −40° to 85° C military specification. Temperature is directly related to bubble cost, according to Morrison. The wider the required temperature range, the smaller the yield becomes because only a relatively small percentage of dies on any given wafer can operate under the harsher temperature requirements. And as the yield decreases, costs increase.

Another consideration regarding bubble memory is security. Government security agencies, according to Morrison, require many random overwrites of magnetic disk media before the stored data can

Melcard memory cards from Mitsubishi can store up to 512 kbytes of static RAM, one-time programmable ROM or masked ROM. Cards and connectors are available with 8- or 16-bit-wide data paths and with two styles of connector: pin or shielded edge connector. One system that uses the Melcards is a lottery terminal made by International Totalizer Systems. Data entered at a local store can be removed by means of the Melcards and taken to a central processing facility for each lottery drawing.

Introducing The Only 1″ High Microfloppy Disk Drive Big Enough To Be A Mitsubishi.



At just 1″ high, our new MF353C and MF355C 3½″ microfloppy drives are designed to give your system a giant edge in performance and reliability.

Developed by Mitsubishi—a $13 billion dollar corporation with resources worldwide—the MF353C and MF355C integrate easily into today's small, lightweight PC designs.

When it comes to features, our microfloppies offer sizable advantages.

Unformatted memory is an impressive 1.0MB on the MF353C; 2.0MB on the MF355C. HCMOS-based LSI architecture with fewer parts and single 5V power requirements reduce power consumption while providing unsurpassed dependability and longer product life. Another big advantage from Mitsubishi: The MF355C is downwardly compatible with the MF353C.

A complete family of floppies.

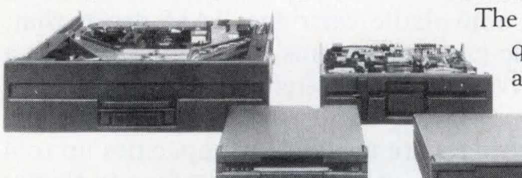
Whether 3½″, 5¼″ or 8″ form factor, Mitsubishi has just the floppy drive you need and available in quantity. Representing over two decades of design and manufacturing expertise, each Mitsubishi drive is vertically integrated to include our own ICs, read-write heads, motors, and other critical components.

It all comes down to quality.

The result is unparalleled Mitsubishi quality from top to bottom, inside and out. A reputation for product innovation, proven performance and reliable, on-time delivery has made Mitsubishi the supplier of choice among the biggest OEMs in the business.

Model No.	Size	Height	Memory Capacity (Unformatted)	Power Requirements
MF353B	3½″	1.26″	1MB	+5V and +12V
MF355B	3½″	1.26″	1MB/2MB	+5V and +12V
MF353C	3½″	1″	1MB	+5V
MF355C	3½″	1″	1MB/2MB	+5V
MF501B	5¼″	1.61″	0.5MB	+5V and +12V
MF504B	5¼″	1.61″	0.5MB/1MB/1.6MB	+5V and +12V
M2896	8″	2.25″	1.6MB	+5V and +24V

For complete information on how our floppy family can make a big difference in your PC designs, contact Mitsubishi Electronics America, Inc., Computer Peripherals Division, 991 Knox Street, Torrance, CA 90502. Telephone: (213) 515-3993, and ask for our Peripherals Sales Department.



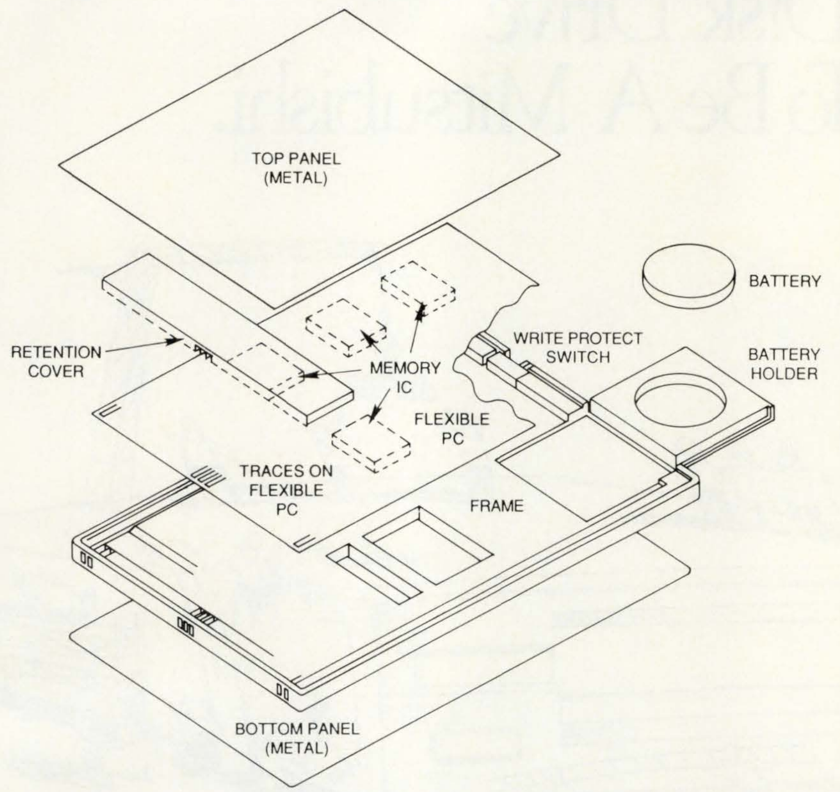
Your Reliable Resource For Reliable Disk Drives.

Mitsubishi Sales Offices

Carrollton, TX (214) 241-5300 • Piscataway, NJ (201) 981-1001
Minnetonka, MN (612) 938-7779 • Mt. Prospect, IL (312) 298-9223
Norcross, GA (404) 662-0758 • Sunnyvale, CA (408) 730-5900
Torrance, CA (213) 515-3993 • Woburn, MA (617) 938-1220

MITSUBISHI ELECTRONICS

CIRCLE NO. 38



Construction of an ITT Cannon Star Card shows memory ICs mounted on a flexible printed circuit board. The lithium battery can be removed from its holder and replaced while the card is in a system, since during that time the card is drawing power from the system's power supply.

be considered securely erased. Even RAM must be overwritten at least 100 times. By contrast, bubble memory can be totally erased with no residual hysteresis by either pulsing a special internal erase coil, passing the memory through the poles of a permanent magnet or overwriting the data one time.

Magnesys' standard bubble storage products are 5¼- and 3½-in. drive replacements that contain the control and interface electronics—primarily the SCSI electronics. Removable bubble cartridges are available in three capacities: 360 kbytes, 720 kbytes and 1.2 Mbytes. They thus correspond to the capacities common to DOS-based computers—capacities requested by customers who wish to put data from cartridges brought in from the field onto floppies for use in office environments. Bubble cartridges with other capacities can be configured based on various combinations of the 4-Mbit chip technology now available and can be used to configure custom storage capacities.

The future of bubble memory, according to Morrison, is much brighter than it was only a couple of years ago, since manufacturers can offer off-the-shelf solutions in addition to custom-engineered systems. But the ultimate goal is to develop vertical Bloch line bubble recording. Bloch lines are regions of transition between areas of different magnetic polarity that exist in the wall between those regions. Current bubble memory reads 1s and 0s according to the different magnetic orientation of bubble regions. By reading values in the walls between the regions, bubbles can be recognized that are 10 times smaller than those used today. Morrison believes that 64-Mbit devices appear to be feasible and 1-Gbit chip-level devices are theoretically possible.

The low power consumption of CMOS and the existence of long-life lithium batteries are combining with increasing cell density and surface-mount technology to produce easily transportable, inexpensive memory modules. Such memory modules come in two basic configurations: preintegrated units with standard interfaces and credit-card-sized devices with connector pins. The card-sized devices require the system designer to implement the actual interface electronics and protocol.

Targa Electronics Systems (Ottowa, Ontario) produces nonvolatile cartridge RAM drives that, like bubble-memory systems, behave the same as a floppy drive or a Winchester via SCSI, RS-232 or parallel interfaces. Battery-backed CMOS static RAM cartridges are available in capacities up to 4 Mbytes. For drive models that interface to floppy disk controllers and act like floppy drives, cartridge capacities come in 360-kbyte, 720-kbyte, 1.2-Mbyte and 1.44-Mbyte sizes.

Battery-backed SRAM cartridges can represent a cost savings over bubble memory as well as provide a high degree of reliability, nonvolatility and immunity to dirt. They're vulnerable, though, in temperature extremes. Due to the battery's characteristics, most of these cartridges can operate between 0 ° and 70 ° C. When temperatures rise above or fall below this range, the amount of current available from the battery drops radically and the cartridge no longer holds data reliably. If this is a possibility, a more expensive, yet more temperature-insensitive, bubble memory may be the answer.

A more compact form of battery-backed memory is the credit-card-sized memory card. Memory cards are modules containing SRAM chips, control circuitry and a long-life (up to 10 years) lithium battery. They have the potential to profoundly affect the design of future systems. Unlike battery-backed SRAM cartridges, memory cards contain pin-outs for data, address and control signals, but they aren't sold as disk replacements. However, they're often used as disk replacements in combination with electronics that emulate a drive. Because memory cards can connect directly to the main memory bus of a microprocessor system, they have potential for system applications beyond peripherals.

The Melcard from Mitsubishi Electronics (Tokyo, Japan) is available not only with battery-backed SRAMs, but also with up to 512 kbytes of one-time programmable ROM or with mask-programmed ROM. The Star Card from ITT Cannon (Santa Ana, CA) also offers the above three options, as well as EPROM and EEPROM versions. Both cards use lithium batteries that can preserve data for up to 10 years. These batteries can be changed while the card is plugged into a powered-up system, with the card drawing power from the system.

The availability of ROMs, EPROMs and SRAMs with high-capacity memory cards makes the cards useful for such applications as medical monitoring equipment that can be worn by outpatients. "As electronics get smaller, people can wear the equipment as outpatients rather than be cared for by members of a hospital staff," says Terry Johnston, Melcard product marketing manager for Mitsubishi. Much of this equipment—such as a unit used to monitor medication flow—must be tuned to a particular patient, and the parameters derived from tests and diagnosis can be stored on a memory card and worn with the unit.

Many memory cards are starting to be used as personality modules to characterize equipment for special functions, to store printer fonts, or simply to expand main memory in a personal computer.

With laptop computers beginning to sport hard disk drives with 20- and 40-Mbyte capacities and beyond, questions of backing up the data will be as important for portables as for desktop systems. Installing a tape drive for occasional backup doesn't seem practical, however, when considering its bulk and power consumption. Mountain Computer (Scotts Valley, CA), therefore, recently introduced a QIC-compatible tape drive, the TD4000, that's available in either 3½- or 5¼-in. form factors. It attaches as an external unit to NEC or Toshiba laptops via proprietary cabling for backup operations. For a number of other laptops, there's cabling and software available to let the TD-4000 back up and restore files by plugging into the laptop's external floppy drive interface.

Even storage devices that are considered massive by most standards in terms of the amount of data they can store are beginning to be tailored for portability. The Integra III storage subsystem by Pacstor (Los Gatos, CA) provides up to 1 Gbyte of fault-tolerant data storage in a suitcase-sized cabinet that contains up to twelve 100-Mbyte 3½-in. Winchester drives. The Integra III can act as a shared storage resource for up to 16 host computers or can be used as the main storage for a network file server. An added degree of portability and security is provided to the unit through a fold-up handle and wheels, which allow it to be easily moved and perhaps locked in a vault at night.

While truly massive data storage still requires disk drives that are mechanically sensitive, even the venerable Winchester appears to be rising to the challenge of portability. Beyond that, the outlook for bubble memories to surpass disk storage in capacity and reliability is bright. And a vast field of applications seems to be opening up for high-density, compact and inexpensive memory cards. These new options will make portability achievable even in equipment and applications where a few years ago it might never have seemed possible. **CD**

Power supplies shed weight and size for portability

Richard Goering, Senior Editor

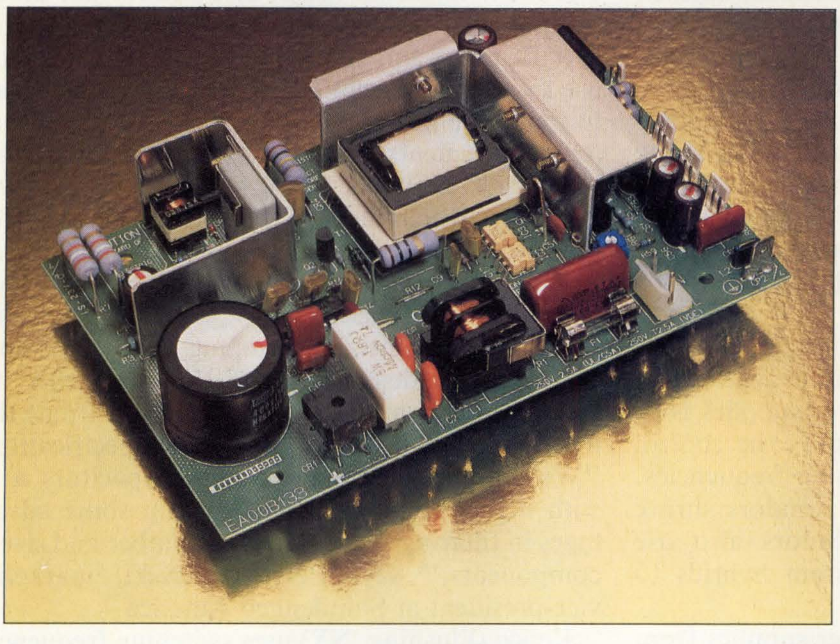
Selecting a power supply is a major concern for designers of portable computer-based systems. When portability is required, power supplies must be as lightweight and compact as possible—and be efficient and reliable. Often, however, the ac-to-dc power supply is the single bulkiest item in a piece of equipment.

The first decision engineers must make when selecting a power supply is whether to build or to buy. Although most power supplies today are built in-house, an increasing proportion are being built by outside vendors. If engineers choose to work with a power-supply vendor, they must then decide whether to select custom power supplies or off-the-shelf models. Today's merchant power-supply business is predominantly custom.

The type of power supply to choose is another important issue. While switching power supplies offer the most efficient ac-to-dc conversion and are widely used for computer-based systems, linear power supplies are more rugged and can be more cost-effective in extremely low power applications. The location of the power supply must also be taken into consideration. Some portable equipment, for example, uses external power supplies that plug into a wall or sit on a desk.

Battery-powered systems don't need a conventional power supply and generally use dc-to-dc converters to provide regulated dc voltage to the system. They may also use external power supplies that can run the system under ac power. High-performance battery-powered systems, such as the new Turbosport 386 laptop computer from Zenith Data Systems (Glenview, IL), require a very sophisticated power-management system that can conserve battery life.

The willingness of an increasing number of vendors to work closely with clients to customize power supplies has influenced some manufacturers to buy power supplies rather than build their own. Tektronix (Beaverton, OR), for example, has tradition-



Switching power supplies are becoming compact enough for many portable applications. This Kepco/TDK triple-output 35-W supply is $3.93 \times 6.3 \times 1.18$ in. and weighs 12.3 oz. A switching frequency of 100 kHz helps reduce the size.

ally designed the power supplies for its logic analyzers—but the company recently purchased outside power supplies for two new models. "We'll bend a long way to use an OEM power supply rather than build our own. We're finding that power-supply vendors are becoming more willing to work with us on a custom basis," says David Bennett, engineering project manager for the Tektronix DAS 9200 logic analyzer.

Engineers at Hewlett-Packard (Palo Alto, CA), in contrast, designed their own power supply for the new HP 437B microwave power meter. HP needed a 4-W linear power supply with ±5-V and 15-V outputs and was unable to find one on the off-the-shelf market.

Of course, the least expensive route is to find an off-the-shelf model. An industry ideal for off-the-shelf switching power supplies is 50 cents/W in the 100-W range. Although that goal is rarely attained, some power supplies above 50 W can be purchased in volume for less than $1/W. The price per watt increases sharply as the power decreases.

Along with low cost, another advantage of working with outside power-supply vendors is that they are familiar with regulatory agency requirements. The strictest safety requirements are set by the VDE (Verband Deutscher Electrotechniker) and the IEC (International Electrotechnical Commission). These standards require a 3750-V_{ac} withstand voltage between inputs and outputs, an 8-mm spacing between primary and secondary circuitry, and a 3-mm creepage between live parts and dead metal. Much stricter than the U.S. requirements set by Underwriters Laboratories, VDE and IEC compliance is essential for any product sold in Europe.

The electromagnetic interference standards set by both VDE and the U.S. Federal Communications Commission also require consideration. Class A limits cover frequencies above 150 kHz, while class B limits extend down to 10 kHz. Extra filtering is generally required to meet class B limits.

Once designers determine where they will obtain their power supply, they must select a type of power supply. In a linear power supply, ac power is converted to an unregulated dc voltage and then linearly regulated with power semiconductors. Switching (or switch-mode) power supplies use a high-speed switching element to regulate voltage through pulse-width modulation.

Switching power supplies are more lightweight, compact and efficient than linear power supplies—and generally cheaper in the medium power ranges. A switcher typically weighs one-quarter of a comparable linear and occupies one-third the space. While a linear power supply is about 40 percent efficient in terms of input-to-output power, switchers can achieve 70 percent efficiency.

Although it might appear that switchers are the obvious choice for portable systems, linears offer better line and load regulation, generate less noise, and are more resistant to shock and vibration. "If weight isn't a concern, linears are wonderful for portable equipment because they're so hardy," says Steve Cole, vice-president of marketing at Power-One (Camarillo, CA).

For extremely low power applications, such as those under 25 W, the size and weight of a linear isn't a major concern. Computer Products (Pompano Beach, FL), for example, offers its PM500 series of 1- to 10-W linear power supplies in board-mountable, 2.5- × 3.5- × 1.62-in. cases. Also, many of the external power supplies that plug into wall sockets are linear power supplies. Since switchers generally cost more in low-power ranges, linears are usually the choice for small portable systems.

Portable systems demand compact power supplies, and vendors are working to provide them. One way to shrink switching power supplies is to use power MOSFETs, which simplify the control circuitry and permit higher switching frequencies. A higher frequency, in turn, lets vendors shrink transformers and capacitors. Vendors also use surface-mount technology or custom hybrids to reduce component count.

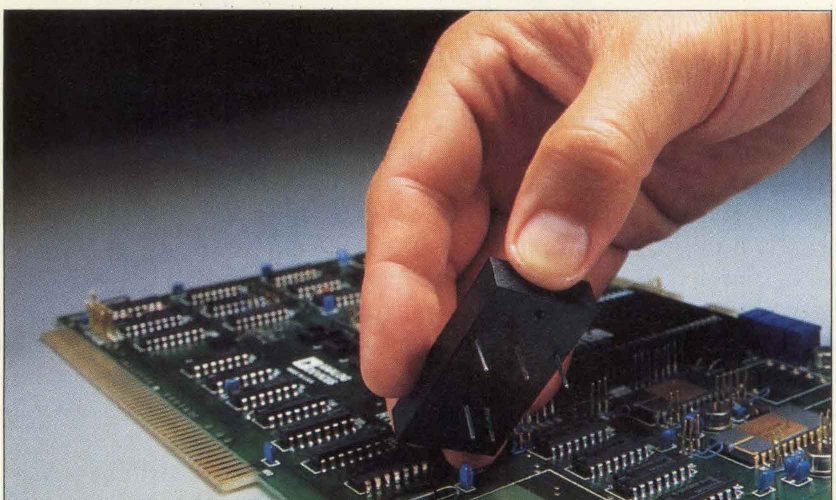
The LS series of switching power supplies from Lambda Electronics (Melville, NY), for example, includes single-output models from 10 to 150 W and triple-output models from 50 to 100 W. Power densities reach 2.2 W/cubic in., and prices go down to 86 cents/W. A 10-W single-output model weighs just 0.46 lb and measures 2.91 × 2.83 × 1.22 in. A 50-W triple-output model weighs 0.93 lb and is sized at 6.10 × 3.74 × 1.42 in.

Lambda achieves these size reductions through a combination of switching frequencies between 70 and 130 kHz, power MOSFETs and surface-mount technology. The LS series doesn't meet VDE safety specifications and is intended for North American use only. "To meet VDE specifications, you have to make the power supply larger because of spacing requirements," says Ron Koslow, marketing manager. Lambda's new LF series of low-power switchers, which meets VDE specifications, offers power densities of about 1 W/cubic in.

Shindengen America (Westlake Village, CA) and RTE Powermate (San Diego, CA) are among the manufacturers pushing switching frequencies up to 200 kHz. Shindengen's GY/G 50-W switcher, for example, occupies a 7.6- × 3.8- × 1.9-in. frame that meets full VDE safety and EMI specifications. "We don't reduce magnetics or capacitors a lot with higher frequency, but we gain some advantages in filtering and reduce the number and size of components," says Peter Gajewski, marketing vice-president at Shindengen America.

Kepco (Flushing, NY) uses switching frequencies as high as 300 kHz in its miniaturized Kepco/TDK line of switching modules. The 10-W dual-output FCP model, for example, comes in a 2.17- × 3.15- × 0.75-in. case and weighs 3.53 oz. Such packaging isn't cheap, however—the unit price is $47. A new addition to the Kepco/TDK line, the MRW 150KV 35-W power supply, uses a 100-kHz switching frequency and keeps component height to 1 in. above the printed circuit card.

Higher switching frequencies aren't an instant



A 4.5-W dc-to-dc converter from Computer Products occupies just 1 × 2 × 0.375 in. on a printed circuit board. Dc-to-dc converters are frequently used to supply regulated voltages to battery-powered systems.

Intelligent power management enhances battery-powered laptop

When Zenith Data Systems (Glenview, IL) designed its latest series of battery-powered laptop computers, the company did far more than just look for an efficient battery. Rather, it designed the entire system to operate on minimal power and implemented a sophisticated power-management system to conserve battery life.

Introduced in April, the 80386-based Turbosport 386 and the 80286-based Supersport 286 rival the performance of desktop IBM PC compatibles. Claimed to be the fastest portable ever built, the Turbosport 386 features 12-MHz no-wait-state operation, a high-contrast LCD display and the industry's first battery-operated 40-Mbyte hard disk drive. The Supersport 286 includes a 20- to 40-Mbyte drive and a display similar to that used in previous Zenith laptops.

To conserve power, Zenith used a high level of CMOS integration in the display, memory, CPU and disk drive. Because CMOS consumes power in transition states, the no-wait-state requirement was an important design consideration. "The slower you run CMOS, the better the power characteristics," says Kevin Mankin, product development manager for Zenith computer systems. "Wait states rob you of performance and battery life."

The power requirements of subsystem components are extremely low. Zenith's Page White LCD display, which features a contrast ratio of 20:1 and a 640-×400-line resolution, draws just 4 W. The 40-Mbyte hard disk drive consumes 2.5 W—less power than a nightlight.

When the system is powered up, users can select power allocations to the peripheral ports, display, modem and hard disk. The system also automatically allocates power under microprocessor control. The hard disk drive, for example, has four power levels. To start up the drive, a very short pulse of 8 W is given for less than 1 s. When the drive is spinning, it consumes 2.5 W; when it does a read or write, it consumes 3 W; and when the disk is spun down but ready to spin up, it uses a mere 0.5 W.

Zenith designed its own rechargeable nickel-cadmium batteries. "Nickel-cadmium maintains its voltage for a long time, but it drops off fast when it discharges," says Mankin. "So we have charge and discharge monitoring of the battery under microprocessor control." Fast-charge batteries are provided for the Turbosport 386, but they're not cheap—the suggested retail price is $169/pack.

A dc-to-dc conversion board routes regulated dc power to system components. External battery chargers and ac-to-dc adapters are also available with the laptops. For users on the go, Zenith even provides an automobile cigarette lighter adapter for the Supersport 286.

solution for power-supply vendors, according to Larry Slagal, sales vice-president at RTE Powermate. "As you go up in frequency, you create other problems, such as the transfer of heat to emitting surfaces," he says. "You're dealing with different noise levels and filtering problems. So you have to pay very close attention to the layout of the boards that make up the power supply."

Surface-mount technology and custom hybrids can be as effective as switching frequency in reducing size. Todd Products (Brentwood, NJ), for example, uses surface-mount technology and claims power densities up to 3.5 W/cubic in. for its SC series of 150- to 500-W switchers. Power-One's Cole says his company achieved power-supply size reductions of 40 percent by placing the control circuitry in custom hybrids.

An effective way to avoid taking up space inside a system is to use external power supplies. Available in wall plug-in or floor units, external power supplies are used with equipment such as modems, plotters, laptop computers, portable instrumentation and musical keyboards. More expensive than internal power supplies, external power supplies are typically priced around $1 to $1.50/ W.

One of the greatest advantages of an external power supply is that the actual instrument doesn't have to go through safety agency approvals. Only the power supply itself must meet UL or VDE safety standards. Another big advantage of external power supplies is that they remove heat generation from the system.

Today's external power supplies are more than just ac-to-dc adapters. Users can select unregulated linear, regulated linear or regulated switching power supplies. "Most of our applications are ac-to-dc unregulated," says Bill Dull, chief executive officer of Tamura America (Carson, CA). "If a system has to be tightly regulated, many people want to put the regulator on-board, because there's a 5- to 6-ft cord between the power supply and the equipment."

If regulated dc power is required, designers typically use linears below approximately 15 W. "Linears are larger, but at lower power levels they're more cost-effective," says Harold Myers, vice-president of marketing and sales at Elpac (Santa Ana, CA). Elpac makes unregulated linear wall-mount units from 1.5 to 8 W, and regulated linear wall-mount and desktop units from 5 to 30 W.

Ault (Minneapolis, MN) makes external linear power supplies from 1.5 to 14 W, uses a hybrid linear and switching technology in the 8- to 16-W range, and makes switching power supplies at 50 and 100 W. A 14-W linear occupies the same 3.75- × 6.50- × 2.25-in. wall-mount case as a 50-W switcher. James Electronics (Chicago, IL) offers external linear supplies up to 36 W and external switching supplies up to 60 W.

Ault also manufactures external ac-to-ac transformers and battery chargers, which are current-controlled devices that can sense the battery condition. Hayes Microcomputer Products (Norcross, GA) uses Ault's ac-to-ac transformers and provides its own ac-to-dc conversion inside its modems. Ault provides a battery charger for Zenith Data Systems laptops that also functions as a switching power supply to run the laptop off ac power.

A visible trend in portables is the move toward battery-powered systems. Although a battery removes the need for ac-to-dc power conversion, dc-to-dc converters are usually still required to provide regulated dc voltages to system components. Most dc-to-dc converters come in either board-mountable or rack-mount versions.

Dc-to-dc converters are available in a variety of power ratings and voltage outputs. International Power Devices (Brighton, MA), for example, provides standard converters from 0.5 to 120 W and builds custom converters up to 500 W. Single- and multiple-output versions are available. A 1-W, dual-output supply is housed in a 1.25- × 0.8- × 0.4-in. case, while a 100- to 120-W single-output supply occupies a 3.5- × 5.5- × 0.91-in. case.

Dc-to-dc converters can be either isolated or nonisolated. An isolated converter protects the output from the input, so that a failed converter won't send a voltage surge through the system.

Many dc-to-dc converters allow a wide voltage-input range. A series of dc-to-dc converters from Computer Products, for example, accept inputs from 20 to 60 V, while others handle input ranges of 9 to 18 V, 18 to 36 V and 36 to 72 V. "If you take a battery from peak charge to discharge, you go through quite a range," says Gene Zuch, director of marketing. Computer Products' dc-to-dc converters range from 0.5 to 100 W.

Although dc-to-dc converters are already compact, vendors are making them even smaller. International Power Devices uses a topology called current-mode control, which allows a faster transient response and reduces the number of components. Power-General (Canton, MA) used surface-mount technology to fit a 25-W converter into a 3- × 3- ×

0.375-in. package. Computer Products claims to have reduced its 4.5-W AF series of dc-to-dc converters by 50 percent to a measurement of $1 \times 2 \times$ 0.375 in. by manufacturing them on a thick-film substrate using surface-mount components.

Nickel-cadmium and lead-acid batteries, the dominant energy sources in portable computer-based systems such as laptop computers, are usually rechargeable. While lead-acid batteries are less expensive and provide higher voltages, nickel-cadmium batteries have a longer shelf life and can better withstand a deep discharge.

"There was an initial trend toward lead-acid batteries in laptops, but now it's back to nickel-cadmium," says Joe Carcone, marketing manager for Sanyo Energy (San Diego, CA). "Nickel-cadmium has a high energy density, can be stored up to five years in any state of charge and can be deeply discharged." Varta Batteries (Elmsford, NY) claims to have improved nickel-cadmium batteries as a result of its mass-plate cell technology, which lets batteries retain 60 percent of their capacity after 12 months. Varta button cells and batteries require recharging rates as low as 1 μA.

On the other hand, sealed-lead rechargeable batteries from Gates Energy Products (Gainesville, FL) boast a float (shelf) life of up to 10 years and a cycle life of anywhere between 200 and 2,000 charges and discharges. Lead-acid batteries from Panasonic (Seacaucus, NJ) boast a shelf life of eight years and can recover from a deep discharge.

As battery technology advances, and other components of computer-based systems become more compact, there will be an increasing number of portable systems that don't have to be plugged in except to recharge. The next revolution in computer design will take advantage of this portability. **CD**

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 261 *Average 262* *Low 263*

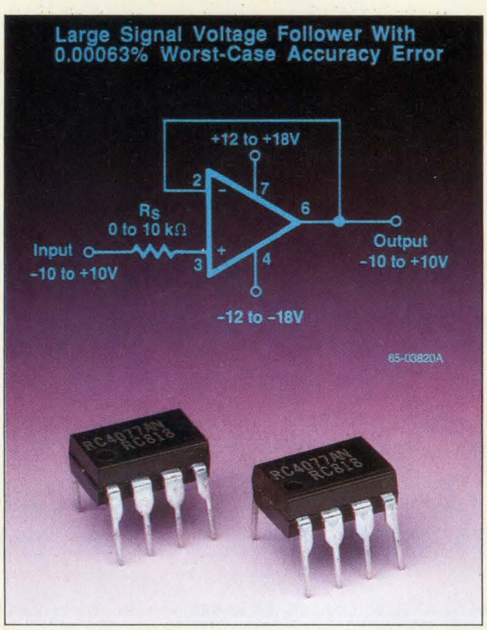
Innovative processes spawn faster, more precise monolithic op amps

PRODUCT FOCUS

Michael Donlin
Associate Editor

Ask any number of manufacturers to define the most significant advances in op amp technology these days, and you'll get as many opinions as there are manufacturers. Certainly, everyone will cite speed, precision and a myriad of lower/higher parameters as the most-sought-after qualities, but exactly how to achieve one of these qualities without sacrificing the others is a source of continued debate. Some engineers will tout the advantages of dielectric isolation bipolar processes, while many others will warn of parasitic consequences when using such methods and claim that complementary bipolar processes are the means to the desired end. Meanwhile, CMOS technology is offering higher bandwidths than ever before with the traditional advantages of high input impedance and low input bias current.

The Max452 from Maxim (Sunnyvale, CA) is one such CMOS product, with a bandwidth of 50 MHz and a low input bias current of 10 pA. "It's an example of how a standard CMOS device is going to take the traditional bipolar op amp market by storm," says Brian Gilling, Maxim's director of product planning and management. Unheard-of bandwidths and additional analog switches inside CMOS op amps permit such applications as on-board two-, four-, or eight-channel multiplexers for video amplifiers.



Raytheon's RC4077 achieves an ultra-low offset voltage of $\pm 10\ \mu V$ maximum via a patented offset voltage nulling adjustment of internal thin-film resistors.

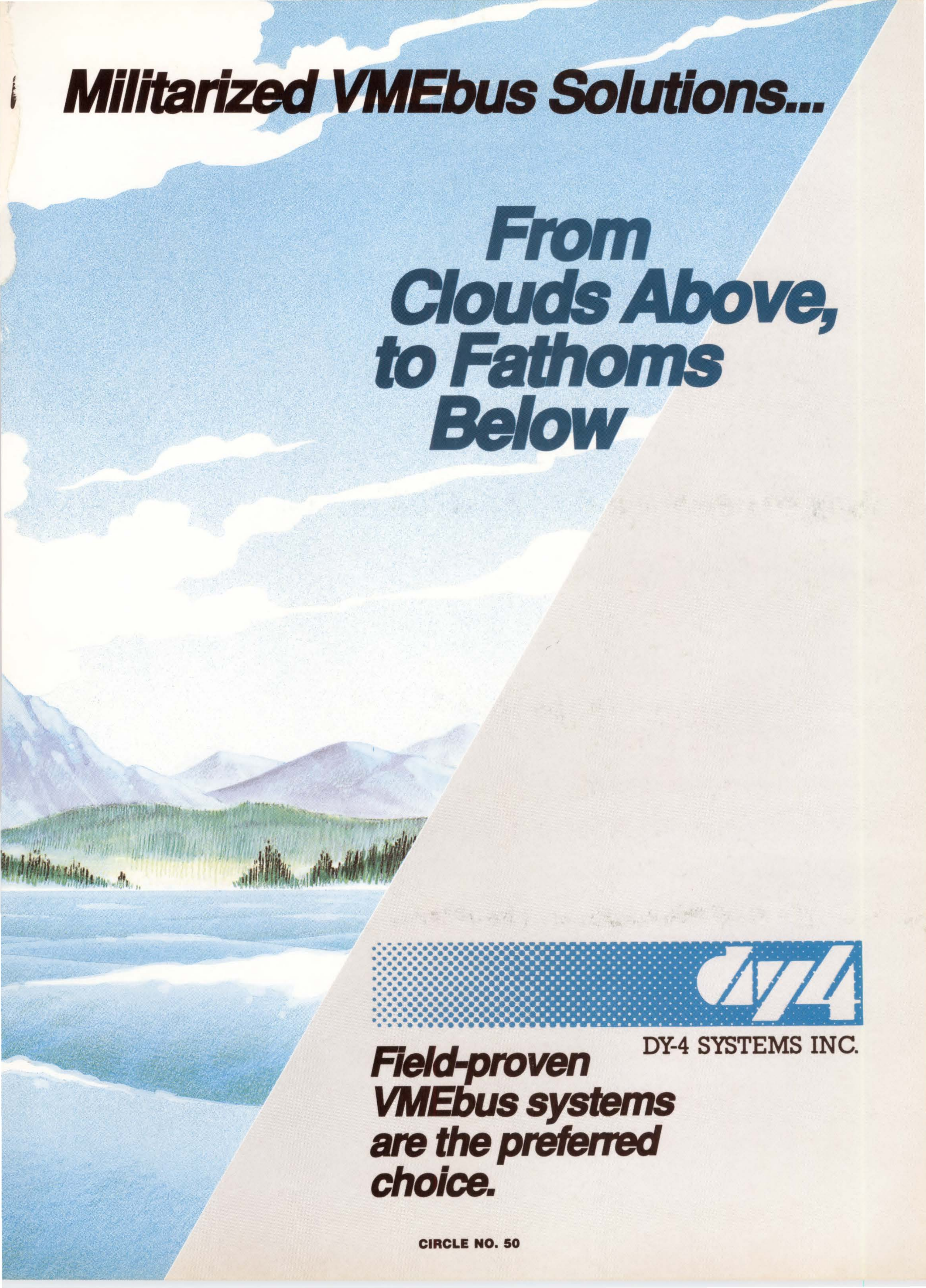
Innovations increase speed

While changes in CMOS technology are bringing about expanded bandwidths, bipolar processes are being improved to decrease settling times. Complementary bipolar technology is a process breakthrough developed by Analog Devices (Norwood, MA). "With this process, NPN transistors are just as fast as PNP transistors," says John Krehbiel, product marketing engineer at Analog Devices. "We are looking at 40- to 50-MHz signal bandwidths with a settling time of 100 ns for a 10-V step." The use of wideband PNP and NPN transistors eliminates the poor frequency response associated with lateral PNPs, allowing higher bandwidths as well as faster settling times.

Another manufacturer of op amps with fast settling times is Precision Monolithic (Santa Clara, CA). Designed for use in 12-bit digital-to-analog converters, the company's OP42 settles to within 0.01 percent of full scale in 750 ns. "We also market devices, such as the OP90, that have relatively small slew rates but are optimized for use in remote or solar-powered sensors," claims Art Kapoor, senior staff product marketing engineer. "Although the slew rate is 5 V/ms, the supply current is only 20 μA. A device like that can run on a 3-V lithium battery for almost nine months."

Harris Semiconductor (Melbourne, FL), meanwhile, is pursuing both ends of the op amp market by producing products that combine high slew rates with low supply currents. Fabricated in an advanced dielectric isolation process, the HA-2544 has a high slew rate (150 V/μs), a wide bandwidth (33 MHz), full internal compensation for unity gain stability and a low supply current.

Harris is exploring the use of junction field-effect transistor (JFET) inputs on its high-speed products. "The JFET is beneficial at the transducer level for small signals such as temperature samples because its very high input impedance does



Militarized VMEbus Solutions...
From
Clouds Above,
to Fathoms
Below
DY-4 SYSTEMS INC.
Field-proven
VMEbus systems
are the preferred
choice.
CIRCLE NO. 50

VMEbus System Solutions...

Chosen for many good reasons.

High performance, industry standard, multiprocessing architectures, applicable to Mil-Spec applications, field-proven ... DY-4's VME solutions satisfy the most stringent performance issues, regardless of the environment.

DY-4, a leader in Mil-Spec VME system solutions provides you with more than high-performance boards. We understand the specialized needs of mission-critical programs. Our products are many — boards, chassis, system-level diagnostics, RTOS, and application software supported by program management, ILS, QA, configuration management and proposal support.

At DY-4, we offer experience-proven capabilities.

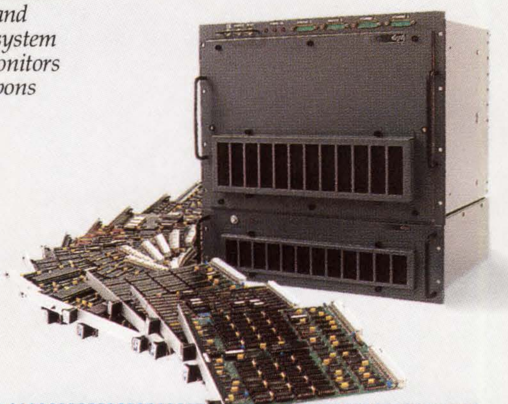
Proven on land, sea and air.

Off-The-Shelf and NDI

Backed by years of design experience, we offer over 50 off-the-shelf VME boards for a variety of applications:

- *68020/68030 Single Board Computers*
- *Intelligent Peripheral Controllers*
- *Multiprocessor RTOS*
- *System-level Diagnostics*
- *NTDS Interfaces*
- *IEEE 802.3*
- *ANSI X3T9.5 (FDDI)*
- *SDC/DSC*
- *Graphics*
- *MIL-Std 1553B*
- *ARINC 429*
- *ANSI X3T9.2 (SCSI)*
- *Memory*
- *Chassis*

CIRCLE NO. 50



...And Into the Future.

Anticipating the demands of tomorrow's applications. Providing the systems solutions. DY-4 is laying the technology groundwork today. Look to us for:

- *Advanced conduction-cooled products and system chassis*
- *Man-machine interfaces*
- *Ada™ Multiprocessor Development Environment*
- *Enhanced performance via custom silicon*
- *Relational Data Base Processor Subsystem*

DY-4 SYSTEMS INC.

For more details on DY-4's VME solutions, contact:

DY-4 Systems Inc.
21 Credit Union Way
Nepean, Ontario
Canada K2H 9G1

Phone: (613) 596-9911
FAX: (613) 596-0574
TELEX: 053411

Campbell, California (408) 377-9822
Los Angeles, California (714) 549-2559
Washington, D.C. (301) 964-5554
Boston, Massachusetts (617) 692-9308
Denmark (06) 96-3624
Ferranti Computer Systems, England 011 44 6333 71111

™ Ada is a trademark of the United States Department of Defense

Printed in the USA

CIRCLE NO. 50

Model	Full-power Bandwidth (MHz)	Min. Slew Rate (V/μs)	Typ. Settling Time to 0.1 Percent (ns)	Max. Input Bias Curr. (nA)	Input Offset V (μV at +25° C)	Supply Voltage (V)	Max. Offset V (μV/° C)	Packages	Price (OEM qty)	Comments
Advanced Linear Devices 1030 W Maude Ave, Suite 501, Sunnyvale, CA 94086 (408) 720-8737 **Circle 100**										
ALD1701	0.7	0.7	10,000	0.03	900	±1 to±6/ +2 to+12	7	SO, DIP, DIE	$1.07	rail to rail
ALD1702	1.5	2.1	3,000	0.03	900	±2 to±6/ +4 to+12	7	SO, DIP, DIE	$1.26	rail to rail
ALD1703	1.5	2.1	3,000	0.05	10,000	±2 to±6/ +4 to+12	10	SO, DIP, DIE	$0.89	—
ALD1704	2.1	5	2,000	0.02	900	±3.25 to±6/ +6.5 to+12	5	SO, DIP, DIE	$1.13	rail to rail
ALD1706	0.3	0.17	10,000	0.03	900	±1 to±6/ +2 to+12	7	SO, DIP, DIE	$1.30	rail to rail
ALD1706	0.7	0.7	10,000	0.03	2,000	±1 to±6/ +2 to+12	7	SO, DIP, DIE	$1.31	rail to rail; dual
ALD4701	0.7	0.7	10,000	0.03	2,000	±1 to±6/ +2 to+12	7	SO, DIP, DIE	$2.50	rail to rail; quad
Anadigics 35 Technology Dr, Box 4915, Warren, NJ 07060 (201) 668-5000 **Circle 101**										
AOP1510	35	750	30	100	1,500	±9	—	DIP	$29	—
AOP3510	100	1,500	15	100	1,500	±9	—	DIP	$32.75	—
Analog Devices 1 Technology Way, PO Box 9106, Norwood, MA 02062 (617) 329-4700 **Circle 102**										
AD9610B	80	3,000	25	15 μA	1,000	±15	—	TO-8	$49.88	mil-spec versions
AD9611B	210	1,900	19	1 μA	3,000	±5	5	TO-8	$84	—
AD548C	0.03	1.8	8,000	0.01	250	±15	2	mini-DIP, TO-99	$1.45	BiFET
AD648C	0.03	1.8	8,000	0.01	300	±15	3	mini-DIP, CERDIP, TO-99	$1.80	low-power BiFET
AD707C	0.9	0.3	—	1	15	±15	0.1	mini-DIP, CERDIP, TO-99	$16	ultra low drift
AD711J	0.2	16	1 μs	0.05	250	±15	3	mini-DIP, CERDIP, TO-99	$0.80	BiFET
AD845J	1.75	100	350	1	1,500	±15	20	mini-DIP, CERDIP	$4.50	complementary bipolar process
AD847J	12.7	200	65	6.6	1,000	±15	15	mini-DIP, SO, CERDIP	$2.95	high speed; low power
Burr-Brown PO Box 11400, Tucson, AZ 85734 (602) 746-1111 **Circle 103**										
OPA111AM	0.032	1	6,000	0.002	100	±5 to±18	±5	TO-99	$5.95	low end of series
OPA121KP	0.032	2	6,000	0.01	±500	±5 to±18	±10	TO-99, DIP, SO	$3.40	low end of series
OPA128JM	0.047	0.5	5,000	300 fA	260	±5 to±18	±20	TO-99	$7.70	low end of series
OPA404AG	0.57	24	600	0.012	1,000	±5 to±18	±3	DIP, SO	$6.60	low end of series
OPA602BP	0.57	20	600	0.01	1,000	±5 to±18	±15	DIP, TO-99	$2.20	low end of series
OPA606KP	0.47	20	1,000	0.025	300	±5 to±18	20	DIP, TO-99	$2.40	low end of series
OPA27C/G	—	1.7	—	80	25	±4 to±22	1.8	DIP, SO, TO-99	$2.65	low end of series
OPA37C/G	—	11	—	80	25	±4 to±22	1.8	DIP, TO-99, SO	$2.65	low end of series
OPA445AP	0.45	5	—	20	2,000	±10 to±45	15	DIP, TO-99	$3.50	low end of series
OPA541AM	0.55	8	2	0.5	2,000	±10 to±35	40	TO-3	$16.30	low end of series
Comlinear 4800 Wheaton Dr, Fort Collins, CO 80525 (303) 226-0500 **Circle 104**										
CLC400	50	450	10	2,500	2,000	±2.5 to±7	40	DIP	$15.50	commercial, mil-spec
CLC401	100	700	10	3,000	3,000	±2.5 to±7	50	DIP	$15.50	same as above
CLC401	80	700	—	3,000	1,500	±2.5 to±7	20	DIP	$17.10	output voltage clamp

Key: BiFET=field-effect transistor input/bipolar amplifier; CERDIP=ceramic dual in-line package; DIP=dual in-line package; Isy=supply current; JFET=junction field-effect transistor; LCC=leadless chip carrier; SO=small outline IC; V_{os}=offset voltage.

TCP/IP

for 386 UNIX PCs.

Up and running, fast and easy.

Presenting CMC's TCP/System V.3 for 386-based UNIX PCs. Teamed with CMC's ENP-66 intelligent Ethernet node processor, you get both industry-standard TCP protocols with simultaneous use of AT&T-style networking and 4.2 BSD networking. This powerful performance package includes full support for the STREAMS I/O system, the Transport Level Interface (TLI) and Remote File System (RFS), AT&T's distributed file system.

The fastest TCP for V.3 available is also the easiest. TCP/System V.3 provides an exceptionally simple procedure for installing its device driver and applications programs.

TCP/System V.3 is just one part of CMC's family of high-performance Ethernet TCP/IP and ISO networking solutions.

Set your own LAN speed record. You chose your 386 PC for its power, so choose your networking the same way. The fastest way to get TCP/IP up and running on 386 UNIX PCs is to call CMC today.

1/800/CMC/802.3

CMC

We set the LAN speed record.

125 Cremona Drive, Santa Barbara, CA 93117
1/805/968/4262 TWX 240876 FAX 1/805/968/6478

CIRCLE NO. 42

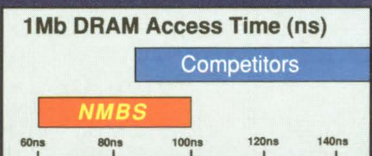
Model	Full-power Bandwidth (MHz)	Min. Slew Rate (V/µs)	Typ. Settling Time to 0.1 Percent (ns)	Max. Input Bias Curr. (nA)	Input Offset V (µV at +25° C)	Supply Voltage (V)	Max. Offset V (µV/° C)	Packages	Price (OEM qty)	Comments
Elantec 1996 Tarob Ct, Milpitas, CA 95035 (408) 945-1323										Circle 105
EHA51XX/ 21XX	5.09	160	330	15,000	2,000	±5 to ±17.5	20	DIP, LCC, TO-8	$8.65	—
EHA260X	0.06	4	250	10	4,000	±5 to ±17.5	5	DIP, LCC, TO-99	$1.76	—
EHA262X	0.4	25	200	15	4,000	±5 to ±17.5	5	DIP, LCC, TO-99	$4.95	—
EL2020	4.77	300	70	15,000	10,000	±5 to ±17.5	20	DIP, LCC	$4.95	—
EL2038	12.73	800	90	20,000	4,000	±5 to ±17.5	20	DIP, LCC	$3.90	—
EL2041	2.39	150	90	20,000	2,000	±5 to ±17.5	20	DIP, TO-8	$6.08	—
EHA24XX	0.32	20	1,500	200	4,000	±5 to ±22.5	20	DIP	$11.27	—
EHA250X	0.4	25	330	200	5,000	±7 to ±20	20	DIP, LCC, TO-99	$2.51	—
EHA251X	0.8	50	250	200	8,000	±7 to ±20	20	DIP, LCC, TO-99	$1.92	—
EHA252X	1.59	100	200	200	8,000	±7 to ±20	20	DIP, LCC, TO-99	$3.25	—
EHA253X	8.75	550	—	20,000	2,000	±5 to ±17.5	20	DIP, LCC	$3.71	—
EHA254X	5.57	350	1,500	20,000	2,000	±5 to ±17.5	20	DIP, LCC	$4.01	—
Harris Semiconductor PO Box 883, Melbourne, FL 32901 (305) 724-7000										Circle 106
HA-2539/40	9.5	550	180	20,000	8,000	±5 to ±15	20	CERDIP, LCC, PLCC	$3.71	wide bandwidth
HA-2541	4	200	90	25,000	800	±8 to ±15	9	DIP, can	$6.08	unity gain stable
HA-2542	5.5	300	100	35,000	5,000	±8 to ±15	14	DIP, can	$7.09	video line driver
HA-2544	4.2	100	120	18,000	6,000	±5 to ±15	10	DIP, PLCC, LCC, can	$3.04	new video amp
HA-2529	2.6	135	200	200	2,000	±5 to ±15	10	DIP, LCC, PLCC, can	$4.05	high output current
HA-5147A	0.5	28	400	40	25	±5 to ±15	0.6	CERDIP, LCC, can	$6.58	ultra low noise; high speed
HA-5127A	0.16	7	1,500	40	25	±5 to ±15	0.6	same as above	$5.06	—
HA-5134	0.016	0.75	13,000	25	100	±5 to ±15	1.2	DIP, LCC, PLCC	$9.45	quad precision
HA-5177	0.01	0.5	14,000	2	25	±5 to ±15	0.3	DIP, LCC, can	$4.39	—
HA-5170	0.12	5	1,000	0.1	100	±8 to ±15	5	DIP, LCC, can	$8.52	JFET input
HA-5111/ 12/14	0.318	12	600	200	5,000	±5 to ±15	3	DIP, LCC, can	$4.73	uncompensated; single, dual, quad
Linear Technology 1630 McCarthy Blvd, Milpitas, CA 95035 (408) 432-1900										Circle 107
LT1024A	0.7	0.1	—	0.12	50	±20	50	DIP	$6.95	dual matched input
LT1057A	3.5	10	1.3	0.05	450	±20	150	DIP, TO-99	$4.95	dual
LT1058A	3.5	10	1.3	0.05	600	±20	180	DIP	$9.55	quad
LT1012M	0.7	0.1	—	0.01	35	±20	35	DIP, TO-99	$6.50	—
LTC1052C	1.2	4	—	0.03	5	±18	5	DIP, TO-99	$4.30	chopper stabilized
LT1008	—	0.1	—	100	120	±20	120	DIP, TO-99	$3.80	—
LT1014A	1	0.2	—	20	50	±22	150	DIP	$8.50	quad
LT1007A	5	11	—	35	25	±22	25	DIP, TO-99	$5	—
LT1006A	1	0.25	—	15	50	±22	50	DIP, TO-99	$2.80	—
LT1013A	1	0.2	—	20	40	±22	150	DIP, TO-99	$5.90	—
LT1078A	0.2	0.07	—	10	120	±22	70	DIP, TO-99	$5.15	micropower; dual
LT1079H	0.2	0.07	—	10	150	±22	70	DIP	$6.50	micropower; quad
LT1028A	50	11	—	90	40	±22	40	DIP, TO-99	$7.55	very low noise
Maxim 120 San Gabriel Dr, Sunnyvale, CA 94086 (408) 737-7600										Circle 108
Max 400	0.4	0.3	—	2	10	±3 to ±22	0.3	DIP, TO-99	$6	low V_{os}; bipolar
Max 430	0.5	0.5	—	0.1	5	±2.5 to ±16.5	0.05	DIP	$5.65	bipolar
Max 452	50	150	100	10	5,000	±4.5 to ±5.5	100	DIP, SO	$3	CMOS

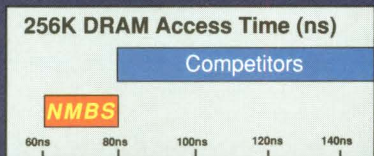
Model	Full-power Bandwidth (MHz)	Min. Slew Rate (V/μs)	Typ. Settling Time to 0.1 Percent (ns)	Max. Input Bias Curr. (nA)	Input Offset V (μV at +25° C)	Supply Voltage (V)	Max. Offset V (μV/° C)	Packages	Price (OEM qty)	Comments
Motorola Semiconductor Products PO Box 20912, Phoenix, AZ 85036 (800) 521-6274 **Circle 109**										
MC34080	0.8	40	720	0.2	1,000	±3 to±18	10	DIP	$0.38	single, dual, quad
MC34181	0.2	7	1,100	0.1	2,000	±1.5 to±18	10	DIP, SO	$0.35	same as above
MC33077	0.2	8	–	1,000	1,000	±2.5 to±18	2	DIP	$0.82	dual
NEC Electronics 401 Ellis St, PO Box 7241, Mountain View, CA 94039 (415) 960-6000 **Circle 110**										
PC815	7	0.8	–	±55	20	±3 to±22	20	DIP	–	–
PC816	25	3	–	±55	20	±3 to±22	20	DIP	–	–
PC842	3.5	7	–	500	1,000	+3 to+36	–	DIP	–	dual
PC844C	3.5	7	–	500	1,000	+3 to+36	–	DIP, flat IC	–	quad
Precision Monolithics 1500 Space Park Dr, Santa Clara, CA 95054 (408) 727-9222 **Circle 111**										
OP-43GP	–	5	–	0.025	1,500	±10 to±18	7.5	DIP	$2.60	JFET; tighter spec grades avail.
OP-42FZ	0.6	40	300	0.25	1,500	±8 to±20	8	CERDIP	$3.75	same as above
OP-44FZ	1.2	80	200	0.25	1,500	±8 to±20	8	CERDIP	$5.40	same as above
OP-200GP	–	0.1	–	5	200	±3 to±18	2	DIP	$2.95	dual OP-77
OP-400GP	–	0.1	–	7	300	±3 to±18	2.5	DIP	$5.35	quad OP-77
OP-77GP	–	0.1	–	2.8	100	±3 to±18	1.2	DIP	$1.25	tighter grades avail.
OP-90GP	–	0.005	–	25	450	+1.6 to±36/ ±0.8 to±18	5	DIP	$1.60	Isy=20 μA max
OP-290GP	–	0.005	–	25	500	same as above	–	DIP	$2.50	dual OP-90
OP-490GP	–	0.005	–	25	1,000	same as above	–	DIP	$3.30	quad OP-90
OP-97FP	–	0.1	–	0.15	75	±2 to±20	2	DIP	$1.60	Isy=600 μA max
Raytheon, Semiconductor Div 350 Ellis St, Mountain View, CA 94043 (415) 968-9211 **Circle 112**										
RC4077	0.8	0.25	–	20	4	±15	0.3	DIP, LCC, TO-99	–	–
LT1001	0.8	0.2	–	2	7	±15	0.6	DIP, LCC, TO-99	–	–
RC4227	8	2.7	–	15	20	±15	1.3	DIP	–	dual
RC4207	1.5	0.3	–	5	30	±15	1.3	DIP	–	dual
LM148/ 248/348	1	0.5	–	100	1	±15	–	DIP	–	quad
OP-07	0.5	0.1	–	2	10	±15	0.6	DIP, LCC, TO-99	–	quad
OP-27	8	1.7	–	40	10	±15	0.6	DIP, LCC, TO-99	–	very low noise
OP-37	40	11	–	40	10	±15	0.6	DIP, TO-99	–	same as above
OP-47	42	25	–	55	20	±15	1.3	DIP, TO-99	–	same as above
OP-05	0.5	0.1	–	2	70	±15	0.9	DIP, TO-99	–	instrumentation grade
RC5532	10	8	–	400	0.5	±15	–	DIP, TO-99	–	dual
SGS-Thomson 1000 E Bell Rd, Phoenix, AZ 85022 (602) 867-6100 **Circle 113**										
LM318	15	50	–	500	0.2	±20	–	DIP, TO-99, SO	$0.67	–
LM301A	–	0.5	–	250	7,500	±18	30	DIP, TO-99, SO	$0.24	–
LM308A	–	–	–	7	–	±18	5	DIP, TO-99, SO	$0.31	–
LM346	4.5	12	–	250	6,000	±18	–	DIP, TO-99, SO	$0.85	–
LF355A	2.5	5	4,000	0.2	2,000	±18	–	DIP, TO-99, SO	–	–
LF356A	4.5	12	1,500	0.2	2,000	±18	–	DIP, TO-99, SO	–	–
LF357A	20	40	1,500	0.2	2,300	±18	–	DIP, TO-99, SO	–	–
TL061B	1	3.5	–	0.2	3,000	±18	10	DIP, TO-99, SO	$0.90	–
TL071B	3	10	–	0.2	3,000	±18	10	DIP, TO-99, SO	$0.85	–
TL081B	3	13	–	0.2	3,000	±18	10	DIP, TO-99, SO	$0.84	–

DRAMATIC!

Now...Highest speeds AND production... 60/70/80ns 1Mb AND 256K DRAMS...

Exclusively from NMB Semiconductor - the high speed DRAM specialist - we've broken the speed barrier with FutureFast™ 256K and 1Mb DRAMS...first with access times of 60/70/80ns. This means designers can now have true "0" wait state systems without using complex, expensive cache memory techniques.

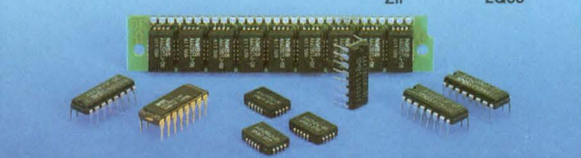




We've broken the delivery barrier too. NMBS offers much higher volume production than our competitors. These dramatic advances are made possible in the most advanced CMOS/VLSI plant in the world optimized for volume production of high speed DRAMS. With computerized operation and robot control in Class 1 ultra-clean rooms. Plus state-of-the-art design, processing and testing.

Product Line Summary

Series*	Access Time	Organization	Package**	Availability
AAA2800 256K	60/70/80 (ns)	256Kx1	P-DIP PLCC C-DIP	Production Production Production
AAA1M100 1Mb	100/120 (ns)	256Kx4 1Mbx1	P-DIP SOJ ZIP	Production Production Production
AAA1M200 1Mb	60/70/80 (ns)	256Kx4 1Mbx1	P-DIP SOJ ZIP	2Q88 2Q88 2Q88



* All Series available in Static Column and Page Modes ** SIMM'S and SIPS available for each series

Available in the packages and organizations designers want for high performance projects.

More good news. We're now shipping qualification samples of our new 1Mb DRAM.

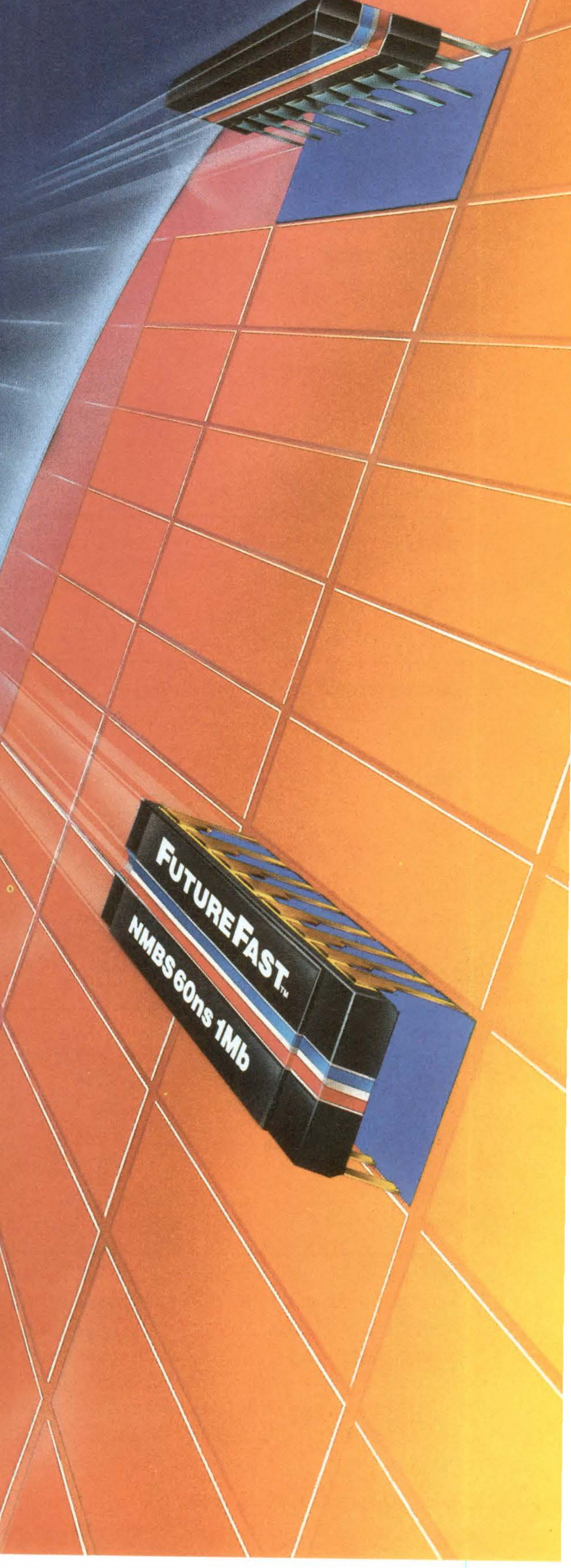
So for complete specs, evaluation units, quantity prices and delivery call NMBS - the high speed DRAM specialists - today. Prove to yourself that with FutureFast™ DRAMS, your future is now.

NMB | NMB TECHNOLOGIES INCORPORATED

SEMICONDUCTOR DIVISION
9730 Independence Ave. • Chatsworth, CA 91311
Tel: 818/341-3355, FAX: 818/341-8207, TLX: 651340

FUTUREFAST™
...IS NOW.

CIRCLE NO. 43



Model	Full-power Bandwidth (MHz)	Min. Slew Rate (V/μs)	Typ. Settling Time to 0.1 Percent (ns)	Max. Input Bias Curr. (nA)	Input Offset V (μV at +25° C)	Supply Voltage (V)	Max. Offset V (μV/° C)	Packages	Price (OEM qty)	Comments
Signetics 811 E Arques Ave, PO Box 3409, Sunnyvale, CA 94088 (408) 991-4250										**Circle 114**
NE5212	140	—	—	±80	—	+4.5 to 6	—	DIP, SO	$229	—
NE5230	0.18	0.25	2	40	400	±0.9 to ±7.5	—	DIP, SO	$0.99	—
NE5205	650	—	—	—	—	+5 to +8	—	DIP, SO, TO-46	$1,002	self-biasing; ac coupled
Silicon General 11861 Western Ave, Garden Grove, CA 92641 (714) 898-8121										**Circle 115**
SG1536	0.023	2	—	20	2,000	±40	—	TO-99	—	—
SG1436	0.023	2	—	40	5,000	±34	—	TO-99	—	—
SG1436	0.023	2	—	90	5,000	±30	—	TO-99	—	—
SG1173	—	—	—	500	2,000	±24	—	TO-66, 220	—	—
SG124	—	—	—	300	2,000	±16	—	DIP	—	quad
SG224/324	—	—	—	500	2,000	±16	—	DIP	—	—
SG1250	—	—	—	20	4,000	±18	—	DIP	—	single, dual, triple
SG3250	—	—	—	50	7,500	±18	—	DIP	—	same as above
SG4250	0.25	0.16	—	50	7,500	±18	—	DIP	—	single
Siliconix 2201 Laurelwood Rd, Santa Clara, CA 95054 (800) 554-5565										**Circle 116**
L144A	0.6	0.4	—	200	5,000	±1.5 to ±15	3.3	DIP, flat IC	—	—
L144B0.6	0.6	0.4	—	200	6,000	±1.5 to ±15	3.3	DIP, flat IC	—	—
L144C	0.6	0.4	—	250	10,000	±1.5 to ±15	3.3	DIP, flat IC	—	—
Texas Instruments 2804 Linden Lea, Irving, TX 75061 (214) 233-5161										**Circle 117**
TLC25L4	0.1	0.04	—	0.001	10,000	1.4 to 16	0.7	DIP, SO	$5.61	quad; factory set
TLC274	2.2	5.3	—	0.0007	10,000	3 to 16	2	DIP, SO	$1.25	quad; programmable
TLC279	2.2	5.3	—	0.0007	1,200	3 to 16	2	DIP, SO	$2.61	quad; high precision; high gain
TL031	1.1	2	1,000	0.2	1,500	±18	—	DIP, SO	$0.49	single; low power
TL054	2.7	10	1,000	0.2	4,000	±18	8	DIP, SO	$1.09	single, dual, quad
TL064	1	2	1,500	0.2	15,000	±18	10	DIP, SO	$1	quad
TL074	3	8	1,200	0.2	10,000	±18	18	DIP, SO	$0.75	single, dual, quad
TL084	3	8	1,200	0.4	15,000	±18	18	DIP, SO	$0.58	single, dual, quad
TL087	3.2	10	1,200	0.4	15,000	±18	18	DIP, SO	$2.92	single; ultraprecise input
TL287	3.2	10	—	0.2	500	±18	9	DIP, SO	$4.43	ultraprecise input
VTC 2401 E 86th St, Bloomington, MN 55425 (612) 851-5200										**Circle 118**
VA701	0.3	10	10,000	40	25	±6	±1	DIP, TO-99	$2.93	available in quad
VA705	1.8	35	250	900	1,000	±6	±20	DIP, SO, TO-99	$3.36	same as above
VA706	2.2	42	200	1,100	4,000	±6	±20	DIP, SO, TO-99	$3.03	same as above
VA707	5.6	105	150	1,100	3,000	±6	±20	DIP, SO, TO-99	$4.60	same as above
VA708	4.8	90	150	1,100	3,000	±6	±20	DIP, SO, TO-99	$4.10	same as above
VA711	0.8	30	10,000	40	25	±6	±1	DIP, SO, TO-99	$4.36	same as above
VA721	4	150	2,500	40	25	±6	±1	DIP, SO, TO-99	$4.86	same as above

not load down the original signal,'' says Daniel Bye, senior applications engineer for Harris.

There are applications—such as instrumentation and low-level signal conditioning—where accuracy is more important than speed. Manufacturers are meeting these needs by producing higher-precision op amps. The RC4077 from Raytheon (Mountain View, CA), for example, uses post-packaging trim techniques to achieve offset voltages as low as ±4 μV at 25° C with a temperature coefficient of 0.3 μV/° C. With zener-zapping trim techniques, Raytheon can put these low offset specs into a variety of packages, such as plastic dual in-line (DIP) and small-outline packages, which result in a low-cost, precision product. **CD**

Who's got the button?

Nobody, but nobody, offers or <u>delivers</u> more rechargeable button cells and batteries than Varta.

The first in NiCd batteries.

This year, 1988, Varta celebrates its 100th year in manufacturing batteries of all types. In the '50's we led the world in commercialization of NiCd batteries.

100 years 1888 1988 VARTA

We invented the mass-plate cell construction which excels over sintered nickel-cadmium cells.

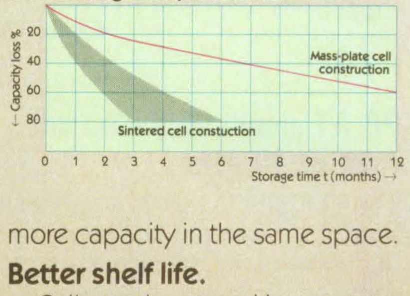
Unique performance advantages.

In stand-by at ambient temperatures, our mass-plate button cells retain 60% capacity after 12 months versus about three months for sintered NiCd cells, because they have much lower internal losses. Similarly, they require much lower recharging rates, as low as 1mA (C/100) versus 4-7mA for competition, so charging power and circuitry will be minimized.

More compact designs.

Varta mass-plate button cells and batteries usually take much less space—or let you put up to 40% more capacity in the same space.

Self discharge comparison at 20°C



Better shelf life.

Cells can be stored in any state of charge for over five years without significant loss of performance.

Cost benefits, too.

With all their advantages, Varta mass-plate button cells and batteries usually cost <u>less</u> than comparable sintered-type cells.

Many sizes and types.

Capacities range from 4 mAh to 1000 mAh. Many flat or stacked batteries can be assembled. Extra high temperature ratings and UL listings are available in key sizes. For rechargeable applications above 1000 mAh, Varta also offers a complete line of NiCd cells and batteries.

For an introduction to Varta's world-leading line of rechargeable button cells and batteries, please ask for "Who's Got The Button". Call 1-800-431-2504, Ext. 260, or write below.

VARTA

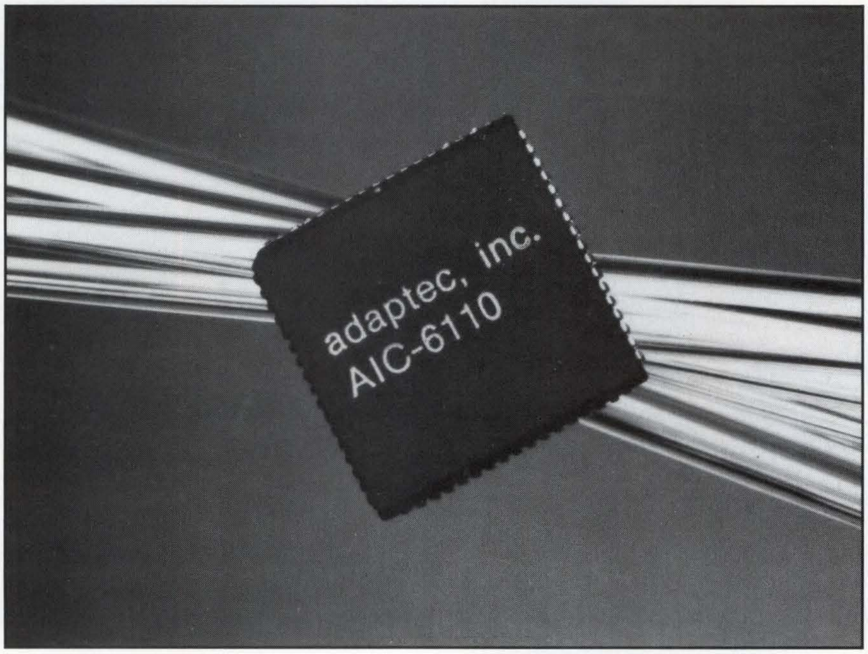
VARTA Batterie AG, Am Leineufer 51, D-3000 Hannover 21, West Germany, Tel. (49) 0511/79031
VARTA Batteries, Inc., 300 Executive Blvd., Elmsford, NY 10523, USA, Tel. 1-800-431-2504, Ext. 260
VARTA Batteries Pte Ltd., 1646 Bedok North P.O. Box 55, Singapore 9146, Tel. (65) 241-2633

CIRCLE NO. 44

Single-chip SCSI controller offers 5-Mbyte/s transfer rate

Supporting drive data transfer rates of up to 20 MHz, the AIC-6100 single-chip small computer system interface (SCSI) controller boasts a synchronous data transfer rate of 5 Mbytes/s and an asynchronous rate of 3 Mbytes/s.

The chip provides all the functions of a mass-storage controller except data separation, and it offers enhanced functional capability for direct 64-kbyte dynamic RAM access and write precompensation support.



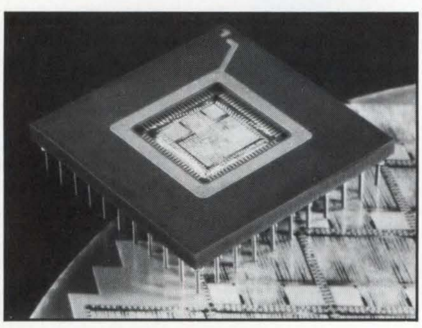
The device features additional logic for enhanced functionality and interface, as well as 48-mA drivers that allow direct connection to the SCSI bus. Functions of a programmable controller, buffer manager, encode/decode chip and host interface SCSI protocol chip are on the controller.

The chip's SCSI bus initiator and target modes let one drive act as an initiator when copying to another drive, while the 8-byte first-in, first-out buffer maximizes synchronous or asynchronous performance. Programmable precomp lets designers compensate for variations in bit recording, enabling the use of greater portions of a disk surface without external delay lines. Pricing is $25 for 1,000-piece quantities.

Adaptec, 691 S Milpitas Blvd, Milpitas, CA 95035. **Circle 121**

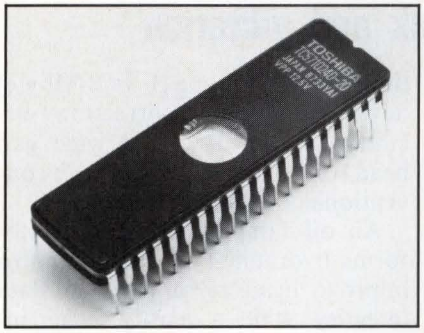
16-bit microcontroller performs at 10 Mips

Designed around the Forth-based reduced-instruction-set core processor, the RTX 2000 16-bit programmable microcontroller for embedded real-time applications provides greater than 10-Mips processing speed. The chip features parameter and stack memories of 256 words each, a single-cycle 16- × 16-bit hardware multiplier, an interrupt controller and three general-purpose timers. The microcontroller's ASIC Bus allows the attachment of external ASIC peripherals to the IC. The bus provides a parallel communications interface for system enhancements such as hardware acceleration or design flexibility through application-specific I/O. Pricing is $190 each in quantities of 1,000. **Harris,** PO Box 883, Melbourne, FL 32901. **Circle 122**



PC AT-compatible chip set runs at 16 MHz

The VL82CPCAT-16 is a zero-wait-state, high-integration five-chip set that reduces the nonmemory device count on the mother boards of IBM PC- and PC AT-compatible computers from 88 to 15 ICs. A clock-modulation feature permits operations on slower expansion cards in the 16-MHz environment, while "shadow RAM" enhances performance by bypassing ROM access delays. An on-chip "hot reset" allows faster access to protected memory. Address and data buffers are part of the chip set, as well as peripheral, system and memory controllers. In 5,000-set quantities, the price is $69. **VLSI,** 8375 S River Pkwy, Tempe, AZ 85284. **Circle 123**

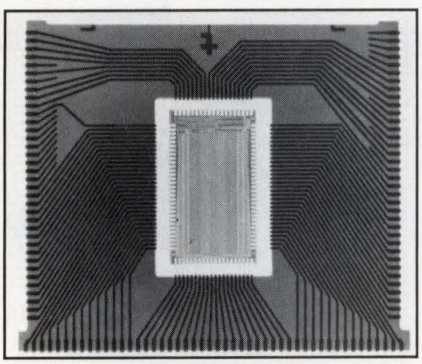


1-Mbit EPROM offers 16-bit word width

Organized as 64 kwords × 16 bits, the TC571024 1-Mbit EPROM offers an access time of up to 150 ns. With n-channel MOS memory cells and CMOS peripheral circuitry, the device operates at a maximum of 40 mA with a standby current of 100 μA from a single 5-V power supply. Packaged in the JEDEC standard 40-pin package, the chip is priced at $32.75 in 5,000-piece quantities. **Toshiba America,** 9775 Toledo Way, Irvine, CA 92718. **Circle 124**

LCD driver limits power consumption to 100 mW

With a data transfer rate of 16 Mbits/s, the PCF2201 liquid crystal display (LCD) driver provides multiplex rates from 1:32 to 1:256 while only using 100 mW of power. Driving both conventional twisted nematic and supertwisted birefringement-effect (SBE) LCDs, the device converts display data into parallel LCD drive waveforms for up to 81 rows or 80 columns of an LCD matrix. A 640- × 400-pixel SBE screen



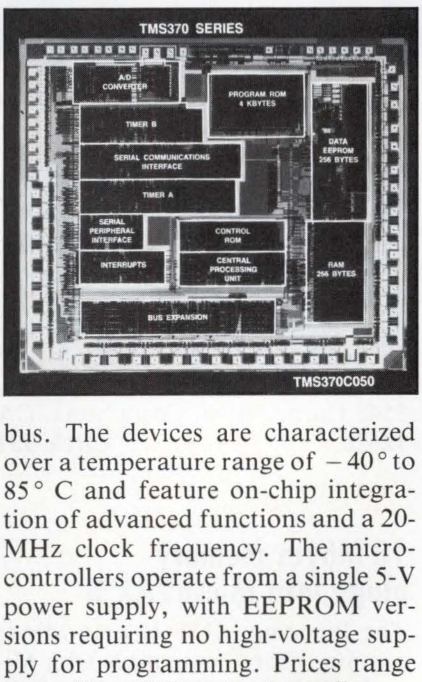
can be driven by 21 of the ICs, which come in a 120-pin tape automated bonding package. The chip, which runs at 4 MHz, includes over-temperature protection circuits and requires four supply voltages between −20 and +5 V for the four-level signals to the LCD.

Philips Components, PO Box 523, 5600 AM Eindhoven, The Netherlands. **Circle 125**

Signetics, 811 E Arques Ave, Sunnyvale, CA 94088. **Circle 126**

8-bit microcontrollers operate at 20 MHz

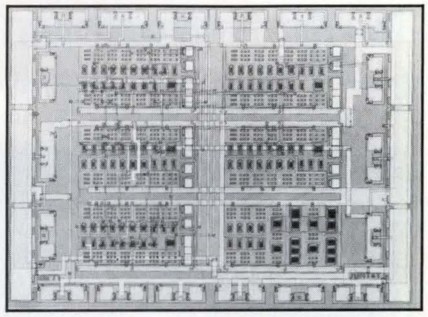
Fabricated in 1.6-micron CMOS, the TMS370 family of configurable 8-bit microcontrollers is based on a high-performance CPU and a modular



bus. The devices are characterized over a temperature range of −40° to 85° C and feature on-chip integration of advanced functions and a 20-MHz clock frequency. The microcontrollers operate from a single 5-V power supply, with EEPROM versions requiring no high-voltage supply for programming. Prices range from $3 to $10 each, depending on model and quantity. **Texas Instruments,** PO Box 809066, Dallas, TX 75380. **Circle 127**

Semicustom linear arrays provide 4.5-GHz speeds

Two additions to a family of semicustom linear arrays, the ALA201



and ALA202, offer the advantages of NPN and PNP transistors at speeds of 4.5 GHz for the NPN and 3.75 GHz for the PNP. The ALA201 is divided into six modules consisting of five standard modules and one power module, while the ALA202 is divided into 12 modules consisting of nine standard modules, two power modules and one input module. Both devices are designed on a regular grid system, and both have multiple collector contacts, which optimize output current drive. **AT&T Microelectronics,** 555 Union Blvd, Allentown, PA 18103. **Circle 128**

1-Mbit EPROM features 150-ns access time

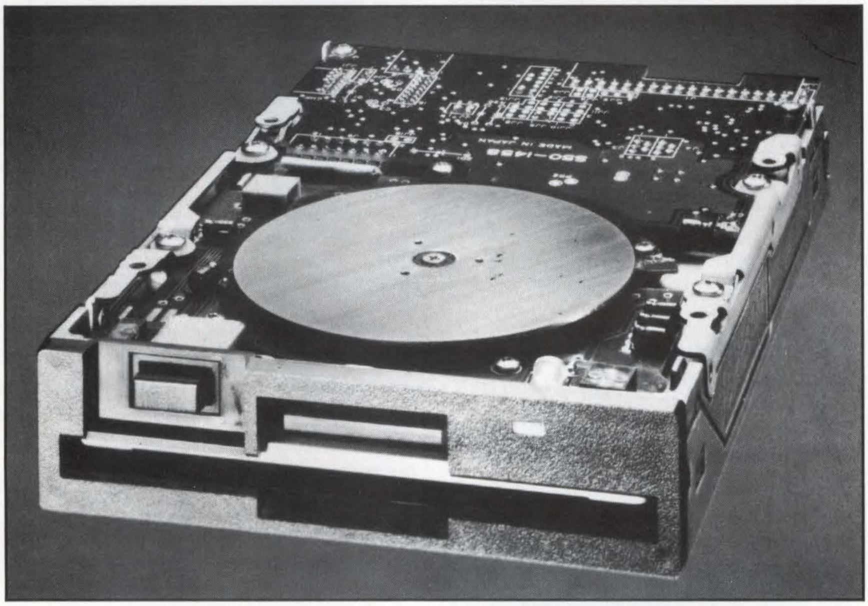
Produced in a low-power 1.3-micron CMOS process, the Am27C010 128k × 8-bit UV EPROM offers a maximum standby current of 100 μA for use in power-sensitive applications such as compact or portable systems. The chip comes in 170-, 200-, 250- and 300-ns versions and is available in 32-pin dual in-line and leadless chip carrier packages. In 100-piece quantities, prices start at $29.05. **Advanced Micro Devices,** 901 Thompson Pl, Sunnyvale, CA 94088. **Circle 129**

Coming August 1

Look for John Mayer's product focus report on nonvolatile memory.

Two-Mbyte microfloppy disk drive withstands shock and vibration

Designed for portable and laptop computers, the MD3611 3½-in. microfloppy disk drive boasts a die-cast chassis and a 60-G, 11-ms specification.

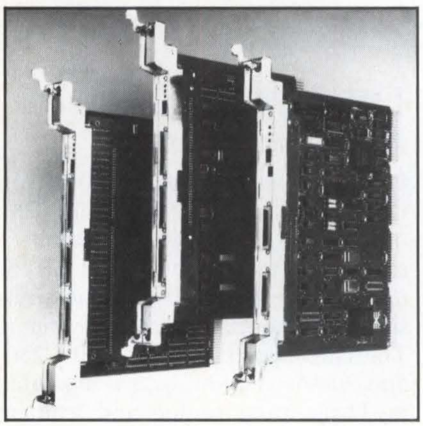


The dual-mode (1- or 2-Mbyte) device uses phase-correction circuitry combined with a wide gap head for full compatibility with conventional 1-Mbyte drives.

An oil-damping mechanism performs hydraulic-type cushioning to improve head reliability and data integrity, while a density sensor informs users whether 1- or 2-Mbyte media is being used.

Other features of the microfloppy disk drive include a dust shutter, automatic eject, a flush bezel, an optional dust cover and a dual-color LED to indicate which mode (1 or 2 Mbytes) is in operation. A brushless dc motor and CMOS circuitry let the device be powered from a single 5-V source. The drive and a documentation kit is priced at $100.

Canon USA, One Canon Plaza, Lake Success, NY 11042. **Circle 130**



Controller family interfaces with MicroVAX

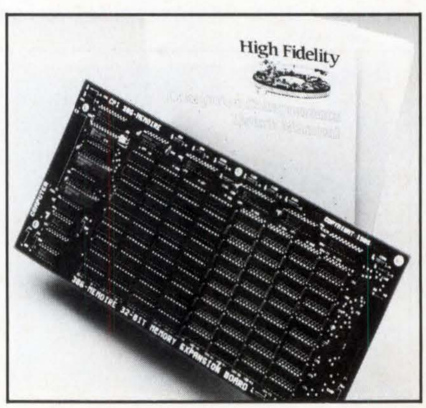
A family of quad-sized controllers conform to the revised Q-bus packaging used by Digital Equipment Corp in the MicroVAX 3500/3600. With a transfer rate of 3 Mbytes/s, the QD34 disk controller connects up to four enhanced storage module disk drives to the system, while the QD24, with transfer rates of up to 15 Mbits/s, can support up to four 5¼-in. enhanced small device interface disk drives. Supporting tape formats at speeds ranging from 12½ to 140 in./s, the QT14 tape controller handles data transfer rates of up to 1 Mbyte/s. The device has a 64-kbyte data buffer. The QD34, QD24 and QT14 are priced at $2,495, $1,795 and $1,395, respectively. **Emulex,** 3545 Harbor Blvd, Costa Mesa, CA 92626. **Circle 131**

16-Mbyte memory plugs into MicroVAX II

The Pincomm 616S is a 16-Mbyte memory board compatible with MicroVAX II and MicroVAX II workstations. Based on 1-Mbit dynamic RAMs, the board comes in either 8- or 16-Mbyte versions and may be used with Digital Equipment Corp boards already in the system. Each memory data word stored by the device is 36 bits wide, consisting of 32 data bits (four 8-bit bytes) plus 4 parity bits. **WesPac Technologies,** 9 Whatney St, Irvine CA 92718. **Circle 132**

32-bit memory board expands to 2 Mbytes

The 386 Memoire is a 32-bit memory expansion board for the Compaq Deskpro 386. The board supports up to 2 Mbytes of high-speed parity-checked memory and is designed to fit the 32-bit memory expansion slot on the Compaq. One Mbyte of memory is soldered on the board, which is socketed for upgrades to 2 Mbytes. Prices start at $695. **Computer Peripherals,** 667 Rancho Conejo Blvd, Newbury Park, CA 91320. **Circle 133**



Disk controller eliminates wait states in 80386 systems

A family of compact, short-form, high-speed Winchester hard disk drive controllers needs no wait states to match disk transfer rates and 80386-based CPU speeds. The 5122 (hard disk only) version can support two hard- or soft-sectored drives as well as optical devices, while the 5123 (hard disk/floppy combination) supports up to two hard disks and two floppy drives in any combination. The controllers are based on the enhanced small drive interface and provide error-free 2:1 sector interleaving to boost system throughput by as much as 30 percent. Prices begin at $135 in OEM quantities. **NCL America,** 1221 Innsbruck Dr, Sunnyvale, CA 94089. **Circle 134**

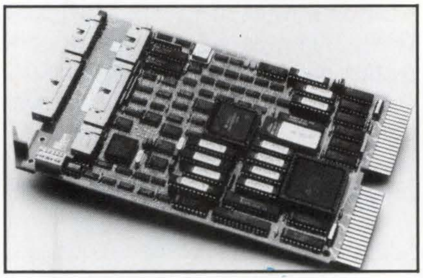
Single AT-compatible board provides 16-Mbyte memory

Occupying one chassis slot, the Just-RAM/AT 16 expansion board offers 512 kbytes to 16 Mbytes of conventional or extended memory. The card operates at either 10 MHz with no wait states or 12 MHz with one wait state, and requires only 15 W of power. Features of the board include switch-selectable starting addresses on 128-kbyte boundaries from 0 to 16 Mbytes; 256-kbyte or 1-Mbyte memory modules; and an expanded memory specification 4.0 driver with diagnostics. **Monolithic Systems,** 84 Inverness Cir E, Englewood, CO 80112. **Circle 135**

ESDI controller supports 2-Mbyte/s disks

Designed for the Compaq 386 and the IBM PC AT, the CFN 1000 is a 16-bit high-speed disk controller that interfaces with up to four enhanced small device interface disk drives. The board is capable of running with CPUs as fast as 20 MHz with no wait states and can support disk drives with data rates of over 2 Mbytes/s. Other features of the ESDI controller include universal use in any computer with an AT bus independent of ROM basic I/O system restrictions, and user-selectable running mode in either direct memory access or program I/O. The controller eliminates the DOS 32-Mbyte limits and lets disk drives be formatted in single volumes up to the physical limit of the drive. **CFN Industries,** 30-A Lindbergh Ave, Livermore, CA 94550. **Circle 136**

Controller interfaces floppy, Winchester drives to Q-bus



The MQ696 multipurpose disk controller is designed to interface up to two enhanced small disk interface Winchester disk drives and up to two SA450-compatible floppy disk drives to Q-bus computers. The controller supports hard disks that have data transfer rates as high as 2.5 Mbytes/s and floppy drives with either 5¼- or 3½-in. formats. It is compatible with DEC RX50/RX33 drives. The device's formatter is accessible through either the system processor or an RS-232 port to provide interactive terminal access to the controller. An automatic self-test function is initiated each time a drive is brought on-line. If the controller fails its self-test, the disk drives are isolated and a card-edge LED is extinguished. The board costs $1,550. **Digilog,** 1555 S Sinclair St, Anaheim, CA 92806. **Circle 137**

Design and Development Tools

Silicon composer uses variety of module sources

A generation tool for designing cell-based semicustom and structured-custom ICs handles full-custom blocks, compiled cells and standard cells simultaneously. Called SC II, the system offers a range of features optimized for mixed design.

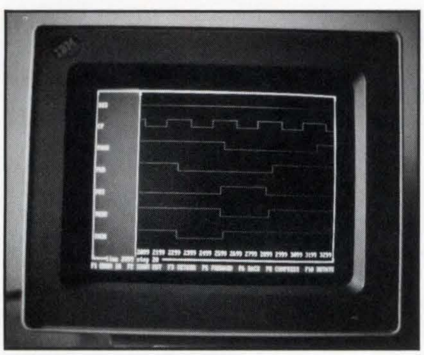
System features include column or row standard cell regions, free placement of large blocks in any location or orientation, multiple physical macros of different aspect ratios for each logic function, use of hard macros representing layouts of lower levels in the hierarchy, and flexible power busing.

The composer also offers both interactive and algorithmic floor-plan generation, allowing production of more compact layouts in less time. Over 20,000 cells per hierarchy level can be automatically placed and routed in an unlimited number of hierarchies, permitting the handling of an unlimited number of cells.

Floor plans that reflect, but aren't restricted to, the logic hierarchy may be generated algorithmically starting from user guidelines, including an optional fixed I/O placement. This floor planning accounts for the global connectivity of the circuit, producing floor plans that evenly distribute the routing over the chip area, minimizing congestion and reducing overall chip size.

Detail routing includes gridless, 2-, 2½- and 3-layer capability expandable to n layers, routing across and through cells, conditional routing and variable width routing. Pricing for the SC II silicon composer starts at $60,000.

Silvar-Lisco, 1080 Marsh Rd, Menlo Park, CA 94025. **Circle 138**



OS/2 version of logic simulator boosts PC capacity

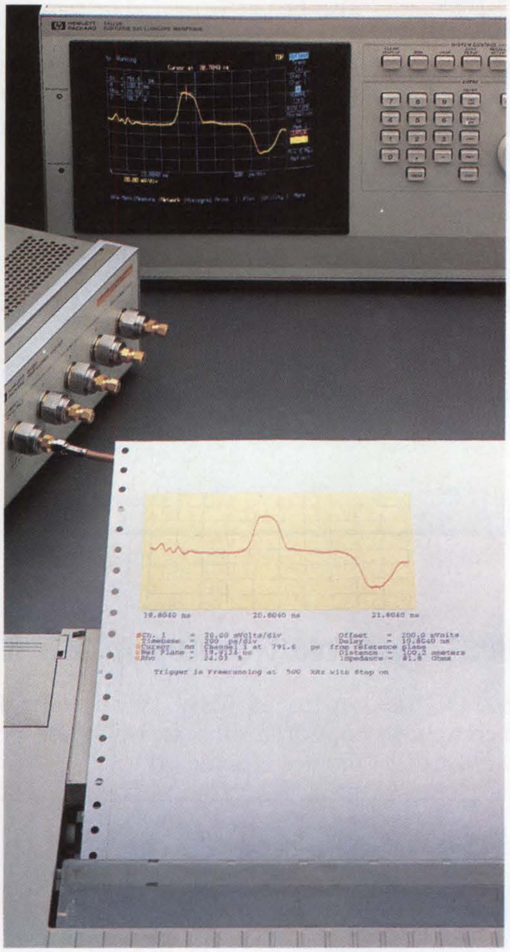
The Dsim logic simulator takes advantage of the 16-Mbyte addressable memory support provided by OS/2 1.0. Dsim can simulate only 2,500 gates within DOS's 640-kbyte limit. But under OS/2, it can simulate 7,000 gates in 1 Mbyte of memory. Other features include interactive waveform display, switch-level simulation and tabular display functions. The package costs $1,250. **Roche Systems,** 1705 N Rankin St, Appleton, WI 54911. **Circle 139**

CASE product provides 33 analysis reports

The Excelerator/RTS Version 1.8 is a computer-aided software engineering tool that offers expanded analysis capabilities for helping system designers improve the reliability and maintenance of real-time systems. The extended analysis feature provides 33 analysis reports and 25 matrices that check the validity, efficiency and completeness of systems designs. Graph-analysis functions allow logic verification of an entire system model while detecting errors. The graph-analysis reports check the system model against 50 rules specified in the Ward-Mellor technique regarding the flow of data and control in the system. The software is priced at $8,400. **Index Technology,** One Main St, Cambridge, MA 02142. **Circle 140** *we never stop asking* "What if..."

TDR Yesterday

TDR Today



The HP 54120T: precise TDR measurements never before possible.

Throw away the calculators and slide rules. Toss out the CRT camera, the pencils and the scratch paper. Enter an unprecedented realm of TDR measurement that is powerful, fast, accurate, and easy to use. The HP 54120T Digitizing Oscilloscope and TDR with 20 GHz bandwidth and 10 ps resolution will make your life a lot easier.

Match bandwidth to system requirements.

The software we developed for the HP 54120T enables you to accurately match bandwidth to the speed of the device under test. Normalization* then corrects for reflections and imperfections caused by connectors and cables. You measure the device–not the connecting hardware–for error-free readings.

In addition, the HP 54120T features unmatched speed and convenience. HP Auto-Scale gets waveforms to the screen quickly, automatic measurements produce test results fast, English-like commands via HP-IB make programming easy, time and voltage markers customize measurement parameters, hardcopy documentation is available at the push of a button. And there are numerous other features we simply can't get into a single ad.

Call HP today!
1-800-752-0900, Ext. F786.

Application notes are yours for the asking. They include "Improving TDR Network Analysis," "TDR Fundamentals," and other technical data. You'll see for yourself what the HP 54120T can do for your design, characterization and test applications.

**Normalization is accomplished using the Stanford Bracewell Transform. The Bracewell Transform is under license from Stanford University.*

HEWLETT PACKARD

Physical modeling module runs at 16.7-MHz clock rate

Offered as an option to the manufacturer's PMX Physical Modeling System, the Deepboard Part Evaluation Module has a memory capacity of 1 million simulation vectors while running at a 16.7-MHz clock rate with 94 available signal channels. The system is used during the simulation of an electronic system design to model actual IC components with components modeled in software. Functional verification on prototypes of application-specific ICs can also be performed. The part evaluation module is priced at $40,000. **Daisy Systems,** 700 E Middlefield Rd, Mountain View, CA 94043.

Circle 141

Logic-synthesis tool makes testable implementations

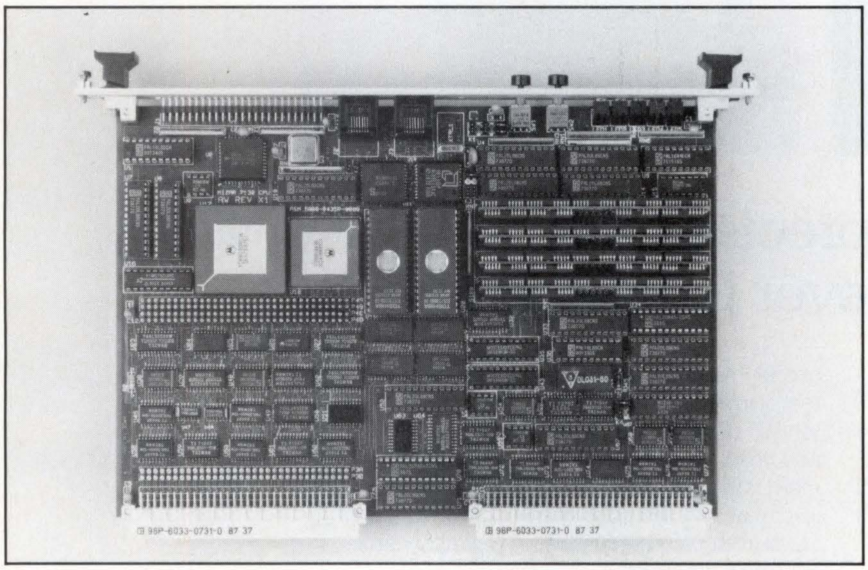
An Electronic Design Automation system for application-specific ICs, Silcsyn is a logic-synthesis-based tool that can automatically generate gate-level structural implementations from high-level behavioral descriptions. The system can be used for any semicustom design and can synthesize both combinational and sequential logic, can handle synchronous and asynchronous timing, and can accommodate single or multiple clock systems. And it doesn't depend on programmable logic arrays or require a restrictive circuit architecture. The price of the system is $40,000. **Silc Technologies,** 34 Third Ave, Burlington, MA 01803.

Circle 142

Computers and Computer Subsystems

68030 CPU achieves zero wait states at 25 MHz

Based on the Motorola 68030 CPU, the MZ 7130 single-board computer reduces critical wait states to zero at up to 25 MHz. With static RAM options, subzero wait-state performance is achieved.



Memory includes 4 Mbytes of dual-ported dynamic RAM, up to 3 Mbytes of SRAM, up to 1 Mbyte of EPROM, a 16-kbyte cache and a VME subsystem bus memory expansion interface. An optional 68881 or 68882 floating-point coprocessor is offered, while I/O facilities include two RS-232 ports, a high-speed small computer system interface, a time-of-day clock with battery backup, and additional serial and parallel I/O expansion capabilities.

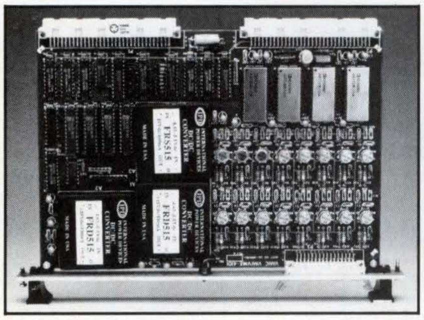
An interrupt handler, an interrupt generator and mailbox interrupts are provided, as well as a 32-bit master/slave interface to the VMEbus with full system controller functions including four-level arbitration. With 4 Mbytes of DRAM, the unit is priced at $5,995.

Mizar, 1419 Dunn Dr, Carrollton, TX 75006. **Circle 143**

Intelligent I/O module houses VMEbus board

A user-defined I/O module constructed around a 68000 processor provides a 110- × 145-mm design area on the I/OM-1 VMEbus board. The device also acts as a slave module with mailbox interrupts, while the user design area provides a development breadboard for prototype design. Memory includes 512 kbytes of dynamic dual-ported RAM and up to 128 kbytes of EPROM. There are two software packages available that support the developer, the EMSbug, the Debug Monitor and a 68000 OS-9 kernel with a character file manager module. **MCP Electronics,** 26-32 Rosemont Rd, Alperton, Wembley, Mddx, UK.

Circle 144



Analog output board drives 16 channels at 10 mA

A high-current drive analog output board, the VMIVME-4100 features built-in test support logic. Limited to 5 mA per channel, the board will drive up to 16 channels of analog output simultaneously at a maximum load current of 10 mA. Each channel features a 12-bit digital-to-analog converter with dedicated buffered outputs and a 10-μs settling time. Price is $3,295. **VME Microsystems,** 12090 S Memorial Pkwy, Huntsville, AL 35803. **Circle 145**

VMEbus CPU module executes at 10 MHz

Built around the Signetics 68070 CPU, the SAC-700 is a 16-bit industrial VMEbus CPU module designed for a variety of control applications. The module offers up to 2 Mbytes of battery-backed CMOS RAM, with another 2 Mbytes residing in two JEDEC EPROMs. Advanced bus timing lets the board execute at 10 MHz. The board features a memory-management unit, a two-channel direct memory access controller, five multimode timers, a watchdog device, three RS-232/-422 ports and a 16-bit parallel I/O port. Prices start at $590. **American Eltec,** 569 S Marengo Ave, Pasadena, CA 91101.

Circle 146

Mil-spec computer offers 32-bit memory bus

Developed for the military market, the SECS 80/386 is a 32-bit, 80386-based microcomputer engine with a 80387 numeric coprocessor. The three-card family is made up of the CPU, an EPROM/static RAM support memory card and a 2-Mbyte expansion dynamic RAM card. The cards bring a nondevelopment item solution to high-end computational needs via a 32-bit local memory bus, which facilitates data transfers between the CPU and its companion memory cards. **Titan,** 20151 Nordhoff St, Chatsworth, CA 91311.

Circle 147

Application accelerator delivers 40 MFlops

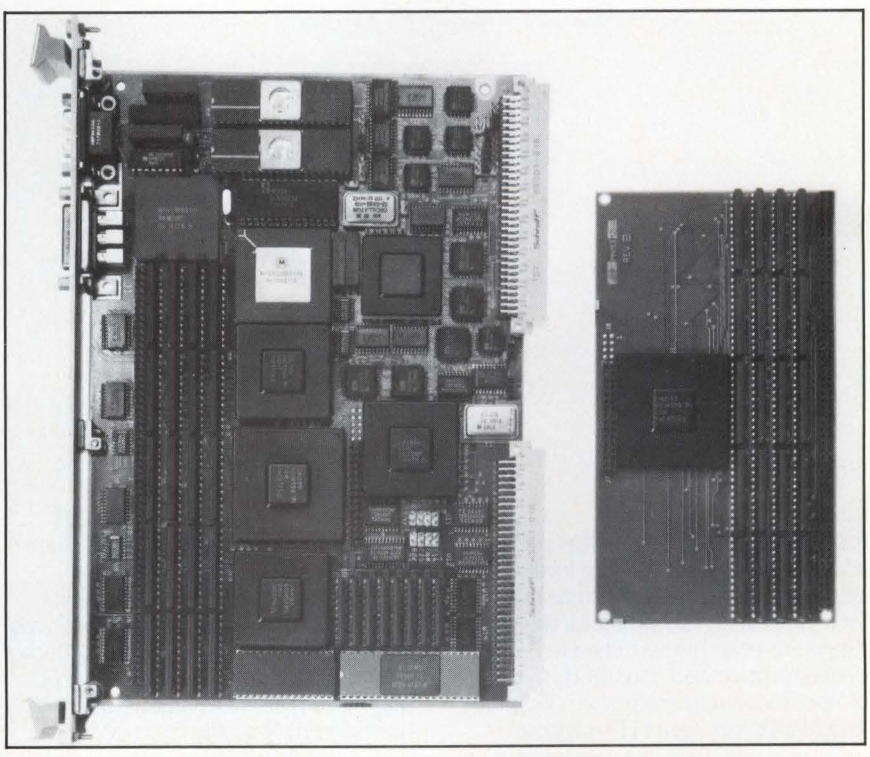
Plugging directly into a MicroVAX, the MAP-4000 single-board application accelerator provides 40 MFlops of single-precision (32-bit), and 20 MFlops of double-precision (64-bit) performance. According to the manufacturer, the board delivers anywhere from a 10-times speedup on general compiled code to a 100-times improvement on computationally intensive vector and matrix arithmetic. The application accelerator comes with 2 Mbytes of memory, expandable to 256 Mbytes. The device also includes a set of integer, byte and bit manipulation instructions that run at up to 40 Mops. **CSPI,** 40 Linnell Cir, Billerica, MA 01821.

Circle 148

Graphics and Imaging

VMEbus graphics card achieves 1,280- × 1,024-pixel resolution

Combining VLSI circuitry with surface-mount technology, the GCS-4700 graphics engine provides a resolution of 1,280 × 1,024 pixels while occupying a single VME slot. The device off-loads the graphics pro-



New high performance PC-based emulators from HP.

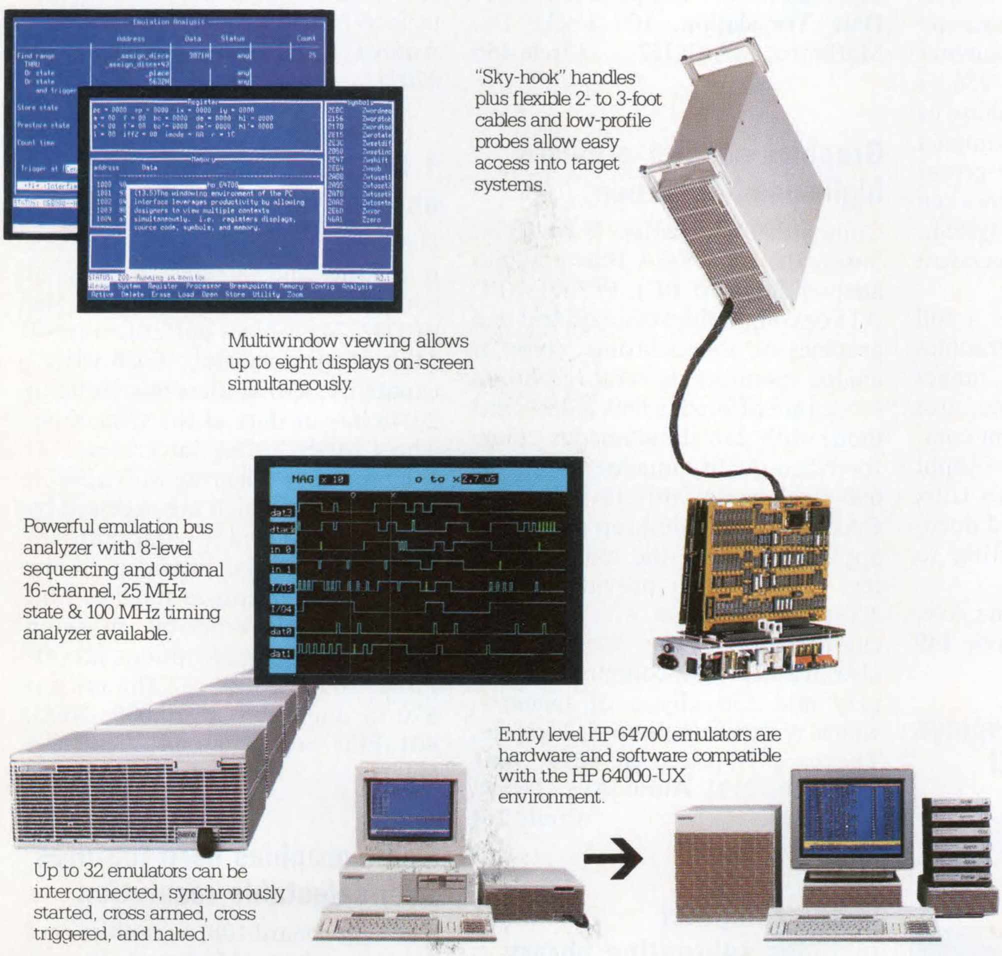
Introducing the HP 64700 Series emulators. Low-cost, entry-level, PC-based emulators with features you won't find with any others in the price range–or even higher. The HP 64700s deliver unmatched capability, ease-of-use, measurement power, flexibility, and reliability . . . plus HP support.

While the HP 64700s are tailored to meet the needs of individual engineers and small design teams, they'll perform equally well for large teams working on complex projects.

The rapidly expanding family of HP 64700 emulators provide real-time, transparent emulation at full processor speeds with no wait states. The PC user interface gives a new meaning to the term "friendly" with features like multiple windows, single-letter keystroke command entry, access to symbols for powerful debugging capability, timing diagrams, and on, and on, and on. The experienced user as well as the beginner will appreciate how easy these emulators are to work with.

In addition to the features shown above, there are lots of others that put the HP 64700s in a class by themselves. To name a few: function with IBM-PC, HP Vectra and compatibles, RS-422 high-speed serial

You could spend a lot more and get a lot less.



"Sky-hook" handles plus flexible 2- to 3-foot cables and low-profile probes allow easy access into target systems.

Multiwindow viewing allows up to eight displays on-screen simultaneously.

Powerful emulation bus analyzer with 8-level sequencing and optional 16-channel, 25 MHz state & 100 MHz timing analyzer available.

Entry level HP 64700 emulators are hardware and software compatible with the HP 64000-UX environment.

Up to 32 emulators can be interconnected, synchronously started, cross armed, cross triggered, and halted.

interface for superior download and upload speed, code coverage analysis for efficient software testing and design, host-independent portability, and compatibility with popular absolute file formats such as Tektronix and Intel hexadecimal and Motorola S record.

Once you get your hands on an HP 64700 emulator, you'll agree that this is the new standard in the field. Especially at a starting price of $8,900.

Free demo disc.

For a free demo disc that gives you the "hands-on" feel for HP 64700 Series capabilities, call HP at 1-800-752-0900 ext. 786E, or mail the attached business reply card.

HEWLETT PACKARD

cessing from the host via a Motorola 68020 microprocessor that interprets graphics commands, handles display list functions and executes graphics control software commands.

Six custom-designed VLSI gate arrays control functions such as vector drawing, polygon fill, character drawing, pixel manipulation, pan, scale and rotate, while a DSP32 processor executes floating-point operations and matrix processing duties.

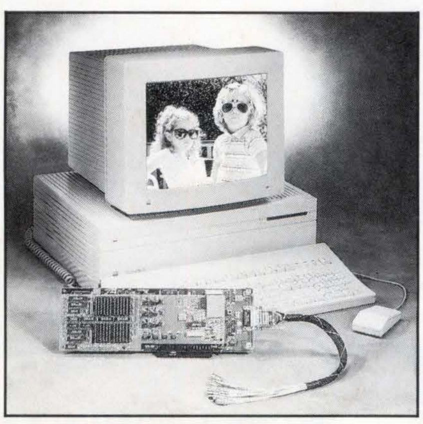
The engine also has eight pixel planes—four on the main board and four more on the attached daughter board—for displaying up to 256 simultaneous colors from a palette of 16.7 million. Because of its compact size (8.4 × 10.5 in.) and low power consumption, up to four engines can be installed in a single VME system, allowing for multiple independent graphics workstations.

Resident on the boards is a full complement of computer graphics interface functionality that ranges from primitives such as lines, arcs and fill, to high-order segment commands. Provided is input/output driver support for Motorola's Unix SYSV/68, as well as tools and documentation to assist in porting to other operating systems.

Calcomp, 2411 W La Palma Ave, Anaheim, CA 92801. **Circle 149**

Color frame grabber displays images on Macintosh II

Geared for applications in animation, electronic publishing, film colorization and video production, ColorCapture is a plug-in color frame-grabber board that captures and displays live-motion video images on the Macintosh II. Images are displayed in a 640- × 480-pixel format from a palette of 32,768 colors. The board fits into any Macintosh expansion slot; cables directly to video cameras, VCRs or electronic still-video equipment; and features an external trigger, a zoom-pan-scroll controller and a memory plane for merging text or drawn images with the captured frame. The price is $2,995. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Circle 150**

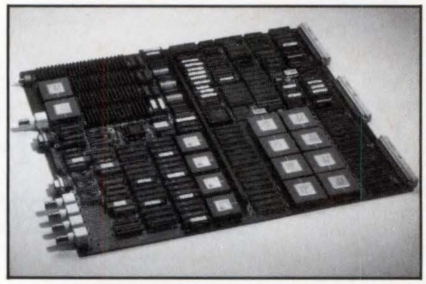


Graphics adapter provides high-speed operation

Compatible with either 8- or 16-bit buses, the AST-VGA Plus graphics adapter for IBM PCs, PC XTs, PC ATs or compatibles displays text and graphics on monochrome, color or analog monitors. Several resolution modes are offered: a 640- × 480-pixel mode with 256 simultaneous colors for video-quality images, an 800- × 600-pixel mode with 16 colors for CAD/CAM and desktop publishing applications, and the monochrome text mode, which provides 720- × 400-pixel resolution with a 9- × 16-character box. The ¾-size board also features 132-column text display and 256 kbytes of memory, which is expandable to 512 kbytes. The card is priced at $599. **AST Research,** 2121 Alton Ave, Irvine, CA 92714. **Circle 151**

Image computer includes subroutine library

The ICS-400 image computer for the Sun Series 3 and 4 workstations contains an extensive C-callable subroutine library for image processing and fonts. A single 9U-sized VMEbus-compatible Eurocard, the board has a 100-Mips architecture that includes parallel processing, multiple instruction/multiple data design and proprietary pixel cache controllers implemented with semicustom gate arrays. Real-time image-acquisition



and display capabilities feature resolutions of up to 1,024 × 1,024 pixels and RGB acquisition and display interfaces. Prices begin at $10,900. **Androx,** 150 Royall St, Canton, MA 02021. **Circle 152**

1 Mbit of memory resides on dual-port graphics buffer

Designed for high-speed graphics processing and targeted at personal computers and workstations, the uPD42274 graphics buffer features 1 Mbit of memory and "flash write" capability, letting users rewrite up to 2,048 bits of data at the same time. The CMOS buffer integrates a 1-Mbit memory cell array with a 2-kbit data register, which are accessed by using a RAM and a serial port. Information can be provided to the RAM in increments as small as 1 bit using the write-per-bit masking feature. Two speed options are offered: 100 and 120 ns. The price is $70 in quantities of 10,000. **NEC,** 401 Ellis St, Mountain View, CA 94039. **Circle 153**

Color graphics card features user-selectable resolution

The Colorboard 108, a graphics card for use with the Macintosh II, provides a simultaneous display of 256 colors from a palette of 16.7 million colors. The board can control user-selectable display densities of 1,024 × 768 pixels, 800 × 600 pixels or 640 × 480 pixels at video rates of 64, 40 and 30.24 MHz, respectively. The card allows the full-page display on 16- or 19-in. monitors for desktop publishing. The price is $1,495. **Rasterops,** 10161 Bubb Rd, Cupertino, CA 95014. **Circle 154**

Video capture board interfaces with PS/2

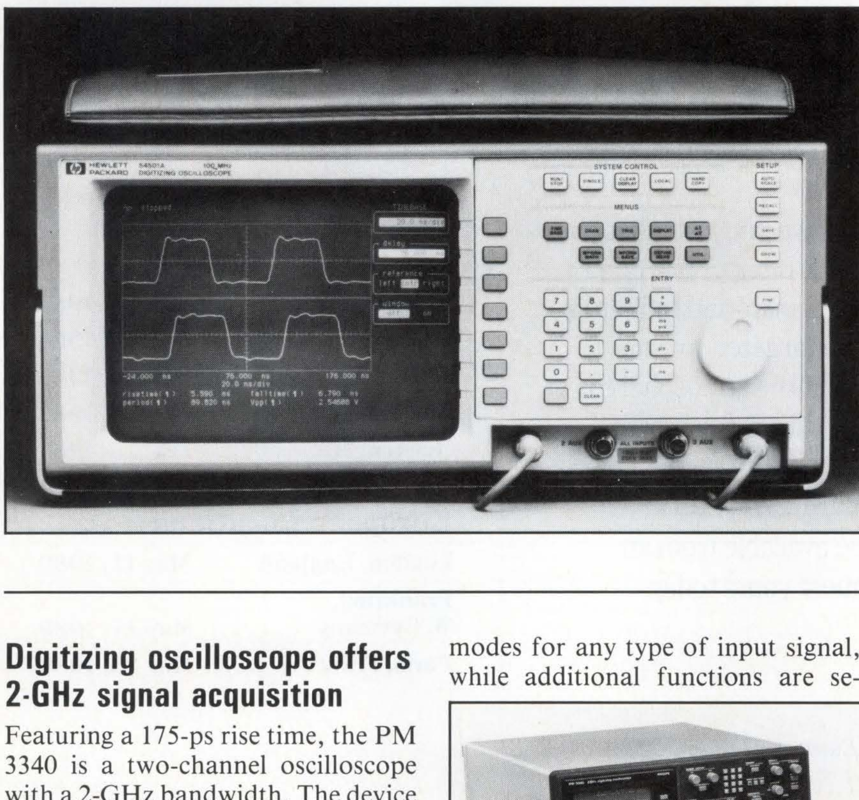
Taking a composite video signal from a VCR or video camera, the RAMCorder Video Capture Board digitizes images for storage and manipulation by an IBM PC or Personal System/2. A captured frame can be displayed on a Video Graphics Array monitor in several resolutions ranging from 640×480 pixels with 16 shades of gray to 320×200 pixels in 256 colors. A color television with video input or an analog multisynch monitor can be connected to the board to display the image in real-time mode. Once captured, the image can be saved in various file formats for later use within specific applications. Retail price of the video capture board is $749. **Sigma Designs,** 46501 Landing Pkwy, Freemont, CA 94538.

Circle 155

Testing and Manufacturing

Four-channel digitizing oscilloscope features 100-MHz bandwidth

A general-purpose benchtop oscilloscope, the HP 54501A offers 16 pulse-parameter measurements, advanced logic triggering and an IEEE-488 interface for programmable data acquisition and control. With the device's measurement-limit test capability, upper and lower limits can be set for any of the instrument's automatic measurements, allowing unattended operation. If preset limits are exceeded, the oscilloscope will transfer all measurement results to an external printer or controller.



The user interface has been simplified so that most adjustments are made with the front-panel knob. In addition, automatic measurements are made with a single keystroke, and the number of menu levels has been reduced. Dual time-base windowing lets users define part of a waveform for magnification.

A 16-channel, 16-bit digital-to-analog converter provides the internal voltage references for functions such as offset, vernier, trigger-level and dc-calibration signals, while a 25,000-device time-base IC provides all of the instrument's time-base circuitry. Other key specifications are 5-mV sensitivity, 8-bit vertical resolution and 10-Msample/s digitizing rate. List price is $3,465.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 19310.

Circle 156

Digitizing oscilloscope offers 2-GHz signal acquisition

Featuring a 175-ps rise time, the PM 3340 is a two-channel oscilloscope with a 2-GHz bandwidth. The device has a 10-bit vertical axis as well as 512 measuring points along the time axis. A triggering facility on the instrument automatically selects the most suitable of the three trigger modes for any type of input signal, while additional functions are selected through the use of soft keys, with on-screen menus to show available options. A number of dedicated processing modes are featured, such as an "eye-pattern" mode for testing digital communication signals. The unit is priced at $16,000.

Philips, 5600 MD Eindhoven, The Netherlands. **Circle 157**

John Fluke Mfg, PO Box C9090, Everett, WA 98206. **Circle 158**

Multitasking system tests up to 12 SCSI peripherals

The SDS1000 is a small computer system interface (SCSI) peripheral tester for quality assurance, evaluation and incoming inspection applications. Up to 12 SCSI peripherals can be tested concurrently in any combination by the multitasking system, with each test started, stopped and watched via process-monitoring displays invoked by the operator. Data reduction and documentation functions make it possible to run, interpret and log test results without operator intervention. A standard library of tests can be used directly or strung together, while a C compiler allows the combination of user-written test code and library elements. Prices start at $22,450. **Adaptec,** 691 S Milpitas Blvd, Milpitas, CA 95035. **Circle 159**

Portable oscilloscope has 20-MHz storage capability

The DSS 5020A portable oscilloscope has a 1-Msample/s digitizer with a sine interpolation mode that allows waveform storage of frequencies up to 400 kHz. Along with a 20-MHz storage capability, the device features auto focus, high-frequency reject and a video synch separator. A channel 1 signal output provides 50 mV/div to a 50-Ω load, enabling the observation of miniscule waveforms. A jitter-cancel circuit stabilizes the display by eliminating the instability caused by nonsynchronization of the sample clock and trigger signals. The device weighs 15 lb and is priced at $1,750. **Kikusui International,** 17819 S Figueroa St, Gardena, CA 90248. **Circle 160**

Trademark Information

UNIX is a registered trademark of AT&T Bell Laboratories.

PAL and PALASM are registered trademarks of Monolithic Memories Inc.

GEOMETRY ENGINE is a trademark of Silicon Graphics Inc.

APLEX and UTX/32 are trademarks of Gould Inc.

COMPUTER DESIGN / SALES OFFICES

EXECUTIVE OFFICE: P.O. Box 417, 119 Russell St, Littleton, MA 01460-0417
(617) 486-9501 Telex: 883436 ELN: 62649490

PUBLISHER, David L. Allen
ASSOCIATE PUBLISHER, John C. Miklosz
MARKETING SERVICES MANAGER, Mary M. Gregory
SALES PROMOTION AND RESEARCH MANAGER, Judy Leger
ADMINISTRATIVE ASSISTANT, Tina LePage
ADVERTISING COORDINATOR, Shari Hasche
POSTCARDS/SYSTEM SHOWCASE/RECRUITMENT, Shirley Lessard, Barbara Kovalchek
CIRCULATION DIRECTOR, Bob Dromgoole
LIST RENTAL, Bruce McCarthy
ASSISTANT CIRCULATION MANAGER, George Andrew

NEW ENGLAND/UPSTATE NEW YORK/E. CANADA
Kevin Callahan
KMC Inc.
P.O. Box 605
North Scituate, MA 02060
Tel: (617) 545-6603

NEW YORK/NEW JERSEY/ PENNSYLVANIA/DELAWARE/MARYLAND
Neil Versen
Park 80 West, Plaza Two
Saddle Brook, NJ 07662
Tel: (201) 845-0800
Fax: (201) 845-6275

MIDWEST/ONTARIO, CANADA
Robert D. Wentz
75 East Wacker Drive
Chicago, IL 60601
Tel: (312) 236-2537

SOUTHWEST/SOUTHEAST
Eric Jeter
3050 Post Oak Blvd.
Houston, TX 77056
Tel: (713) 621-9720
Fax: (713) 965-6285

SOUTHERN CALIFORNIA/COLORADO
Tom Boris, Greg Cruse
2082 SE Bristol, Suite 216
Santa Ana, CA 92707
Tel: (714) 756-0681
Fax: (714) 756-0621

NORTHERN CALIFORNIA
Tom Boris, John Sly,
Bill Cooper
1000 Elwell Court, Suite 234
Palo Alto, CA 94303
Tel: (415) 965-4334
Fax: (415) 965-0255

OREGON
Tom Boris
2082 SE Bristol, Suite 216
Santa Ana, CA 92707
Tel: (714) 756-0681
Fax: (714) 756-0621

WASHINGTON
John Sly
1000 Elwell Court, Suite 234
Palo Alto, CA 94303
Tel: (415) 965-4334
Fax: (415) 965-0255

U.K.
David Round
69 Imperial Way
Croydon, Surrey
CRO 4RR, England
Tel: 01 686 7655
Telex: 938420
Fax: 01 688 2134

SCANDINAVIA
David Betham-Rogers
PennWell House
39 George St, Richmond Upon Thames
Surrey TW9 1HY England
Tel: 01 948 7866 Telex: 919775 PENWEL G

FRANCE, BELGIUM, S. SWITZERLAND, SPAIN AND THE NETHERLANDS
Daniel R. Bernard
247, Rue Saint Jacques
75005 Paris France
Tel: (1) 43 54 55 35 Telex: 214235F MISIVZ
Attn: Missitex: PENNWELL

W. GERMANY, AUSTRIA, N. SWITZERLAND AND EASTERN EUROPE
Johann Bylek
Verlagsburo Johann Bylek
Stockaeckerring 63
D-8011 Kirchheim/Munchen
Federal Republic of Germany
Tel: 089 903 88 06
Telex: 529355 vbb d

ITALY
Luigi Rancati
Rancati Advertising
Milano San Felice Torre 5
20090 Segrate ITALY
Tel: 2 753-1445
Telex: 328601 RANCAD I

JAPAN
Sumio Oka
International Media Representatives, Ltd.
2-29 Toronomon-Chome
Minato-ku, Tokyo 105 Japan
Tel: 3-502-3806 Telex: J22633 MEDIAREP

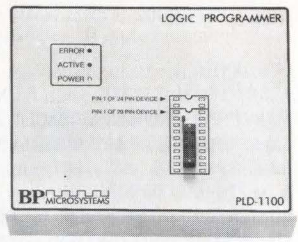
SOUTHEAST ASIA
Seavex, Ltd.
Anne Goh-Taylor
400 Orchard Rd, #10-01
Singapore 0923
Republic of Singapore
Tel: 734-9790 Telex: 35539 SEAVEX RS

Jay G. Seo
Doobee International, Ltd.
Centre Building (Byulgwan)
1-11 Jeong-dong, Choong-ku
CPO Box 4557
Seoul, Korea
Tel: 776-2096/8 Telex: 27117 DOOBEES

SYSTEM SHOWCASE

Circle 220 for rates and information, or call: Shirley Lessard or Barbara Kovalchek 800-225-0556. In Massachusetts 617-486-9501.

UNIVERSAL LOGIC PROGRAMMER



- PROGRAMS, READS, DUPLICATES, TESTS AND SECURES HUNDREDS OF 20- AND 24-PIN LOGIC DEVICES
- 23 UNIVERSAL PIN DRIVERS WITH INDEPENDENT DAC, ADC & SLEW FUNCTIONS PROGRAM ALMOST ANY LOGIC DEVICE
- MENU DRIVEN OPERATION IS EASY TO LEARN AND QUICK TO OPERATE
- CONNECTS TO ANY IBM COMPATIBLE COMPUTER VIA PARALLEL PRINTER PORT
- EDITS FUSE DATA & TEST VECTORS WITH FULL SCREEN EDITOR
- TESTS WITH VECTORS & SECURES AFTER PROGRAMMING
- SUPPORTS ALL POPULAR PLD DEVELEPOMENT SOFTWARE
- ONLINE HELP FUNCTION
- ONE YEAR WARRANTY
- SELF CALIBRATING
- SAME DAY SHIPMENT
- JEDEC FILE INPUT & OUTPUT
- TOLL-FREE TECH SUPPORT
- 30 DAY MONEY BACK GUARANTEE
- UPDATABLE VIA FLOPPY
- GOLD TEXTOOL ZIF IC SOCKET
- EPROM PROGRAMMERS ALSO
- JUST $798

CALL FOR FREE DEMO DISK OR INFO 800/225-2102

BP MICROSYSTEMS

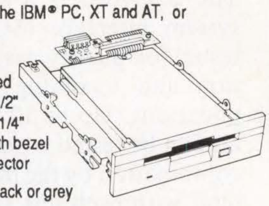
10681 HADDINGTON #190 HOUSTON, TX 77043
713/461-9430 TLX: 1561477 FAX: 713/461-7413

CIRCLE NO. 221

3 1/2" Drives With Adapters For 5 1/4" Slots

Models MF353B (1 MB) and MF355B (2 MB/1 MB) are 3 1/2" flexible disk drives with built-on mounting frames and connectors that enable installation into standard 5 1/4" PC system slots.

- Easily installed into the IBM® PC, XT and AT, or compatible systems
- Adapter unit comes completely assembled and consists of a 3 1/2" flexible disk drive, 5 1/4" mounting bracket with bezel and card edge connector
- Comes with either black or grey bezels



For more information write or call:
Mitsubishi Electronics America, Inc., Computer Peripherals Division, 991 Knox Street, Torrance, CA 90502
(213) 515-3993, ext. 382.

MITSUBISHI ELECTRONICS

CIRCLE NO. 222

target over 30 microprocessors

CROSS ASSEMBLERS

Universal Linker, Librarian

micro VAX, VAX VMS, PC/MS DOS

- Powerful macros
- Relocatable or absolute code
- Binary or ASCII Hex file output
- Fast Version 2.2
- Universal Linker for all targets
- Conditional assembly
- Prompt delivery

ENERTEC INC, 19 Jenkins Avenue
Lansdale, PA 19446 • 215-362-0966

CIRCLE NO. 223

SOFTWARE VERSION CONTROL

The **POLYTRON** Version Control System (PVCS) provides precise & flexible configuration management for software development projects on Personal Computers, PC Lans and VAX minicomputers, including:

- Storage and retrieval of multiple revisions of source code.
- Maintenance of separate lines of development using branching.
- Merging of simultaneous changes.
- Modules can be reviewed by their own revision number, system version number, or specified date.
- Efficient disk storage. PVCS uses a very intelligent difference detection technique that minimizes the amount of disk space required to store a new version.

Personal PVCS — Offers most of the power and flexibility of Corporate PVCS. **$149**

Corporate PVCS — Offers features to maintain source code of very large and complex projects that may involve multiple programmers. **$395**

Network PVCS — Extends Corporate PVCS to use on networks. File locking and security levels can be tailored for each project. Call (503) 645-1150 for pricing on licenses for more than 5 stations. **$995**

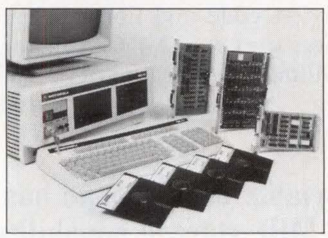
VAX PVCS — Call for pricing

Requires DOS 2.0 or higher. Compatible with the IBM PC, XT, AT and other MS-DOS PC's. Works with any language.

TO ORDER: VISA/MC **1-800-547-4000.**
Dept. CPD Oregon and outside US call (503) 645-1150.
Send checks, P.O.'s to: **POLYTRON** Corporation, 1700 NW 167th Place, Dept. CPD, Beaverton, OR 97006.

CIRCLE NO. 224

IEEE-488 for VMEbus & MULTIBUS



Hardware Options — High-speed DMA or low cost programmed I/O
Software Support — UNIX, PDOS, MTOS, VERSAdos, Aegis

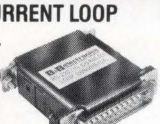
NATIONAL INSTRUMENTS™
The Software is the Instrument™

Call for FREE Catalog
512/250-9119 or 800/531-4742

CIRCLE NO. 225

SAME-DAY SHIPMENT! MONEY-BACK GUARANTEE!

"RS-232C TO CURRENT LOOP BI-DIRECTIONAL CONVERTER"
Model 232CL2
only **$39.95**



Interface your RS-232 port to existing current loop system. Model 232CL2 couples and isolates Transmit and Receive Data through high speed optical isolators. Powered from pins 4, 5, 6, 8 and 20 on the RS-232 side; one pin must be high, one must be low.

No power required if current loop port is active. Model 232PS-12V DC Power Supply required if current loop port is passive; only $14.95.

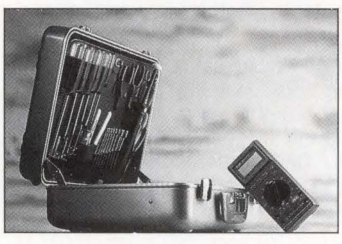
Order direct from manufacturer *TODAY* and *SAVE!**

Request your FREE copy of B & B ELECTRONICS' Catalog which lists a host of interface and monitoring equipment for RS-232 ports.

*Terms: Visa, MC, cash orders postpaid; P.O.'s from qualified rated firms accepted. IL residents add 6¼% sales tax.

B&B electronics MANUFACTURING COMPANY
1514G Boyce Memorial Drive • P.O. Box 1040
Ottawa, IL 61350 • **Phone: 815-434-0846**

CIRCLE NO. 226



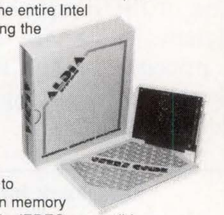
ELECTRONICS TOOLS AND TEST EQUIPMENT

Color illustrated 210-page catalog from Specialized Products Company details an extensive selection of electronic tool kits, test equipment, telecommunications equipment and electronic production aids. Indexed catalog shows digital multimeters, breakout boxes, hand tools, soldering equipment and more—all with specifications and prices. **Specialized Products Co.,** 2117 W. Walnut Hill Ln., Irving, TX 75038. Phone (800) 527-5018.

SPECIALIZED PRODUCTS CO.
CIRCLE NO. 227

IT'S EASY TO LOCATE ROM SOFTWARE SUPPORT

PC-LOCATE: Produce ROM-able code from your "exe" files. PC-LOCATE assigns physical addresses to the re-locatable image based on user inputs. PC-LOCATE supports the entire Intel processor family including the 8086, 8088, 80186, 80188 and 80286.



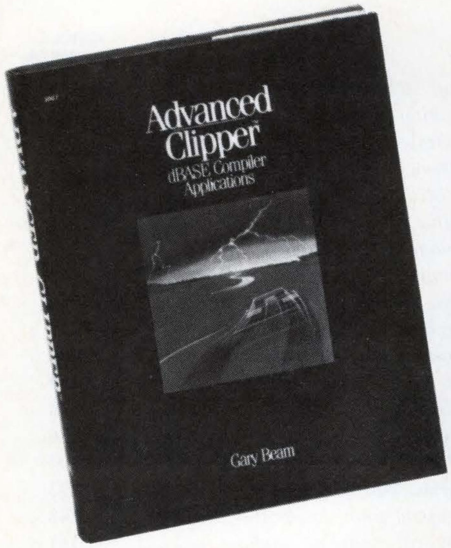
PC-PROMPAK: A PROM/ROM expansion board for IBM and IBM-compatible computers. PC-PROMPAK provides up to 384 Kbytes of expansion memory and supports most 28-pin JEDEC compatible devices.

PC-ROMDRIVE: Create a "Diskless PC" that can include MS-DOS and your application program. Program execution can be automatically invoked through the use of an "autoexec.bat" file.

ALDIA SYSTEMS INC.

P.O. BOX 37634 PHOENIX, AZ. 85069
(602) 866-1786

CIRCLE NO. 228



Advanced Clipper™
dBASE Compiler Applications
by GARY BEAM
Clipper expert Gary Beam has done it again. Using a comprehensive business application throughout the book, Beam demonstrates important database programming techniques: advanced user-defined functions, multiple-file data entry, multi-screen usage, data backup and archive methods, and program debugging. Complete program listings are provided (or are available on disk).

Experienced Clipper users will especially appreciate the advanced techniques—like data validation and relative addressing—which have never been published before in any form.
$17.95 **Circle 241**

SQL®: The Structured Query Language
by Dr. CAROLYN J. HURSCH and Dr. JACK L. HURSCH
Recently a need has developed for a flexible database language that is user-friendly enough for the casual user, yet powerful enough for the programmer and applications builder. SQL has been developed by IBM to fill that need.

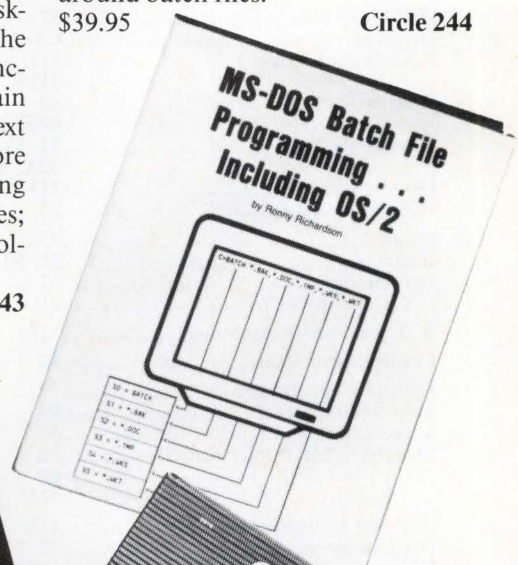
This book presents the complete picture of SQL. Although aimed toward computer science professionals, its hands-on approach, with many examples of each concept, makes the book equally appropriate for database operators who simply want to understand and use SQL.
$24.95 **Circle 242**

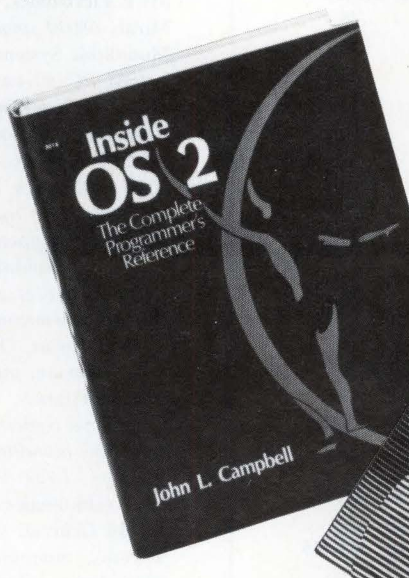
Inside OS/2: The Complete Programmer's Reference
by JOHN CAMPBELL
John Campbell has created the most complete and technically precise book available on OS/2, MicroSoft's new operating system for 80286- and 80386-based machines (such as IBM®'s Personal System/2 line).

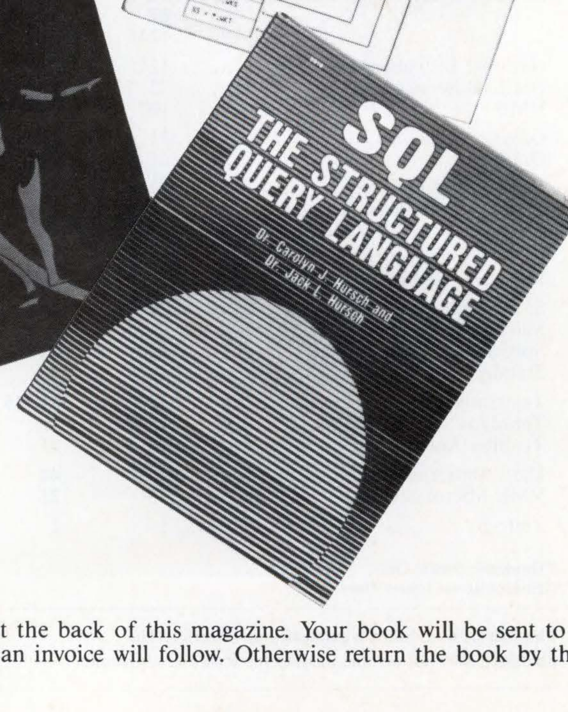
Campbell covers OS/2 fundamentals: entering commands, copying diskettes, changing drives, clearing the screen, and using control key functions. Every chapter recaps the main points in a useful summary. In the next section readers can move on to more complex aspects of OS/2: working with files, disks, and other devices; creating and editing files; and controlling the graphic display.
$25.95 **Circle 243**

MS-DOS Batch File Programming . . . Including OS/2
by RONNY RICHARDSON
Richardson begins with the simplest batch files, assuming readers have no previous experience. Then, progressively more complex batch files are explained. By the end of the book, readers will be able to implement even the most difficult batch files, and will thoroughly understand the whole process.

Special attention is given to the most important batch file: AUTOEXEC.BAT, and to the building of complete systems around batch files. Readers will easily follow along as the author explains how to build a menu system and a document archival system around batch files.
$39.95 **Circle 244**







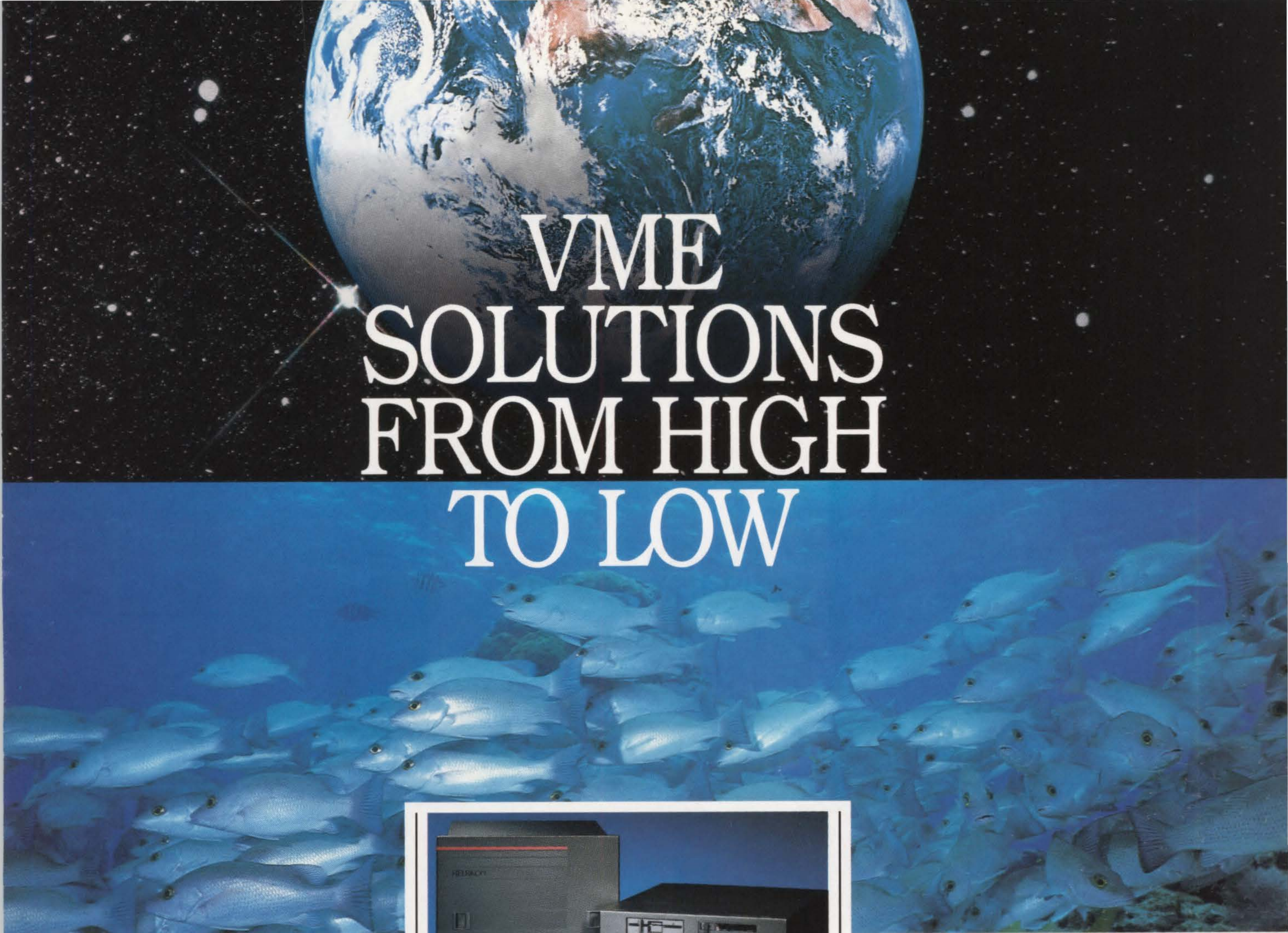
HOW TO ORDER:
15-DAY FREE EXAMINATION
(U.S. AND CANADA ONLY)
Simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine. Your book will be sent to you for your **15-day free trial**. If you are satisfied keep the book and an invoice will follow. Otherwise return the book by the end of the 15-day period and owe nothing.

ADVERTISERS' INDEX

***Domestic Issues Only**
****International Issues Only**

The Advertisers' Index is published as a service. The publisher does not assume liability for errors or omission.

SYSTEM PRODUCTS INDEX



VME SOLUTIONS FROM HIGH TO LOW

The Power to Serve. Whatever your application, high or low-end, Heurikon has the VME power to drive it. From UNIX™ to real-time. From satellite communications to oceanographic research. We can solve the problem.

A New Dimension in Processors. Get into the fast lane with Heurikon's 16 or 32-bit microcomputers. Your choice of 68000-68030 or NS32532. Single boards or systems. Off the shelf or customized. With unmatched support from day one.

Potent Development Tools. Slash your development time. Choose from multiple networked or bus-based environments. Wind River VxWorks™ and Heurikon BusLink™. SUN, VAX and other hosts. Plus solid in-house support for UNIX V.3 and VRTX® or OS-9™ real-time operating systems ensures the integrity of your design.

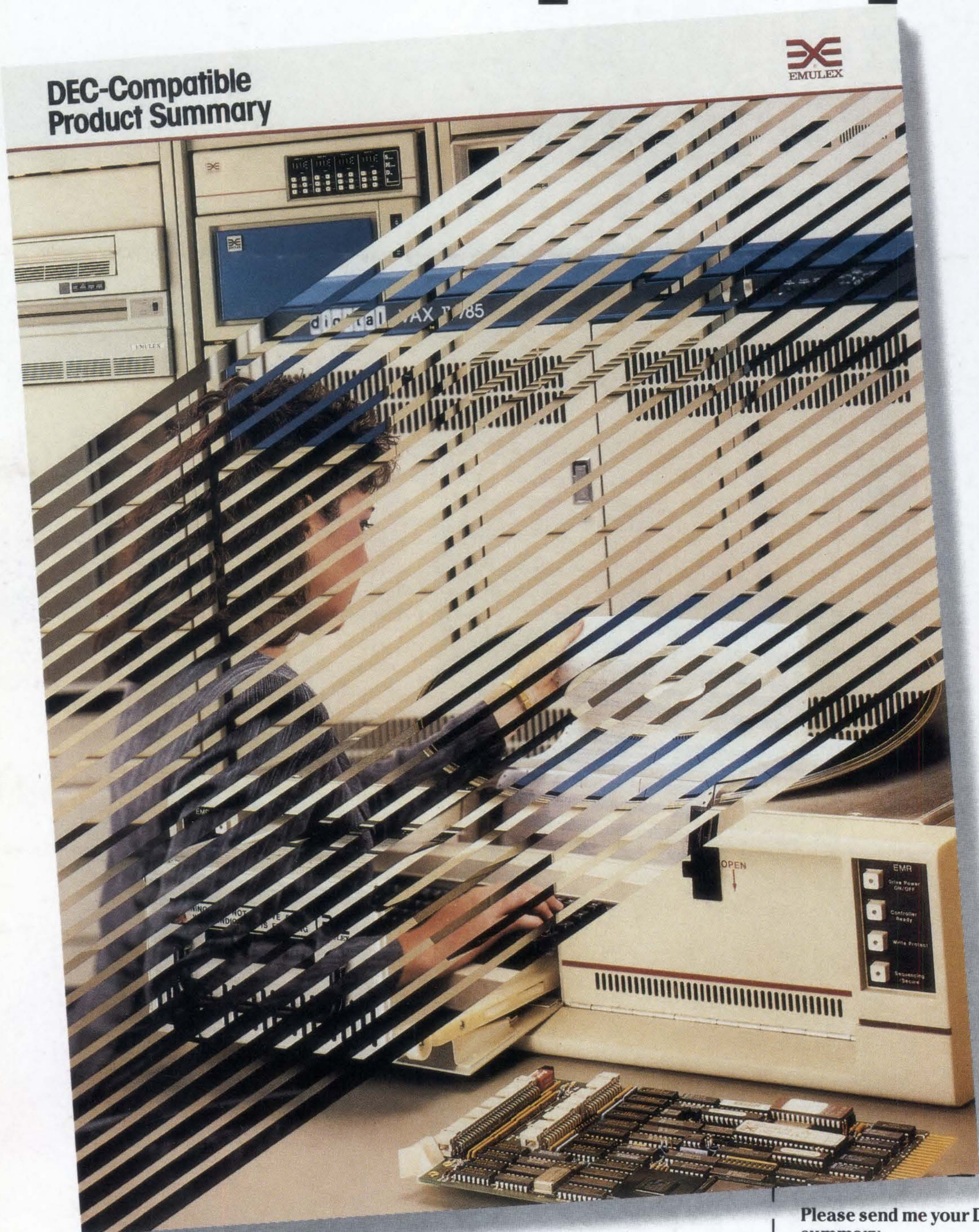
From high to low, power your application with VME from Heurikon. Call us today.

1·800·356·9602
ext. #501

Heurikon Corporation
3201 Latham Dr., Madison, WI 53713
TLX: 469532 FAX: 608-251-1076

HEURIKON CORP.

The real catalog of DEC-compatible products.



Are you an OEM working with DEC systems?

An in-house integrator looking for the highest possible performance?

Or simply a sophisticated end-user searching for a higher performance alternative than DEC offers?

Then this one's for you.

Spring '88 Edition

Whether you need a controller for 5¼, 8, or 14-inch drives. Or for optical drives. Or for ½-inch tapes. For LSI-11s, PDP-11s, MicroVAX's or VAX's; for MSCP or other emulations.

They're all here—from boards to complete subsystems, along with host adapters, communications multiplexers, and embedded drive kits.

This 40-page book of best sellers from the world's largest supplier of DEC-compatible products is free while supplies last. For a copy, call toll-free (800) EMULEX 3 or (714) 662-5600 in California. Emulex Corporation, 3545 Harbor Blvd., Costa Mesa, CA 92626.

EMULEX

CD 7/88

Please send me your DEC-compatible product summary.

Name ______________________

Company ______________ Title ______________

Street ______________________

City ______________ State ________ Zip ________

Regional Offices: Anaheim, CA (714) 385-1685; Atlanta, GA (404) 587-3610; Burlington, MA (617) 229-8880; Chicago, IL (312) 490-0050; Dublin, CA (415) 829-1170; Teaneck, NJ (201) 836-3717; Washington, DC (703) 264-0670. **International Offices:** Bracknell 344-484234; Munich 89-3608020; North Sydney 2-957-1669; Paris 134-65-9191; Tokyo 3-234-8951; Toronto (416) 673-1211. DEC, LSI-11, PDP-11, MicroVAX and VAX are trademarks of Digital Equipment Corporation.

CIRCLE NO. 47