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JANUARY 1985

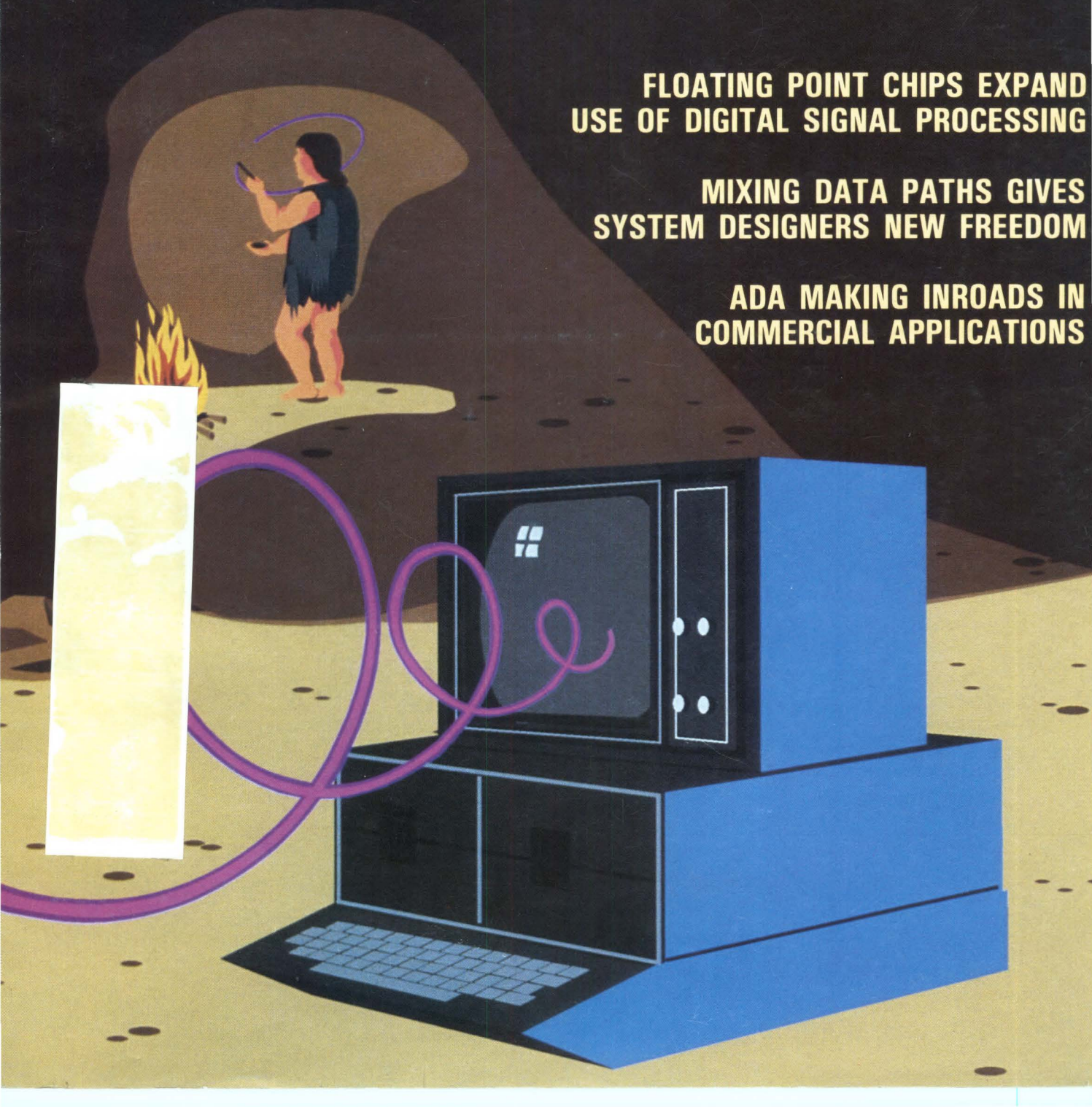
COMPUTER DESIGN

TECHNOLOGY FOR ADVANCED WORKSTATIONS

FLOATING POINT CHIPS EXPAND USE OF DIGITAL SIGNAL PROCESSING

MIXING DATA PATHS GIVES SYSTEM DESIGNERS NEW FREEDOM

ADA MAKING INROADS IN COMMERCIAL APPLICATIONS



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CIRCLE 2

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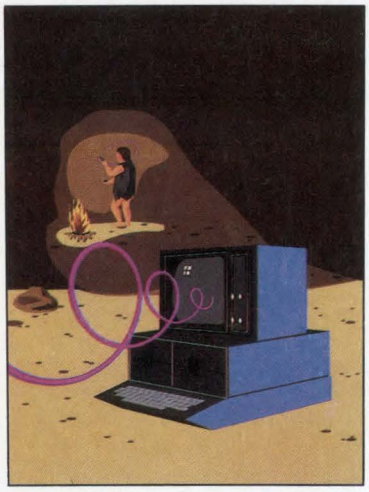


This month's cover was designed and created by Tom McCullough at Coddbarrett Associates, Inc. It was executed using a DICOMED D-38 design station and a D-48 high resolution film recorder.

SPECIAL REPORT ON

TECHNOLOGY FOR ADVANCED WORKSTATIONS

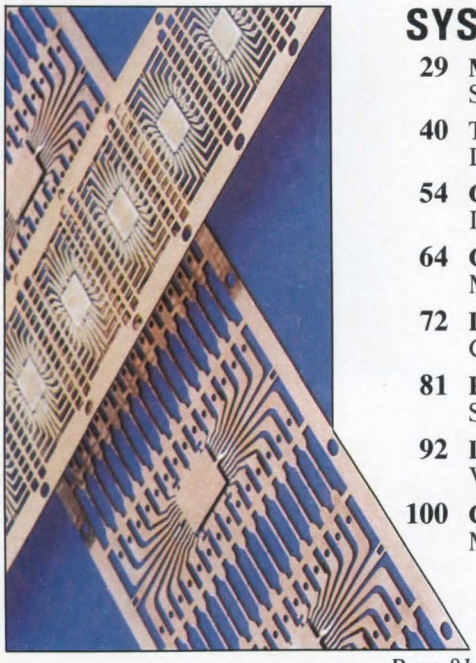
109 Workstations are adopting artificial intelligence techniques to improve software development as well as component and system design. For example, symbolic processing software, Lisp environments, and data flow architectures are making their mark. Designers of computer-based systems need to know what these new workstations can do for them. They also need to know how to choose between the new offerings as costs decline and workstations become generally available.

111 Revolution brewing in workstation technology
New machines sport symbolic processing environments to speed the design process and accommodate the realities of design work.

131 Data flow concepts speed simulation in CAE systems
By exploiting the similarities between a fifth-generation, data-driven system and the so-called discrete-event simulation algorithm, a hardware accelerator can boost simulation speed 100 times.

147 Symbolic processor aids design of complex chips
A workstation offering object oriented programming is used to develop a mouse chip that is testable, reproducible, and fully functional at first silicon.

155 Lisp workstation brings AI power to a user's desk
Built around a full 32-bit NuBus using high density surface mount technology, this system provides an exploratory programming environment in a small ergonomic package.



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Shrinkage continues unabated—Winchesters settle in at 3½ in.

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Debugging tools transform CAE environments

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Machine vision technology is coming of age—but it's not here yet

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Gallium arsenide technology on the move

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Surface-mount technology paves the way for smaller boards

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Variety, density, and high performance mark ISSCC chip designs

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Mini/Micro West stands alone

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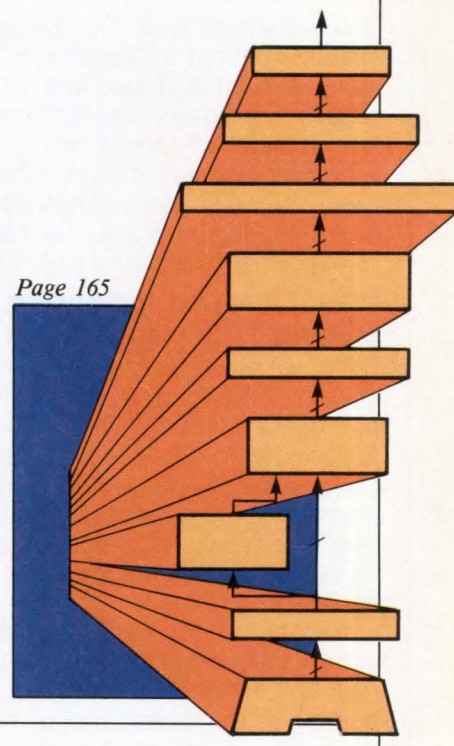
SYSTEM DESIGN

165 Integrated circuits: **IEEE floating point chips implement DSP architectures**
Full compliance with Draft 10 version of the standard allows designers to produce working systems now.

173 Software: **Ada may define new ground rules for programming**
By providing such benefits as structural constructs, modularity, and concurrent processing, Ada could help set a new standard for programming languages both outside and inside the DoD.

179 Test & development: **Integrated tools accelerate code development**
Integrated source and version control, electronic mail, and standard interfaces for programming languages and operating systems can move the software task faster than using additional programmers.

187 Integrated circuits: **Mixing data paths expands options in system design**
Chip designers are creating powerful CPUs and peripherals with 16- and 32-bit parts. Combining these with 8-bit parts overcomes limitations imposed by established designs, incomplete families, and software incompatibility.



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201 Chip set improves floating point performance tenfold

206 A 32-bit VLSI family provides independent building blocks

208 Single-chip image processor sports non-von Neumann architecture

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202 Integral disk and printer mark transportable computer that runs Unix

202 Supercomputer/supermini gap narrowed by 64-bit system

204 Latest VAX delivers performance with large machine technology

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204 Single board holds complete VMEbus system

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206 Voice recognizer broadens data entry options

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"Keep it simple" was the principle of the 14th Century English philosopher William of Occam and it has even more validity today. Faced with the problems of sophisticated computer systems, designers have found that ever more complex programming languages are further complicating their tasks. Until now.

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CIRCLE 3

UP FRONT

Hitachi's 32-bit micro scares Motorola investors

Hitachi, Ltd leaked news of its plans to build a 68000-compatible 32-bit microcomputer at a recent Tokyo technical conference. Although the chip will not be available until 1987, Hitachi's apparent aim to dominate the high end of the microprocessor market sent tremors through the semiconductor industry. Hitachi's Micro 32 now has 300,000 transistors, but the final 1.3-micron technology CMOS chip will contain 420,000 transistors, according to microprocessor marketing manager Sarv Thakur. Tests conducted at Hitachi's Central Research Labs confirm the 32-bit chip will operate at 5 million instructions per second, with a 20-MHz internal clock (40-MHz external clock), according to Thakur. The chip will control a 32-bit bus and will perform full multiply and divide operations on 32-bit data. It includes a pipelined architecture and a high speed cache memory to aid interfacing with I/O processors and other fast peripherals. Eventual packaging is likely to be a leadless chip carrier or a pin-grid array system. As significant as the chip's high performance will be its full upward compatibility with the Motorola 68000. The chip may become 68020-compatible. "We are negotiating with Motorola to license the 68020," says Thakur. However, he is quick to add, "We are talking about a 1987 part. The 68020 really doesn't compete directly with the Micro 32. The 68020 is a step beyond the 68000, but the Micro 32 is several steps beyond." On the day of Hitachi's announcement, Motorola's stock was the most active issue on the New York stock exchange, falling $1.625. While some of the trading was attributed to Merrill Lynch's reduced earnings estimates for Motorola the same day, many analysts said the Hitachi news contributed heavily.—*W.E.S.*

Realtime operating system runs Unix software

Despite its many benefits as a programming environment, Unix is inherently unsuited for realtime applications. Industrial Programming, Inc of Jericho, NY, promises a solution for software developers who want to develop realtime applications in such fields as machine and process control, signal processing, and image enhancement, yet work within the Unix environment. By the second or third quarter of 1985, Industrial Programming's MTOS-UX operating system will run on the 68000 and the 68010, providing rapid response to external interrupts. Otherwise, it looks like Unix System V to the application software. A 68020 version is in the planning stage.—*H.H.*

IBM-to-VAX links proliferate

IBM products are moving into former Digital Equipment Corp strongholds. At the recent Dexpo West in Anaheim, Calif, a number of companies introduced IBM PC-to-VAX file transfer packages. Among those making it possible to use PCs in the VAX environment were Ross Systems (Palo Alto, Calif), Marc Software International (Palo Alto, Calif), Data Processing Design (Anaheim, Calif), and National Information Systems (Cupertino, Calif). Xyplex of Concord, Mass unveiled a controller that links IBM

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(continued from page 5)

PCs to VAX/VMS systems over Xyplex's proprietary local area network. "DEC blew it so badly in the personal computer area that hooking up PCs to VAXes has become a major part of the DEC market," one exhibitor who wanted to remain anonymous remarked. Meanwhile, IBM's Engineering and Scientific Support Center in Atlanta, Ga demonstrated links between DEC products and IBM's new 4361 supermini, a VAX competitor. Attempting to make inroads into the VAX market, IBM showed a unit to give its 4361 DEC Unibus compatibility, plus a software package from Flexcomm (Seattle, Wash) to transfer files between the 4361 and the VAX. According to Dick Evans, manager of the Atlanta facility, IBM is telling DEC users, "Keep your [DEC] products, but take a look at ours. Now we can communicate."—*R.G.*

Digital Research may unveil multitasking for 68000

Combined with Digital Research's Macintosh-like Graphics Environment Manager shown at Comdex in November, the Concurrent DOS multitasking operating system appears ideal for system integrators targeting end users with MS-DOS compatible computers. The Concurrent/GEM combination offers MS-DOS compatibility within the 8086 family, a full complement of proven language compilers, and the chance to develop transportable vertical applications. The only missing link at this point is a Concurrent DOS for processors outside the 8088/8086 family. Developers may not have long to wait. Among those seen visiting the Digital Research suite at Comdex was Sam Tramiel, president of Atari Corp of Sunnyvale, Calif. Tramiel has already admitted that Atari's new home computers, expected to battle IBM, Apple, and Commodore for the low end consumer market, will feature the GEM interface. It is believed Atari's new 16-bit machines will use the 68000 microprocessor and cost around $500. If GEM is indeed running on the 68000, Digital Research of Pacific Grove, Calif will probably announce GEM and Concurrent for the 68000 and possibly the 80286 in the next few months.—*W.E.S.*

Manufacturers back proposal for design data standardization

The Electronic Design Interchange Format, an attempt to standardize the formatting of design data used in computer aided design/computer aided engineering enters the public arena this month with release of the first EDIF specifications. EDIF revision 1.0 proposes a design interchange format for gate array and semicustom ICs. Eventually, EDIF will provide a standard interface for the transfer of design data between silicon foundries, CAD/CAE equipment, and automatic test systems. With active support from Daisy, Mentor Graphics, Tektronix, Motorola, National Semiconductor, and Texas Instruments, EDIF should be off to a good start.—*R.G.*

STC learns perils of surviving in IBM's shadow

The Chapter 11 filing by Storage Technology Corp (Louisville, Colo) and its ensuing financial reorganization demonstrate not only the internal auditing troubles that can bring a high-tech company to its knees, but the danger of following too closely in IBM's footsteps as well. STC manufactures copycat peripherals

(continued on page 8)

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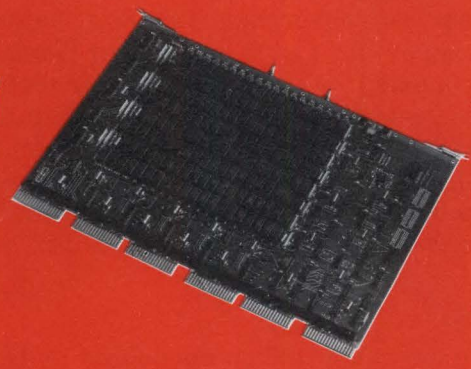

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CIRCLE 4

(continued from page 6)

for IBM mainframes. Its problems began with production of the 2.5-Gbyte 8380 disk drive, the highest-capacity drive STC sells. "We didn't have the thin-film head technology in place until late 1983," explains corporate communications vice president Gordon Swartzfager. But, IBM already had a stranglehold on customer orders for 8380s by the time STC made it to market. Then, in September, IBM cut prices 10 percent. In its rush to get orders, Storage Technology discounted heavily; when sales figures for the quarter ending September 30 were tallied, STC faced a $60 million loss. The situation holds its share of irony. STC recently received a $10 million order from IBM itself. IBM has been having trouble stocking parts for one of its small tape drive controllers, which STC also sells. So IBM is ordering the tape drive systems from STC until it can catch up with the demand. According to one industry consultant, STC shipped half the 11,500 tape drives sold last year—several times as many as IBM.—*W.E.S.*

Floppy disk drive makers are flipping

Hard times have hit floppy disk drive makers, and it's not just the trend toward hard disks. Slowed personal computer sales and increased competition have manufacturers spinning their wheels. Among those hurt, Seagate Technology (Scotts Valley, Calif) reported sales for the quarter ending Sept 30, 1984 were roughly half those of the previous quarter. Miniscribe Corp (Longmont, Colo) reported a third-quarter loss of $2.5 million after netting $1.4 million a year earlier. The bad news doesn't stop there. Other manufacturers of drives or media with sliding third-quarter sales and earnings include Tandon (Chatsworth, Calif), Verbatim (Sunnyvale, Calif), and Dysan (Santa Clara, Calif). The storage company with the most exciting revenue increases (338 percent increase from third-quarter 1983 to third-quarter 1984) doesn't even sell conventional media. That's Iomega Corp (Ogden, Utah), makers of the Bernoulli Box. Of course, there's good news for purchasers of disk drives—the predicted disk drive shakeout should pull prices down faster than a disk head crash.—*W.E.S.*

Transputer nears readiness

Inmos Corp, which announced its Occam parallel programming language about two years ago and promised a silicon transputer by the fourth quarter of 1984, is on schedule. Inmos has the T424 processor in silicon and is working on final masking. First samples of the chip will be released on a Eurocard evaluation board around the middle of the year. Individual chips should follow in the second half. Meanwhile, true believers can begin developing software for the device on a VAX using the Inmos Occam Programming System for the VAX/VMS.—*W.E.S.*

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CIRCLE 5

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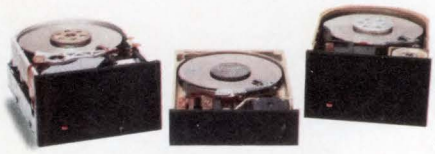

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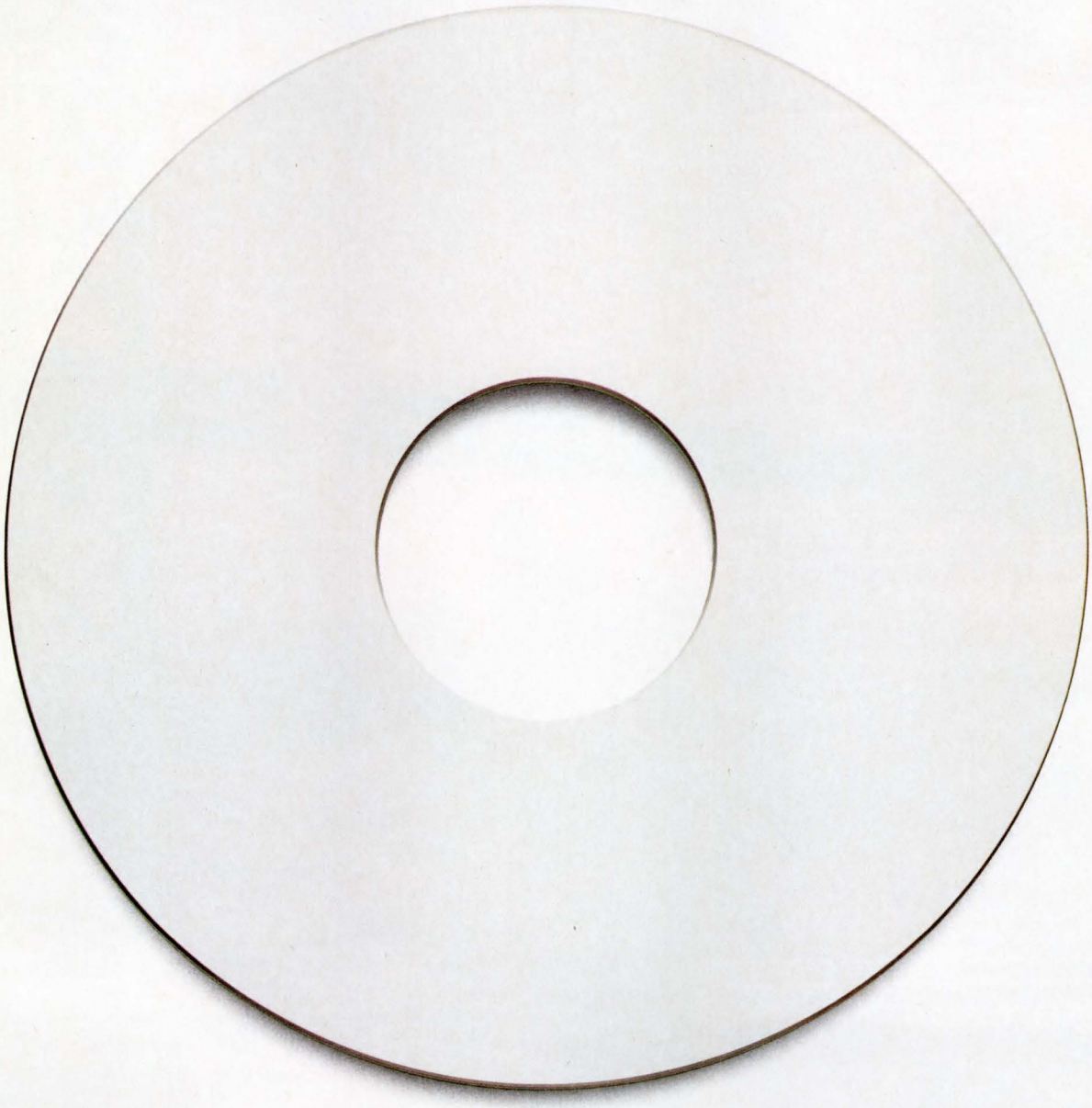

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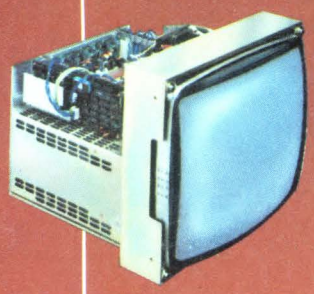

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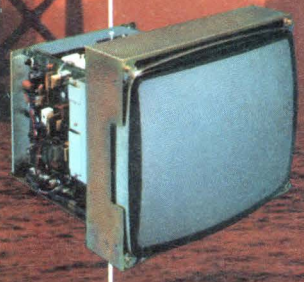

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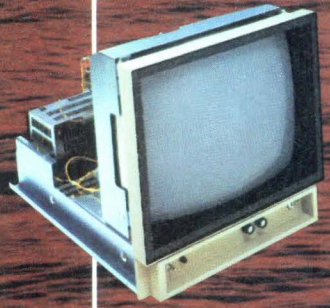

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CIRCLE 7

THE VAR AND OTHER GOBBLEDYGOOK

More than any other industry, it seems, the computer business is afflicted by too many acronyms and abbreviations. Originally intended to simplify and speed communication, all this jargon more often causes confusion and impedes the flow of information. Though some trade publications could have helped to reinforce a standardized terminology, they have merely added to the confusion by proliferating ambiguous acronyms. As an editor this saddens me; as an engineer it really annoys me.

The confusion has escalated to the point where, even within the computer industry, some abbreviations have at least two entirely different meanings. Consider, for example, PCB, μC, VAR, and PC.

Depending on which story you read in which publication, PCBs might be printed circuit boards or polychlorinated biphenyls. This gets even more confusing when the polychlorinated biphenyl is a solvent for cleaning a printed circuit board—in other words, you have a PCB degreasing a PCB. As a journalist, I can understand the pressure on headline writers to abbreviate. But the acronym PCB in computer publication headlines is about as confusing and frustrating as the use of "Giants" in a sports headline (when the story could be about the San Francisco baseball Giants or the New York football Giants).

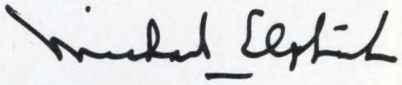
While the acronym PCB may have originated with overzealous headline writers, I believe the magazines that promoted the new μC and VAR acronyms did so deliberately. Those magazines compete with *Computer Design* to some extent; therefore, our editors and readers must grapple with the confusion other magazines helped to create.

The first heavy use of μC to mean microcomputer occurred in a magazine that somewhat immodestly describes itself as "everything designers need" (a slogan that helps us forget its initials originally stood for *Electrical Design News*). To put itself on the map as a microprocessor and microcomputer journal, it adopted such eye-catching abbreviations as μP and μC. The main problem with that, of course, is that μC and μP were already standard abbreviations (with μC meaning microcoulomb). Fortunately, most other design magazines either refused to use the μC and μP acronyms, or have reversed their earlier decisions to use them.

Now let's look at the VAR. When I first studied electrical engineering, a VAR was a clearly defined electrical unit. The initials stood for volt ampere reactive. Today, however, the initials have a vastly different meaning within the computer industry. Depending on who uses the term, a VAR can be a value added reseller, value added remarketer, or value added retailer.

According to another competing magazine that calls itself "the trade journal of the value added marketplace," VARs are system houses, consultants, computer distributors/dealers, and third-party system integrators. Recently, VARs have become increasingly attractive to companies selling hardware and software because VARs buy products for resale into vertical end-user markets. Note, however, that a VAR is not a clearly defined occupation (such as engineering management) but a rather amorphously defined group of organizations. Note, also, that most of those types of organizations employ engineers (such as readers of *Computer Design*) and that the engineers are responsible for any real value added to systems built by those organizations. Why then does the "trade journal of the value added marketplace" define the concept so vaguely? My theory is that its editors are forced to do so because the readership of the magazine itself is vaguely defined. The lack of clarity allows them to avoid explaining who adds value and who merely adds cost.

Before closing, I would like to nominate PC as the most confusing abbreviation of all time. In a computer publication, PC could stand for printed circuit, personal computer, professional computer, programmable controller, program counter, or professional communication. For the creation of that particular monster, we must all accept part of the responsibility. Even at *Computer Design*, I must confess, we have sometimes used it without defining it.



Michael S. Elphick
Editor in Chief

256K DRAMS IN CHMOS. THERE HAVE BEEN OTHER INNOVATIONS AS IMPORTANT.

But not lately. Intel's 256K DRAM in CHMOS will set new industry standards. Redefine high performance. And change the direction of VLSI technology.

Our revolutionary new chip provides four times the storage capacity, a high data bandwidth mode and a drastically lower power consumption than NMOS DRAMs.

It combines the best benefits of CMOS static RAMs, low power and high bandwidth, with the traditional high density and cost effectiveness of DRAMs.

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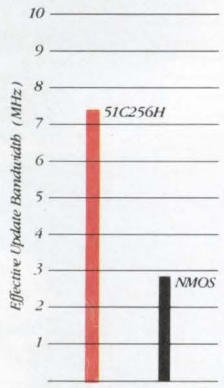

The high-performance advantage: For a typical 1Kx1K display, Intel's CHMOS DRAMs outperform NMOS better than two to one.

For the first time, you can design your truly portable system to run the most powerful spreadsheet software on the market. Without costly CMOS SRAMs. Even workstation processing is possible in a portable.

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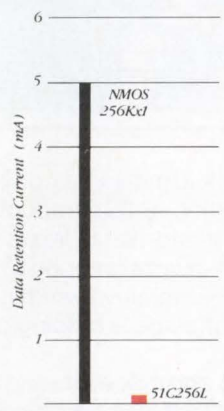

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CIRCLE 115

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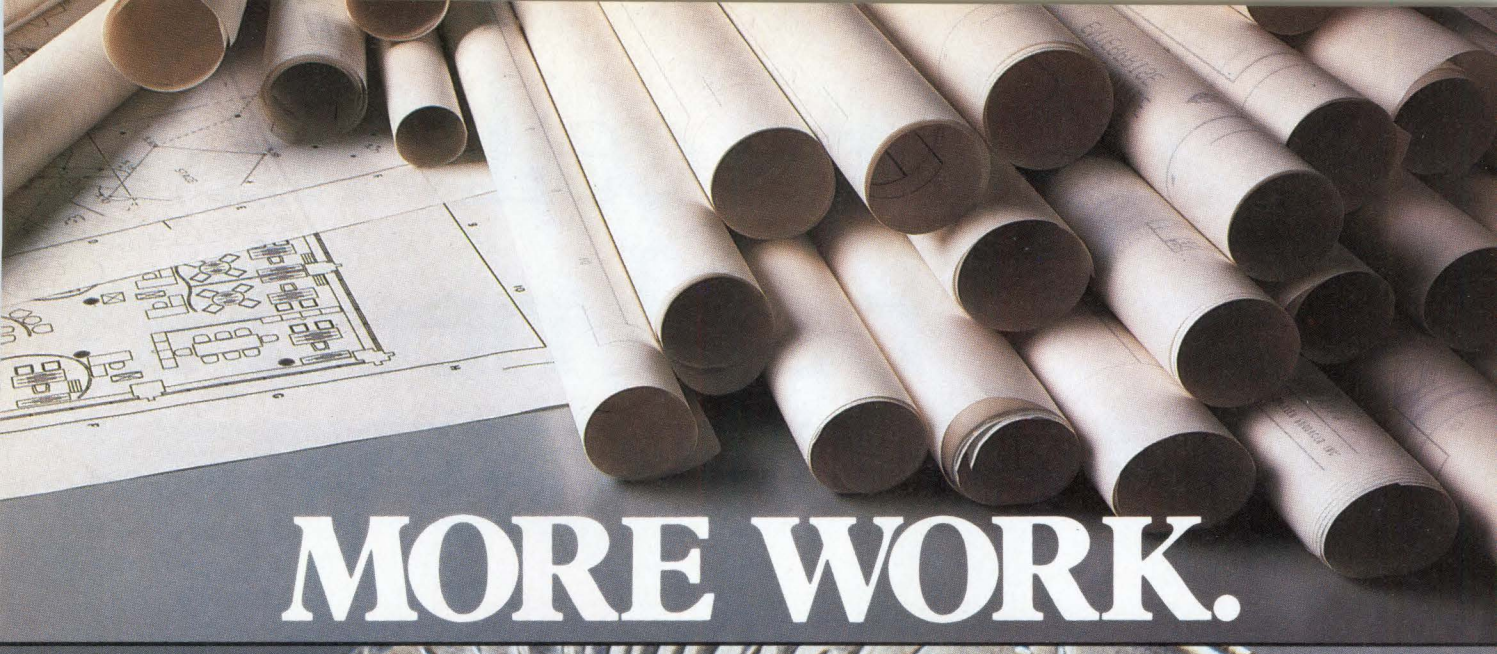

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CIRCLE 9

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TI's Standard-cell Design System is TTL based. That means we can quickly, easily, and accurately translate your TTL logic requirements into equivalent standard-cell functions to arrive at reliable cost figures.

In so doing, we will determine the chip size and the number of I/Os—major factors affecting costs. We will evaluate the advantages of various partitioning schemes and take into consideration packaging options.

TI will detail nonrecurring engineering costs—what it will take to get you prototypes—as well as recurring, or production, costs. We will tell you where these costs will occur and why they will occur. We will also suggest ways to keep them to a minimum. The result: No surprises along the line.

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Count on significant system savings

Major improvements in system performance, reliability, and power consumption alone often justify the cost of standard-cell ICs.

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Familiar TTL design techniques are used in the design of your TI standard-cell ICs. Actually, the process is very similar to breadboarding with standard TTL logic packages. Which means you don't have to invest time and effort in learning new rules.

TI's standard-cell library contains all the popular SN54/74 functions you've worked with over the years. Plus RAM, ROM, PLA, ALU, and linear functions. As well as design-for-test cells that ensure thorough design testability.

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TI Regional Technology Centers can add to your savings

You can hold costs down by performing much of the initial design work yourself. For example: Schematic capture, simulation, testability analysis, test-pattern generation, and the test-pattern grading required to finalize your standard-cell design. You can also perform the chip layout, or leave that to us.

You'll find these steps progressively easier as you execute subsequent standard-cell designs, but the first time you will probably need assistance.

That's where TI's convenient Regional Technology Centers come in. Strategically located throughout the country, they are staffed with standard-cell specialists who will provide whatever advice and counsel you need. Each Center has engineering work stations for your use plus the software tools and the computers necessary to complete your logic design. In short, the Centers are a reliable time- and money-saving design resource.

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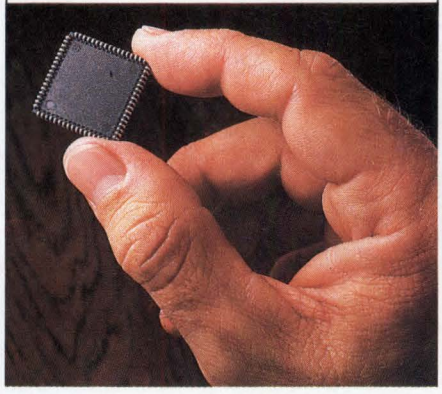

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A number of simulation and testability steps are built into TI's standard-cell design flow. These checks and double-checks are vital to fulfilling our commitment to deliver prototypes that perform to your specifications. They help us achieve our goal of first-pass success, so you are spared any second-pass expenses.

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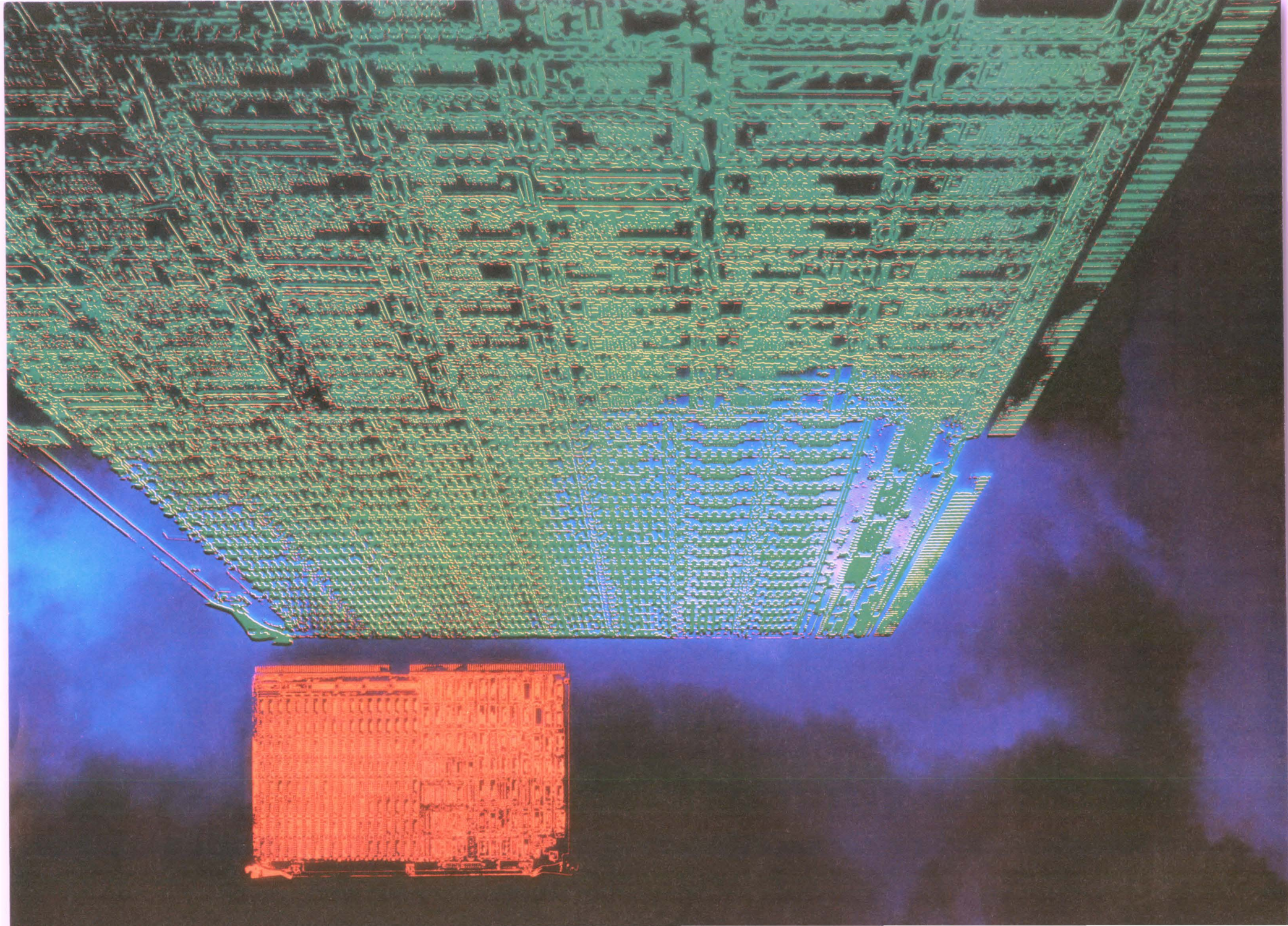

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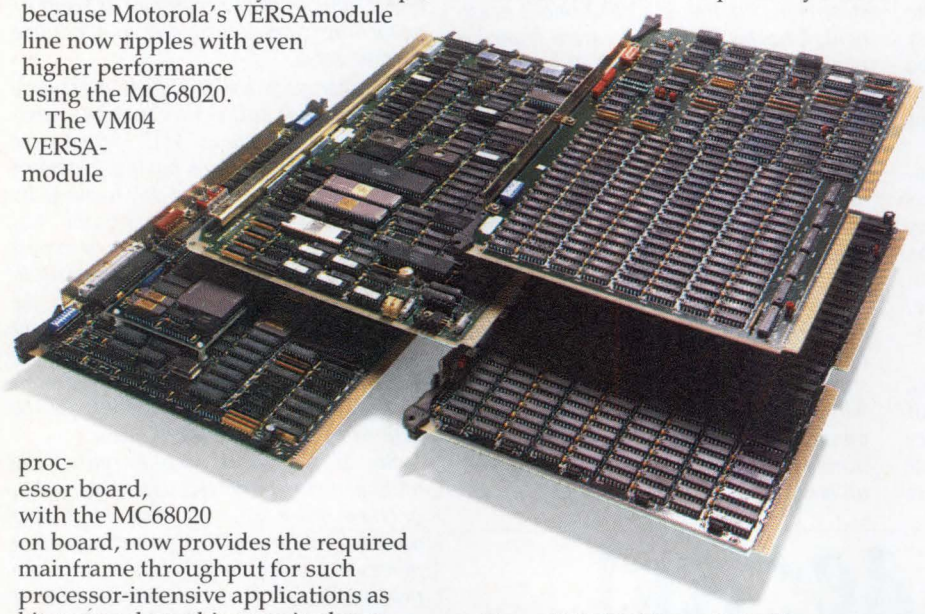
VERSAmodule microcomputer boards have already proven themselves in performance-demanding communication, industrial, laboratory and imaging applications. You knew these boards were powerful workhorses before, but hold on to your bootstraps, because Motorola's VERSAmodule line now ripples with even higher performance using the MC68020.

The VM04 VERSAmodule processor board, with the MC68020 on board, now provides the required mainframe throughput for such processor-intensive applications as bit-mapped graphics manipulators, scientific data acquisition systems and artificial intelligence machines. Applications that, before this, required mainframe machines.



Gaining speed, adding power, lowering overhead.

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16K bytes of instruction/data cache on-board help reduce off-board memory accesses to ensure top performance. When off-board access is needed, the VM04 calls on the interface capabilities of Motorola's MC68020-specific RAMbus™ to eliminate most arbitration overhead and speed memory transfers.

The VM04 monoboard is the first MC68020 processor board to offer paged memory management hardware, plus an interface to support the soon available MC68881 floating point math co-processor.

These new modules add to a broad offering of board-level products including processor, memory, controller and communication modules with complete evaluation and development systems.

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Two new high density memory boards have been added to the line to complement the MC68020-based monoboard.

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The VERSAmodule Family is supported by both of Motorola's M68000 operating systems: the VERSAdos™ operating system for real-time applications, and the SYSTEM V/68™ operating system where a UNIX™ operating system environment is desired.

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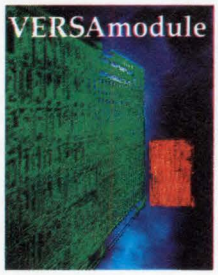

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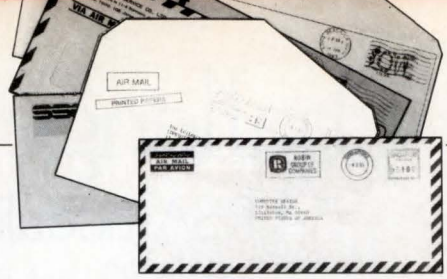

In search of essence

You are to be commended for your Editorial in the Oct 15, 1984 issue (p 13). This country surely needs quality circles and problem-solving groups. However, are you sure what you have written is, in fact, the essence of the company you describe? I don't want to sound like sour grapes.

For years, I have been involved in the purchase of electronic components. Very seldom do I find a company person to be helpful. National Semiconductor is no exception, for I remember an incident in particular.

I called National Semi at various locations on the West Coast for various quantities of programmable logic array chips manufactured there. After many transfers I got to the correct person. I was told that the chips were available, but with a long delivery time. (The person was indifferent.)

I checked with a local supplier who told me that he had a sufficient stock of Japanese PLA chips for my needs. They were cheaper also. It's been my experience that National Semi is no different from any other American corporation. The Japanese are always there, ready to give you what you need. It's amazing.

John Haines
4004 Heathfield Rd
Rockville, MD 20853

As I pointed out in my editorial, the statements attributed to National's president, Charles E. Sporck, were from his testimony to the Congressional Joint Economic Committee. Moreover, having visited the company's Santa Clara plant several times and having observed some of the strategies he claims to use, I have no reason to doubt his word. The question seems to be, therefore, not whether National uses these management strategies but, whether the strategies are effective.

Also, I think Mr Haines is really asking another important question not directly related to the company's management style. I, too, have never really understood why most American semiconductor companies encourage their sales and applications people to concentrate their efforts on large volume purchasers while diverting other potential customers to distributors. This strategy does not allow for the fact that design engineers initially buy only small quantities of ICs for breadboarding and prototyping—even though their designs may eventually result in huge orders after the system goes into production. So, with their existing strategy, many semiconductor companies seem to be turning away future sales to maximize current sales.

Another question Mr Haines might have asked, but did not, is why so many semiconductor companies with progressive management styles are having problems with the U.S. government due to allegedly inadequate testing of military-grade ICs. At the very minimum, one would expect that use of a quality circle would result in improved product quality. If, however, the major benefit of the new management strategies is a unified sense of purpose and direction throughout the company, management cannot duck responsibility for the actions of individual employees.

So, as Mr Haines implies, either the management strategies do not work, or they work so well that employees quickly sense when top management places a greater emphasis on short-run profitability than on customer service or product reliability.

Michael Elphick
Editor in Chief

Article corrections

In the article "Digital Signal Processing Moves into High Gear" by Harvey Hindin, *Computer Design*, Oct 15, 1984, p 61, the credit for some information extracted from the Apr 19, 1984 issue of "In-Stat Research Letter" was inadvertently omitted. In addition, in the illustration on p 66, also from the "In-Stat Research Letter," an error from the original was repeated; "MkHz" should, of course, have been "MHz." Finally, in that same illustration, "RAM multiply speed" should have been "raw multiply speed."

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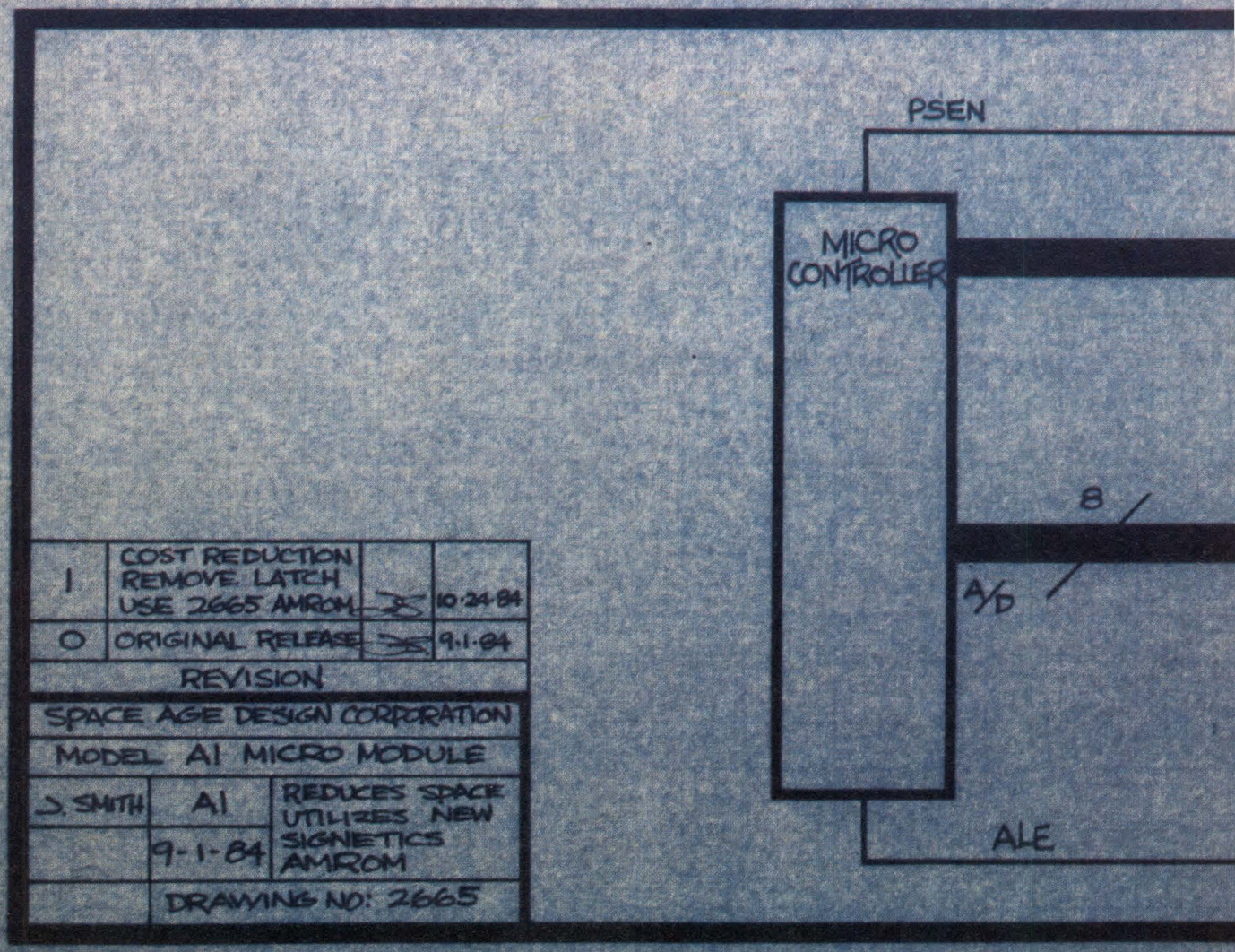

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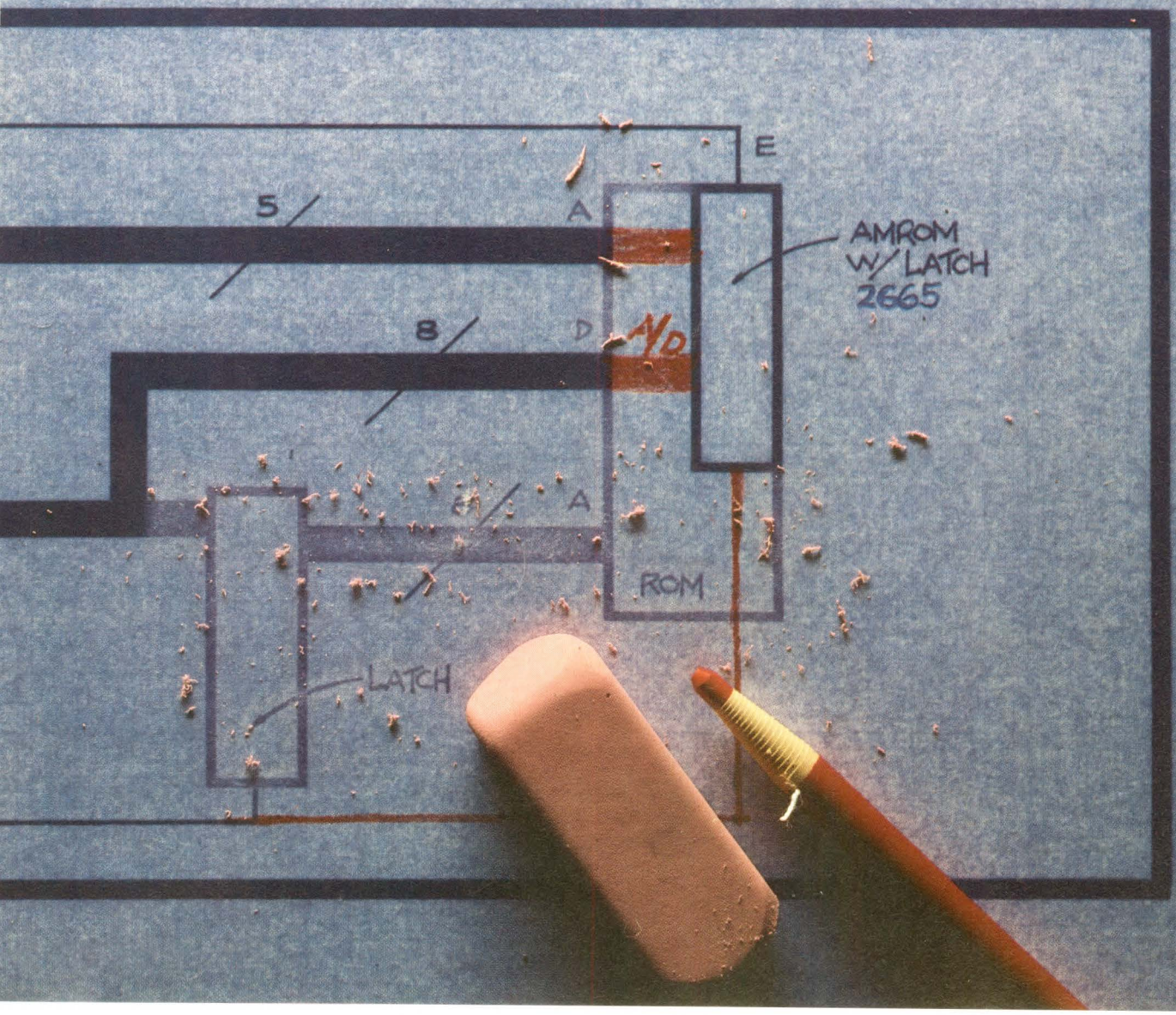

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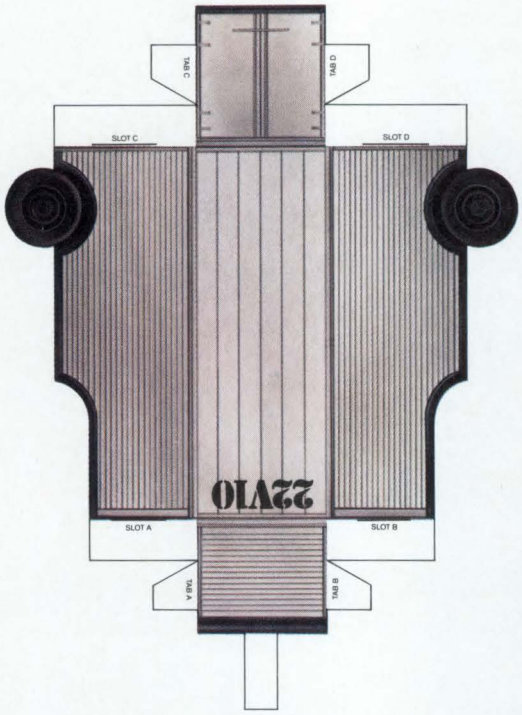

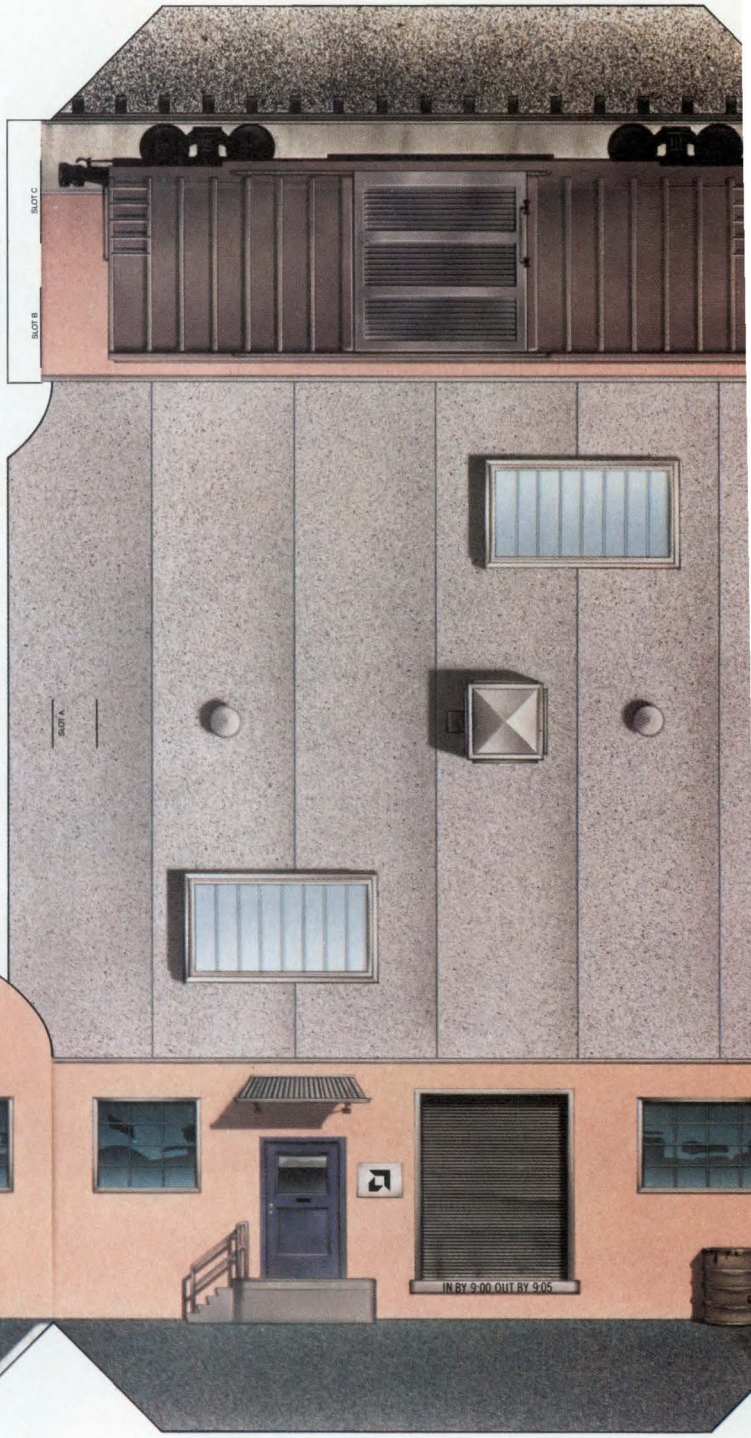

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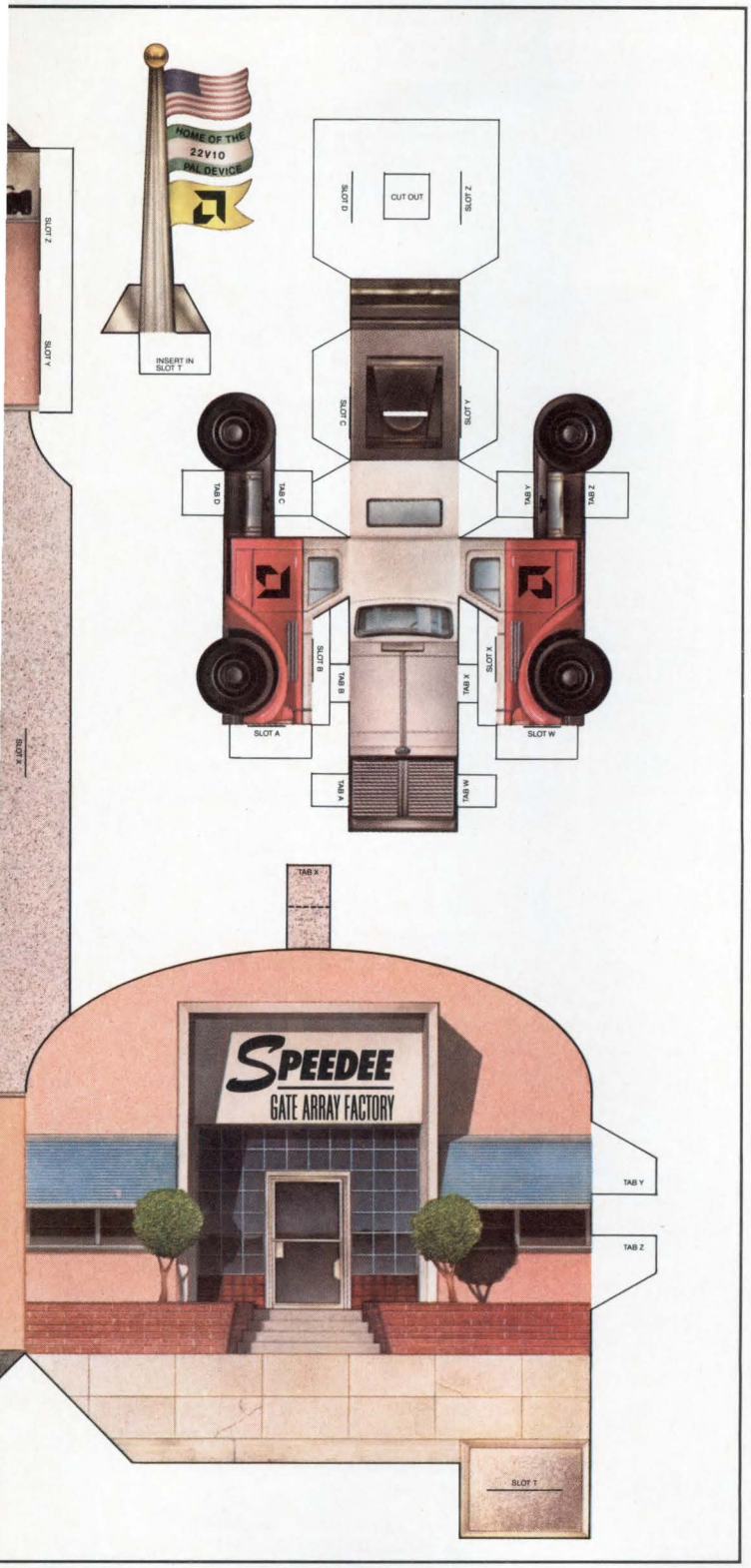

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CIRCLE 14

New SKY WARRIOR

15 MFLOP Array Processor cuts through $1,000/MFLOP barrier!

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The 15 MFLOP SKY WARRIOR isn't simply a minor technological advance. It's nearly a revolution, fully twice as cost effective as anything else on the market. Capable of performing 15 million 32-bit floating point operations per second. And ½ million operations per second on 64-bit data.

Use it for 2-D Fast Fourier Transforms in imaging systems, in on-site seismic analyses, in 3-D graphics workstation transformations, in real time laboratory signal processing systems, or anywhere else requiring fast interaction with lots of data.

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You don't have to worry about delivery, performance or backup when you deal with SKY. We specialize in floating point products. Our customer list reads like a scientific and engineering Who's Who. Ask and we'll give you references. They'll tell you what they tell us, things like *rock solid engineering*, *instant responsiveness*, *super technical support*, and *total product reliability*.

For detailed technical information on our exciting new SKY WARRIOR or any of the other products in our LEGION of arithmetic processors, contact SKY Computers, Inc., Foot of John Street, Lowell, MA 01852, telephone (617) 454-6200.

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CIRCLE 15

Shrinkage continues unabated—Winchesters settle in at 3½ in.

At only a quarter the size of the now ubiquitous 5¼-in. mini Winchesters, 3½-in. Winchesters with 10-Mbyte capacities are reaching the market in production quantities. Measuring 4 x 5.8 x 1.6 in. (10.2 x 14.6 x 4.1 cm), these 10-Mbyte drives may soon be overshadowed by units that pack 20 Mbytes into the same volume.

Despite the pressure for higher capacity, the major goal at this time is to produce reliable drives in the 10-Mbyte capacity range. To accomplish this while maintaining the low cost needed to compete successfully with 5¼-in. drives, the components used in manufacturing them must be readily available and designs must be eminently manufacturable. These criteria call for drives that use low cost stepper motor positioning systems, conventional ferrite head technology, and multiple sourced oxide-coated media.

Because these drives will ultimately be used in environments far more hostile than the computer room, considerable engineering effort has been made to ensure that they can survive abuse. Shock and vibration are probably the most common types of abuse. For this reason, the necessary protection is being designed into the drives. Power requirements are also being kept low to eliminate the need for a separate power supply. This allows the drives to operate off the power supply of the system into which they are designed.

In addition to reduced power consumption, the lower mass of the components used to build the drives cuts the total unit weight, making shock and vibration protection easier. Using a single multilayer PC board for drive control and electronics saves both power and space.

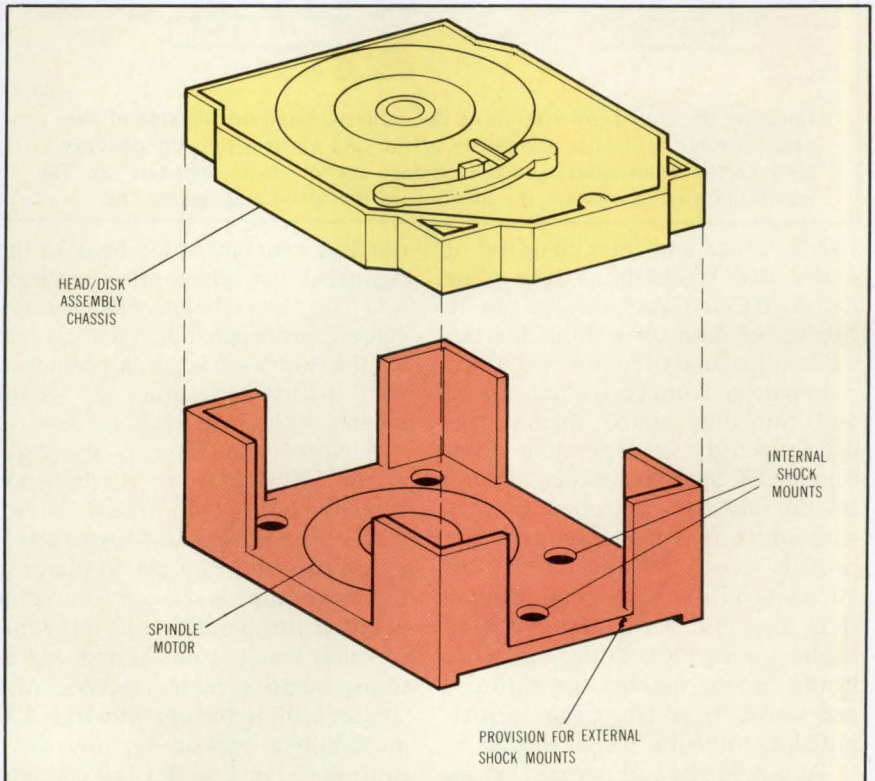
Efforts to achieve these savings in power and size are dictated by the compact nature of the systems into which the drives will go. In portable applications, for example, weight is a major system constraint. The results of these efforts can be seen in power specifications that range from 15 W down to 9 W, and in finished weights that range from 2.5 lb to less than 2 lb.

Another feature that these drives have in common is a standard interface. Their intended application in single-user portable and desktop computer systems allows effective use of the ST506/412 interface specification. This specification enables the units to provide the 10-Mbyte capacity deemed desirable for these applications on the surfaces of two platters. The linear and track densities needed for this capacity are within the range of the open-loop stepper motor positioning systems dictated by cost constraints.

Doing things differently

Designers from Hewlett-Packard (Greeley, Colo) have chosen to implement the system-level Small Computer System Interface rather than the industry standard ST506/412 in their drives. Rotating at 3000 rpm rather than the typical 3600, the drive provides a 4-Mbit/s transfer rate rather than the more common 5 Mbits/s of the ST506 spec. Dubbed the Rugged One, the HP 97501A records at 12 kbits/in. and packs tracks at a density of 1100 tracks/in. Other drives in this form factor typically specify linear densities in the

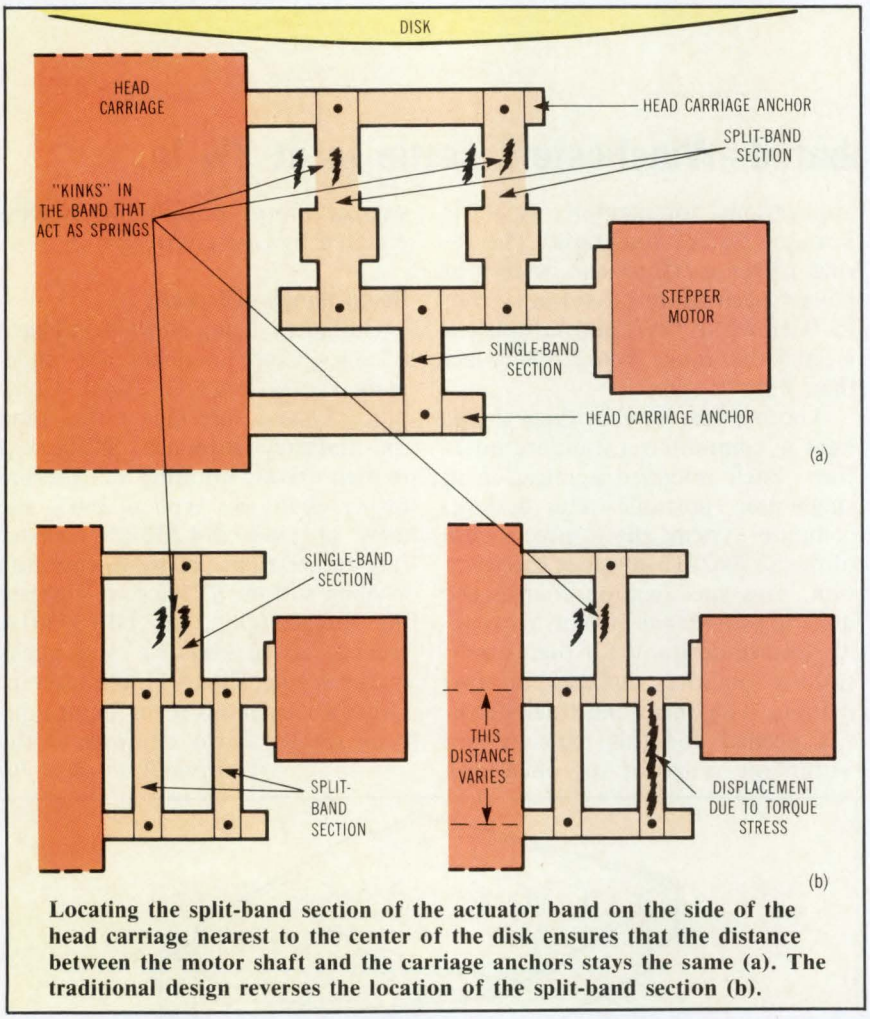
(continued on page 30)



The box within a box design of LaPine Technology's micro-Winchester drive combines with a 4-point internal suspension system to protect components from shocks up to 40 G.

Shrinkage continues unabated

(continued from page 29)



Locating the split-band section of the actuator band on the side of the head carriage nearest to the center of the disk ensures that the distance between the motor shaft and the carriage anchors stays the same (a). The traditional design reverses the location of the split-band section (b).

10-kbit range and track densities of under 650 tracks/in. Using these drives, Hewlett-Packard can put 10 Mbytes of data on a single platter, while other units require two disks.

Departing from both oxide-coated and thin-film plated media, this drive records on sputtered thin-film media. Sputtered media, because of the closely controlled process with which it is manufactured, can provide areal densities of up to 30 kbits/in.^{2}—more than double that possible with oxide-coated media—using monolithic read/write heads. It also supplies the hardness and resistance to abuse that is attributed to thin-film plated media.

To obtain the full potential from this media, the drive uses a closed-loop servo positioning system to ensure accurate head placement. Servo data written in each sector on the disk's surface is fed back to the stepper-driven positioning mechanism. This allows the controller to compensate for thermal differentials and lets the read/write heads be positioned with sufficient accuracy to record reliably at the 1100 track/in. density.

A closed-loop servo is also used in the HH-312 from Microscience International (Mountain View, Calif). Providing a 10-Mbyte capacity on two thin-film plated platters, this drive embeds servo information to correct head positioning inaccuracies that result from thermal variations, stepper motor delays, and stepper settling factors. The HH-325, a 20-Mbyte version of this drive (introduced at Comdex last November), uses this closed-loop servo to further advantage.

Reference data is written in wedges on the data surface and is available on every track rotation. Each servo byte consists of a 3-bit burst that contains a synchronizing pulse and positioning pulses. When initialized, the drive samples four tracks of servo information. This information is used to adjust the stepping operation before proceeding to the track following algorithm. The technique achieves high accuracy over various operating conditions.

Raising the ante in this form factor to 40 Mbytes with a 40-ms access time, Newbury Data Recording, Ltd (Staines, Middlesex, England) supplies the penny. "The main challenge in accomplishing this capacity," according to the company's international marketing manager, Dave Muir, "was to get four disks in the box so that linear density could maintain the ST506 data rate." This was achieved by using minimonolithic heads that are staggered to reduce the space between disks.

A brushless dc motor serves as the key to the drive's 40-ms access time. Effectively used as a voice coil, the motor provides fast, precise positioning. Its rotary motion is translated to linear motion for head positioning through a metal band that drives the actuator assembly.

Microcomputer Memories (Van Nuys, Calif) has also stretched the capacity of the 3½-in. form factor to 20 Mbytes. These drives write on four oxide or plated platters at 10,943 bits/in. using monolithic heads to attain this capacity. Miniscribe (Longmont, Colo) is also said to have 20-Mbyte units under evaluation.

Back to basics

Regardless of the capacities provided by drives of this caliber, the crux of the matter is how well the drive performs its intended function. Since 3½-in. Winchester drives are aimed at the storage needs of portable computers, the ultimate criterion becomes how well these drives resist damage from the various hazards they encounter when they are thrown into a car trunk and subjected to extremes in temperature.

And it seems that designers of these midget drives have also taken

a serious look at the hazard potential of the portable environment. Specifications for these units cite shock levels up to 100 G and vibration to 1-G acceleration, 5 to 50 Hz. In addition, various methods are used to protect data stored on these disks against loss. Head and spindle locks, guard bands, and dedicated landing zones are used to ensure adequate protection.

Designed to survive the abuse potential of the portable and desktop personal computer environment, LaPine Technology's (Santa Clara, Calif) drives claim to withstand shock loads of up to 100 G. A 4-point internal suspension system allows Ranger family units to survive shocks to 40 G. Additional external shock absorbers mounted on two sides bring specifications up to a shock load of 100 G with power off.

According to LaPine's vice president of marketing, Rick Brechtlein, "To put the technology where it is exposed to abuse and enable it to meet reliability requirements, extraordinary measures must be taken to reduce the effects of shock, vibration, and temperature changes." These extraordinary measures in LaPine's case resulted in a "box within a box" design. In such a design, the head/disk assembly is mounted within a frame such that it is shock mounted within itself.

Seagate (Scotts Valley, Calif) has paid particular attention to shock characteristics in designing its recently announced ST112 drive. According to product planning manager, Bob Toda, "In some regards shock pads may help shock aspects, but hurt vibration aspects of a design." Since shock and vibration are contrary to each other, attempts to dampen vibration may result in amplification and transmission of shock, Toda points out. To minimize the impact of both, it is necessary to make a compromise between the two.

Instead of focusing solely on shock and vibration, Seagate concentrated more on the use of low mass minislider heads to minimize the impact of shock during operation. Seagate designers believe that most of the damage incurred during handling results from the head slapping onto the media. Because of the smaller cross-sectional area and relatively low mass, the use of minislider heads reduces damage resulting from head slap.

Recognizing the abusive conditions under which these drives must operate, Microscience took steps to maintain accuracy under stress conditions. According to Ron Schlitzkus, director of marketing, accuracy is ensured by a unique actuator band design. Unlike typical designs, where the split band section is located on the back side of the carriage head assembly, Microscience locates the single-band section toward the back. This, according to Schlitzkus, places the primary stress on the single stronger element of the band and allows a constant distance to be maintained between the stepper motor shaft and carriage anchor.

In addition to shock and vibration, temperature conditions also contribute to the abuse that these drives must endure. According to Brechtlein, "LaPine expended a lot of engineering time and detail to make sure that thermal characteristics could respond

(continued on page 32)

The half-height removable Winchester cartridge

Reducing a complex and precise product to pocket-sized dimensions is no easy task. Couple this problem with the requirement for removable rigid media in a package that will withstand abuse from unsophisticated users, and the challenge becomes even greater.

One major consideration faced by manufacturers of removable Winchesters is how to avoid head/media damage and data loss without violating size and cost restrictions. Because the typical environment subjects the drive to rough handling, protection of the delicate head and selection of durable media are paramount.

Along these lines, two trends have developed in removable Winchesters. One is to continue to use standard oxide media, and mechanically retract the heads from the head/disk assembly. This adds to the overall size of the drive, representing a trade-off into the larger 5¼-in. form factor. Another solution to the head/disk interface problem is to combine traditional design with variations on a Winchester theme.

Operating under the company philosophy that adding mechanical complexity often trades one problem for another, Syquest Technology (Fremont, Calif) has designed a simplified head/media control element into removable Winchester disk drives. When no cartridge is housed in a drive, a simple cam device keeps the heads out of contact with each other. This protects the heads during drive transport, and keeps the total size of the drive to a minimum. A failsafe cartridge interlock mechanism ensures correct cartridge insertion and disengages the heads when the drive door is opened. When the heads are delivered onto the media for read/write, a dash pot damper ensures a gentle, controlled landing.

For the media, Syquest has chosen to combine thin-film metallic plated disks with a microscopic sputtered layer of graphite over the disks' cobalt surface. Standard Winchester media are coated with ferrous oxide and have a hardness of 3.3 on the Mohr scale. Cobalt coated plated media have a hardness of 5.5. When coated with graphite, the cobalt media's characteristics for head takeoffs and landings improve more. The lubricating graphite also seals and protects the media from environmental reaction and contamination from dust or smoke particles.

Plated media provide improved magnetic switching that results in higher recording densities: 12.4 kbits/in. versus the 9300 associated with ferrous oxide media. The result is high data capacities on a small disk. Current half-height product offerings provide 10 Mbytes of removable storage on 100-mm cartridges.

Shrinkage continues unabated

(continued from page 31)

Comparison of Hard Disk Drives

	Seagate	Rodime	Microcomputer Memories	Microscience	Microscience	LaPine	Hewlett-Packard
Model No.	ST112	RO 352	M-112/125	HH-312	HH-325	3522	HP 97501A
Disks	2	2	2/4	2	2	2	1
Heads	4	4	4/8	4	4	4	2
Capacity (in Mbytes)	10	10	10/20	10	20	10	10
Access time	65 ms	92 ms	85 ms	70 ms	80 ms	80 ms	75 ms
Power requirements	13 W	13 W	12 W	9 W	9 W	13 W	10 W
Shock operating	40 G	30 G	—	10 G	10 G	50 G	50 G
Temperature rough operating	50 to 113 °F	50 to 122 °F	40 to 115 °F	40 to 122 °F	40 to 122 °F	40 to 122 °F	32 to 122 °F
Weight	2.5 lb	2.2 lb	1.7 lb	2.25 lb	2.25 lb	2 lb	2.1 lb

to a wide range of temperature fluctuations." In the design, LaPine had the advantage of starting from scratch specifically to meet these requirements. The design achieves a balance between the thermal expansion and contraction of components "through careful selection of materials and attention to nitty gritty equations," says Brechtlein.

Rodime's (Mission Viejo, Calif) design relies on the same basic principles. In the RO 350 series, head/track relationships are maintained by designing thermal variants such that thermal expansion of disk and positioners are balanced within the operating range. George Rea, marketing manager, says that the problems are minimized by the 3½-in. form factor. A 3½-in. disk results in a smaller excursion since the radius is 1½ in. as opposed to the 2½-in. radius of 5¼-in. media. Rodime handles this by selecting materials with matching thermal characteristics (eg, aluminum substrate balanced by aluminum parts in the head assembly flexure).

Stepper motors are major contributors to problems of uneven thermal expansion. Microscribe minimizes these effects by thermally isolating the stepper motor from the head/disk assembly. This practice achieves greater reliability by allowing heat produced by the motor to be dissipated without affecting the disk or head positioning mechanism.

Another point that Seagate considers important in achieving high reliability is elimination of the dedicated landing zone used by many designs in favor of a purely random landing point. By landing the heads at random on the data surface of the disk, potential damage due to start/stop effects can be minimized. Toda says that while some people express concern that this method might damage the data surface, extensive tests performed by Seagate show that having the heads land in random locations reduces the chance of damaging any one area. Also, the chance of head damage caused by abused media is less than when the heads always land within a certain area.

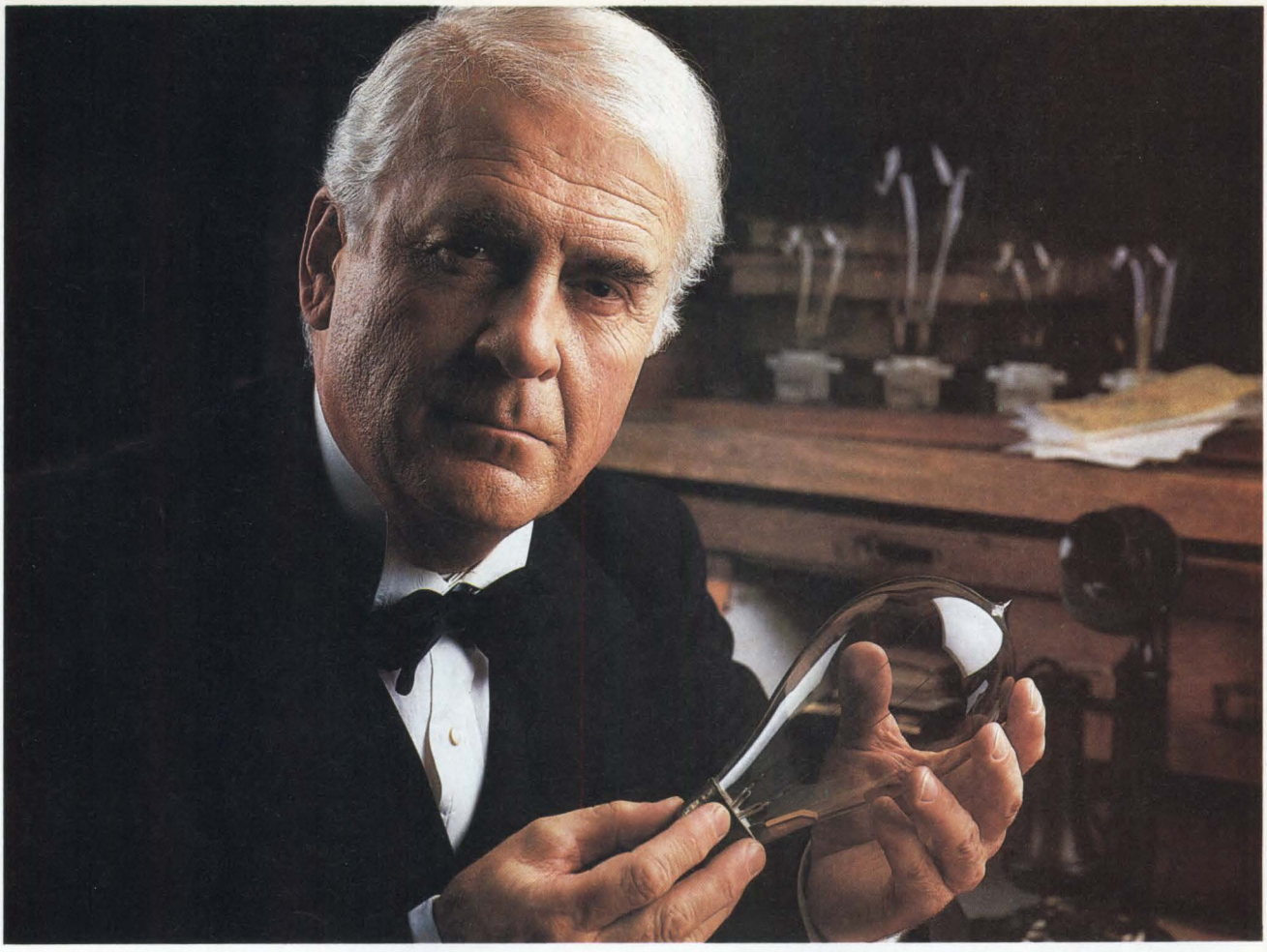
Instead of providing a shipping zone on which to park the heads during transportation as many drives do, some vendors feel that more extreme measures are required to prevent head/media damage. Rodime's RO 350, for example, provides brakes. The dual acting failsafe brake in this design automatically brakes the dc spindle motor at power off. It also acts as a transit lock for the spindle motor and locks the stepper motor to immobilize the actuator arm. These brakes release automatically when power is switched on to the drive.

LaPine's drives provide a further measure in this regard, both lifting the heads off the media's surface and locking them in a lifted position. According to Brechtlein, this is extremely important for shock and vibration protection when units are being moved. The proprietary mechanism used by LaPine acts similarly to that of a removable media device. " By lifting the heads off the media and holding them off," Brechtlein says, "the chance of head or disk damage is virtually eliminated."

While LaPine is starting to incorporate thin-film plated disks in its drives, it is not doing so because of the persistent arguments that thin-film media provide harder surfaces and therefore are less susceptible to damage. Countering those contentions, Brechtlein states that "although plated media is more tolerant than oxide media as far as damage is concerned, there are also heads involved." When a device is subjected to movement and shock, the plated media may resist damage, but head cracking may result if impact occurs because of its relatively greater hardness. "You have to consider the head and the media as a combined system," says Brechtlein.

—Peg Killmon, Senior Editor
SYSTEM TECHNOLOGY

(continued on page 40)



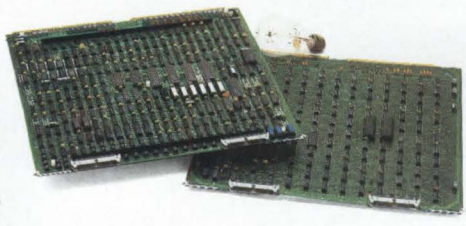
Zetaco's latest inventions make 86 disk and tape drives Data General BMC compatible.

Zetaco's BMX-1 disk drive controller and BMX-2 mag tape coupler give the user of Data General's high-speed BMC (Burst Multiplexor Channel) full compatibility with the newest high-speed, high-capacity, non-DG drives.

These two bright ideas let you choose virtually any high performance SMD-type disk drive or ½" tape drive to run on the BMC or Data Channel on DG's newest Eclipse or MV Series mini.

Each BMX-1 supports up to 4 SMD-interfaced hard disk drives. Each BMX-2 supports up to 8 streaming or start/stop tape drives.

Zetaco's full emulation of DG's 60XX and 61XX series disk and 6026 and 4307 tape subsystems means no software patching is required. E^2 PROMs eliminate switches, making drive configurations and functions selectable via downline loaded software. And Zetaco's exclusive backplane cable design is plug-and-go compatible with DG's FCC and non-FCC compliant chassis.



Discover the BMX Series from Zetaco, 6850 Shady Oak Road, Eden Prairie, MN 55344, (612) 941-9480. Telex 290975. European Headquarters: 9 High Street, Tring, Hertfordshire, HP23 5AB, England. (044282) 7011. Telex 827557. ZETACO G.

ZETACO™

Controller Division, Custom Systems Inc.

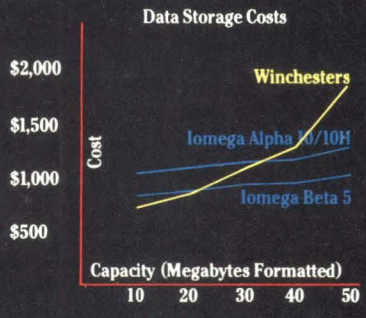
CIRCLE 16

A DECLAR
DATA INDE

When In The Course Of Business Events . . .

OEMs designing systems for today's businesses face two realities. One, data processing is rapidly becoming more decentralized. It is pushing outwards into individualized work units, defined more by job function and applications, performed by more people in more places, demanding more data flexibility—more data independence.

Which brings OEMs face to face with a second reality. Winchesters. Because the prevailing mass storage technology—in the form of large storage units used for access or downloading, or smaller, high capacity desk-top mechanisms—continues to head in the opposite direction. Rather than freeing users to operate effectively in the new environments of distributed data processing, Winchesters keep them device-dependent, keep them tied to a shared system of storage.



Slavery By Any Name . . .

There are lessons here. That the central issue isn't more data, but more data dynamics. And that Winchesters are hardly data dynamic at all.

Consider the aggravations of "wait your turn" access, or the need for lots of "system savvy" on the user's part. Consider the time consumed in backing up and restoring data. And consider the ever-present risk of a system going down or files lost to expensive head crashes.

Now consider the alternative.

IOMEGA HAS REMOVED CAPACI

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ATION OF PENDENCE.

IOMEGA's Distributed Data Storage: Freedom Of Information.

The IOMEGA family of data management/storage systems effectively matches today's distributed data processing reality with a new reality: *distributed data storage.* Because IOMEGA's reliability and performance specs often exceed Winchesters, particularly in access times and transfer rates. And they deliver cost-per-megabyte figures that Winchesters cannot figure at all.

	IOMEGA BETA 5	IOMEGA ALPHA 10/10H	TYPICAL WINCHESTER
Formatted Capacity	5.0 Mbytes per cartridge	10.0 Mbytes per cartridge	10.0 Mbytes fixed
Data Transfer Rate	5.0 Mbits/Sec	9.0 Mbits/Sec	5.0 Mbits/Sec
Average Access Time	50 msec includes settling	35 msec includes settling	85 msec
Form Factor	5.25"	8"/8" Half Height	5.25"

The key is "in/out" simple—the IOMEGA cartridge. Think about downloading data and software to a single 5- or 10-megabyte cartridge, then manipulating, updating, and uploading with maximum convenience and cost efficiency. And think about a total enterprise solution, about storing individual applications, complex software programs, or data sets—all of which can be passed along to others without expensive networking resources. And when you need more storage, you use more cartridges, not more hardware.

Accept No Other Alternatives.

IOMEGA's distributed data storage solutions—in full- and half-height 8-inch 10-megabyte solutions, and a 5-megabyte, 5¼-inch version as well—give OEMs Winchester performance and reliability, and floppy convenience and cost efficiency. They are proven, risk-free solutions. And of the few cartridge opportunities on the market today, IOMEGA's—besides being available—are the only ones that are rugged, absolutely interchangeable, and inexpensive. As such, they give OEMs the most precious commodity of all: *the freedom of designed-in freedom.* The freedom your customers require.

Take The Liberty.

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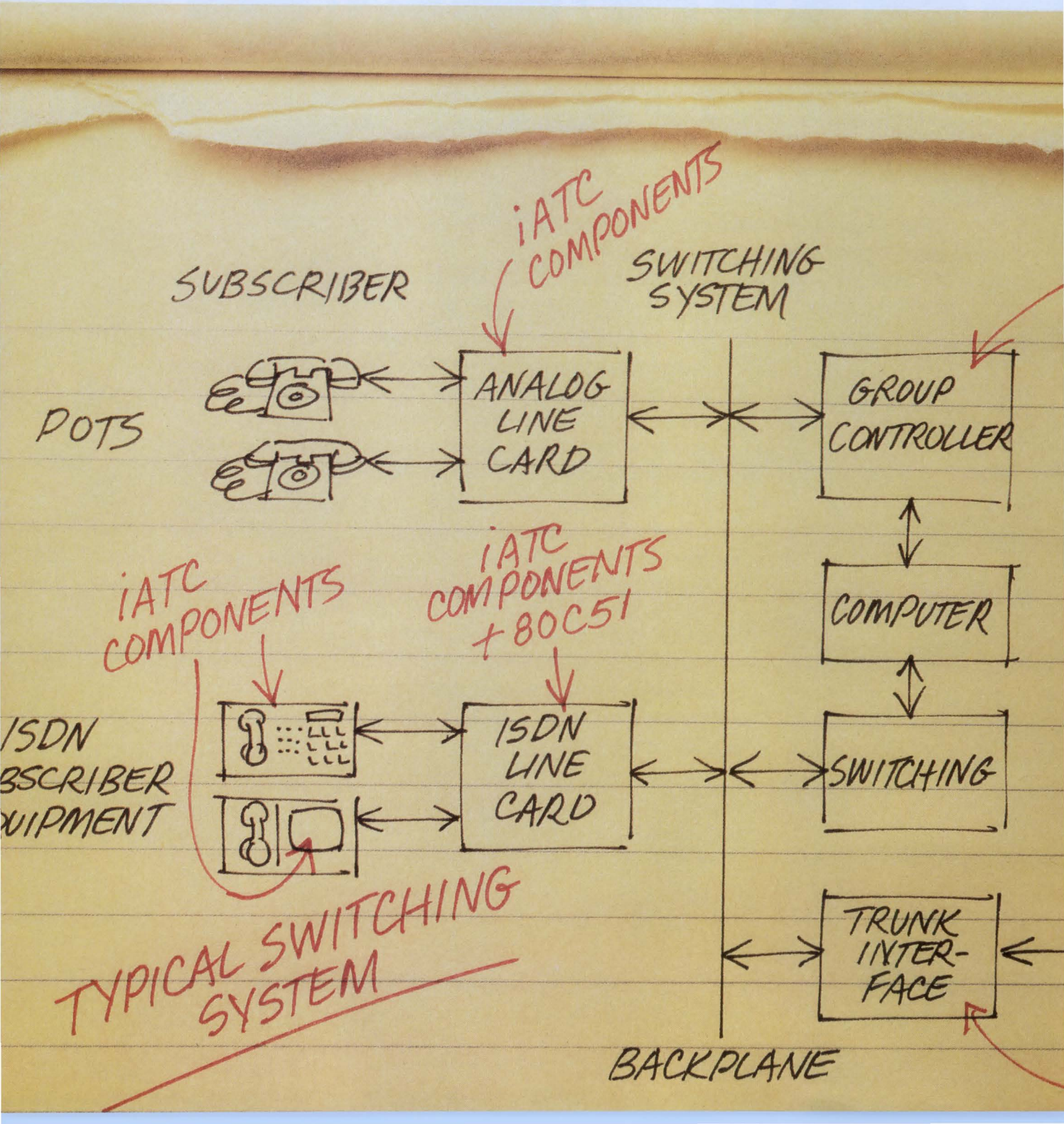
CIRCLE 17

INTEL CHMOS GIVES DATA EQUAL VOICE.



The telephone system of tomorrow will be digital end to end. Able to handle voice and data. Simultaneously.

Today, there's a short-cut to get you there.

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Together, they can handle all pulse code modulation coding and encoding. Subscriber voice channel filtering. Control signaling. And backplane interfacing.

Alone, the 29C51 handles all the analog to digital switching. It's software programmable with a total of 10 features under user control, including transmit and receive gain. You can also program the 29C51 for subscriber line balancing.

It offers a secondary analog channel capable of monitoring an analog subscriber's line.

And internal analog three-way conferencing.

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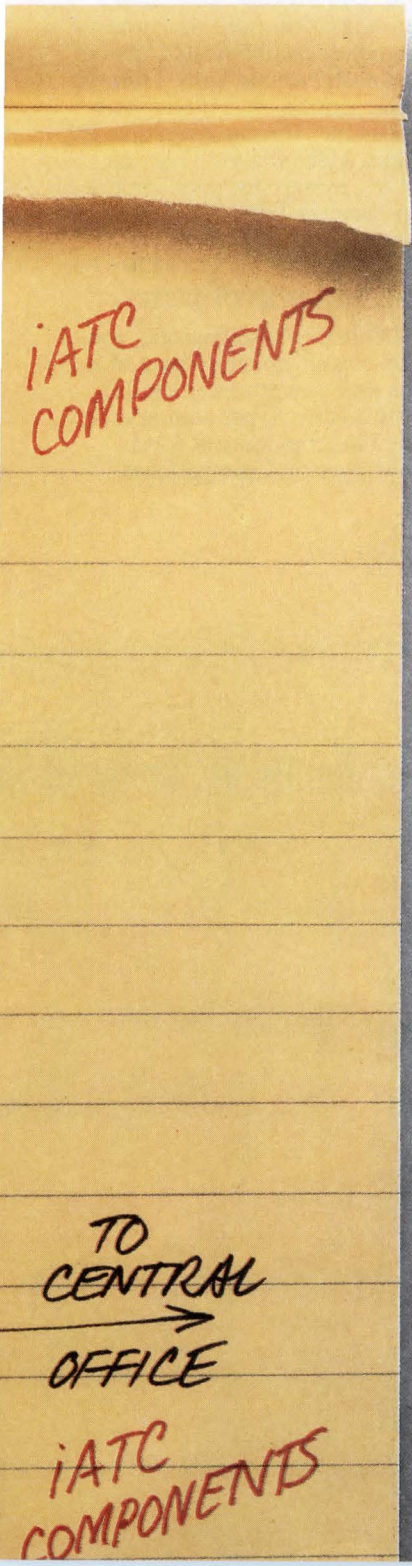
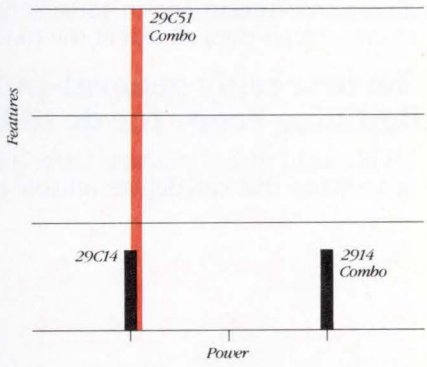
Developed for use with the 29C51, the 2952 Line Card Controller provides the bridge to ISDN upgrades.

It can control up to 16 subscriber lines at once, plus manage all voice and data transfers between the backplane and the line circuits. This includes matching time slots on PCM highways and intelligent interface to a control highway.

Although the 2952 can interface with just about any part of your system it's optimized for use with Intel's 80C51 microcontroller and the Intel iAPX family of microprocessors.





Which means your telecommunication system design can be virtually unlimited in scope.

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CIRCLE 18

Introducing the HP 54100A/D 1 GHz General Purpose Digitizing Oscilloscope.

Now see waveforms you've

The waveform you see displayed here was captured by the new HP 54100A/D 1 GHz Digitizing Oscilloscope. It shows an intermittent extra pulse at the Q output of a D flip-flop. Plus, it automatically positions the event of interest in the center of the display and shows the events in negative time that led up to the trigger. The new HP 54100A/D can easily capture rare events like this and hold them for you to analyze with no blooming or fading. What's more, you get this with 10 psec resolution and 1 GHz bandwidth necessary to capture sub-nanosecond transistions in today's high speed logic designs. And it does all this at the touch of a button.

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With logic speeds pushing faster all the time, you need a scope that can deliver reliable measurement results from dc all the way to ECL. The new HP 54100A/D 1 GHz Digitizing Oscilloscope gives you that versatility. It combines a fast 350 psec rise time with a crystal-controlled timebase, sophisticated on-board analysis firmware, and easily re-configured inputs. It lets you see low duty-cycle signals with clarity and brightness not previously possible. You can even take it out of the lab into production. Make it a vital part of your computer-based ATE test system for even greater productivity and usefulness through HP-IB.

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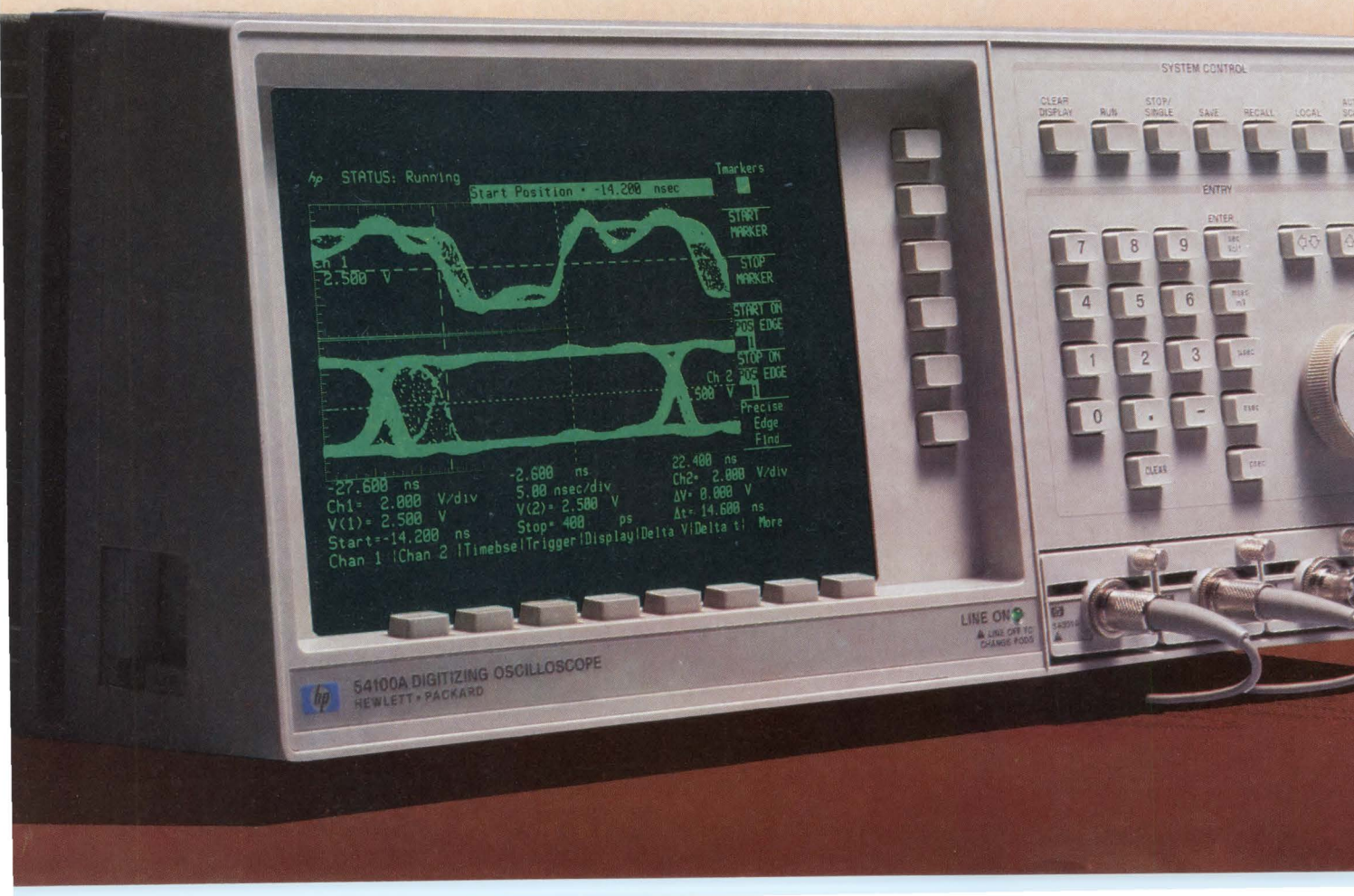
DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.



never seen before.

time-qualified patterns or state, or you can delay the trigger by edge count or absolute time. The HP 54100A/D unloads much of the setup and test burden from you so you can devote your time to designing.

Expanded probing capability and convenience.

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CIRCLE 19

Debugging tools transform CAE environments

Test and verification hardware is making a dramatic entry into the computer aided engineering environment. By supporting the later stages of design, particularly prototype test and characterization, these tools are closing a major gap in the CAE design cycle. While some vendors are providing test tools specifically designed for the CAE environment, others are offering software packages that link existing hardware to workstations or PCs. The end result is that engineers will not have to build complex instrument clusters or fight for time on production automatic test equipment systems to test and verify their designs.

Logic analyzers, pattern generators, and in-circuit emulators are among the tools that can now run under PCs or workstations. Several manufacturers have opted for a modular approach that allows plug-in instruments to function interactively. In this case, one box takes the place of a whole cluster of instruments. Other vendors have developed tools that look more like miniature VLSI ATE systems, complete with fixturing for prototype chips.

Several test tool manufacturers have made nonexclusive OEM deals with workstation vendors. The trend toward nonexclusive agreements will apparently continue. "A wide variety of tools will be available with workstations," predicts Norbert Laengrich, marketing vice president at Hilevel Technology. "You won't see a narrow tie-up where CAE people sign up with just one vendor." Instead, Laengrich says, software packages will allow each workstation to support instrumentation from many vendors.

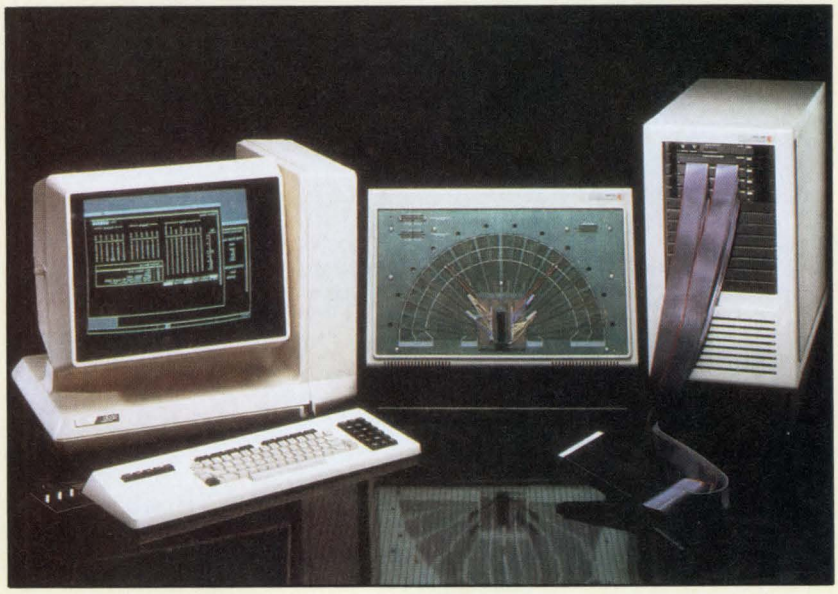
From the CAE vendors' viewpoint, the major issue is integrating a variety of tools into the workstation environment with a common interface. "It's nothing to hook up a logic analyzer to a CAE workstation," says Stephen Swerling, vice president and general manager of Mentor Graphics' Computer System Division. "Integration is what makes a difference to the engineer. We have to give identical human interfaces to simulation and testing." Although Mentor Graphics has an OEM agreement with Northwest Instruments, it is looking at tools from other manufacturers, including Tektronix and Hewlett-Packard, for possible links to Mentor Graphics workstations.

The movement toward CAE test and verification is coming from two fronts—from the test tool manufacturers themselves, and from workstation vendors who want to offer a complete set of design and test services. A flurry of announcements in late 1984 made it clear that test and verification will be an integral part of CAE. In 1985, PCs and workstations will support a much wider range of design and test services, with a growing trend towards automation and integration of diverse functions.

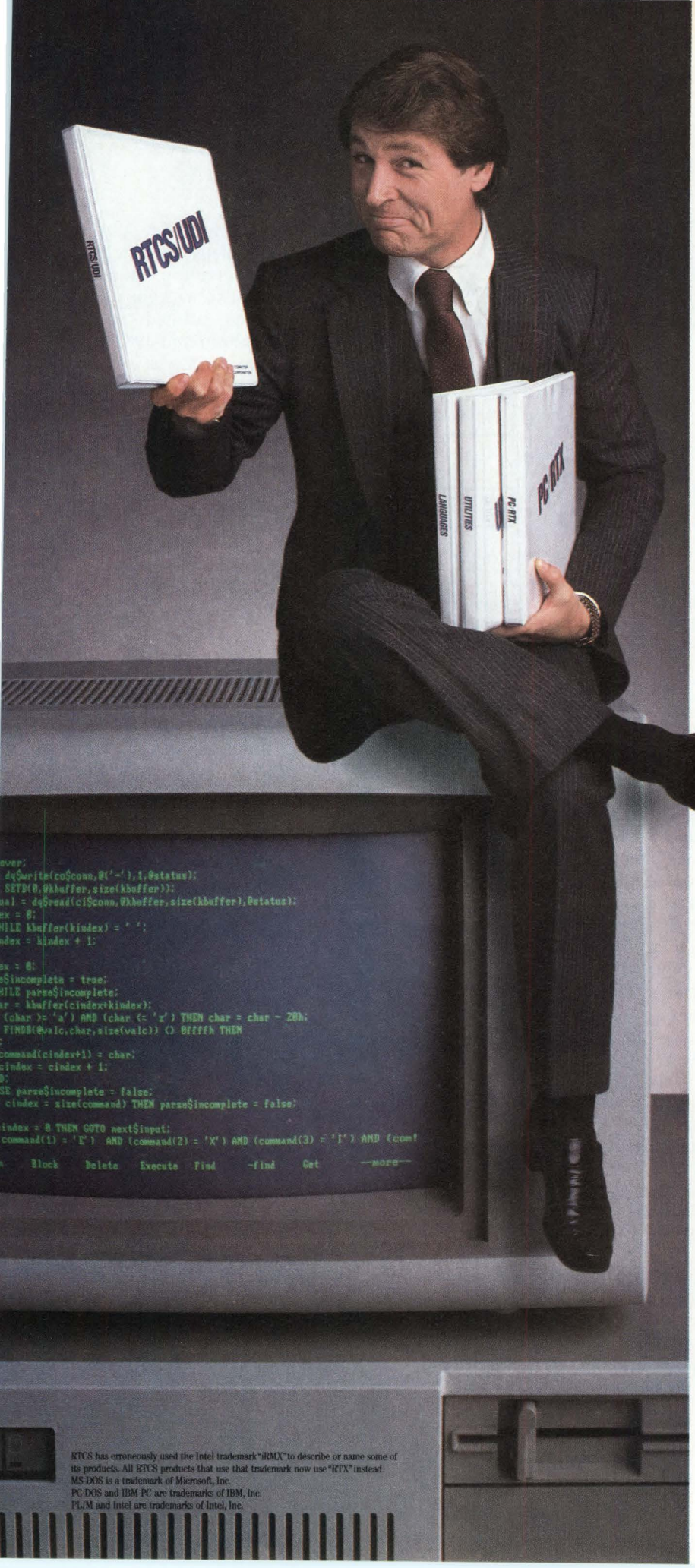
Dynamic prototype testing

The Integrated Measurement Systems' Logic Master brings dynamic prototype IC testing to the CAE environment. Logic Master provides the necessary hardware and software to stimulate the prototype, acquire the

(continued on page 42)



The IMS Logic Master brings many capabilities found in production VLSI testers to the CAE environment. A built-in fixture constructed with plug-in pods is provided for prototype ICs. Logic Master provides all necessary hardware to stimulate the IC, acquire the results, and compare the results to simulator output in real time.



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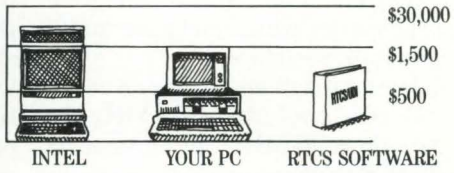

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CIRCLE 20

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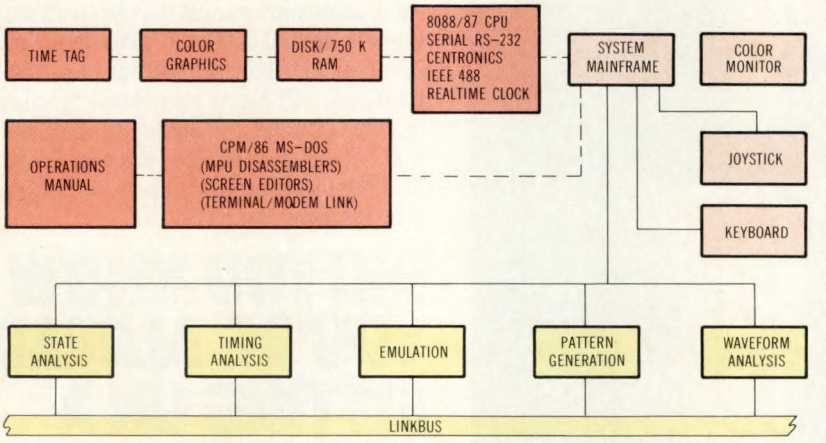
Debugging tools

(continued from page 40)



The modular approach to test instrumentation is illustrated by Nicolet Paratronics' DTS 5000. Plug-in instrument modules include a logic state analyzer, logic testing analyzer, in-circuit emulator, pattern generator, and waveform analyzer.

output, and compare the output to known-good simulator output—all at realtime operating speeds. With RS-232 and IEEE 488 links, Logic Master can use most mainframes, minicomputers, and microcomputers (including the IBM PC) as a host computer. Logic Master can also be linked to any CAE workstation, and IMS is exploring OEM agreements that would integrate Logic Master with simulation under a common interface.

The specifications are impressive: a 1-ns timing resolution, a 20-MHz test rate with a 40-MHz option, and 64 data channels expandable to 384 channels. The system can do ac testing, but not dc parametrics. Logic Master I is priced at $29,200, and is used primarily for functional verification. Logic Master II, priced at $39,300, adds features such as 16 Kbits of memory per channel, and is geared toward detailed engineering evaluation.

In principle, Logic Master is similar to a production VLSI ATE system—at a fraction of the cost. "We have many capabilities of the big systems," says IMS marketing director Ken Lindsay, "but we're not optimized for go/no-go testing. We're providing an interactive design tool." Lindsay says Logic Master is appropriate for "functional characterization," in which engineers bring up their prototypes and manipulate test vectors to find out how it works. However, Lindsay adds, Logic Master is not designed to replace large ATE systems for full VLSI characterization.

One distinctive feature of Logic Master is its built-in fixturing, which is constructed with plug-in pods. Typically, engineers have had to build their own fixtures from probes. IMS competitors such as Tektronix and Northwest Instruments will be watching the IMS approach for possible introduction into their own product line. "We'll have to see if it's really general purpose enough, or if users have to modify it," says Dick Lempke, general manager of the Tektronix Logic Analyzer Division.

Logic Master is also distinctive in that it provides realtime comparison of actual output to simulator output. While some competitors have questioned the value of realtime comparison, Lindsay notes that it gives the engineer much more flexibility. For example, the engineer can program the Logic Master to immediately branch to a diagnostic routine for analysis of a failure.

Logic Master is similar in concept to HHB Softron's Chipchecker, a prototype IC tester available with Softron's Cadat logic and fault simulator. Chipchecker automatically extracts test patterns from Cadat simulations, stimulates the IC, and compares data—but not in real time. Fixturing is provided with universal device under test printed circuit boards. Introduced in mid-1984 as a low cost add-on to Cadat, Chipchecker pioneered the concept of a prototype IC tester linked with a workstation.

Another link to simulation

As a static, functional tester, Chipchecker is inappropriate for devices that have to run at full system clock rates. However, Softron plans to introduce a dynamic prototype IC tester in early 1985. This product will differ from Logic Master in at least two respects—it will operate over an Ethernet link, and it will be sold with the Cadat simulator. Softron's new product, like Chipchecker, will thus be linked to the simulation process from the beginning. At present, Cadat runs on VAX/VMS and VAX/Unix systems, and has been ported to a variety of workstations.

Jim Scharf, Softron's director of engineering, says that no product in the CAE environment will completely replace the need for large ATE systems for VLSI characterization. "You need full speeds and full parametrics, and you're not going to put that on a desktop for under $50,000," Scharf says. "If the GenRads and the Fairchilds can't do it, we can't. What we can give engineers is tools to verify their first prototype. They can then commit to silicon and send their chips to characterization."

Softron is currently looking at a variety of test instrumentations that could be potentially integrated into the CAE environment. Such test instrumentations include the new Dataprobe (Santa Clara, Calif) laser IC tester marketed by Mitsui. This tester uses a laser detection scheme to noninvasively determine the logic states of circuit nodes. "If your design doesn't work once it's cast in silicon, you might want to take a look inside to see what's happening," Scharf says.

(continued on page 44)

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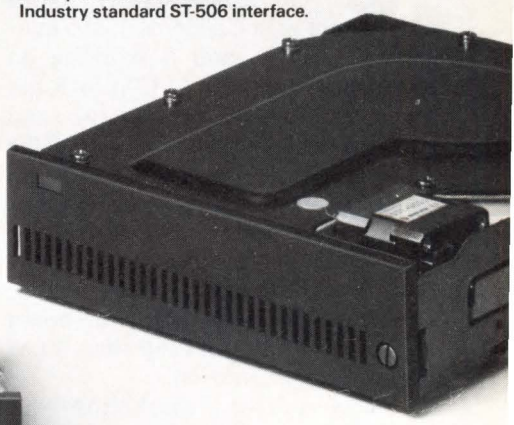

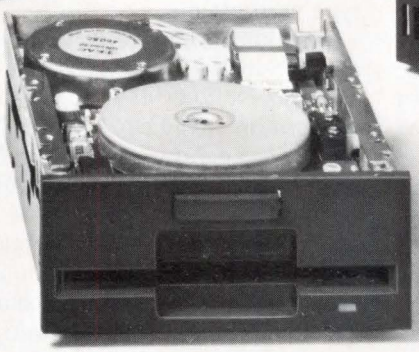

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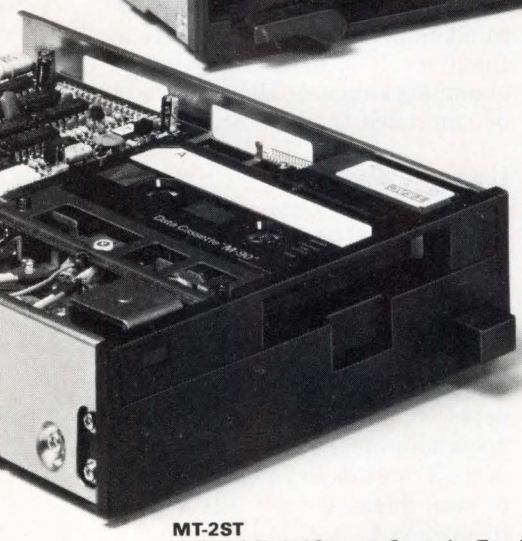

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CIRCLE 21

Debugging tools

(continued from page 42)

Several manufacturers sell modular systems that use plug-in instruments for tasks such as pattern generation and logic analysis. These systems allow instruments to be used interactively, with realtime comparisons between data from various domains. A modular system can replace a cluster of standalone instruments. Users cannot select instruments from different vendors, however, and modular instruments are often not as powerful as standalone instruments.

Specific modular systems

Dolch Logic Instruments can support a variety of instruments with its CAESAR 400, or CAE System Analyzing Resource. The CAESAR 400 is an evolution of the Atlas and Colt analyzers, and it uses the same plug-in instrument modules. Over 30 instruments are available for the four-slot CAESAR, including logic analyzers, pattern generators, word generators, and in-circuit emulators. These instruments can be linked in real time to provide interactive stimulus and analysis.

Dolch has a nonexclusive OEM agreement with CAE Systems to market CAESAR, and is working on VAX and Apollo links. CAESAR has three Z80 processors of its own, and is faster than systems that place all the intelligence at the host. CAESAR can support functional IC prototype testing, with realtime comparison to simulator output, but it is limited to 48 channels. For this reason, CAESAR is more useful for board and subassembly testing than VLSI prototype verification.

Terry Larson, marketing vice president, says Dolch's eventual goal is "iterative, automated design support." This means a CAE system will develop all documentation and test data, run tests, and if requested to do so, modify specifications to match the prototype. For characterization, CAE systems will automatically change test vectors and rerun many types of tests—a process that is now done by hand. Larson sees this type of environment developing over the next 12 to 18 months, "in subsets."

Northwest Instruments' MicroAnalyst workstation consists of an IBM PC AT, Northwest's Series 2000 logic analyzer, and Lotus Symphony software. The system is competitively priced with many standalone logic analyzers.

Nicolet Paratronics' DTS 5000 provides an 8088 processor with a keyboard and CRT, and 12 slots for plug-in instrument modules. The DTS 5000 was introduced in late 1983 as a standalone system, but the company is negotiating possible OEM agreements with several CAE workstation vendors. The system runs CP/M and is compatible with the IBM PC. In a CAE environment, the DTS 5000 can be used for prototype verification.

Instruments currently available for the DTS include a 25-MHz logic state analyzer, a 200-MHz logic timing analyzer, in-circuit emulator, 50-MHz pattern generator, and 100-MHz waveform analyzer. The number of slots an instrument occupies is variable. For example, the timing analyzer includes one control board and up to four memory boards with 16 channels each. One could fill 10 slots with two timing analyzers, and have 128 channels with 200 MHz for each channel.

Hilevel's DS370 Emulyzer initially provided an emulator and logic analyzer, and was oriented to hardware and firmware debugging. A new option, DS370/PG101, provides a 20-MHz pattern generator, which moves the product into the area of VLSI prototype verification. According to Laengrich, the DS370/PG101 is ideally suited for characterization. "We have a lot of features that allow users to change the stimulus or look at the response in a different way. Users can interact very easily. They don't have to know what the device is supposed to do," Laengrich says.

Running off an IBM PC or VAX, the DS370/PG101 has its own 2901 bit-slice processor. Test vectors from simulation can be downloaded to the Emulyzer. The EPL Emulyzer Programming Language allows the test to be controlled by the host computer.

Linking to the PC

Some test tool manufacturers are linking their products to the IBM PC. Although the PC lacks the speed and memory of more expensive workstations, the gap is narrowing with the introduction of the AT. The PC is far more likely to be found on engineers' desks. It also has many nondesign applications that might appeal to engineers. For example, it can keep track of such things as parts lists and bills of materials.

(continued on page 46)

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Disk Emulation	RM02/05, RM80, RP06 (2 drives)	RM02/05, RM80, RP06 (4 drives)	RK06/07 (4 drives)
Tape Emulation	TS11 (4 drives)	TS11 (4 drives)	TS11, TM11 (4, 8 drives)
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Configurable On-Line	Yes	Yes	No
*Single function disk controller			

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SPECTRA LOGIC

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CIRCLE 22

Debugging tools

(continued from page 44)

CAE Verification and Test Tools

Supplier	Product	CAE Links	Cost	Comments
Dolch Logic Instruments (San Jose, Calif)	CAESAR	CAE Systems Workstations	$13,000 to $35,000	Modular instrumentation for design, test
HHB Softron (Mahwah, NJ)	Chipchecker	VAX/Unix, VAX/VMS	$12,000 to $31,500	Prototype IC tester used with Cadat
HiLevel Technology (Irvine, Calif)	DS370/PG101	IBM PC, VAX/Unix	$20,000 to $50,000	Modular instrumentation with pattern generator
Integrated Measurement Systems (Beaverton, Ore)	Logic Master	Any PC or workstation	$29,000 to $39,300	Design verification for prototype ICs
Kontron Electronics (Redwood City, Calif)	KPI	IBM PC	$1500*	Links emulator, logic analyzer to PC
Mentor Graphics (Beaverton, Ore)	HVS	Mentor Graphics workstations	$24,000	Series 2000 logic analyzer, pattern generator
Nicolet Paratronics (Fremont, Calif)	DTS	Under development	$25,000 to $40,000	Modular instrumentation for design, test
Northwest Instruments (Beaverton, Ore)	MicroAnalyst	IBM PC/AT	$17,900	Series 2000 logic analyzer, Lotus software
Tektronix (Beaverton, Ore)	DesignLink	IBM PC, VAX/Unix	$1000*	Links DAS 9100 to IBM PC or VAX

*Does not include instruments or PC

Northwest Instruments' MicroAnalyst Logic Analysis Workstation has 100-MHz Series 2000 logic analyzer, an IBM PC AT, and Lotus Symphony software. Since the logic analyzer does not have a processor, all the intelligence is in the PC. This keeps the cost low—under $18,000, including the AT—but it also makes realtime comparisons and high speed, cross-domain analysis infeasible. As currently marketed, the MicroAnalyst is primarily a debugging tool.

The same Series 2000 logic analyzer is sold by Mentor Graphics as part of its Hardware Verification System. That system also includes Northwest's pattern generator, and a common interface provided by Mentor Graphics. HVS normally comes with a Mentor Graphics workstation, and can be used for prototype test and verification. In the future, Northwest plans to provide a pattern generator with its MicroAnalyst, which would give it capabilities similar to HVS.

In mid-1984, Tektronix announced a software link between its DAS9100 logic analyzer and VAX/Unix systems. An IBM PC link was recently added. According to Dick Lempke, general manager of Tektronix' Logic Analyzer division, the only real constraint with the PC is that it might have less memory for a given task. The PC is used as a front end to load test vectors into the DAS, which has its own Z80 controller.

The DAS can stimulate a prototype IC and compare the results to simulator output. Unlike Logic Master, it does not provide realtime comparisons or built-in fixturing. However, Lempke notes, the DAS is a general-purpose machine with many applications other than functional prototype testing. And for users who already have a DAS and a PC, the DesignLink package that ties them together costs only $1000.

Kontron Electronics has introduced hardware and software that links its KPA logic analyzer and KSE emulator to the IBM PC. The hardware interface is provided by a Z80-based Kontron Personal Instrumentation card, which is mounted in the PC. Disk-based software includes MS-DOS utilities, CP/M utilities, and cross assemblers. The entire package sells for $1500. Kontron is also looking at possible links to CAE workstations.

Although test tool manufacturers are jumping into the CAE marketplace, they are not about to abandon standalone instrumentation. One manufacturer that intends to enter the CAE market, while remaining strong in standalone instrumentation, is Gould's Design and Test Systems Division (Santa Clara, Calif) "CAE is a solid market segment, and it's going to grow fast," says Bruce Hansen, marketing manager for logic analyzers. "But the standalone market won't go away—it will grow at a steady rate. Manufacturers always chase after the latest, hottest, brightest new thing, but you can't ignore your base business." For Gould, as well as other manufacturers, the real focus will be on improving performance, both within and outside the CAE environment.

—Richard Goering, Field Editor

SYSTEM TECHNOLOGY

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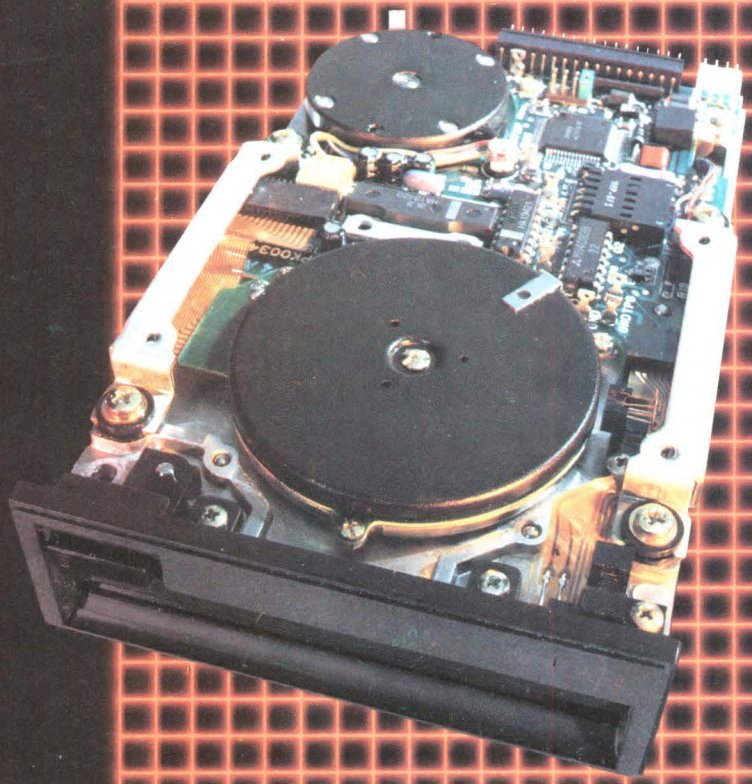
Panasonic 3½" Floppy Disk Drives



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CIRCLE 25

Integration fuels personal computer hardware advances

Advances in personal computer hardware will result from the fusion of new materials with semiconductor technology. This fusion will affect a broad range of products including printers and plotters, sensor technology, displays, and personal computer architecture. According to Susumo Aizawa, senior managing director at Epson Corp (Torrance, Calif), these developments will employ three key technologies: high precision LSI, thin film, and ultrahigh precision mechanical processing. This fusion of different materials, says Aizawa, will result in "hardware taking on new forms, doubtlessly changing the form of the personal computer."

The Japanese coined the term "mechatronics" to indicate the combination of mechanical and electronic engineering. Thus, references to integration in this context involve more than ICs—they mean the combination of new types of materials and semiconductor materials. Aizawa has now begun to speak of a process he calls "supermechatronics," which will take advantage of developments in all three areas mentioned above.

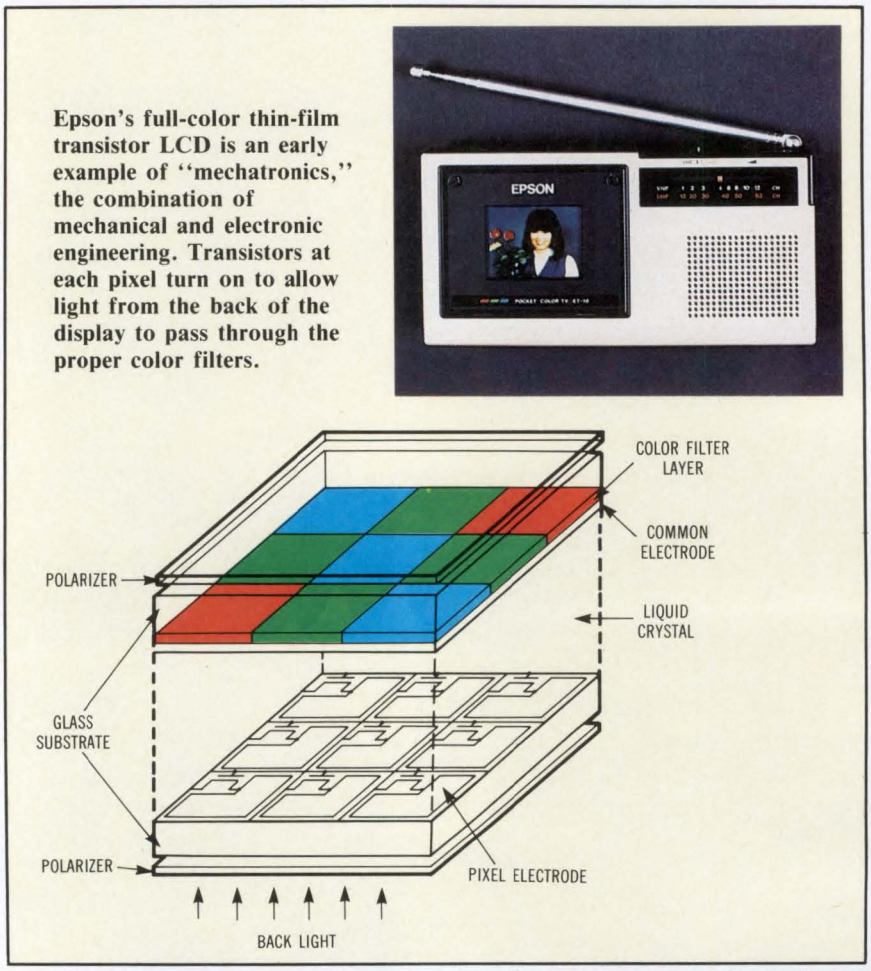
One goal of high precision LSI is to increase processing speed. But, Aizawa points out, "Power consumption will grow in proportion to the second or third power of speed. Therefore, gains in speed of more than four- or fivefold are unrealistic." Techniques to reduce the operating energy of individual elements represent an "intermediate solution," and "real increases in information processing speed require a switch from serial to parallel processing." But, this architectural approach to increasing speed depends on the availability of high precision LSI in the "mechatronic" sense.

Aizawa sees thin-film technology as one of the major avenues for integrating silicon semiconductor material with coatings of complex metallic alloys and new materials, many composed of rare earth elements. "Processing for other than semiconductors has hitherto been limited to the so-called electronic 'passive' elements, but this must now be extended to include nonlinear and active elements," he says. Thin-film technology has already expanded beyond its well-known applications in disk drive heads and media to nonimpact printer heads (both ink jet and magnetic). It is also used in LCDs based on active matrices of thin-film transistors—each pixel in the display is an active element.

Ultrahigh precision mechanical processing is a third key element in the mechatronic integration process. According to Aizawa, "Tolerances down to the submicron level. . . will be necessary for the interfaces in transducers working between different physical qualities—light, magnetism, electrons, etc." For example, optical communications require that optical cable connectors be within tolerances of 0.1 micron.

These technology trends will heavily impact personal computer products. In printers, for example, Aizawa predicts nonimpact printers with high speed, high resolution, and color may outpace the dot-matrix impact printers by 1986. The three nonimpact technologies currently showing the most promise are ink jet, thermal transfer, and optical printing. But, says Aizawa, none are now capable of coping with all print requirements. Thermal transfer, for

(continued on page 56)



Epson's full-color thin-film transistor LCD is an early example of "mechatronics," the combination of mechanical and electronic engineering. Transistors at each pixel turn on to allow light from the back of the display to pass through the proper color filters.

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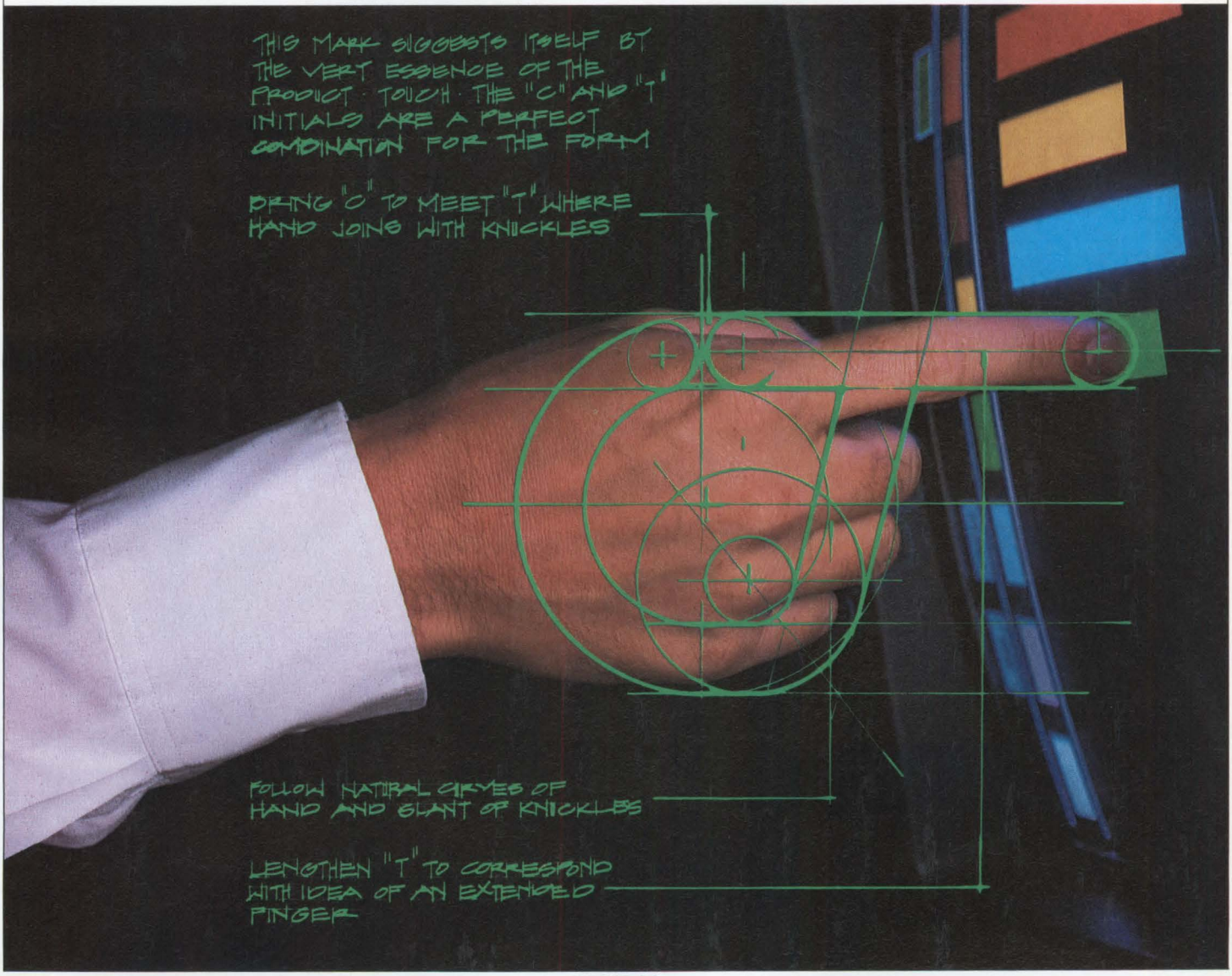

CIRCLE 26

Integration fuels advances

(continued from page 54)

example, is low cost, but it is slow. Ink-jet technology holds great promise for high resolution, but it also has a speed limitation.

Aizawa sees the solution to the speed bottleneck of ink-jet printing in the integration process. Developing a bank of 2000 nozzles would allow the ink-jet printer to achieve speeds comparable to those of optical printers. This development, however, could take up to five years. "And, it will take just as long to develop a color printer for personal computers that will use optical printing," notes Aizawa.

Sensors, or input devices other than alphanumeric keyboards, will develop well beyond the level of the mouse, which Aizawa calls "little more than a toy in comparison with a true sensor." While voice input of any practicality or reasonable cost appears to be many years away, line sensors for inputting characters and graphics seem feasible outcomes of the LSI process. "I would like to see the early implementation of input by pattern recognition equipment," says Aizawa.

According to Epson's Susumo Aizawa, by 1986 we can expect to see the printer market moving toward nonimpact printers, higher speed, higher resolution, and color.

Epson has done a great deal of development work in LCD technology including a commercially available 80-char, 25-line display and a color TV with a 2-in. LCD. The latter is an example of the integration process, which produced an active matrix of 57,600 thin-film transistors on a quartz glass plate. It is hardly surprising, then, that Epson sees a bright future for LCDs.

Aizawa predicts that although the CRT will dominate the market for the next five years, during that time flat panel displays will appear with a size, resolution, and price equivalent to CRTs. This will have two results. First, CRTs will become bigger and slimmer, with even faster response time and higher resolution than at present. Second, Aizawa predicts that "in the 1990's, the CRT will give way to the flat LCDs." Several factors will have to develop in concert to push these results along: contrast and diagonal size must improve, as well as resolution and response speed. Thus, in addition to developing thin film technology, which enables the

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placement of so many transistors or diodes on a large glass surface; fine chemical technology must also progress toward producing a far more sensitive liquid crystal material.

The effects of these technological developments on personal computers will be influenced by consumer demands. Aizawa doubts that the portable computer will be readily accepted by consumers. He defines a portable computer as one that "a 10-year old child could carry for at least one mile and that operates on the order of 10 hours on its own batteries." To date, however, no such portable computer incorporates the full architecture of a professional computer. "That is," says Aizawa, "an 80 x 25 12-in. screen, a 16-bit CPU with 128-Kbyte RAM, two 320-kbyte floppy drives, and an MS-DOS, CP/M-86 or Unix operating system." Portables suffer from poor screen display and higher cost. Unless these problems can be overcome, Aizawa feels, portable computers may be relegated to more specialized market segments than desktop units.

Whatever the possibilities offered by developments in technology, the market force of the personal computer will not be strong enough to carry them through alone. The much larger consumer market for TVs, VCRs, and other products using magnetically processed images, and for copy machines and cameras (what Aizawa calls the video processing industry) will help make the technical developments cost effective.

For example, Aizawa points out, "The existence of the TV industry, with an annual production of 40 million units, provided the inexpensive CRT display monitors that made the spread of the personal computer possible." Similarly, the small, high capacity floppy disk drives are the results of technology transfer with video recorder technology; LCDs started with watches, and so forth. Consequently, the manufacturers of video processing products may also be the manufacturers of computer peripherals. "To be frank, Epson's development of the world's first LCD color TV sprang from this realization," says Aizawa.

Linking computer technology to these much larger markets makes a developing technology less expensive and speeds its progress. If the flat panel were of use only to computers, the volume of flat panel displays might represent at best a quarter of the market for TV sets. "However," adds Aizawa, "if the flat panel can be introduced to both markets—personal computers and TVs—the situation becomes very different."

—Tom Williams,
West Coast Managing Editor
SYSTEM TECHNOLOGY
(continued on page 64)

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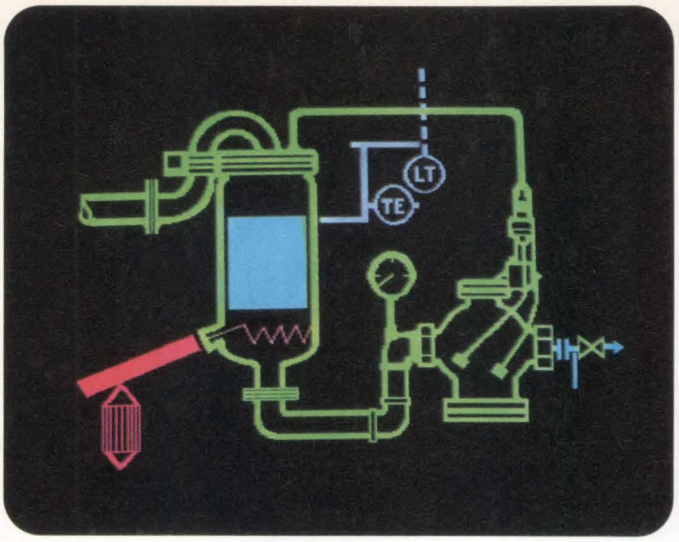

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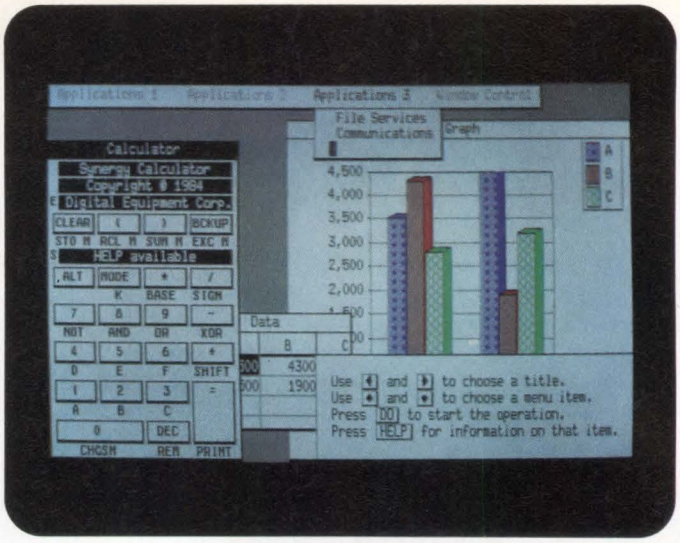

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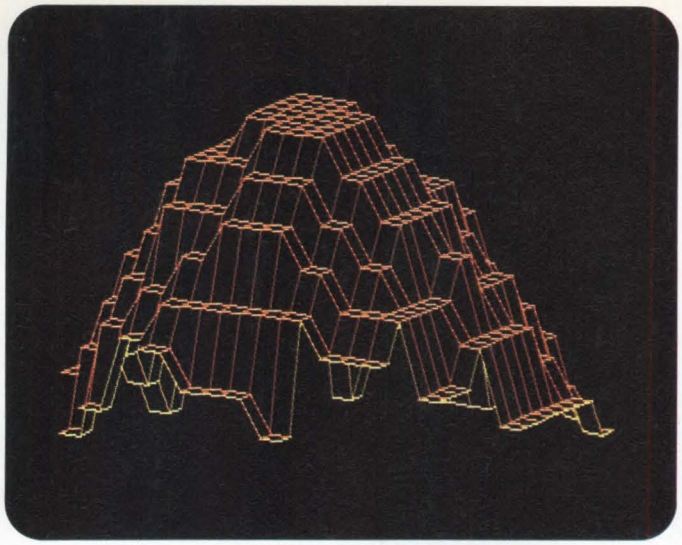

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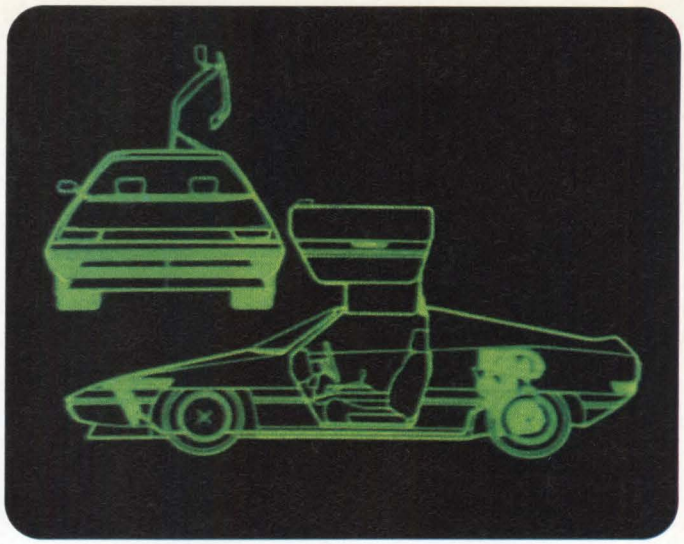

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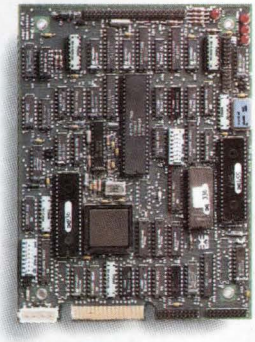

MEDALIST ST506/SCSI DISK CONTROLLER.

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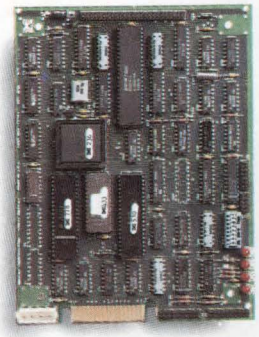

CHAMPION ESDI/SCSI DISK CONTROLLER.

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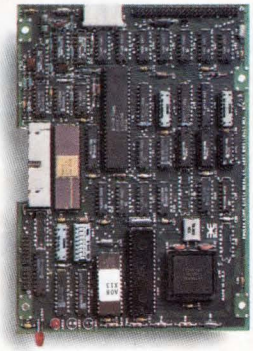

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CIRCLE 30

There Are Only Two Things New Tested Pairs

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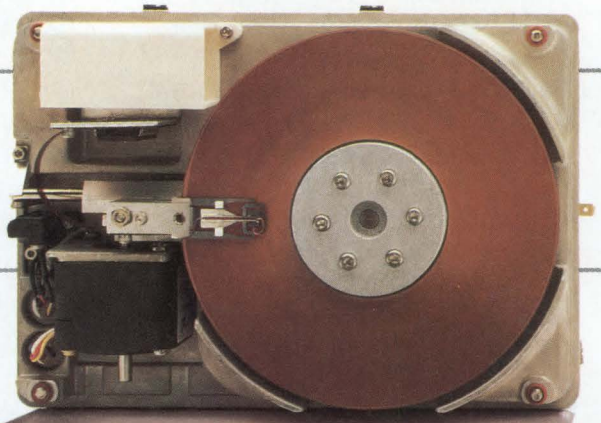

OEMs face major problems trying to decide which hard disk drives to build into their microcomputer systems. What with the wide range of drives, and so many hidden costs associated with evaluation, testing and integration, the process becomes a time-consuming and costly hassle.

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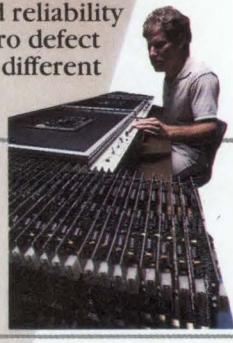

It's simple. Tell us which drives you're considering and we'll test them on Xebec-designed equipment against the most rigorous standards in the industry. Standards we at Xebec have set. Then we'll tell you which of our controllers is the best match for that drive—or we'll customize a controller for you—and accelerate your time to market.

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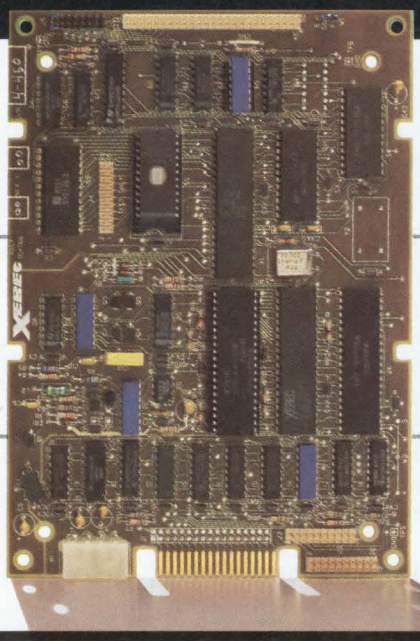

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CIRCLE 31

Machine vision technology is coming of age—but it's not here yet

Limited capabilities of current machine vision systems have forced nearly all system manufacturers to concentrate on refining a single task, or at best two of four basic tasks. At least one company, however, now offers a system that it claims is diverse enough to do any of the four.

The first of these machine vision tasks is recognition—identifying what the object is. Second is inspection—determining how good it is. Third is gauging—calculating what size it is. And the fourth is guidance—figuring out where it is, or where it should go.

According to its director of marketing, Pattern Processing Technologies of Minneapolis, Minn is one of the few manufacturers with a system that defies the need for specialization. Arne L. Watland says that his assessment is founded on a unique feature of the company's APP 90 system. The APP 90 is the only hardware-based machine vision system now available, he maintains.

Not only does the hardware base permit versatility, Watland says, but it provides what he claims to be the fastest speed of any system. A simple task, the analysis of a very small, singular window, for example, might require only 4 ms. Such a task would tell only where the window is and what is in it. However, very few tasks of far greater complexity would take more than 30 ms. "Software-based systems cannot provide these speeds or the ability to perform multiple tasks," Watland says.

The system uses a statistical analysis technique, according to systems engineering manager, Craig Valenty. A random statistical evaluation is first made of a number of pixels within a given window. From that, a "fingerprint" is generated to identify what is being viewed. The rest of the process is proprietary, Valenty says.

System accuracy results from use of 256 encoders. Each encoder performs a statistical analysis of a specified area. It provides resolution up to 1 pixel within a 4- x 4-pixel window. One encoder would ordinarily be assigned to one window. When fewer than 256 windows are being viewed, however, several encoders could be assigned to each window.

There is only one processor in the system, according to Valenty. A communication processor that acts as a traffic cop controls communication between the processor and the outside world (eg, an interface with the robot and the CRT).

Although most machine vision systems perform only one of the four basic tasks, Dr Alan Strelzoff (director of machine vision products for Analog Devices in Norwood, Mass) said the company's IVS-100 system can handle two of the four: recognition and gauging. He admits a basis exists for the specialization theory, however. If an Analog Devices' system were used for something other than its original purpose, for example, new software would have to be written.

Strelzoff points out that the IVS-100 is in the middle of the range between very low cost/low processing power and very high cost/high processing power systems. The system, therefore, is specialized. It cannot do everything, but it is not meant to.

Machine Vision International of Ann Arbor, Mich has organized its Genesis 4000 vision processing algorithms on principles of what the company calls mathematical morphology. Marketing manager Don Vuchetick defines morphology as the use of shapes to probe the spatial nature of digital images. Gray scale processing occurs simultaneously across entire images. This enables the user to filter out information that would interfere with locating defects.

The Genesis system could be used in the second of the vision tasks—inspection. Speed depends on the application, according to MVI marketing communications specialist David J. Gayman. In a robotic application involving six degrees of freedom, for example, a complete cycle is unlikely to require more than 10 s.

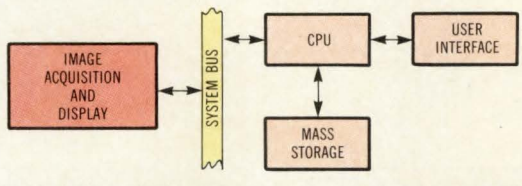
Cameras are bottlenecks

Machine vision systems have four basic sections: image acquisition, CPU, mass storage, and user interface. Capabilities of the last three sections are almost always greater than those of the first, which in essence is a camera.

Most machine vision systems could provide greater speed and resolution if not for the limited capability of current cameras. Camera quality is particularly critical for two-camera systems that provide three-dimensional viewing.

Pattern Processing Technologies has spent a lot of time investigating how to bypass the camera bottleneck, according to Watland. "Many of the present cameras have such a narrow gray level representation that they miss the outer edges of the item being

(continued on page 66)



In basic operation, a typical machine vision system acquires, digitizes, and processes video information. Digitized information from the image acquisition subsystem is analyzed by the CPU that is based on computational algorithms developed for a specific application. Results are presented to such devices as a host computer or production line equipment.

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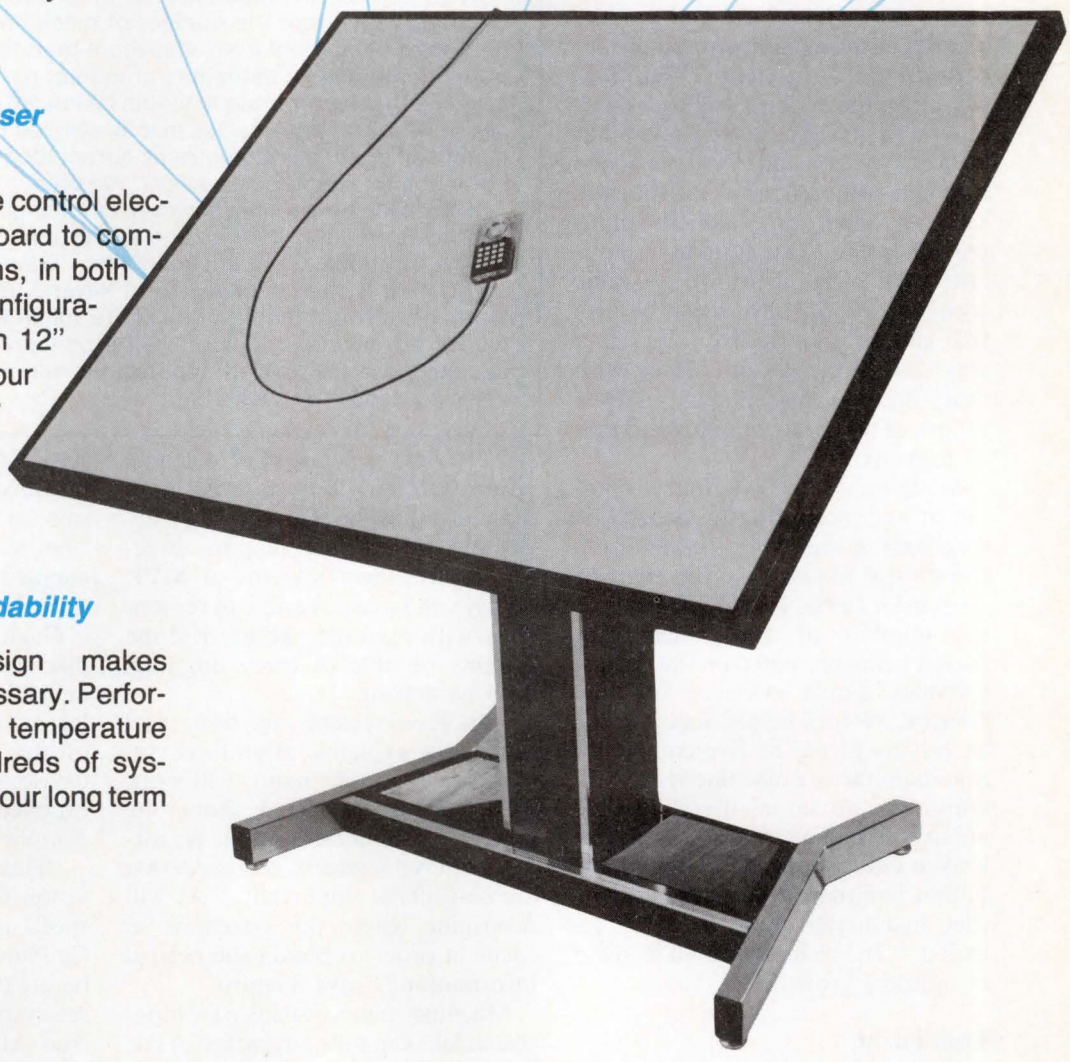

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CIRCLE 32

Machine vision technology

(continued from page 64)

studied," he says. The PPT system is definitely "camera-limited."

Analog Devices, for one, is doing something to bypass this problem. The company recently entered into a joint agreement with a camera company in France to develop a camera specifically for machine vision applications, according to Strelzoff.

Strelzoff also predicts changes within the machine vision industry during the next few years. "Progression of machine vision architectures will gradually make machine vision systems look more and more like vision systems, and less and less like general purpose microcomputer special software," he claims. That does not mean the systems will ever emulate human vision, however. "What we want to do is make vision systems that can comprehend what they are seeing by incorporating artificial intelligence into those systems," Strelzoff says. "But when we get done with that, we will have vision systems that can do quantitative things in a way that humans can't. Even with that, the systems will have limited ranges of activities compared to that of humans."

Machine vision is definitely coming of age, according to George R. Gagliardi, a senior consultant at the Cambridge, Mass research firm of Arthur D. Little. He said he believes the number of conferences and papers being presented on the subject provides ample evidence of this. General Motors helped legitimize it by buying pieces of five companies that manufacture machine vision systems with an initial investment of about $50 million. "Other companies look at GM and decide that if an $80 billion company has invested in it, they had better study it, too," he added. "The result is a rapid increase in industry growth."

Need for AI

There is almost universal agreement among machine vision experts that artificial intelligence will be a major factor in the growth of machine vision technology. The only disagreement centers on when AI will be developed sufficiently to be incorporated.

"The next generation of machine vision systems will have to do more than just low level processing, according to Dr Linda Shapiro, director of intelligent systems at MVI. "They will have to be able to reason. Only with reasoning ability will the systems be able to carry out high level processing."

Low level systems are now pixel based, she explains. High level systems, on the other hand, will work with entities extracted from the image. Those entities might be surfaces or even segments of images that are considered important. "AI will determine where the system is to focus in order to obtain the needed information," says Shapiro.

Machine vision systems now in research labs can take advantage of AI, Shapiro claims, even though that is not true of commercial systems. Experimental machine vision systems that use AI now exist, she adds.

Analog Devices' Strelzoff agrees that AI will be very important to the development of future machine vision systems. But he disagrees with Shapiro on the question of timing. Strelzoff says he is somewhat less optimistic, "but we will have some aspects of AI coupled with vision before the end of this century."

Gagliardi says far less stress is placed on AI. "Ultimately [AI] can help a lot. But the industry won't be lost without it," he maintains. Part of [its use] will be in application development. Right now you need an experienced person who understands complex techniques.

"Having an expert system with vision as an input would probably speed up the development cycle," Gagliardi adds. "I would say that before the end of the decade you will see systems out there that are using true AI. But right now the vision companies are more concerned about establishing a market base than they are about getting AI into the system."

—Sydney F. Shapiro,
Managing Editor
SYSTEM TECHNOLOGY

(continued on page 72)

Machine vision system sees expanding market

Applications for machine vision are growing in number—and so are the number of companies making machine vision systems. Today's online machine vision systems evolved from experimental versions developed at such organizations as General Motors' Research Lab and at universities around the world. As such, they are far more sophisticated than their predecessors.

Estimates of the number of firms now making machine vision systems vary widely, but most indicate a range of from 50 to 200 companies. The actual number depends upon definition of machine vision itself. According to George R. Gagliardi, a senior consultant at Arthur D. Little, "the market is growing steadily. An increase of 50 percent a year for the next couple of years is not unrealistic."

In a report still in preparation for the Cambridge, Mass research firm, Gagliardi notes that the number of machine vision system manufacturers has catapulted from 30 to more than 150 in just four years. "Part of the confusion [in estimates of market participation] is that a lot of systems that incorporate machine vision are not really machine vision *per se*. Many companies use machine vision in their products, but they might call themselves electronic automation companies, for example, not machine vision companies," he says.

Increased competition, however, is forcing manufacturers to differentiate their products by focusing on systems built for specific markets and applications, Gagliardi maintains. "Vendors have been burned trying to modify their systems to fit several uses. So now that there is more interest out there [for machine vision systems], the vision companies are providing customized products. Machine vision systems designed for specialized applications will account for 70 percent of sales by 1988," he predicts.

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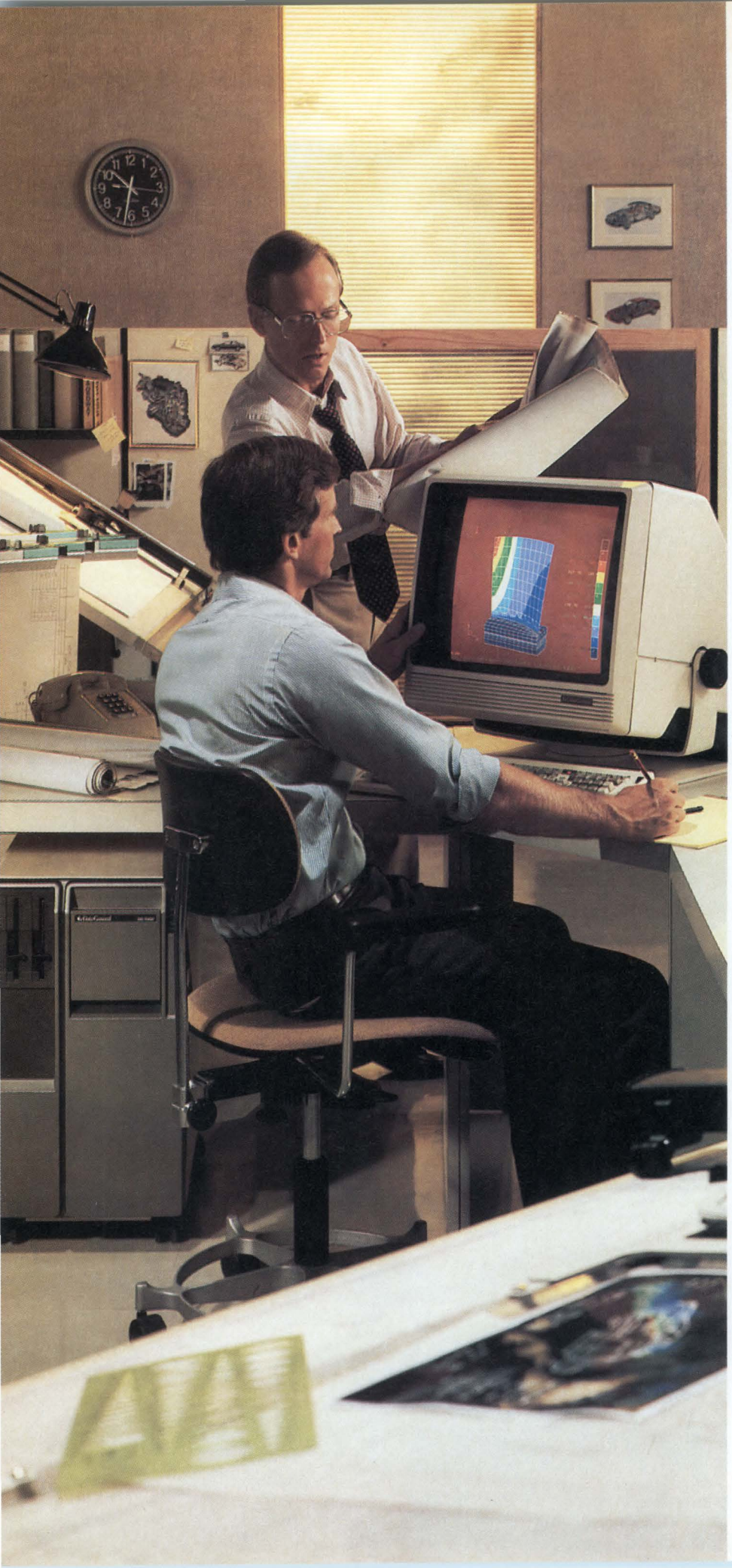

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◀ **Improved memory efficiency** is produced by the unique multiport architecture of TI's new TMS4161 Video RAM. It increases memory system functionality while reducing system size and cost for applications such as this advanced Data General engineering work station.

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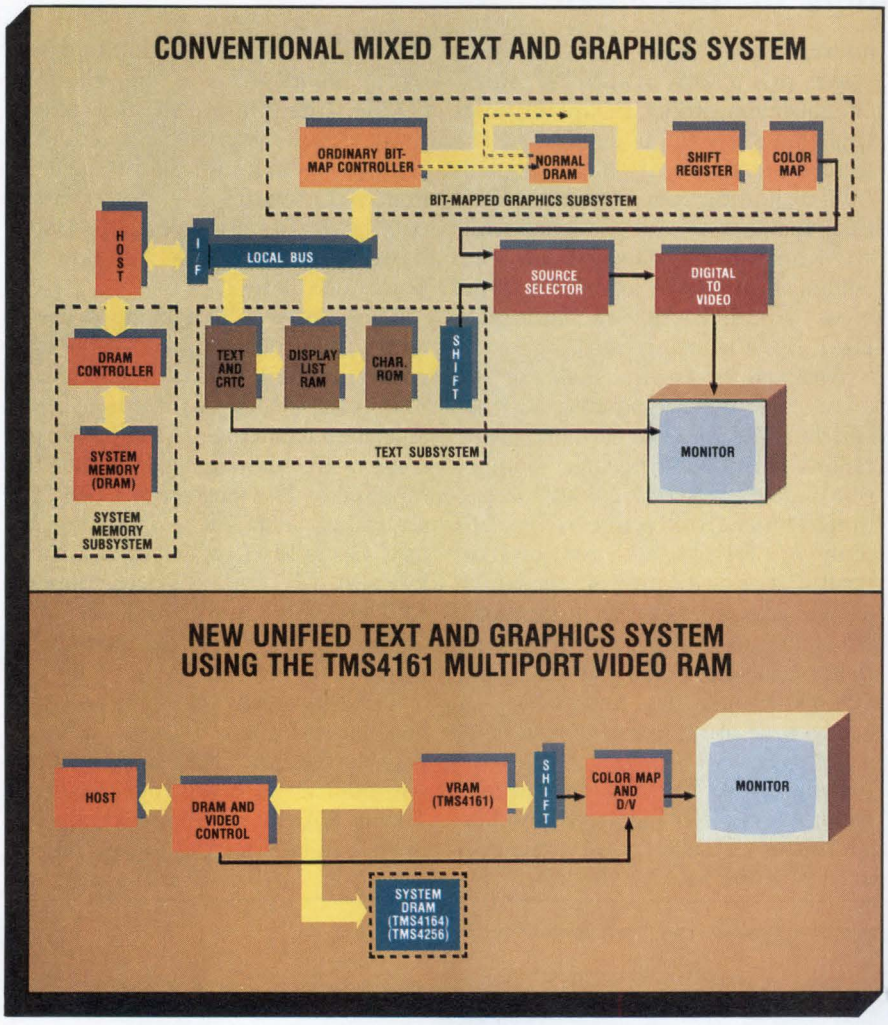
video memory bandwidth with TI's new Multiport RAM.



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CIRCLE 33

Gallium arsenide technology on the move

GaAs digital IC technology continues to advance rapidly. Real strides forward are taking place both in the laboratory and in real-world manufacturing. These developments, exemplified by progress in GaAs RAMs, are also evident in the commercial market activity taking place in GaAs arrays and logic devices. Although MESFETs continue to be the most common device, researchers are examining other types of circuits. Researchers hope that bipolar ECL technology will lead to even faster GaAs circuits. Finally, there is much activity in packaging and manufacturing technology as GaAs gets closer to high volume commercialization.

GaAs RAMs

At the recent 1984 IEEE GaAs Symposium held in Boston, researchers from Nippon Telephone & Telegraph (Atsugi, Japan) described a 16-Kbit GaAs static RAM that was designed using direct coupled FET logic. With more than 100,000 FETs, it is the largest GaAs IC yet produced. The device has minimum address access time of 4.1 ns and power dissipation of 2.52 W. Both enhancement-mode (E-mode) and depletion-mode (D-mode) MESFETS were fabricated using a self-aligned FET technology developed at NTT. Each memory cell was designed with six transistors composed of one enhancement/depletion (E/D) type cross coupled flipflop and two DMESFET transfer gates.

Although access time is shorter by a factor of 4000 compared to 16-Kbit silicon ECL SRAMs, its developers remain unsatisfied because simulation had predicted a 2.06-ns access time. This shortfall is due to the scattering of FET threshold voltages that results from dislocations in the GaAs crystal. Experiments with dislocation-free material confirm that the speed increases as predicted. Despite that, 100,000 transistors and a 4.1-ns access time are impressive results in a GaAs IC.

Progress in the allied cryogenic technology, High Electron Mobility Transistor (HEMT), was represented in a 4-Kbit SRAM described by Fujitsu Ltd (Atsugi, Japan). Operating at liquid nitrogen temperatures (77 °K), the GaAs/AlGaAs selectively doped heterostructure device exhibits a minimum address access time of 2 μs with 1.6-W power dissipation. At room temperature (300 ° K) access time is 4.4 ns with 0.86-W power dissipation.

The selective dry etching process used for the development of the circuit results in highly uniform device parameters, such as threshold voltage. This technique, however, causes some wafer damage, which can be repaired by low temperature (400 °C) annealing. The 4-K x 1-bit SRAM uses D-mode HEMTs for load devices with E/D type direct coupled FET logic used for the basic memory circuit—a six transistor, cross coupled flipflop.

The 2-ns speeds were obtained, according to Fujitsu, by using 1.5-μm gate devices and 3-μm design rules. Although 2 ns is the highest speed 4-Kbit RAM ever reported, developers estimate that the address access

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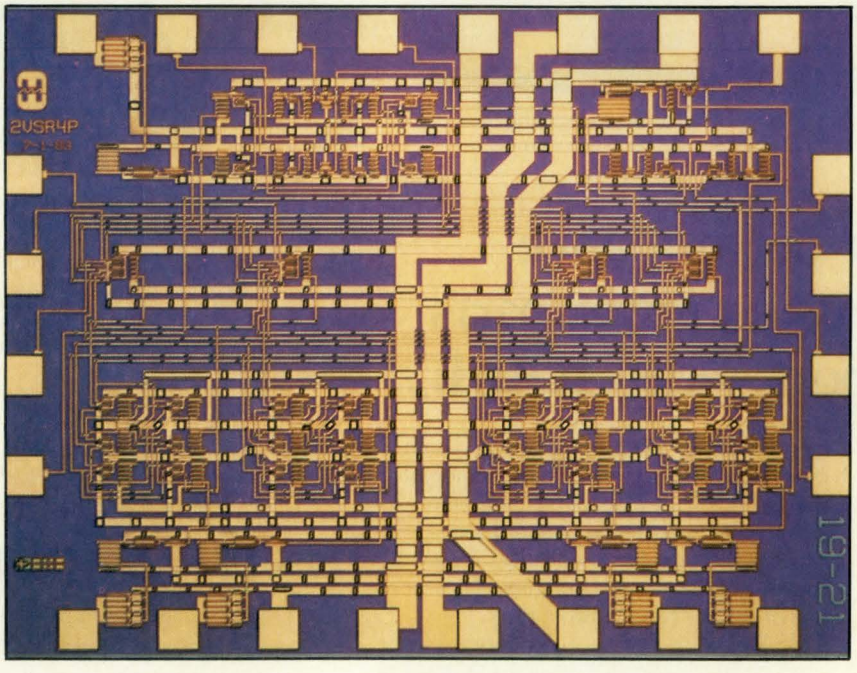

The HMD-11141-1, a 1.4-GHz, 4-bit shift register from Harris Microwave Semiconductor, represents the new breed of ultrahigh speed logic circuits designed in GaAs. The ECL-compatible chip is packaged in a hermetic flat pack to minimize parasitics and cross talk.

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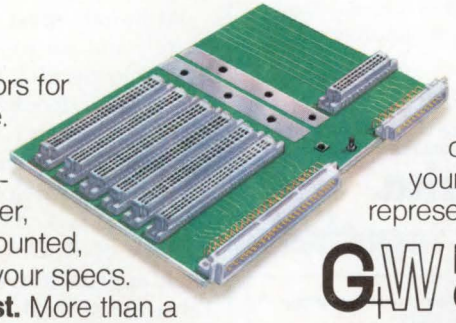

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CIRCLE 34

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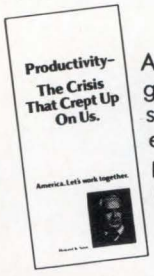

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Gallium arsenide technology

(continued from page 72)

time can be improved to less than 1 ns by using 1-μm gates and 2-μm design rules.

Like silicon memory, GaAs memory is in the forefront of process technology. For commercial circuits, however, we must look elsewhere. No GaAs memories are available in the commercial market. Only three companies presently offer GaAs digital circuits in the marketplace. They are Gigabit Logic, Inc, with a line of logic circuits; Harris Microwave Semiconductor, offering logic and cell arrays; and Tektronix, with MSI cell arrays.

GaAs logic circuits

The Tektronix Quick Chip array, described by Louis Perque of Tektronix (Beaverton, Ore), is a DMESFET array that can integrate both digital and analog functions. The 80 x 80 mil array contains 28 corecells that can each contain 2 gates or 1 latch. The array has 24 I/O cells and pads. Typical gate speed is 190 ps at 10 mW per gate. I/O power ranges between 25 and 50 mW and total nominal chip power is 2 W. Circuits can be fabricated that use clock rates up to 2- and 5-GHz analog bandwidths. The cell library of logic gates, macrofunctions, and I/O buffers contains over 60 corecell and I/O cell designs. The I/O cells interface with ECL, CMOS, or TTL.

Although most of the GaAs research and all of the commercially available circuits, to date have used MESFETs, Rockwell International Corp (Thousand Oaks, Calif) has expanded the technology by applying heterojunction bipolar transistors to SSI digital ICs. As reported by P.M. Asbeck of Rockwell, the use of an ECL approach allowed engineers to fabricate several circuits that prove the benefits of bipolar circuitry. The circuits include ring oscillators with 40-ps gate delays, frequency dividers with 8.56-Hz input frequency, and a 4-bit pattern generator operating with 2-GHz clock and nonreturn to zero data rates of 4 Gbits/s. Most of the circuits were based on current mode logic where current is steered between alternate paths according to the gate input states. Developers claim that the transistors display a better transconductance than that of FETs and cutoff frequency as high as 40 GHz—both excellent results.

Uniformity of threshold voltage was much better than MESFETs or HEMTs. Since nonuniformity of threshold voltage from one transistor to the next is a continuing problem with FETs, this was a very important finding. The smaller deviation in threshold voltage that was observed appears to be process related rather than the result of dislocations in the GaAs as is the case with FETs. Yields at wafer probe have been as high as 90 percent. Such yields coupled with high speeds and the adoption of unmodified silicon circuits portend a bright future for GaAs heterojunction bipolar transistors.

GaAs IC technology is now mature enough that practical problems are beginning to stir industry interest. Among these are packaging considerations and manufacturing. Gigabit Logic (Newbury Park, Calif) describes two types of chip carriers that are suitable for ultrahigh speed GaAs ICs. They are designed to reduce delay, transmission line loading, cross talk, and power supply noise pulses. Tektronix has designed a sophisticated 48-pin chip carrier for its Quick Chip. The carrier incorporates coplaner 50-Ω signal lines from the die to the I/O pads. Berylia substrate is used for thermal performance, and integral bypass switching capacitors minimize digital switching noise.

Still, numerous manufacturing problems are holding back the commercialization of GaAs. A Defense Advanced Research Projects Agency study described by Steven A. Rooslid of DARPA states that the manufacturing difficulties of GaAs relate to the present state of the art in material and process control. A major problem is the lack of reproducibility in the characteristics of material delivered by commercial crystal growers. Today's substrates are barely adequate for production.

—John Bond, Senior Editor

SYSTEM TECHNOLOGY

(continued on page 81)

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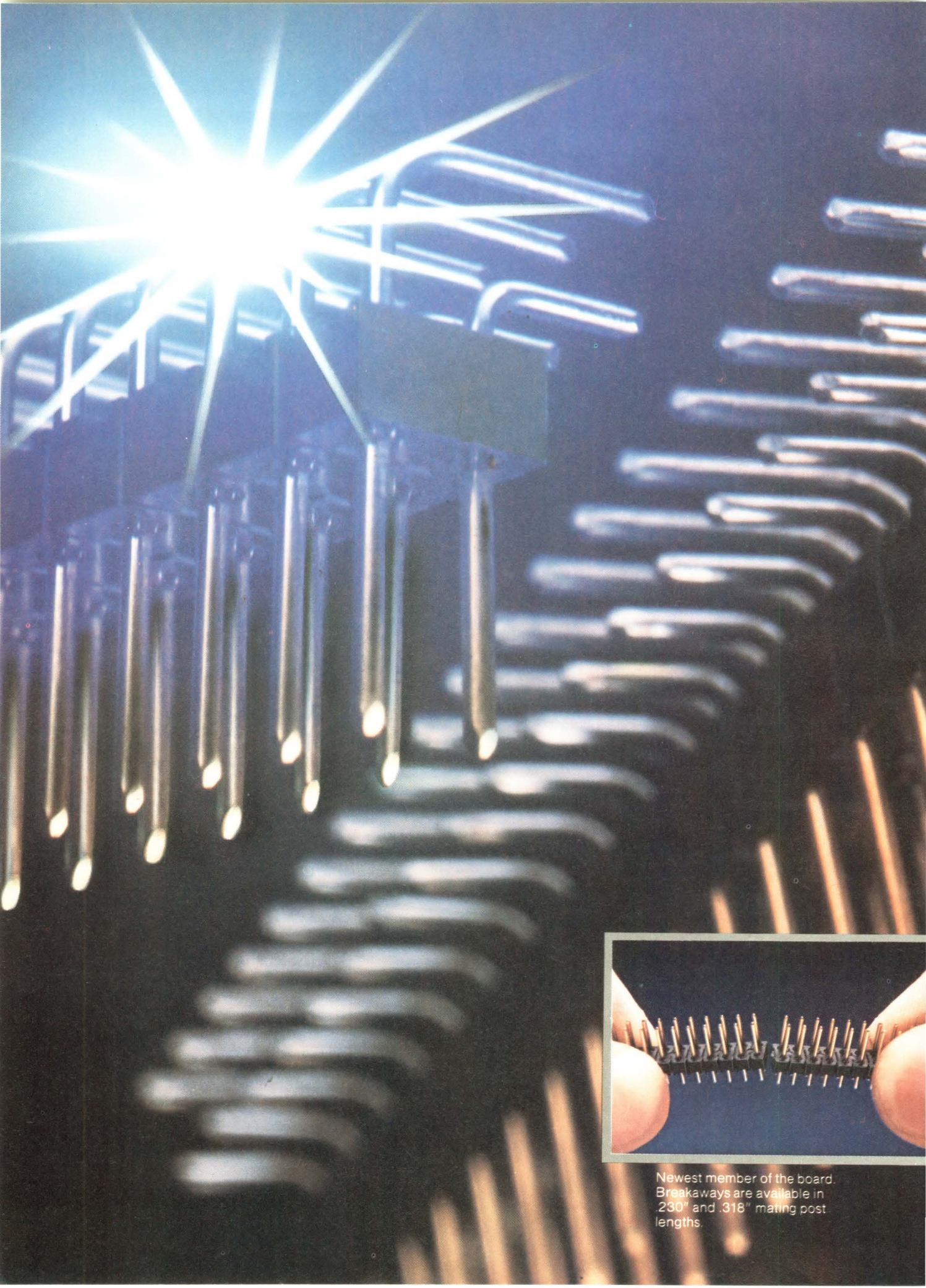
CIRCLE 36



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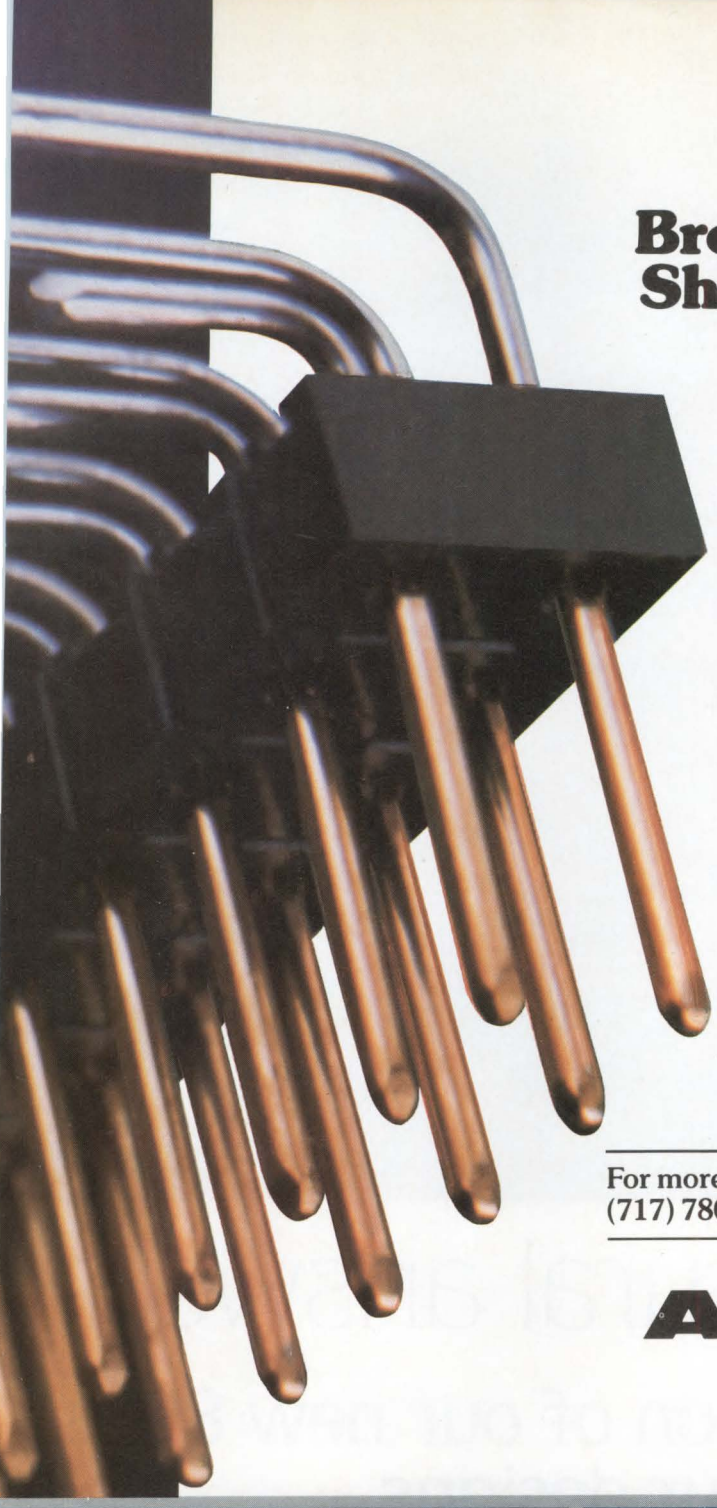

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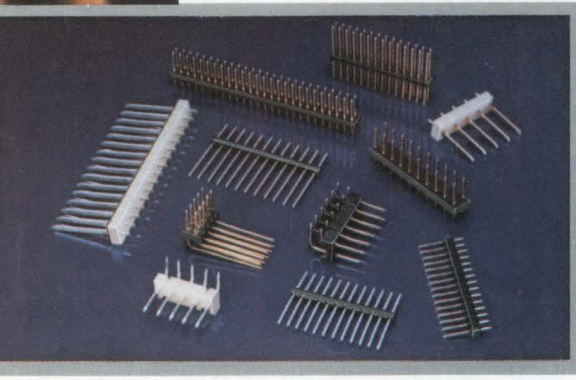
CIRCLE NUMBER 10

AMP Interconnecting ideas



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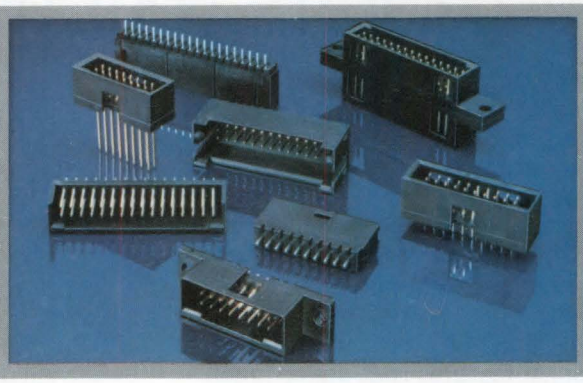

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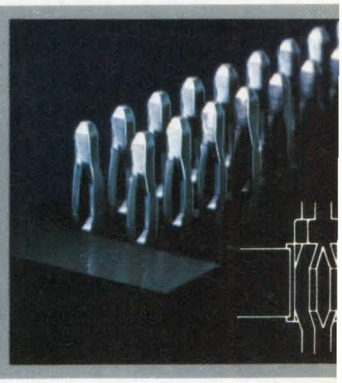

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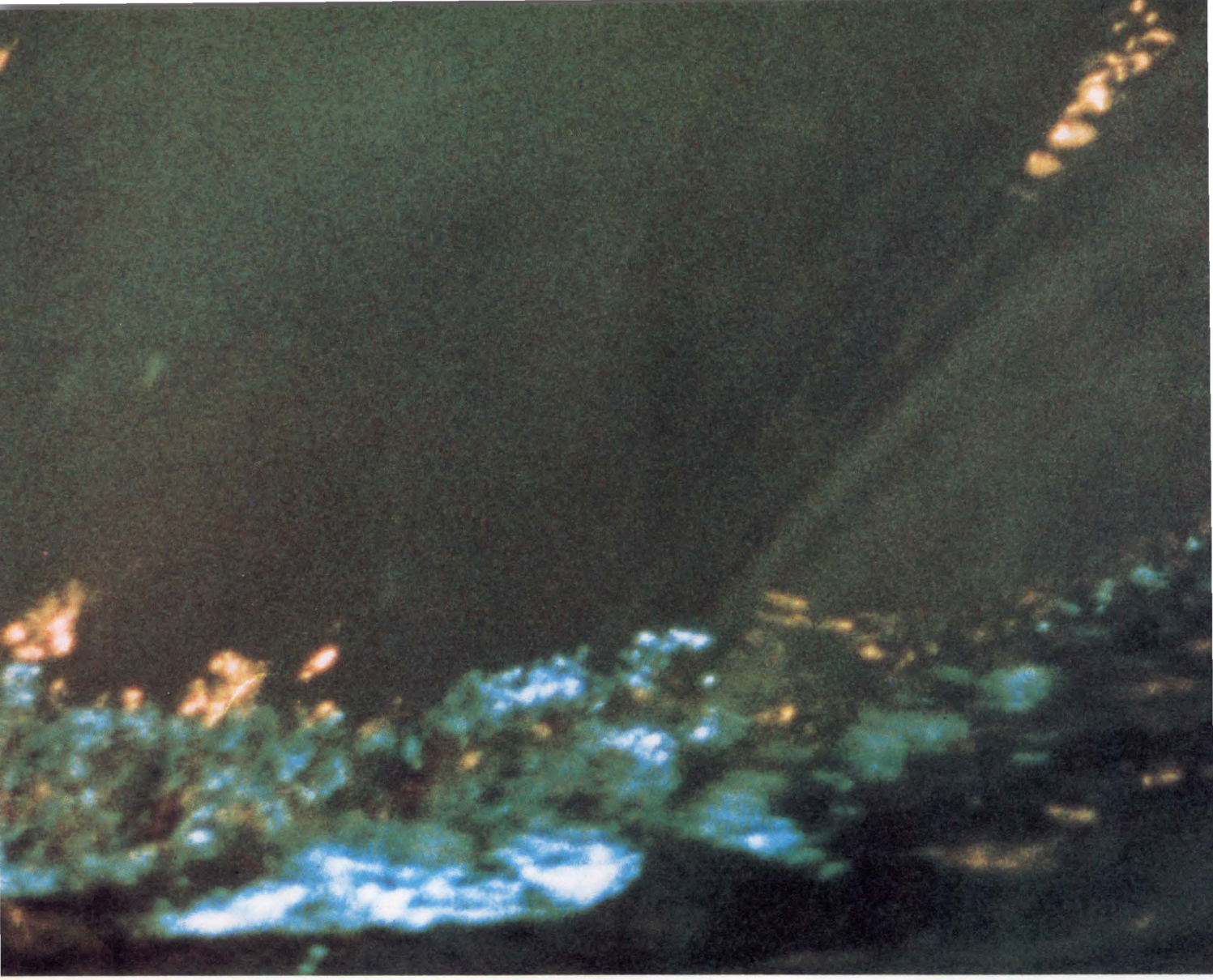

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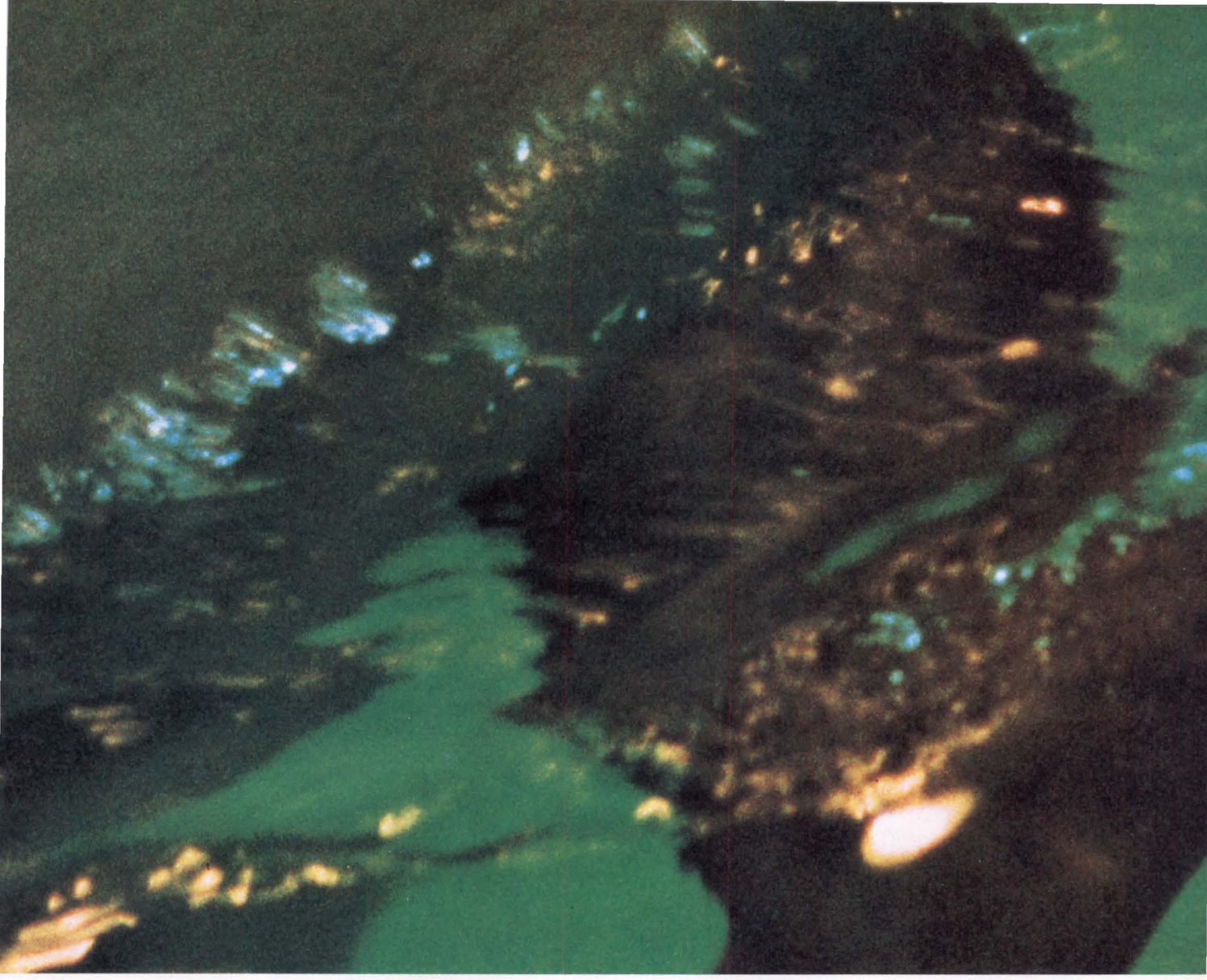

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CIRCLE 39

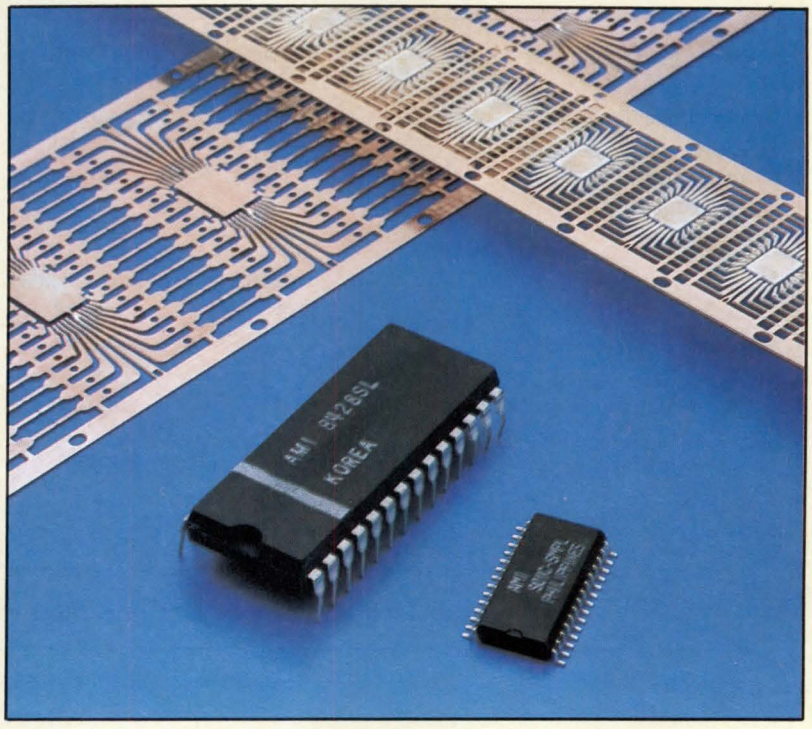
Surface-mount technology paves the way for smaller boards

Surface-mount technology, introduced in the 1960s and now enjoying widespread use in consumer products (especially watches and calculators), offers advantages that make it the packaging choice for new board designs. As space becomes a premium in products outside the consumer area, the industrial market will take a closer look at SMT.

The most obvious advantage to using SMT is that board size can be decreased. Surface-mount devices are considerably smaller than conventional parts so they can be more densely packed. This reduces board area by up to 50 percent, resulting in material cost savings and weight reduction. There is also space savings in the third dimension because boards are not as high. This two-way reduction proves beneficial to the manufacturer who wants smaller systems (ie, portable computers) and also to the manufacturer who wants to offer more capability in the same footprint.

Surface-mount devices need no through holes in the PC board. With no contact through the board, both leaded and surface-mount devices can be soldered on the same board. Although eliminating some SMT advantages, this process can be useful when components have no surface-mount device counterparts. And, in contrast to traditional boards, signal lines can be shortened. This, in turn, reduces inductive noise spikes, switching speed delays, and electromagnetic interference. Yet another benefit of SMT is that board manufacturing lends itself to automation. For some companies, the entire manufacturing process is integrated including designing with computer aided engineering/computer aided design systems, software controlled manufacturing, and testing.

Despite its advantages, SMT's biggest drawback is the initial investment in capital equipment. Nevertheless, for large companies with high volume production, the use of surface mount will become a requirement to remain competitive. Several companies, particularly those based in Europe and Japan, have a head start in manufacturing and using surface-mount components. For small or medium volume producers who need the advantages of surface mount, there are third-party manufacturers that provide this service.



One major advantage of surface-mount technology is the reduction in component size. To illustrate this space savings, compare a typical 28-pin DIP with the 28-lead small outline integrated circuit (SOIC).

An example of such a third party is Micro Industries (Westerville, Ohio). It provides engineering services as well as manufacturing services and uses an integrated process from design through board test. It starts with a CAE system that handles schematic capture and simulation. This information is passed over a local area network to a CAD system. At this point, data from the CAD system is used to lay out the board, eliminating duplication of effort by either the engineers or the CAD operators. The CAD system then turns out PC board layouts and this information is used to direct pick-and-place machines.

Micro Industries uses a vapor phase method to solder the surface-mount devices. An infrared method used prior to vapor phase was abandoned because it required rework due to shorts. In addition, hot spots appeared that would burn up components.

The controlling factor in the vapor-phase process is the speed at which the boards travel through the chamber. This speed can be adjusted so that a part stays in for a minimum amount of time. This closely controlled method offers the ability to put solder only where required.

Testing considerations

The final aspect of SMT consists of testing. Because there are no leads, or extremely short ones, testing is

(continued on page 82)

Surface-mount technology

(continued from page 81)

Cost Comparisons of Surface-Mount Technology—I

Assembly Method	Component Cost	PC Board Cost	Overheaded Labor Cost	Direct Manufacturing Cost
Manual conventional	$550	$50	$27.50	$627.50
Automatic conventional 50 percent manual	$550	$50	$19.36	$619.36
Surface-mount technology	$550	$25	$8.50 to $13	$582.50 to $588
	Capital Investment	**Annual Volume Required**	**Total Available Volume**	
Automatic insertion facility	$1 million	40,000	50,000	
Low to medium volume surface-mount device facility	$10 million	100,000	100,000	
High volume surface-mount device facility	$25 million	200,000	1 million	

Material from Micro Industries shows the cost of a typical 512-Kbyte RAM board as well as the capital expenditure justification. Dollar savings are not as dramatic when taken as a percentage of the total cost of board production.

Cost Comparisons of Surface-Mount Technology—II

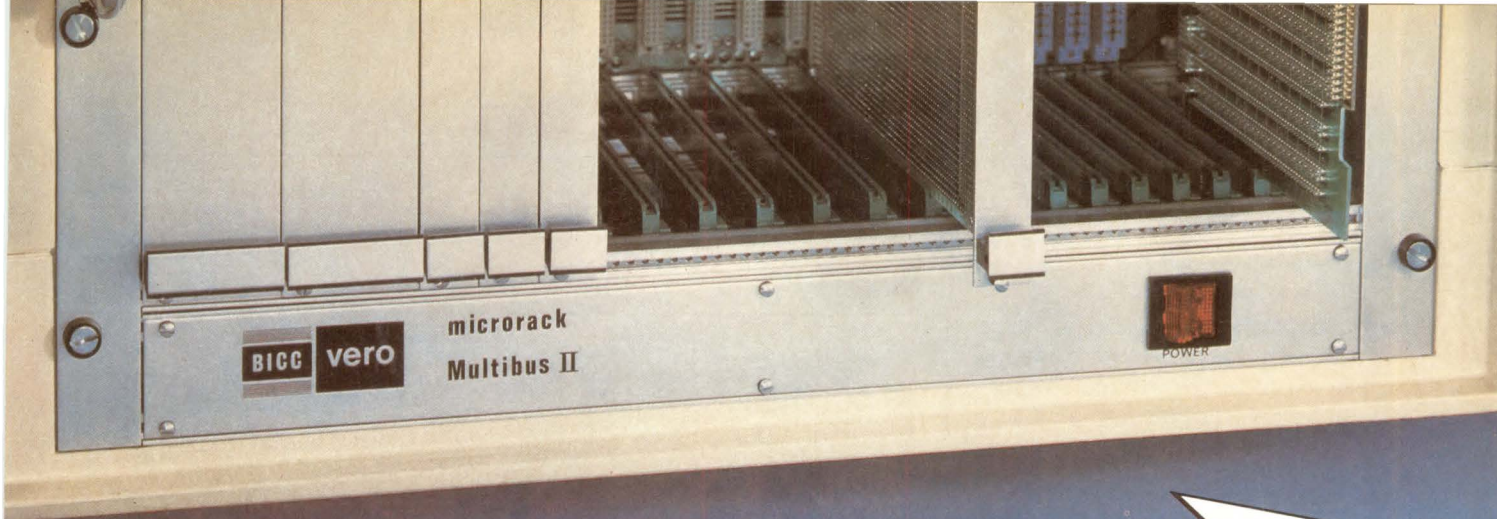
Assembly Method	Component Cost	PC Board Cost	Overheaded Labor Cost	Direct Manufacturing Cost
Manual conventional	$2200	$200	$110	$2510
Automatic conventional 50 percent manual	$2200	$200	$77	$2477
Surface-mount technology	$1673	$50	$9 to $16	$1732 to $1739
	Capital Investment	**Annual Volume Required**	**Total Available Volume**	
Automatic insertion facility	$1 million	40,000	50,000	
Low to medium volume surface-mount device facility	$10 million	5000	100,000	
High volume surface-mounted device facility	$25 million	12,000	1 million	

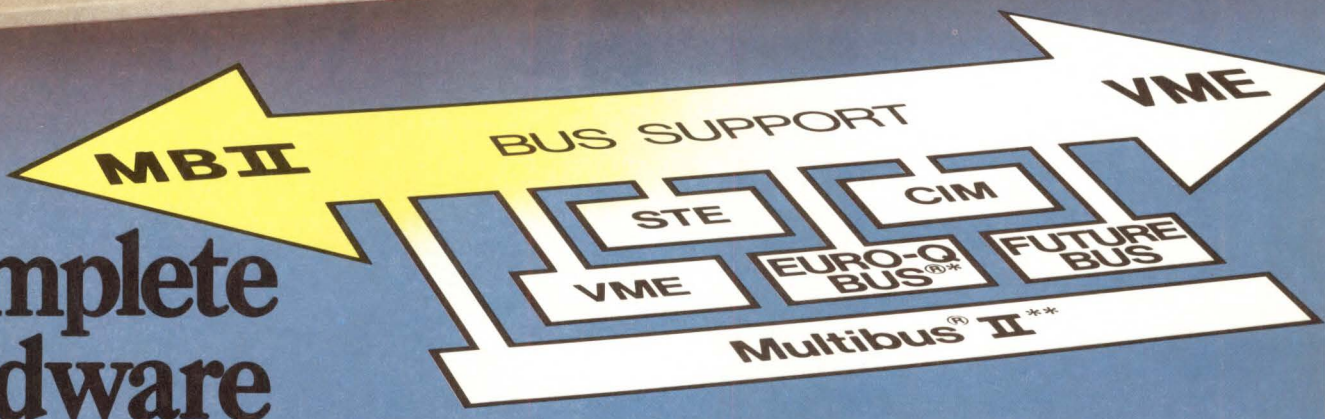
Material shows the board factor with 2 Mbytes of RAM. Clearly, cost savings increase substantially due to the elimination of duplicate hardware and volume production.

difficult. The boards must be designed to be testable so either one side or both sides will have test pads to access nodes. This can sometimes mean giving up the space advantage gained by using SMT, but the number of test pads can be limited or the board can be broken up into sections for testing purposes.

Michael Curran, chief executive officer of Micro Industries, says that in order to compete with offshore competitors, the process has to be as automated as possible. He also points out that capital expenditure savings should be considered in terms of system level savings instead of savings in component costs. Offering a similar service is Texas Instruments' Surface Mount Technology Center (Houston, Tex). At the center, users can assemble a TI-supplied demo board, or their own prototype. The lab has a pick and place robot that can handle a variety of components and is used by TI in the assembly of its SIP

(continued on page 84)





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CIRCLE 40

MULTIBUS® II SUPPORT HARDWARE

Leaders in Microprocessor Backplanes

Surface-mount technology

(continued from page 82)

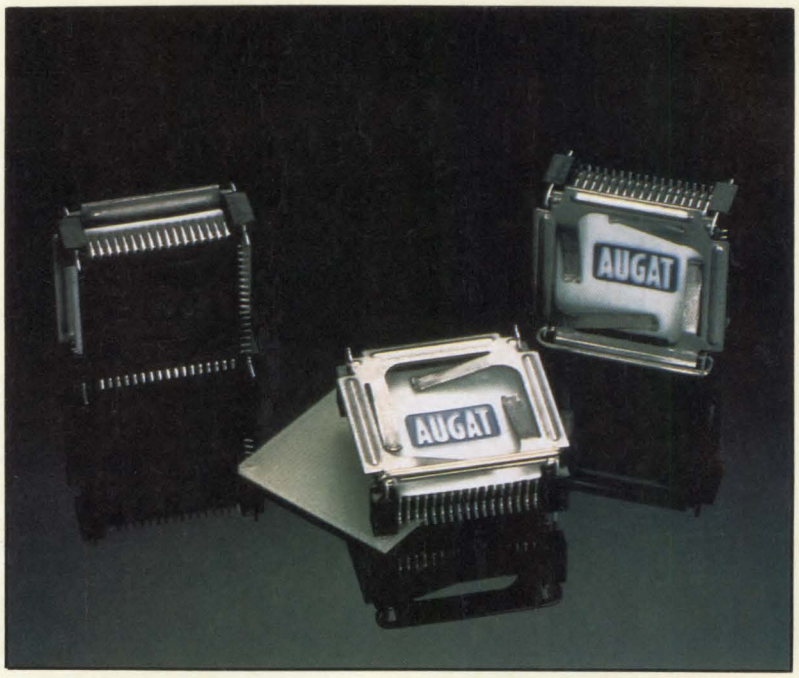
dynamic RAM modules. In addition to the robot, the workshop contains solder paste screen printers, vapor-phase reflow equipment, a defluxer, and inspection stations.

Even with the increasing number of components available from a myriad of companies combining with the advantages of surface mounting, the traditional DIP is not on the way out. Expressing the position of Motorola's MOS Integrated Circuits Group , manager of technical communications James Farrell says, "Even if surface mount becomes overwhelmingly popular in the next 5 or 10 years, there will always be a significant percentage of DIPs in use." The best place for SMT, according to Motorola, is in a new design that incorporates a large number of microprocessors or memories on a small board, coupled with a desire to keep cost low. As an example, mainframe memory boards that are big, expensive, and heavy could be replaced with surface-mount devices.

Motorola is committed to SMT and offers the full component spectrum. For instance, package planning for a 1-Mbit DRAM is separating itself into two groups. Motorola and Intel are proposing both a 300-mil wide DIP and a standard plastic leaded chip carrier to hold the rectangular memory chip. TI (and IBM) favor a 400-mil wide DIP and a "quintet" package with leads in four groups. This package is similar to a PLCC with j-type leads yet is a longer, narrower package.

The j-type is just one lead type that is used in surface-mount devices. Used primarily with PLCCs, it works best with higher pin counts. JEDEC standards do exist for both square and rectangular bodies with j-type lead spacing on 50-mil centers. Positioning and replacement is fairly easy with these lead forms. The j type leads form a package that is thicker than the small outline IC package, which could be a weakness when trying to save board space. The j type however, provides more lead strength.

For small outline IC packages, the gull wing type lead is popular. One advantage of gull wing leads is visible solder joints, an important consideration for inspection. One drawback to gull wing leads is that leads are narrow and can be damaged. In addition, high pin count packages are impractical. The gull wing lead is popular in Japan and as such offers the advantage of being a proven process.



Surface-mount devices are available in a variety of forms. This leadless chip carrier socket (or connector) acts as an interface between the chip carrier and the board.

Leadless packages, particularly ceramic chip carriers, are put on the board in a variety of ways. The package can be placed in a socket or connector, it can be directly mounted on an alumina substrate, or on a PC board that offers the same coefficient of expansion as the chip carrier.

Components are available at many levels in surface-mount packaging—from the low level sockets to memory chips and microprocessors. Augat Interconnection Components (Attleboro, Mass), for example, provides several surface-mount devices. The CCS series leadless chip carrier socket provides test point provisions and an open-sided insulator for improved heat dissipation. The series features an outboard contact for inspection of reflow solder joints, cleaning, and repair. The socket is compatible with JEDEC type A and B design on 0.050-in. centers.

Rohm Corp (Irvine, Calif) provides another example of the kinds of parts available as surface-mount devices. Although the company offers a variety of such devices, one of its latest designs is a chip resistor network. The devices are available with two, four or eight isolated resistors per package. A notched space between terminals prevents bridging of adjacent terminals during soldering operations.

An example of a typical standard semiconductor component available in a surface-mount package is the μPD4364, a low power "mixed MOS" 8-K x 8 static RAM from NEC Electronics, Inc (Mountain View, Calif). Available in a mini-flat package, the chip features low operating power and two chip-enable inputs for power down battery backup applications. A CMOS version is also available. NEC has had 2-K x 8 CMOS RAMS for several years in a mini-flat

(continued on page 86)

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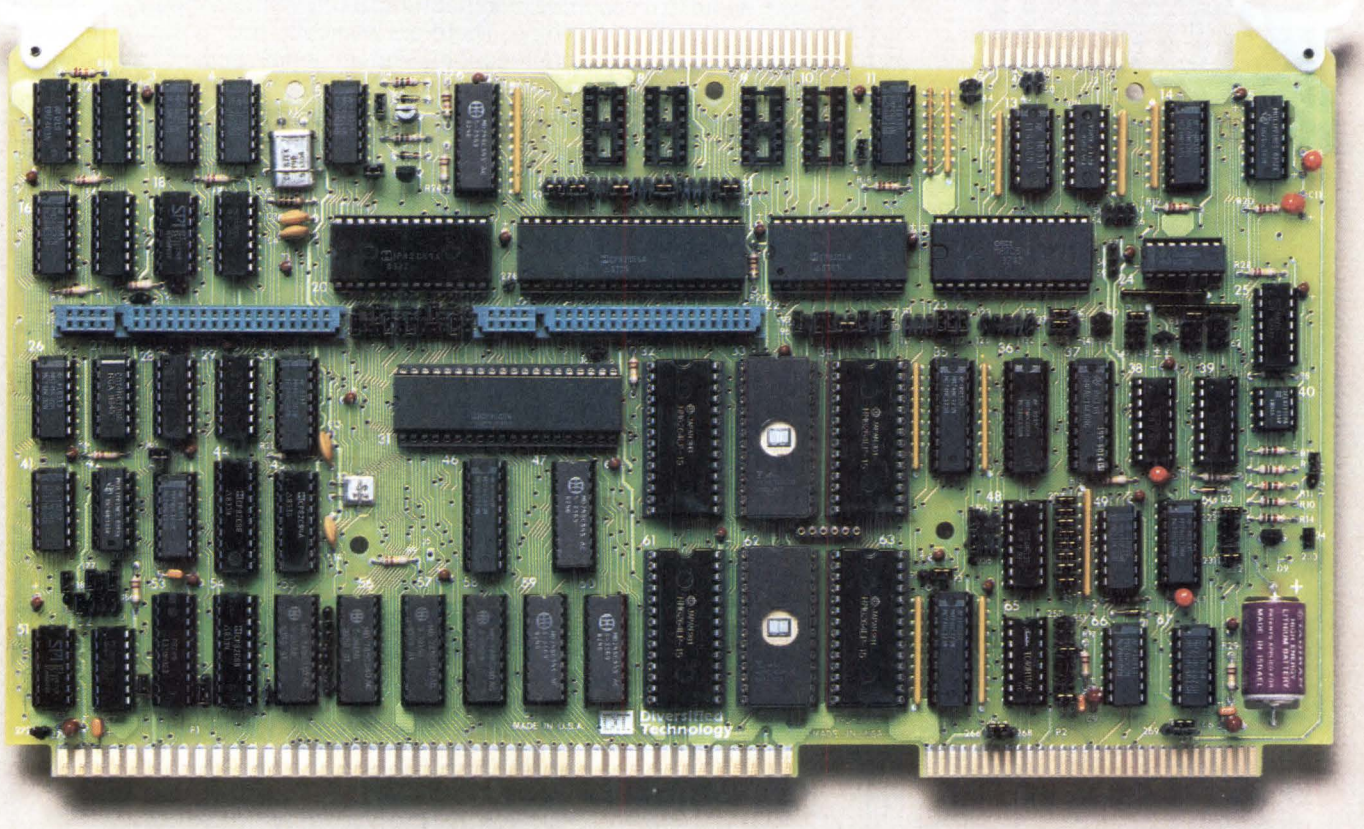

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Surface-mount technology

(continued from page 84)

The manufacturing process

Once a board is ready to be manufactured using surface-mount, it goes to a pick-and-place machine. There are basically four types of these systems that address component placement: inline, sequential, simultaneous, and simultaneous-sequential. The inline machine uses dedicated heads to place surface-mount devices in set positions as they pass. Although a simple process, resetting these machines for different boards is time consuming. And, as the number of components increases, the line can become impractical.

Sequential systems use software to control where surface-mount devices will go. Either the placement head or the circuit board determines their movement. This system offers the advantage of fast reprogramming for different boards, but because components are placed one at a time, the process is slow.

The advantage of simultaneous systems is that by placing several surface-mount devices at one time, an entire board can often be filled in one step. While this contributes to high output, the time required to reset the system is long. The simultaneous/sequential systems combine the advantages of both these systems.

As lead damage can be a problem, surface-mount device packaging is often an important part of the process. While some types of carriers require special packages, others can travel in standard tubes, flat trays, or in tape-and-reel. An automatic tape loading machine can put ICs into sealed tape. The sealed tape is opened at the time of assembly and the pick-and-place machine takes it from there.

Wave soldering and vapor phase are the two basic types of soldering used in surface-mount technology. Solder paste or glue holds the component in place. If attached by solder paste, the technique used for soldering is reflow (vapor phase); if attached by glue, they are immersion soldered (wave).

Vapor phase soldering heats substances to particular temperatures creating vapor zones. The boards are put into the vapor for a short period where soldering occurs by condensation heating of the solder paste. The boards are then cooled, dried, and removed. This technique is spared corrosive residue problems and can be fast. The vapor phase process works well with the in-line placement to form a closed system. Another advantage to this type of soldering is the controlled temperature, which ensures uniform heating of components.

package or small outline package. The primary uses have been in portable applications where space is crucial. NEC plans to support the surface-mount device market with capacitors, resistors, linears, and single-chip micros.

Representative of the surface-mount device activity in custom/semicustom ICs, Gould AMI Semiconductors (Santa Clara, Calif) feels that the right packages are extremely important. They offer a variety of lead forms and metallurgical options—all driven by the customer's particular needs. In some cases, Gould buys surface-mount packages, then assembles them by putting the die into the package and selling the assembled package to the customer. In other cases, it designs assembly equipment to do its own surface-mount package. Gould offers a small outline IC package in a 0.300-in. "wide body" package. This gull wing package can accommodate a range of die sizes and has either 16 or 28 leads.

—Malinda Banash, Senior Associate Editor

SYSTEM TECHNOLOGY

(continued on page 92)

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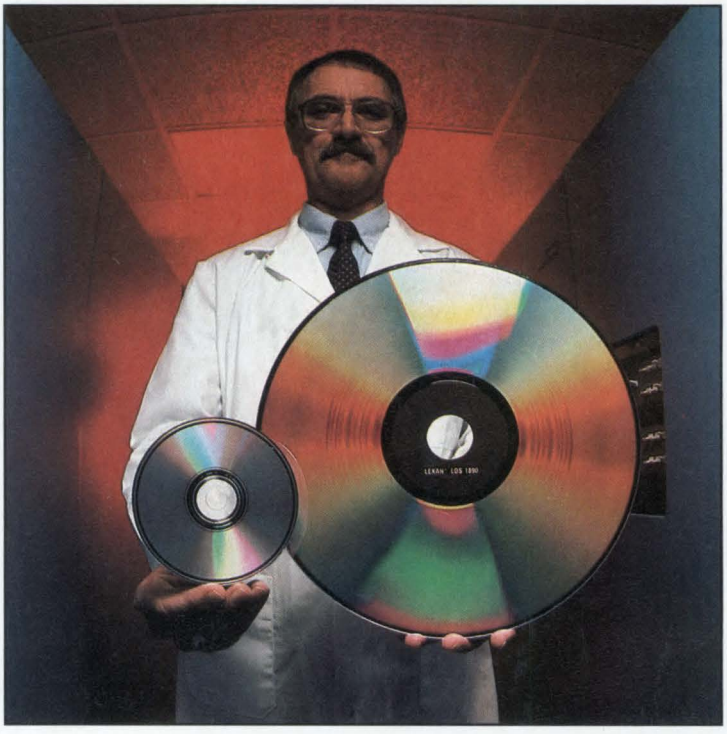

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Semiconductor advances fuel computer progress—and the IEEE-sponsored International Solid State Circuits Conference is the premier semiconductor conference. As such, the ISSCC is as important to computer system designers as it is to semiconductor designers.

As if to underscore that relationship between computers and semiconductors, Dr Raj Reddy was selected to make the keynote address. Reddy is a Professor of Computer Science, and Director of the Robotics Institute at Carnegie-Mellon University. He is also the Chief Scientist at the World Center for Computer Science and Human Resource in Paris. His research focuses on artificial intelligence, human-machine communication and signal understanding systems.

Reddy is, in short, the complete systems person. And his keynote remarks on "Super Chips and Artificial Intelligence," highlight the evolving union of system- and device-level technologies. As Reddy will note, at least one field—AI—can use all the advances of semiconductor technology. Even as the growing sophistication of computers drives semiconductors to greater and higher levels of integration and speed, VLSI will give way to ultra-LSI and will transform the design of computers.

Dynamic and dense

As usual, dynamic RAMs lead the way in density. Less expected, considering the inroads CMOS has made, is the number of 1-Mbit DRAMs still designed in NMOS. Engineers from NEC Corp (Kawasaki, Japan) for example, will describe a 1-Mbit DRAM that has an 85-ns access time. Apparently, NMOS still has room to grow before it reaches its power/density limits as evidenced by the 300-mil plastic DIP in which NEC chose to package the chip. The 43.2-mm^2 chip uses trench capacitors with an additional polycide interconnect layer. The presentation will also discuss a quasi 4-bit wide test capability.

Not to be outdone, Mitsubishi Electric Corp (Itami, Japan) has designed its 1-Mbit DRAM with multibit test mode. This feature allows testing of the 256-Kbit x 4 memory through the use of a test pin. The 1-Mbit chip's area is 65 mm^2. It uses one-half V_{CC}-biased memory cell with a reduced electric field of 2 mV/cm. The design includes shared sense amplifiers and continuous nibble mode.

Along with the movement toward more testable chips, a complementary requirement exists that large DRAMs be repairable. Although not a new technology, a 1-Mbit CMOS DRAM from Mostek (Carrollton, Tex) is the latest to rely on this method to increase yields. Over 80 percent of the die area is repairable using laser programmed redundant rows and columns. The use of a divided bit-line matrix architecture and a 1.2-micron double metal CMOS process permits an array area-to-die ratio of 56.6 percent.

Another NMOS 1-Mbit DRAM from Toshiba (Kawasaki, Japan) has a typical column address strobe access time of 30 ns. This is achieved with a folded capacitor cell structure. The chip is fabricated using buried oxide isolation and two-level metallization.

As the 1-Mbit DRAMs come out of the lab, attention must eventually turn to that inevitable next step, the 4-Mbit DRAM. No presentations on the 4-Mbit DRAM are scheduled, but if past conferences are any indication, there could be late additions to the itinerary in order to cover progress in this technology. Although no one has yet built a 4-Mbit DRAM (or at least no one is ready to talk about it), Hitachi, Ltd's (Tokyo, Japan) presentation may offer a peek into the future. Hitachi will describe a single transistor dynamic memory circuit that has a four-fold density storage advantage over conventional DRAMs. The 16-level, 4-bit/cell device offers a read/write operation with a storage level of 80 to 100 mv.

CMOS and 256 Kbits appear to be the state of the art in static RAMs, although numerous approaches to this technology exist. Nonetheless, activity continues in smaller SRAMs where

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ISSCC Conference Sessions

Wed, Feb 13	Thurs, Feb 14	Fri, Feb 15
9-11:45	9-12:15	9-12:15
Microprocessors and floating point processors	Flexible digital arrays	Megabit DRAMs
Consumer ICs	Analog techniques	Modeling and technology
Memories for special applications	Communication links	Monolithic filters
1:30-2:10	1:30-5:00	
Conference opening	Nonvolatile memories	
2:10-2:50	Processors for specific applications	
Keynote address	High speed arrays	
3:20-6	High speed technology and design	
High density SRAMs		
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Signal processing		
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NEC Electronics Inc.

CIRCLE 45

ISSCC chip designs

(continued from page 92)

density is often traded off for speed or other features. Fastest of all is the only non-CMOS SRAM reported—a CML gallium arsenide 4-Kbit (1-K x 4-bits) from NEC Corp. It has a 2.4-ns address access time with a 1.1-W power dissipation.

A 64-Kbit CMOS SRAM designed by Toshiba offers a blistering 17-ns access time. It employs Schmitt trigger sense amplifiers. Eschewing the more common 6-transistor depletion load memory cell, this device uses a 4-transistor cross-coupled flipflop memory cell with a high resistivity double polysilicon load cell.

Varied designs mark the 256-Kbit CMOS SRAMs. For example, a 45-ns Hitachi chip with 200-mW active power dissipation at 10 MHz utilizes variable impedance dataline loads, pulsed word lines and latched output buffers. A 55-ns NEC SRAM uses optimized polysilicon load resistors, buried isolation, and Titanium-polycide to achieve 10-μW standby power. Mitsubishi's 45-ns device obtains a peak current of 45 mA by using an address transition activated circuit combined with a tri-level word line circuit.

The only American company reporting on SRAM technology will be Motorola (Austin, Tex). The company's 8-K x 8-bit, 34-ns SRAM dissipates only 55 mA by the use of an internal power down feature. Internal

(continued on page 97)

Informal Discussion Sessions

Wed, Feb 13 (8 pm)

- Computing for artificial intelligence
- Video signal processing
- The effects of scaling on future analog/digital systems
- System applications and limitations of submicron MOS
- Nonvolatile circuits as building blocks
- CAE workstations

Thurs, Feb 14 (8 pm)

- Custom and semicustom design approaches for the future
- A-D architecture of the future
- Fault-tolerant techniques for memory components
- Using optical links to interconnect digital equipment
- High speed LSI technologies challenging the CMOS VLSI era

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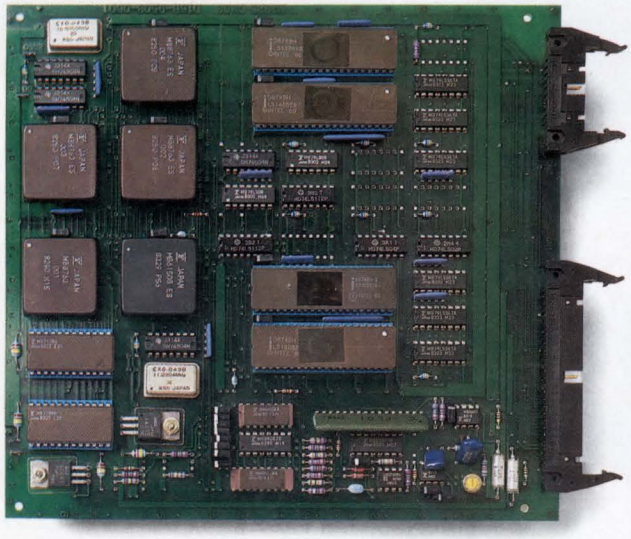

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CIRCLE 46

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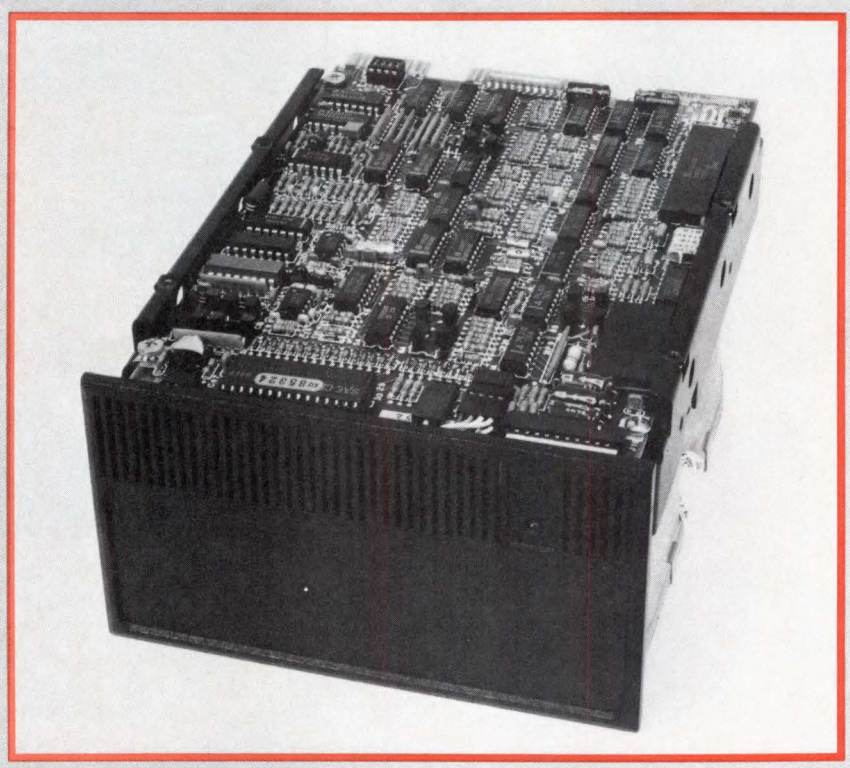

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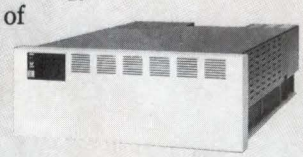

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CIRCLE 47

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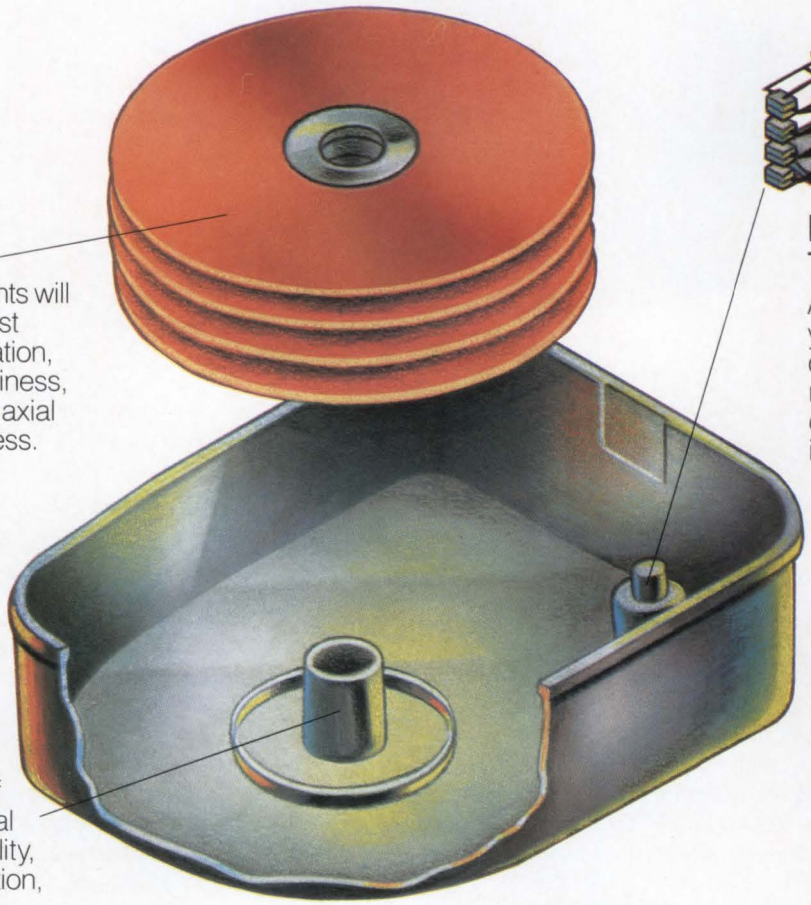

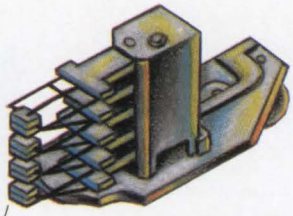

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CIRCLE 48

ISSCC chip designs

(continued from page 94)

chip selection is broken down in several blocks to reduce power surges.

Microprocessors first up

The first session at ISSCC covers microprocessors and floating point processors. Hitachi will discuss an 8-bit CMOS microcomputer implemented in 2-micron rules. A reconfigurable RAM register file and direct instruction control of a ROM-based microprogram allow instruction set redefinition.

Single-chip floating point processors come into their own with new designs from NTT (Kanagawa, Japan) and AT&T (Holmdel, NJ). The NTT FPP uses a 1.2 micron n-well CMOS technology to build a 5.6-million floating point operation, 80-bit chip that contains 50,000 gates and 15 Kbits of memory. The AT&T FPP implements the IEEE floating point standard. The 14-MHz chip was designed in 1.75-micron twin tub CMOS as a coprocessor to AT&T's own 32-bit microprocessor. The chip performs single, double, and extended double precision floating point along with 32-bit integer and 18-digit BCD operations.

NMOS still holds sway over digital signal processors as they stand poised to leap into the next generation. AT&T's programmable 32-bit DSP chip implemented in 1.5-micron NMOS, contains 155,000 transistors and operates at 16 MHz. It is a full 32-bit chip with 32-bit data path, instruction set, and floating point arithmetic.

A DSP chip with multiprocessing capability will be described by Texas Instruments (Houston, Tex). The multitasking chip is implemented in 2.4-micron NMOS and can do 8 to 13 million instructions per second. It includes a 544- x 16-bit RAM and single cycle multiply/accumulation instructions.

An NMOS pipelined image processor designed at Tohoku University (Sendai, Japan) is noteworthy not for process technology (5 μm) or speed (2 MHz), but for the unique use of quatenary logic. Multiple ion implant quatenary logic results in a four-fold reduction in complexity compared to conventional binary logic.

A presentation by Hughes Research Labs (Malibu, Calif) will detail an 8- x 8-bit parallel multiplier in submicron NMOS technology. The 16-ns 8- x 8-bit amplifier is fabricated with .85 micron gate lengths. The 1427-transistor chip dissipates 600 mW and has a 420-ps average gate delay.

Researchers from Catholic University (Louvain La Neuve, Belgium) will report on a 2-MHz optical character

(continued on page 98)

Featuring the 12.5MHz 68000 with four multi-protocol serial ports.

This is a powerful single board computer designed for your high performance applications like engineering work stations and real time process control. Look at these features:

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- (4) multiprotocol Asynchronous/ Synchronous RS232C ports with baud rates up to 1000K baud.
- Optional memory management.
- One iSBX* connector—and more!

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ISSCC chip designs

(continued from page 97)

recognition chip. The chip can support preprocessing, binary, and feature extraction types of algorithms.

Two ways to go with array logic

Sparked by the explosive growth in semicustom logic, this year's conference will have two digital array sessions. One session concentrates on flexible arrays and the other details the latest in high speed arrays.

Toshiba reports a triple-level wired 24,000-gate CMOS array. Implementation of a digital signal processor on the chip is compared to a full custom design. A 240,000-transistor CMOS array from Fujitsu permits flexible allocation of logic, memory, and wiring channels. An 8000-gate array—capable of integrating RAM, ROM and microprocessors, along with the usual logic—has been developed by Mitsubishi. It is implemented in 1.5-micron CMOS technology.

The growing need to test arrays forced Hitachi to design a 4000-gate CMOS array with automatically generated test circuits. Cell structure and D-A system supports 98 to 100 percent dc fault testing. Test circuits use only about 5 percent of the chip area.

Signetics Corp (Sunnyvale, Calif) has combined technologies to build a 50-ns, 48-term, CMOS erasable, programmable logic array. The 48 P-term AND-OR array with 16 inputs and 8 outputs can be programmed with a 21-V EPROM programmer.

Among high speed arrays, bipolar and GaAs technologies are clearly in front—with the exception of one CMOS 20,000-gate array from Fujitsu, Ltd that has typical gate delays of 1 ns and memory access times of 15 ns. More common high speed bipolar arrays are NTT's 80-ps, 2500-gate device, Siemen's 100-ps, 9000-gate ECL masterslice, and National Semiconductor's ECL field programmable logic array with a 3.6-ns delay.

CMOS makes more inroads as PROMs and EPROMs rely on that technology. Cypress Semiconductor Corp (San Jose, Calif) for example, has built a 25-ns 250-mW, 16-Kbit (2-K x 8-bit) CMOS PROM that uses a 4-transistor differential cell; Intel (Santa Clara, Calif) and Hitachi have both concentrated on 256-Kbit CMOS EPROMS.

Toshiba reports that a 256-Kbit flash EEPROM with single transistor cells has been achieved with 2-micron design rules and polysilicon technology. Advanced Micro Devices, Inc (Sunnyvale, Calif) remains at the 64-Kbit level with its EEPROM, choosing to build in such advanced features as a page mode operation that allows 32 bytes to be written in 10 μs. The 1.8-micron n-channel EEPROM operates over an extended temperature range from −50 to 125 °C.

—John Bond, Senior Editor

SYSTEM TECHNOLOGY

(continued on page 100)

REYE SYNDROME

Reye syndrome is a ***rare but dangerous*** condition that can develop from ***flu or chicken pox.*** It occurs mainly in ***children under 16,*** usually when they ***appear to be recovering.*** Watch for these signs:

- ***Persistent vomiting***
- ***Fatigue***
- ***Confusion and belligerence.***

If your child displays any of these symptoms, ***consult a doctor immediately.***

Some studies indicate that there may be an association between the use of ***aspirin*** for flu and chicken pox and the development of Reye syndrome. Further studies are being conducted on this possibility. In the meantime, the ***U.S. Surgeon General*** suggests that you check with your doctor before using aspirin or any medication when your child has flu or chicken pox.

—A message from the Food and Drug Administration.

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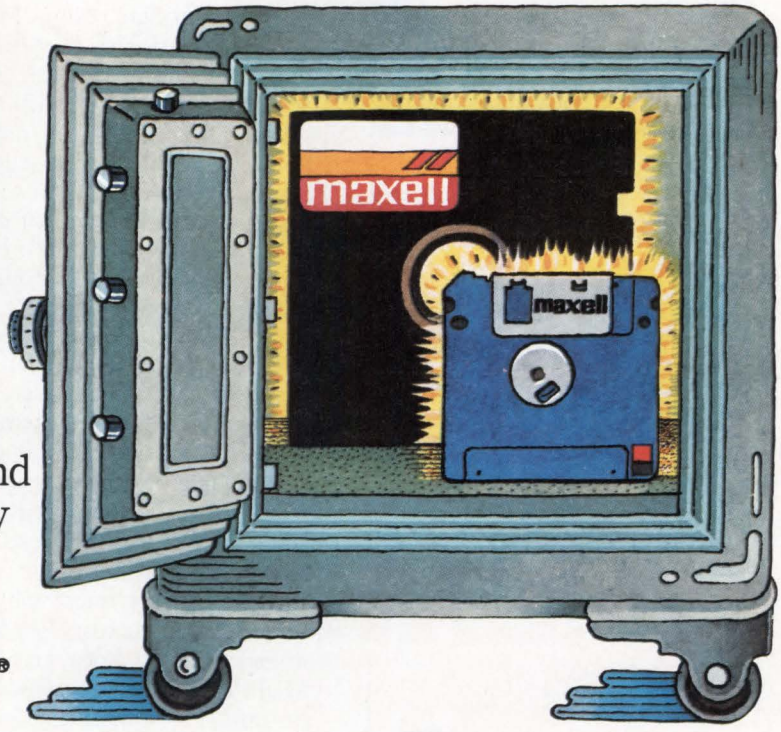

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CIRCLE 50

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Mini/Micro West stands alone

This year, Mini/Micro West will stand on its own for the first time. In the past, its meetings were tied to other regional trade events, such as Wescon, that are organized by Electronic Conventions, Inc. From Feb 5 to 7 at the Anaheim, Calif Hilton & Towers, Mini/Micro will feature a broad professional program, including three tutorial sessions.

The expanded professional program consists of parallel morning and afternoon sessions. A total of 11 sessions covers hardware and software.

On Tuesday, two sessions will deal with advances in computer architecture. The morning focuses on multiprocessor architectures, emphasizing data-flow and fault-tolerant multiprocessor systems, modular architectures for remote terminal systems, and response in microcomputer ring networks. The afternoon concentrates on vertical migration architectures, 32-bit micros and bit-slice devices.

Another Tuesday morning session covers the design of local area network controllers using MOS and bipolar techologies. A session later that afternoon entitled "Network Software in the 80s" will focus on subjects in the LAN/networking field. It will include discussions of emerging network software standards, interconnection of dissimilar systems on the same network, and the impact of the personal computer on network technologies.

On Wednesday, a morning session covers high performance, semicustom devices. Devices covered include programmable logic arrays, gate arrays, and other bipolar programmable logic devices that threaten to replace conventional SSI and MSI chips. The other Wednesday morning session will center on mass storage systems interfacing. Representatives of Maxtor, Seagate Technology, Shugart Corp, and Advanced Micro Devices will present their views on interface standardization.

Wednesday afternoon will treat attendees to a session on the design and application of realtime multiple processor systems. Such systems appear to be the answer to problems in signal processing and other applications where high throughput is required for complex operations. This session will be useful to designers interested in the state of the art for relatively low cost multiple processor systems.

The second Wednesday afternoon session deals with "Advanced System Software in Higher Level Languages." These discussions will cover realtime operating systems that support popular high level languages.

Thursday's program includes two morning sessions and one afternoon meeting. One of the morning sessions, "The Big Picture in Computer Graphics," explores advances in VLSI graphic display controllers and their architectures. It also deals with the various concepts designers need to understand to design systems that use today's advanced bit-map graphics. The second morning session covers the architecture of desktop 68000-based systems. Speakers here will discuss why they chose to build their systems around single boards or buses, and why they chose networked, standalone, single-, or multiuser systems.

Thursday's final session discusses Modula-2 as a language system and a development environment. Implementations for CP/M-80, the Macintosh, the IBM PC, and other systems that will be discussed by their respective vendors.

Mini/Micro also offers three paid tutorial sessions, one each Wednesday morning and afternoon, and another Thursday morning. These will cover "Optimizing the Design for a Network of Microcomputer Workstations," "Forth Language Software for Microcomputer Application," and "Mini/Micro Database Management," respectively.

—Jim Hughes,
Special Features Editor

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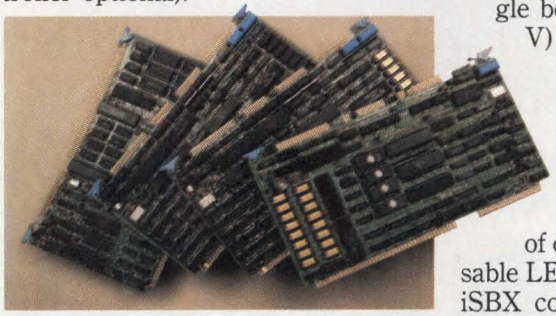

MLZ-91A single board CP/M™ system with on-card floppy disk drive controller, winchester interface, optional AM9511, streamer tape interface, two serial ports, one parallel port, 64K or 128K bytes RAM with parity, two EPROM sockets, and GPIB CONTROLLER.

MLZ-92A single board CP/M™ system with four serial ports on-card, floppy disk drive controller, winchester interface, optional AM9511, Centronics printer interface, 64K or 128K bytes of RAM with parity, and two EPROM sockets.

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HK68™ powerful and versatile single board UNIX™ (System III or V) or CP/M68K™ system with 68000/68010 CPU (8Mhz or 10Mhz), MMU, quad channel DMA, four serial ports, 128K, 256K, 512K or 1M bytes of on-board RAM with parity, up to 32K bytes of on-board EPROM, user accessable LEDs and dip switches, and two iSBX connectors for I/O expansion. Heurikon can also supply a full line of iSBX I/O expansion modules including quad channel serial port module, floppy disk controller, A/D converter, bubble memory and many more.

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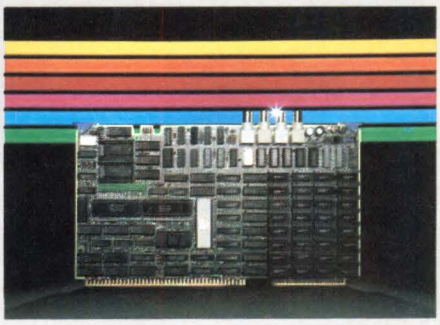

MLZ-VDC intelligent 640 x 480 x 4 color graphics controller based on the NEC 7220 controller chip with on-board Z-80 CPU, DMA controller, and user definable FIFO interface to Multibus™. Users may display up to 16 colors from a 4K palette. Up to 1024 x 1024 x 3 interlaced also available.

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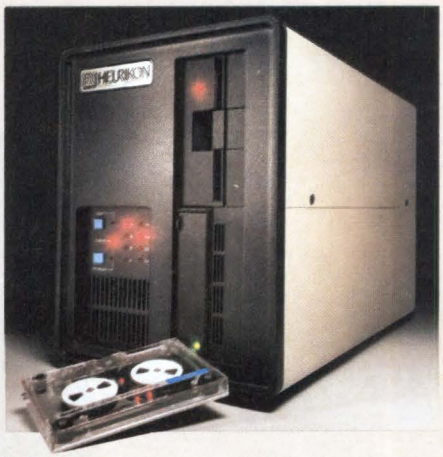

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CIRCLE 51

I/OPE

NERS

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Mostek also offers an 8-bit version of the 68000, the MK68008, which provides software portability from 8 to 16 to 32 bits. Our proprietary 68200 family of high-performance 16-bit, single-chip microcomputers is ideal for I/O intensive applications like robotics.

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The HD68450

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This highly "intelligent" device can meet different data transfer requirements for your newest product design. For more information about the new Hitachi HD68450 DMA Controller, call your local Hitachi Representative or Distributor Sales Office.

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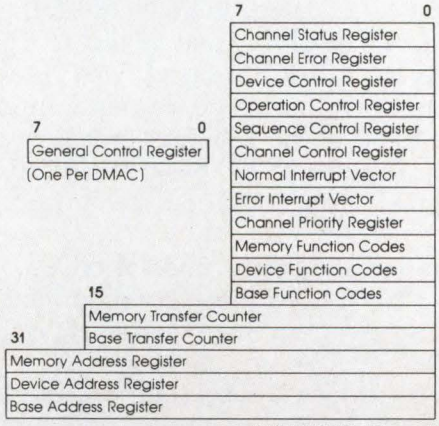

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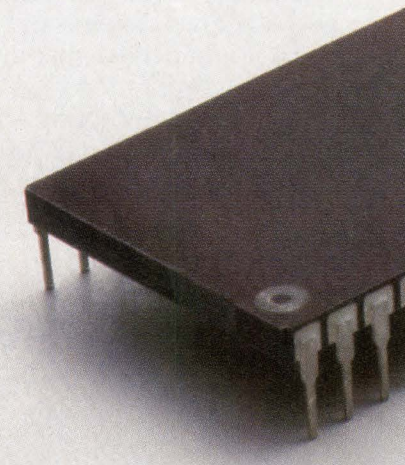

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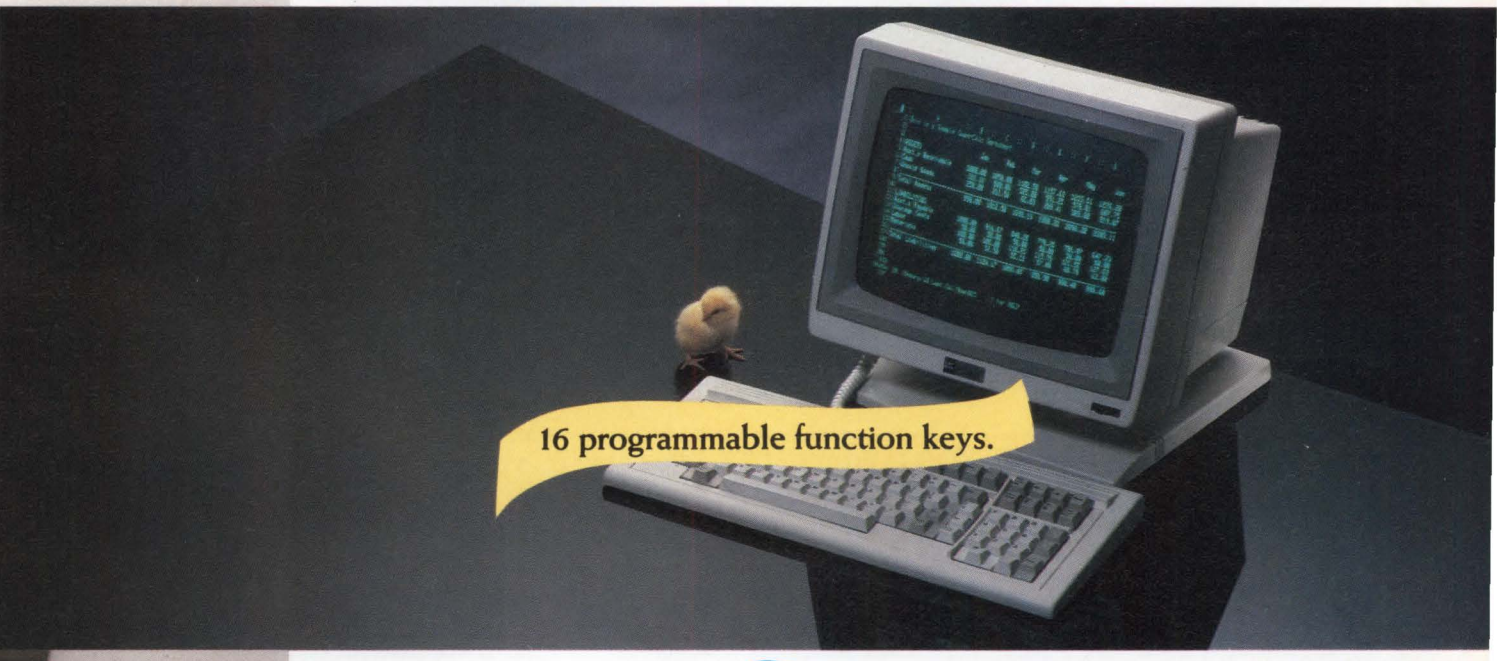

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PEACE OF MIND TECHNOLOGY

CIRCLE 55

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Genicom 3000 printer reliability can keep a customer happy for years.

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CIRCLE 56

SPECIAL REPORT ON

TECHNOLOGY FOR ADVANCED WORKSTATIONS

Workstations for computer aided design, computer aided manufacturing, computer aided engineering, and software development are ever-present at firms concerned with computer hardware and software. Most models of these machines use the latest hardware and software technology, but remain basically conventional in design. Number-crunching based classical software and von Neumann architectures are typical. Advances are confined to offering 32-bit instead of 16-bit systems, more software development tools and applications, better graphics, and other nonradical, evolutionary changes as the market demands more cost-effective machines. With all the new workstation vendors using hardware and software that is available to all comers at ever lower prices, product differentiation is difficult.

The conventional workstation market is fast becoming a "me-too" set of offerings that will soon see a shakeout, leaving but a few survivors to serve the market. But, there is a new workstation market developing that offers different technology. Proprietary, multichip, bit-slice processors replace conventional single-chip, general-purpose microprocessors. Symbolic processing, using languages such as Lisp and Prolog, takes the place of number crunching. And, data flow architectures supplement traditional architectures. Also provided are microcode compilers, tagged data structures, and more.

With a few exceptions (Tektronix, Texas Instruments, Xerox), the firms supplying these new technology based workstations are young and relatively small. Most of the workstations come from firms that, until now, have been active in the rather small artificial intelligence community (LISP Machines, Inc, Symbolics, Xerox). Yet, all the players now realize that the software development environments that their workstations provide are ideal for software development in non-AI domains. Still other firms like Daisy have not concentrated on symbolic processing, but have adopted new technologies like data flow architectures to enhance their workstation operation.

The section starts with an overview of the hardware and software in the new technology based workstations and their relationships. Subsequent articles explain how a data flow architecture speeds the hardware accelerator in one workstation, and how a symbolic processing based workstation can perform a chip design. Another article explores the development of an office based, symbolic processing workstation. Read it all to find out what is offered in the latest efforts in order to get your workstation dollar.

Harvey J. Hindin

Harvey J. Hindin
Special Features Editor

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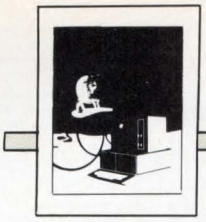
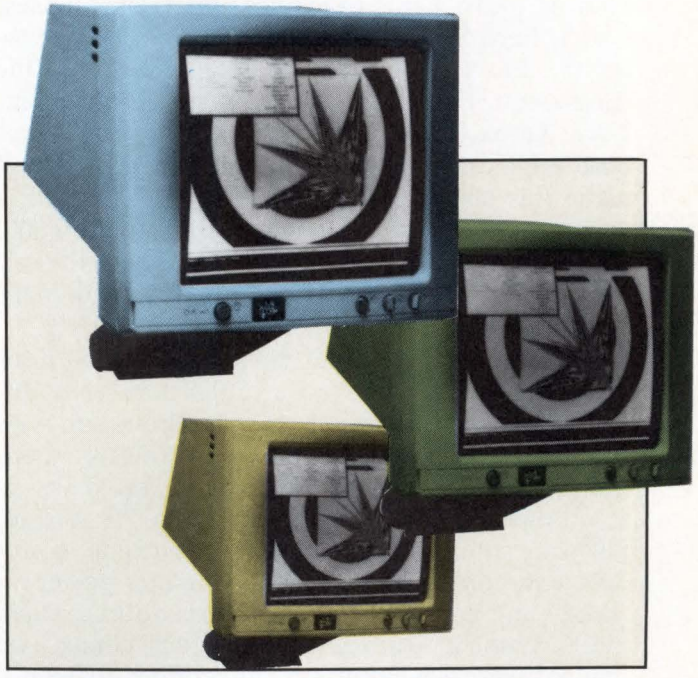


REVOLUTION BREWING IN WORKSTATION TECHNOLOGY

New machines sport symbolic processing environments to speed the design process and accommodate the realities of design work.



by Harvey J. Hindin,
Special Features Editor

Whether working at the chip, board, subsystem, or system level, engineers have barely assimilated workstations based on conventional computer architectures and software into their daily chores. Now a new breed of workstations offered by some half dozen firms are giving them more to digest. These new machines perform symbolic processing, not the number-crunching of conventional machines. They use symbolic processing languages—formerly used by artificial intelligence aficionados. Moreover, some of them forgo the classic von Neumann architecture for the data flow paradigm, or some degree of parallel processing.

The new workstations promise to make designers' jobs easier. In fact, symbolic processing languages create an ideal environment for software development and hardware design. In the real design world, designers spend most of their time experimenting. They often do not know in advance just what will happen during a design or what software or computing resources will be necessary. Therefore, they need to revise their designs many times as the total picture becomes clear.

Every designer knows these claims are true. No one ever writes a complex software program correctly on the first try. The neat flow charts that the textbooks show for software design and the smooth techniques for implementing them are pure fiction. The actual process is a study in organized chaos. Similarly, designers know that hardware design, such as chip design or printed circuit board layout, is done over and over again until it is right. Worse, much of what is done is lost to the next design, even if it is similar, because of the kind of software development that must be done.

What designers do not know is if, or how, the new machines can help them. They have heard many claims over the last two years about conventional workstations and are skeptical of these proffered

panaceas. Further complicating the task of choosing the best system for each need, the overcrowded conventional workstation vendor market has some 30 suppliers (soon to shake out, say industry observers, and the big names are not yet even in the field), offering a host of "me-too" products. In contrast, the symbolic processing based workstation arena has but six dedicated vendors (with several on the way). However, a host of firms are offering symbolic processing add-ons to their conventional machines, hoping to tap a market that promises both rapid growth and future shakeouts.

Process that symbol

The claim of manufacturers of symbolic processing based workstations is simple. They will provide a software development environment—the hardware, such as disks, networks, mice, keyboards, and graphics; and the software, such as symbolic processing languages and development tools—to allow software and hardware designers to design more easily than ever before. Regardless of their machine's hardware variations, symbolic processing language, or kind of tools, LISP Machines, Inc (Los Angeles, Calif), Perq Systems Corp (Pittsburgh, Pa), Symbolics, Inc (Cambridge, Mass), Tektronix, Inc (Beaverton, Ore), Texas Instruments, Inc (Austin, Tex), Xerox Corp (El Segundo, Calif), and others both large and small, established and start-up, all make this claim. The products of these firms are different and prices range from $15,000 to $150,000. But, there are great similarities too, owing to their common origins and their use of the Lisp language and its add-ons.

While the new machines can be used very well for hardware development [eg, a 15,000 device chip for an optical mouse (see "Symbolic Processor Aids Design of Complex Chips," on p 147 of this issue)], they are mostly being touted for software development, especially outside their traditional AI domain. Software continues to become more difficult to produce and more costly, even as computer power increases and hardware costs decrease. Sources claim that the same hardware is available to all comers and that software is what makes for product differentiation. So, any workstation manufacturer offering a more cost-effective way to produce software is sure to have an eager design audience.

Most workstations run the Lisp language—today the latest thing. Lisp was actually developed in the 1950s by John McCarthy, the inventor of number-crunching Fortran, which also made its appearance at that time. More or less ignored except by the AI community, since the notable failure of AI to produce much of value in the 1950s, Lisp is today in competition with Prolog as the choice AI language (see *Computer Design*, Sept 1984, p 150). Although preferences may change, the AI part of the Japanese Fifth-Generation Computer Project favors Prolog; U.S. researchers favor Lisp, although they are also looking at Prolog.

Key words in symbolic processing

cdr-coding: Contents of decrement registers (cdr) coding is a technique for compact list storage. In every memory word, 2 bits indicate whether the word following a preceding word is the contents of the next word in a list (cdr-next), the address of the next word in a list (cdr-normal), or the end of a list (cdr-nil).
Data type checking: Data elements can be classified as specific types such as integers, floating point numbers, character strings, and flavor instances. These may be data type checked during run time as a part of instruction execution. Thus, datatypes are sure to match instructions.
Flavors: These are language features that support object oriented programming. Flavors are abstract data types, methods are generic operators, and objects are flavor instances manipulated by sending messages that are requests for specific instances of an operator.
Garbage collection: These are techniques for recovering parts of an address space that have been used to represent objects that are no longer accessible. Recovered memory can represent new objects.
Macroinstruction: A Lisp compiler translates Lisp source code into a sequence of macroinstructions—machine language instructions directly executed by the machine—not the same as microinstructions.
Microcode: Microcode is low level software that controls the internal data paths within a processor to execute macroinstructions. A multiply macroinstruction causes a processor to execute a sequence of microinstructions that fetch the operands, perform the multiplication, and store the results.
Microinstruction: A microinstruction controls a processor's internal data paths. It is stored in a microword and requires one clock cycle (microcycle) for execution.
Mouse: This is a handheld pointing device with two or three buttons on it for command entry. It has a tracker ball underneath or an optical mechanism. When moved, a cursor on a bit-mapped screen follows the mouse's movements.
Streams: A "software channel", often implemented with flavors, this is used to implement Lisp input and output.

Source: Adapted from Symbolics-furnished information.

New workstation market set to go

Which software environment will prevail is a moot point for designers who want a symbolic processing workstation now. Actually, what designers can get for their software development chores was determined some five years ago. The market for symbolic processing workstations, since the first of them were introduced (but not actively marketed) in the late 1970s by Xerox and in the early 1980s by LMI and Symbolics, has been geared toward AI researchers

using Lisp and its many variations. Market activity was rather dull until the AI field started to boom last year. Workstation manufacturers expanded their markets by touting their products' general applicability for software and hardware design work.

Estimates vary depending on who is consulted, but approximately 2000 machines have been sold by LMI, Symbolics, and Xerox as the first entrants in the field; with Perq, Tektronix, and Texas Instruments yet to establish a record (although TI reportedly sold hundreds of its new machines for delivery to the Massachusetts Institute of Technology in 1985 and 1986). In five years, say the pundits, sales could range from $1 to $2.5 billion depending on how successful the vendors are in convincing software designers that the Lisp software development environment is the way to go. Of course, no one knows what will happen if IBM or Digital Equipment Corp opts for Lisp and symbolic processing workstations.

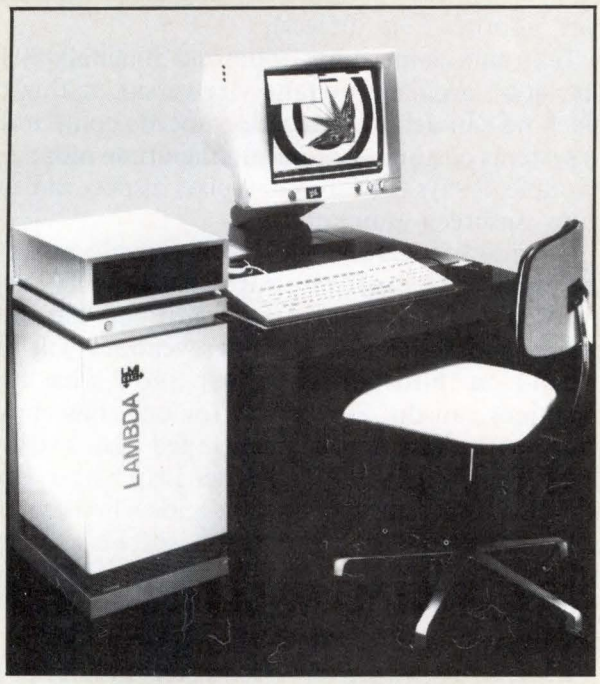
LMI and Symbolics are arch rivals. Each sees the other as the major competitor. Both see Xerox as unable to make money from the fine products that come out of the firm's Palo Alto Research Center. LMI and Symbolics have another link besides a mutual respect for Xerox's technology innovation and lack of concern for its marketing. Both firms were started by researchers from MIT's AI Laboratory (Cambridge, Mass)—and in fact pay license fees to MIT when they sell a machine.

LMI and Symbolics offer access to other computers and Lisp machines through an Ethernet local area network connection. And, both firms offer an interface to Intel Corp's (Santa Clara, Calif) Multibus based peripherals. But, the two groups have gone their separate ways and have incorporated some different technological approaches in their products.

Unlike Symbolics, LMI's machines feature internal printed circuit boards (and any the designer cares to add on) connected through the 32-bit, read/write only NuBus architecture. To some observers NuBus's processor independence makes it a prime candidate for the multiprocessor environment that high end workstations need to perform their varied chores. A contender for IEEE standard honors for a 32-bit synchronous bus, NuBus is an outgrowth of MIT work (see *Computer Design*, Feb 1984, p 27).

The synchronous NuBus is designed for a multiprocessing environment. For example, most LMI machines run both a Lisp environment from a proprietary four-board, bit-slice microprocessor set, and a Unix environment on a Motorola 68010 based board. On the other hand, LMI's latest workstation offering only handles Lisp.

Other entangling alliances exist in the symbolic workstation world. Taking a major software risk in going against the Lisp trend, Tektronix's symbolic processing software environment is based on Xerox's Smalltalk-80 language. This interactive, object and graphics oriented exploratory programming language developed at Xerox PARC has seen little use outside of the research community. Lisp and Prolog, however, are available as options—all on the machine's Motorola 10-MHz 68010 microprocessor.



As the seventh, most compact member of the LISP Machines, Inc family of symbolic processing workstations, the Lambda/E features the same bus architecture and software compatibility as the other models. Software designers can choose it as a delivery vehicle.

Available this month, the Tektronix 4404 sells for only $15,000. It is specifically designed as a low cost symbolic processing delivery vehicle and has smaller screen, disk, memory, and so on, than its more expensive cousins. Like its relatives, it sports bit-mapped graphics, a mouse, and networking.

Most dedicated, proprietary Lisp processors have instruction sets similar to Lisp statements. This facilitates Lisp language implementation. In contrast, Tektronix's 4404, as mentioned earlier, has a 68010 microprocessor, and for good reason. The firm's main markets include instruments and workstations. So, it wanted a symbolic processing machine that could serve these applications. As a result, Tektronix designed its workstation to run the object oriented Smalltalk programming language, which it feels is ideal for its customers and in-house designers. Because it is architecturally configured for Smalltalk, the 4404 is less in need of a processor whose instruction set mimics the Smalltalk language.

Graphics oriented Smalltalk supports its applications, Tektronix says, because it easily handles logic diagrams, circuits, and schematics. Even text is treated like graphics. Tektronix has in-house applications for instrument trouble-shooting, using its

4404, which also supports Prolog and Franz Lisp (yes, another Lisp dialect).

Tektronix claims it has optimized Smalltalk-80 for the 4404's architecture (and vice versa), so that the machine can achieve execution speeds comparable to systems costing an order of magnitude more. For example, it says the 640- x 480-pixel display can even show onscreen animation.

Outside software vendors will provide much of the applications software support so the 4404 will be used for a variety of software and hardware design chores. Certainly, other vendors will also depend on third parties to help show what their machines can do. Symbolics, for one, has chosen to show the way and has developed Lisp software for a chip design. But, like other Lisp based workstation manufacturers, it must decide whether it will go into full-fledged application software design. Most likely, Symbolics and its competitors will just develop software for general uses and depend on third parties and customers for the rest.

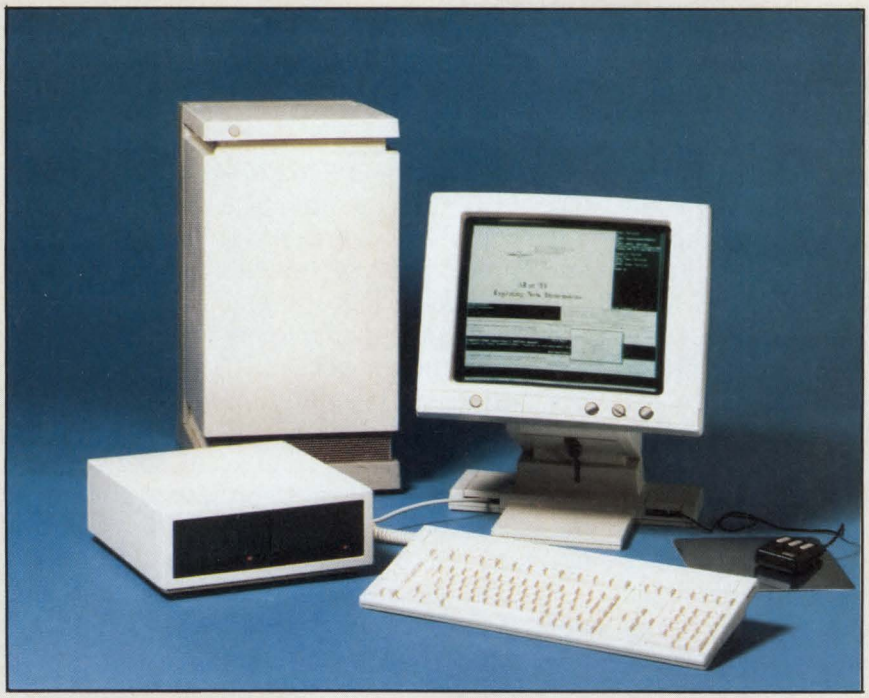
LMI, Symbolics, and Xerox offer families of far more powerful machines from both hardware and software points of view. These have been written about extensively, although new developments continue apace. For example, Xerox just announced a personal computer connection for its Model 1108; LMI just announced the seventh machine in its Lambda series; and so on.

Actually, LMI's new machine points out yet another alliance in the symbolic processing workstation business. The $52,500, single-user Lambda/E, as the workstation will be known at LMI, is more

Tektronix, Inc is making its mark in the world of symbolic processing workstations with its 4404. Designed around the Motorola 68010 and the graphics oriented Xerox Smalltalk-80 programming environment, the workstation is geared to help hardware designers.

or less a repainted TI Explorer (see "Lisp Workstation Brings AI Power to a User's Desk," on p 155 of this issue). LMI, under president Frank Spitznogle a former TI employee, is owned in part by TI (some 9 percent of the privately held firm). Furthermore, LMI uses two TI properties obtained from MIT: the NuBus and the NuMachine.

TI just swung a deal with MIT to sell hundreds of Explorers. Thus, TI, in one fell swoop, will become one of biggest vendors of symbolic processing machines in terms of units sold. TI benefits in being put on the symbolic processing workstation map overnight. But, more important, it may be following AT&T's Unix strategy: AT&T seeded the



The ergonomic Texas Instruments Explorer workstation for software development in a Common Lisp environment is designed for the office and may be variously configured. The seven printed circuit board slot main chassis fits under a desk or may be 168 ft away.

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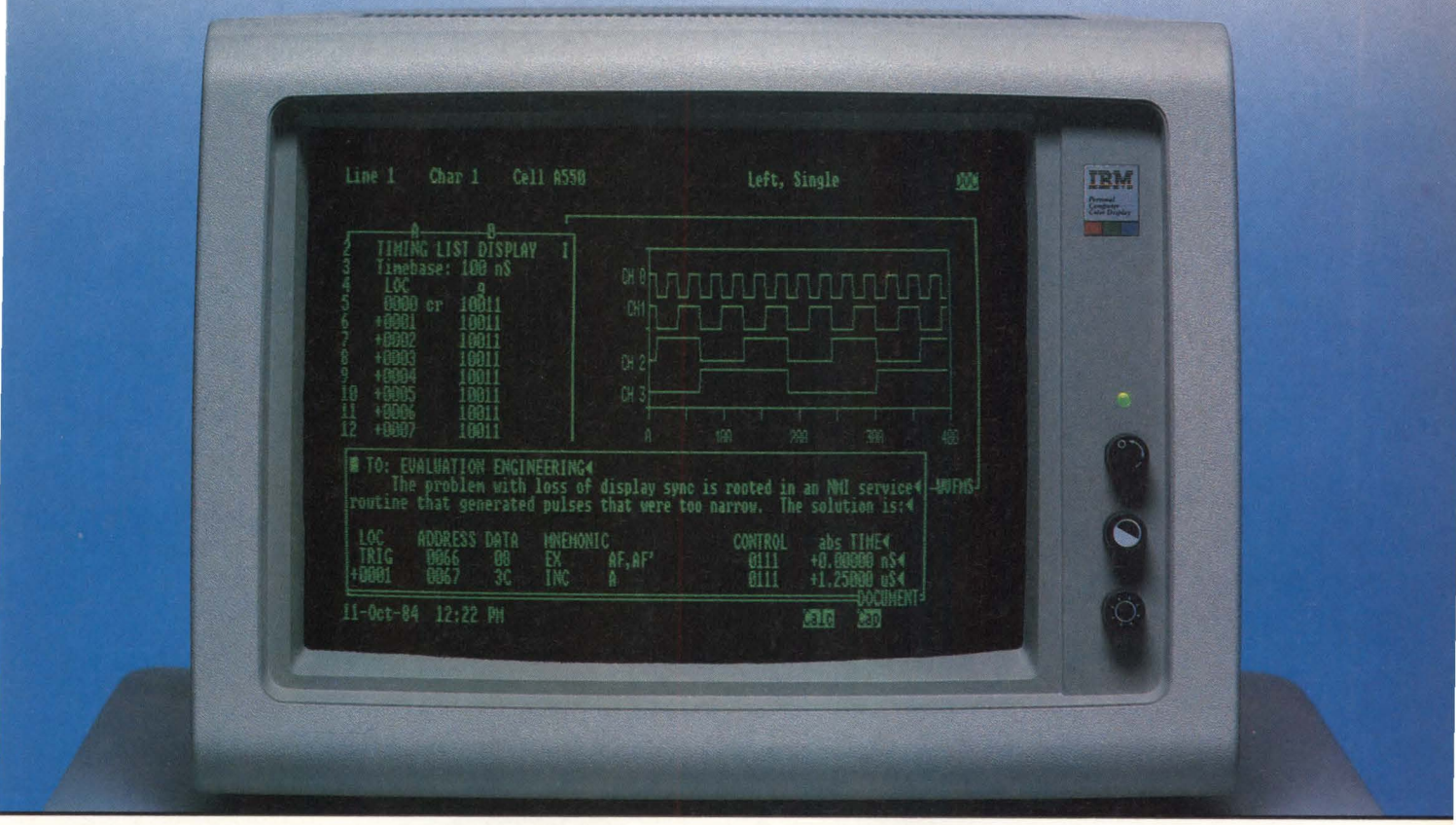

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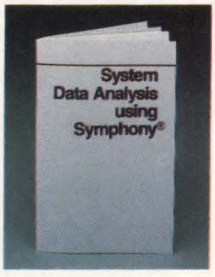

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Unix software system and its environment in universities at preferential prices for many years. As a result, the software community is trained in Unix and demands it wherever it goes. TI may hope to do the same with its machines and Lisp environment.

TI has just received a $6 million, 27 month contract to reduce most of the Lisp processor circuitry onto one VLSI chip. Compared to the four printed circuit boards used in the LMI machines to implement a Lisp processor and the one board used in the Explorer, the savings in space, power cost, and reliability in having a single-chip implementation cannot be underestimated. The block diagram (see "Lisp Workstation Brings AI power to a User's Desk," p 155) of the Explorer processor implemented with ALUs and other parts gives some idea of the complexity of the endeavor, which will take hundreds of thousands of transistors and the latest process technology to implement in VLSI. Symbolics, under president Russel Noftsker, is said to be working on a Lisp chip. But, it is hard to see, unless it makes a connection with another major semiconductor firm, how Symbolics could come up with what is needed since it is not in that business.

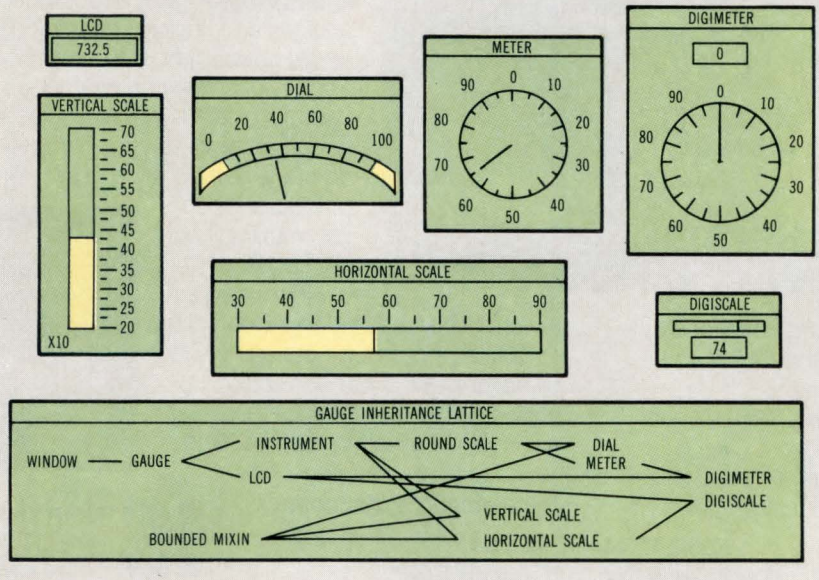
Meanwhile, Xerox is now taking the symbolic processing workstation market very seriously. On the one hand, it has reorganized for greater marketing strength; on the other hand, it possesses first-class technology and is a research leader. For example, the firm is making a research prototype of the Loops environment that is available for its 1100, 1108, and 1132 symbolic processing workstations.

Loops is an extension of the Xerox Interlisp-D programming environment. It combines all the techniques of advanced programming styles such as procedure, object, data, and rule orientation. Not a final product, Loops is another innovation from PARC, where it is still under development. It is available for license for internal use for merely a distribution cost. If Loops is successful, it will be one test of the marketing smarts of Xerox's newly organized Artificial Intelligence Systems Business Unit under Gary S. Moskowitz. Note however, that Loops is unsupported; if the designer has a question, there is no official number to call.

Special this week only

TI is not alone in seeking to develop the academic marketplace for Lisp environment workstations. For example, Perq Systems Corp (formerly Three Rivers Computer Corp) is providing discounted packages for university users of its proprietary bit-slice, processor based LN-3000 symbolic processing workstation, Accent operating system, and Common Lisp environment—all on the Ethernet based Linq local area network. The firm provides a variety of file, print, computation, and other servers for the network. It has designed Accent to be portable so that other, non-Perq, machines on the network can use it. The system is geared to distributed processing for multiple users. Company president Aaron Coleman hopes it will serve the low cost symbolic processing workstation market.

The Common Lisp environment is microcoded and microprogrammable, and features tagged data structures. Moreover, it is supported by a message passing, 32-bit virtual memory addressability, multiprocessing operating system (Accent) that supports multiple, co-equal user environments and multiple, co-equal instruction set architectures. Developed in conjunction with Carnegie-Mellon University (Pittsburgh, Pa), Accent simultaneously supports its own



With Loops symbolic processing, gauges are tools to monitor variable values; they are probes inserted into program variables. The "browser" at the bottom shows the relationships between classes of gauges. For example, a digimeter is a meter and an LCD.

native environment, as well as Qnix (a Unix System V environment) and a Common Lisp environment.

Under window manager software, different screen windows can run different environments as the designer requires. The native operating system also changes workstation instruction sets dynamically, depending on the language of the process it is executing, so that process speed is optimized. Supported languages include Pascal, C, Fortran, and Lisp.

Inside Lisp machines

Specialized hardware is found in symbolic processing workstations. Moreover, since symbolic processing programs are large and complex, the hardware is designed for efficient program development, as well as efficient program execution. Program development efficiency features include high resolution, bit-mapped, physically large graphics displays with overlapping windows, and mice. Execution efficiency features include large memories, optimized processors, networking capabilities, and interactive, integrated program development tools.

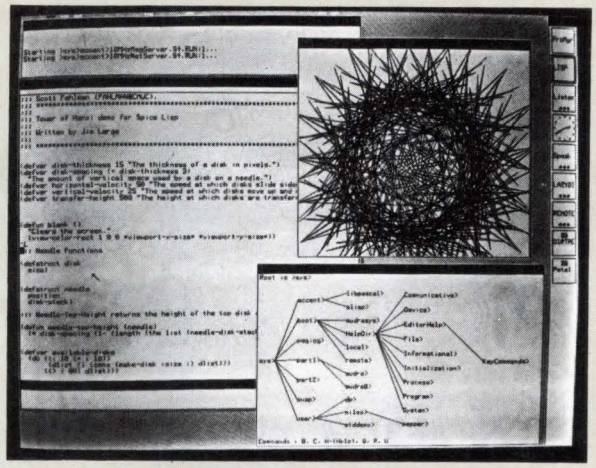
Symbolic processing programmers who used these machines originally for AI work need these features not only because their programs are large and complex, but also because their programs are usually ill-specified and ill-understood at the start. Today, it is realized that such hardware/software combinations are the best development environments for any large, complex programs—AI or otherwise—since, in reality, they are all ill-specified and ill-understood before they are actually written by software designers.

For program execution efficiency, one important feature in symbolic processing computers is a hardware supported, parallel processing, or pipelined architecture. Not as advanced as the parallel processing architectures for fifth-generation computers (see *Computer Design*, Sept 1984, p 104), this architecture allows an operation within one symbolic processing instruction to be executed in parallel with another. This speeds up the overall instruction execution pace.

Another execution efficiency feature is a microcode compiler. It compiles Lisp program source code directly to the "lower" than machine code level Lisp processor instructions known as microinstructions. A microcode compiler is not often seen on conventional machines and is one of the hardware architecture features that makes symbolic processing workstations unique.

The same but different

Just as conventional machines with a Lisp environment are different, so are dedicated machines. For example, Xerox machines are supposed to feature lower cost and the best programming environment as a trade-off against execution efficiency. On the other hand, LMI and Symbolics have first-class programming environments and frequent price cuts, as well as efficient symbolic processing program execution. Yet, they approach the speed problem in different ways.



While the software environment is all-important for symbolic processing, hardware must support the development effort. The Perq LN-3000 workstation can sport up to 2 Mbytes of RAM, two RS-232 interfaces, two 5¼-in. Winchesters, an 8-in. floppy, and more.

The LMI Lambda workstations gain speed through the use of a microcode compiler that compiles programmer-written Lisp source code directly into microcode. Microcode is a low level code that specifies the internal control signals for the internal parts of a microprocessor, such as registers. The compilation step skips the conventional, intermediate assembly and machine code steps. Difficult to do because it addresses the most basic operating level of a processor, microprogramming is even tougher than assembly language processing. It requires the ultimate in software skills. But, it is said to be worth it because of increased execution speed.

For its design, Symbolics has a tagged architecture supported by hardware along with a more conventional compiler for converting Lisp source code. Tags are bits that identify data attributes, such as data type or operand length. Compiler set, they are used by the symbolic processing workstation to quickly and reliably determine the type of operations to be performed. In contrast, conventional workstations define data type information with program instructions.

Tagged data has many advantages. It allows for generic instructions and needs only one type of addition instruction. Which type of addition is to be performed (say integer or floating point) is determined by examining the tag bits of the instruction operands. Clearly, the number of instruction types that has to be handled in a tagged architecture is decreased compared to other designs. This simplifies tools, compilers, editors, and so on. This is especially important because the complex parts of Lisp

programs need time for memory management and garbage collection. Any execution speed enhancement they can get is a plus.

Symbolics supports its tagged architecture in hardware. For example, with tag bits, execution speed is gained because data type checking is performed (by hardware) in parallel with instruction execution. The hardware support is said to speed execution even more. Nevertheless, like the choice of a Lisp dialect or the deciding of which editor is best, the use of a microcode compiler, or a tagged architecture, or both, is a matter of personal preference.

Of mice and windows

Symbolic processing requires the viewing and manipulation of much information on a display screen. To do this requires multiple windows on large, very high resolution screens under mouse control. Windows allow symbolic processing software system developers to build their systems in parts and view each part as needed.

In other words, with windows, software developers can build their programs in a natural way. In the real world of software development, programs are not written sequentially, but in a "back and forth" mode. With windows, programmers switch back and forth between various parts of the system and learn from their work as they do it. Note that, in contrast to the windows on conventional workstations, windows in symbolic processing workstations can be "objects" in the object oriented programming paradigm. Thus, they are far more than just part of a screen display. For manipulating many windows on a screen, a mouse is simply faster and more flexible than a set of keyboard commands could be; to the user, it acts as a screen pointer control.

The high end Symbolics 3670 symbolic processing workstation has all the hardware needed to support a Zetalisp environment. Flavors, an object oriented Lisp extension, and a variety of integrated Lisp based software tools such as editors, windows, compilers, and debuggers, are also provided.

Stay loose

As mentioned, symbolic processing programs are large and complex and the environment to develop them must be user friendly in the extreme and support totally open-ended, exploratory, experimental programming. Most software and hardware designers really do not know much about their code until a late stage in program development. They need an environment that allows for this uncertainty, since they do not know what software (and hardware) resources they will need.

For example, traditional program development takes place in a static environment. Before program execution, a compiler knows all about subroutine and data object lengths and types, as well as memory locations. The compiler works with the operating system's linkers and loaders to set up fixed static software structures to handle the program under development. In contrast, in a symbolic processing environment that serves exploratory programming, matters are too changeable for static techniques. The environment is dynamic: subroutine sizes change and are redefined dynamically (perhaps at execution time). Variables suffer the same problems. In short, with experimental programming and changes at both compile and execute time, not much is known about what will happen to data types, variables, and the like. The development environment must not require these and other software parameters to be specified beforehand.

A Lisp environment does not require advance notice of what the designer is going to do. But, with every blessing there is a curse, and a Lisp environment is no exception. There is no single, standard Lisp language: there are dialects, and the dialects have dialects. Bolt, Beranek & Newman and Xerox, came up with Interlisp; Maclisp (and its descendants) came out of MIT. These are the major Lisp versions. It may be said that Interlisp emphasizes its user interface and performance is Maclisp's strong point—but some experts demur.

Xerox's 1100 workstation series runs Interlisp-D with an editor that edits the actual data structure that represents a program. It does not edit files. This approach reduces editing errors and makes it easy to write programs that can modify other programs—important for an experimental environment. The price of all this, some say, is performance speed because of the software overhead involved in the user interface.

The Interlisp data structure approach somewhat restricts programmer experimentation with imperfect program structures. In contrast, the Zetalisp environ-

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ment edits programs as text files rather than data structures and is said by some not to suffer this disadvantage. The argument rages with proponents on both sides—many with a view sympathetic to their employer's view. Both Symbolics and LMI have opted for Zetalisp, a Maclisp superset.

The arguments also rage as to which Lisp environment is "better." The answer depends on one's definition of better and, like most language choices even for conventional programming languages, comes down to personal preference. Editing files rather than data structures, the degree of integration of tools and the kinds of tools, emphasis on minimal or a more complex software structure, and the kind and level of programmer restrictions are the major differences between Interlisp and Zetalisp. In partial solution of the problem and recognition of marketplace realities, Symbolics and LMI offer Interlisp-compatible packages so that Zetalisp users can debug and run Interlisp programs. Moreover, both companies' workstations run Common Lisp, a Maclisp dialect out of a university and industry consortium.

As might be expected, conventional programming languages are also handled by symbolic processing workstations. For example, Symbolics has integrated Fortran-77, Pascal, Ada, and C into the Zetalisp environment. For its part, LMI workstations feature both a Motorola 68010 processor for Unix, as well as a proprietary Lisp processor. The Unix processor supports C, Pascal, and Fortran-77. The idea of all this is to have the mentioned high level languages produce Lisp code when they are compiled so they may have access to the symbolic processing workstation's software development tools. Ada is supposed to have its own set of sophisticated software development tools, so its porting to the Lisp environment is controversial. With all that development effort on Ada tools, some observers ask, what do we need a Lisp environment for?

Object orientation

It turns out that Lisp is not enough. All the symbolic processing workstations extend Lisp with some form of object oriented programming. An object is a data structure that combines data with procedures and attributes about the data (see *Computer Design*, Sept 1984, p 150). When programmers define an object, they also define its operations (behaviors). These are known as methods. In contrast to conventional programming, an object rather than a procedure is important in object oriented programming.

Xerox Corp's Smalltalk, used in the Tektronix symbolic processing workstation, was the first object oriented programming language. It has not been integrated with the Xerox Interlisp environment and is ideal for graphics activities. The Xerox workstations can integrate yet another object oriented language known as Loops into the Interlisp-D environment.

For their part, LMI and Symbolics offer Flavors as an object oriented programming system. A "flavor" is like an object and exists as part of a data structure hierarchy with inheritance features. There are subtle differences between Flavors and Smalltalk, which are of interest to computer scientists and programmers. For designers, the difference can be significant—flavors can inherit characteristics from hierarchically unrelated multiple parent flavors, objects cannot.

Object oriented programming is useful for the symbolic processing software developer because it enhances experimentation. All program segments are modules that are extensible and reusable. A change in an object's structure requires little if any program modification. This is the opposite of what happens in most conventional programming where changing one line of code can propagate changes throughout the program. In short, object oriented programming methods shield users from program implementation problems and speed the design of large programs when change is constant.

Software development

The symbolic processing workstation's user interface is geared to exploratory programming and rapid software prototyping. This interface combines a host of software features into one integrated whole that watches over the user. For example, tools in the interface environment know the syntax rules of the Lisp dialect in use. The tools work with the programmer and track changes made to records, files, variables, or data structures. They recompile code when necessary, or reconstruct programs that were derived earlier so progress can be checked. These functions can occur automatically without programmer intervention.

Tools accommodate program editing, debugging, incremental compiling, dynamic linking, and program management. They also perform standard functions like electronic mail. But, it is not the individual tools that are special for program development. Some similar tools may be had on mainframes and conventional technology based workstations.

For example, the Unix programming environment on minicomputers is famous for its tools. But, these usually are not integrated. A software developer must use one tool at a time to modify a file, operate on it, save it, exit the tool, perhaps enter another tool, or repeat the whole tedious, error prone process. This is an inefficient procedure that eats computer and design time.

Lisp based computers have no such problems because their tools are fully integrated. Software developers switch between tools totally under editor control; it is not necessary to leave the editor at any time and efficiency is greatly enhanced. For example, a designer can log in to the editor, edit a program, compile a segment, and execute, all in the

editor environment. If an error is found, the editor allows programmers access to a window oriented debugger that traces the program. The editor can fix the bug, and continue program execution from the point where the error occurred. All this integration is possible because, among other reasons, the Lisp machine's large address space can handle the Lisp language, its large tool programs, linkers, loaders, and more, in memory.

Personal computer connections

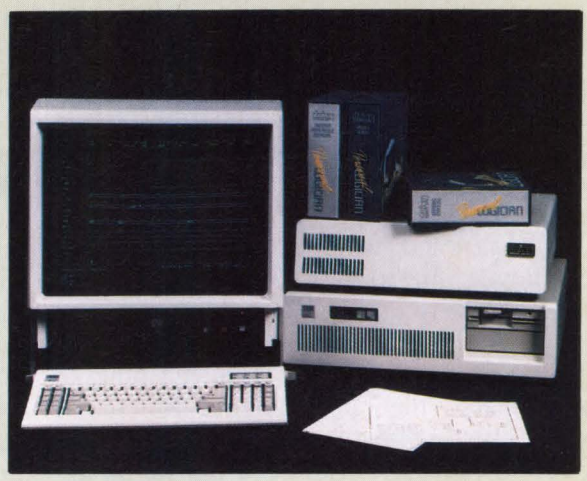
As versatile as Lisp environment workstations are, they do not stand alone in today's networked office and laboratory environment. Be it through networks or direct links to every machine from mainframes, other symbolic processing workstations, file and print servers, and inexpensive personal computers, the symbolic processing workstations communicate with the resources of every other computer in a locale.

While local area networks are starting to appear everywhere in the corporate environment, the IBM PC has already done so. It has become a personal productivity tool found almost everywhere. Both Xerox and Daisy Systems Corp (Mountain View, Calif) have reacted to this phenomenon by allowing certain of their machines to directly link to IBM PCs. Other firms are following the example.

For Xerox, a personal computer to Lisp environment workstation link (available the first quarter this year) means an interface option for hooking its 1108 workstation to the IBM extension card cage. The purpose, Xerox says, is to allow the 1108 to access the wide range of PC peripherals, such as color monitors, and use PC features, such as an analog/digital speech input as an 1108 input.

Xerox is also making use of the Ethernet local network to hook the 1108's Interlisp-D software through a streams interface (Lisp's equivalent of the Unix pipes communication mechanism) to other corporate sites. In fact, the 1108 can be made to conform to the layers of the Xerox network systems architecture (XNS)—the firm's analog of the International Standards Organizations seven layer model for computer communications. Not all the functionality of all the layers has been implemented but layers one and two (the physical and data link layers corresponding to Ethernet) are available, as are upper layer facilities for print and file serving, electronic mail, and more.

A similar approach is taken by LMI, which features a software conversion from Lisp streams to Unix pipes (using its Lambda machine-resident, Unix processing Motorola 68010) which can then be transmitted on a local area network or directly to other computers. Like any networking scheme, the purpose of all this is to allow sharing of resources—even mainframes. TI is a natural for a software development connection between its new Explorer symbolic processing workstation and its Professional personal computer. The two machines have a unique set of AI software based development tools that can run on both of them. Thus, Explorer developed applications for conventional engineering offices could run on the Professional (and vice versa), which TI uses in-house for engineering design and personal productivity, and is selling to the outside world.



Daisy Systems Corp ports its Personal Logician software to the IBM PC AT. With an Ethernet connection, designers will be able to tap Daisy's high end Logician workstation with its data flow architecture based PMX hardware accelerator.

Go with the flow

Daisy has also made a PC connection. The firm says it has signed on as an IBM value-added reseller. Thus, its Personal Logician computer aided engineering software runs on the IBM PC/XT. Engineers will enjoy, in one terminal on their desks, CAE with the XT's word processing, spreadsheets, and integrated programs. A high resolution color display rounds out the package. Since the XT can be a networked front end to full scale Daisy machines on Ethernet, can Personal Logician software on the IBM local area network (see *Computer Design*, Oct 1, 1984, p 27) be far behind?

Even more important for the designer who wants to take advantage of advanced workstation technology, as a node on Daisy's Ethernet local area network, the Personal Logician can upload XT developed information to the data flow architecture based physical modeling extension (PMX) on the high end Daisy machine known as the Logician PMX (see "Data Flow Concepts Speed Simulation in CAE Systems," p 131). Furthermore, Daisy says that the new Intel 32-bit 80286 based IBM PC AT (ultimately a multi-user system) will run the Daisy Personal Logician software.

As the Daisy data flow architecture proves, workstation advances are not restricted to developing symbolic processing environments. The machine's architecture offers several benefits to the designer. Indeed, a host of advances in hardware design and parallel computer architectures are in the wings, although few practical products for workstations are now available.

Calling for a distributed CAE environment, Daisy will allow engineers with room for just one machine at their desks to do logic entry, perform engineering and simulation functions in an AT environment and upload the results to larger Daisy machines for more sophisticated high performance functions. Daisy figures it will sell high end machines for each clump of XT or AT users who need not tie up an expensive, high end machine with low end chores.

While its data flow architecture is unique, Daisy has lots of competition with many firms providing personal CAE software for the PC. They can take care of the low, such as net lists and schematic capture, but these firms may be hard pressed to fight the Daisy/IBM access to data flow based machines for high end design.

Conventional computer makers move in

Manufacturers of conventional computers and their associated workstations will not leave the symbolic processing market to dedicated Lisp machines. Until last year, of the traditional computer manufacturers, only DEC actively marketed symbolic processing on its PDP-10s, 20s, and VAXs. But, when the trend started to move symbolic processing out of the AI domain, other firms entered the field.

TI and Tektronix opted for the dedicated symbolic workstation route. Other firms, including IBM, Data General, Prime, and Apollo, modified their existing machines to do the symbolic processing job. Most of them opted for Common Lisp as best suited for conventional machines; few disagree with the claim that dedicated machines and tools are better for high end applications. For example, the degree of integration of tools in the Lisp environment on conventional computer workstations is far less than that of dedicated machines. And, object oriented programming is usually not available.

On the plus side, Lisp in conventional computers may be added at low cost to access data bases, programs, and programming languages that are familiar to hundreds of thousands, not hundreds of programmers. The same is true for Lisp machines. Conventional work can go on while symbolic processing benefits are explored.

The general purpose computer companies are enhancing their symbolic processing capabilities with different Lisp dialects and associated tools. For example, DEC's VAXs, and Data General's Eclipse family run Common Lisp and other dialects. Apollo's Domain network and workstations support, "Portable Standard Lisp," which is smaller than Common Lisp. For its part, IBM announced that, all along, it has had its own Lisp that runs on 370, 4300, and 30XX systems under the various IBM operating systems.

All these firms have their own versions of a development environment with edit, compile, link, debug, and execution functions from within the editor. And, they allow conventional software to be called from the Lisp editor. But, there are differences in overall system characteristics, such as number of windows, mouse usage, and graphics. Moreover, there are execution speed differences, limited resources such as disk and memory availability, problems with a timesharing environment, and so on.

Still, all of the mentioned vendors allow varying degrees of symbolic processing on their conventional computers and workstations. The designer who cannot afford a spanking new Lisp machine, or who only wants to "fool around," or has low end problems to work on, may find the conventional machine approach cost-effective—especially if the symbolic processing capability need only be added to an already purchased machine in the next room.

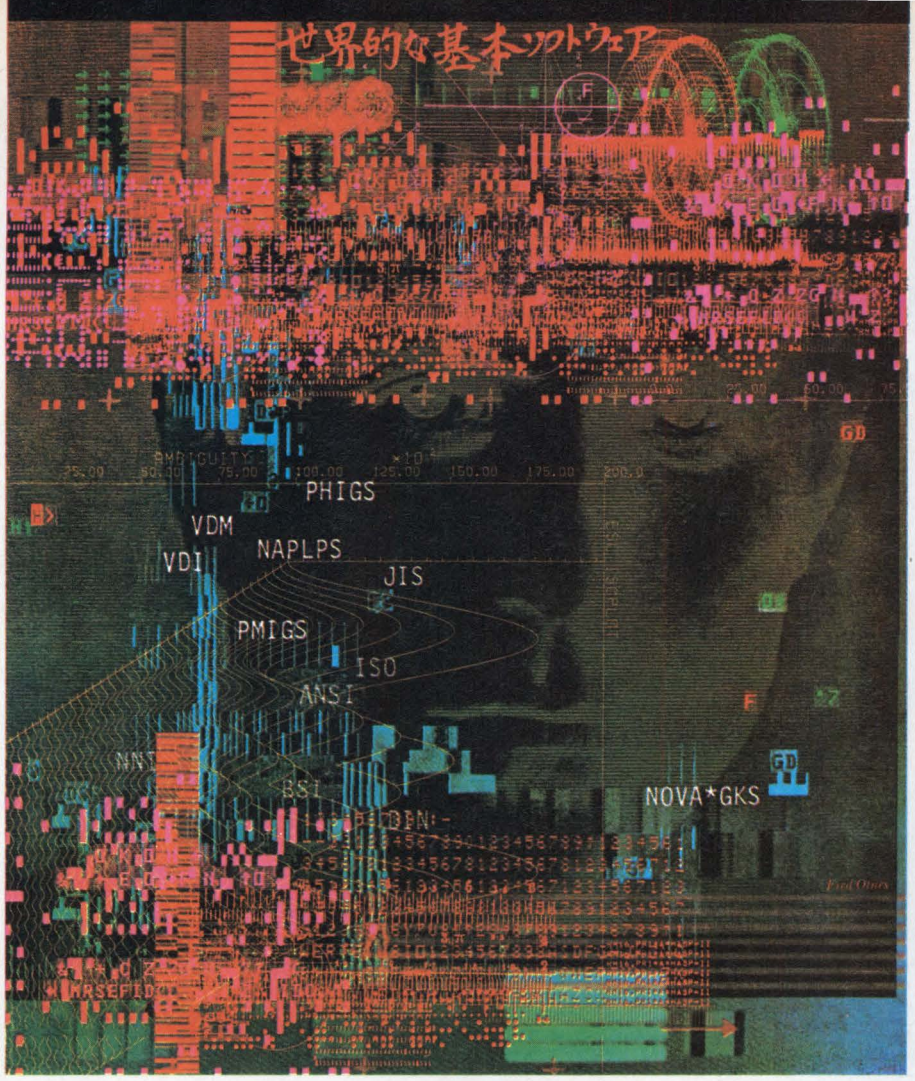
Still another approach to low cost symbolic processing experimentation is typified by Sun Microsystems, Inc's (Mountain View, Calif) marketplace offering. The firm has just introduced an under $10,000 workstation known as the Sun-2/50. Featuring a Motorola 68010 and the Unix 4.2 BSD operating system, this "diskless node" workstation can communicate over Ethernet to all the workstations in the Sun family.

But, most important for the symbolic processing devotee, Sun's third party software sources are making a variety of symbolic processing software products available to the Sun workstations. These include Prolog, Common Lisp, symbolic processing utilities, an applications development environment, and other symbolic processing software, as well as the Franz Lisp dialect. Thus, the designer with access to standalone or networked Sun workstations will be able to do exploratory programming work in a symbolic processing environment.

Application programs

While Symbolics has designed a chip for an optical mouse on its machine using symbolic processing, and TI makes a variety of symbolic processing application programs available for its Explorer, other firms are not idle. They are both developing software for symbolic processing applications on their own and negotiating with third parties to do the job.

A lot of this activity is related to chip design so, ultimately, computer designers in need of a custom or semicustom VLSI part, but unable to get



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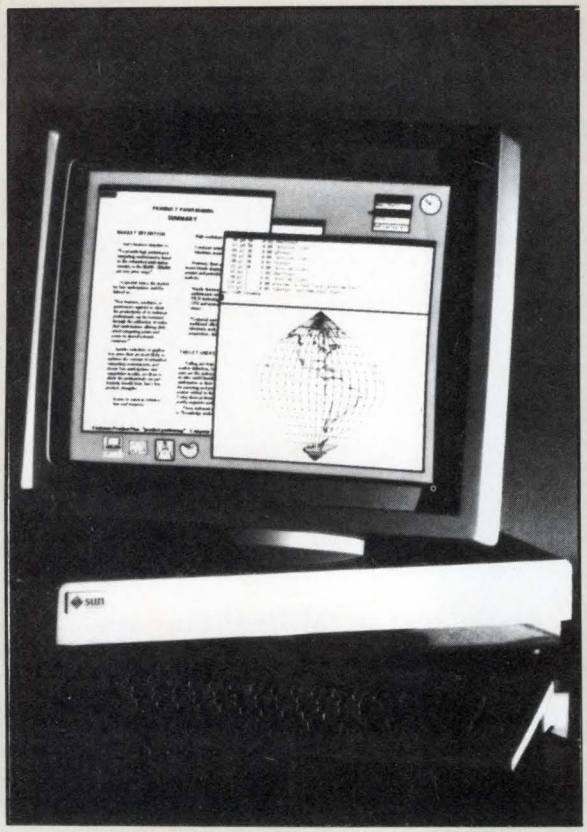

The Sun Microsystems inexpensive, diskless, networkable workstation accesses third party vendor-supplied symbolic processing software. The designer can enjoy the benefits of Lisp and Prolog, as well as the Unix 4.2 BSD operating system—all on a 32-bit 68010 microprocessor.

it from conventional sources because of limited demand, will be able to "roll their own." Specific programs to perform some of these designs will appear this year. And other more advanced programs are under development.

For example, expert systems running on symbolic processing workstations hold the most hope of aiding the chip design tyro in design chores. So far, the layout and design problems have been too complex for all but the simplest chips and expert systems. And, often, what comes out of these systems is not as good as what a human designer could do.

Some observers say that Lisp workstation environment based expert systems will act as a designer's assistant or design consultant. Still in the research stages, VLSI design consultant software would provide advice and suggestions for VLSI designers. It would act much like editors, debuggers, and other Lisp environment tools for software program development.

A typical VLSI design consultant understands the purpose of various chip components, such as memory and ALUs. For example, it can examine the trade-offs in making discrete connections between components using multiplexers, buses, or point to point links. Much work has been done in this area at Carnegie-Mellon University. And, although projects are still under development, Silicart, Inc, a custom chip house in Montreal, Canada, uses Lisp as its VLSI design environment. In addition, MOS circuit simulation is underway in a Lisp environment at the University of California, Berkeley's Electronic Research Laboratory and a Lisp based expert system for circuit schematic creation is under study at the Honeywell Computer Sciences Center in Minneapolis. In the Honeywell work, both OPS-5 and Flavors symbolic processing environments assist the Lisp environment.

Lisp environment add-ons such as object oriented programming can facilitate VLSI design. VLSI programs handle a large number of logic devices and transistors. As the number of elements the program must handle increases, the time and memory needed to handle these elements increases rapidly. Here, object oriented programming simplifies VLSI design by letting the designer associate procedures with the different components and data structures of the design. The components and data structures each know how to execute these procedures.

Circuit additions, deletions, and modifications are made easier with object oriented programming because it is not necessary to know all the components that could be adversely affected by changing a procedure. Thus, code changes are minimized when a design change is made. In other words, since information about a component is encapsulated with that component and hidden from others, the object oriented programming provides modularity, which reduces the chance of errors.

The organization of components into inheritance hierarchies in object oriented programming also provides benefits for designers interested in rapid prototyping. For example, procedures and attributes of components low in the hierarchy are inherited from their parents. As each lower level component or circuit is created, it knows how it is related to others already created. The designer need not worry about rewriting code, errors are reduced, and designed components behave in a consistent manner.

Expert systems running in Lisp environments are not just to aid the chip designer. Many of them function as assistants or consultants for other applications which, in the future, will form a fertile field for exploratory software designers.

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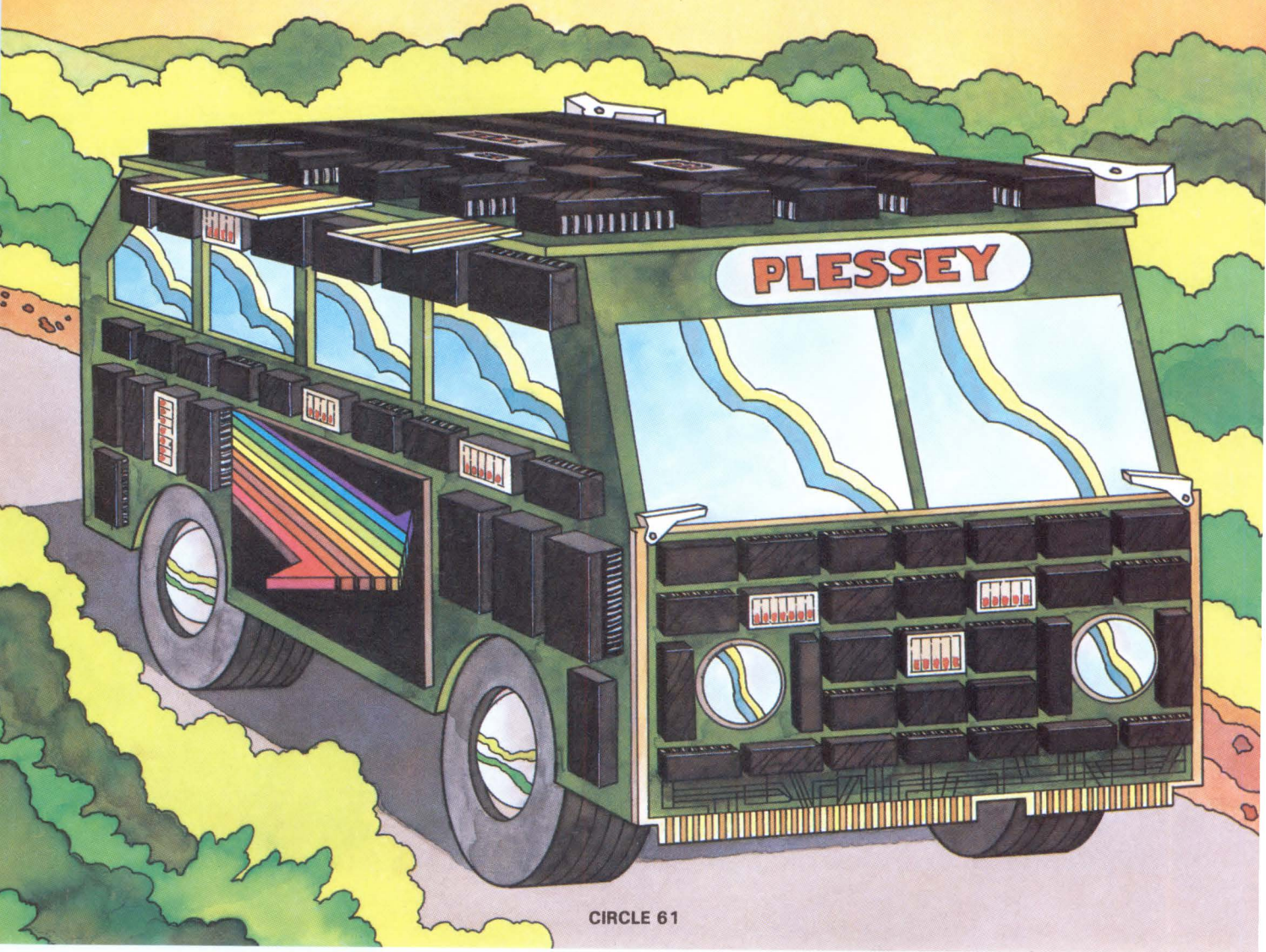

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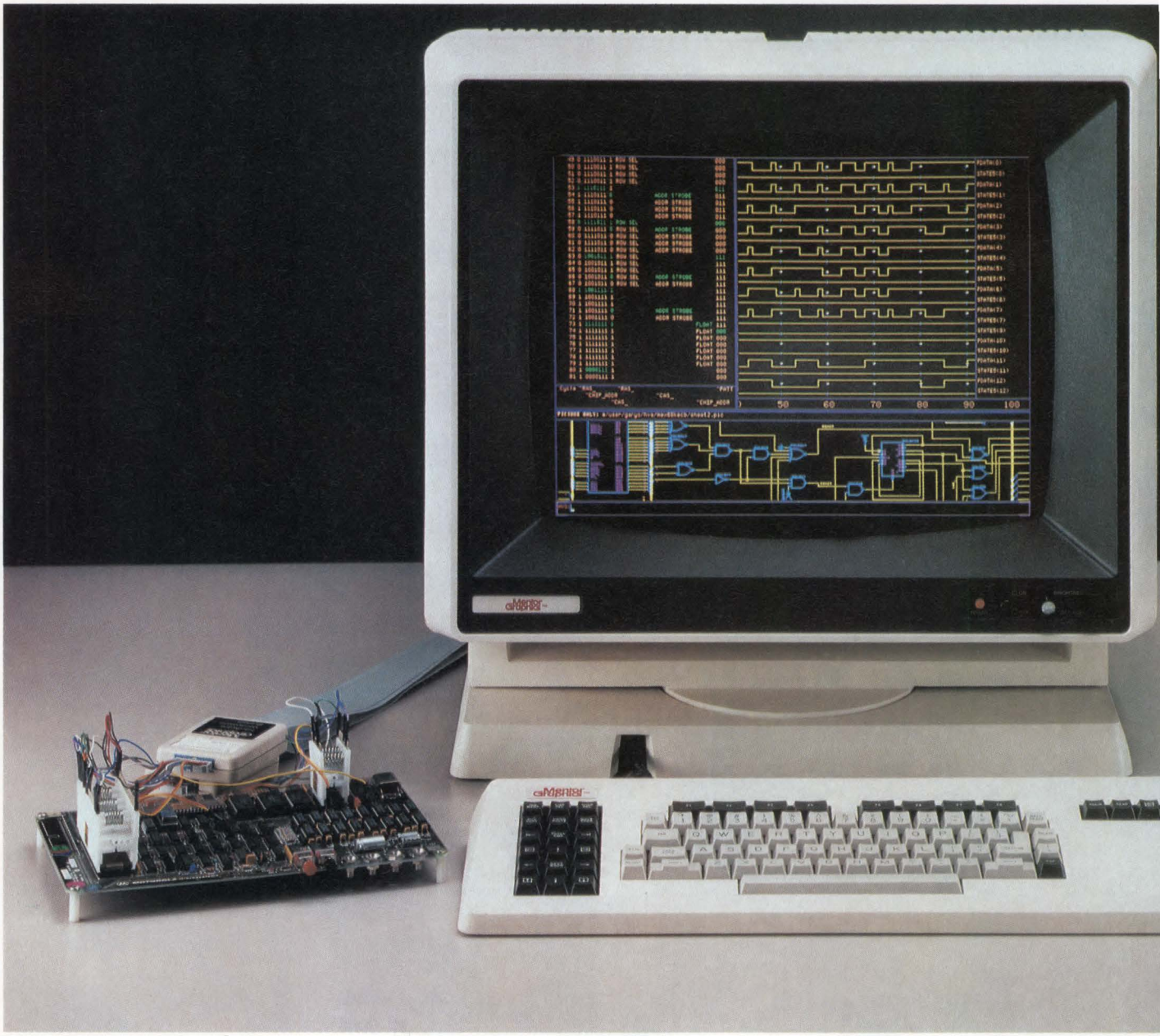

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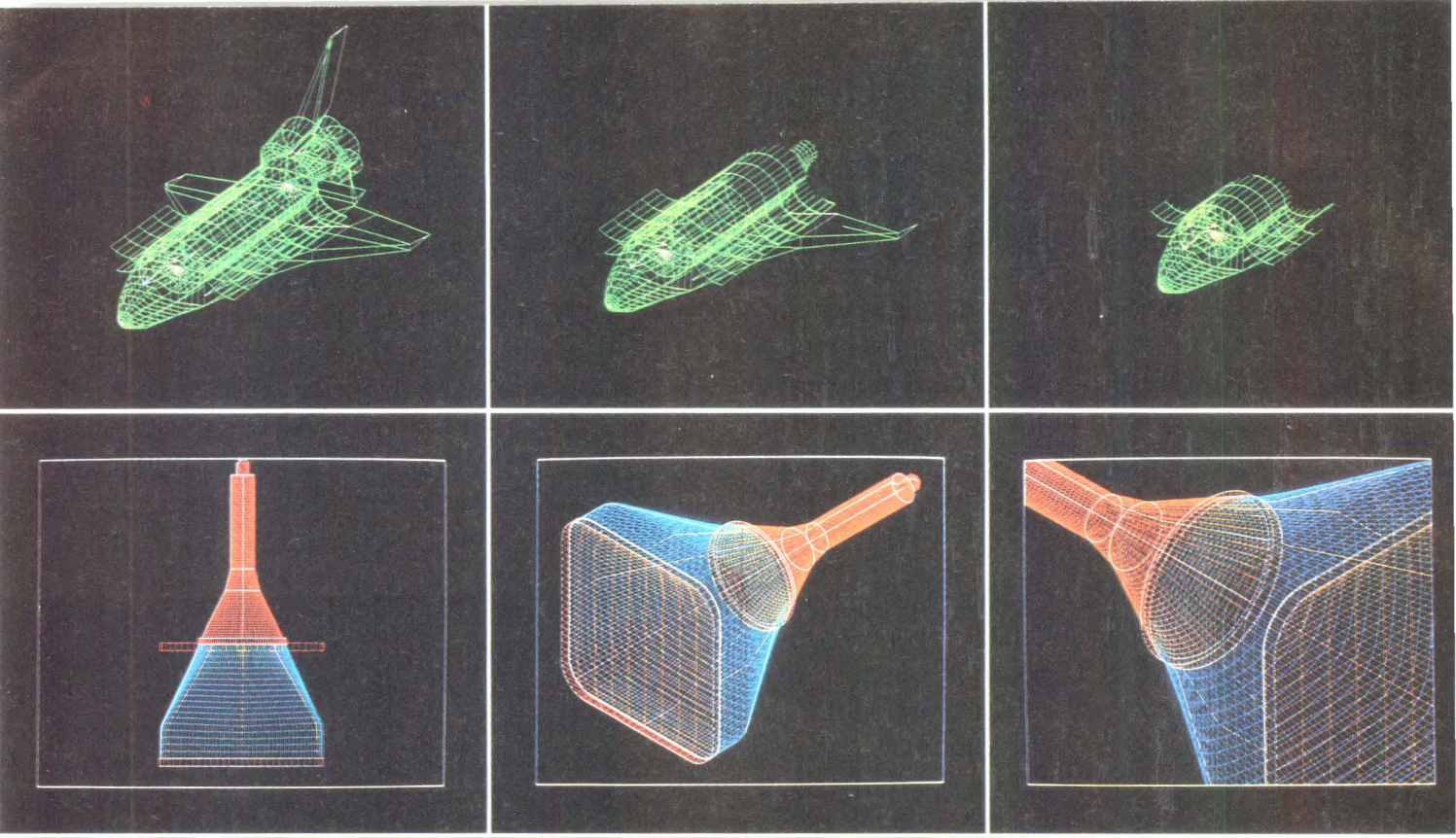

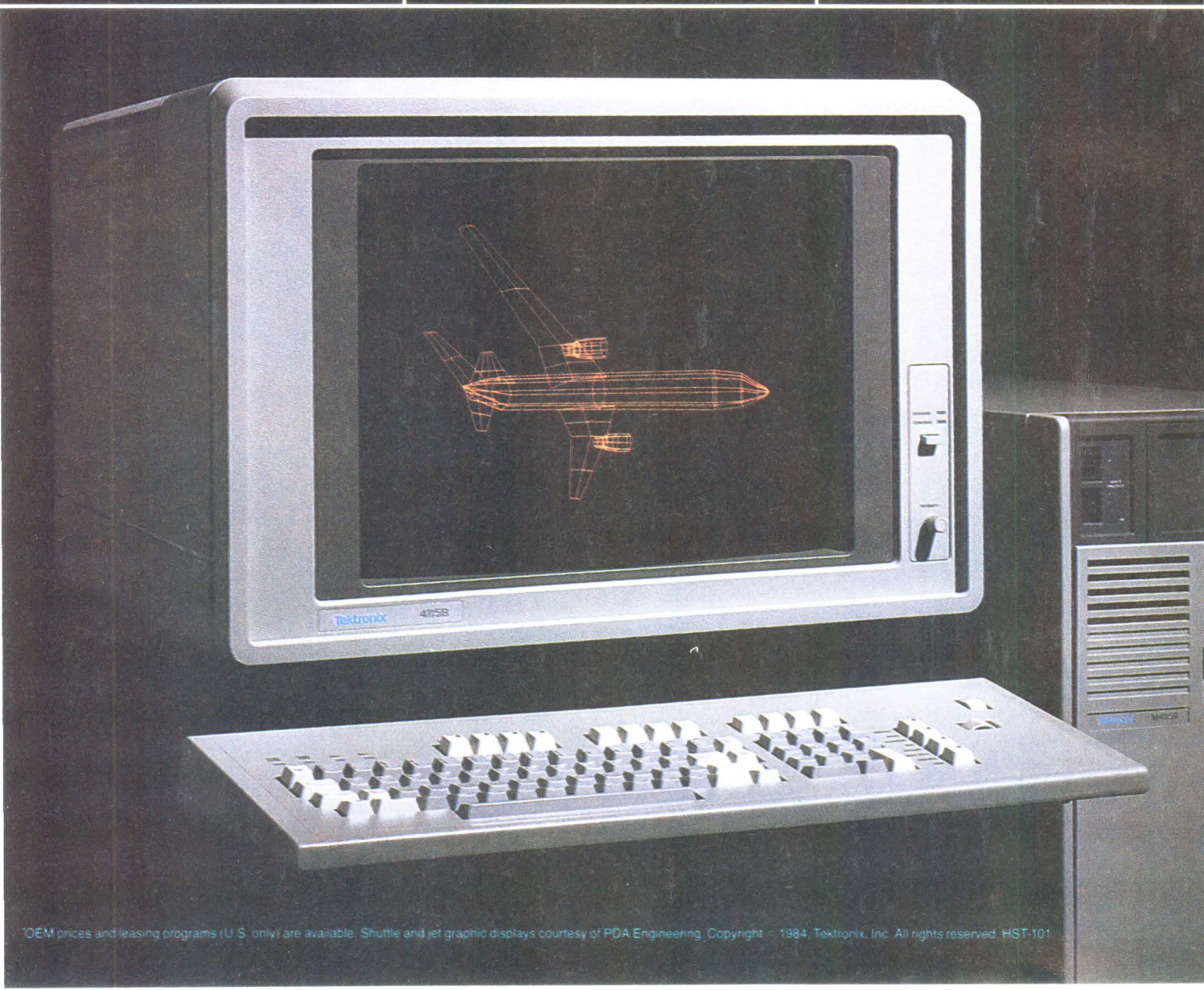

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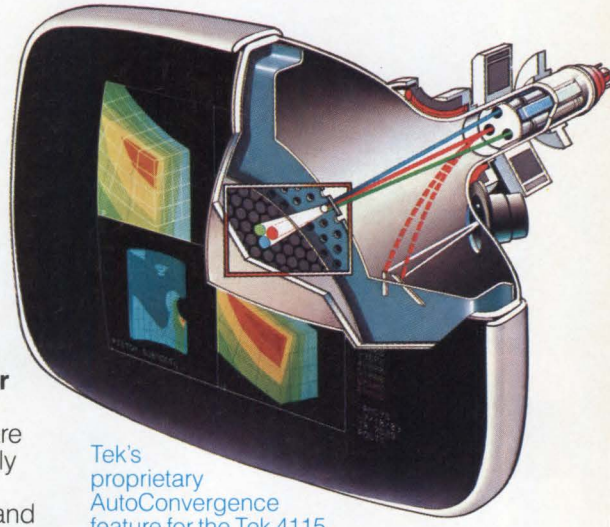

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CIRCLE 63

DATA FLOW CONCEPTS SPEED SIMULATION IN CAE SYSTEMS

By exploiting the similarities between a fifth-generation, data-driven system and the so-called discrete-event simulation algorithm, a hardware accelerator can boost simulation speed 100 times.

by William G. Paseman

Combining a standard interface computer aided engineering workstation and a high speed simulator greatly simplifies computer system design and verification. When a simulation engine is integrated in a complete CAE environment, designers can work with a CAE graphics interface, Boolean expressions, or a standard behavioral language. In any case, the system automatically loads the simulator with input data and retrieves results for display.

Until recently, engineers have not had ready access to high performance computational engines, which are needed to simulate large circuits at high speed during the design phase. To speed execution of an application as computationally intensive as the logic simulation of a large circuit, engineers have had to rely on general-purpose supercomputers or special-purpose attached processors. Unfortunately, the supercomputers needed to do this task are very expensive. On the other hand, special-purpose attached processors, while less costly than supercomputers, typically cannot perform interactive simulations needed by design engineers.

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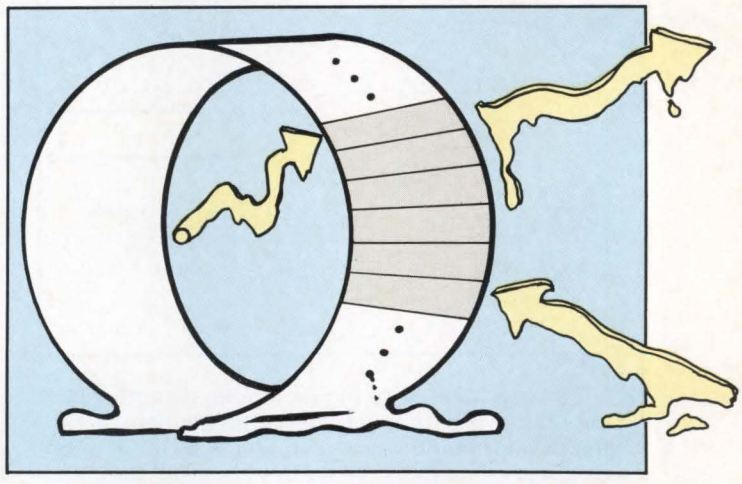


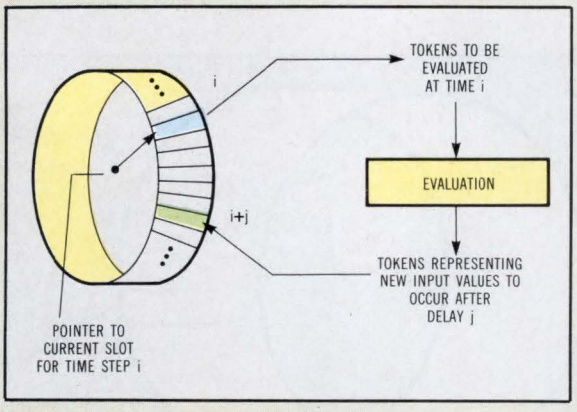
The availability of general-purpose microprocessors has spurred the development of high performance systems such as Daisy's Logician workstation. It can execute software simulation packages at a reasonable speed. However, when faced with the high capacity and high speed requirements of large circuit simulation, general-purpose devices leave little room for improvement. Even using such techniques as assembly language coding or dedicating a microprocessor to a particular aspect of the simulation activity cannot provide the required speed. At most, assembly language code triples execution speed.

To satisfy its goals, Daisy has selected a fifth-generation architecture using microcoded bit-slice

The discrete-event simulation algorithm

To deal with real-world events, a digital computer approximates the continuous flow of physical processes as a sequence of events occurring at discrete time steps. With a high resolution—a small elapsed time between steps—this discrete treatment of time faithfully represents physical processes, just as discrete waveform sampling at twice the highest frequency of an analog signal (the Nyquist criterion) faithfully represents an original analog signal.

Similarly, a logical simulator for digital circuits evaluates the inputs of circuit elements only at discrete time steps. Following a change of the input values, a simulator evaluates the circuit element, and schedules the appropriate values to appear on the outputs of a particular circuit element at a time corresponding to the circuit element's internal delay. Although simulators such as IBM's Logic Simulation Machine, Yorktown Simulation Engine, and Engineering Verification Engine evaluate every gate at each time step, other simulation engines evaluate a circuit element only at time steps when its input values actually change. Because only a small percentage of a large circuit's gates' changes ever occur on their inputs during a particular time step, this latter incremental method, called discrete-event simulation, cuts the number of evaluations needed at each time step.



To keep track of changing inputs, discrete-event simulators maintain a table, or time wheel, listing the new values that are to appear in a circuit at the different time steps. At each time step, the simulator increments a pointer to select the next slot in this time wheel. If it finds that a particular time slot is empty, it does not need to perform any evaluations, but simply increments its pointer to the next time slot.

On the other hand, when an input or set of inputs does change values at a particular time step, the simulator applies the new values to the associated circuit element. It also evaluates the circuit element's operation, and places the associated output value in the time wheel slot corresponding to the circuit element's internal delay. Consequently, as a discrete-event simulator cycles through its time wheel, it evaluates only those circuit elements for which it finds new input values at the current time slot.

processors that coordinate their individual specialized activities for high speed and capacity. Unlike circuits based on general-purpose microprocessors on one extreme, or special-purpose circuits hardwired with special functions on the other extreme, microprogrammable systems reach an optimum balance of flexibility and raw power. Furthermore, even though they can be developed using the most advanced technologies, these systems can also be developed from conventional parts. The final product results in a less expensive and more reliable system than one built from new or custom devices.

Simulation approaches

As in any type of simulation, the basic goal of logical circuit simulation is to describe circuit behavior in detail, based on the static and dynamic properties of the components. Thus, a logical circuit simulation produces a set of simulated waveforms. Such waveforms are produced by evaluating the effect of a set of simulated input waveforms on a circuit description. This circuit description comprises a combination of functional elements such as MOS gates, latches, and registers along with the description of their interconnection.

As part of its information about a circuit's functional elements, a simulator includes a description of transformations performed by each circuit element. Based on the input/output relationships between functional elements—as described by the netlist—the simulator applies inputs to nodes in the circuit. It also computes the corresponding output value and passes this output along to the next node. All digital circuit simulators evaluate the circuit elements in discrete time steps, which determine the resolution of a simulation. However, these simulators generally use two different approaches to perform evaluations: event-driven or clock-driven. Although the clock-driven approach, used in IBM's Logic Simulation Machine, provides very high speed simulations, it requires a large expensive machine to carry out gate-level evaluations at each simulation time step.

On the other hand, event-driven simulation requires evaluation of only those elements whose inputs change at a particular simulation time step. Statistics show that only about one percent of a circuit's gates are ever active at any particular simulation time step. Therefore, a simulator could improve in speed nearly a hundred-fold by evaluating only those gates whose inputs have actually changed during a particular time step.

Hardware accelerators often draw on special event processors to handle the functions associated with event-driven simulation. In this design, a pipeline within an event processor sets up event information, evaluates circuit elements, and schedules new events as needed. Rather than relying on high speed

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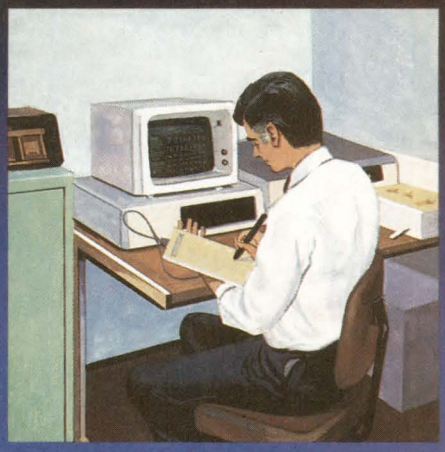

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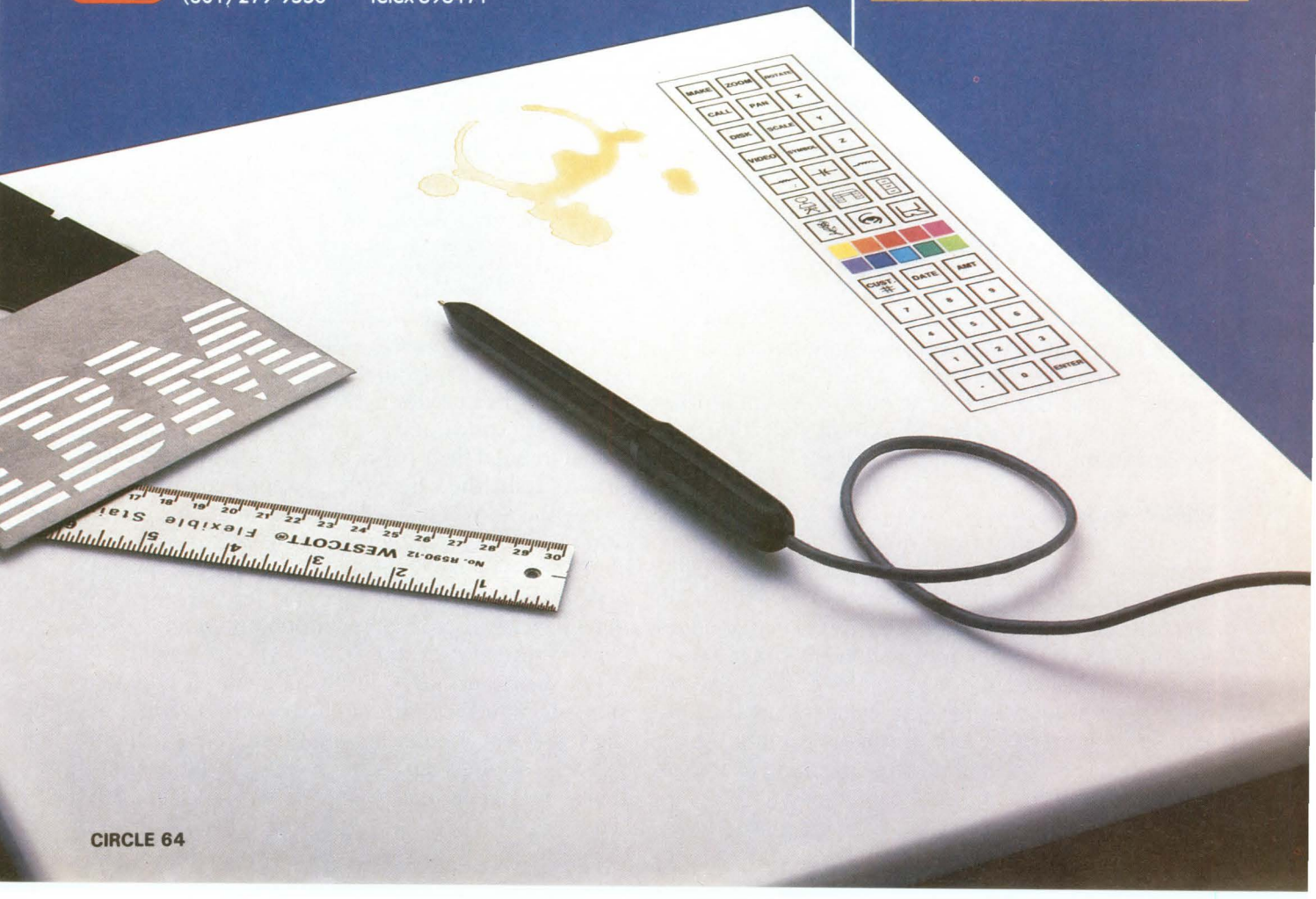


CIRCLE 64

What is data flow?

In a conventional von Neumann machine, the primary operation principle is the sequential execution of a series of instructions. In these machines, an instruction pointer selects the next instruction for execution by the CPU, then increments to the next instruction (or is adjusted by interrupts or instructions such as jump instructions or subroutine calls). Consequently, the control instructions of programs determine the operation of von Neumann machines.

A fifth-generation approach, such as a data flow architecture, replaces the control-driven operation with one where the data itself controls the operation sequence. In the data flow model, a network of processing elements performs the fundamental operations needed to complete a particular calculation. Unlike the explicit sequencing of instructions in the von Neumann model, operations occur only when all the data operands for the operation are available.

Typically, data flow programs, or graphs, explicitly draw out the concurrent operations in an algorithm as a set of arcs and nodes. The nodes in a data flow graph represent processing elements, while the arcs between processing elements carry tokens that contain actual data values. These tokens are typically represented on the arcs of a data flow graph as filled circles.

In the classical data flow model, as soon as tokens appear on all the arcs flowing into a node, the node fires—or performs its associated set of operations on the input. As a result of this evaluation, the input tokens disappear, while a new token appears on the output arc(s) flowing from a node. This output token contains the result of the node's evaluation. Because the classical model does not allow nodes to store information, a node cannot fire again (if all its input arcs contain tokens) until the output token is removed by some node downstream in the data flow graph.

An advantage of the data flow approach is its ability to exploit the parallel organization of some algorithms. In fact, the data flow graph explicitly lists operations that can occur concurrently on the same level of the data flow graph. Ideally, each node represents a processing element. Consequently, each operation at the same level in the data flow graph may execute independently and asynchronously with other processing elements. Thus, rather than being driven by a master system clock, a data flow machine is driven by the arrival of data at processing elements in the data flow network.

In implementing this theoretical model for a data flow architecture, a data flow system will typically have fewer processors than nodes in a particular graph. The task of translating this graph to a specific allocation scheme in a specific data flow system falls to compilers, loaders, and operating software. Standard compilers and loaders produce an image, which might be paged during run time by an operating system. In a data flow system, runtime operating software might simply use the static processor allocation determined by the compiler and loader, or it might allocate processors dynamically.

Although they both act to perform the sequence of actions specified in a data flow graph, static and dynamic data flow systems trade efficient use of processing elements for allocation complexity. In a static system, a data flow compiler simply assigns processing elements to perform tasks, beginning with the first level of operations in the data flow graph, and flowing down. This static approach does not use the processing elements efficiently.

In the architecture just discussed, processing elements downstream in the data flow sit idle until tokens arrive. To exploit the computational power of individual processing elements more efficiently, dynamic data flow systems assign processors on the fly to aid in processing the tokens upstream. A processor is assigned a number of different types of operations, depending on the complexity of the problem and other processing element availability.

Unlike von Neumann machines, where the instruction pointer and stack pointer provide all the contextual information needed to evaluate instructions and use operands, data flow systems require

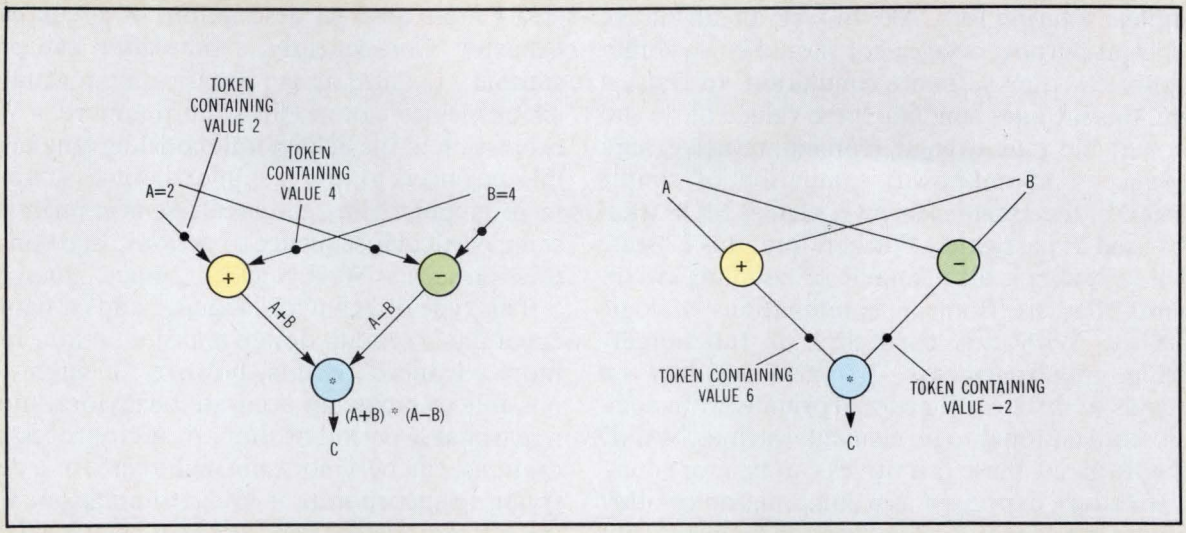
hardware to implement event-driven simulation, however, an alternate approach is used. Daisy's Megalogician simulation engine exploits the similarities between the discrete-event simulation algorithm and the operation of a data flow machine.

Similar workings

In the pure data flow model, a node begins processing only after all of its inputs appear. Thus, a simple data flow graph for $c = (a + b)*(a - b)$ would begin processing the sum and difference as soon as both operands a and b appear. On the other hand, a discrete-event simulator evaluates an element, or node, whenever any of its input values changes. Consequently, a discrete-event simulator could produce an identical result as a data flow machine provided that two conditions hold.

First, all inputs arrive at nodes simultaneously (to ensure that a node in a discrete-event simulator would not fire prematurely and produce undefined results). Second, delays through nodes can be adjusted to align their processed results (to satisfy condition 1). In the case of a balanced equation such as the one above, it would not be difficult to ensure that a and b arrived simultaneously, and that the sum and difference outputs reached the product node at the same time. In this case, a data flow machine and discrete-event simulator could produce similar results.

On the other hand, in an unbalanced equation, such as $c = ((a + a)*b) + 1$, a data flow model and discrete-event simulator would seem to perform differently. While a data flow system would wait until the results generated correctly down through the



tokens to carry their own contextual information as they pass between nodes. Data flow tokens are actually complex information packets that carry the instruction to be performed and the operands for the instruction.

As processing elements complete operations, they use these pointers to fill out packet templates. Only after all the operand slots in a template are filled is a completed template dispatched to an available processing element. Because of the asynchronous nature of data flow computations, templates can be filled out without regard to the overall context of a computation. Thus, if it is performing some iterative operation, a processing element could complete a packet needed for the (i + 1)st iteration, even though other processing elements are still completing operations for the ith iteration.

Consequently, dynamic data flow systems encode contextual information as a separate "tag" associated with values in a packet. Because of the need to create packets, to dispatch completed packets, and to perform operations encoded in the packet, the classical data flow architecture uses a ring of three separate units to perform these functions. Although the net effect is the same, the two versions of the data flow architecture fill out templates somewhat differently. In systems with token storage, an update unit fills out the template located in a common memory pool. After the template is completed, the update unit notifies the fetch unit, which retrieves the completed packet and dispatches it to the processing unit for execution. In contrast, in systems with token matching, a matching unit collects individual data tokens in its own local storage. After it has matched the tags of related data tokens, the matching unit passes a set of related tokens to the fetch-and-update unit. This unit combines the data with instructions, drawn from its own local memory, to create a complete packet. The fetch-and-update unit then dispatches the completed packet to the processing unit for execution.

In either case in this architecture, data flows in only one direction. Rather than using the instruction pointer of conventional von Neumann architectures, the data flow approach lets the demands of the data dictate the processing flow through the ring. No individual unit acts as the conventional CPU, but each unit continues performing its specialized functions until data tokens indicate that no further operations are required.

nodes, a discrete-event simulator would produce undefined results at the lower nodes when b and 1 were first applied to the inputs.

The discrete-event simulator could be adjusted to give the appropriate results by balancing out nodes having null operators—operators that simply transfer the input to the output after a specified delay. In this case, the delays of the null operators would be adjusted to match those of the addition, multiplication, and addition operators at the three nodes representing the unbalanced equation. With this design, results would propagate "evenly" down the data flow program to reach successive nodes simultaneously, producing the same result as the corresponding data flow machine. Even in more complex applications, provided that the initial input values are delivered simultaneously, the use of null nodes with delays results in a data flow program that will produce the same result in either a data flow or a discrete-event simulation model.

The similarity between a static data flow model and event-driven simulation extends to both basic algorithms and data structures. Logic operations of individual circuit elements serve as the instructions encoded in data flow packets, while logic levels function as the operands. Simulation time serves as the tag, and other circuit elements (specified in the netlist) become the destinations for evaluation results.

Well-knit environment

Although the data flow architecture closely matches the particular characteristics of event-driven circuit simulation, it is still only one tool in a larger development environment. Therefore, it must work

with the other tools in the environment to provide a complete solution for CAE. In fact, an advantage of a special-purpose accelerator should be its ability to support existing software simulation. In Daisy's system, this includes handling three-valued (0, 1, and unknown) and four-strength (forcing, resistive, high impedance, and unknown) simulation of simple gates and bidirectional elements, such as MOS transistors used as pass gates. Furthermore, this 12-state modeling system is also capable of handling circuit elements that are Boolean combinations of logic primitives. With this capability of functionally modeling circuit elements, designers can draw on thousands of different functional primitives. In addition to conventional logic elements such as NAND and NOR gates, these primitives can be more complex functions, expressed as a combination of other primitives in a higher level description language. For example, an exclusive OR (named XOR) with delay N would be modeled as

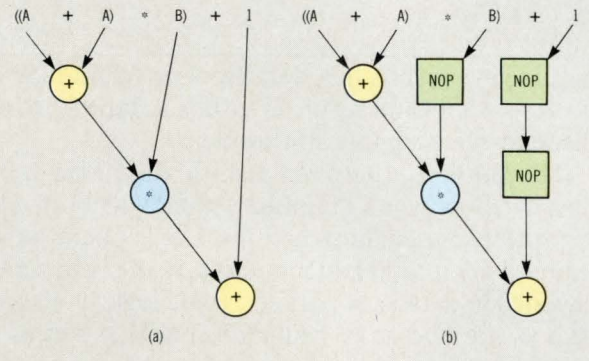
```
XOR:EXPR <outputs:o1[N]; inputs:i1,i2>;
{o1 = nand(nand(i1,not i2), nand(not i1,i2))};
```

where the delay for the entire operation is lumped into some single value N. This sequence of logical operations is described as a single expression. So, whenever a simulator scheduled this XOR function, the entire expression would be evaluated at once, rather than as a number of individual events. Similarly, this function could be defined as a circuit component and compiled into a simulation function set. But, this approach introduces individual event scheduling for the component logic elements.

In addition to this functional modeling, the system supports a higher level description language for behavioral modeling. Using standard structured expressions such as IF, and THEN/ELSE, designers can create more abstract descriptions of circuit element behavior. Consequently, a simulation can proceed without a detailed design specification for individual circuit elements or modules. Furthermore, a WHEN expression in the behavioral modeling language permits engineers to, for example, sensitize a circuit element's inputs. Thus, the circuit element might initiate some particular sequence of actions based on an expression such as WHEN (clock_input_goes_high).

This type of behavior language adds a significant capability to circuit design and simulation. In some more advanced circuits, however, it might not be possible to create an accurate behavioral model in a reasonable period of time. A microprocessor, for example, can be a modeling nightmare for a designer trying to incorporate it into a simulation. Even if the microprocessor vendor has a behavioral model, it might not be available—or even if it is available, there would be no guarantee that it would accurately reflect the final part.

Rather than produce a software model of a complex circuit such as a microprocessor, a simulator such as Daisy's can use the chip itself to physically model the interactions between the designer's circuit and the complex part. Rather than calling on a software subroutine that represents a device, the simulator uses the Physical Modeling Extension (PMX) as the equivalent of a hardware subroutine for the simulation. Besides these behavioral and physical models that serve early phases of the design cycle, engineers need other techniques to test designs as they near completion. One common series of tests determines how completely a physical device is checked. Because a limited series of tests might not check all gates, circuit designers typically create a set of test vectors, and analyze the efficacy of the vectors for toggling all or most of the gates.



A data flow system handles an unbalanced equation correctly (a); a discrete-event simulator evaluates nodes prematurely (b), unless the discrete-event solution introduced no operation (NOP) delays. These ensure that tokens reach the same tree level simultaneously.

Architecture selection

Fault simulation fills this role by testing how thoroughly a vector set tests circuit gates. Similar to normal (or "straight') logic simulation, fault simulation requires an evaluation of circuit elements based on a set of inputs. But, fault simulation adds a twist to straight logic simulation by purposely introducing a fault into a circuit. This is done to check a test vector set's ability to uncover the artificial fault. Thus, engineers can determine the fault coverage of a test vector set.

To fulfill these requirements and constraints, the Daisy simulation accelerator has to be a somewhat general-purpose device. Similarly, to keep the price down, the implementation has to rely on conventional technology in an architecture dedicated to the particular application. Yet, such implementation must be flexible enough to adapt to new applications and algorithms as design needs dictate.

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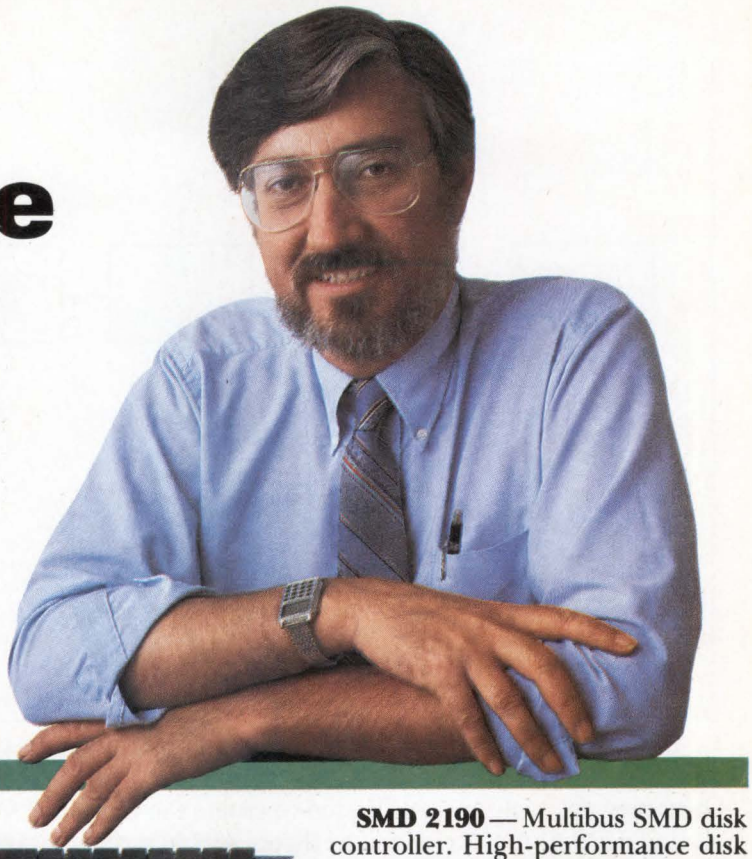

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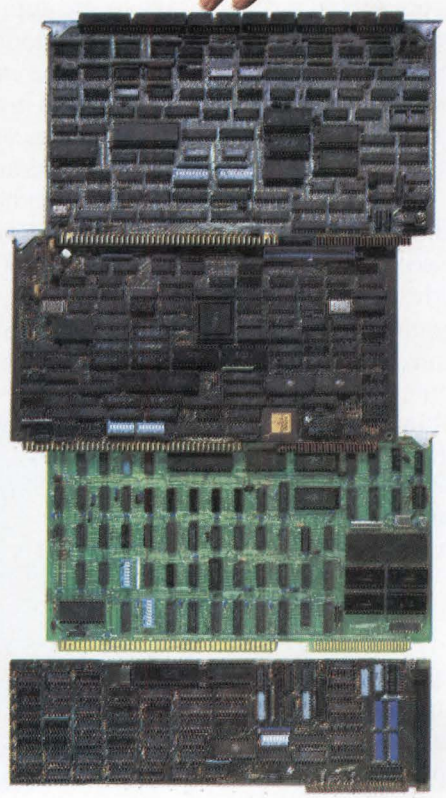

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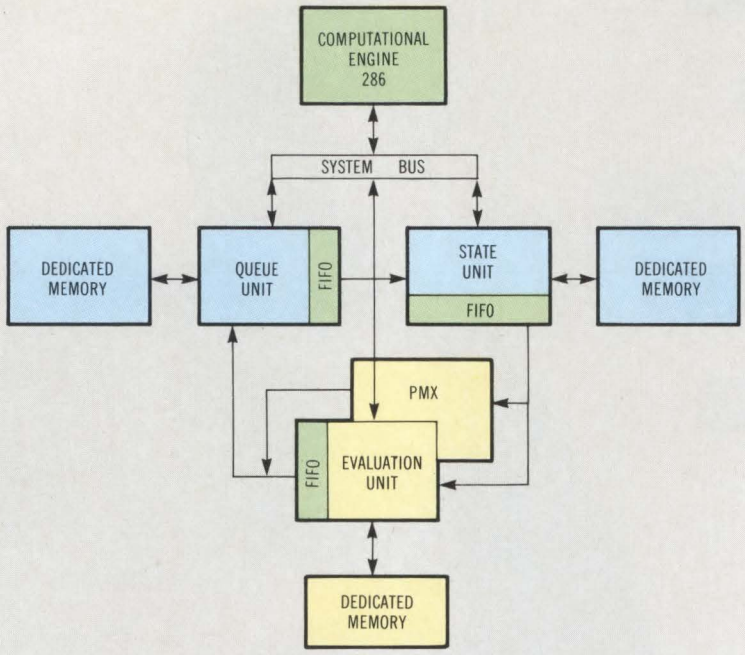


The simulation accelerator uses three units. After the state unit assembles packets, the execution (evaluation) unit evaluates them and passes results to the queue unit that processes data for the next event. A Physical Modeling Extension (PMX) allows direct chip simulation.

Because the static data flow model of computation strongly supports discrete-event simulation, this becomes the basic approach used to create the simulation accelerator. Arranged as three units in a ring, the simulation engine implements data flow packet communication with token matching. Each unit includes its own local memory and storage queue that serves a bit-slice processor. In turn, each unit's processor is specialized to its individual function through microcode.

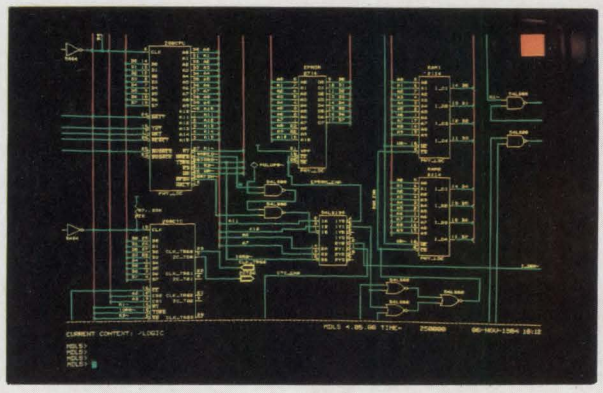
The execution (evaluation) unit devotes its processing to evaluating logic elements based on a particular set of input values, and producing the corresponding output values. For its part, the queue unit collects result data from the execution unit, schedules the data, and passes the scheduled events on to the state unit. This state unit, in turn, combines instructions (logic functions) with operands (input states) and places the complete packets in the execution unit's evaluation queue. During a simulation, information continues to cycle in this single direction until all evaluations are satisfied.

Simpler data flow with PMX

Besides this core of data flow processors, up to 5 PMX modules, each containing up to several dozen integrated circuits being used as simulation models, can attach as coprocessors to the primary execution unit. This unit mediates all transfers between the data flow ring and the PMX units. Because they coordinate their activity with the primary execution unit, the PMX units avoid reproducing costly communication hardware and maintain a simpler data flow design and communication model.

During a simulation, when an execution unit receives one of the extended operation codes for PMX service, the execution unit dispatchs a message to the appropriate PMX. Because the PMX can process its models independent of the primary execution unit, the execution unit is free to begin processing the next instruction in its queue even while the PMX unit is working on its instruction.

The accelerator coordinates its activities with the Megalogician host through connections with the system bus, and also ties in with the existing software system. Besides supporting existing software simulation functions and increasing the capacity of the simulation to one million gates, the accelerator executes 100 times faster than a software simulator. It



A hardware accelerator provides an extra measure of power to a CAE workstation without altering the user's perception of the development environment. Circuit designers create circuits for simulation with the Megalogician's graphics interface.

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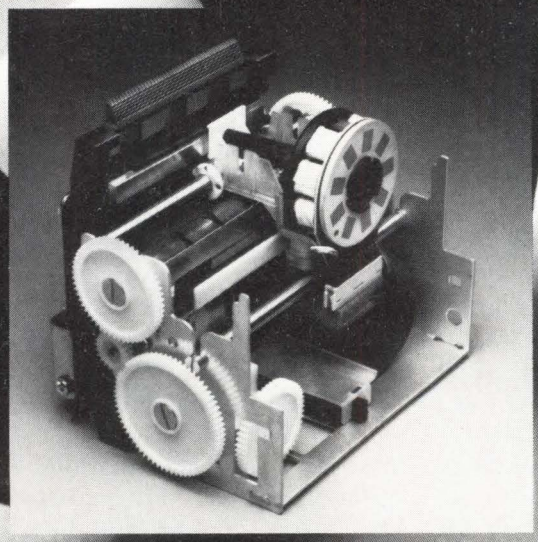

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does so without altering the existing user interface. In fact, other than the fact that the interactive simulator's Run command executes faster, users notice no other differences between the use of the accelerator and the Daisy software implementation.

In most advanced architectures, users must adapt to a programming paradigm that is unfamiliar and difficult to use. In contrast, coordination between the Megalogician host and the accelerator permits users to continue using more familiar design approaches—graphics waveforms, Boolean expressions, and a standard behavioral language.

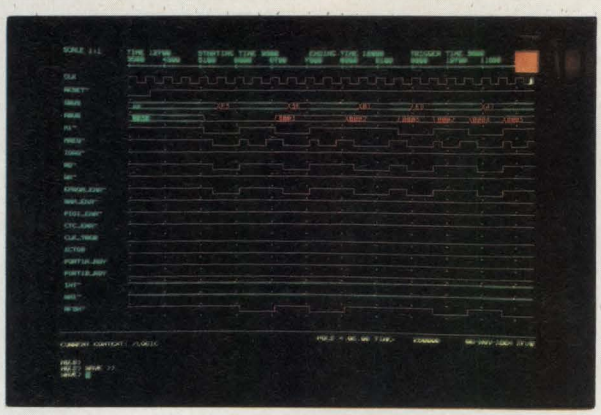
Designers can use the standard Daisy circuit design system to create circuit schematics. In turn, the Megalogician creates a netlist that is transformed into the specific information needed by the accelerator to simulate the circuit design. As the accelerator cycles through the simulation, it sends "snapshots" of its results back to the system, which can then draw the corresponding input and output waveforms for various simulated nodes in the circuit. Design engineers work in the same CAE environment, with the added performance boost of a hardware accelerator for simulation. Thus, they can quickly assess the significance of a design decision.

Parallel advantages

Unlike certain other attempts to apply data flow architectures, Daisy's application of data flow worked because it was applied to an appropriate application. However, because of its parallel structure, a data flow system can provide a significant boost in performance in its own right. For example, because the three units in the simulation accelerator balance the processing load evenly, the architecture itself accounts for a threefold performance increase over the previous Daisy system. On the other hand, the functional specialization afforded by the microcoded architecture, which permits each unit to be tuned to the particulars of its own individual task, accounts for a 33-times performance increase over the Daisy software package. The product of these factors results in the overall hundred-fold increase.

Functional specialization plays a dual role in advanced systems such as this. On one hand, the processors can be tailored to fit the general characteristics of their application. In event simulation, for example, processors deal with many different token types and must emulate a wide variety of instructions and logical functions. Because a processor in this system is constantly switching between the different token packets, the overhead for a context switch must be low. In fact, these processors are optimized to ensure that the overhead for context switch is negligible.

The second role of functional specialization—when it is implemented as microcoded processors—permits the data flow system to adapt to other applications that can be solved by the data flow model. Both



Simulation engine operation produces simulated waveform tracings as just a software simulation package. During a simulation, the accelerator transmits simulation "snapshots" back to the Megalogician for display.

serial and concurrent fault simulation, for example, are modified forms of normal (true) simulation. By adding a mechanism for introducing the single faults of serial fault simulation—and multiple simultaneous faults of concurrent fault simulation—the same architecture can handle this important aspect of circuit design. Similarly, with additional logic values for rising, falling, and changing waveforms, an architecture that can support simulation can also handle circuit timing verification chores.

Beyond circuit design applications, an architecture such as that used in Daisy's hardware accelerator, opens doors to high performance implementations of specific processors for Lisp and Prolog—programming languages popularly used in artificial intelligence applications. Lisp performs best in the kind of environment where indirection and type checking account for little overhead and a set of functionally specialized processors can be easily tuned to perform these operations efficiently.

On the other hand, efforts to create parallel versions of Prolog have been based on data-driven architectures. Such a parallel Prolog can schedule instantiations of a variable-based rule to be evaluated by a processing unit in a data flow system. In this case, a template might contain a copy of the expression itself (in the instruction slot), along with the variables bound to the expression (in the operand slot). In turn, the processing unit could return (in the results slot of the template) the values bound to the variables for successful instantiations of the clause.

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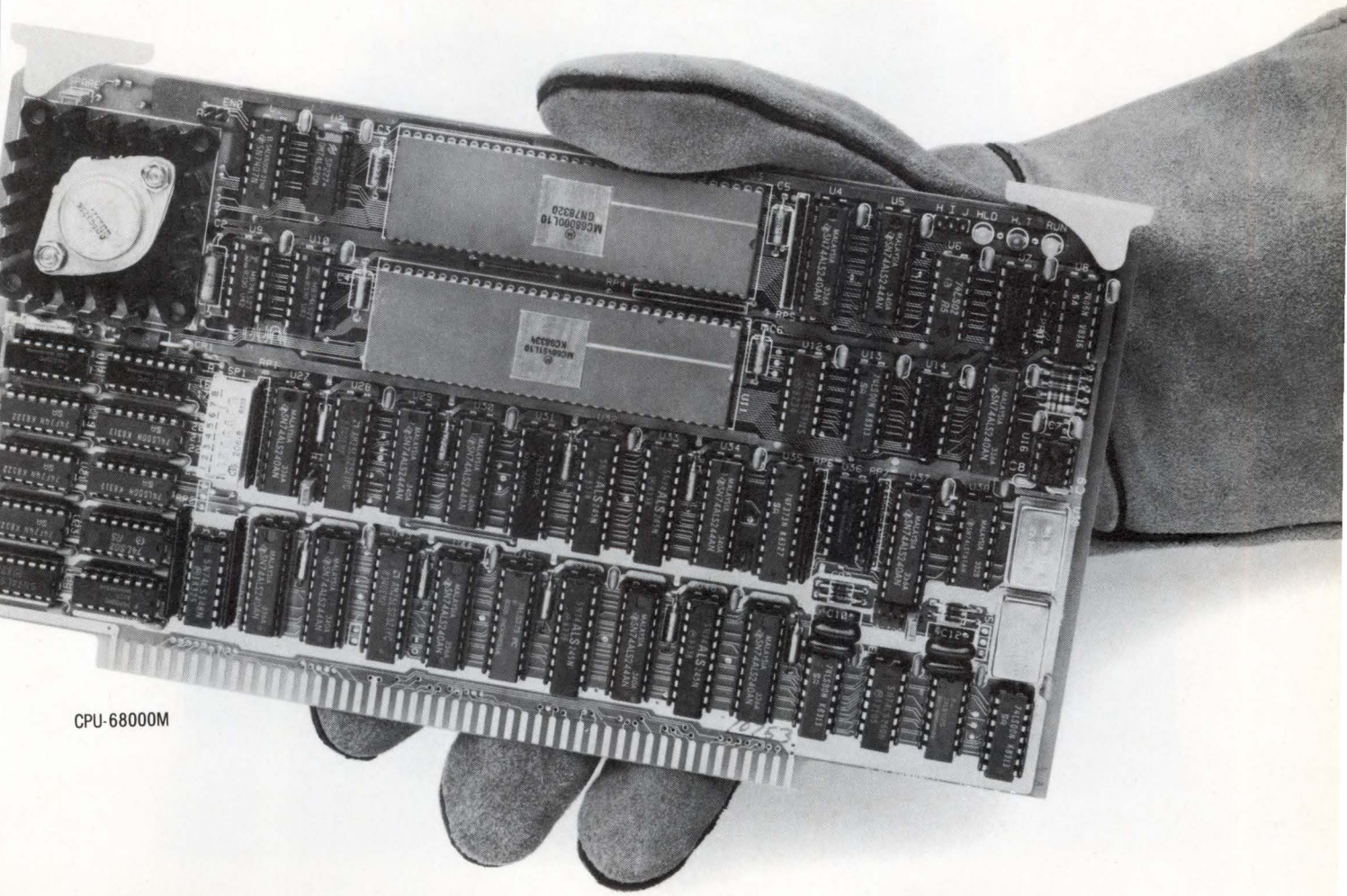

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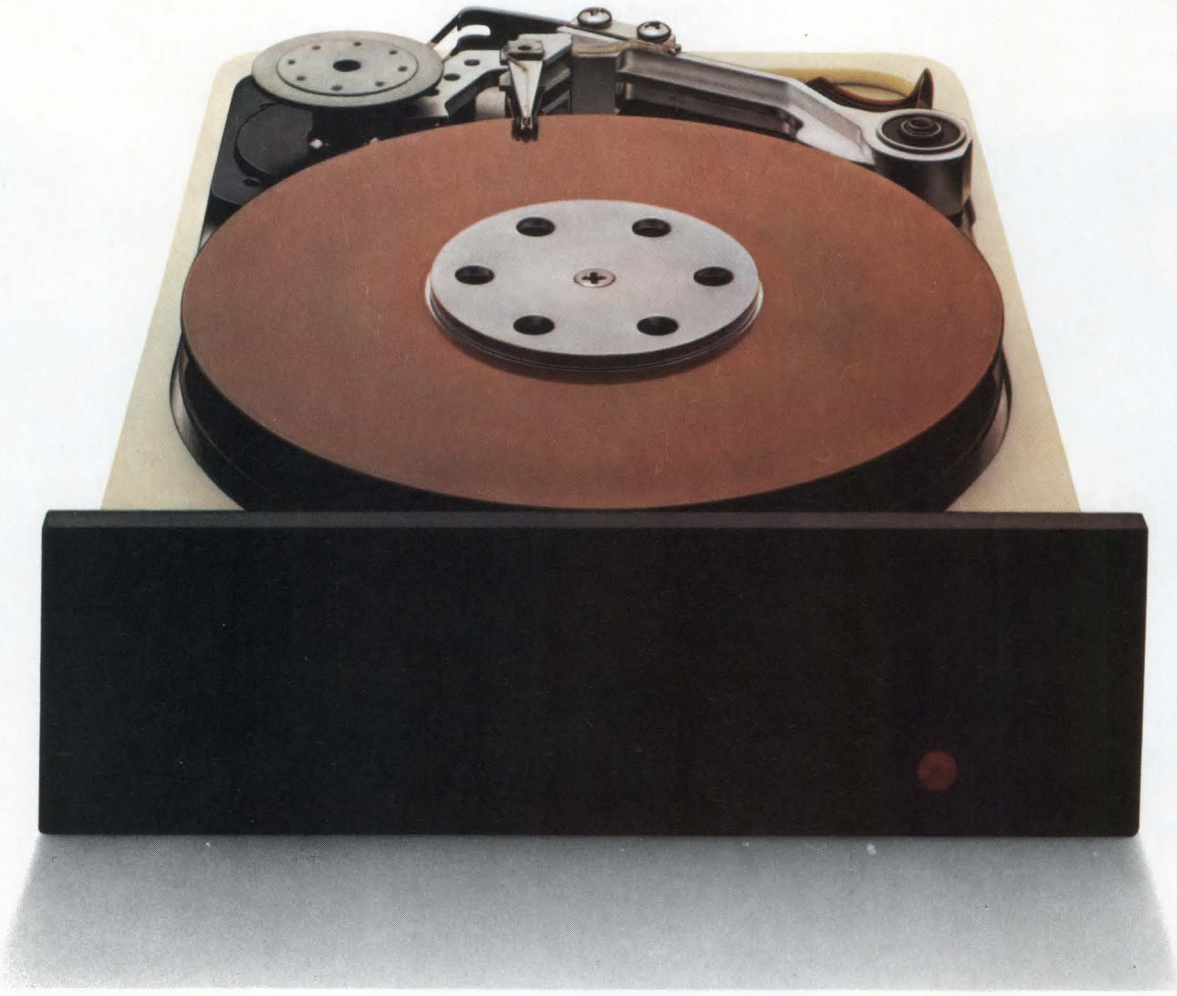

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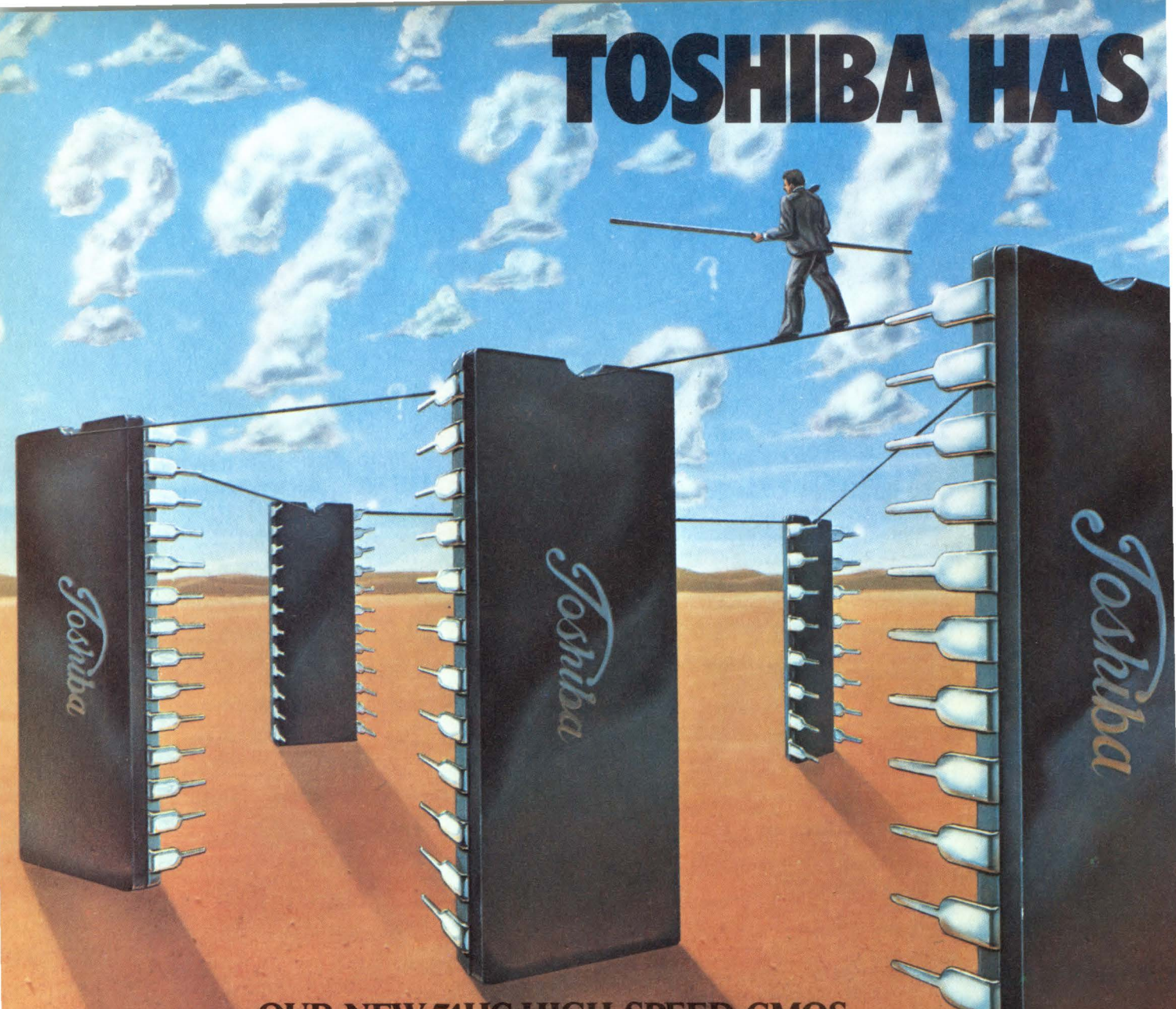

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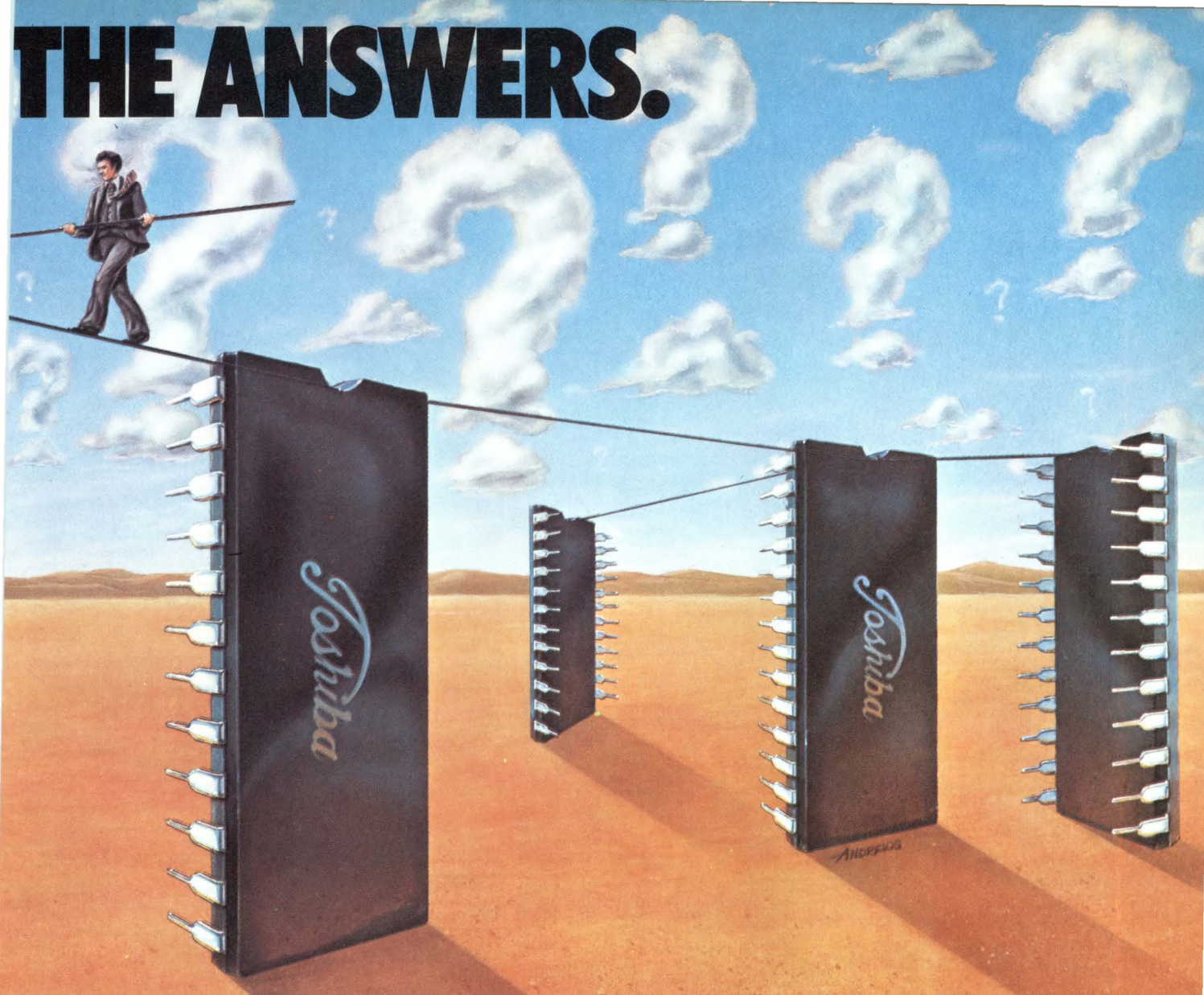

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Noise Margin V_{IH} (min)/V_{IL} (max)	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current $\|I_{OH}\|$ (min)/I_{OL} (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	4.75-5.25V	2-8V	3-18V
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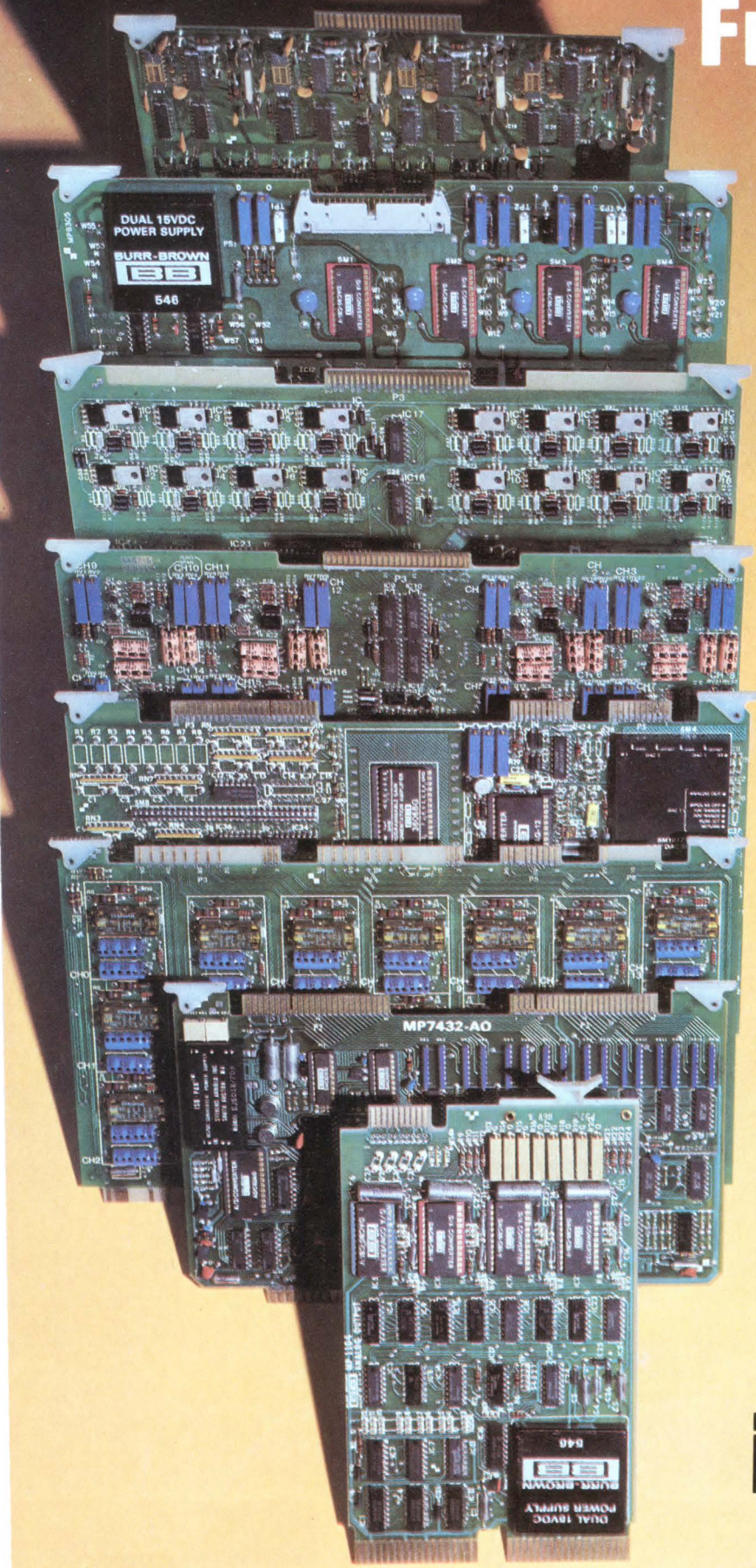

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SYMBOLIC PROCESSOR AIDS DESIGN OF COMPLEX CHIPS

A workstation offering object oriented programming is used to develop a mouse chip that is testable, reproducible, and fully functional at first silicon.

by Eric Nestler

Object oriented programming in a Lisp environment has gained attention with its promise to solve design problems by allowing rapid prototyping in an exploratory software environment. One way to use the power of this system is in designing complex chips. The interactive Lisp environment allows the computer design engineer to extend and integrate software for many complex schemes. Lisp offers greater design efficiency than possible with conventional programming languages and workstations. More importantly, designing chips within a Lisp symbolic processing environment is an example of expanding the applications of Lisp workstations beyond artificial intelligence activities. In fact, Lisp may offer advantages over traditional chip design techniques for semicustom products.

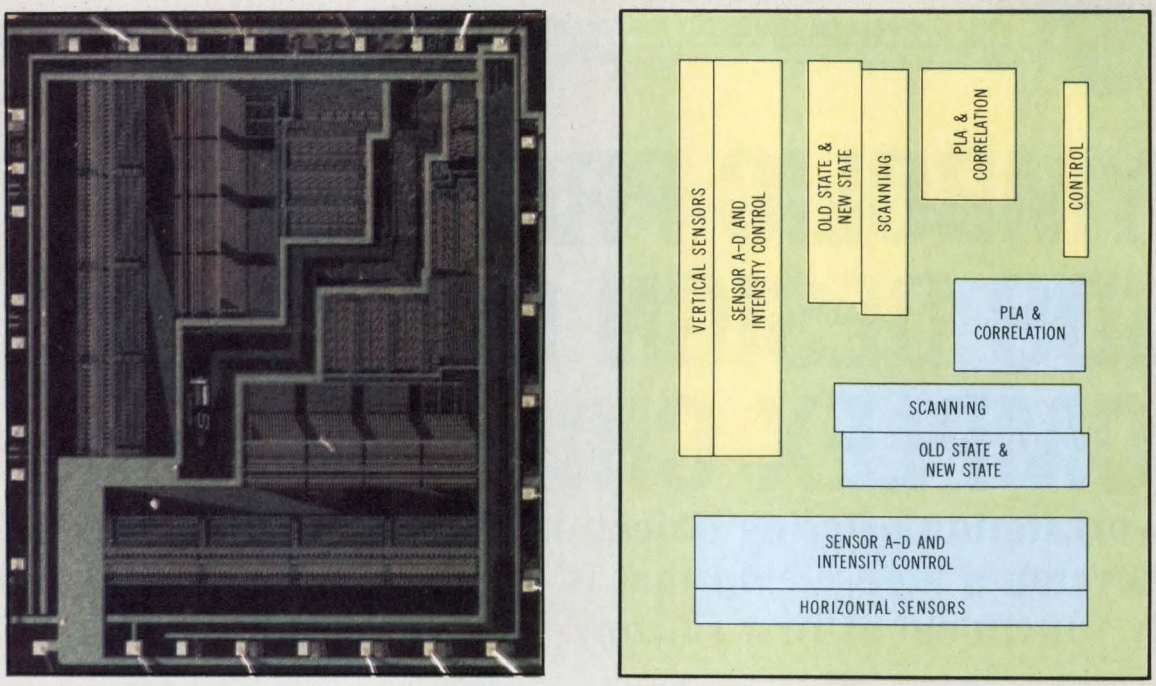
Designing a chip with a symbolic processor is still a complex effort. As in the normal custom IC design cycle, the designer determines and implements chip logic specification, design, and layout. However, in addition, specific Lisp based software is written and workstation-resident tools for design, simulation, layout, verification, design rule check (DRC), electronic rule check (ERC), and extraction are used in the design of custom VLSI chips. The total design project for the chip described here took a team of three engineers approximately 12 man-months.

Symbolics has completed an IC chip design that proves the many benefits of a Lisp environment with object oriented programming in a high end workstation, such as the Symbolics 3670. The testable, reproducible chip was 100 percent functional on the first fabrication run. The first product to use this chip is an optical mouse. The chip and an optical path team up to focus an image on the chip die and perform motion detection. Without this chip, mice require either mechanical or optical sensors supported by peripheral parts and chips.

Eric Nestler is a senior member of the technical staff at Symbolics, Inc (Cambridge, Mass). He holds an MS in electrical engineering from the University of Wisconsin, Madison.

Design tools

Circuit design and implementation are only half of the design task—choosing the best computer aided design/computer aided engineering (CAD/CAE) tools for implementation is equally important. The proprietary CAD/CAE Lisp based tools used for the latter tasks include extensions of previously implemented tools and a set of newly implemented tools. Before these tools can be designed, however, the method for transforming a chip's functional specification into an IC layout must be determined.



The optical mouse chip is a 12,000 device chip in 4 micron NMOS process technology. The chip is designed in a symbolic processing Lisp environment on a Symbolics 3670 workstation. Functional from first silicon, the chip will be incorporated in a production mouse.

A functional specification can be transformed in many ways. The degree of implementation ease is a trade-off for speed and component density performance. Understanding these trade-offs helps explain how and why symbolic processing can be a preferred design approach. For example, while gate arrays provide a rapid system-level design, they present certain size and speed limitations. On the other hand, full custom layout obtains the highest performance at the expense of the design complexity.

Circuit forms, such as programmable logic array based designs or strip-line designs, attempt to take advantage of replication as much as possible and reduce the time penalty of a full custom effort. Silicon compilers take these circuit forms a step further and specify special macrocells that can be assembled as large system building blocks. Modules such as RAM, ROM, ALUs, and PLAs are often found in these systems.

All cell based systems, including existing silicon compilers, suffer from a common set of problems. To establish a cell library, fixed timing disciplines must be used and technology changes (both process and circuit) are slow to be incorporated. In short, the fixed cell and module set limits the designer's imagination.

Other design methods have their problems as well. Fabrication processes may provide the speed for more restrictive layout design techniques. CPU clock cycle times, however, are not stagnant. For example, below 50 ns, 32-bit microprocessors will appear on the market as a result of designers pushing chip fabrication processes to their limits. The power of symbolic processing is perhaps a more flexible alternative.

Rather than restricting the circuit to particular forms (beyond what falls naturally out of the needed degree of function), symbolic processing can postulate a more intelligent class of tools in lieu of more complex modules. The features of these tools should ideally address the two time consuming activities of chip layout—global wiring and composition. In particular, changes at the end of the assembly of the layout can be most painful. And, changing the bounding box of a low level leaf cell may cause changes at all levels of the layout hierarchy. Global wiring is especially difficult when interconnection stretches over thousands of microns with many branches; and the wiring must be done with conventional interactive graphics.

Design tasks

Although Lisp based tools were used in the chip design, certain traditional design principles remain. The layout strategy remains hierarchical in nature with small cells combined into larger functional blocks. As much as possible, wiring between functional blocks is done by abutment. As layout cells are placed next to each other, the layout rectangles, representing wires, stop at the boundary of one cell and continue into the next. Unfortunately, this efficient technique is not possible for all chip

circuit interconnects. For example, generally, at the final top assembly of the major functional blocks explicit wiring is done between the I/O pads and the block edges.

Lisp based tools address two needs. First, physical placement of leaf cells is done in a relative sense. This means that, most often, the layout designer wants to place two cells next to each other. For example, the bottom-left of cell B should always touch the top-right of cell A. If the top boundary of cell A should extend upward, then cell B should move upward also so that no overlap occurs. If cells A and B were placed by specifying absolute coordinate positions, then overlap would occur. Clearly then, part of the design process is to write a Lisp program to assemble the low level cells into larger cells. Then they can be combined into large functional blocks at the designer's convenience.

Lisp programs also meet procedural method requirements for global wiring specification. When wiring must be done from one side of the chip layout to the other, a graphical editor, requiring explicit rectangles for wiring, forces the designer/operator to scan large areas of the layout at large scale factors on the display screen. This is not only inconvenient, but also is often not practical for real design.

With this technique, the operator view of the layout is very limited. As a result, planning is very difficult unless there is a current plot at a large scale to constantly refer to. In fact, the area for the wire may already have been dedicated by the floor plan of the layout in the form of bus widths and wiring channels. If so, then global wiring can refer to the already allocated wiring channels as a layout object.

Making the connection

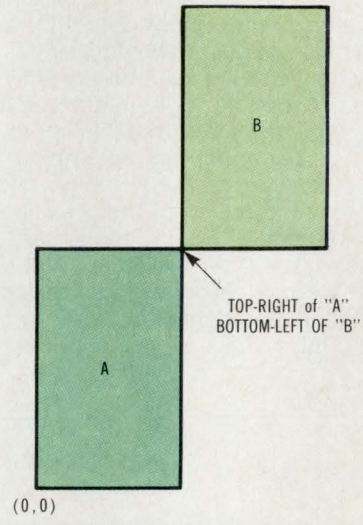
The symbolic processing chip design approach of Symbolics implements wiring procedures which can wire through one of the allocated channels and place layout rectangles automatically. The procedural wiring is specified between connection points on cell edges and the wiring channel is used as needed. These connection points are labeled during the chip's cell layout.

During global wiring, the connection points are referred to by name, rather than by location. If the lower level cell is altered by moving the labeled connection point, the global wiring will connect to the new location. Global wiring mazes are difficult to avoid except by expanding the area used.

Current automatic routers work well for constrained routine problems such as those found in gate arrays. In a custom layout, the routing style may vary considerably depending on the design. While a library of general routers may be constructed, it is often more straightforward to implement the specific routing in terms of symbolically specified software.

Another advantage of the symbolic method is the simultaneous initiation of top-down and bottom-up design activities. In addition, floor planning the die from the top-down does not create conflicts with bottom-up design, simulation, and layout of difficult leaf cells. While ideally chip design should be a top-down effort, it is more realistically a set of top-down proposals followed by bottom-up reality checks. The symbolically specified design tools allow a designer to jump from an abstract top view to a detailed bottom aspect with ease.

To help ensure design success, simulation of the circuit function was done at two levels. The first technique was behavioral simulation by a Lisp program. The second was by means of a timing simulator using a network extracted from the full layout.



(a)

```
TOP-RIGHT OF "A"
BOTTOM-LEFT OF "B"
;;
;; Place rectangle named "A"   with bottom-left at location 0,0
;;
(part 'A RECTANGLE
      (bottom-left (pt 0 0))
      (layer 'diff) (width 5) (length 10))

;;
;; Place rectangle named "B" with bottom-left at the same spot
;;  as the top-right of rectangle "A".
;;
(part 'B RECTANGLE
      (bottom-left (>> top-right A))
      (layer 'diff) (width 5) (length 10))
```

(b)

Physical placement of the optical mouse chip's leaf cells is done in a relative sense. Typically, the chip layout designer must place two cells next to each other (a). There are many ways to accomplish this feat; one procedural method is shown in (b).

Chip overview

An NMOS device, the mouse chip is implemented in practical 4 micron technology on a die 220 x 235 mils. The 12,000 transistors operate on one 5-V supply and consume but 250 mW. Since there is an onboard oscillator and clock driver, chip operation requires only an external crystal and a 5-V power supply. The horizontal and vertical sections of the chip block diagram are similar. In operation, an image is focused on the die surface. The two linear arrays of 64 sensors each detect motion along the X and Y axis on the die. The linear array for each axis is further subdivided into four groups of 16 sensors each.

Subgroups are established so that data processing occurs in parallel and independently for each subgroup. This redundancy is necessary to avoid chip malfunction if dirt or dust blocks the image to a sensor. In fact, only one subgroup of sensors is necessary for movement detection by the chip.

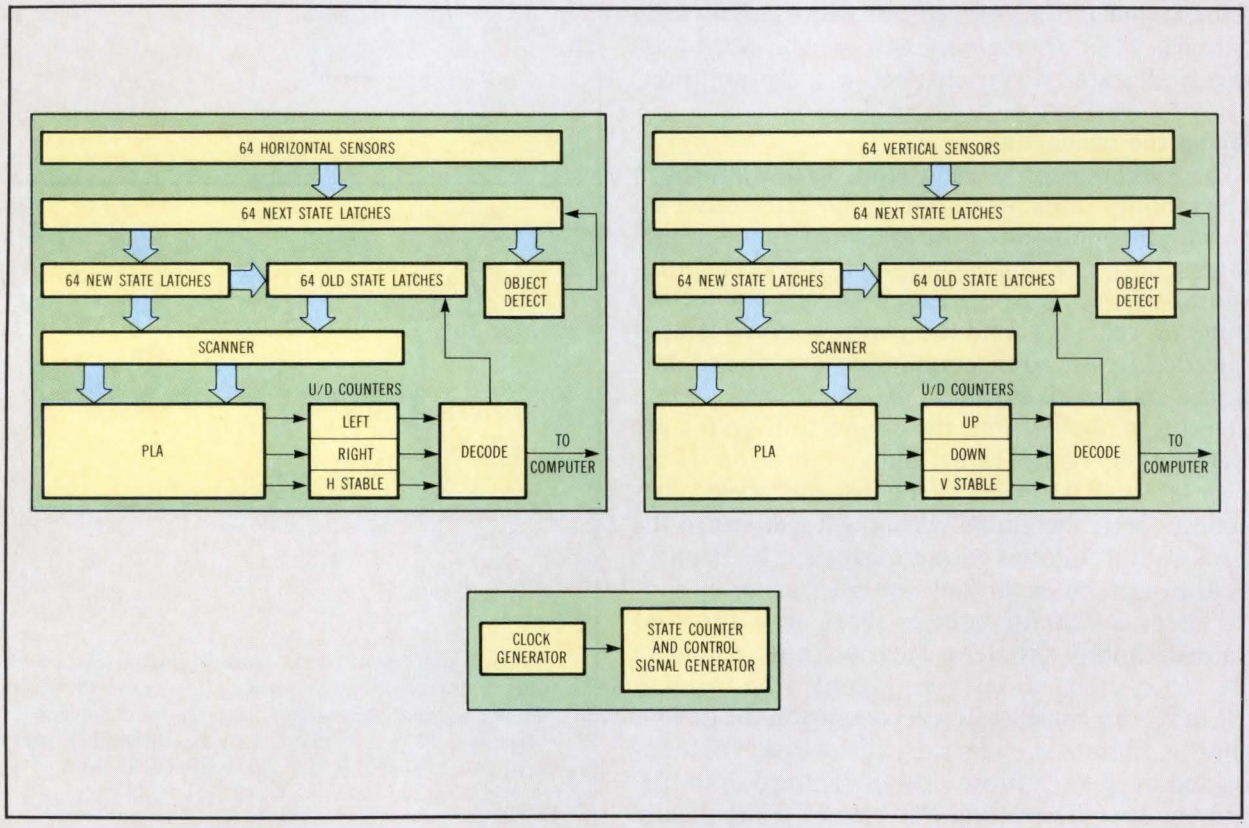
During chip operation, the derived analog sensor voltage is converted to a digital signal by a Schmidt trigger sampled at the chip's internal clock rate. The sampling logic that performs this chore also incorporates logic to continuously change the light sensitivity of the sensor. This design allows a one hundred to one variation of the peak light intensity of the image while still allowing the use of preferred synchronous logic for testability and reliability.

Image movement is detected by performing a correlation calculation between the current or present sampled digital image vector (64 binary states of the sensors in each axis), and an old image saved in a register array. The old image is from a previous state which need not necessarily be the preceding state. The old image register array is updated only when movement is detected during the current major cycle.

The correlation is accomplished by scanning the present image state and the old image state. A programmed logic array compares the present and old state images. The logic contents of this PLA predefine state transitions as up (right) or down (left) movement.

The PLA output is integrated by counters, predefining ups (rights) or downs (lefts) indicates movement in the respective direction. This correlation technique offers several advantages. For one, the PLA can be designed to detect selected image state transitions. The result is the reduction of the effect of single sensor image noise between the present and old image states. The chip outputs a two-bit, grey-coded value for each direction of motion. The output state of either axis changes only when motion in the axis is detected.

During the test of the chip wafers, object "images" can be digitally shifted into the internal register arrays. This eliminates the need for the test fixture to project any optical images onto the die. Furthermore, during test, internal counters can be read during any clock cycle via data and control buses brought out to the chip pads. This design shortens the test paths for certain states.



The outputs of the two simulations were compared by other Lisp forms to verify functional capability. Finally, the entire circuit was simulated to guarantee logic correctness and additional Lisp software performed DRC and static electrical checks.

Lisp environment

The Symbolics 3670 workstation used for the mouse chip design application has a 400-Mbyte hard disk—half of this capability is devoted to virtual memory with the memory management system. For this chip, the final layout data base occupies less than one percent of this space for all 12,000 chip transistors and devices. This small percentage leaves the entire chip layout available as input for any other Lisp program to operate on. In particular, simulators, extractors, DRC, and ERC can run on the same data base without the need for any disk file intermediate forms.

The object based nature of Lisp allows VLSI chips to be handled from program to program with a single pointer.

The single symbolic data base can be traversed by database walkers. A walker is a function that finds all bottom level leaf cells (like a DRC), or a function that finds all connection points on the perimeter of each bottom level cell (like a function wiring to connection points). A single common data base and the functional ease of extending Lisp programs require little or no database management programming for each new design task. In addition, the definition of the layout data base need not anticipate all the tasks to be performed. Experience shows that in applications such as the mouse chip design, database management is typically the majority of the software. Once this hurdle is overcome, adding functional capability is easy. In the 3670 environment, all systems are also written in Lisp. Access to such Lisp routines provides one more path of common software functional capability to build future applications on.

The optical mouse chip typically keeps the timing simulator, Spice output plots, ERC, and DRC outputs active, and a graphical editor with the full layout loaded simultaneously. Each of these activities is accessible with a single key stroke. Extensions to layouts that are at least an order of magnitude larger are possible with no software changes.

Lisp has advantages in symbolic processing, particularly in applications like the design of complex IC chips. Lisp, unlike other languages, permits the manipulation of complex data structures and symbolic information without the large overhead of memory management and data typing beforehand. Conventional languages frequently resort to textual intermediate forms to convey the output of one program to the input of another. This slows programmer productivity and makes such software unwieldy. The object based nature of Lisp allows objects as large as VLSI chips to be handled from program to program with a single pointer.

Lisp's ability to manipulate symbols makes it ideal for many subcategories of artificial intelligence (eg, expert systems and vision systems). Its major drawbacks are its large size and flexibility that can swamp even a mainframe. This flaw is more the result of the capacity limitations of a computer's conventional von Neumann architecture than any shortcoming of the Lisp language itself.

Complex knowledge and data are described in Lisp by physical or abstract symbols in natural language (words and numbers) with attached lists of properties to describe them. The properties consist of a variety of data types such as text, numbers, and other lists of properties. These form an itemized list attached to each symbol.

Any property attached to a symbol can have other properties associated with it describing how some function should use or process it. These are inherited properties. This approach is different from most other computer languages where variables have only one numerical value and it is up to a subroutine to know how to interpret the value. In this case, there are no inherited properties.

Dynamic processing

The closest analogue to symbols is records in a data base. But, normal database records are full of fixed length fields that are difficult to manipulate. Fields are totally arbitrary in terms of data type, length, and order, with no fixed structure among their symbols. Symbols in a Lisp based symbolic processing environment take the database concept many steps further.

Simply put, symbols are defined by lists of properties that can be dynamically processed—unlike those in a normal data base. They can be broken apart or combined to form new symbols, at run time, without knowing, at compile time, all the possible symbol values. These properties can, of course, be other symbols and properties.

What is more, because the symbols are processed dynamically at run time, there are certain memory allocation/deallocation problems in conventional programming languages that do not occur in symbolic processing. For example, most computer languages define variable and fixed arrays, and allocate memory space for them at compile time. If the computer needs more memory space during execution and the space is unavailable, the program will abort.

Code does the job

Several features of symbolic processing are well illustrated by examples of the Lisp code that applies. The text format of a simple cell—in this case, an NMOS NOR gate (a)—is based on DPL, a Lisp-like language for procedurally specifying IC layouts (J. Batali, N. Mayle, H. Shrobe, G. Sussman, and D. Weise; *The DPL/Daedalus Design Environment*, VLSI 81, Edinburgh, Scotland, 1981, pp 183-192). This text form is used for generating the symbolic data base. It becomes part of a library of text files for the layout—somewhat similar to what is normally developed for IC layouts using conventional CAD/CAE.

The NOR PROTOTYPE (b) is a printed representation of the internal symbolic data base. This symbolic data is a hierarchy of lists. For example, at some level, a component list might represent all of the rectangles of a particular leaf cell. Other lists might be all children of some higher level cell, or all parents of some leaf cell. SMASH (c) shows the code for a recursive walker that collects all of the rectangles of some top level cell regardless of that cell's hierarchy.

NOR (a)

```
(deflayout nor-1 nil
  (part nil diff-contact
      (bottom-left (pt 11.5 48.)))
  (part nil inlinepull
      (bottom-left (pt 8. 21.)))
  (part nil rectangle (layer 'diff)
      (bottom-left (pt 11. 18.))
      (length 3.0)
      (width 10.0))
  (part nil pulldown-1
      (width 10.)
      (bottom-left (pt 8. 10.)))
  (part nil diff-contact
      (bottom-left (pt 11. 0.)))
  (part nil pulldown-1
      (width 10.)
      (bottom-left (pt 28. 10.)))
  (part nil rectangle (layer 'diff)
      (bottom-left (pt 14. 18.))
      (length 6.)
      (width 27.))
  (part nil rectangle (layer 'diff)
      (bottom-left (pt 21. 0.))
      (length 10.)
      (width 20.)))
```

NOR PROTOTYPE (b)

```
#<PROTOTYPE 127605326> is a PROTOTYPE
   TYPE:                #<TYPE 127543350>
   PARAMETERS:          NIL
   PARTS:               (*LIST* (INSTANCE (VC (*RECTANGLE*DIFF 10 20 NIL) #<PROTOTYPE 12760532
6> NIL)
                                          (IDENTITY 31 . 5) NIL)
                                (INSTANCE (VC (*RECTANGLE* DIFF 6 27 NIL) #<PROTOTYPE 127605326
> NIL)
                                          (IDENTITY 27.5 . 21) NIL)
                                (INSTANCE (VC #<PROTOTYPE 127550027> #<PROTOTYPE 127605326> NIL
)
                                          (IDENTITY 36 . 14) NIL)
                                (INSTANCE (VC #<PROTOTYPE 127547717> #<PROTOTYPE 127605326> NIL
)
                                          (IDENTITY 16 . 5) NIL)
                                (INSTANCE (VC #<PROTOTYPE 127550027> #<PROTOTYPE 127605326> NIL
)
                                          (IDENTITY 16 . 14) NIL)
                                (INSTANCE (VC (*RECTANGLE* DIFF 3.0 10.0 NIL) #<PROTOTYPE 12760
5362> NIL)
                                          (IDENTITY 16.0 . 19.5) NIL)
                                (INSTANCE (VC #<PROTOTYPE 127550334> #<PROTOTYPE 127605326> NIL
)
                                          (IDENTITY 14 . 34) NIL)
                                (INSTANCE (VC #<PROTOTYPE 127547717> #<PROTOTYPE 127605326> NIL
)
                                          (Identity 16.5 . 53( NIL))
   INSTANCES:           (*LIST* (INSTANCE (VC #<PROTOTYPE 127605326> #<BUFFER 126524445> NIL) (
IDENTITY 0 . 0) NIL))
   BOUNDING-BOX:        (*BOX* BOUNDARY (8 . 0) (44 . 58))
   UNIQUE?:             NIL
   DISPLAY-CACHES:      NIL
   NODIFIED?:           NIL
   BINDINGS:            NIL
   IVE-BEEN-MODIFIED:   0
   IM-A-REPLICATION:    0
   IM-A-WIRE:           0
   IM-A-GROUP:          0
   IM-NOT-DISPLAYED:    0
```

SMASH (c)

```
(defun smash-object (&optional (object *me*) &aux parts)
  (cond ((primitive-box? object)
         (push object parts))
        ((instance? object) (let ((sub-parts (the-list-of (the 'parts object))))
                              (dolist (sub-part sub-parts)
                                (setq parts (append (smash-object sub-part) parts)))))
        ((or (buffer? object) (prototype? object))
         (let ((sub-parts (the-list-of (prototype-parts object))))
          (dolist (sub-part sub-parts)
            (setq parts (append (smash-object sub-part) parts))))))
```

In contrast, symbolic processing is so dynamic that the computer's operating system does not need to know at compile time how big the data structures are going to be, or what they will look like when the program finally executes.

Lisp efficiency

Lisp can represent arbitrary objects and the relationships between them while maintaining the memory allocation and data typing flexibility that is needed for such chores as optical mouse chip design. Lisp also allows the modeling of procedural knowledge that such designs require—how to do something, as opposed to what something is. Procedural knowledge is expressed by functions as executable Lisp subroutines that know how to perform some design-specific action or computation when they are supplied with appropriate arguments and symbols and the relationships between them.

Lisp efficiently deals with these symbolic lists and data structures. For example, the language imposes no penalty for dividing a program into dozens or hundreds of functions, each one the expert in some specific task. Thus, Lisp promotes modularity or the clean division of a program into unique areas of responsibility with well defined constructs. Such program segments are easily revised and updated without rewritting other program parts. They are also easily combined into larger, integrated programs with other added programs for more sophisticated applications. Symbolics has used these features for its optical mouse chip design and expects to use them even more for more complicated VLSI chip designs.

Lisp also frees the programmer from the detailed management of memory in the computer. Although it is possible to construct fixed-size arrays, Lisp excels in providing facilities to represent arbitrary size objects, sets of unlimited numbers of elements, and objects in which the number of details or parameters is totally unknown at compile time, if ever. As such, Lisp is ideal for the experimental, interactive, design of a chip like the one described where the problem is really incompletely specified at the beginning of the design and the chip designer must design on-the-fly.

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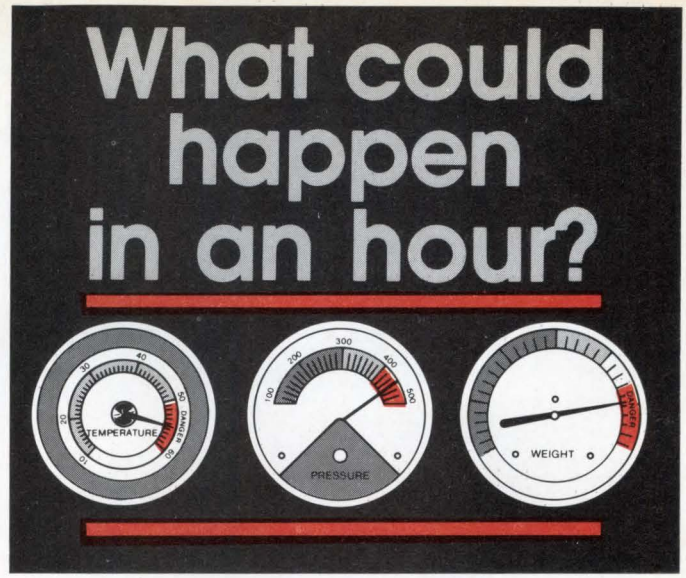

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CONTROL DATA

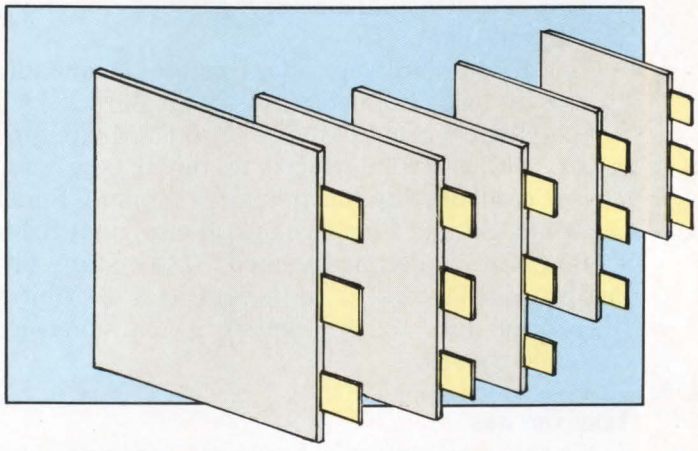
LISP WORKSTATION BRINGS AI POWER TO A USER'S DESK

Built around a full 32-bit NuBus using high density surface mount technology, this system provides an exploratory programming environment in a small ergonomic package.

by Charles J. Corley and Joyce A. Statz

Software development geared for artificial intelligence is moving from the guru's mountaintop down to the computer system designer's office and lab. A workstation that can provide a rich, exploratory programming environment would serve the needs of these more down-to-earth experts—particularly when the software design problem is not well defined in advance and when software experimentation is needed.

If it could work in a Lisp environment, possess the hardware and software tools for performing many software development functions, and come in an ergonomic package fitting on or near an office desk, designers would have the means for attacking their problems at their fingertips. They could resolve any issue not only with hardware, but with graphics tools, natural language interfaces, relational table managers, command interfaces, and knowledge engineering tools developed by the OEM and third party vendors. The Explorer workstation from Texas Instruments accomplishes these tasks.



The Explorer is small compared to other workstations of its power (keyboard and display fit on a desk; disk drives and CPU can go under or next to the work area). In large part, this is due to its extensive use of surface mount technology—the workstation's IC-based components are packed as densely as possible. The boards come in the standard three-high Eurocard format with DIN connectors for reliability; board and cable connections are through a chassis backplane for reliability.

Office suitability, flexibility, ergonomics, and reliability are only part of the story, however. An office-sized workstation with a design that

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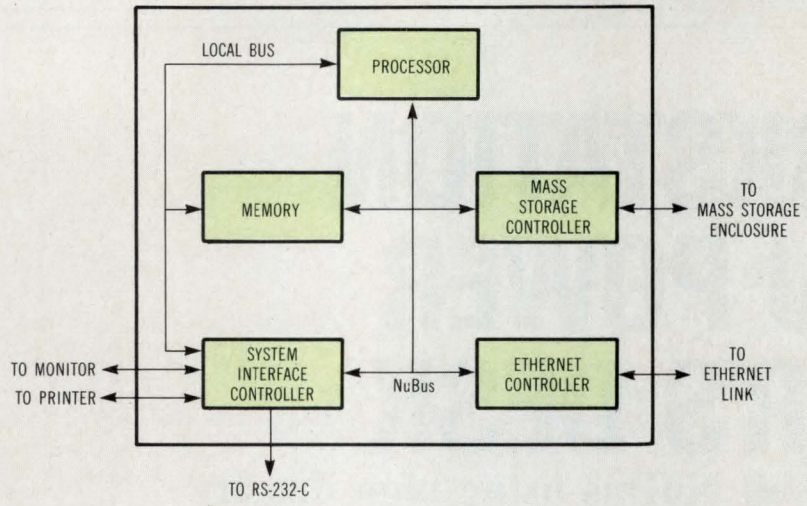
Joyce A. Statz is a project manager at TI. She holds a PhD in systems and information science from Syracuse University.



The system enclosure contains both a 32-bit NuBus and a 32-bit local bus that tie the main workstation units together. Links to I/O devices and other computers are also controlled by this enclosure that handles a variety of NuBus-based optional boards.

compromised its power would be of little use. The Explorer makes few design compromises and is suitable for many software development chores. On the software side, for example, it sports a full 32-bit data path Lisp processor and 16-K x 56 bits of writable control store for microcode. Moreover, the processor hardware support handles up to 128 Mbytes of demand-paged virtual memory, garbage collection, and tagged data.

On the pure hardware side, Explorer can handle up to eight daisy chained mass storage devices such as 112-Mbyte (formatted) disks and 60-Mbyte tape drives. These are interfaced to the chassis mass storage controller by the industry's standard Small Computer System Interface bus. It also has a 1024-x 808-pixel, landscape-oriented, raster scan, bit-mapped display that is connected by a 68-Mbit/s fiber optic link to the chassis system interface controller board.

Take the bus

All the workstation's hardware communicates through the full 32-bit read/write-based NuBus (see "Thirty-two bit system designers face decision time," *Computer Design,* Feb 1984, p 27). With the NuBus, each device (a PC board under onboard microprocessor guidance, for example) takes control of the system, becomes a master, and addresses another device which becomes a slave for that transaction. A handshake protocol between master and slave allows different-speed devices to communicate and permits fair arbitration between masters that evenly divide bus bandwidth.

This 37.5-Mbyte transfer rate, fair arbitration, 100-ns clock period bus can support direct address memory of up to 4 Gbytes because of its 32-bit addressability. The Explorer allows connections to the outside world through RS-232-C links, Ethernet, and other networks for which an interface board may be designed.

Most important for designers who seek a flexible workstation are the NuBus's processor independence and its ability to allow for a multiprocessor environment. PC boards added to an empty slot in the Explorer may have their own microprocessors that can communicate over the NuBus without causing the system integrator any anxiety. The system designer need not worry because the synchronous NuBus also accommodates 8- and 16-bit memory reads and writes.

Finally, in keeping with its design philosophy, NuBus allows memory-mapped event mechanisms rather than hardwired interrupts. Interrupts are implemented as write operations and need no protocols. A device can interrupt another device by writing to an address space monitored by the device to be interrupted. Priorities are determined by addresses.

To relieve the NuBus of many local operations, and thereby allow it to concentrate on making the Explorer system efficient, a local or private bus enables the Lisp processor to communicate with both the main memory and the graphics bit map. This 32-bit bus's operation is tranparent to the software tools that operate with the workstation; the user is unaware of its presence and function.

Lots of boards

Explorer's NuBus provides hardware support for research and development of complex applications. For example, the system provides a minimum of 2 Mbytes of RAM—expandable to 4 Mbytes with an optional memory board. Most important, the boards are designed to handle the 256-Kbit RAMs that are becoming available. As a result, 16 Mbytes of RAM are possible.

Memory words comprise 32 data bits and 4 parity bits. As might be expected, data parity is checked

on each memory byte. Using the local or private bus, memory access time from the Lisp processor to the memory is under 300 ns (800-ns cycle time). Of course, the memory boards can also respond to reads and writes from the NuBus. Like those on the local bus, these may be either 8, 16, or 32 bits wide.

As basic as memory boards are to workstation operation, the actual heart of the workstation may be said to be the so-called system interface board. This provides a variety of user and workstation services, including an interface to the 17-in. diagonal monitor, 111-key keyboard, 3-button optical mouse, and a future microphone and headset (for a speech option) through the fiber optic link. The dual 50-micron fiber optic link is critical to the Explorer's user interface. In fact, it is the only link from the display/keyboard combination (the workstation user's input mechanisms) and the system interface board (it connects via the local and the NuBus) to the rest of the Explorer system. The interface board also supports graphics control logic, connection to a parallel printer (Centronics-compatible), asynchronous and synchronous 19.2-kbaud RS-232-C ports, and various system resources.

For its part in system interface board operation, the graphics controller has a 1-Mbit bit map implemented with 120-ns RAM for fast image update. Write operations to the bit map are interleaved with display refresh at 60 times/s to eliminate flicker.

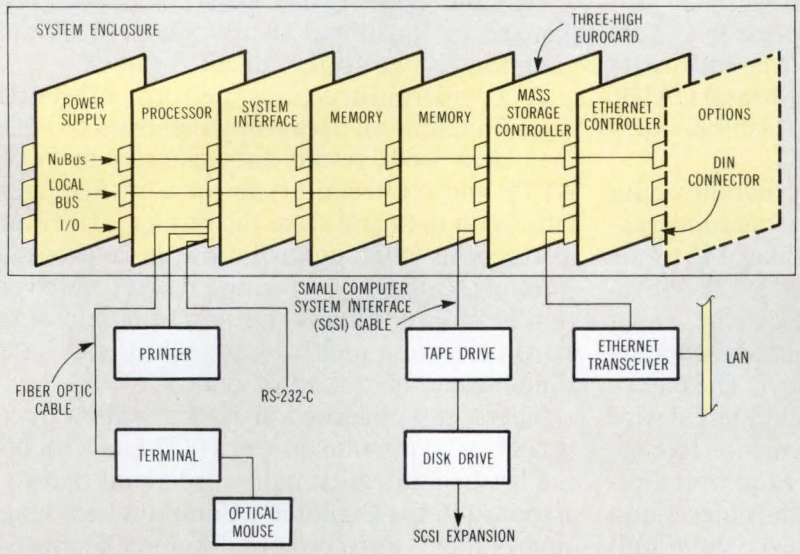
Much mass storage

As is typical in workstation design, the mass storage subsystem of the Explorer has dedicated microprocessor control for offloading the main processor from mass storage control overhead chores. A 10-MHz Motorola 68000 interprets processor requests for reads and writes; it also coordinates the transfer of commands, data, and status information between memory and mass storage. The 68000 takes care of data transfers to and from noncontiguous pages in main memory as well by means of the software mechanism known as scatter/gather. What is more, a data path in the mass storage controller, separate from the 68000 processor bus, allows noninterleaved data transfers to and from disks.

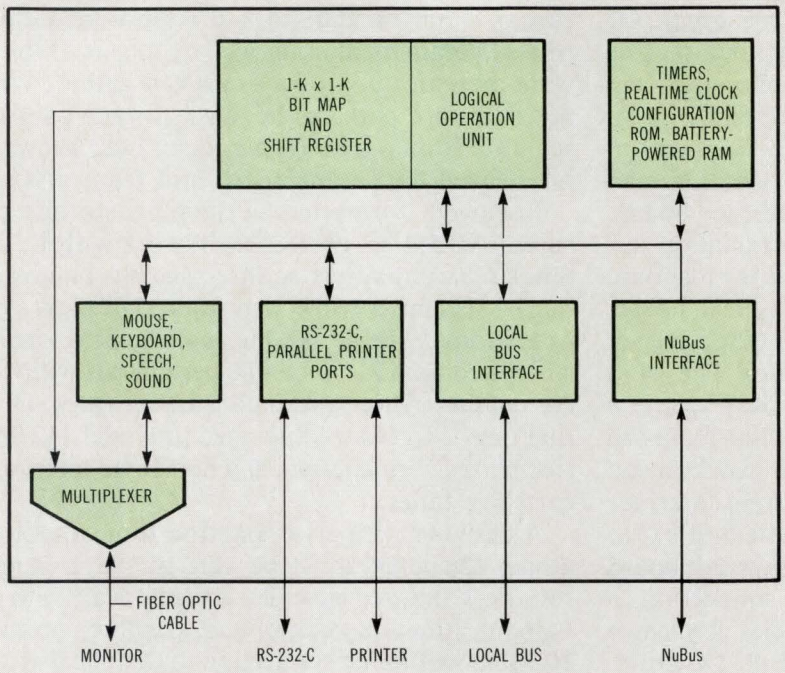
Intelligent formatters in the mass storage enclosures (two 5¼-in. devices each) work with 1.5-MHz Small Computer System Interface bus bandwidths, but 3-MHz buses will enhance speed of mass storage operations. The SCSI bus uses generic mass of storage commands to handle peripherals with different characteristics and data transfer rates. Devices that are currently supported include 112-Mbyte (formatted) Winchesters and 60-Mbyte quarter-inch cartridge tapes.

A designer with a workstation tool cannot work alone. Designers must be able to share expensive resources and, for example, communicate with other Lisp machines and computers. Explorer provides a 10-Mbit/s Ethernet connection to that local area network. Programs communicate physically over Ethernet through an Ethernet controller that plugs into the backplane of the Explorer system enclosure. This controller, in turn, hooks to an I/O adapter card and Ethernet transceiver and cable. Lisp programs communicate with other Lisp programs on the network through data streams—a software mechanism manipulated by Explorer's standard I/O calls.

Uni- or bidirectional streams are set up initially by a nonstandard "open" call. Streams allow for three networking services. The first of these, transparent file I/O, permits a user on one Explorer to access files, directories, and devices on the network as if these resources were local. The second service,



Typically, the NuBus and local bus connect boards in the system enclosure. The DIN connector-based three-high Eurocard PC boards are connected together and to the outside world through a variety of industry standard cables and interfaces.



The system interface board provides critical workstation functions. Moreover, a battery-based clock avoids system clock initialization; interval timers issue events at programmable intervals, and a 2-Kbyte nonvolatile RAM stores critical data at board removal time.

remote log in, allows a user to log into any network host by acting as a virtual terminal. The virtual terminal looks like either an ASCII device or a standard VT100 terminal. Finally, the electronic mail service allows mail to be sent to, or read from, a remote host.

Microinstruction formats

The Lisp processor and its software are the key to the workstation's software development power. By design, the Lisp processor is a general purpose, 32-bit microprogrammed processer with support for the Lisp virtual machine that the Explorer architecture implements. The processor and its circuitry occupy a single PC board dedicated to symbolic processing. This microprogrammed processor and its microcode are an outgrowth of the Massachusetts Institute of Technology (Cambridge, Mass) CADR design that is also used in LISP Machine, Inc's (Culver City, Calif) AI workstations.

The processor's 32-bit capability handles data paths and a writable control store for microinstructions. (One microinstruction cycles takes 142 ns, or 7 MHz.) The processor also features a 128-Mbyte virtual address space, a 4-Kbyte stack cache, and a 1-Kbyte page size. Demand-paged memory mapping hardware is also on the processor board. The microcode works with hardware to accommodate device handling, virtual memory management, storage allocation, and garbage collection. Moreover, bit-field hardware manipulates Lisp data objects and structure, tagged architecture for typed data, multiway branching to facilitate the complex control structures Lisp requires, language kernel support, and graphics support.

Explorer's Lisp processor is built around a set of nine Texas Instruments 74AS181 ALU ICs and one 74AS882 lookahead carry generator. This enables it to perform 16 high speed binary arithmetic operations on two 32-bit words. The ALU can function as a comparator—in its logic mode it performs 16 logic functions.

The Explorer microcode is implemented as microinstruction sets that are accessed from either the Lisp processor's control store PROM or from the writable control store dynamic RAM. The four possible microinstruction formats are ALU, BYTE, JUMP, and DISPATCH. Each comprises 56 bits organized in functional fields. Some fields may be common to two, three, or all formats.

ALU microinstructions perform arithmetic or logic functions on data from memories or registers; they then store results in memories or registers. BYTE microinstructions perform bit-field manipulations on data and store the results. JUMP microinstructions alter control flow in a program by jumping, calling, or returning if some tested condition is "true." Finally, DISPATCH microinstructions perform a multiway branch or call based on examination of a field of data.

These microinstruction formats allow the Lisp processor to operate on words (32 bits with bit 0 as the least significant), half-words, and bytes—as is standard in the Explorer's Common Lisp language environment. Furthermore, Explorer supports such Common Lisp extensions as the object-oriented

flavor system, MIT Lisp machine system functions, and loop macros.

With the Lisp processor board's architecture, data of any type is stored in memory in 32-bit quantities called storage quantums, or Qs. The three-field Q has a 2-bit first field used to reduce the storage requirements for Lisp data. The 5-bit second field stores the Q's data type or tag. Finally, the 25-bit third field contains either a pointer to another Q (its address), or data (depending on the Q's data type).

Programming causes the processor to perform a variety of workstation chores. For example, it accesses local memory via the local bus; it accesses other memory, posts events to other processors either in the local workstation or on the network, and performs I/O via the NuBus. It also takes charge of the configuration ROM that, conforming to user or system specifications, initializes system boards and devices.

Program development

No matter how efficient the Lisp processor may be at its assigned chores, the workstation user still needs a system that is conducive to software development and programming exploration. An integrated set of tools to create, compile, execute, and debug programs without leaving the editor is key to making full use of a workstation.

Explorer's Zmacs editor aids users by providing a realtime, window-oriented display editor (based on the MIT Emacs editor) that supports Lisp programming and other text development. It also has a Lisp Listener—a window-oriented tool that allows direct user interaction with the Lisp interpreter. A compiler converts Lisp functions to machine code for optimizing a program's execution speed and reducing its memory requirements. This is an essential feature in traditionally slow, memory-intensive Lisp environments.

The debugging toolkit exemplifies how the workstation was designed to ease software development. Simply, the debugger lets the user examine the environment in which an error or notable condition was signaled; the user can then correct the problem and resume execution, or abort the program.

When the debugger is entered, it displays a message describing the error and where it occurred. Inside the debugger, a variety of options are displayed. Starting from where the error was detected, it may be possible to examine and change the values of local arguments or variables, call the editor to change and recompile source code, and evaluate a Lisp object or reinvoke a function within the context of the current environment. A window-oriented debugger displays different types of information simultaneously as well.

Debugging tools include a break facility for halting program execution (either as specified in a program or from the keyboard at any time). A trace facility permits trace conditions to be user-specified. Each time a traced function is entered, its name and arguments may be printed. The step facility allows the program developer to follow each step in the evaluation of a Lisp form. At the user's option, the next form can be examined.

The advise facility can prove useful to the software experimenter. It allows a function's behavior to be modified without actually changing a source definition. This is useful for testing function changes

Common Lisp extensions

Even though a consortium of university, research laboratory, and industry parties has developed the Common Lisp environment, it can be extended. TI furnishes two of these extensions—the loop macro and flavors. The former is a facility for programmable iteration; the latter is a facility for object-oriented programming.

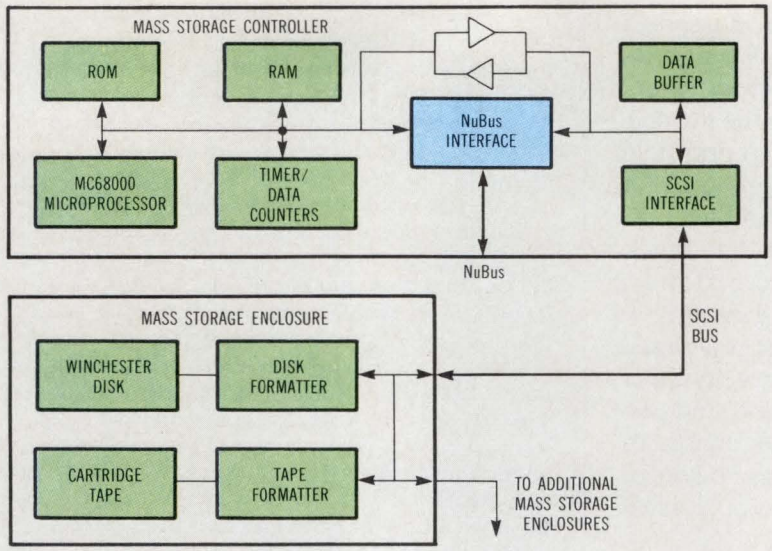
With the loop macro, a number of key words and predefined verbs allow the software developer to choose and combine English-like software clauses to define program iterations. Flavors use object-oriented programming constructs to deal with objects (see "Fifth-generation computing: dedicated software is the key," *Computer Design,* Sept 1984, p 150). These are active entities or data types that act as real-world objects to be represented in some way on the workstation screen. An object definition consists not only of data fields, but of the operations that can be performed on that data.

The basic idea of object-oriented programming is to hide the implementation of objects from the programs that use them. This is to enable software developers to concentrate on what can be done with objects, not on how these operations are coded. The goal is to enhance exploratory programming by concentrating on programming concepts. In addition, this approach to software design reduces the inherent complexity of symbolic programming programs. Programs are therefore easier to use, maintain, and modify.

A flavor is an object that describes a class of similar objects. It is said that a specific object is an instance of a flavor. When a flavor is instantiated, each instance has its own set of variables specifying attributes of the particular instance. These can be specified or set by default.

A flavor also has "attached methods"—these are functions that define operations for a flavor instance and operate on any instance variable. In order to operate on a specific object, an instance of the appropriate flavor is created and messages are sent to the object that names the desired operations. The object uses the attached method to handle the named operation, and returns the result.

The flavor system provides many predefined flavors that can be instantiated in programs as desired. It also provides a set of tools for user-defined flavors. In either case, flavors may be combined to define new flavors; and a new flavor inherits instance variables and methods belonging to its component parts.



The mass storage subsystem is controlled by both the mass storage controller PC board in the system enclosure and formatters in each mass storage enclosure. Mass storage enclosure wiring allows daisy chaining of up to eight 5¼-in. devices.

without a major commitment on the part of software developers, enabling them to save time and effort.

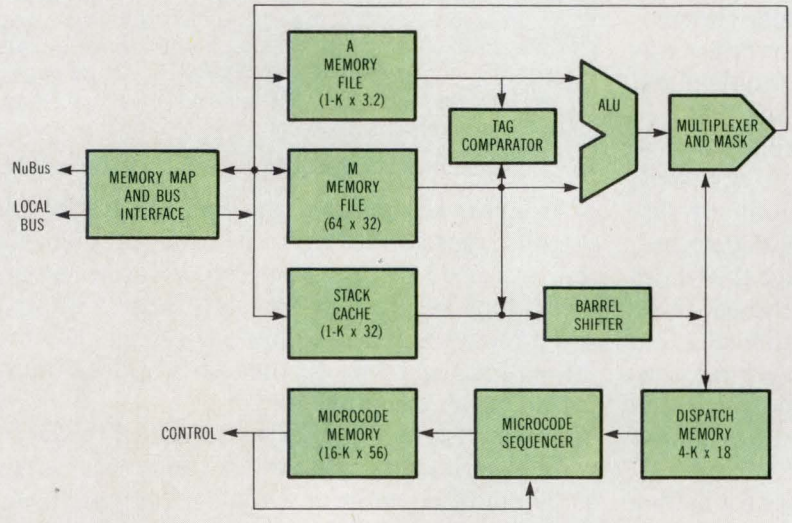
Because there is more to programming experimentation and software development than an editor, code optimizers, and debuggers, the workstation also features the Inspector. This is a window-oriented program for viewing and modifying such data structures as a Lisp object's properties. And the system definition and patch facility is designed to allow the integrating of many programs into program systems.

The performance monitoring facility was also designed with program developers in mind. This set of Explorer microcode-maintained performance "meters" can be Lisp program-accessed to monitor and analyze use of Explorer system resources. It ensures optimization of resource use. Finally, the command interface toolkit is geared to building interfaces to applications programs. This toolkit has macros and functions to support human factors including menus of commands and access to tutorial.

In addition to the program development tools, a set of toolkits are available to build application programs. Toolkits for building general kinds of applications include a text formatter, a graphics window system, natural language interfaces, and relational tables. For such knowledge engineering applications as the building of expert systems there are Prolog language and semantic network representation toolkits.

The natural language interface well-illustrates the kind of application software that may be developed in the Explorer environment. The natural language interface toolkit allows nonexperts to build natural language interfaces to their programs or to other systems such as a database query system.

In the TI approach to such queries, a set of windows and menus containing words and phrases in

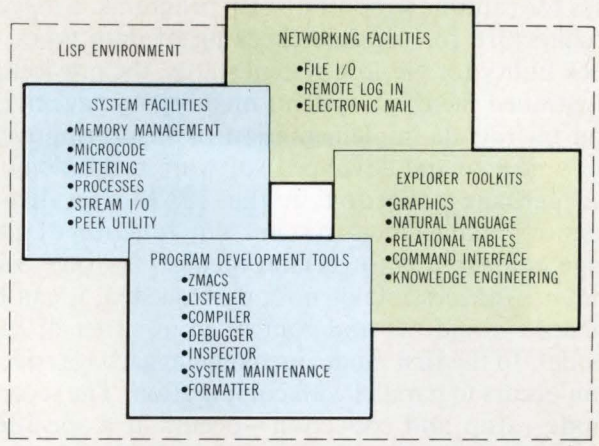


A variety of components work in a complex union in the Lisp processor. This interaction is best understood by first looking at the function of individual components, then dividing the processor operation into data paths and control paths, and then analyzing data and control pipelining (in order to understand processor timing). Finally, the processor's interface to memory, peripherals, and both the local bus and Nubus is determined.

English (or another natural language) is put up on the screen. Users make queries to their particular applications by selecting correct combinations of words and phrases with the mouse. Software controls the process, allows only proper sentence construction, and permits selections in active windows only. As the query is created, the software examines it, decides what windows will be activated next, and determines their contents. An incorrect, inappropriate, or ambiguous query cannot occur—contrary to the case in certain other natural language systems. Furthermore, error checks are unnecessary. Once the sentences are built, they are passed to the system or application, through translation, in the target language.

This feat has a cost. The natural language interface designer must build a lexicon, a grammar, and a screen description. The natural language interface toolkit helps in designing these data structures and makes the task straightforward. The lexicon specifies the words and phrases that can be used correctly in sentence construction and how they contribute to sentence meaning. The grammar indicates how words and phrases can be combined to form a sentence, and the screen description indicates how menus and their contents are configured.

Expert systems are one of the most promising areas of AI applications—and the Prolog toolkit is designed to help build simple rule-based expert systems. Another tool—a graph representation language known as Grasper—can describe an expert system's knowledge if that knowledge can be represented naturally in a semantic network. Grasper primitives include functions to create, delete, bind, evaluate, and show the existence of network elements. In such a network, the nodes represent specific objects, edges represent object relationships, and spaces represent object collections or specific views of object collections. Grasper primitives can describe data using these conventions, and the user can compose them into application-specific primitives.



Integrated software development tools furnished with the Explorer workstation are either system or application oriented. They are designed to work with each other and many of them have what amounts to internal tools to speed the workstation user's development work.

Doing windows

Window orientation is key to many of the Explorer's features. In fact, interaction with the Explorer system *per se* is through different rectangular screen areas called windows. A window is usually associated with one program and functions as a stream—it provides a place for the program to write to and read from. The Lisp processor supports a large amount of window system software that allows window creation, size allocation, labeling, graphics, mouse and keyboard monitoring, and interaction menus. The windows may be customized and incorporated into application software.

Window manipulation is a complex chore. For example, windows exist in a hierarchy with a screen on top and many subdivisions below. Moreover, a window may be divided into panes that can be manipulated like windows. Thus, their contents may be scrolled, created and destroyed, moved, and changed in size. Explorer also has a graphics package to allow interactive creation and modification of graphics displays in windows.

The graphics software toolkit for windows is necessary because the window system itself only provides basic facilities that allow an application to draw images on the screen. To change the image in even the smallest way, the application must redraw the whole image. The main goal of the toolkit is to speed up this process and allow the creation and deletion of objects that can be stored in files or moved about on the screen.

The toolkit comprises three integrated parts. The graphics window system provides flavor-based support to allow drawing lines, splines, arcs, circles, polygons, and text. They may be outlined, filled, or shaded. Once these objects are created, they may be manipulated like any other object. They may be combined, stored, printed, and shared.

The graphics editor and tree editor are built on top of the graphics window system. The graphics editor provides an interactive mechanism for using the graphics window system that includes, for example, rules and grids to locate points. On the other hand, the tree editor graphically displays any tree-structured entity. For example, it will display a flavor hierarchy which may be formatted vertically or horizontally. And, it allows pan or zoom on the displayed structure. For a specific application, the software developer writes interface routines so the tree editor can do its work.

Explorer's hardware and its program and application development tools are optimized for exploratory software development. But the system itself has

design features to help the user. These include facilities for runtime support of Lisp programs, a tagged architecture for runtime checking of data types, a peek utility for viewing system status, the previously mentioned metering system, memory management, and microcode implementation of Lisp primitives.

Typical of the advanced software technology is the garbage collection in the 128-Mbyte virtual memory management system. The function of garbage collection is to reclaim memory storage cells that are inaccessible or no longer needed; it can be turned on and off and controlled in either of two modes. In the first mode, incremental garbage collection occurs in parallel with computation. The second mode—stop and collection—occurs at a specified program point, or whenever the garbage collection is turned on in this mode.

Although garbage collection is normally difficult, the Explorer system eases the task by allowing objects to be created in specific areas of memory. Storage is divided into areas containing related objects that are independent of type. Users may specify the areas programs will use for storage (or users can opt for the default). Because related objects are grouped, data is paged more efficiently. And because the software developer can declare certain areas static (contents change slowly if at all), the garbage collector will not try to reclaim memory space in them.

Many of the system facilities, just as many of the software tools in Explorer, depend on the flavors extension to Common Lisp for their operation. Processes, for example, are implemented using the flavors system, allowing the software developer to define appropriate flavors for different processes. To do this, facilities are provided that allow the creation and control of user-defined processes.

With this software design, several computations may be executed concurrently by placing them in separate processes—each having its own program counter, function calls, and execution environment. All these processes run in the same virtual address space and share the same set of Lisp objects. Indeed, sharing objects is an interprocess communication technique, as are more conventional Lisp mechanisms such as interlocks. As expected, all processes are under the control of a scheduler that performs active process search functions as well as default time management.

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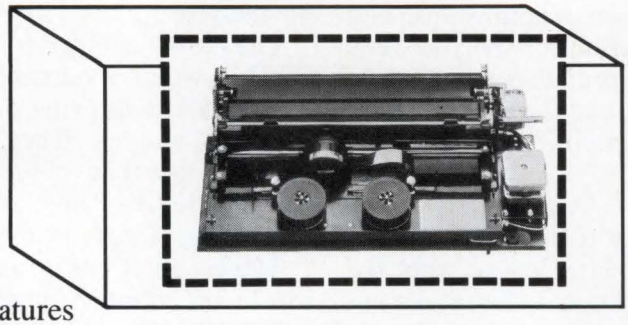

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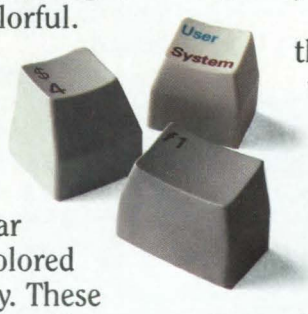

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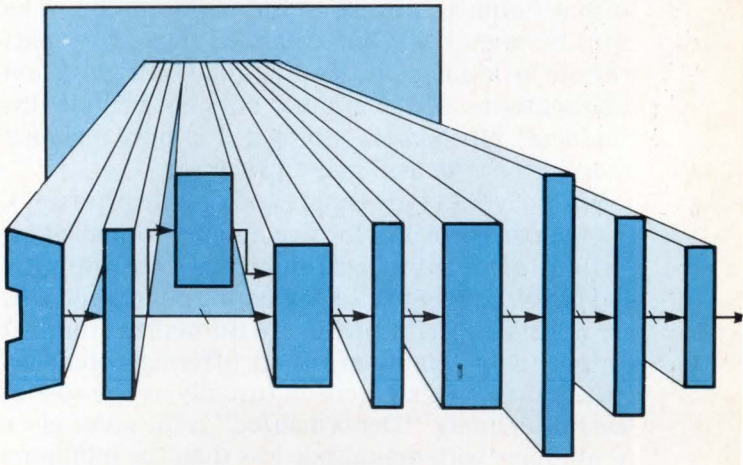
CIRCLE 73

IEEE FLOATING POINT CHIPS IMPLEMENT DSP ARCHITECTURES

Full compliance with Draft 10 version of the standard allows designers to produce working systems now.

by William A. Windsor, II



Digital signal processing and engineering analysis application designs have started to converge in recent years. Due to the advent of fast VLSI floating point processors, designers of digital signal processing systems need to be aware of issues normally common to engineering analysis. Although digital signal processing applications have focused on high throughput using fixed point processors, these applications now require the precision and dynamic range of floating point arithmetic in engineering analysis applications. Engineering workstation designers, for example, must know about high speed processing and pipelining, traditionally the domain of digital signal processing. But floating point processors meeting these demands have been complex and expensive.

Floating point processing has become widespread with the acceptance of proposed IEEE Standard 754 for binary floating point arithmetic. It specifies data types, rounding modes, and exception handling for floating point arithmetic. Application programs written to the standard are portable between computers. The standard applies to several aspects of digital signal processing design, including VLSI chip sets. One such set is the ADSP-3210 floating point multiplier and ADSP-3220 floating point ALU.

The latest version of IEEE Standard 754—Draft 10—defines the number formats that allow movement between floating point data and application programs using floating point operations. This version covers four areas: data formats, rounding, supported operations, and exception handling. Furthermore, according to the standard, any number has three parameters: a 1-bit field giving the number's sign as positive or negative, an exponent field in unsigned integer format, and a fraction field in unsigned magnitude format. The single-precision format has a 24-bit mantissa (fraction plus a sign bit) and an 8-bit

William A. Windsor, II is a product marketing specialist at Analog Devices, Inc, Digital Signal Processing Div, Norwood, Mass. He holds an MBA from Harvard Business School.

exponent. In contrast, the double-precision format has a 53-bit mantissa, including the sign bit, and an 11-bit exponent.

Inside the standard

Determining the value of a number according to the IEEE standard requires a series of calculations. A number's exponent, for example, is determined to be all 0s or all 1s. An exponent in the range of $00...0 < e < 11...1$ is called a "normalized" single-precision (32-bit) or double-precision (64-bit) floating point number. Exponents of all zeros or all ones are reserved for special operands. All zeros mean the number is a "denormalized" number (or zero); all ones signify infinity or "not a number" (NAN).

The IEEE Standard supports arithmetic, conversion, and comparison types of operations.

If the number is normalized, the exponent's field is decreased by the value or the exponent bias. This bias allows the exponent to take on negative values. In addition, a "hidden" bit is inserted before the implicit binary point or the fraction to make IEEE format numbers precise to an additional bit. The extra bit gives twice the dynamic range of formats without a hidden bit. The 32-bit single-precision representation of the number does not include this "hidden" bit memory storage; it is only included internally in the arithmetic processor.

For each data type (single and double precision), the standard provides for five number formats: normalized or denormalized numbers, zero, infinity, and NAN. Computations in floating point arithmetic are normally performed in the normalized number format, with double-precision offering higher accuracy than single-precision (usually as the cost of less throughput). "Denormalized" is the name given to numbers with magnitude less than the minimum value that can be represented in the normalized format. Zero has a special format and assigns a precise value that is separate from an underflow result. Infinity permits division by zero, or allows overflow to continue program execution rather than performing automatic trapping. Finally, NANs act as a data flow flag to signal a special value (such as an uninitialized variable) or to signify an invalid operation (such as zero times infinity). These diverse data types provide the system designer with the flexibility to handle a wide variety of results and conditions in a computation-intensive environment.

A rounding operation modifies a number to fit the amount of bits in such destination formats as single precision. Rounding can be biased or unbiased. Biased rounding introduces a small mean offset that alters the number in one direction when the rounding operation is performed. Unbiased rounding always rounds a number to the nearest representable number. When a number is exactly between two representable numbers, half the time the unbiased method rounds the number up, and half the time it rounds it down.

The IEEE Standard gives designers flexibility to select the best rounding matching scheme for each application. The Draft 10 version supports four rounding modes for each data format. "Round to nearest" is the default rounding mode. It rounds the result of the calculation to the representable value nearest the result. For a result halfway between two representable values, this unbiased rounding method yields the value with the least significant bit set equal to zero. "Round toward zero" rounds the result to the destination format's value closest to, but not greater than the result. Round toward zero is a biased rounding scheme that truncates all fraction bits with magnitude less than the destination format's LSB.

"Round toward plus infinity" rounds the result to the destination format's value closest to, but not less than the result. If a result is greater than the maximum representable normalized number, the number is rounded to plus infinity. "Round toward minus infinity" rounds the result to the destination format's value closest to, but not greater than the result. If a result is less than the minimum negative representable number, the number is rounded to minus infinity. Both round toward plus infinity, and its converse, round toward minus infinity, are biased rounding schemes used in interval arithmetic. They establish the bounds of the interval within which a number is expected to lie.

Supported operations

The IEEE Standard supports arithmetic, conversion, and comparison types of operations. These provide the core functions for designing a scientific computation processor, or for supporting a high level language's arithmetic operations. An arithmetic exception condition happens when an operation yields an abnormal result (such as an overflow to plus infinity). The floating point processor signals each exception with a flag that may generate a trap, if traps are enabled in the external system.

The Draft 10 version specifies five types of exceptions. One of these, the "invalid operation," is signaled when an operand is invalid for the performed operation. The invalid operation exception occurs in a variety of cases. These include any operation on a signaling NAN, magnitude subtraction of infinities [(+infinity) + (-infinity)], multiplication (zero x infinity), division (zero/zero or infinity/infinity), remainder (x REM y, where y is zero or x is infinite), and square root for an operand less than zero. Finally, comparisons using "less than" or

"greater than" signal an invalid operation when the operands are unordered.

Exceptions occur in four other cases. The first results from a zero denominator. The second, overflow, is signaled when the rounded result exceeds the maximum representable number in the destination format. The third, underflow, occurs when the operation's result is less than the minimum representable number in the destination format, or when accuracy is lost in representing a denormalized number. Finally, inexact exceptions occur when the rounded result is not exact, or when the result overflows without an overflow trap.

Design options

One of three options can be used to design an IEEE floating point processor. One option makes it possible to design the processor from SSI, MSI, and LSI logic. This design usually has fixed point processors (multipliers and ALUs) and barrel shifters to perform the floating point normalization and denormalization functions. These designs—found in array processors and mainframe arithmetic processors—are programmable and fast, but large and expensive.

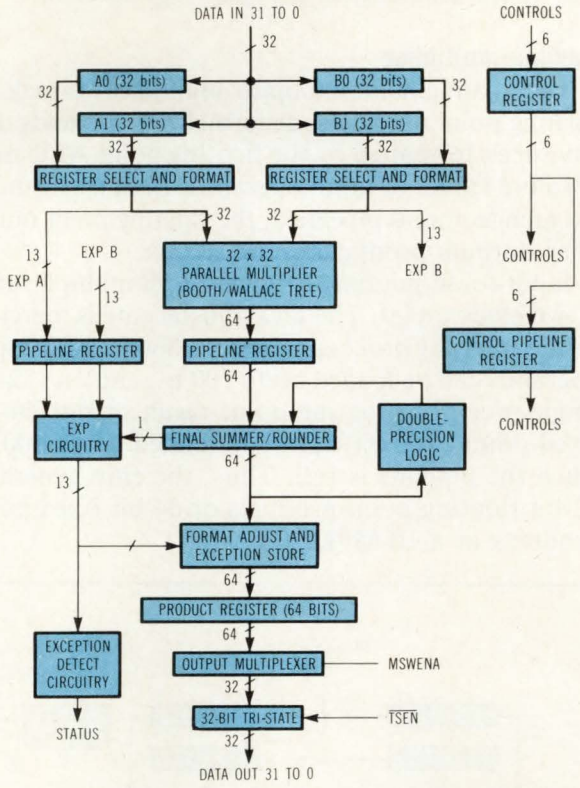
A second design option incorporates a floating point coprocessor for the system microprocessor. Although coprocessors handle a wide range of operations and data types, they are slow and designed only for certain microprocessor buses.

Finally, the engineer can design the processor with VLSI floating point devices. This design, while more expensive than the coprocessor solution, offers 100 to 200 times the performance, at a fraction of the cost of MSI processors. VLSI floating point chip sets offer such basic floating point functions such add, subtract, and multiply. Using these, the designer implements any remaining functions with microcode.

One of three options can be used to design an IEEE floating point processor.

One such VLSI chip set, Analog Devices' ADSP-3210 floating point multiplier and ADSP-3220 floating point ALU, comprises the basic elements needed to construct an IEEE-compatible processor. The set permits 32-bit single-precision floating point at a throughput rate of 10 million floating point operations per second, 64-bit double-precision floating point operations at 5 MFLOPS for the floating point ALU, and 2 MFLOPS for the floating point multiplier. It also handles 32-bit fixed point capability at 10-MHz throughput. All this is compatible with the standard, using only a single-level pipeline processor.

The chip set's three data formats handle performance requirements in applications such as engineering analysis, DSP, array processing, and graphics. For example, engineering workstation simulations require single- and double-precision floating point for Spice analysis and finite element analysis. And, the graphics processors in these systems use 32-bit fixed point arithmetic to calculate the memory pointers to their pixel arrays.



Analog Devices' floating point multiplier conforms to the proposed IEEE floating point arithmetic standard. This half of a two-chip set is geared to digital signal processing (DSP) applications, featuring single-pipeline operation.

The three data formats are also necessary in computer arithmetic processors and Fortran accelerators, and for implementing high level software language computations. Integrating all three data types onto one chip set is essential for offering full arithmetic processor capability with minimum expense and board space use.

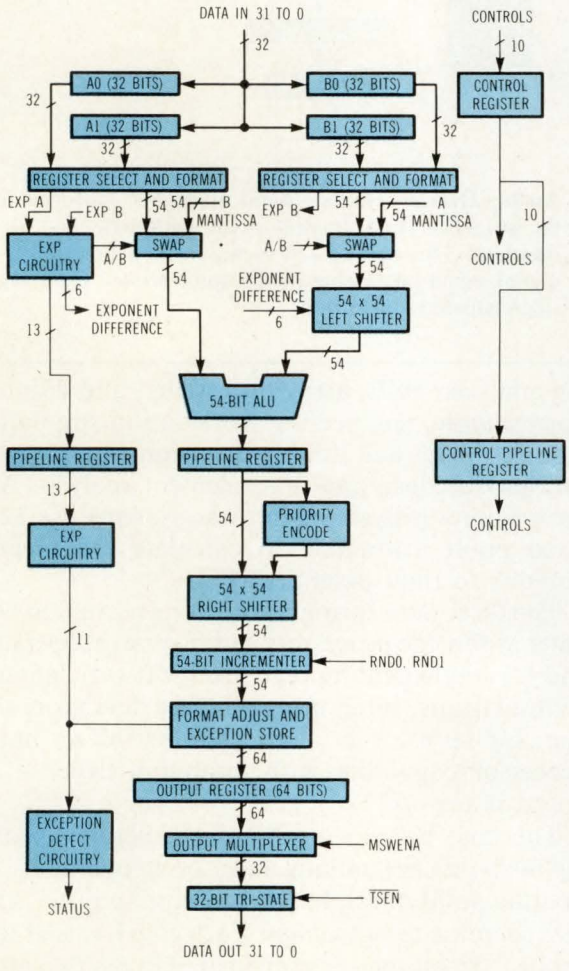
The chips have identical input structures, providing flexibility in handling and storing operands. The floating point multiplier has an input register structure common to both chips. Each chip has four independent 32-bit registers, divided between two inputs (A and B). The input register select controls enable writing to any A and B input registers on every cycle. At the same time, the input operand select determines which A and B input registers are used as multiplier/ALU array operands. The input registers allow storage of data used to compute several output values.

This feature is valuable in fast Fourier transform algorithms and double-precision operations.

Flexible multiplier

The floating point multiplier multiplies normalized floating point operands, denormalized operands that have been formatted by the floating point ALU, and absolute values of input operands. Because its internal architecture is pipelined, the floating point multiplier outputs products every 100 ns.

Input-to-output time for each 32-bit multiplication is two clock cycles. The I/O transfer rate is matched to the internal processing speed. Two 32-bit input operands can be loaded every 100 ns, and one 32-bit single-precision floating point result or one 64-bit fixed point product can be unloaded every 100 ns when the pipeline is full. Thus, the chip generates 32-bit floating point products or 64-bit fixed point products at a 10-MFLOPS rate.



The floating point ALU has the same four input registers as its companion chip, the floating point multiplier. It also has a single-pipeline level, and each pipeline stage is completed in one clock cycle.

The floating point multiplier handles denormalized operands by multiplying denormals that have been formatted ("wrapped") by the floating point ALU. This method is chosen because of constraints on chip space. Handling denormalized numbers requires a barrel shifter. The size of the multiplier array, however, tends to prohibit inclusion of a barrel shifter. Denormalized multiplier inputs are flagged by a status ouptut signal and returned to the floating point ALU for formatting. With this design, the floating point multiplier achieves calculation compatibility with the full range of IEEE operand values. This is possible without any overhead for numbers in the normalized range.

Double-precision operations are performed in five cycles. On the first cycle, the floating point multiplier starts to multiply the two least significant 32-bit words stored in A0 and B0. At the same time, the user loads A1 and B1 with the most significant 32-bit words of each operand. Thereafter, the multiplier chip controls the operand sequencing and control for all the double-precision cross products. The 64-bit output product is available five cycles after the multiplying begins. This is equivalent to a double-precision floating point multiply 2-MFLOPS throughput.

High throughput ALU

The floating point ALU performs addition, subtraction, and conversions between the supported data types at the same 100-ns cycle rate as the floating point multiplier. It also performs absolute value operations and 32-bit logical operations. The floating point ALU's single pipeline stage matches that of the multiplier, providing parallelism in the processors and avoiding data flow bottlenecks. It processes all 32-bit single-precision floating point and 32-bit fixed point operations at an effective throughput of 10 MFLOPS.

Arithmetic operations, logical operations, and conversions are present in the floating point ALU instruction set. Arithmetic operations (add, subtract, add with carry, subtract with carry) provide flexibility in ordering the input operands (A-B or B-A). These operations also enable absolute value operations on any input or output operand. The floating point ALU performs arithmetic operations directly on normalized and denormalized numbers. Logic operations on 32-bit fixed point fields are also performed at the 100-ns cycle rate.

The floating point ALU executes conversions between floating and fixed point formats. In addition, the wrap instruction formats ("wraps") denormalized multiplier operands. The unwrap instruction will convert wrapped operation back to the denormalized format.

The floating point ALU throughput matches that of the floating point multiplier for single-precision

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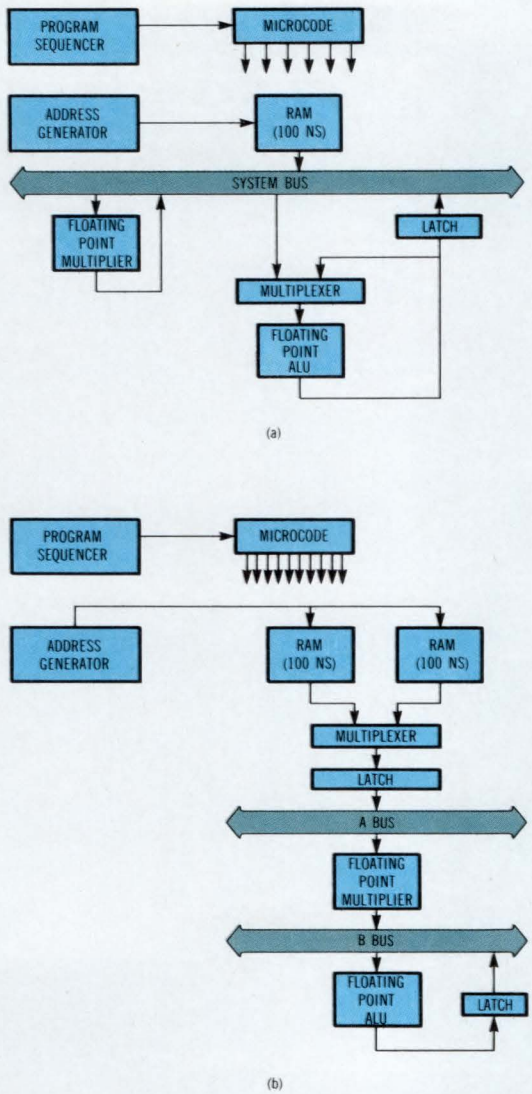

To meet the performance goals of a DSP system, the designer can choose from the floating point system's single-bus (a) or a dual-bus (b) architecture. Each has advantages that may be traded off in the initial design stages.

The floating point ALU throughput matches that of the floating point multiplier for single-precision and fixed-point operations, but performs double-precision operations faster than the floating point multiplier. The chip generates 32-bit floating point sums or 32-bit fixed sums at a 10-MFLOPS rate. However, 64-bit double-precision floating point sums are generated every two cycles, corresponding to a double-precision floating point 5-MFLOPS throughput.

As discussed, the chip set is fully compatible with the IEEE Standard 754. It supports operations on normalized, denormalized, zero, infinity, and NAN data types for both single- and double-precision floating point formats. It also supports all four rounding modes for each of the three data formats. Four exception conditions are provided as direct status output pins (overflow, underflow, invalid operation, and inexact result). This design provides immediate system response to an exception. The fifth exception, division by zero, is detected in microcode when division is performed.

System integration

Several features of the floating point chip set increase the design flexibility of DSP systems and general-purpose floating point processors. For example, the four input registers on each chip allow operand storage. This gives flexibility in timing operand transfer and storage. Furthermore, the registers avoid bus collisions that occur when data transfers are constrained to certain cycles. Another feature latches all instruction controls at each pipeline stage. This allows controls to change every cycle without waiting for pipeline delays. Both these features also facilitate microcode programming.

Two system-level designs illustrate the characteristics and performance trade-offs of the system. The single-bus floating point processor is simpler and less costly than the dual-bus architecture. Dual-bus architecture offers higher performance, however. Both architectures offer high throughput for the multiply/accumulate operations critical in DSP. They also minimize the glue chips for system interfacing.

The single-bus floating point processor performs multiply/accumulate at a 300-ns throughput rate. This provides the basis for an 8-cycle FFT butterfly operation that allows a 4-ms time for a 1024-point complex FFT. Even double-precision floating point operations have a 1.4-MFLOPS throughput.

The dual-bus architecture offers higher throughput while maintaining a general-purpose processor structure. Multiply/accumulate can be performed at the 10-MFLOPS throughput rate for the processors, and a full radix-2 butterfly takes six cycles. A 32-tap floating point finite impulse response filter can be processed at a throughput rate of 3.2 μs.

Finally, a second multiplier added to the dual-bus architecture lets the designer perform double-precision floating point multiply/accumulate at a 2.0-MFLOPS rate. By trading off system complexity issues, therefore, the DSP designer has multiple options for attaining high performance.

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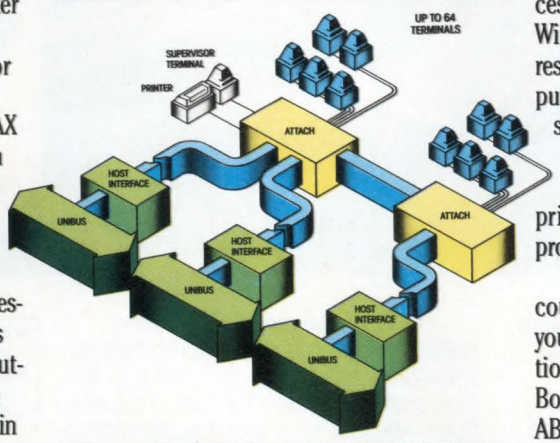

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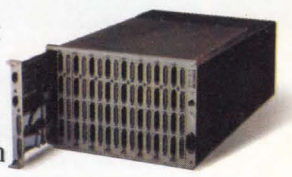

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CIRCLE 75

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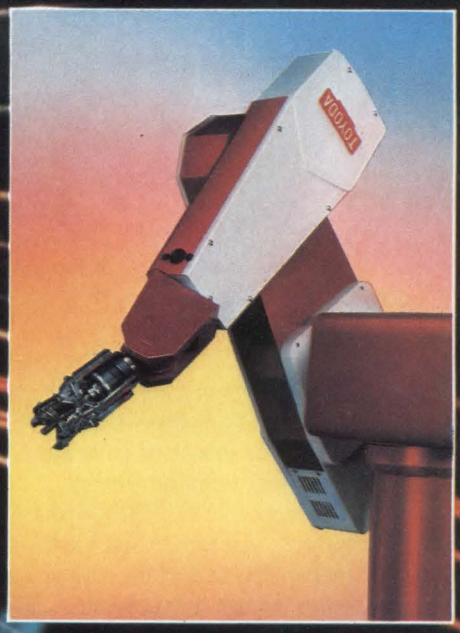

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CIRCLE 76

ADA MAY DEFINE NEW GROUND RULES FOR PROGRAMMING

By providing such benefits as structural constructs, modularity, and concurrent processing, Ada could help set a new standard for programming languages both outside and inside the DoD.

by Robert Bergman

The world's largest software buyer, the United States Department of Defense, faced a software crisis in the early 1970s. More than 450 computer languages (including incompatible dialects of the same language) were used to write the programs that controlled an expanding share of the U.S. defense system. Many of those programs were virtually incomprehensible and difficult to maintain. Often, the expense of maintaining a program amounted to many times its original cost.

Creation and installation of the Ada language has resulted from a decade-long effort to remedy that situation. Ada is a complete, general-purpose, high order language designed to make programs legible, reliable, and easy to maintain. It embodies such software engineering concepts as structured constructs, abstraction, modularity, and concurrent processing.

Ada's modularity allows several people to write programs simultaneously, and it permits substantial use of previously written material. Explicit data typing enforces Ada's clarity and maintainability while simple and standard exception handling provides fault tolerance. Ada also allows direct interface to hardware, an important factor in systems critical to defense missions.

The U.S. DoD has ensured Ada's future by its fiat declaring the new language alone acceptable for the most vital of the United States defense projects. The DoD handed down a similar mandate for Cobol in the 1960s. Therefore, private companies that fail to incorporate Ada in their systems cannot do business with the DoD.

Ada was designed under the direction and funding of the DoD for use in large, long-term, frequently modified software systems. It will be used in three classes of applications within the defense system: numerical, systems, and realtime programming.

In forming the language, developers paid particular attention to maintaining similarity to existing languages. The result is a product of language engineering, not computer language science. Many of its constructs are Pascal-like, with strong influences from Algol 68, Simula, and PL/1. APL Basic, Cobol, and Fortran influenced the language to a lesser degree. Due to this distillation, Ada marks a clear and recognizable reference point in the history of programming language development.

Strict control

Ada development is rigidly monitored by the DoD. To be called "Ada," a language must comply with MIL-STD 1815 as published in the Ada Language Reference Manual. The LRM allows no variations from the standard, no subsets or supersets. To become an officially recognized Ada compiler, for example, a submitted program must pass more than 2000 separate tests and be validated by the DoD before being used in any mission-critical system. Only a few organizations, including New York University, Rolm Corp (Santa Clara, Calif), Data General Corp (Westborough, Mass) TeleSoft (San

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Tracing Ada's evolution

From 1968 to 1973 the United States DoD experienced a 51 percent increase in direct costs of its computer systems. These costs were aggravated by the fact that the DoD's computer programs were beset by late delivery, unreliability, and cost overruns. By the end of that period, the DoD was expecting geometric increases in its computerization costs. Software in 1973 comprised about $3 billion, or 46 percent of DoD computer costs, and it was obvious that the total would increase exponentially as systems became more sophisticated.

In looking at the problem more closely, the DoD realized that many of the approximately 450 computer languages and dialects loose in its own house were ill suited to applications. Moreover, it recognized that there were few programming tools available and that programming methodologies often were not easily developed and implemented. Since embedded systems, which were later redefined to mean mission-critical systems, used more than half the software, it became apparent that something had to be done to end the proliferation of languages within the DoD.

The U.S. Navy, Army and Air Force found that no current language could meet its needs for parallel processing, realtime control, powerful exception handling, and unique I/O control. As a result, in 1975 a major effort was undertaken to develop a new high level language. Input was received from 85 DoD organizations, 26 industrial contractors, and 16 universities. By the end of 1976, a recommendation was made that a new language be based on the best concepts of Pascal, Algol, and Pl/1. In 1977, after 17 vendors responded to the DoD's request for proposal to develop a new language, four vendor "finalists" were selected, all of whom were using Pascal as a base. In May 1970, under contract to the DoD, the combined effort of Cii Honeywell Bull in France and the Honeywell Systems and Research Center (Minneapolis, Minn), with a team led by Jean D. Ichbiah of Paris, was selected to implement and define the work of the many who had contributed ideas and concepts.

The product of this massive language engineering effort was originally named DoD-1. As finalization approached, the language was renamed for Ada Augusta Byron Lovelace, daughter of the poet, Lord Byron. Lovelace wrote the "programs" for Charles Babbage's 19th century analytical engine, becoming the first programmer and undoubtedly encountering history's first computer program bugs. A number of housekeeping steps followed, including the trademark of the name "Ada," establishment of MIL-STD 1815 (the numeric honoring the year of Lovelace's birth), and establishment of validation procedures and tests.

Diego, Calif), and Western Digital (now GenSoft of Irvine, Calif) have certified compilers. A number of other compilers are expected to be validated within the next year.

A DoD policy memorandum, dated June 10, 1983, details Ada's impact on businesses that are planning to work with the DoD. According to the official statement, "The Ada programming language shall become the single, common computer programming language for Defense mission-critical applications. Effective Jan 1, 1984 for programs entering advanced development and July 1 1984 for programs entering full-scale engineering development, Ada shall be the programming language."

The DoD requires such stringency because the United States will be defended by "smart and agile" weapon systems that are dependent on computer power. And computer power depends on sophisticated, responsive, understandable, and maintainable software. A look at Ada's characteristics shows how these goals will be achieved.

How the language works

Ada has a very large semantic structure, incorporating many powerful constructs. Six areas highlight the range of Ada's capabilities: program structure, declarations, data types, statements, I/O, and generics.

An Ada software "system" (a more meaningful concept than "program") is made up of one or more of three distinct structural elements: subprograms, packages, and tasks. A subprogram expresses a single action or complete algorithm within a program. Subprograms include procedures and functions that are used primarily as main program units. They can express functional control and implement type operations.

A package is a collection of data types and operations allowed between objects of those data types. Packages express or enforce a user's logical abstraction of the data and can include data types, data objects, subprograms, other packages, or tasks. Packages are used primarily in the named collection of declarations. They identify groups of related program units and contain abstract data types.

Tasks define action logically executed in parallel through a single processor, multiple processors, or a network of computers. Tasks are used in concurrent actions, for routing messages, controlling system resources and providing interrupts, and for other similar program needs. While these broad definitions may seem to set the elements apart, no one structure has actual precedence over another. In fact, each unit can occur within each of the other units, depending on the specific solution and system being developed.

The declarative part of any Ada unit denotes types, variables, and constants of the logical entities to be used in the program unit. Further, the declarations can be used to specify names and parameters of various subunits (packages, task modules) that are included in a program unit. The declarations necessary for a program unit may be physically

separate from the implementation of those declarations, and as a result may be compiled separately. This represents an important consideration in modular construction of a program system.

Data types provide clarity

Explicit data typing is the main reason for Ada's clarity and maintainability. Every data object used has a specified type defining its set of possible values, the applicable operations, and its internal representation. The language structure ensures that each object is consistent with its definition. It also permits the definition of unique types to conform to one of three needs of the program: value range, applicable operation, and internal representation. Ada also encourages the use of subtypes. These set forth a subset of an established type explicitly by adding some special constraints, or by distinguishing one value from another through definition.

Several predefined data types are available to the Ada programmer. These include such scalar types as integer, floating point, and character; enumeration types; composite types; dynamic array types; and allocator types. Enumeration types, including Boolean, can be used for character sets (up to 128 ASCII) and for problem-oriented data. Unlike enumeration types in Pascal, the enumeration values in Ada may be used with I/O routines.

Composite types indicate array objects with several components. Array types represent a collection of homogeneous types; record types also represent a grouping of homogeneous types. For dynamic array types, the specified range may be unconstrained in the declarations, but bounded by a value developed within execution of the program. Allocator types are used for storage of an object. These types can be initialized to a value, and return an access value to an object. Private types are used to hide package structure details.

Experienced programmers will be comfortable with Ada systems and syntax because the statements used are well known and direct. The semicolon is the statement terminator as in Pascal and C, and the control structures are well defined, rigid, and restricted in use. Statements used in sequential programming include assignment statements, conditional statements, loop statements, and case statements.

Assignment statements replace the current value of a variable with a new value specified by an expression. If-Then and If-Then-Else statements select a sequence of statements according to logic dictated by the values of Boolean conditions. Case statements allow the execution of alternative statement sequences based on the value of the case selector.

Loop statements, which can be labeled, take one of three forms. These are the basic loop; the while loop, which continues iterations as long as some condition is met; and the for loop, which adds a control variable and range of values to a basic loop. Ada also uses the exit statement, which allows departure from any loop when a specified condition is met.

Another series of statements is available only within tasks. These statements control the parallel processing of tasks. They include an entry call (specifies a rendezvous between two or more tasks), an accept (dictates the action when an entry call is initiated), and a select (a predetermined wait for a particular rendezvous).

Standard I/O handles the nonstandard

The language definition includes standard packages for I/O, including direct I/O, sequential I/O, and text I/O. Within these types are strict procedures for working with individual characters in the I/O stream, for dealing with integer I/O, floating point I/O, Boolean I/O, and enumerated I/O in general.

Since defense systems often interface with nonstandard I/O devices, this kind of I/O is handled in still another standard I/O package called low level I/O. It uses two parameters to identify the device and the data. Procedures within the low level I/O package send control instructions to the device and also receive information from the device. This standard method for handling I/O makes it possible to exploit the underlying hardware features of a system with relatively simple address, enumeration typing, length and record typing specifications.

Ada provides for the broad use of generic program units, which are similar to common macros. Generic units in Ada are templates of program units. The "blanks" in these units only need to be filled in when

A reliable and maintainable language

As a design language, Ada has capabilities that validate three vital and basic assumptions. First, Ada can express programming solutions to application problems throughout the anticipated life of a project. The language allows design of a program solution without immediate concern for the actual code.

Secondly, Ada code can be written by several people working simultaneously or independently over a period of time. Individual modules (or even parts of modules such as declarations) can be compiled separately. Finally, Ada makes substantial use of previously written material and subprograms. Coupled with its flexibility in writing code, this means the resulting code will be understandable.

Ada's design encourages programming that uses such software engineering techniques as structured constructs, modularity, strong typing of variables and objects, "information hiding," and data abstraction. The language also supports concurrent processing, simple and standard exception handling to provide fault tolerance, and generic definitions to support macros in the use of development. Above all, Ada's clarity provides strong reliability and maintainability. Black boxes incorporated into many mission-critical defense systems allow Ada to interface directly with this hardware.

compiling and adding to a program under development. This reduces the complexity of large programs. Generics are powerful tools because they are easily understood and used, yet have been refined to the point of maximum efficiency. Generics do not create any code and must be defined before use. They are composed of normal Ada statements and do not require a special and separate programming language.

Exception handling is yet another key consideration in defense systems because the systems are usually unattended and must be able to recover gracefully and quickly from errors. In many languages, an input format error or divide by zero would cause a program to abort. Such "trivial" errors are not acceptable in a mission-critical system. As a result, Ada provides for simple and standard handling of exceptional situations in a structured way. Some of these methods even allow for continuance of statement execution within the error handling routine itself.

Ada contains stong and broad provisions for overloading (the process of assigning several alternative meanings to an identifier or operator). Ada then determines which meaning to use in the program by referencing the "homonym" declarations. One advantage of such overloading is that separate programmers, working independently on the same system, do not need to be concerned about duplicating identifiers. The language itself will resolve most conflicts in syntax and direct redefinition procedures will take care of the rest.

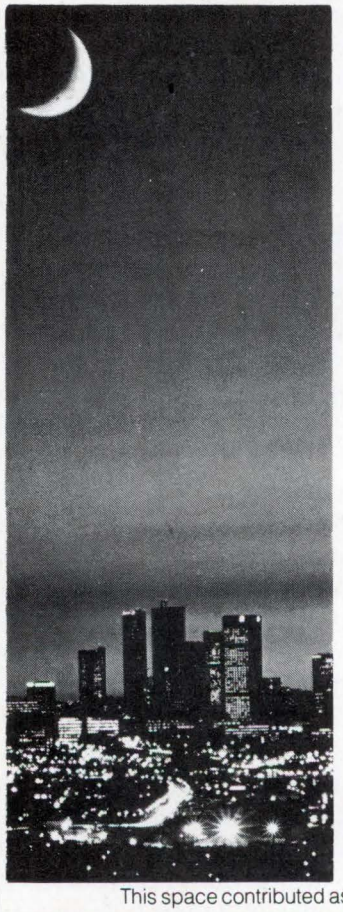
Advantages and disadvantages

As happens with any "new" language, the programming community has not received Ada with total enthusiasm. On the negative side, there have been complaints about its complexity and size, as well as the rigid definitions; insistence by the DoD on no subsets or supersets; and depth and intensity of the validation procedure. Many of these same objections were raised against Unix and the C language when that now commonplace pair was introduced. In addition, initial costs of training to use Ada will be high, but the eventual costs of maintaining Ada systems should be low.

On the positive side, Ada has a number of desirable features. For example, its similarity to other languages should speed the process of learning the language. The flexibility, exception handling, and wealth of I/O routines seem to make it ideal for the large realtime systems used in defense applications. Strong typing and modern structuring techniques help achieve reliability, ease of understanding, and simplified maintenance. And previously written packages can be reused in new and developing projects. Ada can function as a system design language, an architectural language, or an implementation language. This flexibility should enhance the communication process between system designers and programmers.

With the weight of the DoD behind the Ada effort, there is little doubt that the language will become a significant factor in data processing of all types. It is well to remember how Cobol became a major language after the DoD encouraged its development. Ada can be expected to follow the same path. Its applications in primary defense systems undoubtedly will be the first benefits recognized, but all private corporations expecting to do data processing business with the DoD must realize that use of Ada will be an inviolate ground rule.

Because of the DoD's backing and its clear advantages as a language, Ada seems certain to become one of the key languages in the next decade's software development. Ada may help end the proliferation of languages outside the DoD as well as within it.



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Ada's First Family

Compiler	In Production Use	Validated
MC68000/ROS		✓
TeleSoft	✓	✓
Labtek (Wicat)	✓	
MC68000/ Unix		✓
System V	✓	✓
Berkley 4.2bsd	✓	In Process
Unisoft Unix	✓	In Process
VAX/VMS	✓	In Process
VAX/Unix	✓	In Process
IBM 370/VM/CMS	✓	In Process
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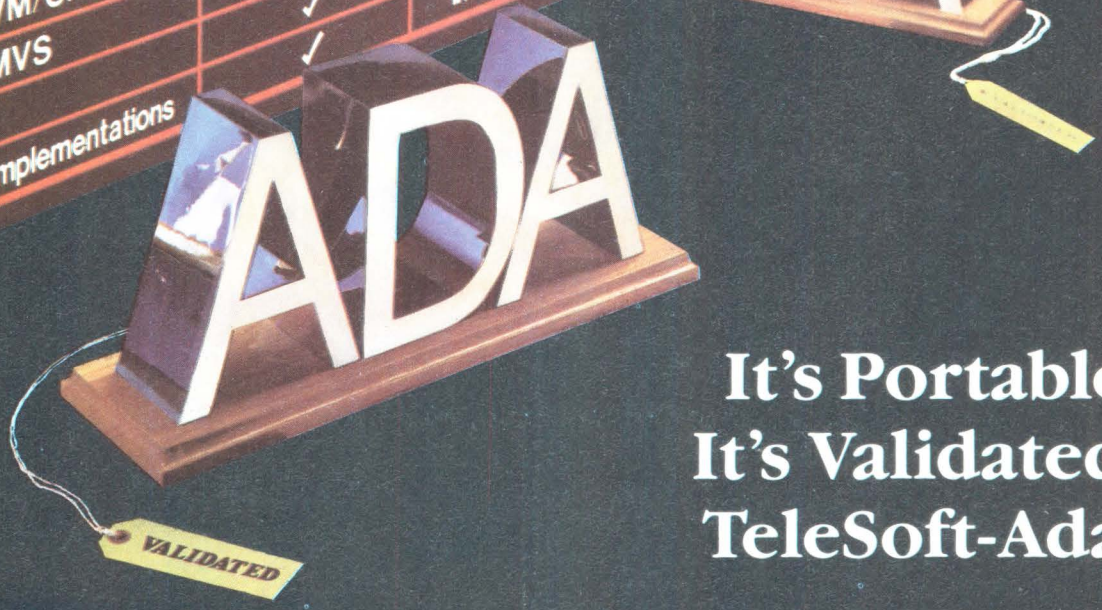
Additional Implementations		



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CIRCLE 78

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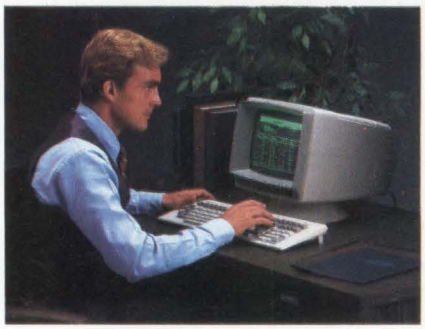

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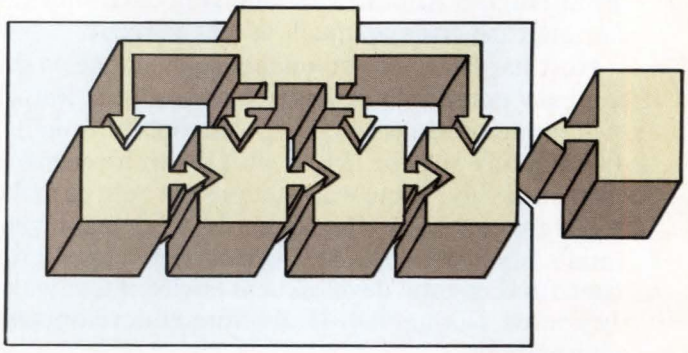
CIRCLE 79

INTEGRATED TOOLS ACCELERATE CODE DEVELOPMENT

Integrated source and version control, electronic mail, and standard interfaces for programming languages and operating systems can move the software task faster than using additional programmers.

by Dennis Carter



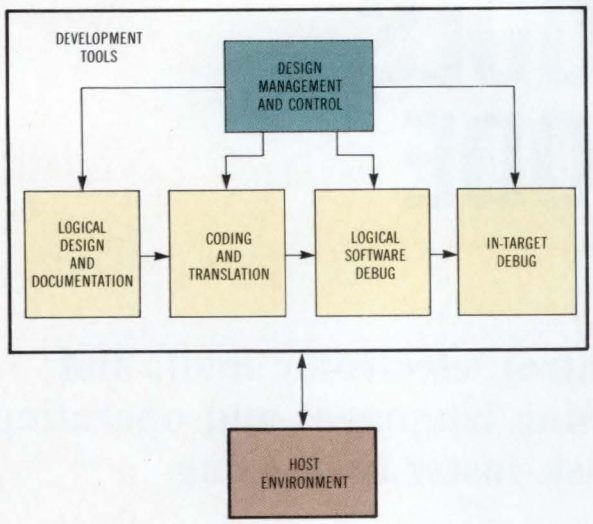
If a project is running behind schedule, adding staff members is not always the best tactic for getting it back on schedule. As the saying goes, adding manpower to a late software project makes it later. Often the best solution is to coordinate programming efforts and project management through an integrated development environment. This type of system stimulates greater efficiency by combining management, programming, and debugging tools in one environment. Productivity increases especially for microprocessor systems with separate target and host development systems. As a result, industries can meet critical delivery schedules without needing additional programmers.

System development is a complex process involving several different stages that continually pass information between each other. The development environment should be more than a collection of assorted tools that are poorly linked. It must efficiently coordinate the diverse stages of development in a single environment, allowing information to flow easily between different tiers of the project.

An efficient development cycle has two parts. Managers must have a clear view of the project from inception through test and implementation. Thus, planning work schedules and anticipating design bottlenecks are easier. Software engineers must share their ideas, designs, and programs—passing information throughout the different development stages.

Yet, in developing products for other target machines, an integrated environment for the host development system alone is not enough. Unless a smooth transition to the final target environment

Dennis Carter is software product marketing manager for Intel (Santa Clara, Calif). He holds an MBA from Harvard University and an MS in electrical engineering from Purdue University.



An integrated development environment must do more than act as a library for development tools. It must ensure that information flows smoothly between components. As organizations shift to new development policies and expand development hardware, the system must be able to migrate smoothly to the new host environment.

is provided, the project will bog down during the critical target system integration and test. The transition from host to target development environments is one of the two major factors affecting the project cost. According to Randall W. Jensen, chief scientist at Hughes Aircraft Co, changing environments can increase costs as much as 122 percent.

Host hardware environments also change as the company expands its development resources. Rather than losing previous investments in tools or training, the company must be able to shift the entire environment smoothly. Some workstations are built to make this transition easy. For example, engineers using Intel's Intellec® Series IV workstation maintain the same fundamental development environment when they move to the NDS-II distributed development environment.

With its multiple stages, system development can turn into a logistical headache for managers and engineers alike. Managers supervising several programming teams, each developing different versions of programs, can easily lose the thread of revisions to the source code. Similarly, programmers can find themselves working at cross-purposes in their attempts to generate and test the most recent versions of code, rather than a hybrid of current and obsolete code versions.

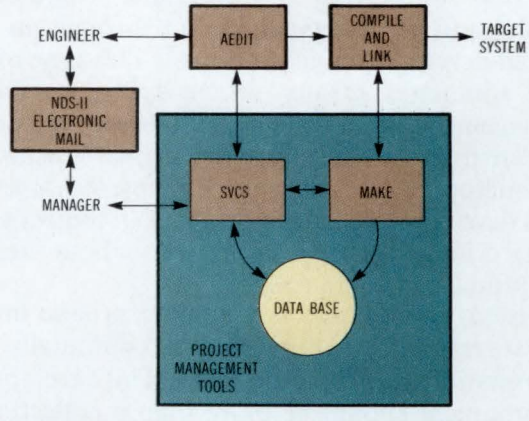
An integrated system can help prevent these problems by combining different tools and making them work well together. For example, Intel's configuration management tools, Source Version Control System (SVCS) and MAKE, manage multiple versions of a program. The tools can automatically combine the most current versions of several modules in larger programs. Similarly, Intel's debugging aids, PSCOPE and Integrated Instrumentation and In-Circuit Emulation (I²ICE™) package, use information implanted by compilers to permit programmers to debug during the integration process at the source level. Such an integrated environment increases efficiency through good allocation of available resources.

Management and control

Modular design helps software engineers break a large complex problem into a set of small simple programs. Unfortunately, a modular design system requires more overhead for managing a large number of modules and different versions of the same module. If the logistics become too troublesome, programmers might even collapse several modules into a single file to save themselves the trouble of manipulating the separate modules. Project management tools can free engineers from the housekeeping chores associated with program development.

Programmers keep track of major changes in their programs by either creating copies of the new version or changing an older version. The result is a series of similar programs that lack proper documentation to indicate the change and reason for the change. SVCS provides an automated approach to this record keeping. It tracks changes to the baseline version of a program, and demands that programmers record their reasons.

When software engineers need a particular version of a file, whether the current or some older copy, SVCS automatically retrieves the correct version from its data base of updates and baseline versions. Similarly, after the programmers have added changes, SVCS records the updates and the reasons for the



Besides controlling changes to the source files in its data base, SVCS helps managers audit source updates. Automatically generating the software for the target system, MAKE reduces generation time by about 50 percent, leaving engineers more time to concentrate on development.

changes, adding as little as a 3 percent overhead. In addition, SVCS helps project managers exercise precise control in large team projects by preventing certain engineers from making changes independently.

While programmers work directly with SVCS to manage different program versions, MAKE works closely with SVCS facilities to generate current versions of systems. While generating large systems from several different modules, programmers often find that one or two modules have been updated since the last compilation. This problem is compounded when modules depend on a series of other submodules. MAKE automates the manual procedures often resorted to by software engineers to track current object modules.

Management tools can free engineers from housekeeping chores.

Using templates that detail the modules' interdependence, MAKE ensures that only current versions of modules are included in the system generation. If it finds that a required object module is obsolete, MAKE will automatically compile the appropriate source module to produce the current version of the object module. Furthermore, if source modules depend on submodules, MAKE will continue searching through its templates to ensure it recompiles modules using the current submodules for these source modules.

MAKE selectively compiles the needed modules. Only if a module or one of its submodules is obsolete does MAKE execute a recompilation. This cuts the inefficient massive compilation procedures commonly used to ensure that object modules are current.

In addition to the project management tools handling version control and system generation, a complete integrated development environment should also facilitate communication among users. Acting as an electronic central distribution center, the NDS-II electronic mail facility maintains mailboxes for individual users and groups of users on the network, and an electronic bulletin board for all users. In addition to supporting document distribution, electronic mail manages a file transfer facility. Team members can transmit both source and object modules to any other user on the network.

Another feature, NDS-II's network resources manager (NRM), provides extensive support for file management and resource sharing. The NRM manages files with a hierarchical structure that arranges files into volumes and multiple subdirectories. The NRM also improves allocation of resources through its distributed job control (DJC) facility. DJC permits users on private workstations to export a batch job to the NRM for remote execution. The NRM then moves the job to a free workstation for execution, returning the completed job status to the user's directory.

Logical design

An integral part of the software development environment and its primary interface with the user is the text editor. Because software engineers typically spend 40-50 percent of their time using a system editor, it is a critical element in software development and can greatly enhance productivity if used well. For example, programmers often need to work simultaneously on two separate files, such as two different source programs or a program and a specification document. Editors such as Intel's AEDIT permit them to edit two files of any size simultaneously and transfer text between them.

AEDIT's ability to store a sequence of edit commands also simplifies the use of edit macros. With AEDIT, programmers build macros simply by typing in their commands. They can reexecute the command series or save it on disk for later use. AEDIT also helps software engineers with structured programming techniques through its automatic text indentation. Furthermore, AEDIT protects programmers' efforts by optionally creating backup copies of files being edited.

Although a text editor serves as the primary interface between the development system and programmer, programming languages serve as the principal interface between design concepts and the target hardware. With the right set of programming languages and support tools, software professionals can develop the optimal solution for a particular situation, without the design bias often seen when designers plan projects with an eye on their eventual implementation.

For example, different programming languages like assembler, PL/M, C, Pascal, and Fortran enjoy certain advantages over each other. Software developers should be able to draw on the most appropriate language to implement the different facets of a design. In order to support this kind of free choice, however, the development environment must be able to coordinate the use of a mix of programming languages, so that programmers can use different languages without concern about how the different modules will eventually be combined.

Like spoken languages, the virtue of programming languages lies in their ability to represent abstract ideas in concrete terms. Just as it may be easier to express a certain idea with a particular spoken language than another, programming languages vary in their ability to represent certain design concepts. For example, software engineers find that Pascal represents structured designs more faithfully than a language like Fortran. Also, languages like PL/M

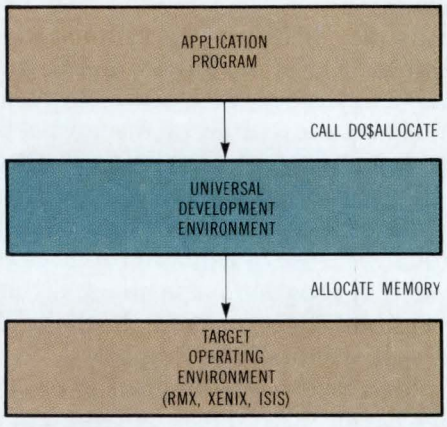
or C, which closely reflect the hardware base of a design; or assembly language, which provides the ultimate visibility into the hardware, are powerful tools for developing realtime embedded systems.

Still, programming languages share another feature with natural languages—varying degrees of popularity. For example, Fortran remains one of the most popular programming languages. Its continued strong momentum translates into a large installed base of software. For managers, this large installed base provides a ready source of existing code. On the other hand, managers must remain ready to incorporate newer languages like Ada into designs without starting from scratch.

In many software development projects, managers often look for a way to juggle several programming languages simultaneously. Software engineers can usually adapt quickly to new programming languages—particularly when they are supported by project management tools. On the other hand, the development environment often acts as a bottleneck in mixing several different languages in the same target system because of its inability to match the varying program and system interfaces of different languages.

The Intel development environment integrates different languages through a common object module format (OMF). A standard OMF works at several levels. During link time, OMF presents a standard method for indicating data type information, which the linker uses to build its memory allocation tables. Furthermore, debuggers exploit OMF's standard arrangement of symbolic information for handling symbolic debugging.

Two other aspects of the standard development environment include the definition of standard conventions for passing parameters between different programs—regardless of their implementation language—and standard interfaces to the operating environment. Besides accounting for critical implementation details another key measure of the effectiveness of a development environment is its support of application level standards like IEEE 754 for floating point operations or IEEE 802 for Ethernet.



Where application standards do not already exist, a development system should follow some baseline. The universal development interface sets a baseline for interactions between application programs and operating software. For example, an application that requires memory uses a UDI call (DQ$ALLOCATE), which is later translated into the appropriate call for the target operating environment.

System-independent interface

For those areas currently without standards, the development environment takes the initiative with a baseline for the operating environment. Here, Intel's universal development interface (UDI) defines a system-independent interface between application programs and the operating environment. Rather than write their programs with system-dependent calls to operating system utilities, software developers use the same UDI call to allocate memory, for example, regardless of the target operating system. During link-time, the linker uses this UDI call to link in the appropriate system utility in RMX, for example. Consequently, programs that use the UDI can be ported between ISIS, RMX, and Microsoft's Xenix simply by loading the modules into the new environment. Thus, if the design calls for a realtime operating environment like RMX, engineers can develop the application under ISIS without fear that their work will be lost when the system is transported to the RMX environment.

For the manager trying to improve productivity, no faster method exists than simply porting existing code to a new environment. Besides IEEE standards, which provide a common application environment, the use of a OMF and UDI provide a clear migration path between different operating environments.

In the kind of cross-development environments commonly used for creating microprocessor-based products, engineers work most effectively if they are able to split debugging into two phases. In the first phase, debugging occurs in parallel for the target hardware system and for the software. Here, engineers use the host environment to debug the basic logic of the software system. Once they are satisfied both with the logic of the software and with the operation of the hardware, the engineers then load the software into the target system for the second phase—integration and test.

This in-target phase is the critical step where hardware and software are finally integrated as a total system. As noted earlier, differences between the host and target environments can more than double costs. Consequently, a key feature of an integrated environment is a common debug interface between host and target.

Intel's PSCOPE debugger permits programmers to check out programs at the source level both during logic debug and during in-target test. Because

Debugger Command Language

Command	Action
Go/Listed/Pstep	Control program execution
Define Display Modify Remove	Manipulate debugger or program objects
Call/Return	Execute debugger procedures
Call/Return	Execute debugger procedures
Write/CI	Console input/output
Do/End	Define command blocks
Repeat/Count	Repetition of commands or command blocks
If/Then/Else	Conditional execution of commands or blocks
Input/Put/Append	Save/restore to and from disk

PSCOPE shows up again as one of the three major components of the I²ICE system, software engineers are assured of a smooth transition between host and target. Along with PSCOPE, the I²ICE and the logic timing analyzer (LTA) give developers a full view simultaneously into the hardware and software components of their systems. Without this kind of coordinated approach to system integration and test, developers can never deal with the hardware and software as an integrated system, but are forced to switch continually between hardware testing and software debugging.

Supporting system integration at the most fundamental level, in-circuit emulation provides a transparent, full speed emulation of the iAPX 86 and iAPX 286 families of processors. Besides handling multiple level breakpoints and traces in single microprocessors, I²ICE extends its support to multiprocessor environments. Developers can emulate a system of up to four microprocessors and examine complex processor interactions like synchronization. For example, I²ICE lets engineers define events like breaks and traces conditionally, so that a microprocessor will break when another defined event occurs in a different microprocessor.

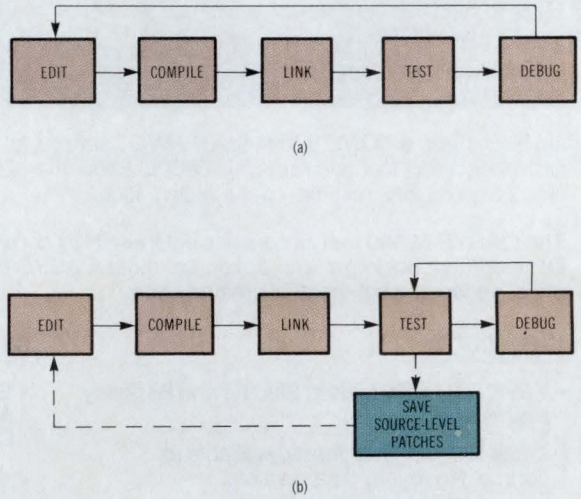
While I²ICE and PSCOPE provide the fundamental support for a system's underlying hardware and software, the LTA also serves as a key element of the system's integrated package. Displaying 16 channels of logic and timing information, the LTA helps isolate critical state and timing problems. In order to speed the analysis process, this menu-oriented system also permits engineers to save debugging setups and waveforms on disk.

A key advantage of an integrated environment is its ability to present information, through a consistent command language, in a familiar form. With I²ICE, this feature extends to logic and timing analysis. Rather than present a morass of digits, the LTA displays most information in easy to understand waveform diagrams.

Source-level debugging

Just as the LTA has moved system integration and test above the bit level, PSCOPE shortens software debugging by permitting engineers to test programs using their own symbols, rather than machine code. With the traditional machine code debugger, if they wanted to patch a section of machine code, programmers would spend hours converting machine code between different formats, like binary and hex, and calculating the machine code equivalents of assembler instructions. Even somewhat more sophisticated debuggers that disassemble machine code are little help in retaining the sense of a program as expressed through its use of symbols.

Instead, even though it helps software engineers deal with machine code when necessary, PSCOPE can handle debugging at the level of the original source code. Consequently, programmers can set an unlimited number of breakpoints by statement number, step through a single source statement at a time, and trace execution by statement number,



In the past, engineers have needed to iterate through a lengthy development cycle in order to debug source code in the target system (a). On the other hand, PSCOPE lets engineers use source-level code to debug and patch the target system and continue debugging. Then, after many bugs are found, PSCOPE saves the source-level patches on disk for later addition to the original source files (b).

procedure name, or label (regardless of whether they are working with the host or target system).

From the user's point of view, the utility of PSCOPE lies in its built-in, CRT-oriented editor and in its command language that resembles a high level structured programming language. Using PSCOPE's editor, engineers can write extensive procedures in the command language for testing code and even for patching existing code with new or revised source statements.

The many advantages of an integrated environment include source-level debugging tools, such as PSCOPE.

PSCOPE's ability to handle source-level patches avoids the conventional development scenario where software developers go through a continual cycle of edit-compile-link-test-debug. Source-level patching short-circuits this loop; programmers can remain in the debug phase—patching at the source-level and even saving the source-level patch on disk for later incorporation into the original source-code files maintained under SVCS.

The advantages of an integrated environment show up here dramatically. During compilation, the compiler places symbolic information associated with a program into the object modules it generates. In turn, the linker carries this information along into the runtime image. Both PSCOPE and I²ICE draw on this symbolic information for their source-level debugging. Consequently, during system debugging, developers see familiar procedure and data names, rather than a confusing series of machine codes or disassembled mnemonics. Furthermore, because it maintains this symbolic information in a virtual table, PSCOPE is able to handle arbitrarily long symbol tables—it just brings a new page of symbols from disk, if necessary.

As a result of its ability to coordinate its tools for the various stages of development, the Intel development environment lets system engineers concentrate on product development, rather than on administrative chores. For the development manager, this translates into on-time product delivery, without the costs of additional resources.

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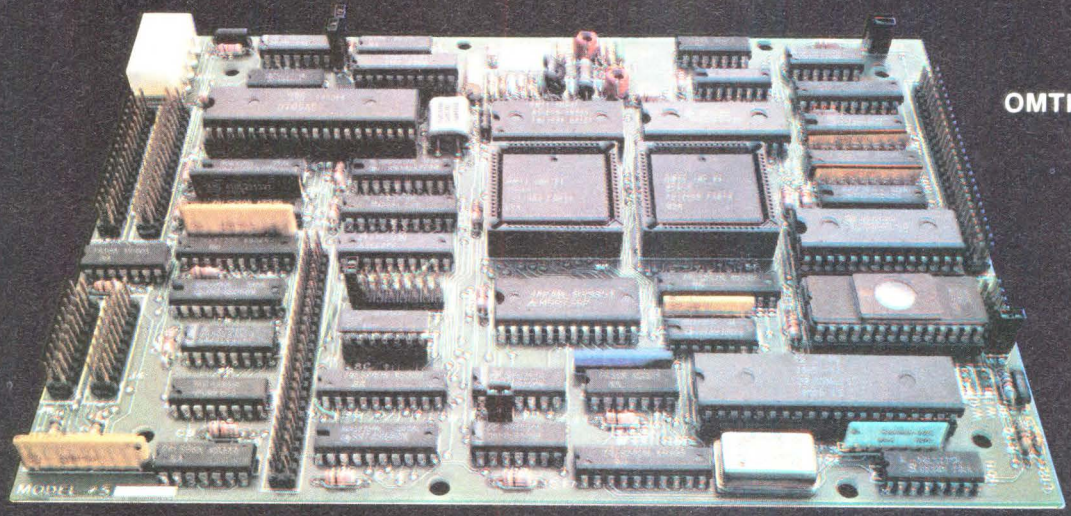

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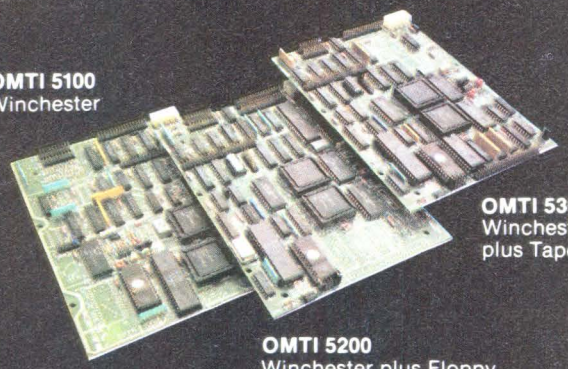

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CIRCLE 81

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CIRCLE 82

MIXING DATA PATHS EXPANDS OPTIONS IN SYSTEM DESIGN

Chip designers are creating powerful CPUs and peripherals with 16- and 32-bit parts. Mixing these with 8-bit parts overcomes limitations imposed by established designs, incomplete families, and software incompatibility.

by Mark S. Young and James R. Williamson

Integrating 16- and 32-bit peripherals and CPUs into 8-bit designs, at the simplest level, means separating the control and data paths from new peripherals and the systems. Mixing different data path widths and control protocols, however, makes possible major improvements in function, performance, and cost.

The price/performance curve of VLSI chips, for example, allows designers to obtain more and better functions for the same amount of money every year. Alternately, the functionality of a device can remain constant while the price falls.

Moreover, these new devices with wider data paths can extend the life of older designs. For example, many of the most popular personal computers today use the 8088 microprocessor and, therefore, are constrained to an 8-bit data path. Designers of add-on accessories for these personal computers prefer the newer 16-bit peripherals. These peripherals will let users preserve their software investments, improve performance, and stave off obsolescence.

Mixing different data path widths can also enhance new designs. For example, it is less expensive to use an 8-bit bus in a new design because the memory requirements are generally cheaper. Only half as many dynamic RAMs are necessary for the same number of kilobytes of memory. In addition, an 8-bit bus needs much less control and support logic. Designers can mix smaller data path peripherals with wider data path CPUs. This allows them to introduce systems based on the newer, more powerful 32-bit CPUs even before 32-bit peripherals are available.

Designers can use this mixing method to obtain wider data paths from existing designs until a new system design is warranted. They can also use parts in unexpected applications. For example, cost-conscious terminal manufacturers might want to use the Am8052/8152A chip set (the 8052 is an advanced CRT controller and the 8152A is a video system controller) in new terminals based on the relatively inexpensive 8051 microprocessor. Mixing the 8-bit, single-chip microprocessor with the 16-bit CRT controller allows designers to maximize the cost/performance ratio of the terminal.

Mixed data path widths can improve bus utilization as well. A 16-bit peripheral in a 32-bit system only occupies half the data bus for data transfers. If the designer mixes the data paths correctly, however, the 16-bit peripheral could transfer data as

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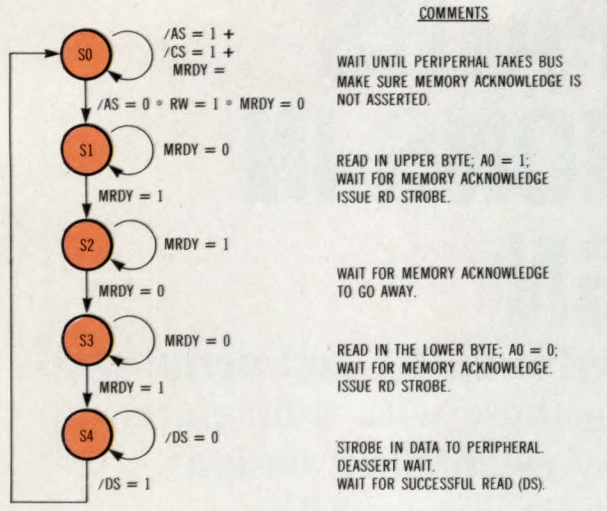


The state flow control diagram for a bus master read operation illustrates the control sequence employed by the 8/16-bit bus control logic.

32-bit chunks and improve bus efficiency by 100 percent for that peripheral.

Two central concerns stem from mixing devices that communicate over different-sized buses. The first problem results when two devices communicate on a "common" data bus. Consider, for example, a 32-bit system utilizing 8- and 16-bit peripherals. Overcoming the mismatched data paths requires some form of controlled multiplexing/demultiplexing of the different data paths. In addition, extra control signals for partitioning the 32-bit word into 8-, 16-, and 32-bit chunks may be required.

Many 16-bit CPU-based systems that use 8-bit peripherals normally use just the lower 8 bits of the data bus to transfer data to and from the peripheral. This method does not work in systems using 16-bit peripherals and 8-bit CPUs, however, and it tends to break down in systems with 8-bit peripherals having bus master capability.

A bus multiplexing method involves multiple transfers when taking data from or adding data to a mismatched data bus. For example, before a 16-bit peripheral can transfer data over an 8-bit bus, the 16-bit data must be divided into two 8-bit chunks. It is then transferred sequentially. First, the lower 8 bits are transferred out on the bus. Then, in the next transfer cycle, the upper 8 bits of the 16-bit word are sent out. The major difference in the opposite case—a bus read operation from an 8-bit bus to a 16-bit device—is that the first byte read from the system must be latched. Once the second byte has been fetched, the 16-bit peripheral reads in the assembled 16-bit (2-byte) word. Additional provisions may be needed when the 16-bit peripheral only wants to access a single byte.

The other major problem in mixed data path transfers is the actual data read/write operation. The nature of the multiple transfer forces designers to guarantee that the stretched transfer will occur and that it will not be interrupted. Two aspects of stretching the transfer cycle from or to the peripheral illustrate the complexity of this problem.

The first case, when the peripheral is the bus master, is the simplest. A 16-bit peripheral holds its data available for what normally would be two complete bus transfer cycles. This function can be performed when the transfer acknowledge signal to the peripheral is delayed. If the data was latched instead of holding the peripheral in a multiple word transfer, however, the device could try to send the next 16-bit data word and its "new" address. The procedure of latching the data and releasing the peripheral should not be used, therefore, because it may interfere with the addressing of the remaining (pending) 8-bit transfer.

Whenever a device acts as a bus slave to a CPU that cannot access the device's natural word width in a single operation, a different constraint appears. The sequence must be set up so the peripheral cannot obtain the bus while the CPU is in the middle of a slave read/write operation. In a typical system, the CPU is the last device in the interrupt queue. It is possible for the peripheral to become bus master between the first and second read operations and invalidate the results of the first read operation in a realtime system. This is because an 8-bit CPU would have to perform two consecutive read operations to examine a 16-bit peripheral control register.

This function can be handled two different ways. If the CPU has a bus lock instruction, as in the iAPX family of CPUs, the programmer must use one of these instructions before the CPU accesses the peripheral. Alternately, the CPU needs to disable the arbitration logic while it is performing the uninterruptible access with the 16-bit peripheral.

Crucial cycle

The uninterruptible word transfer cycle is crucial for maintaining the integrity of the data transferred. When either the CPU or a peripheral on the bus makes an access using the 8/16-bit control logic, it must complete the larger device's word access before relinquishing the bus. If this requirement is not met, a transfer's integrity can be violated easily by some other device. This interrupts the transfer, and corrupts or aborts the multiplexing sequence.

To illustrate this point, consider a system consisting of an 8-bit CPU and several 8- and 16-bit peripherals. Assume one of the peripherals is executing a block transfer of 16-bit data onto the 8-bit bus. If the CPU interrupted the transfer in order to poll the peripheral during a half-word transfer, two undesirable events would occur. Either the multiplexing

sequence would be damaged irreparably when the CPU polled the peripheral, or the CPU would read garbage from the peripheral.

Designing the control interface to allow mixing of 8- and 16-bit peripherals requires attention to the data and control flow. During a write operation, the data is written out sequentially: the lower byte comes before the upper byte (or vice versa). The read operation differs only because the data bus is 8 bits and because it forgets the last byte transferred; it knows the current byte only. Hence, the interface requires that one of the bytes be latched until the full 16-bit word has been assembled.

The slave mode of operation works almost the same as the peripheral bus master mode. The single exception is the slave write operation. When the interface is defined, the designer must make a conscious choice about which byte (upper or lower) to latch during peripheral read operations (or conversely, slave peripheral write operations). Once this decision has been made, the CPU must always access the latched data byte first (during a slave write) and then access the non-latched byte to complete the transfer. This restriction is minor, requiring no extra software overhead. It could affect the ease of the programmer's coding if not handled properly, however. For example, if the programmer used a compiler to generate the software for the system, extra care may be necessary to ensure the compiler generates the correct addressing sequence.

An alternative solution would be to latch both the upper and lower data bytes. In this case, however, the cost of the interface would increase, as would the complexity, with no appreciable gain. The control flow in these designs derives from two different sources: the state control flow itself and the 16-bit peripheral interfacing with the 8-bit bus. A state diagram can be used to specify how uninterrupted word transfers will occur and how the upper and lower byte address is generated.

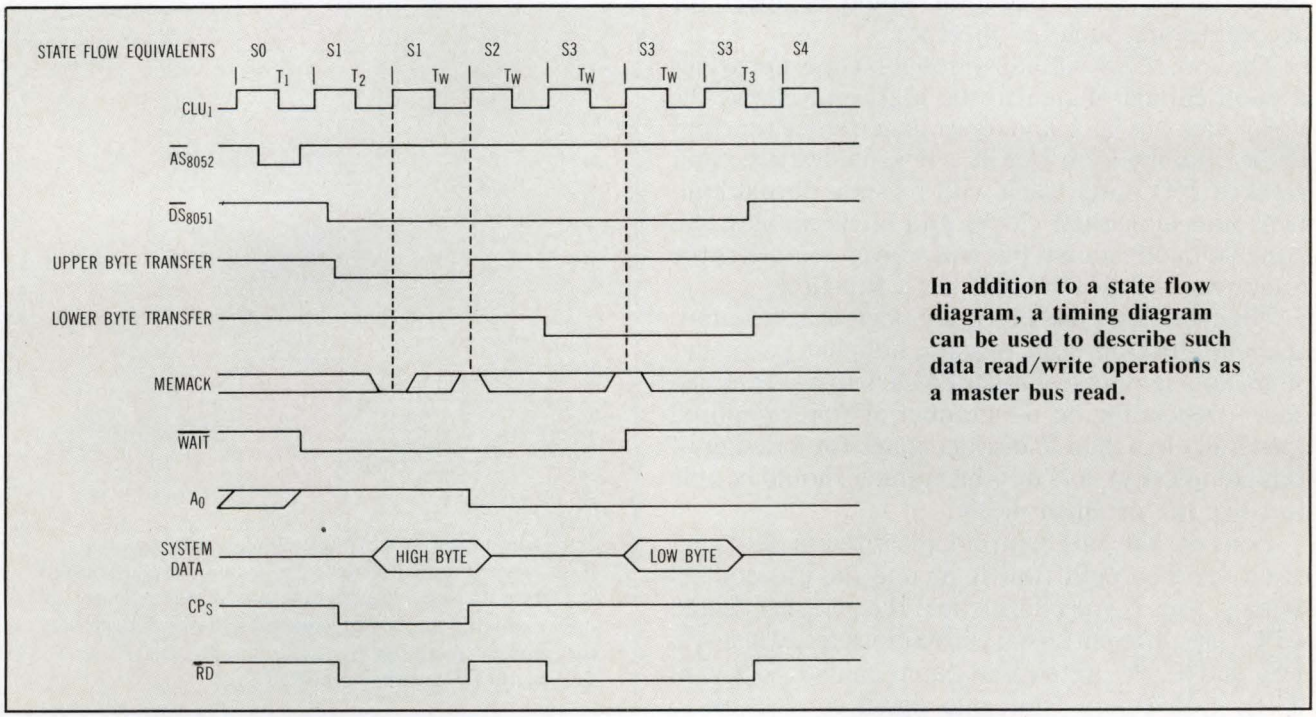
In addition, the specific bus timing of the peripheral and the data bus must be examined to quantify the state control flow. These timing specifics also provide information on data latching, read/write control strobes, and addressing to and from the peripheral. The state control flow is divided into four operations: bus master read, bus master write, slave read, and slave write.

For a bus master read/write operation from a 16-bit peripheral device operating on an 8-bit bus, four control signals must be generated by the 8/16-bit control unit: address bit 0 (A0), peripheral hold ($\overline{WAIT}$), bus read ($\overline{RD}$), and bus write ($\overline{WR}$). The A0 line is generated by the 8/16-bit control logic to indicate which byte is to be transferred in bus master modes only. Otherwise, the A0 generated by the system is used to indicate which byte is being accessed. The $\overline{WAIT}$ line holds up the peripheral during transfers. The $\overline{RD}$ and $\overline{WR}$ lines are required to indicate successive transfer cycles on the bus.

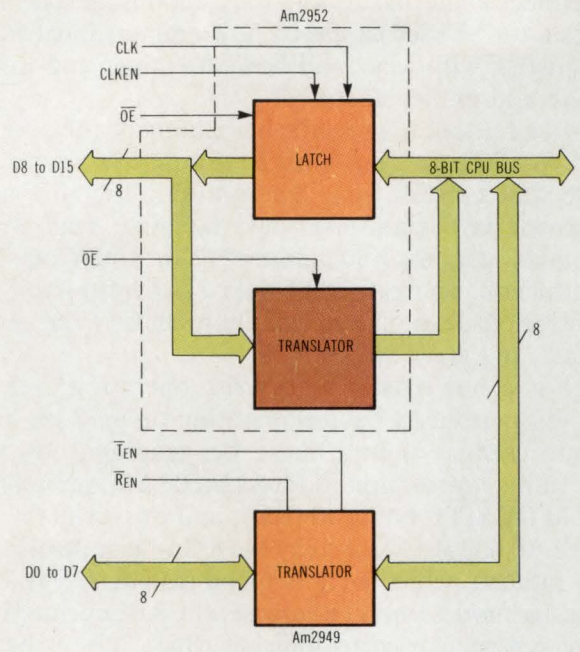
Hidden transfers

The peripheral's signals will only strobe active once because it does not know that two transfers are being executed. The slave transfer flows are almost identical, except the CPU is generating the bus signals and the transfer directions are reversed (ie, a bus write goes into the peripheral).

For this 16- to 8-bit data flow example, the data on the upper byte only needs to be latched when data



In addition to a state flow diagram, a timing diagram can be used to describe such data read/write operations as a master bus read.



The 16- to 32-bit conversation logic diagram indicates the complexity of bus and funnel logic control. It must convert between different signal conventions and polarities as well as generate extra functions and bus arbitration control signals.

is being read (as bus master) or written (as a bus slave). An interface to handle this operation needs to latch data coming from the 8-bit data bus into the peripheral, it also needs to act as transceiver when the peripheral is sending data out to the system. A device with a clocked, tri-state output that has an 8-bit wide latch in one direction and a tri-state transceiver in the other direction would be ideal for accomplishing such an interface.

The Am2952 8-bit bidirectional I/O port provides a good enough match to the logic and allows the upper data bus latch and upper data transceiver chips to be combined on one IC. It provides two 8-bit clocked I/O ports, each with tri-state output controls and individual clocks and latch enables. An Am2949 bidirectional bus transceiver completes the logic required for the data path function.

The state flow control requires logic that can move sequentially from state to state, hold in a particular state, and be reset or initialized back to a predefined state. Depending on the number of states required (generally less than 16 distinct states for a design of this complexity), a 3- or 4-bit counter should be able to solve the problem nicely.

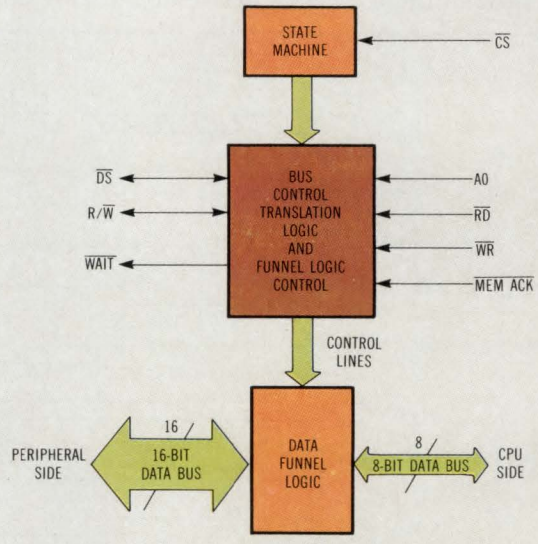
Considerable bus control logic is required to generate the data path flow logic and the bus control signals. This is especially true if the peripherals and CPUs use different signal conventions (eg, when $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ use address latch enable, $\overline{RD}$, and $\overline{WR}$). Conversion from one signal convention to another, changes in signal polarity, and provision for extra functions (such as generating A0) require a lot of logic synthesis ability. If the peripheral has bus master capability, such additional information as bus arbitration controls must be fed into the next state determination logic in order to decide what control sequence to follow.

Customized interface minimizes cost

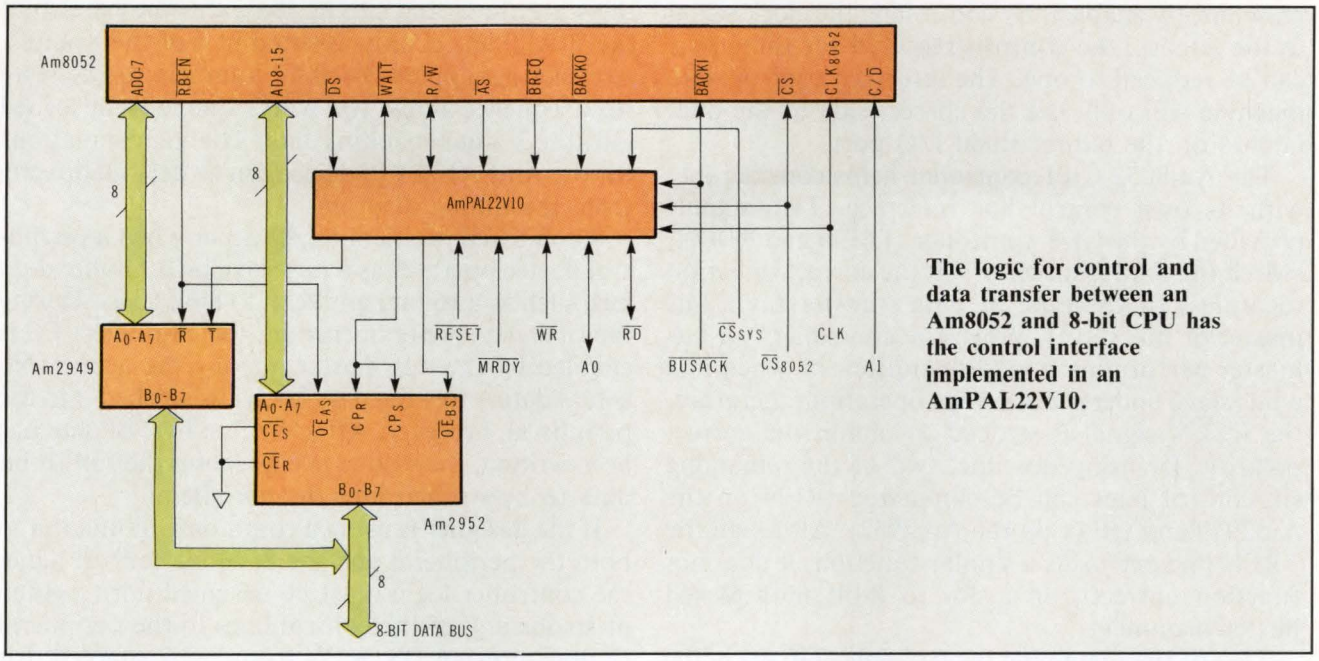
An 8/16-bit control interface between the Am8052 CRT controller and an 8-bit CPU provides a good example of how customizing a general interface can reduce costs. (The CRT controller is designed with a 16-bit data interface.) The onboard DMA unit fetches data from system memory and the CPU polls the CRT controller's internal status and control registers. Because the CRT controller does not modify system memory, however, a bus master write operation is unnecessary. Thus, there is no reason to generate a system write control signal (WR).

In addition, the control and display information must be aligned on word boundaries. This requirement relieves the 8/16-bit control logic from funneling the bytes and performing odd/even byte transfers. It also saves control inputs from the CRT controller because all transfers are words; that is, no need exists for upper and lower data strobes or byte high enable inputs.

The bus master read operations are standard 16-bit data transfers divided into two 8-bit transfers. The CPU's slave accesses are either pointer writes (to select the desired control/status register) or 16-bit data read/write operations. (Pointer write operations



The state machine and the bus and latch controls have to be coupled in order to transfer data between the 8- and 16-bit buses. This generalized machine is designed with the assumption that the peripheral has bus master capability. If this is not the case, the design can be greatly simplified.



The logic for control and data transfer between an Am8052 and 8-bit CPU has the control interface implemented in an AmPAL22V10.

are actually 8-bit operations because only the lower 8 bits of the data form the register address.) The bus master read operation can be represented by a state flow diagram or a timing diagram. Conceptually, state flow diagrams are easier to understand, but timing diagrams usually convey more information. Other state flow diagrams can be derived directly from the timing diagrams of the CRT controller to 8-bit interface.

Simplifications allow synthesis on one device

Two special conditions must be met in the state machine implemented in the 8/16 interface. First, before a new transfer cycle is attempted (when the state machine is waiting in the initial state, S0), memory acknowledge ($\overline{MRDY}$) must be inactive. This prevents interference from the last transfer.

The second special condition occurs when the CRT controller asserts the R/$\overline{W}$ line to indicate a write operation. Although the CRT controller does not write data into system memory, when it updates the upper 8 bits of the 24-bit address latch the R/$\overline{W}$ line indicates a write operation (in conjunction with $\overline{AS}$). The CRT controller is not actually performing a system data write, only an address latch update. The state machine, therefore, must not start a bus sequence if the R/$\overline{W}$ line is held active low by the CRT controller during a bus master operation.

These simplifications in design allow the CRT controller to 8-bit CPU control interface to be synthesized in a single AmPAL22V10 programmable logic array device. In addition, the bus control signals are converted from $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ to $\overline{RD}$ and $\overline{WR}$. The minimum CRT controller and bus control signals that must be generated are $\overline{RD}$, A0, $\overline{DS}$, and R/$\overline{W}$. Although the CRT controller uses $\overline{DS}$ and R/$\overline{W}$ as inputs during a bus master operation, the PAL device must convert the CPU $\overline{RD}$ and $\overline{WR}$ signals to $\overline{DS}$ and t/$\overline{W}$ for slave I/O operations.

The signals A0 and RD are generated by the control logic when the CRT controller is performing a read access to system. The $\overline{WAIT}$ (or not READY) signal to the CRT controller must also be generated by the control logic. The data flow controls require six additional controls to load and strobe the latch, and to enable transceivers to pass data to and from the 8-bit bus. Theoretically, 4 more bits (outputs) are required to represent all the control states needed to manipulate the 8/16-bit control logic. This means the design appears to need 14 output logic units in a PAL device to perform the required task.

Reducing the 14 output cells to the 10 cells available in the PAL device requires a closer look at the timing and output switching functions. The A0 and $\overline{RD}$ control lines are in effect part of the system bus control and, therefore, cannot be multiplexed easily. The $\overline{DS}$ and R/$\overline{W}$ lines to the CRT controller are also fixed because they must be valid throughout the entire transfer cycle as well.

This leaves 6 of the 10 output logic cells of the PAL device to represent the remaining 10 identified control lines. This method of minimization involves careful state synthesis, analysis of the signal switching functions during the transfers, and utilization of several control pins on the CRT controller. By using the $\overline{BREQ}$, $\overline{BACKI}$, $\overline{BACKO}$, $\overline{CS}$, and C/$\overline{D}$ inputs to the PAL device, we can reduce the number of unique states required to 8 instead of 15. This reduces the number of logic cells required for the state machine from 4 to 3 bits.

At this stage, the design requires seven control signals to manipulate the data transfer registers and $\overline{WAIT}$ line. The two latch enables ($\overline{CE_S}$ and $\overline{CD_R}$) on the Am2952 bidirectional I/O port can be

permanently enabled. By controlling the clock signal to the latches, the controls required for three pins can be reduced to one. The interface control state machine will only use the correct side of the dual latches on the bidirectional I/O port.

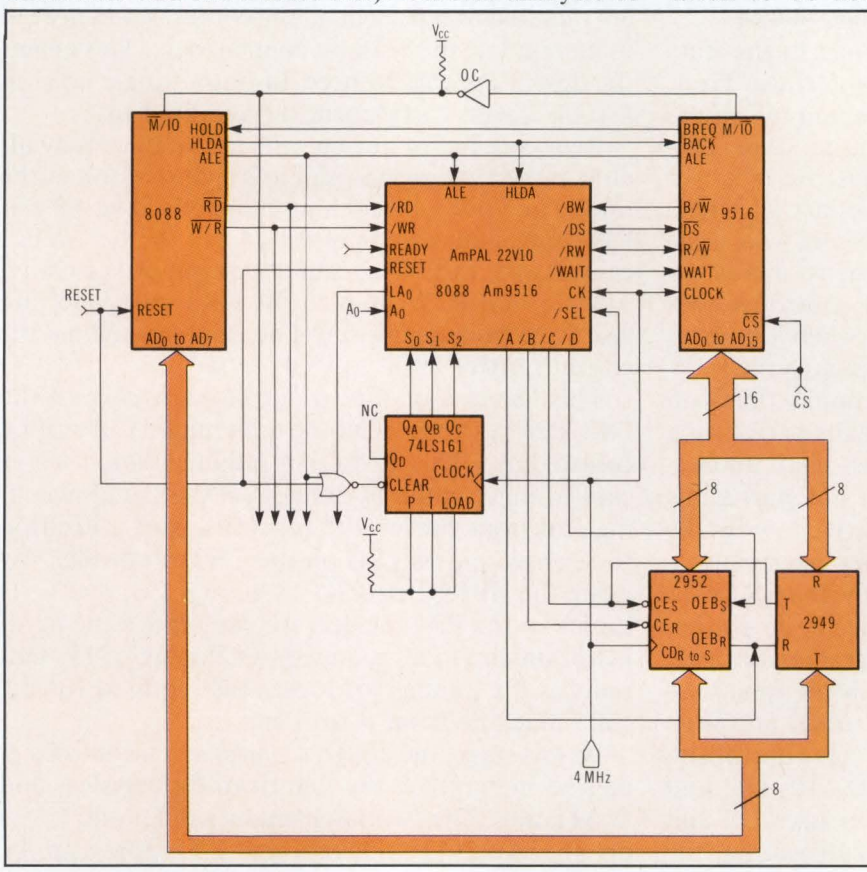
The Am8052 CRT controller helps considerably with its own control bus interface. Two signals provided by the CRT controller, $\overline{\text{TBEN}}$ and $\overline{\text{RBEN}}$, switch the data transceivers in the correct direction regardless of the type of data transfer (as a bus master or bus slave). When the controller is a bus master performing a read operation, or when it is a bus slave undergoing a write operation, therefore, the $\overline{\text{RBEN}}$ signal is strobed to obtain the correct polarity. By using this line, two of the remaining six control lines can be eliminated ($\overline{\text{REN}}$ on the Am2949 and $\overline{\text{OE}}_{\text{AS}}$ on the Am2952). Although the $\overline{\text{TBEN}}$ line performs a similar function, it does not function correctly in a 16- to 8-bit multiplexed bus environment.

Two of the remaining control lines ($\overline{\text{OE}}_{\text{AS}}$ on the Am2952 and 10 on the bidirectional bus transceiver) must be generated by individual cells in the PAL device. The two clock enables on the Am2952 are permanently enabled. The two Am2952 clocks are tied together to minimize the amount of logic required in the PAL device used to generate clock strobes to the latches.

This leaves the design with three logic cells and four output functions (the $\overline{\text{WAIT}}$ line to the CRT controller and the 3 state bits). Careful analysis of the state flows and timing diagrams indicates that the $\overline{\text{WAIT}}$ line is only asserted in 4 of the 8 states. A clever assignment of state numbers to the state flow sequence allows the $\overline{\text{WAIT}}$ line to be absorbed into the 3 state encoding bits. The logic equations for the AmPAL22V10 device can be derived directly from the timing diagrams.

An unusual problem might occur when a peripheral device operates as a bus slave on a smaller data bus, such as a 16-bit peripheral to 8-bit CPU. During the first slave write operation, the chip select $\overline{\text{CS}}$ is enabled by the bus master making the access. No actual data—just the data latch—is strobed into the peripheral, however. After the first byte of data has been written, the second access causes the full 16-bit data to be strobed into the peripheral.

If the designer is using a common $\overline{\text{CS}}$ function to both the peripheral and the 8/16-bit control logic, the controller logic must be designed not to glitch or strobe any of the control lines to the peripheral (it must prevent $\overline{\text{DS}}$, R/$\overline{\text{W}}$ from being enabled, for example). For some peripheral devices, glitches on the control lines might cause the register to be written accidentally onto a register that will be overwritten in the next write cycle anyway. With other peripherals this might be a catastrophic event. Many devices acting as bus slaves have write recovery time requirements (ie, a certain minimum interval between consecutive write operations). Glitches on the control lines might force the next (and final) write operation to be delayed—or cause a violation of the



The data bus and control interface between an 8-bit 8088 CPU and a 16-bit Am9516 DMA controller uses an AmPAL22V10 for control, and a 74LS161 for state sequencing along with a bidirectional I/O port and transceiver.

device specifications. Glitches might evade any special addressing/register accessing scheme used in the peripheral. This might occur, for example, if the slave device requires the user to write the address of the register that was accessed immediately before the register was written. In this case, glitches or useless control strobes could wreck the sequence.

The problem can also be solved by using two lines. In this solution, one of the lines would go to the peripheral device and the other would connect to the 8/16-bit controller. The chip select to the peripheral is activated each time a slave read occurs (for both upper and lower byte accesses), or when a slave write operation occurs and the unlatched 8-bit data is being written. The chip select function to the 8/16-bit controller is chosen each time the peripheral is selected normally (for slave read/writes on both upper and lower 8-bit data transfers). This problem is bypassed completely when two separate chip select functions are used: one for loading up the Am2952 latch during a slave write/read and one to strobe the Am8052 controller into action when it is needed by the 8-bit CPU.

Bus conversion maximizes flexibility

A data bus and control interface to an 8088 8-bit microprocessor and Am9516 16-bit DMA controller can be created using four devices: an AmPAL22V10 for the control block, a 74LS161 counter for the state sequencer, an Am2952 bidirectional I/O port, and an Am2949 bidirectional transceiver.

This design incorporates certain simplifications. The DMA controller requires word accesses only during command chaining and for slave register accesses. The 8/16-bit data transfer interface for bus master operations (ie, DMA data transfer functions) is handled automatically as a programmable option. During slave write operations, the first byte output to the DMA controller must have an odd address and the following second byte an even address. Conversely, during a slave read cycle, the first byte read from the DMA controller must be at an even address and the second at the next higher odd address.

Furthermore, for bus master operations, the system must use the latched address line A0 (LA0) from the AmPAL22V10 as its sole A0. Because the logic is already available, the system does not have to provide this function. LA0 now becomes the system address bit 0 with full 24-mA drive capability.

Deciding on a means for controlling the funneling of the data stream—that is, transforming 16-bit data into 8-bit data and vice versa—was the first step in deriving this example. As mentioned earlier, simply dividing each 16-bit access into two 8-bit data transfer cycles presents one way of doing this. On outgoing accesses (16-bit path from the DMA controller) during the first cycle, the upper half of the 16-bit path is latched while the lower half passes through

```
PIN
        CK      = 1     /RD     = 23
        S[0:2]  = 2:4   /WR     = 22
        A0      = 5     LA0     = 21
        /SEL    = 6     /DS     = 20
        ALE     = 7     /RW     = 19
        HLDA    = 8     /WAIT   = 18
        /BW     = 9     /A      = 17
        READY   = 10    /B      = 16
        RESET   = 11    /C      = 15
                        /D      = 14;
BEGIN
        IF (RESET) THEN ARESET( );
This section defines the wiggles when the Am9516 is bus master
        IF    (HLDA) THEN ENABLE( );
        IF    (/S[2] * HLDA) THEN BEGIN
              IF (S[1] * /S[0]) THEN
                    LA0   = /CK * BW + /BW * A0 *
                            ALE + / BW * LA0 * /ALE ;
              ELSE
                    LA0   = BW + /BW * A0 *
                            ALE + /BW * LA0 * /ALE  ;
        END;
        IF    (HLDA) THEN
              (CASE) (S[2:0])
                    BEGIN
                      1) BEGIN
                      RD   = /RW * DS                ;
                      A    = /BW * /RW * /CK         ;
                      WR   = /BW * RW * DS           ;
                      C    = /BW * RW                ;
                      WAIT = 1                       ;
                    END;
                      2) BEGIN
                      RD   = /RW * DS                ;
                      B    = BW                      ;
                      A    = /BW * /RW               ;
                      WR   = /BW * RW * DS           ;
                      C    = /BW * RW
                      WAIT = /BW
                    END;
                      3) BEGIN
                      RD   = /RW * DS * B            ;
                      B    = BW * CK                 ;
                      A    = /BW * RD                ;
                      WR   = /BW * RW * DS           ;
                      C    = /BW * RW                ;
                      WAIT = BW                      ;
                    END;
                      5) BEGIN
                      RD   = /RW * DS                ;
                      A    = /BW * /CK               ;
                      WAIT = BW                      ;
                    END;
                      6) BEGIN
                      RD   = /RW * DS                ;
                      A    = /BW                     ;
                    END;
                      7) BEGIN
                      RD   = /RW * DS                ;
                      A    = /RD                     ;
                    END;
        END;
This section defines the wiggels when the 8088 is bus master
        BEGIN
        LA0= A0 * ALE * SEL + LA0 * /ALE * SEL
        B  = LA0 * WR * SEL
        A  = /LA0 * WR * SEL
        DS = A + /LA0 * RD * SEL
        C  = /LA0 * RD * SEL
        D  = LA0 * RD * SEL
        END;
END.
```

This PLPL file implements an interface between the 8-bit 8088 and the 16-bit Am9516.

Programming the PAL and the counter

In writing the Programming Language for Programmable Logic (PLPL) file to control the operation of the AmPAL22V10 and the 74LS161 counter, the inputs to the PAL device from the counter are assigned S0, S1, and S2, respectively. Then, it is possible to apply a "sculptured design" technique to the entire timing diagram (see figure in Panel, "A matter of timing") by using the Case statement from PLPL. By assigning combinatorial equations to only one binary partition or column at a time (Case), the designer can ignore all other aspects of the design for the time being and generate simple equations directly from the timing waveforms.

During clock time T1 of the Am9516's word read cycle the state of the 74LS161 (S0, S1, S2) is cleared to 000 by the assertion of address latch enable (ALE). LA0 is the only output control signal from the CRT controller asserted during this period. This signal is handled as a special case, however. During time T2 of the DMA controller's word read cycle, the $\overline{RD}$ and $\overline{WAIT}$ outputs from the CRT controller must be asserted. This time partition corresponds to the state inputs S2, S1, S0 = 001. Therefore, the first Case equations are

```
CASE     (S[2:0])
  BEGIN
  1)  BEGIN
        RD = /RW*DS  ; Transform Control
                     ; Signals /RW and DS
                     ; into Intel /RD

        WAIT = 1     ; Assert     Wait
                     ; unconditionally

  END;
```

During time T2 of the DMA controller's byte read cycle, $\overline{A}$ is the only additional output not already accounted for in the Case statement. This signal allows a byte of data to flow through the bidirectional bus transceiver into the DMA controller during byte read operations. Some additional constraints are placed on this signal, however: it must only be asserted in time T2 on byte read operations (the B/W input) and it must be delayed by a half clock period from the rising edge of T2 ($\overline{CK}$ signal). Thus the Case statement becomes

```
CASE   (S[2:0])
  BEGIN
  1)  BEGIN
        RD = /RW*DS          ;
        A = /BW*/RW*/CK      ; enable the
                             ; receiver

        WAIT = 1

  END;
```

Finally, by examining the last time T2 elements ($\overline{WR}$ and C) during the DMA controller's byte write cycle, the remaining terms in Case 1 are derived. With the exception of LA0, the remaining equations were developed in the same fashion. Clearly, this "sculptured" technique is a very simple and methodical means for arriving at the Boolean requirements for a logic block.

As the PLPL listing shows, the signal LA0 was handled slightly differently from the previously discussed method. The number of product terms generated via the Case statement made this approach necessary. The number exceeded the upper limit (16 terms) for a programmable logic array. As a practical matter, therefore, it was necessary to optimize this signal manually. However, it should be noted that this step will not be necessary once the fully optimized version of PLPL becomes available.

a tri-state buffer onto the 8-bit bus. During the second cycle, the tri-state buffer is turned off and the previously latched half of the data is driven onto the bus. On incoming accesses (8-bit path to 16-bit path), the process is reversed.

The control mechanisms that perform this cycling depend on the WAIT and R/W signals passing to and from the DMA controller, and on the ability to enable or disable the latches and transceivers selectively. The Am2952 bidirectional I/O port was chosen because of its dual registers and its flexible control. The AmPAL22V10 device was chosen to match the required number of control pins and functions. Since the complexity of this design requires the use of all of the PAL's I/O pins for control functions, however, it was necessary to use a 74LS161 counter to provide the state sequencer function.

Programming with PLPL

It has long been the logic designer's "art" to merge the often very different concepts and notations of timing information with Boolean logic. Yet, the evolution of a syntax to fully express this art has taken a long time. AMD recently developed such a language for programming the AmPAL22V10, however.

"Programming Language for Programmable Logic," or PLPL, allows the designer to specify a design using multiple input formats. This specification flexibility supports the variety of design approaches necessary to express different design problems efficiently. These formats range from simple sum-of-products Boolean equations to high level constructs. PLPL also supports the input specifications for many types of AND/OR based devices, including all of the current AMD programmable logic array and PROM devices.

PLPL is block structured, and includes the high level language constructs If-Then-Else, Case, and For; all familiar to many programmers of the C and Pascal languages. Macros, functions, constants, and variables may also be used in PLPL. The language also facilitates use, clarity, and self-documentation.

Such current programmable logic technology and associated programming languages as PLPL allow

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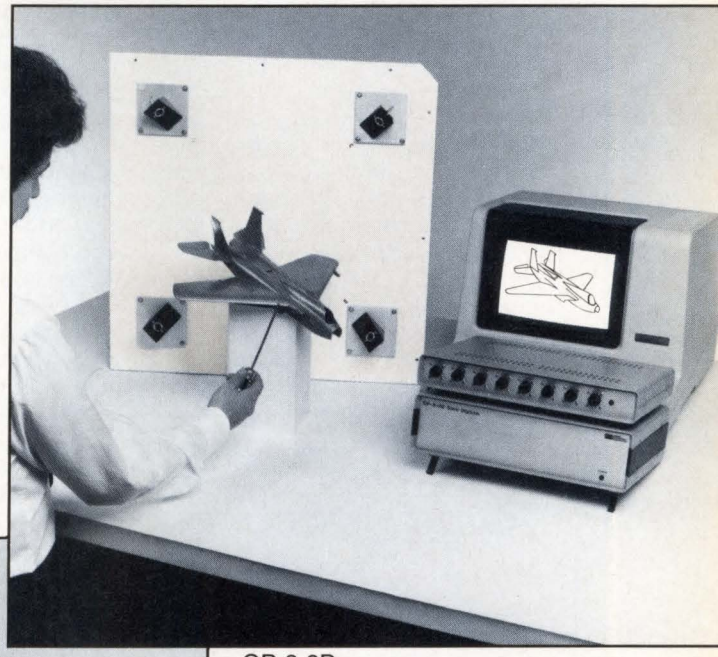

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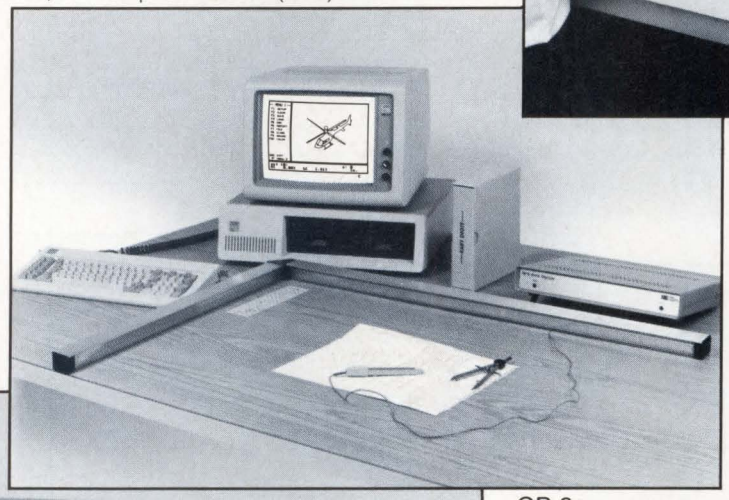

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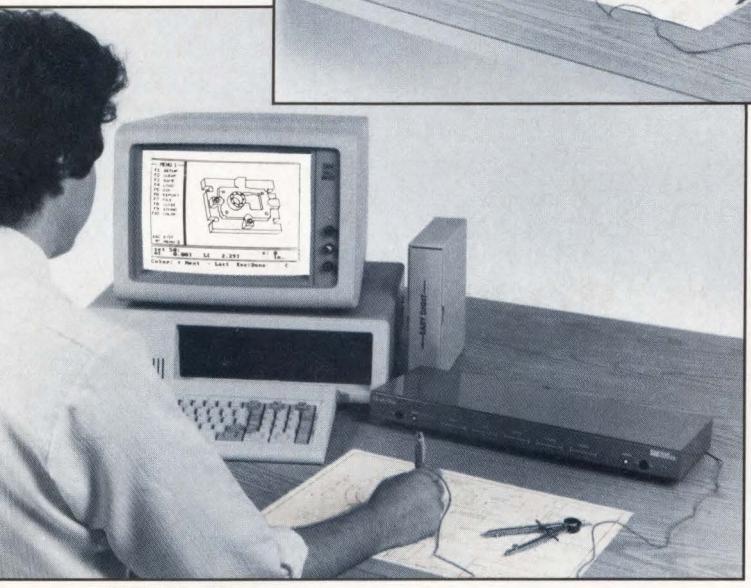

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CIRCLE 83

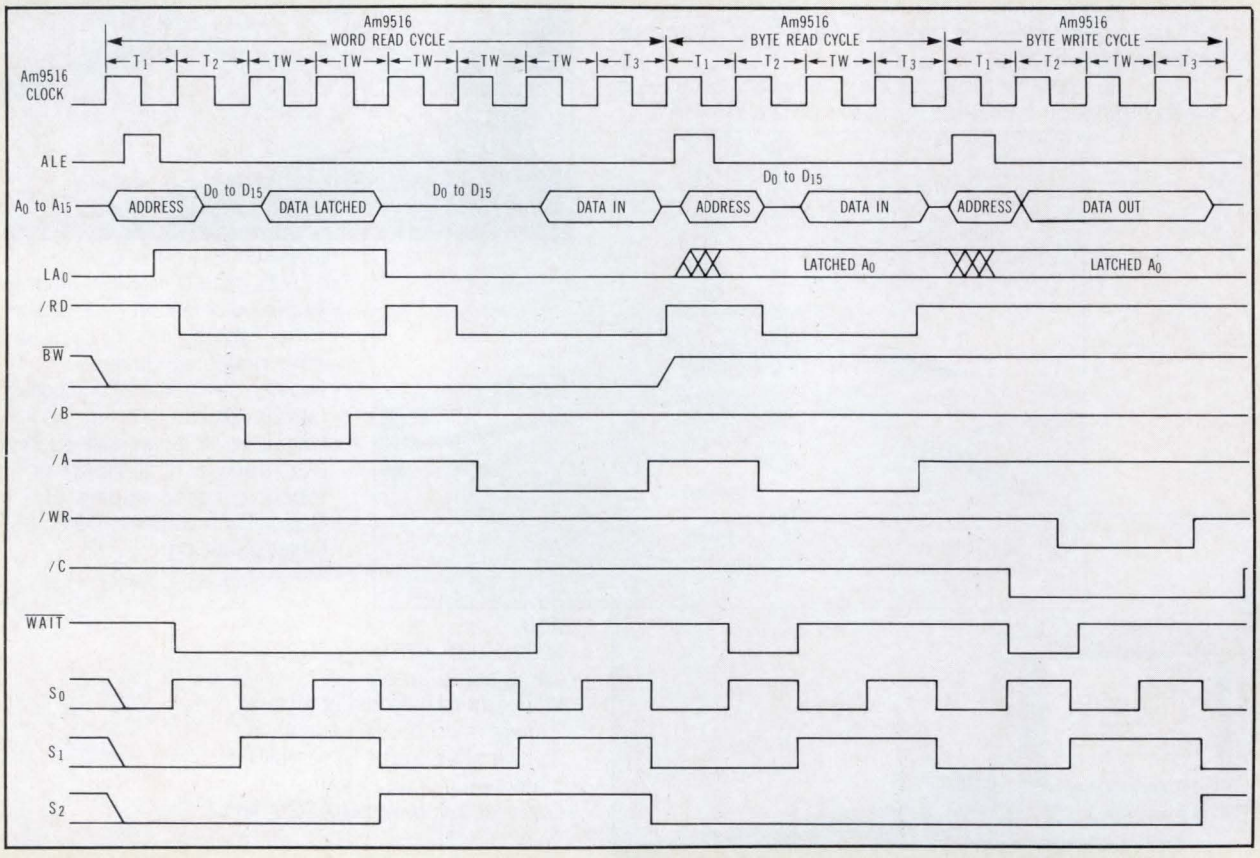
A matter of timing

The complex AmPAL22V10 design used the accompanying timing diagram to correspond to the desired waveforms. They are partitioned by the respective binary state (or count) from the counter.

The desired timing requirements during the period when the DMA controller is bus master appears below. During time T1, address latch enable (ALE) is asserted by the DMA controller to denote the beginning of the cycle; a short time later, an address is driven onto the bus. This address is valid at the falling edge of ALE. The control signal LA0 (latched A0), therefore, must be valid at this time, as well. In this phase of the cycle, it must also be high to enable the odd byte from memory to be loaded into the bidirectional I/O port. In addition, the assertion of ALE performs the function of resetting the 74LS161 counter to 0000 in order to synchronize the cycle.

During time T2, the DMA controller will assert its $\overline{DS}$ signal. The timing for this signal, in conjunction with the R/$\overline{W}$ signal (asserted in T1) must be transformed into an 8088-equivalent $\overline{RD}$ signal. During a word read cycle, this $\overline{RD}$ signal also must be artificially negated and then reasserted to accomplish a double byte read. At the same time, the DMA controller must be "parked" in order to multiplex or assemble a word. Thus, the $\overline{WAIT}$ signal is also asserted at time T2. During time TW (S2, S1, S0 = 010), the receiver clock enable control signal $\overline{B}$ must be asserted in order to allow the next system clock's rising edge to strobe the upper byte into the bidirectional I/O port. This is accomplished during the next TW period (S2, S1, S0 = 011).

During the remainder of the word read cycle, $\overline{RD}$ is negated and then reasserted after LA0 has been forced low to address the even byte. $\overline{A}$ is then asserted to allow both the previously latched upper byte and the current lower byte to be driven onto the DMA controller's pins. And finally, the $\overline{WAIT}$ signal is negated, allowing the DMA controller to finish its read cycle by strobing in the 16 bits of command data on its data pins.



highly organized application-oriented control blocks to be formed easily. These tools can conceptually raise the designer above the details of the design at the logic level and directly translate the necessary response characteristics from a timing diagram.

This approach can be referred to as a "sculptured design" technique because it is analogous to the way solid stone is formed according to an artist's image. Raw logic can be transformed directly into useful control functions from the desired timing information.

The AmPAL22V10 is, in essence, a fuse-programmable gate containing up to 22 inputs and 10 outputs. It can define and program that architecture of each output on a pin by pin basis. Thus, the designer is free to optimize the design mix between registered and combinatorial functions as needed.

The AmPAL22V10 is programmed by opening fusable links in any or all of its 10 output macrocells, as well as in its AND gate array. The AND gate structure is very similar to other PAL devices; therefore

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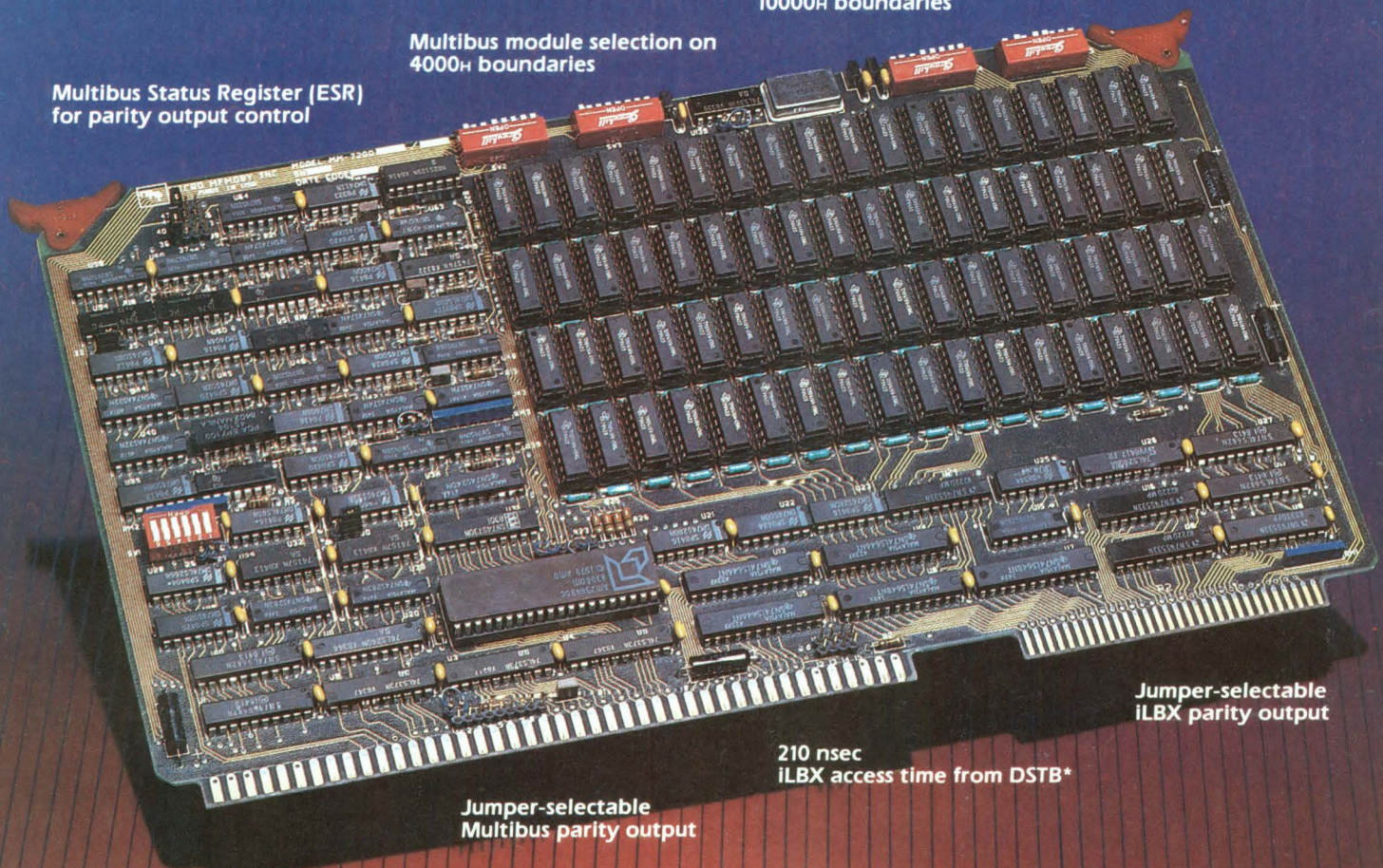

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iLBX parity output

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iLBX access time from DSTB*

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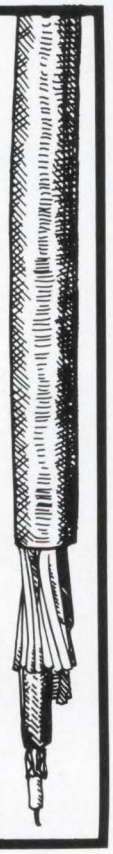

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it allows the same powerful, yet familiar features. However, it is the AmPAL22V10's 10 output logic macrocells that give the designer substantial new design freedom. Moreover, at each macrocell output is a tri-state output buffer controlled by a separate output-enable AND gate.

These macrocells provide the AmPAL22V10's key features. They can be configured to make any or all of the I/O pins act either in sequence or in combination and have either active-high or active-low characteristics. Furthermore, the output enables can individually control the direction of the pins so they act as outputs, inputs, or bidirectional ports.

A number of trade-offs and limitations are apparent in a design that so dramatically affects the input and output of the system. The most obvious limitation stems from under utilization of 16-bit peripherals on an 8-bit bus—the speed of all I/O operations are cut in half. As a result, bus utilization will increase if the l6-bit peripheral represents a significant factor of the bus use. A CRT controller such as the Am8052 might use 5 to l0 percent of the bus bandwidth for display information when using 16-bit I/O. Converting to 8-bit I/O would double bus use to 10 to 20 percent. Another factor that might affect the bus usage is the efficiency of the 8- to 16-bit conversion control logic. If the state machine designed to perform the 8/16-bit (or 16/32-bit) conversion is improperly designed, extra transfer overhead might be introduced. This might mean a sequential transfer of two 8-bit values would take twice as long a single 16-bit transfer.

The design constraints might limit the use of the peripheral to byte-only operations during data transfers (as in the design using the DMA Am9516 controller), and slow it down by a factor of two during command operations. For such a DMA device as the Am95l6, the extra time required for command fetching is not usually a significant portion of bus time.

System designers will have to weigh the cost of the extra overhead on a case-by-case basis. The benfits may well justify these limitations—particularly when the bus is self-limiting, but the device characteristics allow for value-added designs. In addition to bus degradation for certain configurations, extra logic and design effort are involved. Most interfaces outside a system's immediate family require some kind of extra interface logic, however. By manipulating the signals and incorporating them into programmable logic devices such as the AmPAL22V10 device, therefore, most of this logic is free.

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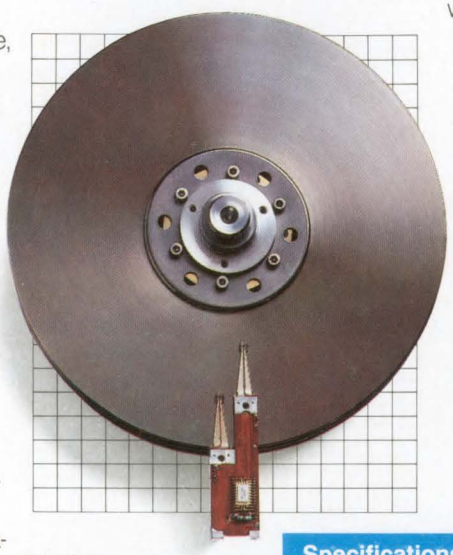
CIRCLE 87

8 INCH DISK MEMORIES

Quality Performers

Century Data Systems now introduces its new C-Series, a line of higher capacity, 8-inch disk memories. These memories are available in a variety of models to offer OEMs the versatility they want, along with the quality and reliability they have come to expect.

This new family of high performance, 8-inch disk memories uses advanced technology and provides compact, reliable mass storage. For example, our new 8-inch Winchester, the C2476, is the ideal choice for computer systems utilizing disk memories in multi-user and multi-task environments which require fast access to large files of data. The C2476 stores 476 megabytes in significantly less cabinet space than previously available models and has an average positioning time of 15 milliseconds.



The C2075, our initial C-Series offering, is an 8-inch fixed/removable disk memory containing 80.2 megabytes of storage. Continuing this line of disk memories is the C2120, our new 122.9 megabyte fixed/removable disk. Both of these disk memories provide OEMs with powerful new sales tools. The fixed Winchester disk portion of the device provides high-capacity, reliable, on-line storage while the removable cartridge extends the on-line storage and provides faster, more convenient backup than tape.

These compact, fixed/removable 8-inch disk memories are the perfect match with large personal computers, microcomputer systems or transaction-oriented systems.

All C-Series products fit in our new, standard 8.5-inch wide package. OEMs using large disk memories can now standardize on one compact package for installation in computer cabinets, equipment pedestals, or on desktops.

Like all our disk memories, the new 8-inch product line is reasonably priced, easy to install, and includes the quality and performance OEM systems require. We invite your inquiries. Write or call: Century Data Systems, Product Marketing, 1270 N. Kraemer Blvd., Anaheim, CA 92806 (714) 632-7500.

Specifications	C2075	C2120	C2476
Storage capacity, fixed disks	53.5 megabytes	87.8 megabytes	475.9 megabytes
Storage capacity, removable cartridge	26.7 megabytes	35.1 megabytes	———
Positioning time, average	32 milliseconds	32 milliseconds	15 milliseconds
Interface	SMD/LMD	SMD/LMD	ESMD
Transfer rate	1209 kilobytes/sec	1209 kilobytes/sec	1859 kilobytes/sec
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CIRCLE 88

Chip set improves floating point coprocessor performance tenfold

The WTL1164/WTL1165 floating point coprocessor chip set claims to have speeds that are 10 times faster than those of existing single-chip coprocessors. Specifications indicate high levels of performance for this two-chip set. These specs include single-add operation time of 0.360 μs, double-add of 0.540 μs, single-multiply of 0.360 μs, double-multiply of 0.660 μs, single-divide of 1.860 μs, and double-divide of 3.780 μs. A full 32-bit 16.67-MHz data bus provides the necessary bandwidth to sustain performance of at least 1 million floating point operations per second.

Both the WTL1164 IEEE floating point multiplier and the WTL1165 ALU provide high performance single- and double-precision (32- and 64-bit) scalar floating point processing for general-purpose computer systems. Emphasis on minimum-latency operations means increased scalar throughput as well as an expanded set of operations.

All four floating point operations (add, subtract, multiply, and divide), as well as direct functions for floating point comparison, are provided on the low power (1.5 W) NMOS VLSI chip set. Data format and floating point operations conform to the proposed IEEE 754, version 10.0 standard. This requirement includes all rounding modes, infinity, denormalized and zero-operand representations, and treatment of such exceptions as overflow, underflow, divide by zero, invalid, and inexact operations.

Dedicated circuit arrays provide faster processing than designs that rely solely on sequential, clocked logic. Array throughput time for the multiplier chip is less than 180 ns for a single precision (32-bit) and less than 300 ns for a double precision (64-bit). Array throughput time for the ALU is less than 180 ns for both single- and double-precision functions. These figures include the time for performing arithmetic function, denormalization, renormalization, and exponent adjustments.

The multiplier design is also novel. Increased density results in an increase in array size to 27 x 53 bits, double the size of some pipelined floating point multipliers. The chip set includes mixed-precision operations and IEEE divide. It comes in a small die size (under 300 mil) and a small package (64-pin DIP and 68-pin leadless chip carrier).

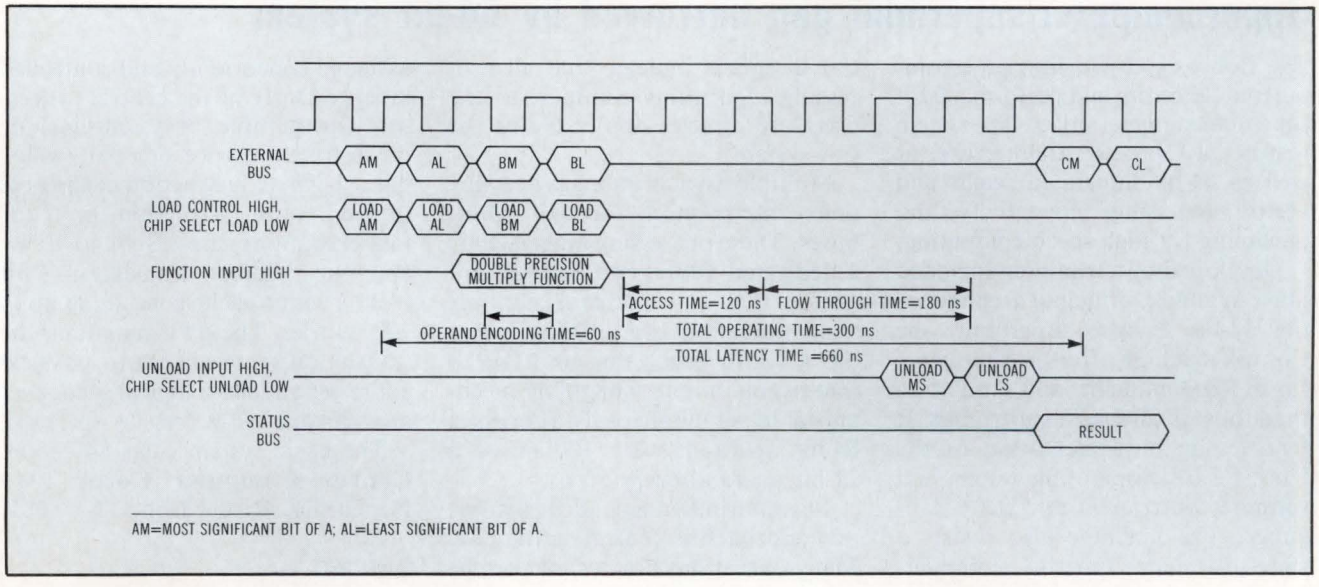
The chip set interfaces directly with 32-bit buses. Single-phase, edge-triggered clocked interfaces sport fully registered TTL-compatible inputs and outputs. Conversion occurs between 32-bit two's complement integers and any floating point format.

The chip set has speed ratings that include 2.78-MFLOPS (360-ns) 32-bit and 1.87-MFLOPS (540-ns) 64-bit add/subtract/convert/compare; 2.78-MFLOPS (360-ns) 32-bit and 1.52-MFLOPS (660-ns) 64-bit multiply; 0.54-MFLOPS (1.86-μs) 32-bit and 0.26-MFLOPS (3.78-μs) 64-bit divide; up to 3.33 MFLOPS (300 ns) for pipelined operations; up to 4.17 MFLOPS (240 ns) for chained operations; and 32-bit data input or output operation every 60 s.

Prices for the two-chip set start at $600 in quantities of 100. Sampling will begin in March and production quantities will be available in late April. **Weitek Corp,** 501 Mercury Dr, Sunnyvale, CA 94086.

—S.F.S.

Circle 260



Integral disk and printer mark transportable computer that runs Unix

A 68000-based portable computer announced by Hewlett-Packard integrates a 9-in. electroluminescent display, ink-jet printer, graphics processor, 3½-in. floppy drive, and the Unix operating system in a 24-lb package. The Integral Personal Computer comes standard with 800 Kbytes of memory. This is divided into 256 Kbytes of ROM for the Unix kernel, 512 Kbytes of RAM for the system itself, and 32 Kbytes of display RAM.

Additional features include a realtime clock and a 16-bit graphics processing unit that supports a windows package on the 512- x 255-pixel display. Window management provides a user interface to applications and can be accessed via menu options corresponding to function keys.

This computer provides technical end users with an entry-level, transportable machine that runs HP's Unix product (known as HP-UX). The machine also aims at business professionals working in a Unix environment, although some features are obviously directed at the realms of instrumentation and realtime computing.

A built-in HP-IB (IEEE 488) link and two expansion ports distinguish

this machine. A bus expander allows addition of memory cards or other options (eg, an eventual Ethernet card). Two human interface loop connectors are available, one of which can be used for an optional mouse. Currently available plug-ins include an RS-232 interface, the HP-IL serial interface loop, a binary coded decimal interface, and a current loop interface. Plug-in RAM cards are available in 256-Kbyte or 512-Kbyte sizes.

HP says that for the purposes of the Integral Computer—and because the Unix kernel is in ROM—a hard disk is not needed. One could clearly be attached via the bus expander, however. Instead, the 3½-in. microfloppy provides 710 Kbytes of storage. Because the operating system is mostly in ROM, the majority of the disk is available for application programs and data.

The Unix version supported by the Integral personal computer is Bell System III Unix with extensions to form HP-UX 2.1. Extensions include the proprietary window manager, a graphics library, Technical Basic, and the Personal Applications Manager. PAM is the main user interface to the Unix system and allows the user to run applications and manipulate files from a menu.

In addition to Technical Basic, the Integral personal computer supports several high level language development environments, each consisting of a compiler, an editor, a loader, and an assembler. It supports C, Pascal and Fortran. The Technical Basic interpreter is specifically designed to aid in instrumentation with graphics support, plus instrumentation I/O, and matrix manipulation commands. The machine costs $4495. **Hewlett-Packard,** 11000 Wolfe Rd, Cupertino, CA 95014.

Circle 261 —*T.R.W.*

Supercomputer/supermini gap narrowed by 64-bit system

The Convex C-1 provides supercomputer architecture and performance at superminicomputer prices. The system features a Cray-like architecture, as well as 64-bit integrated scalar and vector processing, interactivity, and pipelining for high speed computing.

Developed by a team that included Steve Wallach, principal architect of the 32-bit Eclipse supermini, the Convex machine offers greater benefits in R&D modeling and simulation than those available in superminis. It features an implementation of the Unix 4.2 BSD operating system and supports Fortran 77 and the C language. The machine also boasts a state-of-the-art Fortran compiler. C-1 designers indicate that all processing algorithms common to the Cray are directly applicable to the C-1 system.

Multiple asynchronous processing units interconnect through 64-bit buses. These processing units include a dedicated address and scalar unit (ASU) that can perform multiple scalar operations every 100 ns. It also has a vector processing unit (VPU) that uses a unique scheduling mechanism to simultaneously process a 64-bit operand every 100 ns or a 32-bit operand every 50 ns.

The multiple independent subsystem approach is central to the C-1. Many operations besides I/O can be executed concurrently and controlled independently of the central processor. The multiple subsystems include the instruction processing unit (which has a 1-Kbyte instruction cache able to hold entire instruction loops for fast execution), the ASU and VPU, and the address translation unit (ATU) with a cache containing up to 1024 entries. The ATU maintains the translation from virtual to physical addresses and has a logical cache that provides one-cycle access to operands.

The basic system costs $495,000. **Convex Computer Corp,** 1819 Firman Dr, Richardson, TX 75081.

—*J.V.*

Circle 262

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CIRCLE 89

High end VAX delivers performance with large machine technology

With about the same physical size and power needs as the VAX-11/780, the high end VAX 8600 delivers up to 4.2 times more performance. To enhance speed and reduce the number of operations, the machine uses customized ECL gate arrays, a dedicated memory bus, pipelined operation, and write-back cache.

The system can provide 32 Mbytes of main memory, 160 Gbytes of on-line storage, and 4 Gbytes of program address capability—all speeding up large computation-intensive applications. Support is provided for 512 communication lines (more under DECnet), Unibus, DR780, and Massbus general purpose I/O interfaces.

Internal architecture incorporates many large-system features. ECL macrocell array chips combine with reduced data paths and faster RAMs to deliver a cycle time that is 2.5 times faster than the Schottky TTL gate arrays used in the VAX-11/780. Further increases in performance result

from four stage pipelining that overlaps fetch, decode, address calculation, operand fetch, and instruction execution. This reduces the average number of machine cycles required per instruction.

While the VAX-11/780 uses an 8-Kbyte write-through cache, the 8600 uses a two-way associative 16-Kbyte write-back cache to improve the overall cache throughput. This cache allows the processor to continue at full speed without waiting for the update of slower main memory, as does the write-through cache. A memory controller ensures that modified data is written to main memory only when necessary and without interrupting the processor.

Various enhancements in version 4 of the VMS operating system facilitate the system's use in the VAX-cluster environment. Features include cluster-wide batch and print queuing, a distributed lock manager for data integrity, and a distributed file system for easier access to files stored on disk subsystems throughout the cluster.

Allowing the system to operate in a VAXcluster configuration of up to 16 processors, the Computer Interconnect dual path bus also attaches intelligent storage controller subsystems. The company offers a building block configuration of the 8600 for $450,000. Volume deliveries of the systems are scheduled for April. Prices will range from $576,000 to $970,000. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.

Circle 263 —*M.B.*

Single-board computer holds complete VMEbus system

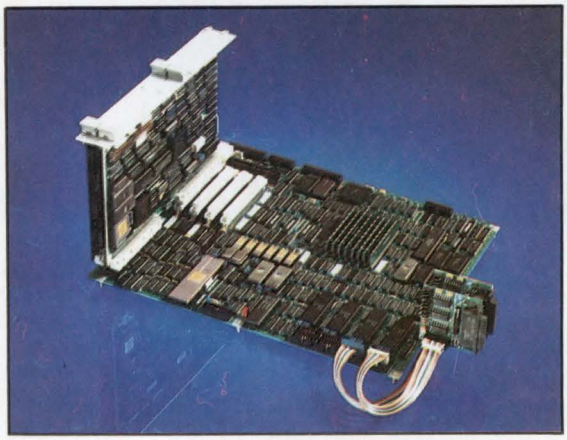
The Baseboard is a single-board VMEbus system with a Winchester/floppy disk controller, eight serial ports, an 8-bit general-purpose parallel port, and five VMEbus expansion slots. This 68000-based unit replaces nine independent modules as well as the backplane of a typical VMEbus system.

The unit features a 32-bit 68010 microprocessor that runs at 10 MHz with no wait states. The CPU supports virtual memory and demand paging. Onboard dynamic RAM expands from 512 Kbytes to 2 Mbytes. Two EPROMs provide 64 Kbytes of bootstrap and diagnostic code. A "single level" MMU allows 32 or 64 contexts with up to 4096 pages, plus protection and status mechanisms.

Programmable serial ports can handle up to eight users and, with additional serial cards, can handle as many as 32 users. Each user can program serial ports for data rate, bit format, and bus protocols. Serial communications are handled with vectored interrupts.

The 68008-based Winchester/floppy disk controller can support up to three mixed ST506, ESDI, or ST412HP Winchester drives, in combination with four DS/DD 5¼-in. floppy drives. The controller permits a high level, task-oriented command structure, and performs DMA by cycle interleaving.

Built-in VMEbus expansion slots accommodate virtually any type of memory or peripheral control board. The bus interface has 24-bit addressing and 16-bit data.



Standard software includes Motorola's Versabug and Unix version 5.2. Cost is $3895 in OEM quantities. **Interphase Corp,** 2925 Merrell Rd, Dallas, TX 75229.

—*R.G.*

Circle 264

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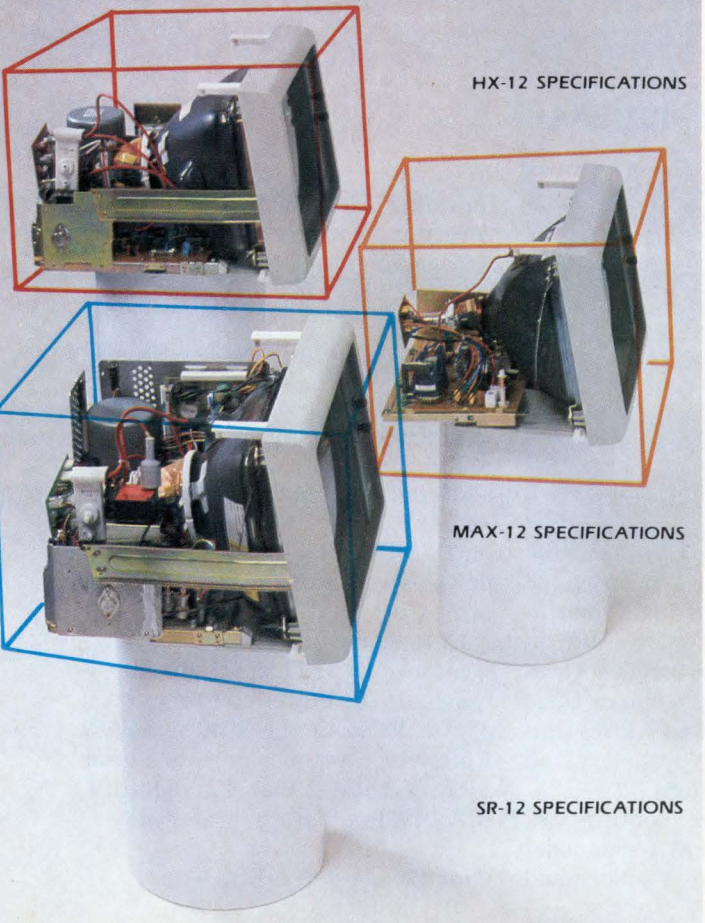


HX-12 SPECIFICATIONS

CRT	12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22)
Input Signals	R, G, B, channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video Bandwidth	15 MHz
Scan Frequencies	Horizontal: 15.75 KHz Vertical: 60 Hz
Display Size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 240 lines (non-interlaced) 480 lines (interlaced)
Misconvergence	Center: .6mm max Corner: 1.1mm max
Display Colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows—8x8 dots)
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

MAX-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor)
Input Signals	Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels
Video bandwidth	18 MHz
Scan frequencies	Horizontal: 18.432 KHz Vertical: 50 Hz
Display size	204mm x 135mm
Resolution	Horizontal: 900 dots Vertical: 350 lines
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

SR-12 SPECIFICATIONS

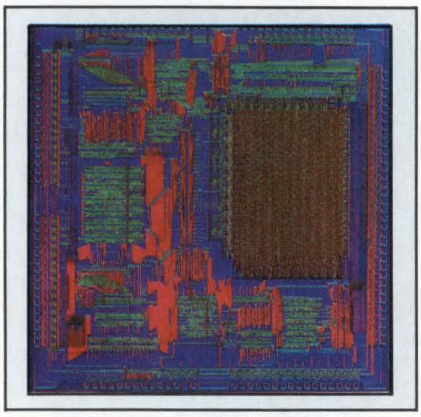
CRT	12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface
Input Signals	R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video bandwidth	25 MHz
Scan frequencies	Horizontal: 31.5 KHz Vertical: 60 Hz
Display size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 480 lines (non-interlaced)
Misconvergence	Center: .5mm max Corner: 1.0mm max
Display colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows)
Input Connector	9 Pin (DB9)—cable supplied

CIRCLE 90

A 32-bit VLSI family provides independent building blocks

Members of the 32-bit Am29300 family are functionally partitioned building blocks intended to provide design flexibility. Device-level integration makes these chips top performers in array and digital signal processing, intelligent peripheral control, and graphics. The first chip in this series available for sampling is the Am29325—a single-precision 32-bit floating point processor that requires only one cycle to execute all instructions.

The Am29325 floating point processor performs addition, subtraction, and multiplication operations in a single IC. Data path functions are also integrated onboard. The device has a three-bus architecture, common to all Am29300 family members. With two input buses and one output bus (each of which is independent),



the coprocessor configuration provides high I/O bandwidth because bidirectional data buses are eliminated. Programmable I/O allows interface to 16- and 32-bit systems.

The chip supports both the IEEE and Digital Equipment Corp single-precision floating point formats. Operations for conversion between 32-bit integer format and floating point format, and conversion between IEEE and DEC VAX floating point formats are available. Input voltage ranges from −0.5 to 5.5 V.

The devices implement a scaled, ion-implanted, oxide-isolated bipolar process that features three-layer metal interconnections. Internal ECL circuitry is used for high speed, with I/Os done in TTL.

Family members in addition to the floating point processor, include the Am29332 ALU; Am29323 32-bit parallel multiplier, Am29331 microprogram sequencer; and the Am29334 four-port, dual-access register file. All devices will be sampled this year. **Advanced Micro Devices, Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 265 —*J. V.*

Voice recognizer broadens data entry options

The series 4000 voice recognition system allows easy creation of custom voice application vocabularies for data entry. This low cost system uses the continuous-recognition, speaker-dependent format. It can operate in tough environments that exhibit very high background noise.

The system links with mainframes, minis, or microcomputers, as well as with industrial controllers. The 4000 uses a version of Verbex's patented continuous voice recognition algorithm, first implemented in the firm's 3000 series of data entry systems. The Verbex algorithm uses flexible word models that accommodate natural variations in a user's voice without sacrificing vocabulary size or recognition accuracy.

Standard hardware consists of a single-board speech processor, two RS-232-C asynchronous ASCII I/O ports handling data at 9.6-Kbaud transmission, front-loading CMOS

voice cartridges, and a microphone headset. The voice cartridges contribute greatly to the system's use in rugged settings where media such as floppy disks are prone to abuse. These battery-driven CMOS cartridges contain the application vocabulary and each user's voice pattern.

The voice recognizer converts verbal data into a digital format and compares it with the user's individual voice patterns, which are stored on the voice cartridge. Alternatively, voice prints can be stored on the host. Recognition response time is less than 300 ms. The machine recognizes word/phrases of between 0.1- and 2.0-s duration. Vocabulary size reaches 100 words.

Series 4000 voice planner software lets the user develop voice data entry routines, word lists, training scripts, and translation tables for the recognizer. The software package runs on MS-DOS/PC-DOS compatible units, as well as on the Digital Equipment Corp VAX, and others.

Console size of the voice recognizer measures 18 x 13 x 3.5 in. and it weighs 15 lb. Power consumption is 45 W. Price of the 4000 is $4900, while voice planner software costs $500. **Verbex,** 2 Oak Pk, Bedford, MA 01730.

—*J. V.*

Circle 266

Telex Shamrock cuts tape drive problems down to size.

(this size)

This gate array chip takes the place of two 10 x 14 PC boards of previous technology. But, small as it is (only 0.4" square), it plays a large part in providing the huge boost in reliability and full performance GCR you'll get in the Shamrock 9250 tape subsystem.

Telex has combined over a decade of GCR advancements, the latest in vacuum column technology and reduced component count to make Shamrock the most reliable 50 ips tape subsystem in its class. Shamrock is so well designed, there are no planned service calls. Ever. Resident diagnostics and four microprocessors monitor and make any corrective adjustments necessary.

Reliability alone should give you all the reason you need to make Shamrock your first choice in tape subsystems. But Telex can give you a lot more reasons. Starting with the fact that Shamrock's unit price is less than half that of previous GCR subsystems. There's also Shamrock's full-size performance — faster access, greater storage efficiency, higher data reliability — all with reduced energy levels.

Size up Shamrock for yourself. Call the Telex OEM Sales Office nearest you or call Telex OEM Marketing at (918) 627-1111.

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International Telex Computer Products International, Inc. 115 Norwood Pk. South, Norwood, Massachusetts 02062 (617) 762-6700

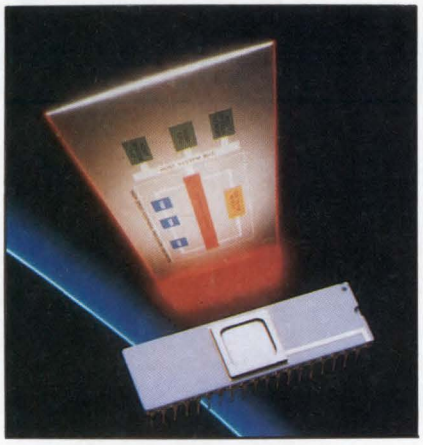
CIRCLE 91

Single-chip image processor sports non-von Neumann architecture

The UPD7281D combines a data flow system with a pipeline approach to produce a processing speed of 5 million instructions per second. This chip is suited for image processing applications using such algorithms as two-dimensional convolution and rotation, and is also appropriate for realtime signal processing.

The token-based data flow architecture allows easy multiprocessor design and includes separate input and output data buses for high speed I/Os. The data flow processor is controlled by tokens instead of by instructions. A token consists of a data field, a control field, and a tag. The tag holds processor address and identifier fields. The operands contained in the tokens control the order of computation.

This data flow scheme makes use of available multiprocessing capabilities without requiring a complex control scheme. This architecture also



eliminates the time spent in fetching instructions from program memory and time needed for storing and loading intermediate results during the computation.

The chip also features a powerful set of image processing instructions including barrel shift, bit operation, and bit check. This instruction set can condense program sizes significantly. The IC also contains a high speed multiplier that produces a 33-bit product from a 17-bit multiplier and multiplicand in 200 ns.

Two system configurations are available for combining chips. A cascade configuration requires a processor that feeds the input data token in one end and receives output from the other. The ring configuration has an image memory, host processor, and hardware logic to multiplex data from the host processor and the image memory.

To produce the NMOS device, NEC uses a design rule of 1.75 μm and integrates 115,000 transistors on a 6.93- x 6.99-mm chip. The IC comes in a cerDIP with 40 external pins and uses a single 5-V power supply voltage. Engineering samples are approximately $200 to $250. **NEC Electronics, Inc,** 401 Ellis St, Mountain View, CA 94043.

Circle 267 —*M.B.*

Graphics system downloads rendering tasks from the host

Important three-dimensional graphics functions are performed locally with the Model One/380. This high resolution 60-Hz refresh system, featuring a 32-bit floating point processor, provides a complete and integrated "rendering pipeline" that can be adapted easily by the system designer. (Rendering is the representation of an object in perspective view.) Using this system, functions important to realistic three-dimensional image generation—such as coordinate transformations, light model calculations, smooth shading, and hidden surface removal—are executed downline from the host.

This machine is an upwardly compatible extension of the Model One/80 and Model One/10. The 380 contains a 1-Mbyte display list memory, expandable to 4 Mbytes. Memory configurations include a 1280- x

1024- x 24-bit format with eight planes of image memory and a 16-bit full resolution Z-buffer for depth. Flicker-free display resolution at 6 MHz is 1280 x 1024 x 8 pixels. Monitor refresh rate is 60 Hz (noninterlaced) and software-selectable rate is 30 Hz (noninterlaced).

Local hidden surface removal and full-color smooth shading are performed on the 380 via custom gate arrays to help produce speeds of 1 to 3 μs/pixel. Further, this graphics system allows local light source modeling with variable surface properties. Interactive manipulation of three-dimisional objects can be done quickly and locally.

A local debugger allows the programmer to step through program execution, list defined macros, execute graphics commands locally and return to normal execution. Standard on the Model One/380 is an integral DMA port conforming to Digital Equipment Corp DR11W and DRV11B specifications. The Model One/380 comes in either a 5¼-in. high enclosure suited for rackmounting, or in a deskside tower enclosure. A complete system—including 19-in. monitor, keyboard, data tablet, and mouse—costs $41,500. **Raster Technologies, Inc,** 9 Executive Park Dr, N Billerica, MA 01862.

Circle 268 —*J.V.*

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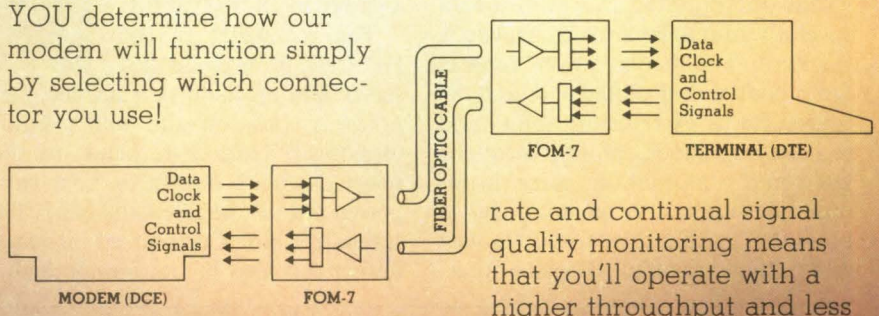

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CIRCLE 92

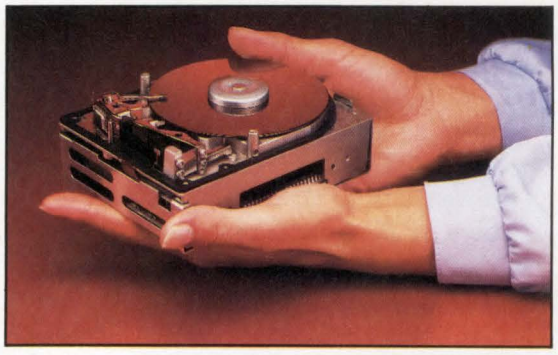
Micro-Winchester disk drive is built tough for the portable world

A 10-Mbyte, 3½-in. Winchester disk drive sports a controller using servo code embedded in the disk. The unit's rugged design—it can withstand a 50-G shock and still operate—aims it squarely at personal and portable computer applications, as well as industrial environments.

The HP 97501A micro-Winchester writes on sputtered thin-film media specially manufactured by Hewlett-Packard. The media, which departs from coated and plated methods, is touted for its extreme durability and resistance to shock damage. Reduced environmental contamination in industrial settings is ensured by a pressure-tested internal seal, as well as a particle trap and corrosion filter.

Unformatted capacity lists at 14.09 Mbytes. Formatted capacity is 7168 bytes per track, 256 bytes per sector. The HP97501A transfers at a rate of 4 Mbits/s. Average seek time is 75 ms, maximum seek time is 150 ms, and average latency is 10 ms.

The controller in the HP drive, using embedded servo data on the disk's surface, can precisely position the unit's mini-monolithic read/write heads to the selected track. Interfaces now supported include the SCSI and IEEE 488 standard links. Customized interface design can also be accommodated.



The 3½-in. disk drive is available now at under $400 in quantities of 10,000. **Hewlett-Packard,** 1820 Embarcadero Rd, Palo Alto, CA 94303.

—J.V.

Circle 269

Diversification and enhancement highlight portable scope family

Enhanced measurement ability is the hallmark of the three latest members of the Tektronix 300-MHz portable oscilloscope family. The 2465 DVS (digital video system), 2465 DMS (digital multimeter system), and 2465 CTS (counter/timer system) scopes feature IEEE 488 (General-Purpose Interface Bus) programmability. But they are also recognized for their standalone attributes.

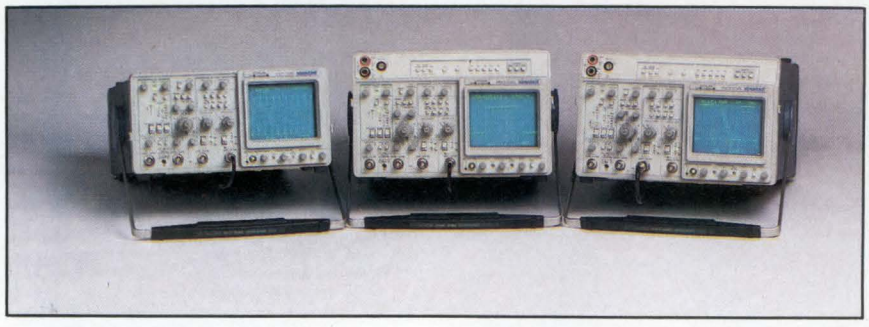
The top performer of the trio—the 2465 DVS—incorporates a counter/timer/trigger as well as a digital word recognizer, an auto-ranging 4½-digit voltmeter, specialized television waveform measurement capability, and a general-purpose interface bus link. These traits combine with the standard features of the 4-channel 2465 family (onscreen readouts of trigger level, voltage, time interval, frequency, and phase). Special television waveform measurement capabilities built into the DVS make the device especially useful for testing raster-scan video systems.

The counter/timer/trigger feature on these scopes provides users with functions such as delay time, delta time (and 1/delta t), frequency, and period—all accurate to 10 parts per million. The 2465 DVS costs $8500.

A 4½-digit auto-ranging digital multimeter, which is also fully GPIB-programmable, comes with both the DVS and DMS 2465 models and provides direct or IEEE 488-bus readout of voltage, current, resistance, temperature, or such measurements as decibel referred to 1 V and decibel referred to 1 mW. Any measurements can be averaged and smoothed for CRT display or transmission to the GPIB controller. This multimeter also provides audible continuity checks and front-panel calibration. A temperature probe helps to locate circuit board hot spots that occur during troubleshooting.

The 2465 DMS, priced at $7800, includes all of the features of the DVS except the unique TV measurement abilities. The 2465 CTS gives up the multimeter feature and specialized TV functions, but is priced at $6600. **Tektronix, Inc,** PO Box 1700, Beaverton, OR 97075.

Circle 270 *—B.F.*



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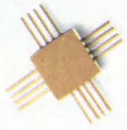

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CIRCLE 93

INTERFACE PROBLEMS?

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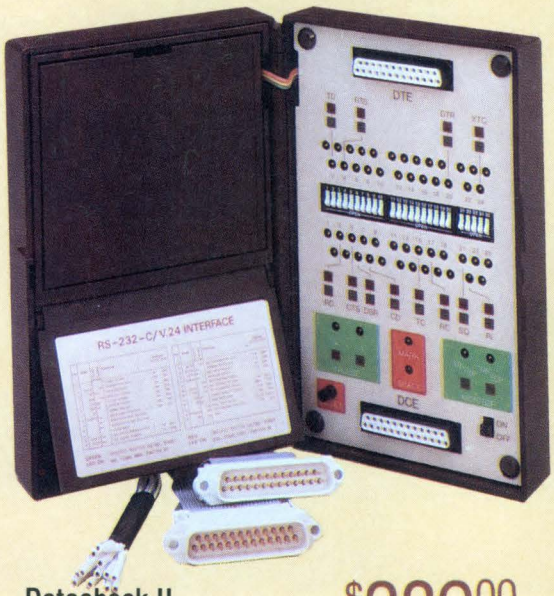
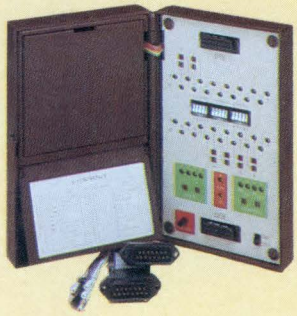


Datacheck II
The ultimate breakout box $239.00



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Digital filter chips drive resolution improvements

A digital filter component featuring 24-bit data resolution is dubbed the KSC 2408. This VLSI device allows data and coefficients each to be represented in 24 bits. Filtering occurs with 48 bits of internal accumulation. Signal-to-noise ratio improvements of up to 50 dB over other general signal processing chips are touted. The NMOS chip has eight programmable second-order filters that can be configured for independent operation or cascaded to form higher order filters. It can filter signals throughout the audible range and beyond, up to a sampling rate of 125 kHz. The KSC 2408's bit serial arithmetic and internal multiplexing functions allow filtering along with such features as input rectification and output decimation. Onchip multiplexing capabilities make the filter suitable in arrays (filter banks). KSC 2408s are $57 each in 1000-piece quantities. **Kurzweil Applied Intelligence,** 411 Waverly Oaks Rd, Waltham, MA 02154.
Circle 271

DRAMs in 256-Kbit format offer page or nibble mode

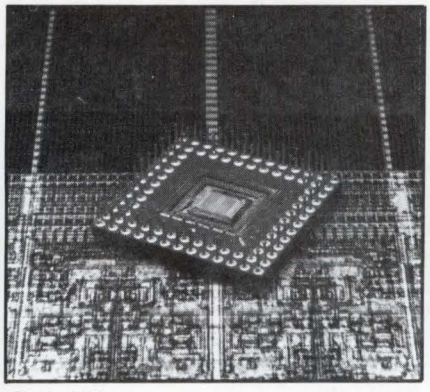
Both the HM50464P and HM50465 are organized in 64 Kbits x 4. Their ability to store data in 4-bit words makes them apt for terminal, microcomputer, and RAM image storage applications where memory bandwidth is critical. The devices use 2-μm process technology. The difference between the two 256-Kbit chips is that the 50464P transfers data in page mode and the 50465P uses nibble mode for faster reading and writing. Both devices consume 350 mW while active and 23 mW on standby. The chips are priced at about $75 in sample quantities of 1 to 24. **Hitachi, Ltd,** 2210 O'Toole Ave, San Jose, CA 95131.
Circle 272

Single-chip microcomputer has advanced peripheral functions

A microcomputer manifested as a single chip combines HCMOS and EEPROM technology. It is called the MC68HC11. This unit provides sophisticated onchip peripheral functions, as well as low power consumption. It is further compatible with the M6801 family and provides an improved instruction set that includes two programmable power-saving operating modes, called Stop and Wait. Static design can run at a 2-MHz bus speed across a wide temperature range. Onchip memory systems include 8 Kbytes of ROM, 512 bytes of EEPROM, and 256 bytes of SRAM. Peripheral functions featured include an eight-channel, 8-bit A-D converter, an enhanced set of serial ports, and timer functions. The CPU uses a four-page opcode map to allow execution of 91 opcodes beyond those native to the 6800 and 6801. Other key MC68GC11A8 features include 3- to 5½-V operation, strobe and handshake parallel I/O, as well as a 21-level vectored interrupt system. First samples are available now. It is priced under $20 in volume quantities. Production quantities will be available in the second quarter of 1985. **Motorola Inc, Microprocessor Products Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 273

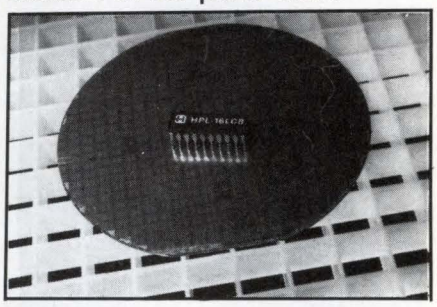
Array logic device packs equivalent of 5000 gates

Programmable array logic devices under the PAL64R32 nomer are packed with the equivalent of 5000 gates. They are seen as an alternative to gate arrays. Embedded in the device are four banks of eight bypassable registers that are capable of performing registered or combinatorial operations on a bank-by-bank basis. One clock input per bank allows asynchronous operation. The PAL64R32 device can run at speeds above 16 MHz and has an output drive of 8 mA. Clock-to-clock output time is 25 ns. This circuit has 64 device inputs and 32 registered outputs. It is available in 84-pin leadless chip carrier and 88-pin grid array packages that (in quantities of 100) cost $215.91 and $225.33, respectively. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050.



Circle 274

Programmable logic device available in low power CMOS

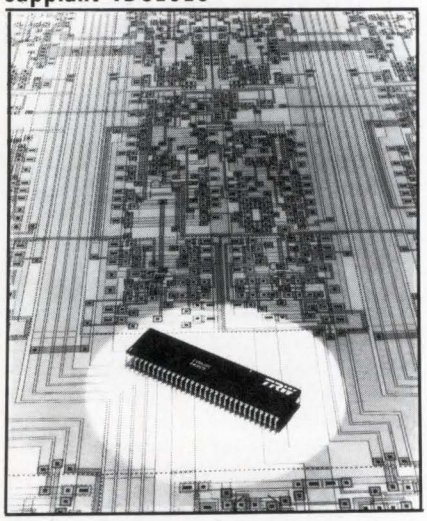


HPL-16LC8 is functionally equivalent to, and pin compatible with, the bipolar 16L8. The HPL-16LCB programmable logic device consumes 95 percent less power than the 16L8. Applications include random logic replacement, address decoding, and pattern recognition. A programmable output polarity feature increases design flexibility and reduces parts count. Thus, device polarity can be individually changed from active low configuration to active high via programming. Static CMOS design allows standby currents set at 150 μA maximum. Average operating power needs are less than 50 mW, with a typical 250-μW standby power requirement. A ceramic DIP, commercial temperature version of the chip costs $12.99 in units of 100 to 999. **Harris Corp,** Box 883, Melbourne, FL 32919.
Circle 275

Pipeline register cuts board space and power needs for DSP

A 16-bit CMOS pipeline register replaces eight octal registers or two 8-bit pipeline registers. Dubbed the LPR520/LPR521, this is a 16-bit version of the AM29520 and AM29521 8-bit registers. Fully compatible, it features four 16-bit registers that can be operated as two independent two-level registers or as one four-level register. It operates at an access speed of 25 ns or less. The LPR520/521 can be used as a double-buffer or "ping-pong" memory element serving two processors. The chip comes in two versions. The LPR520 shifts data through its registers as new data is received, and overwrites data in the last register. The LPR521 retains data in subsequent registers and overwrites in the first. Both parts are available in plastic or ceramic 40-pin DIPs. The plastic parts are priced at $20 in 100-unit lots. **Logic Devices Inc,** 628 E Evelyn Ave, Sunnyvale, CA 94086.
Circle 276

Multiplier/accumulator aims to supplant TDC1010



A high speed 16- x 16-bit parallel multiplier-accumulator, the TMC2110, is a 1-μm CMOS product that replaces the TDC1010 bipolar chip. At full speed, the device can perform a multiply-accumulate operation in 90 ns, for a 11.1-MHz throughput rate. The 16- x 16-bit chip can perform two's complement or unsigned magnitude multiplication that will yield a full-precision 32-bit product. Products can be accumulated up to 35 bits. Individually clocked I/O registers in the form of positive edge-triggered D-type flipflops are provided. The 64-lead DIP is priced at $120. Under a full-throttle, worst-case condition, power consumption is under 350 mW. **TRW Electronic Component Group, LSI Products Div,** PO Box 2472, La Jolla,CA 92038.

Circle 277

Reduced redundancy means easier bit-mapping for 256-Kbit chips

Dynamic RAMs, in three configurations, each offer 256-Kbit capacity. The three configurations are: uPC41256—a 256-Kbit x 1 page-mode device; uPD41257—a 256-Kbit x 1 nibble-mode part; and uPD41254—a 64-Kbit x 4 part. The first chip is available in quantity now, while the latter two are available for sampling. Access times for three parts are 150 and 200 ns. The devices are implemented in NMOS. Reduced redundancy in chip design spells easier bit-mapping for these units. Pricing begins at $27.50. **NEC Electronics Inc,** 401 Ellis St, PO Box 7241, Mountain View, CA 94039.

Circle 278

COMPUTERS

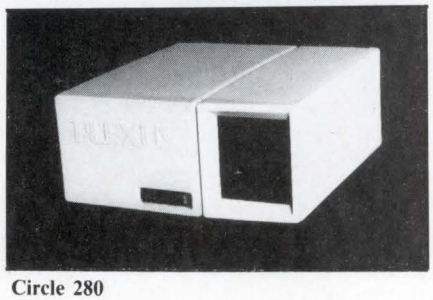
Single-user 32-bit workstation provides VAX/VMS operation

VAXstation I is a true 32-bit single-user system that incorporates the MicroVAX 1 with high resolution graphics and multiwindowing capabilities. Typical applications include laboratory data analysis, schematic capture, process control, and software development. Based on VAX architecture and using the VAX/VMS operating system, the workstation supports the Graphical Kernel System standard. The featured monitor has a 60-Hz noninterlaced 19-in. screen with 960- x 864-pixel resolution. Basic configuration includes 1 Mbyte of main memory., 1-K x 2-K bit-mapped video RAM, a dual 400-Kbyte, 5¼-in. disk drive, and mouse. Combined hardware and software price is $21,095. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.

Circle 279

Supermicro provides Unix operation for one- to eight-user setups

Based on the MC68010, the Plexus P/15 offers compatibility with the present Unix-based line while providing 2 Mbytes of storage. This 32-bit supermicrocomputer features a multiprocessor architecture and uses two MC68010 microprocessors. Eight full-duplex serial ports for terminals or other peripherals further enhance the system. Packaged to fit in small places, the low profile unit is less than 25-in. high and weighs less than 75 lb. It allows for up to 54 Mbytes of disk storage in two Winchester disks, as well as a single 5¼-in. floppy using standard 115 Vac power. Full SCSI interfacing is offered. The 32-bit I/O processor handles all character I/O. Using current 256-Kbit RAM devices, the P/15 memory is available with up to 1 million 16-bit words. **Plexus Computers Inc,** 3833 N First St, San Jose, CA 95134.



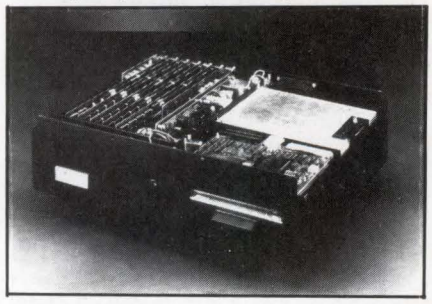
Circle 280

Regulus systems run 68008-based multi-user setups

A range of 32-bit, Unix-based computers, with disk capacities of up to 150 Mbytes, offers six levels of integration. The systems use 68008 microprocessors and Unix-compatible Regulus operating systems. Known as VAR/68Ks, these systems incorporate automatic task-switching hardware to reduce the time for transfer between supervisor- and user-operating modes. External DMA transfers execute at rates up to 2 Mbytes/s and programmed I/O operations run at up to 1.6 Mbytes/s. Minimum configuration includes 1 Mbyte of flexible disk and 5 Mbytes of hard disk memory, eight RS-232-C ports, a Centronics-type port, and the Regulus operating system. Prices range from $7900 to $25,000. **Smoke Signal,** 31336 Via Colinas, Westlake Village, California 91362.

Circle 281

Multi-user systems configure around backup tape and memory unit



Designed to serve as a hub for personal computer expansion, QICSTOR-Plus forms the foundation for a multi-user system. Configured with other IBM PC expansion boards, PC-Slaves, PCs, and PC compatibles, the system supports dumb terminals. In one unit, the QICSTOR-Plus combines a high capacity hard disk, quarter-inch streaming tape backup, and five expansion slots compatible with a an IBM PC. Backup is file oriented. Interfacing the unit to a PC requires only one expansion slot. Hard disk storage runs from 20 Mbytes to 128 Mbytes, with access times as low as 28 ms. The unit measures 19.6 x 18 x 5.4 in. (497 x 457 x 137 mm) for convenient stacking. Pricing starts at $5595. **Alloy Computer Products, Inc,** 100 Pennsylvania Ave, Framingham, MA 01701.

Circle 282

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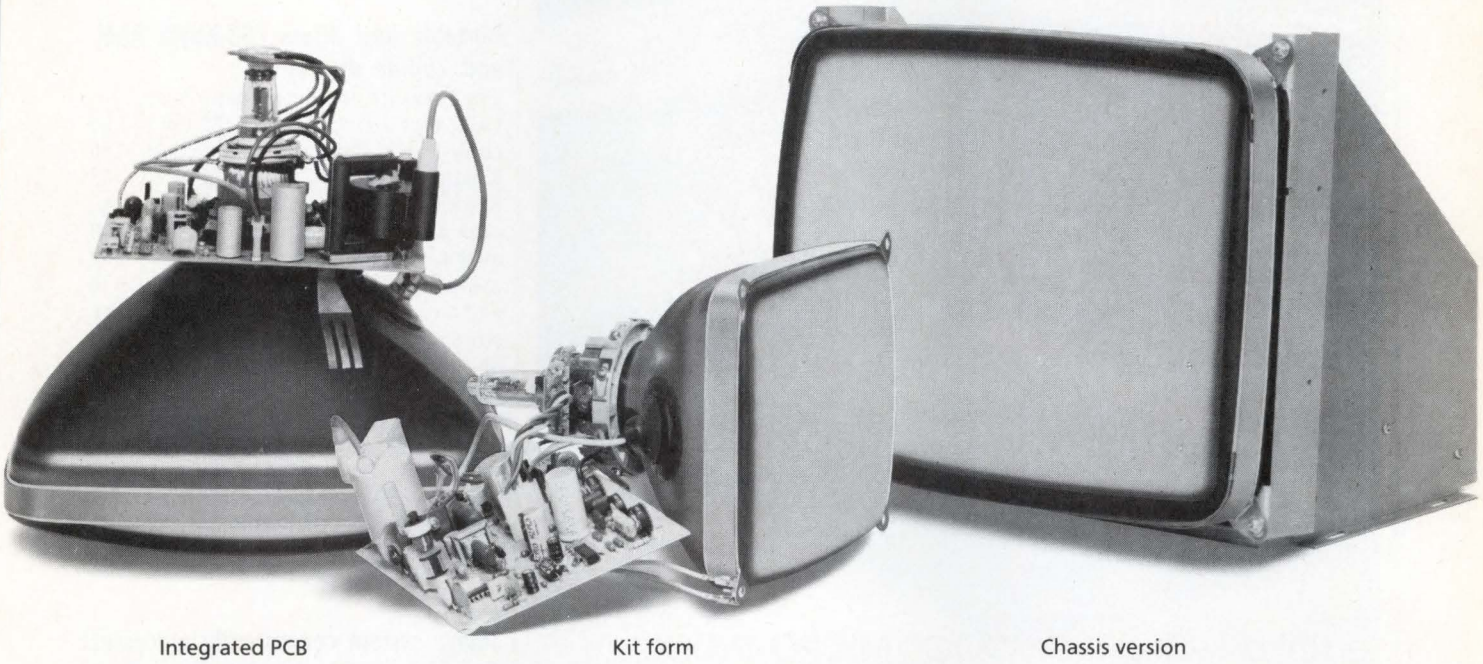

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CIRCLE 95

Document-image system brings optical technology to forefront

Procedures dominated by paperwork are automated via the document-image processor, which incorporates FileNet's recently announced optical disk storage and retrieval (OSAR) library. Using the system, printed, typed, handwritten or drawn documents are captured and their exact images stored, retrieved, and processed electronically. Online storage of a fully configured OSAR library reaches 128 billion bytes. Eight such systems are supported by the document-image system. Other system components include entry stations, integrated workstations, an image management system, and a laser printer. The printer re-creates images, data, or text with a resolution of 400 dots/in. at the rate of 12 pages/min. A basic document-image processor costs $258,000. **FileNet Corp,** 1575 Corporate Dr, Costa Mesa, CA 92626.

Circle 283

Portable unit offers 768-Kbyte RAM and 25-line display

The Pro-Lite computer features a 12-in. LCD that shows 80 col x 25 lines. The entry-level configuration includes 256 Kbytes of RAM, expandable to 768 Kbytes. At the heart of the Pro-Lite resides a 16-bit 80C88 microprocessor, with an 80C87 numeric coprocessor optionally available. This machine weighs 10.5 lb and has a 3½-in. floppy disk drive. Disk storage capacity is 720 Kbytes. Through an expansion box that attaches to the back of the Pro-Lite, either a second disk drive, or a battery pack, or both can be added. The keyboard has 79 full-size, full-travel keys. Price is $2995. **Texas Instruments Inc, Data Systems Group,** PO Box 809063, Dallas, TX 75380.

Circle 284

Image system concurrently processes two 512- x 512-bit images in memory

An integrated image processing development system, the ImTrain, plugs in via ASCII terminal or IEEE 488 devices. Video rate processing technology is used to ensure a realtime interactive environment. Functions such as signal averaging, image addition, and motion detection occur rapidly. Two image frames of 512 x 512 x 8 bits can be held and processed in memory concurrently. Digitized video data transfers over a 10-Mbyte/s bus. The system uses the C language, and operators can write code that calls on standard ImTrain library functions. **Eigen/ Optivision,** PO Box 848, Nevada City, CA 95959.

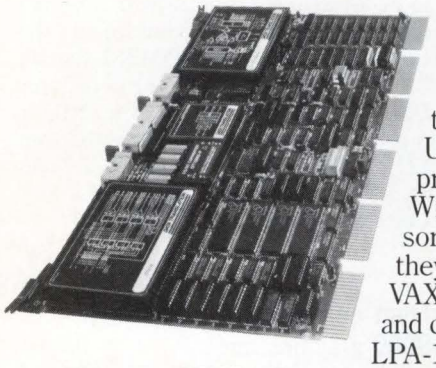
Circle 285

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Finally, a cure for data acquisition and control problems for VAX™ and PDP-11™.

Fred Molinari, President



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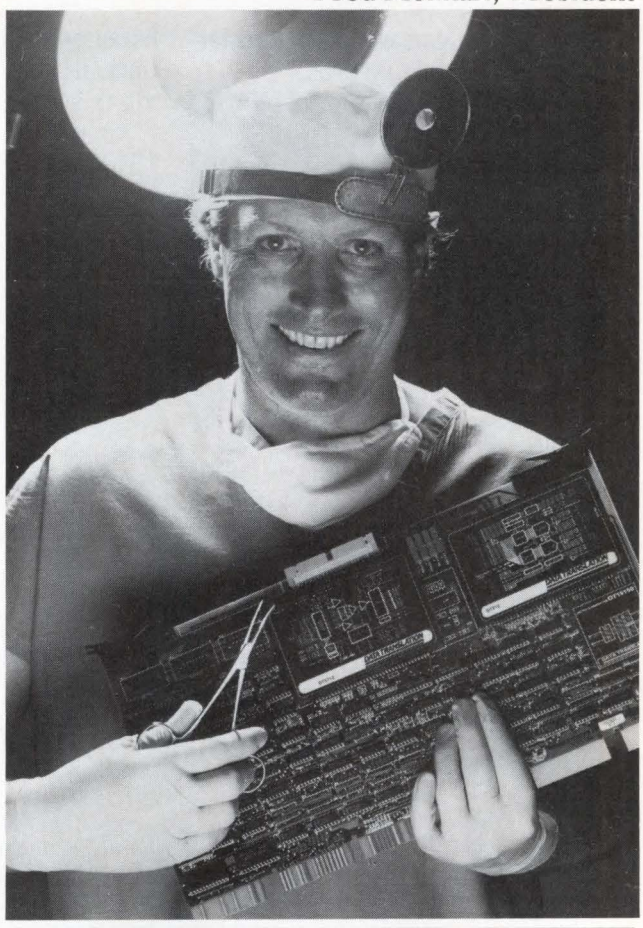

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Model	Analog In	Analog Out	Features	A/D Resolution	Thruput (kHz)	Software UNIX, RSX, VMS	Digital I/O Lines	Prog. Timer
DT1771	8DI	4	Programmable Gain, Signal Averaging, Histogramming, pre/post gate sampling	12 bit	250	Yes	16	Yes
DT1777	4DI	4	Signal Averaging, Histogramming, pre/post gate sampling	16 bit	100	Yes	16	Yes
DT1778	4SE	4	Simultaneous measurements, Signal Averaging, Histogramming, pre/post gate sampling	12 bit	100	Yes	16	Yes

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646.
European Headquarters: Data Translation, Ltd., 430 Bath Rd., Slough, Berkshire SLI 6BB England (06286) 3412 Tlx 849 862.
In Canada: (416) 625-1907.

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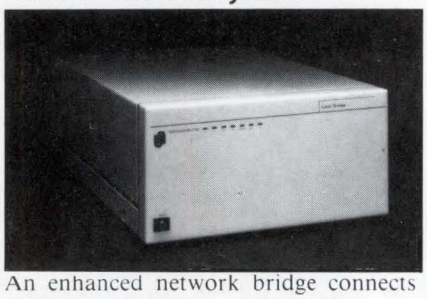
CIRCLE 97

Local bridge increases data transfer rates for Net/One systems



An enhanced network bridge connects multiple Net/One communication systems. Known as the Local Bridge, the product functions as a packet switching node between individual Ethernet/IEEE 802 baseband, and broadband or fiber optic Net/One systems. The Local Bridge consists of network access hardware for each of the two linked nets and a 68000 microprocessor, providing the necessary internetwork intelligence. Virtual circuit and datagram packet transfer speeds exceed 1000 packets/s. Transparent and dynamic packet routing provides automatic adaptation to topology changes. Full duplex operation over transmission facilities occurs at speeds from 9.6 kbits/s to 504 kbits/s. Price is $9850, with software costing $1000 per bridge. **Ungermann-Bass, Inc,** 2560 Mission College Blvd, Santa Clara, CA 95050.

Circle 286

Digital multiplexer offers computing capability

A digital signal conditioning, data acquisition multiplexer with computational power is designated the MP-8400. The device can perform basic math as well as signal select and file functions. Thus, equations that would usually require valuable computer time to solve can be executed within the multiplexer. Equipped for 32-input channels and 64-computational channels, the MP-8400 has a maximum of 512 inputs and 1024 computationals (attainable through daisy chaining). Dual digital output ports for local or remote RS-232-C, RS-422, or 20-mA current loop communications are provided as standard. User configurations, assignments, and calibration data are stored and protected in a nonvolatile memory that requires no batteries. Rates up to 19.2 kbaud are achieved. Inputs are scanned every 2 s. **Rochester Instruments Systems,** 255 N Union St, Rochester, NY 14605.

Circle 287

Advanced data communications derive from network circuit switchers

The Datakit virtual circuit-switch family is composed of the models 500 and 2000. The model 500 packs 100-plus connections within a single-shelf cabinet measuring 15 x 25 x 22 in. (38.1 x 63.5 x 55.8-cm). The 2000, on the other hand, is a four-shelf unit with up to 2500 virtual circuits. Controller and multiplexed host interfaces that are integrated within the Datakit cabinets permit many circuits to be carried over a single high speed channel. Any number of Datakit virtual circuit switches may be linked by optical fibers, copper wire, or both. This enables users to connect buildings within a campus or across the country. **AT&T,** 22 Broadway, New York, NY 10038.

Circle 288

Local network product melds MS-DOS, PC-DOS, and Unix-based micros

ViaNet is a local area network software product that links MS-DOS, PC-DOS, and Unix-based microcomputers. ViaNet offers a fully distributed architecture, application software compatibility, and hardware independence. ViaNet claims support for Ethernet, ARCnet and Proteon's Pronet, among others. A network interface card is required for each machine, as well as an appropriate transmission bus (coaxial cable, twisted-pair wire, or fiber optic cable). A minimum 192-Kbyte RAM configuration is also required. **Vianetix, Inc,** 5766 Central Ave, Boulder, CO 80301.

Circle 289

Multiplexers connect serial lines to VAX and PDP-11 machinery

Two asynchronous multiplexers connect serial lines to Unibus-based VAX and PDP-11 computers. The DHU11 interfaces up to 16 asynchronous PDP-11 or VAX lines to an integral Unibus operating under Version 4.0 of VAX/VMS. Its sibling, the DMZ32, supports as many as 24 asynchronous lines to Unibus-based VAX machines. The two multiplexers enable users to address medium to high performance communication requirements. The DHU11 connects to external equipment through RS-232-C and RS-432-A interfaces, while featuring DMA and FIFO operations that reduce CPU overhead associated with terminal communications. The DMZ32 multiplexer allows a terminal distribution panel to be located as far as 5000 ft from the multiplexer's Unibus connection in the computer system. The DMZ32 has 24 RS-232-C connectors. It also features DMA and FIFO operation. The DHU11 is priced from $3120; the DMZ32, from $3215. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.

Circle 290

Front end drives subsystem for 9000 graphics line

A self-contained network communications subsystem for the 9000 line of graphics workstations implements TCP/IP Ethernet protocols. This frontend communications processor offers advantages within the Unison network environment that include reduced load on the workstation CPU and improved use of memory. The link allows file and resource sharing with VAX equipment. Price for the device, including software, is $6000. **Cadmus Computer Systems,** 600 Suffolk St, Lowell, MA 01854.

Circle 291

Unit offers flexible performance for multiport communications

A protocol converter for popular asynchronous terminal families is available as either a single-port or multiport configuration. Multiport versions allow expansion up to 16 ports with the addition of cards. Each port is supported by a dedicated microprocessor. IBM Bisync and SNA/SDLC, as well as Sperry Uniscope protocols are supported. Cards for ports can be removed for reprogramming or repair without halting operation of other ports. **JBM Electronics Co,** 6020 Lindbergh Blvd, Hazelwood, MO 63042.

Circle 292

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Rate (Mbits/s)	Carrier freq. (Mhz)	RG-59 (ft.)	RG-11 (ft.)	JT4412J (ft.)	JT4750J (ft.)	T41000J (ft.)
1.0	3	5K	12K	20K	32K	50K
2.0	5	4.2K	9.5K	15K	25K	37.5K

**Quantities of 5000.

Modem M-1

FSK/LSI MODEL 30-0194

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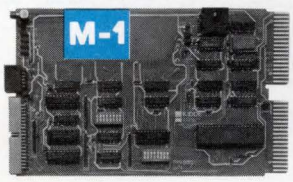
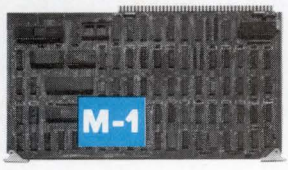
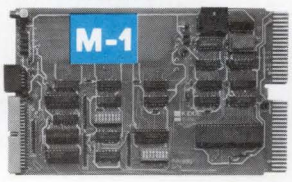


MULTIbus* . . .



UNIbus* . . .



VMEbus . . .

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CIRCLE 98

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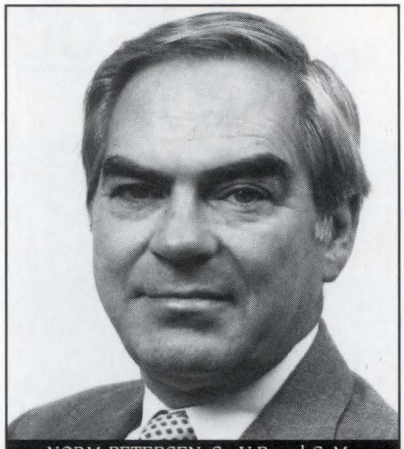

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Jan. 29, '85	Houston, TX
Jan. 31, '85	Dallas, TX
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CIRCLE 99

Software to form core for industrial VAX programs

Baseway software is designed to integrate industrial controllers with manufacturing applications. Three components comprise the Baseway system. First, the Shop Floor gateway is an intelligent hardware/software communication device. It runs on a PDP-11 system and acts as a translator between specific shop floor devices and the host. Allen-Bradley's Data Highway and Gould's Modbus are two protocols that the Shop Floor gateway now handles. The second component, the Baseway application software bus, runs on the VAX/VMS. It communicates with control devices on the shop floor and provides a means of sharing data throughout the factory, while leaving an audit trail. Finally, Programmable Device Support represents the manufacturer application now supported by the software bus. Programmable Device Support is a menu-driven application that is capable of uploading/downloading, reading/writing, comparing, documenting, and maintaining a library of ladder logic programs. Prices for the Baseway set are: $4000 for the Shop Floor gateway, $4000 for the Programmable Device Support, and $18,000 for the Baseway application software bus. The minimum configuration required to run this set includes a VAX-11/750 computer with a VMS operating system and a PDP-11/24 mini with an RSX-11S realtime operating system. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.

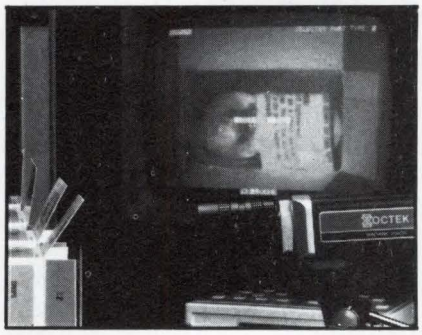
Circle 293

Eurocard-compatible unit offers onboard power-fail logic

GESSBS-4 single-board microcomputers are built around the 8-bit MC6809. The systems reside on a standard single-height Eurocard and are compatible with a G-64 bus. Three 28-pin JEDEC sockets accommodate up to 32 Kbytes of EPROM and 16 Kbytes of CMOS RAM. CMOS RAM can be powered from the standby power line on the G-64 bus. This allows the memory to retain its data when power is turned off or in the case of power failure. A selection of alternate memory pages provides an extended addressing range of up to 28 Kbytes. The GESSBS-4 is supported with full debugger firmware, OS-9 disk operating system, and drivers for Gespac controller boards. The product is available for $495. **Gespac Inc,** 550 E Grandview Dr, Mesa, AZ 85203.

Circle 294

Vision system backed by bubble memory for nonvolatile operation

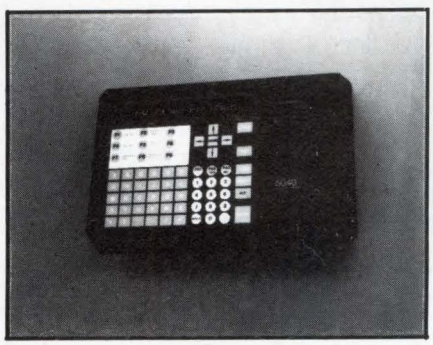


A machine vision system for the inspection and verification world is designed to handle labor-intensive and repetitive visual inspection tasks. Called InVision, the system uses high speed recognition algorithms in performing package inspection. The system sets accurate gray-level transitions for establishing accept/reject parameters. Downline equipment can automatically reject packaging via a communications link with InVision. Multiple-file, nonvolatile bubble memory makes this product well-suited for tough environments. **Octek Inc,** 7 Corporate Pl, S Bedford St, Burlington, MA 01803.

Circle 295

Terminal provides ASCII and 3270 emulation in factory environments

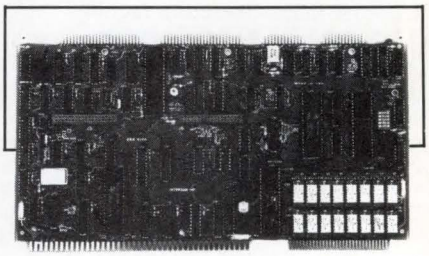
The 5740MT is an intelligent, interactive, online terminal designed to help implement, shop floor control systems. Possible input combinations include keyboards, and magnetic stripe and bar code devices. The 5740MT terminal provides 3270 emulation or interactive ASCII CRT terminal emulation. It can connect directly to a host or utilize a communications processor. Display options include a two-line by 40-char alphanumeric LCD, or a 12-in. CRT supporting a 25-line x 80-char format. **Infolink Corp,** 1925 Hoste Rd, Northbrook, IL 60062.



Circle 296

Extensive interfacing options highlight single-board Multibus system

The ERG 9000 Multibus microcomputer board runs the TMS9995 16-bit microprocessor. It comes with up to 128 Kbytes of onboard RAM and 8 Kbytes of EPROM. The board works in either a single-processor or multiprocessor system. A floppy disk controller and an SASI bus interface allow the user to add Winchester disks and various tape drives, with all transfers supported by the onboard DMA controller. Both I/O and memory-mapped Multibus transfers are handled by the ERG 9000. Two SBX connectors offer additional I/O flexibility. Single- and double-wide multimodules can connect piggyback fashion for added peripheral and controller functions. ERG 9000 features two versions. The ERG 9000-1 comes with 64 Kbytes of RAM (without mapper) and costs $1395. The 128-Kbyte version, which can address up to 1 Mbyte on the Multibus, costs $1695. **Intergon Inc,** 3000 Wilcrest Ave, Houston, TX 77042.



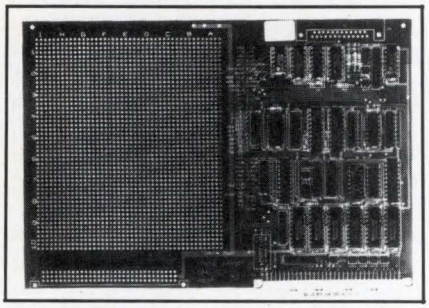
Circle 297

Solids modeler reaps downstream benefits

Cimplex represents a set of software products developed for automated factories. Cimplex modules meet needs in the realm of mechanical parts design, analysis, and manufacturing while integrating information management software. The module set, available for installation in the second quarter of 1985, will feature interactive 2- to 5-axis capability for multipath sculpturing that reduces time and cost associated with numeric control programs. The information management module is used to collect the design and engineering data, perform configuration management, and maintain in a central location files that have been drawn from several CAD systems. The minimum annual license fee for an individual module is $40,000. **Automation Technology Products,** 1671 Dell Ave, Campbell, CA 95008.

Circle 298

Board accommodates custom configurations



The DSSEWRAP board interconnects directly to the VMEbus. This double-Eurocard wire-wrap board leaves 60 percent of the surface free for system development. All chip sizes can be accommodated. Features include address decoding for words up to 32 bits, TTL-compatible buffered inputs for both the address bus and the control bus, and tri-state TTL-compatible buffered I/O for the data bus. The base address is jumper-selectable anywhere in the entire 16-Mbyte memory map. Operation requires 5 and 12 V with maximum power draw set at 3 A. The DSSEWRAP is priced at $495. **Data-Sud Systems/U.S., Inc,** 2219 S 48th St, Tempe, AZ 85282.
Circle 299

Board-level system uses the 286 as a CPU and 186 for I/O

The DPX86/ME board-level computer implements both the Intel iAPX286 and iAPX186. This machine uses surface-mount integration and boasts PC/AT-type performance. The 286 chip runs applications and the 186 handles all I/O. The DPX86/ME has 1 Mbyte of onboard memory and can be configured with up to 216 Mbytes of memory (the full 286 addressing range) via an iLBX bus extension. Additional ROM capacity to 500 Kbytes provides enough operating system and networking storage to open a large area of main memory to the user. An 82586 controller chip is onboard as well. The unit offers the IEEE 802.3 Ethernet local area network as an integrated function. **Little Machines,** 4141 Jutland Dr, San Diego, CA 92117.
Circle 300

LSI-11-type system comes with up to 2.5 Mbytes of memory

The SMS 1000 model 40 is a complete Q-bus compatible, Winchester-based microcomputer system that uses SMS Foundation architecture. It consists of a system enclosure, a choice of fixed and removable peripherals, and LSI-11 processors and memory. It runs system and applications software developed for the LSI-11/23 or /73 CPUs, without modification. The support monitor subsystem within the Foundation module contains resident firmware and hardware used for system status analysis, utilities, and diagnostics. The model 40 contains a quad-wide, 22-bit Q-bus backplane with six usable slots. It emulates the handler and device driver via a mass storage control protocol. The model 40 comes with either LSI-11/23 or /73 CPUs, and up to 2.5 Mbytes of main memory. Two serial communication ports are standard. Realtime and time-sharing systems supported include RT-11, RSK-11M-Plus, and RSTS/E Unix. Pricing starts at $5800. **Scientific Micro Systems, Inc,** 339 N Bernardo Ave, Mountain View, CA 94043.
Circle 301

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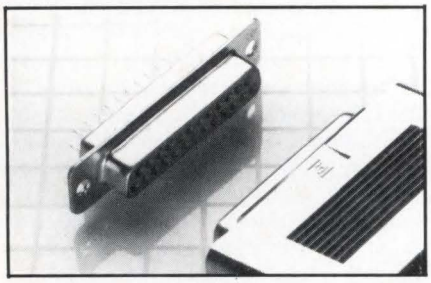
Have you written to the editor lately? We're waiting to hear from you.

SYSTEM ELEMENTS

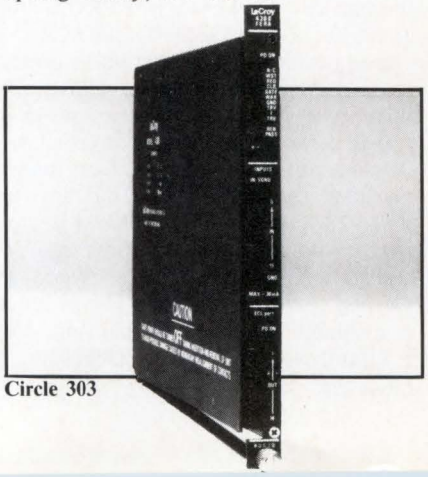
Sockets compatible with military standard D-type connectors



Metal shell straight sockets in the FCN-774J series provide compatibility with military standard D-type connectors. The shielded metal shells made of Nickel-plated steel ensure emi protection. UL-reconginized materials are used. Temperature range is set at −55 to 105 °C. The socket has a current rating of 3 Adc and a dielectric withstanding voltage of 250 Vac for 1 min. They cost $3 each in lots of 100. **Fujitsu America, Inc, Components Div,** 918 Sherwood Dr, Lake Bluff, IL 60044.
Circle 302

Fast encoding and readout ADC offers 8.5 μs conversion

Accuracy to 11-bits merges with 8.5 μs conversion in the model 4300 and 4302 A-D converters. Applications range from high speed data acquisition to analog data integration and realtime industrial process control. This fast encoding and readout system permits hundreds of sources of analog signals to be digitized with accuracy of up to 0.05 percent (or 11 bits). The signals can be corrected for dc offsets and transferred into a buffer memory or programmable processor. The heart of the system is an A-D converter module that simultaneously performs a digital conversion on 16 separate analog signals. Under remote control, converted data may have pedestals subtracted and empty channels deleted. Data can be read at speeds of up to 100 ns per word. **LeCroy Research Systems Corp,** 7000 S Main St, Spring Valley, NY 10977.



Circle 303

IGNORANCE IS NO EXCUSE.

America's declining productivity is serious business. It's about time we all got serious about it.

America's productivity growth rate has been slipping badly for several years now, compared to that of other nations. And it's adversely affecting each and every one of us.

We've all seen plants and businesses close down. Tens of thousands of jobs lost. Prices rising, quality deteriorating. A flood of foreign-made products invading our shores. It's all part of our declining productivity rate.

We've simply got to work it out—and we've got to work together to do it. But first, we need to know more about the problem and the possible solutions so we can act intelligently and effectively.

That's why you should send for this informative new booklet. It hasn't got all the answers—there are no quick and easy ways out—but it's a very good place to start the productivity education of yourself, your associates and your workers. It's free for the asking—and in quantity. Mail the coupon right away. Ignorance is no excuse.

Ad Council

A public service of this publication and the American Productivity Center.

A

National Productivity Awareness Campaign
P.O. Box 480, Lorton, VA 22079

Yes, I would like to improve my company's productivity. Please send me a free copy of "Productivity: the crisis that crept up on us." (Quantities available at cost from above address.)

Name_____

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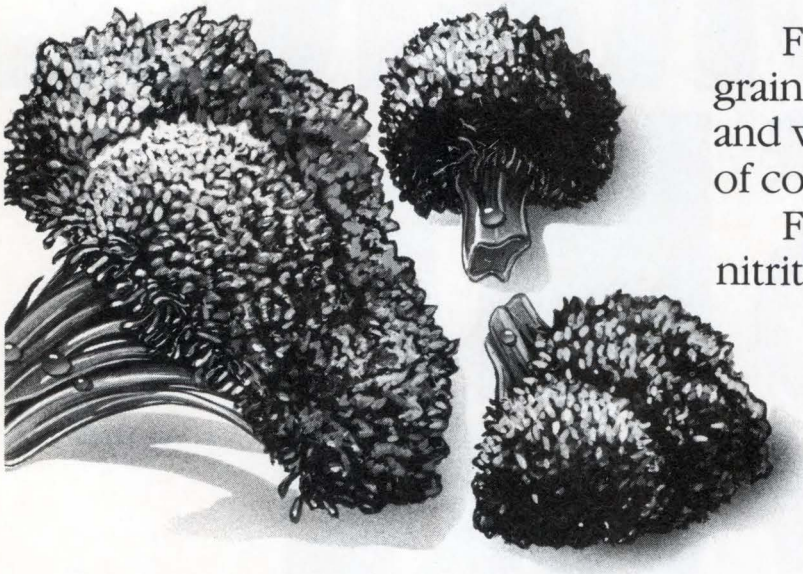
City_____ **State**_____ **Zip**_____

Please allow 4-6 weeks for delivery.

America. Let's work together.

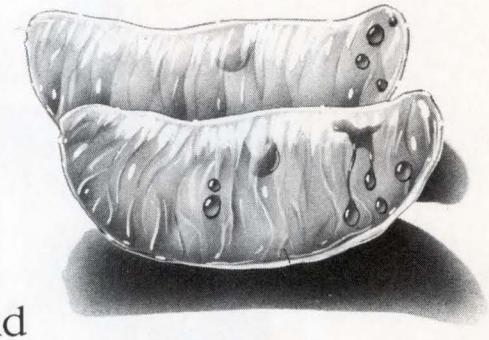
THIS SPACE CONTRIBUTED AS A PUBLIC SERVICE

A defense against cancer can be cooked up in your kitchen.



Fruits, vegetables, and whole-grain cereals such as oatmeal, bran and wheat may help lower the risk of colorectal cancer.

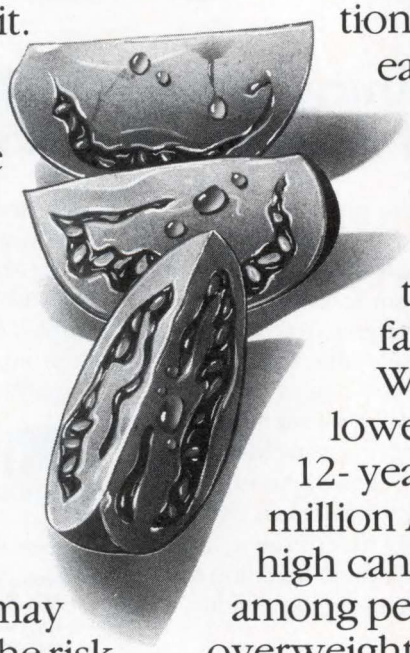
Foods high in fats, salt- or nitrite-cured foods like ham, and



fish and types of sausages smoked by traditional methods should be eaten in moderation.

There is evidence that diet and cancer are related. Some foods may promote cancer, while others may protect you from it.

Foods related to lowering the risk of cancer of the larynx and esophagus all have high amounts of carotene, a form of Vitamin A which is in cantaloupes, peaches, broccoli, spinach, all dark green leafy vegetables, sweet potatoes, carrots, pumpkin, winter squash and tomatoes, citrus fruits and brussels sprouts.



Be moderate in consumption of alcohol also.

A good rule of thumb is cut down on fat and don't be fat.

Weight reduction may lower cancer risk. Our 12-year study of nearly a million Americans uncovered high cancer risks particularly among people 40% or more overweight.

Foods that may help reduce the risk of gastrointestinal and respiratory tract cancer are cabbage, broccoli, brussels sprouts, kohlrabi, cauliflower.

Now, more than ever, we know you can cook up your own defense against cancer. So eat healthy and be healthy.

No one faces cancer alone.

AMERICAN CANCER SOCIETY®

DG One connects to minis and mainframes via diskette software

The Blast family of generic communications software covers universal file transfer and terminal mode access for a range of minis and micros that include Data General's One notebook portable. Blast software allows the portable to transfer binary data, text data, or commands with machines that include the MV 1000. This software also provides file transfer capability between the DG One and the DG CEO system. Held on a 3½-in. diskette, this version of Blast software costs $250. **Communications Research Group,** 8939 Jefferson Hwy, Baton Rouge, Louisiana 70809.

Circle 304

Faster operation and advanced graphics mark integrated offering

KnowledgeMan integrates a third-generation spreadsheet, statistical analysis, printed form management, and screen management with a structured programming language and a relational data base management system. Highlights include an online help facility with over 6800 lines of text and more than 380 help screens. A language learning feature enables the system to learn the user's own terminology (eg, jargon, slang, or foreign words and phrases). An enhanced mouse option supports the Microsoft mouse in spreadsheet processing, forms painting, and text processing. KnowledgeMan also featues dynamic form positioning, which allows multiple multicolored forms to be displayed in positions chosen at run time. **Micro Data Base Systems, Inc,** PO Box 248, Lafayette, IN 47902.

Circle 305

Compiler library for C improves string handling

The Greenleaf Functions Version 2.0 library features over 220 functions and routines for C programmers. For the PC or XT, this release includes functions coded in Assembler for improved speed and code density. Major C compilers supported include Computer Innovations C86, Lattice C, and MicroSoft C, and the Mark Williams C development system. The library helps PCs to interface with mainframes, minis, and other PCs. String manipulation functions include replace, extract, insert, delete, find and blank characters or words—generalized from left to right. All IBM graphics printer capabilities are supported. **Greenleaf Software Inc,** 2101 Hickory Dr, Carrollton, TX 75006.

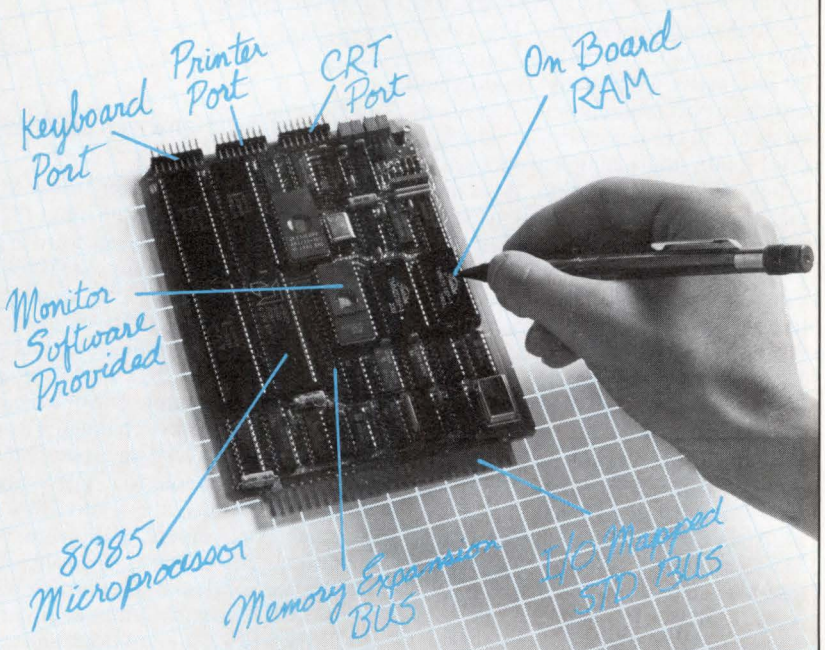
Circle 306

Terminal emulation software package links micros to mainframe graphics

SmarTerm 125 enables the IBM PC to connect to mainframe graphics software packages. PC compatibles are also covered. The program supports the ReGIS graphics protocol of the VT125 and also allows the PC to function in a VT100, VT101, VT102, or VT52 mode. File transfer functions built into SmarTerm 125 let the user put received data into a disk file and transfer either ASCII or binary files to the host without special system software. **Persoft, Inc,** 2740 Ski Lane, Madison, WI 53713.

Circle 307

SMART CRT CONTROLLER ON STD BUS



Cubit's new I/O Processor controls a CRT, printer and keyboard.

Using an 8085 microprocessor with its own memory, the board frees your system CPU to race ahead of slower peripherals. Terminal-like commands permit easy communication between this smart controller and the host-processor.

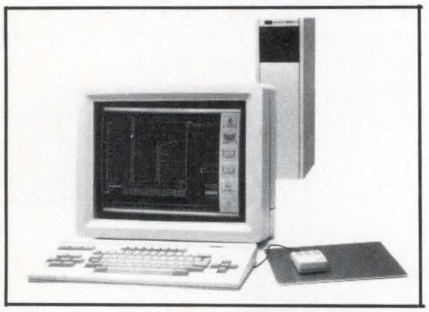
Bring distributed processing to your STD Bus system for $345 in single quantity. With stock to two week delivery, you won't have to wait long.

CuBIT INC.
Division of Proteus Industries

190 South Whisman Road, Mountain View, CA 94041
Telephone: (415) 962-8237

CIRCLE 102

Workstations match the 68010 with up to 2.5-Mbyte internal memory



The CDX-5000A represents a lower cost version of the CDX-5000. Using the same 32-bit, 68010-based architecture, the system includes 1.5 Mbytes of internal memory, expandable to 2.5 Mbytes, with a virtual operating system. The system allows automatic and manual placement, fast interactive and manual routing, and automatic back-annotation. Software includes an object-oriented user interface, netlist input, and a complete package for tooling and documentation. Also available, the CDX-50000 is a high performance offering for printed circuit board design. It features a Graphics Accelerator Engine, a hierarchical schematic editor, plus automatic placement and routing software. The engine is based on a bit-sliced processor with an 88-bit- wide microcode word, enabling up to 400,000 clips and transforms per second. It performs fast graphics operations, even on boards in the 700 IC range. The CDX-50000 is priced at $79,900. The CDX-5000A goes for $49,900. **Cadnetix Corp,** 5757 Central Ave, Boulder, CO 80301.

Circle 308

Plotter and controller improve graphics operation

The 1044 dual-mode plotter and the 955 controller have joined a graphics product line. The 1044 provides A- through E-sized drawings on cut-sheet or roll-fed media. Eight pens move at 14 in./s. Price is $11,995, with discounts available. The 955 vector controller delivers shared resource plotting. It is designed for use with the 5700 series of electrostatic plotter/printers and relieves the host computer of the burden of vector-to-raster conversion. Bit-slice technology produces an output transfer rate of up to 500 Kbytes/s and a raster speed of up to 1 million raster elements/s. **Calcomp,** 2411 W La Palma Ave, Anaheim, CA 92801.

Circle 309

Protocol analyzer studies diverse interfaces, comes in lightweight unit

A portable protocol analyzer, dubbed the VP-3682P, troubleshoots and analyzes faults in a data comm network. It can record and store data in its 64-Kbyte memory and display this data on a CRT without affecting online status. The machine weighs 22 lb (10 kg). Optional interfaces include X.20, X.20 bis, and RS-232-C (V.24). Protocol translation can be done according to CCITT X.25 level 2 or 3 (with display in mnemonic code). Idle suppress function and idle time display are other significant features. The VP-3682P can be enhanced with ROM-pack and simulation options. **Panasonic,** One Panasonic Way, Secaucus, NJ 07094.

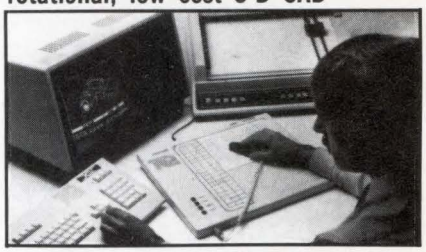
Circle 310

Benchtop logic analyzer provides 40 channels of input

A benchtop logic analyzer, the PALAS 40C50, has 40 channels of input (32 for data collection plus 8 trigger word expansion channels). It is a composite (state and timing) logic analyzer with all channels operating in synchronous or asynchronous mode. As a timing analyzer, the 40C50 can operate 16 channels at a 50 MHz maximum sample rate at a memory depth of 2000 bits per channel. The timing display shows all data inputs with 100 percent timing resolution. For synchronous applications, the unit offers two external clock inputs, each with three qualifiers. The 40C50 is especially suited to coprocessor designs. Features include: a 9-in. CRT, asynchronous sampling to 100 MHz, RS-232 and GPIB links, and nonvolatile setup memory. Microprocessors supported include the Z80, 8080, 8085, the 68000, and the 8086/88/186. The 40C50 costs $3950. **Dolch Logic Instruments, Inc,** 2029 O'Toole Ave, San Jose, CA 95131.

Circle 311

Design system provides fully rotational, low cost 3-D CAD



Fully rotational three-dimensional design is possible on a 68000-based machine called the TQ Continuum System. This unit also offers word processing, spreadsheet, and database programs. A high resolution 12-in. monochromatic monitor and dual 8-in. disk drives are complimented by 330 Kbytes of RAM. A full keyboard, digitizing pad, eight-color plotter, and menu-driven CAD program complete the basic system. A proprietary, variable two-dimensional menu is used to store two-dimensional primitives—automatically drawn from coordinates—for later recall. Standard symbols can be drawn once, then stored. Objects can be viewed from any angle and perspective by entering viewpoint data. Four windows are available to monitor or plot all views simultaneously. Other three-dimensional options include exterior and interior eye-level views and topographic projections for multistructure relationships. Total system costs range from $15,000 to $20,000. **TecQuipment Inc,** PO Box 1074, Acton, MA 01720.

Circle 312

Uniform development environment derives from Pascal compiler

A new version of the Oregon Software Pascal-2 compiler for the Digital Equipment Corp VMS operates across DEC's full line of micros, minis, and superminis. Pascal-2 runs on the VAX, the PDP-11 (with its RSX, microRSX, RSTS/E, Unix, RT-11, and TSX-Plus operating systems), and the Pro 350 RT-11 operating system. Pascal-2 is also available for 68000-based Unix systems. Using the compiler, source code remains essentially intact and the development scheme—editing, compiling, linking and debugging—is identical on all systems. The debugger allows the programmer to solve logical errors in applications code using Pascal notation. Pascal-2 for VMS is available now with license fees beginning at $4950. **Oregon Software, Inc,** 6915 SW Macadam Ave, Portland, OR 97219.

Circle 313

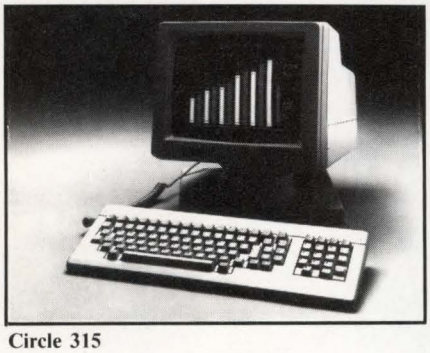
Graphic displays and controllers update PC performance

IBM PC professional graphics displays and controllers handle up to 256 colors simultaneously. The controllers have two modes: current PC color graphics emulation mode and expanded graphics mode. Pixel definition hits 640 x 480, with the color palette listed at 4096. Built-in hardware capabilities take care of two- and three-dimensional drawing. The RGB display sports flicker-free performance and a noninterlaced 60-Hz refresh rate. These devices run on the XT, AT, and on the PC expansion unit. The display is priced at $1295 and the controller at $2995. **IBM, Information Systems Group,** 900 King St, Rye Brook NY 10573.

Circle 314

Terminals convert PCs into time-sharing multi-user systems

The KT-7/PC uses an IBM PC character set and has nonembedded PC-compatible video attributes. This unit provides proprietary features, including 25 display lines that can be scrolled and addressed. Tilt, swivel, and height adjustment of the monitor is provided, as well as a serial printer port. Standard ASCII terminal emulation is provided for other general terminal requirements. The product offers a four-page memory option. The KT-7/PC costs $895, with quantity discounts available. A plain KT-7 version goes for $595. **Kimtron Corp,** 2225-I Martin Ave, Santa Clara, CA 95050.



Circle 315

Card-based security devices function as subsystems in critical applications

Codercard security system integrated into any type of computer network or data communications environment and reliably monitors access attempts and authenticates system users. The Codercard system combines hardware and software, interchanging data between user subsystems and a central verification subsystem. Centered around a device slightly larger than a credit card, the Coder Card contains a microprocessor, 128 bytes of RAM, and 2 Kbytes of ROM. The card inserts into a base unit that connects to a host via standard RS-232 interface. Each Codercard contains a unique identification and DES-based algorithms. The unit runs at up to 19.2 Kbits/s. Codercards are priced from $80 to $100 in quantities of 1000 or more, and card readers range from $150 to $170 in the same quantities. **Codercard, Inc,** 2901 Redhill Dr, Costa Mesa, CA 92626.

Circle 316

REYE SYNDROME

Reye syndrome is a ***rare but dangerous*** condition that can develop from ***flu or chicken pox.*** It occurs mainly in ***children under 16,*** usually when they ***appear to be recovering.*** Watch for these signs:

- ***Persistent vomiting***
- ***Fatigue***
- ***Confusion and belligerence.***

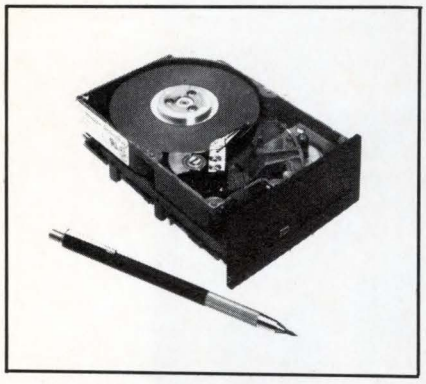
If your child displays any of these symptoms, ***consult a doctor immediately.***

Some studies indicate that there may be an association between the use of ***aspirin*** for flu and chicken pox and the development of Reye syndrome. Further studies are being conducted on this possibility. In the meantime, the ***U.S. Surgeon General*** suggests that you check with your doctor before using aspirin or any medication when your child has flu or chicken pox.

—A message from the Food and Drug Administration.

Winchester drives in 3½-in. form factor offer 10-Mbyte capacity

The ST112 is a 10-Mbyte, 3½-in. Winchester disk drive that supports the ST412 interface. The drive uses two platters. Unformatted drive capacity measures 12.76 Mbytes—3.19 Mbytes per surface and 10,416 bytes per track. Access time for the unit is 20 ms track-to-track, with average latency set at 8.33 ms. Average access time, including settling, is 65 ms. Seagate has also released the ST225—a 20-Mbyte, 5¼-in. half-height drive. This unit has an advanced stepper motor, a metal band actuator, and an onboard microprocessor with a buffered seek mode that provides an average access time of 85 ms, including settling. **Seagate Technology,** 920 Disc Dr, PO Box 66360 Scotts Valley, CA 95066.



Circle 317

Family of Winchesters sports access times averaging 30 ms

Full-height, 5¼-in. Winchester disk drives with storage up to 85.3 Mbytes make up the 6000 family. The group is comprised of four models—the 6085 with unformatted storage capacity of 85.3 Mbyte, the 6074 with 74.7 Mbytes, the 6053 with 53.3 Mbytes, and the model 6032 with 32 Mbytes. Model 6000 drives feature a dual-chassis construction that protects the head-disk assembly from shock and vibration. All these drives have an average access time of 30 ms. A patented breather filter and recirculating air filter creates a clean, pressurized operating environment for heads and disks. Features include mini-Winchester heads, automatic actuator lock, and an ST412-compatible interface. **Miniscribe Corp,** 1861 Lefthand Cr, Longmont, CO 80501.

Circle 318

Removable bubble cassette means 1-Mbyte solid state storage

The compact BCK 10 is a bubble memory cassette that can be removed for transport. It contains no moving parts and offers bubble technology's proven virtures in harsh realms. The BCK 10 has 1 Mbyte of mass storage memory. Operating temperatures range from 10 to 50 °C. The part is available for $530 in 100-unit lots. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 319

Streaming tape backup sports file-oriented operation

The MT-25 represents a file-oriented, streaming cartidge tape backup unit incorporating the Cipher model 526. The 526 is a 25-Mbyte drive packaged with a software interface that emulates a floppy disk interface and responds to floppy commands. The file-oriented setup allows backup or restore of individual files, groups of files, or an entire disk (including subdirectories), along with time and date stamping. Data moves between a hard disk and the tape drive at up to 1 Mbytes/m. The MT25 plugs directly into the IBM PC floppy disk controller's external connector. The price is about $1050. **Microsystems International Corp, a unit of Alloy Computer Products, Inc,** 100 Pennsylvania Ave, Framingham, MA 01701.

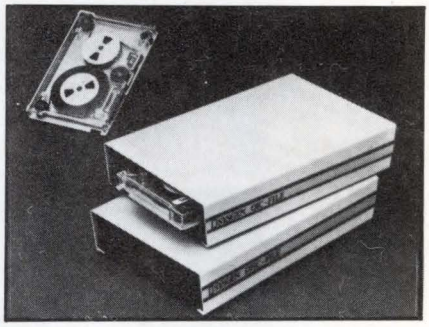
Circle 320

VMEbus memory board offers 1 Mbyte of RAM and fast long-word cache

A 1-Mbyte dynamic RAM board, designated the MK75702, is VMEbus compatible and features a longword cache with typical read access time of 135 ns on a cache hit, and 300 ns on a cache miss. It is billed as a second-generation VMEbus product. The board is capable of byte (8-bit), word (16-bit), or longword (32-bit) data transfers. It is also available with parity generation and checking. The MK75702 contains a control and status register that allows onboard option selection by software. Additional features include 23-bit address, programmable or boot-strapped starting address, an access- and status-LED indicators. Address modifiers are decoded in a PROM, allowing customized address modifiers. This 1-Mbyte DRAM board is priced at $3500, with discounts available. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 321

Streaming tape backup protects via mirror-image and file-by-file modes

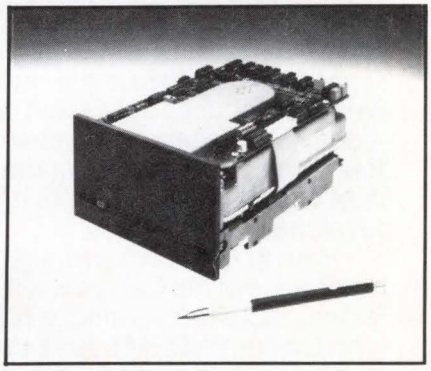


Backup for the IBM PC, XT, and AT is provided by a low cost 45-Mbyte cartridge tape system called the Qic-File. The unit offers mirror-image backup and file-by-file backup. These modes allow verification on-the-fly and continuous diagnostics on the tape unit's double heads. Reports put the Qic-File read/write speed at 90 in./s and transfer rate at about 90 Kbytes/s. The Qic-File supports the Qic-24 recording format and records in a nine-track serpentine mode. Price of an internal version is $1395, while an external model is $1495. **Sysgen, Inc,** 47853 Warm Springs Blvd, Fremont, CA 94539.

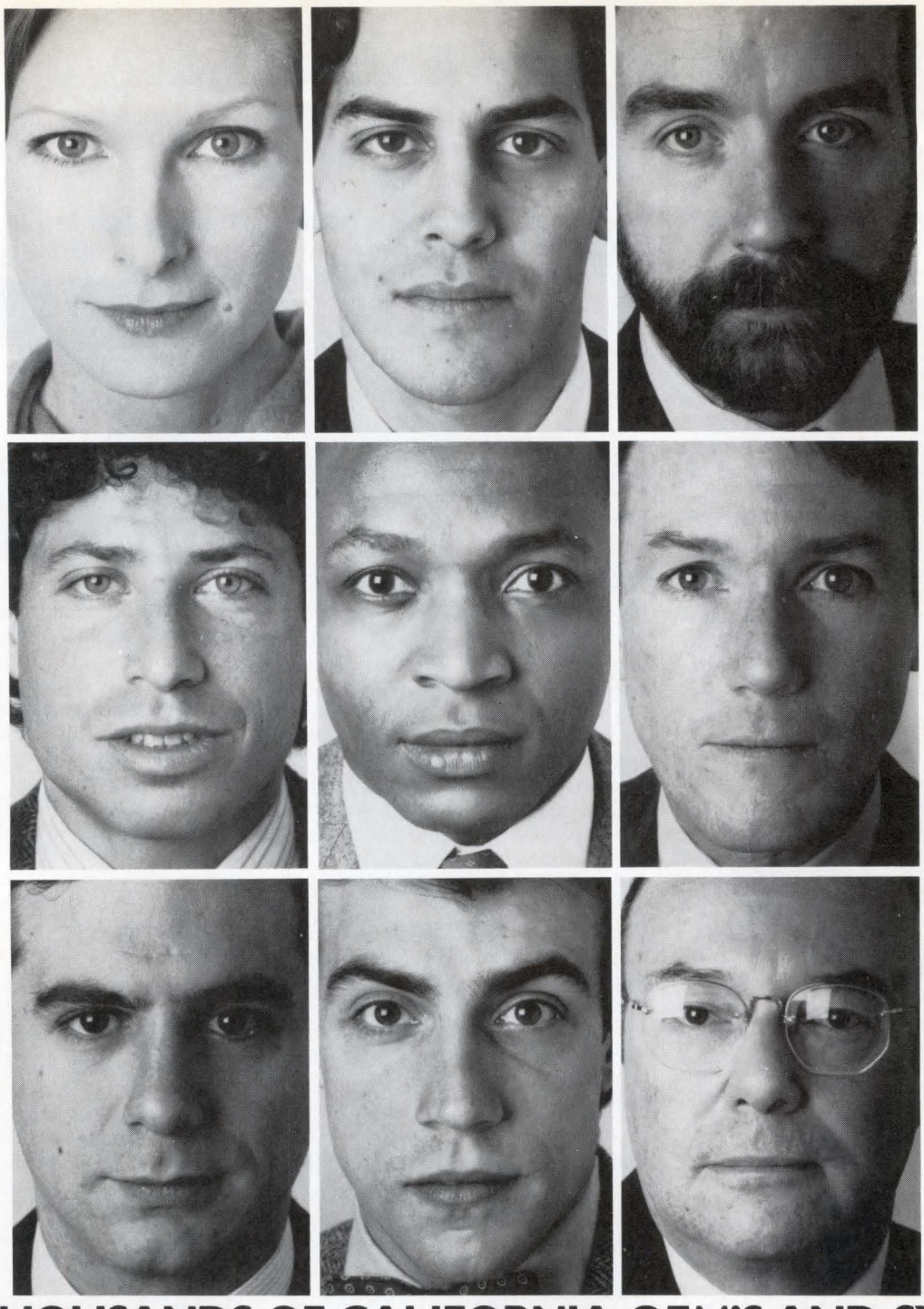
Circle 322

Disk drive with closed-loop positioning stores 40 Mbytes

The ST4051 represents a 40-Mbyte, full-height disk drive memory. The unit features closed loop positioning. It incorporates a voice coil actuator and supports the ST412 interface. Average access time is 40 ms. Soft read errors for the ST4051 are listed at 1 per 10^{10}. Three disks and five read/write heads are employed in the unit. The machine runs at temperatures of 50 to 113 °F. **Seagate Technology,** 920 Disc Dr, PO Box 66360, Scotts Valley, CA 95066.



Circle 323



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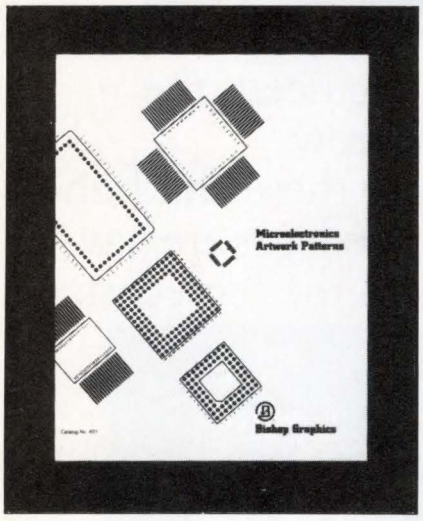
CIRCLE 105

PC board artwork



A microelectronic line of artwork patterns is described in a catalog of packages. These include hybrids, surface-mounted devices, ICs, and small outline transistors. Custom manufacturing capabilities are also portrayed. **Bishop Graphics, Inc,** Westlake Village, Calif.
Circle 410

Emissions specs

A brochure on FCC emissions specs consists of eight short questions and answers. Problems associated with the recent drive toward interference reduction are covered. **TKC,** Pinellas Park, Fla.
Circle 411

Modem advance

Type 9648 modems are featured in a full-color leaflet. Offering transmission at 4.8, 7.2, and 9.6 kbits/s over four-wire leased circuits, the type 9648 has an integral four-port multiplexer option. **Thorn EMI Datatech, Ltd**, Middlesex, England.
Circle 412

Conversion tract

Specification and technical information for data bus products and converters for A-D, D-A, synchronous-to-digital, and digital-to-synchronous converters are noted in a short form catalog. **ILC Data Device Corp**, Bohemia, NY.
Circle 413

International modem protocol update

Recent modem standards are among topics covered in the revised edition of the "V-series Report" from Bootstrap. CCITT recommendations are described in practical terms. **Glasgal Communications, Inc,** Northvale, NJ.
Circle 414

A guide to the T-1 scene

Primer aids designers in the use of T-1 carrier devices and PCM systems. Specific application examples describe features of T-1 devices. **Rockwell International, Semiconductor Products Div**, Newport Beach, Calif.
Circle 415

Electronic measuring instruments

A 48-page, 1984/85 engineering catalog is available for a line of electronic measuring instruments. Detailed specs cover over three dozen different measuring instruments, including logic analyzers, a digital oscilloscope, and digital plotters. **Panasonic Industrial Co,** Secaucus, NJ.
Circle 416

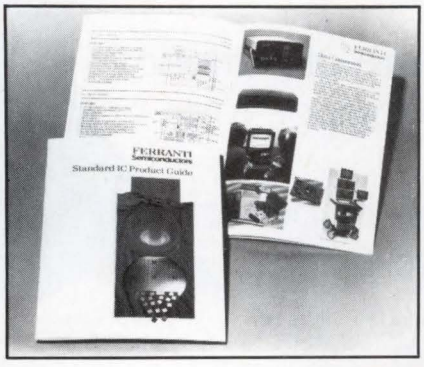
Standard cells in focus

The SCAN newsletter seeks to bring coherence to the standard cell scene. With a tutorial style, the newsletter provides data on unfolding standard cell developments. **International Microelectronic Products,** San Jose, Calif.
Circle 417

Technical courses

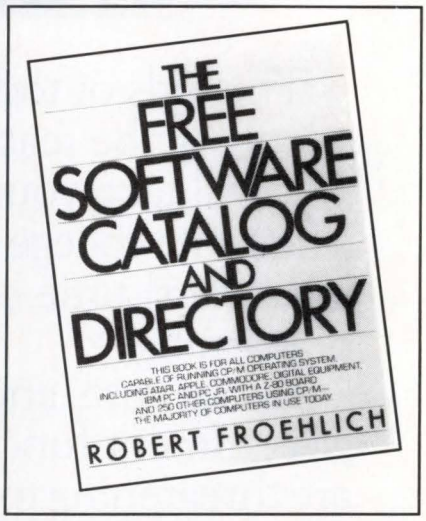
Special interest short courses covering computer graphics, knowledge-based systems, and effective technical management are among the items depicted in a brochure from Integrated Computer Systems. These four-day courses are offered throughout the U.S., Canada, and Europe. **Integrated Computer Systems,** Los Angeles, Calif.
Circle 418

IC products guide



Ferranti Semiconductors has published a guide to its IC products. Listed are data conversion devices, as well as telecommunication chips and voltage devices rated from 2.45 to 10 V. **Ferranti Semiconductors,** Commack, NY.
Circle 419

Public domain software



Free or public domain software is listed in a 256-page catalog. Focus is on software from the CP/M Users Group and the Special Interest Group for Microcomputers. Included are business programs, educational and database software, plus automation and productivity enhancing programs. Price is $9.95. **Crown Publishers, Inc,** One Park Ave, New York, NY 10016.

Protocol conversion guide

Technical background information on protocols and protocol conversion is available in a data communication booklet that includes text, diagrams, and illustrations. SNA protocols receive special treatment. **Timeplex, Inc.** Woodcliff Lake, NJ.
Circle 421

Surge testing

A two-page bulletin and application note describes equipment and methods for surge testing telecommunications gear. Necessary surge waveforms, energy requirements, coupling methods, and diagnostic measurement techniques are covered. **Key Tek Instrument Corp,** Burlington, Mass.
Circle 422

Multilevel pipeline registers

Data sheets showing the 16-bit CMOS LPR520 and 521 pipeline registers are available. Design information is given for both circuits—including pin configuration and description charts, functional and timing diagrams, package drawings, and tables outlining electrical and switching characteristics. **Logic Devices Inc,** Sunnyvale, Calif.
Circle 423

Watch your investment grow.

The kids of today are the doctors, the engineers, the scientists, the teachers, the leaders of tomorrow.

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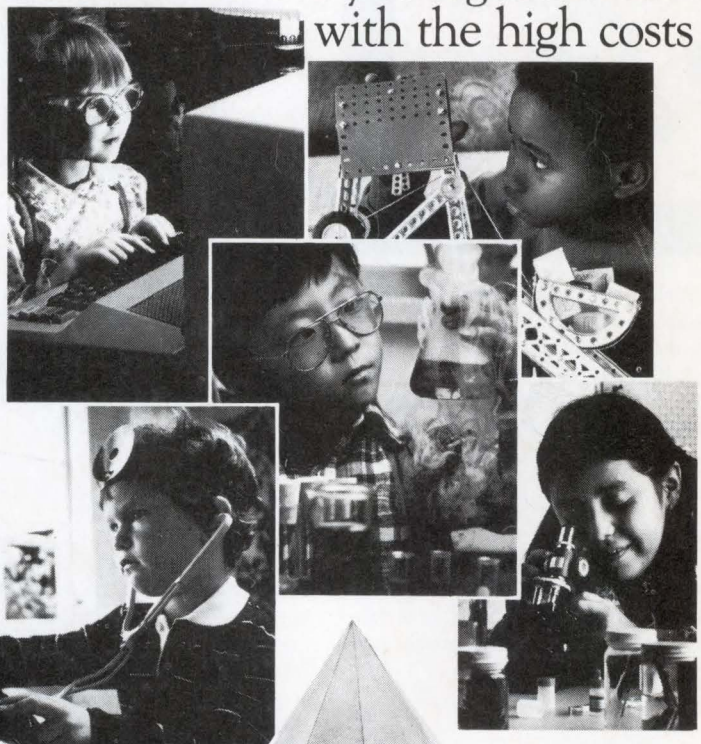
Rising costs and less government funding are threatening to lower the quality of higher education and reduce the number of well-qualified college graduates.



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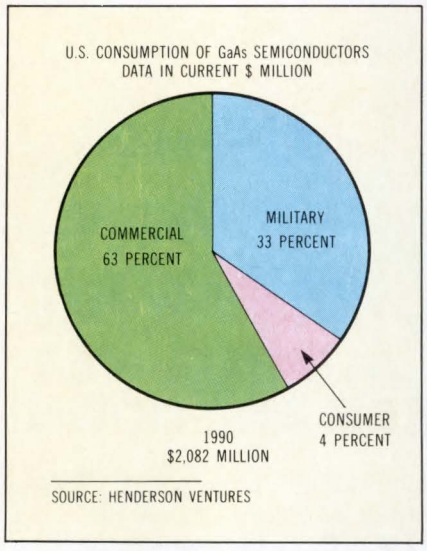
Gallium arsenide semiconductors

By the end of the decade, commercial gallium arsenide applications will surpass the military applications that this technology has been dependent on, according to the *Henderson Electronic Market Forecast.* While nonmilitary uses now account for 26 percent of the $106 million GaAs semiconductor market, the nonmilitary segment will equal 63 percent in 1990, when the estimated dollar value of the entire GaAs market hits over $2 billion. Still, the Henderson firm projects that GaAs will only account for 6 percent of overall U.S. semiconductor consumption, with silicon-based products continuing to hold the lion's share. Large computers, microwave communications, and instruments stand out among GaAs uses. The report foresees special difficulties for interconnection product vendors working in the GaAs realm. PC board makers, in particular, will have to rethink present designs



to cope with the material's faster switching speeds. *The Henderson Electronic Market Forecast* is published monthly. Annual subscription price is $750. **Henderson Ventures,** 101 First St, Los Altos, CA 94022.

Circle 469

Rigid disk drives

Worldwide shipments of fixed 5¼-in. drives will reach 2.3 million units in 1984, up 105 percent from 1983's 1.1 million figure, according to the *Disk/Trend 1984* report. Shipments of full-size, 5¼-in. drives with less than 30 Mbytes are expected to peak in 1985 as production of half-height versions picks up steam. The report anticipates that the share of worldwide OEM unit shipments held by U.S. manufacturers will drop from about 81 percent in 1983 to 62 percent in 1987. Recent Japanese successes in the 100- to 300-Mbyte range will be complemented by that country's incursions in 3½-in. disk manufacturing. By 1987, 3½-in. drives will lead other small fixed-media drives in worldwide shipments, according to the report. Subscriptions to the 1984 Disk/Trend report are available for $1530. **Disk/Trend, Inc,** 5150 El Camino Real, Los Altos, CA 94040.

Circle 470

CAD/CAE for IC design

IC design will steadily shift from the IC manufacturer to system designer over the rest of the decade, with 90 percent of IC design dependent on CAD/CAE tooling by 1990. These projections form the heart of *The Impact of CAD/CAE on IC Design,* a report from Electronic Trend Publications. Hidden costs and current inadequacies of present CAD/CAE systems are sized-up in the report, as well as the developing technology's impact on departmental and company-wide organization. ETP anticipates that CAD workstation prices will decline from today's $60,000 to $75,000 range to about $14,000 to $26,000 in 1990. The report may be ordered for $795. **Electronic Trend Publications,** 10080 N Wolfe Rd, Cupertino, CA 95014.

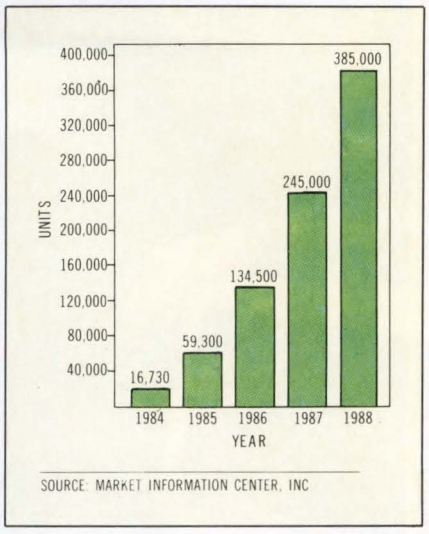
Circle 471

Interactive videodisk systems

Interactive videodisk-based systems may soon gain acceptance in public location applications. Indications are, according to Link Resources, that interactive videodisks work well in such public settings as airports and department or specialty stores. The research firm puts the present U.S. videodisk-based point-of-sale installation figure at over 1000 units, with an aggregate installation base of 113,000 units projected over the next five years. Computer stores are seen as an early market for the systems because of the complexity required for microcomputer and software sales pitches. In related developments, some observers see that interactive videodisks in public settings are increasingly being configured with touch-screen input capabilities. International Resource Development, Inc expects a $48 million market in 1986. Observers expect public sector applications to account for a large part of this growth. The report on videodisks in electronic selling is available from **Link,** 215 Park Ave S, New York, NY 10003.

Circle 472

VMEbus boards



A market census sponsored by *Computer Design* takes a look at the potential of the VMEbus. Value in 1984 for all types of VMEbus boards shipped ranges from about $65 million to $70 million worldwide, according to the study. Prepared by the Market Information Center, Inc, the study measures 1983 VMEbus shipments at 5395 units, with units shipped in 1987 expected to reach 245,000. Although the percentage of VMEbus products today hits approximately 60/40 in favor of non-U.S. markets, this ratio is likely to change rapidly. The study's authors foresee a reversal of the 60/40 figure as U.S. VME markets expand through 1988. The VMEbus marketplace study is available for $295. **Market Information Center, Inc,** 100 Pennsylvania Ave, Framingham, MA 01701.

Circle 473

Integrated software packages

Demand for personal computer-based integrated software packages will exceed 3.6 million units in 1988, compared to 445,000 unit sales in 1983, according to Venture Development Corp. This is foreseen by VDC in its report: *Integrated Software for Personal Computers, 1983-1988.* The firm estimates that nearly half of present day integrated software sales are handled by computer stores, with the direct manufacturer and mail order venues each holding about 22 percent of the end-sale market. VDC sees computer store personnel sorely taxed by the demands this sophisticated integrated software sales growth implies. The study sells for $2650. **Venture Development Corp,** 1 Washington St, Wellesley, MA 02181.

Circle 474

Photo courtesy Personal CAD Systems, Inc.

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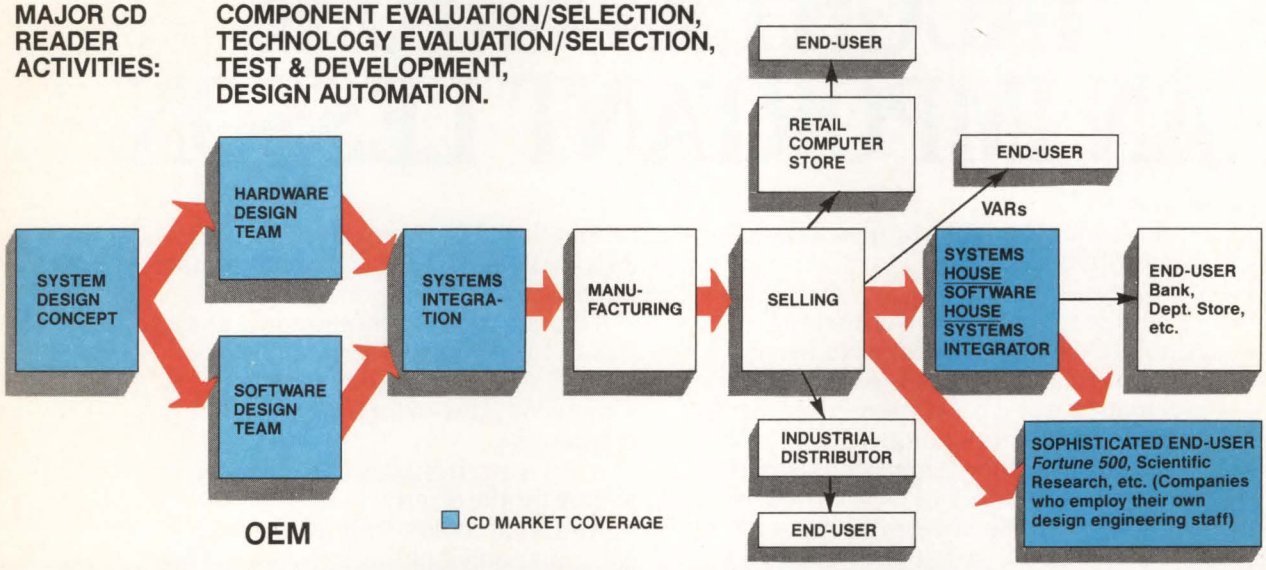

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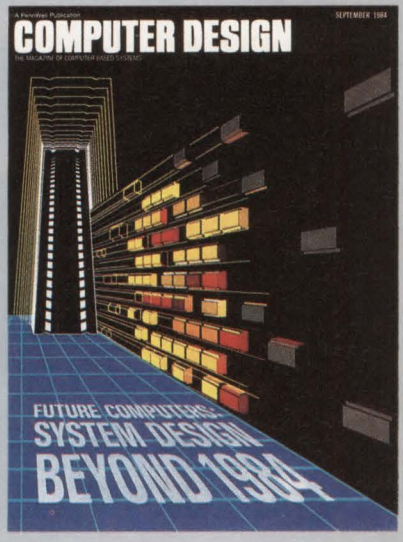

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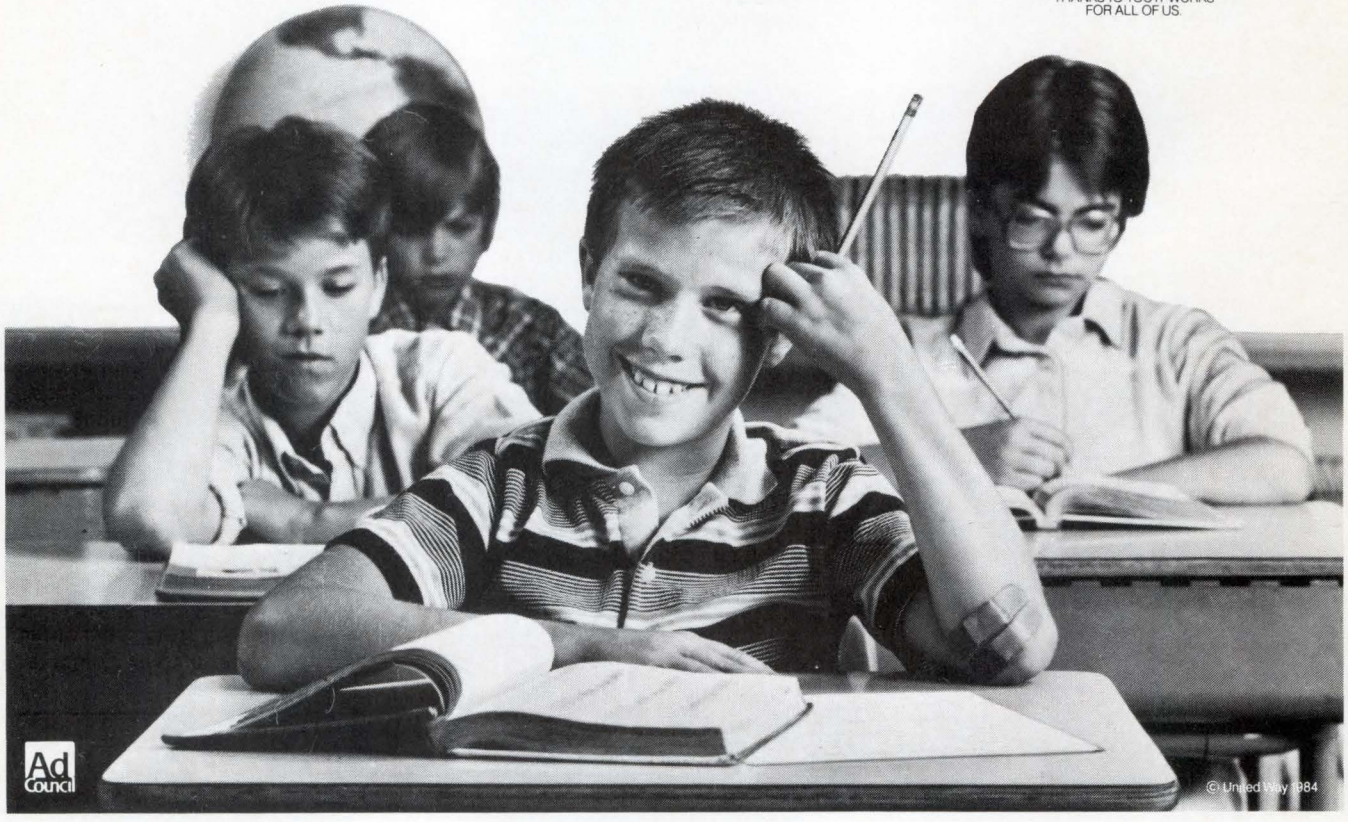

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CONFERENCES

FEB 5-7—Mini/Micro West Computer Conf and Exhibit, Anaheim Hilton Hotel, Anaheim Calif. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965.

FEB 13-15—Int'l Solid State Circuits Conf, New York Hilton, New York, NY. INFORMATION: Lewis Winner, Almeria, Coral Gables, FL 33134. Tel: 305/446-8193/4.

FEB 25-28—Compcon Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142.

FEB 26-28—Automated Design & Engineering for Electronics, Anaheim Hilton & Towers, Anaheim, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311.

MAR 5-7—Southcon & Mini/Micro Southeast, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Dale Litherland, Electronic Conventions, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965.

MAR 7-8—Int'l Conf in Industrial Automation, Hong Kong. INFORMATION: Conf Secretary, Autotech Hong Kong, Hong Kong Productivity Center, 12/F, World Commerce Center, 11 Canton Rd, Tsimshatsui, Hong Kong. Tel: 3-723-5656.

MAR 11-14—National Design Engineering Show, McCormick Place, Chicago, Ill. INFORMATION: Cahners Expo Group, PO Box 3833, Stamford, CT 06905. Tel: 203/964-0000.

MAR 13-15—Picosecond Electronics and Optoelectronics, Hyatt Lake Tahoe, Incline Village, Nev. INFORMATION: Optical Society of America, 1816 Jefferson Pl, NW, Washington, DC 20036. Tel: 202/223-0920.

MAR 13-15—Simulation Symposium, Tampa, Fla. INFORMATION: Alexander Kran, IBM Corp, East Fishkill Facility, Hopewell Junction, NY 12533. Tel: 914/894-7142.

MAR 20-22—Phoenix Conf on Computers & Communications, Hyatt Regency Hotel, Tampa, Fla. INFORMATION: Doug Powell, Motorola, Inc, PO Box 2953, Phoenix, AZ 85062. Tel: 602/244-3965.

MAR 25-28—IEEE Infocom 85, Washington, DC. INFORMATION: Celia L. Desmond, Rm 1855, 160 Elgin St, Ottawa, Ontario, Canada K1G 3J4. Tel: 613/239-4510.

MAR 25-29—IEEE Int'l Conf on Robotics and Automation, Marriott's Pavilion Hotel, St Louis, Mo. INFORMATION: Dr K. S. Fu, Dept of Electrical Engineering, Purdue Univ, West Lafayette, IN 47907. Tel: 317/494-3433.

MAR 26-28—Applied Machine Vision Conf, Cobo Hall, Detroit, Mich. INFORMATION: Robotics Industry Assoc, PO Box 1366, Dearborn, MI 48121. Tel: 313/271-7800.

MAR 31-APR 3—Softcon, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Northeast Expo, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000.

APR 1-2—IEEE VLSI Test Workshop, Bally Park Place Hotel, Atlantic City, NJ. INFORMATION: Bob Tigue, IBM Dept 69J/422, Neighborhood Rd, Kingston, NY 12401. Tel: 914/385-7440.

APR 2-4—IEEE Microprocessor Forum, Bally Park Place Hotel, Atlantic City, NJ. INFORMATION: Helen Yonan, IEEE Office, Moore School of Electrical Engineering, Univ of Pennsylvania, Philadelphia, PA 19104. Tel: 215/898-8106.

APR 14-18—Computer Graphics Conf, Dallas Conv Center, Dallas, Tex. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Ste 601, Fairfax, VA 22031. Tel: 703/698-9600.

APR 16-18—Computer Integrated Mfg and Communications Conf, Disneyland Hotel, Anaheim, Calif. INFORMATION: CASA/SME Public Relations, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777.

APR 17-24—Hannover Fair '85, Hannover, West Germany. INFORMATION: Hannover Fairs Information Center, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044.

APR 23-25—Electro and Mini/Micro Northeast, Coliseum and Sheraton Center, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965.

APR 29-MAY 2—Intermag Conference, Radisson St Paul Hotel, St Paul, Minn. INFORMATION: J. H. Nyenhuis, Dept of Electrical Engineering, Purdue Univ, West Lafayette, IN 47907. Tel: 317/494-3524.

APR 30-MAY 2—Artificial Intelligence and Advanced Computer Technology Conf/Exh, Long Beach, Calif. INFORMATION: Tower Conference Management Co, 331 W Wesley St, Wheaton, IL 60187. Tel: 312/668-8100.

SHORT COURSES

FEB 15-MAR 1—Operating Systems for Microcomputers; MAR 11-15—Electromagnetic Interference & Control, Washington, DC. INFORMATION: Merril Ann Ferber, The George Washington Univ, School of Engineering & Applied Science, Washington, DC 20052. Tel: 202/676-8522.

FEB 18-20—Design of Fiber Optic Communication Systems, Univ of Wisconsin, Madison, Wis. INFORMATION: Francis P. Drake, Dept of Engineering & Applied Science, Univ of Wisconsin-Extension, 432 N Lake St, Madison, WI 53706. Tel: 608/263-7427.

FEB 18-22—Knowledge Acquisition for Expert Systems, Washington, DC. INFORMATION: Expert-Knowledge Systems, Inc, 6313 Old Chesterbrook Rd, McLean, VA 22101.

MAR 14-16/MAY 30-JUNE 1—Workshop on Personal Computer and STD Computer Interfacing for Scientific Instrument Automation, Blacksburg, Va. INFORMATION: David E. Larsen, Virginia Polytechnic Institute & State Univ, Blacksburg, VA 24061. Tel: 703/961-6478.

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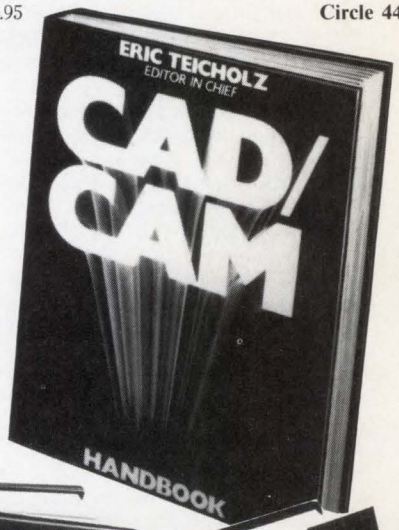

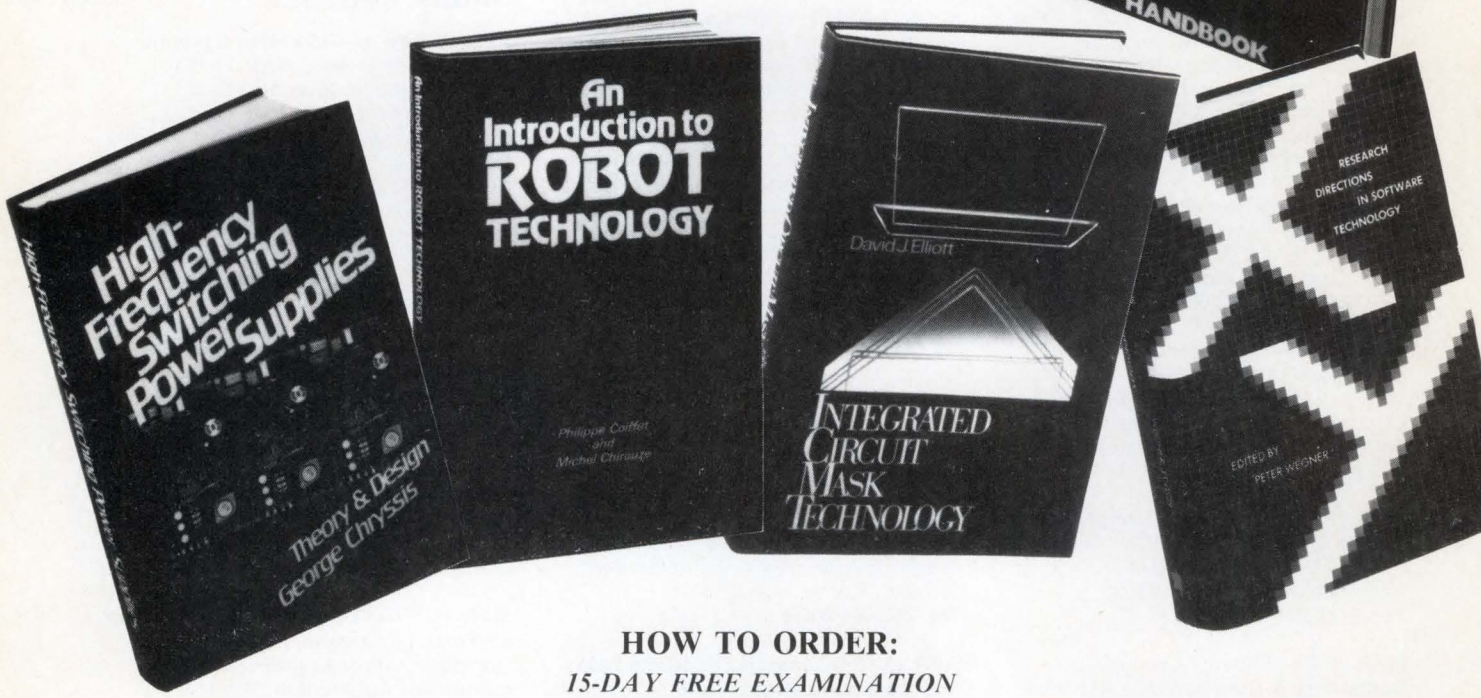

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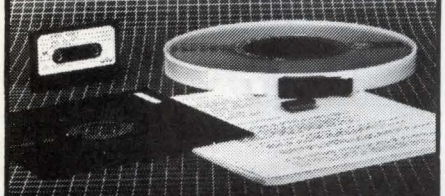

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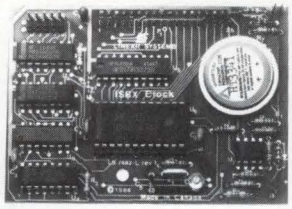

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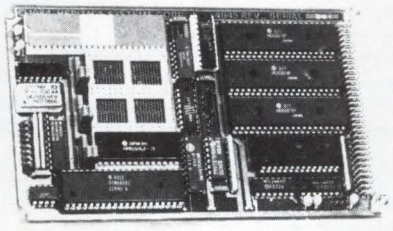

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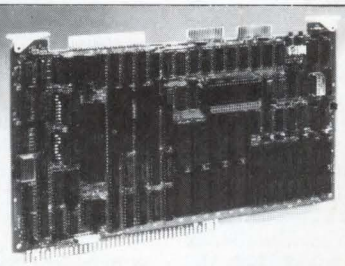

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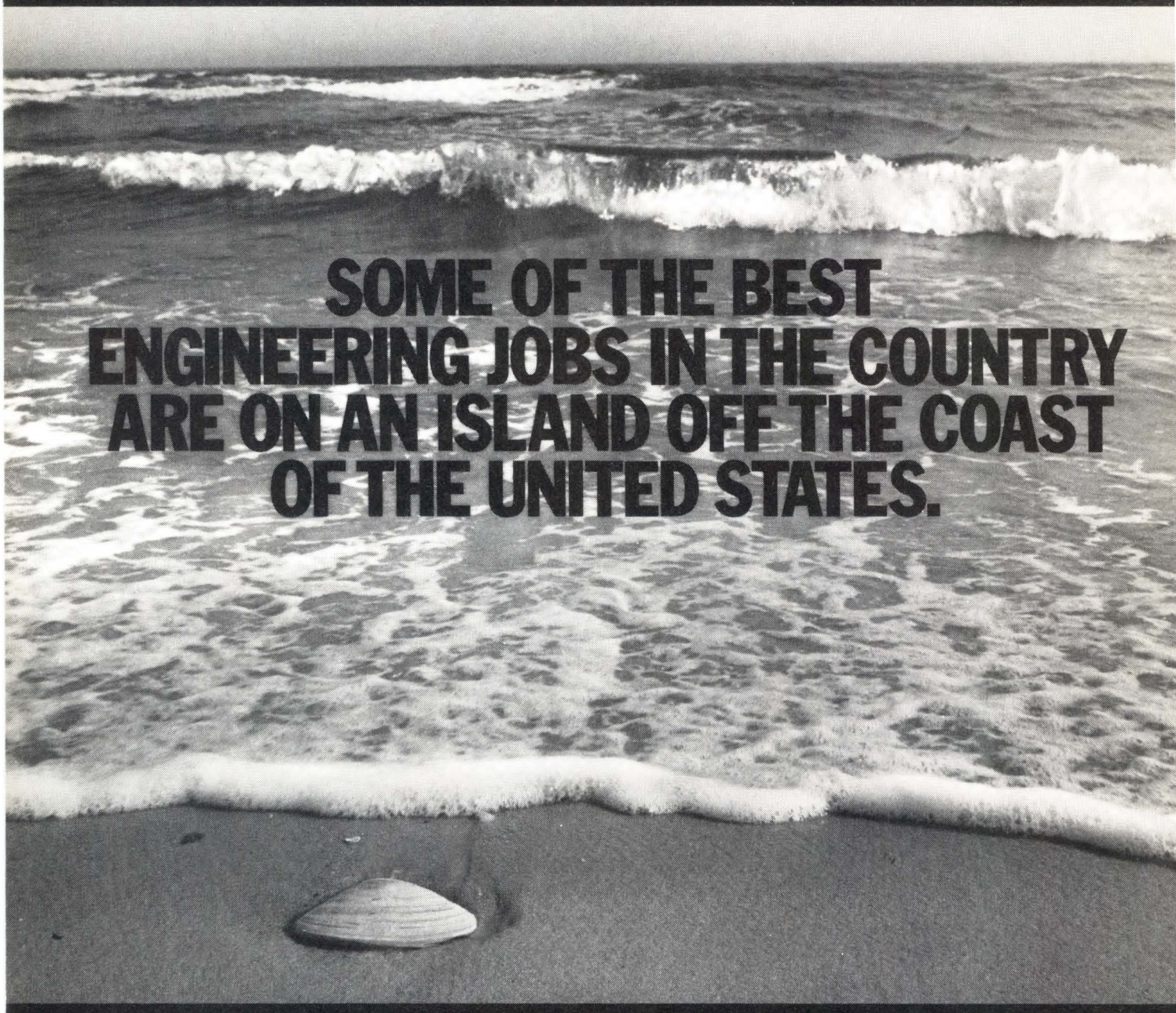

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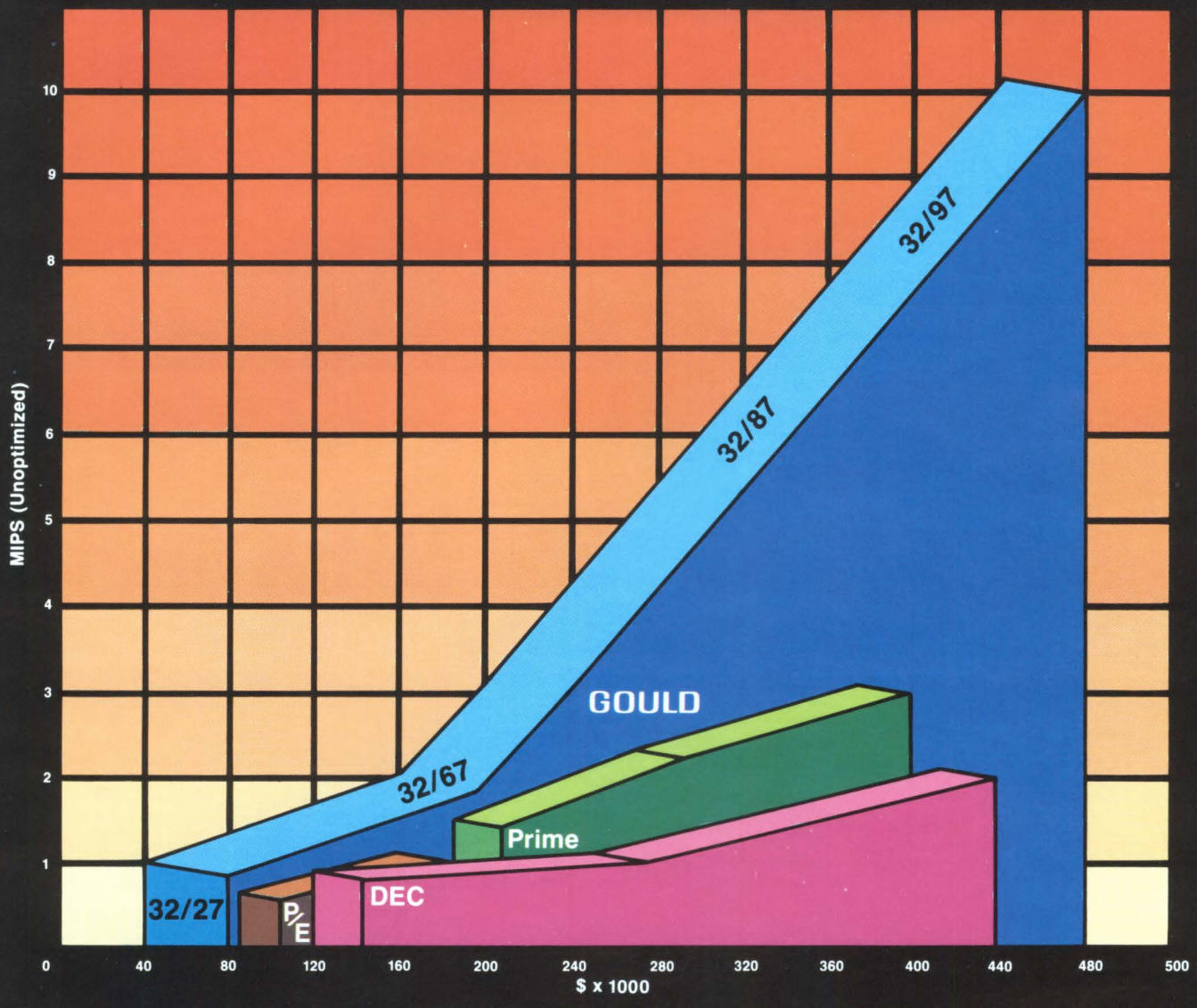

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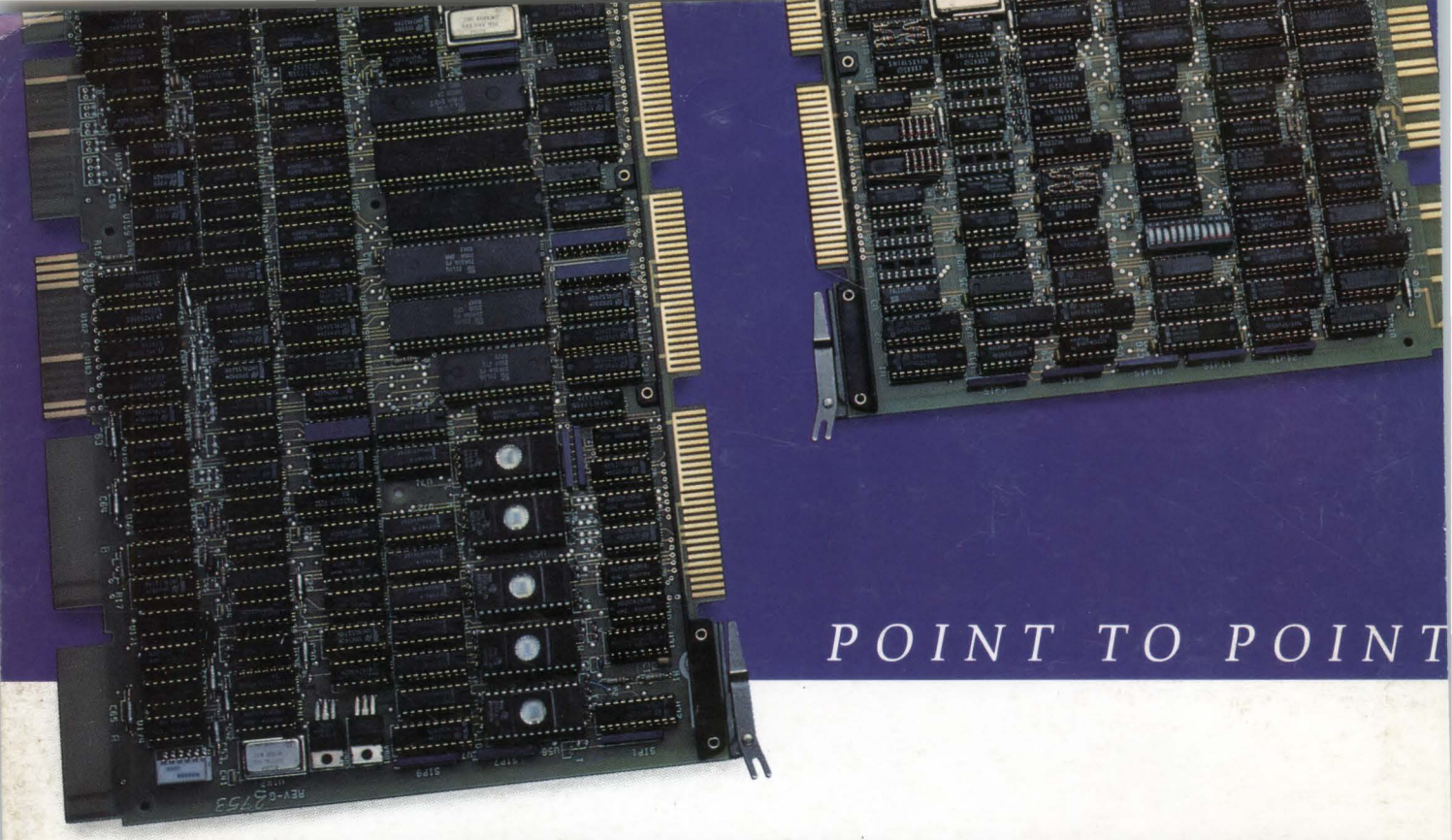

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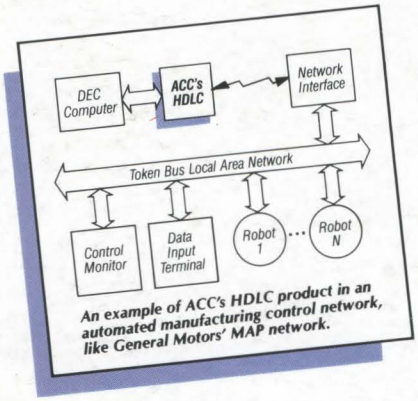

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