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FEBRUARY 1984

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

SPECIAL REPORT:
DATA COMMUNICATIONS

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CIRCLE 1

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MDB Systems Europe, Inc.
9 route des Jeunes
CH-1227 Geneva (Switzerland)
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FAX (41) (22) 439414

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UP FRONT

French private branch exchange enters U.S. market

Although it is fashionable to expound on the "upcoming next generation" of equipment (see staff report, p 149), some companies are content to nibble away at a "real" market by offering equipment of a "before-the-next" generation caliber. For example, Jistel of Stamford, Conn has introduced a family of analog and digital private branch exchanges (PBXs) with which the company hopes to capture a 4- to 6-percent share of the U.S. market by 1987. (Jistel is a division of JS of America Inc, which in turn is a subsidiary of Jeumont-Schneider of Puteaux, France.) The U.S. PBX market—40 percent of that worldwide—is relatively free of the restrictions imposed in European countries. Also, the breakup of the Bell Telephone System offers an even more lucrative target for competitive companies.

Two analog voice-only systems available this quarter are time division multiplex switches using pulse amplitude modulation techniques. Jistel 95 has a capacity for 16 trunk lines and can accommodate 80 stations, while the Jistel 200 handles 32 trunk lines and 208 stations. Both products have been in use in France and other European countries for several years, but are reconfigured to adhere to U.S. FCC regulations and to match U.S. PBX competitive features. Two digital products, the 150 and 500, to be available in the last quarter of 1984, will be able to route both voice and data at a 56-kbit/s rate.

"Concept-processing" workstation links to powerful computing

For the most part, array-based schemes favored for developing artificial intelligence, robotics, vision systems, and signal processing applications have been ideas in search of a practical development tool. To that end, Analogic Corp (Wakefield, Mass) has created its APL Machine, which turns an unmodified IBM PC into a programmer's workstation fronting its 10-MFLOPS, 32-bit AP500 array processor. Under a Unix-derived operating system, the PC runs the International Standards Organization-validated APL written on its own or outside hardware. The APL interpreter runs in the 12.5-MHz, 16/32-bit micro control processor; primitive functions and operators of APL reside in pipeline microcode. In addition, the company provides Unix-like shells that incorporate non-APL code for applications using compiled or assembled code.

Macintosh or Granny Smith?

The high stakes personal computer game gets yet another raise in the form of Apple's long-awaited Macintosh. By spurning the pack and IBM PC compatibility, Apple is clearly drawing a line in the dirt. The 68000-based machine will have a Lisa-like operating environment such that Macintosh programs will run on the Lisa but not vice versa. The machine should also give a big boost to acceptance of the 3½-in. floppy disk that Hewlett-Packard is already using in its PC-compatible model 150. Apple is emphasizing support for independent software developers, and at the price of $2495, Macintosh (if it makes it in the initial post-introduction phase), should give the competition a real run for the money. The basic price includes a word processing program (MacWrite) and a graphics package (MacPaint). Apple has also introduced three new models of Lisa: Lisa 2, 2/5, and 2/10, all software compatible with the Macintosh.

Seeq to produce high endurance EEROM

One million write cycles per byte is to be the new standard for electrically erasable ROMs produced by Seeq Technology (San Jose, Calif). The 5516A, a 16-Kbit (2-K x 8) EEROM, will hopefully encourage more design-in by designers wary of write limitations in EEROMs. The part has an onchip timer and a write cycle time of 10 ms. Seeq offers the million-write version as a high endurance version of its existing 2816A. Future products will include high endurance versions of existing parts as well as yet unannounced million-write EEROMs and other ICs incorporating the high endurance "Q cell" technology onchip.

UP FRONT

Motorola completes CMOS RAM tests for VHSIC program

Engineers at Motorola Semiconductor (Phoenix, Ariz) have completed tests on a 4-port silicon-gate CMOS RAM as part of phase I for the Department of Defense's very high speed integrated circuit (VHSIC) program. The 4-Kbit chip is believed to be the first bulk CMOS part manufactured using Motorola's 1.25-μm HCMOS design rules. In operation, the RAM can have two independent addresses read out while two other independent addresses are being written into it, all using a single 25-MHz clock. The part is slated for an electronic warfare application for which Motorola's VHSIC partner, TRW Inc (Redondo Beach, Calif), is supplying the brassboard. The memory IC is functionally compatible with TRW's triple-diffused bipolar parts, with both types of circuits operating off a 3.3-V power supply. With 12 transistors/memory cell, the 290- x 313-mil memory chip contains a total of 59,700 transistors. This translates to a functional throughput rate (FTR) of 10^{11} gate•Hz/cm^2 which, in turn, requires 300 mW of power to dissipate. The next challenge for Motorola engineers is to build a 6-Kbit CMOS gate array chip that will also be compatible with the other chips on TRW's brassboard. (Sperry Corp is a third member of the program team.)

IBM PC backs Unix

IBM Information Systems Group (Rye Brook, NY) has announced its flavor of Unix for the IBM PC. Known as the personal computer interactive executive system (PC/IX), the operating system implements a superset of Unix System III with an interactive full-screen editor. The minimum configuration needed is 256 Kbytes of RAM, a single 320-Kbyte floppy disk drive, and a 10-Mbyte rigid disk drive. The Unix port was done by Interactive Systems (Santa Monica, Calif). It will be ready for release at the beginning of April.

Industrial computer slides in processing capability

Departing from the traditional shared logic approach of single CPU systems, Indocomp, Inc's (Drayton Plains, Mich) IMP-68000 depends on independent processors. Each processor runs its own operating system and executes its own application programs. This prevents one processor crash from affecting other running processes. Slide-in processor boards (all front accessible) consist of a standard processor section and a customized I/O section. Current I/O sections include both digital and analog boards as well as a development board with predrilled holes and a large wirewrap area.

TI and Fujitsu to alternate source bipolar, CMOS arrays

At a still-unannounced future date, Texas Instruments (Dallas, Tex) will supply gate array products based on design and fabrication information from Fujitsu Ltd (Santa Clara, Calif). This alternate-source agreement between the American and Japanese semiconductor giants covers both bipolar and CMOS devices. Specifically, these will be bipolar Schottky TTL arrays with 1.9-ns delays in densities ranging from 240 to 1100 gates; and H-series and VH-series CMOS arrays in densities from 440 to 8000 gates. Both TI and Fujitsu have proprietary computer aided design systems and design languages. To aid customers, each company will provide the means to accept circuit descriptions written in the other's language and convert them to produce guaranteed compatible parts. The companies emphasize that Fujitsu is giving TI parameters for producing compatible designs rather than actual process technology.

COMPUTER DESIGN©1984 (ISSN-0010-4566) is published monthly, with a thirteenth and fourteenth issue respectively in June and October by PennWell Publishing Company, Advanced Technology Group, 119 Russell Street, Littleton, MA 01460. Second-class postage paid at Littleton, MA 01460 and additional mailing offices. COMPUTER DESIGN is distributed without charge to U.S. and W. Europe-based engineers and engineering managers responsible for computer-based equipment and systems design. Subscription rate for others is $50 in U.S.A. and $75 elsewhere. Single copy price is $5.00 in U.S.A. and $7.50 elsewhere. Microfilm copies of COMPUTER DESIGN are available and may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Road, Ann Arbor, Michigan 48106. POSTMASTER: CHANGE OF ADDRESS-FORM 3579 to be sent to COMPUTER DESIGN, Circulation Department, P.O. Box 593, Littleton, MA 01460 (USPS 127-340).

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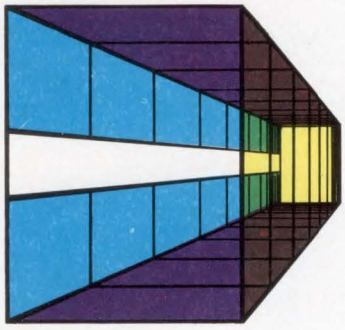
CIRCLE 4

System technology



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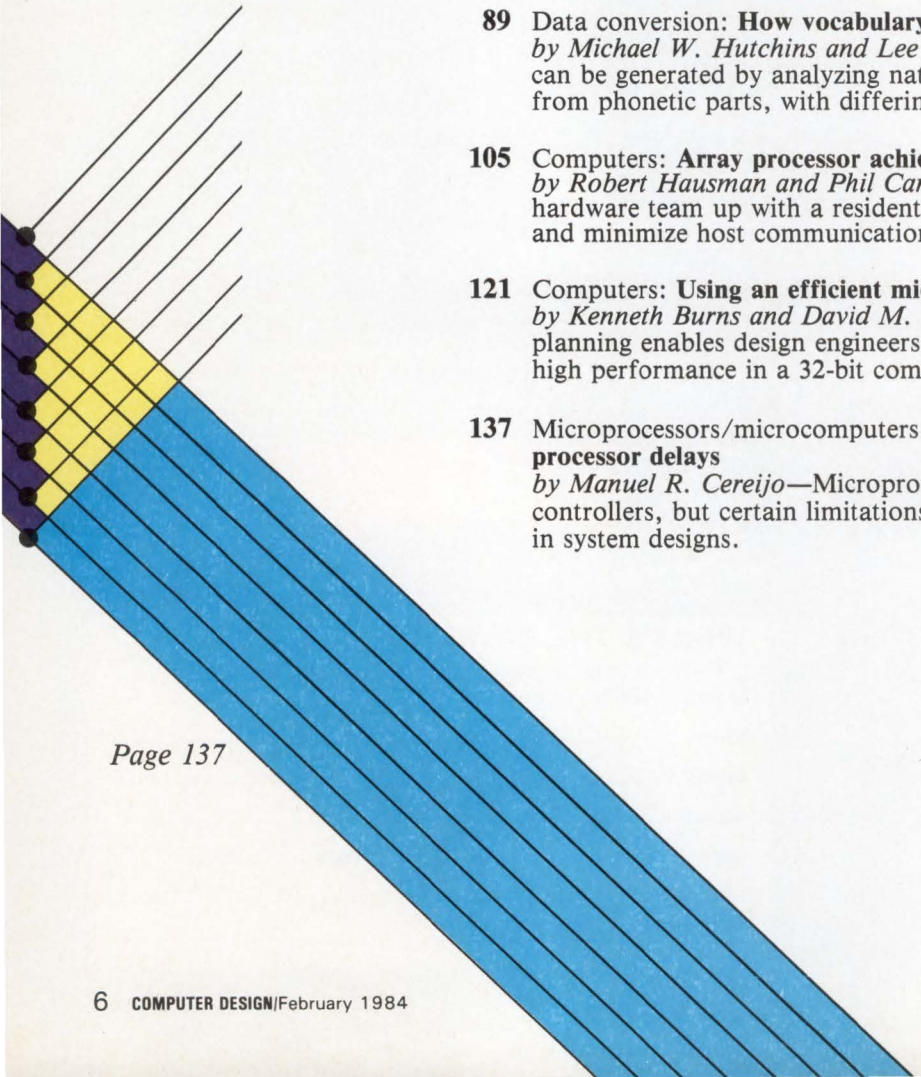
System design



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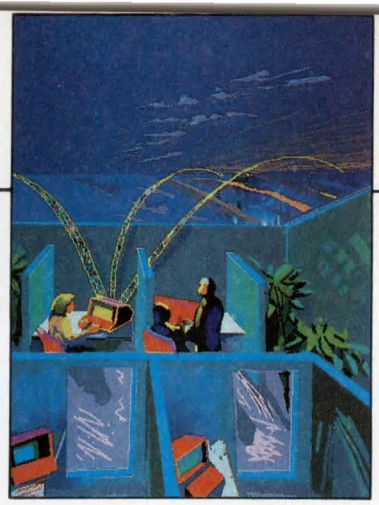
Special report on data communications



This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

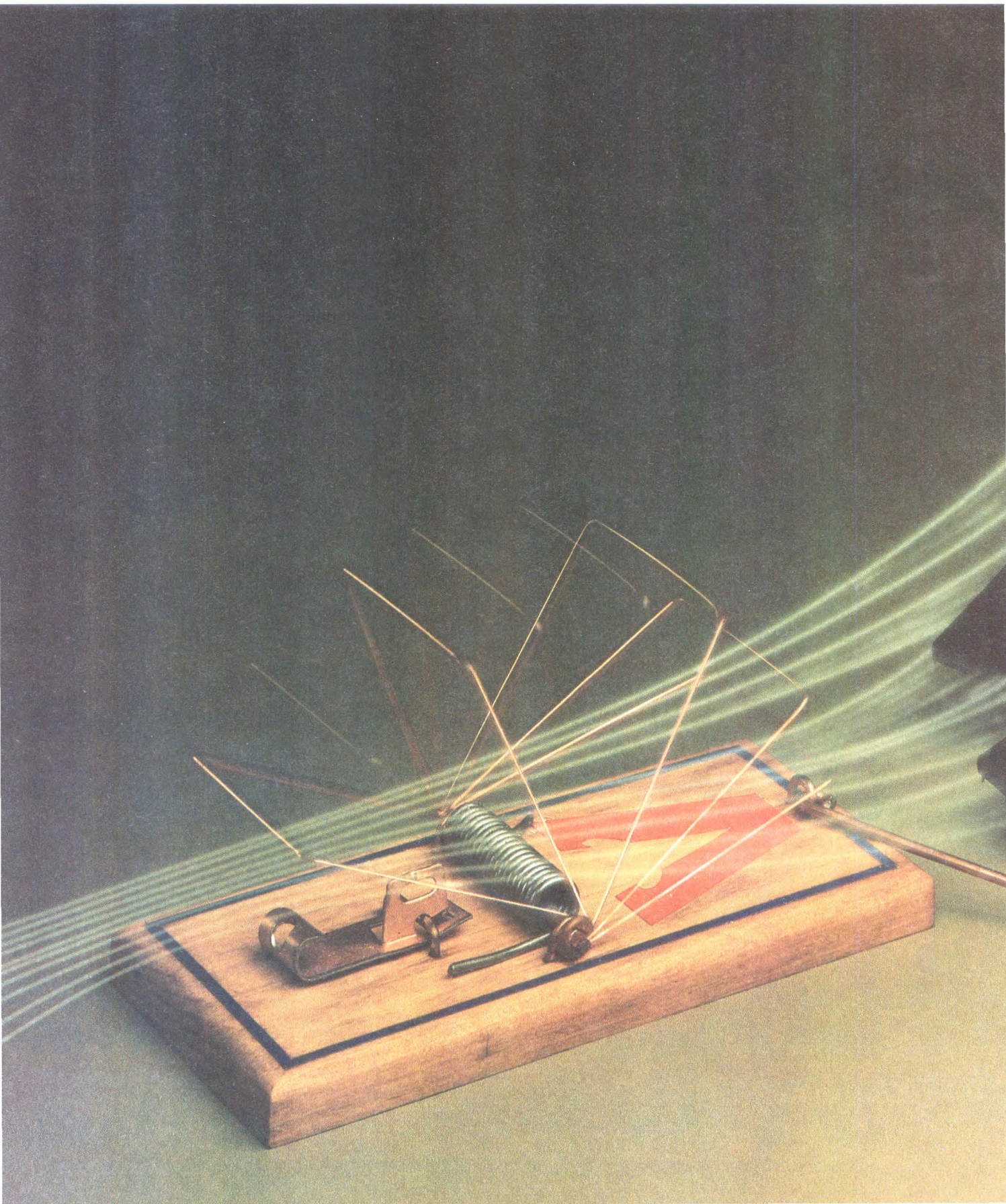
System components

Departments

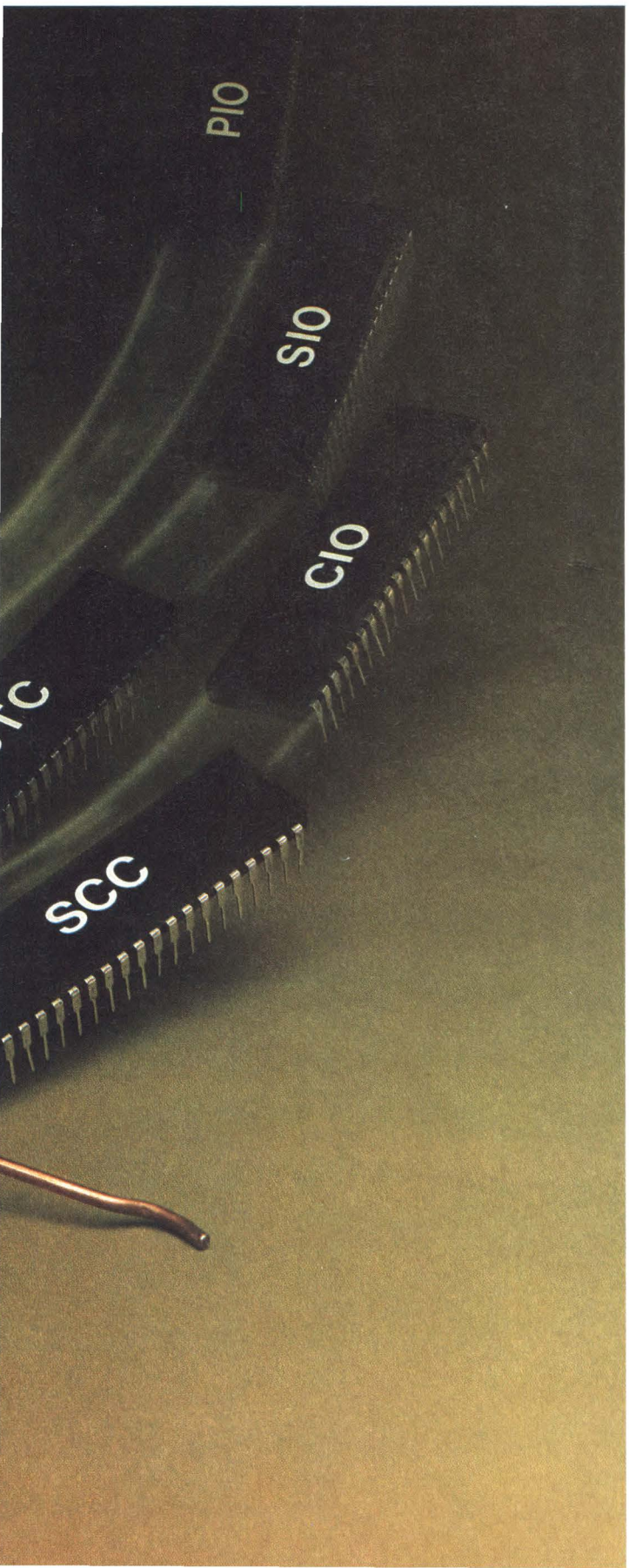
Editorial reviewer for part of this issue:

D. Iuster, Sr

You'll never get trapped into dead-end designs with



Zilog's high-speed Z80B CPU's and Peripherals.



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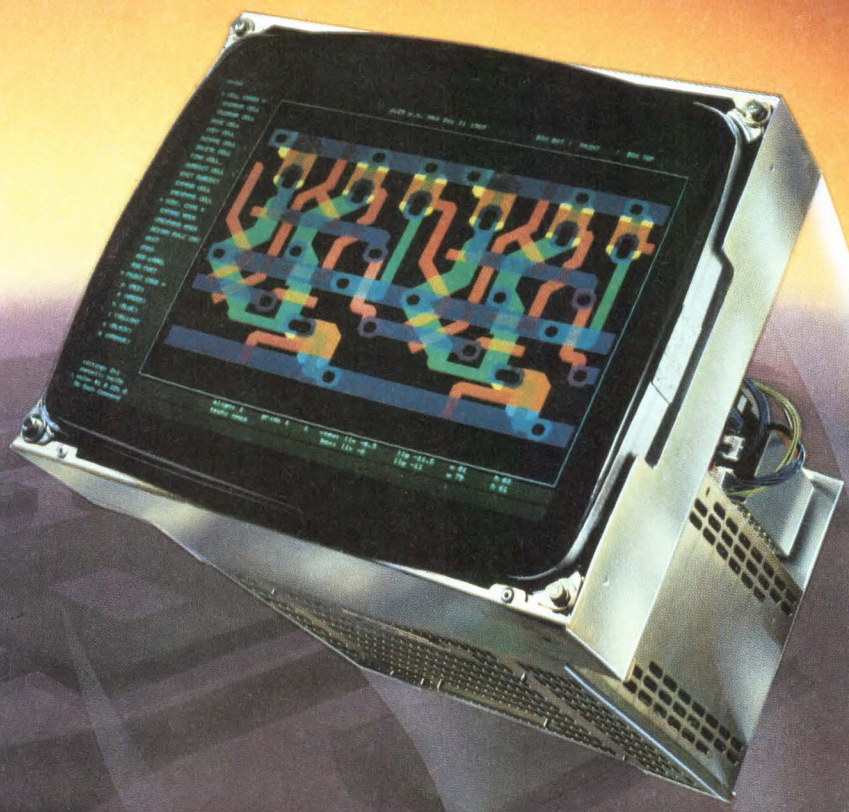

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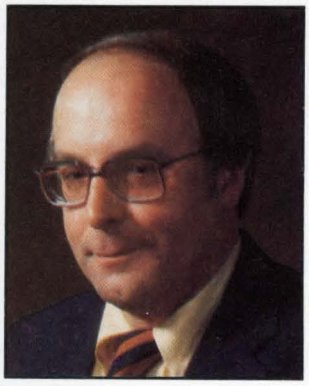
CIRCLE 6

THE COMPUTER ILLITERACY THREAT



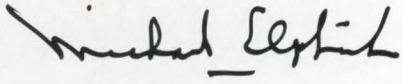
Many years ago, we knew a fellow who sold encyclopedias. His selling technique was brutal but quite effective. Usually, he would work low income neighborhoods, going from door to door. If the prospects had children, he would ask if they wanted their kids to grow up as poor and uneducated as their parents. Except in those cases where the door slammed in his face, it was then surprisingly easy for him to convince the concerned parents that the purchase of a set of encyclopedias on an easy payment plan virtually guaranteed that their kids would become prosperous geniuses.

Today, unfortunately, many personal computers are being sold in a similar fashion. Now we are starting to read and hear a lot about "computer literacy" without which, it is said, our children will not be able to survive in an increasingly competitive and computerized world. Yet, although many people talk about computer literacy, nobody ever bothers to define it. Therefore, we are not sure whether it means the ability to play a fair game of Pac-Man, or the ability to write device drivers in assembly code. Either way, however, the skill does not seem to have any particular relevance to survival in tomorrow's business world.

Computer system designers know that, by the time today's schoolchildren join the work force, a business computer will be no more difficult to use than a typewriter or telephone. Tomorrow's computer users will not have to worry about the subtle quirks of operating systems, just as today's users do not have to get Cobol programs keypunched onto decks of cards. Yet, the public seems to have been brainwashed by the computer literacy argument that has been pounded home by repeated TV commercials. People today ask engineers not whether they should buy a personal computer, but only which one to buy.

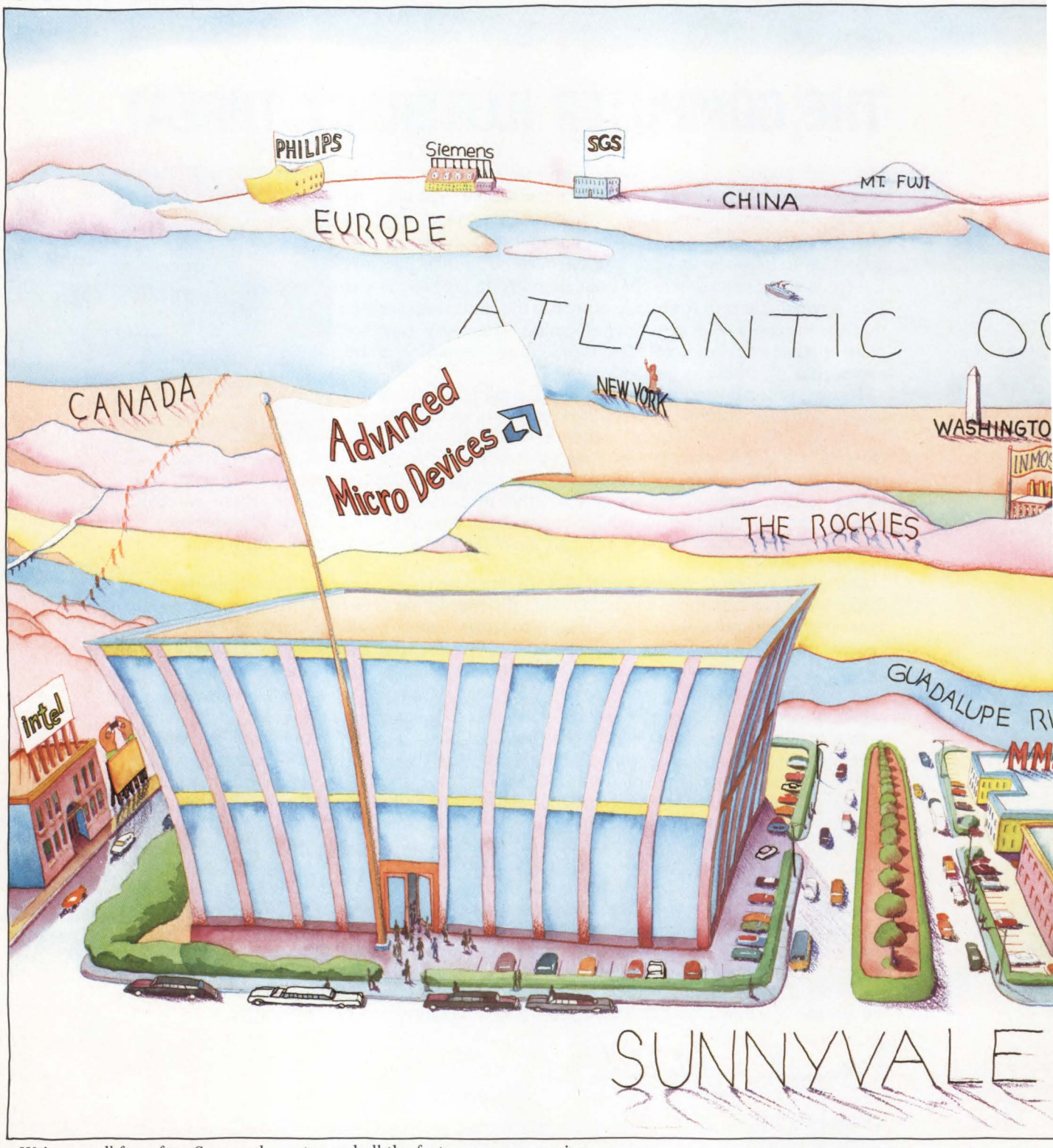
In a few years, it is very possible that personal computers will provide convenient educational workstations at which children can learn, draw, write, and calculate. So far, however, most educational software is so abysmal that a computer is a needlessly expensive replacement for a conventional blackboard and textbooks.

Apart from maintaining the financial health of computer companies, therefore, we see no urgent need to accelerate the introduction of personal computers into the school or home. Certainly, we see no overwhelming national benefit in such proposed legislation as HR701—a bill introduced by Congressman Fortney Stark of California—which would give computer makers a double tax write-off for donating their computers to schools. If we as engineers push too vigorously for such legislation—in the misguided hope that it will aid the computer industry—we may find that we have lost our professional credibility when the fad has passed and unused personal computers are littered around like Rubik's Cubes or Pet Rocks. Yes, computers should have a bright future in business, the classroom, and the home—but not if we kill the industry with premature and excessive hype.



Michael Elphick
Editor in Chief

MEMORIES.



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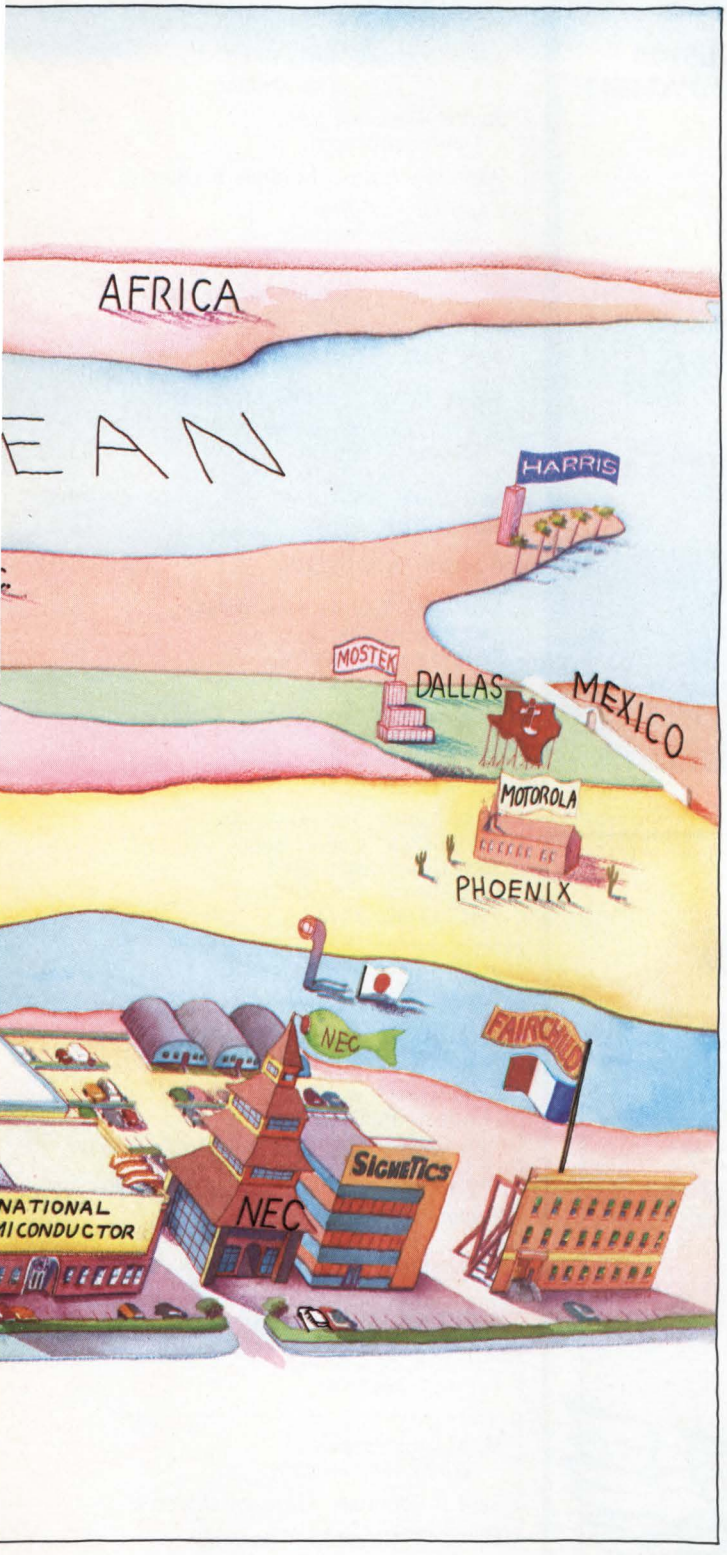

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It's just not fair to claim that TEMPLATE® is the best graphics software available. Our competition's already discouraged.

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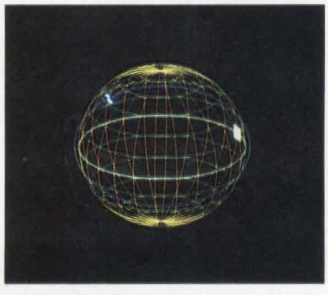

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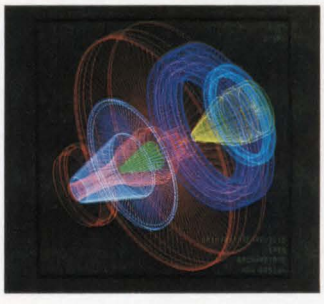

But let's be fair. If you're looking for graphics software, call our competitors first. Find out what they have to say about theirs. Then call us, and find out why TEMPLATE really has no competition.

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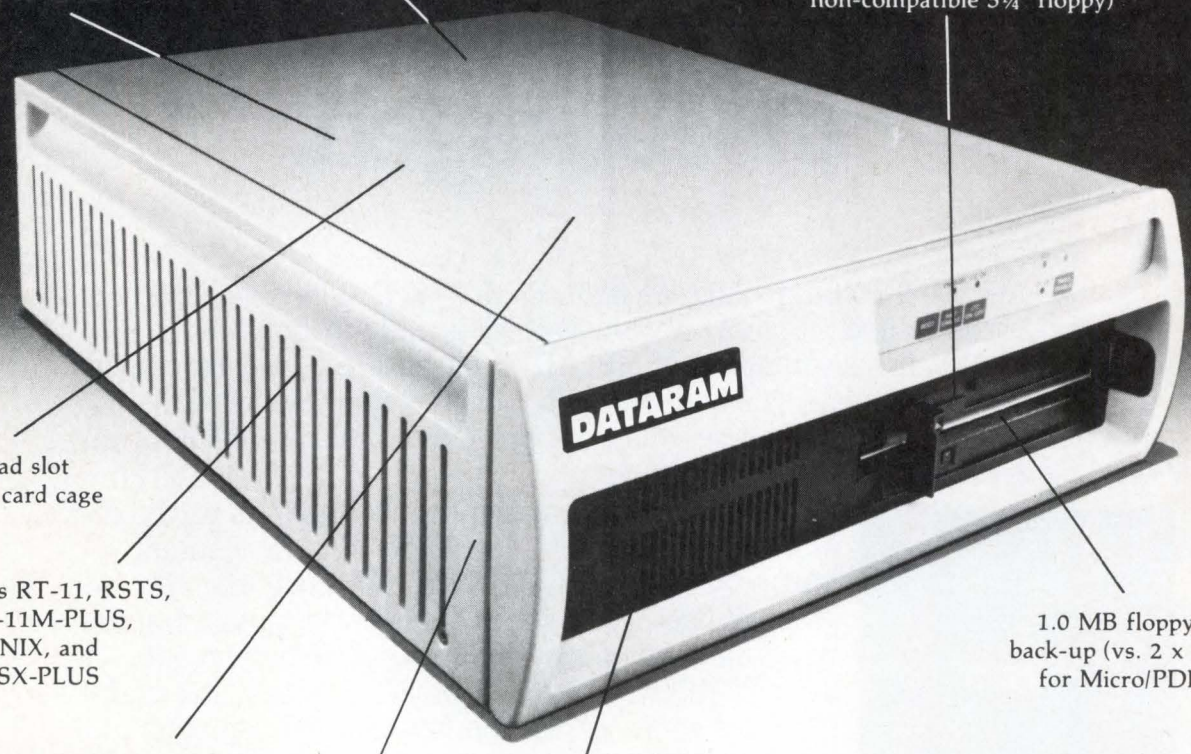
CIRCLE 9

Like DEC's.



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CIRCLE 11

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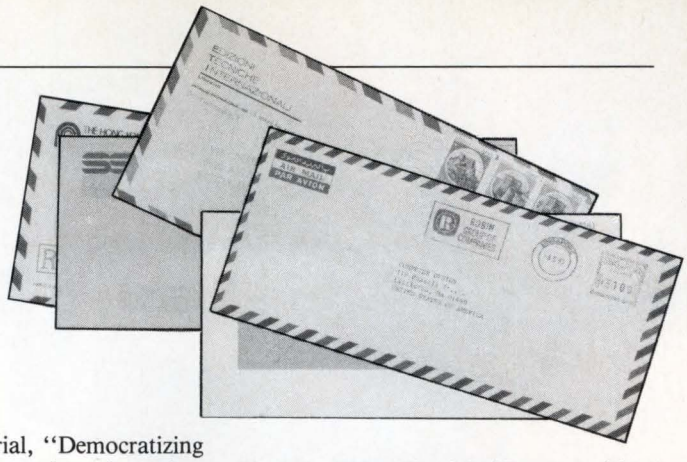
LETTERS TO THE EDITOR



Identifying management differences

This is written in response to your editorial (Oct 4, 1983) entitled "Wa Versus the Gunslingers." I believe that you identified the main point of management style differences. American managers seem to love a crisis where they can fumble or manage their way through it. Japanese managers consider a crisis, any crisis, a management failure. Simple, isn't it? But what a difference.

Eugene S. Redner
Digital Equipment Corp
146 Main St
Maynard, MA 01754

Another look at the IEEE...

Congratulations on the Nov 1983 editorial "Democratizing the IEEE." I am sure that Mr Elphick has done the IEEE and the profession a great service by airing some of our dirty laundry in public. Perhaps this will lead to less dirty laundry.

The editorial was of special interest to us in Rochester, because Malcolm "Mac" Drummond is a Rochesterian, and is active in local Section activities. With your kind permission, I would like to reprint your editorial in *The Rochester Engineer*. It is a monthly publication of the Rochester Engineering Society, and carries several pages of IEEE news, as well as news from other member engineering societies. The total circulation is, I believe, in excess of 3000, including about 1400 IEEE members.

I hope that you are able to continue to present, on occasion, an unsanitized view of the IEEE. The only other unbiased source of information on IEEE doings seems to be *EE Times*.

Jacob Z. Schanker
IEEE, Rochester Section
65 Crandon Way
Rochester, NY 14618

I just got to the Nov 1983 IEEE editorial. I hope you voted for Irwin Feerst and also sent his committee a contribution. Perhaps your editorial and others will help get IEEE back on track, but I doubt it. I quit several years ago and haven't had any second thoughts.

Jonathan A. Titus
The Blacksburg Group, Inc
PO Box 242
Blacksburg, VA 24060

The Nov 1983 editorial, "Democratizing the IEEE," was terse and to the point. Simply put, the IEEE does not support the group that supports it—the working engineer.

Your identification of Edward J. Doyle (IEEE's former VP for Professional Activities as of Dec 31, 1983) as the villain in the RCA pension dispute was correct. And in the furor surrounding the "return home" clause of the pending immigration bill (which would require that all foreign graduates of American colleges return home for at least two years) you were also correct. So long as this important position is selected by IEEE's Board of Directors and not elected by the membership, there is little hope that the VP for Professional Activities will reflect the wishes of the membership.

For this reason, we are sponsoring an amendment to IEEE's constitution that would make this position an elective one. Interested readers may obtain a copy of the petition form by writing to the undersigned.

Irwin Feerst
Committee of Concerned EEs
PO Box 19
Massapequa Park, NY 11762

...A different look at the IEEE

The perennial gadfly, Irwin Feerst, has received so much unwarranted press coverage, the effect is nauseating. The Nov 1983 issue of *Computer Design* carries another of his unsubstantiated diatribes. Not only that, Mr Michael Elphick, editor in chief, joins him in belittling IEEE procedures and policies. I expect more mature journalism.

IEEE is by no means perfect, but as many times as Irwin Feerst has run and been rejected by the majority of its members, he and Michael Elphick ought to be getting the message. While Mr Elphick may have a valid point in the case of Mr Lewis and Mr Drummond, he cannot be trusted if he associates himself with Mr Feerst. *Computer Design* ought to be able to do better.

Jens J. Jonsson
Brigham Young University
Electrical Engineering Science Dept
Provo, UT 84602

The Nov 1983 editorial, "Democratizing the IEEE" is in tune with the loud noise exerted by the street people who are always fortified by "coke" and weeds. Legislation requiring alien engineering students to return home upon graduation is a pathetic political attempt to rectify inexorable economic facts. The logic behind it is equivalent to saying that we had better ship Einstein back to Germany, because he is competing unfairly with Americans.

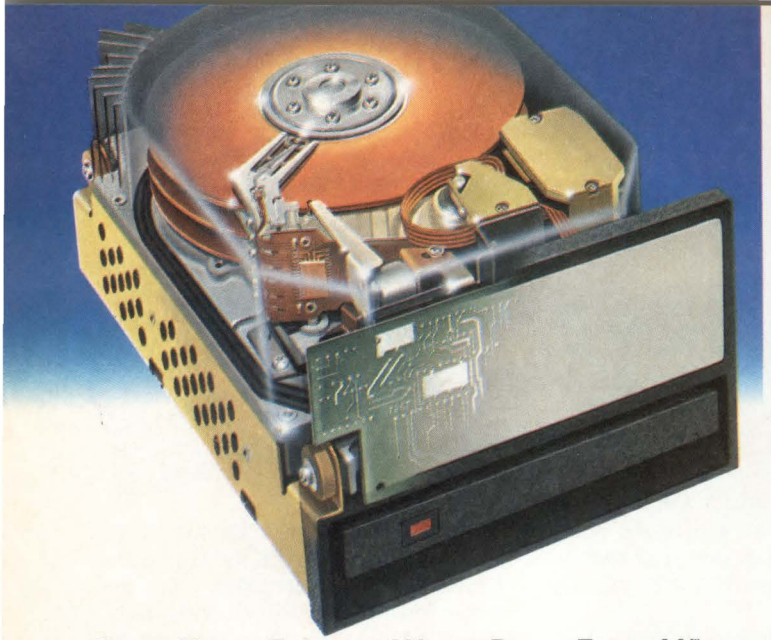
Legislating import quotas for computers, autos, and engineers is simply a frank admission of mediocrity. It is untenable in a free market. Trying to "democratize" IEEE will have no effect whatsoever. Your editorial efforts will be more appreciated if you will stick to developing better guidelines for computer design.

Frederick Marich
Amdahl Corp
110 Seville Way
San Mateo, CA 94402

In my editorial, I never took a position either for or against a return-home clause for foreign engineering students. I merely proposed that the IEEE should be responsive to the wishes of the majority of its members. In the absence of a formal referendum, we still do not know the majority position on this issue. Apparently, the IEEE's Professional Activities Committee changed its position without consulting the membership. This indecisiveness undermined the credibility of any position the IEEE might adopt and also forced the resignation of an energetic volunteer worker. If the IEEE persists in taking positions on major issues without polling the membership, its leadership must take full responsibility for their actions. This makes them fair game for editorial comment and for criticism from people like Irwin Feerst who suspect they are motivated by narrow corporate and academic interests.

Michael Elphick
Editor in Chief

(continued on page 20)



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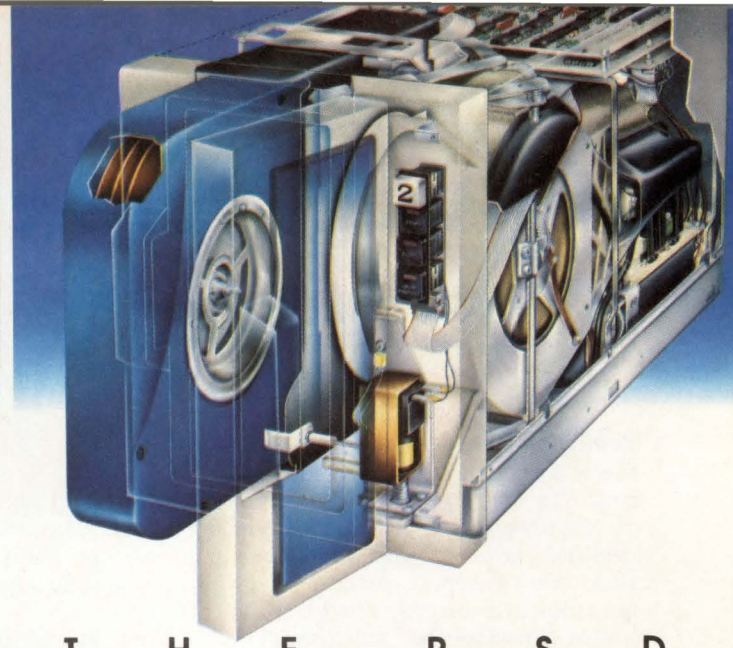
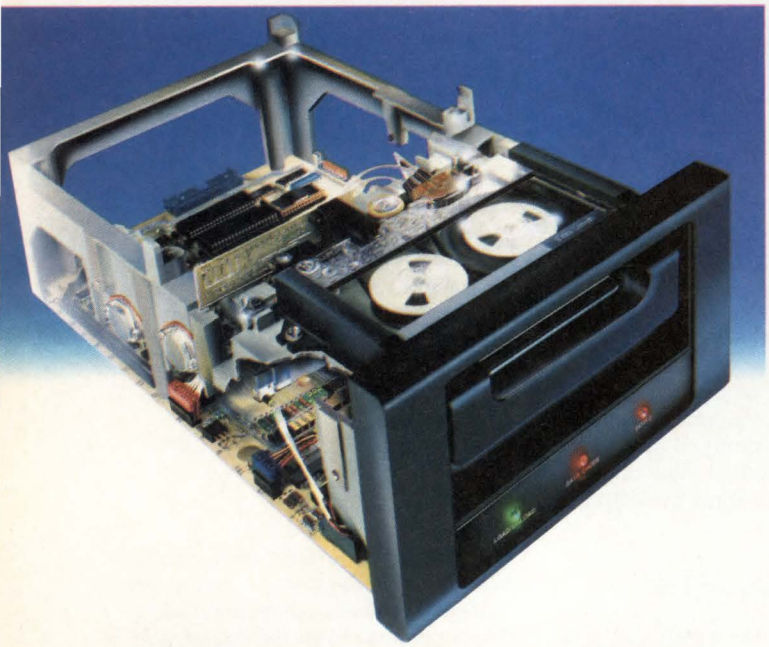


THE RSD



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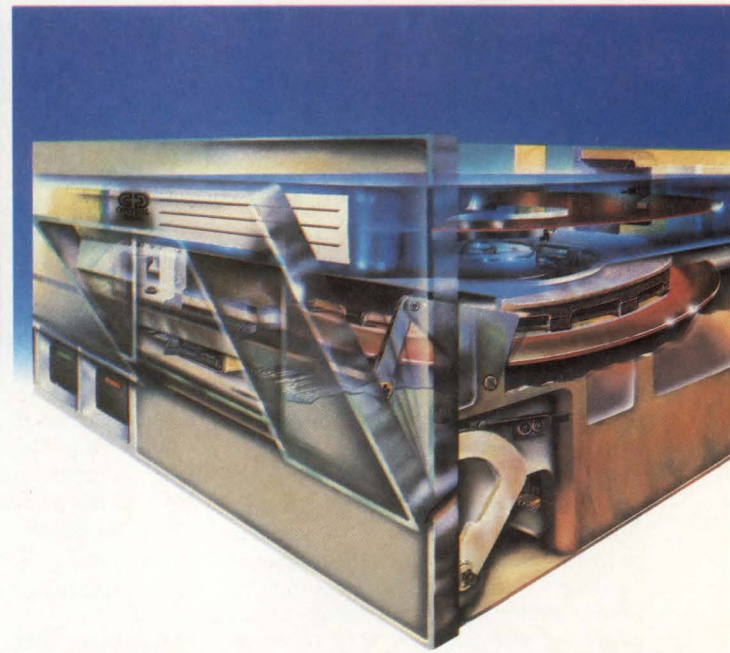

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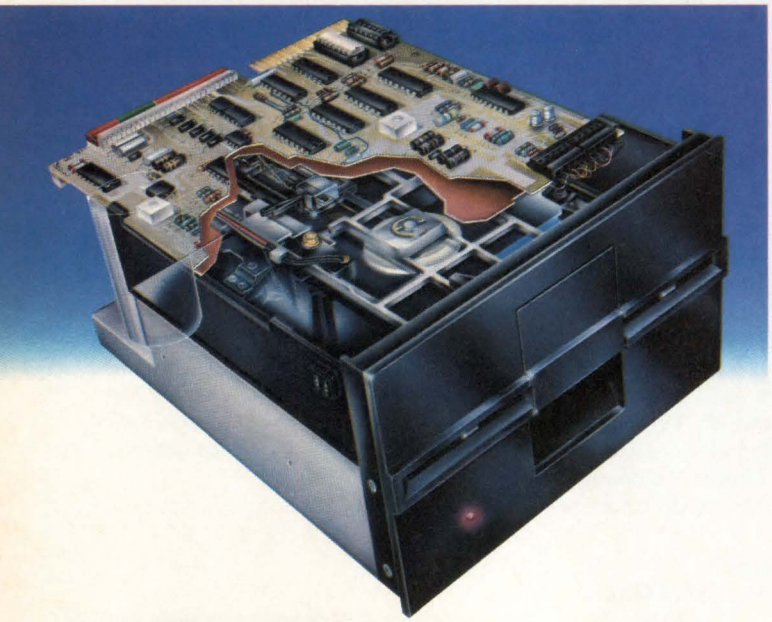

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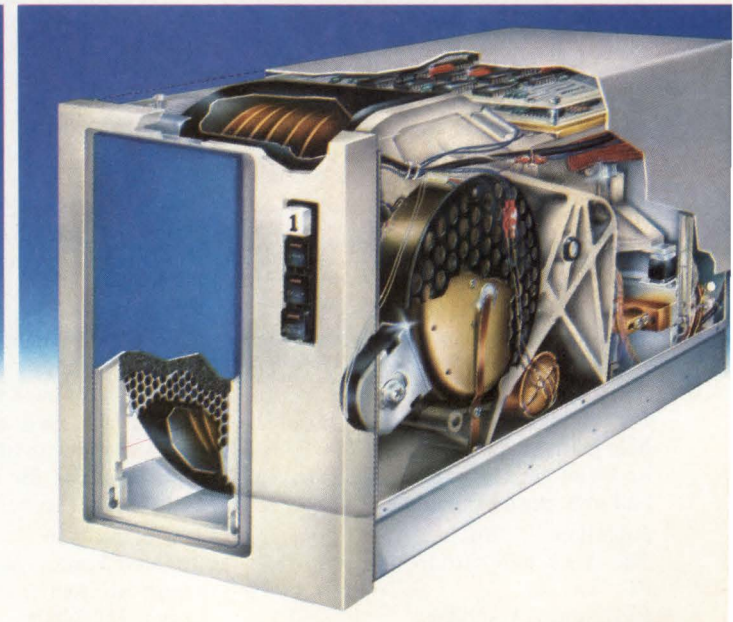

THE FSD

CONTROL DATA: AFTER 25 YEARS, STILL THE LEADER IN THE PERFORMING ARTS.

Designing peripherals with exceptional performance is as much an art as a science. We know. We've been doing it since 1962. From the beginning, we've been dedicated to giving you solutions to on-line and back-up storage needs. Example: the Storage Module Drive (SMD) we introduced became the industry standard for removable media disk drives. The SMD is just one of the high-performance products that helped make us the world's leading independent supplier of storage peripherals.

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Add to this the commitment to research, to development and to manufacturing quality that a corporation the size of Control Data contributes, and you're looking at precisely the kind of performance that makes our OEM peripherals top-rated in independent preference studies year after year.

Every performance needs a program. We'll send you one **free:** our new 48-page OEM products catalog. Write OEM Product Sales, Control Data Corporation, P.O. Box 0, HQN08H, Minneapolis, MN 55440.

CONTROL DATA

CIRCLE 12

(continued from page 17)

Marketing chip sets

I find it necessary to elaborate on a statement made in Joseph Aseo's article, "Processors Divorced from Peripherals with Separate I/O Bus" (Nov 1983, p 64). The statement "NCR Corp also shows an interest in marketing chip sets" is somewhat ambiguous. NCR Corp was one of the earliest promoters of the SCSI standard, as appreciable marketplace advantages would be available with the creation of this SCSI "universal bus with generic commands" standard. In fact, NCR Corp's Microelectronics Div was the first semiconductor manufacturer to bring a commercially available SCSI protocol controller packaged in a 48-pin DIP to the OEM marketplace.

The NCR 5385 SCSI protocol controller, supporting the 1.5-Mbyte/s data transfer rate and arbitration, was first press released in *Electronic Design* (Apr 1983). Since then, the device has been available directly from NCR's Microelectronics Div Colorado Springs facility, as well as through distribution. As you can see, not only is NCR Corp interested in marketing this standard device, we are actively pursuing it.

Michael B. Burchman
NCR Corp
Microelectronics Div
1635 Aeroplaza Dr
Colorado Springs, CO 80916

Forth is core of CATS-1 system

In the report by Nic Mokhoff, entitled "Artificial Intelligence Systems Make Their Mark" (Nov 1983, p 33), Lisp is described as the core language in expert systems. The accompanying photograph identifies the CATS-1 system for locomotive repair as an example of an expert system. The CATS-1 system was programmed in Forth. For references, see the article by Harold E. Johnson and Piero P. Bonissone, "Expert System for Diesel Electric Locomotive Repair," *The Journal of Forth Application and Research,* vol 1, no. 1, Sept 1983.

Harvey Glass
University of South Florida
College of Engineering
Tampa, FL 33620

The article "Artificial Intelligence Systems Make Their Mark" (Nov 1983, p 33) conveys two misconceptions. First, the expert system used in the CATS-1 system of General Electric was actually implemented in Forth and not Lisp, as the article implies. Nowhere in the article is it mentioned that any environment other than Lisp is suitable for artificial intelligence, whereas in fact many other environments are used. The Japanese, for instance, are scheduled to use Prolog.

Secondly, a consequence of the first misconception is the impression that the best machines for development work in artificial intelligence are optimized for Lisp. Since expert systems are very small when implemented in Forth, and since Forth is implemented on more different machines than any other high level language, there is a good chance that the particular machine already available to the knowledge engineers will probably be cheaper to configure for artificial intelligence (in time and money) than a new dedicated Lisp processor. In fact, Lisp itself has been implemented in Forth, and could still be used if necessary.

Paul Thomas
Inner Access Corp
PO Box 888
Belmont, CA 94002

Updating specifications

As a communicator for Gould CSD, I am constantly working with our development and product planning people to keep abreast of changes in our product line. It is not easy. We work in an industry where specifications and performance figures are constantly being revised upward as a result of enhancements in hardware and software. Therefore, I can understand how difficult it is to keep up with the specifications for multiple vendors when doing a report like "Superminis: Changing Direction for the Future," by Peg Killmon (Nov 1983, p 167). For the record, however, I would like to correct some factual errors in the report.

First, in recent benchmark tests, the Gould Concept 32/87 computer performed 5.6 million Whetstone instructions per second (MIPS). This is a significant improvement over the 4-MIPS level indicated in the report, and was achieved using our new Fortran 77 compiler and Multiply Accelerator.

Also, the report implied that the 4-MIPS performance level was achieved using "dual processing units." This is not true. The 5.6-MIPS performance was achieved by the Concept 32/8750 computer, a single processor. The Concept 8780, which features our unique CPU/IPU combination, is capable of performing 10 MIPS. This represents an 80-percent improvement over a single CPU configuration.

Another part of the report states that the 75-ns cycle time of 100-K ECL logic "doubles or triples the performance potential over Schottky TTL or other ECL families." This is not entirely correct either. The Concept 32/87 computer uses 10-K ECL and it too has a 75-ns cycle time. Furthermore, although 10-K ECL logic is a mature technology, it is still viable and will continue to be so for years to come.

Joe Barcheski
Gould Inc
SEL Computer Systems Div
6901 W Sunrise Blvd
Fort Lauderdale, FL 33310-9148

Speaking out for Forth

I am a user of Forth and as such would like to reply to John D. Stanley's letter about the flaws of the Forth language (Sept 1983). Certainly one cannot deny that Forth is slower than well-written assembly language code. As one who has written many thousand lines of assembly code I would be the first to admit this. But, I don't agree that this represents a weakness of Forth.

The point is that Forth is not assembly language but a higher level language of admirable speed and compactness. Not only is it faster than many other higher level languages, but it also produces more compact code than assembly language for complex programs.

Forth can support user defined interrupt handling. Bryte-Forth is an implementation currently available for the Intel 8031 microcontroller that not only allows interrupt handlers defined in Forth or machine code but also supports runtime reassignment of handlers, systems time/date, fully buffered interrupt driven serial I/O, user defined error handling, and self-starting, ROM-resident user applications. What more could a realtime application programmer need?

On the subject of readability, I contend that "unreadable" programs can be (and are) written in any higher level language or assembly language. Readability is influenced most by the ability of the programmer and the experience of the reader. Well-written Forth is very readable because of the ability to build a problem-oriented vocabulary of mnemonic words or phrases.

Forth is a fine language. Those just learning should read a good book on the concepts and programming techniques of the Forth language.

Christopher K. Johnson
Bryte Computers, Inc
PO Box 46
Augusta, ME 04330

October/Fall designer's preference study winner: Duke W. Okes, TRW—Winner of an HP 41CV programmable calculator.

NS32032

The First True 32-Bit Microprocessor to Become Reality.

NS32032

The first commercially available microprocessor to feature:

1. *Full 32-bit architecture*
2. *Full 32-bit internal implementation*
3. *Full 32-bit data bus to memory*

The industry's consensus: with the introduction of the NS32032, the NS16000™ microprocessor family has become the foundation for the next generation of high-performance, low-cost computers.

Any software developed for the 32-bit NS32032 will run just as well on the 16-bit NS16032 or the 8-bit NS08032, and vice-versa. And it will also run on future NS16000 32-bit CPUs. Consider this absolute *downward-upward* object code compatibility in contrast to the *upward-only* compatibility of other microprocessor families, which will make their 16-bit processors obsolete when they add 32-bit processors to their product line.

The NS16000 microprocessor family already includes peripherals compatible with its CPUs, and each is in full production: the *NS16201* Timing Control Unit (TCU), the *NS16202* Interrupt Control Unit (ICU), the *NS16081* Floating Point Unit (FPU), and the *NS16082* Memory Management Unit (MMU). Since the FPU and MMU interfaces are almost entirely invisible to NS16000 programs, the decision to include or omit floating point or memory management hardware (for cost/performance reasons) will not affect NS16000-based systems' software compatibility.

The billions of bytes of existing mainframe software can now be easily ported to run on NS16000-based systems. The NS16000 family's mainframe-in-silicon architecture (designed specifically to support high level language programming), its full high-speed floating point arithmetic capability, its integral support for Demand Paged Virtual Memory, and the NS32032's 32-bit data bus to memory combine to make this possible for the first time.

Elegance, you see, is everything.

Think about it.

The only limits on NS16000-based applications are those of the imagination.

The full 32-bit architecture of the NS32032 (shared by all NS16000-family CPUs) sets no bounds to programmers' productivity or creativity.

No other processor family—micro, mini, *or* mainframe—has an architecture designed to fully support the use of high level languages, with a structure and behavior corresponding directly to the objects and operations of HLLs.

Its powerful features:

- —A compactly encoded, completely symmetrical, two-address instruction set.
- —Thirteen addressing modes (many not found in other microprocessors) designed for the kinds of accesses compilers generate.
- —Indexing automatically scaled to argument size (1, 2, 4, or 8 bytes), applicable to any addressing mode.
- —Instructions to implement high level language constructs such as case statements, loops, and calls, as well as bit-field and string manipulation.
- —A fully integrated floating point instruction set, supported by hardware.

The 32-bit architecture of the NS32032 (like that of the other NS16000 CPUs) is fully implemented, without exception or restriction.

Simply stated, physical limitations in processing or packaging technology have not constrained internal implementation. All NS16000 CPUs have a full 32-bit Arithmetic Logic Unit (ALU), a full 32-bit register set, and a full 32-bit internal data bus to the input/output control block.

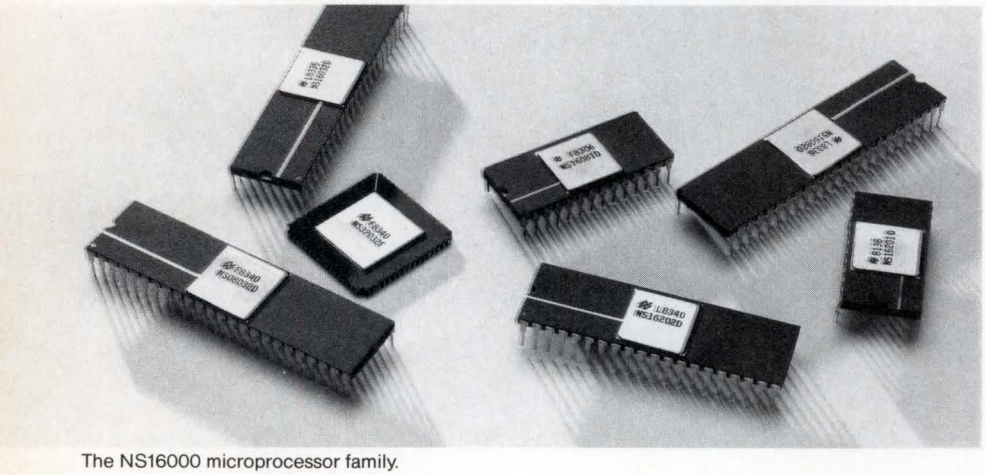
The value of such elegant implementation? An example: competitive microprocessors take eight to twenty internal steps to execute the expression evaluation "A = A * X + Ai," commonly used in high-performance technical and scientific applications.

The NS32032 takes four.

The NS32032's full 32-bit data bus to memory increases memory bus bandwidth—and thus the speed at which data can be transferred.

In simple systems (CPU and memory), the NS32032's ability to access a full 32 bits of external data dramatically increases the rate at which instructions and data are processed, while leaving bus time available for system peripherals.

Because it requires less than 50% of the available bus bandwidth in standard applications, the NS32032 is also ideally suited to complex *multi*-processor systems, DMA transfers, and high-speed graphics.



The NS16000 microprocessor family.

In the NS16000 family of CPUs, the primary feature that distinguishes one processor from another is the width of the data bus to memory.

The fact that the NS08032 and the NS16032, with their 8-bit and 16-bit data buses, share identical 32-bit architecture and 32-bit implementation with the NS32032 means that it is now possible to develop 8- and 16-bit systems with all the benefits of 32-bit software performance. The same software can now be implemented on all the systems within a product family; an enormous benefit to programmers and systems designers.

Future 32-bit CPUs planned for the NS16000 family will feature improved performance—bettering the NS32032's 1 MIPS tenfold by 1988—yet these future CPUs will also be compatible. This clear migration path guarantees the preservation of your initial software investment while providing for significant enhancement in your product line.

No other family of microprocessors shows such forethought or foresight.

TYPICAL EXECUTION TIMES (in μs at 10MHz)

		Register-to Register	Memory-to-Memory		
	Instruction	NS08032 NS16032 NS32032	NS08032	NS16032	NS32032
Mov	Byte	0.3	1.7	1.7	1.7
	Word	0.3	2.5	1.7	1.7
	Dbl.word	0.3	4.2	2.6	1.7
Add	Byte	0.4	2.0	2.0	2.0
	Word	0.4	3.2	2.0	2.0
	Dbl.word	0.4	4.7	2.3	2.0
Mul	Byte	3.8	4.3	4.3	4.3
	Word	5.4	7.0	5.8	5.8
	Dbl.word	8.6	12.0	9.6	8.4

Additional reasons why the NS16000 family now leads in microprocessor design-wins:

1. *Hardware development can begin immediately.* All three CPUs are available right now. So are all the necessary peripherals in the family.

2. *Software development can begin immediately.* Appropriate evaluation tools, and both resident- and cross-support packages, are available now, as is an extensive list of third-party software.

Our *SYS16*™—a multi-user, multi-tasking development system—incorporates the *complete* family of NS16000 chips (CPU, TCU, ICU, FPU, and MMU), and therefore gives up to eight programmers a true, native environment to work in.

GENIX,™ a product of our software engineering group, is the first microprocessor operating system capable of implementing Demand Paged Virtual Memory.

Adapted from the Berkeley 4.1 bsd version of UNIX,™ it has been elegantly tailored to optimize the NS16000 architecture. (We also offer source code under license for GENIX and its utilities.) Together, the SYS16 and GENIX demonstrate that the NS16000 microprocessor family makes the best "UNIX engine" on the market today.

For customers with VAX-11™ systems under UNIX, our GCS™ (GENIX Cross Software) contains the C compiler and other NS16000 tools from the SYS16. For VAX-11 systems running the VMS™ operating system, our NSX-16™ cross software provides full NS16000 family support.

To help complete your development cycle simply and quickly, all of our development tools provide support for our easy-to-work-with ISE/16.™ An elegant development tool in its own right, the ISE/16 allows real-time evaluation of the NS16000 chips, for testing and debugging hardware and software in your own hardware environment, and requires no target-system modification.

3. Every resource imaginable to help you get your NS16000-based application to market first is available now. We are totally committed—with in-house hardware, software, and systems expertise; with service, documentation, and customer training. We are backing the NS16000 microprocessor family to a degree unparalleled in the history of the semiconductor industry.

But then, there has never been anything like the NS16000 microprocessor family before.

NS16000

Elegance is everything.

See it.

The NS16000 microprocessor family will be on exhibition at *Uniforum* and *Electro*.

Talk with us.

Please call the National Sales Representative nearest you for more information, and the answers to your questions. Ask to meet with one of our Field Applications Engineers, too. Or, circle the number below.

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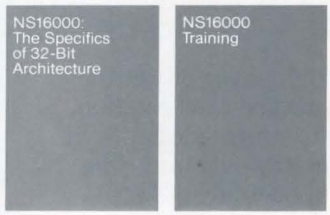

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CIRCLE 13

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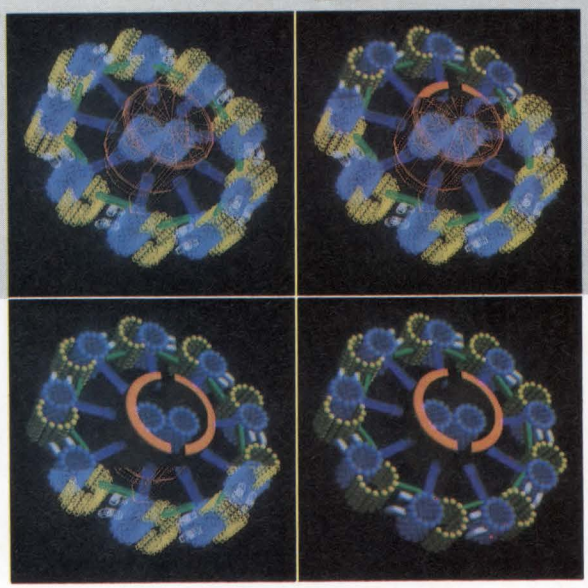

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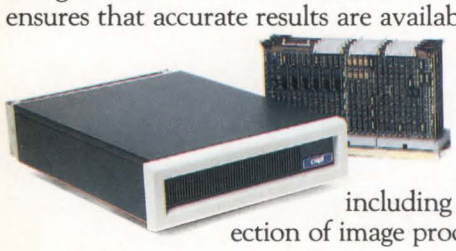

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CIRCLE 14

Thirty-two bit system designers face decision time

Computer system designers and system integrators producing leading edge equipment in the next five years will often opt for powerful 32-bit microprocessors, or 32-bit microprocessor-based boards and systems. They must hook these chips, boards, and boxes together with a 32-bit bus if they want to take full advantage of 32-bit machine functionality.

Designers can choose an open system bus, whose specifiers will cooperate with other firms to generate industry support in the form of interface, driver, and other chips needed to run a bus. Third-party firms will also produce single- and multi-board computers, software, memory, peripheral driver boards, and the like, for open buses.

Today, there are two major open bus choices—the Multibus II from Intel (Hillsboro, Ore) and the Versa Module Europa (VME) bus from the Motorola (Phoenix, Ariz), Signetics (Sunnyvale, Calif), Mostek (Carrollton, Tex) troika. In addition, there is the NuBus from Texas Instruments (Dallas, Tex), a 32-bit bus from Digital Equipment Corp (Maynard, Mass) and a 32-bit bus standard from the IEEE.

To help make an intelligent decision as to which bus to choose for a computer system's lifetime, designers should be cognizant of major and minor differences between the buses. It is equally important to be aware of how they evolved into their present form, and what they can be expected to offer from both the technical and marketing points of view. Finally, designers understand that a bus is really a local network in a small geographical area. As such, like any local network, it can be designed much like an implementation of the International Standards Organization (ISO) seven-layer model for computer communications—the Open Systems Interconnection (OSI) model.

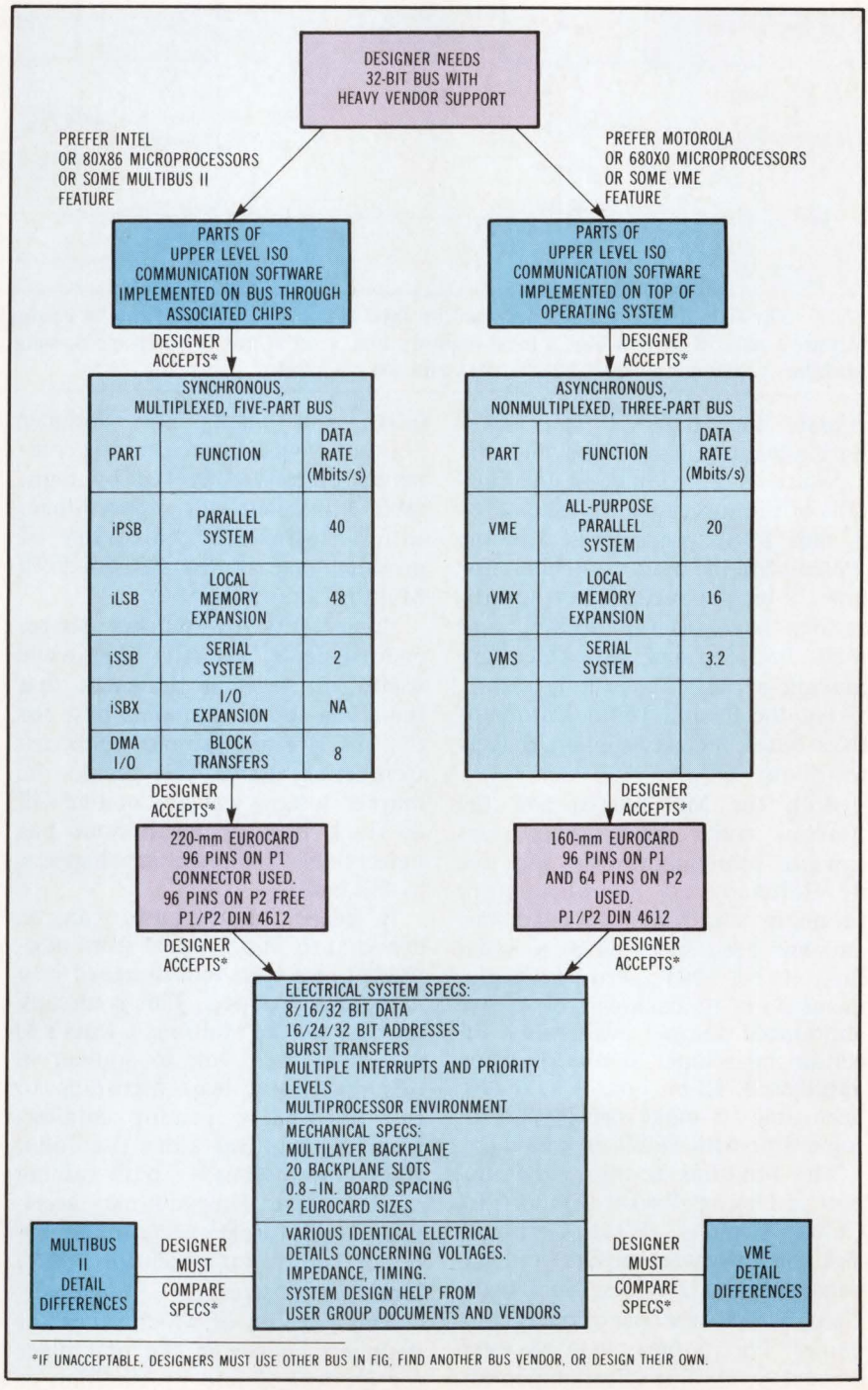

Fig 1 Computer system designers who must choose between Multibus II and VMEbus can help their engineering intuition with the data shown. If the data is not enough to reach a decision, a detailed analysis of the bus specifications is necessary.

Significantly, the Multibus II specification addresses how to implement not only the usual layers 1 and 2 of this model (the physical and data link layers), but also parts of the higher, software-based layers. In contrast, the VMEbus confines itself to implementing the first two layers in the bus with the higher layers taken care of by microprocessor operating system software. Of

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Designers face decision time

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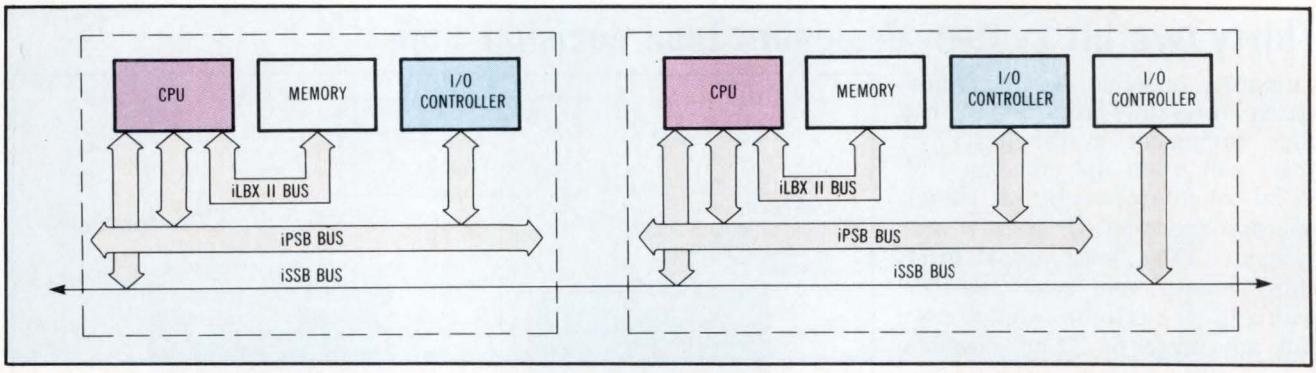

Fig 2 The five different buses designed by Intel to form Multibus II can be configured in various ways. They include a parallel system bus, a local memory bus, a serial bus for message passing, and two buses adapted from Multibus I. These I/O buses handle DMA and I/O expansion.

course, the different approaches have advantages and disadvantages.

Multibus II, (riding on the bustails of the successful Multibus I for 8- and 16-bit processors), and the VMEbus are the main contenders for new 32-bit products. Their specifications have been published, and their backers and advocates are making a major marketing effort. Given the 8- and 16-bit history of these buses, industry support is likely to follow.

Both the Multibus II and the VMEbus have made their start toward implementation and the development of complementary products. VME has had a head start and has been specified as a 32-bit bus since 1981. For example, members of its backing troika have announced sample availability for certain bus chips. Vendors making VME-based, 32-bit boards have also been able to make prototypes for some time with 16-bit processors.

The Multibus II enjoys the support of Hewlett-Packard (Palo Alto, Calif) Siemens (West Germany) Tektronix (Beaverton, Ore) and Advanced Micro Devices (Sunnyvale, Calif) as well as a host of other companies. For its part, VME has been blessed by Philips Gloeilampenfabrieken in The Netherlands (Signetics' parent firm), France's Thompson-CSF, and its own list of major and minor companies.

The gut issue for computer system designers is not who approves what bus or the size of a supporting consortium. It is what they can do with the bus for the product they have in mind, and when. This designer point of view assumes that the competing buses are backed by reputable firms that will support them with a sufficiently varied line of products—clearly the case for both Multibus II and the VME.

Projections of market share, endorsements, and the like, while useful in showing designers that there is a sound economic base for the bus, are not primary concerns. Competing giants will divide the market in some way and no one will be stuck with an unsupported bus unless one of the contenders happens to fail badly.

In reality, both buses can be expected to find support from hundreds of vendors and designed into numerous products. This is already the case for the Multibus I, Intel's 8- and 16-bit bus. Not so popular in this regard—at least according to the third-party vendor catalogs issued by IronOak Corp (La Jolla, Calif), the VMEbus is rapidly gaining market share. This gain may accelerate as Motorola's 68000 microprocessor family, for which the VME is ideal, gets onstream.

The question of which processor designers choose in the first place (or are locked into by tradition or software) is a major one for both the Multibus II and VMEbuses. Designers who opt for the Motorola 68000 or Intel 80X86 family will probably not make a detailed investigation into bus specifications. Bus functionality at least for the next few years of microcomputer products, will remain about the same. So, many designers will pick the bus associated with the manufacturer of the processor they have chosen and assume they best support each other.

Erstwhile computer system designers need a comparison of the basic specifications of the Multibus II and VMEbuses to determine whether one can be rejected out of hand (Fig 1). A detailed comparison of bus specifications determines more sophisticated rejection criteria. Any one of the specifications can eliminate a bus from further consideration—eg, multiplexing or asynchronous behavior.

Some users find the plug-and-socket connector in the VMEbus (introduced in Nov 1981 as an 8-, 16-, or 32-bit data width bus) to be more reliable than the Multibus I's edge connector. In any case, Intel has come up with a Deutsche Institut für Normung (DIN) plug-and-socket connector for the Multibus II design (introduced at the Las Vegas Comdex show in Nov 1983), so connector reliability is not an issue.

Intel's Multibus II offering comprises five, "software configurable," connectable buses. The fastest bus is a 32-bit wide, synchronous communications, 10-MHz bandwidth system bus that links single-board computers, microprocessors, memory, I/O, and other components. The system bus can handle a theoretical maximum of 40 Mbytes/s in a burst mode.

The second new Multibus II offering is a local bus extension designed to hook local memory to a microprocessor. It runs at 12 MHz

for up to 64 Mbytes of memory that must be accessed by a microprocessor without contention problems.

The third member of the bus quintet passes messages between software processes in a serial mode at 2 MHz. This bus member and the 32-bit parallel system bus have what Intel says is the "same interface for VLSI chips," thereby making them software compatible.

The last two Multibus II parts are a multichannel DMA bus for I/O and an I/O expansion bus that have been adopted from the Multibus I. Fig 2 illustrates how the five different buses function in a computer system.

Because of the large amount of software that has been written for the Multibus I devices, continuing software compatibility with the Multibus II is an Intel goal. For Multibus II project manager Frank J. Costa of Intel's Hillsboro, Ore facility, such software compatibility "is a matter of writing new device drivers," a chore he does not think is too difficult—at least for Multibus I software porting to Multibus II without tapping II's new functions. Just how complex a chore it is depends on the microprocessor or computer operating system used. In any case, according to Michael Klever, VMEbus marketing manager at Philips (Einhoven, The Netherlands), the fact that Multibus I is asynchronous and nonmultiplexed while Multibus II is neither, greatly complicates the chore. He also notes that Multibus I software cannot implement the upper-level ISO software features under development for Multibus II.

The VME, NuBus, (see Panel, "What's Nu?") and the IEEE bus (see Panel, "A matter of diplomacy") implement layers 1 and 2 of the ISO model. But, as mentioned, Intel has done more in its bus specification. The additional, upper-layer ISO software on Multibus II has no software counterpart in Multibus I's specification and is implemented in Multibus I systems by adding software to the attached microprocessor's operating system.

On the one hand, Intel's Multibus II software design approach may take some of the software burden off designers. However, it may force them to do things Intel's way. Clearly, Intel has differentiated its bus product but has taken a risk.

VMEbus modifications

Until recently, the VMEbus has meant a single, 32-bit wide, asynchronous data path, dynamically configurable by the attached computer system into either a data-transfer bus, a seven-level priority interrupt bus, a four-level arbitration bus, or a utility bus. However, Motorola and its colleague companies, although enjoying their two-year lead time in the 32-bit bus business, have not been idle.

Besides announcing new VME interface chips and stimulating their user groups last Nov, the Motorola, Signetics, and Mostek troika announced additional buses for the VME architecture. These include a high speed memory expansion bus (the VMX bus), and a self-arbitrating high speed serial bus that can be used in the existing VME bus, as seen in Fig 3.

As mentioned, Motorola's buses use ISO layers 1 and 2 only. For Motorola, system software functions that correspond to higher ISO software layers are best handled in software that rides on the microprocessor operating system, not in the bus specification. Once the software is well defined, it will be implemented in hardware. In any case, system software considerations are being worked on by both Intel and Motorola.

The details of the VME and Multibus II bus designs in Fig 1 and the bus specifications are best understood by specialists. For Motorola's John A. Black, Jr, manager of systems and technology at the firm's Tempe, Ariz operation, this means that bus-pickers will have chosen a bus from the company that makes the processor they prefer. "Moreover," he adds, "most bus details concerning ISO layers 1 and 2 that are talked about to help make a distinction between VME and Multibus II are rather small points. Neither bus stands out above the other."

According to Black, the products available for each bus are the primary considerations. Designers are pressed for time, and Black points out that it will take a year for Intel to have Multibus II products on the market. "In contrast," says Black, "VME customers can start work with 16-bit VME boards now, and the software will run on 32-bit versions since the 68000 family software is upward compatible."

As might be expected, Intel has a similar point of view for its microprocessors and buses. However, Black says that the upper ISO layer-like software, (eg, message space mapping), that Intel features on its Multibus II is not supported by the present Intel Multibus I hardware or

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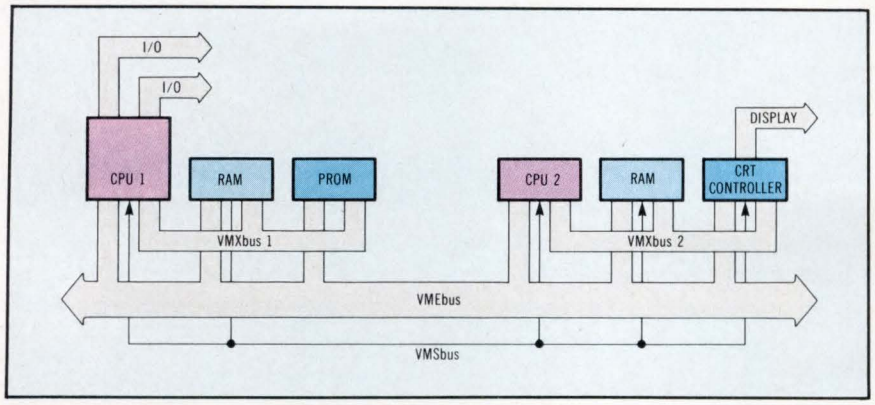

Fig 3 In its latest version, Motorola's VMEbus is no longer a single, multifunction parallel bus that is configured to do all system chores. It has two partners: the VMSbus handles serial chores like message passing; and the VMXbus connects CPUs to local memory or other devices.

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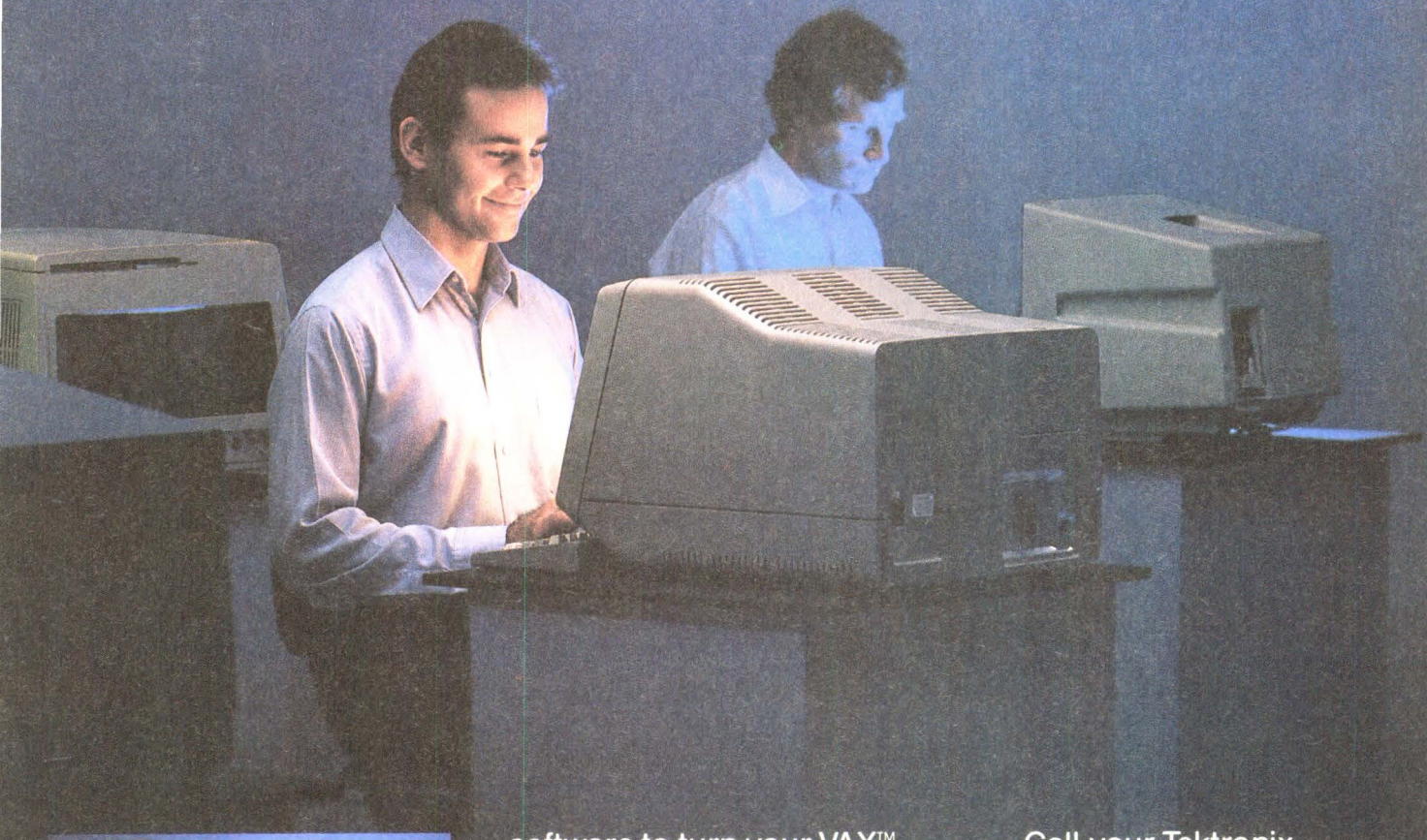

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Designers face decision time
(continued from page 29)

What's Nu?

Although the 32-bit, 10-MHz synchronous NuBus is not being promoted by TI with the same intensity as the VME and Multibus II buses, it has nevertheless been proposed by TI to the IEEE 896 committee for consideration as the basis for a 32-bit synchronous bus standard. It is also being used in a TI-developed technical workstation introduced in Jan 1984.

According to George P. White, who is both the 896.2's coordinator, synchronous version task group, and TI's Nu Machine development manager, NuBus was originally developed by MIT for workstation research in artificial intelligence, networking, and office automation. Western Digital licensed it from MIT and TI took over the license from Western.

NuBus is designed to be as processor-independent as possible, White says, since MIT, Western, and TI have no specific processor interest. For example, the artificial intelligence workstation known as the Lisp Machine from LISP Machines, Inc (Culver City, Calif) has a four-board, bit-sliced, microcoded MSI processor that operates on a NuBus.

While TI would "like to see industry standard boards based on the NuBus", and it has converters, (eg, to hook up NuBus cards to Multibus I cards), it has "not yet decided to what extent it will try" to accomplish this goal. Current TI activities include, for example, rewriting of the NuBus specification to make it more user-friendly. In addition, TI designers are looking into certain system aspects of the bus and how they could be hardware- or software-implemented.

"NuBus is designed to implement layers 1 and 2 of the ISO model," White reports, noting that this helps in keeping it processor-independent since "the more ISO levels 3 through 7 (or parts of them) are implemented in bus specifications, the more the bus is tied to system architecture and the more processor dependent it is."

software. Therefore, software rewriting and reconfiguration will be needed.

All those details

Eschewing the bus specifications battle, Tom Hunter, systems program manager for VME products at Mostek, says that computer designers should opt for the VMEbus because it is available today. Hunter, who has technical responsibility for VMEbuses also says that there is no clear technical distinction between the Multibus II and the VMEbus as far as system designers are concerned—both can be made to handle most jobs. "After all," Hunter says, "we are all still working with Von Neumann architectures. True multiprocessing, the next stage of the hardware art which requires a radically different bus design, is not yet with us." (See Panel, "In the wings").

Agreeing with this viewpoint—but not with the view that designers should opt for the VME—is Intel's Rob Hughes, marketing development manager within strategic marketing at the firm's Hillsboro, Ore facility, and Intel liaison person with the Multibus II manufacturers group. For Hughes, "Buses are becoming more alike—in fact, part of the Intel bus specification is part of the Motorola bus specification." For its part, Motorola, points out that part of the VME specifications can be found in Multibus II.

Clearly, both buses will be well supported as their backers fight hard for the dominant share of what they perceive is a large market for 32-bit microcomputers. In fact, Hughes notes that pragmatic engineers, confused over which bus to use for their new designs, could probably choose either and do well. "But, that's today," he adds. "The real question is which bus will be around a few years from now and which will be supported by a wide variety of sources."

For Hunter, the distinction between buses is more a question of which microprocessor family computer designers are going to use. Supporters of both buses claim that different microprocessors can be accommodated. However, Hunter says there is no question that the VMEbus is designed to work best with Motorola's 68000 family and the Multibus II with Intel's 80X86 designs. And there, Hunter claims, is an important difference for designers.

Other engineers and marketeers at the firms involved said that both buses could accommodate all common proccessors but it was a matter of how many glue chips would be needed, what software modifications would have to be made, and whether any throughput problems would arise. All agree that the issues are complex and best addressed on a case-by-case basis.

VME partisans feel that an asynchronous bus is better suited for a variety of processors since it is not locked to a fixed clock frequency. Other observers feel that Intel's Multibus II, because it includes some upper-ISO level software, fixes certain system design details, thereby making it more processor-dependent. Such dependency would be for the 80X86 family, which can be expected to be the first to implement the ISO-based software.

Asynchronous or synchronous?

Although the synchronous Multibus II bus makes provision for different device speeds by interfacing and translating them to its 10 MHz, there are more timing constraints than with an asynchronous bus. However, Intel's John Beaston, product marketing manager, points out that bus interface chips can accommodate a variety of speeds with no trouble. Furthermore, they can do this at little incremental cost in their VLSI versions, which will perform many other chores. He says there are also speed translator chips all over the VMEbus even though it is asynchronous.

(continued on page 34)

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Designers face decision time
(continued from page 32)

A matter of diplomacy

In what might be called bus diplomacy, Paul Borrill, Research Fellow at University College in London, England is chairing the IEEE's P896 committee. The committee is charged with setting a standard for an asynchronous, 32-bit bus known as the Futurebus. Borrill's committee works closely with P896.2, an IEEE P896 group handling a synchronous, 32-bit bus standard (headed by another bus diplomat, Task Group Coordinator George White at TI's digital systems operation in Irvine, Calif).

According to Borrill, the work of the 896 committee is complete as far as the asynchronous bus is concerned and its documents are out for public comment after some five years of work. "Several companies are prototyping to this specification even though they have their own bus," Borrill notes, mentioning Tektronix. In contrast, much remains to be done on 896.2, which only recently started its work.

Intel will introduce its Multibus II specification for consideration as the 896.2 standard (or as an 896.2 implementation) at the Feb 1984 Compcon meeting in San Francisco. TI's 32-bit NuBus (out of Western Digital and MIT and already presented to P896), belongs in 896.2's domain, as does Digital Equipment Corp's new 32-bit bus. "Multibus II is being proposed as a basis for 896.2," Borrill says, adding that the IEEE bus committee goal is to reduce the number of buses available, not increase them.

As far as the asynchronous VMEbus is concerned [it conforms to IEEE specification in P1014], Borrill says it has a simpler bus interface implementation and a simpler system implementation for single and multiple processors and is very well optimized for its applications." The VMEbus follows the traditions of the Multibus I, the Motorola Exorcisor bus in that it is asynchronous and non-multiplexed, and the STD bus, Borrill says, adding that it provides more features and a higher performance than both of them. "Its performance is even better now that it has secondary buses on which to put communication overhead traffic. This will be of great help in a multiprocessor environment where all buses have bandwidth problems."

Borrill's reflections on various IEEE committee efforts to standardize buses shed interesting light on some VME versus Multibus II controversies. The 896 committee consensus was that the most processor-independent bus was asynchronous. On the other hand, the question of whether asynchronous or synchronous buses are better for high performance takes on "the tone of a religious argument with passionate believers on both sides." As far as the original intent of the committee is concerned, Borrill says that the intended application of Futurebus is high end, fault-tolerant systems, while 896.2's application is medium-range, 32-bit markets.

Yet to come from the 896 committee are specifications (for both synchronous and asynchronous buses) that define how to take care of software chores in the next layer of the 896 architecture. These include specification of identical address mapping on both buses, specification of identical error control methods, and specification of the same method of accessing the bus with a higher level protocol, such as a message passing protocol. These specifications will move software transparently between any 896 asynchronous or 896 synchronous bus without changing a line of code.

Bus specification accomplished so far for the 896 committee is equivalent to the physical and data-link layers (layers 1 and 2) of the ISO seven-layer model for computer communications. DIN connectors and Eurocard boards are equivalent to layer 1 and the bus communication protocol is equivalent to layer 2. Now the committee would like to consider implementing higher level communication-oriented protocols that can be built into the bus interface. For its part, Intel, with its message passing and error detection schemes in the Multibus II specification, has already taken a step toward implementing some higher level ISO functionality in the bus itself.

The 68000 and 80X86 families are said to work with either an asynchronous or synchronous design. Asynchronous is more flexible, Hunter says, adding that the 80X86 family functions best with a synchronous bus. Intel's Hughes and Beaston disagree, each noting that Intel's processors work well with the asynchronous Multibus I and are being designed onto VMEbuses by third-party vendors.

While the asynchronous versus synchronous question rages, there are more mundane considerations in bus design. For example, Intel's opting for a longer Eurocard (220 mm instead of the VMEbus 160 mm) for its board may be a short-term advantage but a long-term disadvantage. Today's designers may need the room but, as chip integration technology improves, and more functions are crammed onchip, less board space may be needed. On the other hand, it may be that additional space will be needed both today and tomorrow as more functions are put on a board. Indeed, TI's NuBus board is 60 mm longer than Intel's—the next step in the Eurocard standard.

More to the story

There is more to bus design than how to take care of ISO levels 1 and 2 (or higher). Rick Main, the VMEbus manufacturer's group secretary, manager of microsystems engineering at Signetics, and designer of both Intel- and Motorola-chip-based computer boards and systems has found that the practical hardware and software problems of

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In the wings

While the VME and Multibus II buses are the major contenders right now for 32-bit bus honors, they are not without competitors in the long run. Digital Equipment Corp is working on a 32-bit bus design that will hook up machines based on its PDP/11-70 minicomputers into a distributed, realtime multiprocessor network. Philips and Intel have such designs in prototype form but DEC has wired systems together and is working feverishly on developing software to make them run with all the DEC applications.

Called variously the BI-bus (for bus interface bus), the enhanced Q-bus, and the Q-32 bus, DEC's bus will help DEC minicomputers compete with the microcomputer and supermicrocomputers whose functionality has been migrating up into the traditional minicomputer area. In short, DEC, pressured by the increasing power of micros, has increased mini capability, but it will soon directly counterattack the micro world with its 32-bit bus mini-based system.

The new bus will not hurt the sales of DEC's computer boards, which have made a strong industry mark. Moreover, if DEC opts for an open bus with all its specifications made public, it may well compete with Intel and Motorola for third-party vendor support—as may TI if it decides to push its NuBus.

The choice between the VME and Multibus II will be easier as both Motorola and Intel further define the system functions mentioned and how they are implemented. On the other hand, DEC could complicate matters with its impending 32-bit bus if it is indeed different. According to IEEE's Borrill, DEC's bus is "far more radical in design concept than the Multibus II."

making real, bus-based computer systems have general applicability. According to Main, both the VME and Multibus II user groups and the written bus specifications deal with these practical issues.

First, there is the problem of the internal design and operating environment of the boards that vendors furnish for bus connections. Some design and environmental standards would be useful. Main also notes that power distribution, electrical noise, and thermal problems must also be solved in practical computer systems. It would be helpful if the bus specification provided guidance. This is especially true now that standard buses and standard boards mean there are more nonexpert computer system designers.

Then, there is the software problem. With readily available industry-standard languages, operating systems, compilers, and the like for realtime, multitasking, and multiuser applications, designing one's own software is unnecessary except for highly specialized applications. The real problem is integrating software with hardware—especially when both are developed by different vendors who are not in contact with each other.

According to Main, some of these software/hardware integration problems can be addressed by appropriate system specifications. For example, if a bus has standard I/O driver interfaces, board vendors can supply software drivers with their boards and users can integrate these drivers into their operating systems. This allows modular replacement or reconfiguration of systems but without the operating system impact.

Bus manufacturers and bus standards can bring about software standards for coprocessor chips for floating point algorithms. And, as operating systems are standardized, standards will follow for assembly language commands to create software tasks, wake-up tasks, send messages, and more. Once standardized, these algorithms can be implemented in faster hardware that plays well with a particular bus design. Both Motorola and Intel promise VLSI to help reach these goals.

Software must also work with hardware to perform such chores as power-fail recovery and automatic operating system configuration to fit the hardware on which it is running. Main says these are ambitious chores for any bus but at the very least, "guidelines can be established if not full-fledged specifications for getting the job done." Some of this material is under review by both Motorola and Intel, and Intel has gone so far as to specify (in Multibus II) ways to accomplish several of the important tasks.

A look at system issues

System issues separate the Multibus II from the VMEbus since the VMEbus (combined with the VMX and VMS buses) functions in a way similar to Multibus II—at least for the next few years. In fact, both Motorola and Intel feel that 32-bit data paths are just part of the increased functionality needed by 32-bit systems, and system attributes like ease of use, reliability, and multiprocessing capability are equally important.

As far as ease of use is concerned, Intel's Beaston says that the Multibus II specification makes it software configurable compared to the hardware-configurable VMEbus. He notes that many of the jumpers and spikes on a Multibus II board are eliminated, since starting addresses, interrupt vectors from memory, and the like are more readily handled by Multibus II.

Motorola's Black disagrees, pointing out that auto-configuration or automatic system generation are but one part of the different bus design philosophies of Intel and Motorola. Motorola is working on a system specification to be released in mid-1984. The document will address system software modularization and its hardware module implementation, including such factors as automatic configuration.

This specification will respect the separation and independence of the upper-ISO layers. Unlike the Intel approach, it will not specify how parts of the layers should be implemented by the bus specification. According to Black, Motorola believes that system software implementation is

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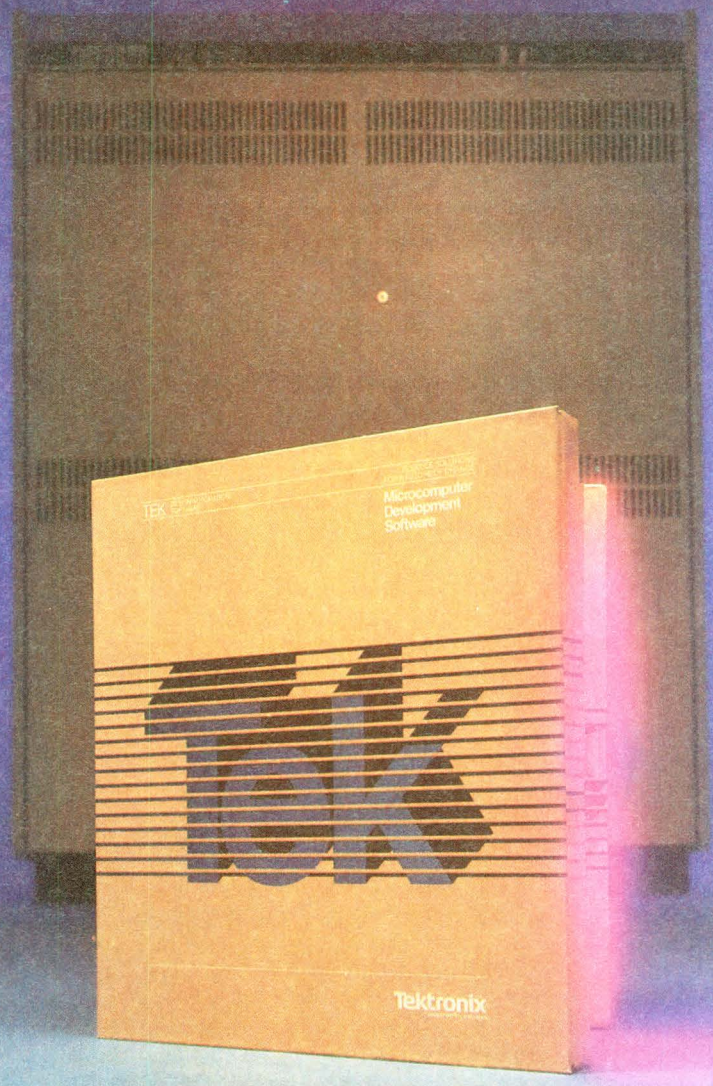

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Designers face decision time

(continued from page 36)

best done by system designers to suit their own needs. This means using the operating system, not the bus, as a foundation.

"Software configuration is flexible but costly in board real estate and board performance," Black says. "Moreover," he adds, "it's hard to do halfway with some done by the operating system and some by hand. It also needs operating system intelligence resources and memory; our experience shows it's not something customers are inclined to pay for."

Beaston also claims that remote diagnostics are more readily handled by Multibus II. For example, having the interconnect address space in the bus specification to allow designers to identify boards by their physical position in the backplane facilitates implementation of the diagnostics facility. Motorola's view is that such a use is best built on top of the microprocessor operating system at designer option (today in software, tomorrow in hardware) and not into the bus specification with a predefined method and addresses.

As far as comparative bus reliability is concerned, there is the matter of error detection. Multibus II has a nonoptional feature that allows parity checks for error detection on data transfers so that a processor has an indication that something is amiss, and can abort or retry if necessary. Multibus II is also designed to allow the detection of operational errors. For example, a request for a 32-bit read on an 8-bit I/O line will cause an error indication, as will several other operational errors. These chores are taken care of by the Multibus II protocol.

There are several other reliability considerations. For one, Multibus II data samples are said to be taken so that they have less noise sensitivity than VME samples. Beaston claims that the connector pinout is better designed than that of the VME since the different signal groups are shielded from one another. In addition, there are more ground lines for better noise performance as well as more power pins. Finally, there is less crosstalk since the pins are multiplexed and fewer lines are switched at once.

Black has a different point of view regarding relative bus reliability. He again points out that Intel is forcing a procedure on computer designers by insisting they use parity checks and pay the board space and speed penalty. Parity found on VME memory boards is a valid concept for memory but is not valid for bus drivers. Unlike RAMs, they are not likely to break down before the system mean time before failure (MTBF) calls for a system breakdown.

The VME approach to error diagnosis is to handle it in the microcomputer operating system where the operating system software handles all possible system errors and communicates with the system hardware to take care of them. In contrast, Multibus II handles some errors in its bus specification and would have to handle others in the operating system. In Black's view, this is an improper partitioning of operating system functions.

For Black, Beaston's comments about Multibus II's superiority in noise behavior, crosstalk, and pinout are not relevant, given today's advanced backplane technologies and multilayer boards. "There are no edge-sensitive noise, high frequency grounding, or shielding problems with the VMEbus," he says.

Lots of processors

Perhaps most important from the point of view of future designs for a multiprocessing environment, Beaston says that Intel's Multibus II is better designed for many processors than the VMEbus.

Normally, when a multiprocessor computer system shares memory, its processors must work with overlapping memory space. If there are more than two processors, there are likely to be address aliasing problems for the microprocessor's operating system to manage. The microprocessor has contention and pointer manipulation chores to handle and can do nothing else when it is so occupied. The Multibus II philosophy is to take care of part of the support for multiprocessor data sharing in bus interface hardware. For example, an 8-bit 8088 can

(continued on page 40)

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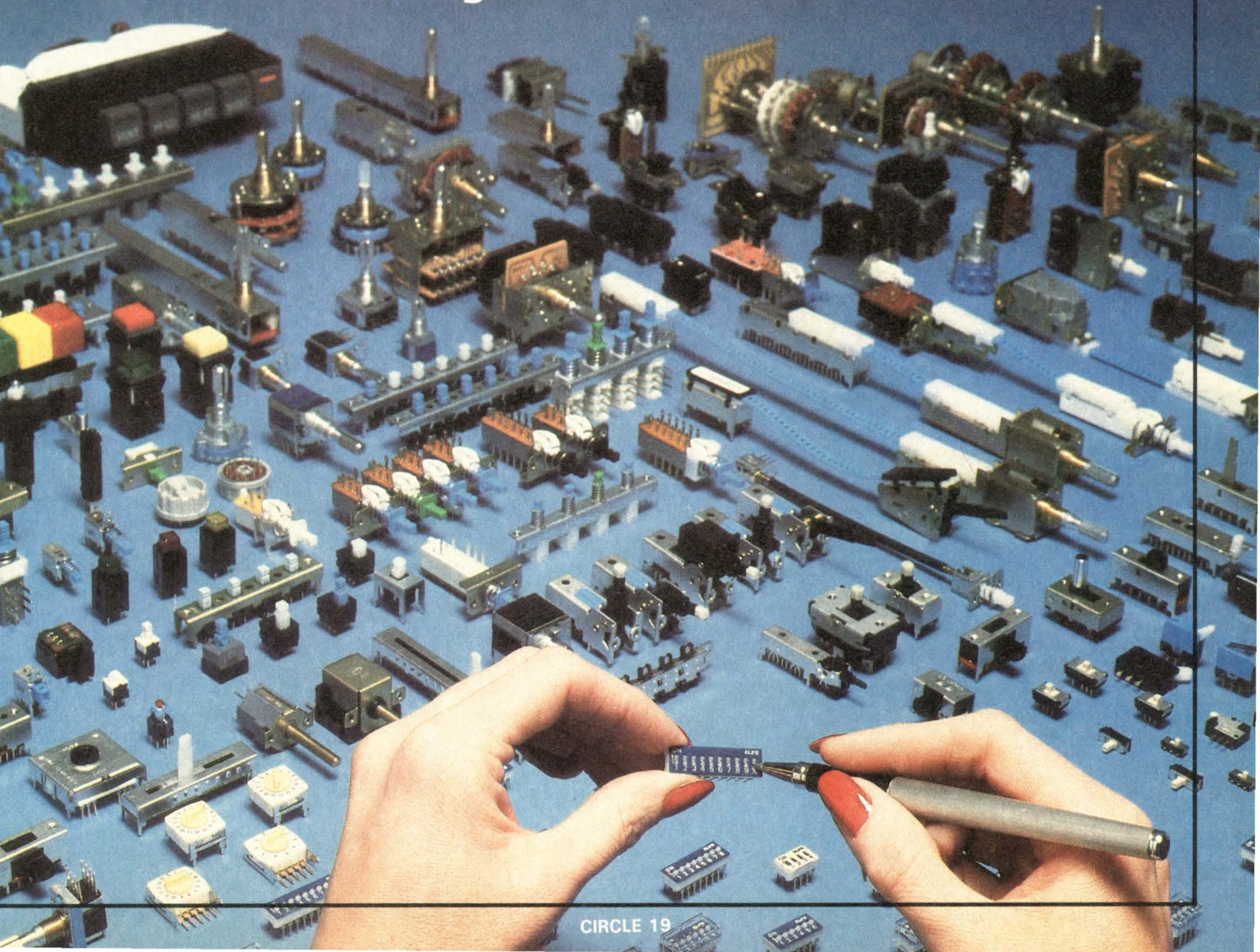

CIRCLE 19

Designers face decision time

(continued from page 38)

control message passing in a 32-bit wide burst transfer interface.

Such a procedure is not possible with the VMEbus, which does not have a mechanism in its specification to do it, Beaston says. He adds that the VMEbus would require a separate address space in the bus specification to take care of message passing in the bus interface hardware and it cannot be added.

The VME manages data sharing by means of pointer passing on its VMS serial bus. According to Beaston, this is inferior to the Multibus II's approach because its 32-bit parallel bus would pass a 32-bit pointer in one clock cycle (32 times faster than the serial bus) even if their speeds were the same—and the parallel bus is much faster.

For Motorola's Black, the VME has unsurpassed multiprocessing capabilities. "All multiprocessing systems need, and will do, message passing, and the VMEbus has a memory map for messages," he says, adding that the real question is where in the system you define the mapping. According to the VME system plan, the VMEbus will pass messages over either its serial or parallel buses under control of the microprocessor, not the bus.

The VMEbus's realtime executive in its operating system takes care of all message passing with what is known as "address modifier codes." In contrast, Intel has divided message passing so it is partially handled by the bus specification and partially by operating system software. All Multibus II has done so far, Black maintains, is define a message space—a separate page of memory—and specify some registers without saying what goes in them.

According to Black there are no inherent limitations to the multiprocessing capability of the VMEbus which might make it inferior in any way to the Multibus II. He goes on to say that the number of processors that can be handled is a function of the application, and such factors as bus arbitration efficiency.

The two bus arbitration schemes are basically equivalent, Black says. As both buses have the same number of backplane slots, both arbitration schemes will accept a processor board in each slot, and bus arbitration (even though the VMEbus is marginally faster) is not a major factor since both buses arbitrate concurrently with bus activity.

The only remaining factor is how fast designers can move data through the bus and, as Black puts it, both are subject to the same laws of physics. For real world block transfers using real memory and other components designers can buy, not theorize about, the buses have equivalent throughput for block transfers, Black says. He adds that the VMEbus can do twice the transfers of a Multibus II for a single-cycle access because it is not multiplexed.

—Harvey J. Hindin,
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SYSTEM TECHNOLOGY

(continued on page 49)

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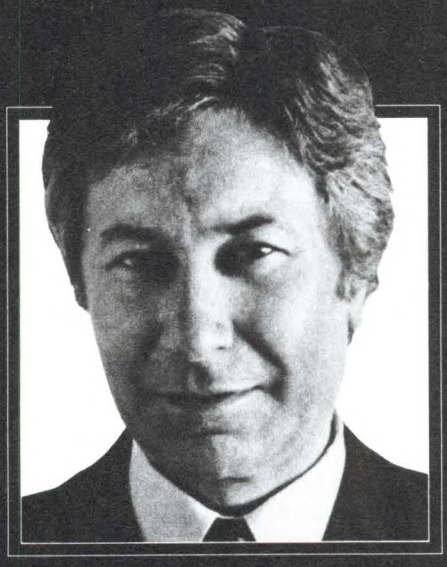

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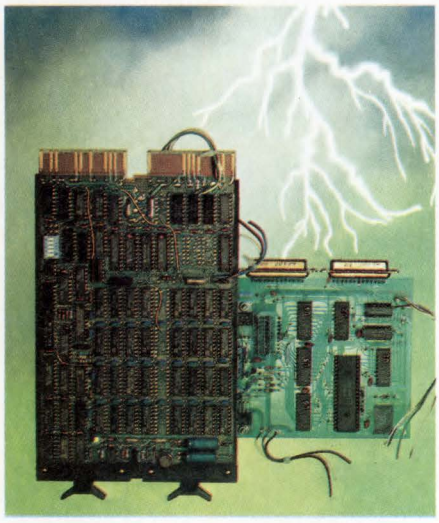

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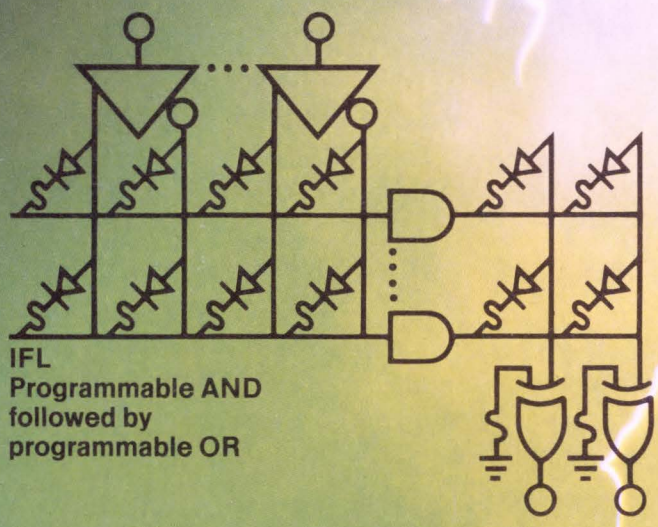

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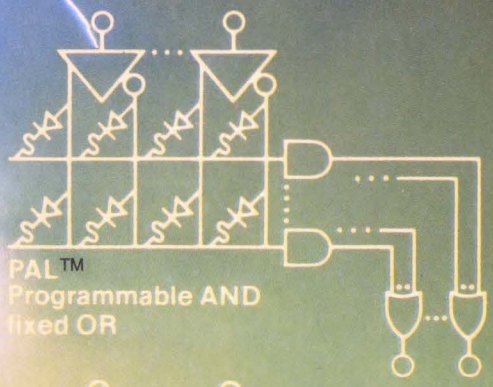

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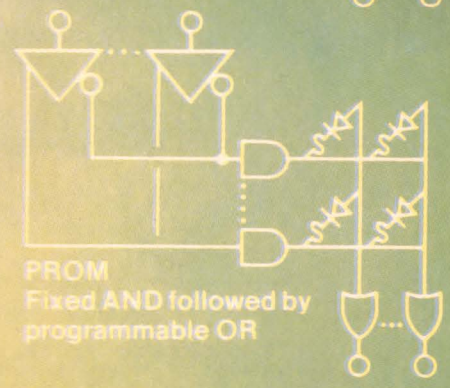

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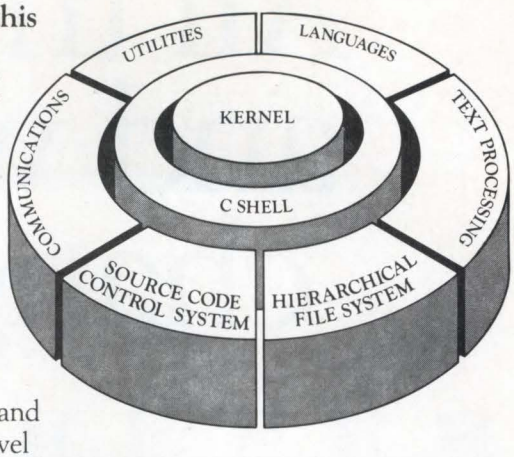

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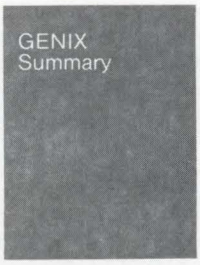

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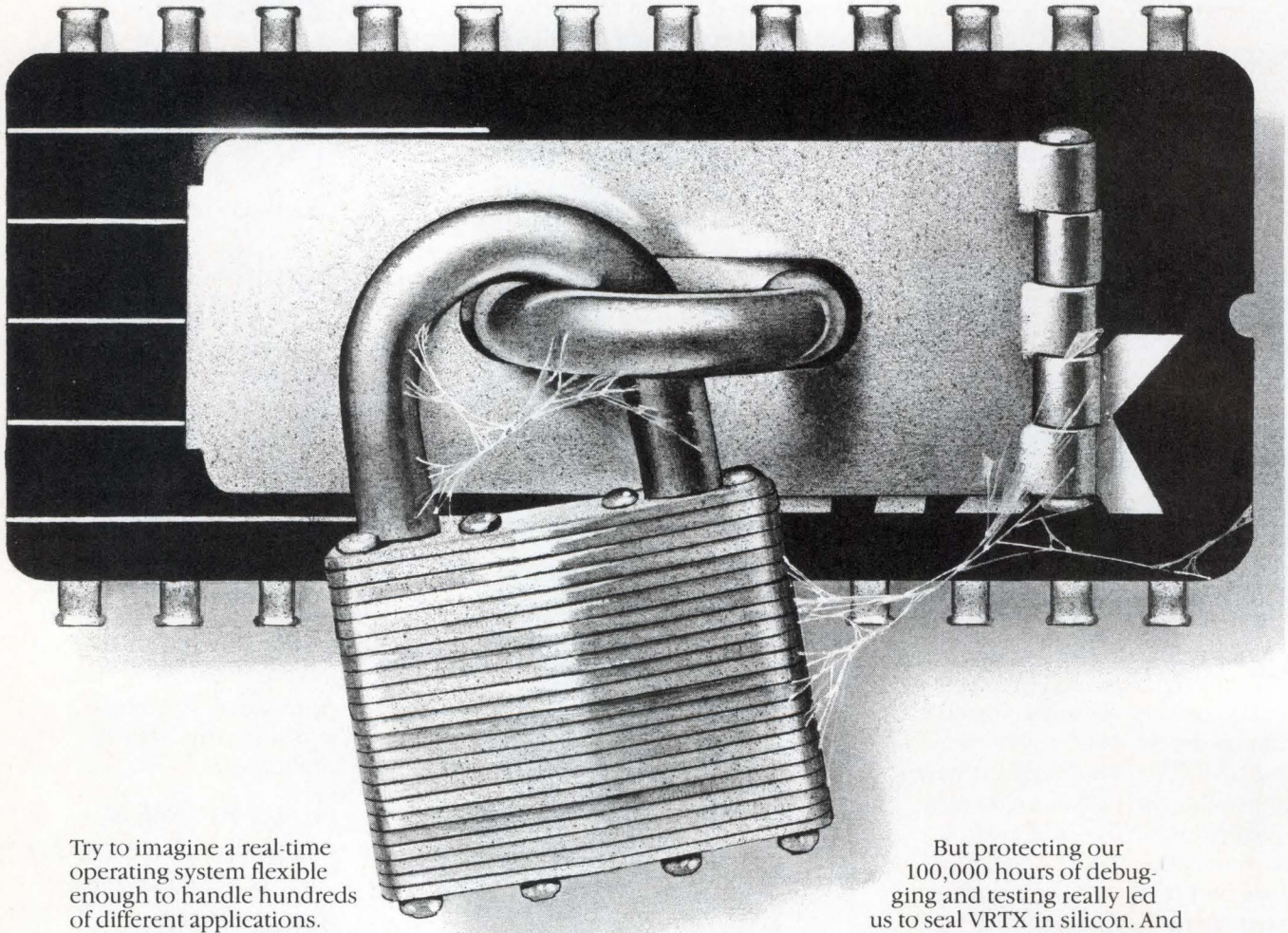

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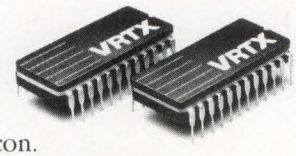

Operating systems in silicon.

Local area networks proliferate while standards lag

Since VLSI devices and interfaces to support them have appeared, local area networks (LANs) have been multiplying like rabbits. The advantages of connecting relatively cheap workstations to expensive file servers and graphics peripherals are obvious, as is the need to connect to mainframes with superior computing power and database structures.

The problem, however, is that individual hardware and software vendors have gone haring off in separate directions. Each provides relatively easy interconnection between users of their particular products, but no simple way of transferring data or programs to other systems.

The resulting incompatibilities, like the chaos of floppy disk formats, are a disservice to the industry and the consumer. The real and pressing need, at all levels of the computer industry, is for a free flow of data and information among all levels of machines and users.

Purely commercial concerns—locking users into a particular hardware/software combination—will prove counterproductive in the long run. Telecommunication managers are already beginning to see that a 10-Mbyte/s Ethernet link, with expensive cables, interface hardware, and installation, is not much good if the machines at either end of the link cannot understand one another.

Creating a local network interface is a fairly straightforward technical problem that can usually be solved relatively quick. Standards, on the other hand, are a political problem involving a large number of people and the reconciliation of conflicting points of view. Technology, as usual, is outrunning the political process.

Considering implementations

DR Soft/Net, from Digital Research, Inc (Pacific Grove, Calif), implements the session and transport layers of the International Standards Organization (ISO) interconnect standard. It is basically a distributed file-serving mechanism that allows various machines running Digital Research operating systems to share data files and use remote peripherals.

Its strength is in its modularity. Each function is a self-contained routine that other functions access via strictly defined interfaces. Data and service requests are passed between modules in a standard and easily understood way. Thus, details

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LANs proliferate

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are effectively hidden and design effort can be concentrated on the job at hand.

Implementation of this modularity (which has received much academic attention over the last 20 years) is Digital Research's technical contribution to the computer field. By putting all hardware interfaces into one module, basic I/O system (BIOS), file handling in another, basic disk operating system (BDOS), and a simplified user interface, console command processor (CCP) in another, Digital Research has created a flexible operating system. This system has made writing relatively inexpensive application programs feasible and quick.

Soft/Net continues the tradition of modularity, and was designed to make it easy for manufacturers to configure for particular hardware. The strictly logical component, network disk operating system (NDOS) is provided in both 8-bit (8080/Z80) and 16-bit (8086) versions. Hardware connections network I/O system (NIOS) are presently available for Ethernet and Arcnet, with documentation available for adapting to other transmission media.

File sharing, password protection, record and file locking, and remote peripheral use are all supported by Soft/Net. The first release of Soft/Net will be as part of Concurrent CP/M-86 next month. This package will allow remote operations to go on in the background, while other programs are running.

However, the weakness of modularity is that the user is dependent on the functions that the vendor has chosen to include. CP/M has been criticized for allowing only four I/O devices apart from the disks—a Teletype (CON:), tape reader (RDR:), a punch (PUN:), and a line printer (LPT:). Each of these four logical devices can be dynamically connected to any one of 12 device drivers, but the choices are not many. Nonstandard peripherals must often be driven directly from the application program, defeating the concept of modularity.

In providing the NIOS for Soft/Net, and the Graphic I/O System (GIOS) for the recently introduced graphics system, the company has begun to address this weakness. Given the company's announcement that development work is now being done in the C language, further modular extensions of the basic operating system can be expected. High level source code will also make possible, for better or worse, porting to new processors. CP/M-68K (for Motorola's 68000) is already available, and rumors about an implementation for the 16032/32032 are circulating.

A technical problem with the CP/M file structure is that it is flat, consisting of a single list of files with 8-character names and 3-character

extensions. Hierarchical files (eg, PC-DOS 2.0 and Unix) can probably be expected in the future, especially since Digital Research has been chosen to complete the Unix implementation for Intel's 286 processor. With the simultaneous increase in capacity and decline in price of mass storage (eg, 100 Mbytes on a 5¼-in. Winchester) the hierarchical file structure, in one form or another, should become the standard for 16-bit and larger systems.

Unix to PC networking

Distributed processing, using the most widespread, commercially available desktop microcomputer, is the goal of an Ethernet-based Unix network recently announced by Plexus Computers, Inc (Santa Clara, Calif) and LanTech Systems (Dallas, Tex). The network lets users of the IBM PC take advantage of Unix files, utilities, and multiuser capabilities.

LanTech's uNETix, a single-user Unix-compatible operating system for the PC, includes software interfaces to Plexus' network operating system (NOS). Together with a standard Ethernet interface board, the system turns the PC into a very intelligent distributed workstation with access to the resources of a supermicrocomputer. It is available 90 days ARO for $250 from LanTech.

Modularity is built into Unix, although the granularity is different than in CP/M. All data is treated as a character stream—a one-dimensional series of bytes. Programs accept streams through their standard input, process them, and emit them from the standard output.

This approach facilitates the creation of software tools. These small, well-understood, and tested programs can be strung together easily to do any job needed. It also makes a hierarchical file structure imperative, to keep the hundreds of small tools from cluttering the programmer's "workbench."

Strictly defined and adhered to, a character stream approach also imposes time and space penalties on applications, such as data bases, which use two- (or more) dimensional data structures. Transferring a large data array byte by byte can be a long process.

Vendors like Plexus are working to make a distributed Unix environment a viable competitor to IBM's 3270/SNA network connections to and between mainframes. While it is undoubtedly a good environment for programmers to work in, Unix has been described as being "user-hostile." The face it presents to the casual user is both cryptic and confusing.

While IBM's batch-processing interface may leave much to be desired, particularly in the realm of job control language, there are a

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LANs proliferate

(continued from page 51)

host of productivity tools, text editors, and utilities (eg, SPF) are available from both IBM and independent vendors. These tools and interfaces, called shells in Unix, are being developed, and even exist in full form at some installations. However, they are not generally available to the business user.

More specifically, this uNETix-Ethernet combination competes directly for board and disk space with IBM's recent PC/3270 (for communications) and PC/370 (for executing mainframe software in the PC) products. Neither system makes provision for communicating with the other—except, perhaps, by writing data to the PC disk, and rebooting with the other operating system to read it. This is, however, an inherently slow and clumsy process. In the absence of formal standards and user demands for compatibility, manufacturers will continue to create technical solutions that cause intercommunication problems.

Unveiling a new "standard"

Billing it as "The standard in network software," SofTech Microsystems (San Diego, Calif) has introduced Liaison, a networking implementation of the UCSD p-System. Liaison includes a limited multiprocessing operating system ($750 to $4000, depending on number of users), a disk server ($150) to manage files for remote users, a print server ($150), and a tool kit ($200) to help develop Liaison systems.

The system is presently available for the Apple IIe, IBM PC, TI Professional, and Corvus Concept computers. It communicates via the Corvus Omninet LAN. Implementations for other computer systems and other LANs are slated to become available later this year.

An intriguing, and somewhat lamentable, feature of the system is the Liaison Monitor, which allows the independent seller of the system to limit the number of simultaneous users. This is justified in SofTech's literature as a way for software developers to ensure profits by charging different prices for the same program, according to the number of users. While the goal of networking and communications is to increase productivity by making data and programs more widely available, profitability is generally the motivating force behind business. But this seems like a step backwards—the same thing can be accomplished cheaper with a single program on a single disk that will only run on a single machine (eg, VisiCalc on the Apple.)

While the UCSD p-System has a wealth of tools, a Pascal that cures most of the standard language deficiencies and a large, vocal, and active programmer community, it is by no means a standard or "universal" operating system. Standards are created by the general consensus of large numbers of vendors and users. Despite the fact that the majority of p-System users have bought it from Apple Computer Inc (Cupertino, Calif), and not SofTech, the latter shows a certain lack of interest or awareness that anyone else exists in the data processing world.

Technically expert users feel that Liaison is an excellent solution to networking between machines running the p-System. It addresses the needs of a multi-user system very well, providing for interchange of data and program source and object files, as well as the file-locking and password protection necessary to keep a multi-user system secure. It is modular, and provides services at all seven levels of the ISO interconnection model.

It does not, however, make direct provision for communication with other systems which are not running Liaison, whether they are non-Liaison p-Systems or others. Some of this lack can be charged to the vendor; but a greater percentage must be charged to the whole industry and user community worldwide, in delaying the implementation of clear interconnect standards and translation protocols.

—Sam Bassett, Field Editor

Window worlds open to independent programmers

The open applications environment and the desktop metaphor are common concepts among the newer 16-bit operating system user interfaces. Notable among these are the Lisa by Apple Computer, the Windows system by Microsoft, and VisiOn by VisiCorp. The desktop metaphor uses windows, icons, menus, and a mouse to select actions and is obviously meant to make the systems appealing to those who are not totally familiar with computers. The open application environment, however, has two purposes: to allow the user to select and run applications from different software vendors, and to encourage independent software vendors (ISVs) to write applications for the window environments.

To this end, Apple Computer (Cupertino, Calif), Microsoft (Bellevue, Wash), and VisiCorp (San Jose, Calif), have come up with ISV programming aids and support. They have also specifically designed their operating environments to make it easy to adapt independently produced applications programs to their computers. Such ISV support has appeared in the form of "tool kits" for adapting to the world of windows and as porting aids for adapting existing programs to the new environment.

Porting existing software from other systems can be done in two ways. In some cases, programs can be recompiled and adapted to a subset of the window environment. In other cases, an application must run in a window which simply emulates a standard alphanumeric terminal. The programmer may

(continued on page 54)

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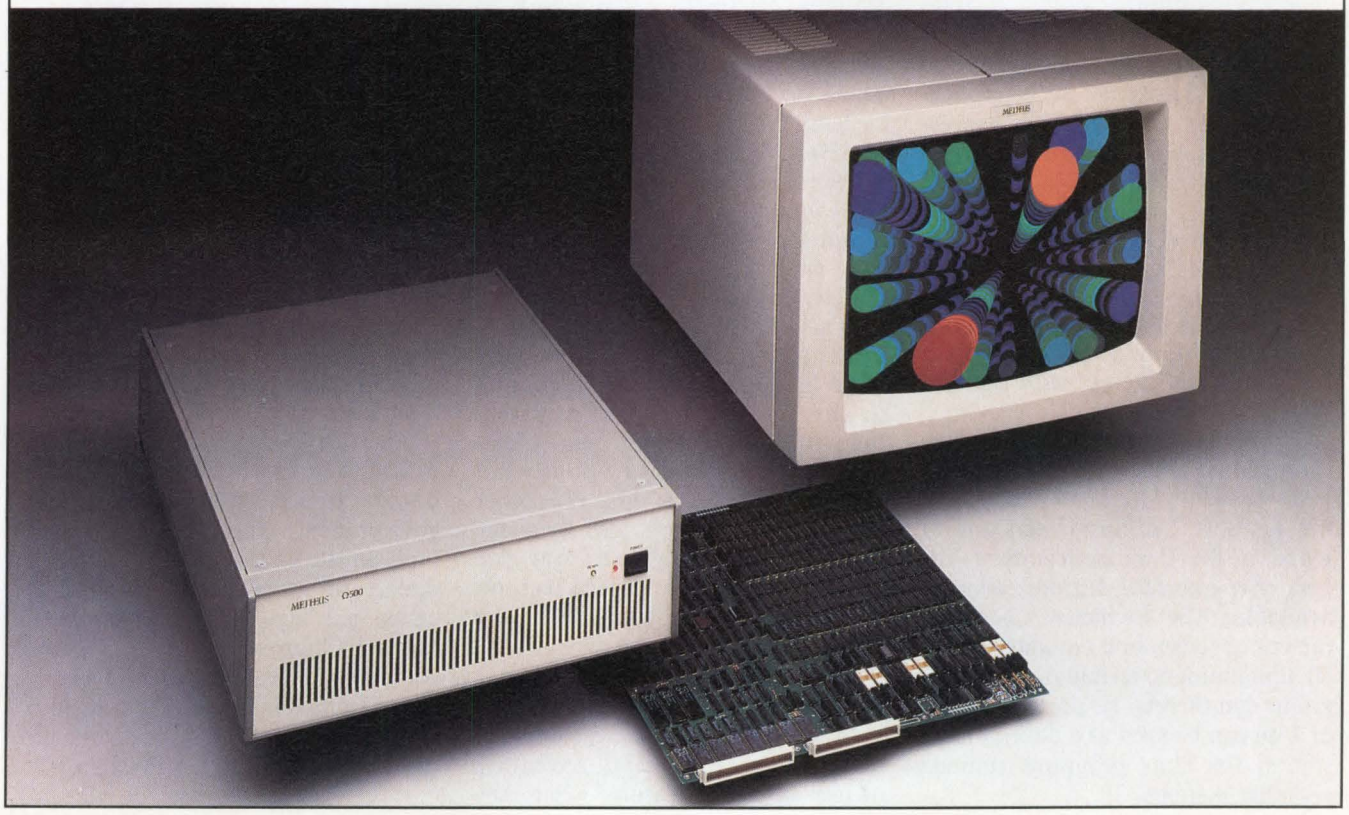

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Window worlds

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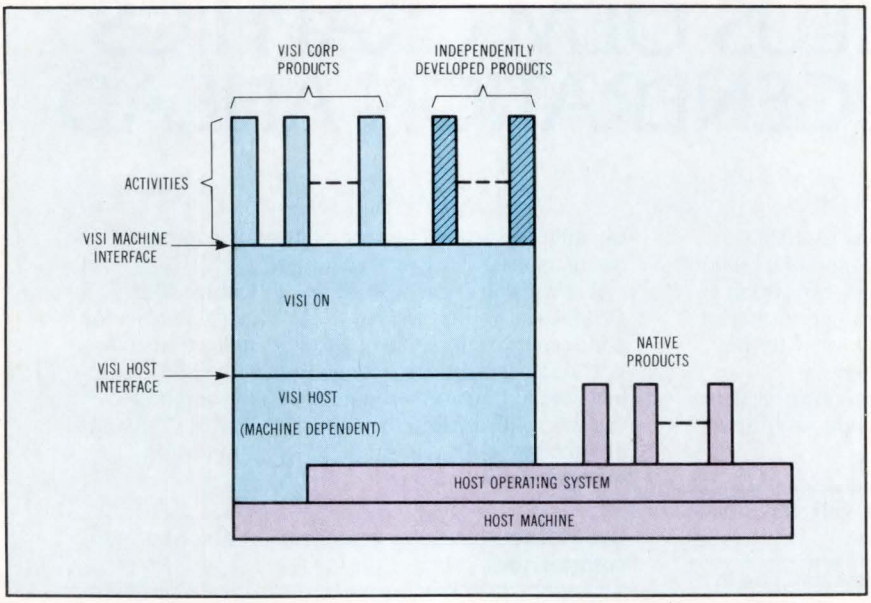

The machine-dependent interface, VisiHost, connects the VisiOn environment to the host operating system. Applications written by VisiCorp, as well as those by ISVs, run consistently in the VisiOn world sharing user interface and data.

later have the option of rewriting routines in the ported application to make it work more closely with the world of windows, but at least the existing software investment is preserved in the new environment.

The Apple Lisa system has a tool called QuickPort, which enables applications written in Basic-Plus, Cobol, or Pascal to be quickly moved to the Lisa Desktop. Such applications readily make use of complementing screen features. They will have their own menu, window, icon, and stationery pad, as well as be able to utilize Lisa's scrolling and printing interfaces. Thus, although the Lisa uses an object-oriented programming approach, nonobject-oriented programs can be written for it and can interact with the user in a Lisa-like manner.

For programs that have been developed in a Unix-only environment, Lisa runs the Microsoft Xenix and the UniSoft UniPlus+ versions of Unix. In the Unix environment, the Lisa user-interface features are not available. The "window" occupies the entire screen and emulates a 24 x 80 alphanumeric terminal. Unix programs can thereby be ported to Lisa, or Lisa can be used as a development station for Unix programs running on other systems.

One main difference exists between the Lisa world and the window systems offered by VisiCorp and Microsoft. Lisa is a hardware environment with its own operating system, while the latter two represent extensions to existing operating systems. Microsoft's Windows is an extension of its own MS-DOS operating system. Visicorp's VisiOn interfaces to other 16-bit operating systems via a machine-dependent VisiHost/operating system interface.

Microsoft does provide the ability for a window to emulate a VT-52 type terminal for straight alphanumeric I/O. But, applications that write directly to hardware, bypassing MS-DOS, will not run in a window. Here, in contrast to Lisa, the portability issue involves porting the program to the MS-DOS environment rather than to a hardware system. Unix-only programs would obviously not run under MS-DOS. On the other hand, Microsoft provides language bindings to six languages that give them access to the standard features of Windows when compiled under MS-DOS.

Program development

In all three approaches, applications are able to take full advantage of user-interface features when they are written specifically for that environment, and all three companies provide tools for the ISV to do that. Each of the three, however, has a somewhat different focus. Apple is primarily a hardware manufacturer with its own operating system. Microsoft has concentrated primarily on the MS-DOS operating system running on a wide variety of machines. VisiCorp has focused mainly on consistent application software tht run in a number of operating systems. The three companies are also aware that they cannot service the full demand for applications, and hence the importance of the ISV.

Apple provides a development environment called the Workshop that consists of a Lisa machine, the ToolKit/32 package, which includes the Generic Application, QuickDraw graphics, and an object-oriented extension of Pascal called Clascal. The Generic Application can start software development using all of Lisa's standard user-interface features, including cut/paste integration, scrolling, menu handling, and window management. Since applications are built using ToolKit/32, all programs written with it will have a consistent user interface.

Programming with Clascal on the Workshop takes an object-oriented approach where the user describes characteristics and interactions of objects, such as windows, which comprise the application. The Generic Application contains a library of object descriptions (windows, documents, commands, etc). The developer has only to describe the objects needed to make up a specific application and the characteristics that might make a given object distinct. Syntax is very close to that of Pascal.

VisiCorp's approach with VisiOn is first to interface the VisiOn environment to a given operating system environment. Applications are then built on top of VisiOn using VisiC, a dialect of the C language, and C extensions (eg, the menu compiler, the help compiler, and the forms compiler) to create the user interface. These compilers turn C-like code into the menus and screens that make up the window interface of VisiOn.

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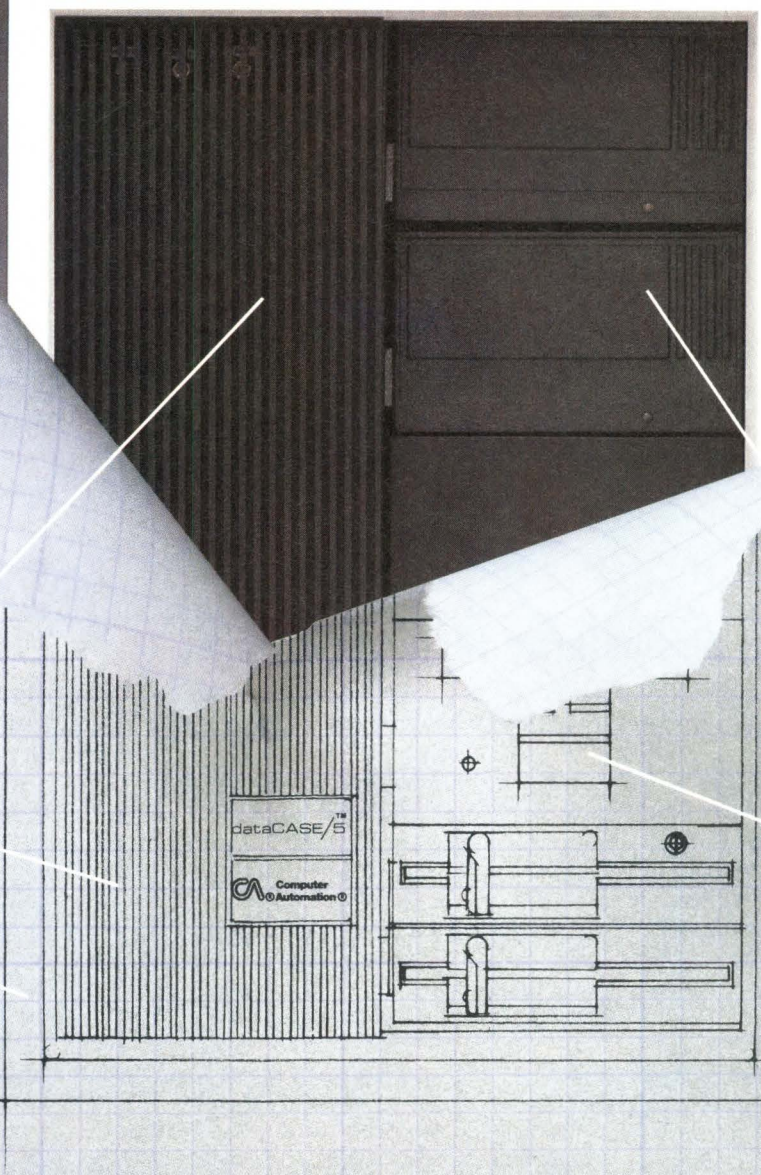

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Window worlds

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With these tools, the program developer can create a standard interface between the user and all products that run under VisiOn. The interface, called Basic Interaction Techniques (BITS), includes a mouse input, forms input, and multimedia (combined mouse and text) input. Interaction with devices is via VisiOps which provides high level services between the C program and the VisiHost/ operating system interface. VisiCorp provides its ISV toolkit in the form of packages that run in the Digital Equipment VAX Unix environment or on a 68000-based Unix system.

In the world of Microsoft Windows, the system takes responsibility for screen management, data exchange, and device independence. There is an icon editor to allow the ISV to create unique icons for the application which are then displayed as available in the windows display.

For communicating with external devices, primarily bit-mapped displays or other output devices, the programmer can write in terms of a graphics device interface (GDI) which provides primitives for an "abstract device." Hardware OEMs will assume responsibility for providing physical device drivers that interface to the GDI on systems running windows. Thus, any program written for Windows will run on the devices supported by any system running Windows.

Microsoft has also provided a way for programs from different vendors—written using the ISV toolkit—to exchange data. Applications from Microsoft itself will use the Symbolic Link (SYLK) data interchange protocol. However, the toolkit also allows data to be passed between applications in uninterpreted binary or in ASCII form. Programs would have to find and agree on a protocol before they could share data.

One effect of the open application trend may be the emergence of a standard for the human interface. By not witholding interface tools from ISVs, the major companies are not only encouraging vendors to write software for their systems, but are also encouraging the use of ready-made tools. These tools will provide users with a familiar way to interact with the new generation of applications.

—Tom Williams,
West Coast Managing Editor

INTEGRATED CIRCUITS

Chip finds degree of similarity between strings

Adaptive pattern recognition techniques have to date been mostly software systems that try to deal with information based on inexact, inaccurate, or incomplete data. One of the main problems has been determining the degree of similarity between strings. That function—computing similarity—has now been placed on a silicon chip called the PF474 microcircuit by Proximity Devices Corp.

The Proximity Filter PF474 performs extremely fast serial string comparisons and computes a degree of similarity for each. This comparison is expressed as a 32-bit binary fraction. Two totally dissimilar strings will yield a zero, while two exactly matching strings will produce a one. In computing the degree of similarity, the PF474 uses a set of parameters that are stored in onchip RAM. The 16 best matches are then stored in the ranker section of the chip, which also contains flags to locate the 16 next best matches, and so on. The Proximity computer section and the ranker operate in a pipelined mode so that neither need slow down the other in order to complete an operation.

Software comparison algorithms have yielded computation times that are proportional to the square of the number of characters in the string. With the PF474, however, the comparison time is linear with the length of the string, provided data is supplied at the chip's full input rate. This can be quite fast, since the PF474 is mapped into memory address space and has a DMA capability of up to 2 Mbytes/s. Thus, 8-character (byte) strings can be compared at a rate of 49,600 comparisons/s, while 127-byte strings run at 3870 comparisons/s.

The PF474 normally operates by taking a query string, for which parameters of similarity have been loaded into its parameter RAM, and rapidly searching through a long list of comparison strings in a data base. It is thereby possible to perform an exhaustive search in an acceptable amount of time without having to limit the search space and risk missing some similar strings.

To the system, the PF474 looks like a 1024-byte address range that is partitioned into four 256-byte sections: control, parameter, string, and ranker. The chip also contains the special purpose Proximity computer core which calculates the comparisons. The string section is further divided into two 128-byte sections to hold the query string and the string currently being compared to it. Since a string must be terminated by a null character, strings of up to 127 bytes in length can be processed.

The Proximity computer uses the 256 values stored in the parameter RAM section to compute the similarity. The fact that the parameters are stored in RAM means that they can be set and altered by the user, or even dynamically by a running program. This is quite important because the same kinds of parameters that work for English might not work as well for French or proper names, and a signal-processing application might require different parameters altogether. The three

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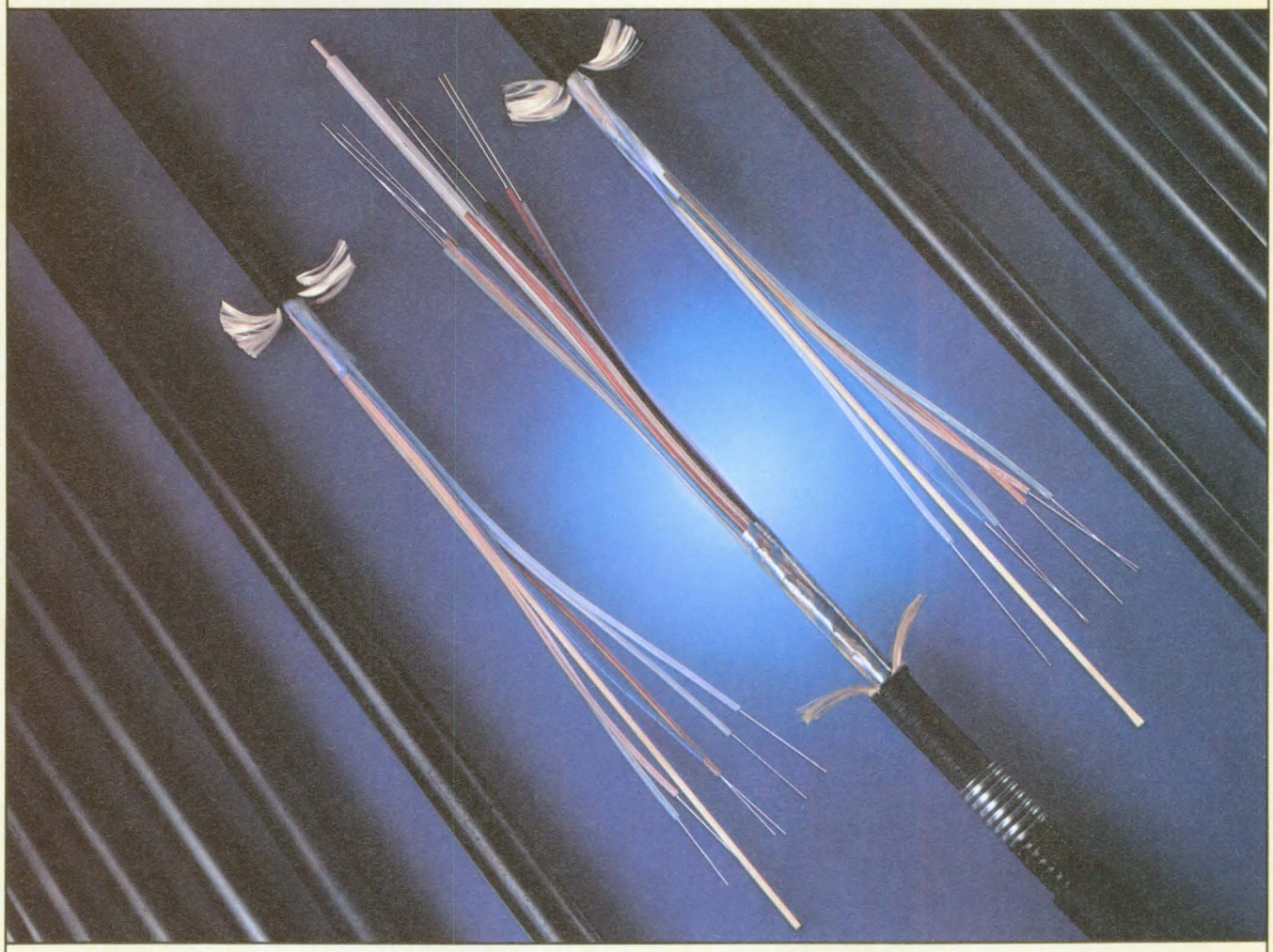
STRAIGHT.....



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CIRCLE 28

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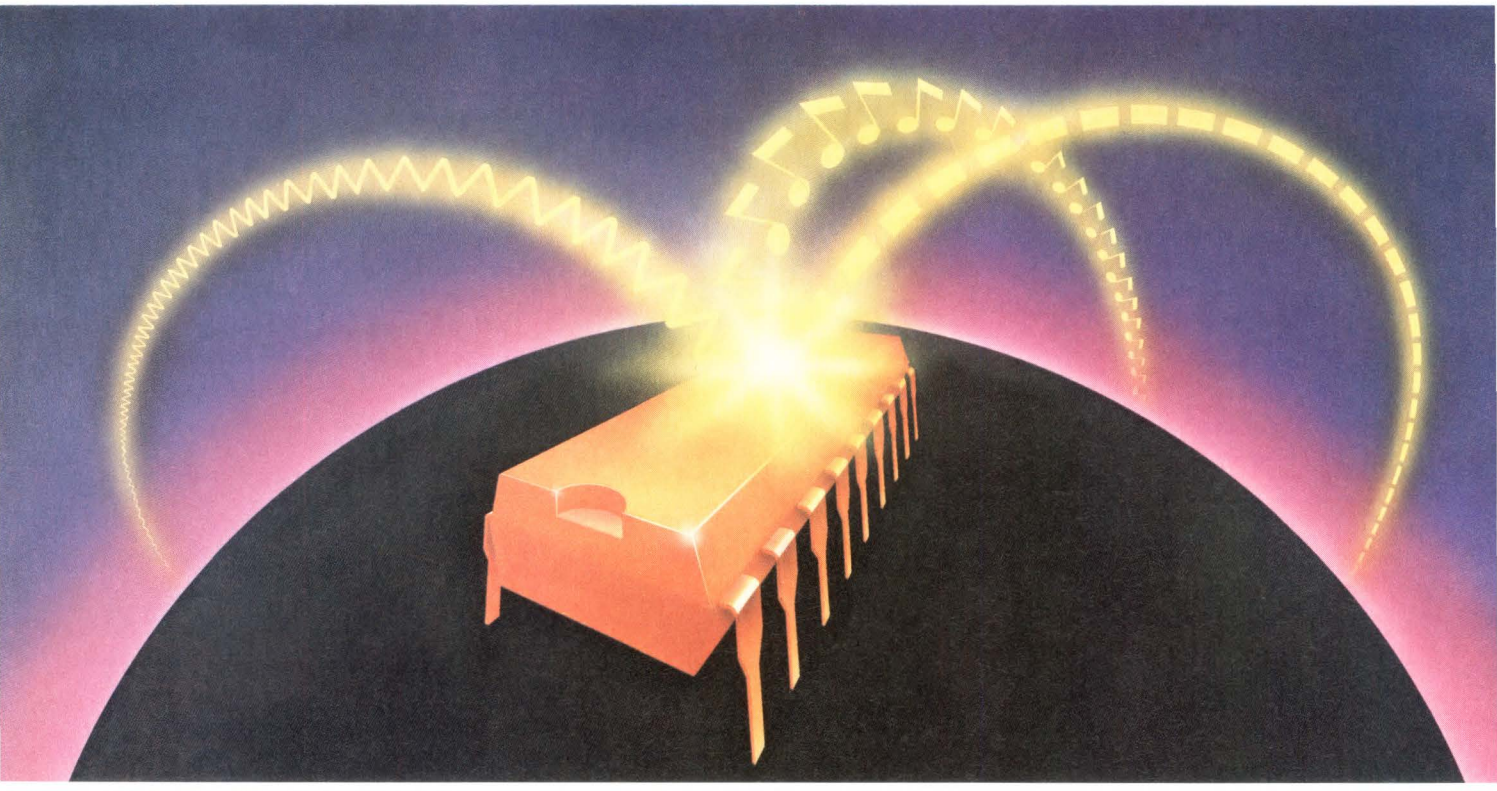

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INNOVATORS IN INTEGRATION

CIRCLE 183

Chip compares strings

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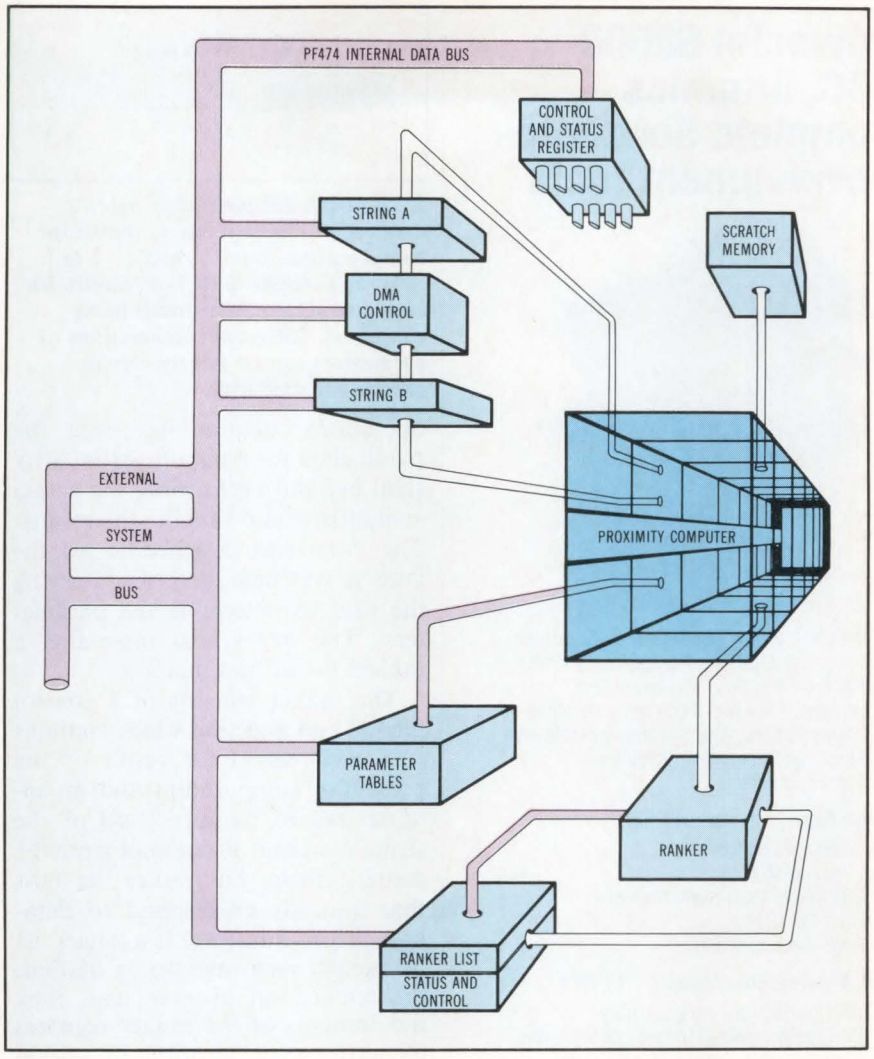

In the PF474 architecture, four major blocks, string space, control, parameter tables, and ranker, appear to the system as memory address ranges and can be directly addressed. The Proximity computer generates 32-bit binary fractions that are used by the ranker to establish the list of 16 best matches.

parameters stored in each byte are weight, compensation, and bias.

Weight is a direct reflection of the importance of a character in the string, and can vary in value from 0 to 7 (3 bits). For example, in comparing English words, less weight would be assigned to vowels than to consonants and different consonants might have different weights according to the similarity or difference of the sounds they make. A weight of 0 would be almost ignored, but it would affect the similarity since it occupies a position in the string.

The bias parameter tells if a character is more important near the beginning or near the end of the string. Bias can range from a value of -2 to $+1$. For instance, if all characters had a negative bias, the computer would assign more importance to similarity near the beginning of the word than near the end.

Compensation considers the dissimilarity between two characters and whether a word contains a given character or not, or whether a given character is in the same position in both words. The compensation value of unmatched characters is cumulative in a comparison. Setting a high compensation parameter will make the comparison more tolerant of dropped characters.

This type of pattern recognition therefore necessitates two main

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Chip compares strings

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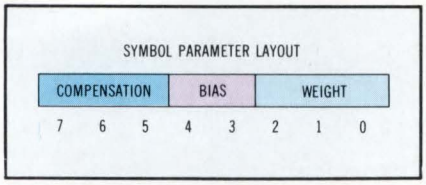

Each of the 256 parameter bytes is divided into three fields as shown for compensation (0 to 7), bias (−2 to +1), and weight (0 to 7) attributes for each character in the strings being compared. Different combinations of parameters can set widely varying criteria for similarity.

operations: determining what the parameters for computing similarity shall be; and performing the actual comparison and ranking the results. The PF474 was designed to do the latter at very high speed while leaving the user to determine the parameters. The PF474 also maintains a ranked list of best matches.

The ranker consists of a control section and a section which contains (for each entry) the result of the proximity computation and an internal record number (IRN) of the string matched. It does not store the actual strings, but rather the IRNs that typically correspond to database record numbers. If a longer list of ranked near-matches is desired, the application program can copy the contents of the ranker registers to some other location in system memory and keep track of the order of such lists.

Where it lends a hand

An example of the kinds of applications to which the PF474 can lend itself is the Savvy system by Excalibur Technologies. Savvy is an adaptive pattern recognition software system which is available integrated into a database management and automatic program generator for use with Apple and IBM personal computers. To facilitate natural language input and programs that "learn" based on patterns of interaction with users, Savvy incorporates pattern recognition using routines encoded in ROM.

For a given input string, Savvy has routines that discover the parameters which determine the degree of similarity. It then performs the type of string comparison described for the PF474. A spokesperson for Excalibur noted that the string comparison and proximity computation portion of the Savvy system could be vastly accelerated by using a chip such as the PF474.

Another very promising application area is in speech recognition. Here, the system simply analyzes time slices of speech that have been broken into characteristic spectra. There is no need for the pattern processor to pay attention to syntax at this level; meaning would emerge as patterns of patterns of patterns, etc. In experiments performed by Excalibur, it has already been possible to transmit intelligible speech at rates between 200 and 400 baud.

Speech in these experiments had been broken into 40-ms time slices, then transformed into patterns of 16 frequency bands with characteristic relative strengths for each frequency. Such spectra constituted patterns that could be characterized and compared. Excalibur recorded roughly 1000 distinct patterns which emerged from many hours of speech from different speakers.

Speech transmission could take place at such low data rates because what was actually being transmitted was not speech, but rather the references to various patterns which were reassembled and turned back into analog signals at the other end. The use of such methods for speech encryption—encoding the references—is but another extension of the technique. Proximity Devices has already mentioned the possibility of PF474 arrays or similar processors attacking large data arrays. It seems certain that the potential opened up by the silicon implementation of rapid string search and comparison is only beginning to dawn on designers. **Proximity Devices Corp,** 3511 NE 22nd Ave, Fort Lauderdale, FL 33308; **Excalibur Technologies,** 800 Rio Grande Blvd NW, 21 Mercado Plaza, Albuquerque, NM 87104.

—Tom Williams,
West Coast Managing Editor

Circle 240

SYSTEM TECHNOLOGY

(continued on page 64

CONFIDENCE BUILDERS

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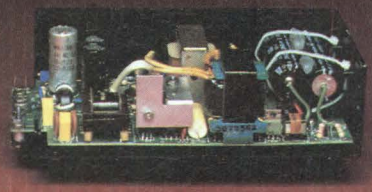

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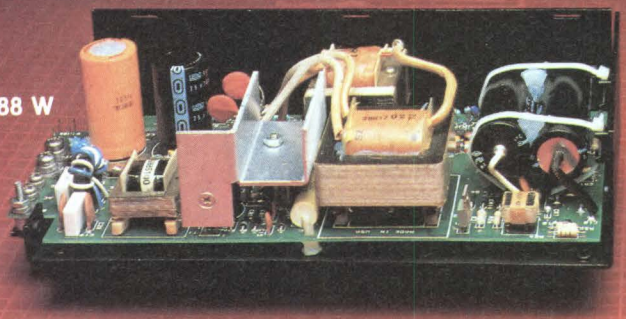

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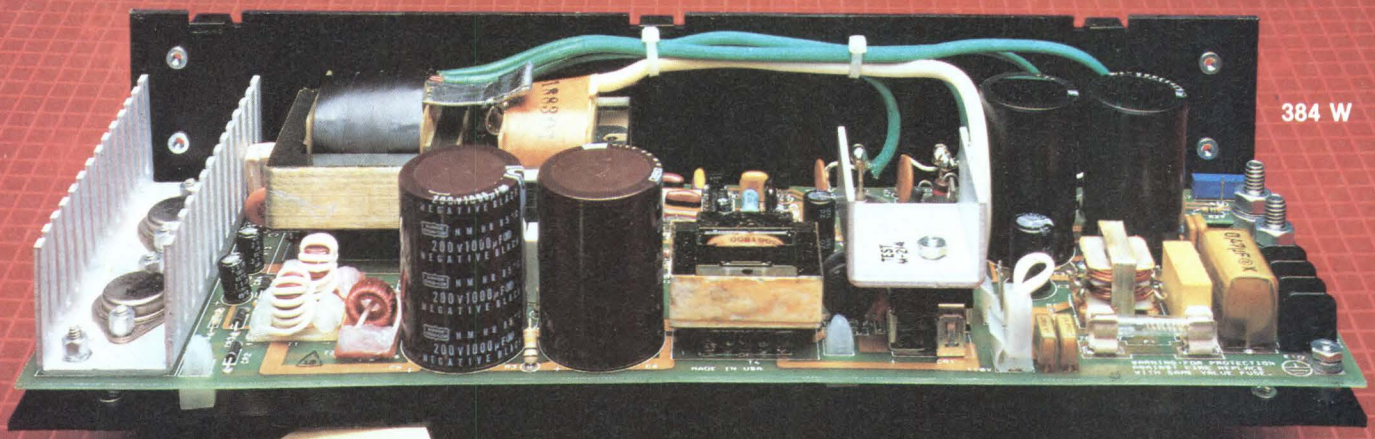

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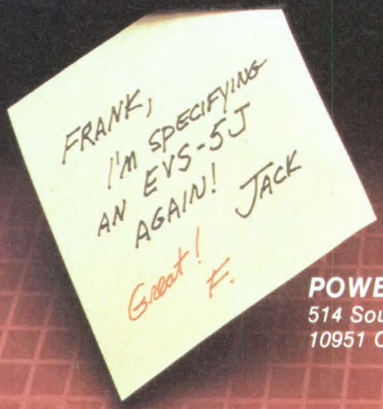

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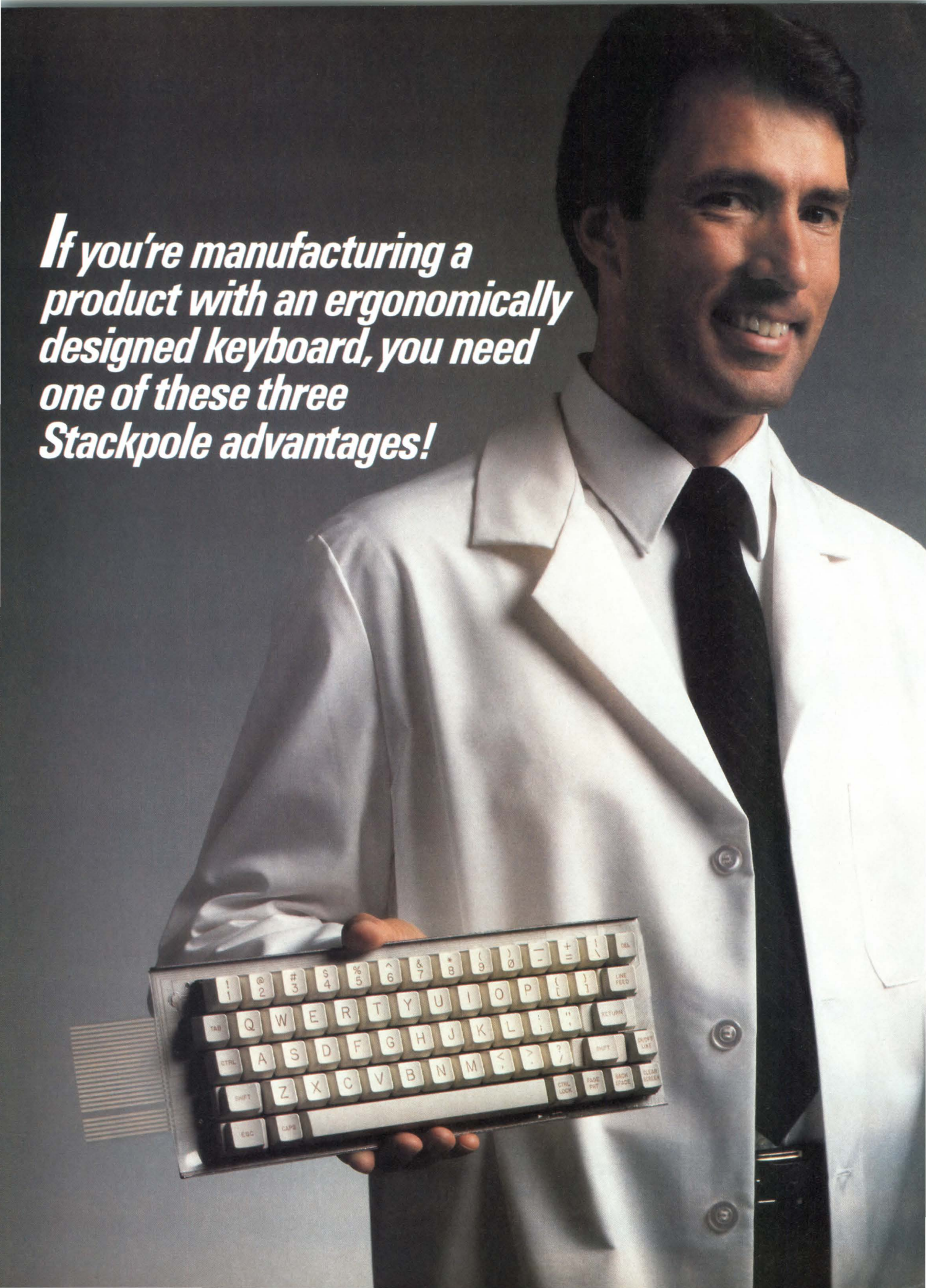
CIRCLE 31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The KS-500E shows just how good a membrane keyboard can be. Full travel. Ergonomically designed to the latest DIN requirements. Engineered into a monolithic housing that eliminates keyswitch alignment problems. It has a lot in common with its cousin – the KS-200E.

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CIRCLE 32

Terminals move to X.25 transparent to host

Local and remote terminal users move freely between Digital Equipment's VAX-11 computers and packet-switched networks with a frontend communication processor from Advanced Computer Communications. The IF-11/X.25 Plus handles any necessary packet assembly and disassembly (PAD) called for in the X.25 specification, as well as necessary terminal protocols, without host intervention. The host services each terminal in a normal time-sharing fashion, regardless of where it is physically located.

Such transparency results from the ability to emulate a terminal multiplexer, such as the DH-11. Few modifications to existing software drivers are needed. Furthermore, the host computer cannot distinguish between attached and remote terminals. The controller hides its ability to operate in one of two modes: access by remote terminals only, or in access by attached and remote terminals.

Remote terminal access is the most straightforward of the two modes, since the 32 data ports dedicated on the host computer handle just incoming calls. Local terminals require additional hardware support since they can initiate X.25 conversations as well as converse with the host system. As a result, the IF-11/X.25 Plus allocates one of the 32 channels for each attached terminal, with the remaining channels free to support remote terminals.

Under either hardware configuration, remote users initiate a terminal session by placing a call to the desired network node. Packet switched networks typically use dialup lines for these incoming calls, with RS-232 serial communications used as the physical link. Implementation of the high level data link (HDLC) protocol at the transport layer (ISO layer 2) ensures error-free data transmission. Messages are transmitted across the network at 56 kbits/s. Incoming calls can either choose a specific port address (1 to 32) or allow the controller to assign the lowest port address available.

In addition to routing incoming calls to the appropriate port address, the controller handles PAD functions. The data link established at layer 2 is divided into 32 logical channels. These channels identify individual user conversations that have been combined for transmission over a single trunk line in the packet network.

Packets also contain session and presentation-dependent information such as baud rate and terminal characteristics (ISO layers 5 and 6) enabling the user to communicate effectively with the remote host. Moreover, the IF-11/X.25 Plus translates these parameters (which are set forth in the X.3 and X.28 specifications) into specific terminal protocols (eg, VT100). If necessary, users can reconfigure a remote network node with parameters defined in the X.29 specification.

Besides handling incoming calls, the IF-11/X.25 Plus also provides a means for local users to send packets to remote network nodes. Terminal line expansion boards link as many as 32 users (in groups of eight) to the controller, although the host computer cannot tell the difference. All ASCII terminal functions are available to each user. In fact, terminal communications can occur at a rate as fast as 9600 bits/s.

Only when the user enters a special character sequence does the controller come into play. The user, in effect, disconnects from the host and further terminal communications are routed to the controller for action. Special PAD commands are then used to connect an X.25 data network, as well as to move back to local mode for further interaction with the host computer. Users need not log off the host system at all to enter the PAD mode.

The IF-11/X.25 Plus occupies a double hex-width Unibus slot on any PDP-11 or VAX-11 minicomputer running RSX-11, VMS, or Unix operating systems. The device driver is included in the $9000 single-unit price; each optional terminal expansion board is priced at $3000. **Advanced Computer Communications,** 720 Santa Barbara St, Santa Barbara, CA, 93101.

Circle 241

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CIRCLE 34

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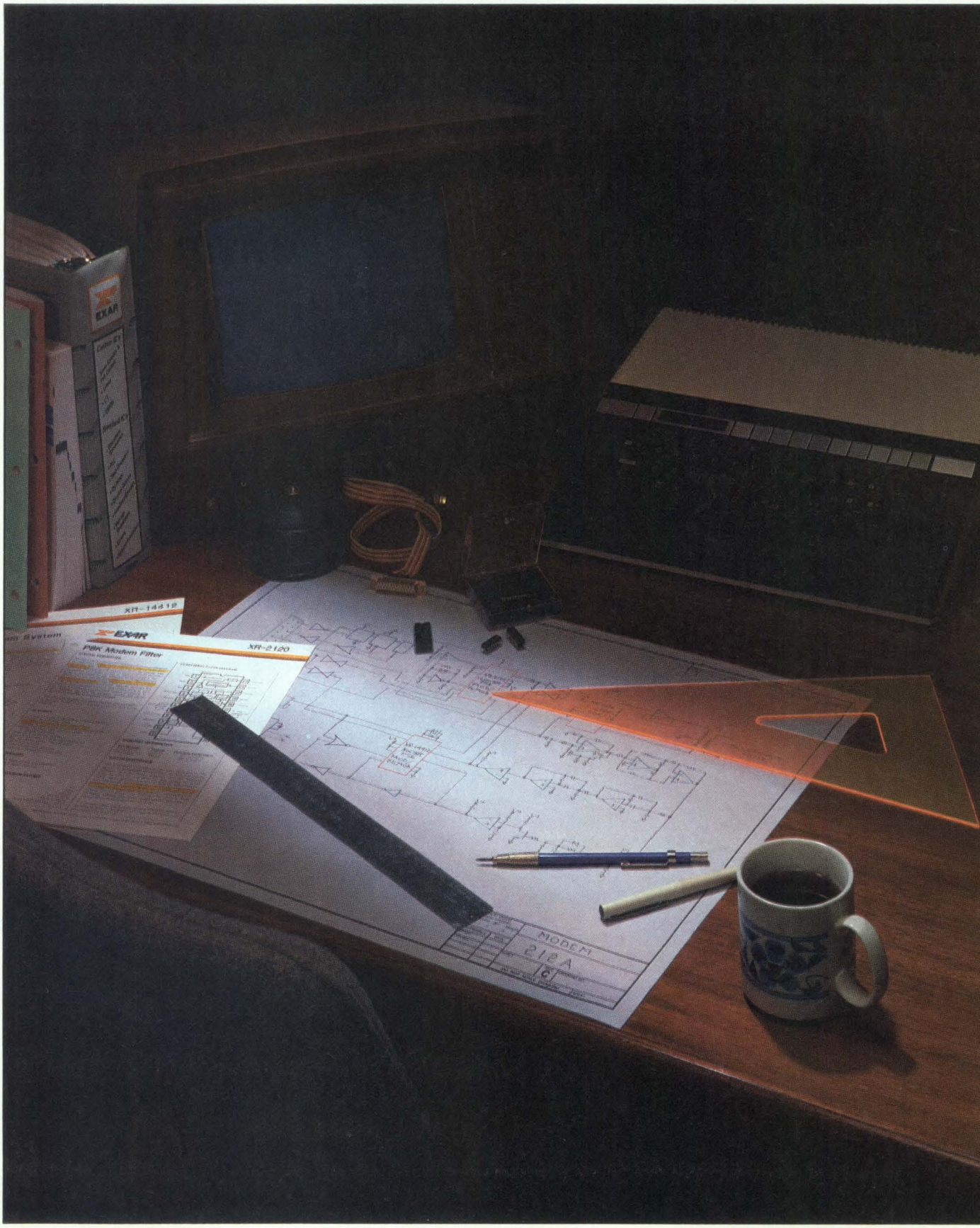

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But, Exar does not stop there. In order to implement these devices into a compatible Bell 212A modem, we have devised a simple and cost effective trouble-free way to evaluate them in a system. Exar can provide you with a modem evaluation kit including these three devices, along with all the necessary supporting components, PC board, schematic and operating instructions to minimize your design task.

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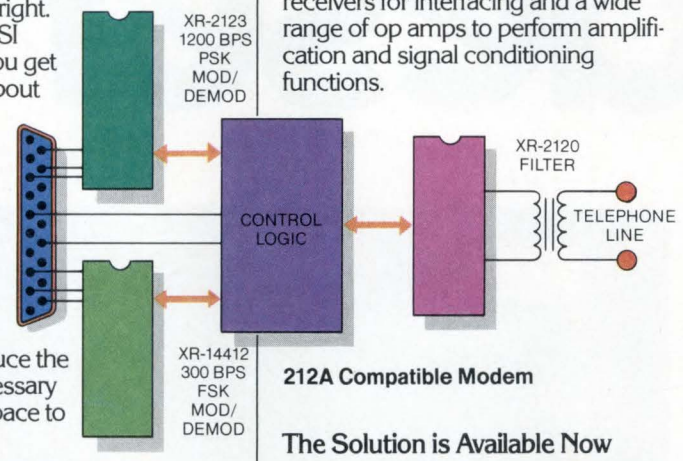

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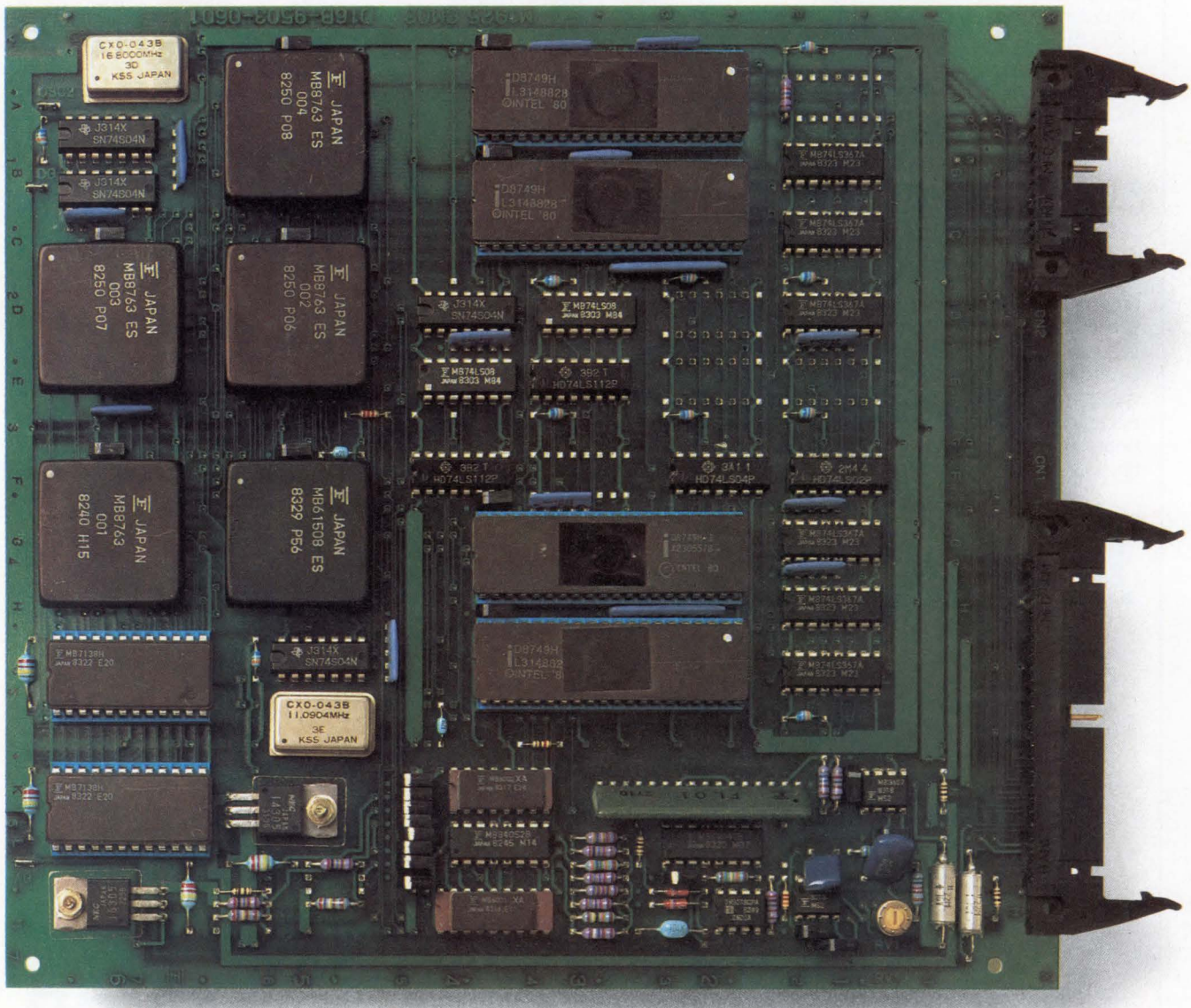

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CIRCLE 36

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CIRCLE 37

We can't keep it quiet any longer!

Occam is the language for today's microprocessors

Today's microprocessor systems are growing up. New boundaries in performance and functionality are being called for and met.

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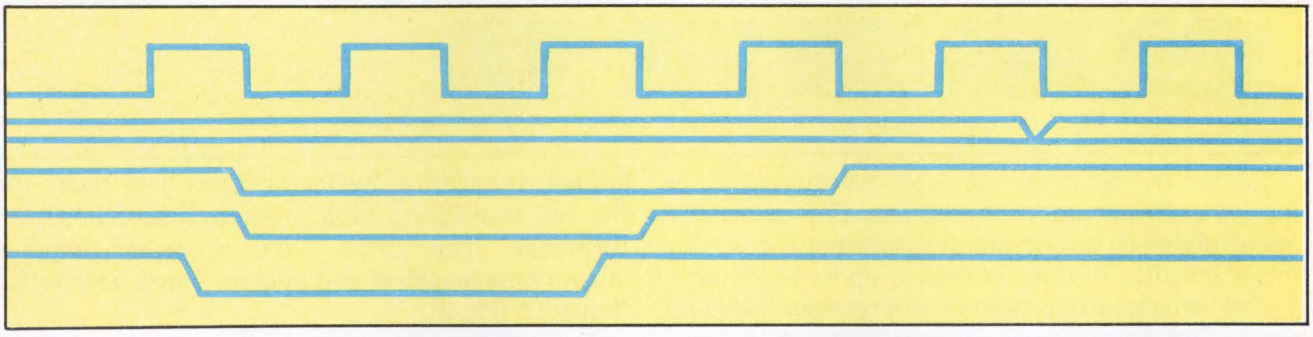
CIRCLE 38

TRIPLE-BUS ARCHITECTURE GAINS SPEED, VERSATILITY

Both problems and opportunities lurk for designers of realtime minicomputer systems. A three-pronged approach attacks the problems inherent to single-bus architectures.



by Dave Cane and Steve Mullen

In traditional minicomputer architecture, a single high speed internal bus transfers digital data throughout the system. However, the problems inherent to this design can be overcome with an alternative, multiple-bus architecture. Using multiple industry standard processors with multiple industry standard buses, the MC-500's 32-bit architecture distributes data acquisition, computation, and graphics tasks among several very high performance processors.

The main system CPU uses a proprietary bus to connect the VLSI processors to system memory. A high performance Intel Multibus (IEEE 796) supports a data acquisition and control processor (DA/CP), up to four independent graphics processors (IGPs), and system peripherals. An enhanced STD bus—controlled by the DA/CP module—provides efficient data acquisition and control.

This triple-bus design, the core of the system architecture (Fig 1), provides a flexible structure that anticipates future system enhancements with technological advances in microprocessors, memory, mass storage peripherals, communication devices, and realtime interfaces.

Cumulative bandwidth in triple-bus structure

Since the primary design goal was to provide a one million sample/s analog acquisition rate, the bus that supports the A-D converter—the STD bus—must operate at 2 Mbytes/s. Operating at this speed, however, requires a 4-Mbyte/s transfer rate since the Multibus needs twice the bandwidth of the STD bus. This is necessary because, in analog throughput-to-disk applications, data must travel over the Multibus twice.

At first glance, it appears that the Multibus bandwidth will allow this rate. If a bus runs near capacity, however, bus latency problems may surface. Long latencies slow data transfer and generally make data acquisition/control performance highly unpredictable. Since the Multibus must also carry data traffic from system peripherals during data acquisition, it is loaded at 80 percent capacity. Thus, the Multibus transfer rate was designed at 6 Mbytes/s.

Dave Cane is a hardware development manager at Masscomp, 543 Great Rd, Littleton, MA 01460, where he is responsible for hardware design. He holds an MSEE and a BSEE from the Massachusetts Institute of Technology, Cambridge, Mass.

Steve Mullen is an end user marketing manager at Masscomp. He holds a BA from Lawrence University and a PhD from the University of Minnesota.

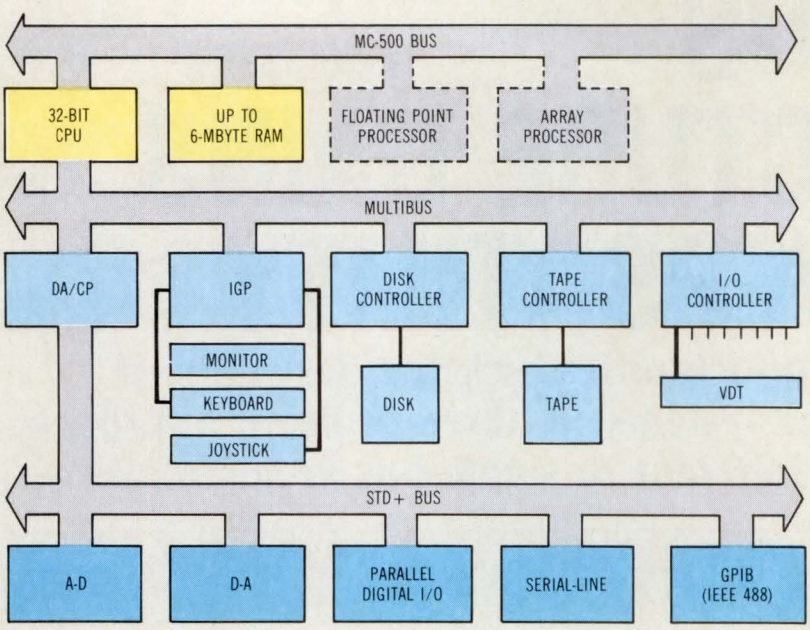


Fig 1 The MC-500's triple-bus structure connects CPU to memory through a proprietary bus operating at 8 Mbytes/s. It uses a Multibus for I/O and handles data acquisition through an enhanced STD bus.

Primarily, the proprietary MC-500 bus serves as the CPU to memory connection. To allow the Motorola 68000 to operate at maximum speed, this bus is specified to transfer data at up to 8 Mbytes/s.

One 68010 and one 68000 microprocessor make up the MC-500 VLSI virtual memory CPU. A 4-Kbyte instruction and data cache are used to raise the microprocessors' speed. Memory management control supports up to 16 Mbytes of virtual memory space in a demand-page format.

Memory is mapped in 4-Kbyte pages. A 4096-entry address translation table maps virtual to physical addresses. A 1024-entry RAM-based address translation buffer operates as a cache for the full translation table, thereby improving performance. The CPU's 68000 processor handles memory management and address translation buffer "misses" (Fig 2).

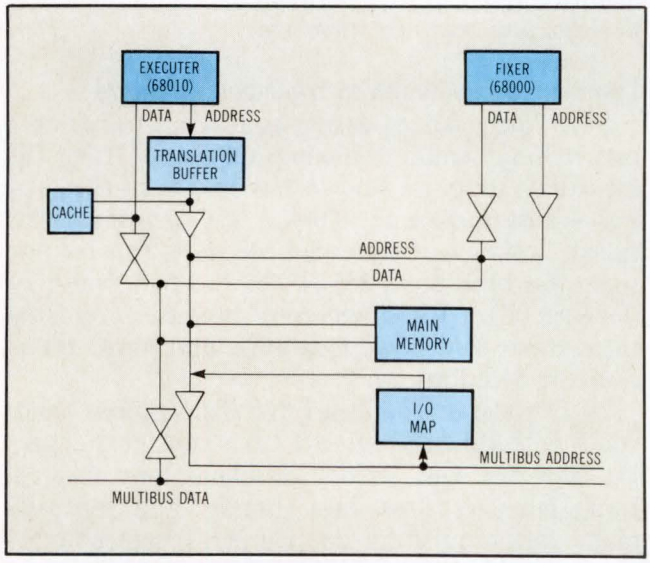


Fig 2 A 68010 (executer) and a 68000 (fixer) make up the system CPU. Speed is gained using a 4-Kbyte instruction/data cache between the main processor and memory, and by using the 68000 to handle memory management.

The MC-500 bus connects the CPU to physical memory (storage capacity ranges from 0.5 to 6 Mbytes). The fastest bus in the system, it transfers blocks of data at up to 8 Mbytes/s. It also supports the optional Masscomp floating point and array processors.

Providing the CPU with a dedicated high speed bus avoids the time that would be lost on CPU/Multibus access arbitration if memory were placed on the Multibus. In addition, the 68000 processor uses an unusual handshake process—it notifies a bus that it will strobe data a full cycle before actually transferring that data. The Multibus protocol, however, is designed to move data almost simultaneously upon request. This causes the bus (as well as the processor) to be idle while it waits. The triple-bus design eliminates this bus wait state.

Finally, the system design is most effective when multiple main CPUs are integrated into a system. Rather than a multiple CPU architecture where the CPUs must share multiport memory access, each CPU has its own physical memory connected by an MC-500 bus (Fig 3).

CPU/Multibus connection

Using the industry standard Multibus (IEEE 796) allows the peripheral controllers, the data communication devices, and the data acquisition interfaces that exist for this bus to be attached to the system. Connected to the MC-500 bus through a Multibus adapter, the Multibus supports a DA/CP;

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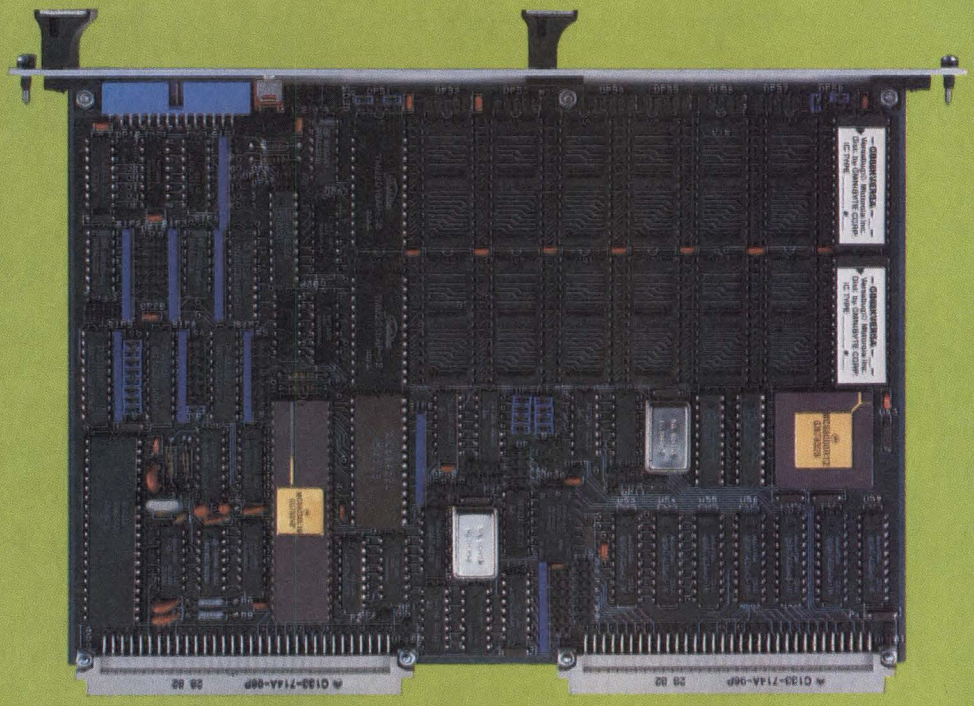

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- ★ Powerful 12.5MHz 68000R12 16/32 Bit CPU
- ★ 8 pairs of 28 pin sockets for ROM/RAM.
  -ROM 2732, 2764, 27128 or 27256 (Maximum of 7-pairs may be used, at least one pair required).
  -RAM 2K × 8 or 8K × 8 static (Maximum of 7-pairs may be used, at least one pair required).
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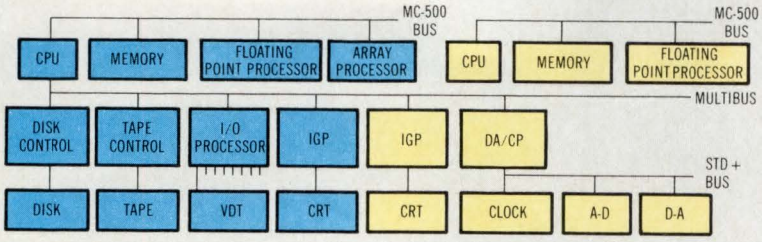


Fig 3 Designed for efficient operation incorporating multiple processors, the MC-500 provides each processor with its own physical memory and proprietary bus.

as many as four IGPs, each incorporating a 68000 processor; multiple disk and tape drives; terminals; printers; plotters; and network communication via RS-232 and Ethernet. The Multibus adapter enables 32-bit block transfers, providing a bus bandwidth of up to 6 Mbytes/s.

Historically, the Multibus evolved from a 1-Mbyte, 20-bit address version to a 16-Mbyte, 24-bit address configuration. Putting both types of boards on a system creates a DMA address problem. A second DMA problem results because peripheral memory buffers are not continuous for virtual memory systems. Therefore, DMA controllers cannot handle transfers that cross page boundaries.

To solve these problems, the design incorporates an I/O map in the CPU/Multibus adapter. A 1024-entry RAM, the I/O map converts the logical address from a DMA memory reference to the appropriate physical address. The operating system sets up this map before initiating the mass storage transfer. Once set up, contiguous addresses produced by a peripheral are mapped to noncontiguous physical pages.

A private line added in the Multibus P2 connector causes the I/O map to be bypassed when asserted; ordinary Multibus devices do not assert this line. When one CPU uses the Multibus to communicate to another CPU's memory, mapping is not necessary because the first CPU has already performed a virtual-to-physical translation.

A Multibus protocol defines a busy line, a set of address lines, and a strobe line. The bus also specifies address setup time and address hold time, as well as XACK (slave acknowledges on a read that it put data on the bus, and that it has removed data from the bus on a write). This Multibus protocol carries addresses made on bracket strobes, giving devices time to decode their own assert and deassert addresses. The 68000 has a similar protocol.

Unfortunately, comparing the 68000 timing specification to the Multibus timing specification shows that available address time for the 68000 after completion of its address strobe is not long enough to match the Multibus signal timing pattern. Therefore, to guarantee that 68000 strobes meet the Multibus setup for proper access, system designers have provided an address latch on that patch when the 68000 is bus master performing a read/write over the Multibus.

Finally, designers had to address the deadlock problem in the CPU/Multibus interconnection (ie, the CPU has to request and obtain Multibus time for a reference to memory). This eliminates the benefits of the high speed MC-500 bus. If, however,

When one CPU uses the Multibus to communicate to another CPU's memory, mapping is unnecessary.

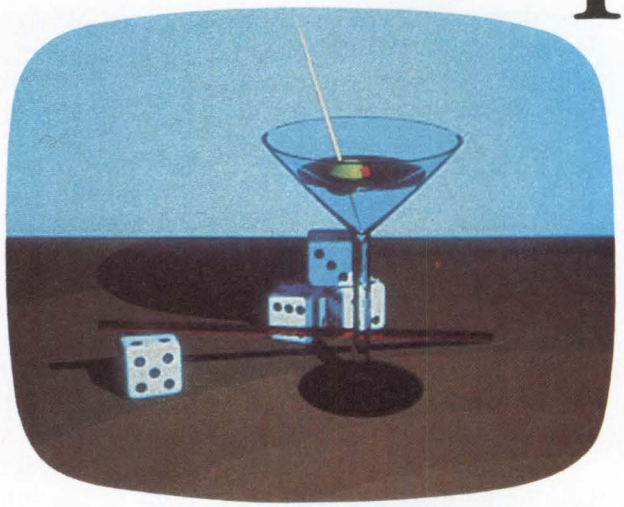
the CPU references a location that is not in local memory, the request must be made on the Multibus. If, at the same time, a peripheral also requests and wins the Multibus, a stalemate exists. The peripheral will not give up the Multibus until it receives its handshake from memory. To obtain that handshake, it must use the MC-500 bus to access memory.

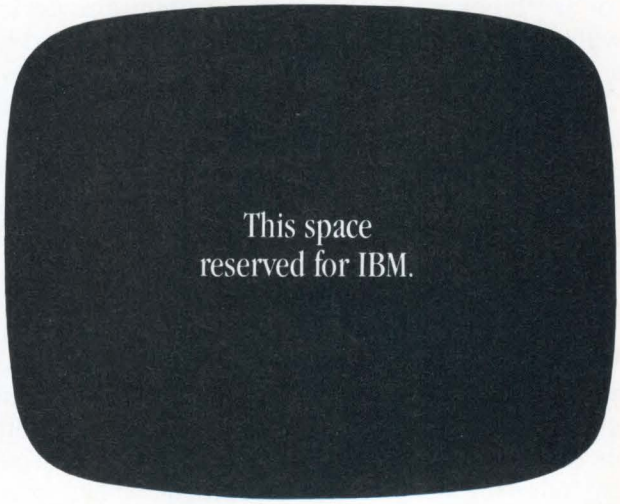
Although the CPU could hold the high speed bus while waiting to obtain the Multibus, this condition is avoided by logic, external to the 68010. This causes the CPU to temporarily withdraw its request. The peripheral can then enter its memory cycle to transfer data. Once the transfer is complete, the Multibus is free for access by the CPU. Using external logic rather than the deadlock avoidance mechanism built into the 68010, allows the 68010's full instruction set to be used. Using the 68010's deadlock function makes a critical 68010 instruction (the test and set instruction) unavailable in this case, because it does not function appropriately when the chip itself breaks a deadlock.

Multibus block transfer mode

The 32-bit block transfer mode on the Multibus follows the MC-500 high speed bus protocol. Midcycle, the master flips address line A1 to command the other half of the longword. In a read, the slave senses the A1 flip and switches its data to the other word within the long-word. In a write, the master changes A1 and the write data simultaneously.

We were going to compare Vectrix graphics to IBM's. Unfortunately, there is no comparison.





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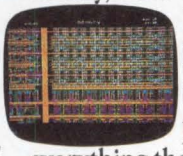

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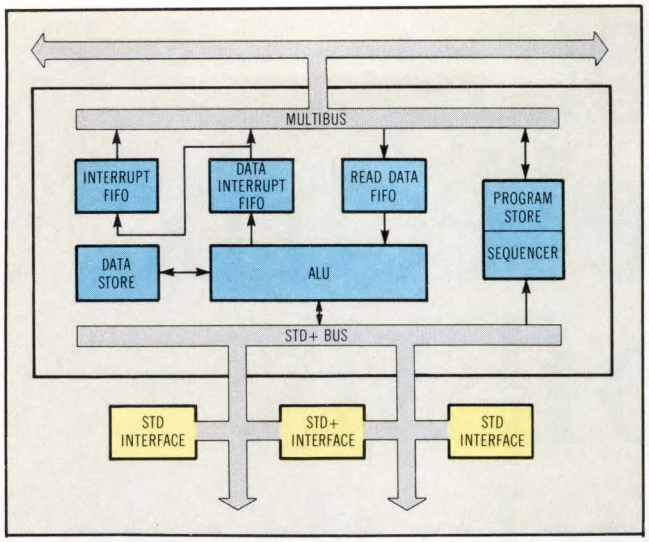

Fig 4 The DA/CP provides connection between the Multibus and a standard bus via an 8-MIPS bipolar bit-slice processor. Passing time-critical data to the Multibus through FIFOs isolates the processor from DMA latencies.

Sensing the A1 change, the slave obtains the data and does the write.

To differentiate this special mode, the design designates another unused line from the P2 connector as "block mode." An ordinary Multibus device will not select this mode; however, it can be used by a special device such as the DA/CP.

As part of its definition, the Multibus's protocol has a clock edge. While bus exchanges (arbitration determining bus master) happen on clock edges, the clock edge becomes irrelevant during address strobes, XACK, and data transfers, which are just asynchronous handshakes.

In block mode, the clock again becomes relevant. The slave must assert XACK on the clock edge. When the master flips A1, it must be on the clock edge, and when the slave swaps the data, it again must be on the clock edge. This reduces the time involved (and wasted) in round-trip handshakes. By following an agreed upon protocol, which occurs on clock edges, the transfer process gains considerable speed.

The burden of flipping A1 always rests on the host. Once XACK is asserted, the master can wait an arbitrary number of cycles before flipping A1; this means that it can accept data at any rate. The burden of handling the second word rests on the slave because there is no handshake on the second part of the transfer. Once A1 flips, the slave must handle the data.

Multibus/STD+ bus connection

The large number of data acquisition interfaces available on the STD bus led to the decision to equip the system with a STD bus. While the simplest approach to providing the system with a STD bus would have been to incorporate another bus adapter, this would have required the 68000/68010 CPU to supply all STD device control. Results would have decreased Bell Labs' Unix System III performance when there were high levels of data acquisition activity, and less predictable data acquisition performance. A separate processor avoids these problems and makes the connection between Multibus and STD bus devices.

Making this connection, DA/CP is a programmable, DMA controller based on an 8-million instructions per second (MIPS) bipolar bit-slice processor, which executes each instruction in 125 ns (Fig 4). The DA/CP also contains 1024 locations of 40-bit storage for the control software, 256 locations of 24-bit temporary data storage, two 16-element first in, first out (FIFO) buffers, and one 64-element FIFO.

These components allow devices connected to the STD+ bus to input or output data to buffers within an application program. Designed as an enhanced industry standard, the STD+ bus combines two, nine-slot STD buses side by side. These buses share address lines, but have separate data paths and read/write control lines.

Most Z80-compatible 8-bit STD boards plug into the STD+ bus; however, the data transfer rate for these devices is limited to a maximum of 1 Mbytes/s. Several STD+ Masscomp interfaces transfer at rates twice as high as those of normal STD boards; therefore, they plug into two slots. Since data transfer happens over two separate byte-wide pathways, the STD+ bus moves data in and out of the system at up to 2 Mbytes/s (see the Panel).

Since the DA/CP performs 24-bit arithmetic, it can command simple data reduction and data-dependent realtime decisions.

When an application program wants to perform realtime data I/O, it makes a request to the interface handlers resident in DA/CP program memory. The DA/CP uses these routines to manipulate the STD+ bus interfaces. Since the DA/CP performs 24-bit arithmetic, it can command simple data reduction and data-dependent realtime decisions. For example, the DA/CP could acquire 100,000 samples before or after an analog trigger or threshhold event.

Priority-interrupt logic in the DA/CP allows it to respond to interrupts generated by up to ten interfaces on the STD+ bus. This simple interrupt structure, added to the DA/CP's fixed instruction duration, makes data acquisition highly stable and predictable.

The DA/CP was designed as a Multibus peripheral. To ensure that Multibus DMA and interrupt latencies do not affect DA/CP performance, all time critical data is passed to and from the Multibus via hardware FIFO registers. The DA/CP is able

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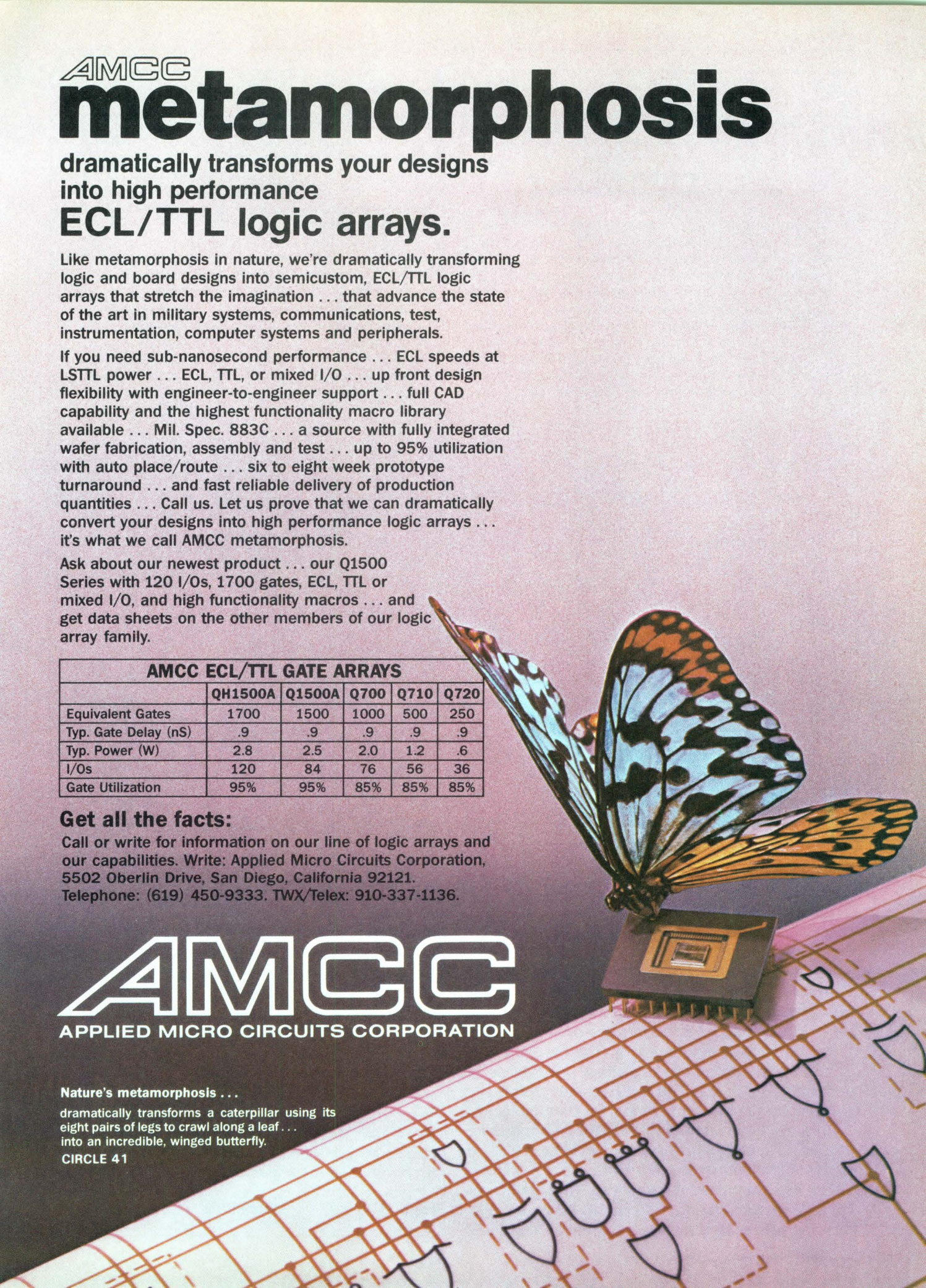

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STD+ bus compatibility

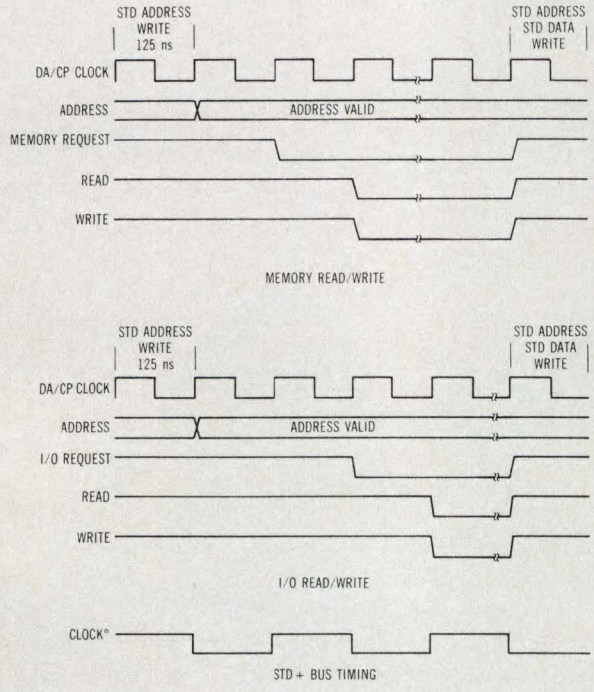
Using the STD bus as the basis of the STD+ bus is relatively straightforward. However, several STD+ characteristics require explanation.

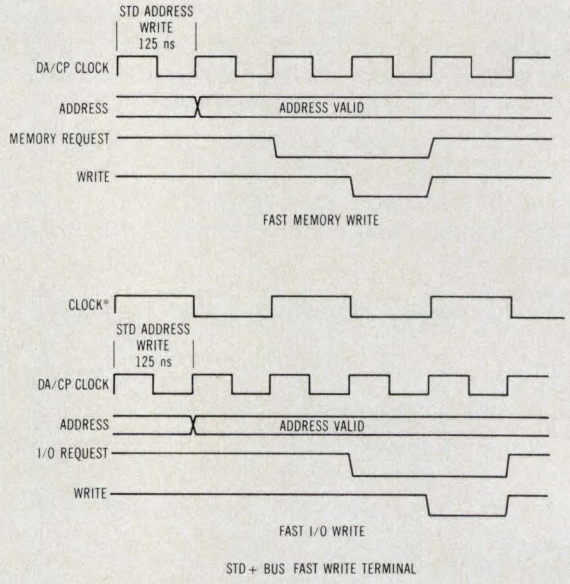
For example, the DA/CP does not issue an INTAK* signal in response to interrupts. An interrupt from a STD bus module must be cleared by a read/write operation to a STD address recognized by that module. An interrupt should be cleared on the leading edge of a read/write operation. This allows the interrupt to clear out of the DA/CP interrupt register before the DA/CP code again enables interrupt service.

The most efficient way to handle this is to have the interrupt service action (ie, a register read operation) clear the interrupt. A status register with an error and a done flag is desirable. The error flag should show when data have been lost because the DA/CP responded too slowly to interrupts. The done flag is the same as the interrupt signal. The DA/CP uses it to distinguish between two modules asserting the same interrupt. A module with more than one interrupt function should have a done bit for each function in the status register.

In addition, the DA/CP does not issue an MCSYNC* signal (sometimes used to synchronize interrupts). A device may assert interrupts asynchronously, or it may use the CLOCK* signal to assert them.

Read/write timings for the STD+ bus are equivalent to those provided by a 4-MHz Z80 processor (see the Fig). But, pins 35, 37, 38, 39, 40, 41, 42, 43, 46, 48, 50, 51, and 52 are not supported. These lines are held at ground. Pins 55 and 56 carry 15V and −15 V, respectively.





to read and write data to main CPU memory by issuing data requests.

A write request is composed of a 24-bit address, followed by a 16- or 32-bit data word; a read request is a 24-bit address. These requests pass through a 64-bit FIFO to the Multibus interface logic. The 16- or 32-bit data obtained from the MC-500's CPU memory pass through a 16-element FIFO back to the DA/CP. Thus, these FIFOs effectively isolate the DA/CP from the Multibus's inherent DMA latencies.

The DA/CP can issue Multibus interrupt requests; these are also passed through the 64-element FIFO to synchronize them with read/write requests. However, when they emerge from this FIFO, interrupt requests pass through a second 16-element FIFO. This prevents data transfers from being held back by Multibus interrupt latencies. Data transfers on the Multibus use the special 32-bit block mode gained through the CPU/Multibus adapter.

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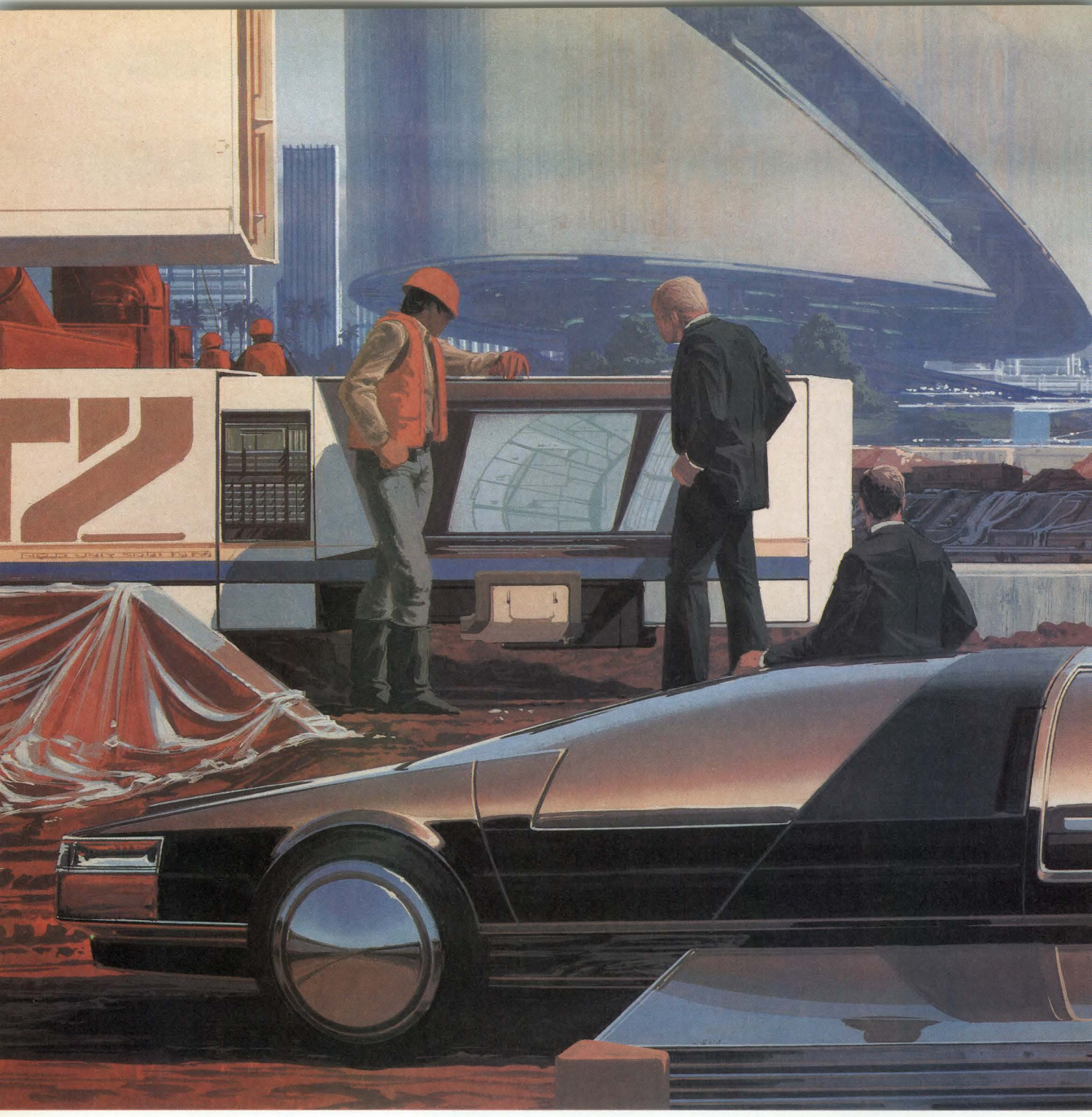

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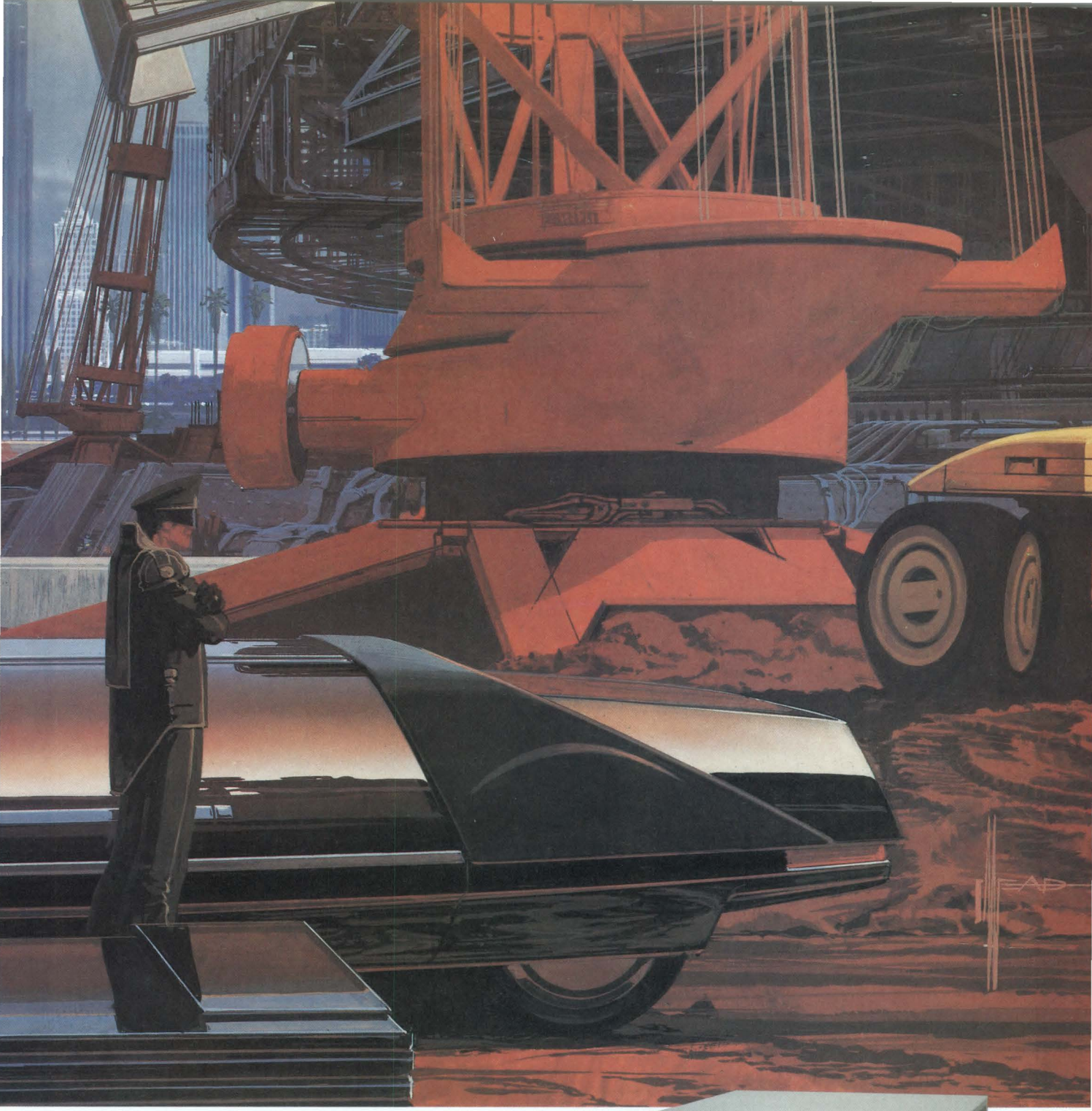

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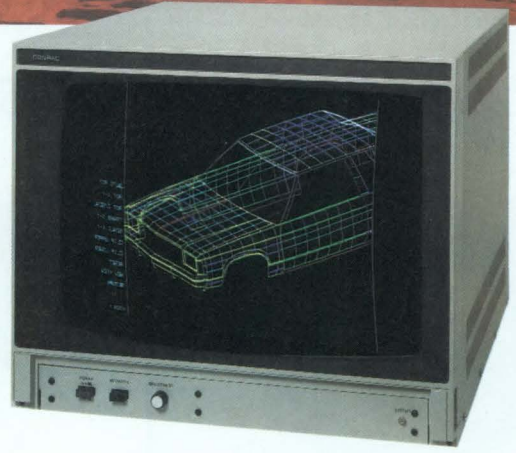

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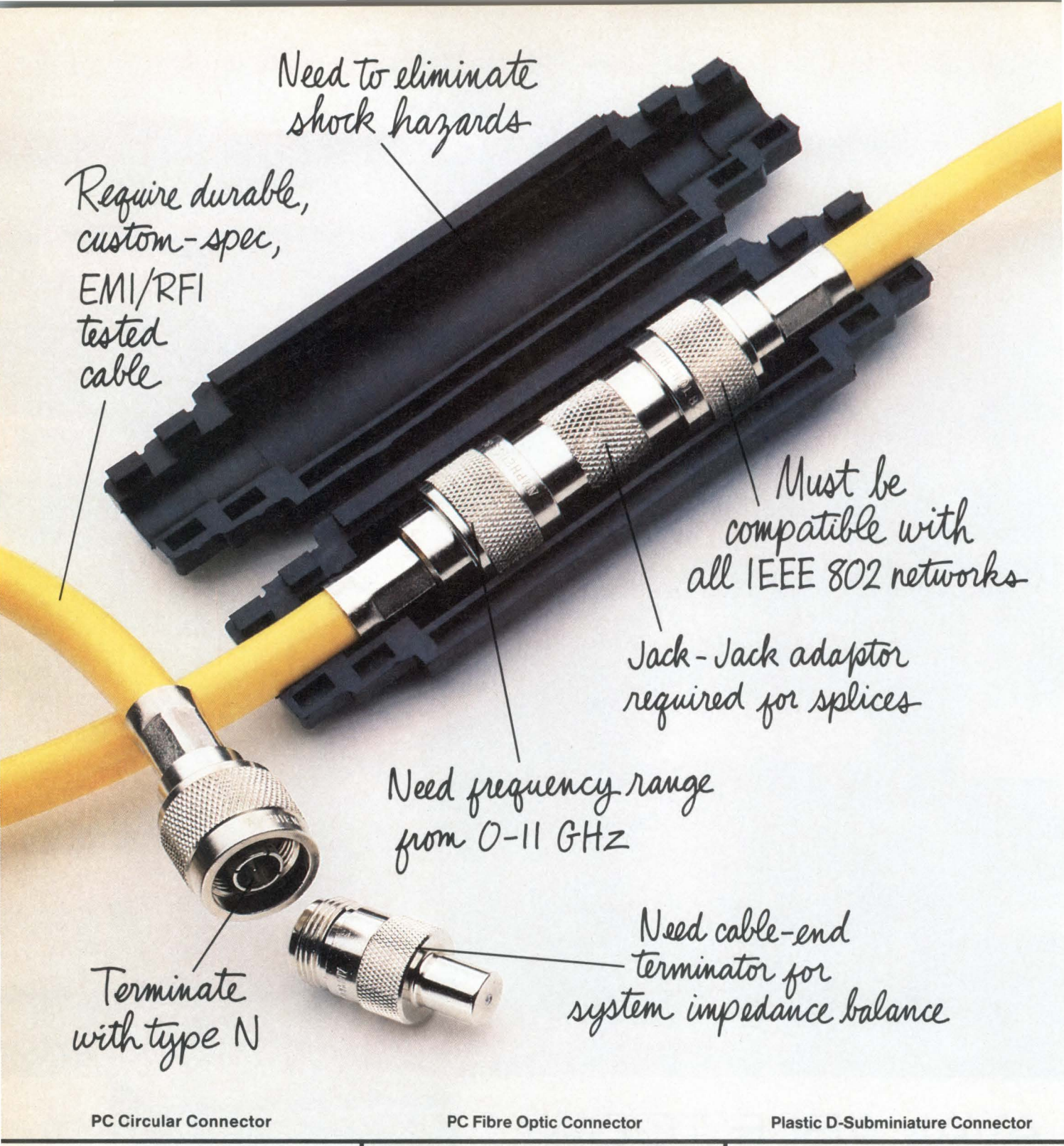

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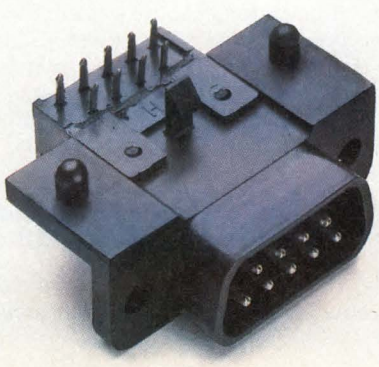

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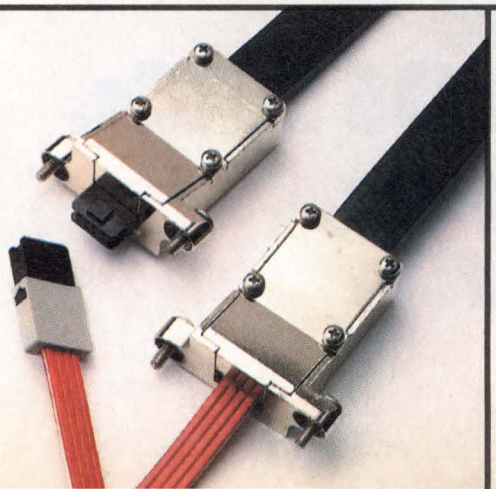

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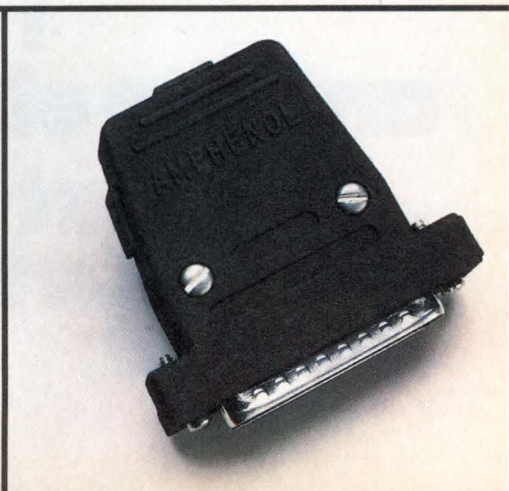

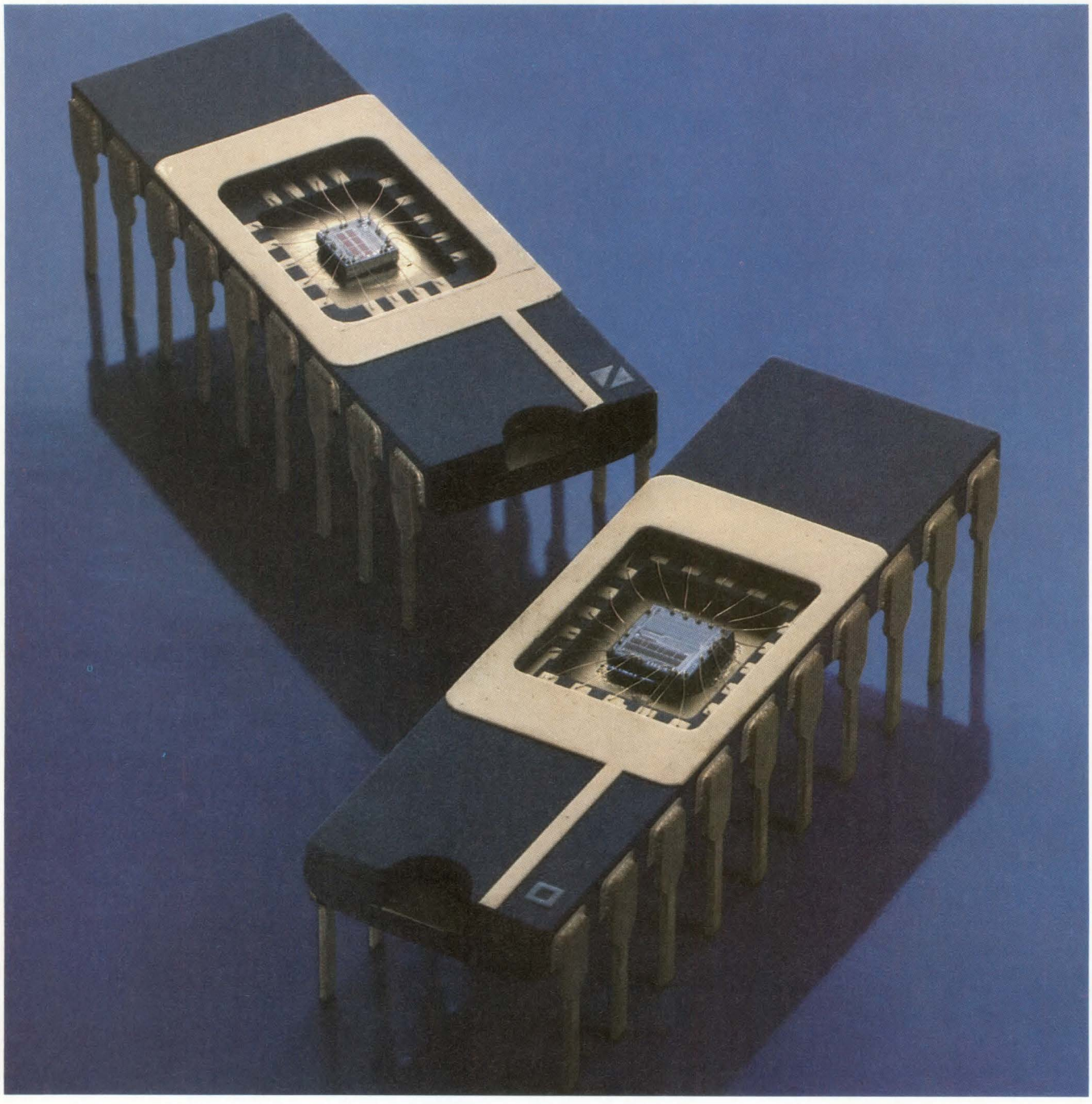

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HOW VOCABULARY IS GENERATED DETERMINES SPEECH QUALITY

Synthetic speech vocabulary can be generated by analyzing natural speech or by artificial construction from phonetic parts, with differing results.

By Michael W. Hutchins and Lee Dusek

Computer games and even appliances can easily add speech output with low cost speech synthesizer chips. Without a vocabulary, however, chips are mute. Words, phrases, and sentences in the vocabulary must be clearly understood, and if required, the sound should be natural and pleasant, not mechanically monotonic.

A vocabulary can be assembled from written text by means of artificial phonetic approximations, or from real speech (Fig 1). For large vocabularies exceeding several hundred words, artificial constructive/synthesis word and phrase generation appears attractive because vocabulary size in a given language is virtually limitless. However, its artificial source in phonetic speech parts—like sets of phonemes and allophones—makes it difficult to get an understandable, natural sound.

Real speech as a vocabulary source generally produces the highest quality results and, at least for small vocabularies, the lowest cost system. This approach involves collecting words, phrases, and sentences from speakers having the desired voice characteristics; converting this analog data to digital form; analyzing the speech content into spectral coefficients; and encoding these components into a suitable format, such as linear predictive coding (LPC) for storage in a ROM (Fig 2).

Because the analysis/synthesis method derives its vocabulary from actual human speech, the final speech synthesizing resembles real speech more closely in inflection, emotion, and intelligibility. Conversely, speech synthesized by the constructive/synthesis method—piecemeal approximations from text—generally sounds less natural. With this artificial approach, sound variations that depend on an utterance's context (ie, what sounds precede and follow it, and where within the word, phrase, or sentence the utterance appears) are difficult to generate accurately.

Using spectral coefficients

Whether the natural speech analysis/synthesis or the artificial constructive/synthesis method is used, spectral coefficients are involved. Entire words or phrases in most current synthetic speech systems are analyzed into spectral components in the former case, or built up from selected component sets in the latter case.

Constructive synthesis can be based on phonemes, diphones, demisyllables, or morphs. Of these, phonemes are usually employed in modern speech synthesis. Phonemes emphasize an alphabet-like simplicity. Accordingly, American English can be created from just 40 to 50 (of about 90 total) phonemes. This is accomplished by following an appropriate set of rules requiring a minimal amount of memory storage space.

Michael W. Hutchins is product engineer for the Speech Products Dept, at Texas Instruments, PO Box 1443, MS 6418, Houston, TX 77099. Mr Hutchins received his BS in biology and BA in psychology from the University of California at Irvine.

Lee Dusek is substrategy manager for the Speech Products Dept at Texas Instruments, Houston. She has been involved with the use of speech processing algorithms on minicomputer and microprocessor-based systems. Ms Dusek holds a BS in math from Longwood College and an MS in Math and an MSISE from Ohio State University.

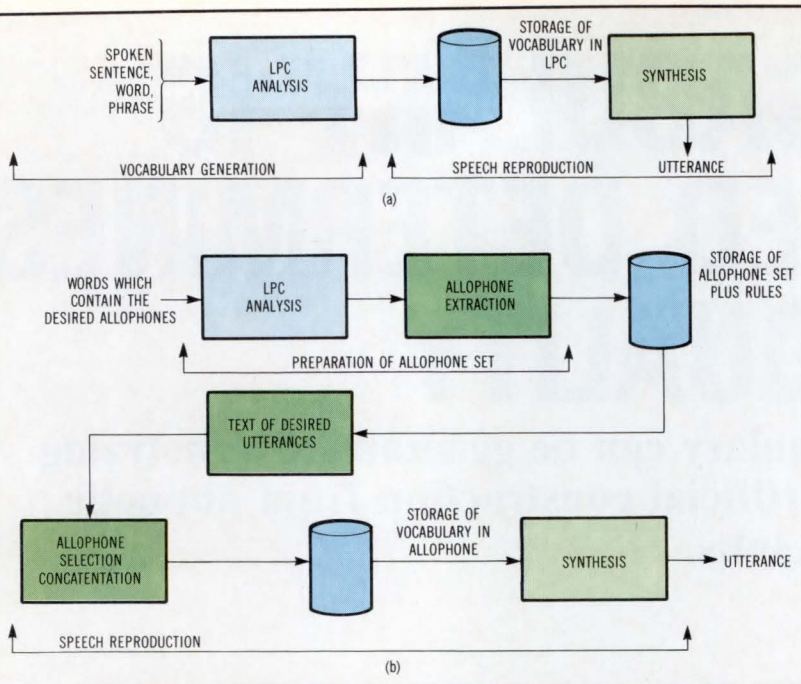

Fig 1 Analysis/synthesis (a) and constructive/synthesis (b) are the two major approaches to vocabulary generation.

Phonemes include speech characteristics like voicing and manner. Any voiced sound, including a voiced phoneme, is produced with vibrating vocal cords. In English, voiced phonemes include all the vowels and 11 consonants. Eight other consonants produce unvoiced phonemes. Articulation depends on the way sounds are modulated by the lips, tongue, and teeth: full closure produces a stop, or plosive sound or phoneme; partial closure produces a fricative.

Allophones needed

Phonemes alone are not enough to characterize speech so that reconstituted synthetic speech can be made to sound nearly natural.

In constructive synthesis, deciding which collection of speech components to use requires a closer look at speech sounds. There may be hundreds of minor variations between sounds that are categorized roughly as the same. For example, the /P/ sound in "pin" is aspirated, that is, followed by a puff of air. The /P/ sound in "spin" is not aspirated. Sounds that are slightly different but generally perceived as the same are the phonemes of a language. Subsets of phonemes that change slightly depending on the context or environment in which the sounds appear are called allophones. Thus, the unaspirated /P/ sound in "spin" and the aspirated /P/ sound of "pin" are different allophones of the same phoneme, /P/, and represent the sound more accurately than the phoneme. In order to preserve this linguistic accuracy, the TI text-to-speech system uses allophone stringing to form words and phrases.

Allophones are more fundamental than most other linguistic components, except morphs. About 130 allophonic sound characteristics can provide the needed variations for all the phonemes.

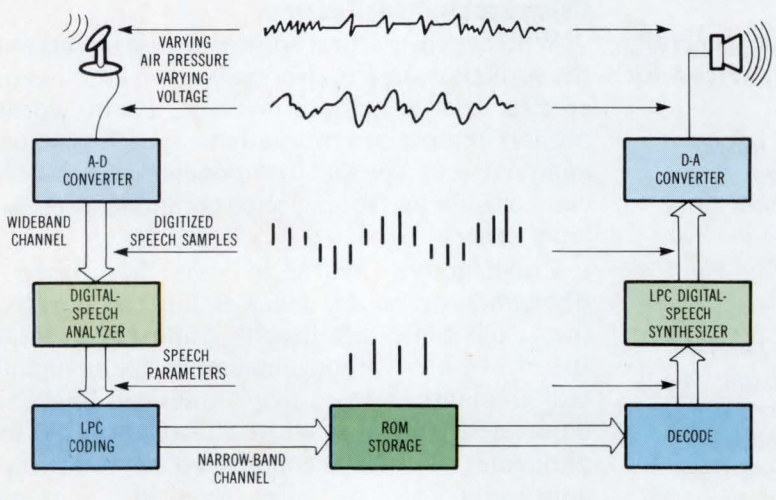

Fig 2 Generating a vocabulary from natural speech produces a more natural sounding synthetic speech.

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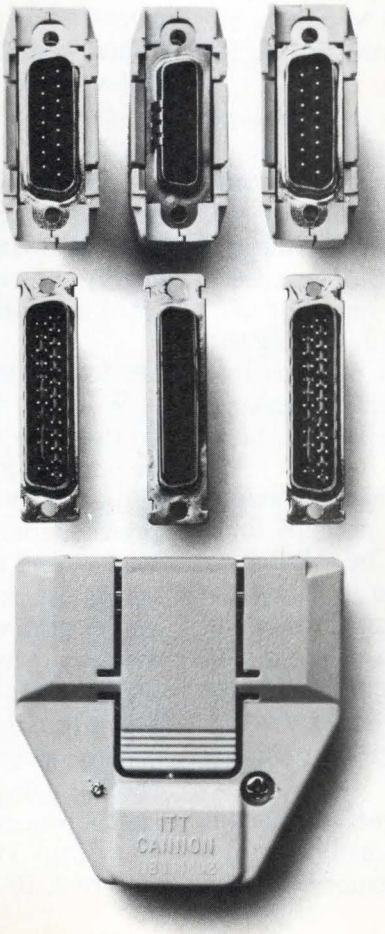

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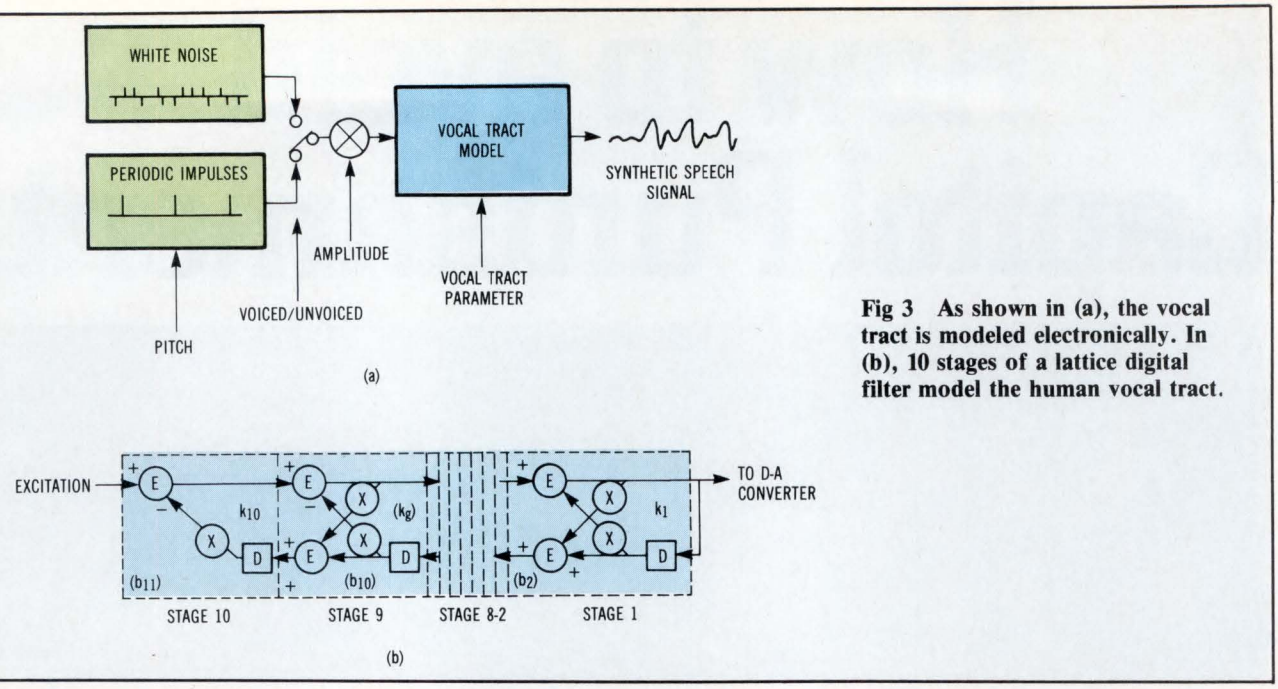

Fig 3 As shown in (a), the vocal tract is modeled electronically. In (b), 10 stages of a lattice digital filter model the human vocal tract.

Consequently, in order to preserve linguistic accuracy, Texas Instruments' text-to-speech system utilizes allophone stringing to form the words and phrases.

Allophones provide many of the subtle variations each English phoneme can encompass, and allophone rules can select each variation in an appropriate relationship to the utterance's context. Although much better than a pure phonemic approach, the allophonic help is not perfect. Some speech systems, such as Lingua and Mitalk, use a more complex morph approach for still higher quality speech.

However, there are drawbacks to a morph system. While a good quality set of 128 allophones (set sizes can range from 80 to 500) can be stored with its 650 rules in less than 10 Kbytes of memory, a typical high quality morph system needs about 600 Kbytes of memory for at least 12,000 of its speech parts. Even with a relatively small number of allophones, most of the stress and intonation, rising and falling inflections, and other speech patterns that convey much of the information when speaking, can still be handled effectively. The speech, however, is still somewhat unnatural.

In a great many applications, this is not a serious problem. For more natural speech, perhaps for a different use, an allophone set can be tailored to that application. Speech can be used in many different places. For example,an automated banking facility must use a clear and pleasant sounding voice, while the owner of a video game arcade may prefer a distorted mechanical sounding voice. Each, accordingly, would be best served by a different set.

Although not perfect, the allophone approach is still a good compromise among many factors. These include vocabulary size, memory storage requirements, versatility and flexibility, hardware and software complexity, cost, and quality.

An allophonic system lends itself to translation from American English text with a reasonably-sized set of rules. Input text from an ASCII keyboard can be automatically converted into allophones. TI's text-to-allophone rules are an enhanced version of work done at the U.S. Naval Research Laboratory. For instance, rules have been added to the basic navy list to ensure that word-ending allophones properly terminate appropriate words. Longer words stress the monosyllables before voiced consonants, and unstressed vowels are used before suffixes such as "er," "ely," and "es" (after t and d).

The resulting rules can then string allophones that are 97 percent correct on only one pass for the 2000 most common American English words. (Accuracy, however, drops to about 92 percent when word usage frequency is measured.)

LPC forms the basis

Whether words to be synthetically spoken are from text or from natural speech, these words must be coded for use with a digital speech synthesizer chip. LPC is a particularly effective form of compressed speech digital data. While all the allophones and essential rules needed to construct 200 words use only 10 Kbytes of memory, the equivalent custom vocabulary would require 16 Kbytes of memory. Moreover, the system data rate must be a higher 1200 bits/s than the allophonic 400 to 600 bits/s to convey speech at a realtime rate.

The speech synthesizer chip, driven by LPC speech data, is essentially an electronic, digital signal processor model of the human vocal tract [Fig 3(a)]. The p-channel MOS (PMOS) device consists of a 10-stage time-varying digital lattice filter

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and associated control logic [Fig 3(b)]. Its source is an internal digital excitation function when producing voiced sounds, and a digital white-noise generator when delivering unvoiced sounds. Because the synthesizer has 10 stages, the vocal tract parameters, or LPC data supplied to it, are designated LPC-10.

Voiced sounds are coded for energy levels and pitch and for 10 so-called filter reflection coefficients (K_1 through KPV_{10}), according to Table 1. Together, the chip receives 247 levels of data coded with 49 bits (plus an extra bit for a repeat operation) for each 25 ms of operation, called a frame.

The synthesized speech output consists of 10 bits output every 125 μs and are converted to an analog signal of up to 1.5 mA (with a resolution of 5.9 μA). This is more than sufficient to drive a power audio amplifier. The 7 low order bits determine the magnitude of the analog output level. The MSB of the 10-bit word is the sign bit, which, when combined with the next two bits, is used to force the output driver to full on or full off.

Although the LPC-10 parameter input to the synthesizer needs 50 bits to describe them, the commands to the synthesizer are minimal—just six operational commands make up the total (Table 2). Thus, a synthesizer chip needs minimal control from a host processor (typically less than 1 percent). The host passes commands only to initiate specific activities and does not involve itself in carrying out the speech producing activity. Thus, the host selects data for the desired word, phrase, or sentence by locating its starting address; passes a command, such as speak external; and sends the required data from memory.

TABLE 1

Parameter Coding

Parameter	Levels	Code bits
Energy	15*	4
pitch	64	6
K_1	32	5
K_2	32	5
K_3	16	4
K_4	16	4
K_5	16	4
K_6	16	4
K_7	16	4
K_8	8	3
K_9	8	3
K_{10}	8	3
12	247	49 + repeat = 50 bits

*Energy = 1111 is the stop code

TABLE 2

Synthesizer Commands

Data Bus Command Code (D_0-D_7)*	Operation
X000XXXX	NOP (No operation)
X001XXXX	Read byte
X010XXXX	NOP (No operation)
X110XXXX	Speak external
X011XXXX	Read and branch
X100AAAA	Load address
X101XXXX	Speak
X111XXXX	Reset

*A = Address
X = Don't care

Synthesizer chip handles both speech sources

Both the constructive/synthesis method of stringing allophones together from a library by given rules, and the analysis/synthesis method of analyzing natural speech, end up in LPC-10 form. For this reason, the TMS5220C synthesizer chip can work with data derived from either source. However, when derived from a natural source, with a relatively low cost development system, the user has more complete control over speaker, dialect, inflection, and other speech characteristics, including language. Moreover, it is even possible for sound effects to be analyzed and synthesized from natural sources.

Analysis/synthesis is language independent; constructive/synthesis is not. The latter requires a completely different set of allophones and rules for each language or even for each dialect. Dialect is a complicating factor in reproducing speech sounds from the multilingual areas of Europe and Asia. This may be overcome, however, by using a common multilingual subset of allophones with only the language-specific allophones added to reduce total memory requirements.

To help in applying the analysis/synthesis approach, TI's Dallas speech laboratory has recorded speakers so that potential users can make selections. Then a selected person can be brought in to record the actual words wanted, or customers can bring in their own speakers, or previously recorded speech. In either case, TI can make an analysis and provide the results in LPC-10 on almost any memory device or combination of devices.

Unless customers want to develop their own in-house capabilities, analysis/synthesis allows easy access to an outside agency. Working together, customer personnel and TI speech analysis experts can often reduce vocabulary size substantially by using generic words. Such words cover a variety of situations, yet are specific enough when combined to avoid ambiguity. In this way, storage requirements can be minimized in the final system, and many phrases and sentences can often be strung together with selections from these words. This is especially true where the quality of emotion and intonation are not important, as in a learning aid such as TI Speak-and-Spell.

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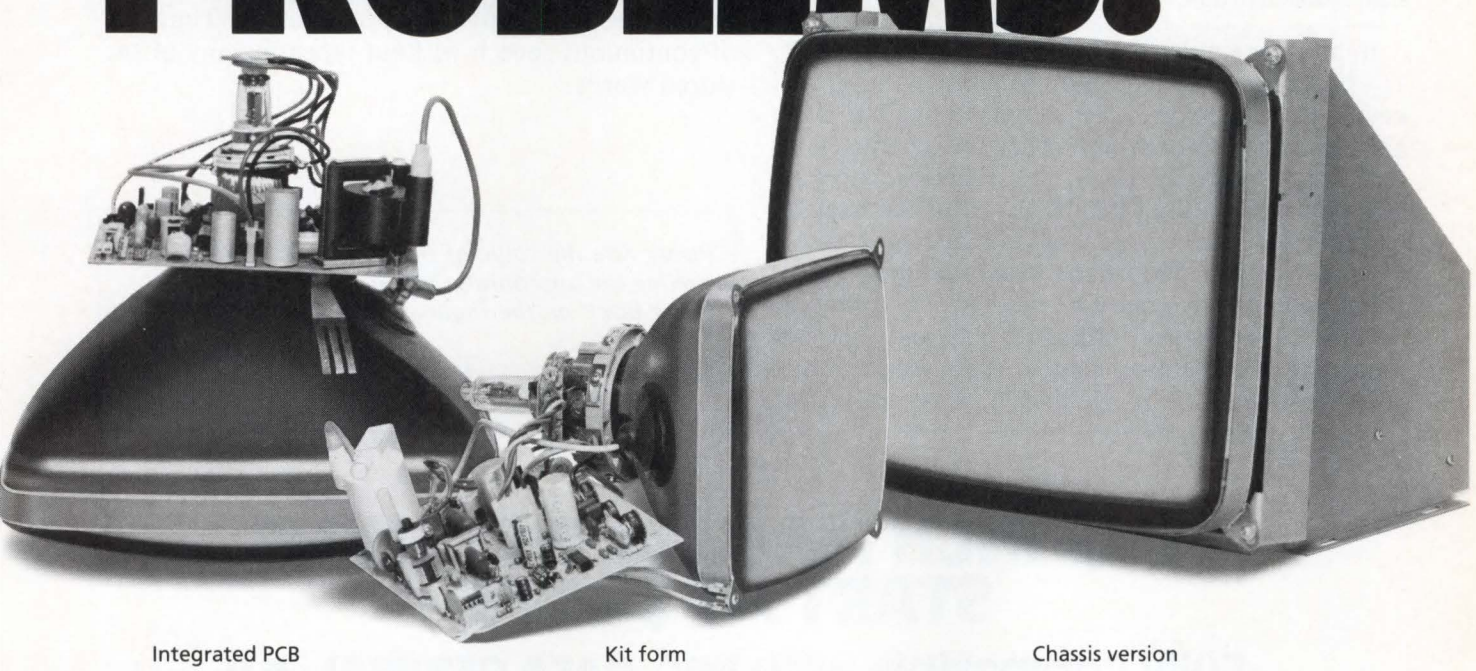

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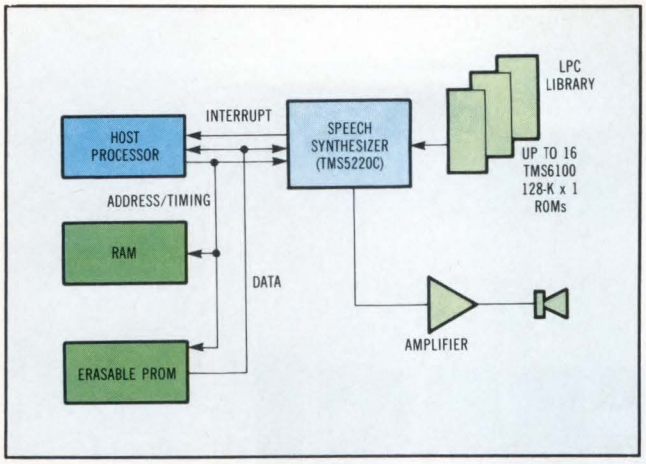

Fig 4 An extensive LPC library can be handled by the TMS 5220C synthesizer chip.

In another similar but more complex application, TI programmed a huge Mandarin alphabet keyboard with about 1260 characters on it to echo back individual words and other text characters as they were entered. Even for English, checking keyed-in material by listening to words fed back on earphones would be a great aid in reducing errors. A selection of just 500 of the most common words could be quite adequate for most such applications.

With the TMS5220C synthesizer chip and a custom ROM (one, for instance, made up of several TMS6100 voice synthesis 128-K x 1 ROMs), ROM addressing can be handled automatically without involving the host processor except to provide the synthesizer with a starting address (Fig 4). Until the utterance is completed, the processor is not involved except for possibly checking the synthesizer's status register. This behavior is similar to a built-in DMA system.

The TMS5220C has an onchip 16-byte first in, first out (FIFO) buffer that can hold two full frames of speech (about 50 ms when operated at a nominal system-clock of 160 kHz). When the FIFO's contents fall to less than 8 bytes, the synthesizer can generate an interrupt or set a polling level for the host computer to indicate that more data is needed.

For a vocabulary of several thousand words, a single TMS5220C synthesizer chip can access up to 16 TMS6100 ROMs to provide approximately 30 minutes of continuous speech without repeating any of the stored words.

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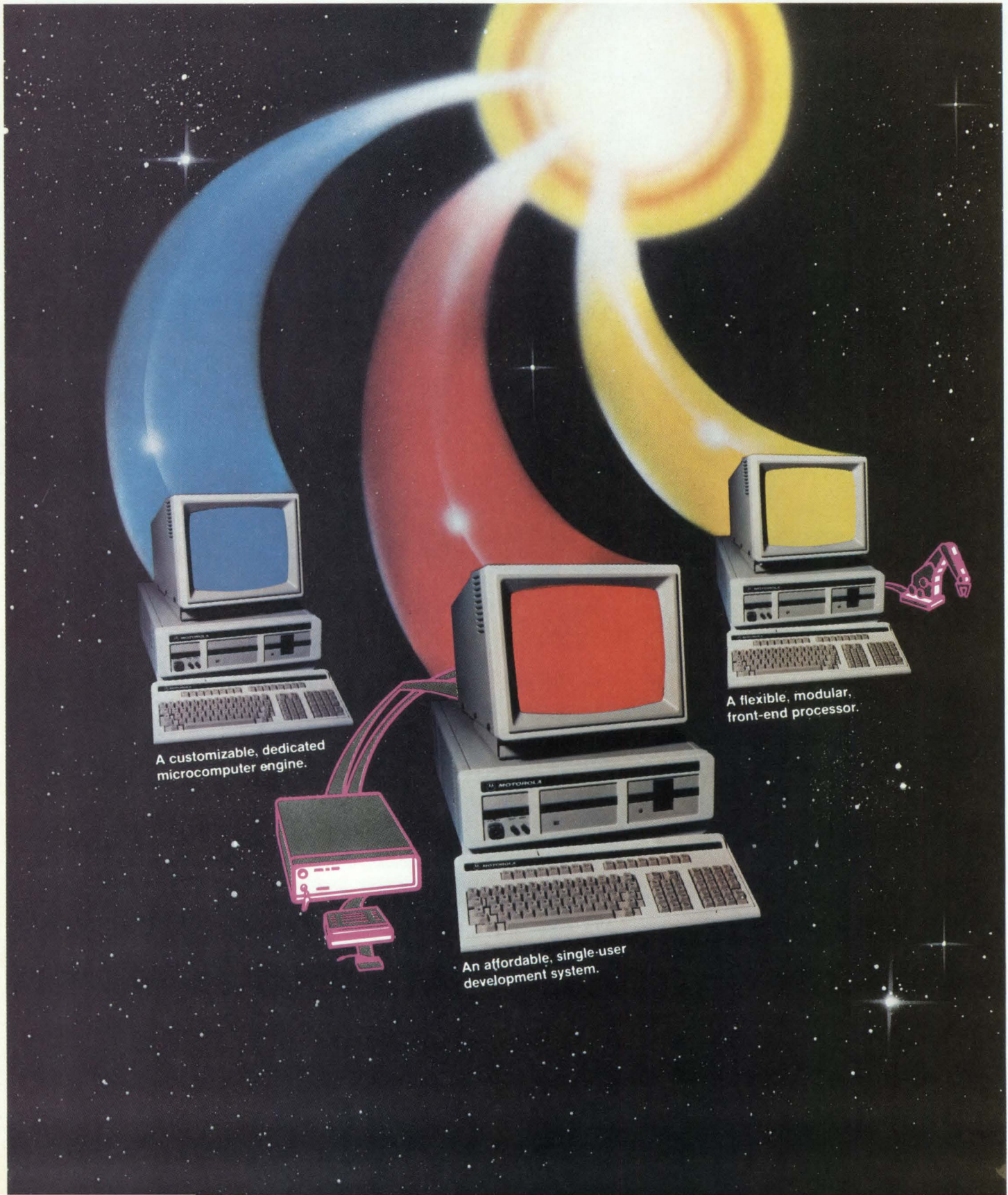

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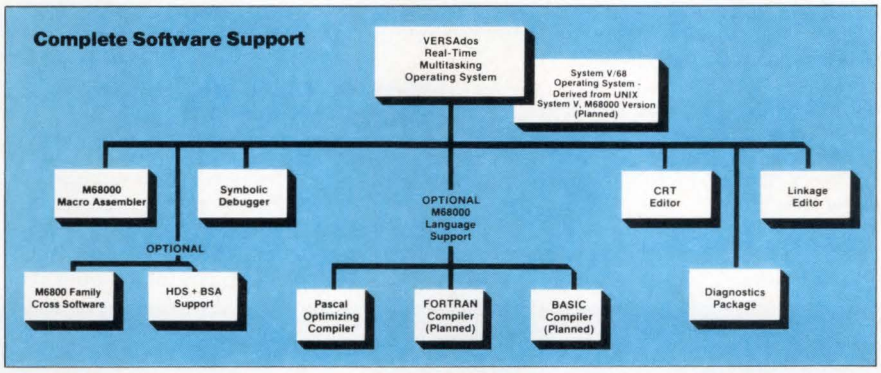

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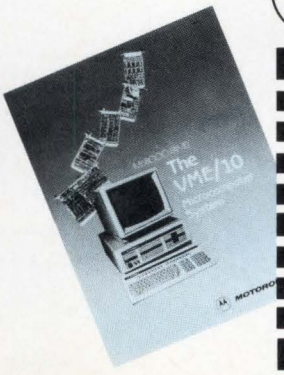

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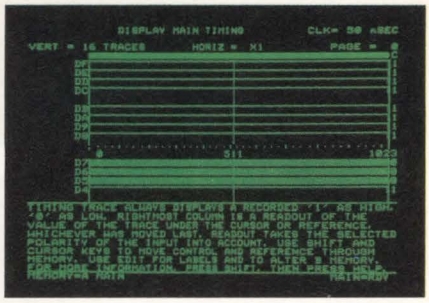

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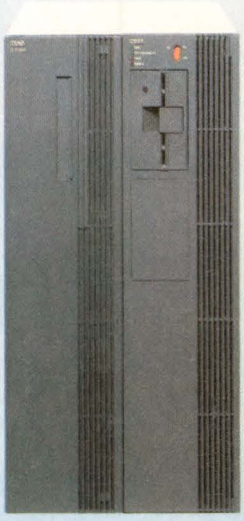

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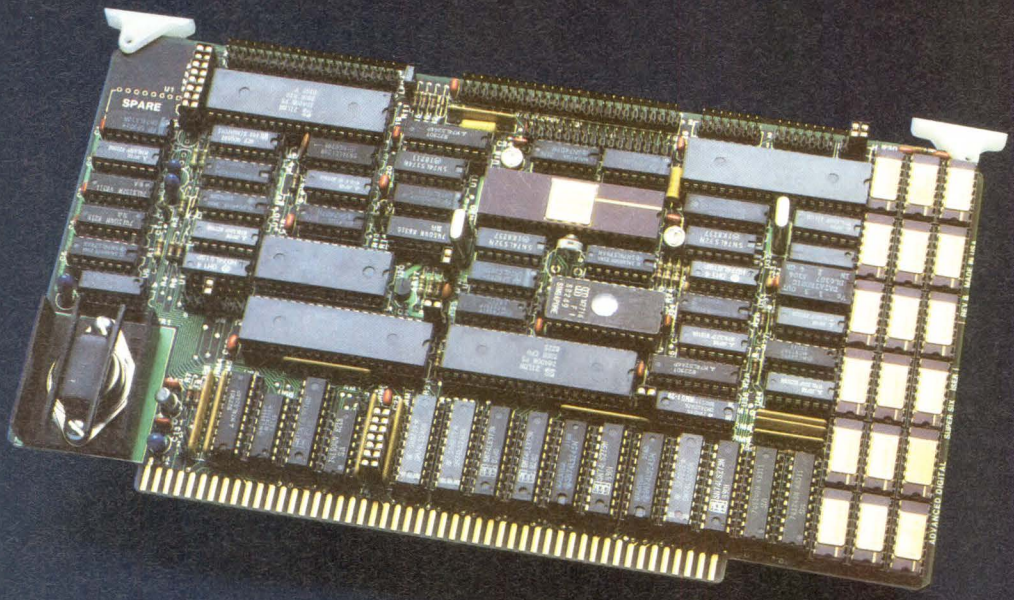

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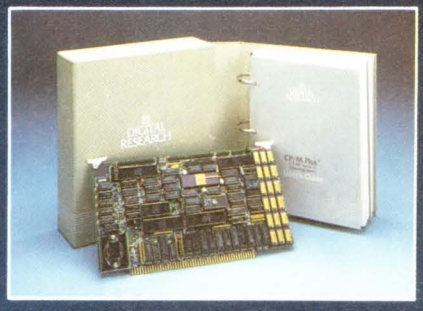

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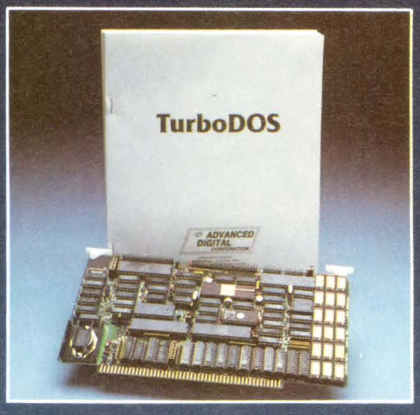

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ARRAY PROCESSOR ACHIEVES 100 MFLOPS

Parallel architecture and fast hardware team up with a resident operating system to speed data flow and minimize host communication.

by Robert Hausman and Phil Cannon

Until recently, a gap of roughly an order of magnitude has existed between the computation rate of supercomputers (eg, the CDC Cyber 205 and the Cray machines) and that of the fastest array processors. An affordable machine that approaches the speed of today's supercomputers is needed to solve the increasingly complex problems in seismic exploration, image processing, simulation, and signal processing. Computation requirements in seismic exploration, for example, have progressed from those involving two-dimensional arrays to three-dimensional ones. To obtain results in an acceptable time, throughput must be much faster than what existing mid-sized array processors provide, and at costs below the several million dollar price tags of supercomputers.

With a 100-mega floating point operation per second (MFLOPS) maximum internal computation rate, the ST-100 array processor addresses this need by combining fast parallel processors, a large onboard memory, and parallel programming techniques. The array processor's design incorporates several hardware improvements. An 8-Mword main memory allows block transfer of large scale computation routines (processes) from host to array processor together with the large data arrays that will undergo operation. A multichannel I/O subsystem provides high speed communication with the host computer and with dedicated peripherals. A separate parallel processor controls internal movement of data. All parallel hardware elements operate in time-overlapped fashion under direction of a control processor.

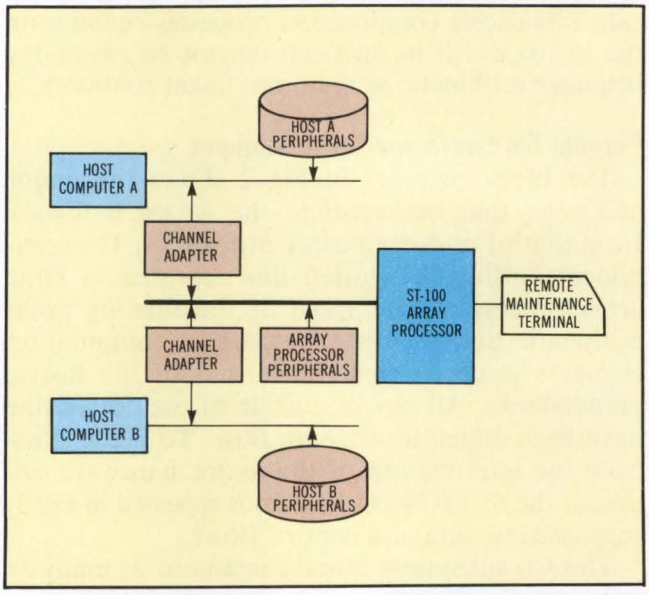

Fig 1 In the host/array processor system, the ST-100's intelligent I/O controller allows use of the array processor with multiple and different host computers.

The large scale computation routines are written in a higher level array processor control language. This allows the user to develop processes for execution on the array using a Fortran-like language. Another significant innovation relative to conventional array processors is an operating system that coordinates simultaneous execution of various programming levels on the parallel hardware elements.

This combination of hardware and software results in computation speed rivaling that of multimillion

Robert Hausman is vice president of R&D Engineering at Star Technologies, Inc, 1200 Benjamin Franklin Plaza, One SW Columbia, Portland, OR 97258, where he was the principal architect of the company's ST-100 array processor. Mr Hausman has a BSEE from South Dakota State University.

Phil Cannon is a senior consultant at Star Technologies, Inc, where he was an initial contributor to the design of the architecture and instruction set of the ST-100 array processor. He holds a BSEE from the Illinois Institute of Technology in Chicago and is a member of the IEEE and ACM.

dollar supercomputers. Parallel support hardware and multilevel programming permit attainment of a high percentage of the arithmetic unit's 100-MFLOPS maximum.

Like other array processors, the ST-100 operates in conjunction with a host mini or mainframe computer and attaches physically to the host like any other peripheral device (Fig 1). Note, however, that this array processor can be shared by more than one host and that it can have its own peripheral devices.

Logically, the array processor acts as an extension of the host processor, executing computation-intensive application routines called processes. Properly speaking, three levels of application software execute on the host/ST-100 system. At the top is a host Fortran application program. This program calls large scale computation processes running on the ST-100 which in turn call macros (ie, assembly language arithmetic or data movement routines).

Parallel hardware speeds throughput

The block diagram in Fig 2 shows the major additions that differentiate the ST-100 hardware from that of mid-sized array processors. The components inside the dotted line represent a large array processor. The speed of the floating point arithmetic unit with its five parallel computation elements is up to eight times that of the fastest predecessors. All blocks outside of the dotted line have been added to aid data flow. To better illustrate the interrelation of the major hardware elements, the ST-100 block diagram is repeated in Fig 3, emphasizing data and control flows.

The I/O subsystem block consists of as many as eight parallel I/O processors, seven device interface adapters, and a DMA channel. Through this block flows all data and control communication between the array processor and the outside world.

One of the parallel I/O processors is dedicated to internal system control while the others are connected through interface adapters to host computers or to array processor peripherals. The interface adapters match the hardware characteristics of the external devices to those of the array processor. Each I/O processor is capable of operating at rates up to 12.5 Mbytes/s with a maximum multiplexed channel rate of 25 Mbytes/s to/from the main memory. The DMA channel can transfer data at rates up to 100 Mbytes/s.

The control processor (CP) has been added to the conventional array processor architecture to coordinate the many parallel elements of the ST-100. To do this, it uses its own operating system, the array processor monitor (APM). This operating system runs on the CP and supervises the execution of application programs in the various elements. The application processes execute on the CP.

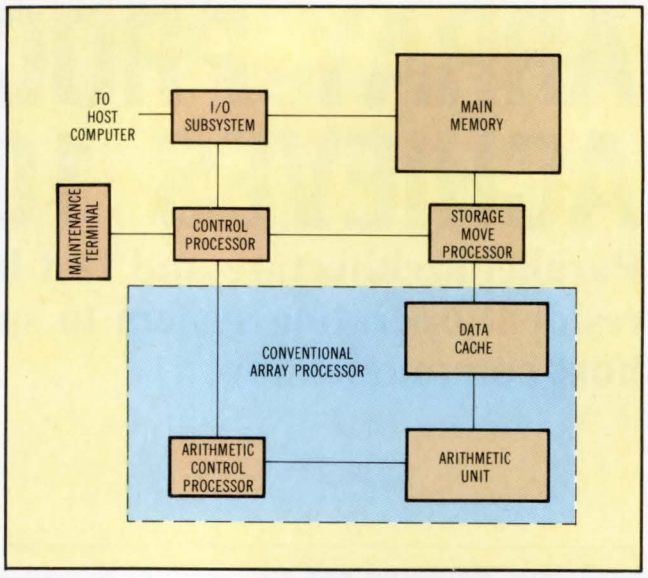

Fig 2 Additional parallel hardware elements (outside dotted line) add to conventional array processor elements to aid program and data manipulation and reduce host overhead.

All activities of the ST-100 are scheduled by the CP. It initiates and synchronizes program loading and execution for all of the ST-100's other processors. Hardware design permits the queuing of commands to both the storage move processor (SMP) and arithmetic control processor (ACP) so that their functions can be both synchronized and time overlapped.

The CP is built using two Motorola 68000 microprocessors, clocked at 80 ns. They share a 192-Kbyte memory with each processor also having a nonshared 32-Kbyte memory. Cycle time for the memory is 120 ns. One of the microprocessors executes the APM operating system and controls the I/O subsystem, the maintenance terminal, dead start, and the other microprocessor. The second microprocessor executes array processor application processes. To accomplish this, it communicates with the main memory, the SMP, and the ACP.

A large main memory (up to 8 million 32-bit words) allows complete application processes to be transferred from the host to the array processor as single blocks. In previous designs, such a task would have been broken down into multiple transfers of smaller computation routines. In addition, return of intermediate results would have been necessary, all with attendant host overhead. Memory size also permits storing of multiple application processes for sequential execution. The marked reduction in time-consuming host/array processor communication enhances computation throughput substantially.

Three 32-bit wide main memory ports are assigned respectively to the data I/O channels, a DMA channel, and the data cache. The data I/O port operates at 25 Mbytes/s, while the DMA and data cache ports operate at 100 Mbytes/s. The eight-way

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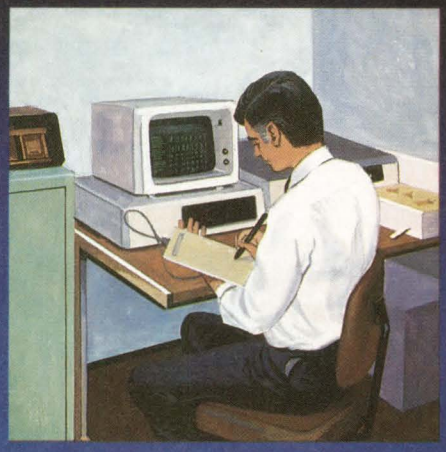

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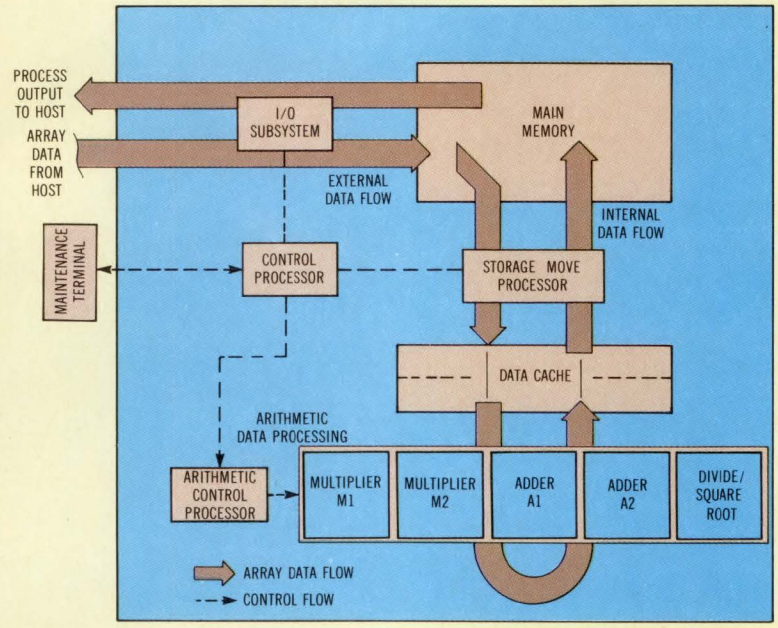

Fig 3 Under supervision of the control processor, data can be physically and logically moved about in main memory and between main memory, data cache, and arithmetic processor. Automatic reformatting of data can also be done without host intervention.

interleaving of 320-ns access time memory devices allows a complete 32-bit word transfer every 40 ns. An extra 7 bits per word provide single-error correction and double-error detection.

The data cache provides fast access working memory for the floating point arithmetic unit. It consists of three physical noninterleaved banks each containing 16 Kwords of 32-bits each. Each bank has address space available to allow expansion to 65 Kwords per bank. The CP can divide each bank into two logical sections and assign any of the six possible logical sections to either the SMP or the ACP. Three accesses to the cache memory by the ACP and one by the SMP can be made in every 40-ns machine cycle.

Parallel processing advances execution

The SMP executes macros loaded into it by the CP. These macros control data movement between ST-100 main memory and the data cache. The SMP can perform complex address generation for both memories as well as on-the-fly data format conversion between them. Since it operates in parallel with the other processors, data movement can be time overlapped with floating point computation and control program execution. Upon completion of its assigned task, the SMP issues an interrupt to the CP.

An 80-bit wide control word allows the three ALUs within the SMP to run in parallel. A 32-bit ALU performs 32-bit main memory address generation and can also perform auxiliary 32-bit integer computation. A 16-bit ALU can address any of three data cache banks as well as control bank selection. A second 16-bit ALU provides loop control for the two address generation ALUs. The SMP also controls conversion between the various data formats that may be stored in main memory and the ST-100's internal formats (ie, two's complement 32-bit integer and 32-bit floating point). A three-stage, pipelined conversion unit reformats data during transfers between main memory and the data cache.

The arithmetic section controls and executes the application computations on array data. It contains two parts: an ACP and a floating point computation subsystem. The ACP is a microprogrammed device, which contains three ALUs that generate addresses to and from the data cache plus a fourth for loop control. It has its own 4-Kword x 128-bit micro instruction memory; address space permits an increase to 16 Kwords. The 128-bit wide control word permits parallel performance of four integer ALU operations, four floating point arithmetic operations, one test-and-branch operation, and three memory references during each 40-ns clock cycle. The ACP also controls a crossbar switch between the data cache and the floating point computation subsystem. This switch enables a process or other macro to treat the three banks in the data cache as logical rather than physical banks so that they can be assigned to the three address generators in any order.

Thus, the ACP can move data logically about in the cache for different calculations without time-consuming physical movement. Within the floating point computation subsystem, a data interchange

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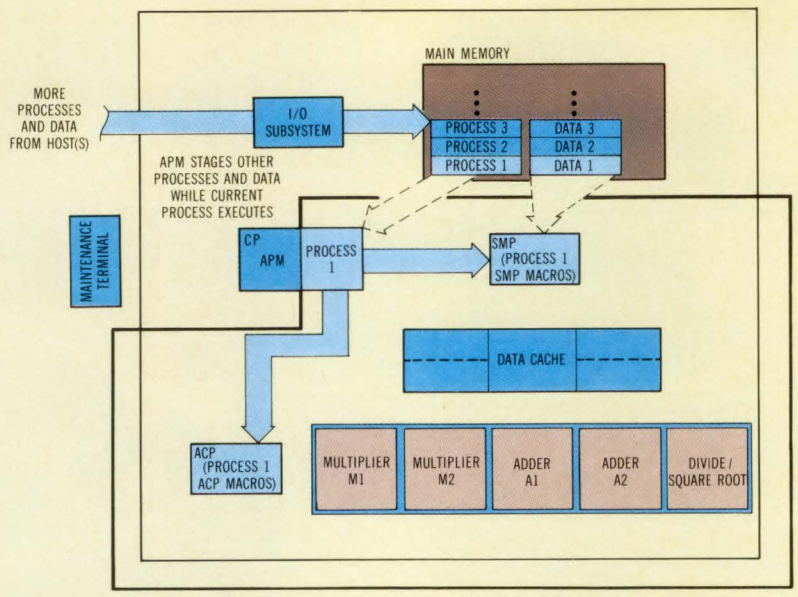

Fig 4 With the storage and sequencing of multiple processes, the array processor monitor (APM) operating system can schedule and coordinate the operations of the ST-100's parallel hardware elements to optimize throughput.

unit maintains an orderly flow of operands between the data cache and the parallel arithmetic elements. It universally distributes the operands between the individual arithmetic elements without having to return intermediate results to the data cache.

Two adders, two multipliers, and a divide/square root unit comprise the floating point computation elements. The adders and multipliers are three-step pipelines executing at 25-MHz (40-ns) clock rates. The divide/square root unit requires 13 clock periods for a complete calculation. With the four adders and multipliers in operation, the arithmetic unit's computation rate is 100 MFLOPS.

Processes reduce communication overhead

Three distinct levels of application software execute on the host/ST-100 system. The top level is the user's Fortran application program, which executes on the host. For traditional array processors, this application program would call array processor computation routines (eg, vector arithmetic, matrix operations, transforms, and filters). Such an approach requires time-consuming host/array processor communication at the beginning and end of each individual computation. While such communication overhead may be tolerable in an intermediate speed array processor, it would severely degrade potential throughput in a machine with an arithmetic unit capable of 100 MFLOPS for certain types of algorithms.

To overcome the communication bottleneck, the ST-100 has added an intermediate application software level called a process. A process can be thought of as a very large application routine which can be called by the host Fortran application program. It encompasses many computation subroutines to accomplish a sizable portion of a total application program (eg, a three-dimensional migration in a seismic exploration program).

A process consists of general purpose control code that executes on the ST-100 control processor plus specialized instructions (macros) for execution on the SMP and ACP. Multiple processes and their associated data can be stored in the array processor's large main memory and executed sequentially as shown in Fig 4.

Other major blocks of ST-100 software are production (executive) software, which is discussed separately below, and maintenance software. Maintenance software consists of idle loop reliability tests that run automatically during any ST-100 idle time, a user confidence test routine that can be called by the application program, and various diagnostic programs. The first two are designed to report on array processor usability; the diagnostic programs aid in fault isolation.

To overcome communication bottlenecks, the ST-100 has added an intermediate application software level called a process.

Two major blocks of software aid the user in coding the application processes discussed above. The first, is the array processor control language (APCL). It is the software counterpart to the parallel elements which make up ST-100 hardware. This higher level language is used to generate the

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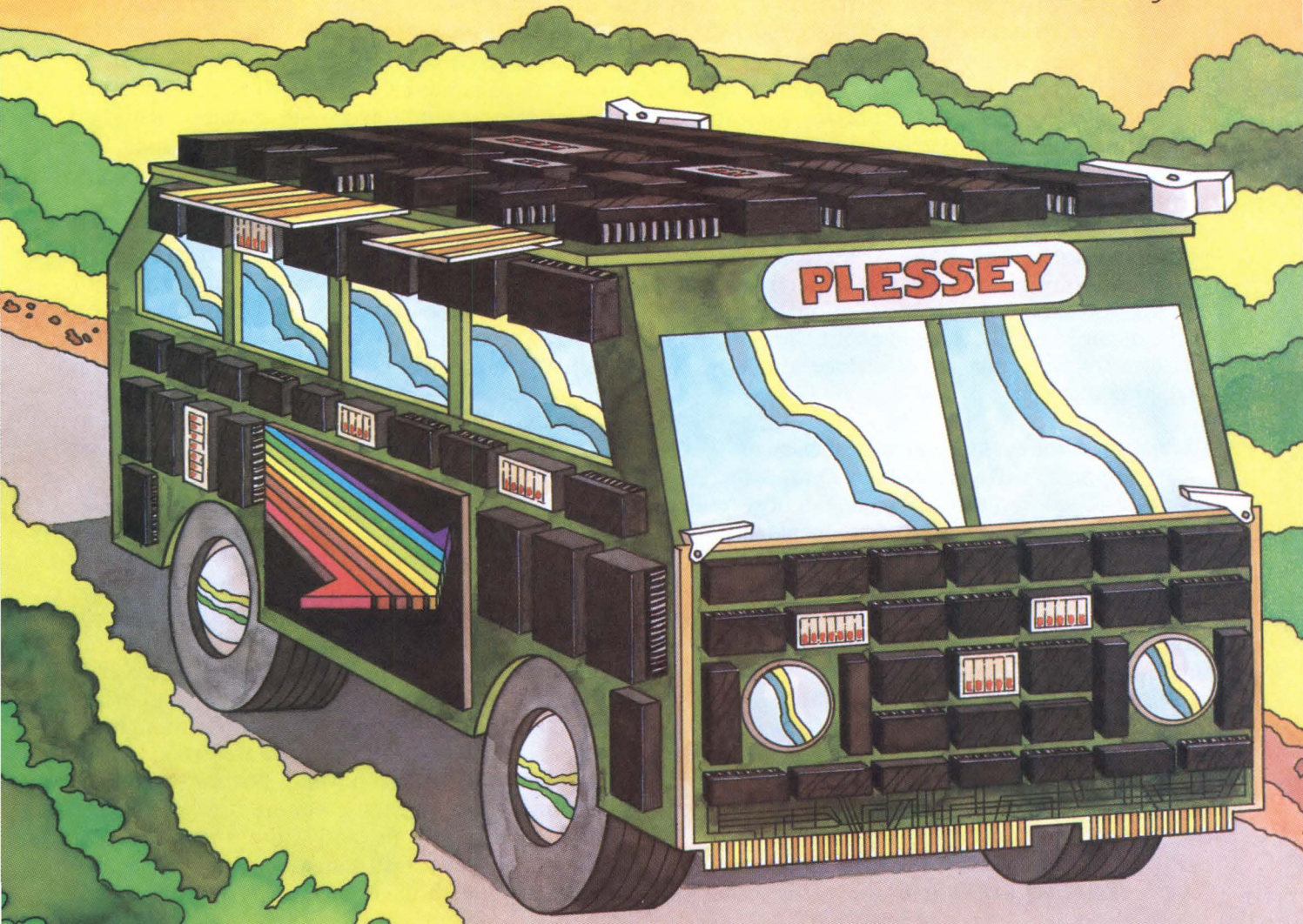

CIRCLE 58

Standard macro types	
Storage move macros are provided for:	Arithmetic macros are provided for:
Moving data between main memory and data cache with format conversion	General vector arithmetic (real and complex)
Performing integer and logical operations on data in main memory or data cache	Vector-to-scalar arithmetic
	Vector logical operations
	Matrix operations
	Transform operations
	Filtering operations

program that will control process execution. The APCL compiler executes on the host to produce a process object module that will run on the ST-100 control processor. It also produces a Fortran host process subroutine (HPS), which can be linked to the host Fortran application program. The ST-100 linker combines the process object module with the called SMP and ACP macros to form a process load module suitable for execution on the array processor. When the host application program calls the process for execution, the HPS module provides the necessary interface to load the process module into the array processor.

APCL is a subset of ANSI Fortran 77 with statements added to control the architectural features unique to the ST-100, such as the hierarchical memory structure. The language also supports service requests to the array processor monitor via subroutine calls. The Macro Assembler is used to write macros for execution on the ACP and the SMP. A meta-assembler concept allows the same assembler to serve both processors. Assembler output includes a source listing with errors and cross references, object code for the target processors, and information to define the relationship between cache memory banks. APCL uses the cache memory relationship in order to determine the crossbar switching control.

Library supports custom macro development

Development software also includes a linker, a debugger to aid in macro debugging, a host-resident simulator (for the SMP and ACP) to aid in macro development, an application support library, and library maintenance facilities. The application support library is a set of macros for performing commonly used storage move and arithmetic control functions. The types of standard macros contained in the library are indicated in the Table. Custom macros can be developed by the user and readily added to the library. The macro level development software is provided for the user to create application specific macros (instructions) to be added to the applications support library.

Production software consists of the array processor executive (APX) and the array processor monitor (APM). These software blocks link the host computer and the array processor for execution of ST-100 processes. The APX interprets a set of Fortran-callable subroutines that interface the user application program to the array processor. It is bound and linked to the application program and executes within the context of the user's address space. APX subroutines enable the user to request array processor resources, define main memory arrays, control data movement to and from the array processor, and release array processor resources.

Resident operating system coordinates operations

The array processor's multiple parallel hardware elements function concurrently. Thus, an operating system is needed to control and coordinate their operation. The APM runs on the CP and oversees all of the activities within the ST-100. It communicates with multiple hosts through the I/O subsystem. This mechanism allows the APM to control data transmission between host computers and array processor main memory and to supervise main memory allocation and protection.

Execution of the multiple processes stored in main memory is scheduled on a priority basis. The APM loads a new process into the CP memory as soon as space becomes available. Execution of the new process is initiated by the APM upon completion of the currently executing process. When an application partition is released by the user, the APM returns accounting information to the host.

Turning to array processor application software, the user's fundamental concern is process development. All process development takes place on the host computer. This results in two blocks of code—a process load module which will execute on the array processor, and an application load module (ie, HPS), which will execute on the host. The top level of application software is a Fortran application program, which will execute on the host computer. This application is developed using standard host Fortran development software.

An APCL process is logically divided into a declaration section and an executable section. Process statements, Memory statements (main memory, cache memory, and local memory), and Data statements make up the declarations section. Process statements identify processes and list arguments being passed between the host and the process. The executable section contains Assignment statements as well as Call, Continue, Do, Goto, arithmetic If, logical If, Return, and End statements. These statements have their normal Fortran meaning. Assignment statements compute the results of arithmetic expressions and store them in local memory locations. Call statements initiate the execution of SMP and ACP macros or of service

requests. Return and End statements transfer control to the host application program. To code processes the user also needs an understanding of functions executed by the application library macros and of data cache mapping.

All process development takes place on the host computer.

Main memory statements allocate storage of array data in main memory. Local memory statements assign space in local memory (memory contained within the control processor) for scalar variables to be used in controlling process execution. Data statements assign initial values to local memory variables. Cache memory statements allocate space for data in the six logical sections of the data cache discussed earlier. Using the STsync service request, a process can assign any combination of the six cache sections to the SMP and to the ACP. This allows the programmer to direct the SMP and ACP macros to simultaneously operate on the data cache. Calls are issued by the APCL coded process to SMP and ACP macros. Using these calls, the user is able to control the sequence of operations performed on application data.

To be debugged and executed, an ST-100 process must be called by a Fortran Call statement in the host application program. Specifically, the call is issued to an HPS. An HPS in turn directs loading of the process load module into the array processor and execution of the process via the APX. The HPS object module is generated automatically by the APCL compiler during compilation of the process object module. It remains, however, for users to link the HPS with their application programs, forming a complete application load module for execution on the host.

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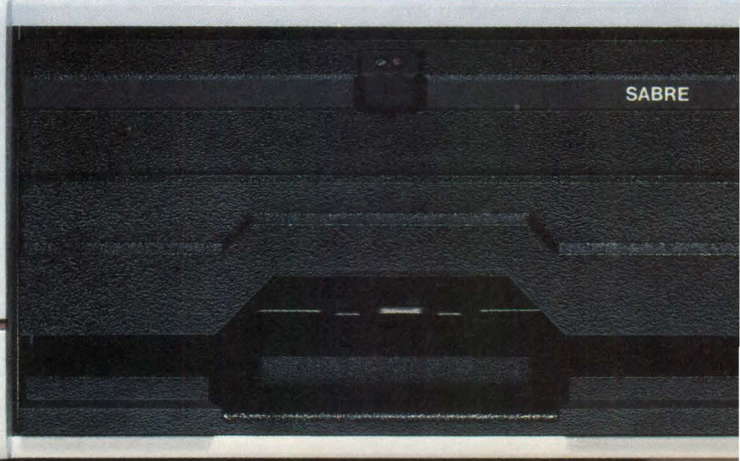

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CIRCLE 60

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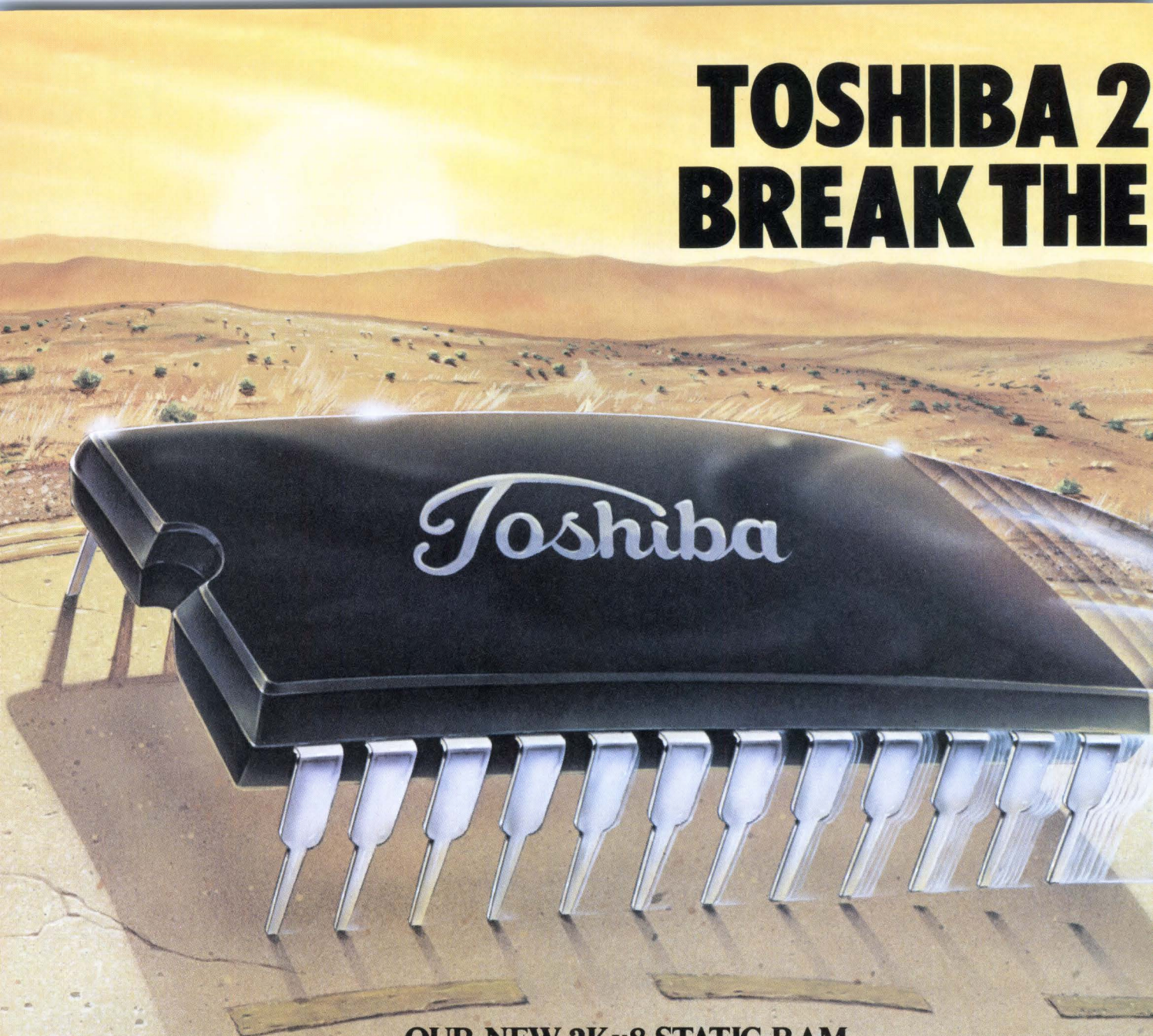

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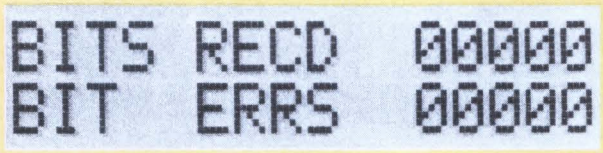

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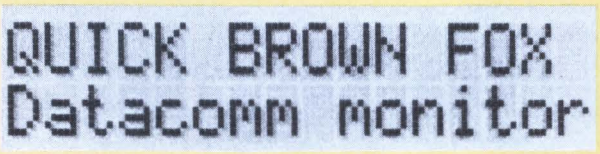

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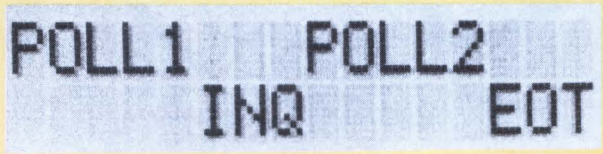

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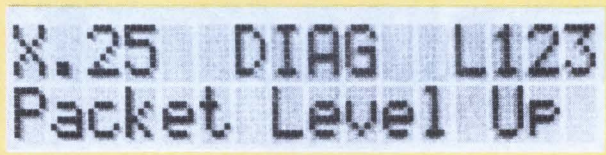

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CIRCLE 63

USING AN EFFICIENT MICROARCHITECTURE ACHIEVES GOALS

Careful microarchitecture planning enables design engineers to achieve dual goals of low cost and high performance in a 32-bit computer.

by Kenneth Burns and David M. Burns

A computer's architectural specification defines that machine on a functional level. As technology advances, the machine itself may change. But as long as it maintains the required relationship between input and output, it can be said to adhere to the architectural specification.

New generations of machines with the same architecture acquire different levels of price and performance by adding or deleting such performance accelerators as pipelining or cache. To help in the development of new models along the price/performance curve, design engineers use a software tool called a hardware simulator. By simulating the runtime environment of the proposed machine, designers can determine if the incremental performance gain is worth the additional hardware cost.

A machine's microarchitecture design requires similar trade-offs. An increase in microcode speed and flexibility usually means a commitment to a more costly design. Thus, the microarchitect's task is to design a microcode structure based on the proposed hardware design. This allows the machine to be positioned at its targeted level on the price/performance curve. A perfectly horizontal microword exists when every control line in the machine is associated with a bit in the microcode word. Once conceptualized, this initiates the design process. This structure offers the maximum amount of parallelism, and hence speed, which is available with a proposed set of hardware resources.

In reality, trade-offs are inevitable, since the hardware limits the amount of parallel processing possible within the machine. As the design process continues, the microcode structure moves toward a more vertical implementation. This means that a narrower microword can be used, resulting in a lower implementation cost.

Data General's recently introduced Eclipse MV/4000 system is a low cost, high performance implementation of the same MV architecture on which the Eclipse MV/8000 system is based. Although it was unnecessary to redesign a new functional instruction set, engineers faced several design challenges during the machine's development. An intitial constraint was that the entire CPU be contained on only two boards. This required the development of a highly efficient and flexible microarchitecture that produced optimum algorithm execution speeds.

The MV/4000 CPU (Fig 1) is a version of the company's 32-bit MV/family architecture. Although it has the functional ability of the higher performance

Kenneth Burns is senior development engineer at Data General Corp, 4400 Computer Dr, Westboro, MA 01581, where he is responsible for MV/Family microarchitecture design. He holds a BSE from the University of Connecticut in electrical engineering and computer science.

David M. Burns is currently sales engineer at Data General Corp; he was previously development engineer on the MV/8000. He holds a BSE in computer science and electrical engineering from the University of Connecticut.

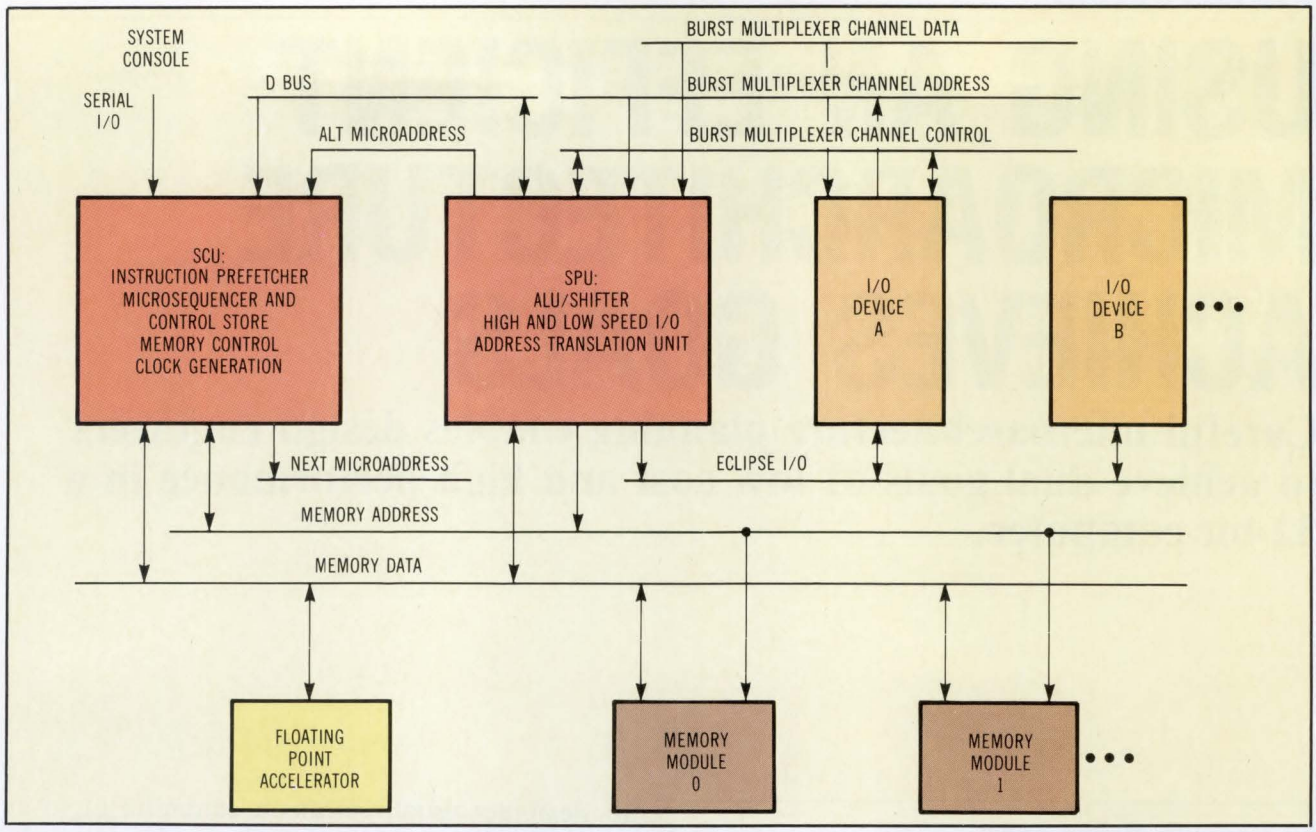


Fig 1 The Eclipse MV/4000 CPU is implemented in two boards, the system control unit (SCU) and the system processing unit (SPU).

MV/8000, the CPU board count was reduced from eight to two boards. This was made possible by using VLSI, gate array, and high speed Schottky technology, and by the definition of a highly compact and efficient microarchitecture.

The system control unit (SCU) in Fig 2 contains the instruction prefetcher, microsequencer and its associated control store, memory control, and clock generation logic. The instruction prefetcher consists of a three-level pipe that allows overlapped fetch and execution of instructions. The prefetch unit also generates the displacements used in memory reference address calculations. These displacements, together with the instruction predecode gate array and macroinstruction decode PROMs, form a starting microcode address that is sent to the microsequencer.

The microsequencer determines the order in which the vertical control store words are accessed and subsequently executed. A 9-bit field in the currently executing vertical microword determines the selection of the proper horizontal control word. At power-up time, and before the soft vertical control store has been loaded from system media, the microsequencer addresses a NOVA instruction set that is contained in kernel PROM. Using the I/O instructions contained in this kernel, the vertical control RAM is loaded with the full MV instruction set, and control is transferred to it.

Additional SCU logic performs error checking and correction on all memory accesses, and controls main memory refreshing. Hardware referenced and modified bits for each physical page are used by the AOS/VS operating system to support its page replacement algorithm.

How the system processing unit functions

The system processing unit (SPU) of Fig 3 performs all arithmetic and logical operations, both high and low speed I/O, and translates 32-bit logical addresses to physical memory addresses. Within it, a 32-bit ALU is responsible for all data manipulation. It contains eight 4-bit-slice ALU chips that are cascaded together to give full 32-bit capability. A separate nibble shifter allows for efficient data alignment. The ALU also contains the microcode visible register set (GR0 to GR7), user visible accumulators, wide stack pointer, and macro program counter (PC).

Data General's two standard I/O buses are implemented on the MV/4000. The low speed Eclipse data channel transfers data at 1.5 Mbytes/s, while the high speed burst multiplexer channel (BMC) performs block transfers at the rate of 5 Mbytes/s.

To implement full 32-bit virtual capabilities, the SPU contains logic that translates the 32-bit logical address to a 22-bit physical address. Using this address, the CPU can directly access the entire 8 Mbytes of physical memory.

To form the physical address, the logical address is taken from the ALU output (YBUS) and placed in the logical address register (LAR). This address is

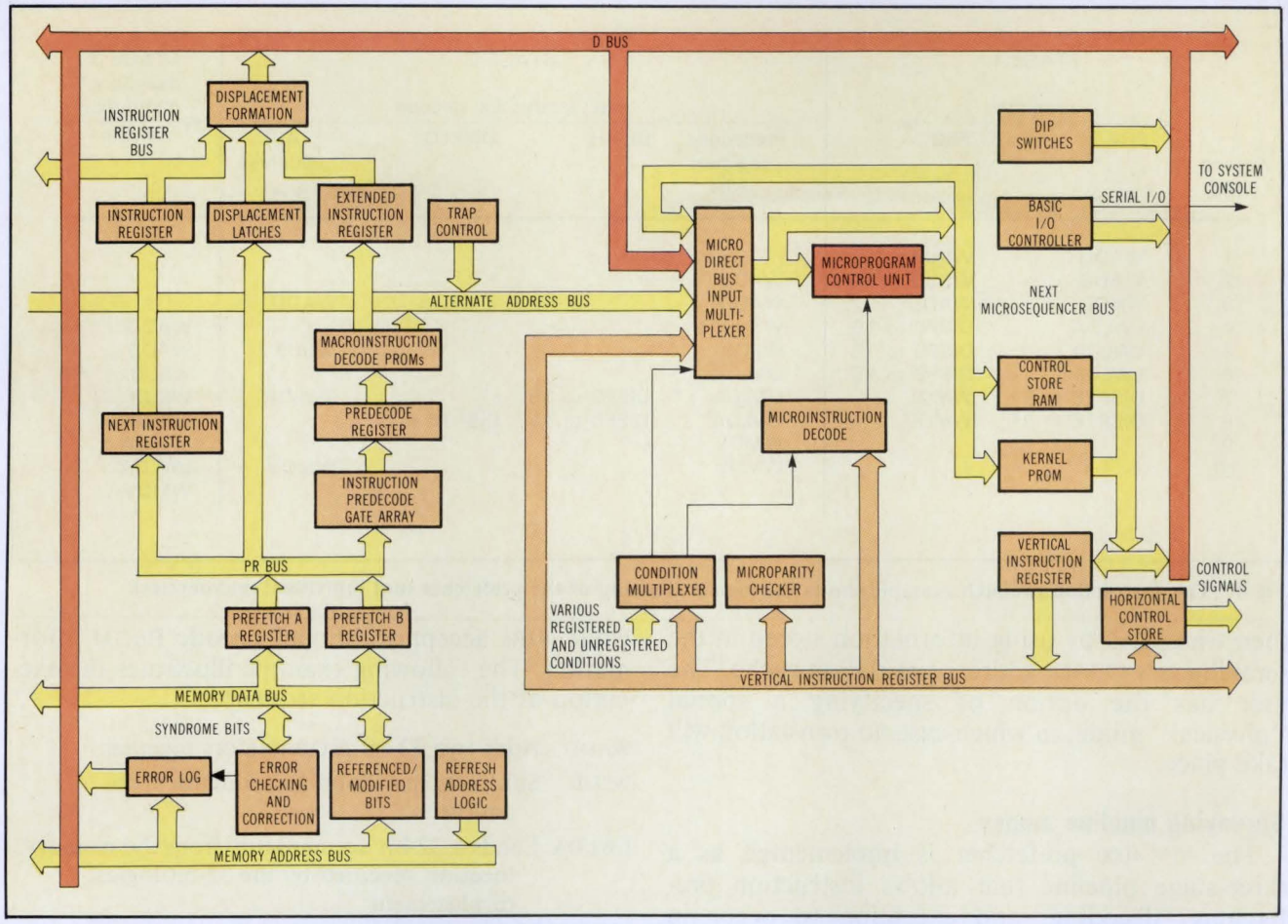


Fig 2 The MV/4000 system control unit performs instruction prefetch, microsequencing, memory control, and clock generation.

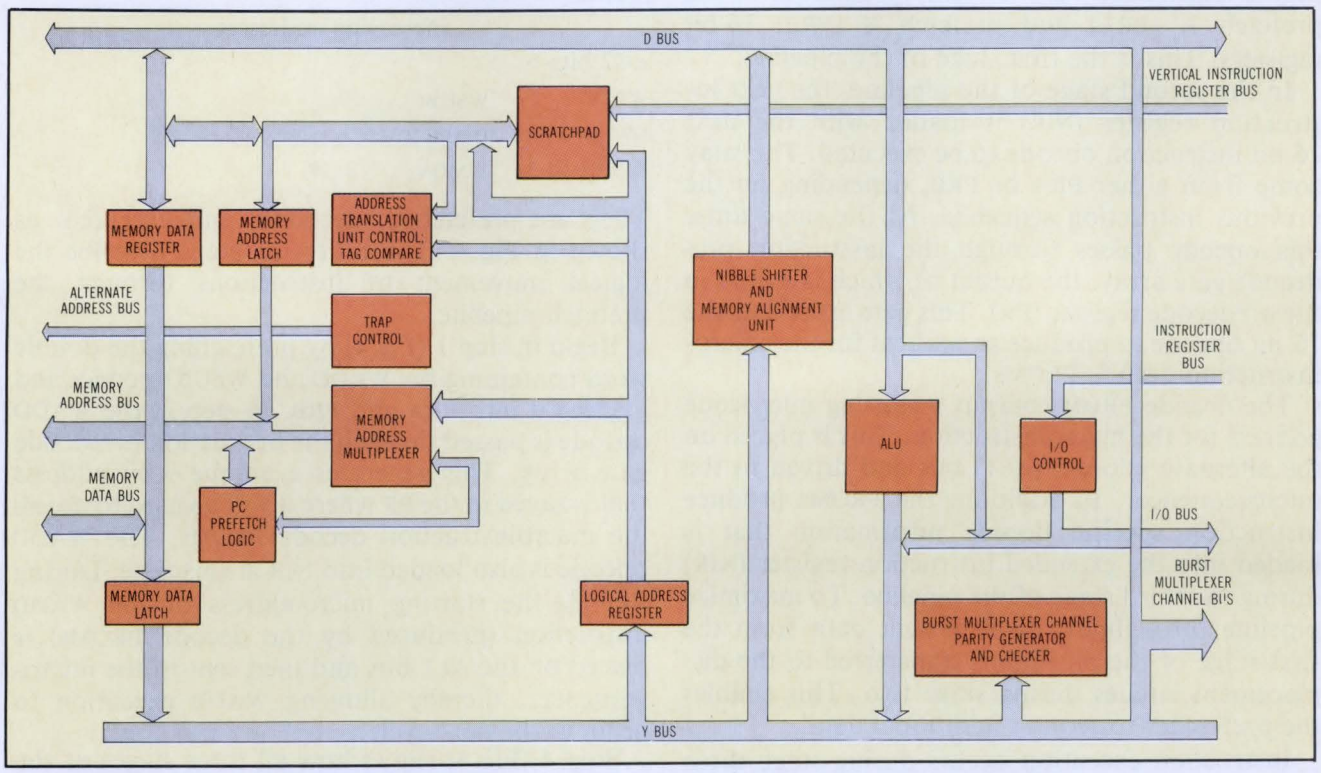


Fig 3 The MV/4000 system processing unit performs arithmetic and logical operations, I/O and address translation.

	STAGE 1		STAGE 2				STAGE 3
	prefetch		next instruction decode				executing instruction
μseq step	PRA	PRB	Predecode register, NIR	DISPHI	DISPLO	ALT μaddress	IR,XIR
1	WADD	WSUB	-	-	-	-	-
2	WADD	WSUB	WADD	-	-	-	-
3	WADD	WADD	WADD	-	-	WADD	-
4	LWLDA	DISP0 to 15	WSUB	-	-	-	WADD
5	LWLDA	DISP0 to 15	WSUB	-	-	WSUB	WADD
6	LWLDA	DISP0 to 15	LWLDA	-	-	-	WSUB
7	DISP16 to 31	WMOV	LWLDA	DISP0 to 15	-	LWLDA	WSUB
8	DISP16 to 31	WMOV	LWLDA	DISP0 to 15	DISP16 to 31	-	LWLDA
9	-	-	WMOV	-	-	-	LWLDA
10	-	-	WMOV	-	-	WMOV	LWLDA
11	-	-	-	-	-	-	WMOV

Fig 4 This instruction prefetch example shows the logical stepping of the prefetcher (not individual microcycles).

then translated by using information stored in the scratchpad's (SPAD) address translation cache. The user has the option of specifying a special "physical" mode, in which case no translation will take place.

Surveying pipeline stages

The MV/4000 prefetcher is implemented as a three-stage pipeline that allows instruction prefetching, decoding, and execution to occur in parallel. The PC prefetch logic on the SPU (Fig 3) initiates a double word (32-bit) read from memory that is transferred via the memory data bus to the prefetch A (PRA) and prefetch B (PRB) 16-bit registers. This is the first stage of the pipeline.

In the second stage of the pipeline, the next instruction register (NIR) is loaded with the next 16-bit instruction opcode to be executed. This may come from either PRA or PRB, depending on the previous instruction sequence. At the same time, this opcode passes through the instruction predecode gate array, the output of which is stored in the predecode register (PR). This gate array uses the 16-bit opcode to produce an address for the macroinstruction decode PROMs.

The decode PROMs output a starting microcode address for the macroinstruction. This is placed on the alternate address (ALT) bus and driven to the microsequencer. In addition, the PROMs produce instruction specific decode information that is loaded into the extended instruction register (XIR) during the third stage of the pipeline. To maximize pipeline throughput, displacement data from the first stage of the pipeline is transferred to the displacement latches during stage two. This enables the prefetcher to request additional data.

Instruction execution occurs during stage three of the pipeline. The instruction register (IR) is loaded with the instruction opcode saved in NIR, while XIRs accept additional decode PROM information. The following example illustrates the execution of the instruction sequence:

WADD Adds two 32-bit accumulators together

WSUB Subtracts one 32-bit accumulator from another

LWLDA Loads a 32-bit accumulator from the memory location specified by the 32-bit logical displacement

WMOV Moves one 32-bit accumulator to another

These instructions are stored in memory as shown below:

increasing addresses

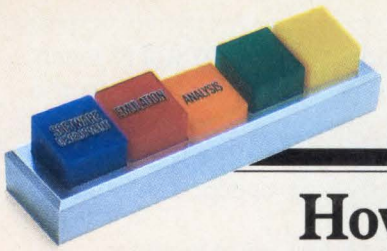
<-32 bits->

WADD	WSUB
LWLDA	DISP0 to 15
DISP16 to 31	WMOV

They are prefetched, decoded, and executed, as shown in Fig 4. The following steps describe the logical movement of instructions through the prefetch pipeline.

Begin in step 1 (Fig 4) by prefetching the double word containing the WADD and WSUB opcodes and loading it into PRA and PRB. In step 2, the WADD opcode is passed through the instruction predecode gate array. This generates a unique 9-bit address that is saved in the PR where it will be used to access the macroinstruction decode PROMs. The WADD opcode is also loaded into NIR at this time. During step 3, the starting microaddress of the WADD instruction (produced by the decode PROMs) is placed on the ALT bus and then sent to the microsequencer, thereby allowing WADD execution to begin in the next cycle.

Step 4 (Fig 4) shows how all three stages of the prefetch pipeline can advance simultaneously. Here, the IR is loaded with the WADD opcode,



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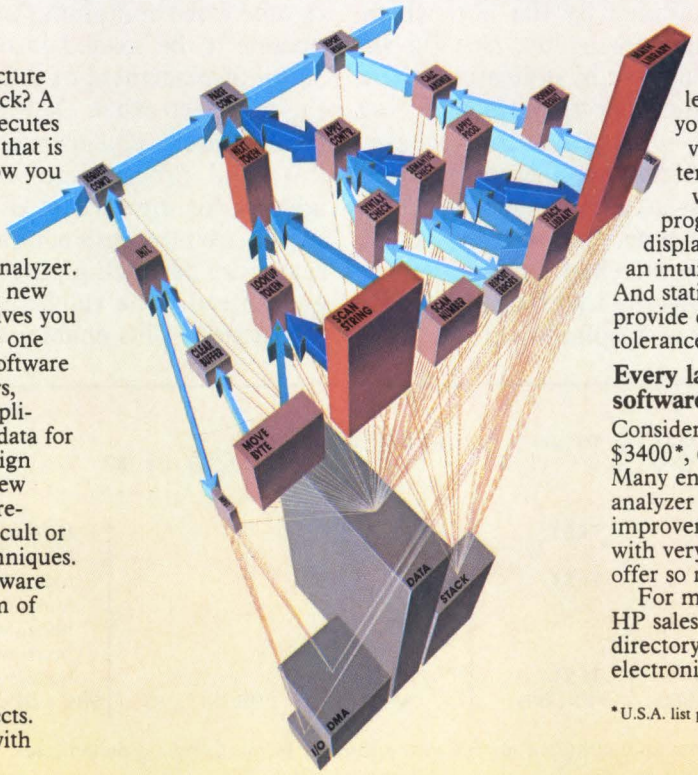

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while the XIR receives the instruction specific decode PROM information for WADD execution. At the same time, the WSUB opcode in PRB is driven through the instruction predecode gate array and loaded into the predecode register. The WSUB opcode in PRB advances to the next stage of the pipe and is saved in NIR. The prefetch logic, having detected that the WADD and WSUB opcodes are no longer needed in PRA and PRB, now proceeds to load the next double word from memory. This double word fetch is initiated by the SCU which starts the PC prefetch logic on the SPU (see Fig 3).

Microcode assists in this task by indicating to the prefetcher, via the instruction prefetcher GO (IPGO) random (Fig 5), when the currently executing instruction will be completed. Upon completion, the pipeline will advance, and since both PRA and PRB are free at this time, they will be loaded with the double word prefetched from memory. This double word contains the LWLDA opcode and its upper 16 bits of address displacement.

The starting microaddress for the WSUB is generated in step 5 and is sent via the ALT bus to the microsequencer. Since WSUB is now executing, and its opcode has advanced to the IR, the predecode register and NIR are free to accept the LWLDA information in step 6.

To allow the lower 16 bits of the LWLDA displacement (DISP16 to 31) to be fetched, the upper portion of the displacement (DISP0 to 15) is saved in the DISPHI latch during step 7. This permits the double word containing DISP16 to 31 and the WMOV opcode to be loaded into PRA and PRB. The full 32-bit displacement of the LWLDA will be formed in the next step when DISP16 to 31 is loaded into the DISPLO latch. The instruction prefetch logic detects this, and proceeds to drive the starting microaddress for the LWLDA over the ALT bus.

The LWLDA instruction executes in step 8. To maximize perfetch piping, the displacement is only guaranteed to be valid during the first cycle of the instruction. This enables DISPHI and DISPLO to be

Note: μF1 is always bits 0,1,2 and parity is in 31 even if not shown.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	to	31	
μF1																								#	
μF1			μF2								TEST							PA					horizontal		COND PA
μF1			μF2											AA									horizontal		UNCOND AA
μF1			μF2								TEST												horizontal		COND
μF1			μF2																				horizontal		UNCOND
μF1																							horizontal		NEXT
μF1			μF2															PA					horizontal		UNCOND PA
μF1											TEST							PA					horizontal		COND GOTO
μF1			BREG				AREG				ICI	BIN				MEM			DBUSI		G		SRC I OP I DES		VONLY

Note: μF1 and horizontal and parity are always in the formats of the following definitions.

																		SPAD 8							SPAD ADDR 8
																		Constant							Constant 8
			AREG																						AREG 1
					AREG																				AREG 2
															AREG										AREG 3
			BREG																						BREG 1
					BREG																				BREG 2
																		I BREG							BREG 3
												I OP													ALUOP 1
															MEM										MEM 1
																		DBUS							DBUS 1
																		DES							ALUD 1
																					C				CARRY 1
										I C															CARRY 2
												BIN I													BIN 1
																		NIBSC							NIBSC 1
														I	SRC										ALUS 1
						I NCU				I															SCU Control
														I G I											IPGO

Vertical only defaults:

a) YBUS= ALU
b) SPAD address control= address translation unit (ATU)
c) SPAD operation= read
d) NIBSC= align__d
e) SPAD address= ATU

Fig 5 A vertical field example shows vertical formats and usage.

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used in the next cycle in the event of back to back 32-bit memory reference instructions. Steps 9, 10, and 11, show the WMOV instruction as it advances through the instruction decode and execution stages of the pipeline.

Microinstruction flow

The MV/4000's microcode architecture was designed to allow the greatest degree of flexibility, and reduce the necessary control store width to allow a two-board implementation. Algorithmic speed was among the primary concerns of the microword architects. The chosen architecture takes into account the most common microcode operations, allowing them to be performed in one cycle.

To initiate the actual execution of a macroinstruction, a starting microcode address is driven from the prefetcher to the microsequencer via the ALT bus. Once there, it passes through the micro direct bus input multiplexer and enters the microprogram control unit. This address is then used to access vertical control store RAM, the output of which is registered in the vertical instruction register (VIR). Because a vertical microinstruction is associated with every microcycle, subsequent microaddresses for the executing macroinstruction are generated by the next address control (NAC) field contained within the vertical microinstruction.

The NAC field allows for conditional and unconditional sequencing. Conditional microsequencer functions are based on the results of a test selected by the vertical microword. On the other hand, unconditional operations will always be performed. Examples of microsequencer operations include jumps, subroutine calls and returns, 16-way calls, advancing to the next microaddress (NEXT), microstack push, and microstack pop. Many of these functions use the 16-level microstack because microaddresses can be saved on it.

The microword architecture selected for the MV/4000 consists of both vertical and horizontal control store (Fig 6). The power and flexibility of this architecture is due to the large amount of interaction between the two.

Vertical control store

Each vertical microword, except for the vertical only format, can specify any 1 of 512 horizontal microwords. The selected horizontal may in turn specify that certain bits of the vertical microword be used as control during the microcycle. In addition to selecting the horizontal, the vertical microword performs other functions such as determining which microsequencer operation is to be performed, supplying 1 of 128 possible test conditions, and supplying an absolute microaddress field. Thus, the microcoder logically sees the execution of a very powerful "functional" microword on every machine cycle. This functional microword consists

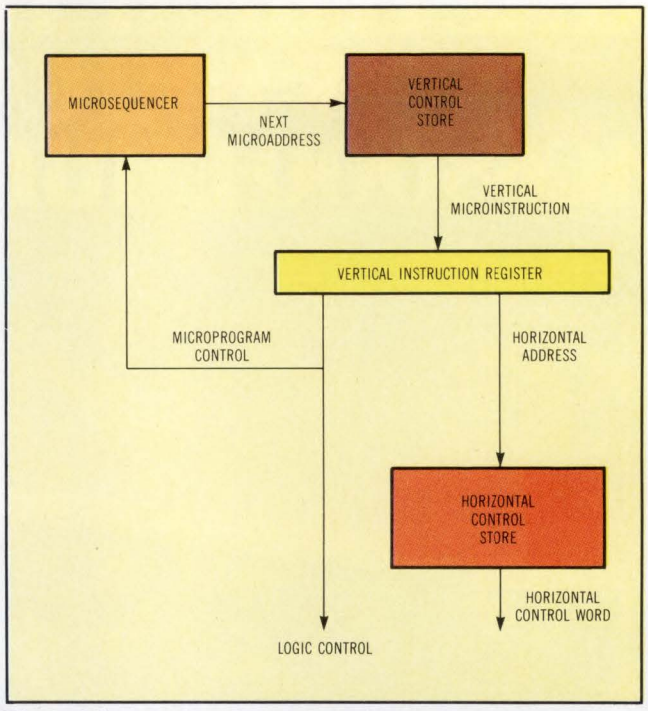

Fig 6 Microword architecture includes vertical and horizontal control stores.

of a combination of the selected horizontal along with certain vertical fields (vertical modifiers) specified by the horizontal.

The MV/4000 contains 16-K x 32 bits of vertical control store, thereby requiring a 14-bit address field for full access capability. In order to use fewer vertical bits to specify an address, microcode is broken into 256-word pages, requiring only an 8-bit page address (PA) for operations within the same page. The 6 page bits, maintained by the microsequencer, specify which of the 64 pages is currently being accessed. To change the current page of execution, a microsequencer format containing the full 14-bit address (AA) must be selected. Fig 5 shows all possibilities of vertical field usage.

The vertical control word is only 32 bits wide. Of these bits, 7 bits select the microsequencer function (μF1 and μF2), 1 bit is for parity (#), and 9 bits select 1 of the 512 horizontal control words, leaving 15 bits of vertical microword free to specify control These 15 free bits are often required to specify a TEST and NEXT PA, or to select a constant.

The horizontal can fill a field in one of two ways. It can specify the value for the field directly, or it can indicate which vertical control word bits will be used to control the field. Several of the fields have more than one possible vertical source. For example, Fig 5 shows that the ALU B register source (BREG) may come from one of three possible places in the vertical microword. BREG1 uses the vertical bits 3 to 6, BREG2 bits 7 to 10, and BREG3 bits 18 to 21, as the value for BREG. This 4-bit BREG value is used to select one of 16 possible microcode visible registers from the ALU register file. The horizontal may also specify that the BREG value must come directly

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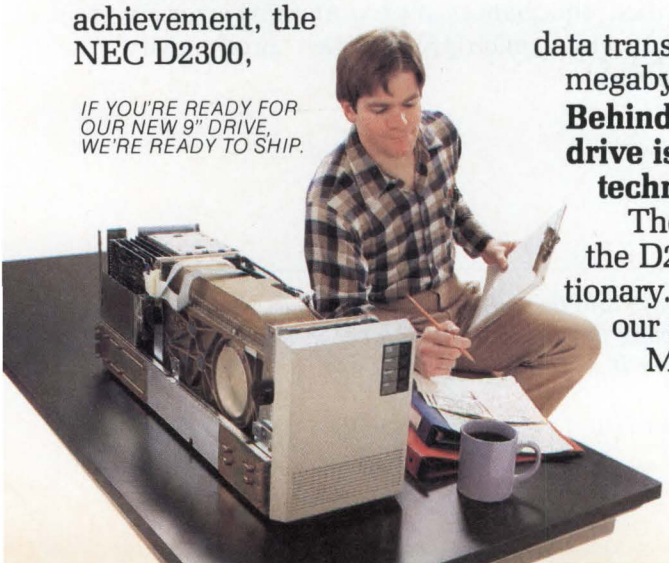

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from its own HREG field instead of using one of the three previously mentioned vertical fields. The horizontal's ability to select the control of a field from one of several vertical sources increases the microarchitecture's flexibility.

The final BREG select value is generated by the currently executing vertical microinstruction which selects 1 of 512 possible horizontals. The BREG field of the selected horizontal is then used to control the BREG MUX. This multiplexer allows one of four possible 4-bit BREG sources (horizontal HREG value, V18 to 21, V7 to 10, or V3 to 6) to be chosen as the ALU B register address. The selected 32-bit register is then used as the input to the ALU's B side.

Specific vertical bits can often be used to control more than one portion of the machine. For example, Fig 5 shows that vertical bits 18 to 21 can be used to specify an ALU B source (BREG), DBUS control, ALU destination (DES) and ALU carry input (C), or nibble shifter control (NIBSC). One of the constraints placed on the microcoder is that it must be aware of all possible combinations of vertical fields allowed. In most cases this can be overcome by permitting the horizontal to be the source for some of the control. This is not always possible, however, due to the limited number of horizontals.

Although control sourcing several fields from the same vertical bits may seem a constraint, it actually allows more combinations of fields to be specified than would be possible if these bits were only used to control a single field. To take advantage of this "microfield multiplexing" capability, the majority of horizontals were designed to be as general as possible. This means that they choose to use a large number of vertical modifiers, enabling a small group or horizontals to handle most operations.

Examining vertical field usage

Another way of controlling the machine is called vertical only. This method does not require a horizontal to be specified, thus allowing 9 more bits of vertical control. Vertical only is used whenever the next microaddress can be derived from the current microsequencer state. Examples include situations where control proceeds directly to the next microaddress, and operations such as popping the microstack on microcode subroutine returns. The vertical only word is designed to be the most general word available to the microcoder. It allows for complete control of the ALU and memory. Associated with the vertical only field are several default values for fields not specified by the vertical only microword.

To further illustrate vertical field usage we will examine all microsequencer functions that have an impact on BREG selection (see Fig 5). If μF1 contains the NEXT encoding, then vertical bits 3 to 21 are all free to be selected by various fields in the horizontal. This means that the horizontal may select either BREG1, BREG2, or BREG3. Of course, the horizontal is always free to specify BREG directly through the use of its HREG field.

When a conditional microsequencer function is specified that does not require an address field (see Fig 5, COND), then vertical bits 14 to 21 become available. Such a case is the conditional return operation where the desired address has been previously stored on the microstack. This allows the use of vertical bits 18 to 21 (BREG3) or HREG from the horizontal to specify BREG.

UNCOND PA is an unconditional microsequencer operation that specifies a microcode address. This format allows vertical bits 7 to 10 (BREG2) to be used for BREG specification. The horizontal HREG field is also available.

If a conditional goto (COND GOTO) is coded into the μF1 field, then only vertical bits 3 to 6 (BREG1) are available for selection by the horizontal. Vertical bits 7 to 10 (BREG2) and 18 to 21 (BREG3) cannot be chosen because these fields are occupied by TEST and PA, respectively. Again, the HREG field of the horizontal may also be used as the BREG value.

An unconditional subroutine call must use the UNCOND AA format to specify a new 15-bit microaddress (AA). This means that no vertical bits are available to specify BREG, leaving only the HREG field of the horizontal to supply the BREG value. If a horizontal is not needed, the vertical only (VONLY) format may directly select BREG from vertical bits 3 to 6.

The MV/4000 microcode is written in a high level register transfer language developed solely for the machine. Earlier microcode languages used a fixed format input in which every field required a mnemonic to be entered for proper input to the microassembler. In contrast, the MV/4000 uses a free form input to its microassembler that enables the microcoder to input high level language statements that are logically equivalent to the desired hardware function. Since unused fields need not be specified, the chances of programming error are reduced while microprogrammer productivity is increased.

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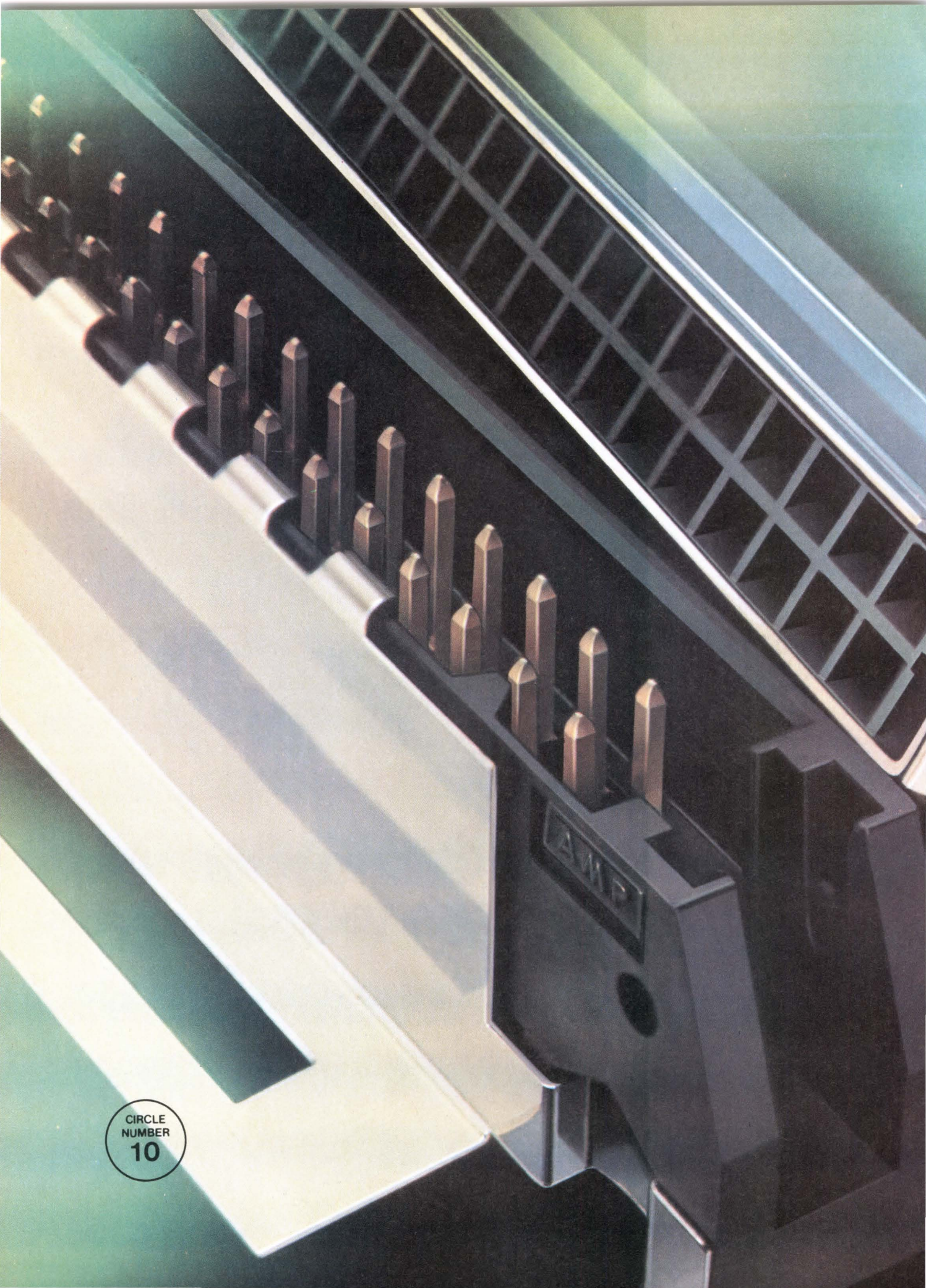

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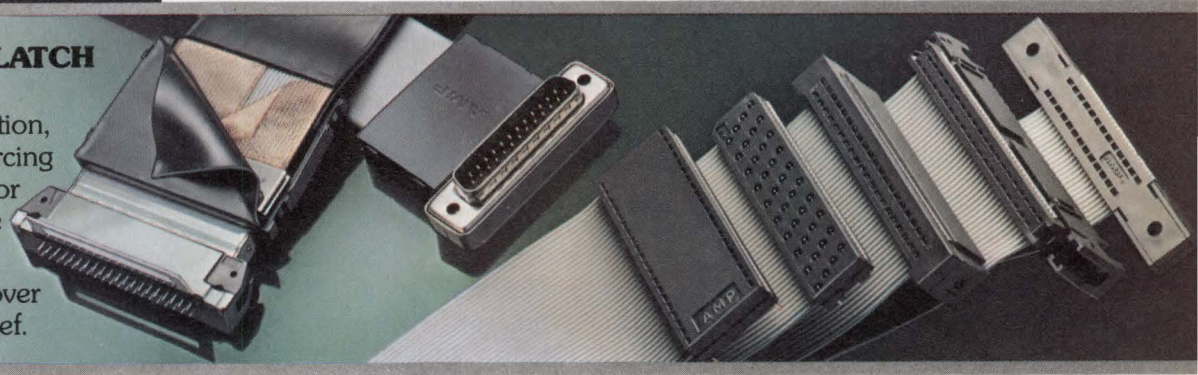

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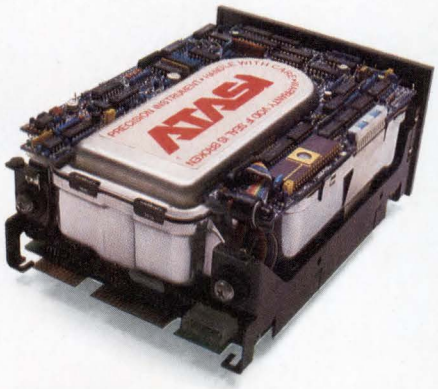
AN ENVIRONMENTAL IMPACT REPORT.

drive's head to "slap" against the disk, removing a "divot" of oxide material, along with the data written there. Severe vibration can cause the head to overshoot or undershoot a track, so that the head can't find the data it's seeking. In addition, vibration can fatigue components over time, and perhaps lead to premature failure.

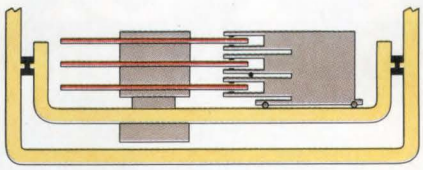


ATASI's 46 Mbyte, 5¼-inch Winchester disk drives are available in production quantities immediately.

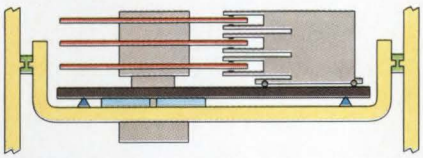
Double shock isolation

In order to sustain high shock loads, the ATASI design incorporates a unique dual system for shock and vibration isolation. Like most disk drives, ATASI drives have isolators between the frame and the head/disk assembly bowl. In addition, ATASI's proprietary design includes elastomere isolators inside the bowl, between the bowl and baseplate on which the head/disk assembly is mounted. A foam pad with high damping properties, also located between the baseplate and the bowl, further protects the head/disk assembly from vibration.

The grommets ATASI uses for isolators are far from ordinary. To handle both pulse shocks and vibration effectively—to avoid a declining spring rate with displacement while maintaining adequate damping properties—ATASI tested 330 different options before making a choice. These tests involved the use of a laboratory shaker as well as computer models.



Most disk drives only have shock and vibration grommets (black) between the frame and the bowl.



ATASI's proprietary design also includes isolators (blue) between the bowl and baseplate.

ATASI's double isolation system more than protects its drives—and the data they store—from the shocks of the office environment.

Beyond the shock/vibration problem

Shock and vibration engineering is only one of a number of ways ATASI achieves such a high level of data integrity. ATASI drives also feature dedicated "landing zones." Upon powerdown—intentional or emergency—the back e.m.f. of the motor is used to position the carriage over data-free landing zones. A carriage lock then mechanically holds the carriage in place, protecting the data field from any head contact.

The ATASI White Paper

At ATASI, we are proud of the quality we build into every drive we make, and we encourage clients to test our products rigorously. To help, we have prepared a White Paper on shock and vibration for systems integrators. It discusses test methods and the interpretation of test data in detail.

If you are a systems integrator, contact ATASI Corporation now to receive your ATASI White Paper. Corporate headquarters: 2075 Zanker Road, San Jose, CA 95131, (408) 995-0335; Eastern region: (617) 890-3890; Southwest region: (714) 432-0757.

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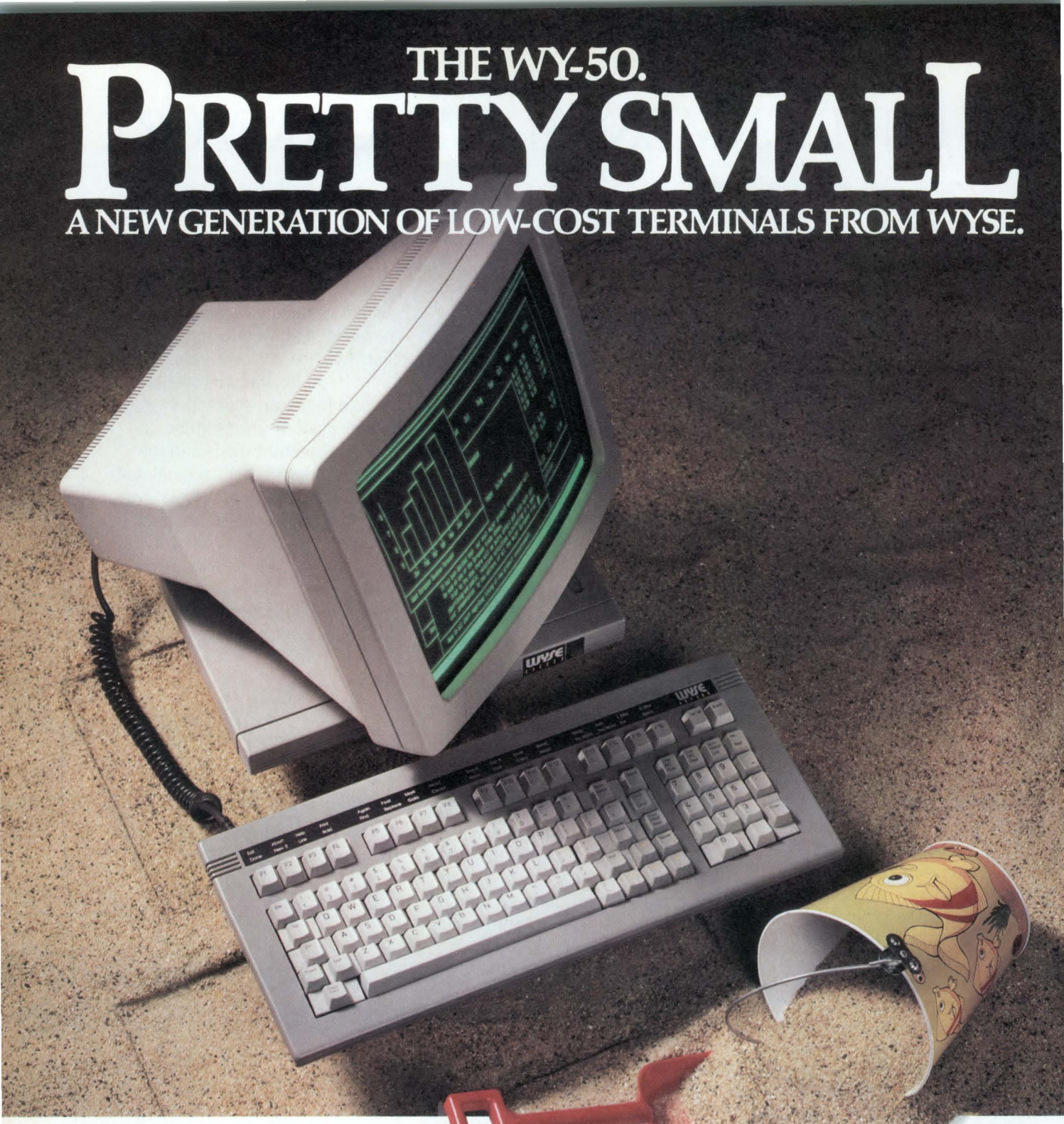

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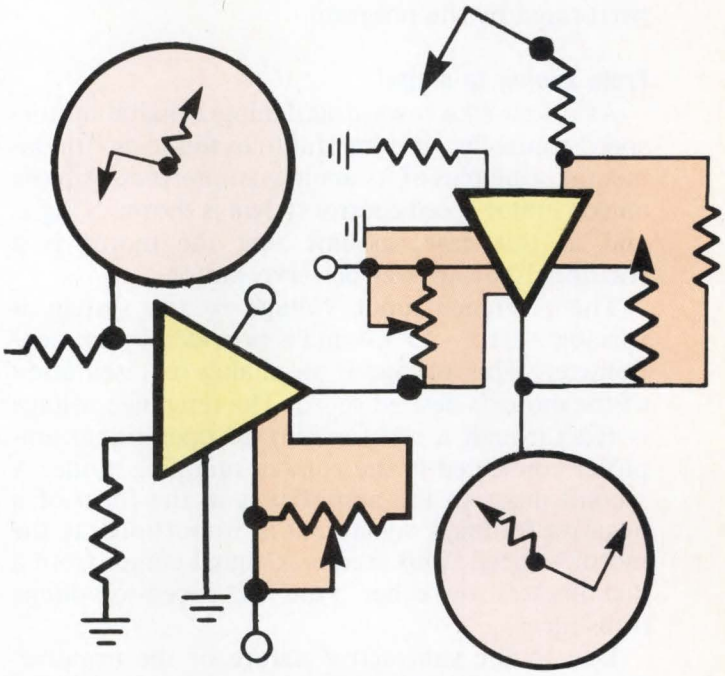
CIRCLE 69

MOTOR CONTROL SYSTEM DESIGN HINGES ON PROCESSOR DELAYS

Microprocessors are a boon to motor-speed controllers, but certain limitations of the devices must be accounted for in system designs.



by Manuel R. Cereijo

Although microprocessor-based control systems are quickly overtaking analog controllers, designers must understand that using a microprocessor does not remedy all design problems. In fact, in realtime systems, time delays in microprocessor execution can significantly affect system response. For example, in digital motor-speed control applications, execution speed can be relatively slow, putting an inherent upper limit on the sampling rate. Another limitation of a microprocessor is finite word length. If a processor handles only 8 bits, resolution is limited to 256 discrete outputs.

Before undertaking the design of a complex system such as a digital motor-speed controller, a prudent designer should be aware of the types of problems usually encountered. In the matter of time delays, two factors stand out. The first is long delays; if they are too lengthy, there is insufficient time to carry out the computations necessary to execute the control algorithm. The second is the adverse effect that delays have on the stability of closed-loop systems.

Time delays resulting from microprocessor computation can be identified by analyzing both the program for the control routine and any subroutines called from utility packages. Each of these programs are composed of an instruction set, and each requires a specific number of machine (microprocessor) cycles to execute. In turn, each machine cycle requires a known number of machine states. The time needed for a processor to execute a particular instruction is directly proportional to the number of machine states used to complete the instruction. For example, typical machine state time in many current microprocessors is in the range of 500 ns. While this appears adequate to handle most control applications, it should be understood that even a simple program may require thousands of machine states to execute.

The Table gives the amount of time consumed executing the types of instructions found in many control systems. The execution times given are based on a 500-ns machine state time. If instruction combinations that make up a program are totaled, a

Manuel R. Cereijo is associate dean for the College of Technology, School of Engineering, at Florida International University, Tamiami Campus, Miami, FL 33199. Dr Cereijo holds a DSC from Universidad Central, Cuba, and an MSEE from the Georgia Institute of Technology.

Typical microprocessor execution times	
Task	Time required
Floating point addition	18.5 to 202.5 μs
Floating point multiplication	63.5 to 446.0 μs
Floating point to fixed point conversion	25.0 to 109.0 μs

control algorithm can take anywhere from 2 to 5 ms to execute completely. Obviously, execution time varies according to the processor and the program. A designer must come up with a good estimate of the minimum and maximum delay times for the system. Such information is available in the microprocessor's user manual, and this allows a designer to calculate the total number of machine states to execute a program, or to determine the time required to reach a specific point in any computation performed by the program.

From analog to digital

As a first step toward designing a digital motor-speed controller, it is helpful to examine the fundamental principles of its analog counterpart. A basic analog motor-speed control system is shown in Fig 1, and in this case, assume that the motor is a fractional-horsepower dc servo motor.

The reference input voltage to the system is variable—0 to −15 V—and is provided by a potentiometer. This voltage is an analog representation of the motor's desired speed. The reference voltage is fed through a resistor into an operational amplifier connected in the voltage-summing mode. A second input to the amplifier is in the form of a negative feedback signal that is proportional to the motor's speed. This feedback signal comes from a tachometer, or other type of speed-to-voltage transducer.

Due to the subtractive nature of the negative-feedback signal, the system is stable. The output

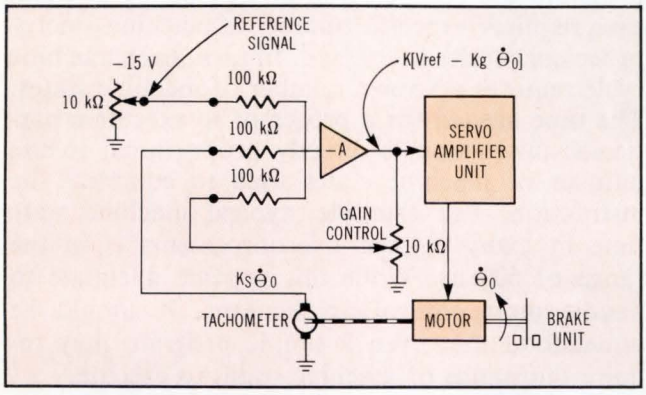


Fig 1 A basic analog motor speed-control system uses an operational amplifier connected in the voltage-summing mode to compare a feedback signal with a reference signal. This system can be connected to a digital controller to provide computer control of the motor's speed.

voltage of the operational amplifier, called the error signal, is the difference between the reference and feedback voltages and drives the servo amplifier unit in Fig 1. In addition, the output of the servo amplifier drives the servo motor to the desired speed. A third input to the operational amplifier summing-network, the gain-control potentiometer, is provided to increase the system's sensitivity and power transfer.

The servo motor is powered by a transistor amplifier within the servo amplifier unit. Current can be supplied to either the field or armature windings of the motor, but the most accurate control results from an armature connection. The tachometer or tachogenerator connected to the motor shaft generates a voltage proportional to the speed of the shaft multiplied by a tachometer constant. In this case, the constant is determined experimentally and equals 2.55 V/1000 rpm. Thus, when the motor shaft spins at 1000 rpm, the tachometer generates 2.55 V. This voltage is subtracted from the reference voltage at the summing junction.

An analog system of this type can be adapted to digital control techniques by digitizing the voltage variations and writing the feedback loop in software. Digitizing the control voltages involves the design of a control interface whose software is available in a number of different forms. The software's function is to successively compare the feedback and reference signals and generate a compensation signal to the motor-drive circuitry.

Digitized voltage and software feedback loops convert some analog systems to digital control.

If the control system is simple, machine language programming may be adequate. However, a user should be aware that problems can arise in writing and debugging the program, and that modifications to the program can be difficult. In most cases, it is wiser to rely on high level language (Basic, Pascal, etc) programming since it permits more attention to be given to control operations rather than causing concern about the information flow in the processor's registers and internal memory.

Converting voltage values

To digitize control-system feedback signals, an A-D converter of the type shown in Fig 2 is used. The converter, a Teledyne 8703, is a dual-slope type. A low logic-level on the Enable input line activates the device and a positive-going pulse on the Initiate Conversion line starts A-D conversions. The analog input voltage to be converted is applied to the 8703's V_{in} line.

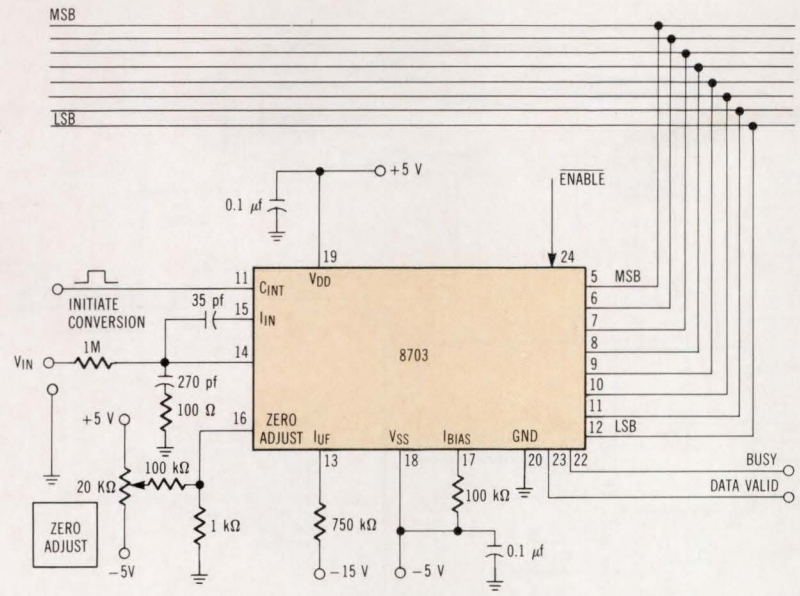


Fig 2 Data conversion is one of the operations that must be performed when an analog speed-control system is to be controlled by a microprocessor. An A-D converter of the type shown here converts the analog representation of the reference signal into a digital value for use by the microprocessor.

The converter contains a zero-adjust terminal that connects through a fixed resistor to a potentiometer. This permits a user to adjust the converter output to 0 V when a 0-V signal is present at the analog input. The I_{Bias} input serves to establish the bias current for the converter's internal circuitry. With a reference voltage of -15 V and a 750 kΩ current-limiting resistor, the maximum current that can be drawn by the chip during a conversion is a $-20\ \mu A$. The eight output lines of the converter connect to the control system data bus, which feeds, in turn, into a system I/O port.

Fig 3 illustrates the control system's (D-A) conversion system, centered around the DAC-100 D-A chip. Internally, the DAC-100 has a series of current switches that are activated by data on the data bus. The current switches are connected to a highly accurate and stable R2R resistor ladder network. It is this internal resistor network that forms the basis of D-A conversions. A potentiometer connected between -15 V and the converter's full-scale adjust terminals permits a user to obtain a 0-V output for an all-logic 0 input.

The converter's output feeds into an AD 118A operational amplifier. This device is chosen for its accuracy, response, and fast slew-rate characteristics. Slew rate, in particular, is important because the input to the amplifier often changes at a fast rate. For the 118A, the slew rate is $6V/\mu s$—the output signal switches at a rate of 6 V in 1 μs. The

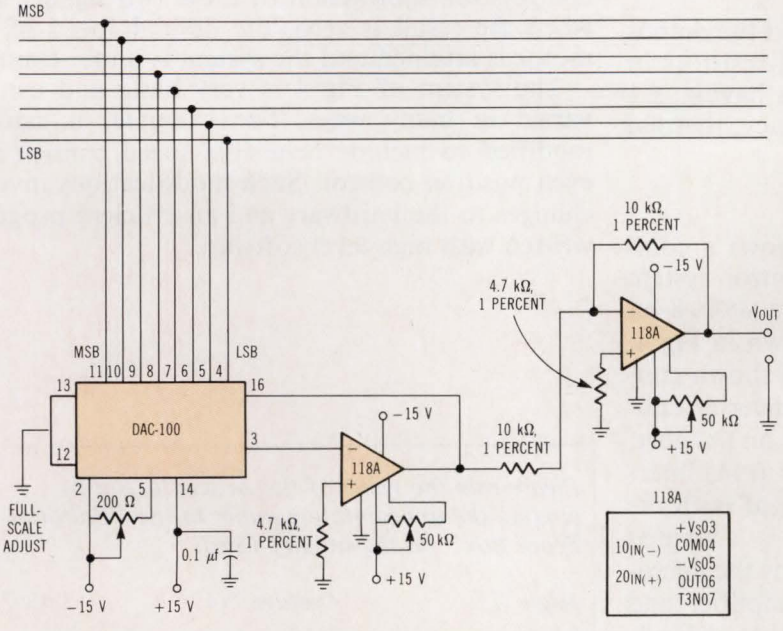


Fig 3 To drive the system servomotor, digital signals must be converted into analog values by a D-A converter subsystem. The converter, a DAC-100, is activated by digital signals on the data bus.

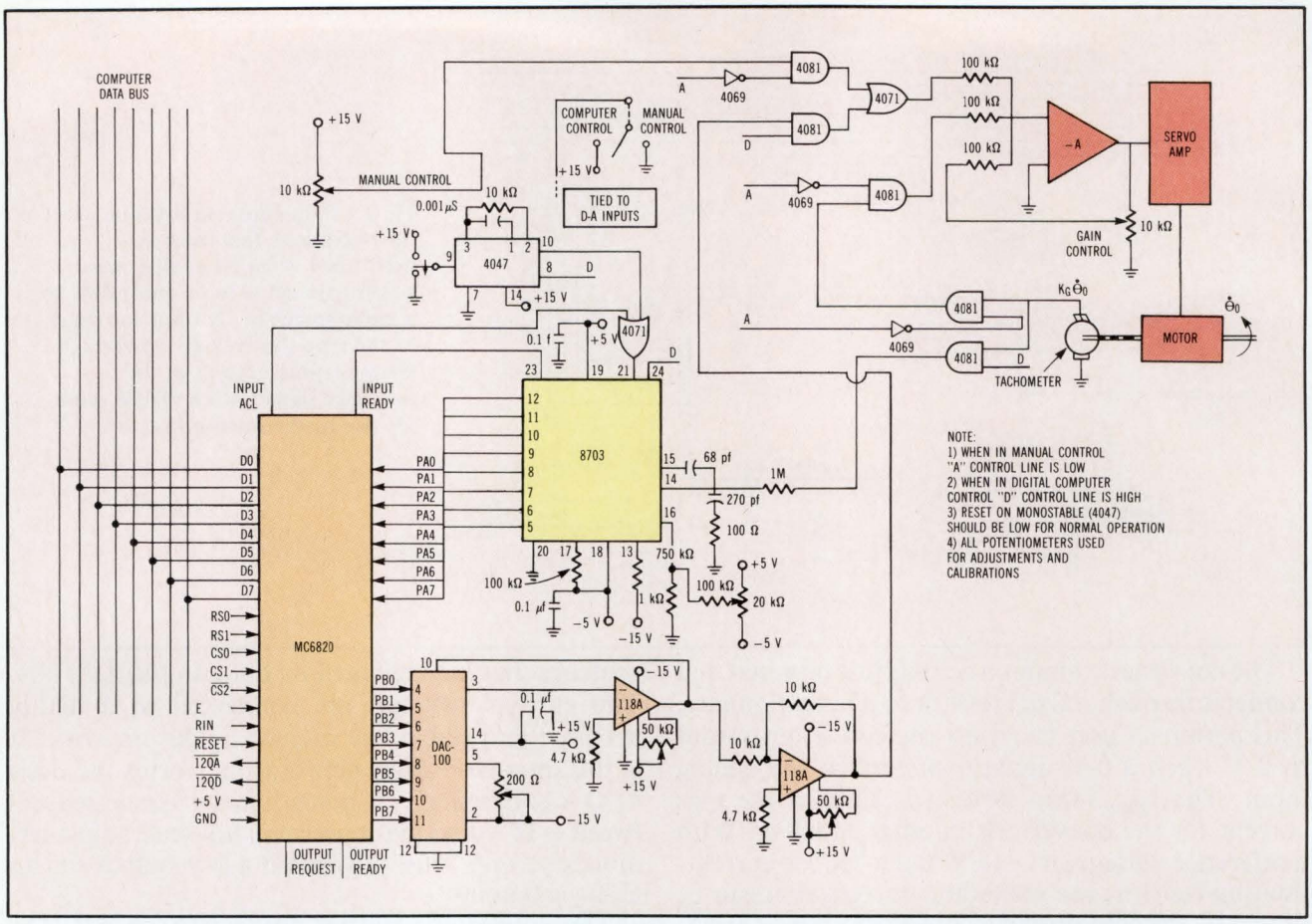


Fig 4 A complete digital motor-speed controller—not including the controlling microprocessor—incorporates the circuitry of Figs 1, 2, and 3. The converters and motor-drive circuits interface to the microprocessor through a peripheral interface adapter—the MC6820.

amplifier also provides excellent thermal stability. Another trimming adjustment is included on the amplifier to allow the output signal of the D-A system to be set to 0 V when the input to the system is found to be 0 V.

A second AD 118A is included to invert the output of the first operational amplifier. All resistors in the system should be metal-film types having ±1 percent tolerance to ensure high accuracy, thermal stability, and low noise generation.

A complete speed controller

The schematic diagram of Fig 4 shows a complete microprocessor-based speed control system whose computing element is a Motorola M6800 8-bit microprocessor. The M6800 is not shown in Fig 4, but its interface device, the MC6820, is shown connecting to both the A-D and D-A converter subsystems of Figs 2 and 3 respectively. As an I/O port, the M6820 peripheral interface adapter (PIA) interfaces the system data bus to the buses of both the A-D and D-A converters. The PIA is activated through a series of control signals sent by the microprocessor. Note that the summing amplifier and servo amplifier circuitry is the same as that of Fig 1.

The reference signal to the controller comes from an external source such as a keyboard. However, the feedback signal is available at the output of the A-D converter. The system software controls the subtraction of these two signals, and when the result is zero, the desired speed of the motor is attained and the system is under control.

The system of Fig 4 is very basic and can be varied in many ways. For example, it can be modified to include reversible speed control and even position control. Such modifications involve changes to the hardware and an efficient program written with high level software.

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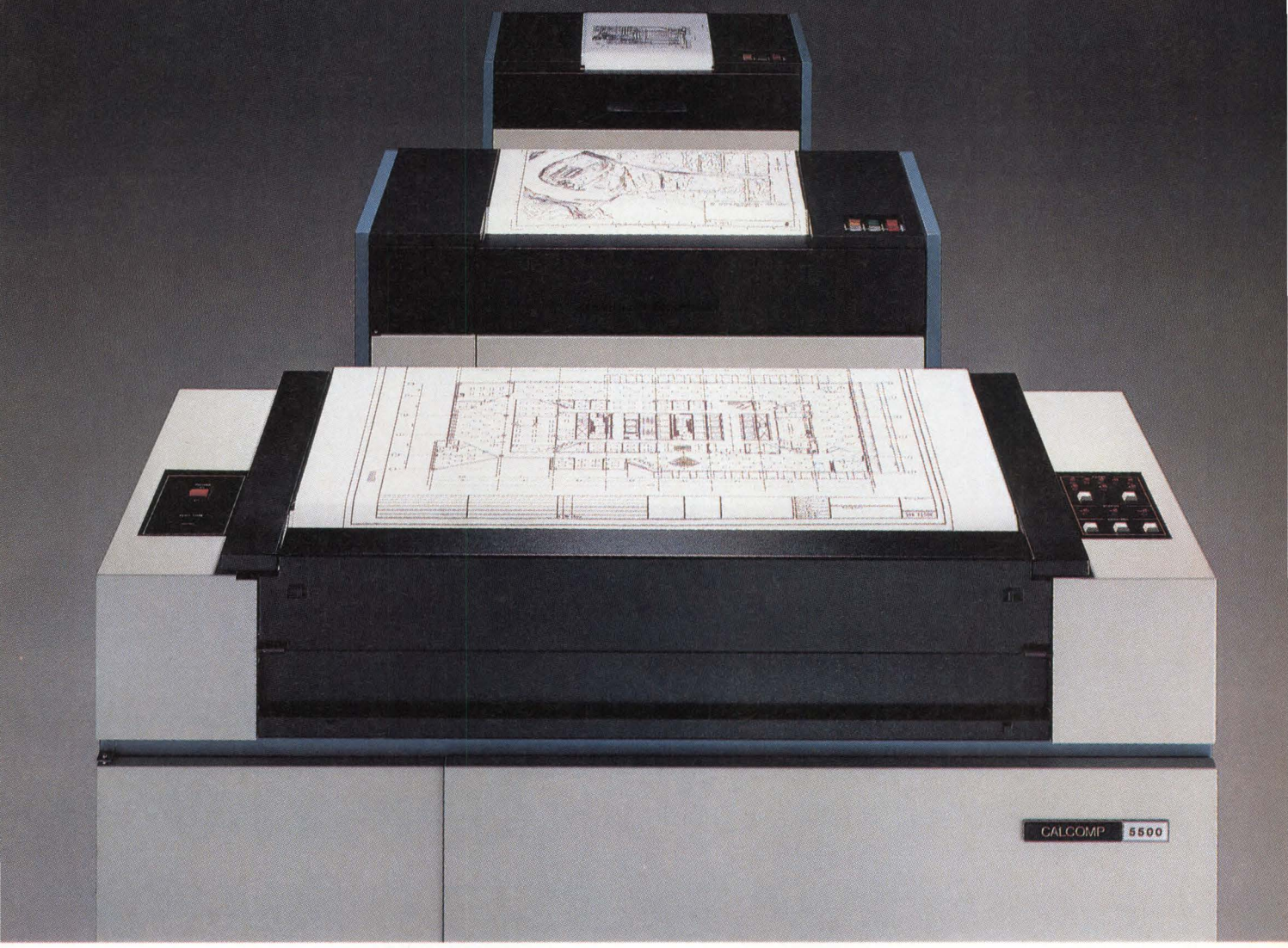

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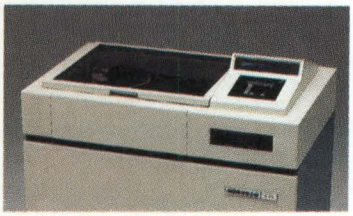

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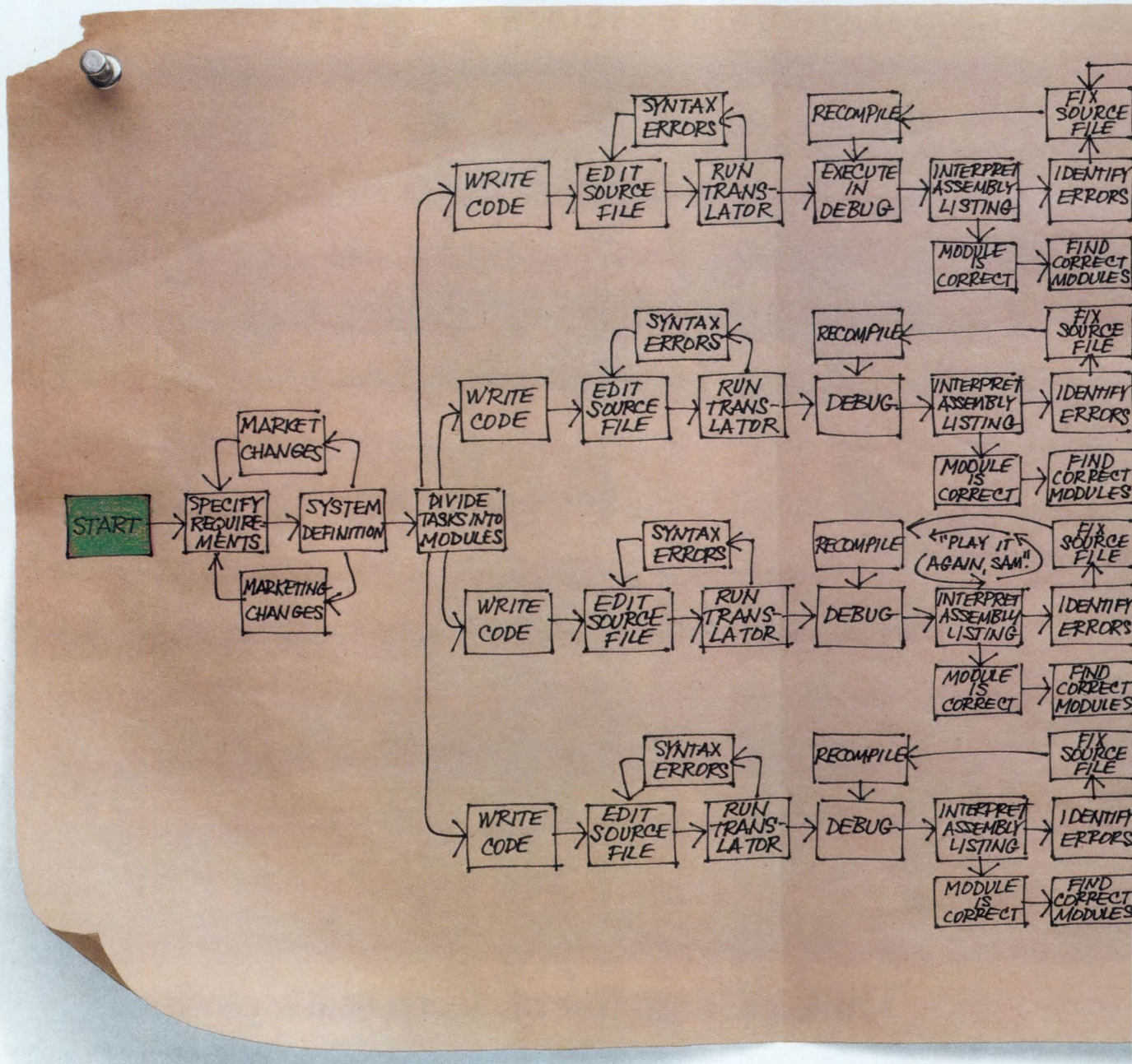
CIRCLE 70

WHOEVER FINIS



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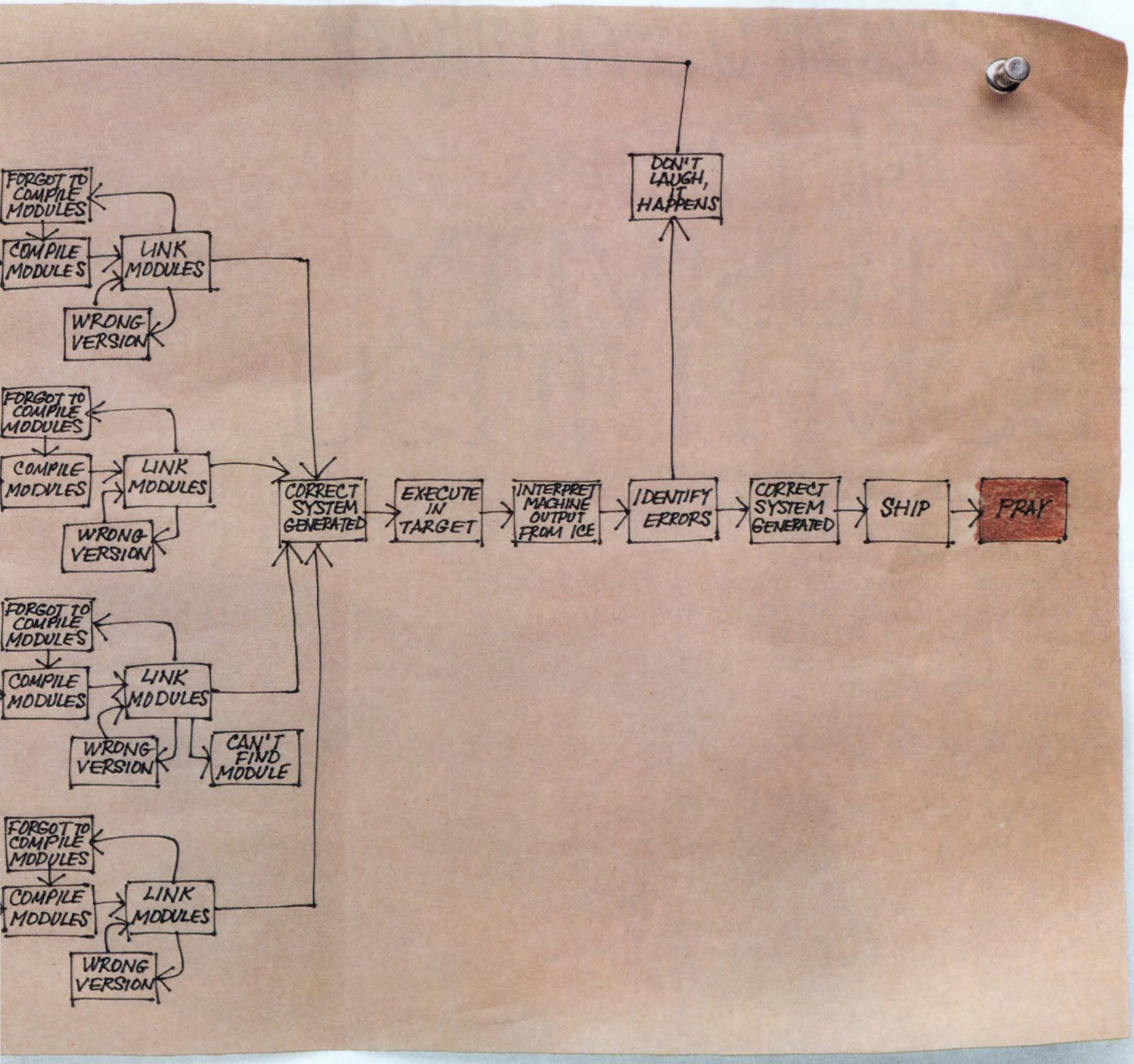

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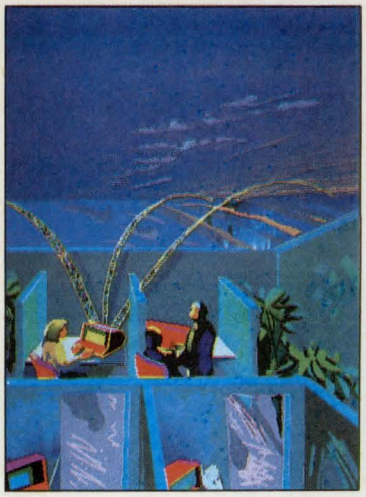

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CIRCLE 73

SPECIAL REPORT ON DATA COMMUNICATIONS

To switch or not to switch, that is this year's choice for the computer designer. Is a digital private branch exchange (PBX) really needed to switch data and voice throughout a facility, or does a local area network (LAN) suffice for today's communication needs? The answer, of course, depends on the individual need. More and more applications require communication of both high speed data and digital voice and, in some cases, even digitized video. These applications necessitate handling a large amount of data and currently are being wooed by both LAN and PBX vendors, each of whom claim to provide the "total" solution to short-distance communication needs.

A good amount of this short-haul communication technology is being geared for offices where some kind of PBX already routes telephone traffic. Now that switching technology has graduated its third generation, a new breed of voice/data digital PBXs—the fourth generation—is starting to be launched to effectively compete with LANs for office applications.

This special report examines the technology behind the upcoming fourth-generation PBXs while highlighting the major trade-offs among various media access contention schemes used by major vendors, including IBM and AT&T Information Systems. In addition, the report details a typical fourth-generation digital PBX to reveal a natural merging of LAN technology in a PBX configuration. Finally, the report reviews the latest trends in LAN developments.

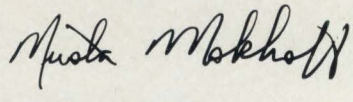
Five articles that are variations on the PBX/LAN theme complement the report. The engineers of four established semiconductor companies and a startup venture present the scope of state-of-the-art developments. David Berry of Advanced Micro Devices reviews standards for protocols needed to communicate between different terminals that use the Open Systems Interconnection (OSI) model. He reviews the ongoing protocol standardization efforts of various organizations for the upper levels of the OSI model.

Two authors from Motorola, Henry Wurzburg and Steve Kelley, show how a digital PBX can be transformed into a LAN by using a universal digital loop chip set. The allotted 64-kbit/s data rate adequately meets the effective 40-kbit/s data rate of current LANs when these are fully loaded, and does so at a lower cost per connection, according to the two authors. Signetics' three authors—Joonees Chay, Jeff Seltzer, and Naseer Siddique—propose to link Ethernets that use a CSMA/CD contention scheme with token-bus networks that use a token to get on the bus. Their gateway controller chip set, in theory, allows Ethernet-based offices to talk to realtime response token-bus LANs in factories.

As more Ethernets are installed and more users gain access to Ethernet media, more intelligence must be added to the nodes to contend with the added data congestion. Mostek's James A. Fontaine offers a solution to the congestion problem that combines a 16-bit microcomputer with an Ethernet controller chip to form a smart node.

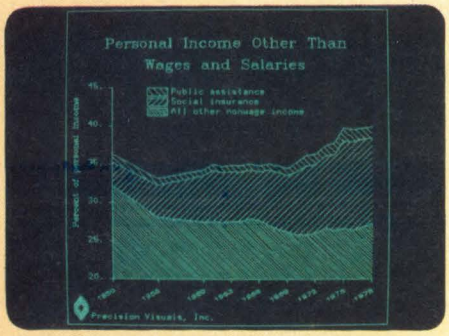
Local intelligence by itself can be a self-defeating goal if the processed information stays within the confines of that terminal. As IBM PCs spring up wherever the appetite for data warrants them, microcomputers must be linked to mainframes to become effective corporate team players. As such, the latest trend for some startup companies is to develop the tools for the micro-to-mainframe link. Forte Data Systems' Dan Erlin is one such entrepreneur who discusses his product—an IBM PC plug-in board and associated software—which links the PC, operating as an IBM 3270-type terminal, directly to a mainframe via a serial RS-232 coaxial cable.

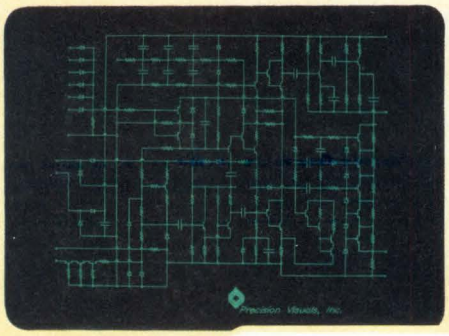
Thus, from the highest levels of protocol to the lowest wired connections comes a myriad of communication challenges for the computer designer to solve. Now is the time to meet these challenges by choosing from the crop of communication technologies becoming available.

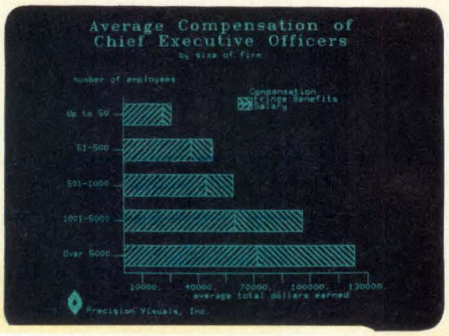


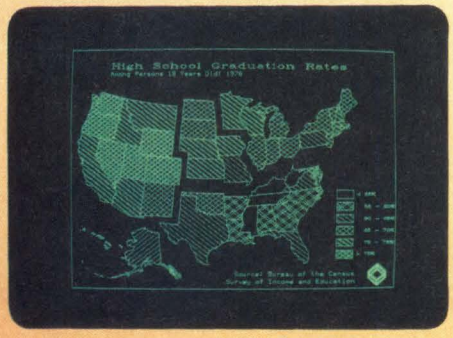
Nicolas Mokhoff
Senior Editor

High resolution, low cost graphics should be more than a retrothought.









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Dot Density Ratio	1:1	1:1	1:2	1:1	1:3	1:1	1:4	1:4	1:1
Screen Size	14″	14″	12″	12″	12″	12″	12″	12″	12″
Tektronix 4014 Compatible	STD	STD	NO	NO	NO	STD	NO	STD	STD
Data Tablet Support	STD	STD	NO	NO	OPT	OPT	NO	NO	NO
Multi-Vendor Printer Support	STD	STD	OPT	OPT	OPT	OPT	OPT	OPT	OPT
8 Dir. Cross Hair Cursor	STD	STD	NO	NO	NO	NO	OPT	OPT	OPT
Programmable Function Keys	STD	STD	NO	NO	NO	NO	NO	NO	NO
Tilt/Swivel Enclosure	STD	STD	NO	NO	NO	NO	NO	NO	NO
Compatibility	VT52 ADM3A H1500 D200	VT100 VT52 ANSI X3.64	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52
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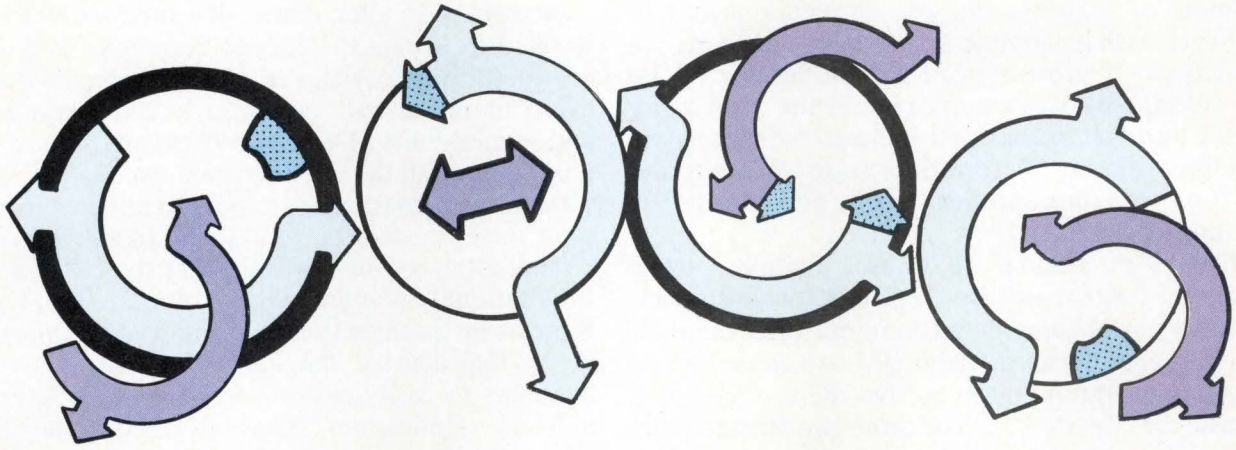
CIRCLE 74

NETWORKS EXPAND AS PBXs GET SMARTER

Local area networks integrate with private branch exchanges as data acquires a new partner in voice.



**by Nicolas Mokhoff,
Senior Editor**

In communication systems, 1984 may be the year of integration. True voice/data integration has been the quest of computer and communication design engineers since the beginning of the digital era. When the concept of digitizing audio signals was first proposed for data transmission and subsequently for voice transmission, and both had finally materialized, it remained only for designers to find an economical means for merging the two into a packet-format stream of information. While integrated voice/data networks have been designed for wide area network applications, and even for satellite transmission, the proliferation of remote processing applications recently prompted designers to develop local communication networks with integrated voice/data transmission capability.

Today, two mainstream technologies allow local distribution and communication of digital voice and data—private branch exchanges (PBXs) and local area networks (LANs). Sometimes the two technologies compete, and at other times they complement each other.

Integrated voice/data PBXs allow simultaneous switched voice and data communications without the use of modems. In any switching system, the flow of information passes from the point of origin to potential destinations via a switch that significantly reduces the total number of required paths.

Several voice/data communication switching schemes represent alternatives to dedicated point-to-point data communication connections. These include multidrop, computer terminal-to-host connections; bus-type LANs (Ethernet, etc); and PBX-type LANs. Each of these schemes may have different architectures, media, speeds, bandwidths, protocols, and formats. The objective of each scheme is communication between terminals and host processors, between host processors, or between terminals.

The PBX's traditional function is to connect a number of telephone lines supporting telephone sets to each other and to a lesser number of trunks that connect the PBX to the outside telephone world. Each telephone line and trunk typically require one port or time slot on the system in order to operate.

As the PBX evolved from an electromechanical device to a computer-based, stored-program control

system using digital technology internal to the switch, it became evident that the PBX could become a vehicle for switching digital data between processors and peripherals without using modems. Potential benefits included removing modem cost, increasing transmission speed, and improving transmission quality and reliability. Also, access to the data processing environment could be accomplished without additional wiring and hardware.

Ideally, voice and data transmissions are multiplexed over a single twisted pair of wires, requiring only one port at the PBX. Data communication capability can then be perceived as an added feature gained with little incremental cost, since at least one twisted pair and one port are already required on the system for voice communication.

Implementing an integrated voice/data transmission efficiently depends on several variables: the number of channels and type of media needed to connect each telephone set or data device to the switch; the number of ports used at the switch; and the additional hardware needed in the system and at the terminal to accomplish integrated voice/data communication. These variables are usually found in the succeeding second-, third-, and fourth-generation PBXs.

Second-generation PBXs are digitally stored program-control switches designed for voice communication. Adding data communication capabilities was actually an afterthought. An example of a second-generation PBX is Northern Telecom's (Nashville, Tenn) SL-1. The same two twisted pairs that were originally installed for voice communications adapt for data transmission by adding a line card to the PBX for each data terminal, and a data interface device at the terminal site. An additional port is used for each data device. This type of PBX supports data transmission speeds up to 9.6 kbits/s and can potentially handle up to 56 kbits/s.

Third-generation PBXs were designed to support simultaneous voice and data transmission, either over the same twisted pair, or over parallel twisted pairs, without using an additional port. An example is the InteCom (Allen, Tex) IBX system, which requires two twisted pairs but only uses one port on the PBX. An additional circuit board is required at the switch and in the telephone set. Currently, these systems operate at up to 19.2 kbits/s and are expected to be available for rates to 56 kbits/s.

Fourth-generation machines debut

Last year, a handful of companies announced fourth-generation switches. Rolm Corp (Santa Clara, Calif), NEC Information Systems (Lexington, Mass), and CXC (Irvine, Calif) have designed systems that combine a PBX and a bus-type LAN.

Ztel (Wilmington, Mass), on the other hand, designed its Private Network Exchange, or PNX, from the beginning as an integrated voice/data network using a token-ring topology. Designers were able to fully integrate the voice features of a computerized PBX and high speed data into a single, unified system.

It made a lot of sense for Ztel to combine the two technologies. Several advantages are inherent in developing a PBX-based product. As opposed to installing coaxial cable, PBX wiring is already in place in most businesses, and the PBX voice functionality will always be required. Adding the LAN technology facilitates the linking of devices, such as facsimile and personal computers that require high speeds.

One current trend is to use the PBX as a gateway to other network types.

According to Ztel, combining the PBX and LAN in the PNX lowers the cost of both voice and data communications, yields a more compact system, offers more features, and ensures better reliability and serviceability. These improvements are accomplished through the use of custom LSI circuits, software implementation techniques, and new types of fault tolerant, distributed system architecture.

The PNX system software strictly follows the International Standards Organization's (ISO) Open Systems Interconnection model and is implemented in the high level C language. This allows system designers to easily customize the PNX for specific industry applications. Currently, no other PBX allows this level of accessibility, according to Ztel.

Ztel made a radical departure from typical PBX architecture. The PNX architecture reflects current trends in the corporate environment. In a typical PBX star architecture, telephones and terminals connect to a central processor. The information flows through some common carrier to its destination, where it is then distributed to the proper recipient. This typical PBX environment is changing very rapidly. While the PBX function will always be needed for voice communications, the growing trend is to add productivity aids such as electronic mail and calendaring to the PBX.

Another trend is to use the PBX as a gateway to other network types. A gateway is needed when voice and data information exit a facility. Add to this a growing marketplace that requires significantly more information. While one data device currently serves every 10 to 15 office workers, within a few years one device will be required for five (or fewer) workers. With this explosion in devices, implementing separate communication solutions becomes very expensive.

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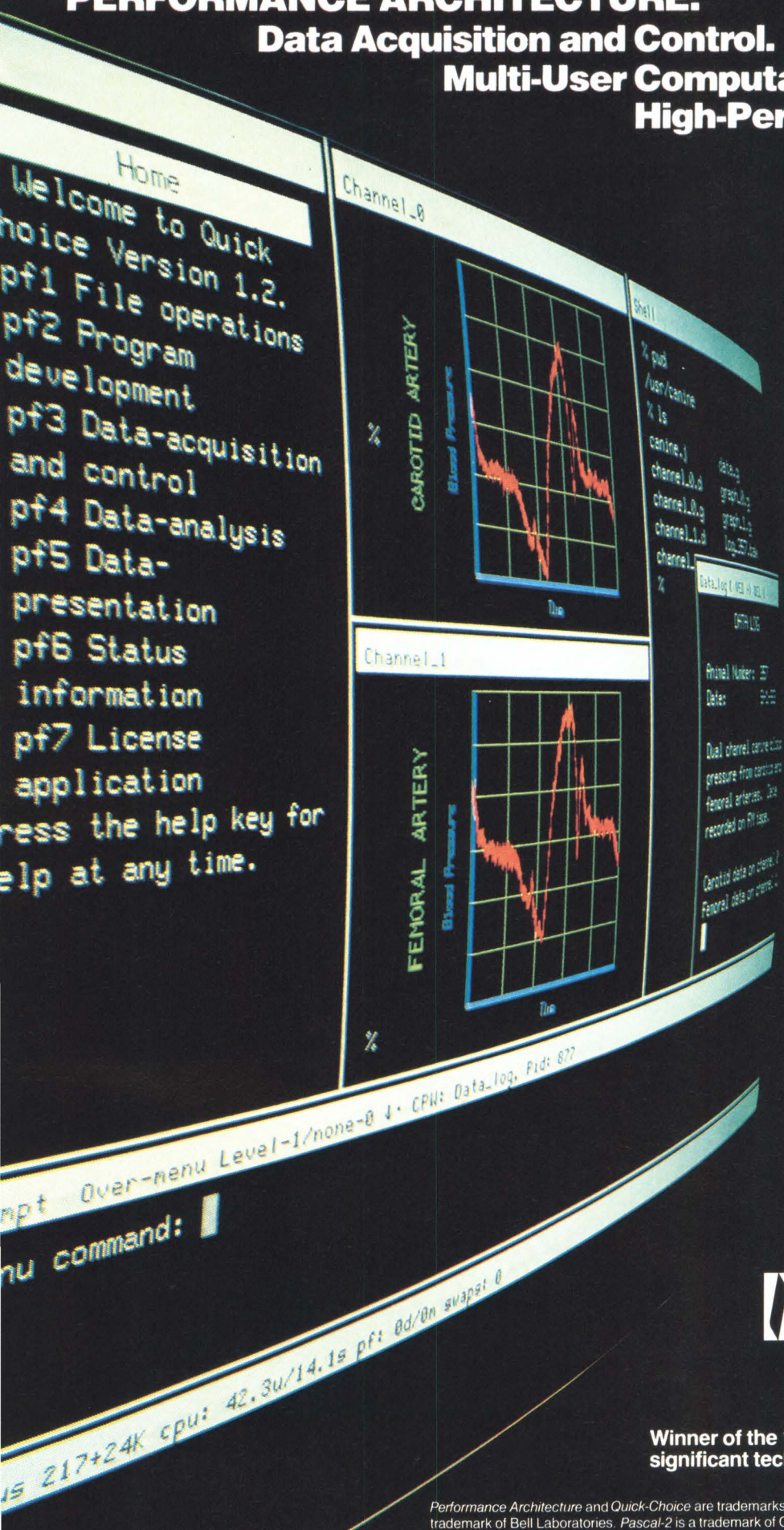

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continues nationally and internationally. Without a totally integrated network, it will be more difficult to achieve the information flow and transfer required to support decision making.

The PNX architecture shines

Ztel's PNX design was based on several determinations about the requirements such a network should meet. Ztel's engineering managers decided that their system needed voice communications equal or superior to a traditional PBX system, or it would be unacceptable. The system required great reliability because all of a company's communication requirements—voice, data, image, and video—would move through one system. Of course, it would incorporate local area networking as well.

This LAN would have to be compatible with some accepted standard. Adopting the IEEE 802.5 token-passing standard was a major step in this direction, especially since IBM has opted for a version of that standard for its upcoming LAN. Ztel engineers selected a token-ring scheme after evaluating both carrier sense multiple access/collision detection (CSMA/CD) and token-bus standards, and rejecting both because of performance inadequacies and reliability problems. Each ring in the PNX network operates at the IEEE 802.5 standard rate of 10 Mbits/s—the minimum rate needed for voice transmission.

In a token-ring network, the transmission medium forms a circle through each connected device. Information is communicated in sequential order around the ring. Devices transmit and receive information by appending or extracting messages from the medium as tokens circulate through the network.

The PNX digitizes the data and analog information as it enters the network. Data is also formed into packets, and these packets are intermixed with packets from other transmissions and routed through the network. They therefore make efficient use of available bandwidth.

To implement a LAN based on a token-passing protocol with a ring structure, Ztel added devices to the system processing units (SPUs) to provide the functionality of a data switch. Each SPU can perform three types of processing: switch processing to handle and connect voice and data calls; applications processing to perform tasks such as least-cost routing, directory look-up, or other value-added applications; and data conversion processing to format data into packets and provide protocol conversion between different types of equipment. SPUs can be added to expand the system. The failure of any one processor will not shut down the system; its work load can be distributed among other processors.

Devices such as phones and terminals can be interfaced to the SPU via a standard quad telephone line up to 5000 ft long that carries two information channels. The Ztel channel structure includes one digitized voice channel, one data channel, and two control channels of the correct size to guarantee correct data operations at 56 kbits simultaneously with voice.

Foreign computer equipment meeting protocol requirements can be attached directly to the token ring. This is done by using simple wall connectors, as defined by the IEEE 802.5 standard.

The PNX's very high throughput is due to its deterministic nature, which allows prediction of the worst-case performance of the network independent of its load. This is a valuable characteristic in both telephone and data communications. A deterministic network can achieve transmission rates high enough for transmission of video, graphics, and file services without fear of deteriorating performance.

An even higher throughput rate can be achieved by using multiple rings, which may be installed according to the required level of service. Ztel's initial release allows up to 40 rings to operate in one PNX system, with each ring operating at 10 Mbits/s, for total throughput of 400 Mbits/s. Thus, the PNX has the throughput potential to handle extremely high data rates that will be required in the near future by automated equipment. In addition, a high level of system reliability is possible with a multiple-ring network. If one ring fails, backup mechanisms redistribute that ring's traffic over other active rings.

As more bandwidth is required, more rings can be added incrementally at relatively low cost. While packaging artificially imposes the current limit of 40 rings, the architecture allows hundreds of rings. According to Ztel, future implementations will remove this packaging barrier.

PNX has both packet and circuit rings. The totally transparent circuit rings handle digitized voice—one 10-Mbit circuit can handle 113 simultaneous conversations, each in a 64-kbit/s slot. Any data call can also be put on the ring but trransmitting a 4800-bit/s data transaction over a 64-kbit/s slot is considered wasteful. The circuit ring can also be used to transmit video information.

LAN-compatible devices are connected to the packet ring, which transfers packetized data from source to destination. The PNX determines whether the circuit or packet ring will be used, and packetizes the information accordingly. Depending on the network's characteristics, there may be any number of circuit and packet rings.

IBM rings in new LAN

Because of its size, IBM will tend to dominate the networking market with the architecture and standard that it chooses. IBM also has a large commitment in its systems network architecture (SNA),

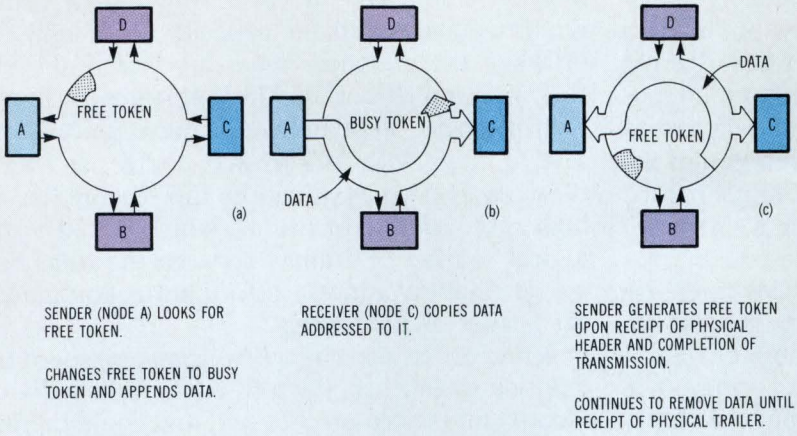

Fig 1 In the token-access control scheme, a node that has data to transmit captures the free token, changes the token to a busy status, and begins transmission. The receiving node unties the busy token after receiving the physical header from the sending node, which allows other nodes to transmit.

which has to bear on the company's LAN architecture choice. IBM has thus narrowed its choice down to a ring topology with token-access control.

The control mechanism for regulating data flow in a ring topology is generally based on use of a token passed sequentially from node to node around the ring. The token contains a 1-bit indication that it is "free" (T = 0). This single free token circulates on the ring, giving each node in turn an opportunity to transmit data when it receives the token (Fig 1). A node that has data to transmit can capture the free token, change the token status to busy, and begin data transmission. The node that initiates a frame transfer must remove that frame from the ring and issue a free token upon receipt of the physical header. This allows other nodes an opportunity to transmit. If a node finishes transmitting the entire frame prior to receiving its own physical header, it continues to transmit idle characters (contiguous 0s) until the header is recognized. This ensures that only one token (free or busy) is on the ring at any given time.

IBM engineers chose the token-access control protocol because they say that it provides uniform access to the ring for all nodes. A node must release a free token after each transmission and is not allowed to transmit continuously (beyond a maximum frame size or preset time limit) on a single token. All other nodes on the ring will have a chance to capture a free token before that node can capture the token again. In some system configurations, it may be necessary for selected nodes, such as bridges or synchronous devices, to have priority access to the free token.

Setting priorities

A priority mode is used along with reservation indicators to control this access mechanism. Various nodes may be assigned priority levels for gaining access to the ring. A selected node can then capture any free token that has a priority mode setting equal to or less than its assigned priority. The requesting node can set its priority request in the reservation field of a busy token if the priority of that node is higher than any current reservation request.

The current transmitting node must examine the reservation field and release the next free token with the new priority mode indication, but retain the previous priority level for later release. A requesting node uses the priority token and releases the new token at the same priority so that any other nodes assigned that priority also have opportunity to transmit. When the node that originally released the priority free token recognizes a free token at that priority, it then releases a new free token at the level that was interrupted by the original request. Thus, the lower priority token resumes circulation at the point of interruption.

In the IBM LAN, normal token operation is monitored by a token monitor that is perpetually active in a single node on the ring. This function can be performed by any node on the ring and is necessary to initiate the proper error recovery procedure if normal token operation is disrupted. This includes the loss of a free token or the continuous circulation of a busy token, both of which prevent further access to the ring. The monitor function exists only for token recovery and does not play an active role in the normal exchange of data frames.

The ability to be an active token monitor exists in all active nodes attached to a ring. These other nodes maintain a standby monitor status and are prepared to become the new active monitor should a failure occur in the current active monitor. The standby monitors are essentially monitoring the ring to detect abnormal ring operation that could occur whenever the active monitor fails. Detection of an error condition by any standby monitor initiates a recovery procedure that allows it or one of the other nodes to become the new monitor.

While the LAN provides a basic transport mechanism for data transfer among nodes within the network, it does not provide all of the functions necessary for two nodes to manage and conduct a

meaningful two-way information exchange. The same higher level communication protocols implemented to control data transfer across public data networks are also applicable to data transfer across a LAN. Both the SNA concept and the ISO reference model separate network functions into layers to facilitate the description and implementation of the protocols. The SNA protocols can be implemented for managing information flow within a LAN as in any other SNA environment.

The functions of the lowest physical layer are unique to the particular transport mechanism implemented—whether it be a communication loop, a multidrop bus, or a token ring. The model's physical layer encompasses the basic functions associated with placing electrical signals onto the transmission medium. This includes such fundamental operations as signal generation, phase timing along the ring, and encoding of signal information using the differential Manchester scheme. These operations are performed within the ring interface adapter at each active node in the network.

The next higher layer, data-link control, is traditionally independent of the actual physical transport mechanism. It performs the functions necessary to ensure the integrity of the data reaching the layers above the data-link control level. The IEEE 802 Committee and the European Computer Manufacturers Association (ECMA) have proposed that, for LANs, the data-link layer of the ISO model, which corresponds to the same layer of the SNA, be further subdivided into two functional sublayers: logical link control (LLC) and media access control (MAC). This functional decomposition essentially separates functions into hardware dependent and hardware independent. Thus, compatibility between SNA and the ISO model implementation is ensured.

Proposed data-link sublayers

The MAC sublayer of a token-ring LAN would include functions associated with frame and token transmission that can be, but are not necessarily, performed by the interface adapter in each node. The LLC sublayer would include those functions unique to the particular link control procedures associated with the attached node and not the medium access one. This would permit various logical link protocols to coexist on a common network, such as a SNA-compatible token-ring LAN, without interfering with one another. Logical links are established primarily to ensure data integrity to the higher layers. Multiple LLCs may exist within each node. In these instances, a link multiplex function within the LLC layer directs incoming frames to the appropriate LLC task and also provides the correct address information for outgoing frames. LLCs are logically associated within nodes.

IBM engineers, like those at Ztel, do not rule out multiple-ring LANs in cases where data transfer requirements exceed the capacity of a single ring, or when the attached nodes are widely dispersed (eg, in a multifloor building or campus environment). These large networks may typically have several rings with 100 to 200 nodes per ring. In those cases, two rings can be linked together by a high speed switch, or bridge, which would provide logical routing of frames between the rings based on destination address information contained in the header of the frames.

A bridge can also change transmission speed from one ring to another. Each ring retains its individual identity and token mechanism, and could therefore stand alone in the event the bridge or another ring is disrupted. The bridge's interface to a ring is the same as any other node's interface, except that it must recognize and copy frames with a destination address for one of the other rings within the network. Also, several frames can be temporarily buffered in the bridge while awaiting transfer to the next ring.

The local network can be further expanded to meet larger data capacity requirements by interconnecting multiple bridges. This results in a hierarchical network in which multiple rings are interconnected via bridges to a separate high speed backbone. The backbone itself can be a high speed token ring or it may be a token-access bus link, such as a channel within a broadband cable TV system. The address field format is structured to designate the specific ring to which a node is attached, thereby facilitating the routing of frames through bridges.

Finally, a gateway node provides an interface between the token-ring LAN and a wide area network. Here the gateway node allows long-distance communication between nodes within different LANs. The gateway performs the necessary address translations, as well as speed and protocol conversions necessary to interface the LAN to these various transmission facilities. A gateway could also be used as an intermediate node between a token-ring LAN and nodes located in either a CSMA/CD- or PBX-based LAN.

A ring interface adapter at each node performs the primary functions associated with token recognition and data transmission. Advances in VLSI technology make it possible to delegate a large portion of the communication function to the adapter itself, thus freeing the node from this processing. The adapter handles basic transmission functions including frame recognition, token generation, address decoding, error checking, buffering of frames, and link fault detection.

There may be instances where a particular device with an incompatible communication interface is to be attached to the LAN. In such cases, a separate interface converter can be attached between the

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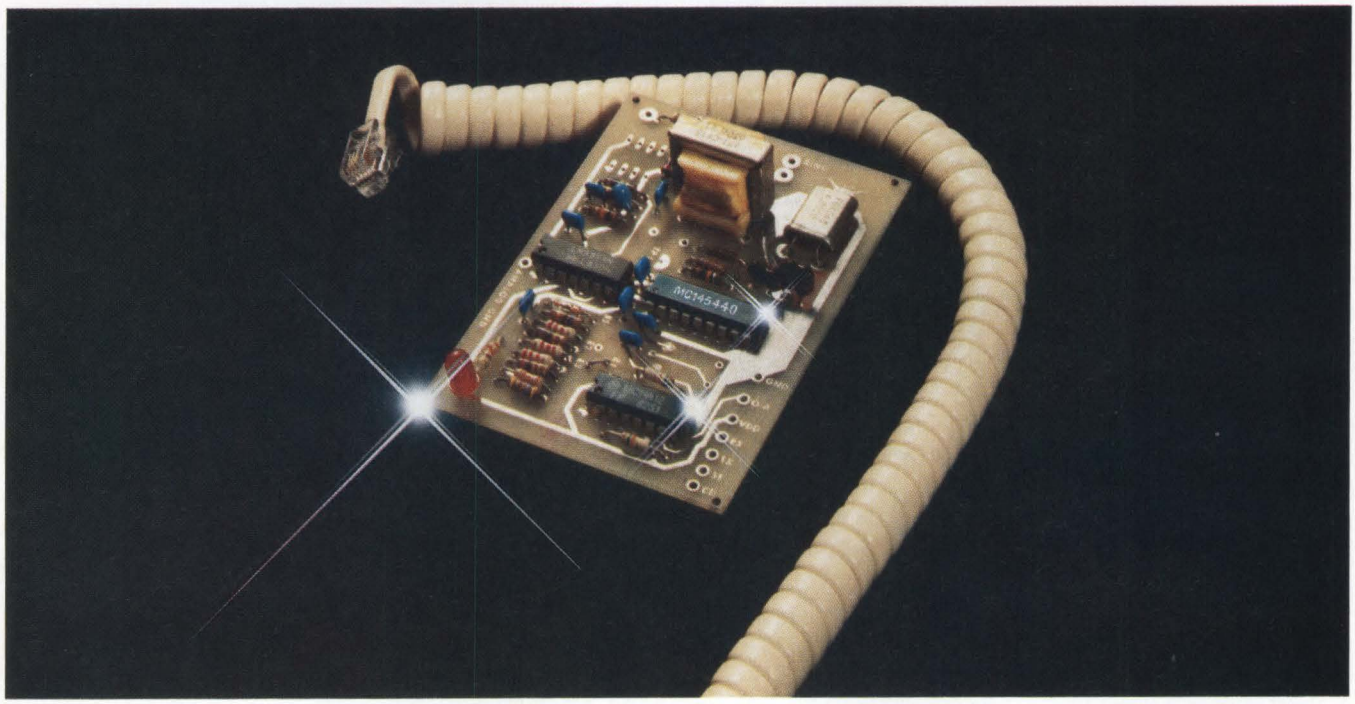

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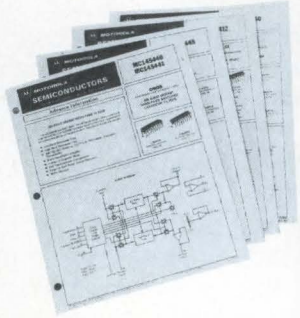

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device and the token ring to perform the conversions that are required to send and receive data over the LAN.

The IBM-TI affair

IBM is working with Texas Instruments (Dallas, Tex) to develop an adapter for a token-ring LAN. Requirements for an adapter to a LAN are essentially independent of the type of local network used. Engineers from both companies concluded that the requirements can be summarized as follows: performance, functionality, hardware and software compatibility, error detection and isolation, flexibility, quality, reliability, and cost.

Obviously, the adapter must meet serial data communication rates specified for the LAN. Due to frequency versus distance trade-offs, however, this rate should vary to allow longer distance connections. The IEEE 802 Committee has recognized this by standardizing a range of data communication speeds. For token-ring networks, the data transmission rate exceeds 10 Mbits/s. The VLSI architecture of an adapter should also accommodate the range of functions adapters will include, but partition the interface breaks for each increment of functionality at cost-effective points.

The two companies' engineers considered two approaches for their LAN adapter: a closely coupled design and a controller architecture design. In the closely coupled approach, the LAN peripheral coexists on the system bus with main memory, the host processor, and other peripherals. This environment leads to the LAN buffers for transmission and reception of data and the LAN linkware (or lower level software) sharing main memory with the attaching product operating system and application code. The host processor provides bandwidth to support the processing on low level interrupts and the execution of low level software.

Making the closely coupled configuration fit the initial adapter requirements resulted in many drawbacks. In the face of these drawbacks, TI engineers opted for a controller approach. The integrated design includes an engine, ROM, scratchpad memory, and flexible system interface (Fig 2). As a result, adapter requirements are met. System performance is isolated from the capabilities of the attaching product host processor and the system memory speed. This puts buffering of data flows between the host microprocessor and the asynchronous events on the LAN. Rapid-response interrupt processing necessary to support LAN traffic is also separated from the host.

The software required by the adapter for response-intensive low level functions resides primarily in the adapter processor memory space. As such, it does not require integration with the operating system. The very nature of a controller design is to isolate the function from a given hardware processor bus.

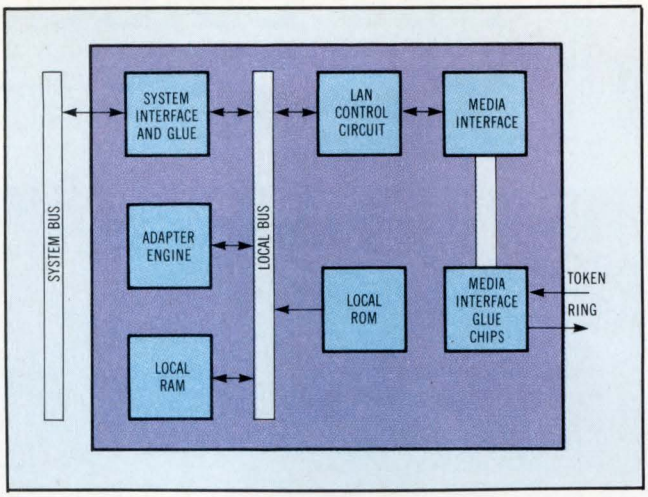

Fig 2 A joint IBM/TI effort to develop a token-ring LAN adapter resulted in this preliminary design. The adapter engine is a 16-bit microprocessor that can accommodate fast interrupt response times. The VLSI adapter chip will be able to meet ring transmission speeds over 10 Mbits/s in a full-duplex mode.

This allows interface of a broad range of processor types, thereby increasing the flexibility of the architecture for users.

Significant software is required just to support the lower levels of the data communication hierarchy. This software is integrated into the LAN adapter, ensuring that different vendors' software will act the same in different processor/memory system environments at the peer levels supported in the LAN adapter chip.

A high level of error detection and isolation capability is built into the adapter. By isolating the engine and control memory of the adapter from the host processor, the LAN adapter can execute diagnostics independent of the host. The adapter can also alert a LAN management facility that its attaching product is having a problem, thereby requesting reconfiguration.

By integrating the design of an engine and control memory from the beginning, operating cost and initial cost are lower than if a closely coupled architecture were used, according to TI engineers. Life cycle costs for end users are lower through a high level of integrity built into adapters of attaching products—this raises the network's overall availability. Exceptional fault isolation capabilities ensure rapid service, thereby also reducing cost. These features reflect through to the overall network level, resulting in a connection facility of high performance and availability with a very aggressive life cycle bit transport cost.

The adapter chip meets the ring transmission performance requirements, with speeds over 10 Mbits/s in full-duplex mode. With two DMA channels for transmit and two for receive, it is capable of receiving back-to-back frames on the ring.

Also, the adapter implements all protocol features. Extensive internal control code and data

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buffering permit the adapter to send and receive MAC frames without user processor intervention, significantly reducing the load on the user processor bus. In fact, recent experience has shown that the limiting factor in LAN communication is the software layering overhead of sending or receiving frames. By providing much of this software in silicon, TI's token ring adapter reduces this bottleneck.

The adapter meets hardware compatibility requirements by being able to select from a variety of popular microprocessor family bus timings and 8- or 16-bit data transfers. Bytes can be swapped by changing pins on the chip, thereby maintaining sequentially transmitted bytes in increasing system address order, regardless of the system byte-numbering conventions.

The IC meets quality goals by implementing a special single-cycle mechanism during chip testing that allows the test program to check for possible stuck-at faults. Extensive checking performed by each adapter ensures high ring reliability. Thus, faulty adapters can be quickly isolated and removed from the ring.

More token chips

Another semiconductor firm with a token-passing LAN adapter chip is Western Digital Corp (Irvine, Calif). And, Standard Microsystems Corp (Hauppauge, NY) has developed the COM9026 IC, principally for the ARCNET, a token-passing PBX/LAN system from Datapoint Corp (San Antonio, Tex). Western Digital's WD2840 Token Access Controller (TAC) is designed to interconnect distributed intelligent devices via a shared broadcast medium such as coax cable, air radio, or twisted-pair party line. The medium is shared by all attached stations using a token-passing protocol. A station is a microprocessor-based device incorporating a TAC and connected to the network.

The key design goal of the TAC was to free the system designer from data communication concerns. For example, once the TAC is initialized, the host microprocessor need never be concerned with the protocol. It simply processes frames addressed to it (the TAC filters out all others) and generates any messages it wants to send (the TAC sends them when the token is received).

Because all functions affecting network performance (eg, token processing and acknowledgment generation) are inside the TAC, the user need not be concerned about the type of host processor. The TAC is designed to interface to a microprocessor system already busy with a specific application. An example might be the microprocessor common in today's CRT terminals. A microprocessor in a terminal already must scan the keyboard and perform limited editing. Its leftover processing power is sufficient to drive the TAC, since it only handles data to/from that specific terminal. If the microprocessor falls behind momentarily, it only affects that terminal, all others on the network continue to enjoy full speed operation. Thus, a network of TACs is not slowed by its weakest link.

Western Digital engineers based the WD2840 on a highly microprogrammed device that incorporates three microcontrollers, a two-channel DMA subsystem (shared by the three microcontrollers), a shared register file, two timers, and high speed bit-oriented controllers on a single NMOS LSI device.

The DMA subsystem inside the WD2840 consists of two internal sets of sixteen bit address counters, two independent byte counters, and the required control/sequencing logic. The value of doubling up is to support the full-duplex operation needed for loop-back testing. In addition, this architecture gives the device the ability to interleave data and control block accesses from memory for optimum efficiency.

Where AT&T stands

Meanwhile, AT&T Information Systems (Morristown, NJ) engineers have developed a unique LAN architecture that stays away from both established types—CSMA/CD and token passing. Their concept combines the advantages of both distributed and centralized LAN architectures. Moreover, the intended media is wide band fiber optic cable. AT&T engineers contend that although a bus is a good means for interconnecting many information-handling devices because it offers modular growth and can employ simple techniques (eg, polling or contention) for traffic handling, it is somewhat limited. Most computers use buses to interconnect their internal components. However, when a bus is used for a LAN where the distance between devices can be significant, propagation delays must be taken into account. These delays complicate the methods used to govern traffic on the bus, say AT&T engineers, and in general, the transport efficiency of the bus declines as distance and delays increase.

The engineers chose a centralized bus to solve this problem. The bus is made very short to promote high efficiency. Physically, the bus is realized as the backplane of a cabinet to which relatively long access lines can be connected via plug-in interface modules. Interface modules can be designed to give access to various device types, such as terminals, hosts, or personal computers. Thus, the advantages of modularity and simplicity are retained, while the problem of efficient traffic handling is solved. Also, fiber optics can be used in a straightforward manner.

Designers based the system on a central node containing a contention bus, a broadcast bus, and a switch module as its fundamental elements (Fig 3). This node acts as a fast packet switch that provides virtual circuit service. All data enters via the contention bus and passes through the switch module to the broadcast bus. Interface modules connected

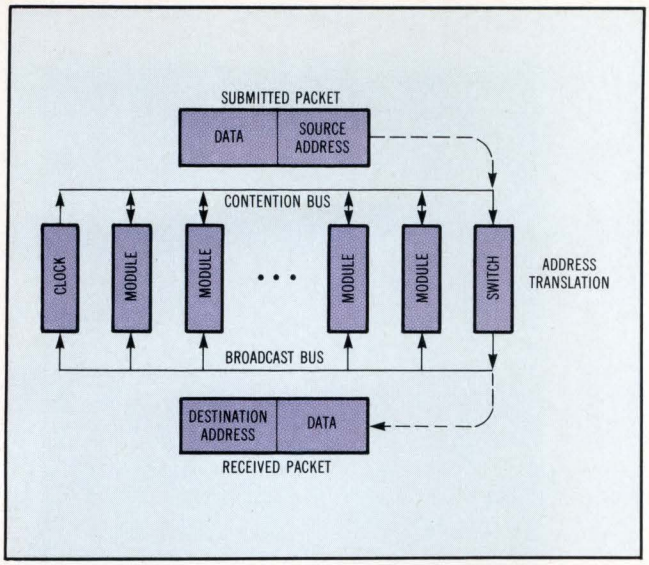

Fig 3 AT&T's answer for including both a centralized PBX-like network and a distributing ring or bus network is to combine the two into a network that includes a central node with a contention bus, a broadcast bus, and a switch as the essential elements. In such a network, each node acts as a fast packet switch that provides virtual circuit service.

to both buses buffer and form the data packets. The packet is then placed on the contention bus in the next available time slot. Time slots are defined via a separate clock bus controlled by a clock module. If more than one interface module tries to place a packet on the bus in a given time slot, the contention is resolved in a nondestructive manner and the winning module places its packet on the bus. Each packet contains a source address that is read by the switch module and translated into a destination address. The translation is stored in a table within the switch module where entries have been set by a prior call setup process. In this way, a virtual circuit service is provided. The switch module then places the packet and its destination address on the broadcast bus to be picked up by the appropriate interface module for delivery to the destination device.

AT&T engineers have ensured that the central node functions with minimal delay. Propagation delay on the bus is less than a bit period even at multi-megabit speeds. This ensures "perfect scheduling" of packet transmissions. No time is lost in the contention process, and there are no idle periods when packets are ready for transmission, so bus access delay is minimized. In addition to low bus access delay, the switch module performs address translation in hardware so it functions quite rapidly. The delay through the module is equivalent to that of a single-packet time or time slot on the bus. Time slots are very short because the bus speed is high. Packet lengths are kept relatively short to promote efficiency and flexibility of transport.

Many devices can access the central node. Instead of running separate lines, the data streams can be efficiently combined into a single high speed line for transport to the central node. Optical fiber—an ideal medium for such transport—is very advantageous in physical plant applications. The system's centralized nature allows straightforward use of fiber without the need for taps. Of course, the difficulty in tapping a fiber adds to system security. Local Bell companies have already installed fiber optic LAN test beds in several locations.

Perfect schedules

The centralized-bus architecture uses a contention mechanism to gain access to the bus. This results in a perfect scheduling of packet transmissions on the time-slotted bus. That is, in contrast to distributed bus and ring architectures, the centralized-bus system avoids destructive collisions as well as idle periods during which the transmission medium holds packets awaiting transmission. Moreover, this characteristic is robust with respect to selected packet size, bus transmission rate, and geographical separation among the attached devices. In addition, AT&T engineers say the scheduling of packet transmissions is flexible, permitting multiple priority classes, round robin-like scheduling within a priority class, and even IC and packet switching. With these features, real time synchronous data and voice can be readily integrated.

The contention off the bus is never missed because interface modules residing on a node or concentrator backplane transmit packets in fixed-length time slots. As shown in Fig 4, the packet format consists of a header followed by a data field. The header is composed of a priority code, module number, and channel number. The module and channel numbers are used in the virtual circuit addressing and routing of packets. The priority code

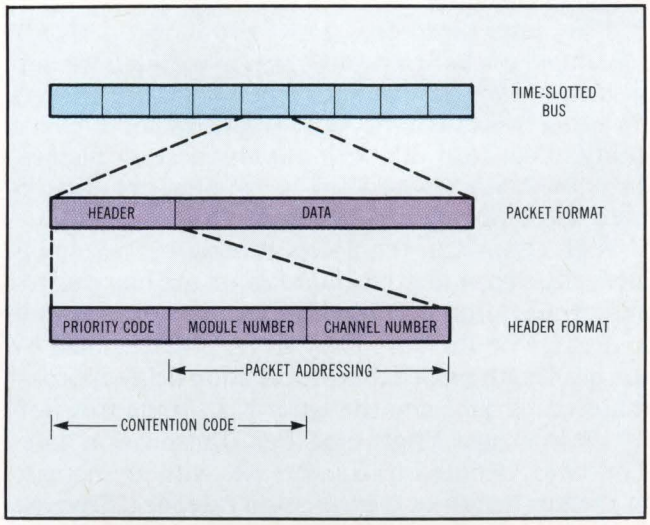

Fig 4 The contention method to access the AT&T short bus uses a packet format that consists of a header followed by a data field. The header, which consists of a priority code, module number, and channel number, specifies the time slot by having the contending interface module with the highest contention code transmit its packet in that time slot.

and module number comprise the packet contention code. Contention occurs at the beginning of each time slot when the contending interface module with the highest contention code wins the contention and transmits its packet in the time slot. Although the module number is fixed and unique to each interface module on the backplane, the priority code can change with time, allowing flexible distributed scheduling of packet transmissions.

The contention mechanism relies on two properties of the bus to achieve perfect scheduling of packet transmissions. First, the end-to-end propagation delay of the short bus is less than the time to transmit one bit. Second, each module can simultaneously transmit and receive with the (open collector) bus functioning as a logical OR gate. With these two properties, the bus contention operates as follows. At the start of each time slot, each contending module begins transmitting its contention code. After each bit, if a module's transmission differs from what is read off the bus, it stops contending. That is, if a module transmits a 0 and reads a 1, it drops out of contention and waits for the next time slot. Hence, by the end of the module number transmission, the module with the highest contention code wins the contention and continues to transmit the remainder of its packet without interference.

Contention takes place on a bus separate from the one on which packets are transmitted. The module winning contention in one time slot transmits its packet in the next time slot on a higher speed, parallel data bus. With this approach, transmission rates on the order of 50 to 100 Mbits/s are possible, according to AT&T engineers.

A good competitor

The centralized-bus LAN produces perfectly scheduled packet transmissions, avoiding both collisions and bus idle periods when there are packets awaiting transmission. AT&T engineers conducted a study to contrast this with popular access schemes, such as CSMA/CD and token passing, for distributed bus and ring architectures.

With CSMA/CD, the access protocol efficiency is critically dependent on the ratio of the bus end-to-end propagation delay to the mean time to transmit a message on the bus. The former is determined by the bus length (with cable propagation delay approximately 5 μs/km) and the latter is a simple function of the message length and bus transmission rate. The ratio, denoted by α, increases with an increase in the bus length or transmission rate, or a decrease in the mean message size. The average delay versus load performance for CSMA/CD degrades from that of perfect scheduling as α increases from 0 (Fig 5). For a system with a 2-km cable length and a mean message length of 1000 bits, the three values of α, 0.01, 0.05, and 0.1, correspond to a bus transmission rate of 1, 5, and 10 Mbits/s respectively. As α increases, the usable bandwidth provided by the bus diminishes and thus the delay experienced approaches infinity at smaller loads. Therefore, the load on the bus approaches this capacity limit, at which point, AT&T engineers contend, operation is unstable. The perfect scheduling of the shorter bus performance shown in Fig 5, which corresponds to $\alpha = 0$, is for an unslotted system.

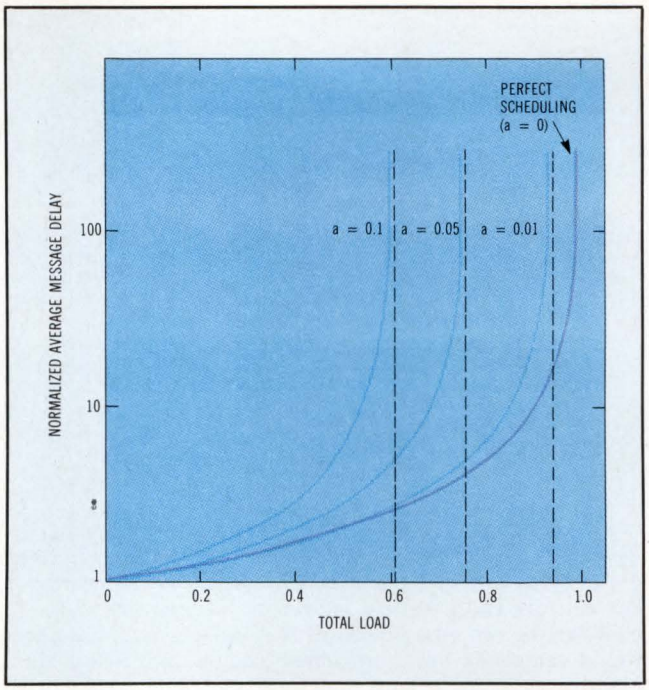

Fig 5 When comparing AT&T's contention bus delay to that of a typical CSMA/CD scheme for a normalized average message delay, AT&T's contention scheme fares better than CSMA/CD for scheduling packet transmission at different loads. The average delay versus load performance degrades in CSMA/CD versus that in the short bus as the ratio α (bus propagation delay to the mean message transmission time) increases from zero.

As for token-ring architectures, AT&T engineers assert that media access efficiency decreases as ring latency increases. The ring latency equals the delay in transmitting a bit completely around the ring. This includes both the ring propagation delay and the processing delay at each ring interface unit. Degradation occurs in performance for a single token system as α (now the ratio of the ring latency and mean message transmission time) increases. The ratio increases with an increase in the ring length, transmission rate, number of interface units, or processing delay per interface unit, or a decrease in the mean message size. For a system with 50 interface units, a 2-km cable length, and a mean message length of 1000 bits, the three values of α, 0.1, 0.5, and 1.0 (Fig 6) correspond to, respectively, a transmission rate and per interface unit processing delay of 5 Mbits/s and 1 bit, 10 Mbits/s and 8 bits, and 20 Mbits/s and 16 bits. Thus the usable bandwidth decreases as α increases.

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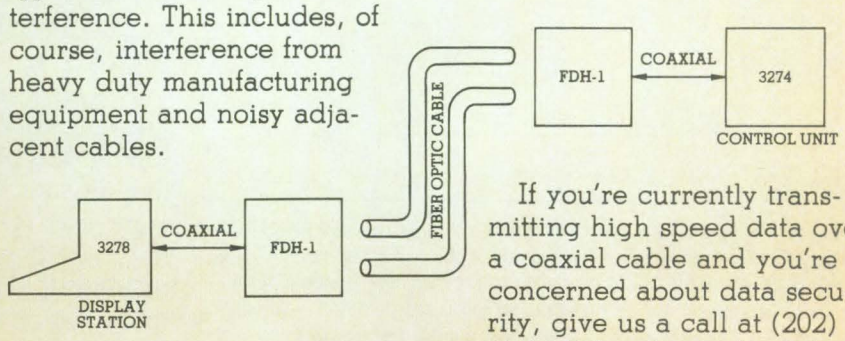

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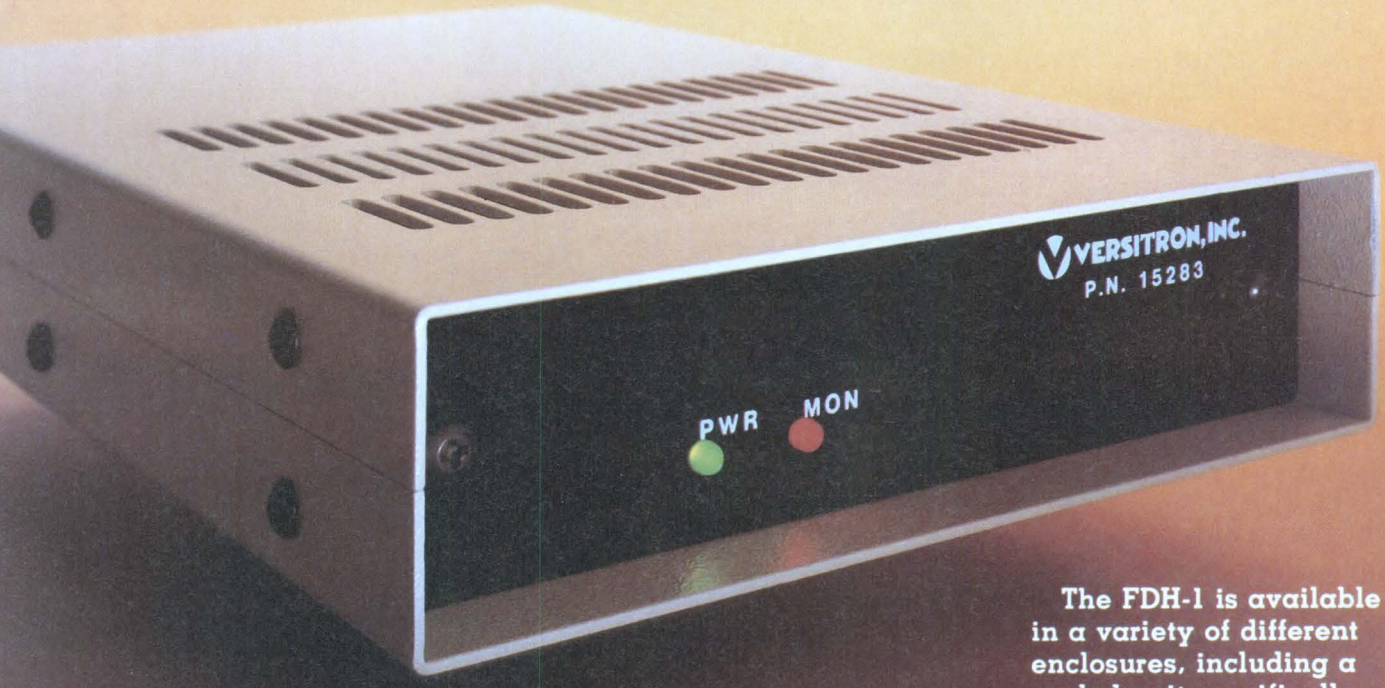

The FDH-1 is available in a variety of different enclosures, including a sealed unit specifically designed for EMI/RFI suppressed applications.

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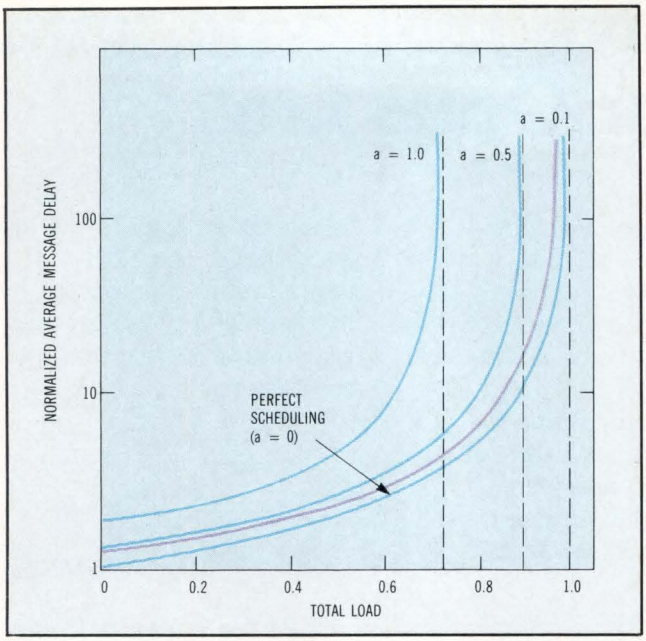

Fig 6 When comparing the short contention bus to a token ring, AT&T's contention bus again excels. As the ratio α (the ratio of the ring latency to the mean message transmission time) increases, the performance for a single-token system degrades. This results in a smaller usable bandwidth.

From these comparison results, AT&T engineers conclude that average delay performance for the short-bus contention scheme exceeds that of CSMA/CD and token passing. In fact, its average delay performance is lower bound to that achieved by the other two schemes.

Throughput is an important measure of data communication system performance. At the data-link level, throughput depends on the serial bit rate (the rate at which data is actually transferred on the link), and the interframe spacing (the time that passes from one transmission or reception of a frame until the controller is ready for a new transmission or reception).

A heavy-duty controller chip

A powerful controller chip that accommodates a high throughput rate is the i82586 from Intel Corp (Santa Clara, Calif). Intel's chip handles all the functions of a CSMA/CD controller. The i82586 operates at data rates up to 10 Mbits/s, which is about an order of magnitude higher than most LSI communication controllers now provide. Intel claims that alternative implementations to the i82586 require many chips to meet this bit rate. This rate is achieved because transmission and reception are performed by separate onchip machines dedicated to these tasks (Fig 7).

The i82586 can receive any number of back-to-back frames that maintain interframe spacing of at least 9.6 μs. This is due to the concurrent operation of three processors on the chip: the fast micromachine that handles memory structure, the onchip DMA controller that transfers data between the chip and system memory, and the transmit or receive machines that interact with the network.

The chip is intended for four main application areas. As a serial backplane it acts like a network, interconnecting devices inside a hardware cabinet or a room. It replaces bulky "parallel" cables with a single twisted pair or coaxial, while still providing high bandwidth.

It also serves Ethernet and networks conforming to the IEEE 802.3 and 802.4 standards, which are intended for office automation and similar applications. The transmission medium is shielded baseband coaxial cable with a branching nonrooted tree topology. Maximum station separation is specified as 2.5 km and the bit rate, of course, can be up to 10 Mbits/s.

The chip can also be implemented in mid-range local networks such as Mirlan—the Intel and NCR joint effort targeted at cost-sensitive applications that do not require high performance. This network uses inexpensive cable plus hierarchical data link control flags as well as bit stuffing for frame delimiting. The data rate is 1 Mbits/s and maximum station separation 1.3 km without repeaters.

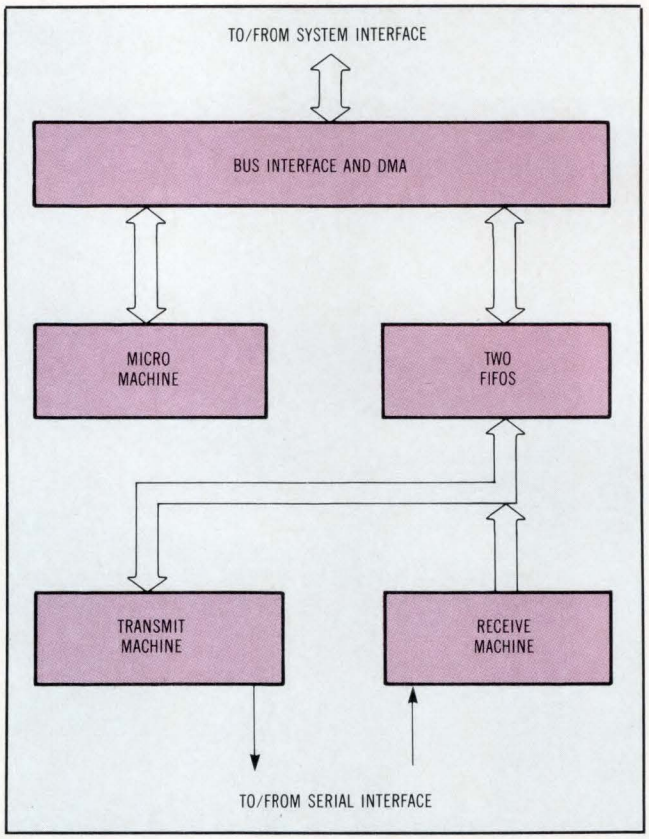

Fig 7 In order to accommodate a fast throughput for Ethernet nodes, Intel engineers optimized their controller chip to allow any number of back-to-back frames with interframe spacing set at least 9.6 μs to be received. This feat is accomplished using three concurrent onboard processors. The two first in, first outs (FIFOs) are used to accumulate bits to prevent overruns or underruns due to bus latency and also to reduce the number of data bursts to minimize bus switching overhead.

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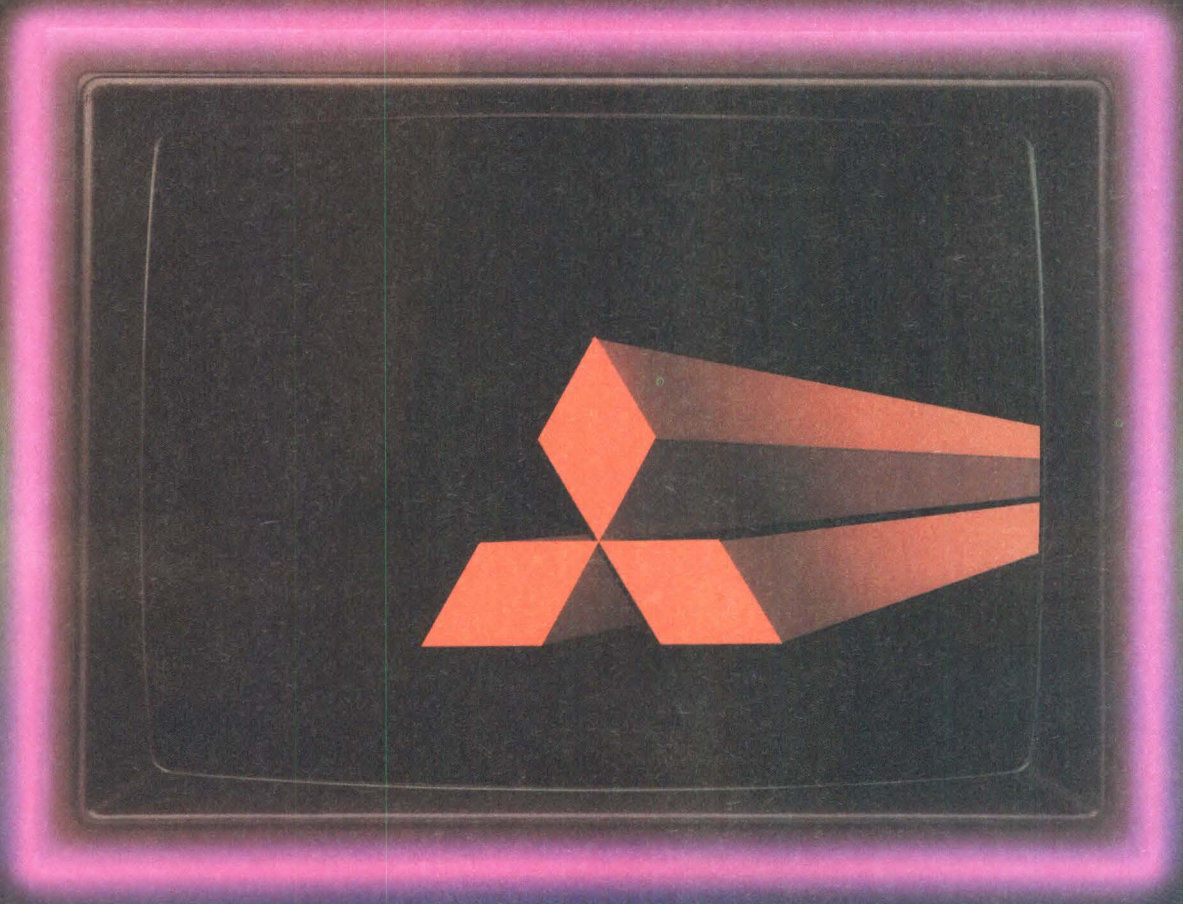

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TABLE 1

Key Considerations for Choosing LAN Topologies

Key considerations	Twisted wire	Baseband	Broadband	Fiber optics
Terminal type	low speed intelligent or dumb	intelligent only	dumb or intelligent	dumb or intelligent
Central network intelligence	yes—PBX	not required but can be done for network management	yes	no
Bandwidth	3 MHz (limited distance)	50 MHz (limited distance)	440 MHz (many miles)	virtually unlimited
Capacity per cable	one channel	one channel	hundreds of voice video and data channels	presently one channel
Maximum number of terminals	limited by conduit space	limited by bandwidth of channel	unlimited	potentially unlimited
Videoconferencing	yes—but not full motion	no	yes	yes
High data rate graphics capability	no	no	yes	yes
Capacity for higher data and future expansion rate devices	very difficult	very difficult	easy	easy
Distance	unlimited with modems via phone network	1500 m-one mile	40 miles	unlimited
Repeater requirement	standard phone network	every 1500 m—very expensive, inefficient	ordinary cable TV amplifiers at 2000-ft spacing	every 4000 ft
Speeds	9600 bits/s max 2400 baud typical	50 Mbits/s max	10 Mbits/s maximum on each of many channels	200 Mbits/s
Typical configuration	point-to-point/ multidrop/radial	radial/ring/ point-to-point-bus	tree and bus	point-to-point or limited multidrop
Transparency	yes	no—must be adapted via special interface	yes—on dedicated subchannels	yes—only on dedicated fiber
Data error rate	1×10^{-5}	1×10^{-7}	1×10^{-9}	very low
Noise vulnerability	yes	yes	no	no
Data security	low	moderate—tapper must know encoding scheme	very high—tapper must know channel and encoding	very high
Maintenance	difficult	very easy	easy	very difficult
Modifying network	new cable is difficult to install	fairly easy, but must watch limits on each cable	very easy	impossible today
Ductwork required	yes	yes	no—self-contained	yes—vulnerable to breakage
Wiring in place	likely	unlikely	unlikely	no

Source: Interactive Systems/3M

Finally, the i82586 serves metropolitan networks where standard Cable TV cable is used. The topology is typically a rooted tree and data rates are in the 128-kbit/s range for a 30-km radius.

In the broadband arena, Interactive Systems/3M, (Ann Arbor, Mich) introduced its Videodata LAN/1 last year. The LAN/1 concept uses a token-passing protocol between intelligent modems called network interface units (NIUs), which route terminal-to-terminal and terminal-to-multiple-host communications with direct addresses. The 3M engineers state that broadband networks offer particular flexibility in that they can handle virtually any type of electronic information including video, audio, and digital data. Table 1 compares the key considerations that a vendor might have when evaluating topologies. Several important broadband applications hold almost universal value regardless of the kind of installation. The broadband LAN/1 network serves as an information utility reaching even the most remote point of a facility or complex with full communication capability. And, the network can be monitored using an IBM PC that is equipped with the appropriate cards and software. LAN/1 applications include data processing, word processing, security systems, energy management, video training programs, production control, and electronic mail.

Broadband offers capabilities of particular interest to specific kinds of organizations. For example, in large academic institutions, video is increasingly used for instructional purposes, videoconferencing, and audio/video training. Without distributed communication, an instructor wishing to use a particular film or videotape in a classroom setting must arrange for pickup of the program, setup of equipment in the appropriate room, operation of the equipment, and return of the program material and projection device. Because of its high bandwidth, a broadband system makes it possible to build a central video distribution center that contains all of the campus audio/visual software and projection/playback equipment, and distributes signals over the cable network.

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TABLE 2

Worldwide LAN Installations Reported by Vendors

	Baseband	Broadband	Total
Vendors contacted with installations	28	7	35
Installed LANs worldwide as of 12/31/82 (as reported by vendors)	15,189	758	15,947
Installed LANs U.S. as of 12/31/82 (as reported by vendors)	10,488	645	11,133
U.S. percentage of total installed	69.0	85.1	69.8
Worldwide percentage installed work area LANs	62.7	20.0	60.6
Worldwide percentage installed facility wide LANs	37.3	80.0	39.4
Type of premise installations:			
Office	66.3	25.5	64.4
Factory	8.6	40.5	10.1
School/campus	13.6	12.5	13.5
Military	2.9	6.2	3.1
Research/engineering	8.6	15.3	8.9
Average number of nodes per installed network—worldwide	22	73	30

Source: International Data Corp, Framingham, MA

The LAN/1 uses a token-passing protocol between intelligent NIUs without need for a host computer. Communicating devices in the network are connected to a single coaxial cable through microprocessor-based NIUs which process point-to-point transfer of data packets. Transmission cannot occur unless an NIU has possession of the network token, which is passed sequentially from one NIU to the next in a circular manner.

The NIU handles all message processing and formatting tasks, traffic acknowledgment, and automatic contention for network access on an equal share basis. Channel capture is not possible, yet the system allows each node maximum throughput based on traffic levels.

The overall LAN/1 data rate is 2.5 Mbits/s for up to 10,000 devices—2000 on each of five channels. Terminal transmission rates can vary from 300 baud to 19.2 kbits/s. NIUs are available in two-, four-, and eight-port configurations.

LAN/1 operates on five channel pairs of 6-MHz bandwidth each. Transmission from NIUs takes place at the lower end of each channel. A channel converter connected to the cable intercepts all transmissions, converting them to a secondary frequency at the high side of each channel, and remodulating the data for retransmission. Redundant circuitry in the converter ensures dependable operation. The network frequency spectrum ranges from 53.75 to 276 MHz in five channels. LAN/1 works with either a mid-split or super-split broadband coaxial cable system. The total system also accommodates point-to-point data transmission, video applications, and selected audio applications.

LAN/1 hardware design includes a network monitor unit (NMU), which analyzes network performance statistically to facilitate routine maintenance and troubleshooting. NMU data enables system management to adjust channel assignments for maximum communication efficiency. This monitor unit consists of an IBM PC equipped with a two-port NIU and LAN/1 network monitoring software. In addition to its monitoring function, the NMU operates as a conventional user port on the network.

The total LAN/1 system accommodates point-to-point data transmission, and selected video and audio applications.

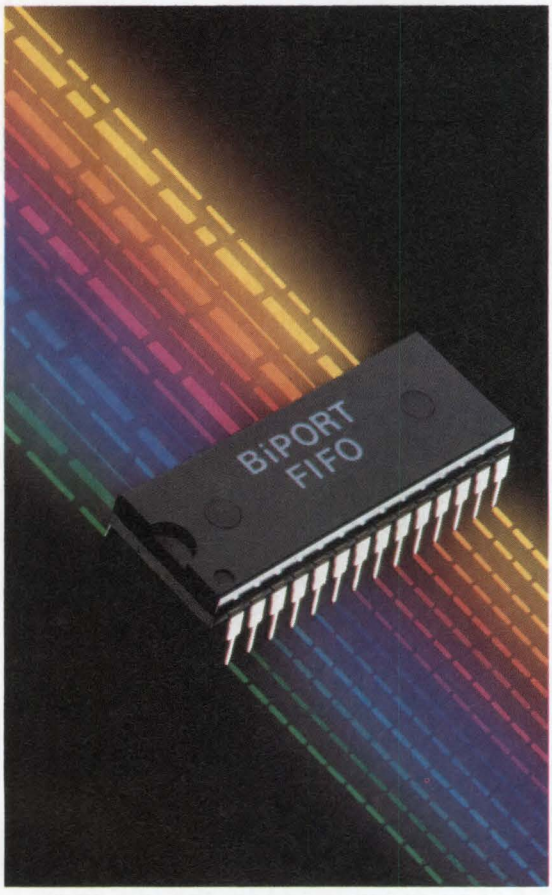
In an attempt to forecast market growth for both baseband and broadband LANs, International Data Corp (Framingham, Mass) has differentiated current LAN offerings into baseband and broadband topologies regardless of the kind of access method used. Table 2 lists the number of LAN installations by baseband/broadband orientation as reported by vendors to the market research firm.

Universal PC network

Microcomputers such as the Eagle, Kaypro, IBM PC, and other incompatible machines will eventually be linked to the same LAN. One of the first vendors to offer this capability is Alspa Computer, Inc (Santa Cruz, Calif).

The company first introduced Alspa-Net, a low cost LAN for its own microcomputer workstations and terminals last year. Alspa then developed interface cards and software enabling different brand name computers to become nodes in the network. The card and software are installed in the node computer, not in the system master, so the modification does not affect system reliability. Now, Alspa interfaces the IBM PC and its look-alikes with Alspa-Net. The interface card and software cost

SYNC THE UNSYNCABLE



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CIRCLE 81

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Alspa-Net is a linear bus network using a CSMA/CD protocol; each network supports up to 256 terminals, with any mix of master and slave workstations. Each intelligent workstation supports hard and floppy drives as well as serial and parallel printers, although any workstation can interact with remote peripherals in the network. TurboDOS, the network operating system, fully supports CP/M and MP/M software without modifications, and it allows the network to operate about 30 percent faster than a single computer using CP/M.

As the community of LANs merges with PBXs, more peripheral enhancements can be expected.

One of the most spectacular commercial developments in recent years has been the emergence and growth of personal computers. While companies hesitated to make large-scale capital investments in office automation, their individual managers and professionals found that low cost personal computers could be immediately justified by time savings and improved productivity. VisiCorp (San Jose, Calif) is often credited with igniting the explosion of personal computer usage in business when it introduced VisiCalc, the first "electronic spreadsheet" program, on the Apple II personal computer in 1979. More than 500,000 copies of VisiCalc are currently in use.

But both hardware and software technologies for personal computers have made dramatic advances. Several developments over the last two years have made personal computers as "workstations" and local area networking practical and economical. The IBM PC, introduced in 1981, was the first in a series of professional computers featuring 16-bit processors, main memory of 256 Kbytes or more, bit-mapped graphics displays, and hard disk drives. Taking advantage of these hardware capabilities, VisiCorp has developed VisiON, an integrated operating environment for concurrently running applications, with the window display and mouse features formerly found only in higher cost workstations such as Xerox Star. And 3Com Corp (Mountain View, Calif), using the latest VLSI chip technology, has developed an Ethernet controller on a printed circuit card small enough to plug into an IBM PC and costing less than $1000.

Last year VisiCorp, 3Com, and Xerox Corp (Los Angeles, Calif) teamed to combine these technologies in order to overcome some of the drawbacks associated with local area networking of personal computers. The low cost of personal computers, VisiCorp's VisiON, and 3Com's EtherLink card make it now possible to use local area networking with just two personal computers connected by a simple coaxial cable, for under $10,000. Yet, this configuration is fully compatible with a full-scale Ethernet-based integrated office system and a wide range of office products.

With the plethora of Ethernet-type LANs currently being touted, it is a wonder that users have a clear understanding of how to evaluate their choice. Enter the Nutcracker from Excelan (San Jose, Calif). It purports to solve two long-standing industry problems: how to debug and test very complex, high speed multiple-node networks (particularly their protocol software components) and how to characterize, or define the operating limits of, a given LAN configuration.

For example, to do a complete and thorough debugging and testing, a user must be able to get access to every packet on the network. Excelan claims that Nutcracker is the only commercially available product providing such complete observability. Its observation circuitry operating at 10 Mbits/s (approximately 1000 times faster than most communication instruments), allows it to see every packet, even in a fully saturated system.

Proprietary, high speed state machine logic with extremely powerful pattern recognition circuitry is the heart of the Nutcracker. The system also includes an 8086-based CPU and features over 900 Kbytes of RAM, a 20-Mbyte Winchester disk drive, and a 600-Kbyte floppy disk drive.

It is packaged as a single integrated workstation that includes a 12-in. monochromatic CRT with 82-key keyboard and an external 100-char/s matrix printer with graphics capability.

Thus, as the community of LANs merges with the colony of PBXs, more peripheral enhancements can be expected to be introduced at a feverish pace that can simulate, test, and expand individual systems. At the same time, interested parties will continue to strive to develop acceptable standards for interconnecting machines. It remains to be seen whether users will benefit in the long run from this fervent standardization activity, or settle instead for capabilities provided by the *de facto* standards that will be promulgated by the two giants—IBM and AT&T—to ensure compatibility with their respective installed base.

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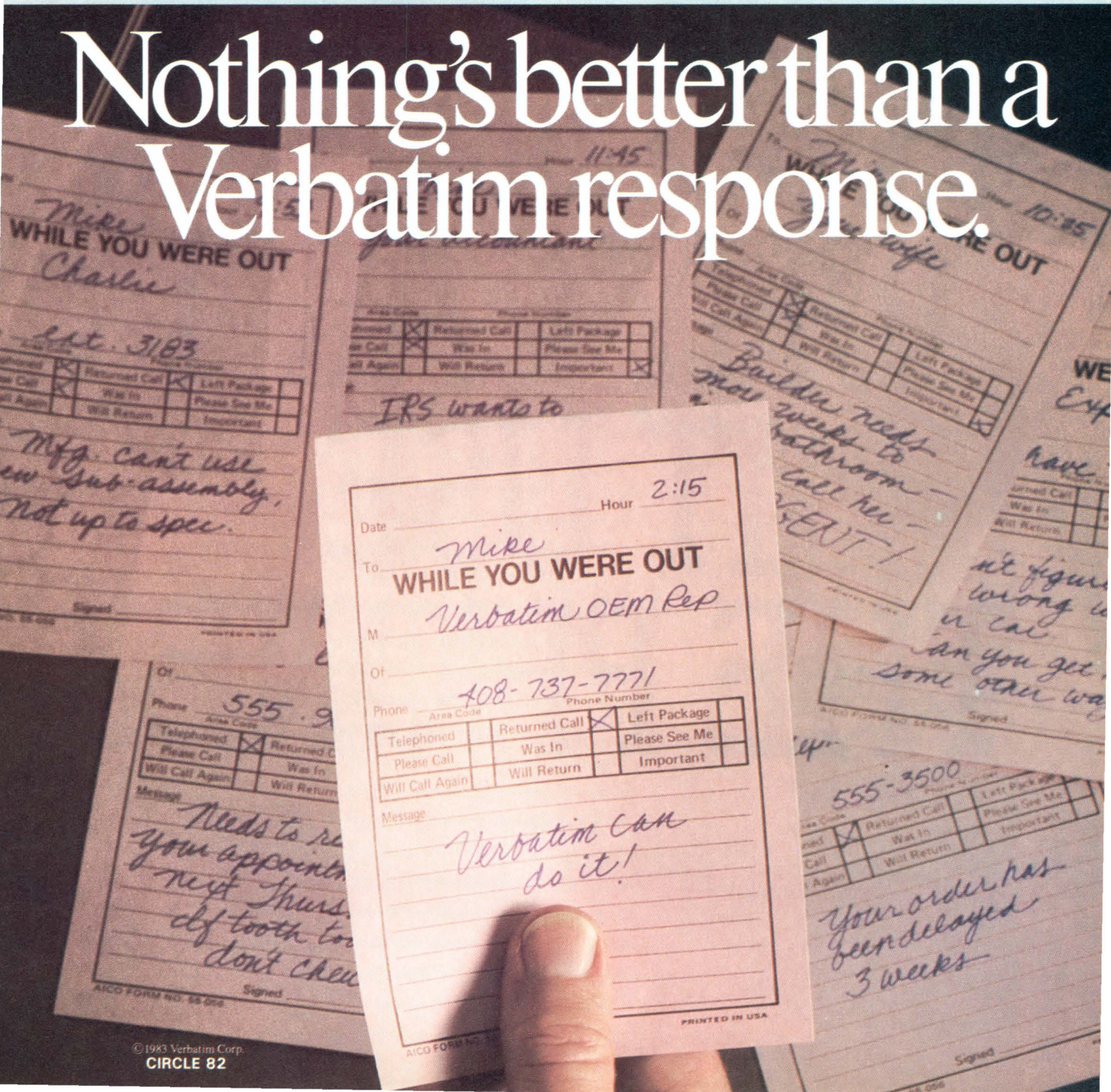

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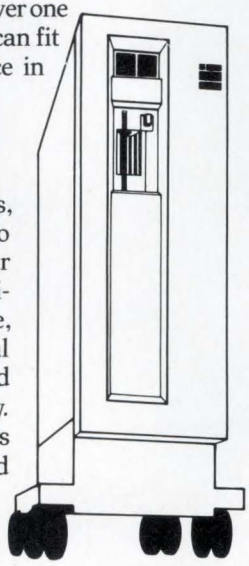

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STANDARDIZING UPPER-LEVEL NETWORK PROTOCOLS

Data communication networks will communicate more efficiently once standards are defined for the upper-level layers of the International Standards Organization seven-layer model.

by David Berry

The need for network interconnection standards has always been apparent. Over the past few years, the emergence of reasonably priced network technology for network connections has increased networking awareness. However, the debate over network technology itself and its access methods—broadband versus baseband, deterministic versus probabilistic, and token access versus carrier sense multiple access—has masked the importance of protocols for data flow control in networking.

As the number of real applications has grown, the International Standards Organization (ISO) has drawn on the experience of proprietary networks, the Advanced Research Projects Agency Network (ARPANET), and the public data network to summarize both known and anticipated networking requirements. ISO has done this by dividing network protocol functions into distinct groupings. This has resulted in a formal specification called the Seven Layer Model. The object of the model is to organize related groups that can be standardized independent of each other. This enables each layer to be defined with minimum reference to any other layer. Thus nodes in a network can be "constructed" with these layers and communication between nodes is ensured via peer-to-peer protocols between each node's layers. (See Panel, "Peer-to-peer is more than just here to here.")

A diagram of a node with the connection to the network medium at the bottom and the user interface at the top (Fig 1) illustrates the model. The functional groups are vertically arrayed.

The primary interface between the classical host functions and the network itself occurs in the network layer (layer 3). This layer allows each host to communicate directly with any other host connected to the global network. Routing and mapping problems are transparent to the network layer service users.

Prior to 1975, layers 1 and 2 were all that were usually specified. Provided that nodes were connected physically on the same network cable, this was adequate. With the development of more sophisticated packet-switching among heterogeneous networks, however, the need for more sophisticated routing protocols became apparent.

The network layer creates a route through the globally interconnected set of networks over which two hosts can converse. To avoid traffic congestion of faulty equipment in nodes of gateways in the path, this may need to be dynamically monitored. There are two basic types of network layers—connection-oriented (CO) and connectionless (CL). The former provides logical or virtual circuits for use by higher layers. The latter deals with each packet independently—ie, a datagram service.

In addition, traffic handling and packet fragmentation/reassembly may be required in order to use available physical circuits. The network layer

David Berry is section manager of the product planning division, Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94086, where he is responsible for network protocols. He holds a BS in physics from the University of Edinburgh, Edinburgh, Scotland.

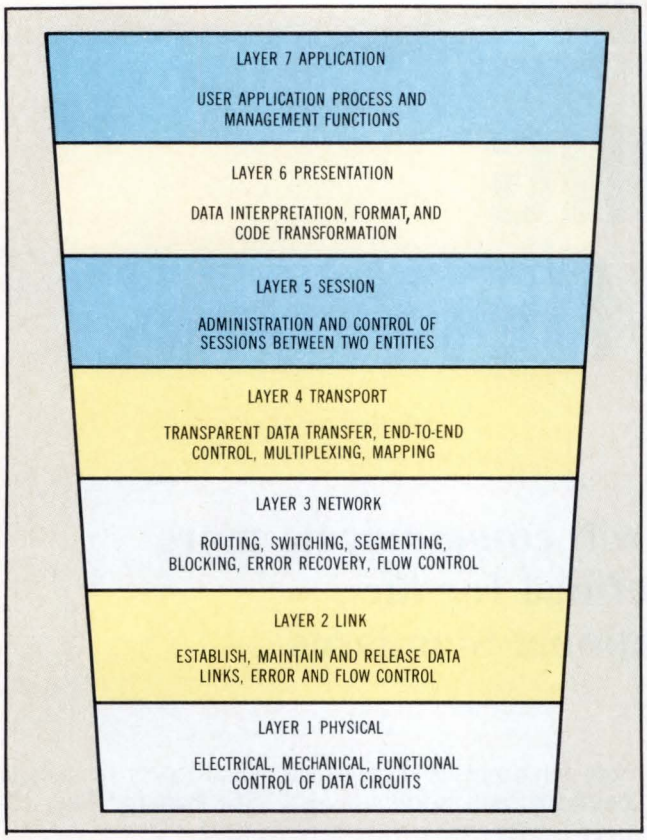

Fig 1 The seven-layer Open Systems Interconnection (OSI) model developed by the ISO serves to organize communication functions within a network (according to functioning) that can relate to each other. So far, the LAN world has standardized on the two lower levels. The challenge remains to find common goals for standardizing the other five levels.

service is closely related to that of the transport layer above it. (The two were once considered as a single layer.) One of the two layers must provide the virtual circuit over which packets are transmitted between hosts. Both implementations already exist. In public data networks, the X.25 protocol provides for virtual circuits and error detection. In the ARPANET system, the transport layer provides a (CD) service to the user on top of a less complex network layer than the X.25.

Currently, no obvious resolution between the two major types of network service is provided. A comparison of the two is shown in Table 1.

Datagram service is the most primitive of the two. Error and sequence control must be added by the transport layer in order to provide a reliable service to the user. In virtual circuits, much of the service is provided by the network layer itself. This is not always an advantage. When disk sectors are transmitted as packets with an embedded sector address, sequence is unimportant. In this case, delay of data to users because of sequence problems is inefficient and unnecessary.

The network layer itself usually consists of three distinct sublayers, shown in Table 2. Not all three sublayers need be present. Access protocols are not usually required on local area networks (LANs) since LANs tend to provide sophisticated medium access protocols as a part of the data link layer (layer 2). Packet-switched wide area networks (WANs), however, use complex protocols such as the X.25 at this point.

The harmonization sublayer is required only to connect two subnetworks with differing services, such as a CL LAN to a CO WAN. This can be very involved, and practical experience in this area remains limited. The internet sublayer is solely concerned with the problems of mapping and packet-routing between nodes.

Controlling data flow

The transport layer is the highest layer concerned with data movement across the network. It is intended to bridge the gap between the network layer service and the services required by the session layer. Therefore, the transport layer has end-to-end responsibility for reliable data delivery. It monitors and controls all traffic in and out of the node to ensure that no data is lost or garbled. Thus, while the lower layers are concerned with packet framing, transmission, and routing, the transport layer concerns itself with the following areas: virtual connections, the logical circuit between receiving and transmitting nodes; flow

TABLE 1

Virtual Circuit and Datagram Comparison between Network Service

Issue	Virtual Circuit (Connection-oriented)	Datagram (Connectionless)
Initial setup	Required	Not possible
Destination address	Only during connect	In each packet
Error handling	Transparent to host (done in the subnet)	Done by host
End-to-end flow control	Done by the subnet	Not available in the subnet
Packet sequencing	Messages passed in order sent	Messages passed in order received

TABLE 2

Network Sublayer Functions

Sublayer	Name	Function
3a	Access	Provides the interface to the data link layer
3b	Harmonization	Provides a mapping of the services available to give a common set to sublayer 3c
3c	Internet	Provides the routing and address mapping required to cross the network

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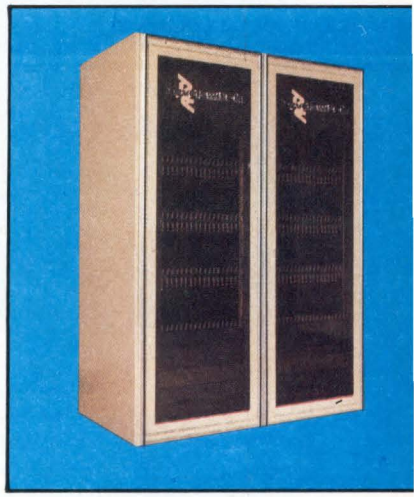

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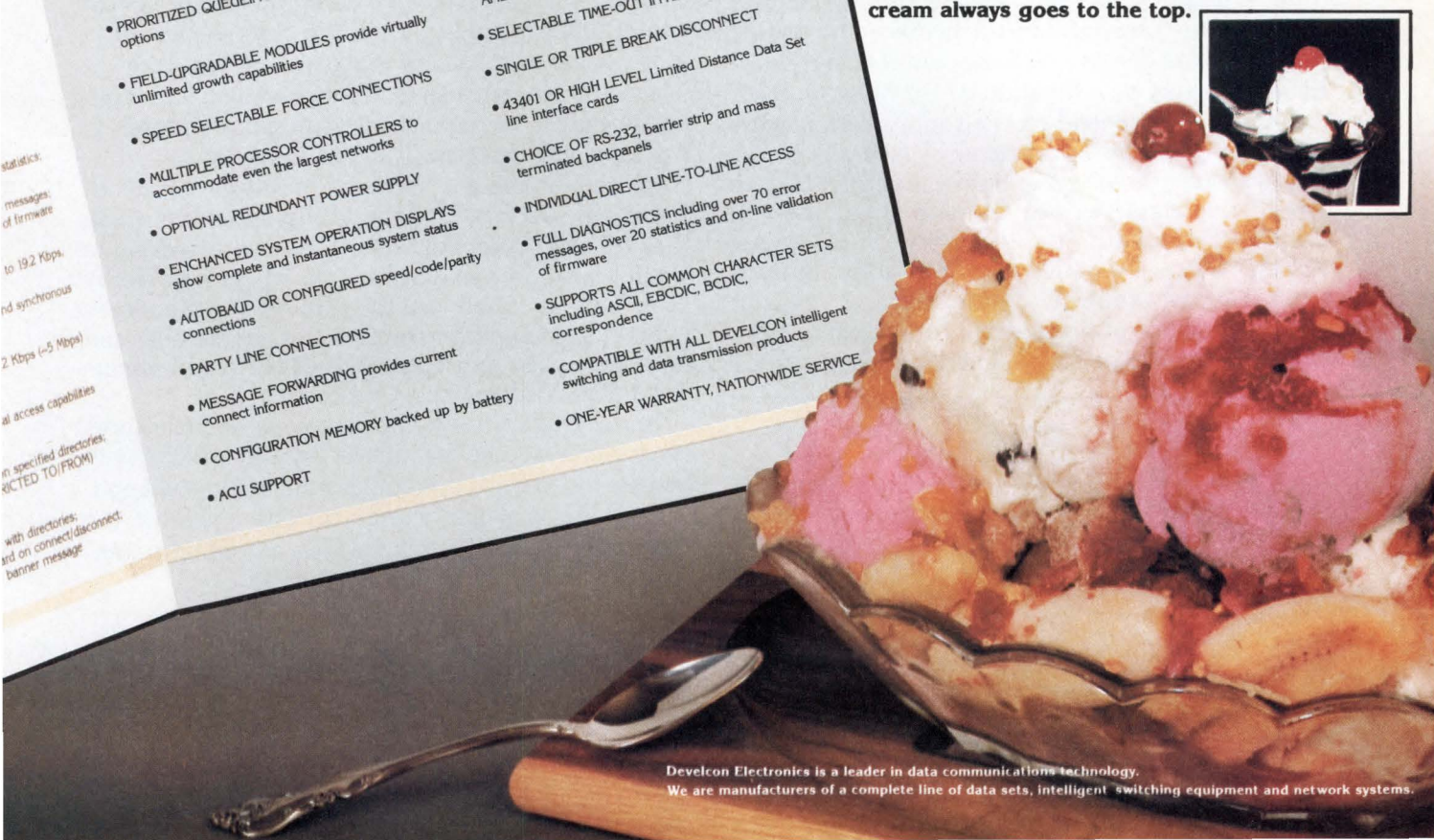

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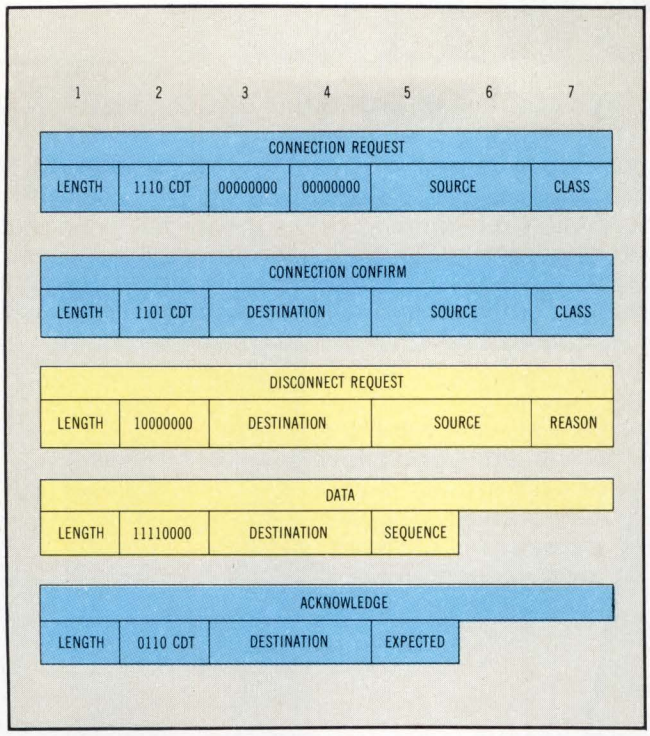


Fig 2 The transport level is the highest level that concerns itself with the movement of data across the network and where the real problems of the OSI must be solved. The OSI transport protocol standard headers shown here are compatible with most major standards organizations.

control, monitoring the amount of data not yet acknowledged as received; error detection, the ability to monitor the packet sequence for missing, duplicated, or missequenced packets; and error recovery, the ability to rectify errors detected by this or lower layers without host intervention.

To a large extent, the degree of complexity required in the transport layer depends on the quality of the network across which the data is being moved. Reliability may be a function of the network itself, but it may also depend on the sophistication of the protocols being run at the network layer. To reflect this, transport service is generally made available in one of five classes: Class 0—simple, for use with Comite Consultatif Internationale (CCITT) networks; Class 1—basic, not yet fully defined; Class 2—flow control, limits number of outstanding acknowledgements for packets sent; Class 3—error detection, detects mishaps in the flow; and Class 4—error recovery, corrects mishaps automatically.

TABLE 3
Transport Layers

Standards Body	Transport Protocol Standard
ISO	DP 8072
ISO	DIS 8073
ECMA	72
DoD	TCP
CCITT	So70
NBS	TP

The transport service provides a pair of queues between two users that carry both data and control information in a duplex manner. It provides this as a transparent service, which then removes any need for users to be concerned with the physical data transmission.

Examples of transport layer protocol implementation are the transmission control protocol used in ARPANET, the network services in DECNET, and transport control systems in systems network architecture (SNA). None of these is normally used with a CO network layer, as in an X.25 network. This highlights the main division in the current debate on the transport layer. An example of the headers used in the ISO transport protocol standard are shown in Fig 2.

With transport layer protocols, two different approaches have been taken. On the one hand, packet-switching proponents, headed by CCITT, have approached networks from the point of view of existing telephone networks. Much of the work to be done in the transport layer is already incorporated in the virtual circuit protocols of the X.25 network layer. Some vestigial functions are required, such as reset recovery, since the X.25 protocol allows asynchronous resets to the connections.

On the other hand, those involved with computer networks require more transport layers. The main driving forces behind this approach were the National Bureau of Standards (NBS) and the ARPANET community in the U.S., and the European Computer Manufacturers Association (ECMA) in Europe. The majority of computer and system manufacturers are supportive of their efforts for a more complex protocol since this is the layer at which the real problems of open system interconnection must be handled. The major standards at the transport layer are listed in Table 3.

Although Table 3 seems to imply a variety of standards, the ISO, ECMA, and NBS standards are in fact virtually compatible. At the time of writing, a single transport standard will shortly be ratified by ISO. This is based on the NBS/ECMA standards (which are compatible in all but some details) and includes a class that covers the CCITT requirements for a truncated transport protocol.

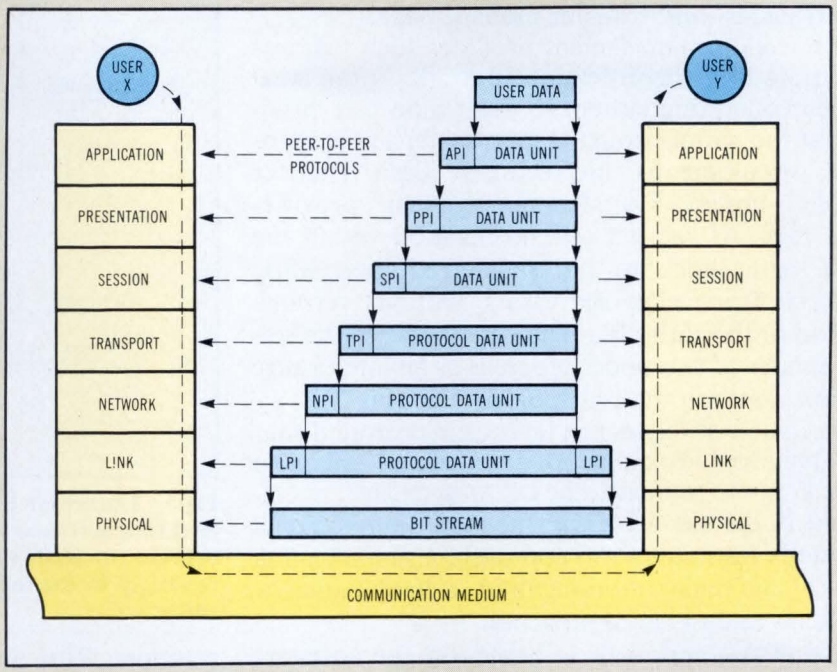
In the attempt to define protocols, the transport layer appears to be the highest layer at which it will be possible to find common ground among all applications for a single standard. This explains the comparative rapidity with which a common standard for this layer has been achieved.

Making the connection

The session layer functions are still the subject of major discussion in networking. Several existing networks (such as the ARPANET) dispense with the

Peer-to-peer is more than just here-to-here

The seven-layer OSI model serves as a road map for network users. Network communication begins when the user in one node addresses the top or seventh layer of that node. This layer then communicates with the corresponding layer in the other user's node with some form of peer-to-peer protocol. This is accomplished by having the seventh layer use the services of the next lower layer, much as the user makes use of the seventh layer. This lower layer, in turn, corresponds with its opposite peer layer by means of its own peer-to-peer protocol, which is transported using the service of the next lower layer.



The importance of this layered arrangement is that functions associated with a network connection are grouped in an ascending order with respect to the host, and in a descending order with respect to the medium. The decoupling of layers allows a wide degree of flexibility to the network system designer in choosing the functions needed layer by layer. Each functional group is concerned only with those tasks associated with the layer in question. A node can therefore be assembled in a highly modular fashion.

Functions that are associated with lower layer protocols include packet framing (grouping of characters and messages), error control (detection of erroneous data or formats), data encoding (bit coding of the characters being sent), and frame addressing (routing of frames to destination nodes). These functions are typically concerned with providing access to the transmission media.

Besides the required protocols to communicate between the same layer in different nodes, protocols are also needed for communication between different layers in the same node. One layer interacts with another via a protocol in three ways: peer-to-peer, where a layer communicates with the same layer of another node; service provider, where a lower layer provides a service to the next higher layer of the same node; and service requester, where a higher layer uses the services provided by the next lower layer of the same node.

To date, most of the network protocols that have been considered for standardization are peer-to-peer protocols. Information is passed from peer-to-peer by attaching a header to the beginning of the data packet that is to be transmitted. Each layer encodes its header according to its specification (see Figure.)

Each layer provides a service to the layer above and expects service from the layer below. It receives data units from the layer above, along with interface control units that indicate the service to be performed for the layer above. The data units will already contain appended headers with protocols from the higher layers. This is completely transparent to the lower layer—ie, the lower layer has no understanding of the protocol used by the preceding layer and has no way to distinguish upper-layer protocol headers from the data proper. The lower layer then operates on the data packet as required. It might, for example, encrypt the data or split the data into packet lengths acceptable to the network to be traversed. Finally, it will pass control to the next lower layer by means of another interface control unit. The header now appended to the packet is transparent to the next lower layer.

Upon receipt of the packet at the destination node, a similar process is performed in reverse order. Each layer examines the packet area where it expects to find its header. This is interpreted according to the protocol specification for that layer, and any remaining part of the packet is passed up to the next layer for further examination as required.

Not every packet originates or terminates in the application layer. Also, several physical packets are usually required to transfer one logical packet. The actual ratio depends on a number of factors, such as the protocols in use, the error rate of the network, and the number of fragments into which a packet must be broken.

The logical mechanism by which protocols are transmitted across the network is a set featuring commands known as primitives. These are encoded in the appropriate packet header. Each primitive is generated by a layer within a node and transmitted to its peer in the other node by means of the services provided by lower layers. A given layer invokes these services by passing a primitive, such as a REQUEST, to the lower layer. This appears in the destination node as a REQUEST being passed up to the peer layer by the lower layer. Responses are passed back in a similar manner in the opposite direction. Thus, orderly transactions are ensured.

session layer altogether. The basic session layer functions manage data transfer (using transport service to move raw data), and add three categories of user-oriented services: connection management, data transfer, and transfer management.

Connection management provides such features as remote user identification that allows the local resident operating system to determine user privileges at the remote node. Data transfer service provides simultaneous bidirectional data transfer between nodes. Transfer management provides some form of subunit synchronization within the entire data block to be transferred, permitting recovery from network errors without retransmission of the entire file. Dialogue between the session entities of two nodes proceeds as an interchange of data units via the transport service (Fig 3).

Discussion of the session layer centers around four main philosophies: the ECMA approach, as embodied in the ECMA-75 standard; the CCITT approach, as embodied in the S.62 standard; the American National Standards Institute (ANSI) approach, a simplification of both; and the ISO working draft, a combination of the ECMA and CCITT approaches.

The ECMA approach is based on the software architecture of mainframe session functions. It attempts to provide the user with a more generalized control of the transport services of the layer below. The functions provided include reliable, organized, and synchronized data transfer; four distinct service subsets; and an optional data quarantine function.

In addition, the commands that are used by the protocol can be classified into four groups: session (connect/release/abort); data (data/expedited); synchronization (sync/resync/endDU/tokens); and quarantine (deliver/cancel).

The CCITT approach is based on the requirements of the teletext service and makes a number of less general assumptions about the application than the ECMA approach. It is designed to operate on a public data network and assumes that the major use will be in a teletext environment. It has only one distinct class of operation. Within this class are a number of possible commands, divided into two groups—session commands and document commands. These groups correspond roughly to the session and synchronization commands of ECMA-75.

The ISO approach, as characterized by the last meeting of the TC97/SC16/WG6 committee in Mar 1983, has been to combine all of the facilities of both the ECMA and CCITT approaches. This has resulted in a somewhat cumbersome specification that includes all of the command types from ECMA-75, plus an activity management (ie, document control) command group, plus exception reporting, capability data exchange, and typed data.

This complexity has not yet been well received in the U.S. and ANSI has yet to come to a definitive

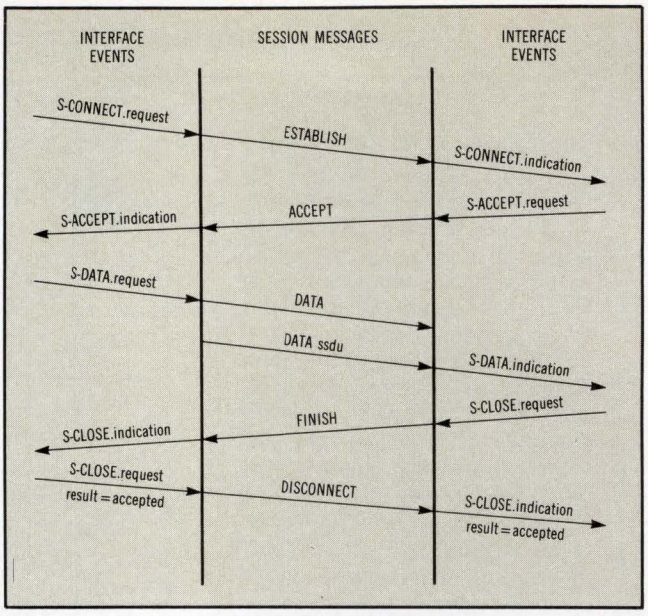


Fig 3 The session level manages the data that the transport level transmits in an unmessaged state. The dialogue between two session levels follows four different approaches advocated by the following organizations: ANSI, ISO, CCITT, and ECMA.

position. The group has neither issued a draft standard of its own nor modified one of the above. There is unlikely to be agreement on the basis of any of the above due to the feeling among major U.S. manufacturers that the session layer does not require this degree of complexity and corresponding overhead. The likelihood of a unified session standard being available in the next year is not good. It may even prove necessary to agree on multiple standards that are appropriate for differing applications.

Speaking the language

While layers 5 and below deal with the transmission of data units that are transparent to them, the presentation layer is more concerned with network user interface. As the name suggests, the presentation layer presents the user with data transferred on the network in an orderly and unambiguous manner.

This layer is therefore application-specific, and any comprehensive standard that will define all its functions in one protocol is unlikely. Currently, a number of nonoverlapping protocols for the presentation layer are being defined. These include virtual terminal functions; video/teletext; packet assembly/disassembly (PAD) functions; and text compression and character coding.

The most comprehensive standard for the presentation layer so far is the ECMA-86 standard on generic presentation service (GPS). The standard describes a model of the layer and the services it provides. It defines the GPS as a set of common service facilities that are dependent on the underlying session service to establish and maintain contact between users of the presentation services. Once

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contact has been established, all communication between the users takes place according to the GPS protocol, known as the p-service. Access to the p-service by the user is performed by an implementation-dependent interface.

Within the GPS, many service subsets are possible. These correspond to applications, such as file transfer or data base management. A specific presentation service and a protocol used to provide it should be defined for each application.

Virtual terminal protocols (VTPs) are a subset used at the presentation level. An example is the ECMA-88 basic class virtual terminal, which is a subset of the ECMA-87 standard generic virtual terminal description of a virtual terminal service. Virtual terminals are a convenient construct in networking.

In practice, both the terminal and the application have access to the data being transferred as a two-dimensional array. The array consists of a number of cells that can be accessed (read from or written to) by either. The main difference is that the application has direct access to the data structure, while the terminal user views it through the display device and modifies it using the keyboard.

The application and the terminal communicate by means of character strings. A string is entered via the keyboard, which is passively viewed by the application until it can be interpreted as a command or response. The application then takes over and performs the appropriate action. The result of this is then communicated to the operator by means of a message entered in the data structure.

Since the terminal and the application both have their own views of the data structure, it is the task of the virtual terminal protocol to synchronize their communication. It negotiates the compatibility of the data structure, and establishes a set of functions to be implemented in a standard fashion. However, it does not address the exact nature of the terminal itself.

In addition, the upper interfaces of the VTPs to the terminals concerned are nonstandard. However, the interface to the session layer and the protocol used to communicate with another node follow the VTP standard.

Teletext and videotex are examples of presentation layer functions. Both have their origins in the idea of a low cost information service available to both the home and the business market. Information in the form of both text and graphics is disseminated by the network to some kind of display, usually a modified TV set.

The distinction between teletext and videotex is in the degree of user interaction. Teletext permits almost no control over the selection of the data transmitted. A number of information screens are repeatedly transmitted, and the user may select one to display. Videotex users equipped with a small keyboard can select from the data base available on the network. In real applications, these distinctions become blurred, and teletext and videotex are generally grouped together. Moreover, they provide a spectrum of services ranging from one-way transmission from dumb terminals up to enhanced services available on sophisticated two-way transmissions from external data networks and intelligent terminals.

Examples of teletext in use today are the Ceefax and Oracle systems provided by the two television networks in Britain, and the Antiope in France. The current market in Britain is the largest in the world for teletext and provides 100-page magazines via the blanking intervals (the period of time when the electron beam is being repositioned at the top of the screen for another pass) in ordinary TV broadcasts.

Both teletext and videotex point the way to electronic information delivery to the home and office as a matter of routine. Limited bandwidth broadcast systems are excellent media for news, sports, and entertainment guides. More sophisticated interactive systems can also offer teleshopping and electronic banking.

Both systems require that a universal standard for transmission of the information is available. This is less of a problem with text displays than it has been with graphics. However, within the last year, there has been a considerable increase in support for the North American Presentation Layer Protocol Standard (NAPLPS). This is a method for encoding visual information in a standard and compact manner. Graphic and textual information

Limited bandwidth broadcast systems are excellent media for news, sports, and entertainment guides.

can be represented in a variety of modes, colors, and styles. In addition, facilities are provided by the protocol for the user to interact with the two-dimensional display in a very flexible manner.

NAPLPS is one of the three contenders for a presentation layer standard for a graphics protocol. Whether the European Conference Éuropean des Postes et Télégraphique (CEPT) or the Japanese Captain will be incorporated in, or simply supplanted by, NAPLPS remains to be seen.

The PAD functions of the presentation level protocols historically preceded the ISO model. For that reason, PAD is something of a misfit in that it belongs conceptually in the presentation layer, but operates as if it were a part of the network layer.

The PAD was a parametric approach to a virtual terminal taken by the CCITT in their efforts at standardization. It contrasts with the virtual machine approach described above by using a predefined set of parameters to define all terminal characteristics.

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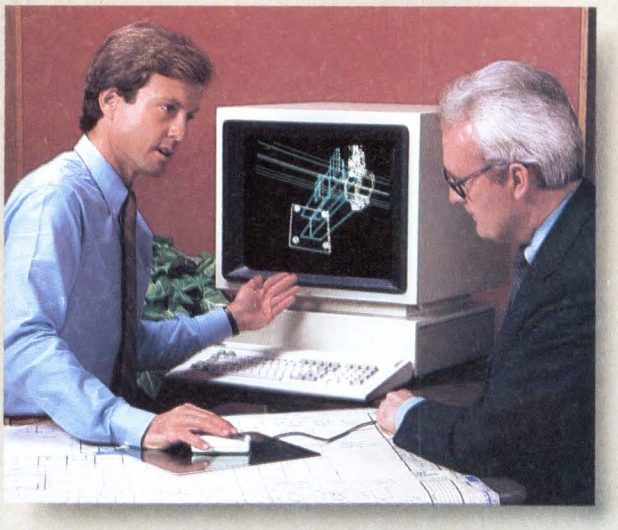

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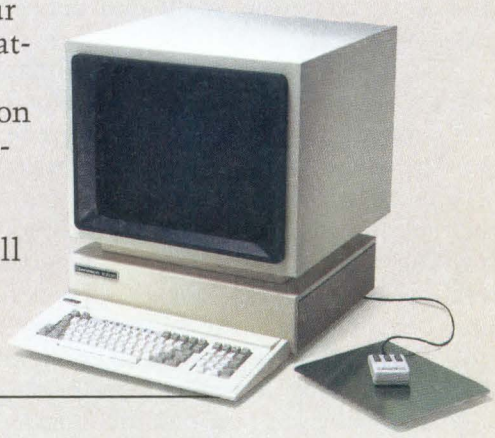

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A set of these parameters is negotiated for each connection made. This is easy to implement, usually as a table-driven scheme. Additionally, the standards in general use for these PAD functions are all from the CCITT "X" series. They include X.3, X.28, and X.29.

The text compression and character coding parts of the presentation level protocol are terms used to describe the encoding of data to be transferred on the network and its subsequent decoding at the receiving node. This can usually be related to encryption.

Text compression attempts to reduce the amount of traffic on the network by encoding repetitive strings of characters—eg, by putting blanks in a more compact form. The strings are then expanded to their original format at the destination.

Character coding is used when communicating between hosts that use incompatible coding for their data, such as extended binary-coded decimal interchange (EBCDIC), and ASCII 7 bits. There are few true protocols involved in either character coding or text compression, and little has been done toward universal standardization.

Talking to the user

Of all the layers involved in networking, the application layer provides the most diversity and yet the least opportunity for standardization. It is the one most intimately concerned with user processes. The term "user" is generally taken to mean any user process or user machine, not necessarily a person using the system directly. The diversity is particularly true in the present environment where a multiplicity of systems exists.

The boundary with the presentation layer separates network designers from true network users. This layer has received less detailed attention than any of the layers, in part because of the lack of motivation towards standardization. The activities associated with the application layer are usually considered to include file transfer control; data base management; remote job entry (RJE) and data handling; electronic mail; and network operating systems.

File transfer protocols (FTPs) handle files that are accessed by remote users in a standard fashion. This differs from local file management provided by the operating system. The operating system creates files with unique names within the local system and manages them according to local conventions. For global networks, a network-wide file management system needs to be defined. In the local environment, the most common operation is file access. On the network, it is file transfer.

The criterion for file transfer is to establish network-wide conventions for unique file naming. The FTP identifies both the source and the destination, and locates the file(s) involved. Details such as privilege of access, code encryption, or compression and merging must be standardized.

After the initial control phase, the data transfer takes place with associated control between the two servers involved. In the transfer of long files, the session layer services can be vital to efficiency. Should an error occur during file transfer, the session protocol should be capable of establishing the most recent checkpoint up to which the data was correctly transferred and of restarting the transfer from this point, rather than from the beginning of the file.

The application layer provides the most diversity and yet the least opportunity for standardization.

Currently, the closest thing to a standard in this area is an ISO FTP. It includes a logical model to help define the concept of virtual filestore that enables access and file management in the global network as well as the local environment. As a result, nonhomogeneous processes will be able to function interactively.

Database protocols are a generic grouping that includes such specific examples as RJE and interprocess communication protocols. The need for data bases was advocated long before the advent of networking and the availability of lower cost distributed systems. Many applications have multiple geographic locations where data must be available and operated on. Relational data bases have evolved to meet the requirements of query processing, concurrency control, and the relational distribution problem. None of this has yet been standardized for the networking environment.

Communication paths between data bases can either exist within a single-user system, or can be used to connect several user systems over some form of network. In a distributed system, the distinction between a remote and a local connection becomes trivial. Any protocol standard for distributed data bases must control both the access and any associated communication in an orderly manner. Processes can be located either in a single system or across several systems. In the latter case, the liaison must be established in order to exchange information, whereupon it makes no real difference whether the process accessed is local or remote.

The RJE protocols are used to enter jobs or batches of jobs to a remote computer. These will access the network through some form of VTP at the presentation layer. It requires a degree of high level activity, with program files being transferred by an FTP. Little has yet been done to achieve standardization in this area.

The details of how FTPs, distributed data bases, and RJEs will interact in the networks of the future

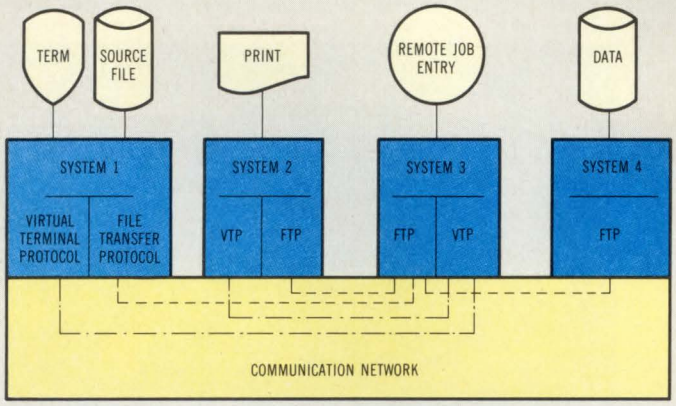

Fig 4 The application level is concerned with the end-user applications and is the least likely to become standardized. Five generic application activities are handled at this top level: file transfer control, database management, RJE, electronic mail, and network operating systems. For the most part, the transactions are handled through file transfer protocols (FTPs).

is a matter of speculation. A general scheme is illustrated in Fig 4.

Electronic mail is the means whereby messages may be exchanged by the same network users. This has received considerable attention recently. It is also known as computer-based message systems and is conceptually divided into three sublayers within the application layer: user agent sublayer, which provides message preparation tools; message transfer sublayer, which provides transfer mechanism; and reliable transfer sublayer, which controls error recovery. While a number of vendors such as MCI Communications Corp (Washington, DC) provide electronic mail service, little progress has been made towards a standard.

The remote job entry protocols are used to enter jobs to a remote computer.

Business data exchange is an area in which ANSI is attempting to reach a standard protocol agreement. The series of X.12 standards attempts to define protocols for the following common business issues: purchase order transactions (X12.1).; invoice transactions (X12.2); and data elements (X12.3). Although these three standards have been officially approved, they have not yet been applied widely.

Network operating system is a generic term for the concept of distributing the functions of an operating system among the nodes of a network. It is a logical extension of hardware distribution implied by networks to the software itself.

Each host continues to run its prenetworking operating system, but the network operating system is implemented as a collection of user programs distributed among the nodes that manage data and communication in an orderly and uniform manner. Little has been done in this area, but the problems are closely related to those of a distributed data base. Thus, the functions of a node can be efficiently organized by adhering to the specifications of the seven layers of the OSI mode.

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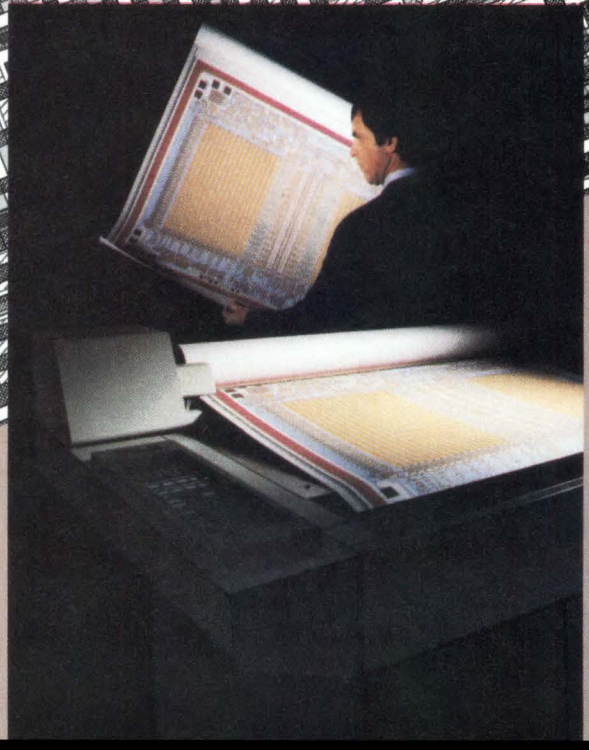

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PBX-BASED LANs: LOWER COST PER TERMINAL CONNECTION

Universal digital loop transceiver chip set offers attractive alternative to coaxial and fiber optic based local area network.

by Henry Wurzburg and Steve Kelley

To date, the major emphasis in local area networks has been on systems that provide a very high speed communication link by means of a single fiber optic or coaxial cable with multiple drops. These systems have installation costs that are attractive because they require the addition and routing of only a single cable throughout the office. In addition, these systems, whether they are the contention/arbitration type (such as Ethernet), or the token-passing type, are highly efficient at passing large data blocks at a very high speed. As such, they are well suited for communications between large data processing/storage machines. However, since their goal is to economically provide access to as many office workers as possible, these systems still have a few disadvantages.

Although most present and proposed local area networks (LANs) boast 10-Mbit/s data rates, they only have effective data rates of 40 kbits/s when fully loaded. This ignores additional slow-downs caused by contention. In addition, the maximum number of user drops is limited, in some cases to 256 or lower. Increasing the capacity requires the addition of more cable and the provision of gateways between systems. This adds considerably to system expense. Also, much intelligence must be provided at each drop in the system to handle data switching and protocol, which further increases cost.

However, many offices already have most of the equipment needed to form a LAN that has the advantages of low cost, easy expansion, and simple installation: the digital telephone switch or private branch exchange (PBX). These switches digitize the analog voice as it comes in from each phone and route it throughout the switch to its destination at 64 kbits/s. Virtually every office worker has a telephone. Therefore, widespread user access to such a PBX-based LAN is established with the existing installation of twisted-pair wiring. And, since the digital PBX is inherently a data routing switch, minimal intelligence is required at each termination of the LAN. The use of existing telephone wiring, easy expandability, and the low complexity required at user equipment interfaces result in a digital PBX-based LAN that has a considerably lower cost per connection than other approaches (Fig 1).

The PBX's ability to directly handle digital data is a comparatively recent development. Traditionally, analog telephone signals have been switched and transmitted using elements called crosspoints. Although implemented with various technologies, all crosspoints are designed to switch and propagate .3- to 3-kHz audio signals with small and

Henry Wurzburg is manager of Hi-Rel & Telecom Systems Design, and a member of the technical staff at Motorola, MOS Integrated Circuits Group, 3501 Ed Bluestein Blvd, J6, Austin, TX 78721. Mr Wurzburg holds a BSEE from the Georgia Institute of Technology and an MSEE from Arizona State University.

Steve Kelley is Hi-Rel & Telecom design manager and a member of the technical staff at Motorola's MOS Integrated Circuits Group. Mr Kelley holds a BS and an MS in electrical engineering from Cornell University.

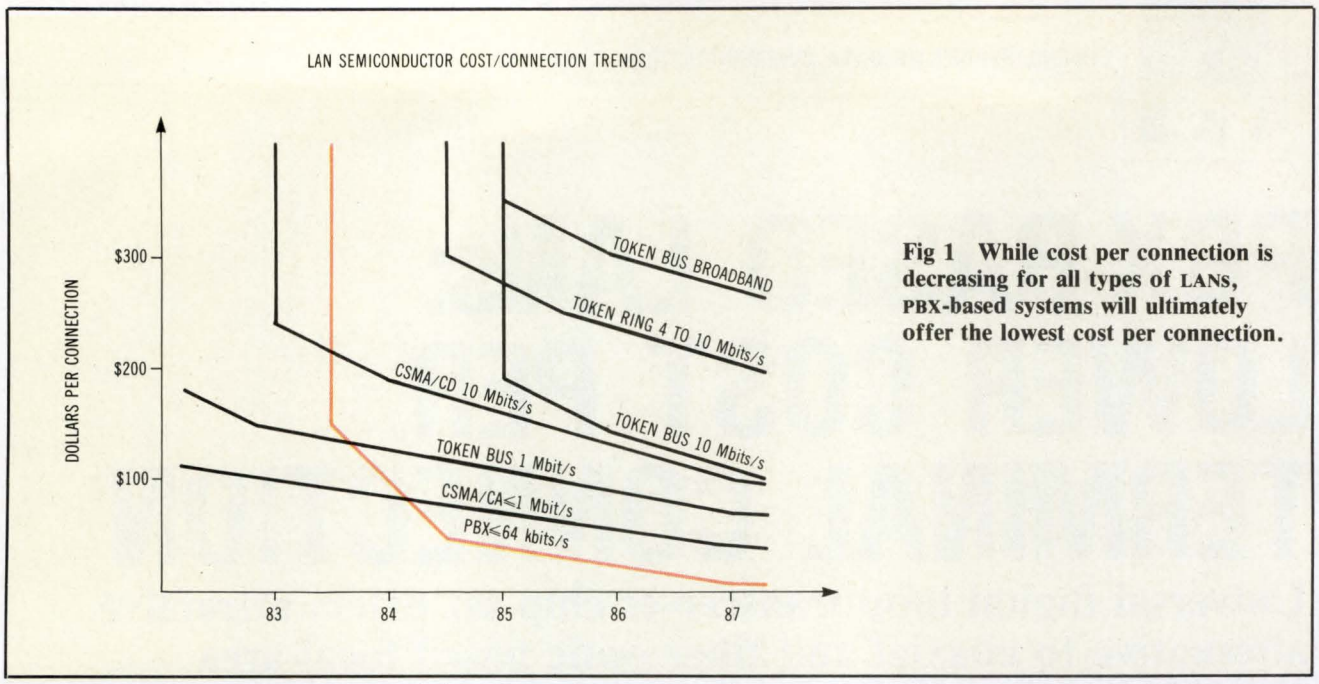

Fig 1 While cost per connection is decreasing for all types of LANs, PBX-based systems will ultimately offer the lowest cost per connection.

controllable losses. A standard dial-up phone connection supplies the user with a .3- to 3-kHz full-duplex audio channel that is adequate for voice and audible control tones, but will not pass either dc contact closures or digital data streams. The need and convenience of using the dial-up voice network for data transmission has long been recognized. Today, this need is served with modems.

A modem converts serial digital data into audible tones that are within the .3- to 3-kHz band. In its simplest form, a "1" is signaled with one tone frequency while a "0" is sent with another. However, the 3-kHz audio bandwidth constraint limits the toggling rate between audio symbols (bauds) to about one-half of 3 kHz, or 1200 Hz. Usable data rates vary from 300 to 4800 bits/s, depending on the complexity of the modem design, and the separation method used to let data pass in both directions. Modems will continue in widespread use because they are universally compatible with the dial-up network's analog channel capacity. However, during the last decade, the digital telephone switch has emerged as a means of implementing analog channels. Where that technology is used, it is now possible to bypass the modem and its speed limitations by employing the inherent digital capacity of the switch.

The digital switch is born

The 3-kHz audio channel on which all telephone equipment is standardized can be implemented by digitizing voice at the channel ends and producing interconnectivity with memory and logic instead of crosspoints. The input audio signal is sampled at 8 kHz and each sample is coded into an 8-bit byte using an amplitude compression standard called Mu-law pulse code modulation (PCM). The result is that an active audio port inputs 8000 eight-bit words/s to the digital PBX. Thus, a 64-kbit/s data stream replaces the 3-kHz audio channel internal to the digital switch.

The voice data bytes are typically time multiplexed into 2.048-Mbit/s streams consisting of 32 eight-bit conversation time slots. Programming port A to read port B's time slot, and port B to read port A's time slot at continuous 8-kHz intervals accomplishes a bidirectional telephone connection through the digital PBX. A central call processor does the port's time-slot programming based on dialing commands input from the ports on separate signaling channels. Thus, the digital PBX is nothing more than a programmable and fast read/write memory placed between ports that digitize and undigitize incoming and outgoing audio signals.

The speed difference between using a digital switch's ports instead of a modem can be illustrated by the following example. Suppose a dial-up data user unknowingly encounters a digital PBX. The "A" user supplies a data stream at some 1200 bits/s to a modem that converts the data to 1200-Hz analog symbols for the PBX. The digital PBX's port converts those 1200-Hz symbols to 8000 eight-bit bytes/s, which are placed in its time slot and read by port B. Port B reads 64-kbit/s data, puts out 1200-Hz analog symbols, and user B's modem decodes the symbols into 1200 bits/s. If users A and B only knew how to access port A and B's time slots, this whole transaction could occur 50 times faster with much less hardware.

In a typical application, the digital PBX switch and its time slots are centrally located on an office campus. They are also connected to telephones that are remotely located by distances of more than a mile via bundled twisted-wire pairs. The PBX supplies dc power to, and exchanges transmit and

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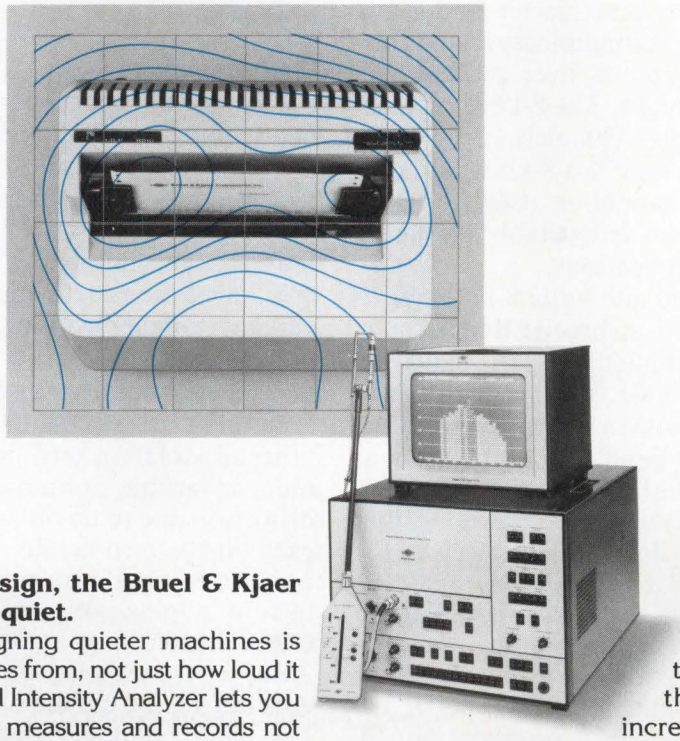

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CIRCLE 93

receive 3-kHz analog signals with, the telephone set over a one twisted (or untwisted) pair of 26-gauge or larger wire. Coincidentally, those wire pairs already exist near almost every potential dial-up data user in an automated office. If the 64-kbit time slot could be remoted out to the telephone set on the same twisted pair, access to a relatively high speed data switching facility would be achieved at far more locations than the most elaborate ring or bus coax scheme one could ever imagine. Due to the sheer volume of potential applications, the transceivers used to upgrade the miles of twisted pair to full-duplex digital service must be inexpensive and easy to use.

This is precisely the intent of a new IC family introduced by Motorola in the first quarter of 1984. The universal digital loop transceiver (UDLT) family consists of three CMOS devices. Two of these are the master and slave UDLT devices. The third is a data-set interface (DSI) device that provides a RS-232 to time slot data conversion so that existing data equipment can be interconnected to these new transceivers without modification.

Chips provide for digital PBX

The MC145422 and MC145426 master and slave UDLTs are designed to communicate at a full-duplex data rate of 80 kbits/s over twisted pair from 0 to 1.25 miles in length. The 8-kbit total has three basically independent channels: a voice or data channel of 64 kbits, and two 8-kbit channels. Typically, one 8-kbit channel is used for PBX signaling, while the second is available for up to 9600-bit/s use in data applications.

Since the PBX must read and write 8-bit bytes to and from each active port at precise 8-kHz intervals to support voice communication, the baud rate of the UDLTs is set at 256 kHz. The master UDLT at the PBX port receives an 8-kHz sync pulse from the PBX and transmits a 10-baud (8 + 1 + 1) burst at regular intervals. This burst arrives at the slave UDLT up to 12 μs (3 baud) later due to propagation delay on the wire. The slave totally receives the burst between 10 and 13 baud after the master's sync. The slave UDLT then responds with its 10-bit burst after a 4-baud delay for transient settling. The return burst arrives and is received by the master from 14 to 17 baud after the end of the master burst at the slave. This is no more than 30 baud after the master's original sync pulse. Since there are 32 baud periods per 8-kHz frame, the round-trip propagation time can be greater than 6 baud without error.

This full-duplex transmission method is called ping-pong, and conservative wire propagation data puts the ping-pong range at over 1.25 miles. The master/slave relationship between the PBX and the telephone set provides the set with precise frame synchronization such that the PBX time slots appear to have been remoted to the slave. Thus, the synchronous data device can be directly connected to the UDLT, while async to sync conversion is handled by the DSI chip, which is discussed later. The UDLT transmission technique uses one baud, or symbol, per bit, but the nonreturn to zero (NRZ) bit stream cannot be directly applied to the twisted pair. The UDLT uses triangular modified differential phase shift keying (MDPSK), as shown in Fig 2.

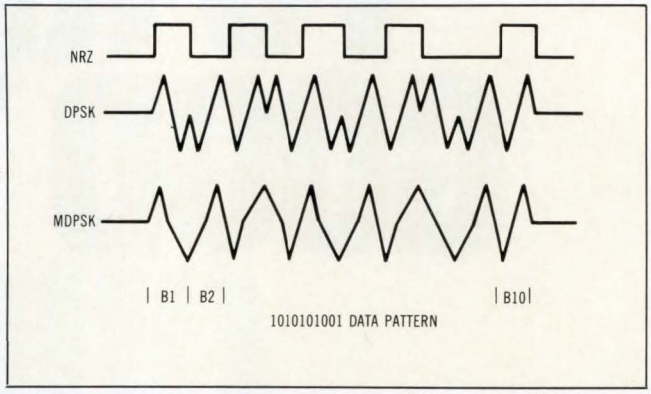

Fig 2 The universal digital loop transceiver (UDLT) uses a modified form of differential phase shift keyed (DPSK) modulation that reduces spectral content of the transmission waveform while retaining the strength of DPSK transmission techniques.

In classical DPSK, a "1" is indicated by the carrier being the same phase as that during the last baud, while a "0" is coded as a 180-degree phase shift in the carrier from the last baud. This scheme has been modified by replacing the phase reversals of the 256-kHz DPSK waveform with a half cycle of 128 kHz. This lowers the spectral content considerably. Since the system must conform to present and perhaps tougher future American (FCC) and the European (VDE) rfi and emi requirements, excessive spectral content is of great concern.

In addition, MDPSK has several advantages over other modulation techniques. MDPSK does not require a start bit, nor a balancing bit to prevent bias distortion due to dc buildup during the burst, since each bit has zero net dc. This allows each bit in the burst to be data information. Additional overhead bits in a ping-pong scheme would require that either shorter loops, or higher baud rates, be used. Also, a zero-crossing of the waveform always occurs during the middle of each baud, which simplifies baud boundary timing recovery. Field trials and extensive computer simulation have verified the overall performance of the MDPSK transmission scheme. They yielded a bit error rate of better than 10^{-7} for 99 percent of the loops using 26-gauge or larger wire at lengths up to 1.25 miles while operating in cables with 49 interfering pairs.

The UDLT transmission scheme occupies a 10- to 500-kHz bandwidth that does not include dc. Thus, the remote digital telephone can derive its power from the PBX. By using CMOS technology,

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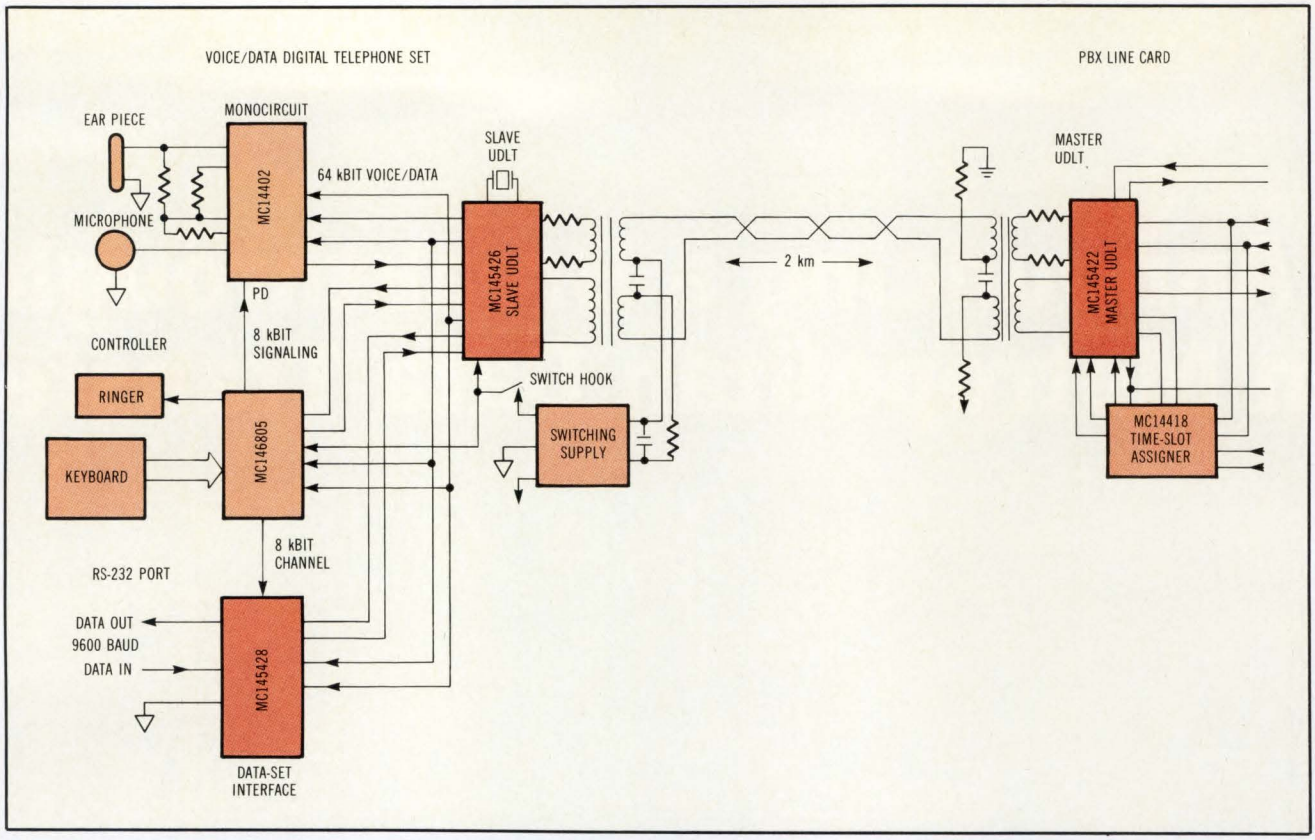


Fig 3 By replacing the existing analog telephone set and PBX line card with UDLTs, both voice and high speed data transmission can be run over existing office telephone wiring.

the total power dissipation of an active digital telephone instrument is 1/4 W when active and can easily be supplied by a 5-V switching regulator. Furthermore, a startup algorithm has been designed in both the master and slave to let the ping-pong interaction stop when the digital telephone is not in use. Moreover, the idle power dissipation is under 50 mW.

Applying the remote time slot

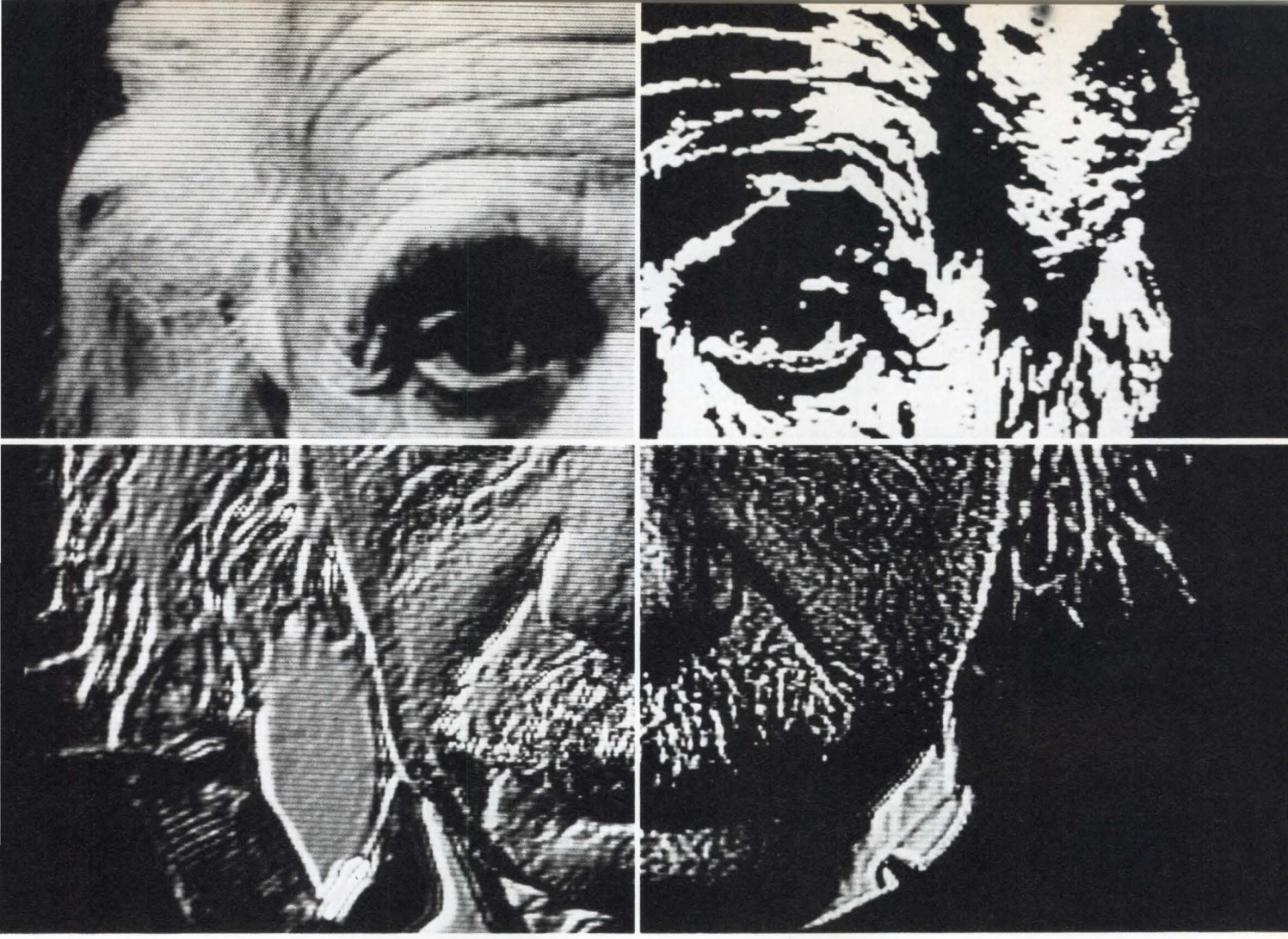
The slave UDLT puts an 80-kbit/s data capacity at a digital telephone's location. Fig 3 shows a minimum digital telephone connected to a UDLT-equipped PBX port. Three data sources are connected to the slave UDLT in this configuration. To provide voice telephone service at this telephone site, the MC14402 PCM monocircuit digitizes and undigitizes the audio signals for the 64-kbit/s channel compatible with the compression and sampling standards mentioned earlier. One 8-kbit/s data channel is interfaced to the dial, ringer, and phone feature hardware via a CMOS microprocessor. Signaling to the PBX may be standard dial-pulse formats or an expanded command channel for voice or data user features. Finally, the last 8-kbit/s channel is connected to the MC145428 DSI. With this UDLT connection, voice and asynchronous data communication up to 9600 bits/s are possible simultaneously. Higher data rates can be achieved (if voice is not required) by using the UDLT's 64-kbit/s channel for synchronous data, or, in conjunction with the DSI, for asynchronous data up to 57.6 kbaud.

The DSI takes the async start/stop bit formatted characters from any RS-232 interface, removes the start/stop bits, and stores them in a first in, first out (FIFO) memory. This data is then reformatted for the 8- or 64-kbit/s channel using a low overhead synchronous bit-stuffing algorithm. Incoming synchronous data is decoded and loaded into another FIFO. Async start/stop characters are then output at the selected baud rate.

PBX LAN configurations abound

Converting an existing analog line only requires the swapping of the PBX analog line card with a UDLT-based digital line card, and the replacement of the user's analog telephone with a UDLT-based digital telephone or workstation (Fig 4). Routing the data through the PBX can be accomplished two ways without requiring any modification to existing PBX software. First, the data channel can be inserted directly into the voice channel using the UDLT's pin-controlled signaling bit insertion feature. This provides a direct data path connection between the two parties who are conversing. Or, if separate routing of data and voice is desired, the data channel can be inserted into another 64-kbit/s time slot at the digital line card. This allows voice and data connections to two independent destinations.

The user equipment could consist of either a basic digital telephone set featuring a data port for



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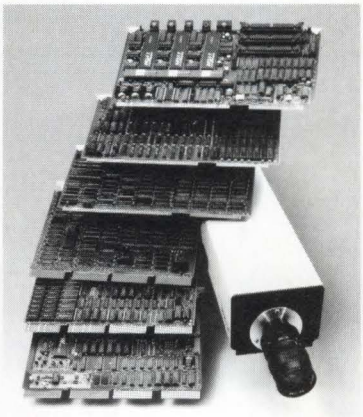

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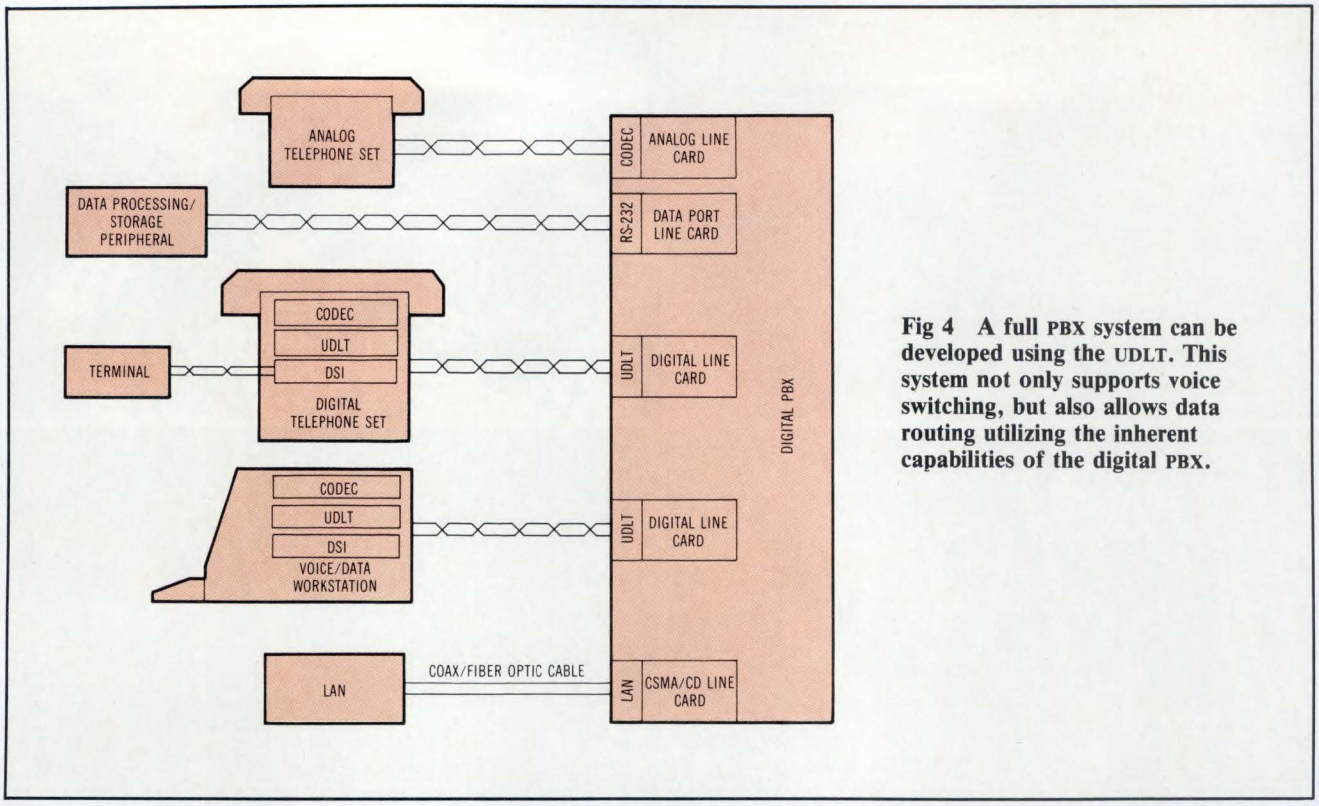

Fig 4 A full PBX system can be developed using the UDLT. This system not only supports voice switching, but also allows data routing utilizing the inherent capabilities of the digital PBX.

connecting terminals or other data equipment, or a workstation that has the code/filter and UDLT integrated into it to provide the telephone set function. If the data equipment communicates in an asynchronous start/stop format, the MC145428 (DSI) provides the interface. As shown in Fig 4, using digital line cards as entry ports to the PBX gains access to other LANs and centralized data facilities. Communication to these devices could be over twisted pairs using the UDLT, RS-232, coax, or fiber optic links.

If the existing telephone switch is not digital, or if the designers do not want to directly retrofit their PBX, an alternative approach to a LAN is feasible. This approach, which retains the advantages of easy reconfiguration and low installation costs, calls for the addition of an auxiliary data switch to the PBX (Fig 5). Additional equipment at the PBX location handles data switching, while the existing PBX switches voice conversations.

Connections to this LAN use existing telephone twisted-pair wiring and the user's analog telephone set is replaced by a UDLT-based digital telephone set or workstation. The data switch's UDLT-based digital line card is similar to that used for retrofitting a digital PBX, except that the voice data is reconverted to analog by a codec/filter and fed to the PBX's analog line card. The auxiliary switch

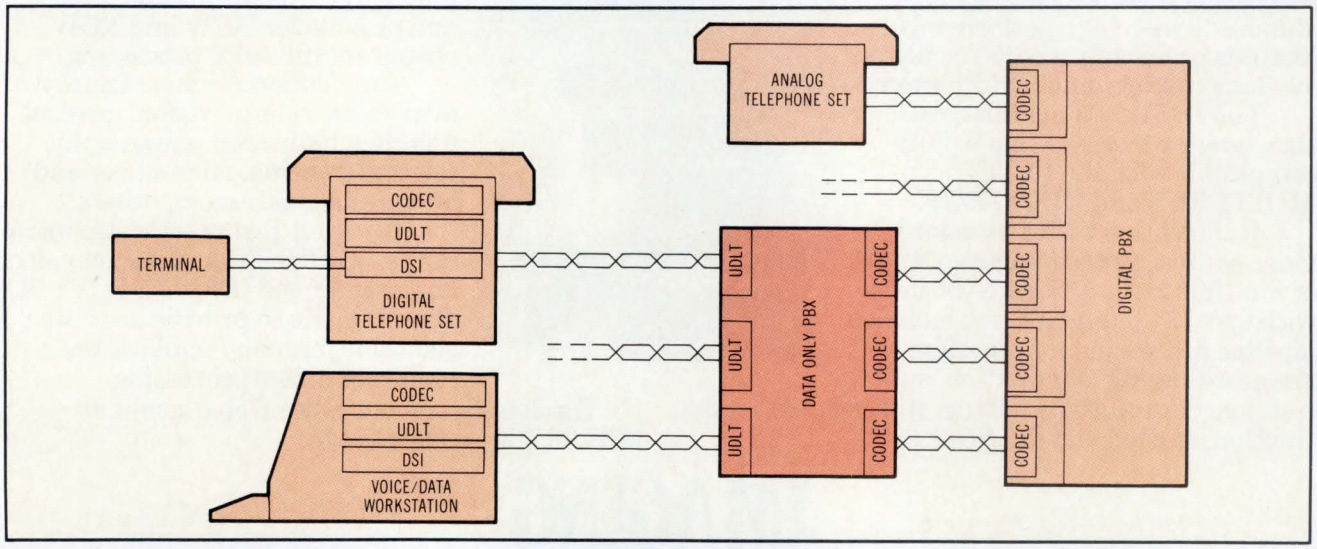

Fig 5 An alternative configuration with the UDLT can be obtained with the addition of a "data only" switch when access to the PBX is unavailable, or if an analog PBX is used.

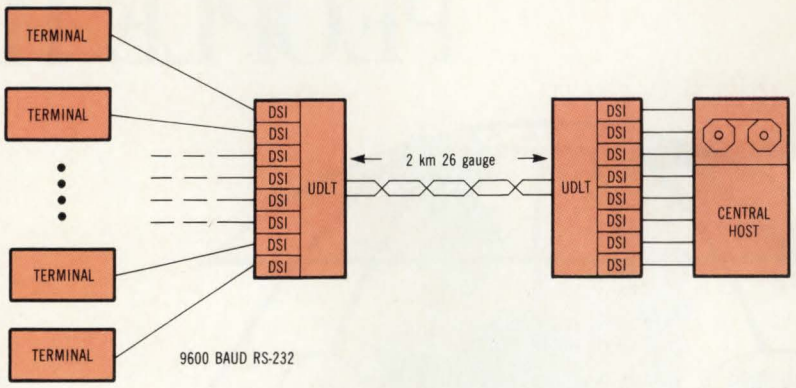

Fig 6 The UDLT and data-set interface (DSI) also provide an inexpensive means of implementing data multiplexers and point-to-point data communications for both asynchronous and synchronous channels.

then routes only the data. Since this switch does not have to handle voice protocol and call progress supervision (bus signaling, ring back dial-tone generation, etc), its software and hardware requirements are much less complex than those for a conventional PBX. This approach allows a LAN implementation with most of the advantages of the retrofitted PBX-based systems. However, it does not require the system designer to have any detailed knowledge of the specific PBX used for voice switching.

In many data networking applications, a need often arises for high speed, dedicated, and unswitched data links. Rather than installing new cabling or expensive modems, existing telephone twisted-pair wiring (with the UDLT as a limited distance modem) can provide a very low cost link. Synchronous 64-kbit/s data transmission at distances exceeding 1.25 miles can occur using a UDLT and a few MSI logic ICs for clock generation/gating. This results in an extremely low cost installation. Asynchronous operation is possible by using the MC145428 DSI in conjunction with the UDLT (Fig 6). In fact, by using multiple DSIs with the UDLT at each modem end, up to eight terminals can be multiplexed into the single UDLT modem link.

The chip set can be an alternative to a coaxial and fiber optic LAN.

Thus, by using master and slave UDLTs, the DSI, and the PCM monocircuit in various combinations, the 64-kbit time-slot capacity of the digital PBX can be used for voice/data LAN applications with the central simplicity of the dial-up network. The use of existing telephone wiring and lack of requirements for controller/port sophistication in the user equipment gives the PBX-based LAN several advantages over coax/fiber-based LANs. The network configuration can be host for both dumb terminals as well as for simultaneous intelligent-peer-to-intelligent-peer communications. There is, therefore, the option to reconfigure the office and rearrange it with the same ease as standard telephone service.

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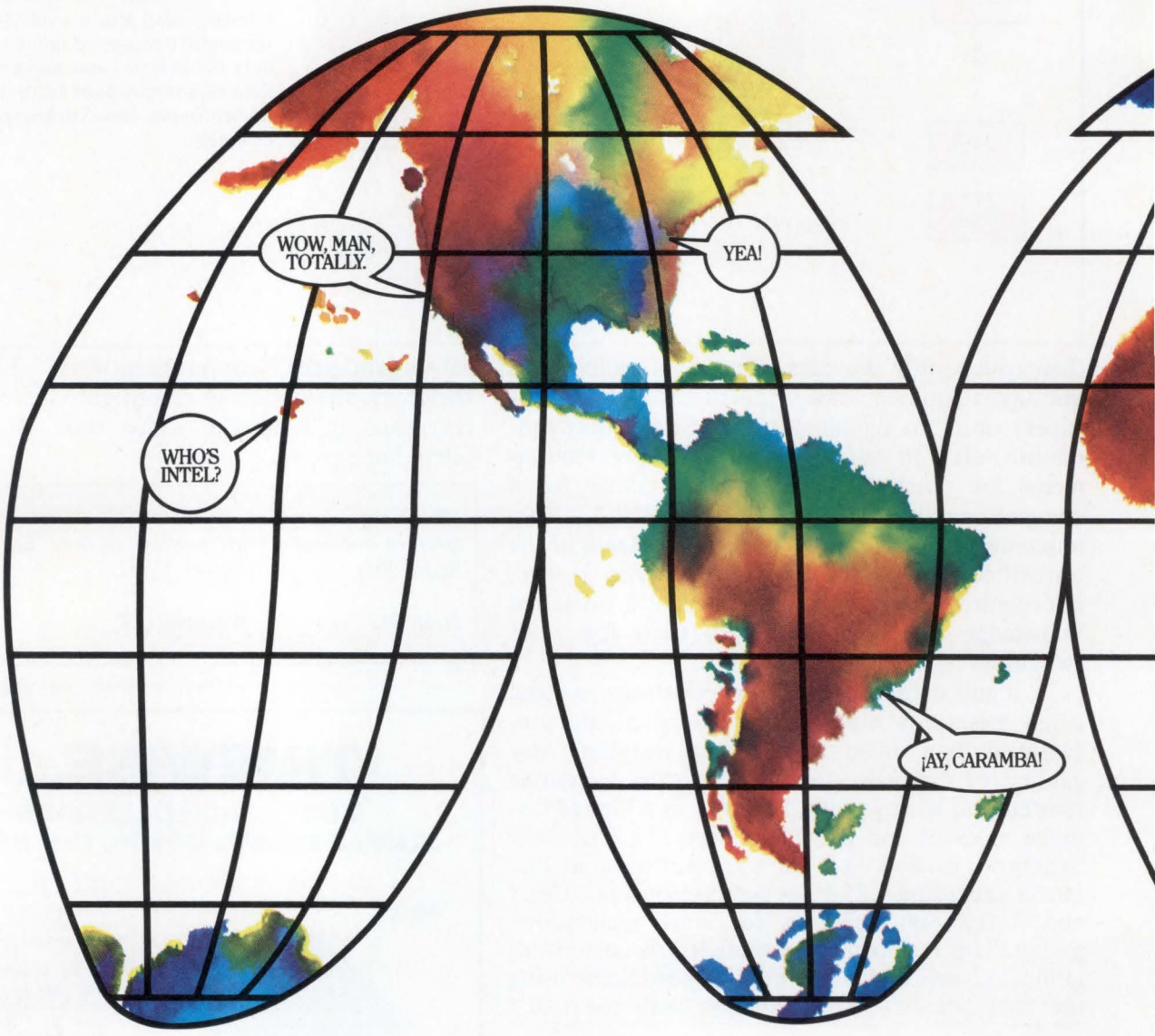

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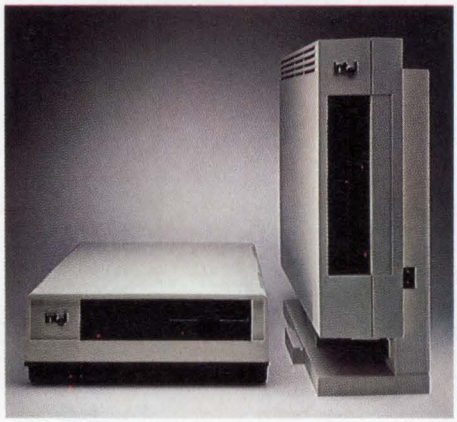

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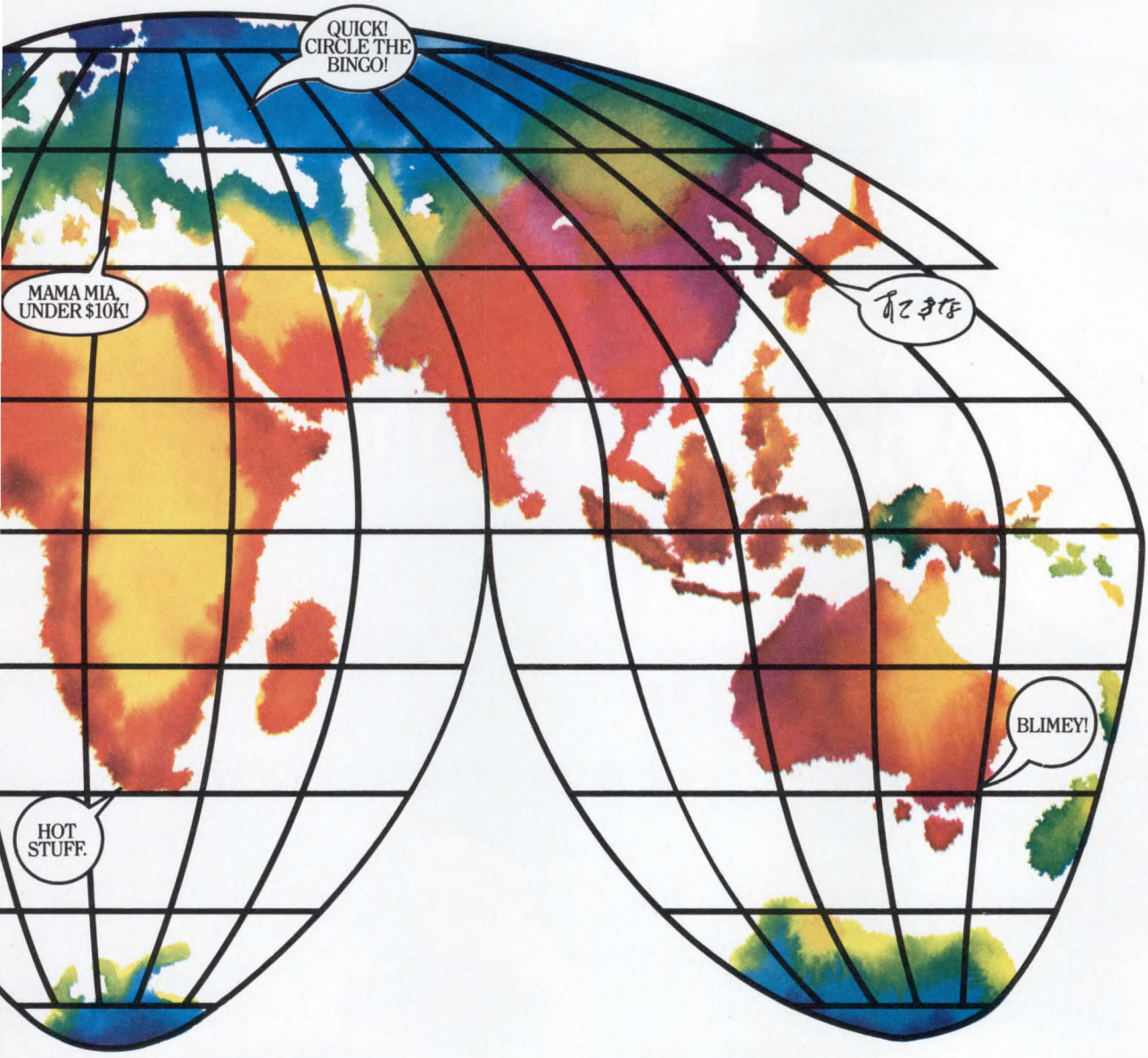

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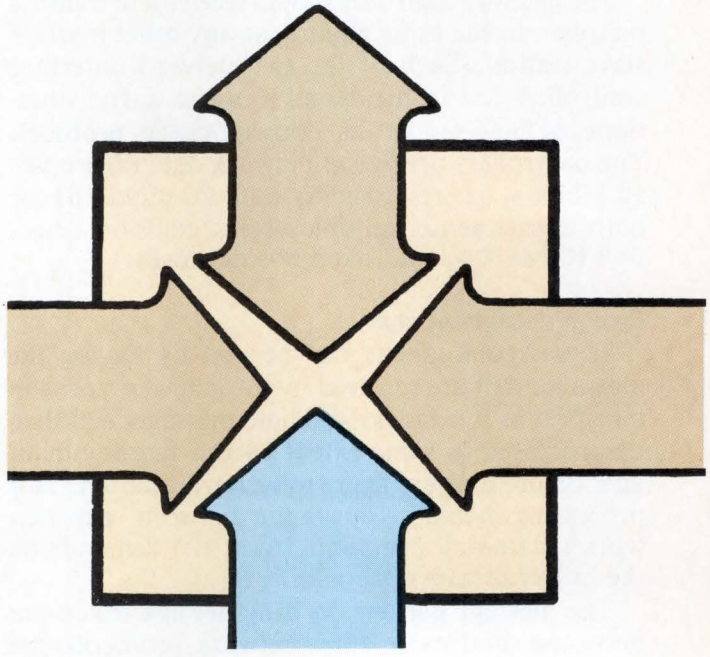
CIRCLE 98

A SIMPLE GATEWAY FOR ODD NETWORKS

Ethernets talk to token-bus baseband networks via a gateway implemented with LSI chips.

by Joonees K. Chay, Jeff Seltzer, and Naseer Siddique



As different types of local area networks are installed in both offices and factories, more users are finding a need to connect them with intranetwork interface controller systems. Currently, however, few vendors offer gateway controllers that allow many different networks to be connected. Thus, networks such as Ethernet, used in office applications where realtime response is not a requirement, cannot talk to token-passing networks that offer realtime response to the critical manufacturing process, and to robotics control operation.

An Ethernet can be connected to a token-bus network using a gateway that is based on a high performance, bit-stream manipulation scheme (Fig 1). The configuration assumes that the two network media can be interconnected locally without the need for long-distance communication. However, the same general hardware design and software structures can be applied to many network types, as well as to gateway halves that interconnect remotely located networks.

The gateway controller has stringent requirements. It must be able to receive back-to-back messages on either network interface and store the messages that are addressed to the gateway for later transmission to the opposite network. It must also be able to receive or transmit on one network while simultaneously receiving or transmitting on the other. To accomplish this, processing power is usually distributed among three controller subsections: two network interface controllers (Ethernet and token-bus), and one centralized gateway management controller. The functions of the Ethernet and token-bus interface controllers are shown in the Table.

Joonees K. Chay is applications manager for standard products at Signetics Corp, Bipolar LSI Div, 290 N Wolfe, Sunnyvale, CA 94086. Mr Chay holds a BSEE from Pennsylvania State University.

Jeff Seltzer is an applications engineer for standard products at Signetics' Bipolar LSI Div. He holds a BA in physics from the University of Pennsylvania and an MS in computer science from California State University.

Naseer Siddique is an applications engineer for standard products at Signetics' Bipolar LSI Div. Mr Siddique holds a BSEE from the University of Engineering and Technology, Lahore, Pakistan, and an MS in computer engineering from Wayne State University in Detroit.

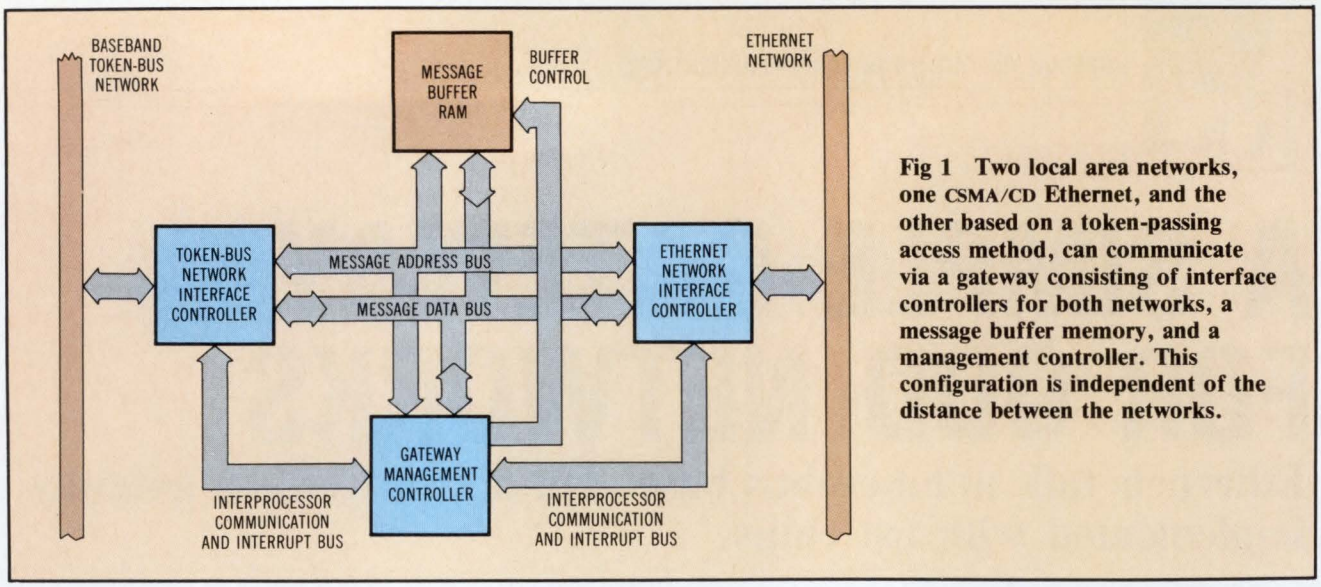


Fig 1 Two local area networks, one CSMA/CD Ethernet, and the other based on a token-passing access method, can communicate via a gateway consisting of interface controllers for both networks, a message buffer memory, and a management controller. This configuration is independent of the distance between the networks.

The gateway controller should receive and transmit messages in the same manner as any other master/slave station. Each of the two network interface controllers has to handle all message traffic situations defined under its corresponding protocol. The controllers operate at network data rates up to 10 Mbits/s, as prescribed by IEEE 802 standards for both carrier sense multiple access/collision detection (CSMA/CD) and token-bus networks.

Design considerations

These requirements can be met by having the messages that are received by the gateway stored in a central buffer memory. These messages can then be processed to some extent by the gateway manager before they are ready to be retransmitted. This processing includes translation between each network's data-link protocols. And, the demands on the buffer memory are significant.

The message packets on Ethernet and token-bus networks (and most other network protocols) are variable in length. In the case of the token bus, the packet length can vary from about 20 bytes up to over 8000 bytes. Moreover, messages addressed to the gateway are received from either network at random times. After protocol translation is completed, the message is held in queue until its destination's network controller gains access to the media for transmission.

For Ethernet communications, the buffer must be ready to either supply a stored message for transmission, or receive a new incoming message on short notice. The latter usually occurs when another station's transmission precedes or collides with the outgoing message.

At a 10-Mbit/s data rate, a new data byte has to be accessed by a controller every 800 ns. Within that time interval, the message buffer is able to access a data byte for each of the three controller subsections. If necessary, it will do so in different memory regions. In addition to handling all these varied requirements, one important objective is that the system make the most efficient use of available buffer memory space to prevent a buffer overflow condition. This requires a robust memory management scheme implemented in the gateway management controller.

One IC answers that call. The Signetics 8X305 bipolar microcontroller was designed for bit-manipulative I/O operations. Thus, it can execute 5 million instructions per second, including data I/O instructions. Its Harvard architecture separates the

Functional Distribution of Three Gateway Network Controller Sections

Ethernet and token-bus controller section	Gateway management controller
Receiving and transmitting message packets on the network media	Allocation of buffer areas to incoming and outgoing messages
Media access control functions (eg, Ethernet collision recovery, token passing, etc)	Arbitration of the central message buffer between the gateway manager's processor and the two network controllers
Serialization, coding, and synchronization of the data stream	Interrupt handling and interprocessor communication with the network interface controllers
Packet destination address matching	Translation of the packet format into the data-link protocol of the destination network
CRC generation and error detection	Any additional higher level protocol translation and management functions
DMA to central message buffer	
Interrupt handling and interprocessor communication with the gateway management controller	

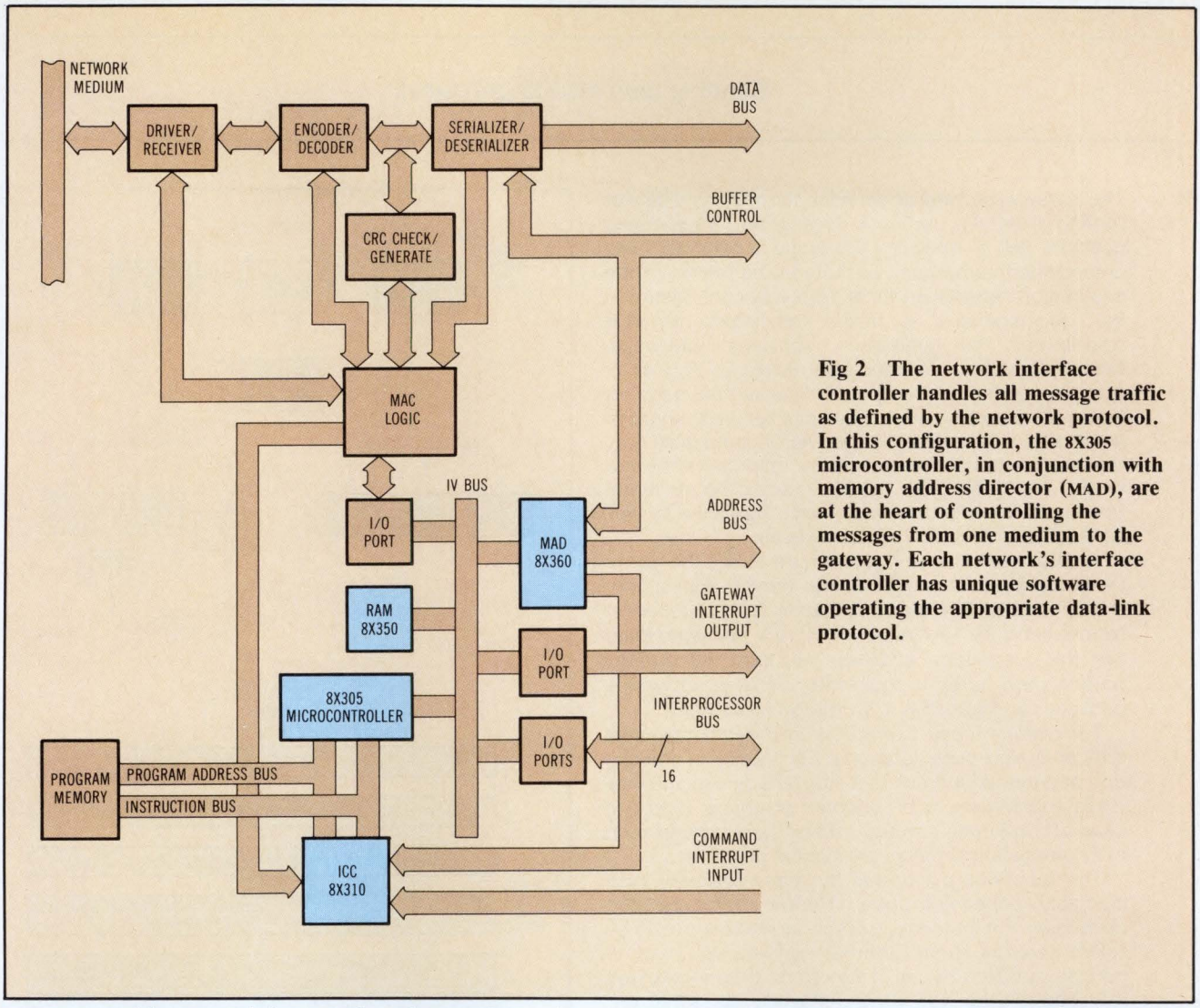


Fig 2 The network interface controller handles all message traffic as defined by the network protocol. In this configuration, the 8X305 microcontroller, in conjunction with memory address director (MAD), are at the heart of controlling the messages from one medium to the gateway. Each network's interface controller has unique software operating the appropriate data-link protocol.

program address and instruction buses from its local data (IV) bus. This keeps system control and message data flowing at peak rates. The 8X305 architecture also supports configuring the system into separate independent buses for optimal data throughput. This allows network message data transfer operations to gain exclusive access to the central message buffer.

In contrast, conventional MOS microprocessor architectures allow the message buffer to be located within the processor's main memory and attached to its common address and data buses. In addition to message traffic, these buses are used by the microprocessor for instruction fetching and local working storage. Since the network controllers may not be able to gain immediate access to the processor's memory bus, first in, first out (FIFO) buffers are usually required to keep the message data flowing. Use of the bus by the network interfaces may also result in an overall reduction in the processor's data throughput rate.

However, the 8X305 supports separating the local program buses, local data bus, and system message buses, therefore allowing multiple independent operations to be performed in parallel. Yet, the I/O performance capabilities of the 8X305 let it access the message buffer as quickly as most MOS processors access their own memory.

The controller, coupled with the 8X310 interrupt control coprocessor (ICC), adds priority-set, multilevel interrupt handling capability. This gives the 8X305 the power to deliver realtime interrupt responses within about 400 ns. The 8X360 memory address director (MAD) completes the critical link for each of the gateway's controllers to access the central message buffer management.

Controlling the network interface

The gateway system's essential activity centers around the data bus. This bus interconnects the gateway management and the two network interface subsections (Fig 2). All message traffic flows over this data bus.

Messages on the data bus are passed to and from a network medium (Ethernet or token bus) through physical interface circuitry and serial interface control logic. Standard line driver and receiver circuitry form the physical interface to a baseband network medium. They fulfill the electrical requirements defined by the network's physical layer

Sending packets via gateways

The gateway controller services the message-packet routing from one network to another, fragmenting packets for a specific destination network, and embedding internetwork packets in the format of the destination network protocol. Gateway controllers can be subcategorized as media translators, protocol translators, and application translator gateways. Media translators connect two networks that differ from each other only at the physical and the data-link layers. Media conversion gateways can be thought of as devices that bridge an otherwise incompatible gap.

Protocol translator gateways interconnect networks that differ from the physical to the presentation layer. Such gateways convert the media as well as the higher level network protocols.

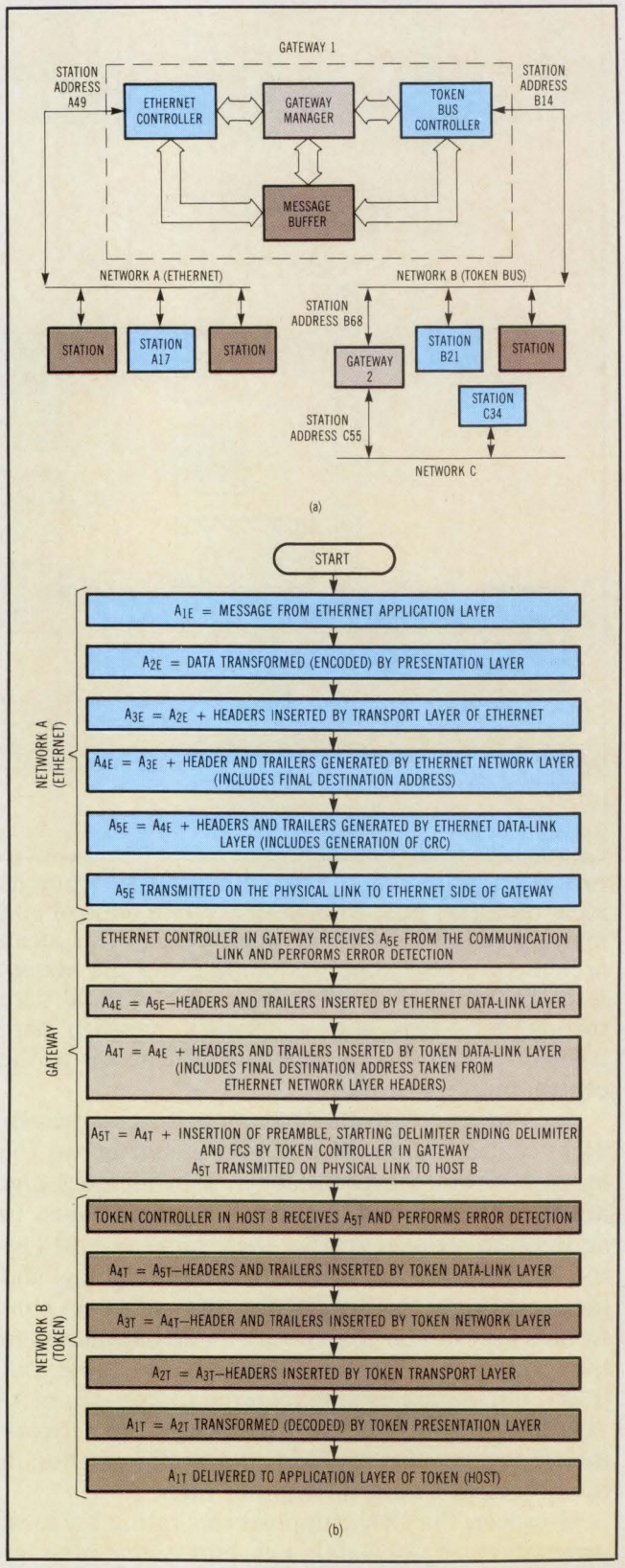
Application translator gateways manage the higher level communication layers and handle application-specific tasks. The gateway has to receive a packet from a network, unwrap the network package, identify the destination address, calculate the optimal routing path, wrap it again into the next network's package, and transmit it on the other network.

Translating these operations into design requires critical design considerations. For example, translation of a longer address to a shorter address and vice versa, translation of bit-oriented protocols (HDLC) to character-oriented protocols (Bisync), and translation of higher level protocols are typical problems.

The functions performed by gateways vary considerably, depending upon different interconnection strategies. For instance, a gateway interconnecting a token network to an Ethernet network will have to perform a different set of functions than a gateway interconnecting an X.25 network to Ethernet. Therefore, interconnecting heterogenous networks raises various questions. Are there any standards available? Should the protocols of one network be directly translated to the protocols used in another, or should both of them be converted to a standard protocol? What kind of performance will be achieved?

A case in point is an Ethernet that has to communicate with a token-passing network (see Figure). Suppose a station with address A17 on the Ethernet (network A) has a packet to be transmitted to a station with address B21 on the token bus (network B). The actual message will be formed by station A17's application layer and passed to its presentation layer, which will transform (encode) the message. The next level, the session layer, handles functions such as recovery from abnormal situations and establishment of the connections across the network. Thus, it is not really in the way of the data flow.

The encoded packet, therefore, is passed directly to the transport layer. This layer encapsulates the entire packet into its data field, and generates and adds new headers to the packet. As the packet flows down to the network layer, new headers and trailers are added. This includes the final destination address on the token network (in this case, station B21). The actual header and trailer formats generated at each layer depend upon the higher level protocols used to



implement the corresponding layer. The packet format generated by the network layer will be passed to the data-link layer, which will generate the standard Ethernet packet at the link level, including the CRC field. The packet's destination address will be A49, the station address of gateway 1 on the Ethernet. This packet will then be passed on to the physical layer for transmission on the communication channel to the Ethernet side of gateway 1.

Upon receiving the packet, the Ethernet controller in the gateway will unwrap it by peeling off all the necessary headers and trailers inserted by various layers (the number of layers to be unwrapped will depend upon the type of gateway being used). In case of a media translator gateway, it will only unwrap up to the data-link layer of Ethernet, which will also include error checking.

By eliminating the fields added to the packet by the data-link layer, the message will be retrieved as it was in the network layer of station A17. The gateway controller will now convert the packet to a standard token-packet format by generating another set of headers and trailers. The source address will be B14 (the address of gateway 1 on token network B) and the destination address will be B21 (as indicated in the network layer header). As the message passes through the token controller in the gateway, it will be appended with a new frame check sequence, starting and ending delimiter, and a preamble. This reformatted packet will be transmitted by the token controller on network B. Upon reception, station 21 will have to unwrap all the layers up to the application layer to get the actual message.

Several different networks can be interconnected through multiple gateways. In such situations, a message that has to be transmitted from one network to another may need to be routed via a third network. The possibility of errors is of course increased, but one can assume that every gateway involved in transmission, reception, and translation of packets can detect and correct the errors. Suppose the packet transmitted by station A17 is destined for station C34 on network C, but the packet has to go through network B. The packet will first be reformatted for network B by gateway 1 and then again for network C by gateway 2.

Station A17 defines the immediate destination address (A49) in its destination field and the final address (station C34) in its network layer header, then forwards the packet to gateway 1. Upon reception, gateway 1 reformats the packet by replacing the source address with its own address (B14) and the destination address with the intermediate address for gateway 2 (B68). Gateway 1 also generates a new CRC, then forwards the packet to gateway 2. Upon reception, gateway 2 reformats the packet again, replacing the destination address field with the address of station C34 and the source address field with its own address (C55). Gateway 2 also calculates a new CRC, then forwards the packet to the final destination.

protocol, and convert between the higher voltage signals on the medium and TTL logic levels used by the controller hardware.

Data on the network medium is encoded so that the high/low logic levels convey both data and synchronization information. Several standard coding formats are currently used in both data communication and mass storage applications. The most common include "Manchester" and fm.

The serial interface control logic consists of an encoder/decoder circuit, a cyclic redundancy check (CRC) generator/checker, and a serializer/deserializer circuit. The encoder/decoder circuit translates between the encoded data on the medium and raw serial data. The decoder section must lock onto an incoming message's synchronization pattern and provide the data bits extracted from the message, as well as a clock signal by which the adjacent circuitry can strobe in the serial data. The decoder also detects coding violations that may be caused by line noise, but are also used intentionally by the token-bus protocol for certain message delimiters. The decoder typically employs a phase locked loop (PLL) to establish synchronization. In the transmit mode, the encoder section receives raw serial data and generates the encoded pattern at its own fixed clock rate.

Each network interface controller performs error checking and generation of CRC values (referred to as the frame check sequence in the token-bus protocol). It is necessary to regenerate a new CRC for each outgoing message because the packet header information is altered during protocol translation. Depending on its software capabilities, the gateway manager may correct detected errors in received messages. Otherwise, the message is tagged to inform the destination host of the error condition.

The serializer/deserializer logic converts between the raw serial data and parallel data bytes that can be transferred on the gateway's data bus. The encoder/decoder circuit synchronizes the serial interface. Every eight clock cycles, a parallel data byte is transferred between the shift register (which performs the conversion) and a holding register. Before the next byte is finished shifting (ie, within the next eight clock cycles), the holding register must be serviced (contents read or replaced). This is the point at which the network data stream synchronizes with the message buffer access cycles.

The serial interface control logic performs functions that are fairly common to various data communication and mass storage controller applications. Serial interface control logic implemented with discrete logic functions, or more advanced field-programmable arrays, or even gate arrays, typifies the current solution to management of the data stream. Inevitably, single-chip solutions will appear to replace discrete implementations.

The 8X305 microcontroller coordinates all the activities within the network interface control section. It controls data movement through the serial interface control logic and to and from the message buffer without actually standing in the data path. Instead, it sets up conditions that allow the buffer to be accessed directly by hardware. Arbitration logic in the gateway management section controls the actual realtime access to the buffer.

The message transfers on the data bus are very similar to conventional DMA in computer systems, except that the data bus is used exclusively for the message data traffic. For example, there is no host processor on the bus to contend with. These message transfers require that the controller generate a sequence of buffer addresses to accompany the data. The MAD performs that function.

After the microcontroller initializes the various registers and counters, the MAD chip can count through a sequence of addresses independently with respect to the 8X305's processing. In the gateway design, the MAD output connects to the system address bus, which runs parallel to the data bus. The MAD units in each of the three controller sections supply address information to the message buffer via the address bus.

A collection of I/O ports provides a multipurpose interface between the microcontroller and other parts of the system for passing data and control/status signals. All I/O ports and data-oriented peripherals, such as the 8X360, are connected to the microcontroller on a special local data bus called the IV bus. A 256-byte high speed bipolar RAM (8X350) is also attached to the IV bus, which provides local working storage to the microcontroller.

Media access control (MAC) functions are distributed between the MAC logic (specialized hardware) and microcontroller software in each network interface controller. The 8X305's instruction execution and data transfer speeds allow the microcontroller to handle many of the packet-header processing and MAC functions in software. In turn, the size of the MAC hardware can be minimized. The primary duty of the MAC logic is to handle the operations that require an immediate response on the network.

The network controller activities are coordinated with the gateway management controller through the exchange of interrupts between the respective microcontrollers. Interrupt request signals coming in from the gateway manager are handled by the 8X310 ICC. The ICC attaches to the 8X305's program address and instruction buses to control interrupt calling and return transfers. The microcontroller is also interrupted to respond to certain network control activity requested by the MAC logic, and to occasionally service the MAD.

Interrupt requests to the gateway manager are software generated. A pair of I/O ports passes information directly between the controllers over a separate interprocessor bus. These exchanges are in conjunction with interrupt requests and include such information as interrupt type, buffer address, and message length. Since these interrupts often occur during realtime message transfers, the system data bus cannot be used conveniently to exchange the information.

The main functions of the gateway manager are to maintain the message buffer and to perform all necessary message packet translations and higher level protocol processing. As in the network interface controllers, the heart of the gateway manager is an 8X305 microcontroller that is interfaced to the message buffer RAM via an 8X360 MAD and an I/O port. Also included are the 8X310 ICC and I/O ports required to perform the interprocessor communication with the network controllers (Fig 3).

Buffer benefits

The message buffer itself consists of 32 Kbytes of RAM. With a maximum token-bus message size of 8 Kbytes, this buffer size accommodates one incoming message on each network interface plus storage for other messages being translated or awaiting transmission. This message buffer is segmented by the controller into 128 pages of 256 bytes. Although this should be sufficient for this application, the buffer size can be doubled if extremely heavy traffic is anticipated or lengthy protocol translation routines are to be implemented. With an access cycle time of 200 ns, the buffer memory can serve all three controller sections within the required time interval of 800 ns (derived from the network transmission data rate up to 10 Mbits/s).

The buffer arbitration logic acts as a special-purpose standalone DMA controller (Fig 4). At the end of every 200-ns memory access cycle, the DMA controller samples the buffer access request lines from each of the three controllers and arbitrates a memory cycle on a round-robin priority basis. In the worst-case situation, when all three requests are active during consecutive cycles, the arbiter rotates among the three controllers and grants each an access window every 600 ns. The logic required to perform this function is easily implemented using a few latches and a field-programmable logic sequencer (FPLS) circuit.

The buffer access request signal for a network controller is taken from the parallel data strobes of the serial interface control logic. This signal also triggers the local MAD to sequence to the next address in its assigned buffer space. When the arbiter grants the memory cycle, the corresponding MAD is enabled and a data byte is transferred in or out of the buffer over the data bus. Since all of the gateway manager's buffer accesses are software-controlled, the memory cycle requests for this

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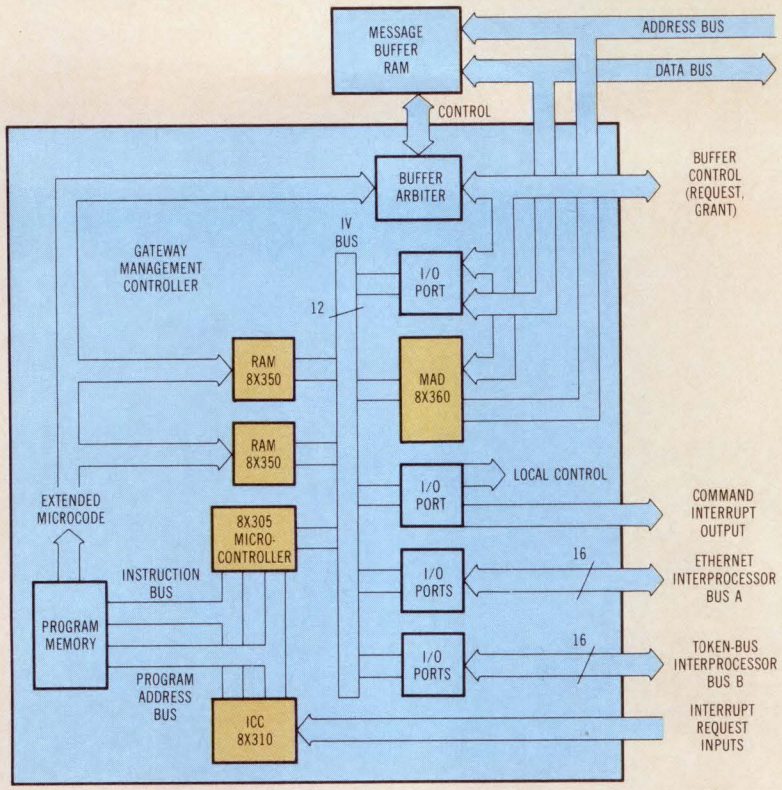
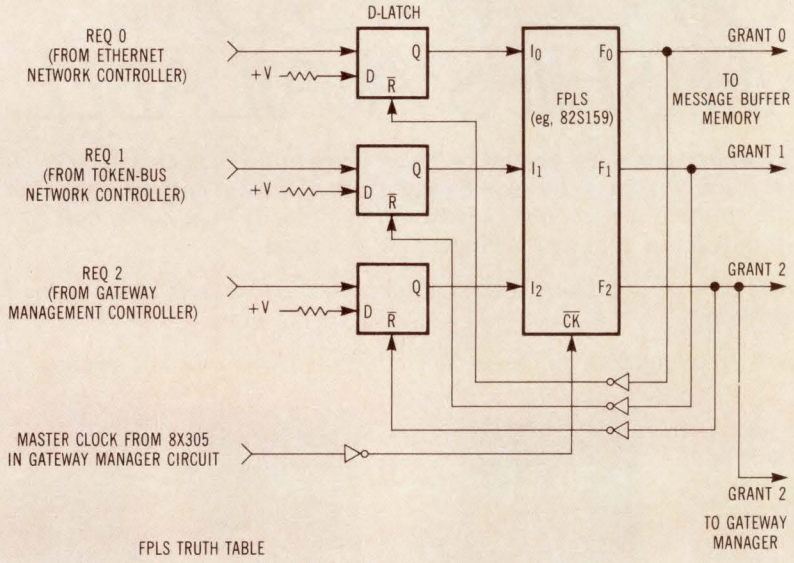


Fig 3 The same chips that made up the heart of the network interface controller can be used for implementing the functions of the gateway management controller. The message buffer memory should be able to accommodate data from both the management controller and the two interface controllers within the 800-ns access time that is available in a network operating at up to a 10-Mbit/s rate.

controller are generated by extended microcode bits programmed in the local microcontroller's program memory. Extended microcode is a block of extra bits added to the program memory's width to provide, with each instruction executed, signals for general control functions and for fast I/O port selection.

The software running on all three microcontrollers exists as a collection of realtime tasks. Except for initialization, all tasks in the network interface controller are invoked in response to interrupts that are received either from the gateway management controller or from local operational units. Most tasks that are in the gateway management



FPLS TRUTH TABLE

GRANT 0	= REQ 0 • $\overline{\text{GRANT 0}}$ • $\overline{\text{GRANT 1}}$ + REQ 0 • $\overline{\text{REQ 2}}$ • GRANT 1 + REQ 0 • $\overline{\text{REQ 1}}$ • $\overline{\text{REQ 2}}$
GRANT 1	= REQ 1 • GRANT 0 + REQ 1 • $\overline{\text{REQ 0}}$ • $\overline{\text{GRANT 1}}$ + REQ 1 • $\overline{\text{REQ 0}}$ • $\overline{\text{REQ 2}}$
GRANT 2	= REQ 2 • GRANT 1 + REQ 2 • $\overline{\text{REQ 1}}$ • GRANT 0 + REQ 2 • $\overline{\text{REQ 0}}$ • $\overline{\text{REQ 1}}$

Fig 4 The buffer arbitration logic acts as a special-purpose standalone DMA controller. Using a few latches and a field-programmable logic sequencer (FPLS), this logic circuit samples the request lines from the three interface controllers every 200 ns and arbitrates a memory cycle to the message buffer memory according to the round-robin sequence specified by the FPLS truth table.

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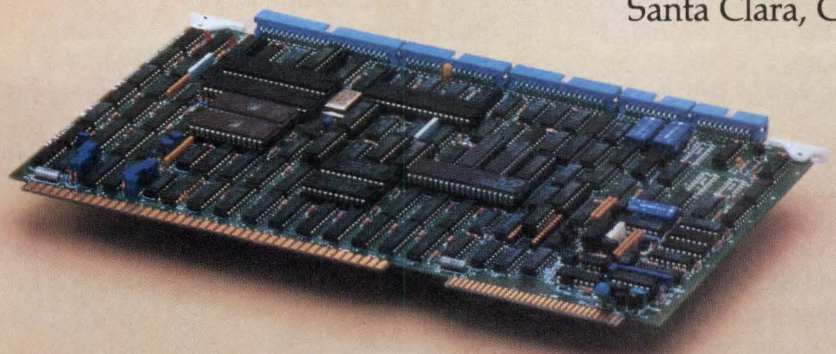

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CIRCLE 100

controller are invoked by interrupts from the network controllers, with the exception of the packet translation routines. These run in the main program under the control of a primitive executive.

As mentioned earlier, the message buffer is divided into 128 pages with 256 bytes/page. The gateway management software maintains a table of 128 pointers in its local working storage that corresponds to the 128 pages. When a message received from a network controller runs over into more than one buffer page, the pointer for the first page will contain the address of the pointer for the second page which, in turn, contains the next pointer address, etc. Thus, a linked list is formed. The software includes several lists for packets currently being received, those waiting for protocol translation, those waiting to be transmitted, and free pages ready to be allocated to new messages. For each of the above processes (except free pages), separate lists are maintained for each of the two networks from which messages originate.

The first and last pointer of each list are tracked. As a process is completed on a buffer page or packet (packets may consist of one or more pages), the corresponding pointers are removed from that process' list and appended to the list for the subsequent process. For example, when a packet is finished being translated from token-bus protocol to Ethernet, the pointers for those message pages are removed from the "translate token-bus" list and added to the packet list awaiting transmission on the Ethernet.

Initializing the gateway manager

When the gateway manager is initialized, it links all the pointers to the free page list. Then, it allocates one page to each network receiver and sends each network interface controller an ALLOCATE-RECEIVE-PAGE (ARP) command. The command is sent by placing the ARP command code and the allocated page address on the interprocessor bus to the desired controller and generating an interrupt request.

When interrupted, the network controller prepares its MAD (8X360) with the received page address and awaits an incoming message. As a message addressed to the gateway is detected, the controller begins filling the designated buffer page and immediately requests another page to use in case the first one fills up. The network controller sends a REQUEST-RECEIVE-PAGE (RRP) interrupt to the gateway manager, which responds by sending another ARP command with a new page address. Each page allocated to that receiver is added to the receive Ethernet list or to the receive token-bus list.

As a page does become filled during an incoming message, the network controller is interrupted by its MAD. The MAD is then reloaded so that the incoming message begins to fill the new buffer page. At this time, another RRP interrupt is issued to set up for the next page.

When an incoming message terminates, the network controller sends a RECEIVE-MESSAGE-COMPLETE interrupt with the length of the last buffer page on the interprocessor bus. The gateway manager responds by transferring all page pointers associated with the completed message from the receive list and links them onto the appropriate translate list. A flag is then set to notify the operating system kernel to execute the protocol translation routines.

For basic media-translation operation, where only the data-link fields of the packet are altered, the network controllers are set up to leave sufficient padding at the beginning of each packet so that translation can be performed in place (ie, without copying the message data to another buffer location). However, if additional higher level protocol translation routines require message copying, another pointer list (for each network) could be added to keep track of the intermediate pages.

After message translation is completed, the associated pointers are transferred to the transmit list for the opposite network. A TRANSMIT-PAGE command with the first page address is sent to the network controller. The MAC logic is armed and awaits the appropriate conditions on the network medium to begin (or attempt to begin) transmission of the outgoing message.

Similar to the receiving process, whenever the network controller begins to transmit a new page of the outgoing message, it sends a REQUEST-TRANSMIT-PAGE (RTP) interrupt to the gateway manager so that it can continue to transmit when the current page becomes exhausted. The gateway manager responds to RTP interrupts with TRANSMIT-PAGE commands.

Upon completion of a packet transmission, the network controller sends a TRANSMIT-MESSAGE-COMPLETE interrupt that lets the gateway manager return all page pointers associated with the completed message back to the free page list, thereby making them available for new incoming messages. Thus, communications between different local area networks is assured through a gateway configuration that has LSI circuits and sophisticated software.

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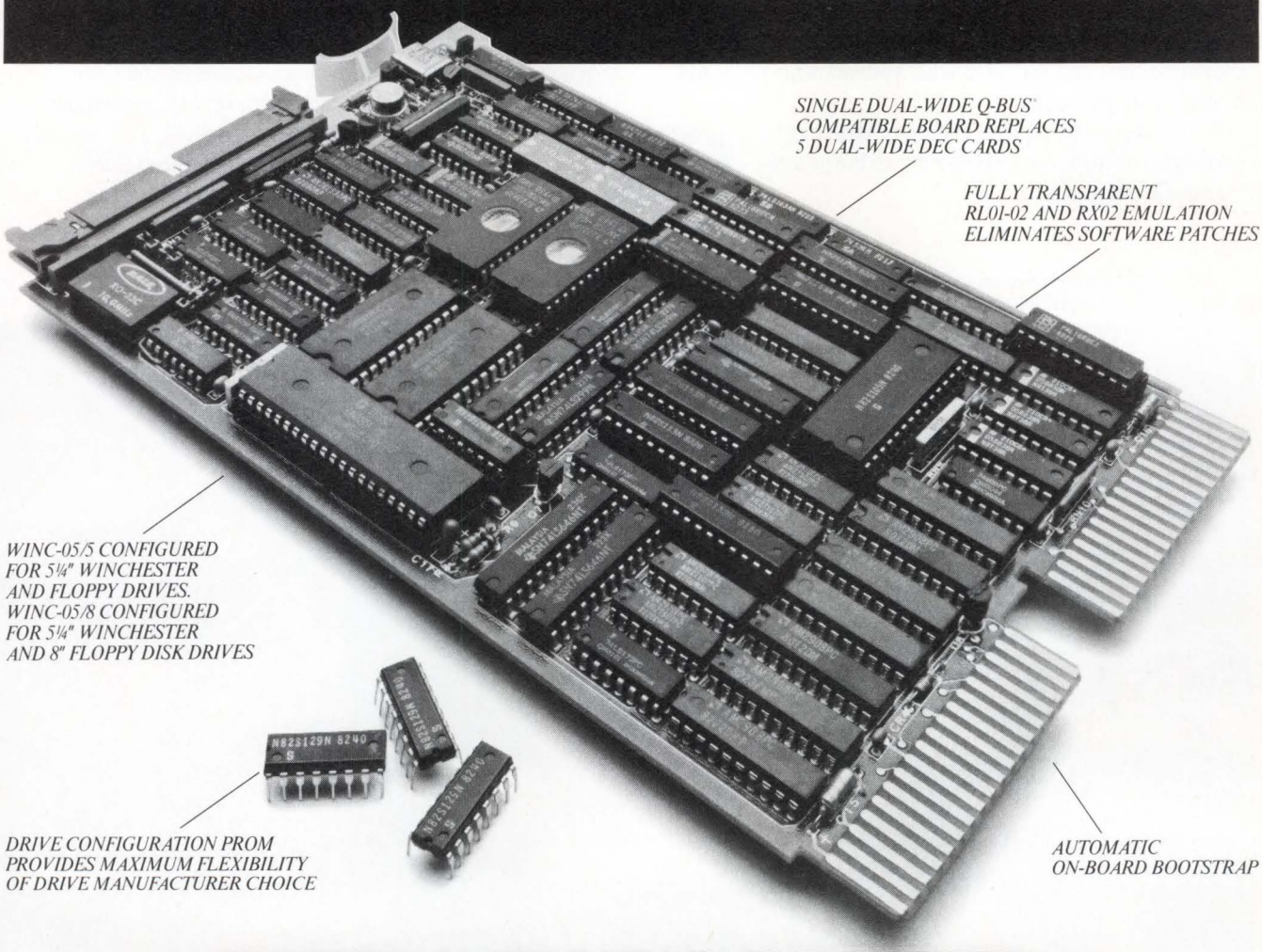

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The LANCE chip adapts 16-bit power of micro to form a true Ethernet connection.

by James A. Fontaine

A common problem associated with high speed data transfers in Ethernet-like local area networks is receiver-end data congestion, caused by a system's failure to process messages and reallocate receiver-buffer space at an adequate rate. This is due to either insufficient processing capability or inadequate computer system bus bandwidth. An intelligent VLSI processor with dedicated memory can alleviate data congestion, thereby allowing efficient attachment of intelligent node devices. A number of local area network control chips are available to perform this kind of operation (see Panel, "Ethernet controller chip comparison"). One possible configuration utilizes the Local Area Network Controller for Ethernet (LANCE) MK68590 chip in conjunction with a single-chip, 16-bit microcomputer like the MK68200.

Ethernet's performance level often depends directly on the throughput of a host computer. In addition, transmitted messages can only be generated by the host during the time it controls the system bus. However, if each message consists of large amounts of data, the amount of bus bandwidth available for host computer processing may become the factor limiting throughput.

An effective method to reduce bus congestion is the use of a 16-bit microcomputer, such as the 68200, for an Ethernet node's local processor. The chip's architecture provides for onchip ROM and RAM, as well as an onchip baud rate generator and timers that produce the interrupt time-outs necessary for implementing upper levels of the Ethernet protocol. The 68200 can handle message acknowledgment, buffer manipulation, frame-related errors, and software implementation of upper level protocols. This frees the main CPU to handle only the core of the messages.

Utilizing the leadless chip carrier (LCC) version of the 68200, both the private bus and the system bus can access an external memory-mapped I/O (see Panel, "A closer look at LANCE and the micro"). Up to 111 Kbytes of memory can be addressed with two independent bus structures, enabling concurrent host and node processor activity. Thus, the 68200 does not have to stop processing when the host or LANCE requires control of the system bus to load or unload messages. The 68200 has its own private bus and program space from which it can continue to execute. This architecture makes the 68200 an ideal processor in situations where concurrent activity from both a local processor and a host processor is required.

Two types of configurations can be supported with the 68200-68590 interface. One configuration is the standalone mode, used when interfacing a terminal or number of terminals via an Ethernet link to a main processor located up to 2.8 km away. In this configuration, the 68200 handles local processing of both transmitted and received messages, achieving economic interfacing of many terminals to the main processor. The second configuration uses the interface as a peripheral or a frontend processor to the host.

James A. Fontaine is senior architectural engineer at Mostek Corp, a subsidiary of United Technologies Corp, 1215 W Crosby Rd, Carrollton, TX 75006. He holds a BS in electrical engineering from Marquette University.

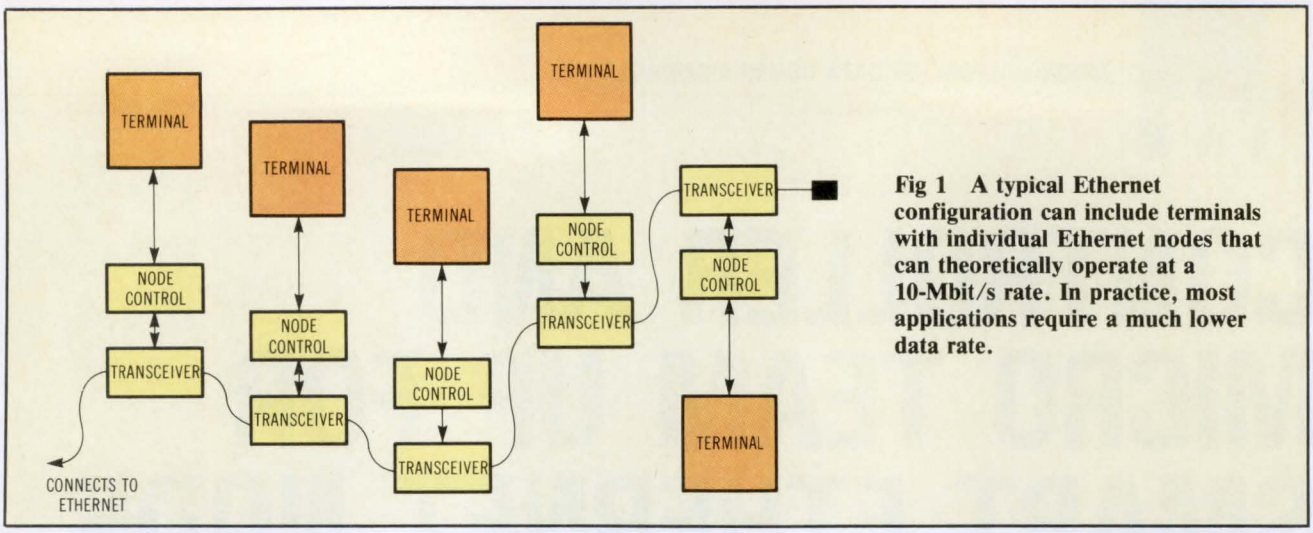

Fig 1 A typical Ethernet configuration can include terminals with individual Ethernet nodes that can theoretically operate at a 10-Mbit/s rate. In practice, most applications require a much lower data rate.

In some applications, it may be desirable to interface one or more user terminals to an Ethernet link, each with an individual interface (Fig 1). The 68200's onchip serial port and baud rate generator make this configuration simple to implement. The chip's serial channel provides for a double buffered receive and transmit interface with data rates up to 1.5 kbits/s if the clock is asynchronous, and up to 1.5 Mbits/s with a synchronous clock. It also provides for internal or external baud rate generation.

For user terminal and similar interfaces, the 10-Mbit/s message rate that Ethernet offers is not typically required. Therefore, a cost-effective configuration may be implemented in which a local node services many terminals (Fig 2). A series of universal synchronous/asynchronous receiver/transmitters (USARTs) can be placed on the private bus to accommodate more than one terminal. Also, a modem interface can be provided to link the Ethernet to other local area networks (LANs) via telephone lines. This provides a link to additional LANs at a reasonable cost, but at data rates much lower than those that can be attained by a direct Ethernet link.

Such a standalone configuration can also be used in other applications to reduce Ethernet's cost. For example, designers can configure a printing station composed of a letter-quality printer, a fast line printer, and a plotter. Although the need to use all three simultaneously may not arise very often, each device can be accessed at any time.

System peripheral configuration

The second configuration, where the 68200-68590 interface acts as a peripheral or frontend processor to the host, greatly unburdens the host CPU as well as the system bus. The host can gain access to the local bus and transfer messages and commands to the 68200 by dumping them into memory space and then notifying the 68200 that a transfer has occurred. This is done by either interrupting the 68200 or setting a bit in a shared status block (Fig 3). The 68200 would have control of the node's local bus, which may be accessed by both the LANCE and the

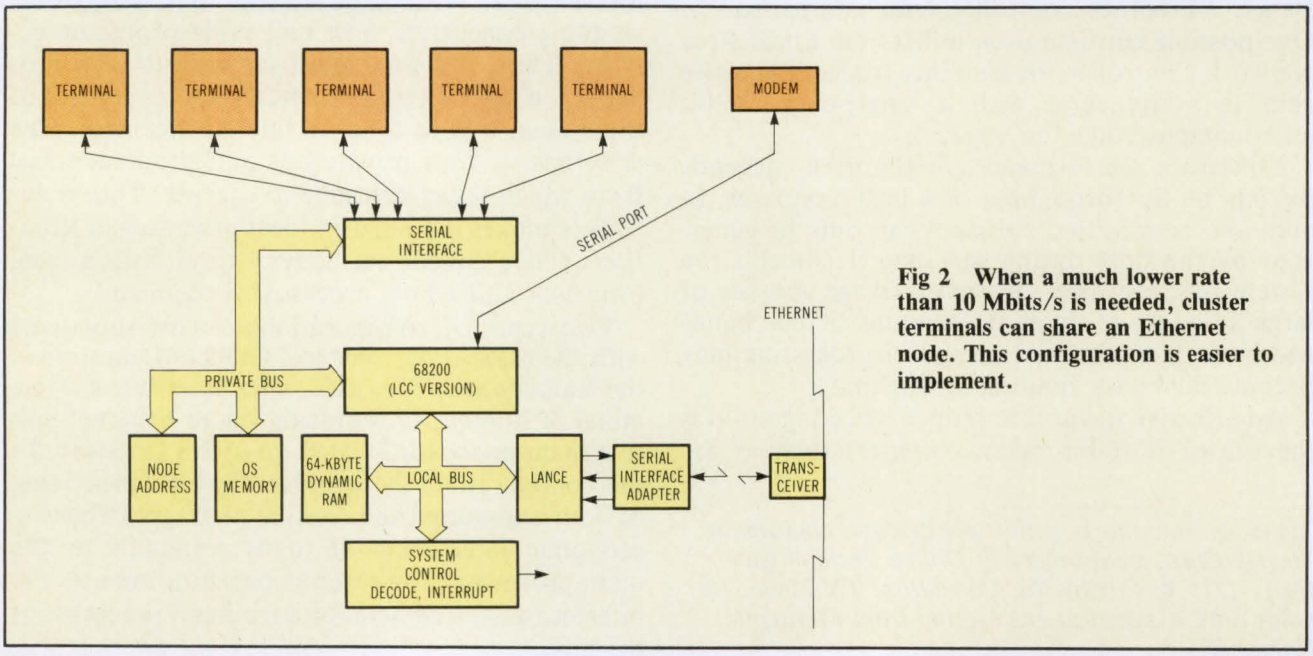

Fig 2 When a much lower rate than 10 Mbits/s is needed, cluster terminals can share an Ethernet node. This configuration is easier to implement.

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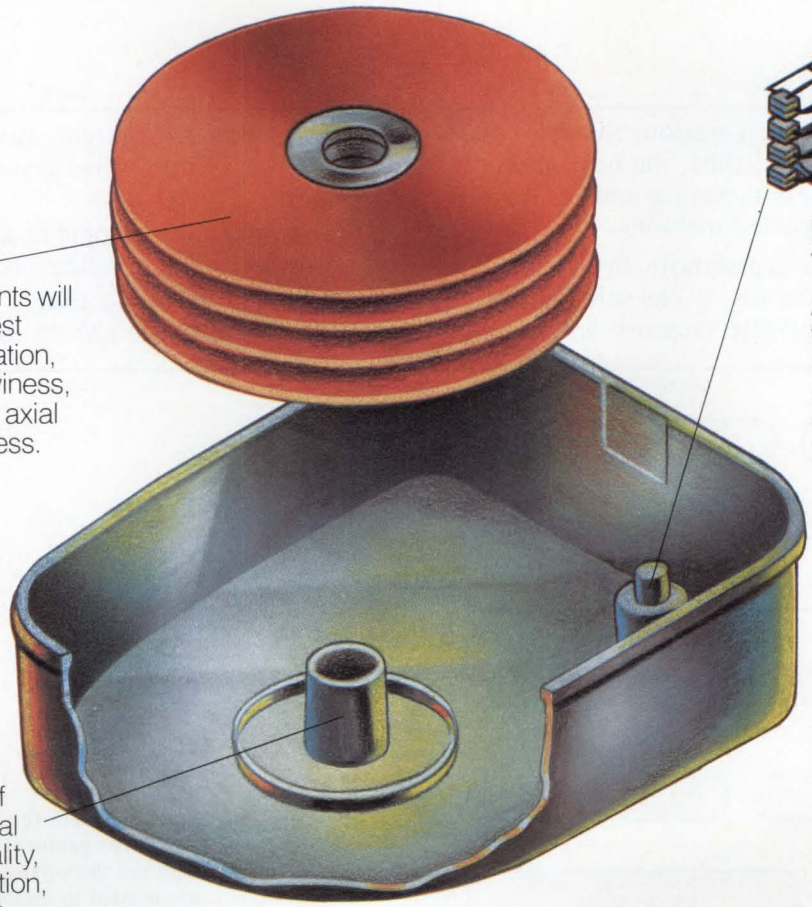

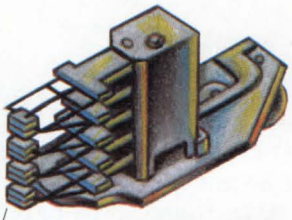

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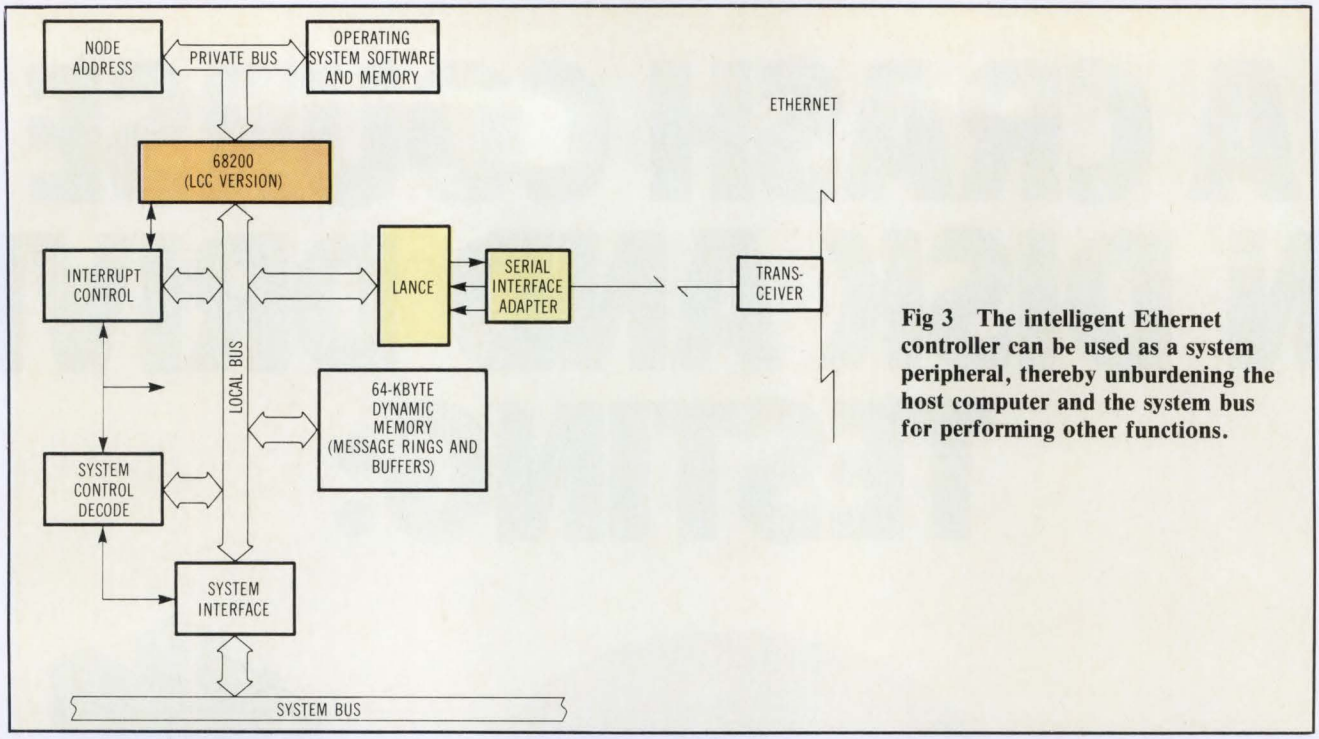

Fig 3 The intelligent Ethernet controller can be used as a system peripheral, thereby unburdening the host computer and the system bus for performing other functions.

host CPU. Using this configuration, the 68200 does not access the system bus; thus, the host must use its DMA function to pass messages and commands in and out via a two-ported memory.

While the 68200 can access both the local node bus and its own private bus, it has sole control of its private bus. The private memory will contain the node's operating system software required to implement the bottom three layers of the Ethernet specification (Fig 4).

Interface and control logic must be incorporated to perform local bus accessing as well as all of the memory access decoding that is required for the host, the 68200, and the LANCE to access memory.

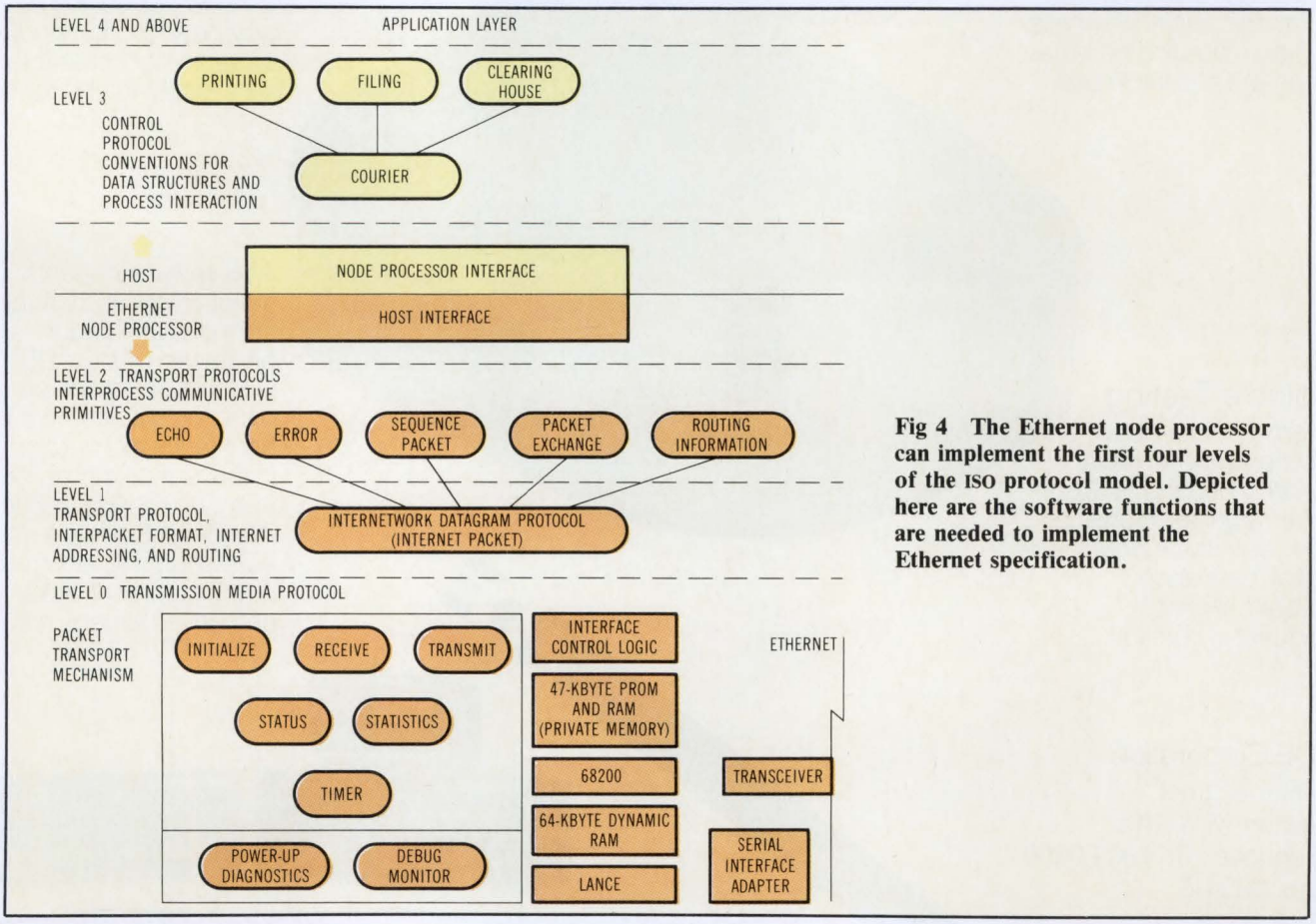

Fig 4 The Ethernet node processor can implement the first four levels of the ISO protocol model. Depicted here are the software functions that are needed to implement the Ethernet specification.

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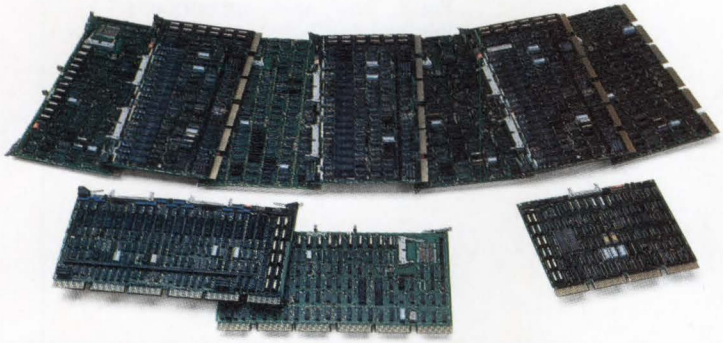

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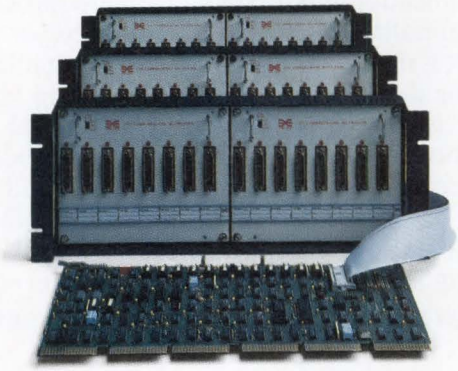

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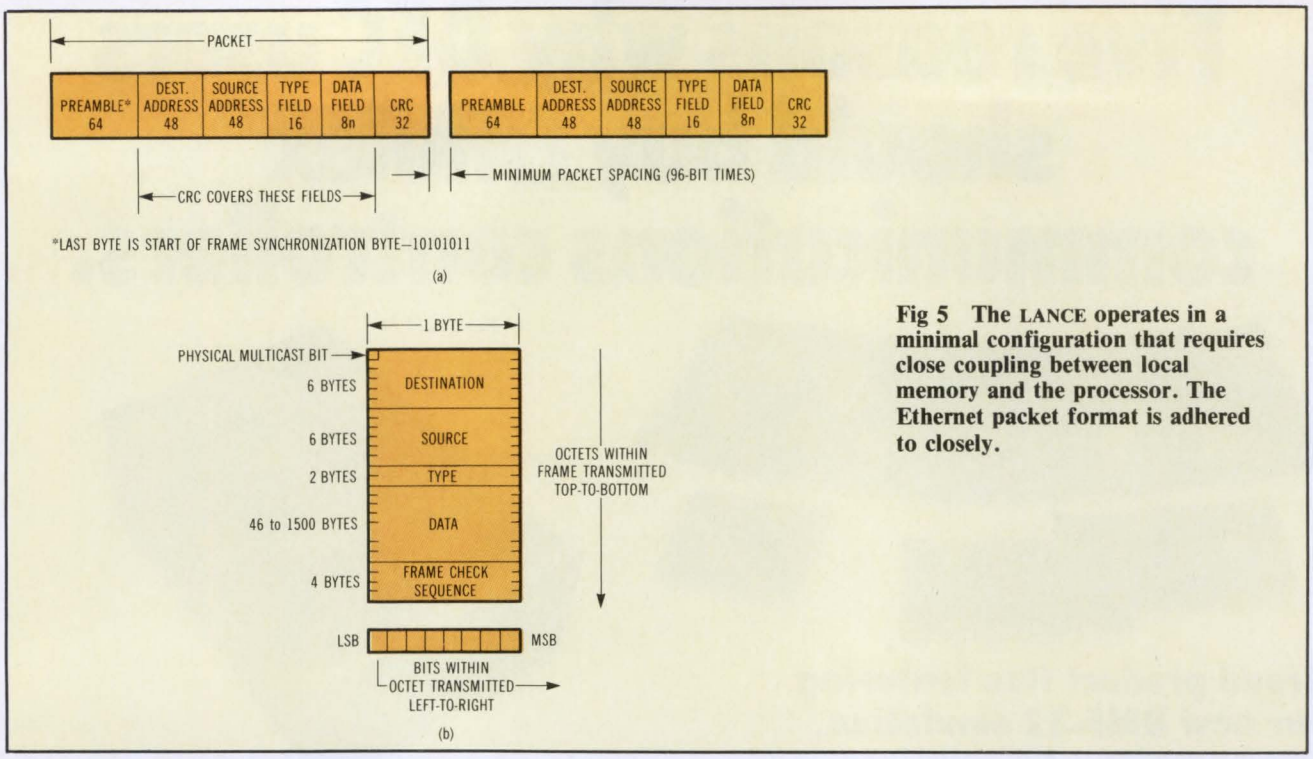

Fig 5 The LANCE operates in a minimal configuration that requires close coupling between local memory and the processor. The Ethernet packet format is adhered to closely.

If one were to implement the node processor scheme using true dual-ported memory (memory that can be simultaneously accessed from two sources without ill effect), the host would not have to gain access of the local bus. It could instead simply read and write to memory via one access port while the 68200 reads and writes to the memory via the second access port.

The Ethernet packet format consists of a 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and a 46- to 1500-byte data field terminated with a 32-bit cycle redundancy code (CRC) as shown in Fig 5. The variable widths of the packets accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (eg, 1024-byte disk sectors). Packets are spaced a minimum of 9.6 μs apart to allow a node time enough to receive back-to-back packets.

The LANCE is intended to operate in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between chip and processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operation mode of the chip via two control registers. It is only during this initial phase that the host processor talks directly to LANCE. All further communications are handled via a DMA machine under microword control contained within the LANCE. Fig 6 is a block diagram showing the LANCE and serial interface adapter (SIA) that is used to create an Ethernet interface for a computer system.

The intelligent node processor not only unloads a congested bus but it also implements higher level IEEE 802.3 protocols. With effective software, the

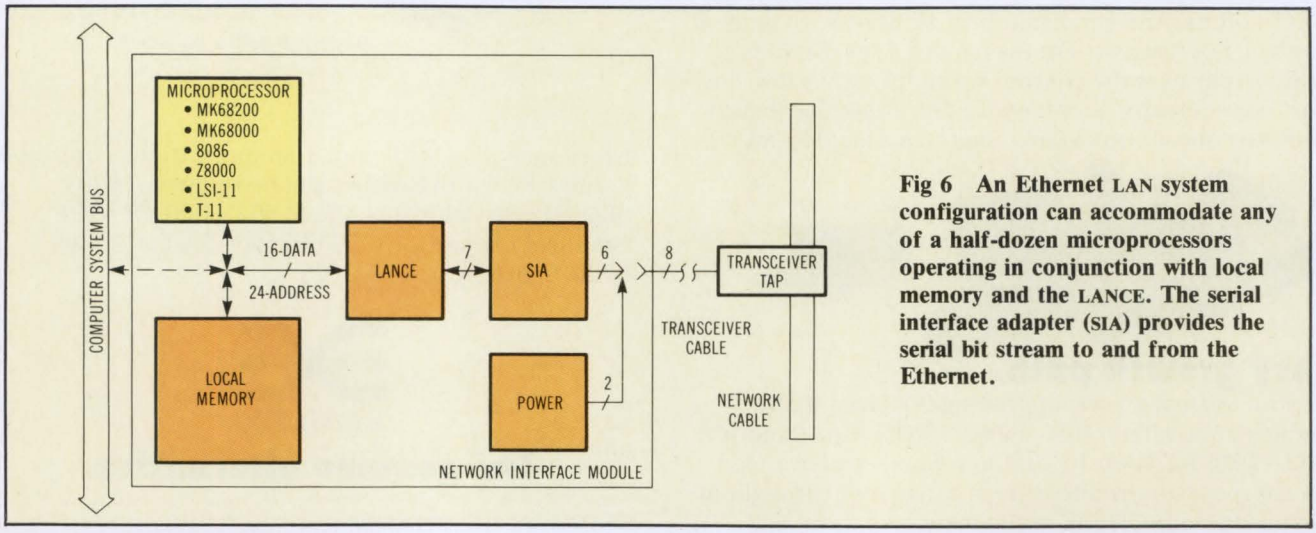

Fig 6 An Ethernet LAN system configuration can accommodate any of a half-dozen microprocessors operating in conjunction with local memory and the LANCE. The serial interface adapter (SIA) provides the serial bit stream to and from the Ethernet.

Ethernet controller chip comparison

The designer has a variety of VLSI Ethernet controller chips from which to choose. There are presently five Ethernet controller chips available: MK68590 (LANCE) from United Technologies/Mostek, i82586 (LAN) from Intel, the R68802 (LNET) from Rockwell International, the 8001 (EDLC) from Seeq Technology, and the MB61301 (DLC) from Ungermann-Bass/Fujitsu. These devices can generally be grouped according to performance by comparing the performance specifications of their respective data sheets. The LANCE and i82586 can manage multiple simultaneous transmit and receive buffers while the EDLC, LNET, and DLC can manage only one transmit or receive buffer at any one time. The Rockwell, Seeq, and Ungermann-Bass/Fujitsu devices meet the IEEE 802.3 specification, and although they support the implementation of ISO layers 1 and 2, they leave implementation of multiple buffer management to the designer. The LANCE and i82586 also provide all of the layer functions mentioned above, but do so with a sophisticated buffer management technique along with the physical Ethernet protocol functions.

Both the LANCE and i82586 access the transmit and receive buffers by first accessing the descriptor rings to determine the starting address of the message buffer. This method provides multiple buffers for both transmit and receive, and does not require the host to provide a buffer address for each message. The Rockwell, Seeq, and Ungermann-Bass/Fujitsu devices support only one memory address at a time for transmit and one for receive. Thus, the host must supply this address each time a buffer is allocated for either receive or transmit.

The Seeq, Rockwell, and Ungermann-Bass/Fujitsu controller chips require external hardware to implement DMA capabilities, while both the Mostek and Intel parts have controlling microcode to perform onchip DMA operations on both sequential receive buffers and sequential transmit buffers. The LANCE has a contiguous ring arrangement allowing up to 128 transmit and receive buffers. The i82586 uses a linked list arrangement that allows software control of the unlimited number of buffers for each side. Both devices provide for multiple buffers within a single transmit or receive frame.

Both the Intel and Mostek devices provide flexible memory arrangement, allowing the designer to interface them to operating systems with little software effort. Meanwhile, the Seeq, Ungermann-Bass/Fujitsu, and Rockwell devices require the hardware designer to plan a memory access arrangement that accommodates the local software environment, all at the expense of added board real estate. The LANCE requires contiguous, 8-byte-aligned, buffer descriptor rings that localize all the buffer descriptors at any properly aligned location within a 16-Mbyte address space, and also requires three word memory accesses to acquire the next buffer address. The i82586 device allows the buffer descriptors to be placed anywhere within a 64-Kbyte address range, with a linked list arrangement. It requires at least four word memory accesses to obtain the next buffer address. This is one more than the LANCE requires; the number of memory accesses is critical in sequential message handling.

Both the Intel and Mostek controllers have complete station, broadcast, and multicast address recognition capabilities. The Seeq chip requires external multicast address recognition. In contrast, Rockwell's chip supports only the single node and indiscriminate address recognition modes. LANCE, i82586, and the R68802 perform the binary exponential backoff algorithm, while the Seeq device performs only part of it. The Seeq device notifies the CPU of collisions and waits for CPU completion of the computed backoff interval.

Mostek's LANCE and Intel's i82586 must be regarded as superior devices to other available controllers. The LANCE and i82586 are equal in performance, with the exception of LANCE's greater allowable bus latency, which directly reduces the possibility of first in, first out (FIFO) overrun. According to Dale Taylor, Dave Oster, and Larry Green in their article, "VLSI Node Processor Architecture for Ethernet" (*IEEE Journal on Selected Areas in Communications*, Nov 1983, p 733), "The FIFO buffer in an Ethernet controller provides two valuable functions: more efficient bus/memory usage through multiple transfers for each bus acquisition (bursts) and more tolerance to long bus latencies. The deeper the FIFO is, the larger a burst transfer may be and the longer peak latency will be." Intel's FIFO is 8 words deep, while Mostek's FIFO is 24 words deep. It can be shown that the average allowable latency that LANCE offers is almost equal to twice that of the i82586, while the allowable peak latency is greater than three times that of the i82586. They continue, "the larger the allowable peak latency of an Ethernet controller is, the less likely it will suffer a FIFO overrun/underrun in a system with a heavily utilized bus."

node processor can implement International Standards Organization (ISO) layers 1 to 4—the physical, data link, network, and transport layers. These correspond to layers 0 through 2 in the Ethernet specification. As shown in Fig 4, there are software routines that must be executed in order to implement the bottom three layers of the Ethernet specification.

Layer 0, the transmission media protocol level, could be implemented by executing a basic software kernel. This kernel provides an interface between user software and hardware elements of the node processor. The kernel performs all nonsystem-bus I/O port addresses and interrupt vector locations. Basic hardware elements needed for level 0 are the 68200, LANCE, SIA, transceiver, memory, and interface and control logic.

To verify proper operation of the node, this kernel should contain basic power-up diagnostic software. The routine should include a memory test, an I/O register test, timer test, and the LANCE test. The LANCE test would implement an internal loopback checking routine that essentially transmits and receives the message at the same time.

A closer look at LANCE and the micro

The MK68590 LANCE is a 48-pin VLSI device designed to greatly simplify the interfacing of a microcomputer (such as the 68200) or minicomputer to an Ethernet LAN. This chip is intended to operate in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled NMOS technology and is compatible with several popular microprocessors.

The LANCE interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide, but byte transfers occur if the buffer memory address boundaries are odd. An added advantage is that the address bus is 24 bits wide.

One of the key features in LANCE is its onboard DMA channel and the flexibility and speed that it gives in communicating with the host, or the dedicated microprocessor, through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings (Fig A). There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "lookahead manner" to determine the next empty buffer in order to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

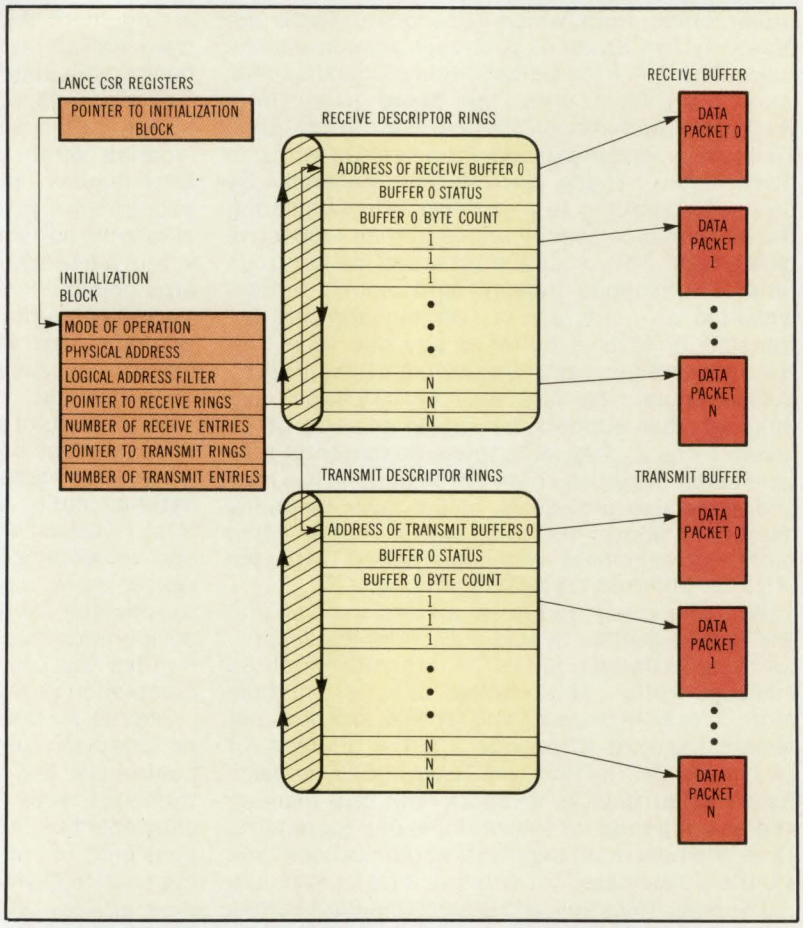

Fig A The LANCE memory management feature allows flexible communication between the host and common memory.

The 68200 is a recent addition to the 68000 family line (see "Microcontroller Addresses Control and Instrumentation" by Don Folkes and John Bates, *Computer Design*, Oct 1983, p 229). The chip is a

This would verify proper controller chip operation. The kernel should also contain some basic debugging software.

Software must also execute the basic operating routines of the transmission level. These include the initialization module, which initializes the LANCE to a particular mode of operation; the transmit and receive modules, which handle all buffer management of the descriptor rings; the network statistics module, which keeps track of collisions and other errors occurring on the net; the status module which keeps track of the node's activity; and the timer module, which generates timer interrupts needed for execution of upper level protocols.

Layers 1 and 2, the internet and transport layers, are implemented by the Ethernet node's user software. The function of layer 1's internet datagram protocol is to address, route, and deliver standard internet packets. Each of these packets is treated as an independent entity with no relation to other internet packets traveling throughout the system. The protocol must determine if the node has been addressed by either the broadcast or multicast method through the use of a software filter.

Implementing layer 2

In order to implement layer 2, primitives must be generated and contained in the Ethernet node's firmware to execute the following procedures: routing information, error, echo, sequenced packet, and packet-exchange protocols. The routing information protocol provides a means by which the data base is maintained in a dynamic manner and therefore the way routers direct

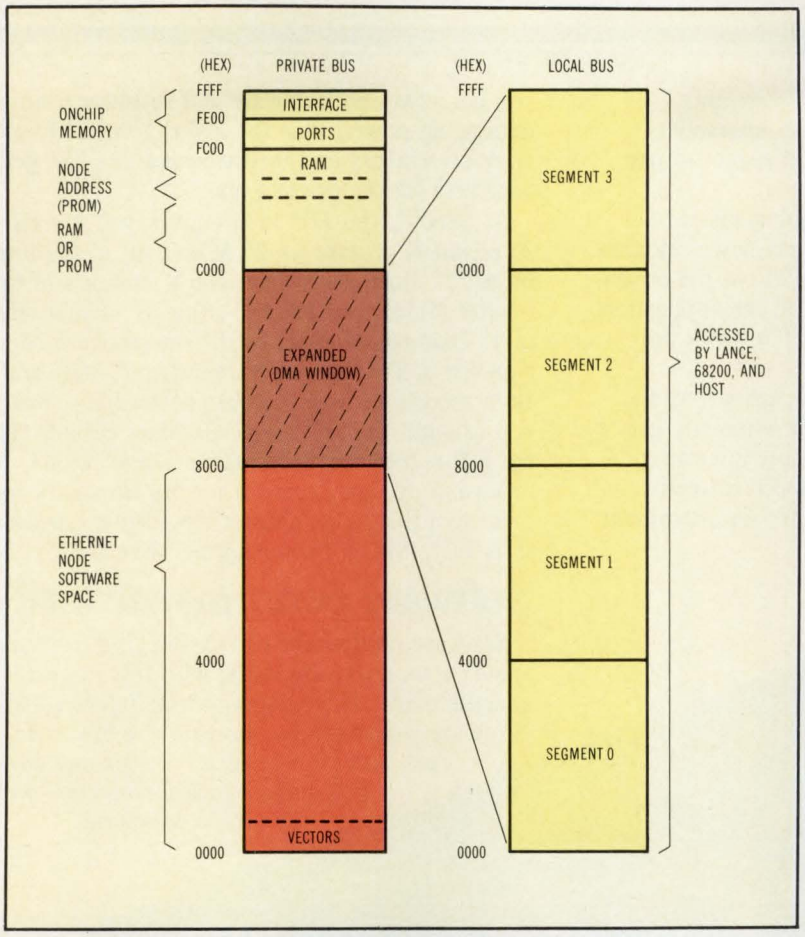

Fig B On the memory map of the 68200 and the GP-LCC configuration, DMA window expansion allows access of up to 111 Kbytes of memory.

16-bit microcomputer chip with onchip CPU, ROM, RAM, and I/O that provide parallel expanded bus modes operating with a full complement of multiprocessing features. The user can select I/O architecture allowing the device to operate both as a high performance single-chip microcomputer with a fully expandable CPU that can address external memory and I/O, and as a dedicated I/O controller that can share a 16-bit system bus with a 68000 or other types of 16-bit microprocessors. This architecture makes it an apt choice as a node processor for standalone or peripheral configurations. In addition, the 68200 provides an onchip serial I/O port that significantly reduces the amount of interfacing hardware needed to connect the Ethernet node to a serial device such as a terminal.

Forty of the 48 available pins on the device can be used for I/O, and their functions are programmable. I/O capabilities include parallel I/O, three timers, a serial channel, and an interrupt controller. In the single-chip configuration, all 16 bits of Port 0, and 9 bits of Port 1, are used for general purpose I/O. Up to three of the pins on Port 1 can be programmed as external interrupt sources, and up to four pins can be programmed as I/OS for the onchip serial channel. All 8 bits in Port 4 can be used as simple inputs or outputs or can serve as timers. For example, TAI can be used as an input for timer A, an interrupt source, or a general purpose input pin. If it is used as an interrupt source, it can be selected simultaneously with either of the other two functions. With the LCC 68200 version in the bus grant mode, the processor can access up to 64 Kbytes using the system bus and up to 47 Kbytes using the private bus and onboard RAM (Fig B). Thus, the 68200 can access up to 111 Kbytes of memory. The LCC allows the 68200 to grant system bus use to a host or peripheral, and private bus use for concurrent operations.

packets to other routers on their way to the final destination. The error protocol provides a means for error reporting when a packet has been discarded. It is intended as a diagnostic tool for analyzing network performance. The echo protocol is used simply to echo, or return each received packet to its source in order to verify proper operation. The sequenced packet protocol provides transmission of successive internet packets by the use of sequence numbers.

Using these numbers ensures proper rearrangement of a packet once it reaches its destination. The final software required for the intelligent node processor's operation is the interface software. This is necessary to ensure proper communication and message transfer between the host and the node processor.

The chip count for implementing intelligent nodes is low enough so that the entire intelligent Ethernet controller can be placed on a single standard PC board such as VME, Versabus, or Multibus. This facilitates an easy system integration of Ethernet throughout the entire product line, regardless of the particular application. Standard software may be written for the Ethernet frontend processor, and unique software may be written to enable the host to implement particular applications.

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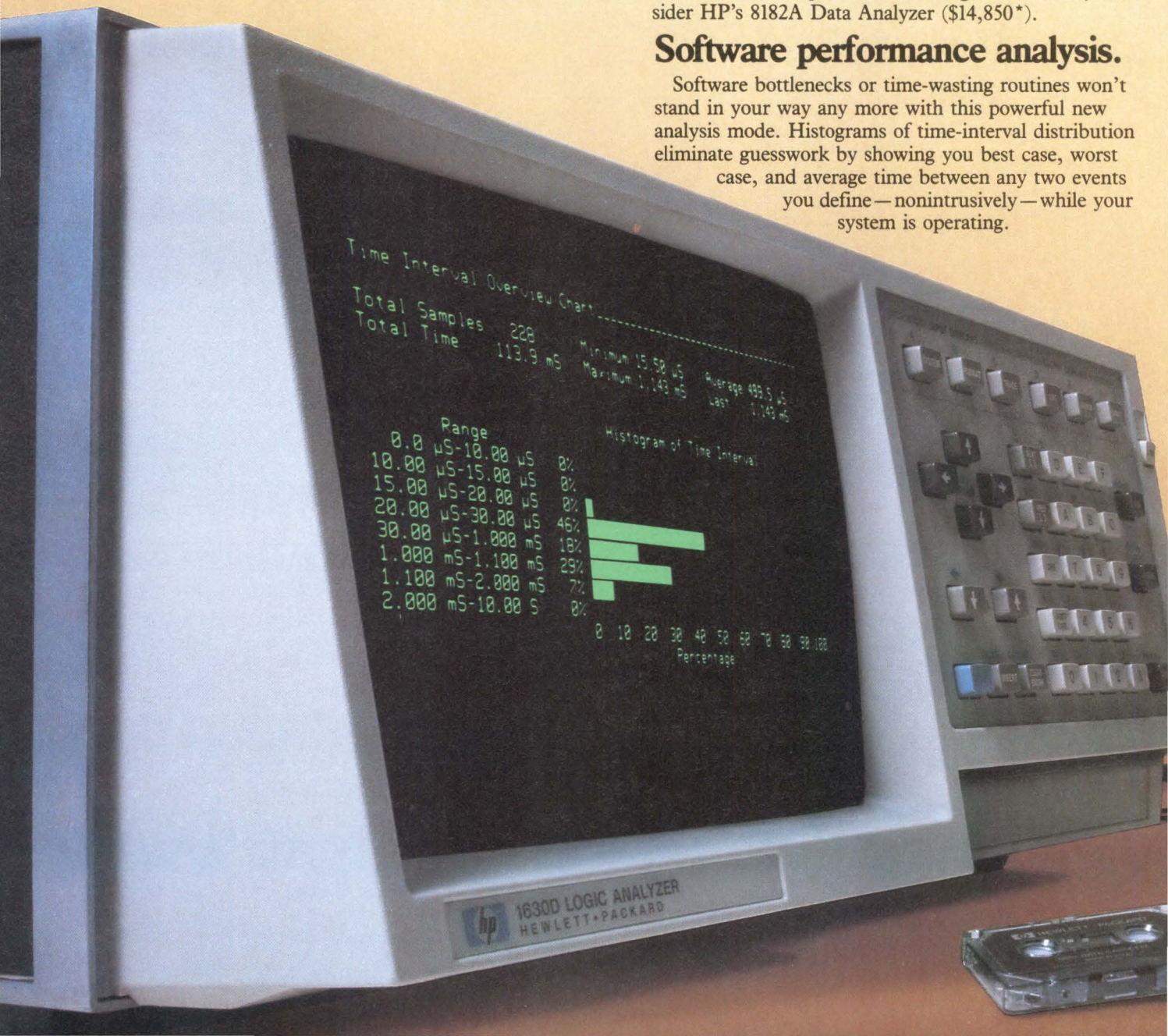

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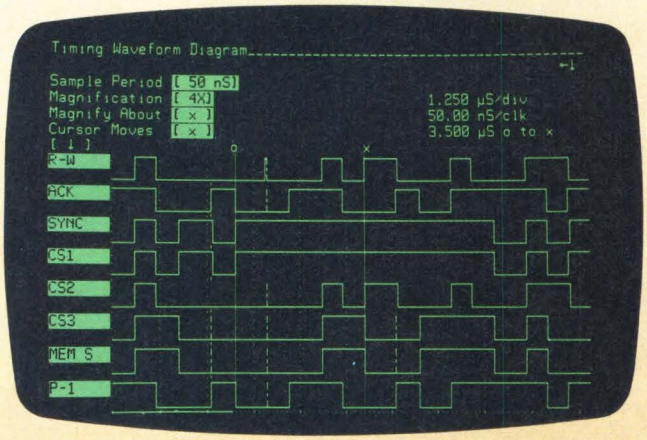

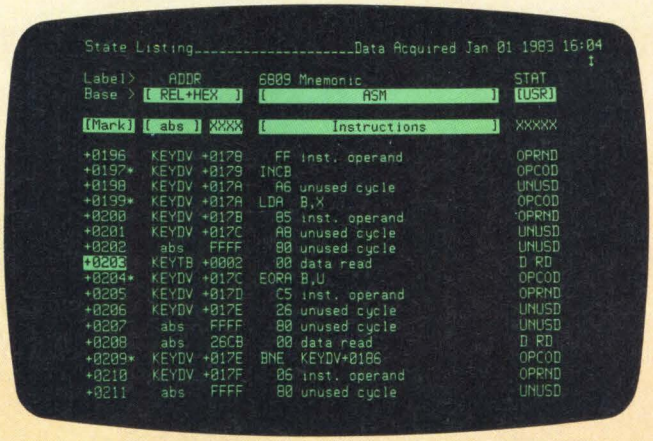

Timing analysis.

For timing analysis, the HP 1630 gives you pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. You can also monitor bus activity in the state mode, trigger on a given bus pattern, then view asynchronous status and control line activity in the timing mode. This quickly unravels problems such as I/O port malfunctions.

State analysis.

In the state mode, four user-defined terms can be used in any combination to define sequence, store qualification, trigger and restart conditions, so you get right to the problem. But that's not all. The HP 1630 makes it easier yet by letting you assign alphanumeric labels to input channels and status or control line patterns. Measurements are then displayed in your system's terminology for rapid interpretation.

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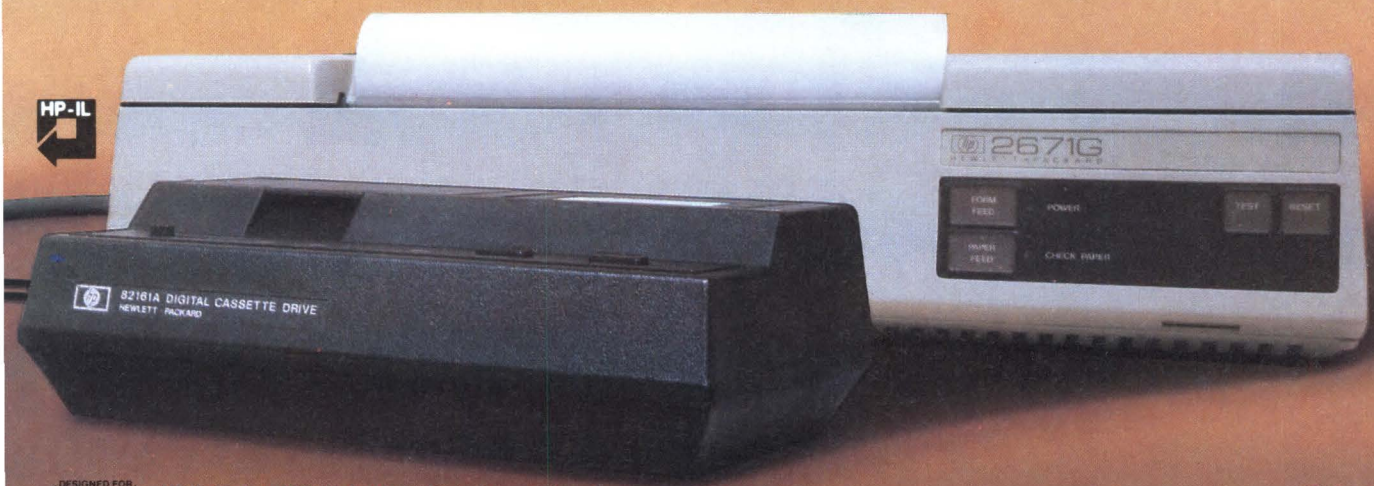

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ADM 3A
ADM 31

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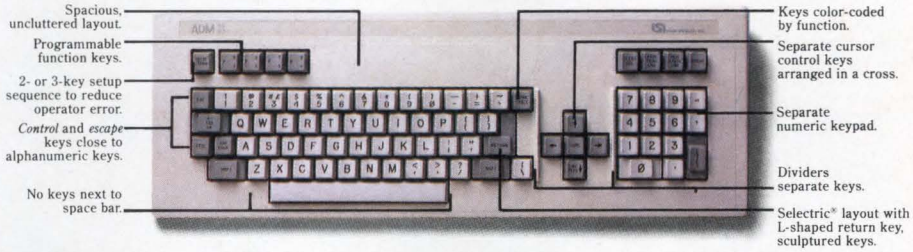

Low-profile, tapered, DIN-standard keyboards with Selectric layout feature logical key groupings and adjustable tilt for comfort and efficiency. ADM 11 shown above.

	ADM 11 Conversational	ADM 12 Editing	ADM 24E Host Programmable
Programmable Function Keys	4 (Shiftable to 8)	16 (Shiftable to 32)	16 (Shiftable to 32)
Non-Volatile Function Keys	Optional	Standard	Standard
Function Key Legends on 25th Line	From Host	From Host	Standard Non-Volatile
No. of Pages of Display Memory	1	2	4
Display Memory Configurations (Plus 25th Message/Status Line)	24 Lines by 80 Characters	(2) 24 x 80 or (1) 48 x 80 or (1) 24 x 158	User Definable up to 96 x 80
Scrolling	Standard Scrolling	Smooth, Jump or Horizontal Scrolling Split Screen	Smooth or Jump Scroll Split Screen
Transmission Mode	Conversation Mode	Conversation or Block Mode	Conversation or Block Mode
Editing	Limited	Full Editing & Protected Fields	Full Editing & Protected Fields
Visual Attributes: Reduced Intensity, Blink, Blank and Reverse Video. Underline also on ADM 12 and ADM 24E	3 Embedded 1 Non-Embedded	4 Embedded, 1 Non-Embedded or All Non-Embedded, plus Full Screen Reverse Video	5 Embedded, 1 Non-Embedded or All Non-Embedded, plus Full Screen Reverse Video and Highlight
OEM Flexibility	Modifiable Set-Up Characteristics	Modifiable Set-Up Characteristics & Personality	Modifiable Set-Up Characteristics. Add to Program in ROM or Down-Line Load in RAM (56K ROM or RAM. Up to 22K Display Available) Room for additional Logic Boards.
Terminal Compatibility	ADM 3A, ADM 5, ADDS Viewpoint & Regent 25, Hazeltine 1400, 1420 & 1500, DEC VT-52	ADM 3A, ADM 5, ADM 31, ADM 32	ADM 3A, ADM 5, ADM 31, ADM, 32, ADM 42

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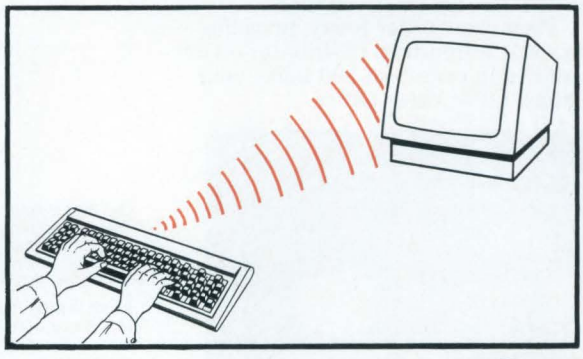

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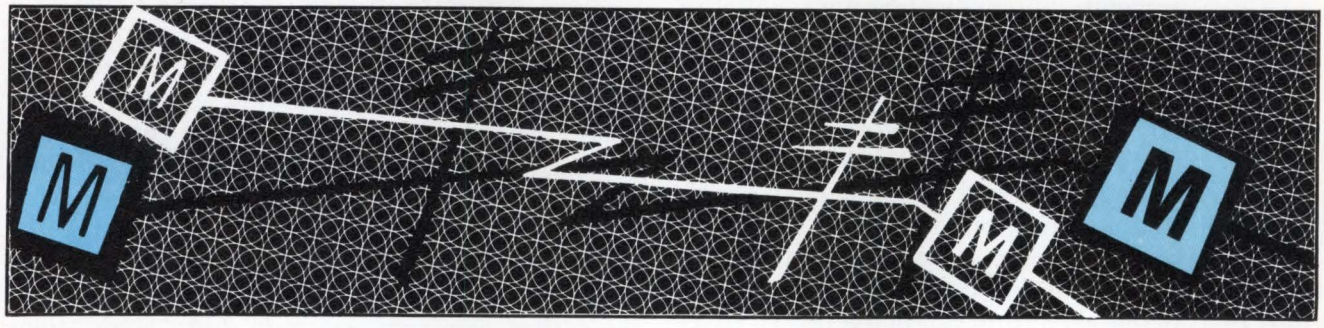
CIRCLE 107

ESTABLISHING THE MICRO-TO-MAINFRAME CONNECTION

The 3270 emulator accommodates coaxial link with RS-232 serial data on the same card.



by Dan Erlin

As more personal computers are used in the corporate environment, their usefulness is hampered by the lack of communication with the mainframe. Establishing an effective communication link is becoming a necessity.

Given the preponderance of IBM mainframes in medium-to-large corporations, a desirable feature of the mainframe-to-PC interface should be an easy adaption to IBM's own communication environment. In most cases, this means emulating IBM's 3270 family of controllers and terminals. International Data Corp, a Framingham, Mass market research firm, estimates that 80 percent of potential IBM users want mainframe connectivity via 3270 protocols.

Dan Erlin is founder and chairman of Forte Data Systems, 1500 Norman Ave, Santa Clara, CA 95050. Mr Erlin holds a BA in business from the University of Southern California.

What is the best method? The PC can be connected to a host in a number of ways for it to perform the desired interactions and then return to its local processing tasks. In most cases, the PC must emulate another device to accomplish this.

One way is to use an asynchronous link, which is the most familiar and also the least expensive. However, while this link is appropriate for some applications, its typical data transmission rate of 300 to 1200 baud can limit its usefulness. A synchronous link, on the other hand, has the PC emulate the 3274 control unit, operating at 1200 to 9600 baud. While faster than an asynchronous connection, the synchronous link ties up a dedicated port on the host that could be put to better use by a cluster controller that is capable of supporting up to 32 users.

Protocol converters are currently available that can emulate a remote 3274 controller connection to the IBM 3705 communication processor and communicate with the PC over a switched or leased asynchronous line. This type of converter provides the user with full-screen capability. It also permits access to the mainframe by a number of PCs. This method, however, is not very cost efficient.

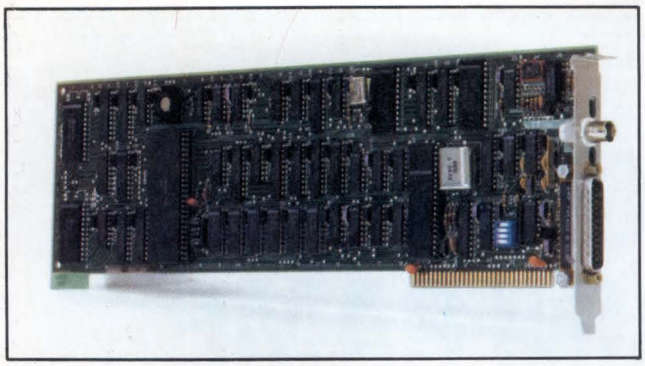


Fig 1 Plugging a PC78/79 into an IBM PC lets the user fully emulate the IBM 3270 environment. The board and its associated software are transparent to the operating system, access method, and application. The board includes an RS-232 link that is MS-DOS compatible and allows the PC to attach to printers and other peripherals.

Although connection costs vary considerably, there are common factors to consider when estimating total costs. These factors include the necessary modems, communication lines, and host frontend costs. In general, the most economical connection is a PC-to-mainframe link via coaxial cable. Coaxial cable provides a ready-made data pathway, but currently many personal computers do not have access to that pathway. Also, the coaxial link is incompatible with the available personal computer's communication interface.

Within the past year, however, a handful of companies have introduced circuit boards that fit into an available expansion slot in the IBM PC or XT and thus provide that essential coaxial link. The board permits PC connection directly to the category "A" coaxial cable of a 3274/3276 cluster controller. No modems, phone lines, or special cabling are required. In addition, the control unit can be channel attached or remotely attached using binary synchronous communication (BSC) or systems network architecture/synchronous data link control (SNA/SDLC) protocols through the frontend processor. The associated software enables the PC to emulate a 3278-type terminal/display unit.

Transparency as a goal

Forte Data Systems' PC78/79 interface board and its accompanying software can be used with the IBM PC in any operating environment where a 3278/3279 terminal is appropriate (Fig 1). The PC78/79 is transparent to the operating system, access method, and application. The PC can thus fully emulate an IBM 3278, models 2, 3, 4, and 5, or in the case of a PC with color monitor, emulate the 3279, models 2A, 2B, and 3A (Fig 2).

The PC78/79 software allows all communication and emulation functions to be soft loaded. Future upgrades or enhancements are accommodated by swapping diskettes without making any changes in PROM. Having the functional ability resident on the disk also allows an easy adaption to various vendors' hardware. It is not necessary to design a new set of PROMs for each manufacturer.

In addition, a file transfer utility, which uses special interfacing subroutines, permits downloading of data files to the PC. These data files can then be manipulated by PC-resident application software. Menu selection, under MVS/TSO and VM/CMS operating environments, performs file transfers. Interfacing subroutines used in the file transfer enable end users to also write PC applications that can converse with host applications through the processor board.

To make the IBM PC function efficiently in the emulation mode, its processor (the Intel 8088) must not be burdened with communication responsibility. In addition, a high speed microprocessor on the PC78/79 board provides complete 3278 line protocol compatibility and maintains an image of the current 3278 display screen. This image is available for

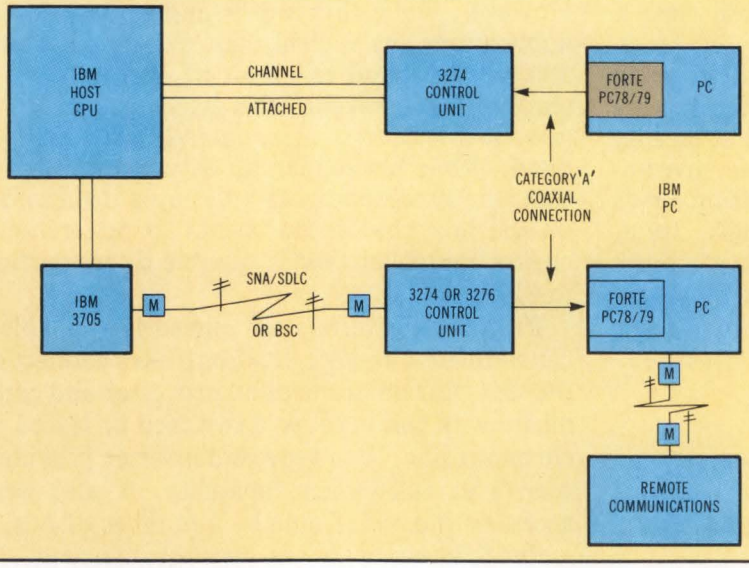


Fig 2 The micro-to-mainframe link can be established in two ways with Forte Data's PC78/79. The control unit can be channel attached or remotely attached using BSC or SNA/SDLC protocols. Either way, the PC is linked to the controller via the category "A" coaxial connection.

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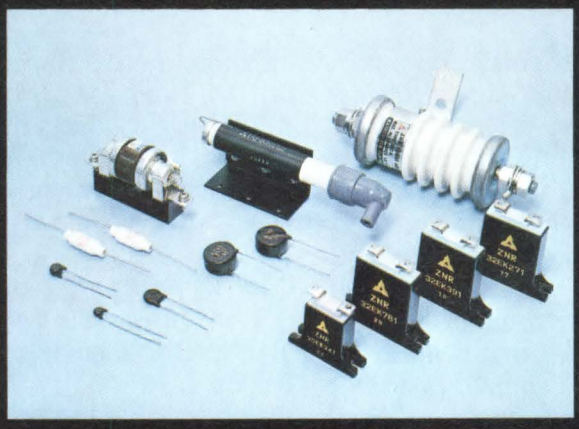

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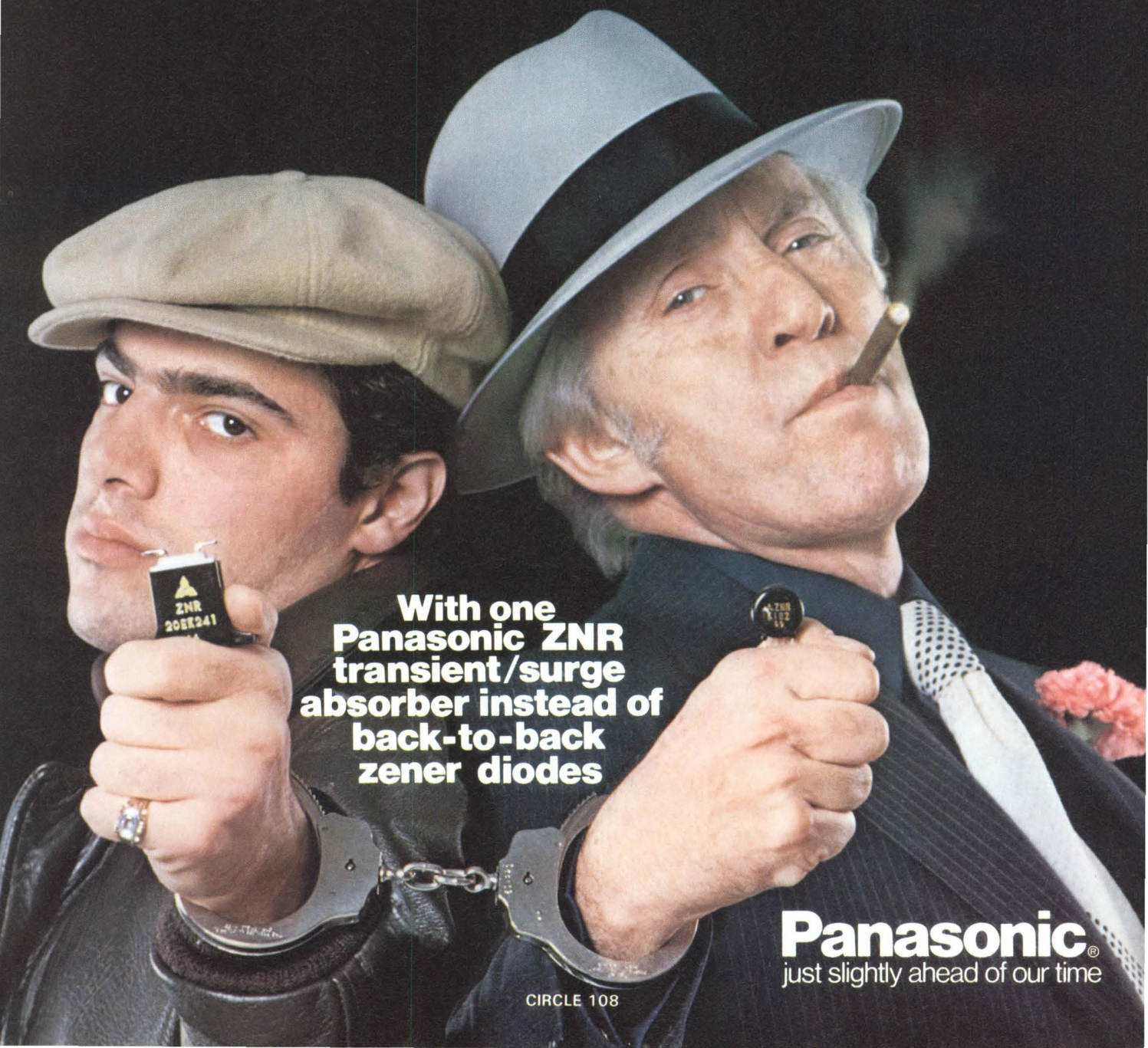

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presentation when the PC is in its emulation mode. The microprocessor's architecture allows concurrent and independent operation of host and PC programs. The operator need only strike a single command key to place the PC in the emulation mode or return it to the current PC program.

A serial RS-232 interface provides access to a local printer, modem, or other peripherals. The serial interface and the coaxial link are combined on one card. This frees an expansion slot that is normally allocated to IBM's asynchronous adapter board.

Under MS-DOS, the user has the choice of operating in a resident or nonresident mode. The emulator program can become a subroutine to DOS, thus allowing the operator to toggle between the host environment and the MS-DOS environment. While resident 3278 emulation may require the PC to be configured with an additional RAM, the advantage of freeing up disk drives or other system resources may warrant this configuration.

The ability to configure various other elements with the PC78/79 is an added bonus. Customer preferences of keyboard layout can be accommodated, such as converting the IBM PC layout to the conventional 75-key ASCII keyboard. The user can also define the PC colors for any of the 3270 fields. In addition, multiple displays and monitors can be configured.

Eyeing the competition

Converting the PC into an intelligent workstation replacement for 3278-type terminals has also been addressed by IBM. The company has announced shipments of an emulation adapter and control program to begin in April of this year. As in Forte Data's device, which was first shipped some 10 months ago, the connection will be made via the coaxial cable to the 3274 control unit.

A close examination of IBM's emulator package, however, reveals a certain lack of consideration for the end user. For instance, unlike Forte Data's incorporation of the 3270 and RS-232 interface on the same board, IBM lacks an asynchronous RS-232 interface. While both products allow screen copy of the 3278/3279 session to a supported printer that is attached to the PC, the PC78/79 provides easier screen capture to the PC-DOS file. Diagnostics are standard in the Forte Data package.

In developing its emulator package, Forte Data has provided PC users with important benefits achieved with soft-loaded software. While the potential for PC-to-mainframe connections has not been completely exploited, the software emphasis has furnished users with the tools to completely integrate their system. PROM or ROM are not required to be replaced when enhancements and upgrades are developed. This is not the case with the IBM emulator package.

The two products differ in other respects, with each having strengths and weaknesses. However, if performance is the primary criterion, Forte Data's PC78/79 delivers more capabilities and flexibility.

C for flexibility

The source code for the PC78/79 is written in a high level C language that gives the end user good flexibility to modify the emulation program. The card is then used as an I/O device and software can be compiled under a different operating system. For example, the emulation program could be modified to be compatible with QNX, a Unix (Bell Labs) look-alike operating system for the IBM PC that is marketed by Quantum Software Systems, Inc (San Jose, Calif).

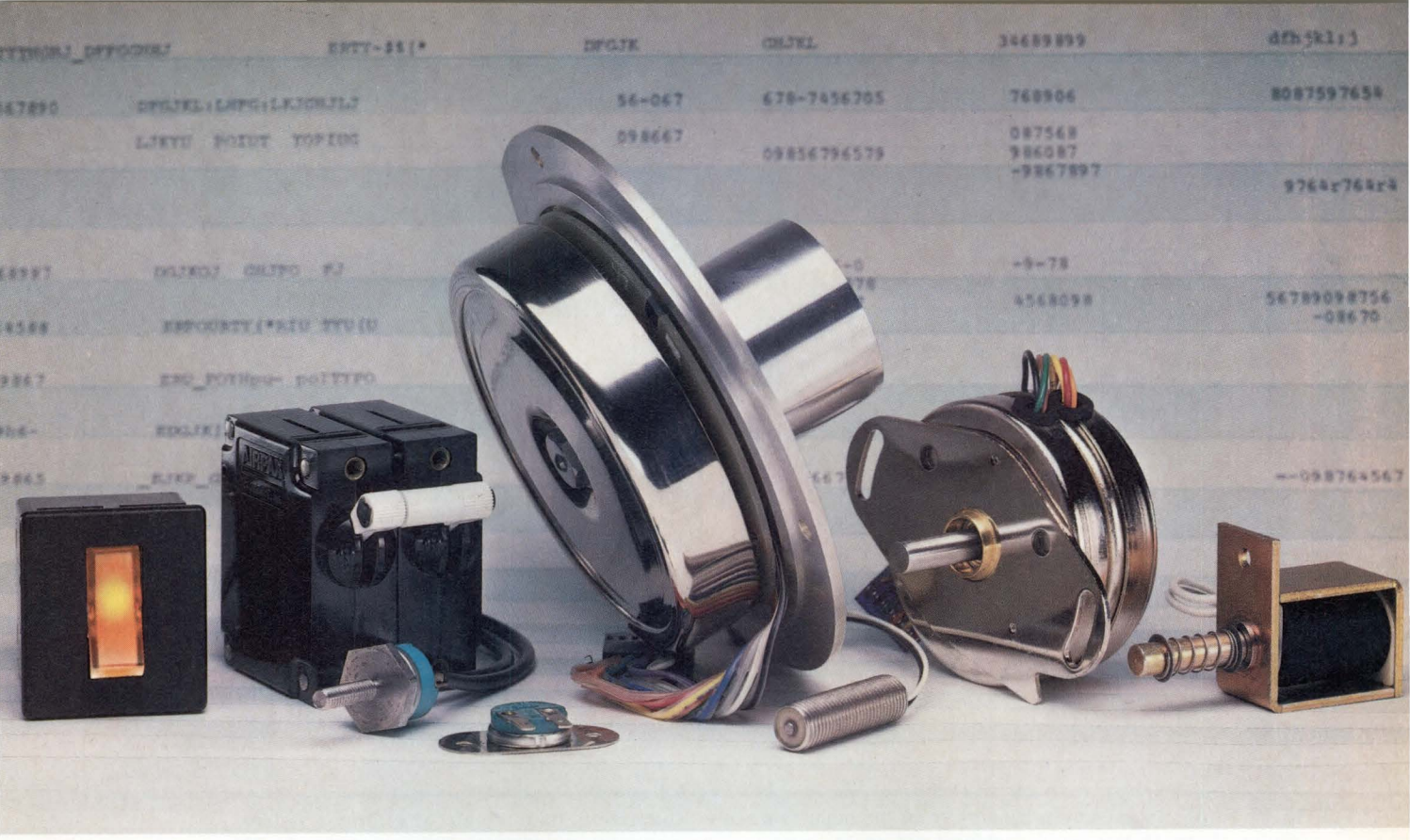
The PC78/79 card has an onboard parity-checked screen buffer that ensures consistency in the error checking system. Data is received with parity, buffered with parity on the circuit board, and then transferred to the application program with 100-percent integrity. For users who transfer numerical and statistical data files, this feature is especially important.

Identifying problems that occur during initial load or during operation can sometimes be difficult for the experienced operator and next to impossible for the novice. The Forte Data product includes two diagnostic modes to alleviate user frustration. First, power-on diagnostics are executed before the PC78/79 attaches itself to the coaxial line. In addition, local diagnostics, which are menu driven, can be run to isolate problems suspected by the user.

The diagnostic portion of the program, called INSTALL, appears as a separate DOS command to the user. When executed, it allows the user to ascertain the error, obtain information on corrections to make (via INSTALL), and then proceed to solve the problem at hand.

While the ability to interface with the mainframe greatly increases the PC's utility, the next generation of products should more fully integrate the PC into the mainstream of a company's data processing facilities. In order to take full advantage of the PC-to-host coaxial connection, users should be able to take data they have developed with PC applications and make that information available to the mainframe, and from there to other PC users on the network.

Forte Data is planning to follow that direction with future products. The emphasis will be on the communication requirements of the end user—to provide the operation with a much faster and easier transfer of data and data files. Access to the data



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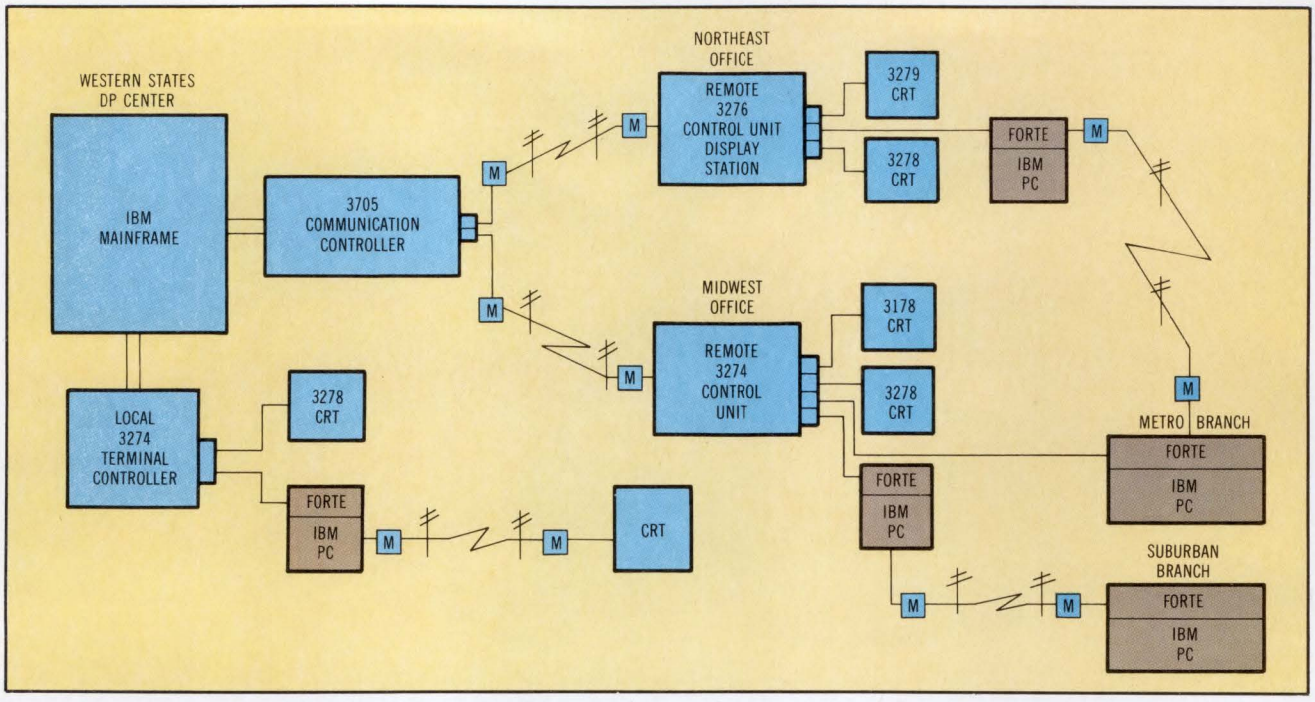

Fig 3 To obtain maximum benefits from the mainframe-to-PC connection, users should be offered a system solution. Forte Data's future products will enable users to fully access the mainframe's data processing facilities, and to transfer data to and from the mainframe, and also to other PC users on the data network.

will be provided via familiar PC-DOS commands. Users should not be burdened with having to learn the mainframe's operating system or contend with separate communication software. In a word, transparency will be the key to future enhancements. Currently under development is a hardware/software package that will offer four major functions: storage capability of PC-generated files on the mainframe, electronic mail capabilities, complete data and file transfers between the host and the PC environment, and availability to the personal computer of the mainframe's batch processing facilities.

Future capabilities will allow the host computer to be an information repository for PC-generated data (Fig 3). Most personal computers have two locally attached floppy disks for storage. This slows down some tasks that are data intensive. If the host computer can offload PC-generated data, then this would effectively add a gigantic hard disk drive to every PC on the network. Since the method of communication is via the coaxial cable, which permits data to be transferred at a rate of 2.35 Mbits/s, the PC user experiences no performance degradation while maintaining the access speeds of the floppy disk.

The disk space on the mainframe would be accessible by any user who could link to the owning user's director. This way, data could easily be shared between PC users, even if located in different buildings or separate locations. (Some form of encryption or decryption would be needed to maintain file security.)

Even though the file setup in the mainframe is enormously different from setting up PC files, Forte Data's new product would provide an almost transparent method to transfer data. Commands learned on the PC for manipulating floppy disks would be usable to move files to the mainframe and back again. This function would allow a PC operator to capture live data from an online data base and use the information in an electronic spreadsheet or other computation. For example, a company's accounting files would reside in the mainframe and normally not be accessible to an individual manager. Given the new capability, the manager could retrieve the profit-and-loss statements for the last six months from the online data base and analyze the data on the PC using the VisiCalc-like application program.

The overriding objective of the functions just described is to increase the capability and productivity of the personal computer. Forte Data's operating philosophy is to move the personal computer away from acting as a standalone computer to functioning as a truly interactive professional workstation.

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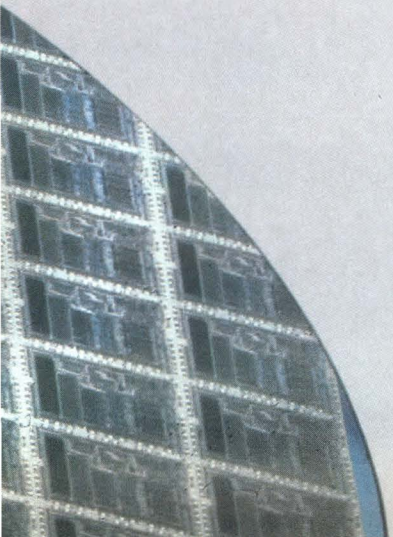

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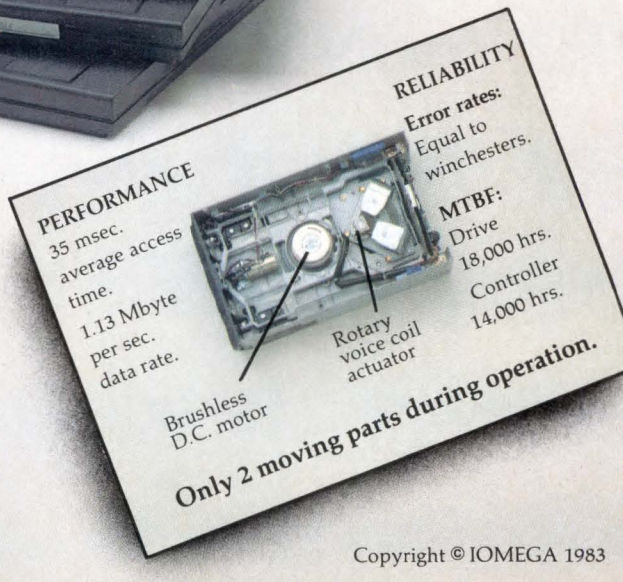

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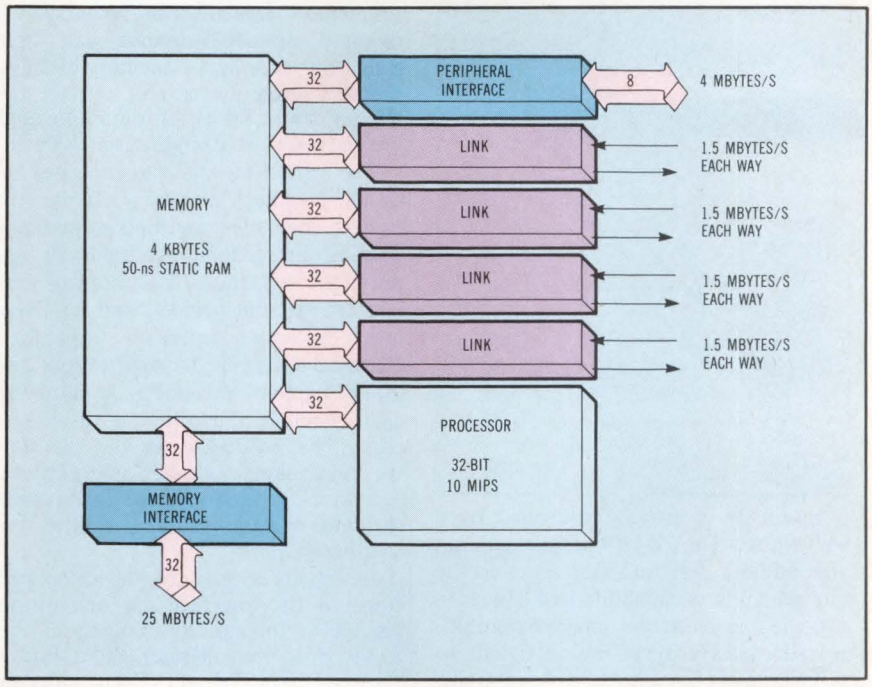


Transputer—a programmable component that gives micros a new name

It is a cross between a computer and a system building block, like a transistor, and it executes 10 MIPS. The entire IMS T424 transputer consists of a small, fast processor, 4 Kbytes of memory, interfaces to external memory and peripherals, and four high speed communication links. The transputer can respond to external interrupts within 600 ns and support simultaneous block transfers between the peripheral interface, the four standard links, and memory without significant degradations in processor performance.

System architecture is optimized to execute Occam, a concurrent programming language that was used to design the transputer itself. This software sees the system as a collection of concurrent processes that communicate with each other and with peripherals through channels. Programs are built from three primitives: assignment, input, and output. Assignment changes the value of a variable, input receives a value from a channel, and output sends a value to a channel. The same Occam program that a transputer network executes can run unchanged by a smaller network or a single transputer.

The three processes combine to form sequential, parallel, or alternative constructs. A construct is also a process, and can act as a component for another construct. Conventional sequential programs translate into Occam via variables and assignments, which then combine to form sequential constructs.

Concurrent programs translate to Occam by combining channels, inputs, and outputs to form parallel and alternative constructs. Each channel provides a one-way connection between two concurrent processes that communicate when both are ready. An alternative process may be ready for input from any channel, so that input is taken from the first channel to be used for output by another process.

Besides Occam, the transputer processor can be programmed in industry standard high level languages, such as C or Pascal. The processor executes programs sequentially—it implements parallel processes by sharing its time between the process sets that are active at any instant. For example, a currently running process continues to execute until it requires I/O communication. At that point, the processor temporarily abandons the running process in favor of the next process on the active queue. When the processor communicates with a ready channel, the message passes to the waiting process, which then goes to the end of the active queue.

Supporting two priority levels—0 for high and 1 for low—the processor maintains a queue of active processes for each level. When there are no active priority 0 processes, the latency is typically 600 ns, maximum 2600 ns. (Latency is defined as the time from the instant an external channel is ready to the start of the first instruction of the relevant waiting priority 0 process). If a priority 0 process is already executing, the waiting process links to the end of the priority 0 queue.

Four standard Inmos high speed links provide transputer communication and a variety of network configurations. Each link has two Occam channels: an output, and an input to carry data and link control information. Links operate independently and provide block transfers between transputers. The sending transputer transmits messages as a sequence of bytes, then awaits an acknowledgment. This signifies that the receiving transputer is ready to accept another byte.

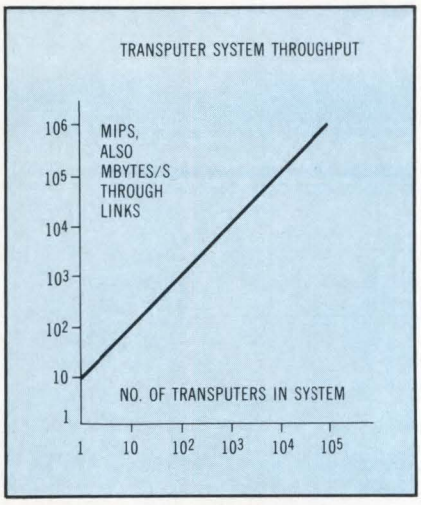
Transmission is continuous because the receiving transputer acknowledges as soon as it starts to receive a data byte. Moreover, this asynchronous protocol guarantees reliable transmission despite sending or receiving delays. During transmission, both processes are set inactive and will link to the end of their respective active queues only after final byte acknowledgment.

Software sets data rates on each link using the LinkSet configuration channel. Highest frequency is 20 Mbits/s for a maximum data rate of 1.8 Mbytes/s on a channel.

Separating the peripheral interface from the memory interface optimizes each one for its principal function. The memory interface supports mixed memory systems that generate signals for both nonmultiplexed and multiplexed memory. Memory timing is selected by a

(continued on page 244)

(continued from page 243)



program or externally controlled by a wait signal. The 32-bit multiplexed data and address bus interface extends the internal address capability to 4 Gbytes in a single linear address space. Nonmultiplexed cycles provide timing signals to drive industry standard RAMs and ROMs, while the multiplexed cycle provides RAS and CAS control signals for external address multiplexers.

Memory cycle types can be externally selected after the address is outputted, so memory systems can be mixed. If required, an asynchronous wait input externally determines memory timings. Memory cycle times and refresh frequency can be set by a program through the ExtMemSet configuration channel.

The peripheral interface accesses industry standard devices such as controllers, memories, and microprocessors. Its 8-bit bidirectional bus inputs or outputs byte sequences. Two control lines address external devices, and an Event input provides interrupt capability. Accessed via four standard output and input channels, the interface allows all eight channels to use the same 8-bit data path. The processor initiates transfers via handshaking. Transfers are synchronized to a separate external clock; asynchronous operation is also permitted, but at a lower speed.

Externally addressable device connections to the interface use one output channel as the address channel, another as the write-data channel, and a third as the read-data channel. Both addresses and data can be arbitrarily long byte sequences. The 4-Mbyte/s data rate allows the connection of high performance peripheral chips without FIFOs or DMA controllers.

Similar to an interrupt, the Event input communicates with a waiting process to schedule it. Typical latency is 600 ns. This input also enables the peripheral interface to respond to an access from a standard microprocessor bus.

To summarize, the entire transputer incorporates a number of hardware processes that represent its main concurrent elements. First, the processor receives an Occam program through one of the transputer communication links and begins executing. Second, the link controllers determine the state of their channel pairs and communicate with external devices.

Meanwhile, the memory interface controller determines the state of the memory interface and communicates with external memory. The peripheral interface controller follows along the same lines. In turn, the processor communicates with these hardware processes using a set of standard channels that is program controllable. The entire transputer process results in concurrency needed for high performance systems. Samples of the T424 will be available in the second half of 1984. **Inmos**, PO Box 16000, Colorado Springs, CO 80935.
Circle 260

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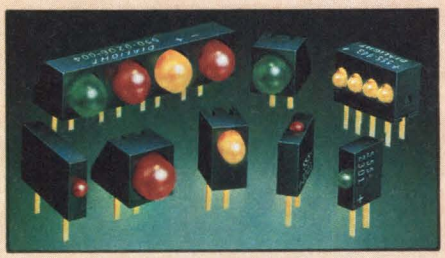

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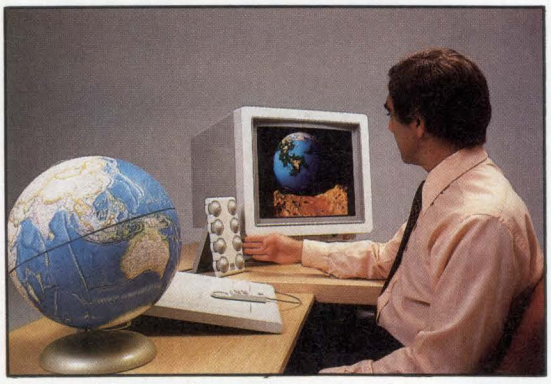
CIRCLE 115

Graphics system functionality swells with million addressable points



Designed for a wide-ranging engineering and scientific work, the 5080 graphics system produces precise, highly detailed displays. The compact system has a display, a graphics processor, a channel controller, and auxiliary software and peripherals.

The 5085 graphics processor performs a variety of graphics operations. These include high speed vector-to-raster conversion, polygonal area fill, circle generation, and two- and three-dimensional scaling transformations (scaling, clipping, rotating, and translating). A user can replace display images instantaneously with no screen blanking between images—an ideal feature for animation. An option allows a user to switch quickly between graphics mode and 3270 mode for network and database access.

Model 5081 display can simultaneously show up to 256 shades of gray. A color model displays up to 256 colors from a 4096-color palette. The noninterlaced raster unit refreshes the 1024 x 1024 addressable points on the screen 50 times/s. This rate results in a steady, bright, and clear image. To help reduce distortion, the tube face is cylindrically shaped with contrast-improving, antiglare-treated glass. For operator comfort, the display tilts 5 degrees forward and 15 degrees backward.

Operating as a shared high speed control unit between host channel and 5085 and/or 3255 control units, the 5088 channel controller attaches to a System/370, 43XX, or 30XX channel. Speeds range up to 2.5 Mbytes/s in data streaming mode, and up to 1 Mbyte/s in conventional channel mode.

The primary device for system interaction is the 5083 tablet. With either its mouse-like cursor control device or a stylus, the tablet digitizes drawings or emulates the operation of a light pen. The thin, flat-surface unit weighs 6.5 lbs and features a palm rest and height adjustment.

The graphics access method/system product release 2 (GAM/SP2) supports current 3250 functions and a full range of advanced functions under VM/SP, MVS, and MVS/XA. Other software allows users to examine surfaces in detail, highlight changes in color, and display designs for structural analysis.

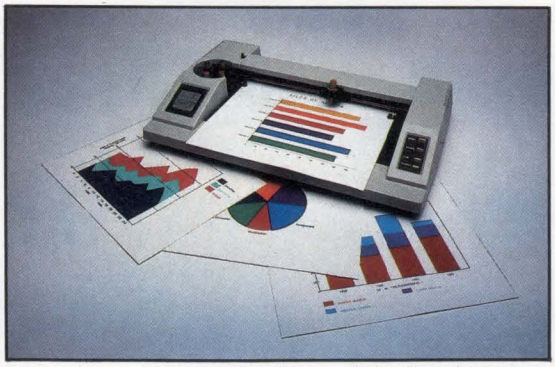
Peripherals include an alphanumeric keyboard, a lighted program function keyboard, a tablet with either stylus or cursor control device, and a dial unit. All devices attach to the processor through connections in the display's base. Purchase price for a 5081 monochrome display with four gray shades, keyboard, a 5083 tablet with stylus, and a 5085 processor is $19,750. With a color display and 16 colors, the price is $24,750. **IBM Corp, Information Systems Group,** 900 King St, Rye Brook, NY 10573. **Circle 261**

Low cost plotter combines graphics command set and offline operation

To meet the demand for multiple color, low cost graphics plotting, Enter Computer is producing a six-pen plotter at an end user price of $1095. The Sweet-P 600, or "Six-Shooter," stores six fiber-tip, Rapidograph-type, or ball-point pens in a rotating carousel to provide six colors online. Additionally, carousels can be switched to provide several palettes for writing on either paper or acetate.

The Sweet-P 600 takes either 8½- x 11-in. or 11- x 17-in. paper. The pen moves along a single axis, the X-axis, while the paper is moved back and forth on the Y-axis by gripping rollers. The smallest addressable increment is 0.004 in., and maximum plotting speed is 14 in./s. Repetition accuracy for any given pen is the minimum step size of 0.004 in., while repetition accuracy from pen to pen is two step sizes, or 0.008 in.

Among the techniques that have enabled this degree of accuracy at a low cost is the use of stepper motors controlled by a microprocessor using ROM-based microstepping routines. The 600 also contains 19 internal character sets, including katakana, and a Sweet-P graphics (SP/GL) command set. The command set includes line, curve, and point drawing; axis and tick drawing; and routines for drawing and filling rectangles and wedges.



The Sweet-P 600 is also compatible with the Hewlett-Packard graphics language (HPGL) so that software written for the HP 7400 series plotters can also run the 600. In fact, there already exists a considerably large body of software packages from over 25 independent software vendors to run the Six-Shooter on a variety of computer systems including Texas Instruments, IBM, Digital Equipment Corp, Wang, Apple, and a variety of MS-DOS and CP/M systems.

The Six-Shooter has both RS-232 serial and Centronics-compatible parallel interfaces and can be used in an "eavesdropping" mode for a multi-user environment. There, it is placed between microcomputer and printer or between terminal and mainframe, and performs tasks when specifically instructed to do so. This is made possible by the 2-Kbyte buffer supplied or by using the optional 8-Kbyte buffer to download tasks. Even in a single-user microcomputer environment, the plotter can operate without tying up the computer resources, except to receive additional downloaded tasks. **Enter Computer, Inc,** 6867 Nancy Ridge Dr, San Diego, CA 92121. **Circle 262**

Put powerful instrument control at your fingertips.

IEEE-488

The new Fluke 1722A Instrument Controller combines the computational ability and interfacing flexibility you need with the rugged packaging and easy-to-use human interface your factory demands. All at a new, low price. Now you can integrate your next factory test, process control or OEM system faster and put your people to work sooner.

The power of the 1722A is a 16-bit single-board computer with 136K bytes of main memory. Its 12 MHz speed puts it in the same class as many minicomputers. Four programming languages are available to simplify programming,including Interpreted and Compiled BASIC, FORTRAN and Assembly. Each includes special adaptations for controlling IEEE-488-compatible programmable instrumentation. And if you already own a 1720A Instrument Controller, you can run existing software on the 1722A—without modification.

The modular mainframe easily mounts in a standard 19 inch rack and allows you to configure the interfaces and memory to your exact needs. The IEEE-488 (1980) and RS-232-C interfaces can be expanded with an optional IEEE-488 and RS-232-C interface card, parallel interface card or dual serial interface card. Onboard memory is expandable to 2.6M bytes with RAM cards or 1.4M bytes with bubble memory.

The 1722A's touch-sensitive display dramatically simplifies system operation. Once programmed, your system can be operated entirely from the CRT. The 1722A displays only the pertinent options, allowing you to structure the user's response to a system. This helps reduce mistakes and increase throughput.

The 1722A is priced at $7450 (U.S. list), including BASIC Interpreter, documentation and a limited one-year factory warranty. So get in touch with your local Fluke Sales Engineer or Representative. Or call us toll free at **800-426-0361** for more information.

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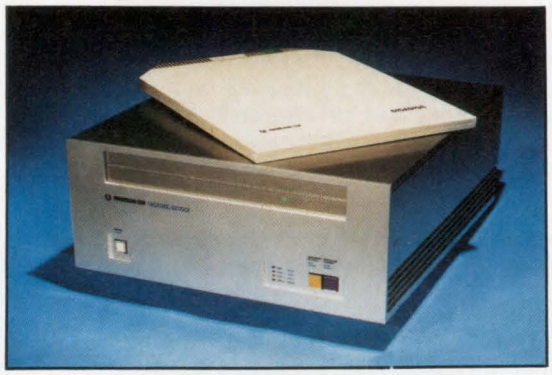
CIRCLE 116

Laser-based optical disk drive stores 1 billion bytes

Digital Gigadisc GD 1001 has features that set it apart from traditional recording technologies. Based on a solid state diode laser, the drive provides a 210-Mbit/in.^{2} (33-Mbit/cm^2) recording density and a 4.1-Mbit/s disk transfer rate. With three access methods—random, optimized random, and sequential—the drive allows direct access to any sector in the read or write mode and 3-ms access times within a band.

Because of its disk format, the read/write unit is easy to operate and highly reliable. The unit subassemblies include an optical unit, optical head, linear motor, rotation motor, and a set of logic boards. The optical unit consists of a semiconductor laser module and a photo detector, while the optical head is actuated for both radial and vertical positioning of the laser beam (fine access). The linear motor provides the coarse access by moving the optical head and focusing it on the target track area. The rotation motor, on its axis, includes a disk seating and clamping device. Finally, the logic boards control servomechanisms and disk accesses.



A 12-in. (305-mm) diameter cassette encased disk eases all handling, storage, loading, and unloading operations. Each disk is preformatted in tracks and sectors. A sector can be directly accessed by its logical address. A spiral track organization allows continuous writing and reading of information streams. Once recorded, a physiochemical process (plastic copies) can entirely replicate a disk in one step.

The powerful automatic error detection and correction feature guarantees effective disk capacity. In addition, it maintains records at the quality level required in data processing environments, even after numerous years in archival storage. Data-handling software is kept simple since each record is physically located at a programmer-defined address. This eliminates the need to check physical copies of the disk. The user is kept informed on the level of difficulty that the error correction process has met each time a record is read back. This lets the user check file integrity. The optical disk will sell in the range of $6000 to $9000; the media range from $200 to $300. **Thomson-CSF Communications,** 360 N Sepulveda Blvd, El Segundo, CA 90245. **Circle 263**

Open architecture characterizes programmable handheld computer

A versatile tool for technical professionals, the HP-71B is optimized for numeric computation and calculation. In contrast with earlier policy, Hewlett-Packard is providing extensive documentation on the unit's internal workings, and is actively seeking third-party vendors for software, hardware, and HP-IL products.

Based on a 4-bit processor, the computer accesses up to 1 Mbyte of virtual memory by bank-switching. It has an operating system, Basic, and a sophisticated calculator mode in 64 Kbytes of onboard CMOS ROM, as well as 16 Kbytes of CMOS RAM. At present, four slots below the front edge of the keyboard accept 16 Kbytes of RAM, 256 Kbytes of ROM, or any combination of the two. Only the size of available CMOS static chips limits plug-in memory.

At power-on, the operating system checks installed memory and configures it automatically. Thus, segmentation is transparent to the user's application program. Expanded ROM Basic includes enhancements for statistics, trig functions, and IEEE floating point math.

This spring, application ROM packages will be released for math, engineering, surveying, and text editing, as well as Forth and assembly language development systems. Software comes in ROM, cassette tapes, or magnetic cards.

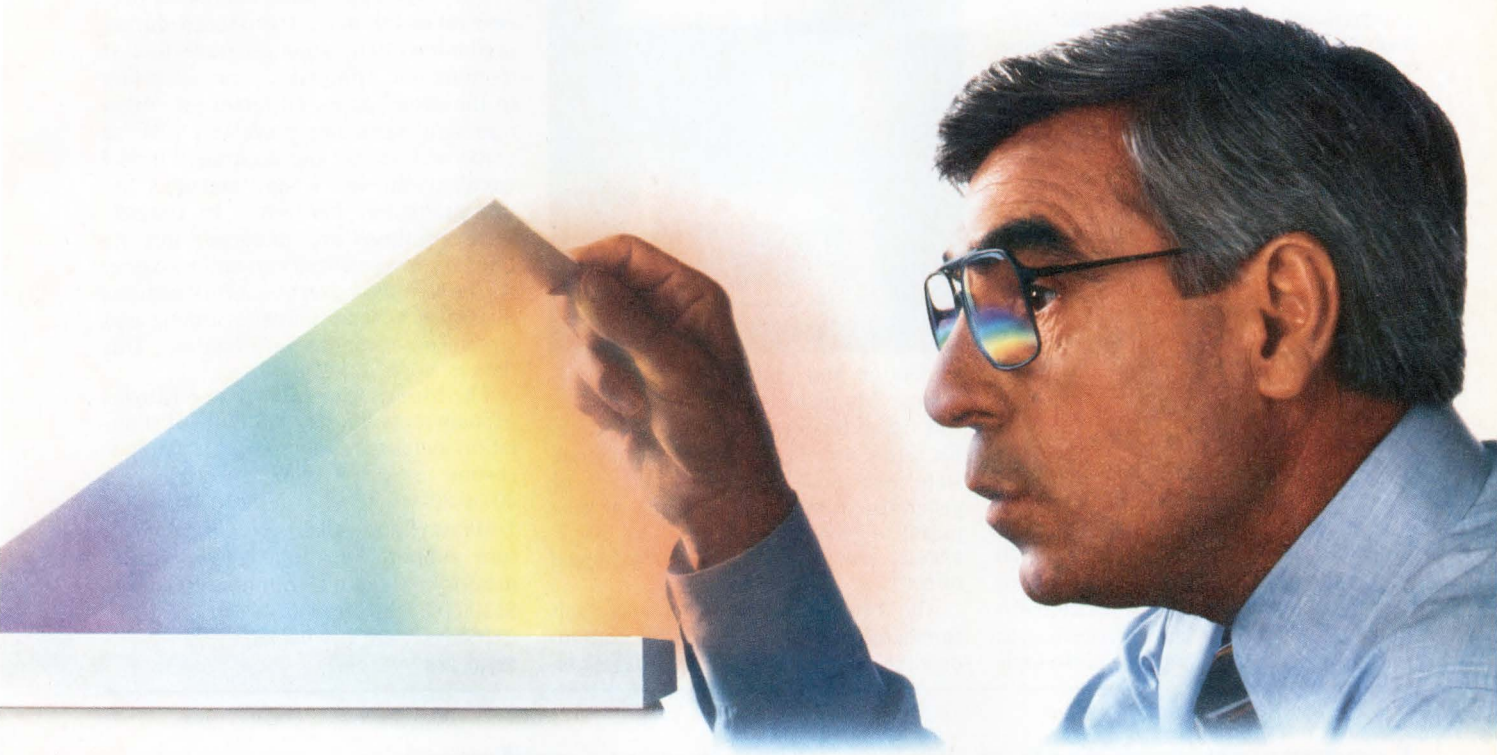
Interfaces for a magnetic card reader (photo upper right) and HP-IL connector (left) enable the unit to read and store programs. The reader plugs into the back of the unit, and the HP-IL connector inserts into a slot on the left. In addition, HP-IL controllers for the IEEE 488 bus, RS-232, and GPIO interfaces equip the unit to work with a broad range of peripherals.

The 8 x 132 dot-matrix LCD shows 22 out of 96 possible characters on the input line. This keyboard-controlled window scrolls horizontally as characters are entered. Alternately, an ASCII terminal can be the display device under control of a small Basic program.

Key definitions on the QWERTY-style keyboard are controlled by the gold "f" and blue "g" keys. Keyfiles, Basic extensions, simple display graphics, auto-start, and other programming aids facilitate custom features. The basic unit, with 16-Kbyte RAM and 64-Kbyte ROM, costs $550. **Hewlett-Packard Co,** 1000 NE Circle Blvd, Corvallis, OR 97730.

Circle 264

The Newest Innovation in Controller Technology From the Oldest Name in Multifunction Controllers.



Introducing the World's First LSI-11 Emulating Multifunction Disk/Tape Controller.

Say hello to SPECTRA 25, the cornerstone of our new family of high-performance disk/tape controllers designed for use with DEC's LSI-11 computer.

This revolutionary Q-Bus compatible single quad board lets you interface any combination of two SMD disks and four formatted ½-inch tape drives. By using extended commands to program the onboard E^2PROM, you can easily select drive mixing, mapping, and many other features–all without removing the controller from the system.

The SPECTRA 25 emulates DEC's RM02/5 and RM80 disk subsystems, and DEC's TSI1 tape subsystem. It also provides complete emulation for operation with DEC's RT-11, RSX-11M, RSX-11M-PLUS and RSTS/E operating systems.

To further enhance system performance, Spectra Logic offers SPECTRA STREAM™ software, a streaming tape backup utility that can back up an entire 80MB drive in only seven minutes.

Spectra Logic first introduced the multifunction concept back in 1979. And we've been quietly revolutionizing the market ever since with families of controllers that provide the high-performance, proven reliability, and added value you need to stay competitive.

We also offer the industry's most comprehensive one year warranty, responsive nationwide service, and ongoing technical support.

SPECTRA 25 is the latest innovation in controller technology from the company with peripheral vision. Spectra Logic. For further information, including complete technical specifications, call or write us today.

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SPECTRA LOGIC

CIRCLE 117

Compact station engineers hierarchical VLSI design system

A high end design station called the MegaLogician combines powerful mainframe simulation with the verification functions of a breadboard in one desktop package. Its Ethernet interface controls integrated network communication between workstations, file or print servers, and mainframes. By simulating up to one million gates and making 100,000 evaluations/s, the MegaLogician is said to improve performance 100 times and capacity 10 times over existing design stations. Future capacities of 10 million gates are projected.

Graphics capability and automatic feature extraction help build circuits from the ground up. Database structure and architecture, including Intel's 286 CPU and a proprietary microcoded TTL circuit emulator, permit fast switching between different circuit views at any level of complexity. Changes in viewpoint (eg, from gate to functional level) take place within 3 s.

Gate-level editing describes in detail and manipulates individual gates and interconnections. Timing information for gates built from different processes, as well as interconnect lines, feed into logic

simulation and timing verification programs. Multigate structures appear as functional blocks, and store as modules for future use. Text descriptions of finite state machines can be created or generated from flowcharts; PLA or ROM masks designed; and FPLAS, PALS, PROMS, and erasable PROMs programmed directly.

The behavioral level generates fault simulation and test programs for both individual circuits and for complete systems. Designers can model the effects of particular software programs or interrupt schemes and alter circuits as required.

The knowledge-based simulation process takes the net list produced during preliminary design and generates lists of "simulation primitives" corresponding to the circuit gates. Different primitives represent particular processes, such as CMOS and NMOS, and accurately model circuit parameters when "executed" by the simulation hardware. In essence, these primitives are microcode instructions for a specialized emulation engine. As the simulator executes its instructions in sequence, it accumulates timing and circuit performance information. This data is stored on disk.

The MegaLogician has 1 to 6 Mbytes of main memory, 4 to 8 Mbytes of simulation memory, a high resolution monochrome or color graphics terminal, a 40-or 80-Mbyte Winchester disk, and a 1-Mbyte floppy disk. System architecture supports up to 1-Gbyte virtual memory. Standard configuration costs $120,000. **Daisy Systems Corp,** 139 Kifer Ct, Sunnyvale, CA 94086.
Circle 265

Condensing architecture makes small system perform big

The Eclipse MV/8000C can address 4 Gbytes of virtual memory and is program compatible with other Eclipse MV/ family computers. Using bit-slice architecture and a pipelined instruction processor lets the system run at a 220-ns microcycle speed. The compact 10.5-in. high rackmountable system uses both 256-Kbyte dynamic RAMs and gate arrays for its compact power.

The instruction processor interprets instructions for execution. After receiving an instruction sequence, it keeps up to four in a pipeline at one time. This achieves one onsite instruction execution every microcycle. It simultaneously executes one instruction while it decodes a second and fetches a third. A 1-Kbyte instruction cache that is directly mapped to the system cache buffers the system. Transferring instructions from the instruction cache and data from the system cache to main memory occurs simultaneously for improved performance.

Both system cache and main memory reside on a single 15- x 15-in. board that uses 2000+ custom gate array circuitry. The 16-Kbyte system cache ports to both the CPU and I/O system. With a 150-ns cycle time, it functions as a lookahead and lookback buffer for the system. Transfers between system cache and main memory occur at a rate of 16 bytes in 550 ns for a write, and 16 bytes in 440 ns for a read.

When memory control receives an address from the system cache, the circuitry addresses specific memory locations and performs error checking and correction on data transfers between the bank controller and main memory. It also provides byte parity checking on data transfers from the system cache. Each main memory location is put through a check at a 2-s/Mbyte rate. At the same time, refresh operations are performed on the 64- or 256-Kbit DRAM-based memory array.

As a hardware accelerator for the demand paging subsystem, the address translation unit (ATU) eliminates processor overhead for page translations. It maintains a table of recently referenced page addresses, using the fact that during processing, memory references tend to cluster in page groups that are repeatedly referenced. The 265-page table is stored in the ATU cache. When a program requests a page, the hardware first checks for the page location in the ATU cache. This relieves the processor from having to regenerate the translation for every page reference.

Other system features include an eight-level hierarchical security system, the full MV series instruction set, and a three-level independent I/O subsystem. The 32-bit system is priced at $55,500 for one, and $40,515 each in quantities of 20. **Data General Corp,** 4400 Computer Dr, Westboro, MA 01580.
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Winchester/floppy controller rules over diverse disk selections

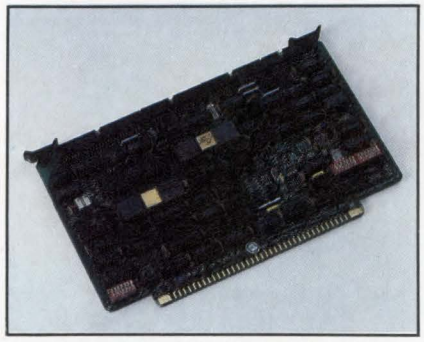
Occupying only 16 memory locations, the GMS6529 intelligent module can control three Winchesters and four floppies. Its five onboard processors cover functions ranging from communication to error correction. They perform specific functions at maximum speed with minimal operating software.

A master single-chip processor operates at a 10-MHz clock speed. It performs all communication between the system and control processors and sector buffer RAM. The second processor works with a custom data separator device to perform all read/write operations to the disk. Used to lock phase locked loops to the incoming clock, it also drives some 8-in. floppy signals.

The third processor controls the 5¼- and 8-in. floppies. The floppy controller contains a built-in data separator, write precompensation, and all seek functions. The fourth processor, as an error correction/detection unit, can automatically generate ECC or CRC on data stream. When it detects an error, it automatically corrects up to a 5-bit stream on a single data burst. A retry will also automatically start if the data cannot be corrected. In addition, this processor generates and verifies CRC/ECC on both data and ID files.

Finally, the fifth processor is an optional DMA device that transfers data to/from sector buffer RAM onboard to/from system RAM. It speeds the transfer rate by up to 10 times (when used in the halt burst mode) or 4 to 5 times (in halt steal mode). Another advantage is the decrease in user software needed to read/write to and from floppies or hard disks. A programmable counter generates a DMA grant signal that is normally generated by system processors. However, not all processors have this capability, so with the counter, the DMA option can be used with all four types of processors used in the single-board computer (6502, 6802, 6809, and Z80).

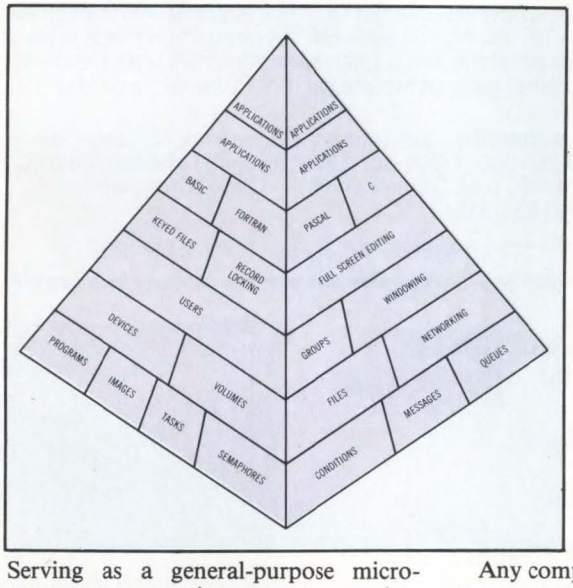
In addition to the five processors, a versatile interface adapter provides two ports for custom applications. The first port with eight I/O lines reads a DIP switch. The switch positions indicate to



the operating software the following parameters: file booting, drive size and density, and whether or not a removable hard disk is installed. The other port performs hard disk removable functions, such as the disk being removed, write protected, and cartridge changed. This port is also used to format hard sectors and to generate system interrupts.

The controller is burned in for 72 hours and carries a full-year warranty. It is priced at $387 in 100-piece quantities. **General Micro Systems, Inc,** 1320 Chaffey Ct, Ontario, CA 91762. **Circle 267**

Portable operating system easily adapts to specific microcomputers



Serving as a general-purpose microcomputer operating system, SI has several characteristics that distinguish it from other operating systems. Its machine independence and building block construction provide flexibility, while realtime facilities and machine language implementation deliver performance.

Taking user requests, a command processor causes appropriate programs to run. There are three types, all of which can reside in a single system. Switching between them occurs with a single command. The conventional processor accepts lines typed into the terminal, decodes the command into names and operands, loads the appropriate command program, and then gives it control.

The menu processor displays the command choices. The prompting processor is used like the conventional one. However, omitting required operands does not cause an error message to be printed and the command discarded. Instead, it prompts for each operand.

Any complete program can be used as a command. The system provides several commands, including assemble, back up, charge, clean, debug, and link. Other commands arise from word processors, spreadsheet programs, compilers, and interpreters.

A command list is a command sequence in a file. It is used like a command but is easier to compose. A file with commands executes directly. Ordinarily, each command will be invoked when the preceding one has finished. The command process provides a language for controlling command execution. Unlike conventional programming, changing a command list only involves its editing. No recompiling or relinking is needed.

System variables comprise the names and values that SI associates with the system information. They provide a way to alter the appearance and behavior of SI without rebuilding the system. The set command changes system variables, which the user can directly examine, set, and alter from a running program.

The system adapts to specific hardware on three levels. Moving SI from one architecture to another requires rewriting the code generation part of the compiler. To change system facilities, commands create a new system copy that includes or excludes particular features. To add a new device, the only requirement is a subroutine that acts as the device driver.

Currently available versions run on the 68000, Z80, 8080, 8085, and 8086/88, with versions planned for the 80186/286 and the 16032. Prices range from $200 to $1100. **Multi Solutions, Inc,** 660 Whitehead Rd, Lawrenceville, NJ 08648. **Circle 268**

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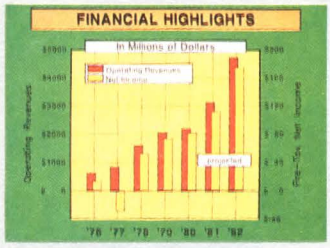

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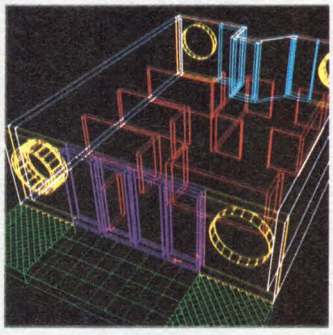

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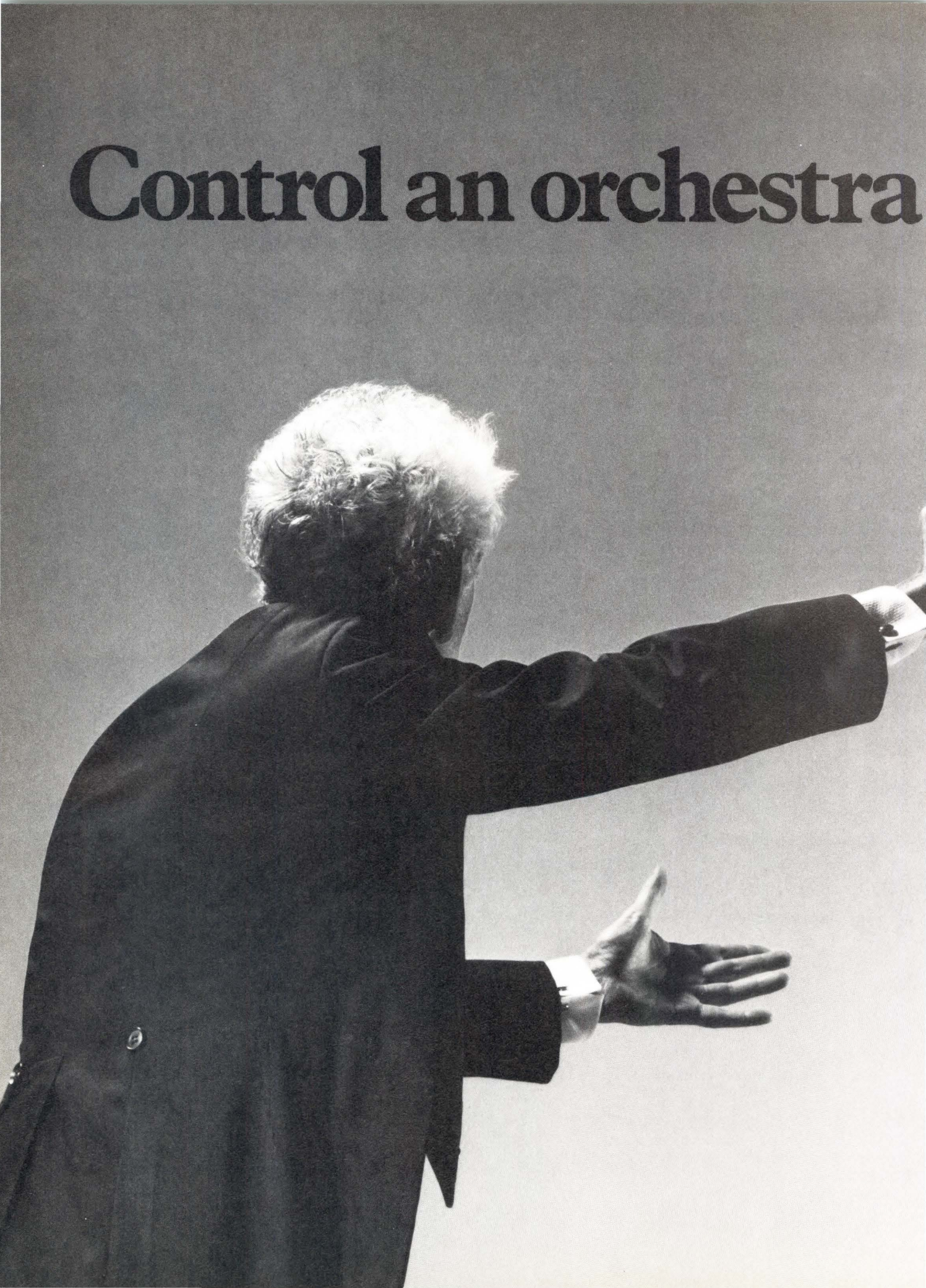
CIRCLE 119

Control an orchestra



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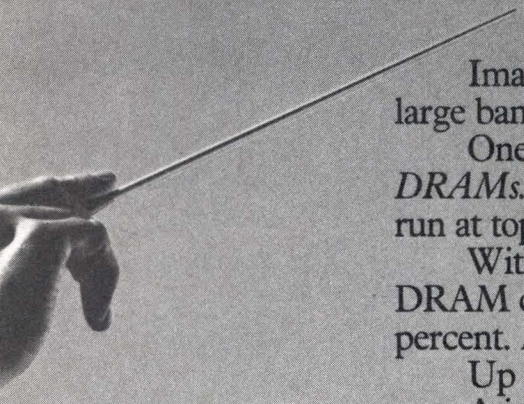

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CIRCLE 122

Converter for dumb terminals

Protocol converter allows access to IBM mainframes and provides a communication path for 12 async devices. The Micro7400 has all standard 3270 capabilities and, in addition, it offers the ability to switch between two IBM hosts or between an IBM host and a minicomputer. A command port allows alteration of parameters such as priority assignments, and provides monitoring, diagnostic, and control facilities. Five models are offered with prices beginning at $2250. **Micom Systems, Inc,** 20151 Nordhoff St, Chatsworth, CA 91311.
Circle 269

Communication processor

Designed to serve as a hardware engine for a range of standard communication protocols, the ICP is an intelligent processor that handles 2780/3780 and X.25 protocols. Peripheral I/O and other communication-related functions are offloaded to raise throughput. As a terminal controller it uses ITH software to reduce the number of interrupts sent to the CPU. Interfacing to serial terminals at rates to 9600 baud, the software buffers the main processor by assembling character blocks in local memory. The unit costs $3950. **Zilog, Inc,** 1315 Dell Ave, Campbell, CA 95008.
Circle 270

Protocol converters

Enabling ASCII terminals to communicate with IBM hosts, the series 100 emphasizes the price/performance factor. To IBM hosts, the devices are indistinguishable from IBM peripheral controllers. Terminals and printers supported by the series 100 appear to the host as IBM peripherals. Model 176 supports seven personal computers. Model 167 allows 3767 users to substitute low cost ASCII terminals and other peripherals for IBM SNA/SDLC devices. Pricing for the series starts at $2850. **Protocol Computers, Inc,** 6150 Canoga Ave, Woodland Hills, CA 91367.
Circle 271

Frontend processor

The 6100 communication subsystem allows Nonstop II and TXP systems to manage several hundred communication lines simultaneously. Data rates are up to 56,000 bits/s. Three transmission types (asynchronous, byte synchronous, and bit synchronous) and two line disciplines (point-to-point and multipoint supervisor) are available. It is microprogrammable on a per-line basis allowing different protocols, line disciplines, and line speeds to be mixed in a single system. Price is $23,900. **Tandem Computers, Inc,** 19333 Vallco Pkwy, Cupertino, CA 95014.
Circle 272

Packet-switched network

The Sopho-Net network allows previously incompatible equipment to communicate freely, while it remains transparent. Node throughput rates are in excess of 1500 packets/s, node transit times are less than 20 ms, up to 4000 lines can connect to a node, and any number of nodes can make up a single network. The system carries all types of traffic: data, text, and image, and can superimpose any on the other. Systems are connected to the network in their native protocol so no hardware or software modifications are necessary. **Phillips Telecommunications Industries,** PO Box 32, 1200 JD Hilversum, The Netherlands.
Circle 273

Two-unit processors

Improved design equips Comten 3650 communication processors to terminate up to three times the number of SDLC communication lines at the processor. The frontend and remote units support two hosts without an expansion cabinet. In addition, two improved price/performance models (R8 and S8) manage up to 16 communication lines, 512 Kbytes of memory, and two hosts. Several configurations are available. **NCR Comten, Inc,** 2700 Snelling Ave N, St Paul, MN 55113.
Circle 274

March Preview
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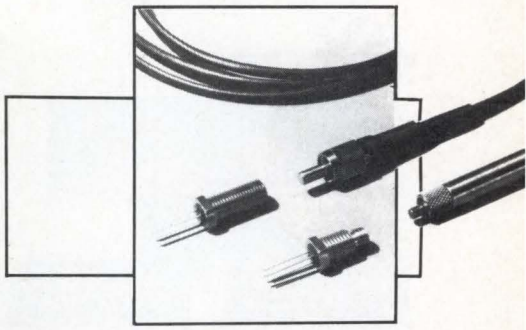
Fiber optic transmitter



Capable of speeds up to 100 Mbaud, the HFBR-1203/1204 operates at distances in excess of 1 km. The high optical power—7.4 dBm when coupled into 100/140-μm fiber—allows for applications in LANs and high speed computer links. Optical coupling scheme keeps optical power variation within 5 dB. An etched-well, 820-nm emitter provides thermal conduction for the high optical power. In quantities of 100, the transmitters are $66 each. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 275

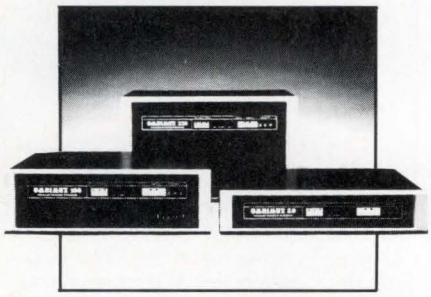
Virtual circuit switch

The Datakit VCS is a kit of compatible hardware modules assembled to provide a highly efficient network of terminal-to-computer and computer-to-computer communication. Architecture is designed to handle different protocols simultaneously. With the hardware, communication hubs link to LANs, and each link provides high speed transmission with low delay. The network uses a star topology with host computers at the center. **AT&T Western Electric,** 222 Broadway, New York, NY 10038.
Circle 276

Digital line interface module

The MH89700 thick-film hybrid module provides 256 kbits/s of full-duplex communication between digital terminations over two common twisted-pair telephone cables. It shares the 2.048-Mbit/s, 32-channel, 8-bit/channel serial transmission format designed for PCM encoded voice and digital data. The module uses any four 64-kbit/s channels from a ST-BUS interface at the network port. In addition, it provides a line port and a microprocessor port. Switching is with asynchronous or synchronous data between any of the three ports. In a 40-pin DIP, price is $96.25 in 100s. **Mitel Semiconductor,** PO Box 1663, Buffalo, NY 14203.
Circle 277

Integrated modems



The 2400-, 4800-, and 9600-bit/s modems offer reliability with LSI circuit design, compatibility with Omnimux MUXes, and backward compatibility with modems. Switches mounted on the front change operating parameters. Loopback test functions speed system fault isolation. The 2400-bit/s modem is compatible with the 24-LSI Mark II modem and meets CCITT V.27 bis recommendations. Pricing begins at $700. **Racal-Milgo,** 8600 NW 41st St, Miami, FL 33166.
Circle 278

Distributed processing LAN

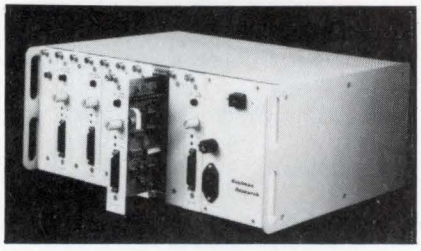
A LAN software system offers compatibility with both Unix and mixed MS-DOS/ Unix environments. Designed to run on IBM PCs, it allows sharing of all devices and unrestricted files on a system. The software will turn each node into a window on the entire network and on connected networks through gateways. Software can be stored in a few centralized places and downloaded to any computer on demand. An unlimited license costs $250,000; 500-node costs $50,000, with basic licenses at $10,000, plus $200 a node. **Phoenix Software Assocs Ltd,** PO Box 207, N Easton, MA 02356.
Circle 279

Networking extras

Additions to DECnet include an interface to connect all Q-bus micros, three Ethernet servers, remote fiber optic repeater, and supporting software packages. The Deqna uses the H4000 transceiver and cabling to connect the computer to Ethernet coaxial cable. It operates at a 10-Mbit/s rate and provides both physical channel and data-link functions conforming to the latest specs. Price is $1150. Communication servers link Ethernet to other networks. Prices range from $17,000 to $26,995. Repeater enables designers to configure large Ethernet configurations up to 1000 m through a fiber optic link. Cost is $4400. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
Circle 280

Protocol conversion

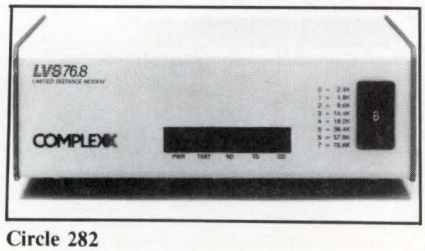
Model 870 converts binary sync protocols into async, emulating the IBM 3270 cluster controller. The modular converter supports devices from one to eight channels each with its own microprocessor. The micro offers faster async conversion and the capability to support 256 terminals per host port. A rotary switch selects the data transmission rate, which ranges from 110 to 19,200 bits/in. An autobaud rate detect feature determines the correct baud rate for each terminal. CRT controls are individually remapped for each terminal line, allowing full emulation. Cost of a basic system is $3395. **Kaufman Research Manufacturing, Inc,** 145 E Dana St, Mountain View, CA 94041.



Circle 281

Limited-distance modem

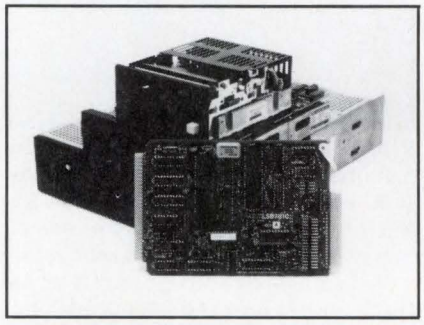
The LVS 76.8 allows thumbwheel-switch selection of eight sync speeds from 2400 to 76,800 bits/s. It operates at other speeds via an outside clock. At maximum speed, it can send data 5000 m on a typical 22-gauge wire. Either EIA RS-232-C or V.35 interface is available. The modem is programmed to provide standard EIA and line loopback testing from either end of the line. Prices range from $650 to $725. **Complexx Systems, Inc,** 4930 Research Dr, Huntsville, AL 35805.



Circle 282

INTERFACE

Floppy disk controller



As a single-board STD bus device, the LSB-7810 simultaneously controls up to four disk drives in any size and format combination. An optional DMA controller frees up the host during disk transfer and provides full vectored interrupt capability. Interrupts are jump selectable. All drive parameters and sector lengths are software programmable for each drive. Quantity-one price is $280, plus $35 for the DMA controller. **Axis, Inc,** 7825 Engineer Rd, San Diego, CA 92111.
Circle 283

Multibus floppy controller

The V8004 supports both 5¼- and 8-in. disk drives, providing oncard data separation and double-density write data precompensation. Proper clocks are under software control for the disk being used. There are no oncard adjustments. Disk cable terminations mount in sockets for easy replacement. Fabricated with multilayer printed circuits, the card is a single-wide iSBX module 100 percent compatible with iSBX specs. Unit costs $450. **Century Computer Corp,** 14453 Gillis Rd, Dallas, TX 75234.
Circle 284

Intelligent controllers

The series 6000 attaches ESDI/ESTI disk and tape drives to a variety of host systems. The host computer bus is the SASI bidirectional bus interface. Both kinds of drives attach to the bus without sacrificing performance characteristics. Controller chip set features consecutive sector transfers, 2-Mbyte host data transfer rates, and intelligent buffer management. In 1000s, prices range from $225 to $350. **OMTI,** 557 Salmar Ave, Campbell, CA 95008.
Circle 285

"BUBBLES ARE HELPING NIXDORF BREAK INTO NEW SALES FIGURES."

—Axel Hass
Sales Director of Retail Industry
Nixdorf Computer AG

Computer product codes. Each as unique as a fingerprint. Each representing a product and its cost. Designed to eliminate the time and expense of price tags and stickers, while providing critical up-to-the-second inventory updates.

In order to make efficient use of this system, a retailer must have fast and reliable access to thousands of codes, anytime. Unfortunately, a modular, computerized access has never been provided.

Until now, that is.

Nixdorf Computer has introduced an affordable system that is both easy to use and to install. A system that doesn't discount quality, performance or reliability. A system made possible with a purchase from Intel.

Rather than counting on more RAM for keeping the data base, Nixdorf depends on an Intel 7110 bubble featuring a full megabit of non-volatile memory. Capable of storing thousands of codes for any store.

The solid state bubble also outperforms disks and floppies in this demanding environment. Which means Nixdorf's memory system runs maintenance-free 24-hours a day. So the downtime that means "no sale" is prevented. And the bubble's high speed access even helps keep check-out lines moving.

The 7110's small size also helps make Nixdorf's stand-alone system self-contained and modular. So the system fits smoothly into any size retail organization, can be easily networked, and can grow as the store's customer base grows.

Even if its customer base grows as fast as Nixdorf's.

Whatever your line in electronics, Intel bubbles just may be the break you've needed.

So write us for more information. Lit. Dept. Y7, 3065 Bowers Avenue, Santa Clara, CA 95051.

Or call us, toll-free. (800) 538-1876. In California, (800) 672-1833.

Then, perhaps, celebrate your new sales figures with a French bubble product. Its computer code is shown above.

Dom Perignon, 1975.

intel® delivers solutions

Disk SMD controller for Unibus

The MDB-RM11-Q (quad-size) emulates DEC's RM02/03/05, while the MDB-RK11-Q emulates RK06/07 disk drives. Each controller interfaces two physical disk drives (up to four logical units) to the PDP-11 Unibus. Either controller can simultaneously mix emulation modes within the same family. They are software transparent to all DEC operating systems plus Unix and TSX, and handle up to 56 Mbytes or 512 Mbytes per formatted device. Data capacity is 1.023 Gbytes with transfer rates to 10 Mbits/s. Prices range from $2800 to $3200. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.
Circle 286

Drivers for LED display

The M5450 and M5451 drive 34 and 35 segments, respectively, with sink currents to 5 mA. They operate four- or five-digit alphanumeric displays with minimal interface to the display and data source. A serial data and clock signal transfer data. Both drivers feature continuous brightness control and TTL compatibility. No external resistors are required. The 40-pin plastic DIP costs $4.20 each in 100s. **SGS Semiconductor Corp,** 1000 E Bell Rd, Phoenix, AZ 85022.
Circle 287

Mag-tape peripheral processor

Supporting the PDP-11 series of computers, model TC-200 is a single-board processor that takes one SPC slot in the backplane. It contains the necessary logic to control four 9-track tape drives. Speeds range from 25 to 125 in./s. Firmware provides an auto self-test verification routine on power up. The routine tests all internal registers, flags, and data paths. Read-after-write logic verifies data. The processor supports all DEC operating systems. Price is $3000 with delivery in 30 days. **Computer Storage Technology, Inc,** 1369 S State College Blvd, Anaheim, CA 92806.
Circle 288

Floppy controller board

Providing the required governing, formatting, and interfacing logic between the VMEbus and disk drives, the DSSEFDCONT-1 can handle four single- or double-sided 5¼- or 8-in. drives. The board occupies 24 Kbytes of memory, and base address is jumper selectable anywhere in the entire memory map. A hex display shows disk status and disk test results. The address bus and the control bus have TTL-compatible buffered inputs while the data bus has three-state, TTL-compatible buffered I/Os. Unit price is $1375. **Data-Sud Systems/U.S., Inc,** 2219 S 48th St, Tempe, AZ 85282.
Circle 289

Serial I/O for Multibus systems

This board allows up to eight EIA RS-232 interfaces to connect to any Multibus system. With a 45-ns access time, the MP8518 is controlled by a USART containing an onchip baud rate generator. Therefore, each USART can be set at a different speed. Baud rates range from 50 to 19,200. It requires 32 I/O ports and its base address can be on any 32-port boundary. Standard I/O addressing uses a 16-bit DIP switch. Interrupt combinations can be set by strap selection. In one to nine quantities, price is $465. **Burr-Brown, Data Acquisition and Control Systems Div,** 3631 E 44th St, Tucson, AZ 85713.
Circle 290

Disk controller slave

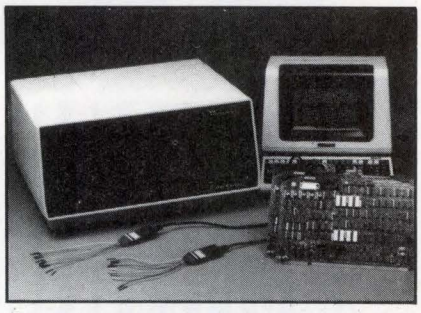
The Octafloppy is an IEEE 696/S-100 compatible slave card that provides up to 9.6 Mbytes of online storage via two strings of four drives. Each string can be either 5¼ or 8 in., single or double sided and single or double density simultaneously. It appears to the host as 16 I/O ports with optional extended device addressing. Up to a 64-Kbyte transfer can be performed anywhere on the 16-Mbyte address space. An onboard wait state generator allows it to be used in 8-MHz systems. Single-quantity price is $495. **Ackerman Digital Systems, Inc,** 216 W Stone Ct, Villa Park, IL 60181.
Circle 291

Winchester disk controller

Designed to maximize the I/O performance of multi-user, multitasking micro systems, the ACB-5500 board allows users to concurrently perform read or write operations on different disk drives. It supports seven host CPUs through a SASI/ANSI SCSI bus and four 5¼-in. Winchester drives of any capacity. The controller supports file sharing and shared disk applications through a reserve/release command. This command prevents access to a set of sectors that are being updated. Price is approximately $300. **Adaptec, Inc,** 580 Cotton Wood Dr, Milpitas, CA 95035.
Circle 292

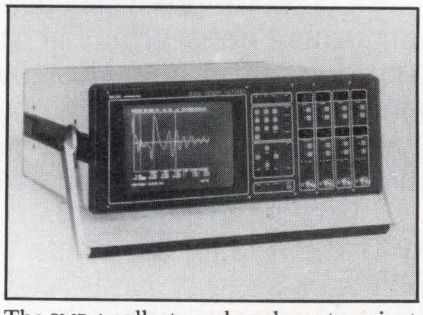
TEST & MEASUREMENT

Integrated timing analysis



An ITA component for the 9516/16S microsystem integration system adds high speed logic timing measurement and display. It offers async timing to 100 MHz and detects glitches as fast as 5 ns. An ITA consists of PC board and eight-channel probe pod. Users can capture up to 1024 samples/channel and display results in a waveform format on the screen. The ITA option will be available in the first quarter of 1984. Prices will be $4000 for the eight-channel version and $7000 for the 16-channel version. **Gould Inc, Design & Test Systems Div,** 4600 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 293

Signal memory recorder



The SMR-1 collects and analyzes transient waveforms. The modular unit provides each of 2 to 16 channels with 16 to 64 Kbytes of nonmultiplexed memory. Sampling is done at 1, 2, or 10 MHz with resolutions of 8, 10, or 12 bits. The 9-in. monitor displays in either Y-t or X-Y format. All functions and parameters are programmable by IEEE 488 or RS-232 interfaces or by front-panel selection. A dual-time base allows pretrigger information to be sampled at one rate with other triggered data to be sampled at another. **Soltec Corp,** 11684 Pendleton St, Sun Valley, CA 91352.
Circle 294

Memory and logic programmer

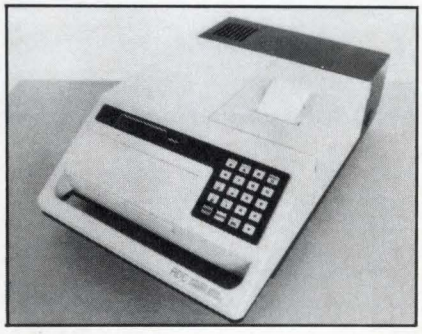
The 160 series universal programmer uses software (instead of hardware) that runs on a small computer. The complete system includes a programming station with two zero-insertion force sockets: one for devices of up to 28 pins, and one for 40-pin ICs. Software contains all the necessary programming algorithms and device data bases on floppy disks. Hardware includes an interface card that plugs into the computer, and a programming console containing power supplies and D-A converters that supply proper signals to the programming socket. Prices start at $4495. **Valley Data Sciences Inc,** 2426 Charleston Rd, Mountain View, CA 94043. **Circle 295**

Logic analysis system

The NPC-864ST combines a 48-channel state analyzer and a 16-channel 200-MHz timing analyzer into one package. It also includes a dual double-density floppy drive for test storage, automation, postprocessing, and performance monitoring using CP/M. Performance monitoring includes both time and event histograms with the time histogram used to display the percent of time the software takes to execute specific segments of code. Event histograms give the user frequency of occurrence information. Prices range to $19,500. **Nicolet Paratronics,** 201 Fourier Ave, Fremont, CA 94539. **Circle 296**

Portable floppy tester

Model PT-350 offers overlapping tests for data integrity and read-window margins. While a phase-locked loop generates a programmable data window, a programmable one-shot measures the relationship between read-data pulses and reference clocks. The tester has over 30 test routines and downloads to RAM for custom designed tests. It accommodates 8-in., 5¼-in., and 3½-in. disk drives, FM or MFM encoded. Firmware holds 32 Kbytes of data integrity tests. In unit quantities, it is priced at $2995 complete. **Applied Data Communications, Inc,** 14272 Chambers Rd, Tustin, CA 92680.



Circle 297

Test-generation system

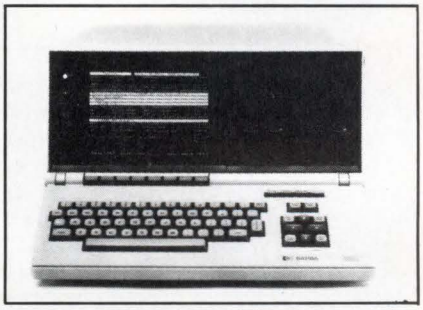
Using a hierarchical approach that accepts functional and structural circuit descriptions, Hitest improves test program efficiency. The knowledge-based software uses a data base to automatically generate appropriate test programs. The package runs on VAX 32-bit virtual memory computers in combination with a color graphics test generation terminal. An interactive simulator provides accurate MOS simulation and logic strengths. Circuits designed on the HILO-2 simulator or on general-purpose computers (Apollo, VAX, Prime, or IBM) can be fed to the Hitest system. A typical system costs $200,000. **GenRad, Inc,** 170 Tracer Lane, Waltham, MA 02254.

Circle 298

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Logic state/software analyzer



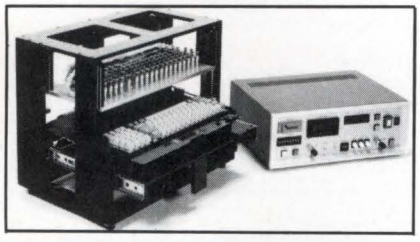
As an integrated modular system, the 64000 supports every phase of microbased product development. All functions operate from a development station that features syntax-driven softkeys. Assemblers, linkers, and C and Pascal compilers support software development. A software performance analyzer offers a measurement set to guide programmers in optimizing and streamlining subroutines or total system flow. State traces can be started with simple conditions or with complex series of events in a specific order. Depending on the number of input channels selected, prices range from $4350 to $9610. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 299**

Data-bus exerciser

Portable BUS-68000 exercises, tests, and troubleshoots MIL-STD-1553 systems. Local programming is via a front-panel, 24-pad keyboard and 10-character alphanumeric display. Remote programming is with an 8-bit parallel I/O port or optional IEEE 488 and RS-232 interfaces. Additional features include error generation and error detection, single or continuous messages, variable response time, and built-in self-test. The unit costs $4995 in quantities of one to nine. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

Circle 300

Tester for keyboards



The KRC-2000 system consists of two units, a programmable system control module, and a keyboard actuating module. Together they provide a programmable automated testing device that performs both life and functional tests for virtually any keyboard assembly. Capacity is 128 keys at 10 keys/s. The keyboard operates by input signals from external memory, or built-in ROM data inside the control unit. Printer interface is Centronics parallel. **Osawa & Co,** 1 Mamiya Ct, Kensington Ctr, Mt Prospect, IL 60056. **Circle 301**

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Scope calibration system

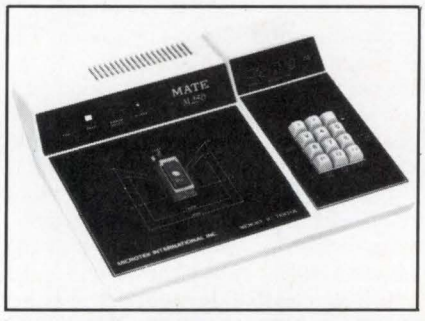
Calibrating scopes with bandwidths up to 1 GHz, the 4003A makes fast controlled checks by a software/hardware combination. This consists of a Computest software package, IBM PC, color display, dual disk drives, and printer. Color options provide 16 foreground and 8 background choices. The system is priced at $28,500. **Ballantine Laboratories, Inc,** 90 Fanny Rd, Boonton, NJ 07005. **Circle 302**

Universal field tester

Through a DSA bus, the 2610 provides high speed data transfers essential to complex microprocessor-based devices. Available modules include diagnostic control, micro interface, measurement, and protocol floppy tests. Based on a Z80A micro, hardware consists of a 5-in. CRT, 256 Kbytes of memory, an 89-key tactile keyboard and a 3½-in. disk drive. Prices start under $7000. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.

Circle 303

Static RAM EPROM tester



Mate M256 benchtop unit evaluates, tests, and measures access times of 16- to 256-Kbyte EPROMs or EEPROMs, and 16- to 64-Kbyte static RAMs. The tester indicates pass or fail for access times between 50 and 770 ns. Desired access time is keyed into the actual time registers on a digital display. Supply voltage can be 5.5, 5.25, 5, 4.75, or 4.5 V. An RS-232-C port allows memory up/downloading form the host CPU. **MicroTek Lab, Inc,** 17221 S Western Ave, Gardena, CA 90247.

Circle 304

MEMORY SYSTEMS

Winchester disk system

A 51-Mbyte universal mass storage system is compatible with Corvus host adapters available for IBM, TI, and Apple. The system uses run-length limited coding and a proprietary controller design for up to 60 percent more usable storage. In addition, transfer rates increase from 5 to 7.5 Mbits/s. Up to 64 users can share a single unit. A removable backup ¼-in. tape cartridge with 32 Mbytes of online storage comes separately. The system costs $4595 and the backup is $1295. **Sunol Systems,** PO Box 1777, 1027 Serpentine Lane Pleasanton, CA 94566. **Circle 305**

High speed Multibus memory

The MM-7000D memory board features an 200-ns access time and a 325-ns cycle time. Compatible with 68000, 8086, and Z8000 micros, the unit uses either 256- or 64-Kbyte RAMs in five capacities. Odd parity generation and checking are available with parity output stored in onboard error status register. An onboard option allows auto-switch to external backup batteries at power failure. Adjustable XACK/delays optimize system performance. A 512-Kbyte unit costs $995. **Micro Memory, Inc,** 9436 Irondale Ave, Chatsworth, CA 91311.

Circle 306

Memory board with 64 Kbytes

The CMOS memory module has battery backup and a write protect feature. The DCM 64 accepts eight 8-Kbyte 6264s or 2-Kbyte 6116s, or eight 8-, 4-, or 2-Kbyte PROMs or EPROMs. The write protect functions to convert RAM into ROM. For example, during software development, a program can be written, executed, and debugged in RAM, then protected in ROM. An onboard NiCad rechargeable battery makes the module portable. In single piece, fully populated with eight 6264 RAMs, the board costs $850. **Dynatem Inc,** 22600-D Lambert St, El Toro, CA 92630. **Circle 307**

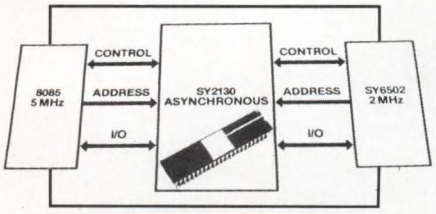
Universal floppy reader

Model TM-500 is a media translation system that accepts source computer data from floppy disks of any size, density, and format. It transfers data to an internal buffer memory where overhead formatting data is stripped away. Next, data is reformatted and written back out. In addition to disks, it unifies data formats for I/O ports and magnetic tape. A standard X-on/X-off feature enables the translator to accept realtime data communication input. IBM's Bisync protocol is optional. The system costs $15,800. **Applied Data Communications, Inc,** 14272 Chambers Rd, Tustin, CA 92680. **Circle 308**

Magnetic tape systems

Designed for the Mostek/Prolog STD bus line of single-card computers, the systems are 1/2-in., 9-track and perform at 800/1600 bits/in. They use an intelligent micro-based controller that provides an 8-bit bidirectional parallel interface. Asynchronous handshaking and ping-pong buffering (2 Kbytes/dual) are standard features for maximum throughput. STD bus users are provided with data interchange and transportation via IBM/ANSI/ECMA and ISO-compatible tape and over 40 Mbytes of unformatted data storage for archival and/or disk backup. Prices range from $9575 to $11,950. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.
Circle 309

Dual-port static RAM



Organized as 1024 x 8, the SY2130 allows asynchronous reading and writing to a common-memory array. It features two separate I/O ports that give independent access to any location in memory. Two contention modes are available: in one, the contention is ignored and both operations proceed; in the other, onchip control logic arbitrates. An interrupt function communicates between systems and acts as a writable flag. The chip has a 100-ns access time and operates off a 5-V supply. In 100-piece quantities, the price is $42 for 48-pin ceramic DIPs. **Synertek Inc, sub of Honeywell,** 3001 Stender Way, Santa Clara, CA 95054.
Circle 310

PERIPHERALS

Infrared touch input system

Designed for the ISC 8000 series of 19-in. color graphics terminals, the touch system uses LED emitters and phototransistor detectors. They create a lattice of infrared light beams just in front of the display surface. When the screen is touched, light beams are broken and the computer responds to the reported X-Y coordinates of the touch. There is no overlay between the viewer and the screen, so screen brightness and resolution are unaffected. **Carroll Touch Technology,** 2902 Farber Dr, Champaign, IL 61821. **Circle 311**

Laser printing subsystem

Using laser technology and electrophotography, the 6100 prints forms, data, and text at speeds up to 103 pages/min. It allows the user to change font sizes and character densities within a single line. A large page buffer holds one or more pages of information, and allows incoming data to be printed continuously. Densities of 6, 8, 10, and 12 lines/in. and 10, 12, and 15 chars/in. are user options. Print resolution is made up of 240 x 240 dots/in. The printer is priced at $195,000. **Storage Technology Corp,** 2270 S 88th St, Louisville, CO 80028. **Circle 312**

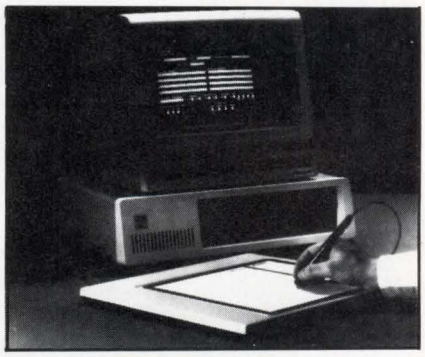
Battery-operated matrix printer

The TTX 1280 portaprint uses rechargeable or replaceable 6-V batteries that provide 4000 to 5000 lines of print. In battery mode, the bidirectional printer features a 40-char/s print speed. With ac power, speed increases to 80 chars/s. A 5- x 7-matrix printhead produces a variety of character sizes and densities. The 3-lb unit allows bold or shadow printing, oversided printing, and condensed printing. Price is $199. **Teletex Communication Corp,** 3420 E Third Ave, Foster City, CA 94404.
Circle 313

Mini magnetic card readers

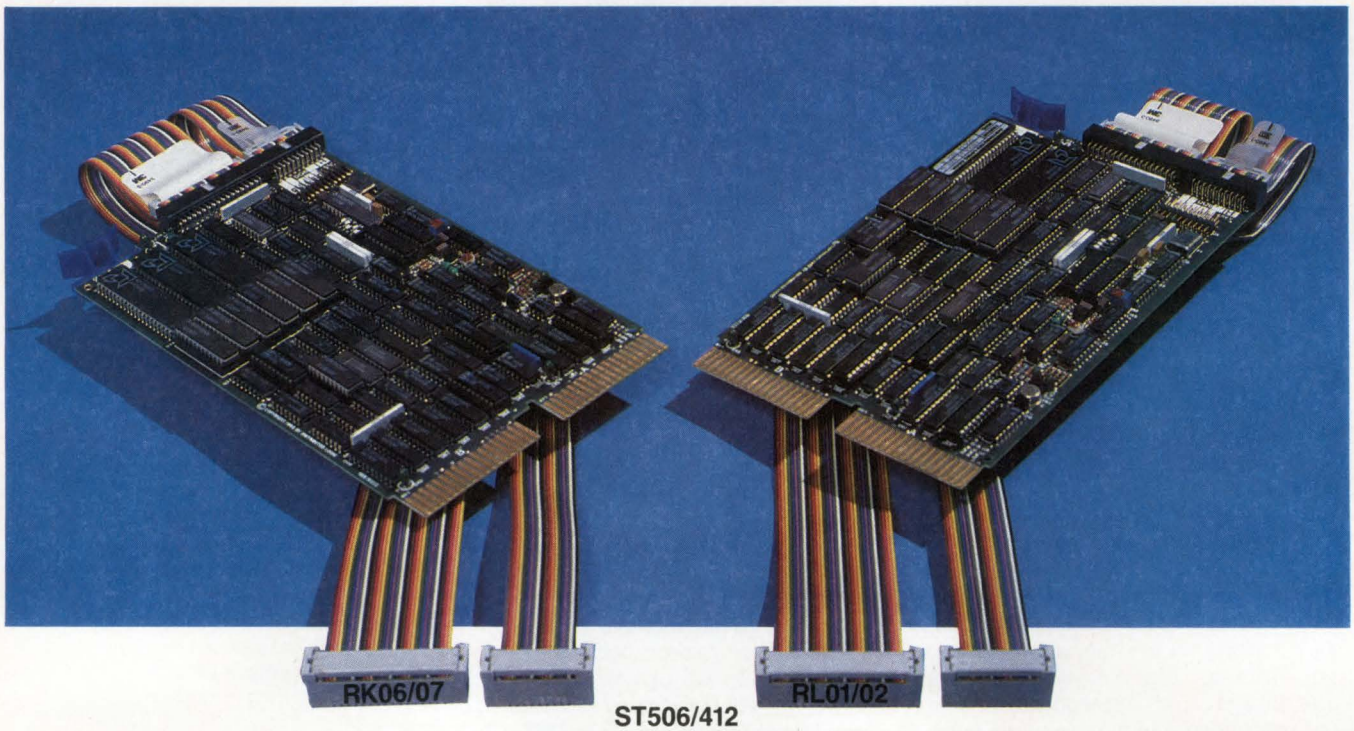
Model 801 reads previously recorded data from cards that have magnetic stripes and meet current ATA, ABA, or Thrift specs. They can also read data from other cards with F/2F data properly placed on a magnetic track. The reader uses single- or dual-track read heads and a read only electronics package. They have no moving parts and can be mounted horizontally or vertically. Output is fully decoded into two lines representing serial data and clock using a proprietary LSI circuit. **Vertel Div, Vertex Industries, Inc,** 23 Carol St, PO Box 1123, Clifton, NJ 07014. **Circle 314**

Handwriting terminal



The Penpad consists of a writing tablet, control unit, pen, and display monitor. A menu-driven setup mode allows the setup of power-up terminal parameters. Once selected, parameters are stored in nonvolatile memory. Control unit handles serial asynchronous, TTY-compatible, ANSI X3.64 standard communications and offers line-buffered, page-buffered, character/coordinate, and graphics input modes. The system features dynamic character recognition that reads handwritten information. **Pencept, Inc,** 39 Green St, Waltham, MA 02154.
Circle 315

The Only Way You Can Get Q-BUS* Compatibility And Interface Flexibility With ANY or ALL These 5¼" Winchester Drives is With These Two Controllers



ST506/412

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ATHENAEUM	*MAXTOR*	*NEC*	*SYQUEST*
CDC	*MEMOREX*	*NISSEI SANGYO*	*TANDON*
CMI	*MICROPOLIS*	*PRIAM*	*TOKYO ELECTRIC*
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CIRCLE 170

Low cost 68000 board

This 16-bit micro runs at 10 MHz and contains 17 internal 32-bit registers and a 24-bit program counter. Onboard memory consists of EPROMs and static RAMs, allowing the memory to run at full speed without wait states. Interfaces are a 24-line parallel and an RS-232-C. The system features a monitor in EPROM providing debug facilities, single step/trace, downline loader, and an EPROM programmer handler. A complete development system consisting of Z80 host, cross assembler, 68000 CPU board, and EPROM programmer sells for about $1500. **Apollo Software,** Bucklebury Alley, Cold Ash, Newbury, Berks, England.
Circle 316

PC-compatible CPU board

Capable of supporting a no-disk, ROM-based system, the CP-88 features BIOS with MS-DOS-compatible calling conventions. It can be combined with a memory board, video board, and floppy disk driver to operate as a hardware/software PC workalike. For applications requiring high speed complex math processing, an enhanced numeric processing extension is available. It can also serve as a remote control box at the end of a host computer in process control applications. Cost is $476. **Electro Design Inc,** 690 Rancheros Dr, San Marcos, CA 92069.
Circle 317

Hybrid processor

An S-100 board with both Z80 and NS16032 chips, the 16KZ runs CP/M. Software tools permit individual Z80 subroutines to be replaced with NS16032 code using switch processor macro calls to transfer from one MPU to another. Hardware floating point and memory management units are options, operating at a 10-MHz clock rate. The floating point unit implements high speed 64- and 32-bit floating point arithmetic, while the MMU implements program protection and debugging. **Innervision Computers,** 1632 Roll St, Santa Clara, CA 95050.
Circle 318

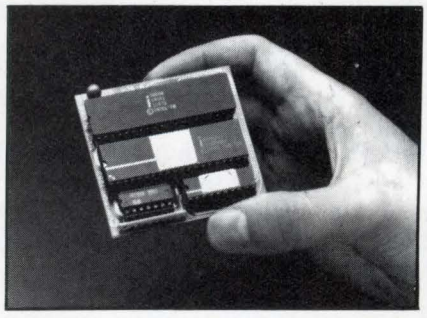
Sixteen-bit microprocessor

The 65816 is completely hardware and software compatible with the 8-bit 6502. As a hybrid 8- and 16-bit CMOS processor, it accommodates the object code of its 8-bit predecessor as a subset. On power-up, it is in emulation mode, allowing for normal operation of existing 6502 monitor routines or operating systems. Software includes an operating system for the development of 65816 software. It is complementary to the underlying Pro-DOS kernel, which handles all of the disk file management tasks. It will include a command processor, full-screen text editor, link editor, and several other utilities. **Hayden Software Co,** 600 Suffolk St, Lowell, MA 01853.
Circle 319

All-CMOS board computer

While providing hardware and software compatibility with Intel's iSBC 80/24, the CBC 80C/24 reduces power dissipation by 95 percent. The board comes in 3.58- and 2.5-MHz versions. Four 28-pin sockets allow 32 Kbytes of onboard RAM/EPROM. A lithium battery gives over 3 years of onboard memory backup. A total of 48 parallel I/O lines can be software configured as bidirectional or unidirectional ports. System software selects the data transfer format, control character format, parity, and communication baud rate. Pricing is $950 for the 8-Kbyte version. **Diversified Technology, Inc,** PO Box 748, Ridgeland, MS 39157.
Circle 320

Floating point coprocessor



Designed for AIM's 8086 CPU board, a floating point device can replace the original CPU for increased computational capabilities. The upgraded board extends the CPU instruction set with arithmetic, logarithmic, transcendental, and trigonometric instructions It implements the proposed IEEE floating point standard including all the single- and double-precision options. Applications are in robotics, graphics, numerical control, and process control. **AIM Technology,** 3333 Bowers Ave, Santa Clara, CA 95051.
Circle 321

Single-board computer for S-100

The SBC-300 is a high performance self-contained micro system designed around the Z80 micro family. It can perform as an IEEE 696 permanent bus master or as one of the slave processors on the bus to support multi-user applications. Features include 64 Kbytes of onboard dual-ported parity-checked memory, I/O functions that include two full-duplex ports, and a SASI port with 8-bit bidirectional data buses. Two versions are available: the 4-MHz version is $741, while the 6-MHz version is $825. **SDSystems, Inc,** PO Box 28810, Dallas, TX 75238.
Circle 322

High speed central processor

Based on the NS16032 chip, the UB3050 processor features a Multibus interface. The CPU has full 32-bit internal arithmetic and a symmetric instruction set for high level languages. Board has an 8-Kbyte cache memory with an access time of 45 ns. The interface supports 16 Mbytes of memory with 25-bit addressing. Bus arbitration can be either serial or parallel. The memory management unit provides full virtual 24-bit address mapping into a 25-bit physical address space. A single board costs $3995. **Unidot, Inc,** 602 Park Point Dr, Golden, CO 80401. **Circle 323**

System compatible with STD bus

The DT2712 provides 10 bits of resolution on 32 single-ended analog channels. It is powered directly from the 5-V supply on the STD bus. The input signals can be scanned at a throughput rate of 3300 samples/s. Compensation for timing differences is performed by an onboard jumper, making the board compatible with all STD bus processors. Jumper selectable for either I/O-mapped or memory-mapped addressing, it supports either software polled or vectored interrupt schemes. In 100s, price is $195. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Circle 324**

Converting rms to dc

With a guaranteed maximum nonlinearity of 0.02 percent, the AD637 operates from dc to 8 MHz. Fixed offset is ±0.5 mV and reading total unadjusted error is ±0.2 percent. The device computes the true rms value of complex ac waveforms. A crest factor compensation scheme holds additional measurement error to ±0.1 percent for crest factors of 3 and 10 percent duty cycles. The converter contains provisions for a decibel output and a denominator input. The output has a typical range of 60 dB with a ±1 dB typical error over a 7 mV to 7 V rms input. Pricing in 100s ranges from $13 to $23. **Analog Devices, Inc,** Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062. **Circle 325**

High capacity converter

On a single STD bus card, the DA-32 provides 32 channels of analog output. It uses only two I/O addresses and has a self-contained microprocessor. Specs include output range of 0 to 10 V, 8-bit resolution, 2-ms settling time, and 0.15 percent full-scale linearity accuracy, ± ½ bit. Levels for each channel are set by writing a value for a channel to the odd port followed by the channel number for that value to the even port. Price is $455 in single quantities. **rmac,** 716 Capitola Ave, Capitola, CA 95010. **Circle 326**

High speed analog/digital system

The GMAD1A-15B features 1-MHz conversion rates, 15-bit resolution, and multiplexing capability for 128 channels. The system is equipped with a sample and hold amp that provides a 1-ns aperture time. Maximum full-scale input voltage level is 10.24 V and the dc crosstalk between channels is less than ±0.005 percent of full scale. Specs include ±11-V, 70-dB common mode rejection, and 1.5-mV typical noise. Microcoded programmable interface has interchangeable logic adapters for compatibility with minis. Cost is approximately $10,000. **Preston Scientific,** 805 E Cerritos Ave, Anaheim, CA 92805. **Circle 327**

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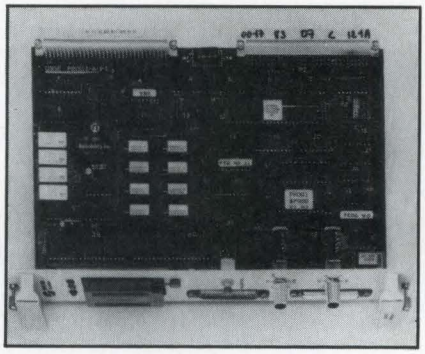
CIRCLE 128

Development station for PC

The EZ-PRO II, with an in-circuit emulator and associated software, forms a complete development system. Each emulator has a cross-assembler, linking editor, and debugger that run on the PC. Emulators are transparent and run at full speed without wait states. Assemblers are written in C and are transportable to other processors. Sixteen-bit processor support includes the 68000, 8086, and Z8001/2. Basic cost is $3995, and emulators range in price from $1395 to $3395. **American Automation,** 14731 Franklin Ave, Tustin, CA 92680.
Circle 328

Programmer board for VMEbus



Model DSSEPROG-1 programs all JEDEC-approved EPROMs. Onboard firmware includes programming routines, monitor, and communication software. An intelligent peripheral controller's dual ported RAM handles VMEbus interrupts. The board can be located anywhere in memory and occupies 256 consecutive odd-numbered addresses. In addition, it has 48 Kbytes of MOS dynamic RAM. Jumper selectable rates range from 4.8 to 19.2 baud. Price is $1995. **Data-Sud Systems/U.S. Inc,** 2219 S 48th St, Tempe, AZ 85282. **Circle 329**

In-circuit emulators

Development support for 8085, Z80, and NSC800 works with Intel's iPDS. Software packages that run under ISIS-PDS or CP/M allow linking via the serial port on the iPDS to give the user emulation control from the console. In addition, the software transfers hex files between the host computer and the emulator. Devices provide realtime emulation, mappable memory, hardware breakpoints, and debugging facilities. Prices start at $1895 for the emulators and $100 for the software. **Huntsville Microsystems, Inc,** PO Box 12415, Hunstville, AL 35802.
Circle 330

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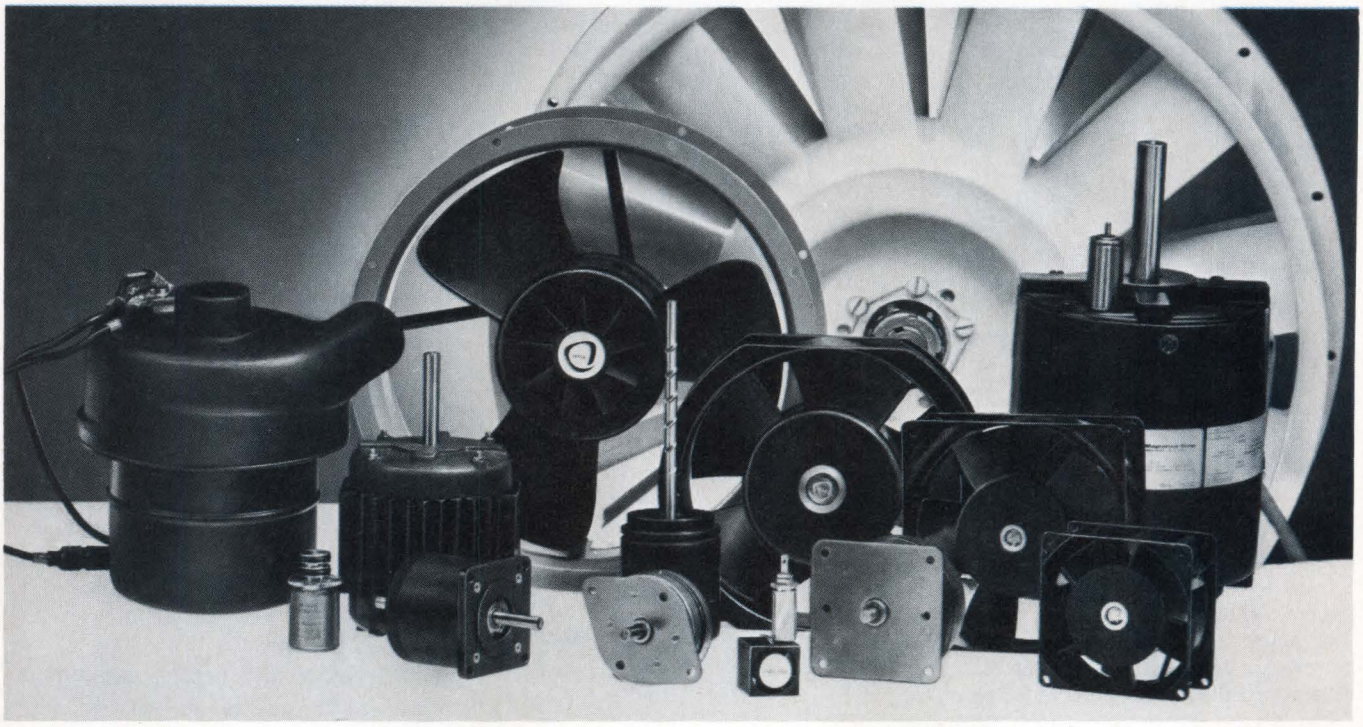

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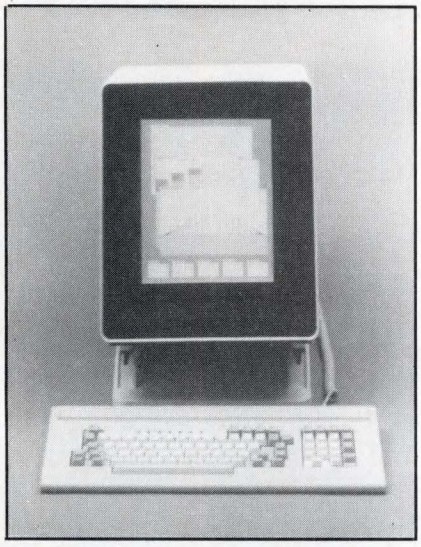
Graphics workstation



The Metamorph 15-in., 640- x 808-pixel monochrome display simulates an 8.5-in. x 11-in. sheet of paper. Hardware features include a 128-Kbyte display memory under the control of a 7220 graphics processor. The controller fills areas at 740 ns/pixel. Architecture is based on the 8088, which controls up to 256 Kbytes of programmable memory and up to 64 Kbytes of ROM. Supplied firmware allows emulation of DEC text and VT-125 graphics terminals, as well as Tektronix 401X graphics terminals. Unit price is $3495. **Companion Computer Corp,** 7404 Washington Ave S, Eden Prairie, MN 55344. **Circle 331**

Hardware/software package

The package allows PDP-11s and LSI-11s to run Intel micro development software. It consists of an 8080-compatible processor that plugs into the DEC system and software that emulates the Isis operating system. Data transfers to an Intel computer by floppy disk or serial communication link. In most cases, the Intel software executes two to three times faster on a DEC system. CP/M is also supplied with the system. The package costs about $2000 for a single-user system and less than $5000 for a three-user system. **Decmation,** 3375 Scott Blvd, Santa Clara, CA 95051. **Circle 332**

Computational nodes

The DN460 and DN660 provide high end 32-bit supermini performance. They have an integrated hardware floating point processor to handle IEEE format single- and double-precision numbers. With a 1-MIPS performance, the nodes include a three-stage, bit-slice pipelined processor with separate data and instruction caches, and a virtual address space expanded to 256 Mbytes per process. Available with color or monochrome displays, both nodes have low profile keyboards. A standard 12-Mbit/s LAN interface allows nodes to run on the same network. **Apollo Computer Inc,** 15 Elizabeth Dr, Chelmsford, MA 01824.
Circle 333

Microprocessor development

Based on the IEEE 696/S-100 standard, the Engineering Development Station (EDS) supports word/byte-wide ROM simulators and PROM/micro programmers. It features two double-sided, double-density 8-in. Shugart drives with a 2-Mbyte capacity; CP/M; 64 Kbytes of RAM; and two RS-232 ports. In addition, it has a 16-bit parallel port and a 4-MHz Z80 with memory management. Up to 16 Mbytes of RAM can therefore be addressed. Each station has six card slots for easy placement of connections. Price in single units is $5995. **Inner Access Corp,** 517K Marine View, Belmont, CA 94002.
Circle 334

Macrocell arrays

The HCA6348 has 4860 equivalent gates; the HCA6324 has 2295; the HCA6312 has 1200; and the HCA6306 has 648. The 3-micron silicon gate CMOS arrays constructed in two-layer metal technology yield loaded onchip gate delays of 2 ns. Input buffers operate at either TTL or CMOS voltage levels, while output buffers can drive 10 LS/TTL loads. Hardware macros implement 42 designs ranging from simple gates to shift registers. A variety of standard packaging options is available. Pricing is approximately $0.01 per gate for 10,000 pieces (plastic). **Motorola, Inc, MOS Integrated Circuits Group,** 3501 Ed Bluestein Blvd, Austin, TX 78721. **Circle 335**

Realtime graphics workstation

Either as a standalone workstation or as a terminal in a network, IRIS responds immediately to instructions without sacrificing functional range. The system is based on the geometry engine, which is a specialized floating point arithmetic chip. It performs all calculations for repositioning, shading, and other adjustments to 2-D and 3-D images. An array of either 10 or 12 engines handle rotation, translation, scaling, clipping, and perspective. Standalone workstation with disk is $60,000; $37,500 with terminal. **Silicon Graphics,** 630 Clyde St, Mountain View, CA 94043.
Circle 336

Add-in package for Apple II

As an add-in board and software package, QPAK-68 turns the Apple II into a 68000 assembly language development system. The complete system includes a plug-in board to run 68000 programs, a combined editor/assembler for source code, and a debugger for testing. The board uses a 68008 that is driven from the 7.16-MHz clock so it can run in parallel with the 6502. It shares the Apple's 64-Kbyte memory space and can access the same memory and peripherals as the 6502. Local memory is 8 Kbytes of EPROM and 2 Kbytes of RAM, expandable to 32 Kbytes and 8 Kbytes, respectively. Cost is $695. **Qwerty Inc,** 9252 Chesapeake Dr, San Diego, CA 92123.
Circle 337

Hierarchical CAE design package

Designed for use on the IBM XT, the structured interactive design system (STRIDES) eliminates redundant drawing of common elements. The editing system allows a change in one document to be automatically incorporated into the overall design including update of pin, net, and material lists. It manages an entire document tree from the top block diagram to individual components that include VLSI equivalents at the gate array or chip level. Price is $1900. **FutureNet Corp,** 21018 Osborne St, Canoga Park, CA 91304.
Circle 338

Software application modules

Designed for the Expert engineering workstation, software modules configure for electronic and electromechanical engineering, PC board design, or mechanical drafting. Types of modules include schematic design, logic simulation, and timing analysis. The simulation module is a true interactive logic simulator that enables verification of designs created with logic design software. It supports a large array of primitives—transistors and gates to RAMs, ROMs, and programmed logic arrays. Module prices range from $3900 to $10,000. **Versatec, a Xerox Co,** 2710 Walsh Ave, Santa Clara, CA 95051.
Circle 339

Tools for graphics support

Designed for the IBM 5080 graphics system, the DI-3000's capabilities include 2-D and 3-D dynamic image transformation, complex polygon fill with colors or patterns, and complete color table access. Written in ANSI Fortran, the integrated system contains 200 user-callable subroutines. It supports a broad range of terminals and hardcopy devices, and allows existing applications to be transported with little or no modification. Prices for the 25-year license including driver will start at $12,000. **Precision Visuals,** 6260 Lookout Rd, Boulder, CO 80301. **Circle 340**

Expansion board for PC

The Time Spectrum SB384 facilitates memory expansion to 640 Kbytes and offers communication functions in a single chassis slot. Standard features include socketed RAM, calendar/clock with rechargeable battery backup, one asynchronous communication port, and a Centronics or data products compatible parallel printer port. Memory features are parity checking and error reporting, switch-selectable addressing on any 64-Kbyte boundary, and complete IBM hardware/software capability. Cost is $395. **Persyst Products, Personal Systems Technology, Inc,** 15801 Rockfield Blvd, Irvine, CA 92714. **Circle 341**

Single-board evaluation module

When connected to a terminal or host computer, a module evaluates virtual memory performance in Multibus-based 16-bit SAM-Z8003EVM. Resident monitor program and control unit control, inspect, and alter onboard and offboard resources, including memory, I/O ports, VMPU and PMMU registers, and breakpoint set and clear. The evaluation module, including board, control unit, monitor program, and two RS-232 connectors for terminal and host computer connections, is $2500. **SGS Semiconductor Corp,** 1000 E Bell Rd, Phoenix, AZ 85022. **Circle 342**

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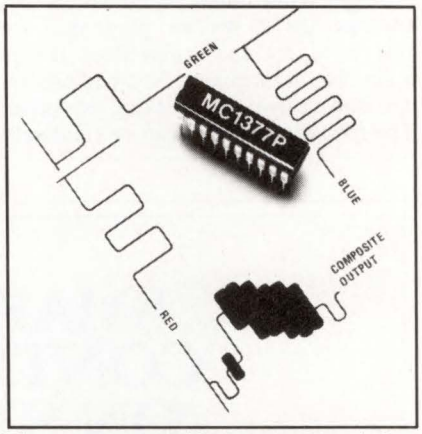
Communication/cluster control

An expandable family of emulation subsystems, the PS-3270/BSC plugs into the IBM PC, PC/XT, and compatibles. It uses a Z80B-based intelligent frontend processor with its own multitasking executive. The following systems can be emulated: single-station IBM 3276-2 control unit display with attached printer, small cluster system with printer and three downline display stations, or a large cluster system with printer and 13 display stations. Prices start at $1295. **ABM Computer Systems,** 23362 Peralta Dr, Laguana Hills, CA 92653. **Circle 343**

Video encoder circuit



The MC1377P combines RGB video information into a composite video signal using either NTSC or PAL formats. The chip contains a subcarrier oscillator, voltage-controlled phase shifter, two double-side band modulators, and RGB input matrices. The oscillator can be used as the master in a system or be driven externally. Inputs are ac coupled and a 1-V peak-to-peak input level produces full color saturation in the output. Price (in 100 to 999 quantities) is $2.35. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 344

Parallel CMOS multiplier

Featuring 100 percent screening to MIL-STD-883 Class C, the IDT7216/7217 is manufactured with proprietary CEMOS I technology. The multiplier has a 90-ns clocked multiply over military temperature ranges with maximum power consumption at 440 mW. The chip is available in 68-pin surface-mounted LCCs and 64-pin flatpacks. Applications include graphics display systems, speech synthesis/recognition, and digital filtering. In 100-unit lots, prices begin at $120 each for the 145-ns commercial grade version. **Integrated Device Technology, Inc,** 3236 Scott Blvd, Santa Clara, CA 95051.
Circle 345

Monolithic quad D-A converter

The AD7226 combines four latches, four 8-bit D-A converters, and four output buffer amps on a single chip. Fully microprocessor compatible, the converter transfers data into one of four data latches through a common TTL/CMOS input port. Control logic signals permit the user to address each chip separately. Single-supply operation is from 11.4 to 16.5 V, and an additional −5-V supply for dual operation provides higher accuracy. Housed in a 20-pin DIP, the converter comes in three packages for three operating temperatures. Cost is under $20 in 100s. **Analog Devices, Inc,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.
Circle 346

Programmable interval timer

The CMOS 82C54 is a TTL compatible pin for pin replacement for the NMOS 8254. It consists of three independent, separately programmable 16-bit timers. Maximum timer count frequency is 8 MHz; a 5-MHz 80C86/8086 system operates with no wait states. Standby power dissipation is 55 μW with a 10-mA operating current. Dual output voltage specification guarantees reliable operation in both NMOS and CMOS systems. The 24-pin chip comes in cerDIP and plastic. In quantities of 100, prices range from $15.40 to $79.73. **Harris Corp, Semiconductor Sector,** PO Box 883, Melbourne, FL 32901.
Circle 347

Resettable static RAM

Organized 1024 x 4 bits, the Am9150 uses a reset feature that clears the entire memory array in two cycle times. The architecture is suited for cache memory applications in mainframes, minis, and engineering workstations. Additional applications include address translation, memory mapping, and high speed buffer memory. Reset/clear feature allows use in video imaging and laser printing. The 25-ns device is packaged in 24-pin ceramic and is priced at $25 in 100s. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086.
Circle 348

Metal-gate CMOS gate array

The TM3600 features a 13-ns/5-V gate delay, 3- to 5-V power supply, TTL or CMOS compatibility, and maximum clock frequency of 5 MHz at 5 V. After preparation of the proprietary mask, the wafer is processed, tested, and made available as dice or packaged parts. It has 69 bonding pads; package choices include LCC, flatpack, ceramic, cerDIP, and DIP. The cells perform logic functions such as gates, flipflops, counters, current/voltage source, and op amps. The 10,000-piece price ranges from $5 to $10. **Telmos Inc,** 740 Kifer Rd, Sunnyvale, CA 94086.
Circle 349

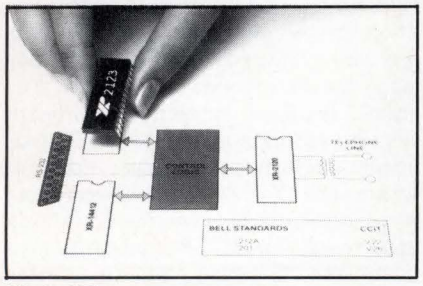
Register-file EEPROM

Integral address latch and input data latch eliminate the need for a 2048-bit EEPROM to hold address and data valid during the erase/write operation. Any byte can be written or erased without affecting the rest of the memory, or the entire memory can be erased in one cycle. The SY2802E endures 1 x 10^4 write cycles and retains data for 10 years. Organized as 256 words x 8 bits, the chip comes in 18-lead cerDIP and plastic packages. Prices are $4.50 in 1000s. **Synertek Inc, sub of Honeywell,** 3001 Stender Way, Santa Clara, CA 95054.

Circle 350

Bell-compatible modem chip

The XR2123 is a CMOS IC that provides phase-shift keyed modulation and demodulation. It performs either 1200 bits/s (needed for Bell 212A compatibility) in full-duplex, or 2400 bits/s in half-duplex mode. Power consumption is 10 mW and the chip requires only a 5-Vdc supply. Modem is packaged in a standard 28-pin DIP. Price is $23 in 1000s. **Exar Integrated Systems, Inc,** 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088.



Circle 351

Microcontroller in CMOS

The COP424C/COP425C has 1 Kbyte of ROM, while the COP444C/COP445C contains 2 Kbytes of ROM. In addition to the CMOS instruction set, the controllers offer 50-μW power dissipation and instruction cycle times from dc to 4 μs. Based on microCMOS double-polysilicon gate technology, the chips are micros with all system timing, internal logic, ROM, RAM, and I/O. Users have up to 27 mask-programmable output options that can be programmed at the same time as the ROM pattern. Prices begin at $2.60 each in 100,000-piece quantities. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle 352

Low noise op amps

The LT1007 and LT1037 offer 2.5 nV$\sqrt{\ }$Hz wideband noise, 1/f corner frequency of 2 Hz, and 60 nV peak-to-peak, 0.1 to 10-Hz noise. Open-loop voltage gain is 20 million driving a 2000-Ω load. With a 600-Ω load, the amps achieve 12 million open voltage gain. The 1007 is internally frequency compensated for unity gain and guarantees 1.7 V/μs minimum slew rate. The 1037 is stable in closed-loop gains of five or more, and slews at a minimum of 11 V/μs. In 100s, prices start at $4. **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle 353

Gate arrays with higher density

The Q1500A offers 84 I/Os; the QH1500A offers 120. Both arrays have 1500 gate densities and can be used in TTL, ECL, or mixed systems. Typical gate delays are 0.9 ns with flipflop toggle rates of 250 MHz. A 95-percent utilization is achieved with automatic layout. A high I/O-to-gate ratio relieves system partitioning problems, and a mixed TTL/ECL structure reduces system part count by eliminating transistors. Both arrays operate over the full military temperature range. **Applied Micro Circuits Corp,** 5502 Oberlin Dr, San Diego, CA 92121.

Circle 354

Multiplying D-A converter

The 12-bit MP7623 features both integral and differential linearity at 0.2 ppm/°C maximum and monotonicity guaranteed over the entire temperature range. Settling time is less than 1 μs for a 20-V step to 0.01 percent. Specific applications include digital/synchro conversion, programmable amps, and automatic test equipment. Improved design makes the device latchup free, so no output protection diodes are needed. Also, a MSB technique reduces system feedthrough error and noise. The 100-piece price ranges from $12.45 to $40.65. **Micro Power Systems, Inc,** 3100 Alfred St, Santa Clara, CA 95050.

Circle 355

SOFTWARE

Generic concurrent CP/M

The software can be configured for single- and multi-user systems and is compatible with PC-DOS. It supports networking via DR soft/net, and it features shared code support. This allows sharing of separately written code segments for lower memory requirements and reduced program loading time. It also supports Intel's 8087 math coprocessor chip. Based on a high performance file system, it includes multisectored I/O, record buffering, and directory hashing tables. **Digital Research Inc,** 160 Central Ave, Pacific Grove, CA 93950.

Circle 356

Communication software

Applications for SNA, network management, and X.25 communication are available on the Tower 1632 under Unix and on the 9300 under ITX. Programs assume the SNA profile of several IBM devices, while development tools perform active logic traces and breakpoints. An SNA/RJE application, 3270 data stream compatibility, and X.25 packet level interface are available. **NCR Corp,** 11010 Torreyana Rd, San Diego, CA 92121.

Circle 357

Realtime option for RT-11 systems

Share-eleven supports more than 10,000 interrupts/s. It provides kernel debugging facilities and a graphic system performance monitor for multi-user RT-11 systems. A full set of system calls and utilities eases realtime programming. Documentation is included. The Share-eleven realtime option costs $1500, while the basic Share-eleven is $1000. **Contel Information Systems, Inc, Software and Systems Div,** 4330 East-West Hwy, Bethesda, MD 20814.

Circle 358

Network development

High level Bridge software customizes Ethernet communication servers. The software includes C compiler, a 68000 assembler, link editor, S-hex record formatter and downloader, and documentation. It supplies the tools needed to compile and assemble C source code. Available on nine-track tape (1600 bits/in.), it is in Unix tar format for customization. Price is $250. **Bridge Communications, Inc,** 10440 Bubb Rd, Cupertino, CA 95014.

Circle 359

Virtual memory operating system

A release of iMAX 432 is aimed at designs for fault tolerant computer systems, Ada-based workstations, and 32-bit computer systems. The system performs deallocation and afterwards combines variously sized blocks into large contiguous blocks for new storage. The architecture supports a segmented memory management approach where segments can vary in size from 1 byte to 64 Kbytes. Software can be written in modular form to reduce development time and software maintenance. Price is determined by quantity, with the first copy at $8000, and each copy beyond 150 priced at $500. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 360**

Application processor

Fourth-generation Pro-IV develops, modifies, and operates applications. The multiterminal multidata file development/runtime system processes Cobol, Basic, and Fortran files. Features include menu driven application development, common data dictionary, interactive screen and report definition, windowing, and auto-generated documentation. Development license is $20,000. **Pro-IV, Inc,** 119 Russell St, PO Box 595, Littleton, MA 01460. **Circle 361**

Management information software

Themis understands English questions and commands. It will retrieve information requested via keyboard for output on a screen or printer. Users can also ask for functions such as sorting, logical comparisons, and calculations. The initial version runs on the VAX-11. It uses 1.5 to 2 Mbytes of main memory and requires either Datatrieve or Oracle relational DBMS. Basic vocabulary of more than 900 English words can be easily expanded. Translation from English into database query adds 0.4 s to CPU time. Price is $24,500. **Frey Assocs, Inc,** Chestnut Hill Rd, Amherst, NH 03031. **Circle 362**

Operating software extension

Microsoft Windows upgrades MS-DOS to provide a universal operating environment for bit-mapped application programs. It allows independent software vendors to develop graphically based, integrated software packages that run without modification on any 16-bit micro. A window management feature allows users to view unrelated application programs simultaneously, and to transfer data from one program to another. Hardware requirements are 192 Kbytes of RAM, a mouse, two floppy drives, and a bit-mapped display. **Microsoft Corp,** 10700 Northup Way, Bellevue, WA 98004. **Circle 363**

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Megaword timing. Using our transistional timing, capture and display two 20ns pulses occuring up to 5 seconds apart, with 20ns resolution. This means no more trading off resolution against memory. And it opens up new applications such as disc drives.

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8048	8051	6800	6502
8080	8085	6809	1802
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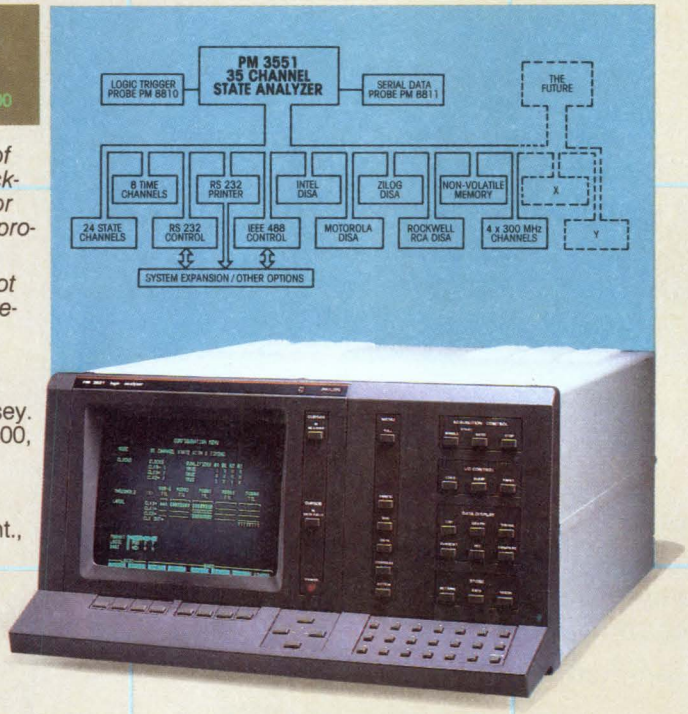
CIRCLE 135



PHILIPS GOOD
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Chassis for Q-bus

The 8700 series of logic enclosures is designed for users needing expanded capacity for existing LSI 11/23 systems. The 8705 chassis features a side-loading Q-bus backplane with 27 dual-wide slots. It also has a 300-W power supply, ac input connector with line filter and switch, cooling fans, and DEC-compatible power sequencing. Cost is $1600. The 8703 provides 18- or 22-bit memory address, while retaining the use of 18-bit Q-bus peripheral controllers. Cost is $5300. **Monolithic Systems Corp,** 84 Inverness Circle East, Englewood, CO 80112.
Circle 364

Leadless chip carrier family

Three different designs mount VLSI chips on a minimum of board space without sacrificing easy assembly, inspection, economy, or reliability. The CCPS connector series includes a 160-pin socket with a hinged cover to hold a LCC securely. A second socket is JEDEC type A 68-pin with a twist-on cover that can accept a heat sink. A LCC pin frame 68 consists of a glass reinforced thermal plastic frame with embedded connecting pins. Prices for the connectors run from $2 to $8 each in quantity. **ITT, Cannon Electric Div,** 10550 Talbert Ave, PO Box 8040, Fountain Valley, CA 92708.
Circle 365

Ribbon cables

The PTFE insulated series is compatible with insulation displacement connector systems approved under MIL-C-83503. The 0.050-in. pitch cables support widths up to 64 connectors, in AWG sizes of 24, 26, and 28. They provide a low dielectric constant, low crosstalk characteristics, fast signal speed, and a low dissipation factor. Nickel-plated version functions in extreme temperatures ranging from −65 to 260°C; silver-plated option provides solderability. **W L Gore & Assocs, Inc, Electronic Products Div,** 1505 N Fourth St, PO Box 1389, Flagstaff, AZ 86002.
Circle 366

Family of Ethernet cables

The 9880 is a trunk/coaxial cable with tinned copper conductor and cellular polyethylene. It has a four-layer shield. Standard put-ups are 500 ft, 1000 ft, and 1640 ft, with 1000-ft price of $933. The 89880 is a plenum non-conduit trunk/coaxial cable. Also with a four-layer shield, the cable has a bare copper conductor and a cellular FEP Teflon dielectric. Standard put-ups are 100 ft, 500 ft, 1000 ft, and 1640 ft with 1000 ft priced at $4350. **Belden,** 2000 S Batavia Ave, Geneva, IL 60134.
Circle 367

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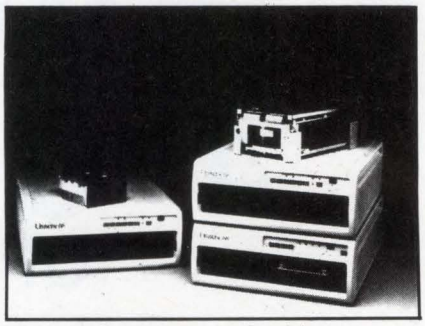
Full-function small computer

The PC Traveler has a gas plasma display, with a full 80 x 25 format. The 9¼-in. screen offers complete graphics capability. It uses dual 16-bit 80186 CPUs for fast processing. The full-function 80-chars/s printer supports multiple print fonts, character sets, and dot-addressable graphics. It prints at 80 or 132 chars/line on letterhead or fanfold paper. Other features include a 6.2-Mbyte cartridge disk drive and a custom keyboard with key-initiated, ROM-based diagnostics. Cost is $4495. **Strategic Technologies, Inc,** 7001 Peachtree Industrial Blvd, Norcross, GA 30071. **Circle 368**

Two supermicrocomputers



The Universe 68/35 and 68/67 use 12.5-MHz 68000s for high speed. They incorporate a 32-bit Versabus I/O bus, 32-bit main memories, 32-bit disk channels, and a 32-bit,4-Kbyte cache. The 68/35 features a 5¼-in. Winchester with a formatted capacity of 35 Mbytes. The 68/67 has an 8-in. Winchester with a 64-Mbyte formatted capacity. A built-in 45-Mbyte streaming tape drive provides system backup. The 68/35 is priced at $14,900, while the 68/67 is $24,900. **Charles River Data Systems, Inc,** 983 Concord St, Framingham, MA 01701. **Circle 369**

Microcomputer with Unix

Based on the 68000, the 83/80 combines high throughput and a full Unix operating system. It conforms to IEEE 696/S-100 bus standards with a 10-MHz clock rate and memory management. A SMD disk controller yields 800-kbyte/s average transfer rate in read mode and 560 kbytes/s in write mode. The controller supports one or two 80-Mbyte hard disks. Standard 512 Kbytes of RAM expands to 3.25 Mbytes. Four-channel serial RS-232-C I/O boards use DMA for all outputs. Cost is $20,990 with Unix. **Dual Systems Corp,** 2530 San Pablo Ave, Berkeley, CA 94702. **Circle 370**

Single-board computer

The Super 186 is a 16-bit, S-100 device built around the 80186. The 8-MHz computer configures as a standalone bus master or bus slave to serve single or multiple users. It features 256 Kbytes of memory expandable to 1 Mbyte, and a floppy drive controller that supports both 8- and 5¼-in. disks simultaneously. The computer also has four serial RS-232 and two parallel I/O ports, DMA controller, parity, and monitor EPROM to aid in initial loading. Price is $1650. **Advanced Digital Corp,** 5432 Production Dr, Huntington Beach, CA 92649. **Circle 371**

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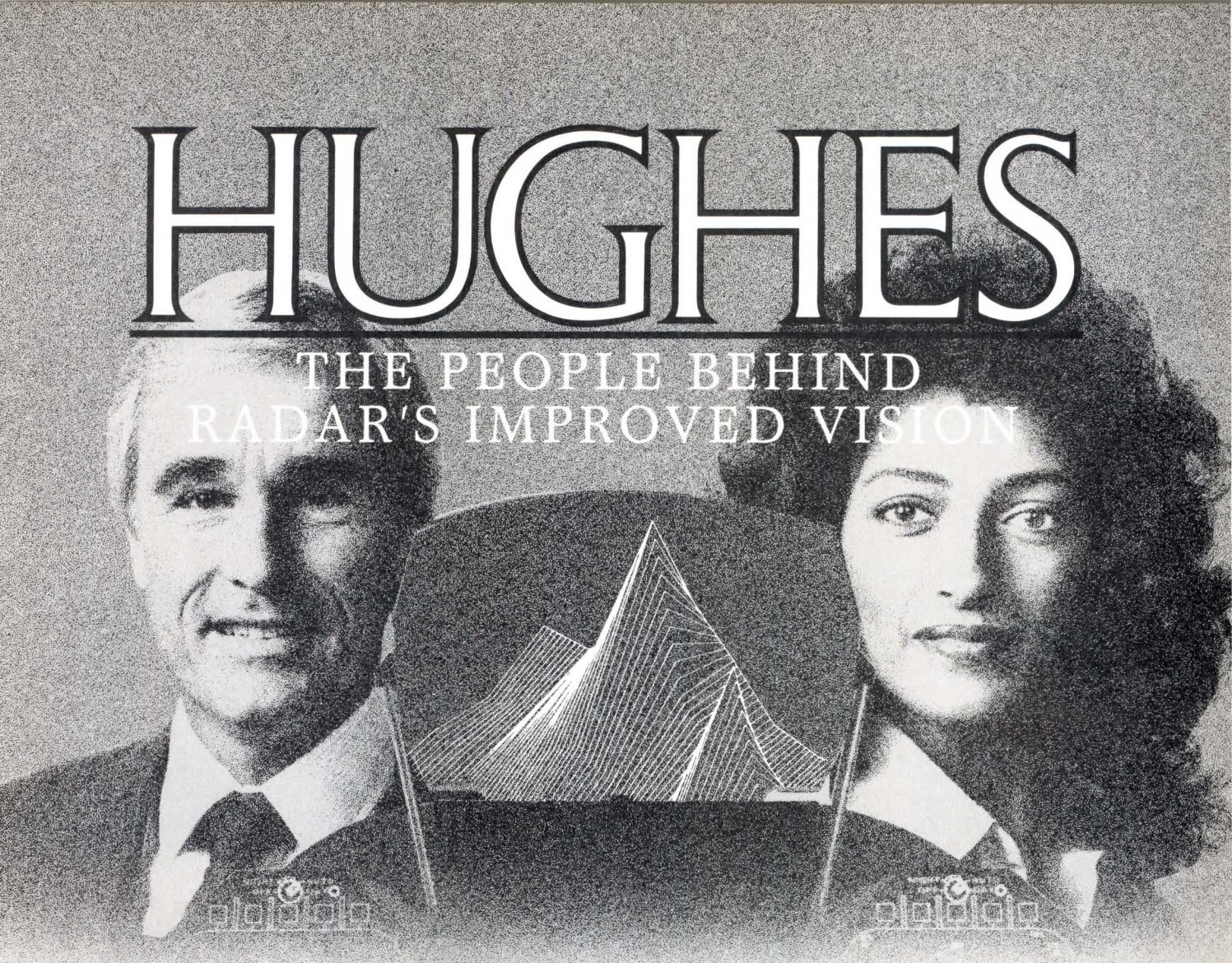

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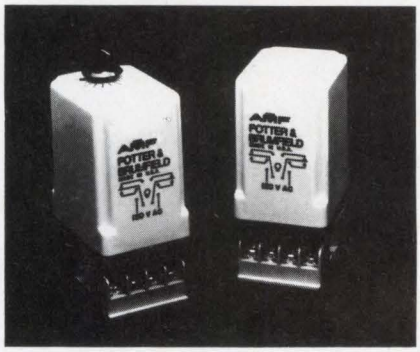
Keyboard plug-compatible with PC

Besides familiar key placement, the low profile Inductric unit features microbased electronics and solid state inductive switches. It comes with sync/async RS-232 format and TTL level ASCII serial output. Depressing a key moves a ferrite core into the field of a balanced differential transformer etched on the PC board. As inductive coupling changes, the transformer becomes unbalanced so a signal is received by the pulse circuitry. The model 88KT-15 is priced at $250 (1 to 9 pieces). **Elco Corp, Keytek Div,** 6424 Warren Drive, Norcross, GA 30093.
Circle 372

Time-delay relays

The plug-in CB series features a CMOS IC to precisely control timing functions. Shortest timing range is from 0.1 to 1 s, while the longest is from 10 to 100 min. Relays have delay on operate, delay on release, and interval on timing modes. Depending on timing function and termination, spdt or dpdt contacts are available. Contacts are rated 10 A at 240 Vac. All models have octal-style plug termination. Cost ranges from $22.50 to $26.25 each in 100-piece quantities. **Potter & Brumfield Div, AMF Inc,** 200 Richland Creek Dr, Princeton, IN 47671.



Circle 373

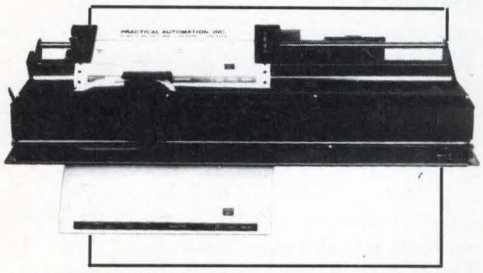
Thin-film resistor and network

The devices offer an integration density of 600 kΩ/mm^2 with 0.001 percent and up to 0.0005 percent precision. Temperature coefficient is less than ±5 ppm/°C. Stability specs include less than 500 ppm drift after 1000 h at 155 °C, tracking characteristic is better than 1 ppm/°C, and relative stability between two resistors under stress is less than 200 ppm. Applications are in miniature networks such as A-D and D-A conversion circuits. Networks can be packaged bare or in chip carriers. **Sfernice International,** 117, bd de la Madeleine, BP 17-06021, Nice, Cedex, France.
Circle 374

Antiglare VDT filter

The CP-50 contrast enhancement filter uses a circular polarizer to reduce the effects of glare and to improve screen contrast. The polarizer absorbs ambient light falling on the screen rather than allowing it to bounce back to the user's eyes. Filter attaches to the screen with self-adhesive mounts; no tool or assistance is needed to install or remove them. They are easy to clean with a filter-cleaning fluid. Cost is $49.95. **Polaroid Corp,** 575 Technology Square, Cambridge, MA 02139.
Circle 375

Matrix printer mechanism

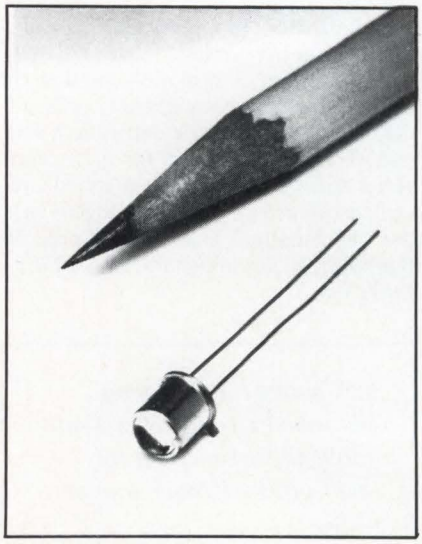


The heavy duty 15-PMC accepts 3- to 16-in. wide perforated paper and prints at 275 chars/s, 10 pitch, and from one to six part forms. It uses a nine needle free flight head, rated for 1350 Hz at 0.025 stroke for over 300 million characters. The ribbon cassette is stationary and driven directly from the carriage motor. The dc motor uses an encoder with photocells in quadrature for motion control. Head moves bidirectionally. Price is $243, quantity 1000. **Practical Automation,** Trap Falls Rd, PO Box 313, Shelton, CT 06484.

Circle 376

Hermetic infrared emitting diode

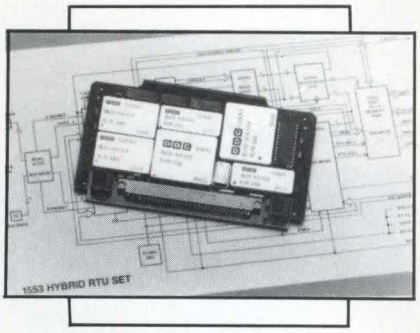
The OP231 series are GaAlAs devices available in hermetic TO-46 housings. Emitting wavelength centers at 875 nm to match the spectral response of silicon phototransistors. Improved coupling efficiency allows lower drive currents and improves reliability. Higher noise immunity means lower output signal amplification. Applications include signal/data transmission in scientific, military, and industrial markets. **Optoelectronic Div, TRW Electronic Components Group,** 1270 Tappan Circle, Carrollton, TX 75006.



Circle 377

Dual-redundant RTU

The BUS-65401 provides a complete intelligent interface between a serial MUX data bus and a three-state data highway. The unit's interface appears to the subsystem as a 256-word memory mapped I/O. All RTU protocol, memory management, and built-in tests are performed without subsystem intervention. The device consists of a set of standard hybrid products including a dual transceiver, two encoder/decoders, RTU protocol hybrid, and dual-port memory. In addition, the card contains two transformers, a crystal oscillator, and three ROMs. Prices start at $3695. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.



Circle 378

High efficiency green LEDs

Lamps are two to three times brighter than standard green, and as bright or brighter than high efficiency red and yellow. Sizes are T-1, T-1¾, and T-¾, with clear and diffused lenses and eight viewing angles from 24 to 180 degrees. They are also available in rectangular lamps. Price in quantities of 1000 is $0.23 to $0.48, depending on lamp type and intensity rating. **General Instrument, Optoelectronics Div,** 3400 Hillview Ave, Palo Alto, CA 94303.

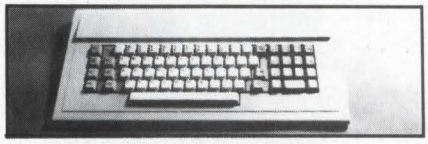
Circle 379

Choke on DIP footprint

The Multiple Choke provides simultaneous protection of eight data lines. It is used on computers, terminals, and other equipment that requires interfacing cables. Each winding gives inductance of 150 μH (reference 1 kHz and $\pm$25 percent). Isolation is 1000 Vac between windings. The device mounts on a standard 16-pin DIP spacing with 0.042-in. diameter pins and a maximum height above the PC board of 0.430 in. **Cramer Coil & Transformer Co, Inc,** 1121 15th Ave, Grafton, WI 53024.

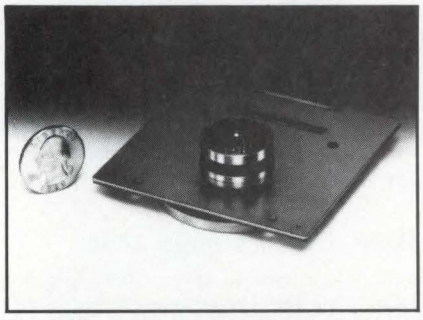
Circle 380

Ergonomic design keyboard



As standard equipment with the 8510 graphics computer system, the 8535 includes height and angle adjustment and a coiled connection cable. It provides a 128-character ASCII set and function keys for cursor control, space, carriage return, escape, and delete functions. The numeric keypad is active only in shift mode, otherwise it generates character and control codes for use as function keys. LSI n-channel MOS electronics perform keyboard encoding with n-key rollover. **Terak Corp,** 14151 N 76th St, Scottsdale, AZ 85260.
Circle 381

Brushless pancake motor



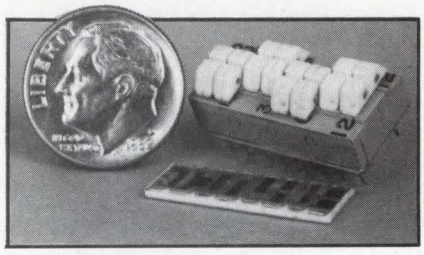
The 12-Vdc device is designed for direct drive of microfloppy disks. Its brushless design and use of ball bearings give it service life in excess of 10,000 hours. Rated load is 50 g-cm, rated current is less than 230 mA. Speed regulation is ±1.5 percent of 300 rpm over a torque range from 0 to 72 g-cm. Rise time to rated speed is 300 ms maximum. Starting torque is 150 g-cm minimum, and starting current is 700 mA maximum. **Canon USA, Inc, Electronic Components Div,** One Canon Plaza, Lake Success, NY 11042.
Circle 382

Flat-panel display

The CVA 640/250 displays 25 lines of 80 characters on its bit-mapped LCD. The module consists of a panel/driver assembly with a viewing area of 5 x 6.4 in. The 640- x 250-pixel format allows the use of a broad range of application software. Also available is a system controller card with both an RS-232 and parallel ASCII input. The 1000-quantity price is $345. **CrystalVision Inc,** 1313 Geneva Ave, Sunnyvale, CA 94089. **Circle 383**

Switchable DIP attenuator

Balanced T type 7010 series has 50-, 75-, and 600-Ω impedance values. The eight-pole device configures in a standard 16-pin DIP. It uses a precision laser trimmed thick film resistor network, mated to a gold contact switch system. Custom design or standard attenuation increments of 0.1 to 1.5 dB are available. The 7010 comes unsealed, or sealed with a plastic adhesive that washes off. Prices range from $3 to $5. **Vernitron Corp, VRN Div,** PO Box 44000, St. Petersburg, FL 33743.



Circle 384

Silicon transistor

The BFQ 77 has a line width of only 0.8 μm and an operating range up to 6 GHz. Rated noise is 2.8 dB at 4 GHz (8-dB associated gain). The Cerec package is suitable for mounting on all types of PC boards. High service reliability is realized through multilayer metallization, ion implementation, self-aligning lithography, and additional double passivation. **Microwave Semiconductor Corp,** 100 School House Rd, Somerset, NJ 08873.
Circle 385

Video amplifier

The 3-bit digital device has 100-MHz bandwidth and 3.5-ns rise and fall time. It accepts either 3 bits of TTL or ECL (differential) digital information and directly converts the data into eight gray scales on the CRT. The amp is virtually glitch-free and eliminates the need for a D-A converter at the controller. Bit-mapped controllers can drive 3-bit planes directly into the CRT monitor. **U.S. Pixel Corp,** 59 Fountain St, Framingham, MA 01701.
Circle 386

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Does the 60-Hz monitor you're considering meet these design parameters?

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CIRCLE 139

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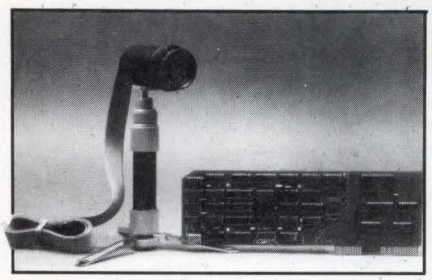
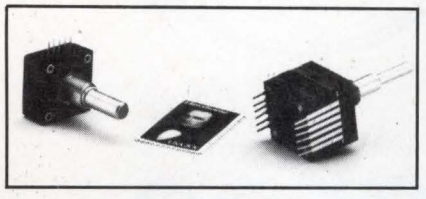
CIRCLE 167

Digital image sensor



Using a 256 x 128 silicon array and menu driven software, the Micro D-CAM interprets, enhances, or stores images via a computer. With the added dimension of sight, the computer can be used in graphics, pattern and character recognition, and robotics. Utilities handle auto-exposure, multilevel gray scale, screen dumps, picture storage, and image enhancement. IBM PC and Apple II versions are available (RS-232 version available on special order). The sensor costs $295. **Micromint, Inc,** 561 Willow Ave, Cedarhurst, NY 11516.
Circle 387

Custom-built logic switch



The microminiature device provides a direct digital interface for complex manual switching requirements. In a 0.865-in.-square package, the 28-position P/REL has a high temperature withstanding ability for wave soldering. The terminals are 0.016-in. thick for greater strength and can automatically be trimmed to any specified length up to 0.875 in. The switches sell for about $3 each in 1000-lot quantities. **Standard Grigsby, a Gordos International Co,** 920 Rathbone Ave, Aurora, IL 60507.
Circle 388

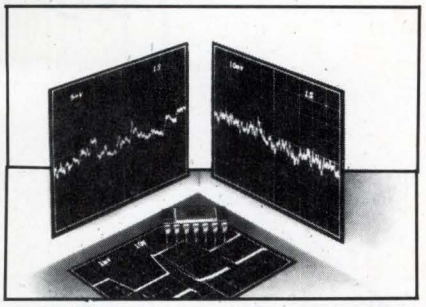
Wide-angle LED

Cylindrical SLV 56 series features a precision cone-shaped clear lens with full 180-degree brightness. Users can mount the LED perpendicular to the PC board, but view it parallel to the board. Applications include mainframe card cages, telecommunication switch gears, and disk drives. Colors are red, orange, green, and yellow. Price in 1000 pieces is $0.25 each. Delivery is four to six weeks. **Rohm Corp,** PO Box 19515, Irvine, CA 92713.
Circle 389

Digital filter

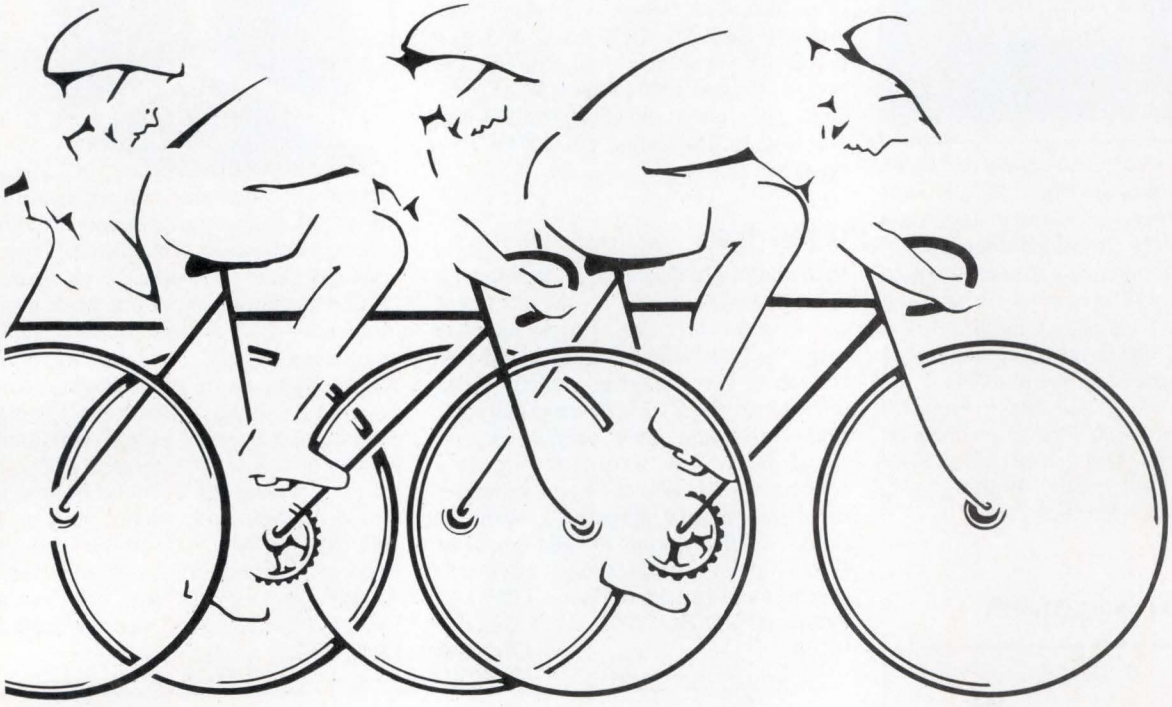
Providing eight delay stages, multipliers, and adders in a single IC, the TDC1028 is TTL-compatible for finite impulse response filters and multibit digital correlators. The bit-slice, video speed device provides a 20-megasample/s throughput and 4-bit coefficient and signal data words. Format for words is selectable with a choice of two's complement or unsigned magnitude. Applications for the device include matched filters, pulse compression, waveform synthesis, and adaptive filters. **TRW LSI Products,** PO Box 2472, La Jolla, CA 92038.
Circle 390

Instrumentation amplifier



Designed for high precision applications, the AD624 delivers maximum ±0.001-percent nonlinearity. In addition, it provides maximum ±10-ppm/°C gain tempco and maximum 0.2-μV peak-to-peak input and 10-μV output noise. Onchip gain setting network eliminates factoring in cost, temperature, and accuracy effects of external gain setting resistors. The pin-programmable gains permit maximum gain error from ±0.02 percent (G = 1) to ±0.5 percent (G = 1000). Four gain setting pins can connect for gains of 1, 100, 200, or 500. The 16-pin ceramic package is priced in 100s from $11.90. **Analog Devices, Inc,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.
Circle 391

proNET™



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proteon

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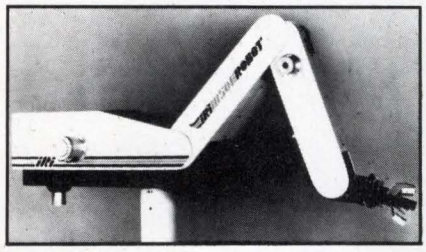
CIRCLE 141

Servomotor-controlled robot

The IRI M50-E is controlled by digital signals generated by a proprietary monoboard with eight micros. Servomotors improve velocity control of robot motion for more accurate path control. Operating at 400 Hz or above, the small-lightweight servos easily fit existing robot modules. Targeted for precision-oriented tasks, the robot is priced under $20,000. **International Robomation/Intelligence,** 2281 Las Palmas Dr, Carlsbad, CA 92008.



Circle 392

Expert system generator

Artificial intelligence program Expert-Ease works by generating rules from examples. It will then remove redundant logic, producing a logic tree that specifies the key to the decision or the result. An expert or novice can use the inquiry facility to produce an expert decision, predict a result, or solve a problem. Applications are in fields of industry, commerce, and research. **Expert Software International Ltd,** 4 Canongate Venture, New St, Royal Mile, Edinburgh, United Kingdom.
Circle 393

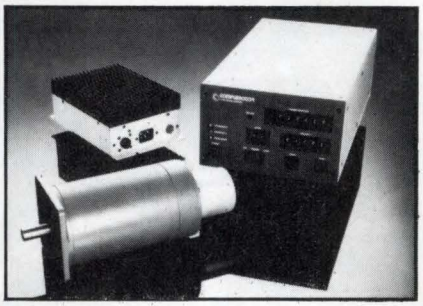
Optical inspection system

The P-SEE uses pattern verification as opposed to design rule inspection. It features nonspecular lighting that allows virtually no false readings. Cameras provide 1.67 square-ft/min of inspection at a 0.0005-in. resolution. Speed can be increased with extra cameras. Applications include inspection of PC boards, glass masters, inner layers, substrates, and flex circuits. System adapts to any host, or networks with other company equipment. **DIT-MCO International,** 5100 E 59th St, Kansas City, MO 64310. Circle 394

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

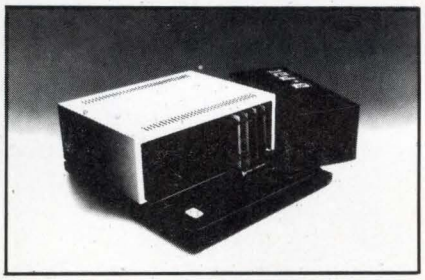
Digital servo system



The Model 2100-PT indexer provides precise closed-loop position control based on feedback from an optical encoder. It drives standard stepping motor translators and 25,000-step/rev motor/drives, thereby simplifying precision positioning. It connects to any standard incremental optical encoder (linear or rotary) and is suitable for ultraprecise X-Y table indexing (to 0.5 μm) and stall detection. The system is programmed via RS-232-C or optional IEEE 488 interface. **Compumotor Corp,** 1310 Ross St, Petaluma, CA 94952. Circle 395

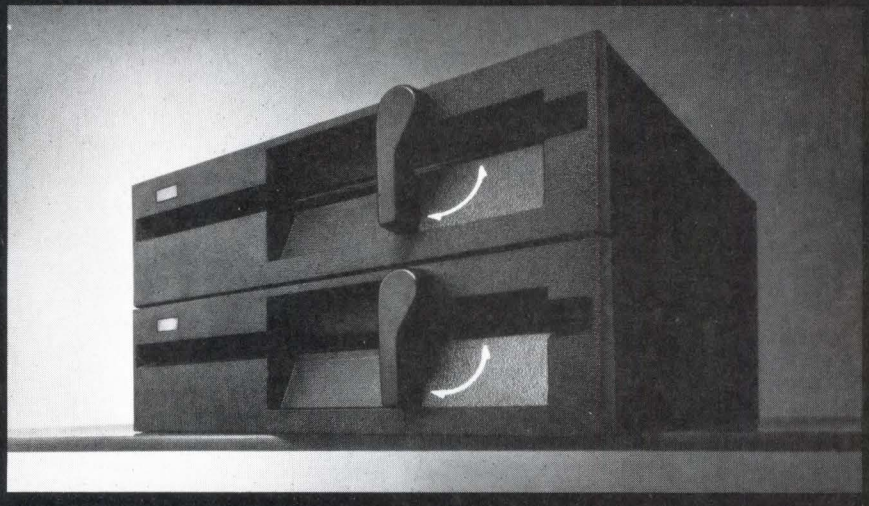
Industrial microcomputer

The A-PAC, designed for programmable acquisition and control, combines a built-in analog and I/O interface with a personal computer and a logic controller. A selection of application programs is available for data logging, multiloop PID control, batch control, and distributed processing. Additional features are enhanced EPROM, battery-backed RAM, and clock/calendar. The startup kit has a CRT and keyboard peripherals, I/O interfaces, and cables. Cost is $5999. **Action Instruments Inc,** 8601 Aero Dr, San Diego, CA 92123.



Circle 396

PUT MORE DRIVE INTO YOUR SYSTEM.



Teac's FD-55 series half-high floppy disk drives run on a mere 5 watts. So now you can add more drives without the need to add more power.

In fact, Teac offers the only full line of 5¼ inch half-high mini disk drives that run on half the power of ordinary dual drive units.

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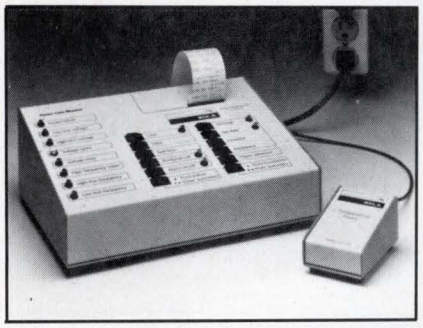
Power monitor



The device features user-adjustable disturbance thresholds, disturbance value printouts, and ambient temperature and dc voltage level monitoring. It allows continuous analysis of line power quality at installation sites. An onsite pot adjustment triggers power disturbance recording. The unit monitors both the dc voltage of power supply and high frequency or spike on the dc supply line via a BNC. The monitor is priced below $2000. **Sola Electric,** 1717 Busse Rd, Elk Grove Village, IL 60007. **Circle 397**

Chassis-mountable power supply

Redesign of models CM 3.15.5 and 3.12.5 results in triple-output supplies that run cooler than before. Output of the 3.15.5 is ±15 V at 100 mA and 5 V at 500 mA, while output of 3.12.5 is ±12 V at 100 mA and 5 V at 600 mA. The 5-V output is isolated from the dual output so it can be used to power linear/digital circuit combinations. A clamp barrier strip secures wires without twisting. A recessed barrier strip makes tight connections while protecting the unit from damage. **Calex Manufacturing Co, Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523.
Circle 398

Power MOSFETs

The devices come in ratings from 50 to 500 V, 0.2 through 40 A, in six package configurations. Ultrafast switching speeds make them ideal for high frequency switching applications. The MOSFETs have low conduction losses at low blocking voltages up to 200 V. Also available are IGTs that offer high input impedance, voltage-controlled turn-on/off features of MOSFETs, and low on-state conduction losses of bipolar transistors. Initial offerings include 10- and 25-A, 500-V rated devices. **General Electric Co,** 1 Belmont Ave, Bala Cynwyd, PA 19004.
Circle 399

Switching voltage regulator

The LAS 6320P series is a monolithic IC designed for fixed frequency pulse width modulation converter applications. Capable of output voltages from 2.25 to 24 V with output currents of 2 A, the chip features a temperature compensated voltage reference. In addition, it has a sawtooth oscillator with overcurrent frequency shift, linear trailing edge pulse width modulator, and transconductance error amp. The device is available in a 14-pin plastic DIP with prices ranging from $2.20 to $4.50 depending on quantity. **Lambda Semiconductors, div of Veeco Instruments,** 121 International Dr, Corpus Christi, TX 78410. **Circle 400**

Converters with 4:1 input range

Additional models in the WP series provide 25 to 30 W of isolated regulated power. They operate over a 9- to 36-Vdc input range and have outputs of 5 V at 5 A, 6 V at 4.5 A, 12 V at 2.5 A, and 15 V at 2 A. The units accept standard battery inputs of 12, 24, or 28 V with virtually no deviation in performance over the entire range. Features include efficiencies up to 85 percent, 500-Vdc isolation, input surge protection to 50 Vdc, and output noise of 5 mV rms, maximum. Prices range from $149.30 to $209, depending on quantity. **Stevens-Arnold, Inc,** 7 Elkins St, Boston, MA 02127.
Circle 401

Filtered power module

The series FPM incorporates an IEC power input receptacle, on/off switch, fuse protection, emi filter, and a voltage selector. Isolation of the line and load wiring is provided by an emi filter directly at the input source. The IEC connector, together with the emi filter, eliminates virtually all coupling of the module. It uses either a 5-mm or standard ¼ x 1¼ fuse; the voltage selector provides 120- or 250-Vac operation. Prices start at $17.88 in 100-piece lots. **Stanford Applied Engineering, Inc,** 340 Martin Ave, Santa Clara, CA 95050.
Circle 402

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Left to right, Fred Molinari, President

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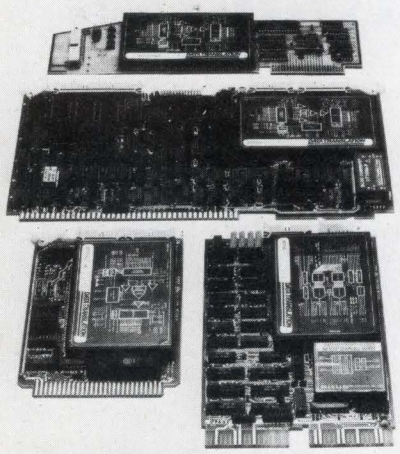

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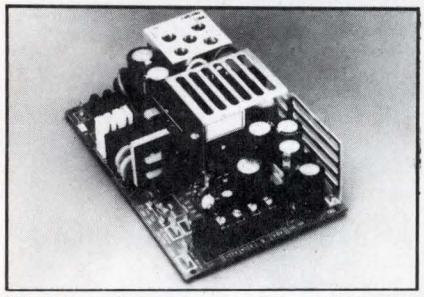
CIRCLE 145

Triple-output switcher



Model KFD-40E meets UL/CSA and international safety specs IEC 380 and VDE 0806. The 40-W dual-input unit is available with three outputs of 5 V at 5 A, 12 V at 2.5 A, and −12 V at 0.5 A. For emi, it complies with FCC level B and VDE 0871 level B. Applications include CRT terminals and modems. The 25-piece price is $74. **KEC Electronics, Inc,** 20817 Western Ave, Torrance, CA 90501.
Circle 403

Dual-mode suppression filters

The devices provide control of line to ground noise and reduce low frequency line to line noise and transients. They will protect equipment from malfunctions due to conducted interference coming into the equipment from the line. Specs include rated voltage 115/250 Vac; rated frequency 50/60 Hz, 0.50 mA; and line to ground at 250 Vac/50 Hz, 1 mA. The filters are designed to meet UL and CSA standards. **RTE Aerovox, Inc,** 740 Belleville Ave, New Bedford, MA 02745.
Circle 404

Rechargeable lead-acid battery

Model PS-12150 is a 12-V unit with 1.3 W-h/cubic in. Sealed construction lets the battery be used in any position. The 15 A-h battery fills a gap between the 10- and 20 A-h capacities. Applications include UPS systems, telecommunication equipment, standby power for micro-based devices, and alarm systems. The battery weighs 12.8 lbs, can be recharged 300 to 400 times, and has a life expectancy of over 5 years. **Power-Sonic Corp,** PO Box 5242, Redwood City, CA 94063.
Circle 405

Power transistors

Faster than comparable bipolar transistors, Power MOS devices function as majority carrier devices without storage time. Voltage drive requirements are just above threshold; high input impedance allows a voltage generator to drive them. The generator need only provide adequate charge of the input capacitance. The devices use an n-channel structure with multiple square cells. Twenty-eight types cover nine voltage ranges from 50 to 400 V. Prices in 1000-piece quantities range from $0.62 to $1.95. **SGS Semiconductor Corp,** 1000 E Bell Rd, Phoenix, AZ 85022.
Circle 406

Chip with negative voltage levels

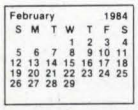
With two external capacitors, the TSC7660 converts a 1.5- to 10-V input signal to a 1.5- to −10-V level. It allows 5-V digital logic systems to incorporate analog components without adding an additional main power source. The chip charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across output. The negative open circuit output voltage is within 0.1 percent of the positive input voltage. Available in 8-pin DIPs, prices range from $1.90 to $8. **Teledyne Semiconductor,** 1300 Terra Bella Ave, Mountain View, CA 94043.
Circle 407

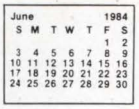
Lithium power cells

The AL2-AA cells offer high performance, long life, and safety of lithium thionyl chloride batteries in a standard AA package. They feature durable stainless steel construction and a ceramic to metal seal for reliable operation. Cells deliver a standard open circuit voltage of 3.6 V and have a shelf life of more than 10 years. They are unaffected by spin, altitude, or position. Nominal capacity is 2 A-h at the 23-mA rate at 20 °C to a 2.5-V cutoff. **Altus Corp,** 1610 Crane Ct, San Jose, CA 95112.
Circle 408

March Preview
Special Report on Advanced Digital ICs

CALENDAR





CONFERENCES

FEB 28-MAR 1—Compcon/Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAR 12-15—Interface, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: Richard Katzeff, The Interface Group, Inc, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

MAR 12-16—Internat'l Conf on Robotics, Atlanta Hilton, Atlanta, Ga. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAR 19-21—Phoenix Conf on Computers and Communications, Phoenix Hilton, Phoenix, Ariz. INFORMATION: David Gretton, Digital Equipment Corp, 2500 W Union Hills Dr, Phoenix, AZ 85027. Tel: 602/869-5273

MAR 25-28—Numerical Control Society Technical Conf and Expo, Queen Mary, Long Beach, Calif. INFORMATION: Lisa Schultz, Numerical Control Society, 111 E Wacker Dr, Suite 600, Chicago, IL 60601. Tel: 312/644-6610

MAR 26-30—Internat'l Conf on Software Engineering, Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 2-5—Test & Measurement World Expo, Brooks Hall, San Francisco, Calif. INFORMATION: Meg Bowen, Interfield Publishing Co, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

APR 4-11—Hannover Fair, Hannover, West Germany. INFORMATION: Delia Assocs, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

APR 5-7—Comdex/Winter, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

APR 10-12—Infocom, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 18-20—Optical Data Storage, Monterey Convention Ctr, Monterey, Calif. INFORMATION: Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. Tel: 202/223-8130

APR 24-27—Compdec (Internat'l Conf on Data Engineering), Bonaventure Hotel, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 25-27—Friendly Systems: 1984 or 2001? Sheraton-Atlanta, Atlanta, Ga. INFORMATION: Donald Chand, Dept of Information Systems, Georgia State Univ, Atlanta, GA 30303. Tel: 404/658-3886

APR 30-MAY 2—Workshop on Computer Vision, Hilton Hotel, Annapolis, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

MAY 13-17—Computer Graphics, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

MAY 14-17—Internat'l Conf on Communications, Congresscentrum Rai, Amsterdam, The Netherlands. INFORMATION: K. Teer, Philips Research Lab, 5600 MD Eindhoven, The Netherlands.

MAY 15-17—Electro, Bayside Exposition Ctr and Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 15-17—Mini/Micro-Northeast, Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 22-25—Comdex/Spring, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

JUNE 4-8—SID (Society for Information Display Internat'l Symposium), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

JUNE 5-7—Internat'l Symposium on Computer Architecture, Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-8517

JUNE 5-7—Symposium on Mass Storage Systems, Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. Tel: 303/494-5151

JUNE 6-8—Communications Architectures and Protocols, Montreal, Canada. INFORMATION: Rebecca Hutchings, Honeywell/FSD, 7900 Westpark Dr, McLean, VA 22102. Tel: 703/827-3982

JUNE 19-22—Internat'l Symposium on Fault Tolerant Computing, Hyatt Orlando, Orlando, Fla. INFORMATION: Richard Sedmak, Sperry Univac, PO Box 500, MS C1SW12, Blue Bell, PA 19404. Tel: 215/542-3638

JUNE 24-27—Design Automation Conf, Albuquerque Convention Ctr, Albuquerque, NM. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 9-12—National Computer Conf, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 23-27—Siggraph Conf on Computer Graphics and Interactive Techniques, Minneapolis, Minn. INFORMATION: Lynn Valastyan, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

JULY 30-AUG 2—Internat'l Pattern Recognition Conf, Montreal, Canada. INFORMATION: ICPR Secretariat, 3450 University St, Montreal, Quebec, Canada H3A 2A7. Tel: 514/392-6744

SHORT COURSES

MAR 12-14—Distributed Telecommunications Networks; MAR 12-14—Fiber Optic Systems Design; AND MAR 15-16—Public and Private Packet Switched Networks: The X.25 Protocol, Orlando, Fla. INFORMATION: Continuing Engineering Ed, George Washington Univ, Washington, DC 20052. Tel: 202/676-6106; 800/424-9773 (outside DC)

MAR 26-29—Personal Computer Interfacing and Scientific Instrument Automation, Virginia Tech, Blacksburg, Va. INFORMATION: Linda Leffel, CEC, Virginia Polytechnic Institute and State Univ, Blacksburg, VA 24061. Tel: 703/961-4848

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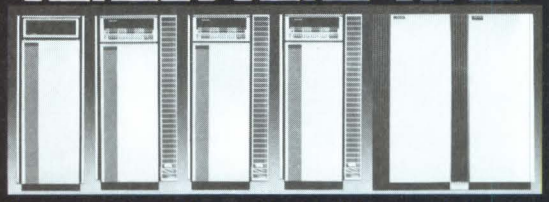

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CIRCLE 147

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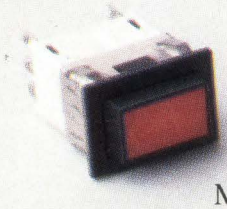

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CIRCLE 148

Scope measurement system
Brochure discusses guidelines for developing an automatic testing strategy, and tracks the role of the HP 1980 scope in an automatic test environment. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 410

Isolated input MUX
Data sheet summarizes essentials of DMS504; plug compatible with LSI-11, Multibus, IEEE 488, and RS-232/RS-422 formats, the unit handles input voltages of ±5 mV to ±10.24 V full scale. **DI-AN Micro Systems, Ltd,** Cheshire, England.
Circle 411

Flat-panel switches
Ordering catalog gives technical and application background for RAFI 15/19 dust and waterproof push buttons, accompanied by construction and dimensional drawings. **Ledex Inc,** Vandalia, Ohio.
Circle 412

Macrocell library
Software data book has tools for semicustom design of LSI LL5000 series gate arrays on Daisy Systems Logician, Mentor Graphics Idea 1000, and Valid Logic SCALDsystem engineering workstations; macrocell model data sheets, tutorial documentation, and information on gate array design rules are included. **LSI Logic Corp,** Milpitas, Calif.
Circle 413

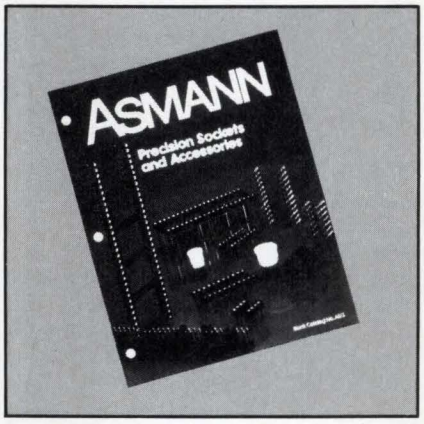
Modular switches
Brochure highlights momentary and alternate versions in various keycaps and bezels, covering cross sections, specs, function-principles, and wiring diagrams. **MEC, Electronic Components Group,** Minneapolis, Minn. **Circle 414**

Cards for STD bus
More than 35 cards are featured in 16-page catalog detailing Approach series microcomputers for machine control and Romaid 2704 programmer/simulator for software debugging. **Micro-Link Corp,** Carmel, Ind.
Circle 415

Digital panel meters
Selection guide covering 22 manufacturers tabulates about 80 panel meter features as they relate to specific applications; typical listings include scaling adjustments, control outputs, data formats, mounting techniques, display types, and reliability considerations. **Nationwide Electronic Systems, Inc,** Streamwood, Ill.
Circle 416

Circuit data to CAD/CAM
Application note describes how to transfer circuit information from typical CAD/CAM systems to automatic testers, as well as how to generate circuit files offline. **Advanced Microcomputer Systems, Inc,** Coral Springs, Fla.
Circle 417

Custom resistor networks
Eight-page technical bulletin details specs for axial lead, high reliability, lug terminal, subminiature, and printed circuit type resistors, following up with circuit applications and diagrams for encapsulated networks. **Armtec Industries, Inc,** Manchester, NH. **Circle 418**

Sockets and assemblies


Ordering catalog lists over 200 Asmann components, including DIP, test and transistor, and LED/LCD sockets; carrier assemblies; and contact terminal strips. Precision sockets fit standard DIPs with 0.100- x 0.100-in. pin spacing. **ebm Industries, Inc,** Unionville, Conn.
Circle 419

Molded disconnects
Bulletin describes continuously molded, fully insulated female Pan-Term units supplied on 3000-piece reels for wire ranges from 22 to 14 AWG. **Panduit Corp,** Tinley Park, Ill. **Circle 420**

Data communication equipment
Short-form catalog outlines full line of network testers, protocol analyzers, and patching/switching products. **Atlantic Research Corp,** Alexandria, Va.
Circle 421

Professional plotters
Folder features Hiplot DMP-41 and -42 models, listing firmware commands as well as operating and electrical/mechanical specs. **Houston Instrument,** Austin, Tex. **Circle 422**

Pancake synchros and resolvers
Technical folder contains representative specs, mechanical configurations, schematics, and mounting requirements for 19 high accuracy models. **Harowe Servo Controls, Inc, AC Operation,** West Chester, Pa.
Circle 423

Transmission line assemblies
Twenty-page source book covers design and testing of multiple- and single-signal assemblies and accessories; chart cross-references part numbers with cable, connector, and measurement data. **Chabin Corp,** Chico, Calif.
Circle 424

Unix ported to minicomputer
Four-page leaflet outlines Unix System III implementation in dataCASE/5, which offers over 1-MIPS performance, 560-Mbyte storage, and 5-Mbit/s data transfer. **Computer Automation, Naked Mini Div,** Irvine, Calif.
Circle 425

Ceramic disks and capacitors
Forty-page catalog provides detailed specs and performance curves for low voltage, temperature compensating, rectangular plate, and medium to Hi K, as well as disk and high voltage, ceramic capacitors. **Murata Erie North America, Inc,** Marietta, Ga.
Circle 426

Test and measurement
Eighty-page catalog features 13 scopes including a 100-MHz, four-channel and a 50-MHz, two-channel dual time base model, along with four frequency counters ranging from 80 MHz to 1 GHz. **Leader Instruments Corp,** Hauppauge, NY. **Circle 427**

Low cost PC drafting system
Specs and detailed price list summarize IBM XT/PC 68000 two-dimensional drafting system with three-dimensional modeling, which is also compatible with the full range of PC software. **Summit CAD Corp,** Houston, Tex.
Circle 428

Portable test equipment
Six-page folder features the Tracer-2 signature analyzer, which generates a characteristic waveform pattern on a 2.5-in. CRT; the 3-lb miniscope MS-230 and other portable testers are also outlined. **Non-Linear Systems, div of Kaypro Corp,** Solana Beach, Calif.
Circle 429

Coaxial cable assemblies

Full-line, 120-page catalog gives electrical, mechanical, and environmental data for subminiature and miniature connectors, along with field-replaceable launchers and semi-rigid cable assemblies. **Applied Engineering Products Inc,** New Haven, Conn.
Circle 430

Thin-film hybrids

Product summaries, electrical and mechanical specs, outline drawings, and ordering information come in a 16-page booklet summarizing chip resistors, chip networks, packaged networks, substrates with conductors, and substrates with resistors. **Hybrid Systems Corp,** Billerica, Mass.
Circle 431

Instrumentation computer

Booklet features six pages of hardware and software specs for multitasking model 6000, with applications in instrument control, industrial automation/test, military/aerospace, and manufacturing. **Wavetek, Inc,** San Diego, Calif.
Circle 432

Card connectors

Technical data describes and specifies DIN 41612 printed circuit card connectors in styles B, C, and D; drilling layouts and prices are included in 12-page catalog. **Amlan Inc,** Stamford, Conn.
Circle 433

Video course in VLSI design

Brochure describes introductory VLSI design course, which deals with principles and techniques through first silicon. Course consists of 17 color videotapes, study guide, and textbook. **Massachusetts Institute of Technology, Center for Advanced Engineering Study,** Cambridge, Mass.
Circle 434

Electronic components

The 160-page 1984 catalog contains specs, performance curves, and dimensional drawings for over 12,000 in-stock items. **Mouser Electronics,** Santee, Calif.
Circle 435

Read-only CMOS memories

Twenty-page brochure lists complete line of mask-programmable ROMs, detailing pinout diagram and significant features for each basic type. **RCA/Solid State Div,** Somerville, NJ.

Open frame linear power

Eight-page brochure lists complete electrical/mechanical specs and tabulates voltage/current ratings for Universal series. **ACDC Electronics,** Oceanside, Calif. **Circle 437**

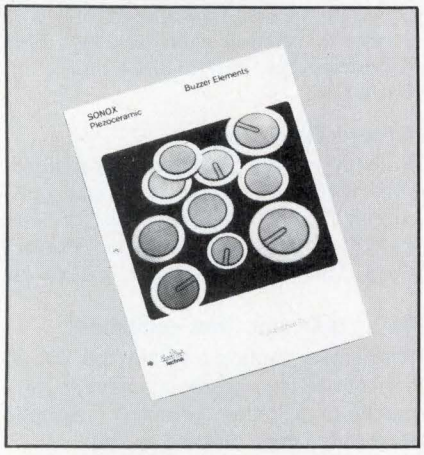
Idris application software

Third-party directory lists over 20 application packages running under Unix look-alike operating system; also included are product profiles, hardware requirements, and prices/ordering information. **Whitesmiths, Ltd,** Concord, Mass.
Circle 438

Stock relays

Forty-page bulletin describes physical and electrical characteristics of reed, solid-state, hybrid, sensitive, and power relays; selection guide identifies switching capabilities, coil voltage ranges, contact styles, and series number. **Sigma Instruments, Inc,** Braintree, Mass.
Circle 439

Piezoelectric buzzers



Six-page bulletin gives spec charts and technical diagrams for electronic buzzer elements, covering styles, dimensions, characteristics, mounting modes, resonator frequency formula, and driving circuits. **Rosenthal Technik North America, Inc,** Providence, RI.
Circle 440

Equipment for emi/emc

Fifty-two page guide describes and specifies over 500 items from major manufacturers; reference section lists handbooks on emi/emc technology. **Tucker Electronics Co,** Garland, Tex.
Circle 441

Solid state relays

Miniature units rated at 25 A, 120/240 Vac are subject of six-page brochure that gives engineering specs, dimensional and wiring diagrams, and current/surge graphs. **Grayhill, Inc,** La Grange, Ill.
Circle 442

Storage management

A 486-page handbook presents a line of controllers and support devices for Winchester and floppy disks, as well as Winchester board and main memory products; items feature proprietary VLSI and are compatible with SASI, Multibus, general purpose, and custom interfaces. **Western Digital Corp,** Irvine, Calif. **Circle 443**

Local area networks

Thirteen-page booklet explains access methods and environmental factors involved in selecting a LAN, discussing 10-Mbit/s UniLAN in detail; baseband, broadband coaxial, and fiber optic cable are covered. **Applitek Corp,** Wakefield, Mass. **Circle 444**

Technical overview of Z8

Twenty-three page booklet on single-chip microcomputer family describes entire line of circuits and support products, including development module and Z-Scan 8 in-circuit emulator. **Ziiog, Inc,** Campbell, Calif. **Circle 445**

Microcircuit packaging

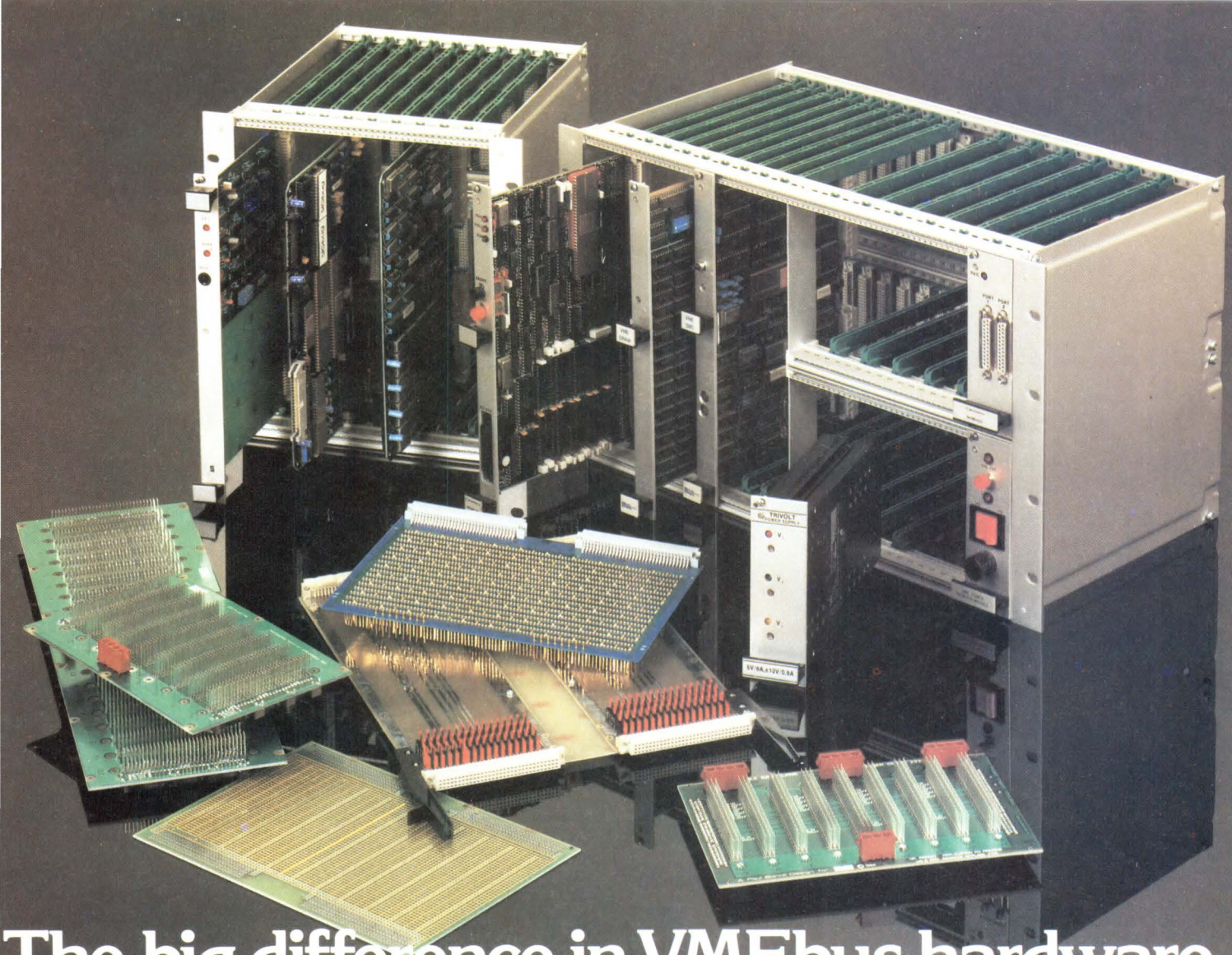
Illustrated short-form catalog explains design, production, packaging, and applications for DIPs, solid sidewalls, TO-5 and TO-8 headers, all-metal flats, and power hybrids. **Airpax Corp,** Cambridge, Md. **Circle 446**

Slide-on coaxial connectors

Sixteen-page brochure outlines design features, sizes, electrical properties, and performance of miniature to subminiature connectors. **Sealectro Corp, RF Components Div,** Mamaroneck, NY.
Circle 447

Variable-frequency ac

Folder profiles family of Class D ac power sources; performance specs for standard 12- to 72-kVA models in single- and triple-phase versions are included. **Helionetics, Inc,** Irvine, Calif.
Circle 448



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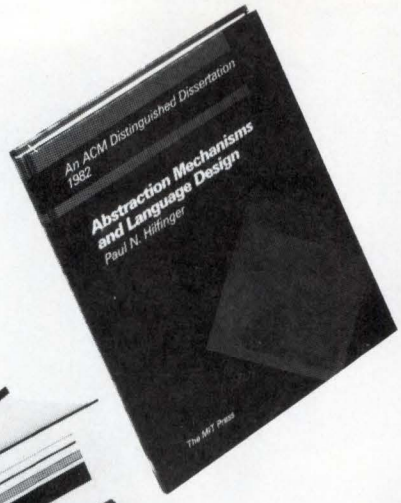

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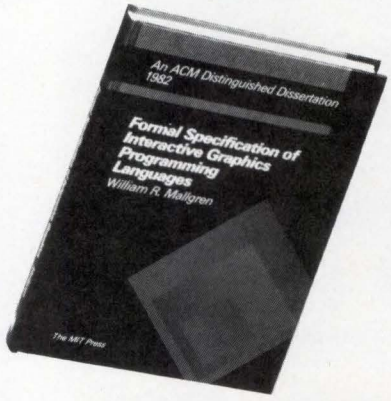

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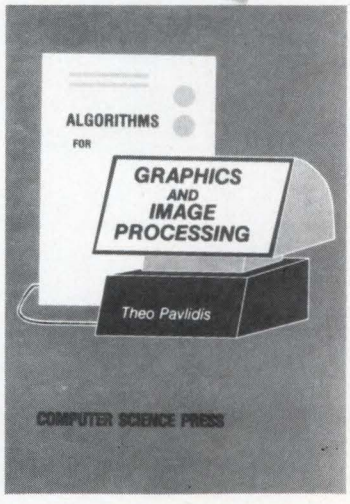

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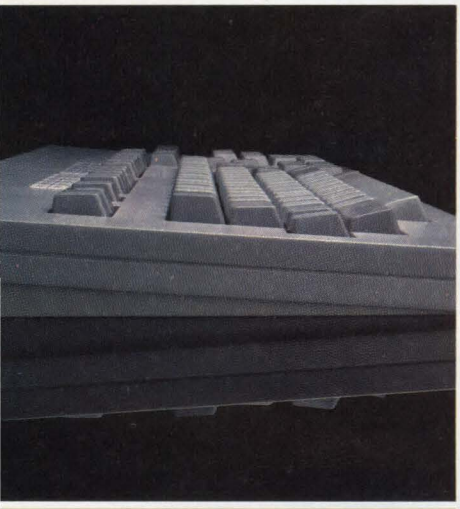
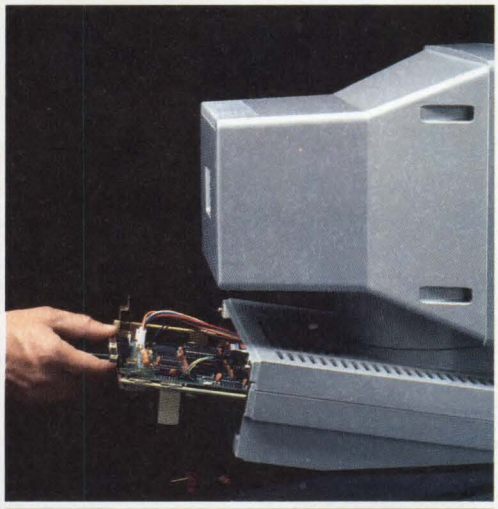
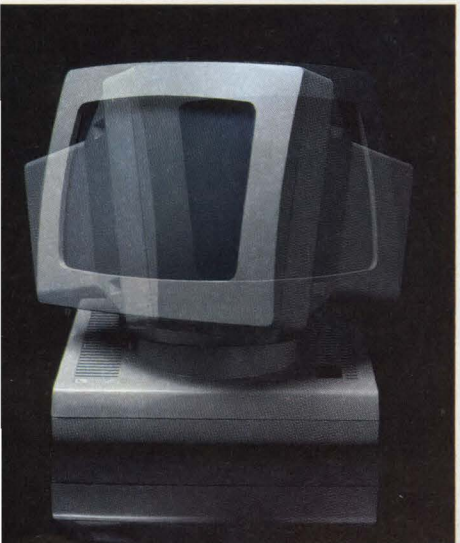
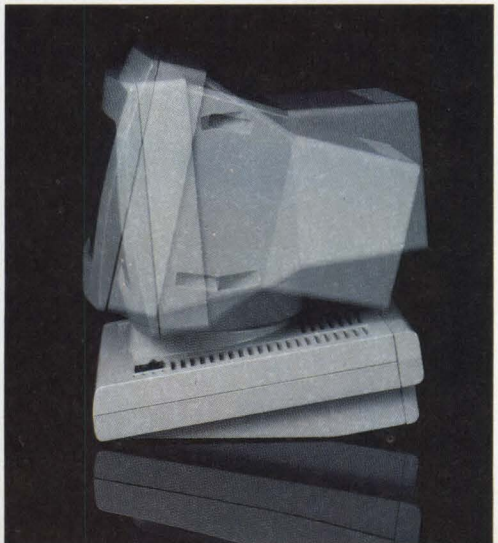
Computer Science Press, 1982, 416 pages, ISBN 0-91489465-X, $26.95 **Circle 459**









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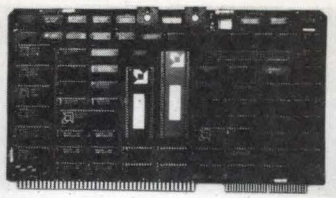

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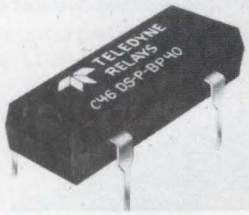

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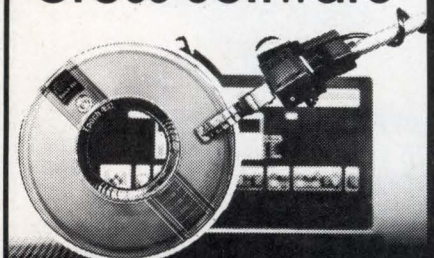

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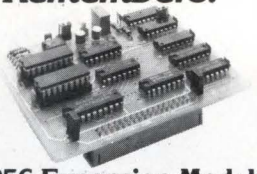

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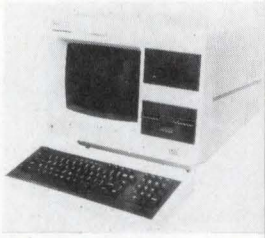

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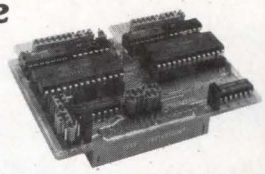

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SERIAL-2S Expansion Module

For low cost serial communication with system peripherals

- Two independent RS-232C compatible ports
- Based on popular 8251A USARTs
- Uses baud generation circuitry of host single board computer
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Expansion modules for all requirements

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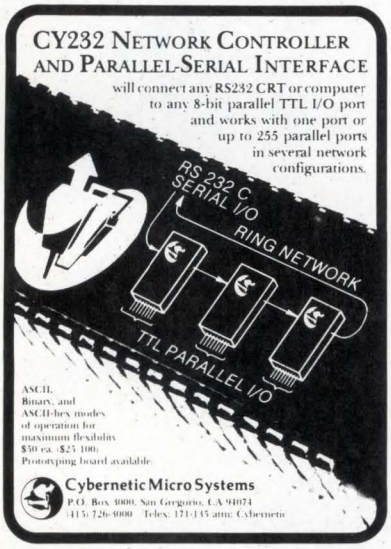
CY232 Network Controller and Parallel-Serial Interface

will connect any RS232 CRT or computer to any 8-bit parallel TTL I/O port and works with one port or up to 255 parallel ports in several network configurations.



ASCII, Binary, and ASCII-hex modes of operation for maximum flexibility
$50 ea. ($25 100)
Prototyping board available

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P.O. Box 3000, San Gregorio, CA 94074
(415) 726-8080 Telex: 171-115 attn: Cybernetic

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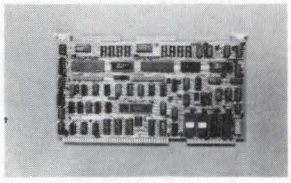

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All-CMOS MULTIBUS* compatible using NSC 800 CPU. OP-Code compatible with Z80**, 8085 and 8080. 4, 28-pin RAM/ROM sockets backed-up with lithium battery for non-volatility. Expandable to 8 sockets. 2 iSBX*-compatible connectors. 48 parallel I/O, 1 serial port, 12 interrupts. 150ma @ 5V. $950 single piece w/8K RAM. Contact Bill Long, **DIVERSIFIED TECHNOLOGY,** P.O. Box 748, Ridgeland, MS 39157. (601) 856-4121.
*TM Intel. **TM Zilog.

CMOS Board Computer

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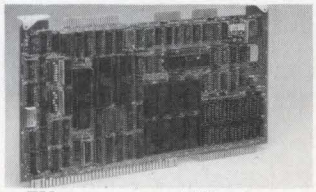

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Z8001 or Z8002 16-bit CPU (6 MHz); 32K or 128K DRAM (upgradable to 512K); up to 48K static RAM or EEPROM; up to 128K EPROM; 2 RS-232 ports (Z8030 SCC); 40 parallel I/O lines and six 16-bit counter-timers (Z8036 CIOs); vectored interrupts; two 8-bit DIP switches. EPROM resident Debug Monitor, MICRO CONCURRENT PASCAL, C, FORTH, VRTX. Develop Z8000 software on your IBM PC, PDP-11, Intel MDS, Olivetti M20 or any 8080/Z80 CP/M system. Z8000™ Zilog, Multibus™ Intel Corp. **SINGLE BOARD SOLUTIONS,** 7669 Rainbow Drive, Cupertino, CA 95014. (408) 253-0181

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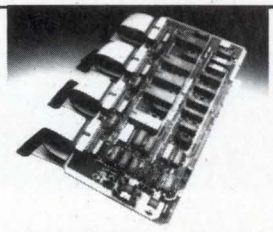

MULTI-PORT SERIAL CARD FOR S-100 (IEEE-696) SYSTEMS

Designers who need an IEEE-696 serial interface card have a choice of either 2 or 4 ports with the Multi-Port Serial Card. Each port can operate as either a "data set" or as a "data terminal." Independent baud rate generators for each port (50—19.2k baud) and an 8-level vectored interrupt controller are provided. 36" cables are included. Single Qty: $280.00 (4-port), $210.00 (2-port). **SEATTLE COMPUTER PRODUCTS, INC,** 1114 Industry Dr, Seattle, WA 98033. Tel: 1-800-426-8936.

Dealer and OEM inquiries are invited.

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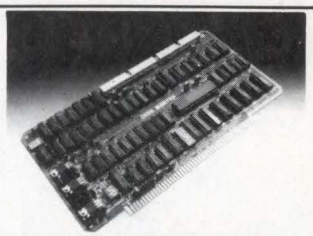

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Disk Master™ by Seattle Computer controls as many as four 8" and four 5.25" floppy disk drives simultaneously, in any combination. It can be configured for virtually any floppy disk drive on the market. The Disk Master based on the 1793 disk controller chip. It is fully IEEE-696 compatible and can be used with CPU's operating to 10 MHz. Single quantity: $325.00. Dealer and OEM inquiries are invited. **SEATTLE COMPUTER PRODUCTS, INC,** 1114 Industry Drive, Seattle, WA 98033. Tel: (800) 426-8936.

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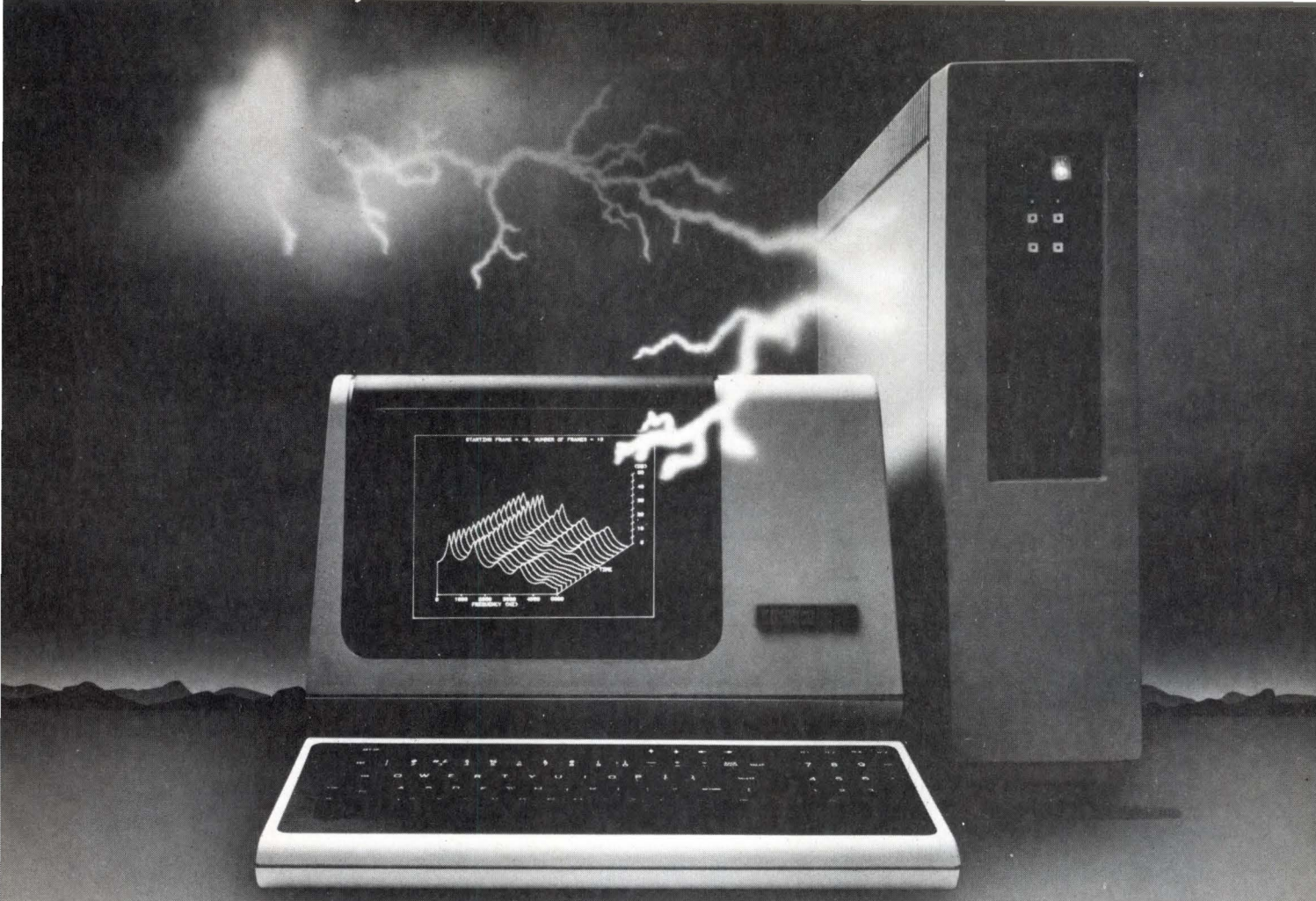

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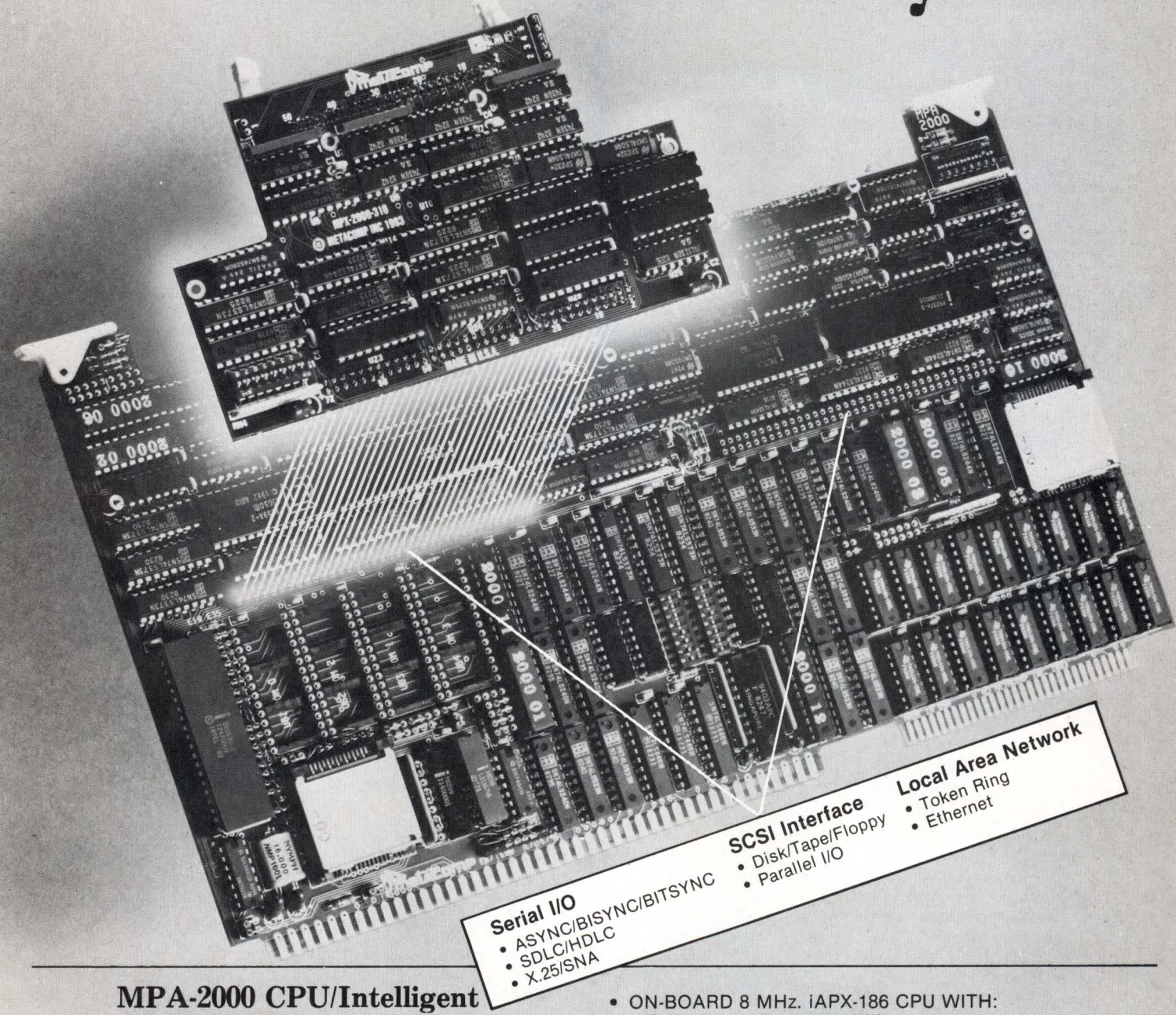
AD INDEX

High Performance Multibus* Modularity



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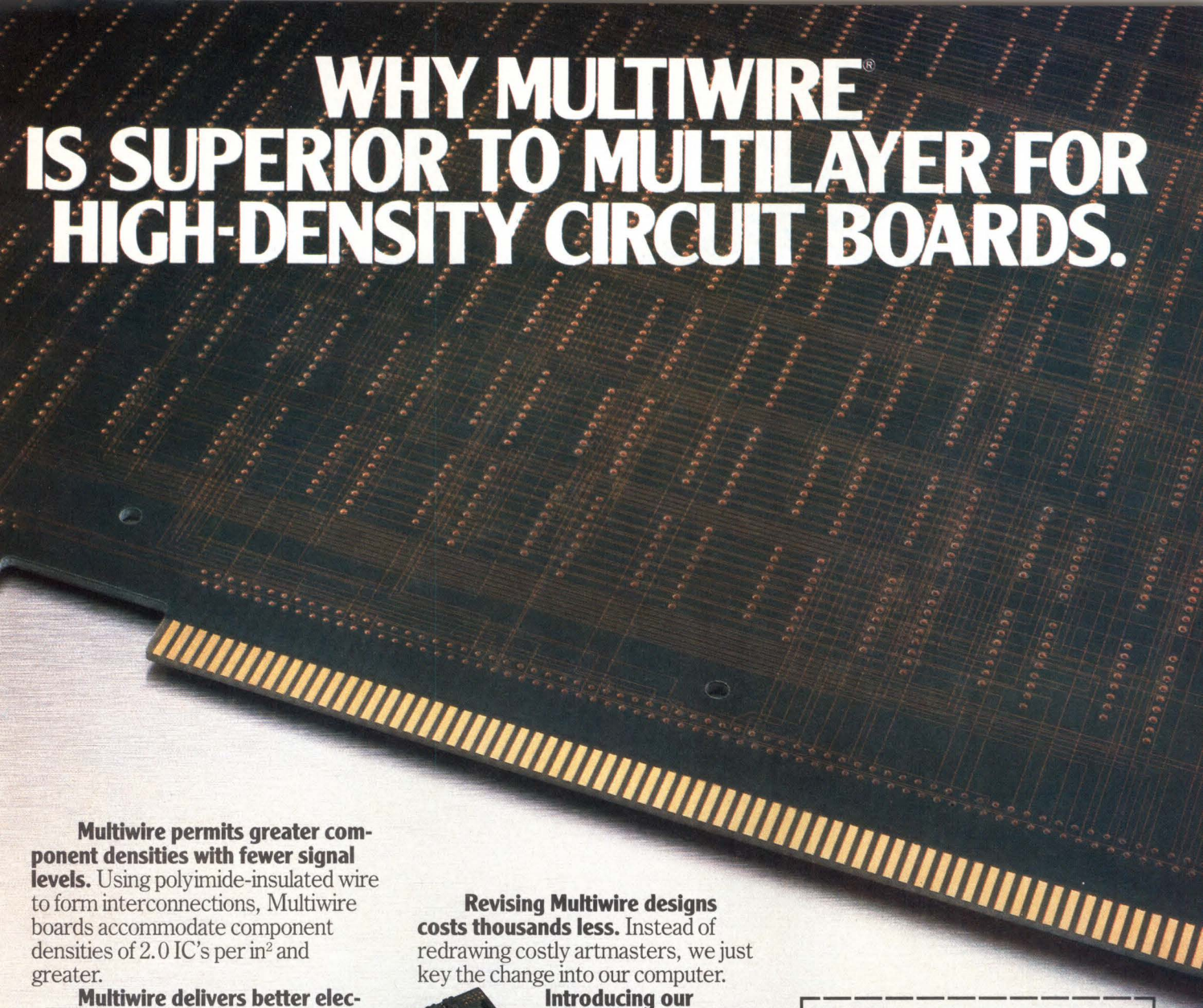
AD INDEX

AD INDEX

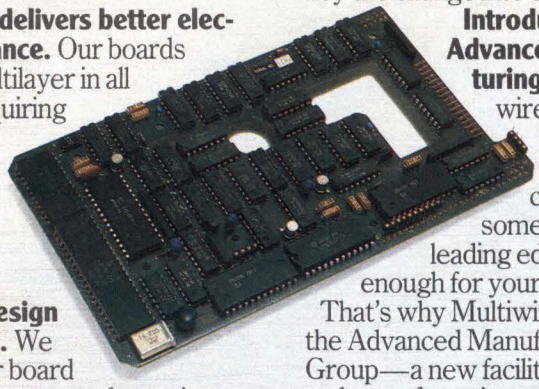
*Domestic Issues Only

WHY MULTIWIRE® IS SUPERIOR TO MULTILAYER FOR HIGH-DENSITY CIRCUIT BOARDS.



Multiwire permits greater component densities with fewer signal levels. Using polyimide-insulated wire to form interconnections, Multiwire boards accommodate component densities of 2.0 IC's per in^2 and greater.

Multiwire delivers better electrical performance. Our boards outperform multilayer in all applications requiring tight-tolerance on impedance controlled transmission lines.



Multiwire shortens the design cycle by weeks. We can design your board from as little input as a schematic or net list, reducing your in-house design time. And when you make revisions, you'll get new boards back in days instead of weeks.

Revising Multiwire designs costs thousands less. Instead of redrawing costly artmasters, we just key the change into our computer.

Introducing our Advanced Manufacturing Group. Multiwire technology provides the most advanced circuit boards. But sometimes even our leading edge designs are not enough for your requirements. That's why Multiwire has established the Advanced Manufacturing Group—a new facility with design and manufacturing specialists dedicated to solving the interconnection problems for your next generation of products. To learn more, just fill out and return the coupon.

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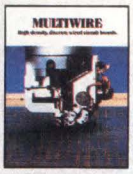

- ☐ Please send me your 8-page brochure.
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DATACHECK II
THE ULTIMATE BREAKOUT BOX

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- Top to bottom functional panel layout.
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- LED's separated by signal source (DTE and DCE sides).
- Pocket-size, illustrated operators manual.
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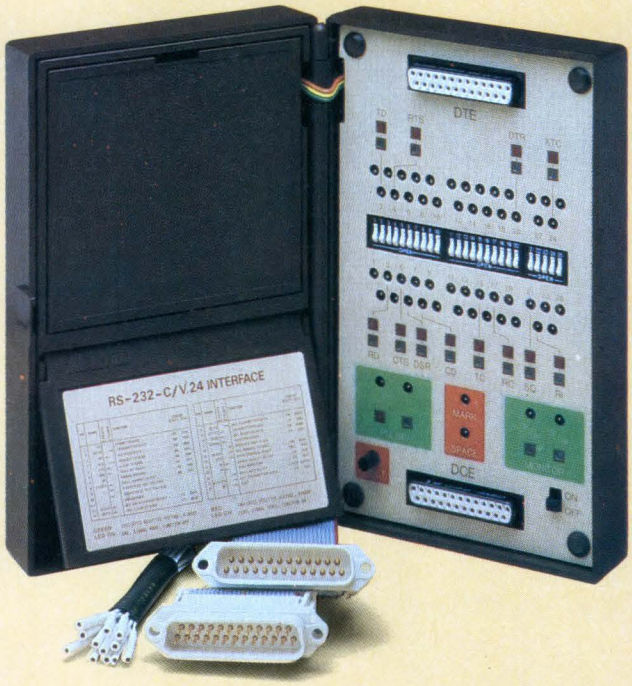
RELIABLE

- Power off/reset button (conserves battery life).
- Molded ABS plastic case with metal hinge for durability.
- Two 9 volt batteries.
- Separate compartment for cable and jumpers.
- Gold-plated recessed pins.



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ADDED FUNCTION

- Detachable RS-232C ribbon cable (connection flexibility).
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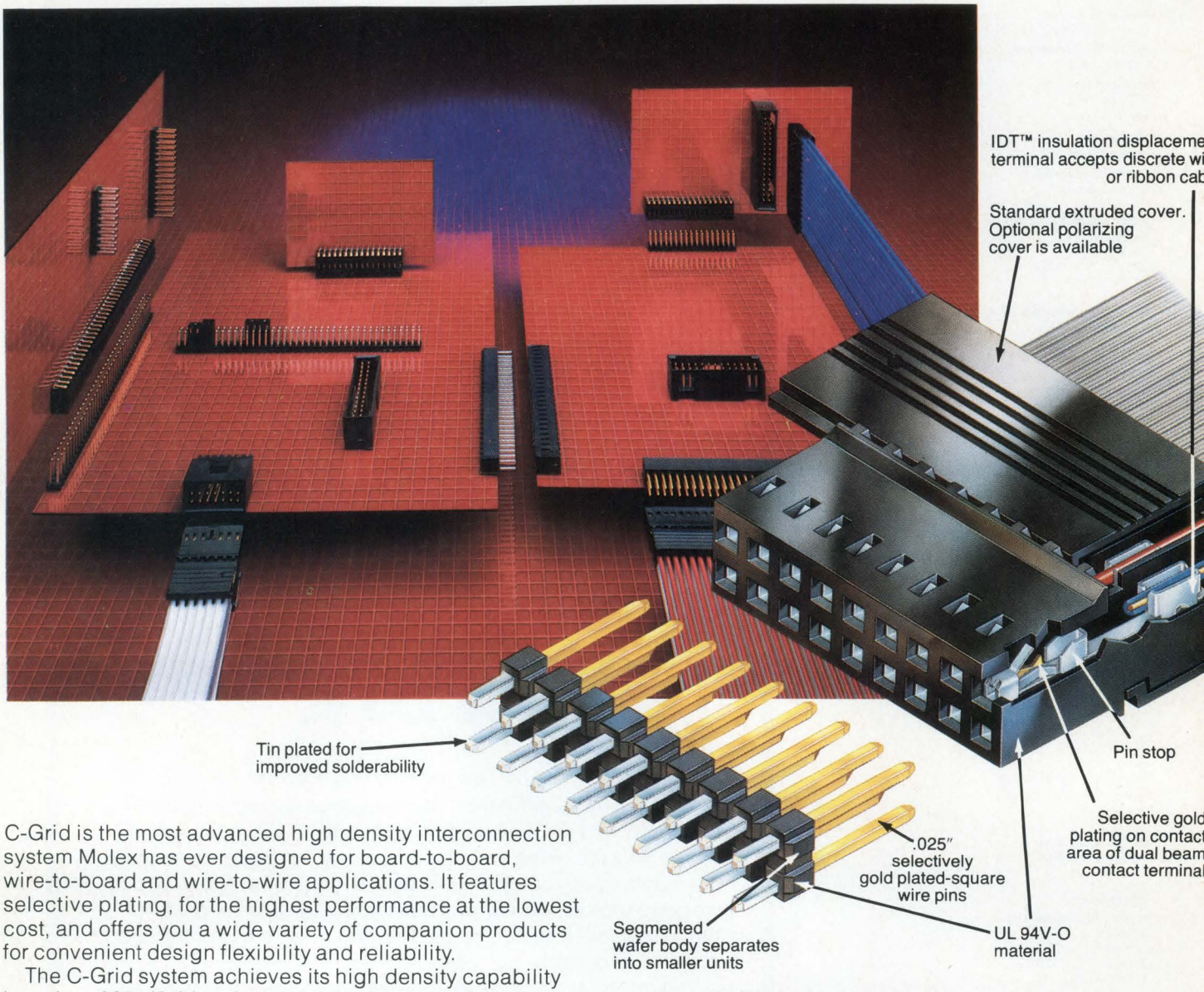
C-Grid: the Molex .100" x .100" PCB interconnection system.



C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

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Shrouded and unshrouded headers are available in straight and right-angle wafer bodies.

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Molex closed-or open-end shunts make it easier and less expensive to retrofit board circuitry by avoiding DIP switches.

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Virtual and physical address space of 4K words – standard. Expanded configuration uses a 4K cache memory to extend total memory to 64K words.

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Data I/O is supported by DMA transfers into data memory with a physical address space of 16 million words. A data memory page-loading feature provides the option of zero overhead background loading of data during time critical program execution. No DMA cycle stealing overhead is incurred. Uninterrupted processing can occur simultaneously with high-speed I/O transfers.

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FORTRAN compiler, linker, and trace/monitor provide high-level language access to the MARS-432.

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Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

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As the interface to the MARS-432 at run time, AREX provides processor initialization, I/O operations, and array function execution.

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CIRCLE 163

Network Designers— Introducing the simplicity of a Remote Procedure Call ...ACCES XNS.

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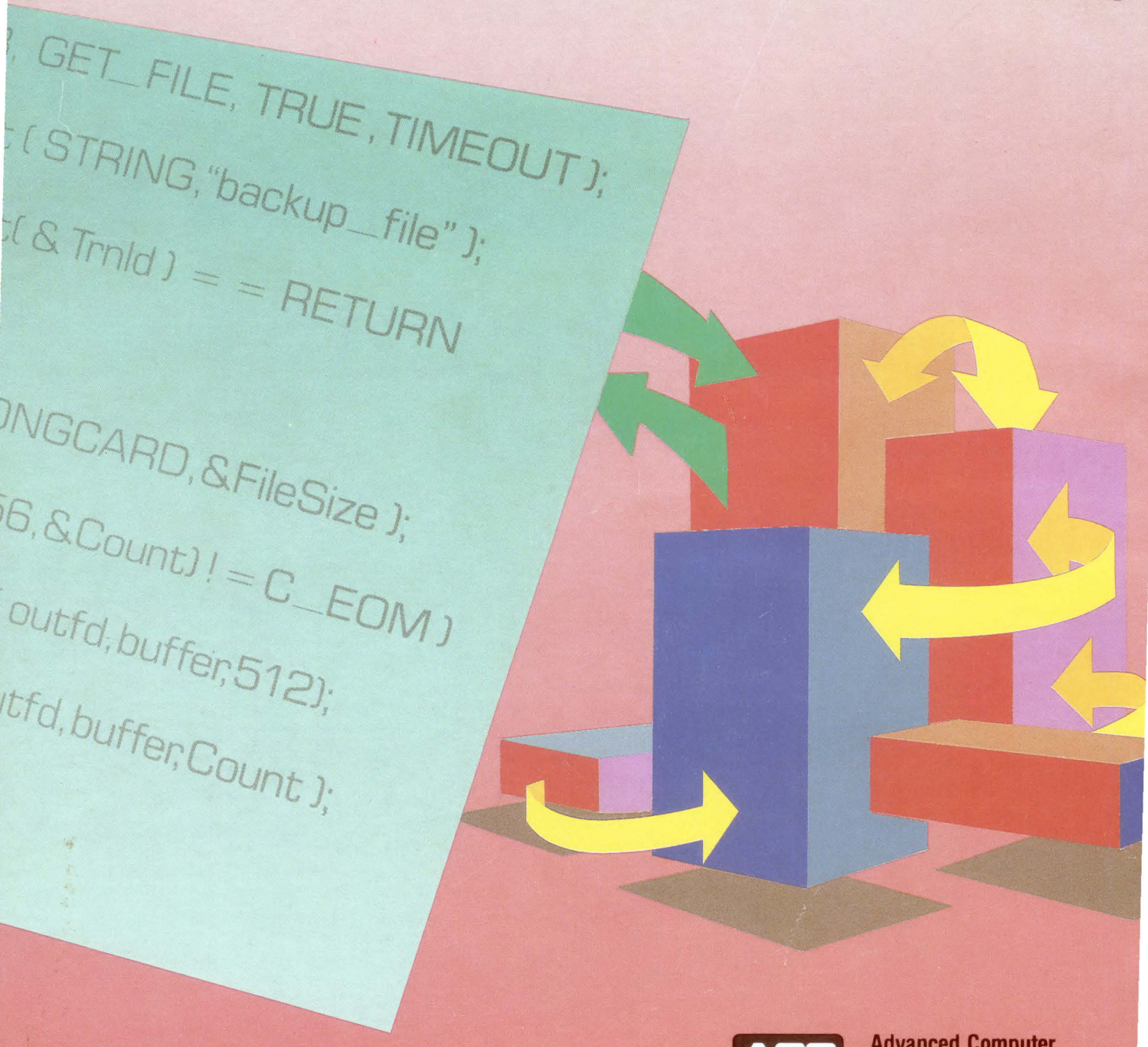
Whether you are responsible for designing a communication enviror ment around your company's product line, or interconnecting your company's computer resources, ACCES XNS meets your network design requirements.

To learn more about ACCES XNS, Courier, and Remote Procedure Calls, phone ACC at (805) 963-9431 and we'll gladly send you the ACCES XNS Brochure.

We Make Advanced Computers Communicate.



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